
STM32
CubeMX

1. Description

1.1. Project

Project Name	F407-EFALCON4
Board Name	custom
Generated with:	STM32CubeMX 6.2.1
Date	06/24/2021

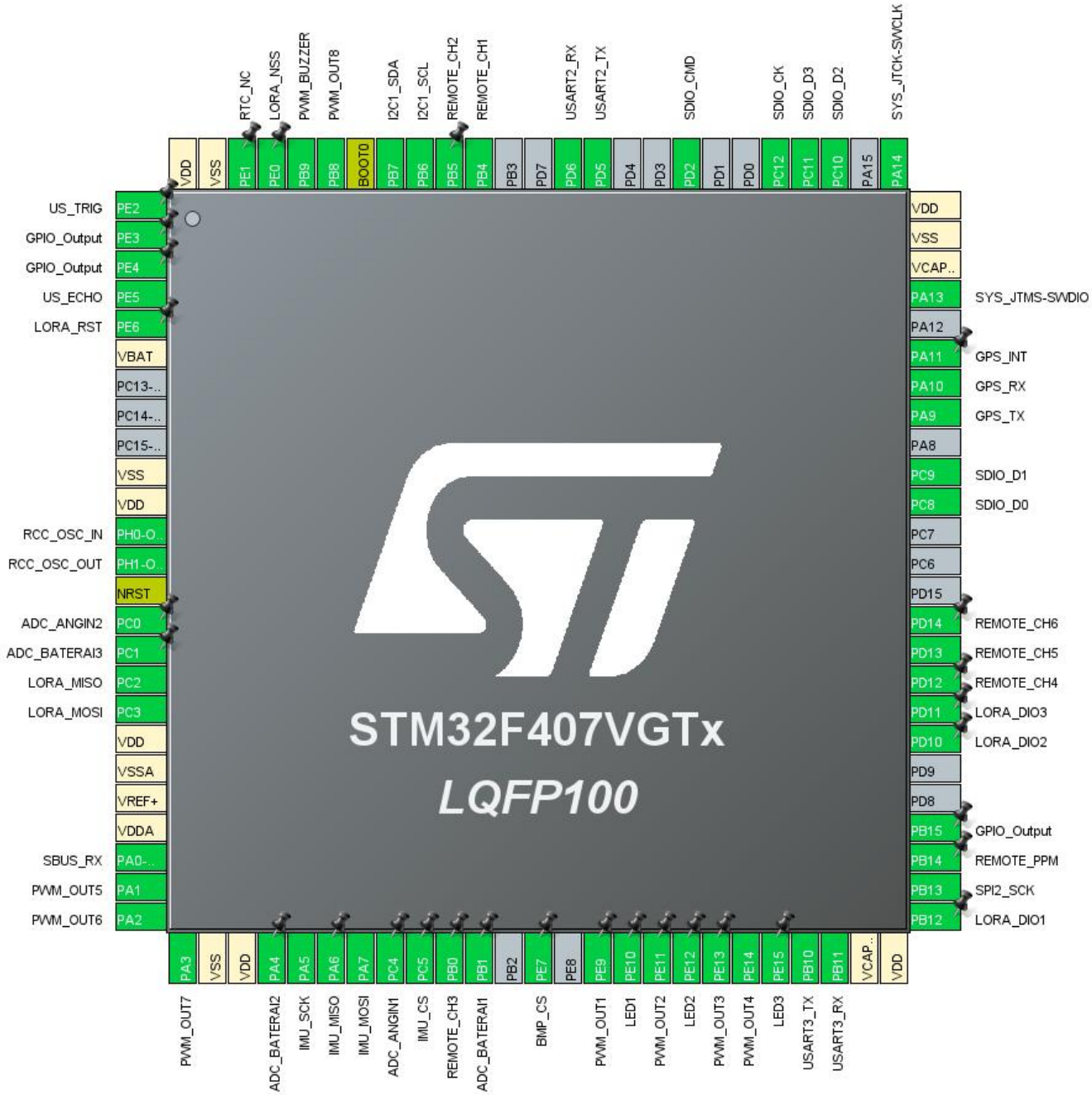
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407VGTx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



3. Pins Configuration

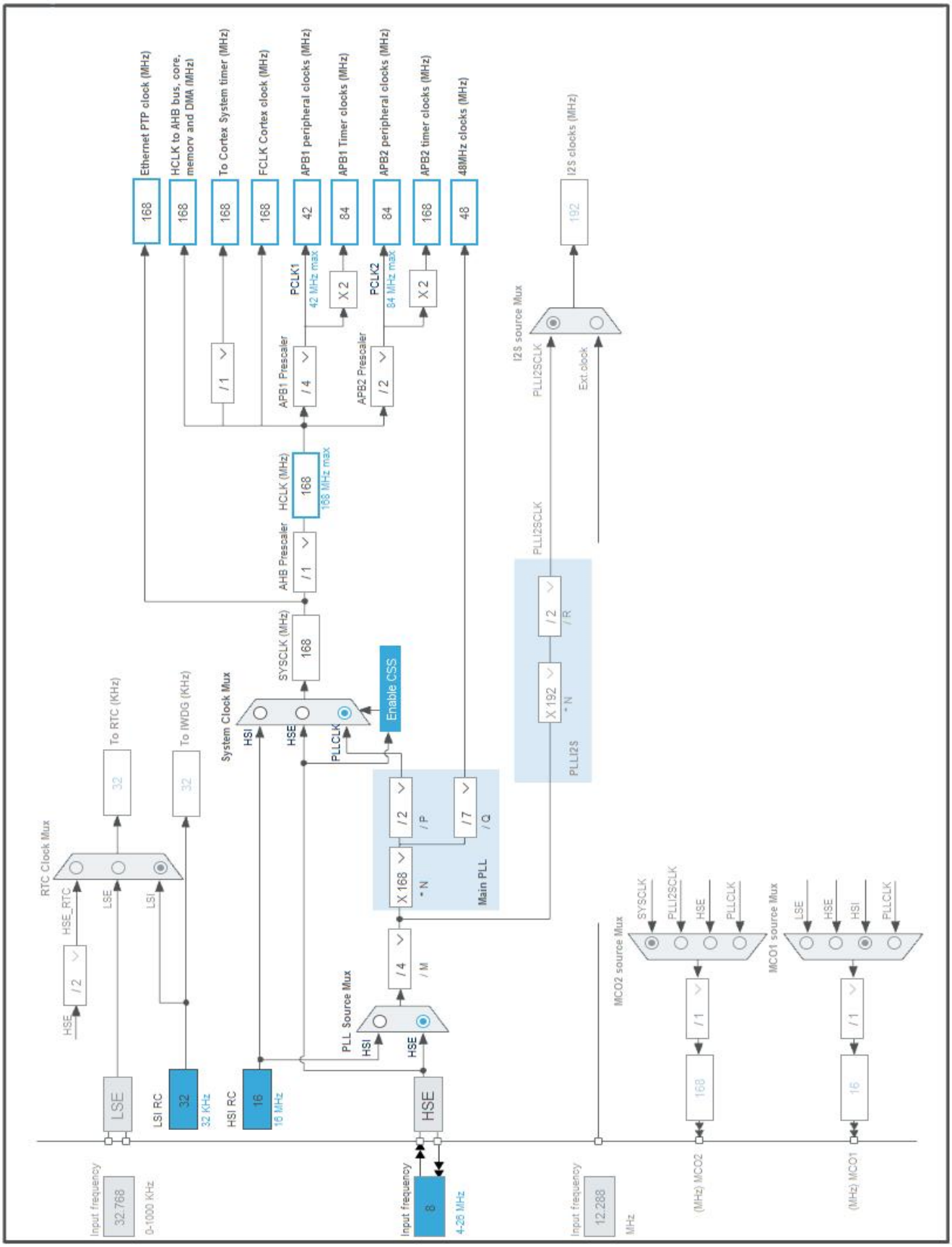
Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	US_TRIG
2	PE3 *	I/O	GPIO_Output	
3	PE4 *	I/O	GPIO_Output	
4	PE5	I/O	TIM9_CH1	US_ECHO
5	PE6 *	I/O	GPIO_Output	LORA_RST
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0	I/O	ADC1_IN10	ADC_ANGIN2
16	PC1	I/O	ADC1_IN11	ADC_BATERAI3
17	PC2	I/O	SPI2_MISO	LORA_MISO
18	PC3	I/O	SPI2_MOSI	LORA_MOSI
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	UART4_TX	SBUS_RX
24	PA1	I/O	TIM5_CH2	PWM_OUT5
25	PA2	I/O	TIM5_CH3	PWM_OUT6
26	PA3	I/O	TIM5_CH4	PWM_OUT7
27	VSS	Power		
28	VDD	Power		
29	PA4	I/O	ADC1_IN4	ADC_BATERAI2
30	PA5	I/O	SPI1_SCK	IMU_SCK
31	PA6	I/O	SPI1_MISO	IMU_MISO
32	PA7	I/O	SPI1_MOSI	IMU_MOSI
33	PC4	I/O	ADC1_IN14	ADC_ANGIN1
34	PC5 *	I/O	GPIO_Output	IMU_CS
35	PB0	I/O	TIM3_CH3	REMOTE_CH3
36	PB1	I/O	ADC1_IN9	ADC_BATERAI1
38	PE7 *	I/O	GPIO_Output	BMP_CS
40	PE9	I/O	TIM1_CH1	PWM_OUT1
41	PE10 *	I/O	GPIO_Output	LED1

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
42	PE11	I/O	TIM1_CH2	PWM_OUT2
43	PE12 *	I/O	GPIO_Output	LED2
44	PE13	I/O	TIM1_CH3	PWM_OUT3
45	PE14	I/O	TIM1_CH4	PWM_OUT4
46	PE15 *	I/O	GPIO_Output	LED3
47	PB10	I/O	USART3_TX	
48	PB11	I/O	USART3_RX	
49	VCAP_1	Power		
50	VDD	Power		
51	PB12 *	I/O	GPIO_Output	LORA_DIO1
52	PB13	I/O	SPI2_SCK	
53	PB14	I/O	TIM12_CH1	REMOTE_PPM
54	PB15 *	I/O	GPIO_Output	
57	PD10 *	I/O	GPIO_Output	LORA_DIO2
58	PD11 *	I/O	GPIO_Output	LORA_DIO3
59	PD12	I/O	TIM4_CH1	REMOTE_CH4
60	PD13	I/O	TIM4_CH2	REMOTE_CH5
61	PD14	I/O	TIM4_CH3	REMOTE_CH6
65	PC8	I/O	SDIO_D0	
66	PC9	I/O	SDIO_D1	
68	PA9	I/O	USART1_TX	GPS_TX
69	PA10	I/O	USART1_RX	GPS_RX
70	PA11	I/O	GPIO_EXTI11	GPS_INT
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
78	PC10	I/O	SDIO_D2	
79	PC11	I/O	SDIO_D3	
80	PC12	I/O	SDIO_CK	
83	PD2	I/O	SDIO_CMD	
86	PD5	I/O	USART2_TX	
87	PD6	I/O	USART2_RX	
90	PB4	I/O	TIM3_CH1	REMOTE_CH1
91	PB5	I/O	TIM3_CH2	REMOTE_CH2
92	PB6	I/O	I2C1_SCL	
93	PB7	I/O	I2C1_SDA	
94	BOOT0	Boot		

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
95	PB8	I/O	TIM10_CH1	PWM_OUT8
96	PB9	I/O	TIM11_CH1	PWM_BUZZER
97	PE0 *	I/O	GPIO_Output	LORA_NSS
98	PE1 *	I/O	GPIO_Output	RTC_NC
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	F407-EFALCON4
Project Folder	C:\Users\LENOVO\git\F407-EFALCON4\F407-EFALCON4
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.26.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_I2C1_Init	I2C1
4	MX_SDIO_SD_Init	SDIO
5	MX_SPI1_Init	SPI1
6	MX_SPI2_Init	SPI2
7	MX_TIM5_Init	TIM5
8	MX_TIM9_Init	TIM9
9	MX_TIM10_Init	TIM10
10	MX_TIM11_Init	TIM11
11	MX_UART4_Init	UART4

Rank	Function Name	Peripheral Instance Name
12	MX_USART1_UART_Init	USART1
13	MX_USART2_UART_Init	USART2
14	MX_USART3_UART_Init	USART3
15	MX_ADC1_Init	ADC1
16	MX_TIM2_Init	TIM2
17	MX_TIM6_Init	TIM6
18	MX_TIM12_Init	TIM12
19	MX_FATFS_Init	FATFS
20	MX_TIM1_Init	TIM1
21	MX_TIM3_Init	TIM3
22	MX_TIM4_Init	TIM4

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407VGTx
Datasheet	DS8626_Rev8

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

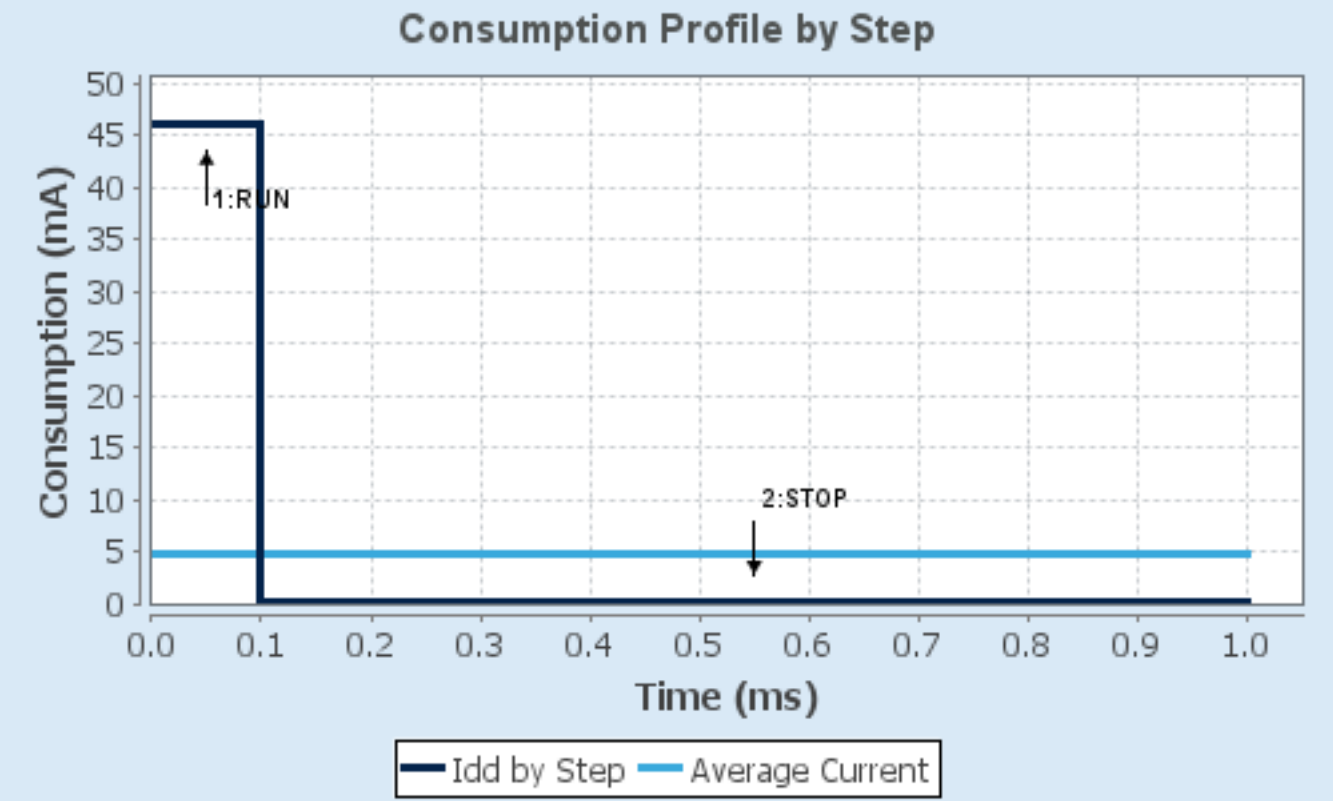
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	168 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	46 mA	280 µA
Duration	0.1 ms	0.9 ms
DMIPS	210.0	0.0
Ta Max	98.47	104.96
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	4.85 mA
Battery Life	29 days, 4 hours	Average DMIPS	210.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
50
45
40
35
30
25
20
15
10
5
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN4

mode: IN9

mode: IN10

mode: IN11

mode: IN14

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel 9 ***
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. I2C1

I2C: I2C

7.2.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.4. SDIO

Mode: SD 4 bits Wide bus

7.4.1. Parameter Settings:

SDIO parameters:

Clock transition on which the bit capture is made	Rising transition
SDIO Clock divider bypass	Disable
SDIO Clock output enable when the bus is idle	Disable the power save for the clock
SDIO hardware flow control	The hardware control flow is disabled
SDIOCLK clock divide factor	**4 ***

7.5. SPI1

Mode: Full-Duplex Master

7.5.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**32 ***
Baud Rate	**2.625 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.6. SPI2

Mode: Full-Duplex Master

7.6.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**21.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.7. SYS

Debug: Serial Wire

Timebase Source: TIM7

7.8. TIM1

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1

Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.9. TIM2

Clock Source : Internal Clock

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.10. TIM3

Channel1: Input Capture direct mode

Channel2: Input Capture direct mode

Channel3: Input Capture direct mode

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 3:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.11. TIM4

Channel1: Input Capture direct mode

Channel2: Input Capture direct mode

Channel3: Input Capture direct mode

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division

auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 3:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.12. TIM5

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable

Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.13. TIM6

mode: Activated

7.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**84 - 1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10 - 1 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.14. TIM9

Channel1: Input Capture direct mode

Channel2: Input Capture indirect mode

7.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division

auto-reload preload	Disable

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Indirect
Prescaler Division Ratio	No division

7.15. TIM10
mode: Activated
Channel1: PWM Generation CH1

7.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.16. TIM11
mode: Activated
Channel1: PWM Generation CH1

7.16.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up

Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.17. TIM12

Channel1: Input Capture direct mode

Channel2: Input Capture indirect mode

7.17.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**84 - 1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Input Capture Channel 1:

Polarity Selection	**Falling Edge ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Indirect
Prescaler Division Ratio	No division

7.18. UART4

Mode: Single Wire (Half-Duplex)

7.18.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200

Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	**Receive Only ***
Over Sampling	16 Samples

7.19. USART1

Mode: Asynchronous

7.19.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.20. USART2

Mode: Asynchronous

7.20.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.21. USART3

Mode: Asynchronous

7.21.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.22. ARM.CMSIS.5.6.0

mode: CMSISJjDSP

7.23. FATFS

mode: SD Card

7.23.1. Set Defines:

Version:

FATFS version	R0.12c

Function Parameters:

FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_EXPAND (Use f_expand function)	Disabled
USE_CHMOD (Change attributes function)	Disabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Latin 1
USE_LFN (Use Long Filename)	Disabled
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	512
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_TINY (Tiny mode)	Disabled
FS_EXFAT (Support of exFAT file system)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
FS_REENTRANT (Re-Entrancy)	Enabled
FS_TIMEOUT (Timeout ticks)	1000
USE_MUTEX	Disabled
SYNC_t (O/S sync object)	osSemaphoreId_t
FS_LOCK (Number of files opened simultaneously)	2

7.23.2. Advanced Settings:

SDIO/SDMMC:

SDIO instance	SDIO
Use dma template	Enabled
BSP code for SD	Generic

7.24. FREERTOS

Interface: CMSIS_V2

7.24.1. Config parameters:

API:

FreeRTOS API	CMSIS v2

Versions:

FreeRTOS version	10.3.1
CMSIS-RTOS version	2.00

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	**Enabled ***

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock

TICK_RATE_HZ	1000
MAX_PRIORITIES	56
MINIMAL_STACK_SIZE	**512 ***
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled
USE_COUNTING_SEMAPHORES	Enabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Enabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	1024

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

CMSIS-RTOS V2 flags:

USE_OS2_THREAD_SUSPEND_RESUME	Enabled
USE_OS2_THREAD_ENUMERATE	Enabled
USE_OS2_EVENTFLAGS_FROM_ISR	Enabled
USE_OS2_THREAD_FLAGS	Enabled
USE_OS2_TIMER	Enabled
USE_OS2_MUTEX	Enabled

7.24.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Enabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Enabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Enabled
xTaskGetCurrentTaskHandle	Enabled
eTaskGetState	Enabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Enabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

7.24.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	Disabled

Project settings (see parameter description first):

Use FW pack heap file	Enabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN10	Analog mode	No pull-up and no pull-down	n/a	ADC_ANGIN2
	PC1	ADC1_IN11	Analog mode	No pull-up and no pull-down	n/a	ADC_BATERAI3
	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	ADC_BATERAI2
	PC4	ADC1_IN14	Analog mode	No pull-up and no pull-down	n/a	ADC_ANGIN1
	PB1	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	ADC_BATERAI1
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SDIO	PC8	SDIO_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDIO_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDIO_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDIO_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDIO_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDIO_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	IMU_SCK
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	IMU_MISO
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	IMU_MOSI
SPI2	PC2	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	LORA_MISO
	PC3	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	LORA_MOSI
	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_OUT1
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_OUT2
	PE13	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_OUT3
	PE14	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_OUT4
TIM3	PB0	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	REMOTE_CH3
	PB4	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	REMOTE_CH1
	PB5	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	REMOTE_CH2
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	REMOTE_CH4
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	REMOTE_CH5
	PD14	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	REMOTE_CH6
TIM5	PA1	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_OUT5
	PA2	TIM5_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_OUT6
	PA3	TIM5_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_OUT7
TIM9	PE5	TIM9_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	US_ECHO
TIM10	PB8	TIM10_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_OUT8
TIM11	PB9	TIM11_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_BUZZER
TIM12	PB14	TIM12_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	REMOTE_PPM
UART4	PA0-WKUP	UART4_TX	Alternate Function Open Drain	Pull-up	**Very High ***	SBUS_RX
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	GPS_TX
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	GPS_RX
USART2	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PD6	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USART3	PB10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	US_TRIG
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LORA_RST
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IMU_CS
	PE7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BMP_CS
	PE10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1
	PE12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PE15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED3
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LORA_DIO1
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LORA_DIO2
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LORA_DIO3
	PA11	GPIO_EXTI11	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	GPS_INT
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LORA_NSS
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RTC_NC

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
USART2 global interrupt	true	5	0
TIM8 break interrupt and TIM12 global interrupt	true	5	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	5	0
TIM7 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt	unused		
USART1 global interrupt	unused		
USART3 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
SDIO global interrupt	unused		
TIM5 global interrupt	unused		
UART4 global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

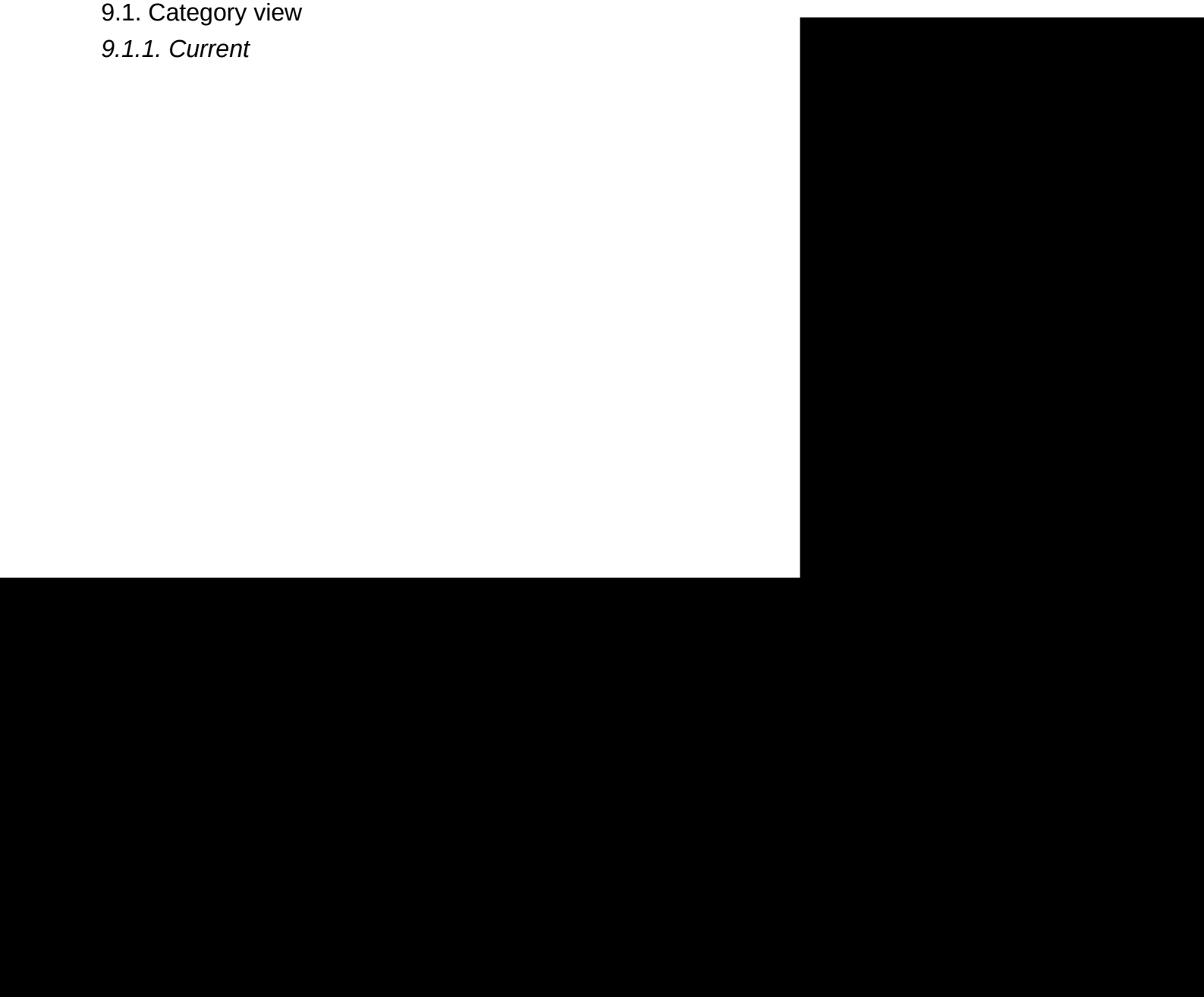
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
USART2 global interrupt	false	true	true
TIM8 break interrupt and TIM12 global interrupt	true	true	true
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	true	true
TIM7 global interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Software Pack Report

10.1. Software Pack selected

Vendor	Name	Version	Component
ARM	CMSIS	5.6.0	Class : CMSIS Group : CORE Version : 5.3.0 Class : CMSIS Group : DSP Variant : Library Version : 1.7.0

11. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00037051.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00031020.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00037591.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00249778.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00024853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00025071.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040802.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040808.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00046011.pdf
Application note	http://www.st.com/resource/en/application_note/DM00050879.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00115714.pdf
Application note	http://www.st.com/resource/en/application_note/DM00123028.pdf

Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00154959.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00213525.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00263732.pdf
Application note	http://www.st.com/resource/en/application_note/DM00281138.pdf
Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00373474.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00431633.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf