
STM32
CubeMX

1. Description

1.1. Project

Project Name	F303-ELECTROMAID
Board Name	custom
Generated with:	STM32CubeMX 6.1.1
Date	12/28/2020

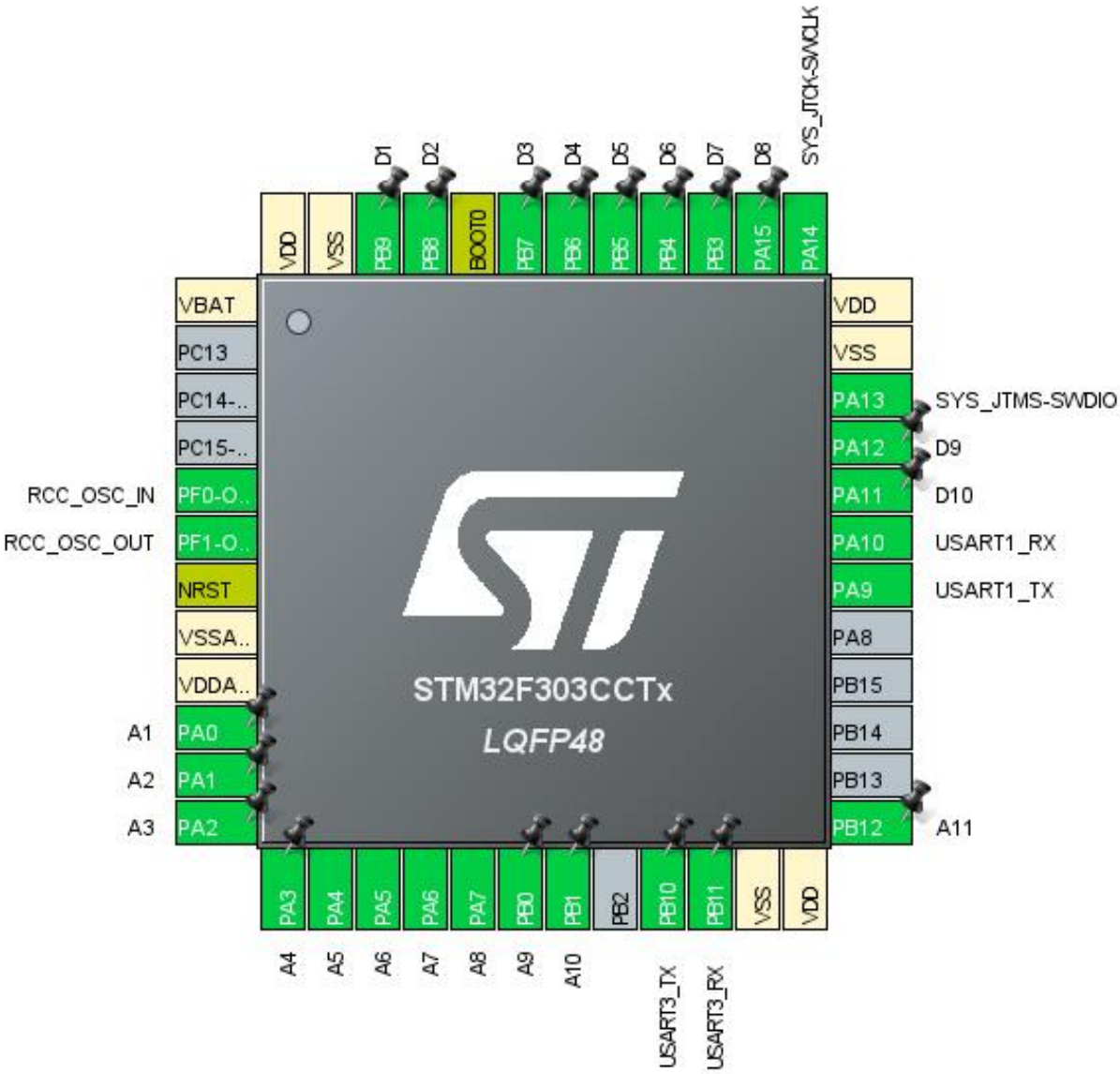
1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F303
MCU name	STM32F303CCTx
MCU Package	LQFP48
MCU Pin number	48

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



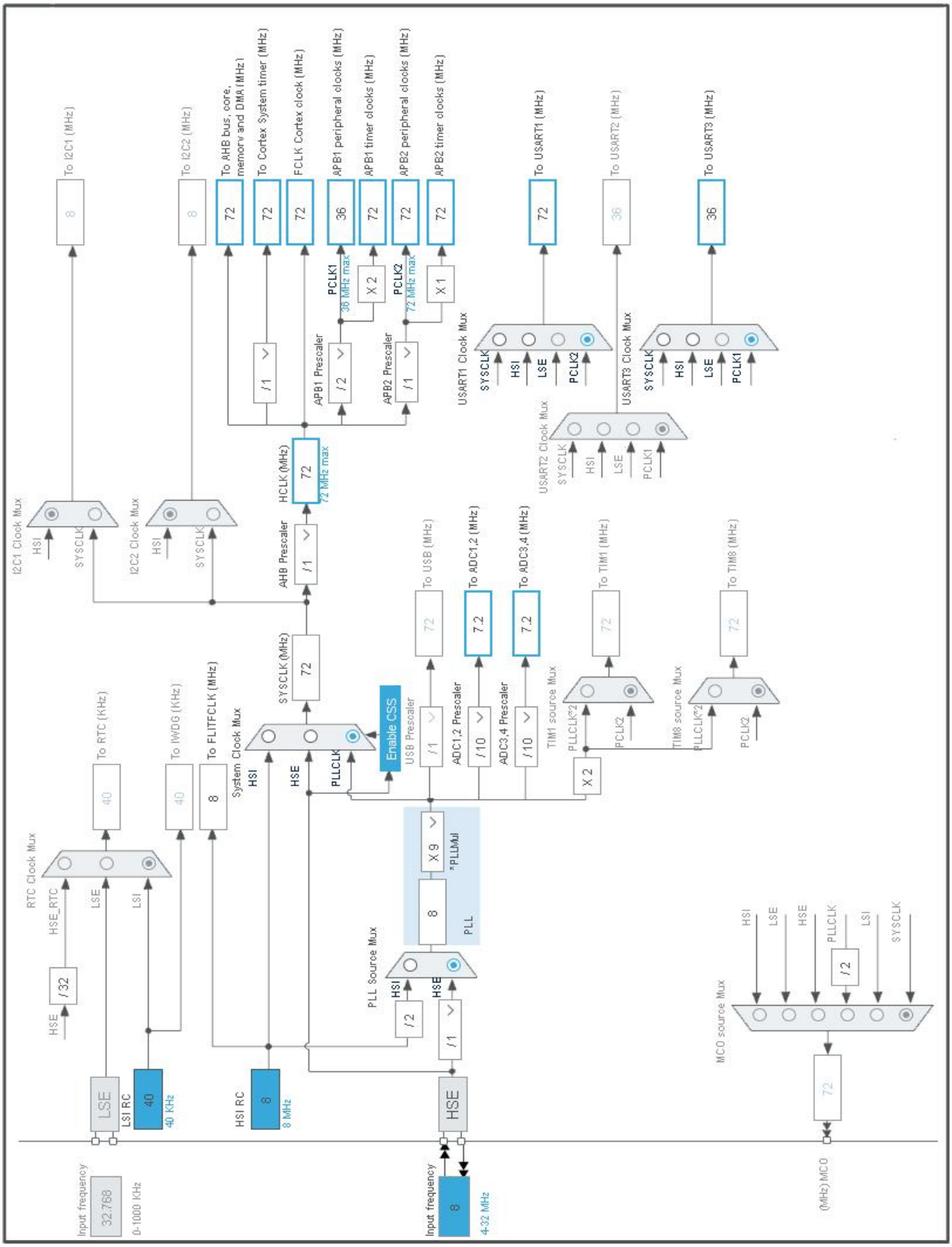
3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA/VREF-	Power		
9	VDDA/VREF+	Power		
10	PA0	I/O	ADC1_IN1	A1
11	PA1	I/O	ADC1_IN2	A2
12	PA2	I/O	ADC1_IN3	A3
13	PA3	I/O	ADC1_IN4	A4
14	PA4	I/O	ADC2_IN1	A5
15	PA5	I/O	ADC2_IN2	A6
16	PA6	I/O	ADC2_IN3	A7
17	PA7	I/O	ADC2_IN4	A8
18	PB0	I/O	ADC3_IN12	A9
19	PB1	I/O	ADC3_IN1	A10
21	PB10	I/O	USART3_TX	
22	PB11	I/O	USART3_RX	
23	VSS	Power		
24	VDD	Power		
25	PB12	I/O	ADC4_IN3	A11
30	PA9	I/O	USART1_TX	
31	PA10	I/O	USART1_RX	
32	PA11 *	I/O	GPIO_Output	D10
33	PA12 *	I/O	GPIO_Output	D9
34	PA13	I/O	SYS_JTMS-SWDIO	
35	VSS	Power		
36	VDD	Power		
37	PA14	I/O	SYS_JTCK-SWCLK	
38	PA15 *	I/O	GPIO_Output	D8
39	PB3 *	I/O	GPIO_Output	D7
40	PB4 *	I/O	GPIO_Output	D6
41	PB5 *	I/O	GPIO_Output	D5
42	PB6 *	I/O	GPIO_Output	D4
43	PB7 *	I/O	GPIO_Output	D3
44	BOOT0	Boot		

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
45	PB8 *	I/O	GPIO_Output	D2
46	PB9 *	I/O	GPIO_Output	D1
47	VSS	Power		
48	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	F303-ELECTROMAID
Project Folder	C:\Users\LENOVO\STM32CubeIDE\workspace_1.4.2\F303-ELECTROMAID
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F3 V1.11.2
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_ADC1_Init	ADC1
5	MX_USART1_UART_Init	USART1
6	MX_ADC2_Init	ADC2
7	MX_ADC3_Init	ADC3
8	MX_ADC4_Init	ADC4
9	MX_USART3_UART_Init	USART3
10	MX_TIM6_Init	TIM6
11	MX_TIM2_Init	TIM2

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F3
Line	STM32F303
MCU	STM32F303CCTx
Datasheet	DS9118_Rev13

6.2. Parameter Selection

Temperature	25
Vdd	3.6

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

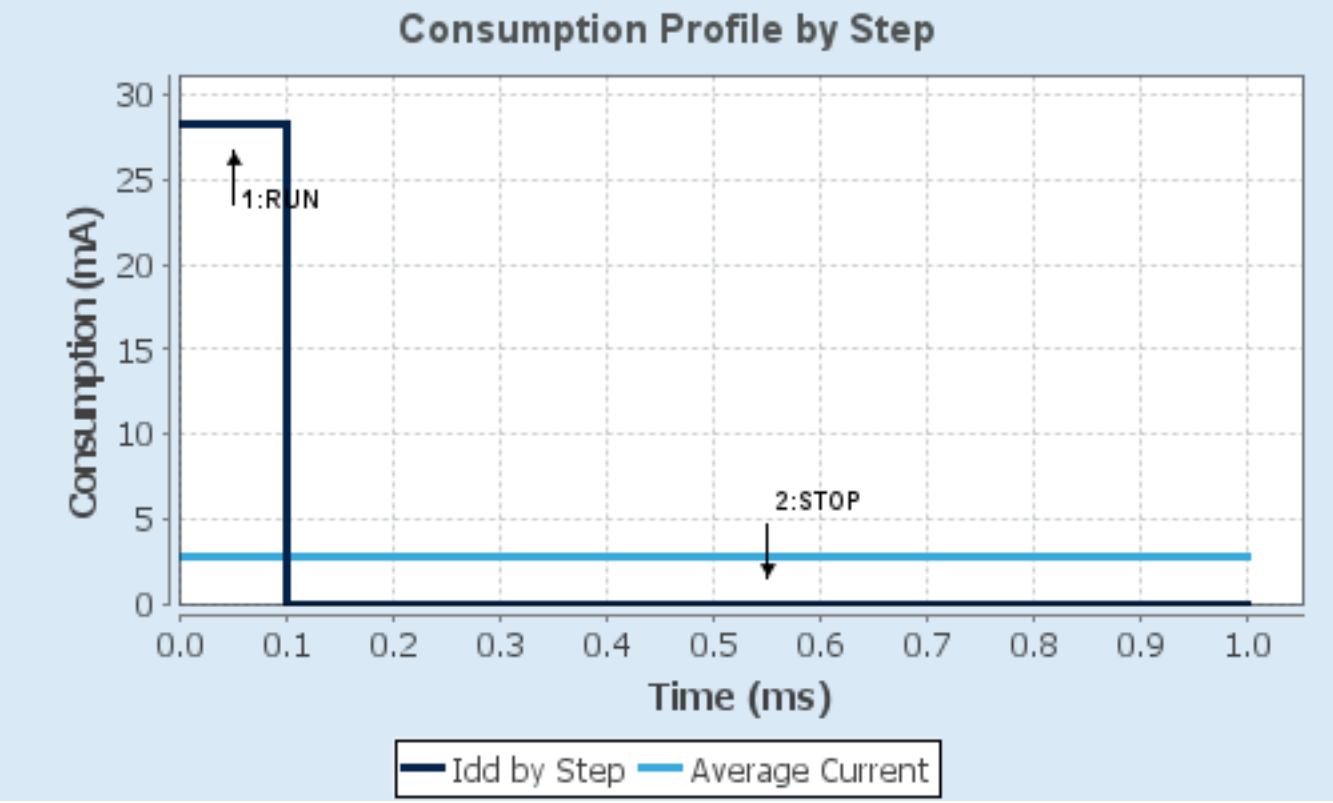
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.6	3.6
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	72 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	28.24 mA	10.85 µA
Duration	0.1 ms	0.9 ms
DMIPS	63.0	0.0
Ta Max	99.41	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	2.83 mA
Battery Life	1 month, 19 days, 12 hours	Average DMIPS	63.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
30
25
20
15
10
5
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

IN1: IN1 Single-ended

IN2: IN2 Single-ended

IN3: IN3 Single-ended

mode: IN4

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	ADC Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	**End of sequence of conversion ***
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**4 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
SequencerNbRanks	1
Rank	1
Channel	Channel 1
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**2 ***
Channel	**Channel 2 ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**3 ***

Channel	**Channel 3 ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**4 ***
Channel	**Channel 4 ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. ADC2

IN1: IN1 Single-ended

IN2: IN2 Single-ended

IN3: IN3 Single-ended

mode: IN4

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	ADC Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	**End of sequence of conversion ***

Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**4 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
SequencerNbRanks	1
Rank	1
Channel	Channel 1
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**2 ***
Channel	**Channel 2 ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**3 ***
Channel	**Channel 3 ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**4 ***
Channel	**Channel 4 ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.3. ADC3

IN1: IN1 Single-ended

mode: IN12

7.3.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	ADC Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**2 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
SequencerNbRanks	1
Rank	1
Channel	**Channel 12 ***
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**2 ***
Channel	Channel 1
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.4. ADC4

IN3: IN3 Single-ended

7.4.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	ADC Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	**End of sequence of conversion ***
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
SequencerNbRanks	1
Rank	1
Channel	Channel 3
Sampling Time	**601.5 Cycles ***
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.5. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.5.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

7.6. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.7. TIM2

Clock Source : Internal Clock

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**7200 - 1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

7.8. TIM6

mode: Activated

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**7200 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10000 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.9. USART1

Mode: Asynchronous

7.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	**115200 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.10. USART3

Mode: Asynchronous

7.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	**921600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_IN1	Analog mode	No pull up pull down	n/a	A1
	PA1	ADC1_IN2	Analog mode	No pull up pull down	n/a	A2
	PA2	ADC1_IN3	Analog mode	No pull up pull down	n/a	A3
	PA3	ADC1_IN4	Analog mode	No pull up pull down	n/a	A4
ADC2	PA4	ADC2_IN1	Analog mode	No pull up pull down	n/a	A5
	PA5	ADC2_IN2	Analog mode	No pull up pull down	n/a	A6
	PA6	ADC2_IN3	Analog mode	No pull up pull down	n/a	A7
	PA7	ADC2_IN4	Analog mode	No pull up pull down	n/a	A8
ADC3	PB0	ADC3_IN12	Analog mode	No pull up pull down	n/a	A9
	PB1	ADC3_IN1	Analog mode	No pull up pull down	n/a	A10
ADC4	PB12	ADC4_IN3	Analog mode	No pull up pull down	n/a	A11
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull up pull down	**High ***	
	PA10	USART1_RX	Alternate Function Push Pull	No pull up pull down	**High ***	
USART3	PB10	USART3_TX	Alternate Function Push Pull	No pull up pull down	**High ***	
	PB11	USART3_RX	Alternate Function Push Pull	No pull up pull down	**High ***	
GPIO	PA11	GPIO_Output	Output Push Pull	**Pull down ***	Low	D10
	PA12	GPIO_Output	Output Push Pull	**Pull down ***	Low	D9
	PA15	GPIO_Output	Output Push Pull	**Pull down ***	Low	D8
	PB3	GPIO_Output	Output Push Pull	**Pull down ***	Low	D7
	PB4	GPIO_Output	Output Push Pull	**Pull down ***	Low	D6
	PB5	GPIO_Output	Output Push Pull	**Pull down ***	Low	D5
	PB6	GPIO_Output	Output Push Pull	**Pull down ***	Low	D4
	PB7	GPIO_Output	Output Push Pull	**Pull down ***	Low	D3
	PB8	GPIO_Output	Output Push Pull	**Pull down ***	Low	D2
	PB9	GPIO_Output	Output Push Pull	**Pull down ***	Low	D1

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low
ADC2	DMA2_Channel1	Peripheral To Memory	Low
ADC3	DMA2_Channel5	Peripheral To Memory	Low
ADC4	DMA2_Channel2	Peripheral To Memory	Low
USART3_RX	DMA1_Channel3	Peripheral To Memory	Low

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC2: DMA2_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC3: DMA2_Channel5 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC4: DMA2_Channel2 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***

Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

USART3_RX: DMA1_Channel3 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
DMA1 channel3 global interrupt	true	0	0
TIM2 global interrupt	true	0	0
USART3 global interrupt / USART3 wake-up interrupt through EXTI line 28	true	0	0
Timer 6 interrupt and DAC underrun interrupts	true	0	0
DMA2 channel1 global interrupt	true	0	0
DMA2 channel2 global interrupt	true	0	0
DMA2 channel5 global interrupt	true	0	0
PVD interrupt through EXTI line16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 interrupts	unused		
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	unused		
ADC3 global interrupt	unused		
ADC4 interrupt	unused		
Floating point unit interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false

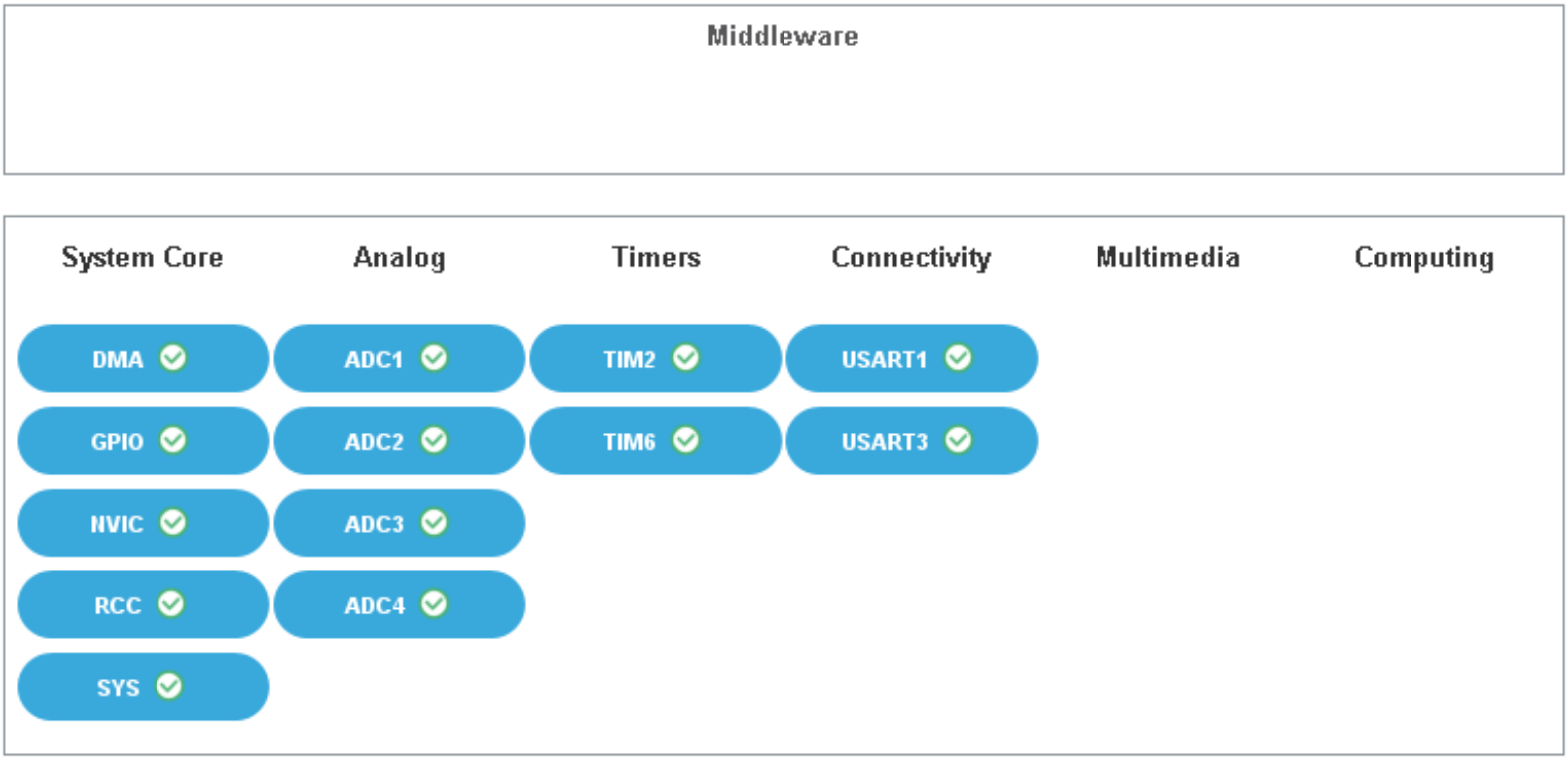
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 channel1 global interrupt	false	true	true
DMA1 channel3 global interrupt	false	true	true
TIM2 global interrupt	false	true	true
USART3 global interrupt / USART3 wake-up interrupt through EXTI line 28	true	true	true
Timer 6 interrupt and DAC underrun interrupts	false	true	true
DMA2 channel1 global interrupt	false	true	true
DMA2 channel2 global interrupt	false	true	true
DMA2 channel5 global interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00058181.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00043574.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00063985.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00025071.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00074240.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00083249.pdf
Application note	http://www.st.com/resource/en/application_note/DM00085385.pdf
Application note	http://www.st.com/resource/en/application_note/DM00087593.pdf
Application note	http://www.st.com/resource/en/application_note/DM00121474.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf

Application note	http://www.st.com/resource/en/application_note/DM00157785.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00260340.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00269146.pdf
Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00355687.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00607955.pdf
Application note	http://www.st.com/resource/en/application_note/DM00442720.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf