L_4

Laboratory IV

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1 Details of Lab 4

Q. 1 **C**. Change the gate-delay of the AND gate to 0, 3, 5. Observe the output changes with respect to the changes of input x.

They mimic the input x with an offset along the time axis associated with the time of the gate delay.

Q. 2 Draw the circuit to implement the Boolean function as follows

$$f(a,b,c,d) = (a'+b)'c + d(b'+ac)$$

according to the expression directly. Connect b, c and d to binary switches and make them to be 0, 1 and 0, respectively. Connect a to a clock.

Q. 2.1 According to your simulation, how much time does it take for the change of a to be reflected in the output f?

Five nanoseconds.

Q. 2.2 Change the gate delays of all the gates along the path from a to f to 0, 2 and 4. Verify that the total delays from a to f you observed are correct.

For a 0ns delay, a and f corresponded exactly. For a 2ns delay, a and f differed by a 10ns delay. For a 5ns delay, a and f differed by a 45ns delay.

Q. 3 Here follows the Karnaugh map of f.

$$f(a,b,c,d) = (a'+b)'c + d(b'+ac)$$

		CD			
		00	01	11	10
AB	00	0	1	1	0
	01	0	0	0	0
	11	0	0	1	0
	10	0	1	1	1

Which shows that f can be represented as the sum of minterms as follows:

$$f(a,b,c,d) = b'd + acd + ab'c$$

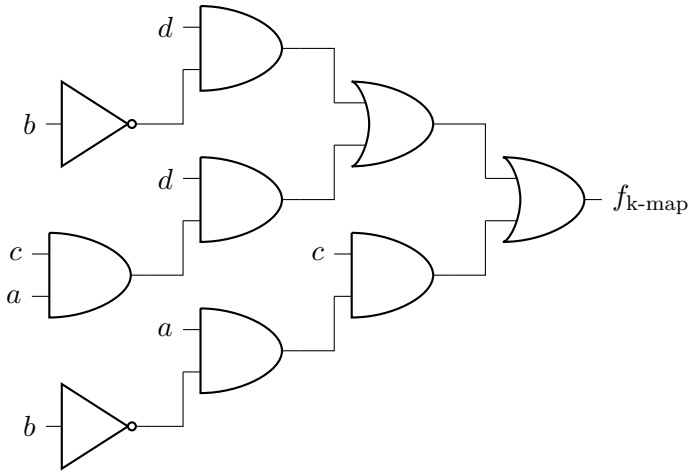

Figure 1: Circuit diagram for f after reduction to sum of midterms.

Q. 4 Compare the circuits.

Testing all 16 possible input combinations resulted in identical outputs if the gate delay is set to 0ns.