L_4

Laboratory IV

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1 Details of Lab 4

Q. 1 **C**. Change the gate-delay of the AND gate to 0, 3, 5. Observe the output changes with respect to the changes of input x.

They mimic the input x with an offset along the time axis associated with the time of the gate delay.

Q. 2 Here follows the Karnaugh map of f.

$$f(a,b,c,d) = (a' + b)'c + d(b' + ac)$$

		CD			
		00	01	11	10
AB	00	0	1	1	0
	01	0	0	0	0
	11	0	0	1	0
	10	0	1	1	1

Which shows that f can be represented as the sum of minterms as follows:

$$f(a,b,c,d) = b'd + acd + ab'c$$

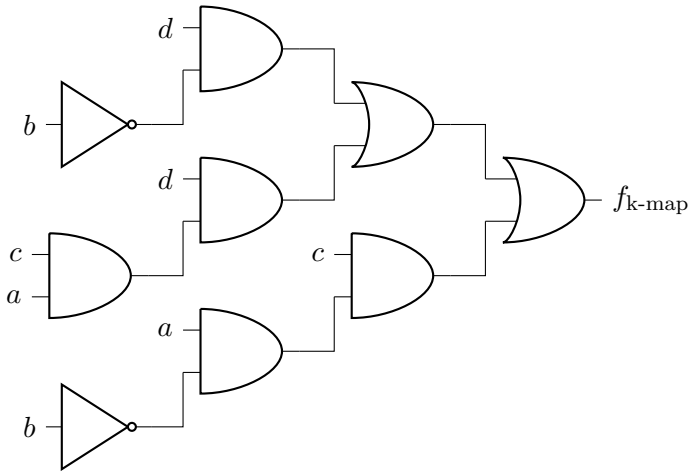

Figure 1: Circuit diagram for f after reduction to sum of midterms.