A_2

Assignment 2

CS 3482; Professor Tang

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1. To test the circuits, we will assure that the Q only changes when G is 1 and D is changed. Q should reflect the value of D while G is on, and then lock when Q is 0. G should serve as the *latch* in the D latch circuit.

   The D flip flop is edge triggered rather than level triggered as the D latch is. This means that the D flip flop should only change on rising edges of G. Q only reflects D if it is at the rising edge of G, otherwise it is locked.

2.

3. Each row of output D bits is the input Q bits of the last state plus 1. The sum of minterms obtained from the Karnaugh maps of each of the four Ds are as follows:

$$D_0 = Q_0'$$

$$D_1 = Q_0'Q_1 + Q_1Q_1'$$

$$D_2 = Q_3'Q_2'Q_1Q_0 + Q_3'Q_2Q_1' + Q_3'Q_2Q_1Q_0' + Q_3Q_2Q_1Q_0 + Q_3Q_2'Q_1' + Q_3Q_2'Q_1Q_0'$$

$$D_3 = Q_3Q_2 + Q_3Q_2'Q_1' + Q_3Q_2'Q_1Q_0' + Q_3'Q_2Q_1Q_0$$