A Multiphase Switched Capacitor Power Amplifier

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***Abstract*— This paper presents an all-digital multiphase switched capacitor power amplifier (MP-SCPA) implemented in a 130-nm CMOS. Quadrature architectures suffer reduced output power and efficiency owing to the combination of out-of-phase signals. The MP architecture reduces the phase difference between the basis vectors that are combined, and hence the output power and efficiency are greatly improved. Sixteen clocks with identical adjacent phase separations are produced by a phase generator with each phase's relative amplitude weighted on the top plate of a capacitor array and combined on a common bottom plate, resulting in linear amplification. The MP-SCPA delivers a peak output power P_{out} of 26 dBm with a peak system efficiency (SE) of 24.9%. When amplifying a long-term evolution signal at 1.85 GHz, the average P_{out} and the SE are 20.9 dBm and 15.2%, respectively, with an Adjacent Channel Leakage Ratio (ACLR) < −30 dBc and error vector magnitude of 3.5% rms using a 2-D digital predistortion.**

***Index Terms*— Class-D power amplifier (PA), digital PA, multiphase (MP) transmitter, RF digital-to-analog converter (RF-DAC), switched capacitor PA (SCPA).**

I. Introduction

HIGH-SPEED wireless communication systems [e.g., long-term evolution (LTE) and Wi-Fi] operate with high bandwidth and large peak-to-average power ratios (PAPRs). This is largely due to the use of orthogonal frequency-division multiplexing (OFDM) modulation that is used to maximize spectral efficiency. The RF power amplifier (PA) in the transmitter is the dominant energy consumer in the radio, largely due to the PAPR of the input signal. To reduce the energy consumption in the system, PAs that simultaneously achieve high efficiency and high linearity are necessary. Furthermore, to lower the cost for high volume production, it is desirable to achieve complete system-on-chip (SoC) integration including the RF PA.

Linear PAs, where the device operates as a linear transconductor for some part of the input cycle (e.g., Class-A, -B, and -AB), are inefficient when amplifying signals with large PAPR (e.g., LTE, Wi-Fi, and OFDM). Switching PAs (e.g., Class-D, -E, and -F) are very promising due to their high efficiency compared with their linear amplifier counterparts; however, their responses are insensitive to amplitude modulation. An added advantage of switching PAs is that deep-submicrometer CMOS technology is optimized for performance as a switch for digital logic circuitry [1]. Moore's law scaling of CMOS optimizes transistors to operate as high-speed low-loss switches rather than high-gain transconductors [2]. Hence, it is advantageous to use transistors as switches in switching PAs and use high-speed digital logic circuitry to implement linearization systems and circuitry.

Linearization techniques for switching amplifiers have been intensively investigated to enable the operation of switching amplifiers for nonconstant envelope (non-CE) modulation. Techniques such as analog/digital polar PAs [3]–[9], digital-Doherty [10], outphasing [11], and pulsewidth modulation [12], [13] have been proposed. All of the techniques above require a conversion from the Cartesian to the polar coordinate system, via either analog or digital signal processing. Polar architectures result in bandwidth expansion of the amplitude and phase modulated signals due to the nonlinear conversion from the Cartesian to the polar domain. Additionally, because the amplitude and phase modulation signals propagate at different frequencies, they experience different group delays and are hence subject to delay mismatches [14]. Moreover, they require wideband amplitude and phase modulators, the latter of which are difficult to implement in closed loops [e.g., phase-locked loops (PLLs)], due to the excessive bandwidth, which can be ten times the RF bandwidth [15]. Open-loop phase modulators can be implemented with wide bandwidth, but they introduce phase quantization, digital-to-phase nonlinearity, and spectral images and require careful calibration [8].

Quadrature architectures avoid the bandwidth expansion and delay mismatch, as well as the elimination of both the supply modulator and phase modulator [16]–[18]. The expanded bandwidth of the quadrature generation does not need to be modulated in a closed loop and does not propagate at a different frequency than the envelope. Hence, nonlinearity associated with signal bandwidth and delay mismatch is mitigated, while still accommodating a good interface to the digital backend. However, the power loss due to the out-of-phase summation of the I and Q signals significantly limits their peak/average power and efficiency. One solution is to reduce the separation between the summed adjacent phases, which reduces the loss due to the vector summation. This can be accomplished by adding basis phase vectors in the complex plane [19], [20].

In this paper, we present a multiphase switched capacitor PA (MP-SCPA) for non-CE amplification [21]. A block diagram of an MP-SCPA is shown in Fig. 1(a). In the proposed architecture, a single clock is used to generate M different phases. This can be accomplished using an MP ring oscillator, polyphase filters, or delay-locked loops (DLLs). Each phase can be weighted and summed in the charge domain in an

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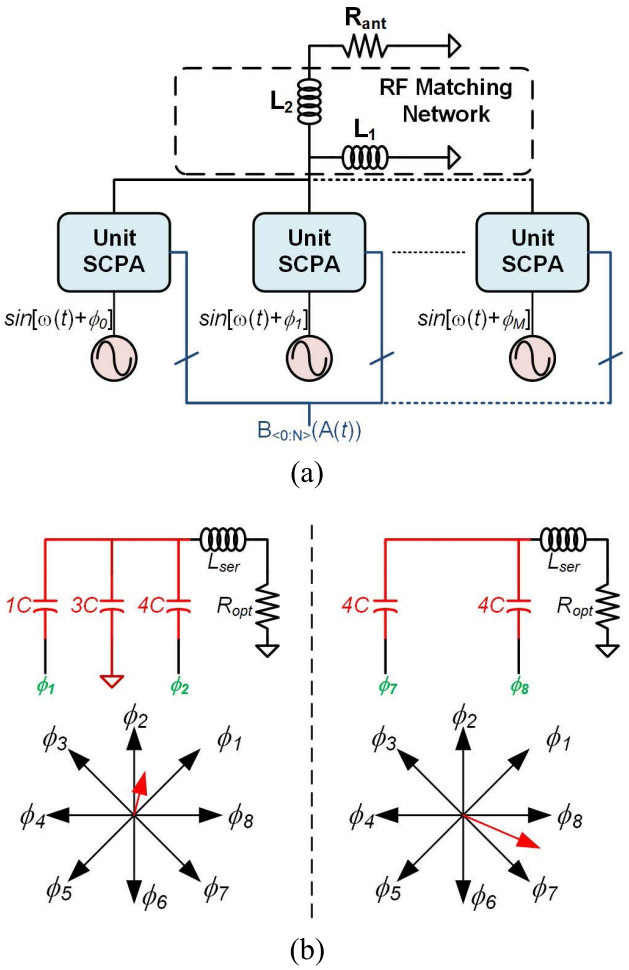

Fig. 1. (a) Block diagram of an MP-SCPA-based transmitter. (b) Schematics of capacitively combined MP-SCPAs outputting different amplitudes and phases.

SCPA to output the desired amplitude and phase [Fig. 1(b)]. MP architectures increase the output power compared with quadrature architectures by reducing the angular separation of the basis phases. Because the phase generation and logic are low power, it is a cost effective means to improve the output power and efficiency of digital transmitters. Like in a quadrature architecture, the expanded bandwidth of the phase generation does not need to be modulated in a closed loop and hence does not suffer the problems associated with polar architectures.

This paper is organized as follows. In Section II, theoretical operation of the MP-SCPA is discussed. The design details of the presented MP-SCPA are provided in Section III, followed by the measurement results in Section IV. Finally, conclusions are presented in Section V.

II. Theory of Operation

A. Operation of Q-SCPA

The quadrature SCPA (Q-SCPA) is an example of an MP architecture, where the number of phase vectors M is equal to four [Fig. 1(a)] [17]. The capacitor array is subdivided into four subarrays that are clocked by $\pm I$ and $\pm Q$, respectively. Selection logic (e.g., bin) controls whether the cell is either switched between V_{DD} and V_{GND} or held at V_{GND}. This operation allows precise control of the output amplitude and phase, using a vector sum in the charge domain on the top plate of the capacitors in the SCPA array. The input upconverting clock pulses for the I and Q capacitor subarrays are 90° out of phase. The output signal $s(t)$ is the direct summation of $I(t)$ and $Q(t)$ waveforms

$$s(t) = I(t)p(t) + Q(t)p\left(t + \frac{T}{4}\right) \tag{1}$$

where T is the carrier period, and $p(t)$ and $p(t + T/4)$ represent the input 50% duty cycle square waveforms. The $I(t)$ and $Q(t)$ signals are given by

$$I(t) = A(t) \cdot \cos[\phi(t)] \tag{2}$$

$$Q(t) = A(t) \cdot \sin[\phi(t)] \tag{3}$$

where $A(t)$ and $\phi(t)$ are the amplitude and phase of the modulated signal, respectively.

When the magnitudes of I and Q are equal, the maximum amplitude of the summation of the two vectors is given by

$$V_{IQ} = V_\theta \cos(P/2) \tag{4}$$

where V_θ is the amplitude of the I/Q vector and P is the phase angle separation between the two vectors. For a quadrature system, $P = \pi/2$. Compared with a polar system, the maximum amplitude of the system is V_θ. Hence, a power ratio comparing a quadrature system with a polar system P_{rel} can be calculated as follows:

$$P_{\text{rel}} = 10\log_{10}\left[\frac{V_{I,Q}^2 \cdot \cos^2(\pi/4)}{V_{I,Q}^2}\right] = -3.0 \text{ dB}. \tag{5}$$

Thus, the output power of a quadrature system is reduced by 3 dB when compared with the vector summation of two signals that are in phase (e.g., polar). Hence, there is a phase-dependent power drop that is caused by the 90° phase difference of the I/Q clocking signals.

For an OFDM modulated signal, the phase is uniformly distributed between 0 and 2π, and hence the average power drop can be found due to all combinations of IQ summation. The output phase is given by ϕ and the output amplitude is given by A_0. In an SCPA, the output amplitude is proportional to the number of the capacitors that are switched. The ratio between the amplitudes of digital polar SCPA and Q-SCPA, V_{rel}, for any output phase ϕ is thus expressed as follows:

$$V_{\text{rel}} = \frac{A(\phi)}{I(\phi) + Q(\phi)} = \frac{A_0}{|A_0\cos\phi| + |A_0\sin\phi|} = \frac{1}{|\cos\phi| + |\sin\phi|}. \tag{6}$$

It is noted that this result derives from the fact that both phases in the quadrature system can be used to switch the same capacitor bank. The average ratio from 0 to 2π is calculated as follows:

$$\overline{V_{\text{rel}}} = \frac{1}{2\pi}\int_0^{2\pi} \frac{1}{|\cos\phi| + |\sin\phi|} d\phi = \frac{\sqrt{2}}{\pi}\ln\left(\frac{\sqrt{2}+1}{\sqrt{2}-1}\right) \approx 0.794. \tag{7}$$

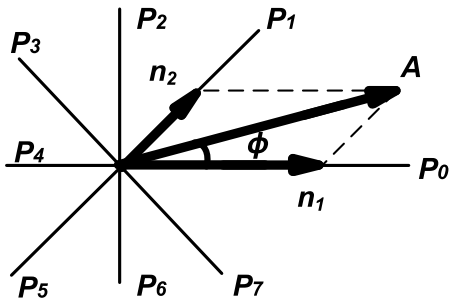

Fig. 2. Polar to MP conversion diagram.

Similarly, the average output power ratio is calculated

$$\overline{P_{\text{rel}}} = \frac{1}{2\pi}\int_0^{2\pi} \frac{1}{(|\cos\phi| + |\sin\phi|)^2} d\phi = \frac{2}{\pi} \approx -1.96 \text{ dB}. \tag{8}$$

Hence, for an OFDM modulated signal, the output power of a Q-SCPA is 2 dB lower on average than that of a polar SCPA. This loss of output power can be alleviated by increasing the number of basis phases M to be greater than 4. The MP-SCPA is discussed next.

B. Operation of the MP-SCPA

An example of MP summation is shown in Fig. 1(b) using eight clock phases. Additional clock phases reduce the separation between adjacent phase vectors, resulting in the increased constructive summation between any adjacent phase vectors and hence reducing the power loss.

The circuitry to generate precision MP signals and the digital logic to implement the MP signal processing were difficult to implement when polar amplification was introduced by Kahn [3]. Such circuitry is readily available in modern fine line CMOS processes. Deep-submicrometer CMOS technology is fundamentally a digital technology, as it is optimized to yield fast low-loss switches. The MP architecture leverages the strengths using low-cost and low-power digital circuitry to reduce the power loss and hence increase efficiency in high-power switching PAs.

As shown in Fig. 2, an arbitrary vector with amplitude A and phase θ can be converted into the MP domain using the following:

$$n_1 = A\cos(\pi/M) \cdot \frac{\sin(2\pi/M)}{\sin[2\pi/(M-\phi)]} \tag{9}$$

$$n_2 = A\cos(\pi/M) \cdot \frac{\sin(2\pi/M)}{\sin\phi} \tag{10}$$

$$\phi = \theta - \frac{2\pi}{M} \cdot m. \tag{11}$$

It is noted that there are multiple ways to perform this conversion due to the lack of orthogonality in the basis vectors and hence more than one solution exist. The scalars n_1 and n_2 represent the amplitudes of the two adjacent phase vectors to the desired output θ, and m is an integer representing the index of the selected phase vector that is determined using the following:

$$\frac{m}{M} \cdot 2\pi \le \theta < \frac{m+1}{M} \cdot 2\pi. \tag{12}$$

Rearranging (12) yields the following:

$$\frac{\theta}{2\pi} \cdot M - 1 \le m < \frac{\theta}{2\pi} \cdot M. \tag{13}$$

To quantify the efficiency improvement of the proposed MP architecture, the relative power of a MP system compared with that of a polar system $P_{\text{rel,MP}}$ can be calculated for any output phase ϕ

$$P_{\text{rel,MP}} = \frac{A^2(\phi)}{(n_1(\phi) + n_2(\phi))^2} = \frac{\sin^2(\pi - 2\pi/M)}{(|\sin(2\pi/M - \phi| + |\sin\phi|)^2}. \tag{14}$$

The maximum power loss occurs when $\phi = \pi/M$, and is given as follows:

$$(P_{\text{rel,MP}}) = \frac{A^2(\pi/M)}{(n_1(\pi/M) + n_2(\pi/M))^2} = \cos^2(\pi/M). \tag{15}$$

Hence, the maximum power loss for an eight-phase MP architecture is only -0.69 dB, whereas a 16-phase system yields a power loss of -0.17 dB.

The output voltage ratio comparing an M-phase architecture and a polar architecture for any output phase, $V_{\text{rel,MP}}$, can be calculated as follows:

$$\begin{aligned} V_{\text{rel,MP}} &= \frac{A(\phi)}{A_M(\phi) + A_{M+1}(\phi)} \\ &= \frac{A_0 \sin[(M-2)\pi/M]}{|A_0 \sin(2\pi/M - \phi)| + |A_0 \sin\phi|} \\ &= \frac{\sin[(M-2)\pi/M]}{|\sin(2\pi/M - \phi)| + |\sin\phi|}. \end{aligned} \tag{16}$$

The average for a uniformly distributed phase signal over the range from 0 to 2π is given by

$$\begin{aligned} \overline{V_{\text{rel,MP}}} &= \frac{1}{2\pi}\int_0^{2\pi} \frac{\sin[(M-2)\pi/M]}{|\sin(2\pi/M - \phi)| + |\sin\phi|} d\phi \\ &= \frac{M \cdot \sin[(M-2)\pi/M]}{2\pi C} \\ &\quad \cdot \ln\left(\frac{\sec(\pi/M) + \tan(\pi/M)}{\sec(\pi/M) - \tan(\pi/M)}\right) \end{aligned} \tag{17}$$

where $C = (2 - 2\cos(2\pi/M))^{1/2}$. Similarly, the average output power ratio is calculated as follows:

$$\begin{aligned} \overline{P_{\text{rel,MP}}} &= \frac{1}{2\pi}\int_0^{2\pi} \frac{\sin^2[(M-2)\pi/M]}{(|\sin(2\pi/M - \phi)| + |\sin\phi|)^2} d\phi \\ &= \frac{M \cdot \sin^2[(M-2)\pi/M]}{2\pi[1 - \cos(2\pi/M)]} \cdot \tan(\pi/M). \end{aligned} \tag{18}$$

The average power drop for an OFDM modulated signal is reduced to -0.46 dB for an 8-phase system and -0.11 dB for a 16-phase system, respectively.

The SCPA has good linearity and constant impedance with respect to the load, and hence it is a good candidate to

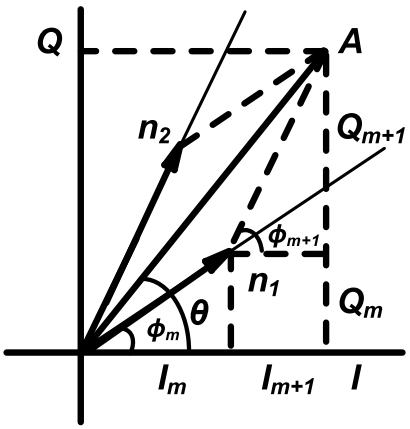

Fig. 3. Cartesian to MP conversion diagram.

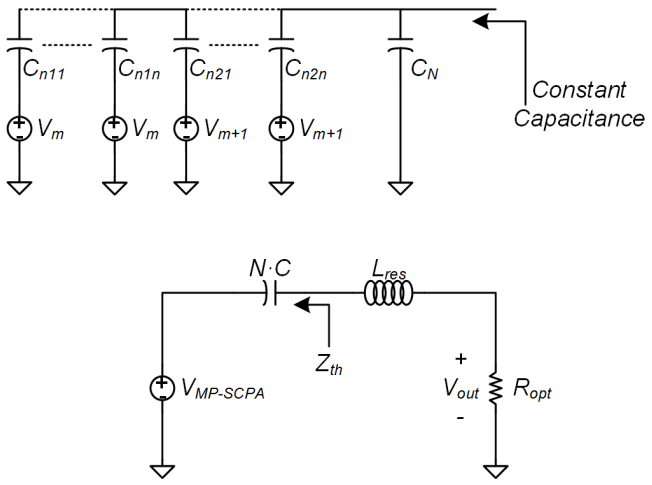

Fig. 4. MP capacitor array (top) and its Thévenin equivalent circuit in an MP-SCPA (bottom).

implement the MP architecture. In an SCPA, an array of capacitor cells has a shared bottom plate, whereas the top plates are separate and driven by a phase-modulated pulsewave, switching between $V_{\rm DD}$ and $V_{\rm GND}$ or held at $V_{\rm GND}$ to control the output amplitude. To accommodate the MP operation, an RF clock signal is subdivided into M equally spaced output phases (ϕ_1–ϕ_M). Such signals can be generated using ring oscillators, polyphase filters, PLLs, or DLLs [22], [23]. A digital phase selector selects the chosen phase to drive each capacitor. An example of an MP-SCPA is shown in Fig. 1(a). In the example, each unit SCPA is clocked by one of M phases and a decoder selects the amplitude weight of each phase to achieve the desired output vector. It is noted that the actual implementation is slightly different, as will be described in Section III.

1) MP-SCPA Output Power: In order to facilitate transitioning from Cartesian to MP architectures and vice versa, a set of transformations is derived that allow easy mapping from one coordinate system to the other. As shown in Fig. 3, the I and Q components of an MP vector can be expressed as follows:

$$I = I_m + I_{m+1} = n_1 \cos\left(\frac{2\pi m}{M}\right) + n_2 \cos\left(\frac{2\pi (m+1)}{M}\right) \tag{19}$$

and

$$Q = Q_m + Q_{m+1} = n_1 \sin\left(\frac{2\pi m}{M}\right) + n_2 \sin\left(\frac{2\pi (m+1)}{M}\right) \tag{20}$$

where n_1 and n_2 are the amplitudes of the two selected phase vectors that are adjacent to the desired output phase and m represents the index of the selected phase vector that is determined by (13).

From (19) and (20), the Cartesian to MP conversion can be obtained as follows:

$$n_1 = \frac{I \sin\left(\frac{2\pi (m+1)}{M}\right) - Q \cos\left(\frac{2\pi (m+1)}{M}\right)}{\sin\left(\frac{2\pi}{M}\right)} \tag{21}$$

and

$$n_2 = \frac{I \sin\left(\frac{2\pi m}{M}\right) - Q \cos\left(\frac{2\pi m}{M}\right)}{\sin\left(\frac{2\pi}{M}\right)}. \tag{22}$$

The output voltage of the MP PA is proportional to the vector summation of the n_1 and n_2 components across an array of N ($N = n_1 + n_2$) total capacitors

$$\begin{aligned} V_{\text{MP-SCPA}} &= \frac{\vec{n_1} + \vec{n_2}}{N} \cdot V_{\rm DD} \\ &= \frac{\sqrt{n_1^2 + n_2^2 + 2n_1 n_2 \cos\left(\frac{2\pi}{M}\right)}}{N} \cdot V_{\rm DD}. \end{aligned} \tag{23}$$

This can be seen as a Thévenin equivalent voltage driving a fixed capacitor, and hence a Thévenin equivalent circuit replaces the array of capacitors and is connected in series with a resonant inductor and an optimum resistance for power delivery, as shown in Fig. 4. Assuming that a square waveform is input with an amplitude of $V_{\rm DD}$, but only the fundamental tone is output due to the bandpass operation of the series resonant circuit, the output voltage delivered to $R_{\rm opt}$ is found by

$$V_{\rm out} = \frac{2V_{\rm DD}}{\pi} \frac{\sqrt{n_1^2 + n_2^2 + 2n_1 n_2 \cos\left(\frac{2\pi}{M}\right)}}{N} \tag{24}$$

where the $2/\pi$ factor is the Fourier coefficient of the fundamental tone of the input square pulse wave.

The output power can be extracted from the rms value of the output waveform as follows:

$$P_{\rm out} = \frac{V_{\rm out,rms}^2}{R_{\rm opt}} = \frac{2}{\pi^2}\left(\frac{n_1^2 + n_2^2 + 2n_1 n_2 \cos\left(\frac{2\pi}{M}\right)}{N^2}\right)\frac{V_{\rm DD}^2}{R_{\rm opt}}. \tag{25}$$

Here, it can be seen that as M tends toward infinity (e.g., a polar modulator) and the MP-SCPA behaves like the original SCPA, as expected. The efficiency of the SCPA can be calculated by finding the input power required to switch the capacitor array.

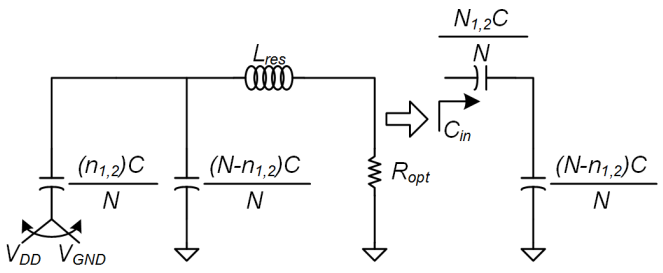

Fig. 5. Equivalent circuit for calculation of the input power of the MP-SCPA. The inductor approximates a fixed high impedance during fast switching transitions of the capacitor.

2) MP-SCPA Efficiency: The input power of the SCPA is due to the energy required to charge and discharge the capacitors in the array [17], [24]. Assuming that the inductor (Fig. 5) acts as an RF current source, it can be treated as an open circuit; hence, the equivalent capacitance C_{in} is the series combination of the capacitors being switched with those not being switched. Note that this must be done for the capacitors being clocked on phase m (e.g., n_1) and those being clocked on phase $m+1$ (e.g., n_2)

$$C_{\text{in}} = \left[\frac{(n_1)(N-n_1)}{N^2} + \frac{(n_2)(N-n_2)}{N^2} + \frac{2n_1n_2}{N^2}\right]C. \quad (26)$$

The input power P_{SC} is thus the power required to switch C_{in}

$$P_{\text{SC}} = C_{\text{in}} V_{\text{DD}}^2 f_0 \quad (27)$$

where f_0 is the switching frequency used to drive the switches in the capacitor array and is equivalent to the RF output frequency. The loaded quality factor of the series resonant network comprising the capacitor array, the series inductor, and the load resistor is given by

$$Q_{\text{NW}} = \frac{2\pi f_0 L_{\text{ser}}}{R_{\text{opt}}} = \frac{1}{2\pi f_0 C R_{\text{opt}}}. \quad (28)$$

From this, the drain efficiency η of the SCPA can be defined as

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{SC}}}. \quad (29)$$

Substitution of (25)–(28) into (29) yields the following:

$$\eta = \frac{4\left(n_1^2 + n_2^2 + 2n_1n_2\cos\left(\frac{2\pi}{M}\right)\right)}{4\left(n_1^2 + n_2^2 + 2n_1n_2\cos\left(\frac{2\pi}{M}\right)\right) + \frac{\pi[n_1(N-n_1)+n_2(N-n_2)]}{Q_{NW}}}. \quad (30)$$

For on-chip matching networks, reasonable values of Q_{nw} must be chosen due to losses in the passive components (e.g., spiral inductors). If it is assumed that $n_1 = n_2$ and $Q_{\text{NW}} = 3$, η is plotted versus the number of switching capacitors and phase vectors, M, as shown in Fig. 6.

It is observed that there is a significant increase in efficiency when increasing the number of phases from $M = 4$ to $M = 8$, but not a significant jump when increasing beyond 8.

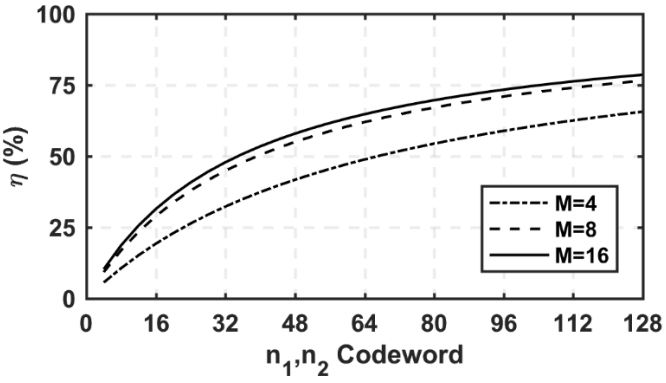

Fig. 6. Drain efficiency versus the number of switching capacitors with different M values.

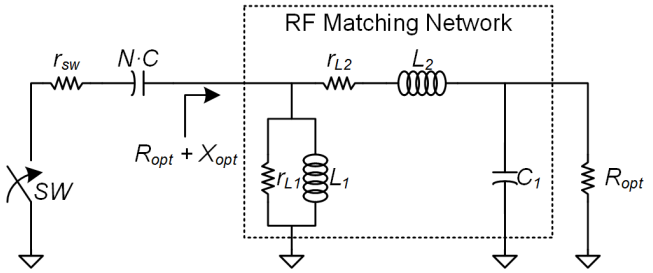

Fig. 7. Circuit schematic for estimating losses in the matching network and due to voltage division.

This is primarily due to the added output power. Another factor in choosing M is that the charge should settle on each capacitor that is switched on phase m before the beginning of phase $m+1$; with the increasing number of phases, there is less time for settling and hence interaction between the phases would cause nonlinearity. In our design, $M = 16$ phases was chosen based on the settling limits and the lack of significant improvement in output power and drain efficiency.

3) Additional Loss Mechanisms: Other losses that affect the overall efficiency (e.g., matching network, voltage division due to switch resistance, parasitic driving power, and clock distribution) are similar to other SCPA implementations [9], [17], [24]. They can be accounted for in the SE calculation, with the addition of terms to capture the voltage division, matching network losses, and additional dc power consumption as follows:

$$\text{SE} = \frac{\alpha^2 \beta P_{\text{out}}}{P_{\text{out}} + P_{\text{SC}} + P_{\text{DR}} + P_{\text{clock}} + P_{\text{misc}}} \quad (31)$$

where α is the voltage division due to switch resistance, β is the attenuation in the matching network, and P_{DR}, P_{clock}, and P_{misc} are the power consumed by the drivers, clock distribution, and all other sources (e.g., pad buffer power, parasitic charging, and logic power), respectively.

The attenuation terms can be accounted for using the schematic shown in Fig. 7. The term α can be found from the voltage division across the switch resistance

$$\alpha = \frac{R_{\text{opt}}}{R_{\text{opt}} + r_{\text{sw}}} \quad (32)$$

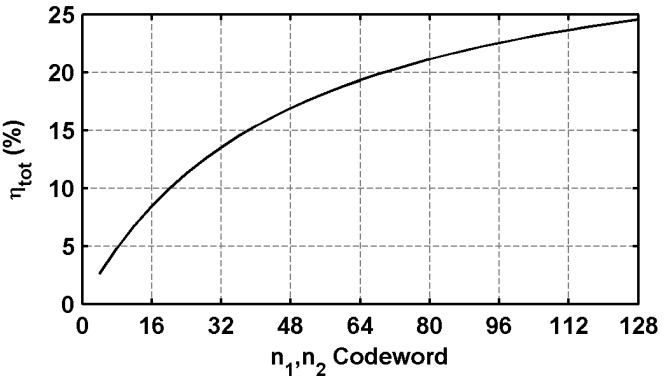

Fig. 8. Total drain efficiency versus input code for an MP-SCPA.

where r_{sw} is the resistance of the output switch. In the design, $R_{opt} = 2.25\ \Omega$ and $r_{sw} = 1\ \Omega$, leading to $\alpha = 0.69$. Similarly, β is found by calculating the attenuation in the matching network [25]

$$\beta \approx \frac{1 - \frac{Q_{NW}}{Q_{L1}}}{1 + \frac{Q_{NW}}{Q_{L2}}} \tag{33}$$

where Q_{L1} and Q_{L2} represent the quality factors of inductors L_1 and L_2, respectively, and Q_{NW} represents the quality factor of the network. The quality factors are found through simulation, $Q_{L1} \approx Q_{L2} \approx 15$ and $Q_{NW} \approx 2.5$, yielding $\beta = 0.71$. The simulation also finds that the total power for all dc terms in the reference design to be discussed in Section III is 120 mW, including all pad drivers and buffers, the clock receiver, and distribution network; in an SoC implementation, the input power would be reduced significantly. The modified SE for an MP-SCPA outputting ~26 dBm with the aforementioned loss factors is plotted versus input code in Fig. 8.

III. Circuit Details

A. Top Level of the 7-b MP-SCPA

The block diagram schematic of the prototype 16-phase MP-SCPA is shown in Fig. 9. Note that a single-ended version is shown although the fabricated circuit is differential. A 7-b unary switched capacitor array is implemented in this design, which is adequate to meet the error vector magnitude (EVM) and close-in out-of-band (OOB) noise specifications for wireless communication standards such as LTE and IEEE 802.11 (e.g., Wi-Fi) [14], [15].

In the proposed architecture, an off-chip phase generator creates 16 evenly distributed phase vectors (ϕ_0–ϕ_{15}) that are input to a clock selection MUX. The MUX is implemented with pass transistor logic. Four bits from a digital pattern generator control digital logic that is used to select the two adjacent phases (ϕ_A–ϕ_B) to the phase of the desired output signal. The phases ϕ_A–ϕ_B are distributed via a clock distribution network to every cell of a 7-b unary capacitor array. This allows any cell to be switched by either ϕ_A or ϕ_B, accommodating cell reuse and allowing the output vector to be steered fully toward either basis phase [16], allowing for larger peak and average amplitude. A 14-b MP logic decoder is used to select whether each capacitor is to be switched by

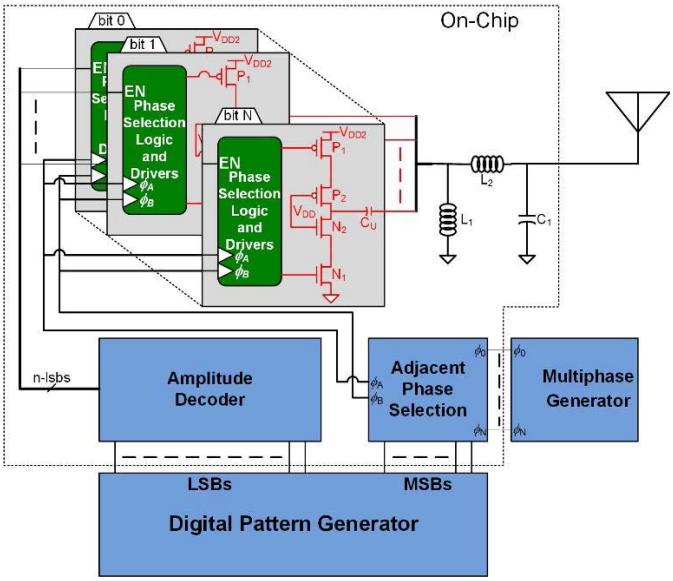

Fig. 9. Block diagram schematic of the prototype 16-phase SCPA.

ϕ_A or ϕ_B or to be ground to V_{GND}. This allows precise control of the output amplitude and phase. The circuit details of the individual blocks are now discussed.

B. Unit Cascoded SCPA

The switch is a cascoded inverter (Fig. 9) that allows for operation with a doubled supply voltage to increase the output power and reduce losses in the output matching network, by reducing the magnitude of the impedance transform required [25]–[27]. For each cell, a level shifter and separate buffer chains are implemented to drive the high side and low side of the switch. To avoid conduction loss, nonoverlapping signals are generated for the switch drivers [24].

C. Phase Selector and Amplitude Decoder Logic

The phase selector comprises a decoder and a MUX tree. The 16-phase clocks are buffered on chip and then input to a pass-transistor MUX. A synthesized decoder controls the MUX and selects two clocks with adjacent phases (ϕ_A and ϕ_B) to the output. A well-matched pair of inverter chains buffer and drive the two selected clocks to each cell of the MP-SCPA, where the amplitude decoder can select whether the capacitor cells are to driven by either ϕ_A or ϕ_B or to be held at ground.

The amplitude decoder logic consists of two sets of thermometer decoders. The first 7-b thermometer decoder decides how many cells n_1 are switched by phase ϕ_A. The second 7-b thermometer decoder decides whether the balance of the cells n_2 are switched by phase ϕ_B or held at ground. The amplitude decoder is implemented in Verilog and synthesized.

The phase and amplitude decoders are both clocked at the same sampling frequency (e.g., 200 Msamples/s) and their data paths are closely matched through careful signal routing. The data are latched after being input to the chip and again before it is input to the decoders. Because of this, the delay mismatch in the paths is minimal, compared with polar DPAs, where the phase signal propagates at the RF carrier frequency

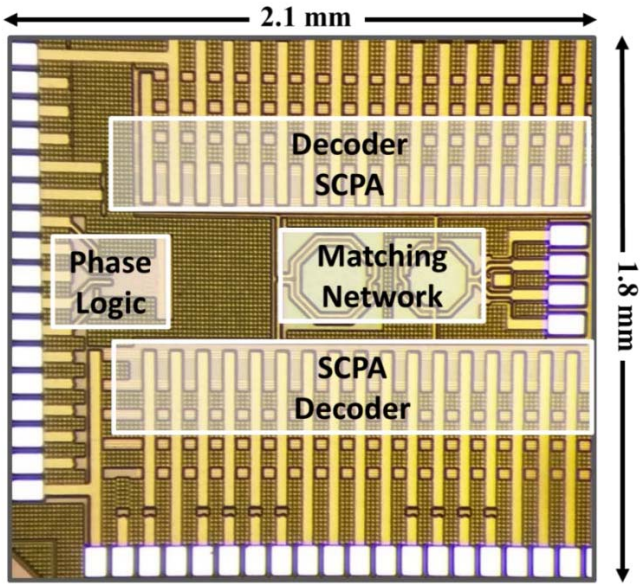

Fig. 10. Chip microphotograph of the prototype 130-nm MP SCPA.

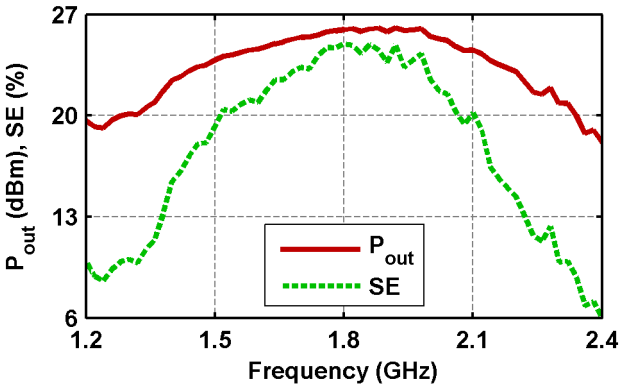

Fig. 11. Measured P_{out} and SE versus frequency.

and the amplitude signal propagates at the sampling rate, resulting in a delay mismatch. Hence, this is the primary benefit of MP architectures. Another way of viewing this is that the amplitude selector selects only the relative phases for combination.

IV. Experimental Results

The prototype MP-SCPA is fabricated in a 130-nm RF CMOS process with ultrathick top metal for high-quality passives. The chip microphotograph is shown in Fig. 10. It occupies a total area of 2.1 mm × 1.8 mm, dominated by the I/O pads for supply and data; SoC implementations would reduce size. A 4-b phase selection decoder (m) selects the two clock phases adjacent to the desired output, whereas two 7-b decoders (n_1, n_2) independently control the capacitors that are switched or held at ground. Most circuitry operates from a supply voltage of 1.5 V, with the exception of the cascoded output switch and their drivers that operate from 1.5 to 3 V.

A. Static Measurements

Shown in Fig. 11 is the measured static output power P_{out} and total SE versus frequencies. It is noted that the total

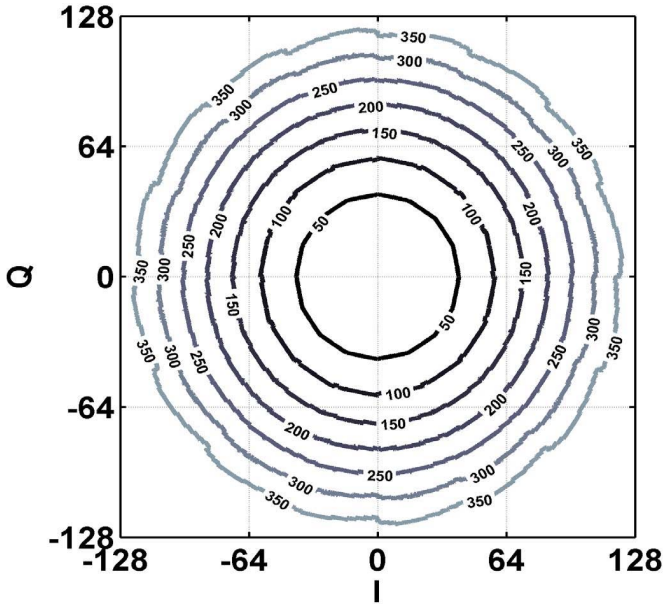

Fig. 12. Measured P_{out} versus input code (n_1, n_2, and m are mapped to IQ). The contour lines represent the measured P_{out} in milliwatts.

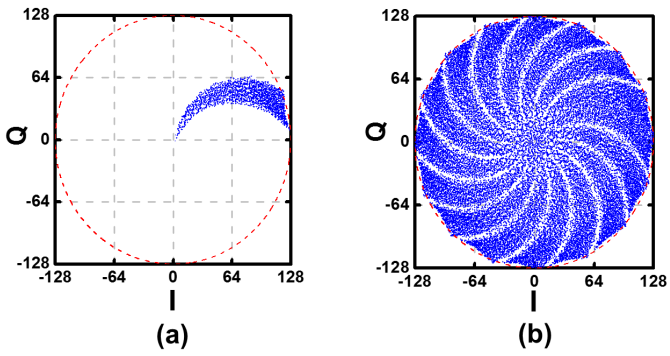

Fig. 13. Measured output for all digital codes using (a) 2 phases and (b) 16 phases.

SE is the ratio of the delivered output power to all input (dc and RF) power coming onto the chip. The PA delivers a maximum output power of 26 dBm with an SE of 24.9% at 1.82 GHz. The measured −3 dB bandwidth of the PA is around 750 MHz, which is consistent with the loaded quality factor of the bandpass matching network.

The output power is plotted as a function of the digital input code in Fig. 12. The digital input codes n_1, n_2, and m are mapped to IQ plane using (19) and (20). The nonlinearity observed at higher output power is caused by the bondwire inductance and the phase offsets of the adjacent clocks. Excess bondwire inductance causes supply and ground bounce and affects the dynamic response at the output in the form of memory effects. Additionally, the difference in the clock's duty cycle and rise/fall time can result in mismatch in the output amplitudes along different phase vectors.

The measured phase and amplitude distortions (AM–PM and AM–AM) are shown in Fig. 13. It is observed that a relatively larger distortion occurs at high power, which can be explained by the interaction between supply/ground bounce

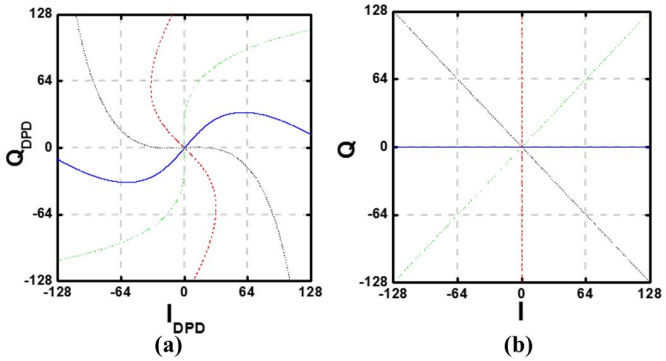

Fig. 14. Measured example output vectors of the (a) predistored input and (b) output after DPD.

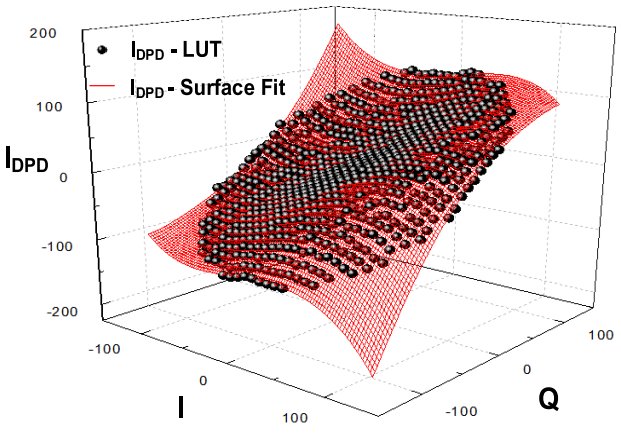

Fig. 15. 2-D surface fit DPD from the measured output of MP-SCPA.

and clock duty cycle mismatch. When the output power is high, the effect of the clock differences enlarges the supply and ground bounce, resulting in a larger difference in output amplitudes switching at different clocks.

B. Digital Predistortion

Nonlinearity in PAs causes spectral mask violations, increased bit error rate resulting from the in-band distortion, and adjacent channel interference due to spectral regrowth. Owing to the low cost and low power of CMOS digital circuitry, it is cost effective and advantageous to linearize the PA using digital predistortion (DPD) at the baseband. In low inductance packages (e.g., flip-chip), the need for DPD in SCPAs can be almost entirely mitigated. However, in packages where supply is provided through a bondwire, the settling behavior of the supply can create distortion; this is true of almost all PAs. In the presented design, the wirebond packaging dictates the need for DPD.

Similar to quadrature DPAs [16], [18], [28], [29], the MP-SCPA requires a 2-D DPD. This can be done in the Cartesian or polar domain. In the presented MP-SCPA, the digital input code (e.g., n_1, n_2, and m) are mapped to the measured output amplitude and phase. To visualize the mapping, both the digital input code and the output amplitude and phase are converted into Cartesian coordinates and plotted in the

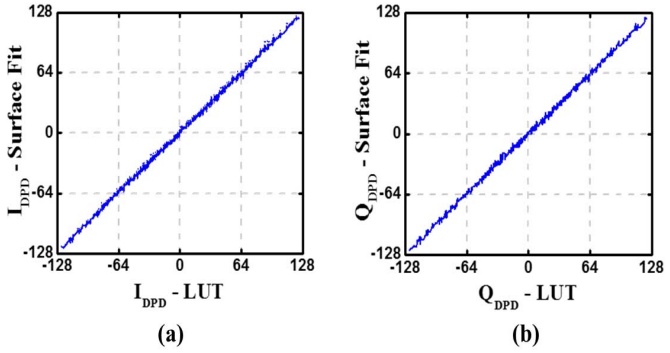

Fig. 16. Comparison between LUT and 2-D surface fit DPD for (a) I_{DPD} and (b) Q_{DPD}.

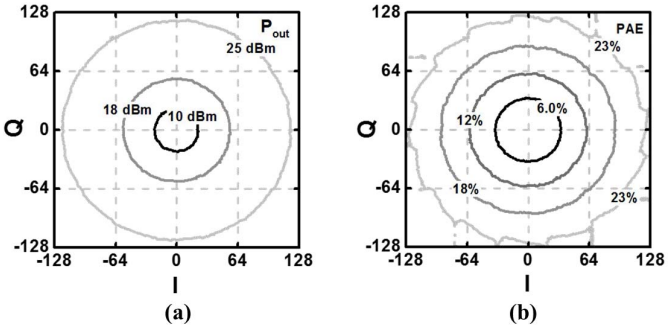

Fig. 17. Measured (with DPD) (a) output power and (b) SE.

complex plane. The measured output with all codes using two adjacent phases are plotted in Fig. 13(a), whereas all possible combinations are plotted in Fig. 13(b).

These measurements are the basis of a lookup table (LUT) that is used to build a digital predistorter. It is noted that such an LUT-based DPD can be very large for all possible combinations of digital input codes. The predistorted input codes are converted into the Cartesian domain and several examples of the predistorted input and linearized output are plotted in Fig. 14(a) and (b), respectively.

A large LUT occupies significant memory, especially when the LUT must be found for different frequency and operating temperatures. Such large LUTs occupy significant die area for memory. To overcome this disadvantage, a 2-D polynomial surface is fit to the measured data. Assuming that I_{DPD} and Q_{DPD} are independent of each other, then they can be expressed as a polynomial function of the in-phase and quadrature inputs, respectively

$$I_{DPD} = \sum_{j=0}^{J} \sum_{k=0}^{k=j} a_{k,j-k} I^k Q^{j-k} \tag{34}$$

and

$$Q_{DPD} = \sum_{j=0}^{J} \sum_{k=0}^{k=j} b_{k,j-k} I^k Q^{j-k}. \tag{35}$$

Equations (34) and (35) represent two different continuous surfaces in a 2-D coordinate system, as shown in Fig. 15. By fitting the surface to the measured data, the desired coefficients $a_{k,j-k}$ and $b_{k,j-k}$ are obtained. A third-order

Fig. 18. Measured ACLR for a 10-MHz, 64 QAM LTE signal (a) without DPD and (b) with DPD.

TABLE I
COMPARISON WITH THE PRIOR ART

	This Work	[17]	[18]	[16]	[8]
Process technology (nm)	130	65	65	28	65
Supply voltage (V)	3	1.2/2.4	1.3	1.1	1.2
Resolution (bit)	7-MP	9-IQ	13-IQ	6-IQ	9-Polar
Carrier Frequency (GHz)	1.8	2.0	2.4	0.800	2.2
Peak P_{out} (dBm)	26	20.5	22.8	13.9	23.3
SE at peak P_{out} (%)	24.9	20.0	34*	40.4	38
Modulation signal	LTE 10 MHz 64-QAM	LTE 10 MHz, 16-QAM	Single carrier 22 MHz, 64-QAM	LTE 10 MHz, 16-QAM	802.11g 20 MHz, 64-QAM
Average P_{out} (dBm)	20.9	14.5	15	6.97	16.8
Average SE (%)	15.2	12.2	NA	29.1	21.8
EVM (%-rms)	3.5	3.6	3.98	NA	3.98
ACLR (dBc)	-30.3/-31.7	-30.7/-31.0	<-43	-32.4/-32.7	NA
Matching Network	On-Chip LC Matching	On-Chip LC Matching	Transformer	No	Transformer
w/ DPD	Yes	Yes	Yes	NA	Yes

*Including Frequency Generation

polynomial expression is determined and it is plotted as the red surface in Fig. 15. Predistorted codes from the 2-D surface fit and the 2-D LUT are compared and plotted in Fig. 16(a) and (b) for the I_{DPD} and Q_{DPD}, respectively. There is a close fit since the surface fit polynomial is constructed from the LUT.

The polynomial DPD saves die area and complexity compared with the LUT. It can also accommodate the effects due to operation temperature and frequency and the memory effects by changes to the polynomial coefficients. To demonstrate the effectiveness of the 2-D surface fit DPD, the output amplitude is plotted in a contour after DPD in Fig. 17(a). It shows a linear response across all possible codewords and phases. The corresponding SE contours are plotted in Fig. 17(b).

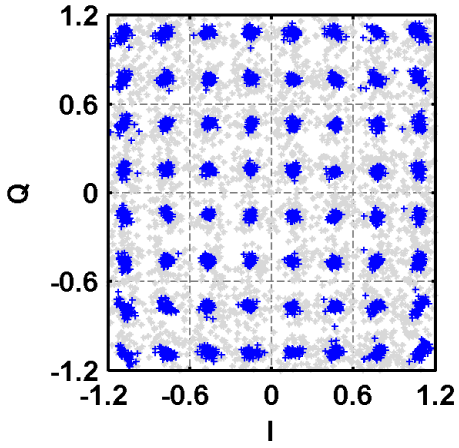

Fig. 19. Measured signal constellation for a 10-MHz, 64 QAM LTE signal (the blue dots represent the signal after DPD and the gray points represent the signal before DPD).

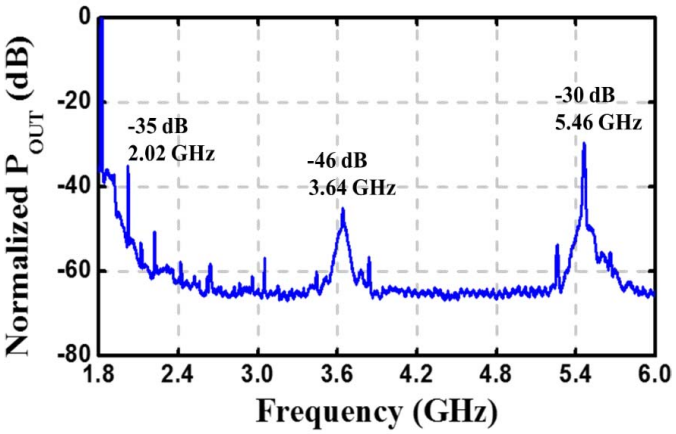

Fig. 20. Measured OOB spectrum for a 10-MHz, 64 QAM LTE signal.

C. Dynamic Measurements

To verify the MP-SCPAs performance with modulated signals, it is tested with a 10-MHz, 64 QAM LTE signal. Without DPD, the ACLR is ≈ -20 dBc as shown in Fig. 18(a). By applying the DPD to linearize the PA, the measured ACLR is less than the specified -30 dBc, as shown in Fig. 18(b). The average output power is 20.9 dBm with a total SE (including pad buffers and all internal circuitry) of 15.2%. The measured EVM is $\approx$3.5%rms after DPD, whereas the EVM is $>$10%rms without DPD. The signal constellation is plotted in Fig. 19.

The far-out OOB noise of the MP-SCPA is dominated by signal quantization. The far-out OOB noise for the 7-b Q-SCPA when transmitting a 10-MHz, 64 QAM LTE signal is plotted in Fig. 20. The OOB noise can be suppressed with higher resolution. The alias at 2.02 GHz is due to the 200-MHz sampling rate of the input LTE signal and it can be further suppressed with a higher sampling rate. The sampling rate and resolution in our design were limited by the instruments available for testing and the pad count available on the die.

V. Conclusion

The concept of MP modulation is introduced and implemented in a prototype MP-SCPA in a 130-nm CMOS. It leverages the advantages of digital PAs while not requiring the wideband phase modulator (e.g., polar DPAs) or having high combining loss (e.g., quadrature DPA). This PA delivers a peak P_{out} of 26 dBm at 1.82 GHz with 24.9% SE. The performance is validated from the static and modulation measurements using a 10-MHz, 64-QAM LTE signal. A 2-D surface fit DPD method is proposed to save die area occupied by a large LUT and to accommodate temperature coefficients and frequency compensation in the future. With DPD, the ACLR is below E-UTRA required -30 dBc LTE standard and the measured EVM is 3.5%rms. A comparison with the prior art is provided in Table I. The MP-SCPA is compared with prior quadrature DPAs and a complete polar transmitter, since the MP-SCPA is a digital transmitter frontend. Though this circuit was implemented in 130-nm technology, it achieves a higher average P_{out} and a higher SE than a quadrature variant in a finer line technology [17]. It should be noted that for the Q-SCPA and MP-SCPA, the SE accounts for all power sources input to the chip, excluding the local oscillator generation.

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