A DC-to-12.5 Gb/s 9.76 mW/Gb/s All-Rate CDR With a Single *LC* VCO in 90 nm CMOS

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***Abstract*— A dual-lane DC-to-12.5 Gb/s all-rate clock and data recovery (CDR) IC with a single LC voltage-controlled oscillator is fabricated in a 90 nm CMOS. An all-rate clock divider with an asynchronous phase calibration scheme is employed to generate all-rate clock signals without a phase mismatch or duty cycle distortion. The IC features an automatic loop gain control scheme that adjusts the bandwidth of a CDR in the background for optimal bit error rate (BER) performance by monitoring the phase difference between the incoming data and the recovered clock signal. The proposed CDR consumes 244 mW at 12.5 Gb/s under dual-lane operation with an input sensitivity of 12 $mV_{pp,diff}$. The CDR supports referenceless all-rate operation with a BER $< 10^{-12}$ on PRBS31 and compensates for 20 dB of channel loss using a continuous-time linear equalizer (CTLE), a one-tap decision feedback equalizer (DFE), and a three-tap pre-emphasis filter. The power efficiency of the test chip is 9.76 mW/Gb/s.**

***Index Terms*— All-rate CDR, all-rate clock divider, asynchronous calibration loop, automatic loop gain calibration, backward compatibility, clock and data recovery, continuous rate, referenceless clock and data recovery, stochastic reference clock generator (SRCG).**

I. Introduction

THE ever-increasing data rate demands necessitate the emergence of new communication standards operating at higher data rates. Network equipment employing conventional CDRs [1]–[5] cannot offer backward compatibility because the frequency range of a voltage-controlled oscillator (VCO) is narrow in nature. As such, >25 Gb/s CDRs are generally required to include a bypass mode to support legacy 10 Gb/s links [6], [7]. However, the signal integrity degradation and routing complexity when large digital circuit blocks reside between RX and TX are drawbacks of the bypass mode design because the input data should be driven by multistage CML buffers from the input of the CDR to the output.

Recently, several wide-range CDRs [8]–[25] have been proposed to achieve backward compatibility by using a wide-range clock generator (CG). Those wide-range CDRs are generally implemented with either a ring VCO, multiple *LC* VCOs, or a combination of both. Ring VCO-based wide-range CDRs [8]–[17] are common for such applications because the operational frequency range of a CDR can be easily extended with a negligible area penalty. In such ring-VCO-based designs, a high-bandwidth supply regulator or an additional jitter filtering loop with external elements are typically employed to suppress excessive jitter. Nevertheless, the inherent poor spectral purity of the ring VCO makes itself vulnerable to external interferences, which prohibit its widespread commercial use. *LC* VCO-based wide-range CDRs [18]–[22] have also been proposed to support backward compatibility without sacrificing the jitter performance. In such designs, multiple narrow-range *LC* VCOs are employed to facilitate wide-range CDR operation and achieve good jitter performance. However, the requirement of a large chip area is the main drawback. Wide-range CDRs employing both ring and *LC* VCOs [23]–[25] mitigate the aforementioned problems to some extent. In this design, the number of *LC* VCOs can be reduced by using a ring VCO for the low-data-rate regime. However, poor jitter performance in the low-data-rate regime and relatively large chip area due to more than one *LC* tank are some limitations.

In this paper, a dual-lane all-rate CDR with a single *LC* VCO is presented [26]. An all-rate CG is implemented by using a CMOS-based all-rate clock divider together with a narrow-range *LC* VCO. An asynchronous phase calibration scheme is employed to suppress phase mismatch among multiphase clock signals and duty cycle distortion caused by the CG. The proposed design employs referenceless clock recovery and automatic loop gain control (ALGC) [27] schemes for optimal plug-and-play operation. The ALGC algorithm adjusts the CDR bandwidth automatically in the background to minimize the phase difference between the input data and the recovered clock signal. A built-in self-test (BIST) module is implemented internally to validate the performance of the ALGC algorithm.

Section II describes the overall architecture of the proposed all-rate CDR. In Section III, an all-rate CG including the proposed all-rate clock divider and the asynchronous calibration loop is introduced, and Section IV describes the principle of the ALGC and the measurement result of the ALGC operation. The measured results of the proposed all-rate CDR are presented in Section V. Section VI concludes this paper with a summary.

II. CDR Architecture

Fig. 1 shows the overall architecture of the proposed all-rate CDR. It consists of a global CG with a single *LC* tank and two CDR lanes comprising an analog front-end, a quadrature transceiver (TRX), and a stochastic reference CG (SRCG). The

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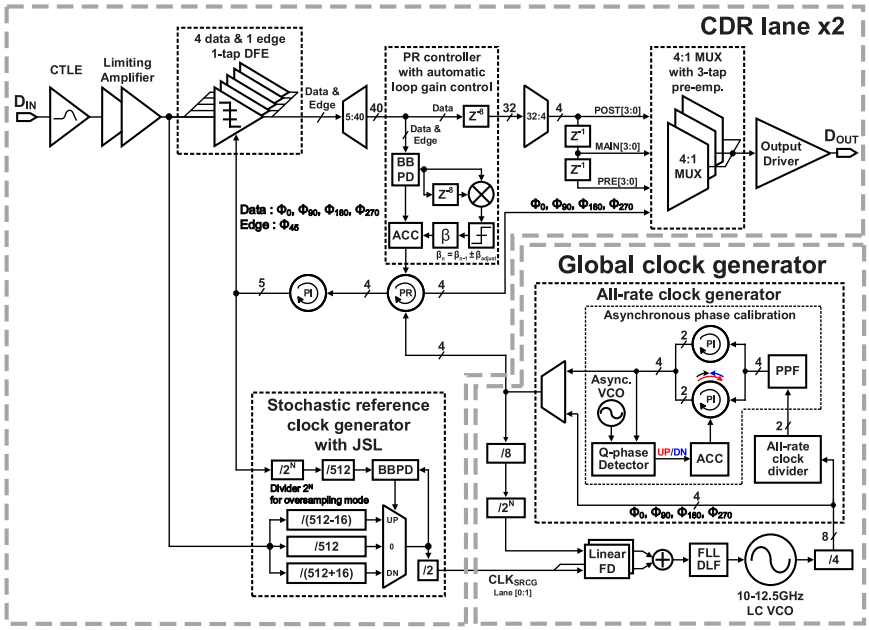

Fig. 1. Top block diagram of the proposed all-rate CDR architecture.

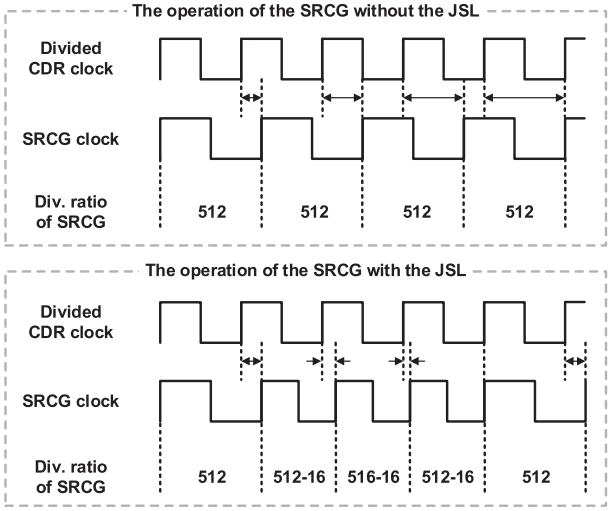

Fig. 2. Timing diagram in the operation of the JSL when the transition density of the input data is low.

global CG includes the all-rate clock divider for frequency generation and employs an asynchronous phase calibration scheme to reduce deterministic jitter created during the clock generation.

For the referenceless frequency acquisition, cascaded data dividers in the SRCG of each channel extract the input frequency information by creating a quasi-periodic reference clock signal through dividing the input data [8], [28]. The jitter suppression loop (JSL) automatically controls the division ratio of the SRCG based on the recovered CDR clock signal to suppress the accumulation jitter from the SRCG and desensitize the SRCG from the transition density [29].

The JSL consists of a data divider with a controllable division ratio and a bang-bang phase detector (BBPD). The BBPD in the JSL detects the instant frequency shift of the SRCG by using the CDR clock signal as a reference signal, and the division ratio of the data divider in the JSL is adjusted by ± 16 to counterbalance the frequency drift of the SRCG output [29]. Note the clock signal of the CDR has smaller instantaneous frequency offset compared to that of the SRCG thanks to the jitter filtering of the CDR loop. The conceptual operational timing diagram of the JSL in the case with a low data transition density is shown in Fig. 2. As a consequence, jitter-suppressed SRCG output cleans the CDR clock signal, and in-turn, a cleaner CDR clock signal makes the SRCG output even cleaner in a bootstrap manner.

The output of the SRCG from each channel is fed to counter-based linear frequency detectors in the global CG. The outputs of the frequency detector are linearly combined in the digital loop filter (DLF) of the frequency-locked loop. As a result, the frequency of the locked VCO is equivalent to the average data rate of each channel. The full-rate VCO clock signal is divided by a factor of 4 to implement a quadrature TRX, which saves power and area by enabling extensive usage of CMOS logic gates in the clock-and-data paths. The all-rate clock divider followed by an asynchronous phase calibration block generates puncture-less all-rate multiphase clock signals.

In the data path, a CTLE compensates for the channel loss up to 20 dB at Nyquist, and a limiting amplifier (LA) offers a broadband gain of 20 dB. Severe channel loss in a long lossy channel is compensated by suppressing the low frequency gain in the CTLE, which results in overall attenuation of the input signal. As such, the output of an LA satisfies sufficient linearity condition for the DFE under channel loss. In contrast, a large incoming signal in a short link does not rely heavily on the equalization capability of the CTLE and DFE, thus an LA with finite gain imposes a negligible bit error rate (BER) penalty in practical links. Parallel track-and-holds are employed as an input sampler. A DC offset calibration scheme is applied for the CTLE, LA, and input sampler. The input sampler comprises four data comparators and one edge comparator for power savings. The data- and edge-sampling clock signals are generated by using 7-bit phase

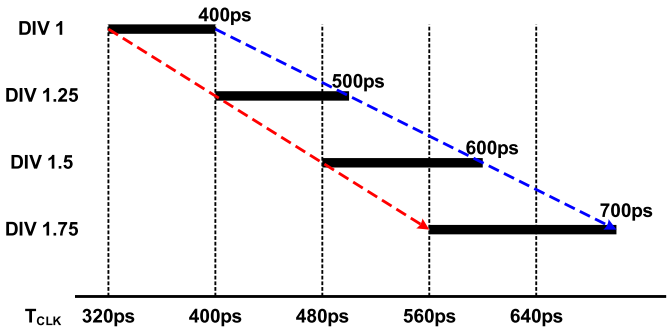

Fig. 3. Conceptual time-domain coverage of the all-rate CG.

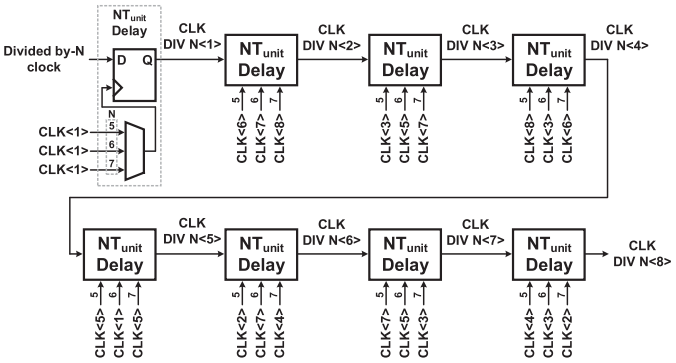

Fig. 4. Block diagram of the MDCG.

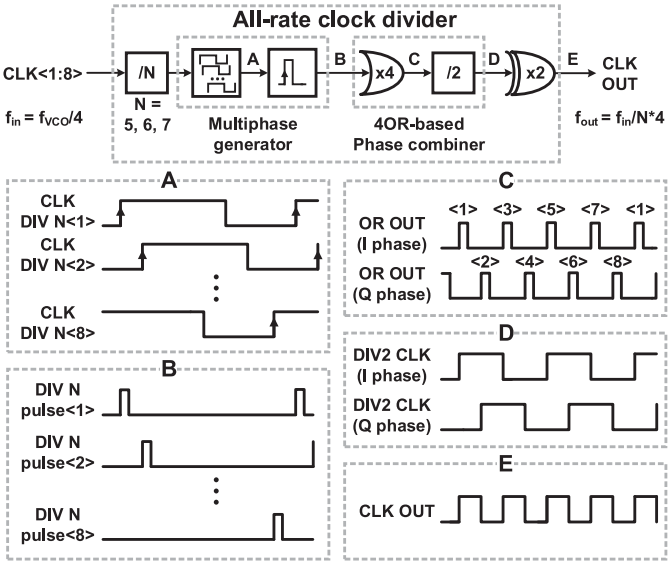

Fig. 5. Architecture of the proposed all-rate clock divider and the waveform of each output.

interpolators (PIs) subsequent to phase rotators. The sampled data are deserialized by a factor of eight considering the operating frequency of the synthesized logic blocks. A 7-bit phase rotator controller (PRCON) employs a second-order DLF for the frequency offset tracking, and the ALGC in the PRCON determines the optimal loop bandwidth that minimizes the phase error between the input data and the recovered clock signal. The 32-parallelized input data at the PRCON are serialized by a 32:4 CMOS logic multiplexer (MUX) and a pseudo NMOS 4:1 MUX for retransmission. The output driver implements a three-tap pre-emphasis filter.

III. All-Rate Clock Generator

The tuning range of the VCO in the all-rate CG is $\pm 11.1\%$. A 10-to-12.5 GHz VCO clock signal is divided by a factor of four using a multiphase clock divider. The divided quadrature clock signals are time shifted to each other by a half-period, T_{half}, of the VCO clock signal. An all-rate CG creates continuous clock frequencies in the divide-by-4 clock domain as if the VCO has a frequency coverage of $f_{\max}/2$ to $f_{\max}$. The created differential clock signals are converted into mismatch-calibrated quadrature phase clock signals using a polyphase filter for quadrate operation, and a subsequent asynchronous phase calibrator (APC) removes phase mismatches and duty cycle distortion.

A. All-Rate Clock Divider

Conceptual time-domain coverage of the all-rate CG is shown in Fig. 3. Because the all-rate CDR operates in quadrate, the sampling clock period ranging from 320 to 640 ps must be generated for all rate operations up to 12.5 Gb/s. Any clock periods longer than 640 ps are integer multiples of the generated fractional clock signal between 320 and 640 ps. Hence, the proposed CDR operates in the oversampling mode for data rates below 6.25 Gb/s. Because the div-4 clock signal covers the clock periods from 320 to 400 ps, the proposed all-rate clock divider is designed to cover the clock periods between 400 and 640 ps continuously for puncture-less all-rate operation.

The clock period of 400 ps is created from multiphase clock signals with the period of 320 ps by using a frequency division factor of 1.25, which is equivalent to a frequency division by a factor of five of a 12.5 GHz clock signal. When the division ratio is 1.25, the divider covers between 400 and 500 ps. Similarly, the coverage is 480–600 and 560–700 ps when the division ratio is 1.5 and 1.75, respectively (see Fig. 3). The division factors of 1.5 and 1.75 are equivalent to a division factor of 6 and 7 of the VCO clock signal, respectively. Because the fractional ratio of 0.25 in the quadrate domain is equivalent to a half-period, T_{half}, of the VCO clock signal, such a division factor can be achieved through proper edge selection from the quadrature phase clock signals.

The div-N ($N = 5, 6, 7$) clock signal of the VCO has rising and falling edges separated by NT_{half}. To create such div-N clock signals, a pulse train with a period of NT_{half} is created and then frequency divided. As the first step, the differential quadrate clock signals (total eight phases) are divided by a factor of N. Multiphase clock division is implemented by triggering the div-N signal with selected quadrature clock signals with time spacing of NT_{half}. Fig. 4 shows the block diagram of the multiphase division CG (MDCG). The MDCG consists of eight edge-triggered registers; the triggering clock phase of the register is $\text{CLK}\langle \bmod(kN, 8) + 1\rangle$ ($k = 0, 1, 2, \ldots$), where k denotes the phase index of div-N. To balance the delay among eight phase output clock signals, a dummy register is employed as a load capacitance at the node of CLK DIV $N\langle 8\rangle$.

The locations of the rising edges of the divided clock signals have time domain separations of NT_{half} (see A in Fig. 5). The generated multiphase clock signals are transformed into

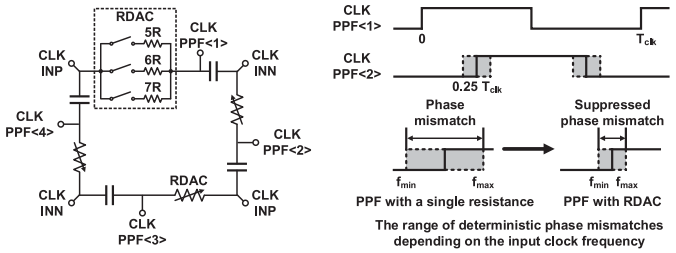

Fig. 6. Architecture of RDAC-based polyphase filter and the diagram of the output quadrature clock signals.

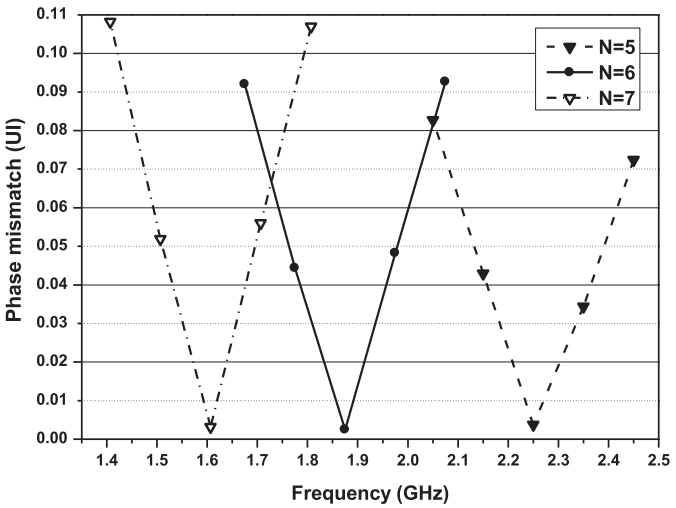

Fig. 7. Simulated absolute phase mismatches in UI with the RDAC-based polyphase filter for each division ratio of N.

pulse trains aligned at every rising edge of the divided clock signals (see B in Fig. 5). Even and odd phase pulse trains are separately gathered by using a four-input OR gate (see C in Fig. 5) and converted into clock signals (see D in Fig. 5). The generated quadrature clock signals are then converted into targeted div-N clock signals through logical XOR operation (see E in Fig. 5). The multiphase pulse trains can be combined all at once and converted into a targeted clock signal through frequency division. However, this approach requires wide circuit bandwidth, thus CMOS logic gates cannot be used. The width of the pulse shown in Fig. 5 (B) is chosen carefully considering the bandwidth requirement of the CMOS OR gates and registers for frequency division. The all-rate clock divider generates only a single-phase div-N clock signal to save power and area. The maximum simulated deterministic jitter of the div-N CG is 0.0015 UI in 10 Gb/s operation.

B. Multiphase Generation and Asynchronous Phase Calibration

To generate quadrature clock signals, a polyphase filter is employed. Because the phase response of a polyphase filter is susceptive to the operating frequency, a resistor DAC (RDAC) is incorporated for phase adjustments. A detailed circuit schematic and the timing diagram of the output quadrature clock signals are shown in Fig. 6. The RDAC in the polyphase filter provides three different resistances, which corresponds to the cases of $N = 5, 6, 7$ in the all-rate clock divider. Fig. 7 shows simulated absolute phase mismatches in UI

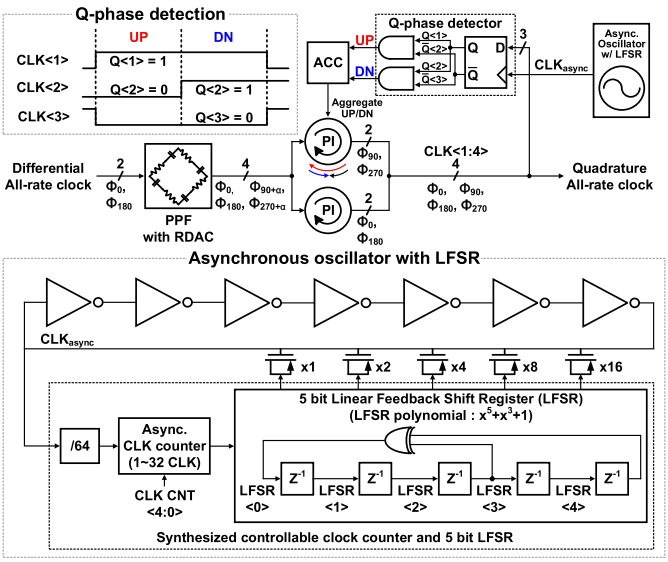

Fig. 8. Block diagram of an asynchronous phase calibration loop.

with different RDAC values when $N = 5, 6, 7$. The phase mismatches are suppressed within 0.11 UI because of the resistive tuning scheme, which is a 66% reduction from those with the fixed resistor case.

To reduce residual phase mismatches among quadrature clock signals under PVT variations, an APC is employed. Fig. 8 shows the block diagram of the APC. The APC comprises a PI, a Q-phase detector, an accumulator, and an asynchronous clock oscillator. The APC samples quadrature clock signals with an asynchronous clock signal and generates up and down (UP/DN) signals using the Q-phase detector. Owing to the high phase-domain resolution of the asynchronous sampling scheme, accumulated UP/DN signals indicate a precise quantitative long-term phase mismatch. The APC adjusts the phase of quadrature phase clock signals as illustrated in Fig. 9. UP and DN signals are generated by sampling the quadrature clock signals at the output of a PI with an asynchronous clock signal. When the sampling location is between CLK⟨1⟩ and CLK⟨2⟩ (see Fig. 9), the phase detector generates a UP signal. In case the sampling location is between CLK⟨2⟩ and CLK⟨3⟩, the phase detector generates a DN signal. An accumulator gathers these UP and DN signals to control the phase of the PI to balance the total number of UPs and DNs.

In case the frequency of the all-rate clock, f_{clk}, is close to an integer multiple of that for the asynchronous clock signal, f_{async}, the periodic time shift between consecutive samples $\Delta T_{\mathrm{shift}}$ is small. The periodic time shift $\Delta T_{\mathrm{shift}}$ is given by

$$\Delta T_{\mathrm{shift}} = \frac{1}{f_{\mathrm{async}}} - \frac{N_{\mathrm{ratio}}}{f_{\mathrm{clk}}} = \frac{f_{\mathrm{clk}} - N_{\mathrm{ratio}} f_{\mathrm{async}}}{f_{\mathrm{async}}} T_{\mathrm{clk}} \qquad (1)$$

where N_{ratio} is the nearest integer ratio between the clock frequencies given by $[f_{\mathrm{clk}}/f_{\mathrm{async}}]$, and T_{clk} is the period of the all-rate clock signal. Because the UP/DN signals are generated during a quarter-period of the all-rate clock signal (see Fig. 8), the number of consecutive UP/DN signals, N_{cons}, and the optimal number of truncation bits to suppress the

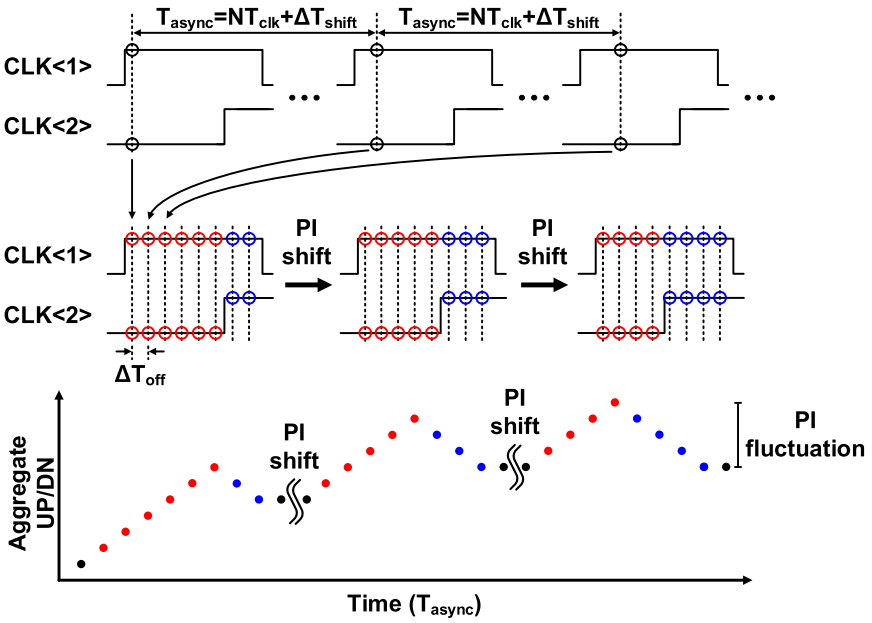

Fig. 9. Phase adjustment in the asynchronous phase calibration and the PI fluctuation of aggregate UP/DN signals in the accumulator.

cyclic fluctuation, N_{trunc}, are

$$N_{\text{cons}} = \frac{T_{\text{clk}}}{4|\Delta T_{\text{shift}}|} = \left|\frac{f_{\text{async}}}{4(f_{\text{clk}} - N_{\text{ratio}} f_{\text{async}})}\right|$$

and

$$N_{\text{trunc}} = \log_2\left(\left|\frac{f_{\text{async}}}{4(f_{\text{clk}} - N_{\text{ratio}} f_{\text{async}})}\right|\right) \tag{2}$$

respectively. In case an integer multiple frequency of the asynchronous clock signal, $N_{\text{ratio}} f_{\text{async}}$, is identical to that of the all-rate clock signal, ΔT_{shift} is zero, and the number of consecutive UP/DN signals is infinite. As such, the asynchronous clock frequency is adjusted continuously by using a 5-bit cap bank controlled by a linear feedback shift register (LFSR). The LFSR generates pseudorandom control bits for the 5-bit cap bank to randomize the asynchronous clock frequency. The periodic time shift between consecutive samples at a state index k, by using $T_{\text{async·LFSR·}k} = T_{\text{async}} + \Delta T_{\text{shift·LFSR·}k} = T_{\text{async}} \times f_{\text{async}}/(f_{\text{async}} + (k - 2^{N_{\text{LFSR}}-1}) f_{\text{LSB·LFSR}})$, is then

$$\Delta T_{\text{shift·LFSR·}k} = -\frac{N_{\text{ratio}}(k-2^{N_{\text{LFSR}}-1}) f_{\text{LSB·LFSR}}}{f_{\text{async}} + (k-2^{N_{\text{LFSR}}-1}) f_{\text{LSB·LFSR}}} T_{\text{clk}} \tag{3}$$

where $f_{\text{LSB·LFSR}}$ is the frequency-domain LSB of the LFSR, and N_{LFSR} denotes the total number of LFSR states. To accumulate a sufficient number of UP/DN signals in each LFSR state, an asynchronous clock counter is employed to count the number of rising edges for the asynchronous clock and shifts the logic state once the counted value reaches the preprogramed target value of 32. Suppose the time shift $\Delta T_{\text{shift·LFSR·}k}$ at the Nth state of the LFSR is zero because $N_{\text{ratio}} f_{\text{async}} = f_{\text{clk}}$; the minimum time shift then occurs at the $(N+1)$st state, and the resolution of the counter N_{counter}

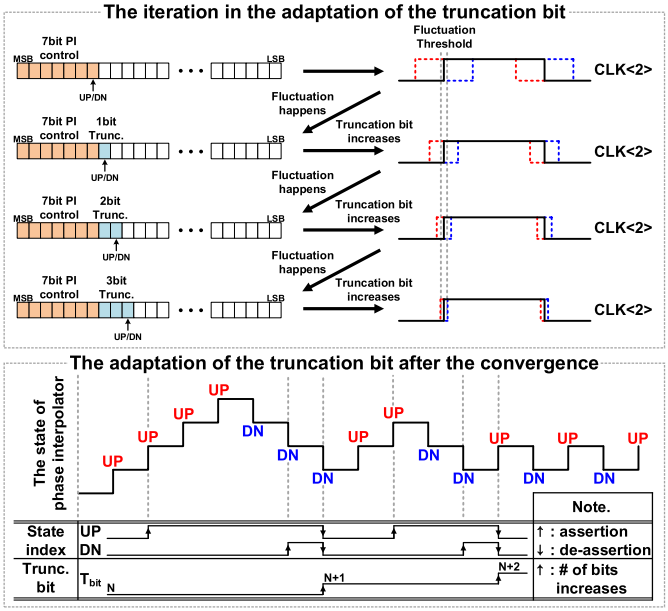

Fig. 10. Operation procedure of the truncation bit control scheme.

should be

$$N_{\text{counter}} = \log_2\left(\frac{T_{\text{clk}}}{|\Delta T_{\text{shift·LFSR·}2^{N_{\text{LFSR}}-1}+1}|}\right) = \log_2\left(\left|\frac{f_{\text{async}} + f_{\text{LSB·LFSR}}}{N_{\text{ratio}} f_{\text{LSB·LFSR}}}\right|\right). \tag{4}$$

Because the integer ratio of the clock frequencies, N_{ratio}, is set to 64 and the frequency resolution of the LFSR, $f_{\text{LSB·LFSR}}/f_{\text{async}}$, is 500 ppm, the resolution of the counter is set to 5 bits. Consequently, the pseudorandom phase sampling enabled by an LFSR suppresses the fluctuation of the logic state of the APC significantly.

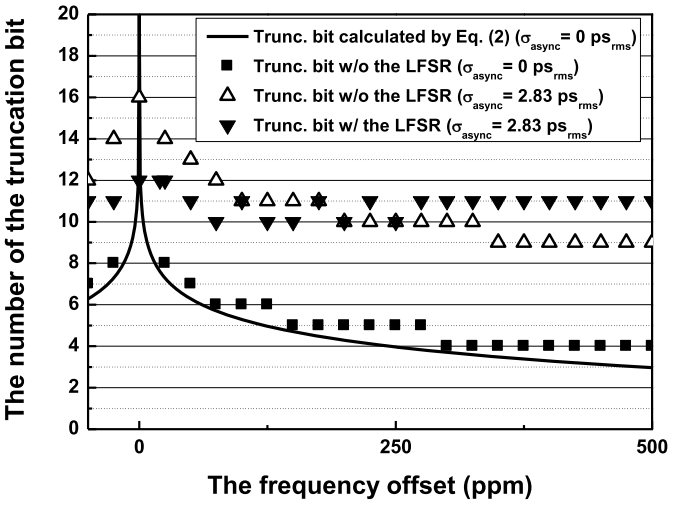

Fig. 11. Required number of truncation bits with various frequency offsets between all-rate clock signal and the asynchronous clock signal, and the simulated result with the proposed bit truncation process.

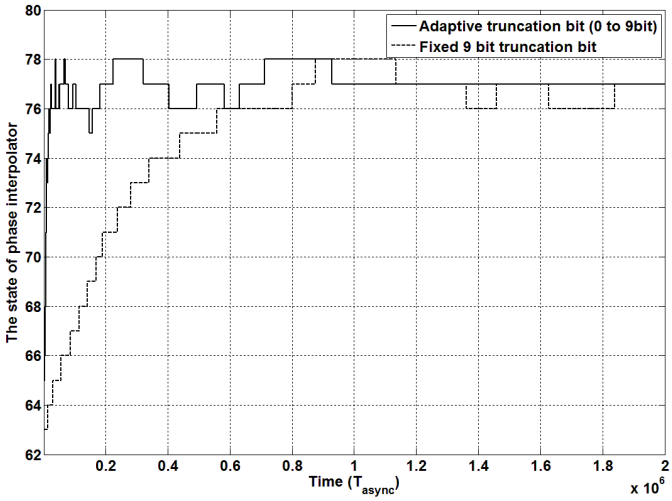

Fig. 12. Simulated state convergence using the fixed- and adaptive-truncation bits in the asynchronous phase calibration loop.

C. Dynamic Truncation for Fast Transient Response

To suppress the residual PI state fluctuation of the APC in the steady state (see Fig. 9) without deteriorating the transient response, the number of truncation bits in the accumulator is adjusted automatically by controlling the resolution of the accumulator. The increase in the truncation bits of the accumulator is equivalent to the reduction of the integrator gain, which, in turn, reduces the closed-loop bandwidth of the calibration loop. The bit truncation process suppresses periodic signal fluctuation effectively while identifying valid signal in a nonlinear manner. The resolution of the accumulator varies between 7 and 22 bits, where the number of PI control bits is 7. Initially, the resolution of the accumulator is made identical to that of the PI control bits. In case the PI control signal demonstrates cyclic fluctuation, a bit truncation is performed by increasing the resolution of the accumulator while assigning the MSBs for the PI control (see Fig. 10).

To achieve fast convergence, the number of truncation bits in the accumulator is increased only when consecutive UP and DN signals appear successively. A state UP index is asserted when consecutive UPs appear, and a state DN index is declared with sequential DN signals. In case both state indexes are asserted sequentially, the number of truncation bits is increased, and the accumulator deasserts both indexes. Fig. 10 illustrates the operation of the proposed dynamic truncation scheme. The dynamic bit truncation process achieves fast convergence while suppressing state–state clock jitter.

To demonstrate the effectiveness of the bit truncation process, the analytic number of truncation bits calculated by (2) and the simulated number of truncation bits under various conditions are compared as shown in Fig. 11. The converged number of truncation bits controlled by the proposed scheme approaches the analytic optimal number of truncation bits, N_{trunc}, under various frequency offsets in the jitter-free condition. In addition, accumulation jitter of the asynchronous clock signal is considered for the sake of practicality. By integrating the phase noise of -100 dBc/Hz at a 1–MHz frequency offset from 100 kHz to 40 MHz, the estimated standard deviation of the clock jitter, σ_{async}, is 2.83 ps_{rms}. According to the behavioral simulation, the maximum required number of truncation bits without the LFSR approaches 16. However, the required maximum number of truncation bits with the LFSR is reduced to 12. This maximum required number of truncation bits with the LFSR is achieved when the total accumulated time period of the LFSR is identical to an integer multiple of that for the all-rate clock signal as given by

$$\begin{aligned} T_{\text{async}\cdot\text{LFSR}} &= \sum_{k=1}^{2^{N_{\text{LFSR}}}-1} 2^{N_{\text{counter}}} T_{\text{async}\cdot\text{LFSR}\cdot k} \\ &= T_{\text{async}} \times \sum_{k=1}^{2^{N_{\text{LFSR}}}-1} \frac{2^{N_{\text{counter}}} f_{\text{async}}}{f_{\text{async}} + (k - 2^{N_{\text{LFSR}}-1}) f_{\text{LSB}\cdot\text{LFSR}}} \\ &= 2^{N_{\text{counter}}} (2^{N_{\text{LFSR}}} - 1) N_{\text{ratio}} T_{\text{clk}} \end{aligned} \tag{5}$$

where $2^{N_{\text{counter}}}$ denotes the number of samples per LFSR state. The asynchronous clock frequency requiring maximum truncation bits, $f_{\text{async}\cdot\text{T}_{\max}}$, is

$$\begin{aligned} f_{\text{async}\cdot\text{T}_{\max}} &= \frac{\sum_{k=1}^{2^{N_{\text{LFSR}}}-1} \frac{2^{N_{\text{counter}}} f_{\text{async}\cdot\text{T}_{\max}}}{f_{\text{async}\cdot\text{T}_{\max}} + (k - 2^{N_{\text{LFSR}}-1}) f_{\text{LSB}\cdot\text{LFSR}}}}{2^{N_{\text{counter}}} (2^{N_{\text{LFSR}}} - 1) N_{\text{ratio}} T_{\text{clk}}} \\ &= \frac{\sum_{k=1}^{2^{N_{\text{LFSR}}}-1} \frac{1}{1 + (k - 2^{N_{\text{LFSR}}-1}) f_{\text{LSB}\cdot\text{LFSR}} / f_{\text{async}\cdot\text{T}_{\max}}}}{(2^{N_{\text{LFSR}}} - 1) N_{\text{ratio}}} f_{\text{clk}}. \end{aligned} \tag{6}$$

The frequency offset requiring the maximum number of truncation bits is 20 ppm when the frequency resolution of the LFSR, $f_{\text{LSB}\cdot\text{LFSR}}/f_{\text{async}\cdot\text{T}_{\max}}$, is 500 ppm. In our design, the number of truncation bits is set to 15 considering PVT variations. Simulated state convergence using a fixed truncation scheme and the proposed adaptive truncation scheme is compared in Fig. 12. In this simulation, the fixed truncation

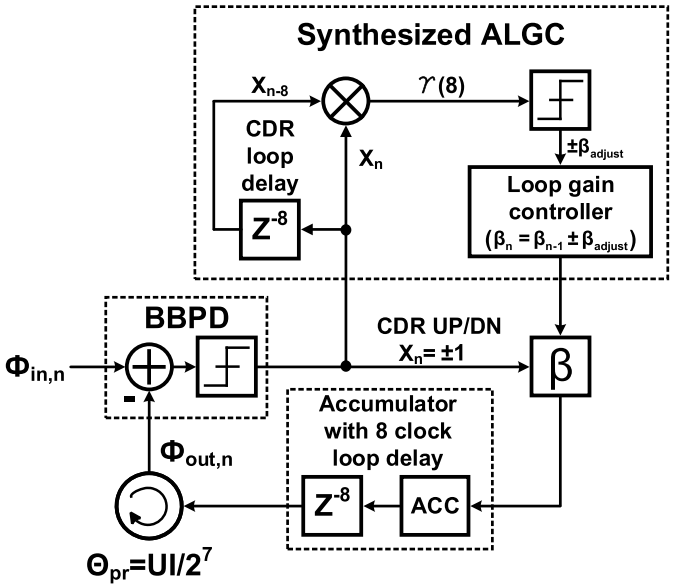

Fig. 13. Block diagram of the ALGC algorithm.

scheme employs nine truncation bits. It is clear that the proposed adaptive truncation scheme achieves faster convergence while suppressing limit cycle oscillation compared to the fixed truncation scheme.

IV. Automatic Loop Gain Control

Excessive loop gain makes the recovered clock signal oversensitive to the random period jitter, whereas insufficient loop gain jitter reduces the tracking capability of a CDR. In conventional all-rate CDRs targeting multiple communication standards, the loop gain should be adjusted manually for optimal BER performance based on given jitter tolerance specifications. However, the ALGC scheme enables plug-and-play operation by finding the optimal loop gain in the background regardless of the data rate or link conditions.

Fig. 13 depicts the block diagram of the ALGC algorithm employed in the proposed all-rate CDR design. The optimal loop gain that minimizes the mean-squared phase error between the input data and the recovered clock of a CDR can be derived analytically in case the input jitter can be modeled by a random walk process. In such a case, the optimal loop gain is the random walk step size σ_W of the input data [30]. Note that the jitter in an actual link resembles random noise, and sinusoidal jitter is used only for testing purposes. The ALGC algorithm controls the loop gain by monitoring the correlation between consecutive BBPD outputs, where it is proven that the optimal loop gain minimizes such correlation [27]. Intuitively speaking, the outputs of a BBPD will show a strong correlation if the loop gain is set too small or large—i.e., the same consecutive signs in a case with a small loop gain and opposite signs in a case with a large loop gain. Because the delay of the designed CDR loop is eight clock cycles, the autocorrelation of the BBPD output with eight cycle delays, $\gamma(8)$, is monitored continuously, and the CDR loop gain is updated to minimize the autocorrelation.

The clock delay N in the autocorrelation $\gamma(N)$ should be set identical to that of the CDR loop. In case N is set greater than the loop delay, the converged CDR loop gain is smaller than the optimal value. This is because the autocorrelation between longer delayed samples corresponds to the power of lower frequency input jitter, which can be tracked with lower gain because more time is given for the tracking. Note that the clock delay of eight cycles has a negligible impact on the loop gain estimation because the frequency of the input jitter specified in the jitter tolerance mask is sufficiently lower than the reciprocal of the loop delay.

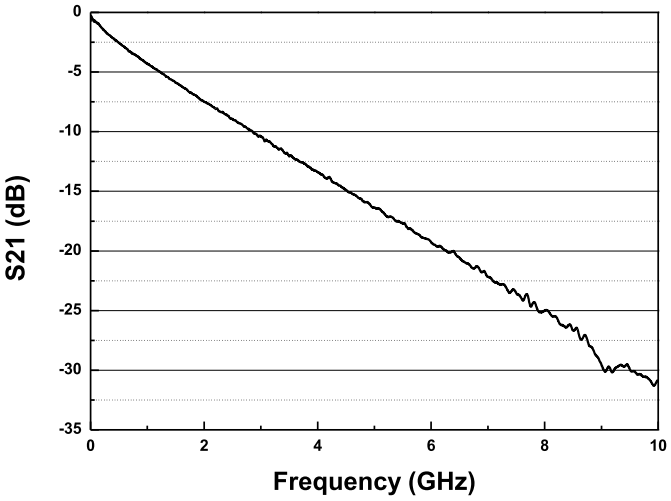

Fig. 14. Measured channel loss of 60 cm FR4 channel.

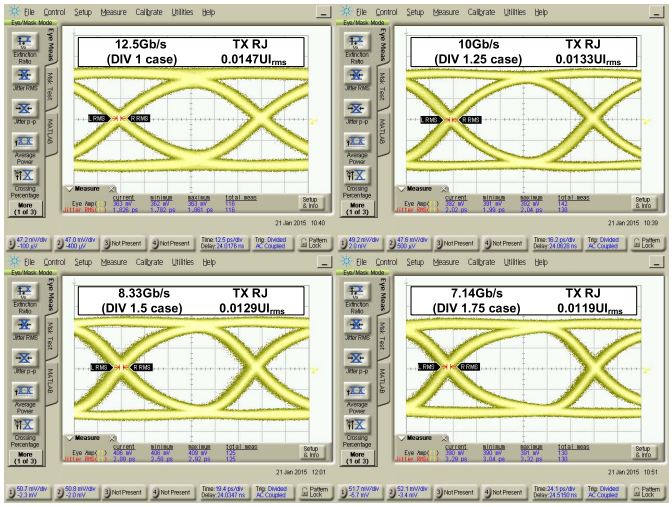

Fig. 15. Measured eye diagrams at each fractional division ratio.

V. Measurements and Results

The test chip consumes 244 mW at 12.5 Gb/s under dual-lane operation with a sensitivity of 12 $mV_{pp,diff}$. The CDR operates from 50 Mb/s to 12.5 Gb/s without a reference clock signal with a BER $< 10^{-12}$ on PRBS31 under 20 dB loss channels at Nyquist. The measured channel loss of a 60 cm FR4 channel is shown in Fig. 14. A wideband ring VCO is also implemented for a performance comparison with the proposed single *LC* VCO-based all-rate CDR design. The recovered clock jitter of *LC*- and ring-VCO-based CDR designs are 2.6 and 5.8 ps_{rms}, respectively, in the referenceless mode.

TABLE I
COMPARISON OF THE CDR PERFORMANCE

	JSSC 2011 [8]	ISSCC 2014 [9]	ISSCC 2009 [16]	CICC 2014 [19]	JSSC 2011 [22]	CICC 2014 [23]	ISSCC 2015 [25]	This work (Ring VCO)	**This work**
Technology	0.13μm	65nm	65nm	0.13μm	40nm	20nm	20nm	90nm	**90nm**
Supply (V)	1.2/0.8	1.2/1.0	1.2	3.3/1.8/1.2	1.1	1.2/1.0/0.95	1.2/1.0/0.95	1.0	**1.0**
Architecture	Half rate Single RX	Half rate Single RX	Quad rate Single lane	Half rate Single lane	Half rate Quad-lane	Half rate Quad-lane	Half rate Quad-lane	Quad rate Dual-lane	**Quad rate Dual-lane**
TRX Equalizer	X	X	X	CTLE	CTLE, 10-tap DFE, 4-tap TX pre-emphasis	CTLE, 11-tap DFE	CTLE, 15-tap DFE	CTLE, 1-tap DFE, 3-tap TX pre-emphasis	**CTLE, 1-tap DFE, 3-tap TX pre-emphasis**
Max. channel loss with BER under 10^{-12}	Not specified	Not specified	Not specified	12dB @11.3Gb/s	26dB @14.025Gb/s	28dB @16.3Gb/s	10.4dB @32.75Gb/s	Not measured	**20dB @12.5Gb/s**
Data rate	0.5Gb/s - 2.5Gb/s	4Gb/s - 10Gb/s	650Mb/s - 8Gb/s	6.5Mb/s - 11.3Gb/s	1.0625Gb/s - 14.025Gb/s	0.5Gb/s - 16.3Gb/s	0.5Gb/s - 32.75Gb/s	50Mb/s - 12.5Gb/s	**50Mb/s - 12.5Gb/s**
Oscillator	Ring VCO	Ring VCO	Ring VCO	4 LC VCOs	2 LC VCOs	4 LC & 4 Ring VCOs	4 LC & 4 Ring VCOs	Ring VCO	**Single LC VCO**
VCO tuning range (GHz)	0.09-1.7 (± 89.9%)	2-7.5 (± 57.9%)	Not specified	5.6-11.5 (± 34.5%)	8-15.5 (± 31.9%)	LC : 8-16.3 (± 34.2%) Ring : 2-6.4 (± 52.4%)	LC : 8-16.375 (± 34.4%) Ring : 2-6.25 (± 51.5%)	6.25-12.5 (± 33.3%)	**10-12.5 (± 11.1%)**
Automatic CDR loop gain control	X	X	X	X	X	X	X	O	**O**
Recovered clock jitter	5.4ps_{rms}	2.2ps_{rms}	9.7ps_{rms}	Not specified (TX RJ 0.0045UI_{rms})	Not specified (TX RJ 0.0045UI_{rms})	Not specified (TX RJ 0.0057UI_{rms})	Not specified (TX RJ 0.0067UI_{rms})	5.8ps_{rms}	**2.6ps_{rms}**
Power (mW)	6.1mW @2Gb/s	22.5 @10Gb/s	88.6 @8Gb/s	415 @11.3Gb/s	410 @14.025Gb/s	278 / lane @16.3Gb/s	785 / lane @28Gb/s	231.77 @12.5Gb/s	**244 @12.5Gb/s**
FoM (mW/Gb/s)	3.05	2.25	11.08	36.73	7.31	17.06	28.04	9.27	**9.76**
Area (mm^2)	0.39	1.63	0.11	4	3.88	4.36	5.98	2.63	**3.03**

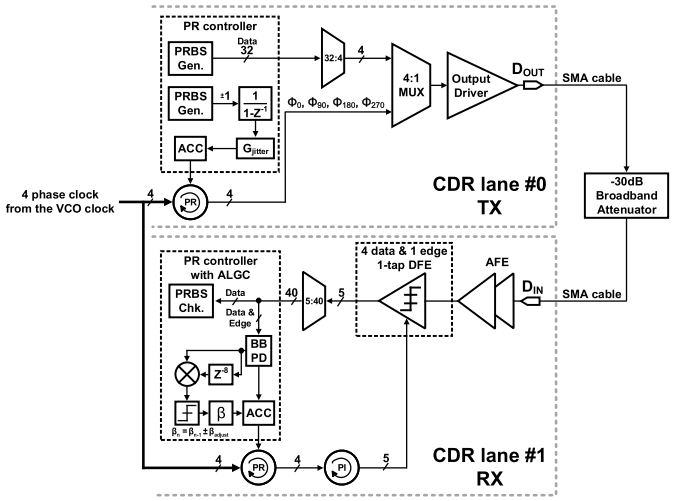

Fig. 16. Measurement setup diagram of the ALGC.

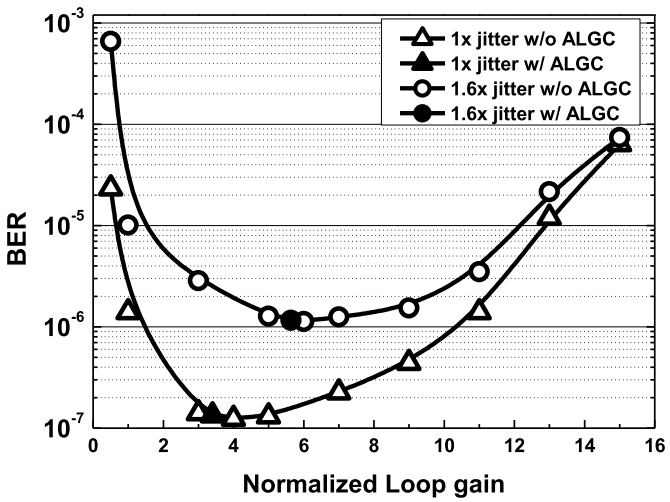

Fig. 17. Measured BER performance of the ALGC with two accumulation jitter conditions.

TABLE II
POWER BREAKDOWN OF THE ALL-RATE CDR IC

RX		
	Block	**Power consumption (mW)**
Front-end	Equalizer	5.9
	Limiting amplifier	19.7
SRCG	Data divider and buffers	7.15
	Clock dividers and BBPD for the JSL	1.12
Clock path	PR, PI and RX clock buffers	9.4
	RX to TX clock buffer	5
Data path	DFE and DEMUX	17.2
	Synthesized blocks (PRCON, ALGC, etc.)	7
Total power consumption of RX per a lane		72.47
TX		
	Block	**Power consumption (mW)**
TX	TX clock buffers	4.88
	3-tap generator and MUXs	4.78
	Pre-driver and output driver	15.6
Total power consumption of TX per a lane		25.26
Clock generator		
	Block	**Power consumption (mW)**
VCO and clock dividers	LC VCO and clock divider **(LC VCO case only)**	7.6
	Ring VCO **(Ring VCO case only)**	5.5
	VCO clock selector and clock divider	9.98
All-rate clock generator (LC VCO case only)	All-rate clock divider	5.45
	Asynchronous calibration loop	4.68
FLL and a lane clock driver	Clock divider and buffers	3.7
	Synthesized block (FLL FD, DLF, etc.)	2
	Clock driver for CDR lanes	5.02
Total expected power consumption of the clock generator (ring VCO case)		26.2
Total power consumption of the clock generator (LC VCO case)		38.43
Bias and miscellaneous blocks		10.11
Total expected power consumption of all-rate CDR IC (2 lanes, ring VCO case)		231.77
Total power consumption of all-rate CDR IC (2 lanes, LC VCO case)		244

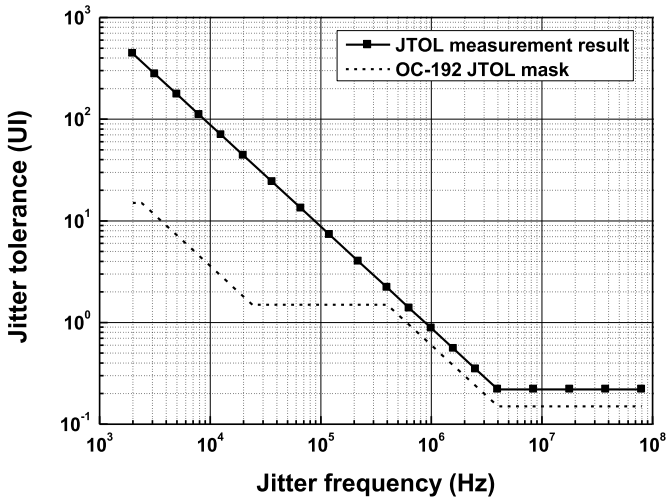

Fig. 18. Measurement result of the jitter tolerance.

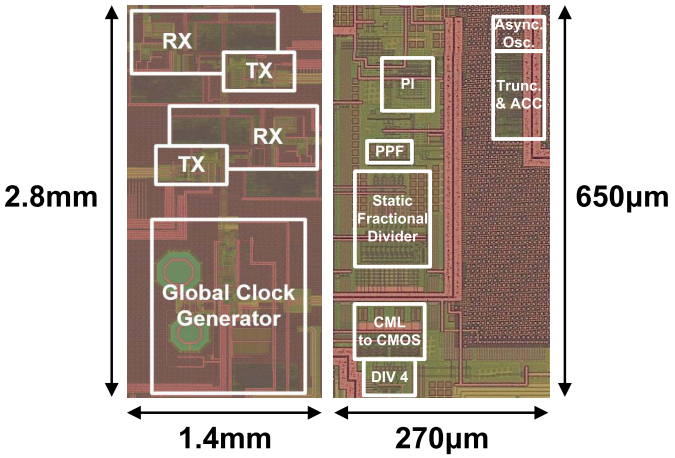

Fig. 19. Microphotographs of the chip and the all-rate CG.

Fig. 15 shows the TX output eye diagram and the amount of random jitter in each fractional division case. The pre-emphasis is used to compensate for the channel loss in an FR4 trace between the TX output and an SMA connector when the data rate is over 10 Gb/s. The maximum TX jitter is 0.0147 UI_{rms} with PRBS31 under 12.5 Gb/s operation.

Fig. 16 illustrates the measurement setup diagram of the ALGC. For this measurement, an internal accumulation jitter generator is implemented in a PRCON for a BIST of the ALGC algorithm. In order to generate accumulation jitter modeled by a random walk process, a PRBS31 is accumulated to control the register of the phase rotator. The step size of the jitter is made controllable by adjusting the multiplication factor prior to the accumulation. The CDR clock signal including the accumulation jitter is used for the TX clock of CDR lane #0. The TX of CDR lane #0 generates a PRBS31 sequence with various amounts of accumulation jitter, and the RX of CDR lane #1 recovers the data while adjusting the loop bandwidth

using the ALGC algorithm. Given that each lane shares the VCO clock signal from the global CG, the accumulation jitter from the VCO does not affect the performance of the ALGC algorithm in this test setup. A 30 dB broadband attenuator was inserted between the TX of CDR lane #0 and the RX of CDR lane #1 to control the SNR of the link and set the initial BER to approximately 10^{-10}. Fig. 17 shows the measured BER with various normalized loop gains under two different accumulation jitter conditions. It is clear that the converged loop gain using the ALGC guarantees the minimal BER under diverse input jitter conditions.

Table I compares the proposed design with previous works. The proposed all-rate transceiver achieves better jitter performance compared to ring VCO-based all-rate designs and occupies less area than conventional multiple *LC* VCO-based all-rate designs. Table II shows the power breakdown of all-rate CDR IC. The power and area overheads for the all-rate functionality are an additional 10 mW and an active area of 0.05 mm^2, respectively, which correspond to the power and area of the all-rate clock dividers. The test chip passes the OC-192 jitter tolerance test with a sufficient margin. The measurement result of the jitter tolerance is shown in Fig. 18. A microphotograph of the test chip is shown in Fig. 19.

VI. Conclusion

A dual-lane DC-to-12.5 Gb/s all-rate referenceless CDR IC with a single *LC* VCO in 90 nm CMOS is presented. A CMOS-based all-rate clock divider with an asynchronous phase calibration scheme generates puncture-less all-rate clock signals using a single *LC* VCO without a phase mismatch or duty cycle distortion. The required minimum frequency tuning range of the *LC* VCO is $\pm 11.1\%$.

An ALGC scheme is implemented to adjust the bandwidth of a CDR automatically for optimal BER performance in the background regardless of the data rate or link conditions. The synthesized ALGC calculates the autocorrelation function of a BBPD output and adjusts the current loop gain to the optimal loop gain by monitoring the sign of the autocorrelation function.

The proposed CDR IC achieves error-free operation from 50 Mb/s to 12.5 Gb/s and consumes 244 mW at 12.5 Gb/s under dual-lane operation. The measured sensitivity is 12 $mV_{pp,diff}$. The proposed IC compensates for 20 dB channel loss at Nyquist by using a CTLE, a one-tap DFE, and a three-tap pre-emphasis filter. The power efficiency of the test chip is 9.76 mW/Gb/s.

References

[1] J. G. Kenney *et al.*, "A 9.95–11.3-Gb/s XFP transceiver in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2901–2910, Dec. 2006.

[2] N. Kocaman *et al.*, "An 8.5–11.5-Gbps SONET transceiver with referenceless frequency acquisition," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1875–1884, Aug. 2013.

[3] S. Huang *et al.*, "An 8.2-to-10.3Gb/s full-rate linear reference-less CDR without frequency detector in 0.18μm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 152–153.

[4] H. Won *et al.*, "A 0.87 W transceiver IC for 100 gigabit Ethernet in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 399–413, Feb. 2015.

[5] U. Singh *et al.*, "A 780 mW 4×28 Gb/s transceiver for 100 GbE gearbox PHY in 40 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Sep. 2014, pp. 40–41.

[6] Broadcom. (Nov. 12, 2010). *BCM56640 Product Brief*. [Online]. Available: http://www.broadcom.com/collateral/pb/56640-PB00-R.pdf

[7] Inphi. *IN112510-LD/LS Product Brief*, accessed on May 20, 2016. [Online]. Available: https://www.inphi.com/products/in112510-ldls.php

[8] R. Inti *et al.*, "A 0.5-to-2.5 Gb/s reference-less half-rate digital CDR with unlimited frequency acquisition range and improved input duty-cycle error tolerance," in *ISSCC Dig. Tech. Papers*, 2011, pp. 438–439.

[9] G. Shu, W.-S. Choi, S. Saxena, T. Anand, A. Elshazly, and P. K. Hanumolu, "A 4-to-10.5Gb/s 2.2mW/Gb/s continuous-rate digital CDR with automatic frequency acquisition in 65nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 150–151.

[10] P. K. Hanumolu, G.-Y. Wei, and U.-K. Moon, "A wide-tracking range clock and data recovery circuit," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 425–439, Feb. 2008.

[11] R.-J. Yang *et al.*, "A 200-Mbps∼2-Gbps continuous-rate clock-and-data-recovery circuit," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 4, pp. 842–847, Apr. 2006.

[12] G. Balamurugan *et al.*, "A scalable 5–15 Gbps, 14–75 mW low-power I/O transceiver in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 1010–1019, Apr. 2008.

[13] H. Song *et al.*, "A 1.0–4.0-Gb/s all-digital CDR with 1.0-ps period resolution DCO and adaptive proportional gain control," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 424–434, Feb. 2011.

[14] K.-Y. K. Chang, D.-S. Kim, D-H. Oh, S. Kim, and D.-K. Jeong, "A 0.4–4-Gb/s CMOS quad transceiver cell using on-chip regulated dual-loop PLLs," *IEEE J. Solid-State Circuits*, vol. 38, no. 5, pp. 747–754, May 2003.

[15] A. P. van der Wel and G. W. den Besten, "A 1.2–6 Gb/s, 4.2 pJ/bit clock & data recovery circuit with high jitter tolerance in 0.14 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1768–1775, Jul. 2012.

[16] S.-K. Lee, Y.-S. Kim, H. Ha, Y. Seo, H.-J. Park, and J.-Y. Sim, "A 650Mb/s-to-8Gb/s referenceless CDR circuit with automatic acquisition of data rate," in *ISSCC Dig. Tech. Papers*, 2009, pp. 184–185.

[17] R.-J. Yang, K.-H. Chao, S.-C. Hwu, C.-K. Liang, and S.-I. Liu, "A 155.52 Mbps–3.125 Gbps continuous-rate clock and data recovery circuit," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1380–1390, Jun. 2006.

[18] D. Dalton *et al.*, "A 12.5-Mb/s to 2.7-Gb/s continuous-rate CDR with automatic frequency acquisition and data-rate readback," in *ISSCC Dig. Tech. Papers*, Dec. 2005, pp. 230–231.

[19] J. Kenney *et al.*, "A 6.5Mb/s to 11.3Gb/s continuous-rate clock and data recovery," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2014, pp. 1–4.

[20] J. Kim *et al.*, "A 16-to-40Gb/s quarter-rate NRZ/PAM4 dual-mode transmitter in 14nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

[21] B. Zhang *et al.*, "A 28Gb/s multi-standard serial-link transceiver for backplane applications in 28nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

[22] F. Zhong *et al.*, "A 1.0625∼14.025 Gb/s multi-media transceiver with full-rate source-series-terminated transmit driver and floating-tap decision-feedback equalizer in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 3126–3139, Dec. 2011.

[23] J. Savoj *et al.*, "Wideband flexible-reach techniques for a 0.5–16.3Gb/s fully-adaptive transceiver in 20nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2014, pp. 1–4.

[24] T. Kawamoto *et al.*, "Multi-standard 185 fs_{rms} 0.3-to-28Gb/s 40dB backplane signal conditioner with adaptive pattern-match 36-tap DFE and data-rate-adjustment PLL in 28nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

[25] P. Upadhyaya *et al.*, "A 0.5-to-32.75Gb/s flexible-reach wireline transceiver in 20nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

[26] J.-H. Yoon, S.-W. Kwon, and H.-M. Bae, "A DC-to-12.5Gb/s 4.88mW/Gb/s all-rate CDR with a single LC VCO in 90nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2015, pp. 1–4.

[27] S.-W. Kwon *et al.*, "An automatic loop gain control algorithm for bang-bang CDRs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 12, pp. 2817–2828, Dec. 2015.

[28] J. Han *et al.*, "Analysis of a frequency acquisition technique with a stochastic reference clock generator," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 59, no. 6, pp. 336–340, Jun. 2012.

[29] J. Y. Lee *et al.*, "A 4×10-Gb/s referenceless-and-masterless phase rotator-based parallel transceiver in 90-nm CMOS," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 6, pp. 2310–2320, Jun. 2016.

[30] J.-Y. Lee and H.-M. Bae, "Application of Kalman gain for minimum mean-squared phase-error bound in bang-bang CDRs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 12, pp. 2825–2834, Dec. 2012.

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