

A 4th-Order Continuous-Time Delta-Sigma Modulator Using 6-bit Double Noise-Shaped Quantizer

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Abstract—This paper presents a continuous-time delta-sigma modulator using a double noise-shaped quantizer (DNSQ), which not only provides 2nd-order noise shaping but also generates a 6-bit quantization in the modulator. The proposed DNSQ efficiently extracts the quantization error in the time domain from a noise-shaped integrating quantizer (NSIQ), and directly applies it to a gated ring oscillator-based quantizer, hence achieving a 2nd order of noise shaping on its own. By incorporating the DNSQ, the modulator can achieve 4th-order noise shaping with only a 2nd-order loop filter. The proposed modulator is fabricated in a 0.13- μm CMOS process with an active area of 0.17 mm². It operates at 640 MHz and achieves a peak SNDR of 80.4 dB in a 15-MHz bandwidth while consuming 11.4 mW from a 1.2-V power supply.

Index Terms—Analog-to-digital conversion (ADC), continuous-time (CT) delta-sigma modulator (DSM), digital integrator, Gm-C based, noise-shaping quantizer.

I. INTRODUCTION

AS DEMANDS for wireless communications with higher data rates continue to rise, the design of analog-to-digital converters (ADCs) faces many challenges to achieve both high resolution and wide bandwidth with minimal power consumption. A suitable ADC architecture that satisfies these demands is the continuous-time (CT) delta-sigma modulator (DSM) with a multi-bit quantizer as DSMs benefits from oversampling and noise shaping to enhance the signal-to-quantization noise ratio (SQNR). CT DSMs are more beneficial in terms of power efficiency and anti-alias filtering compared to their discrete-time (DT) counterparts. Conventionally, flash quantizers have been used to generate multi-bit outputs, but due to the considerable power consumption, alternative ways have been proposed. Among different structures, noise-shaping quantizers have been actively employed as an attractive method to improve the efficiency of the modulator. Compared to conventional flash quantizers, which does not provide noise-shaping property, the noise-shaping quantizer alone offers

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an extra order of noise shaping, thus improving the overall performance of the modulator. Furthermore, common noise-shaping quantizers described below often use single transistor input device, reducing the capacitive loading of the loop filter as well as routing complexity associated with traditional flash ADCs.

Various implementations of noise-shaping quantizers have been proposed to enhance the performance while consuming minimal power. Among them, voltage-controlled oscillator (VCO)-based quantizers [1]–[3] are popularly used due to the advantage of a highly digital implementation, but the VCO's non-linearity limits the overall performance. In contrast, noise-shaped integrating quantizers (NSIQs) [4]–[7] are inherently linear, but suffer from a tradeoff between counting clock speed and resolution. Another noise-shaping quantizer is a gated ring oscillator (GRO)-based quantizer [8]–[10]. By operating as ON and OFF states, the GRO-based quantizer is inherently linear, but it requires a voltage-to-time conversion circuit to be used as an ADC since its input is in the time domain. However, all of these quantizers provide only a 1st order of noise shaping. In order to further improve the performance, a double noise-shaped quantizer (DNSQ) is proposed, which provides a 2nd order of noise shaping by combining the NSIQ and GRO-based quantizers.

This paper describes the details of the analysis and implementation of the DNSQ presented in [11]. In the DNSQ, the quantization error of the NSIQ, which is extracted in the time domain, is directly applied as an input to the GRO-based quantizer so that the DNSQ not only provides 2nd-order noise shaping, but also generates a 6-bit effective quantization. The proposed DNSQ is employed in a CT DSM to improve the efficiency of the modulator. Additionally, the impact of various non-idealities of the DNSQ in the modulator is analyzed and discussed in this paper.

The remainder of this paper is organized as follows. Section II provides a brief overview of the conventional noise-shaping quantizers and discusses properties and limitations of each noise-shaping quantizer. Section III presents the proposed DNSQ using a Gm-C-based NSIQ and a GRO-based quantizer. In Section IV, implementation details of the proposed quantizer in a CT DSM and effects of non-idealities are discussed. Measurement results obtained from the prototype chip are provided in Section V. Finally, Section VI concludes the paper.

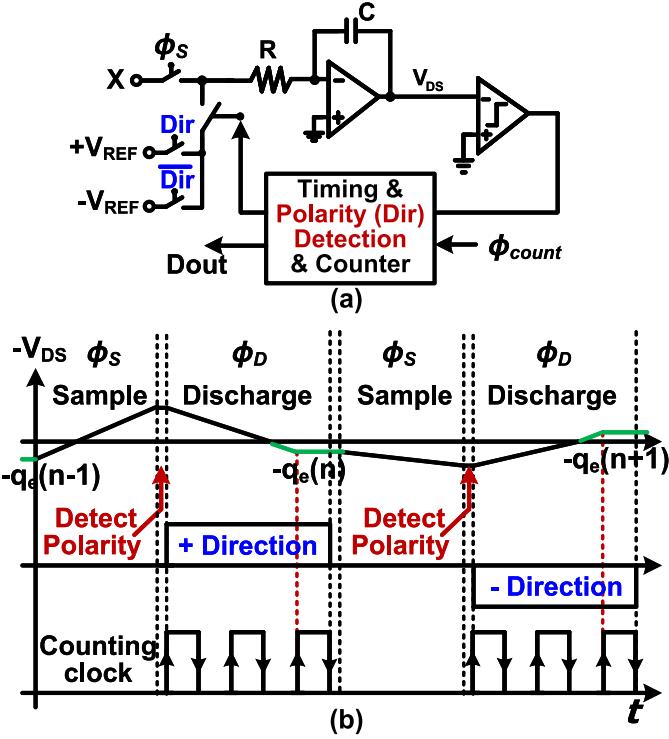


Fig. 1. (a) Simplified NSIQ block diagram with the bi-directional scheme. (b) Timing diagram of the NSIQ with discharging direction.

II. OVERVIEW OF NOISE-SHAPING QUANTIZERS

Noise shaping quantizers such as NSIQs and VCO-based quantizers have become a topic of great interest due to the extra order of noise shaping in DSMs. This section describes the basic operations of noise-shaping quantizers, and reviews their advantages and disadvantages.

A. Noise-Shaped Integrating Quantizer

The NSIQ is essentially a variation of a dual-slope ADC, as illustrated in Fig. 1(a). In a dual-slope ADC, after the input signal is sampled on the integrating capacitor in the sampling phase (ϕ_s), it counts the discharging period with a counting clock until the discharging stops at the zero-crossing during the discharging phase (ϕ_D). Alternatively, in the NSIQ, instead of terminating the discharging at the zero-crossing point, the discharging is continued after the zero-crossing and stopped at the next edge of the counting clock. This way, the quantization error is stored on the capacitor and subtracted from the input in the next sampling phase. In effect, a first order of quantization noise shaping is obtained, $(1 - z^{-1}) \cdot q_e(z)$, where $q_e(z)$ is the quantization error.

As described in [4] and [5], the bi-directional scheme enables the discharging in NSIQ to occur in both the positive and negative directions using different polarities of the reference voltage. As shown in Fig. 1(b), the discharging is determined to be in either the positive or negative direction depending on the polarity of the input at the beginning of the discharging. The polarity detection halves the counting clock speed requirement since the MSB (polarity) is resolved first. Also, this polarity detection plays an important role in the

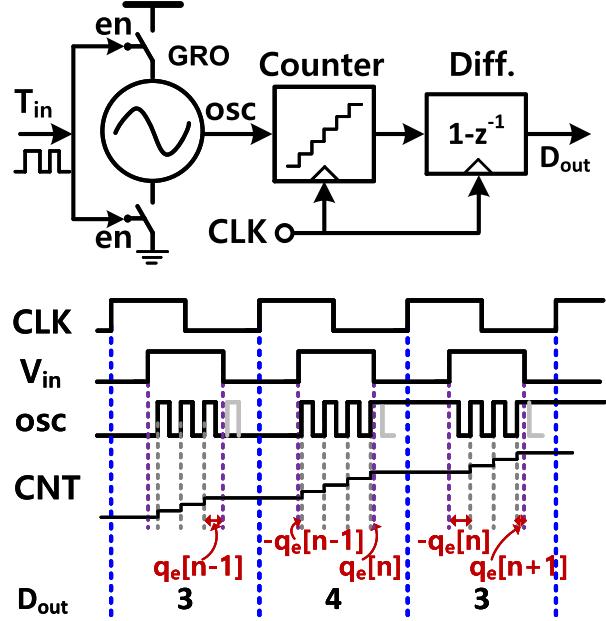


Fig. 2. Conceptual block diagram of a GRO-based quantizer and timing diagram for 1st order of noise shaping.

proposed quantizer, which will be elaborated in more detail in Section III. In addition to a 1st order of noise shaping, the NSIQ provides the quantization error in both analog and time domains so that it can be easily extracted to obtain an additional order of noise shaping. However, the NSIQ requires a high-speed counting clock ($2^N \cdot F_s$, where N and F_s are the number of quantization levels, and the frequency of the sampling clock, respectively) because the number of quantization levels is dependent on the counting clock speed.

B. GRO-Based Quantizer

Similar to a VCO-based quantizer, the GRO-based quantizer counts the oscillator output and generates a digital output with a differentiator, as illustrated in Fig. 2. The main deviation from the VCO-based quantizer is that the GRO takes a time domain input instead of a voltage input. Conceptually, the GRO can be realized by adding switches in series with a conventional ring oscillator to the power rails. Thus, it oscillates only when the switches are closed, and the oscillation phase is suspended in the OFF-state when the switches are open. Thus, the GRO starts with the previous quantization error at the beginning of every clock cycle, and the quantization error occurred in the current cycle is transferred to the next clock cycle. This way, the GRO-based quantizer provides 1st-order noise shaping.

In addition to the advantages of a VCO-based quantizer [2], [3], the GRO-based quantizer has an inherently linear behavior by operating as ON and OFF states. Once the GRO is ON, it oscillates at a certain frequency independent of the input amplitude, whereas the oscillation frequency of the VCO is dependent on the input amplitude. However, a voltage-to-time conversion circuit is required to employ it in ADCs. In this paper, the voltage-to-time conversion is inherently performed in the NSIQ which is explained in detail

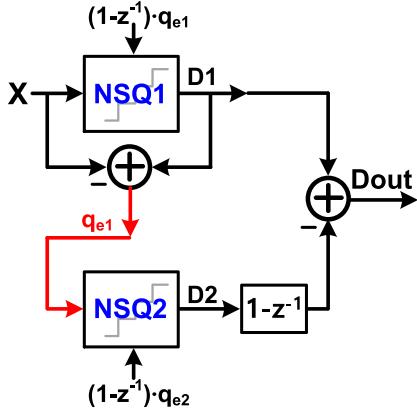


Fig. 3. Conceptual block diagram of the DNSQ.

in the following section. Other design considerations of the GRO-based quantizer in practice include the dead-zone behavior [9] and leakage [12] during the OFF-state caused by circuit non-idealities.

III. PROPOSED DOUBLE NOISE-SHAPED QUANTIZER

In this paper, we propose a DNSQ effectively benefiting from both a NSIQ and a GRO-based quantizer. The operation principle and properties of the DNSQ as well as the necessary design considerations are discussed in this section.

A. Operation Principle

Fig. 3 illustrates the conceptual block diagram of the proposed DNSQ. The DNSQ consists of two noise-shaping quantizers, NSQ1 and NSQ2. The first noise-shaping quantizer (NSQ1) converts the analog input signal (X) into the digital MSB output with first-order noise-shaped quantization error (q_{e1})

$$D1 = X + (1 - z^{-1}) \cdot q_{e1}. \quad (1)$$

Meanwhile q_{e1} is extracted and fed to the second noise-shaping quantizer (NSQ2) so that the digital LSB output from NSQ2 is given as

$$D2 = q_{e1} + (1 - z^{-1}) \cdot q_{e2}. \quad (2)$$

By subtracting (2) from (1) through the digital filter $(1 - z^{-1})$ in the digital domain, q_{e1} is ideally cancelled out and the final output contains only a 2nd-order shaped quantization error, q_{e2} from NSQ2

$$Dout = X - (1 - z^{-1})^2 \cdot q_{e2}. \quad (3)$$

The main benefit of this architecture is to simultaneously provide both quantization and noise shaping from both NSQ1 and NSQ2.

Generally, in multi-step quantizer such as this one, the main design challenge is how to extract the quantization error, q_{e1} from NSQ1 effectively. The conventional way of extracting the quantization error is performed in the analog domain by subtracting the input signal X of the first quantizer from its output, which requires a DAC and a residue (or sample-and-hold) amplifier for the subtraction, or a

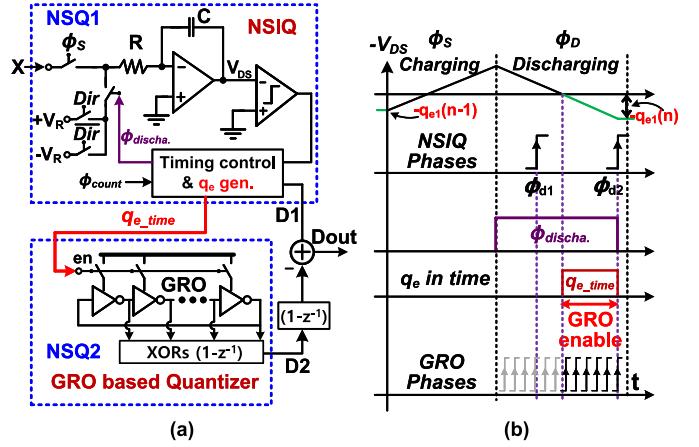


Fig. 4. (a) Proposed DNSQ. (b) Timing diagram of the DNSQ.

multiplying DAC [13]–[15], which adds circuit complexity and requires additional power consumption. Moreover, the inter-stage gain mismatch and linearity of the DAC are critical limitations in achieving the desired performance. Although the successive approximation-register-based quantizer with the noise-coupling technique presented in [16] provides an additional 2nd order of noise shaping without an extra DAC to extract the quantization error, it requires additional buffers with extra passive components to implement the noise-coupling scheme. In the proposed quantizer, the quantization error is inherently extracted in the time domain without the necessity of using any DAC or amplifier as explained in the following section.

B. NSIQ and GRO-Based Quantizer

In the proposed DNSQ, the NSIQ operates as the first noise-shaping quantizer, as shown in Fig. 4(a). As mentioned in Section II, the NSIQ provides quantization error in both the analog and time domains. Utilizing this advantage, the easily extracted quantization error in the time domain q_{e_time} is directly fed to a GRO-based quantizer, which functions as the second noise-shaping quantizer. As described conceptually in the previous section, the quantization error from the NSIQ is cancelled out in the digital domain, and the final output will have only the 2nd-order noise-shaped quantization error from the GRO-based quantizer. This enables the proposed quantizer to act as a 2nd-order noise-shaping quantizer.

The quantization error from the NSIQ is the time duration from the zero-crossing point to the next counting clock edge after the zero-crossing point, as illustrated in Fig. 4(b). The zero-crossing point can be easily detected with a comparator. Hence, no additional DAC or amplifier is required in the proposed quantizer to extract the quantization error. Moreover, the GRO-based quantizer operates in a delay-free fashion as the extraction of the quantization error starts immediately after the zero-crossing point, and at the same time the GRO starts shifting its phases. In other words, as soon as the NSIQ begins generating quantization error, the GRO-based quantizer processes the quantization error in a delay-free fashion. Thus, it eliminates the requirement of any sample-and-hold circuitry to create an additional delay in the modulator.

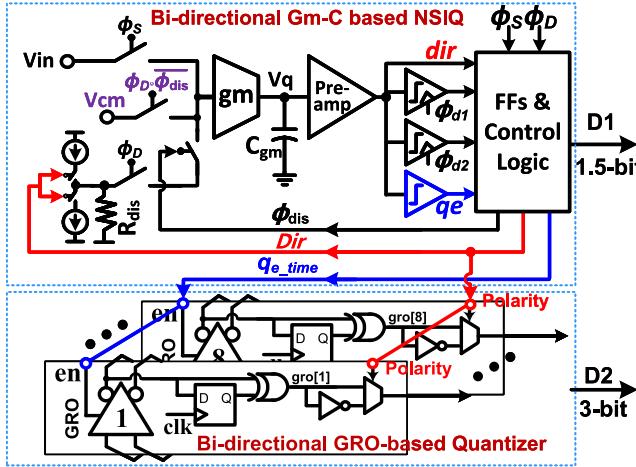


Fig. 5. Simplified schematic of the bi-directional DNSQ including the Gm-C-based NSIQ and GRO-based quantizer.

The proposed DNSQ may be considered as a counterpart of multi-stage noise-shaping (MASH) DSMs [17] due to the multi-step quantization and only the last stage quantization error appearing at the output with multi-order noise shaping. However, the DNSQ has several advantages over the MASH DSMs. In conventional MASH DSMs, each stage requires a loop filter and a quantizer with feedback DACs. Extra hardware for extraction of the quantization error such as a DAC and amplifier is required. On the other hand, each stage in the proposed DNSQ is a quantizer itself, providing noise shaping without a loop filter. In addition, only a single comparator is required to extract the quantization error. These features allow for an easy integration of the DNSQ in DSM architectures to achieve high order of noise-shaping and aggressive quantization with minimal design complexity. Although the DNSQ is an attractive topology for a stand-alone oversampling ADC due to the SQNR provided by the 2nd-order noise shaping, it is prone to the leakage of the quantization error of NSQ1, similar to MASH modulators. This leakage can degrade the cancellation of qe_1 at the final digital output and cause distortions. In this paper, the DNSQ is employed in a modulator so that the leakage of NSQ1 and any other non-idealities from the DNSQ are processed and suppressed by the loop filter, relaxing the circuit requirements of the DNSQ. More detailed analysis of this leakage is provided later in this paper.

C. Bi-Directional Scheme in the Double Noise-Shaped Quantizer

The Gm-C-based NSIQ [4] with a bi-directional scheme is utilized for the proposed DNSQ, as shown in Fig. 5 (single-ended shown for simplicity). Compared to an active-RC integrator, the Gm-C integrator is chosen in this design because of its power efficiency. During the sampling phase (ϕ_s), the input signal is integrated on the integrating capacitor (C_{gm}) through the gm . At the beginning of the discharging phase (ϕ_d), the polarity of the voltage on C_{gm} is detected first, and a discharging voltage from a combination of a current source and a resistor is applied to the gm to

discharge the capacitor in the desired direction while the control logic generates the discharging enable signal (ϕ_{dis}). At the first clock edge after the zero-crossing, the control logic terminates ϕ_{dis} to stop discharging by disconnecting the discharging voltage from the gm . Therefore, the quantization error is stored on C_{gm} . To preserve this quantization error, the input of the gm is shorted to common-mode voltage (V_{cm} in Fig. 5) after discharging until the next sampling phase. Together with the bi-directional discharging scheme, the Gm-C integrator, and the pre-amplifier with only two dynamic latches, three quantization levels (1.5 bit) are obtained with a 1st order of noise shaping. Essentially, the Gm-C-based NSIQ is a 1st-order DSM and can be otherwise implemented using a Gm-C integrator followed by a flash quantizer. However, besides the benefits of NSIQ such as its availability of quantization error in both time and analog domains, NSIQ can be realized by a single comparator without multi-bit DAC while the DSM with a Gm-C integrator and flash requires multiple comparators (which are power hungry blocks) and multi-bit DAC with large capacitive loading.

Moreover, since only the zero-crossing point is of concern in the NSIQ, the gm of the NSIQ can be designed to be small (which saves power consumption) compared to the gm of the conventional DSM with a multi-bit flash quantizer where large gm (for large swing) is required. Also, the variation of the gm value in the NSIQ does not affect the desired noise transfer function (NTF) because the capacitor is charged (integrated) and discharged with the same gm , whereas that in conventional DSM directly causes NTF variation.

With the bi-directional scheme described in [4] and [5], the number of counting clock phases and related hardware of the NSIQ can be reduced by half hence minimizing control logic and power consumption in the proposed DNSQ. In contrast to a conventional NSIQ, the half LSB adjustment [5] is not utilized in the DNSQ since the quantization error from NSIQ is ideally cancelled out at the output of the DNSQ and only relatively small 2nd-order shaped quantization error from the GRO-based quantizer remains.

As a result of removing half LSB compensation, the quantization error of the NSIQ ranges either from 0 to LSB or from 0 to $-LSB$, depending on the detected polarity of the input signal, as shown in Fig. 6(a). However, the quantization error in the time domain always takes a positive form. This means the quantization error fed from the NSIQ to GRO can only take a positive form, regardless of the polarity of the quantization error stored on the NSIQ, and hence creates a severe signal/polarity dependent error. To address this issue, the output of the pseudodifferential GRO-based quantizer is swapped based on the NSIQ discharging polarity to effectively present a negative quantization error, as illustrated in Fig. 6(b). In this fashion, the negative quantization error from the NSIQ can be represented with the polarity detection at the output of the GRO-based quantizer. As a result, the bi-directional scheme with the polarity detection in the proposed DNSQ not only enables the reduction of the number of counting clock phases, hardware, and power consumption, but also properly represents the negative quantization errors in the time domain. Since the discharging polarity is available at the beginning of

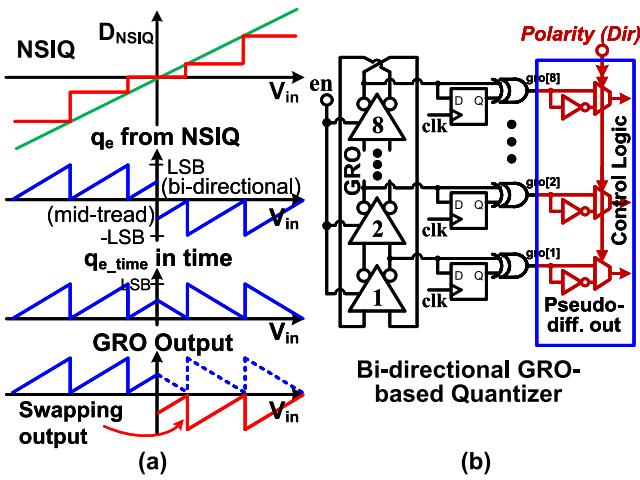


Fig. 6. (a) Quantization error of the bi-directional NSIQ in voltage and time domains, and output of GRO-based quantizer. (b) Simplified schematic of the bi-directional GRO-based quantizer.

the discharging phase, this action does not impose any critical timing path.

The zero-crossing detection must be faster than half of the time domain LSB of the NSIQ and demands large power [5]. To reduce the power consumption of the zero-crossing detector, the polarity dependent offset injection in [5] is used in this design.

D. Minimization of Gain Mismatch Between NSIQ and GRO-Based Quantizer

Although the quantization error can be easily extracted in the time domain with minimal hardware, the gain mismatch between the NSIQ and the GRO-based quantizer needs to be carefully considered [18], [19]. To minimize the gain mismatch, a delay locked loop (DLL) replicating the GRO delay cells is employed. All the output phases of the GRO should be equally spaced in the time duration corresponding to 1LSB of the NSIQ, which is the time difference between the counting clock edges, as illustrated in Fig. 7. In order to equally spread the eight phases of the 3-bit GRO-based quantizer between the counting clock edges, ϕ_{d1} and ϕ_{d2} are generated from the DLL with 12 delay cells, noting that the first quantization step in the bi-directional and mid-tread scheme should be equal to a half LSB. If the delay cells of the DLL and the GRO have the same propagation delay, the gain mismatch between the NSIQ and the GRO will be minimized. Thus, an identical delay cell shown in Fig. 8(a) is utilized to match the propagation delays of both the DLL and the GRO biased by the same control voltage (V_{ctr}), as shown in Fig. 8(b). Such approach alleviates the gain mismatch between the NSIQ and GRO-based quantizer over PVT variations.

It is worth noting that the NSIQ is intentionally designed to have only 1.5-bit quantization levels, although 12 phases of the DLL are available for the counting clock edges. Resolving only 1.5 bits in the NSIQ reduces the design burden of the NSIQ while more quantization levels are effectively obtained from the second quantizer with an additional order of noise

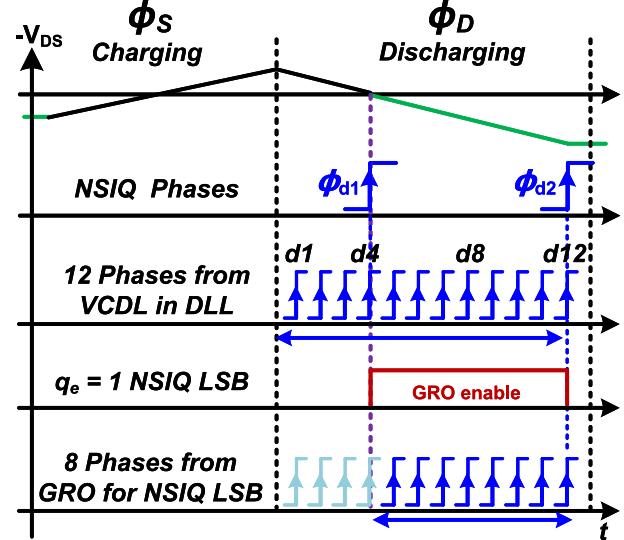


Fig. 7. Timing diagram including phases of the DLL and GRO.

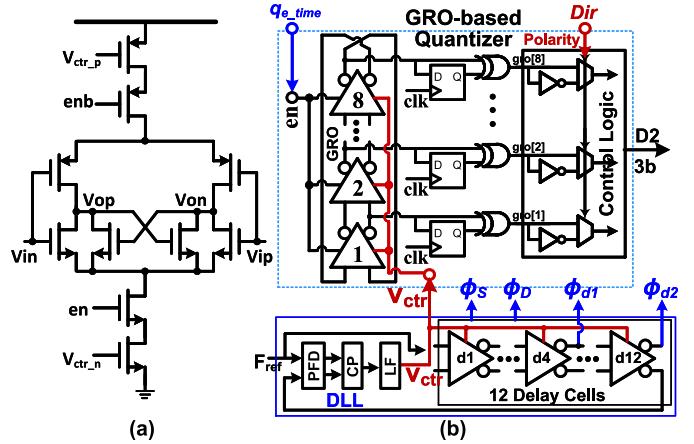


Fig. 8. (a) Delay cell used for both DLL and GRO. (b) Simplified block diagram for the minimization of gain mismatch between GRO and NSIQ using a DLL.

shaping. In other words, instead of adding 12 dynamic latches and complex digital logic with additional power consumption into the NSIQ, obtaining 3 bits from the GRO-based quantizer results in a more efficient quantizer with 2nd-order noise shaping.

E. Minimum Pulse Injection in GRO-Based Quantizer

Another design consideration is the case when the pulsewidth of the GRO input is too short. In the NSIQ, the quantization error in the time domain is generated from the zero-crossing point, detected by the comparator [comp. in Fig. 9(a)] to the end of discharging period (ϕ_{dis}). It is critical that the generated pulsewidth provides enough time for the GRO to operate properly. However, if the zero-crossing occurs near to the clock edges or the zero-crossing and the clock edges are aligned together, the GRO input will be too short for proper operation. In the worst case, the pulse will look like a glitch, as shown in Fig. 9(b). Such condition can create a dead-zone or meta-stable behavior in the GRO. The corrupted GRO output due to the dead-zone or meta-stability

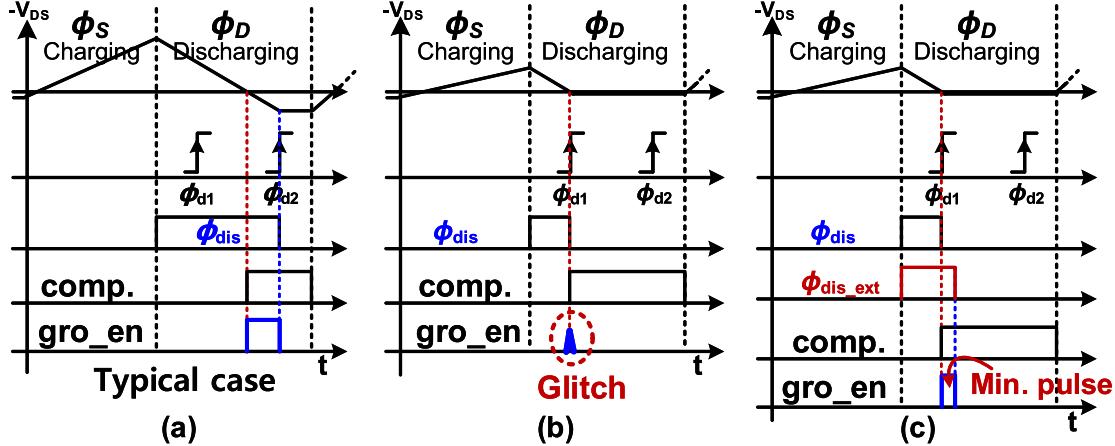


Fig. 9. (a) Typical case of the GRO input having enough time to operate properly. (b) Case of too short pulsewidth or glitch occurred for the GRO input. (c) Case of minimum pulsewidth generated for the GRO input.

will not only degrade the performance of the modulator, but can possibly cause instability in the modulator.

In order to avoid any dead-zone or meta-stable behavior in the GRO, a minimum pulse injection for the input of the GRO is performed. The key idea is to generate a pulse (ϕ_{dis_ext}) which is an extended version of the discharging period (ϕ_{dis}), as illustrated in Fig. 9(c). With the minimum pulse injection, the dead-zone or meta-stable behavior will be avoided. This effectively acts as an added offset to the q_{e1} pulse, and while the added offset does not directly degrade SNDR, it will eat up the dynamic range of the GRO quantizer, if the offset is large. More importantly, since the q_{e1} pulse ideally varies from 0 to a full LSB, adding an offset might push this pulse to go over full LSB in time domain, therefore shifting all the phases by π resulting in a complete cycle of the GRO. To eliminate this issue, it is crucial to make sure the added pulse is long enough to eliminate the glitch like behavior and short enough not to push the maximum quantization error larger than $LSB_{NSIQ} + LSB_{GRO}$ (in time domain). In this design, the added pulse was less than $LSB_{GRO}/2$ to ensure the above criteria are satisfied (two inverter delays).

IV. PROPOSED CONTINUOUS-TIME DELTA-SIGMA MODULATOR

In this section, the architecture and implementation of the CT DSM using the proposed DNSQ are described. Compared to conventional 4th-order CT DSMs, where a conventional flash quantizer is one of the most power hungry blocks [20], [21] and it may be rather difficult to implement a single-step power efficient quantizer, the proposed DNSQ needs only a 2nd-order loop filter to achieve 4th-order noise shaping, and achieves 6-bit quantization levels with minimal added hardware and power consumption. Also, the design considerations and effects of the proposed quantizer's non-idealities in the modulator are analyzed and discussed in more detail.

A. Proposed Modulator Architecture

Generally, the requirement of any quantizer at the backend of the loop filter in DSMs is suppressed by the in-band

gain of the loop filter. However, the input voltage to the quantizer, which is the sum of the input signal and the filtered quantization error can be relatively large and, depending on the NTF, can have a large signal component. To alleviate the quantizer from processing large input signals, we propose a DSM loop which employs the DNSQ followed by a digital integrator, as illustrated in Fig. 10(a). In addition, as described in [4], a modulator with the combination of an NSIQ and a digital integrator benefits from several advantages, such as the effectively increased number of output bits and relaxed linearity requirement of the quantizer, given that digital integrator reduces the signal amplitude at the input of the quantizer. Although the NSIQ even when implemented using nonlinear Gm-C can achieve relatively good linearity due to dual-slope operation (the non-linearity in charging and discharging follow the same), employing the digital integrator at the back end reduces the number of counting clock edges to mitigate speed/resolution tradeoff [4]. As a side advantage, the linearity requirement of Gm-C can be even further reduced since the signal component at the output of Gm-C will be suppressed.

The loop shown in Fig. 10(a) can be further simplified. That is, the noise-cancelling filter ($1 - z^{-1}$) at the output of the GRO can be cancelled out by the digital integrator and simply be replaced with a delay, as illustrated in Fig. 10(b). This way, redundant digital blocks can be removed without changing the loop transfer function. In the realized architecture, the digital addition at the output is performed outside of the loop, as shown in Fig. 10(c). Thus, the critical timing delay in the feedback path caused by the digital addition can be eliminated and the global DAC (DAC_1) can be relaxed to two 3-bit DACs [22]. Although adding digital outputs of the NSIQ and GRO in digital domain would result in a single global DAC [structure of Fig. 10(b)] and hence no gain mismatch as opposed to two separate DACs (the implemented structure), the practical implementation is not straightforward. First, the output of the GRO automatically operates as DWA, therefore the output codes are shuffled making them difficult to add directly in the thermometer fashion. Second, the allowable time for this summation is limited, and third, it will increase

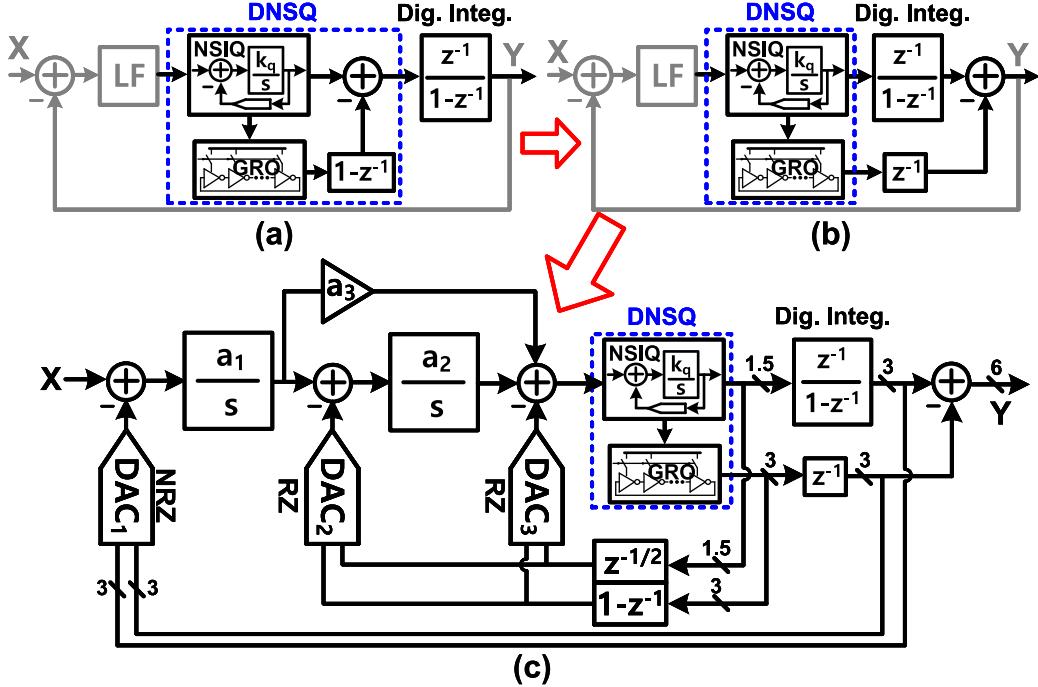


Fig. 10. Simplified block diagrams of the proposed CT DSM architecture using the DNSQ. (a) Initial DSM architecture with the DNSQ and a digital integrator at back-end. (b) Differentiation ($1-z^{-1}$) is canceled out with the digital integrator. (c) Finally realized CT DSM architecture.

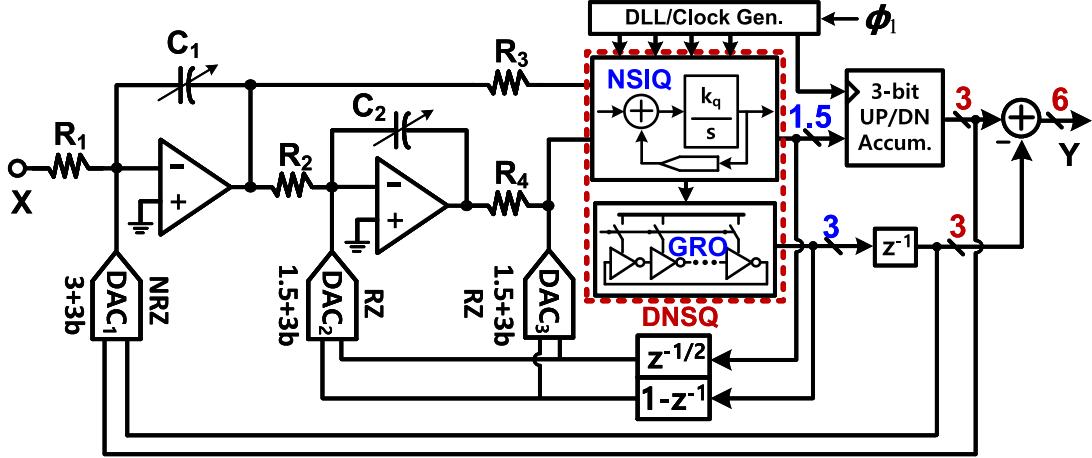


Fig. 11. Simplified schematic of the implemented CT DSM using the DNSQ.

the routing complexity. In this design, a 2nd-order CT loop filter is employed and the digital integrator effectively increases the 1.5-bit quantization levels of the NSIQ to 3-bit, resulting in a 6-bit output with 3 bits from the GRO-based quantizer. The internal DACs (DAC₂ and DAC₃) are driven directly by the 1.5-bit NSIQ and 3-bit GRO-based quantizer instead of the 6-bit final output, reducing the size of the internal DACs.

The output of the proposed CT DSM with the DNSQ shown in Fig. 10 is calculated as

$$Y = X \cdot STF - q_{e2} \cdot NTF_{LF} \cdot NTF_{NSIQ} \cdot NTF_{GRO} \quad (4)$$

where STF denotes the signal transfer function, and NTF_{LF}, NTF_{NSIQ}, and NTF_{GRO} denote the noise transfer functions provided by the loop filter, the NSIQ, and the GRO-based

quantizer, respectively

$$\begin{aligned} NTF_{LF} &= \frac{(1-z^{-1})^2}{1 - 1.225z^{-1} + 0.4415z^{-2}} \\ NTF_{NSIQ} &= NTF_{GRO} = (1-z^{-1}). \end{aligned}$$

The out of band gain (OBG) of NTF_{LF} is 1.5 and the OBGs of NTF_{NSIQ} and NTF_{GRO} are 2. Since the DNSQ has an overall 6-bit quantization, the OBG of NTF_{LF} can be larger for higher SQNR. However, higher OBG of NTF_{LF} inevitably requires more number of levels in the NSIQ (which has only 1.5 level in this design) to avoid overloading. Furthermore, because NTF_{NSIQ} and NTF_{GRO} provide large OBG of 4 together, NTF_{LF} is designed to have lower OBG in order to avoid NSIQ overloading and achieve larger dynamic range. Including the

finite opamp gain and parasitic capacitances, the SQNR of the design is about 95 dB.

B. Modulator Implementation

Fig. 11 illustrates the simplified schematic of the proposed modulator employing a 2nd-order CT loop filter with the DNSQ and a back-end digital integrator. A single-ended implementation is shown for simplicity. The 2nd-order loop filter is realized using active-*RC* integrators which provide more linearity compared to a Gm-C integrator and a clean virtual ground to ease the feedback DAC design. Both zeros of the DNSQ (from NSIQ and GRO) are placed at dc. Therefore, for lower OSR applications, it would be beneficial to spread the remaining zeros of the loop filter. Three-stage opamps with feedforward compensation [4] are chosen to minimize the loop delay caused by the integrator [23]. An up/down accumulator with a barrel-shift algorithm is employed for the digital integrator [4].

All the feedback DACs are cascode current steering types. Non-return-to-zero DAC pulse is implemented for the global DAC (DAC_1), which consists of two 3-bit DACs with equally sized units. Fig. 12 shows the effect of the global DAC non-linearities: gain mismatch and unit element mismatch. Fig. 12(a) shows SNDR versus the DAC gain mismatch and Fig. 12(b) shows the fast Fourier transform (FFT) spectrum of the proposed modulator with 0.1% DAC gain mismatch. As shown, the quantization noise of the NSIQ is not perfectly cancelled due to the DAC gain mismatch and directly appears at the output without noise shaping, creating harmonics and degrading SNDR. Fig. 12(c) shows the effect of unit element mismatch of each DAC. The DAC associated with the NSIQ (DAC_1_NSIQ) requires more stringent linearity requirement since it contains the input signal. The DAC associated with the GRO (DAC_1_GRO) has relaxed linearity requirement since it processes only the quantization error and has inherent dynamic element matching. Although the DAC_1_GRO does not require high linearity, a 14-bit linear DAC [4] is used for both DAC_1_NSIQ and DAC_1_GRO to match the gain between the DACs. Also, timing calibration scheme used in [4] is employed in this design to reduce ISI effect.

The internal DACs (DAC_2 and DAC_3) are implemented using a return-to-zero scheme, and driven by the 4.5-bit DNSQ output. The differentiation ($1 - z^{-1}$) in the internal feedback path of the GRO-based quantizer output is performed with two separate DACs [24]. This avoids the need for extra logic in the digital domain which can increase power consumption and alter the loop delay.

C. Effect of Leakage From NSIQ

In an ideal case, the quantization noise of the NSIQ is perfectly cancelled as can be seen in (4). However, in real situations, the quantization errors of both NSIQ and GRO are not completely preserved due to leakage. In this section, the leakage of the NSIQ and GRO and their effect on the overall performance are discussed.

We categorize the sources of the NSIQ leakage to two components: output swing of the gm and hold time

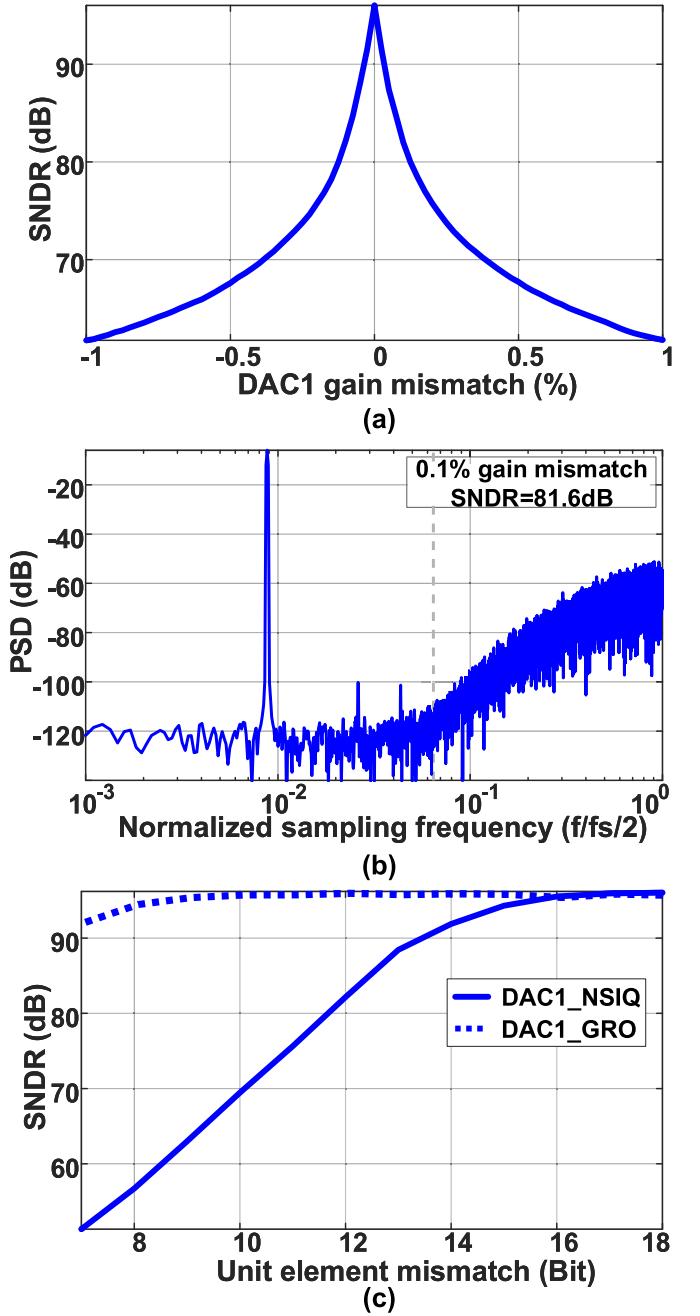


Fig. 12. Global DAC mismatch. (a) SNDR versus DAC gain mismatch. (b) Spectrum with 0.1% DAC gain mismatch. (c) SNDR versus unit element mismatch.

(time duration that holds the quantization error). First, leakage due to the output swing is discussed. As described in Section III-C, the NSIQ should hold the previous quantization error on the integrating capacitor. This is performed by shorting the differential inputs of the gm to the common-mode voltage. Since the differential input voltage is zero the differential output current is zero. However, because of the finite output resistance (R_{out}) of the gm, the V_{DS} will create additional current, which charge or discharge the integrating capacitor. This is illustrated in more detail in Fig. 13 with a five-transistor gm as an example, as shown in Fig. 13(a), for simplicity. It is assumed that the output common mode is set

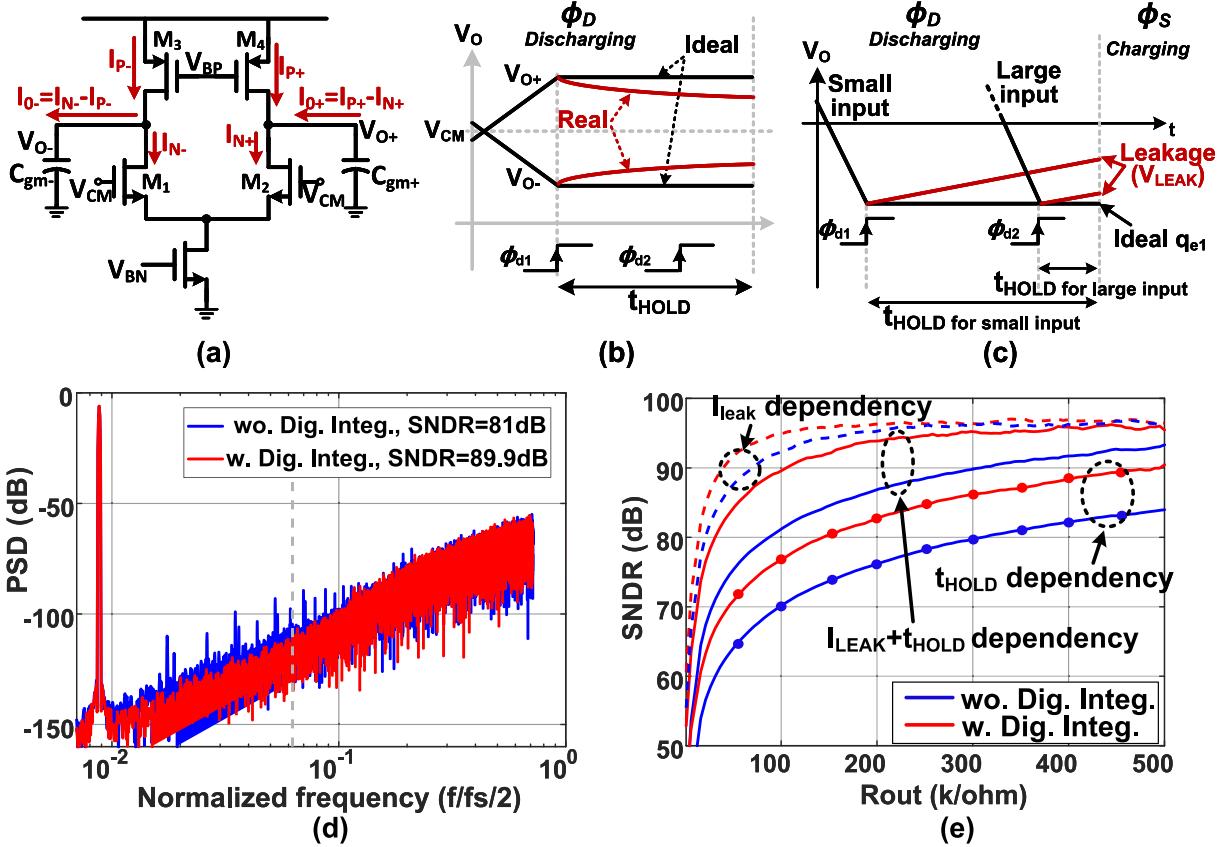


Fig. 13. Behavioral diagram of leakages of the NSIQ. (a) Source of leakage. (b) Swing dependent leakage. (c) NSIQ digital output dependent leakage. (d) FFT results when $R_{out} = 100 \text{ k}\Omega$. (e) SNDR versus output resistance.

such that V_{DS} of M₁-M₄ are equal for the sake of argument. When the discharging stops [rising edge of ϕ_{d1} in Fig. 13(b)], the differential inputs of the gm are connected to V_{CM} to generate zero differential current. However, at this moment assuming $V_{O+} > V_{O-}$, I_{O+} will discharge C_{gm+} because $V_{DS2} > V_{DS4}$ and I_{O-} will charge C_{gm-} because $V_{DS3} > V_{DS1}$. Therefore, the leakage is dependent on the output swing of the gm. Generally, a nonlinear leakage due to the output swing causes harmonic distortion because the swing of the gm in the stand-alone NSIQ is signal dependent. However, the swing of the interest is not the swing of the entire clock phase but only of when the discharging stops, in other words, the quantization error. Thus, the leakage due to the swing will mainly affect the noise floor rather than introducing harmonic distortion. The leakage current during charging and discharging will affect the signal component and create harmonic distortion in a conventional design. However, in this design, the NSIQ does not process large signal component because of the use of the digital integrator, the harmonic distortion created from the leakage during sampling/discharging will be very small.

Another source of the leakage is the code dependent hold time (t_{HOLD}) which is defined by the time difference of when the discharging stop time and the rising edge of the next sampling phase. Two situations are illustrated in Fig. 13(c) with small and large inputs. The discharging stops at either ϕ_{d1} or ϕ_{d2} depending on the input amplitude. Assuming

for simplicity that there is linear leakage current after the discharging stops, the voltage loss (V_{LEAK}) due to the leakage current is directly dependent on the hold time (t_{HOLD}), as seen in Fig. 13(c).

From the above discussions, the digital output of the stand-alone NSIQ including the leakage can be represented as

$$D1 = X + (1 - z^{-1}) \cdot q_{e1} + V_{LEAK} \quad (5)$$

where

$$V_{LEAK} = I_{LEAK}(z^{-1}q_{e1}) \cdot t_{HOLD}(z^{-1}D1) \quad (6)$$

which implies that the leakage is a function of the quantization error and the digital output of the NSIQ. Due to the output code dependence on t_{HOLD} , this leakage will mainly introduce harmonics, if the input to the quantizer has a large signal component. However, in the proposed structure, the NSIQ mostly processes the filtered quantization error due to the use of the back-end digital integrator [4]. Therefore, the harmonic distortion from the leakage will be mostly randomized and only result in increasing the noise floor. The 2nd-order loop filter further suppresses the leakage error as well.

A comparison of the proposed DNSQ modulator with and without the digital back-end integrator is simulated in Simulink to compare the effect of the NSIQ leakage. Fig. 13(d) shows the FFT results of the two structures with the NSIQ leakage in (6). It shows that without the digital back-end integrator, the DNSQ modulator has harmonic distortions but

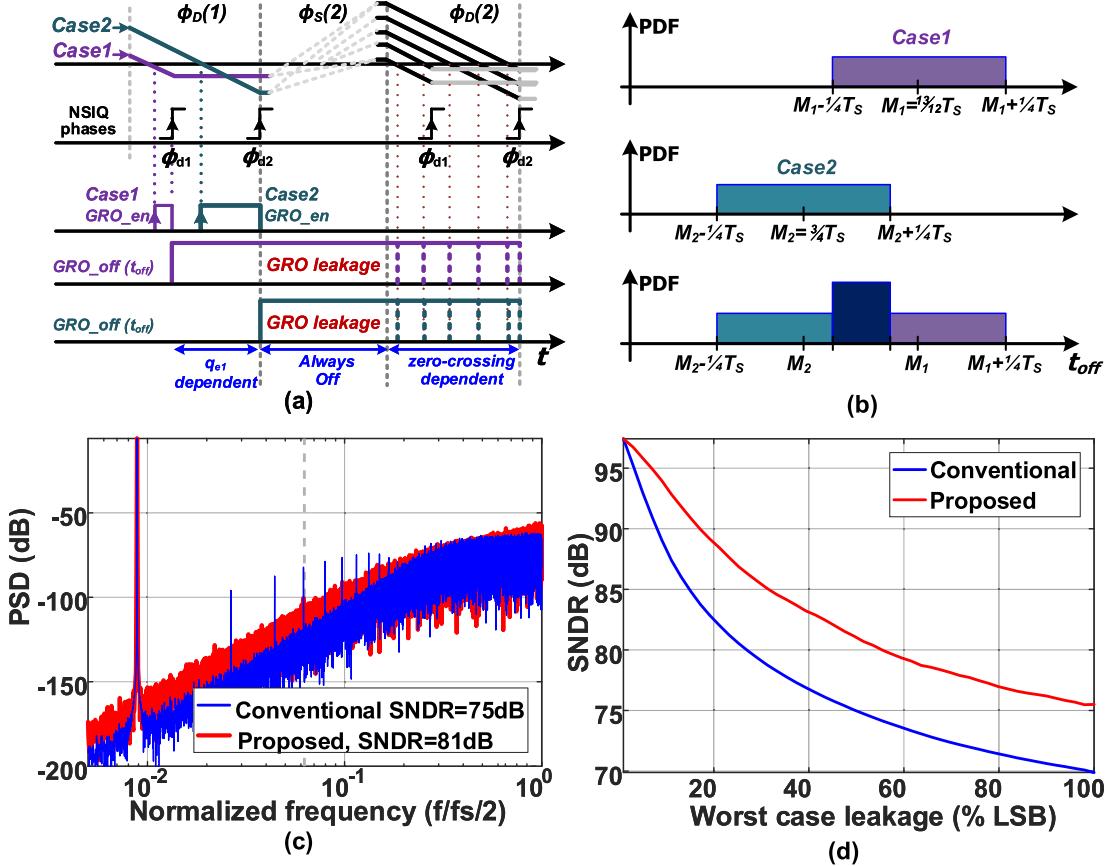


Fig. 14. Behavioral diagram of GRO leakage. (a) Timing diagram. (b) PDF of GRO-OFF time (t_{off}). (c) Effect of GRO leakage with worst case leakage of 50% LSB. (d) SNDR versus worst case leakage.

is harmonic free with the addition of the digital back-end integrator as discussed above. Fig. 13(e) shows the output resistance requirement of the gm. Based on (6), three cases are simulated: I_{LEAK} dependence (dashed line), t_{HOLD} dependence (dotted line), and with both I_{LEAK} and t_{HOLD} dependence (straight line). As seen in Fig. 13(e), t_{HOLD} dependent leakage causes the most significant performance drop due to added harmonic distortions, while I_{LEAK} dependent leakage itself does not deteriorate the performance to such a degree. When both effects are simulated together, the leakage due to t_{HOLD} is randomized by the I_{LEAK} dependent leakage. The output resistance requirement of the gm with the digital back-end integrator is much less than that without the digital back-end integrator. In this design, a telescopic OTA, of which output resistance is roughly 50 k Ω , and 400-fF load capacitor (slightly overdesigned) is used to minimize the leakage.

D. Effect of Leakage From GRO-Based Quantizer

In the proposed DNSQ, the GRO is enabled for only a small amount of time (q_{e1} of the NSIQ) and stays off for the remainder of the clock cycle. Therefore, the nonlinear leakage of the GRO is an important factor to analyze even though the GRO is placed at the back end of the modulator. A timing diagram is provided in Fig. 14(a) to describe this in more detail considering two different cases. In Fig. 14(a), ϕ_{d1} is placed

at 1/3 of the discharging phase (ϕ_D) and ϕ_{d2} is at the end of the discharging phase for simplicity. First, it is assumed that the input of the NSIQ is small (Case 1). The discharging of the NSIQ stops at ϕ_{d1} , and at the same time the GRO is disabled [t_{off} in Fig. 14(a)]. The GRO stays off until the zero-crossing of the next discharging phase [$\phi_D(2)$ in Fig. 14(a)], which can happen at any time during this phase. In the second case, the input of the NSIQ is large which cause the discharging to stop after ϕ_{d1} and the GRO to turn OFF at ϕ_{d2} . Similar to the previous case, the GRO will remain off until the zero-crossing of the next discharging phase. From this, we can divide t_{off} into three portions: q_{e1} dependent time, always-OFF time (during sampling phase ϕ_S), and zero-crossing of the next discharging phase. It is important to note that the zero-crossing time is directly related to the input voltage of the NSIQ. Therefore, the zero-crossing can happen anywhere during $\phi_D(2)$ since the input of the NSIQ in the proposed loop mostly consists of the filtered quantization error [4]. Assuming that the zero-crossing time has uniform probability density function (PDF) with a mean of $T_s/4$ (half of the discharging period), the t_{off} in case 1 also has the same PDF with a mean of $13/12 \cdot T_s$ (by adding q_{e1} dependent time, always-OFF time, and mean of the PDF) while case 2 has the same PDF with a mean of $3/4 \cdot T_s$ (by adding always-OFF time and the mean of the PDF). The overall PDF t_{off} can be obtained from the PDFs of cases 1 and 2 which is shown in Fig. 14(b).

The simulated GRO leakage effect is shown in Fig. 14(c) and (d). The proposed modulator (2nd-order loop filter with the DNSQ) is compared to a conventional 3rd-order modulator with a GRO-based quantizer for a fair comparison of the 4th-order noise-shaping effect. Also, the worst case is used as a quantity of leakage which is defined by

$$V_{L\text{-worst}} = I_0 \cdot t_{\text{off-worst}} / C_p \quad (7)$$

where I_0 , $t_{\text{off-worst}}$, and C_p represent the leakage current (assumed constant for simplicity), the worst case (longest) OFF time which happens from ϕ_{d1} in $\phi_D(1)$ to ϕ_{d2} in $\phi_D(2)$ in Fig. 14(a), and the parasitic capacitance at the GRO, respectively. In this design, the simulated (expected) values of I_0 , $t_{\text{off-worst}}$, and C_p are 10 nA, 2 nS, and 10 fF, respectively. Fig. 14(c) shows the effect of the GRO leakage where $V_{L\text{-worst}}$ is 50% of the LSB_{GRO}, which means that the phase of the GRO is changed by 50% due to the worst case leakage. As shown, the performance of conventional modulator becomes distortion limited because the GRO leakage is signal dependent, whereas the GRO leakage in the proposed modulator mainly increases the noise floor without adding any distortion as t_{off} is strongly q_{e1} dependent. Fig. 14(d) shows the GRO leakage in terms of the worst case leakage. It can be clearly seen that the proposed modulator can tolerate more GRO leakage than the conventional type.

E. Effect of Gain Mismatch Between NSIQ and GRO-Based Quantizer

Although the propagation delays of delay cells for both the GRO and DLL are matched closely as discussed in the previous section, gain mismatch between the NSIQ and the GRO-based quantizer may still be exhibited due to the different loading or device mismatch of delay cells. Thus, the mismatch between the oscillation period of GRO and the time duration from ϕ_{d1} to ϕ_{d2} (or timing period for 1LSB in NSIQ) causes the gain mismatch, which can be presented as

$$e_{\text{gain}} = \frac{T_{\text{GRO}}}{T_{\text{NSIQ_LSB}}} \quad (8)$$

where T_{GRO} and $T_{\text{NSIQ_LSB}}$ denote the oscillation period (1/F_{GRO}) of GRO and the duration of 1LSB in NSIQ, respectively. With the gain mismatch in (8), the output of the modulator is given by

$$Y = X \cdot \text{STF} + \text{NTF}_{\text{LF}} \cdot (-e_{\text{gain}}) \cdot (1 - z^{-1}) \cdot q_{e1} \\ - \text{NTF}_{\text{LF}} \cdot (1 - z^{-1})^2 \cdot q_{e2}. \quad (9)$$

This gain mismatch degrades the performance by imperfect cancellation of the q_{e1} at the output of the modulator. However, this non-ideal effect is suppressed by the loop filter, making it much more relaxed. In this case, the gain mismatch term with q_{e1} is third-order high-pass filtered by $\text{NTF}_{\text{LF}} \cdot (1 - z^{-1})$. A behavioral simulation has been performed to check the effect of the gain mismatch. The simulation result in Fig. 15 shows that the DSM loop minimizes SNDR degradation to less than 5 dB due to a gain mismatch of $\pm 10\%$ between the NSIQ and the GRO-based quantizer which allows relatively relaxed matching between the GRO and DLL.

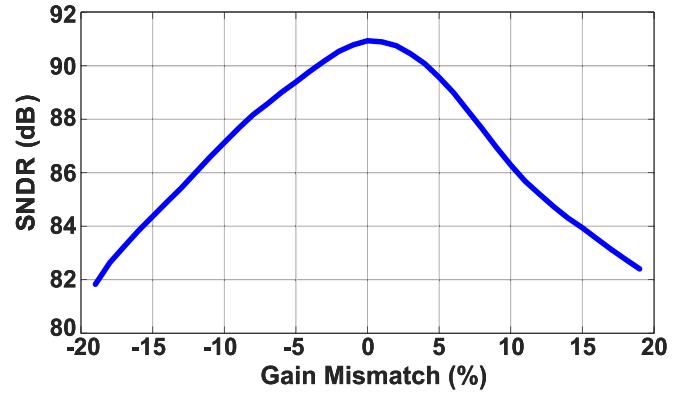


Fig. 15. SNDR performance versus the gain mismatch between the NSIQ and the GRO-based quantizer.

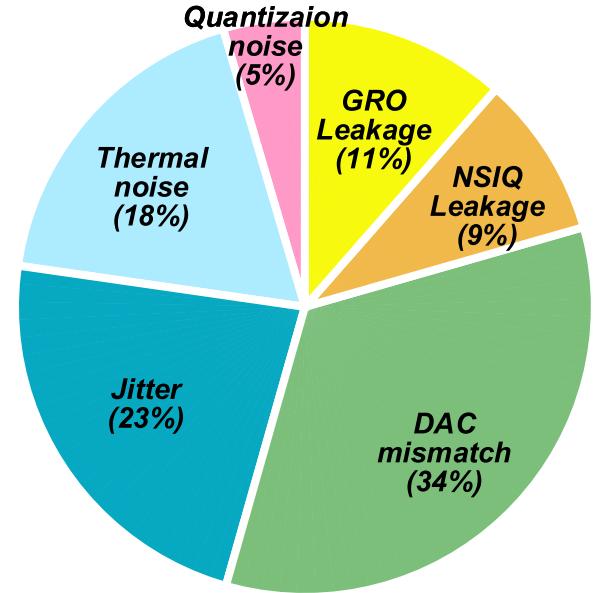


Fig. 16. Noise and distortion breakdown.

F. Noise and Distortion Breakdown

The possible distortion sources of the proposed DNSQ are discussed in the previous subsections. To sum up, the noise and distortion breakdown chart is shown in Fig. 16. The major noise/distortion source is the global DAC mismatch (both gain mismatch and unit element mismatch). Clock jitter of the global DAC is the second dominant noise source. Although the total quantization bit is 6 bit from the DNSQ, since the global DAC is not a 6-bit DAC but two 3-bit DACs, the effect of the clock jitter is limited by a 3-bit DAC.

V. MEASUREMENT RESULTS

The CT DSM using the proposed DNSQ was fabricated in a 0.13- μm CMOS process with an active area of 0.17 mm². The die photograph is shown in Fig. 17. The modulator clocked at 640 MHz, consumes 11.36 mW from a 1.2-V supply, of which 4.48 mW is drawn by the analog part, 3.63 mW by the digital circuitry, and 2.25 mW by the clock generation circuitry.

Fig. 18 plots the measured 32k windowed FFT spectrum of the modulator output with a -1 dBFS 3-MHz input sine

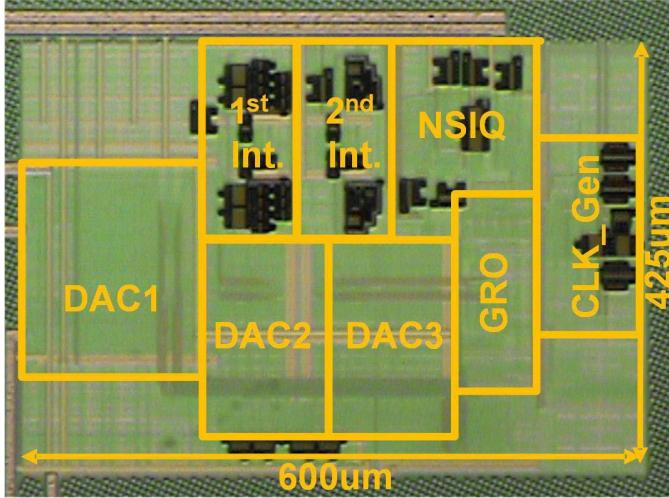


Fig. 17. Die microphotograph of the fabricated DSM.

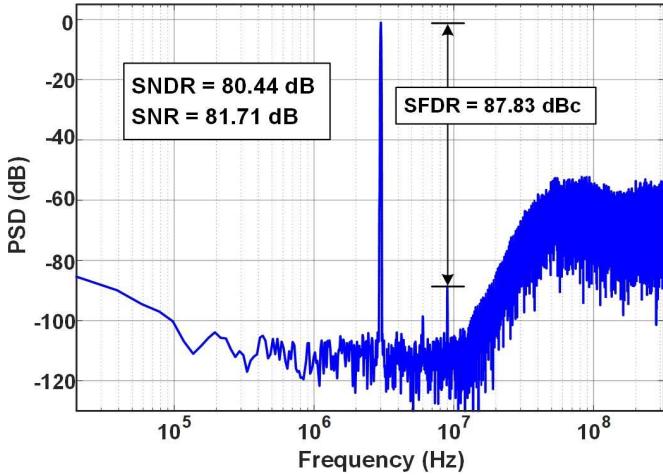


Fig. 18. Measured 32k-samples FFT output spectrum.

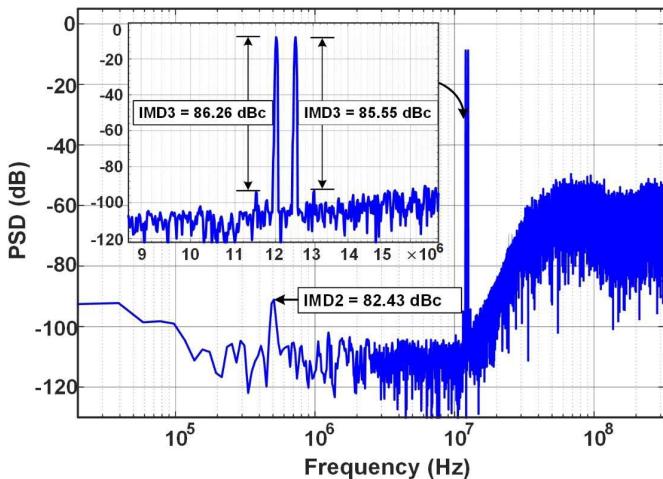


Fig. 19. Measured output spectrum with two input tones at 12 and 12.5 MHz.

wave at a sampling frequency of 640 MHz. It illustrates that the modulator achieves 4th-order noise shaping. In a 15 MHz BW, the proposed DSM achieves a peak SNDR, SNR, and SFDR of 80.4, 81.7, and 87.8 dB, respectively. In Fig. 19, two in-band sinusoidal input tones with -9 dBFS

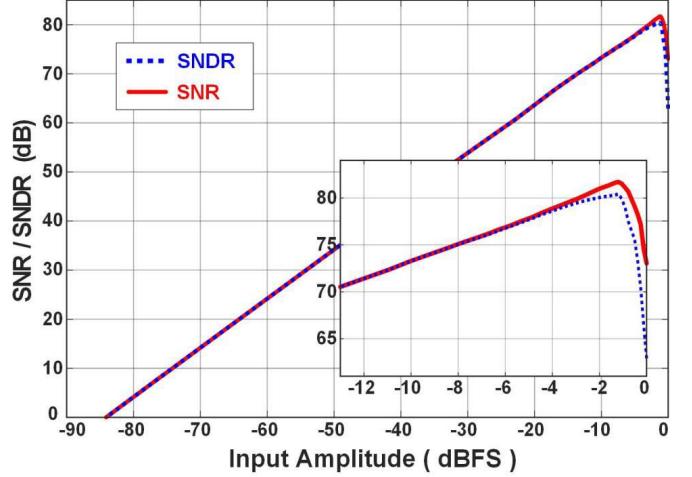


Fig. 20. Measured SNDR and SNR versus varying input signal amplitudes.

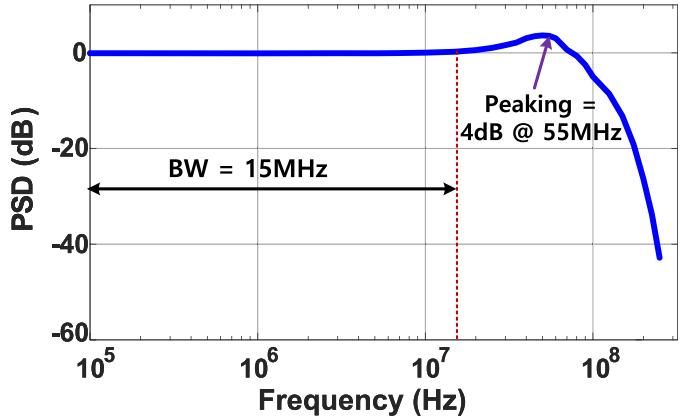


Fig. 21. Measured STF.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This Work	[4]	[25]	[26]	[27]
Technology (nm)	130	130	65	28	40
Supply (V)	1.2	1.2	1.0	1.2/1.5	-
Fs (MHz)	640	640	1000	640	1200
Bandwidth (MHz)	15	10	10	18	20
DR (dB)	82.9	78.5	77	78.1	70
Peak SNDR (dB)	80.4	75.3	72.2	73.6	69.4
Peak SNR (dB)	81.7	75.5	76	75.4	-
Peak SFDR (dB)	87.8	94.1	77.8	80.5	-
Power (mW)	11.4	7.19	1.57	3.9	3.24
Active Area (mm ²)	0.17	0.08	0.027	0.08	0.0194
FOMWa (fJ/conv)	44.1	75.9	23.6	27.7	28.4
FOMSch (dB)	174.1	169.9	170.2	174.7	164.3

at 12 and 12.5 MHz are applied and it shows the IMD3 and IMD2 of 85.5 and 82.4 dB, respectively. The measured SNR and SNDR as a function of the input amplitude are plotted in Fig. 20. The measured dynamic range is 82.9 dB and the full-scale of the modulator is 1.2 V_{p-p}. This measured performance with the low power consumption shows the effectiveness of the proposed architecture combined with the DNSQ.

Fig. 21 shows the measured STF of the modulator and it shows 4-dB peaking around 55 MHz as expected for the feedforward architecture. Table I summarizes the measured performance and compares it with the state-of-the-art DSMs with similar BW and resolution. The proposed DSM achieves a Walden FOM ($FOM_{Wa} = \text{power}/(2 \cdot \text{BW} \cdot 2^{\text{ENOB}})$) of 44.1 fJ/conversion-step and a Schreier FOM ($FOM_{Sch} = (\text{DR})_{\text{dB}} + 10 \cdot \log(\text{BW}/\text{Power})$) of 174.1 dB.

VI. CONCLUSION

A DNSQ using a Gm-C-based NSIQ and a GRO-based quantizer were presented and the details of its properties and implementation in a CT DSM were discussed in this paper. The proposed DNSQ not only provides a 2nd order of noise shaping, but also performs 6-bit quantization effectively with a digital back-end integrator. As a result, the efficiency of the DSM can be significantly increased by the 2nd-order noise shaping from the quantizer, and the quantizer can be further improved with scaled CMOS nodes.

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