60-dB SNDR 100-MS/s SAR ADCs With Threshold Reconfigurable Reference Error Calibration

Chi-Hang Chan, *Member, IEEE*, Yan Zhu, *Member, IEEE*, Cheng Li, Wai-Hong Zhang, Iok-Meng Ho, Lai Wei, Seng-Pan U, *Fellow, IEEE*, and Rui Paulo Martins, *Fellow, IEEE*

***Abstract*— This paper presents a reference error calibration scheme for successive approximation register (SAR) analog-to-digital converters (ADCs) verified with two prototypes. Such a reference error often occurs in high-speed SAR ADCs due to the signal dependent fast switching transient, and leads to a large differential nonlinearity and missing codes, eventually degrading conversion accuracy. The calibration concept aims to differentiate the error outputs and correct them by simply performing a subtraction in the digital domain. It runs in the background with a little hardware overhead, and does not depend on the type of the input signal or reduce the dynamic range. Two prototypes were measured which are made up of different reference generation circuits. Design #1 has the reference voltage from off-chip and a 3-pF decoupling capacitor on-chip, while design #2 includes an on-chip reference buffer. Both designs were fabricated in 65-nm CMOS and achieve at least 9-dB improvement on signal-to-(Noise + Distortion) ratio (SNDR) after calibration. The total core area is around 0.012 mm^2 for both chips and the Nyquist SNDR of designs #1 and #2 is 59.03 and 57.93 dB, respectively.**

***Index Terms*— Reference buffer, reference error calibration, successive approximation register (SAR) analog-to-digital converter (ADC), threshold reconfigurable comparator.**

I. Introduction

SUCCESSIVE approximation register (SAR) analog-to-digital converters (ADCs) [1]–[3] exhibits excellent energy efficiency due to their simple structure and operation. The SAR ADC often employs a capacitive digital-to-analog converter (DAC) to store the input signal, which is then controlled by the SAR logic based on the comparator's decisions to perform the binary-searched approximation to the input. Though the sequential operation in the SAR ADC limits the conversion speed, its primarily digital implementation benefits from technology down-scaling which enables high-resolution designs at moderate speed [1]–[3]. Furthermore, low-power dynamic comparators [4], [5] are usually adopted in SAR ADCs working at medium to high resolution. While the switching power of the DAC is fully dynamic, the energy per conversion step [figure of merit (FoM)] can be low [4], [5]. Previous designs mostly explored low-power DAC switching techniques [2]–[5] and improved the logic circuit [6], [7] that further pushed the FoM of SAR ADCs toward the theoretical limit [8]. However, when considering peripheral circuitries for ADC's interface, such as input buffer [9], reference buffer [10], and the clock receiver, they can be even more power hungry than the ADC core and power reduction in the converter becomes negligible. It remains a challenge to be addressed, but simultaneously maintains good energy efficiency in both the ADC core and its interface circuitries.

As the SAR conversion relies on the switched-capacitor DAC to subtract the input from the references, a fast DAC switching is desirable to achieve high speed and high resolution. The delay in each bit cycling is usually dominated by the DAC settling in medium to high resolution, and sufficiently low-output impedance of the reference buffer for fast reference voltage recovery leads to substantial power dissipation [10], [11]. Alternatively, to relax the tradeoff, a large number of decoupling capacitors (several tens to hundreds picofarad) are often introduced to suppress the switching ripple from the reference voltage, but that imposes a large core area which is highly undesirable as the cost of die area is extremely high in advanced technologies.

Adding redundancies in successive approximation (SA) conversion can relax the settling accuracy for the leading bits, ultimately reducing power from the reference buffers. However, this approach either needs extra capacitors in the DAC [12] thus reducing the dynamic range, or has limited tolerance range due to the constraint on the DAC arrangement [1]. Other than redundancy, there are also compensation methods. Adding the reservoir capacitors [13] can ease the most significant bit (MSB) capacitor settling, but it takes up a large area and degrades SNR as the extra capacitors are separated from sampling capacitors. The data driven charge compensation method [14] similarly can reduce the switching transient in MSB settling, but it requires matching between the SA and the compensation logic, adding to design complexity.

Different from using redundancies this paper proposes a threshold reconfigurable reference error (TRRE) calibration scheme to correct settling errors caused by switching transients in leading bits. The errors are detected during SA conversion adaptively and fixed in the digital domain with

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C.-H. Chan, Y. Zhu, C. Li, W.-H. Zhang, I.-M. Ho, and L. Wei are with the State Key Laboratory of Analog and Mixed-Signal VLSI, Department of ECE, Faculty of Science and Technology, University of Macau, Macao 999078, China (e-mail: ivorchan@ieee.org).

S.-P. U is with the State Key Laboratory of Analog and Mixed-Signal VLSI, Department of ECE, Faculty of Science and Technology, University of Macau, Macao 999078, China, and also with Synopsys Macau Ltd., Macao 999078, China.

R. P. Martins is with the State Key Laboratory of Analog and Mixed-Signal VLSI, Department of ECE, Faculty of Science and Technology, University of Macau, Macao 999078, China, on leave from the Instituto Superior Técnico, Universidade de Lisboa, 1049-001 Lisboa, Portugal.

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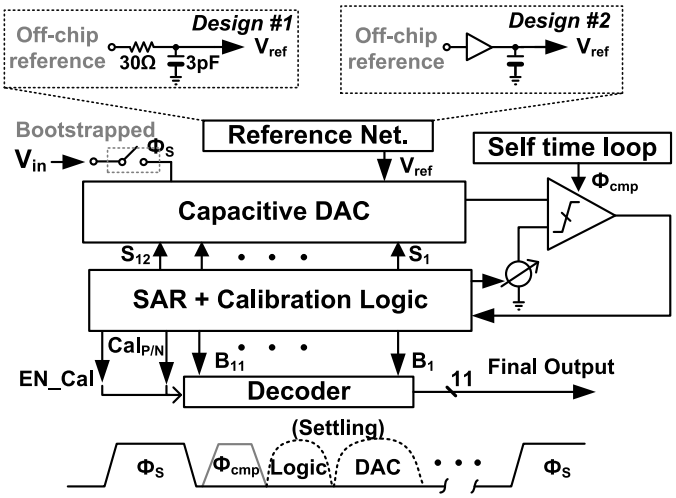

Fig. 1. Overall ADC architecture.

a large tolerance range. The detection circuit is embedded in the SA conversion and requires a little modification of the conventional SAR ADC. It also has a low-hardware overhead for decoding the final output. Moreover, the calibration concept can be used to quantize an input signal beyond the rail to rail. Two prototypes in 65-nm CMOS are measured to verify the proposed calibration, where a 3-pF decoupling capacitor is added on-chip for the reference voltages in design #1, and other design (design #2) contains a reference buffer on-chip. The experimental results of the two designs implemented with and without reference buffer demonstrate the effectiveness of the proposed calibration method. The signal-to-(Noise + Distortion) ratio (SNDR) is at least improved by 9 dB before and after calibration in both ADCs. Designs #1 and #2 have a SNDR of 59.03 and 57.93 dB at Nyquist and achieve 60.4 and 58.94 dB at a low-frequency input, respectively. Thanks to the proposed scheme, only a 3-pF decoupling capacitance needs to be added with ∼840-μW power on the reference buffer being consumed in designs #1 and #2, respectively. The total power consumptions of design #1 and #2 are 1.6 and 2.44 mW at 100 MS/s from a 1.2-V supply, respectively.

II. ADC Architecture

The overall ADC architecture is illustrated in Fig. 1, which consists of a bootstrapped sample-and-hold front-end, self-timed loop, capacitive DAC array, comparator, SAR controller, reference network circuitry, and decoder for the calibration scheme. The SAR ADC performs Vcm-based switching and has a similar operation as [2]. Reference voltage in design #1 is provided by off-chip and a 3 pF decoupling capacitor is added in on-chip. Besides, an extra 30-Ω resistance is inserted between the off-chip references and the ADC core to model the reference sources finite output impedances, while an on-chip reference buffer is added in design #2 and the off-chip reference voltages are isolated by the buffer. It is worth noting that the low dropout linear regulator (LDO) is omitted in both designs since the testing environment is relatively ideal and only contains the ADC. In order to embed the calibration scheme in the converter, two simple modifications are made. First, the threshold of the comparator is modified

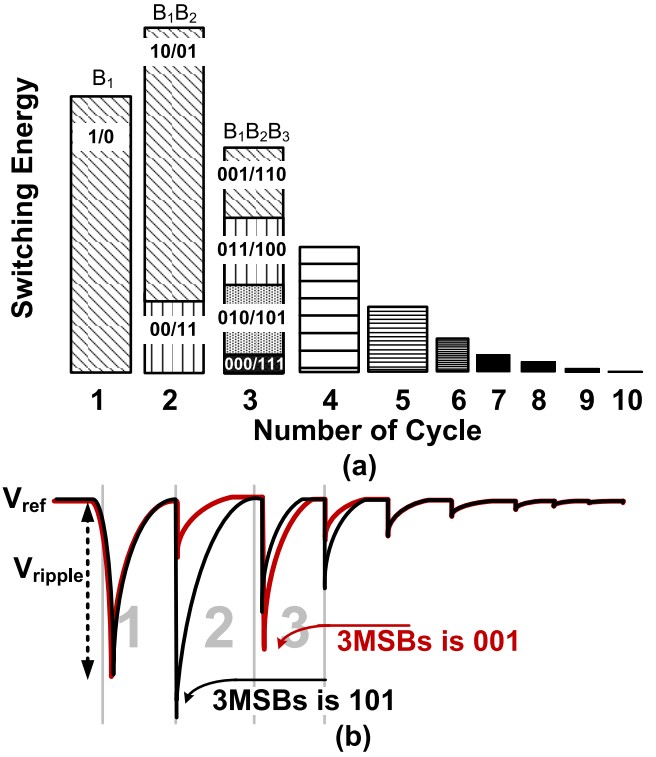

Fig. 2. (a) Switching energy versus digital outputs in ten cycles. (b) Signal behavior of reference ripple during switching transients.

to be configurable. Second, one extra cycle is introduced during the SA conversion for reference error detection. The signals EN_Cal and CalP/N indicate whether the calibration is triggered and reflected the polarity of the reference error in either case. The output codes are eventually corrected based on the calibration decision. The calibration details will be discussed in Section IV.

The total capacitance of the DAC array is 768 fF for matching consideration. A synchronous time loop with ∼600 ps for each bit cycling is designed where the time allocation for the comparison and logic processing versus the DAC settling is assigned to be 3:2 in a typical process corner. Obviously, this setup will cause the time for MSBs settling becoming rather short and large reference ripples cannot be recovered before the next comparison. Thanks to the calibration, their reference and settling errors are expected to be calibrated.

III. Reference Error in High-Speed SAR ADC

The capacitive DAC is typically employed to perform the binary-search approximation. While the capacitors in the first three leading bits occupy more than 80% of the total capacitance, they are charged or discharged according to the switching nature thus leading to a large current-induced reference ripple [15]. If this ripple is not able to recover within the required accuracy before the next bit comparison, it will eventually affect the conversion precision. The high-resolution SAR ADC has a particularly stringent requirement for reference voltages since the SAR loop provides limited time for reference recovery and the DAC settling. Such reference errors are difficult to correct at post-processing in the digital domain as they are highly signal dependent.

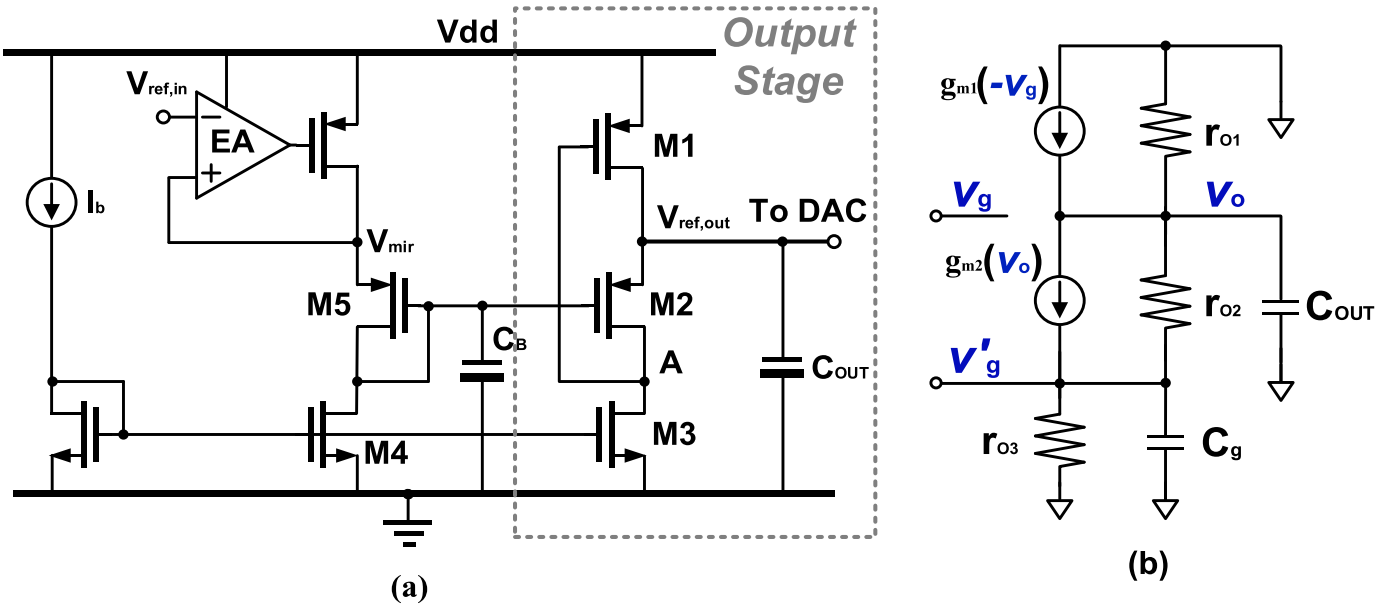

Fig. 3. (a) Schematic of FVF buffer. (b) Equivalent small signal model of FVF output stage.

Fig. 2(a) indicates the switching energy corresponding to each output code in an 11-b SAR ADC built with a binary-weighted DAC and Vcm-based switching. As shown in Fig. 2(b), the switching energy required for each bit cycling is code dependent. Therefore, the reference ripple due to the switching transient is also signal-dependent. The worst case scenario occurs when the first two leading bits results in a complementary logic decision (B_1B_2 = "10" or "01"). The switching energy for each bit cycling is gradually reduced as the remaining bits contain less number of units, implying that the reference ripples are also getting smaller.

IV. Design Considerations for the Reference Generation Circuit

In practice, analog circuitry is normally biased through a low-noise reference voltage provided by a LDO [16] that can isolate low-frequency supply noise and switching noise from the digital circuits. On the other hand, the DAC switching noise in a high-speed SAR ADC is often in the gigahertz range with heavy load, implying that the LDO will not be able to cover it in time. In order to alleviate such noise and provide fast recovery, reference buffers are required.

A. Reference Generation Circuit-Flipped-Voltage Follower

The multiple supplies for NMOS-source follower (NSF) [1], [17] topology demand additional LDOs, or charge pump in the system, which requires extra capacitors thus increasing design complexity and area. Unlike the NSF topology, the flipped-voltage follower (FVF) topology can work under a single supply. It is widely used as reference buffer due to its simple structure and fast transient performance [10]. Its schematic is shown in Fig. 3(a). The biasing circuits for devices M2 and M3 are similar to the NSF, while the FVF topology forms a local feedback loop through devices M3 and M1. The shunt feedback on the other hand helps to reduce the output impedance and improve its current sourcing capability.

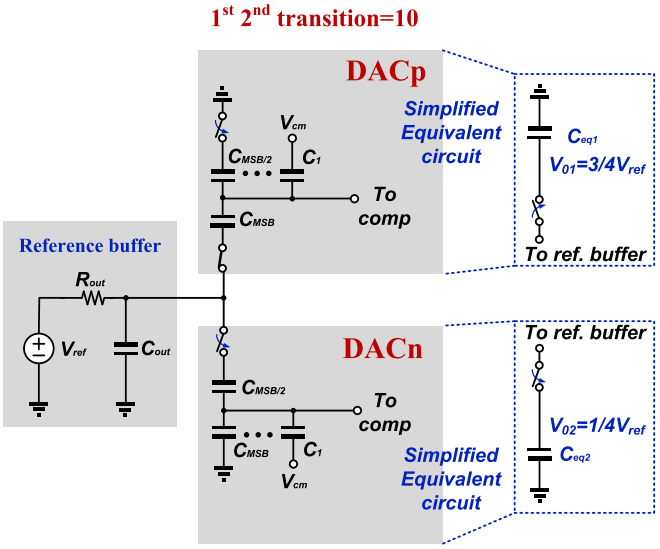

Fig. 4. Equivalent *RC* model of critical DAC settling case.

To support a high-speed and high-resolution SA operation, the gain bandwidth (GBW) product of the reference buffer needs to be large to have a fast transient response. By breaking the feedback loop, the equivalent small signal circuit of FVF is depicted in Fig. 3(b). Based on its transfer function and dominant pole location, the GBW of the FVF circuit is equal to $g_{m1}g_{m2}r_{o2}/C_{\text{out}}$, where g_{m1} and g_{m2} are the tranconductance of M1 and M2, respectively, r_{o2} is the output resistance of M2 in the saturation region and C_{out} is its capacitive load. While, the GBW of the NSF is g_m/C_{out}, where g_m is the tranconductance of the NSF input transistor. Assuming that two topologies are designed with the same current in the main branch and the same W/L ratio for the input transistor (M1)

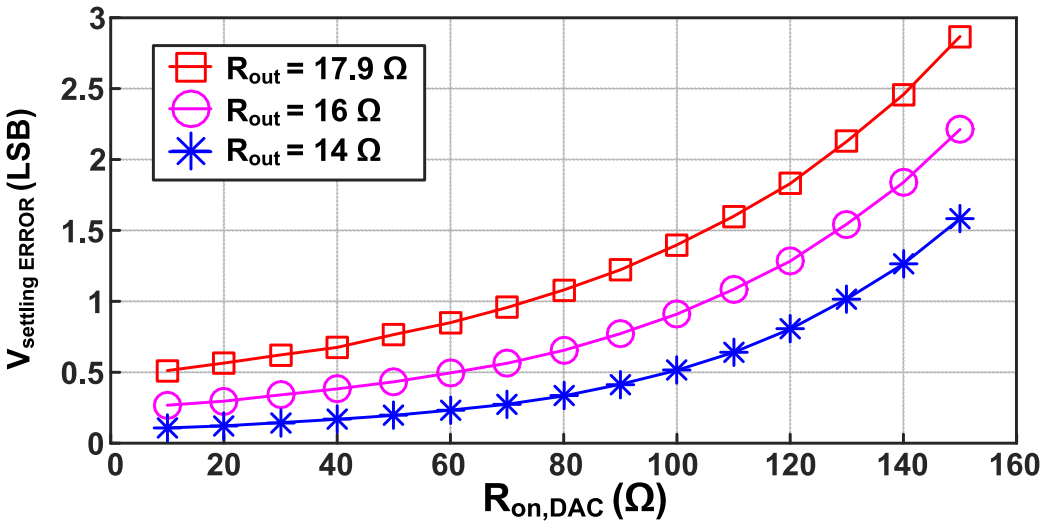

Fig. 5. Simulation result of DAC settling error in term of LSB versus $R_{\mathrm{ON,DAC}}$ in various R_{out}.

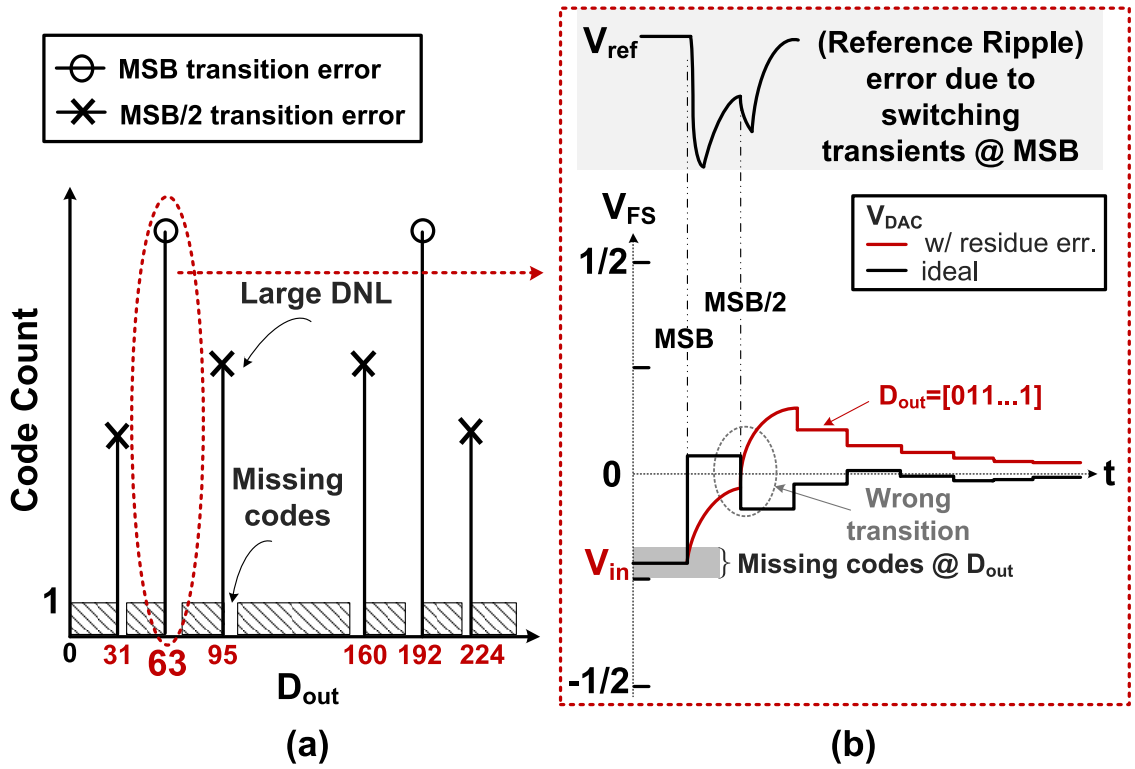

Fig. 6. (a) Code histogram of an 8 b example with reference error. (b) Signal behavior of the DAC's output.

under the same load (C_{out}).Though $g_m/g_{m1} < 2$, the intrinsic gain of M2 in FVF ($g_{m2}r_{o2}$) is much larger than g_m/g_{m1} (e.g., $g_{m2}r_{o2} > 4$ with its overdrive voltage of ~0.15 V and W/L of 1.2/0.06 μm in the adopted technology). Consequently, the GBW of FVF topology is larger than NSF leading to a better transient response. Therefore, we adopted the FVF topology as the reference buffer in this design.

B. Design Considerations of the Reference Buffer in SAR ADC

To avoid reference error during the SA conversion, the reference buffer needs to support the most critical switching transient. Fig. 4 demonstrates the MSB/2 transition of the DAC, where two leading bits result in complementary decisions drawing most switching energy. According to required switching energy the transition can be equivalent to charge an equivalent capacitor C_{eq1} from initial value (V_{01}) of $3/4V_{\mathrm{ref}}$ to V_{ref} in DAC$_p$, and a C_{eq2} from $1/4V_{\mathrm{ref}}$ to V_{ref} in DAC$_n$. For binary DAC, $C_{\mathrm{eq1}} = 1/4C_{\mathrm{dac}}$ and $C_{\mathrm{eq2}} = 1/8C_{\mathrm{dac}}$. Initially the buffer's output decoupling capacitor C_{out} providing the charge for C_{eq1} and C_{eq2} causes a reference ripple (V_{err}), which can be approximated as

$$V_{\mathrm{err}} \approx V_{\mathrm{ref}} - \left(\frac{C_{\mathrm{out}} + 3/4C_{\mathrm{eq1}} + 1/4C_{\mathrm{eq2}}}{C_{\mathrm{out}} + C_{\mathrm{eq1}} + C_{\mathrm{eq2}}}\right) V_{\mathrm{ref}}. \quad (1)$$

The ripple can be recovered with support from the reference buffer, which simultaneously provides charges for C_{out}, C_{eq1}, and C_{eq2}. For n-bit resolution, the settling time for the error within β least significant bit (LSB) can be derived as

$$t_{\text{wst}} \approx \ln\left(\frac{V_{\text{err}}}{\beta\Delta}\right)\cdot\tau = \ln\left(\frac{2^N V_{\text{err}}}{\beta V_{\text{ref}}}\right)\cdot R_{\text{out}} \cdot(C_{\text{eq1}} + C_{\text{eq2}} + C_{\text{out}}) \quad (2)$$

where Δ is the LSB, τ is the time constant dominated by the buffer output impedance R_{out}. According to design, C_{out} is set to $4C_{\text{dac}}$ which helps the decoupling capability. It is worth noting that (2) ignores the ON-resistor of the DAC switches ($R_{\text{ON,sw}}$) that can induce error in the estimation. On the other hand, when considering the $R_{\text{ON,sw}}$ it is difficult to derive a close-loop formula as it affects the V_{err} at (1) and the equivalent RC-network is rendered complex as other capacitors connecting to the reference also need to be considered. Therefore, a simulation is performed under the adopted technology with design parameters in this paper. With 11-b resolution, the target SNDR is around 60 dB which leads to $N = 11$ and $\beta = 0.5$ (considering a margin for other errors). The loop time spared for the DAC settling is ~300 ps and total DAC capacitance of 768 fF. From the simulation as illustrated in Fig. 5, it can be found that the output impedance of the reference buffer should be less than 17.9 Ω even when R_{ON} is close to 0, which is consistent with (2). At the same time with reasonable ON-resistance 100 Ω (W/L = 12/0.06 μm), the buffer output impedance has to be 14 Ω in order to meet the above target. Based on the FVF topology introduced in the last section, the reference buffer would consume >2.4 mW power which is at least twofold larger than state-of-the-art ADC designs in the adopted technology.

V. Proposed TRRE Calibration and Comparison With State of the Arts

A. Reference Error Behavior in SAR ADC

In order to demonstrate error behavior caused by insufficient DAC settling and reference ripple, an 8-bit SAR ADC with reference errors in the 2nd bit transition is adopted in the following example. Its output code histogram is plotted in Fig. 6(a) which can well demonstrate the error behavior. There exists both missing codes and large hits at the digital outputs (D_{out}), corresponding to the ADC transition points of the MSB/2 and MSB/4. On the other hand, Fig. 6(b) depicts the signal behavior of the DAC output (V_{DAC}) during the successive approximation. The 1st MSB decision of the ADC does not depend on reference accuracy as differential input signals (V_{in}) are compared directly without any switching. Since V_{in} is smaller than the comparison threshold "0," the MSB is set to "0." Correspondingly, the MSB capacitor is charged to V_{ref} for the next bit comparison. Charging such large capacitance with finite impedance on V_{ref} node causes a large reference ripple [Fig. 6(b) (Top)]. As such, if this ripple cannot recover before the next comparison, it will result in a wrong transition at MSB/2. Ideally in this example, the V_{DAC} should be smaller than the comparison threshold but now V_{DAC} is still above "0" due to the false previous decision.

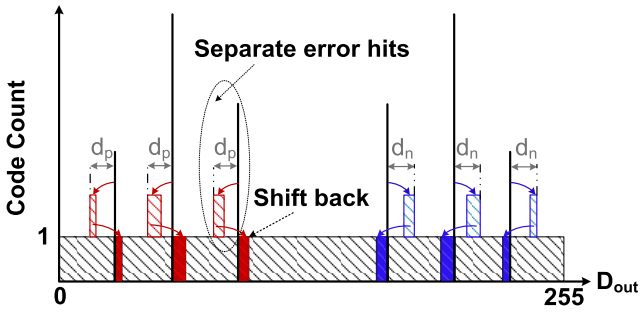

Fig. 7. Proposed TRRE calibration concept in output code histogram.

Such error makes V_{DAC} unable to converge back to the comparison threshold within 1/2 LSB and the decision of the rest of the bits all equal to "1." As a result of the reference errors, certain ranges of V_{in} have the same digital representation which explains why there is a large hit and missing adjacent codes at $D_{\text{out}} = 63$. Such errors cannot be recovered by any post-signal processing in the conventional SAR ADC without redundancy scheme, since the code in large hits cannot be separated to represent their corresponding inputs. To correct the error in the digital domain, error detection with certain analog circuit modifications are introduced by the proposed scheme further detailed in Section V-B.

B. Proposed Calibration Technique and Considerations

The proposed TRRE calibration concept is demonstrated with the histogram plot of a 6-bit ADC in Fig. 7. It is important to recall here the fact that the reference error causes large hit and missing codes in the local transition. The idea is to remove the large hits and fill up the gaps. First, those large hits due to single dependent reference ripple must be separated, then by shifting them back to their corresponding digital outputs, the gap from the missing codes can be filled.

The code-separation is done during the SAR conversion by inserting an additional error-detection step and new threshold levels. Fig. 8 illustrates the detailed operation in a 6-bit ADC example with and without reference errors in the conversion. The top-plate residue corresponding to each operation is shown in the blue and red curve at the bottom of Fig. 8. In this example, the 3rd step is assigned for error detection. During the sampling phase, the input signal is sampled at the top plate of the DAC. As mentioned before, the MSB transition of the ADC is reference error independent, which directly compares the input signal (V_{in}) with threshold level "0," thus avoiding the switching activity in the DAC. As V_{in} is smaller than 0, the 1st transition of the DAC sets the MSB ($16C$) to $+V_{\text{ref}}$. Assuming that the red residue contains a reference error in the 1st transition, the decision D_1 sets the MSB/2 ($8C$) to $+V_{\text{ref}}$. On the contrary, the blue curve is fully settled before the next comparison and MSB/2 is set to $-V_{\text{ref}}$. The decision of the 3rd comparison (D_2) determines the transition of $4C$ as well as the reset polarity of the upcoming error detection step. If $V_{\text{DAC@2}} > 0$, the rest of the capacitor all reset to $+V_{\text{ref}}$ in the 3rd transition and vice versa to $-V_{\text{ref}}$.

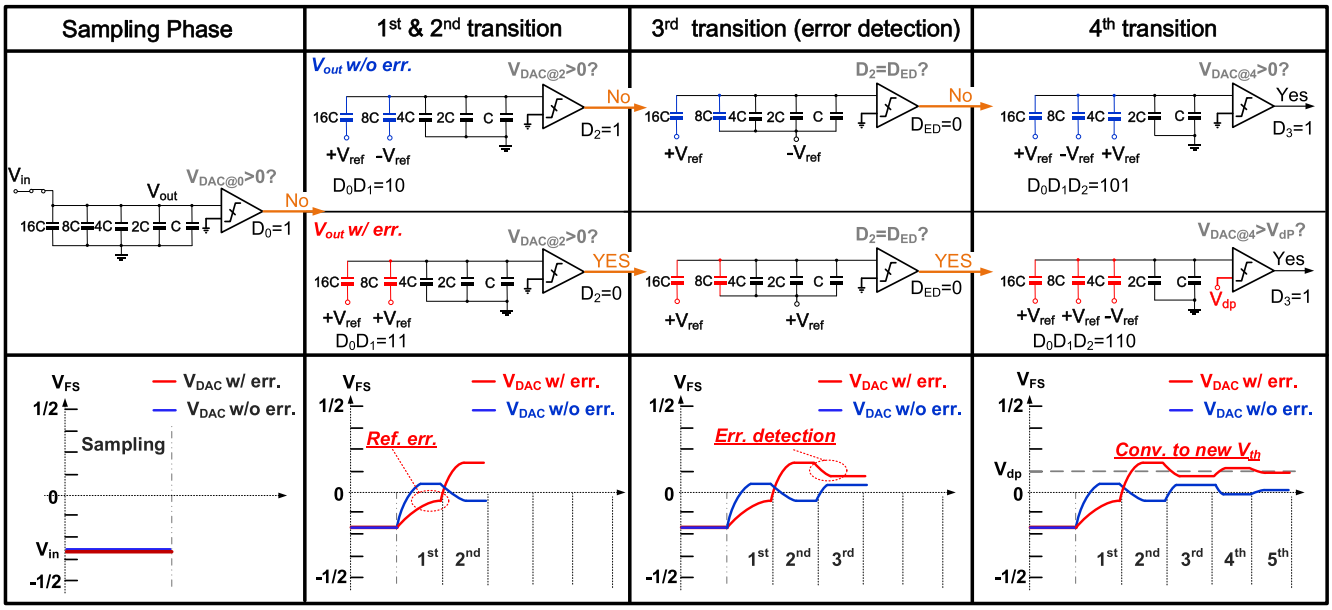

Fig. 8. ADC operation and signal behavior of the DAC's output during calibration. Two examples with and without the reference error are demonstrated.

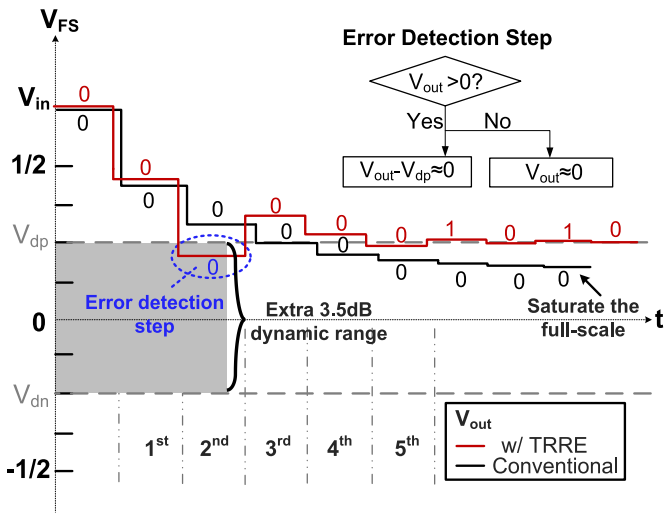

Fig. 9. DAC outputs during the quantization of an input signal larger than full-scale rail with and without the TRRE calibration.

The 3rd supplementary cycle detects whether the final residue crosses the comparison threshold. If the decision in the adjacent comparison is the same ($D_2 = D_{ED}$), it indicates that the reference error does affect the previous comparison. Then, $-V_{ref}$ will apply to $4C$, the rest of the capacitors are reset to Gnd (Vcm in differential implementation) and the V_{DAC} converges to a new threshold V_{dp} for the rest of the bits cycling. If $V_{DAC@4} < 0$, implying no occurrence of comparison error, then the ADC resumes its normal conversion. If the residue conveys to a new threshold, the corresponding outputs will contain a constant offset from nominal values. Such offset can be easily measured from the mean of the output code separately between the normal and with the new threshold conversion cases. Two extra digital signals are brought off-chip which are EN_cal and CalP/N. EN_cal indicates whether the calibration is triggered and CalP/N represents the reference error polarity. After obtaining the offset, a shifting operation is done in the digital domain to obtain the final result.

In order to cover both positive and negative reference errors, a complementary threshold (V_{dn}) is also required which can easily be accomplished in a differential operation by flipping the reference input polarity of the comparator. Besides, it is worth noting that V_{dp} and V_{dn} do not have matching requirements, since their value only determines the error correction range. Once sufficient design margin is left, then the calibration accuracy can be guaranteed. The correction range is correlated with the bit assigned for error detection. If the mth ($m > 1$) transition is set as the error detection step, the maximum error covering range can be up to $1/2^{m-1}V_{FS}$. Furthermore, it is possible that settling error occurs during the error detection DAC switching. However, as this switching only consumes less than 20% of the total switching energy, the error can be suppressed by sufficient low-impedance reference network with decoupling. While the proposed technique can only handle the reference error during the SAR conversion, the cycle-to-cycle reference incomplete recovery error is suppressed by a low enough output impedance reference network.

C. Comparison With the Existing Solutions

The non-binary searching algorithm [18] or adding redundancy [1], [12] in SAR conversion provides certain amount of correction range in the corresponding conversion cycles depending on the setup, which allows the previous conversion errors, such as incomplete settling or dynamic offset, to be recovered in the later comparison cycles. The non-binary searching can be implemented simply by using a sub-radix-2 DAC. Even though more comparison cycles are needed, it does not degrade overall conversion speed as each cycle can be condensed. The Binary-scaled error

TABLE I
COMPARISON WITH EXISTING SOLUTIONS

	This Work	BEC [12]	BRW [1]
Bit Weight (MSB-LSB)	Binary	1024,512,256,128 128,64,32,16,8,8, 4,2,2,1	960,512,272,144, 72,40,20,12,6,4,2, 2,1,1
Capacitor Overhead	No	Yes	No
Radix	2	2	<2 (Non-fixed)
Digital logics	5FA 1HA *(only activated when error is detected) 6MUX	10FA 1HA 11MUX	11FA 2MUX
No. bit cycle / Resolution	12/11b	14/11b	13/11b
Dynamic Range	Enhanced	Reduced	Keep
Switching Cycle	Tolerance Range (%V_{FS})		
1st	6.25%	6.2%	2.9%
2nd	6.25%	6.2%	2.9%
3rd	6.25%	6.2%	1.4%

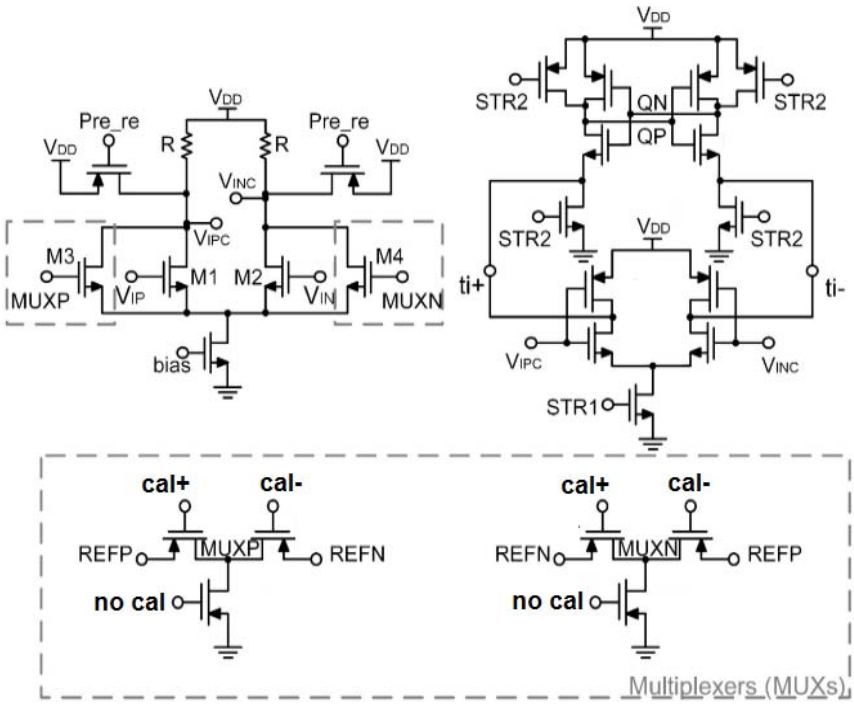

Fig. 10. Circuit Schematic of reference configurable comparator.

compensation [12] effectively corrects the conversion errors through the insertion of several binary-weighted redundant bits in the DAC. The error tolerance range normalized to full scale can be derived as for ith cycle and N-bit ADC

$$\mathrm{Er_{tol}}(i) = \frac{\sum_{k=i+2}^{M-1} C_k - C_{i+1}}{2^N C + C_r} \times 100\%(i+1 < M-1) \quad (3)$$

where C is the unit capacitor in the DAC array, C_i is the capacitance switched in the ith cycle, the C_r is inserted capacitor for the redundant bit, and M is the total bit resolution. The implementation of the addition based decoder is simpler and costs less power dissipation when comparing it with [18]. However, the dynamic range of the ADC can be significantly reduced when a large error range needs to be covered. Another binary-scaled recombination weighting method [1] splits the MSB capacitor for redundant bits generation. Therefore, the overall array capacitance remains the same as the conventional ($C_r = 0$) avoiding the loss of the dynamic range, while the

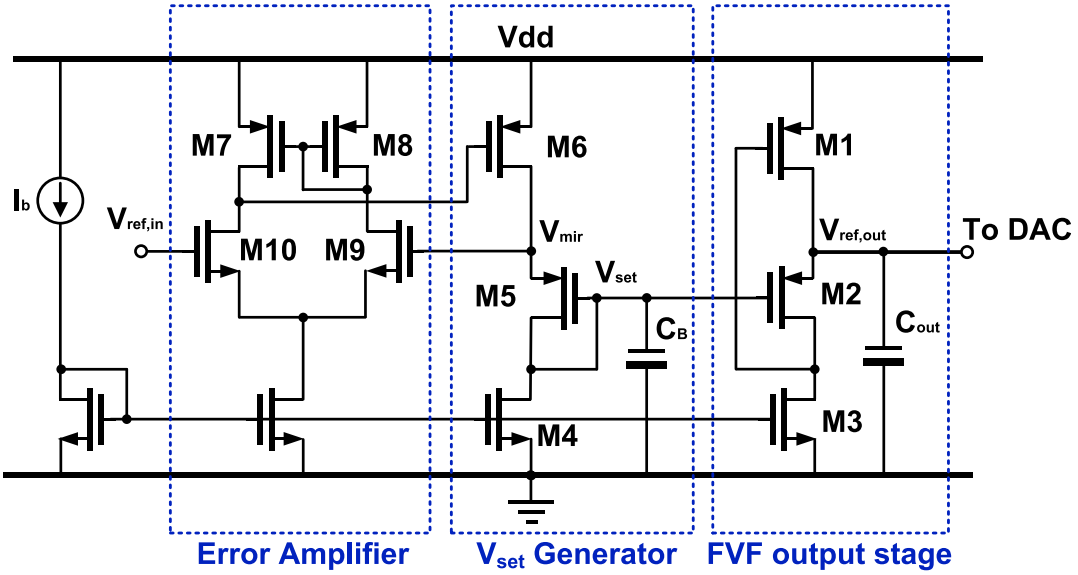

Fig. 11. Complete circuit schematic of adopted reference buffer.

tradeoff is related with the fact that the error tolerance range is limited by the number of the capacitors split from MSB. The proposed scheme is compared with the above existing solution based on the setup of this prototype. The results are shown in Table I. Determined from the post-layout simulation, the error detection bit in the proposed method is set at the 5th bit transition resulting in error tolerance range of 6.25% from the previous three leading bits. Other methods are arranged for a similar correction range and they are also depicted in Table I. It is worth noting that our scheme requires the references to settle fully by the time the error detection bit decision is made, which is similar in the redundancy schemes [1], [12].

It can be observed that the proposed calibration does not have an extra capacitor overhead. It also has a minimum number of cycles. The decoder digital overhead is less when compared with others and it is worth noting that the decoder is not always working and it is only activated when calibration is needed. Furthermore, the proposed calibration concept can be used to quantize an input signal swing larger than the full scale rail corresponding to the enhancement of the dynamic range. As illustrated by an example in Fig. 9, once V_{in} exceeds the full scale rail, the digital output will be all 0 and the ADC is saturated. In this example, the error detection step is set at the 2nd transition which determines whether $V_{\text{in}} - 1/2V_{\text{FS}}$ crosses the threshold or not by resetting all the rest of bits to $-V_{\text{ref}}$. In the case of $V_{\text{DAC2}} > 0$, the DAC output converges to the threshold V_{dp} that is set as $1/4V_{\text{FS}}$. Therefore, the final output can be obtained by subtracting the V_{dp} from the digital output (000001010). An extra 3.5-dB dynamic range can be achieved in this specific example. Depending on the mth transition cycle assigned for error detection, the extra input covering range is $1/2^{m-1}V_{\text{FS}}$.

On the other hand, the extra transistor pair for the reference voltage in the comparator can induce extra noise which requires extra power to suppress. However, the proposed scheme does not reduce the dynamic range and it can simplify the decoding logic. Such power consumption overhead can be relieved by these parts. The switchable comparator reference can drift with voltage and temperature changes and therefore has to be monitored in the background. In conclusion, when comparing with the redundancy scheme, the proposed structure can keep the DAC in full binary which favors the layout arrangement. Besides, our scheme can also correct a large reference error without any penalty in the dynamic range.

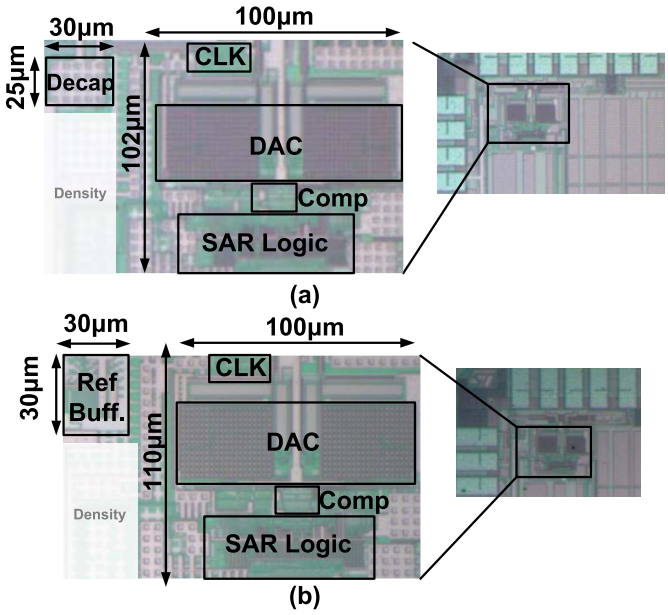

Fig. 12. Chip microphotographs of (a) design #1 and (b) design #2.

VI. Circuit Implementations

A. Threshold Reconfigurable Comparator

The comparator consists of a resistive load preamplifier followed by a two-stage dynamic latch [19] as shown in Fig. 10, which achieves an input-referred noise of 500 μV_{rms}.

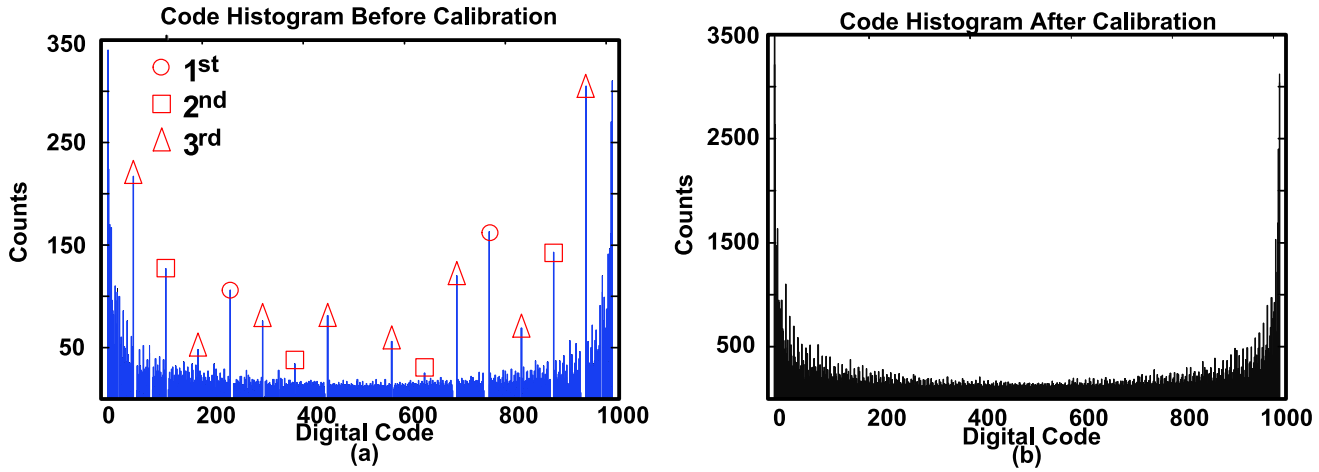

Fig. 13. Code histogram of the design #1 with sinusoid wave input. (a) Before calibration. (b) After calibration.

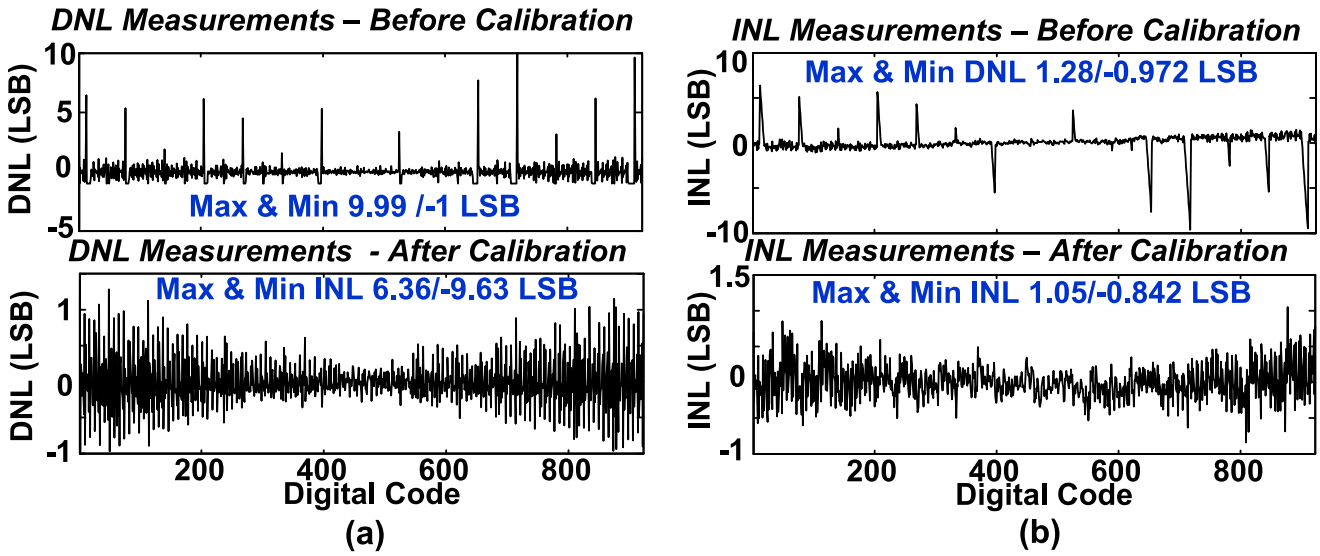

Fig. 14. (a) DNL and (b) INL of design #1 before and after calibration.

For threshold voltage configurability, an extra input transistors pair (M3 and M4) is inserted at the pre-amplifier whose voltage is controlled by a multiplexer. During the normal SAR operation, the gate voltage of M3 and M4 are pulled to Gnd; while it switches to REFP/REFN depending on reference error polarity. MOS decoupling capacitors are added on the reference voltage to suppress the thermal and kick back noises. According to post-layout simulation the reference error limited the conversion SNDR to near 50 dB and the maximum ripple error is around 120 mV with approximately 5% of V_{FS}. Therefore, the error-detection step is set at the 5th cycling that can tolerate 6.25% error of V_{FS}. The thresholds V_{dp} and V_{dn}, which are originally designed as ± 75 mV could vary about 20% under the mismatch variation. As mentioned before, the code-separation does not rely on the accuracy of two additional thresholds, which only require an error range within 5%.

B. Reference Buffer

Fig. 11 illustrates the circuit schematic of the reference buffer adopted in this design. Similar to [20], the complete circuit schematic consists of three parts, including the error amplifier, V_{set} voltage generator and the FVF output stage. External reference voltage $V_{\mathrm{ref,in}}$ is provided at the input of the error amplifier in an unit-gain configuration. The mirror voltage V_{mir} at the source of M5 is forced to be equal to $V_{\mathrm{ref,in}}$ by the negative feedback loop. The error amplifier is designed with a simple low-power differential opamp, which also provides supply-noise-rejection for V_{mir}. The dc gain of the error amplifier in this design is 36.6 dB, with a unit-gain bandwidth of 40 MHz and phase margin of 84°. V_{mir} is used to generate the V_{set} by the diode-connected transistor M5. In the FVF output stage, the V_{set} at the gate of M2 sets the output voltage $V_{\mathrm{ref,out}}$ such that $V_{\mathrm{ref,out}}$ is mirrored from V_{mir}. Since M2 and M5 are designed to be well matched (same size and same biasing condition), $V_{\mathrm{ref,out}}$ is equal to V_{mir}. Hence, $V_{\mathrm{ref,out}} = V_{\mathrm{mir}} = V_{\mathrm{ref,in}}$. A decoupling capacitor C_B of 2 pF is placed at the gate of M2 and M5 for isolating the switching noise coupling from the DAC switching to the V_{set} voltage generator circuit, as well as stabilizing the error amplifier with negative feedback. The voltage output of the

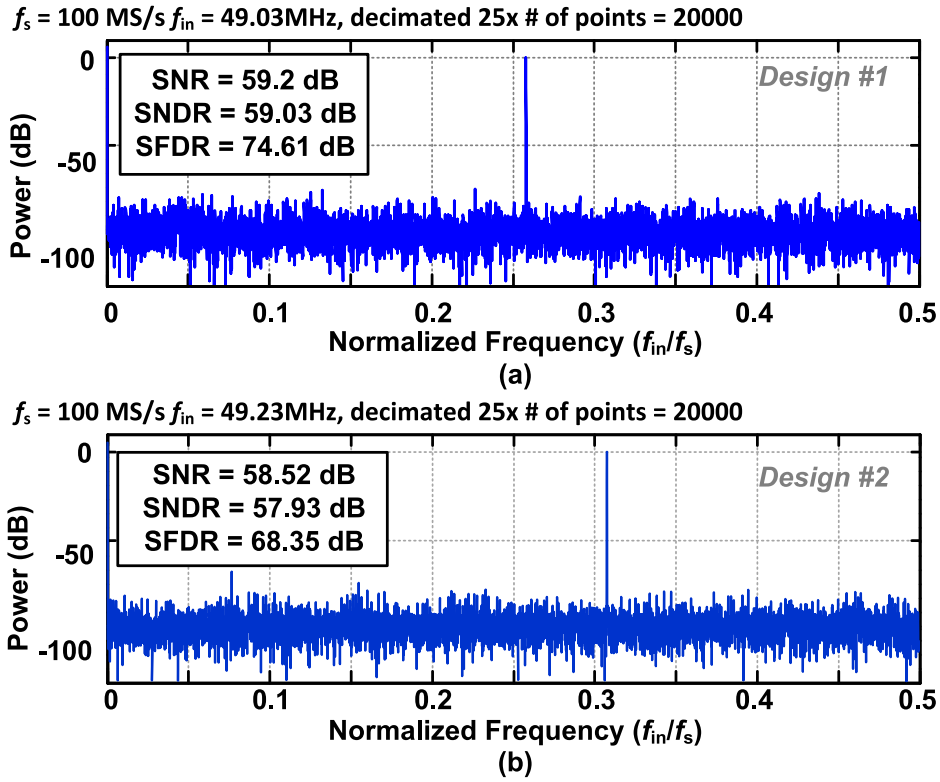

Fig. 15. Output spectrum at around Nyquist input after calibration for (a) design #1 and (b) design #2.

FVF based reference buffer is designed to be 1 V with a supply voltage at 1.2 V.

Thanks to the proposed calibration in this design, the reference buffer can be designed to be partially settled during the transition of three leading bits. In addition, by using a relatively large current (∼580 μA) and a decoupling capacitor C_{out} of 3 pF, the internal pole at the gate of the M1 is pushed to a high frequency up to several gigahertz and the dominant pole of the fast FVF feedback loop is designed to be at the output node. Such decoupling also helps to reduce the kick-back noise from the DAC. Besides, the large current ensures low-output impedance for the reference buffer that allows the reference voltage to be fully recovered during the last few bits cycling. The low-voltage-threshold transistor is chosen for M1, M2, and M5 to achieve higher bandwidth and lower power consumption. The open-loop gain of the FVF output stage is 20 dB with a unit-gain-bandwidth of 958 MHz. Consequently, the circuit occupies a small die area and power consumption with 8% and 25% of the total ADC, respectively. Including the biasing circuit, the reference buffer consumes ∼840 μW, which is about four times smaller than the reference buffer design without the reference-settling error calibration scheme.

VII. Measurement Results

The proposed reference error calibration was implemented in two 11-b 100-MS/s SAR ADCs fabricated in a 65-nm 1P7M digital CMOS process. The input full-swing of the ADC is $2V_{pp}$. Fig. 12(a) and (b) shows the chip microphotograph of designs #1 and #2, respectively; the active area of design #1 is 0.011 mm^2 where the decoupling capacitors of the reference voltages only occupy 6.8% of the total area. The total area of design #2 is 0.012 mm^2 which includes the on-chip reference buffer. Fig. 13(a) illustrates the output code histogram of design #1 before calibration with remark of the first three transition locations. Before calibration, there are large hits and gaps near the leading bits' transition points and they are well suppressed or filled after calibration as shown in Fig. 13(b). Fig 14(a) and (b) illustrates the differential nonlinearity (DNL) and integral nonlinearity (INL) of design #1 before and after calibration, respectively. The maximum DNL and INL are 10/−1 LSB and 6.39/−9.63 LSB before calibration, respectively. The DNL and INL improved to 1.28/−0.97 LSB and 1.05/−0.84 LSB after calibration, respectively. The SNDR before calibration is 50.01 and 48.64 dB, which is improved to 59.03 and 57.93 dB after calibration in designs #1 and #2, respectively. Measured FFTs plotted at near Nyquist input frequency after calibration of designs #1 and #2 are shown in Fig. 15 (a) and (b), respectively. Though in the post layout simulation the settling accuracy of the later few bits are guaranteed, in the measurement we find that the design margin is not sufficient where the output still contains small DNL errors. The switching of less units causes smaller reference ripples, while the error referred to the DAC's output depends on the total number of units connected to the reference. To improve this, 1-bit redundancy ($2C$) can be inserted before the last two bits conversion to relax the previous settling accuracy to 0.1% consuming a negligible loss of the dynamic range. Furthermore, in case the offset is too large imposing V_{dp}

TABLE II
BENCHMARK WITH STATE-OF-THE-ART WORKS

	ISSCC '10 [12]	ISSCC' 12 [21]	A-SSCC '13 [22]	ISSCC '16 [23]	This work	
Architecture	SAR	CI-SAR	SAR	SAR+ Dig. Slop	SAR	
Technology (nm)	65	40	40	28	65	
Resolution (bit)	10	10	10	12	11	
Sampling Rate (MS/s)	100	80	50	100	100	
Supply Voltage (V)	1.2	1.1	1.1	0.9	1.2	
Power (mW)	1.13	5.54	0.47	0.35	1.6	2.44
ENOB @Nyquist	9	8.71	9.18	10.41	9.51	9.33
SFDR (db) @Nyquist	66.9	65.12	68.16	75.42	74.61	68.35
Area (mm^2)	0.026	0.08	0.0114	0.0047	0.011*	0.012**
Decoupling (F)	N/A	N/A	N/A	N/A	3p	3p
FoM @Nyq. (fJ/conv.step)	22	178	16	2.63	21.9	37.9

* including the decoupling capacitor for the reference voltages
** including the reference buffer

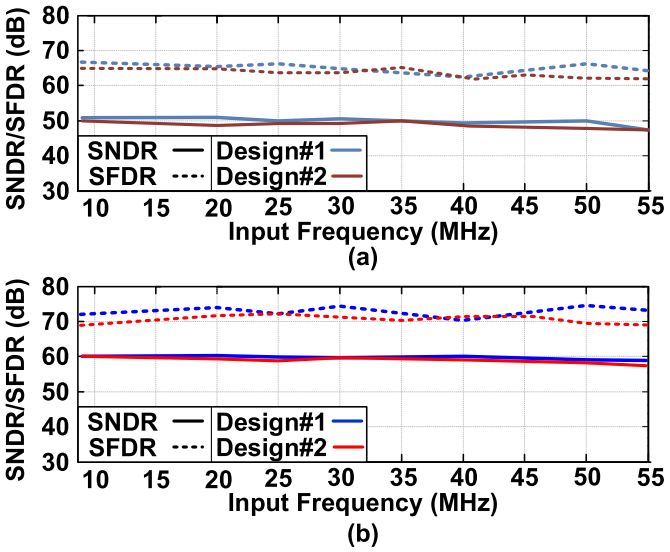

Fig. 16. Sweep around input frequency of designs #1 and #2. (a) Before calibration. (b) After calibration.

and V_{dn} over the correction range, we can trim them according to the mean code difference between the normal and the threshold configured mode of the ADC's output but this is not necessary in our design. Fig. 16 shows the measured dynamic performance across different input frequencies. The SNDR remained around 59 dB until the Nyquist input in both designs. Table II summarizes and compares the overall measured performance with state-of-the-art SAR ADCs at the similar performance. The total power consumption is 1.6 and 2.44 mW at 100 MS/s from a 1.2-V supply in design #1 and #2, respectively. This paper shows a competitive FoM when compared with others in the same technology. While the decoupling capacitor or buffer for the reference voltages is included on-chip, the active area is still kept small.

VIII. CONCLUSION

A reference error calibration has been proposed in this paper for high-speed and high-resolution SAR ADC. Results indicate that the presented scheme can greatly relax the stringent requirements of reference generation in SA operation which has been revealed as a steep tradeoff on either the area or power consumption. Thanks to the calibration, the adopted decoupling capacitor is small and the power consumption of the reference buffer is low. The calibration scheme also has a small hardware overhead and is able to enhance the dynamic range of the ADC. The calibration can be simply embedded in the SA operation and the correction is performed in the digital domain. The measured results of two prototypes demonstrate that the SNDR can be improved at least by 9 dB in an 11-b SAR ADC with only a 3-pF on-chip decoupling capacitor as reference or 0.84-mW power reference buffer.

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Chi-Hang Chan (S'12–M'15) was born in Macau, China, in 1985. He received the B.S. degree in electrical engineering from the University of Washington, Seattle, WA, USA, in 2008, the M.S. and Ph.D. degrees from the University of Macau, Macao, China, in 2012 and 2015, respectively.

He was an Intern with Chipidea Microelectronics (Now Synopsys), Macao. He is currently an Assistant Professor in electrical engineering with the University of Macau, Macao. His current research interests include Nyquist ADC, mixed signal circuits, comparator offset calibration, flash, and multi-bit SAR ADC.

Dr. Chan was a recipient of the Chipidea Microelectronics Prize and Macau Science and Technology Development Fund (FDCT) Postgraduates Award (Master Level) in 2012 and 2011, respectively, the Macau FDCT Award for Technological Invention (2nd class) and the Macao Scientific and Technological Research and Development Postgraduates Award (Ph.D. Level) in 2014 for outstanding Academic and Research achievements in Microelectronics, and the 2015 Solid-State Circuit Society Pre-Doctoral Achievement Award. He was also a co-recipient of the 2011 ISSCC Silk Road Award and Student Design Contest Award in A-SSCC 2011.

Yan Zhu (S'10–M'12) received the B.Sc. degree in electrical engineering and automation from Shanghai University, Shanghai, China, in 2006, and the M.Sc. and Ph.D. degrees in electrical and electronics engineering from the University of Macau, Macao, China, in 2009 and 2011, respectively.

She is currently an Assistant Professor with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao. She has involved in more than 15 research projects for low-power and high-performance ADC. She has authored or co-authored more than 30 papers in technical journals and conference papers in her field of interests, and holds four U.S. patents. Her current research interests include low-power and wideband high-speed Nyquist A/D converters as well as digitally assisted data converter designs.

Dr. Zhu received the Chipidea Microelectronics Prize and the Macao Scientific and Technological Research and Development Award—Postgraduate Level—in 2012 for outstanding Academic and Research achievements in Microelectronics, as well as the Student Design Contest Award in A-SSCC 2011. She is currently a technical program committee of Data Converter Sub-Committee of A-SSCC.

Cheng Li was born in Heyuan, China, in 1992. He received the B.Eng. degree in microelectronics from Sun Yat-Sen University, Guangzhou, China, in 2014. He is currently pursuing the M.Sc. degree with the University of Macau, Macao, China.

His current research interests include power management design for high-speed SAR ADC, especially in LDO and reference buffer.

Wai-Hong Zhang was born in Macau, China, in 1992. He received the B.S. degree in electrical and computer engineering from the University of Macau, Macao, in 2015, where he is currently pursuing the M.S. degree.

His current research interests include mixed analog/digital circuit designs, especially on low-power data converters.

Iok-Meng Ho received the B.Sc. degree in electrical and computer engineering from the University of Macau, Macao, China, in 2015, where he has been pursuing the M.Sc. degree since 2015, with a specialization in high-speed analog-to-digital converters.

Lai Wei received the B.Sc. degree in electrical and computer engineering from the University of Macau, Macao, China, in 2016, where she is currently pursuing the M.S. degree.

She is currently with the Research Group of the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao. Her current research interests include high-speed and high-resolution A/D converter designs.

Seng-Pan U (Ben) (S'94–M'00–SM'05–F'16) received the B.Sc. and M.Sc. degrees in 1991 and 1997, respectively, and the dual Ph.D. (Hons.) degrees from the University of Macau, (UM) and the Instituto Superior Técnico (IST), Lisbon, Portugal, in 2002 and 2004, respectively.

From 1999 to 2001, he was on leave from the Center of Microsystems in IST, as a Visiting Research Fellow. He has been with Faculty of Science and Technology, UM, Macao, since 1994, where he is currently a Professor and Deputy Director of the State Key Laboratory of Analog and Mixed-Signal VLSI. In 2001, he co-founded the Chipidea Microelectronics Ltd., Macau, as the Engineering Director, and later the Corporate VP-IP Operations Asia Pacific devoting to advanced AMS Semiconductor IP product development. The company was acquired in 2009 by the world leading EDA and IP provider Synopsys Inc. (NASDAQ: SNPS), and currently as Synopsys Macau Ltd, where he is also the Corporate Research and Development Director and Site General Manager. He has co-authored about 200 publications, four books (Springer and China Science Press) in the area of VHF SC filters, analog baseband for multi-standard wireless transceivers, and very high-speed TI ADCs. He co-holds 14 U.S. patents.

Prof. U was a member of the Science and Technology (S and T) Commission of China Ministry of Education and also S and T Committee of Macau. He is the Honorary Chairman of the IEEE SSCS (as founder), and the CAS/COMM Macau chapter. He was a recipient of 30+ research and academic/teaching awards and a co-recipient of the 2014 ESSCIRC Best Paper Award. He is also the Advisor for 30+ student research award recipients; the awards include the SSCS Pre-Doctoral Achievement Award, the ISSCC Silk-Road Award, the A-SSCC Student Design Contest Award, the IEEE DAC/ISSCC Student Design Contest Award, the ISCAS Award, the MWSCAS Award, and the PRIME award. As the Macau founding Chairman, he was a recipient the 2012 IEEE SSCS Outstanding Chapter Award. Both at the 1st time from Macau, he received the Science and Technology Innovation Award of Ho Leung Ho Lee Foundation in 2010, and also the National State S and T Progress Award in 2011. He was a recipient of both the 2012, 2014, and 2016 Macau S and T Invention Award and Progress Award. In recognition of his contribution in Academic Research and Industrial Development, he was awarded by Macau SAR government the Honorary Title of Value in 2010. He was also elected as the "Scientific Chinese of the Year 2012." He was the IEEE SSCS Distinguished Lecturer from 2014 to 2015 and the A-SSCC 2013 and will be the ISSCC 2018 Tutorial Speaker. He has also been on the technical review committee of various IEEE journals and the program committee/chair of the IEEJ AVLSIWS, the IEEE APCCAS, the ICICS, the PRIME Asia, and the IEEE ASP-DAC'16. He is currently technical program committee of ISSCC, the Data Converter Sub-Committee Chair of A-SSCC, and the Analog Sub-Committee Chair of VLSI-DAT and an Editorial Board Member of the *Analog Integrated Circuits and Signal Processing.*

Rui Paulo Martins (M'88–SM'99–F'08) born in 1957, received the bachelor's (5-years), master's, and Ph.D. degrees, as well as the Habilitation for Full-Professor in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively.

He has been with the Department of Electrical and Computer Engineering, IST, Lisbon, since 1980. He is with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau, Macao, China, since 1992, where he became a Chair-Professor in 2013. In FST, he was the Dean of the Faculty from 1994 to 1997 and has been the Vice-Rector of the UM since 1997. From 2008, after the reform of the UM Charter, he was nominated after open international recruitment, and reappointed (in 2013), as Vice-Rector (Research) until, 2018. Within the scope of his teaching and research activities, he has taught 21 bachelor and master courses and, in UM, has supervised or co-supervised 40 theses—Ph.D. (19) and Masters (21). He has co-authored six books and 12 book chapters; 25 Patents, U.S.A (23) and Taiwan (2); 400 papers, in scientific journals (126) and in conference proceedings (274); as well as other 62 academic works, in a total of 505 publications. He was a Co-Founder of Chipidea Microelectronics (Macao) [now Synopsys] from 2001 to 2002, and created, in 2003, the State Key Laboratory of Analog and Mixed-Signal VLSI of UM, elevated in January 2011 to State Key Laboratory of China (the 1st in Engineering in Macao), being its Founding Director.

Prof. Martins was a member of the IEEE CASS Fellow Evaluation Committee from 2013 to 2014, and a Nominations Committee Member of IEEE CASS in 2016. He was the Founding Chairman of both IEEE Macau Section from 2003 to 2005 and the IEEE Macau Joint-Chapter on Circuits and Systems (CAS) / Communications (COM) from 2005 to 2008 [*2009* World Chapter of the Year of IEEE CAS Society (CASS)]. He was the General Chair of the 2008 IEEE Asia-Pacific Conference on CAS –APCCAS' 2008, and was the Vice President for Region 10 (Asia, Australia, and the Pacific) of IEEE CASS from 2009 to 2011. He was the Vice President (World) Regional Activities and Membership of IEEE CASS from 2012 to 2013. He was the CAS Society Representative in the Nominating Committee, for the election in 2014, of the Division I (CASS/EDS/SSCS)–Director of the IEEE. He was the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference–ASP-DAC' 2016. He is currently the Chair of the IEEE CASS Fellow Evaluation Committee (Class 2018). He was a recipient of the IEEE Council on Electronic Design Automation Outstanding Service Award 2016 and the two government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999, and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001. In 2010, He was elected, unanimously, as Corresponding Member of the Portuguese Academy of Sciences (in Lisbon), being the only Portuguese Academician living in Asia. He was an Associate Editor of the IEEE TRANSACTIONS ON CAS II: EXPRESS BRIEFS from 2010 to 2013, and was nominated the Best Associate Editor of the T-CAS II for 2012 and 2013.