

High-Breakdown, High- f_{\max} Multiport Stacked-Transistor Topologies for the W-Band Power Amplifiers

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Abstract—Effect of silicon technology limitations, including transistor nonidealities, layout parasitics, and low-quality factor on-chip passive components on millimeter wave stacked switching power amplifiers operating at the W-band frequencies (75–110 GHz), is presented in this paper. To mitigate the performance degradation in output power and PAE arising from such causes, high-breakdown voltage, high- f_{\max} multiport stacked-transistor topologies are proposed for realizing power amplifiers with high output power and high efficiency at 75–110 GHz. A 90-nm silicon germanium (SiGe) BiCMOS process is used to propose active structures comprising of two and three stacked transistors with integrated layout parasitics that achieve f_{\max} and breakdown voltage of 295 GHz and 8 V and 260 GHz and 11 V, respectively. Functionality of such multiport transistor topologies is demonstrated in proof-of-concept implementations, including a five-stage two-stacked switching power amplifier (PA) that achieves peak output power and PAE of 22 dBm and 19% at 85 GHz, and a six-stage three-stacked PA that achieves peak output power and PAE of 23.3 dBm and 17% at 83 GHz, respectively. For comparison with conventional switching PA designs using native transistor footprints, a five-stage W-band nonstacked Class-E amplifiers is also fabricated in the same 90-nm SiGe BiCMOS process with output power and PAE of 19.5 dBm and 16% at 88 GHz. The superior performance of output power and PAE in designs using the multiport transistor topologies highlights the benefit of the proposed approach.

Index Terms—Class-E, HBT, millimeter wave (mm-wave), power amplifier (PA), silicon germanium (SiGe), transmitter.

I. INTRODUCTION

THE W-band frequency spectrum (75–110 GHz) is used for various applications, such as wireless back haul (71–76 and 81–86 GHz), automotive radars (77–78 GHz), and possibly 5G communications. Most millimeter wave (mm-wave) communication links envision a large-scaled phased-array system to achieve highly directed beam with high Equivalent Isotropically Radiated Power (EIRP), necessitating silicon integration of the entire mm-wave transceiver chain.

One such hypothetical system is highlighted in Fig. 1, comprising of a 128-element Tx–Rx phased-array transceiver

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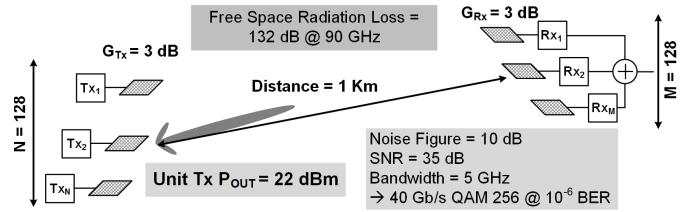


Fig. 1. Phased-array W-band transceiver architecture.

supporting 40-Gb/s data-rate using 256 QAM constellation over 5-GHz channel bandwidth around 90-GHz carrier frequency. It can be shown [1], that to achieve a bit error rate less than 10^{-6} over a line of sight distance of 1 km, the required receiver SNR is 35 dB while the output power requirement from each element of the phased-array transmitter exceeds 22 dBm. The total system dc power consumption of the transceiver chain is thus dominated by the front-end PA performance.

The high peak-to-average power ratio of complex amplitude and phase modulated signals, such as 256 QAM that are used to increase the data rate for a given channel bandwidth, necessitates using linear power amplifiers with low efficiency. Switching power amplifiers, such as Class-E amplifier, while efficient, cannot support amplitude modulated waveforms. An array of switching amplifiers may be used in a digital polar transmitter architecture to support amplitude as well as phase modulated waveforms. In such a scheme, the number of switching power amplifiers that are turned on and contribute to the output depends on the instantaneous desired amplitude level. Efficient mm-wave digital PA using a power-combined array of eight Class-E stacked silicon germanium (SiGe) HBTs has been reported [7], [9].

Modern scaled silicon CMOS or SiGe technologies with f_T , $f_{\max} > 300$ GHz, are limited by low-breakdown voltages. As such, silicon W-band transmitters implemented in scaled CMOS Silicon on Insulator (SOI) or bulk SiGe BiCMOS process are limited to < 50-mW output power generation [2], [4]. For applications requiring higher output power at mm-wave frequencies, two approaches, namely, power combining and transistor stacking have been used in silicon technologies. On-chip [3], [5] or spatial [2] power combining may be used to increase the total output power mm-wave PA modules. Transistor stacking enables higher voltage swing, and hence higher output power, across a given load [6], [22], [25]. A comparison between these two approaches for efficient power generation

at mm-wave frequencies is offered in [9]. Previous works have demonstrated efficient, small-scale (2:1 and 4:1) power combining in small form factors [3]. However, to achieve Watt-level output power, using nonstacked low voltage silicon transistors necessitates large-scale (e.g., 16:1) power combiners. For the metal stacks available in planar silicon technologies, the insertion loss of a typical on-chip transmission line at the W-band frequencies approaches ≈ 1 dB/mm [9]. For large-scale power combining, using either an N-way $\lambda/4$ power combining or N-stage corporate combiner architecture, the total combiner loss can exceed 3 dBm [9]. On the other hand, while moderate amount of transistor stacking enables output power scaling with minimum efficiency degradation, large-scale transistor stacking at mm-wave frequencies suffers from efficiency degradation and nonoptimal power scaling due to layout and transistor parasitics [6]. As such, realization of mm-wave stacked PA architectures requires special layout topologies as discussed in [24] for CMOS FETs and in [23] for SiGe HBTs. Efficient stacked PA modules with 22–23-dBm output power can then use area-efficient small-scale power combiners to achieve Watt-level output power with high overall system efficiency. This hybrid approach of transistor stacking and power combining was demonstrated in [9] for Q-band implementations. This paper covers a layout parasitic aware design methodology for efficient >22-dBm W-band SiGe stacked power amplifiers, which can then be used in similar hybrid solutions for efficient Watt-level power generation at the W-band frequencies.

Section II proposes design methodologies for linear and switching amplifiers that maximize the current density-dependent breakdown voltage of SiGe HBTs to achieve best performance (P_{out} , G_P , and PAE) at the W-band frequencies. Section III discusses transistor stacking in silicon power amplifiers and effects of layout parasitics and transistor nonidealities of such stacked architectures on PA performance at the W-band. To mitigate the drawbacks of conventional stacked PA designs with discrete transistor layouts at the W-band frequencies, a multiport composite stacked-transistor topology has been proposed in Section IV. These multiport composite transistor topologies have been used to showcase the W-band linear and switching PA design examples in Section V. Experimental results for proof-of-concept fabricated prototypes are covered in Section VI. Section VII concludes this paper.

II. MAXIMIZATION OF BREAKDOWN VOLTAGE IN SiGe HBT POWER AMPLIFIERS

Transistor scaling improves the speed at the cost of lower transistor breakdown voltage as predicted by the so-called “Johnson Limit” [8]. In recent years, series stacking of transistors has been proposed for both linear [22] and switching amplifiers [6] to ameliorate the low-breakdown voltage of silicon transistors. However, as will be highlighted in Section III, transistor stacking comes with its own associated challenges and drawbacks especially at the higher W-band frequencies. More fundamentally, at the transistor level, especially in SiGe HBTs, the voltage and current waveforms play a critical role in determining the effective transistor breakdown voltage.

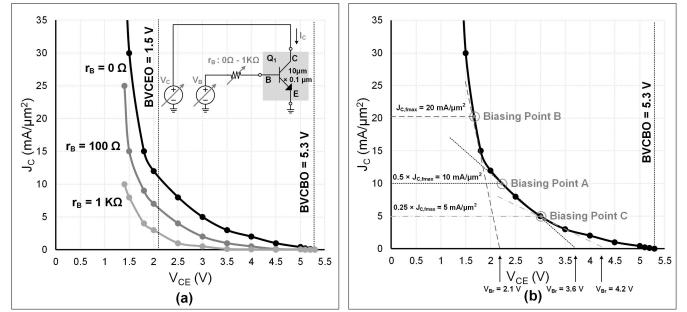


Fig. 2. (a) Breakdown voltage (BV) versus collector current density (J_C) for the 90-nm SiGe HBTs for different base resistance (r_B) terminations. (b) SiGe HBT effective breakdown voltage (V_{Br}) under Class-A amplifier load line: maximum collector voltage swing in SiGe HBT Class-A amplifiers can be higher than $BV_{CEO} = 1.5 \text{ V}$ depending on dc bias point.

Understanding and exploiting these transistor characteristics is very beneficial for efficient power amplifiers at mm-wave frequencies.

The effective breakdown voltage of SiGe HBTs is a strong function of collector current density (J_C) and base impedance (r_B) termination [19], [20]. For the 90-nm SiGe BiCMOS process under consideration in this paper, the effective breakdown voltage of the SiGe HBTs under different collector current densities and different base impedance terminations (r_B) can be obtained from the circuit simulation setup, as shown in Fig. 2(a). It can be observed from Fig. 2(a) that for the 90-nm SiGe BiCMOS process, while for $J_C > 30 \text{ mA}/\mu\text{m}^2$, V_{CE} must remain $BV_{CEO} = 1.5 \text{ V}$, for low J_C with low r_B , V_{CE} can reach as high as $BV_{CBO} = 5.3 \text{ V}$. This unique property of bipolar transistors can be leveraged especially for PA designs at mm-wave frequencies. The three times improvement in breakdown voltage enables significant improvement in power generation capability from the scaled SiGe processes at mm-waves, mitigating need for large-scale power combining or impedance transformation for efficient high power generation. The technology parameters of some modern SiGe processes are shown in Table I [6] and will be useful in evaluating mm-wave linear and switching amplifier performance metrics Section IIa, IIb and Section III. The input time constant τ_{in} is defined as $r_B \times C_{\text{in}}$, where r_B is the base resistance and C_{in} is the total input (base) capacitance. Time constant τ_{out} is defined as $r_{\text{ON}} \times C_{\text{OFF}}$ and corresponds to the transistor output (collector), when the transistor operates in the switching mode.

A. Linear Class-A Power Amplifier Operation at the W-Band

Linear PA designs have been extensively studied in the literature [21]; but, such designs typically assume a fixed transistor breakdown voltage irrespective of the instantaneous current density. However, in SiGe HBTs, since the effective breakdown voltage can vary between $BV_{CEO} = 1.5 \text{ V}$ and $BV_{CBO} = 5.3 \text{ V}$, the linear amplifier load lines and supply voltages can be optimally chosen to benefit from the collector voltage swing maximization. At mm-wave frequencies, the performance metrics of linear Class-A amplifiers in terms of

TABLE I
TECHNOLOGY PARAMETERS FOR SELECTED SiGe HBT PROCESSES

Technology	HBT	BV_{CEO} (V)	BV_{CBO} (V)	V_K (V)	Peak f_T (GHz)	$J_{C,\text{ff}}$ (mA/ μm^2)	Peak f_{max} (GHz)	$J_{C,\text{fmax}}$ (mA/ μm^2)	T_{in} (ps)	T_{out} (ps)	C_{in} (pF/ μm^2)	C_{OFF} (fF/ μm^2)	α ($C_{\text{in}} / C_{\text{OFF}}$)	$I_{\text{dc},Q}$ (mA/ μm^2) ($V_B = 0.75$ V)
0.25 μm 7WL	High f_T	3.3	11	0.8	60	3.5	100	3.5	22	0.53	0.68	4	172	0.035
0.13 μm 8HP	High f_T	1.7	5.9	0.6	220	14	280	12.5	8	0.22	0.325	9.76	33.3	0.07
	High BV	3.55	12	0.8	60	1.4	120	1.2	18	1.6	0.68	9.76	69	0.035
90 nm 9HP	High f_T	1.5	5.3	0.3	300	20	350	20	5	0.1	0.4	17	33.3	0.22

technology parameters (Table I) can be summarized as

$$\begin{cases} P_{\text{out},\text{max}} = \frac{1}{2} \frac{(V_{\text{CC}} - V_K)^2}{R_{\text{Load}}} = \frac{1}{8} \frac{V_{\text{Br}}^2}{R_{\text{Load}}} \\ G_P,\text{max} = \frac{P_{\text{out}}}{P_{\text{in}}} = \epsilon \times \left(\frac{\omega}{\omega_{\text{max}}} \right)^2 = \epsilon \times U \\ \eta_{\text{max}} = \frac{1}{2} \left(1 - \frac{V_K}{V_{\text{CC}}} \right) = \frac{1}{2} \left(\frac{V_{\text{Br}} - V_K}{V_{\text{Br}} + V_K} \right) \\ \text{PAE}_{\text{max}} = \eta_{\text{max}} \times \left(1 - \frac{1}{G_P,\text{max}} \right) \end{cases} \quad (1)$$

where V_{CC} is the collector dc supply voltage, V_{Br} is the transistor maximum breakdown voltage, V_K is the transistor knee voltage, R_{Load} is the resistance seen at the collector, ω is the frequency of operation, ω_{max} is the transistor unity-gain frequency, and U is Mason's invariant gain. The supply voltage V_{CC} is determined from breakdown voltage and knee voltage as

$$V_{\text{CC}} = \frac{1}{2}(V_{\text{Br}} + V_K). \quad (2)$$

In order to achieve maximum efficiency of (1), the load resistance R_{Load} must also satisfy

$$R_{\text{Load}} = \frac{V_{\text{CC}} - V_K}{I_{\text{dc},Q}} = \frac{1}{2} \frac{V_{\text{Br}} - V_K}{I_{\text{dc},Q}} \quad (3)$$

where $I_{\text{dc},Q}$ is the collector dc quiescent current. Parameters ϵ in G_P,max expression are introduced to model the gain degradation that happens when R_{Load} is chosen for efficiency maximization rather than gain maximization [21]. For ϵ varying between 0.5 and 0.8, the power gain degrades by 1–3 dB from the theoretical value predicted by Mason's invariant gain U .

It is evident from (1), that maximizing V_{Br} improves both output power P_{out} and efficiency η . Choosing a low base impedance $r_B = 0$ enables the effective V_{Br} to move along J_C versus V_{Br} contour, as shown in Fig. 2(a). But, V_{Br} maximization under a Class-A linear load line also depends on the quiescent current density $J_{C,Q}$, as shown in Fig. 2(b). To maximize power gain G_P and PAE, the current density in the SiGe HBTs during the maximum current swing $I_{C,\text{max}}$ must be $J_{C,\text{fmax}} = 20$ mA/ μm^2 for the 90-nm SiGe process (Table I). Since $I_{C,\text{max}} = 2 \times I_{\text{dc},Q}$, this determines the dc quiescent current density for $J_{C,Q} = 0.5 \times J_{C,\text{fmax}} = 10$ mA/ μm^2 (Biasing Point A) and fix $V_{\text{Br}} = 3.6$ V under a tangential Class-A load line, as shown in Fig. 2(b). A higher $J_{C,Q}$ biasing point (Biasing Point B) will result in lower effective breakdown voltage ($V_{\text{Br}} = 2.1$ V), while a higher

effective breakdown voltage $V_{\text{Br}} = 4.2$ V can be obtained at the Biasing Point C in Fig. 2(b) at the cost of suboptimal $J_{C,Q}$ and thus lower power gain.

For a specified P_{out} , V_{Br} obtained from Fig. 2(b) for the optimum $J_{C,Q}$ (Biasing Point A) sets the Class-A load line R_{Load} . Values of R_{Load} and V_{Br} , and the frequency of operation ω in turn determine power gain G_P , efficiency η and PAE from (1) and technology parameters from Table I. The dc quiescent current $I_{\text{dc},Q}$ can be determined from (3). The total dc quiescent current $I_{\text{dc},Q}$ and the $J_{C,Q}$ current density (Bias Point A) then fix the SiGe HBT size. For the chosen SiGe HBT transistor size, the total parasitic output capacitor C_{OFF} (obtained from Table I) can be significant at mm-wave frequencies. This collector-bulk capacitance, OFF capacitance C_{OFF} , is now resonated out by the collector inductance given $L_1 = 1/\omega^2 C_{\text{OFF}}$. All the design parameters for a linear Class-A power amplifier, as shown in Fig. 3(a), operating at a certain frequency ω to generate a specified P_{out} are now fixed.

To validate the above mentioned design procedure, the design of a linear Class-A PA with $P_{\text{out}} = 17.5$ dBm at 90 GHz is shown in Fig. 3. For $V_{\text{Br}} = 3.6$ V (determined from $J_{C,\text{max}}$ as discussed before), $R_{\text{Load}} = 25$ Ω shall be chosen for $P_{\text{out}} = 17.5$ dBm. This requires a 6×0.1 $\mu\text{m} \times 10$ μm HBT transistor. This R_{Load} value does not require significant impedance transformation that degrades the efficiency due to finite loss of passive components. The design steps to maximize V_{Br} in a SiGe HBT Class-A PA and thus obtain a specified P_{out} with maximum PAE are summarized in Fig. 3(b). Transient collector voltage and current waveforms in Fig. 3(c), collector voltage-current contour in Fig. 3(d), and performance summary table (assuming ideal lossless passives) in Fig. 3(e) validate the analytical results when compared with simulations. The significance of the aforementioned approach is the ability to extract more power from Class-A SiGe HBT amplifiers when considering the safe operating region (and not merely BV_{CEO}) in the design.

B. Switching Class-E Power Amplifier Operation at the W-Band

Switching power amplifiers at mm-wave frequencies have been demonstrated in both CMOS and SiGe HBT technologies [11], [12]. The main advantage of switching amplifiers is the higher achievable collector efficiency due to nonoverlapping collector voltage and current waveforms. However, the same nonoverlapping of voltage and current waveforms feature also enables the switching amplifiers in SiGe HBTs

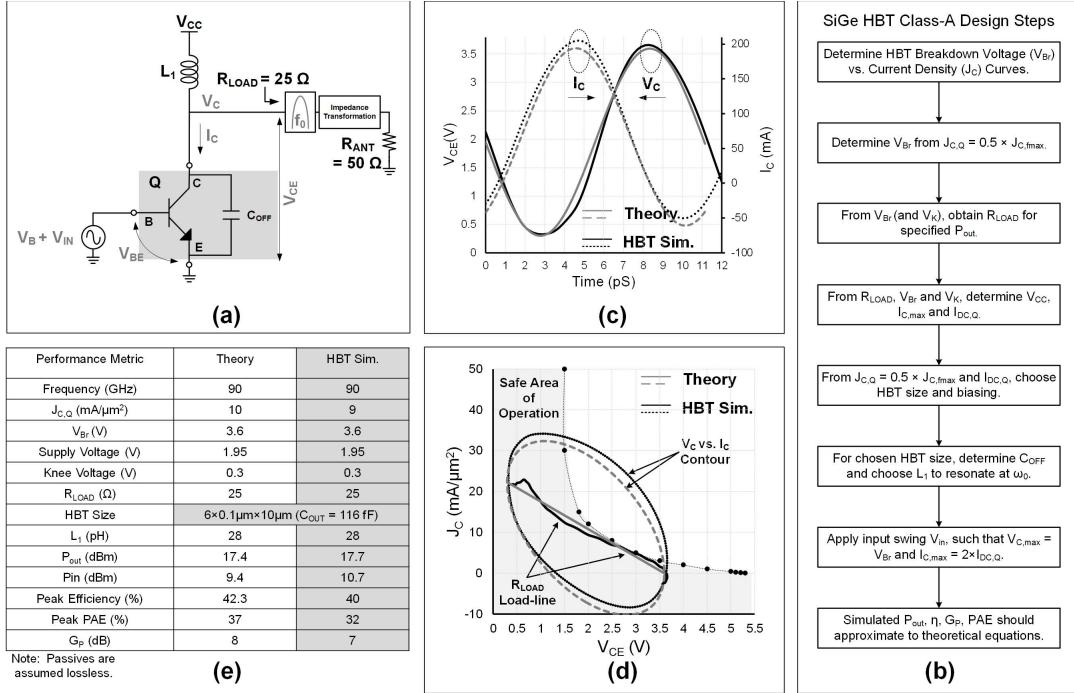


Fig. 3. 90-nm SiGe HBT Class-A amplifier at 90 GHz. (a) Schematic. (b) Design steps in a SiGe HBT process for mm-wave Class-A amplifiers. (c) Collector voltage and current transient waveforms. (d) Collector voltage–current density contour showing the SiGe HBT stays within the “Safe Area of Operation” while still swinging up to $V_{Br} = 3.6$ V ($BV_{CEO} = 1.5$ V). (e) Performance metrics.

to achieve higher collector voltage swing by exploiting the SiGe HBT breakdown curves of Fig. 2(a). In contrast to linear power amplifiers, the maximum transistor breakdown voltage (V_{Br}) in switching power amplifiers can always be as high as BV_{CBO} [6]. Thus, switching amplifiers can achieve high output power while maintaining high efficiency at mm-waves. The design procedure for mm-wave SiGe HBT Class-E power amplifiers has been extensively analyzed in [6]. In this paper, the design methodology for Class-E amplifier design at mm-wave frequencies in the 90-nm SiGe process is summarized in Fig. 4(b).

To verify that the Class-E switching amplifier waveforms can be obtained at the *W*-band frequencies in the 90-nm SiGe HBT process, a 90-GHz Class-E PA with $P_{out} = 20$ dBm is designed and simulated (Fig. 4) with $R_{Load} = 25 \Omega$. At the *W*-band frequencies, the simulated collector voltage and the collector current waveforms, as shown in Fig. 4(c), can only support the first three harmonics; but, they compare well with the theoretical Class-E waveforms [10]. The simulated Class-E voltage–current contour at 90 GHz shown in Fig. 4(d) also compares favorably with the theory. Estimate of Class-E performance based on technology parameters has been extensively covered in [6] and matches well with the simulated values (assuming lossless passives) in the performance table of Fig. 4(e).

The purpose of the aforementioned discussions was to highlight that the SiGe HBT breakdown voltage curves can be leveraged for output power and efficiency improvement in both linear as well as switching power amplifiers at mm-wave frequencies. As evident from the two design examples, switching amplifiers even at 90 GHz achieve better performance for the

same output power compared with linear Class-A amplifiers in the 90-nm SiGe process.

However, in both the cases, the maximum voltage swing is still limited to $BV_{CBO} = 5.3$ V and further circuit techniques need to be applied to increase the effective breakdown voltage V_{Br} even higher to generate >22 -dBm output power without any power combining at mm-wave frequencies.

III. TRANSISTOR STACKING IN THE W-BAND POWER AMPLIFIERS

Series stacking of transistors in which the overall collector voltage swing is divided amongst the stacked transistors have become popular to support larger voltage swing and higher output power [17], [18]. Transistor stacking in CMOS technologies at mm-wave frequencies has been reported for both linear amplifiers [13]–[15] as well as switching amplifiers [11], [16]. The principle of transistor stacking has also been applied to realize SiGe HBT stacked Class-E amplifiers [6]. Series stacking in SiGe HBT technologies can benefit from additive scaling of breakdown voltage of each stacked transistor while still leveraging the SiGe HBT breakdown voltage curves of Section II for each individual stacked transistor. Thus, compared with a nonstacked SiGe HBT with maximum voltage swing of $BV_{CBO} = 5.3$ V in the 90-nm SiGe process, a stacked PA design with two series-stacked SiGe HBTs can sustain maximum collector voltage swing >8 V (ideally 2×5.3 V = 10.6 V) and generate $P_{out} > 22$ dBm across 50Ω without impedance transformation.

Operation principle and design guidelines for stacked transistors at mm-wave frequencies in the context of switching

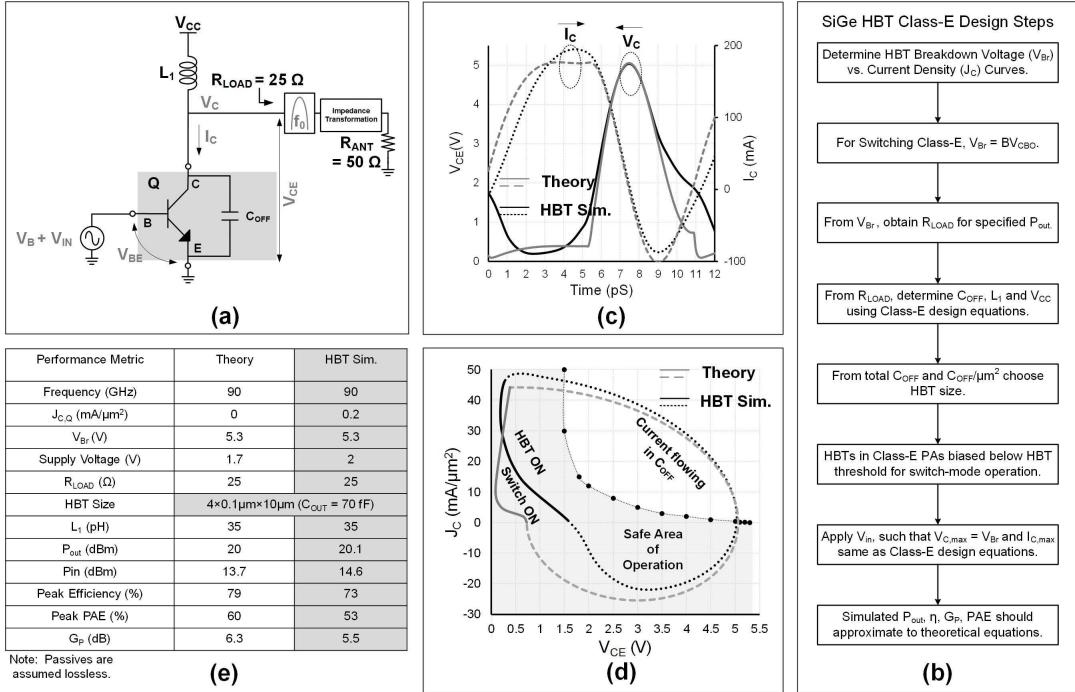


Fig. 4. 90-nm SiGe HBT Class-E amplifier at 90 GHz. (a) Schematic. (b) Design steps in a SiGe HBT process for mm-wave Class-E amplifiers. (c) Collector voltage and current transient waveforms. (d) Collector voltage-current density contour showing the SiGe HBT stays within the ‘Safe Area of Operation’ while still swinging up to $V_{Br} = BV_{CBO} = 5.3$ V. (e) Performance metrics.

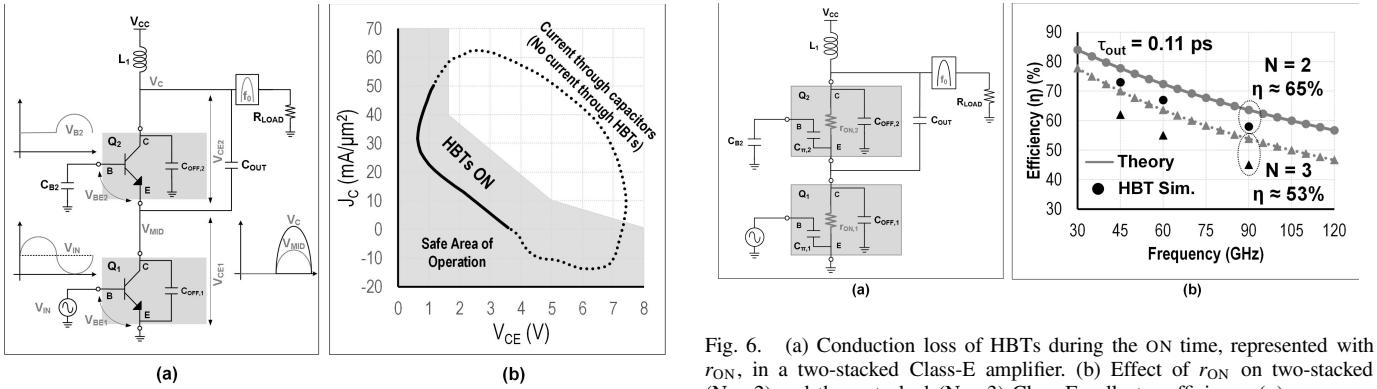


Fig. 5. Transistor stacking at the W-band. (a) Two-stacked Class-E schematic. (b) Class-E voltage-current density contour for safe operation at 90 GHz.

amplifiers have been discussed before [6] and are only briefly summarized here. For mm-wave switching Class-E power amplifiers, the stacked-transistor configuration of Fig. 5(a) consists of SiGe HBT transistors that are connected in series with appropriately chosen capacitors values C_{OUT} and C_{B2} . During large-signal switching mode operation, the intrinsic HBT parasitics in conjunction with the added capacitors ensure that each transistor operates within the 5.3-V BV_{CBO} breakdown limit while resulting in an increase of the overall breakdown voltage of the stacked-transistor configuration [Fig. 5(b)]. For simplicity, the collector-bulk capacitors C_{CB} are denoted as C_{OFF} and the base-emitter capacitors C_{BE} are denoted as C_π in Fig. 6(a). The capacitor network $C_{OUT} - C_{OFF,1}$ ensures that the collector voltage V_C is equally

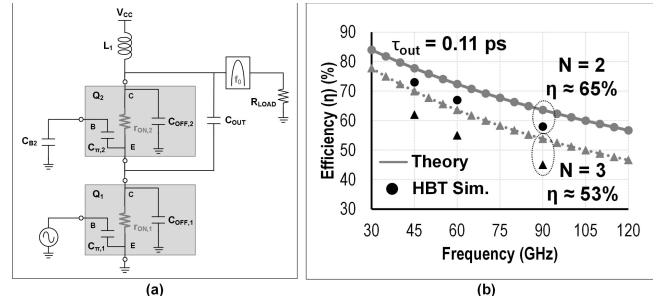


Fig. 6. (a) Conduction loss of HBTs during the ON time, represented with r_{ON} , in a two-stacked Class-E amplifier. (b) Effect of r_{ON} on two-stacked ($N = 2$) and three-stacked ($N = 3$) Class-E collector efficiency (η).

divided between the top and bottom HBTs $Q_1 - Q_2$, while the $C_{B2} - C_{\pi 2}$ network ensures that the base-emitter voltage V_{BE2} of the stacked HBT Q_2 swings in synchrony with the base-emitter voltage V_{BE1} of the bottom HBT Q_1 . For mm-wave linear stacked amplifiers, the circuit configuration remains identical to Fig. 5, with the only difference being the maximum allowable collector-emitter voltage swing V_{CE} dependent on the load line and biasing conditions as was discussed in Section II-A.

The benefits of transistor stacking in PA designs at lower mm-wave frequencies have been demonstrated in CMOS SOI and SiGe HBT technologies [12], [13]. However, at higher W-band frequencies where transistor layout parasitics can become as significant as the discrete passive components, the benefits of transistor stacking needs to be revisited. Layout of series stacked-transistors comprises of many more metal

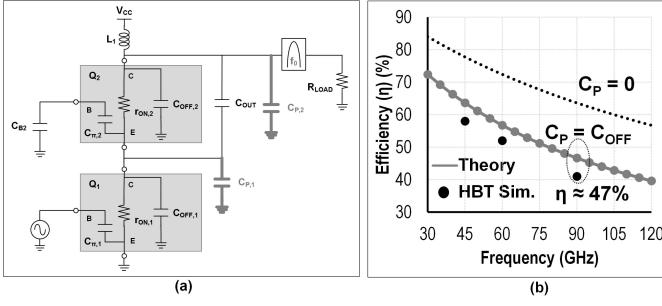


Fig. 7. (a) Parasitic layout capacitor C_P in a two-stacked Class-E amplifier. (b) Effect of C_P on collector efficiency (η) in a two-stacked amplifier.

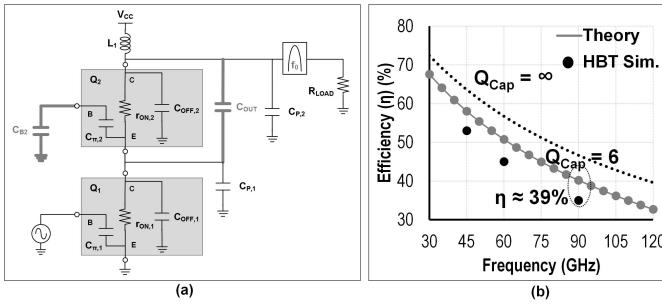


Fig. 8. (a) Output network capacitor C_{OUT} in a two-stacked Class-E amplifier. (b) Effect of C_{OUT} quality factor on collector efficiency (η) in a two-stacked amplifier.

interconnections with many sensitive intermediate nodes. As such, layout approaches followed in lower frequency stacked amplifier implementations, in which the transistors and the necessary passive components are treated separately, will significantly affect performance at the higher W-band frequencies [23]. The effect of various transistors and layout nonidealities on the W-band stacked switching power amplifier (PA) performance is discussed next.

A. Effect of Series Switches

The increased output power in stacked Class-E designs comes at the cost of reduced collector efficiency. In a stacked Class-E design, when multiple switches are placed in series, the switch ON resistances add up leading to higher conduction loss, as shown in Fig. 6(a).

In a generalized “N” series-stacked PA configuration, assuming equally sized series transistors, the collector efficiency (η) as proposed in [6] can be generalized for N-stacked Class-E configuration as

$$\eta_{\max}^{N\text{-Stacked Class-E}} \approx \frac{1}{1 + 4.6 \times N \times \omega \times \tau_{\text{out}}} \quad (4)$$

where ω is the operational frequency in radians, $\tau_{\text{out}} = R_{\text{ON}} \times C_{\text{OFF}}$ is the HBT output time constant ($= 0.1$ ps for the 90-nm SiGe process) of Table I. At the higher W-band frequencies, this leads to low efficiency from stacked switching PAs. For a two-stacked design, assuming ideal passives for all the input and output matching networks, the theoretical collector efficiency degrades to 65% at 90 GHz from the ideal theoretical 100% value [Fig. 6(b)]. SiGe HBT designs

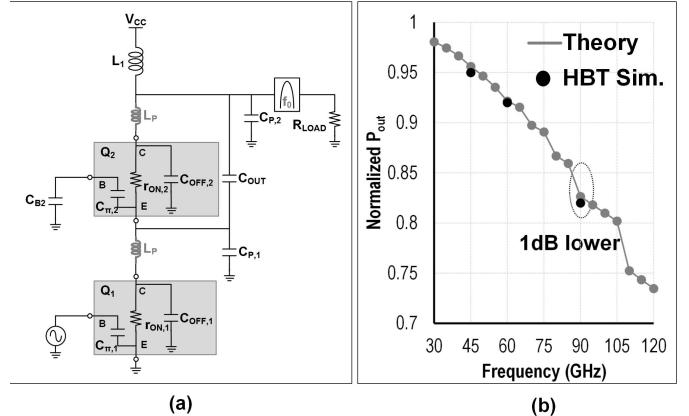


Fig. 9. (a) Parasitic collector inductance L_P in a two-stacked Class-E amplifier. (b) Effect of L_P on the output power of a two-stacked amplifier.

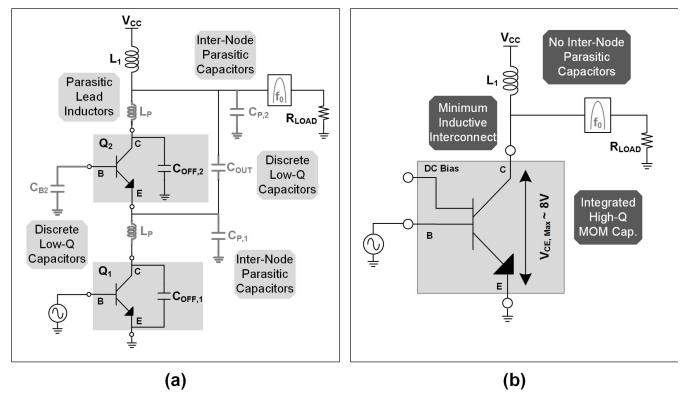


Fig. 10. (a) Parasitics associated with discrete transistor stacking at mm-wave frequencies. (b) Conceptual integrated multiport high-breakdown, high- f_{max} transistors.

at 45, 60, and 90 GHz assuming ideal passives are also shown in [Fig. 6(b)] and achieve a collector efficiency of 58%. The discrepancy between theoretical estimates and SiGe HBT design is mainly due to the unavailability of higher harmonics (> 3) of the mm-wave frequencies in the collector waveforms.

B. Effect of Parasitic Layout Capacitors

Metal interconnection of large power transistors in a stacked configuration can result in significant layout parasitic capacitors at mm-waves. As shown in Fig. 7(a), when the two discrete HBTs Q₁ and Q₂ are connected in series, the layout capacitors C_{P,1} and C_{P,2} result at each HBT collector terminal. These parasitic capacitors force a smaller transistor size to satisfy the desired Class-E capacitance budget C_{OFF}. This leads to higher conduction loss (higher r_{ON}) and lower collector efficiency.

The effect of layout parasitic capacitors from each collector node on the overall collector efficiency can be predicted by

$$\eta_{\max}^{N\text{-Stacked Class-E}} \approx \frac{1}{1 + 4.6 \times N \times \omega \times \tau_{\text{out}} \times \left(1 + \frac{C_P}{C_{\text{OFF}}}\right)} \quad (5)$$

where for simplicity, identical device sizes in the stacked configuration leading to $C_{\text{OFF},K} : K \in (1, N) = C_{\text{OFF}}$ and identical

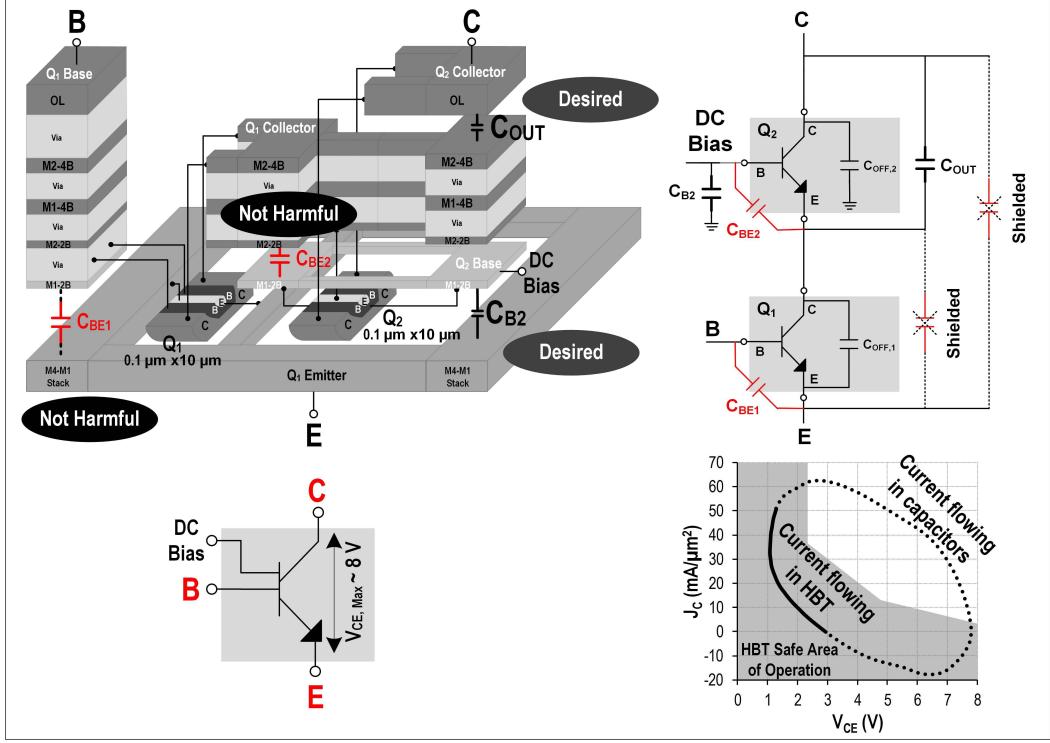


Fig. 11. Composite two-stacked multiport SiGe HBT layout.

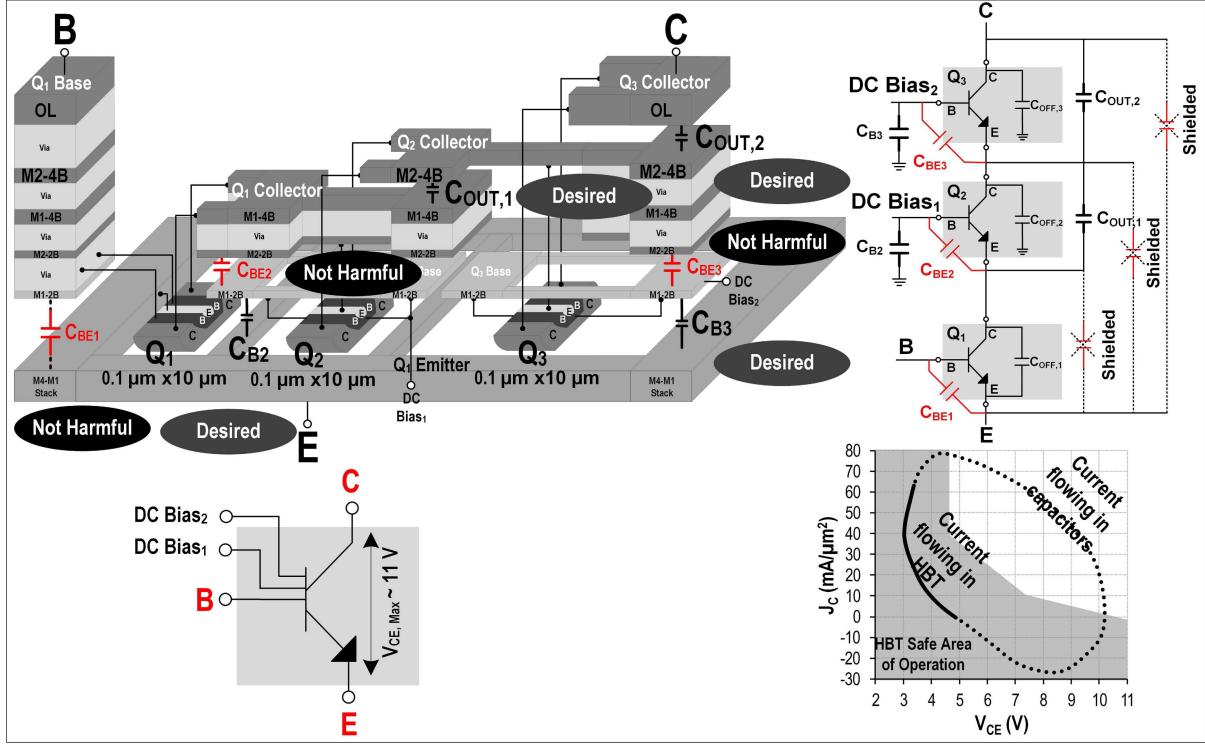


Fig. 12. Composite three-stacked multiport SiGe HBT layout.

parasitic capacitances at all intermediate nodes $C_{P,K : K \in (1,N)} = C_P$ are assumed. As the transistor output capacitance, C_{OFF} , that needs to be chosen for the W-band switching, PA implementations become smaller and

smaller at the higher mm-wave frequencies [6], the layout parasitic capacitors C_P become a significant proportion of the smaller device OFF capacitance C_{OFF} and lead to significant additional efficiency degradation. In an example where

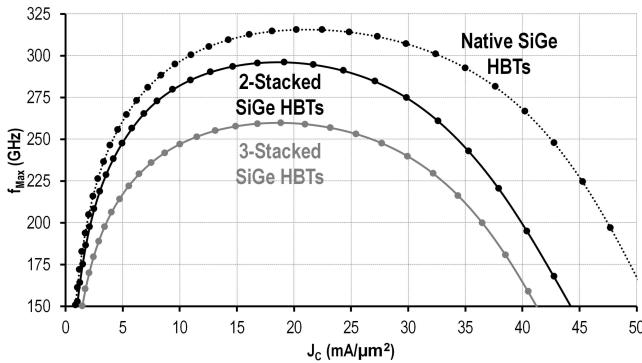


Fig. 13. f_{\max} versus current density J_c for nonstacked native SiGe HBTs, composite two-stacked and three-stacked HBTs.

$C_P = C_{OFF}$, the maximum achievable collector efficiency of a 90-GHz two-stacked Class-E amplifier drops from 65% to 47% [Fig. 7(b)]. The collector efficiencies achieved in the SiGe HBT designs on adding the parasitic C_P also correlate well the theoretical estimates.

C. Effect of Capacitor Q-Factor

In a stacked switching PA architecture, an output capacitor divider network shown as C_{OUT} in Fig. 8(a) ensures that the overall collector voltage swing can be divided between the top and bottom transistors. At lower mm-wave frequencies, this C_{OUT} can be implemented using discrete metal–insulator–metal (MIM) capacitors. At the W-band frequencies, however, the low Q of the MIM capacitors ($Q_{Cap} \approx 5\text{--}7$) results in significant efficiency degradation as seen from

$$\eta_{\max}^{N\text{-Stacked Class-}E} \approx \frac{1}{1 + 4.6 \times N \times \omega \times \tau_{out} \times \left(1 + \frac{C_P}{C_{OFF}}\right) + \frac{1.87}{Q_{Cap}}}. \quad (6)$$

Fig. 8(b) shows the efficiency degradation in a two-stacked Class-E amplifier. The SiGe HBT designs with finite Q of the C_{OUT} capacitor also shows similar performance degradation, as predicted by (6).

D. Effect of Parasitic Collector Inductance

Parasitic lead inductance L_P at each transistor collector node, as shown in Fig. 9(a), arising primarily from the via inductance for connecting the different layers of the metal stack also leads to performance degradation. At mm-wave frequencies, this layout parasitic inductance L_P can become a significant portion of the collector inductance L_1 . The parasitic inductance L_P reduces the output power generation in stacked switching PAs, since the voltage swing across L_P reduces the overall collector voltage swing. The output power reduces both with the number of stacked transistors (N) as well as the L_P/L_1 ratio given by

$$P_{out, L_P}^{N\text{-Stacked Class-}E} = \frac{P_{out}}{\left(1 + N \times \frac{L_P}{L_1}\right)^2}. \quad (7)$$

The values of both L_1 and shunt class-E capacitance C_{OFF} scale down with frequency. But as fewer number of parallel HBTs are now used to realize smaller values of C_{OFF} , the parasitic lead inductance L_P scales up with frequency. Thus, $L_P/L_1 \propto \omega^2$ where ω is the frequency of operation in radians. This increasing L_P/L_1 ratio with frequency degrades output power by more than 1 dB at 90 GHz in the 90-nm SiGe process [Fig. 9(b)].

In summary, layout parasitic capacitance C_P , collector inductances L_P , and low-quality factor of discrete C_{OUT} implementations are the major performance limiting factors in stacked amplifier designs at higher mm-waves frequencies [Fig. 10(a)]. These nonidealities affect both linear as well as switching amplifier operations at the W-band frequencies. In linear amplifiers, tuning out intermediate node parasitic capacitors using inductive networks have been proposed before [22]. However, in switching amplifiers, such tuning networks need to work at multiple harmonics and are more difficult and lossy to implement. The conventional stacked switching PA implementations using SiGe HBTs show that the collector efficiency degrades from 58% (Fig. 6) to 35% (Fig. 8) due to the layout parasitics while the output power also degrades by 1 dB (Fig. 9). The significant performance degradation at the W-band frequencies from layout parasitics in stacked switching PA configurations motivates the synthesis of multiport composite transistor topologies, as shown in Fig. 10(b), that can eliminate and/or incorporate the layout parasitics into the amplifier design network and result in an improved overall performance.

IV. MULTIPORT STACKED-TRANSISTOR TOPOLOGIES

To mitigate the deleterious effect of layout parasitics and lossy on-chip passives, a composite multiport transistor topology for realizing high-breakdown, high- f_{\max} stacked HBTs is proposed in this section. The objective of this layout technique conceptualized in Fig. 10(b) is to shield the sensitive intermediate collector nodes from the harmful layout parasitic capacitance and inductance while realizing the desired network capacitors C_{OUT} and C_{B2} from the layout interconnects.

A. 8-V Breakdown, 290-GHz f_{\max} Composite Transistor

To enable stacked switching PA designs at the W-band (75–110 GHz), a composite multiport two-stacked-transistor layout is built up, as shown in Fig. 11. Two native SiGe HBTs, Q_1 and Q_2 , available in the technology library are placed in series having their connections made in a three-layer metal stack of “M2-4B,” “M1-4B,” and “M2-2B.” This Q_1 – Q_2 interconnect stack is laid out to shield the Q_2 collector connection (in “OL” layer) from forming an unwanted parasitic capacitance [$C_{P,2}$ in Fig. 10(a)].

A major part of the Q_2 collector parasitic capacitance ($C_{P,2}$) is from the Q_2 collector manifold (overhang) that is required to connect HBT devices of large multiplicity. A wide Q_2 collector manifold is also required to reduce the collector connection resistance and handle large collector current density. The layout topology shown in Fig. 11 uses the collector

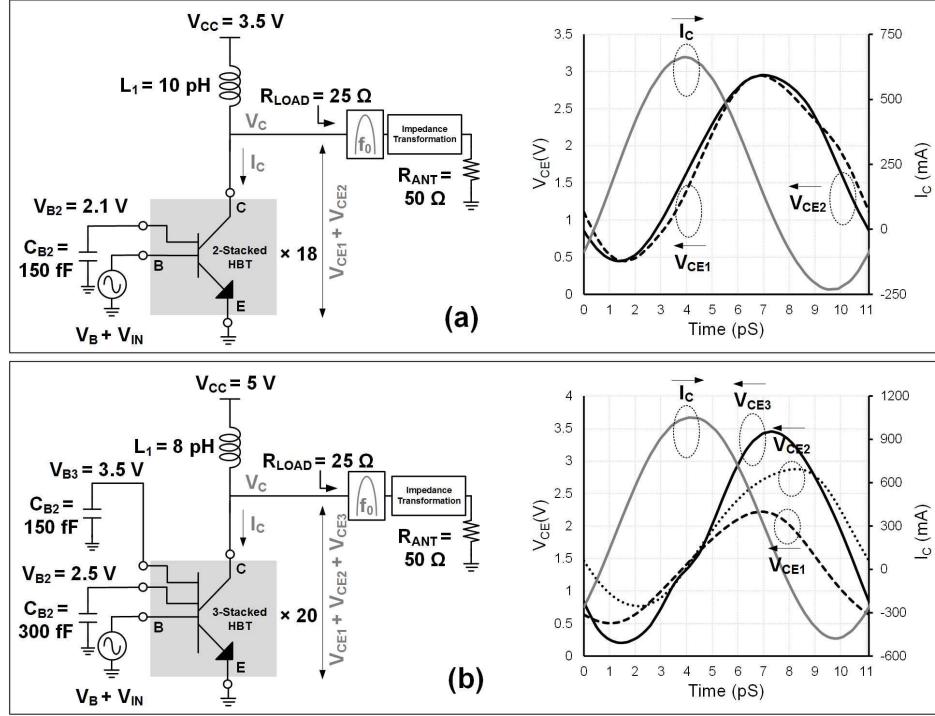


Fig. 14. Linear PA design examples at 90 GHz. (a) Two-stacked Class-A PA along with transient collector voltage–current waveforms. (b) Three-stacked Class-A PA along with transient collector voltage–current waveforms.

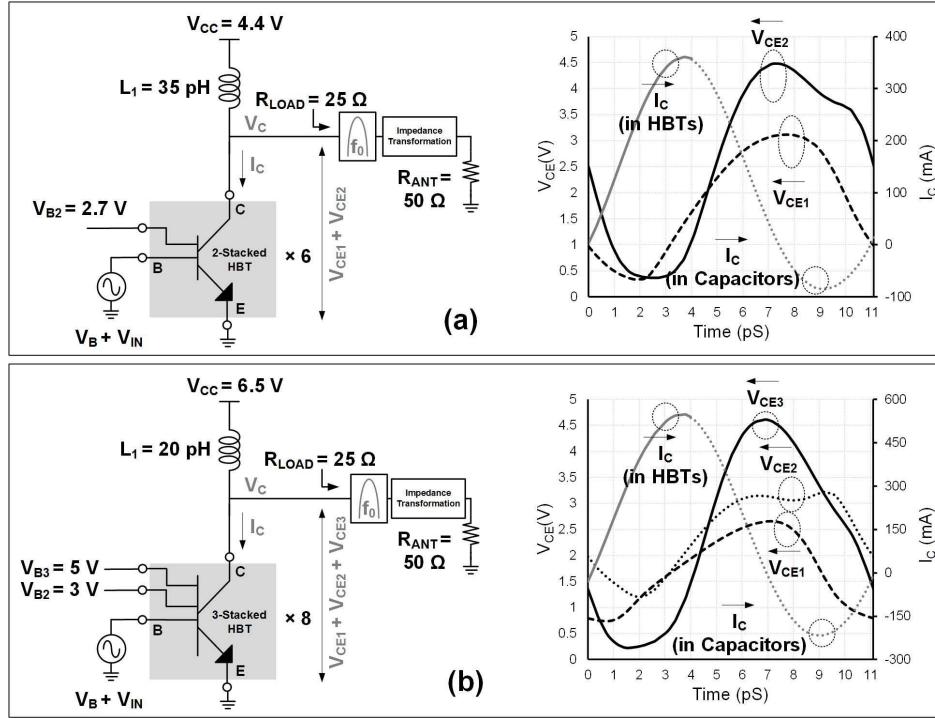


Fig. 15. Switching PA design examples at 90 GHz. (a) Two-stacked Class-E PA along with transient collector voltage–current waveforms. (b) Three-stacked Class-E PA along with transient collector voltage–current waveforms.

manifold of Q_1 to shield the collector manifold of Q_2 . The via and metal layers that are required for the Q_2 collector connection to move up to metal layer OL also contribute some parasitic capacitances. However, in a collector-base-emitter-base-collector (CBEBC) HBT layout, the side-wall parasitic capacitances due the via/metal stack mainly lead to

collector–base parasitic capacitances (C_{CB2}), which are connected to the much larger CBE HBT intrinsic capacitances and do not change circuit performance.

Furthermore, the output capacitor C_{OUT} is now entirely synthesized from the transistor footprint ($Q_1 - Q_2$ collector connection overlap). This output capacitor C_{OUT} enables

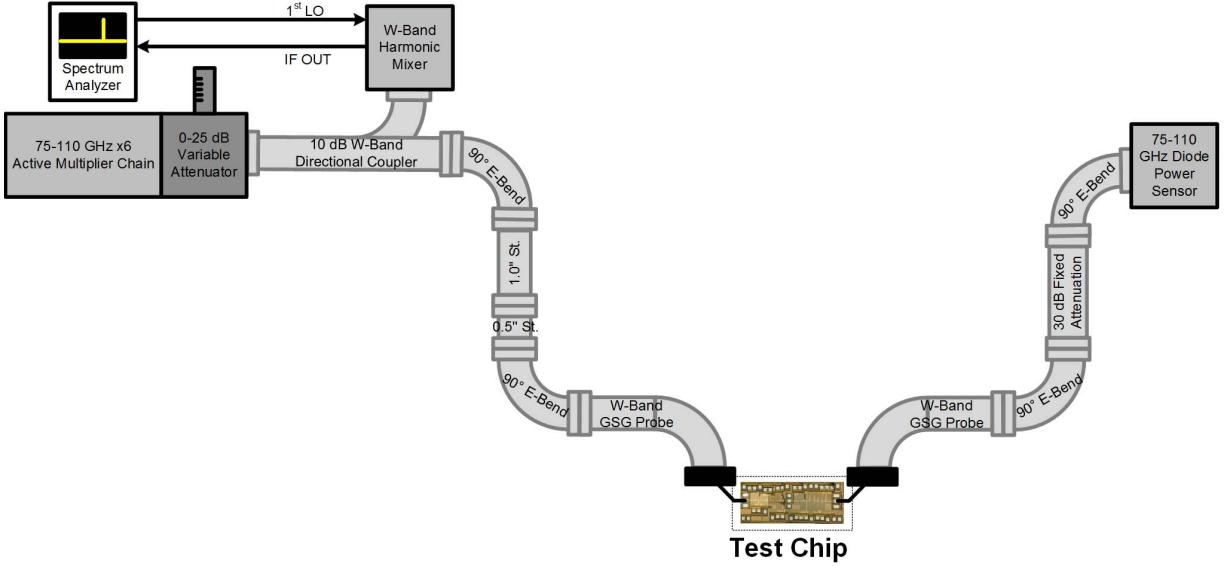


Fig. 16. Large-signal measurement test setup for the W-band switching PAs.

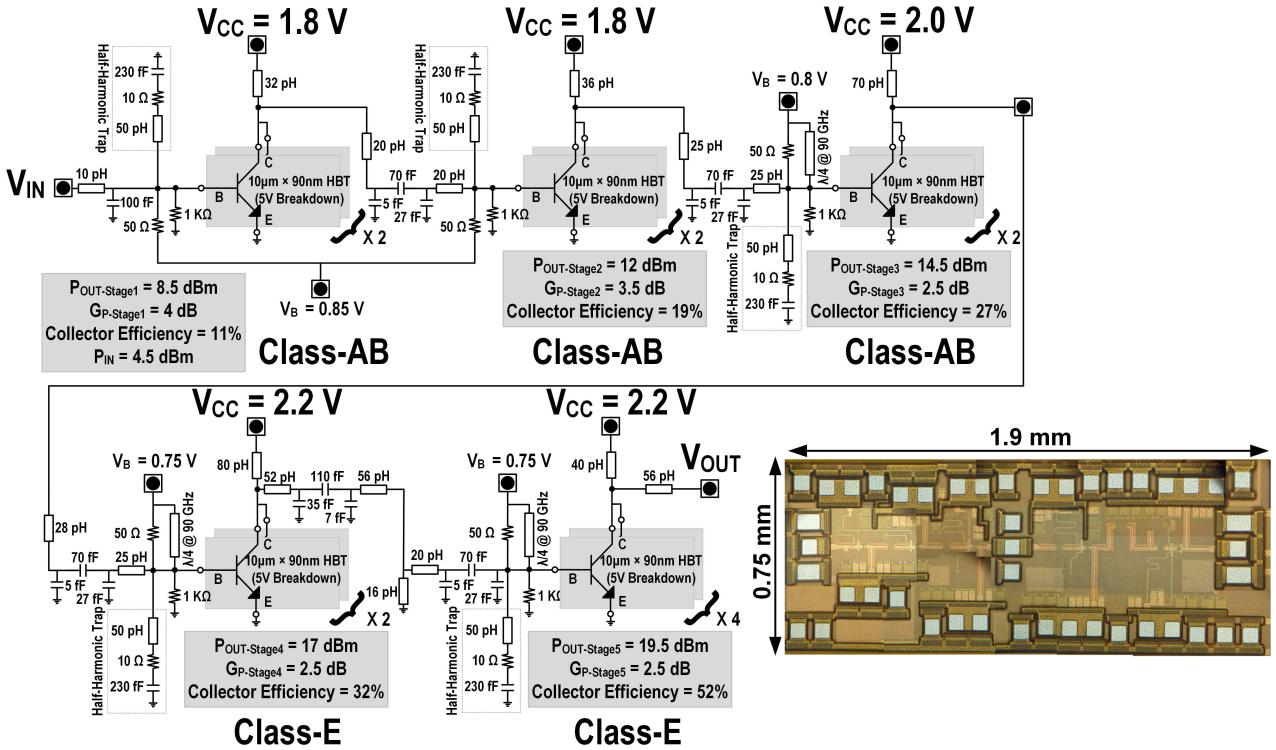


Fig. 17. Schematic and chip microphotograph of the five-stage W-band nonstacked Class-E PA.

equitable distribution of collector voltage across series transistors Q_1-Q_2 and its realization from the “OL” and “M2-4B” metal overlap achieves a metal–oxide–metal (MOM) capacitor having comparatively high Q -factor of 25 at the W -band frequencies. The base terminal connection of Q_2 using the metal layer “M1-2B” is used to shield the Q_1 collector terminal from forming an unwanted parasitic capacitance [$C_{P,1}$ in Fig. 10(a)]. The “M1-2B” base terminal connection is also

used to realize the Q_2 base terminal capacitor C_{B2} , which ensures that Q_2 switches synchronously with Q_1 . Since the relative separation between “M1-2B” and the “M1-M4” ground layer is small, this arrangement is ideal to realize high- Q relatively large C_{B2} values in small form factor. Two parasitic base–emitter capacitors, C_{BE1} and C_{BE2} , are generated in this composite two-stacked HBT layout strategy. However, since these parasitic base–emitter capacitors come in parallel

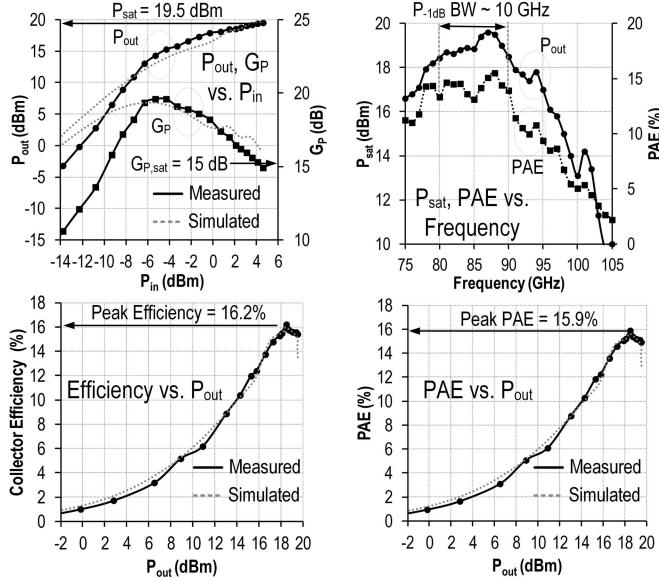


Fig. 18. Large-signal measurements of five-stage W-band nonstacked Class-E PA at 88 GHz.

to the large intrinsic HBT base–emitter capacitors, they do not degrade the W-band amplifier performance. The close spacing of the Q_1 and Q_2 collector connection also ensures that the collector lead inductance is minimized. This composite transistor layout may be imagined as a three-terminal transistor (with an additional dc bias node) having an 8 V equivalent breakdown voltage.

A Class-E amplifier (described in detail in Section V) using several such “two-stacked” composite multiport HBTs placed in parallel can be designed. The simulated voltage–current contour of such composite transistors shown in Fig. 11 confirms that the collector voltage in such composite transistors can swing as high as 8 V even at the W-band frequencies.

B. 11-V Breakdown, 260-GHz f_{\max} Composite Transistor

A similar approach can be taken to include more series-stacked HBTs resulting in a composite transistor with even higher breakdown voltage. Fig. 12 shows a three-stacked composite transistor with 11-V breakdown voltage. In the three-stacked composite multiport HBT layout of Fig. 12, the desired network capacitors $C_{OUT,1}$, $C_{OUT,2}$, C_{B2} , and C_{B3} are realized by the overlap of Q_1 , Q_2 , Q_3 base, collector, and emitter metal interconnects. Like before, the sensitive collector nodes of Q_1 , Q_2 , and Q_3 are protected from any additional parasitic capacitor to the grounded emitter, improving collector efficiency. The only resulting parasitic capacitances from this layout, viz., C_{BE1} , C_{BE2} , and C_{BE3} are all parallel to much larger intrinsic base–emitter device capacitors and negligibly affect the W-band performance. As shown in Fig. 12, this composite transistor may again be imagined as an equivalent three-terminal transistor (with two additional dc bias nodes) having a larger breakdown voltage of 11 V. Multiple instances of such three-stacked composite multiport HBTs in parallel

can be used in the design of the W-band switching amplifiers. The simulated collector voltage–current contour of such composite transistors confirms SiGe HBT operation within safe limits while swinging 11 V.

The proposed two-stacked and three-stacked composite multiport HBTs enable realization of high power, efficient W-band switching amplifiers by eliminating the harmful layout parasitics. The layout parasitic modeled two-stacked and three-stacked composite multiport HBT configurations show a high peak f_{\max} of 290 and 260 GHz, respectively, with the marginal degradation arising from the resistivity of the metal interconnects (Fig. 13). As such, these composite cells can also be used for stacked linear amplifier designs at mm-wave frequencies.

V. W-BAND DESIGN EXAMPLES USING MULTIPORT TRANSISTOR TOPOLOGIES

To illustrate the effectiveness of the proposed multiport stacked-transistor structures, linear and switching amplifiers at 90 GHz are designed. $R_{Load} = 25 \Omega$ has been chosen to ensure that losses arising from output matching networks affect both designs equally.

A. W-Band Class-A PA Designs

Similar to the nonstacked Class-A linear PA design in Section II-A, the composite “two-stacked” transistor topology can also be biased at different collector current densities J_C for different effective breakdown voltages V_{Br} . From Fig. 13 and following the logic outlined in Section II, choosing a quiescent current density $J_{C,Q} = 0.5 \times J_{C,fmax} = 10 \text{ mA}/\mu\text{m}^2$ results in optimum tradeoff between power gain and breakdown voltage. Under this biasing condition, the effective breakdown voltage V_{Br} for the “two-stacked” and “three-stacked” topologies is 5.8 and 8.5 V, respectively. The schematic of the Class-A design using the two-stacked’ multiport topology under a 25- Ω load line and the transient collector voltage and current waveforms are shown in Fig. 14(a). Simulations predict the power of $P_{out} = 21 \text{ dBm}$, $G_P = 7 \text{ dB}$, $\eta = 20\%$, and PAE = 17%. The schematic of the Class-A design using the three-stacked’ multiport topology under a 25- Ω load line and the transient collector voltage and current waveforms are shown in Fig. 14(b). Simulations predict $P_{out} = 23.8 \text{ dBm}$, $G_P = 8.5 \text{ dB}$, $\eta = 16\%$, and PAE = 14%.

B. W-Band Class-E PA Designs

From the HBT safe-area-operation shown in Fig. 11 and Fig. 12, the breakdown voltages for the “two-stacked” and “three-stacked” topologies under Class-E operation are 8 and 11 V, respectively. The schematic of the Class-E design using the “two-stacked” multiport topology under a 25- Ω load line and the transient collector voltage and current waveforms are shown in Fig. 15(a). Simulations predict $P_{out} = 23.5 \text{ dBm}$, $G_P = 9 \text{ dB}$, $\eta = 55\%$, and PAE = 49%. Compared with the conventional stacked Class-E layout topology, where the layout parasitics of Section III degrade the collector efficiency to 35%, and the proposed layout topology can achieve a high collector efficiency of 55%.

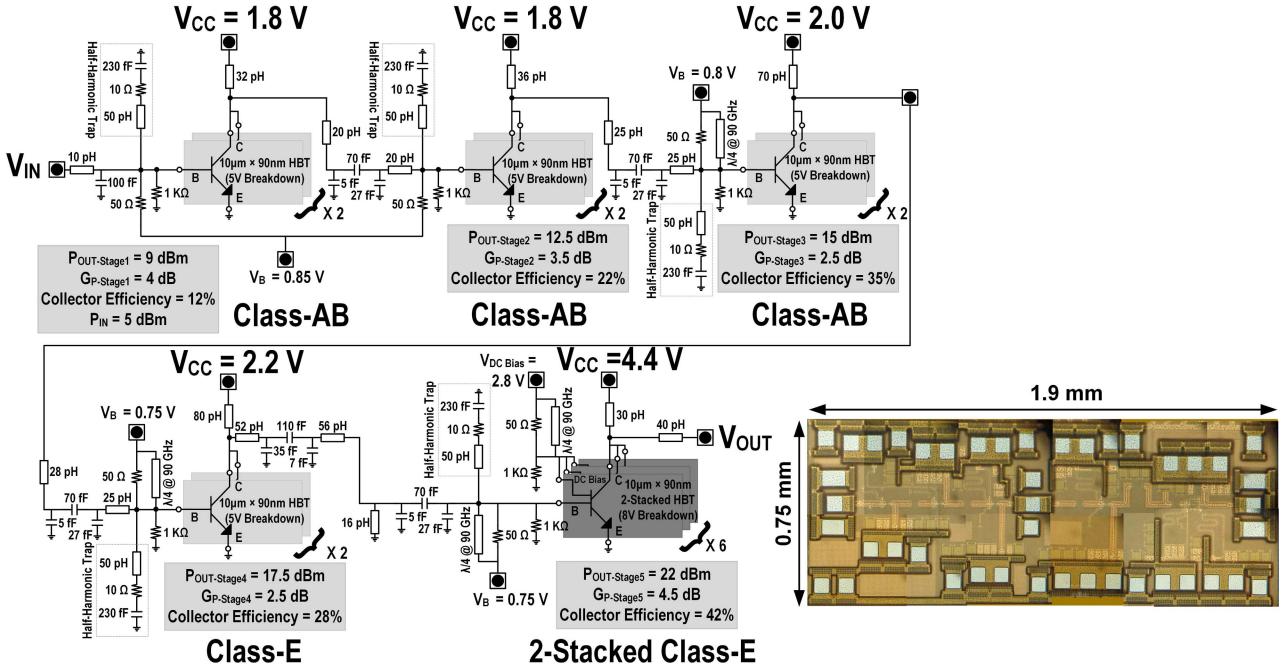


Fig. 19. Schematic and chip microphotograph of the five-stage W-band two-stacked Class-E PA.

The schematic of the Class-E design using the “three-stacked” multiport topology under a 25- Ω load line and the transient collector voltage and current waveforms are shown in Fig. 15(b). Simulations predict $P_{\text{out}} = 25 \text{ dBm}$, $G_P = 11 \text{ dB}$, $\eta = 35\%$, and PAE = 31%. In both the cases, it can be seen that the output power and efficiencies are significantly higher when compared with the Class-A design that uses the same composite transistor structures. The effectiveness of these multiport stacked-transistor topologies at the W-band frequencies have thus been demonstrated by implementing multistage stacked switching power amplifiers in the 90-nm SiGe process.

VI. IMPLEMENTATION AND MEASUREMENT RESULTS

Multistage W-band implementations of the two-stacked and three-stacked switching PAs using the proposed multiport transistor topologies have been fabricated in a 90-nm SiGe process [23]. In all the following designs, accurate prediction of the layout parasitics especially for the multiport transistor topologies has been estimated using HyperLynx 3-D electromagnetic simulator [26]. Stability of SiGe HBT power amplifiers is ensured by the addition of half-harmonic traps and parallel base resistance to the base of each transistor [6]. To prevent thermal runaway in the SiGe HBT designs, each transistor array is designed to operate within safe collector current density, and a symmetrical layout is implemented to ensure equal heat dissipation across the power transistor array.

The PA implementations have been measured under continuous wave input. The test setup for large-signal power measurement at the W-band frequencies is shown in Fig. 16. An active multiplier chain followed by a variable attenuator

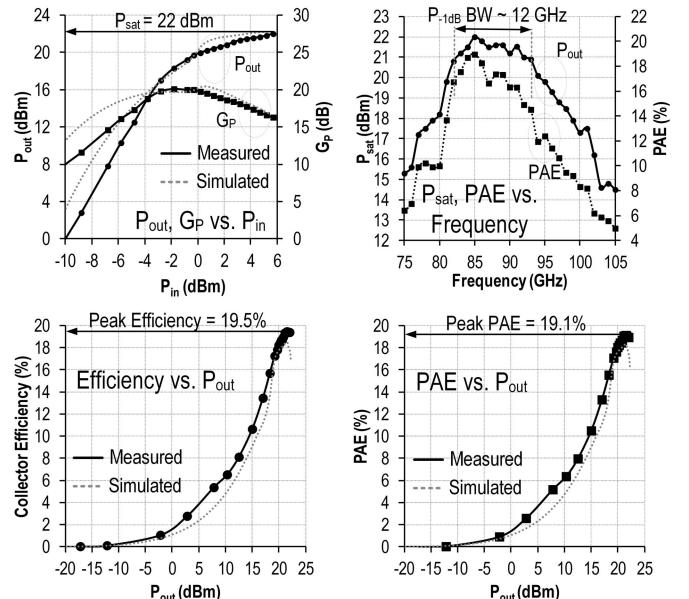


Fig. 20. Large-signal measurements of five-stage W-band two-stacked Class-E PA at 85 GHz.

is used to generate the continuous wave W-band input signal. A spectrum analyzer connected with the W-band harmonic mixer is first used to verify the absence of spurs/oscillatory behavior under large-signal measurement in the power amplifiers. For accurate power measurement, the W-band diode power sensor is used at the output. Input power to the PA modules is calculated using the W-band coupler/harmonic mixer combination for accurate power gain calculation. All the input/output connections in the test setup are implemented using WR-10 waveguides.

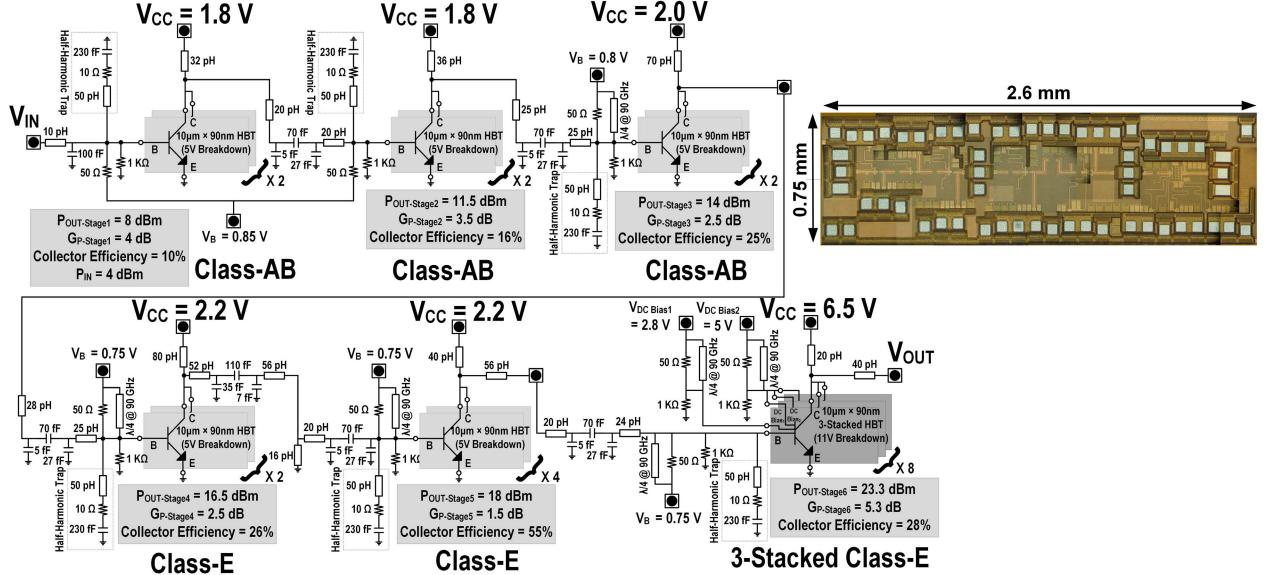


Fig. 21. Schematic and chip microphotograph of the six-stage W-band three-stacked Class-E PA.

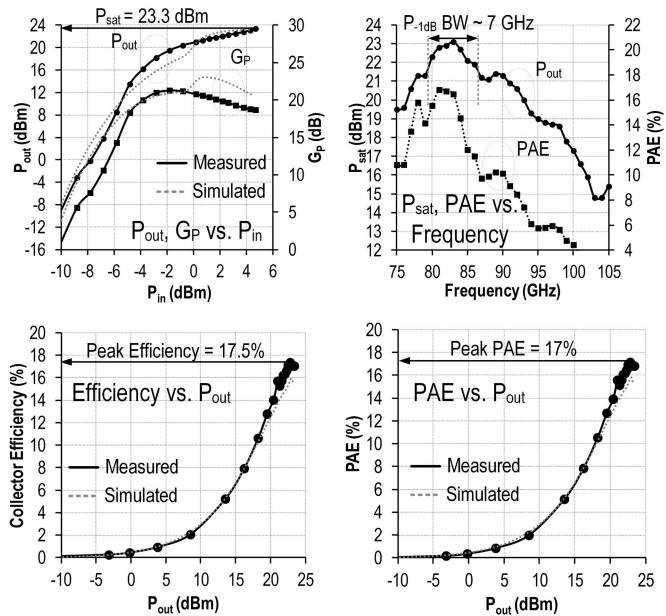


Fig. 22. Large-signal measurements of six-stage W-band three-stacked Class-E PA at 83 GHz.

A. 19.5-dBm, Five-Stage, W-Band, Nonstacked Class-E PA

To benchmark the 90-nm SiGe process for switching PA operation at the W-band frequencies, a five-stage nonstacked PA was designed and fabricated using the native SiGe HBTs, as shown in Fig. 17. The last two power stages are designed as Class-E switching PAs and operate under large supply voltage of 2.2 V. The first three stages are designed as high gain Class-AB amplifiers and operate under lower 1.8 V supply. The large-signal measurements of this switching PA are shown in Fig. 18. This PA achieved a peak output power of 19.5 dBm

at 16% peak PAE at 88 GHz. The measured performance of this switching PA will be used to benchmark the proposed stacked Class-E PA designs also fabricated in the same process.

B. 22-dBm, Five-Stage W-Band Two-Stacked Class-E PA

To demonstrate the performance benefits of using the proposed composite transistor topologies, a five-stage W-band PA was implemented with the 8 V two-stacked composite multiport HBT configurations in the final stage (Fig. 19). The last two power stages are biased for Class-E switching operation and the initial three stages operate in Class-AB/B. Fig. 20 shows the measured large signal performance of the implemented W-band PA chain at 85 GHz. A maximum output power of 22 dBm (220 mW), 17 dB of large-signal power gain, peak collector efficiency of 19.5%, and peak PAE of 19% are reported. The implemented PA also demonstrates wideband performance with P_{-1} dB bandwidth of 12 GHz with PAE > 16% across the P_{-1} dB band. The output power remains > 14 dBm across the 75–105 GHz with upper frequency measurements limited by test-setup limitations.

C. 23.3-dBm Six-Stage W-Band Three-Stacked Class-E PA

The operation of the three-stacked composite multiport HBT configuration is demonstrated by implementing a six-stage W-band PA (Fig. 21). The last three stages are biased in Class-E switching amplifier mode and the initial stages as Class-AB/B mode. The measured large-signal performance in Fig. 22 shows an even larger output power of 23.3 dBm (220 mW) with 18.7-dB power gain at 83 GHz. The peak efficiency and PAE are reported as 17.5% and 17%, respectively, with a P_{-1} dB bandwidth of 7 GHz with PAE > 15% across the P_{-1} dB band. In both the implementations, the measurement results and simulation follow closely, validating

TABLE II
MEASURED PERFORMANCE SUMMARY OF THE STACKED W-BAND SiGe HBT AMPLIFIERS

Performance Metric	This Work			ISSCC 2014 [3]	JSSC 2014 [22]	BCTM 2008 [4]	RFIC 2014 [2]	TMTT 2016 [5]
	Normal Class-E	2-Stacked Class-E	3-Stacked Class-E					
Center Frequency (GHz)	88	85	83	80	91	90	94	76
P_{out} (dBm)	19.5	22	23.3	20.9	19.2	19.6	24	27.3
Peak Efficiency (%)	16.2	19.5	17.4	23	14.9	16	5	N/R
Peak PAE (%)	15.9	19.1	17.1	22.3	14	15.4	N/R	12.4
G_P (dB)	15	17	18.7	13	12.4	10.6	N/R	19.3
$P_{-1\text{dB}}$ Bandwidth (GHz)	10	12	7	15	8.5	N/R	N/R	6
$P_{-3\text{dB}}$ Bandwidth (GHz)	20	16	17	N/R	>11	22	5	> 10
Supply Voltage (V)	2.2	4.4	6.5	0.9	3.4	2.3	4	1.8
Power Combining	No	No	No	4-Way Combined	No	Off-Chip 2:1 Balun	16-Way Spatial	16-Way Combined
Area (mm^2)	1.425	1.425	1.95	1.6	0.36	2.4	26	6.48
Technology	90nm SiGe BiCMOS			40nm SOI	45nm SOI	130 nm SiGe	45nm SOI	90nm SiGe

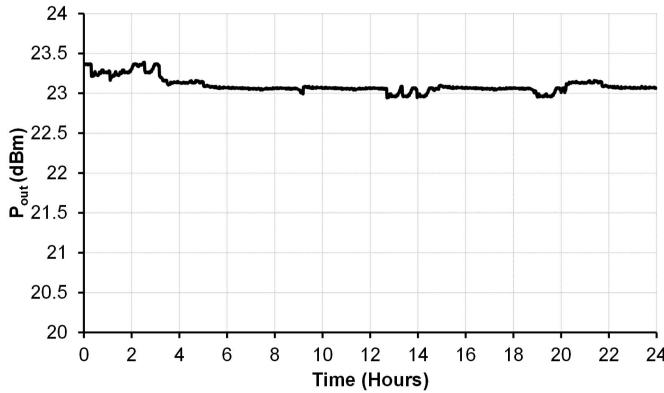


Fig. 23. Output power measurement of the three-stacked Class-E PA at 83 GHz for 24 h under continuous wave input.

the accuracy of the composite device parasitics and passive modeling. To illustrate reliability and robustness of the W-band stacked-transistor Class-E amplifiers, the output power of the three-stacked PA was recorded for 24 h under continuous wave measurement (Fig. 23). The small (<0.3 dB) variations in output power may be due to small mechanical displacements of the input and output probes during lengthy measurements.

Table II shows that the stacked Class-E designs with the proposed composite transistors achieve better performance compared with the reference Class-E design. Compared with the reported state-of-the-art silicon PAs at the W-band, the proposed designs demonstrate the widest frequency of operation, the highest power generated without power combining, and the highest reported PAE for such power levels.

VII. CONCLUSION

Multiport stacked-transistor topologies with integrated layout parasitics as proposed in this paper can enable efficient, high power switching Class-E power amplifiers in silicon technologies for the W-band operation. The implemented stacked PA designs with multiport stacked-transistor topologies

demonstrate >22 -dBm output power with $\approx 20\%$ PAE and can be used in energy-efficient high-speed mm-wave wireless links.

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