

A Low-Power Digitizer for Back-Illuminated 3-D-Stacked CMOS Image Sensor Readout With Passing Window and Double Auto-Zeroing Techniques

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Abstract—This paper presents a high-performance digitizer based on column-parallel single-slope analog-to-digital converter (SS-ADC) topology for readout of a back-illuminated 3-D-stacked CMOS image sensor. To address the high power consumption issue in high speed digital counters, a passing window (PW)-based hybrid counter topology is proposed. In this approach, the memory cells in the digital counters of SS-ADCs are disconnected from the global bus during non-relevant timing. To address the high column fixed pattern noise (FPN) under bright illumination conditions, a double auto-zeroing (AZ) scheme is proposed. In this technique, the AZ process is employed twice at reset and signal level, respectively. The double AZ scheme not only allows the comparator to serve as a crossing detector around the common-mode level, but it also enables low-voltage comparator design. The proposed techniques are experimentally verified in a prototype chip designed and fabricated in the TSMC 40 nm low-power CMOS process. The PW technique saves 52.8% of power consumption in the hybrid digital counters. Dark/bright column FPN of 0.0024%/0.028% is achieved employing the proposed double AZ technique for digital correlated double sampling. A single-column digitizer consumes a total power of 66.8 μ W and occupies an area of 5.4 μ m \times 610 μ m.

Index Terms—CMOS image sensor digitizer, correlated double sampling (CDS), fixed pattern noise (FPN), low-power counter, single-slope (SS) ADC.

I. INTRODUCTION

RECENT innovations on back-illuminated 3-D-stacked process for CMOS image sensors [1]–[12] have stimulated a new leap forward in the image sensor industry. The separation of the conventional image sensor process for pixels and the logic process for the readout circuits enables independent performance optimization leading to cost reduction. Instead of sticking to an image sensor process, advanced logic technology

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nodes are applicable choices for the image sensor digitizer which infers both power and area benefits with process scaling.

The most critical building block of an image sensor digitizer is the analog-to-digital converter (ADC). Diverse topologies of ADCs integrated at different levels have been reported targeting high-speed, low-power, and area-efficient implementation [1], [3], [10]–[12], [13]–[21]. Binary-search algorithm-based ADCs like cyclic [12]–[14] and successive approximation registers (SARs) [17]–[19] are typically faster compared with ramp-based ADCs [1], [3], [10], [11], [20], [21] and oversampling ADCs [15], [16]. However, cyclic ADCs demand amplifiers with precise gain while SAR ADCs require well-matched capacitor digital-to-analog converters (DACs) to achieve high resolution. Forcing cyclic/SAR ADCs into a column-parallel array with a small pixel pitch results in significant layout complexity and column non-uniformity [17]. Furthermore, issues in reference voltage and power supply distribution can degrade far-end ADC performance [19]. Employing a single chip-level pipelined SAR ADC to read out the entire pixel array avoids the area and the analog voltage distribution issues, but the frame rate of the image sensor is limited by the speed of the ADC [18]. Column-parallel oversampling ADCs with noise filtering can achieve low random noise and wide dynamic range, but complicated decimation filters are usually demanded. On the contrary, single-slope ADCs (SS-ADCs), working in column-parallel array and sharing the same ramp signal, have superior fitness for fine-pitch-pixel readout. With only comparators in the analog domain, SS-ADCs benefit from the 3-D-stacked process revolution because of their simplicity. Another advantage of an SS-ADC is its good differential non-linearity (DNL) performance without large spikes, which is common problem in cyclic/SAR ADCs [19]. In addition, the digital correlated double sampling (CDS) technique has proven effective in SS-ADC, resolving a number of limiting issues like resetting KT/C noise, pixel and readout fixed pattern noise (FPN), clock skew, and ramp delay [20].

However, employing SS-ADC architecture as a digitizer for CMOS image sensor application comes with two obstacles. A high-speed SS-ADC demands a fast-counting clock, which implies high power consumption in the digital counters lumped to each column [20]. In [11] and [21], by sharing a global 5-bit

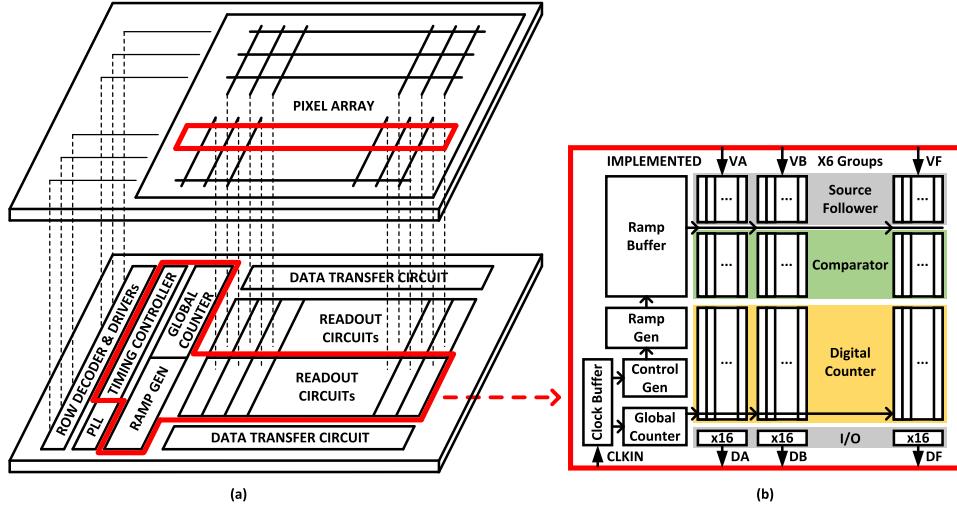


Fig. 1. Block diagram of (a) 3-D image sensor chip and (b) 96-column digitizer prototype.

least significant bit (LSB) counter between every 248 columns and put memory cells in columns, the power consumption of the digital counter was reduced. However, if the memory cells in columns are implemented as transparent standard-cell latches [11], the continuous refreshing of the memory cells before the real latching moment will lead to a large amount of power waste. Second, in the conventional CDS scheme [20], during auto-zeroing (AZ), the offset and delay information stored for cancellation purpose only corresponds to small pixel information levels. Nevertheless, under bright illumination conditions, the input of the comparator [20] crosses at a much lower voltage level, which corresponds to a different offset and delay information. For the aforementioned reasons, the digital CDS subtraction introduces a cancellation error, which results in large column FPN left under bright illumination conditions.

In this paper, passing window (PW) and double AZ techniques are presented to address these two issues. The LSB memory cells in the hybrid digital counters of SS-ADCs are only connected to the global buses during an auto-generated PW. This allows power saving in both LSB memories and global data bus drivers. The first attempt to employ double AZ concept to solve bright column FPN was made in this design. The AZ process of comparator is employed twice during reset and signal readout phase, respectively, such that the comparator operates as a crossing detector only around the same common-mode level. With a double AZ scheme, an effective comparator offset and delay cancellation with digital CDS can be achieved even under bright illumination. Normally, dark image column FPN is more visible than bright column FPN. However, as when designers lower down the power supply aiming to save power, the bright column FPN performance gets worse and becomes more noticeable.

This paper is organized as follows. Section II describes the overall architecture of the image sensor chip. Section III describes the proposed PW and double AZ techniques. The circuit-level implementations of the most relevant building blocks of the digitizer are detailed in Section IV. The measurement results are discussed in Section V, and Section VI concludes this paper.

II. SENSOR ARCHITECTURE

A typical CMOS image sensor system consists of a pixel array, a digitizer, a row decoder and driver, a timing controller, a phase-locked loop, and a data transfer circuit. In a conventional 2-D implementation, the pixel array is arranged at the center of the chip and the peripheral circuits have to be designed using the same process optimized for the pixels. This arrangement limits the performance of the peripheral circuits and degrades the silicon area efficiency. The first commercial product of a back-illuminated 3-D-stacked image sensor was reported in [1]. The connection between the interconnect layers between the top and bottom parts was realized with through-silicon vias outside the pixel array. In [10]–[12] and [22], with direct connection of top and bottom wafers with Cu–Cu bonding, the pixel array to chip area ratio is improved because the connection position can be under the pixel array.

Fig. 1(a) shows a back-illuminated 3-D-stacked CMOS image sensor with direct interconnection between the top and bottom wafers [10]. While the design techniques are eventually targeting at entire multi-megapixel image sensor readout, in this prototype, only 96 columns of readout circuits are implemented as shown in Fig. 1(b), in order to focus on the characterization of the digitizer design. The source followers, together with switches multiplexing between reset voltage and signal voltage, are employed to mimic the pixel operation. No column gain amplifiers are used and the source follower outputs are directly connected to the column SS-ADCs. The main counting 1.7 GHz clock is generated externally and buffered on chip, while both the timing control and the global ramp are generated on chip.

III. PROPOSED TECHNIQUES

The column-parallel digital counters and comparators are critical blocks for digitizing the analog pixel information level into digital numbers (DNs). The two proposed techniques, PW and double AZ, are dedicated to improving the performance of digital counters and comparators, respectively.

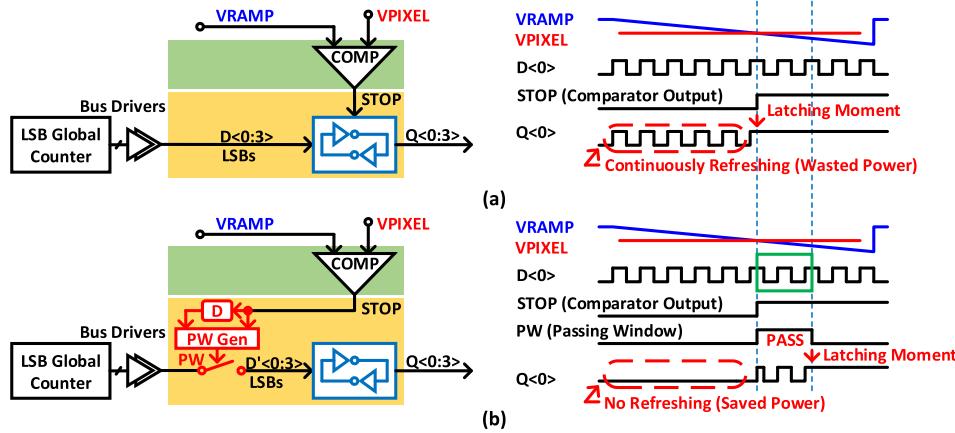


Fig. 2. Global counter latching scheme (a) without PW and (b) with PW.

A. Passing Window Compatible With CDS

In the conventional SS-ADC, the ripple counter topology [20] is a popular choice for the digital counter. First, the architecture is simple with only a single line of cascaded D-flip flops resulting in an area efficient solution. Second, no synchronization circuits are demanded. Third, a ripple counter capable of doing both up and down counting makes digital CDS subtraction possible in every column. However, a main issue with ripple counter topology in high-speed SS-ADCs is that the lower-bit D-flip flops are always counting at high frequency until the STOP signal from the comparator is generated.

To address this issue, a hybrid column counter scheme was proposed first in [21]. The digital counter is divided into two parts: 1) a lower 5-bit global counter shared by 248 column memories and 2) an upper 9-bit column-based ripple counter. In this partitioning manner, replacing 5-bit continuous running D-flip flops with memory cells sharing one global counter, power can be saved. However, if the memory cells in columns are implemented as transparent standard-cell latches [11], before the comparator output flips, the high-speed LSB data buses are always refreshing the memory cells. As the comparator output can flip at any time, the memory cells in [11] needs to be connected to the global LSB counter bus all the time before the latching moment. The power needed for charging and discharging the capacitors in the memory cells is wasted, as the relevant counting information is only captured at the latching instant STOP as shown in Fig. 2(a). Only after the latching signal is generated can the memory cells be latched to the data and saved for readout before the next horizontal scan.

Fig. 2(b) shows the improved latching scheme with the proposed PW technique. The PW digital switch disconnects the memory cells from the global data bus during non-relevant timing which not only allows power minimization in the column memories, but also enables power savings due to the lower capacitance driven by the data bus drivers. It is possible to generate a PW based on delaying the comparator output [2] as shown in Fig. 2(b). However, with this method, the real latching moment is also delayed which introduces

a process-voltage-temperature (PVT)-dependent offset and affects the performance of the SS-ADC. In [10], a look-ahead circuit consisting of a dynamic comparator (D-CMP) and logic in each column together with a globally shared early ramp generator, was proposed to cut unnecessary power consumed by the static comparator (S-CMP) and digital counter. This approach, however, requires complex circuitry. Moreover, the power saved through gating the high-speed clock until decision of D-CMP is limited.

In this design, the hold-and-go counting scheme as defined in [23] is adjusted to generate the PW, which makes the proposed PW technique fully compatible with the digital CDS. Fig. 3(a) and (b) show the proposed CDS timing scheme of the SS-ADC within one horizontal scan under bright and dark illumination condition, respectively. The column-parallel digital counter contains a FLAG generation circuit, a reset counter, and a signal counter composed of LSB memories and a most significant bit (MSB) counter. The conventional digital CDS operation demands the following procedures.

- 1) Quantize the reset information corresponding to T1 in the reset readout phase (Φ_{rst}).
- 2) Quantize the signal information corresponding to T3 in the signal readout phase (Φ_{sig}).
- 3) Subtract the reset information (T1) from the signal information (T3) in the digital domain.

In the proposed CDS scheme, by splitting T into T1 and T2, T3 into T and T4, the real pixel information level can be expressed as

$$T_{pixel} = T_3 - T_1 = (T_4 + T) - (T - T_2) = T_4 + T_2 \quad (1)$$

where T is the full counting time of the reset counter and T2 is the time left for the reset counter to count to full starting from T1. T4 is defined as the time difference from the moment when the signal counter start counting to the moment when the comparator output flips during Φ_{sig} . Based on this definition, T4 is always equal to T3 - T and can become negative when T3 < T under dark illumination condition as shown in Fig. 3(b). Thus instead of quantizing T1 and T3 separately, single capture of T4 + T2 in the signal counter is possible following the procedures below.

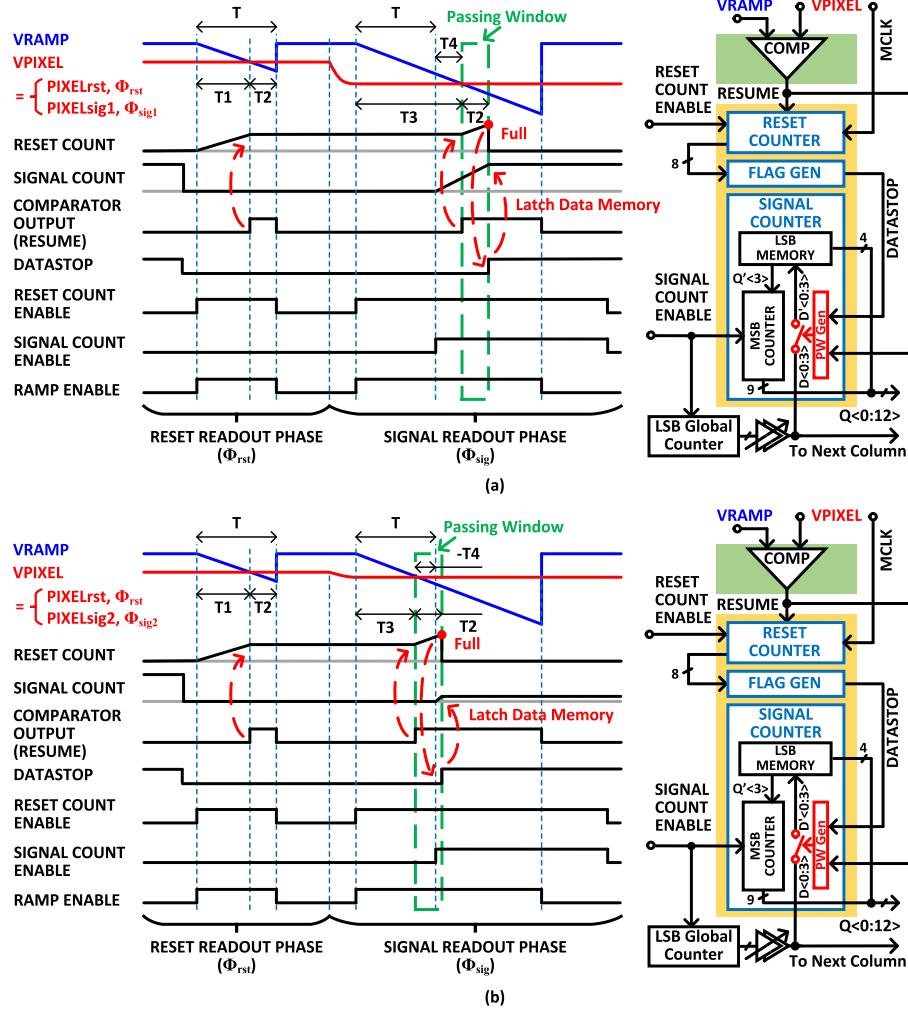


Fig. 3. CDS timing scheme for one horizontal scan (a) under bright illumination condition and (b) under dark illumination condition.

- 1) During Φ_{rst} , the reset counter is enabled at the same moment that the ramp starts and stops when VRAMP crosses with VPIXEL_{rst}. T1 is then saved on the reset counter.
- 2) During Φ_{sig} , the signal counter and the LSB global counter start counting time of T later than the start of the ramp. When VRAMP crosses with VPIXEL_{sig}, the reset counter resumes counting from saved T1. The PW switches are then closed allowing the LSB data buses to refresh the LSB memory cells in the signal counter.
- 3) During Φ_{sig} , the state when the reset counter counts to its full range is detected by the FLAG generation circuit. The generated DATASTOP signal opens the PW switches and disconnects the LSB memory cells from the LSB data buses. As the LSB memory cells are latched, the cascaded MSB counter also stops.

After finishing the procedure above, the targeted digitized pixel information level after CDS corresponding to time $T_4 + T_2$ is stored in the signal counter. The real latching moment is defined by the FLAG generation, and time T_2 after the comparator output flips. Thus, the PW of T_2 is created automatically using the comparator output together with the

DATASTOP signal without introducing any additional offset or complex digital circuitry. The PW technique is proposed to save the power spent in driving and refreshing the column memory cells, and thus more effective for bright illumination condition when more time of driving and refreshing is needed before the latching moment. Under dark illumination, if the demanded counting time is smaller than the PW as the case shown in Fig. 3(b), the power saving benefit of the proposed PW technique is less compared to the case of bright illumination.

B. Double Auto-Zeroing

In a conventional CDS scheme, the AZ of the comparator is employed only once in Φ_{rst} as shown in Fig. 4(a) [20], [24]–[27]. A modified implementation of the comparator in Fig. 4(a) with a fully differential first stage to avoid systematic offset is shown in Fig. 4(b). One critical drawback of the topologies shown in Fig. 4(a) and (b) is that the offset and delay information of the comparator saved in the capacitors for cancellation purpose during Φ_{rst} only corresponds to dark illumination conditions. During Φ_{sig} , the comparator makes the critical decision at very different voltage levels. If the offset and delay of analog comparators vary much with its input

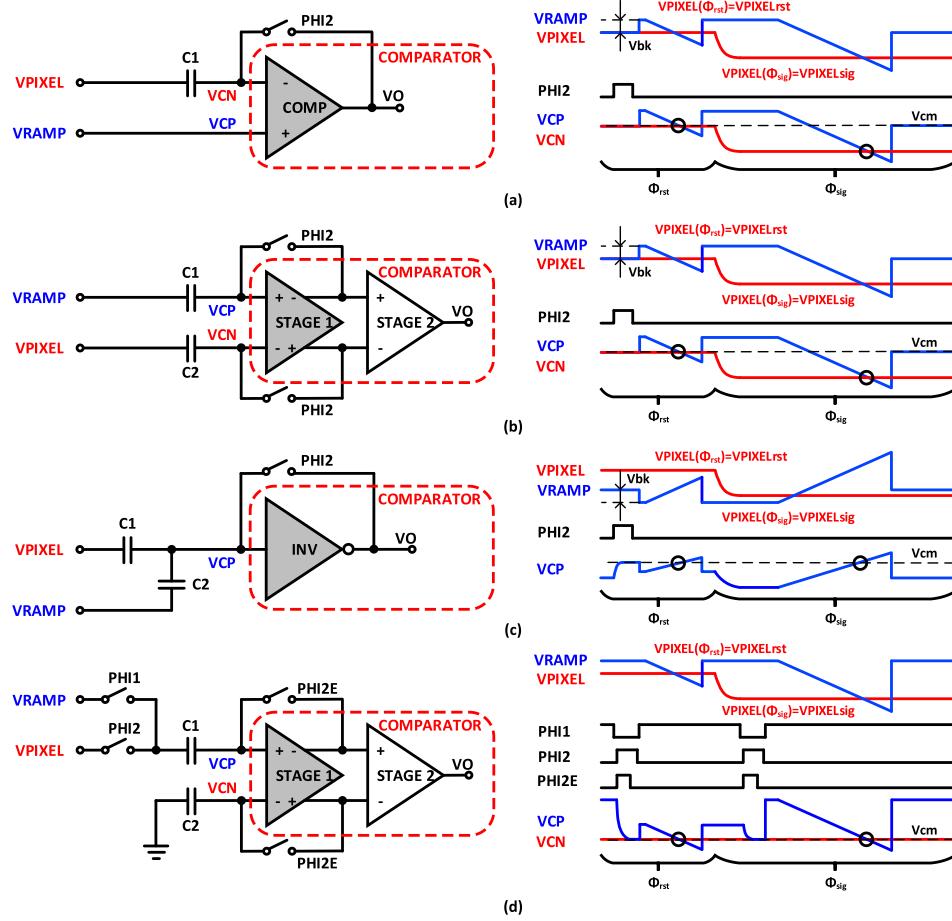


Fig. 4. Column comparator topologies.

voltage crossing level, the conventional CDS scheme is not quite effective, especially under bright illumination conditions, when the difference between pixel reset voltage and pixel signal voltage can be full-scale. The imperfect digital CDS induced cancellation error results in large column FPN left under bright illumination condition. Although shot noise and pixel FPN dominate, column FPN can be noticeable to human eyes, especially when the comparator input common-mode range is very limited under low power supply.

Designing a low-power comparator under low supply voltage with a constant offset and constant time delay over the entire pixel information range in the presence of PVT variations can be challenging and power demanding. Instead, an improved topology as shown in Fig. 4(c) [11] was proposed to avoid this problem by maintaining the input crossing point of the comparators always at AZ level. However, the charge sharing structure demands well matched capacitor ratios of C1 and C2 among columns to achieve low column FPN. The charge recombination present at node VCP reduces the error signal by 6dB leading to SNR degradation. Finally, even though a dynamic inverter-based comparator in [11] offers the benefit of simplicity and almost zero static power, the single-ended circuit is very sensitive to substrate and supply noise sources and PVT variations.

In the proposed design, a double AZ scheme is employed to resolve the comparator input crossing point issue while

avoiding the additional issues present in the topology as shown in Fig. 4(c). In Fig. 4(d), the AZ process is employed twice, once during Φ_{rst} and the other during Φ_{sig} . During the first AZ phase, the left terminal of C1 is connected to VPIXEL, while the right terminal is connected to common-mode voltage Vcm defined by the comparator with its first stage in unity gain feedback. The voltage across the capacitor, VPIXELrst-Vcm, together with the non-idealities to cancel is saved on C1. After the first AZ phase, the left terminal of C1 is switched to connect to VRAMP. VCP will follow the ramping down of VRAMP until it crosses with Vcm and then the comparator output flips. During the second AZ phase, the procedure is similar to that in the first AZ phase. The only difference is that now the voltage across the capacitor, VPIXELsig-Vcm, together with the non-idealities is saved on C1. After the second AZ phase, the left terminal of C1 is switched to connect to VRAMP, and the comparator output flips again when VCP crosses with Vcm. After digital CDS subtraction, the real pixel information level is VPIXELrst-VPIXELsig with the system non-idealities well canceled. With this method [28]–[30], the comparator only needs to be optimized around the input common-mode Vcm, which accommodates low supply voltage design in advanced technology nodes. The matching of C1 and C2 is less critical since the proposed approach does not rely on charge recombination; however, matching is still desirable for PSRR considerations. As the un-correlated sampling noise

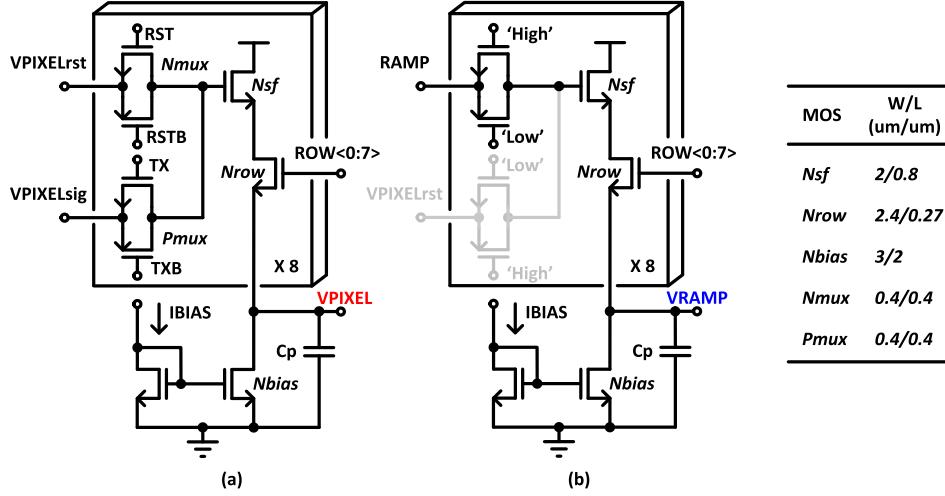


Fig. 5. (a) Pixel source follower. (b) Ramp buffer.

power gets doubled at final output after subtraction of the two samples converted during Φ_{rst} and Φ_{sig} , respectively, C1 and C2 still need to be sized large enough based on KT/C noise requirements.

IV. CIRCUIT IMPLEMENTATION

A. Pixel Source Follower/Ramp Buffer

To emulate one column of active pixel sensors in a multi-mega pixel array, a pixel source follower as shown in Fig. 5(a) is built with eight source follower unit cells, a column bias current mirror circuit, together with an additional capacitor of 8×64 fF added to mimic the loading from the rest of the source follower unit cells, which are not implemented in this prototype. The source follower unit cell consists of a source follower transistor, Nsf, a row selection transistor, Nrow, controlled by ROW $<0:7>$, and the input selection multiplexer, RST and TX, which are two non-overlapping digital signals that control the transmission gate multiplexer selecting VPIXELrst or VPIXELsig during Φ_{rst} or Φ_{sig} clock phases, respectively. The same topology in Fig. 5(b) enables the global ramp buffer (one for all columns) to track the pixel source follower over PVT and therefore reduce the demanded reset counting range and improve the INL performance of the digitizer. For the global ramp buffer, the multiplexer always passes the RAMP to the gate of Nsf and the same ROW $<0:7>$ controls which source follower unit cell to turn ON.

B. PW-Based Hybrid Digital Counter

The implementation and timing scheme of the proposed PW-based hybrid digital counter introduced in Fig. 3 are detailed in Fig. 6(a) and (b), respectively. The hybrid digital counter is built with a FLAG generation circuit and two counters containing an 8-bit reset counter and a 12-bit signal counter. The signal counter consists of a 4-bit LSB global counter combined with in-column LSB memory cells and 9-bit in-column MSB ripple counters. This segmentation of the signal counter is good enough for power saving considering

that the 5th-bit LSB of the conventional counter counts at a low speed that is 1/32 of its 1st-bit LSB counterpart.

For the global counter, synchronous gray-code and delay-line-based counter topologies are welcomed for their property wherein only a single bit changes from count-to-count [11], [25]. This feature enables power savings as the frequencies of LSB data buses are lowered. However, the proposed PW technique can push this benefit to its extreme by avoiding all unnecessary data transfer outside of predetermined small PW as shown in Fig. 6(b). In this design, a simple but robust synchronous binary counter based on half-adders and D-flip flops from a standard cell library is employed as the LSB global counter. As shown in Fig. 6(c), DATASTOP is generated using the LSB D-flip-flop of the ripple counter, which is already synchronized with the master clock (MCLK); hence a power-consuming circuit to synchronize the comparator output is avoided. However, to ensure a proper latching moment of LSB data into memory cells, the delay of the two paths, data signal path in blue and latch signal path in red, still needs to be properly controlled. The delay of buffers for four LSB data buses is made adjustable to compensate for the delay of the logic circuits, which only exists in the red path. In addition, special care has been taken on the 520 μm routing of MCLK together with the four LSB data buses to maintain their delay to the same column, Td1 and Td2, close to each other. Multiple global counters are required for readout of a complete multi-mega pixel readout circuits because the delay matching of clock and data buses at different frequencies cannot be guaranteed for long distance routing.

The reset counter is implemented using a ripple counter topology for the benefits explained in Section III. To cover the PVT variations on VPIXELrst, the reset counter needs resolution of 8 bit, which corresponds to 2.55 μs in time domain with T1 and T2 arranged to be equal. Since the reset counting time T is short (256 cycles), the power consumption is only a small portion of the entire digital counter, unlike the signal counter (4096 + 256 cycles). Instead of using a latch for its LSB counting [20], the reset counter still employs

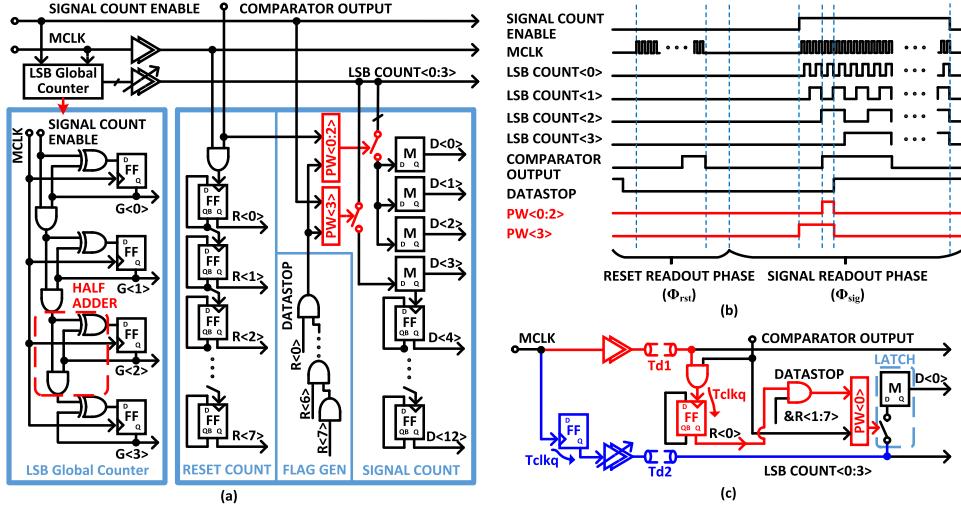


Fig. 6. Proposed digital counter. (a) Architecture. (b) Timing scheme. (c) Delay paths.

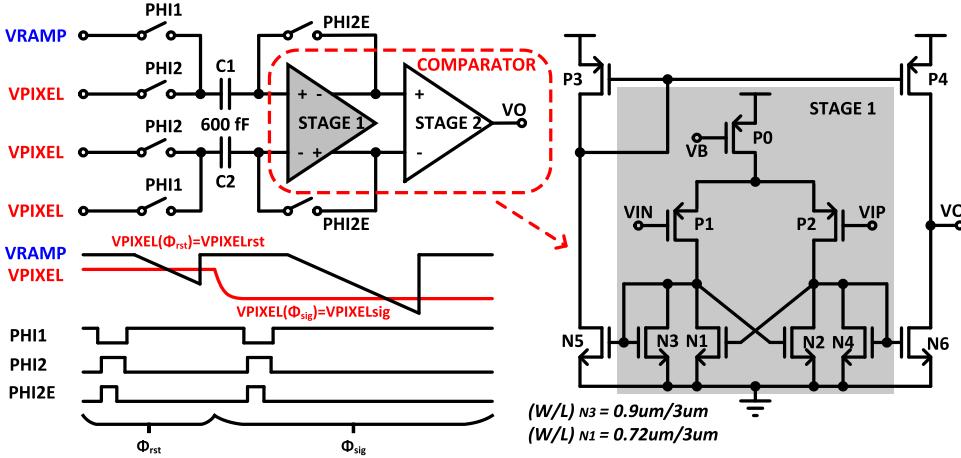


Fig. 7. Proposed comparator with double AZ scheme.

a D flip-flop for two reasons: 1) it offers better delay matching between the red and blue paths shown in Fig. 6(c) and 2) the latch can result in meta-stability issues depending on the comparator output flipping moment [11]. The outputs of the reset counter are sent to a cascading line of AND gates and DATASTOP signal is generated when the counter is at full count.

As shown in Fig. 6(b), PW(0:2) generated using comparator output together with DATASTOP is applied to control the connection of the last 3-bit LSB memory cells in the signal counter to their corresponding data buses. PW(3) for controlling the connection of the 4th-bit LSB memory cell to its data bus needs to be generated based on SIGNAL COUNT ENABLE and DATASTOP. This is because the memory cell needs to be all transparent to its input until DATASTOP is achieved so as to trigger and stop the column-based MSB ripple counter.

C. Double AZ Comparator

Fig. 7 shows the detailed implementation of the proposed comparator with double AZ scheme introduced in Section III-B. The topology in Fig. 4(d) is modified by

connecting the left terminal of C2 to V_{PIXEL} instead of ground to make the comparator fully symmetrical. Non-overlapping PHI1 and PHI2 controlled dummy switches are added between C2 and V_{PIXEL} to reduce non-idealities introduced by clock feedthrough and charge injection. The first stage of the comparator is implemented using a fully differential topology [23]. During the AZ phase, the comparator in unity gain feedback operates at a nominal common-mode voltage of 0.93 V, which is well-defined by the tail current and diode connected transistors N1-N4. The differential gain of the first stage is around 29.4 dB achieved by the cross-couple transistors N1 and N2. The high gain in the first stage relaxes the offset and noise requirement of the second stage. The first stage consumes 16 μ A current from a 2 V analog supply and achieves a bandwidth of around 8.46 MHz, which enables: 1) fast tracking and settling during the AZ phase and 2) small delay variation at different input crossing levels. Since only the first stage with a single pole at output is placed in closed loop during the AZ phase, closed loop stability is not an issue. The second stage possesses a lower bandwidth to help filter out some high frequency noise. The overall gain

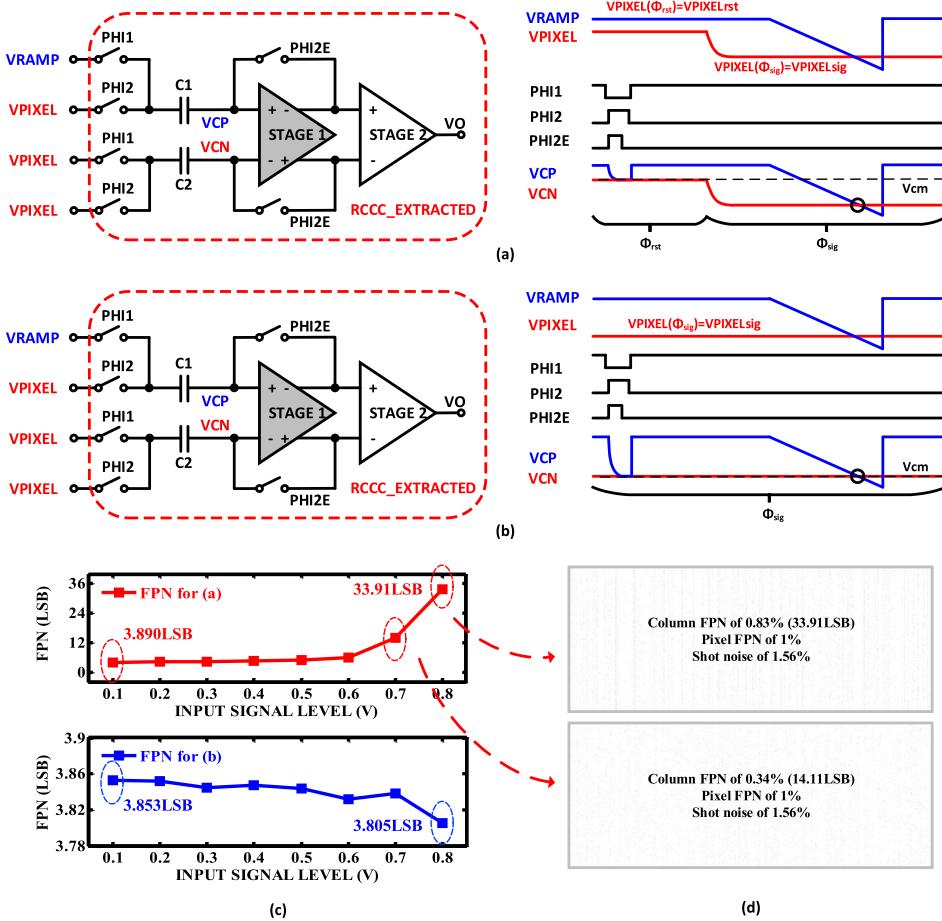


Fig. 8. Column FPN caused by comparator delay variations without CDS. (a) VCP/VCN does not cross at comparator common-mode voltage V_{cm} . (b) VCP/VCN crosses at comparator common-mode voltage V_{cm} . (c) Column FPN under various input signal levels for (a) and (b). (d) Sample images with column FPN of 0.83% (33.91 LSB) and 0.34% (14.11 LSB), respectively.

and bandwidth of the analog comparator is around 66.7 dB and 3.55 MHz, respectively.

To validate the concept of the proposed double AZ method, two test-benches simulating RCCC-extracted view of the transistor level comparator including all components shown in Fig. 7 are run under various timing schemes. In the first test-bench shown in Fig. 8, the AZ process is done only once for a single readout without CDS. The single AZ happens during Φ_{rst} as shown in Fig. 8(a); thus, the VCP/VCN does not cross at V_{cm} when realizing comparing the two signals. While in Fig. 8(b), a single AZ is completed during Φ_{sig} , and this time, when decision is made, the VCP/VCN crossing happens at V_{cm} . As shown in Fig. 8(c), the equivalent column FPN, caused by the comparator delay variations alone under different pixel information levels is characterized based on Monte-Carlo simulations with a global variation model. The column FPN for Fig. 8(a) goes up to 0.83% (33.91 LSB) and 0.34% (14.11 LSB) under an input signal level of 0.8 V and 0.7 V, respectively. This is caused by the fact that when a very low crossing voltage is applied to the comparator input, the differential pair consisting of P1 and P2 is too close to the triode region. Sample images under bright illumination with 1% pixel FPN, 1.56% shot noise, together with column FPN of 0.83% and 0.34% are shown in Fig. 8(d) and the

vertical strips are clearly noticeable. Nevertheless, the column FPN for Fig. 8(b) stays below 3.86LSB throughout the entire input signal range benefiting from the constant VCP/VCN crossing level. The second test-bench introduces the effect of CDS to the first test-bench as shown in Fig. 9. In Fig. 9(a), a single AZ is employed in Φ_{rst} and the topology becomes the same as shown in Fig. 4(b); thus, VCP/VCN crosses at V_{cm} for the reset readout, while remaining at a signal-dependent level for the signal readout. On the contrary, in the proposed double AZ scheme as shown in Fig. 9(b), VCP/VCN always crosses at V_{cm} . Fig. 9(c) shows that the column FPN is improved from 0.65% (26.78 LSB) to 0.004% (0.163 LSB) at the 0.8 V input level using the proposed double AZ method. Sample images in Fig. 9(d) further illustrate the effect of the proposed method in canceling out the noticeable strips under bright illumination conditions. With the help of CDS, the dark column FPN is improved from around 3.9 LSB to below 0.3 LSB.

D. Ramp Generator

The ramp generator in this design is implemented using a current-charging-capacitor topology as shown in Fig. 10. A switch controlled by the RAMP ENABLE signal is used to pull the RAMP voltage to its top value when necessary.

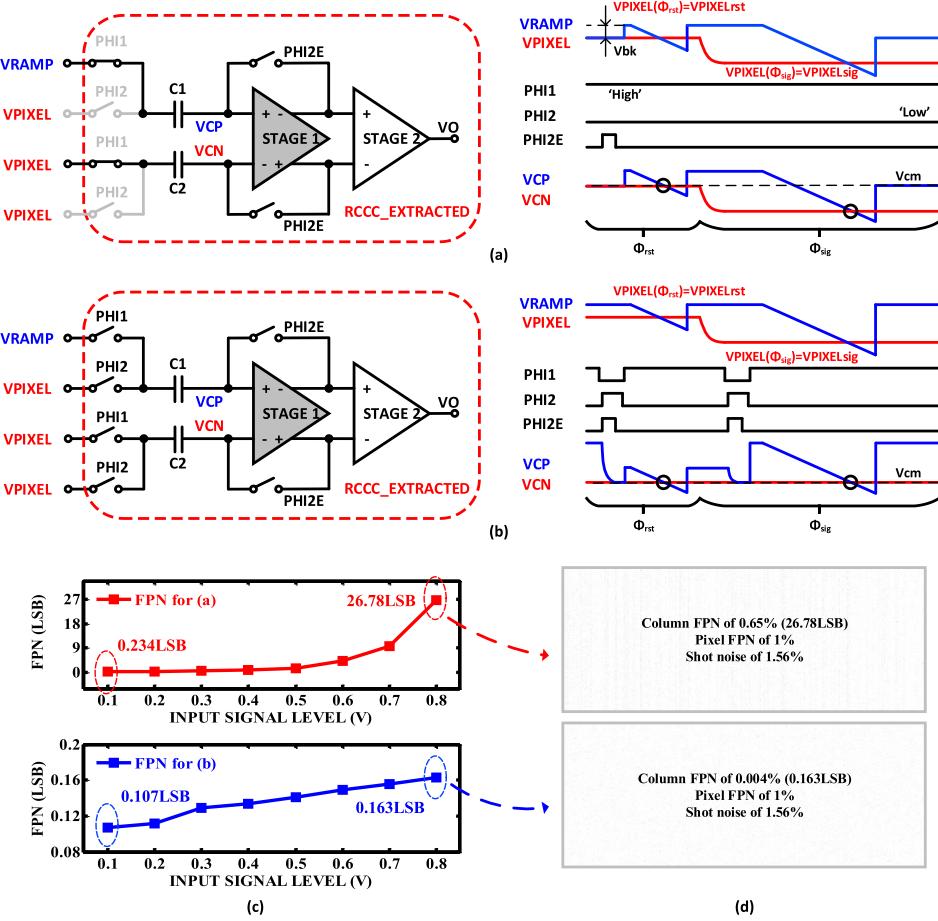


Fig. 9. Column FPN caused by comparator delay variations with CDS. (a) VCP/VCN does not cross at comparator common-mode voltage V_{cm} . (b) VCP/VCN crosses at comparator common-mode voltage V_{cm} . (c) Column FPN under various input signal levels for (a) and (b). (d) Sample images with column FPN of 0.65% (26.78 LSB) and 0.004% (0.163 LSB), respectively.

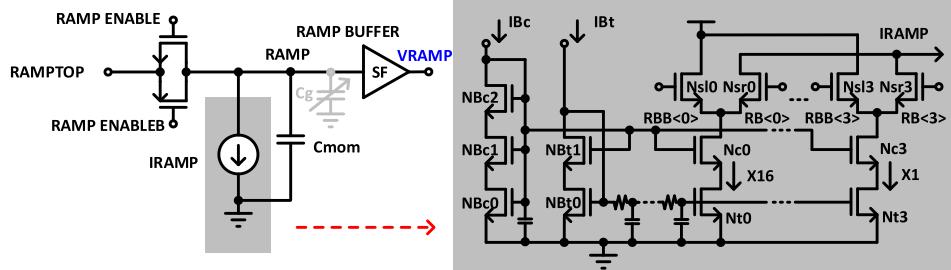


Fig. 10. Proposed ramp generator.

The capacitor is implemented using metal-oxide-metal (MOM) topology for its good linearity performance at the cost of relatively lower area efficiency. The current source is digitally controllable with 4-bit binary-weighted current branches for $\pm 100\%$ current control to compensate for the slope variations with PVT. The ‘‘High’’ voltage controlling the differential switches of the current branches is designed to be 1.8 V, so as to achieve high output impedance by cascading three transistors in saturation. A distributed RC filter is needed in front of the gate of the tail transistor in the current branches to filter out the noise from the bias circuitry.

V. MEASUREMENT RESULTS

The image sensor digitizer prototype is fabricated in 40 nm low-power CMOS process, and Fig. 11 shows the microphotograph of the chip. The SS-ADC array of the 96-column digitizer is implemented within a column pitch of 5.4 μ m and a vertical length of 325 and 290 μ m for the comparator and digital counter, respectively.

By emulating active pixels using external voltage sources together with on-chip pixel source followers and timing control, the entire readout chain including the pixel source follower and the digitizer is tested based on a single die in SS corner at room temperature. One horizontal scan for

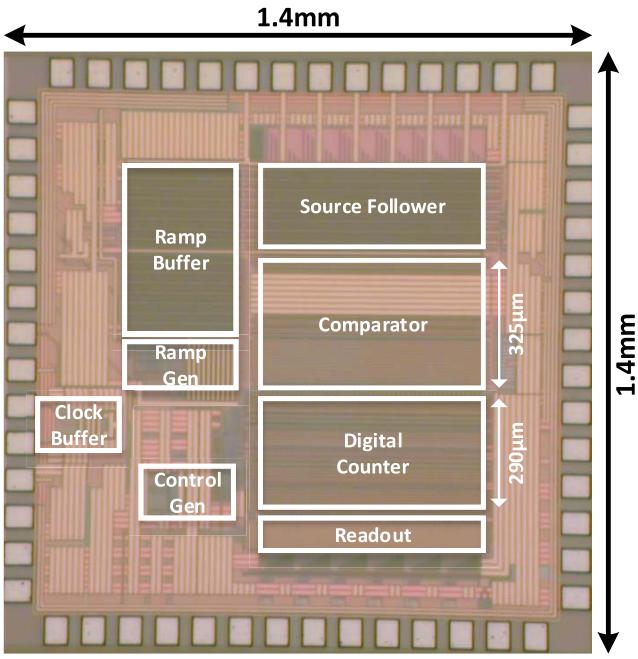


Fig. 11. Microphotograph of image sensor digitizer chip.

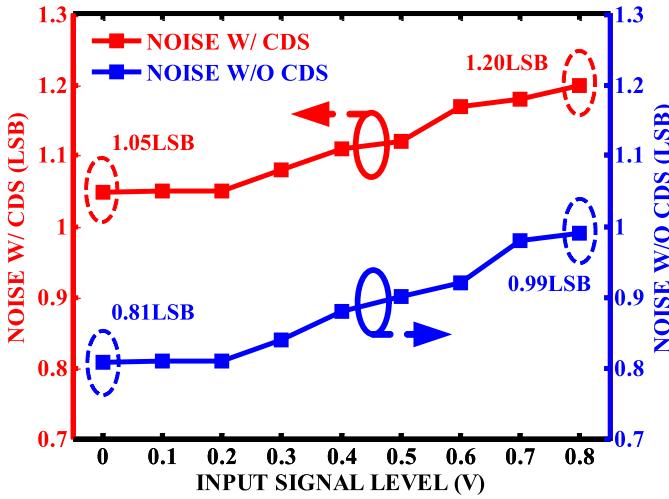


Fig. 12. Measured random noise performance.

the 12-bit digitizer is $6.02 \mu\text{s}$, while the proposed PW-based hybrid digital counter counts at 1.7 GHz. Although the double AZ timing scheme is fixed and not possible to bypass it in the implemented prototype, by setting VPIXELrst higher than VRAMP during the entire phase Φ_{rst} , the comparator will not flip and thus the reset read out is disabled. Benefiting from this setup, we are able to get measured data under no CDS condition for comparison purposes.

Fig. 12 shows the measured random noise performance of the designed image sensor readout array with and without the proposed CDS scheme, shown in red and blue, respectively. The random noise with CDS scheme is roughly $\sqrt{2}$ times higher than the same condition but without CDS over the entire input signal range, which is attributed to its double sampling behavior. Under a dark illumination condition, the random

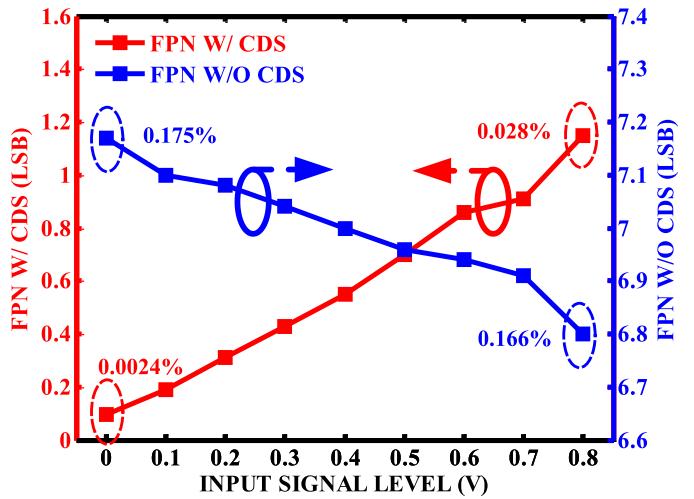


Fig. 13. Measured column FPN performance.

noise voltages through the entire readout chain are $261.5 \mu\text{V}$ and $202 \mu\text{V}$ with and without CDS, respectively. The dynamic range of the readout chain is calculated to be 71.8 dB without any column gain stages under CDS scheme.

Fig. 13 shows the measured column FPN performance of the designed image sensor readout array with and without the CDS scheme, shown in red and blue, respectively. In both the cases, the crossing happens at the AZ level, and the variation of column FPN with input signal level is very small. Combining the proposed double AZ scheme with the CDS scheme, the dark and bright column FPN performance of 0.0024% and 0.028% is achieved in this design. Fig. 14(a) and (b) show the DN distribution behavior of the 96 readout chains with a unified input level under dark illumination and bright illumination, respectively. By controlling “SIGNAL COUNT ENABLE” independently, the design can be improved to tolerate the condition when the image sensor has negative output level due to random noise.

Fig. 15 shows the measured linearity performance of the near-end and far-end column readout chain, shown in red and blue, respectively. The far-end column is expected to be the worst case with DNL and INL of $+0.32/-0.28$ LSB and $+4.21/-0.94$ LSB, respectively. The INL performance is believed to be limited by the linearity of the ramp. Even though linear MOM caps are used as the main capacitor for current charging, the non-linear gate capacitance from the ramp buffer degrades the INL performance.

Fig. 16 illustrates the power consumption of the column-parallel digital counter. In the conventional hybrid counter topology [11], [21], the most power demanding component is the signal counter which consumes $23.48 \mu\text{W}$ under bright illumination conditions. Nevertheless, with the proposed PW technique, this power can be reduced to $8.88 \mu\text{W}$ under the same condition. A power saving of 52.8% in the entire hybrid digital counter is obtained using the proposed PW technique without introducing any additional circuitry. As the design is not reconfigurable to disable PW, the detailed comparison of the power consumption of single-column counter with and without PW shown in Fig. 16 is based on post-layout simulations scaled to match the measured total power. As there

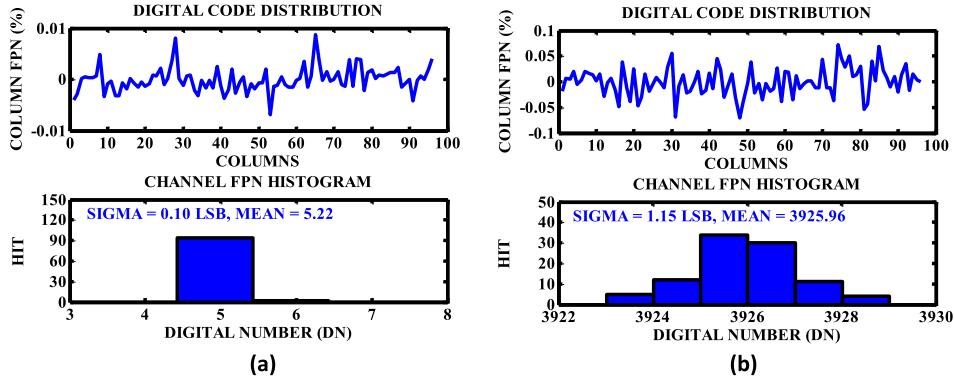


Fig. 14. Measured column FPN under condition of (a) dark illumination and (b) bright illumination.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE OF THE ART

	This Work	[2] VLSI 2015	[10] ISSCC 2016	[14] ISSCC 2012	[19] ISSCC 2015	[12] ISSCC 2016
Processss	40nm CMOS	180nm CMOS	65nm CIS/ 65nm CMOS	180nm CIS	180nm CMOS	40nm CIS/ 65nm CMOS
Power Supply	2.5V/2V/1.1V	3.3V/1.8V	2.5V/1.8V/1.2V	3.3V/1.8V	3.3V/1.8V	2.8V/2.5V/1.2V
Digitizer Topology	Column- Parallel SS	Column- Parallel SS	Column- Parallel PGA+SS	Column-Parallel CDS+2-Stage- Cyclic	32-Column- Shared CMR+SAR	Column-Parallel CDS+Cyclic- Cyclic-SAR
1 Horizontal Time (T_{lh})	6.02μsec	5μsec	10μsec	1.92μsec	1.85μsec	0.92μsec
ADC Conversion Time	2.7μsec	N/A	5μsec	1.92μsec	55.7nsec	0.92μsec
ADC Resolution (N)	12bit	11bit	11bit	12bit	12bit	12bit
ADC Area	5.4μm x 610μm	N/A	N/A	5.6μm x 1770μm	N/A	4.4μm x 920μm
Digital CDS	Y	Y	Y	N	N	N
DNL	+0.32/-0.28LSB	+0.26/-0.23LSB	N/A	+0.5/-0.7LSB	+6/-1.0LSB	+0.82/-0.88LSB
INL	+4.21/-0.94LSB	+7.5/-14.5LSB	N/A	+86/0LSB	N/A	+1.04/-11.75LSB
Column FPN	0.0024%(Dark) 0.028%(Bright)	N/A	N/A	0.31%(Dark) before off-chip calibration	N/A	N/A
Random Noise (V_n)	261.5μVrms (0dB Gain)	N/A	N/A	320μVrms (0dB Gain)	614.4μVrms (6dB Gain)	414μVrms (0dB Gain)
Dynamic Range (DR)	71.8dB	N/A	N/A	62.9dB	62.3dB	62.1dB
Per Column Power (P)	66.8μW	108μW	N/A	161μW	242.1μW	N/A
Total Breakdown	ADC(66.8μW)	N/A	PGA(32.5μW) S-CMP(4μW)	CDS(59.9μW) ADC(101μW)	CMR(134.3μW) ADC(107.8μW)	ADC(120μW)
FoM1 ^a [V·pJ]	0.105	N/A	N/A	0.099	0.275	N/A
FoM2 ^b [V·fJ/step]	0.026	N/A	N/A	0.024	0.134	N/A
FoM3 ^c [dB]	162.75	N/A	N/A	154.9	152.8	N/A

^a FoM1 = $P \cdot V_n \cdot T_{lh} \cdot 10^{12}$ [V·pJ] (Image Sensor FoM1 from [12])^b FoM2 = $P \cdot V_n \cdot T_{lh} \cdot \text{Gain} \cdot 10^{15}/2^N$ [V·fJ/step] (Image Sensor FoM2 from [12])^c FoM3 = $\text{DR} + 10\log_{10}(1/(2 \cdot T_{lh} \cdot P))$ [dB] (Schreier ADC FoM3)

is no dedicated supply for each block, the power consumption values shown for signal counter, reset counter and FLAG GEN are calculated based on their percentage attained from post-layout simulations and measuring the total power consumption of single column counter.

Fig. 17 shows the power breakdown of a single-column digitizer with a total power of 66.8 μW. For the global counter, the ramp and ramp buffer, their equivalent single-column power is calculated by dividing their entire power over the number of columns. In this design, the column comparator

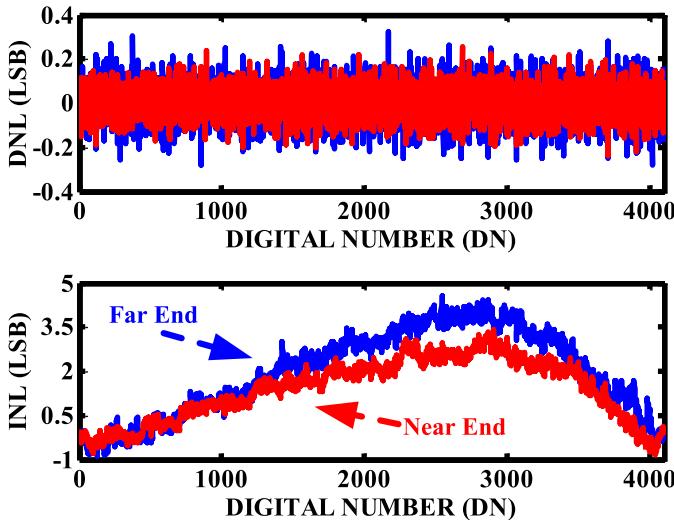


Fig. 15. Measured linearity performance.

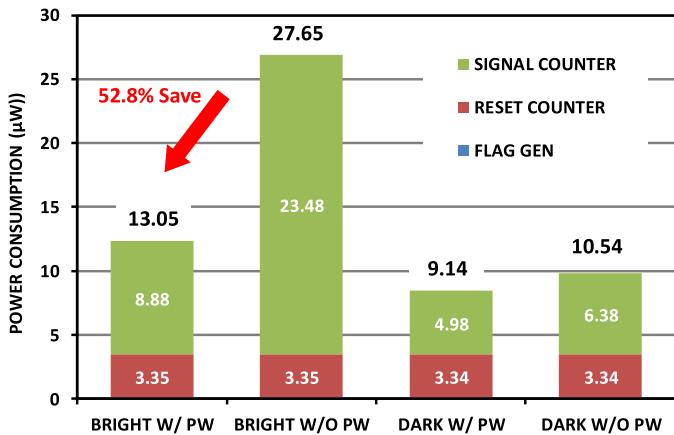


Fig. 16. Power consumption of single-column digital counter.

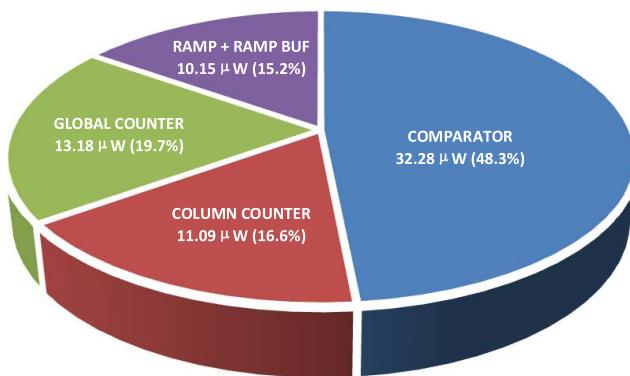


Fig. 17. Power breakdown of single-column digitizer.

power dominates as it is a conservative design still covering a full-scale input signal level range.

Table I summarizes the performance of the implemented image sensor digitizer. Single-column-wise comparison with the state-of-the-art implementations for image sensors can be made even though this design does not include an entire multi-megapixel readout array. For fair comparison purposes, only the ADC power is considered. Compared with the cyclic/SAR

ADC-based implementations in [12], [14], and [19], the proposed design appears to be slower as additional time is needed for completing the digital CDS procedure. Nevertheless, the proposed digitizer achieves high dynamic range, the lowest per-column power consumption, the smallest area, and competitive Schreier FOM of 162.75 dB.

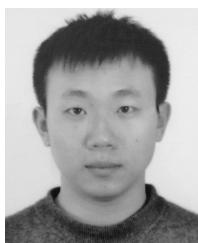
VI. CONCLUSION

A 66.8μ W-per-column image sensor digitizer based on SS-ADC topology was designed and implemented in a 40 nm low-power CMOS process. The proposed PW technique enables a power saving of 52.8% in the hybrid digital counter, while maintaining the capability of completing digital CDS in column. A dark/bright column FPN of 0.0024%/0.028% from the readout circuit is achieved with the proposed double AZ technique without any off-chip processing. The proposed design achieves low readout noise and a wide dynamic range of 71.8 dB without any column gain stages. The proposed techniques are suitable for readout of back-illuminated 3-D-stacked CMOS image sensor pixel array and exportable to other architectures.

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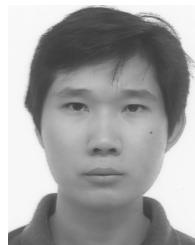
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