A 100 MHz Hybrid Supply Modulator With Ripple-Current-Based PWM Control

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***Abstract*— This paper presents a 100 MHz hybrid supply modulator (HSM) with ripple-current-based pulse width modulation (PWM) control. By sensing the ripple current, a ripple current sensor (RCS) is able to overcome the bandwidth limitation of an absolute current sensor. By leveraging the RCS, we propose a large-signal PWM control method for HSMs. This method has an intrinsically fast switching loop, and thus eliminates the need for the feed-forward path used in many previous designs. The possibility of generating high-order harmonics in PWM-controlled HSMs is pointed out for the first time, and design recommendations to avoid them are presented. A very-high-frequency triangular wave generator that is robust to both process-voltage-temperature (PVT) variations and device mismatches is proposed. A proof-of-concept prototype was fabricated in CMOS 130 nm technology. Switching at 100 MHz, this HSM is able to track a 0.8 V_{pp} sinusoidal waveform up to 13 MHz with high fidelity. It achieves a peak efficiency of 88.2% at the maximum output power of 23 dBm. To the best of our knowledge, this is the first PWM-controlled HSM that is able to operate at 100 MHz.**

***Index Terms*— Current sensor, envelope tracking, hybrid supply modulator (HSM), polar amplifier, power amplifier (PA), PWM control, ripple current sensor (RCS), very high frequency (VHF).**

I. Introduction

SUPPLY modulator is one of the key building blocks in supply-modulated RF power amplifiers (PAs) [1], [2]. An ideal supply modulator is expected to track wideband envelope signals with high efficiency, high linearity, and small output voltage ripple. It is quite challenging for conventional linear regulators or switching regulators to meet these requirements simultaneously. Linear regulators offer high linearity and small output voltage ripple, but suffer from poor efficiency. Switching amplifiers achieve high efficiency, but have poor linearity and large output voltage ripple. By combining a wideband linear amplifier (LA) and a high-efficiency switching stage in parallel, a hybrid supply modulator (HSM) could achieve an optimized tradeoff between efficiency, linearity, and output voltage ripple. As shown in Fig. 1, an HSM splits the load current I_{sm} between the switching stage and the LA. By controlling the switching stage to supply the majority of the load current, an HSM is able to achieve much higher efficiency than using the LA alone. Furthermore, the LA enables the HSM to achieve better linearity and wider bandwidth than using the switching stage alone. There are two main control methods used in previous designs, namely hysteretic control [3]–[6] and and pulse width modulation (PWM) control [7]–[9]. The hysteretic control offers a very fast switching loop but has a variable switching frequency and cannot support multiple switching phases. In contrast, the PWM control is able to support multiple switching phases and offers a fixed switching frequency, but is generally considered to have a slower loop response [8], [9].

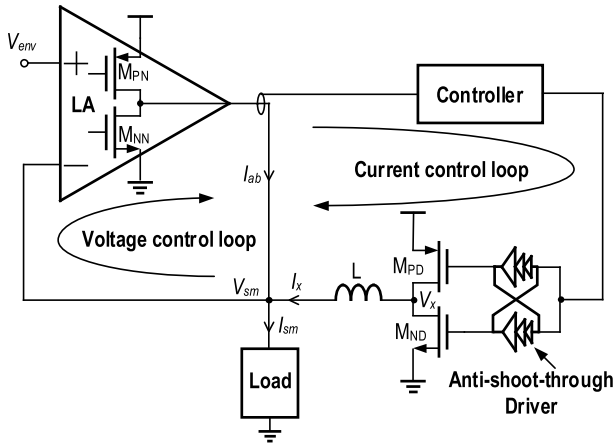

Fig. 1. Conceptual diagram of a generic HSM.

Designing an HSM involves the tradeoff between efficiency, linearity, and output voltage ripple. For wideband applications, its efficiency depends on the inductor value L and the switching frequency f_{sw}. Using a small L increases the slew rate of the HSM, but results in large ripple current that is detrimental to efficiency. Switching an HSM in the very high frequency (VHF, 30–300 MHz) range reduces the ripple current, but brings additional design challenges. For a hysteretic-controlled HSM, its f_{sw} is limited by the bandwidth of its current sensor, and most previous designs switch below the VHF range [5]–[10]. Reference [3] achieved a maximum f_{sw} of 118 MHz, but its current sensor is only able to sense positive current, and thus, its LA delivers only positive current in the steady state, degrading the efficiency [11]. For an HSM with PWM control, the stability of the switching loop has to be considered [7]–[9]. Furthermore, the design of the VHF synchronization waveform is very challenging. To increase the speed of the switching loop, a feed-forward path is required in some previous works [8], [9], increasing the design complexity

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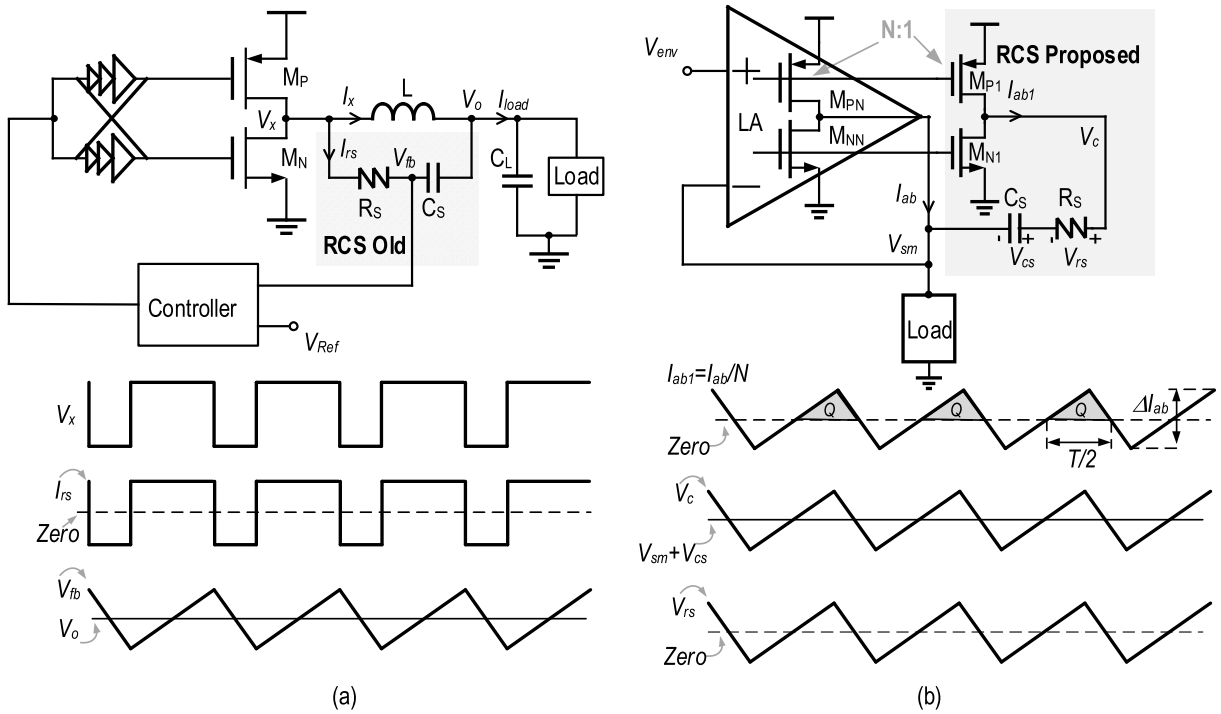

Fig. 2. (a) Previous RCS for sensing inductor current ripple and its steady-state waveforms. (b) Proposed RCS for sensing LA current ripple and its steady-state waveforms.

greatly. Due to these reasons, the switching frequencies of the PWM-controlled HSMs in the literature are below the VHF range [7]–[9].

In this paper, we present a ripple-current-based PWM control method to address the aforementioned challenges. The ripple-current-based control has been used in switching converters [12], [13]. It is a large-signal control method that is able to overcome the bandwidth limitation of an absolute current sensor (ACS). Despite the attractiveness of ripple-based control, adapting it to the HSMs is not trivial. The remainder of this paper is organized as follows. Section II discusses the ripple current sensor (RCS). Section III presents the proposed control method, discusses the origin of high-order harmonics, and details the implementation of a novel VHF triangular wave generator. Section IV presents the measurement results, and Section V concludes our design efforts.

II. Ripple Current Sensor

In many designs, the current information of a device has to be converted into a voltage by a current sensor for further processing. Depending on the content of the sensed information, current sensors fall into two categories, namely ACS [14] and RCS [12]. For an ACS, the sensed voltage V_{sen} is a scaled version of the current (I_d) being sensed, that is, $V_{\text{sen}}(t) = \alpha \times I_d(t)$ for some constant α. Although an ACS gives complete current information of a device, its speed and accuracy are limited by the associated active devices. Although using passive devices is possible, this approach usually consumes more power and is not preferred. In many applications, the current may change by several orders of magnitude, and the associated ACS is required to have a wide sensing range. Due to these limitations of the ACSs, the state-of-the-art current-mode PWM-controlled buck converter using an ACS is only able to switch at 5 MHz with a limited duty-ratio range of 0.6 [15]. An RCS differs from an ACS in that it provides only the ripple information but not the dc value of the current, and the required sensing range is therefore much reduced. For an RCS, the sensed voltage ripple $\Delta V_{\text{sen}}(t)$ is a scaled version of the current ripple $\Delta I_d(t)$, that is, $\Delta V_{\text{sen}}(t) = \beta \times \Delta I_d(t)$ for some constant β. An RCS can be easily implemented with passive devices, enabling much faster speed than the ACS counterpart. The comparison between these two types of current sensors is summarized in Table I. In the literature, the RCS-based switching converter is reported to achieve a switching frequency of 233 MHz [12]. As an RCS can switch in the VHF range, while an ACS cannot, one may consider using an RCS in the VHF HSMs. One RCS that draws considerable attention is the series *RC* RCS [12]. As shown in Fig. 2(a), by connecting a series *RC* network across the inductor of a buck converter, the ripple current of the inductor can be sensed. The operating principle is briefed as follows [16]. In the steady state, the output voltage V_o is regulated to the reference voltage V_{Ref}. In State 1, $V_x = V_{\text{DD}}$, and $V_{\text{fb}}(t)$ is charged up toward V_o; while in State 2, $V_x = 0$, and $V_{\text{fb}}(t)$ is discharged toward ground. As the time constant $C_s R_s$ is much larger than the switching period T, the charging and discharging slopes are

TABLE I
Comparison Between ACS and RCS

ACS: $V_{sen}(t)=\alpha \times I_d(t)$	RCS: $\Delta V_{sen}(t)=\beta \times \Delta I_d(t)$
1. Large sensing range.	1. Reduced sensing range.
2. Often implemented by active devices.	2. Implemented by passive devices.
3. Limited bandwidth.	3. Wide bandwidth.

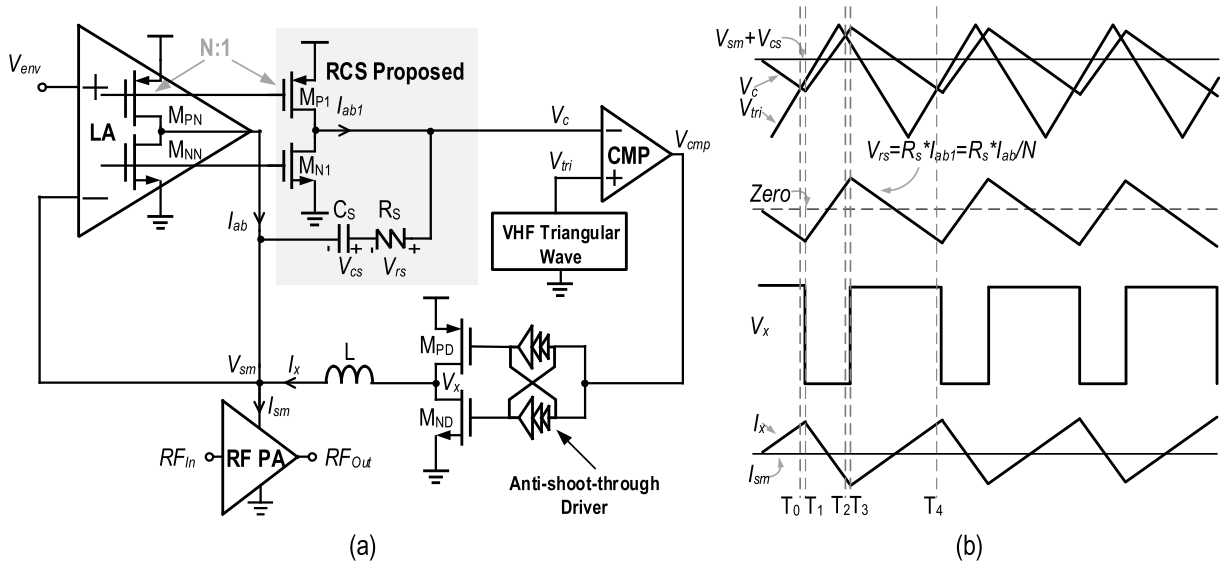

Fig. 3. (a) Conceptual diagram and (b) steady-state operating waveforms of the proposed design.

approximately linear. Simple computation shows that the rising slope is $(V_{\rm DD}-V_o)/(C_sR_s)$, and the falling slope is $-V_o/(C_sR_s)$. They differ from the inductor current slopes, $(V_{\rm DD}-V_o)/L$ and $-V_o/L$, by a scaling factor only. Hence, the ripple of $V_{\rm fb}$ is roughly a scaled version of the ripple of I_x. As only passive devices are used, its speed is no longer limited by the bandwidths of active elements, and the VHF operation is therefore possible.

Despite its effectiveness and simple implementation, the series *RC* RCS cannot be deployed in the HSMs directly as the HSMs use the LA current rather than the inductor current for control. Fortunately, after minor modifications, the series *RC* RCS can be used to sense the ripple current of an LA. Fig. 2(b) shows the block diagram of the proposed RCS and its steady-state waveforms. In this RCS, a series *RC* network is connected between the output of a transistor pair and the output $V_{\rm sm}$. The transistor pair is matched to the last stage of the LA with a ratio of $1{:}N$ such that $I_{\rm ab1} = I_{\rm ab}/N$. We assume that in the steady state, the average current of the LA is roughly zero, and the dc voltage of $V_{\rm cs}$ is fixed by a negative-feedback network. These assumptions will be shown to hold in Section III. By using a relatively large C_s, the ripple voltage $\Delta V_{\rm cs}$ on C_s can be made much smaller than the maximum sensed voltage $V_{\rm rs}(\max)$ across R_s, and $V_{\rm rs}$ is then roughly a scaled version of the ripple current $I_{\rm ab}$ from the LA. From the waveforms shown in Fig. 2(b), we can calculate the ripple voltage $\Delta V_{\rm cs}$ as

$$\Delta V_{\rm cs} = \frac{Q}{C_s} = \frac{\Delta I_{\rm ab}}{8Nf_{\rm sw}C_s} \tag{1}$$

where $\Delta I_{\rm ab}$ is the magnitude of the ripple current. If $\Delta V_{\rm cs}$ is much smaller than $\Delta V_{\rm rs}$, then we have

$$\Delta V_{\rm cs} = \frac{\Delta I_{\rm ab}}{8Nf_{\rm sw}C_s} \ll \Delta V_{\rm rs} = \frac{\Delta I_{\rm ab}R_s}{N}. \tag{2}$$

From (2), by ensuring that

$$C_s \gg \frac{1}{8}\frac{1}{f_{\rm sw}R_s} \tag{3}$$

the effect of $\Delta V_{\rm cs}$ on the accuracy of our proposed RCS is negligible. For robustness considerations, we need to account for PVT variations in determining the values of C_s and R_s. In general, C_s can be connected to any node that is ac ground. To save area, we may connect C_s to ground, and implement it as an MOS capacitor. To further reduce the value of C_s, a larger matching ratio N and/or a higher switching frequency can be used. Note that the resistor R_s directly senses the ripple current of the LA. This is different from the conventional RCS [12], [16], where the sensed ripple current information is obtained by integrating the current through the resistor.

III. Ripple-Current-Based PWM Control

By incorporating the RCS discussed in Section II into an HSM, we propose a ripple-current-based PWM control method for the HSMs. We discuss its operating principle and show that it is able to maintain a high-speed switching loop without using any feed-forward path. Furthermore, we study the mechanism of the generation of high-order harmonics, and provide design recommendations to avoid them. We also detail the implementation of the VHF triangular wave generator.

A. Operating Principle

The key idea of the proposed ripple-current-based PWM control method is to use the ripple current instead of the absolute current of the LA for control. More specifically, an RCS converts the ripple current of the LA into a control voltage V_c that is then compared with a synchronization waveform to modulate the duty ratio of the PWM waveform. Fig. 3(a) shows the block diagram of the proposed control method. The switching loop consists of an RCS, a high-speed comparator (CMP), a VHF triangular wave generator, an anti-shoot-through driver, a pair of power switches $M_{\rm PD}$ and $M_{\rm ND}$, and an inductor L. The matching ratio N of the RCS is chosen to be 80 and the magnitude of the triangular wave is designed to be 0.8 V.

Fig. 3(b) shows the steady-state operations of our design. We denote the synchronization waveform as $V_{\rm tri}$, the control

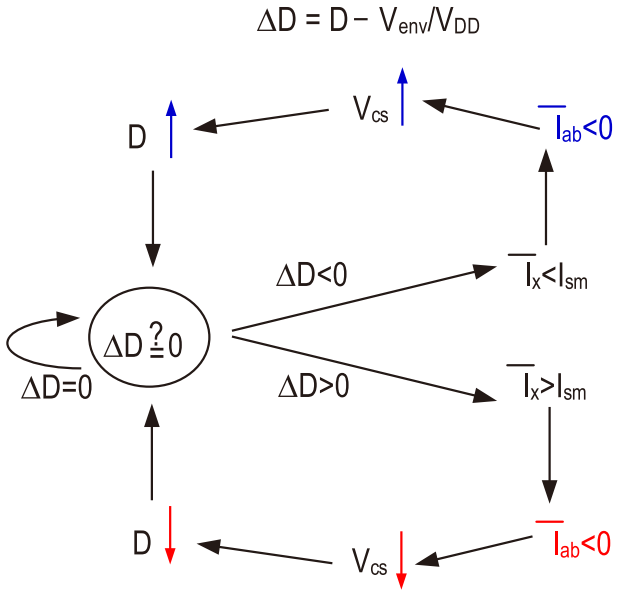

Fig. 4. Regulation of duty-ratio D with large-signal negative feedback.

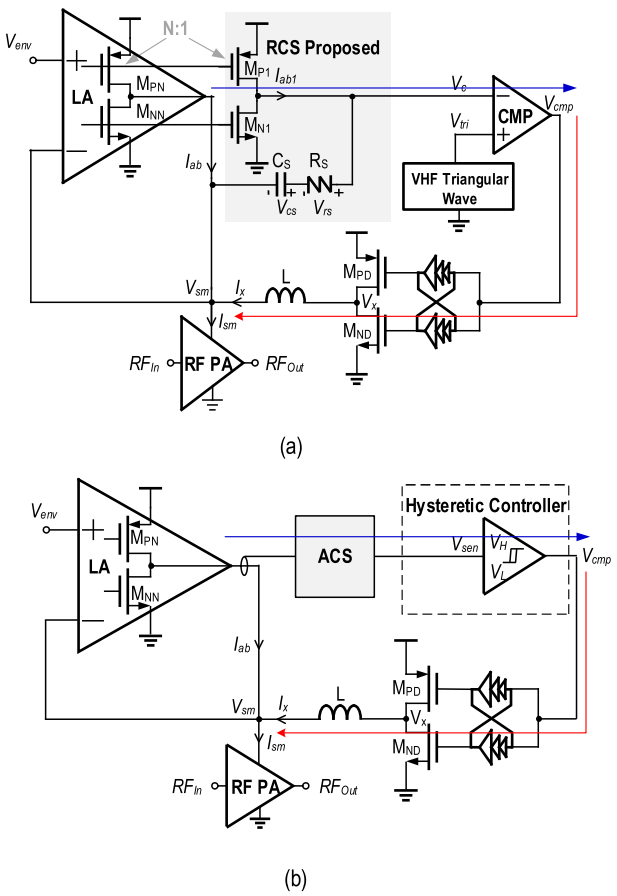

Fig. 5. Switching-loop signal path for an HSM with (a) ripple-current-based PWM control and (b) hysteretic control.

voltage as V_c, the comparator output as $V_{\rm cmp}$, the output current of the LA as $I_{\rm ab}$, the voltage across the sensing resistor R_s as $V_{\rm rs}$, and the voltage across the capacitor C_s as $V_{\rm cs}$. In the steady state with a fixed envelope voltage $V_{\rm env}$, the HSM ensures that the output voltage of the HSM $V_{\rm sm}$ follows $V_{\rm env}$ closely, thus creating a constant load current $I_{\rm sm} = V_{\rm env}/R_L$. The switching loop supplies most of the load current, and the LA cancels the ripple content from the switching loop. The controller splits $I_{\rm sm}$ between the two control loops. The detailed operations proceed as follows. Just before T_0, the power switch $M_{\rm PD}$ is ON, and $M_{\rm ND}$ is OFF, I_x ramps up, $I_{\rm ab}$ ramps down, and so does V_c, which is the output of the RCS. The moment V_c drops below $V_{\rm tri}$, and the comparator trips high. After the switching-loop delay, at T_1, $M_{\rm PD}$ is turned off and $M_{\rm ND}$ is turned on, I_x ramps down, and $I_{\rm ab}$ and V_c ramp up, until V_c hits $V_{\rm tri}$ at T_2 when the comparator trips low. After the switching-loop delay, at T_3, $M_{\rm PD}$ is turned on and $M_{\rm ND}$ is turned off, I_x ramps up, and $I_{\rm ab}$ and V_c ramp down, until V_c hits $V_{\rm tri}$ again at T_4. The operation then starts to repeat and a large-signal negative-feedback loop is established. We will explain this feedback mechanism in more detail by using Fig. 4 in the next paragraph. As V_c returns to the same value after each cycle, the net charge accumulated on C_s is zero, so does the average current of $I_{\rm ab1}$. It follows that the average current of $I_{\rm ab}$ is also roughly zero.

For switching converters with the ripple-current-based control, the dc voltage of $V_{\rm fb}$ has to be defined in the steady state. This is accomplished via its global feedback control loop [12]. Similarly, we also need to define the dc voltage of $V_{\rm cs}$. This is achieved via a large-signal negative-feedback mechanism. Meanwhile, this feedback mechanism fixes the duty ratio D of the PWM waveform to be $V_{\rm env}/V_{\rm DD}$. Let us consider the case when D is greater than $V_{\rm env}/V_{\rm DD}$. In this case, the magnitude of the inductor current during the rising period, which is equal to $|+m_1{\rm DT}|$, is larger than that during the falling period, which is equal to $|-m_2(1\text{-D})T|$, where m_1 and $-m_2$ are the rising and falling slopes of the inductor current, respectively, and T is the switching period. As a result, the inductor current $I_x(t)$ will increase after each cycle. As the average inductor current $\bar{I}_x$ becomes larger than $I_{\rm sm}$, the LA has to sink the extra charge from the switching loop in order to ensure a fixed output voltage. As the net charge from the LA during each cycle becomes negative, the accumulated charge on C_s is reduced, thus lowering the dc level of V_c and decreasing the duty ratio D of the PWM waveform. As this process continues, D will eventually return to its steady-state value $V_{\rm env}/V_{\rm DD}$, forcing $\bar{I}_x$ to be the same as $I_{\rm sm}$. As a result, the average current of $I_{\rm ab}$ is forced to be zero when the HSM is working in the steady state. As $I_{\rm ab1}$ is a scaled version of $I_{\rm ab}$, the net charge accumulated on C_s during each cycle is also zero and the dc value of $V_{\rm cs}$ stays constant in the steady state. The case when D is initially smaller than $V_{\rm env}/V_{\rm DD}$ can be analyzed similarly. The operations of this large-signal negative-feedback loop are summarized in Fig. 4. For different input voltages, the control waveform V_c will move up or down to modulate the width of the PWM waveform, therefore generating the desired duty ratio $V_{\rm env}/V_{\rm DD}$. Measurement results will be provided in Section IV to consolidate our theoretical analysis.

Previous PWM-controlled HSMs all use small-signal-based control [7]–[9], and the bandwidth of the switching loop is limited to be much lower than the switching frequency. In contrast, our proposed control scheme is a large-signal-based design, and the speed of its switching loop is no longer

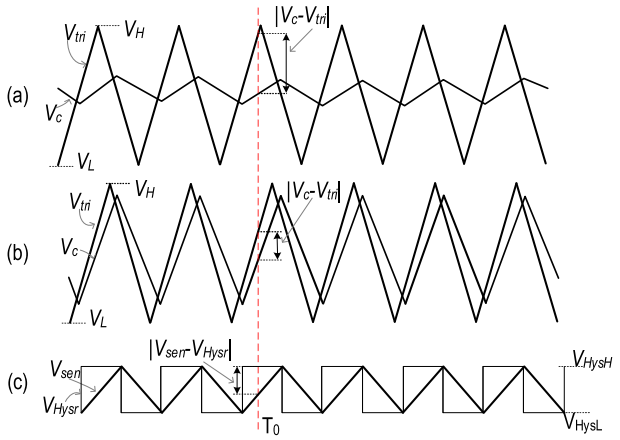

Fig. 6. Comparator input voltage difference of the proposed design with (a) small R_s, (b) large R_s, and (c) hysteretic-controlled HSM.

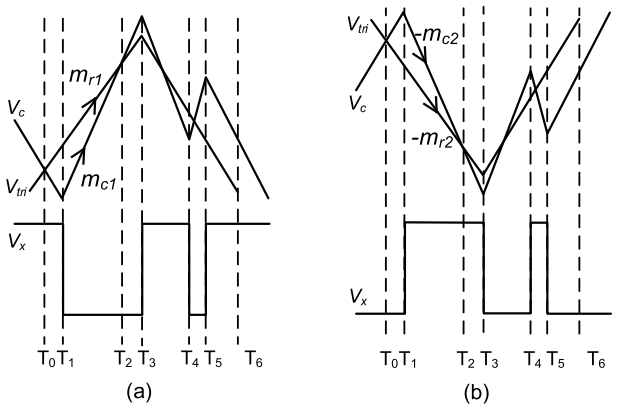

Fig. 7. Generation of high-order harmonics at (a) rising edge of T_{tri} and (b) falling edge of T_{tri}.

limited by the switching frequency. As such, no feed-forward path is needed. Analysis shows that with an optimized R_s, the speed of the switching loop of this design can be made comparable to that of a hysteretic-controlled HSM. To illustrate this point, we only need to consider the speed of the signal path starting from the LA output to the comparator output, as the rest of the signal path along the switching loop is the same for both control methods. This is shown in Fig. 5. Assuming that the ACS in a hysteretic-controlled HSM and the RCS in our proposed design have the same bandwidth, we are left to consider the speed of the signal path starting from the output of the current sensor to the output of the comparator. For large-signal-based designs, the input voltage difference of the comparator has to reduce from $|V_c{-}V_{\text{tri}}|$ to zero before the comparator starts to flip as shown in Fig. 6. Fig. 6(a) and (b) shows the steady-state waveforms of V_{tri} and V_c for a small R_s and a large R_s, respectively. Apparently, using a larger R_s is able to reduce $|V_c{-}V_{\text{tri}}|$. Nevertheless, R_s cannot be made too large as will be discussed in Section III-B. For hysteretic control, the ACS converts the current of the LA into a voltage V_{sen} that oscillates between the upper bound V_{HysH} and the lower bound V_{HysL} of the hysteretic comparator, as shown in Fig. 6(c). At T_0, the input voltage difference of the comparator is $|V_{\text{sen}}{-}V_{\text{HysH}}|$. For hysteretic control, the ACS converts the current of the LA into a voltage that has to travel all the way to either

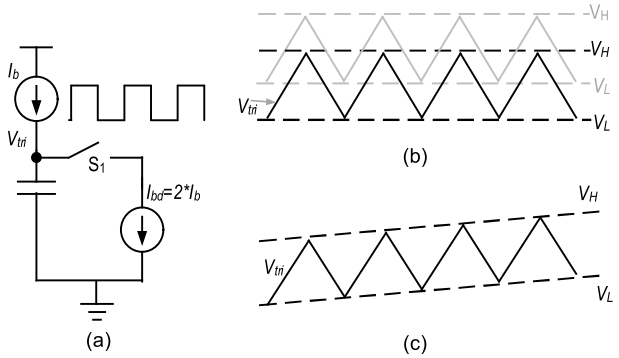

Fig. 8. Triangular wave generation using half duty-ratio clock signal. (a) Block diagram. (b) Problem with drifting V_H and V_L. (c) Problem with current mismatch ($I_{\text{bd}} < 2I_b$).

V_{HysH} or V_{HysL} to trip the comparator, while in our proposed design with an optimized R_s, V_c tracks V_{tri} closely and needs to travel only the voltage difference of $|V_c{-}V_{\text{tri}}|$ to trip the comparator. Given that the RCS and the ACS have similar bandwidth, if the voltage difference $|V_c{-}V_{\text{tri}}|$ is comparable to the hysteresis $|V_{\text{HysH}}{-}V_{\text{LysL}}|$, then the switching-loop speed of the proposed design becomes comparable to that of the hysteretic control counterpart. Our control method thus offers an intrinsically fast switching loop that eliminates the need of using the feed-forward path as in the previous designs that have a slow switching loop. With the help of Fig. 5, we can show that the duty ratio of the switching stage is able to change to 0 or 1 within one cycle. Considering a sudden step-up input, the LA has to provide a large current before the switching loop can respond. As V_{rs}, the voltage across R_s, is proportional to I_{ab}, it increases immediately. If the change of V_{rs} (i.e., ΔV_{rs}) exceeds $|V_c{-}V_{\text{tri}}|$, then D goes to 1 immediately. This can be accomplished by using a large R_s that results in a small $|V_c{-}V_{\text{tri}}|$. The case of a sudden step-down input can be analyzed similarly.

B. High-Order Harmonics

It is observed that the proposed design may switch more than once within one cycle of the synchronization waveform, thereby generating high-order harmonics. The simplified steady-state waveforms that illustrate this situation are shown in Fig. 7(a) and (b) for the rising edge and the falling edge cases of V_{tri}. Let us consider Fig. 7(a) first. The comparator is triggered at T_0, and after the switching-loop delay, it is flipped at T_1 when the driver turns off M_{PD} and turns on M_{ND}. Then, I_x ramps down and I_{ab} ramps up to cancel the change of I_x so as to maintain a constant I_{sm}. As I_{ab} ramps up, so does V_c, whose change is proportional to the ripple current of I_{ab}. Assuming a constant V_{cs}, then V_c is a piecewise linear curve, and its rising slope m_{c1} is determined by the falling slope of I_x, the matching ratio N, and the sensing resistor R_s. Let m_{r1} denotes the rising slope of V_{tri}. If m_{c1} is larger than m_{r1}, then V_c runs into the risk of hitting V_{tri} more than once during each cycle. In Fig. 7(a), V_c eventually hits V_{tri} at T_2. To avoid this situation, we would like to make the slope of V_c smaller than that of V_{tri}. The falling slope case can be analyzed in a similar fashion. In Fig. 7(b), denoting the falling slope of V_c and V_{tri} by $-m_{c2}$ and $-m_{r2}$,

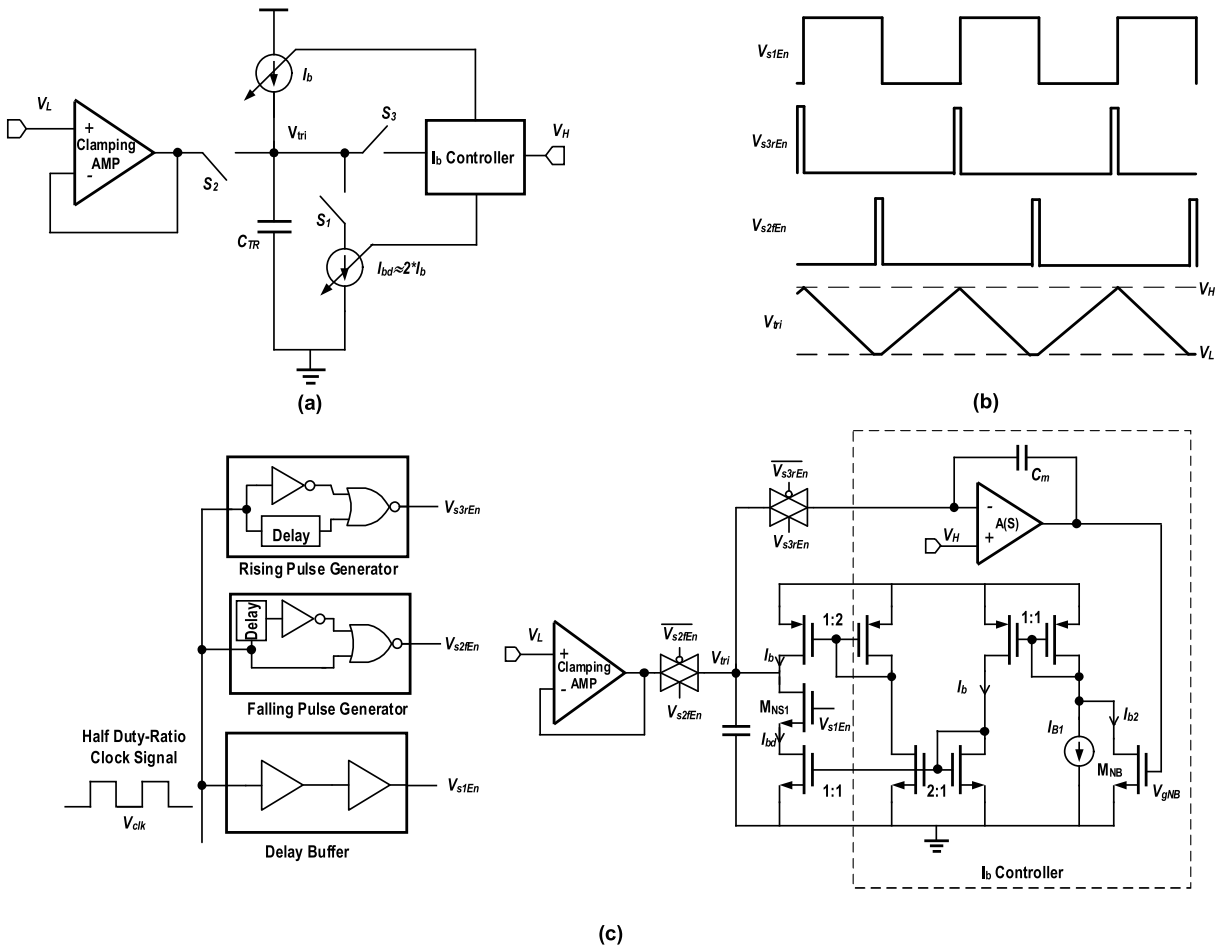

Fig. 9. Proposed VHF triangular wave generator. (a) Simplified block diagram. (b) Timing waveforms. (c) Circuit implementation.

respectively, we can avoid high-order harmonics during the rising period of I_x by ensuring that m_{r2} is always larger than m_{c2}. From Fig. 7(a) and (b), we conclude that the rising slope and falling slope of the synchronization waveform are equally important in avoiding high-order harmonics. Therefore, a symmetrical triangular synchronization wave is preferred. Note that the switching-loop delay increases the separation between V_c and V_{tri} at T_1, and $m_{c1}(m_{c2})$ does not always need to be smaller than $m_{r1}(m_{r2})$. In practice, this parameter is more conveniently determined by computer simulations. Using a high switching frequency allows the use of a larger R_s, resulting in better dynamic efficiency and faster switching loop as discussed in Section III-A. For performance optimization, we would like to choose the largest R_s without causing high-order harmonics. For a 100 MHz 0.8 V_{pp} triangular synchronization signal with $C_s = 22$ pF, simulations show that high-order harmonics can be avoided if R_s is smaller than 10 kΩ for an output voltage ranging from 0.15 to 1 V.

C. Circuit Implementations

For the proposed HSM, we optimize the three-stage Class-AB LA in [11] that uses cascode Miller compensation [17] in the outer compensation loop and *RC* Miller compensation in the inner compensation loop. This LA achieves a unity-gain frequency of 700 MHz. The quiescent current of the LA is 4.2 mA, and it is able to sink and source 100 mA current.

Next, we discuss the design of the VHF triangular waveform generator. Achieving the precision control of the frequency and the magnitude of a triangular waveform operating at the VHF is not trivial. For conventional designs, the control of the magnitude relies on the high-speed comparators that can be power consuming, and the switching frequency suffers from PVT variations. If multiple switching phases are required, the design becomes even more challenging. In [9], a two-phase triangular generator is proposed that works up to 10 MHz. Furthermore, this topology is limited to two switching phases and cannot be extended to multiple phases. In [18], a ramp generator that uses two calibration loops is proposed. It works up to 70 MHz but is not capable of generating multiple phases. Here, we propose a novel triangular wave generator with one calibration loop that is capable of generating multiple phases.

For system-on-chip implementations, there is usually a high-precision half duty-ratio clock reference. Using this clock reference, we are able to build a VHF triangular wave generator. This idea is shown in Fig. 8(a). The half duty-ratio clock signal is used to control the charging and discharging of the capacitor C_{TR}. When the switch S_1 is OFF, C_{TR} is charged by I_b; when S_1 is ON, C_{TR} is discharged by I_{bd}. If I_{bd} is equal to 2 I_b, the total charge across C_{TR} is then zero after each cycle and the resulting waveform V_{tri} is a triangular signal with a swing of $I_b T/C_{\text{TR}}$, where T is the period of the clock signal. Multiphase VHF triangular signals can be easily generated if multiphase clock signals are available. However, this approach suffers from two problems. First, as shown in Fig. 8(b), the maximum voltage V_H and the minimum voltage V_L of V_{tri} may drift. Second, due to the mismatch

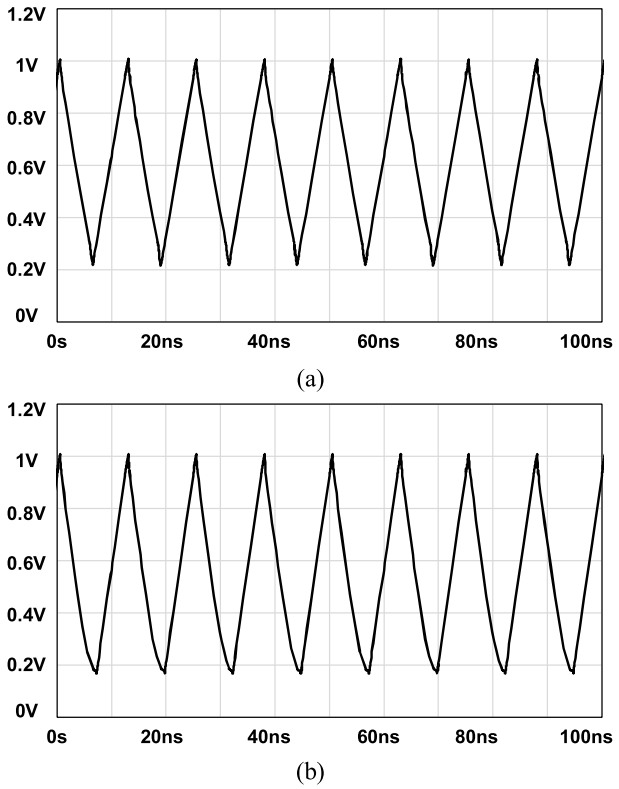

Fig. 10. Simulated triangular waveform with (a) 10% and (b) −10% duty ratio offset.

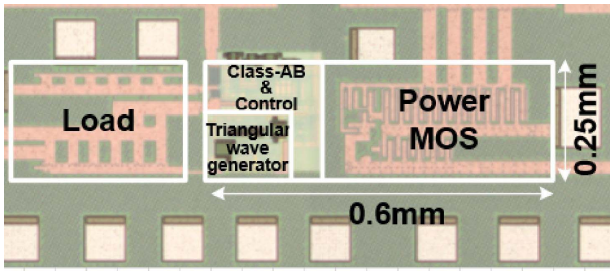

Fig. 11. Die micrograph.

between the charging current and the discharging current or the imprecision of the duty ratio, the dc voltage of V_{tri} will shift toward the supply rail or ground. Fig. 8(c) shows the case when the discharging current is smaller than 2 I_b. In this case, the total charge accumulated on C_{TR} during each cycle is positive and V_H increases continuously.

A novel VHF triangular waveform generator using a single calibration loop is proposed to address. Fig. 9(a) and (b) shows the block diagram and operating waveforms, respectively. A feed-forward clamping amplifier and an I_b calibration loop are added to the original structure in Fig. 8(a). The switch S_1 is controlled by V_{s1En}, a delayed version of the half duty-ratio clock signal V_{clk}. The switches S_2 and S_3 are controlled by V_{s2fEn} and V_{s3rEn}, which are the falling pulse and the rising pulse of V_{clk}, respectively. The reference voltages V_H and V_L define the maximum and the minimum voltages of the triangular waveform, respectively. The capacitor C_{TR} is charged and discharged by I_b and $I_{\text{bd}} - I_b$, respectively. Ideally, I_{bd} should be twice of I_b and the net charge on C_{TR} during each cycle is zero. However,

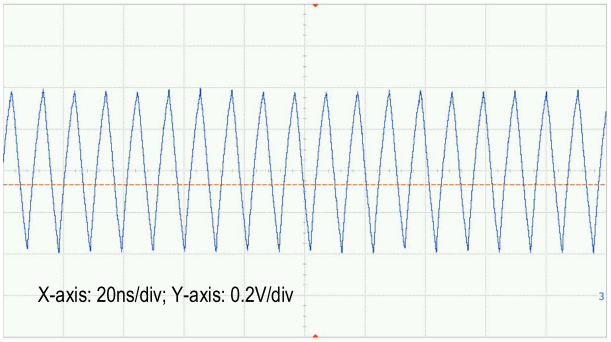

Fig. 12. Measured triangular waveform.

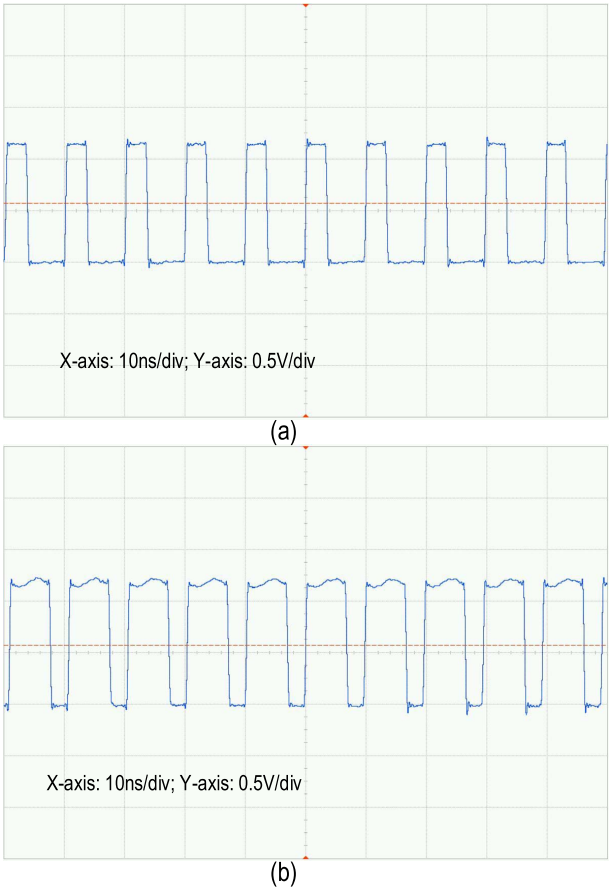

Fig. 13. Measured switching node waveform with (a) $V_{\text{env}} = 0.4$ V and (b) $V_{\text{env}} = 0.8$ V.

due to device mismatches and PVT variations, the precision control of I_{bd} is very challenging. To address this problem, a clamping amplifier with unity-gain feedback is used to force the minimum voltage of V_{tri} to be V_L at the beginning of each cycle. Furthermore, a bias current calibration loop is used to enforce the maximum voltage of V_{tri} to V_H at the end of each cycle. As the clamping amplifier is used in a feed-forward fashion, this triangular wave generator is essentially a single-loop system that involves only the bias current calibration loop.

The detailed operation of the proposed VHF triangular wave generator is illustrated in the timing waveforms in Fig. 9(b). When S_1 is OFF, the capacitor C_{TR} is charged. When S_1 is ON, C_{TR} is discharged. The maximum value of V_{tri} is calibrated by the I_b-controller via a negative-feedback control loop. When

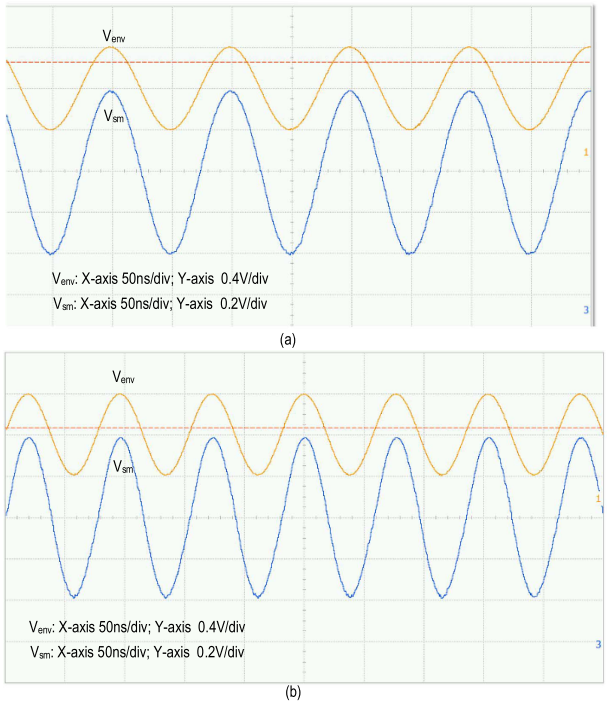

Fig. 14. Measured waveforms when tracking a 0.8 V_{pp} sinusoidal signal at (a) 10 MHz and (b) 13 MHz.

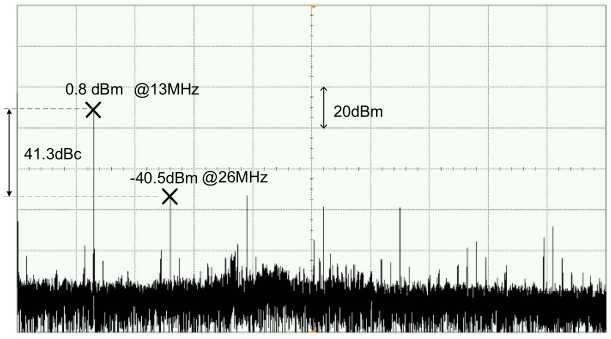

Fig. 15. Measured output spectrum when tracking a 13 MHz 0.8 V_{pp} sinusoidal signal.

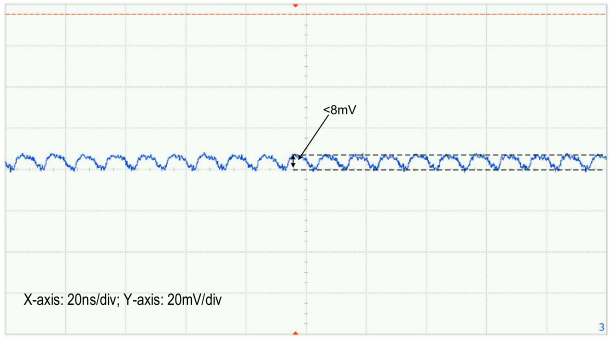

Fig. 16. Output voltage ripple at 100 MHz with $V_{env} = 0.6$ V.

S_3 is ON, the I_b-controller compares V_{tri} with V_H to adjust I_b. When V_{tri} is lower than V_H, the gate voltage of M_{NB} is then charged up, I_b increases, and so does the maximum voltage of V_{tri}. Eventually, the maximum voltage of V_{tri} will be calibrated to V_H. The case when V_{tri} is higher than V_H during the ON-period of S_3 can be analyzed in a similar fashion. In both the cases, this calibration loop is able to regulate the maximum

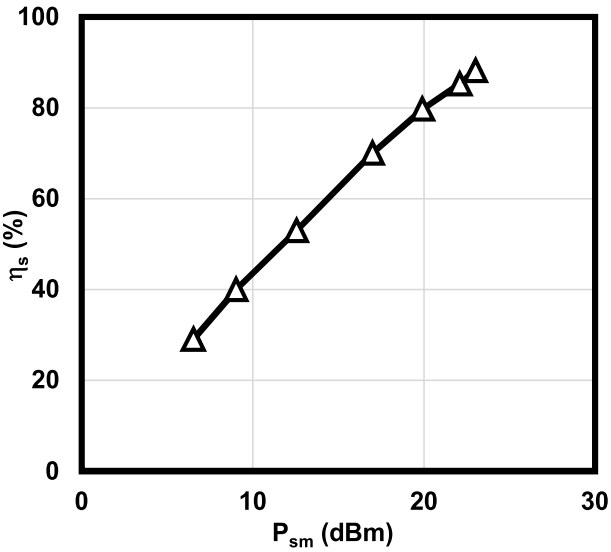

Fig. 17. Measured static efficiencies.

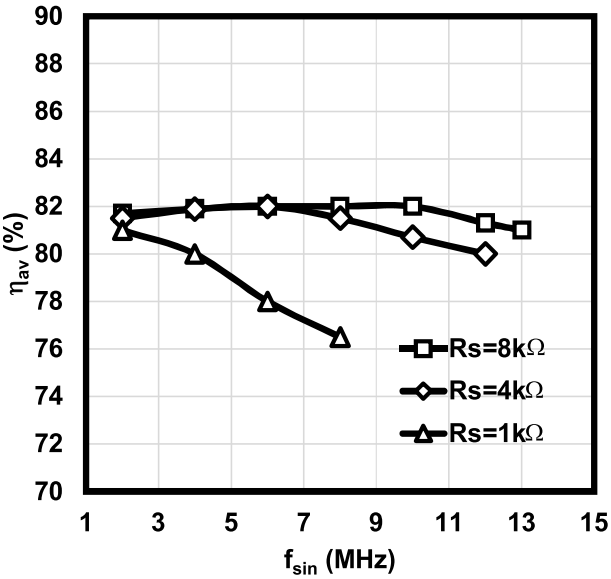

Fig. 18. Measured dynamic efficiencies.

voltage of V_{tri} to V_H. Since V_{tri} is used only as a reference signal, the speed of the calibration loop is not important. This enables us to design a slow I_b-controller with very low power. In practice, a clock signal with a precise duty ratio of (1/2) cannot be obtained and the total charge on C_{TR} during each cycle may not be exactly zero even if I_{bd} is exactly twice of I_b. In this case, the dc voltage of V_{tri} may shift. At the start of each period, S_1 is turned ON and the clamping amplifier forces V_{tri} to be V_L. Note that the ON-period of S_1 can be made very small so that it is negligible when compared with the switching period.

The simplified schematic of our proposed triangular wave generator is shown in Fig. 9(c). The control signals, V_{s1En}, V_{s2fEn}, and V_{s3rEn}, are generated from the clock signal V_{clk}. The switch S_1 is realized by an nMOS transistor M_{NS1}, while the switches S_2 and S_3 are implemented by transmission gates. The I_b-controller consists of an amplifier and several current mirrors. The amplifier adopts the current-mirror Miller structure [19] and is used to tune I_{b2} by

TABLE II
PERFORMANCE COMPARISON

Design	[3] JSSC'09	[20] ISSCC'14	[8] JSSC'07	[9] JSSC'10	**This work**
Process	65nm CMOS	0.13μm CMOS	0.35μm CMOS	0.35μm CMOS	**0.13μm CMOS**
Control Method	Hysteretic	PWM + AC-Coupling	PWM	Two-Phase PWM	**Ripple-Current Based PWM**
Supply Voltage	1.2V	3.8V	3.5V	3.3V	**1.2V**
Maximum Output Power	22.7dBm	33dBm	33.5dBm	33dBm	**23dBm**
Peak Static Efficiency	87.5%	N.A.	88.3%	89%	**88.2%**
Dynamic Efficiency	N.A.	86.2%@10MHz LTE (SR_{max}<16.5V/μs)	N.A.	80%@4MHz Rectified Sine (SR_{av}≈19.2V/μs)	**81%@13MHz Sine** (SR_{av}≈21V/μs)
Linearity (1st and 2nd tone difference)	N.A.	N.A.	N.A.	43dBc@2MHz Sine (SR_{av}≈9.6V/μs)	**41dBc@13MHz Sine** (SR_{av}≈21V/μs)
Output Voltage Ripple	~10mV	N.A.	~12mV_{pp}	~40mV_{pp}	**~8mV_{pp}**
Switching Frequency	118MHz (peak)	2MHz	2MHz	10MHz	**100MHz**
Inductor Value	80nH	4.7μH	4μH	500nH	**100nH**
Load Resistor	5.3Ω	4.7Ω	4Ω	3.8Ω	**5Ω**

adjusting the gate voltage of $M_{\rm NB}$. A Miller capacitor C_m is connected across the amplifier to stabilize the control loop. The bias current I_b is the sum of the fixed bias current I_{B1} and the current I_{b2} that is calibrated by the feedback loop. The current I_{B1} determines the minimum frequency, and the maximum value of I_{b2} determines the maximum frequency, that is

$$\frac{1}{2}\frac{(I_{B1}+I_{b2}(\max))}{(V_H-V_L)C_{\rm TR}} \geq f_{\rm sw} \geq \frac{1}{2}\frac{I_{B1}}{(V_H-V_L)C_{\rm TR}}. \quad (4)$$

A wide tuning range of the frequency can be achieved by carefully choosing related parameters. Computer simulations are used to verify the robustness of our proposed VHF triangular wave generator. We denote the duty ratio of $V_{\rm clk}$ by $D_{\rm clk}$. Fig. 10 shows the simulated waveform of $V_{\rm tri}$ at 80 MHz with 10% and −10% offsets in $D_{\rm clk}$. In both the cases, the dc voltage of $V_{\rm tri}$ is kept fixed, the frequency of 80 MHz is achieved, and the magnitude of $V_{\rm tri}$ is maintained to be around 0.8 V with $V_H = 1$ V and $V_L = 0.2$ V. Similar results can also be obtained under PVT variations. Compared with the previous designs, our proposed design reduces the design complexity greatly by using only one calibration loop while achieving good robustness against PVT variations and device mismatches. Moreover, multiphase triangular waveforms can be generated easily by using multiphase clock signals.

IV. MEASUREMENT RESULTS

The proposed design has been fabricated in 0.13 μm CMOS process with a core area of 0.25×0.6 mm^2, and the die micrograph is shown in Fig. 11. As flip-chip bonding is unavailable, on-chip decoupling capacitors and multiple power pads are used to suppress the supply ripples. An off-chip inductor of 100 nH (PFL1005-101MR) is selected and an on-chip 5 Ω resistor modeling the RF PA is used as the load. We design the switching frequency to be 100 MHz. The series *RC* RCS is placed off-chip to allow for flexible tuning. The series capacitor C_s connected to the ground is designed to be 22 pF. Unless otherwise specified, R_s is chosen to be 8 kΩ in order to maintain a high-speed switching loop while avoiding high-order harmonics. According to [11], static efficiency, dynamic efficiency, output voltage ripple, and linearity are the four parameters that adequately capture the performance of an HSM. We measure these four parameters and other related parameters.

Fig. 12 shows the measured triangular waveform $V_{\rm tri}$ switching at 100 MHz with an amplitude of 0.8 $V_{\rm pp}$. Fig. 13 shows the switching node waveform V_x at different envelope voltages. With the proposed large-signal PWM control, V_x switches with different duty ratios at different $V_{\rm env}$ values while maintaining a fixed switching frequency. Fig. 14 shows the measured waveforms when the HSM is tracking a 0.8 $V_{\rm pp}$ (from 0.2 to 1 V) sinusoidal signal at 10 and 13 MHz. At 10 MHz, the magnitude of $V_{\rm sm}$ is almost the same as that of $V_{\rm env}$ and high-fidelity tracking is achieved. Starting from 13 MHz, the slew rate of the HSM gradually becomes insufficient and a slight magnitude reduction of $V_{\rm sm}$ is observed. Note that the output range of the HSM is only limited by that of the Class-AB LA, which is rail-to-rail in our design. Fig. 15 shows the measured output spectrum when the HSM is tracking a 13 MHz 0.8 $V_{\rm pp}$ sinusoidal signal. The difference between the first tone and the second tone is 41 dBc. For RF PAs, intermodulation is also used for characterizing the linearity. However, the method used for measuring the intermodulation cannot be applied directly to the HSMs. Fig. 16 shows the output voltage ripple $\Delta V_{\rm sm}$.Thanks to the wideband Class-AB amplifier in [11], $\Delta V_{\rm sm}$ is reduced to below 8 mV. Fig. 17 shows the measured static efficiencies η_s as a function of output power. The proposed design achieves a peak η_s of 88.2% at the maximum output power of 23 dBm.

At 6 and 12 dBm backoff power, our design is able to maintain a static efficiency of 70% and 48%, respectively. Fig. 18 shows the measured dynamic efficiencies for different

R_s values when tracking a 0.8 V_{pp} sinusoidal input signal. Using a larger R_s increases the speed of the switching loop, and reduces the required I_{ab} during wideband sinusoidal tracking, benefiting both the tracking range and the dynamic efficiency. With $R_s = 1$ kΩ, our design is only able to track the sinusoidal input wave with high fidelity up to 8 MHz. With $R_s = 4$ kΩ and $R_s = 8$ kΩ, the tracking range is extended to 12 and 13 MHz, respectively. Furthermore increase in R_s does not help increase the tracking capability significantly. Table II summarizes the performance metrics of our proposed design and other recent designs. Compared with [9] that used two switching phases and a feed-forward path, the proposed design extends the tracking capability from an average slew rate of 19.6 V/μs to 21 V/μs. Furthermore, It achieves much better tracking range while maintaining similar linearity. It also achieves the lowest output voltage ripple among all designs. Compared with other PWM-controlled designs, our design could switch at a much higher frequency due to the use of the RCS.

V. Conclusion

In this paper, we present a 100 MHz HSM with ripple-current-based PWM control. It uses an RCS for control, thus overcoming the bandwidth limitation of an ACS and enabling the VHF operations. As it is a large-signal-based design, the switching-loop response is no longer limited by the switching frequency. Therefore, it does not need the feed-forward path while achieving a high-speed switching loop. A VHF triangular wave generator that works up to 100 MHz is proposed. Our theoretical predications have been validated by measurement results.

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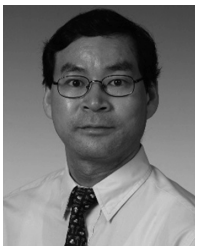

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