

Wideband Mixed-Domain Multi-Tap Finite-Impulse Response Filtering of Out-of-Band Noise Floor in Watt-Class Digital Transmitters

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Abstract—A major drawback of digital transmitters (DTX) is the absence of a reconstruction filter after digital-to-analog conversion which causes the baseband quantization noise to get upconverted to radio frequency and amplified at the output of the transmitter. In high power transmitters, this upconverted noise can be so strong as to prevent their use in frequency-division duplexing systems due to receiver desensitization or impose stringent coexistence challenges. In this paper, we describe a DTX that embeds mixed-domain multi-tap finite-impulse response (FIR) filtering with programmable analog sub-sample delays within a highly linear and mismatch-resilient switched-capacitor DTX architecture. It is shown that switched-capacitor power amplifiers (SCPA) in conjunction with transformer-based power combining are ideal candidates for embedding mixed-domain FIR filtering since the near-constant source impedance of the SCPA greatly aids in linear FIR summation thereby preserving the desired noise-shaping profile. Moreover, their excellent mismatch characteristics help in ensuring precise tap weights in the FIR which enhances noise suppression. The availability of multiple taps in this architecture also allows the synthesis of FIR configurations with wide notch bandwidths (BW). Theoretical analyses of this architecture and design trade-offs related to linearity, mismatch, output power, and efficiency are discussed. The implemented 65 nm CMOS prototype exhibits a peak output power of 30.3 dBm and a peak system efficiency of 34%, and achieves a noise floor of -149 dBc/Hz over a BW of 20 MHz at an offset of 135 MHz from a 2.23 GHz carrier while transmitting a 1.4 MHz 64-QAM signal with an average output power of 22 dBm.

Index Terms—Digital filters, digital integrated circuits, FET integrated circuits, finite-impulse response (FIR) filters, high power amplifiers, mixed analog digital integrated circuits, MOS integrated circuits, nonlinear circuits, notch filters, predistortion, radio frequency (RF) integrated circuits, radio transmitters, RF transmitters, sampled data circuits, switched-capacitor circuits.

I. INTRODUCTION

DIGITAL transmitters (DTX) represent an evolution in the architecture of radio frequency (RF) transmitters from the conventional analog form to highly integrated digital versions. The conventional analog transmitter consists of a

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baseband digital-to-analog converter (DAC) followed by an analog reconstruction filter to suppress its quantization noise and spectral images. This is followed by a variable-gain amplifier for power control and a mixer before the signal is amplified (potentially off-chip) using a power amplifier [1]–[5]. Fully integrated DTXs [6]–[16] collapse the functionalities of DAC, mixer, and power-amplifier (PA) into one block. Their digital nature allows reconfigurability across multiple standards, easy portability across technology, and potentially full synthesizability [17], while eliminating power hungry and bulky analog blocks that do not scale well with technology. However, since the reconstruction filter is absent, the baseband quantization noise gets directly upconverted to RF and amplified.

Fig. 1(a) shows a frequency-division duplexing (FDD) configuration with a DTX and a receiver attached to an antenna through a duplexer. The unfiltered baseband quantization noise in the DTX is upconverted to RF, amplified and leaks to the input of the receiver through the duplexer thereby degrading its noise figure (NF). For a peak transmitter output power of 1 W, 6 dB modulation signal peak-to-average power ratio (PAPR), and stand-alone receiver NF of 5 dB, the effective receiver NF as a function of the transmitter noise in the receive (RX) band for three duplexer isolations is shown in Fig. 1(b). For a typical isolation of 45 dB, the transmitter noise floor in the RX band must be < -156 dBc/Hz to negligibly degrade receiver sensitivity. Aside from FDD, coexistence requirements of multiple wireless transceivers on the same platform impose very similar transmitter noise floor requirements to avoid receiver desensitization. Quantization noise can be suppressed by increasing the sampling rate and/or DAC resolution, both of which are associated with a corresponding increase in power consumption and complexity. Meeting the challenging -156 dBc/Hz noise requirement requires an effective number of bits (ENOB) of 11 bits and a sampling frequency of 0.5 GS/s. Such a high ENOB is extremely challenging in high power, highly efficient, digital PAs given their strong nonlinearity.

A survey of the existing CMOS RF transmitters and modulators (Fig. 2) consisting of analog transmitters [1]–[5], [18], [19], digital polar [10], [11], [13], [20]–[23], and digital cartesian [6], [7], [24]–[26] transmitters shows that the -156 dBc/Hz requirement has been adequately met in transmitters with low output powers. However, there is still a gap of about 2 orders of magnitude for DTXs, particularly those with high output power levels (>15 dBm). In [23], signal generation algorithms are used to reduce the out-of-band noise

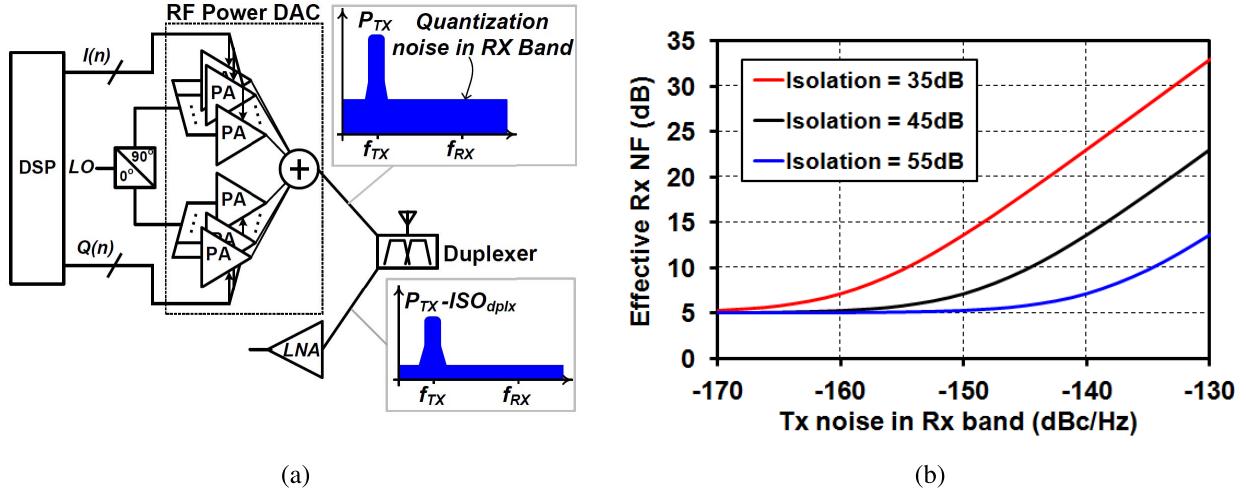


Fig. 1. (a) RF DTX in an FDD setup. (b) Receiver NF degradation as a function of transmitter noise in the RX band for different duplexer isolations.

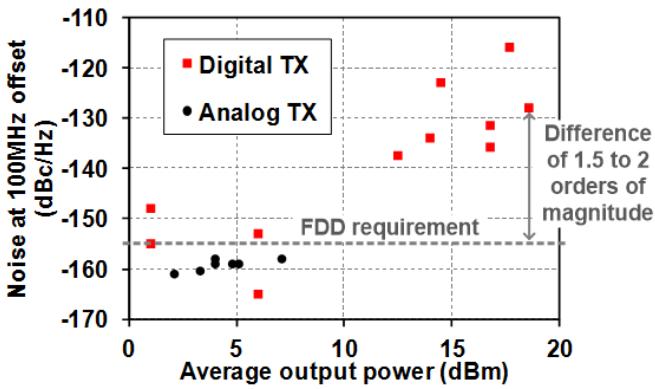


Fig. 2. Survey of the existing analog and digital CMOS RF transmitters.

in the RX band in a digital polar transmitter. Linear-phase finite-impulse response (FIR) filters are applied to the amplitude and phase paths in addition to employing delta-sigma algorithms on the amplitude path for lower noise. However, the achieved noise floor is -136.5 dBc/Hz (as opposed to the expected -154 dBc/Hz from simulations) at 12.5 dBm of output power. This is due to the nonlinearity of the buck converter in the amplitude path which drastically reduces the filtering provided by the digital-domain techniques mentioned above. This underscores the sensitivity of purely digital-domain noise filtering techniques to the output stage nonlinearity. In [16], a two-tap mixed-domain FIR filter is embedded in a Class E/F_{odd} -based digital cartesian RF transmitter. However, owing to the severely nonlinear source impedances of the current-combined radio-frequency digital-to-analog converter (RFDAC) taps, the filtering is limited to just 8 dB in the RX band. As a result, the transmitter only achieves -134 dBc/Hz noise floor at 18.3 dBm of output power. Moreover, the bandwidth (BW) of suppression achieved was very narrow (<1.5 MHz) owing to the 2-tap configuration. Furthermore, the delays of the embedded FIR can only be integer multiples of the digital clock period which limits the number of possible notch locations.

This paper describes a high-power DTX first introduced in [27] that reaches the challenging -150 dBc/Hz RX band

noise level by: 1) embedding mixed-domain FIR filtering in a highly linear and mismatch-resilient switched-capacitor digital PA architecture to improve notch depth and 2) a multi-tap FIR structure with programmable analog sub-sample delays that enables >20 MHz notch BW and flexible notch placement for arbitrary duplexing offsets. The DTX achieves a peak output power of 30.3 dBm at a peak efficiency of 34% through power-combining, impedance transformation and IQ cell re-use [28].

Section II describes the concept of mixed-domain FIR filtering and the need for it over purely digital-domain filtering. In Section III, a highly linear implementation of mixed-domain FIR filtering using transformer combiners and switched-capacitor RFDACs is introduced. Section IV delves into the implementation details of the 65 nm CMOS >1 W 2.2 GHz DTX. We conclude this paper with measured results of the implemented prototype in Section V and conclusion in Section VI.

II. MIXED-DOMAIN MULTI-TAP FIR FILTERING OF OOB QUANTIZATION NOISE

In order to suppress quantization noise, we first demonstrate the ineffectiveness of the approach, wherein the baseband quantized signal is filtered in the digital domain using a notch filter to suppress its noise in the RX band. This digital-domain FIR scheme is shown in Fig. 3. The baseband sampled and quantized signals $I_{\text{BB}}/Q_{\text{BB}}$ are generated by the DSP. The simulated power spectral density (PSD) of $I_{\text{BB}}/Q_{\text{BB}}$ 1.4 MHz 64 -QAM signals sampled at 560 MHz with 9 bit resolution is also shown in the figure. This signal is filtered digitally using a 3-tap 4th order FIR filter ($1 + 2z^{-2} + z^{-4}$) which places a wideband notch at 140 MHz in the digital signal. In Section III-B, further details on how this choice of FIR coefficients leads to wideband notches are elaborated. It must be noted that the filtered signal $I_{\text{FIR}}/Q_{\text{FIR}}$ has a resolution of 11 bits and as expected, its simulated PSD shows infinitely deep notches. This filtered signal is passed through a two-dimensional (2-D) digital predistortion (DPD) [8], [29] to compensate

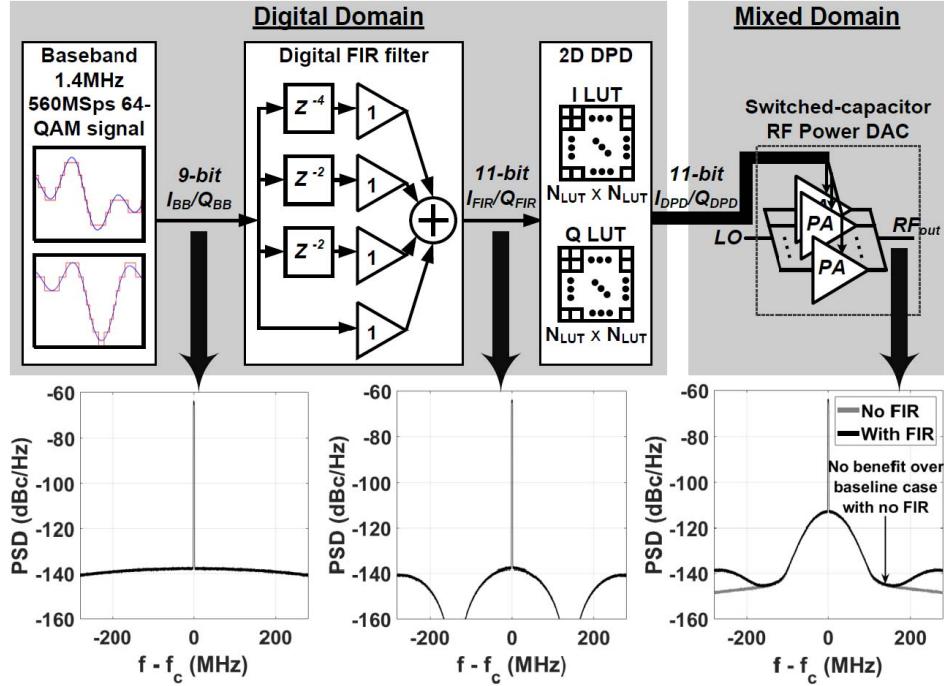


Fig. 3. Digital-domain FIR filtering scheme showing the PSD at each point in the signal flow.

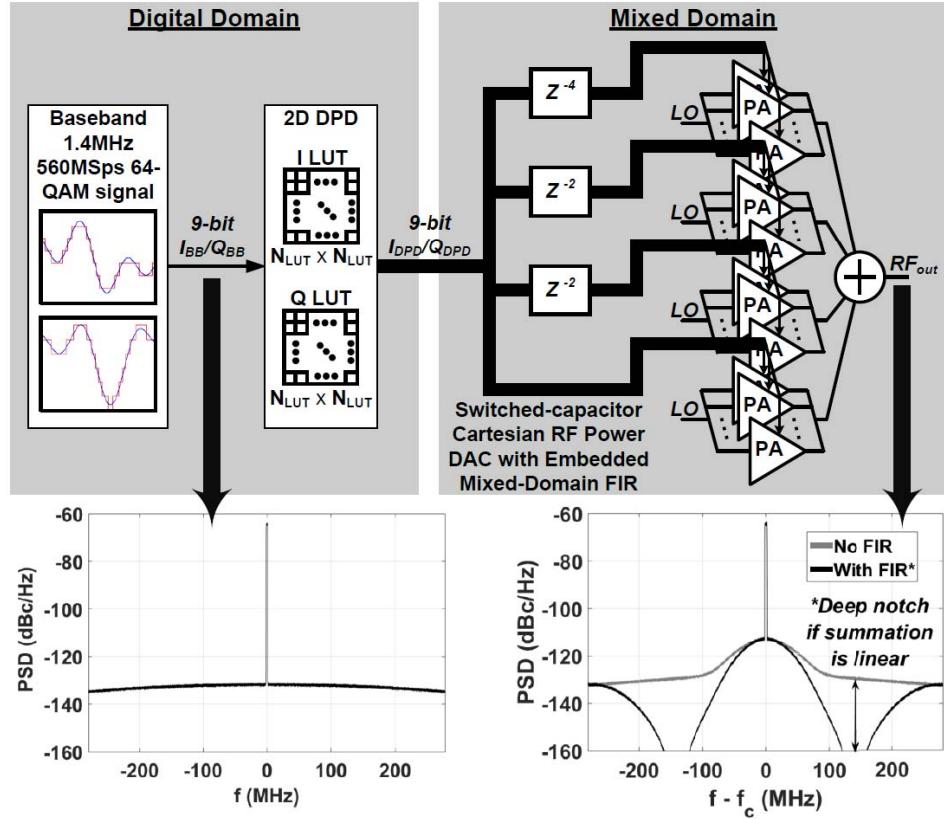


Fig. 4. Ideal mixed-domain FIR filtering scheme showing the PSD at each point in the signal flow.

for the nonlinearity of the DTX. The DPD uses an look-up table (LUT) size of 64×64 elements on which 2-D cubic interpolation is performed to obtain I_{DPD}/Q_{DPD} . The static

nonlinearity used for this simulation study is the measured nonlinearity of a 9-bit switched-capacitor DTX which is interpolated to obtain the equivalent nonlinearity of a 11-bit

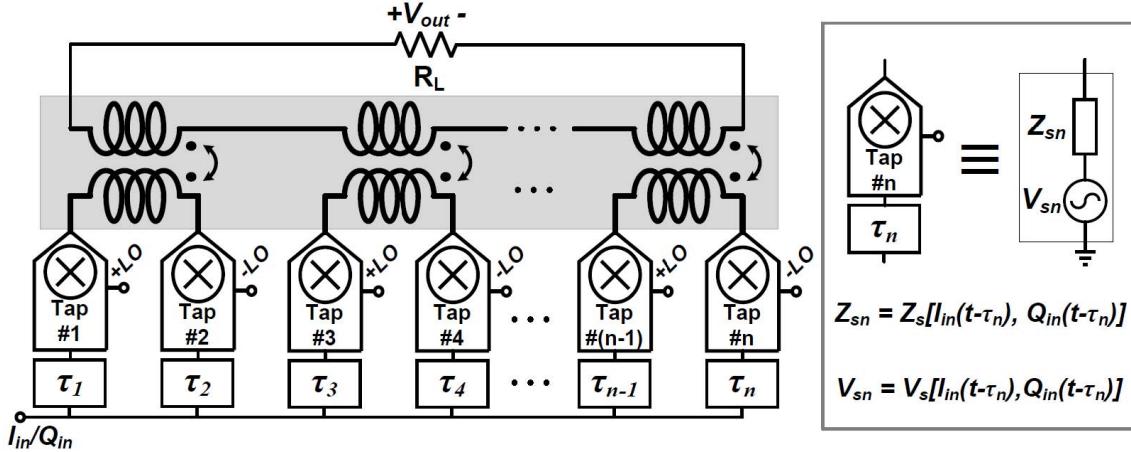


Fig. 5. Transformer based mixed-domain FIR filtering.

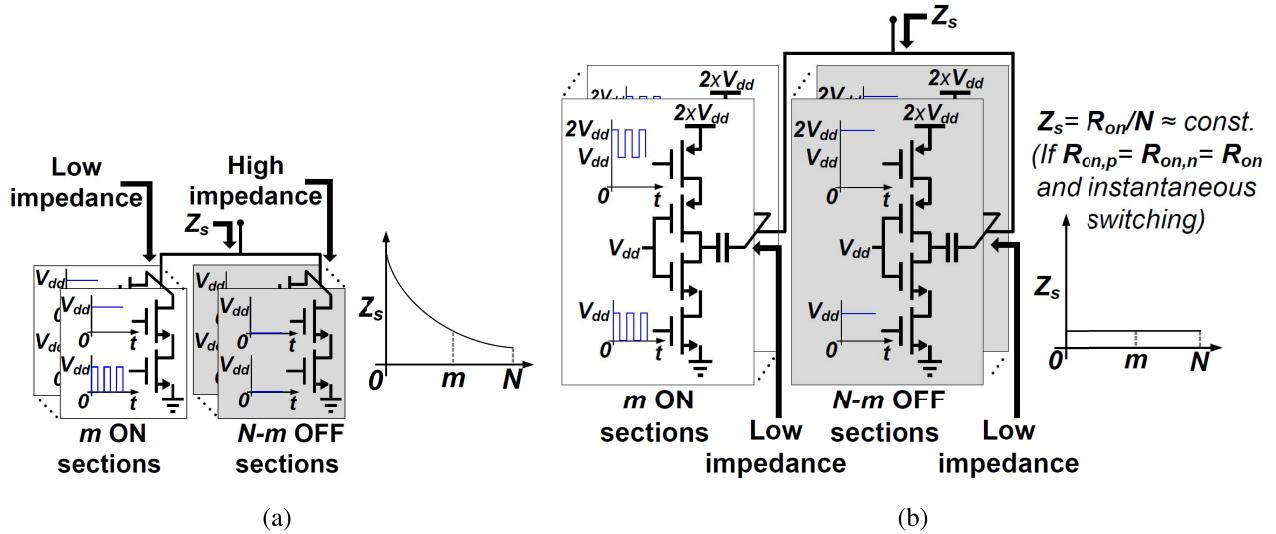


Fig. 6. Two types of RFDAC taps and their source impedance profiles. (a) Current-combined RFDAC taps. (b) Switched-capacitor RFDAC tap.

DTX. The predistorted data I_{DPD}/Q_{DPD} is then fed to the DTX to generate the RF output. The simulated PSD of the RF output shows that the deep notches in I_{FIR}/Q_{FIR} are severely degraded. This is due to the residual nonlinearity after 2-D predistortion which results in an effective noise floor that is no better than the baseline case when filtering is disabled. This is despite the fact that the switched-capacitor DTX is more linear than traditional current-combined Class-E/Class-EF_{odd}⁻¹/Class-D⁻¹ DTXs. Static DPD algorithms such as the one employed here are typically insufficient to knock down the spectral regrowth of the main signal at RX band offsets to the required noise floor of the DTX. Hence, while static DPD can drastically improve the error-vector-magnitude (EVM) of a modulated signal, it cannot be used to reach accuracies required to shape the noise floor of the DTX. In other words, digital-domain filtering of the quantization noise is largely ineffective for RX band noise shaping of high-power DTXs owing to its sensitivity to the residual nonlinearity after DPD.

To circumvent this problem, we propose the mixed-domain FIR filtering scheme shown in Fig. 4. The baseband sampled

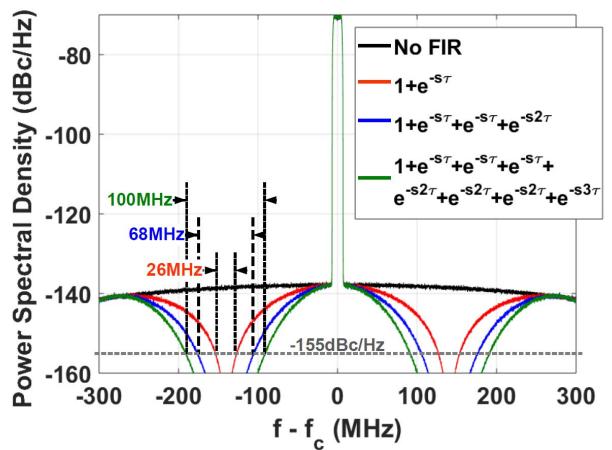


Fig. 7. Benefits of a multi-tap FIR structure as opposed to a simple 2-tap FIR.

and quantized signals I_{BB}/Q_{BB} are generated in the DSP and directly passed through the 2-D digital predistorter. The predistorter here also has 64×64 LUT elements and uses cubic interpolation. The predistorted data is then fed to the DTX

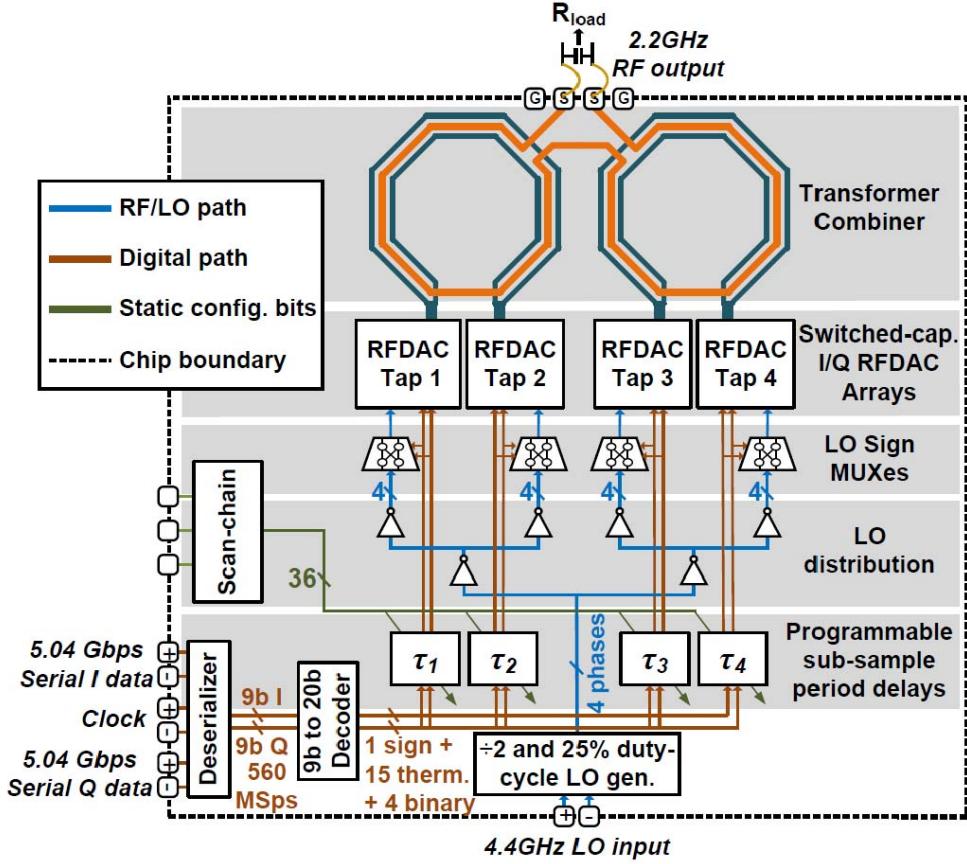


Fig. 8. Block diagram of the switched-capacitor DTX with wideband mixed-domain multi-tap FIR filtering of out-of-band noise floor.

which is itself in an FIR configuration with multiple delayed 9-bit RFDAC taps summed linearly. The net resolution of the RFDAC is still 11 bits as in the previous case, since each RFDAC has a 9 bit resolution and the remaining 2 bits are implemented in a thermometer fashion via power combining. The digital predistortion is trained using the nonlinearity of the transmitter with FIR turned off, i.e., all delays being identical. To ensure a fair comparison, the transmitter nonlinearity assumed here is identical to that used for the transmitter in the digital-domain FIR filtering approach in Fig. 3. When FIR is turned on, the residual nonlinearities after predistortion are identical at the output of all the taps. Hence, although the residual nonlinearity mildly distorts the signal in each path, delayed versions of the identically distorted signals appear at the output of each RFDAC tap. If the final FIR summation is linear (a topic that is discussed in greater detail in Section III), the notch in the FIR profile is perfectly preserved thus making the filtering insensitive to the particular nonlinearities of the transmitter (Fig. 4).

III. TRANSFORMER-BASED MIXED-DOMAIN MULTI-TAP FIR FILTERING

Fig. 5 shows an implementation of n -tap mixed-domain FIR filtering, wherein $n/2$ identical differential RFDACs are combined using an $n/2$ -way transformer combiner. Each half of a differential RFDAC receives digital baseband signals via

independently programmable delays thus realizing an n -tap structure. The RF signals from all taps are summed across the transformer combiner in the RF domain to realize a mixed-domain FIR filter. The nominal sign of local oscillator (LO) signals going to each tap in a differential RFDAC are flipped so as to cause an addition of the signals from the two taps in the RF domain. Each RFDAC tap may be represented as an equivalent digital control word (DCW)-dependent voltage source $V_s(I_{in}, Q_{in})$ in series with a DCW-dependent source impedance $Z_s(I_{in}, Q_{in})$. Z_s is a steady-state value that assumes immediate settling of the circuit when DCW is changed. This assumption is less valid as the signal BW increases as does the efficacy of static DPD. Assuming the transformer combiner is ideal with a 1:1 turns ratio for each section, the output voltage V_{out} of the transformer combiner may be written as (1)–(3), as shown at the bottom of the next page.

From (3), it is seen that the output response has the form of an FIR filter. However, the identical weights of each tap are nonlinear (dependent on I_{in}/Q_{in}). In order for the summation not to be distorted by the time-varying multiplication factor, the variation in the source impedance $Z_s(I_{in}, Q_{in})$ of each RFDAC tap across DCW must be minimized.

An interaction between notch depth, signal BW, and notch offset frequency can be seen here. The signal BW dictates how different the DCWs going to each tap in the FIR are from each other. The higher the signal BW, the faster the

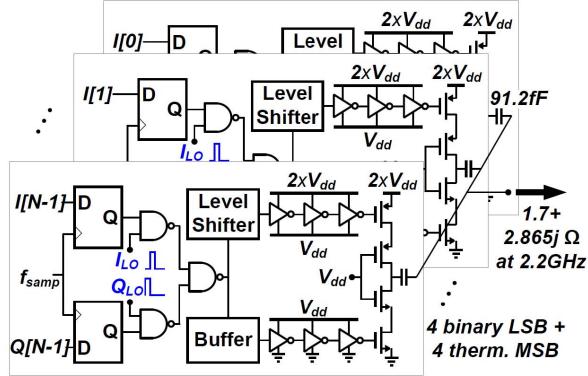


Fig. 9. Circuit diagram of the switched-capacitor RFDAC tap.

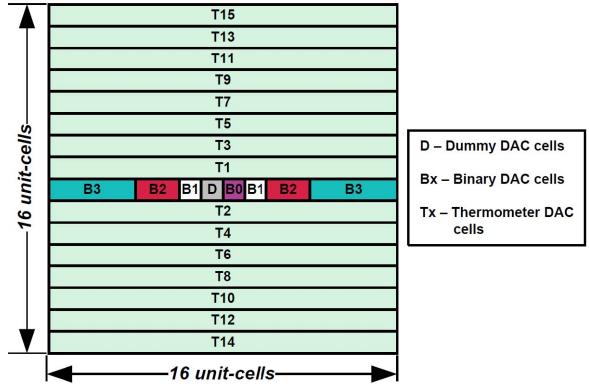


Fig. 10. Switched-capacitor RFDAC tap layout.

signal variation in the time domain which results in larger differences in the DCWs going to each tap for a given notch offset frequency. Also, closer notch offset frequencies necessitate the use of larger delays in the FIR which also leads to the aforementioned phenomenon. These large differences in DCWs and correspondingly large differences in the source impedances of all taps cause a larger distortion in the FIR response and result in shallower notches.

A. Types of RFDAC Taps

In typical current-combined DTXs with Class-D⁻¹ [8], [10], [11], [30], Class-E [14], [15], or Class EF_{odd}⁻¹ [16] RFDAC taps, the source impedance of the taps varies drastically with DCW—from being almost a short-circuit when all sections are ON to a very large impedance when only a few sections are ON [Fig. 6(a)]. This degrades the noise floor in two ways. First, the nonlinearity of the transmitter is severe which causes an increase in the effective noise floor after DPD. In other words, the ENOB of the transmitter degrades with stronger nonlinearity. Second, if transformer-based mixed-domain FIR is used, the strong nonlinear impedance also causes the net FIR response to be multiplied with a DCW-dependent gain in the time domain (as seen in (3)) resulting in distortion of the response. This in turn leads to a shallow notch in the RX band.

Switched-capacitor PAs [6], [13], [27] offer a solution to both these drawbacks. In a switched-capacitor RFDAC [Fig. 6(b)], the output impedance of the tap remains nearly constant across DCWs [31]. This is because an OFF section in the tap exhibits a low impedance through

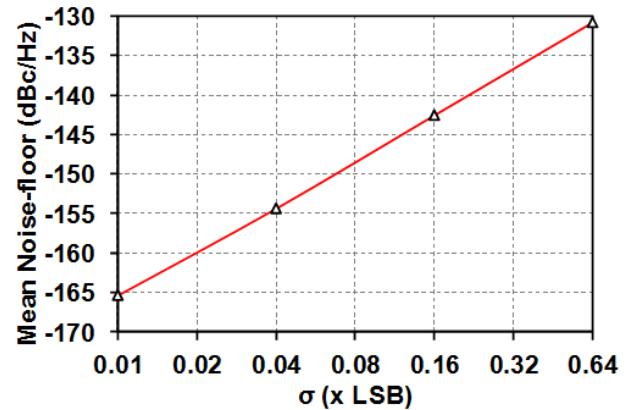


Fig. 11. Effect of mismatch on the notch depth of an effective-3-tap FIR.

the triode-region resistance of the NMOS device stack. This impedance is nearly equal to the impedance of an ON section which alternates between the triode-region resistance of the PMOS stack and the NMOS stack. This effect helps the noise floor in two ways—by making the PA more linear, and hence, increasing its ENOB, and by making the final FIR summation linear. The higher ENOB results in a lower baseline noise floor (without FIR) and the linear FIR summation results in strong suppression of quantization noise in the RX band.

Although switched-capacitor RFDACs exhibit sufficiently linear output impedance to enable strong FIR suppression across a transformer combiner, in conjunction with DPD, they are not linear enough to preserve digital-domain FIR filtering, as discussed earlier. Therefore, by extension, one might

$$V_{\text{out}} = \frac{R_L}{R_L + Z_{s1} + Z_{s2} + \dots + Z_{sn}} \cdot (V_{s1} + V_{s2} + \dots + V_{sn}) \quad (1)$$

$$= \frac{(V_s(I_{\text{in}}(t - \tau_1), Q_{\text{in}}(t - \tau_1)) + \dots + V_s(I_{\text{in}}(t - \tau_n), Q_{\text{in}}(t - \tau_n)))}{1 + \frac{Z_s(I_{\text{in}}(t - \tau_1), Q_{\text{in}}(t - \tau_1)) + \dots + Z_s(I_{\text{in}}(t - \tau_n), Q_{\text{in}}(t - \tau_n))}{R_L}} \quad (2)$$

$$= \underbrace{\frac{1}{1 + \frac{Z_s(t - \tau_1) + Z_s(t - \tau_2) + \dots + Z_s(t - \tau_n)}{R_L}}}_{\text{Time-varying weights}} \cdot \underbrace{[V_s(t - \tau_1) + V_s(t - \tau_2) + \dots + V_{sn}(t - \tau_n)]}_{\text{FIR response}} \quad (3)$$

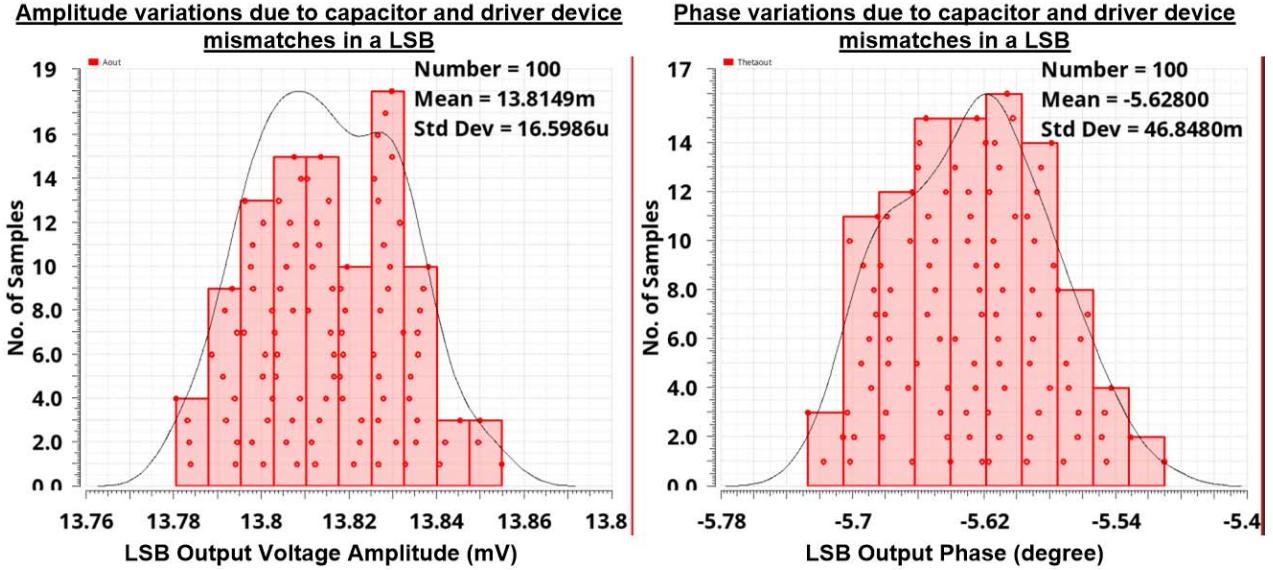


Fig. 12. Simulated mismatch of the implemented design.

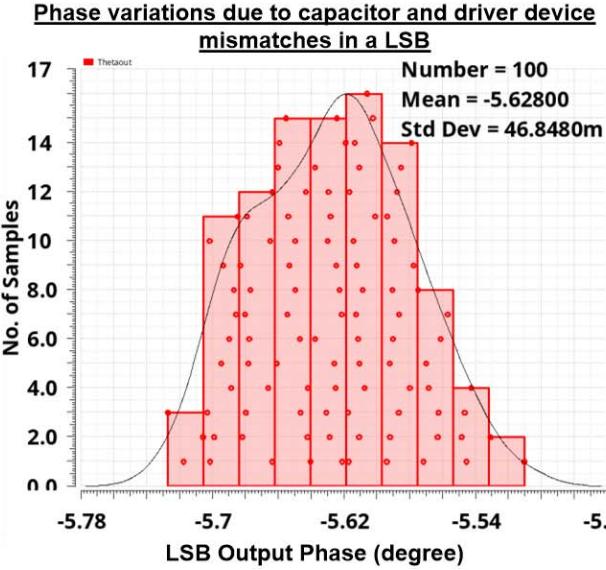
envision that a multi-bit transformer combiner with single-bit switched-capacitor PAs on each tap might be the most linear configuration, enough to preserve digital-domain FIR notches. However, a high-bit transformer combiner is prohibitively complex and area intensive, and therefore, a 4-way transformer combiner with 9-bit switched-capacitor RFDACs on each tap represents a trade-off between linearity and area/complexity.

B. Wideband Noise Suppression

Although it is sufficient to have only two identically weighted taps in an FIR structure to create a notch filter, the BW of the notch is very narrow. Such a 2-tap structure has a transfer function given by $H_1(s) = G(1 + e^{-s\tau})$, where G is the gain of each tap. This filter creates an infinite number of notches, the closest of which is at a frequency of $0.5/\tau$ Hz in the baseband signal (offset from the carrier in the RF signal). Fig. 7 shows the results of the simulations performed on an ideal 9 bit RFDAC with different FIR configurations. The modulation signal is a 10 MHz single-carrier 64-QAM signal at a sampling frequency (f_{samp}) of 560 MHz. Fig. 7 (red curve) shows the BW of the 2-tap notch defined by a noise floor < -155 dBc/Hz to be just 26 MHz. The BW of suppression can be considerably increased if we cascade multiple such notch filters with the same notch frequency. For instance, if we cascade two identical notch filters, the corresponding transfer function may be expressed as

$$\begin{aligned} H_2(s) &= G(1 + e^{-s\tau}) \cdot G(1 + e^{-s\tau}) = G^2(1 + 2e^{-s\tau} + e^{-s2\tau}) \\ &= G^2(1 + e^{-s\tau} + e^{-s\tau} + e^{-s2\tau}) \end{aligned} \quad (4)$$

which is essentially a 3-tap structure emulated by a 4-tap structure with identical weights where two of the taps have identical delays of τ . This configuration will henceforth be called “effective-3-tap” in the rest of this paper. Fig. 7 (blue curve) shows the corresponding PSD of the RFDAC, and the BW is seen to increase to 68 MHz. A cascade



of the three identical 2-tap notch filters can be reduced to the following:

$$\begin{aligned} H_3(s) &= G^3(1 + e^{-s\tau})^3 \\ &= G^3(1 + e^{-s\tau} + e^{-s\tau} + e^{-s\tau} + e^{-s2\tau} \\ &\quad + e^{-s2\tau} + e^{-s2\tau} + e^{-s3\tau}) \end{aligned} \quad (5)$$

which is an 8-tap emulation of the 4-tap structure. This structure has a notch BW of 100 MHz [Fig. 7 (green curve)]. In this manner, any number of such cascaded 2-tap notch filter structures may be emulated using a single-stage multi-tap structure with identical weights. This makes it particularly amenable to embedding itself in PA arrays which typically have multiple identical PAs (identical tap weights) that are power combined using a passive power combiner. Furthermore, this configuration also allows the option of staggering the notch frequencies in the cascade of 2-tap FIR notch filters in order to obtain a wider BW of suppression at the expense of maximum notch depth. However, this possibility is not explored here. It must also be noted that while choosing the coefficients of the FIR filter, care must be taken to ensure that the FIR response chosen has a sufficient passband BW such that it does not attenuate the main signal itself by placing the notch too close to the desired signal, for instance.

IV. DESIGN CONSIDERATIONS AND CIRCUIT IMPLEMENTATION

Fig. 8 shows the block diagram of the implemented DTX in 65 nm CMOS. The DTX consists of two differential RFDACs power combined via a 2-way transformer combiner. Each half of a differential RFDAC receives I/Q DCWs with independently programmable delays, thus forming the four taps of the mixed-domain FIR filter. The taps’ signals are summed across the transformer combiner in the RF domain. The load impedance is transformed via a matching network formed by an off-chip capacitor, wirebonds, and the transformer to

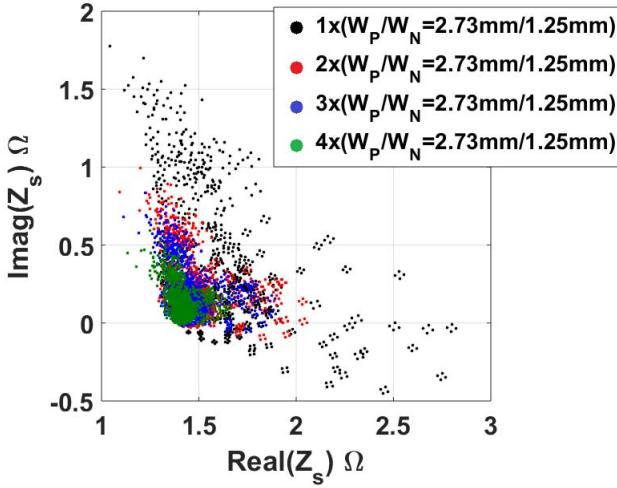


Fig. 13. Source impedance of the switched-capacitor RFDAC tap as a scatter plot versus DCW for different final stage driver sizes (aggregate across all bits in a tap). $2 \times V_{dd} = 2.4$ V, carrier frequency = 2.4 GHz.

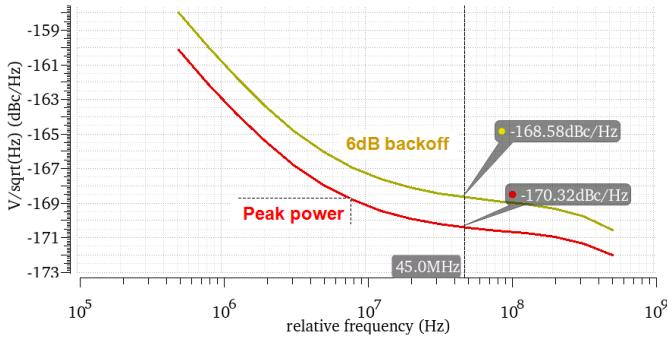


Fig. 14. Simulated phase-noise performance of the DTX.

present 1.7 Ω to each tap. Twenty-five percent duty-cycle I/Q LO waveforms are generated on-chip and fed to taps of the DTX via a corporate distribution network. The LO sign multiplexer (MUXes) are used to select the desired differential phase of the LO signal fed to each tap and constitutes the 9th (sign) bit of each tap. The baseband I/Q data is fed to the chip serially at 5.04 Gb/s on each I/Q lane. The data is deserialized on-chip using a high-speed deserializer and decoded. The decoded data passes through a set of sub-sample-period delay generators whose delays are controlled by user programmable static configuration bits.

A. Switched-Capacitor RFDAC Tap

Fig. 9 shows the circuit diagram of an RFDAC tap. The RFDAC taps are implemented as switched-capacitor power amplifiers (SCPA) employing stacked PMOS and NMOS devices in the final driver. This enables the PA to operate off twice the nominal power supply for higher output power. The tap is sliced in a segmented fashion with four binary and four thermometer bits as a compromise between nonlinearity from the mismatch and complexity of implementation. Buffered level shifters are used to drive the PMOS stack of the final driver stage in every slice. In the NMOS path, the delay of the

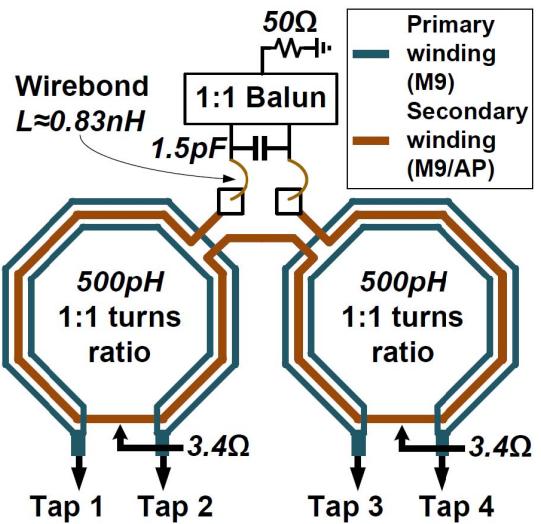


Fig. 15. Output passive network of the SCPA consisting of an L-match network and a 2-way transformer combiner.

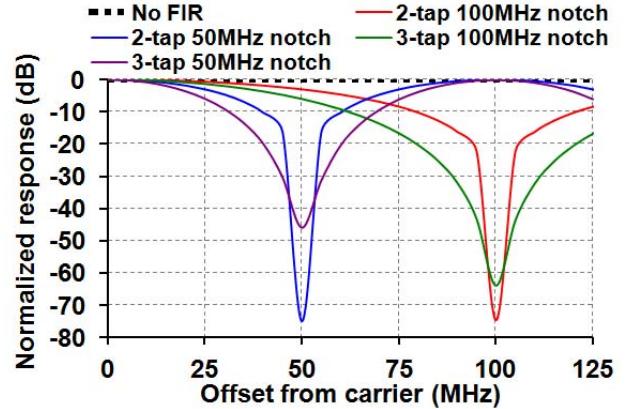


Fig. 16. Simulated normalized FIR transfer function of the 2-way transformer combiner as a function of offset frequency from the 2.2 GHz carrier.

level shifter of the PMOS path is compensated by adding four additional inverter stages. Each slice of the SCPA receives 25% duty-cycle I and Q LO signals ANDed with I and Q DCWs, respectively. In this way, the PA drivers and output capacitors are shared and time-multiplexed between the I and Q DCWs [28]. The switched-capacitor taps are laid out in a common centroid fashion to mitigate the effects of linear gradient mismatches as shown in Fig. 10. The LO and digital clock routings are performed in a corporate/tree manner to minimize the delay differences in the LO and clock signals reaching each bit. The skew-controlled clock is further used to re-time the data signals at each bit using D flip-flops to eliminate any skew in the turn ON or OFF instances of all bits. Minimizing the difference in delays in the LO signals reaching each bit reduces nonlinearity of the tap, while properly retiming the bits alleviates additional random noise from the different turn ON/OFF instances of each bit.

Choosing the LSB capacitance of the switched-capacitor RFDAC tap entails trading-off mismatch between various bits in a tap and between bits in different taps, area, efficiency

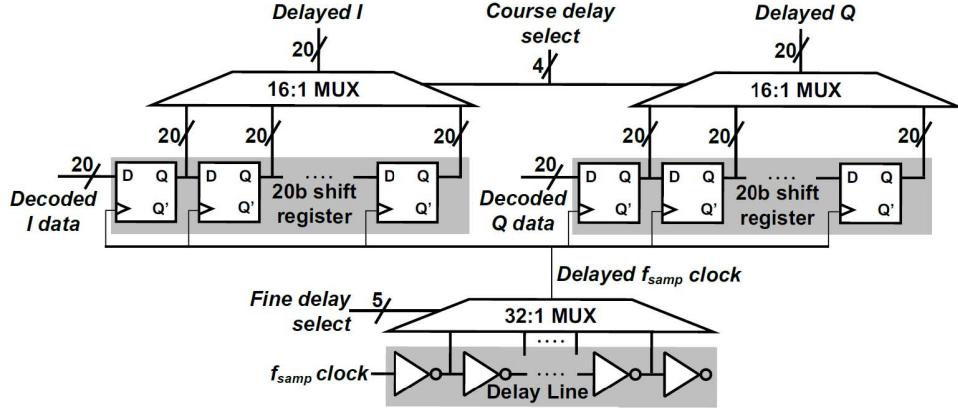


Fig. 17. Schematic of the programmable sub-sample-period delay generator.

under back-off, and RF signal BW. Larger capacitances lead to smaller loaded quality factors which adversely affects efficiency under back-off [13]. However, owing to the lower quality factor, RF BW is enhanced. Also, while the area of the capacitor DAC increases, mismatch between different bits is reduced. An LSB capacitance of 91.2 fF is chosen to ensure that the transmitter exhibits an efficiency under back-off profile similar to Class-B and that the inductance of the transformer combiner is the optimum required to achieve high combining efficiency.

Once the LSB capacitance is chosen, the device sizes of the final stacked inverters must be selected. Beyond a certain device size, larger devices require higher power to be driven adversely affecting power-added efficiency. However, larger devices are less susceptible to random mismatches. The mismatch contribution of the inverters can be made negligibly small by making them very large thus limiting the mismatch to capacitor ratio mismatches which are inherently very precise in modern CMOS processes. Another factor to consider in choosing these device sizes is the source impedance variation of the RFDAC tap and in turn the nonlinearity profile of the DTX. The variation in source impedance is primarily due to the difference in the impedance between an ON section and an OFF section in an RFDAC tap [13]. The effect of this difference in impedance can be made smaller as the devices are made larger, causing their impedances to be small in comparison to the load impedance seen by the tap.

Fig. 11 shows the simulated effect of mismatch on the noise floor after FIR filtering. The simulated nonlinearity of a 9 bit switched-capacitor RFDAC is used for this study. The bits are segmented as four binary LSBs and four thermometer LSBs and random mismatches are assigned to each bit accordingly. Each point on Fig. 11 corresponds to the average noise floor over 20 simulations for a given mismatch standard deviation of the LSB. Also, perfectly linear summation of the signals from all taps is assumed. It is seen that a mismatch standard deviation of <4% LSB is required to achieve a noise floor of <-155 dBc/Hz after filtering. Monte-Carlo simulations (Fig. 12) conducted on the implemented DTX show the worst case mismatch of ~0.12% LSB from amplitude variations alone and the worst case mismatch of ~0.08% LSB from

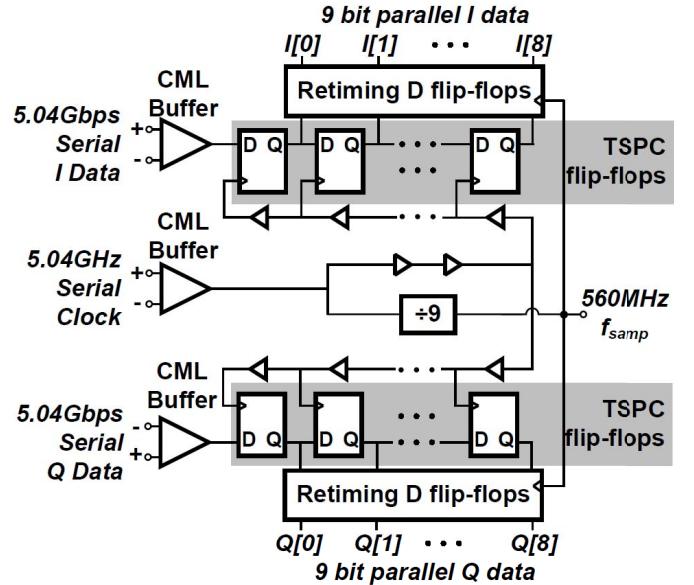


Fig. 18. Block diagram of the high-speed on-chip deserializer to facilitate high sampling-rate testing of the DTX.

phase variations alone which are far below the required levels. This underscores the mismatch resilience in switched-capacitor DTXs which is a key to achieve good filtering of quantization noise.

In this design, since the mismatch characteristics of the DTX easily exceeded the desired specifications, nonlinearity due to source impedance variation as well as the system efficiency considerations decided the size of the final stacked inverters. Fig. 13 shows the source impedance of the switched-capacitor RFDAC tap as a scatter plot across DCW for different final stacked inverter device sizes. It is seen that as the device size increases, the variation in the source impedance of the tap across DCW decreases which contributes to higher linearity of the tap and less distortion in the FIR response. The lower distortion in the FIR response is a direct consequence of (3) where it is seen that if Z_s did not vary at all with DCW, the output FIR response is perfectly preserved. However, if the source impedances vary with DCW, this perfect FIR response is multiplied in the time domain

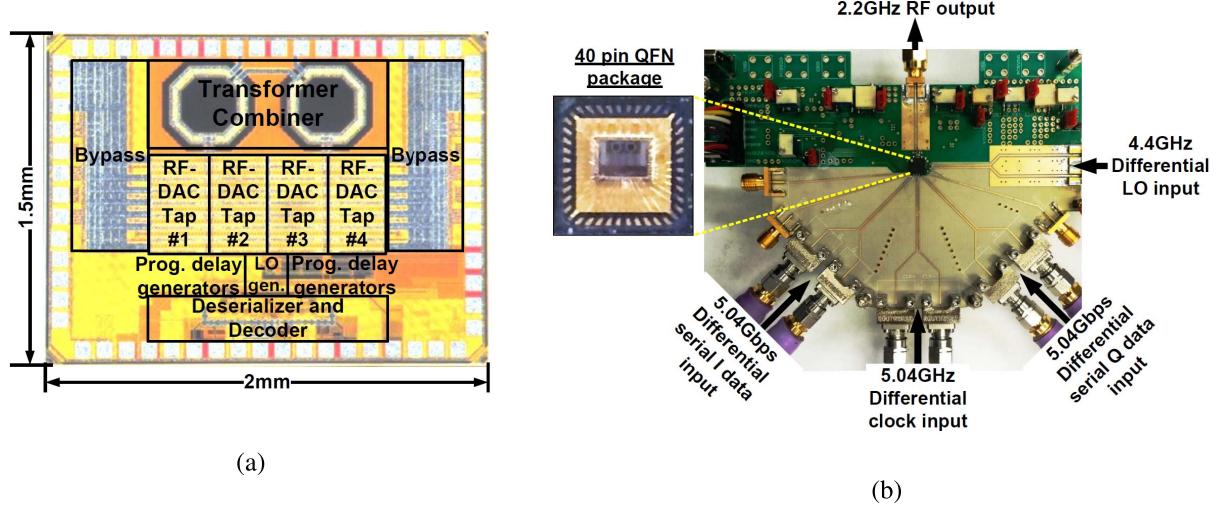


Fig. 19. (a) Chip photograph of the 65 nm CMOS switched-capacitor DTX with wideband mixed-domain multi-tap FIR filtering of out-of-band noise floor. (b) Package and PCB used for the measurement of the implemented prototype.

with a DCW-dependent weighting quantity. In other words, the FIR response is multiplied with nonlinearity, and hence, gets distorted. The stacked inverter device sizes are chosen to ensure a baseline simulated noise floor of -135 dBc/Hz after DPD without FIR, attenuation of quantization noise > 30 dB in the notch after FIR and a simulated peak efficiency $> 40\%$.

Another consideration in determining the sizes of the final stage driver, LO, and clock distribution paths is their effect on phase noise. Phase noise of the LO signal places a lower limit on the achievable noise floor after filtering. The device sizes in each of these must be chosen so as to negligibly degrade the phase noise of the synthesizer and sampling clock generator. Phase noise trades off with power consumption of the distribution paths and, hence, overall transmitter efficiency. The phase noise contribution from the transmitter itself assuming a perfectly clean clock is simulated at peak output power and 6 dB backed-off output power as shown in Fig. 14. It can be seen that the phase noise at 45 MHz offset from the carrier is as low as -168.6 dBc/Hz at 6 dB back-off which implies that the transmitter itself is not a dominant contributor of phase noise. However, it must still be noted that the notch will be limited to the phase noise level of the input clock from the synthesizer (external signal generator in our case) whose phase-noise requirement is at least as low as the desired noise floor in the RX-band after FIR (-155 to -160 dBc/Hz).

B. Power Amplifier Passive Network

The output passive network of the DTX is shown in Fig. 15. In order to minimize the mismatch in impedance seen by each tap looking into the transformer combiner due to combiner asymmetry, a purely differential configuration is chosen, since 4-way single-ended transformer combiners inherently exhibit asymmetry across the taps. The single-ended $50\ \Omega$ load is transformed to a differential $50\ \Omega$ via an off-chip balun. This differential $50\ \Omega$ is transformed using an L-match circuit consisting of an off-chip capacitor and wire-bond inductances to present a differential $23\ \Omega$ at 2.2 GHz.

The transformer combiner then transforms it to $3.4\ \Omega$ differential load resistance at the input of each section of the transformer combiner and an inductance that resonates with the series capacitance of each differential switched-capacitor RFDAC at 2.2 GHz.

The transformer combiner is designed with a turns ratio of 1 with $500\ pH$ of inductance. A coplanar layout is chosen for the transformers with the primary and secondary windings on the same thick metal layer to minimize the interwinding coupling capacitance. The primary winding is split in half and straddles the secondary winding [10]. The spacing between them is adjusted to optimize the coupling coefficient while minimizing the interwinding capacitance. While maximizing the coupling coefficient improves the efficiency of the combiner, the interwinding capacitance causes the transfer functions from each single-ended input terminal of the transformer combiner to the differential output to be non-identical [32]. Minimizing this capacitance is a key to achieve identical weights for all taps in the FIR structure (Fig. 5) and in turn, a good rejection at the notch frequency. The transformer combiner and the output L-match network have a combined simulated efficiency of 62%. The primary and secondary windings have quality factors of 10.7 and 9.7, respectively, at 2.2 GHz, while the coupling coefficient is 0.72. The simulated total interwinding capacitance per section of the 2-way transformer combiner is approximately $300\ fF$. The 2-way transformer combiner is simulated using ideal voltage-sources at all the four inputs to represent the RFDAC taps. The voltage sources are 2.2 GHz carrier signals with a swept baseband tone. The baseband tone in each voltage-source is delayed by the appropriate amount to form different FIR configurations. Notch offset frequencies of 50 and 100 MHz with 2-tap and 3-tap configurations emulated by the 4-tap structure with equal weights and delay appropriately set are simulated to determine the effect of the coupling capacitance on the final response. It can be seen in Fig. 16 that a worst case notch rejection of 46 dB is observed which is more than sufficient to suppress the quantization noise floor of the DTX to below -170 dBc/Hz.

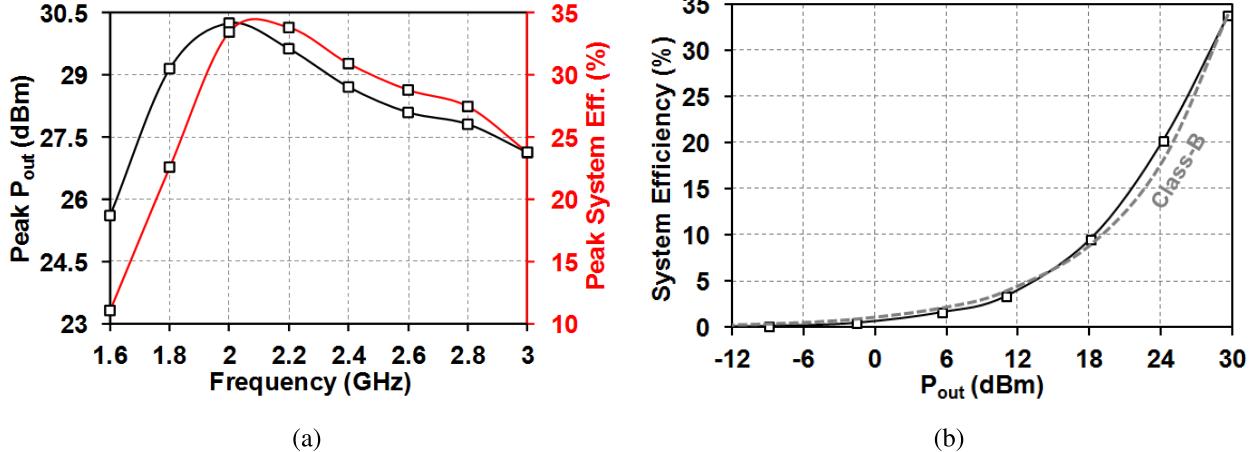


Fig. 20. (a) Measured saturated output power and system efficiency at saturated output power across frequency. (b) Measured efficiency under back off at 2.2 GHz.

C. Programmable Sub-Sample-Period Delay Generator

The circuit diagram of the programmable sub-sample-period delay generators is shown in Fig. 17. Shift registers clocked by the sampling clock are used to delay decoded I/Q data by integer multiples of the clock period. The MUX controls are used to select the appropriate output of the shift registers to set the desired amount of “coarse” delay of each tap. Each RFDAC tap has its own coarse delay generator. The coarse delay generators are synthesized from Verilog code using the standard digital cell library. In order to obtain sub-sample-period delays, the clock is first passed through an inverter-based delay line on-chip. The delay line is tapped at regular intervals and the outputs are MUXed using four independent MUXes to obtain a delayed clock for each RFDAC tap. The delayed clocks are fed to the shift-registers of the respective coarse delay generator of each tap. Since the fine delay is set by inverter delays, a common delay line is used for all the taps to reduce timing mismatches. A resolution of around 50 ps and a maximum delay of 1.55 ns are obtained in this implementation. Sub-sample-period delay generators allow more flexibility in the location of notches in the FIR response. For instance, with only the coarse delay generators exercised, two of the consecutive notch offset frequencies possible are 112 and 140 MHz. However, by exercising the sub-sample-period delay generators, the intervening frequencies are adequately covered.

D. High-Speed Deserializer

In order to be able to conveniently test the DTX at high sampling rates in a packaged setting, a high-speed deserializer is integrated on-chip (Fig. 18). Two separate deserializers, one for the serial I data and Q data each, with a common clock divider path are implemented. The serial data and clock are fed to the deserializer differentially and are converted to single-ended signals on-chip using current-mode logic buffers. The serial clock is divided by a factor of 9 to generate the f_{samp} clock which is the effective baseband sample rate. The targeted f_{samp} is 560 MHz which implies a serial data-rate of 5.04 GS/s. The serial I/Q data pass through a chain of nine true

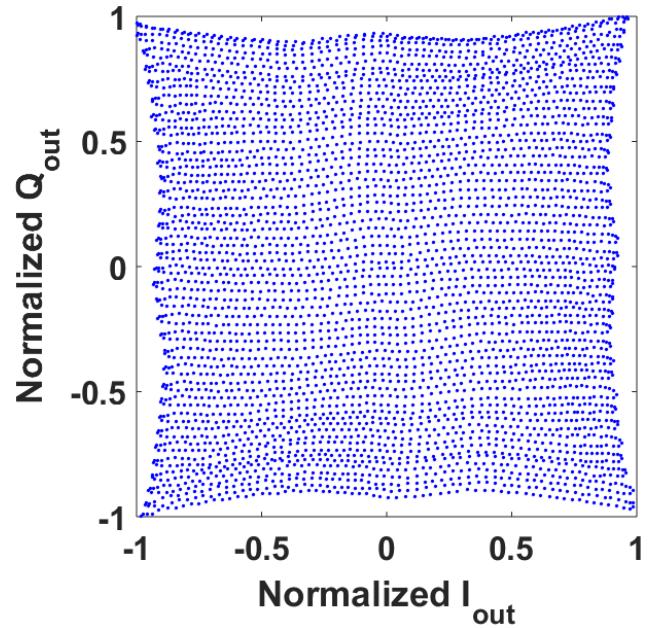


Fig. 21. Measured DTX 2-D nonlinearity at 2.2 GHz.

single-phase clock (TSPC) D flip-flops with carefully timed clock signals. This structure essentially forms a high-speed shift register. The outputs of the TSPC D flip-flops are then re-timed using static-logic D flip-flops with the f_{samp} clock to obtain the parallel 9-bit I/Q data samples.

V. MEASUREMENT RESULTS

The switched-capacitor DTX is fabricated in a 65 nm CMOS process. It occupies an area of 3 mm² including pads. The chip photograph is shown in Fig. 19(a). It is packaged in a 40-pin Quad Flat No-leads and mounted on a high-speed printed circuit-board for testing as shown in Fig. 19(b).

A. Static Measurements

The peak performance of the DTX is measured by setting the I/Q DCWs to their maximum value of +255 and sweeping

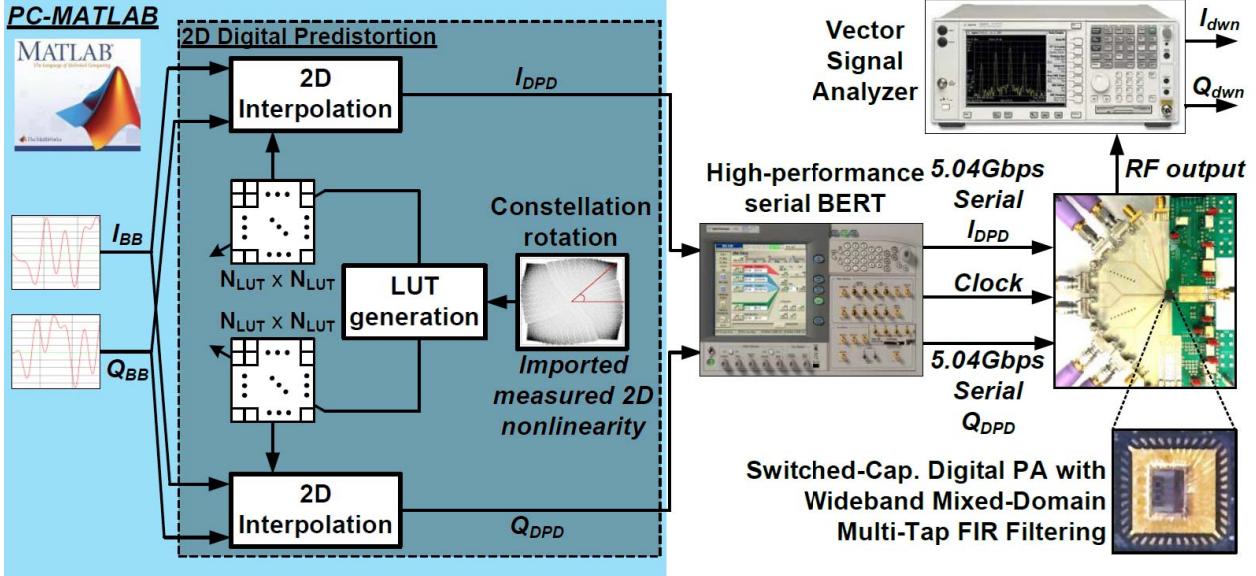


Fig. 22. Measurement setup used for the modulated signal tests on the DTX.

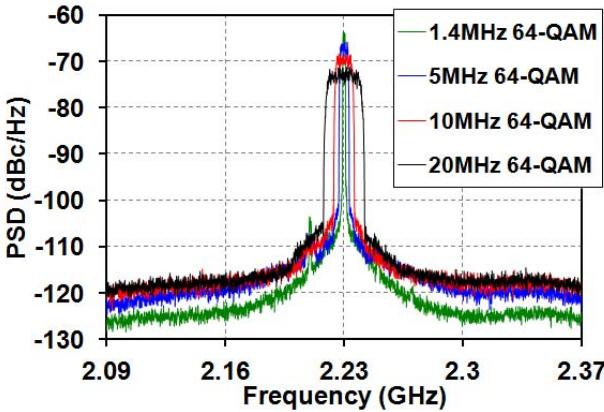


Fig. 23. Measured close-in PSD of predistorted single-carrier 64-QAM signals with different BWs at 2.23 GHz.

the LO input frequency. Fig. 20(a) shows the peak output power and system efficiency across frequency. The loss of the output L-match network excluding the balun is included in these measurements. It is seen that a saturated output power of 30.3 dBm at a system efficiency of 34% is observed at 2.2 GHz. The efficiency under back-off profile measured at 2.2 GHz in Fig. 20(b) follows a Class-B profile.

The 2-D nonlinearity of the DTX is measured by sweeping the I and Q DCWs across all possible combinations. The downconverted I/Q outputs of the DTX are plotted in Fig. 21. A fairly linear profile across DCW settings is seen especially in comparison to the 2-D nonlinearities of the current-combined digital PAs in [7], [14], and [15].

B. Modulated Signal Measurements

Fig. 22 shows the measurement setup used for the modulated signal tests. The 2-D nonlinearity of the DTX is imported into MATLAB. A 2-D search is performed on it to generate

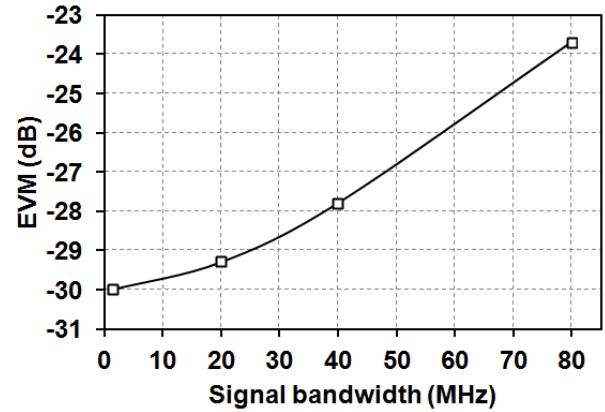


Fig. 24. Measured EVM across signal BW.

64×64 element lookup tables for I and Q each. Cubic 2-D interpolation is performed on the LUTs to generate predistorted versions I_{DPD}/Q_{DPD} of the modulated baseband digital signals I_{BB}/Q_{BB} . A detailed description of the predistortion procedure can be found in [29]. I_{DPD}/Q_{DPD} signals are stored in the memory of a high-performance serial bit error rate tester (BERT). The BERT is only used to generate the high-speed serialized versions of I_{DPD}/Q_{DPD} . The serial data along with the serial clock is fed to the DTX. The output of the DTX is observed on a vector signal analyser.

A predistorted 20 MHz 64-QAM signal is fed at a serial rate of 5.04 GS/s (effective RFDAC $f_{samp} = 560$ MHz) to the DTX operating at 2.23 GHz. The measured average output power is 24 dBm (6 dB PAPR) with a system efficiency of 16%. Fig. 23 shows the close-in PSD of the output of the DTX for predistorted single-carrier 64-QAM signals with 1.4, 5, 10, and 20 MHz BWs. The measured EVM of demodulated signals across signal BWs is shown in Fig. 24. The EVM of a 1.4 MHz 64-QAM signal is -30 dB and degrades

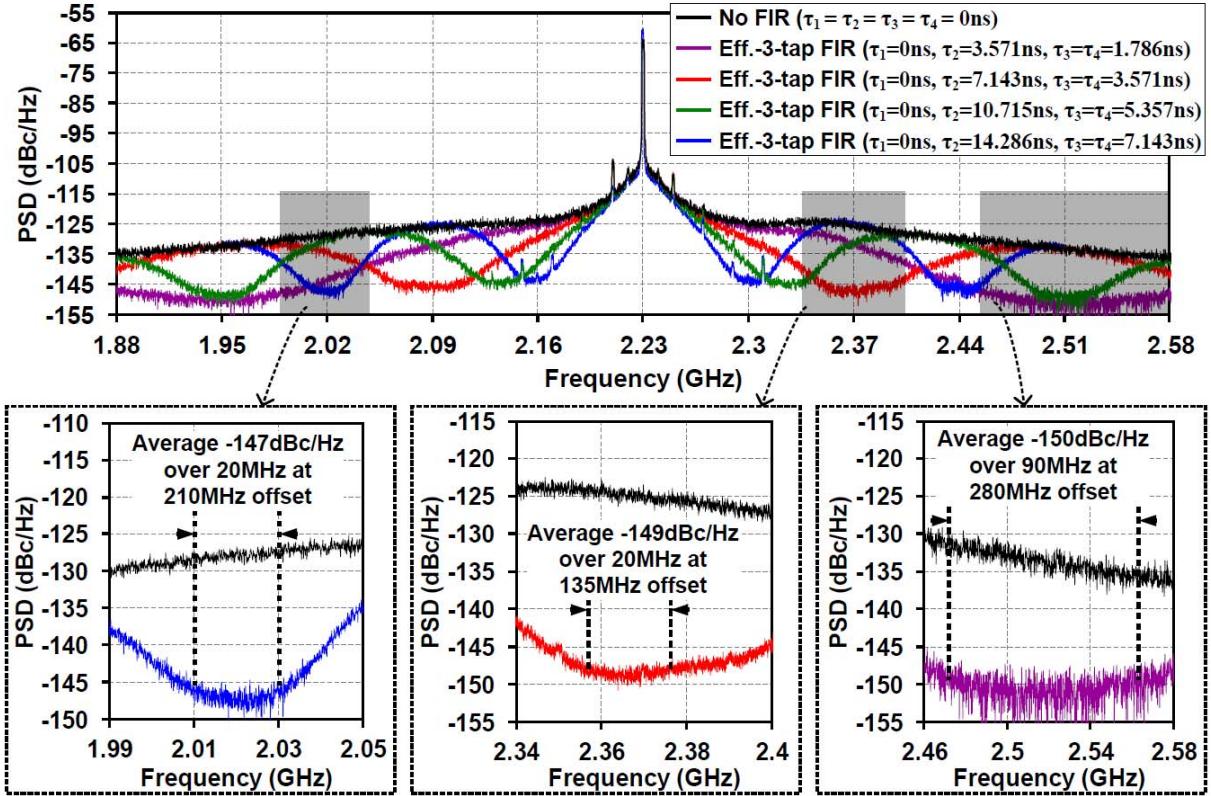


Fig. 25. Measured PSD of a 1.4-MHz single-carrier 64-QAM signal for various filter configurations.

as BW increases to about -23.8 dB for an 80 MHz 64-QAM signal. This is because a simple static 2-D DPD algorithm is used here which does not account for the memory effects that become more apparent at larger BWs. Memory-based DPD can improve the EVM by capturing memory-effects in the non-linearity of the DTX at the expense of increased computational resources and training periods for the DPD algorithm. The measured adjacent channel power ratio for the 20 MHz BW signal is -36.5 dB.

Fig. 25 shows the effect of mixed-domain multi-tap FIR on the PSD of a predistorted 1.4 MHz single-carrier 64-QAM signal. The transmitter is operating at an LO frequency of 2.23 GHz, while the sampling rate is 560 MHz. Without the embedded mixed-domain FIR turned ON, the transmitter has a noise floor of -125 dBc/Hz at an offset of 135 MHz from the carrier [Fig. 25 (black curve)]. With the transmitter configured as an effective-3-tap FIR ($\tau_1 = 0$ ns, $\tau_2 = 7.143$ ns, $\tau_3 = \tau_4 = 3.571$ ns), the noise floor is suppressed by 24 dB achieving -149 dBc/Hz averaged over a BW of 20 MHz at the same offset frequency [Fig. 25 (red curve)]. The delays of each tap for this effective 3-tap configuration are chosen using the transfer function in (4). To demonstrate tunability of the notch frequency, the delays of the effective-3-tap FIR are changed to $\tau_1 = 0$ ns, $\tau_2 = 3.571$ ns, and $\tau_3 = \tau_4 = 1.786$ ns, which place the notch at an offset of 280 MHz from the carrier [Fig. 25 (purple curve)]. Here, it is seen that the FIR suppresses the noise floor by >20 dB to reach -150 dBc/Hz over a BW of 90 MHz. Two other effective-3-tap FIR configurations are shown in Fig. 25. One configuration has notch frequencies

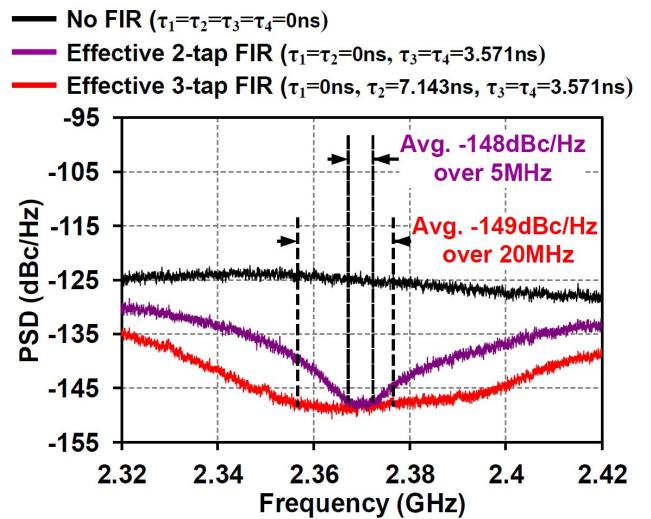


Fig. 26. Measured PSD in the notch region (~ 140 MHz offset) of a 1.4-MHz single-carrier 64-QAM signal for effective-2-tap and effective-3-tap FIR configurations.

at 70 and 210 MHz offsets (blue curve). An average noise floor of -147 dBc/Hz over 20 MHz is achieved in this configuration at the 210 MHz offset. The other configuration has notch frequencies at 100 and 280 MHz offsets (green curve) from the carrier. The output power and average efficiency show no measurable degradation between the cases when FIR is turned ON and OFF. This is because the BW of the passband of the FIR filter is chosen to cause negligible attenuation to the

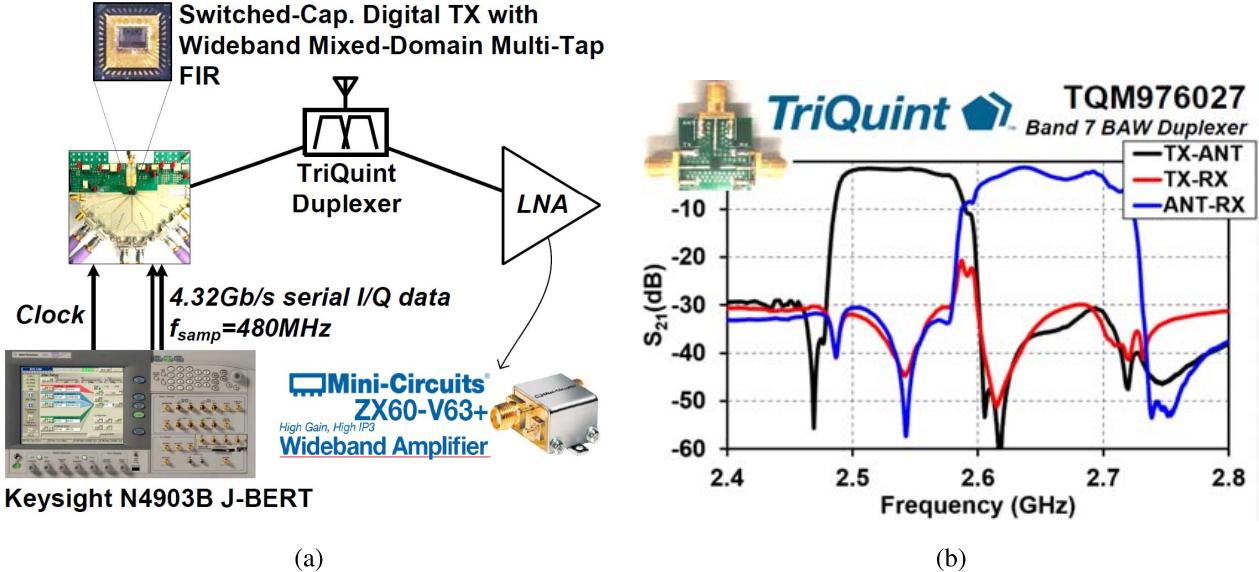


Fig. 27. (a) FDD demonstration with the implemented prototype using a commercial TriQuint duplexer. (b) Measured duplexer characteristics.

desired signal while the quantization noise which is already ~ 70 dB below the desired signal is significantly attenuated.

Measurements are also performed with a 20 MHz single-carrier 64-QAM signal with different FIR configurations. The measured noise floors at 135 and 280 MHz offsets from the 2.23 GHz carrier are -140 dBc/Hz (suppression of 22 dB) and -145 dBc/Hz (suppression of 19 dB), respectively, with FIR turned ON. The degradation in noise floor levels for the larger BW signal is primarily due to the mechanism described in Section III.

The benefit of having a 4-tap mixed-domain FIR filter in the configuration described in Section III-B is shown in Fig. 26. The region of the PSD at an offset of 140 MHz from the carrier is considered. An effective-2-tap FIR configuration is emulated by setting the delays as $\tau_1 = \tau_2 = 0$ ns, $\tau_3 = \tau_4 = 3.571$ ns. It is seen that the noise floor is -148 dBc/Hz over a BW of 5 MHz (purple curve). The DTX is then configured as an effective-3-tap FIR with the delays set as $-\tau_1 = 0$ ns, $\tau_2 = 7.143$ ns, $\tau_3 = \tau_4 = 3.571$ ns. The BW of suppression improves drastically to 20 MHz (red curve) clearly demonstrating the advantage of having multiple taps.

C. FDD Demonstration

The DTX is tested in an FDD setup shown in Fig. 27(a). The DTX and a commercial off-the-shelf low-noise amplifier (LNA) [33] are attached to a band 7 duplexer [34]. The duplexer's measured characteristics are shown in Fig. 27(b). For this demonstration, we set the transmitter's carrier frequency at 2.5 GHz and the duplex offset to be 120 MHz. The duplexer's TX–RX isolation varies from 46 to 50 dB over the considered receiver frequency range.

When the transmitter is OFF, the cascaded NF of the LNA and duplexer is dominated by the LNA's noise and the duplexer's insertion loss. This is measured to be ~ 6 dB in the RX band [Fig. 28 (black line)]. The DTX is turned ON and a predistorted 1.4 MHz 64-QAM signal is fed to it

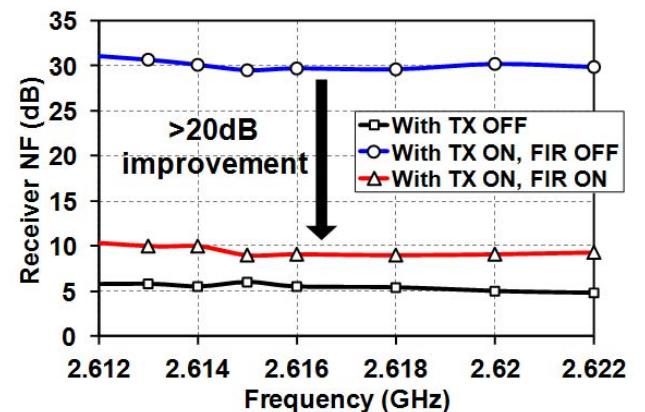


Fig. 28. Measured cascaded NF of the duplexer and LNA with the transmitter OFF, transmitter ON and FIR OFF, and with the transmitter ON and FIR ON.

at $f_{\text{samp}} = 480$ MHz. The measured average output power is 21 dBm at the DTX output. The delays of all taps are set to be identical to each other effectively turning OFF any mixed-domain FIR filtering. In this scenario, the upconverted baseband quantization noise severely degrades the duplexer-LNA NF to ~ 30 dB in the RX band [Fig. 28 (blue line)]. The DTX is then configured as an effective-3-tap FIR by setting $\tau_1 = 0$, $\tau_2 = 8.333$ ns, and $\tau_3 = \tau_4 = 4.167$ ns. This places a wideband notch at 120 MHz offset from the carrier, thereby, suppressing the quantization noise in the RX band. The cascaded duplexer-LNA NF is measured to be ~ 9 dB [Fig. 28 (red line)] > 20 dB improvement over the baseline case with FIR turned OFF. In summary, the switched-capacitor DTX with wideband mixed-domain FIR filtering of quantization noise only degrades the NF of the duplexer-LNA by 3 dB as opposed to > 23 dB with FIR turned OFF. This demonstration proves that the switched-capacitor DTX with wideband mixed-domain FIR filtering is a promising candidate for wireless FDD and coexistence scenarios.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	JSSC 2011 [1]	ISSCC 2013 [2]	ISSCC 2013 [3]	RFIC 2013 [4]	RFIC 2015	This work
Architecture	Switched-capacitor digital polar TX	Class D ⁻¹ current-combined digital polar TX with dynamic load modulation	Class D ⁻¹ current-combined digital IQ TX	Class E/F _{odd} digital IQ TX with embedded 2-tap mixed-domain FIR	Switched-capacitor digital IQ TX	Switched-capacitor Digital IQ TX with IQ bit Reuse and Embedded Sub-sample 4-tap Mixed-domain FIR
Frequency	2.25 GHz	2.2 GHz	2.44 GHz	2.4 GHz	2 GHz	2.2 GHz
Resolution	6b amplitude, off chip phase mod.	8b amplitude, 9b phase	13b IQ	9b IQ	7b IQ	9b IQ
Sampling freq.	160 MHz	1 GHz	800 MHz	200 MHz	190 MHz	560 MHz
Peak Power	25.2 dBm	23.3 dBm	24.7 dBm	29.9 dBm	20.5 dBm	30.3 dBm
Peak System Efficiency	45%	43%	37%	38%	20%	34%
Modulation Waveform	802.11g OFDM 64-QAM	802.11g OFDM 64-QAM	802.11g OFDM 64-QAM	Single-carrier 64-QAM	LTE OFDM 64-QAM	Single-carrier 64-QAM
Avg. Power	17.7 dBm	16.8 dBm	18.8 dBm	18.6 dBm	14.5 dBm	24 dBm
Backoff + PAPR	7.5 dB	6.5 dB	5.9 dB	11.3 dB	6 dB	6.5 dB
Avg. Efficiency	27%	19.3%	17%	14.4%	12.2%	16%
Noise-floor at 140MHz offset	-113.5 dBc/Hz*	-135 dBc/Hz*	-133 dBc/Hz*	-134 dBc/Hz* at 100MHz frequency offset with FIR	-123 dBc/Hz*	-149 dBc/Hz over a BW of 20MHz with FIR

RFIC 2015 - W. Yuan, V. Aparin, J. Dunworth, L. Seward and J. S. Walling, "A quadrature switched capacitor power amplifier in 65nm CMOS," 2015 IEEE RFIC Symp., Phoenix, AZ, 2015, pp. 135-138.

NA - Not available

*Estimated from graphs.

Table I compares this paper with the prior RF DTXs having >20 dBm peak output power. This paper achieves superior RX band noise floor by 14 dB or 25×, while simultaneously achieving the highest peak output power in the table. It is noteworthy that this work approaches the challenging FDD RX band noise requirements which can be fully satisfied with margin by adding an effective bit and by doubling the sampling rate.

VI. CONCLUSION

A fundamental challenge of using DTXs for FDD and in coexistence scenarios is the unfiltered quantization noise that leaks into the RX band. A multi-tap mixed-domain FIR filtering approach is proposed to overcome this limitation. A highly linear SCPA in conjunction with transformer-based power combining is used to improve the ENOB and linearity of FIR summation. A fully integrated high-power DTX which achieves -149 dBc/Hz noise floor in the RX band over a BW of 20 MHz at 24 dBm of output power is demonstrated. Employing memory-based DPD to help compensate for the residual nonlinearity after static DPD to improve notch depth and combining the mixed-domain FIR filtering approach with average efficiency enhancement techniques such as Doherty and Class-G are topics for the future research.

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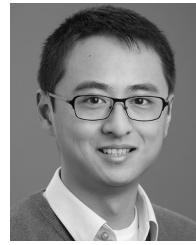
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