

A 0.0021 mm² 1.82 mW 2.2 GHz PLL Using Time-Based Integral Control in 65 nm CMOS

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Abstract—Modern multicore processors employ multiple phase-locked loops (PLLs) to operate individual cores at a power-optimal frequency. This paper presents techniques to implement such PLLs in a small area. The area occupied by classical charge-pump-based analog PLLs is mostly due to the large loop filter capacitor needed to implement the integral control portion of type-II response. Digital PLLs (DPLL) can eliminate the capacitor by implementing the integral control in digital domain but their jitter performance is degraded by the quantization error introduced by DPLL building blocks such as a time-to-digital converter (TDC). We seek to combine the advantages of analog (no quantization error) and digital (small area) PLLs by implementing the integral control using time-based techniques. To this end, a ring oscillator-based integrator (ROI) is used to implement the integral control. ROI integrates its input and generates an output in the form of a pulse-width modulated (PWM) signal. While the ROI does not introduce quantization error, controlling the voltage controlled oscillator with the PWM signal introduces undesirable spurious tones. We propose to use a pseudo-differential ROI to mitigate these tones and achieve good jitter performance. Fabricated in 65 nm CMOS LP process, the prototype PLL occupies an active area of only 0.0021 mm² and operates across a supply voltage range of 0.6 V to 1.2 V providing 0.4–2.6 GHz output frequencies. At 2.2 GHz output frequency, the PLL consumes 1.82 mW at 1 V supply voltage, and achieves 3.73 psrms integrated jitter. This translates to an FoM_J of -226.0 dB, which compares favorably with state-of-the-art designs while occupying the smallest reported active area.

Index Terms—Analog PLL (APLL), current controlled ring oscillator (CCRO), digital PLL (DPLL), integer-N, jitter, oscillators as integrators, pulse width modulation (PWM), ring oscillator integrator (ROI), ring oscillators, phase-locked loops (PLLs).

I. INTRODUCTION

PHASE-LOCKED loops (PLLs) are widely used in analog, digital, RF, and embedded systems to generate a high frequency clock from a low-frequency reference clock. Modern processors and systems-on-chip (SoCs) utilize multiple PLLs

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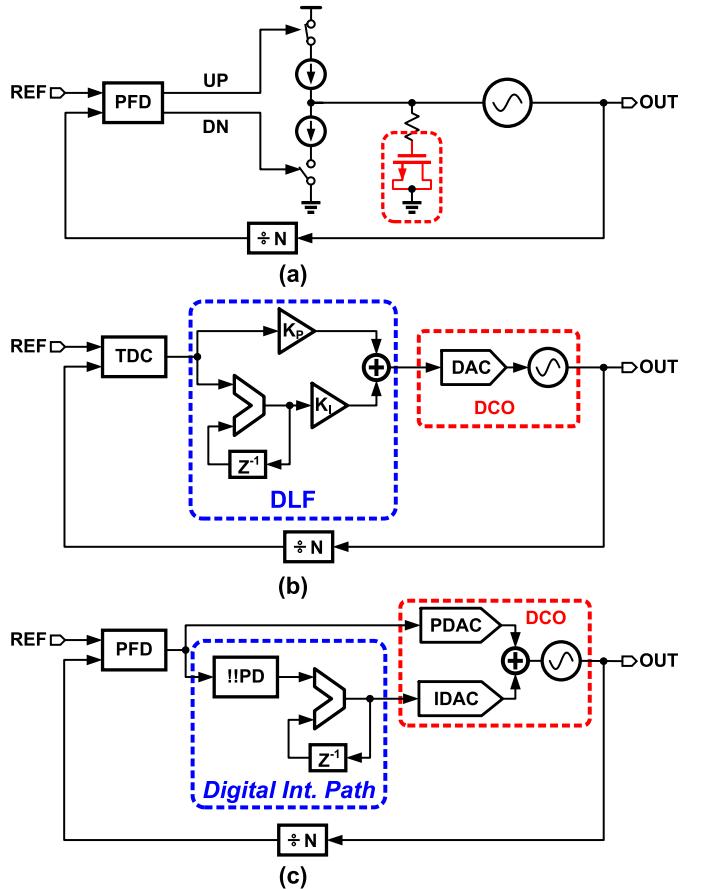


Fig. 1. Conventional PLL architectures: (a) charge-pump based analog PLL, (b) digital PLL, and (c) hybrid PLL.

to cater to varying demands of modules such as multicore processors, memories, I/O interfaces, and power management. If each of these PLLs occupy large area, the total area occupied by PLLs will become a significant portion of the SoC area. Therefore, it is important to implement these PLLs in an area-efficient manner without degrading their jitter or increasing power consumption.

Analog ring oscillator-based charge-pump PLLs have been traditionally used to generate clocks in processors [1]. As depicted in Fig. 1(a), this architecture implements the desired type-II response efficiently by using only a charge pump, resistor, and capacitor. However, loop filter capacitor

occupies large area and is typically the major bottleneck in reducing PLL area. For instance, achieving a PLL bandwidth of 3 MHz and phase margin of 70° requires a capacitance of 300 pF (with $R = 1 \text{ k}\Omega$) to place the loop stabilizing zero frequency at ten times lower than the PLL bandwidth. In 65 nm CMOS process, with capacitor density of $1 \text{ fF}/\mu\text{m}^2$, this capacitance occupies an active area of 0.3 mm^2 . Process scaling further exacerbates this issue because: 1) increasing oscillator gain increases the needed capacitor value and 2) leakage current prohibits the usage of high-density MOS capacitors.

Digital PLLs (DPLLs) offer a means to eliminate the capacitor by implementing loop filter in the digital domain [2]. Specifically, as shown in Fig. 1(b), integral control is realized by using a digital accumulator in place of a capacitor. A time-to-digital converter (TDC) acts as a digital phase detector and digitizes phase difference between the reference clock and divider output and feeds it to the digital loop filter (DLF). A digital-to-analog converter (DAC) converts the DLF output to analog voltage and drives the voltage controlled oscillator (VCO) toward phase/frequency lock. A major drawback of a DPLL is the degraded jitter performance due to the quantization error of TDC. Lowering the amount of TDC quantization error requires a high-resolution TDC, which increases power dissipation. On the other hand, reducing the contribution of TDC quantization error by filtering it imposes conflicting noise bandwidth requirements. For instance, suppressing TDC quantization error by lowering the PLL loop bandwidth increases the contribution of VCO phase noise and *vice versa*. Therefore, DPLLs require either a high-resolution TDC or a low-phase-noise VCO, both of which increase power consumption.

A hybrid PLL (HPLL) [3] was proposed to circumvent conflicting noise bandwidth tradeoffs in conventional DPLLs [Fig. 1 (c)]. Based on the observation that most of the TDC quantization error in a DPLL leaks to the output through the digital proportional path, HPLL uses analog proportional path to completely eliminate the quantization error. Because integral control path bandwidth has minimal impact on VCO phase noise, quantization error in the integral control path is minimized by reducing its noise bandwidth. However, a high-resolution DAC that converts accumulator output into a control voltage occupies a large chip area [4] and reduces area savings of D/HPLLs. Implementing the DAC using a delta-sigma architecture may reduce the number of unit elements in the DAC but the low-pass filter required to filter high-frequency quantization error typically occupies a large area [3].

In this paper, we seek to reduce the area of PLLs while combining the advantages of analog (no quantization error) and digital (smaller area) PLLs. To this end, we propose to use a ring oscillator as an integrator in conjunction with a conventional analog proportional path to eliminate quantization error in both integral and proportional paths. Because of its highly digital nature, the prototype PLL occupies small active area of 0.0021 mm^2 and is capable of operating across a supply voltage range of 0.6 to 1.2 V while generating output frequencies in the range of 0.4 to 2.6 GHz. The PLL consumes 1.82 mW when operating at 1 V supply voltage and achieves an integrated jitter of $3.73 \text{ ps}_{\text{rms}}$ at 2.2 GHz output frequency.

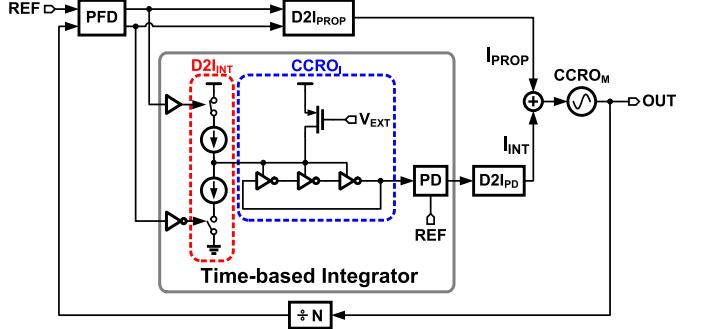


Fig. 2. Implementation of time-based integrator with ring oscillator.

The remainder of this paper is organized as follows. Section II presents the proposed architecture. Section III describes design challenges, and techniques to mitigate them are presented in Section IV. Circuit implementation details of key building blocks are presented in Section V. Experimental results from the test chip are presented in Section VI. Key contributions of this paper are presented in Section VII.

II. PROPOSED ARCHITECTURE

A simplified block diagram of the proposed PLL is shown in Fig. 2 [5]. It consists of a tri-state phase frequency detector (PFD), duty-cycle to current converters (D2I), a time-based integrator, a current controlled ring oscillator (CCRO_M), and a feedback frequency divider. A D2I converter, D2I_{PROP}, converts three levels of the PFD output (UP, DN, RESET) to three discrete currents ($2I_B$, 0 , I_B) and injects them directly into CCRO_M, thus implementing proportional control portion of the Type-II response much like in an APLL [3]. Integral control is implemented using the time-based integrator as described next.

Before describing details of the integral control, it is instructive to briefly review the behavior of current (or voltage)-controlled ring oscillator-based integrators [6], [7]. Because output frequency of a CCRO (F_{CCRO}) is proportional to its input current (and phase is integral of frequency), CCRO acts as a current to phase integrator with the following transfer function:

$$\frac{F_{\text{CCRO}_I}(s)}{i_{\text{in}}(s)} = K_{\text{CCRO}_I} \implies \frac{\Phi_{\text{CCRO}_I}(s)}{i_{\text{in}}(s)} = \frac{K_{\text{CCRO}_I}}{s} \quad (1)$$

where i_{in} and Φ_{CCRO_I} denote CCRO_I input current and output phase, respectively. In other words, a CCRO performs true lossless integration independent of transistor imperfections and supply voltage. The time constant of the CCRO integrator is equal to the inverse of its current-to-frequency gain K_{CCRO_I} .

In order to use CCRO as an integrator, a means to convert its output phase into a voltage (or current) signal is needed. One way to perform this conversion is by using a phase detector (PD) that compares the CCRO phase with the phase of a reference clock and generates a PWM voltage signal as depicted in Fig. 3 [7]. The pulse width (or, equivalently, the duty cycle) of the PD output is a measure of the CCRO phase. Note that, if CCRO free running frequency is not equal to

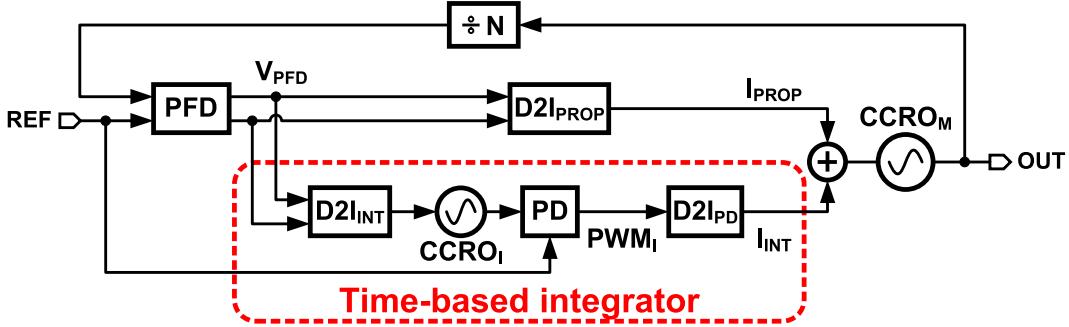


Fig. 3. Block diagram of the proposed time-based PLL architecture.

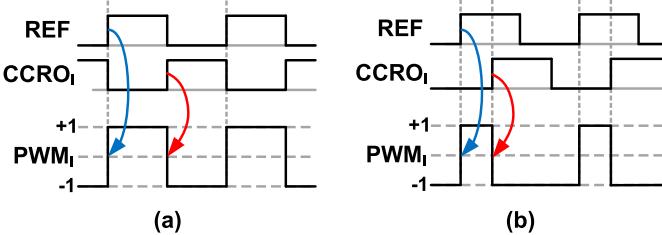


Fig. 4. Time-domain waveform of time-based integrator with input phase difference of (a) π and (b) 0.5π .

the reference frequency, phase error accumulates indefinitely, which saturates the PD output. This is analogous to amplifier output saturation due to input DC offset in conventional voltage-mode integrators. Therefore, to prevent PD saturation, any system using a CCRO integrator must ensure that CCRO frequency is equal to the reference frequency in steady state.

Now, consider the time-based integrator depicted in Fig. 3. The PFD output is first converted to current by $D2I_{INT}$ and subsequently integrated by a CCRO denoted as $CCRO_I$. Because output of $CCRO_I$ is in phase domain, it is first converted into a two-level PWM voltage signal by a PD. As shown in Fig. 4, for example, the PD output with a phase difference of π radians between $CCRO_I$ and reference shows a duty cycle of 50%. The duty cycle changes to 25% when the phase difference is changed to 0.5π . A D2I converter $D2I_{PD}$ converts 2-level PD output into current and feeds it into the main CCRO, $CCRO_M$, thus implementing integral control portion of the Type-II response. It is worth mentioning that, even though the PD output takes only CMOS levels, no quantization error is introduced by the time-based integrator.

As shown in Fig. 3, output oscillator $CCRO_M$ is controlled via the proportional and integral path D2I converter currents, denoted as I_{PROP} and I_{INT} , respectively. The PWM PFD (or PD) output is converted into current using D2I converters. The gain of the D2I converter K_{D2I} is equal to

$$K_{D2I} = I_{D2I} \quad (2)$$

where I_{D2I} is the output current of D2I converter when the input duty cycle is equal to 100%. PFD output is converted to equivalent current by $D2I_{PROP}$ in the proportional path resulting in a proportional path gain of:

$$K_P = \frac{I_{PROP}}{V_{PFD}} = K_{D2I,PROP}. \quad (3)$$

where $K_{D2I,PROP}$ is the gain of $D2I_{PROP}$ and is equal to $I_{D2I,PROP}$. On the other hand, PFD output is integrated by $CCRO_I$, and the PD converts $CCRO_I$ phase to a PWM signal, which is converted to current output I_{INT} by $D2I_{PD}$. Denoting PFD output by V_{PFD} , the transfer function of the time-based integrator is equal to

$$H_{INT}(s) = \frac{I_{INT}(s)}{V_{PFD}(s)} = K_{D2I,INT} \cdot K_{PD} \cdot K_{D2I,PD} \cdot \frac{K_{CCRO_I}}{s}. \quad (4)$$

Therefore, the integral path gain is then equal to

$$K_I = K_{D2I,INT} \cdot K_{PD} \cdot K_{D2I,PD} \cdot K_{CCRO_I}. \quad (5)$$

Loop gain of the proposed PLL is thus calculated as

$$LG(s) = \frac{1}{N} \cdot K_{PFD} \cdot \frac{K_{CCRO_M}}{s} \cdot \left(K_P + \frac{K_I}{s} \right). \quad (6)$$

By equating this to the loop gain of a conventional charge-pump-based PLL, loop parameters needed to achieve the desired loop bandwidth and phase margin can be calculated.

III. IMPACT OF TIME-BASED CONTROL ON PLL PERFORMANCE

The use of a PWM signal to directly control oscillator frequency in the time-based integrator introduces spurious tones. These tones should be carefully managed to reduce their impact on the deterministic jitter performance of the PLL. This section describes the mechanisms behind the spurious tones introduced by the PWM control. Specifically, it will be shown that spurious tones arise when: 1) free-running frequency of $CCRO_I$ is not equal to F_{REF} and 2) PWM signal is fed to the $CCRO_M$ without adequate filtering.

A. Spurious Tones Due to Frequency Offset

Consider an alternate representation of the integral path shown in Fig. 5. The PFD output V_{PFD} is converted to current I_{CCRO_I} by a D2I converter that has a gain of $K_{D2I,INT}$. $CCRO_I$ converts D2I output current to frequency F_{CCRO_I} with a gain of K_{CCRO_I} . The phase error Φ_e seen by the PD is proportional to the integral of $F_{CCRO_I} - F_{REF}$ and is equal to

$$\Phi_e(t) = \int_0^t (F_{CCRO_I}(\tau) - F_{REF}) d\tau. \quad (7)$$

Because of the integration of frequency error, $CCRO_I$ frequency must be equal to F_{REF} in steady state to prevent PD

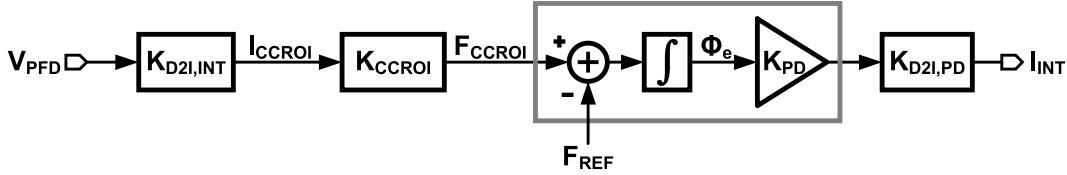


Fig. 5. Small-signal model of the time-based integral path.

output from saturating. Denoting the frequency of CCRO_I as the sum of its free-running frequency F_{FR} and additional deviation due to the input control current, F_{CCRO_I} is equal to

$$F_{CCRO_I} = F_{FR} + I_{CCRO_I} \cdot K_{CCRO_I}. \quad (8)$$

Equations (7) and (8) show that the average CCRO_I input current shall be zero if and only if the CCRO_I free-running frequency F_{FR} is equal to F_{REF} . Under this condition, average PFD output equals zero and the PLL locks without any static phase offset, barring any offsets introduced in the proportional path.

On the other hand, if the free-running frequency of CCRO_I is not equal to F_{REF} , the loop must account for the frequency difference ($\Delta F = F_{REF} - F_{FR}$) by applying adequate control current to CCRO_I such that

$$F_{CCRO_I} = (F_{REF} - \Delta F) + I_{CCRO_I} \cdot K_{CCRO_I}. \quad (9)$$

Because ΔF causes PD output duty cycle to constantly increase (or decrease if ΔF is negative), CCRO_M frequency also increases constantly. The PFD detects CCRO_M frequency deviation and produces UP/DN pulses that minimize frequency errors associated with both CCRO_I and CCRO_M. From (9), control current necessary to make $F_{CCRO_I} = F_{REF}$ is equal to

$$I_{CCRO_I} = \frac{\Delta F}{K_{CCRO_I}}. \quad (10)$$

Because nonzero I_{CCRO_I} requires PFD output to be nonzero in steady state, PLL has to lock with a static phase offset so as to simultaneously achieve $F_{CCRO_I} = F_{REF}$ and $F_{CCRO_M} = N \cdot F_{REF}$. The static phase offset resulting from $\Delta F \neq 0$ can be calculated as

$$\Phi_{OS} = \frac{I_{CCRO_I}}{K_{D2I,INT} \cdot K_{PD}}. \quad (11)$$

Static phase offset causes modulation of CCRO_M control through the proportional path, which manifests as reference spur. Using narrow-band approximation [8], the magnitude of the reference spur can be calculated as

$$\text{Spur magnitude [dB]} = 20 \log \left(\frac{F_{BW}}{F_{REF}} \cdot N \cdot \Phi_{OS} \right) \quad (12)$$

where F_{BW} is the loop bandwidth, and N is the feedback division ratio. The deterministic jitter resulting from the reference spur is equal to

$$DJ_{OUT} = \frac{2}{\pi} \cdot T_{OUT} \cdot 10^{\text{Spur[dBc]/20}}. \quad (13)$$

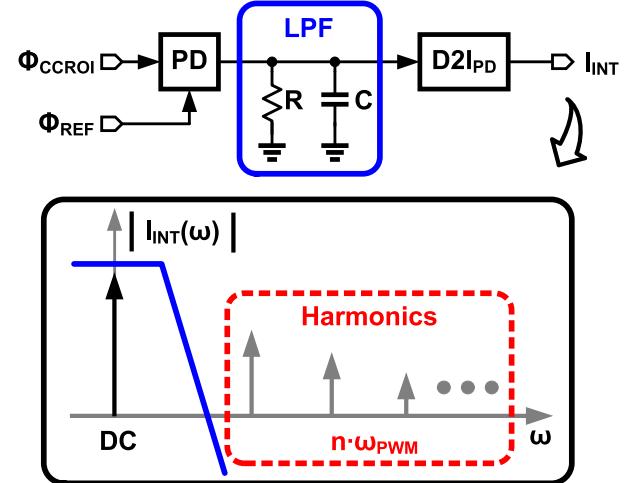


Fig. 6. Illustration of spurious tones arising from PWM control signal.

With $F_{REF} = 275$ MHz and 10 MHz bandwidth, a 1% error in CCRO_I free-running frequency gives rise to a reference spur of -27 dB, which translates to a deterministic jitter of 12.9 ps at an output frequency of 2.2 GHz.

B. Spurious Tones Due to PWM Control

The second set of spurious tones in the proposed time-based controller arise from controlling CCRO_M with PD output. As discussed earlier, the PD output is a 2-level signal with the requisite duty cycle that tunes F_{CCRO_M} to be equal to $N \cdot F_{REF}$. While modulating the frequency with current output of D2I_{INT} makes the average frequency of CCRO_M to be equal to $N \cdot F_{REF}$, perturbations of CCRO_M frequency by the PWM signal manifest as spurious tones at the PLL output. The spurs resulting from PWM control can be calculated by representing steady-state integral control signal PWM_{INT} , whose duty cycle is D and amplitude is I_0 using its Fourier series representation as [9]

$$PWM_{INT}(t) = D \cdot I_0 + \sum_{n=1}^{\infty} \frac{4I_0}{n\pi} \cdot \text{sinc} \left(n\pi \frac{2t_r}{T_{PWM}} \right) \cdot \sin(n\pi D) \cdot \cos(n\omega_{PWM} t) \quad (14)$$

where $T_{PWM} = 2\pi/\omega_{PWM}$, and t_r denotes the transition time of PWM_{INT} (assuming equal rise and fall time of the current pulse). Considering $t_r = 0$, for simplicity, and only the fundamental component at ω_{PWM} , it can be shown that the modulation generates CCRO_M output of the following form [8]:

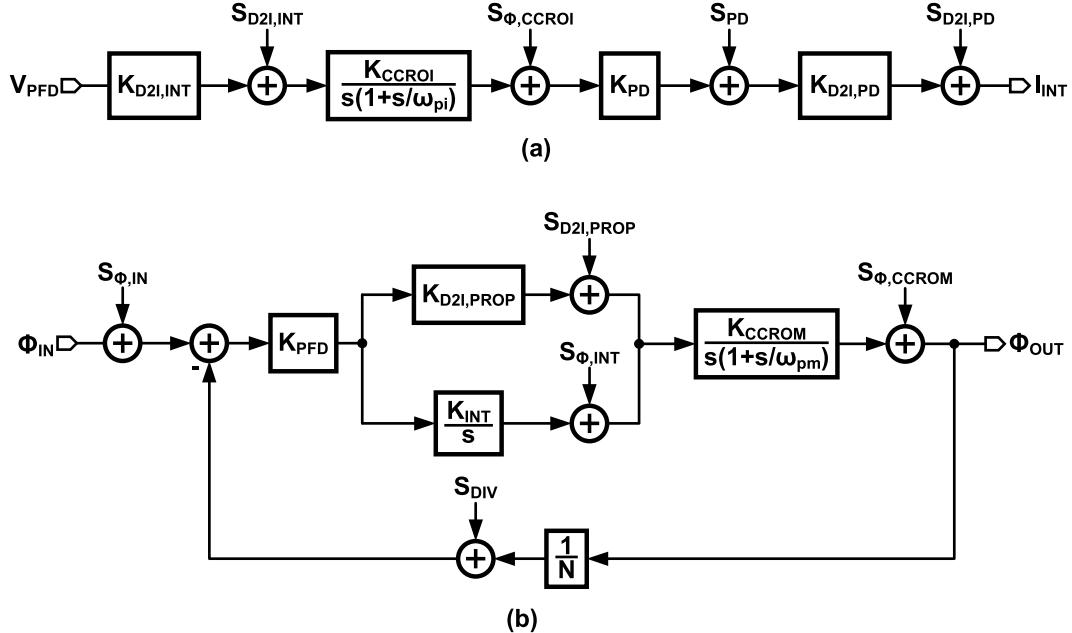


Fig. 7. Noise model of (a) time-based integrator and (b) complete PLL loop.

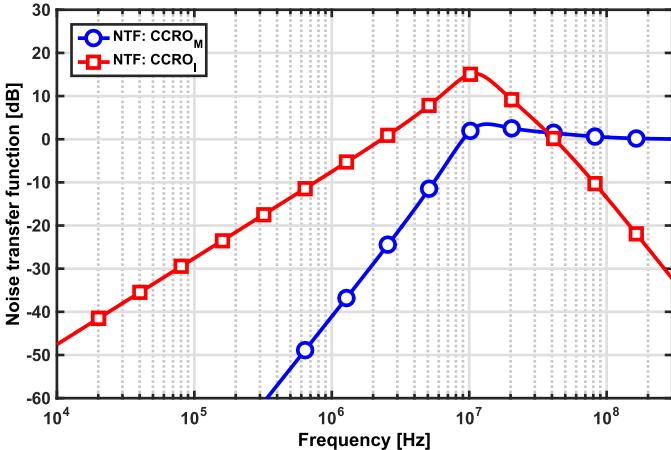


Fig. 8. Simulated CCRO_M and CCRO_I phase-noise transfer functions.

$$V_{CCRO_M}(t) = \sum_{n=0}^{\infty} J_n(\beta_0) \cdot \cos[(\omega_c \pm n\omega_{PWM})t] \quad (15)$$

where \$J_n(\beta_0)\$ represents the \$n\$th-order Bessel function, and \$J_0\$ represents the modulation index due to the fundamental component and \$\beta_0\$ is given by

$$\beta_0 = \frac{K_{CCRO_M}}{\omega_{PWM}} \cdot \frac{2I_0}{\pi} \cdot \sin(D\pi). \quad (16)$$

Under narrowband approximation, spurious tones due to PWM modulation can be estimated using (15) and (16) as

$$\text{Spur magnitude [dB]} = 20 \log \left[\frac{K_{CCRO_M}}{F_{PWM}} \cdot \frac{I_0}{\pi} \cdot \sin(D\pi) \right]. \quad (17)$$

Because \$F_{PWM} = F_{REF}\$, PLL output contains spurs at integer multiples of reference frequency.

It is possible to greatly suppress PWM modulation induced spurious tones by driving CCRO_M with the filtered PD output

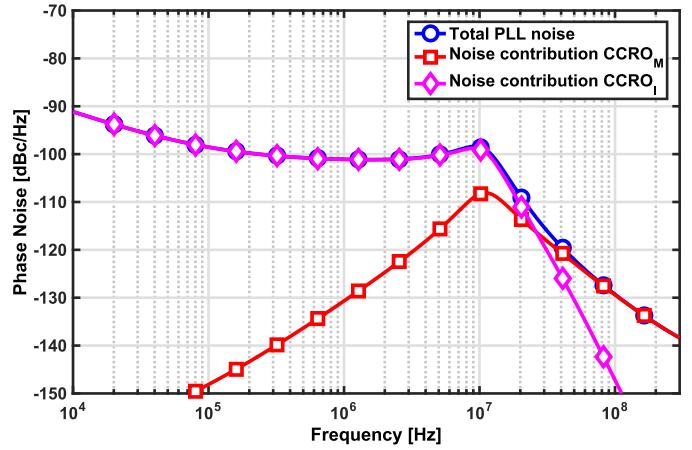


Fig. 9. Simulated output phase-noise plot.

as illustrated in Fig. 6. However, a low-bandwidth filter needed to adequately suppress the spurious tones may occupy a large area thereby mitigating the area benefit offered by the time-based control. Using M-phase PWM control as described in [7], [10] pushes spurious tones to M times the PWM frequency where they can be filtered by a higher bandwidth filter, thus reducing the area penalty by nearly M times. This technique requires replicating single phase circuitry (CCRO buffer, PD, and D2I converters) M times, which increases the controller area.

C. Noise

Compared with a conventional capacitor-based integrator, oscillator-based integrator adds more noise and degrades the PLL phase noise performance. To quantify this, consider its noise model shown in Fig. 7(a) along with the noise model of the complete PLL shown in Fig. 7(b). The output phase-noise power spectral density of the oscillator, PD, and D2I converter are denoted as \$S_{\phi, CCRO_I}\$, \$S_{PD}\$, \$S_{D2I, INT}\$, and \$S_{D2I, PD}\$,

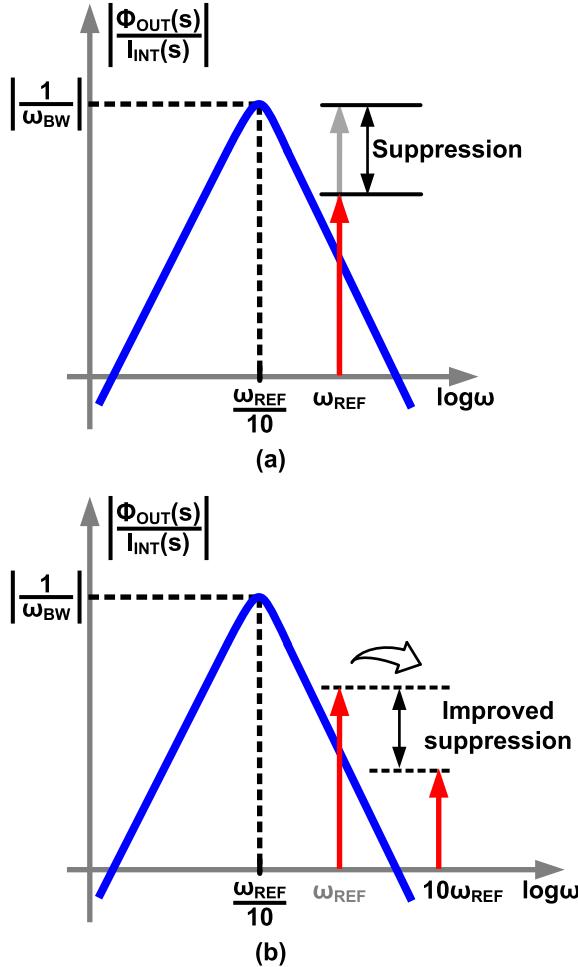


Fig. 10. Diagram of inherent suppression by PLL loop of (a) frequency spur in vicinity of loop bandwidth and (b) improved suppression of high-frequency spur.

respectively. Taking the parasitic poles associated with CCRO_I and CCRO_M into account, the loop gain transfer function shown in (6) changes to

$$\begin{aligned} \text{LG}(s) &= \frac{\Phi_{\text{OUT}}(s)}{\Phi_{\text{IN}}(s)} \\ &= \frac{1}{N} \cdot K_{\text{PFD}} \cdot \frac{1}{1 + s/\omega_{\text{pm}}} \cdot \frac{K_{\text{CCRO}_M}}{s} \\ &\quad \cdot \left(K_{\text{D2I}_{\text{PROP}}} + \frac{K_{\text{INT}}}{s} \cdot \frac{1}{1 + s/\omega_{\text{pi}}} \right) \end{aligned} \quad (18)$$

where ω_{pm} and ω_{pi} denote the parasitic poles at the output of CCRO_M and integrator CCRO_I, respectively. The noise transfer function of CCRO_M ($\text{NTF}_{\text{OUT}}^{\text{CCRO}_M}$) and CCRO_I ($\text{NTF}_{\text{OUT}}^{\text{CCRO}_I}$) are equal to:

$$\text{NTF}_{\text{OUT}}^{\text{CCRO}_M}(s) = \frac{1}{1 + \text{LG}(s)}. \quad (19)$$

$$\text{NTF}_{\text{OUT}}^{\text{CCRO}_I}(s) = K_{\text{PD}} \cdot K_{\text{D2I}, \text{PD}} \cdot \frac{1}{1 + s/\omega_{\text{pm}}} \cdot \frac{K_{\text{CCRO}_M}/s}{1 + \text{LG}(s)}. \quad (20)$$

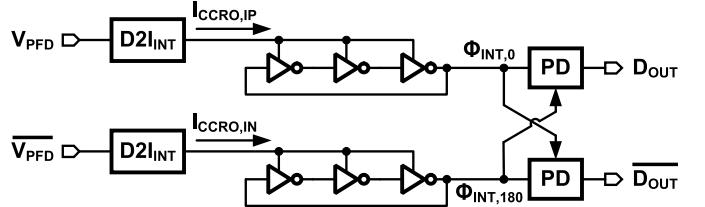


Fig. 11. Pseudo-differential implementation of time-based integrator.

where $\text{LG}(s)$ is given by (18). The output-referred noise of CCRO_M and CCRO_I is calculated to be

$$S_{\Phi, \text{OUT}}^{\text{CCRO}_M} = \left| \text{NTF}_{\text{OUT}}^{\text{CCRO}_M} \right|^2 \cdot S_{\Phi, \text{CCRO}_M} \quad (21)$$

$$S_{\Phi, \text{OUT}}^{\text{CCRO}_I} = \left| \text{NTF}_{\text{OUT}}^{\text{CCRO}_I} \right|^2 \cdot S_{\Phi, \text{CCRO}_I}. \quad (22)$$

Plotting magnitude response of the two noise transfer functions, as shown in Fig. 8, illustrates that increasing the loop bandwidth helps suppress the in-band phase-noise contribution from both CCRO_M and CCRO_I. We also note that noise from CCRO_I experiences only first-order (slope of -20 dB/dec) suppression and therefore can be expected to contribute more noise as compared with that of CCRO_M. Output phase noise plots shown in Fig. 9, assuming that CCRO_M and CCRO_I have a phase noise of -90 dBc/Hz and -94 dBc/Hz, respectively, at 1 MHz offset, show that CCRO_I dominates in-band phase noise. The integrated jitter obtained by integrating the phase noise is equal to 3 ps, of which CCRO_I accounts for 2.85 ps and CCRO_M for 1.06 ps.

IV. SPUR REDUCTION TECHNIQUES

The spur analysis in the previous section showed that the two main sources of spurs are: 1) free-running frequency error of CCRO_I from F_{REF} and 2) modulation of CCRO_M control current by a PWM signal. Before discussing ways to mitigate these spurs, it is instructive to first evaluate the impact of PLL feedback on these spurs. To this end, we first calculate the amount of phase deviations caused by control current perturbations as

$$\frac{\Phi_{\text{OUT}}(s)}{I_{\text{INT}}(s)} = \frac{K_{\text{CCRO}_M}/s}{1 + \text{LG}(s)} \quad (23)$$

where $\text{LG}(s)$ is the loop gain of the PLL and is given by (6). Plotting (23) as shown in Fig. 10(a) indicates a bandpass transfer characteristic with the peak located at around the PLL bandwidth. As a result, output phase is sensitive to control current perturbations that are in the vicinity of PLL bandwidth, while those away from it (either very low or very high frequencies) are suppressed by the loop in proportion to the ratio of PLL bandwidth to the spur frequency. Therefore, spur magnitude can be reduced either by lowering the PLL bandwidth or increasing the spur frequency. Because lowering the PLL bandwidth exacerbates CCRO_M phase noise, we consider ways to increase the spur frequency to improve spur suppression [Fig. 10(b)].

To this end, we employ the pseudo-differential time-based integrator architecture shown in Fig. 11 [7], [11]. The pseudo-differential architecture implements a 2-phase PWM control.

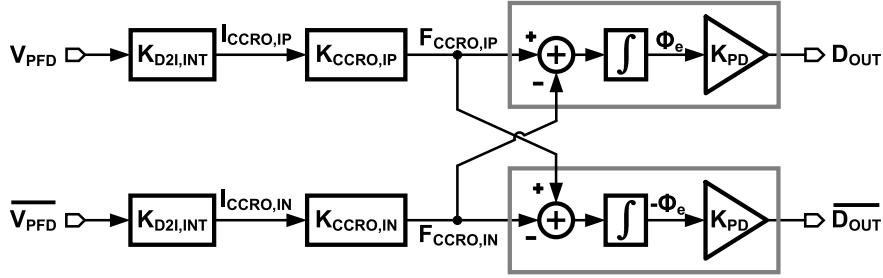


Fig. 12. Small-signal model of pseudo-differential time-based integrator.

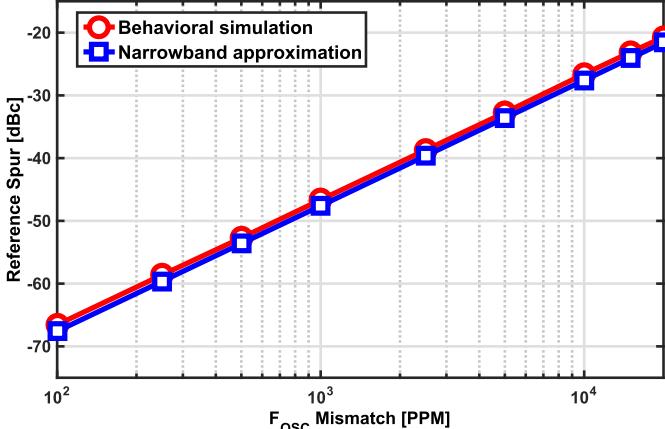


Fig. 13. Reference spur versus free running frequency mismatch between pseudo-differential oscillators with (a) behavioral simulation and (b) narrowband approximation.

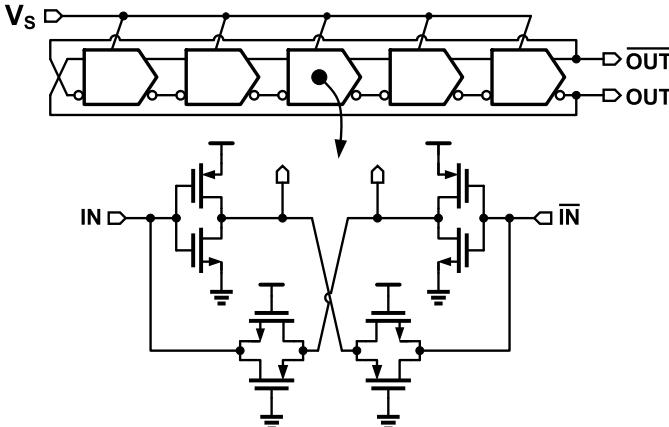


Fig. 14. Schematic of current-controlled ring oscillator.

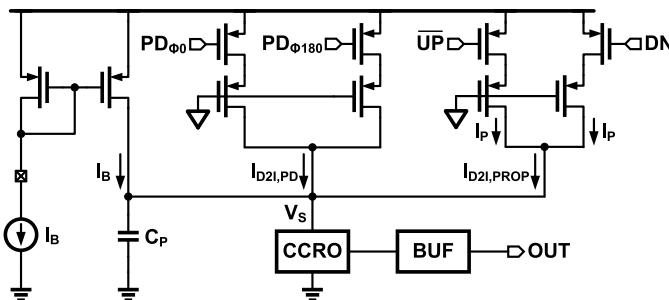


Fig. 15. Schematic of duty-cycle to current converter.

It consists of a set of D2Is that convert pseudo-differential duty cycle input into current and drive a pair of matched ring oscillators. Two PDs compare CCRO output phases, $\Phi_{INT,0}$ and $\Phi_{INT,180}$, and generate pseudo-differential PWM signals, D_{OUT} , and \bar{D}_{OUT} . This pseudo-differential integrator offers two main advantages compared to its single-ended counterpart. First, using two matched CCROs allows to operate the integrator at any switching frequency independent of the reference frequency. Consequently, by choosing the free-running frequency of the two CCROs to be much higher than the reference frequency, the PWM control induced spurs can be pushed to a high frequency where they can be greatly suppressed by the bandpass transfer characteristic of the PLL. Second, ensuring good matching between the two CCROs reduces the static phase offset, which results in a smaller reference spur.

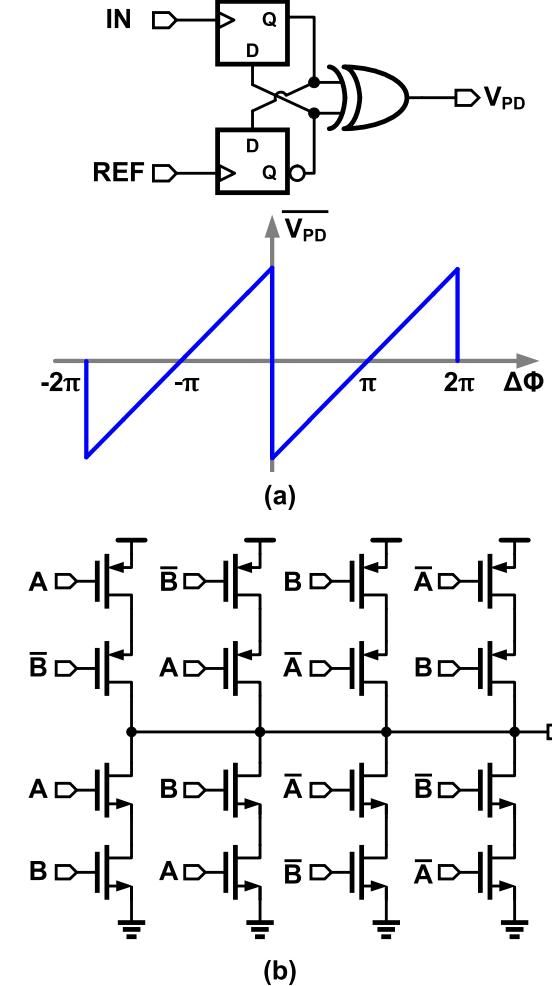


Fig. 16. (a) Two-state phase detector and its transfer characteristic. (b) Fully symmetric XOR gate.

and $\Phi_{INT,180}$, and generate pseudo-differential PWM signals, D_{OUT} , and \bar{D}_{OUT} . This pseudo-differential integrator offers two main advantages compared to its single-ended counterpart. First, using two matched CCROs allows to operate the integrator at any switching frequency independent of the reference frequency. Consequently, by choosing the free-running frequency of the two CCROs to be much higher than the reference frequency, the PWM control induced spurs can be pushed to a high frequency where they can be greatly suppressed by the bandpass transfer characteristic of the PLL. Second, ensuring good matching between the two CCROs reduces the static phase offset, which results in a smaller reference spur.

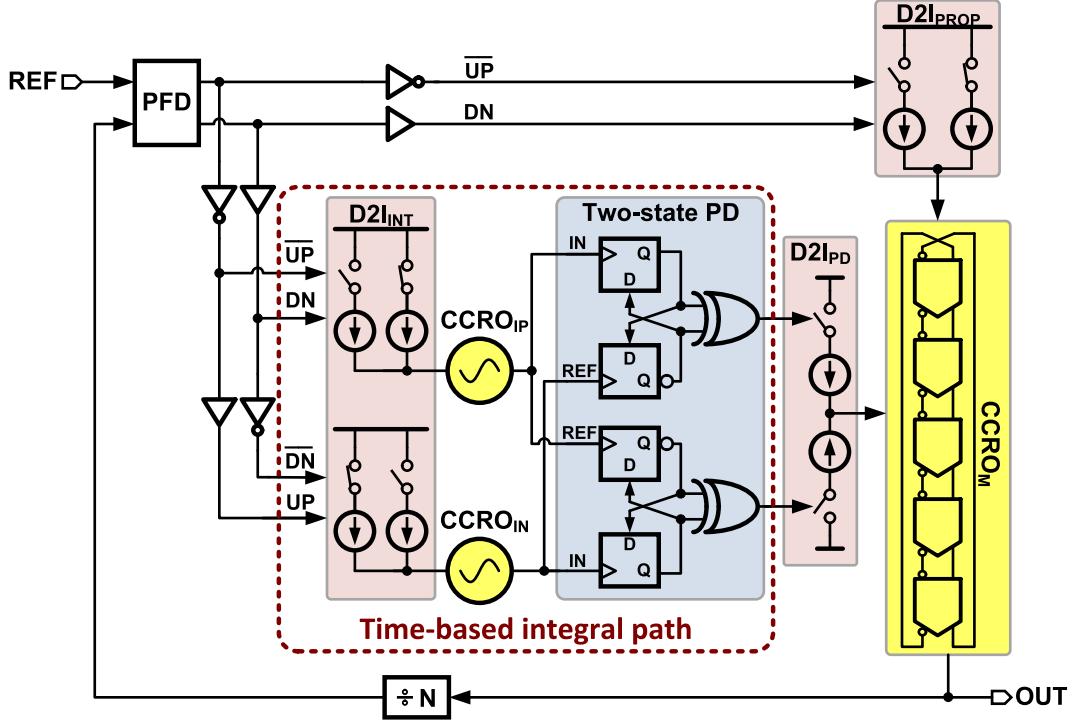


Fig. 17. Complete block diagram of proposed time-based PLL.

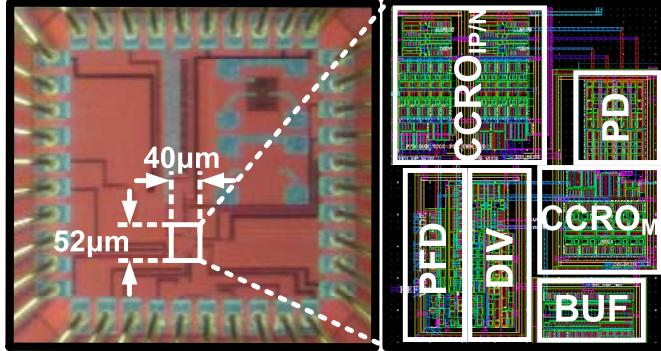


Fig. 18. Die micrograph.

However, effectiveness of the pseudo-differential architecture depends on the matching between CCRO free running frequencies. The difference between the free-running frequencies of the two CCROs, i.e., ($F_{CCRO_{IP}} \neq F_{CCRO_{IN}}$) appears as static phase offset, $\Phi_{OS,diff}$, as described earlier and is equal to

$$\Phi_{OS,diff} = \frac{F_{CCRO_{IP}} - F_{CCRO_{IN}}}{K_{D2I_{INT}} K_{CCRO_I} K_{PFD}}. \quad (24)$$

Note that (24) assumes that no mismatch between the oscillator gain $K_{CCRO_{IP}} = K_{CCRO_{IN}} = K_{CCRO_I}$. Reference spur caused by the pseudo-differential integrator can be calculated similar to the single-ended case and is estimated to be

$$\text{Spur magnitude[dB]} = 20 \log \left(\frac{F_{BW}}{F_{REF}} \cdot N \cdot \Phi_{OS,diff} \right) - 20 \log \left(\frac{F_{REF}}{F_{pm}} \right) \quad (25)$$

where F_{pm} denotes the parasitic pole of $CCRO_M$. Spur magnitude calculated based on (25) is plotted in Fig. 13 assuming $CCRO_I$ free-running frequency of 1 GHz and $K_{CCRO_I} =$

3 MHz/μA. Spur magnitude obtained from behavioral simulations of the PLL is also in Fig. 13. Compared with the simulation, calculation based on (25) indicates that narrowband approximation well captures the spur performance degradation caused by $CCRO_I$ mismatch. Nevertheless, the analysis/simulations indicate that a spur magnitude of -45 dB can be achieved if the mismatch is kept within 1000 ppm.

V. BUILDING BLOCKS

A. CCRO

The schematic of the current controlled ring oscillator is shown in Fig. 14. It is implemented using five current-starved pseudo-differential stages connected in a ring oscillator topology. The delay cell is composed of two CMOS inverters whose outputs are coupled in a feed-forward manner using transmission gates to ensure differential operation [12]. An output buffer (not shown in the figure) is used to convert CCRO output to rail-to-rail CMOS levels. A small inverter-based latch is added at the outputs of the buffer to minimize duty cycle error and achieve close to 50% duty cycle [7]. The pseudo-differential time-based integrator uses two such oscillators. Output oscillator $CCRO_M$ uses the same topology but with transistor dimensions adjusted to achieve the target output frequency range of 0.4 to 2.6 GHz under all process corners.

The tuning of oscillator $CCRO_M$ by the proportional and integral control paths is implemented as shown in Fig. 15. Fixed bias current I_B tunes the CCRO frequency coarsely and brings it close to the target frequency. Proportional ($I_{D2I,PROP}$) and integral ($I_{D2I,PD}$) currents are summed at the virtual supply node, V_S , of the CCRO. Proportional control current, $I_{D2I,PROP}$, takes three values, $2I_p$, I_p , and 0, corresponding to the 3 PFD states, UP, Reset, and DN, respectively. This mapping is performed by the two switches that are controlled

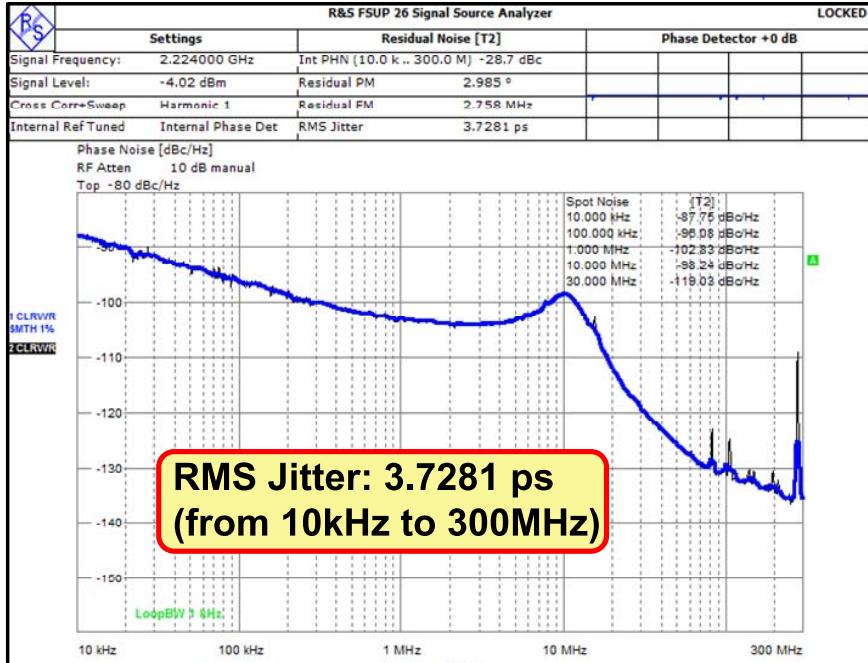


Fig. 19. Phase noise plot at 2.2 GHz output frequency.

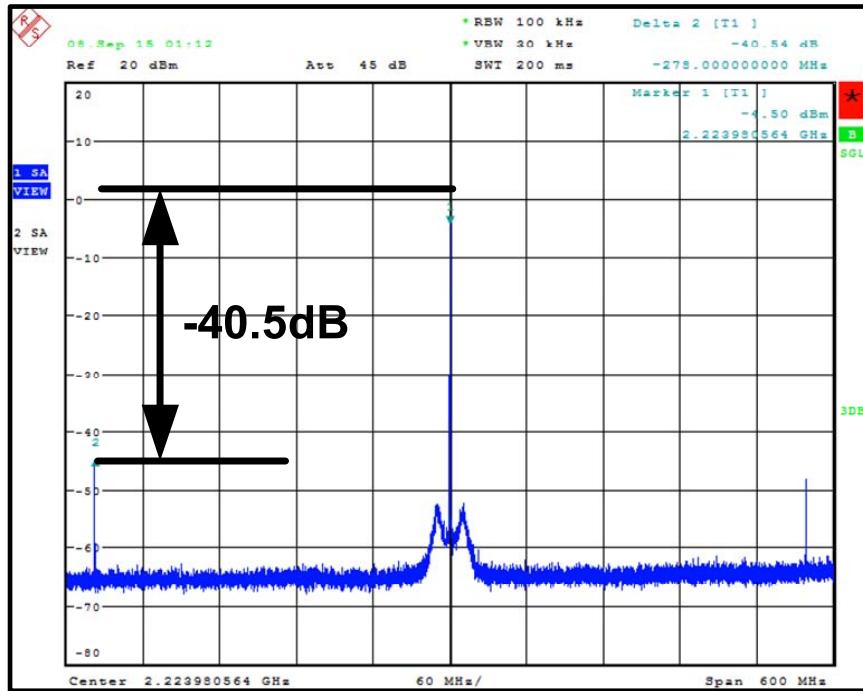


Fig. 20. Measured reference spur at 2.2 GHz output spectrum.

by \overline{UP} and DN [3]. Integral control is similarly implemented by mapping the two states of the PD to 2 current values I_{PD} and 0 by using one switch. Because CCRO integrator is implemented in a pseudo-differential manner, two switches controlled by the two PD outputs are necessary to generate the integral control current $I_{D2I,PD}$ as depicted in Fig. 15.

B. Phase Detector

The PD used in the CCRO integrator is implemented using the 2-state architecture shown in Fig. 16(a). The linear range and gain of the PD are equal to 2π rad and $1/2\pi$ V/rad,

respectively. Compared with a conventional 2-state PD [13], \overline{Q} output of FF2 is used instead of its Q output. This shifts the PD transfer characteristic by π radians resulting in zero average output when the input phase difference is equal to π radians as depicted in Fig. 16(a). Consequently, if the two oscillators in the time-based integrators are matched, the PLL locks with a phase difference of π radians at the PD input, which results in a PD output duty cycle of 50%. This maximizes the tuning range of the integral control path. XOR gate is implemented using a fully symmetric architecture shown in Fig. 16(b).

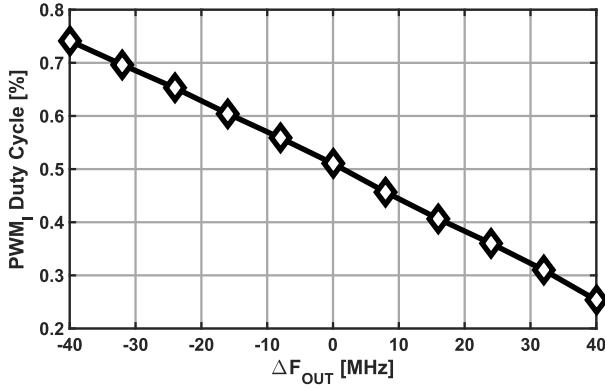


Fig. 21. PD output duty cycle versus oscillator free running frequency error.

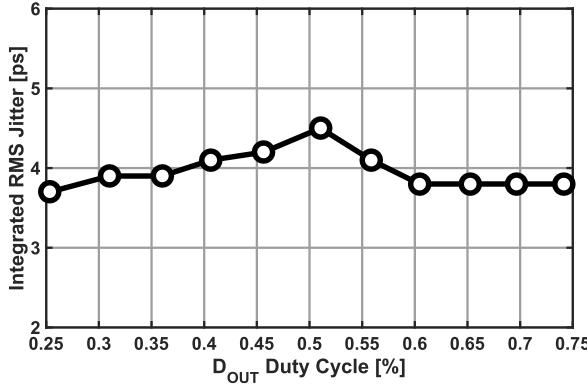


Fig. 22. Integrated rms jitter versus phase detector output duty cycle.

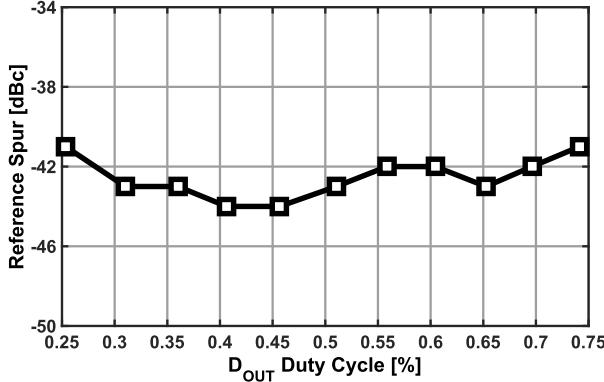


Fig. 23. Reference spur versus phase detector output duty cycle.

VI. MEASUREMENT RESULTS

The complete block diagram of the prototype PLL implemented in a 65 nm CMOS LP process is shown in Fig. 17. The die photograph is shown in Fig. 18. The PLL occupies an active area of 0.0021 mm² (52 μm \times 40 μm). Thanks to its highly digital implementation, the prototype PLL operates across a supply voltage range of 0.6 to 1.2 V, and achieves an operating range of 0.4 to 2.6 GHz while consuming a total power of 0.16 to 2.38 mW. The measured output phase noise plot is shown in Fig. 19. The phase noise at 1 MHz offset is -103 dBc/Hz and the root mean square (rms) jitter obtained by integrating the phase noise from 10 kHz to 300 MHz is 3.73 ps. The peaking observed in the plot is caused by phase

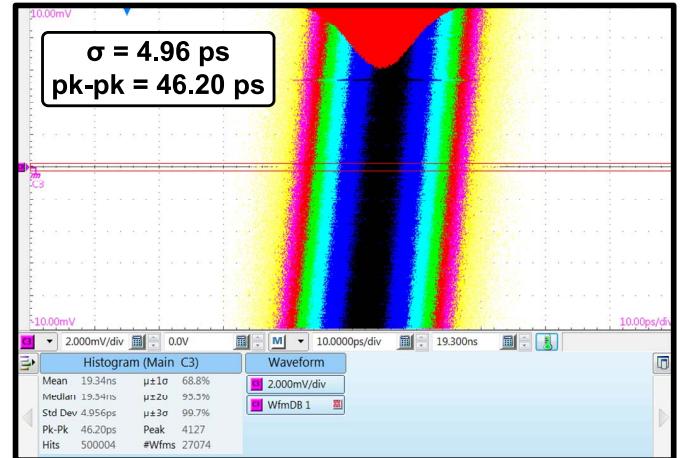
Fig. 24. Measured CCRO_{IP/N} time-domain waveforms at frequency offset of 24 MHz.

Fig. 25. Jitter histogram at 2.2 GHz output frequency.

margin degradation due to more than expected integral path gain resulting from underestimation of K_{CCRO_I} . The spectrum of 2.2 GHz PLL output generated from a 275 MHz reference clock is shown in Fig. 20. The measured reference spur magnitude is -40.5 dBc.

Fig. 21 plots the integral path phase detector output duty cycle as a function of CCRO_M frequency deviation from the target PLL output frequency. The output duty cycle changes from 25% to 75% as the deviation is varied by ± 40 MHz. Therefore, the tracking range of the integral path is about ± 40 MHz, which can be further extended by increasing D2IPD converter current at the expense of increased high frequency spur at the PWM frequency and phase noise contribution from CCRO_I. Note that reference spur stays unaltered if the ratio of proportional path to integral path gain is maintained sufficiently high (see Section III). Thus, in a practical realization, an alternative to increasing the tracking range is to add a double integral path as outlined in [3]. The integrated jitter and reference spur of the PLL output are measured across the tracking range, and the results are shown in Figs. 22 and 23, respectively. No significant variation of integrated jitter is observed and reference spur

TABLE I
PERFORMANCE COMPARISON OF PROPOSED TIME-BASED PLLS WITH STATE-OF-THE-ART DESIGNS

	This Work				ISSCC'12 [14]	ISSCC'14 [4]	ISSCC'14 [15]	ISSCC'15 [16]	ISSCC'16 [17]
Technology	65 nm				22 nm	40 nm	22 nm	14 nm	14 nm
Area [mm ²]	0.0021				0.017	0.013	0.012	0.009	0.021
Normalized Area ¹	1				70.67	16.35	60.36	92.35	215.56
Architecture	Time-based PLL				BB-DPLL	BB-DPLL	BB-DPLL	BB-DPLL	CP-APLL
Supply [V]	1.2	1.0	0.8	0.6	0.5–1.0	1.1	0.9	0.8	0.95
Output Freq. [GHz]	2.6	2.2	1.0	0.4	0.3–3.2	2.418	0.025–1.6	0.032–2.0	2.4
Ref. Freq. [MHz]	325	275	130	50	40	26	26	50	19.2
RMS Jitter [ps]	3.71	3.73	14.4	33.5	3.1	3.29	28	18.8	2.99
Power [mW]	2.38	1.82	0.64	0.16	3.4	6.4	3.1	2.06	1.79
Power Eff. [mW/GHz]	0.92	0.83	0.64	0.4	1.06	2.65	1.94	1.03	0.75
FoM [dB] ²	-224.8	-226.0	-218.8	-217.5	-224.8	-221.6	-206.1	-211.4	-227.9
FoM _r [dB] ³	-224.1	-226.0	-222.1	-224.9	-233.2	-231.8	-216.3	-218.8	-239.5

$$^1 \text{Normalized Area} = \left[\frac{\text{Area}}{0.0021 \text{ mm}^2} \cdot \left(\frac{\lambda}{65 \text{ nm}} \right)^2 \right]$$

$$^2 \text{FoM} = 10 \log \left[\left(\frac{\sigma_{\text{rms}}}{1 \text{ sec}} \right)^2 \cdot \left(\frac{\text{Power}}{1 \text{ mW}} \right) \right]$$

$$^3 \text{Normalized to } F_{\text{REF}} = 275 \text{ MHz } \text{FoM}_r = 10 \log \left[\left(\frac{\sigma_{\text{rms}}}{1 \text{ sec}} \right)^2 \cdot \left(\frac{\text{Power}}{1 \text{ mW}} \right) \cdot \left(\frac{F_{\text{REF}}}{275 \text{ MHz}} \right) \right]$$

is below -40 dBc across the whole range. At a frequency offset of 24 MHz, the integral path oscillator outputs shown in Fig. 24 demonstrate proper operation of the proposed time-based integral control. The measured long-term rms and peak-to-peak jitter at 2.2 GHz output frequency are equal to 4.9 and 46 ps, respectively (see Fig. 25). Note that jitter performance degrades when using a lower reference frequency because of reduced loop bandwidth. Under this condition, jitter can be reduced only by burning more power in the oscillators.

A comparison of prototype PLL performance with the state-of-the-art is shown in Table I. With integral path implemented using time-based integrator, the proposed PLL achieves smallest area among all of the reported PLLs. Use of highly digital circuits such as inverters to implement the integral path allows aggressive supply voltage scaling. While the proposed architecture achieves a large reduction in area, excess flicker noise in deeply scaled technologies (<28 nm) may warrant increasing the oscillator size, thus reducing the area benefit. Such a tradeoff exists in conventional digital PLLs as well because of the increased size of the digital-to-analog converter used to control the oscillator.

VII. CONCLUSION

A time-based integrator-based PLL architecture that achieves low active area and excellent power efficiency is presented. Time-based integral path greatly alleviates the area

penalty seen in conventional PLL architectures, and provides one alternative implementation of type-II PLL featuring good scalability with process and no quantization error in the system. Pseudo-differential architecture of time-based integrator has been proposed to overcome the drawbacks of reference spur degradation when directly applying PWM control to the oscillator. The proposed architecture helps decouple the oscillation frequency choice of integral path oscillator from PLL reference, and better leverage the loop response to achieve spur suppression. Prototype time-based PLL operates over a wide range of supply (0.6 to 1.2 V) with output frequencies ranging from 0.4 to 2.6 GHz and occupies an active area of only 0.0021 mm². At 2.2 GHz, the time-based PLL consumes only 1.82 mW power from a 1 V supply and achieves 3.73 ps_{rms} integrated jitter. The performance of the proposed time-based PLL is compared with state-of-the-art PLLs in Table I.

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