A Fully Integrated Digital Low-Dropout Regulator Based on Event-Driven Explicit Time-Coding Architecture

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***Abstract*— This paper presents a fully integrated digital low-dropout (LDO) voltage regulator based on event-driven control architecture. The focus of the paper is to scale the off-chip output capacitor of an LDO conventionally used to compensate fast load current change. To shrink the output capacitor size, it is paramount to shorten control latency. This can be done by employing a high-speed error amplifier in analog LDO designs and by using fast clock in digital synchronous LDO designs. However, those approaches become less suitable for sub-1-V supply voltage due to the headroom problem of analog circuits and/or increase power dissipation due to the high-frequency clock. In this paper, we tackle the tradeoff between power consumption and control latency by introducing an event-driven approach. Our event-driven approach enables to perform regulation tasks only when the output voltage deviates significantly from a set point, simultaneously achieving short latency and low-power dissipation. We prototyped an event-driven digital LDO that supports 400-μA load current at 0.5-V input and 0.45-V output voltage. The measurements show 40-mV droop voltage and 96.3% peak current efficiency with an on-chip integrated 0.4-nF output capacitor.**

***Index Terms*— Capacitor less, event driven, low dropout (LDO), near-threshold voltage, power management, system-on-chip, voltage regulator.**

I. Introduction

MODERN system-on-chip designs employ a number of power domains to provide optimal voltages for analog, digital, and mixed-signal sub-systems. As the number of power domains increases, area- and power-efficient voltage regulators are highly desirable. Thanks to its high power density, a low-dropout regulator (LDO) is one of the widely used topologies. However, LDO often requires an output capacitor (C_{OUT}) to handle fast load current (I_{LOAD}) change. This C_{OUT} is often too large and thus placed off-chip. The use of off-chip passives is indeed highly undesirable since it increases chip pin count and consumes printed circuit board area. Therefore, it is paramount to scale C_{OUT} to the on-chip integrable level so as to create many voltage domains at low overhead.

However, C_{OUT} scaling is a non-trivial task as it is related to control loop latency of an LDO. In analog LDO designs [1]–[9], we can reduce the control loop latency by using a high-speed error amplifier. However, such amplifiersgenerally consume a large amount of power, and further-

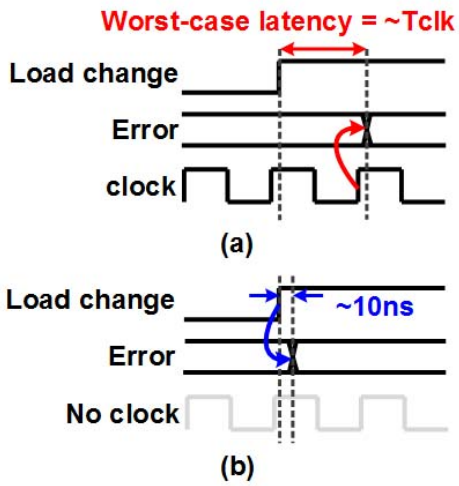

Fig. 1. Latency of (a) time-driven and (b) event-driven control systems.

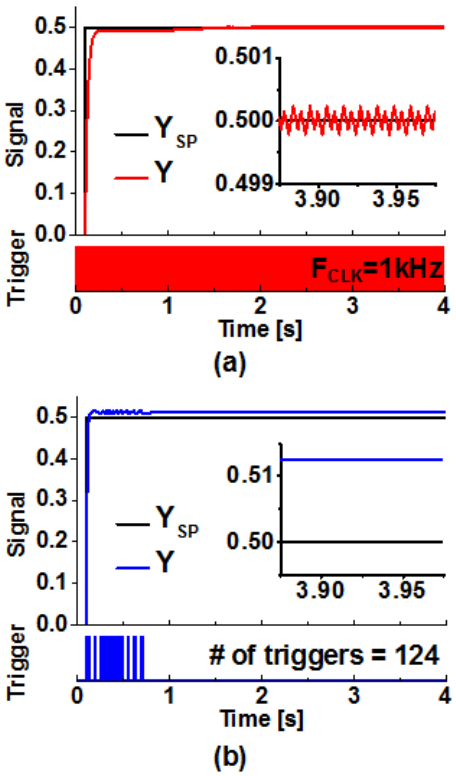

Fig. 2. Transient and steady-state behaviors of (a) time-driven and (b) event-driven control systems.

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more become less effective at supply voltage (V_{DD}) less than 1 V due to the limited headroom problem.

On the other hand, digital synchronous LDO designs [10]–[12] have recently gained a significant amount of attention for the ability to take sub-1-V input voltage (V_{IN}). In the digital synchronous LDO design, we can reduce the control loop latency by using fast clock. However, the use of fast clock inevitably results in high-power dissipation. This approach is particularly worse in the steady state, i.e., its output voltage is already regulated to a set-point voltage (V_{SP}), as it unnecessarily wastes energy due to continuous clock switching.

To avoid the limitations of synchronous control systems, recent regulators and dc–dc converters have adapted non-synchronous control systems. The digital LDO designs in [13]–[16] employed bidirectional asynchronous wave pipeline, updating controller output regardless of clock speed. In [17], the concept of phase-locked loop was applied to digital LDO design to provide regulation across a wide range of load current. The LDO in [18] made use of a continuous-time (CT) current-mirror flash analog-to-digital converter (ADC) together with the synchronous digital controller. Zhao and Prodic [19] have introduced CT digital signal processing (CT-DSP) in an inductive dc–dc converter.

In this paper, we also aim to break the tradeoff between control latency (proportional to C_{OUT} size) and power consumption at low supply voltage in digital LDO designs. Inspired by the event-driven DSP operation from [20], where the concepts of CT ADC and CT-DSPs have been reviewed, we introduced a novel event-driven architecture based on the explicit time-coding architecture [21]. Our event-driven approach allows a controller to update its output only when the LDO output deviates considerably from V_{SP}, i.e., at an event. This architecture can achieve very short latency without high-frequency clock. As shown in Fig. 1, synchronous (time-driven) systems perform a control operation at every rising clock edge. Thus, if LDO output deviates just after a clock edge, the systems must wait for the next clock edge to start regulation. Therefore, the worst case latency is the same as a single-clock period. Unlike time-driven systems, event-driven systems can immediately respond to a new event, significantly improving transient performance.

In addition, the event-driven approach can eliminate unnecessary operations, i.e., updating the output of the controller in the steady state. Once LDO output is settled to a set point, i.e., in the steady state, our event-driven approach observes no new event and thus stops updating controller output. Fig. 2 shows the exemplary step responses of time-driven and event-driven systems. Time-driven systems continue to update its output even after the output is settled to a set point. This not only consumes power but also causes ripples on the output. Event-driven systems, however, stop updating its output after the output is settled to a set point and consume only quiescent power (i.e., digital circuit leakage and bias current of comparators).

In this paper, we designed an LDO based on the event-driven approach, specifically explicit-time coding architecture. To handle the non-uniform sampling distance of event-driven

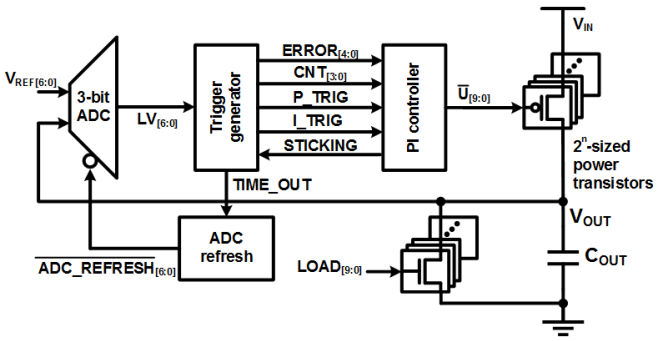

Fig. 3. LDO architecture with the proposed event-driven PI control systems.

systems, our proposed explicit-time coding architecture measures a time interval between two events and codes it into a digital value. Then, both time and magnitude values are used for computing control laws. Our LDO consists of a 3-b level crossing ADC, a trigger generator, an event-driven controller, a set of power transistors, and a fully integrated 0.4-nF output capacitor. The event-driven controller was also designed to handle dynamics unique to only event-driven systems.

The LDO was prototyped in a 65-nm CMOS. The measurement shows that the LDO can support 400-μA load current at 0.5-V input and 0.45-V output voltage. The LDO can also achieve less than 40 mV of droop voltage at $\pm$400-μA load current change over 0.1-ns edge time (T_{EDGE}). It consumes 14.8-μA quiescent current, marking 96.3% peak current efficiency. In the figure-of-the-merit (FOM) for the tradeoff between output capacitor size and power dissipation (FOM), our proposed design advances prior time-driven digital LDOs [10], [11] by 2.7 to 108$\times$.

The remainder of the paper is organized as follows. The architecture and sub-components of the proposed LDO are described in Section II. Then, we explain dynamics of event-driven systems in Section III and analyze the stability of the proposed LDO in Section IV. Section V shows the measurement results of the proposed LDO, and then we conclude the paper in Section VI.

II. Proposed Event-Driven LDO Design

A. Overall Architecture

The architecture of the proposed LDO is shown in Fig. 3. It consists of a CT ADC with refresh circuits, a trigger generator, a proportional–integral (PI) controller, and power transistors. The ADC captures the output voltage (V_{OUT}) when it crosses one of the seven reference voltage levels (V_{REF}[6:0]), then generates LV signal. Upon detecting LV signal change, the trigger generator produces triggers for the following PI controller. It also codes the time interval between two events into a digital value using a free-running oscillator (FRO) and sends it to the PI controller. Then, the PI controller computes P and I part results and produces 10-b output. This output turns on and off power transistors so that they can supply the right amount of current to a load.

B. Continuous-Time ADC

Fig. 4 shows the schematics of our CT FLASH ADC. It consists of seven inverter-based comparators [22]. Each

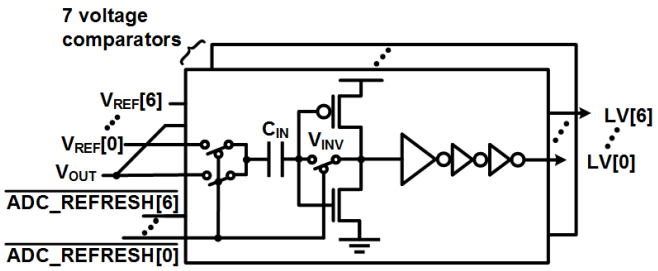

Fig. 4. CT flash ADC based on seven inverter-based comparators.

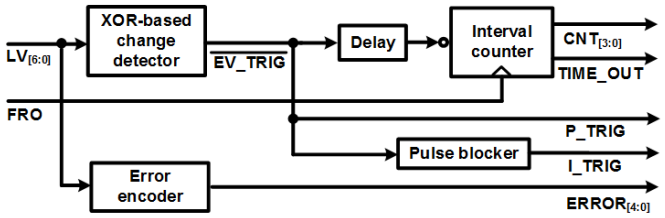

Fig. 5. Trigger generator microarchitecture.

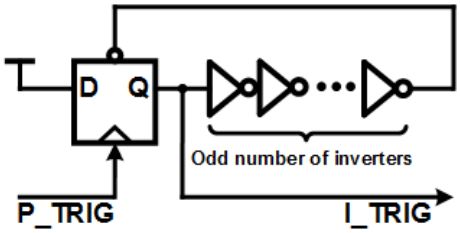

Fig. 6. Implementation of pulse blocker for I_TRIG.

comparator has two inputs and one output. The two inputs take one of the reference voltages ($V_{\mathrm{REF}}[N]$) and the output voltage of LDO (V_{OUT}). The output of each comparator produces LV[N|. The seven reference voltages are equally spaced by the voltage resolution (V_{RES}), typically 10 mV in this paper. Whenever V_{OUT} crosses one of the reference voltages, the ADC updates its 7-b thermometer-coded output.

The ADC operates via two phases: 1) refresh and 2) conversion, coordinated by ADC_REFRESH signal to implement the correlated double sampling method [23]. In the refresh phase, the comparator performs the double sampling operation to compensate process variation and ensuring high gain. Specifically, the input and output of the first inverter in a comparator are shorted and this makes the input and output to be at the mid-point of voltage transfer curve (VTC, $\sim 1/2 \cdot V_{\mathrm{DD}}$). The input capacitor of a comparator (C_{IN}) retains the voltage difference between this mid-point of VTC and the reference voltage. The voltage difference represents the input offset, which in the conversion phase will be automatically subtracted from the input. Note that, the C_{IN} will lose some of the voltage difference via gate leakage. Therefore, it is designed to periodically perform the refresh phase. Also, we interleave the refresh phases of the seven comparators over time so that while one of them is in the refresh phase all the other six are still in the conversion phase.

Note that a comparator in a refresh phase can produce incorrect output. Thus, the refresh-incurred worst case error can happen when a comparator whose reference voltage is the farthest from the set point is being refreshed. To avoid this problem, we design the error encoder to ignore isolated 1 or 0 and to find the error value based on more than two consecutive 0's and 1's. We also design the comparator in a refresh phase produce a value so as to make the error larger than the actual error. With these schemes, the controller receives mostly correct and conservative error values to regulate V_{OUT} even in the refresh phase.

In the conversion phase, the input and output of the first inverter of each comparator are disconnected, making it as an amplifier. Then, we connect the input of every comparator to V_{OUT}, the output voltage of LDO, through C_{IN}. Now if V_{OUT} becomes larger than the $V_{\mathrm{REF}}[N]$, the Nth comparator amplifies the difference (V_{OUT}–$V_{\mathrm{REF}}[N]$) to the logic high level through its four inverters. Otherwise, the comparators produce the logic low level.

C. Trigger Generator

Fig. 5 shows the schematics of trigger generator. It takes the ADC output and produces five digital signals for the following event-driven PI controller.

By comparing the ADC outputs via an XOR-based change detector, the trigger generator produces a pulse, called P_TRIG. The rising edge of P_TRIG has the P part of the PI controller to start to compute. Similarly, it produces a pulse called I_TRIG. As the name suggests, it is for the I part of the controller. I_TRIG generally follows P_TRIG but if several consecutive events happen in a short period of time, I_TRIG produces only one pulse. This design is for accommodating the longer circuit delay of the I part computation than the P part as the I part involves complex computation such as multiplication. The minimum time interval of two consecutive I_TRIG pulses is, therefore, set to the critical path delay of the I part computation. Fig. 6 shows the implementation of the pulse blocker to generate I_TRIG. It asserts I_TRIG at the rising edge of P_TRIG, then it asynchronously resets through the self-resetting loop consisting of the odd number of inverters. The reset is then released again through the loop. The delay of the inverters is matched to half of the I part computation delay so as to produce only one I_TRIG pulse at the first P_TRIG rising edge even if several other consecutive P_TRIGs arrive in a short amount of time.

The trigger generator also produces 4-b CNT signal by measuring the time interval between two successive events using the interval counter. The CNT signal is synchronized at the rising edge of I_TRIG as it is used for the I-part computation in the controller. To count a new time interval, the interval counter is reset by P_TRIG so I part changes its output conservatively with smaller CNT value. Similarly, the trigger generator produces 1-b TIME_OUT for handling the sticking problem (see Section III-A for more details).

Finally, the trigger generator produces 5-b ERROR signal by translating the thermometer-code LV into binary values using the error encoder. The error encoder is designed to be

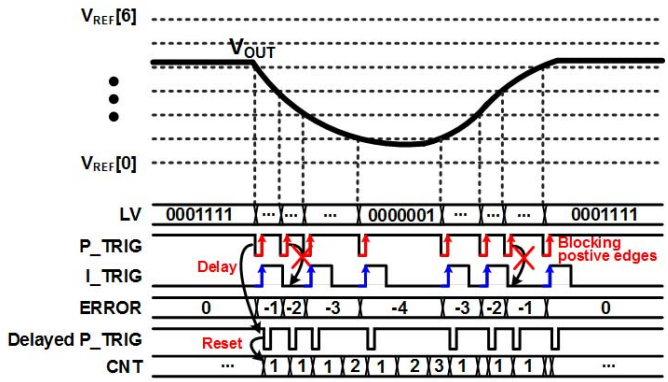

Fig. 7. Operational waveforms of the trigger generator.

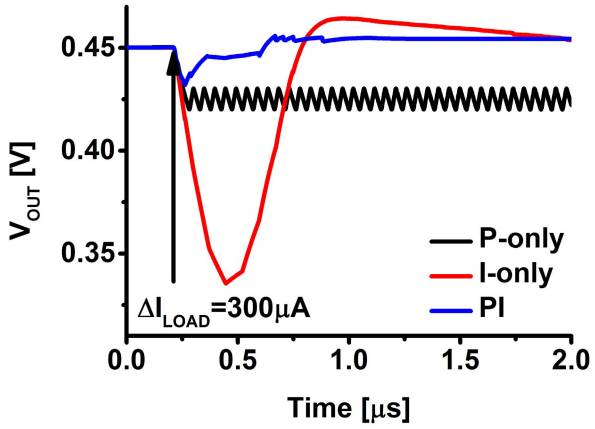

Fig. 8. Transient responses of (a) P, (b) I, and (c) PI controller for the same load current change.

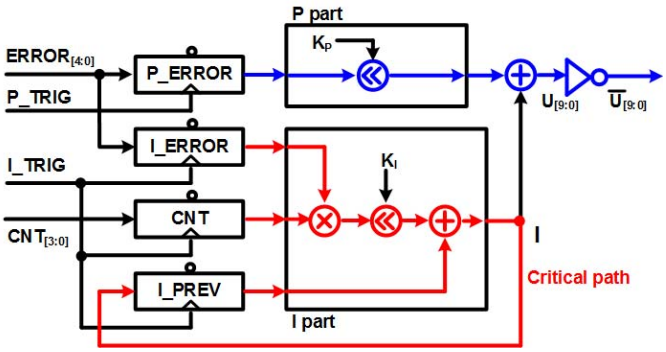

Fig. 9. Event-driven PI controller. The critical delay path is highlighted in red.

configurable to support more than the standard thermometer to binary translation. For example, we can set the ERROR values growing super-linearly with the LV values. Such non-uniform translation can improve transient response to large load current change (see Section V-B for details).

Fig. 7 shows the timing diagram of the trigger generator. As the LDO output voltage (V_{OUT}) crosses one of the reference voltages ($V_{\mathrm{REF}}[N]$), the ADC produces a new LV value, which generates P_TRIG. It also produces I_TRIG based on P_TRIG while ignoring P_TRIG pulses that are too close to the previous pulse. Also, the new LV value becomes the ERROR in the binary format via the error encoder. The interval counter produces the CNT value at the I_TRIG rising edge, and then reset to zero at the delayed P_TRIG signal.

D. Event-Driven PI Controller

In the controller design, we mainly consider the PID control law and its variants for its high performance and simple implementation. The PID control law consists of proportional (P), integration (I), and differential (D) parts. Each part has its own gain, K_P, K_I, and K_D, which will be multiplied for output generation. We can use one of the parts, combine two of them or all. However, we decide not to use the D control since the division operation can significantly increase complexity. Therefore, we mainly compare three control laws, namely, P, I, and PI, in our controller design.

P-only control is similar to what the classical analog LDO is based on. The output of the controller is proportional to the error. The advantage of P controller is its fast transient response (Fig. 8). In the digital LDO design, however, insufficient gain can cause a considerable amount of steady-state error. Insufficient digital-to-analog converter (DAC) resolution can also cause limit-cycle oscillation in the steady state.

I-only control can reduce the steady-state error down to less than one LSB of the ADC resolution. However, its regulation speed is slow, particularly much slower than P-only control in event-driven control systems. This is because, in event-driven control systems, the rate of change of the plant state (V_{OUT} in our LDO design) determines the rate of new event generation, and then the rate of new event generation determines control speed. This self-loop in the event-driven control system process makes I-only control slower than P-only control.

Therefore, we design the event-driven PI controller since it can take advantages of both P and I controls, namely fast regulation and less than one LSB steady-state error (Fig. 8). Fig. 9 shows the schematics of the controller. It takes the outputs of the trigger generator, computes the P and I part results, sums them, and finally produces 10-b unsigned binary output U for turning-on/off power transistors. The P computation requires to multiply ERROR and K_P, as shown below

$$P(k) = K_P \cdot e(k) \tag{1}$$

where P(k) is the output of P part at the kth event and e(k) is the ERROR value at the kth event. The I computation is the accumulation of multiplications of ERROR, CNT, and K_I, as defined below

$$I(k) = \sum_{i=0}^{k-1} K_I \cdot e(i) \cdot \mathrm{CNT}(i) \tag{2}$$

where $I(k)$ is the state of I-part (accumulation result), $e(i)$ is the error of ith event (samples), and CNT(i) is the ith time interval from the trigger generator. Fig. 10 graphically shows the P and I part computations. The P part output is a function of the error magnitude at the kth event. The I part output implements forward Euler method, i.e., it accumulates the area of the rectangle determined by CNT($k-1$) and $e(k-1)$ at the

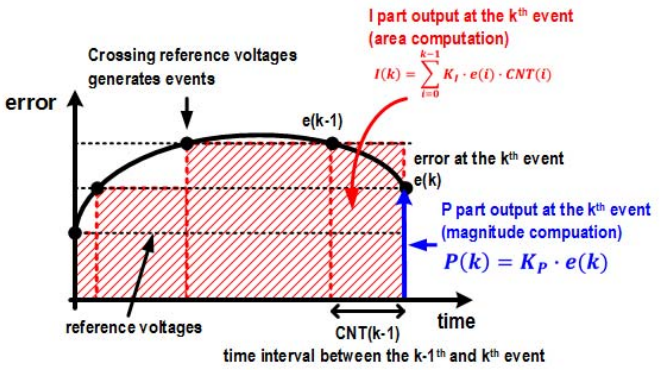

Fig. 10. Graphical representation of P and I part computation in the proposed explicit time-coding architecture.

kth event. We use the shifters to implement the multiplication of each gain (K_P, K_I) with $e(i)$ for short computation latency. We use a 9-b general-purpose multiplier for the multiplication of $e(i)$ with CNT(i). Last, the output of the controller, $U(k)$, at the kth event is determined by the sum of $P(k)$ and $I(k)$ as below

$$U(k) = P(k) + I(k). \tag{3}$$

III. Challenges of Event-Driven Systems

Event-driven control systems have several unique characteristics that time-driven or CT control systems do not have. This is because in the event-driven control, the regulation of output is initiated only by the change of output itself. This can cause several undesirable behaviors, as well, which we try to compensate in our proposed LDO design.

A. Sticking Problem

Sticking problem is a phenomenon that a plant state is stuck to a value that is not a set point. Fig. 11 shows exemplary waveforms of which our LDO experiences such sticking problem. During regulation, the output voltage (V_{OUT}) can change slowly between two reference voltages (e.g., $V_{\mathrm{REF}}[k]$ and $V_{\mathrm{REF}}[k+1]$) for some reason, and this can limit new trigger generation. Without triggers, the controller cannot update its output and thus plant states (V_{OUT}) cannot change further. The lack of change in V_{OUT} prevents new triggers from being generated. Eventually, this forces V_{OUT} to settle at an undesired level.

To resolve this sticking problem, we design our PI controller to generate a compulsive trigger if V_{OUT} is stuck at the non-zero error position for more than a predefined amount of time. Once generated, this compulsive trigger can update controller output, and it helps V_{OUT} to cross one of the reference voltages, generating new triggers and thus reactivating the normal regulation operation.

Fig. 12 shows our proposed PI controller with the aforementioned countermeasure for the sticking problem. Specifically, the sticking detector determines if the current error is zero or not. If not, the sticking detector enables the sticking

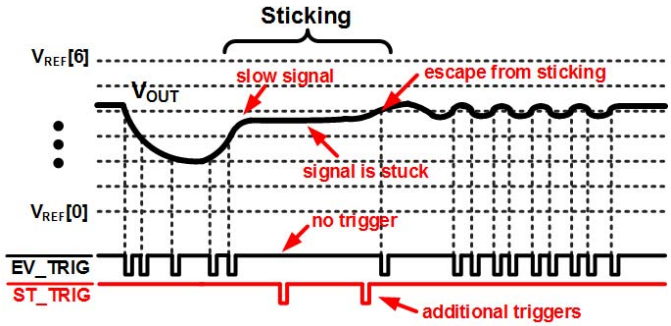

Fig. 11. Sticking problem and the proposed solution in the event-driven LDO.

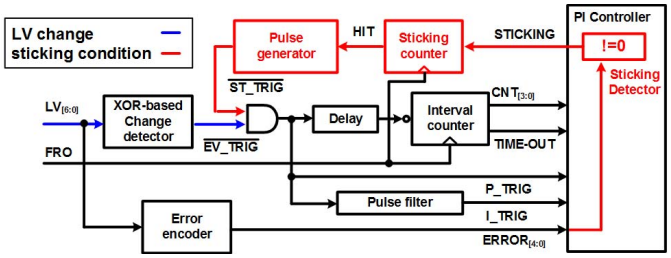

Fig. 12. Modified microarchitectures of the trigger generator and the PI controller for the sticking problem.

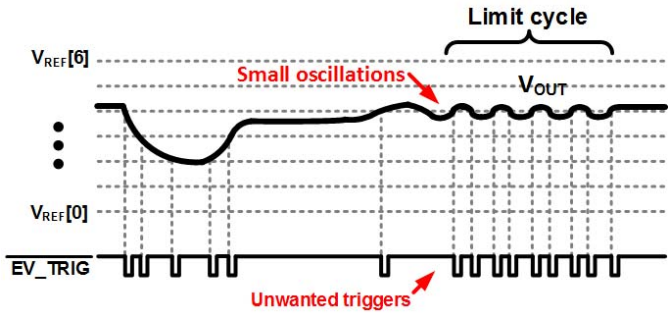

Fig. 13. Insufficient DAC resolution and too large K_I can cause limit cycle in the LDO.

counter (in the trigger generator), and if the sticking counter reaches a predefined threshold, it asserts HIT, which initiates a new trigger generation.

B. Limit Cycle

Limit cycle is a phenomenon that the state of a plant oscillates near a set point in the steady state. Fig. 13 shows the exemplary waveforms of limit cycle occurring in the proposed digital LDO. Although the amplitude of oscillation is not significant, it causes continuous event generation and thus overshadows one of the key benefits of event-driven control systems: no control operation in the steady state. This unnecessarily increases power dissipation.

One of the main causes of the limit cycle is insufficient resolution of DAC. In our proposed LDO system, the DAC resolution is determined by the sizes of power transistors and gains of P and I control law computation (i.e., K_P, K_I). To avoid limit cycle, therefore, we use fine-grained sizes

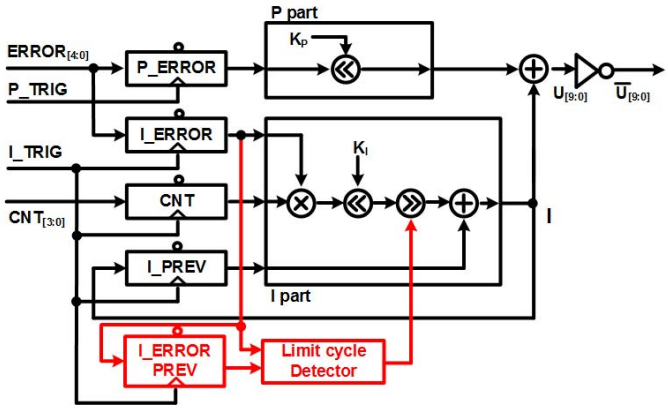

Fig. 14. Proposed PI controller with the adaptive K_I scheme for mitigating limit cycle.

of power transistors. Furthermore, as shown in Fig. 14, we employ an adaptive gain scheme for the I part computation. Specifically, the controller has two sets of registers to store two successive error values. Then, the limit cycle detector determines if one of the two successive errors is zero and the other is ± 1 LSB. If this condition is met, the controller reduces K_I to alleviate the limit cycle.

IV. Stability Analysis

Stability analysis is critical to any control systems. However, it is not straightforward to use some of the conventional analysis techniques to our LDO design since event-driven control systems have a sampling rate that is not constant. A large body of the works has analyzed the stability of non-uniform sampling systems [24]–[26]. In this paper, we devise a stability analysis framework by using the state space model that describes the transient behavior of the LDO system between two sampling moments. With this model, we analyze the stability of our LDO by considering all the possible sampling intervals.

In our LDO design, we model the plant by using supplying current of power transistors (I_{PWR}), load current (I_{LOAD}), and output capacitor (C_{OUT}). One of the states of the plant part is defined as V_{OUT} at the current sampling moment $[V_{\mathrm{OUT}}(k)]$ and that at the next sampling moment $[V_{\mathrm{OUT}}(k+1)]$, which is a function of C_{OUT}, the time interval between current and the next events (T_{EV}), and the difference between load current and supply current ($I_{\mathrm{PWR}}-I_{\mathrm{LOAD}}$). I_{PWR} can be further defined as the product of the controller output (U) and a unit current (I_U) of the power transistor array. $V_{\mathrm{OUT}}(k+1)$ can be derived as

$$V_{\mathrm{OUT}}(k+1) = V_{\mathrm{OUT}}(k) + \frac{(U(k)\cdot I_U - I_{\mathrm{LOAD}})}{C_{\mathrm{OUT}}}\cdot T_{\mathrm{EV}}(k). \tag{4}$$

To simplify the analysis, we normalize V_{OUT} to the ADC resolution (V_{RES}), as shown below

$$e(k) = \frac{V_{\mathrm{REF}} - V_{\mathrm{OUT}}(k)}{V_{\mathrm{RES}}}. \tag{5}$$

By combining (4) and (5), we can derive $e(k+1)$ as below

$$e(k+1) = e(k) - \frac{(U(k)\cdot I_U - I_{\mathrm{LOAD}})}{C_{\mathrm{OUT}}\cdot V_{\mathrm{RES}}}\cdot T_{\mathrm{EV}}(k). \tag{6}$$

The remaining part of the LDO, i.e., the controller, can be modeled based on (1)–(3). We reformulate (2) in a recursive form and also (3) as a function of $e(k)$ and $I(k)$. The output of I part, another state, at the $(k+1)$th sampling time then can be derived as

$$I(k+1) = I(k) + K_I\cdot e(k)\cdot \mathrm{CNT}(k). \tag{7}$$

And the output of the controller at the kth sampling moment can be found as

$$U(k) = K_P\cdot e(k) + I(k). \tag{8}$$

Using (8), we can reformulate (6) into

$$e(k+1) = \left(1-\frac{K_P\cdot T_{\mathrm{EV}}(k)\cdot I_U}{C_{\mathrm{OUT}}\cdot V_{\mathrm{RES}}}\right)e(k) - \frac{T_{\mathrm{EV}}(k)\cdot I_U}{C_{\mathrm{OUT}}\cdot V_{\mathrm{RES}}}I(k) + \frac{T_{\mathrm{EV}}(k)}{C_{\mathrm{OUT}}\cdot V_{\mathrm{RES}}}I_{\mathrm{LOAD}}. \tag{9}$$

Finally, we can model the LDO with two states at the kth event, namely, $e(k)$ and $I(k)$, based on (7) and (9). Those equations can be formulated into a matrix form as below

$$\begin{bmatrix} e(k+1) \\ I(k+1) \end{bmatrix} = \begin{bmatrix} 1-\dfrac{K_P\cdot T_{\mathrm{EV}}(k)\cdot I_U}{C_{\mathrm{OUT}}\cdot V_{RES}} & -\dfrac{T_{\mathrm{EV}}(k)\cdot I_U}{C_{\mathrm{OUT}}\cdot V_{\mathrm{RES}}} \\ K_I\dfrac{T_{\mathrm{EV}}(k)}{T_{\mathrm{FRO}}} & 1 \end{bmatrix} \times \begin{bmatrix} e(k) \\ I(k) \end{bmatrix} + \begin{bmatrix} \frac{T_{\mathrm{EV}}(k)}{C_{\mathrm{OUT}}\cdot V_{\mathrm{RES}}} \\ 0 \end{bmatrix} I_{\mathrm{LOAD}}. \tag{10}$$

The stability analysis of the state space model is done by determining the eigenvalues in its matrix equation, (10) in our case. Fig. 15 shows the eigenvalues of the proposed LDO system as a function of various design parameters. In our systems, T_{EV} is a variable and thus we plot eigenvalue pairs across T_{EV}s. A key factor to consider is that T_{EV} is the multiplication of CNT with T_{FRO} (discretized) and is bounded by the predefined threshold of the sticking counter. This allows us to consider only a limited number of T_{EV}s, and thus simplifies the stability analysis. If eigenvalues are inside a unit circle, the corresponding system is considered stable. As shown in (10), however, the amount of impact of different sampling time can significantly be varying according to the values of design parameters. Each parameter often makes a non-linear impact on a pair of eigenvalues. Thus, we inspect all the possible design parameters to ensure the stability of the LDO (Fig. 15).

It is shown that our choice of design parameters ($K_P = 64$, $K_I = 0.5$, $C_{\mathrm{OUT}} = 400$ pF, $T_{\mathrm{FRO}} = 5$ ns, $V_{\mathrm{RES}} = 10$ mV) makes the LDO system stable. Furthermore, it is worth noting that the stability analysis that we devised is the necessary condition for system's stability. In other words, even if the systems have eigenvalues outside of the unit circle for some sampling moments, we cannot rule out the possibility that the systems could be back to stable. This is because each eigenvalue represents only the behavior between two sampling moments. Even if systems cannot regulate its state across several sampling moments, e.g., due to large T_{EV} values, the systems could recover to a stable state with, e.g., several successive small T_{EV} values. Our proposed stability analysis, therefore, confirms the stability in the worst case.

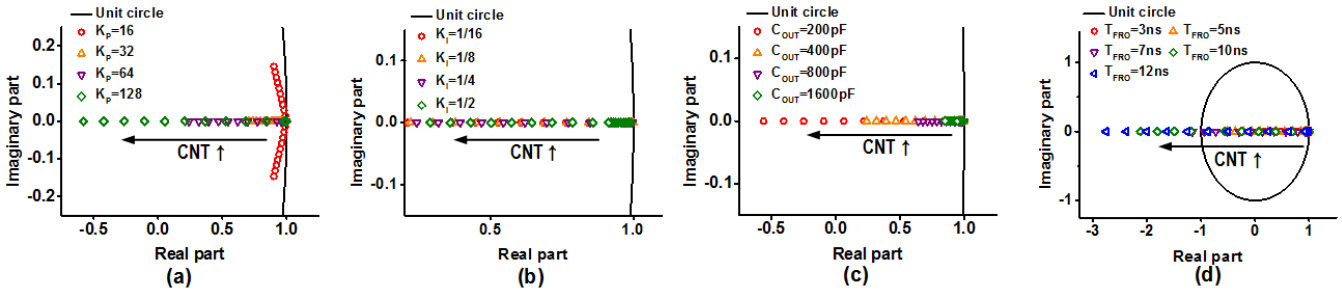

Fig. 15. Eigenvalues of the proposed LDO system across different (a) K_P, (b) K_I, (c) C_{OUT}, and (d) T_{FRO}.

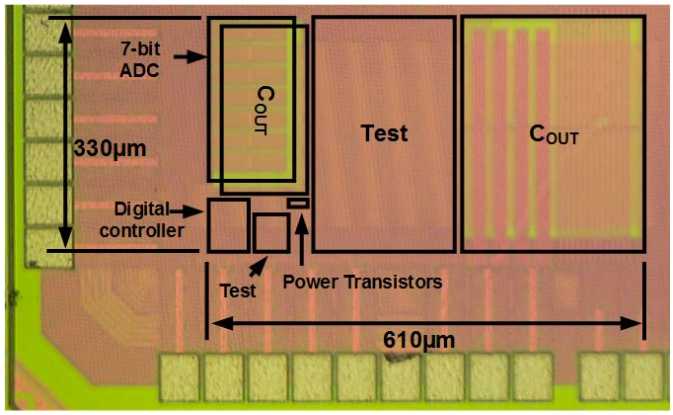

Fig. 16. Test chip die photograph. The ADC C_{IN} which takes the dominant area of the ADC is implemented with MIMCAP but the LDO C_{OUT} with MOSCAP. To save area, we place a part of the C_{OUT} under the ADC C_{IN}.

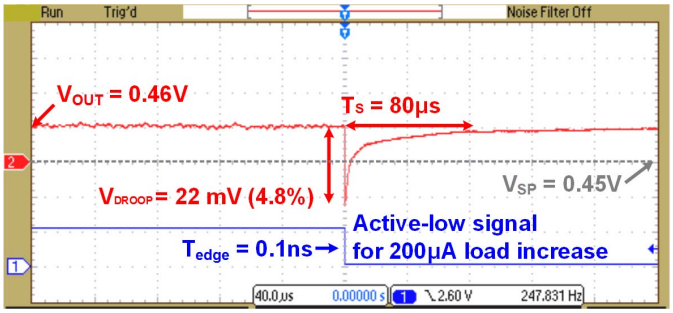

Fig. 17. Dynamic load regulation of the proposed LDO.

V. Chip Prototyping and Measurement

A. Test-Chip Organization

The test chips for the proposed event-driven LDO system have been prototyped in a 65-nm general-purpose CMOS process. Fig. 16 shows the micrograph of the test chip. The integrated output capacitor and the input capacitors of ADC are implemented with metal-oxide silicon capacitors (MOSCAP) and metal-insulator-metal capacitors (MIMCAP). The active area of LDO system without the output capacitor is 0.029 mm^2.

B. Measurement

We investigate the performance of our proposed LDO system across different environments. Fig. 17 shows the transient response to a sudden load current change (200 μA) at 0.1-ns edge time (T_{EDGE}) and the corresponding droop voltage (V_{DROOP}) and settling time (T_S). The ADC resolution (V_{RES}) is set to 10 mV.

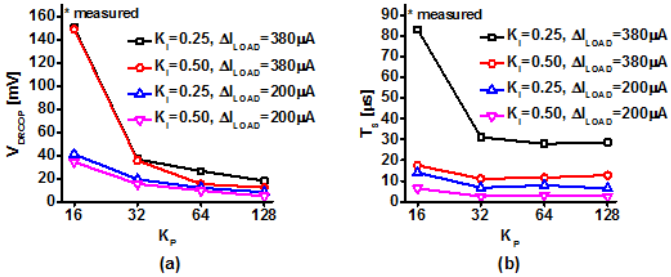

Fig. 18. Impact of K_P and K_I on (a) droop voltage and (b) settling time.

As shown in Fig. 18, we measure the impact of K_P and K_I on V_{DROOP} and T_S. Increasing K_P can significantly reduce V_{DROOP}. This is because large K_P helps I_{PWR} to quickly follow I_{LOAD} upon the first event, and thus prevents further V_{OUT} droop. After that, the I part removes the steady-state error over time.

On the other hand, K_I has a strong impact on T_S. As error becomes smaller during regulation, the I part gradually takes over the current produced by the P part. At the end of regulation, the P part does not contribute to I_{PWR}. Therefore, the I part needs to supply I_{PWR} upon all possible load current. Increasing K_I speeds up the operation of the I control by increasing the amount of I part output change at each event and thus reducing T_S. Note that the increasing K_P also helps to reduce T_S since it reduces V_{DROOP} and the I part needs to correct a less amount of V_{OUT} deviation.

We also investigate the impact of several other design parameters. First of all, we modulate the period of FROT_{FRO} and measure quiescent current (I_Q) and T_S [Fig. 19(a)]. Using small T_{FRO} increases the I part computation result, and this is equivalent to increasing K_I yet without causing limit cycle. However, small T_{FRO} increases dynamic power dissipation of the ring oscillator. In our design, we use 5-ns T_{FRO} as a sweet spot for this tradeoff.

We also investigate the impact of V_{RES}. V_{RES} has a strong impact on the number of events for the same amount of V_{OUT} change. Also, V_{RES} inherently involves the control loop gain since the ADC gain, defined as analog input voltage to digital output code ratio, is inversely proportional to V_{RES}. Therefore,

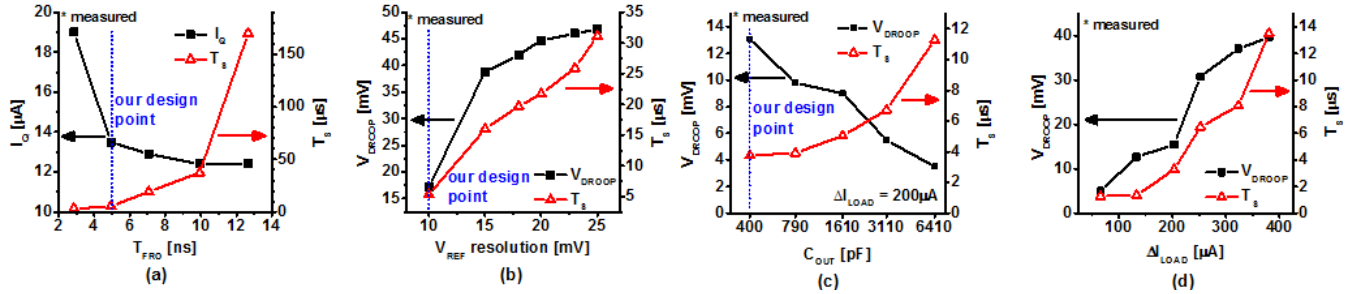

Fig. 19. LDO performance across different (a) FRO periods, (b) reference voltage resolutions, (c) output capacitor sizes, and (d) amount of load current change.

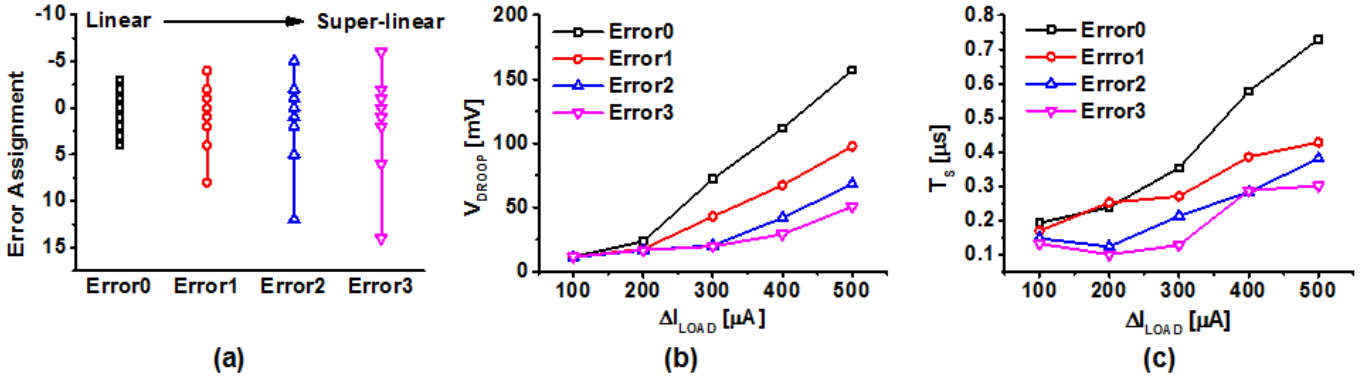

Fig. 20. (a) Four translation configuration of thermometer-coded LV to binary-coded ERROR and the impacts on (b) droop voltage and (c) settling time.

as shown in Fig. 19(b), small V_{RES} is beneficial to V_{DROOP} and T_S. However, implementing small V_{RES} requires more comparators in the FLASH ADC architecture for the same input range. In our design, we use 10-mV V_{REF} as a sweet spot for this tradeoff.

We also investigate the impact of the output capacitor size (C_{OUT}). The LDO transient performance is a function of control loop speed and the rate of V_{OUT} change. The rate of V_{OUT} change is determined by the load current change (ΔI_{LOAD}), and C_{OUT}. While increasing C_{OUT} improves V_{DROOP} for the same load current change [Fig. 19(c)], it is undesirable for on-chip integration. Increasing C_{OUT} also increases T_S since it takes a longer time to charge larger C_{OUT}. In this paper, we set C_{OUT} to 400 pF, the smallest value that has V_{DROOP} less than 10% of V_{OUT} at the ±400-μA I_{LOAD} change. Fig. 19(d) shows the performance across different load current changes. As expected, large I_{LOAD} change increases V_{DROOP}, and thus T_S. To support a larger I_{LOAD} change for the target ΔV_{OUT}, we need to either increase output capacitor size or speed up the control loop latency, which typically increases power consumption and thereby degrades current efficiency.

We also conduct an experiment of the adaptive gain scheme. As discussed in Section III-B, the error encoder in the proposed LDO is configurable on the translation of the thermometer-coded LV into the binary ERROR signal. Fig. 20(a) shows four translation configurations for the evenly assigned V_{REF}s (V_{RES} = 10 mV). The Error3 configuration, for example, has a non-uniform translation scheme where ERROR value increases super-linearly with LV ones. This configuration is equivalent to increasing K_P and K_I only for larger V_{OUT} error. For the precise V_{OUT} regulation, we still keep the linear translation for the error around a set point. As shown in Fig. 20(b) and (c), the adaptive gain scheme improves V_{DROOP} and T_S.

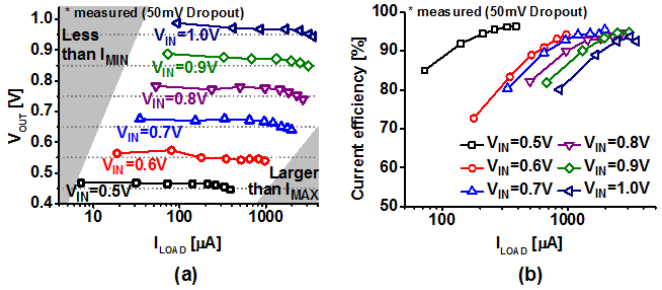

Fig. 21. (a) Supported range of load current and (b) current efficiency across input voltages.

C. LDO Operation Across Input Voltages

While we design our LDO mainly for 0.5-V input voltage (V_{IN}) with 50-mV dropout voltage, it functions across 0.5–1 V V_{IN} with the same dropout voltage. As shown in Fig. 21(a), it can support up to 400 μA at 0.5 V V_{IN} to 3.5 mA at 1 V V_{IN} (about 50× range for I_{LOAD}). The maximum load current is limited by the control loop latency at low V_{IN}s and by the test setup (the size of load transistor array in the test chips) at high V_{IN}s.

We also measure current efficiency across V_{IN}s. The peak current efficiency at 0.5 V is 96.3% [Fig. 21(b)]. The peak

TABLE I
COMPARISONS OF LDO DESIGNS

	[10]	[11]	[12]	[15]	[18]	This work
Technology	65nm	130nm	130nm	65nm	28nm	65nm
Control	Time-driven	Time-driven	Hybrid	Asynchronous	Hybrid	Event-driven
V_{IN} [V]	0.5	0.5~1.2	0.6, 1.1~1.2	0.6~1	1.1	0.5~1
V_{OUT} [V]	0.45	0.45~1.14	0.5~0.55, 0.8~1.1	0.55~0.95	0.9	0.45~0.95
I_{LOAD} [μA]	~200	100~4600	12000	~500000	200000	7.2~3511
I_Q [μA]	2.7	24~221	163.2	300	110	12.5~216
C_{OUT} [nF]	100	1	0.5	1.5	23.5	0.4
Peak current efficiency [%]	98.7	98.3	98.64	99.7	99.94	96.3
T_{EDGE} [ns]	N/A	N/A	2(2)	2(1)	4000(2)	0.1(1)
Max V_{DROOP} @ V_{IN}	40mV @ 0.5V	40mV @ 0.5V	240mV @ 1.2V	35mV @ 0.65V	120mV @ 1.1V	40mV @ 0.5V
ΔI_{LOAD} (I_{LOAD0}-I_{LOAD1})	0.2mA (0-0.2mA)	0.7mA (0.7-1.4mA)	10.3mA (0.03-10.3mA)	100mA (N/A)	180mA (20-200mA)	0.4mA (0-0.4mA)
Active area [mm^2]	0.042	0.114	0.0818	0.158	0.021	0.029
Power transistor area [mm^2]	0.007(2)	N/A	N/A	0.065(2)	0.004(2)	0.00024
FOM [pF]	120(3)	3.05(3)	1.73(4)	0.26(5)	1.72(6)	1.11(3)

Note: N/A stands for "data not available"; (1)Simulated data.; (2)Estimated data from figures; FOM is calculated based on (3)0.5V V_{IN}, 0.45V V_{OUT}; (4)1.2V V_{IN}, 1.1V V_{OUT}, (5)0.6V V_{IN}; 0.55V V_{OUT}; (6)1.1V V_{IN}, 0.9V V_{OUT}

current efficiency is more than 90% across all the V_{IN}s. The peak current efficiency tends to decrease as V_{IN} increases since the CT ADC operates in the super-threshold region and thus consume more crowbar (short-circuit) current.

We evaluate the power supply rejection (PSR) of our LDO. For dc-like V_{IN} change from 0.48 to 0.6 V, the LDO can regulate V_{OUT} error less than one LSB, which is equivalent to 28 dB. For V_{IN} change of 10 kHz and 10 MHz, the LDO exhibits the PSR of 20 and 5.2 dB, respectively. The 50-mV dropout voltage has the power transistors of digital LDOs operate in the deep triode region, which can facilitate to pass V_{IN} change onto V_{OUT}. Our LDO has tens of nanoseconds of control loop latency, and thus can well regulate slow V_{IN} change. But when the time constant of V_{IN} change is comparable to the control loop latency it suffers from low PSR. To improve it, the active and passive techniques (see [27]) are desirable.

D. Comparisons

Finally, we compare our proposed LDO with the state-of-the-art designs based on time-driven control systems that support 0.5-V V_{IN}. To compare the tradeoff between passive size and quiescent power dissipation, we define the first FOM

$$\text{FOM[pF]} = I_Q \cdot \frac{V_{\text{DROOP,MAX}}}{I_{\text{LOAD}} \cdot V_{\text{OUT}}} \cdot C_{\text{OUT}}. \tag{11}$$

The first term represents quiescent power dissipation, the second term represents the load regulation performance normalized to I_{LOAD} and V_{OUT}, and the last term is passive size. As shown in Table I, our proposed LDO achieves 2.7–108× improvement over two previous works [10], [11] which can support 0.5-V V_{IN} operation in this FOM. Note that FOM is a function of V_{IN} and thus it is non-trivial to compare designs of different V_{IN}s. Therefore, in this paper, we compare our design to the design having the same V_{IN} of 0.5 V.

VI. CONCLUSION

This paper presents the fully integrated digital LDO designed based on novel event-driven explicit time-coding architecture. The proposed event-driven architecture enables the significant reduction in control latency while minimizing the power dissipation during the steady state. The measurement based on the prototype chips in 65 nm shows that our proposed LDO achieves 40-mV V_{DROOP} for 0.4-mA ΔI_{LOAD} while having only 0.4-nF C_{OUT}. The peak current efficiency is 96.3% at 0.5-V V_{IN} and 0.45-V V_{SP}.

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REFERENCES

[1] P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan, and S. Borkar, "Area-efficient linear regulator with ultra-fast load regulation," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 933–940, Apr. 2005.

[2] J. Guo and K. N. Leung, "A 6-μW chip-area-efficient output-capacitorless LDO in 90-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1896–1905, Sep. 2010.

[3] J. F. Bulzacchelli *et al.*, "Dual-loop system of distributed microregulators with high DC accuracy, load response time below 500 ps, and 85-mV dropout voltage," *IEEE J. Solid-State Circuits*, vol. 47, no. 4, pp. 863–874, Apr. 2012.

[4] K. N. Leung and P. K. T. Mok, "A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1691–1702, Oct. 2003.

[5] S. K. Lau, P. K. T. Mok, and K. N. Leung, "A low-dropout regulator for SoC with Q-reduction," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 658–664, Mar. 2007.

[6] M. Al-Shyoukh, H. Lee, and R. Perez, "A transient-enhanced low-quiescent current low-dropout regulator with buffer impedance attenuation," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1732–1742, Aug. 2007.
[7] Y. Lu, W.-H. Ki, and C. P. Yue, "A 0.65 ns-response-time 3.01 ps FOM fully-integrated low-dropout regulator with full-spectrum power-supply-rejection for wideband communication systems," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 306–307.
[8] X. L. Tan, S. S. Chong, P. K. Chan, and U. Dasgupta, "A LDO regulator with weighted current feedback technique for 0.47 nF–10 nF capacitive load," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2658–2672, Nov. 2014.
[9] K. Luria, J. Shor, M. Zelikson, and A. Lyakhov, "Dual-mode low-drop-out regulator/power gate with linear and on–off conduction for microprocessor core on-die supply voltages in 14 nm," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 752–762, Mar. 2016.
[10] Y. Okuma *et al.*, "0.5-V input digital LDO with 98.7% current efficiency and 2.7-μA quiescent current in 65 nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2010, pp. 1–4.
[11] S. B. Nasir, S. Gangopadhyay, and A. Raychowdhury, "A 0.13 μm fully digital low-dropout regulator with adaptive control and reduced dynamic stability for ultra-wide dynamic range," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 98–99.
[12] S. B. Nasir, S. Sen, and A. Raychowdhury, "A 130 nm hybrid low dropout regulator based on switched mode control for digital load circuits," in *Proc. IEEE Eur. Solid-State Circuits Conf.*, Sep. 2016, pp. 317–320.
[13] Y. H. Lee *et al.*, "A low quiescent current asynchronous digital-LDO with PLL-modulated fast-DVS power management in 40 nm SoC for MIPS performance improvement," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 1018–1030, Apr. 2013.
[14] C.-C. Chiu *et al.*, "A 0.6 V resistance-locked loop embedded digital low dropout regulator in 40 nm CMOS with 77% power supply rejection improvement," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2013, pp. 166–167.
[15] F. Yang and P. K. T. Mok, "A 0.6–1 V input capacitor-less asynchronous digital LDO with fast transient response achieving 9.5 b over 500 mA loading range in 65-nm CMOS," in *Proc. IEEE Eur. Solid-State Circuits Conf.*, Sep. 2015, pp. 180–183.
[16] F. Yang and P. K. T. Mok, "Fast-transient asynchronous digital LDO with load regulation enhancement by soft multi-step switching and adaptive timing techniques in 65-nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2015, pp. 1–4.
[17] S. Gangopadhyay, D. Somasekhar, J. W. Tschanz, and A. Raychowdhury, "A 32 nm embedded, fully-digital, phase-locked low dropout regulator for fine grained power management in digital circuits," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2684–2693, Nov. 2014.
[18] Y.-J. Lee *et al.*, "A 200-mA digital low drop-out regulator with coarse-fine dual loop in mobile application processor," *IEEE J. Solid-State Circuits*, vol. 52, no. 1, pp. 64–76, Jan. 2017.
[19] Z. Zhao and A. Prodic, "Continuous-time digital controller for high-frequency DC-DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 564–573, Mar. 2008.
[20] Y. Tsividis, "Event-driven data acquisition and digital signal processing—A tutorial," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 8, pp. 577–581, Aug. 2010.
[21] D. Kim and M. Seok, "Fully integrated low-drop-out regulator based on event-driven PI control," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Jan./Feb. 2016, pp. 148–149.
[22] M. Kurchuk, C. Weltin-Wu, D. Morche, and Y. Tsividis, "Event-driven GHz-range continuous-time digital signal processor with activity-dependent power dissipation," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2164–2173, Sep. 2012.
[23] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," *Proc. IEEE*, vol. 84, no. 11, pp. 1584–1614, Nov. 1996.
[24] W. P. M. H. Heemels, K. H. Johansson, and P. Tabuada, "An introduction to event-triggered and self-triggered control," in *Proc. IEEE 51st Annu. Conf. Decision Control*, Dec. 2012, pp. 3270–3285.
[25] J. Lunze and D. Lehmann, "A state-feedback approach to event-based control," *Automatica*, vol. 46, no. 1, pp. 211–215, Jan. 2010.
[26] E. Kofman and J. H. Braslavsky, "Level crossing sampling in feedback stabilization under data-rate constraints," in *Proc. IEEE 45th Conf. Decision Control*, Dec. 2006, pp. 4423–4428.
[27] Y. Lim, J. Lee, S. Park, and J. Choi, "An extemal-capacitor-less low-dropout regulator with less than −36 dB PSRR at all frequencies from 10 kHz to 1 GHz using an adaptive supply-ripple cancellation technique to the body-gate," in *Proc. IEEE Custom Integr. Circuits Conf.*, Apr./May 2017, pp. 1–4.

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