A 63-dB DR 22.5-MHz 21.5-dBm IIP3 Fourth-Order FLFB Analog Filter

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***Abstract*— In this paper, a fourth-order continuous-time follow-the-leader-feedback (FLFB) low-pass (LP) filter is presented. The outstanding FLFB noise behavior is exploited to minimize power consumption. This is achieved by means of customized implementation solutions based on combination of Active-*RC*/Active-g_m-*RC* cells. The 0.18-μm CMOS prototype performs 22.5-MHz −3 dB LP frequency response. Large linearity and dynamic range were achieved resulting in 21.5-dBm in-band (iB) IIP3 and 87-μV_{RMS} input referred iB integrated noise. The SNR for a −40 dB HD_3 is 63 dB. The overall power consumption is 12.6 mW (i.e., 7 mA from a 1.8-V supply). The efficiency of the proposed technique is demonstrated by the achieved figure-of-merit (150.8 dB $\cdot$ J^{-1}), which favourably compares to the state-of-the-art active-*RC* analog filters.**

***Index Terms*— Active filters, analog filters, analog integrated circuits, follow-the-leader-feedback (FLFB), low power.**

I. Introduction

NEW generation cellular communications (LTE compatible with 4G, WiMax, etc.) require higher data-rate wireless transceivers to be used in portable devices, and lower power budget is typically allocated to the analog section, whereas a certain signal quality (depending on filter order, linearity, and noise [1]) must be maintained. These increasingly demanding specifications are addressed by means of specific architectural/circuital solutions. Frequency response mask specifications become more stringent, and higher-order filter transfer functions are then required [2], [3], while linearity requirements are typically satisfied by means of closed-loop structures such as Active-*RC* or Active-g_m-*RC* with suitable analog circuit design for the active devices (opamps) [4]. Finally, noise requirements are usually achieved by reducing impedance levels (i.e., increasing g_m's or reducing R's), causing a power consumption increase. In these choices, the architecture is often defined in tradeoff with the design robustness. In fact, to ensure design reliability common solutions adopt cascade-of-biquadratic-cell topologies (CoBC, exploiting biquadratic (biquad) cells implementations such as Tow-Thomas, Rauch, or Active-g_m-*RC*, each one properly optimized [5]) where, however, each cell contributes to (and thus increases) the output noise power. Similarly, also in popular single-loop ladder structure, where component variation effects are mitigated, each noisy component (R's and opamps) contributes to (and thus increases) the output noise power [3], [6], [7].

In this scenario, this paper studies the closed-loop multi-loop follow-the-leader-feedback (FLFB) filter topology [8], [9]. To improve linearity, the structure is implemented with Active-*RC* and Active-g_m-*RC* [5]–[10] stages. Moreover, thanks to the particular FLFB closed-loop structure, the noise is dominated by the contribution of the first stage, relaxing noise and power consumption requirements for the other stages, where larger R's and lower g_m's could be used. The saved power can be spent to increase opamp linearity.

This concept is demonstrated with a 22.5-MHz fouth-order low-pass (LP) filter that achieves 21.5-dBm IIP3, 63-dB SNR for −40-dB HD_3, which satisfies aggressive LTE transceivers specs [3], [11], and achieves state-of-the-art and figure-of-merit (FoM) for Active-*RC* filters (150.8 dB $\cdot$ J^{-1}).

This paper is organized as follows. Section II introduces the filter transfer function (TF) design, discussing some relevant tradeoffs between in-band (iB) and out-of-band (OoB) filter selectivity. Section III describes the architecture of the fourth-order filter and addresses the main transistor-level design aspects. Section IV shows the experimental results in terms of frequency response, noise, and linearity performance. Section V draws the conclusions.

II. Filter Noise Optimization

Increasingly complex receivers require challenging noise performance to the analog baseband filter in conjunction with an increased selectivity. Regarding the selectivity, receiver specifications rely on iB accurate gain in the full signal band (B) and OoB rejection for adjacent channels and blockers. Regarding noise performance, the relevant receiver specification is defined in terms of in-band-noise (iBN), (i.e., the total noise integrated in the signal band [0-B]). This implies that eventual OoB-Noise and, in particular, an OoB power spectral density (PSD) peak or increasing noise gain close to B is of limited importance.[1]

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[1] In wireless receivers, due to the intrinsic inaccuracy of analog filter transfer function, a digital accurate filter is needed in the digital section to fully reject adjacent channels and blockers energy. These digital filters reject also OoB-noise. This also requires a certain oversampling ratio between the ADC sampling frequency and the signal band [12].

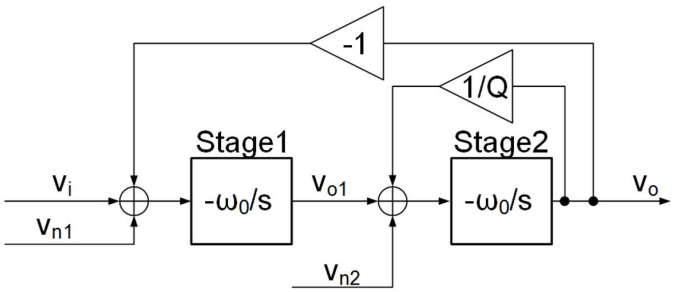


Fig. 1. Biquad cell block scheme.

These two specifications (selectivity and noise) introduce filter design trade-offs as follows.

Let us consider the case of a filter implemented with the CoBC topology, and analyse the noise behavior of the biquad cell (whose architecture is shown in Fig. 1), independently on its circuit implementation, as a first approximation.

The scheme includes two ideal integrators (Stage1 and Stage2) and two noise sources (v_{n1} and v_{n2}). The first one (v_{n1}) models the noise of the components connected to the first stage (like the g_m of the input MOS transistor in the opamp, input and feedback resistors, etc.) and the latter (v_{n2}) is due to the noise sources connected to the second stage. The signal TF v_o/v_i is given in the following:

$$\frac{v_o}{v_i}(s) = \frac{\omega_0^2}{s^2 + s \cdot \frac{\omega_0}{Q} + \omega_0^2}. \tag{1}$$

This TF synthesizes a specific complex poles pair, where ω_0 and Q are frequency and quality factor, respectively. Regarding the noise behavior, the transfer functions from the input stage noise (v_{n1}) and from the internal stage noise (v_{n2}) to the output node (v_o) are given by

$$\frac{v_o}{v_{n1}}(s) = \frac{\omega_0^2}{s^2 + s \cdot \frac{\omega_0}{Q} + \omega_0^2} \tag{2}$$

$$\frac{v_o}{v_{n2}}(s) = -\frac{s \cdot \omega_0}{s^2 + s \cdot \frac{\omega_0}{Q} + \omega_0^2}. \tag{3}$$

As benchmark case, the frequency response mask with 10-MHz passband, 0-dB gain, iB ripple of 1 dB, and 80-MHz stopband with -60 dB rejection is considered here.

The minimum-order filter for a Chebyshev TF, which provides the desired frequency response, is three. This can be realized with the cascade of a biquad cell and a first-order LP filter. Let us assume that in the chain the dominant noise contribution is due to the cell with the highest Q. In this case it is a cell with a complex poles pair having $Q = 1.95$ and $\omega_0 = 2 \cdot \pi \cdot 9.97$ MHz.

The corresponding magnitude frequency responses are plotted in Fig. 2. They show that the internal noise TF (v_o/v_{n2}) has a bandpass behavior with high rejection at dc and a noise peak at the poles frequency (very close to the signal band), whose peak gain is proportional to the poles quality factor Q. On the other hand, v_o/v_i and v_o/v_{n1} coincide and have maximum flat iB response, while they decrease at higher frequencies.

When the poles frequency is placed at the signal band B, the total iB-noise is the combination of the input stage noise (experiencing the LP TF v_o/v_{n1}) and the internal node noise (experiencing a bandpass TF with large noise peaking, v_o/v_{n2}, which could significantly increase total output noise). This is shown in Fig. 3(b), where the output noise PSD of the scheme in Fig. 1 has been plotted (and where both v_{n1} and v_{n2} are fixed to the same Noise PSD value at dc, i.e., 14.1 nV/$\sqrt{}$ Hz).

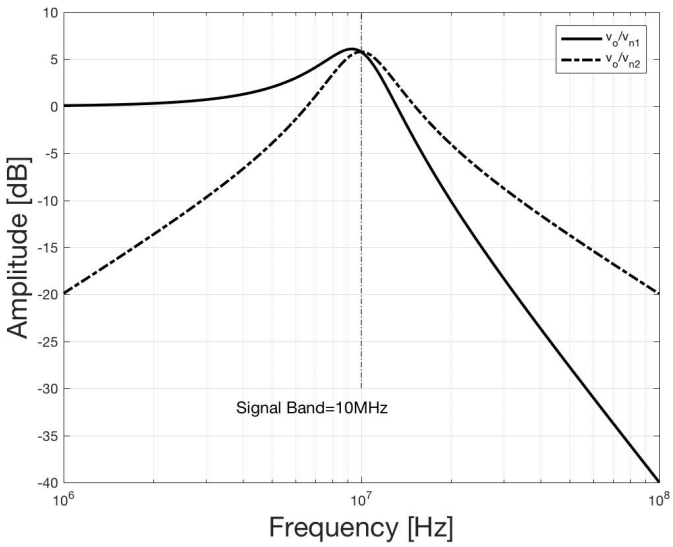
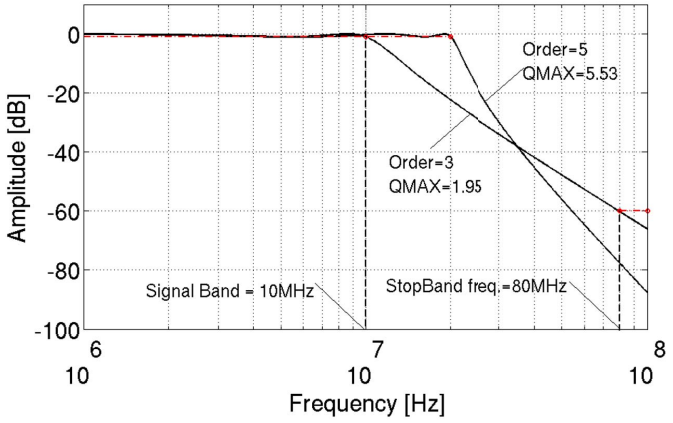
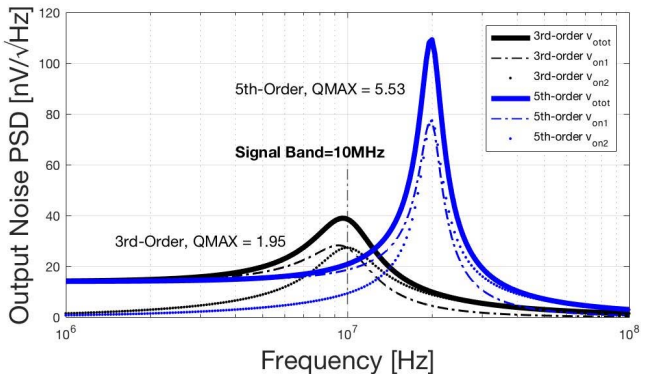


Fig. 2. Biquad cell frequency responses.



(a)



(b)

Fig. 3. Third-order versus fifth-order Chebyshev filter comparison in terms of (a) overall Frequency Response and (b) output noise PSD for the highest-Q biquadratic cell.

Integrating output noise PSD in the full signal band results in 78 μV_{rms}, higher than the input stage noise contribution v_{n1} (54 μV_{rms}). This noise increase is due to the internal node bandpass contribution (v_{n2}, approximately equal to 56 μV_{rms}). This peculiar noise shaping [13] appears in every biquad having an integrator as input stage and forces to consider (and eventually minimize by proper transistor-level design choices) both v_{n1} and v_{n2} contributions. For this reason, aggressive biquad cell performance requires customized aggressive design, and two options are possible.

The first option, operating at circuit level, would properly reduce all noise sources (including the internal noise source components producing v_{n2}) by increasing g_m's and reducing R's. This would dramatically increase power consumption.

The second option is to implement a different TF with higher poles frequency and higher-quality factor, but that complies, however, with the filter mask in Fig. 3(a). Usually, TF synthesis uses the lowest cutoff frequency, with the lowest order and with the poles frequency around the signal Band ($f_p \approx B$) [3], [14]. However, as previously described, locating the poles frequency around B ($f_p \approx B$) results in a significant noise PSD peak in the signal band. Increasing the filter poles frequency ($f_p > B$) with higher filter order and higher poles Q-factor results in higher PSD peak. Assuming the same mask specification as above, the TF could be synthesized assuming a cut-off frequency of 20 MHz (much larger than the signal band, i.e., 10 MHz). In order to fit the mask, a Chebyshev fifth-order TF must be chosen, whit the largest Q poles having $Q = 5.53$ and $\omega_0 = 2 \cdot \pi \cdot 19.88$ MHz. The resulting output noise PSD is plotted in Fig. 3(b), including its different contributions. In this case, a higher output noise PSD peak appears, but this peak occurs around the poles, i.e., at a frequency much higher than B. For the fifth-order case, the total integrated iB output noise (between 0 Hz and 10 MHz) is 49 μV_{rms}, i.e., 4 dB lower than the third-order case. This means, that in terms of iB-noise, higher-order/larger-bandwidth TFs are better than the minimum-order/minimum-bandwidth solutions. Nonetheless, higher-order/larger-bandwidth solutions require more opamps to synthesize the higher-order TF. On top of this, the opamps need larger unity gain bandwidth to enable the larger filter bandwidth and the higher Q values. For all these reasons, the total power consumption is strongly increased.

Using CoBC topology for high-order filters (as typically required in advanced LTE transceivers [1]) further stresses this trend, since the total noise of the full CoBC structure has the drawback of piling-up of the input stage noise (v_{n1}) and the internal stage noise contributions (v_{n2}) for each stage in the cascade.

A similar analysis can be carried out for ladder filters topologies [5].

In conclusion, it appears that the CoBC topology strongly suffers from this noise behavior (iB-noise and OoB-noise) and any adopted noise-reduction solution would inevitably increase power consumption.

This paper explores the use of a different filter topology to reduce iBN without increase in the power consumption. The multi-loop FLFB topology is hereby exploited to synthesize a fourth-order LP TF, avoiding noise sources pile-up (although v_{n1} and v_{n2} are present, as in Fig. 1) and synthesizing four poles with one single cell (instead of two poles as in classical biquads). This reduces power consumption, freeing up a power budget to increase linearity.

In conclusion, this challenging optimization is developed at three levels:

1) At the architectural level adopting a closed-loop topology (the FLFB one instead of the CoBC), whose noise is dominated, at the first-order, by a single first stage (and not by several ones as in the CoBC and in the ladder).
2) At the implementation level, customizing the use of Active-*RC* and Active-g_m-*RC* in the FLFB structure.
3) At the circuit level by optimizing g_m's and R's values of the internal stages in order to make their noise contribution in the signal band negligible.

In this way, the minimum-order/minimum-bandwidth solution TF can be adopted.

III. Follow-the-Leader-FeedBack Fourth-Order Filter

Based on the above considerations, a benchmark fourth-order filter has been implemented with the FLFB topology. The filter block diagram is shown in Fig. 4(a). The structure has been optimized by proper combination of three closed-loop cells (Cell1, Cell2, and Cell3). Cell1 is an integrator, Cell2 synthesizes a single pole LP TF, and Cell3 synthesizes a unitary gain biquadratic cell TF. This scheme can be implemented by Active-*RC* (Cell1 and Cell2) and Active-g_m-*RC* (Cell3, [10]) structures as shown in Fig. 4(b). More in detail, the Active-g_m-*RC* cell exploits the opamp unity gain bandwidth (ω_{U3}) for an efficient complex poles pair synthesis [10]

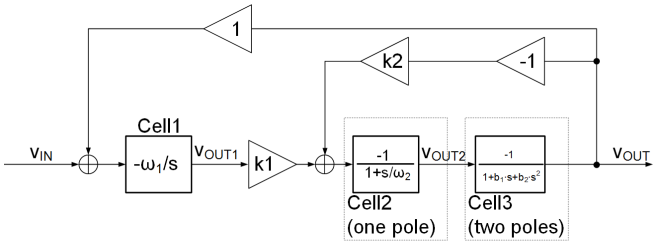
$$\frac{v_{out}}{v_{out2}}(s) \cong -\frac{R_5}{R_4} \cdot \frac{1}{1 + s \cdot \left(1 + \frac{R_5}{R_4}\right) \cdot \frac{1}{\omega_{U3}} + s^2 \cdot \frac{C_3 \cdot R_5}{\omega_{U3}}}. \quad (4)$$

Global feedbacks (implemented by R_6 and R_3) synthesize the fourth-order LP TF. The opamp large gain and bandwidth in Cell1 guarantees an efficient virtual ground for the first Active-*RC* cell, which allows using this overall filter structure in combination of a preceding passive mixer [1], as typically occurs in high-efficiency receivers.

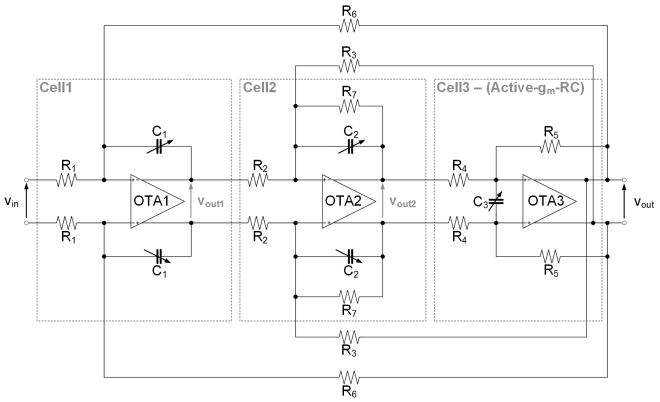
A. Filter Transfer Function

Assuming ideal opamps for Cell1 and Cell2 (i.e., with infinite gain and bandwidth) and an opamp with infinite dc-gain and unity gain bandwidth equal to ω_{U3} for Cell3, the filter synthesizes a fourth-order LP TF that can be written as

$$\frac{v_{out}}{v_{in}}(s) \cong -\frac{R_6}{R_1} \cdot \frac{1}{s^4 \cdot a_4 + s^3 \cdot a_3 + s^2 \cdot a_2 + s \cdot a_1 + 1} \quad (5)$$



(a)



(b)

Fig. 4. (a) Multipath filter block. (b) Schematic top-view.

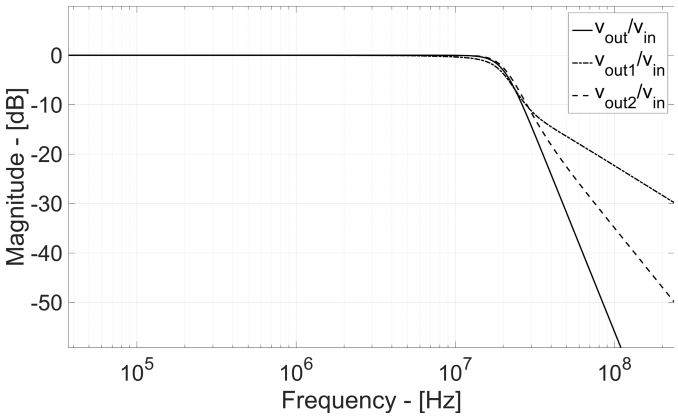


Fig. 5. Filter simulated frequency response.

where a_i values are given by

$$a_4 = \frac{C_1 C_2 C_3 R_2 R_4 R_6}{\omega_{U3}}$$
$$a_3 = \frac{C_1 C_3 R_2 R_4 R_6}{\omega_{U3} R_7} + \frac{C_1 C_2 R_2 R_4 R_6}{\omega_{U3} R_5} + \frac{C_1 C_2 R_2 R_6}{\omega_{U3}}$$
$$a_2 = \frac{C_1 R_2 R_4 R_6}{\omega_{U3} R_5 R_7} + \frac{C_1 R_2 R_6}{\omega_{U3} R_7} + \frac{C_1 C_2 R_2 R_4 R_6}{R_5}$$
$$a_1 = \frac{C_1 R_2 R_4 R_6}{R_5 R_7} + \frac{C_1 R_2 R_6}{R_3}. \quad (6)$$

The transfer functions to the output node ($v_{\text{out}}/v_{\text{in}}$) and to each internal node ($v_{\text{out1}}/v_{\text{in}}$, and $v_{\text{out2}}/v_{\text{in}}$) are plotted in Fig. 5. The design parameters of the filter are listed in Table I, where internal loop resistors values are similar to R_1 and R_6 values in order to limit the OoB-noise peaking (i.e., similar to the v_{n2} contribution in Figs. 1–3).

B. Filter Noise Performance

The FLFB structure is selected for the high-pass filtering shaping of all the internal noise contributions. Assuming a large Cell1 iB-gain (it is an integrator), all the other contributions become, at the first order, negligible when referred to the input, because they are divided by the Cell1 gain which is very high at low frequency.

The Filter iB input-referred-noise PSD (i.e., $\text{IRN}_{\text{FILTER}}$) is then dominated only by the three noise sources connected to the input node. These contributions are the thermal noise of $R_1 - R_6$ and the iB thermal noise of Cell1 opamp IRN_{OTA1} (the flicker noise is negligible due to the large signal band). The overall $\text{IRN}_{\text{FILTER}}$ can be written as

$$\text{IRN}^2_{\text{FILTER}} = 8 \cdot k \cdot T \cdot \left(R_1 + \frac{R_6}{G^2}\right) + \text{IRN}^2_{\text{OTA1}} \cdot \left(1 + \frac{1}{G}\right)^2 \quad (7)$$

where G is the signal dc-gain: $G \approx R_6/R_1$. This noise expression is valid also for any filter order implemented with the FLFB structure, even for high-order filters, as requested by advanced telecommunications system.

TABLE I
FILTER DESIGN PARAMETERS (FOURTH BUTTERWORTH)

Parameter	Value
R_1, R_6	2.61kΩ
R_2, R_4, R_5	653Ω
R_3, R_7	1.3kΩ
C_1	5.2pF
C_2	6.9pF
C_3	8pF
OTA_3 UGB (ω_{U3})	$2\cdot\pi\cdot$65.8 Mrad/s

C. Filter Design in 0.18-μm CMOS Technology

The prototype parameters have been optimized by means of a MATLAB-based procedure. R_1 and R_6 values can be designed as a function of iB-noise ($\text{IRN}_{\text{FILTER}}$) and dc-gain ($G$) requirements

$$R_1 = \frac{\text{IRN}^2_{\text{FILTER}} - \left(1 + \frac{1}{G}\right)^2 \cdot \text{IRN}^2_{\text{OTA1}}}{8 \cdot k \cdot T \cdot \left(1 + \frac{1}{G}\right)} \quad (8)$$
$$R_6 = G \cdot R_1. \quad (9)$$

The design procedure assigns 25% of the total noise to the Opamp1. This has been demonstrated to be an optimum value to reduce power consumption [15].

The other resistors and capacitors are sized according to the output swing/linearity performance and the required TF, respectively. For instance, for a given R_1 value, a small C_1 value would increase the first stage integrator unity gain

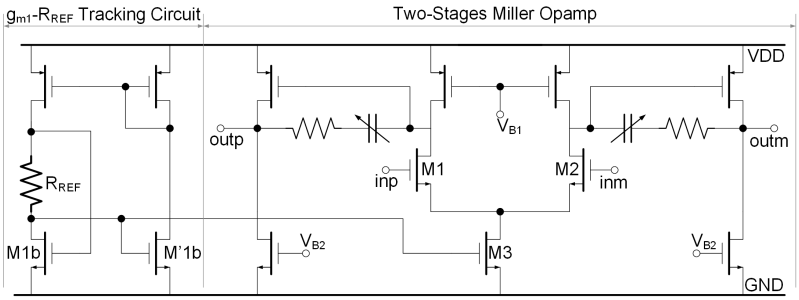


Fig. 6. Cell3 Opamp3 schematic.

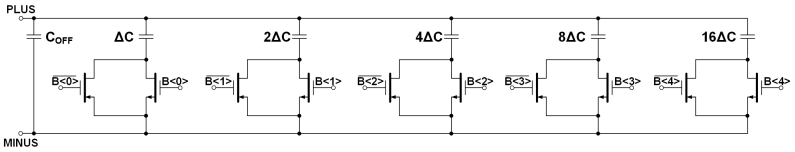


Fig. 7. Programmable capacitor array structure.

TABLE II
OPAMPS DESIGN PARAMETERS

	Opamp1	Opamp2	Opamp3
I_1 [mA]	0.33	0.33	0.42
I_2 [mA]	0.9	0.9	0.9
g_{m1} [mA/V]	5.8	5.8	6
g_{m2} [mA/V]	4.3	4.3	5.7
R_c[Ω]	250	250	180
C_c [pF]	3.6	3.6	10
r_{dsN}[Ω]	25.2k	25k	17.7k
r_{dsP}[Ω]	41.4k	41.4k	37.2k
DC-Gain [dB]	44.3	44.3	41.8

bandwidth [i.e., $1/(C_1 \cdot R_1)$] and the filter capability to high-pass filter the internal loop noise sources (hence it is a good option for noise). On the other hand, with this choice, signal swing at the output of both Opamp1 and Opamp2 increases, leading to more severe requirements for Opamp1-Opamp2 output stage current to achieve linearity specs. On the contrary, higher C_1 value would reduce Opamp1-Opamp2 output swing, while increasing the iB integrated noise. In this design, to optimize linearity, the same iB unitary gain has been assumed at the output of each cell, in order to perform the same iB output swing (and linearity opamp output stage performance) versus input swing.

The internal nodes iB-gain, i.e., $v_{\text{out1}}/v_{\text{in}}$ and $v_{\text{out2}}/v_{\text{in}}$ are given by (with $G = 1$)

$$\frac{v_{\text{out1}}}{V_{\text{in}}} \cong -G \cdot \left(\frac{R_2}{R_5} \cdot \frac{R_4}{R_7} + \frac{R_2}{R_3}\right) = \frac{R_2}{R_5} \cdot \frac{R_4}{R_7} + \frac{R_2}{R_3} \quad (10)$$

$$\frac{v_{\text{out2}}}{v_{\text{in}}} \cong \frac{G}{\frac{R_5}{R_4}} = \frac{R_4}{R_5}. \quad (11)$$

Based on these considerations, the resulting resistors values are listed in Table I, while the main opamps parameters are in Table II.

The operational amplifiers used in this filter design (Opamp1, Opamp2, and Opamp3) are based on the class-A Miller scheme shown in the right side of Fig. 6. The opamp in Cell3 has a suitable dedicated bias circuit shown in the left side of Fig. 6. The main task of the bias circuit is to match the input stage transistors (M_1 and M_2)g_m with an external resistor (R_{REF}), as in classical Active-g_m-RC implementation. In particular, M_{1b} and M_1 and M_2 transistors are based on the same finger aspect ratio W/L and the current source (M_3) operates M_1 and M_2 with the same current density of M_{b1}. Thus, the input g_m is forced to be proportional to $1/R_{\text{REF}}$. This enables the g_m to track the integrated resistor R_{REF}, allowing full technological process spread calibration by acting only on variable capacitors [10]. This way the overall filter TF [see (5)] is correlated with the time constants of the passive components (R and C). These passive components nominal values are typically poorly controlled in integrated technologies and can exhibit a variation up to ±40%, due to process, temperature variations and aging. To compensate for such variations and align the filter TF, proper tuning circuits need to be adopted [16]. All capacitors, including Opamp3 Miller cap, are implemented using 5-bits arrays, which are externally tuned through manually setting the proper digital code during measurements. A schematic of the capacitor array is shown in Fig. 7. It is composed by binary-weighted capacitors and complementary switches controlled by the input 5 bits digital word. The resulting ΔC step capacitance is

$$\Delta C = \frac{(C_{\max} - C_{\min})}{2^{N-1}} \quad (12)$$

where $N = 5$, $C_{\min}$ and $C_{\max}$ are, respectively, given by (13) and (14), with ζ representing the maximum relative variation of the capacitance due to the technological spread

$$C_{\min} = C_{\text{nom}}/(1+\zeta) \quad (13)$$

$$C_{\max} = \frac{C_{\text{nom}}}{(1-\zeta)}. \quad (14)$$

Thanks to 5-bits resolution capacitance array, a maximum deviation from nominal frequency response of about 3% has been achieved. The full tuning algorithm is not implemented

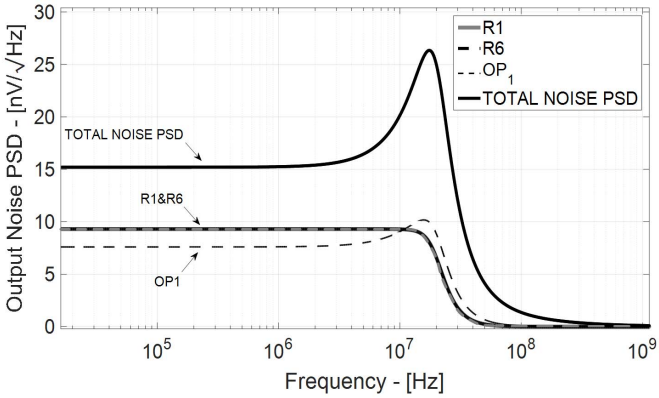


Fig. 8. Cell1 contribution to the output noise and total output noise PSD (Simulation; R_1 and R_6 contributions overlap).

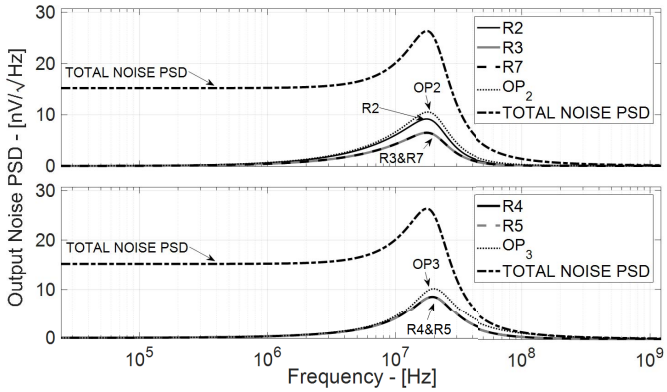


Fig. 9. Cell2 and Cell3 contributions to the output noise PSD (Simulation; R_3 and R_7, and R_4 and R_5 contributions overlap).

here, as it is not the focus of this research activity, and it is left to the full receiver implementation.

All opamps use nMOS transistors input stage, whose larger transconductance at constant current with respect to pMOS reduces the OoB-noise peak close to the signal B. Moreover, all opamps have the same output current since, as it has been highlighted in Fig. 5, the selected design trade-off assumes the same iB output swing for all opamps.

Opamp3 has a slightly higher input stage g_m, compared to Opamp1 and Opamp2, since the Active-g_m-*RC* cell has a lower linearity close the signal B [10]. Hence, in order to mitigate such linearity loss, the Opamp3 input MOS has higher current (in order to avoid OoB-noise power increase due to the input stage g_m reduction).

Finally, the Opamp3 higher output stage g_m guarantees an open-loop phase margin $>70°$ for a 1-pF load, a key point for a stable and accurate Active-g_m-*RC* frequency response, which is slightly sensitive to the output load. The most relevant operating points and small signal parameters of the opamps are listed in Table II.

D. Filter Noise Shaping versus Frequency

The proposed design procedure is based on the assumption that the large Cell1 dc-gain prevents internal nodes noise sources contributions to affect the output noise. However, Cell1 is an integrator and, then its gain decreases with frequency (-20 dB/dec). This implies that the internal noise sources rejection reduces at higher frequencies and experiences a peak around the filter cut-off frequency due to the Q-factor, as described in Section II. Such a situation typically occurs when an Active-*RC* filter (Tow-Thomas, Rauch, etc.) uses an active integrator as input stage. Since the iB-noise increases with frequency, an accurate noise analysis is required. For the design parameters given in Table I, the simulated filter output noise PSD is shown in Fig. 8. Moreover, Fig. 8 shows the simulated output noise PSD for R_1, R_6 and the Opamp1 input stage M_1–M_2 MOS thermal noise. Fig. 9 shows the output noise PSD for all remaining resistors (R_3, R_4, R_5, and R_7) and for Opamp2 and Opamp3 input stage MOS transistors.

At low frequency, internal noise sources are effectively rejected and R_1, R_6, and Opamp1 thermal noise dominates, while, around the poles frequency, Cell2 and Cell3 thermal noise cannot be neglected in terms of total output PSD. The total integrated iB-noise at the output of the filter is 124 μV_{RMS}.

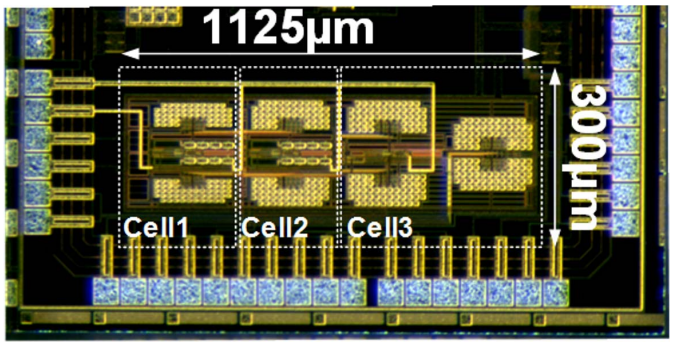


Fig. 10. Filter chip photograph.

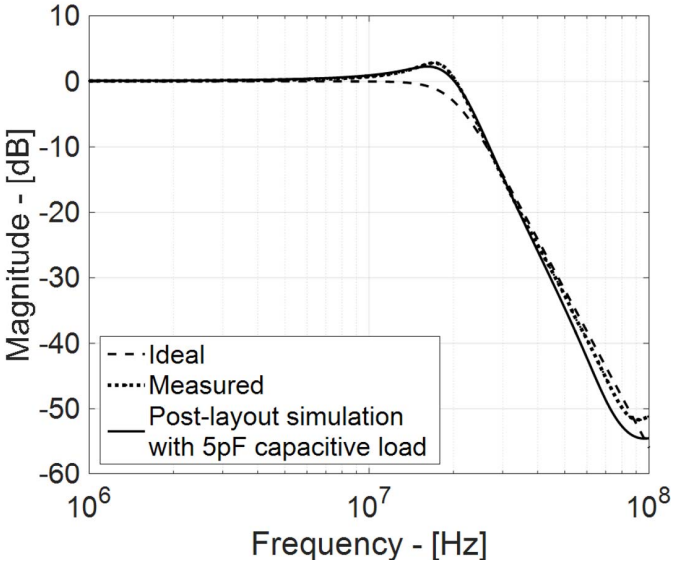


Fig. 11. Filter measured frequency response.

IV. Experimental Results

A filter prototype has been integrated in 0.18-μm CMOS technology. The chip photograph is shown in Fig. 10. The total filter area is 0.33 mm^2, mainly dominated by the capacitor arrays, which represent about 62% of the total area. The filter operates with a single 1.8-V supply voltage and consumes 7 mA.

TABLE III
FILTER PERFORMANCE AND COMPARISON WITH THE STATE-OF-THE-ART

Parameters	De Matteis JSSC'09 [17]	Amir JSSC'09 [18]	Thyagarajan JSSC'11 [19]	Kousai JSSC'07 [20]	Vasilopoulos JSSC'06 [21]	Oskooei JSSC'06 [22]	Vigraham JSSC'14 [23]	Wang TCASII'15 [24]	THIS WORK
Order & TF*	4 - B	5- C	5 - C	5 - C	5 - C	6 - B	4 – B	4 - B	**4 - B**
Topology	Active-g_m-RC	Active-RC	Active-RC	Active-RC	Active-RC	g_m-C	Active-RC	Active-RC	**Active-RC& Active-g_m-RC**
CMOS Tech. [µm]	0.13	0.13	0.18	0.13	0.12	0.09	0.065	0.065	**0.18**
Supply voltage [V]	0.55	1	1.8	1.5	1	1	0.6	1.2	**1.8**
Power [mW]	3.5	7.5	5.6	11.3	6.1	4.35	26.2	9.6	**12.6**
Gain [dB]	0	0	0	2	0	-2.8	0	0	**0.5**
f_0 [MHz]	11.3	20	20	19.7	5	13.5	70	5	**22.5**
IRN [μV_{RMS}]	110	232	980	113	312	275.5	365	80	**87**
THD [dBc]	-40	-40	--	-49.1	-40	-40	-60	--	**-40**
SNR [dB]	60	63.7	60.3	69	73	63	55.8	--	**63**
f_{IM3} [MHz]	2	0.27	6	0.5	3.9	1	2	1	**4**
IIP3 [dBm]	10	31	43.3	18.3	20.4	22.1	18	19	**21.5**
SFDR [dB]	-	-	60.3	69	73	-	65	-	**59.8**
Area [mm^2]	0.43	1.53	0.2	0.2	0.25	0.239	0.38	0.8	**0.35**
Power/pole [mW]	0.87	1.5	1.12	2.26	1.22	0.72	6.55	2.4	**3.15**
f_{IM3}/f_0	0.17	0.013	0.3	0.02	0.78	0.07	0.02	0.2	**0.17**
FOM [dBJ^{-1}]	144.36	143.2	152	139.6	146.7	144.9	134	144.8	**150.8**

** B=Butterworth, C=Chebyshev, E=Elliptic*

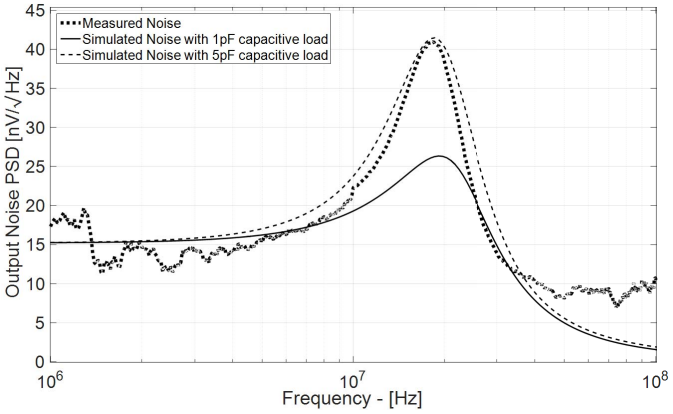


Fig. 12. Filter measured output noise PSD.

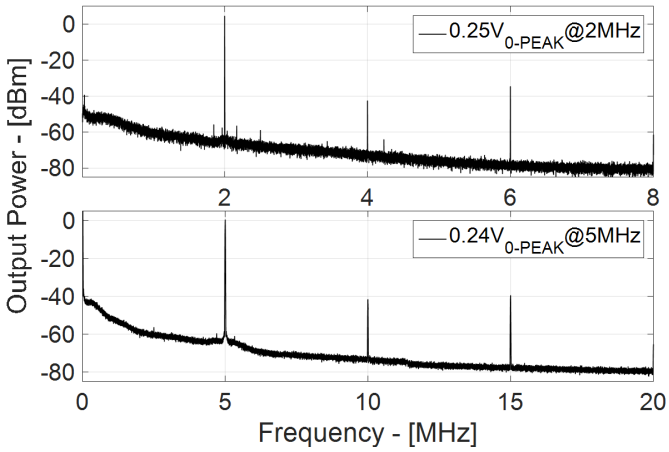


Fig. 13. Output Spectrum for input signal of 0.25 $V_{0\text{-PEAK}}$ at 2 MHz and 0.24 $V_{0\text{-PEAK}}$ at 5 MHz.

The measured LP filter frequency response is shown in Fig. 11 and is compared to the ideal fourth-order Butterworth TF. The measured −3 dB frequency is 22.5 MHz. A +3 dB peak is observed close to the ideal −3 dB frequency. This effect is mainly due to the large (5 pF) parasitic capacitance at the filter output, due to the test set-up (underestimated in the design phase to be 1pF). In particular, the probes and the PCB routing increase the capacitive load, which becomes higher than the C1−C3 caps used in the design (see Table I), and determines such a peaking, since the Active-gm-*RC* opamp phase margin is particularly sensitive to the capacitive load. These considerations are validated by the good matching between the post-layout filter simulated frequency response assuming 5 pF output load (approximately the measured parasitic capacitance in the PCB used for testing) and the measured filter frequency response (see Fig. 11).

The noise measurement set-up is composed by the cascade of the filter and a specifically designed off-chip large bandwidth low-noise amplifier, having 40-dB passband gain and 5 nV/$\sqrt{\text{Hz}}$ iBN PSD over a 25-MHz bandwidth. Fig. 12 shows the measured output noise PSD of the filter (Measured Noise). For sake of completeness the simulated post-layout output

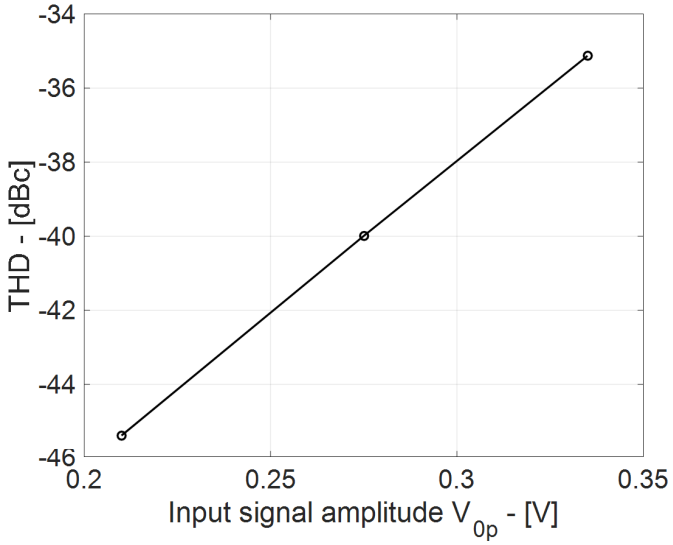


Fig. 14. THD versus input signal amplitude at 5 MHz.

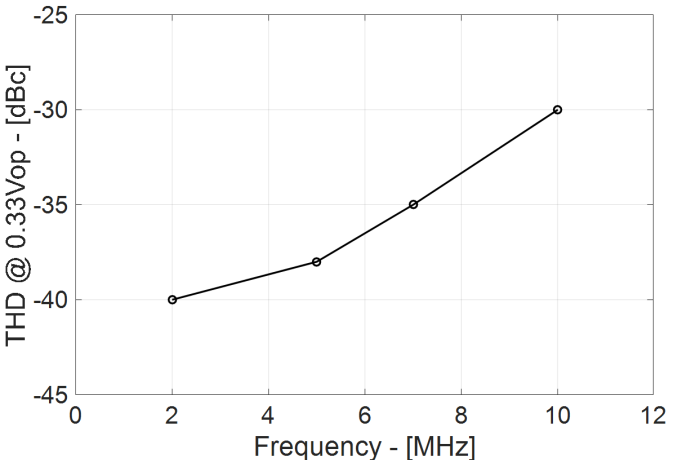


Fig. 15. THD versus input signal frequency at 0.33 $V_{0\text{-PEAK}}$.

noise PSD of the filter with 5-pF output load has been also plotted. The noise PSD features about 3.9 dB higher noise peak (42 nV/$\sqrt{}$ Hz with respect to 27 nV/$\sqrt{}$ Hz) compared to the simulated noise PSD in nominal corner conditions (27 °C temperature and typical-typical process) and with a smaller load (1 pF). This is coherent with the frequency response measurements in Fig. 11, where +3 dB peak has been observed with respect to the ideal design case of 1-pF output load.

The filter linearity performance has been evaluated in terms of single tone test (HD and 1-dB Compression-Point) and two-tones test (IIP3).

The filter output spectrum has been separately measured with two different input tones at 2 and 5 MHz. Fig. 13 shows the output spectrum for one input tone of 0.25 $V_{0\text{-PEAK}}$ at 2 MHz and 0.25 $V_{0\text{-PEAK}}$ at 5 MHz, respectively. In both cases, −40 dBc of HD_3 has been achieved, resulting in 63-dB DR at 124-μV_{RMS} output noise power. Moreover, the output spectrum for 5-MHz input signal features a slight HD_2 power increase.

In Fig. 14, the THD is plotted for different input voltages zero-peak values at 5-MHz input frequency. A minimum

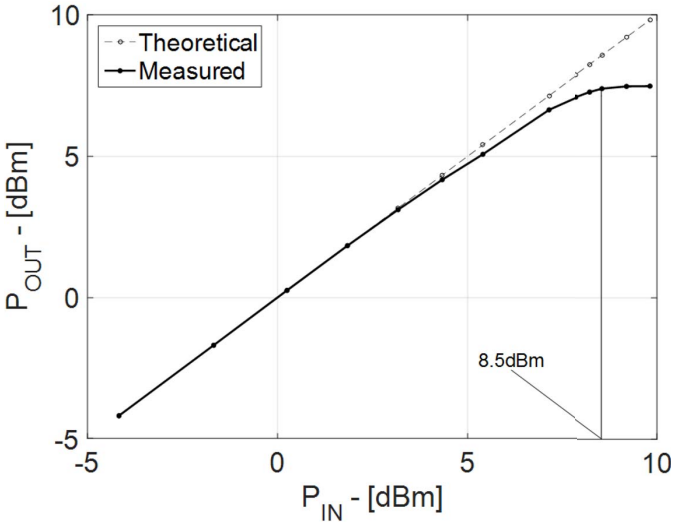


Fig. 16. 1-dB Compression-Point at 5-MHz input tone.

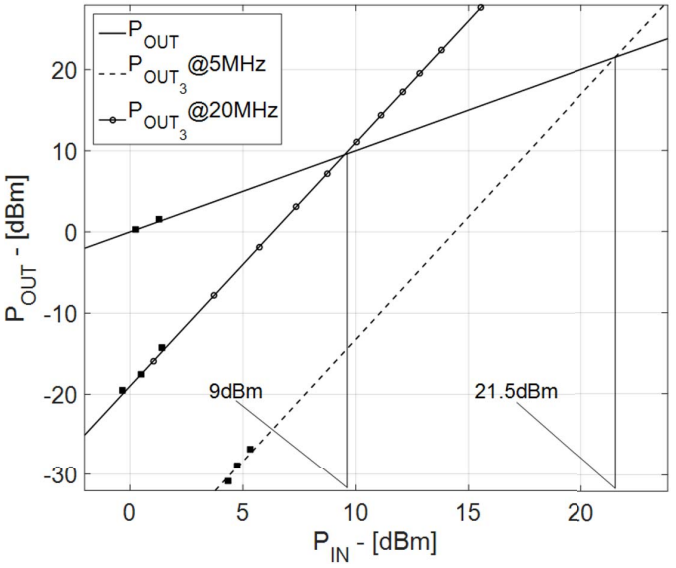


Fig. 17. iB and at band-edge IIP3.

−35 dBc of THD is obtained for 0.335 $V_{0\text{-PEAK}}$. Distortion has been also evaluated with respect to the input tone frequency, as shown in Fig. 15, considering an input signal of 0.33 $V_{0\text{-PEAK}}$ amplitude and resulting in −30 dBc at 10-MHz input frequency.

The 1-dB compression-point is also illustrated in Fig. 16, where 8.5 dBm has been achieved with a 5-MHz input tone.

Finally, the two-tones test for IIP3 has been performed in two different cases: with iB (5 and 6 MHz) two-tones and at the edge of the filter band tones (20 and 21 MHz), resulting in 21.5 and 9 dBm IIP3, respectively. The IIP3 decreases when the frequency of the input tones increases. This is due to the lower loop gain (G_{loop}) of the filter at the edge of the band and is typical of any closed-loop analog circuit. Fig. 17 shows the output power spectrum for both inter-modulation tests.

The filter performance is then summarized in Table III, compared to state-of-the-art Active-*RC* analog filters having similar passband ranges [17]–[24]. A FoM is typically used to directly compare analog filters, taking into account the key

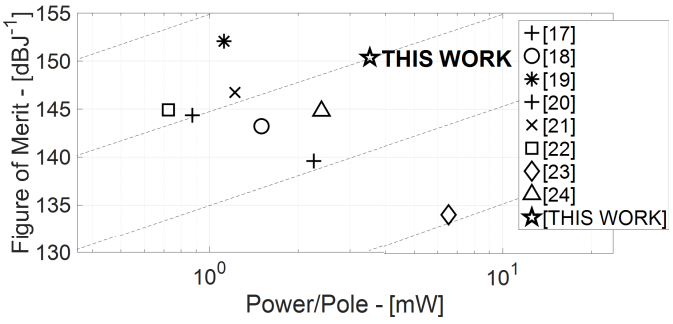


Fig. 18. Active-*RC* Filters FoM versus power/pole (Dashed lines connects isometric points, i.e., points characterized by a constant ratio between FoM and Power/Pole).

performance as power, linearity, noise and bandwidth. The selected FoM [25]–[28] is defined as follows:

$$\text{FoM} = 10 \cdot \log_{10} \frac{\text{IMFDR}_3 \cdot f_{-3\ \text{dB}} \cdot N}{\text{PW}} \cdot \frac{f_{\text{IM3,LOW}}}{f_{\text{POLES}}} \quad (15)$$

where PW is the total power consumption, $f_{-3\,\text{dB}}$ is the cut-off frequency, N is the number of poles, and IMFDR_3 is the spurious-free IM3 which is calculated as

$$\text{IMFDR}_3 = \left(\frac{\text{IIP3}}{V_{N,\text{in}}}\right)^{4/3}. \quad (16)$$

IIP_3 is the third-order input intercept point, while $V_{N,\text{in}}$ is the iB integrated input-referred-noise. Such FoM takes into account the distance of the inter-modulation product from the poles frequency by including the ratio between the lower third-order inter-modulation tone ($f_{\text{IM3,LOW}}$) and the poles frequency (f_{POLES}), as discussed in [25]. FoM versus (Power per pole) has been plotted in Fig. 18, showing that the filter compares well to state-of-the-art solutions.[2]

V. Conclusion

The presented fourth-order analog filter exploits the FLFB topology to reduce iB output noise and uses a single compact cell for four poles synthesis. This approach frees up power that can be used to improve linearity. The filter design, composed by the cascade of Active-*RC* and Active-g_m-*RC* cells, has been described and characterized in terms of power, frequency response, noise and linearity.

The prototype, integrated in 0.18-μm CMOS technology, features a 22.5 MHz -3 dB frequency and exhibits 21.5-dBm iBIIP3 at 5- and 6-MHz input tones with 87 μV_{RMS} of input integrated iBN power. The achieved output SNR is 63 dB, where the correspondent output signal has a HD_3 of 40 dBc and the power consumption is 12.6 mW. The high achieved FoM (150.8 dBJ^{-1}) validates the proposed circuit.

Acknowledgment

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[2]The filter in [19] achieves high efficiency thanks to a driving solution that could be introduced also in the filter topology presented in this paper, increasing its efficiency.

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