A Spur-and-Phase-Noise-Filtering Technique for Inductor-Less Fractional-N Injection-Locked PLLs

Alvin Li, Yue Chao, Xuan Chen, Liang Wu, *Member, IEEE*, and Howard C. Luong, *Fellow, IEEE*

***Abstract*— A novel phase-noise-filtering technique based on phase-domain averaging is proposed to suppress the large injection spurs and poor high-frequency phase noise of inductor-less injection-locked phase-locked loops (IL-PLLs). Demonstrated using a 1.2-GHz fractional-N IL-PLL based on a capacitive-ring-coupled ring oscillator, wideband spur-and-phase-noise suppression of up to 20 dB is achieved allowing for phase noise as low as −146 dBc/Hz at 30-MHz offset with a 2-MHz resolution. This allows for an inductor-less alternative to LC-based PLLs in scaled-digital CMOS technologies. The 65-nm CMOS prototype improves 10-MHz phase noise from −115 to −135 dBc/Hz, injection spurs from −40.5 to −57 dB, and integrated jitter from 3.57 to 1.48 ps while occupying an area of 0.6 mm^2 and consuming 19.8 mW from a 0.85-V supply, resulting in an FoM and FoM$_{\text{Jitter}}$ of −163 and −223.6 dB, respectively.**

***Index Terms*— Capacitor ring (C-ring), coupled, delay line (DL), filter, fractional-N, IL, inductorless, injection-locked phase-locked loop (IL-PLL), local oscillator (LO), phase averager, phase noise, PLL, ring oscillator (RO), synthesizer, voltage-controlled oscillator (VCO).**

I. Introduction

In addition to high-speed digital clocking, frequency synthesizers are widely used in both wireline and wireless communication systems. To support high data rates, wireless standards often employ complex modulation schemes, which impose stringent-integrated jitter and spot-phase-noise requirements on the frequency synthesizer. This typically mandates the use of high quality factor (Q) *LC*-oscillator-based phase-locked loops (PLLs) due to their superior phase-noise compared to ring-oscillator (RO) implementations. However, with the trend toward modern multi-band and multi-mode radios for large-scale integration, in addition to the aggressive pace of CMOS technology scaling, the potential benefits of inductor-less RO-based PLLs are becoming increasingly attractive. This is due to their wider frequency tuning range, smaller area, lower sensitivity to electromagnetic coupling, and excellent process scalability compared to *LC*-PLLs. Nevertheless, the poor phase noise and integrated jitter of RO-PLLs have thus far excluded them from high-data-rate wireless applications.

This paper presents a phase-noise-filtering technique based on continuous phase-domain averaging to reduce both the high-frequency phase noise and spurs generated by RO-based injection-locked (IL)-PLLs. Additionally, a capacitive-ring-coupled IL RO is introduced to increase the IL-PLL's fractional frequency resolution by providing additional injection phases and reducing the mismatch between delay cells. By combining both techniques, an inductor-less frequency synthesizer is presented with an overall phase-noise performance comparable to that of *LC*-PLLs. Demonstrated in a 65-nm CMOS technology, the prototype is capable of wideband spur-and-phase-noise suppression of up to 20 dB and achieves phase noise as low as −146 dBc/Hz at 30-MHz offset. The rest of the paper is organized as follows: Section II reviews several recently proposed techniques for phase noise and jitter reduction. Additionally, the operating principles and key issues of IL oscillators are described. In Section III, the proposed phase-noise-filtering technique is introduced. Section IV gives an overview of the overall frequency synthesizer and describes the key building blocks. Section V presents the measurement results, and finally, the conclusions are drawn in Section VI.

II. Existing Phase-Noise Improvement Techniques

To leverage the benefits of RO-PLLs in high-performance systems, several remarkable techniques have recently been proposed to either cancel the RO's spot-phase noise at high offset frequencies [1], [2] or to aggressively filter their close-in phase noise using edge re-alignment techniques [3]–[12].

A. Spot-Phase-Noise Filtering

In [1], a feed-forward phase-noise cancellation loop is proposed. A delay-discriminator-based phase detector is used to compare the RO's I/Q outputs to an accurately calibrated 90° time delay, similar to commercial spectrum analyzers. The RO's instantaneous phase deviations are then subtracted from the RO's output signal using variable phase shifter in the output path. Unfortunately, this method relies heavily on both accurate amplitude scaling and phase matching between the RO's output cancellation path and the feed-forward detection path in addition to a precisely calibrated 90° time delay, resulting in phase-noise cancellation of less than 12.5 dB.

Manuscript received October 5, 2016; revised February 1, 2017; accepted March 15, 2017. Date of publication April 19, 2017; date of current version July 20, 2017. This paper was approved by Associate Editor Ken Suyama. *(Corresponding authors: Alvin Li and Liang Wu.)*

A. Li, X. Chen and H. C. Luong are with the Department of Electronics and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong (e-mail: alvin.scli@gmail.com).

Y. Chao was with The Hong Kong University of Science and Technology. He is now with Qualcomm Inc., San Diego, CA.

L. Wu was with The Hong Kong University of Science and Technology. He is now with the State Key Laboratory of Millimeter Waves, City University of Hong Kong, Hong Kong (e-mail: eewuliang@ee.ust.hk; liang.wu@cityu.edu.hk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2017.2688384

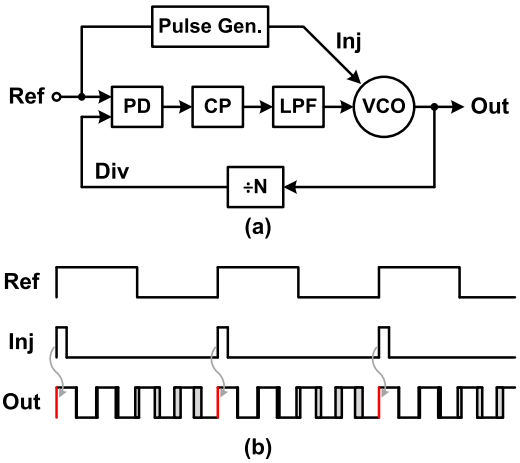


Fig. 1. (a) Block diagram of conventional IL-PLL and (b) timing diagram of periodic VCO edge realignment to suppress accumulated phase noise.

Interestingly, Mikehemar *et al.* [2] propose another feed-forward technique which focuses on canceling the effect of local oscillator (LO) phase noise in the receiver path (reciprocal mixing noise) instead of reducing the LO phase noise directly. While this method can achieve an impressive 20-dB cancellation of reciprocal mixing noise with digitally intensive calibration, it does nothing to improve the effect of LO phase noise in the transmitter path which directly contributes to the error vector magnitude of the transmitted constellation. Additionally, since this method relies on the symmetry of the LO phase-noise skirt, the cancellation would fail in the presence of multiple RX blockers.

B. Injection-Locked PLLs

Unlike the previous cancellation techniques, which focus on reducing spot-phase noise for wireless applications, edge re-timing techniques used in IL-PLLs and multiplying delay-locked loops focus on reducing the RO-PLL's overall integrated jitter by suppressing the LO's close-in phase noise. Initially demonstrated in [3], IL-PLLs periodically realign the voltage-controlled oscillator's (VCO's) noisy edge with a clean reference edge to reset the RO's overall accumulated phase error, as shown in Fig. 1. As a result, the close-in phase noise of the RO-PLL is suppressed by an additional -20 dB/decade within the injection-lock bandwidth (ILBW), which can be as high as $0.5 f_{\mathrm{REF}}$.

For comparison, in conventional type-II PLLs, the free-running RO's phase noise is suppressed by -40 dB/decade only up to the PLL's bandwidth, which is typically limited to $0.05 f_{\mathrm{REF}}$ to ensure loop stability and sufficient spur filtering. Specifically, as illustrated in the linear noise model in Fig. 2, injection locking shapes both the reference and PLL noise according to the NTFs $H_{\mathrm{UP}}(s)$ and $H_{\mathrm{RL}}(s)$, respectively [3]

$$H_{\mathrm{UP}}(s) = \frac{N\beta}{1+(\beta-1)\cdot e^{-j\omega T_r}} e^{-j\omega T_r/2} \frac{\sin(\omega T_r/2)}{\omega T_r/2} \quad (1)$$

$$H_{\mathrm{RL}}(s) = 1 - \frac{\beta}{1+(\beta-1)\cdot e^{-j\omega T_r}} e^{-j\omega T_r/2} \frac{\sin(\omega T_r/2)}{\omega T_r/2} \quad (2)$$

where N is the frequency multiplication ratio, T_r is the reference period, and β is the phase re-alignment factor

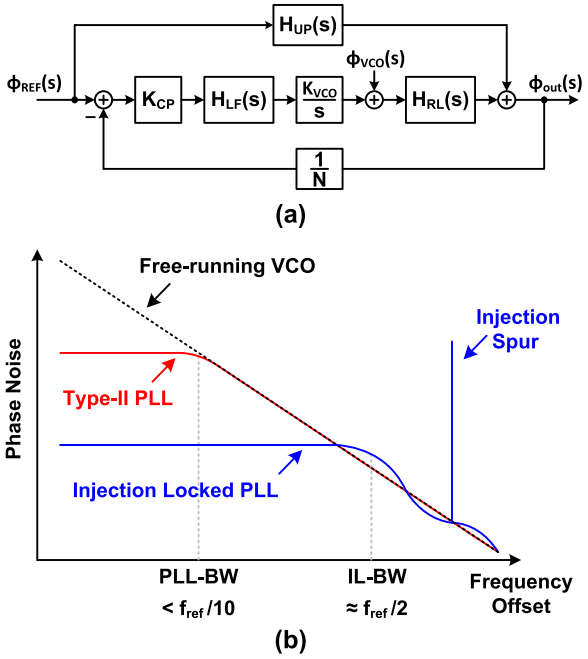


Fig. 2. (a) PLL linear-phase-noise model with injection-locking. (b) Phase-noise suppression characteristics of IL-PLL compared with a conventional type-II PLL.

representing how well the VCO's noisy edge is pulled toward the ideal noiseless edge. In IL-PLLs, where edge re-timing is achieved through current injection, β may lie between 0 and 1, depending on the relative strength between the injected re-timing current and the VCO's self-oscillation current. A $\beta = 0$ represents the case where the injected current has little or no effect on the RO's noisy edge, while a $\beta = 1$ represents perfect edge realignment to the ideal noise-less edge position, completely rejecting the accumulated phase error. From (1) and (2), the ILBW is predominantly determined by both β and the reference frequency $f_{\mathrm{REF}} = 1/T_r$, through the sinc term. A higher β and reference frequency f_{REF} results in a higher ILBW to suppress the PLL's close-in phase noise. The close-in phase noise at frequency offsets below the ILBW is determined by the reference's phase noise shaped by $|H_{\mathrm{UP}}(s)|^2 = N^2$. Therefore, as N increases, the close-in phase-noise suppression becomes less effective as more VCO cycles occur before the accumulated phase error is reset. In RF-PLLs, the use of crystal oscillators as a reference signal source sets practical limitations on the injection frequency to values typically less than 50 MHz.

In addition to low phase-noise performance, achieving a fine-frequency resolution is necessary before IL-PLLs can be utilized in wireless RF applications. Unfortunately, injection locking is inherently an integer-N technique since a signal edge must be present for edge re-timing to occur. Given that a high reference frequency is typically preferred to minimize the IL-PLL's overall jitter and phase noise, according to (1), the resulting frequency resolution is often much wider than the desired channel spacing. To resolve this dilemma, Park *et al.* [7] exploit the multiple phases of a RO to achieve fractional resolution in IL-PLLs. By rotating the injection sequence to specific phases of the RO, a frequency resolution

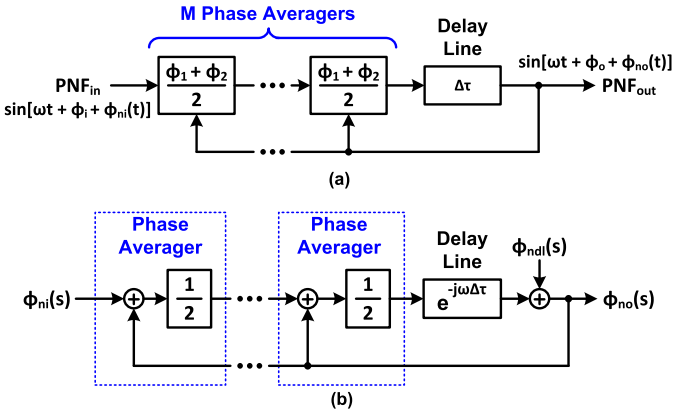


Fig. 3. (a) Block diagram of proposed M-stage PNF and (b) phase-domain noise model of proposed M-stage PNF.

of $f_{RES} = f_{REF}/N_{Phase}$ can be achieved, depending on the number of available phases N_{Phase}. The frequency resolution is limited by delay cell mismatch which degrades as N_{Phase} increases, resulting in larger injection spurs [7].

While edge realignment dramatically reduces the overall integrated jitter and close-in phase noise of RO-PLLs, several critical issues must first be resolved before IL-PLLs can be used in high-data-rate wireless applications. First, injection-locking degrades the RO's already poor high-frequency phase noise due to noise peaking >3 dB around the ILBW, as shown in Fig. 2(b). Second, large spurs are introduced by both sub-harmonic injection and injection timing errors. Finally, the limited frequency resolution of IL-PLLs needs to be increased without increasing the injection spur power. To reduce the phase-noise peaking and high-frequency injection spurs, a phase-noise filtering technique is proposed in Section III. Additionally, a large geometry capacitor-ring (C-ring)-coupled oscillator, described in Section IV, is utilized in the IL-PLL to increase fractional frequency resolution and improve delay-cell mismatches.

III. Proposed Phase-Noise-Filtering Technique

A periodic LO signal, corrupted by phase noise, experiences random fluctuations in its zero-crossing point every cycle due to the amplitude modulation-to-phase modulation conversion of device noise generated from the circuit itself. Since both thermal and flicker noise sources have a zero-mean Gaussian-distributed noise spectrum, the resulting random phase fluctuations also have a zero-mean distribution around the ideal zero crossing [13]. In this case, it should be possible to average multiple uncorrelated edges to reduce the overall phase variations.

To achieve this, a phase-noise filter (PNF), as shown in Fig. 3(a), is proposed. It consists of M cascaded phase averagers followed by a long delay line (DL) placed in feedback. Each phase-domain averaging circuit produces an output edge with a phase of $\phi_{out} = (\phi_1 + \phi_2)/2$ depending on the two input phases ϕ_1 and ϕ_2. Additionally, the DL introduces a long time difference $\Delta\tau$ between the PNF's input and output signal such that the instantaneous phase fluctuations at the inputs of each phase averager are uncorrelated. In the frequency domain, as the delay time increases, less correlation exists between lower-frequency phase-noise components. Overall, input phase fluctuations to the PNF are continuously averaged with previous time delayed fluctuations such that zero-mean phase errors are filtered out.

A. Noise Transfer Functions

Using the time and phase-domain models of an M-stage PNF, shown in Fig. 3, the steady-state behavior and phase-noise transfer functions can be examined. The initial input and output signals of the PNF are expressed as $A_i \sin[\omega t + \phi_i + \phi_{ni}(t)]$ and $A_o \sin[\omega t + \phi_o + \phi_{no}(t)]$, respectively. The static instantaneous phase shifts ϕ_i and ϕ_o are represented independently of the time-varying phase-noise components $\phi_{ni}(t)$ and $\phi_{no}(t)$. Similarly, $\phi_{ndl}(t)$ represents the DL's additive phase noise. The closed loop steady-state equation is given by

$$\omega t + \phi_o + \phi_{no}(t) = \omega\,(t + \Delta\tau) + \left(\frac{\phi_i}{2^M} + \sum_{n=1}^{M}\frac{\phi_o}{2^n}\right) + \left(\frac{\phi_{ni}(t+\Delta\tau)}{2^M} + \sum_{n=1}^{M}\frac{\phi_{no}(t+\Delta\tau)}{2^n}\right) + \phi_{ndl}(t). \quad (3)$$

Equating the signal and noise terms of (3) separately, the steady-state phase relationship can be simplified to (4), while noise transfer functions (NTFs) can be further derived from (5)

$$\phi_o = \phi_i + 2^M\omega\Delta\tau \quad (4)$$

$$\phi_{no}(t) = \left(\frac{\phi_{ni}(t+\Delta\tau)}{2^M} + \sum_{n=1}^{M}\frac{\phi_{no}(t+\Delta\tau)}{2^n}\right) + \phi_{ndl}(t). \quad (5)$$

From (4), we can see that the output phase is just a shifted version of the input phase that depends on the DL's length $\Delta\tau$ and the number of cascaded phase averagers. Additionally, since all time-dependent terms have been canceled out, the PNF's output signal is not frequency modulated and has the same frequency as the input signal. To extract the input and DL NTFs, (5) is converted to the frequency domain using the Fourier transform and $\phi_{no}(s)$ is solved in terms of either $\phi_{ndl}(s)$ or $\phi_{ni}(s)$, while the other is set to zero. The derived NTFs for the input $H_{PNF}(s)$ and DL $H_{DL}(s)$ noise contributions are given by (6) and (7), respectively. Fig. 4 plots the magnitude response of $H_{PNF}(s)$ and $H_{DL}(s)$ for a different number of phase averagers

$$H_{PNF}(s) = \frac{\phi_{no}(j\omega_m)}{\phi_{ni}(j\omega_m)} = \frac{e^{-j\omega_m\Delta\tau}}{2^M - (2^M-1)\cdot e^{-j\omega_m\Delta\tau}} \quad (6)$$

$$H_{DL}(s) = \frac{\phi_{no}(j\omega_m)}{\phi_{ndl}(j\omega_m)} = \frac{2^M}{2^M - (2^M-1)\cdot e^{-j\omega_m\Delta\tau}}. \quad (7)$$

The input-NTF exhibits a sinusoidal filtering response with maximum-attenuation notches and no-attenuation peaks occurring at odd and even multiples of $\omega_m = 1/(2\Delta\tau)$, respectively. Therefore, the attenuation band can be positioned at specific offset frequencies by adjusting the delay time $\Delta\tau$. By increasing the number of cascaded phase averagers used, the input-phase-noise attenuation can be increased from −9.5 dB for $M = 1$ to −23.5 dB for $M = 3$. Similar to the input-phase-noise, the delay-line's phase-noise

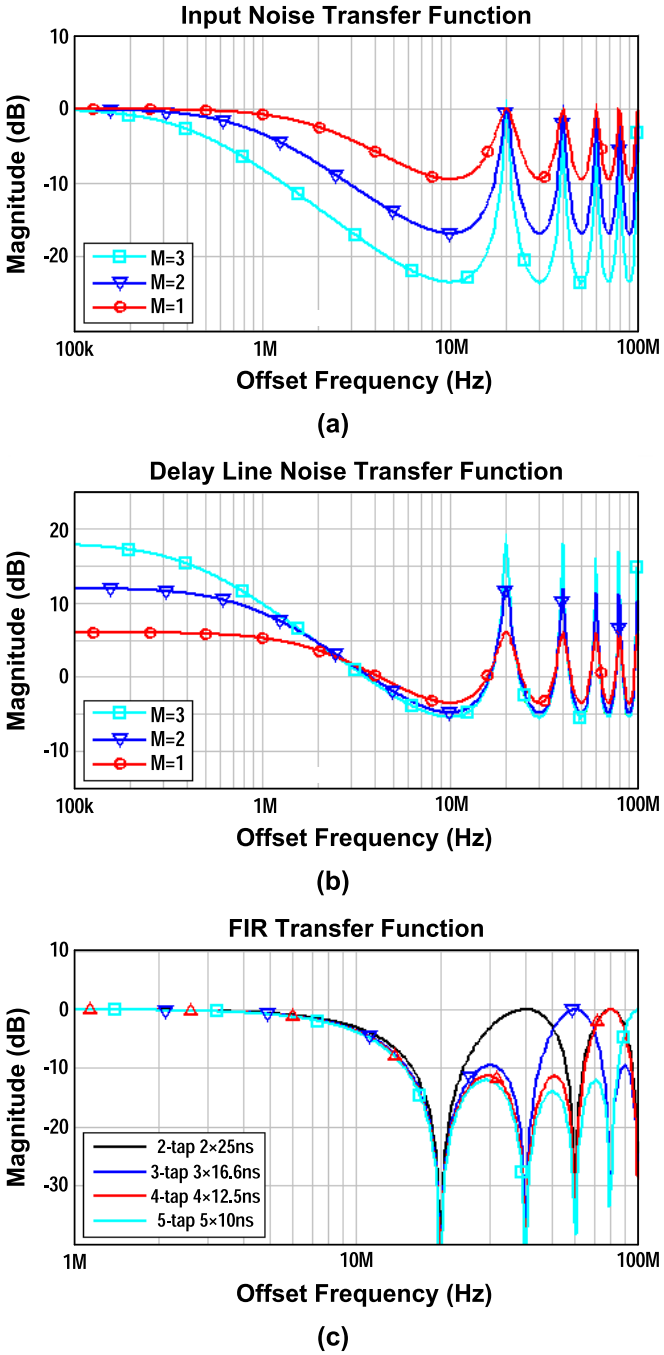


Fig. 4. Magnitude response of (a) input NTF and (b) DL NTF for M-stage PNF using a $\Delta\tau = 50$ ns. (c) FIR transfer function with $\Delta\tau = 50$ ns split into multiple taps.

contribution is also shaped by the PNF to have a sinusoidal response. Fig. 4(b) reveals that the DL's phase-noise contribution increases by 6 dB for each phase averager used at even multiples of $\omega_m = 1/(2\Delta\tau)$, including the in-band offset frequencies around ω_0. Fortunately, the phase-noise floor of a DL is typically much lower than that of a RO [14]. Overall, the trade-off between the input-phase-noise attenuation and delay-line-noise contributions limits the number of phase averagers that can be used. To remove the high-offset-frequency peaks at even multiples of ω_m in both the input and delay-line NTFs, a continuous-time finite impulse response (FIR) is created by combining k time-shifted replicas of the PNF's output signal

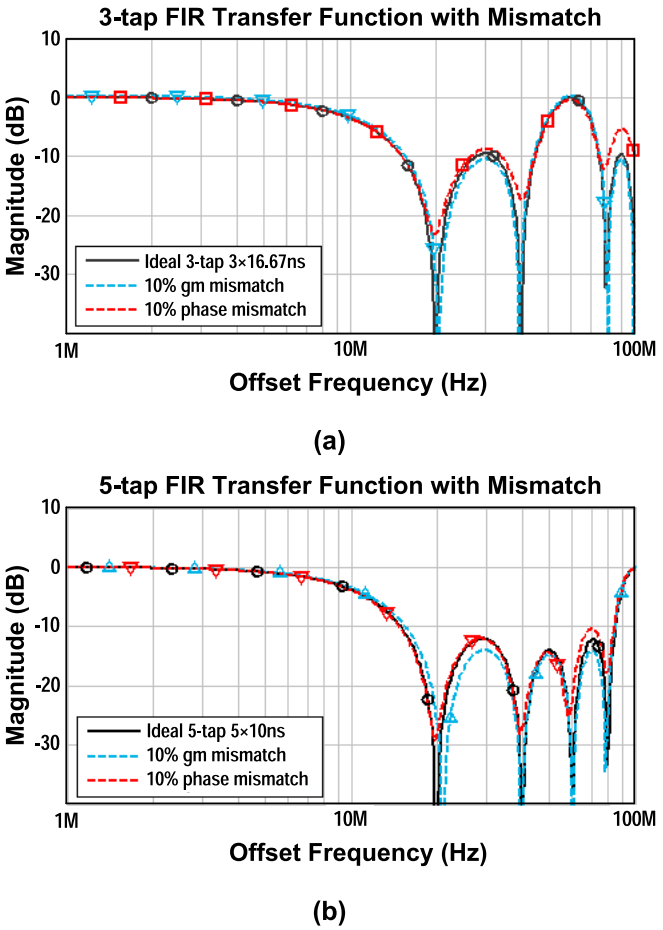


Fig. 5. Effects of gain and phase mismatch on (a) 3-tap and (b) 5-tap FIR NTFs.

from multiple taps of the delay-line. The phase-noise transfer function for a k-tap FIR is given by

$$H_{\mathrm{FIR}}(s) = \frac{\phi_{\mathrm{FIR\_no}}(j\omega_m)}{\phi_{\mathrm{FIR\_ni}}(j\omega_m)} = \frac{1}{k}\{1 + e^{-j\omega_m \Delta d\tau_1} + e^{-j\omega_m(\Delta d\tau_1 + \Delta d\tau_2)} + \cdots + e^{-j\omega_m(\Delta d\tau_1 + \cdots + \Delta d\tau_{k-1})}\}. \quad (8)$$

For equal delay time between time-shifted output signals, $\Delta d\tau_{1,2,3} = \Delta d\tau$, FIR notches and peaks will exist at fractional ($h \neq k$) and integer ($h = k$) multiples of $\omega_m = (1/(\Delta d\tau)) \cdot (h/k)|_{h=1,2\ldots(k-1)}$ respectively. By properly setting $\Delta d\tau$, the $H_{\mathrm{FIR}}(s)$ notches can be aligned to the $H_{\mathrm{PNF}}(s)$ and $H_{\mathrm{DL}}(s)$ peaks as shown in Fig. 4(c). The FIR output signals are interpolated in the current domain using a load capacitor to ensure the in-band phase noise does not degrade.

Since the PNF primarily operates in the phase domain, the NTFs are quite insensitive to amplitude mismatch and variations, especially when amplitude limited signals are used. Phase inaccuracies and mismatch, however, have a larger effect on the NTFs. In the case of $H_{\mathrm{PNF}}(s)$ and $H_{\mathrm{DL}}(s)$, a +10% delay-line variation will cause the maximum-attenuation notch frequencies to shift proportionally from 10 to 9.09 MHz when $\Delta\tau = 50$ ns is increased to $\Delta\tau = 55$ ns while the overall attenuation magnitude is unchanged. In the case of $H_{\mathrm{FIR}}(s)$, matching between adjacent delay-line segments $\Delta d\tau_{1,2,3}$ is

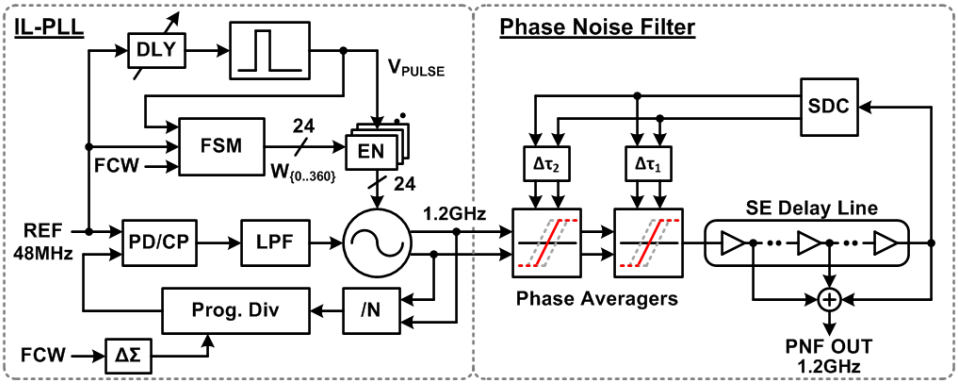


Fig. 6. Proposed inductor-less frequency synthesizer composed of a 1.2-GHz IL-PLL and 2-stage PNF.

critical as shown in Fig. 5. Even a 10% mismatch between adjacent segments, show a significant reduction in notch attenuation from $-\infty$ to finite values <-12 dB and <-17 dB for the 3-tap and 5-tap cases, respectively. Additionally, depending on the mismatch configuration, various portions of the attenuation curve between notches can vary by several decibels compared to the ideal case. To minimize delay-line mismatch between taps, it is recommended to use symmetrical delay-line segment layouts with narrow-band delay-locked loops for calibration to ensure $\Delta d\tau_1 = \Delta d\tau_2 = \Delta d\tau_3$ in the presence of process, voltage, and temperature variations. Due to the high-offset-frequency attenuation characteristic of the input-NTF, the proposed PNF can be applied to IL-PLLs to attenuate the high-frequency spurs and phase noise.

B. Stability

To analyze the stability of the PNF, the characteristic equation, given in (9), of the closed loop transfer functions is solved for their pole location(s), as given by (10)

$$2^M - (2^M - 1) \cdot e^{-j\omega_m \Delta\tau} = 0 \tag{9}$$

$$s = -\frac{1}{\Delta\tau} \ln \frac{2^M}{2^M - 1}. \tag{10}$$

Since any physically realizable delay length must be greater than or equal to zero, $\Delta\tau \geq 0$ and $\ln(2^M/(2^M - 1))$ is always positive for $M \geq 1$, the single pole in (10) is guaranteed to be negative and located in the left-half of the complex plane. This ensures the linear-time-invariant system's region of convergence includes the entire $j\omega$-axis, indicating both $H_{\text{PNF}}(s)$ and $H_{\text{DL}}(s)$ are ideally unconditionally stable. Unlike [1], a precise $\Delta\tau$ is not required as the PNF will automatically track f_{in} and converge to the steady state relation (4). In practice, however, the implementation of the phase averaging circuit does not follow the ideal behavior exactly and a 180° input phase difference to the phase-averager must be avoided as discussed further in Section IV-B.

IV. Circuit Implantation of Frequency Synthesizer

To demonstrate the phase-noise-filtering technique, an inductor-less frequency synthesizer is proposed as shown in the detailed block diagram of Fig. 6. It consists of a fractional-N IL-PLL followed by a two-stage PNF. At the core of the IL-PLL is a 24-phase inductor-less VCO operating around 1.2 GHz. A conventional fractional-N PLL composed of a phase-frequency detector, a charge pump, a third-order loop filter, static and programmable dividers and a MASH 1-1-1 $\Delta\Sigma$ modulator is used for coarse frequency alignment to a 48-MHz reference. To periodically realign the VCO's edge, a pulse generator first creates a narrow injection pulse from the reference signal before injecting it into the VCO in a specific sequence. Based on [7], a finite state machine (FSM) controls the injection pattern according to the frequency control word by toggling one of 24 enable switches per reference cycle, resulting in a fractional frequency resolution as fine as 2 MHz. A manually tuned variable DL included before the pulse generator allows the phase delay between the injection and divider paths to be matched during initial calibration in order to minimize injection spurs [15]. The PNF is composed of two cascaded phase averagers followed by a single-ended DL and a single-to-differential converter (SDC) placed in feedback. Additionally, a fine DL is included in the feedback-path to each phase averager to ensure a 180° initial-input-phase-difference case can be avoided. The synthesizer's output combines three time-shifted replica signals from multiple taps of the DL to create a FIR response at the no-attenuation peak frequencies of the PNF.

A. Injection-Locked Capacitive-Ring-Coupled Oscillator

Coupled ROs using an auxiliary non-oscillating coupling ring are known to not only increase the number of output phases available in a VCO, but to also improve delay cell matching due to phase error averaging. This makes them a natural candidate to improve the fractional resolution of IL-PLLs. As shown in Fig. 7, each delay cell produces an output current that not only flows into its own load capacitor, but also neighboring ones through the auxiliary ring. As a result, phase errors originating from any single delay cell are interpolated together with all other output phases in the auxiliary ring, where immediately adjacent cells have a larger weighting than cells farther away. For example, a 3° error in the 0-phase current vector will be coupled with adjacent 15° and 345° current components, resulting in an overall phase error of only 1.02°. While coupling multiple ROs together in this manner requires higher power consumption for the same output frequency, the phase

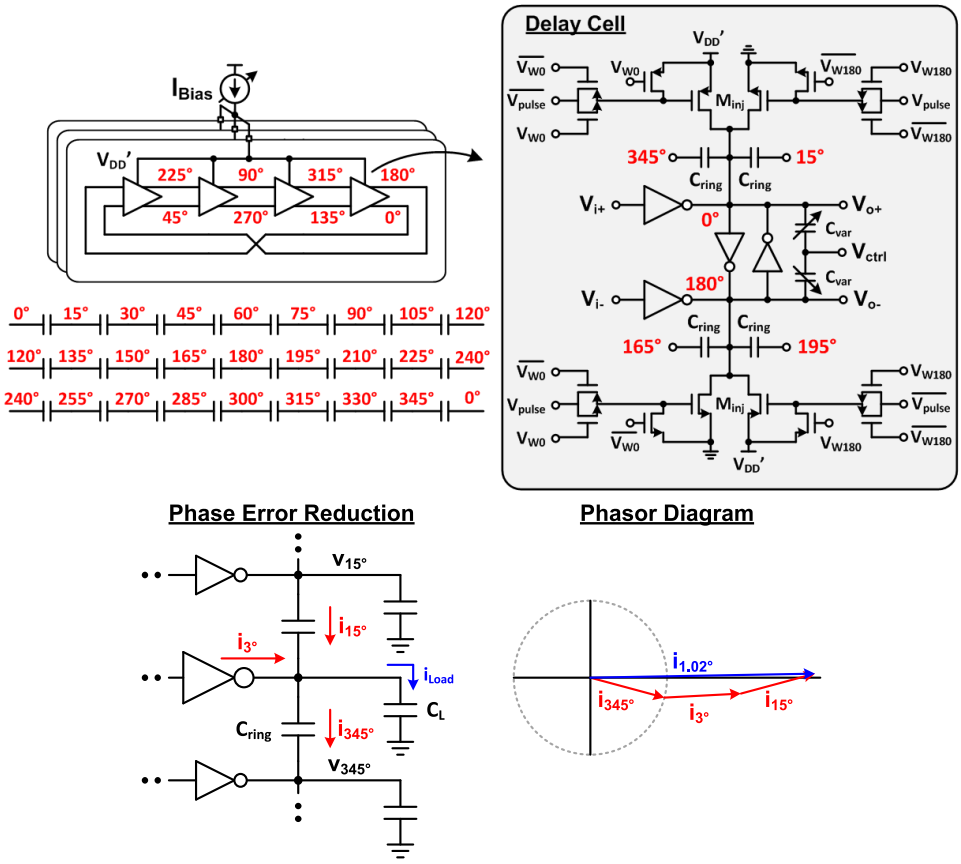


Fig. 7. Schematic of capacitive-ring-coupled oscillator. Example of phase error reduction due to delay cell mismatch with corresponding phasor diagram.

noise also improves proportionally, resulting in no change in the VCO's figure of merit (FoM) assuming the auxiliary ring is noiseless and consumes no power [16]. In practice, however, the auxiliary coupling rings in previous works, implemented using inverters [17], active phase interpolators [18], and resistors with isolation buffers [19], all introduce additional noise and require additional power. Furthermore, in cases where NMOS or PMOS coupling devices are used, the coupling ring itself is sensitive to mismatch due to its small geometry.

In this paper, a passive large-geometry C-ring is proposed to couple three 8-phase ROs together for use in a fractional-N IL-PLL, as shown in Fig. 7. The auxiliary coupling ring uses 8 μm $\times$ 8 μm MIM capacitors, which requires no active power, does not introduce thermal or flicker noise and is less sensitive to mismatch. This, however, requires a larger chip area to accommodate the twenty-four coupling capacitors and more complicated floor plan to ensure symmetrical routing. The primary disadvantage of stand-alone capacitive-coupled oscillators is the existence of multiple modes of oscillation and an undefined phase sequence caused by the bi-directional nature of coupling networks. Therefore, capacitive-coupled oscillators have not been adopted in traditional PLLs. Fortunately, when used in an IL-PLL, the periodic injection pattern defines the VCO's stable mode of oscillation with a reliable output phase sequence comparable to that of a persistent startup circuit. Additionally, since the capacitive ring introduces a finite non-zero phase shift between each coupled RO, both the in-phase oscillation and dc non-oscillatory modes are eliminated [16]. Each delay cell in the RO uses a differential inverter topology with complementary injection devices M_{inj}, which allow for both pull-up and pull-down edge re-timing. A transmission gate separating the reference injection pulse V_{pulse} from the gate of each injection device must be enabled by the FSM for injection to occur. To control the phase sequence of injection, every reference cycle, the FSM generates a set of windowing signals $\{V_{W0} : V_{W345}\}$ that enables specific transmission gates separating V_{pulse} from the gates of each injection device. Additional shunting devices ensure the disabled phases of M_{inj} are biased in cut off. The NMOS sizing of the injection devices M_{inj} is 9.6 μm/60 nm compared to that of the self-oscillating and cross-coupled devices of 7.2 μm/60 nm and 3.6 μm/60 nm, respectively. Since the injection device is not significantly stronger than the self-oscillating and cross-coupled devices, only partial edge-realignment of $\beta \approx 0.4$ is achieved, resulting in a narrower ILBW than the maximum $0.5 f_{\text{REF}}$ possible with $\beta = 1$. To ensure $\beta \approx 1$ for a wide ILBW, [3] suggests an injection-to-self-oscillating sizing ratio of at least five times.

B. Phase Domain Averager

Given two input signals V_{in1} and V_{in2} with instantaneous phases ϕ_1 and ϕ_2, respectively, the phase domain averager (PDA) must produce an output signal V_{out} with an average phase of $\phi_{\text{out}} = (\phi_1 + \phi_2)/2$ with a large enough output amplitude to properly trigger the subsequent differential inverter used to recover the rail-to-rail voltage swing.

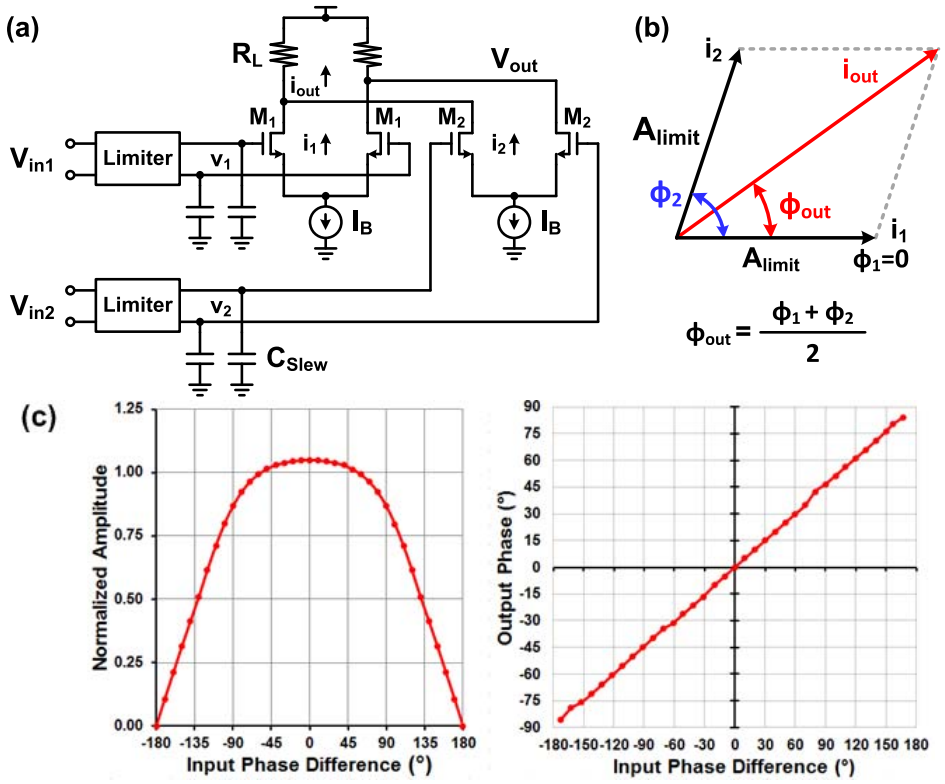


Fig. 8. Phase domain averager (a) schematic and (b) phasor diagram with simulated amplitude and phase characteristics of phase interpolator.

As shown in Fig. 8(a), the phase averager is composed of two amplitude limiters, a slewing capacitor, and a phase interpolator. The input amplitude limiters, implemented using differential inverters, remove all amplitude variations from V_{in1} and V_{in2} due to noise or previous stage mismatches and ensure they have equal amplitudes. The sharp edges of the resulting square wave signals are converted to a triangular waveform using capacitor C_{slew} to ensure their ramped edges overlap with each other when interpolated together in the current domain. As shown in the phasor diagram of Fig. 8(b), the current i_1 is combined in a vector sum with current i_2 to generate an output current i_{out}, which has an average of the two input phases. The simulated normalized output amplitude and output phase response of the phase interpolator is shown in Fig. 8(c) as the input phase difference is changed from $-180°$ to $+180°$. Throughout the entire range, the output phase shift is approximately half of the input phase difference, as required. On the other hand, the output amplitude drops significantly for input phase differences near $\pm 180°$ as i_1 and i_2 partially cancel each other out. As a result, it is critical to avoid an input phase difference close to $\pm 180°$ or else the output signal may be too small to properly trigger the subsequent inverters. To avoid this, as previously mentioned, this paper uses manually tuned variable DLs to calibrate the initial input phase difference to each phase averager. In future work, automatic calibration could be implemented by placing a delay-locked loop [20] around the feedback DL such that the overall delay is an integer multiple of the reference period corresponding to the input phase differences around 0°. A $\pm 10\%$ gain mismatch between interpolation devices M_1 and M_2 slightly alters the phase averager's division modulus between 1.89 and 2.12 resulting in a maximum attenuation variation of less than ± 0.75 dB from the ideal -16.9 dB attenuation in the 2-stage $H_{\text{PNF}}(s)$.

C. Coarse Delay Line

To save power, a single-ended inverter-based DL is utilized in the otherwise differential PNF. Since the input attenuation notch occurs at $\omega_m = 1/(2\Delta\tau)$, it is desirable to increase the DL's $\Delta\tau$ to position the notch at a lower offset frequency for a lower integrated jitter at the expense of delay-line power. Alternatively, if the goal is to maximize injection spur attenuation at f_{REF} or spot-phase noise at a specific offset frequency, $\Delta\tau$ can be adjusted to position a notch accordingly. In this design, a long delay time of 50 ns is used to demonstrate phase-noise attenuation starting at 1 MHz and reaching a maximum at 10-MHz offset. The delay cells are designed with long channel lengths of 180-nm operating with a low V_{DD} of 0.85 V to both reduce the number of delay cells required and also to minimize flicker-noise contributions. While it would be possible to significantly increase the DL's $\Delta\tau$ by further reducing the supply voltage, its phase-noise contribution would rise proportionally [14]. Since the DL's high-frequency phase noise is filtered by both the PNF and FIR, it is the close-in phase-noise contribution that dominates the overall system noise contribution. To ensure a minimal noise contribution in the synthesizer's overall in-band phase noise, the DL's noise should remain at least 3 dB lower than the IL-PLL's in-band phase noise. Accounting for the 2-stage PNF's 12 dB degradation due to the DL NTF and 10-dB flicker noise slope,

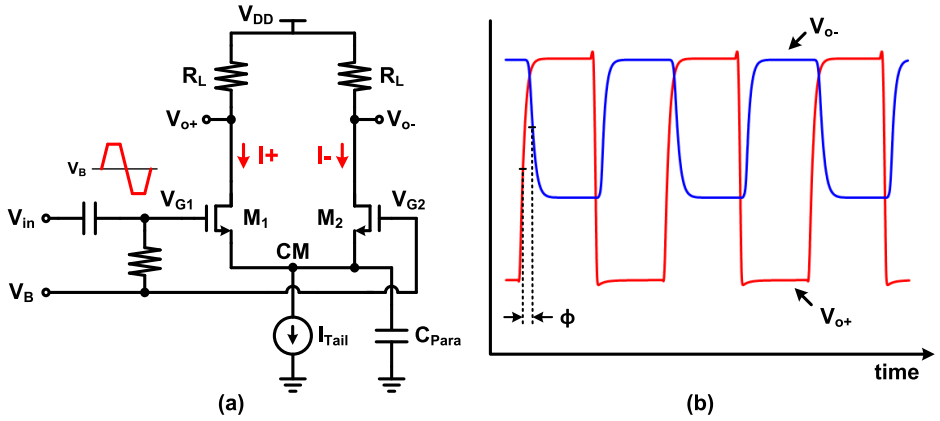


Fig. 9. (a) Conventional SDC pseudo-differential pair. (b) Transient output waveform showing dc offset, amplitude mismatch, and phase error.

as well as the ∼1 MHz 1/f noise corner of the inverters, the DL's noise floor is designed for −130 dB/Hz at 1 MHz for a close-in phase-noise contribution of −108 dBc/Hz at 100 kHz. To tune the FIR notch locations, the DL is designed with binary weighted switches that allow sections of the DL to be bypassed and disabled when not in use. One of the main drawbacks of using a single-ended DL is duty cycle errors caused by uneven PMOS and NMOS pull-up and pull-down strengths. To address this, body biasing has been included for both the PMOS and NMOS transistors within the DL so that the threshold voltages V_{TN} and V_{TP} can be adjusted. Additionally, single-ended DLs are quite sensitive to supply noise so a low noise supply regulator is required.

D. Single-to-Differential Converter

To recover a differential signal from the single-ended DL, a large-signal balanced SDC is required. Conventional SDCs employing a pseudo-differential pair structure, as shown in Fig. 9, are commonly used for small-signal inputs. By keeping the gate bias of M_1 and M_2 equal to V_B, the dc tail current I_{Tail} is equally split between $I+$ and $I-$, resulting in balanced dc output voltages on v_o+ and v_o-. When excited with a small-signal input, the output current is steered between the $I+$ and $I-$ branches, resulting in a differential output signal while both M_1 and M_2 remain in saturation. Asymmetry in the differential output signals is mainly due to the finite impedance and capacitance of the tail node CM that must be charged as the current is steered from $I+$ to $I-$, resulting in a phase shift and signal loss in v_o- compared to v_o+. Additionally, when driven by a large rail-to-rail signal, such as that from the DL's output, the tail current is not symmetrically steered between the two output branches, resulting in a large dc operating point error. During the first half cycle when $V_{G1} = V_{\text{DD}}$ and $V_{G2} = V_B$, both M_1 and M_2 are biased in saturation mode and the tail current is split between both the $I+$ and $I-$ branches according to the R_{ON} ratio of M_1 and M_2. However, during the other half-cycle, when $V_{G1} = V_{\text{SS}}$ and $V_{G2} = V_B$, M_2 stays in saturation mode, while M_1 is cut off. In this case, the tail current flows entirely to the $I-$ branch, resulting in $v_o+ = V_{\text{DD}}$ and $v_o- = V_{\text{DD}} - I_{\text{Tail}}R_L$. As a result, the output waveform, plotted in Fig. 9(b), exhibits both amplitude and phase errors in its differential output signals.

A large-signal balanced SDC, shown in Fig. 10, is proposed and utilized in the PNF. Taking advantage of the highly uniform delay $\Delta\phi$ between adjacent inverters, three single-ended signals from the DL, $v_{1,2,3}$, are interpolated together to create an accurate differential output. This is achieved by first converting the square-wave signals to triangular waves $v'_{1,2,3}$ using the slewing capacitor C_{slew} such that the rising and falling edges of v_1 and v_3 overlap with each other. Since v_2 must drive two slewing stages, two dummy stages are provided to v_1 and v_3 to ensure equal loading of the delay-line inverters. The subsequent phase interpolator then creates both v_o+ and v_o- by interpolating v'_1 with v'_3 and, similarly, v'_2 with itself, as illustrated in the phasor diagram of Fig. 10. While this method results in a slight output amplitude mismatch between v_o+ and v_o-, this will be removed by the subsequent ac-coupled amplitude limiters of the phase averagers.

E. Estimated Synthesizer-Phase-Noise Contributions

The theoretical phase-noise contribution of the overall frequency synthesizer, based on the derived NTFs applied to post-layout VCO and DL simulation results, is shown in Fig. 11 with $f_{\text{REF}} = 48$ MHz and a DL length of 50 ns. The free-running VCO, with phase noise of −115 dBc/Hz at 10-MHz offset while consuming 2.04 mW, has its close-in phase noise suppressed by the IL-PLL below an ILBW ≈ 15 MHz. Applying a 2-stage PNF, the high-frequency phase noise above 1 MHz is attenuated by up to 20 dB at 10-MHz offset. Finally, the PNF's no-attenuation peaks are then further suppressed by the 3-tap FIR, with notches located at 20 and 40 MHz, resulting in high-frequency phase noise of −135 dB and −143 dBc at 10- and 30-MHz offsets, respectively. Overall, the IL-PLL consumes 3.73 mW, while the PNF consumes 15.85 mW, of which 13.6 mW is from the DL, to achieve 50 ns delay with a phase-noise floor of −130 dBc/Hz. To assess the effectiveness of the proposed PNF technique, we can use the VCO's FoM, given by (11) which describes the phase-noise versus power trade-off of stand-alone oscillators. For the RO

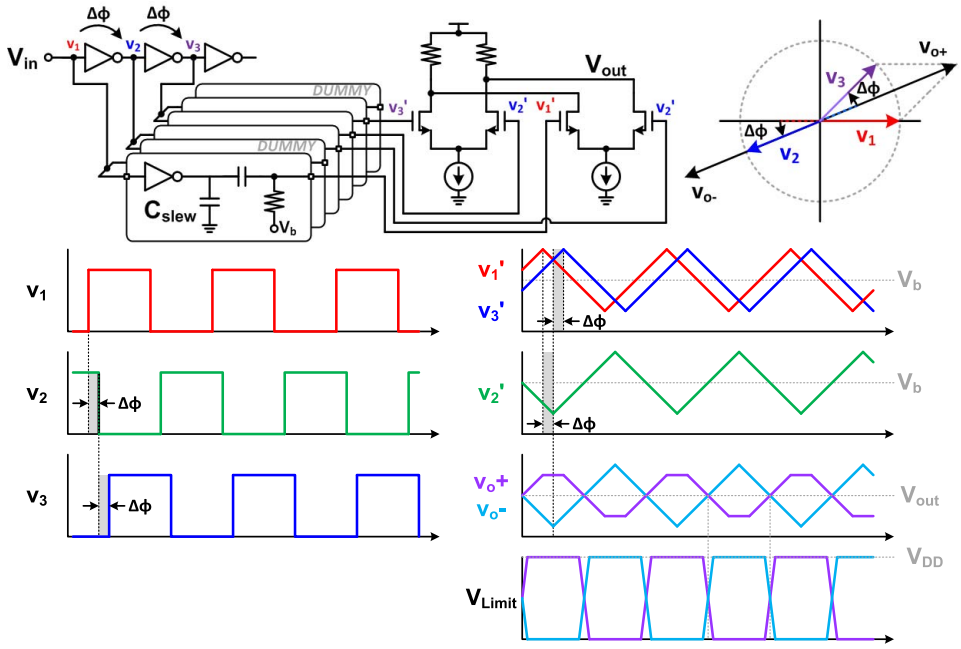


Fig. 10. Schematic of proposed interpolator-based SDC with phasor diagram and transient waveform.

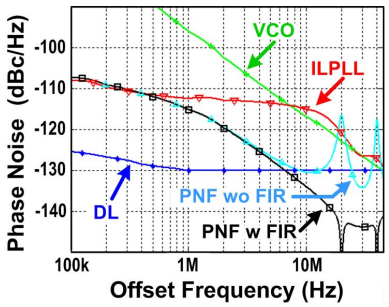


Fig. 11. Frequency synthesizer's overall phase-noise contribution.

to achieve a 20-dB reduction in phase noise, it must increase its power consumption by 100 times, resulting in a power of approximately 200 mW. In contrast, the PNF provides the same 20-dB high-frequency phase-noise suppression for only 15.85 mW, with the additional ability to suppress spurious tones. Alternatively, if the power consumed in the PNF were to be spent in the RO instead, the resulting phase noise improvement would be only 7.28 dB. For applications that target injection-spur reduction without the need for phase-noise filtering, the PNF's maximum-attenuation notch can be positioned at higher offset frequencies than the 10-MHz offset targeted in this paper. This would significantly lower the delay-line power consumption, chip area, and delay-line phase noise contribution

$$\text{FoM} = L\{\Delta\omega\} - 20\log_{10}(\omega_0/\omega_m) + 10\log_{10}(P_{\text{DC[mw]}}). \quad (11)$$

V. Measurement Results

The proposed synthesizer is fabricated in a 65-nm CMOS process and occupies a core area of 800 μm $\times$ 750 μm.

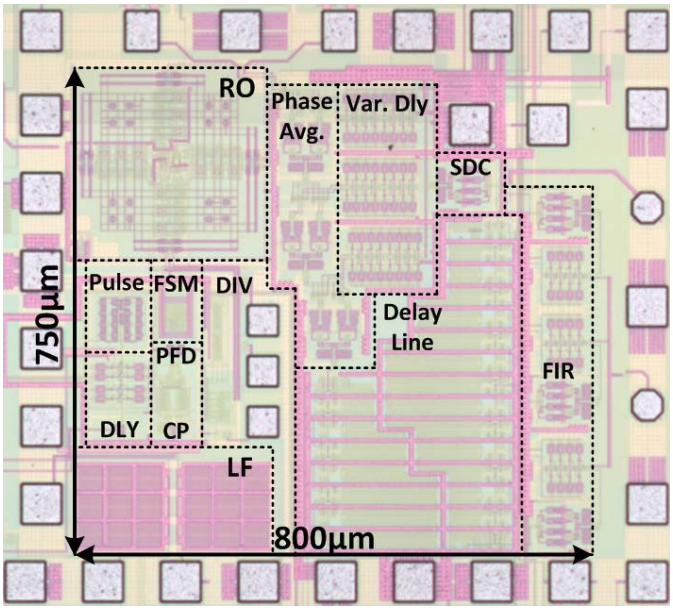


Fig. 12. Die photo of prototype inductor-less frequency synthesizer implemented in 65-nm CMOS.

The die micrograph is shown in Fig. 12. Using a 48-MHz reference, the IL-PLL achieves a fractional resolution of 2 MHz, as shown in Fig. 13. Fig. 14 measures NTFs using an external LO signal. Both the input and DL NTF closely match the derived theoretical equations (6) and (7). Fig. 15(a) shows the measured output spectrum and phase noise performance at 1.152 GHz with and without the PNF while using a 48-MHz reference. The 2-stage PNF's attenuation can be observed starting at 1-MHz offset and increasing up to 20 dB at 10-MHz offset, which closely matches the theoretical attenuation. Without the PNF, the IL-PLL achieves a phase noise

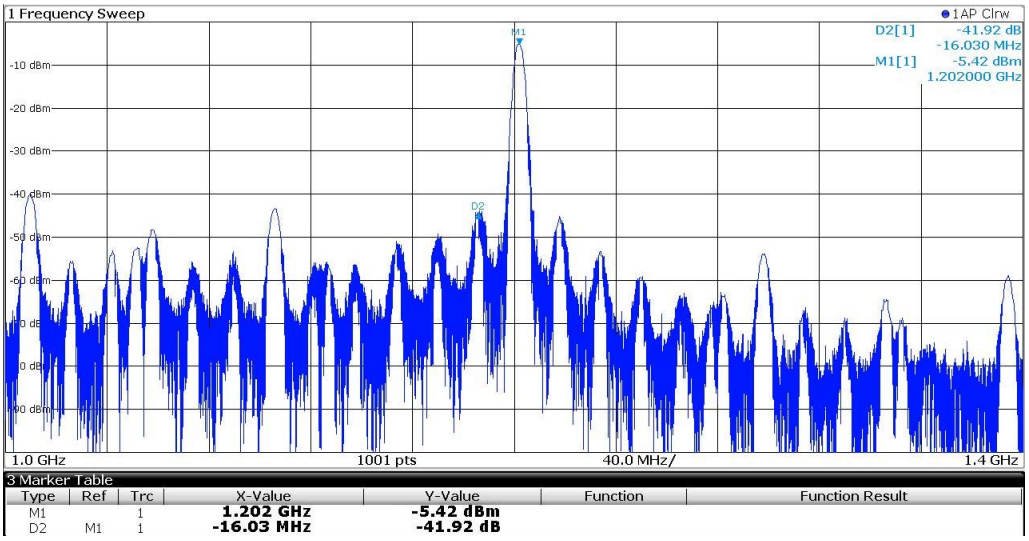


Fig. 13. Output spectrum of IL-PLL locked to 1.202 GHz using a 48-MHz reference injection, with fractional division ratio of $25 + 1/24$ representing a 2-MHz frequency resolution.

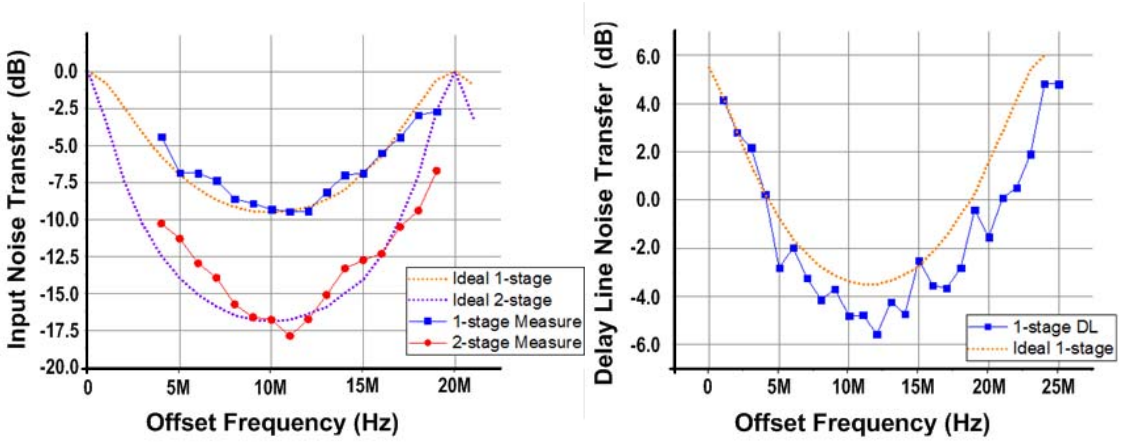


Fig. 14. Measured input and delay line noise transfer functions.

of −98.4 dBc/Hz at 100 kHz and −115 dBc/Hz at 10-MHz offset with an injection spur of −40.5 dBc at 48 MHz. With the 2-stage PNF and FIR enabled, the close-in 100-kHz phase noise remains at −98.4 dBc/Hz, while the 10-MHz phase noise and spurs are reduced to −134.8 dBc/Hz and −57 dBc, respectively. The integrated jitter from 100 kHz to 100 MHz, including the reference spur, is reduced from 3.57 to 1.48 ps while consuming 19.8 mW, resulting in an FoM and $\text{FoM}_{\text{Jitter}}$ of −163 and −223.6 dB, respectively. The degraded in-band phase noise compared to Fig. 11 is due to the only partial rather than complete edge re-timing caused by an insufficiently large injection device size and shared common current tail, similar to [3], resulting in a narrower IL-BW and degradation of the $\text{FoM}_{\text{Jitter}}$. For comparison, the reference frequency is raised from 48 to 96 MHz to observe the phase-noise shaping with a wider ILBW, as originally intended. Fig. 15(b) shows both the measured spectrum and phase-noise plots using a 96-MHz reference. The IL-PLL's close-in phase noise is improved by about 5 dB to −114.6 dBc/Hz at 1 MHz, while the out-band phase noise shows similar attenuation characteristics. This causes the delay-line flicker noise contribution, shaped by the 2-stage DL-NTF, to become dominant below ∼500 kHz. Overall, the integrated jitter is further reduced to 0.98 ps with a reference spur of −62.6 dB. Starting around 1-MHz offset, the phase-noise attenuation gradually increases up to ∼20 dB at 10- and 30-MHz offsets resulting in phase noise of −136.41 and −143.15 dB, respectively. Table I summarizes the performance compared to other recent inductor-less IL-PLLs. Thanks to the proposed phase-noise-filtering technique, this work is able to achieve much lower high-frequency phase noise performance as low as −144.5 dBc at 30-MHz offset while maintaining the IL-PLL's close-in noise suppression, resulting in an excellent FoM. To satisfy the spur requirements of more stringent wireless standards, additional techniques such as self-aligned injection timing [6] may be adopted within the inductor-less synthesizer's IL-PLL.

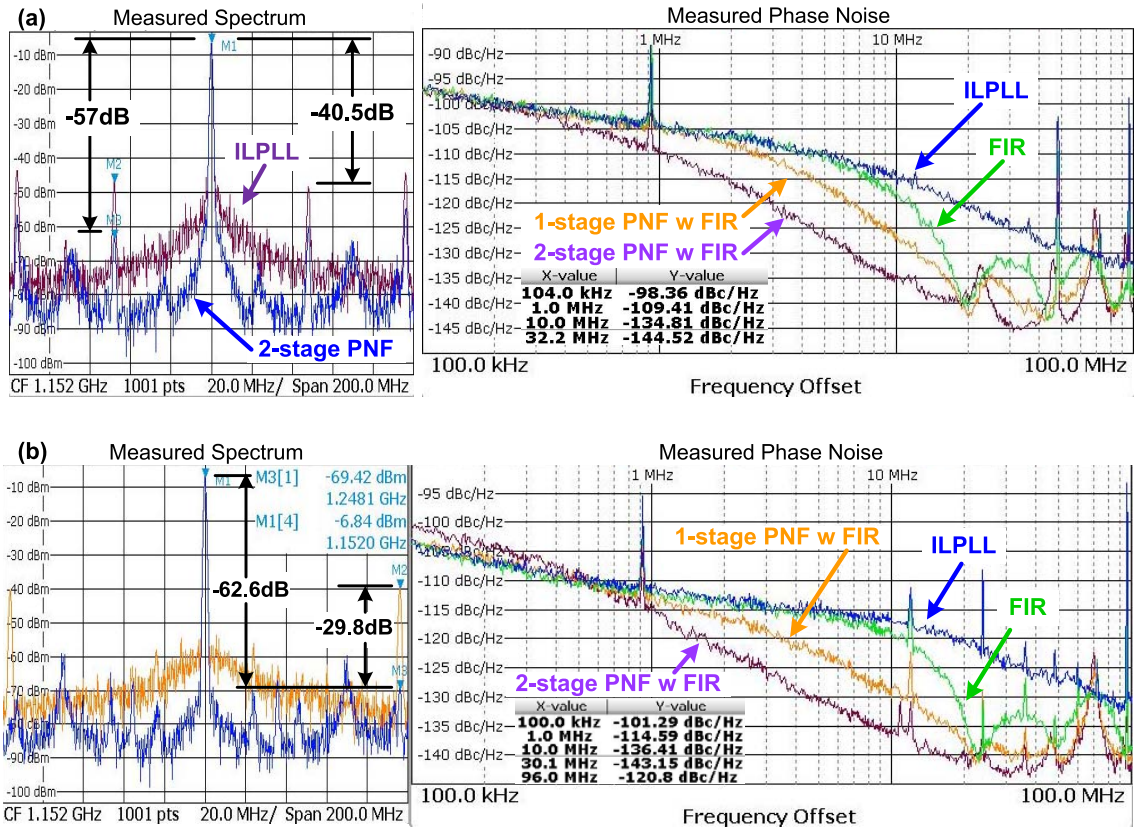


Fig. 15. Measured output spectrum and phase noise with and without PNF enabled, using (a) 48-MHz reference and (b) 96-MHz reference.

TABLE I

PERFORMANCE SUMMARY AND COMPARISON TO OTHER INDUCTOR-LESS PLLS

		This Work	C. F. Liang 2011 [6]	P Park 2012 [7]	W. Deng 2015 [12]	G. Marucci 2014 [10]	S. Min 2013 [1]
Architecture		IL-PLL + PNF	IL-PLL	IL-PLL	Soft IL-PLL	MDLL	RO + PN cancellation
Process		65nm	55nm	65nm	65nm	65nm	90nm
Vdd (V)		0.85	1.2 / 3.3	n/a	0.8	n/a	1.2
Power (mW)		19.8	6.9	10.5	3	3	29.64
Freq (GHz)		1.2	0.216	0.58	1.522	1.651	5
f_{REF} (MHz)		24	27	32	380	50	10
f_{RES} (MHz)		2	27	1	∞	0.19 kHz	10
N		24	8	18.125	4	32	512
Spur (dBc)		-57	-70.7	n/a	-63	-47	-62.5
Jitter (ps)		1.48 100k-100M	2.4 1k-40M	4.23 100-40M	3.6 100k-100M	1.395 30k-30M	3.8 10k-10M
Phase Noise (dBc/Hz)	1MHz	-109.4	-122.78	-113.5	-115	-116.69	-105
	10MHz	-134.81	-128.03	-133	-128	-114.96	-120
	30MHz	-144.52	n/a	n/a	-133	-117.65	n/a
FoM (dB)		-163.06 @10MHz	-146.33 @10MHz	-158.057 @10MHz	-166.88 @10MHz	-154.544 @10MHz	-164.26 @1MHz
FoM_{Jitter} (dB)		-223.62	-224	-217.26	-224.2	-232	-210.96
Area (mm^2)		0.6	0.03	0.158	0.048	0.4	0.122

$FoM = \mathcal{L}\{\Delta\omega\} - 20\log(\omega_0/\Delta\omega) + 10\log(P_{DC[mW]})$ $FoM_{Jitter} = 20\log(\sigma) + 10\log(P_{DC[mw]})$

While [12] also achieves an excellent FoM, this is mainly due to the unreasonably high $f_{REF} = 380$ MHz used, which results in the phase-noise performance mainly being determined by the quality of the external reference signal.

VI. CONCLUSION

A phase-domain-filtering technique has been proposed to reduce the high-frequency phase noise and large injection spurs introduced by injection-locking in an inductor-less

fractional-N IL-PLL. The theoretical phase-noise transfer functions, stability, and steady-state conditions have been developed for the general M-stage PNF. To save DL power, a large-signal SDC based on phase interpolation is also proposed allowing the use of a single-ended DL. Furthermore, a C-ring-coupled oscillator works in conjunction with the fractional injection to both improve the delay cell matching without relying on noisy resistors or active device coupling and to eliminate the uncertain modes of oscillation existing in stand-alone bi-directional-coupled oscillators. Implemented in 65-nm CMOS, the measured results are in close agreement with the theoretical model and demonstrate up to 20 dB phase noise attenuation resulting in a high-performance inductor-less IL-PLL.

REFERENCES

[1] S. Min, T. Copani, S. Kiaei, and B. Bakkaloglu, "A 90-nm CMOS 5-GHz ring-oscillator PLL with delay-discriminator-based active phase-noise cancellation," *IEEE J. Solid-State Circuits*, vol. 48, no. 5, pp. 1151–1160, May 2013.

[2] M. Mikhemar, D. Murphy, A. Mirzaei, and H. Darabi, "A cancellation technique for reciprocal-mixing caused by phase noise and spurs," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3080–3089, Dec. 2013.

[3] S. Ye, L. Jansson, and I. Galton, "A multiple-crystal interface PLL with VCO realignment to reduce phase noise," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1795–1803, Dec. 2002.

[4] M.-J. E. Lee *et al.*, "Jitter transfer characteristics of delay-locked loops—Theories and design techniques," *IEEE J. Solid-State Circuits*, vol. 38, no. 4, pp. 614–621, Jun. 2003.

[5] B. M. Helal, M. Z. Straayer, G.-Y. Wei, and M. H. Perrott, "A highly digital MDLL-based clock multiplier that leverages a self-scrambling time-to-digital converter to achieve subpicosecond jitter performance," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 855–863, Apr. 2008.

[6] C.-F. Liang and K.-J. Hsiao, "An injection-locked ring PLL with self-aligned injection window," in *ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 90–92.

[7] P. Park, J. Park, H. Park, and S. Cho, "An all-digital clock generator using a fractionally injection-locked oscillator in 65 nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 336–337.

[8] A. Elshazly, R. Inti, B. Young, and P. K. Hanumolu, "Clock multiplication techniques using digital multiplying delay-locked loops," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1416–1428, Jun. 2013.

[9] J.-C. Chien *et al.*, "A pulse-position-modulation phase-noise-reduction technique for a 2-to-16 GHz injection-locked ring oscillator in 20 nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 52–53.

[10] G. Marucci, A. Fenaroli, G. Marzin, S. Levantino, C. Samori, and A. L. Lacaita, "A 1.7 GHz MDLL-based fractional-N frequency synthesizer with 1.4 ps RMS integrated jitter and 3 mW power using a 1b TDC," in *ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 360–362.

[11] S. Levantino, G. Marucci, G. Marzin, A. Fenaroli, C. Samori, and A. L. Lacaita, "A 1.7 GHz fractional-N frequency synthesizer based on a multiplying delay-locked loop," *IEEE J. Solid-State Circuits*, vol. 50, no. 11, pp. 2678–2691, Nov. 2015.

[12] W. Deng *et al.*, "A 0.048 mm^2 3 mW synthesizable fractional-N PLL with a soft injection-locking technique," in *ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 252–254.

[13] A. A. Abidi, "Phase noise and jitter in CMOS ring oscillators," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1803–1816, Aug. 2006.

[14] A. Homayoun and B. Razavi, "Relation between delay line phase noise and ring oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 49, no. 2, pp. 384–391, Feb. 2014.

[15] J. Lee and H. Wang, "Study of subharmonically injection-locked PLLs," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1539–1553, May 2009.

[16] G. Li and E. Afshari, "A low-phase-noise multi-phase oscillator based on left-handed LC-ring," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1822–1833, Sep. 2010.

[17] A. Matsumoto, S. Sakiyama, Y. Tokunaga, T. Morie, and S. Dosho, "A design method and developments of a low-power and high-resolution multiphase generation system," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 831–843, Apr. 2008.

[18] W. Deng *et al.*, "A fully synthesizable all-digital PLL with interpolative phase coupled oscillator, current-output DAC, and fine-resolution digital varactor using gated edge injection technique," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 68–80, Jan. 2015.

[19] J.-M. Chou, Y.-T. Hsieh, and J.-T. Wu, "Phase averaging and interpolation using resistor strings or resistor rings for multi-phase clock generation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 5, pp. 984–991, May 2006.

[20] S. H.-L. Tu, D.-L. Shen, and R.-J. Yang, *Analog Circuit Design for Communication SOC*. Sharjah, United Arab Emerates: Bentham Science Publishers, 2012, ch. 5.

[21] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, Sep. 2004.

[22] R. Adler, "A study of locking phenomena in oscillators," *Proc. IEEE*, vol. 61, no. 10, pp. 1380–1385, Oct. 1973.

[23] L. Kong and B. Razavi, "A 2.4 GHz 4 mW integer-N inductorless RF synthesizer," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 626–635, Mar. 2016.

[24] L. Kong and B. Razavi, "A 2.4-GHz 6.4-mW fractional-N inductorless RF synthesizer," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2016, pp. 1–2.

[25] A. Li, Y. Chao, X. Chen, L. Wu, and H. C. Luong, "An inductor-less fractional-N injection-locked PLL with a spur-and-phase-noise filtering technique," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2016, pp. 1–2.

[26] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 790–804, Jun. 1999.

[27] X. J. Wang and T. Kwasniewski, "A compensation way for a differential pair to achieve a high performance single-ended to differential converter," in *Proc. IEEE Can. Conf. Elect. Comput. Eng.*, Apr. 2007, pp. 1137–1140.

[28] R. Farjad-Rad *et al.*, "A 0.2–2 GHz 12 mW multiplying DLL for low-jitter clock synthesis in highly-integrated data communication chips," in *ISSCC Dig. Tech. Papers*, Feb. 2002, pp. 56–57.

[29] S. L. J. Gierkink, "Low-spur, low-phase-noise clock multiplier based on a combination of PLL and recirculating DLL with dual-pulse ring oscillator and self-correcting charge pump," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2967–2976, Dec. 2008.

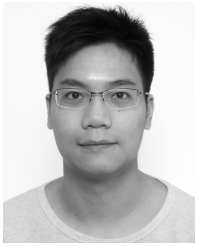
[30] Y. C. Huang and S. I. Liu, "A 2.4-GHz subharmonically injection-locked PLL with self-calibrated injection timing," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 417–428, Feb. 2013.

[31] A. Li, S. Zheng, J. Yin, X. Luo, and H. C. Luong, "A 21–48 GHz subharmonic injection-locked fractional-N frequency synthesizer for multiband point-to-point backhaul communications," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1785–1799, Aug. 2014.

[32] E. Monaco, M. Pozzoni, F. Svelto, and A. Mazzanti, "Injection-locked CMOS frequency doublers for μ-wave and mm-wave applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1565–1574, Aug. 2010.

[33] S. Kundu, B. Kim, and C. H. Kim, "A 0.2-to-1.45 GHz subsampling fractional-N all-digital MDLL with zero-offset aperture PD-based spur cancellation and *in-situ* timing mismatch detection," in *ISSCC Dig. Tech. Papers*, Jan./Feb. 2016, pp. 326–327.

[34] P. Park, D. Park, and S. Cho, "A 2.4 GHz fractional-N frequency synthesizer with high-OSR $\Delta\Sigma$ modulator and nested PLL," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2433–2443, Oct. 2012.



Alvin Li received the B.Eng. degree in engineering physics from McMaster University, Hamilton, ON, Canada, in 2007, and the M.Sc. and Ph.D. degrees in electronic and computer engineering from The Hong Kong University of Science and Technology, Hong Kong, in 2009 and 2017, respectively.

His current research interests include RF and millimeter-wave integrated circuit design for wireless communications and frequency synthesis for high-speed clocking.

Yue Chao received the B.Sc. degree in microelectronics from Shanghai Jiaotong University, Shanghai, China, and the Ph.D. degree from The Hong Kong University of Science and Technology, Hong Kong, in 2015.

Since 2016, he has been with Qualcomm Inc., San Diego, California, USA, where he was involved in RF transceivers. His current research interests include RF/mm-wave IC design.

Xuan Chen received the B.E. degree from South China Normal University, Guangzhou, China, in 2013, and the M.Sc. degree from The Hong Kong University of Science and Technology (HKUST), Hong Kong, in 2014.

From 2014 to 2016, he was a Research Assistant with the Wireless Communications Integrated Circuits Lab, HKUST. Since 2016, he has been with Goodix Ltd., Shenzhen, Guangdong, China, where he was involved in power management circuits. His current research interests include CMOS RF power amplifiers and designed an envelope-shaping-and-tracking-mode-switching local thermal equilibrium power amplifier, RF and millimeter-wave integrated transmitter for wireless communications.

Liang Wu (M'12) received the B.S. and M.S. degrees in materials science from Fudan University, Shanghai, China, in 2004 and 2007, respectively, and the Ph.D. degree in electronic and computer engineering from The Hong Kong University of Science and Technology, Hong Kong, in 2012.

In 2013, he joined the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, as a Research Assistant Professor. Since 2015, he has been with the State Key Laboratory of Millimeter Waves, City University of Hong Kong, as a Senior Research Fellow. His current research interests include CMOS RF/millimeter-wave integrated circuits, phased-array for 60 GHz wireless communications, and visible light communication systems.

Howard C. Luong (F'14) received the B.S., M.S., and Ph.D. degrees in electrical engineering and computer sciences from the University of California, Berkeley, CA, USA, in 1988, 1990, and 1994, respectively.

Since 1994, he has been the EEE Faculty Member with The Hong Kong University of Science and Technology, Hong Kong, where he is currently a Professor. He has co-authored three technical books entitled *Design Techniques for Transformer-Based VCOs and Frequency Dividers*, *Low-Voltage RF CMOS Frequency Synthesizers*, and *Design of Low-Voltage CMOS Switched-Opamp Switched-Capacitor Systems*. His current research interests include RF and analog integrated circuits and systems for wireless and portable applications.

Prof. Luong is currently serving as a Technical Program Committee Member of the IEEE International Solid-State Circuits Conference and an Associate Editor of the IEEE VIRTUAL JOURNAL ON RFIC. He was an IEEE Solid-State Circuits Society Distinguished Lecturer and an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I and II.