

A Dual-Imaging Speed-Enhanced CMOS Image Sensor for Real-Time Edge Image Extraction

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Abstract—This paper presents a CMOS image sensor (CIS) that extracts a multi-level edge image as well as a human-friendly normal image in a real time from conventional pixels for machine-vision applications, utilizing a proposed speed/power-efficient dual-mode successive-approximation register analog-to-digital converter (SAR ADC). The proposed readout scheme operates in two modes, fine step SAR (FS-SAR) mode and coarse-step single-slope (CS-SS) mode, depending on the difference (Δ) between a chosen pixel and the previous pixel. If a chosen pixel is at a boundary of an object with a large Δ from the previous pixel, the readout ADC works in the CS-SS mode to readout the edge strength (ES), while the FS-SAR mode is applied for other pixels. By displaying the ES, a multi-level edge image can be obtained in a real time along with a normal image with no hardware/time overhead. By saving the MSBs conversion cycles regardless of Δ , the proposed dual-mode readout scheme enhances the readout speed and reduces power consumption. A prototype QQVGA CIS with 10-bit SAR ADCs was fabricated in a 0.18- μm 1P4M CMOS image sensor process with a 4.9- μm pixel pitch. With a maximum pixel rate of 61.4 Mp/s, the prototype demonstrated figure of merits of 70 pJ/pixel/frame, 0.35 e⁻ · nJ, and 0.34 e⁻ · pJ/step.

Index Terms—CMOS image sensor (CIS), delta (Δ), dual-mode readout scheme, multi-column-parallel (MCP), multi-level edge image, real-time edge image, successive-approximation register analog-to-digital converter (SAR ADC).

I. INTRODUCTION

THE markets for high-performance CMOS image sensors (CISs) have grown significantly in recent years. At the same time, the performance requirements of the next-generation CISs have been expanding in terms of frame rate, noise, dynamic range (DR), and pixel resolution, as well as power consumption. In particular, the pixel rate (= frame rate \times pixel resolution) has been getting higher for most applications, including scientific imagers and cameras for recording sports activities [1], [2]. Most mobile devices also now have integrated CISs, and while the need for high-performance increases, low power consumption is still an essential requirement.

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Various approaches to develop low power CIS readouts have been proposed, which employ power-efficient analog-to-digital converters (ADCs), such as a two-step single-slope ADC [3], a successive-approximation register (SAR) ADC with modified digital-to-analog-converter (DAC) switching technique [4], [5], and an inverter-based cyclic and sigma-delta ($\Sigma\Delta$) ADC [6], [7]. Among various ADC architectures, in recent years, SAR ADCs have been spotlighted for their excellent power efficiency [8] and have been utilized in many sensor applications, such as touch-screen sensors [9], [10] and biosensors [11], [12]. Some CISs have also followed this trend of using power-efficient SAR ADCs for readout [4], [5], [13]–[17].

Recently, new attempts to achieve further power savings beyond the circuit-level approach have been reported. In [17], the difference (Δ , Δ_{pixel}) between two neighboring pixels is read to skip several most significant bits (MSBs) decisions (i.e., Δ -readout scheme). Further power reduction could be achieved by utilizing a low-power SAR ADC to realize the Δ -readout: the A/D conversion can be completed by resolving just the remaining LSBs after the MSBs are copied from the previous pixel. One drawback with [17], however, is that a normal SAR conversion should be conducted if the Δ -readout failed to find a large Δ_{pixel} , which would increase the entire number of decision cycles compared with the traditional SAR ADCs.

Meanwhile, Δ -readout failure occurs mainly in the edge portion of an object in an image, because most of the large Δ_{pixels} are generated when two neighboring pixels have a large signal difference. For that reason, it is worth considering the possibility of extracting the edge information in an image in the event of a failure in the Δ -readout scheme.

In recent years, feature extraction from human-friendly images has become an essential function in computer-vision-based intelligent systems [18], and edge detection is an important preprocessing step for feature extractions. While the demand for real-time edge detection capability continues to increase for applications such as augmented reality, the computational complexity of edge detection algorithms has been a major cause of the speed bottleneck [19]. In addition, while the operating latency in image processing for edge extraction from a normal image is often considerable, demand for real-time edge extraction has grown for high-speed CIS applications. Image sensors with analog-domain edge detection capability have been reported, as in [20], but the complexity of the dedicated pixels is a major drawback. Additionally, the increased pixel resolution in recent CISs

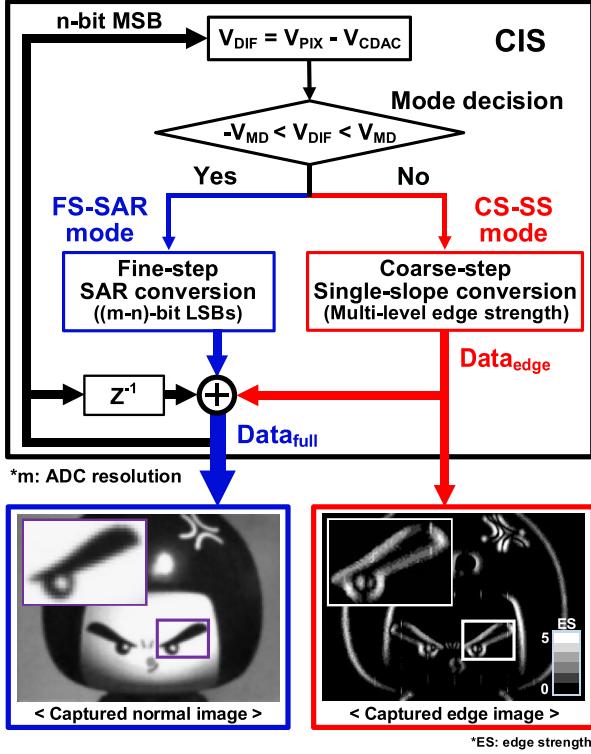


Fig. 1. Operational principle of the proposed CIS with dual-mode readout scheme and sample images.

will make the requirement of real-time CIS applications worse.

With these motivations, this work proposes the first dual-imaging CIS, which extracts a multi-level edge image in a real time from conventional pixels for machine and computer vision applications. A human-friendly normal image is also produced simultaneously. To exploit the approach, the speed reduction disadvantage of [17] also needs to be improved: if a Δ -readout scheme can be designed so as to cover a large Δ_{pixel} without a following normal SAR operation, the conversion speed could be improved with a further enhancement in power efficiency. This paper proposes a dual-mode readout scheme in which the Δ -readout is applied for speed and power efficiency, with decision cycles just for LSBs conversion, resulting in dual imaging in real time.

This paper is organized as follows. Section II discusses the proposed readout algorithm. The optimum conditions affecting the design tradeoff for a high-speed/power-efficient readout are analyzed in Section III. Section IV describes the prototype CIS architecture and implementation. The experimental results and discussions about the prototype chip are presented in Section V, followed by the conclusion in Section VI.

II. PROPOSED READOUT ALGORITHM

Fig. 1 illustrates the operation of the proposed dual-imaging CIS, and shows sample output images of a normal image and an edge image taken by the prototype CIS. The A/D conversion for a chosen pixel (V_{PIX}) begins by copying the *n*-bit MSBs (MSB_P) from the conversion result of a previous

pixel to the CDAC of the SAR ADC. This is done to reduce the number of conversion cycles and power consumption by utilizing the correlation between neighboring pixels, as in [17]. The proposed dual-mode readout scheme operates in two modes. By comparing the difference in the CDAC voltage generated by the *n*-bit MSB_P (V_{CDAC}) and V_{PIX} ($V_{DIF} = V_{PIX} - V_{CDAC}$) with a pre-determined mode decision threshold of V_{MD} , the operation mode is determined for V_{PIX} . If $|V_{DIF}| < V_{MD}$, the SAR-mode A/D conversion is conducted with fine steps (FS-SAR mode) for the remaining LSBs, similar to [17], and the full digital code ($Data_{full}$) is obtained by merging the LSBs from the FS-SAR mode with the *n*-bit MSB_P .

On the other hand, if $|V_{DIF}| > V_{MD}$, the chosen pixel is likely to be near a characteristic boundary that determines the shape of an object, and the ADC works in a CS single-slope mode (CS-SS mode) to readout the edge strength (ES), where ES means the difference between the previous pixel and the current pixel, instead of reading the actual V_{PIX} . By displaying the ES (generated as $Data_{edge}$, in Fig. 1), the edge image can be obtained in real time with no hardware/time overhead. In addition, by adding $Data_{edge}$ with the *n*-bit MSB_P , the representation of V_{PIX} ($Data_{full}$) is also obtained to generate a normal image.

Fig. 2 illustrates the detailed operation of a 10-bit SAR ADC that utilizes the proposed dual-mode readout scheme with the 4-bit MSB_P . The left-hand side of Fig. 2 shows the ten pixel values (V_{PIXEL}) of pixels P_1-P_{10} located in series on a selected row. Pixels are read from P_1 to P_{10} , in order. Let us consider pixel P_3 as a specific example (Case 1: corresponding waveform provided on the bottom center in Fig. 2). When readout begins for pixel P_3 , the 4-bit MSBs of D_{9-6} are copied from the previous pixel P_2 (i.e., 4-bit MSB_{P2}) and transferred to the CDAC of the SAR ADC in T_1 . Note that the copied 4-bit MSB_{P2} (D_{9-6}) is assumed "0011" in this example. According to the 4-bit MSB_{P2} , V_{CDAC} is generated to represent the center of the corresponding range (assuming VCM-based CDAC [21], [22]), and by comparing V_{CDAC} with the present pixel voltage of P_3 (V_{P3}), the digital code that determines the direction of decision (D_{DD}) is obtained in T_1 . A redundant cycle of T_2 is inserted with a DAC step size equivalent to that of T_1 [16], [17], resulting in the output code of D_5 . By adding D_{9-6} , D_{DD} , and D_5 , the 4-bit MSB_P value of P_3 is updated (from 0011 to 0100). If a crossing of V_{CDAC} and V_{P3} occurred during T_2 (zero crossing), the FS-SAR mode is basically applied in the following cycle of T_3 , and the output code of D_4 can be achieved. However, even though a zero crossing does not occur in T_2 , if the current pixel P_3 is very close to the previous pixel P_2 , P_3 still can be read by the following SAR operation. Considering this kind of case, in the proposed readout scheme, the operational mode is determined based on the result of T_3 . That is, if zero crossing occurred in T_3 , the following decisions in T_{4-7} are conducted in the FS-SAR mode, and the output code of D_{3-0} is obtained as the results of the remaining LSBs; if not, CS-SS mode follows. Throughout the total seven cycles, the ADC achieves 10-bit $Data_{full}$ by adding D_{9-6} , D_{DD} , and the LSBs of D_{5-0} according to their weights, as shown in Fig. 2 with Case 1. As a result, $Data_{full} = "0100001001"$

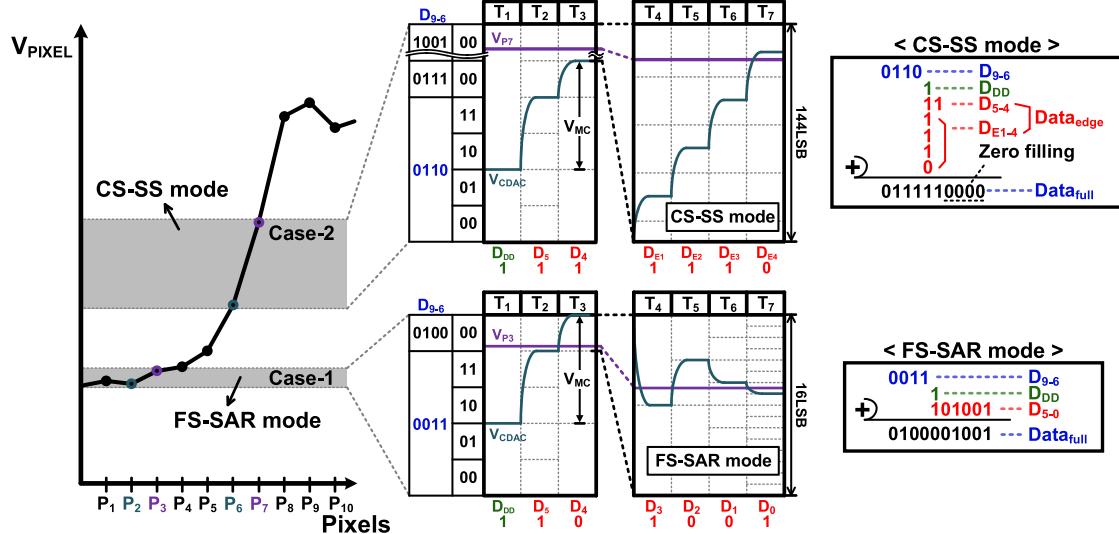


Fig. 2. Detailed operation of a 10-bit SAR ADC that utilizes the proposed readout scheme.

is obtained and its 4-bit MSBs of “0100” as 4-bit MSB P_3 are then utilized for the P_4 readout.

On the other hand, the readout of P_7 introduces another readout mode (Case 2: corresponding waveform illustrated in the top center in Fig. 2). Note that the decision procedure up to T_3 is identical to that of the P_3 example. However, because the crossing of V_{CDAC} and V_{P7} does not occur till T_3 , V_{DIF} would not be covered by the remaining LSBs. In order to measure V_{P7} , therefore, the decisions are made in the CS-SS mode thereafter. In T_{4-7} , a single-slope conversion with a CS size of 32 LSB is conducted to read the difference in P_6 and P_7 , and by concatenating D_{E1-4} (the resulting code from T_{4-7}) and D_{5-4} , the ES is extracted for edge information ($Data_{edge}$). In addition, interestingly, by adding the 4-bit MSB P_6 , D_{DD} , and $Data_{edge}$, with zero filling for the LSBs, resulting in $Data_{full}$, the pixel value of P_7 is also achieved for a normal image. Then, the 4-bit MSBs in the result of P_7 (“1001”) are used for the P_8 readout. One important issue with the CS-SS mode readout might be degraded image quality due to the CS quantization. This issue will be discussed in the following section in detail. Note that in the specific examples shown in Fig. 2, the range of V_{MD} is 48 LSB, since the step size in T_2 is 32 LSB and that in T_3 is 16 LSB.

According to the proposed conversion algorithm of the dual-mode readout, the conversion rate of the SAR ADC is improved by reducing the number of required conversion cycles to seven for 10-bit resolution. In addition, by saving the MSBs conversion cycles, which account for a large portion of the switching power consumption of the CDAC, the energy efficiency of the SAR ADC can be improved.

III. STUDY ON DESIGN TRADEOFF

Unlike the FS-SAR mode operation with fine resolution, when V_{PIXEL} is read in the CS-SS mode, a loss of pixel information occurs because of not only the CS size but also the limited number of decision cycles. (In other words, images around edges are likely to be blurred and smoothed.)

Fig. 3 explains the edge-blur phenomena produced by the finite readout coverage in the CS-SS mode, and illustrates the effect of the CS size (Δ_{CS}) on image quality in both normal and edge images. Let us take P_8-P_{10} from Fig. 2 as an example [Fig. 3(a)]. P_8 is read in the CS-SS mode due to the large difference (e.g., $|V_{DIF}| > V_{MD}$) with P_7 , and the ES is found to be $5.5 \Delta_{CS}$ in T_7 with an error of about $2.5 \Delta_{CS}$, resulting in edge smoothing. While this loss in ES can be somewhat compensated later, when P_9 is read, P_9 cannot be read with a fine resolution, even though P_9 is very close to P_8 . This results in a large quantization error (Q_{error}), resulting in edge blur. A VGA-formatted image is simulated to illustrate the image qualities depending on the size of Δ_{CS} , as shown in Fig. 3(b). If Δ_{CS} is as small as 4 LSB, smoothing occurs around the strong edges due to the limited readout coverage. If Δ_{CS} is as large as 64 LSB, the overall image becomes noisy because of the large Q_{error} s. In other words, if Δ_{CS} is too small or too large, edge smoothing or the blur phenomena will occur.

In order to study how images degrade in the edge region, the difference between the pixel value of the original image and that achieved by the proposed readout scheme, the edge error (EE), is defined as

$$EE = P_{Edge_Ideal} - P_{Edge_CS} \quad (1)$$

where P_{Edge_Ideal} is the original value of each edge pixel and P_{Edge_CS} is the detected value of the corresponding pixel in the CS-SS mode. The histogram of EE gathered from the VGA-formatted sample image of Fig. 3 for various values of Δ_{CS} is shown in Fig. 4, with the vertical axis representing the normalized number of pixels that have a non-zero EE (N_{EE_NORM})

$$N_{EE_NORM} = N_{EE}/N_{Edge_PIX} \quad (2)$$

where N_{EE} is the number of pixels that have non-zero EE and N_{Edge_PIX} is the total number of edge pixels read in the CS-SS mode. The log-scaled horizontal-axis represents EE in

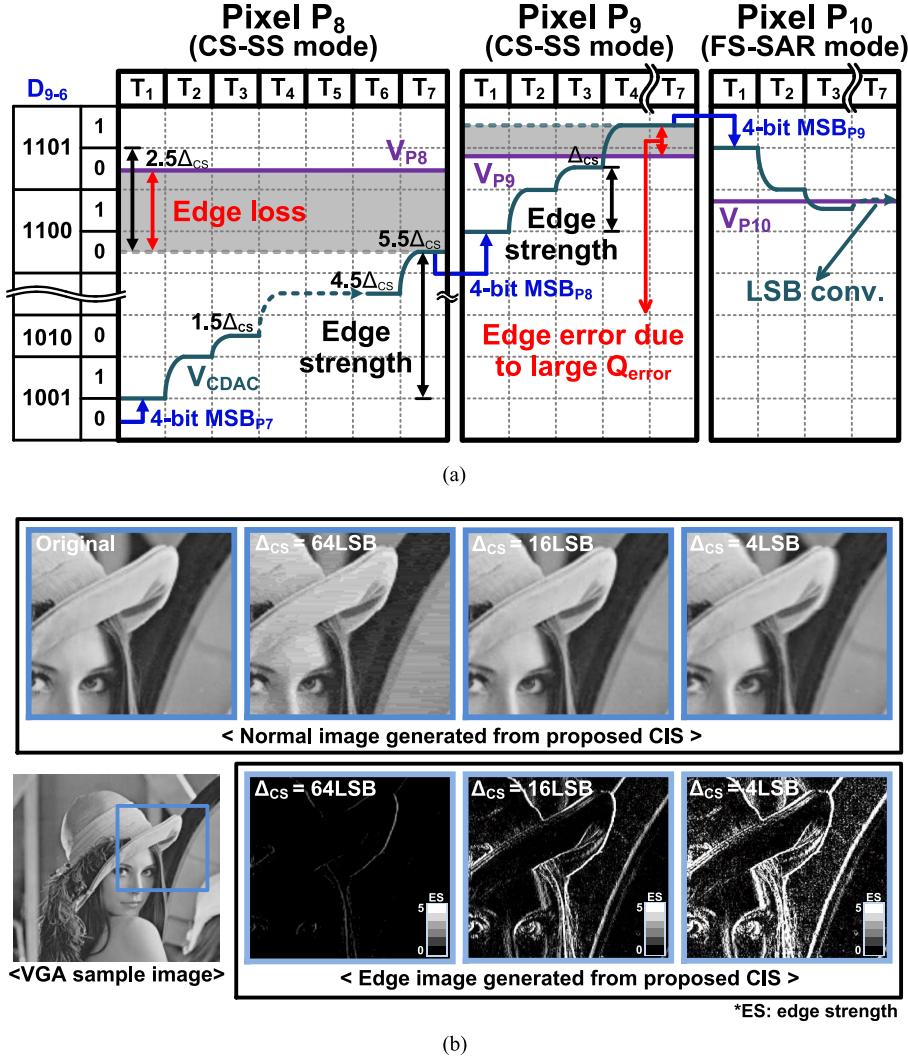


Fig. 3. (a) edge-blur due to the finite detection range and (b) effect on the image quality for various CS sizes.

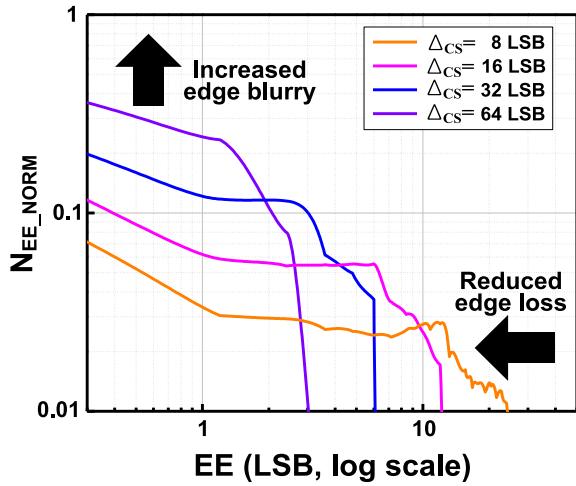


Fig. 4. Histogram of EE depending on the size of Δ_{CS} size.

units of LSB in the 10-bit resolution. As Δ_{CS} increases from 8 to 64 LSB, the value of EE is reduced while the edge blur increases.

On the other hand, since the correlation with adjacent pixels increases when the pixel resolution increases [17], the optimum Δ_{CS} can be found for various image formats. In order to define image quality with a representative quantity, the averaged EE (EE_{AVG}) is defined as

$$EE_{AVG} = \sum_{k=1}^{N_{Edge_PIX}} |EE_k| / N_{Edge_PIX}. \quad (3)$$

Fig. 5 shows the EE_{AVG} for various image formats depending on Δ_{CS} in units of LSB in 10-bit resolution, and the optimum Δ_{CS} for each image format can be found. Sample images were collected from a variety of themes in Full HD, HD, VGA, QVGA, and QQVGA pixel resolution, respectively, with each set consisting of 10 000 samples. Here, the resolution of the MSB_P in each image format is taken from the research in [17]: 6-bit MSB_P for VGA and 7-bit MSB_P for HD/FHD. For QQVGA, the calculated EE_{AVG} becomes minimum with $EE_{AVG} = 8.6$ LSB at $\Delta_{CS} = 32$ LSB. Note that the optimum Δ_{CS} is reduced when the image resolution increases with reduced EE_{AVG} . The EE_{AVG} of VGA is found to be 3.9 LSB at $\Delta_{CS} = 16$ LSB while that of FHD is

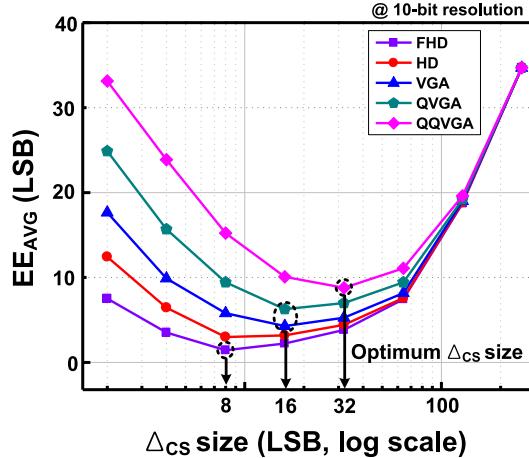


Fig. 5. Optimum Δ_{CS} for various image formats.

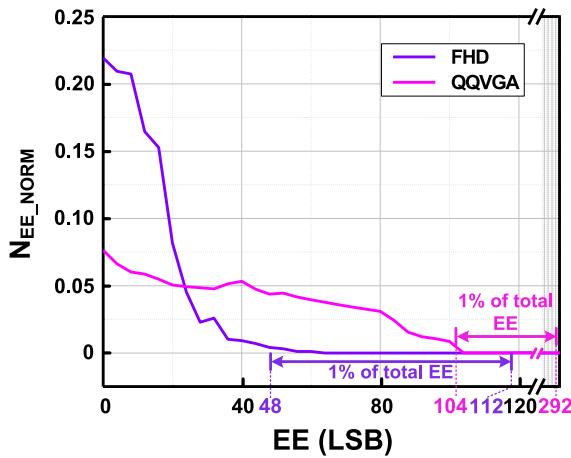


Fig. 6. Histogram of EE plot with optimum Δ_{CS} size.

1.8 LSB at $\Delta_{CS} = 8$ LSB. These plots of EE_{AVG} imply that the proposed dual-mode readout is more suitable for higher resolution imagers, where it offers great power savings and enhanced speed due to the considerably reduced decision cycles.

Meanwhile, an issue with EE_{AVG} is that it does not show the maximum pixel error value. In order to show more detailed error information with the optimum Δ_{CS} , as an example, the histograms of EE of QVGA and FHD are shown in Fig. 6 with the same data gathered for Fig. 5. Whereas 99% of the EE in QVGA is less than 104 LSB at Δ_{CS} of 32 LSB, that in FHD is less than 48 LSB at Δ_{CS} of 8 LSB at 10-bit resolution. The peak values of EE in QVGA and FHD are found to be 292 LSB and 112 LSB, respectively. In order to see the effect of EE on image quality, two images in the FHD image format are compared in Fig. 7: the top one with the conventional readout scheme and the bottom one with the proposed dual-mode readout scheme. It would not be easy to tell the difference between the two images at a glance. However, if we zoomed-in view to the part where the peaks of the EE are included, as shown in the box, we can see that the edges are blurred in the bottom image. The

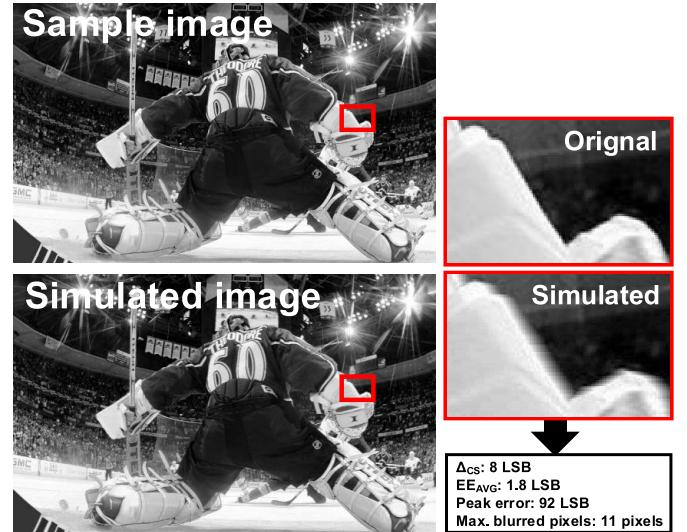


Fig. 7. Effect of EE in FHD sample image.

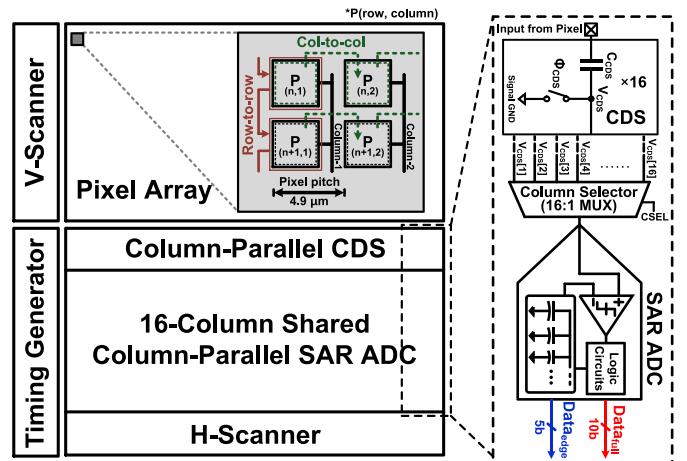


Fig. 8. Block diagram of the prototype CIS.

bottom image has EE_{AVG} of 1.8 LSB when it is read with Δ_{CS} of 8 LSB. In the enlarged region of the simulated image, the maximum pixel error and the maximum number of blurred pixels are 92 LSB and 11 pixels, respectively. This means that the proposed readout scheme is suitable for applications where clear edged normal images are not highly requested, such as video camera (oriented to moving objects) or machine-vision applications (oriented to feature extraction). Note that since the ADC will be implemented with the full hardware required for 10-bit resolution, as will be shown in Section IV, we can add an additional operational mode so that the ADC can work as a typical SAR ADC when a clear edge is preferred to more efficient power or speed.

IV. PROTOTYPE CIS ARCHITECTURE AND IMPLEMENTATION

Fig. 8 is the block diagram of the prototype CIS with the proposed dual-mode readout scheme, which is composed of a QVGA pixel array (160×120) of 4T-APS with $4.9-\mu\text{m}$ pitch,

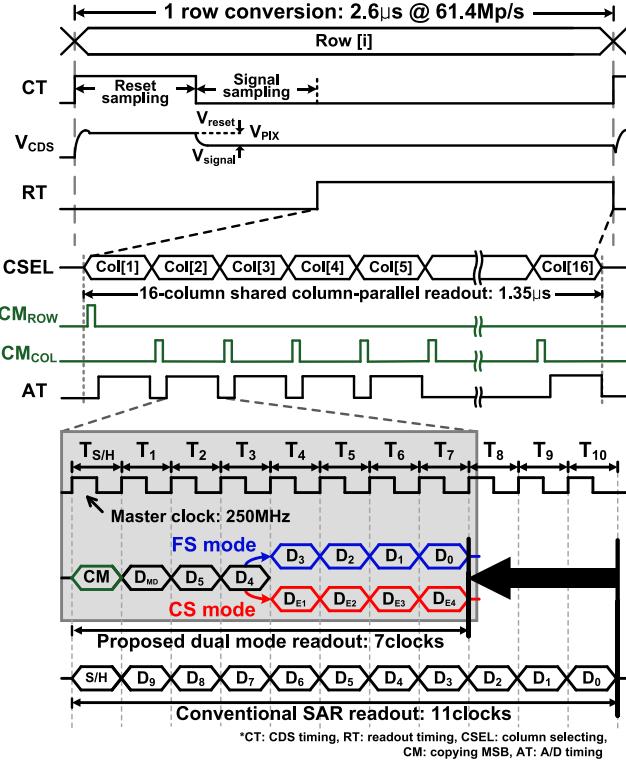


Fig. 9. Operational timing diagram of the prototype CIS.

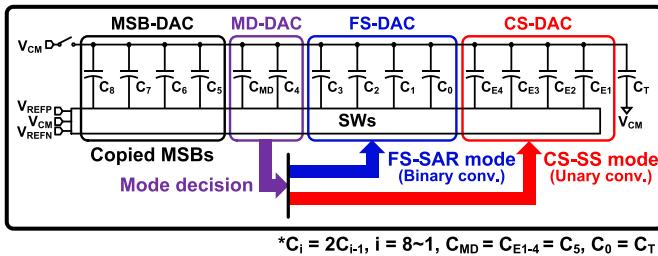


Fig. 10. Simplified CDAC schematic of the proposed SAR ADC.

a V-scanner for sequential row activation, correlated double-sampling (CDS) arrays for pixel fixed-pattern noise (FPN) reduction, and a column selector array for sequential column activation at a selected row. Similar to [17], 16-column-shared 10-bit SAR ADCs are used for the 160-column readout (a total of ten channels) to alleviate the ADC integration issue in narrow pitches of pixels, building a multi-column-parallel (MCP) readout architecture [15], [17], [23]. The H-scanner scans the A/D converted data from each MCP unit.

The key sequences of the proposed dual-mode readout scheme in a MCP unit follow the same readout direction as in [17]: a pixel chosen for readout takes its 4-bit MSBs from its left-side pixel in the column-to-column direction ($P_{(n,1)} \rightarrow P_{(n,2)} \dots$), and the leftmost pixel of each row unit takes them from the pixel above in the row-to-row direction ($P_{(n,1)} \rightarrow P_{(n+1,1)} \dots$) in a MCP unit.

A simplified operational timing diagram is shown in Fig. 9. The operation of the MCP unit is as follows: each pixel in

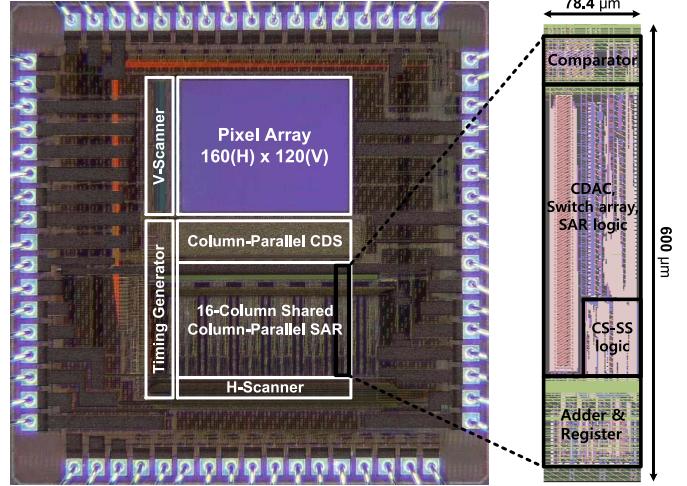


Fig. 11. Chip microphotograph.

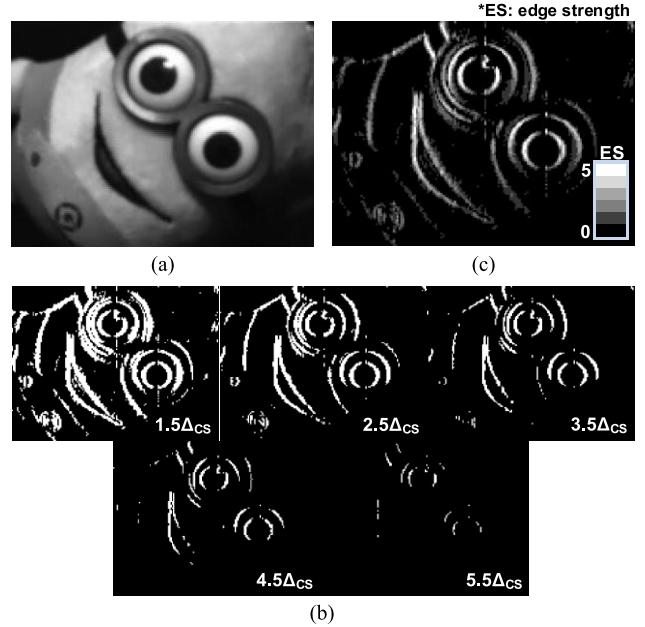


Fig. 12. (a) Captured normal image. (b) Captured five different edge images. (c) Synthesized five-level edge image.

an enabled row will be read out by ADC sequentially, after the analog CDS making $V_{CDS} (=V_{reset} - V_{signal})$ eliminates the FPN of the row by enabling CT (CDS timing). During readout timing, one ADC selects 16 columns sequentially (ten ADCs cover 160 columns) and performs the proposed dual-mode operation during ADC timing. At CM_{ROW}, the dual-mode readout is performed in a row-to-row manner for the first pixels of each MCP unit, and the 4-bit MSBs of the previous row are adopted to the CDAC in an SAR ADC. Similarly, CM_{COL} is used to sample the pixel data in a column-to-column manner.

In this design, as studied with Fig. 5, 4-bit MSBs are copied from the previous pixel for QVGA image format. Compared with a conventional 10-bit SAR ADC design in [24] and [25] which requires 11 cycles for A/D conversion including input sampling, the proposed SAR ADC with the dual-mode readout

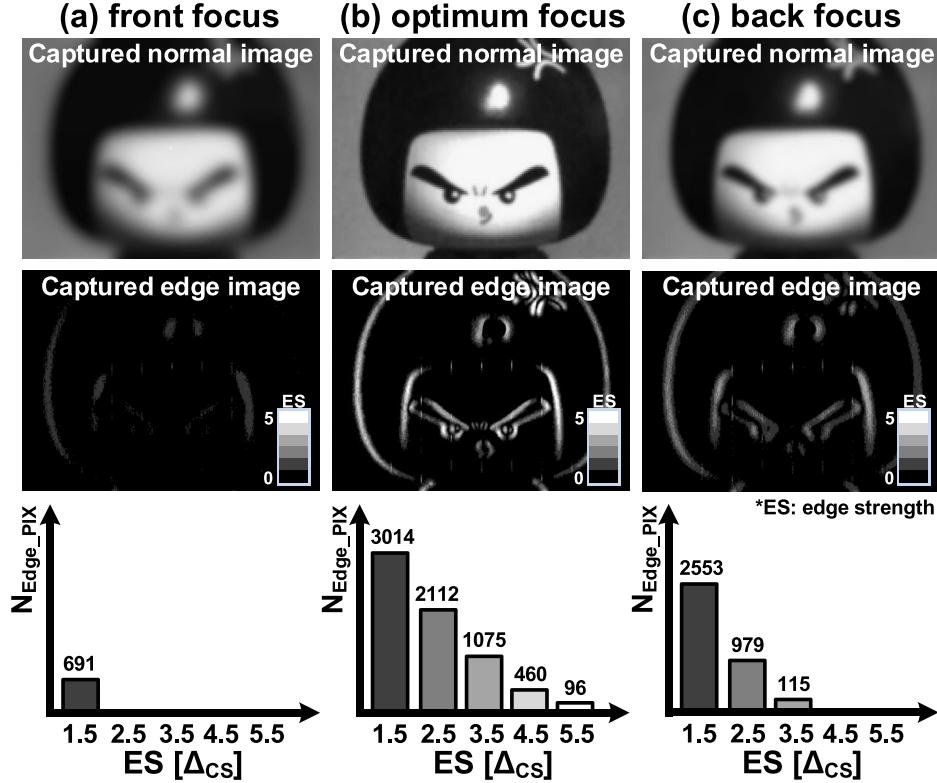


Fig. 13. Edge extraction capabilities in different focus conditions. (a) Front focus. (b) Optimum focus. (c) Back focus.

scheme needs only a total of seven cycles for A/D conversion. In addition to the low-power and high-speed characteristics of the SAR ADC, the proposed dual-mode readout scheme reduces conversion cycles and thus further improves the conversion rate, with enhanced energy efficiency.

Fig. 10 shows the simplified CDAC schematic of the proposed 10-bit SAR ADC with the proposed dual-mode readout scheme. The binary-weighted CDAC based on trilevel switching [26], [27] is composed of a 4-bit MSB-DAC, a MD-DAC for the mode decision in T_2 and T_3 , a 4-bit FS-DAC for the LSBs decision in the FS-SAR mode, and a CS-DAC with 32-LSB unit capacitors for the CS-SS mode. The capacitances of C_{MD} and the CS-DAC array (C_{E1-4}) are designed to be equal to the capacitance of C_5 according to the operational principle discussed with Fig. 2. The entire CDAC is composed of 672C, including 160C for the C_{MD} of the MD-DAC and the C_{E1-4} of the CS-DAC. The total capacitance is 470 fF with a 700-aF MOM-type unit capacitor considering matching and kT/C noise requirements.

V. EXPERIMENTAL RESULTS AND DISCUSSION

A prototype CIS image sensor chip was implemented with a 1P4M 0.18- μ m CIS process. A chip microphotograph of the fabricated CIS imager is shown in Fig. 11. A QQVGA (160×120) array of 4.9 μ m-pitch 4T-APS pixels and the array of the proposed MCP SAR ADCs applying the dual-mode readout scheme were implemented in a chip size of 2.35 mm \times 2.35 mm with control circuitry, including I/O pads. The single-channel SAR ADC occupies an area of 78.4 μ m \times 600 μ m

and is laid out across 16 columns of pixels. The prototype CIS has a data rate of 61.4 Mp/s, resulting in 3200 frames/s at the QQVGA pixel resolution, which corresponds to 355 frames/s in the FHD pixel resolution.

For the proof of concept, the prototype QQVGA CIS was designed with a Δ_{CS} of 32 LSB for the optimum EE_{Avg}. Fig. 12(a) and (b) show two types of raw images taken from the prototype CIS: (a) a normal image from the Datefull and (b) five different edge images taken from each bits of the 5b Date_{edge} representing $1.5\Delta_{CS}$ (D_4) = 48 LSB, $2.5\Delta_{CS}$ (D_{E1}) = 80 LSB, $3.5\Delta_{CS}$ (D_{E2}) = 112 LSB, $4.5\Delta_{CS}$ (D_{E3}) = 144 LSB, and $5.5\Delta_{CS}$ (D_{E4}) = 176 LSB. Fig. 12(c) is the five-level edge image synthesized from Fig. 12(b) by simple addition as illustrated in Fig. 2. Note that the normal image (Data_{full}) and the edge image (Data_{edge}) are all generated from the CIS chip and do not require extra off-chip calculation.

The ES discrimination capability shown in Fig. 12(b) might be useful for several purposes. As an example, it can be utilized for contrast-based autofocus control: Fig. 13 shows the captured normal and edge images taken by the prototype CIS with three different focus conditions. The images taken in the front and back focus conditions are blurry and vague; thus, the number of pixels recognized as edges N_{Edge_PIX} are relatively small with poor ES discrimination. On the other hand, the optimum focus case shows various ES values with high N_{Edge_PIX} . The weighted sums of ES and N_{Edge_PIX} in the front and back focus cases are 1036 Δ_{CS} and 6679 Δ_{CS} , respectively, while those of the optimum focus case is 16161 Δ_{CS} . This implies that the proposed dual-mode readout

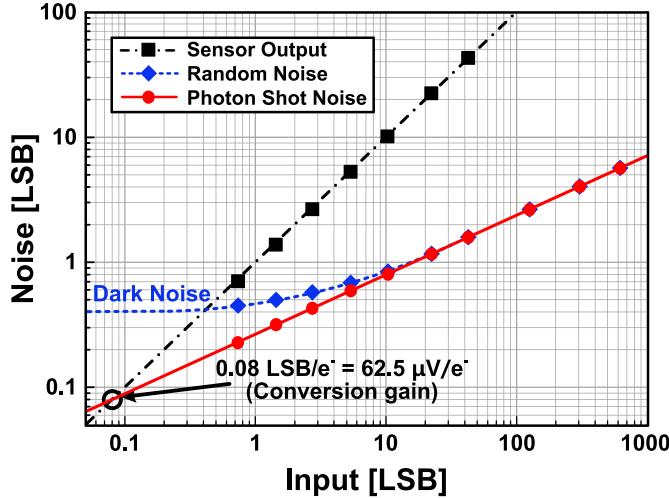


Fig. 14. Measured photon transfer curve.

can contribute to low-cost autofocus simply by adjusting the focus so that the weighted sum of $\text{Data}_{\text{edge}}$ has the maximum value.

One issue with the proposed delta-readout scheme along a selected row (column-to-column difference) is that delta information between the rows is not detected by the proposed scheme, except for the pixels in the first column of every group of 16 columns that shares a single readout ADC. The pixels in the first column of each group compare delta with the pixel sitting above them, and thus, horizontal-direction delta is detected every 16 columns. Thus, edges in horizontal direction are not clearly detected, and therefore, further study is needed for improvement of edge detection capability.

Fig. 14 is the measured photon transfer curve, which shows the random and shot noise results in response to incident illumination [28]. The random noise floor (dark noise) was measured to be 0.4 LSB from 10 000 sample images. In this design, 1-LSB corresponds to $780 \mu\text{V}$ with the 0.8-V reference at a 10-bit resolution. Therefore, the dark noise is about $320 \mu\text{V}_{\text{rms}}$, which corresponds to $5 e^-_{\text{rms}}$ with a measured pixel conversion gain of $62.5 \mu\text{V}/e^-$. Since the noise of the stand-alone readout circuit was measured to be $4.9 e^-_{\text{rms}}$, the pixel noise is estimated to be about $1 e^-_{\text{rms}}$. As a result, a DR [29] of 67.9 dB was obtained. Note that all the measurements were performed at room temperature with an IR cut filter.

The measured maximum differential nonlinearity (DNL) and integral nonlinearity (INL) profile of the prototype ADC are 0.65 LSB and 0.92 LSB, respectively, as shown in Fig. 15.

The measured performances of the fabricated chip are summarized in Table I. The total power consumption of the image sensor is 4.3 mW under supply voltages of 2.8 V for the pixel array and 1.8 V for the readout circuitry at 3200 frames/s. A single-channel 10-bit SAR ADC runs at a conversion rate of 6.3 ms/s. The time period spent in reading out one entire row is 2.6 μs .

Table II shows a comparison of the primary characteristics of our imager with those of some recent image sensors, including normal image sensors utilizing SAR ADC for readout [5], [17], [31] and dedicated image sensors for real-time edge extraction applications [19], [32], [33]. The

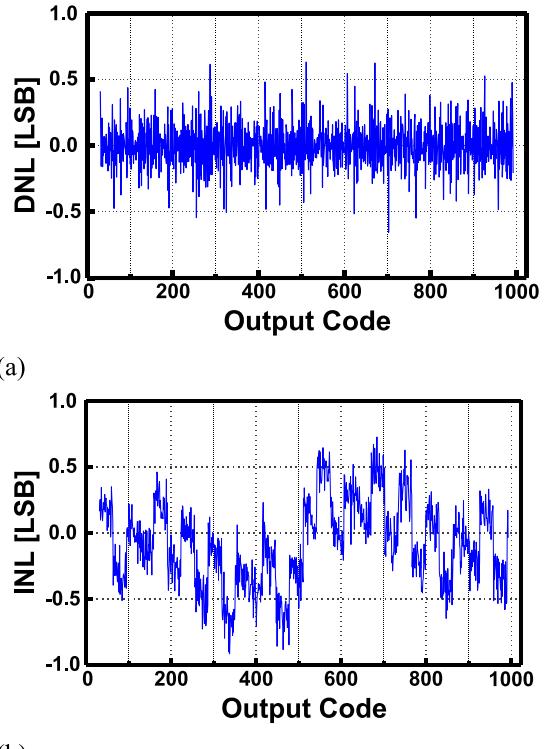


Fig. 15. Measured linearity of the ADC. (a) DNL. (b) INL.

TABLE I
PERFORMANCE SUMMARY

Parameter	Value
Technology	$0.18 \mu\text{m}$ 1P4M CIS Process
Total area	$2.35 \text{ mm} \times 2.35 \text{ mm}$
Supply voltages	2.8 V (Pixel), 1.8 V (Circuit)
Power consumption	4.3 mW
Number of pixels	$160 (\text{H}) \times 120 (\text{V})$
Pixel type	4-TR (Pinned Photodiode)
Pixel size	$4.9 \mu\text{m} \times 4.9 \mu\text{m}$
Fill factor	53%
Sensitivity	$6.5 \text{ V/lx}\cdot\text{s}$
Conversion gain	$62.5 \mu\text{V}/e^-$
Random noise	$5 e^-_{\text{rms}}$
CFPN	$0.67 e^-_{\text{rms}}$
Dynamic range	67.9 dB
ADC resolution	10 bits
DNL / INL	0.65 LSB / 0.92 LSB
Data rate	61.4 Mp/s

edge extraction function is integrated in the proposed dual-mode readout image sensor as a unique function. In comparison with dedicated image sensors [19], [32], [33] that can extract only 1-bit edge images with relatively large pixel sizes, five-level edge images were extracted using the proposed image sensor with a conventional 4T-APS. For

TABLE II
PERFORMANCE COMPARISON

	TCAS-I'14[5] D. G. Chen	JSSC'16[17] H. Kim	VLSI'16[31] S. Ji	This work	VLSI'15[32] K. Bong	ISSCC'13[33] J. Choi	ISSCC'08[19] N. Massari
Process	0.18 μm CIS	0.18 μm CIS	0.18 μm CIS	0.18 μm CIS	65 nm CMOS	0.18 μm CMOS	0.35 μm CMOS
Supply voltage	3.3/1.8	2.8/1.8	3.3/1.8	2.8/1.8	3.3/2.5/1.2	1.3/0.8	3.3
Pixel type	Conventional 4T APS	Conventional 4T APS	Conventional 4T APS	Conventional 4T APS	Specialized pixel	Specialized pixel	Specialized pixel
Pixel size	1.85 $\mu\text{m} \times$ 1.85 μm	4.4 $\mu\text{m} \times$ 4.4 μm	N/A	4.9 $\mu\text{m} \times$ 4.9 μm	7 $\mu\text{m} \times$ 7 μm	5.9 $\mu\text{m} \times$ 5.9 μm	26 $\mu\text{m} \times$ 26.5 μm
Pixel number	118 K	19.2 K	76.8 K	19.2 K	67.8 K	65 K	8 K
Pixel rate	2.12 Mp/s	19.2 Mp/s	10 Mp/s	61.4 Mp/s	2.3 Mp/s	983 Kp/s	410 Kp/s
ADC type	SAR	SAR	SAR	SAR	N/A	Single Slope	1-bit comparator
ADC resolution	9 bit	10 bit	10 bit	10 bit	N/A	8 bit	1 bit
Dynamic range	73 dB	60 dB	N/A	67.9 dB	N/A	54.8 dB	N/A
Conversion cycle (Normalized)	1	1.4	1	0.7	1	1	1
Integrated edge extraction	None	None	None	5-level edge image	1-bit edge image	1-bit edge image only for moving object	1-bit edge image
Power consumption	40 μW (ADC only)	1.5 mW	2.2 mW	4.3 mW	10 mW	51.06 μW	100 μW
*FoM ¹ [pJ/pixel/frame]	37.7	78.1	220.3	70	4340.2	51.94	244
**FoM ² [$e^- \cdot n\text{J}$]	36.4	0.86	1.1	0.35	N/A	N/A	N/A
***FoM ³ [$e^- \cdot p\text{J}/\text{step}$]	35.5	0.84	1.08	0.34	N/A	N/A	N/A

*FoM¹ = Power / ($N_{\text{PIX}} \times \text{fps}$), **FoM² = (Power \times Noise) / ($N_{\text{PIX}} \times \text{fps}$), ***FoM³ = (Power \times Noise) / ($N_{\text{PIX}} \times \text{fps} \times 2^N$), N = ADC resolution

various figure of merits (FoMs) [34], the prototype CIS demonstrates state-of-the-art class performance with FoM¹ of 70 pJ/pixel/frame, FoM² of 0.35 $e^- \cdot n\text{J}$, and FoM³ of 0.34 $e^- \cdot p\text{J}/\text{step}$.

VI. CONCLUSION

This work introduces the first CIS to produce a real-time multi-level edge image with conventional pixels, while also producing a human-friendly normal image. The proposed CIS utilizes an SAR ADC with a high-speed/power-efficient dual-mode readout scheme. With a maximum pixel rate of 61.4 Mp/s, the prototype demonstrated state-of-the-art FoMs.

For computer vision image sensor applications requiring high-speed operation and low power consumption, the proposed readout scheme can be a promising solution. The proposed readout scheme will be very suitable for a high-resolution image sensor, offering great power savings and speed enhancement due to the saved decision cycles for MSBs.

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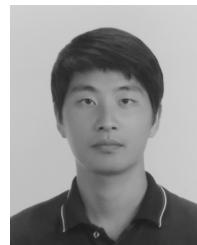
REFERENCES

- [1] J. Ohta, *Smart CMOS Image Sensors and Applications*. Boca Raton, FL, USA: CRC Press, 2010.
- [2] A. Khosla and D. S. Kim, *Optics Imaging Devices*. Boca Raton, FL, USA: CRC Press, 2015.
- [3] S. Lim, J. Lee, D. Kim, and G. Han, "A high-speed CMOS image sensor with column-parallel two-step single-slope ADCs," *IEEE Trans. Electron Devices*, vol. 56, no. 3, pp. 393–398, Mar. 2009.
- [4] D. G. Chen, F. Tang, and A. Bermak, "A low-power pilot-DAC based column parallel 8b SAR ADC with forward error correction for CMOS image sensors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 10, pp. 2572–2583, Oct. 2013.
- [5] D. G. Chen, F. Tang, M. K. X. Law; Zhong, and A. Bermak, "A 64 fJ/step 9-bit SAR ADC array with forward error correction and mixed-signal CDS for CMOS image sensors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 11, pp. 3085–3093, Nov. 2014.
- [6] Y. Chae *et al.*, "A 2.1 M pixels, 120 frames/s CMOS image sensor with column-parallel $\Delta \Sigma$ ADC architecture," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 236–247, Jan. 2011.
- [7] T. Yasue *et al.*, "A 1.7-in, 33-Mpixel, 120-frames/s CMOS image sensor with depletion-mode MOS capacitor-based 14-b two-stage cyclic A/D converters," *IEEE Trans. Electron Devices*, vol. 63, no. 1, pp. 153–161, Jan. 2016.
- [8] B. Murmann, *ADC Performance Survey 1997–2016*. [Online]. Available: <http://web.stanford.edu/~murmann/adcsurvey.html>
- [9] J. H. Yang *et al.*, "A highly noise-immune touch controller using filtered-delta-integration and a charge-interpolation technique for 10.1-inch capacitive touch-screen panels," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 390–391.
- [10] H. J. Kim, D. S. Jo, J. H. Yang, and S. T. Rye, "A low-power fast readout circuit using a dual-mode sensing algorithm for medium-size capacitive touch screen panels," in *SID Symp. Dig. Tech. Papers*, 2014, pp. 540–543.
- [11] F. M. Yaul and A. P. Chandrakasan, "11.3 A 10 b 0.6 nW SAR ADC with data-dependent energy savings using LSB-first successive approximation," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 198–199.
- [12] G.-Y. Huang, S.-J. Chang, C.-C. Liu, and Y.-Z. Lin, "A 1 μW 10-bit 200-kS/s SAR ADC with a bypass window for biomedical applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 11, pp. 2783–2795, Nov. 2012.
- [13] S. Matsuo *et al.*, "8.9-megapixel video image sensor with 14-b column-parallel SA-ADC," *IEEE Trans. Electron Devices*, vol. 56, no. 11, pp. 2380–2389, Nov. 2009.
- [14] M. S. Shin, J. B. Kim, M. K. Kim, Y. R. Jo, and O. K. Kwon, "A 1.92-megapixel CMOS image sensor with column-parallel low-power and area-efficient SA-ADCs," *IEEE Trans. Electron Devices*, vol. 59, no. 6, pp. 1693–1700, Jan. 2012.
- [15] R. Funatsu *et al.*, "133Mpixel 60fps CMOS image sensor with 32-column shared high-speed column-parallel SAR ADCs," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 112–113.

- [16] H. Kim *et al.*, “Delta readout scheme for image-dependent power savings in a CMOS image sensor with multi-column-parallel SAR ADCs,” in *Proc. IEEE A-SSCC*, Nov. 2015, pp. 1–4.
- [17] H. Kim *et al.*, “A delta-readout scheme for low-power CMOS image sensors with multi-column-parallel SAR ADCs,” *IEEE J. Solid-State Circuits*, vol. 51, no. 10, pp. 2262–2273, Oct. 2016.
- [18] I. Hong *et al.*, “A 2.71 nJ/pixel 3D-stacked gaze-activated object-recognition system for low-power mobile HMD applications,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 326–327.
- [19] N. Massari, M. Gottardi, and S. Jawed, “A 100 μ W 64 \times 128-pixel contrast-based asynchronous binary vision sensor for wireless sensor networks,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 588–589.
- [20] P. Dollár and C. L. Zitnick, “Fast edge detection using structured forests,” *IEEE Trans. Pattern Anal. Mach. Intell.*, vol. 37, no. 8, pp. 1558–1570, Aug. 2015.
- [21] K. Bacrania, “A 12-bit successive-approximation-type ADC with digital error correction,” *IEEE J. Solid-State Circuits*, vol. 21, no. 6, pp. 1016–1025, Dec. 1986.
- [22] S. H. Cho, C. K. Lee, J. K. Kwon, and S.-T. Ryu, “A 550-W 10-b 40-MS/s SAR ADC with multistep addition-only digital error correction,” *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1881–1892, Aug. 2011.
- [23] S. Huang, D. Estrada, D. V. Blerckom, and B. Manssoriam, “Design of analog readout circuitry with front-end multiplexing for column parallel image sensors,” in *Proc. IEEE IISW*, Jun. 2013, pp. 1–4.
- [24] C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, “A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure,” *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, Apr. 2010.
- [25] C.-C. Liu *et al.*, “A 10b 100MS/s 1.13 mW SAR ADC with binary-scaled error compensation,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 386–387.
- [26] Y. Zhu *et al.*, “A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS,” *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1111–1121, Jun. 2010.
- [27] M. Saberi, R. Lotfi, K. Mafinezhad, and W. A. Serdijn, “Analysis of power consumption and linearity in capacitive digital-to-analog converters used in successive approximation ADCs,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 8, pp. 1736–1748, Aug. 2011.
- [28] J.-H. Park, S. Aoyama, T. Watanabe, K. Isobe, and S. Kawahito, “A high-speed low-noise CMOS image sensor with 13-b column-parallel single-ended cyclic ADCs,” *IEEE Trans. Electron Devices*, vol. 56, no. 11, pp. 2414–2422, Nov. 2009.
- [29] F. Tang, D. G. Chen, B. Wang, and A. Bermak, “Low-power CMOS image sensor based on column-parallel single-slope/SAR quantization scheme,” *IEEE Trans. Electron Devices*, vol. 60, no. 8, pp. 2561–2566, Aug. 2013.
- [30] J. Deguchi *et al.*, “A 187.5 μ Vrms-read-noise 51 mW 1.4 Mpixel CMOS image sensor with PMOSCAP column CDS and 10b self-differential offset-cancelled pipeline SAR-ADC,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 494–495.
- [31] S. Ji, J. Pu, B. C. Lim, and M. Horowitz, “A 200pJ/pixel/frame CMOS image sensor with partial settling readout architecture,” in *Proc. Symp. VLSI Circuits*, 2016, pp. 1–2.
- [32] K. Bong, I. Hong, G. Kim, and H.-J. Yoo, “A 0.5-degree error 10 mW CMOS image sensor-based gaze estimation processor with logarithmic processing,” in *Proc. Symp. VLSI Circuits*, 2015, pp. C46–C47.
- [33] J. Choi, S. Park, J. Cho, and E. Yoon, “A 3.4 μ W CMOS image sensor with embedded feature-extraction algorithm for motion-triggered object-of-interest imaging,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 478–479.
- [34] S. Kawahito, “Column readout circuit design for high speed low noise imaging,” presented at the IEEE ISSCC Image Sensor Forum, San Francisco, CA, USA, Feb. 2010.

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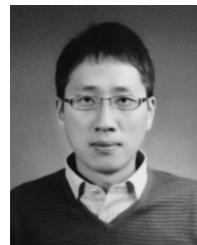
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