A ±50-mV Linear-Input-Range VCO-Based Neural-Recording Front-End With Digital Nonlinearity Correction

Wenlong Jiang, Vahagn Hokhikyan, Hariprasad Chandrakumar, *Student Member, IEEE*, Vaibhav Karkare, *Member, IEEE*, and Dejan Marković, *Member, IEEE*

***Abstract*— Closed-loop neuromodulation is an essential function in future neural implants for delivering efficient and effective therapy. However, a closed-loop system requires the neural-recording front-end to handle large stimulation artifacts—a feature not supported by most state-of-the-art designs. In this paper, we present a neural-recording front-end that has an input range of ±50 mV and can be used in closed-loop systems. The proposed front-end avoids the saturation due to stimulation artifacts by employing a voltage-controlled oscillator (VCO) to directly convert the input signal into the frequency domain. The VCO nonlinearity is corrected using area-efficient foreground polynomial correction. Implemented in a 40-nm CMOS process, the design occupies 0.135 mm^2 with an analog power of 3 μW and a digital switching power of 4 μW. It achieves ten times higher linear input range than prior art, and 79-dB spurious-free dynamic range at peak input, with an input-referred noise of 5.2 μV_{rms} across the local-field-potential band of 1–200 Hz. With on-chip subhertz high-pass filters realized by duty-cycled resistors, the front-end also eliminates the need of off-chip dc-blocking capacitors.**

***Index Terms*— Closed-loop, front-end, Horner's method, neural-recording, neuromodulation, nonlinearity correction, quantizer, very large time-constant synthesis, voltage-controlled oscillator (VCO).**

I. Introduction

ACCORDING to the World Health Organization, neuropsychiatric disorders are the leading cause of disability in the U.S. [1]. Deep brain stimulation (DBS) has been used as an important treatment method in a small group of patients who are not responsive to medication and psychological therapies [2]–[4]. It has also largely replaced other invasive treatment approaches, such as ablative brain surgery.

A neurostimulator, which delivers electrical pulses through implanted electrodes to the brain regions that are responsible for the patient's condition, is at the heart of a DBS system. Traditionally, these electrical pulses are delivered in a continuous, open-loop fashion with no real-time feedback from the brain as it is being stimulated. This open-loop stimulation approach can lead to various unintended adverse effects, including mania, depression, apathy, panic, impulsivity, anxiety, hallucinations, and even suicidal ideation [6], [7].

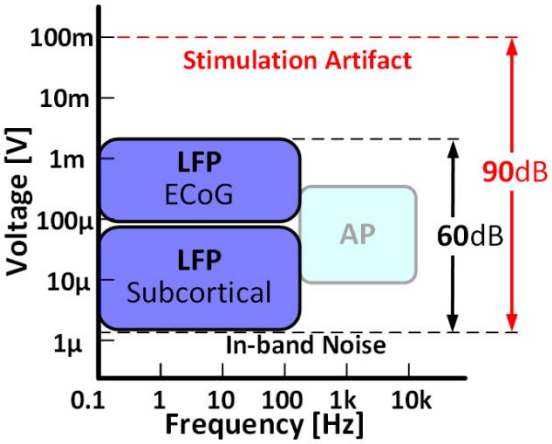


Fig. 1. Neural recording signal frequency range and voltage level. Stimulation artifact can go as high as 100 mV, which extends DR to 90 dB.

Recently, there have been attempts in advancing neuromodulation devices by closing the stimulation loop with feedback from local-field-potential (LFP) recordings [10], [11]. LFPs, as electrophysiological signals spanning 1–200 Hz, represent aggregate neural activity recorded either on the cortical surface, known as electrocorticography, or in subcortical areas. By using feedback from LFP recordings to control stimulation, these devices can potentially lead to better clinical outcomes, mitigate the adverse effects of DBS, and reduce the time required for tuning stimulation parameters [12].

Nevertheless, closed-loop neuromodulation exposes LFP recording front-ends to large stimulation artifacts that can be much higher than the magnitude of recorded neural signals. The stimulation artifacts refer to the voltage disturbances at recording sites because of injected stimulation currents, which are most pronounced at recording sites close to the stimulation electrodes. For a typical stimulation current ranging from 100 μA to several mAs, and the estimated current injection path resistance of 100 Ω for the stimulation, stimulation artifacts are in the range of 10–100 mV, or about 30 dB beyond the LFP signal range, as shown in Fig. 1.

Manuscript received April 10, 2016; revised September 2, 2016 and October 20, 2016; accepted October 24, 2016. Date of publication December 20, 2016; date of current version January 4, 2017. This paper was approved by Guest Editor Roman Genov. This work was supported by the Defense Advanced Research Projects Agency.

W. Jiang, V. Hokhikyan, H. Chandrakumar, and D. Marković are with the University of California at Los Angeles, Los Angeles, CA 90095-1594 USA.

V. Karkare is with Silicon Laboratories, Sunnyvale, CA 94085 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2016.2624989

Traditional implantable recording front-ends are designed to sense neural signals only, which are up to several millivolts [17]–[19]. They will be saturated by large stimulation artifacts. Given the large time constants associated with neural signal recording, a saturated front-end will take tens of milliseconds or longer to recover to its normal bias condition. To address the saturation problem, some neuromodulation systems blank the front-ends in the event of a large input to avoid saturation and the associated recovery time [15], [20]. However, this approach leads to signal loss for milliseconds during stimulation, especially when delivering a burst of stimulation pulses. Frequency-domain separation of the stimulation pattern and the sensed signal is another approach to combat the problem of stimulation artifacts [14]. Such frequency separation may not be feasible, since closed-loop neuromodulation therapies can require stimulation frequencies to overlap with those of the recorded signals. Recently, analog/mixed-signal feedback techniques to cancel the stimulation artifact have been proposed [21]. However, this cancellation has been demonstrated for artifacts with an amplitude of <3 mV. The larger artifacts may still saturate the front-end and render the cancellation inoperable.

To allow robust recording of LFP signals in the presence of stimulation artifacts, this paper presents an implantable LFP recording front-end design with a linear-input-range of ± 50 mV and $\sim$80-dB dynamic range (DR). With a front-end that does not saturate under large stimulation artifact, adaptive signal processing techniques can be used downstream to remove the stimulation artifact from the recorded signal. Moreover, with full capture of stimulation artifact as well as neural signals, the artifact rejection can have more flexibility and faster convergence.

The rest of this paper is organized as follows. Section II discusses the front-end architecture that we used in this paper to achieve a large input range and high DR with a low power consumption. Section III details the circuit-level tradeoffs used to design this front-end. Bench-top and in-vitro measurements are presented in Section IV. Section V concludes this paper.

II. Recording Front-End Architecture

Closed-loop neuromodulation systems are subject to various constraints on input range, noise, power consumption, input dc offset rejection, and input dc impedance. As discussed in Section I, the front-end needs to reach a linear-input-range of 50–100 mV. The noise of the recording front-end should be on the order of a few microvolts for high-fidelity neural feature extraction. The input range and the noise constraints imply that a DR of 80 dB is required from the front-end. The front-end power consumption is required to be less than 10 μW per channel for an uninterrupted recording duration of several days. This power consumption also ensures that the generated heat flux does not cause necrosis [28]. The front-end dc offset, resulting from the polarization at the electrode-electrolyte interface, can range up to ± 50 mV at the electrode and can significantly reduce the voltage headroom of the front-end. Hence, these offsets need to be filtered out with a high-pass filter (HPF). Since the frequency band of the LFP signals extends as low as 1 Hz, the corner frequency of the HPF should be less than 1 Hz. To prevent electrode corrosion and tissue damage, the dc input impedance of the front-end needs to be larger than 100 MΩ. Tissue damage occurs when large dc currents flow in the electrodes due to offset voltages created by electrode polarization [22]. An input impedance of >100 MΩ with the dc offset within ± 50 mV limits the electrode dc current to <1 nA, which ensures a safe electrode–tissue interface. The specifications discussed earlier are also summarized in Table I.

TABLE I
Front-End Specification for Closed-Loop Neuromodulation

Specifications	Target Value
Integration noise (1 Hz-200 Hz)	< 10 μVrms
Input range	50—100 mV
Dynamic Range	80 dB
Power consumption	< 10 μW/ch
HPF corner for DC offset rejection	< 1 Hz
DC input impedance	> 100 MΩ

Unfortunately, the state-of-the-art neural-recording front-end designs do not provide the input range required for closed-loop neuromodulation systems. In most of these systems, a high-gain instrumentation amplifier (IA) is used after the electrode followed by a moderate resolution (9–11 b) analog-to-digital converter (ADC) [15], [17]–[20], [23]. The high gain (40–60 dB) of the IA relaxes the noise requirement for the following stages, thus reducing the power consumption for achieving a given input-referred noise performance. The ADC is usually chosen to be a SAR-ADC for its superior power efficiency. However, a high gain for the IA implies that the front–end will saturate for large input swings. Therefore, there is an inherent tradeoff between the input range requirement and the voltage gain in a voltage/current domain neural-recording front-end. When designed for a low input referred noise, the circuit has a limited input range. Therefore, the large stimulation artifacts would saturate the IA and render it impossible to recover neural signals. Moreover, since a DR in excess of 80 dB is required in the presence of stimulation artifacts, the ADC resolution needs to be greater than 12 b. The commonly used SAR-ADC is ill-suited for such a high resolution due to limited capacitor matching available in modern CMOS processes.

There are some recent works that try to solve this input range/gain tradeoff in the voltage domain. In [39], a frequency-shaping amplifier architecture is proposed to lower the gain at low frequencies so as to allow a larger DR without adding the complexity to the ADC design. This approach is equivalent to attenuating the low-frequency signal at the input and, therefore, leads to a sharp rise of the input-referred noise PSD at low frequencies. The high-frequency components of the artifacts may still saturate this front-end. Despite a high power consumption, its noise and linearity performance are not sufficient. Another possibility is to lower the front-end gain while designing an ADC with much higher effective resolution, which is typically

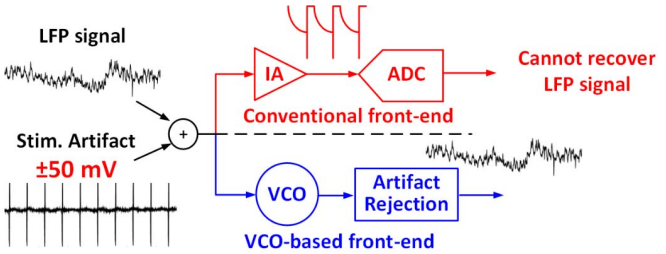


Fig. 2. Conventional front-end is saturated at the present of stimulation artifacts and cannot recover LFP signals. The VCO-based front-end allows full capture of LFP signals and stimulation artifacts.

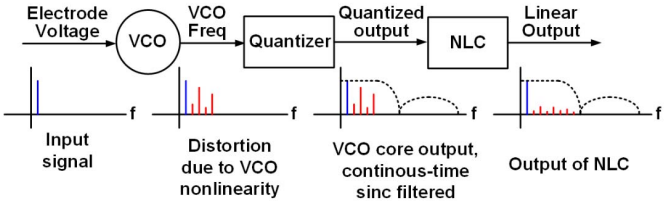


Fig. 3. Proposed front-end architecture: a cascade of VCO, quantizer, and NLC block.

an oversampled ADC. Yet such a design choice pushes the linearity/noise requirement onto the feedback DAC of the ADC and also typically requires a precise op-amp, resulting in a significantly higher power consumption than SAR-ADC.

Instead of processing the input signal in the voltage domain, we propose to directly convert the input voltage into the frequency domain using a voltage-controlled oscillator (VCO) [24], [25]. The converted VCO frequency is quantized by counting the phase increment of the VCO in a given time window within every sampling period. In modern CMOS processes, the VCO can provide a high voltage-to-frequency gain (K_{vco}) over a large input range. Given the low sampling rates required for an LFP front-end, the digitization can easily provide a high resolution (SQNR), rendering a low quantization noise while retaining a high input range. Therefore, VCO can be directly applied at the input without any preamplification, to capture both neural signals and stimulation artifacts. The quantized output is then fed to adaptive, blind-source artifact rejection algorithms to recover LFP signals, as shown in Fig. 2. Thus, the VCO-based design paradigm fundamentally overcomes the input noise versus input range tradeoff in previous neurorecording front-end designs, enabling the possibility of closed-loop neuromodulation. The phase counting is confined in the window instead of a whole period to avoid the transient due to the the chopping technique that will be discussed in Section III. In this manner, the phase measurement in one period does not carry the quantization error from the previous period. Therefore, our use of VCO for this application does not possess the inherent first-order noise-shaping feature that has been exploited in previous VCO-based general-purpose ADC designs [26], [27], [35].

To guarantee high recording sensitivity within a high DR, a careful treatment of the VCO circuit noise and nonlinearity is needed for fully exploiting the high SQNR provided by the VCO front-end. The VCO noise, which is dominated by flicker noise, is optimized by proper transistor sizing and the chopping technique that will be discussed in Section III. VCO nonlinearity is mitigated using foreground digital correction. In general, foreground correction is susceptible to coefficient drift. However, for the case of correcting the VCO nonlinearity for neural recording, foreground correction is acceptable for the following reasons.

1) Most of the nonlinearity from a VCO is attributed to its nonlinear voltage-to-frequency tuning curve, which is time invariant. Provided that the VCO-ADC maintains monotonicity in its transfer function, this nonlinearity can be corrected by learning and inverting the VCO tuning curve.
2) Implanted neural recording systems, being inside the body, operate at stable and well-regulated temperatures. Moreover, given the low current that neural-recording front-ends draw from the design, it is very easy to design an LDO for them that have a high power-supply rejection. With a well-controlled temperature and supply, the VCO nonlinearity remains time invariant and can be accurately corrected using a one-time measurement.
3) In modern CMOS processes, digital correction logic at the kilohertz rate required for neural recording can be synthesized with a few microwatts of power. We will discuss the digital correction logic in further detail in Section III.

In this design, the foreground correction is implemented via a fifth-order polynomial that inverts the VCO tuning curve, therefore correcting the VCO nonlinearity. Compared with previously reported background VCO correction algorithms [36], [37], it does not need the replica VCO and look-up table (LUT), which takes extra area. The details of the polynomial algorithm implementation are presented in Section III-C.

III. Circuit Implementation Details

The proposed front-end is a cascade of three blocks, as shown in Fig. 3: the VCO, the quantizer, and the NLC block. In this section, we shall discuss the circuit implementation for each of these modules.

A. VCO Design

The front-end uses a differential current-starved VCO architecture, as shown in Fig. 4. The differential structure is chosen for a good common-mode rejection ratio (CMRR) provided that the tail current source, as constructed by long-channel transistors, is biased in the saturation region. The bias current, directly related to K_{vco}, remains stable and does not change by more than 0.6% within a ±50-mV change in the input common-mode voltage. The dc offset in the signal is rejected by the RC HPF. The diff pair (M1/M2) converts the high-pass filtered input differential voltage into a differential current. To provide maximum K_{vco}, no degeneration is introduced at the source side of the diff pair transistors. The differential current is chopped by a commutating switch at the chopping

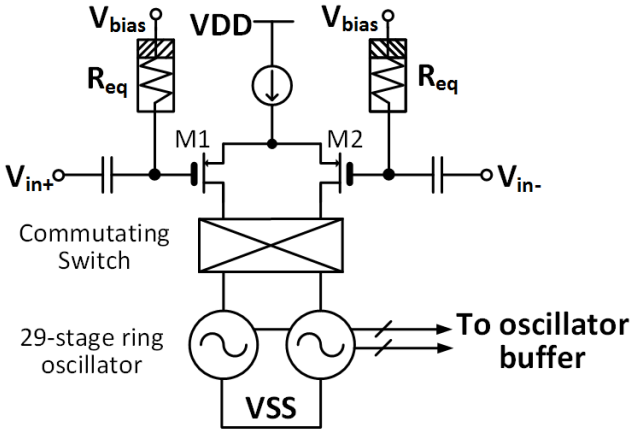


Fig. 4. VCO schematic.

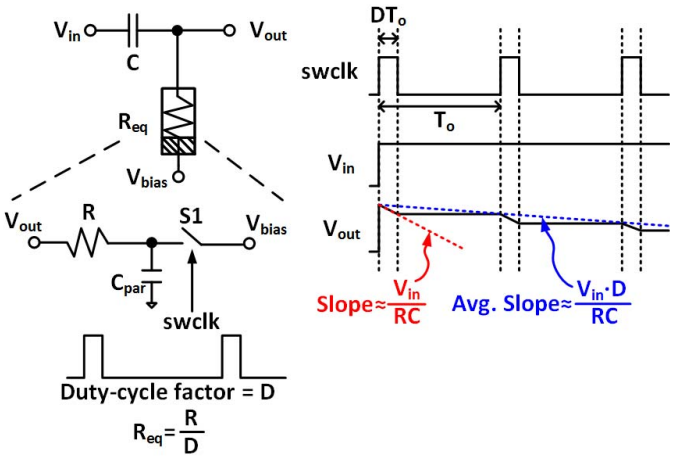


Fig. 5. HPF employing the duty-cycled resistor. The HPF output transient with input step function is demonstrated for intuitive understanding.

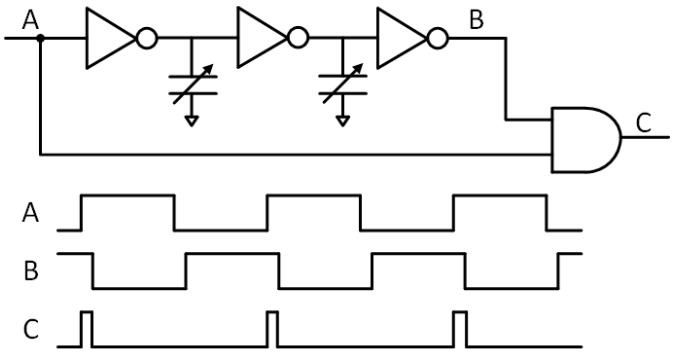


Fig. 6. Schematic and timing diagram for *swclk* generation for duty-cycle resistor.

frequency (f_{chop}) before being fed into the two ring oscillators (ROs). The input differential voltage is thus converted to the frequency difference of two ROs. This diff-pair-based VCO topology, with sufficient local decoupling capacitance and low-resistance supply network, also eliminates the possible interchannel interference due to oscillator switching that is a concern for multichannel sensing, easing the requirement for LDO design in the system.

As stated in Section II, the input HPFs need to have a corner frequency of less than 1 Hz. With an acceptable on-chip capacitor size of around 100 pF, the corresponding resistance has to be significantly larger than 1 GΩ. However, the noise requirement sets an even higher requirement for the resistance value. The integrated noise contributed by the HPF, when the signal band is beyond the HPF corner frequency, is

$$V_{n,\text{HPF}}^2 = \int_{f_{\text{Lo}}}^{f_{\text{Hi}}} \frac{4\text{kTR}}{1+(2\pi f RC)^2} df \approx \int_{f_{\text{Lo}}}^{f_{\text{Hi}}} \frac{4\text{kTR}}{(2\pi f RC)^2} df$$
$$= \frac{2\text{kT}}{\pi C} f_{\text{HPF}} \left(\frac{1}{f_{\text{Lo}}} - \frac{1}{f_{\text{Hi}}} \right) \approx \frac{2\text{kT}}{\pi C} f_{\text{HPF}} \frac{1}{f_{\text{Lo}}}$$

where f_{HPF} is the HPF corner frequency and f_{Lo} is the lower bound of the signal band. For $C = 100$ pF and $R = 10$ GΩ, the corner is set to $f_{\text{HPF}} = 0.16$ Hz, and with $f_{\text{Lo}} = 1$ Hz, $V_{n,\text{HPF}}$ is about 2 μV. Therefore, the resistance should be no less than 10 GΩ.

This extremely high resistance has been realized in prior art using pseudoresistors [28]. Although pseudoresistors can achieve high small-signal resistances of >100 GΩ, the pseudoresistor-based design has two major disadvantages. The leakage of the pseudoresistor can create an unpredictable offset across the pseudoresistor, making it difficult to accurately set a bias voltage (V_{bias}). For a differential design with HPFs for each input, the mismatch of the pseudoresistor leakage will cause an unknown offset across the diff pair input. This offset can significantly degrade the CMRR and power supply rejection ratio (PSRR). Also, the pseudoresistor being inherently nonlinear can lead to rectification and intermodulation of signals. These distortions cannot be easily corrected due to the time constant associated with the HPF.

To eliminate these problems arising from the pseudoresistor, we adopt a duty-cycled resistor to achieve large resistances for the HPF over a large input range [29]–[31]. As shown in Fig. 5, the duty-cycled resistor consists of a conventional resistor in series with a switch, which is controlled by a clock (*swclk*) signal with a duty-cycle factor D. The equivalent resistance of the duty-cycled resistor is $R_{\text{eq}} = R/D$. The resistance boosting obtained from the duty-cycled resistor is intuitively explained in Fig. 5, by examining the HPF output for a step function input following the transient analysis approach [29]. When the switch (S1) is ON, the HPF behaves like a linear RC filter. The slope of the output signal is approximately V_{in}/RC. While the switch is OFF, no charge can flow out of the capacitor, and thus, the output voltage is held constant. With a duty-cycle factor D, the average slope of the filter output is $V_{\text{in}}D/RC$. Hence, this filter response can be interpreted as an equivalent HPF with a time constant of RC/D, which implies an effective resistance $1/D$ times the original value. This allows us to synthesize large equivalent resistances by choosing a small duty cycle. The maximum resistance that can be achieved is limited by the parasitic capacitor C_{par} appearing on the switch and the resistor. While the output ideally is held constant when the switch is OFF, it actually continues to change because of charge sharing between C and C_{par}. The upper limit of the resistance is thus $1/fC_{\text{par}}$, which can be set high enough by minimizing the switch and resistor size.

The generation circuitry of *swclk* signal is shown in Fig. 6. The input clock signal is first delayed by a delay line composed of inverters and tunable capacitors. This delayed signal is then

inverted and fed to an AND gate with the original clock signal. The output is a derived clock with the same frequency as the input clock and an ON-pulse duration equal to the delay-line delay. The duty-cycle factor D can be easily around 0.01%, for a clock frequency of a few kilohertzes to tens of kilohertz and a delay-line delay of several nanoseconds. The *swclk* signal then controls the duty-cycle switch, which is implemented as a minimum-size thick-oxide nMOS transistor to minimize C_{par} while avoiding the gate leakage in thin-oxide core devices. This results in >10-GΩ effective resistance with a 1 MΩ or lower unsilicided polysilicon resistor. It shall be noted from [30, eq. (8)] that the noise contribution from the duty-cycled resistor-based HPF approximates that of a HPF built by R_{eq} and C. Thus, >10-GΩ equivalent resistance is sufficient for our noise requirement.

MOSFETs M1 and M2 in the differential pair are also chosen as thick-oxide transistors to avoid gate leakage currents, which could affect the input dc bias and alter the HPF response. M1/M2 are sized considering the noise, linearity, and matching requirements, given a current budget of 2.5 μA. To reduce the input-referred thermal noise in a power-efficient manner, it is desired to bias the diff pair devices in weak inversion to achieve a high g_m/I_D. However, an aggressive reduction of the overdrive voltage (V_{OV}) would lead to strong high-order distortions for large differential inputs, which can be difficult to correct. We found that that biasing M1/M2 with a V_{OV} of ~80 mV can ensure that the sixth-order and higher order nonlinearity are negligible within ±50-mV input range. The flicker noise and matching requirement dictates the minimum area of the input transistors. Large transistor area reduces the diff pair flicker noise contribution and provides better matching for CMRR and PSRR. Conversely, the transistor-area higher bound is set by the maximum allowable gate capacitance of M1/M2. The in-band signal is attenuated due to the impedance division between the M1/M2 gate capacitance and the HPF capacitance, and such attenuation directly worsens the front-end noise performance. M1/M2 are sized as $W = 15$ μm and $L = 30$ μm for an input-referred offset within 1 mV and corresponding CMRR and PSRR of around 70 dB from Monte Carlo simulations over 100 iterations. The transistor gate capacitance is around 10 pF, ten times smaller than the capacitor used in the HPF. The resulting input-referred noise degradation is <1 dB.

The VCO is implemented as a 29-stage RO that has simple CMOS inverters as the delay stages. The inverters oscillate between ground and around 0.45 V for a bias current of 1.25 μA. A relatively high number of stages is chosen for the RO in order to reduce the flicker-noise translated phase noise [32]. However, increasing the number of stages complicates the phase decoder design. We identified 29 stages to be a suitable tradeoff between phase decoder complexity and phase-noise reduction. To minimize the translation of flicker noise in the voltage domain to the frequency domain, the inverter stage is designed for equal rise and fall times in the typical process corner [33]. To further reduce the flicker noise, the devices used in the inverter stages are sized to occupy a large area. The RO output is fed into a buffer array operating on a digital supply also at 0.45 V.

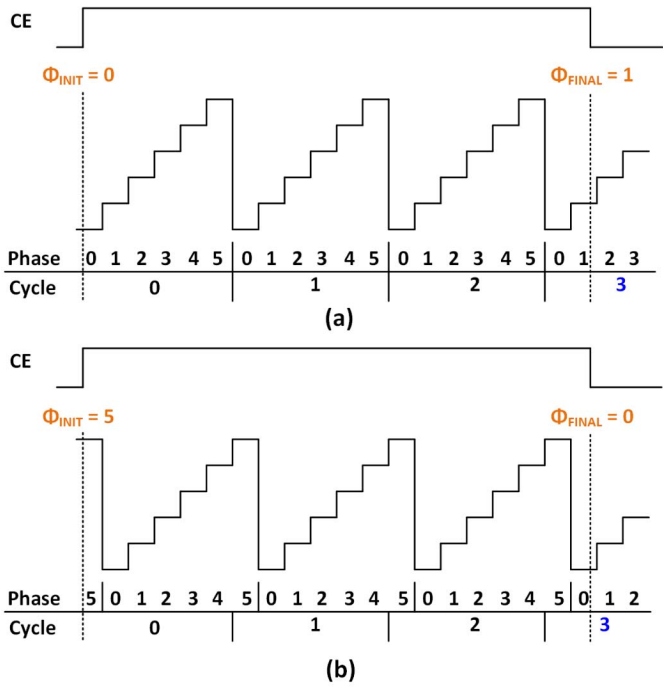


Fig. 7. Explanation of phase counting with an example of three-stage RO. (a) Positive phase difference and (b) negative phase difference conditions are accounted.

In spite of these design choices to reduce close-in phase noise of the RO, it can still significantly influence the system noise performance, especially with process variations when the inverter stage has unequal rise and fall time. To avoid signal degradation due to this noise, a commutating switch is placed in-between the diff pair and ROs to chop the differential current. The chopping frequency f_{chop} is equal to the sampling frequency, with one chopping period containing a positive phase and a negative phase controlled by signals *Sp* and *Sn*, respectively (refer to Fig. 10). The two phases are overlapping for 1–2 μs to ensure that a conducting path is always available for the diff pair current. By commutating the current flowing into the two ROs, the input signal is modulated up to around f_{chop} and its odd harmonics, as shown in Fig. 11(b) and (c). It is separated from the flicker noise of the RO in the frequency domain. The following quantizer can demodulate the input signal back to baseband and filter out the flicker noise of the RO.

B. Quantizer Design

The quantizer counts the VCO phase increment within a window by combining the RO cycle count and the phase information decoded from the RO outputs. Its principle is exemplified in Fig. 7, with a three-stage RO and the *CE* signal that defines the window. At the rising edge of the *CE* signal, the phase decoder decodes the initial phase from the three-stage outputs, referred to as Φ_{INIT}. The quantizer also begins counting the number of cycles using a counter. The input to the counter is selected from the three available RO outputs, using the information from Φ_{INIT}. This choice of the input to the cycle counter ensures that counting begins from

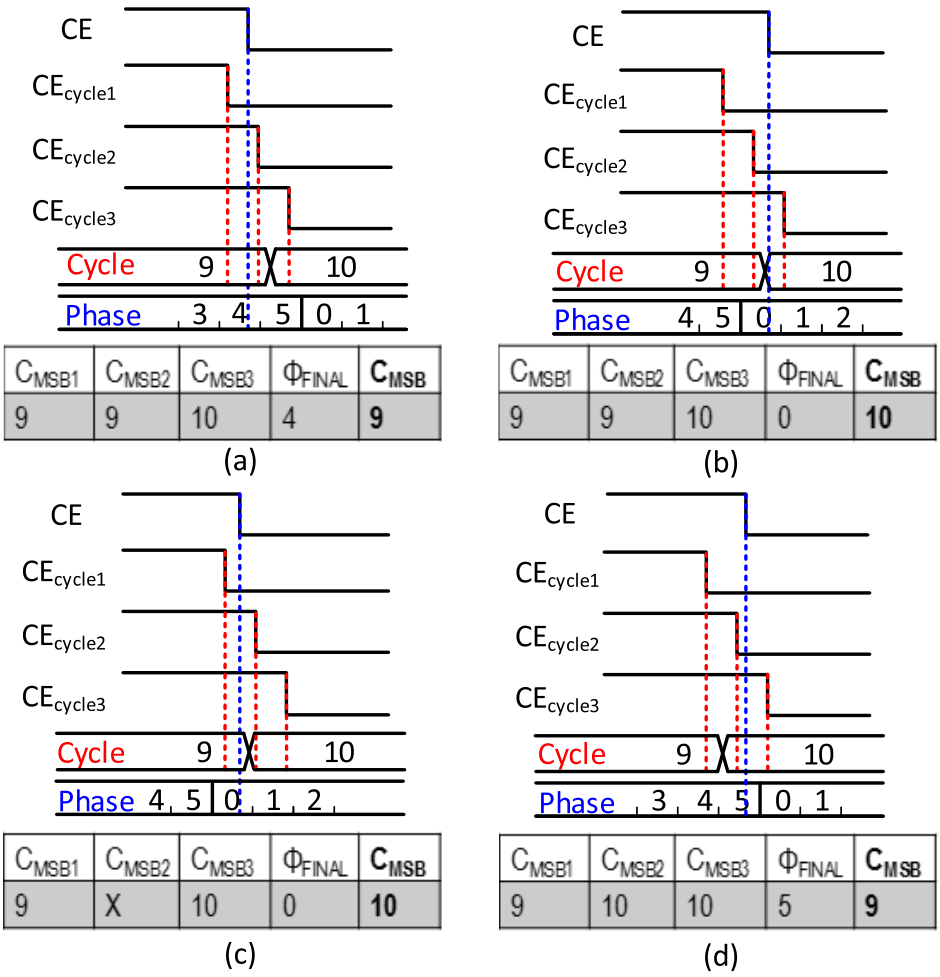


Fig. 8. Decision of C_{MSB} based on three sampled counter outputs under different situations. For simplicity, we assume $\Phi_{\mathrm{INIT}} = 0$ (generally phase difference is inspected instead of Φ_{FINAL} only). (a) $C_{\mathrm{MSB1}} = C_{\mathrm{MSB2}} \neq C_{\mathrm{MSB3}}$, $\Phi_{\mathrm{FINAL}} > 3$, $C_{\mathrm{MSB}} = C_{\mathrm{MSB1}}$; (b) $C_{\mathrm{MSB1}} = C_{\mathrm{MSB2}} \neq C_{\mathrm{MSB3}}$, $\Phi_{\mathrm{FINAL}} < 3$, $C_{\mathrm{MSB}} = C_{\mathrm{MSB1}} + 1$; (c) $C_{\mathrm{MSB1}} \neq C_{\mathrm{MSB2}}$, $\Phi_{\mathrm{FINAL}} < 3$, $C_{\mathrm{MSB}} = C_{\mathrm{MSB3}}$; (d) $C_{\mathrm{MSB1}} \neq C_{\mathrm{MSB2}} = C_{\mathrm{MSB3}}$, $\Phi_{\mathrm{FINAL}} > 3$, $C_{\mathrm{MSB}} = C_{\mathrm{MSB3}} - 1$.

the most recent transition edge of RO. At the falling edge of the *CE* signal, the phase is decoded as Φ_{FINAL} and the cycle counter output is sampled as C_{MSB}. The phase difference between Φ_{FINAL} and Φ_{INIT}, either positive or negative, will be corrected by a modulo operation, because the actual phase difference is always positive according to our selection of the cycle counter input. Thus, the phase traversed by the RO is given by

$$\text{Total Phase} = 2N \cdot C_{\mathrm{MSB}} + \mathrm{mod}\left(\emptyset_{\mathrm{FINAL}} - \emptyset_{\mathrm{INIT}}, 2N\right)$$

where N is the number of RO stages. The traversed phase as calculated gives 19 for both initial conditions in Fig. 7(a) and (b).

The quantizer needs to resolve potential errors due to the cycle/phase sampling misalignment and the metastability when employing this equation. Since the cycle count and the final phase cannot be perfectly sampled at the same time, a ± 1 cycle count error can occur in the scenario when the *CE* falling edge is close to the counter transition edge. More severely, the metastability can also occur in this scenario, which gives an erroneous cycle count. To avoid these errors, the cycle counter output is sampled three times using sampling edges derived from the *CE* signal, as shown in Fig. 8: one edge (CE_{cycle1}) is an advanced version of the *CE* signal, and the second edge (CE_{cycle3}) is a delayed version of *CE*. The third sampling edge (CE_{cycle2}) sits between CE_{cycle1} and CE_{cycle3}. If the *CE* falling edge is away from the counter transition edge, the three sampled counter outputs (C_{MSB1}, C_{MSB2}, and C_{MSB3}) will be the same. If these three samples are different, only one sample may be captured in the metastability region. The other two samples are either the same or differ by one. The decision of choosing C_{MSB} between these two samples, if they differ by one, is based on the phase difference, which is $\mathrm{mod}(\emptyset_{\mathrm{FINAL}} - \emptyset_{\mathrm{INIT}}, 2N)$. If the phase difference is larger than N, the smaller sample output is chosen as C_{MSB}. On the other hand, the larger sample output is chosen when the phase difference is smaller than N. Fig. 8 demonstrates the decision of C_{MSB} from the three sampled outputs at four different situations, with situation [Fig. 8(c)] showing C_{MSB2} in metastability. This triple-sampling technique needs no redundancy in the relatively high-speed cycle counter path and, therefore, has potentially better power efficiency compared with the technique proposed in [38].

A schematic of the quantizer for our RO is shown in Fig. 9. Φ_{INIT} is fed to a multiplexer (MUX) to select the

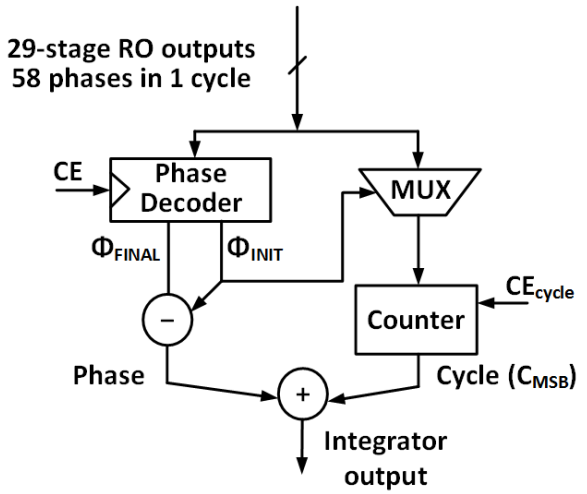


Fig. 9. RO quantizer schematic.

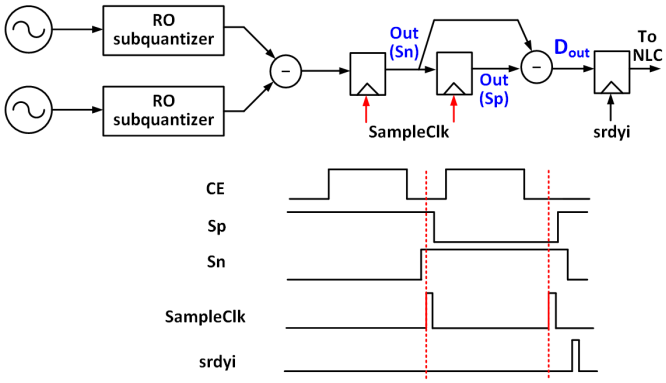


Fig. 10. Whole VCO quantizer schematic with timing diagram. Signals at the rising edge of *srdyi* are labeled.

desired input for the cycle counter from the 29 available outputs of the RO. The counter output is sampled by the CE_{cycle} signal, which represents an ensemble of the three derived signals from *CE*. The phase information and the cycle information are then combined to determine the total phase increment of the RO during the counting window.

The whole VCO quantizer schematic, as shown in Fig. 10, contains two subquantizers for each RO. The two subquantizer outputs are subtracted to determine the phase increment of the whole VCO during the window. To invert the chopping operation of the commutating switch in the VCO (refer to Fig. 4), the front-end implements two equal-duration counting windows within one sampling period, one for the positive phase and one for the negative phase, as defined by the *CE* signal. The windows are positioned with sufficient margin away from the transition of the two phases, as shown in Fig. 10, to allow the settling of the chopping transient before the phase counting begins. The VCO phase increments during the two windows are latched at two *SampleClk* rising edges. After the second *SampleClk* rising edge, the two latched values are subtracted to demodulate the input signal back to baseband. The result D_{out} represents the sampled value of the VCO frequency for the whole period. The subtraction of the two phase outputs also introduces a filter to any noise added by

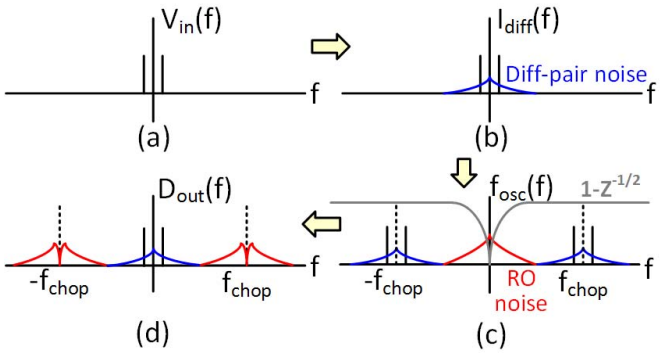


Fig. 11. Input signal and diff-pair noise are modulated up around f_{chop} when converted to the frequency difference. The quantizer demodulates the signal while notching out the RO-induced noise. (a) Input voltage power spectrum. (b) Power spectrum of differential current. (c) Power spectrum of the frequency difference. (d) Digital output power spectrum.

the RO, with a transfer function of $1-z^{-\frac{1}{2}}$. This high-pass transfer function filters out the RO-induced flicker noise before modulating it away from the signal band, as shown in Fig. 11(c) and (d).

The quantizer output can have high enough resolution for the DR specification of 80 dB when combining both the cycle and phase information. The VCO gain K_{VCO} is about 150 MHz/V. The front-end sampling frequency of 3 kS/s allows two counting windows of ~100 μs within one sampling period, which sum to a total counting time T_{sample} of 200 μs. The quantized output range is

$$\begin{aligned} &K_{\text{VCO}} \cdot 2N \cdot T_{\text{sample}} \cdot V_{\text{pp}} \\ &= 150\ \text{MHz/V} \times 2 \times 29\ \text{stages/cycle} \times 200\ \mu\text{s} \times 100\ \text{mV} \\ &= 174\,000 \end{aligned}$$

for a peak input of ±50 mV, which is equivalent to 17.4 b. Thus the output quantization noise level is kept sufficient low.

The phase counting for 200 μs, corresponding to a sinc filter bandwidth of ~2.5 kHz, allows the capture of major distortion terms unattenuated while suppressing the high-frequency noise. Input LFP signals, spanning 1–200-Hz frequency range, will cause distortions ≤1-kHz frequency for nonlinearities up to the fifth-order term. The distortion terms sit in the sinc filter passband, thus allowing the following NLC block to accurately invert the VCO nonlinearity.

C. NLC Design

The NLC block receives the quantizer output and applies a polynomial function to correct for the VCO nonlinearity. The VCO is designed such that a fifth-order polynomial is sufficient to correct for the VCO nonlinearity within the specified ±50-mV input range. The general form of our fifth-order polynomial is the following:

$$\begin{aligned} y[n] = a_0 + a_1 x[n] + a_2 x[n]^2 + a_3 x[n]^3 \\ + a_4 x[n]^4 + a_5 x[n]^5 \end{aligned}$$

where $x[n]$ is the NLC input sample, a_0–a_5 are the polynomial coefficients, and $y[n]$ is the NLC output. For better accuracy, we use single-precision floating-point operations to

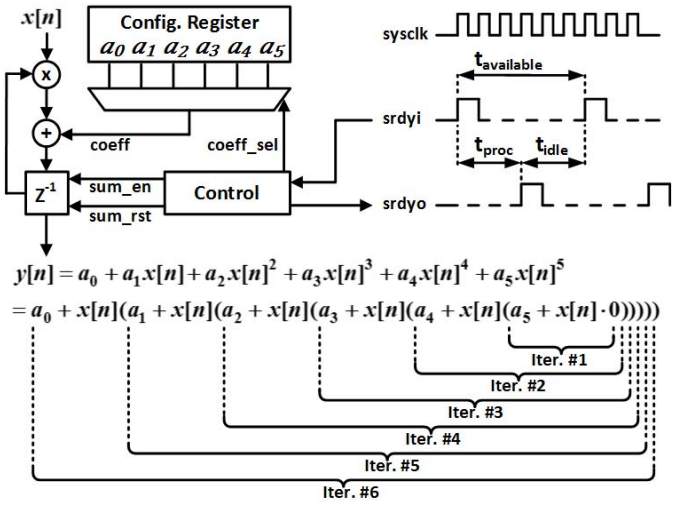


Fig. 12. NLC implementation.

compute the polynomial. A straight-forward implementation would require too many floating-point multipliers that take up significant area even in an advanced technology node. Noticing that the sampling rate of the quantizer is very low, a tradeoff of execution time and area can be made in our favor by adopting Horner's method, which allows iterative computation of a polynomial using a single multiplier-accumulator (MAC) kernel. With Horner's method, our polynomial can be rewritten as

$$y[n] = a_0 + x[n](a_1 + x[n](a_2 + x[n](a_3 + x[n] \times (a_4 + x[n](a_5 + x[n] \cdot 0))))).$$

Thus, $y[n]$ can be computed starting with the innermost MAC operation $a_5 + x[n] \cdot 0$, then expanded outward until the whole polynomial is computed.

The schematic representation of the implementation is shown in Fig. 12. When the quantizer output is ready, the raw sample $x[n]$ is sent to the NLC engine and the input valid (*srdyi*) signal is asserted for one clock cycle. The engine then starts the first iteration, where it multiplies the input sample $x[n]$ with the accumulator register content (which is initialized to 0), adds the fifth-order coefficient a_5 to it, and stores the result back into the accumulator register. In the second iteration, the input $x[n]$ is multiplied with accumulator register content (which is now nonzero); the fourth-order coefficient a_4 is added, and the result is stored into the accumulator register again. This process continues until the whole polynomial $y[n]$ is computed. After the last iteration (sixth iteration) is complete, the output valid (*srdyo*) signal is asserted to indicate that the nonlinearity corrected sample is now ready. This iterative polynomial solution with only one MAC kernel reduces the NLC area to be much smaller than the classical LUT approach, as will be shown in Section IV.

IV. Measurement Results

The chip was fabricated in the TSMC 1P10M 40-nm GP CMOS technology. The chip micrograph is shown in Fig. 13.

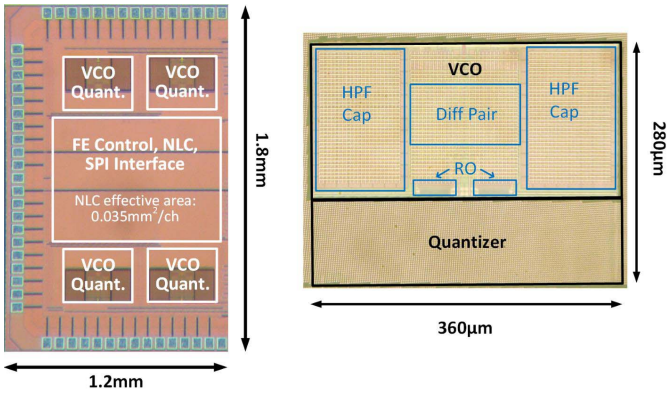


Fig. 13. Chip micrograph.

Four front-ends have been implemented. The VCO block and the quantizer block have been laid out together for each front-end. The NLC block for four front-ends is synthesized, placed-and-routed together in the center of the chip, with a shared control module for the front-ends and the SPI interface to read out the front-end output data. To simplify top-level routing, the NLC and control modules are spread out in the center of the chip to allow short and direct connections between these modules and the VCO front-ends. The effective NLC area is around 0.035 mm^2 per channel due to the area-efficient implementation. This is ten times smaller than the area of the LUT approach with $2^{17.4}$ words and 15 b of word length, assuming 0.124 μm^2 for a 6T SRAM cell [34].

The layout of the VCO and the quantizer is also shown in Fig. 13. The HPF capacitors, each of around 100 pF, take up most of the area in the VCO block. The diff pair is sized up to reduce flicker noise and mismatch. The layout is made symmetric for robust operation with differential inputs. The VCO and quantizer area is around 0.1 mm^2 per channel.

For this prototype chip, the bias voltage of the HPF is generated off-chip. The analog supply is set to 1.2 V to ensure enough voltage headroom for the stacking of the current source, the differential pair, and ROs, as shown in Fig. 4. The digital supply is 0.45 V for direct interfacing with the RO outputs. The bias current of the VCO is programmable from 0.5 to 4.5 μA, and the default value of 2.5 μA is used for the results presented in this section. The sampling rate of the front-end is also programmable over two decades of range, from 187.5 S/s to 24 kS/s, with a default value of 3 kS/s. Under the default conditions, the analog block consumes 3 μW and the digital switching power is about 4 μW. The digital leakage power is excessively high, on the order of 100 μW, due to the high leakage per gate in the GP process. However, moving the design to the LP process, which is more amenable for low-power application, will reduce the leakage by a 100-fold and resolve this issue without incurring penalties in other aspects. The total power is expected to be less than 10 μW in the LP process.

A. Benchtop Test Results

The front-end performance is tested by sending its digital output via an SPI interface to an FPGA board, which streams data to an external terminal. A dedicated software interface

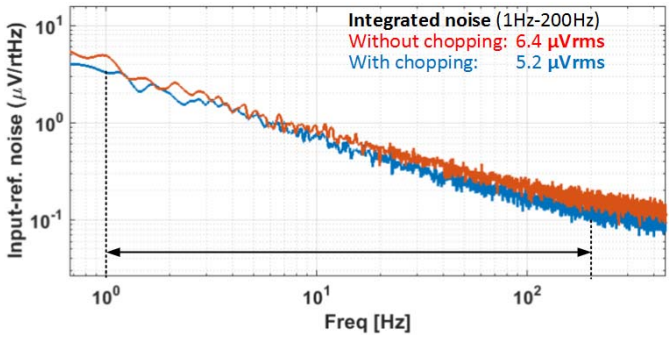


Fig. 14. Input-referred noise measurement.

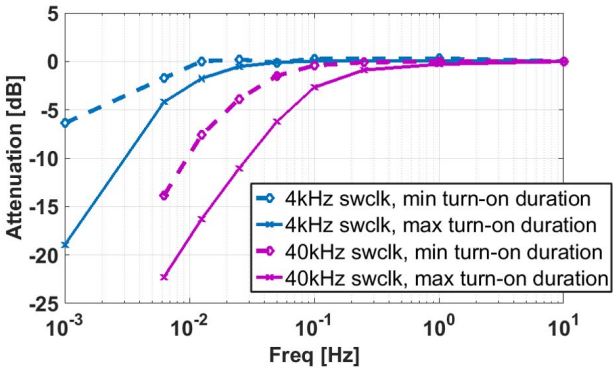


Fig. 15. Front-end frequency response for dc offset rejection.

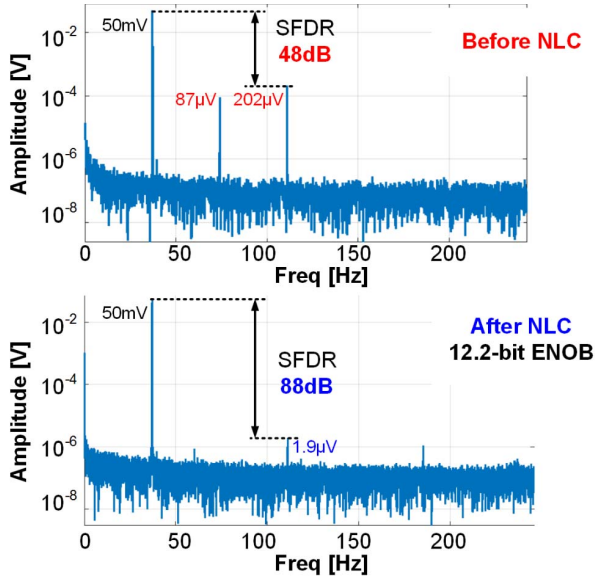


Fig. 16. Single-tone test for the front-end linearity, input amplitude of ±50 mV at 37 Hz.

is also developed to individually configure the sampling frequency, timing control, bias current, and so on, for each channel.

The measured noise spectral density for zero signal input is shown in Fig. 14. The input-referred noise PSD is calculated as the measured output PSD at zero input divided by the in-band front-end gain. The noise PSDs have been measured for both settings with and without the chopping technique, which are configured for similar in-band front-end gains. It can be seen that chopping brings down the noise and, therefore, reduces the input-referred noise integrated over 1–200 Hz for LFP acquisition from 6.4 to 5.2 μV_{rms}. The noise is dominated by

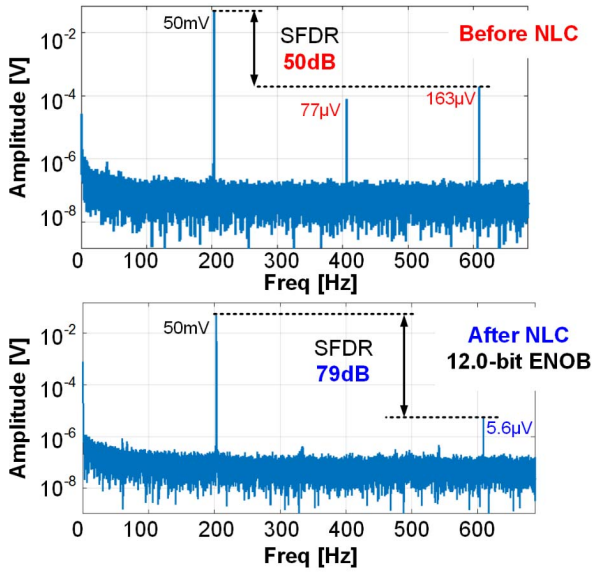


Fig. 17. Single-tone test for the front-end linearity, input amplitude of ±50 mV at 203 Hz.

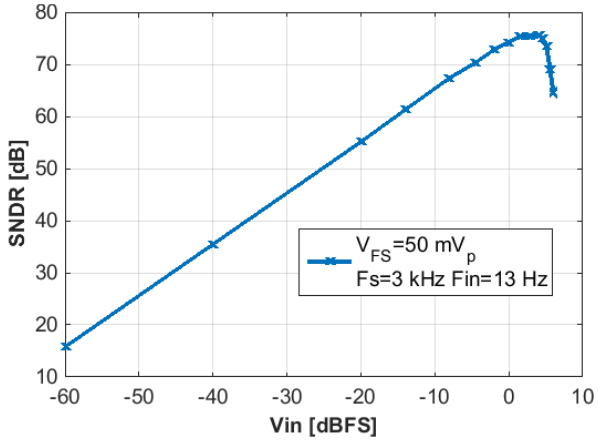


Fig. 18. SNDR versus input amplitude for 13-Hz input.

the flicker noise of the input diff pair and the low-pass filtered HPF noise. The noise improvement compared with the number reported in [25] is due to a more accurate noise-measurement setup.

The frequency selectivity of the front-end for dc rejection is measured by sweeping the frequency of the sine-wave input. The measured frequency response is shown in Fig. 15. The HPF corner can be tuned by changing either the *swclk* frequency or the turn-ON duration, both related to the duty-cycle factor D. It can be seen that the corner is below 0.1 Hz.

To calculate the polynomial coefficients of the NLC block, the raw output of the quantizer with a single-tone input is logged, while the NLC block is disabled. Using this raw data, the polynomial correction coefficients are derived by performing curve fitting. We then enable the NLC block with the derived coefficients, and log corrected outputs with inputs across the signal band. A single-tone input with ±50-mV amplitude is injected to gauge the harmonic distortion. It can be seen that the spurious-free dynamic range (SFDR) across the band is no less than 79 dB, as shown in Figs. 16 and 17.

TABLE II
COMPARISON WITH PRIOR WORK

Reference	[17] JSSC'07	[18] JSSC'12	[19] ISSCC'14	[40] JSSC'16	This work
Topology	CCIA (no ADC)	Diff Amp + ADC	Chop. Amp + ADC	Chop. Amp + MADC	**Direct digitization VCO with NLC**
Signals	LFP	Spike/LFP	LFP	Spike/LFP	**LFP**
Technology	0.8um	65nm	65nm	0.13µm	**40nm**
Supply	1.8V	0.5V	0.5V	1.2V	**1.2V** (Analog) **0.45V** (Digital)
Area/ch	1.7 mm^2	0.013 mm^2	0.025 mm^2	0.018 mm^2	**0.135 mm^2**
Power/ch	2µW	5.04µW	2.3µW	9.1µW	**3µW** (Analog) **4µW** (Dig. sw.)
In-ref. Noise	1µV	4.3µV	1.3µV	4.2µV	**5.2µV**
Integrated Noise BW	0.05-100 Hz	10-300 Hz	1-500 Hz	1-1k Hz	**1-200 Hz**
Peak Input	5mVp	3.5mV	±0.5mV	1mVpp	**±50mV**
SFDR	60dB	40dB	52dB	50dB	**79dB**
ENOB	11.0*	8.0*	7.8	7.1	**12.0**
CMRR	>80 dB	75 dB	88 dB	69.2 dB	**66 dB****
Z_{in}(DC)	8MΩ	∞	28MΩ	∞	**∞ (100pF)**

* ENOB is derived by backing off the signal amplitude to the point where the distortion and noise contributions are equal.
** The measured CMRR is lower than the Monte-Carlo simulation result because of the mismatch between two HPFs.

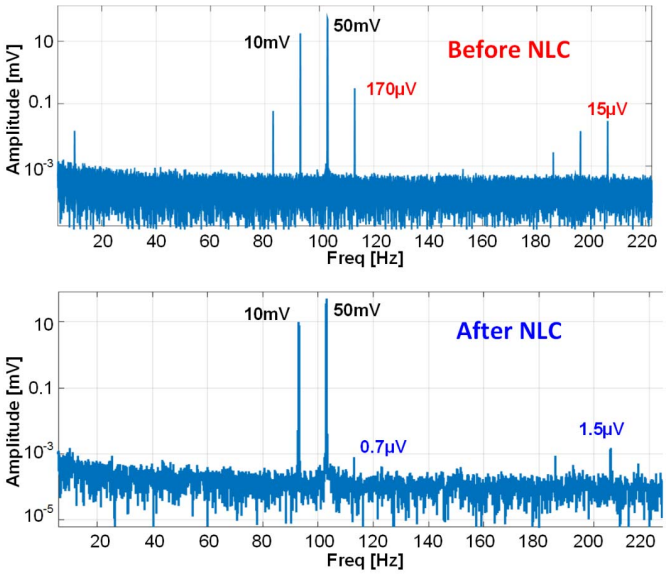


Fig. 19. Two-tone test results for an interferer of ±50 mV at 103 Hz and a signal of ± 10 mV at 93 Hz.

The degradation of SFDR at 203 Hz, with curve-fitting coefficients derived at a low frequency, can be due to the residual frequency-dependent nonlinearity and the window filtering effect due to phase counting. The measurement confirmed that the SFDR remains >75 dB when the HPF bias voltage deviates within ±50 mV from the bias point used to determine polynomial coefficients. This indicates the robustness of the front-end linearity performance against the input CM voltage fluctuation.

The SNDR verses input amplitude is shown in Fig. 18. It can be seen that under a full scale of ±50 mV, the SNDR increases proportionally with the input amplitude. When the amplitude increases beyond the full scale, the SNDR almost levels off until 3 dBFs and then degrades rapidly due to hard nonlinearity.

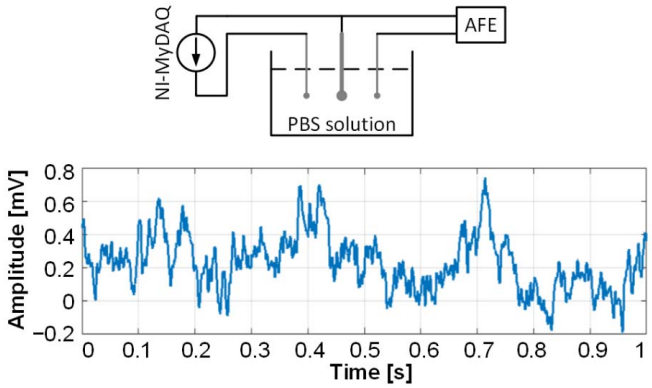


Fig. 20. *In vitro* test setup and recorded signal.

A two-tone test is also performed to evaluate the intermodulation distortion of the front-end. To mimic a realistic situation, the two tones are selected to be an interferer of ±50 mV at 103 Hz and a signal of ± 10 mV at 93 Hz. It can be seen in Fig. 19 that when bypassing the NLC block, the intermodulation components can be as large as 170 μV and the harmonics are as large as 15 μV. The nonlinearity correction dramatically brings down the intermodulation term to less than 1 μV and the harmonics to 1.5 μV.

B. In Vitro Measurement

The front-end is also tested *in vitro* with electrodes in a PBS solution. An NI-myDAQ is used to emulate the LFP signal, which is prerecorded from a human patient. The recorded signal is shown in Fig. 20.

C. Comparison With Prior Work

Table II compares this paper to previous neural-recording front-ends. It can be seen that while complying with the power consumption and noise power specifications, this front-end achieves a peak linear input amplitude of ±50 mV, which is ten times the peak amplitude of prior art. The minimum SFDR is 79 dB across the signal band for an input of ±50 mV, which is 19 dB higher than the SFDR of prior designs. Since the front-end input is ac coupled, it naturally presents an infinite input dc impedance. The 10-pF input differential pair gate capacitance leads to a 5-pF input differential capacitance for in-band frequencies while the input impedance is dominated by a 100-pF HPF capacitor below the HPF corner frequency. Therefore, this front-end does not need an external dc-blocking capacitor at the input, which effectively reduces the overall area.

V. Conclusion

We have presented an LFP-recording front-end design for closed-loop neuromodulation. The front-end achieves a linear input range of ±50 mV, a decade larger than prior art, by employing the VCO-based topology directly at the input. It can record neural signals in the presence of large stimulation artifacts. The front-end features infinite input dc impedance and dc offset rejection by a HPF achieving a subhertz corner using a duty-cycled resistor.

Since the VCO-based recording front-end is digitally intensive, it is well suited for advanced CMOS technology with low supply rail voltage and can be integrated with additional digital processing and data communication modules for the implantable neuromodulation SoC.

Acknowledgment

The authors would like to thank Dr. I. Fried and Prof. N. Suthana, Neurosurgery Department, University of California at Los Angeles, for providing local-field-potential data for *in vitro* test, and Lawrence Livermore National Laboratory, for providing electrodes for *in vitro* test. The views, opinions, and/or findings expressed are those of the author and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government.

References

[1] *U.S. Leading Categories of Diseases/Disorders*. accessed on Feb. 25, 2016, [Online]. Available: http://www.nimh.nih.gov/health/statistics/disability/us-leading-categories-of-diseases-disorders.shtml

[2] R. Fisher *et al.*, "Electrical stimulation of the anterior nucleus of thalamus for treatment of refractory epilepsy," *Epilepsia*, vol. 51, no. 5, pp. 899–908, May 2010.

[3] W. Ondo, J. Jankovic, K. Schwartz, M. Almaguer, and R. K. Simpson, "Unilateral thalamic deep brain stimulation for refractory essential tremor and Parkinson's disease tremor," *Neurology*, vol. 51, no. 4, pp. 1063–1069, Oct. 1998.

[4] D. S. Husted and N. A. Shapira, "A review of the treatment for refractory obsessive-compulsive disorder: From medicine to deep brain stimulation," *CNS Spectrums*, vol. 9, no. 11, pp. 833–847, Nov. 2004.

[5] X. L. Chen, Y. Y. Xiong, G. L. Xu, and X. F. Liu, "Deep brain stimulation," *Intervent. Neurol.*, vol. 1, nos. 3–4, pp. 200–212, 2012.

[6] P. Gubellini, P. Salin, L. K.-L. Goff, and C. Baunez, "Deep brain stimulation in neurological diseases and experimental models: From molecule to complex behavior," *Prog. Neurobiol.*, vol. 89, no. 1, pp. 79–123, Sep. 2009.

[7] P. R. Burkhard, F. J. G. Vingerhoets, A. Berney, J. Bogousslavsky, J.-G. Villemure, and J. Ghika, "Suicide after successful deep brain stimulation for movement disorders," *Neurology*, vol. 63, no. 11, pp. 2170–2172, Dec. 2004.

[8] S. Marceglia, L. Rossi, G. Foffani, A. Bianchi, S. Cerutti, and A. Priori, "Basal ganglia local field potentials: Applications in the development of new deep brain stimulation devices for movement disorders," *Expert Rev. Med. Devices*, vol. 4, no. 5, pp. 605–614, Sep. 2007.

[9] A. Priori, G. Foffani, L. Rossi, and S. Marceglia, "Adaptive deep brain stimulation (aDBS) controlled by local field potential oscillations," *Experim. Neurol.*, vol. 245, pp. 77–86, Jul. 2013.

[10] G. Giannicola *et al.*, "Subthalamic local field potentials after seven-year deep brain stimulation in Parkinson's disease," *Experim. Neurol.*, vol. 237, no. 2, pp. 312–317, Oct. 2012.

[11] A. Abosch *et al.*, "Long-term recordings of local field potentials from implanted deep brain stimulation electrodes," *Neurosurgery*, vol. 71, no. 4, pp. 804–814, Oct. 2012.

[12] M. Arlotti, L. Rossi, M. Rosa, S. Marceglia, and A. Priori, "An external portable device for adaptive deep brain stimulation (aDBS) clinical research in advanced Parkinson's disease," *Med. Eng. Phys*, vol. 38, no. 5, pp. 498–505, 2016.

[13] S. Nanthia *et al.*, "Memory enhancement and deep-brain stimulation of the entorhinal area," *New England J. Med.*, vol. 366, no. 6, pp. 502–510, Feb. 2012.

[14] M. K. Lyons, "Deep brain stimulation: Current and future clinical applications," *Mayo Clinic Proc.*, vol. 86, no. 7, pp. 662–672, 2011.

[15] W.-M. Chen *et al.*, "A fully integrated 8-channel closed-loop neural-prosthetic CMOS SoC for real-time epileptic seizure control," *IEEE J. Solid-State Circuits*, vol. 49, no. 1, pp. 232–247, Jan. 2014.

[16] S. Stanslaski *et al.*, "Design and validation of a fully implantable, chronic, closed-loop neuromodulation device with concurrent sensing and stimulation," *IEEE Trans. Neural Syst. Rehabil. Eng.*, vol. 20, no. 4, pp. 410–421, Jul. 2012.

[17] T. Denison, K. Consoer, W. Santa, A. T. Avestruz, J. Cooley, and A. Kelly, "A 2μW 100 nV/rtHz chopper-stabilized instrumentation amplifier for chronic measurement of neural field potentials," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2934–2945, Dec. 2007.

[18] R. Muller, S. Gambini, and J. M. Rabaey, "A 0.013 mm^2, 5μW, DC-coupled neural signal acquisition IC with 0.5 V supply," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 232–243, Jan. 2012.

[19] R. Muller *et al.*, "A miniaturized 64-channel 225μW wireless electrocorticographic neural sensor," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2014, pp. 412–413.

[20] H. Gao *et al.*, "HermesE: A 96-channel full data rate direct neural interface in 0.13μm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 4, pp. 1043–1055, Apr. 2012.

[21] A. E. Mendrela, J. Cho, J. A. Fredenburg, C. A. Chestek, M. P. Flynn, and E. Yoon, "Enabling closed-loop neural interface: A bi-directional interface circuit with stimulation artifact cancellation and cross-channel CM noise suppression," in *Proc. IEEE VLSI Symp.*, Jun. 2015, pp. 108–109.

[22] T. Jochum, T. Denison, and P. Wolf, "Integrated circuit amplifiers for multi-electrode intracortical recording," *J. Neural Eng.*, vol. 6, no. 1, p. 012001, Jan. 2009.

[23] N. Verma, A. Shoeb, J. V. Guttag, and A. P. Chandrakasan, "A micropower EEG acquisition SoC with integrated seizure detection processor for continuous patient monitoring," in *Proc. IEEE VLSI Symp.*, Jun. 2009, pp. 62–63.

[24] V. Karkare, H. Chandrakumar, D. Rozgić, and D. Marković, "Robust, reconfigurable, and power-efficient biosignal recording systems," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2015, pp. 1–8.

[25] W. Jiang, V. Hokhikyan, H. Chandrakumar, V. Karkare, and D. Marković, "A ±50 mV linear-input-range VCO-based neural-recording front-end with digital nonlinearity correction," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2016, pp. 484–485.

[26] M. Z. Straayer and M. H. Perrott, "A 12-bit, 10-MHz bandwidth, continuous-time $\Sigma\Delta$ ADC with a 5-bit, 950-MS/s VCO-based quantizer," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 805–814, Apr. 2008.

[27] A. Sanyal, K. Ragab, L. Chen, T. R. Viswanathan, S. Yan, and N. Sun, "A hybrid SAR-VCO $\Sigma\Delta$ ADC with first-order noise shaping," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2014, pp. 1–4.

[28] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003.

[29] J. A. Kaehler, "Periodic-switching filter networks-a means of amplifying and varying transfer functions," *IEEE J. Solid-State Circuits*, vol. 4, no. 4, pp. 225–230, Aug. 1969.

[30] M. H. Perrott *et al.*, "A low area, switched-resistor based fractional-*N* synthesizer applied to a MEMS-based programmable oscillator," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2566–2581, Dec. 2010.
[31] H. Chandrakumar and D. Marković, "A 2μW 40mVpp linear-input-range chopper-stabilized bio-signal amplifier with boosted input impedance of 300MΩ and electrode-offset filtering," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2016, pp. 96–97.
[32] V. Karkare, "Robust, reconfigurable, and power-efficient electrophysiological recording systems," Ph.D. dissertation, Dept. Elect. Eng., Univ. California Los Angeles, Los Angeles, CA, USA, 2014.
[33] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 790–804, Jun. 1999.
[34] L. Chang *et al.*, "Stable SRAM cell design for the 32 nm node and beyond," in *Proc. IEEE VLSI Symp. Technol.*, Jun. 2005, pp. 128–129.
[35] P. Prabha *et al.*, "A highly digital VCO-based ADC architecture for current sensing applications," *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 1785–1795, Aug. 2015.
[36] G. Taylor and I. Galton, "A mostly-digital variable-rate continuous-time delta-sigma modulator ADC," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2634–2646, Dec. 2010.
[37] S. Rao, K. Reddy, B. Young, and P. K. Hanumolu, "A deterministic digital background calibration technique for VCO-based ADCs," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 950–960, Apr. 2014.
[38] J. Hamilton, S. Yan, and T. R. Viswanathan, "An uncalibrated 2MHz, 6mW, 63.5dB SNDR discrete-time input VCO-based $\Sigma\Delta$ ADC," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2012, pp. 1–4.
[39] J. Xu, T. Wu, W. Liu, and Z. Yang, "A frequency shaping neural recorder with 3 pF input capacitance and 11 plus 4.5 bits dynamic range," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 4, pp. 510–527, Aug. 2014.
[40] H. Kassiri *et al.*, "Battery-less tri-band-radio neuro-monitor and responsive neurostimulator for diagnostics and treatment of neurological disorders," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1274–1289, May 2016.

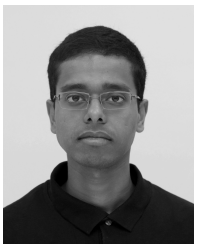
Wenlong Jiang received the B.E. degree in electronic engineering from Tsinghua University, Beijing, China, in 2009, and the M.Sc. degree (*cum laude*) in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 2011. He is currently pursuing the Ph.D. degree with the Department of Electrical Engineering, University of California at Los Angeles (UCLA), Los Angeles, CA, USA.

From 2010 to 2011, he was an Intern with Catena BV, Delft, where he was involved in all-digital phase-locked loop design for the WiMAX standard. From 2011 to 2012, he was with Broadcom, San Diego, CA, USA, where he was involved in the phase-locked loop design for the advanced wireless local area network system. His current research interests include analog, mixed-signal, and RF circuit and system design.

Mr. Jiang received the Best M.Sc. Thesis Award in 2011 for the EWI Faculty in the Delft University of Technology. He also received the Graduate Division Fellowship in UCLA from 2012 to 2013. He serves as a Reviewer of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I.

Vahagn Hokhikyan received the B.S. degree in computer engineering and the M.S. degree in electrical engineering from California State University at Northridge, Northridge, CA, USA, in 2008 and 2010, respectively. He is currently pursuing the Ph.D. degree in biomedical engineering with the University of California at Los Angeles, Los Angeles, CA, USA, where he is directing his efforts on further miniaturization and optimization of implantable medical devices.

He was with Microsys Inc., Mississauga, ON, Canada, as an Embedded Hardware and Software Engineer for four years. He has been a licensed Professional Electrical Engineer in California since 2011.



Hariprasad Chandrakumar (S'12) received the B.E. degree in electrical engineering from the Birla Institute of Technology and Science (BITS)-Pilani, Pilani, India, in 2010, and the M.S. degree in electrical engineering from the University of California at Los Angeles (UCLA), Los Angeles, CA, USA, in 2012, where he is currently pursuing the Ph.D. degree with the Department of Electrical Engineering.

In 2010, he was with the Wireless Group, Texas Instruments, Bangalore, India, where he was involved in analog Butterworth filters and transimpedance amplifiers. In 2013, he was with the WLAN-RF Group, Broadcom, Sunnyvale, CA, USA, where he was involved in programmable high-Q bandpass filters for transmitter applications. At UCLA, he has been involved in implantable neural sensing front-end architectures for neural signal recording in the presence of stimulation artifacts. His current research interests include analog, mixed-signal, and RF circuits, and their applications to develop solutions for biomedical data acquisition systems.

Mr. Chandrakumar received the Merit Scholarship from BITS-Pilani from 2006 to 2009, the Graduate Division Fellowship from UCLA from 2011 to 2013, the Outstanding Student Designer Award from Analog Devices in 2013, the Henry Samueli Excellence in Teaching Award from UCLA in 2013, the Broadcom Foundation Fellowship from 2016 to 2017, and the Dissertation Year Fellowship from UCLA from 2016 to 2017. He serves as a Reviewer of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II, and the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS.

Vaibhav Karkare (M'09) received the B.E. degree in electrical engineering and the M.Sc. degree in physics from the Birla Institute of Technology and Science-Pilani, Pilani, India, in 2006, and the M.S. and Ph.D. degrees in electrical engineering from the University of California at Los Angeles (UCLA), Los Angeles, CA, USA, in 2009 and 2014, respectively.

He is currently a Senior Design Engineer with Silicon Laboratories, Sunnyvale, CA, USA. His current research interests include the design of mixed-signal circuits/systems and their application to emerging areas, such as biosignal sensors, and the design of algorithms and digital architectures for biomedical data compression.

Dr. Karkare was a recipient of the Edward K. Rice Outstanding M.S. Student Award from the Henry Samueli School of Engineering, UCLA, and the Dimitri N. Chorafas Award for his doctoral research contributions.

Dejan Marković (M'04) received the Ph.D. degree from the University of California at Berkeley, Berkeley, CA, USA, in 2006.

He co-founded Flex Logix Technologies, Mountain View, CA, USA, a semiconductor IP startup, in 2014. He is currently a Professor of Electrical Engineering with the University of California at Los Angeles (UCLA), Los Angeles, CA, USA. He is also a Co-Chair of Neuroengineering with the Bioengineering Department, UCLA. His current research interests include implantable neuromodulation systems, domain-specific architectures, embedded systems, energy harvesting, and design methodologies.

Dr. Marković received the 2007 David J. Sakrison Memorial Prize for the Ph.D. degree and an NSF CAREER Award in 2009. In 2011, he was a co-recipient of the 2010 ISSCC Jack Raper Award for Outstanding Technology Directions. He received the 2014 ISSCC Lewis Winner Award for Outstanding Paper.