A 1.9-mm-Precision 20-GHz Direct-Sampling Receiver Using Time-Extension Method for Indoor Localization

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***Abstract*— This paper presents an impulse-radio ultra-wideband (IR-UWB) receiver design for precise wireless ranging using a newly proposed direct sampling with time-extension (DTE) method. To overcome the problems encountered in high-speed sampling for impulse signals, the DTE method, which exploits the characteristics of an impulse, is proposed. The proposed method performs high-speed sampling only during the period when short pulses exist, and quantizes the sampled signal during the dead time where no pulses exist. The high-speed impulse signal can be easily digitized using low-speed analog-to-digital converter. We designed and fabricated the IR-UWB receiver using a 65-nm CMOS process. The measurement result shows a 1.9-mm resolution for indoor wireless ranging within a 1-m range. The receiver has a power consumption of 70 mW at 1.2 V and energy efficiency of 1554 nJ/pulse.**

***Index Terms*— CMOS integrated circuits, impulse radio, radio-frequency (RF) sensor, receivers, time of flight, ultra-wideband technology.**

I. Introduction

PRECISION location sensors are highly useful in many applications including those in the medical, entertainment, and industrial fields. For example, in gaming devices with user-sensory interface, location sensors are used to detect the user movement, providing a more realistic gaming environment. Previous gaming devices with user-sensory interfaces used mechanical sensors such as accelerometers and gyroscopes to detect the user movement [1]. However, such sensors have low accuracy, and those with mechanical control have low life cycle and high power consumption [2].

If these previous location sensors are replaced with radio-frequency (RF) location sensors, the location precision and power consumption can be significantly enhanced and reduced, respectively; furthermore, additional data communication becomes possible [3]–[6].

Fig. 1 shows the basic concept of ranging using impulses. Here, D and T_{diff} are the location and a time difference between receiver positions, respectively. The impulse signal transmitted by the transmitter is received at the receiver with a time delay. If the location of the receiver changes by D, the time of arrival (ToA) of the impulse signal received at the receiver is delayed by as much. Because impulse signal is transmitted at the velocity of light, the change in the receiver location D can be estimated from the time delay of T_{diff} at the receiver [7]–[10].

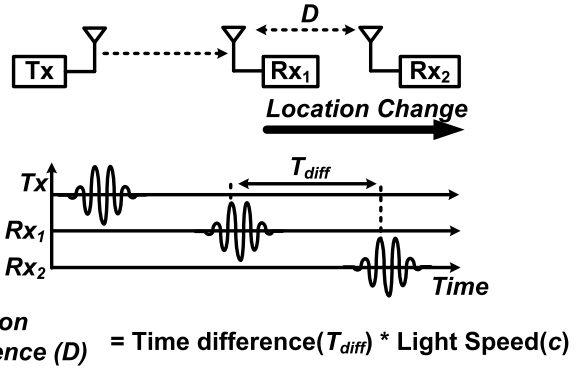

Fig. 1. Concept of ranging with impulse signal.

Fig. 2 shows that various methods have been used to detect the impulse signal. The analog correlation method shown in Fig. 2(a) detects the location by taking the correlation between the template and signals in an analog domain [11]. However, in such an analog correlation method, accurately manipulating the timing is difficult because since it is performed in the high-frequency analog domain which limits the ranging accuracy [12]. The direct-sampling method shown in Fig. 2(b) directly digitizes a received impulse signal using a high-speed analog-to-digital converter (ADC) [13], [14]. It is effective because all signal-processing works such as correlation can be performed in a digital domain. However, the ADC requires high performance to meet the Nyquist criterion. Such a high-speed ADC suffers from the disadvantages of complicated design and large power consumption. To avoid the use of the high-speed ADC with such difficult design requirements, the subsampling method (or the equivalent-time sampling method) shown in Fig. 2(c) has been proposed [15]–[18]. The subsampling method is based on the use of a sampling clock with period, $T_{\text{prf}} + \Delta d_s$, which has a slight difference (Δd_s) from the repetition time of impulse, T_{prf} as shown in Fig. 2(c). In this case, although the sampling rate is much lower than that of the direct sampling, digitizing high-speed signal becomes possible. However, a price is incurred in using

Manuscript received January 20, 2016; revised September 21, 2016 and February 1, 2017; accepted February 21, 2017. Date of current version May 23, 2017. This work was supported by Space Core Technology Program through the National Research Foundation of Korea funded by the Ministry of Science, ICT & Future Planning under Grant NRF-2014M1A3A3A02034806. The CAD tool and MPW were supported by IDEC. This paper was approved by Associate Editor Ali M. Niknejad. *(Corresponding author: Tae Wook Kim.)*

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Digital Object Identifier 10.1109/JSSC.2017.2679068

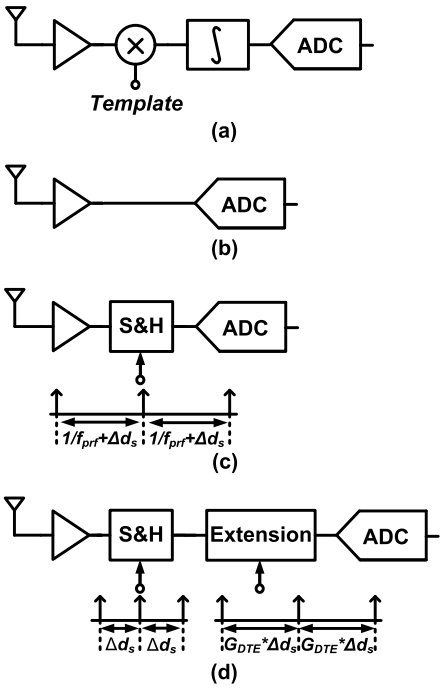


Fig. 2. Impulse radio architectures. (a) Correlation method. (b) Direct-sampling method. (c) Subsampling (equivalent-time sampling) method. (d) DTE method.

low-speed sampling to detect high-speed impulse

$$G_{\text{sub}} = \frac{T_{\text{prf}}}{\Delta d_s} \tag{1}$$

$$T_{\text{prf\_sub}} = G_{\text{sub}} \cdot T_{\text{prf}}. \tag{2}$$

Here, G_{sub} is the ratio of the pulse repetition time (T_{prf}) to the virtual-sampling speed (Δd_s), and $T_{\text{prf\_sub}}$ is the pulse repetition time of the subsampled impulse. From (1) and (2), G_{sub} increases as the virtual sampling speed increases, which results in the increase in $T_{\text{prf\_sub}}$. In other words, more time is required to obtain one period of the impulse signal. In the frequency domain, the bandwidth of the wideband impulse signal decreases by G_{sub} during subsampling. Therefore, a high-speed ADC is not needed. However, since it needs as many as G_{sub} pulses for a single pulse recovery, its detection speed is low. It sacrifices the sampling speed for the detection speed.

To relieve such digitization issues in the high-speed impulse, we propose the direct sampling with time-extension (DTE) method as shown in Fig. 2(d) which exploits the characteristics of an impulse [19]. The proposed method performs a high-speed sampling only during the occurrence of short pulses, and slowly quantizes the sampled signal during dead time, as shown in Fig. 2(d). By using this method, we can digitize high-speed impulse signals (3–5 GHz) with oversampling ratio of greater than five, even with a low-speed ADC (100 MHz). Thus, the ToA estimation for localization is performed with high accuracy in digital domain.

Table I compares the above techniques in terms of detection speed, ranging accuracy, and power consumption. Since the analog correlation method generally uses a 1-b quantizer, the receiver consumes less power. However, it is difficult to have

TABLE I
TRADEOFF BETWEEN IMPULSE RADIO ARCHITECTURES

	Analog Correlation Method	Direct-sampling Method	Sub-sampling Method	Time-extension Method
Ranging Accuracy	Low	Mid	Mid	High
Detection Speed	High	High	Low	High
Power Consumption	Low	High	Low	Low

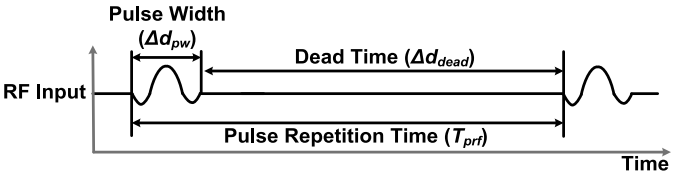


Fig. 3. Characteristics of impulse transmission.

a fine step correlator, which is necessary for high accuracy; thus, the receiver with analog correlation method has low ranging accuracy. In case of direct sampling, a high-speed ADC generally consumes much power and it is hard to achieve high resolution because of its limitation of quantization level. In the subsampling method, we can save power of a receiver by replacing the high-speed quantizer with low-speed quantizer. So, it is possible to use a high-resolution quantizer. However, since multiple pulses are necessary in restoring one pulse, the detection speed is low. Thus, we assume same time for a detection the proposed method has more room to take average of multiple pulses as many as G_{sub} than subsampling method has. In this respect, the proposed method can have higher SNR as much as G_{sub} than subsampling method. The proposed method can achieve high accuracy, low power consumption, and high detection speed.

This paper is organized as follows. Section II explains the proposed time-extension method based on time-interleaving technique. Section III describes circuit and system design for a receiver with the proposed technique in detail. Section IV summarizes the measurement results. Section V concludes the paper.

II. TIME-INTERLEAVED SAMPLING FOR TIME EXTENSION

A. Concept of the Time-Extension Method

Fig. 3 shows the characteristics of the impulse transmission and shows the impulse that has a short pulsewidth (Δd_{pw}) during T_{prf}, but a large dead time (Δd_{dead}). In a typical impulse-based communication, Δd_{pw} is set to 0.2% of the total pulse-repetition period. In this case, Δd_{dead} is 99.8% [20], [21]. For example, if T_{prf} is 1000 ns and the impulse has a short pulsewidth of approximately 2 ns, then Δd_{dead} is 998 ns. In the time domain, this condition results in using only 0.2% of one period for communication, and wastes Δd_{dead} which contributes 99.8% of T_{prf}. In the proposed DTE method, the large and wasted dead time is used to convert the high-speed impulse signal to a low-speed signal. Fig. 4 shows the concept of the proposed DTE method. Here, Δd_s is the sampling interval, and Δd_e is the extension interval. During one period of pulse transmission, the impulse has

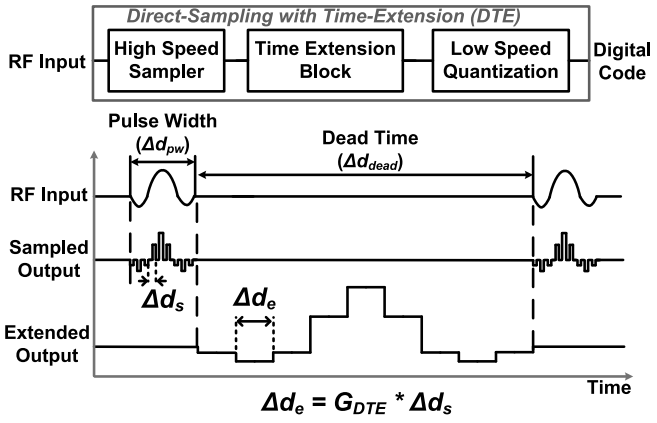


Fig. 4. Concept of the proposed DTE method.

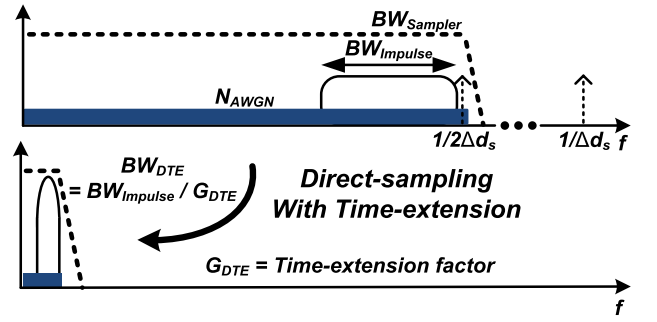


Fig. 5. Noise characteristic of proposed DTE method.

a short pulsewidth, and the majority consists of dead time. A high-speed sampler performs high-speed sampling with Δd_s during Δd_{pw}, when the impulse exists. The time-extension block consecutively and slowly passes the signal sampled by a high-speed sampler to the quantization block in the interval Δd_e during Δd_{dead}. Here, the time-extension factor of the extended signal is described by

$$G_{\mathrm{DTE}} = \frac{\Delta d_e}{\Delta d_s}. \tag{3}$$

Here, G_{DTE} is the time-extension factor. Compared with the RF input signal, the pulsewidth of the extended output increases by a factor of G_{DTE} in the time domain. However, in the frequency domain, as shown in Fig. 5, the DTE method decreases the bandwidth by a factor of G_{DTE}, because the pulsewidth of the RF input signal increases by a factor of G_{DTE}. The center frequency of the extended output also decreases by a factor of G_{DTE}. In other words, the frequency and bandwidth of the extended signal decrease by a factor of G_{DTE}. For example, if a high-speed sampler in the DTE block has a sampling time (Δd_s) of 50 ps, and the time-extension block has an extension time (Δd_e) of 20 ns, then G_{DTE} is 400. If we assume that the center frequency and bandwidth of the RF input signal are 4 GHz and 500 MHz, respectively, the extended output from the time-extension block has the center frequency and bandwidth decreased by a factor of $1/G_{\mathrm{DTE}}$, to 10–1.25 MHz, respectively. Because the time-extended output signal is converted into a relatively low-speed signal, a high-speed ADC is no longer needed. The proposed DTE method converts the high-speed signal into a low-speed signal similar to the subsampling. Here, $\mathrm{BW_{DTE}}$ is the bandwidth of the extended output. Because the DTE method directly samples the impulse only when the signal exists, it does not need multiple impulses for the sampling, unlike the subsampling. In addition, the center frequency and bandwidth of the converted signal of the DTE are reduced by as much as $1/G_{\mathrm{DTE}}$, and thus high SNR with low quantization speed can be achieved.

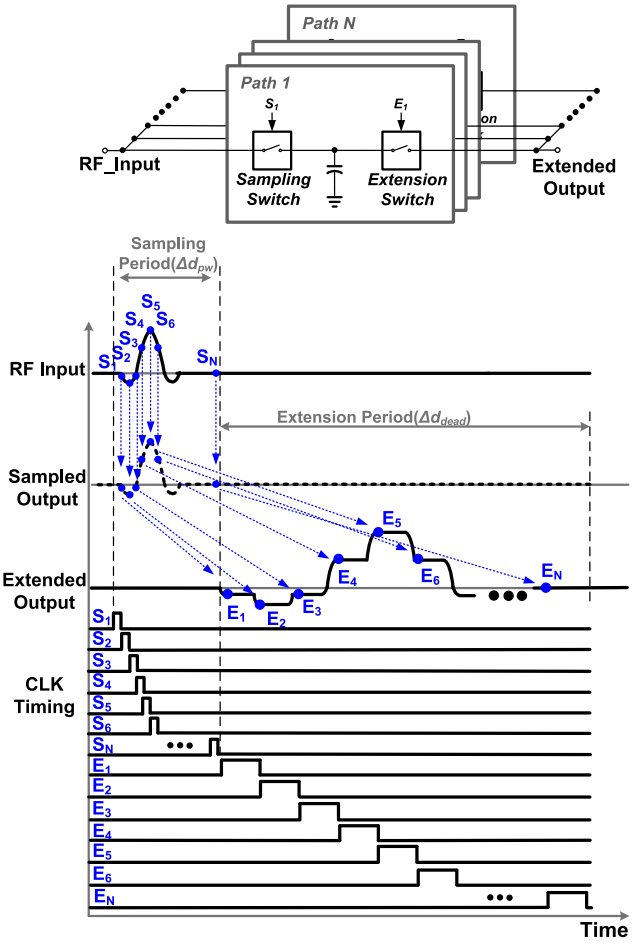


Fig. 6. Schematic and timing diagram of the N-path sampler and time-extension block.

B. High-Speed Sampling for Time Extension

The high-speed sampler in DTE block is realized using the time-interleaving technique. To overcome the speed limitation of the sampler for high-speed sampling, the operating speed of the sampler is reduced using multiple interleaving paths [22], [23].

Fig. 6 shows the schematic and timing diagram of the N-path sampler and time-extension block in DTE method. S_N and E_N denote the sampling and extension clocks of the Nth path, respectively. Each path consists of a pair of sampler and extension switch. The sampler in each path samples the RF input signal in a capacitor through S_N. S_N, which is applied to the Nth path, has a time difference of Δd_s with S_{N-1}, which is applied to the $(N-1)$th path. Therefore, the N-path sampler consecutively samples the RF input signal in Δd_s intervals. The sampling range (Δd_{pw}) becomes $N \times \Delta d_s$.

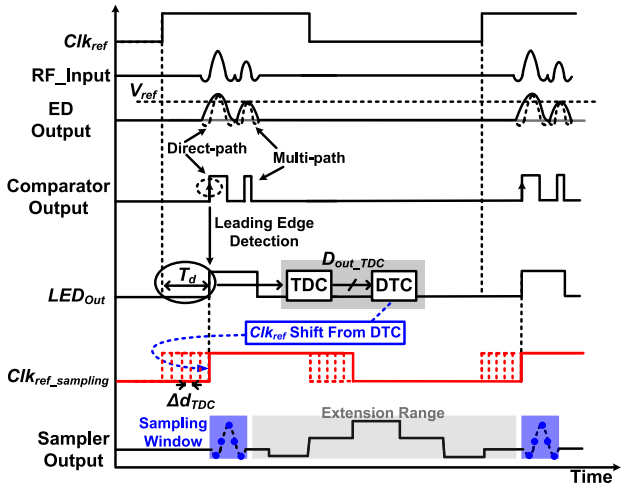


Fig. 7. Timing diagram of sampling window generation method.

Moreover, each path holds the sampled value in a capacitor during S_N.

The values stored in each path are delivered as extended outputs, in synchrony with E_N. E_N which is applied to the Nth path is G_{DTE} times slower than S_N, with a time difference of Δd_e from E_{N-1}, which is applied to the $(N-1)$th path. Thus, the extension range ($\Delta d_{\mathrm{dead}} = N \times \Delta d_e$) is large compared with the sampling range ($N \times \Delta d_s$) by the ratio of G_{DTE}. The N-path extension switch gradually delivers the signals stored in the capacitors as extension outputs in Δd_e intervals.

In this case, the extended output is the dilation of the RF input signal by a factor of G_{DTE} in the time axis, as explained in Section II-A. Conversely, the signal is contracted by a factor of $1/G_{\mathrm{DTE}}$ in the frequency axis. In other words, it appears as if the impulse is dilated in the time axis using the existing dead time as extension range (Δd_{dead}), and in the frequency axis as if it is reduced, enabling the reduction in the quantization speed to digitize the impulse.

However, the coverage of the DTE method is limited by the number of time-interleaved paths. If a high-speed sampler with DTE architecture consecutively performs the sampling in accordance with S_N, the sampling range is $N \times \Delta d_s$, which is fixed by the number of time-interleaving paths. If the impulse, which is an RF input signal, does not exist within this sampling range, the signal is missed and sampling cannot be performed. To overcome this problem, the position of the received impulse is roughly determined by the receiver. Then, it provides sampling window. Fig. 7 shows how to determine the position of the received impulse signal and generate the sampling window. The envelope of the RF input signal is compared with threshold voltage (V_{ref}) in the comparator and then converted into a digital pulse [24]. Because the transmitter and receiver are synchronized through the system reference clock ($\mathrm{Clk_{ref}}$); the location of next RF input signal can be determined by the time interval (T_d) between the pulse from comparator output and $\mathrm{Clk_{ref}}$. Based on the measured time-to-digital convertor (TDC) code, digital-to-time convertor (DTC) shifts $\mathrm{Clk_{ref}}$ with 1-ns (Δd_{TDC}) step to generate a sampling window for the high-speed sampler, which is the sampling reference clock ($\mathrm{Clk_{ref\_sampling}}$). (Detailed explanations regarding

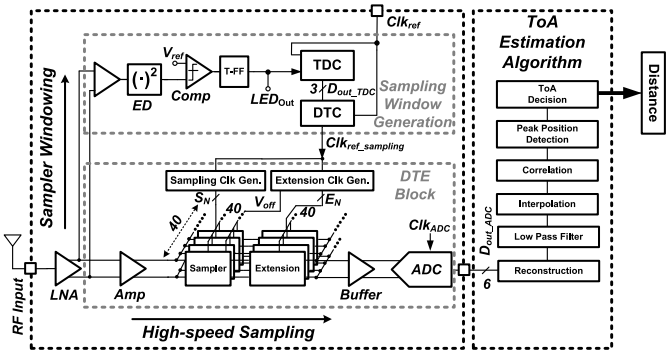


Fig. 8. Block diagram of the proposed system.

the operation of the TDC and DTC are provided in Section III.) By referring to this sampling window, the DTE block conducts sampling and extension. The sampling clock generator and the extension clock generator are triggered by $\mathrm{Clk_{ref\_sampling}}$ and generate S_N and E_N, respectively.

The proposed time-extension method decomposes sampling from quantization, which allows high-speed sampling with time-interleaved sampling, and low-speed quantization with the time-extension technique. The technique is extended from time-interleaving techniques by exploiting a heavy duty cycle which is one of the major characteristics of impulse-radio ultra-wideband (IR-UWB). The conventional time-interleaved (TI) ADC has its own quantizer for each sampling path, but the time-extension technique allows to have only one low-speed quantizer for all sampling paths. The low-speed quantization can allow high quantization level.

III. System Implementation

A. System Design

Fig. 8 shows the block diagram of the proposed system. The system consists of the sampling window generation block, high-speed sampling path, and digital signal processing block for ToA calculation [19]. The received RF input signal is amplified using a low-noise amplifier (LNA), and the amplified signal is delivered to the DTE block and sampling window generation block. The sampling window generation block converts the signal received from the LNA to a digital pulse using energy-detection method. From the digital pulse, the position of the received pulse is estimated where high-speed sampling starts.

The DTE block consists of 40 time-interleaved samplers. The time-interleaved sampler performs high-speed sampling in 50-ps intervals which is equivalent to 20 Gs/s for 2-ns duration. Because the frequency of the impulse is 4 GHz, S_N has an oversampling ratio of five, which effectively increases the SNR. The signals sampled in each path are delivered to the ADC through time-extension block in 20-ns intervals, for 800-ns duration. The delivered extended signal is digitized by a 100-MHz, 6-b ADC. Because the center frequency and bandwidth of the RF input signal have been decreased by a time-extension factor (G_{DTE}) of 400 through time-extension method at the DTE block, 100-MHz ADC can sufficiently digitize this signal. ToA estimation is performed in the digital domain using computer software.

TABLE II
PARAMETERS FOR MDS CALCULATION

Parameter	Value	Note
$B_{-3,sig}$	500 MHz	3 dB Bandwidth of Signal
f_c	4 GHz	Center Frequency
PRF	1 MHz	Pulse Repetition Frequency
D_g	26.9 dB	Duty Gain ($\approx 10\log\frac{B_{-3,sig}}{PRF}$)
P_a	-14.2 dBm	Average transmitted Power
P_t	12.7 dbm	Transmitted power of Tx
$G_t,\ G_r$	3 dBi	Tx/Rx Antenna gain
P_l	44.4 dB	Path loss at when D = 1 m
P_r	-25.7 dBm	Input power at the Rx
G_{window}	32 dB	Gain of sampler windowing path
L_{window}	2.25 dBm	Detection limit of comparator($V_{ref} = 300\ mV$)
MDS_{window}	-29.75 dBm	Minimum detectable signal of the sampling window generation
$B_{-3,Rx}$	4.25 GHz	3 dB Bandwidth of Rx
N_{AWGN}	-77.4 dBm	AWGN floor($k_oTB_{-3,Rx}$)
F_{DTE}	9.6 dB	Noise Factor of high speed sampling path
M_{avg}	20 dB	Average number = 100
SNR_{DTE}	39 dB	Required SNR for 1mm accuracy
MDS_{DTE}	-48.6 dBm	Minimum detectable signal of high speed sampler path

B. Signal Analysis

Table II shows parameters for a minimum detectable signal (MDS) calculation. The transmitted power of the transmitter considering D_g is as follows [20]:

$$P_t = P_a + D_g. \tag{4}$$

Path loss depending on distance is as follows:

$$P_l = 20\log_{10}\left(\frac{4\pi\, Df_c}{c}\right) \tag{5}$$

where c is the velocity of light. When D is 1 m, path loss is 44.4 dB. In this case, the signal power that arrives at receiver is as follows:

$$P_r = P_t + G_t + P_l + G_r. \tag{6}$$

Antenna gain used for transmitter and receiver is 3 dBi, so input power received at the receiver antenna is -25.7 dBm.

First, an MDS of the sampling window generation block ($\mathrm{MDS_{window}}$) is calculated, which allows initiation of sampling. The MDS for the sampling window generation block depends on the voltage level of the comparator's V_{ref} which is L_{window}, and then $\mathrm{MDS_{window}}$ is calculated from the following:

$$\mathrm{MDS_{window}} = L_{\mathrm{window}} - G_{\mathrm{window}}. \tag{7}$$

The input signal received at the distance of 1 m is -25.7 dBm, which is greater than -29.75 dBm. If we increase the gain of the sampling window path, we can easily increase the $\mathrm{MDS_{window}}$. For example, if we use an external amplifier, we can extend the ranging distance.

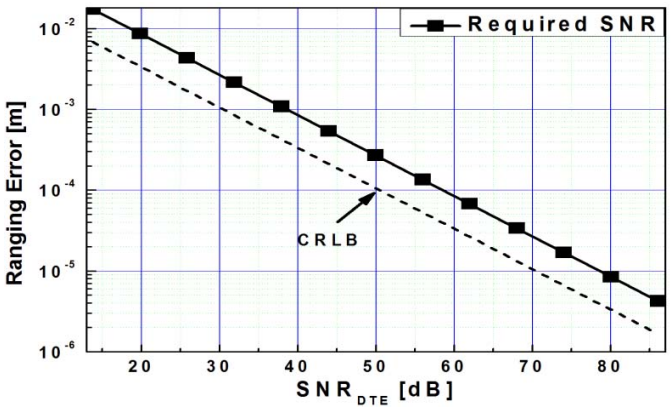


Fig. 9. Ranging error versus $\mathrm{SNR_{DTE}}$ and CRLB.

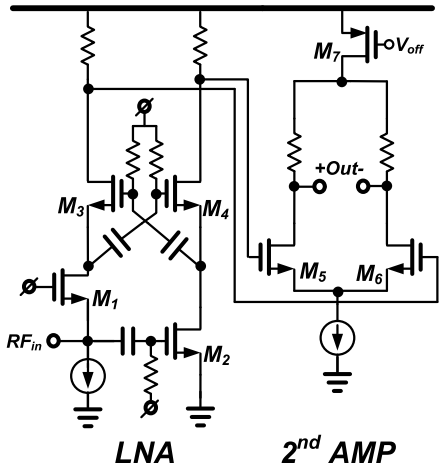


Fig. 10. Schematic of LNA and second stage amplifier.

We also calculated an MDS of the DTE ($\mathrm{MDS_{DTE}}$) path, which determines ranging accuracy. MDS of DTE block is as follows:

$$\mathrm{MDS_{DTE}} = N_{\mathrm{AWGN}} + F_{\mathrm{DTE}} + \mathrm{SNR_{DTE}} - M_{\mathrm{avg}}. \tag{8}$$

$\mathrm{SNR_{DTE}}$ is obtained from simulation as shown in Fig. 9. For 1-mm accuracy, a 39-dB SNR is required. We can relax the required SNR by taking the average of multiple signals; here, we assume 100 multiple signals which corresponds 20 dB (M_{avg}). Thus, the $\mathrm{MDS_{DTE}}$ is calculated to -48.6 dBm. In other words, when the input signal becomes equal to or more than -48.6 dBm, the receiver can have accuracy of 1 mm.

C. RF Amplifier Design

Fig. 10 shows the schematic of LNA and second stage amplifier. To satisfy the wide bandwidth requirement, LNA is designed with single-to-differential architecture in combination of the common-gate and common-source topologies. To minimize mismatch among the differential signals of the single-to-differential structure, cross-coupling structure is used at the cascode stage [25]. The S_{11} is less than 8 dB for frequency between 1 and 7 GHz. The voltage gain is 10 dB, BW is 6 GHz, noise figure (NF) is 4.5 dB, and IIP3 is -8 dBm.

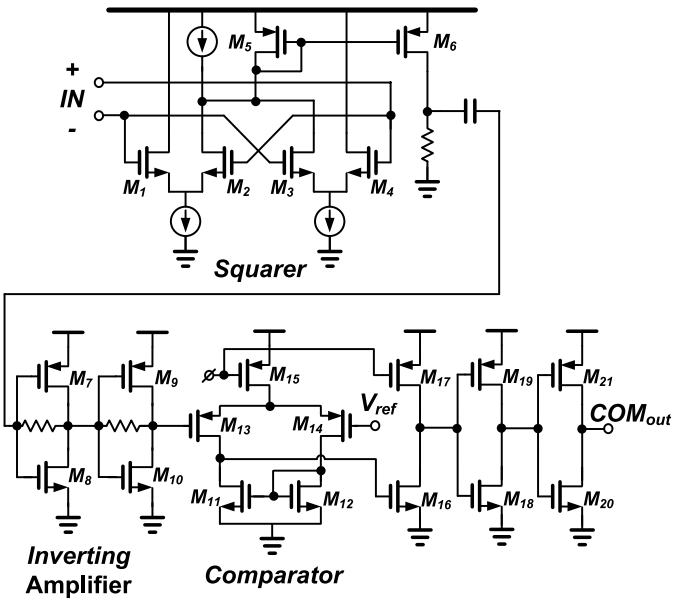


Fig. 11. Schematic of analog signal path of the sampling window generation block.

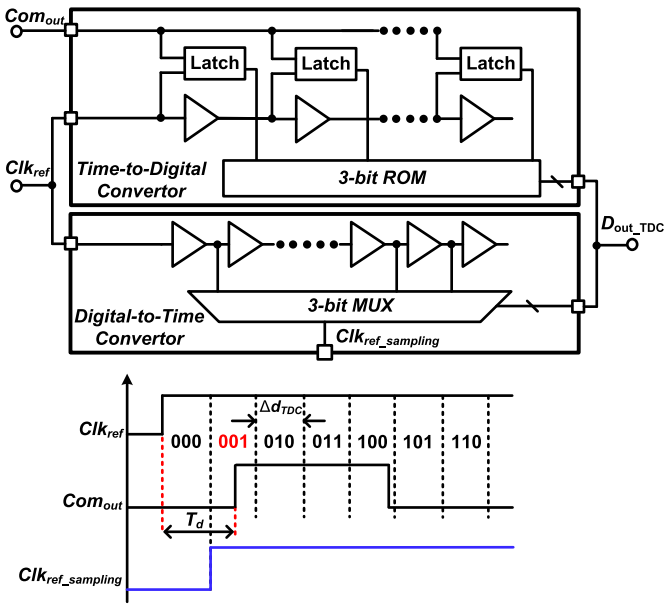


Fig. 12. Schematic and timing diagram of TDC and DTC in the sampling window generation block.

The power consumption is 3.6 mW. The second stage is designed with a differential-amplifier structure. To secure sufficient bandwidth (>5 GHz) without using inductors to save silicon area, the amplifier has a voltage gain of 8 dB with a power consumption of 7.2 mW. The second stage amplifier used in the DTE block is controlled using a pMOS (M7) head switch so that it is turned on only during sampling to save on power consumption.

D. Sampling Window Generation Block

Fig. 11 shows the schematic of the analog signal path of the sampling-window generation block for the detection of the envelope of the received signal. The analog signal path in the sampling window generation block uses an envelope detector structure based on a squarer and a comparator. The input signal is squared using the squarer, and the inverter-type amplifiers are connected to the output of the squarer. The output of the inverter-type amplifier is compared to the threshold voltage (V_{ref}) of the comparator, and is converted to a digital pulse. Fig. 12 shows the schematic and timing diagram of TDC and DTC in the sampling-window generation block. An example of target applications of this paper is a short-range RF location sensor, as discussed in the introduction, which assumes line of sight (LoS). In the case of LoS, the first arriving pulse determines location. Therefore, the sampling window generation path adapts a leading-edge detection technique with the envelope detector and the comparator, which detects the first arriving pulse and ignores other multipath components [24]. The digital pulse generated from the comparator is used to determine the rough position of the received pulse using a 3-b TDC as shown in Fig. 12 [26]. Because the digitization of accurate waveform is performed in the DTE block, TDC can sufficiently determine the rough position of the pulse. The TDC outputs a digital code by calculating the time difference in the digital pulse to the Clk_{ref} with Δd_{TDC} resolution. The DTC generates $\text{Clk}_{\text{ref\_sampling}}$ by delaying Clk_{ref} according to the TDC code. The 3-b DTC consists of a delay line and a multiplexer. The delay line of the DTC copied that of the TDC, and thus the timing mismatch between TDC and DTC was minimized. Δd_{TDC}, which is the delay step of the TDC and DTC, is designed to be 1 ns, which is half of the entire sampling range (=2 ns) of the DTE block, so that it covers the timing mismatch between the sampling window generator block and the DTE block. The sampling window is 1 ns, and the duration of the impulse is 2 ns; in the worst case, it might be impossible to sample the entire pulsewidth. However, most of location sensors use a digital algorithm such as Kalman filter which uses temporal history information for position estimation so it can relieve the issue in the extreme case.

E. Direct-Sampling With Time-Extension Block Design

Fig. 13 shows that the high-speed sampler utilizes a differential source-follower sampling structure [27], [28]. Source-follower sampling is more advantageous in high-speed sampling than in the switched-cap sampling. However, a disadvantage exists in that each sampler has high power consumption for high-speed sampling. To overcome this disadvantage, head switches (M_{S9}) are assigned to each sampler so that the sampler is switched ON only during the sampling period and is switched OFF after the signal has been sampled. The head switches can be controlled by either the $\text{Clk}_{\text{ref\_sampling}}$ or Clk_{ref} in Fig. 7. When the power-OFF switch is controlled by Clk_{ref}, it is turned on 10 ns prior to the rising edge of Clk_{ref} and turned off 10 ns after its falling edge. Thus, it can cover a 3-m ranging distance in a ToA measurement. In the ToA measurement, the power-OFF switch is controlled by an external clock which also provides the Clk_{ref}. Also it is possible for the power-OFF switch to use $\text{Clk}_{\text{ref\_sampling}}$ for time difference of arrival (TDoA) measurement. The extension block is designed with a pMOS source-follower buffer and a transmission gate switch. The signals extended from each path

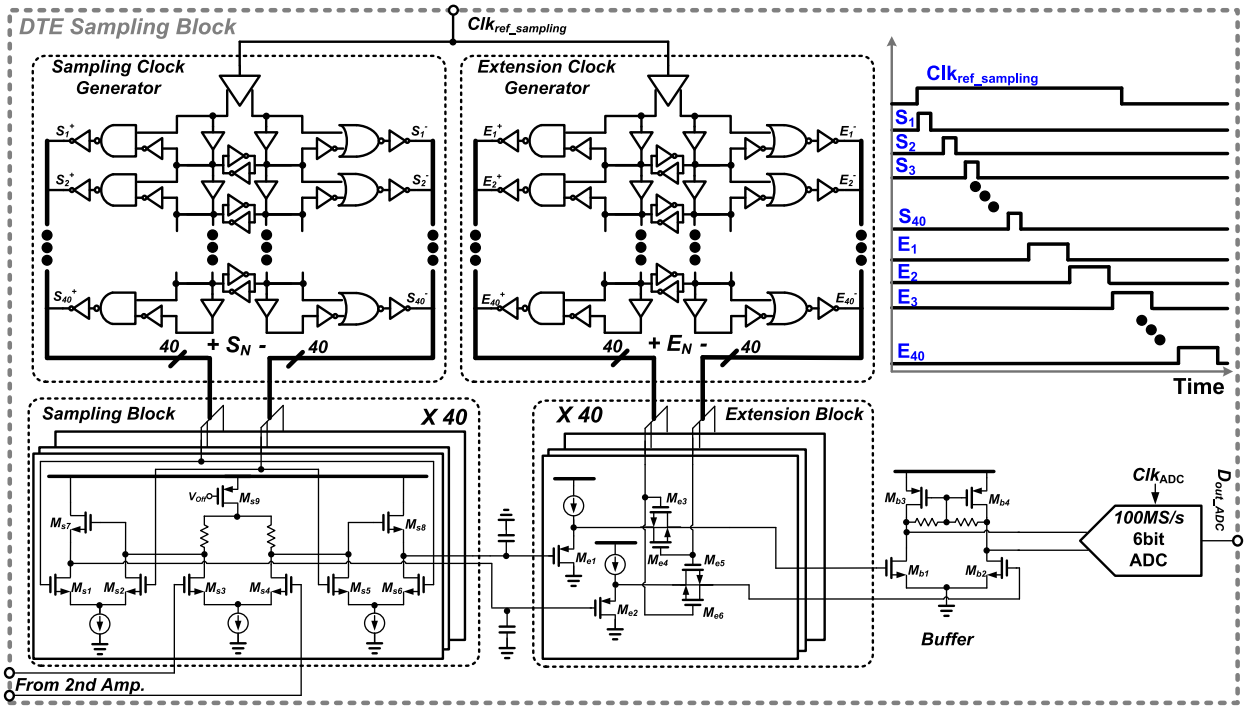


Fig. 13. Schematic of DTE sampling block.

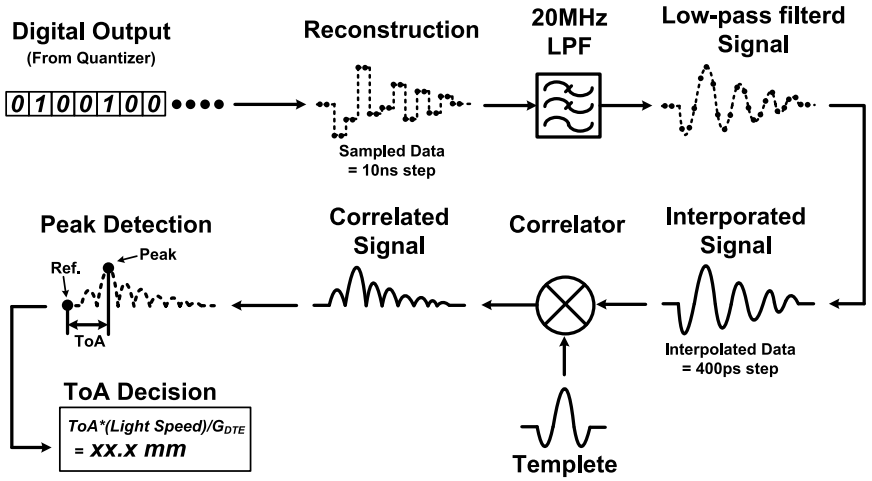


Fig. 14. ToA estimation using digital signal processing.

are summed by the buffer. The number of sampling block and extension block is 40. The extended output is delivered to a 6-b, 100-MHz ADC [29].

The sampling- and extension-clock generator block is designed as a delay-based timing generator. The sampling-clock (S_N) generator block generates consecutive high-speed sampling-clock pulses with a pulsewidth of 50 ps from $\text{Clk}_{\text{ref\_sampling}}$ using a unit inverter delay of 50 ps to provide the sampling clocks for each path for 2 ns (=40 × 50 ps) duration. Similarly, the extension-clock (E_N) generator block generates the extension clock for each path for 800-ns duration (=40×20 ns). Each clock generator block is designed to allow external trimming by designing the timing buffer of the input to be a variable delay. The clock buffer can be trimmed to prevent the overlap between sampling period and extension period.

F. Digital Signal Processing Block Design for ToA Estimation

The proposed receiver roughly determines the location of the received impulse signal within an 8-ns range (3 b of 1 ns) in units of 1 ns using the 3-b TDC of the sampling-window generator block. In terms of distance, 2.4-m range can be covered in units of 30 cm. The high-speed sampler, which operates on the basis of $\text{Clk}_{\text{ref\_sampling}}$ generated by the sampling-window generator block, performs high-speed sampling in intervals of 50 ps for 2 ns with 40 time-interleaving sampling paths that cover 60-cm range-wise, which is twice the TDC resolution.

Fig. 14 is a conceptual diagram of digital signal processing. A precise estimation of the actual ToA is performed by the ToA estimation algorithm of the digital signal processing block using the ADC outputs. It is first reconstructed to a waveform in the digital domain. Then, in order to eliminate

high-frequency noise, the signal is low-pass filtered with a cutoff frequency of 20 MHz, which is greater than the bandwidth of the extended signal we used. Since the received data is sampled at a sampling speed of 10 ns with of the time-extension method, we perform spline interpolation with a timespace of 400 ps [30]. Then, the cross-correlation technique is employed to determine the ToA between a template signal and the received pulse which is defined in (9). In (9), g[n] is a template signal and f[n] is an incoming pulse

$$(f * g)[n] \stackrel{\text{def}}{=} \sum_{M=-\infty}^{\infty} f^*[m]g[m+n]. \tag{9}$$

For the template pulse, we used an impulse that is the average out of 10 000 pulses wirelessly measured with receiver. The difference between a maximum correlation point and a reference indicates ToA in the digital domain [31]. The actual distance is calculated from ToA by multiplying the speed of light and $1/G_{\text{DTE}}$ which is time-extension ratio.

Unlike the previous receivers who use the analog correlation method, the proposed receiver can digitally reconstruct the impulse, allowing for a more precise correlation in the digital domain and, thus, improving the ToA accuracy. Thus, even though we use timing resolution (Δd_s) of 50 ps in the sampler, it is possible to have lower distance resolution than Δd_s.

G. Ranging Accuracy Analysis

The sampling window generation block estimates the location of pulse roughly, and then the DTE block determines the remaining location with fine accuracy. If we use a large timing step for the rough estimation, then we need to increase the number of samplers, but the effect of timing error in the rough estimation is reduced, and vice versa. We took such tradeoffs into consideration; thus, the sampling window generation block has a timing step of 1 ns and the DTE covers the range of 2 ns by 50-ps step with 40 samplers. The rough position of the signal is calculated with a TDC. In the rough timing estimation with comparator, there could be settling time issue as a timing error. However, if the timing error is less than the timing step of the TDC, the error influences the rough position estimation. The settling time variation is only 36 ps over 0.3–1.1 V variation of V_{ref} from the simulation. The timing step of the TDC is 1 ns. Thus, the effect of timing error in the comparer is negligible. The high-speed sampler measures distance with fine resolution; the number of bits of quantizer and sampling time exerts a strong influence on the ranging accuracy. Fig. 15 plots ranging error over the number of bits and sampling speed in the fast sampler. As expected, a higher number of bits in the quantizer as well as high sampling speed guarantee low ranging error. We choose 6-b quantization level and 20-GHz sampling speed.

The sampling clock for 40 parallel paths is provided by an inverter chain in the delay line. We run a simulation of ranging error over timing mismatch among delays cells, as shown in Fig. 16. The ranging error from the timing mismatch is not critical in our ranging system because a timing mismatch among delay cell in a neighborhood is usually small [32]. In this case, we run a Monte Carlo simulation

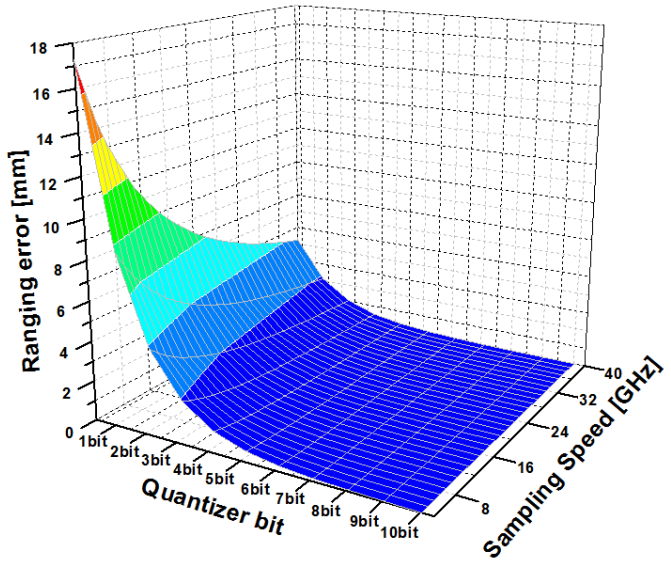


Fig. 15. Simulation result of ranging error versus quantizer bit and sampling speed.

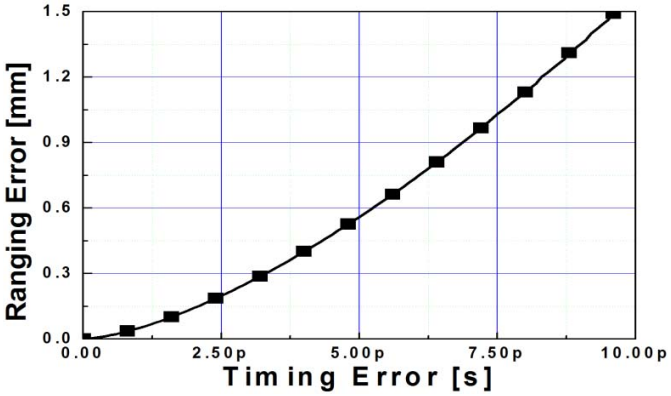


Fig. 16. Simulation result of ranging error from timing error in time-interleaved path.

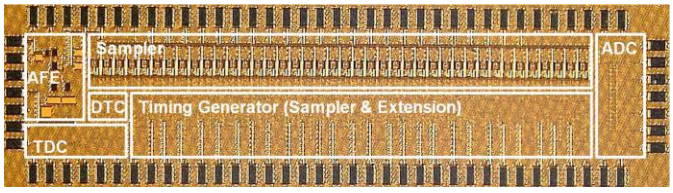


Fig. 17. Microphotograph of the receiver.

(sample size = 100) that shows that it is less than 2.7 ps. Another error caused by mismatch among the time-interleaved paths is an offset error caused by mismatch among high-speed samplers. In order to calibrate the offset, we apply zero volts at the input, and measure the offset for each sampling path and calibrate it in the digital domain.

IV. Measurement Result

The proposed IR-UWB receiver was implemented using 65-nm CMOS technology. The receiver has a power consumption of 70 mW. Fig. 17 shows the microphotograph of the receiver. The receiver has an area of 6 mm^2. Fig. 18 shows the measurement setup. A commercially available directional

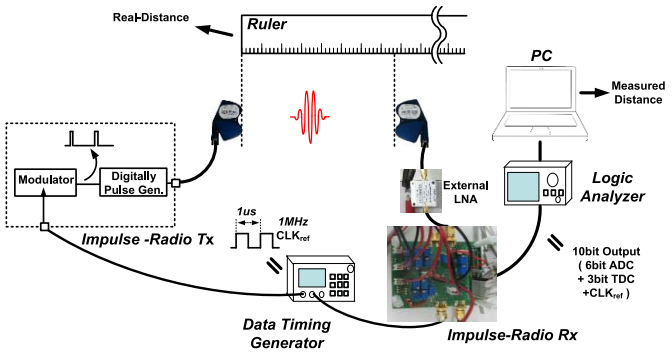


Fig. 18. Measurement setup.

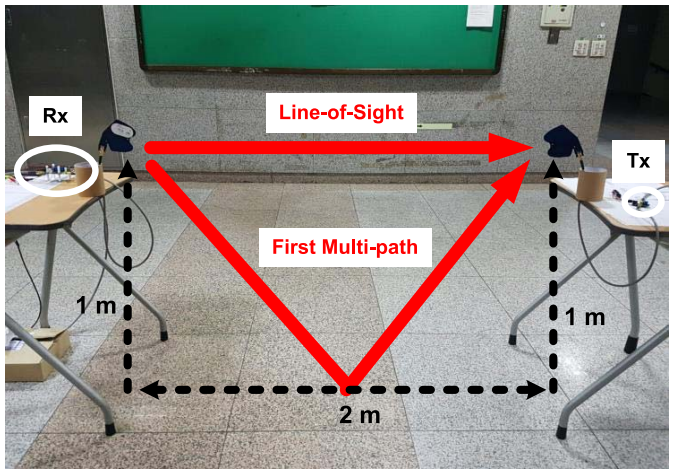


Fig. 19. Measurement environment.

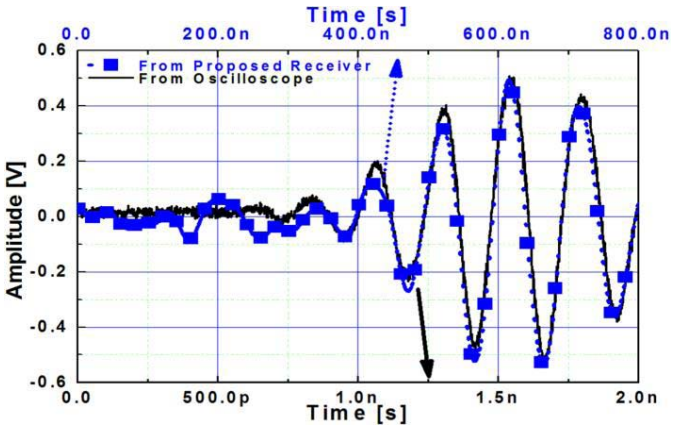


Fig. 20. Waveform from a high-speed oscilloscope (black line) and the proposed system (blue dotted line) (timing offset was trimmed so that impulses overlap).

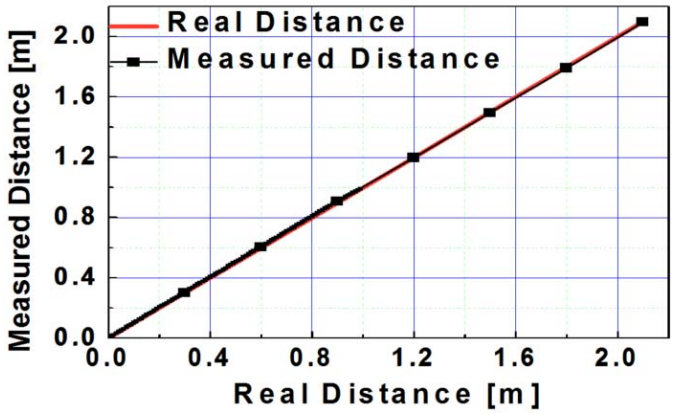


Fig. 21. Result of distance measurement within 2.1-m range. (One-point calibration is applied.)

antenna with a 4-dBi antenna gain is used for the receiver and transmitter. The directional antenna used in this paper has the gain of 4–8 dBi in the frequency range of 3–6 GHz. The transmitter is designed with a Gaussian impulse generator structure [33], [34]. The transmitter obtains a reference clock from the data timing generator, and uses the rising edge of the reference clock to generate impulses. To measure distances of 1–2.1 m between the receiver and transmitter, an external amplifier is used. The external LNA which can provide additional gain to RF path is used to extend the ranging distance as discussed in Section II-B. The external amplifier has a gain of 15 dB and power consumption of 250 mW. The received signal is digitized by the receiver which is synchronized with the transmitter. A total of 10 b of digital output is fed from the receiver into a logic analyzer, including the 3-b TDC output of the sampling window generator, 6-b output of the ADC of the DTE block, and the $\mathrm{Clk_{ref}}$. In order to identify the ranging accuracy of the proposed method, ToA is measured by sharing a clock between receiver and transmitter, even though it is not realistic in localization sensor applications [36]. The localization sensor that employs this technique can be applied to localization using the TDoA algorithm, which shares a clock among receivers [15]. The digital code acquired through a logic analyzer is used in the ToA estimation using a computer software.

Fig. 19 shows the measurement environment. The measurement was conducted in an actual office environment where interferences and multipath components existed. The measured MDS for sampling window generation block is −25 dBm. The MDS is quite high compared to other works. This is because the primary purpose of this paper is to verify our idea of the time-extension method, and thus we simplify other circuits as much as possible. By adding more gain in RF stage, we can easily increase the MDS. Fig. 20 shows the comparison between the impulse waveform measured using a high-speed oscilloscope, and that from the proposed receiver. The black line represents the measurement result from oscilloscope, and the time axis represents the x-axis at the bottom of the figure. The blue dotted line represents the measurement result from the proposed receiver, and the time axis here is the x-axis at the top of the figure. In order to overlap black line and blue dotted line for comparison purpose, we manually trimmed timing offset between the result of the high-speed oscilloscope and that of Rx timing. It can be observed that the time-scale of the waveform measured using the proposed receiver is 400 times longer than that of the waveform measured from an oscilloscope. This implies that DTE-based receiver appropriately digitizes the high-speed impulse signal.

Fig. 21 shows the result of the distance measurement within a 2.1-m range. The measurements were carried out in units of 1 cm for the 0–1 m range, and 30 cm for the range

TABLE III
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART WIRELESS RANGING RECEIVERS

	This Work	[36]	[16]	[5]	[18]
Feature	Direct-sampling with time-extension	Equivalent-time sampling	Equivalent-time sampling	Frequency sweep	Direct-sampling with integration
Max. Radio Range	2.1m (measured)	5m (measured)	12m (theoretical)	2m (measured)	15m (theoretical)
Signal Level	-29.75 dBm	-37 dBm	-31 dBm	Not available	Not available
Precision	1.9mm@<1m (measured)	4mm @ 3.6m (measured)	Depth resolution 7.5mm (theoretical)	7.6mm @ >1m (measured)	7.3mm (theoretical)
Energy Efficiency	1554nJ/detection @<1m 7104nJ/detection @>1m**	3900nJ /detection	3300000nJ /detection	428nJ /detection	139000nJ /detection
Detection time	100us	20us	1000us	2us	300us
Number of Arrival pulses	100	100	12500	Not available	3000
Receiver Power Consumption	Max. 1m: 70mW* Max. 2.1m: 320mW**	195mW	3300mW	214mW	695mW
Frequency band (Bandwidth)	4GHz (500MHz)	60GHz (2GHz)	3GHz (2GHz)	144GHz (1.7GHz)	5GHz (5GHz)
Signal Type	Impulse	Multi-Tone	Impulse	Single Tone	Impulse
Application	Location Sensor	Location Sensor	Radar	Radar	Radar
Number of Target	Single	Single	Multi	Single	Multi
Process	65 nm CMOS	40 nm CMOS	180 nm CMOS	65 nm CMOS	130 nm CMOS

** : dynamic power of the sampler is included, ** : power of external amplifier id included*

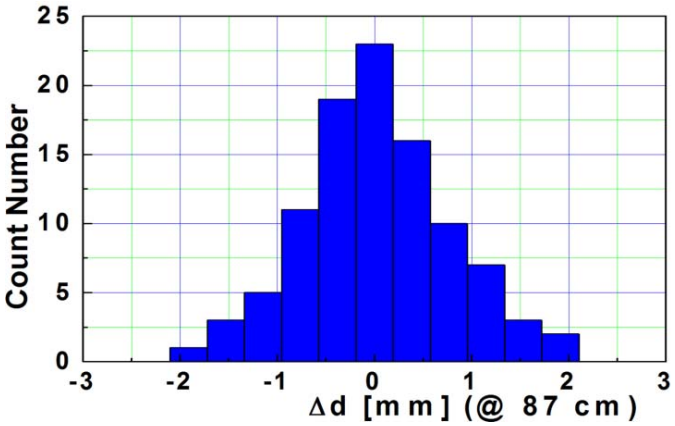
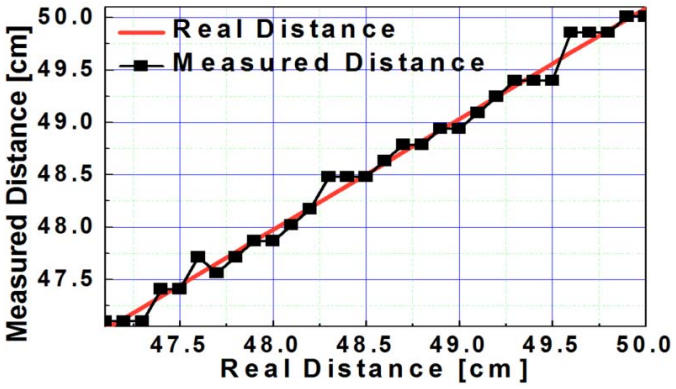


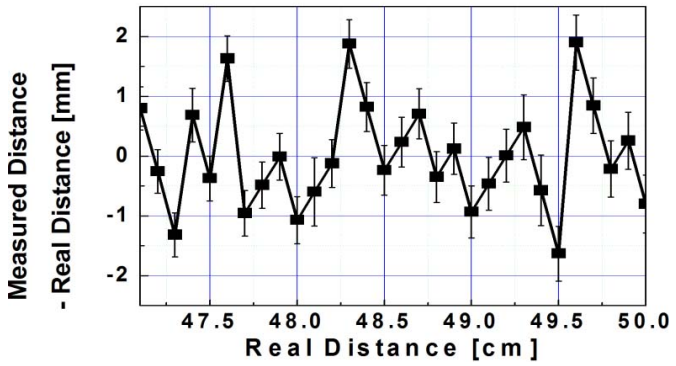
Fig. 22. Histogram of 100 measurement results at 87-cm distance.

from 1 to 2.1 m. As aforementioned, an external amplifier was used in the above measurement setup for the range measurements from 1 to 2.1 m. We performed an average of 100 measurements for each point. Fig. 21 shows that the result is almost identical, compared to the actual distance (red line). Fig. 22 shows the histogram of the 100 measurement results at an 87-cm distance. The x-axis is the distance variation of the measured result with respect to the 87-cm reference, and the y-axis is the number of pulses measured at the corresponding distance. We can see that the 100 measured pulses have a maximum error range of $+/-$ 2 mm, and show a Gaussian distribution. Fig. 23(a) shows the result of the measurement in units of 1 mm at the 47–50 cm range, and Fig. 23(b) shows the error between the measurement results in Fig. 23(a) and the actual distance. The maximum distance error is 1.9 mm. The measurement result of distance which is shown in Figs. 21 and 23 uses one-point calibration which is commonly used in sensor applications [37]. There exists offset between real distance and measured distance because of signal propagation delay from various blocks and printed circuit board trace, etc. An offset is measured by comparing a real distance and a measured distance at 20-cm distance. Then, the offset is used for calibration for all distances.

Table III lists the comparison between the performance of the proposed receiver and the state-of-the-art CMOS receivers used for indoor ranging. The proposed receiver has the best ranging error of 1.9 mm. The reception range can be increased by further optimization of the RF circuits. The energy efficiency of the receiver is 7104 nJ for single detection by taking an average of 100 measurements. This includes the power



(a)



(b)

Fig. 23. (a) Measurement result in units of 1 mm at 47–50 cm range. (b) Error between the measurement results in (a) and the actual distance with 1 σ. (One-point calibration is applied.)

consumption of the external amplifier. If an external amplifier is not used for the range within 1 m, the energy efficiency is 1544 nJ.

V. Conclusion

This paper has proposed a direct-sampling receiver with time-extension method for indoor-location tracking. For this receiver, the time-extension method was applied based on the characteristics of an impulse to overcome the problems of high-speed sampling. Because the proposed method performs high-speed sampling only during the occurrence of a short pulse, and slowly quantizes the sampled signal during dead time, the high-speed impulse signals can be digitized even using low-speed ADC. Furthermore, ToA estimation is performed in the digital domain with high accuracy. The advantages of the time-extension method are as follows.

1) It can have low power consumption because it allows having a low-speed quantizer as well as operating the sampler and quantizer only when a signal exists.
2) High accuracy is possible because it can have a high quantization level with its low-speed quantization. The proposed receiver has the power consumption of 70 mW, and a ranging accuracy of 1.9 mm.

Acknowledgment

The authors would like to thank the School of Integrated Technology and the Yonsei Institute of Convergence Technology for their support.

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