On-Chip Two-Tone Synthesizer Based on a Mixing-FIR Architecture

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***Abstract*— A low-distortion current-steering two-tone sinusoidal signal synthesizer based on a mixing-finite impulse response (FIR) architecture is proposed. The proposed robust synthesizer adopts only digital blocks. It implements a two-stage cascade FIR harmonic cancellation technique that generates a single tone quasi-sinusoidal waveform and suppress the odd-order harmonics up to the 21st order. Differential-mode circuitry and a 50% duty cycle clock are also utilized to cancel the even-order harmonics. The single-tone signal is further up-converted to the desired local oscillator (LO) frequency band, thereby producing the desired two-tone sinusoidal signals. The proposed synthesizer contains a current mirror array implementing the FIR tap coefficients. Accuracy is enhanced using dynamic element matching. The other building blocks consist of a 24-phase clock generator, a current combiner, and a passive mixer with bootstrapped MOS switches. This two-tone synthesizer can be used to conduct a linearity built-in self-test. It is fabricated in 130-nm standard CMOS technology, occupying a 0.056-mm^2 silicon area. Measurement shows better than −68 dBc third-order intermodulation (IM3) below 480-MHz LO frequency without calibration. For the LO frequency <76.8 MHz and the two-tone difference <2 MHz, an IM3 better than −75 dBc can be achieved. The imbalance between the two-tone amplitudes is measured <0.1 dB across the whole frequency range from dc to 1 GHz.**

***Index Terms*— Built-in self-test (BIST), finite impulse response (FIR) filter, harmonic cancellation (HC), linearity, receiver test, sine-wave synthesizer, sinusoidal generator, two-tone signal generator, two-tone test.**

I. Introduction

THIRD-order intermodulation (IM3) distortion, as well as the IM3 interception point (IP3), gives a direct relationship between the input signal level and the linearity. They are very important figures of merits (FoMs) in the measurement and characterization of analog/RF circuits or systems. These parameters characterize the linearity of the device-under-test (DUT). To obtain these key metrics, the two-tone test method is the industry standard. It can be used to measure the linearity of a wide-bandwidth active filter [1], [2], a $\Sigma\Delta$ analog-to-digital converter (ADC) [3], a power amplifier [4], and so on. The two-tone test has also been applied to a wider aspect, such as sensing the electro-chemical impedance of protein [5], and detecting the electro-thermal modulation of conductivity in passive antennas [6].

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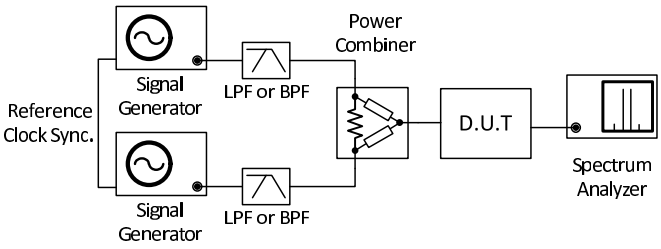


Fig. 1. Traditional two-tone test configuration using testing equipment.

Fig. 1 demonstrates the traditional two-tone test configuration. Two arbitrary waveform signal generators are generating two single tones at different frequencies. Usually, the generated sinusoidal waveforms are not just two tones, but contain some other harmonic components. Thus, two passive low-pass filters (LPFs) or bandpass filters are required to suppress the residue harmonics. A power combiner is used to combine the two single tones and stimulate the DUT with the desired two-tone signal. The spectrum analyzer at the DUT's output will measure the IM3. However, this conventional test bench is bulky and costly. Later in this paper, analysis will show that the IM3 tones in the stimulus are the main measurement error contributor. Therefore, we are proposing a compact on-chip two-tone synthesizer that focuses on suppressing the third-order distortion.

Although the two-tone test is a critical measurement methodology, few papers have discussed potential for on-chip built-in implementation. Ahmad *et al.* [7] propose a direct two-tone generation using two voltage-controlled oscillators (VCOs) in a phase-locked loop. The two VCOs work at different frequencies, and their output waveforms are added together by a linear adder. However, Ahmad *et al.* [7] only report the simulation results; thus, it is difficult to predict the circuit overhead and non-ideality of their proposed design. Digital-to-analog converter (DAC) can also be used for on-chip two-tone generation. Lin and Kuo [8] propose a 10-bit current steering DAC with an improved dynamic element matching (DEM) technique. It achieves −62.16 dBc IM3 with 245- and 247-MHz two-tone signals at 500 MS/s. Lin *et al.* [9] further extend the range of IM3 < -61 dBc over 1.4 GHz in 40-nm technology. It should be noted that [8] and [9] achieve smaller footprints (0.034 mm^2 in 180-nm node and 0.016 mm^2 in 40-nm node, respectively) than that of the other state-of-the-art DACs. However, both of them did not include the extra digital area used for encoding the two-tone signal. In fact, a memory storage block for "replaying" the waveform lookup table or a digital signal processor will consume

a considerable area overhead, such as the digital cores in [10] and [11]. They push the third-order intermodulation below −80 dBc, but occupy 1.6 mm^2 [10] and 3.3 mm^2 [11] in the 65-nm node. In addition, Radulov *et al.* [12], [13] proposed 6-bit DACs with a design-for-testability (DFT) memory. Their compact design is appropriate to be embedded into a modern system-on-chip. However, the 5-kB on-chip memory with 0.048 mm^2 is still larger than the DAC's 0.035 mm^2 core circuit, in 28-nm process. Therefore, these stand-alone high-linearity DACs should be considered overdesigned for the purpose of an on-chip linearity built-in self-test (BIST), which requires a tradeoff between the circuit overhead and the third-order distortion suppression.

Developing a compact two-tone signal synthesizer that can meet the emerging on-chip test demands of analog/RF circuits faces many design challenges. On the one hand, a built-in linearity optimization system has been proposed in [14] for an RF low noise amplifier. It integrates an envelope detector, an ADC, an IM3 calibration unit and an on-chip spectrum analyzer, which is introduced in [15]. Additionally, Chauhan *et al.* [15] further analyze the measurement precision impacted by DAC bit numbers and fast Fourier transform point numbers for an on-chip linearity BIST system. However, such a proposed system relies on external two-tone excitation signals, preventing its full integration. On the other hand, high-linearity single-tone sinusoidal synthesizers have been well researched and applied to the BIST architecture. Elsayed and Sánchez-Sinencio [16] propose a digital harmonic cancellation (HC) technique to generate a sinusoidal waveform from only square wave digital clocks. This achieves a 72-dB total harmonic distortion at 10-MHz output frequency. A high-linearity sine-wave synthesizer, based on a finite impulse response (FIR) filter architecture, is further proposed in [17] for high frequency operation. It demonstrates the sensitivity of timing mismatches for the HC effect and adopts an optimization loop to reduce the errors in the clock distribution network. Similarly, the HC technique can be applied to the two-tone signal generation.

Due to the cumbersome approach of synthesizing and combining two high-frequency sine-wave tones with high linearity, we propose to generate the single tone at a relatively low frequency, move it to the desired high frequency band, and duplicate the single tone. In this paper, an on-chip low-IM3 two-tone synthesizer is proposed, consisting of a cascade FIR architecture and a passive mixer. The cascade FIR architecture implements an HC technique to suppress a large number of odd-order frequency components. It benefits from operating at the low "baseband" frequency (ω_0), which reduces the impact of the delay mismatches in the clock distribution network. Thus, the accuracy of harmonic suppression can be improved. The passive mixer utilizes the nature of up-conversion, and mirrors the "baseband" to two side bands around the local oscillator (LO) frequency $\omega_{\rm LO}$. Two tones with equal amplitudes can then be obtained. The mixer's simple structure is able to minimize the linearity degradation introduced by the MOS transistor switches. The proposed design aims at synthesizing two tones with low IM3 from dc to 1 GHz.

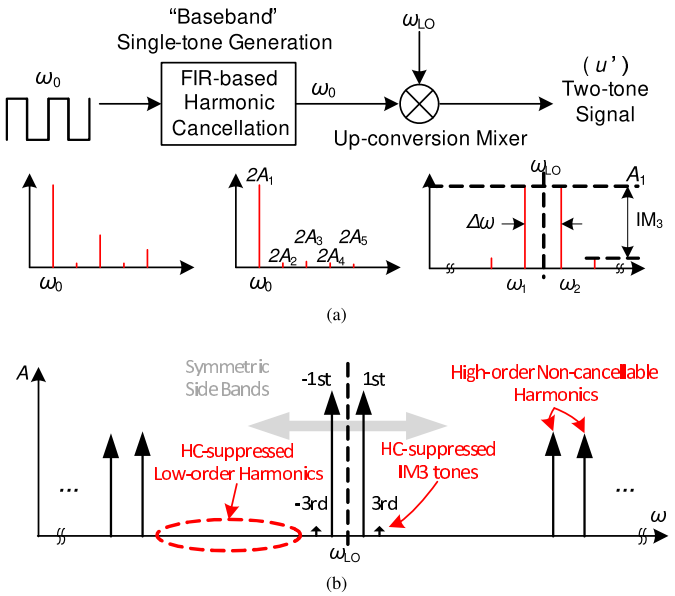


Fig. 2. Two-tone generation architecture concept. (a) Mixing-FIR two-tone generation. (b) Output two-tone signal spectrum.

This paper is organized as follows. The impact on the linearity measurement accuracy by using weakly nonlinear stimulus is analyzed in Section II, as well as the principles of the proposed two-stage cascade FIR architecture. The system architecture and detailed circuit implementation are introduced in Section III. Section IV analyzes the non-ideality effects in the proposed system, such as the timing and the current mismatches, the mixer's linearity, the LO leakage, and the aliasing issue. Section V shows the measurement results, followed by conclusions in Section VI.

II. Two-Tone Generation

A. Two-Tone Signal Generation Architecture

The systematic concept of the proposed mixing-FIR two-tone generator for on-chip linearity BIST is depicted in Fig. 2(a). It implements the fully differential circuit to cancel the even-order harmonics, and uses the FIR-based HC technique to suppress multiple odd-order harmonics. The "baseband" quasi-sinusoidal single-tone signal is generated at the frequency, $\omega_0 = \Delta\omega/2$, where $\Delta\omega = \omega_2 - \omega_1$ is the expected difference frequency between the two tones. A highly linear up-conversion mixer was also adopted to mirror the single-sideband to dual bands and move them around the desired frequency $\omega_{\rm LO}$. Note that we have $\omega_1 = \omega_{\rm LO} - \omega_0$ and $\omega_2 = \omega_{\rm LO} + \omega_0$. Ideally, the two-tone test method (Fig. 1) can generate mostly pure spectrum with only two tones. Correspondingly, as derived in [17], all odd-order harmonics can be suppressed if and only if the FIR architecture has an infinite number of FIR taps, which is not practical in the real circuit design. On the contrary, a limited number of FIR taps eliminates lower order harmonics but leaves higher order non-cancellable harmonics, and they are also up-converted by the mixer, as shown in Fig. 2(b). The spectrum of the output two-tone signal in the proposed design is not theoretically pure. Its impact on IM3 measurement precision

is analyzed in Section II-B, and its aliasing issue is discussed in Section IV-D.

B. Linearity Test Using Weakly Nonlinear Stimulus

The ideal two-tone stimulus signal u is a combination of two sinusoidal waveforms with the same amplitude of A_1

$$u = A_1 \cos(\omega_1 t) + A_1 \cos(\omega_2 t). \tag{1}$$

The DUT is characterized as a nonlinear system (ignoring the dc term), $y = k_1 u + k_2 u^2 + k_3 u^3 + \cdots$, where k_1 is the linear gain of the DUT, and k_2, $k_3, \ldots$, indicate the DUT's nonlinear coefficients. The DUT's linearity can be evaluated by the normalized IM3 [18]

$$\text{IM}_3(\text{dBc}) = \frac{3}{4}\frac{k_3}{k_1}A_1^2 \tag{2}$$

when the low-distortion conditions hold. This includes the mostly linear DUT criteria ($k_1 \gg k_2, k_3 \cdots$) and the relatively low stimulus amplitude criteria ($k_1 A_1 \gg k_3 A_1^3$). In this paper, for short, we use IM3 in dBc to present the normalized value. Particularly, IP3 is defined at the point where $\text{IM}_3 = 0$ dBc. However, note that the analysis in [18] is based on ideal sinusoidal waveforms. In the proposed design, the HC is not perfect due to the mismatches and the process-voltage-temperature (PVT) variations. The "baseband" single tone is still considered a weakly nonlinear waveform. Assuming an ideal up-conversion and ignoring the dc term, the two-tone output signals in Fig. 2(a) can be expressed as

$$u' = \cos(\omega_{\text{LO}} t) \cdot (2A_1 \cos(\omega_0 t) + 2A_2 \cos(2\omega_0 t) + \cdots) \tag{3}$$

where $2A_1$ is used to have the same major tone power as that of (1). Harmonic coefficients A_i are annotated in Fig. 2(a). Under the same low distortion conditions, the actual measured IM3 can be approximated as

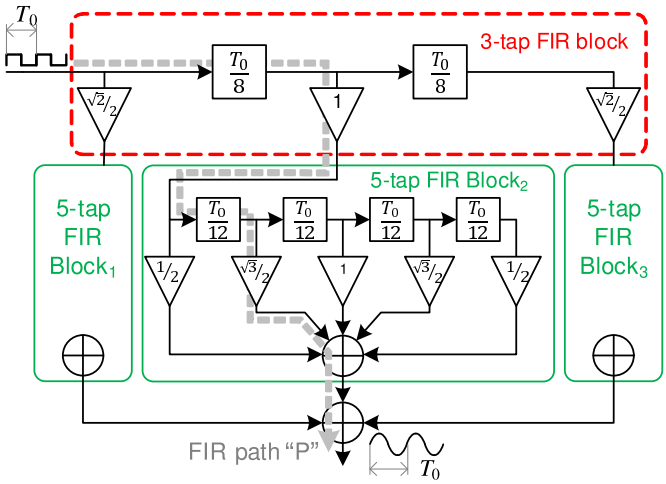
$$\begin{aligned}\text{IM}_3 = {} & \frac{3}{4}\frac{k_3}{k_1}A_1^2 + \varepsilon, \varepsilon \approx \frac{A_3}{A_1} + \frac{9}{2}\frac{k_3}{k_1}A_1 A_3 \\ & + \frac{9}{4}\frac{k_3}{k_1}A_1 A_5 + \frac{9}{2}\frac{k_3}{k_1}\sum_{i=1}^{\infty} A_{2i+1}(A_{2i+3} + A_{2i+5})\end{aligned} \tag{4}$$

where ε is the deviation from the conventional IM3. A_3/A_1 is the relative third-order harmonic amplitude of the "baseband" signal at ω_0. The derivation shows that all "baseband" harmonics will affect the IM3 measurement precision. However, the third-order harmonic (A_3) has the most significant impact on the IM3 measurement accuracy if the proposed architecture is used.

C. Cascade FIR-Based Harmonic Cancellation

Shi and Sánchez-Sinencio [17] have proposed a sinusoidal signal generator based on the FIR filter approach, whose implementation uses only multiple delayed square-wave clocks. The proposed M-tap FIR filter suppresses odd-order harmonics up to the $(2M+1)$th order with designated tap coefficients

$$c_i = \cos\left(\frac{(i+1)\pi}{M+1} - \frac{\pi}{2}\right), \quad (i = 0, 1, \ldots, M-1). \tag{5}$$



M	c_0	c_1	c_2	c_3	c_4
3	$\frac{\sqrt{2}}{2}\left(\frac{12}{17}\right)$	1	$\frac{\sqrt{2}}{2}\left(\frac{12}{17}\right)$		
5	$\frac{1}{2}$	$\frac{\sqrt{3}}{2}\left(\frac{13}{15}\right)$	1	$\frac{\sqrt{3}}{2}\left(\frac{13}{15}\right)$	$\frac{1}{2}$

Fig. 3. Proposed two-stage cascade FIR HC and tap coefficients for the "baseband" single-tone generation.

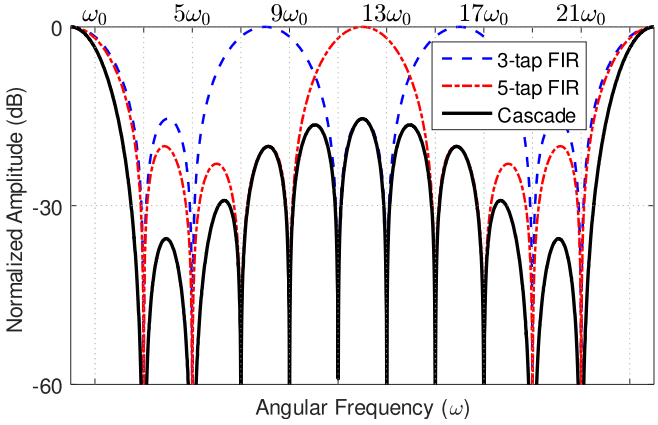


Fig. 4. Frequency response of the cascade FIR architecture.

The five-tap ($M = 5$) single-tone generation architecture implemented in [17] can achieve 55-dBc maximum spur free dynamic range (SFDR) without any tuning after fabrication.

In this paper, we propose a two-stage cascade FIR filter architecture to further suppress the third-order harmonic and push the residue odd-order harmonics to higher frequencies as shown in Fig. 3. The first stage is a three-tap FIR block, and the second stage consists of three identical five-tap blocks (annotated as Block$_1$, Block$_2$, and Block$_3$). T_0 is the period of the output quasi-sinusoidal waveform's fundamental tone ($T_0 = 2\pi/\omega_0$), M is the number of FIR taps, and $c_0, c_1, \cdots$ are tap coefficients obtained from (5). For irrational c_i, we can approximate $(3)^{1/2}/2 \approx 13/15$ and $(2)^{1/2}/2 \approx 12/17$. The quantization errors are only $+0.07\%$ and -0.17%, respectively. Moreover, an FIR path is defined from the input to the output, which passes through multiple delays and through two exact tap coefficients as path "P" shown in Fig. 3. Section III-A will show how to rearrange the FIR path for practical hardware implementation. Fig. 4 shows the frequency response of the proposed architecture.

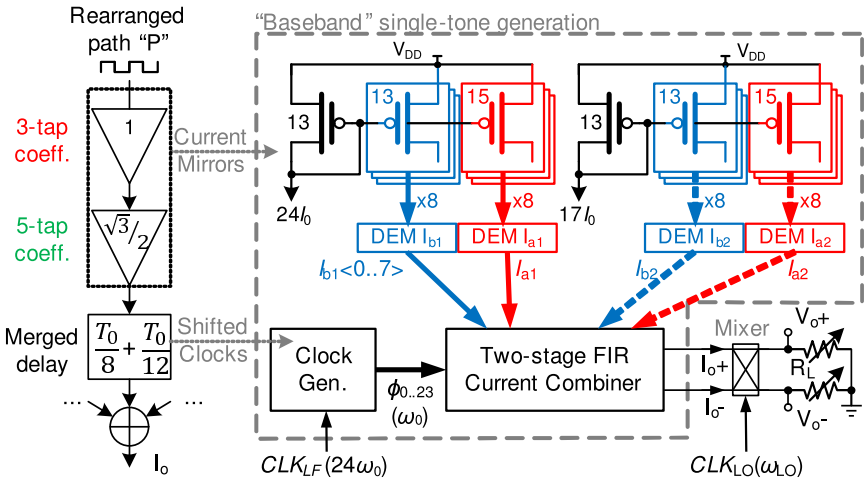


Fig. 5. System architecture of the proposed two-tone synthesizer and the corresponding rearranged FIR path.

The first non-cancellable harmonic is pushed to the 23rd order, and all lower odd-order harmonics are eliminated. To achieve the same HC effect, a single stage approach proposed in [17] would require $M = 11$ (11 taps); thus, a high precision circuit becomes necessary to achieve a series of fractional coefficients obtained from (5) (0.259, 0.5, 0.707, 0.866, 0.966, and 1). Instead, the proposed cascade architecture separates the coefficients into two groups and each group has only two unique factors. The three-tap FIR stage adopts coefficients 1 and 12/17, while 1/2 and 13/15 can cover the five-tap FIR stage (1 is not a unique coefficient as it can be represented by $2 \times 1/2$). This coefficient selection significantly reduces the hardware implementation complexity. Detailed implementation, which uses two different current biases and two different transistor sizes, is discussed later in Section III-B. Moreover, the notching points of the FIR frequency responses will become finite due to the PVT variations as discussed in [17]. The cascade architecture can help emphasize the cancellation of third-order harmonic by stacking a five-tap FIR over a three-tap FIR, which both have a notching point at $3\omega_0$.

Additionally, assuming the FIR architecture has an ideal response, as shown in Fig. 4, and its input is an ideal square wave, we can derive $A_1 = 1$, $A_{23} = 1/23$, $A_{25} = 1/25$, $A_{47} = 1/47$, $\cdots$. The SFDR shown in Fig. 2(b) is not better than 27.2 dB (1/23). However, applying all these components to (4), the measurement error (ε) is around 1.6% compared to the theoretical measured value in (2). It is negligible. Therefore, the design of this cascade FIR architecture should focus on improving the third-order cancellation. Details will be discussed in Section IV-A.

III. Circuit Implementation

A. System Architecture

The conceptual two-tone generation architecture in Fig. 2(a) can be implemented by the system demonstrated in Fig. 5 after rearranging the FIR paths. To illustrate, path "P" in Figs. 3 and 5 shows the proposed rearrangement. On the one hand, tap coefficients are put together and implemented by a current mirror array. In detail, the three-tap coefficients are achieved by two different bias currents, while the current mirror ratios are used to produce the five-tap coefficients. On the other hand, the FIR delays across the whole path are merged together. The total delay of path "P" is $T_0/8+T_0/12 = 5T_0/24$, which is implemented via a MOS switch driven by the clock ϕ_5 with $5T_0/24$ delay in the current combiner. Generally, 50% duty-cycled $\phi_k (k = 0 \ldots 23)$ has a delay of $kT_0/24$. They are used to represent any FIR path delay in Fig. 3. In addition, PVT variations will cause mismatches in a current mirror [19]. The DEM technique is further implemented to alleviate this issue, and Aluthwala *et al.* [20] have proven the DEM able to improve the linearity of sine-wave synthesis. Following the "baseband" single-tone generator, a differential quasi-sinusoidal current waveform I_O is then up-converted to the desired ω_{LO} band by an up-conversion mixer and outputs the voltage waveform V_O across R_L.

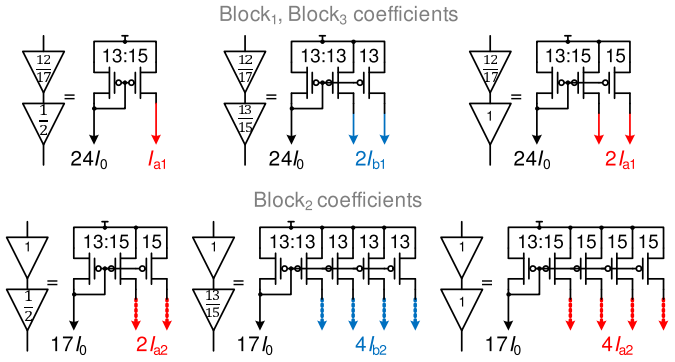


Fig. 6. Current mirror implementation of the two-stage FIR coefficients.

B. Current Mirror Array for FIR Tap Coefficients

The relationship between the FIR tap coefficients of Fig. 3 and the current branches of Fig. 5 is further explained in Fig. 6. Considering the five-tap FIR coefficients $1/2 : 13/15 : 1 = 15 : 13 \times 2 : 15 \times 2$, one I_{a1} branch is used for the tap coefficient 1/2, two I_{a1} branches for 1, and two I_{b1} branches

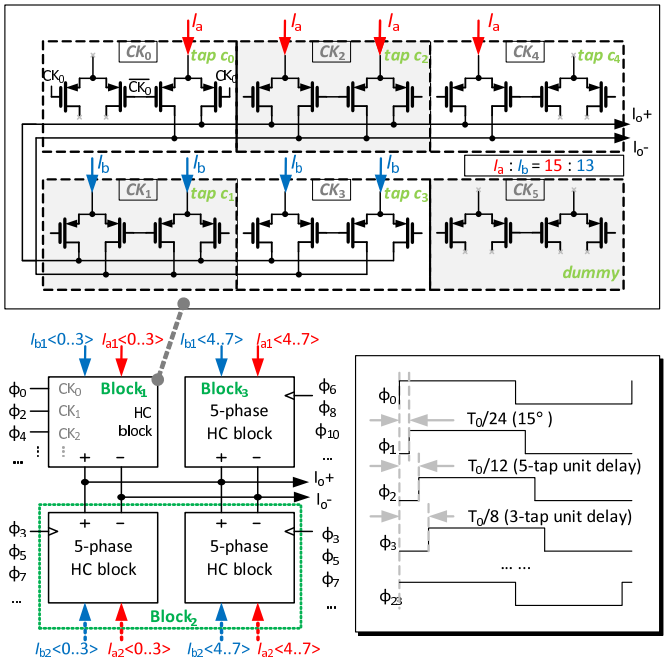


Fig. 7. Current combiner topology and clock connections of the proposed two-stage FIR architecture.

for 13/15. As a result, eight I_{a1} and eight I_{b1} can cover all the tap coefficients of Block$_1$ and Block$_3$ in Fig. 3. To implement Block$_2$, two I_{a2} branches are used for representing 1/2, four I_{a2} for 1, and four I_{b2} for 13/15. Note that the number of current branches used are doubled so as to reuse the 16-branch current mirror design and the DEM blocks. Furthermore, we have three-tap coefficients $12/17 : 1 = 24 : 17 \times 2$, this leads to the bias currents, $24I_0$ and $17I_0$, in Fig. 5, where I_0 is a unit current. These current ratios work together with the clock connection pattern, which will be introduced below to achieve the function of the proposed cascade FIR architecture. Additionally, as shown in Fig. 5, four DEM current branch rotators shuffle each of the eight current channels and output I_{a1}<0..7>, I_{b1}<0..7>, I_{a2}<0..7>, and I_{b2}<0..7> to the following current combiner, where the annotation <$i..j$> is used to index the channel number from i to j.

C. Clock Divider and Current Combiner for FIR Tap Delays

The clock divider is implemented by a 24-bit cyclic shifted register. It is driven by $\mathrm{CLK_{LF}}$ at a frequency of $24\omega_0$, and cyclically shifts twelve 1s followed by twelve 0s. The output ports of 24 registers are used as $\phi_{0...23}$. Noting that $T_0 = 2\pi/\omega_0$, each ϕ_i and ϕ_{i+1} pair has a delay of $T_0/24$ (15° phase shift) between them. Moreover, the two-stage cascade FIR current combiner is implemented as an extra layer of PMOS switches, as demonstrated in Fig. 7. It consists of four five-phase HC blocks. Each five-phase HC switching block is switched by six clocks, $\mathrm{CK}_{0...5}$, and the corresponding inverted phases, $\overline{\mathrm{CK}_{0...5}}$. Fig. 7 shows that, CK_0 and CK_4 switch one I_a channel, respectively. CK_2 switches two I_a channels. CK_1 and CK_3 switch two I_b channels separately. If $I_a : I_b = 15 : 13$ and the delay between CK_i and CK_{i+1} is

TABLE I

24-PHASE CLOCK AND CURRENT BRANCH CONNECTION PATTERN (Ø REPRESENTS THE DUMMY CONNECTION)

$\overline{\phi}$	ϕ_0	ϕ_1	ϕ_2	ϕ_3	ϕ_4	ϕ_5
I_O	$+I_{a1}$<0>	Ø	$+I_{b1}$<0>	$+I_{a2}$<0>	$+I_{a1}$<1>	$+I_{b2}$<0>
	Ø	Ø	$+I_{b1}$<1>	Ø	$+I_{a1}$<2>	$+I_{b2}$<1>
	$-I_{b1}$<6>	Ø	$-I_{a1}$<7>	$+I_{a2}$<4>	Ø	$+I_{b2}$<4>
	$-I_{b1}$<7>	Ø	Ø	Ø	Ø	$+I_{b2}$<5>
$\overline{\phi}$	ϕ_6	ϕ_7	ϕ_8	ϕ_9	ϕ_{10}	ϕ_{11}
I_O	$+I_{b1}$<2>	$+I_{a2}$<1>	$+I_{a1}$<3>	$+I_{b2}$<2>	Ø	$+I_{a2}$<3>
	$+I_{b1}$<3>	$+I_{a2}$<2>	Ø	$+I_{b2}$<3>	Ø	Ø
	$+I_{a1}$<4>	$+I_{a2}$<5>	$+I_{b1}$<4>	$+I_{b2}$<6>	$+I_{a1}$<5>	$+I_{a2}$<7>
	Ø	$+I_{a2}$<6>	$+I_{b1}$<5>	$+I_{b2}$<7>	$+I_{a1}$<6>	Ø
$\overline{\phi}$	ϕ_{12}	ϕ_{13}	ϕ_{14}	ϕ_{15}	ϕ_{16}	ϕ_{17}
I_O	$-I_{a1}$<0>	Ø	$-I_{b1}$<0>	$-I_{a2}$<0>	$-I_{a1}$<1>	$-I_{b2}$<0>
	Ø	Ø	$-I_{b1}$<1>	Ø	$-I_{a1}$<2>	$-I_{b2}$<1>
	$+I_{b1}$<6>	Ø	$+I_{a1}$<7>	$-I_{a2}$<4>	Ø	$-I_{b2}$<4>
	$+I_{b1}$<7>	Ø	Ø	Ø	Ø	$-I_{b2}$<5>
$\overline{\phi}$	ϕ_{18}	ϕ_{19}	ϕ_{20}	ϕ_{21}	ϕ_{22}	ϕ_{23}
I_O	$-I_{b1}$<2>	$-I_{a2}$<1>	$-I_{a1}$<3>	$-I_{b2}$<2>	Ø	$-I_{a2}$<3>
	$-I_{b1}$<3>	$-I_{a2}$<2>	Ø	$-I_{b2}$<3>	Ø	Ø
	$-I_{a1}$<4>	$-I_{a2}$<5>	$-I_{b1}$<4>	$-I_{b2}$<6>	$-I_{a1}$<5>	$-I_{a2}$<7>
	Ø	$-I_{a2}$<6>	$-I_{b1}$<5>	$-I_{b2}$<7>	$-I_{a1}$<6>	Ø

$T_0/12$, this five-phase HC block realizes a single five-tap FIR block shown in Fig. 3. In order to balance the load of each clock signal, dummy switch pairs are added for CK_0, CK_4, and CK_5. Fig. 7 also illustrates the full current-combining topology. The five-phase HC block, which is equivalent to Block$_1$ in Fig. 3, accepts I_{a1}<0..3> and I_{b1}<0..3> as equivalent tap coefficients. It also uses ϕ_0, ϕ_2, ϕ_4, ϕ_6, ϕ_8, and ϕ_{10} for $\mathrm{CK}_{0...5}$. Additionally, ϕ_{12}, ϕ_{14}, ϕ_{16}, ϕ_{18}, ϕ_{20}, and ϕ_{22} are used as the inverted $\overline{\mathrm{CK}_{0...5}}$. Similarly, Block$_3$ equivalent block is driven by ϕ_6, $\phi_8, \ldots, \phi_{22}$, ϕ_0, ϕ_2, and ϕ_4. It takes the remaining I_{a1}<4..7> and I_{b1}<4..7>. Block$_2$ is achieved by two identical five-phase HC blocks, whose $\mathrm{CK}_{0...5}$ and $\overline{\mathrm{CK}_{0...5}}$ are ϕ_3, $\phi_5, \ldots, \phi_{23}$, and ϕ_1. It takes all I_{a2}<0..7> and I_{b2}<0..7>. This special pattern of clock connections guarantee a balanced load for each phase of $\phi_{0...23}$. The delay between ϕ_i and ϕ_{i+2} is $T_0/12$, and the delay between ϕ_i and ϕ_{i+3} is $T_0/8$, which are the unit delays in the five-tap and three-tap FIR blocks of Fig. 3, respectively. Finally, all the current branches are summed together to output the differential quasi-sinusoidal current waveform I_O. Table I summarizes all clock and current connection patterns for the proposed cascade FIR architecture, where the current flowing into I_O+ is indicated by "+," and "−" marks the current flowing into I_O-. Because the PMOS switches are adopted in this design, $\overline{\phi}$ is used to indicate the inverted clock phases.

D. Up-Conversion Mixer

The up-conversion mixer block illustrated in Fig. 5 is implemented as shown in Fig. 8. It moves the generated "baseband" single tone up to the desired high frequency band centered at ω_{LO} and converts the current waveform I_O to the output voltage waveform V_O. In order to reduce the switches' ON resistance, to extend the output voltage swing, and to minimize the impact on linearity, bootstrapped NMOS switches [21] are adopted. The switching NMOS transistors, M_{N1} and M_{N2}, are implemented using twin-well devices and their source terminals are connected to the bulk. Two R_L resistor arrays

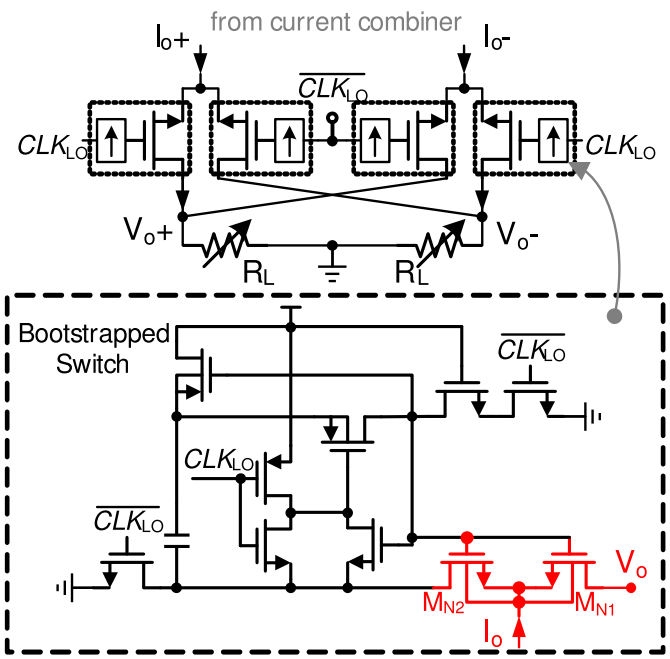


Fig. 8. Passive up-conversion mixer with bootstrapped MOS switches.

are also implemented on-chip as the loads of the mixer. They are digitally controlled and can be manually adjusted (e.g., set to 200 Ω in this design) for impedance matching and test purpose. The major drawback of the proposed mixer design is the LO leakage. Especially, the high gate switching voltage deteriorates the isolation between I_O and $CLK_{\rm LO}$. However, analysis in Section IV will show that the leakage tone still has limited impact on the two-tone test accuracy. In addition, several techniques can help to further extend the proposed mixer's working frequency range to cover more RF applications at the expense of larger area and power consumption. The local mixer array architecture suggested in [22] is able to improve the mixer's linearity at high LO frequencies and it is compatible to the proposed design. I/Q modulation and LO cancellation techniques [23] have been well researched for communication systems, and they can be adopted to reduce the LO leakage.

E. 3-bit DEM Rotator

Fig. 9 illustrates the structure of the DEM current branch rotator. Each current branch rotator is controlled by three control bits to shift the eight-channel current branches cyclically. A 16-bit linear feedback shift register (LFSR) generates the control bits, and each DEM rotator receives a different group of control bits, so as to avoid identical patterns. The chosen feedback taps, B_{10}, B_{12}, B_{13}, and B_{15}, guarantee that the LFSR can cycle through the maximum number of 65 535 states except for the all-zero state. All DEM current branch rotators are driven by a clock of $\rm CLK_{LF}$ divided by 8, which is at a frequency of $3\omega_0$.

IV. Non-Ideality Analysis

A. Baseband Current Mismatch and Phase Error

For the "baseband" single tone signal generation, there are two major error sources—the amplitude error induced by

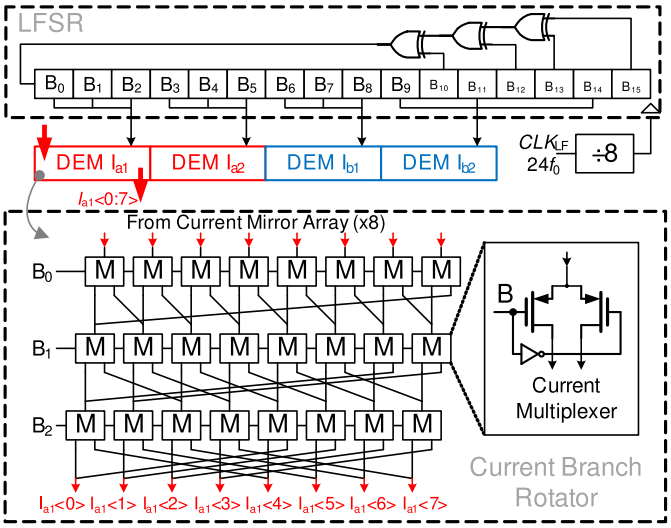


Fig. 9. Current branch rotator with DEM.

current mirror mismatches and the clock phase error induced by delays in the clock divider and distribution network. To analyze the impact factors on the linearity of the generated "baseband" single tone signal, the current errors are annotated as $\Delta I_{\{a1,a2,b1,b2\}}$<0..7>. I_i is used to represent all current branches switched by clock ϕ_i. The detailed combination pattern can be found in Table I. For example, we have $I_0 = +I_{a1}$<0> $- I_{b1}$<6> $- I_{b1}$<7>. The corresponding error term is denoted as ΔI_i. Moreover, θ_i is the phase of the clock ϕ_i. $\phi_{0\ldots23}$ are equally distributed clocks, and thus $\theta_i = \pi/12 \cdot i$, $i = 0, 1, \ldots, 23$. $\Delta\theta_i$ is the annotation of the ith phase error. Consider the Fourier series of the "baseband" output current I_O

$$I_O(t) = \sum_{k=1}^{+\infty} X_k \cos(k\omega_0 t) + Y_k \sin(k\omega_0 t). \tag{6}$$

Noting that $I_i = -I_{i+12}$ for $i = 0, 1, \ldots, 11$, X_k and Y_k in (6) can be expressed as

$$X_k = -\frac{2}{k\pi} \sum_{i=0}^{11} (I_i + \Delta I_i)[M_{k,i} \sin(k\theta_i) + N_{k,i} \cos(k\theta_i)] \tag{7}$$

$$Y_k = \frac{2}{k\pi} \sum_{i=0}^{11} (I_i + \Delta I_i)[M_{k,i} \cos(k\theta_i) - N_{k,i} \sin(k\theta_i)] \tag{8}$$

$$\begin{aligned} M_{k,i} &= \cos(k \cdot \Delta\theta_i) - (-1)^k \cos(k \cdot \Delta\theta_{i+12}) \\ N_{k,i} &= \sin(k \cdot \Delta\theta_i) - (-1)^k \sin(k \cdot \Delta\theta_{i+12}) \end{aligned} \tag{9}$$

where $A_k = (X_k^2 + Y_k^2)^{1/2}, k = 1, 2, 3, \cdots$ are the magnitude components of $I_O(t)$, also known as the "baseband" components described in Fig. 2(a) and (3).

Two-hundred runs of Monte-Carlo simulation are carried out to obtain the mismatch distribution in the current mirror and the clock distribution network; thus, I_i, ΔI_i, and $\Delta\theta_i$ can be obtained. It should be mentioned that DEM is not applied in this analysis. Fig. 10 shows the numeric simulation results with the fundamental "baseband" frequency $f_0 = 1$ MHz. Fig. 10(a) demonstrates the simulated percentage of the deviation from the expected current ($\Delta I_i / I_i \cdot 100\%$) in

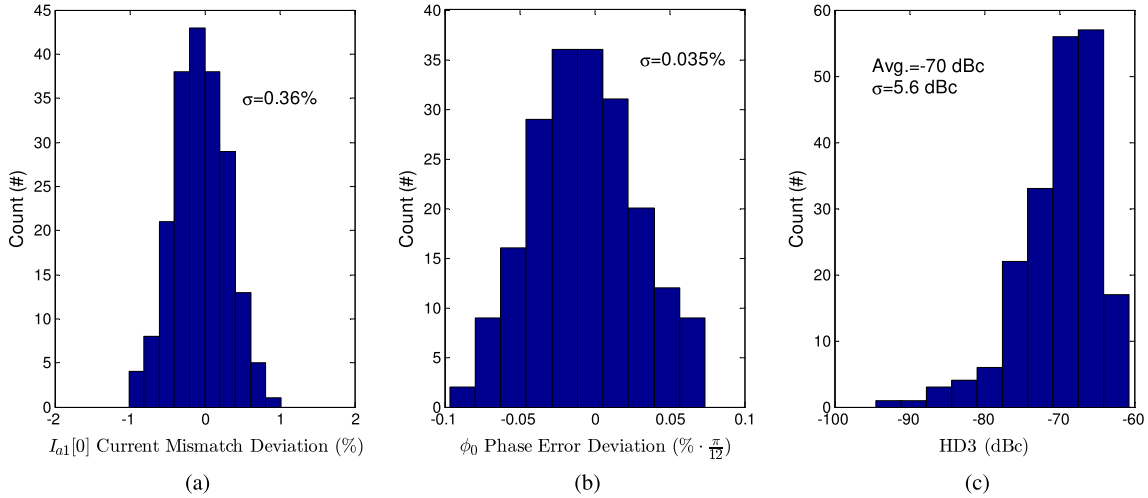


Fig. 10. Monte-Carlo simulation results. (a) I_{a1}<0> branch current deviation. (b) Phase error deviation of ϕ_0. (c) Distribution of the HD3 calculated from the current and the clock phase mismatches.

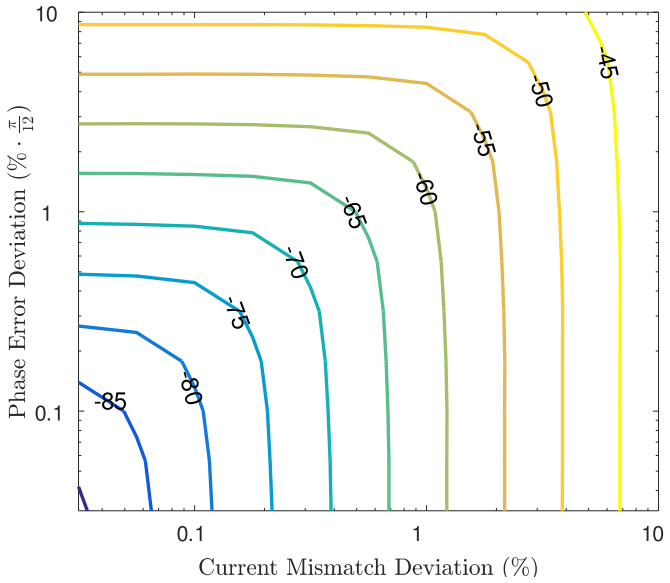
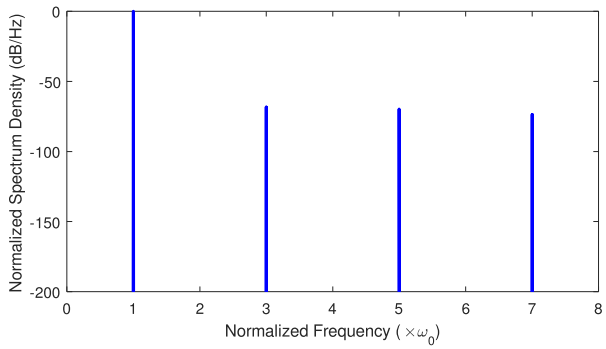


Fig. 11. Contour of the simulated average HD3 by sweeping the current mismatch and the clock phase error.

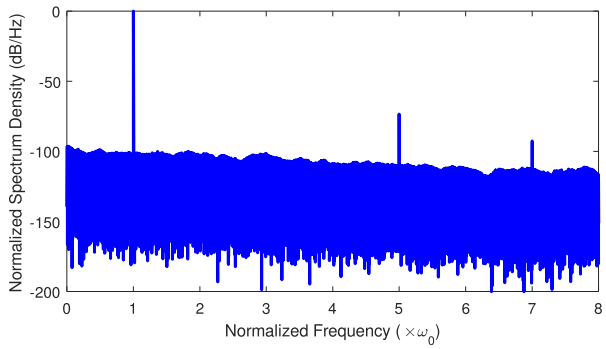
branch I_{a1}<0>. Moreover, the percentage of the deviation from the expected clock phase in ϕ_0 is also illustrated in Fig. 10(b). By applying the statistical data I_i, ΔI_i, and $\Delta\theta_i$ to (6), we can obtain the distribution of the I_O waveform third-order harmonic distortion (HD3) in Fig. 10(c). It shows an average of −70 dBc HD3. Further numerical analysis uses the Monte-Carlo simulation data as a baseline and sweeps the clock phase error deviation and the current mismatch deviation. The newly generated data are fed into (6), leading to the average HD3 performance, which is shown in Fig. 11. It can be found that, to achieve −70 dBc HD3, about 0.3% errors for both the current mismatch and clock phase error are required. 0.1% errors make the HD3 below −80 dBc. Moreover, if an error factor is much bigger than the other, it will become the dominant error source. For instance, 1% current mismatch and 1% phase error result in about −60.5 dBc HD3. If the phase error is reduced to 0.03%, we still have −61.4 dBc HD3. Thus, to increase the "baseband" linearity, both of the current mismatch and the clock phase error should be improved. On the one hand, because the delays in the clock distribution network are almost fixed after fabrication, lower ω_0, which means longer clock period, can help decrease the percentage of delay errors. On the other hand, the DEM technique is introduced to alleviate the current magnitude mismatch when it becomes the dominant error source. To sum up, the mismatched currents and clock phases are both important factors when dealing with the linearity of the "baseband" single tone generation.

B. Dynamic Element Matching

The DEM technique can randomize the branch currents and thus relaxes the matching requirement of the current mirrors. However, it also raises the noise floor of the "baseband" sinusoidal output, deserving further analysis. A behavior model of the "baseband" synthesizer, which adopts the functionality of the proposed DEM approach in Fig. 9, is implemented with the aforemetioned current mismatch data ($\sigma = 0.36\%$). Ideal clock phases are used so as to reveal the intrinsic noise floor induced by the DEM. Fig. 12(a) and (b) demonstrates the normalized power spectrum density (PSD) before and after turning on the DEM for one group of current mismatch data. The DEM reduces the HD3 from a −68 dBc harmonic tone to a noise floor of −102 dBc. The average noise floor obtained from two-hundred Monte-Carlo runs is −105 dBc. Moreover, the distribution of ΔI_i will also affect the noise level. Fig. 13 shows the average noise floor versus different current mismatch deviations. The proposed DEM provides an average 35-dB suppression to the third-order harmonic. To conclude, the DEM technique significantly reduces the HD3 induced by the current mismatch and thus makes the "baseband" synthesizer more sensitive to the clock phase error. The chosen $\sigma = 0.36\%$ current mismatch deviation in this design is considered conservative. In other words, the current mirror array could be designed smaller without much linearity degradation penalty.



(a)



(b)

Fig. 12. Simulated PSD with current mismatches. (a) DEM OFF. (b) DEM ON.

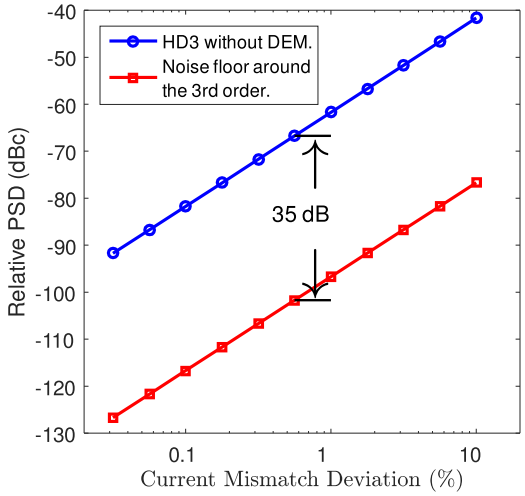


Fig. 13. Simulated HD3 suppression by using the proposed DEM technique.

C. Nonlinear Up-Conversion

The linearity of the passive CMOS mixer has been analyzed in [24], and its conclusion can be applied to the design of the passive mixer in the proposed architecture. Considering the "baseband" single tone generator is an equivalent current-steering DAC, the input impedance of the mixer is large due to the current mirror structure. This impedance is optimal for the mixer's linearity. Particularly, an LPF cannot be implemented to purify the "baseband" signal, such as the one proposed in [17]. Any extra capacitance introduced by an

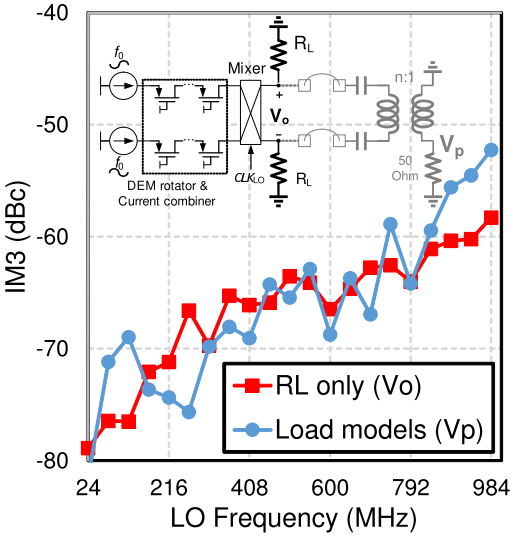


Fig. 14. Simulated IM3 of the passive mixer ($f_0 = 1$ MHz).

LPF may reduce the mixer's input impedance at high frequencies, and, thus, degrade its linearity performance. Moreover, Khatri *et al.* [24] also suggest using low load impedance to improve the linearity. $R_L = 200\ \Omega$ load resistance (see Fig. 5) is adopted in this design. It is reasonable for an on-chip BIST application, which allows the proposed design to drive most DUTs on-chip and significantly reduces the area and power overhead, compared to a 50-Ω load. LO frequency is also a factor that affects the mixer's linearity. To evaluate the mixer's frequency-dependent linearity degradation, a schematic with only resistive load is simulated, compared to another simulation taking the bondwire and the balun models into consideration. The simulated IM3 obtained on V_O and V_P at $f_0 = 1$ MHz are depicted in Fig. 14, as well as the detailed schematic. It can be found that the external components used for test purpose introduce more fluctuation to the output IM3 due to the changing impedance matching conditions. However, in the on-chip BIST application scheme, this fluctuation should not be a concern. From Fig. 14, we can find the simulated IM3 keeps increasing when the LO frequency rises. To the contrary, if given a fixed ω_0, the "baseband" HD3 is almost fixed because the clock phase errors and the current mismatches will not change too much. As the output linearity is determined by both the "baseband" generator and the mixer, at high LO frequency, the output IM3 will increase as the mixer dominates the linearity degradation. While at low LO frequency the output IM3 will keep almost the same, because the "baseband" becomes the major source of IM3 tones.

D. Aliasing of the Residue Harmonics

In Section II-C, we showed that the first non-cancellable harmonic is pushed to the 23rd order. As a result, multiple residue harmonics are located at $(24k \pm 1) \cdot \omega_0$, where $k = 1, 2, \cdots$. The equivalent input of the cascade FIR architecture is a square wave, the closest two significant harmonics, the 23rd and the 25th order, still have high amplitudes $1/(24k \pm 1)$, -27.2 and -28.0 dBc, respectively. The up-conversion mixer adopts the passive switching structure, which

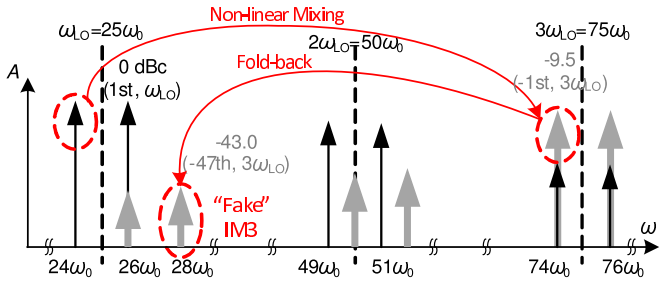


Fig. 15. "Fake" IM3 induced by fold-back harmonics.

has a strong nonlinear mixing behavior, leading to aliasing issues. By replacing $\cos(\omega_{LO}t)$ in (3) with the Fourier series of a square wave, $4/\pi \sum_{l=0}^{\infty} 1/(2l+1) \cdot \cos[(2l+1)\omega_{LO}t)]$, the aliasing will spread the residue harmonics across the whole spectrum, locating at $(2l+1)\omega_{LO} \pm (24k \pm 1)\omega_0$, where $l = 1, 2, \cdots$. Without a carefully chosen ω_{LO} and ω_0, some residue harmonic may fold back to the IM3 frequency, leading to a high "fake" IM3. As shown in Fig. 15, assuming we have $\omega_{LO} = 25\omega_0$, the two major tones are at $\omega_1 = 24\omega_0$ and $\omega_2 = 26\omega_0$, and the IM3 tones emerge at $2\omega_1 - \omega_2 = 22\omega_0$ and $2\omega_2 - \omega_1 = 28\omega_0$. If we have $l = 1$ and $k = 2$, the nonlinear mixing first duplicates the "baseband," centering at $3\omega_{LO}$ and attenuates the whole band by 9.5 dB. The -47th order residue harmonic (where the minus indicates the left side band of $3\omega_{LO}$) of the duplicated band will fold back to $3\omega_{LO} - 47\omega_0 = 28\omega_0$. It has an amplitude of -43.0 dBc, which is much higher than the originally suppressed IM3 tone. To prevent having high "fake" IM3 tones, one solution is to set ω_{LO} an integer multiple of ω_0, but avoid $(12m \pm 1)\omega_0$ or $(12m \pm 2)\omega_0$, where m is an integer number. Fractional multiple of ω_0 can also be used. However, this will make it more complicated to judge whether the "fake" IM3 tones exists. It will also prevent ω_{LO} from being divided to obtain ω_0; and thus an extra clock source is needed.

E. LO Leakage and Imbalance

The analysis above covers different error sources that cause the degradation of IM3. Apart from the two fundamental tones and the corresponding two IM3 tones that will appear in the output spectrum, there are some other tones emerging around ω_{LO}. On the one hand, the usage of a passive mixer raises a concern that the output waveform V_O contains the LO leakage signal, which appears at ω_{LO}. On the other hand, it is difficult to make a fully symmetric layout design or achieve a 50% duty cycle LO clock at high frequency; thus, imbalance is introduced to the output waveform. To take these non-ideal factors into consideration, we can rewrite (3) as

$$u'' = u' + B\cos(\omega_{LO}t) + C\cos[(\omega_{LO} \pm 2\omega_0)t] \quad (10)$$

where B is the amplitude of the LO leakage signal, and C is used to approximate the imbalance. Therefore, by counting A_1 and A_3, extra terms are added into the error in (4)

$$\varepsilon' \approx \varepsilon + \frac{3}{4}\frac{k_3}{k_1}\left[\frac{A_3}{A_1}(3B^2 + 6C^2) + 3C^2 + 6BC\right]. \quad (11)$$

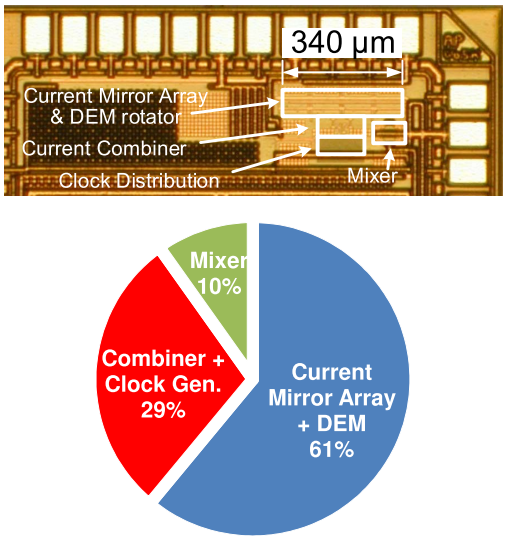


Fig. 16. Die photograph and block area distribution of the proposed two-tone generator.

It can be concluded that, even if the LO leakage amplitude (B) is high, the small coefficient A_3/A_1 will markedly lower its impact in the two-tone test. More emphasis should be put on the symmetry of C. Nevertheless, even $C > A_3$, its effect can be neglected, providing $C \ll A_1$. This observation makes the design constraint of the mixer much more relaxed–relative high LO leakage and some asymmetry in the output waveform are acceptable.

V. Experiment Results

The proposed two-tone signal generator is fabricated in 130-nm standard CMOS technology. The chip die micrograph is shown in Fig. 16, and the percentage of each block's area is also compared. The total silicon area is 0.056 mm^2. From a 1.5-V power supply, the current mirror array draws around 2 mA, while the mixer consumes a maximum 2 mA at the LO frequency of 1 GHz. The other circuits are working under a 1.2-V supply. Moreover, the differential output impedance is set to 400 Ω (200 Ω for each R_L). A balun with an 8:1 impedance ratio is used to bridge the synthesizer and the spectrum analyzer.

Measurement results are shown in Fig. 17. Fig. 17(a) illustrates that an IM3 of -85.4 dBc is achieved at a relative low LO frequency (f_{LO}=4.8 MHz), and $CLK_{LF}(24f_0)$ is set to 2.4 MHz. The measured IM3 rises to -51.4 dBc when f_{LO} is increased to 1 GHz, as demonstrated in Fig. 17(b). Note that a high LO leakage tone appears at f_{LO}, and the even-order distortion at $f_{LO} \pm 2f_0$ also emerge. For (11), we have $B = -33.9$ dBc, $C = -44$ dBc, and $A_3/A_1 = -51.4$ dBc, yielding $\epsilon' \approx \epsilon + (3/4)(k_3/k_1)A_1^2 \times 0.09\%$. Therefore, even in the worst case, the LO leakage and $f_{LO} \pm 2f_0$ distortion has limited impact on the IM3 measurement. Fig. 17(c) shows the change of measured IM3 in the f_{LO} range from 48 to 1008 MHz with a fixed $f_0 = 1$ MHz. Better than -68 dBc IM3 can be achieved when $f_{LO} < 480$ MHz. The results for f_{LO} range from 2.4 to 153.6 MHz are further shown in Fig. 17(d), in which the IM3 values with different values

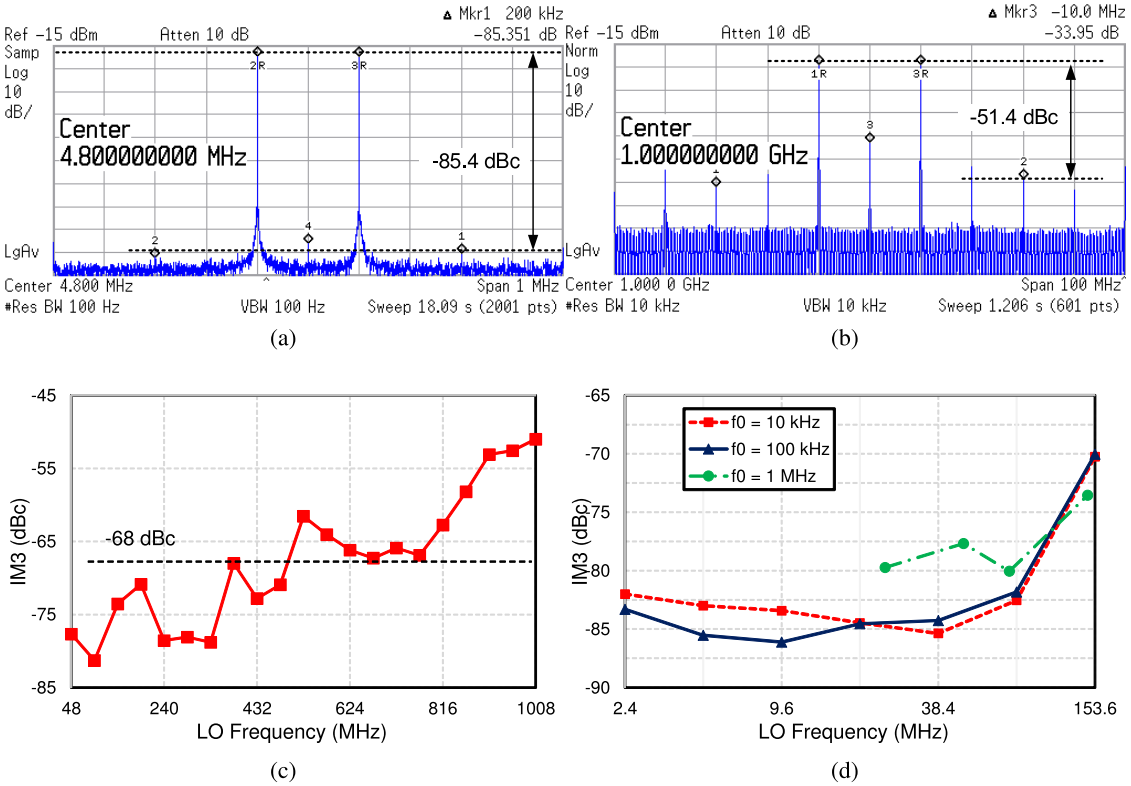


Fig. 17. Measurement results. (a) IM3 ($f_{LO} = 4.8$ MHz and $f_0 = 100$ kHz). (b) IM3 ($f_{LO} = 1$ GHz and $f_0 = 10$ MHz). (c) IM3, where f_{LO} is swept from 48 to 1008 MHz ($f_0 = 1$ MHz). (d) IM3, where f_{LO} is swept from 2.4 to 153.6 MHz (10 kHz, 100 kHz, and 1 MHz f_0).

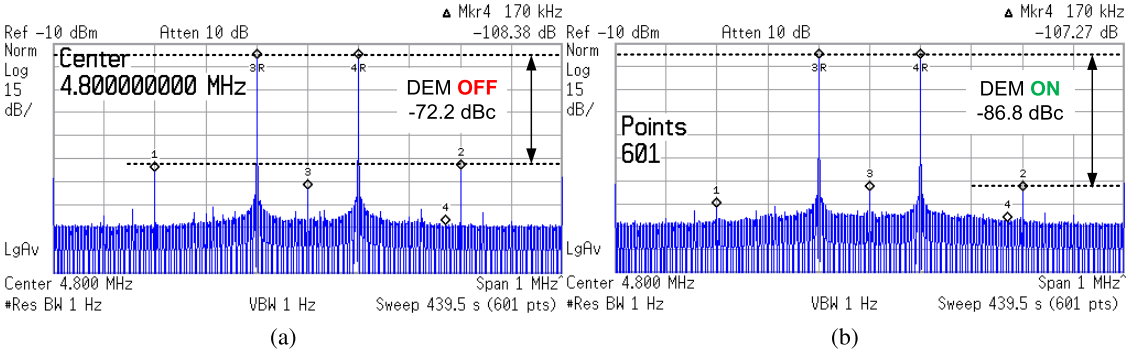


Fig. 18. Measured PSD and IM3 of the two-tone signals ($f_{LO} = 4.8$ MHz, $f_0 = 100$ kHz) (a) without DEM and (b) with DEM.

of f_0 are also compared. The measured IM3 is < -75 dBc within 76.8 MHz f_{LO}, and IM3 < -80 dBc can further be obtained with $f_0 \leq 100$ kHz. These results are close to the simulation results in Figs. 10 and 14. Moreover, it can be concluded that the "baseband" single tone generator has around -85 dBc IM3 limit, which dominates the linearity for $f_{LO} < 100$ MHz. Above 100 MHz, the passive mixer becomes the major contributor of the linearity degradation. Additionally, the balance between the two-tone amplitudes exhibits < 0.1 dB difference across the whole frequency range.

Section IV-A concludes that the DEM technique can provide a further improvement of linearity when the current mismatch becomes the dominant error source. Fig. 18(b) shows that the IM3 improves almost 14 dB when the DEM is ON, compared to the results in Fig. 18(a) with the DEM turned OFF. Around the IM3 tones, the measured noise floor is about -108 dBc without DEM and it raises 1 dB after the DEM is turned ON. We can conclude that the proposed DEM technique achieves low induced noise, which is consistent with Fig. 12(b). Fig. 19 further demonstrates the measured IM3 improvement (for $f_0 = 100$ kHz and $f_0 = 1$ MHz) after turning on the DEM. As expected, the linearity improvement is significant when the current mismatch becomes the dominant error source. While at high LO frequency, the mixer distortion becomes dominant; and thus the DEM is not as effective as working at low LO frequency.

Table II compares the performance of the proposed synthesizer to the other state-of-the-art works. The reported IM3 upper limits and the corresponding frequency ranges are especially significant. Single-tone sinusoidal synthesizers are

TABLE II
COMPARISON OF TWO-/SINGLE-TONE GENERATION PERFORMANCE

Ref.	**This work**	[7] [1]	[8]	[9]	[11]	[10]	[25]	[16] [3]	[17] [3]
Max Freq.	**1 GHz**	N.A.	250 MHz	800 MHz /1.4 GHz	1 GHz	5.26 GHz	1.062 GHz	11 MHz	850 MHz
Area (mm^2)	**0.056**	N.A.	0.034	0.016	3.3 [2]	1.6 [2]	0.23	0.186	0.08
Process (nm)	**130**	65	180	40	65	65	250	130	180
Supply (V)	**1.2/1.5**	N.A.	1.8	1.2	1.0/2.5	1.2/3.3	2.5	1.2	1.8
IM3/ HD3 (dBc)	**-66 @ 720 MHz -68 @ 480 MHz -70 @ 336 MHz -80 @ 20 MHz**	-75	-62.16 @ 246 MHz	-61.5 @ 1.36 GHz[4] -70 @ 800 MHz -75 @ 20 MHz	-80 @ 950 MHz -85 @ 300 MHz	-62 @ 4.1 GHz -82 @ 1.9 GHz	-64.7 @ 1.0 GHz	-72 @ 10 MHz	-70 @ 750 MHz
I_{load} (mA)	**2**	N.A.	10	16	16	20	5.1	N.A.	N.A.
R_L (Ω)	**400**	50	50	50	50	50	100	N.A.	N.A.
P_{total} (mW)	**6**	N.A.	24	40	681	380	122	3.34	57
Type	**Mixing-FIR**	Dual-VCO	DAC	DAC	DAC	Mixing-DAC	Mixing-DAC	HC	HC(FIR)
FoM_{BIST} ($\times 10^4$)	**8.70**	N.A.	1.30	0.41	0.018	0.12	0.38	N.A.	N.A.

[1] Simulation result; [2] Area of digital circuits are included; [3] Single-tone generation HD3 for reference;
[4] IM3 is measured @ 2.8 GS/s, the others are measured @ 1.6 GS/s.

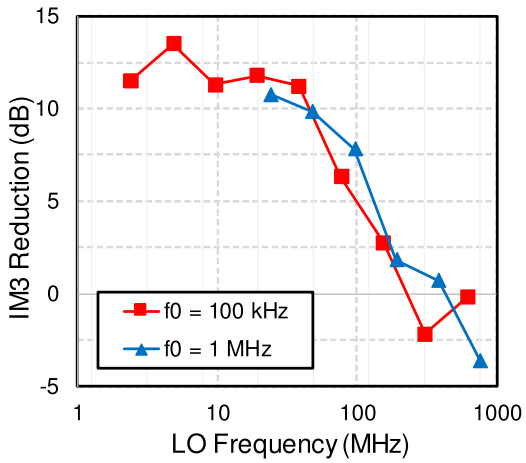


Fig. 19. Measured IM3 improvement by turning on DEM.

also used as references. Furthermore, to evaluate whether the signal generator is suitable for on-chip BIST application, the FoM in [17] can be modified to

$$\mathrm{FoM_{BIST}} = \frac{f_{\mathrm{LO}}(\mathrm{MHz}) \times 2^{\frac{-\mathrm{IM3(dB)}}{6}}}{P_{\mathrm{total}}(\mathrm{mW}) \times \frac{A(\mathrm{mm}^2)}{L_{\mathrm{ch}}^2(\mu\mathrm{m}^2)}} \tag{12}$$

where f_{LO} and IM3 are the characteristic LO frequency and the corresponding reported IM3. L_{ch} is the process node in μm. To sum up, the proposed calibration-free synthesizer architecture shows comparable linearity performance to the other state-of-the-art works but has smaller hardware overhead. It is suitable for on-chip linearity BIST applications.

VI. CONCLUSION

A sine-wave synthesizer is proposed to generate two low-distortion sinusoidal signals for on-chip linearity BIST. It is driven by only square-wave digital clocks and can cover a wide frequency range up to 1 GHz. A cascade FIR architecture with three five-taps and one three-tap current-steering FIR blocks are used in the "baseband" single tone generator to suppress the third-order component, which has the most significant impact on the precision of the IM3 two-tone test. Due to the low frequency "baseband" clock, phase error in the clock distribution network can be minimized. The DEM technique is further implemented to improve matching among current branches in the current mirror array, which implements the FIR tap coefficients. Thus, strong cancellation of the third-order harmonic can be achieved without calibration for the single tone. The generated single tone is then up-converted by a passive mixer using a high speed clock at the LO frequency. The up-converting produces two sinusoidal tones and the mirroring mechanism guarantees balance between the amplitudes of these two tones. Moreover, the compact synthesizer design, which has only logic gates, MOS switches, and current mirror array, is scalable for future advanced IC processes. This approach is one step toward the BIST and *in situ* optimization for integrated circuit design.

ACKNOWLEDGMENT

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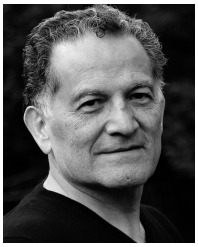

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