

On the Design of Wideband Transformer-Based Fourth Order Matching Networks for *E*-Band Receivers in 28-nm CMOS

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Abstract—This paper discusses the design of on-chip transformer-based fourth order filters, suitable for mm-Wave highly sensitive broadband low-noise amplifiers (LNAs) and receivers (RXs) implemented in deep-scaled CMOS. Second order effects due to layout parasitics are analyzed and new design techniques are introduced to further enhance the gain-bandwidth product of this class of filters. The design and measurements of a broadband 28-nm bulk CMOS LNA and a sliding-IF RX tailored for *E*-band (i.e., 71–76-GHz and 81–86-GHz) point-to-point communication links are presented. Leveraging the proposed design methodologies, the *E*-band LNA achieves a figure of merit ≈ 10.5 -dB better than state-of-the-art designs in the same band and comparable to LNAs at lower frequencies. The RX achieves 30.8-dB conversion gain with <1-dB in-band ripple over a 27.5-GHz BW_{−3-dB} while demonstrating a 7.3-dB minimum NF with less than 2-dB variation from 61.4 to 88.9-GHz. The worst cases in-band ICP_{1-dB} and IIP₃ are −30.7 and −23.8-dBm, respectively, from a 0.9-V power supply. This wideband state-of-the-art performance enables robust and low power multi-Gb/s wireless communication over short to medium distance over the complete *E*-band with wide margin.

Index Terms—Broadband, CMOS, coupled resonators, *E*-band, gain-bandwidth (GBW) product, low-noise amplifier (LNA), millimeter-wave, receiver (RX), transformer, wideband.

I. INTRODUCTION

5TH generation mobile networks will deal with data-rate 100× higher than today [1], posing unprecedented challenges on the wireless infrastructure. The Federal Communications Commission in the U.S. and the European Conference of Postal and Telecommunications Administrations in Europe have recently allocated the 71–76-GHz and the 81–86-GHz bands (known as *E*-band) to enable multi-Gb/s wireless point-to-point back-haul links for low-cost fiber extension or replacement over short to medium distance [2], motivating an increasing research interest in the last few years [3]–[5]. *E*-band wireless links would benefit from a high performance transceiver solution in deep-scaled CMOS technology, since limiting the number of monolithic microwave integrated circuit modules would immediately result in lower

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costs while ensuring higher yield. However, to realize the full potential of such links, a wideband receiver (RX) with high sensitivity and uniform performance over two bands from 71 to 76-GHz and 81 to 86-GHz (i.e., >15-GHz) is needed, which is still an open challenge. The study in [6] shows that an *E*-band transceiver with a 20-dBm output power transmitter and a RX with 10-dB maximum noise figure (NF) would allow a 25 Gb/s maximum theoretical data-rate over 1 km distance using 64-QAM, with 99.9% weather availability in most of the U.S. and Europe. Requirements are even more stringent when the spread due to process variations and modeling inaccuracy is considered. Recently, two separate narrowband SiGe BiCMOS RXs targeting either the low or the high band have been reported in [3], while a narrowband CMOS solution for 79-GHz car radar has been demonstrated in [7]. However, these RXs do not meet the requirements in terms of bandwidth. To the best of the authors' knowledge, a single chip CMOS broadband solution has not been reported in literature so far.

Research efforts in the 60-GHz frequency band have shown the potential of fourth order filters to realize gain-bandwidth enhancement (GBWEN) when compared to classical narrowband solutions, without compromising the already stringent design tradeoffs due to the high frequency of operation [8]–[11]. This paper elaborates further on these techniques with a strong focus on practical on-chip realization in deep-scaled CMOS for *E*-band applications. Second order effects due to the physical layout implementation often neglected in prior works, are deeply investigated. New insight is shed on these kinds of filters, leading to new design techniques to further approach the Bode–Fano limit and significantly advance the state of the art.

The design and measurements of a broadband low-noise amplifier (LNA) [12] and a fully integrated sliding-IF RX tailored for *E*-band point-to-point communication links are discussed. To compare designs at different frequencies, the following figure of merit is used [13] in Fig. 1

$$\text{FOM} = 20 \log_{10} \left(\frac{\text{Gain}_{\text{lin}} \cdot \text{BW}_{\text{GHz}}}{P_{\text{dc[mW]}} \cdot (\text{NF}_{\text{lin}} - 1)} \right). \quad (1)$$

The RX adopts a sliding-IF architecture (see Fig. 2), allowing to relax the requirements on the local oscillator generation and distribution network, i.e., 2/3 lower center frequency and tuning range, with no need for distributing quadrature outputs at the carrier frequency. However, an additional broadband IF stage is required. This RX employs a transformer-based

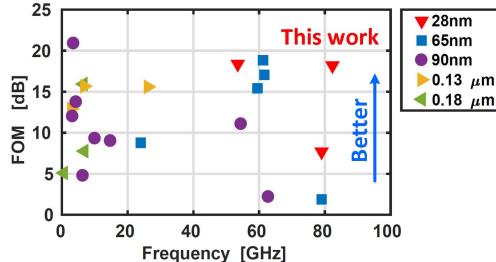


Fig. 1. Comparison of recently published state-of-the-art CMOS LNAs.

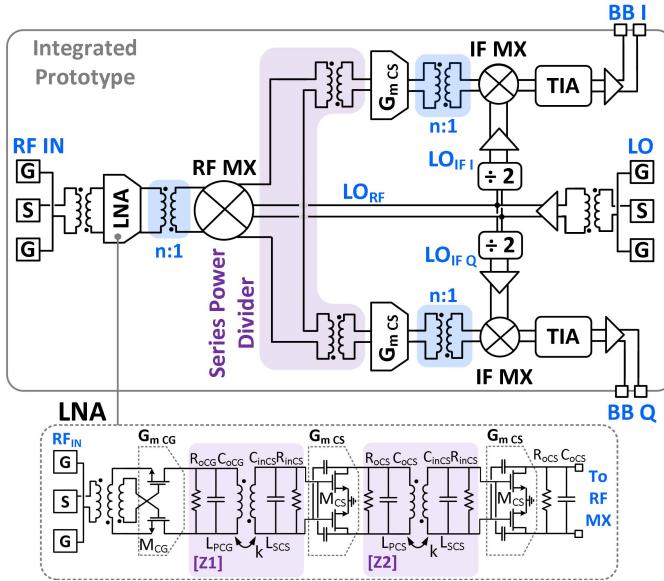


Fig. 2. Block diagram of the integrated RX.

series power divider derived from a fourth order two-port filter to realize >9-GHz (>36%) IF bandwidth.

This paper is organized as follows. Section II gives an overview of prior art, focusing on GBWEN techniques suitable for mm-Wave applications. Section III discusses second order effect of on-chip layout parasitics and their impact on the filter transimpedance. Section IV is dedicated to the design of proposed RX focusing on the key building blocks. Section V presents the measured results. Finally, Section VI draws the conclusion.

II. OVERVIEW OF PRIOR ART

A CMOS amplifier can be modeled as an ideal transconductance G_m with a parallel RC input and output impedance, R_{in}/C_{in} and R_o/C_o , respectively (as in Fig. 2). To achieve the required gain, noise, and input match and/or output power specifications, filters are needed to resonate the parallel capacitance and realize impedance transformation over the required bandwidth. In this sense, LNAs, power amplifiers, on-chip gain stages, and buffers share, to some extent, similar design challenges and solutions. The Bode–Fano criterion states that when an ideal two-port passive lossless filter is terminated on a parallel RC load: 1) it is possible to resonate out perfectly the capacitance C only at a finite number of frequencies and 2) for a given practical filter realization, a broader passband bandwidth can be achieved only at expenses of larger ripple [14], [15]. It is worth noticing that

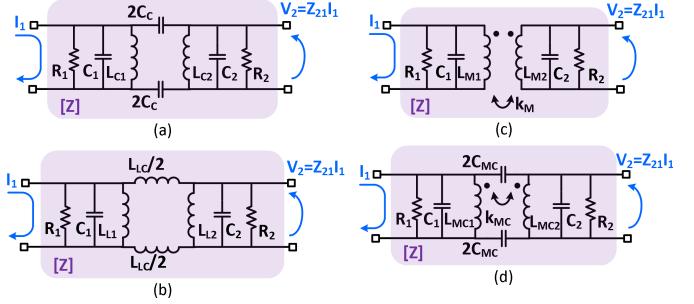


Fig. 3. Recently proposed fourth order two-port filters for GBWEN. (a) Capacitively coupled resonators. (b) Inductively coupled resonators. (c) Magnetically coupled resonators. (d) Magnetically and capacitively coupled resonators.

for a given finger length and technology, the RC product of the input and output impedance of a transistor is almost independent of its width [16], making this result extremely general.

The frequency response of an ideal bandpass filter can only be approximated in reality. A close practical approximation is the Chebyshev filter [15]. However, high order filters demand a large number of passive components that due to technology limitations result in higher losses at mm-Wave. Therefore, the effectiveness of such techniques has been demonstrated so far only in the low GHz range [14], [16], [17]. At mm-Wave frequencies, fourth order coupled resonators offer GBWEN when compared to the simple RLC tank, without compromising the network loss [8]–[12], [18]. Therefore, the focus of this paper is on this latter category of filters.

Fig. 3 shows different implementations of a fourth order two-port filter. In [8], capacitively coupled resonators are proposed [Fig. 3(a)]. Inductively coupled resonators [Fig. 3(b)] are proposed in [9] and [10]. Magnetically coupled resonators [Fig. 3(c)] are adopted in [12]. While [11] proposes magnetically and capacitively coupled resonators [Fig. 3(d)]. The key concept behind these circuits is to couple two RLC tanks by means of C_c in [Fig. 3(a)], L_c in [Fig. 3(b)], k_M in [Fig. 3(c)], and C_{MC} and k_{MC} in [Fig. 3(d)]. All of these networks show two pairs of complex poles ω_L and ω_H . The larger the coupling strength, the wider the bandwidth and higher the in-band ripple.

The derivation of the close form expressions of the filter transimpedance can be found in [8]–[11] and is not repeated hereafter. When $C_1 = C_2 = C$ and under the assumption of high quality factor, ω_L and ω_H can be expressed as

$$\begin{aligned}\omega_L &= \frac{1}{\sqrt{L_C(C+2C_C)}} = \frac{1}{\sqrt{L_L C}} = \frac{1}{\sqrt{L_M(1+|k_M|)C}} \\ &= \frac{1}{\sqrt{L_{MC}(C+2C_{MC})(1-k_{MC})}} \Big|_{k_{MC}<0} \end{aligned}\quad (2)$$

$$\begin{aligned}\omega_H &= \frac{1}{\sqrt{L_C C}} = \frac{1}{\sqrt{\frac{L_L L_C}{2L_L + L_C} C}} = \frac{1}{\sqrt{L_M(1-|k_M|)C}} \\ &= \frac{1}{\sqrt{L_{MC}(1+k_{MC})C}} \Big|_{k_{MC}<0} \end{aligned}\quad (3)$$

where L_C , L_L , L_M , and L_{MC} are the inductors of the two coupled RLC tanks in the case of capacitively, inductively,

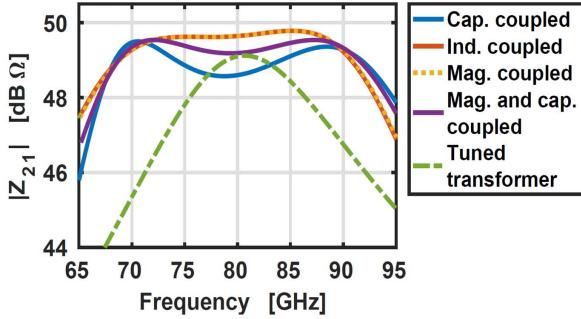


Fig. 4. Comparison of the transimpedance frequency response of different fourth order filters.

magnetically, and both magnetically and capacitively coupled resonators, respectively (as shown in Fig. 3). We now wish to determine which one of these circuits get closer to the Bode–Fano limit. We therefore focus on the following design example. First, assume $R_1 = R_o = 400 \Omega$, $R_2 = R_{in} = 1 \text{ k}\Omega$, and $C = C_1 = C_o = C_2 = C_{in} = 14 \text{ fF}$, typical values for the input and output impedances of a G_m stage of an LNA implemented in 28-nm bulk CMOS. The filters shown in Fig. 3 are all designed to achieve roughly the same >30% fractional bandwidth around the center frequency $f_o = 80\text{-GHz}$, resulting in >24-GHz $BW_{-3\text{-dB}}$. By imposing $\omega_L = 2\pi 68\text{-GHz}$ and $\omega_H = 2\pi 92\text{-GHz}$ in (2) and (3) the values of the circuit components in Fig. 3 are derived. The filter based on magnetically and capacitively coupled resonators [Fig. 3(d)] can be designed to equalize the magnitude of the filter transimpedance at the two maxima by further imposing the conditions $k_{MC} < 0$ and $C_{MC} = -C k_{MC}/(1 + k_{MC})$ as proposed in [11].

The transimpedance of the designed filters is shown in Fig. 4 together with the $|Z_{21}|$ of a classical tuned transformer with $k = 0.8$ for comparison. Clearly, fourth order filters show a GBWEN when compared to a simple RLC tank or a tuned transformer. When the latter is considered, the only way to achieve a larger bandwidth is to lower the quality factor of the load by adding an equivalent parallel resistor and increasing the insertion loss of the filter.

Inductively coupled and magnetically coupled resonators stand out for the lowest ripple for a given bandwidth (Fig. 4). In this design example, these types of filters realize a $\text{GBWEN} \approx 1.67$ when compared to the classical tuned transformer, that reaches $\text{GBWEN} \approx 3.1$ if 3-dB in-band ripple is allowed [10]. Capacitively coupled resonators are the furthest from the Bode–Fano limit. Perhaps not surprisingly, filters based on both capacitive and magnetic coupling achieve performance in between the two. This can be intuitively understood as follows. The quality factor of a filter is proportional to the RC product of the load and the higher the Q the larger the ripple. It is therefore not desirable to add capacitance to the network. Moreover, on-chip capacitors at mm-Wave suffer from a reduced quality factor that degrades every technology node [19].

It is worth noticing that in a practical on-chip implementation, a transformer allows a substantial area reduction, easier dc feed, and ac coupling when compared to inductively

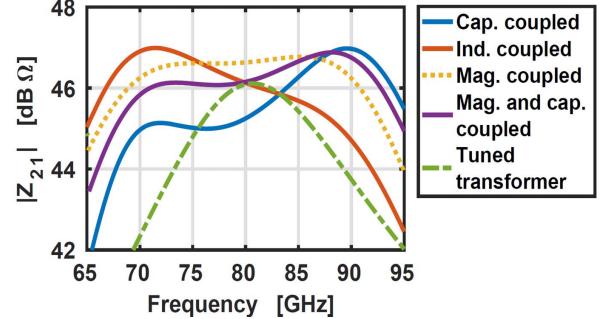


Fig. 5. Effect of unbalanced capacitive terminations (i.e., $C_1 \neq C_2$) on the transimpedance frequency response of different fourth order filters.

coupled resonators. Moreover, the magnetic field is better constrained in a transformer, making the coupling easier to control and model, and limiting the impact of dummies in the final layout [20], [21]. Transformer-based filters are therefore preferred in this paper.

So far, we have compared several previously proposed GBWEN techniques suitable for mm-Wave amplifiers from a theoretical point of view, neglecting second order effects. However, we will show in the following section that those effects are not negligible at all when a practical design in deep-scaled CMOS is considered. By investigating more deeply transformer-based fourth order filters, new design techniques are introduced. Leveraging these insights, a wideband LNA and a sliding-IF RX for E-band applications with large bandwidth, low in-band ripple, and high sensitivity are designed in 28-nm bulk CMOS without penalty terms of power consumption.

III. SECOND ORDER EFFECTS DUE TO PHYSICAL REALIZATION

A. Effect of Unbalanced Capacitive Terminations

The expressions of ω_L and ω_H have been derived assuming $C_1 = C_2 = C$. In general, this is not the case and it is interesting to see how the different filters previously introduced respond to this effect. Following the same approach outlined in [8]–[11] and carrying out the algebra, the frequency of the complex poles when $C_2 = n C_1$ can be derived as

$$\omega_L = \frac{1}{\sqrt{L_{C1}(C_1 + C_C(1 + 1/n))}} = \frac{1}{\sqrt{L_{L1}C_1}} = \frac{1}{\sqrt{L_{L2}C_2}} \quad (4)$$

$$\omega_H = \frac{1}{\sqrt{L_{M1}(1 + |k_M|)C_1}} = \frac{1}{\sqrt{L_{M2}(1 + |k_M|)C_2}} \quad (5)$$

$$\begin{aligned} \omega_L &= \frac{1}{\sqrt{L_{C1}C_1}} = \frac{1}{\sqrt{L_{C2}C_2}} = \frac{1}{\sqrt{\frac{L_{L1}L_{LC}}{L_{L1}(1+1/n)+L_{LC}}C_1}} \\ \omega_H &= \frac{1}{\sqrt{L_{M1}(1 - |k_M|)C_1}} = \frac{1}{\sqrt{L_{M2}(1 - |k_M|)C_2}}. \end{aligned} \quad (5)$$

Unfortunately, the closed form expressions for the filter in Fig. 3(d) do not lead to simple design guidelines or insight, and therefore have been omitted.

Fig. 5 shows the effect of $n = 2$ on the frequency response of the filters. This is a typical value for the inter-stage matching network of a power amplifier, where the driver is downsized

TABLE I
COMPONENT VALUES USED IN THE DESIGN EXAMPLE SHOWN IN FIG. 6(b)

$R_1 [\Omega]$	$C_1 [fF]$	$R_2 [\Omega]$	$C_2 [fF]$	$L_{M1} [pH]$	$L_{M2} [pH]$	k_M	$L_{MC1} [pH]$	$L_{MC2} [pH]$	k_{MC}	$C_{MC} [fF]$
400	14	1000	14	353.7	279.4	-0.362	177.3	177.3	-0.195	2.28

by a factor of 2, and a somewhat extreme case for an LNA were normally the size of the amplifiers in the chain is not increased to save power [8], [10]. $\omega_L = 2\pi$ 68-GHz and $\omega_H = 2\pi$ 92-GHz are imposed in (4) and (5) and the quality factor of the load is kept constant (e.g., $R_2 = 1 \text{ k}\Omega/2$) for fair comparison. Interestingly, the frequency response of both the magnetically coupled resonators and the single tuned transformer are not effected, except for a $10 \log_{10}(n)$ reduction in transimpedance gain. This is not the case for all the other fourth order filters. Capacitively and inductively coupled resonators show a balanced response if and only if $C_1 = C_2$. To solve this issue, in [10] a four-step design procedure that starts from inductively coupled resonators, applies Norton transformation, which finally derives a transformer-based filter is proposed. The end result is the same design parameters derived here in a single step form (4) and (5). Finally, the filter based on both magnetically and capacitively coupled resonators shows a frequency response in between the two, and, most importantly, the condition $C_{MC} = -C k_{MC}/(1 + k_{MC})$ does not result in an equalized frequency response any more.

This design example clearly shows the robustness of the proposed design techniques. Moreover, new insight is shed on these pervasive kinds of filters and simple design equations are derived.

B. Frequency Response Equalization

When inductors with a limited Q -factor are considered, the frequency response of the filter shows amplitude imbalance at the two resonant peaks [10], [11], [22]. To restore a flat frequency response without adding components or change the capacitive load, the filter in Fig. 3(c) can be redesigned by unbalancing the values of L_{M1} and L_{M2} . First, let us define the design parameter (adopting the notation in [23])

$$\xi = \frac{L_{M2}C_2}{L_{M1}C_1}. \quad (6)$$

When $\xi \neq 1$, the analysis of the filter response gets much more involved and the two pairs of complex poles can be written as [23], [24]

$$\omega_{L,H}^2 = \frac{1 + \xi \pm \sqrt{(1 + \xi)^2 - 4\xi(1 - k_M^2)}}{2L_{M2}C_2(1 - k_M^2)}. \quad (7)$$

As it will be shown shortly, the design parameter ξ can be leveraged to achieve pre-emphasis. For a given value of ξ , the magnetic coupling coefficient sets the ratio ω_H/ω_L . When $\xi = 1$, (7) simplifies to (2) and (3).

However, at mm-Wave frequencies the quality factor of inductors is relatively high [19], [20], therefore the required pre-emphasis needed is limited. This means that ξ close to 1 is sufficient to equalize the frequency response and (2) and (3)

are still very good approximations of ω_L and ω_H . Hence, the transformer can be designed with

$$|k_M| = \frac{\omega_H^2 - \omega_L^2}{\omega_H^2 + \omega_L^2} \quad (8)$$

$$L_{M1} = \frac{1}{\omega_L^2 C_1 (1 + |k_M|) \sqrt{\xi}} \quad (9)$$

$$L_{M2} = \frac{\sqrt{\xi}}{\omega_L^2 C_2 (1 + |k_M|)}. \quad (10)$$

The effect of ξ on the frequency response is shown in Fig. 6(a). The remarkably simple expressions shown in (9) and (10) shed new insights into the relation of the transformer design parameters and the filter response.

It is worth noticing at this point that it is possible to equalize the filter response by also adopting other design techniques. In [11] and [22], a coupling capacitor is added, resulting in the circuit in Fig. 3(d). Nonetheless: 1) capacitor losses are relatively high at mm-Wave and 2) adding capacitance to the network will result in larger ripple for the same bandpass bandwidth. Therefore, this approach is not preferable at mm-Wave. To further prove this point, the latter frequency equalization technique is compared against the proposed one in Fig. 6(b). A pessimistic value of 10 is assumed for the quality factor of the inductors at 80-GHz. The losses are modeled with a series resistor. The lower Q -factor of the network results in lower transimpedance gain while it enables to design the filter with a larger bandpass bandwidth for the same ripple. The two filters are redesigned to achieve the same $\text{BW}_{-3\text{-dB}}$ and the components values are listed in Table I. As expected, adding a coupling capacitor C_{MC} results in higher in-band ripple for the same bandwidth. Moreover, when a finite quality factor $Q_{C_{MC}} = 10$ is considered, the condition $C_{MC} = -C k_{MC}/(1 + k_{MC})$ is not sufficient to restore a flat frequency response.

Another design procedure that starts from inductively coupled resonators [Fig. 3(b)] is proposed in [10]. It is worth noticing that the filter in Fig. 3(b) cannot provide pre-emphasis without changing the capacitive terminations, which is not desirable. Therefore, in [10], four design parameters are introduced (i.e., d , m , l , and n in [10]) and several design steps are outlined to synthesize the final transformer-based matching network without acting on the values of C_1 and C_2 . When compared to the study presented here, the excellent work published in [10] lacks of simplicity and does not lead to an intuitive understanding of effect of the transformer design parameters (k_M , L_{M1} , and L_{M2}) on the frequency response of the filter.

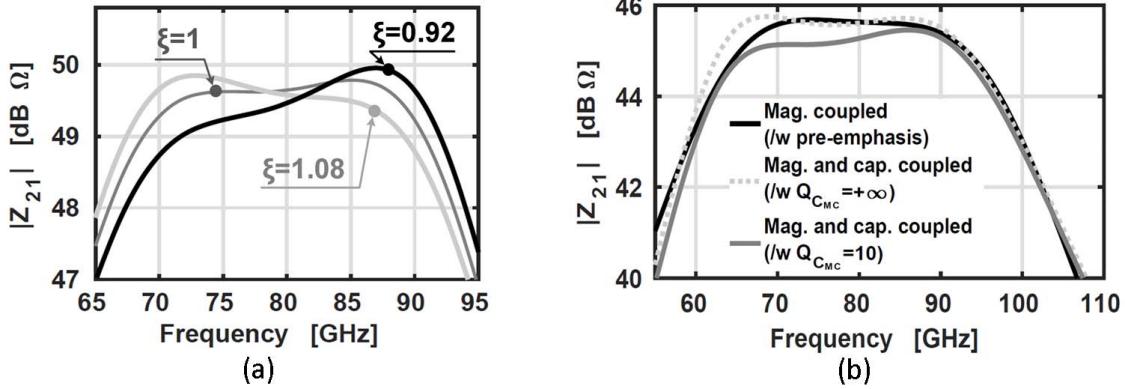


Fig. 6. (a) Effect of ξ on the filter transimpedance frequency response. (b) Comparison between different frequency equalization techniques when a limited $Q_{\text{ind}} = 10$ is considered.

C. On the Parasitic Inter-Winding Capacitance

Fig. 7 shows the layout of typical inverting and non-inverting transformers and their equivalent lumped element models [25]. Highlighted in gray in Fig. 7(c) are the parasitics to the silicon substrate C_{ox} , C_{Si} , and r_{Si} , the parasitic intra-winding capacitance C_{m1} , C_{m2} , and the inter-winding capacitance C_C . To get more insight, it is instructive to focus on the simplified differential mode (DM) model in Fig. 7(d). The parasitics to the substrate and the intra-winding capacitance are modeled as an equivalent parallel RC network, and are absorbed in the filter terminations. To further simplify the analysis and get insight into the effect of the parasitic inter-winding capacitance C_C , in the following R_{S1} and R_{S2} are neglected.

Intuitively, we expect that if there is no voltage drop across the parasitic inter-winding capacitance ($V_{Cc} = 0$), no current is flowing through it and C_C has no effect on the filter frequency response. By the same token, when V_{Cc} is maximum, the effect of C_C is also maximize. Moreover, for a given C_C and V_{Cc} , the higher the frequency, the larger the current I_{Cc} will be [see Fig. 7(d)]. The voltage across C_C can be written as

$$\begin{aligned} V_{Cc} &= V_1 - V_2 = I_1(Z_{11} - Z_{21}) \\ &= I_1(|Z_{11}|e^{j\angle Z_{11}} - |Z_{21}|e^{j\angle Z_{21}}) \\ &= I_1|Z_{21}|e^{j\angle Z_{21}} \left(\frac{|Z_{11}|}{|Z_{21}|} e^{j(\angle Z_{11} - \angle Z_{21})} - 1 \right). \quad (11) \end{aligned}$$

Equation (11) shows that regardless the magnitude of Z_{11} and Z_{21} , the voltage drop across C_C is maximum when $\angle Z_{11} - \angle Z_{21} = \pm 180^\circ$ and minimum when $\angle Z_{11} - \angle Z_{21} = 0^\circ$.

This insight is key to understand the effect of C_C on the filter response. To further investigate this parasitic effect, let us go back to the previous design example and assume a parasitic inter-winding capacitance $C_C = 1 \text{ fF}$. This value is reasonable for a $f_o \approx 80\text{-GHz}$ center frequency when relatively low- k transformers are used, and it is optimistic when high- k transformers are designed (as it is the case for a classical tuned transformer). When C_C is neglected, the sign of the magnetic coupling coefficient k has no effect on the magnitude of the transimpedance of the filter. The $\text{BW}_{-3\text{-dB}} \approx 31.3\text{-GHz}$ with $\approx 0.16\text{-dB}$ in-band ripple. However, when the parasitic

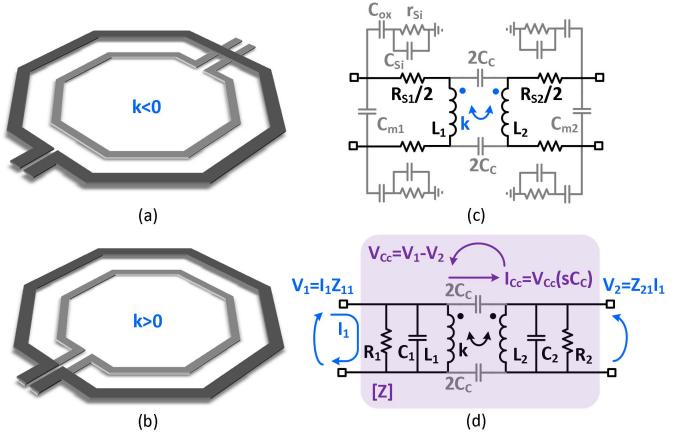


Fig. 7. Physical layout implementation of (a) inverting and (b) non-inverting transformer. (c) Lumped element broadband transformer model. (d) Simplified circuit in DM.

inter-winding capacitance is considered, inverting and non-inverting transformers behave very differently. This is clearly shown in Fig. 8. An inverting transformer ($k < 0$) realizes $\angle Z_{11} - \angle Z_{21}$ that goes from $\approx -150^\circ$ in the proximity of the low frequency pole f_L to $\approx -10^\circ$ in the proximity of the high frequency pole f_H . The resulting effect is that C_C lowers f_L while keeping f_H unchanged, realizing a wider bandwidth ($\text{BW}_{-3\text{-dB}} \approx 37.3\text{-GHz}$) with larger ripple ($\approx 0.67\text{-dB}$) as shown in Fig. 8(a). The contrary is happening when the same filter uses a non-inverting transformer ($k > 0$) [Fig. 8(b)]. In this second case, f_H is moved toward lower frequencies, resulting in $\approx 9\text{-GHz}$ lower bandwidth.

It is worth noticing that in a broadband design, when a transformer with $k < 0$ is adopted, to counteract the larger ripple introduced by C_C , a lower L_1 , L_2 , and k can be used. This results in a further reduction of the parasitic inter-winding capacitance. When a non-inverting transformer is used, however, to balance the reduced bandpass bandwidth caused by C_C a larger value of k is needed. This normally results in a further enhancement of the parasitic inter-winding capacitance. Therefore, it is desirable to use inverting transformers for this kind of networks whenever possible.

Finally, assuming $L_1 = L_2 = L$ (as in the example considered so far), the self-resonant frequency of the transformer

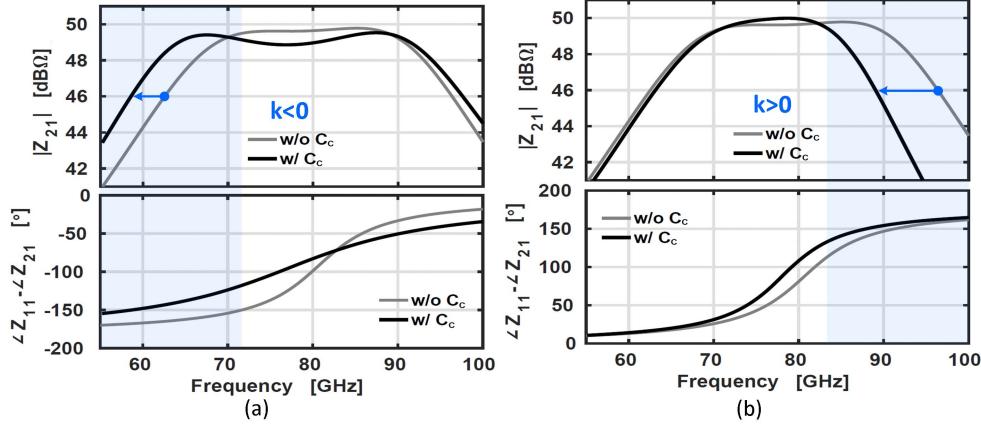


Fig. 8. Effect of the parasitic inter-winding capacitance on the frequency response of broadband fourth order filters implemented with (a) inverting and (b) non-inverting transformers.

can be derived as

$$f_{\text{SRF}} = \frac{1}{2\pi\sqrt{2L(1-k)C_C}}. \quad (12)$$

It is now possible to compare the self-resonant frequencies of an inverting ($f_{\text{SRF},k<0}$) and non-inverting transformer ($f_{\text{SRF},k>0}$) with the same L , C_C , and $|k|$

$$f_{\text{SRF},k<0} = \sqrt{\frac{(1-|k|)}{(1+|k|)}} f_{\text{SRF},k>0}. \quad (13)$$

Interestingly, $f_{\text{SRF},k<0}$ is always lower than $f_{\text{SRF},k>0}$. Therefore, when the f_{SRF} is adopted as a figure of merit to benchmark the upper frequency limit of a transformer, it may lead to the wrong conclusion that $k > 0$ is always preferable when circuits with high frequency of operation are designed.

D. On the Parasitic Magnetic Coupling in Multistage Amplifiers

Another aspect often neglected is the effect of the parasitic magnetic coupling in multistage amplifiers. To keep the silicon area occupation as small as possible, in practice, on-chip transformers are laid out physically close to each other. Therefore, some coupling is to be expected. We also expect that this effect will be exacerbated when several G_m stages are cascaded to achieve the required gain at mm-Wave.

To get insight it is instructive to refer to the schematic shown in Fig. 9. Here we assume to cascade three times the same transformer-based fourth order inter-stage matching network previously designed, and k_{p1} and k_{p2} are added. Fig. 10 shows the effect of different signs of k_{p1} and k_{p2} , when $|k_{p1}| = |k_{p2}| = 0.02$. As it will be shown later, this is a reasonable assumption when transformers are laid out close to each other to save silicon area. The ideal case $k_{p1} = k_{p2} = 0$ is also reported for comparison. Clearly, the effect of the parasitic magnetic coupling is not negligible. This implies the following.

- When a mm-Wave multistage amplifier is designed, it is important to include this effect in the electromagnetic (EM) simulations. When an extra stage is added, its matching network should be designed taking into account the effect of previous ones.

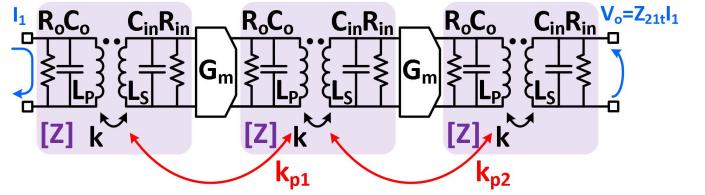


Fig. 9. Simplified multistage amplifier schematic with highlighted on-chip parasitic inter-stage coupling (k_{p1} , k_{p2}).

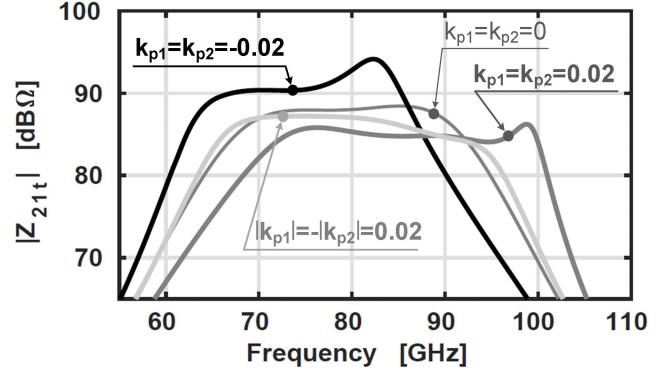


Fig. 10. Effect of k_{p1} and k_{p2} on the frequency response of the amplifier.

- Ground or floating shields may be added to further limit this effect [26].
- The signs of k_{p1} and k_{p2} could be designed to break through the bandwidth-ripple limitation of an ideally isolated fourth order filter [12].

To the best of the authors' knowledge, this is the first time that this effect has been recognized as a major issue in broadband multistage amplifiers and a simple design technique is proposed to take advantage of it.

IV. RECEIVER DESIGN

The previously discussed techniques were used to implement a wideband RX for E-band point-to-point communication in 28-nm bulk CMOS. In this section, the implementation details of the LNA, downconversion mixer, transformer-based power divider, baseband TIA, and dividers-by-2 to realize on-chip quadrature clock signals are given.

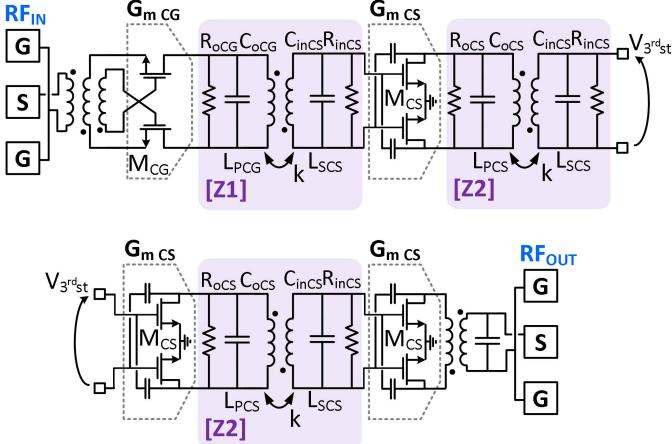
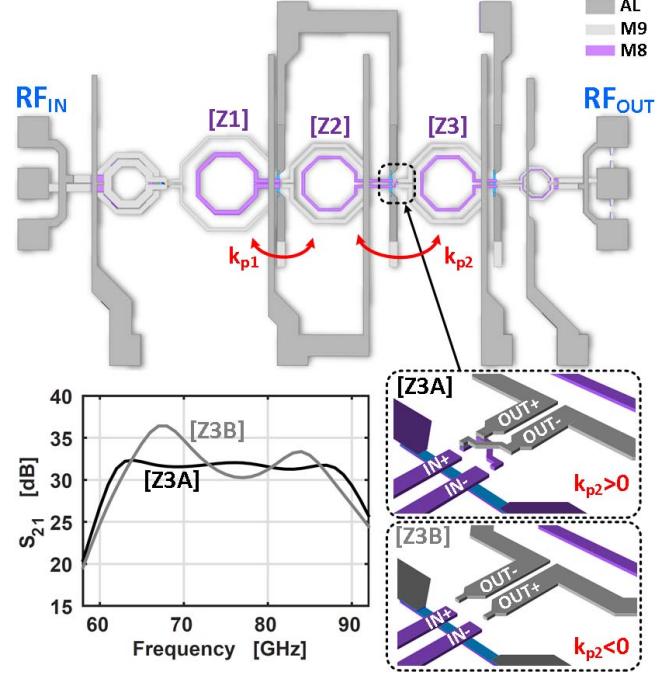


Fig. 11. Simplified schematic of the four-stage LNA test chip.

A. Low-Noise Amplifier

Fig. 2 shows the block diagram of the proposed sliding-IF RX. To limit the detrimental effect on the NF of the following blocks, the LNA employs three active stages to realize ≈ 25 -dB gain. A transformer at the input realizes the required single-ended to differential conversion while providing protection against ESD events. A G_m -boosted common gate amplifier realizes the required broadband input match to 50Ω [27]–[29]. The other transconductor stages are implemented with neutralized common source amplifiers for maximum gain and reverse isolation [20], [30]. fourth order inter-stage matching networks based on transformers are used to enhance the GBW product in the RF band. The transistors are biased with an inversion coefficient $IC \approx 1$ for maximum f_t , gm/I_{DS} product, resulting in an optimal design for speed and noise for a given power consumption [31], [32]. The minimum channel length is adopted to maximize f_t , while the width of the transconductors entails a tradeoff between NF, linearity, and power consumption [8]. $W_{CG} = 35.7 \mu\text{m}$ is set to provide the required input matching [27], [28]. The other transconductors are designed with $W_{CS} = 25.1 \mu\text{m}$ to save dc power. The transistor layout proposed in [20] is leveraged to minimize the parasitics due to the low level metals interconnects and maximize f_{MAX} . After layout parasitic extraction, the following values are derived $R_{oCG} = 472 \Omega$, $C_{oCG} = 12.1 \text{ fF}$, $R_{inCS} = 1.1 \text{ k}\Omega$, $C_{inCS} = 14.4 \text{ fF}$, $R_{oCS} = 415 \Omega$, and $C_{oCS} = 13.3 \text{ fF}$. The magnetic coupling coefficient sets the bandwidth of the filter. From (4), (5), and (8) the transformer design parameters are immediately derived. Inverting transformers are preferred as discussed in Section III.

To further prove the relevance of the on-chip parasitic magnetic coupling between transformers in multistage amplifiers, a stand-alone LNA test chip is designed (as shown in Fig. 11). The LNA is the same adopted in the RX chain with an extra stage added to drive directly the 50Ω measurement equipment. Fig. 12 shows the layout view of the realized prototype. The metal length and width are adopted as design variables to set the required inductance value, while magnetic coupling coefficient is set by the spacing between L_P and L_S (a larger distance results in a lower magnetic coupling).

Fig. 12. Simulated effect on the GBW of interconnections Z3A (black line) and Z3B (gray line) that realize different signs of k_{p2} .

From EM simulations, the values of the parasitic magnetic coupling coefficients are estimated as $|k_{p1}| \approx 0.032$ and $|k_{p2}| \approx 0.005$. The effect of different signs of k_{p1} and k_{p2} are shown in Fig. 12 (bottom), together with the resulting layout implementations. When the interconnection [Z3A] is adopted (i.e., $k_{p2} > 0$), simulations predict a GBW product above 1 THz with a ripple of 1.1-dB. Whereas, when the interconnection [Z3B] is used, k_{p2} is negative, resulting in a higher peak gain at the expenses of much larger in-band ripple. The GBW product in this second case drops below 0.5 THz with a ripple larger than 6-dB. To further probe the robustness of these design techniques, 2000 Monte Carlo simulations were performed under both process and mismatch variations. At 3σ the variation on the main design specifications are the following: ± 0.7 -dB gain, ± 1.7 -GHz BW_{−3-dB}, and ± 0.03 -dB NF.

B. RF Mixer and Power Splitter

The last stage of the LNA drives the RX mixer [implemented with a Gilbert-type switching quad, $(W/L)_{MX} = (25.1 \mu\text{m}/28\text{-nm})$] through a $n:1$ transformer, Fig. 2. This allows a separate dc biasing of the transconductor and the switching quad, yielding better linearity at low V_{DD} [9], [33]–[35]. Moreover, the $n : 1$ turns ratio reduces the voltage swing and realizes passive current gain at the secondary.

Fig. 13 shows two possible implementations of a transformer-based three-port power divider derived from a two-port fourth order filter. This transformation does not affect the frequency response, except for a 3-dB magnitude reduction due to ideal power division. Noteworthy, the series power divider results in 4 times less inductance at the primary winding while keeping a symmetrical bias network, leading

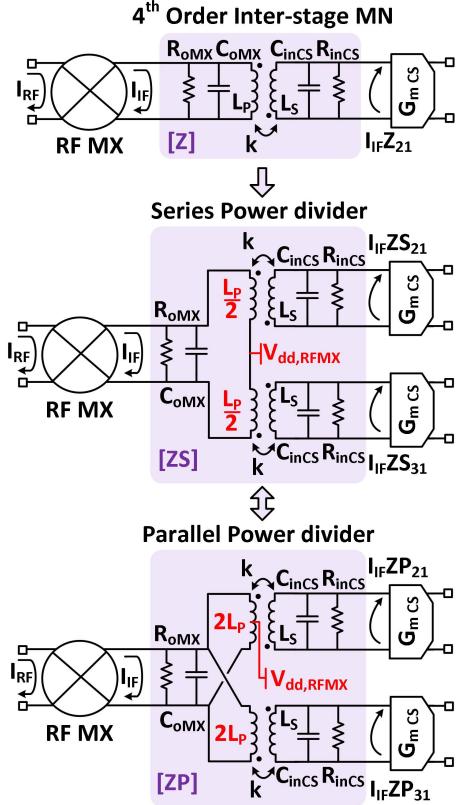


Fig. 13. Extension of broadband fourth order two-port networks based on transformers to realize three-port series or parallel power dividers.

to lower losses and better common mode rejection when compared with its parallel counterpart. Therefore, the former is preferred in this design.

EM simulations predict a Q -factor of ≈ 6 for a 2 nH on-chip inductor at 25-GHz , about $3\times$ lower than the Q of the inductors used in the LNA inter-stage matching networks at 80-GHz . As discussed in Section III, such a low Q impairs the magnitude of the filter transimpedance at the highest resonant frequency. Therefore, ξ in (9) and (10) is designed lower than 1 to realize the required pre-emphasis. In this paper, the power divider is designed to provide $>36\%$ IF fractional bandwidth, i.e., larger than the RF BW, and does not limit the BW of the full RX chain. Finally, it is worth noticing that the simple transformation to implement a power splitter shown in Fig. 13, would not be trivial if realized with a different fourth order network [see Fig. 3(a), (b), or (d)].

C. IF Mixer, Baseband TIA, and I/Q Generation

The schematic of the IF transconductor, IF mixer, and baseband transimpedance amplifier are shown in Fig. 14. A current mode operation is preferred to maximize the linearity of this last stage, bottleneck of the RX chain [29], [34]. A $n : 1$ transformer interfaces the transconductor and the switching quad as in the RF path. The baseband TIA is implemented with a two-stage differential OTA with resistive feedback and provides $\approx 50\ \Omega$ input impedance, $\approx 50\text{-dB}\Omega$ gain over $\approx 5.6\text{-GHz}$ BW_{−3-dB}, while drawing $\approx 8.46\text{ mA}$ from a 0.9 V supply. The TIA is followed by on-chip buffers to drive the $50\ \Omega$ measurement equipment.

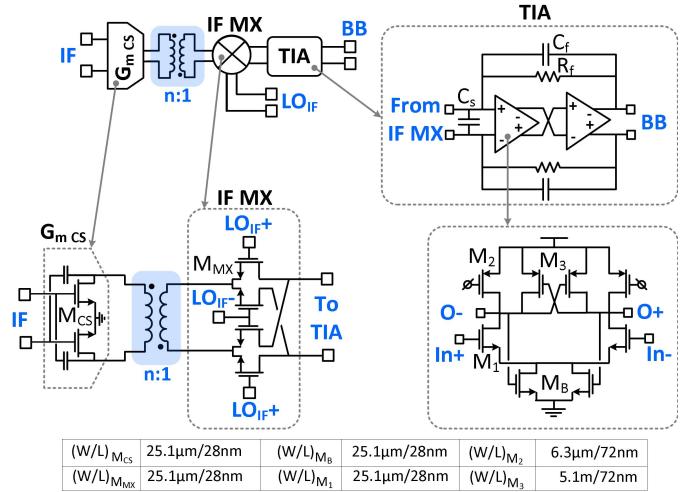


Fig. 14. Circuit implementation of the IF transconductor, IF passive mixer, and baseband TIA.

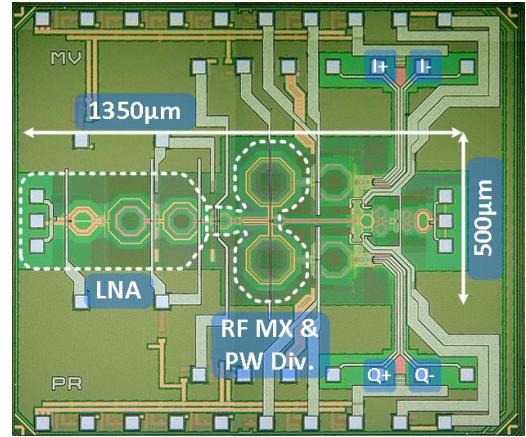


Fig. 15. Die micrograph of the RX test chip. The core area is $1350\ \mu\text{m} \times 500\ \mu\text{m}$. The total pad limited area is $1500\ \mu\text{m} \times 1300\ \mu\text{m}$.

The I/Q LO IF signals are generated on-chip by two inductor-less dividers based on CML static latches locked by an external source. Static dividers are preferred against injection locked ones for their larger locking range and lower silicon area, at expenses of higher power consumption [36], [37].

V. EXPERIMENTAL RESULTS

The RX prototype is integrated in 28-nm bulk CMOS technology without RF thick top metal option (see Fig. 15). GSG probes provide the mm-Wave signals, while the baseband I/Q signals and dc pads are wire-bonded to a PCB. The front-end draws 63 mA, including the baseband TIAs. The dividers and the buffers driving the IF mixers draw 35 mA.

Fig. 16 shows the measured conversion gain. The measured input match against frequency is reported in Fig. 17, while the NF is shown in Fig. 18. Simulation results are also reported for comparison in dotted line. The RX peak conversion gain is 30.8-dB over a BW_{−3-dB} of 27.5-GHz. In-band gain ripple is $<1\text{-dB}$. The minimum NF is 7.3-dB at 70-GHz and varies less than 2-dB over the whole band of operation. S_{11} is lower than -10-dB from 60.5 to 100-GHz. The gain can be reduced by 7.2-dB while keeping a -3-dB bandwidth in excess of 20-GHz by acting on the biasing point of the RF mixer.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART RXs

Ref.	This work	TMTT16 [3]	TMTT16 [3]	ISSCC15 [7]	JSSC16 [11]	JSSC15 [35]	TMTT15 [34]	JSSC11 [8]
Tech.	28nm CMOS	130nm	130nm	28nm	40nm	45nm	65nm	65nm
V _{DD} [V]	0.9	1.6-2.7	1.6-2.7	0.9	1.1	1.1	1	1.2
f _c [GHz]	75	73	83	79	61	55	60	60
Gain [dB]	30.8	23.6	70	70	35	20	26.2	36
RF-BW [dB]	27.5	21.7	5	5	8	20	21	7.5
NF [dB]	7.3-9.1	9.5-12.9	6-7	6-7	6.2-7	>5.5	5.5-10 ⁺	3.8-7
ICP _{1dB} [dBm]	-30.7	-25.3	n.a.	n.a.	-32.5	-24	-27	-18
IIP3 [dBm]	-23.8	-18.1	-10	-12	n.a.	n.a.	n.a.	n.a.
P _{DC} [mW]	57	222	222	59	82.5 [#]	30*	25	40

⁺Graphically estimated [#]No I/Q outputs *Per element

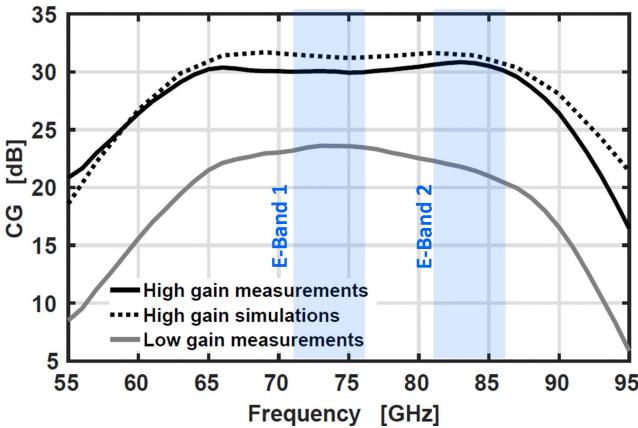


Fig. 16. Measured (continuous line) and simulated (dotted line) RX conversion gain versus frequency, high gain (black line) and low gain (gray line).

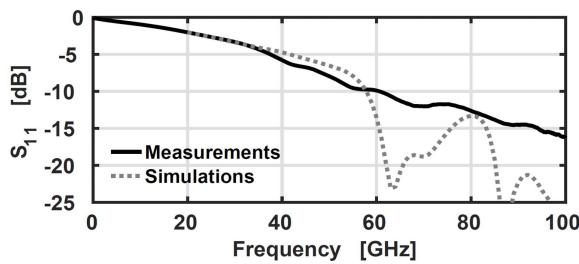


Fig. 17. Measured (continuous line) and simulated (dotted line) RX S₁₁ versus frequency.

Measurements and simulations match very well, especially when the high frequency of operation in combination with the wide bandpass bandwidth is considered.

The IIP3, measured by applying two interferers at 84-GHz with 1-GHz offset is shown in Fig. 19. These measurements were performed using a Millitech CMT-12 Magic Tee with two E-band sources at the input, a 50 Ω termination on one output, and a variable attenuator followed by the DUT on the second output. The measured input-referred 1-dB compression

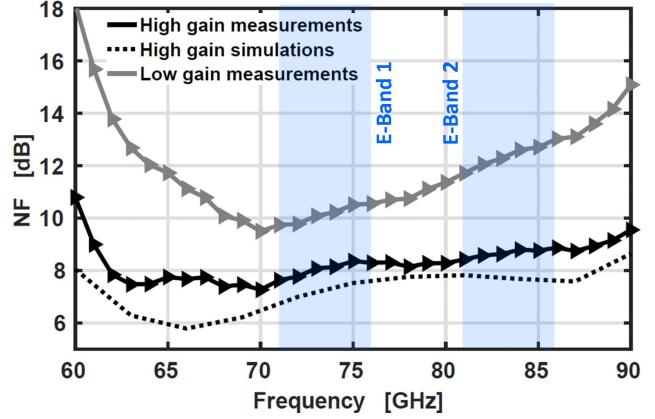


Fig. 18. Measured (continuous line) and simulated (dotted line) RX NF versus frequency, high gain (black line) and low gain (gray line).

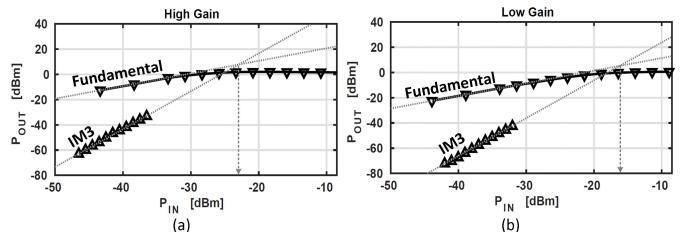


Fig. 19. Measured RX IIP3 (1-GHz offset) against input power at 84-GHz. (a) High gain. (b) Low gain.

point and IIP3 over frequency are shown in Figs. 20 and 21. The worst cases ICP_{1-dB} in the high and low gain mode are -30.7 and -25.3 -dBm, respectively. While the worst case IIP3 is 23.8-dBm (18.1-dBm) in high (low) gain mode over the frequency of operation. Two-tone measurements at 84-GHz repeated for different tone spacing (Δf) are reported in Fig. 22. The IIP3 is -20.6 -dBm at 50 MHz Δf , degrades to -23.1 -dBm at 500 MHz Δf and stays relatively flat up to 2-GHz Δf . It is worth noticing that a large tone spacing ensures a worst case IIP3, particularly relevant when signal with large modulation bandwidth are used.

TABLE III
COMPARISON WITH STATE-OF-THE-ART LNAs IN 70/80-GHz BANDS

Ref.	This work		[38]		[39]	[40]
CMOS Tech. [nm]	28		28		65	65
V _{DD} [V]	0.9		0.9		1.2	1
Gain [dB]	29.6	18	23.8	19.3	17.5	9.4
f _c [GHz]	82.3	81.1	79		77	79
BW _{-3dB} [GHz]	28.3	30.7	10		2	15
GBW [THz]	0.85	0.24	0.15	0.09	0.01	0.04
NF [dB]	6.4-8.2[#]	7.8-9.8[#]	4.9	5.6	7.4	6.7
ICP _{1dB} [dBm]	-28.1	-12.3	-18.5	-15	-22	n.a.
P _{DC} [mW]	31.3	11.7	30.6		30	9.7
FOM [dB]	18.2	12.3	7.7	3.2	-19	1.9

[#]in-band noise figure measurements limited by the available noise source to 90 GHz

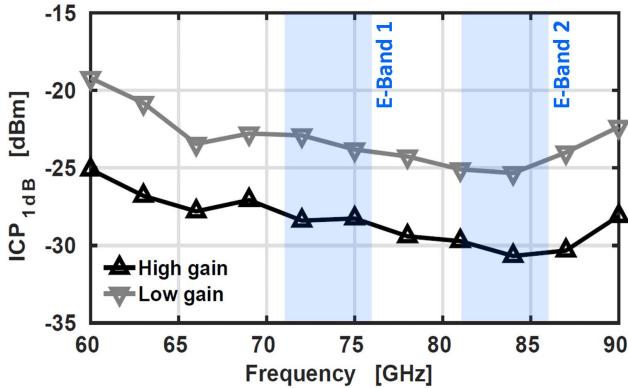


Fig. 20. Measured RX input-referred 1-dB compression point versus frequency, high gain (black line) and low gain (gray line).

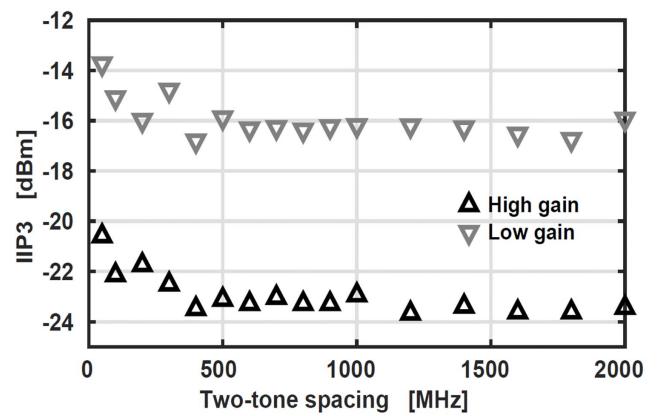


Fig. 22. Measured RX IIP3 versus tone spacing at 84-GHz, high gain (black line) and low gain (gray line).

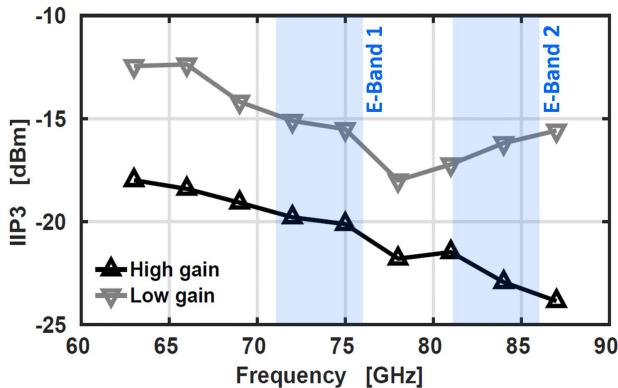


Fig. 21. Measured RX IIP3 (1-GHz offset) versus frequency, high gain (black line) and low gain (gray line).

I and Q phase and amplitude imbalance, measured by applying the downconverted signal to a sampling oscilloscope, are better than 1.6° and 0.7-dB, respectively, from 60 to 90-GHz. The -3 -dB output bandwidth at baseband is 1.9-GHz, limited

by the off-chip connections. The measured image rejection is better 80-dB over the whole band. Table II summarizes the measured results and provides a comparison with state-of-the-art silicon-based mm-Wave RXs. Benefited by the discussed design techniques, this 28-nm bulk CMOS RX achieves the widest BW_{-3dB} with <1-dB in-band gain ripple and <2-dB NF variation at 0.9 V supply.

Fig. 23 shows the die micrograph of the realized stand-alone 28-nm bulk CMOS E-band LNA test chip. The core area is 893 $\mu\text{m} \times 285 \mu\text{m}$, including the input and output RF probe pads. The supply voltage is 0.9 V.

The measured gain, NF, and input match at the highest and lowest gain are reported in Fig. 24. The measured peak gain is 29.6-dB at 84.1-GHz. The BW_{-3dB} spans from 68.1 to 96.4-GHz at the highest gain, resulting in a GBW product of 0.85 THz. The S₁₁ is below -7.6 -dB from 59.4 to 110-GHz, showing a broadband input match. The measured gain can be varied from 18 to 29.6-dB while keeping a bandwidth in excess of 28-GHz, by increasing the bias current from 13 to 34.8 mA. The NF is evaluated using

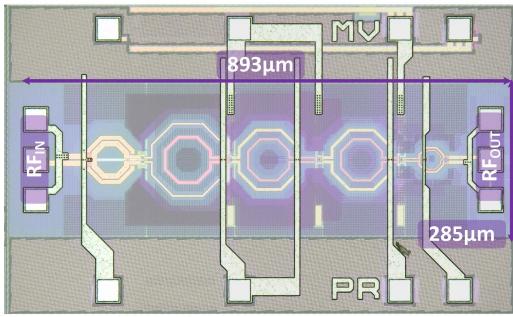


Fig. 23. Die micrograph of the four-stage LNA test chip (core area: $893 \mu\text{m} \times 285 \mu\text{m}$).

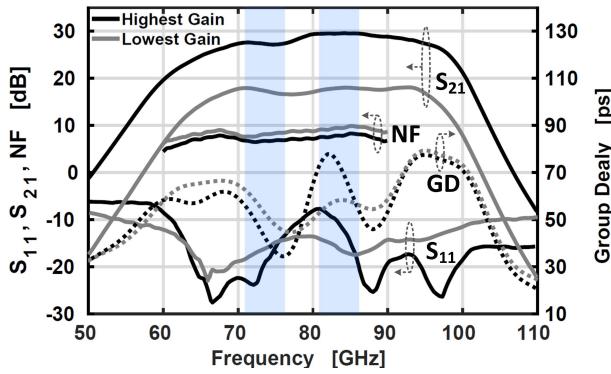


Fig. 24. Measured LNA gain, NF, input match (continuous line) and group delay (dotted line) versus frequency, highest gain (black line), and lowest gain (gray line).

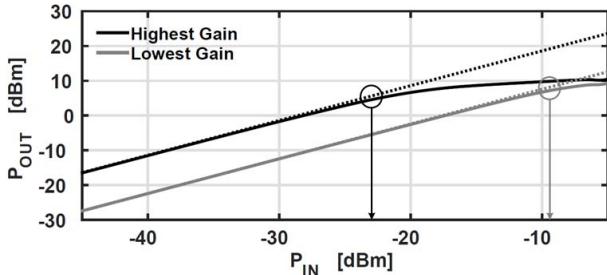


Fig. 25. Measured LNA output power versus input power at 75-GHz, highest gain (black line) and lowest gain (gray line).

a SAGE STZ-12-I1 *E*-band noise source and a Rohde & Schwarz spectrum analyzer. The measured NF reaches the in-band minimum of 6.4-dB at 89.5-GHz, and varies by less than 2-dB from 68.1 to 90-GHz. The measured worst case group delay varies less than ± 21.7 ps from 60 to 100-GHz and less than ± 12.6 ps in each sub-band. Such a flat group delay in combination with the broadband S_{21} response is key to enable wireless data links with wide modulation bandwidth without deteriorating the EVM [6], [16], proving the effectiveness of the proposed design techniques for broadband operation.

The large signal continuous wave measurements at 75-GHz are reported in Fig. 25. The same measurements repeated over frequency are shown in Fig. 26. The worst case in-band input-referred compression point is $-28.1/-12.3$ -dBm at the highest/lowest gain. Table III summarizes the measured results and compares them with state-of-the-art 70/80-GHz CMOS LNAs.

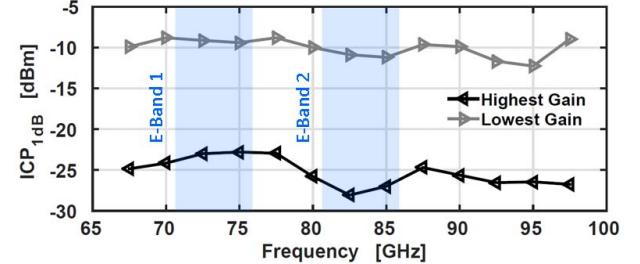


Fig. 26. Measured LNA input-referred 1-dB compression point versus frequency, highest gain (black line) and lowest gain (gray line).

VI. CONCLUSION

In this paper, design techniques to achieve GBW enhancement and high sensitivity at low power consumption for *E*-band RXs, implemented in deep-scaled CMOS have been discussed. Several recently proposed fourth order filters have been compared and the advantages of magnetically coupled resonators over other techniques have been shown. Second order effects such as transformer losses, parasitic inter-winding capacitance, and inter-stage parasitic magnetic coupling on the filter transimpedance have been discussed and techniques to overcome these limitations have been proposed.

Leveraging the discussed design methods, the presented LNA achieves 29.6-dB gain over 28.3-GHz bandwidth, resulting in a GBW product in excess of 0.8 THz. The 28-nm bulk CMOS *E*-band sliding-IF RX shows BW_{-3-dB} from 61.3 to 88.8-GHz with less than 1-dB in-band ripple and <2-dB NF variation at 0.9 V supply. This paper advances the state of the art and demonstrates the first broadband RX suitable for *E*-band point-to-point communication links in deep-scaled bulk CMOS.

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