A 23-mW 24-GS/s 6-bit Voltage-Time Hybrid Time-Interleaved ADC in 28-nm CMOS

Benwei Xu, *Student Member, IEEE*, Yuan Zhou, *Student Member, IEEE*, and Yun Chiu, *Senior Member, IEEE*

***Abstract*— This paper presents a power- and area-efficient 16-way time-interleaved (TI) analog-to-digital converter (ADC) achieving 24-GS/s conversion speed and 6-bit resolution in 28-nm CMOS. A voltage-time hybrid pipeline technique exploiting the comparator input-voltage-output-time dependency is reported to enhance the throughput of successive-approximation-register (SAR) ADCs. A reference-buffer-free capacitive digital-to-analog (CDAC) converter is utilized to mitigate the crosstalk problem in TI-ADCs. Timing mismatches between individual sub-ADCs are estimated with a reference-ADC dithering technique and corrected by digitally controlled delay lines (DCDL). The techniques collectively enabled a very compact design, obviating any input buffer or hierarchical sampling structures. The ADC core consumes 23 mW and occupies an area of 0.03 mm^2. A signal-to-noise plus distortion ratio (SNDR) of 35 dB and a spurious-free dynamic range (SFDR) of 54 dB were measured for a 40-MHz input. For a Nyquist input, the prototype measured an SNDR of 29 dB and an SFDR of 41 dB with all timing mismatch spurs suppressed below −50 dBc after skew calibration.**

***Index Terms*— ADC, background calibration, comparator, crosstalk, skew calibration, SAR ADC, time interleaving, TDC, voltage-time hybrid.**

I. Introduction

TO MEET the ever-increasing demand for data traffic in global networks, new wireline communication systems with 56 Gb/s+ data rate are under high demand [1]. PAM-4 backplane receivers [2]–[4] and coherent fiber-optical receivers [5] are promising devices to achieve such high speed. ADC capable of over 20 GS/s is one key enabler for both technologies. To obtain 20 GS/s + speed, time interleaving is an inevitable choice. Nowadays, designers usually choose either flash or SAR ADC as the sub-ADC to form an interleaved converter array [2]–[12].

Flash ADCs feature high speeds—with a single ADC sample rate of 1∼3-GS/s, 8- to 16-way interleaving can meet the speed target [6], [7]. This leads to a compact TI architecture and minimizes the interleaving overhead, such as the clock generation, interchannel mismatch calibration, and power routing. However, flash ADCs are power inefficient and often require extensive comparator offset calibration [6], [7]. Its large input capacitance and area occupation also make it unsuitable for interleaving. In contrast, SAR ADCs gain a lot of traction for interleaving recently because of its architectural simplicity and superb power efficiency [8]–[12]. Nonetheless, its conversion speed is limited, thus necessitating massive interleaving to support an ultra-high conversion throughput. Massive interleaving complicates the clock generation, calibration, and chip layout, often resulting in more problems than benefits. Large interleaving factor also dictates a hierarchical sampling network with repeated input resampling [8]–[10], introducing extra noise and potentially lowering the overall array power efficiency.

Another issue related to interleaved ADCs is the crosstalk between the sub-ADCs through the shared reference power lines. The conventional solution is to incorporate a separate reference buffer for each sub-ADC [8], [9], often resulting in excessive power/area consumption and potentially introducing an additional source of sub-ADC gain mismatch errors.

While treatments of the static mismatch errors in TI-ADCs are well worked out [13], most existing timing skew calibrations exhibit some limitations. One category of TI-ADC skew calibration relies on a reference ADC with accurate timing [14]–[16]. The autocorrelation of the input signal is utilized in [14] with the help of a 1-bit reference ADC. The autocorrelation of a wide-sense-stationary or wide-sense-cyclostationary signal is inversely proportional to the difference between two sampling points on the same waveform and should be maximized when the skew between the reference path and the array is forced to zero. In [15], the coarse flash ADC in a flash-assisted TI-SAR array is reused as the timing reference. The statistical sampled value difference between the flash and the SAR sub-ADC derived from the code histogram of the SAR is minimized to align the sampling clock of the sub-ADC to that of the flash. Two reference ADCs are employed to extract the input derivative in [16]. One reference ADC samples the input with a Δt delay relative to the other reference; the input derivative is estimated by calculating their output difference and the skew is determined by dividing the skew error by the input derivative.

In this work, we demonstrate a new approach to improve the speed of SAR over 1 GS/s with a voltage-time hybrid structure [17]. Interleaving such ADCs to achieve 24 GS/s, we can take the simplicity and power efficiency advantages of the SAR while retaining a compact design with a low interleaving factor. A reference-buffer-free CDAC is utilized to mitigate the crosstalk problem among the sub-ADCs. Timing skews in the

Manuscript received August 18, 2016; revised October 10, 2016 and December 5, 2016; accepted December 11, 2016. Date of publication January 23, 2017; date of current version March 23, 2017. This paper was approved by Guest Editor Brian Ginsburg. This work is supported by the Semiconductor Research Corporation through Texas Analog Center of Excellence, The University of Texas at Dallas, under Grant 1836.148.

The authors are with the Texas Analog Center of Excellence, The University of Texas at Dallas, Richardson, TX 75080 USA (e-mail: benway.xu@gmail.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2016.2642204

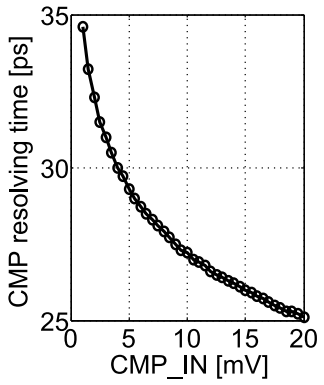


Fig. 1. Simulated comparator resolving time versus input voltage magnitude.

array are extracted using a reference-ADC dithering technique and corrected by DCDLs.

This paper is organized as follows. Section II covers the basics of the voltage-time hybrid pipeline SAR conversion principle. Section III describes the overall interleaving architecture and the skew calibration technique, followed by the circuit design details in Section IV. Section V presents the prototype silicon measurement results. Finally, Section VI concludes this paper.

II. Voltage-Time Hybrid Pipeline SAR ADC

A. Comparator as Voltage-to-Time Converter

A conventional voltage-domain pipeline SAR ADC employs a dedicated residue amplifier (RA) to transfer an amplified residue voltage to the second stage [18]. One feature of the pipeline SAR ADC is the small residue signal due to a multi-bit first stage. Thereby, the RA output swing is small and can easily achieve high conversion speed and linearity. However, since offset inevitably exists between the RA and the SAR comparator, it can easily overwhelm the residue and lead to an overly large RA output swing. Unless the offset is calibrated, the RA linearity will be comprised and extra redundancy in the second stage is required. The RA power consumption is also a bottleneck to achieve high efficiency, especially when clocked at gigahertz range.

In fact, the comparator in the first-stage SAR ADC is a natural "RA"—when the first-stage residue signal is presented to the comparator, with small residue magnitude, its resolving time can be expressed as [19]

$$t_{\text{cmp}} = t_0 - \tau_{\text{cmp}} \cdot \ln(V_i / V_0) \tag{1}$$

where the resolving time of a comparator is defined as the time lapse from when the comparator is strobed until it outputs the decision. The input magnitude information is embedded in the comparator resolving time, as indicated by the simulated resolving time of a strong-arm comparator versus its input voltage magnitude shown in Fig. 1.

If we can determine the voltage-to-time (V2T) transfer curve of the comparator and quantize its resolving time, the comparator voltage input, in turn, can be determined. Most existing works of this genre only report the extraction of one extra bit. For example, this property in SAR ADC is explored in [20] by detecting the comparator resolving time in the LSB cycle to yield one more bit. In flash ADCs, this property is utilized to halve the comparator count by interpolating the adjacent comparators' outputs in the time domain [21].

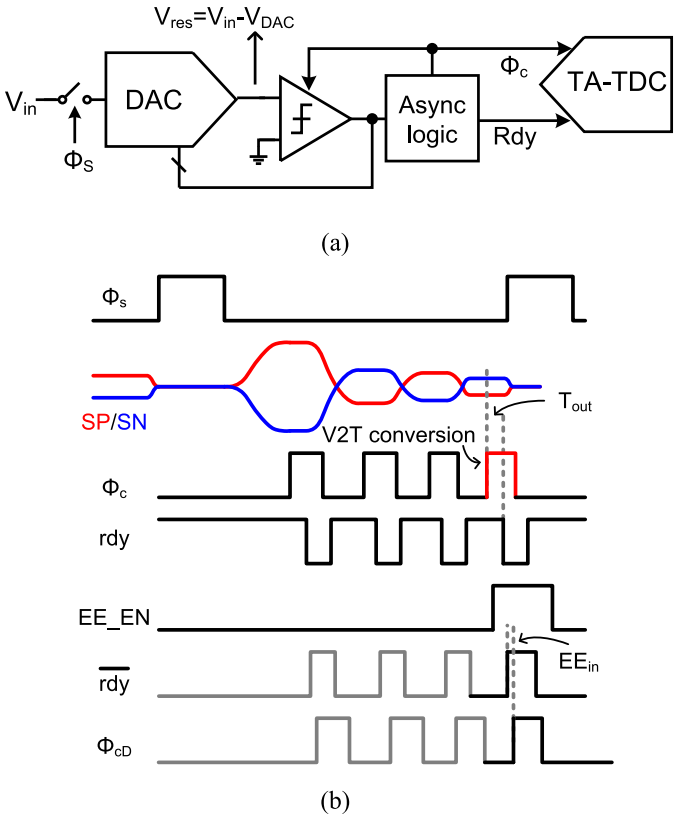


Fig. 2. (a) Block diagram and (b) timing diagram of voltage-time hybrid pipeline SAR ADC.

B. Hybrid Pipeline SAR ADC

We note in Fig. 1 that the V2T conversion gain diminishes as the input magnitude increases. To maintain a reasonable conversion gain, the input range of the V2T converter needs to be limited. The maximum input magnitude for V2T conversion is set to 20 mV in this design. A 3-bit SAR ADC is chosen as the first stage to generate a nominal residue within [−15 mV, +15 mV]. The 4th comparison is then performed as the V2T conversion. The residue sign is determined by the 4th comparison outcome and the residue magnitude is digitized based on the quantized comparator resolving time.

A delay-line-based 4-bit time-to-digital converter (TDC) is employed as the second stage in this work. The TDC input range is set by the technology and is larger than the V2T conversion output range. To match the two ranges, a time amplifier (TA) is inserted between the V2T and TDC. The resulting system diagram is shown in Fig. 2(a) and the timing diagram is shown in Fig. 2(b), where Φ_s is the sampling clock, SP/SN is the differential summing-node voltage, Φ_c is the comparator clock, and rdy indicates that the comparison is done. An edge extractor (EE) is enabled by the EE_EN signal

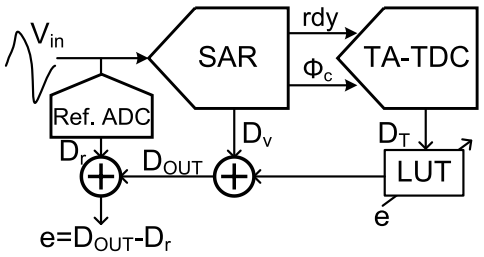
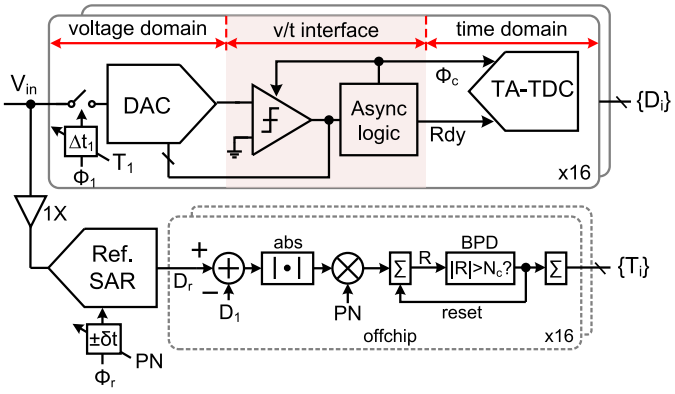
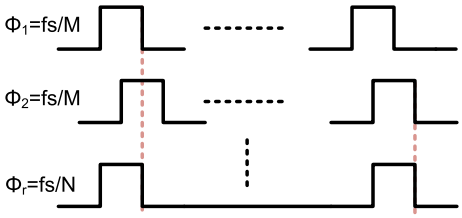


Fig. 3. Concept of V2T nonlinearity calibration by digital postprocessing.



(a)



(b)

Fig. 4. (a) System diagram and (b) timing diagram of the prototype TI-ADC with reference path.

and captures the 4th inverted rdy and the delayed Φ_c (Φ_{cD}) pulse. Detailed explanation of the EE and related signals will be covered in Section IV-C.

C. V2T Nonlinearity Calibration

The V2T transfer curve shown in Fig. 1 exhibits poor linearity. In this work, we choose to correct the V2T nonlinearity by digital post-processing. With a nonlinear V2T transfer and a linear TDC, the input-referred voltage-domain decision levels are unevenly spaced. As long as the output codes of the second stage (D_T) can be mapped to the correct residue amplitude, the input value can be properly derived. To minimize the input-referred quantization noise, a 4 bit instead of 2-bit TDC is employed in the second stage to compensate for the low conversion gain region. The mapping can be realized by a lookup table (LUT). With a known input signal, the LUT coefficients can be learned in the foreground; but with PVT variations, the LUT needs to be updated adaptively—with a reference ADC, the LUT can be trained in the background, as shown in Fig. 3, in which the reference ADC and the two-step hybrid ADC sample the same input. Thus, their digital outputs D_r and D_{OUT} should be identical. Any difference between D_r and D_{OUT} can be used to train the LUT until $D_r = D_{\mathrm{OUT}}$ holds [22].

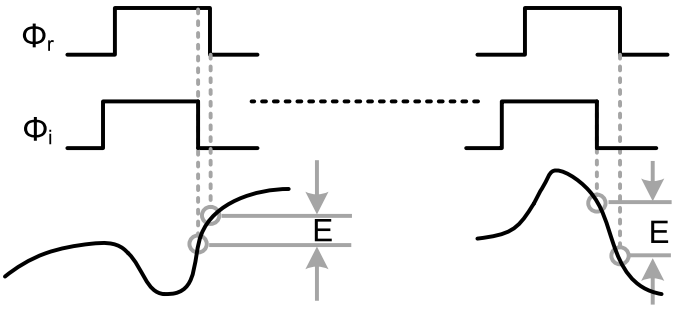


Fig. 5. Skew-induced conversion error.

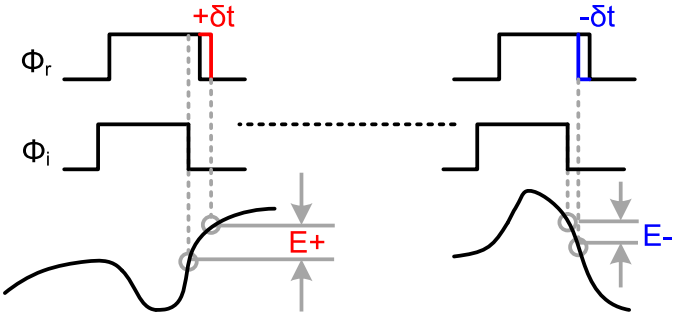


Fig. 6. Skew sign estimation.

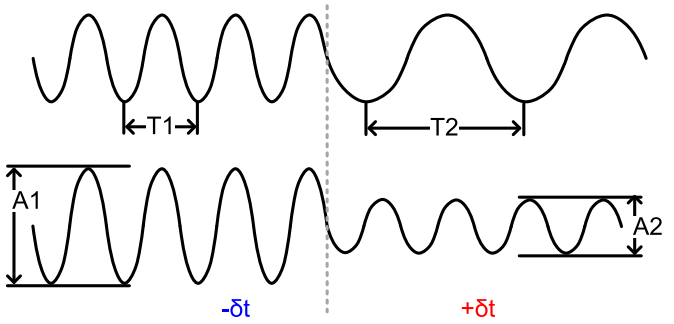


Fig. 7. Problematic scenario for skew estimation.

III. Background Timing Skew Estimation

The overall system diagram is shown in Fig. 4, in which a reference ADC is employed besides the 16-way interleaved hybrid SAR ADCs. Using a reference ADC in a TI-ADC array as static and/or timing references has been discussed in [13]–[16].

In the presence of timing skew, the sampled values of the reference ADC and sub-ADC will be different. As shown in Fig. 5, the reference ADC sampling clock Φ_r is assumed to be lagging the sub-ADC$_i$ sampling clock Φ_i (i.e., $\Phi_r = \Phi_i + \Delta t_i$ with $\Delta t_i > 0$). With a reasonably small skew magnitude, the skew-induced error can be expressed as

$$E \approx \Delta t_i \cdot \frac{dV}{dt}. \tag{2}$$

The error magnitude is proportional to the skew magnitude.

To estimate the skew value, a DCDL is employed to dither Φ_r. The DCDL delays or advances Φ_r by δt_r depending on its digital control bit. As shown in Fig. 6, after dither, the

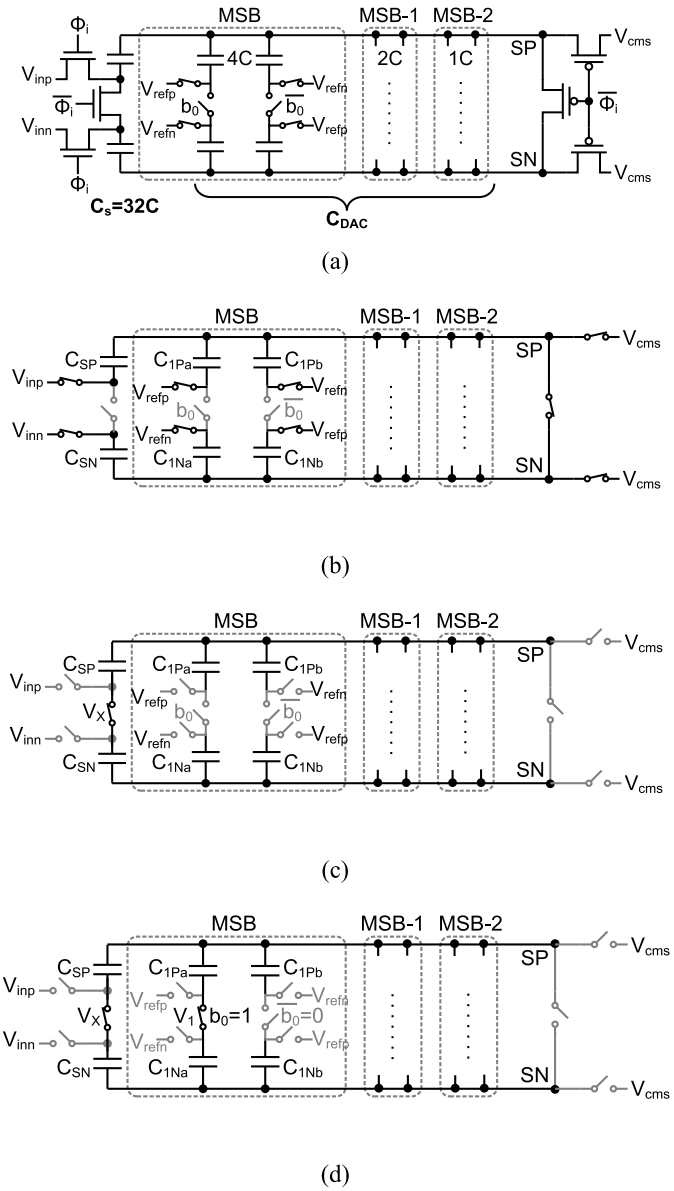


Fig. 8. (a) Reference-buffer-free DAC structure, (b) in tracking phase, (c) in MSB decision cycle, and (d) in MSB DAC charge-redistribution phase.

skew-induced error becomes

$$E = (\Delta t_i \pm \delta t_r) \cdot \frac{dV}{dt}. \tag{3}$$

The average absolute error with advanced Φ_r and delayed Φ_r can be written as

$$\overline{|E_+|} = |D_r - D_i| = |\Delta t_i + \delta t_r| \cdot \overline{\left|\frac{dV}{dt}\right|} \tag{4}$$

$$\overline{|E_-|} = |D_r - D_i| = |\Delta t_i - \delta t_r| \cdot \overline{\left|\frac{dV}{dt}\right|}. \tag{5}$$

Since we have assumed that $\Delta t_i > 0$, $|\Delta t_i + \delta t_r| > |\Delta t_i - \delta t_r|$, thereby $\overline{|E_+|} > \overline{|E_-|}$. Thus, the skew sign can be estimated by

$$\text{sign}(\Delta t_i) = \text{sign}\left(\sum |E_+| - \sum |E_-|\right). \tag{6}$$

If $\Delta t_i < 0$ holds, the converse scenario would be true for $\overline{|E_+|}$ and $\overline{|E_-|}$, as well as the sign relationship. Assuming that Φ_r is delayed and advanced for the same number of iterations, summation can be used to replace averaging. The estimated skew sign is then accumulated and low-pass filtered [23] to drive a DCDL to align Φ_i to Φ_r. The RHS of (6) becomes zero when Δt_i reaches zero and the skew calibration is complete.

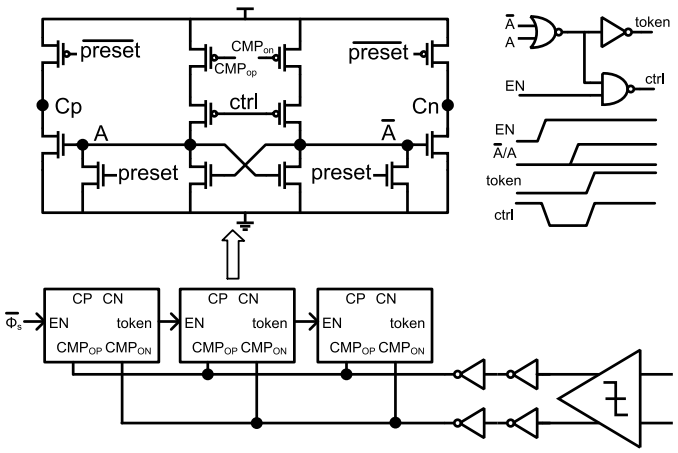


Fig. 9. SAR logic with simplified timing diagram.

If the sub-ADC and the reference ADC are both 6 bit and the input is $A \cdot sin(\omega t)$, the dither-induced sampled value difference can be expressed as $A\omega cos(\omega t) \cdot \delta t$. The maximum sample difference is thus $A\omega \cdot \delta t$. For this difference to be detected, it needs to be larger than 1 LSB, where 1 LSB $= A/32$. Then, we can derive that $\delta t > 1/(64\pi \cdot f)$ is required. On the other hand, the dither magnitude cannot be too large either. If the input signal exercises more than half a period within the dither gap, the skew estimation will fail. In this paper, we restrict the dither magnitude to be less than a quarter of the input signal period, i.e., $\delta t < 1/(4f)$ holds. For example, for $f = 10$ GHz, δt needs to be within [500 fs, 25 ps], and for $f = 1$ GHz, δt needs to be within [5 ps, 250 ps]. In this design, to cover input frequencies from 1 to 12 GHz, the dither range is set to [5 ps, 20 ps].

One potential issue related to the above-mentioned skew calibration scheme is that the modulation pattern of the reference ADC might be correlated with the input signal. As shown in Fig. 7, if T1 $\ll$ T2 or A1 $\gg$ A2, Φ_r is always delayed when dV/dt is large or advanced when dV/dt is small. In this case, (4) and (5) can be rewritten as

$$\overline{|E_+|} = |\Delta t_i + \delta t_r| \cdot \overline{\left|\frac{dV}{dt}\right|}_{\text{large}} \tag{7}$$

$$\overline{|E_-|} = |\Delta t_i - \delta t_r| \cdot \overline{\left|\frac{dV}{dt}\right|}_{\text{small}}. \tag{8}$$

And the relative magnitude of $\overline{|E_+|}$ and $\overline{|E_-|}$ is independent of Δt_i. Instead, it mainly depends on the magnitude of dV/dt. Thus, the skew information cannot be extracted by comparing $\overline{|E_+|}$ to $\overline{|E_-|}$. To avoid this scenario, the DCDL control signal for Φ_r is chosen to be a 1-bit pseudorandom noise (PN). When PN $= +/-1$, the DCDL delays/advances Φ_r, respectively.

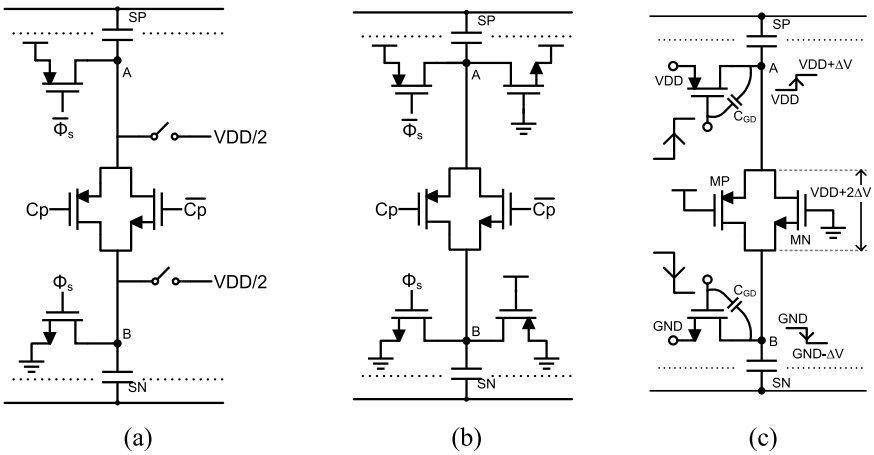


Fig. 10. DAC driver (a) with extra common-mode switches, (b) with dummy switches, and (c) leakage problem of the crowbar switch.

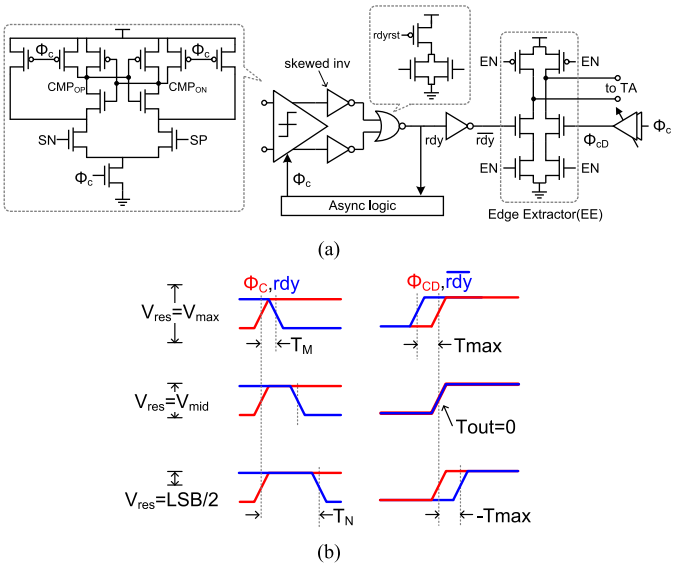


Fig. 11. V2T interface. (a) Schematic. (b) Signal waveforms.

IV. Circuit Implementation

A. Crosstalk-Free Capacitive DAC

The crosstalk through reference power lines is a serious problem in TI ADCs. Conventionally CDACs from different ADCs load the same reference lines, causing periodical disturbance on these lines due to the DAC activities when the decoupling capacitor shares charge with the CDACs [24]. In a conventional single SAR ADC, the comparator can wait for the reference voltage to settle before making a decision. In an interleaved array, the disturbance on the reference lines never stops because of the activities of many sub-ADCs.

We employ a reference-buffer-free CDAC structure in this work, as shown in Fig. 8(a). Similar to [24] and [25], the sampling capacitor C_s and DAC capacitor C_{DAC} are separated. C_s and C_{DAC} are used to sample V_{in} and $V_{\mathrm{refp}}/V_{\mathrm{refn}}$, respectively, during the tracking phase. The simplified circuit in the tracking phase is shown in Fig. 8(b). After the tracking phase, the DAC configuration is shown in Fig. 8(c)—all switches in C_{DAC} are open and the C_s crowbar switch shorts the bottom plates of C_{SP} and C_{SN}. As a result, only C_s and the related charge are involved in the trailing charge redistribution. The summing-node differential voltage is $-V_{\mathrm{in}}$. The comparator can then be strobed to make the MSB decision.

Depending on the MSB outcome, one of the MSB capacitor pairs are shorted by its own crowbar switch. For example, the bottom plates of $C_{1\mathrm{Pa}}$ and $C_{1\mathrm{Na}}$ are shorted and the bottom plates of $C_{1\mathrm{Pb}}$ and $C_{1\mathrm{Nb}}$ are left floating, as shown in Fig. 8(d). With $C_{\mathrm{sp}} = C_{\mathrm{sn}} = C_s$ and $C_{1\mathrm{Pa}} = C_{1\mathrm{Pb}} = C_{1\mathrm{Na}} = C_{1\mathrm{Nb}} = C_1$, the summing-node differential voltage can be derived as

$$V_{\mathrm{SP}} - V_{\mathrm{SN}} = \frac{-(V_{\mathrm{refp}} - V_{\mathrm{refn}}) \cdot C_1 - V_{\mathrm{in}} \cdot C_s}{C_1 + C_s}. \tag{9}$$

In the prototype, V_{refp} and V_{refn} are V_{DD} and GND, respectively, and (9) can be further simplified to

$$V_{\mathrm{sp}} - V_{\mathrm{sn}} = \frac{-C_s}{C_{\mathrm{tot}}} \left(V_{\mathrm{in}} + \frac{C_1}{C_s} V_{\mathrm{DD}} \right). \tag{10}$$

With C_1/C_s as the MSB weight, the structure behaves the same as the conventional SAR DAC. After the DAC voltage settles, the comparator can make the MSB-1 decision and the same operation is then repeated. Eventually, the summing-node voltage can be expressed as

$$V_{\mathrm{sp}} - V_{\mathrm{sn}} = \frac{-C_s}{C_{\mathrm{tot}}} \left(V_{\mathrm{in}} + V_{\mathrm{DD}} \sum D_i \cdot \frac{C_i}{C_s} \right). \tag{11}$$

The reference voltage of the DAC is separated from other blocks and shared by all sub-ADCs. During the bit cycles, CDAC is totally disconnected from the reference power lines. Thus, the crosstalk is largely reduced. In the tracking phase, when C_{DAC} is precharged, since half of C_{DAC} is intact and the other half is always discharged to $V_{\mathrm{DD}}/2$ from the last sample, the kickback from C_{DAC} to the reference lines is always nearly constant.

Conventionally SAR ADCs utilize V_{DD}/GND as $V_{\mathrm{refp}}/V_{\mathrm{refn}}$, respectively, and supports peak-to-peak differential input swing of 2VDD with $\sum C_i = C_s$. High-speed, low-resolution ADCs often use a smaller input swing instead to improve the tracking performance. In the prototype, C_{DAC} can be scaled down to attenuate the reference voltage as it is separated from C_s. With $V_{\mathrm{refp}} = 850$ mV for the target technology, $C_1 = C_s/8$ is chosen to cover a differential input swing of 425 $\mathrm{mV_{pp}}$.

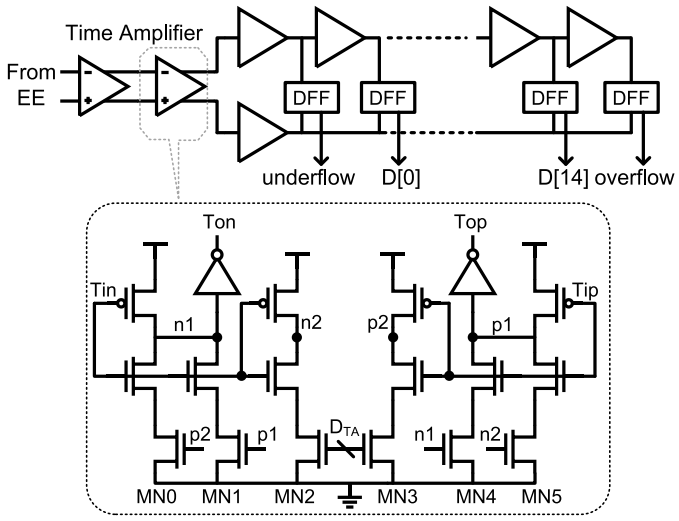


Fig. 12. Circuit details of the TA and TDC.

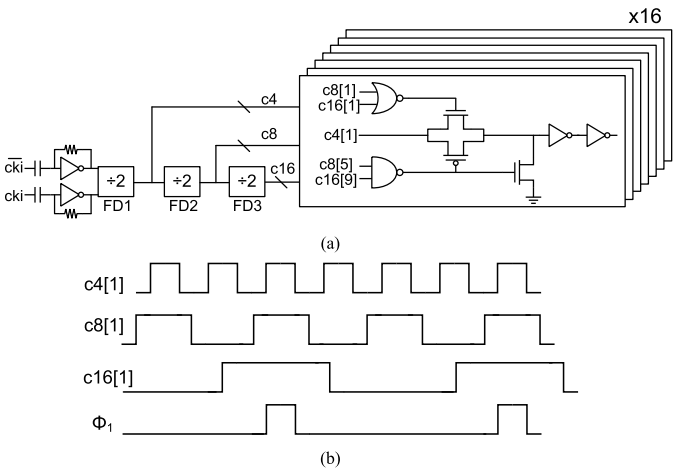


Fig. 13. Multiphase clock generation. (a) Schematic. (b) Timing diagram.

Since bottom-plate sampling is employed in this paper and the input swing is small, both the summing-node common-mode voltage ($V_{\rm cms}$) and the input common-mode voltage ($V_{\rm cmi}$) can differ from $V_{\rm DD}/2$. $V_{\rm cmi}$ of 125 mV is chosen to allow a single nMOS input switch without bootstrapping, whereas $V_{\rm cms}$ of 600 mV is chosen to accelerate the comparator. $V_{\rm cms}$ is supplied directly from an external source and shared by all sub-ADCs.

In the DAC structure outlined earlier, $C_{\rm tot}$ varies from cycle to cycle. It increases from C_s to $C_s + \sum C_i$ from the MSB cycle to the LSB cycle. This means the attenuation of $V_{\rm in}$ elevates as the bit cycles unfold. In a traditional design, since $C_s = \sum C_i$, the input is eventually attenuated by a factor of 2 from MSB to LSB, and thus, the input-referred comparator offset is eventually doubled—SAR ADC cannot tolerate varying comparator offset and this needs to be fixed. In [25], comparator offset calibration is employed. In our prototype, since $C_{\rm DAC}$ is scaled, the variation of $C_{\rm tot}$ is relatively small, i.e., $C_{\rm tot}$ changes from $C_s = 32$Cu to 39Cu. As a result, the offset variation is also small. To avoid offset calibration, this error is absorbed into the interstage redundancy. The nominal residue range is [−15 mV, +15 mV], while the V2T and the second stage are designed to cover [−20 mV, +20 mV]. Behavioral simulation verifies that the scheme works well with comparator offset as large as 50 mV when offset is the only error source.

B. SAR Logic and DAC Driver

The SAR logic is modified from [26] and shown in Fig. 9. It works in a domino-like fashion. When the current SAR logic captures the data, a/abar generate a token signal which locks the data in the current SAR latch and then is used as the EN signal to enable the next SAR logic.

When the bottom plates of the DAC capacitors are shorted, the voltage on the shorted node will become $(V_{\rm refp} + V_{\rm refn})/2$ if the parasitic capacitors on the P side and N side are the same. If the voltage deviates from this value, the summing-node differential voltage is not affected, but the common-mode voltage will change, which can cause the comparator offset to vary. Since pMOS/nMOS switches are used for node A/B, respectively, the parasitics are not the same. Extra switches can be added to tie the middle node to $V_{\rm DD}/2$, as shown in Fig. 10(a). Then, the DAC is no longer floating in this configuration and the summing-node common mode becomes vulnerable to crosstalk. To resolve this problem, dummy switches are added to node A/B to match their parasitic capacitances, as shown in Fig. 10(b).

The voltage across the crowbar switches in $C_{\rm DAC}$ is larger than $V_{\rm DD}$, as shown in Fig. 10(c). As a result, the leakage current cannot be ignored in the target process. To address this issue, MN and MP are chosen as nominal threshold devices with a channel length of $2 \cdot L_{\rm min}$. Short conversion phases also relax the leakage problem.

C. Voltage-to-Time Conversion Interface

The V2T interface is modified from the asynchronous SAR ADC of [27] and the detail is shown in Fig. 11(a). The comparator is a standard strong-arm type [28]. A dynamic NOR gate uses the buffered comparator outputs to generate the rdy signal. During the reset phase, both the comparator outputs and the rdy signal are high. When the comparator finishes the decision, one of its outputs becomes low and the rdy signal is pulled low.

The buffer inverters are designed with a skewed threshold—instead of sizing the pMOS and nMOS to have a threshold near $V_{\rm DD}/2$, the nMOS is sized up to lower the threshold. Low threshold inverter is necessary to avoid the rdy generator being falsely triggered, i.e., with a small input magnitude, after the comparator is strobed and before it finishes decision, both outputs are discharged and can reach a voltage level lower than $V_{\rm DD}/2$ before they depart from each other toward $V_{\rm DD}$ and GND, respectively.

The Φ_c and rdy signal are generated in each cycle, but only those in the 4th cycle need to be passed to the second stage for further processing. The token signal from the 3rd SAR logic is used to enable the EE to capture the 4th Φ_c rising edge and the rdy falling edge, as shown in Fig. 2(b). Before the EE is enabled, both outputs are reset to $V_{\rm DD}$; after it is enabled, the outputs are left floating. When the pull-down nMOS receives

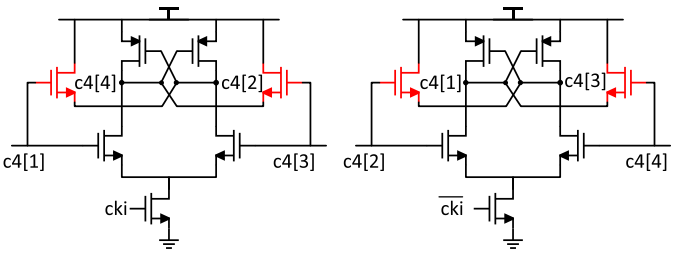


Fig. 14. Schematic of the divide-by-2 FD.

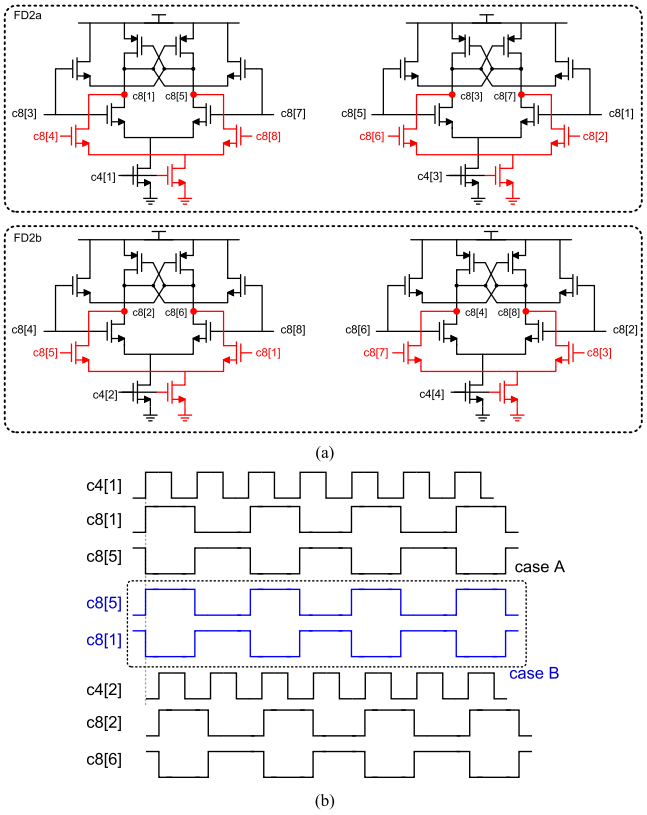


Fig. 15. FD2. (a) Schematic. (b) Timing diagram.

the rising $\overline{\text{rdy}}$ and Φ_{cD}, the outputs are discharged and the time difference between them forms the V2T outcome.

The Φ_c and rdy signal are generated sequentially and (1) suggests that there is a fixed delay between rdy and Φ_c even with an infinitely large input. This fixed delay inevitably enlarges the V2T output range and may saturate the TA. The output time with the largest input voltage (~20 mV) is T_M and the smallest input voltage (~2 mV = LSB/2) is T_N. For an input smaller than LSB/2, the output time is larger than T_N and should be truncated to T_N. The purpose of the added delay line is to delay Φ_c, such that V_{max} is converted to $+T_{\text{max}}$ before the TDC (corresponding to the largest TDC code), while LSB/2 is converted to $-T_{\text{max}}$ (corresponding to the smallest TDC code). When the input voltage is in the middle, the output time is zero, as shown in Fig. 11(b).

D. Time Amplifier and TDC

Simulation reveals that a 20-mV input range results in an output time span of 10 ps. To resolve 4 bit, a TDC with an LSB size less than 1 ps is needed. Since a delay-line-based TDC

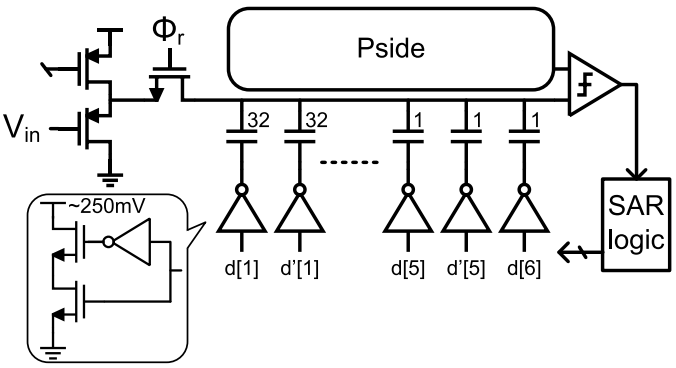


Fig. 16. Block diagram of the reference SAR ADC.

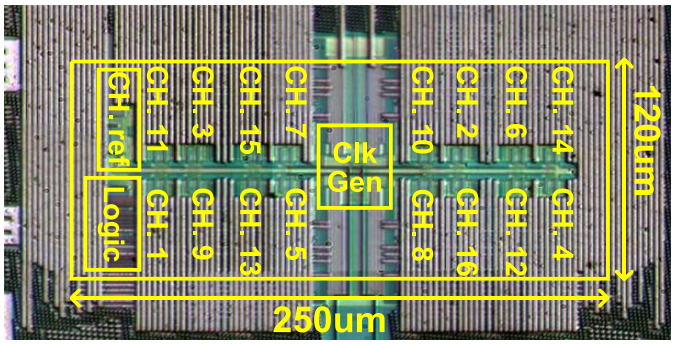


Fig. 17. Chip micrograph.

is used in this design, the LSB size is set by the technology, which is around 9 ps (≈ two inverter delay). The output from the V2T needs to be amplified before it reaches the TDC.

Two cascaded TAs [29] are used to amplify the V2T output, as shown in Fig. 12. The TA gain is digitally controlled by varying the sizes of MN2 and MN3, which controls the discharging speed of the nodes n2 and p2. For both TAs, MN2 and MN3 are implemented as a 4 bit binary-weighted nMOS array. With an input time range of [−20 ps, 20 ps], the TA provides a gain ranging from 2 to 15.

The V2T gain, the TA gain, and the TDC LSB size are all subject to PVT variations. Therefore, the TA gain and the delay line for Φ_c must be made tunable to cover the variations. To assist the calibration, as shown in Fig. 12, underflow and overflow detectors are added before and after the first and last delay cells, respectively, in the 4 bit TDC. For example, when both detectors are triggered, the TDC must be saturated and the TA gain needs to be reduced.

Since the input to the V2T can be as small as zero, which converts to a large output time even with optimal DCDL and TA settings, the underflow detector can still be triggered. When the first-stage residue falls in the range of [−0.5 LSB, 0.5 LSB] and the underflow detector is triggered, it should be considered normal and the second-stage output should be assigned to the minimum TDC code. With an evenly distributed residue signal, its probability of falling within [−0.5 LSB, 0.5 LSB] is 10% (with a 4-mV LSB and a 20-mV maximum residue). As long as the probability of the minimum TDC code plus the triggered underflow detector is less than 10%, the DCDL and TA settings need no update.

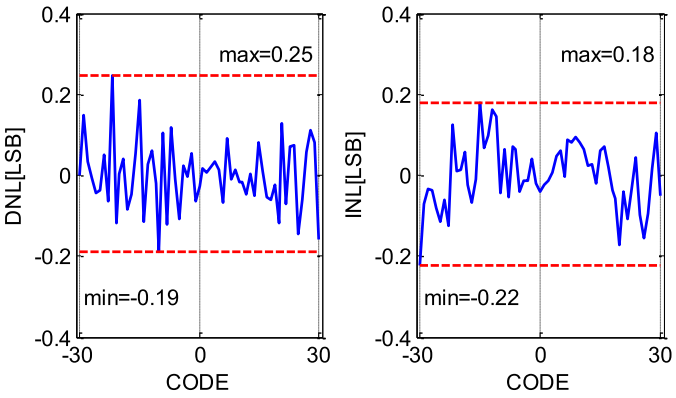


Fig. 18. Measured DNL and INL.

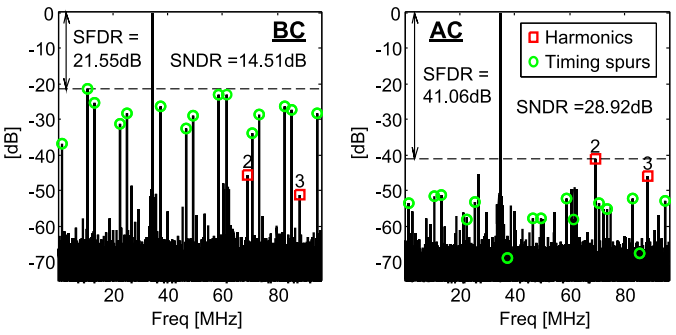


Fig. 19. Measured ADC array output spectra (decimated by 125) before and after skew calibration at fs = 24 GS/s with an 11.9-GHz sine-wave input.

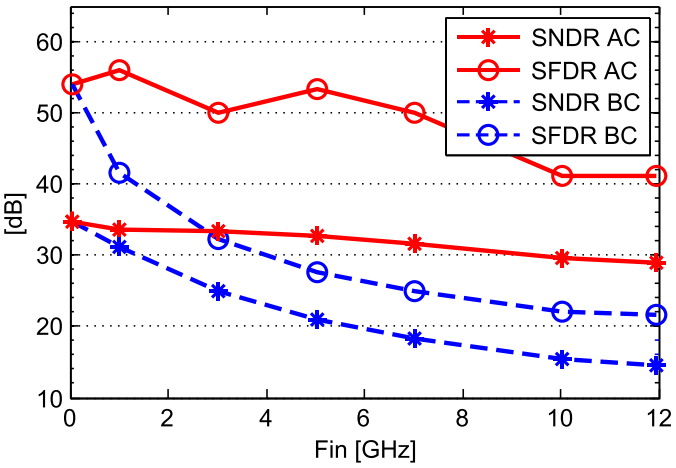


Fig. 20. Measured ADC dynamic performance.

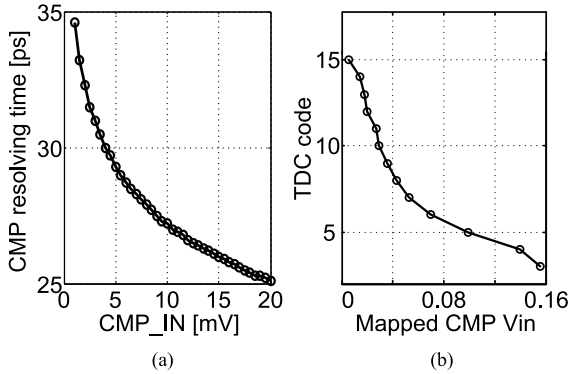


Fig. 21. (a) Simulated V2T transfer curve. (b) Measured LUT content.

E. Circuitry for Interleaving

The multiphase clock generation circuit resembles that of [30]. Differential clocks cki/$\overline{\text{cki}}$ at fs/2 = 12 GHz are used. Three cascaded divide-by-2 frequency dividers (FD) receive cki/$\overline{\text{cki}}$ and generate a 4-phase clock c4[1:4], an 8-phase clock c8[1:8], and a 16-phase clock c16[1:16] sequentially. Different phases from c8 and c16 are used to gate c4[1:4] to generate the sampling clock for each sub-ADC, as shown in Fig. 13(b). The skew performance is mainly determined by c4—with only one critical FD, it is easier to maintain a symmetrical layout and FD2/FD3 can be downscaled to save power and area.

The FD constitutes cross-connected latches, as shown in Fig. 14. A feedforward path highlighted in red is also introduced, in which an nMOS source follower precharges the output node to speed up the latches [31]. The FD1 output c4[1:4] consists of four well-defined phases; c4[1]–c4[4] are generated sequentially with a 90° phase spacing. FD2 consists of two separated FDs, i.e., FD2a is driven by clock c4[1, 3] and FD2b is driven by c4[2, 4]. When c4[1, 3] trigger FD2a, two possible outputs can occur, as shown in black and blue, respectively, in Fig. 15(b). If only the outputs of FD2a are considered, these two scenarios are indistinguishable. If the outputs from FD2b are also considered, a phase ambiguity problem arises (there are two possible outcomes from FD2b as well; for simplicity, only one case is shown here). If the FD2a output is case A, then the c8[1:8] are the correct outputs. However, if the FD2a output is case B, then the output sequence of FD2 becomes [1, 6, 3, 8, 5, 2, 7, 4]. To avoid the ambiguity, weak couplers highlighted in red are added to ensure the phase relationship between the FD2a and FD2b. The same technique is also applied to the FD3.

To facilitate the skew calibration, an on-chip reference ADC clocked at fs/125 (∼192 MHz) is included. Since speed is not of concern, a conventional 7 bit SAR ADC is adopted, as shown in Fig. 16. A pMOS source follower is used to isolate the activity of the reference ADC and to translate V_{cmi} from near ground to roughly $V_{\text{DD}}/2$. Note that the input buffer only drives the reference ADC, not the entire TI array. Since the input swing is smaller than 2 V_{DD}, an extra reference voltage of 250 mV is used for the reference ADC.

V. Measurement Results

The prototype ADC was fabricated in a 28-nm 1P10M CMOS process. A chip micrograph is shown in Fig. 17 with an active area of 0.03 mm^2 (250 μm × 120 μm). Thanks to the small 16 fF (single-ended) input capacitance, the TI-ADC is directly driven from a 50-Ω signal source without any buffer or hierarchical sampler. The prototype is clocked at 24 GS/s and the total power consumption is 22.94 mW. Out of which, 12.8 mW is from the ADC array with an 850-mV supply, 9.5 mW is from the clock generation with a 950-mV supply, and 0.64 mW is from the reference ADC.

TABLE I
PERFORMANCE COMPARISON

	This Work	[9]	[7]	[6]	[11]
Architecture	TI-SAR	TI-SAR	TI-BS	TI-flash	TI-SAR
Technology	28nm	32nm SOI	65nm	32nm SOI	28nm SOI
Power Supply (V)	0.85/0.95	0.9/1	1	0.9	1
Sample Rate (GS/s)	24	36	25	20	10
Resolution (bits)	6	6	6	6	6
SNDR/SFDR @ LF (dB)	34.8/53.9	32.6/47	32/42	34.8/NA	34/39
SNDR/SFDR @ HF (dB)	28.9/41	31.6/42.8	29.7/40	30.7/NA	34.3/41.1
Active Area (mm^2)	0.03	0.05	0.24	0.25	0.01
Power (mW)	23	110	88	69.5	32
FoM @ LF/HF (fJ/c-s)	21/42	88/98	108/143	76/124	81/81

The digital calibration logic is implemented off-chip. The adaptation of the LUT is performed in the foreground using a sine-fit algorithm.

The measured DNL and INL of the prototype are shown in Fig. 18. The maximum DNL is $+0.25/-0.19$ LSBs and the maximum INL is $+0.18/-0.22$ LSBs.

With an 11.9-GHz sine-wave input, the ADC output spectra before and after skew calibration are shown in Fig. 19. Without calibration, the performance was limited by the TI spurs highlighted in green circles. The SFDR was 21.6 dB and SNDR was 14.5 dB. With skew calibration, all skew-related spurs are suppressed to below -50 dBc. The SFDR and SNDR improve to 41.1 and 28.9 dB, respectively.

The ADC dynamic performance for different input frequencies is shown in Fig. 20. Before calibration, the array performance was limited by the skew starting from 1-GHz input frequency. After calibration, the SFDR remained above 50 dB from DC to 7 GHz. For higher input frequencies, the SFDR was limited by the HD2 and the SNDR was mainly limited by the jitter from the clock sources.

The learned LUT content is shown in Fig. 21. It closely matches the simulated V2T transfer curve. The discrepancies between the two curves are mainly attributed to the PVT variations and the random mismatches among the TDC delay cells.

The measured prototype performance is summarized in Table I and compared with a few state-of-the-art works. With competitive speed and SNDR, this paper achieves the lowest power consumption and the best Walden figure-of-merit (FoM). It also occupies the smallest silicon area, making it suitable for SoC integrations.

VI. CONCLUSION

A 24-GS/s, 6-b, 16-way voltage-time hybrid interleaved SAR ADC is reported. The key techniques to achieve outstanding power efficiency and compact size include 1) a two-step voltage-time hybrid SAR architecture exploiting the comparator resolving time for residue transfer without additional effort; 2) a reference dither technique for timing skew estimation; and 3) a reference-buffer-free CDAC topology to mitigate the reference crosstalk problem in TI-ADCs. Collectively, the advocated approaches and techniques yielded an unprecedented Walden FoM of 42-fJ/conversion-step at Nyquist for a 20 GS/s+ throughput, paving a viable path toward highly integrated, ADC-based wireline receivers with low-power consumption in the future.

REFERENCES

[1] *CEI-56G-LR-PAM4 Long Reach Implementation Agreement Draft Text*, Opt. Internetwork. Forum, 2015.
[2] D. Cui *et al.*, "A 320 mW 32 Gb/s 8-bit ADC-based PAM-4 analog front-end with programmable gain control and analog peaking in 28nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 58–59.
[3] Y. Frans *et al.*, "A 56Gb/s PAM4 wireline transceiver using a 32-way time-interleaved SAR ADC in 16nm FinFET," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2016, pp. 48–49.
[4] H. Yueksel *et al.*, "A 3.6pJ/b 56Gb/s 4-PAM receiver with 6-bit TI-SAR ADC and quarter-rate speculative 2-tap DFE in 32 nm CMOS," in *Proc. ESSCIRC*, Sep. 2015, pp. 148–151.
[5] I. Dedic, "56 GS/s ADC: Enabling 100GbE," in *Proc. Opt. Fiber Commun. Nat. Fiber Eng. Conf. (OFC/NFOEC)*, Mar. 2010, pp. 1–3.
[6] V. H.-C. Chen and L. Pileggi, "A 69.5 mW 20 GS/s 6b time-interleaved ADC with embedded time-to-digital calibration in 32 nm CMOS SOI," *IEEE J. Solid State Circuits*, vol. 49, no. 12, pp. 2891–2901, Dec. 2014.
[7] S. Cai, E. Z. Tabasy, A. Shafik, S. Kiran, S. Hoyos, and S. Palermo, "A 25GS/s 6b TI binary search ADC with soft-decision selection in 65nm CMOS," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2015, pp. 158–159.
[8] L. Kull *et al.*, "A 90GS/s 8b 667mW 64× interleaved SAR ADC in 32nm digital SOI CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 378–379.
[9] L. Kull *et al.*, "A 110 mW 6 bit 36 GS/s interleaved SAR ADC for 100 GBE occupying 0.048 mm^2 in 32 nm SOI CMOS," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2014, pp. 89–92.
[10] Y. Duan and E. Alon, "A 12.8GS/s time-interleaved SAR ADC with 25GHz 3dB ERBW and 4.6b ENOB," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2013, pp. 1–4.
[11] S. L. Tual, P. N. Singh, C. Curis, and P. Dautriche, "A 20GHz-BW 6b 10GS/s 32mW time-interleaved SAR ADC with master T&H in 28nm UTBB FDSOI technology," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 382–383.
[12] Y. M. Greshishchev *et al.*, "A 40GS/s 6b ADC in 65nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2010, pp. 390–391.
[13] W. Liu and Y. Chiu, "Time-interleaved analog-to-digital conversion with online adaptive equalization," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 7, pp. 1384–1395, Jul. 2012.
[14] M. El-Chammas and B. Murmann, "A 12-GS/s 81-mW 5-bit time-interleaved flash ADC with background timing skew calibration," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 838–847, Apr. 2011.

[15] S. Lee, A. P. Chandrakasan, and H. S. Lee, "A 1 GS/s 10b 18.9 mW time-interleaved SAR ADC with background timing skew calibration," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2846–2856, Dec. 2014.
[16] D. Stepanovic and B. Nikolic, "A 2.8 GS/s 44.6 mW time-interleaved ADC achieving 50.9 dB SNDR and 3 dB effective resolution bandwidth of 1.5 GHz in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 971–982, Apr. 2013.
[17] B. Xu, Y. Zhou, and Y. Chiu, "A 23mW 24GS/s 6b time-interleaved hybrid two-step ADC in 28nm CMOS," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2016, pp. 202–203.
[18] C. C. Lee and M. P. Flynn, "A SAR-assisted two-stage pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 859–869, Apr. 2011.
[19] B. Wicht, T. Nirschl, and D. Schmitt-Landsiedel, "Yield and speed optimization of a latch-type voltage sense amplifier," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1148–1158, Jul. 2004.
[20] A. Shikata, R. Sekimoto, T. Kuroda, and H. Ishikuro, "A 0.5 V 1.1 MS/sec 6.3 fJ/conversion-step SAR-ADC with tri-level comparator in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 4, pp. 1022–1030, Apr. 2012.
[21] Y. S. Shu, "A 6b 3GS/s 11mW fully dynamic flash ADC in 40nm CMOS with reduced number of comparators," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2012, pp. 26–27.
[22] Y. Chiu, C. W. Tsang, B. Nikolic, and P. R. Gray, "Least mean square adaptive digital background calibration of pipelined analog-to-digital converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 1, pp. 38–46, Jan. 2004.
[23] C.-C. Huang, C.-Y. Wang, and J.-T. Wu, "A CMOS 6-bit 16-GS/s time-interleaved ADC using digital background calibration techniques," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 848–858, Apr. 2011.
[24] R. Kapusta, J. Shen, S. Decker, H. Li, E. Ibaragi, and H. Zhu, "A 14b 80 MS/s SAR ADC with 73.6 dB SNDR in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3059–3066, Dec. 2013.
[25] B. Malki, T. Yamamoto, B. Verbruggen, P. Wambacq, and J. Craninckx, "A 70 dB DR 10 b 0-to-80 MS/s current-integrating SAR ADC with adaptive dynamic range," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1173–1183, May 2014.
[26] J.-H. Tsai, Y.-J. Chen, M.-H. Shen, and P.-C. Huang, "A 1-V, 8b, 40 MS/s, 113 μW charge-recycling SAR ADC with a 14 μW asynchronous controller," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2011, pp. 264–265.
[27] S.-W. Chen and R. W. Broaderson, "A 6-b 600-MS/s 5.3-mW asynchronous ADC in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2669–2680, Dec. 2006.
[28] T. Kobayashi, K. Nogami, O. Watanabe, T. Shirotori, and Y. Fujimoto, "A current-mode latch sense amplifier and a static power saving input buffer for low-power architecture," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 1992, pp. 28–29.
[29] S. K. Lee, Y.-H. Seo, Y. Suh, H.-J. Park, and J.-Y. Sim, "A 1 GHz ADPLL with a 1.25 ps minimum-resolution sub-exponent TDC in 0.18 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2874–2881, Dec. 2010.
[30] L. Kull *et al.*, "A 35 mW 8 b 8.8 GS/s SAR ADC with low-power capacitive reference buffers in 32 nm digital SOI CMOS," in *Proc. IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2013, pp. 260–261.
[31] J. W. Jung and B. Razavi, "A 25-Gb/s 5-mW CMOS CDR/deserializer," *IEEE J. Solid-State Circuits*, vol. 48, no. 3, pp. 684–697, Mar. 2013.

Benwei Xu (S'13) received the B.S. degree in microelectronics from Shanghai Jiao Tong University, Shanghai, China, in 2011. He is currently pursuing the Ph.D. degree in electrical engineering with the University of Texas at Dallas, Richardson, TX, USA.

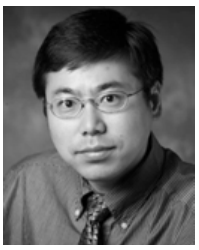
His current research interests include high-speed data convertor design and digital calibration techniques for data convertor.

Mr. Xu was a recipient of the ADI Outstanding Student Designer Award in 2013 and the TxACE Outstanding Student supplement in 2011.

Yuan Zhou (S'12) received the B.S. degree in electrical engineering from Tsinghua University, Beijing, China, in 2009, the M.S. degree from Columbia University, New York, NY, USA, in 2011, and the Ph.D. degree from the University of Texas at Dallas, Richardson, TX, USA, in 2016.

Since 2016, he has been with Broadcom Corporation, Irvine, CA, USA. His current research interests include high-speed SAR ADCs and digital calibration techniques for data convertors.

Dr. Zhou was a recipient of the ADI Outstanding Student Designer Award in 2012.



Yun Chiu (S'97–M'04–SM'10) received the B.S. degree in physics from the University of Science and Technology of China, Hefei, China, the M.S. degree in electrical engineering from the University of California at Los Angeles, Los Angeles, CA, USA, and the Ph.D. degree in electrical engineering and computer sciences from the University of California at Berkeley, Berkeley, CA.

He was a Senior Staff Member of a Silicon Valley startup company from 1997 to 1999, where he was involved in developing analog and mixed-mode circuits for CMOS digital imaging products. From 1999 to 2004, he was with the Berkeley Wireless Research Center, University of California at Berkeley, with a focus on low-power, low-voltage CMOS data converters. In 2004, he joined the Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Champaign, IL, USA, as an Assistant Professor, where he received the tenure offer in 2010. He is currently a Full Professor and the Erik Jonsson Distinguished Professor of the Department of Electrical Engineering with the University of Texas at Dallas, Richardson, TX, USA, where he directs the Analog and Mixed-Signal Laboratory, Texas Analog Center of Excellence.

Dr. Chiu received the Foreign Scholar Award at the University of California at Los Angeles, the Regents' Fellowship, the Intel Foundation Fellowship, the Cal View Teaching Fellow Award at Berkeley, and two awards from the Ministry of Education of China. He was also a co-recipient of the Jack Kilby Outstanding Student Paper Award from the 2004 International Solid-State Circuits Conference (ISSCC), the 46th ISSCC/DAC Student Design Contest Award in 2009, and the Best Regular Paper Award from the 2012 Custom Integrated Circuits Conference (CICC). He was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS from 2007 to 2009, and has served or is serving on the technical program committees of several IEEE Solid-State Circuits Conferences, including the CICC, the Asian Solid-State Circuits Conference, and the Symposium on VLSI Circuits.