A Wideband Noise-Canceling CMOS LNA With Enhanced Linearity by Using Complementary nMOS and pMOS Configurations

Benqing Guo, Jun Chen, Lei Li, Haiyan Jin, and Guoning Yang

***Abstract*— A complementary noise-canceling CMOS low-noise amplifier (LNA) with enhanced linearity is proposed. An active shunt feedback input stage offers input matching, while extended input matching bandwidth is acquired by a π-type matching network. The intrinsic noise cancellation mechanism maintains acceptable noise figure (NF) with reduced power consumption due to the current reuse principle. Multiple complementary nMOS and pMOS configurations commonly restrain nonlinear components in individual stage of the LNA. Complementary multigated transistor architecture is further employed to nullify the third-order distortion of noise-canceling stage and compensate the second-order nonlinearity of that. High third-order input intercept point (IIP3) is thus obtained, while the second-order input intercept point (IIP2) is guaranteed by differential operation. Implemented in a 0.18-μm CMOS process, the experimental results show that the proposed LNA provides a maximum gain of 17.5 dB and an input 1-dB compression point ($IP_{1\ dB}$) of −3 dBm. An NF of 2.9–3.5 dB and an IIP3 of 10.6–14.3 dBm are obtained from 0.1 to 2 GHz, respectively. The circuit core only draws 9.7 mA from a 2.2 V supply.**

***Index Terms*— Complementary configurations, current mirror (CM), derivative superposition, linearization, low-noise amplifier (LNA), multigated transistor (MGTR), noise cancellation, third-order input intercept point (IIP3).**

I. Introduction

THE noise figure (NF) of low-noise amplifiers (LNAs) is a key parameter since it determines the overall noise performance of receivers. In retrospect, a number of CMOS LNAs combining a wideband input match have been proposed. One of the efficient ways to achieve low noise is the thermal noise cancellation technique. In noise-canceling LNAs, wideband input matching, high gain, and low NF can be achieved simultaneously. Based on feed-forward noise cancellation principle, two fundamental noise cancellation topologies, including the main and auxiliary paths, are the resistive shunt feedback LNA and the common-gate (CG) and common-source (CS) LNA, respectively [1], [2]. As shown in Fig. 1(a), the resistive shunted transistor M_1 provides an input impedance matching,

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B. Guo, J. Chen, L. Li, and H. Jin are with the University of Electronic Science and Technology, Chengdu 611731, China (e-mail: rficgbq@gmail.com).

G. Yang is with Qualcomm Atheros Company, Ltd., Shanghai 201203, China.

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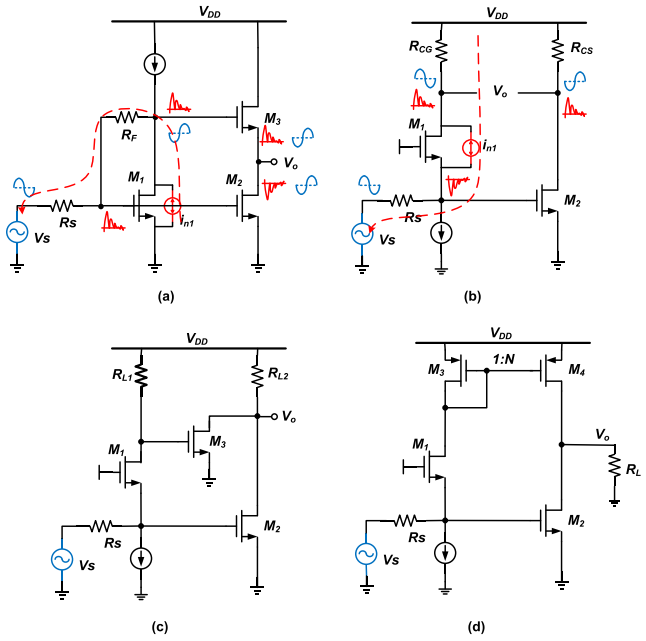


Fig. 1. Noise-canceling LNAs. (a) Resistive shunt feedback topology. (b) CG–CS topology. (c) Single-ended CG–CS topology. (d) CG–CS topology with CM combination network.

while the CS transistor M_2 serves as a voltage-sensing stage. The voltage source V_S induces two in-phase signals in superposition at the single output voltage node. The channel thermal noise current of M_1, i_{n1} flows along R_F and R_S path direction, and produces two in-phase net noise voltages. The two noise voltages are source followed and inverted, respectively, and reductively combined at output node due to off-phase polarity. Provided the transconductance of M_2 and M_3 and the values of the feedback resistance R_F and source resistor R_S are chosen properly, the noise of M_1 can be fully canceled. More interestingly, the distortion of M_1 can be canceled simultaneously. The CG–CS noise-canceling LNA is shown in Fig. 1(b) where the CG transistor M_1 as an input matching stage provides the impedance matching and the CS transistor M_2 serves as a noise-canceling stage. Its noise-canceling principle is quite similar to the former and not repeated again.

Several variants of the CG–CS noise-canceling LNA have been reported consecutively thereafter [3]–[8]. In contrast to Fig. 1(b), Fig. 1(c) adds the CS transistor M_3 to convert differential signals into single-ended output while using multiple inductors to resonate the parasitics of the LNA for

ultra-wideband applications [4]. Complementary CG input configuration is further adopted to reduce the second-order interaction and improve the linearity of the LNA [5]. To avoid undesirable distortions by the voltage–current conversion of M_3, a noise-canceling LNA based on current amplification is shown in Fig. 1(d), where the current mirror (CM) (M_3 and M_4) is used to combine the output signals of the CG stage and the CS stage directly in current mode [6], [7]. With a proper choice of the CM ratio N and the transconductance ratio of M_1/M_2, the noise and distortion currents of M_1 can be fully canceled. Inferior to inherent wideband input matching advantage of the CG–CS noise-canceling LNA, the CS input transistor in the resistive shunt-feedback noise-canceling LNA, necessities the additional feedback resistor R_F to provide low input resistance. Since the feedback resistor R_F contributes noise by itself, it makes the topology less attractive comparatively. Even so, this topology still gets evolved to multiple variants with updated techniques: a gain-enhanced unit is inserted into the main path to increase the overall gain and match the phase delay for two paths [9]. Distortions from the additional pMOS transistor and the nMOS one compensate with each other in the noise-canceling stage [10]. In [11] and [12], complementary configurations are commonly exploited to optimize the linearity and power consumption. In sum, although the distortion from the input match stage is canceled, there is still residual distortion component from the noise-cancellation stage, constructing limitation for high linearity. Besides the robustness of linearization in complementary configuration for process, voltage, and temperature variations is intensively investigated [13], some efforts have also been exerted to reduce the second-order distortion of the noise-canceling stage [7], [11]. But the IP3 improvement is limited due to the remained third-order distortion of that. In contrast, studies [8] and [10] cope with the latter but neglect the former. As a result, minimizing the distortion in the noise-canceling stage poses design challenges, which are addressed in this paper.

Extracted from Fig. 1, a macromodel of noise-canceling LNAs basically includes such three stages: an input matching stage, a noise-canceling stage, and an output stage. At main path direction, the input matching stage, whether the resistive feedback or CG–CS, assumes matched input impedance, while the noise by itself will flow along with two paths separately, and combine out of phase or in phase throughout output stage dependent on specific output port of single and differential style. The noise-canceling stage at auxiliary path with high input resistance just adds a transfer path for signal Vs and the noise from the main path, and normally consumes large current to inhibit its own noise contribution. Output stage may use resistive load or more linear CM load.

In this paper, we try to develop a noise-canceling LNA with CM load, incorporating active feedback input matching stage. Shown in Fig. 2 is the conceptional diagram of the possible LNA. With decreased supply voltage accompanying the scaling down of CMOS technology, the traditional RF circuit operating in voltage mode faces with more challenge of degenerated linearity due to limited voltage headroom. The RF circuit topology with CMs is expected

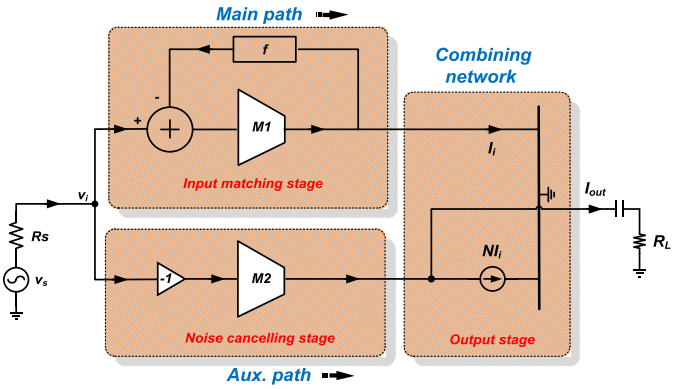


Fig. 2. Conceptional diagram of the proposed LNA.

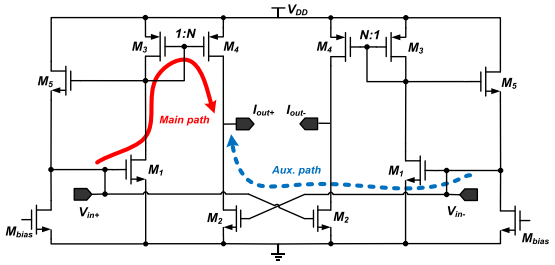


Fig. 3. Proposed basic differential noise-canceling LNA.

to outperform it by operating the signal in high dynamic current mode, where linearity is theoretically limited by power consumption instead of voltage supply. It has been reported that the RF front-end merging CMs demonstrate excellent performance in low-voltage supply scenario [14]. Similarly, the shunt feedback LNA combined with the CM combining network possibly also has a good performance potential. Based on this observation, a wideband noise-canceling amplifier is developed with enhanced linearity. A combination of complementary configurations and linearization by derivative superposition is used to mitigate both the second-order and third-order distortions. The theory and method are validated by the simulated and experimental results. Specifically, this paper is organized as follows. Section II details the proposed wideband LNA, including analysis for the major parameters. In Section III, experimental results are given and discussed to validate the theory. Finally, Section IV concludes this paper.

II. Proposed LNA Circuit

Shown in Fig. 3 is the proposed preliminary noise-canceling LNA schematic, consisting of a CS input stage (M_1) with active shunt feedback (M_5) and a CM (M_3 and M_4) in the main path, and a noise-canceling stage (M_2) in the auxiliary path. The CS input stage provides the input impedance matching by active shunt feedback and converts input voltage signal into current signal. The CM combination network combines the output currents of the main and auxiliary paths, avoiding the use of on-chip inductors and achieving a compact design. Moreover, current mode amplifying by factor N via the CM also enhances the transconductance of the main path, effectively reducing the noise contribution of the following stages. Medium threshold transistors ($V_{\text{th}} = 0.25$ V) are

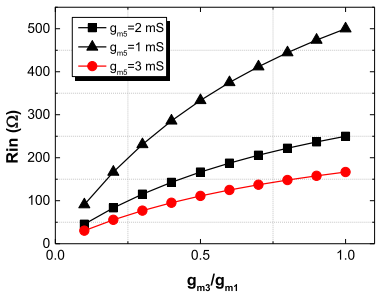


Fig. 4. Calculated input resistance R_{in} with respect to the variations of transconductance ratio, g_{m3}/g_{m1} under different values of g_{m5}.

utilized in the CMs to save more voltage headroom. The noise-canceling stage is for noise and distortion cancellation and further increases the transconductance of the circuit as well. A common-mode feedback circuit is to stabilize the dc output level around $V_{\text{DD}}/2$ by adaptively tuning the bias of M_2. The architecture is differential to avoid common-mode pickups and even-order distortion.

A. Impedance Matching and Gain

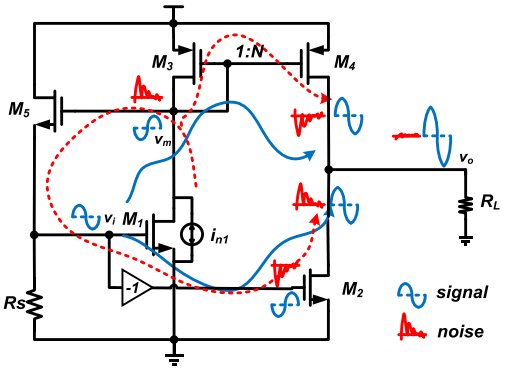
At low frequencies, the single-ended input resistance of the presented circuit in Fig. 3, R_{in} can be expressed as

$$R_{in} = \frac{1}{g_{m5}\left(1+\frac{g_{m1}}{g_{m3}}\right)} \tag{1}$$

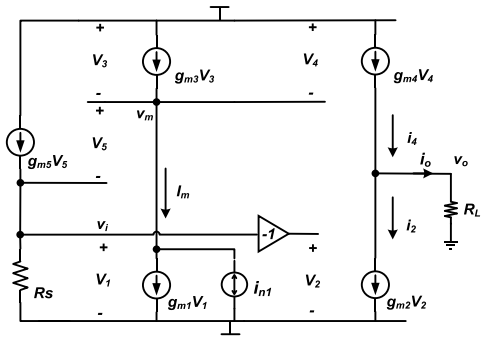
where parameters g_{m1}, g_{m3}, and g_{m5} are the small signal transconductance of transistors M_1, M_3, and M_5, respectively. The input impedance matching here is designed with active shunt feedback. It derives from the active resistive shunt feedback just by removing the feedback resistor R_F in [15, Fig. 7]. Under the determined input matching relationship, a smaller g_{m1} can be used with reduced bias current consumption in the CS input transistor, M_1.

Shown in Fig. 4 is the calculated single-ended R_{in} versus variations of transconductance ratio of $g_{\text{m3}}/g_{\text{m1}}$ with different values of g_{m5}. First, g_{m5} cannot be too large for low-noise design which soon can be seen in the Section II-B. Meanwhile, smaller g_{m3} can facilitate input matching, but the resulted high-resistance node at the drain of M_3 will reduce the headroom of the CS input transistor, degrading the linearity of the LNA. Particularly, an off-chip balun with the ratio of $1{:}(2)^{1/2}$ converts the 50-Ω single-ended resistance to 100 Ω differential one at the input port. And the resulted passive voltage gain partially inhibits the following noise contribution of the circuit [16]. In this paper, a slight impedance mismatch is introduced by setting R_{in} around 70 Ω. And a π-type matching network of off-chip components resonating with on-chip input equivalent parasitic capacitances can extend the input matching bandwidth of the circuit while maintaining in-band S_{11} below a certain level (typically -10 dB) with a higher R_{in} which will be shown in Section II-D.

For simplicity of the following analysis, only the equivalent left half of the differential circuit is concentrated on. As in Fig. 5(a), input signal v_i has two flow paths. In the main path, v_i is converted by M_1 into the signal current, and



(a)



(b)

Fig. 5. (a) Simplified single-ended diagram of noise-canceling LNA with signal and noise flow paths. (b) Equivalent single-ended small signal model for noise-canceling analysis.

further amplified by the CM, $M_{3,4}$ in current domain, resulting in one signal current output at output node v_o; in the auxiliary path, v_i is converted by M_2 into the other signal current output also appearing at the same output node. The two signal current outputs have the same polarity and thus are in superposition. Specifically, the small-signal gain is expressed as follows:

$$\text{Gain} = G_m R_L = (Ng_{m1}+g_{m2})R_L = 2N(g_{m1}+g_{\text{m3}})R_L \tag{2}$$

where parameter N denotes the scaling ratio of the CM and g_{m2} is the transconductance of M_2, while G_m and R_L characterize the equivalent transconductance and load resistor of the circuit. The simplification in (2) uses a noise-canceling condition which will be detailed in the soon later. It requires that the transconductance of M_2, g_{m2} takes

$$g_{m2} = N(g_{m1}+2g_{m3}). \tag{3}$$

Although meeting the equation hints an imbalance between Ng_{m1} and g_{m2}, one can see that the main and auxiliary paths intersect at single-ended output node, and then, the differential circuit still has a balanced gain.

B. Noise Analysis

The noise of M_1 also flows along two paths. As shown in Fig. 5(a), a portion of noise current i_{n1} is directly amplified by the CM, leading to a noise current output by the main path. Additionally, it produces a noise voltage at node v_m. The noise

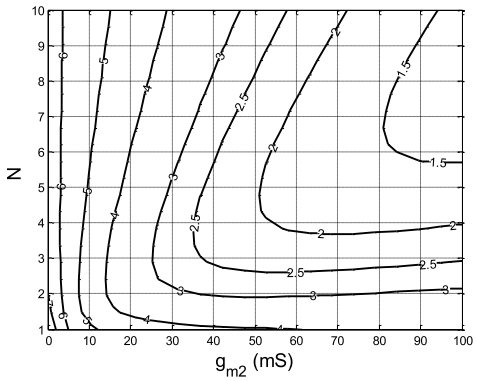


Fig. 6. Calculated NF contour with respect to the parameter variations of N and g_{m2} with $\gamma/\alpha = 0.9$, $g_{m3} = g_{m1}/4$, and $R_{\rm in} = 70\ \Omega$.

voltage is source followed to v_i node and further is converted into a noise current by M_2 in the auxiliary path. The two noise currents in both paths have the opposite polarity, and can cancel each other at the output node upon meeting the noise-canceling condition provided some electrical parameters of the circuit are properly designed. Fig. 5(b) shows the equivalent single-ended small signal model of the proposed LNA for noise-canceling analysis. To obtain null noise output from the single thermal noise source of M_1, i_{n1}, we have the following KCL relationships:

$$\begin{cases} \dfrac{v_1}{R_s} = g_{m5}v_5 \\ v_5 = v_m - v_1 \\ -g_{m3}v_m = g_{m1}v_1 + i_{n1} \\ -g_{m4}v_m + g_{m2}v_1 = 0. \end{cases} \tag{4}$$

Solving the equation yields the noise cancellation condition as in (3). Interestingly, the thermal noise source of M_3 follows the same noise-canceling procedure as described in (4), and produces no noise contribution in theory.

With thermal channel noise of MOSFETs only being considered for simplicity, the noise factor, F yields

$$\begin{aligned} F &= 1 + F_{M1} + F_{M2} + F_{M3} + F_{M4} + F_{M5} \\ &= 1 + \frac{\gamma}{\alpha}\frac{g_{m1}[N(g_{m1}+2g_{m3}) - g_{m2}]^2}{R_s G_m^2 (g_{m1}+g_{m3})^2} + \frac{4\gamma}{\alpha}\frac{g_{m2}}{R_s G_m^2} \\ &\quad + \frac{\gamma}{\alpha}\frac{g_{m3}[N(g_{m1}+2g_{m3}) - g_{m2}]^2}{R_s G_m^2 (g_{m1}+g_{m3})^2} + \frac{4\gamma}{\alpha}\frac{Ng_{m3}}{R_s G_m^2} + \frac{\gamma}{\alpha}R_s g_{m5} \end{aligned} \tag{5}$$

where F_{Mi} characterize the excess noise factor contributed by M_i (i takes 1–5, respectively). Parameters α and γ are bias-dependent parameters [17]. According to the equations, noise contributions from M_1 and M_3 can be canceled due to the aforementioned noise-canceling principle. With proper ratio factor N, noise contribution by M_4 can be better inhibited, while M_5 also contributes little noise output if a small transconductance is correspondingly designed. The remained main noise source still comes from M_2. To decrease the noise contribution of M_2, large transconductance of M_2 is of necessity.

To gain intuitional design insights into the relationship between parameters choosing and electrical performances, hand calculations and simulations are done. Fig. 6 shows the calculated NF contour with respect to parameter variations of N and g_{m2} with $\gamma/\alpha = 0.9$, $g_{m3} = g_{m1}/4$, and $R_{\rm in} = 70\ \Omega$. For a given NF, N and $g_{\rm m2}$ around the turnaround of the contour lead to the lowest power consumption. Fig. 7(a) shows the calculated NF by further varying the current mirroring ratio N and transconductance ratio of g_{m3}/g_{m1} upon meeting the noise-canceling condition, where $\gamma/\alpha = 0.9$ is assumed. Adopting the CM load network to combine the main path and the auxiliary path together, we can obtain high gain and low NF well below 3 dB by increasing N, in general, while the equivalent transconductance of the circuit is enhanced, too. Unfavorably, it coexists with the penalty of large current consumption or large transistor scaling size along with undesirable large parasitics. For the latter, as a rule of thumb, the limited bandwidth of such a CM is estimated by $f_T/(N+1)$, where f_T is the unit gain frequency of a CM transistor [18]. Moreover, a small g_{m3}/g_{m1} is preferred for low power. However, the impedance of the drain node v_m of M_3 will get larger in the case of a small g_{m3} being adopted, which goes against the low node impedance principle of current mode method in [14] and degrades the linearity of the main path. To achieve a balance between NF, gain, linearity, and power consumption, proper scaling ratio and transconductance ratio should be carefully selected. $N = 2.5$ and $g_{m3} = g_{m1}/4$ are finalized by Spectre-RF simulations. Shown in Fig. 7(b) is just the relative noise contribution by individual components in the proposed LNA of Fig. 3 with the optimized CM ratio and the transconductance ratio.

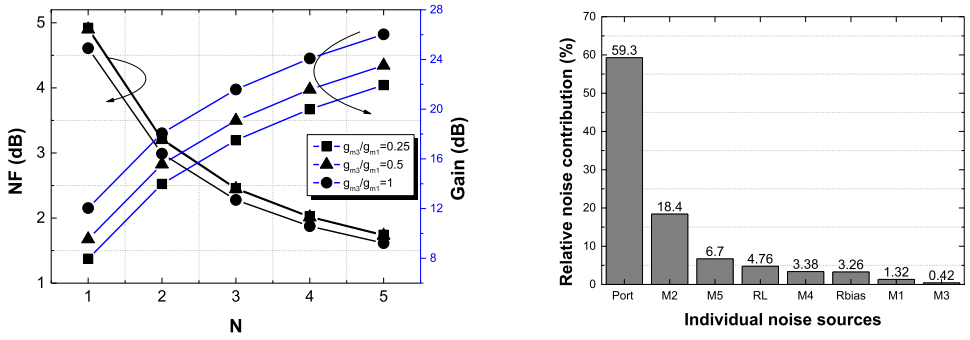
The noise factor of the LNA can be further rearranged as

$$\begin{aligned} F &= 1 + \frac{\gamma}{\alpha}\frac{g_{m1}(g_{m1}+2g_{m3})^2(1-m)^2}{R_s(g_{m1}+g_{m3})^2[g_{m1}+m(g_{m1}+2g_{m3})]^2} \\ &\quad + \frac{4\gamma}{\alpha}\frac{m(g_{m1}+2g_{m3})}{R_s N[g_{m1}+m(g_{m1}+2g_{m3})]^2} \\ &\quad + \frac{\gamma}{\alpha}\frac{g_{m3}(g_{m1}+2g_{m3})^2(1-m)^2}{R_s(g_{m1}+g_{m3})^2[g_{m1}+m(g_{m1}+2g_{m3})]^2} \\ &\quad + \frac{4\gamma}{\alpha}\frac{g_{m3}}{R_s N[g_{m1}+m(g_{m1}+2g_{m3})]^2} + \frac{\gamma}{\alpha}R_s g_{m5} \end{aligned} \tag{6}$$

with the noise-canceling coefficient (NCC), m defined as

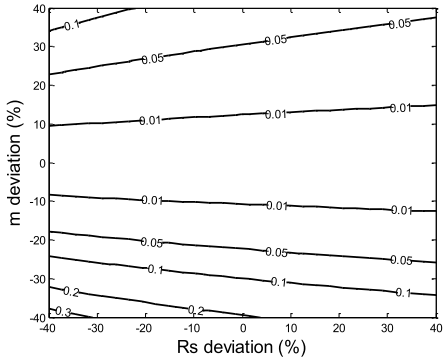
$$m = \frac{g_{m2}}{N(g_{m1}+2g_{m3})}. \tag{7}$$

It can be seen that (6) precisely collapses to (5) when m takes one. Fig. 8 shows the variations of excess noise factor of M_1 and M_3, $F_{M1\text{ and }M3}$ versus deviations of the source resistance, R_S and the NCC, m and noise factor variations of the LNA under the condition of $N = 2.5$ and $g_{m3} = g_{m1}/4$, $R_{\rm in} = 70\ \Omega$, and $\gamma/\alpha = 0.9$. As large as $\pm 20\%$ deviations of both R_s and m, lead to the $F_{M1\text{ and }M3}$ degrading about 0.05. Fig. 8(b) indicates that change as large as ± 30 % in m increases F_{M1} and F_{M3} in sum about 0.1. Thus, the noise-canceling process is insensitive to device parameter deviations. When m goes beyond one, F_{M2} and F_{M4} decrease, because the LNA has higher gain. As shown in Fig. 8(c), the total noise factor of the LNA becomes fairly flat in the region where NCC is larger than one, since the degree to which the $F_{M2} + F_{M4}$ is ameliorated compensates the degree to which

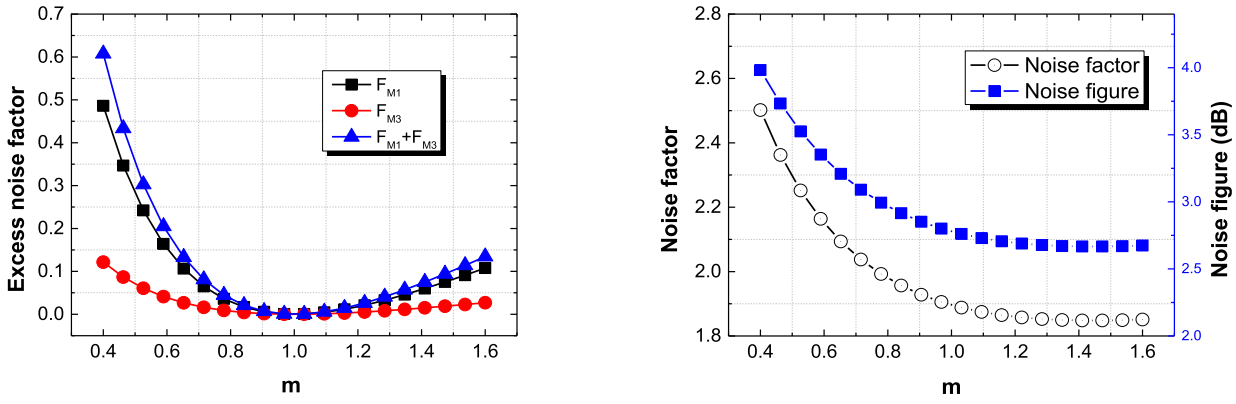


(a) (b)

Fig. 7. (a) Calculated NF and gain versus current mirroring ratio N and transconductance ratio g_{m3}/g_{m3}. (b) Simulated relative noise contributions by individual components in the proposed LNA.



(a)



(b) (c)

Fig. 8. (a) Variation of excess noise factor of M1 and M3, $F_{m1} + F_{m3}$, versus the deviations of R_s and m. (b) F_{m1} and F_{m3} with respect to the deviation of m. (c) Noise factor and NF with respect to the deviation of m.

$F_{M1} + F_{M3}$ is deteriorated. Because the NF is not minimized at $m = 1$, the optimized NF for the LNA can be fixed at m greater than one provided that power consumption constraint is met.

C. Linearity Analysis

Shown in Fig. 9 is the small signal equivalent model for nonlinearity analysis of the circuit, where the transconductance nonlinearity of devices is deemed as the main distortion source and the output conductance nonlinearity of that is ignored. Moreover, the memoryless Taylor series is applied to reduce the analysis complexity. Performing derivations as in the Appendix, we express the third-order input intercept point (IIP3) expression for the circuit in the following:

$$\text{IIP3} = \sqrt{\frac{4}{3}\left|\frac{B_1 a_1}{B_1 a_3 + 2(B_2 + 2g'_{m2})a_1 a_2 + B_3 a_1^3}\right|} \tag{8}$$

where parameters a_1–a_3 and B_1–B_3 are defined in the Appendix. Differential architecture of the LNA justifies that we can neglect (A23). But (A24) presents a more complicated nonlinearity characteristic. There are the third-order nonlinear cross items between $M_{2,4,5}$ and $M_{1,3}$, the third-order nonlinear

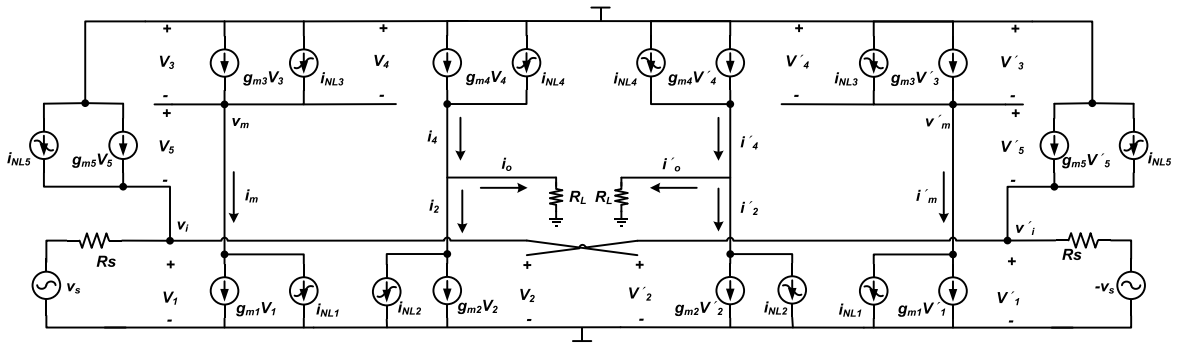


Fig. 9. Small signal equivalent model for the nonlinearity analysis of the circuit.

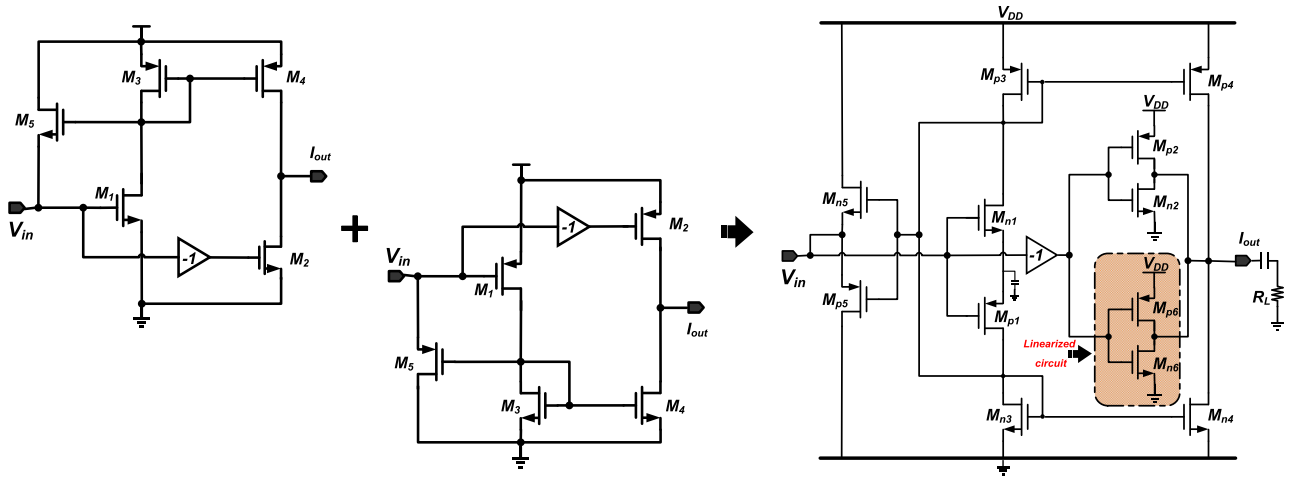
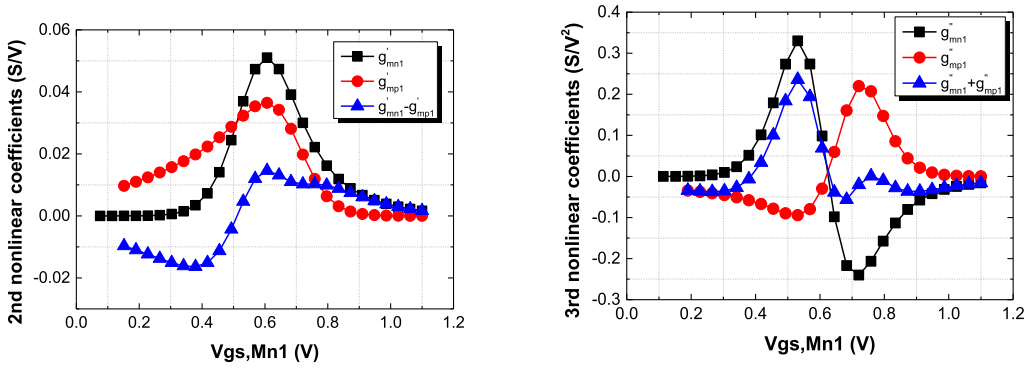


Fig. 10. Evolution from individual nMOS and pMOS architectures to stacked nMOS/pMOS configuration with linearized circuits (bias not shown).

cross items among $M_{2,4,5}$, and the third-order nonlinear items by M_2, M_4, and M_5 themselves but irrespective of that by $M_{1,3}$ due to the noise-canceling principle.

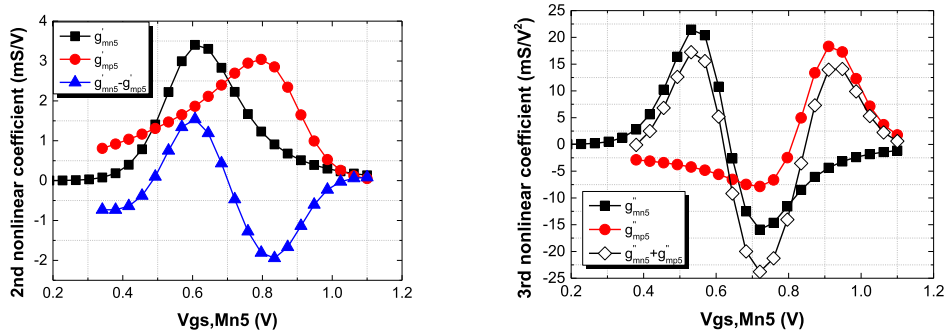
The multigated transistor (MGTR) [also named as derivation superposition (DS)] technique [19] can cancel the third-order nonlinearity around a linearized window by carefully designing the size and bias of an auxiliary transistor. To minimize power consumption, it is also desirable to bias the auxiliary transistor in weak-inversion region. The main drawback is that the combined second-order distortion coefficient is accumulated instead of impaired desirably. The accumulated second-order distortion coefficient then interacts with the parasitics distributed in the circuit, which inevitably constructs a limitation for IP3 at high frequencies (so-called second-order interaction in [20]). Modified DS with a rotated additional vector compensating the composite vector of the second-order and third-order nonlinear items is effective only for point frequency and not suitable for wideband applications [21]. On the other hand, for long channel devices obeying square law, complementary configurations theoretically nullify high-order distortions of circuits if complementary mismatch between the nMOS and pMOS device is neglected [22]. By using short channel I–V model, IP2 is optimized specifically for the stacked nMOS/pMOS circuit in submicrometer process in [7] and [23], but IP3 is yet to be improved efficiently. As in Fig. 10, the foregoing circuit is evolved to a stacked nMOS/pMOS configuration. Especially in the case of the complementary mismatch, the second-order distortion of a half circuit in Fig. 10 inevitably becomes nonzero, but this can be canceled in a differential configuration in our LNA. One point deserving attention is that the residual second-order distortion coefficient, $g_m^{'}$ due to the mismatch will affect IP3 as shown in the Appendix. CM biasing as shown later is thus used for the complementary configurations for $g_m^{'}$ minimization. Moreover, additional complementary transistors M_{n6} and M_{p6} using the MGTR technique are added to compensate the third-order distortion in the noise-canceling stage. The proposed circuit is then expected to outperform [7] with respect to IP3. In sum, the complementary configurations and MGTR technique are combined to cancel the third-order nonlinearity and reduce the second-order nonlinearity in the circuit simultaneously. Due to the symmetry of the circuit, complementary nMOS/pMOS transistors in Fig. 10 can be simply combined into composite transistors to simplify the following analysis. As shown in Fig. 10, M_i represents the combination of M_{ni} and M_{pi}, where i equals 1–6. Consequently, we have following relationship:

$$\begin{cases} g_{mi} = g_{mni} + g_{mpi} \\ g'_{mi} = g'_{mni} - g'_{mpi} \\ g''_{mi} = g''_{mni} + g''_{mpi} \end{cases} \tag{9}$$



(a) (b)

Fig. 11. (a) Second-order and (b) third-order nonlinear coefficients of stacked pMOS/nMOS CS input stage.



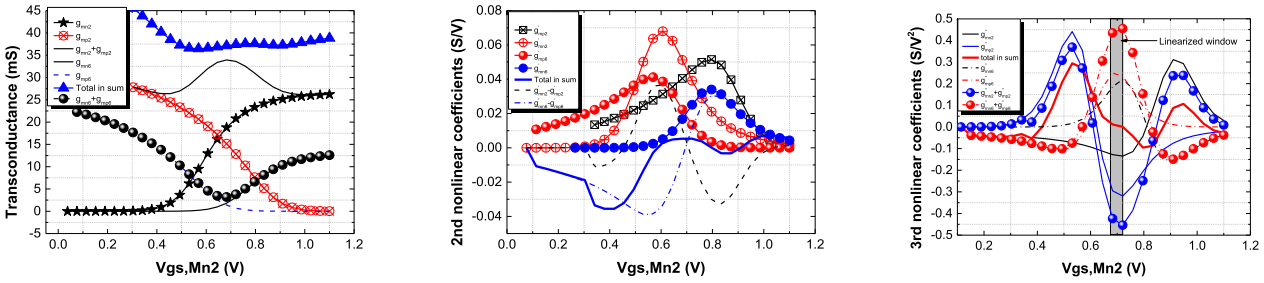
(a) (b)

Fig. 12. (a) Second-order and (b) third-order nonlinear coefficients of CSF stage.

where g_{mni}, g_{mpi}, and g_{mi} denote the transconductance of transistor M_{ni} and M_{pi}, and composite transistor M_i, respectively. g'_{mni}, g'_{mpi}, g'_{mi}, g''_{mni}, g''_{mpi}, and g''_{mi} are the first-order and second-order derivatives of the transconductance of transistor M_{ni} and M_{pi}, and the composite transistor M_i, respectively. By replacing (9) into (A24), the third-order nonlinear component for the complementary circuit in Fig. 10 can be approximately modeled.

By properly designing the size and bias of complementary circuits in the proposed circuit of Fig. 10, the second-order nonlinear components can be generally reduced. Demonstrated in Fig. 11 are the simulated nonlinear results of stacked pMOS–nMOS CS input stage where the horizontal axis is referred to the bias of M_{n1}. The second-order and third-order nonlinearity coefficients of CS input stage, $g'_{mn1} - g'_{mp1}$ and $g''_{mn1} + g''_{mp1}$ can be greatly attenuated when the optimized bias of CS input stage is designed just around the sweet spot, namely, $V_{\mathrm{gs},Mn1}$ taking 0.6 V. Of course, normally they cannot be canceled simultaneously due to high-order nonlinearity difference between submicrometer pMOS and nMOS devices. Similarly, shown in Fig. 13(a) are the simulated transconductance curves of the individual transistors of stacked pMOS–nMOS auxiliary stage and linearized stage where the horizontal axis is referred to the bias of M_{n2}, and their final combination. It can be seen that the combined g_m value is more linear than the individual's. Fig. 13(b) shows the transconductance derivative curves and desirable second-order distortion reduction effect. It is interesting that the combined $g'_{mn2} - g'_{mp2}$ have the opposite polarity and approximated amplitude with the combined $g'_{mn6} - g'_{mp6}$, making the second-order nonlinearity of the auxiliary stage negligible and leading the equivalent composite g'_{m2} nullified in (A24). Demonstrated in Fig. 12 are the simulated results of the complementary source follower (CSF) where the horizontal axis is referred to the bias of M_{n5}. The optimized bias of the CSF stage is designed by taking $V_{\mathrm{gs},Mn5}$ as 0.68 V, making the second nonlinearity can be greatly attenuated, too. Although it is not so flat with respect to the bias of device, the value as small as a factor of 10 compared with that of the CS input stage and auxiliary stage make its effect negligible.

Until now, all the items related to the second-order nonlinearity coefficients in (A24) can be neglected approximately thanks to multiple complementary figurations, and only the first two items related to the third-order nonlinearity coefficients remain. Specifically, as in Fig. 12, the bias of M_{n5} and M_{p5} is trimmed around the negative peak of their third-order nonlinear coefficients to cancel the residual third-order distortion components by M_{n4} and M_{p4}, $g''_{mn4} + g''_{mp4}$. Simulations indicate that, although biased with large overdrive voltage, M_{n4} and M_{p4} still contributes some third-order distortion, deteriorating the linearity. This is commonly neglected in previous studies with CMs [6]–[8]. Making the two nonlinear items related to g''_{m4} and g''_{m5} in (A24) compensate with each



(a) (b) (c)

Fig. 13. (a) Transconductance, (b) first-order, and (c) second-order derivatives of transconductance of complementary auxiliary stage and linearized stage.

other yields

$$g''_{m5} = \frac{g_{m1}^3}{NR_s(g_{m1}+g_{m3})^4} g''_{m4}. \tag{10}$$

The typical value for the circuit is $g''_{m5} = 0.3g''_{m4}$. Furthermore, Fig. 13(c) shows the third-order nonlinear coefficient superposition results of auxiliary stage and linearized stage. There is a linearized window around the bias of 0.7 V with the combined third-order nonlinear coefficients being equal to zero, corresponding to the equivalent g''_{m2} in (A24) being null. The optimized bias of M_{n2} is designed just taking $V_{\mathrm{gs},Mn2}$ as 0.7 V. At high frequencies, the second-order interaction, normally the product of g'_{mi} and frequency-dependent memory network functions can construct limitations for IP3 [20]. Thanks to the compensated g'_{mi}, IP3's dependency on the frequency is expected to be alleviated. In sum, high linearity is expected with the above-mentioned strategy applied to the circuit.

D. Bandwidth

There is parasitic effect mainly distributed at three nodes of Fig. 5. At input node v_i, parasitic capacitance C_{in} accounts for the gate-source capacitance of M_1, M_2, and M_5. Large parasitic capacitances deteriorate input matching at high frequencies. In the main path, the pole of node v_m constitutes a limitation for bandwidth. At output node v_o, C_L includes the following mixer input parasitic capacitance. First, the limitations by the parasitic capacitances of M_2 and M_4 at node v_o can be ignored, since the load resistance R_L is small enough. Typically taking $R_L = 100\ \Omega$, for example, C_L, modeling the input parasitic by the following mixers equals 0.5 pF. The resulted pole is located around 20 GHz. Thus toward the circuit in Fig. 10, the bandwidth of node v_i and v_m yields

$$\omega_i = \frac{1}{R_s(C_{\mathrm{gs}M1}+C_{\mathrm{gs}M2}+C_{\mathrm{gs}M5}+C_{\mathrm{gs}M6})} \tag{11}$$

$$\omega_m = \frac{g_{m3}}{C_{\mathrm{gs}M3}+C_{\mathrm{gs}M4}+C_{\mathrm{gd}M5}} \tag{12}$$

where $C_{\mathrm{gs}M1}$, $C_{\mathrm{gs}M2}$, $C_{\mathrm{gs}M3}$, $C_{\mathrm{gs}M4}$, and $C_{\mathrm{gs}M5}$ are the gate-source capacitance of equivalent composite transistors M_1–M_6, respectively. And $C_{\mathrm{gd}M5}$ is the gate-drain capacitance of the composite M_5. Simulations indicate that ω_i is smaller than ω_m. To cope with input matching degradation, a π-type network, including off-chip L_1, C_1, and internal parasitic C_{in} is designed. As in Fig. 14, effect of bondwire is also incorporated into this resonate network. C_1 stands for the parasitic capacitance of the testing board and extra matching capacitance, L_{bw} is the inductance of the bondwire, and R_{bw} denotes the parasitic resistance of the bondwire. R_{in} and C_{in} are the equivalent input resistance and capacitance of the LNA, respectively. As described in [34], to relieve the deteriorated input matching bandwidth due to the decreased input resistance Z_{in} via C_{in} when frequency is increased, the optimal R_{in} can take a higher value than exact 50 Ω in practice. The resulted S_{11} is −15.6 dB when R_{in} is fixed around 70 Ω. C_{in} extracted from simulations is about 1.4 pF. $L_{bw} = 1$ nH and $R_{bw} = 1\ \Omega$ are assumed. With this matching network, a broaden input matching bandwidth can be achieved than an original L-type (L_{bw} and C_{in}) network, as shown in Fig. 14. Besides S_{11} well below −10 dB at low-frequency band, the upper bound for S_{11} <−10 dB with L-type matching is 0.9 GHz, while it is 2 GHz with the π-type matching even under ±20% inductance variation. Thus, the proposed LNA is expected to have good input matching bandwidth. To alleviate the limitation by parasitic capacitance at node v_m, the neutralization technique is adopted to mitigate gain and bandwidth confliction [6], [24]. Specifically, cross-coupled capacitors $C_{\mathrm{ntr}1,2}$ are added between the input and the output of the CMs to extend the operation bandwidth by compensating the Miller capacitance effect.

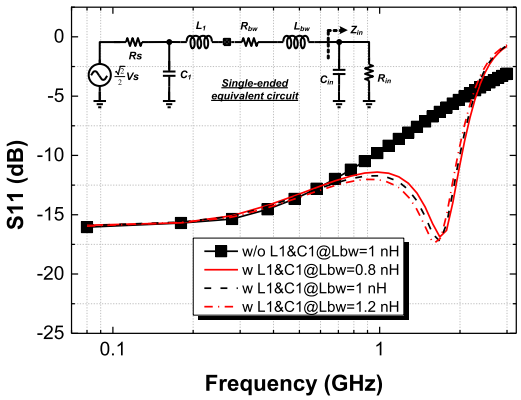


Fig. 14. Input matching versus the inductance (L_{bw}) variation of the bondwire.

III. Results and Discussion

A differential LNA has been fabricated in a 0.18-μm RF CMOS technology, by using the proposed complementary noise-canceling technique. By changing the CM ratio N

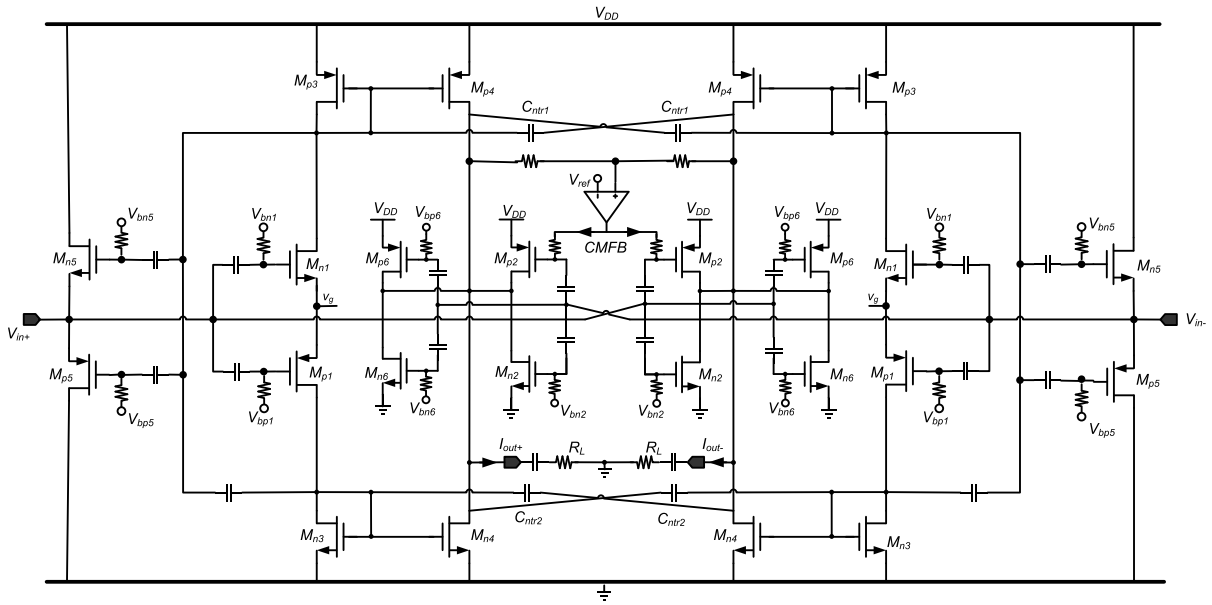


Fig. 15. Completed schematic of the proposed complementary noise-canceling LNA.

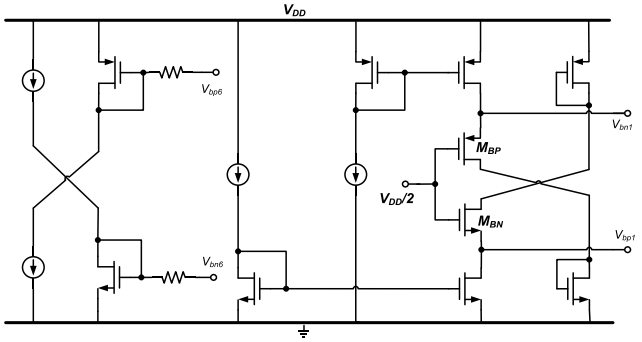


Fig. 16. Bias circuit for the proposed LNA.

TABLE I
DEVICE PARAMETERS FOR THE PROPOSED LNA

Transistors	W/L (μm/μm)	Transistors	W/L (μm/μm)
M_{n1}	30/0.18	M_{n2}	50/0.18
M_{p1}	60/0.18	M_{p2}	125/0.18
M_{n3}	10/0.3	M_{n4}	25/0.3
M_{p3}	10/0.25	M_{p4}	25/0.25
M_{n5}	2/0.18	M_{n6}	25/0.18
M_{p5}	6/0.18	M_{p6}	100/0.18

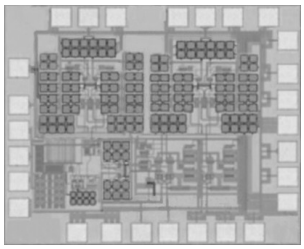
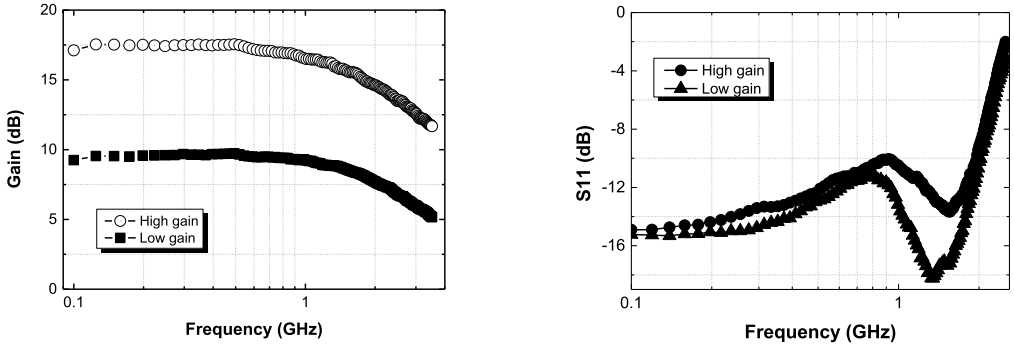


Fig. 17. Micrograph of the LNA.

and auxiliary transistors scaling size via the switch control, we can realize high- and low-gain modes of the LNA, to avoid possible saturation in the case of strong receiving signals. In addition, to minimize die size and add the circuit tuning flexibility, the matching components of inductor L_1 and capacitor C_1 are implemented by off-chip components. Fig. 15 shows the complete schematic view of the LNA, where a strong virtual ground v_g is formed by connecting the source terminals of differential transistors M_{n1} and M_{p1}. A CM-based bias circuit is employed to reduce the influence of process and temperature variation. As in Fig. 16, the applied voltage $V_{\rm DD}/2$ is source followed by $M_{\rm BN}$ and $M_{\rm BP}$ to produce V_{bn1} and V_{bp1}, fixing the source voltage of the CS input stage around middle of power supply, and a scaled version of the similar biasing scheme is used to bias the CSF [25]. The bias of the linearized circuit is correspondingly generated by the CMs in Fig. 16, and so is the bias of auxiliary transistor M_{n2}. The core component values of the circuit are tabulated in Table I. Fig. 17 shows the micrograph of the LNA with a size of 0.89×0.71 mm^2 including all pads. The LNA core consumes 9.7 mA and the supply voltage is 2.2 V to provide enough voltage headroom.

Fig. 18 shows the measured results for S_{21} and S_{11} parameters with high- and low-gain modes, respectively. The gain of the proposed LNA is 14.6–17.5 dB, covering the frequency range of 0.1–2 GHz for high-gain mode, and about 9.5 dB in maximum for low-gain mode. The upper bound frequency of high-gain mode where $S_{11} < -10$ dB is 2 GHz thanks to the π-type matching network. The S_{11} level is slightly improved at low-gain mode. The phenomenon can be ascribed to the decreased parasitic by enabling switch control to reduce the CM ratio N and transconductance of auxiliary stage. As in Fig. 19, the minimum NF value is 2.9 dB located at 0.9 GHz, while the average NF value is about 3 dB. The NF for high-gain mode is smaller than 3.5 dB across the



(a) (b)

Fig. 18. Measured (a) S_{21} and (b) $S_{11}$with high- and low-gain modes.

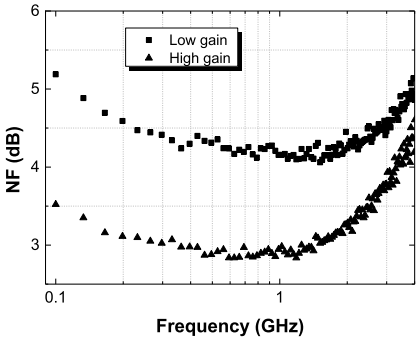


Fig. 19. Measured NF with high- and low-gain modes.

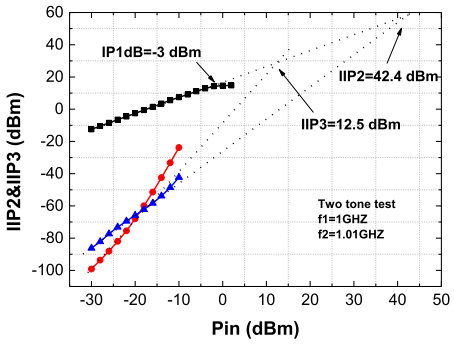


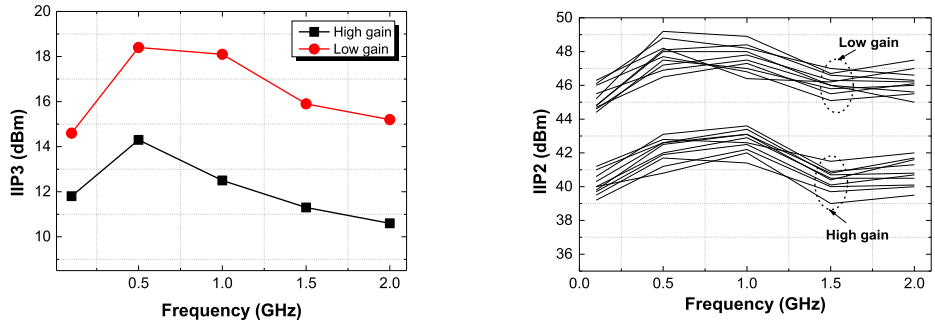
Fig. 20. Measured IIP3 and IIP2 of the proposed LNA.

passband. The NF for low-gain mode is higher than that for high-gain mode only by about 1.2 dB due to the down-scaled CM factor N and transconductance of auxiliary stage. This NF result with low-gain mode is better than that in [7], where the inverter-configured auxiliary stage with a tunable feedback resistor approximately has the input resistance of $1/g_m$, since the input resistance of the voltage-sensing stage in common noise-canceling LNAs must be high enough not to degrade the noise canceling of input matching stage.

A two-tone test at 1 GHz with a 10-MHz tone separation indicates an IIP3 of 12.5 dBm, while a single-tone test at 1 GHz indicates an IP_{1dB} of -3 dBm, which are shown in Fig. 20. The IIP3 characteristic of the proposed LNA across the passband was also examined with 10-MHz frequency spacing at five different frequency points: 0.1, 0.5, 1, 1.5, and 2 GHz, respectively. As shown in Fig. 21(a), the IIP3 in maximum with high-gain mode is 14.3 dBm, and the minimum of IIP3 is 10.5 at 2 GHz; the IIP3 with low-gain mode has improvement as high as 3–4 dB over that with high-gain mode. Note that the IIP3 decreases as the working frequency increases, which possibly can be explained by parasitic capacitances in the circuit. As the frequency increases, the parasitic capacitances cause prominent unbalance phase shift between the main and auxiliary paths. It makes that the distortion cancellation condition under low frequency is not well satisfied any more, degrading the IIP3 as a result. Moreover, a 50-MHz separated two-tone input test is performed for IIP2 measurement with multiple samples. Since the sum of two tones is beyond the passband at 1.5 and 2 GHz, the difference of two tones is measured as the IMD2 component and two tone spacing at the moment takes 100 MHz to ensure the corresponding IMD2 component falling in the low side passband. Fig. 21(b) shows the measured IIP2 over ten samples. Under high-gain mode, it ranges from 39 dBm in the worst case to 43.6 dBm in the best case across the bandwidth. These results confirm the effectiveness of the proposed linearization technique over wide frequency range.

To check the sensitivity of IIP3 to two-tone spacing, IIP3 was also measured by fixing one input tone at one frequency point, while the offset frequency of the other input tone is varied from 10 to 100 MHz, correspondingly. Fig. 22 shows the IIP3 results of the proposed LNA for high-gain mode at 0.1, 1, and 2 GHz, respectively. The IIP3 results show small dependency on the offset frequency with the variation of IIP3 is not more than 3 dB, over the entire range of offset frequencies. Fig. 23 shows the simulated IIP3 and input 1-dB compress point (IP1dB) of the proposed LNA at 500 MHz with respect to the bias voltage of M_{n2}. With reduced $V_{gs,Mn2}$, the inverter-configured auxiliary stage starts to deviate from class-A amplification and enter into class-AB operation with expanded gain, which improves IP1dB but degrades IIP3 as in Fig. 23. Thus, a compromise has to be done between them and the optimized bias for high IIP3 is preferred in this paper.

Fig. 24 shows the simulated NF and IIP3 performance of the proposed LNA at 100 MHz and 1 GHz for temperature



(a) (b)

Fig. 21. Measured (a) IIP3 and (b) IIP2 of the LNA across the passband.

TABLE II

PERFORMANCE SUMMARIES OF THE PROPOSED LNA AND COMPARISON WITH PREVIOUSLY REPORTED WIDEBAND LNAS

Parameter	Bandwidth (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	IIP2 (dBm)	Supply (V)	Power (mW)	Type/ NO. of inductors	Active Area (mm^2)	CMOS (nm)
Noise cancelling LNAs										
[2]	0.2~5.2	15.6	2.9~3.5	0~4	20~22	1.2	21	S[a]/0	0.01	65
[5]	0.8~2.1	14.5	2.5~2.8	16*[e]	N/A	1.5	17.4	S/0	0.1	130
[1]	0.2~1.6	14	1.9~2.4	0[e]	12[e]	2.5	35	S/0	0.075	250
[7]	0.048~1.2	14	2.9~3.2[d]	2.6~3.6[d]	40~45[d]	2.2	34.8	S/0	0.16	180
[9]	0.1~5.1	10.7	2.9~5.4	-6[e]	N/A	1	7	S/0	0.03	65
[11]	0.1~2.5	18	1.7~2.7	-3~0	18~21.5	1.2	13	D[b]/0	0.008	65
[12]	0.1~1.6	13	2.1~3.5	5.2~6	24.5~27	1.2	20.8	S/0	0.014	65
[8]	0.05~0.86	14.5	3 ~4.2	2.4~3	34~41	1.2	9.6	D/2	0.08	130
[10]	0.05~1	12.4	1.6~4	11.5~18	31~35	1.2	22.1	D/0	0.54**	130
[6]	0.02~1.2	20.5	3.1~4	2.7[e]	43[e]	1.8	32.4	D/2	0.12	180
T. W.	0.1~2	17.5	2.9~3.5[d]	10.6~14.3[d]	39~44[d]	2.2	21.3	D/2	0.63**	180
Resistive active feedback LNAs										
[24]	0.2~3.2	15.5	1.8~4.6	-9.5~-7	6~8	1.2	25	D/2	0.134	90
[15]	dc~6.5	16.5	2.7~3.5	-7~1	N/A	1.2	9.7	S/0	0.002	90
[27]	0.5~1.3	10	2.9~3.2	7.5[e]	12.5[e]	2	18	S/2	0.07	180
Resistive shunt feedback LNAs										
[28]	0.04~0.9	20.3	3.7~5	-10.8~-12.7	N/A	1.8	43.2	D/0	0.57	180
[29]	0.1~2.3	21	1.4~2	-1.5~-0.7	N/A	1.8	18	D/0	0.06	90
Other LNA architectures										
[30]	.32~1	23.5	2.2~2.7	-1~1	N/A	1.8	15.3	S/0	0.1	180
[31]	dc~1.4	16.4	3~4.7	-13.3~-9	N/A	1.8	12.8	S/D[c] /0	0.04	180

[a]S single-ended topology; [b]D differential topology; [c]S/D single-ended input to differential output; [d]maximal gain mode; [e]measured at point frequency

* two tone space:190MHz ** including pads

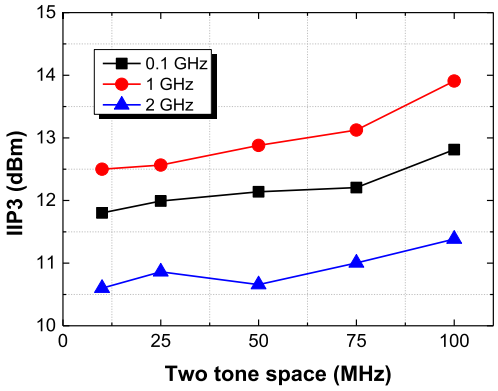


Fig. 22. Meausred IIP3 versus the two-tone separation.

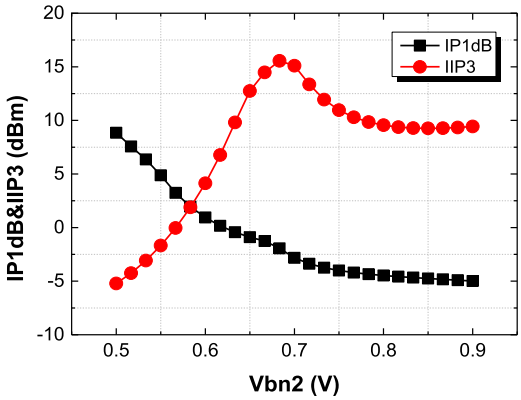
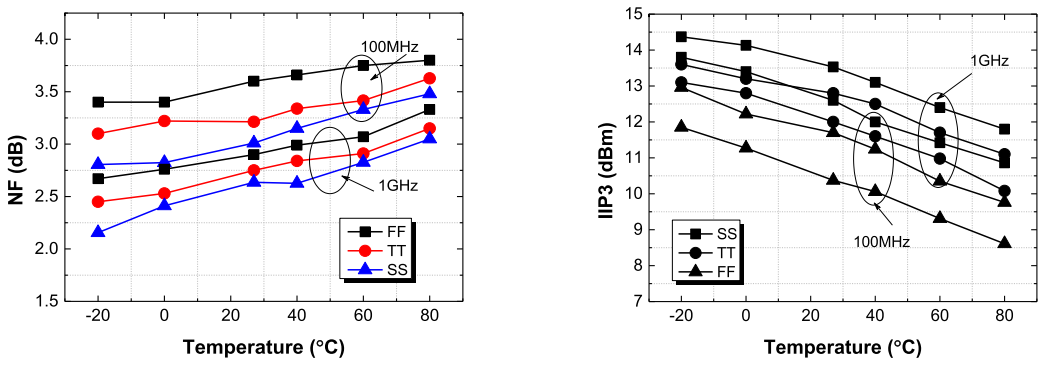


Fig. 23. Simulated IIP3 and IP1dB versus the bias of $V_{gs,Mn2}$ of the LNA.

and process variation, where process corner scenarios of the slow–slow (SS), typical–typical (TT), and fast–fast (FF) are specifically included and 10-MHz tone separation is used again for the IIP3 simulation. The NF degradation is below 0.6 dB compared with normal condition (TT and 27 °C) over all variations. And the NF is less than 4 dB in all cases as



(a) (b)

Fig. 24. Simulated process and temperature variations of (a) NF and (b) IIP3. TT, SS, and FF denote typical, slow, and fast model, respectively.

shown in Fig. 24(a). In the case of IIP3, more than 8.5 dBm of IIP3 can be obtained in the LNA irrespective of process and temperature variation as shown in Fig. 24(b). The IIP3 shows up to −3.4 and +1.8 dB of variations compared with the value of typical condition (TT, 27 °C) over the process and temperature variations. Thanks to the replica bias scheme, the variation of the linearity and noise performances is relatively small and robustness of the proposed circuit is manifested.

Table II summarizes the performances of the proposed LNA in comparison with other recently published LNAs. With moderate power consumption, a superior linearity of IIP3 is achieved over most of other reported LNAs. Particularly even in contrast to the singled-ended CG–CS topology using similar complementary CM figuration [7], our differential architecture not only maintains good IIP2 performance but also has power consumption and IIP3 advantage, thanks to the combined complementary configurations and MGTR technique to minimize the distortion in the noise-canceling stage. A comparable bandwidth is obtained at the cost of using off-chip inductors to resonate the increased parasitic capacitance by the CSF and linearized circuit. Although implemented without state-of-art process and occupying larger die area, the proposed LNA achieves enhanced linearity and comparable noise performance while consuming moderate power.

IV. Conclusion

A wideband LNA with CM combination network is proposed. Thanks to noise cancellation, acceptable NF is obtained with moderate power consumption, while input matching bandwidth is extended by employing a π-type matching network. Complementary nMOS and pMOS configurations commonly restrain nonlinear components in individual stage of the LNA. Complementary MGTR technique is further employed to linearize the noise-canceling stage. Enhanced IIP3 is thus obtained, while IIP2 is also guaranteed by differential operation. The proposed LNA is fairly suitable for full-band mobile TV tuners [34] by covering the VHF of 174–245 MHz, UHF of 470–860 MHz, and L-band of 1452–1492 MHz and 1670–1675 MHz for individual mobile TV standards in different countries.

Appendix

To characterize the nonlinearity of the proposed circuit in Fig. 9, we first express the two input voltages v_i and v_i' as Taylor expansions of the differential signal voltages v_s and $-v_s$, respectively

$$v_i = a_1 v_s + a_2 v_s^2 + a_3 v_s^3 \tag{A1}$$

$$v_i' = -b_1 v_s + b_2 v_s^2 - b_3 v_s^3 \tag{A2}$$

where a_1–a_3 and b_1–b_3 are the linear gain, second-order, and third-order nonlinear coefficients, respectively. Later derivation indicates that b_1–b_3 are the same to a_1–a_3. Taylor expansions only consider up to the third-order nonlinear components for simplicity, and the following is the same unless other stated. Applying Kirchhoff's current law at v_i, v_i', and v_m nodes of the circuit in Fig. 9, respectively, we have

$$\frac{v_i - v_s}{R_s} = g_{m5}(v_m - v_i) + \frac{g_{m5}'}{2}(v_m - v_i)^2 + \frac{g_{m5}''}{6}(v_m - v_i)^3 \tag{A3}$$

$$\frac{v_i' + v_s}{R_s} = g_{m5}(v_m' - v_i') + \frac{g_{m5}'}{2}(v_m' - v_i')^2 + \frac{g_{m5}''}{6}(v_m' - v_i')^3 \tag{A4}$$

$$i_m = g_{m1} v_i + \frac{g_{m1}'}{2} v_i^2 + \frac{g_{m1}''}{6} v_i^3 \tag{A5}$$

$$i_m = g_{m3}(-v_m) + \frac{g_{m3}'}{2}(-v_m)^2 + \frac{g_{m3}''}{6}(-v_m)^3 \tag{A6}$$

where g_{mi}, g_{mi}', and g_{mi}'' (i takes 1, 3, and 5) are the transconductance of M_1, M_3, and M_5, the first-order and second-order derivatives of that, respectively. Moreover, at output node v_o, we can have

$$i_2 = g_{m2} v_i' + \frac{g_{m2}'}{2} v_i'^2 + \frac{g_{m2}''}{6} v_i'^3 \tag{A7}$$

$$i_4 = g_{m4}(-v_m) + \frac{g_{m4}'}{2}(-v_m)^2 + \frac{g_{m4}''}{6}(-v_m)^3 \tag{A8}$$

$$i_o = i_4 - i_2 \tag{A9}$$

where g_{mi}, g_{mi}', and g_{mi}'' (i takes 2 and 4) are the transconductance of M_2 and M_4, the first-order and second-order derivatives of that, respectively. Parameters i_2, i_4, and i_o are the drain current of M_2 and M_4, and output current. Then, (A6) is further rearranged as follows:

$$v_m = h_1 i_m + h_2 i_m^2 + h_3 i_m^3 \tag{A10}$$

where

$$h_1 = -\frac{1}{g_{m3}}, \quad h_2 = \frac{g_{m3}'}{2g_{m3}^3}, \quad h_3 = \frac{g_{m3}''}{6g_{m3}^4} - \frac{g_{m3}'^2}{2g_{m3}^5}. \tag{A11}$$

On the other hand, substituting (A5) into (A10) leads to the following equation:

$$v_m - v_i = (A_1 - 1)v_i + A_2 v_i^2 + A_3 v_i^3 \tag{A12}$$

where

$$A_1 = h_1 g_{m1}, \quad A_2 = \frac{1}{2}h_1 g'_{m1} + h_2 g_{m1}^2$$
$$A_3 = \frac{1}{6}h_1 g''_{m1} + h_2 g_{m1} g'_{m1} + h_3 g_{m1}^3. \tag{A13}$$

Due to the symmetry of the circuit, parameters v'_m and v'_i also follow:

$$v'_m - v'_i = (A_1 - 1)v'_i + A_2 v_i'^2 + A_3 v_i'^3. \tag{A14}$$

Further substituting (A1), (A2), (A7), (A8), and (A12) into (A9), we express the output current i_o as the nonlinear function of input signal v_s

$$i_o = B_1 a_1 v_s + \left[(B_1 - 2g_{m2})a_2 + B_2 a_1^2\right]v_s^2 + \left[B_1 a_3 + 2(B_2 + 2g'_{m2})a_1 a_2 + B_3 a_1^3\right]v_s^3 \tag{A15}$$

where

$$B_1 = -g_{m4}A_1 + g_{m2}, \quad B_2 = -g_{m4}A_2 + \frac{1}{2}g'_{m4}A_1^2 - \frac{1}{2}g'_{m2}$$
$$B_3 = -g_{m4}A_3 + g'_{m4}A_1 A_2 - \frac{1}{6}g''_{m4}A_1^3 + \frac{1}{6}g''_{m2}. \tag{A16}$$

Similarly, solving Kirchhoff's equations at the output node v'_o yields

$$i'_o = -B_1 a_1 v_s + \left[(B_1 - 2g_{m2})a_2 + B_2 a_1^2\right]v_s^2 - \left[B_1 a_3 + 2(B_2 + 2g'_{m2})a_1 a_2 + B_3 a_1^3\right]v_s^3. \tag{A17}$$

So, we can have the differential output $i_{o,\text{diff}} = \left(i_o - i'_o\right)/2$ with the canceled second-order distortion. Then, the IIP3 expression is

$$\text{IIP3} = \sqrt{\frac{4}{3}\left|\frac{B_1 a_1}{B_1 a_3 + 2(B_2 + 2g'_{m2})a_1 a_2 + B_3 a_1^3}\right|}. \tag{A18}$$

We also need to find a_1–a_3 to completely characterize the LNA nonlinearity as in the above-mentioned equations. Then, replacing (A12) into (A3), we have the following equation:

$$\frac{-v_s}{R_s} = C_1 v_i + C_2 v_i^2 + C_3 v_i^3 \tag{A19}$$

where

$$\begin{cases} C_1 = -\dfrac{1}{R_s} + g_{m5}(A_1 - 1) \\ C_2 = g_{m5}A_2 + \dfrac{1}{2}g'_{m5}(A_1 - 1)^2 \\ C_3 = g_{m5}A_3 + g'_{m5}(A_1 - 1)A_2 + \dfrac{1}{6}g''_{m5}(A_1 - 1)^3. \end{cases} \tag{A20}$$

Further replacing (A1) into (A19) and rearranging the equation, we apply the method of undetermined coefficients to the left-hand and right-hand sides of the equation, where all items are with the only independent variable v_s. The obtained a_1–a_3 are shown in the following:

$$a_1 = \frac{-1}{R_s C_1}, \quad a_2 = \frac{-C_2}{R_s^2 C_1^3}, \quad a_3 = \frac{-2C_2^2}{R_s^3 C_1^5} + \frac{C_3}{R_s^3 C_1^4}. \tag{A21}$$

Similarly, solving the combination of (A2), (A4), and (A14) indicates that b_1–b_3 are the same to a_1–a_3, respectively. Finally, replacing (A21) into (A15), we have

$$B_1 a_1 = N(g_{m1} + g_{\text{m3}}) \tag{A22}$$

$$(B_1 - 2g_{m2})a_2 + B_2 a_1^2 = -\frac{N}{8}\frac{g_{m1} + 2g_{m3}}{g_{m1} + g_{m3}}\left[-g'_{m1} + \left(\frac{g_{m1}}{g_{m3}}\right)^2 g'_{m3}\right] + \frac{1}{8}\left[\left(\frac{g_{m1}}{g_{m3}}\right)^2 g'_{m4} - g'_{m2}\right] - \frac{N g_{m3} R_s}{8}\left(\frac{g_{m1}}{g_{m3}} + 1\right)^2 g'_{m5} \tag{A23}$$

$$B_1 a_3 + 2(B_2 + 2g'_{m2})a_1 a_2 + B_3 a_1^3 = \frac{1}{48}\left[\left(\frac{g_{m1}}{g_{m3}}\right)^3 g''_{m4} + g''_{m2}\right] - \frac{R_s N g_{m3}}{48}\left(\frac{g_{m1}}{g_{m3}} + 1\right)^4 \times g''_{m5} + \frac{R_s}{32}\left(\frac{g_{m5}}{g_{m3}}\right)\left[-g'_{m1} + \left(\frac{g_{m1}}{g_{m3}}\right)^2 g'_{m3}\right] g'_{m2} + \frac{R_s}{32}\left(\left(\frac{g_{m1}}{g_{m3}}\right)^2 g'_{m4} + g'_{m2}\right)\left(\frac{g_{m1}}{g_{m3}} + 1\right)^2 g'_{m5} - \frac{1}{32}\left(\frac{g_{m1}}{g_{m3}^2}\right)\left(\frac{g_{m1}+2g_{m3}}{g_{m1}+g_{m3}}\right)\left[-g'_{m1} + \left(\frac{g_{m1}}{g_{m3}}\right)^2 g'_{m3}\right] \times g'_{m4} - \frac{R_s N}{32}\left(\frac{g_{m1}}{g_{m3}} + 1\right)^2 \left[-g'_{m1} + \left(\frac{g_{m1}}{g_{m3}}\right)^2 g'_{m3}\right] \times g'_{m5} + \frac{R_s^2 N g_{m3}}{32}\left(\frac{g_{m1}}{g_{m3}} + 1\right)^5 {g'_{m5}}^2. \tag{A24}$$

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Benqing Guo received the M.Sc. and Ph.D. degrees in electrical engineering from the University of Electronic Science and Technology of China, Chengdu, China, in 2005 and 2011, respectively.

He had several years' industry experience of hardware circuit's development. He is currently a Researcher with the University of Electronic Science and Technology of China. His current research interests include RF/analog integrated circuits and techniques.

Dr. Guo served as a Technical Reviewer for over 15 international journals and conferences, including the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION, and the IEEE International Symposium on Circuits and Systems.

Jun Chen received the B.S. degree in communication engineering from the University of Electronic Science and Technology of China, Chengdu, China, in 2011, where he is currently pursuing the Ph.D. degree.

His current research interests include wireless transceiver front-end and low-phase noise frequency synthesizer.

Lei Li, photograph and biography are not available at the time of publication.

Haiyan Jin, photograph and biography are not available at the time of publication.

Guoning Yang, photograph and biography are not available at the time of publication.