

A Non-Interleaved 12-b 330-MS/s Pipelined-SAR ADC With PVT-Stabilized Dynamic Amplifier Achieving Sub-1-dB SNDR Variation

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Abstract—A process, voltage, and temperature (PVT)-stabilized dynamic amplification technique is reported for the pipelined-successive-approximation-register (SAR) analog-to-digital converter (ADC). A non-interleaved 12-b 330-MS/s pipelined-SAR ADC prototype employing such technique achieves 0.5- and 0.8-dB signal-to-noise plus distortion ratio (SNDR) variations for supply voltage varying from 1.25 to 1.35 V and temperature varying from -5°C to 85°C , respectively. The corresponding residue gain variations are 1.5% and 1.2% under the same conditions, respectively. Moreover, 2-b/cycle SAR architecture together with the attenuated passive residue transfer technique is employed to boost the prototype conversion throughput significantly. Noise analyses of the attenuated passive residue transfer process and of the PVT stabilization circuit are also furnished. At 330 MS/s, the 65-nm CMOS prototype achieves an SNDR of 63.5 dB and a Walden FoM of 15.4 fJ/conversion step for a near-Nyquist input.

Index Terms—2-b/cycle successive-approximation-register (SAR), analog-to-digital conversion, dynamic amplifier, passive residue transfer, pipelined SAR, process, voltage, and temperature (PVT) stabilization.

I. INTRODUCTION

THE great demand for high-speed digitization with low-power consumption has fueled the recent rapid developments of the successive-approximation-register (SAR) and pipelined-SAR analog-to-digital converters (ADCs) [1]–[8]. Aided by the pipeline process, the pipelined-SAR ADC breaks the speed limit of the conventional single-loop architecture while largely retaining its outstanding power efficiency. However, the need for residue amplification in a pipelined-SAR ADC makes the amplifier a critical building block that can potentially limit the overall performance of the converter. This is particularly true for the scenarios targeting high speed and high resolution, wherein the residue amplifiers usually consume significant amounts of power due to the stringent settling speed and accuracy requirements [3], [8].

The operational amplifier (opamp) depicted in Fig. 1 is the traditional approach to implement the residue amplifier for

Manuscript received May 1, 2017; revised June 27, 2017; accepted July 19, 2017. Date of publication August 24, 2017; date of current version November 21, 2017. This paper was approved by Guest Editor Seung-Tak Ryu. (*Corresponding author: Hongda Xu*)

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Digital Object Identifier 10.1109/JSSC.2017.2732731

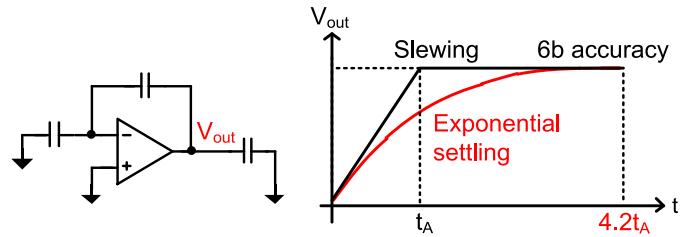


Fig. 1. Opamp-based residue amplifier and its settling curve during amplification phase.

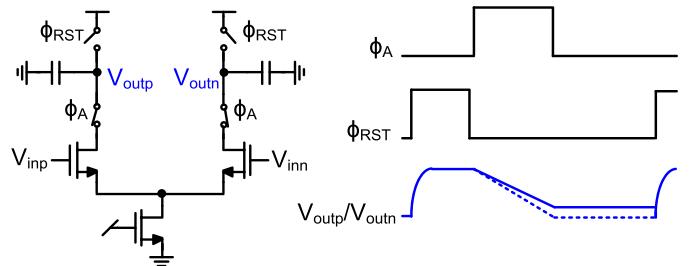


Fig. 2. Schematic and operation waveforms of open-loop dynamic amplifier.

pipelined-SAR ADCs. Unfortunately, as CMOS technology scales, high-performance opamp design becomes increasingly more difficult due to the decreasing supply voltage and the lower intrinsic gain of transistors. Although some techniques, such as gain boosting and multi-stage amplifier, can be used to mitigate the problem, these techniques often bring about considerable signal swing or speed penalties. The conventional exponential settling behavior of the opamp, while offering many benefits in accuracy, is also power inefficient. As shown in Fig. 1, for a 6-b settling accuracy, the required settling time of a non-slewing opamp is about four times longer than that of a constant-slewing amplifier. The comparator-based amplification is one technique to achieve constant slewing and its associated benefits [9]. The downside, however, is the finite delay of the comparator that introduces an overshoot problem, potentially degrading the settling accuracy of the amplifier.

The dynamic amplifier is another technique to achieve constant slewing behavior [10]–[13]. Fig. 2 illustrates the operation principle of an open-loop dynamic amplifier. First, in the reset phase, the outputs are pre-charged to the supply voltage. Then, triggered by the rising edge of the clock Φ_A , the outputs start to discharge with slew rates dependent on the inputs. Lastly, when the clock Φ_A turns low, the amplified

outputs are sampled by the load capacitors. Since there is no feedback applied, this amplifier does not suffer from the overshoot problem. Furthermore, the dynamic nature of this amplifier enables it to consume zero static current, leading to superior power efficiency.

Unfortunately, the advantages of the dynamic amplifier are accompanied by a few undesirable features, e.g., the process, voltage, and temperature (PVT), and clock jitter sensitivities. Particularly, the voltage gain of the amplifier can vary significantly across PVT variations, resulting in undesirable signal-to-noise ratio (SNR) loss of the ADC [10], [12]. The conventional way to compensate for the gain instability is to employ continuous background calibration [13]. Nevertheless, most of these calibrations require some constraints on the statistical property of the input signal or suffer from long convergence time [14], [15]. This work presents a simple analog approach to effectively stabilize the voltage gain over PVT variations [16]. The stabilization can also respond to environmental changes within one conversion cycle. Thus, it can achieve stable operation nearly instantly after power up, enabling its application in scenarios wherein the ADC startup time is important. In this paper, a 12-b 330-MS/s pipelined-SAR ADC employing the PVT-stabilized dynamic amplifier as the residue amplifier is presented. The prototype utilizes a 2-b/cycle first stage to resolve 8 bits, followed by a 1-b/cycle second stage. The 2-b/cycle conversion scheme in conjunction with the attenuated passive residue transfer technique significantly expedite the conversion process, while relaxing the gain, signal swing, and settling accuracy requirements of the residue amplifier. In this work, the inter-stage gain is set to 5 and the settling accuracy needs to be better than 6 bits for a nominal output residue swing of 95 mV_{pp}.

This paper is organized as follows. First, Section II presents the concept and implementation of the PVT stabilization technique. Second, the attenuated passive residue transfer technique is described and analyzed in Section III. Third, the prototype ADC design is covered in Section IV in detail, followed by the measurement results demonstrated in Section V. Lastly, Section VI concludes this paper.

II. PVT-STABILIZED DYNAMIC AMPLIFIER

A. Concept of PVT Stabilization

To clarify the issue of gain instability, the dynamic amplifier shown in Fig. 3 is modeled as an input-controlled current source charging or discharging a load capacitor. Based on this model, the voltage gain can be derived as

$$A_v = \frac{g_{mA}}{C_{LA}} \cdot t_A \quad (1)$$

where g_{mA} , C_{LA} , and t_A are the transconductance of the input transistor, the load capacitance, and the slewing time, respectively. Because all three quantities are non-constant over PVT variations, the gain in (1) can drift dramatically.

Although the absolute values of the transconductance and load capacitor vary significantly over PVT changes, the ratio between two capacitors or between two transconductances can be stable in monolithic forms due to matching. If the slewing

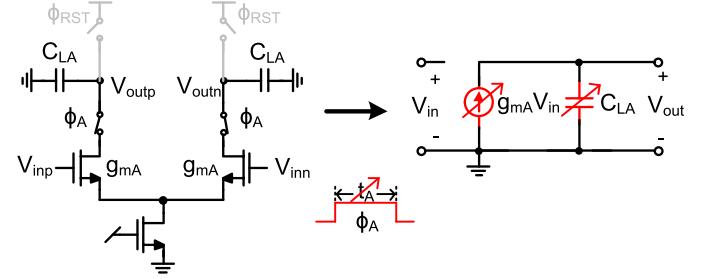


Fig. 3. Circuit model of open-loop dynamic amplifier.

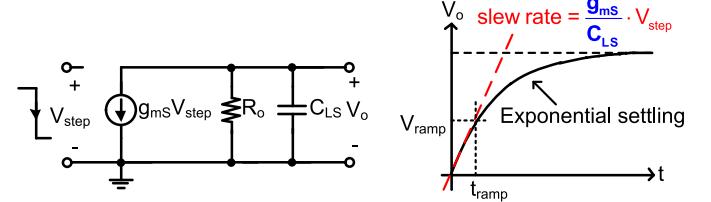


Fig. 4. Single-pole amplifier and its step response.

time t_A in (1) can be proportionally set to

$$t_A \propto \frac{C_{LS}}{g_{mS}} \quad (2)$$

where g_{mS} and C_{LS} are the transconductance and load capacitance of a replica single-pole amplifier, then the gain in (1) becomes the product of a few stable ratios

$$A_v \propto \frac{C_{LS}}{C_{LA}} \cdot \frac{g_{mA}}{g_{mS}}. \quad (3)$$

So, the key point to achieve gain stabilization is to relate the slewing time t_A to C_{LS}/g_{mS} .

Consider the single-pole replica amplifier shown in Fig. 4. When it is driven by a step input V_{step} , its output displays an exponential settling curve described by

$$V_o = V_{step} \cdot g_{mS} R_o \cdot (1 - e^{-t/\tau}). \quad (4)$$

With a Taylor-series expansion applied to (4), it becomes

$$\begin{aligned} V_o &\approx V_{step} \cdot g_{mS} R_o \cdot (t/\tau) \quad \text{for } t \ll \tau \\ &\approx V_{step} \cdot \frac{g_{mS}}{C_{LS}} \cdot t. \end{aligned} \quad (5)$$

It is interesting to note that the beginning part of the exponential curve can be well approximated by a ramp, whose slew rate contains the desired ratio of g_{mS}/C_{LS} . For the linear approximation to hold, the single-pole amplifier should not enter the slewing region and the amplitude of the differential step input is subject to [17]

$$V_{step} < 2\sqrt{2}V_{ov} \quad (6)$$

where V_{ov} is the overdrive voltage of the input differential pair. When a voltage-to-time (V2T) conversion is applied to this ramp signal, the objective slewing time t_{ramp} containing C_{LS}/g_{mS} can be obtained as

$$t_{ramp} = \frac{C_{LS}}{g_{mS}} \cdot \frac{V_{ramp}}{V_{step}} \quad (7)$$

where V_{ramp} is the threshold voltage of the V2T converter.

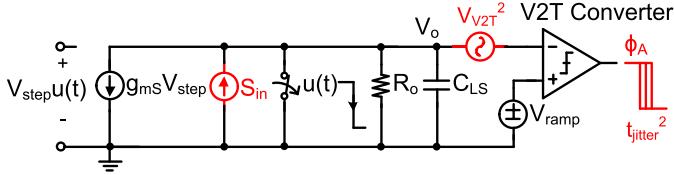


Fig. 5. Circuit model for the noise analysis of the PVT stabilization circuit.

Substituting (7) into (1), the gain expression for the conventional dynamic amplifier becomes the product of a capacitance ratio, a transconductance ratio, and a voltage ratio

$$A_v = \frac{C_{LS}}{C_{LA}} \cdot \frac{g_{mA}}{g_{mS}} \cdot \frac{V_{ramp}}{V_{step}}. \quad (8)$$

Assuming that V_{ramp} and V_{step} are generated from the same reference voltage, their ratio will remain constant. Since all these ratios are constant in monolithic forms, the gain of the dynamic amplifier with stabilization is expected to be constant over PVT variations.

B. Noise Analysis of PVT Stabilization Circuit

The objective of the PVT stabilization circuit illustrated in Fig. 5 is to generate a clock signal Φ_A to control the slewing time of the amplifier. As a consequence, any noise in the PVT stabilization circuit will cause jitter to Φ_A , and eventually gets converted to the output noise of the dynamic amplifier. The noise of PVT stabilization circuit consists of the noise current of the single-pole amplifier and the input-referred voltage noise of the V2T converter (see Fig. 5). Assuming that the noise of the single-pole amplifier is dominated by its input transistors, the power spectral density of the noise current S_{in} can be described as

$$S_{in} \approx 4kT\gamma g_{mS} \quad (9)$$

where γ is the MOSFET thermal noise factor. The output noise of the single-pole amplifier at the threshold crossing time t_{ramp} of the V2T converter can be expressed as

$$\overline{V_{on}^2} = \frac{2kT\gamma g_{mS}}{C_{LS}^2} t_{ramp}, \quad \text{for } t_{ramp} \ll \tau \quad (10)$$

which results from integrating the noise current onto the load capacitor C_{LS} [18]. This output noise and the input-referred noise of the V2T converter will perturb the time instant at which the threshold of the V2T converter is crossed and cause jitter to the resulting output clock. The variance of the induced jitter is

$$\begin{aligned} \overline{t_{jitter}^2} &= (\overline{V_{on}^2} + \overline{V_{V2T}^2}) \left| \frac{dV_o}{dt} \right|_{V_o=V_{ramp}}^{-2} \\ &= \frac{\overline{V_{on}^2} + \overline{V_{V2T}^2}}{\left(V_{step} \frac{g_{mS}}{C_{LS}} \right)^2}. \end{aligned} \quad (11)$$

According to (1), the output noise power of the dynamic amplifier due to this jitter can be calculated as

$$\overline{V_{oj}^2} = \left(\frac{g_{mA} V_{in}}{C_{LA}} \right)^2 \overline{t_{jitter}^2}. \quad (12)$$

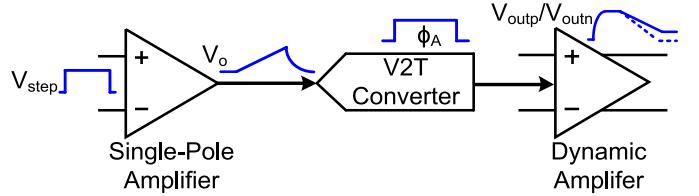


Fig. 6. Block diagram of PVT-stabilized dynamic amplifier.

And the input-referred noise due to the jitter can be written as

$$\overline{V_{inj}^2} = \frac{V_{in}^2}{t_{ramp}^2} \overline{t_{jitter}^2}. \quad (13)$$

Substituting (10) and (11) into (13), (13) becomes

$$\overline{V_{inj}^2} = \frac{V_{in}^2}{V_{step}^2} \left(\frac{2kT\gamma}{g_{mS} t_{ramp}} + \overline{V_{V2T}^2} \left(\frac{C_{LS}}{g_{mS} t_{ramp}} \right)^2 \right). \quad (14)$$

It is interesting to note that this jitter-induced noise decreases with an increasing value of V_{step} . For a larger V_{step} , the corresponding dc current integrating on the load capacitor is increased and it constitutes a relatively large portion of the total current charging the load capacitor, resulting in a cleaner ramp signal. However, V_{step} cannot be too large and its maximum value is restricted by (6) to ensure that the single-pole amplifier stays away from slewing. Usually, t_{ramp} is set by the speed spec of the dynamic amplifier; it should not be changed when someone tries to minimize the jitter-induced noise. When V_{step} is increased, V_{ramp} or C_{LS} should be increased proportionally [see (7)]. As an alternative, one can decrease this jitter-induced noise by increasing g_{mS} , which enlarges the power consumption of the single-pole amplifier. To ensure an unchanged t_{ramp} , V_{ramp} or C_{LS} should be increased as g_{mS} increases.

Simulation result shows that the rms jitter due to the single-pole amplifier and V2T converter described in the following section is around 7 ps. The jitter-induced noise is 9 nV², which contributes 45% of the total noise power of the PVT-stabilized dynamic amplifier. Regarding to this noise, the power consumption of the single-pole amplifier and that of V2T converters are 0.15 and 0.39 mW, respectively.

C. Implementation of PVT-Stabilized Dynamic Amplifier

Fig. 6 illustrates the block diagram of the PVT-stabilized dynamic amplifier consisting of a single-pole replica amplifier, a V2T converter, and a conventional dynamic amplifier. The single-pole amplifier is used to generate a ramp signal fed to the succeeding V2T converter, which extracts the desired time information to set the slewing time of the dynamic amplifier.

The circuit schematic of the single-pole amplifier is depicted in Fig. 7. The circuit operates as follows. First, in the reset phase, the output of the amplifier is reset by the voltage V_{bias} and the capacitors C_1 and C_2 sample the common-mode voltage. After the switches $S_1 - S_4$ turn off, the capacitors C_1 are switched to generate a step input, which drives the output

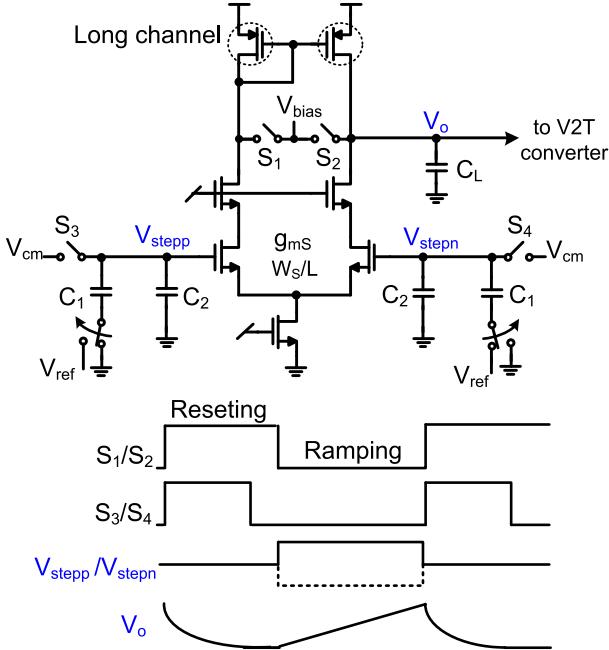


Fig. 7. Circuit schematic and timing diagram of the single-pole amplifier.

to ramp. The amplitude of the step input is defined as

$$V_{\text{step}} = V_{\text{stepp}} - V_{\text{stepn}} = \frac{C_1}{C_1 + C_2} \cdot 2V_{\text{ref}}. \quad (15)$$

The PVT stabilization technique is based on approximating an exponential curve by a ramp, which inherently contains approximation error. In order to minimize this error, the time constant of the single-pole amplifier should be much larger than t_{ramp} , dictating a large output resistance

$$R_o \gg \frac{1}{g_{\text{mS}}} \cdot \frac{V_{\text{ramp}}}{V_{\text{step}}}. \quad (16)$$

In this work, cascode NMOS transistors and long-channel PMOS transistors are employed to increase the output resistance.

Any offset voltage of the single-pole amplifier will modify the exact value of V_{step} and change the voltage gain. If this offset drifts over PVT variations, it will cause gain variations to the PVT-stabilized dynamic amplifier, that is

$$A_{v,\text{os}} = \frac{C_{\text{LS}}}{C_{\text{LA}}} \cdot \frac{g_{\text{mA}}}{g_{\text{mS}}} \cdot \frac{V_{\text{ramp}}}{V_{\text{step}} + V_{\text{os}}}. \quad (17)$$

Differentiating (17) with respect to V_{os} , we have

$$\frac{dA_{v,\text{os}}}{dV_{\text{os}}} = A_v \cdot \frac{-V_{\text{step}}}{(V_{\text{step}} + V_{\text{os}})^2}. \quad (18)$$

Equation (18) indicates that a large V_{step} (assuming $V_{\text{step}} > V_{\text{os}}$) helps to alleviate the gain variation due to the offset drift over ambient changes. In this work, a large V_{step} of 80 mV is chosen to minimize the impact of offset, which also helps to alleviate the jitter-induced noise according to the above analysis. Additionally, one can also apply offset cancellation to the single-pole amplifier to further mitigate this impact.

The V2T converter is implemented with cascaded inverters as shown in Fig. 8. To reject any potential pulselwidth

modulation due to the common-mode PVT variations, a pseudo-differential V2T converter is employed instead of a single-ended one. The V2T converter operates as follows. When the single-pole amplifier is resetting, switches S₁ and S₂ are off and the P-side and N-side V2T converters are disconnected from the single-pole amplifier. Meanwhile, switches S₃–S₈ turn on; the first-stage inverters in the V2T converters are configured in the auto-zeroing mode [19] and all capacitors in the V2T converters sample V_{bias} . After that the sampling switches S₃ and S₄ turn off and the bottom plates of C₃ and C₄ are switched from ground to the reference to add a fraction of V_{ref} to the summing nodes A and B. Once these nodes settle, the switches S₅–S₈ turn off and the threshold voltages of P-side and N-side V2T converters are set to V_{thp} and V_{thn} , respectively

$$V_{\text{thp}} = V_{\text{bias}} + \frac{C_3}{2C_{\text{tot}}} \cdot V_{\text{ref}} + V_{\text{osp}} \quad (19)$$

$$V_{\text{thn}} = V_{\text{bias}} + \frac{C_4}{2C_{\text{tot}}} \cdot V_{\text{ref}} + V_{\text{osn}} \quad (20)$$

where V_{osp} and V_{osn} are the residual offsets of the P-side and N-side V2T converters after auto zeroing, respectively.

When the single-pole amplifier is ramping, the switches S₁ and S₂ turn on and the P-side and N-side V2T converters are connecting to the single-pole amplifier. Once the ramp signal crosses the threshold voltage of the N-side V2T converter, the output clock Φ_A will turn high and the dynamic amplifier starts to discharge the load capacitor. When the ramp signal crosses the threshold voltage of the P-side V2T converter, the clock Φ_A falls and the dynamic amplifier stops discharging the load capacitor. Actually, the voltage difference between V_{thp} and V_{thn} defines the value of V_{ramp}

$$\begin{aligned} V_{\text{ramp}} &= V_{\text{thp}} - V_{\text{thn}} \\ &= \frac{C_3 - C_4}{2C_{\text{tot}}} \cdot V_{\text{ref}} + V_{\text{osp}} - V_{\text{osn}} \\ &\approx \frac{C_3 - C_4}{2C_{\text{tot}}} \cdot V_{\text{ref}}. \end{aligned} \quad (21)$$

It should be noted that the mismatch between V_{osp} and V_{osn} will modify the exact value of the voltage gain and degenerate the gain stability if this offset mismatch drifts over PVT changes. In this design, a large V_{ramp} of 150 mV is chosen to minimize this effect.

Fig. 9 shows the schematic of the dynamic amplifier, wherein cascode transistors are added to improve the linearity of the amplifier. Given that the input transistors of the single-pole amplifier and the dynamic amplifier are biased at the same transconductance-to-current ratio, the gain of the PVT-stabilized dynamic amplifier is eventually derived as the product of capacitor ratios and transistor size ratio

$$\begin{aligned} A_v &= \frac{C_{\text{LS}}}{C_{\text{LA}}} \cdot \frac{g_{\text{mA}}}{g_{\text{mS}}} \cdot \frac{V_{\text{ramp}}}{V_{\text{step}}} \\ &\approx \frac{C_{\text{LS}}}{C_{\text{LA}}} \cdot \frac{W_A}{W_S} \cdot \frac{(C_1 + C_2) \cdot (C_3 - C_4)}{4C_1 \cdot C_{\text{tot}}}. \end{aligned} \quad (22)$$

Considering that both the capacitor ratio and the transistor size ratio are stable over PVT variations; this voltage gain

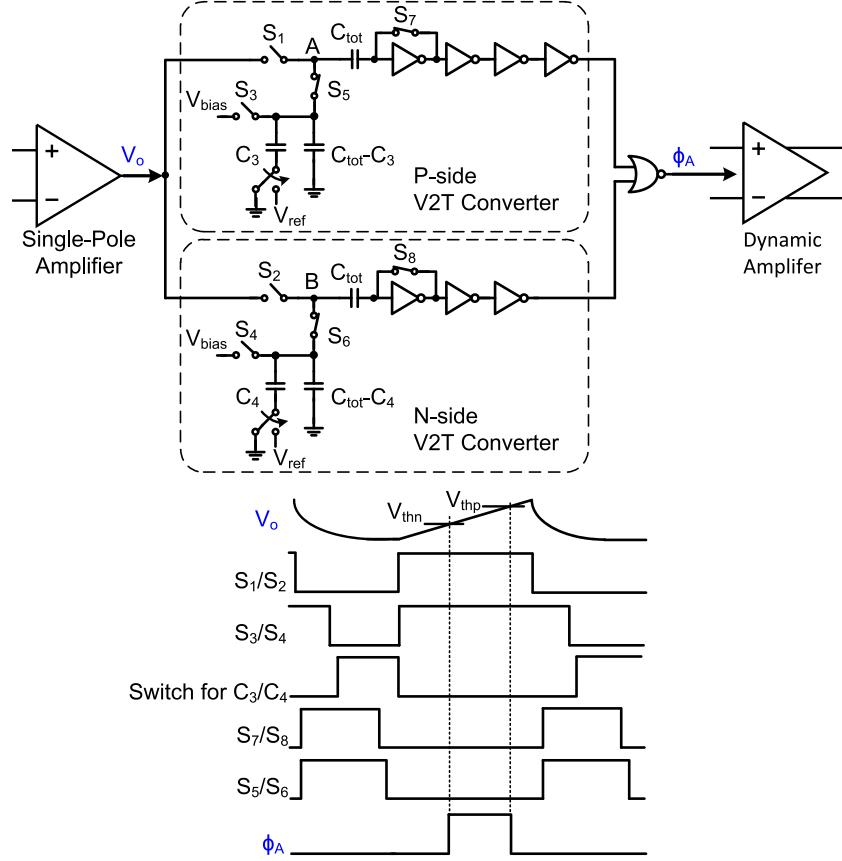


Fig. 8. Circuit schematic and timing diagram of the V2T converters.

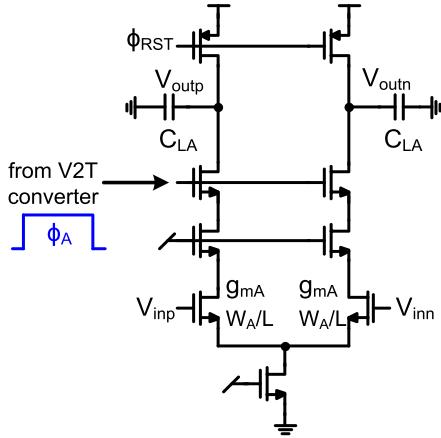
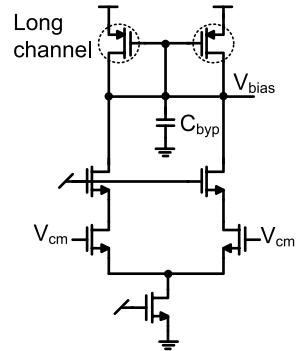


Fig. 9. Circuit schematic of the dynamic amplifier.

is expected to remain constant. Besides, the reference voltage V_{ref} is canceled from the voltage ratio V_{ramp}/V_{step} , implying that V_{ref} does not need to be set precisely.

From the previous narration, we know that the output of single-pole amplifier starts ramping from the voltage V_{bias} and the threshold voltages of the V2T converters are also set by V_{bias} [see (19) and (20)]. The threshold voltages of V2T converters can track the starting point of the ramp signal even though V_{bias} varies over PVT changes, indicating that

Fig. 10. Schematic of the replica circuit for generating the voltage V_{bias} .

V_{bias} does not need to be precisely set either. As shown in Fig. 10, the bias circuit for generating the voltage V_{bias} is just a replica circuit of the single-pole amplifier loaded with PMOS diodes. It is known that the output common-mode voltage of the residue amplifier affects the noise of the second-stage comparator. In this prototype, as the second-stage comparator only contributes a small amount of total noise (see Table I), the variation of the common-mode voltage has a limited effect on the overall conversion accuracy. As a result, no special technique is utilized to control the output common-mode voltage of the dynamic amplifier.

TABLE I
ADC NOISE BUDGET

Quantization Noise [nV ²]	kT/C Noise [nV ²]	Comp. Noise [nV ²]	Dyn. Amp. Noise [nV ²]	Total Noise [nV ²]	SNR [dB]
4.14	24	10	20	58.1	68.1
7%	41%	17%	34%	100%	

III. ATTENUATED PASSIVE RESIDUE TRANSFER

In a conventional pipelined-SAR ADC, the first stage not only needs to sample and coarsely quantize the input, but also needs to participate in the residue amplification for the succeeding stage. In contrast, the second stage only needs to sample the amplified residue voltage and perform the fine quantization. As a result, the total conversion time of the first stage is typically longer than that of the second stage, if the resolutions of the first and the second stages are the same. Thus, the first stage usually constitutes the speed bottleneck of the whole ADC. Fortunately, the attenuated or non-attenuated passive residue transfer technique can be employed to remove the time-consuming task of residue amplification from the timing budget of the first stage [20]–[23]. For the non-attenuated passive residue transfer, the digital-to-analog converter (DAC) of two second stages participate in the sampling of the input signal alternately, potentially causing a bandwidth mismatch problem and limiting the achievable spurious-free dynamic range (SFDR) [22]. As a result, the attenuated passive residue transfer is utilized in this work to boost the conversion speed.

The working principle of the attenuated passive residue transfer is depicted in Fig. 11. First, when the first stage is performing the coarse conversion, the transfer capacitor C_{TRF} is reset to zero. Once the coarse conversion is done, the LSB capacitor in the first-stage DAC is switched to generate the residue voltage. Then, the transfer switch S_{TRF} turns on and the transfer capacitor is utilized to sample the residue voltage. After the residue voltage has been sampled by the transfer capacitor, the first stage is released to sample the next input. Meanwhile, the residue voltage held by the transfer capacitor is amplified.

Thanks to the attenuated passive residue transfer, the DAC in the first stage does not need to hold the residue voltage for the residue amplifier until the amplifier's output is acquired by the second stage. In other words, the first stage can be released during the residue amplification phase, cutting down a large part of the first-stage timing budget. The drawback of the attenuated passive residue transfer is the residue attenuation due to the charge sharing between the DAC and the transfer capacitor, which is expressed as

$$A_{\text{atten}} = \frac{C_{\text{DAC}}}{C_{\text{TRF}} + C_{\text{DAC}}}. \quad (23)$$

This signal attenuation will dramatically impact the overall noise budget of the ADC, as the kT/C noise, the amplifier noise and the second-stage comparator noise need to be chosen

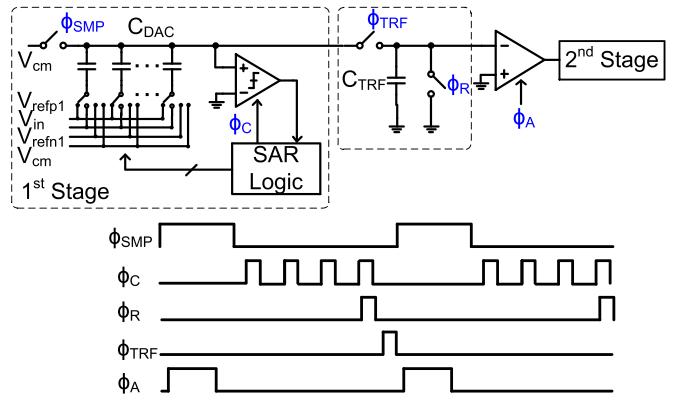


Fig. 11. Schematic and timing diagram of attenuated passive residue transfer.

to meet the SNR requirement relative to the attenuated signal. On the one side, it seems that the smaller the transfer capacitor, the less attenuation the residue sees. On the flip side, as the transfer capacitor directly determines the kT/C noise using this technique [24]

$$\overline{V_n^2} = \frac{kT}{C_{\text{TRF}}}. \quad (24)$$

The transfer capacitor cannot be too small. It turns out that for a specific ADC there exists an optimum value for the transfer capacitor C_{TRF} that leads to an optimum SNR.

IV. PROTOTYPE ADC DESIGN

A. ADC Architecture and Clock Generator

Fig. 12 depicts the schematic and timing diagram of the 12-b prototype ADC incorporating the PVT-stabilized dynamic amplifier and the attenuated passive residue transfer. The first stage resolves 8 b using a 2-b/cycle conversion scheme. While a 2-b/cycle conversion scheme can boost the conversion speed significantly relative to a 1-b/cycle SAR, it suffers from the mismatch between the capacitors in signal DAC (SIG-DAC) and reference DAC (REF-DAC) as well as the comparator offsets during the coarse conversion cycles [25]. In this work, foreground calibration is employed to calibrate the comparator offsets; the first stage is also designed to contain 1-b built-in redundancy for error tolerance.

Ideally, the second stage can also adopt the 2-b/cycle conversion scheme. However, because of the small inter-stage gain ($5\times$), the LSB size of the second stage is not too large. The aforementioned errors will impede the second stage to

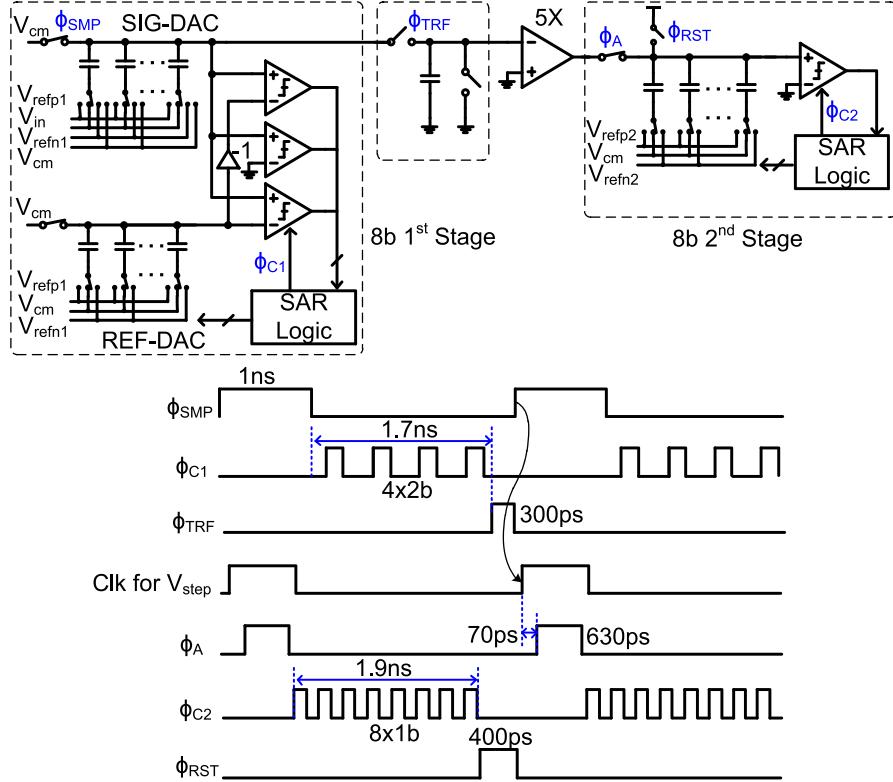


Fig. 12. Schematic and timing diagram of the prototype pipelined-SAR ADC.

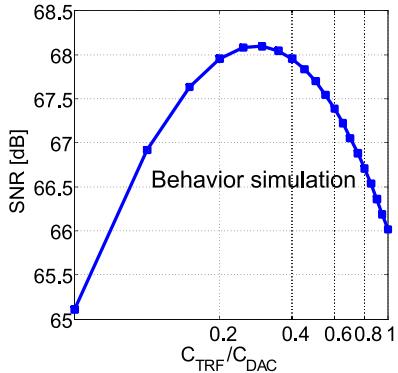


Fig. 13. Simulated SNR versus $C_{\text{TRF}}/C_{\text{DAC}}$.

achieve the desired resolution. In this prototype, the second stage resolves 8 b using the conventional 1-b/cycle conversion scheme. To compensate for the SNR penalty caused by the attenuated passive residue transfer, the quantization noise of the prototype ADC is designed to be at the 13-b level. Furthermore, 2-b inter-stage redundancy is allocated to absorb any small decision errors in the first stage and offset drifts of the amplifier and comparators due to ambient changes. For the prototype ADC, according to the simulation result in Fig. 13, the optimum value of the transfer capacitor C_{TRF} is estimated to be $0.3^*C_{\text{DAC}} \approx 300 \text{ fF}$.

Table I shows the noise breakdown of the ADC, i.e., the kT/C noise of the attenuated passive residue transfer, the noise of PVT-stabilized dynamic amplifier, the second-

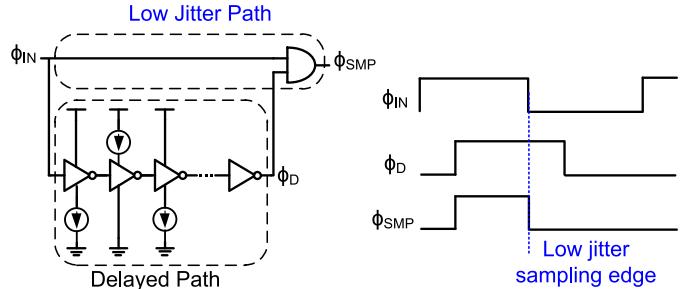


Fig. 14. Sampling clock generator.

stage comparator noise, and the quantization noise, resulting in a 68.1-dB SNR.

Since the inter-stage gain is only 5, the reference voltage for the second stage is different from that of the first stage. The reference generations for both stages are implemented off-chip. Moreover, around 400 and 100 pF bypass capacitors are implemented on chip to stabilize the first stage and the second stage references, respectively.

In this design, the clock generator shown in Fig. 14 is employed to generate the sampling clock [26]. The noisy delayed path sets the pulsedwidth of the sampling clock while a clean input clock defines the sampling edge, resulting in a low-jitter configuration. Asynchronous SAR timing is utilized by this work to generate the high-speed internal clocks for the first- and the second-stage comparators, which also helps to expedite the overall conversion [4].

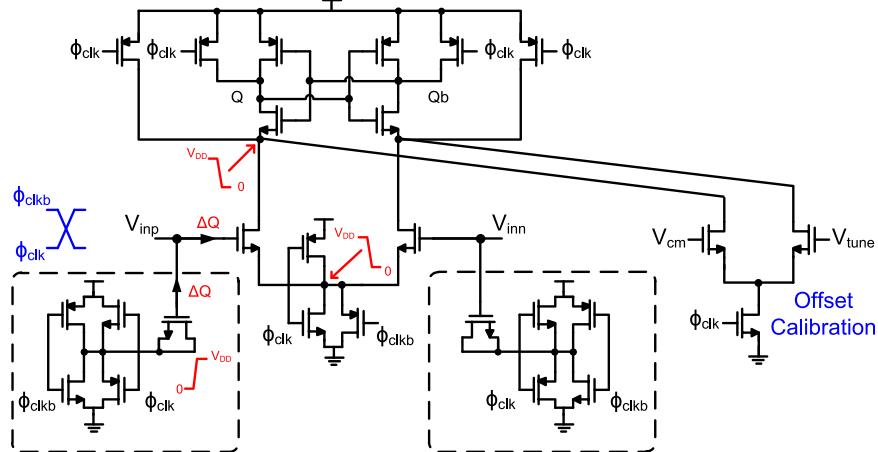


Fig. 15. Circuit schematic of the dynamic comparator with kickback noise cancellation.

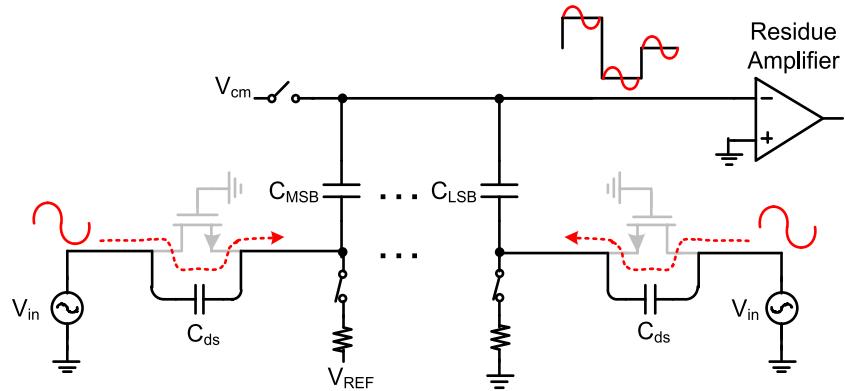


Fig. 16. Input signal feedthrough caused by the drain–source straycapacitance of the sampling switch.

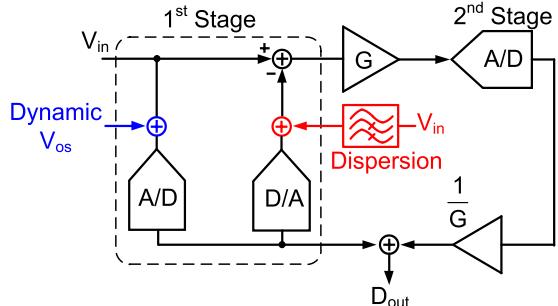


Fig. 17. Impact of input signal feedthrough on the pipelined-SAR ADC.

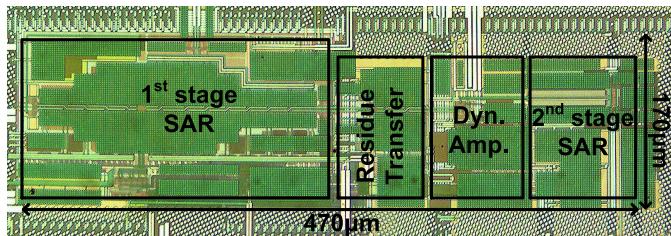


Fig. 18. Die photograph.

B. Comparator With Kickback Cancellation

Fig. 15 shows the schematic of the dynamic comparator used in the prototype ADC. Generally speaking, the kickback noise is a problem for the dynamic comparator. Once the comparator is activated, the source and drain of the input transistors

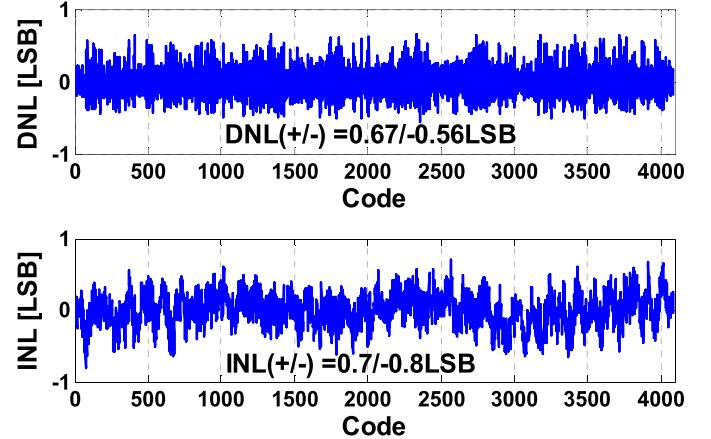


Fig. 19. Measured DNL and INL profiles.

will be pulled toward ground. Through the C_{gs} and C_{gd} of the input devices, this falling transition draws in charge from the gates of the input transistors and causes common-mode kickback noise on the input. Once there is any mismatch between the input transistors, the common-mode kickback noise will be converted into differential noise, interfering with the normal comparison. Since the LSB size of the second stage is not large, the second-stage DAC becomes vulnerable to the kickback noise coming from the comparator.

In this work, dummy transistors are utilized to cancel the common-mode kickback noise [27]. When the comparator is

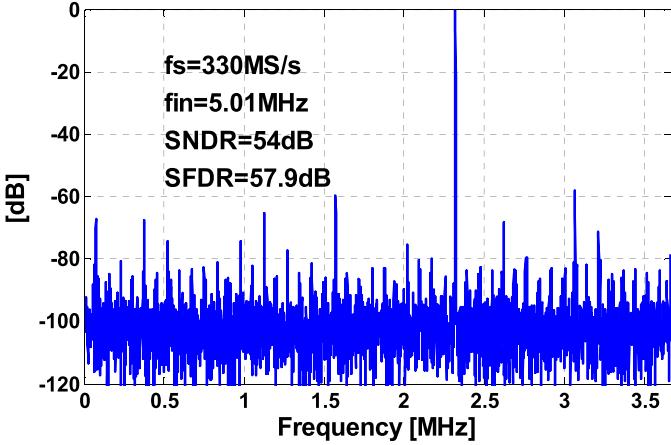


Fig. 20. Measured ADC spectrum before bit weight and offset calibration at 330 MS/s with a 5-MHz input (decimated by 45 \times).

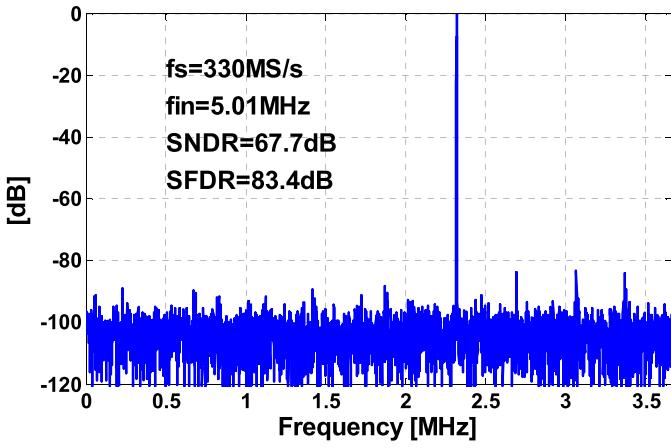


Fig. 21. Measured ADC spectra after calibration at 330 MS/s with (a) 5-MHz input and (b) 200 MHz (both decimated by 45 \times).

triggered, the source and drain of the dummy transistors are pulled up to the supply voltage. Ideally, the rising transition of the dummy transistors supplies all the charge drawn by the falling transition of input transistors, largely canceling the kickback noise. Nevertheless, if there is a timing mismatch

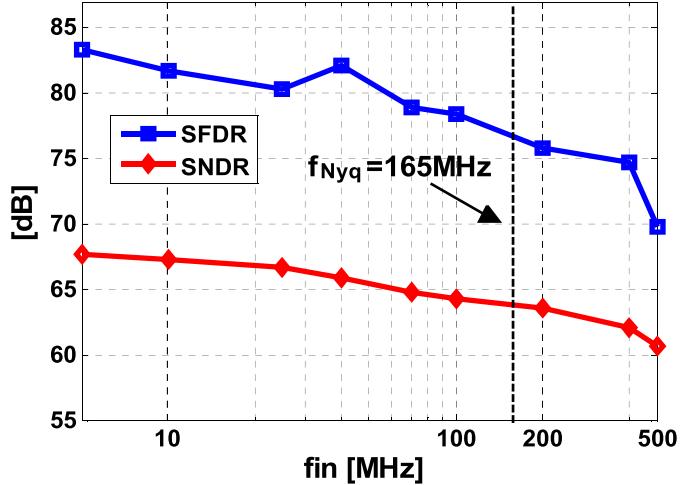


Fig. 22. Measured SNDR and SFDR versus input frequency.

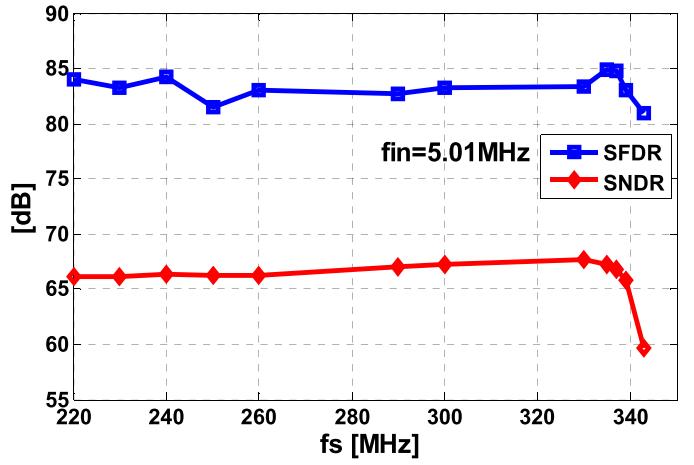


Fig. 23. Measured SNDR and SFDR versus sampling frequency.

between the rising and the falling transitions, the cancellation will not be exact, leaving some residual kickback. The falling edge of Φ_{clkb} is aligned with the rising edge of Φ_{clk} to ensure that the transitions of the input and dummy transistors occur simultaneously. The driver for the dummy transistor in Fig. 15 is modified from that of [27]. Monte Carlo simulation shows that with the modified driver, the comparator creates a smaller common-mode interference to the input when it is activated or deactivated. Due to the kickback cancellation, the common-mode kickback noise on the input is reduced from 40 to 2 mV.

C. Input Feedthrough of Sampling Switch

For high-speed and high-resolution ADC, the input feedthrough to the summing node can degrades the conversion accuracy dramatically. As illustrated in Fig. 16, when the sampling switch is off, the input signal will couple to the summing node of the first-stage DAC through the parasitic C_{ds} of the sampling switch. This coupling equivalently introduces a dynamic offset to the first-stage comparator during the coarse conversion and adds some fluctuation to the residue voltage

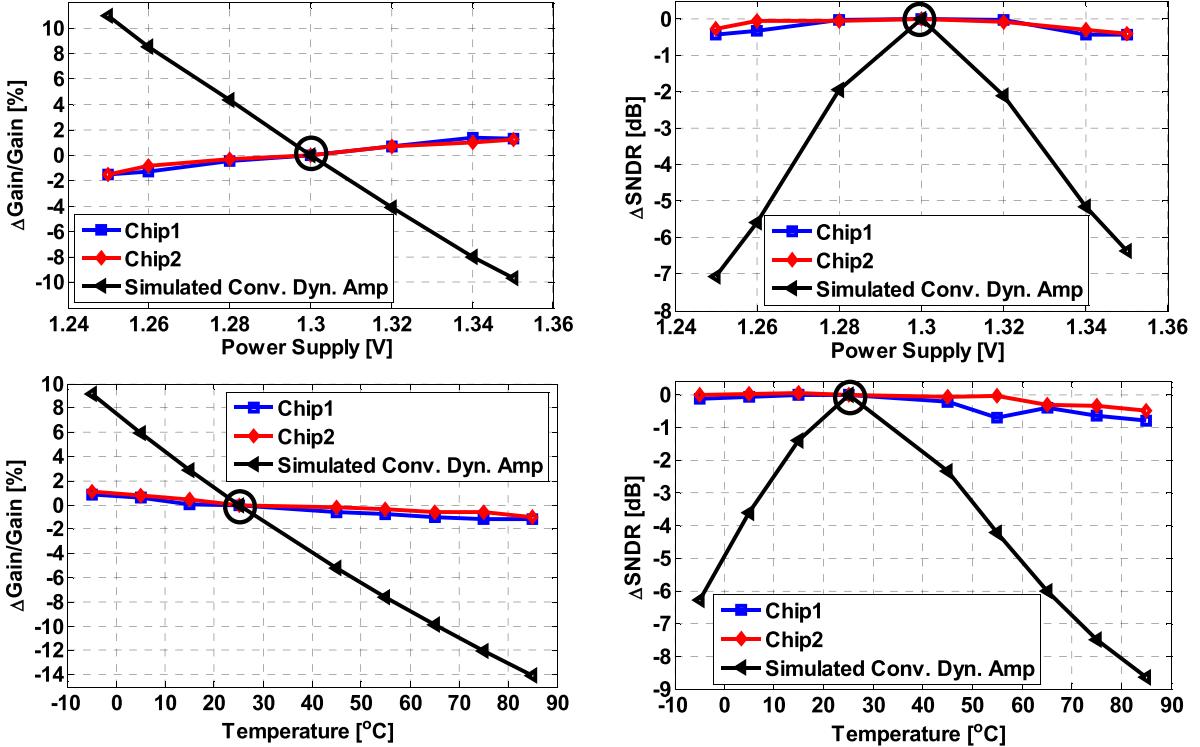


Fig. 24. Measured residue gain and ADC SNDR variations versus power supply and temperature. One-time power-on calibration was performed at 1.3 V and 25 °C.

during the residue amplification phase, as Fig. 17 illustrates. For the dynamic offset, it affects the residue voltage and the first-stage digital output equally but with opposite polarity, resulting in a complete cancellation in the digital output of the ADC. In other words, the dynamic offset impacts the pipelined-SAR ADC like the comparator noise of the first stage, which enlarges the residue voltage range but does not contribute to the overall noise of the ADC if the residue voltage stays within the quantization range of the second stage [28]. However, the input feedthrough sampled by the second stage during the residue amplification phase directly degrades the conversion accuracy. Since the input feedthrough path exhibits frequency selectivity (mostly high pass), the amplitude and phase shift of the input feedthrough depends on the input frequency. For a broadband signal, the feedthrough will add a dispersed input signal to the residue voltage, directly impacting the conversion accuracy.

In this prototype, dummy switches that cross-connect the input and the bottom plates of the DAC capacitors are added to cancel the signal feedthrough [29]. Moreover, some source and drain contacts in the layout of the sampling switch and dummy switch are removed to reduce the parasitic capacitor C_{ds} [30].

D. Calibration

A one-time power-up calibration was performed to correct the first-stage bit weights, the gain and offset of the residue amplifier and the comparator offsets. An extra differential pair is added to the dynamic comparator to facilitate the foreground offset calibration (see Fig. 15). One terminal of

this pair is connected to the input common-mode voltage while the other one is connected to an off-chip potentiometer. During the calibration phase of the first-stage comparators, the ADC's input is shorted to the input common-mode voltage and the potentiometer is tuned to ensure that the probability of a logic “1” output is around 0.5. Since the residue amplifier offset can be lumped into the second-stage comparator, it is not necessary to treat it separately. Note that the input of the dynamic amplifier is shorted to the common-mode voltage when the second-stage comparator is calibrated.

In this work, a one-time sine-wave fitting algorithm (implemented off-chip) is employed to correct the first-stage bit weights, but the bit weights of the second stage are not calibrated [31]. The inter-stage gain error due to process variation is also one-time calibrated by tuning the reference voltage of the V2T converters.

V. MEASUREMENT RESULTS

Fig. 18 shows the die photograph of the prototype ADC, which was fabricated in a 65-nm CMOS process with a core area of 0.08 mm². Fig. 19 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL) profiles after calibration, which are +0.67/-0.56 LSB and +0.7/-0.8 LSB, respectively.

Fig. 20 shows the measured ADC output spectrum before the first-stage bit weight and offset calibration. The output spectra of the ADC after calibration are shown in Fig. 21. For a 5-MHz input, the measured signal-to-noise plus distortion ratio (SNDR) is 67.7 dB and SFDR is 83.4 dB. For a

TABLE II
ADC PERFORMANCE COMPARISON

	This work	ISSCC15 Boo [32]	VLSI14 Zhou [3]	ISSCC16 Liu [33]	JSSC16 Zhu [34]	VLSI14 Lin [21]
Architecture	Pipelined SAR	Pipeline	Pipelined SAR	SAR	Pipelined SAR	Pipelined SAR
Technology	65nm	65nm	40nm	28nm	65nm	65nm
Sample Rate [MS/s]	330	250	160	100	450 (3x TI)	210 (2x TI)
SNDR@LF [dB]	67.7	67	66.5	65.7	59.6	63.5
Input Swing [V _{pp}]	2.4	1.5	2	1.6	1.2	1.6
SNDR@Nyq. [dB]	63.5	65.7	65.3	64.4	56.2	60.1
Peak SFDR [dB]	83.4	85	86.9	79	71	77.5
Power [mW]	6.23	49.7	4.96	0.35	7.4	5.3
FOM@LF [fJ/conv. step]	9.5	108.7	17.9	2.2	21.1	20.6
FOM@Nyq. [fJ/conv. step]	15.4	126.2	20.7	2.6	32	30.5
Area [mm ²]	0.08	0.59	0.042	0.005	0.07	0.48

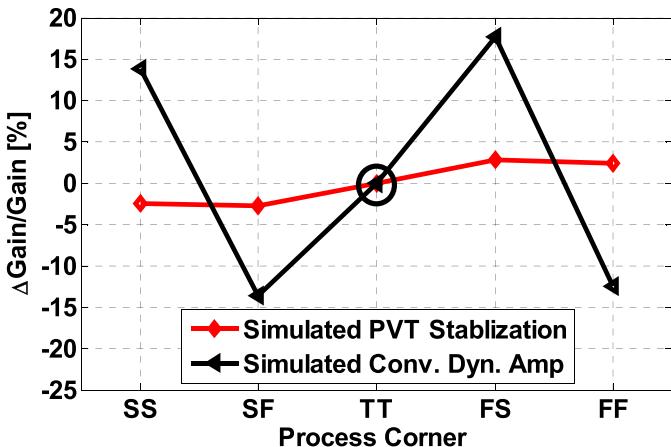


Fig. 25. Simulated residue gain versus process corner.

200-MHz input, the ADC measured an SNDR of 63.6 dB and an SFDR of 75.8 dB. The measured SNDR and SFDR versus the input frequency are summarized in Fig. 22. Note that the SNDR remains above 60 dB even with a 500-MHz input. Fig. 23 depicts the dynamic performance of the prototype ADC versus the sample rate.

The plots in Fig. 24 illustrate the measured SNDR and extracted residue gains of the ADC versus the supply voltage and temperature. For comparison, the simulated gains of the conventional dynamic amplifier in [10] and the corresponding SNDR are also plotted in Fig. 24. Over the supply voltage range from 1.25 to 1.35 V, the measured gain and SNDR fluctuations are reduced from 11% to 1.5% and from 7 to 0.5 dB, respectively. Over the temperature range from -5°C to 85°C , the measured gain and SNDR deviations are improved from 14% to 1.2% and from 8.6 to 0.8 dB, respectively. The prototype ADC was fabricated through a multi-project-wafer program, so only chips of typical corner were provided by the foundry and we could not measure the residue gain of this PVT-stabilized dynamic amplifier at other process corners. As an alternative, the simulated gain of PVT-stabilized dynamic amplifier versus the process corners

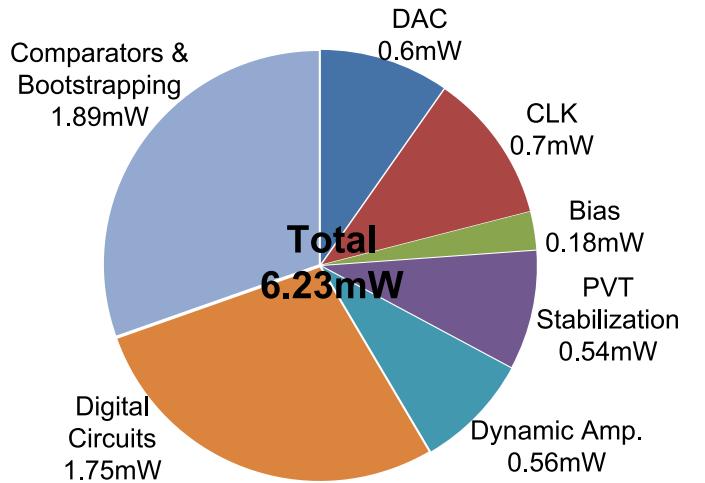


Fig. 26. Power consumption breakdown of prototype ADC.

are provided in Fig. 25. It can be seen that the maximum gain fluctuation is reduced from 18% to 2.8%. The small residue gain and SNDR fluctuations relative to those of the conventional dynamic amplifier validate the effectiveness of the PVT stabilization technique.

The residual gain variation is mostly attributable to the following factors. As discussed in Section II, the offset drift of the single-pole amplifier and the drift of the offset mismatch between the P-side and N-side V2T converters can result in gain variations. Besides, the approximation error of an exponential curve to a ramp also brings about some additional variation. Lastly, the mismatch between the delays of the P-side and N-side V2T converters will modulate the pulsewidth of the clock setting the slewing time of the dynamic amplifier. Some gain variation will be introduced if this delay mismatch varies over ambient changes.

The power consumption breakdown of this ADC is presented in Fig. 26. Clocked at 330 MS/s, the ADC consumes a total power of 6.23 mW, leading to a Walden figure of merit of 15.4 fJ/conversion step. Table II compares this work to the state-of-the-art designs with a similar SNDR. Not only can

the prototype attain a stable SNDR over supply and temperature variations, but it also achieves the highest conversion speed among non-interleaved SAR ADCs published recently, especially considering that this prototype is implemented in a 65-nm process.

VI. CONCLUSION

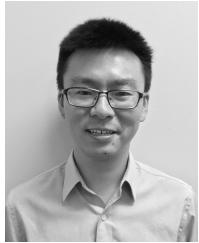
In this paper, a 12-b 330-MS/s non-interleaved pipelined-SAR ADC employing the PVT-stabilized dynamic amplifier and the attenuated passive residue transfer technique is reported. Thanks to the PVT stabilization technique, the prototype ADC measures less than 1-dB SNDR fluctuations over the supply voltage and temperature variations. Benefiting from the attenuated passive residue transfer, the timing burden of the first stage is relieved and a significant speed enhancement is obtained. The noise impact of the attenuated passive residue transfer and of the PVT stabilization circuit have been analyzed. Fabricated in a 65-nm CMOS process, the prototype ADC measured an SNDR of 63.5 dB and an SFDR of 75.8 dB for a near-Nyquist input. At a sample rate of 330 MS/s, the ADC consumes a total power of 6.23 mW, culminating in a Walden FoM of 15.4 fJ/conversion step.

ACKNOWLEDGMENT

The authors would like to thank SRC for the TxACE silicon fabrication program and Analog FastSPICE (AFS) Platform from Mentor Graphics.

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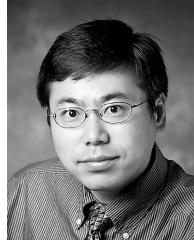
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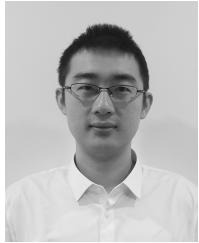
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