

Self-Regulated Reconfigurable Voltage/Current-Mode Inductive Power Management

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Abstract—A reconfigurable power management structure for inductive power delivery has been proposed by adaptively employing either resonant voltage or current mode (VM or CM) to improve the inductive power transmission performance against coils’ coupling distance (d), orientation (ϕ), and load impedance (R_L) variations. At the presence of these variations, unlike conventional VM and CM power managements with poor voltage- and power-conversion efficiencies (VCE and PCE), respectively, the proposed voltage/current-mode inductive power management (VCIPM) chip can achieve high VCE by automatically switching to CM when the receiver (Rx) coil voltage (V_R) is smaller than the required load voltage (V_L), and achieve high PCE by operating in VM when $V_R > V_L$. In addition, since VM and CM are only suitable for small and large R_L within the range of hundreds of ohms and above, respectively, the VCIPM chip can extend the R_L range. The VCIPM chip also eliminates the need for two off-chip capacitors by performing rectification, regulation, and over-voltage protection (OVP) in one step with one off-chip capacitor. In VM, intentional reverse current is employed for both voltage regulation and OVP, while the Rx coil switching frequency (f_{sw}) is adjusted for voltage regulation in CM. The theory behind the proposed VCIPM structure has been presented and validated by simulations and measurements. A VCIPM prototype chip was fabricated in a 0.35- μm 2P4M standard CMOS process occupying 0.52-mm² active area. In measurements, the VCIPM chip, operating at 1 MHz, achieved a high VCE of 4.1 V/V for R_L of 100 k Ω by operating in CM with $f_{sw} = 166.6$ kHz, and extended d and ϕ from 6 to 13.5 cm (125%) and 30° to 75° (150%), respectively, compared to its VM counterpart by adaptively switching from VM to CM.

Index Terms—Current mode (CM), efficiency, inductive link, power management, range extension, voltage mode (VM), wireless power transmission (WPT).

I. INTRODUCTION

MONG different approaches for wireless power transmission (WPT), inductive coupling has been extensively employed over the past decades in a wide variety of applications with different power requirements [1]–[9]. Inductive links are currently used for WPT to low-power devices such as implantable medical devices and radio frequency identification tags [1]–[6]. On the other hand, inductive links are the only viable solution in high-power applications such as recharging the battery of mobile electronics and electric vehicles [7]–[9].

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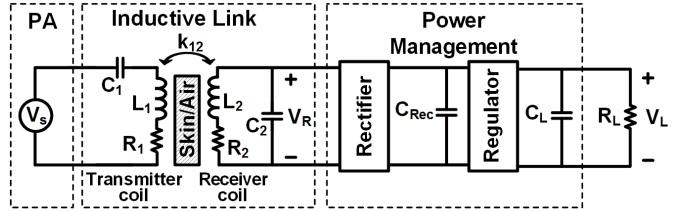


Fig. 1. Schematic of the conventional two-coil inductive link for WPT, followed by a conventional power management that includes a rectifier and a regulator for an ac-dc conversion.

Fig. 1 shows the generic diagram of a conventional two-coil inductive link, in which a transmitter (Tx) coil (L_1) is driven by an efficient power amplifier (PA), modeled with a voltage source (V_s), to wirelessly transfer power to a receiver (Rx) coil (L_2) via mutual magnetic coupling between L_1 and L_2 , i.e., k_{12} . Although we ignore the PA resistance R_s in Fig. 1 for the sake of simplicity, one can simply add it to L_1 resistance R_1 and consider the total loss inside Tx as $R_1 + R_s$ in the rest of this paper. Inside Rx, the ac voltage across the Rx LC-tank V_R is first converted to dc using an ac-dc converter in the form of a voltage rectifier or doubler. Then, a voltage regulator provides a constant voltage V_L across the load resistor (R_L) and capacitor (C_L). In general, there are four key parameters in inductive power transmission: 1) power delivered to the load (PDL) defined as $P_L = V_L^2/R_L$; 2) power transmission efficiency (PTE) defined as P_L/P_S , where P_S is the PA output power; 3) power-conversion efficiency (PCE) within Rx defined as P_L/P_R , where P_R is the power management input power; and 4) voltage-conversion efficiency (VCE) in Rx defined as $V_L/V_{R,\text{peak}}$, where $V_{R,\text{peak}}$ is the amplitude of V_R in steady state.

While achieving high PTE and sufficient PDL should always be considered in the design of inductive links, maximizing PCE or VCE depends on V_R . When V_R is larger than the required V_L , which is the case when coupling distance (d) is relatively small and coils are well aligned, high PCE is more desirable to maximize the power efficiency within Rx, and $VCE < 1$ V/V is quite acceptable. However, for $V_R < V_L$ with large d and/or misaligned coils, $VCE > 1$ V/V is paramount to achieve the required V_L even at the cost of lower PCE. Therefore, for most WPT applications that involve d and coils’ orientation (ϕ) variations and misalignments, the power management should be smart enough to sense V_R and decide to whether maximize VCE or not.

The PTE of the two-coil link in Fig. 1 is also highly sensitive to R_L , which is often given by the application [10].

In order to improve PTE for any R_L , multi-coil links in the form of three- and four-coil links have recently been proposed that provide load matching inside Rx [11]–[13]. However, these links need an additional coil in the Rx, which adds to the size, cost, and complexity of the system. More importantly in some applications R_L can change significantly during the operation while three- and four-coil links cannot dynamically compensate for R_L variations during the system operation [12]. Alternatively, off-chip matching circuits can also be used to transform R_L [14]–[16]. However, a network of off-chip capacitors and inductors is needed to dynamically tune a wide range of R_L during the operation, which again adds to the size, cost, and power loss in the Rx. Therefore, the power management should also provide optimal load condition during the operation.

In order to improve the PCE within Rx, active rectifiers with high-speed synchronous comparators, some equipped with delay compensation, have been presented in recent years [17]–[23]. In [24], a resonant regulation rectifier has been proposed that employs pulse-width/frequency modulation to adjust the ON-time window of the active rectifier switch for self-regulating V_L by controlling the forward current. Although high PCE and self-regulation have been achieved in active rectifiers, they suffer from low $VCE < 1$ V/V due to the voltage drop across the active switch.

In order to improve VCE, voltage doublers, multipliers, and dc–dc converters have been presented in the past [25]–[32]. The power management structure has also been switched between rectifier and doubler for voltage regulation and range extension in [26]. Although these techniques can improve VCE, they require additional ac–dc converters and/or off-chip components due to the low-frequency operation of the inductive links (<20 MHz), adding to the size, cost, and power loss in the Rx. A common theme with the aforementioned power managements is that they use the Rx LC -tank as a voltage source, i.e., they operate in voltage mode (VM), inherently leading to limited VCE.

The Rx LC -tank has recently been used as a current source to operate in current mode (CM) [23], [33]–[37]. In our previous work, we have proposed a new technique called Q-modulation, in which the Rx LC -tank has been shorted twice in every power carrier period, $T_p = 1/f_p$, to store energy and then deliver it to the load [33], [34]. Although Q-modulation can increase V_R and, therefore, PTE and PDL by dynamically transforming relatively small R_L (hundreds of ohms) to the optimal load, its VCE is still limited due to the use of a rectifier, and is only suitable for small R_L matching. A three-level reconfigurable resonant regulating rectifier is presented in [23] that simultaneously rectifies and regulates V_L by switching between full-bridge, half-bridge, and no rectifier structures. A resonant CM battery charger has recently been presented in [35] to recharge a battery from sub-volts ac carriers across the Rx LC -tank. However, this power management is not suitable for direct WPT due to its startup issue, and more importantly it achieves low PCE for small R_L and large V_R . Recently, we have also presented a single-switch CM resonant power delivery technique with the proof-of-concept discrete implementation,

in which the Rx LC -tank has been shorted for several T_p s to store energy as current in L_2 and then delivered it to the load within $T_p/4$ [36]. This CM technique could achieve high VCE of 3.1 V/V at $R_L = 100$ k Ω . In CM, we again define VCE as $V_L/V_{R,\text{peak}}$, but $V_{R,\text{peak}}$ is measured in the steady state from unloaded Rx LC -tank, which results in a lower value for VCE, because in practice $V_{R,\text{peak}}$ slightly decreases when Rx LC -tank is loaded by R_L . The CM technique could also improve PTE for large R_L (tens of kilohms and above) by transforming R_L to the equivalent parallel resistance of the Rx LC -tank, which is typically in the order of several kilohms and below [12], [36].

Considering a wide range of d , ϕ , and R_L variations in inductive links, therefore, neither VM nor CM power managements can provide the optimal performance. This has been our motivation to propose a reconfigurable voltage/current-mode inductive power management (VCIPM) that can adaptively switch between VM and CM based on V_R amplitude to: 1) maximize PTE when V_R is larger than the required V_L of 3.2 V and 2) maximize VCE for small $V_R \leq 3.3$ V [37]. In addition, the VCIPM chip can increase PTE for a wide range of large and small R_L by operating in CM and VM, respectively. The VCIPM chip has been designed for applications with power consumption in the range of several microwatts to tens of milliwatts. In the proposed VCIPM chip, V_R envelope is first detected and compared with 3.3 V. If $V_{R,\text{peak}} > 3.3$ V, VM configuration is selected and the power management operates as an active voltage rectifier with high PCE. If $V_{R,\text{peak}} \leq 3.3$ V, CM configuration is selected and the Rx LC -tank is shorted for optimal number of T_p s to store energy and then deliver it to the load. In addition, the VCIPM chip regulates V_L to 3.2 V by controlling the reverse current, which is defined as the current returning back from C_L to the Rx LC -tank in Fig. 1, in VM and the switching frequency in CM, eliminating the need for the regulator and its associated off-chip capacitor. The VCIPM chip also performs over-voltage protection (OVP) along with self-regulation in VM using the reverse current. Therefore, the VCIPM chip only requires two off-chip capacitors, one for resonance (C_2 in Fig. 1) and one for rectification/regulation/OVP. This paper is an extension of our conference paper in [37], by adding detailed mathematical models and simulations for the VCIPM operation in VM and PTE for CM in Section II, detailed description of VCIPM operation and circuit design in Section III, and comprehensive measurement results and their detailed descriptions including measurement setup, inductive link parameters, VM and CM transient responses, VCE and PTE versus R_L and V_s , V_L versus misalignment, and startup waveforms in Sections IV. Finally Section V concludes the paper.

II. VCIPM MODELING AND OPERATION

The proposed VCIPM operates in either VM or CM. In VM, a half-wave active rectifier with adjustable reverse current for simultaneous rectification, regulation, and OVP forms the power management. Fig. 2(a) shows the simplified circuit model of the inductive link, followed by the proposed VCIPM structure in VM, in which M_2 acts as the rectifier switch,

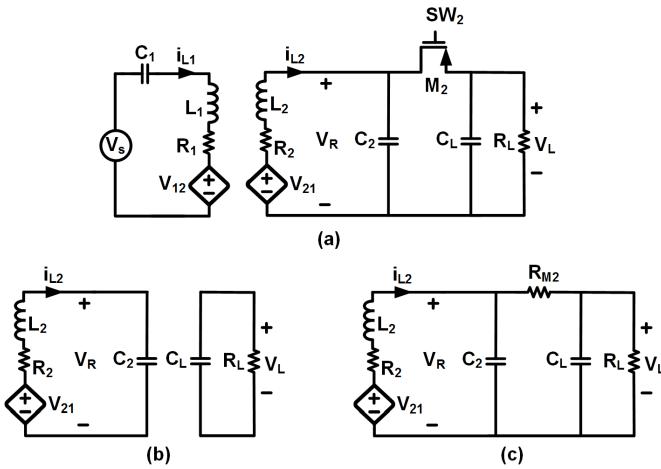


Fig. 2. Simplified circuit models of the inductive link and proposed VCIPM in VM operation with (a) M_2 as the active rectifier switch, (b) turned-off M_2 , and (c) turned-on M_2 .

continuously controlled by SW_2 pulses. This structure can be further simplified to the circuits in Fig. 2(b) and (c) when M_2 is turned off and on, respectively.

For extended-range WPT, in which L_1 and L_2 are loosely coupled and k_{12} is relatively small, if the switch turn-on time is negligible compared with T_p , the amplitude of the induced voltage in Rx, V_{21} in Fig. 2(a), can be written as

$$V_{21} = \frac{|V_s| k_{12} \sqrt{Q_1 Q_2} \sqrt{R_1}}{(1 + k_{12}^2 Q_1 Q_2) \sqrt{R_1}} \quad (1)$$

where $Q_1 = \omega_p L_1 / R_1$, $Q_2 = \omega_p L_2 / R_2$, and $|V_s|$ is the source voltage amplitude at the operation frequency of $\omega_p = 2\pi f_p = 1/(L_1 C_1)^{1/2} = 1/(L_2 C_2)^{1/2}$ [36]. When M_2 is turned off, as shown in Fig. 2(b), L_2 current (i_{L2}) can be found from

$$V_{21}(t) = L_2 \frac{di_{L2}(t)}{dt} + \frac{1}{C_2} \int i_{L2}(t) dt + R_2 i_{L2}(t) \quad (2)$$

the solution of which leads to

$$i_{L2}(t) = \exp(\alpha_1(t - t_0)) [A_1 \cos(\omega_{d1}(t - t_0)) + A_2 \sin(\omega_{d1}(t - t_0))] + B_1 \cos(\omega_p(t - t_0)) \quad (3)$$

where t_0 is the time zero-crossing of V_R , and α_1 and ω_{d1} can be calculated from

$$\alpha_1 = -\frac{R_2}{2L_2}, \quad \omega_{d1} = \sqrt{\frac{1}{L_2 C_2} - \alpha_1^2}. \quad (4)$$

A_1 , A_2 , and B_1 constants in (3) are determined by the initial conditions and V_{21} as

$$B_1 = \frac{|V_{21}|}{R_2}, \quad A_1 = i_{L2}(t_0) - B_1, \quad A_2 = \frac{di_{L2}(t_0)/dt - \alpha A_1}{\omega_{d1}} \quad (5)$$

where $i_{L2}(t_0)$ is L_2 initial current and $V_{21} = |V_{21}| \sin(\omega_p t)$. In startup, $i_{L2}(t_0 = 0) = di_{L2}(t_0 = 0)/dt = 0$. Using i_{L2} in (3), V_R can also be found from

$$V_R(t) = \frac{1}{C_2} \int_{t_0}^t i_{L2}(t) dt. \quad (6)$$

As shown in Fig. 2(b) when M_2 is off, C_L is discharged via R_L that decreases V_L for

$$\Delta V_{L,\text{dec}} \approx V_L \left(1 - \exp \left(\frac{-T_{\text{OFF}}}{R_L C_L} \right) \right) \quad (7)$$

where T_{OFF} is the M_2 OFF-time duration. In the conventional active rectifier [Fig. 2(a)], when V_R amplitude reaches V_L at $t = t_1$, M_2 is turned on that results in the simplified circuit in Fig. 2(c). Since C_L should be chosen large enough (microfarad range) to reduce ripples, we can safely ignore R_L and C_2 compared with C_L . Therefore, i_{L2} in Fig. 2(c) can approximately be found from

$$V_{21}(t) = L_2 \frac{di_{L2}(t)}{dt} + \frac{1}{C_L} \int i_{L2}(t) dt + (R_2 + R_{M2}) i_{L2}(t) \quad (8)$$

where R_{M2} represents M_2 loss. Solving for i_{L2} in (8) results in

$$i_{L2}(t) = \exp(\alpha_2(t)) [E_1 \cos(\omega_{d2}t) + E_2 \sin(\omega_{d2}t)] + D_1 \cos(\omega_p(t - t_1)) + D_2 \sin(\omega_p(t - t_1)) \quad (9)$$

where

$$\begin{aligned} \alpha_2 &= -\frac{R_2 + R_{M2}}{2L_2}, \quad \omega_{d2} = \sqrt{\frac{1}{L_2 C_L} - \alpha_2^2} \\ D_1 &= \frac{|V_{21}| \omega_p}{(R_2 + R_{M2}) \omega_p + [(1/C_L) - L_2 \omega_p^2]^2} \\ D_2 &= \frac{(1/C_L) - L_2 \omega_p^2}{(R_2 + R_{M2}) \omega_p} D_1 \\ E_1 &= i_{L2}(t_1) - D_2 \sin(\omega_p t_1) - D_1 \cos(\omega_p t_1) \\ E_2 &= \frac{di_{L2}(t_1)/dt - \alpha_2 E_1 + D_1 \omega_p \sin(\omega_p t_1) - D_2 \omega_p \cos(\omega_p t_1)}{\omega_{d2}}. \end{aligned} \quad (10)$$

The initial conditions of $i_{L2}(t_1)$ and $di_{L2}(t_1)/dt$ should be calculated from (3) when the switch is off. When the switch is kept on until $t = t_2$, $C_L || R_L$ are charged through the Rx LC-tank and the V_L increase can be calculated from

$$\Delta V_{L,\text{inc}} \cong \frac{1}{C_L} \int_{t_1}^{t_2} i_{L2}(t) dt. \quad (11)$$

Using i_{L2} in (9) when the switch is on, V_R can also be found from

$$V_R(t) \cong \frac{1}{C_L} \int_{t_1}^t i_{L2}(t) dt + R_{M2} i_{L2}(t). \quad (12)$$

Fig. 3(a) and (b) shows the conventional and proposed methods for achieving rectification and regulation simultaneously within the active rectifier with forward and reverse currents, respectively. In the conventional technique, as shown in Fig. 3(a), the switch on-time duration (T_{ON}) is adjusted so that the forward current into $C_L || R_L$ can be controlled, while keeping the reverse current zero, to regulate V_L at the desired V_{DD} . In other words, if $V_L > V_{DD}$, $\Delta V_{L,\text{inc}}$ in (11) is decreased by reducing $T_{\text{ON}} = t_2 - t_1$ in Fig. 3(a) and vice versa [38], [39]. However, this technique suffers from

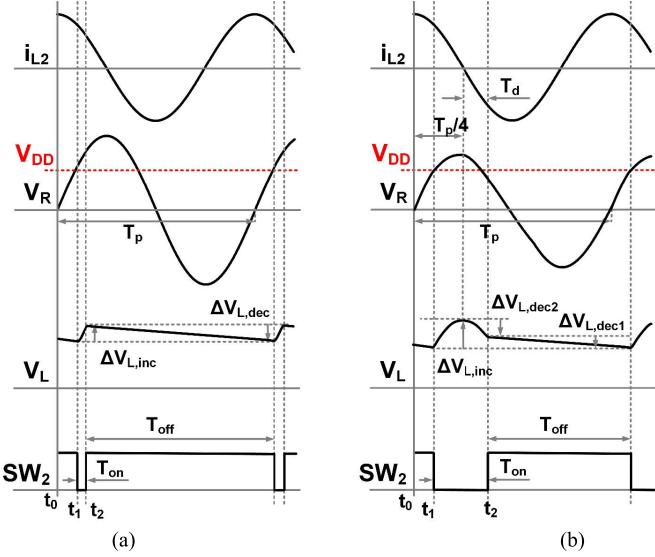


Fig. 3. Key waveforms for achieving both rectification and regulation in an active rectifier, shown in Fig. 2(a), using (a) conventional technique with controlling the forward current by decreasing the switch on-time duration (T_{ON}), and (b) proposed technique with employing the reverse current by increasing T_{ON} .

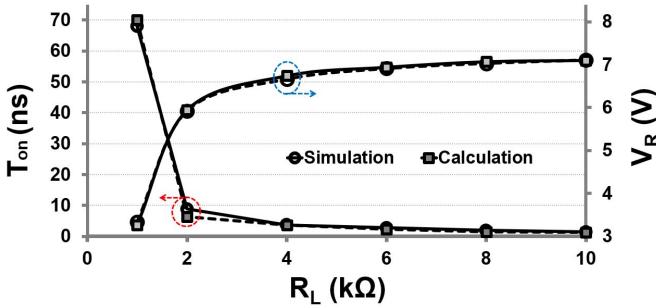


Fig. 4. Simulated and calculated T_{ON} and V_R versus R_L in the conventional self-regulated active rectifier [Figs. 2(a) and 3(a)] to achieve constant V_L of $V_{DD} = 3.2$ V. The circuit parameters are listed in Table I.

very small T_{ON} and large V_R , particularly for large R_L , which have been alleviated in the proposed VCIPM by using reverse current in Fig. 3(b).

Fig. 4 shows the simulated and calculated results for V_R amplitude and T_{ON} versus R_L in the conventional self-regulated active rectifiers [Figs. 2(a) and 3(a)] for maintaining V_L constant at $V_{DD} = 3.2$ V using the circuit parameters listed in Table I and $R_{M2} = 0$. In calculations, V_R was found from (6) and (12) when the switch was turned off and on, respectively, and T_{ON} was calculated by finding t_2 from $\Delta V_{L,inc} = |\Delta V_{L,dec}|$ in (7) and (11), which is needed for regulation, at $V_L = 3.2$ V. In simulations, the circuit in Fig. 2(a) was built in the Cadence Spectre circuit simulator (Cadence Technology, San Jose, CA, USA). Three lessons to learn from Fig. 4: 1) calculation and simulation results match very well, validating the accuracy of our modeling; 2) as R_L was increased to several kilohms, T_{ON} was significantly decreased to nanoseconds and below to less frequently charge C_L , because larger R_L requires less power; and 3) as

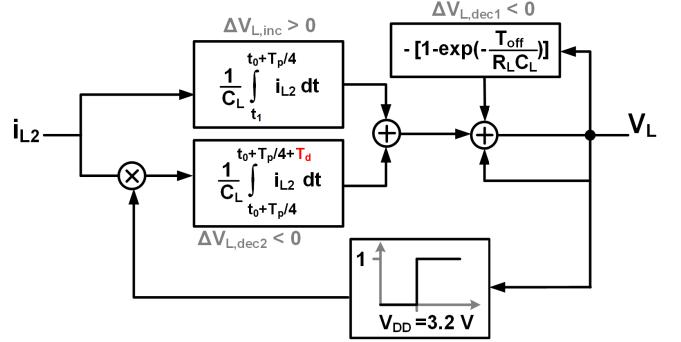


Fig. 5. Block diagram of the control loop for voltage regulation of V_L at $V_{DD} = 3.2$ V with reverse current by adjusting T_d in Fig. 3(b).

TABLE I
CIRCUIT PARAMETERS USED IN CALCULATIONS AND SIMULATIONS

Parameter	Value	Parameter	Value
L_1 (μH)	205	L_2 (μH)	4.2
R_1 (Ω)	30	R_2 (Ω)	1
C_1 (nF)	0.123	C_2 (nF)	6
C_L (nF)	100	k_{L2}	0.01
$ V_s $ (V)	5.5	f_p (MHz)	1

R_L was increased, V_R was significantly increased to several volts, because T_{ON} was intentionally reduced for conventional self-regulation, reducing the loading effect on the L_2C_2 -tank. In circuit implementation, pulses with small T_{ON} are hard to generate due to M_2 large input capacitance and can also increase the dynamic power consumption. On the other hand, large V_R can damage the chip, imposing the need for OVP circuitry and an additional capacitor for detuning the Rx LC-tank [34]. Small differences between calculated and simulated results in Fig. 4 could be due to approximations in calculating V_{21} in (1) and ignoring R_L and C_2 compared with C_L , as well as the inherent nonlinearity of the circuit with the diode, which has been modeled with a fixed resistor R_{M2} .

As shown in Fig. 3(b), our proposed technique for rectification, regulation, and even OVP all in one step employs the reverse current during T_d by maintaining M_2 on for longer time periods (larger T_{ON}) to allow current to flow from C_L to the Rx L_2C_2 -tank. This technique not only increases T_{ON} , but also maintains V_R just slightly above V_{DD} by detuning the L_2C_2 -tank with C_L , when R_L is large and/or d and ϕ are small. Therefore, only one off-chip capacitor (C_L) is needed for rectification, regulation, and OVP. It should be noted that such reverse current can be as small as zero when $V_L < V_{DD}$ to improve PCE of the rectifier, and as large as possible by even extending into $V_L < V_{DD}$ region when V_L is much larger than required V_{DD} . In general, large reverse currents can degrade the rectifier PCE, however, they can be carefully employed for regulation and OVP, as in this paper, when the received power by the L_2C_2 -tank is too much.

Fig. 5 shows how proper adjustment of T_d can regulate V_L . As seen in Fig. 3(b), for $t_1 < t < t_0 + T_p/4$, M_2 is on and V_L increases due to the forward current (positive i_{L2}) from

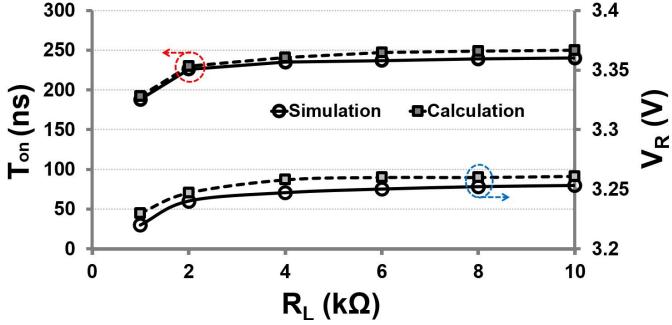


Fig. 6. Simulated and calculated T_{ON} and V_R versus R_L in the proposed self-regulated active rectifier (VM) as shown in Fig. 3(b) to achieve constant V_L of $V_{DD} = 3.2$ V using reverse current. The circuit parameters are listed in Table I.

L_2C_2 -tank to $C_L \parallel R_L$. The amount of V_L increase can be found from

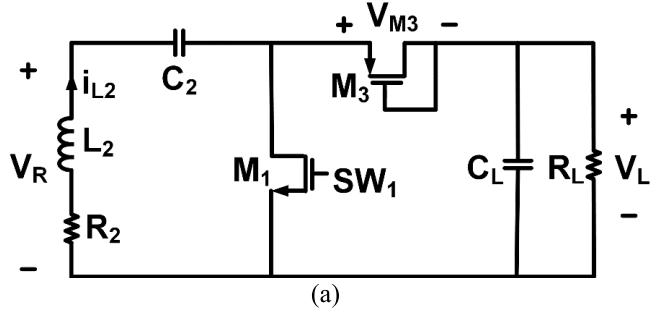
$$\Delta V_{L,inc} \approx \frac{1}{C_L} \int_{t_1}^{t_0+T_p/4} i_{L2}(t) dt. \quad (13)$$

In Fig. 3(b), for $t_0 + T_p/4 < t < t_0 + T_p/4 + T_d$ for the duration of T_d , M_2 remains on and V_L decreases due to the reverse current (negative i_{L2}) from C_L to the L_2C_2 -tank. The amount of V_L decrease can be found from

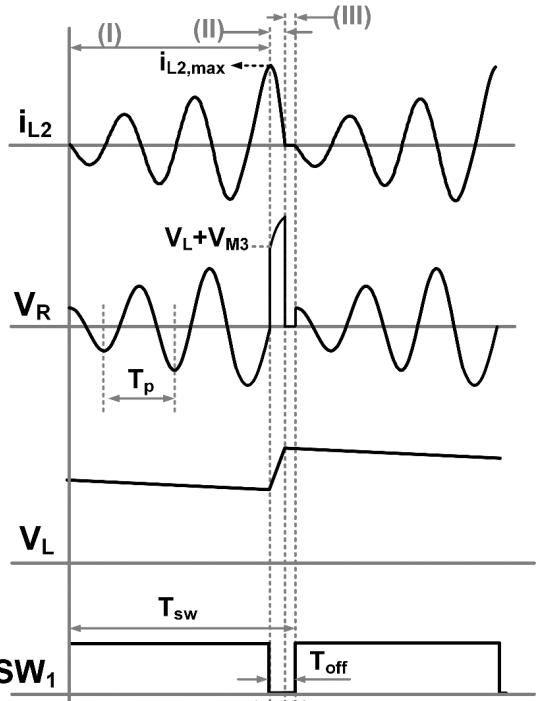
$$\Delta V_{L,dec2} \approx \frac{1}{C_L} \int_{t_0+T_p/4}^{t_0+T_p/4+T_d} i_{L2}(t) dt. \quad (14)$$

When M_2 is turned off at $t = t_0 + T_p/4 + T_d$, V_L decreases for $\Delta V_{L,dec1}$, calculated from (7). As shown in Fig. 5, a negative feedback loop is required to compare V_L with the required $V_{DD} = 3.2$ V in order to generate the proper T_d that adjusts $\Delta V_{L,dec2}$ in (14) with reverse current to achieve $\Delta V_{L,inc} = |\Delta V_{L,dec1} + \Delta V_{L,dec2}|$ in steady state. If $V_L < V_{DD}$, the loop sets $T_d = 0$ (no reverse current) and the power management operates as an efficient active rectifier. The control loop in Fig. 5 has only one dominant pole from the integrator block and, therefore, it is inherently stable.

Fig. 6 shows simulated and calculated T_{ON} and V_R versus R_L for the proposed regulation technique with the reverse current based on the control loop in Fig. 5 to maintain constant V_L of $V_{DD} = 3.2$ V, using inductive link parameters in Table I. In calculations, V_R was found from (6) and (12) when the switch was turned off and on, respectively, and T_{ON} was calculated by finding T_d from $\Delta V_{L,inc} = |\Delta V_{L,dec1} + \Delta V_{L,dec2}|$ in (7), (13), and (14) at $V_L = 3.2$ V. Comparing Figs. 4 and 6, it can be seen that: 1) T_{ON} experiences much less variations of 190 to 250 ns for the same R_L range of 1–10 k Ω ; 2) the required T_{ON} is much larger ($\sim 10\times$) in the proposed technique; and 3) V_R amplitude remains almost constant (safe operation and OVP), thanks to the use of the reverse current. Since for simplicity, M_2 is considered ideal in calculations and simulations, V_R amplitude in Fig. 6 is almost constant. However, in practice, V_R can slightly change due to voltage drop across M_2 .



(a)



(b)

Fig. 7. VCIPM operation in CM. (a) Simplified schematic of Rx by adding SW_1 to short L_2C_2 -tank for several T_p s to store energy and then deliver it to the load through diode-connected M_3 transistor. (b) Key operational waveforms in three different regions, demonstrating the jump in V_R when M_1 is opened for $T_{OFF} = T_p/4$ to charge C_L [36].

Fig. 7(a) shows the simplified circuit schematic of the proposed VCIPM in CM configuration, in which a switch (M_1) has been added in parallel with the series-connected L_2C_2 -tank, and a diode-connected transistor (M_3) provides a unidirectional current path to the load ($C_L \parallel R_L$). Fig. 7(b) shows the CM switching diagram and key waveforms, including i_{L2} , V_R , V_L , and M_1 control signal (SW_1) at the switching frequency of $f_{sw} = 1/T_{sw}$. The operation can be divided into three regions: 1) region-I ($t_0 < t < t_1$): SW_1 is high, M_1 is turned on for several T_p s and, therefore, the high-Q L_2C_2 -tank stores the maximum energy; 2) region-II ($t_1 < t < t_2$): at the peak of i_{L2} , i.e., $i_{L2,max}$, when the voltage across C_2 is zero and all the energy is stored in L_2 , SW_1 becomes low, M_1 is turned off and L_2 energy is delivered to $C_L \parallel R_L$ for less than $T_p/4$; and 3) region-III ($t_2 < t < t_3$): M_1 remains off for $t_3 - t_1 = T_p/4$ while $i_{L2} = 0$ to end a complete

power cycle. The same switching scheme is repeated at f_{sw} . It should be noted that OVP is not required in CM, because VCIPM operates in CM-only at the small V_R of ≤ 3.3 V. However, short but large voltage peaks in region-II might damage M_1 and M_3 if they are low-voltage transistors. While the minimum amplitude of these peaks is $V_L + V_{th3}$, where V_{th3} is the M_3 threshold voltage, the maximum amplitude depends on M_3 size, L_2 current, and V_L . Therefore, in the design phase one should properly optimize these parameters to ensure that V_R peaks in CM are smaller than the transistor breakdown voltage. In VCIPM, we used 5-V transistors, and even similar to [35], two series-connected transistors can replace M_1 and M_3 to further protect them.

The switching timing is a key in CM. At $t = t_1$ in Fig. 7(b), since V_R is zero and the only path for discharging L_2 is M_3 , V_R suddenly increases to $> V_L + V_{th3}$ to charge C_L . Therefore, a large VCE can be achieved in CM for small V_R . We have already discussed the operation of CM in detail in [36]. In CM, f_{sw} is used to self-regulate V_L . If $V_L < V_{DD}$, f_{sw} is increased to its optimal maximum to more frequently charge C_L and vice versa.

The inductive link PTE in VM can be easily found from [12] by modeling the power management and dc R_L as an equivalent ac R_L . In CM, PTE can be similarly defined as

$$PTE = \eta_{Tx} \times \eta_{Rx} = \frac{k_{12}^2 Q_1 Q_{2L,eq}}{1 + k_{12}^2 Q_1 Q_{2L,eq}} \times \frac{Q_{2L,eq}}{Q_{L,eq}} \quad (15)$$

where η_{Tx} and η_{Rx} represent power efficiencies in Tx and Rx, respectively, and $Q_{2L,eq}$ and $Q_{L,eq}$ are the equivalent quality factors within Rx due to the switching of the Rx LC-tank in CM. It should be noted that in VM [Fig. 2(a)], $Q_{2L,eq}$ and $Q_{L,eq}$ can be found from $Q_L Q_2 / (Q_L + Q_2)$ and $R_{L,ac} / \omega_p L_2$, respectively [12]. Considering the general definition of Q as the ratio of averaged stored energy to the averaged dissipated energy within an LC-tank [34], $Q_{2L,eq}$ and $Q_{L,eq}$ in CM (Fig. 7) can be defined as

$$\begin{aligned} Q_{2L,eq} &= 2\pi \frac{0.5 \int_{t_0}^{t_0+T_{sw}} L_2 i_{L2}^2(t) + C_2 v_{C2}^2(t) dt}{T_{sw} [P_{R2} + P_{M1} + P_{M3} + P_{SW1} + P_L]} \\ Q_{L,eq} &= 2\pi \frac{0.5 \int_{t_0}^{t_0+T_{sw}} L_2 i_{L2}^2(t) + C_2 v_{C2}^2(t) dt}{T_{sw} P_L} \end{aligned} \quad (16)$$

where v_{C2} is the voltage across C_2 ($i_{L2} = C_2 \times dv_{C2}/dt$), and P_{R2} , P_{M1} , P_{M3} , and P_L are the power dissipations across R_2 , M_1 , M_3 , and R_L during one switching cycle of T_{sw} , respectively. P_{SW1} represents the dissipated power in generating SW_1 . It can be seen that both $Q_{2L,eq}$ and $Q_{L,eq}$ depend on T_{sw} that shows effective modulation of the Q or loading of the Rx LC-tank with T_{sw} [34]. In other words, T_{sw} is a new degree of freedom provided by CM to perform load matching and further optimize PTE. It should be noted that our PTE definition for CM also includes the loss of power management.

In order to calculate $Q_{2L,eq}$ and $Q_{L,eq}$ in (16), only i_{L2} in different operation regions as specified in Fig. 7(b) is needed, which can be found from [36], because i_{L2} either flows through M_1 or M_3 and $C_L || R_L$. Fig. 8(a) depicts calculated $Q_{2L,eq}$ and $Q_{2L,eq}/Q_{L,eq}$ in (16) versus different f_{sw} for M_1 resistance of 1 Ω , $R_L = 10$ k Ω , and the link

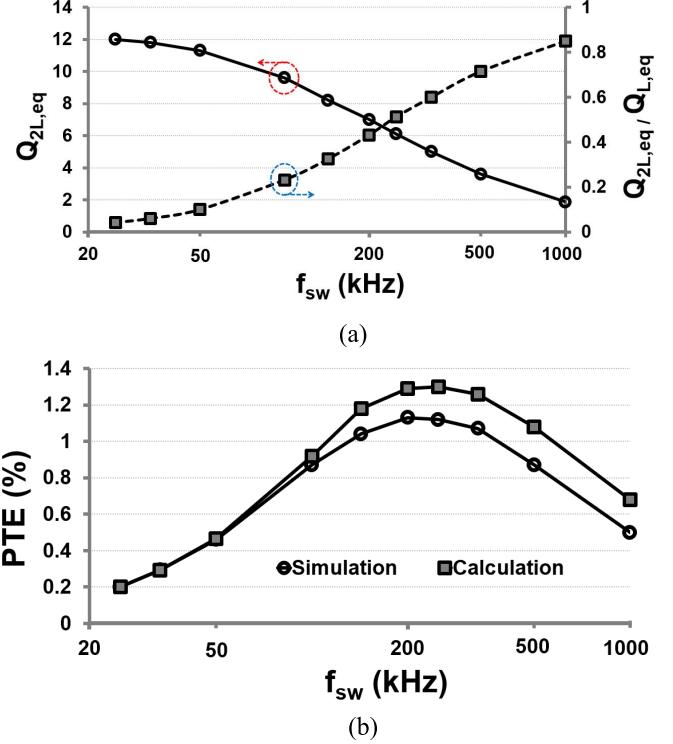


Fig. 8. Impact of f_{sw} on the Q of the Rx LC-tank and consequently on PTE in CM. (a) Calculated $Q_{2L,eq}$ and $Q_{2L,eq}/Q_{L,eq}$ in (16) versus f_{sw} . (b) Calculated and simulated PTE versus f_{sw} . The circuit parameters are listed in Table I (M_1 resistance of 1 Ω , $R_L = 10$ k Ω).

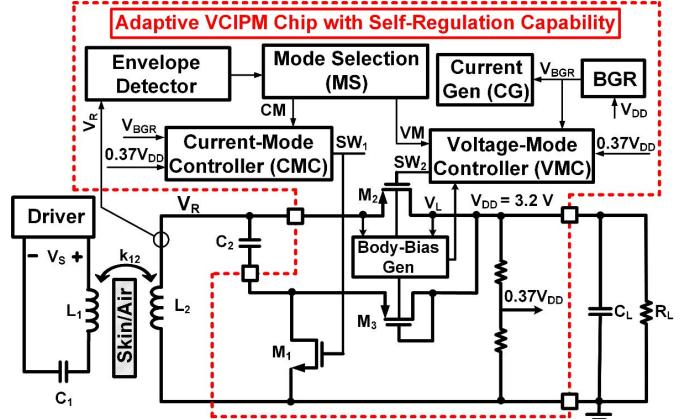


Fig. 9. Block diagram of the proposed adaptive reconfigurable VCIPM chip that operates either in VM or CM based on V_R amplitude, and can perform rectification, regulation, and OVP all in one step using one off-chip capacitor (C_L).

parameters in Table I, ignoring P_{SW1} and M_3 loss for the sake of simplicity. Three lessons can be learned from Fig. 8(a): 1) $Q_{2L,eq}$ decreases with f_{sw} , because $C_L || R_L$ are connected more frequently to the Rx LC-tank at higher f_{sw} , increasing the loading effect and reducing the stored energy in the Rx LC-tank (resulting in lower $Q_{2L,eq}$); 2) $Q_{2L,eq}/Q_{L,eq}$ increases with f_{sw} , because power is delivered to $C_L || R_L$ more often at higher f_{sw} , increasing the ratio of $P_L / (P_{R2} + P_{M1} + P_{M3} + P_{SW1})$ in (16); and 3) there is an optimal f_{sw} that can lead to the highest $Q_{2L,eq}$ and $Q_{2L,eq}/Q_{L,eq}$ in (15) to maximize PTE by optimizing both η_{Tx} and η_{Rx} .

Fig. 8(b) compares calculated and simulated values of PTE versus f_{sw} range of 25–1000 kHz. As expected from Fig. 8(a), there is an optimal f_{sw} of 200 kHz that can strike a balance between $Q_{2L,eq}$ and $Q_{2L,eq}/Q_{L,eq}$ or η_{Tx} and η_{Rx} to achieve the highest PTE. In other words, at $f_{sw} > 200$ kHz, η_{Tx} reduces due to the decrease in $Q_{2L,eq}$, and conversely η_{Rx} reduces at $f_{sw} < 200$ kHz due to the decrease in $Q_{2L,eq}/Q_{L,eq}$. Therefore, f_{sw} is an effective parameter in CM to maximize PTE. The small mismatch between simulation and calculation results could be due to the non-idealities of circuit components and the inherent non-linearity in the CM operation.

III. VCIPM CHIP ARCHITECTURE

Fig. 9 shows the block diagram of a prototype VCIPM chip, which was designed at the f_p of 1 MHz to regulate V_L at $V_{DD} = 3.2$ V. The VCIPM chip operates in either VM or CM based on the V_R amplitude using M_2 or M_1 and M_3 transistors, respectively, and performs rectification, regulation, and OVP all in one step with a single off-chip capacitor (C_L). In VCIPM chip, V_R amplitude is first detected by a passive envelope detector. Then, a mode selection (MS) block determines whether VCIPM chip should operate in VM or CM by enabling VM controller (VMC) or CM controller (CMC) blocks, respectively. This threshold for mode switching should be determined by the maximum load power, which results in the highest voltage drop across the rectifier in VM. In the VCIPM chip, the MS block selects VM for $V_R > 3.3$ V and CM for $V_R \leq 3.3$ V to account for rectifier voltage drop of 0.1 V at the maximum P_L of 20 mW and $V_{DD} = 3.2$ V. If VMC is enabled, $M_1(W/L = 2.5 \text{ mm}/0.6 \mu\text{m})$ is turned on by setting $SW_1 = 3.2$ V, and $M_2(W/L = 0.5 \text{ mm}/0.6 \mu\text{m})$ is controlled by SW_2 to form a half-wave active rectifier, as shown in Fig. 3(b). In VM, diode-connected $M_3(W/L = 10 \text{ mm}/0.6 \mu\text{m})$ is always off, because its source-gate voltage is negative. If CMC is enabled, M_2 is turned off by setting SW_2 to the highest voltage between V_L and V_R using a body-bias generator, and M_1 is controlled by SW_1 , as shown in Fig. 7(b). The body-bias generator, the circuit diagram of which is shown in Fig. 10(a), also controls the bulks of M_2 and M_3 to avoid any leakage current through bulk. Self-regulation will also be achieved in VMC and CMC by adjusting SW_2 and SW_1 pulses, respectively. A bandgap reference (BGR) provides a constant 1.2 V, from which a reference bias current of 60 nA is generated by a current generator (CG).

Fig. 10(a) and (b) shows the block diagrams and key operational waveforms of VMC and CMC, respectively. In VMC, a regulation amplifier [Reg_Amp in Fig. 10(a)], controlling the bias current (I_{bias}) of the active rectifier comparator (VM_Comp), amplifies the difference between V_L and required $V_{DD} = 3.2$ V by comparing $0.37 \times V_L$ with $V_{BGR} = 1.2$ V. If $V_L < 3.2$ V, this amplifier outputs low and I_{bias} is maximized. Therefore, VM_Comp operates at its maximum speed so that it can maximize the forward current and minimize the reverse current to achieve the highest PCE as well as to quickly charge C_L and increase V_L . When V_L surpasses 3.2 V, Reg_Amp reduces I_{bias} , slowing

down VM_Comp in turn-off, that allows reverse current from C_L to L_2C_2 -tank by increasing the width of SW_2 pulses (T_d in Fig. 3), as it can be clearly seen in Fig. 10(a) inset waveforms.

In CMC as shown in Fig. 10(b), a time-base generator (TBG), whenever it is reset, outputs high after 4 μs to enable a regulation comparator (Reg_Comp) that compares $0.37 \times V_L$ with $V_{BGR} = 1.2$ V. If $V_L < 3.2$ V, the CM comparator (CM_Comp) with an intentional offset of 170 mV is enabled by Reg_Comp to detect the time zero-crossings of V_R , where i_{L2} reaches its maximum, with the help of a synchronization block and consequently generates a sharp SW_1 pulse to charge C_L through M_3 . The synchronization block includes two cascaded D-flip-flops that count two pulses to generate a transition, which is then converted to a short pulse (active low) with the width of $T_p/4$ by a pulse-generator block. The pulse-generator output controls M_1 with a driver (SW_1 pulses) and also resets D-flip-flops and TBG for the same process to be repeated. Fig. 10(b) inset shows how synchronization block can eliminate false CM_Comp pulses, which are not at the time zero-crossings of V_R . The intentional offset in CM_Comp compensates for the circuit delays in the CMC path, ensuring M_1 switching occurs at i_{L2} peaks. One can calculate this offset by finding the delays of synchronization, pulse generator, and driver blocks in simulations or measurements. If $V_L > 3.2$ V, CM_Comp is disabled and, therefore, SW_1 remains high and C_L is not charged. It can be seen that f_{sw} is automatically adjusted to regulate V_L at 3.2 V. The maximum f_{sw} is limited to 166.6 kHz in the VCIPM chip according to our CM theory in [36]. Since synchronization block requires ~ 2 clock cycles ($\sim 2 \mu\text{s}$) for synchronization and then resting TBG, the TBG delay is set to 4 μs to achieve the maximum f_{sw} of 166.6 kHz.

Fig. 11 shows the detailed circuit diagrams of TBG, pulse generator, CM_Comp, and VM_Comp blocks, which are discussed in Fig. 10. As shown in Fig. 11(a), the TBG outputs low for $\sim 4 \mu\text{s}$ by first charging $C_1 = 350 \text{ fF}$ with the reference current of 110 nA set by $V_{bp} = 2.15$ V, and then comparing C_1 voltage (V_{C1}) with $V_{BGR} = 1.2$ V using a comparator that employs internal positive feedback. Any timing error in the TBG output due to process, voltage, and temperature variations, which can only have considerable effects on the C_1 value in TBG (bias voltage and currents are generated by a BGR), can change f_{sw} . However, as shown in Fig. 8(b), PTE is fairly robust against slight variations of f_{sw} . Inside the pulse generator in Fig. 11(b), the step input from the synchronization block (either rising or falling edge) is first delayed for $T_p/4 = 250 \text{ ns}$ with a current-starved inverter loaded by a $C_2 = 230 \text{ fF}$, and then passed through an XOR to create SW_1 pulses. The CM_Comp in Fig. 11(c) is designed with non-identical differential-pair transistors ($P_1: W/L = 1 \mu\text{m}/0.6 \mu\text{m}$, $P_2: W/L = 4 \mu\text{m}/0.6 \mu\text{m}$) to create 170-mV offset to generate proper SW_1 pulses, synchronized with time-zero crossings of V_R . Finally, the VM_Comp in Fig. 11(d) with a common-gate topology compares V_L and V_R with an adjustable speed controlled by its bias current (I_{bias}) in the range of 0–230 nA. An internal positive feedback with N_4 is added to further sharpen the falling edge of the output,

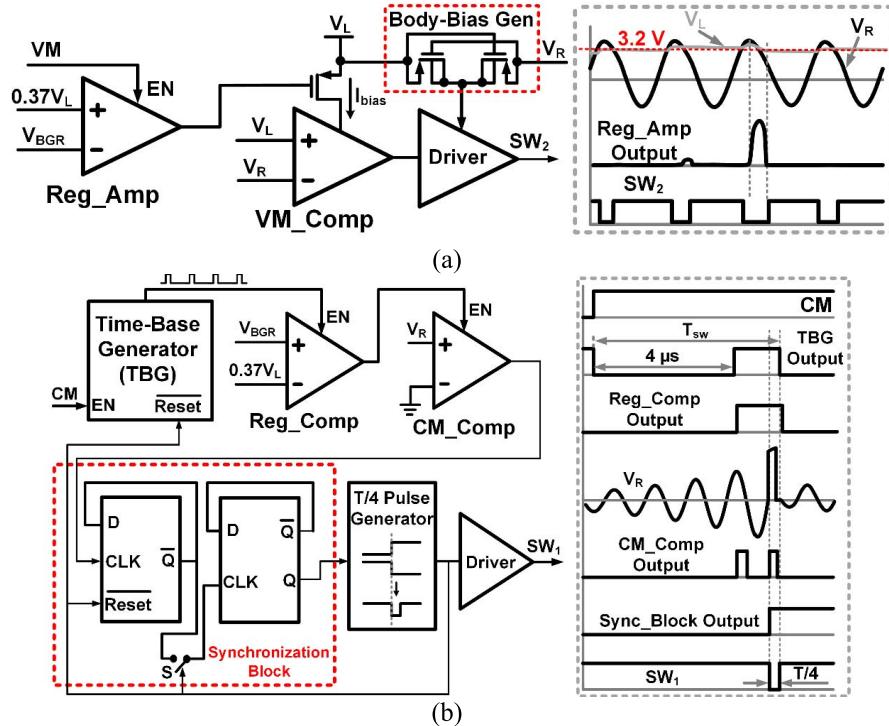


Fig. 10. Schematic diagrams and key waveforms of (a) VMC and (b) CMC blocks to generate proper SW_2 and SW_1 pulses, respectively.

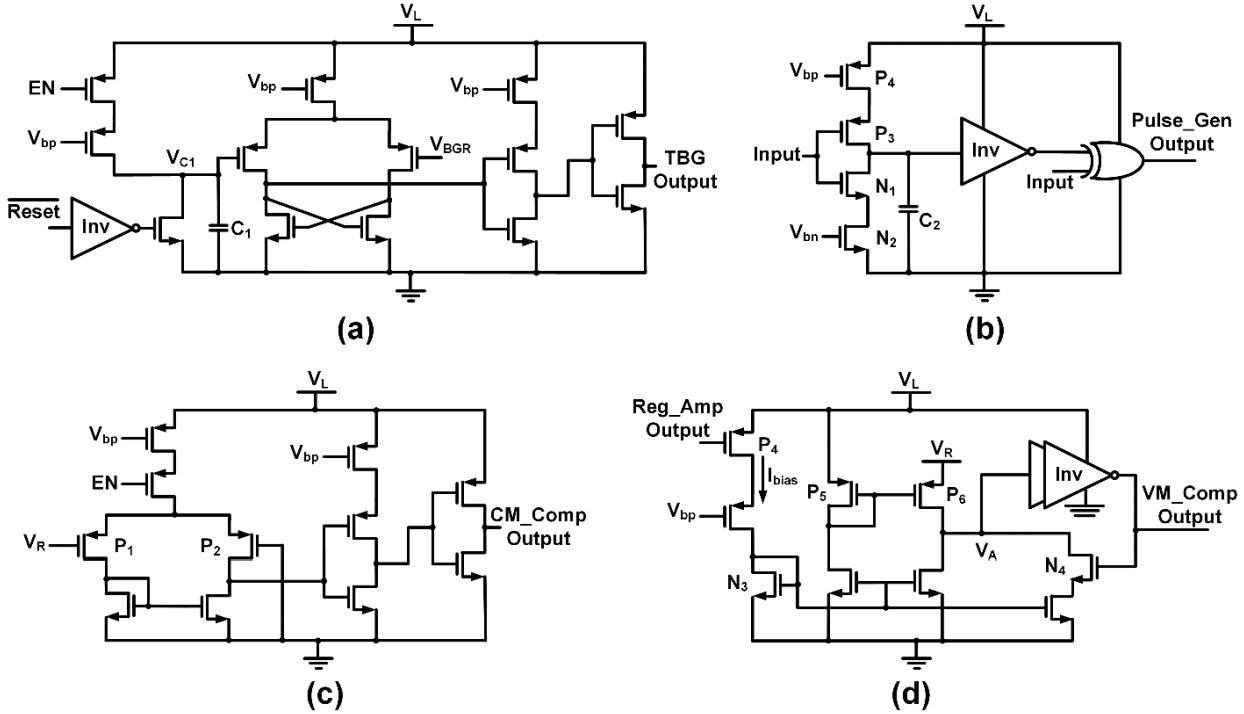


Fig. 11. Detailed schematic diagrams of (a) TBG, (b) pulse generator, (c) CM comparator (CM_Comp), and (d) VM comparator (VM_Comp) blocks, as shown in Fig. 10.

because at $V_R > V_L$, V_A is high and P_6 deeply enters into triode, significantly reducing the comparator gain compared with the rising edge for $V_R < V_L$.

IV. MEASUREMENT RESULTS

The VCIPM chip was fabricated in a $0.35\text{-}\mu\text{m}$ 2P4M standard CMOS process, occupying 1.56 and 0.52 mm^2 with and without pads, as shown in Fig. 12, respectively.

Fig. 13 shows the proof-of-concept VCIPM chip measurement setup with a pair of planar Tx and Rx coils (L_1 and L_2), fabricated on printed circuit board (PCB), as their specifications are listed in Table II. In Tx, a signal generator was used to drive L_1 at $f_p = 1$ MHz. In Rx, the L_2C_2 -tank was connected to the VCIPM chip to achieve a regulated V_L of 3.2 V across $C_L = 2\text{ }\mu\text{F}$ for different d , ϕ , and R_L .

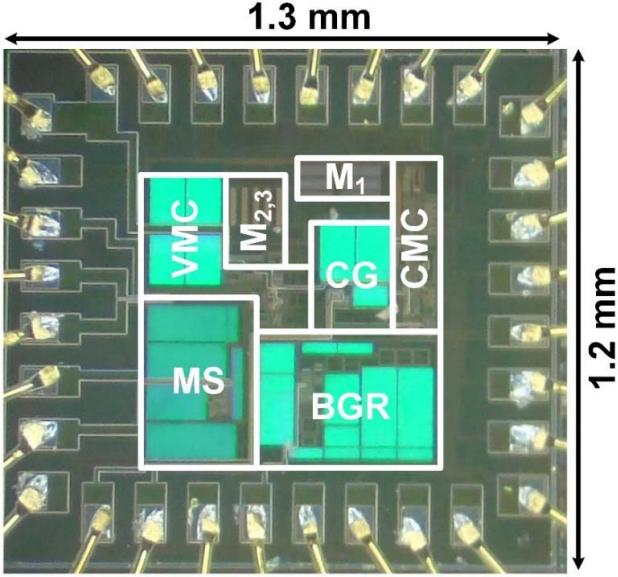


Fig. 12. VCIPM chip micrograph, occupying 1.56 and 0.52 mm² with and without pads, respectively.

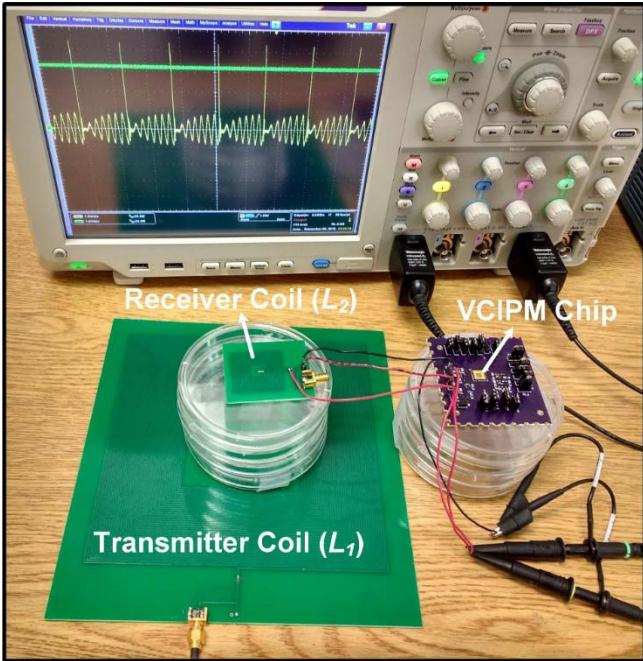


Fig. 13. VCIPM chip measurement setup showing Tx (L_1) and Rx (L_2) PCB coils. The VCIPM chip was operated at $f_p = 1$ MHz to provide a regulated V_L of 3.2 V across $C_L = 2 \mu\text{F}$. Inductive link specifications are listed in Table II.

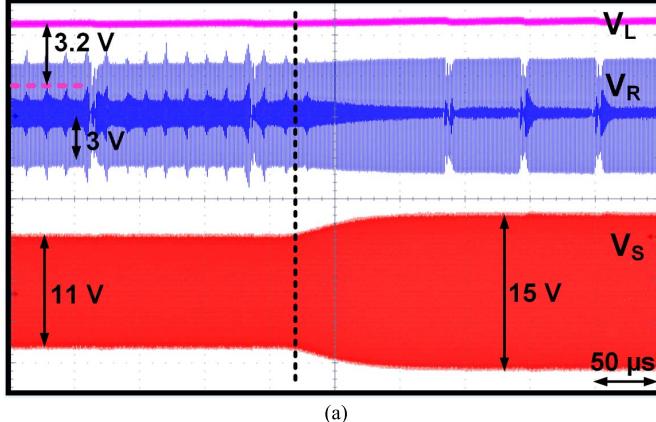
Fig. 14(a) and (b) shows the measured V_L and V_R waveforms with different time scales in VM at $R_L = 100 \text{ k}\Omega$ when the Tx voltage (V_s in Fig. 9) was increased from 11 to 15 V peak-to-peak, demonstrating that despite V_s increase, the VCIPM chip adaptively adjusted the width of SW_2 pulses and consequently the amount of reverse currents to regulate V_L at 3.2 V. For lower $V_s = 11 \text{ V}_{\text{p-p}}$, since R_L of 100 kΩ was very large, which demanded ultralow power in each cycle, and the incoming power was moderate, the chip generated large reverse currents every $\sim 125 \mu\text{s}$ whenever V_L

TABLE II
INDUCTIVE LINK SPECIFICATIONS USED IN MEASUREMENTS

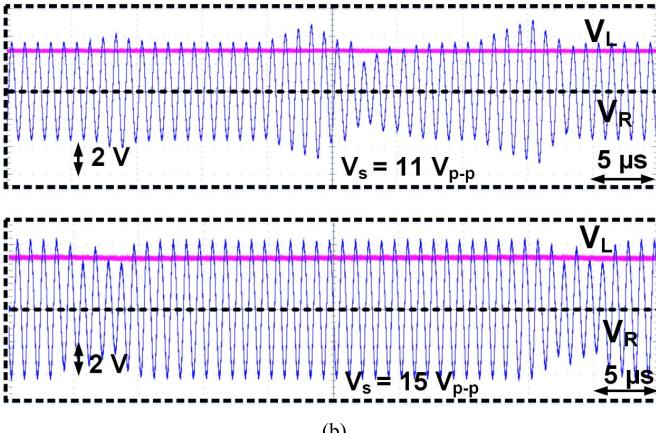
	Parameter	Symbol	Value
L_1	Inductance (μH)	L_1	250
	Outer diameter (mm)	D_{o1}	170
	Number of turns	n_1	35
	Line width (mm)	w_1	1.2
	Line spacing (mm)	s_1	0.2
	Quality factor	Q_1	62
L_2	Inductance (μH)	L_2	4.4
	Outer diameter (mm)	D_{o2}	30
	Number of turns	n_2	14
	Line width (mm)	w_2	0.6
	Line spacing (mm)	s_2	0.2
	Quality factor	Q_2	29
Nominal coupling distance (cm)		d	6
Operation frequency (MHz)		f_p	1
Max switching frequency (kHz)		f_{sw}	166.6
Nominal load resistance (kΩ)		R_L	100
Load capacitance (μF)		C_L	2

exceeded 3.2 V that resulted in a sudden voltage drop in V_R for several cycles to slightly reduce V_L below 3.2 V. As shown in Fig. 12(a), since the Rx LC-tank received more power at $V_s = 15 \text{ V}_{\text{p-p}}$, VCIPM chip employed reverse current more frequently, seen as sudden decreases in V_R , to regulate V_L . Since $V_{R,\text{peak}}$ was higher than 3.3 V, the chip automatically operated in VM. It should also be noted that thanks to the proposed reverse-current regulation, V_R amplitude was maintained fairly constant despite V_s increase.

Fig. 15 shows the VCIPM chip response in VM to significant R_L variations. As R_L was increased by 10× from 1 to 10 kΩ, V_L remained fairly constant at 3.2 V with small ripples of 100 mV_{p-p} by increasing reverse current. Whenever V_L was increased above 3.2 V, large reverse currents were generated by the chip that resulted in sudden and fast drops in V_R . At larger R_L of 10 kΩ with the same input power, C_L was discharging more slowly and, therefore, the VCIPM chip generated reverse currents more frequently (every $\sim 25 \mu\text{s}$) to maintain V_L constant at 3.2 V. Again, it can clearly be seen that despite R_L increase by 10×, V_R amplitude remained fairly constant, protecting the chip against potential large voltages in conventional power managements, as seen in Fig. 4. Fig. 15 shows rectification, regulation, and OVP all in one step for $R_L = 10 \text{ k}\Omega$. In order to further reduce voltage ripples across V_L in VM, Reg_Amp in Fig. 10(a) should be designed for higher gain and bandwidth at the cost of more power consumption. However, in general, the proposed reverse-current technique for regulation adds more ripples compared with conventional techniques that adjust the forward current, because C_L is first charged every cycle with maximum forward current and then extra charge is removed by the reverse current.



(a)



(b)

Fig. 14. (a) Measured V_L and V_R waveforms in VM when the Tx voltage (V_s in Fig. 1) was increased from 11 to 15 V_{p-p} at $R_L = 100 \text{ k}\Omega$. (b) Zoomed-in view of waveforms for V_L and V_R , demonstrating how reverse current regulated V_L at 3.2 V despite V_s variations.

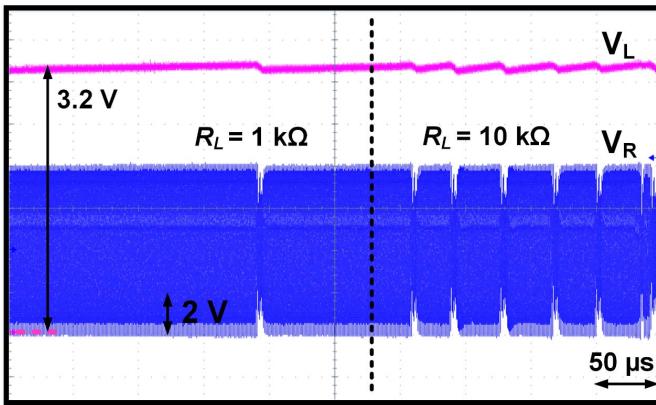
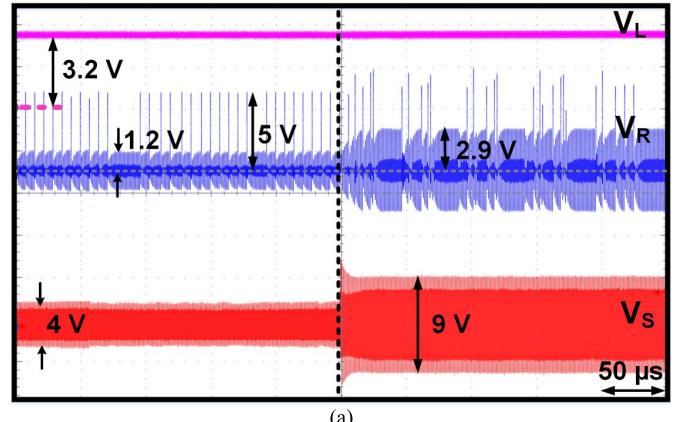
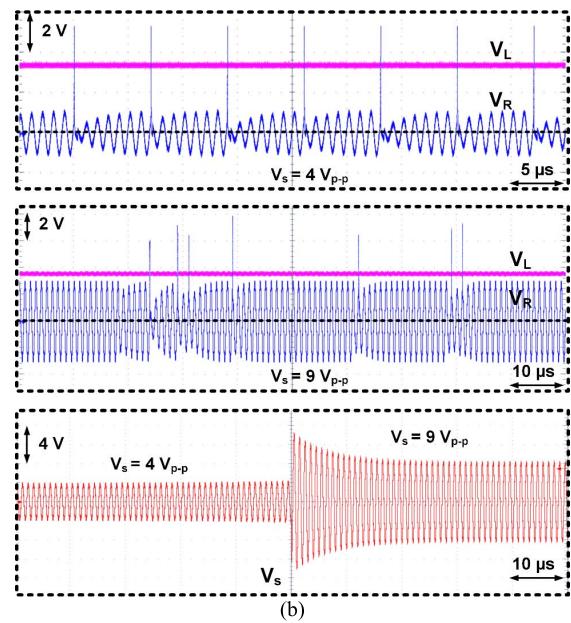


Fig. 15. Measured V_L and V_R in VM when R_L was increased from 1 to 10 kΩ. Thanks to increase in the reverse current, V_L was maintained constant at 3.2 V with small ripples of 100 mV_{p-p} despite 10x increase in R_L .

Fig. 16(a) and (b) shows the measured V_L , V_R , and V_s waveforms with different time scales in CM at $R_L = 100 \text{ k}\Omega$ when V_s was increased from 4 to 9 V_{p-p}, demonstrating that for $V_s = 4 \text{ V}_\text{p-p}$: 1) since $V_{R,\text{peak}}$ was 1.2 V in steady state without switching ($< V_{DD} = 3.2 \text{ V}$), the chip automatically operated in CM and 2) V_R jumped from 1.2 to $\sim 5 \text{ V}$ by turning M_1 off with proper SW_1 pulses to charge C_L to 3.2 V. Despite V_s increase to 9 V_{p-p}, in which $V_{R,\text{peak}}$ increased



(a)



(b)

Fig. 16. (a) Measured V_L and V_R waveforms in CM when V_s was increased from 4 to 9 V_{p-p} at $R_L = 100 \text{ k}\Omega$. (b) Zoomed-in view of waveforms for V_L , V_R , and V_s demonstrating how changes in f_{sw} regulated V_L at 3.2 V despite V_s variations.

to 2.9 V (still below 3.3 V), the VCIPM chip remained in CM configuration and adaptively adjusted f_{sw} to regulate V_L at 3.2 V. As shown in Fig. 16(b), at lower V_s of 4 V_{p-p}, resulting in less power delivered to Rx, the chip generated SW_1 pulses at the highest f_{sw} of 166.6 kHz to more frequently charge C_L . In contrast, at higher V_s of 9 V_{p-p} with increased received power, f_{sw} was automatically decreased to charge C_L less frequently and regulate V_L at 3.2 V. It should be noted that the proposed VCIPM chip achieved a high VCE of 2.7 V/V at $V_s = 4 \text{ V}_\text{p-p}$. Nonetheless, the maximum measured VCE in VCIPM chip was 4.1 V/V at $f_{sw} = 166.6 \text{ kHz}$, $R_L = 100 \text{ k}\Omega$, $V_L = 3.2 \text{ V}$, and steady-state $V_{R,\text{peak}}$ of 0.78 V.

Fig. 17 shows measured V_L and V_R waveforms in CM when R_L was significantly increased by 10x from 10 to 100 kΩ. At smaller R_L of 10 kΩ that demanded more power, the chip adjusted f_{sw} to its maximum of 166.6 kHz to constantly charge C_L and consequently regulate V_L at 3.2 V. In contrast, for larger R_L of 100 kΩ that gradually discharged C_L , demanding less power, f_{sw} was adjusted properly by frequently

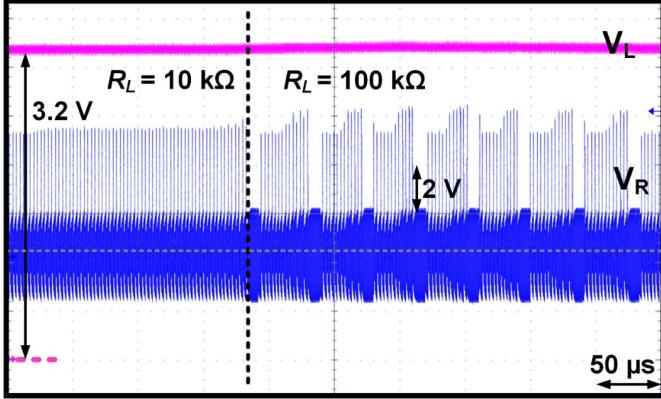


Fig. 17. Measured V_L and V_R waveforms in CM for R_L variations from 10 to $100 \text{ k}\Omega$, demonstrating automatic f_{sw} adjustment to regulated V_L at 3.2 V.

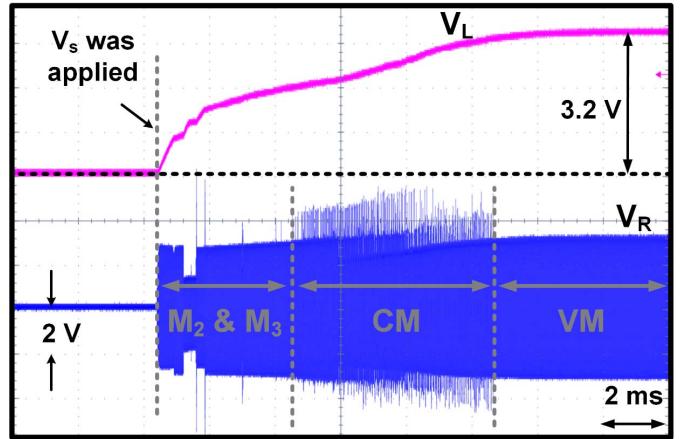


Fig. 19. Measured V_L and V_R waveforms during VCIPM chip startup, in which M_2 and M_3 first slowly charged C_L to $\sim 2 \text{ V}$, followed by CM and VM operations to further increase V_L to 3.2 V.

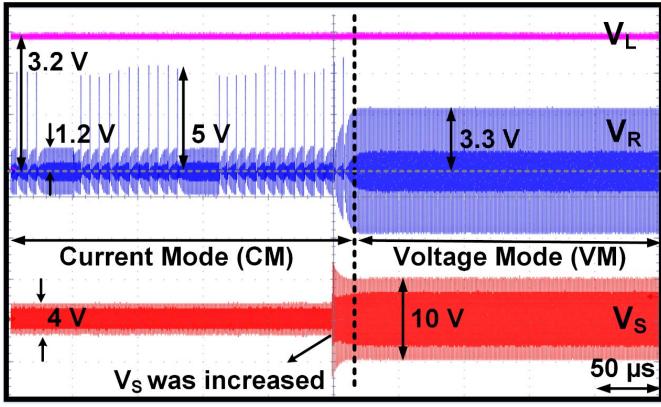


Fig. 18. Measured V_L , V_R , and V_s waveforms when V_s was manually increased from 4 to $10 \text{ V}_{\text{p-p}}$, resulting in the automatic reconfiguration of the VCIPM chip from CM to VM based on the V_R amplitude (1.2 versus 3.35 V) to regulate V_L at 3.2 V.

eliminating large charging pulses of V_R for $\sim 10 \mu\text{s}$ to regulate V_L at 3.2 V with small ripples of $10 \text{ mV}_{\text{p-p}}$. Fig. 17 clearly shows that V_L remained constant at 3.2 V with $10\times$ increase in R_L . Comparing Figs. 13 and 15 shows that voltage ripples in CM are much smaller than those of VM due to the lack of reverse current in self-regulation. In other words, CMC charges C_L as much as needed while VMC might overcharge C_L and then discharge it, increasing ripples.

Fig. 18 shows automatic reconfiguration of the VCIPM chip from CM to VM when V_s was suddenly increased from 4 to $10 \text{ V}_{\text{p-p}}$ in measurements with $R_L = 100 \text{ k}\Omega$. At lower $V_s = 4 \text{ V}_{\text{p-p}}$, the steady-state $V_{R,\text{peak}}$ was 1.2 V and, therefore, the chip operated in CM to regulate V_L at 3.2 V by large $V_{R,\text{peak}}$ of $\sim 5 \text{ V}$, i.e., operating with high VCE of 2.7 V/V . As V_s was increased to $10 \text{ V}_{\text{p-p}}$, $V_{R,\text{peak}}$ was gradually increased to 3.35 V after $\sim 15 \mu\text{s}$ (higher than required V_{DD} of 3.2 V), in which the VCIPM chip automatically changed its configuration to VM. Fig. 18 clearly shows that V_L remained constant at 3.2 V for a drastic change in V_R amplitude.

Fig. 19 shows measured V_L and V_R waveforms during VCIPM chip startup at $R_L = 100 \text{ k}\Omega$. When V_s was applied to Tx, V_L was zero, M_1 was off, and C_L was initially

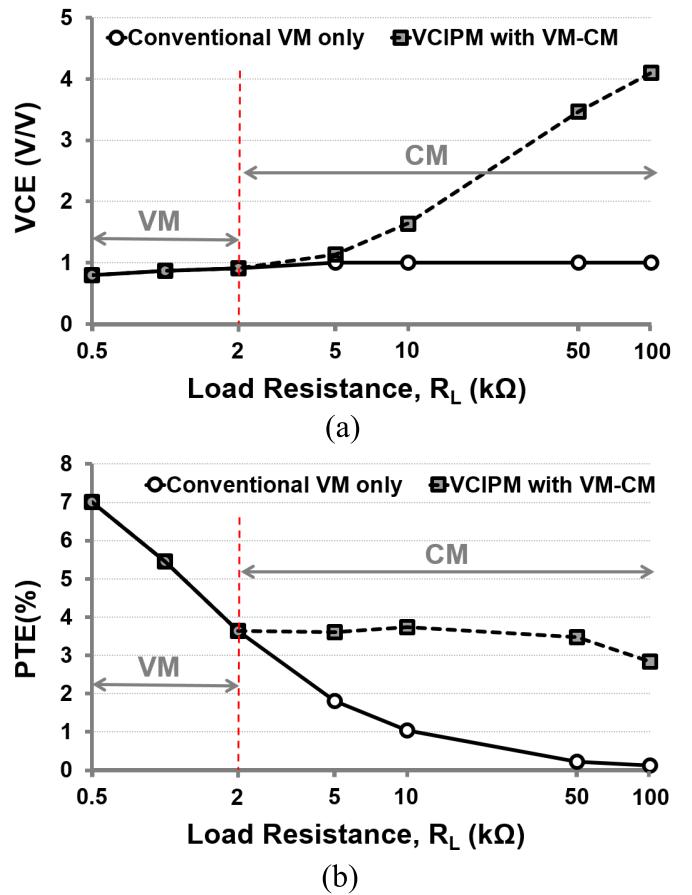


Fig. 20. Measured (a) VCE and (b) PTE versus R_L for conventional VM-only and the VCIPM chip at $d = 4.5 \text{ cm}$ and $f_p = 1 \text{ MHz}$. The VCIPM chip reconfigured itself from VM to CM at $R_L \sim 2 \text{ k}\Omega$ to achieve highest VCE and PTE at larger R_L .

charged through M_3 . When V_L was charged to $\sim 0.6 \text{ V}$, close to M_1 threshold voltage, M_1 was slightly turned on and M_2 significantly helped M_3 to further charge C_L . At $V_L = 2 \text{ V}$, the VCIPM chip became fully functional and operated in CM since $V_{R,\text{peak}}$ was $\leq 3.3 \text{ V}$. In the VCIPM chip, CG and BGR blocks in Fig. 9 require at least V_L of 2 V to generate correct

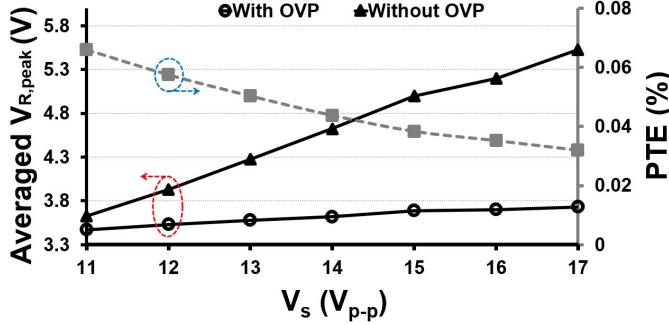


Fig. 21. Measured $V_{R,peak}$ with and without OVP as well as PTE versus V_s in VM at $R_L = 100 \text{ k}\Omega$ and $d = 6 \text{ cm}$. As V_s is increased, the VCIPM chip enables OVP to increase reverse currents and consequently reduce the PTE to maintain V_R within safe regions.

voltage and current biases, which are key in the CM operation. As $V_{R,peak}$ was increased to $> 3.3 \text{ V}$, the chip switched to VM and regulated V_L at 3.2 V . As shown in Fig. 19, the VCIPM chip started up within $\sim 16 \text{ ms}$.

Fig. 20(a) and (b) compares the measured VCE and PTE values between conventional VM and VCIPM chip versus different R_L values of $0.5\text{--}100 \text{ k}\Omega$ at $d = 4.5 \text{ cm}$ and $f_p = 1 \text{ MHz}$, respectively. In VM-only measurements, the VCIPM chip was manually configured to VM by disabling CM, in which M_1 was externally turned on to operate the power management as a conventional active rectifier. It can be seen in Fig. 20(a) and (b) that the VCIPM chip could significantly improve both VCE and PTE, particularly at large $R_L > \sim 2 \text{ k}\Omega$, thanks to reconfiguring itself to CM. For instance, at $R_L = 100 \text{ k}\Omega$ the measured VCE and PTE of the VCIPM chip were 4.1 (4.1 versus 1 V/V) and 21 (2.8% versus 0.13%) times larger compared with the VM, respectively. At large R_L , VM achieves poor $Q_{2L}/Q_L(\eta_{Rx})$ and consequently low PTE, because most of the received power is wasted in R_2 [36]. Using inductive link specifications in Table II, calculated $Q_L = 3.6 \times 10^3$ and $Q_{2L} = 28.8$ at R_L of $100 \text{ k}\Omega$ for VM that leads to the poor η_{Rx} of 0.8%. However, as shown in Fig. 8(a), CM can effectively match the load by improving $Q_{2L,\text{eq}}/Q_{L,\text{eq}}$ with high f_{sw} . In contrast, at small R_L better load matching is provided by VM, since equivalent parallel resistance of the Rx LC-tank is in range of kilohm and below [36], and power is also delivered to R_L with more efficient active rectifier. Nonetheless, the VCIPM chip achieves highest possible VCE and PTE for a wide range of R_L by optimally selecting the operation mode.

Fig. 21 shows measured averaged $V_{R,peak}$ versus V_s in VM with and without OVP, as well as measured PTE with OVP for $R_L = 100 \text{ k}\Omega$ at $d = 6 \text{ cm}$. The $V_{R,peak}$ values with OVP were averaged, because the V_R envelope has small variations due to reverse currents, as shown in Fig. 14(b). For a V_s increase from 11 to 17 V_{p-p}, $V_{R,peak}$ slightly increased for only $\sim 0.2 \text{ V}$ with OVP, compared with the significant $V_{R,peak}$ increase of 1.9 V without OVP. Therefore, OVP with the reverse current is quite effective. As shown in Fig. 21, the measured PTE was decreased from $\sim 0.07\%$ to 0.03% for a V_s increase from 11 to 17 V_{p-p}, because the received power was exceeding the required power for generating the

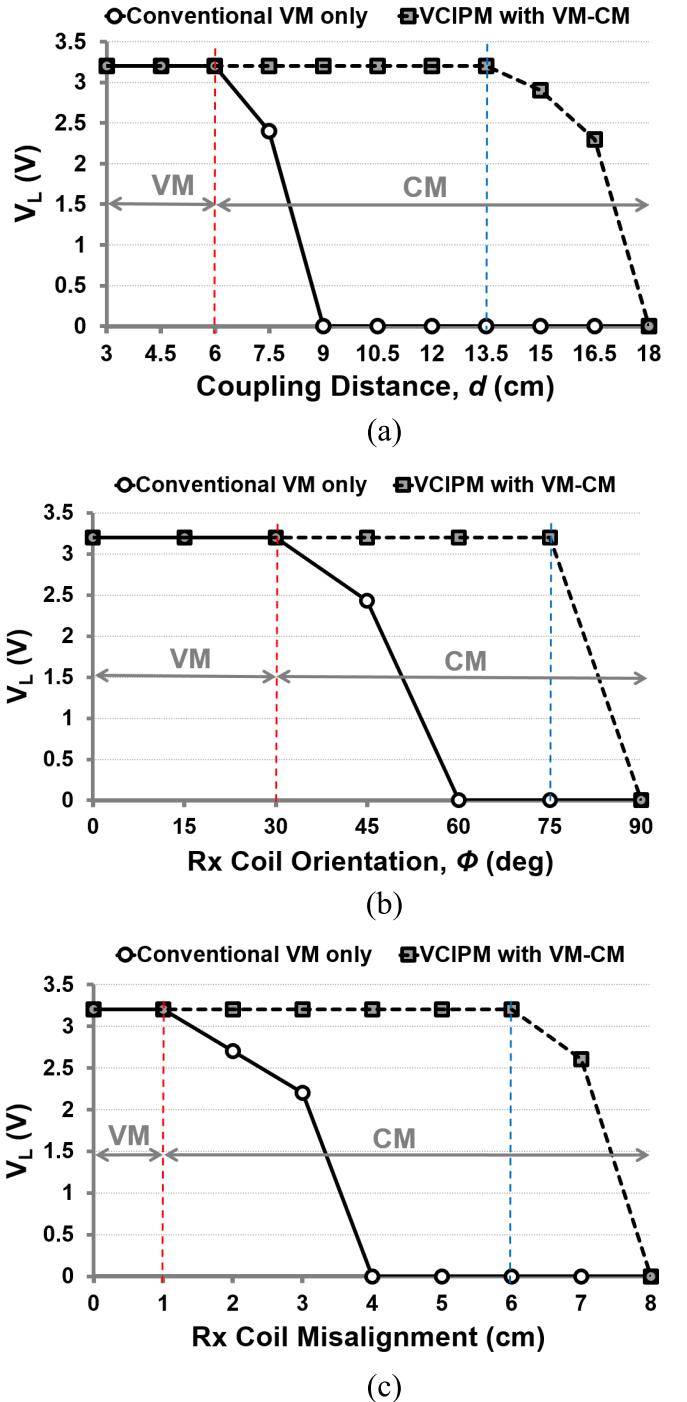


Fig. 22. Measured V_L versus (a) coupling distance d , (b) Rx coil orientation ϕ , and (c) Rx coil misalignment for conventional VM-only and VCIPM chip at $R_L = 100 \text{ k}\Omega$ and fixed input power of 145 mW . The proposed VCIPM could extend d , ϕ , and misalignment robustness for 125%, 150%, and 500%, respectively.

constant V_L of 3.2 V and, therefore, PTE was intentionally reduced by regulation and OVP blocks using reverse currents to maintain V_L at 3.2 V and also protect the chip against high voltages. Such PTE reduction due to regulation or OVP is not an issue, since the regulation block optimizes the rectifier performance to achieve constant V_L of 3.2 V , and OVP operates only when the received power is too high. Nonetheless, the highest measured PCE of the rectifier in

TABLE III
BENCHMARKING THE VCIPM CHIP AMONG STATE-OF-THE-ART INDUCTIVE POWER MANAGMENTS

Publication	ISSCC 2012, [26]	CICC 2015, [27]	VLSI 2016, [28]	JSSC 2017, [23]	ISSCC 2015, [33]	ISSCC 2016, [35]	This Work
CMOS Tech (μm)	0.5	0.18	0.18	0.35	0.35	0.18	0.35
Application	WPT	WPT	WPT	WPT	WPT	Battery Charger	WPT
Rx Structure	VM	VM	VM	CM	CM	CM	VM-CM
Frequency (MHz)	13.56	15	144	6.78	2	0.05	1
Max VCE (V/V) @ R_L ($\text{k}\Omega$)	0.84/1.4* @0.5	1.67* @0.77	-	~0.9 @ 5×10^{-3}	0.83 @0.1	-	4.1 @100
Max PCE (%) @ P_L (mW)	77 @19	87.7 @33	66.5 @0.15	92.2 @6000	87.1 @220	61.2 @0.0028	77 @10
Self-Startup	Yes	Yes	Yes	Yes	Yes	No	Yes
Self-Regulation	No	Yes	Yes	Yes	No	-	Yes
Range Extension (%)	33	-	-	-	-	-	125
Line Regulation (%)	-	-	-	-	-	-	VM: 0.8 CM: 2.5
Load Regulation (%)	-	<2.5	1.12	-	-	-	VM: 0.75 CM: 2.2
Active Area (mm^2)	0.585	0.112	-	~4.77	~4.8	0.54	0.52
Over-Voltage Protection (OVP)	No	No	No	Yes	Yes	No	Yes
Output Power Range (mW)	6-37	0.6-90	0.02-0.2	500-6000	50-1450	0.0006-0.0028 ⁺⁺	0.1-20
**Off-Chip Capacitors	4	3	- ⁺	2	4	-	2

*Voltage doubler.

**Capacitors for Rx resonance, rectification, regulation, and OVP.

⁺Due to high operating frequency and small output power, capacitors are implemented on-chip.

⁺⁺At the receiver coil.

VM was 77% at R_L of 100 $\text{k}\Omega$, when there was no reverse current.

Fig. 22(a)-(c) compares measured V_L in conventional VM and VCIPM chip versus d , Rx coil's orientation (ϕ), and misalignment at $R_L = 100 \text{ k}\Omega$ and fixed input power of 145 mW, respectively. Fig. 22(a) shows that for generating a constant V_L of 3.2 V at the same V_s , the VCIPM chip could extend d from 6 to 13.5 cm for 125%, because at $d > 6$ cm the VCIPM chip employed the CM configuration with high VCE to provide $V_L = 3.2$ V. As shown in Fig. 22(b), the VCIPM chip could extend ϕ for 150% from 30° to 75°, thanks to the CM operation. Finally, the VCIPM chip improved robustness against Rx coil misalignment at $d = 6$ cm for 500% from 1 to 6 cm. In Figs. 20 and 22, the operation of the VCIPM chip in CM has only been compared with VM-only in some regions with small V_R , because operating in CM with large V_R can potentially damage the chip by creating large voltage peaks across L_2 . However, in our previous work using discrete components [36], we compared the operation of CM-only with VM-only for different d and R_L conditions.

Table III benchmarks the VCIPM chip against state-of-the-art inductive power management ASICs. To the best of our knowledge, the VCIPM chip offers the first integrated power management that employs both VM and CM configurations adaptively during the operation, which is suitable for inductively powered systems with variable coupling distance, orientations, misalignment, and loading. In our proof-of-concept VCIPM chip prototype, operating at 1 MHz, maximum VCE and PCE of 4.1 V/V and 77% were achieved inside Rx at R_L

of 100 $\text{k}\Omega$ and P_L of 10 mW, respectively. Designing a full-wave rectifier for increased P_L can further improve the PCE in the future implementation of this chip. The VCIPM chip extended d for 125% thanks to operation in CM and could achieve rectification, regulation, and OVP with a single off-chip capacitor of $C_L = 2 \mu\text{F}$ with measured line and load regulations of 0.8% and 0.75% in VM and 2.5% and 2.2% in CM, respectively. Employing reverse current for regulation and OVP was presented for the first time that differs in principle with conventional regulating rectifiers that adjust forward current with pulse-width/frequency modulation [24], [28].

V. CONCLUSION

We have presented the theory, first ASIC implementation, and measurement results of a reconfigurable VM and CM power management with self-regulation for inductive power transmission. The VCIPM chip could achieve high VCE and PCE by operating in CM and VM, respectively. The VCIPM chip could also increase the inductive link PTE for large R_L by dynamic load transformation in CM configuration. Adjusting reverse current in VM and f_{sw} in CM, regulation and OVP could be achieved along with rectification, eliminating the need for two off-chip capacitors. The VCIPM chip was fabricated in a 0.35- μm standard CMOS process and could provide a 3.2-V regulated output across a 2- μF capacitor with safe received ac voltages under large input power, loading, coupling distance, and coils' orientation variations. The VCIPM chip achieved a maximum VCE of 4.1 V/V and

extended the range by 125% while requiring only two off-chip capacitors for energy storage and resonance.

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