

A 36-V 49% Efficient Hybrid Charge Pump in Nanometer-Scale Bulk CMOS Technology

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Abstract—This paper introduces a hybrid charge pump (HCP) architecture. The HCP enables high-voltage dc outputs in a nanometer-scale CMOS technology at improved power efficiency by optimally mixing different charge pump (CP) types that trade off voltage range and power efficiency. Conventional CP outputs in a bulk CMOS process are limited to a single-diode breakdown voltage (~ 12 V in a 65-nm technology node). To support > 12 V outputs, the HCP extends the voltage tolerance of bulk CMOS substrates via two technology methods: double-diode substrate isolation and field oxide isolation. To enable these isolation methods, two specialized CP cells are devised: an all-nMOS voltage doubler and an improved-drive Dickson-type pump. Two HCP design examples with opposite voltage polarities are implemented in a 65-nm CMOS technology, and their measurement results are discussed. The positive voltage HCP achieves a 36 V output and 49% peak efficiency at a $20\text{-}\mu\text{A}$ load current and occupies 0.18 mm^2 in area. This output voltage represents a $3\times$ increase in the technology's voltage range compared to ranges attainable by conventional designs.

Index Terms—All-nMOS charge pump (CP), device stacking, double-diode substrate isolation, high voltage, hybrid CP (HCP), polysilicon diode.

I. INTRODUCTION

HIGH-VOLTAGE signals are ubiquitous in many of today's electronic systems. Many sensors, actuators, and output devices require dc or switching waveforms with amplitudes that are substantial multiples of a technology's nominal supply voltage (V_{dd}). Often, $>V_{dd}$ voltages are required to enable a device's functionality or improve a system's performance. An example of the latter is found in microelectromechanical system (MEMS)-based oscillators, where biasing the MEMS resonator at a higher dc voltage improves its charge sensitivity and reduces its phase noise contribution [1], [2]. Improved phase noise performance helps MEMS-based timing solutions better meet the tough jitter requirements of many high-end timing applications, e.g., cellular, GPS, and high-speed serial links. Another example is found in ultrasonic transducers, where higher transmit voltages

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help relax the link's budget or enable longer ranges of operation [3]. In both applications, >30 V voltages are not uncommon. To accommodate such voltage levels, older CMOS technology nodes, multichip solutions, or exotic technologies (e.g., silicon on insulator (SOI) and Bipolar-CMOS-DMOS) are typically used [4]–[9]. These choices often increase the system's size and cost or impede the smooth porting of older fully-integrated solutions into better scaled technology nodes. Standard nanometer-scale CMOS technology, on the other hand, allows smaller lower cost electronics with faster and reduced power implementations, yet suffers from diminishing voltage tolerances. For example, the voltage tolerance of a CMOS substrate, mainly determined by its wells' breakdown voltages, is merely ~ 12 and ~ 9 V in 65-nm and 22-nm technology nodes, respectively.

In this paper, we introduce technology and circuit techniques that extend the voltage range of a standard CMOS process while maintaining device and substrate reliability. To increase the substrate's voltage tolerance, we present two substrate isolation methods. First, we introduce a modified well-biasing scheme in a triple-well technology. This modified well bias leverages the technology's deep n-well layer to enable double-diode substrate isolation, as opposed to conventional single-diode isolation designs. Second, to further extend our voltage range, we rely on the isolation of the field oxide (FOX) layer. Since only fairly simple polysilicon and metal structures can be supported on top of the substrate's FOX, we rely on polysilicon p-i-n diodes on top of a deep n-well for our switch implementation. These polysilicon diode switches are used to implement a high-voltage charge pump (CP) circuit akin to the Dickson CP [10]. To enable these two substrate isolation methods, a specialized CP type needs to go hand in hand with each isolation method. Accordingly, we introduce an efficient all-nMOS six-phase voltage doubler (6PVD) in deep n-well, and a polysilicon diode CP with double-stacked clock drivers for improved efficiency. Since higher voltage pumps suffer from lower power efficiency, we introduce the hybrid CP (HCP) architecture. The HCP cascades different pump cell types that gradually tradeoff power efficiency and voltage range. By eliminating inefficient higher voltage-range cells from the pump's first stages and replacing them with more efficient lower voltage-range cells, the HCP achieves a higher overall efficiency than otherwise feasible using a nonhybrid approach.

This paper is organized as follows. In Section II, we describe methods for extending the voltage range of a CMOS substrate beyond conventional limits dictated by different wells' breakdowns. In Section III, we introduce the HCP

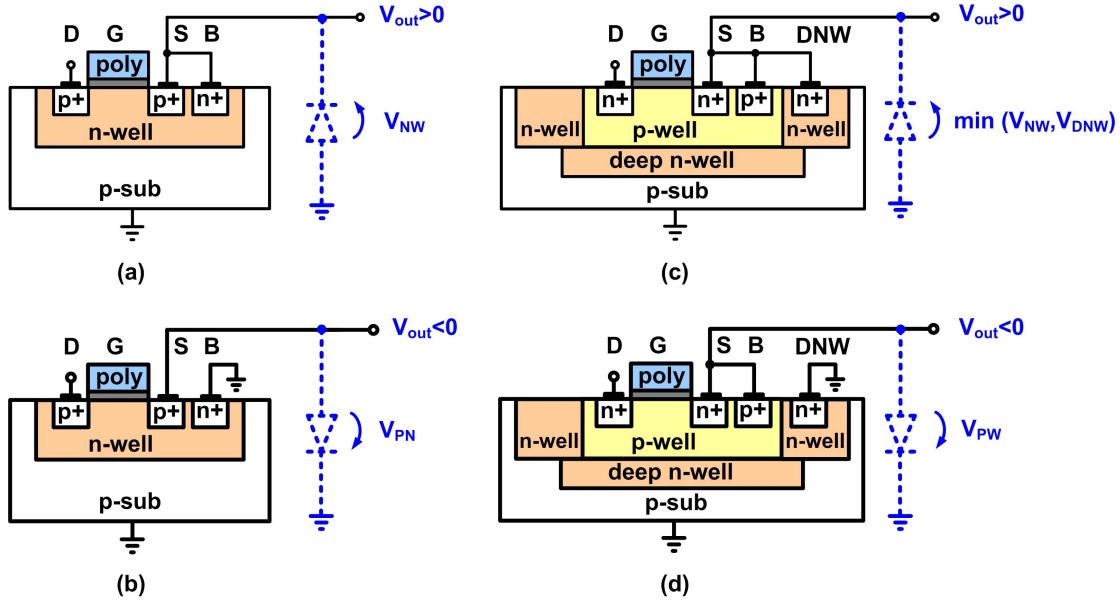


Fig. 1. CMOS substrate breakdown limits for different switch types and voltage polarities. (a) pMOS switch and positive polarity. (b) pMOS switch and negative polarity. (c) nMOS switch and positive polarity. (d) nMOS switch and negative polarity.

architecture and provide two design implementations having opposite polarities in a 65-nm CMOS technology. In Section IV, we delve into the circuit implementation details of the HCP designs. And in Section V, we discuss the measurements results of the test chip prototypes.

II. EXTENDED VOLTAGE RANGE CMOS SUBSTRATES

Thanks to a voltage-tolerant buried oxide (BOX) layer, SOI CMOS is an attractive technology for high-voltage applications. Fundamentally limited by their BOX breakdown, a number of high-voltage CPs have been demonstrated in SOI CMOS technology [7]–[9]. However, SOI CMOS is not as low cost or as aggressively scaled as mainstream bulk CMOS technology. In this section, we explain how to utilize existing technology features in a standard bulk CMOS process to expand the voltage range of CPs beyond what is currently possible with conventional designs.

A. Double-Diode Substrate Isolation

Higher dc voltages are attainable by cascading more pump stages at the cost of decreasing power efficiency. The maximum pump voltage, however, is ultimately limited by the substrate's maximum handling voltage. This maximum voltage is set by the reverse breakdown voltage of one of the substrate diodes. Table I summarizes the different substrate diodes in a triple-well 65-nm CMOS process and their approximate breakdown voltages. Which substrate diode clamps the final pump output depends on the type of transistor switch and the pump's voltage polarity [11]. Shown in Fig. 1 are four different scenarios involving two switch types and two voltage polarities. First, we consider the case of a pMOS switch. For the positive voltage scenario in Fig. 1(a), the transistor bulk and source terminals must be shorted together to prevent a forward body diode. Consequently, the substrate's voltage tolerance is

TABLE I
APPROXIMATE BREAKDOWN VOLTAGES OF DIFFERENT SUBSTRATE DIODES IN A 65-nm CMOS TECHNOLOGY

Symbol	Breakdown Voltage	Description
V_{NP}	9 V	n+ to p-well diode
V_{PN}	9 V	p+ to n-well diode
V_{NW}	12 V	n-well to p-sub diode
V_{PW}	12 V	p-well to deep n-well diode
V_{DNW}	12 V	deep n-well to p-sub diode

is limited by the breakdown voltage of the n-well/p-substrate diode (V_{NW}). Whereas for the negative voltage scenario in Fig. 1(b), the transistor's bulk terminal must be grounded to prevent a forward n-well/p-substrate diode. Accordingly, the substrate's voltage tolerance is limited by the breakdown voltage of the p+/n-well diode (V_{PN}). Next, we consider the case of a deep n-well nMOS switch. Conveniently, to prevent back-gate bias effects, the nMOS bulk and source terminals are always shorted. For the positive voltage scenario in Fig. 1(c), the transistor's deep n-well and bulk terminals must be shorted to prevent a forward p-well/deep n-well diode. Consequently, the substrate's voltage tolerance is limited by the minimum of two voltages, V_{NW} and V_{DNW} , where V_{DNW} is the breakdown voltage of the deep n-well/p-substrate diode. Finally, for the negative voltage scenario in Fig. 1(d), the transistor bulk terminal must be grounded to prevent a forward deep n-well/p-substrate diode. As a result, the substrate's voltage tolerance is

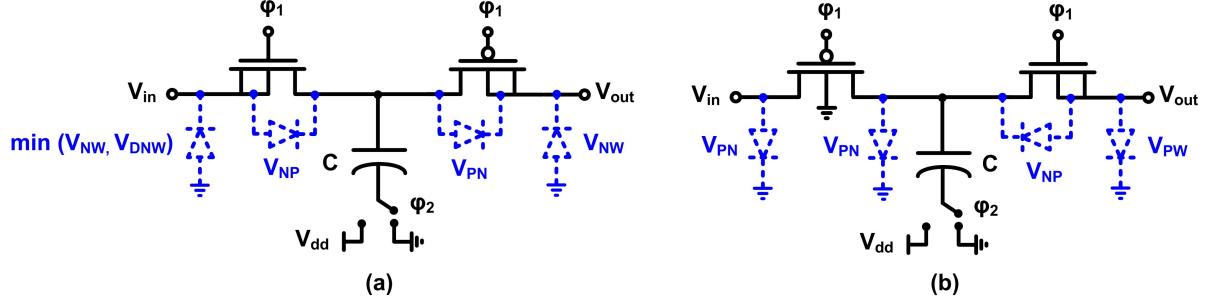


Fig. 2. Simplified CMOS voltage doubler schematics. (a) Positive voltage output. (b) Negative voltage output.

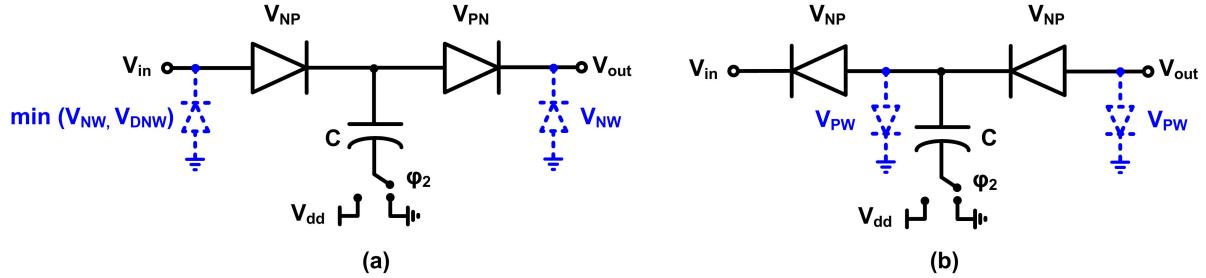


Fig. 3. Simplified Dickson pump schematics. (a) Positive voltage output. (b) Negative voltage output.

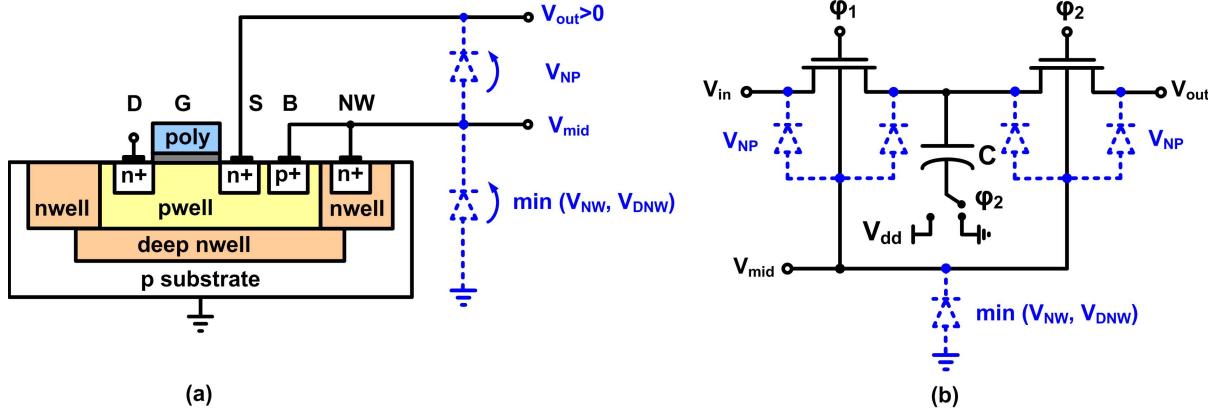


Fig. 4. Double-diode substrate isolation. (a) Process cross section. (b) Simplified voltage doubler schematic.

limited by the breakdown voltage of the p-well/deep n-well diode (V_{PW}).

For the sake of completeness, we also consider the case of a bulk nMOS switch. For the positive voltage scenario, the switch always suffers from back-gate bias effects, and the substrate's voltage tolerance is limited by the breakdown voltage of the n+/p-sub diode (V_{NP}). A negative voltage scenario is not possible here because of the forward biased body diode.

So far, we have only considered the voltage range limitations on individual switch devices in isolation. However, to arrive at a more practical limit on CP ranges, full-stage implementations must be considered. Shown in Fig. 2(a) and (b) are the simplified depictions of commonly used voltage doubler cells having positive and negative polarities, respectively. Each doubler cell has two inputs V_{in} and V_{dd} and two complementary charge transfer switches. In principle,

the switch devices can be of the same type, at the cost of circuit complexity, as we later show. For simplicity, we omit the level shifting circuits necessary to operate the transistors in a charge transfer mode [12]. Moreover, to reduce clutter, the deep n-well terminal for the nMOS switches is omitted from the device symbol, and its bias is always assumed to be in accordance with the rules set forth in Fig. 1(c) and (d). It is assumed that V_{in} can be set arbitrarily—in reality, V_{in} is provided by a preceding voltage doubler stage—and that C has a voltage tolerance well above V_{in} . For the cells to function, two complementary clock phases are needed, ϕ_1 and ϕ_2 . For the positive voltage doubler in Fig. 2(a), during one clock phase, the capacitor's bottom plate is connected to ground and the pumping capacitor (C) is charged to V_{in} . During the second clock phase, the capacitor's bottom plate is connected to V_{dd} and the output voltage is pumped up to $V_{in} + V_{dd}$ to a first order. Given that $V_{NP} > V_{dd}$, it is found that this doubler's maximum

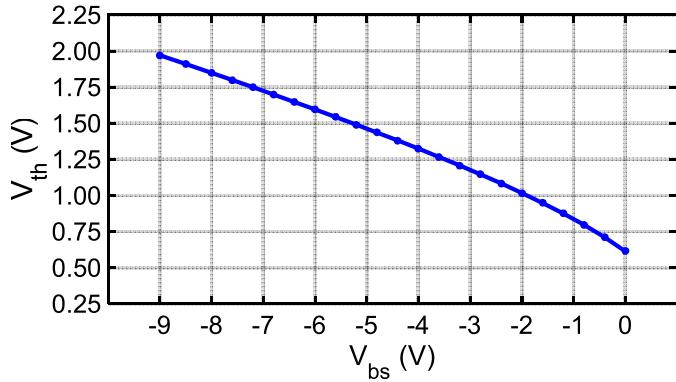


Fig. 5. Simulated threshold voltage of an nMOS device with $W/L = 1.4 \mu\text{m}/0.5 \mu\text{m}$ versus V_{bs} .

range is equal to $\min(V_{NW}, V_{DNW} + V_{dd})$, where $\min(a, b)$ is the minimum of a and b . Similarly, for the negative voltage doubler in Fig. 2(b), during one clock phase, the capacitor's bottom plate is connected to V_{dd} and the capacitor is charged to $V_{in} - V_{dd}$. During the second clock phase, the capacitor's bottom plate is connected to ground and the output voltage is pumped down to $V_{in} - V_{dd}$ to a first order. Given that $V_{NP} > V_{dd}$, it is found that this doubler's maximum negative range is equal to $-\min(V_{PN}, V_{PW})$. A simpler earlier variant of the voltage doubler that uses diodes instead of transistors for switches is the Dickson pump and is depicted for both polarities in Fig. 3(a) and (b). Regardless of the specific diode implementation, e.g., well/body diodes or diode-connected MOS devices, the voltage range of a Dickson pump is still limited by the same breakdown voltages discussed earlier. Note that the p+/n-well diode and the p-well/deep n-well diode cannot be used in negative voltage designs, as the n-well and deep n-well diode terminals must be grounded to prevent forward biased junctions.

Based on the previous discussion and the values in Table I, we observe that the voltage ranges of conventional CP designs in a 65-nm CMOS technology are limited to 12 V and -12 V, for positive and negative polarities, respectively, and are far from the requirements of many high-voltage systems. In an attempt to improve the CMOS substrate voltage tolerance, one method proposed in [13] uses an implant block mask to create a lightly doped p-type buffer region surrounding the n-wells. This buffer region has a reduced doping concentration and results in higher junction breakdown voltages. However, this method is effective in increasing the substrate voltage tolerance by only a few volts.

In this paper, we attain significantly higher substrate tolerances by accumulating the isolation of two series stacked diodes, as opposed to the conventional single-diode substrate isolation practice. This is possible, mainly, because of the additional isolation layer provided by the deep n-well option. To realize double-diode substrate isolation, we choose *not* to short the source and bulk terminals of a deep n-well nMOS device together. Although this defeats the original purpose of the deep n-well, it extends the substrate's voltage tolerance. Instead, we only short the device's bulk and deep n-well terminals together and allow their potential to rise

slowly to an intermediate voltage (V_{mid}), ideally equal to V_{DNW} , as depicted in Fig. 4(a). As a result, the transistor's source/drain potentials can now rise above V_{mid} by another diode breakdown voltage, namely, V_{NP} , and the substrate's new voltage tolerance becomes $V_{DNW} + V_{NP}$. In a 65-nm node, this well-biasing scheme extends a pump's voltage range from 12 to 21 V. However, because of its reliance on a deep n-well layer, this technique can only be used in conjunction with nMOS devices. Consequently, an all-nMOS CP implementation is necessary to enable the double-diode substrate isolation. Shown in Fig. 4(b) is a simplified representation of an all-nMOS voltage doubler cell with all the bulk terminals tied to a common potential V_{mid} . One drawback of this method is that the switches suffer from a larger back-gate bias, resulting in a lower pump efficiency. In the extreme, as more stages are cascaded, even a supply voltage across V_{gs} is not sufficient to turn ON the switch. Shown in Fig. 5 is the simulated threshold voltage (V_{th}) of an nMOS device with $W/L = 1.4 \mu\text{m}/0.5 \mu\text{m}$ in a 65-nm CMOS technology versus its bulk-source potential (V_{bs}). Note that for a 2.5 V device, the supply voltage is still sufficient up to $V_{bs} = -9$ V. It is also noteworthy that double-diode substrate isolation is not compatible with negative voltage pumps since the nMOS deep n-well potential must be grounded to alleviate any forward biased junctions.

B. Field Oxide Isolated p-i-n Diode

To further extend the CP's voltage range, FOX, typically used to better isolate bulk CMOS devices sharing a common substrate, is leveraged to extend the substrate's voltage tolerance. As depicted in Fig. 6, polysilicon devices built on top of FOX are well isolated from the substrate via a few hundred nanometers of oxide and have a maximum handling voltage that is limited by the breakdown of the FOX (V_{FOX}). The use of polysilicon p-i-n diodes to enable a high-voltage Dickson CP in a 0.25- μm CMOS technology has been previously presented in [14]. In our 65-nm technology node, the FOX thickness is ~ 300 nm, and based on measurements, V_{FOX} is found to be ~ 88 V. By inspecting data from the technology files of further scaled process nodes, we find that the FOX thickness scales at a much slower rate than the technology's minimum feature size, rendering FOX isolation a viable method to integrate >20 V dc voltages into nanometer-scale bulk technologies. The drawback, however, is that diode switches suffer from a knee-voltage drop, highlighting again the tradeoff between power efficiency and voltage range. Interestingly, we observe that the voltage range of polysilicon diodes can further extend by combining the FOX with deep n-well isolation. Thus, in our design, the diodes are placed on top of a deep n-well whose bias is as depicted in Fig. 6(a) and (b) for positive and negative voltage polarities, respectively. For positive voltage pumps, we short the p-well (PW) and deep n-well (DNW) terminals together and keep their potential at $V_{mid} = V_{DNW}$, and consequently, the substrate's voltage tolerance extends to $V_{FOX} + V_{DNW}$ (~ 100 V). On the contrary, for negative voltage pumps, the DNW terminal is grounded and the PW potential is kept at $V_{mid} = V_{PW}$, and consequently,

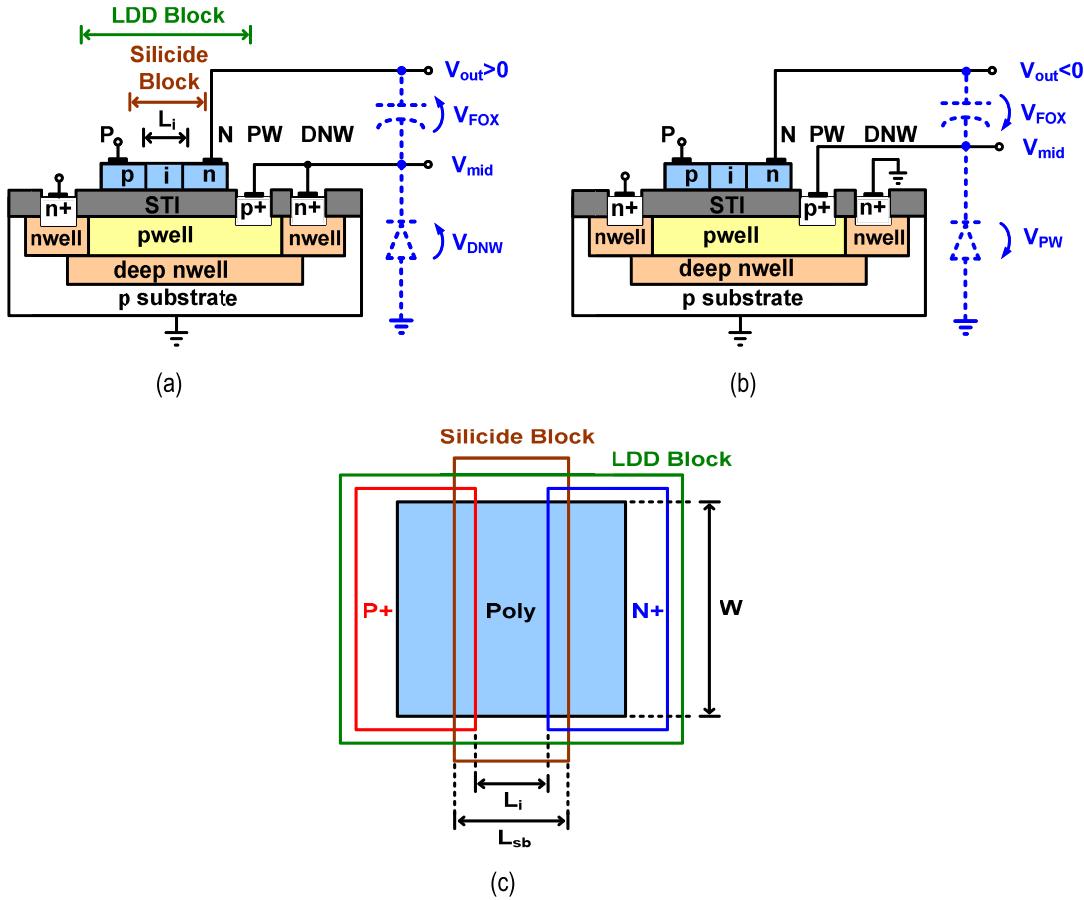


Fig. 6. Polysilicon p-i-n diode on deep n-well well-biasing arrangement for (a) positive voltage pumps, (b) negative voltage pumps, and (c) polysilicon diode layout design.

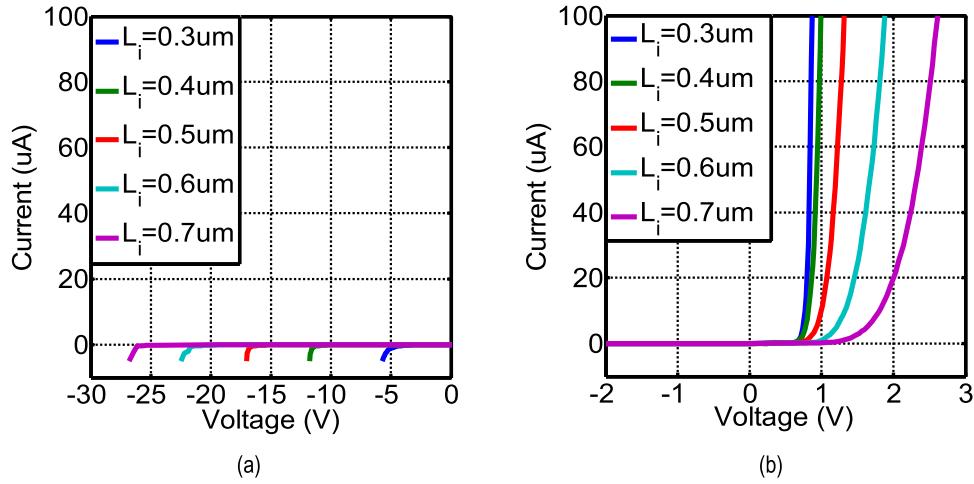


Fig. 7. Measured I - V characteristics of polysilicon diodes with $W = 20 \mu\text{m}$. (a) Reverse bias. (b) Forward bias.

the substrate's voltage tolerance extends to $-V_{\text{FOX}} - V_{\text{PW}}$ ($\sim -100 \text{ V}$).

Although not supported or characterized by traditional CMOS foundries, polysilicon diodes are fully compatible with the standard CMOS process flow and do not require additional processing steps. The diode's layout design is shown in Fig. 6(c). A p-i-n structure is necessary for practical reverse breakdown voltages. The diode's p- and n-type regions

are created using the same implant masks that define the transistor's source and drain regions. The distance between the inner edges of the p- and n-type regions defines the diode's undoped (intrinsic) region length (L_i) and sets its reverse breakdown voltage. A silicide block mask must extend over the intrinsic region boundaries to prevent a shorted diode. Having high-voltage polysilicon regions may result in the creation of undesired inversion layers underneath the FOX. For improved

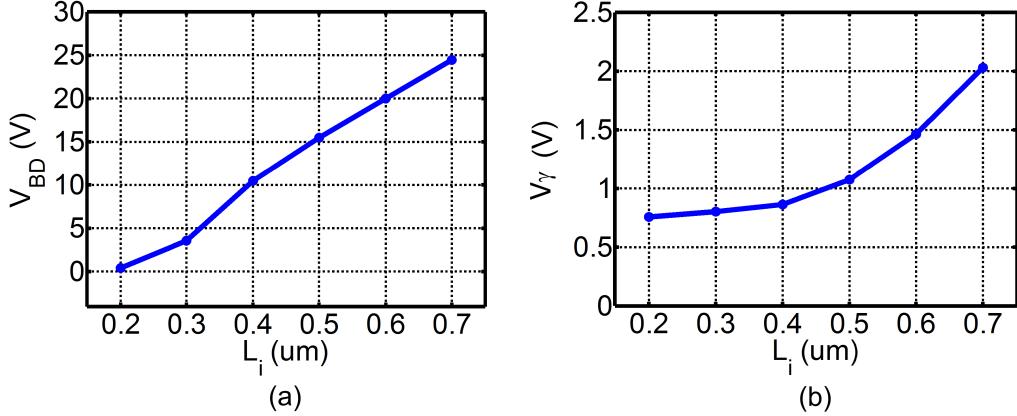


Fig. 8. Measured polysilicon diode parameters versus L_i for $W = 20 \mu\text{m}$. (a) Reverse breakdown voltage. (b) Forward voltage drop.

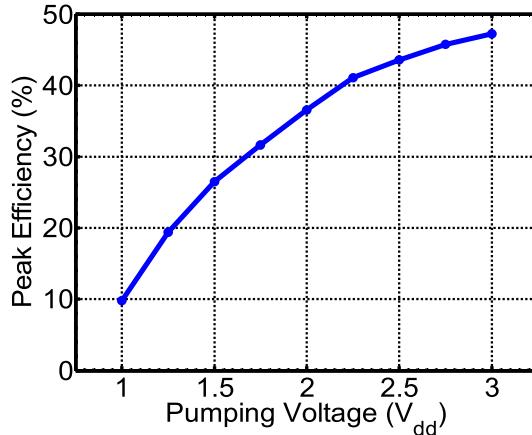


Fig. 9. Measured peak efficiency of a conventional nine-stage polysilicon diode Dickson CP versus V_{dd} .

diode isolation and higher voltage tolerance, the diodes are guarded by a deep n-well. To improve on the variation of diode behavior and dependency on device orientation observed in [15], we use a lightly doped drain block mask to protect the p and n regions from double implants. The measured I - V characteristics of polysilicon p-i-n diodes with a 20- μm width and different L_i values are shown in Fig. 7(a) and (b) for reverse and forward biases, respectively. Diodes with larger L_i exhibit higher reverse breakdown voltages (V_{BD}), yet poorer forward characteristics and a larger knee voltage (V_y). The diodes' measured V_{BD} and V_y versus L_i are shown in Fig. 8(a) and (b), respectively. The diode's V_{BD} is measured at a reverse current of 0.1 μA , while V_y is measured at a forward current of 20 μA .

In a Dickson CP design, the diode's L_i is a critical design parameter and needs to meet certain constraints. The diode's L_i must be chosen small enough for the supply voltage to be able to switch ON the diode (i.e., $V_y < V_{dd}$), yet large enough for the diode to handle the reverse voltage seen when switched OFF (i.e., $V_{BD} > 2V_{dd}$). In the 65-nm technology and V_{dd} of 2.5 V, our measurement results indicate that a suitable design space for L_i is given by $0.35 \mu\text{m} < L_i < 0.6 \mu\text{m}$.

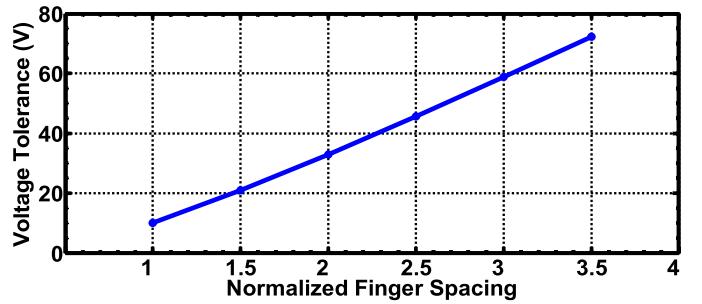


Fig. 10. Estimated voltage tolerances of a 4-pF metal capacitor versus the normalized finger spacing in a 65-nm CMOS technology.

The efficiency of a Dickson CP is a function of its pumping voltage (V_{dd}). To quantify that supply voltage dependence, the measured peak efficiency of a conventional nine-stage Dickson pump, whose polysilicon diodes have $L_i = 0.5 \mu\text{m}$, is plotted versus V_{dd} as shown in Fig. 9. As expected, the pump's peak efficiency improves as V_{dd} increases relative to V_y . We later show how this property is exploited to enhance the efficiency of our improved-drive Dickson design.

C. Voltage-Tolerant Capacitor Design

In high-voltage designs, design for reliability is paramount. Based on the type of CP used, the switches and capacitors can be subjected to voltage stress in a different manner [11]. With an increased stage count, some CP types expose the switches to a progressively higher voltage stress (e.g., heap CP), whereas other types expose the capacitors to a progressively higher voltage stress (e.g., Dickson CP). In our design, we adopt the latter type pump, since integrated transistors have limited voltage ratings set by the reliability of a thin gate oxide. Where possible we opt for thicker oxide IO devices, but these are still limited to <2.5 V operation in this technology. Metal finger capacitors, however, are more voltage tolerant since they have a relatively thicker dielectric separation (>100 nm) that can be adjusted to control the finger spacing and adjust the capacitor's voltage rating.

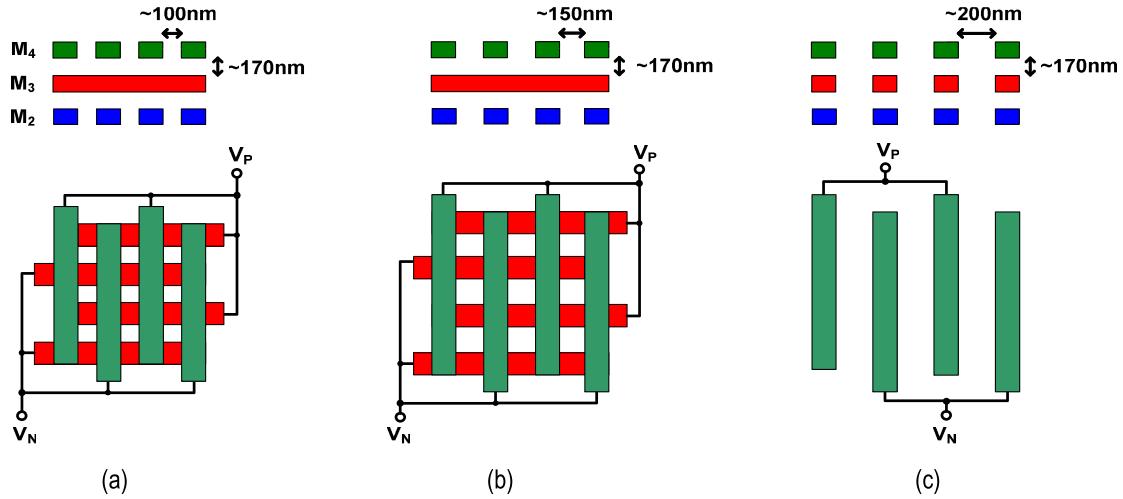


Fig. 11. High-voltage capacitor layout with different finger spacings. (a) 100 nm. (b) 150 nm. (c) 200 nm.

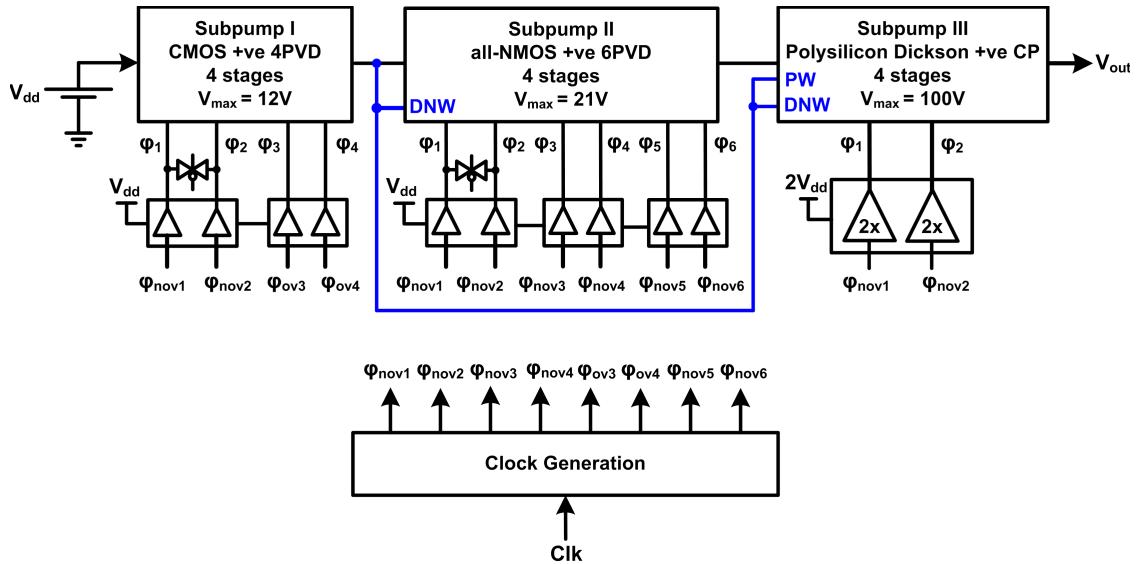


Fig. 12. A +36 V HCP design.

Metal capacitor reliability is mainly determined by time-dependent dielectric breakdown (TDDB) failure rates and is a function of the capacitor's finger spacing. Wider spaced fingers extend the capacitor's voltage rating but increase its parasitic component (C_p), contributing again to the tradeoff between power efficiency and voltage range. Fig. 10 shows the capacitor's estimated rating versus its finger spacing normalized to a minimum value of 100 nm (1×). A 4-pF capacitor with 1× finger spacing is estimated to sustain ~10 V based on a TDDB cumulative failure rate of less than 100 ppm over 10 years at 85 °C. Our TDDB calculations are based on a Weibull statistical distribution, a field accelerated √E-model, an Arrhenius temperature relation, and a Poisson area-scaling model [16], [17]. Layout designs for the 1×, 1.5×, and 2× finger-spaced capacitors used in our HCP are shown in Fig. 11. For the 2× capacitor, the vertical metal spacing is smaller than the finger lateral spacing and the layout is modified so that vertically stacked metals belong to the

same capacitor terminal. Layer M1 is not used in the capacitor design to cut down its bottom plate parasitic.

III. HYBRID CHARGE PUMP ARCHITECTURE

This section describes two CP design examples that blend different pump types and device structures to achieve extended voltage range outputs at efficiencies higher than those feasible with a Dickson-type pump alone. HCP designs for both positive and negative voltage polarities are discussed. The circuit implementation details of these HCPs are covered in Section IV.

A. A +36 V HCP design

Shown in Fig. 12 is the block diagram of an HCP design capable of 36-V outputs in a 65-nm CMOS technology. The design is composed of a cascade of three different subpumps, arranged in the order of decreasing efficiency.

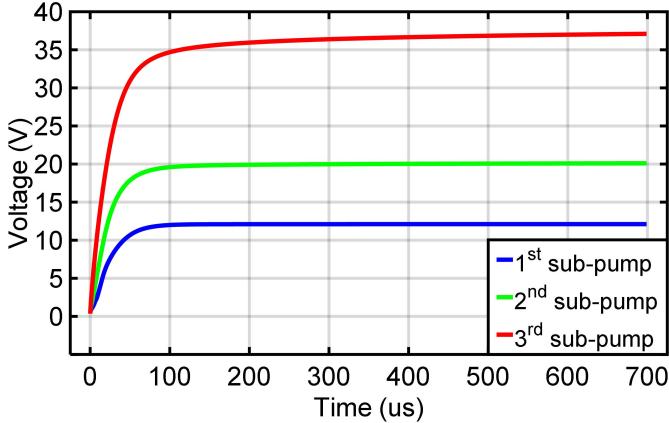


Fig. 13. Transient simulation waveforms of the 36 V HCP.

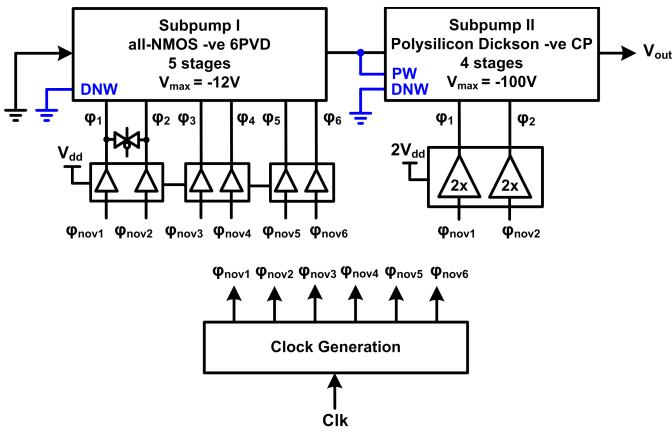


Fig. 14. A -28 V HCP design.

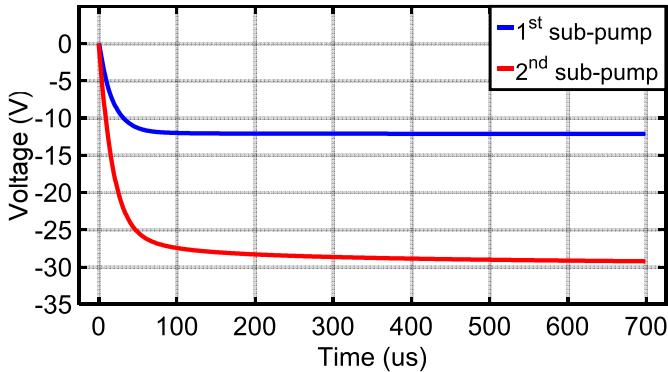


Fig. 15. Transient simulation waveforms of the -28 V HCP.

The first subpump's input is tied to V_{dd} , while the third subpump's output provides the final voltage. Each subpump consists of four stages. The first subpump uses a single-diode substrate isolation, is capable of up to 12V outputs, and has the highest efficiency individually. The unit stage in the first subpump is a CMOS four-phase voltage doubler (4PVD) that uses two additional clock phases to alleviate reverse leakage losses. The second subpump adopts a double-diode substrate isolation, is capable of up to 21-V outputs, and has a lower efficiency than the first subpump. The unit stage in the second subpump is an all-nMOS 6PVD.

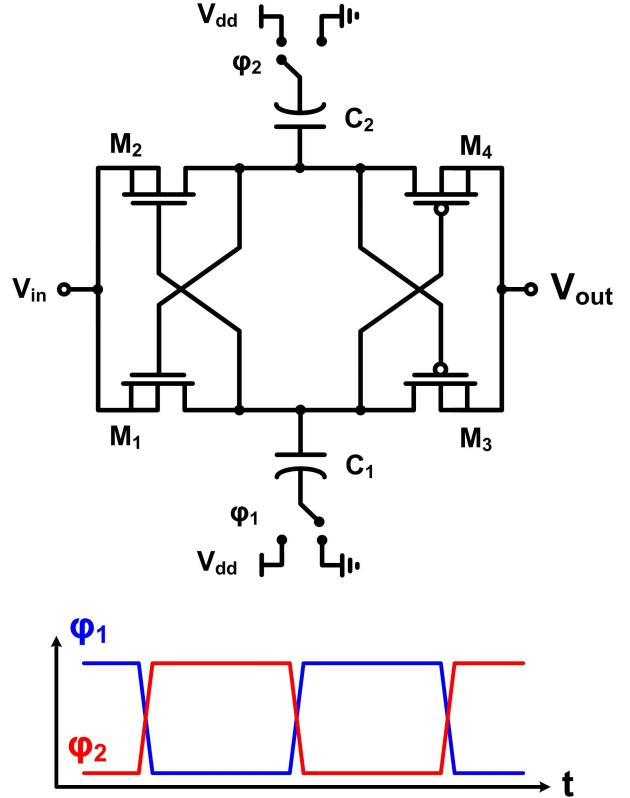


Fig. 16. Conventional 2PVD stage.

This new 6PVD design eliminates the diode drops from the all-nMOS design in [15] by enabling a full-charge transfer switching action. The nMOS switches in this subpump share a common deep n-well that is biased at 12 V by the first subpump's output. The third subpump combines FOX with deep n-well isolation, is capable of >36 V outputs, and has the least efficiency. The unit stage in the third subpump is an improved-drive Dickson doubler using a polysilicon diode. The diodes' deep n-well potential is also kept at 12 V. Based on our reliability models, this deep n-well biasing improves the FOX time-to-failure by $\sim 5000 \times$. To improve the efficiency of the third subpump, its clock drivers use a reliable double-stacked output stage with $2V_{dd}$ swing. The higher clock swings improve the per-stage efficiency and reduces the number of stages needed. With $2V_{dd}$ clock swings, the p-i-n diode's V_{BD} must exceed $4V_{dd}$ (~ 10 V) to prevent reverse pump conduction and loss in efficiency. Based on the measurements provided in Fig. 8(a), the diodes are designed with $L_i = 0.5 \mu m$.

The HCP capacitors are implemented using voltage-tolerant metal capacitors as explained in the previous section. All the three subpumps operate at the same frequency. The first two subpumps use the same per-stage capacitance (2×4 pF), while the third subpump capacitance is half of that value (2×2 pF). Based on our system-level analysis, this relative capacitor sizing for the individual subpumps results in a near-optimal HCP efficiency. To optimize area and power efficiency, the capacitor's finger spacing is gradually tapered based on the voltage requirements of each subpump.

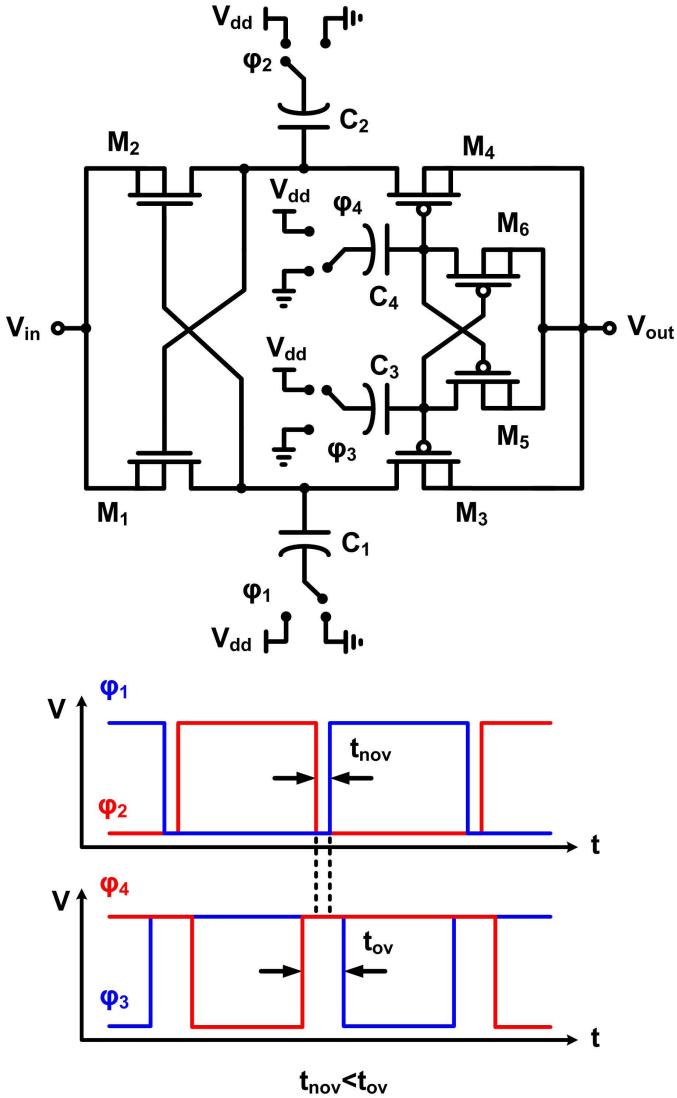


Fig. 17. CMOS 4PVD stage.

The capacitors in the first, second, and third subpumps use $1\times$, $1.5\times$, and $2\times$ finger spacings, respectively. A summary of the parameters for the capacitors used in each subpump is provided in Table II. To further reduce switching losses, charge recycling clock drivers similar to those presented in [18] are used to drive the main pumping capacitors of the first and second subpumps. Maintaining a relatively fixed timing relationship between the clock phases required by each subpump is necessary for efficiency and voltage reliability considerations. A robust clock generation circuit providing the necessary phases for all the subpumps is also explained in Section IV.

As expected of switched capacitor circuits, the current driving capability of the HCP scales directly with the pumping frequency (f_{pump}). The higher f_{pump} is, the more charge gets transferred to the load per unit time. Depending on the relative value of the switch/capacitor RC time constant compared with one clock period, the pump operates in either the slow switching limit (SSL) or the fast switching limit (FSL) [19]. In the SSL, the pump's output resistance exhibits a $1/fC$ dependence and the pump's peak efficiency stays relatively

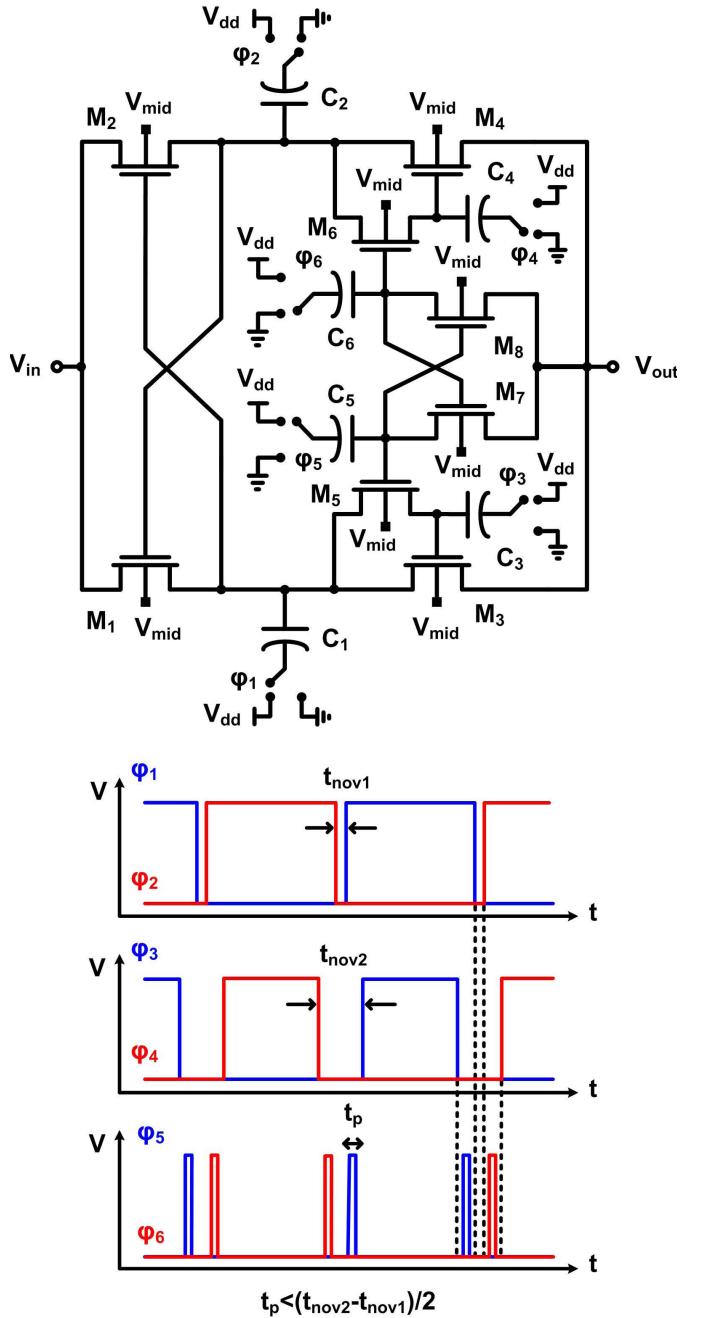


Fig. 18. All-nMOS 6PVD stage.

independent of f_{pump} . In the FSL, the pump's current drive is limited by a fixed switch ON resistance (r_{on}), and the output resistance no longer scales with f_{pump} . In the FSL, the efficiency drops with frequency, as higher switching losses dominate. For optimum efficiency, the HCP is operated in the SSL, with f_{pump} scaling accordingly to meet the load current requirement but not exceeding the SSL. Only 2.5-V-thick oxide devices are used in this design, and all the switches are sized to have $r_{\text{on}} = 1.2 \text{ k}\Omega$. A summary of the switch sizes is also included in Table II. This sizing allows the HCP to operate in the SSL for f_{pump} up to 25 MHz and maintain high peak efficiencies for load currents as high as $120 \mu\text{A}$.

Shown in Fig. 13 are the transient simulation waveforms for the 36-V HCP, indicating how the individual subpump

TABLE II
SUMMARY OF THE CAPACITOR AND SWITCH PARAMETERS USED IN THE DIFFERENT HCP SUBPUMPS

Subpump	Stage Capacitance	Finger Spacing	Capacitor Density	Voltage Tolerance	C _p /C	Switch Size
First	2 X 4 pF	100 nm	1.4 fF/ μ m ²	10 V	3.6 %	PMOS: 2.4 μ m / 0.28 μ m NMOS: 0.8 μ m / 0.28 μ m
Second	2 X 4 pF	150 nm	0.93 fF/ μ m ²	21 V	5.2 %	NMOS: 1.4 μ m / 0.5 μ m
Third	2 X 2 pF	200 nm	0.6 fF/ μ m ²	33 V	8.8 %	Diode: W=20 μ m, L _i =0.5 μ m

outputs build at startup. For our simulations, we use diode models that are fitted to the polysilicon diode measurements. As for the transistors, only body diodes are incorporated within the transistor model. Moreover, the reverse breakdown of these body diodes is not captured by the model. Accordingly, explicit instances of the different well and body diodes must be added to the schematic to accurately capture the voltage range limitations of each subpump. The HCP is found to have a 63% rise time of 27 μ s assuming a 30-pF capacitive load and $f_{\text{pump}} = 4$ MHz.

B. A -28V HCP design

Shown in Fig. 14 is the block diagram of an HCP design capable of -28 V outputs in a 65-nm CMOS technology. Because double-diode substrate isolation is not compatible with negative polarity pumps, this design consists of two subpumps only. The first subpump consists of five stages and has its input shorted to ground, whereas the second subpump consists of four stages and provides the final pump output. The first subpump adopts single-diode substrate isolation and is capable of down to -12 V outputs. The unit stage in the first subpump is a negative voltage all-nMOS 6PVD. An all-nMOS design for this subpump is preferred because it obliterates the back-gate bias of the pMOS switch that otherwise exists in a CMOS implementation. The deep n-well potential of this subpump is grounded to prevent forward junctions. The second subpump combines FOX with deep n-well isolation and is capable of < -28 V outputs. The unit stage in the second subpump is the negative voltage version of our improved-drive Dickson design. The diodes' deep n-well potential in this subpump is grounded, while the p-well is biased at -12 V by the first sub-pump's output. The capacitors used in the first and second subpumps have 1 \times and 2 \times finger spacings, respectively.

Shown in Fig. 15 are the transient simulation waveforms for the -28 V HCP, indicating the individual subpump outputs. The HCP is found to have a 63% rise time of 22 μ s assuming a 30-pF capacitive load and $f_{\text{pump}} = 4$ MHz.

IV. CIRCUIT IMPLEMENTATION

This section explains the circuit implementation details of the different subpump cells and the clock generation circuit needed for our HCP designs.

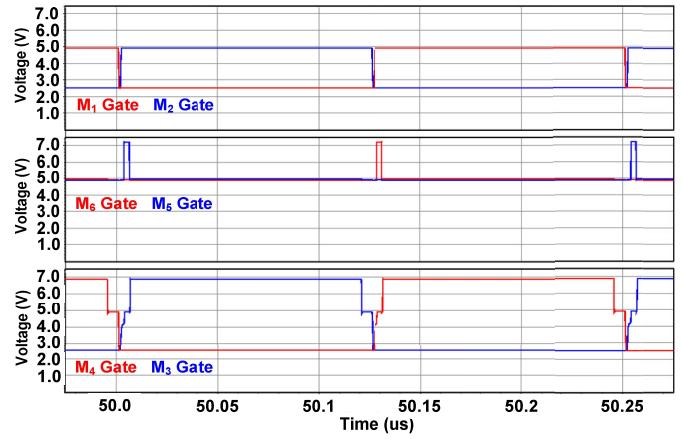


Fig. 19. Transient simulation waveforms of the all-nMOS 6PVD.

A. Four-Phase Voltage Doubler

One common and simple CMOS voltage doubler implementation is the two-phase voltage doubler (2PVD) shown in Fig. 16 [20]. The 2PVD provides a compact and reliable method to generate the level-shifted signals necessary to operate the switches in a charge transfer mode. A drawback of the 2PVD is its reversion current losses. Regardless of the relationship between phases φ_1 and φ_2 , different reverse conduction mechanisms lead to an output charge leakage [21]. To alleviate reversion losses, we introduce a new 4PVD cell design. The 4PVD decouples the nMOS switch operation from the pMOS switch operation. By independently controlling the doubler switches, a break-before-make switching arrangement can be attained in which all different types of reversion losses are eliminated.

The proposed 4PVD schematic and corresponding timing diagram are shown in Fig. 17. Two nonoverlapping phases φ_1 and φ_2 drive the gates of the cross-coupled nMOS devices M_1 and M_2 , while two overlapping phases φ_3 and φ_4 drive the gates of the cross-coupled pMOS devices M_3 and M_4 . Capacitors C_3 and C_4 are chosen to be much smaller than C_1 and C_2 ($\sim 0.1 \times$) since they do not need to deliver any load current. Assuming that the cell's input voltage is equal to V_{dd} , at steady state, capacitors C_1 and C_2 are charged via devices M_1 and M_2 and their top plate potential toggles between V_{dd} and $2V_{dd}$. Because phases φ_1 and φ_2 are nonoverlapping, devices M_1 and M_2 are never simultaneously ON, hence eliminating reversion charges from capacitors C_1 and C_2 into the input

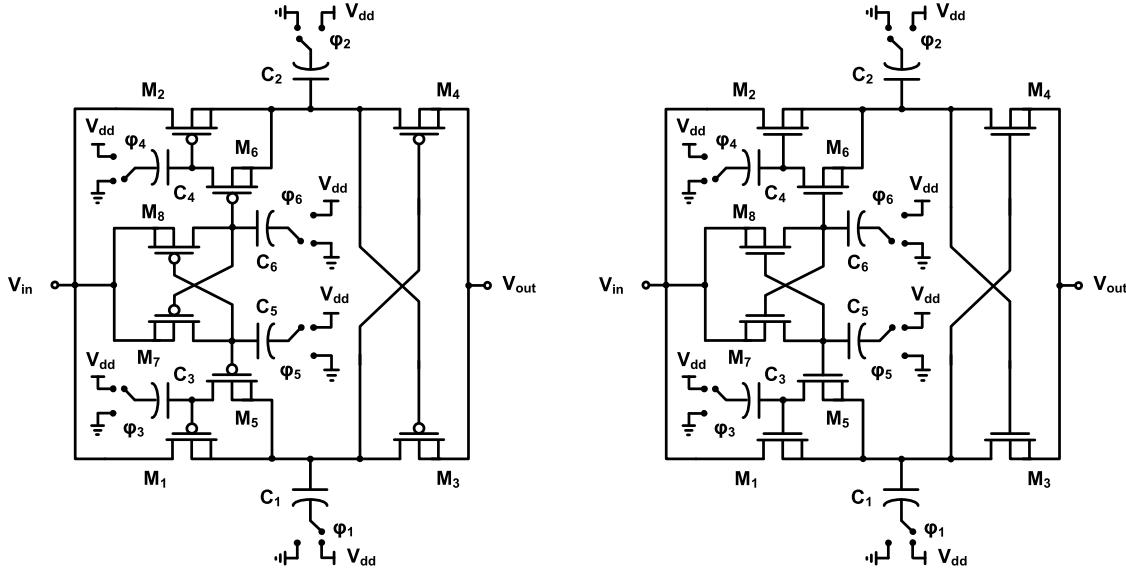


Fig. 20. Same-type switch 6PVD designs with bulk and source terminals shorted. (a) Positive voltage all-pMOS stage. (b) Negative voltage all-nMOS stage.

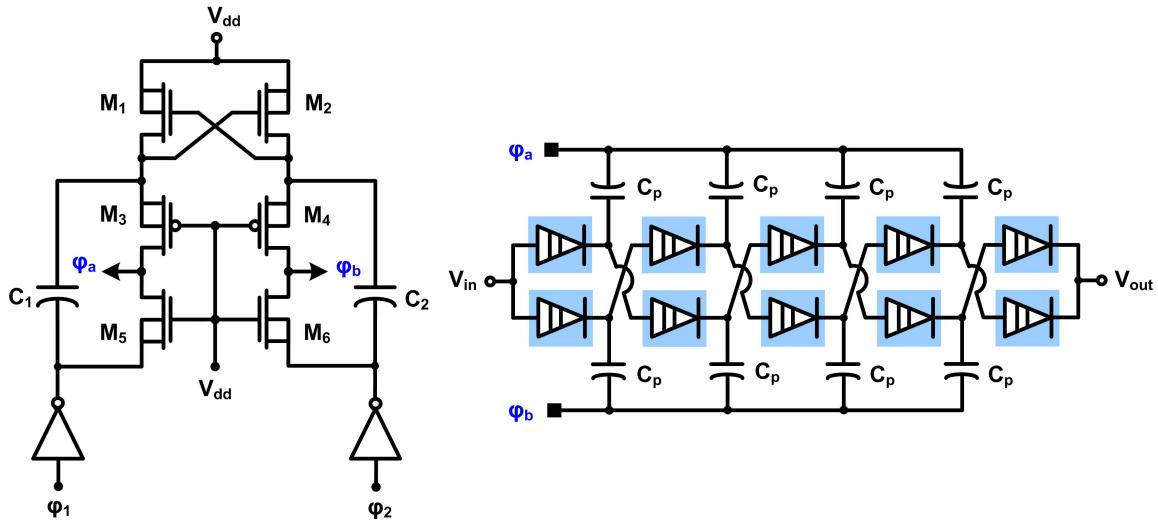


Fig. 21. Improved-drive Dickson CP.

node. Similarly, at steady state, $V_{out} = 2V_{dd}$ and capacitors C_3 and C_4 are charged via devices M_5 and M_6 and their top plate potential toggles between V_{dd} and $2V_{dd}$. Reversion losses from the output node into capacitors C_3 and C_4 are eliminated since phases φ_3 and φ_4 are overlapping and devices M_5 and M_6 are never simultaneously ON. The timing relationship between phase pairs φ_1/φ_2 and φ_3/φ_4 is such that the φ_1/φ_2 nonoverlap interval (t_{nov}) is contained within the φ_3/φ_4 overlap interval (t_{ov}), i.e., $t_{nov} < t_{ov}$. This timing setup guarantees that devices M_1 and M_3 (M_2 and M_4) are never simultaneously ON, hence eliminating the last type of reversion losses occurring directly from the output to the input node.

An alternative (dual) implementation of the 4PVD is also possible by swapping the input and output ports and replacing all the nMOS devices with pMOS devices and vice versa while inverting all the clock phases. Moreover, the negative voltage version of this 4PVD is derived by swapping the input and output ports and connecting all the pMOS devices bulk terminals to ground to prevent forward junctions.

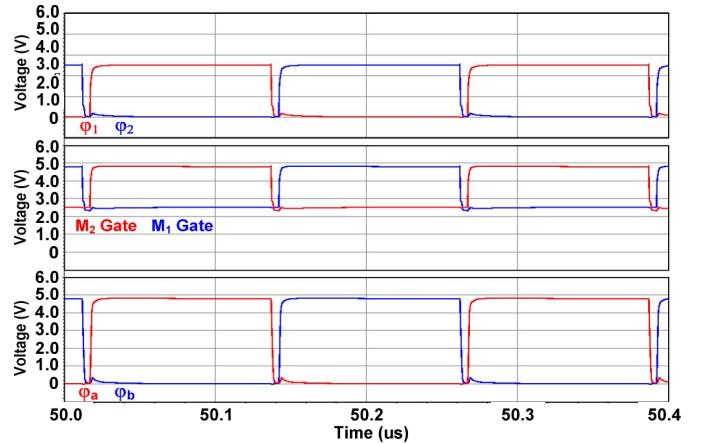


Fig. 22. Transient simulation waveforms of the double-stacked clock driver.

B. All-nMOS Six-Phase Voltage Doubler

The availability of complementary switches in a technology greatly simplifies the CP design as it reduces the total number

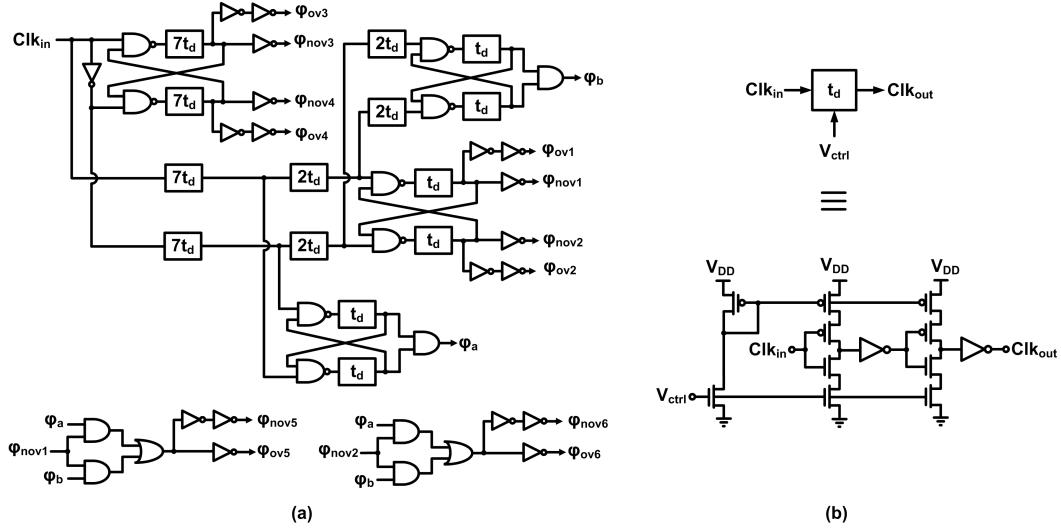


Fig. 23. (a) Process-Voltage-Temperature insensitive CMOS clock generation circuit. (b) Voltage programmable delay element with symmetric rise and fall time delays.

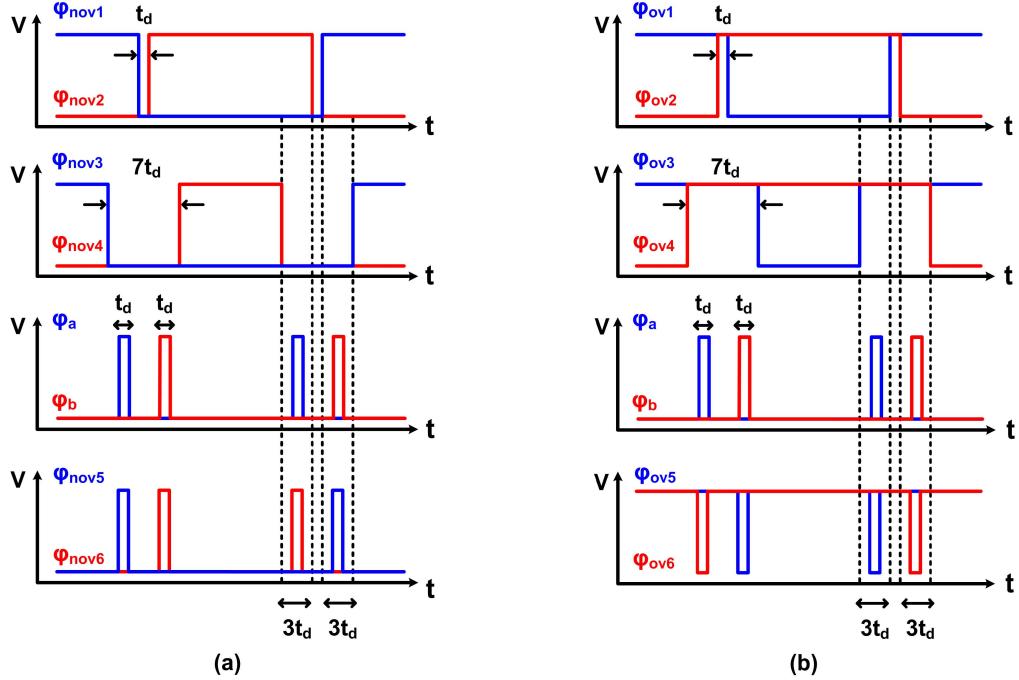


Fig. 24. Timing diagrams of the proposed clock generation circuit for (a) nonoverlapping phases and (b) overlapping phases.

of clock phases needed to operate the pump. However, in order to allow double-diode substrate isolation, only nMOS switches can be used. One possible all-nMOS doubler implementation is derived from the CMOS 2PVD in Fig. 16, by replacing the cross-coupled pMOS devices with diode connected nMOS devices [15]. Diode-connected switches reduce the pump efficiency due to their V_{th} voltage drop. To improve the efficiency of the all-nMOS doubler stage, we present in Fig. 18 an all-nMOS 6PVD with a full charge transfer switching operation.

In order to fully turn ON the nMOS devices M_3 and M_4 , their gate potential needs to rise all the way to $3V_{dd}$.

Moreover, to completely turn devices M_3 and M_4 OFF, their gate potential needs to drop to V_{dd} . Accordingly, to operate M_3 and M_4 as efficient charge transfer switches, their gate control require a $2V_{dd}$ voltage swing. Applying a $2V_{dd}$ swing to the transistor gate directly compromises its oxide reliability. Instead, we propose to perform this voltage transition on two separate steps, each having a single V_{dd} transition to meet the device voltage ratings. To implement this modification, four additional transistors (M_5 – M_8) and two additional capacitors (C_5 and C_6) and two clock phases (φ_5 and φ_6) are needed. Again, the level-shifting capacitors (C_3 – C_6) are chosen $\sim 0.1 \times$ smaller than the main pumping capacitors C_1 and

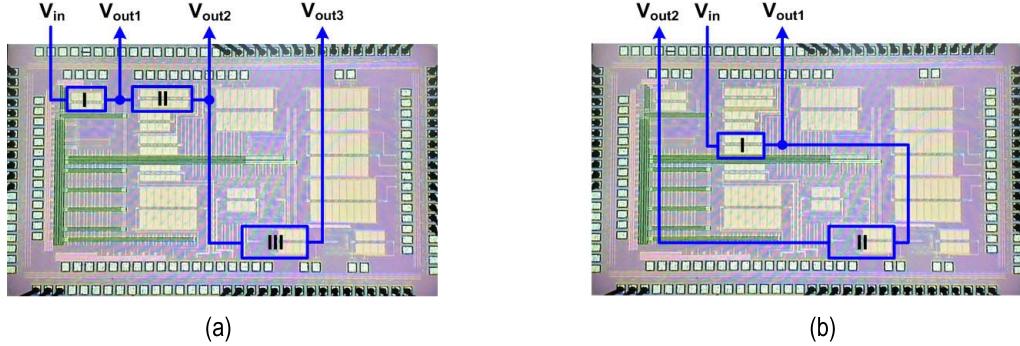


Fig. 25. Die micrographs indicating the different subpump locations for the (a) +36 V HCP and (b) -29 V HCP.

C_2 . Clock phases φ_1 and φ_2 (φ_3 and φ_4) are nonoverlapping with nonoverlap period t_{nov1} (t_{nov2}), such that $t_{nov1} < t_{nov2}$. Also, phases φ_5 and φ_6 are relatively narrow nonoverlapping pulses, where the φ_5 pulses are contained within two successive rising (falling) edges of φ_1 and φ_3 . Similarly, the φ_6 pulses are contained within two successive rising (falling) edges of φ_2 and φ_4 .

Shown in Fig. 19 are the simulated transient waveforms of the all-nMOS 6PVD. Assuming that the cell's input voltage is equal to V_{dd} , at steady state, capacitors C_1 and C_2 are charged via devices M_1 and M_2 and the gate potentials of M_1 and M_2 toggle between V_{dd} and $2V_{dd}$. Also, capacitors C_5 and C_6 are charged via devices M_7 and M_8 , and the gate potentials of M_7 and M_8 (also M_5 and M_6) toggle between $2V_{dd}$ and $3V_{dd}$. To reliably turn ON device M_3 , its gate potential must undergo two transitions. The first M_3 gate transition is from V_{dd} to $2V_{dd}$ and happens as follows.

- 1) φ_1 transitions high, and capacitor C_3 is charged to $2V_{dd} - V_{th}$ through device M_5 .
- 2) φ_5 transitions high, and the M_5 gate potential rises to $3V_{dd}$ allowing C_3 to fully charge to $2V_{dd}$.
- 3) φ_5 transitions back low to turn M_5 OFF and prevent reverse charge leakage from C_3 to C_1 .

The second M_3 gate transition is from $2V_{dd}$ to $3V_{dd}$ and happens as φ_3 transitions high to turn M_3 fully ON so that the output node can charge to $2V_{dd}$. Conversely, to turn M_3 OFF, its gate potential transitions from $3V_{dd}$ to V_{dd} on two steps. The first transition is from $3V_{dd}$ to $2V_{dd}$ and happens as φ_3 transitions low and the M_3 gate potential falls back to $2V_{dd}$, turning M_3 OFF. The second transition is from $2V_{dd}$ to V_{dd} , and happens as φ_1 transitions low and the M_3 gate potential discharges through M_5 to V_{dd} . This exact switching order guarantees that all devices operate within their nominal voltage rating. It is worth noting that in this implementation, the highest voltage nodes, per stage, are the gates of transistors M_3 and M_4 (also M_5 and M_6). Accordingly, it is the gate potentials of M_3 and M_4 of the final pump stage that are eventually limited to $V_{DNW} + V_{NP}$, and the pump's maximum output voltage slightly falls to $V_{DNW} + V_{NP} - V_{th}$.

More generally, same-type switch voltage doublers (all-nMOS or all-pMOS) can be valuable assets when confronted with different polarity, voltage range and technology limitations. So far, we have already made the case for all-nMOS voltage doublers to extend the voltage

range in triple-well technologies. Another case can be made for positive voltage pumps in older twin-tub technologies with no deep n-well. In which case, an all-pMOS doubler alleviates the back-gate bias associated with the bulk nMOS switches and improves the pump efficiency. Correspondingly, for negative voltage pumps in triple-well technologies, a deep n-well all-nMOS doubler alleviates the back-gate bias associated with the pMOS switches. Same-type switch 6PVD cells, with proper bulk and source connections, are shown in Fig. 20(a) and (b) for positive and negative polarities, respectively. As a general rule, given the same polarity, the all-pMOS doubler can be derived from its all-nMOS counterpart by swapping the input and output ports, replacing the nMOS devices with pMOS devices, and inverting all the clock phases. The negative voltage doubler can be derived from its positive voltage counterpart by simply swapping the input and output ports.

C. Improved-Drive Dickson Charge Pump

In the last subpump design, polysilicon diodes are used for the switch implementation. To help overcome the switches' forward voltage drop and improve efficiency, higher pumping voltages relative to the diode's knee voltage are generated for driving the pump capacitors. Shown in Fig. 21 is our improved-drive Dickson CP schematic. A special double-stacked clock driver boosts the input swing of two nonoverlapping clock phases (φ_1 and φ_2) from V_{dd} to $2V_{dd}$. The boosted-swing clocks (φ_a and φ_b) are then applied to the bottom plates of the Dickson pump capacitors. To enable $> V_{dd}$ clock swings and maintain device reliability, a stacked-device output stage is necessary in the output stage. Shown in Fig. 22 are the simulated transient waveforms of the double-stacked clock driver. The nMOS devices M_1 and M_2 operate together with capacitors C_1 and C_2 to level shift the input clocks by V_{dd} , so that the gates of M_1 and M_2 toggle between V_{dd} and $2V_{dd}$. Devices M_3 and M_4 share a fixed gate potential (V_{dd}) and operate as a source-switched output stage. Similarly, devices M_5 and M_6 form the complementary output stage. When φ_1 is low, device M_5 is ON, device M_3 is OFF, and φ_a is grounded. When φ_1 is high, device M_5 is OFF, device M_3 is ON, and φ_a is at $2V_{dd}$. Capacitors C_1 and C_2 are chosen much larger than the pumping capacitors C_p ($\sim 8 \times$) to provide sufficient charge to drive the final load. Conveniently, since capacitors C_1 and C_2 are subject to a small voltage difference

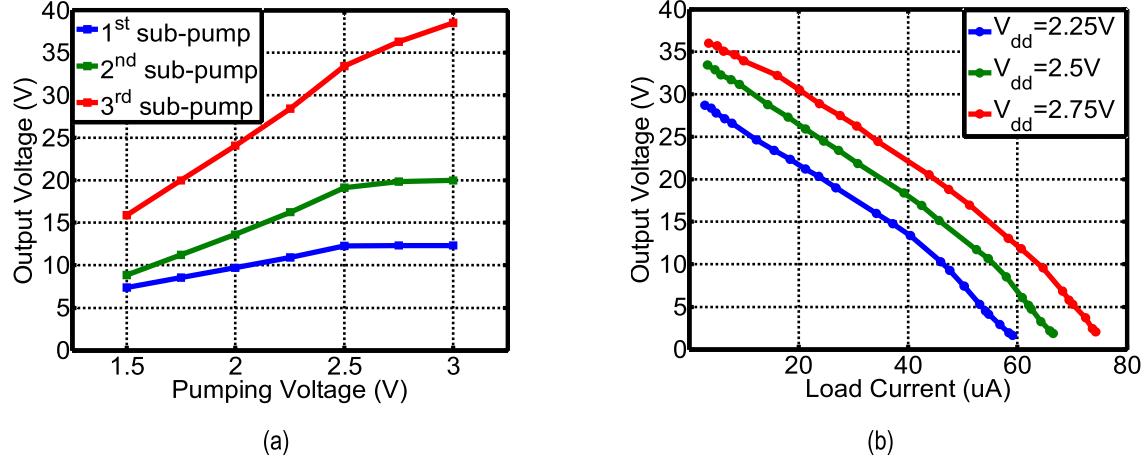


Fig. 26. Measurement results of the 36 V HCP. (a) Unloaded subpump's output voltage. (b) DC I - V characteristics at $f_{\text{pump}} = 4$ MHz.

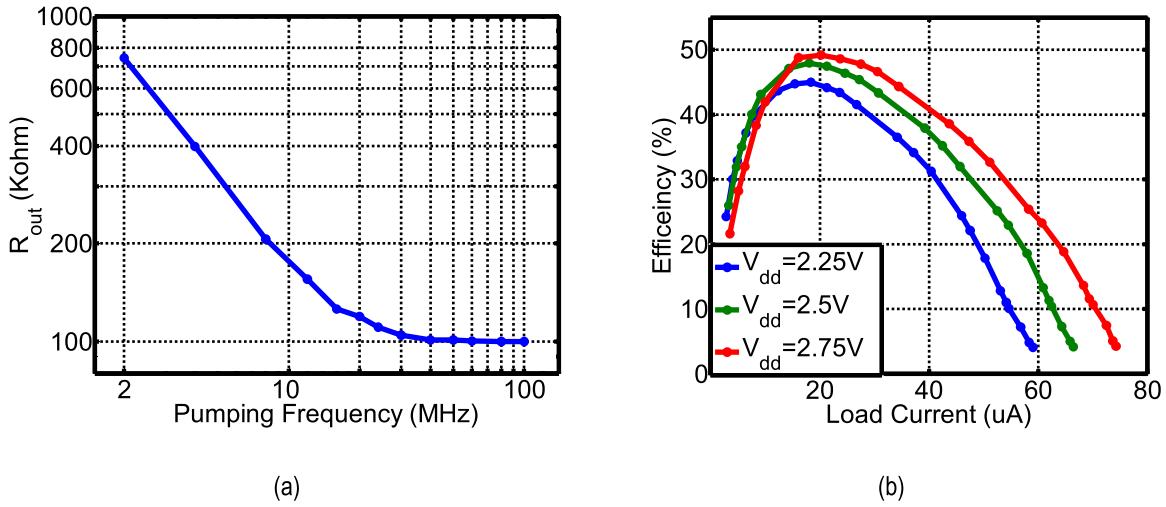


Fig. 27. Measurement results of the 36 V HCP. (a) Output resistance versus f_{pump} . (b) Efficiency at $f_{\text{pump}} = 4$ MHz and different V_{dd} .

of only V_{dd} , they are implemented using area-efficient MOS capacitors. This subpump is laid out in an identical fashion to the schematic shown in Fig. 21. Such layout avoids having to route both clock phases (φ_a and φ_b) to both sides of the pump and hence significantly reduces the parasitic capacitance associated with these clock nets. The negative voltage version of this pump is realized by simply swapping the input and output ports.

D. Clock Generation Circuit

To eliminate undesired charge losses and guarantee device reliability, the relative phase relationship for different subpump clocks needs to be maintained across different process, voltage, and temperature corners. Shown in Fig. 23(a) is a robust clock generation circuit capable of providing all the phases needed by the different subpump types and voltage polarities. At its core, the clock generation circuit is based on pairs of cross-coupled NAND gate with unit delays in the feedback path to generate robust overlapping (nonoverlapping) clock phases. To generate multiple clock pairs with different overlap/nonoverlap intervals ($t_{\text{ov}}/t_{\text{nov}}$) as dictated by our

subpump design, multiple such cross-coupled gates are used with different feedback delays. Because these multiple paths present different delays between their respective input and output edges, additional delay elements are selectively inserted in front of the paths with less delay to align the final output phases. Assuming that the time delay of one delay unit is t_d , the number of units chosen for our implementation is such that $t_{\text{ov}} = t_{\text{nov}} = t_d$ for the φ_1/φ_2 clock pair and $t_{\text{ov}} = t_{\text{nov}} = 7t_d$ for the φ_3/φ_4 pair. In order to align clock pairs φ_1/φ_2 and φ_3/φ_4 , a total delay of $9t_d$ is inserted in front of the φ_1/φ_2 clock generation circuit. All unit delays are identical, noninverting as shown in Fig. 23(b) and have the same fanout. Cascading two inverters guarantees unit delay matching regardless of the direction of the clock transition (rising or falling). Additionally, the amount of unit delay is adjustable by controlling the inverter's bias current. All delay elements are matched in the layout and placed within close proximity.

To generate the narrow pulse width clocks, φ_5 and φ_6 , first, we need to generate the intermediate clocks φ_a and φ_b as shown by the timing diagram in Fig. 24. These intermediate



Fig. 28. Transient measurement waveforms of the 36 V HCP at startup.

φ_a and φ_b pulses are generated by applying two overlapping clock phases with $t_{ov} = t_d$ to the inputs of a two-input AND gate. Proper unit delays are inserted to separate the φ_a and φ_b pulses by $4t_d$ and to center them around the φ_1/φ_2 nonoverlap interval. Clock phase φ_5 is generated by selecting the φ_a and φ_b pulses that occur when φ_1 is high. Similarly, clock phase φ_6 is generated by selecting the φ_a and φ_b pulses that occur when φ_2 is high.

V. MEASUREMENT RESULTS

In this section, we present the measurement results of two HCP circuits having different voltage polarities and output ranges. The circuits are implemented in a 65-nm bulk CMOS technology with their layouts highlighted on the die micrographs in Fig. 25.

A. +36 V Hybrid Charge Pump

These measurements are based on the three subpump HCP topology discussed in Fig. 12. The areas of the first, second, and third subpumps are $240 \mu\text{m} \times 160 \mu\text{m}$, $370 \mu\text{m} \times 160 \mu\text{m}$, and $400 \mu\text{m} \times 200 \mu\text{m}$ respectively. Shown in Fig. 26(a) are the measured output voltages of the unloaded HCP and the individual subpumps at $f_{\text{pump}} = 4 \text{ MHz}$, and different supply voltages (V_{dd}). As expected, the first and second subpump outputs are clipped at 12 V and 20 V, respectively. The third subpump output exhibits no signs of clipping for this V_{dd} range. The HCP has a maximum output voltage of 36 V at $V_{\text{dd}} = 2.75 \text{ V}$. Under normal operation and a given load current (20 μA in our case), the number of stages, pumping voltage, and pumping frequency are chosen so that the first and second subpumps never exceed their breakdown limit to avoid unnecessary loss in efficiency due to the substrate diodes' leakage. The HCP output voltage is also characterized versus different load currents (I_{load}) and V_{dd} , as shown in Fig. 26(b). The pump maintains $>34 \text{ V}$ output voltages for $I_{\text{load}} < 10 \mu\text{A}$ at $V_{\text{dd}} = 2.75 \text{ V}$. The pump's output resistance is plotted versus f_{pump} as shown in Fig. 27(a). In the SSL, the pump's output resistance decreases with f_{pump} . For $f_{\text{pump}} > 25 \text{ MHz}$, the pump operates

in the FSL and the output resistance is limited to 100 k Ω . Shown in Fig. 27(b) is the overall HCP efficiency, measured at $f_{\text{pump}} = 4 \text{ MHz}$ and different V_{dd} values versus I_{load} . For output power comparison at a given efficiency, there exists a one-to-one correspondence between the measured output voltage data versus load current in Fig. 26(b) and the measured efficiency data in Fig. 27(b). The pump's peak efficiency improves with higher pumping voltage and is equal to 49% at $I_{\text{load}} = 20 \mu\text{A}$ and $V_{\text{dd}} = 2.75 \text{ V}$. Note that for $V_{\text{dd}} = 2.75 \text{ V}$ and smaller load currents (higher pump voltages), there is a loss in HCP efficiency compared with the $V_{\text{dd}} = 2.5 \text{ V}$ and $V_{\text{dd}} = 2.25 \text{ V}$ cases. Expectedly, this is attributed to the voltage clipping in the first and second subpump outputs at higher pump voltages. However, the HCP peak efficiency is not impacted much because at larger load currents, the subpump's output voltages drop below the substrate diodes saturation limits. If we were to characterize the efficiency for even higher pumping voltages ($V_{\text{dd}} > 2.75 \text{ V}$), a drop in pump efficiency would become evident even at peak values. Therefore, careful design mandates that various HCP parameters, e.g., V_{dd} , f_{pump} , and the number of subpump stages, are chosen to avoid clipping and maximize the efficiency at a given operating load current.

The individual subpumps are also characterized separately. As expected, the first subpump has the highest peak efficiency at 71%, followed by the second subpump at 49% and the third subpump at 43%. As expected, the HCP pump efficiency is higher than that of the Dickson CP alone. In order to characterize the voltage limitations of the third subpump, its input voltage is ramped slowly for the given f_{pump} and V_{dd} until failure occurs. It is found that when the polysilicon diode deep n-well is biased at 12 V, the pump breaks down at $\sim 100 \text{ V}$.

For the sake of completeness, the transient waveform measurements of the individual subpump outputs at startup are shown in Fig. 28 at $f_{\text{pump}} = 10 \text{ MHz}$, $V_{\text{dd}} = 2.5 \text{ V}$, and an output load of $1 \text{ M}\Omega // 30 \text{ pF}$ (includes measurement scope loading). Note that the final pump voltage is slightly lower than predicted by the dc measurements due to the scope loading on all three subpump outputs. The overall HCP time constant is measured to be 32 μs .

B. -28 V Hybrid Charge Pump

These measurements are based on the two subpump HCP topology depicted in Fig. 14. The areas of the first and second subpumps are $300 \mu\text{m} \times 160 \mu\text{m}$ and $400 \mu\text{m} \times 200 \mu\text{m}$, respectively. Shown in Fig. 29(a) are the measured output voltages of the unloaded HCP and the individual subpumps for $f_{\text{pump}} = 4 \text{ MHz}$ and different V_{dd} values. As expected, the first subpump output voltage is clipped at -12 V. The overall HCP has a maximum negative output voltage of -28 V at $V_{\text{dd}} = 2.75 \text{ V}$. The HCP output voltage is also characterized versus different I_{load} and V_{dd} as shown in Fig. 29(b). The pump maintains $< -27 \text{ V}$ output voltages for absolute $I_{\text{load}} < 10 \mu\text{A}$ at $V_{\text{dd}} = 2.75 \text{ V}$. In the SSL, the pump's output resistance decreases with f_{pump} , as shown in Fig. 30(a), and is limited to 91 k Ω in the FSL. Shown in Fig. 30(b) is the overall HCP

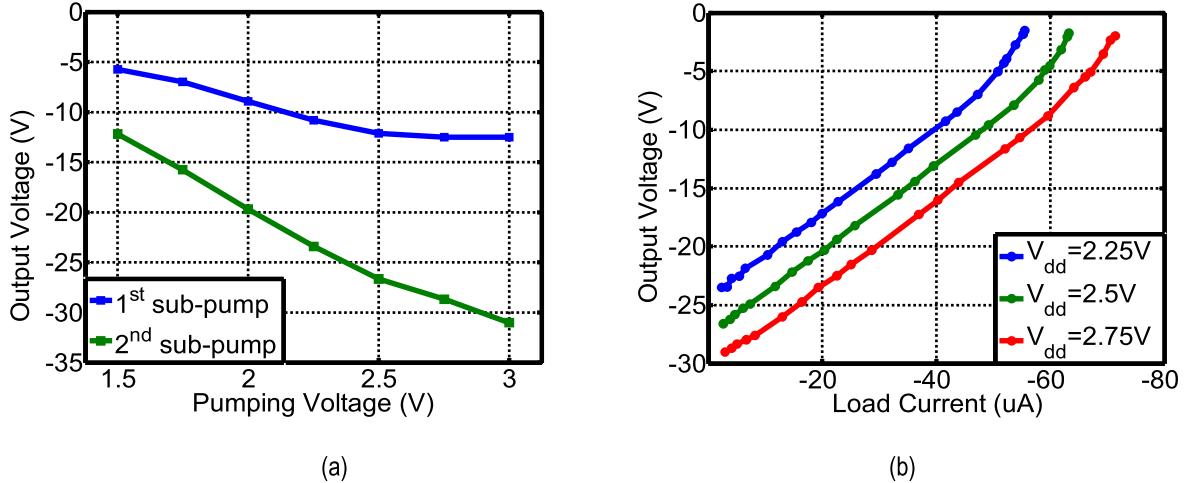


Fig. 29. Measurement results of the -28 V HCP. (a) Unloaded subpump's output voltage. (b) DC I - V characteristics at $f_{\text{pump}} = 4$ MHz.

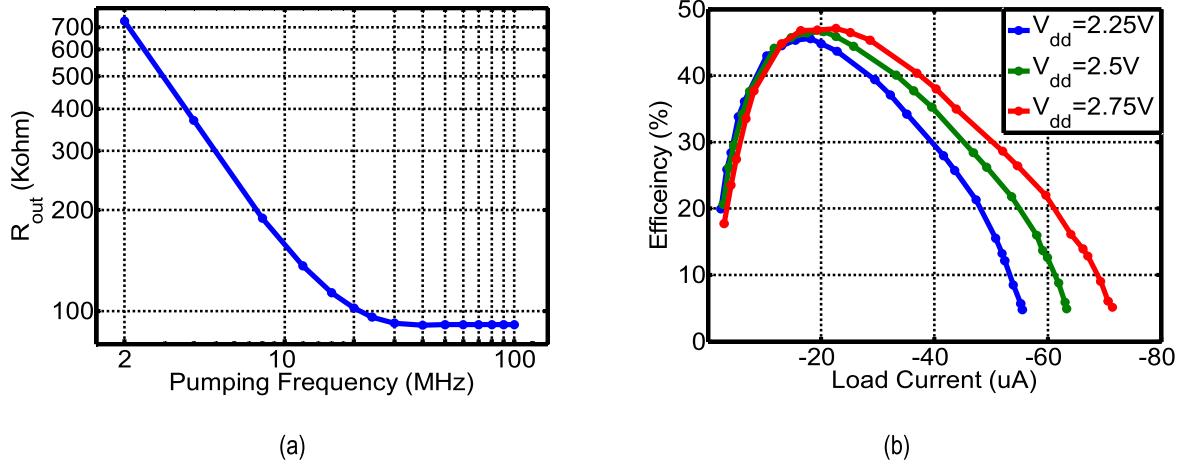


Fig. 30. Measurement results of the -28 V HCP. (a) Output resistance versus f_{pump} . (b) Efficiency at $f_{\text{pump}} = 4$ MHz and different V_{dd} .

efficiency measured at $f_{\text{pump}} = 4$ MHz and different V_{dd} values versus I_{load} . The pump's peak efficiency is equal to 46% at $I_{\text{load}} = 20 \mu\text{A}$ and $V_{\text{dd}} = 2.75$ V. The transient waveform measurements of the individual subpump outputs at startup are shown in Fig. 31 at $f_{\text{pump}} = 10$ MHz, $V_{\text{dd}} = 2.5$ V, and an output load of $1 \text{ M}\Omega // 30 \text{ pF}$. The overall pump's time constant is measured to be $20 \mu\text{s}$.

In Table III, we summarize the performance of our 36-V HCP and compare it with those of other high-voltage CPs reported in the literature. Our design is the only fully integrated CP that attains several tens of volts outputs in an advanced nanometer-scale bulk CMOS technology. Voltages near 50 V are reported in [4] and [6], but are enabled by older technology nodes having higher breakdown-voltage substrate diodes. Moreover, depending on the availability of a deep n-well layer, some or all of the voltage range extension methods explained in this paper are compatible with older technology nodes. The authors believe that if combined with methods from this paper, designs in [4] and [6] can attain >50 -V outputs. Finally, this design achieves a reasonable power efficiency even though it is only of secondary importance at



Fig. 31. Transient measurement waveforms of the -28 V HCP at startup.

this voltage range, as indicated by the lack of efficiency data for most of the high-voltage designs reported in the literature. Unlike our adoption of a standard CMOS technology, a higher

TABLE III
PERFORMANCE COMPARISON OF THE 36-V HCP WITH HIGH-VOLTAGE CHARGE PUMPS REPORTED IN THE LITERATURE

Reference	[4]	[5]	[6]	[8]	[14]	This Work
Output Voltage	51 V	14.8 V	50 V	19.4 V	28 V	36 V (up to 100V)
Load Current	4 μ A	0.7 μ A	50 μ A	19 μ A	2 μ A	20 μ A
Technology	0.6- μ m CMOS	0.18- μ m CMOS	0.8- μ m HV CMOS	0.35- μ m SOI CMOS	0.25- μ m CMOS	65-nm CMOS
Supply Voltage	6 V	1.8 V	5 V	3.3 V	2.5 V	2.5 V
Well Breakdown	70 V	14.8 V	55 V	NA	18.9 V	12 V
Switch Device	PMOS	PMOS/NMOS	PMOS/NMOS	Body Diode	Polysilicon Diode	PMOS/NMOS/ Polysilicon Diode
Number of Stages	18	10	16	6	12	12
Stage Capacitor	50 pF	10 pF	0.5 pF	30 pF	NA	8 pF
Pumping Frequency	0.5 MHz	50 MHz	10 MHz	4 MHz	1 MHz	4 MHz
Efficiency	30 %	NA	NA	79 %	NA	49 %
Area	2.42 mm ²	0.129 mm ²	0.33 mm ²	0.81 mm ²	NA	0.18 mm ²

efficiency of 79% is reported in [8] and is attributable to the unique SOI process and its inherently low stray capacitance ($\sim C_p/C = 3\%$).

VI. CONCLUSION

Toward the combined goals of extended voltage range and improved power efficiency, we have demonstrated a 36-V HCP circuit with 49% efficiency and an area of 0.18 mm² in a 65-nm CMOS technology. We have also demonstrated a negative voltage HCP capable of achieving -28-V outputs and 46% efficiency and occupies an area of 0.13 mm². The positive voltage HCP design enables a threefold increase in the technology's maximum voltage range compared with conventional designs. Substrate isolation for extended voltage ranges is enabled by a modified deep n-well biasing scheme and by leveraging FOX isolation. A new same-type switch voltage doubler and an improved-drive Dickson CP have been introduced to implement the discussed isolation methods. Our hybrid design mixes a high-voltage-range Dickson CP with lower voltage-range but more efficient pump cells to achieve a higher overall pump efficiency. The circuit's long-term reliability is carefully analyzed and accounted for in the layout and choice of device dimensions. Extended CMOS voltage ranges enabled by this design allow for better integrated and cheaper SoC solutions needed by many MEMS applications.

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