

A 14-nm 0.14-ps_{rms} Fractional-N Digital PLL With a 0.2-ps Resolution ADC-Assisted Coarse/Fine-Conversion Chopping TDC and TDC Nonlinearity Calibration

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Abstract—A digital fractional-N phase-locked loop (PLL) is presented. It achieves 137- and 142-fs rms jitter integrating from 10 kHz to 10 MHz and from 1 kHz to 10 MHz, respectively. With a frequency multiplication ratio of 207.0019231 [digitally controlled oscillator (DCO) frequency is 50 kHz away from an integer multiple of the 26-MHz reference clock], a -78.6 -dBc fractional spur is achieved for an output clock that runs at half of the DCO frequency. Time-to-digital converter (TDC) chopping technique, TDC fine conversion through successive approximation register analog-to-digital converters (SARADCs), and TDC nonlinearity calibration improve integrated phase noise and fractional spurs. This design meets the performance requirement of the 256-QAM 4×4 MIMO LTE standard in 5-GHz ISM band and also the 5G cellular 64-QAM standard in 28-GHz band. This work, implemented in a 14-nm fin-shaped field effect transistor (FinFET) CMOS process, is integrated to a cellular RF integrated circuit supporting advanced carrier aggregation operation. This PLL draws 13.4 mW and occupies 0.257 mm².

Index Terms—all-digital phase-locked loop (ADPLL), digital phase-locked loop (PLL), digitally controlled oscillator (DCO), fractional spur, fractional-N PLL, frequency synthesizer, time-to-digital converter (TDC).

I. INTRODUCTION

TO MEET ever-growing demands for higher mobile data rates, long term evolution (LTE) standards continue to evolve. While carrier aggregation (CA) improves data rates, it requires wider aggregated signal bandwidth that limits the number of users that can be serviced simultaneously at high data rates. Techniques like 256-QAM and 4×4 MIMO are attractive because these improvements do not need wider signal bandwidth. For a receiver with sufficient linearity, the SNR improves with the input signal power until it is limited by either I/Q matching or local oscillator (LO) phase noise.

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Since I/Q matching can be improved by digital calibration, LO phase noise defines the receiver SNR floor.

The 4×4 MIMO by itself does not require better SNR or LO integrated phase noise (IPN) comparing to single-in, single-out (SISO) and 2×2 MIMO if the channel is ideal. In reality, however, the channel is not ideal. For the 4×4 MIMO case, it is difficult for the receiver to demodulate the data even though the transmitter sends orthogonal data streams through four antennas. Due to the channel characteristics, the orthogonality between streams is not preserved. With other non-ideal factors like fading, the receiver needs better SNR or IPN comparing to SISO and 2×2 MIMO cases. There is no strict specification on the IPN requirement for the 4×4 MIMO case; To support 256-QAM and 4×4 MIMO under non-ideal channel conditions, we need an IPN of about -48 dBc. For the highest frequency LTE channel of 5850 MHz in the 5-GHz ISM or licensed assisted access band, this requirement translates to 0.15-ps rms jitter.

For 5G cellular operation in the 28-GHz band, we need about -34 dBc IPN to support 64-QAM. This requirement also translates to a 0.15-ps rms jitter. With a second-stage integer- N frequency synthesizer that can be realized as a sub-sampling PLL [1], [2], or an injection-locked frequency multiplier [3], [4], the first-stage frequency synthesizer can have output frequency range similar to a frequency synthesizer designed for LTE. The second-stage frequency synthesizer can be designed to have very low IPN. For example, Yoo *et al.* [4] generates a calculated 38.7-fs rms jitter, resulting in only a minor increase in the overall IPN. As a result, same set of design techniques and circuits can be employed for both LTE and 5G cellular applications.

Recent publications of time-to-digital converter (TDC) and digital-to-time converter (DTC)-based digital phase-locked loops (PLLs) [5]–[8] have demonstrated good IPN, low reference spurs, and good figures-of-merit. In this paper, we have introduced design techniques [9] to break the performance barrier of fractional- N digital PLLs. First, the TDC chopping technique reduces the flicker noise from the TDC and the TDC regulator to improve the phase noise at low offset frequencies. Second, TDC fine conversion with a pair of 7-b successive approximation register analog-to-digital

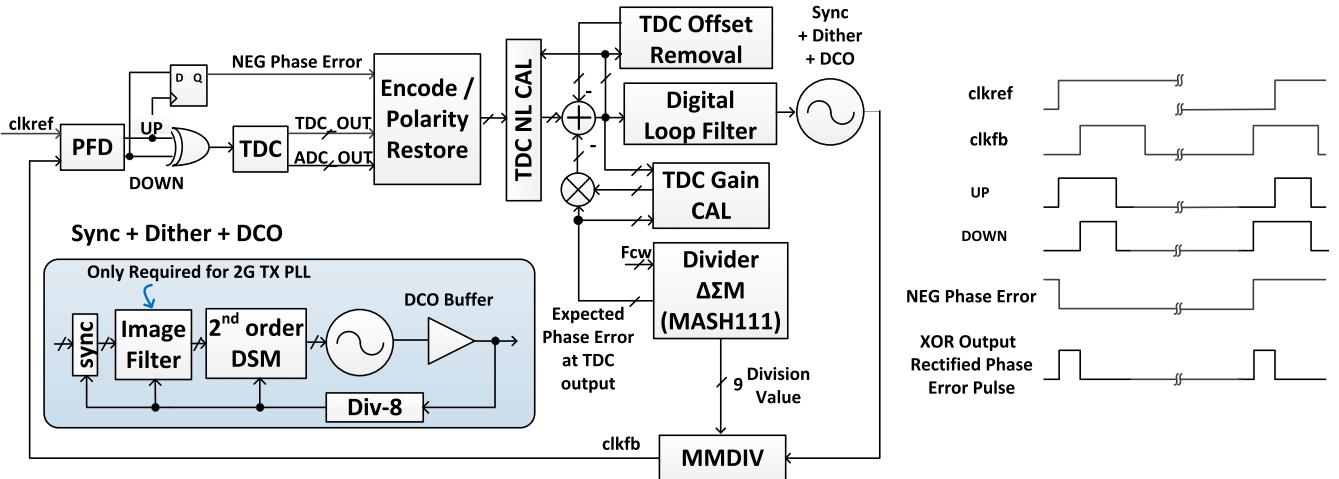


Fig. 1. Digital PLL architecture.

converters (SARADCs) improves the TDC resolution to 0.2 ps. Third, TDC nonlinearity calibration removes the performance impact due to layout and device mismatch. This design achieves 137- and 142-fs rms jitter integrating from 10 kHz to 10 MHz and from 1 kHz to 10 MHz, respectively. A -78.6 -dBC near-integer fractional spur is achieved with a digitally controlled oscillator (DCO) frequency that is 50 kHz away from an integer multiple of reference clock frequency. This design meets the requirements of the 256-QAM 4×4 MIMO LTE and the 5G cellular 64-QAM 28-GHz band standards.

This paper is organized as the following. Section II provides an overview of the digital PLL architecture and circuits. Section III describes the TDC chopping technique. Section IV presents the analog-to-digital converter (ADC)-assisted coarse/fine-conversion TDC. TDC nonlinearity calibration is described in Section V. Section VI presents the experimental results.

II. ARCHITECTURE AND CIRCUIT OVERVIEW

The digital PLL architecture is shown in Fig. 1. This architecture has the form of a classic $\Delta\Sigma$ fractional- N PLL. It contains a phase frequency detector (PFD) and a multi-modulus feedback divider (MMDIV) driven by a MASH111 $\Delta\Sigma$ modulator. The expected phase error is generated from the $\Delta\Sigma$ modulator quantization error. After scaling by the estimated TDC gain, the resulting value is subtracted from the TDC output before entering the loop filter similar to [5]. To support both positive and negative phase error polarity, an XOR gate and a flip-flop are introduced to rectify the phase error and to detect the phase error polarity. The phase error polarity is restored by the TDC encoder. In contrast to [7], which captures only the positive phase errors and drops negative phase error samples, this design reduces the lock time. In addition, it supports TDC chopping to suppress the TDC and the TDC regulator flicker noise as described in Section III. An ADC-assisted coarse/fine-conversion TDC is utilized. The fine-conversion stage, described in Section IV, relies on a pair of 7-b SARADCs to improve the TDC resolution by about 46 times to 0.2 ps. TDC nonlinearity calibration and

compensation circuits, described in Section V, are introduced to improve phase noise and fractional spurs.

The TDC is nonlinear with small magnitude phase errors. Also, the flip-flop that detects phase error could have offset and meta-stability problems. To resolve these issues when the PLL is locked, we can introduce a TDC offset as shown in Fig. 2(a). By adjusting MMDIV division sequence using a circuit shown in Fig. 2(b), phase errors can be steered away from small magnitude values when the PLL is locked. The digital TDC offset-removal loop tracks the magnitude of the TDC offset and removes the expected offset from the TDC encoder output. The expected offset is generated by applying proper polarity to the estimated TDC offset magnitude. This polarity can be extracted from the expected phase error.

For this architecture, the digital PLL bandwidth varies with the TDC resolution. To reduce PLL bandwidth variation, the TDC ring oscillator supply voltage is adjusted to compensate for the TDC resolution process and temperature variation. The reference voltage for the TDC ring oscillator supply regulator is generated by feeding a low-noise proportional to absolute temperature (PTAT) current to a loading circuit that resembles the TDC ring oscillator delay cell.

To reduce the DCO quantization noise, a divide-by-8 DCO clock is used for frequency dithering. A synchronization circuit helps to transfer the digital frequency control word (D_{ctrl}) to the dithering clock domain. Due to the effective up-sampling operation of this interface, images of D_{ctrl} signal appear at harmonics of reference clock frequency. A low-pass image filter operating in dithering clock domain removes the images at D_{ctrl} . This feature is enabled only for 2G cellular transmit mode, and it is bypassed for 3G and 4G modes. A second-order $\Delta\Sigma$ modulator shapes DCO quantization noise to high offset frequencies in order to meet stringent LO phase noise requirement for cellular 2G transmit mode and 3G/4G FDD modes. A 10-b fine-tuning cell is employed, and the layout is arranged as a 32×32 array of 1-LSB fine-tuning cells.

III. TDC CHOPPING TECHNIQUE

For a digital delay-line-based TDC, the flicker noise from delay cells is typically not a concern. For a ring oscillator-based TDC, however, the flicker noise from delay cells

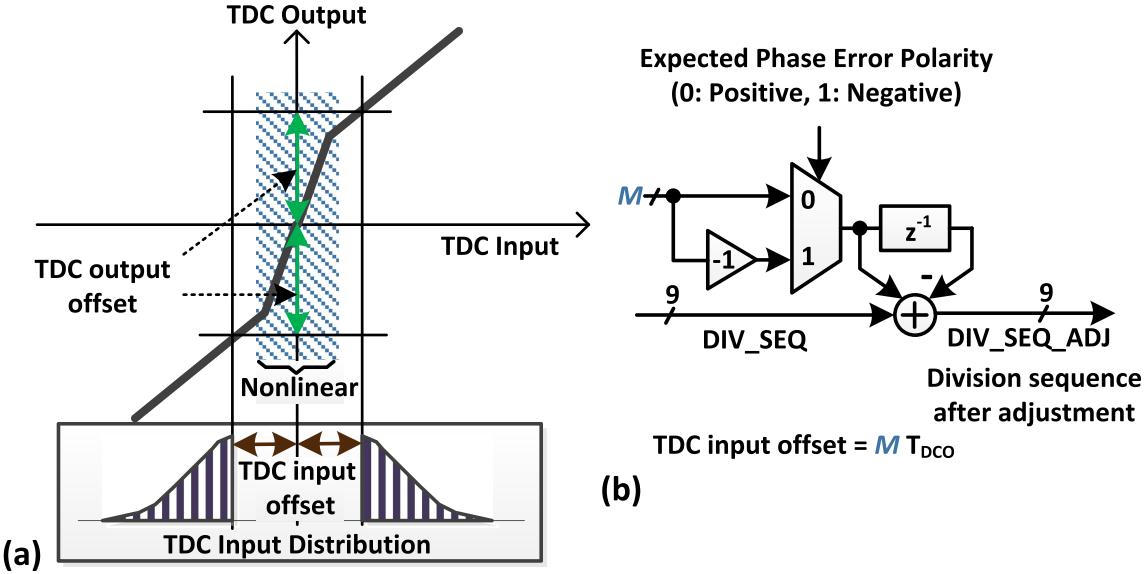


Fig. 2. (a) TDC offset to avoid nonlinear TDC region. (b) Circuit to introduce TDC offset.

becomes more important. With a sufficiently large TDC input magnitude, each delay cell in the ring oscillator is exercised more than once during one single measurement. Since the flicker noise power spectral density is concentrated at low frequencies, jitter due to flicker noise changes slowly as a function of time. Each time we exercise a delay cell in a single measurement, we experience nearly the same amount of jitter due to flicker noise. As a result, the jitter introduced during the second and later periods of the ring oscillator is correlated with the jitter introduced during the first period of the ring oscillator. Therefore, to evaluate the total rms jitter from delay cell flicker noise, we need to multiply the rms jitter introduced by a single ring oscillator period by the number of exercised periods. The jitter power would be the square of the total rms jitter. If we double the TDC input, the phase noise due to the delay cell flicker noise is increased by 6 dB. In comparison, for a delay-line-based TDC, each delay cell is exercised only once for each measurement. To evaluate the total jitter power from delay cell flicker noise, we scale the jitter power of an individual delay cell by the number of delay cells exercised. The phase noise due to the delay cell flicker noise for a delay-line-based TDC only increases by 3 dB if we double the TDC input. In addition, the flicker noise from the ring oscillator voltage regulator also increases the output phase noise. The phase noise due to the TDC voltage regulator flicker noise also increases 6 dB if we double the TDC input. The proposed TDC chopping technique attenuates the phase noise due to the TDC ring oscillator and the TDC voltage regulator flicker noise.

In contrast to alternative digital PLL architectures [5], [8], [10], [11], the chosen architecture can naturally generate both positive and negative phase errors. This property allows us to incorporate a chopping TDC. Chopping techniques [12], [13] have been employed to up-mix amplifier flicker noise and offset to higher frequencies, away from the frequency ranges of interest. Fig. 3 compares a chopping amplifier to the chopping TDC. For a chopping amplifier, we have an input

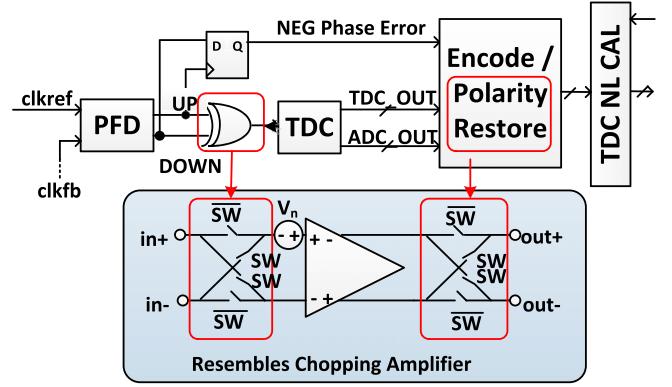


Fig. 3. Chopping TDC and chopping amplifier comparison.

switch and an output switch, and both switches are controlled by the signal SW. Whenever the switch control signal SW = 0, input and output ports are connected to the amplifier without polarity inversion. Whenever SW = 1, both input and output switches reverse polarity. Since the input signal goes through both switches, the polarity is reversed twice, and the same input-to-output transfer function is maintained. However, the input-referred amplifier flicker noise and the offset voltage go through only the output switch and are up mixed to the frequency of the SW signal. For the chopping TDC, the input switch is replaced by the XOR gate that rectifies the phase error polarity, and the output switch is replaced by the polarity restoration circuit inside the TDC encoder. The switching signal SW is replaced by the polarity of phase error sequence generated by the $\Delta \Sigma$ modulator. Effectively, the noise from the TDC and the TDC regulator is mixed by the expected phase error polarity sequence. Strictly speaking, the proposed technique is different from the conventional chopping technique because the phase error polarity sequence is not an alternating polarity sequence. "TDC noise spreading" would be a more accurate description of the proposed technique. Nevertheless,

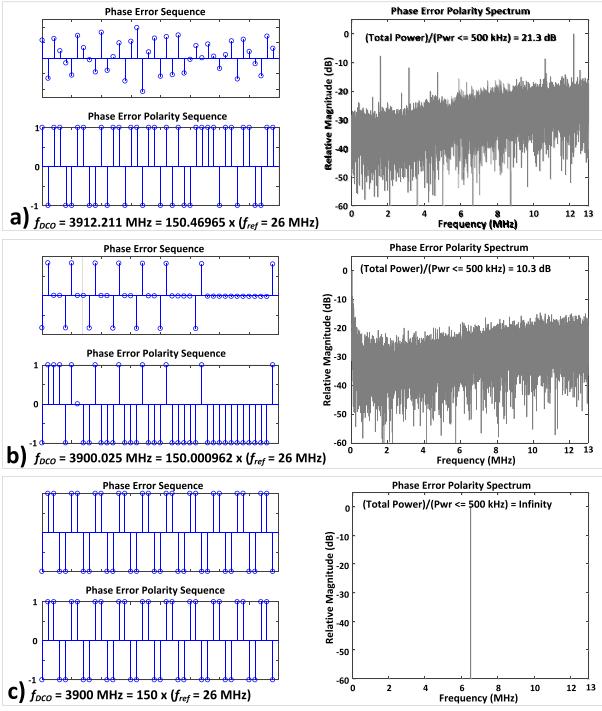


Fig. 4. Expected phase error sequence, polarity sequence, and polarity spectrum for (a) $f_{DCO} = 3912.211 \text{ MHz} = 150.46965 \times f_{ref}$, (b) $f_{DCO} = 3900.025 \text{ MHz} = 150.000962 \times f_{ref}$, and (c) $f_{DCO} = 3900 \text{ MHz} = 150 \times f_{ref}$.

we would like to refer it as a “chopping TDC” because it was inspired by the conventional chopping technique.

To benefit from TDC chopping, the phase error polarity spectrum does not necessarily need to be concentrated at frequencies beyond the PLL bandwidth. As long as the power of the phase error polarity spectrum is spread over a wide range of frequencies, the power of the phase error polarity spectrum integrated over the bandwidth of interest (i.e., up to the PLL bandwidth) would be a small fraction of the total power. When the fractional portion of the frequency synthesis ratio is away from an integer value, noise shaping property of $\Delta\Sigma$ modulator makes the polarity spectrum to concentrate at frequencies beyond PLL bandwidth. Thus, it provides an additional attenuation to the TDC and the TDC regulator flicker noise.

Fig. 4(a)–(c) shows the expected phase error sequence, the expected phase error polarity sequence, and the expected phase error polarity spectrum for $f_{DCO} = 3912.211 \text{ MHz}$ ($150.46965 \times f_{ref}$), $f_{DCO} = 3900.025 \text{ MHz}$ ($150.000962 \times f_{ref}$), and $f_{DCO} = 3900 \text{ MHz}$ ($150 \times f_{ref}$), respectively. To quantify the flicker noise attenuation, let us define $\text{ATTN}_{\text{TDC_CHOP}}$ as the ratio between the total expected phase error polarity power to the portion of power within 500 kHz. This integration bandwidth is chosen because the PLL bandwidth is expected to be lower than 500 kHz. If the phase error polarity spectrum is white, $\text{ATTN}_{\text{TDC_CHOP}} = 10 \log(13 \text{ MHz}/500 \text{ kHz}) = 14.1 \text{ dB}$. With a fractional portion of a frequency multiplication ratio of 0.46965, away from an integer, as shown in Fig. 4(a), the polarity spectrum is concentrated at higher frequencies, and $\text{ATTN}_{\text{TDC_CHOP}} = 21.3 \text{ dB}$, which is 7.2 dB better than

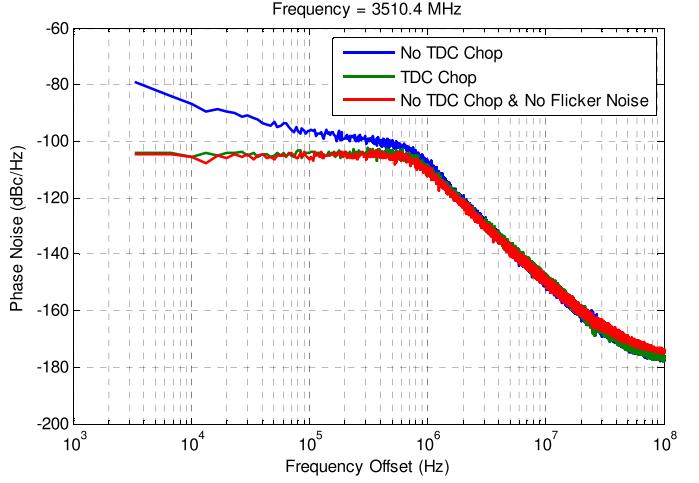


Fig. 5. Simulated phase noise and IPN with TDC chopping turned OFF, with both flicker noise and TDC chopping turned OFF, and with both flicker noise and TDC chopping turned ON.

the ratio with a white spectrum. With a fractional portion of a multiplication ratio of 0.000962, as shown in Fig. 4(b), the polarity spectrum is concentrated at lower frequencies, and the $\text{ATTN}_{\text{TDC_CHOP}} = 10.3 \text{ dB}$, which is 3.8 dB worse than the ratio with a white spectrum. With an integer multiplication ratio, the polarity sequence is periodic, and the $\text{ATTN}_{\text{TDC_CHOP}}$ is infinity.

Fig. 5 compares the simulated phase noise and IPN of three cases. Without TDC chopping, the flicker noise increases the phase noise at low offset frequencies and results in an IPN of 1.1° . If we disable the flicker noise and keep the TDC chopping mode disabled, the IPN is reduced to 0.44° . With both the flicker noise and the TDC chopping mode enabled, the IPN is 0.49° , which is much improved comparing to the case without chopping but slightly higher than the case without flicker noise.

IV. ADC-ASSISTED COARSE/FINE-CONVERSION TDC

To improve the TDC resolution, a coarse/fine conversion TDC is employed. The fine converter improves the TDC resolution by converting a pair of residue voltages from the coarse stage with a pair of 7-b SARADCs. The TDC circuit is shown in Fig. 6(a). The timing diagram of TDC control signals is shown in Fig. 6(b). The coarse TDC employs a 13-stage interpolated ring oscillator [14]. Interpolated delay cells help to increase the ring oscillator frequency and to extend the rising and falling transition time of the oscillation waveforms. Effectively, the interpolated delay cells help to improve the linearity of oscillation waveforms near the rising and falling transitions. Before starting measurements, the 13-stage interpolated ring oscillator node voltages are reset to pre-defined values derived from a resistor ladder. This operation initializes the phase of the ring oscillator. In contrast, a gated-ring oscillator (GRO) [15] does not initialize the phase. For integer- N synthesis ratios, a GRO converts the same input in every clock cycle and generates a periodic output that translates any circuit non-ideality to spurs. Phase initialization eliminates such a problem. In addition, a GRO suffers from charge leak in hold mode that effectively translates to

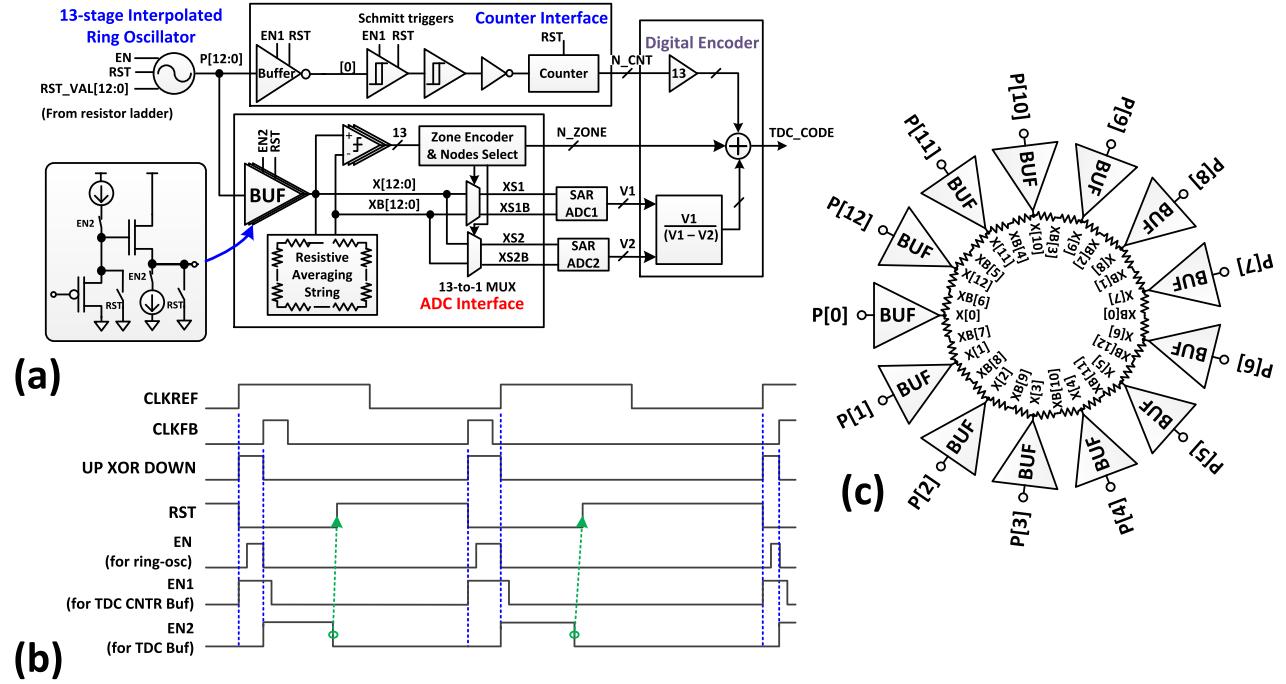


Fig. 6. (a) Coarse/fine-conversion TDC circuit. (b) Timing diagram. (c) Voltage buffer and resistor ring.

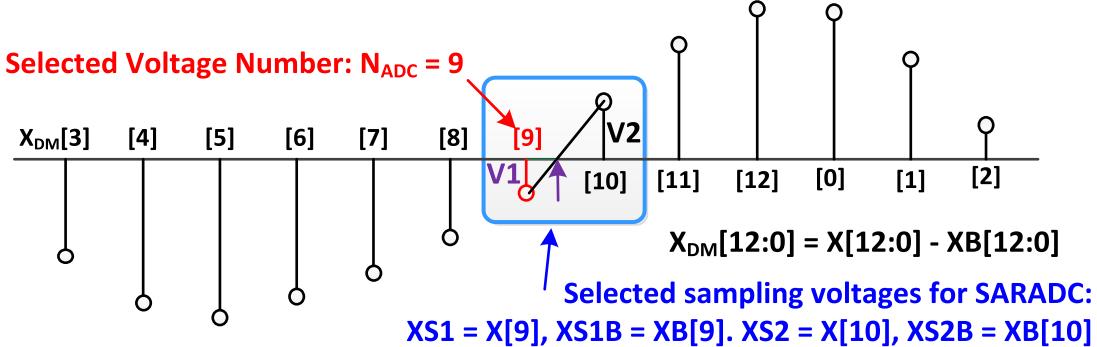


Fig. 7. Snapshot of voltages at resistor ring nodes and fine-conversion nodes selection explanation.

TDC measurement errors [7], [15]. For fractional- N frequency multiplication ratios, the amount of time that a GRO spends in hold mode varies from cycle to cycle. As a result, the GRO charge leak would depend on the previous sample. With phase initialization, the ring oscillator starts from the same state, and therefore, it does not carry memory from earlier conversions.

When the input signal EN in Fig. 6(a) goes high, the ring oscillator starts to accumulate the phase. Pulses generated by the ring oscillator drive a digital counter. When EN goes low, the ring oscillator is disconnected from supply and ground to hold output node voltage values. The 13 buffers together with the output resistor ring generate 13 differential voltages representing the ring oscillator state, as shown in Fig. 6(c). The resistor ring helps to generate the negative polarity signals XB [12:0] through interpolation, and it further linearizes output node voltages as a function of TDC input EN pulse width. The 13 zone-detection comparators determine the phase of the ring oscillator to within 1/13 of the ring-oscillator period.

Fig. 7 shows a snapshot of voltage values at the resistor ring nodes. The node voltage values resemble a “periodic pattern.” A pair of nodes near the low-to-high zero-crossing point is selected for fine conversion. The fine-conversion algorithm is described in Fig. 8. TDC coarse code, $V1(t_{in})$ and $V2(t_{in})$ are shown as functions of TDC input EN pulse width t_{in} . Due to the linearization from interpolated ring oscillator and resistor ring, the $V1(t_{in})$ and $V2(t_{in})$ are linear as functions of t_{in} for the same TDC coarse code. As a result, $[V1(t_{in}) - V2(t_{in})]$ is nearly a constant. Let the TDC coarse resolution be T_{coarse} . The slope of the $V1(t_{in})$ and $V2(t_{in})$ is $[V1(t_{in}) - V2(t_{in})]/T_{coarse}$. The fine-conversion result $T_{fine}(t_{in})$ can be evaluated, and $T_{fine}(t_{in}) = V1(t_{in})/[V1(t_{in}) - V2(t_{in})] \times T_{coarse}$. Let, $V1$, $V2$, and T_{fine} be the values corresponding to a specific TDC input EN pulse width $t_{in'}$. The fine conversion can be expressed relative to T_{coarse}

$$T_{fine} = \left[\frac{V1}{V1 - V2} \right] T_{coarse}.$$

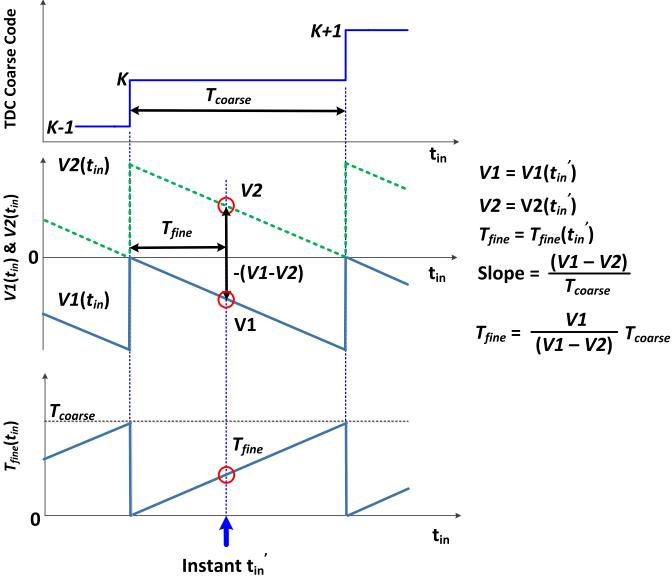


Fig. 8. TDC coarse code, $V1$ and $V2$ as a function of TDC input and fine-conversion encoding algorithm.

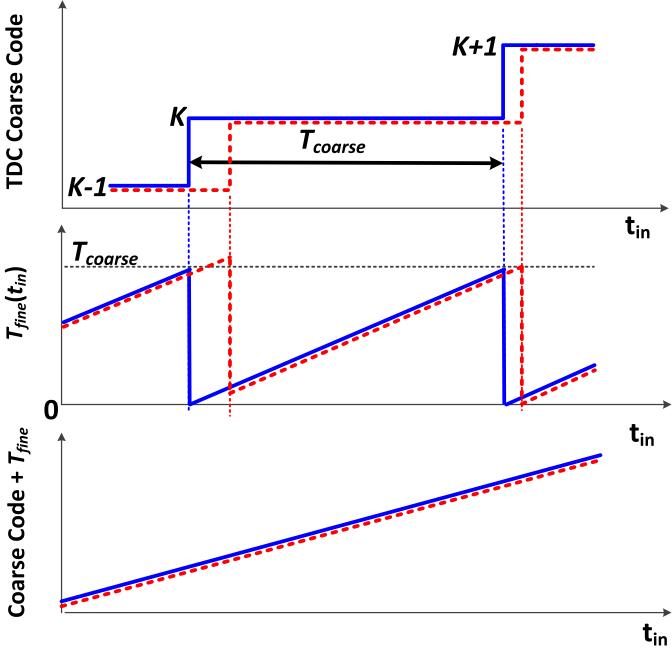


Fig. 9. TDC encoding with zone-detection comparator offset.

At the presence of zone-detection comparator offsets, the coarse code decision boundary is shifted. Such a shift in coarse code decision boundary is reflected in the residue voltages similar to a pipeline ADC [16] as shown in Fig. 9. As a result, zone-detection comparator offsets do not affect encoded TDC output as long as the residue voltages are linear functions of t_{in} . Fig. 10 shows the encoded $T_{fine}(t_{in})$ from circuit simulation without layout and device mismatch. Interpolated ring oscillator and resistive ring are powerful techniques to make encoded $T_{fine}(t_{in})$ linear to t_{in} . From Fig. 10, the simulated TDC fine-conversion error due to nonlinearity is less than 0.1 ps. Thus, we can conclude that the nonlinearity

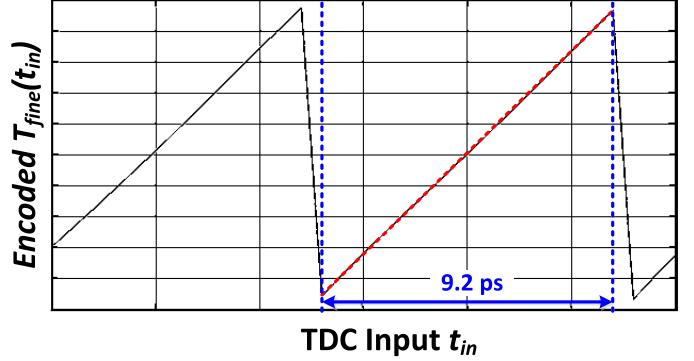


Fig. 10. Encoded T_{fine} as a function of TDC input from circuit simulation without layout and device mismatch.

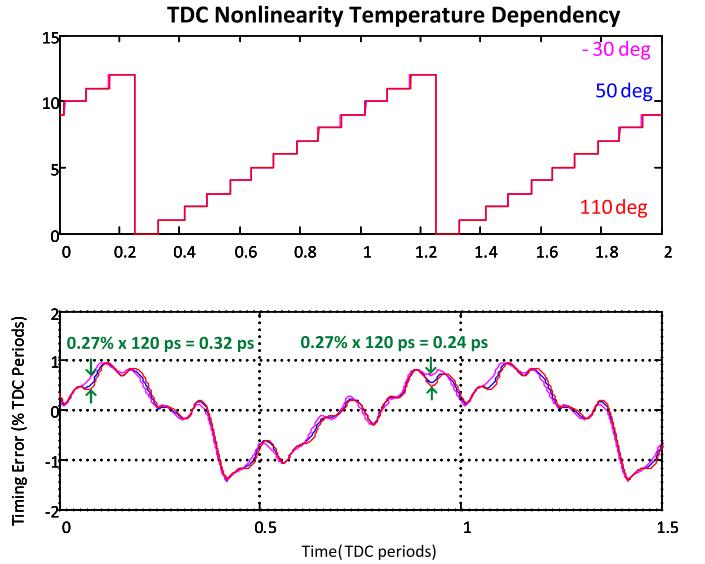


Fig. 11. TDC timing error simulation with extracted layout and device mismatch at -30°C , 50°C , and 110°C .

of the present TDC is limited only by the layout and device mismatch.

Since the TDC nonlinearity calibration is performed only one time during system power up, the nonlinearity due to layout and device mismatch needs to be insensitive to temperature variation. Any TDC nonlinearity temperature dependence would degrade phase noise and fractional spur performance if the operating temperature is different from the temperature during calibration time. The TDC error simulation results with layout parasitic extraction and device mismatch at -30°C , 50°C , and 110°C are shown in Fig. 11. The ring-oscillator supply comes from a regulator with a PTAT reference voltage designed to keep the ring-oscillator frequency nearly constant over temperature. Even with a regulated PTAT supply, the ring-oscillator free-running frequency has a small temperature dependence ($\sim 3\%$ from -30°C to 90°C). This is not a concern because most part of the TDC nonlinearity scales well with ring-oscillator oscillation period. The TDC nonlinearity shown in Fig. 11 is normalized to the ring-oscillator oscillation period for each temperature case. In the actual design, the TDC nonlinearity is estimated and compensated relative to the TDC ring-oscillation period. In Fig. 11, the

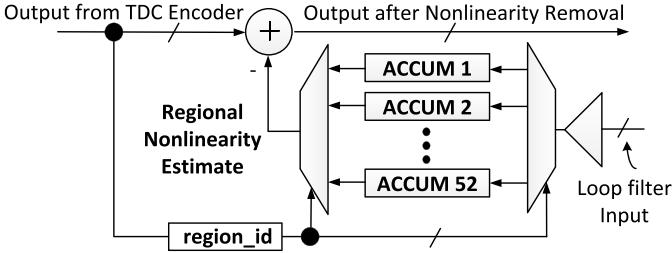


Fig. 12. Fifty-two region TDC nonlinearity calibration circuit.

TDC nonlinearity variation over temperature is less than or equal to 0.32 ps. This result is evaluated with a not-well-matched ring-oscillator layout, and the temperature dependence is expected to improve with a better-matched ring-oscillator layout.

The effective TDC resolution can be calculated using the following equation:

$$\tau_{\text{res}} \approx \frac{T_{\text{RO_peri}}}{N_{\text{stg}}} \frac{1}{(V1 - V2)}.$$

$T_{\text{RO_peri}}$ is the ring-oscillator free-running period. N_{stg} is the number of ring-oscillator delay cells. $V1 - V2$ is the average digital code difference between the two SARADCs, and it is the TDC resolution enhancement factor due to the fine-conversion stage. $V1 - V2$ can have value up to half of the SARADC code conversion range. However, margin is required to accommodate shifts of $V1$ and $V2$ values due to device mismatch and zone-detection comparator offsets. With a $T_{\text{RO_peri}}$ of 120 ps and $(V1 - V2) = 46$, the effective TDC resolution is 0.2 ps.

V. TDC NONLINEARITY CALIBRATION AND COMPENSATION

To improve TDC linearity, calibration is performed at chip power up. During calibration, the PLL is set to a selected frequency multiplication ratio that is comfortably away from integer boundary values. In addition, the fractional portion needs to have sufficient hamming distance to ensure the phase error sequence is sufficiently random. Simple fractional ratios such as 0.25 and 0.5 would degrade the quality of TDC nonlinearity calibration due to limited set of phase error values generated by the $\Delta\Sigma$ modulator. During normal operation, TDC calibration is turned OFF, and TDC is compensated based on nonlinearity estimated during calibration.

The digital TDC calibration circuit is shown in Fig. 12. This design is similar to the nonlinearity calibration circuit for a DTC-based digital PLL [17]. One TDC ring-oscillator period is sub-divided to 52 regions. Due to the averaging effect from the interpolated ring oscillator and from the resistor ring, timing error due to TDC nonlinearity is a smooth function of TDC input t_{in} . As a result, 52 regions are sufficient. Without the interpolated ring oscillator and the resistor ring, more calibration memory would be required. Each of the 52 accumulators in Fig. 12 stores the nonlinearity estimation of the corresponding TDC region. In each clock cycle, the estimated TDC nonlinearity is subtracted from the TDC output. The digital loop-filter input contains reference clock phase noise,

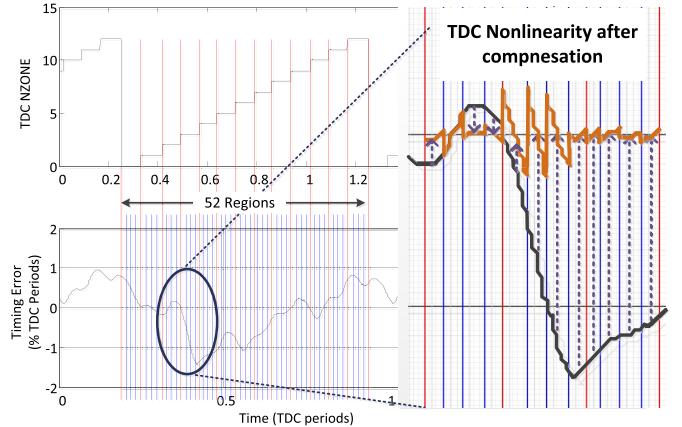


Fig. 13. Graphical representation of TDC nonlinearity calibration.

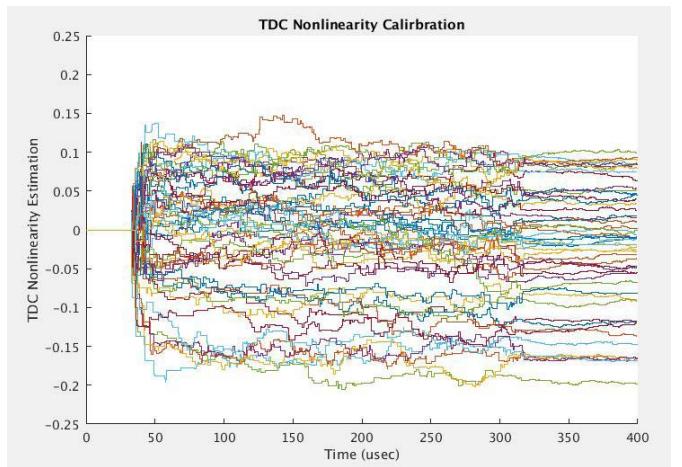


Fig. 14. TDC nonlinearity calibration convergence simulation.

TDC quantization noise, TDC, and DCO device noise and also errors in TDC nonlinearity estimation. The low-pass nature of this TDC calibration circuit makes this circuit tracking the TDC nonlinearity, and it averages out the errors from other sources. Fig. 13 graphically demonstrates the TDC nonlinearity calibration. The nonlinearity shown in Fig. 13 comes from layout mismatch and device mismatch. The TDC nonlinearity repeats every ring-oscillator period. Effectively, we are estimating the average value of samples that falls in each region and remove it from incoming samples that falls to the corresponding region. As a result, the residual nonlinearity is significantly reduced.

The TDC calibration simulation result is shown in Fig. 14. Up to 310 μ s after PLL is started, a wide TDC nonlinearity estimation bandwidth is employed to help faster convergence. After 310 μ s, a low TDC nonlinearity estimation bandwidth is used to average out the noise from other sources. TDC calibration settles within 400 μ s.

VI. EXPERIMENTAL RESULTS

This digital PLL, implemented in a 14-nm fin-shaped field effect transistor (FinFET) CMOS process technology,

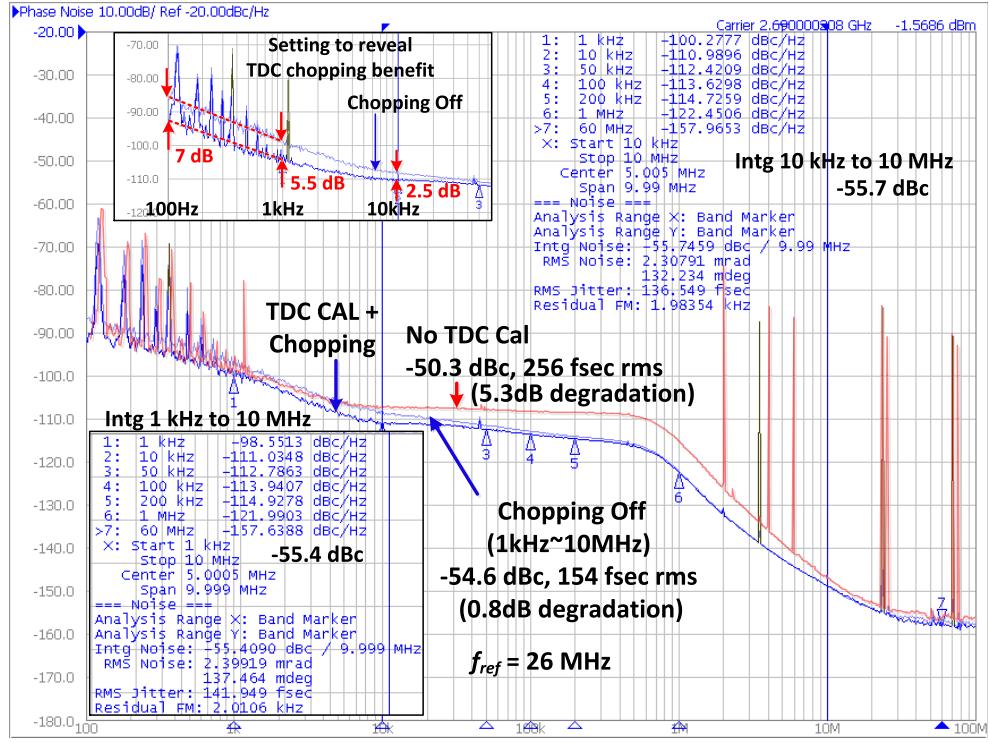


Fig. 15. Phase noise and IPN measurement.

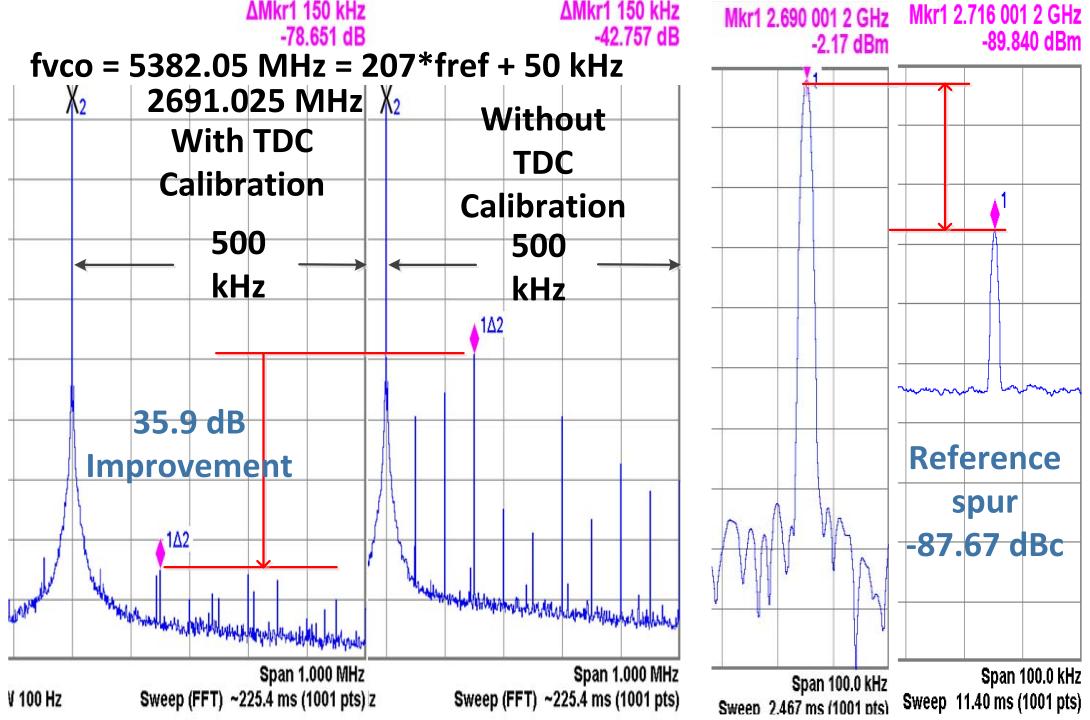


Fig. 16. Fractional and reference spurs measurement.

is incorporated into a cellular RF integrated circuit supporting advanced CA operations. The reference clock is 26 MHz. The frequency synthesizer performance is measured at 2.7-GHz band transmitter output. As shown in Fig.15, for $f_{DCO} = 5380$ MHz ($f_{ref} \cdot 206.963$), the IPN of 2690-MHz output

integrated from 10 kHz to 10 MHz is -55.7 dBc or 137-fs rms. IPN integrated from 1 kHz–10 MHz is -55.4 dBc or 142-fs rms. Without TDC calibration, the IPN degrades by 5.3 dB. Without TDC chopping, the IPN degrades by 0.8 dB. The phase noise at low offset frequencies is limited

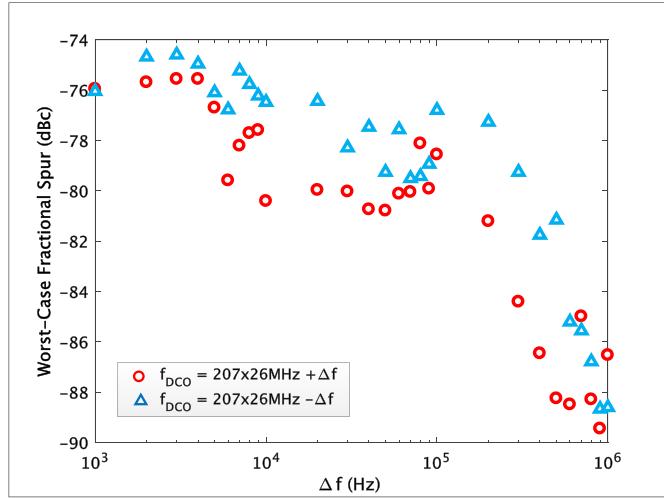


Fig. 17. Worst case fractional spur (measured at half of f_{DCO}) versus f_{DCO} .

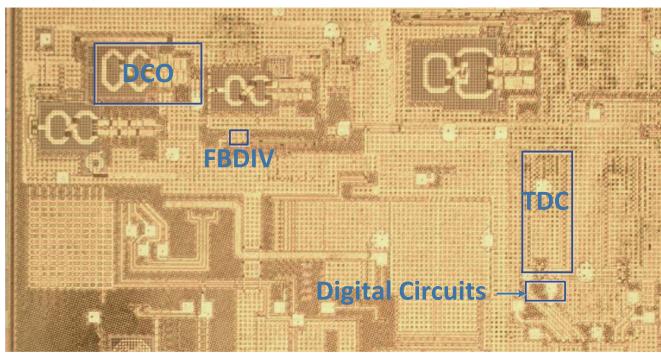


Fig. 18. Chip micrograph.

by the reference clock buffer. Since the flicker noise from the reference clock buffer is not attenuated by TDC chopping, it prevents us from observing the true improvement of the TDC chopping technique. To better reveal TDC chopping benefit, we can use a different reference clock buffer regulated supply voltages to tradeoff reference clock buffer phase noise at higher offset frequencies for better phase noise at lower offset frequencies. TDC chopping improvements with this setting at 100-Hz, 1-kHz, and 10-kHz offsets are 7, 5.5, and 2.5 dB, respectively. Even with this setup, the phase noise at low offset frequencies is still likely limited by the reference clock buffer, thus preventing us from observing the 10-dB minimum improvement predicted by simulation results shown in Fig. 4. With temperature varying within ± 60 °C from the calibration temperature, the IPN variation is within 1 dB.

As shown in Fig. 16, with calibration, the worst case fractional spur is improved from -42.7 to -78.6 dBc for $f_{DCO} = f_{ref} \cdot 207 + 50$ kHz = 5382.05 MHz. (Output is 2691.025 MHz.) The reference spur is -87.6 dBc. The high fractional spurs without calibration suggests that the TDC linearity is limited by layout mismatch, and the fractional spurs without calibration is expected to improve with a better layout. With temperature varying within ± 60 °C from the calibration temperature, the fractional spur variation is within 12 dB. Fig. 17 shows the worst case fractional

TABLE I
DIGITAL PLL POWER CONSUMPTION BREAK DOWN

Component	Power Consumption (mW)	Percentage
PFD, TDC and SARADCs	1.8	13.43%
DCO	6.1	45.52%
DCO dithering	0.6	4.48%
DCO buffers	3	22.39%
Feedback Divider	1	7.46%
Digital PLL Digital Circuit	0.9	6.72%
Total	13.4	100.00%

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	[7] Yao JSSC 2013	[8] Gao ISSCC 2016	[17] Levantino JSSC 2014	[18] Temporiti JSSC 2010	[19] Wang ISSCC 2008	This Work
Technology	180 nm	28 nm	65 nm	65 nm	180 nm	14 nm
TDC/DTC Resolution (ps)	5.2	0.7	0.3	6.8	N/A	0.2
Reference (MHz)	52	40	40	35	12	26
Output Frequency (MHz)	3200	5825.1	3600	3500	2400	2690
RMS jitter (fsec)	230	159	N/A	N/A	N/A	137
In-band Phase Noise (dBc/Hz)	-109.6 100 kHz	-105.5 100 kHz	-103 100 kHz	-101 1 MHz	-98 100 kHz	-113.6 100 kHz
In-band PN Normalized to 2690 MHz (dBc/Hz)	-111.1	-112.2	-105.53	-103.3	-97	-113.6
Near-integer Fractional spur Reference spur	-55	-54	-52	-58	-64	-78.6
Power (mW)	17	8.2	4.2	8.7	27.1	13.4
FOM [20]	-240.4	-246.8	N/A	N/A	N/A	-246
Area (mm ²)	0.62	0.3	0.2	0.44	4	0.257

spur within ± 1 -MHz offset as a function of DCO frequency near $207 \times f_{ref}$. LTE and 5G cellular systems do not have fractional spur requirements. However, high fractional spurs would increase IPN, and therefore, low fractional spurs would ensure consistent IPN performance across all channels.

The complete PLL draws 13.4 mW. The power break down of this work is shown in Table I. The TDC, PFD, and SARADCs together draw 1.8 mW. DCO buffer and DCO $\Delta \Sigma M$ draw 3 mW and 0.6 mW, respectively. The DCO without the $\Delta \Sigma M$ draws 6.1 mW. The feedback divider and the digital PLL digital circuits draw 1 mW and 0.9 mW, respectively. Fig. 18 shows the chip micrograph. The core area, excluding the routing to meet chip floorplan requirements, is 0.257 mm². Performance summary and comparison are shown in Table II. For a fair comparison, the phase noise $L\{\Delta f\}$ reported at frequency f_{out} is normalized to 2690 MHz using the following equation:

$$L_{normalized}\{\Delta f\} = L\{\Delta f\} - 20 \log_{10} \left(\frac{f_{out}}{2690 \text{ MHz}} \right).$$

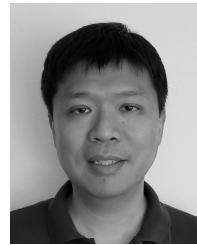
This design achieves better fractional spurs and better normalized in-band phase noise comparing to prior art. It draws higher power than [8]. However, cellular system introduces power overhead to support multiple DCOs (3 in our case), to reduce DCO buffer phase noise floor for 2G cellular transmitter application and to reduce DCO quantization noise. Our measured fractional spur is 11 dB better than the simulated -67 dBc from [17], which applies a similar linearization technique to a DTC-based digital PLL.

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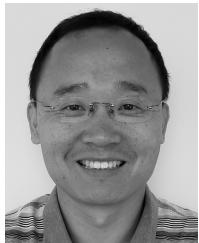
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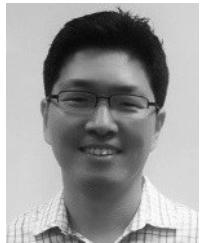
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