

Triple-Mode, Hybrid-Storage, Energy Harvesting Power Management Unit: Achieving High Efficiency Against Harvesting and Load Power Variabilities

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Abstract—This paper presents a triple-mode, hybrid storage, energy-harvesting power management unit (EH PMU) that interfaces a photovoltaic cell, a regulated load, and a rechargeable battery. The objective is to maximize the end-to-end conversion efficiency of the EH PMU against temporal mismatch and variabilities of harvesting and load power. To minimize the involvement (charging or discharging) of a battery in the voltage conversion process, the proposed hybrid energy storage employs both battery and capacitor, which increases transient energy buffering capability and reduces the overall power conversion loss. Measurement results with 65-nm test chips show that the proposed EH PMU can achieve up to 2.2 \times higher end-to-end conversion efficiency than the conventional dual-mode architectures under testing cases emulating realistic load and harvesting power variabilities. We also devised a framework for the system design to guide capacitor sizing, buffering voltage range selection, and end-to-end efficiency tradeoffs.

Index Terms—DC–DC converter, energy harvesting, Internet of Things (IoT), power management, switched capacitor (SC).

I. INTRODUCTION

THE vision of the Internet of Things (IoT) projects deployment of trillions of devices virtually everywhere. Integrated with sensing, computation, and communication capabilities, these devices will boost productivity and ultimately transform our everyday life experience. One of the biggest challenges in realizing the vision of IoT systems lies in powering all these devices in a practical and cost-effective way. Frequently recharging and/or replacing batteries of trillions of devices can significantly increase maintenance cost. In this aspect, energy harvesting garners a significant amount of attention [1], [3]–[10], [15] as it can enable energy-autonomous operations of IoT devices.

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A photovoltaic (PV) cell, which converts light into electrical energy, is one of the most attractive harvesting modalities due to its high efficiency and low cost. Consequently, designing PV energy-harvesting power management unit (EH PMU) has been an active research area [3]–[10].

Fig. 1(a) shows a conventional EH PMU architecture with two converters in series: one for transferring energy from a PV cell to a battery and the other from the battery to a load. This architecture, however, suffers from the fact those two converters always performs high-ratio voltage conversion. Typically, PV-cell output voltage (V_{PV}) is in the range of 0.3–0.6 V, Li-ion battery charging voltage (V_{Bat}) is in the range of 3–4 V, and the load supply voltage (V_{Load}), considering energy-efficient near/sub-threshold circuits, is in the range of 0.3–0.6 V. Therefore, in the worst case, this conventional architecture can perform >100 \times cumulative ratio voltage conversion.

These high-ratio conversions can cause substantial loss in the end-to-end conversion efficiency. Particularly, switched-capacitor (SC) dc–dc converters, which have gained increased popularity for the on-chip integration capability [1], [2], [4], [6], [7], [9], [13], [15], [16], often exhibit decreasing conversion efficiency as the conversion ratio increases [7], [16]. While inductor-based power converters are more resilient to perform high-ratio voltage conversion, the aforementioned high conversion ratio can introduce a considerable amount of conversion loss even in those converters [3].

To avoid such high-ratio conversion, an alternative architecture has been proposed [3]–[5], [7] [Fig. 1(b)]. This architecture has two modes of operation: charging-direct and discharging-direct modes. In the charging-direct mode, it establishes a direct path from a PV cell to V_{Load} to power a load while regulating V_{Load} by storing excessive energy in a battery. In the discharging-direct mode, the load receives power through the direct path and the discharging path from the battery to V_{Load} . This architecture can reduce the amount of energy that flows through high conversion ratio paths, i.e., the paths between V_{Bat} and V_{Load} , improving the overall conversion efficiency. Note that [7] is slightly different from [3]–[5] in the sense that it uses a bidirectional converter for the converter between the battery and the load. But the operations are roughly the same.

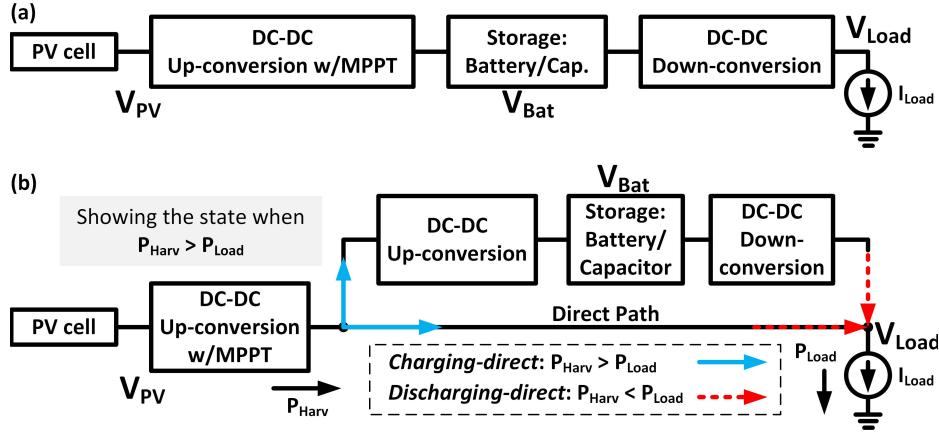


Fig. 1. Conventional EH PMU architectures. (a) Single-mode architecture with two converters in series. (b) Dual-mode architecture with charging-direct and discharging-direct modes.

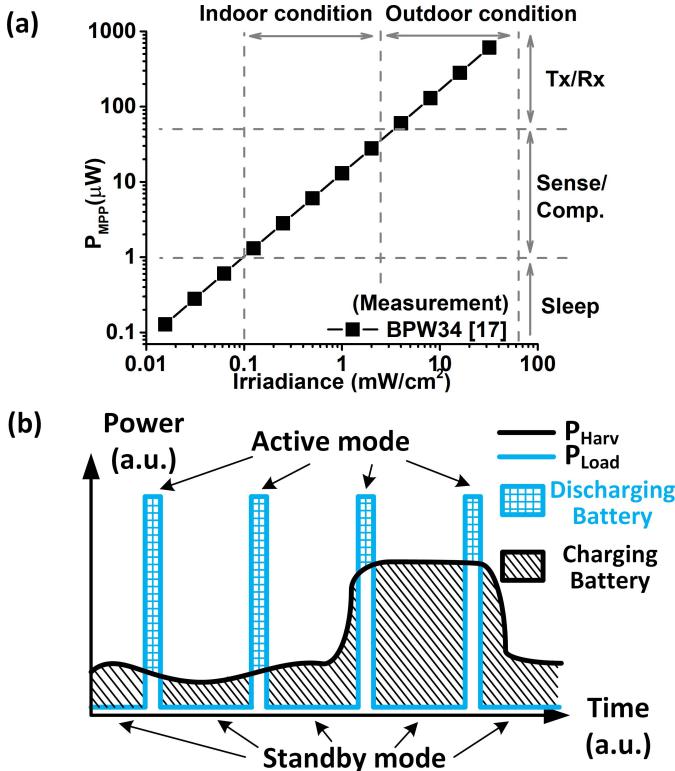


Fig. 2. (a) PV harvesting power values for different lighting conditions are shown, along with typical IoT node power dissipation. (b) Temporal variations of harvested energy and load power dissipation cause frequent battery charging and discharging, degrading end-to-end energy efficiency.

However, in this dual-mode architecture, the amount of energy that travels through the high conversion ratio paths between V_{Bat} and V_{Load} is dependent on the difference between the harvested power (P_{Harv}) and dissipated power (P_{Load}). In practice, considering typical ranges of harvested power and IoT node power dissipation across operating modes [Fig. 2(a)], there exists almost always a substantial temporal mismatch between P_{Harv} and P_{Load} , due to the widely varying lighting conditions [18], as well as varying power dissipation in different operating modes of a load (e.g., data transmission, sensing/computation, and sleep). In Fig. 2(b), an IoT node with active/sleep mode is illustrated as an example, where

significant temporal variation of power dissipation forces a substantial portion of the energy to be either charged to or discharged from the battery, leading to high conversion ratio loss and lower end-to-end conversion efficiency.

To address this challenge, in this paper, we propose a novel EH PMU architecture that has three modes of operation, namely, charging-direct, discharging-direct, and direct modes (Fig. 3). In the newly added direct mode, the proposed architecture only uses the direct path from a PV cell to a load, which involves smaller conversion ratio. The path also contains a capacitor, which serves as an intermediate energy storage and thus allows the voltage of the capacitor (V_{Cap}) to fluctuate within a set range. This enables the proposed architecture to use the direct path without battery involvement even under a temporal mismatch of P_{Harv} and P_{Load} , improving the end-to-end energy efficiency of the EH PMU. Although our architecture is based on SC converters, it can be realized with inductive converters. Inductive converters typically have higher conversion efficiency, yet it can also suffer from low conversion efficiency for performing a large ratio of voltage conversion [3]. Thus maximal utilization of low conversion ratio path under harvester and load power mismatches can improve end-to-end conversion efficiency.

A test chip of the proposed PMU architecture was fabricated in 65-nm CMOS. The measurements show that the proposed architecture achieves up to $2.2 \times$ higher end-to-end conversion efficiency over the conventional dual-mode architecture under typical P_{Harv} and P_{Load} variation scenarios. We also analyzed the effectiveness of the architecture and generated a framework for system design that guides capacitor sizing and capacitor voltage range selection for maximal efficiency improvement.

This paper is organized as follows: In Section II, we introduce the proposed system architecture and circuit design. In Section III, we analyze the end-to-end efficiency of the proposed EH PMU and provide comparison with that of the conventional dual-mode architecture. Section IV presents the test chip prototyping and measurement results. Section V outlines the system design framework of the proposed EH PMU architectures including intermediate capacitor sizing and buffering voltage range selection. Finally, in Section VI, we conclude the paper.

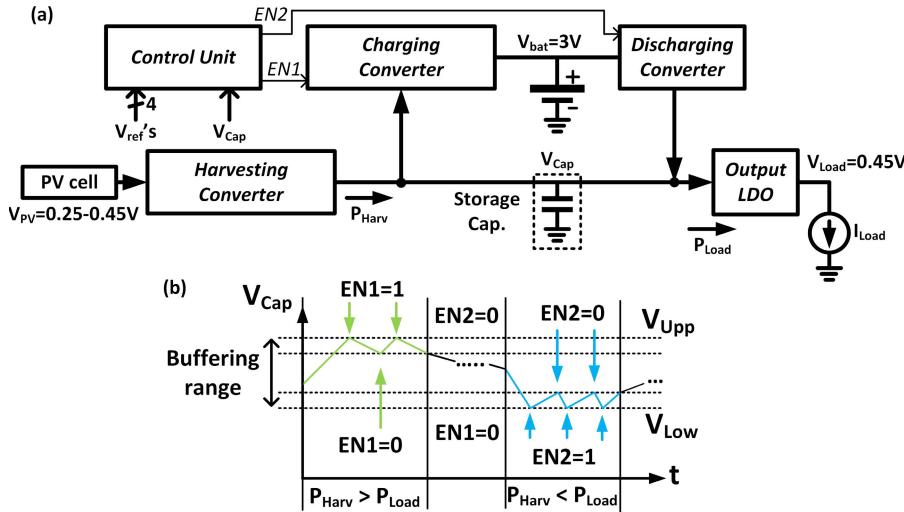


Fig. 3. (a) Proposed triple mode EH PMU architecture with hybrid energy storage in battery and capacitor. (b) Hysteresis control scheme to switch among the three operating modes.

II. ARCHITECTURE DESIGN

A. Proposed EH PMU Architecture

Fig. 3(a) shows the proposed EH PMU architecture. It consists of three SC dc–dc converters and one digital low-dropout regulator (LDO), along with a battery and a capacitor. The first SC dc–dc converter, denoted as harvesting converter, interfaces a PV cell to the capacitor, converting from V_{PV} to V_{Cap} . The second converter, denoted as charging converter, delivers the excessive amount of power to the battery (charging), converting from V_{Cap} to V_{Bat} . The third converter, denoted as discharging converter, supplies the load the necessary power in case the power harvested by the PV cell is not sufficient, converting from V_{Bat} to V_{Cap} . Finally, a digital LDO regulates V_{Load} to the desired voltage level.

The proposed EH PMU operates in one of the three modes, namely, direct, charging-direct, and discharging-direct modes. A control unit, built with comparators and digital logic circuits, switches among the three modes based on the level of V_{Cap} . Fig. 3(b) shows the principle of the mode change control. If $P_{Hav} > P_{Load}$, the excessive power charges the capacitor and raises V_{Cap} . If V_{Cap} crosses an upper threshold (V_{Upp}), it asserts the enable signal (EN1) of the charging converter to store the excessive amount of harvested energy in the battery (i.e., charging-direct mode).

Similarly, if $P_{Hav} < P_{Load}$, the capacitor gets discharged and decreases V_{Cap} . When V_{Cap} crosses the lower threshold (V_{Low}), it asserts the enable signal (EN2) of the discharging converter to supply power from the battery to the load (discharging-direct mode).

Finally, if $P_{Hav} \approx P_{Load}$, both the charging and discharging converters are disabled and the PV cell via the charging converter directly powers the load. Any temporal mismatch between P_{Hav} and P_{Load} is buffered by the intermediate storage capacitor without involving battery charging and charging. In essence, this scheme regulates V_{Cap} between V_{Upp} and V_{Low} , creating a range of voltage as a buffering range. Note that we add hysteresis near V_{Upp} and V_{Low} to avoid excessive

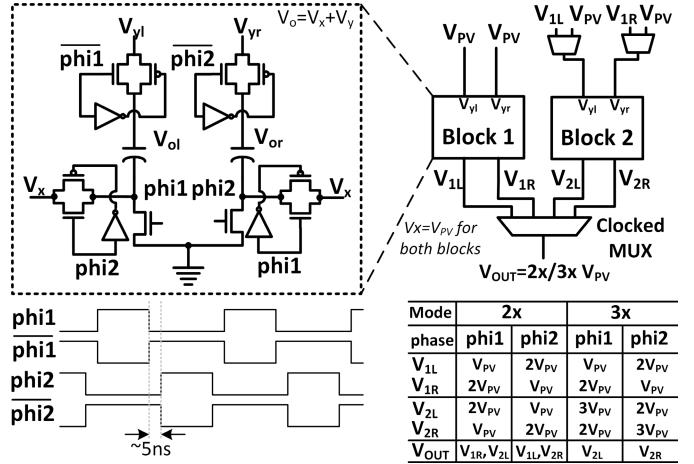


Fig. 4. Harvesting converter schematics.

switching among modes. Other regulation schemes such as pulse frequency modulation can also be used to control the charging/discharging converters.

B. Circuit Design

Fig. 4 shows the schematics of the harvesting converter. It is a step-up converter that can perform 2x or 3x voltage conversion from V_{PV} to V_{Cap} . Specifically, it consists of two unit blocks that can be configured in series for 3x or in parallel for 2x voltage conversion. The settings for each conversion configuration are summarized in Fig. 4 (right bottom). Fig. 4 (left bottom) also shows the waveforms of the non-overlapping clocks (phi1, phi2, and their inverted signals). The parallel configuration in 2x mode can maximize capacitor utilization and thus enable larger power transfer capacity. To support low input voltage (~0.3 V), we used transmission gates in the power transfer path to reduce device ON resistance. Also, the converter generates and uses switching clock and other control signals that swing from 0 to V_{Cap} , further improving the ON resistance of the power transistors.

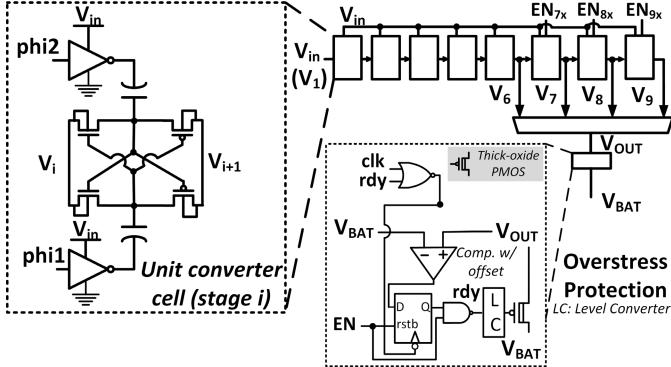


Fig. 5. Schematics of charging converter and overstress protection circuitry.

As shown in Fig. 5, we designed the charging converter based on an 8-stage configurable-ratio charge pump topology. It can perform $6\times$ to $9\times$ step-up operation, converting V_{Cap} to V_{Bat} . We can configure the conversion ratio by skipping some of the last three stages. Fig. 5 (left) shows the unit building block of each stage. High V_i can incur reverse body bias, substantially increasing the ON resistance of the power transistors. To avoid such effects, using deep N well, we connect the body of the NMOS power transistors to the input of the current unit stage (V_i) and the body of PMOS to the output (V_{i+1}).

We used thin-oxide devices in the charging converter to reduce ON resistance while the output voltage of the converter can be as high as 3 to 4 V. Therefore, it is critical to implement overstress protection. Particularly, while the converter is disabled, i.e., while the EH PMU does not charge the battery, the high battery voltage can stress the thin-oxide devices of the charging converters. As shown in Fig. 5, we designed the overstress protection circuitry, which uses a comparator with predefined offset that compares the internal output of the converter and V_{Bat} . If the internal output is smaller than V_{Bat} by a predefined amount, the protection circuitry asserts rdy (i.e., $\text{rdy} = 1$), turning off the thick-oxide output PMOS to isolate V_{Bat} from the thin-oxide devices of the converter. The assertion of rdy gates the clock to the comparator and the flip-flop to save power dissipation. The level converter is designed based on the structure proposed in [19].

The discharging converter is designed based on 2-stage 1/4 step-down architecture (Fig. 6). It down-converts V_{Bat} to V_{Cap} . Fig. 6 shows the schematics of each stage of the converter. Similar to Fig. 4, phi1 and phi2 are non-overlapping clock phases. The transistors on the high side of the stage receive clocks that swing from V_o to V_i , instead of 0 to V_i , which reduces the power dissipation and allows the use of thin-oxide transistors. Similarly, the transistors on the low-side receive clocks that swing from 0 to V_o . Finally, as shown in Fig. 7, we designed the digital output LDO based on the shift-register-based topology [14]. This provides the regulated load supply voltage (V_{Load}) from V_{Cap} .

We designed on-chip clock generators for the three SC dc-dc converters and the output LDO. The clock generators for the harvesting and charging converters and the output LDO are designed based on current-starved ring oscillators

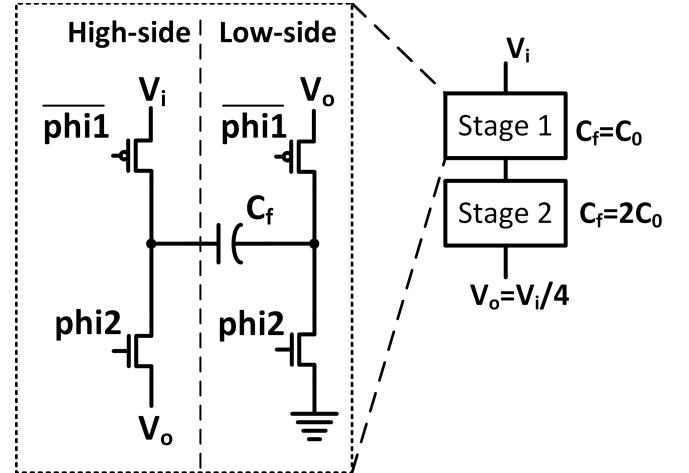


Fig. 6. Discharging converter schematics.

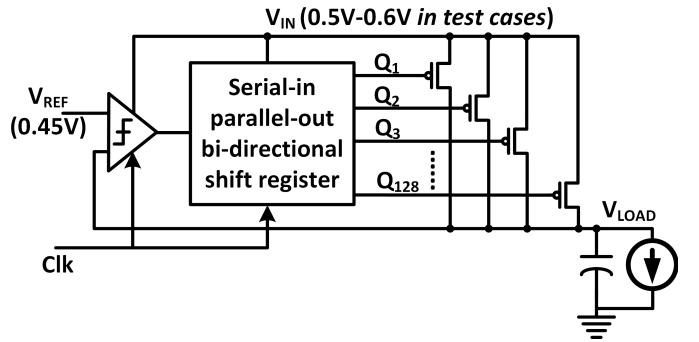


Fig. 7. Digital output LDO schematics.

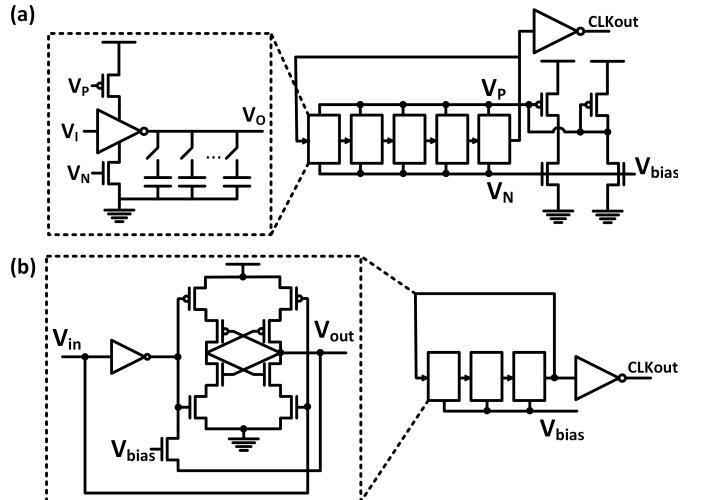


Fig. 8. Clock generator design for (a) harvesting converter, charging converter, and LDO, and (b) discharging converter.

with tunable capacitive loads for frequency tuning [Fig. 8(a)]. These clocks swing from 0 to V_{Cap} . The clock generator for the discharging converter is based on ring-configured delay cells, each of which consists of a self-gated cross-coupled inverter and a leakage device [Fig. 8(b)]. We can tune the oscillation frequency by modulating the gate bias of the leakage device [6]. This clock swings from 0 to V_{Bat} .

Since the clock of the harvesting converter swings from 0 to V_{Cap} , if no charge is stored in the capacitor or battery, the clock

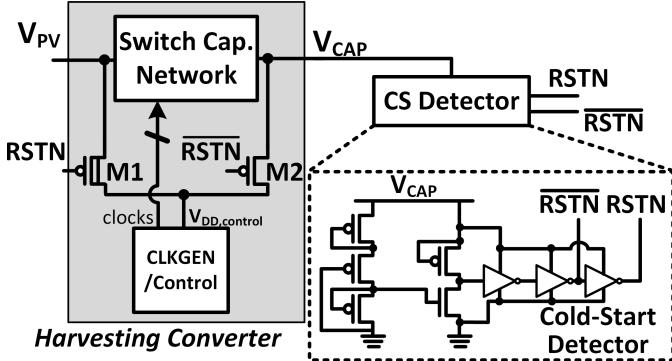


Fig. 9. Self-start circuits including the cold-start detector.

generator cannot function, requiring the harvesting converter to have self-start capability. For implementation of the self-start circuitry, as shown in Fig. 9, we added two PMOS transistors (M1 and M2) and a cold-start detector (similar to [12]). If V_{Cap} is lower than a predefined threshold (i.e., not enough charge resides in the capacitor), it makes V_{PV} to provide power to the clock generator so as to perform cold start. As V_{Cap} increases and crosses a predefined threshold of ~ 0.35 V, RSTN switches to 1, and this makes V_{Cap} to power the clock generator and other controls. While it is possible to keep using V_{PV} , the use of V_{Cap} is desirable to reduce the ON resistance of the power transistors and thus improving the conversion efficiency of the charging converter. Note that we used a thick-oxide device for the PMOS for V_{PV} (M1) to reduce the leakage in the normal non-cold-start operation (Fig. 9).

We performed corner and Monte Carlo simulations to evaluate the robustness of the cold-start technique. As shown in Fig. 10(a), the predefined threshold (V_{trip}) of the cold-start detector varies by 110 mV across process corners. Its power consumption is in the range of tens of nanowatts, small enough not to have a large impact on the efficiency of the EH PMU. Fig. 10(b) shows the results of 250-point Monte Carlo simulation at each of the five process corners. While V_{trip} varies, the detector can robustly assert RSTN to start and stop the cold-start process.

It is noteworthy that our proposed EH PMU architecture may frequently enable and disable the charging and discharging converters if P_{Load} and P_{Harv} largely vary. Frequent enabling and disabling of the converters can waste a considerable amount of energy since the charge stored in the flying capacitors while the converters are enabled can be lost via leakage while the converters are disabled. To save this energy, we can use a charge-retention technique such as one proposed in [13].

III. END-TO-END ENERGY EFFICIENCY ANALYSIS OF EH PMU

In this section, we analyze the end-to-end energy efficiency of the proposed EH PMU. To do so, we first define a metric for the efficiency (Eff_{ov}). The conventional power conversion efficiency metric (PCE) used for individual converters is not sufficient for the evaluation of end-to-end efficiency, since it cannot capture the impact of charging and discharging of

energy storages. Therefore, we propose Eff_{ov} as

$$\text{Eff}_{\text{ov}} = \begin{cases} \frac{E_{\text{Load}} + E_{\text{Bat}} \cdot \text{PCE}_{\text{discharge}}}{E_{\text{mpp}}}, & \text{if } E_{\text{Bat}} > 0 \\ \frac{E_{\text{Load}}}{E_{\text{mpp}} + |E_{\text{Bat}}| / \text{PCE}_{\text{charge}} / \text{PCE}_{\text{Harvest}}}, & \text{if } E_{\text{Bat}} < 0 \end{cases} \quad (1)$$

where E_{mpp} is the total amount of energy that a PV cell harvests at its maximal power point (MPP); E_{Load} is the total load energy consumption; $\text{PCE}_{\text{discharge}}$ is the measured average PCE of battery-to-load conversion; $\text{PCE}_{\text{charge}}$ is the measured average PCE of capacitor-to-battery (proposed) or load-to-battery [conventional dual-mode architecture, Fig. 1(b)] conversions; $\text{PCE}_{\text{Harvest}}$ is the efficiency of the harvester converter; E_{Bat} is the amount of energy that is charged to or discharged from a battery during a time window (negative if a battery is discharged). Note that, we do not include the LDO efficiency in the efficiency improvement analysis simply because it equally affects the proposed and the baseline architectures. In this regard, Eff_{ov} is defined as the efficiency from harvester and battery to the input of LDO.

Note that the energy drawn from the battery is what was previously harvested and charged to the battery. Therefore, we need to take the PCEs of harvesting and charging into account in defining Eff_{ov} . Similarly, the energy charged to the battery will be consumed ultimately by the load. Therefore, we include the impact of PCE for the discharging operation in defining Eff_{ov} . Also, note that Eff_{ov} has no terms related to the change of energy stored in the capacitor. This is because in the test case studies, for simplicity, we assume that the EH PMU system operates in steady state in the energy perspective, i.e., the amounts of energy flowing in and out of the capacitor are roughly the same. Incorporating the capacitor energy storage into Eff_{ov} can be used for more generalized studies.

We also constructed a simplified test case that emulates practical P_{Harv} and P_{Load} variations. We focus on short-term (e.g., a few seconds) temporal mismatch of P_{Harv} and P_{Load} . Therefore, we assume P_{Harv} is constant but P_{Load} changes periodically between active and sleep modes. Fig. 11(a) shows the P_{Harv} and P_{Load} profile of the test case. It can be modeled with three parameters: 1) the active to sleep mode power dissipation ratio of a load ($K_1 = P_{\text{active}} / P_{\text{sleep}}$), 2) the total load energy consumption to harvester energy generation ratio ($K_2 = E_{\text{Load}} / E_{\text{Harv}}$), and 3) the active to sleep mode duration ratio ($K_3 = t_{\text{active}} / t_{\text{sleep}}$).

Using the test case with various parameter values for K_1 , K_2 , and K_3 which are representative for an IoT node system, we analyze and compare the Eff_{ov} of the proposed EH PMU and the conventional dual-mode architecture. We use the representative values (60%) for $\text{PCE}_{\text{charge}}$ and $\text{PCE}_{\text{discharge}}$ based on the test chip measurement (see Section IV). We do not need to specify $\text{PCE}_{\text{Harvest}}$ since it is the same between the proposed triple and the conventional dual-mode architectures and thus has no impact on the comparisons. We also assume that the intermediate energy-storage capacitor is sized large enough not to limit the power transfer over temporal power mismatch in the test case duration. Therefore, for the proposed

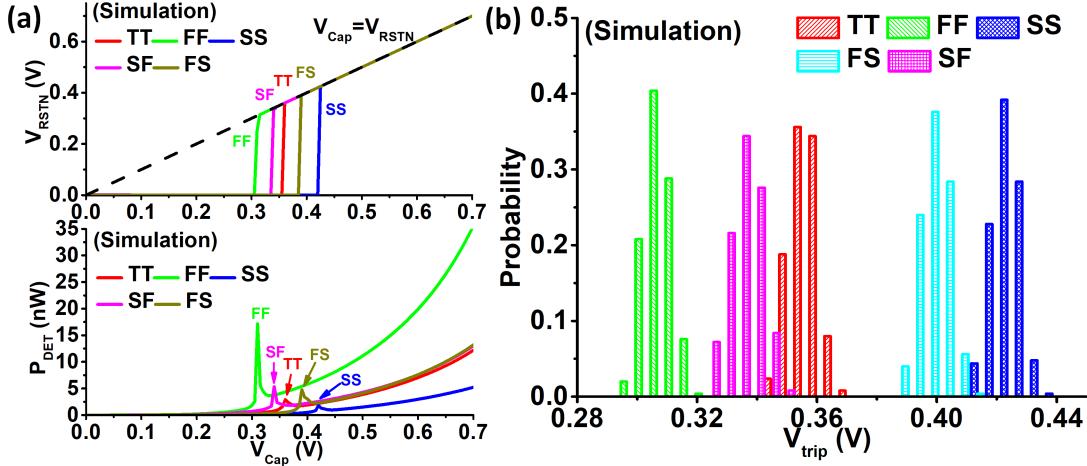


Fig. 10. (a) Robustness of trip point voltage and power consumption of the cold-start detector across corners. (b) Monte Carlo simulations of the trip point voltage at each process corner.

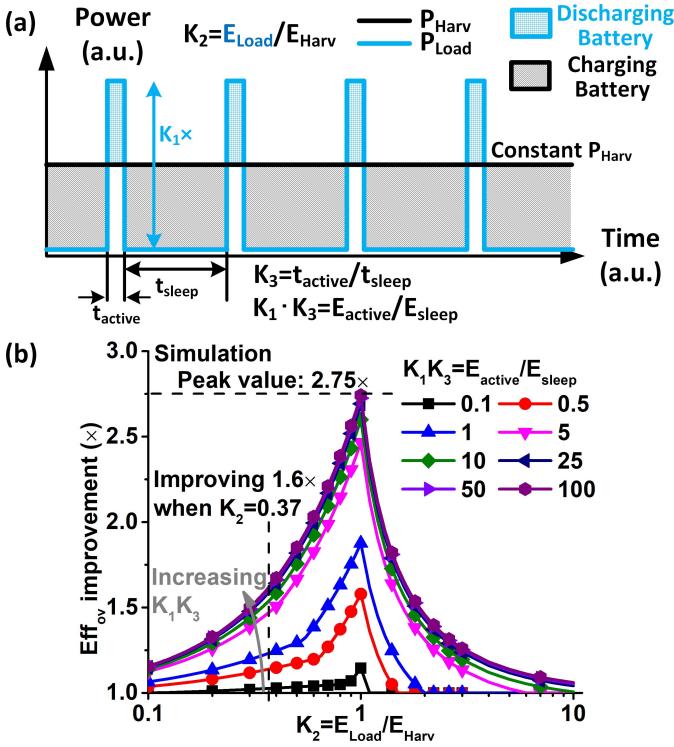


Fig. 11. (a) Simplified test-case emulating P_{Harv} and P_{Load} variations. (b) End-to-end efficiency analysis of the proposed EH PMU architecture.

architecture, only the net difference between E_{Load} and E_{Harv} over the test case duration is charged to or discharged from a battery.

Fig. 11(b) shows the Eff_{ov} improvement of the proposed EH PMU architecture over the conventional dual-mode architecture. Here, we used the V_{UPP} and the capacitor size of our design point. We fixed K_3 at 1% while sweeping K_2 and $K_1 \cdot K_3 (= E_{active}/E_{sleep})$. This analysis shows that the Eff_{ov} improvement of the proposed architecture peaks (2.75) at $K_2 = 1$ and high $K_1 \cdot K_3$ value. It reduces as K_2 deviates from 1 since E_{Bat} dominantly degrades Eff_{ov} in both the

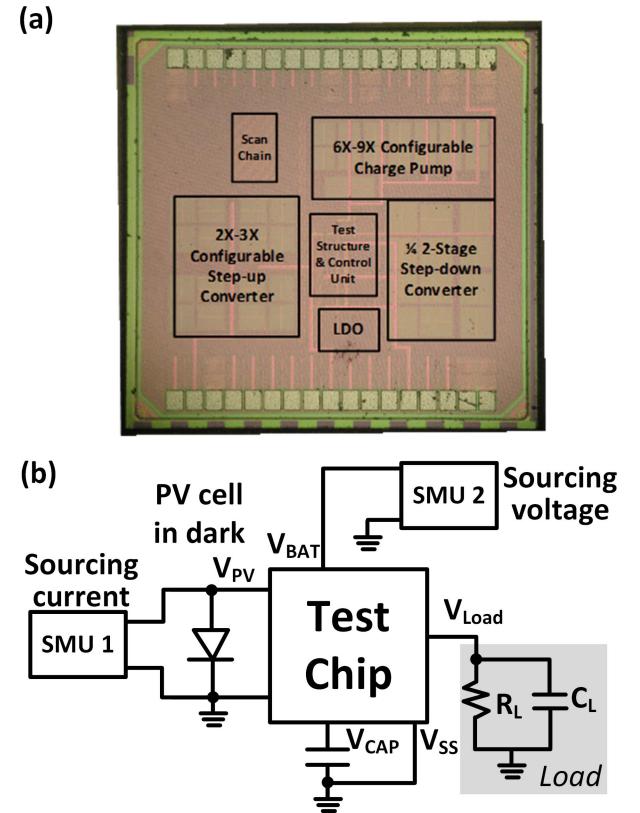


Fig. 12. (a) Die photograph. (b) Testing setup using SMU-based PV cell and rechargeable battery.

proposed and the conventional architectures [see (1)]. Note that the worst case of our proposed architecture happens where it cannot use the storage capacitor and operates similarly with the conventional dual-mode architecture. Specifically, if $K_1 \cdot K_3$ is very small, for example, the variation of load power dissipation becomes small and so does the energy charged to or discharged from the storage capacitor. This makes a large portion of energy flowing to the battery, degrading Eff_{ov} .

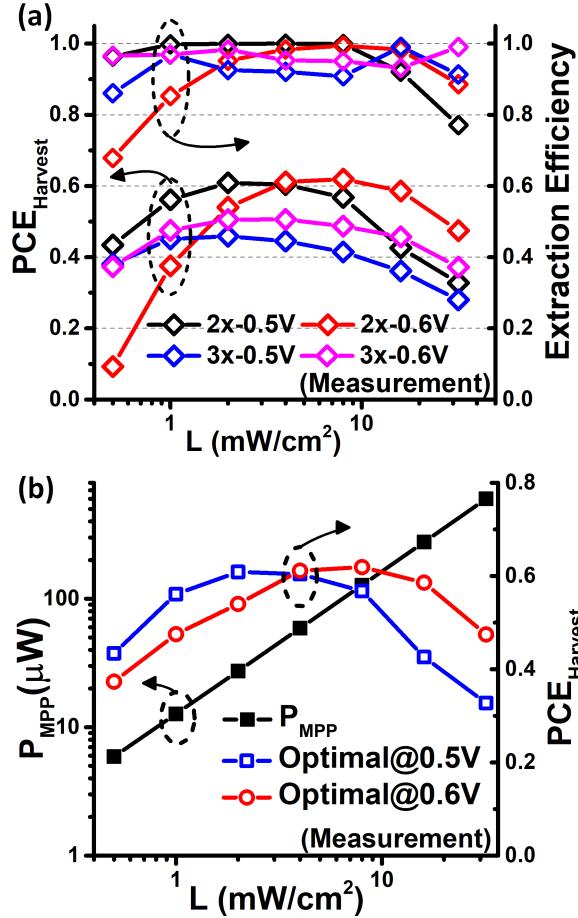


Fig. 13. (a) Harvesting converter conversion efficiency, PV cell extraction efficiency. (b) Output power of PV cell at MPP and optimal harvesting efficiency of the harvesting converter.

IV. TEST CHIP MEASUREMENTS

A. Test Chip Prototyping and Measurement

We fabricated the test chip for the proposed EH PMU in 65-nm CMOS. The target maximum load current of the EH PMU is 140 μ A at 0.45-V load V_{DD} . We use ~ 2 fF/ μ m² metal-insulator-metal (MIM) capacitors to implement the capacitors. The total active area of the design is 0.48 mm², and the die photograph is shown in Fig. 12(a).

We use a PV cell that has a 7.5-mm² radiant sensitive area for measurement. To facilitate the test procedure, instead of using a controllable light source and a real rechargeable battery, we use two source meter units (SMU) to emulate the behaviors of a PV cell and a rechargeable battery. Fig. 12(b) describes the setup, where the first SMU (SMU1) is connected in parallel with a PV cell that is fully covered in dark. This SMU-PV system can emulate PV cell behavior under various lighting conditions simply by adjusting the amount of the current that SMU1 sources. The other SMU (SMU2) is connected to V_{Bat} and V_{SS} , which can emulate a rechargeable battery by operating in the voltage source mode. SMU2 can measure the current coming in and out of the unit, which are roughly equivalent to charging and discharging current.

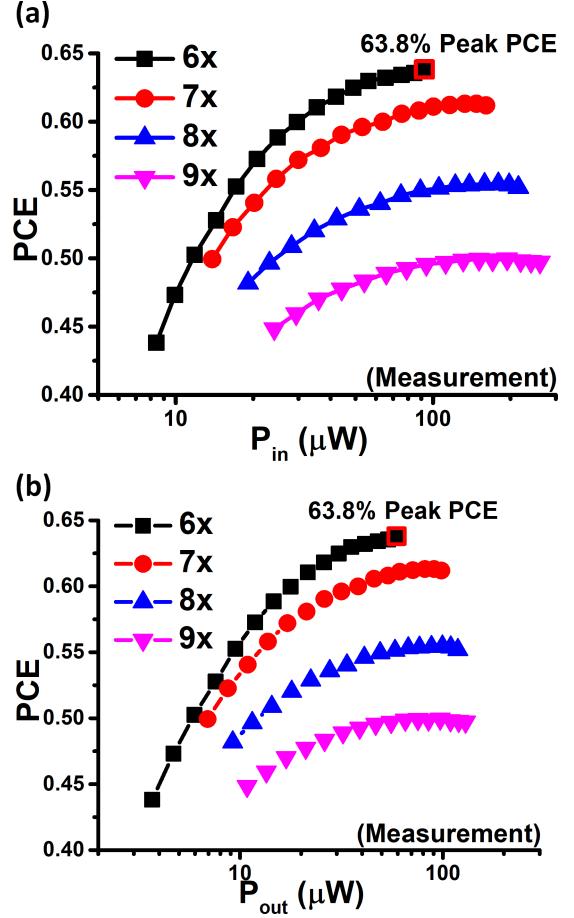


Fig. 14. Power conversion efficiency of the charging converter.

We measured the harvesting efficiency (PCE_{Harvest}) of the harvesting converter across PV cell currents ranging from 0.5 to 32 mW/cm². As shown in Fig. 13(a), the peak PCE_{Harvest} of the converter is measured to be 60.9% for $V_{Cap} = 0.5$ V and 61.9% for $V_{Cap} = 0.6$ V with off-chip maximal power point tracking (MPPT) control. (Our test chip has no on-chip MPPT control loop due to the limited design time.) The extraction efficiency, defined as P_{OUT}/P_{MPP} is also shown in Fig. 13(a), where the P_{MPP} is the output power of the PV cell at the MPP. Fig. 13(b) shows the measured P_{MPP} across varying irradiance levels and the corresponding optimal PCE_{Harvest} of the two operation modes. The maximal P_{MPP} is ~ 600 μ W and the corresponding P_{Harv} is 196 μ W for $V_{Cap} = 0.5$ V and 298 μ W for $V_{Cap} = 0.6$ V.

We also measured the PCE of the charging converter for variable-ratio conversions from 0.6 to 3 V, where the charging converter is enabled when V_{Cap} reaches V_{UPP} (0.6 V in our test cases). As shown in Fig. 14, the peak PCE is measured to be 63.8% at 6 \times conversion and decreases at higher conversion ratios, which are able to convert higher input power. We also measured PCE of the discharging converter (Fig. 15). Converting 3-V V_{Bat} to 0.6-V V_{Cap} , the converter achieves 59.1% peak PCE. When V_{Cap} is 0.5 V, the peak PCE is measured to be 55.8%. At last, we measured the current efficiency of the output LDO. As shown in Fig. 16, operating

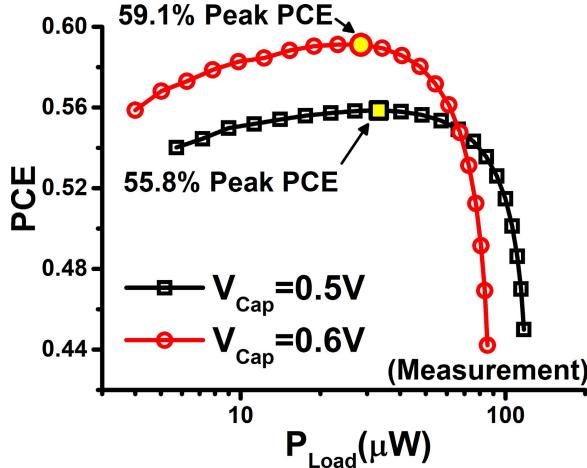


Fig. 15. Power conversion efficiency of the discharging converter.

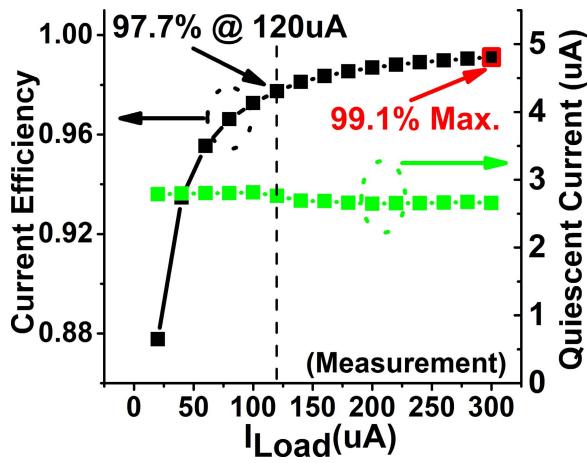


Fig. 16. Current efficiency and quiescent current of the output LDO.

at 1-MHz clock, 0.5-V V_{Cap} , and 50-mV drop-out voltage, the LDO consumes 2.7- μ A quiescent current. Considering a typical load of 120 μ A, the current and power efficiencies are 97.7% and 87.9%. Table I summarizes the measurement results and Table II compares the proposed design with some of the prior works.

B. Test Case Measurement

We configure our proposed EH PMU architecture with the following system parameters: $V_{Upp} = 0.6$ V, $V_{Low} = 0.5$ V, and $C_{Cap} = 0.47$ mF. We choose the capacitor size that is sufficient to handle transient power mismatch between P_{Harv} and P_{Load} . We will have further discussion on optimizing these system parameters in Section V. On the other hand, we emulate the conventional dual-mode architecture by reusing our EH PMU and configuring it with the following system parameters: $V_{Upp} = 0.52$ V, $V_{Low} = 0.5$ V, and $C_{Cap} = 1$ μ F. We cannot completely eliminate C_{Cap} as it causes the control stability issues, but this slightly improves the efficiency of the emulated dual-mode architecture, ensuring fair comparison. Due to the largely reduced buffering voltage range and smaller capacitor, even at the slight mismatch of P_{Harv} and P_{Load} , the EH PMU operates in either charging-direct or discharging-direct mode.

We operate and measure our proposed EH PMU under three test cases that emulate realistic P_{Harv} and P_{Load} variations.

TABLE I
CHIP SUMMARY

Process	65nm CMOS
Area	0.48mm ²
V_{Load}	0.45V
V_{Bat}	3V
Converters	SC DC-DC \times 3 + LDO
Capacitors	First step-up SC:200pF Second step-up SC: 160pF Step-down SC: 240pF 600pF in total (MIM)
Harvesting power	$P_{MPP}=600\mu$ W Max. measured @ $V_{MPP}=0.45$ V P_{Harv}/P_{MPP} : 32% @ $V_{Cap}=0.5$ V, 50% @ $V_{Cap}=0.6$ V
Load Power	LDO: 63 μ W Max. @ 0.5V V_{Cap} Step-down SC: 106 μ W with >0.5 PCE
Peak Conv. Efficiencies	Harvesting: 60.9% @ $V_{Cap}=0.5$ V, 61.9% @ $V_{Cap}=0.6$ V Step-up SC: 63.8% @ 6 \times , 0.6V V_{Cap} Step-down SC: 59.1% @ $V_{Cap}=0.6$ V, 55.8% @ $V_{Cap}=0.5$ V LDO: 97.7% current efficiency @ 120 μ A
End-to-End efficiency	Direct path: 53.3% @ $V_{Cap}=0.5$ V Charging and discharging path: 19.3%

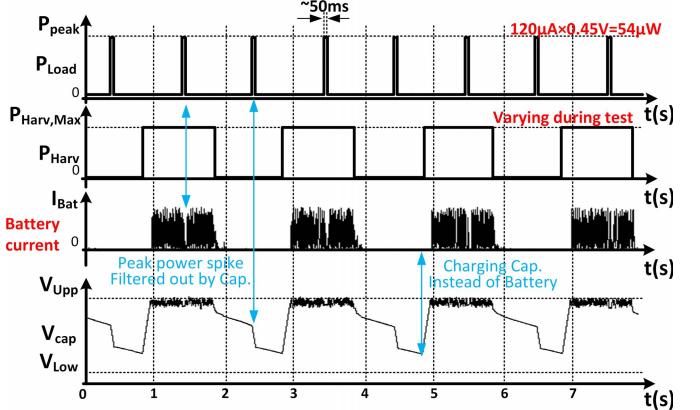


Fig. 17. Example waveforms measured during the Experiment 3. The proposed EH PMU can handle the mismatch between P_{Harv} and P_{Load} , thus minimizing battery involvement.

Table III summarizes the details of the test cases. In the first test case (Experiment 1), we periodically modulate P_{Harv} by enabling and disabling the PV cell output every 1 s. This case can mimic the shading effect, i.e., the PV cell has some shade and thus produces substantially smaller P_{Harv} . In the second test case (Experiment 2), we use a P_{Load} profile that has a 50-ms-long 120- μ A peak power dissipation every 1 s. This mimics the active-sleep mode transition of a load. Finally, in the third test case (Experiment 3), we combine Experiments 1 and 2, i.e., both P_{Harv} and P_{Load} vary in the aforementioned manners. In all three experiments, we consider the lighting level in the range of 0.5–32 mW/cm².

Fig. 17 shows several key waveforms measured during Experiment 3. In the beginning, P_{Harv} is set larger than P_{Load} , assuming the load is in the sleep mode. This increases V_{Cap} toward V_{Upp} as the capacitor is charged. We observe zero battery charging current (I_{Bat}) during this time. Once V_{Cap} crosses V_{Upp} , our proposed PMU enables the charging converter that charges the battery with the excessive amount of

TABLE II
COMPARISON TO PRIOR WORKS

	[3]	[5]	[7]	This work
Architecture	Dual mode	Dual mode	Dual mode	Triple mode
Converters	Inductor based	SC+LDO	SC	SC+LDO
Off-chip components	22 μ H inductor 15 μ F, 47 μ F decaps	No	No	<200 μ F storage cap. @V _{Upp} =0.6V
Process	0.35 μ m	0.18 μ m	65nm	65nm
Area	~2.5mm ²	~0.94mm ²	0.48mm ²	0.48mm ²
Energy storage	Battery	Battery	Capacitor	Battery & capacitor
Voltage levels	Battery: 3.3V Thermal: 20-160mV PV: 0.15-0.75V Piezo.: 1.5-5V Load: 1.8V	Battery: 3.6V PV: ~0.3V Load: 0.4 and 0.5V	Storage cap: 0-3V PV: 1V	Battery: 3V PV: 0.3-0.5V Load: 0.45V
End-to-end efficiency	58%: Thermal; 83%: PV; 79%: Piezo.	38% (Only down conversion reported)	53% (cycle average)	53.3% (direct) 19.3% (up-down)

TABLE III
DETAIL SETUPS OF THE EXPERIMENTS 1–3

Test		I _{load} Variations	P _{PV} Variations	V _{Low} -V _{Upp}	C _{Cap}
Exp. 1	Proposed	Constant 50 μ A	1Hz enabling/disabling	0.5-0.6	0.47mF
	Baseline	Constant 50 μ A	1Hz enabling/disabling	0.5-0.52	1 μ F
Exp. 2	Proposed	120 μ A, T _{active} =50ms, Period=1s	Always enabled	0.5-0.54	0.47mF
	Baseline	120 μ A, T _{active} =50ms, Period=1s	Always enabled	0.5-0.52	1 μ F
Exp. 3	Proposed	120 μ A, T _{active} =50ms, Period=1s	1Hz enabling/disabling	0.5-0.6	0.47mF
	Baseline	120 μ A, T _{active} =50ms, Period=1s	1Hz enabling/disabling	0.5-0.52	1 μ F

harvested power. Non-zero I_{Bat} is observed. Note that I_{Bat} and V_{cap} fluctuate because of the hysteresis-based control (Fig. 2). Specifically, if V_{cap} reaches V_{Upp} , the controller enables the charging converter, and this makes V_{cap} not to rise too much beyond V_{Upp} , and eventually drop to below $V_{\text{Upp}} - \Delta V$, at which the controller disables the charging converter. This makes both I_{BAT} and V_{cap} fluctuate. Shortly, the load enters active mode and starts to draw current, directly from the harvester. This temporarily makes I_{Bat} smaller, creating a notch in the I_{Bat} waveform (denoted by the first blue arrow). Then, P_{Harv} is reduced, assuming the lighting condition gets worse. The load, although in the sleep mode, consumes some amount of power, and thus V_{Cap} reduces. As denoted by the second blue arrow, the load again enters the active mode, consuming the peak amount of power. This creates a steeper slope in the V_{Cap} waveform. Still the sufficiently sized capacitor delivers the necessary power, and therefore no current is drawn from

the battery. Note that V_{Cap} does not cross V_{Low} . After this, P_{Harv} again becomes larger than P_{Load} , and the excessive power is charged into the buffering capacitor, increasing V_{Cap} towards V_{Upp} (denoted by the third blue arrow). Throughout this experiment, our proposed EH PMU operates either in the direct or the charging-direct mode. No battery discharge occurs.

Across all three test cases (i.e., Experiments 1–3), the proposed EH PMU architecture can significantly improve the end-to-end efficiency. In Experiment 1, as shown in Fig. 18, we find that our proposed architecture achieves 1.52× higher Eff_{ov} than the baseline that emulates conventional dual-mode architecture. Especially, the Eff_{ov} improvement is large at the light intensity that makes E_{Harv} similar to E_{Load} . This is because any difference of E_{Harv} and E_{Load} requires charging to or discharging from the battery, worsening Eff_{ov}. This is indeed the same conclusion that we have in the Eff_{ov} analysis

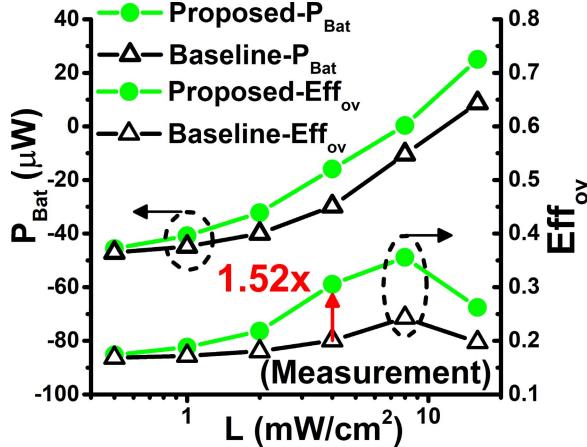


Fig. 18. Battery charging and discharging power (average) and end-to-end efficiency measurement during Experiment 1. The proposed EH PMU achieves up to 1.52× higher Eff_{ov} over the conventional dual-mode architecture.

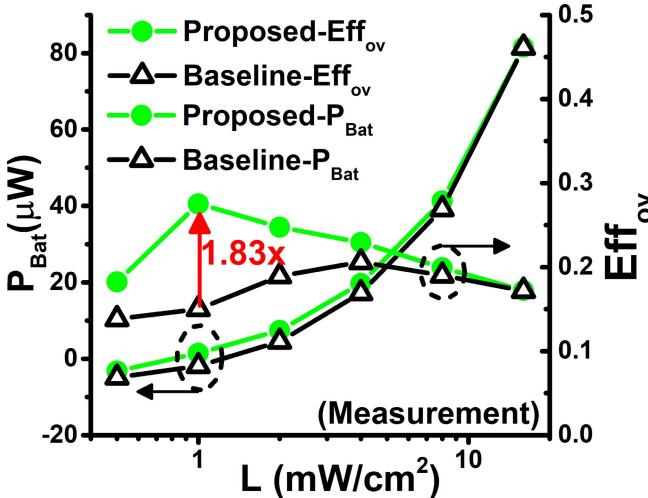


Fig. 19. Battery charging and discharging power (average) and end-to-end efficiency measurement during Experiment 2. The proposed EH PMU achieves up to 1.83× higher Eff_{ov} .

in Section III. Similarly, in Experiments 2 and 3, the proposed EH PMU architecture × and 2.20× higher Eff_{ov} over the baseline that emulates conventional dual-mode architecture (Figs. 19 and 20). Again, we find that Eff_{ov} improvement is large at the light intensities that make E_{Harp} and E_{Load} to be similar. In addition, larger P_{Harp} and P_{Load} variations (used in Experiment 3) benefit the proposed EH PMU architecture.

V. SYSTEM DESIGN FRAMEWORK

In this section, we further analyze the tradeoff among capacitor size, buffering voltage range, and end-to-end efficiency with a goal to provide a system design framework.

The size of the capacitor and buffering voltage range together determine the amount of buffered energy in the intermediate capacitor storage. The capacitor size proportionally increases the buffering capability while the buffering voltage range has a more complicated relationship. In the first order, the amount of energy buffered in the capacitor increases quadratically with the buffering voltage range. However, as we increase the buffering voltage range, i.e., increasing V_{Upp} , the linear loss of the last output LDO proportionally increases.

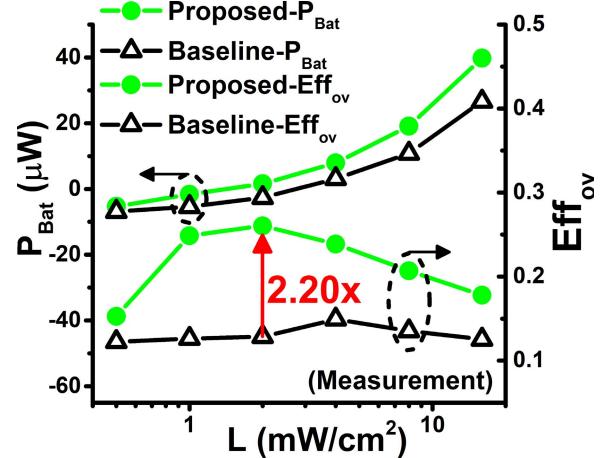


Fig. 20. Battery charging and discharging power (average) and end-to-end efficiency measurement during Experiment 3. The proposed EH PMU achieves up to 2.20× higher Eff_{ov} .

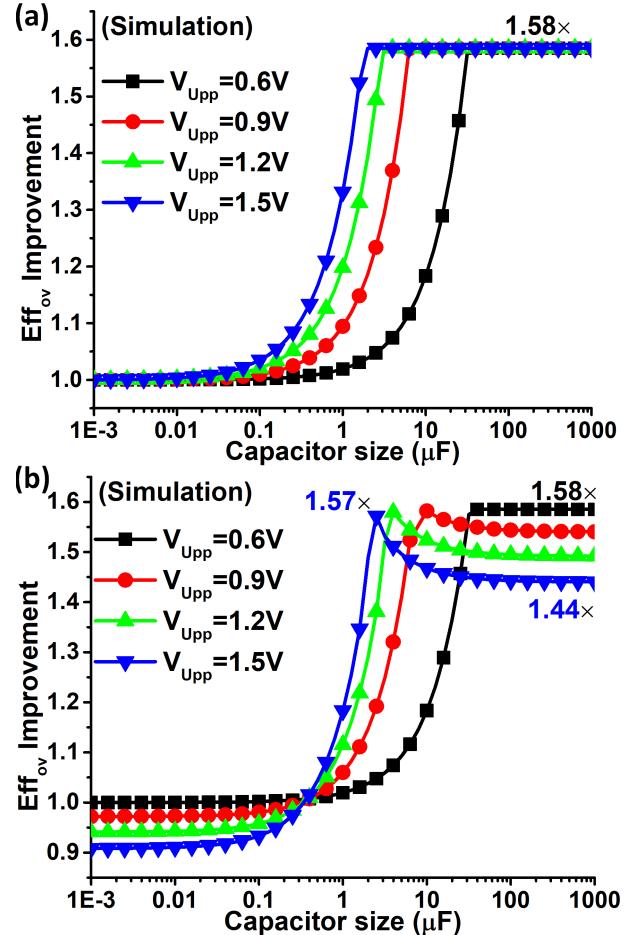


Fig. 21. Tradeoff among capacitor size, buffering voltage range (V_{Upp}) and Eff_{ov} improvement over the conventional dual-mode architecture. (a) Results without considering converters' PCE dependencies on V_{Cap} . (b) Results with considering the dependencies. At $E_{\text{Load}}/E_{\text{Harp}} = 0.4$, the maximal Eff_{ov} improvement is ∼1.58× for both (a) and (b).

We can reduce such loss by replacing the output LDO with a more efficient SC dc–dc converter. However, as we discussed in Section I, SC dc–dc converters indeed exhibit lower PCE with an increasing voltage conversion ratio. Furthermore,

```

1 // PCE0: PCEDischarge from VBat to VLoad; independent of VCap
2 // PCE1: PCEHarvest; function of VCap
3 // PCE2: PCECharge; function of VCap
4 // PCE3: Conversion PCE from VCap to VLoad; function of VCap
5 // We use Linear interpolation to find PCE1, PCE2, PCE3 as a function of VCap
6 // Eq1(EBat, Eharvest, PCE0, PCE1, PCE2): Equation (1) calculating Effov
7 // when cap is small, VCap fluctuate between upper/lower bound
8 PCE3previous = PCE3((VUpp + VLow)/2); // initial PCE3, as VCap fluctuate btw. VUpp & VLow
9 PCE1previous = PCE1((VUpp + VLow)/2); // initial PCE1, as VCap fluctuate btw. VUpp & VLow
10 For CCap = CCap,min: CCap,step: CCap,max {
11     Ecap-active = (Pactive/PCE3previous - Pharvest · PCE1previous) · Twindow · K3;
12     Ecap-sleep = (Pharvest · PCE1previous - Psleep) · Twindow · (1-K3);
13     Ebuffer = CCap · (VUpp2-VLow2);
14     if (Ecap-active>Ecap-buffer & Ecap-sleep>Ebuffer) { // VCap reach both boundaries
15         EBat = (Ebuffer - Ecap-active)/PCE0 + (Ecap-sleep - Ebuffer) · PCE2((VUpp + VLow)/2);
16         Effov = Eq1(EBat, Eharvest, PCE0, PCE2((VUpp + VLow)/2));
17     } else {
18         if (Ecap-active > Ecap-sleep) { // VCap stays near VLow
19             // x: actual higher bound of VCap during test
20             x = solve (CCap · (x2-VLow2) == Ecap-sleep);
21             PCE3previous = PCE3((x + VLow)/2);
22             PCE1previous = PCE1((x + VLow)/2);
23             EBat = (Ecap-sleep - Ecap-active)/PCE0; // EBat<0
24             Effov = Eq1(EBat, Eharvest, PCE0, PCE1((x+VLow)/2), PCE2((x+VLow)/2));
25         } else { // VCap stays near VUpp during test
26             // x: actual lower bound of VCap during test
27             x = solve (CCap · (VUpp2-x2) == Ecap-active);
28             PCE3previous = PCE3((x + VUpp)/2);
29             PCE1previous = PCE1((x + VUpp)/2);
30             EBat = (Ecap-sleep - Ecap-active) · PCE2((x+VUpp)/2); // EBat>0
31             Effov = Eq1(EBat, Eharvest, PCE0, PCE1((x+VUpp)/2), PCE2((x+VUpp)/2));
32     }
33 }
34 }

```

Fig. 22. Framework to evaluate the tradeoff between capacitor size, buffering range selection, and end-to-end efficiency of the proposed EH PMU architecture.

as V_{Cap} gets higher, the harvesting converter also becomes less efficient, again due to the increasing conversion ratio. On the other hand, higher V_{Cap} requires smaller voltage conversion for the charging converter (i.e., V_{Cap} to V_{Bat}), improving its conversion efficiency.

To understand these tradeoffs, we created a framework that can estimate the end-to-end efficiency of the proposed EH PMU (Fig. 21). This framework takes inputs, namely, P_{Harv} (average harvesting power); P_{active} (load power dissipation during active mode); P_{sleep} (load power dissipation during sleep mode); t_{active} (active mode time); t_{window} (steady-state time window); V_{Low} (lower bound of buffering voltage range); V_{Upp} (upper bound of buffering voltage range), and produces Eff_{ov} . The PCE₀, PCE₁ (=PCE_{Harvest}), and PCE₂ are PCE of discharging, harvesting, and charging converters, respectively. PCE₃ is PCE of the last down conversion from

V_{Cap} to V_{Load} , which the digital LDO performs in the current design. We assumed for higher V_{Upp} , a SC dc–dc converter will be used to this conversion. $E_{cap-active}$ and $E_{cap-sleep}$ represent the amount of energy discharged from and charged to the capacitor during the active period and sleep period, respectively. E_{buffer} is the amount of energy that C_{Cap} can store (provide) while V_{Cap} increases (decreases). Note that the power profile in Fig. 21 has been represented by K_1 , K_2 and K_3 in the same manner as they are in Section III. We can evaluate the framework while increasing C_{cap} (intermediate storage capacitor size) in a small step size. By comparing Eff_{ov} values from the framework evaluations, we can find the optimal system parameters.

Note that V_{Cap} is a complex function of various parameters including power profile, capacitor size, V_{Upp} , etc. To precisely solve for V_{Cap} , therefore, we would need to perform an

iterative process which increases complexity of the framework. Instead, we approximated the converter efficiencies (which are functions of V_{Cap}) by using the efficiency values that were found in the previous evaluation with one-step smaller capacitor size, i.e., using $\text{PCE}_{1\text{previous}}$ and $\text{PCE}_{3\text{previous}}$ instead of PCE_1 and PCE_3 in calculating $E_{\text{cap-active}}$ and $E_{\text{cap-sleep}}$ (line #11 and 12 in Fig. 21). As long as we use a fine-grained step in the capacitor size sweep, this approximation causes little error.

As an example, we evaluated the framework with the following parameters: $P_{\text{harvest}} = 10 \mu\text{W}$, $P_{\text{active}} = 360 \mu\text{W}$, $P_{\text{sleep}} = 0.360 \mu\text{W}$, $t_{\text{active}} = 10 \text{ ms}$, $T_{\text{window}} = 1 \text{ s}$, $V_{\text{Low}} = 0.5 \text{ V}$, and $V_{\text{Upp}} = [0.6, 0.9, 1.2, 1.5 \text{ V}]$. These parameters result in $E_{\text{Load}}/E_{\text{Harv}} = 0.4$, $t_{\text{active}}/t_{\text{window}} = 1\%$, and $P_{\text{active}}/P_{\text{sleep}} = 1000$. Fig. 22(a) shows the results of the framework evaluations, i.e., Eff_{ov} improvement of the proposed EH PMU architecture over the conventional dual-mode architecture as a function of C_{cap} . Here we assume the PCEs of the converters are roughly constant across V_{Cap} , i.e., the increased loss when converting from higher V_{Cap} to V_{Load} and from V_{PV} to higher V_{Cap} , as well as reduced loss when converting from higher V_{Cap} to V_{Bat} , are all neglected. In Fig. 22(b), we considered the impact of V_{Cap} on the PCEs in evaluating the framework.

Both results show that increasing C_{cap} benefits the proposed EH PMU architecture with a maximal improvement of $\sim 1.58\times$. It is also shown that increasing V_{Upp} can help reduce C_{cap} for the same amount of Eff_{ov} improvement. Finally, as shown in Fig. 22(b), the V_{Upp} incurred PCE degradation of the converters is pronounced if C_{cap} is too small or large. Specifically, if the capacitor is too small, it can tolerate only a small amount of power mismatch between harvester and load, worsening Eff_{ov} . If the capacitor becomes too large, V_{Cap} remains very close to V_{Upp} because $C_{\text{cap}}(V_{\text{Upp}}^2 - V_{\text{Low}}^2)$ is larger than $E_{\text{cap-active}}$. In this case, large V_{Upp} can hurt PCE_1 and PCE_3 .

At last, it is noteworthy that the model we used above can be extended to general power profiles, by dividing the time window in a more fine-grained way, adding the history effect on the V_{Cap} , and employing iterative solving function of V_{Cap} from power and previous V_{Cap} values. Also, the PCE calculation can be improved as the current PCEs in the model is using an average value calculated at average V_{Cap} , while the actual PCE should be averaged in the energy aspect. Finally, in the above analysis, leakage of the energy-storage capacitor is ignored as we use a ceramic capacitor with little leakage in the experiments. A leakier capacitor can waste a fixed amount of power, degrading end-to-end efficiency. Thus we need to avoid the capacitor whose leakage is in the good fraction of average harvesting and load power.

VI. CONCLUSION

In this paper, we present a triple mode, hybrid storage EH PMU architecture interfacing a PV cell, a 3-V-battery and a 0.45-V load. It consists of three SC dc–dc converters and a digital LDO for load supply voltage regulation. The proposed EH PMU architecture can effectively cope with

the temporal mismatch of harvested and load power, which enabling minimization of battery charging and discharging operations. Based on several test cases that emulate practical harvested power and load power variations, our proposed architecture achieves up to $2.2\times$ better end-to-end efficiency than the conventional dual-mode architecture. We also analyze the tradeoff among capacitor sizing, capacitor voltage range selection, and end-to-end efficiency, providing system-level design guidelines.

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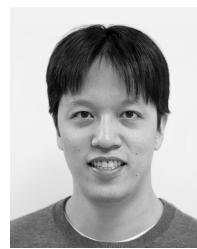
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