Pole-Converging Intrastage Bandwidth Extension Technique for Wideband Amplifiers

Guangyin Feng, *Member, IEEE*, Chirn Chye Boon, *Senior Member, IEEE*, Fanyi Meng, *Member, IEEE*, Xiang Yi, *Member, IEEE*, Kaituo Yang, *Student Member, IEEE*, Chenyang Li, *Student Member, IEEE*, and Howard C. Luong, *Fellow, IEEE*

***Abstract*— To overcome limitations on bandwidth extension in conventional design techniques, a novel pole-converging technique with transformer feedback for intrastage bandwidth extension is proposed and analyzed in this paper. For verification, a three-stage cascode low-noise amplifier (LNA) based on the pole converging and negative drain–source transformer feedback is designed and implemented in a 65-nm CMOS technology. Consuming 27 mW dc power from a 1.8 V supply, the fabricated prototype exhibits peak power gain of 18.5 dB, minimum noise figure of 5.5 dB, 3-dB bandwidth of 30 GHz, and fractional bandwidth of 38.7%. The bandwidth of the three-stage cascode LNA is significantly extended without increasing power consumption and die size.**

***Index Terms*— Broadband amplifiers, bandwidth extension, CMOS amplifiers, frequency compensation, gain boosting, gain flatness, low-noise amplifiers (LNA), millimeter-wave (mm-wave) integrated circuits, pole converging, transformer feedback.**

I. Introduction

THANKS to the aggressive scaling of CMOS technology in recent years, millimeter-wave (mm-wave) CMOS circuits are greatly explored for many applications, such as wireless uncompressed HD-video streaming systems, automatic radars, ultrahigh capacity E-band point-to-point links, and mm-wave/terahertz imaging systems. As the first amplification stage in receiver chains, low-noise amplifier (LNA) plays a critical role in determining signal-to-noise ratio and link budget. Besides power gain and noise figure (NF), operating bandwidth of LNA is also an important specification. In mm-wave imaging receivers, imaging sensitivity and quality are quantified by noise-equivalent temperature difference, which is defined as

$$NETD = T_S\sqrt{\frac{1}{B\tau}+\left(\frac{\Delta G}{G}\right)^2} \tag{1}$$

where T_s is receiver noise temperature, B is RF front-end bandwidth, τ is integration time, G is the overall gain of receiver front-end, and ΔG is the effective value of gain variations [1], [2]. To achieve an excellent thermal resolution, LNA must provide a stable high power gain over a wideband-width. For Frequency Modulated Continuous Wave automatic radars, widebandwidth leads to high range resolution [3]. Furthermore, mm-wave cellular wireless networks with wide-bandwidth have tremendous potential to provide huge capacity and data rates for cellular communications, which may be adopted by next-generation cellular systems in the future [4]. Therefore, wideband LNAs are greatly desired in these systems. Indeed, III-V compound semiconductor technologies have been the desirable platforms for wideband amplifiers with extremely high power gain and low NF at high frequencies compared to its silicon counterparts [5]–[8]. However, CMOS technology demonstrates merits of overwhelmingly low cost and high level of integration, which make them more attractive for the implementation of multiantenna systems with complex digital circuitries [9], [10].

In the literature, distributed architecture and multistage architecture are two widely adopted topologies for wideband amplifiers. However, the former has drawbacks of high power consumption and large chip size; besides, extensive modeling and electromagnetic (EM) simulation are needed to achieve attractive performances [11]–[14]. For multistage amplifiers, bandwidth is limited by intrinsic capacitances of transistors and other parasitic capacitances at the nodes of input, output, and interstages. To extend the bandwidth of multistage amplifiers, different matching networks and peaking techniques are explored to achieve higher bandwidth extension ratio, which is defined as the ratio of the 3-dB bandwidth to that of the reference common-gate (CG) or common-source (CS) amplifier without peaking techniques [15]. Four topologies of interstage matching network are evolved to broaden the bandwidth, namely, L-type [16]–[19], π-type [20], [21], T-type [2], [22], [23], and combination of different types [24], [25], as shown in Fig. 1. By combining L-type and T-type matching networks, the work in [25] demonstrated wide 3-dB bandwidth of 21 GHz with a peak gain of 14.8 dB in CMOS technology. More recently, one LNA in SiGe BiCMOS technology achieved 3-dB bandwidth over 30 GHz using a T-type matching network [2]. Although complex matching networks provide wideband matching, additional insertion loss and chip area are also introduced.

Manuscript received March 10, 2016; revised July 26, 2016 and December 5, 2016; accepted December 10, 2016. Date of publication January 11, 2017; date of current version March 3, 2017. This paper was approved by Associate Editor Ali M. Niknejad. This work was supported by the Singapore Ministry of Education Academic Research Fund Tier 1 under Grant MOE RG86/16.

G. Feng, C. C. Boon, X. Yi, K. Yang, and C. Li are with VIRTUS, IC Design Centre of Excellence, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798 (e-mail: feng0051@e.ntu.edu.sg; yixiang@ntu.edu.sg).

F. Meng is with the School of Physical Electronics, University of Electronic Science and Technology of China, Chengdu 610054, China (e-mail: meng.fanyi@gmail.com).

H. C. Luong is with the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2016.2641459

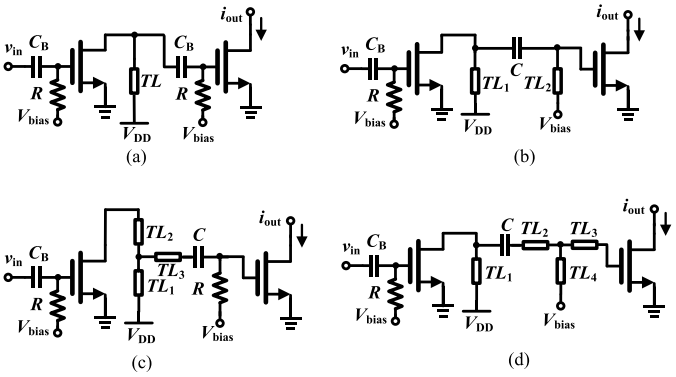


Fig. 1. Interstage matching networks. (a) L-type. (b) π-type. (c) T-type. (d) Combination of L- and T-types.

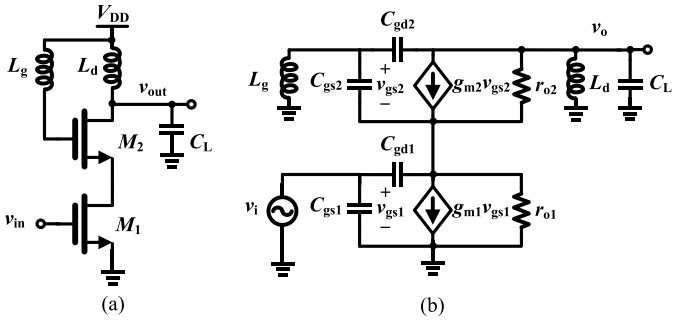


Fig. 2. (a) Schematic of a cascode LNA with gate inductor. (b) Simplified small-signal equivalent circuit.

In this paper, a pole-converging technique with transformer feedback for intrastage bandwidth extension is proposed and verified experimentally. By using the pole-converging and negative drain–source transformer-feedback techniques in the intrastage of amplifiers, the transfer function of each stage exhibits two dominant poles, demonstrating a flat gain-frequency response over an ultrawide bandwidth. For verification, a three-stage cascode LNA with the proposed design techniques is implemented in a 65-nm CMOS technology. In Section II, circuit analyses of pole-converging and negative drain–source transformer-feedback techniques are provided. Section III describes the design methodology with the proposed techniques and the circuit implementation of the prototype. The experimental results are given in Section IV, followed by the conclusion drawn in Section V.

II. Circuit Analysis

A. Proposed Pole-Converging Technique

Fig. 2 shows the schematic and small-signal equivalent circuit of a cascode LNA with an inductor connected to the gate of CG transistor. At mm-wave frequencies and above, accurate modeling becomes critical, and parasitic capacitances and inductances should be taken into consideration, which have substantial effects on the frequency response due to high frequency operation. However, even for the simple circuit shown in Fig. 2, because of many energy storage elements (i.e., inductors and capacitors), equation-based analysis of the gain-frequency response becomes quite challenging, and the analytical solution is too complicated to provide any circuit design insights. Instead, pole–zero analysis of the transfer function is explored using SpectreRF in the Virtuoso Analog Design Environment, through which the effects on frequency response of the LNA due to the changing of the pole positions are graphically analyzed and interpreted.

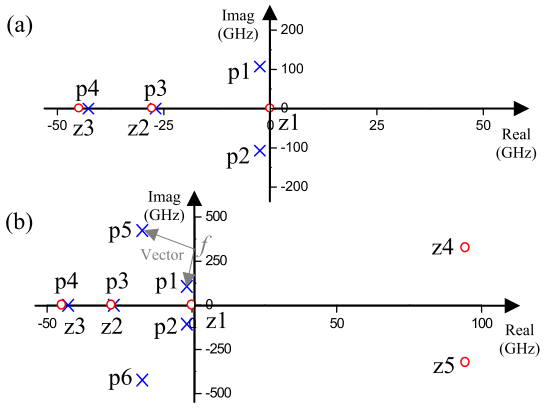


Fig. 3. Poles and zeros of the LNA (a) without gate inductor and (b) with gate inductor ($L_g = 10$ pH).

Fig. 3 indicates the poles and zeros of the cascode LNA with and without gate inductor with poles and zeros far away from the imaginary axis being ignored, which is also applicable for the following pole–zero plots. The main differences between Fig. 3(a) and (b) are the complex conjugate pairs of poles (p_5 and p_6) and zeros (z_4 and z_5) introduced by the gate inductor. The poles close to the imaginary axis dominate the frequency response [26]. Based on the geometric evaluation of the Fourier transform from the pole–zero plot [26], the effects of additional complex poles and zeros on the LNA frequency response are investigated. Because p_3 (p_4) and z_2 (z_3) are quite close, their effects on the frequency response tend to be canceled with each other. At low frequencies, the length of the vector for the pole p_1 is much more sensitive to frequency than that of the pole p_5. Hence, the frequency response is influenced principally by the pole p_1. In particular, the length of that pole vector has a minimum at $f = \mathrm{Im}[p_1]$, and a peak value (peak1) in the magnitude of the frequency response can be expected in the vicinity of that frequency [26]. As the frequency increases, the magnitude of the frequency response exhibits the second peak value (peak2) at $f = \mathrm{Im}[p_5]$, where the pole vector for p_5 reaches its minimum [26]. The effects on frequency response from gate inductor are also verified through ac simulation, as shown in Fig. 4. By pushing the two peak gains, peak1 and peak2, toward each other, i.e., converging the imaginary parts of p_1 and p_5, the bandwidth of the cascode LNA can be extended.

Indeed, the phenomena of *pole converging* can be observed in the pole–zero plot with the increase of L_g, as demonstrated in Fig. 5. As L_g increases, the nondominant pole p_5 is pushed toward to p_1 and becomes dominant one. Although z_4 moves closer to the imaginary axis, the zero z_1 located at the origin still dominates, which does not change with the gate inductor. As p_3 (p_4) and z_2 (z_3) are also not affected by L_g, the frequency response is still dominated by p_1 and p_5. Fig. 6

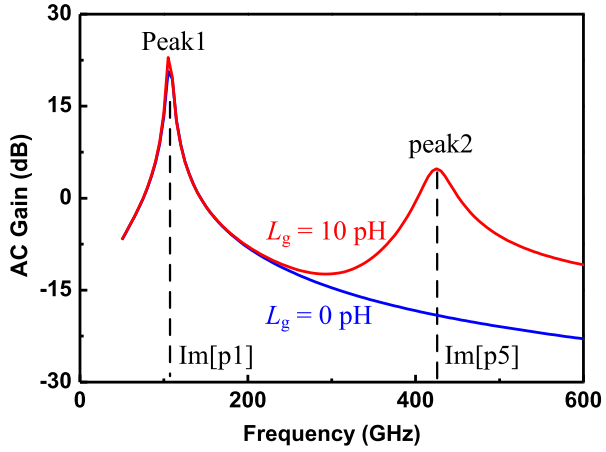


Fig. 4. Gain-frequency response of the LNA with and without gate inductor.

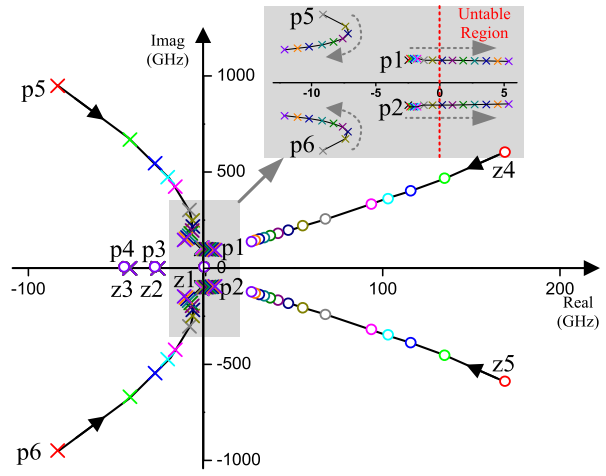


Fig. 5. Locus of poles and zeros as gate inductor varies from 2 to 100 pH, dashed line with arrow shows the moving direction as L_g increases.

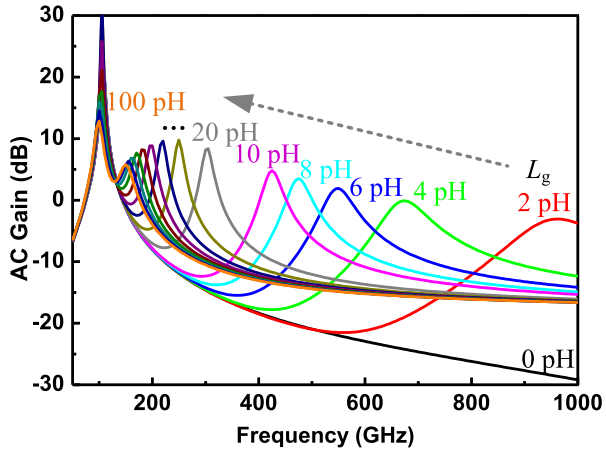


Fig. 6. Gain-frequency response of the cascode LNA as gate inductor varies from 0 to 100 pH.

illustrates the frequency response of the LNA as L_g increases from 0 to 100 pH. As expected, the distance between two peak gains is greatly reduced due to the pole converging between Im[p_1] and Im[p_5].

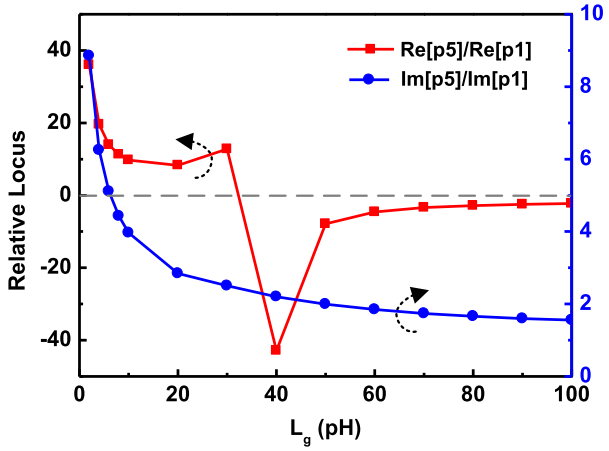
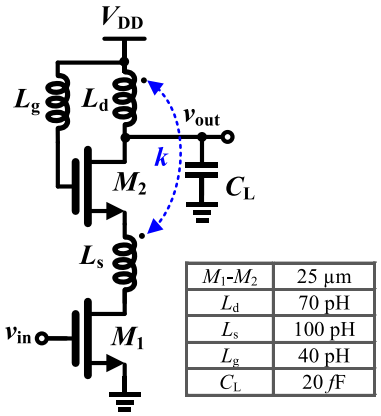


Fig. 7. Relative locus between p_1 and p_5 as gate inductor varies from 2 to 100 pH.



M_1-M_2	25 μm
L_d	70 pH
L_s	100 pH
L_g	40 pH
C_L	20 fF

Fig. 8. Schematic of a cascode LNA with gate inductor and drain–source transformer.

Fig. 7 demonstrates the relative locus between p_1 and p_5 as gate inductor increases. The ratio between Im[p_5] and Im[p_1] reduces from 8.9 to 1.5 as L_g increases from 2 to 100 pH, which results in distance reduction between two peak gains. The ratio between Re[p_5] and Re[p_1] stands for the relative distance to the imaginary axis. As pointed out in [26], it is the poles close to the imaginary axis that dominate the frequency response. When L_g increases from 2 to 20 pH, the ratio between Re[p_5] and Re[p_1] changes from 36 to 9, thus non-dominant pole p_5 turns out to dominate the frequency response together with p_1. In addition, the magnitude of the frequency response is also enhanced due to the increase of L_g. The closer to the imaginary axis results in the smaller minimum value of pole vector, which leads to higher magnitude of the frequency response. However, if large L_g is used, the stability becomes an issue. As shown in Fig. 7 and the zoom-in figure inserted in Fig. 5, p_1 moves into the right-half plane and Re[p_1] changes from negative to positive when L_g larger than 30 pH. Although Im[p_5] and Im[p_1] keep converging, Re[p_5] starts to move away from the imaginary axis slowly, reducing the magnitude of the frequency response, as indicated in Fig. 6. Therefore, attentions must be paid to avoid the unstable operation and gain degradation when designing the gate inductor.

B. Negative Drain–Source Transformer Feedback

As shown in Fig. 6, the gate inductor introduces a gain peaking to extend the bandwidth but with large ripple. Only when the gain at the first dominant pole, p_1, is restrained and that at the second pole, p_5, is enhanced, will the cascode LNA with pole-converging technique achieve a flat gain-frequency response over a widebandwidth. In the literature, transformer feedback is extensively used for the design of wideband amplifiers. Based on different configurations, this technique can achieve various benefits such as neutralization [27], transconductance enhancement [28], wideband matching [17], [29], [30], noise cancellation [29], and bandwidth extension [7], [15]. Nevertheless, negative transformer feedback has an inevitable drawback of gain reducing in almost direct proportion to other benefits achieved, which actually can improve the gain-frequency response of the pole-converging cascode LNA. Therefore, a negative drain–source transformer feedback is introduced through magnetically coupling the drain inductor and source inductor of the CG amplifier in the cascode stage, as shown in Fig. 8. The source inductor L_s tunes out the parasitic gate–source and gate–drain capacitances of the CG and CS transistors, respectively, which leads to higher f_T of cascode structure, improving the performance of cascode amplifiers at mm-wave frequencies [31]. The drain inductor L_d, as a shunt-peaking inductor itself, leads to more initial charging current to the load capacitor of next stage by delaying current flow to the inductor. Besides, the transformer introduces a negative feedback current into L_d through magnetic coupling. Thus, the charging process of the load capacitor becomes much faster, which further extends the 3-dB bandwidth. To investigate the effects on the gain-frequency responses from the negative transformer feedback, further investigations on magnetic coupling coefficient k, drain inductor L_d, and source inductor L_s are taken in the simulation.

Fig. 9 shows the locus of poles and zeros under various coupling coefficients, while Fig. 10 demonstrates the gain-frequency response of the cascode LNA with pole converging and transformer feedback as coupling coefficient varies. Four contributions of the proposed negative transformer feedback can be observed in Figs. 9 and 10. First, p_1 (p_2) moves toward to the left-half plane, which increases the stability of the LNA. Second, p_1 (p_2) moves away from the imaginary axis, and the minimum value of pole vector for p_1 is increased, which reduces the magnitude of the frequency response at the first dominant pole. Third, p_5 (p_6) moves toward the imaginary axis, and the minimum value of pole vector for p_5 is reduced, which increases the magnitude of the frequency response at the second dominant pole. Fourth, Im[p_1] and Im[p_5] do not change much due to the increase of coupling coefficient, therefore, the proposed transformer feedback has much smaller effect on the pole converging compared to the gate inductor. If the magnetic coupling is too strong ($k > 0.8$), p_5 will be pushed to right-half plane, as shown in Fig. 9, leading to stability issue. However, it is quite difficult to achieve high magnetic coupling coefficient at mm-wave frequencies for on-chip transformers. Thus, by designing the drain–source transformer properly, a flat gain-frequency response can be achieved over a widebandwidth.

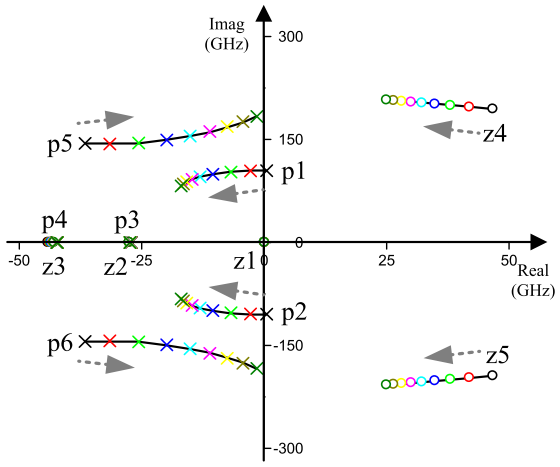


Fig. 9. Locus of poles and zeros as coupling coefficient varies from 0 to 0.8 when $L_g = 40$ pH, dashed line with arrow shows the moving direction as k increases.

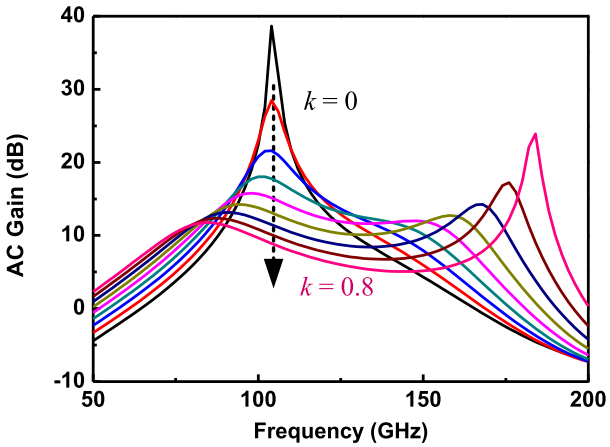


Fig. 10. Gain-frequency response of the cascode LNA with pole converging and transformer feedback as coupling coefficient varies from 0 to 0.8 when $L_g = 40$ pH.

Fig. 11 illustrates the frequency responses with different values of L_d and L_s. As indicated in Fig. 11(b), the first gain peaking attributed to the drain inductor shifts down to lower frequency as L_d increases. Compared to the magnetic coupling coefficient, shown in Fig. 10, L_s has smaller impact on the gain-frequency response, which actually offers a design freedom to obtain optimal k by changing the value of L_s.

C. Wideband Input Matching

At mm-wave frequencies, the parasitic pad capacitance C_{pad} reduces the matching bandwidth of conventional source degeneration matching network because of introducing an additional parallel resonant circuit at the input. Thus, C_{pad} must be designed as part of the matching network. By using a shunt-series feedback, C_{pad} and the input capacitance of the transistor can be simultaneously compensated over a widebandwidth [17]. Fig. 12 shows the input stage of the cascode LNA with shunt-series feedback and the simplified

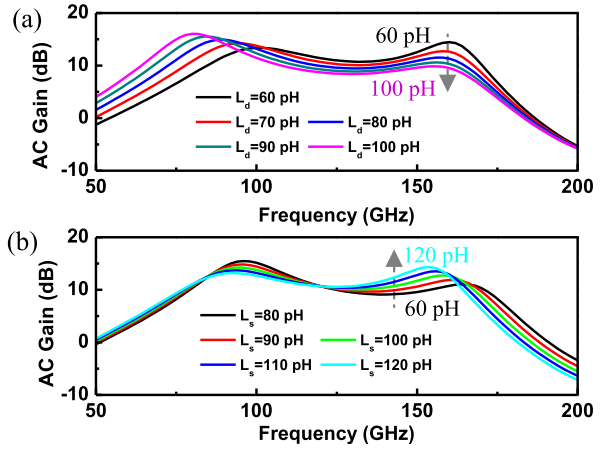


Fig. 11. Gain-frequency response as (a) drain inductor L_d varies (when $L_g = 40$ pH, $L_s = 100$ pH, and $k = 0.5$) and (b) source inductor L_s varies (when $L_g = 40$ pH, $L_d = 70$ pH, and $k = 0.5$).

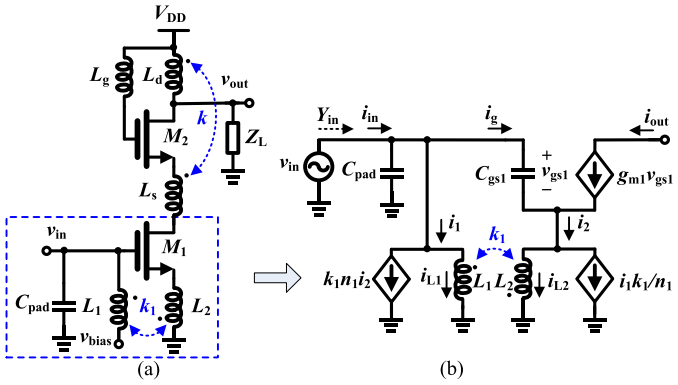


Fig. 12. (a) Input stage of the cascode LNA with shunt-series feedback. (b) Simplified small-signal equivalent circuit of the CS amplifier.

small-signal equivalent circuit of the CS amplifier. Based on the small-signal analysis, the input admittance can be derived as (2)

$$Y_{\text{in}}(s) = sC_{\text{pad}} + \frac{1}{sL_1} + \frac{\frac{k_1}{n_1}\left(1+\frac{k_1}{n_1}\right)g_{m1} + \left(1+\frac{k_1}{n_1}\right)^2 sC_{gs1}}{1+\left(1-k_1^2\right)sL_2g_{m1} + \left(1-k_1^2\right)s^2L_2C_{gs1}}$$
$$\approx \frac{k_1}{n_1}\left(1+\frac{k_1}{n_1}\right)g_{m1} + \frac{1}{sL_1} + s\left[C_{\text{pad}} + \left(1+\frac{k_1}{n_1}\right)^2 C_{gs1}\right] \quad (2)$$

where

$$n_1 = \sqrt{L_2/L_1}. \quad (3)$$

As can be seen in (2), C_{pad} is absorbed into the input capacitance of M_1, forming one parallel resonant circuit with L_1. The simulated effects on input matching from k_1 and L_1 are illustrated in Fig. 13(a) and (b), respectively.

To analyze the impacts on the input matching from the gate inductor and the drain–source transformer, further analysis about the input stage of the three-stage cascode LNA and

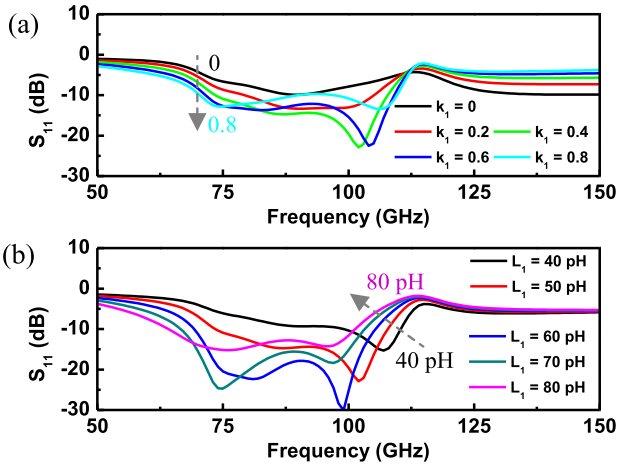


Fig. 13. Simulated input matching as (a) k_1 varies (when $L_1 = 50$ pH, $L_2 = 30$ pH, $L_d = 70$ pH, $L_s = 100$ pH, $L_g = 90$ pH, and $k = 0.5$) and (b) L_1 varies (when $L_2 = 30$ pH, $L_d = 70$ pH, $L_s = 100$ pH, $L_g = 90$ pH, $k = 0.5$, and $k_1 = 0.4$).

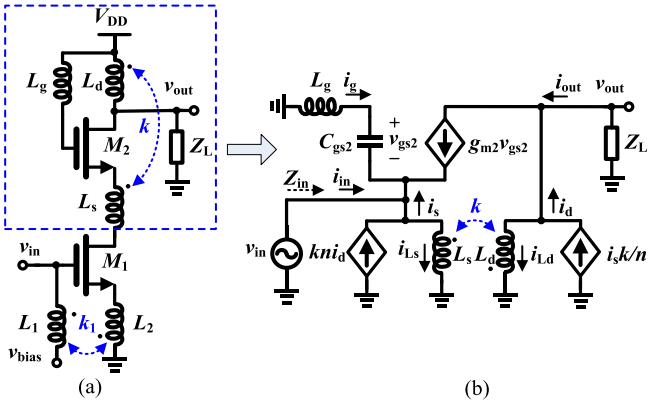


Fig. 14. (a) Input stage of the cascode LNA with shunt-series feedback. (b) Simplified small-signal equivalent circuit of the CG amplifier.

the simplified small-signal equivalent circuit of the CG amplifier is also provided. As shown in Fig. 14, the shunt-series transformer (L_1 and L_2) feedback of M_1 itself provides a wideband input matching [17], but the input matching is also affected by the input impedance of the CG amplifier as the magnetic coupling coefficient varies. For the sake of simplicity, only the input impedance of the CG amplifier is theoretically analyzed. Based on the small-signal equivalent circuit shown in Fig. 14(b), the input impedance of the CG amplifier is derived as (4)

$$Z_{\text{in}}(s) = \left[\beta g_{m2} + \beta sC_{gs2} + \frac{1}{sL_s} + \frac{\beta kn}{1-k^2}\cdot\frac{g_{m2}Z_L}{(sL_d+Z_L)}\right]^{-1} \quad (4)$$

where

$$\beta = \frac{1}{1+s^2L_gC_{gs2}} \quad (5)$$

$$n = \sqrt{L_d/L_s} \quad (6)$$

where β is G_m-boosting coefficient, n is the turn ratio of the drain–source transformer, and Z_L is the load impedance

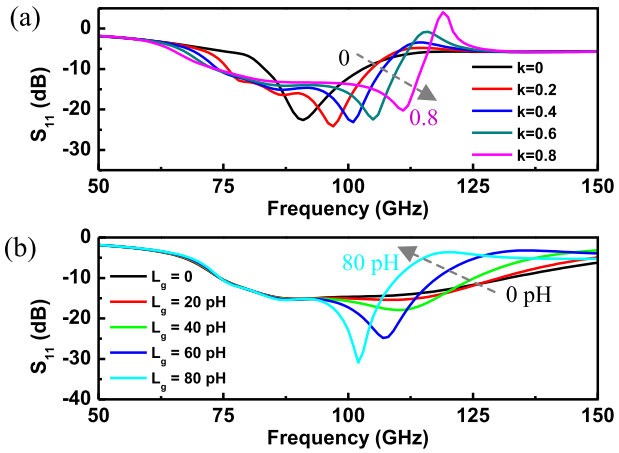


Fig. 15. Simulated input matching as (a) magnetic coupling coefficient k varies (when $L_d = 70$ pH, $L_s = 100$ pH, and $L_g = 90$ pH) and (b) gate inductor L_g varies (when $L_d = 70$ pH, $L_s = 100$ pH, and $k = 0.4$).

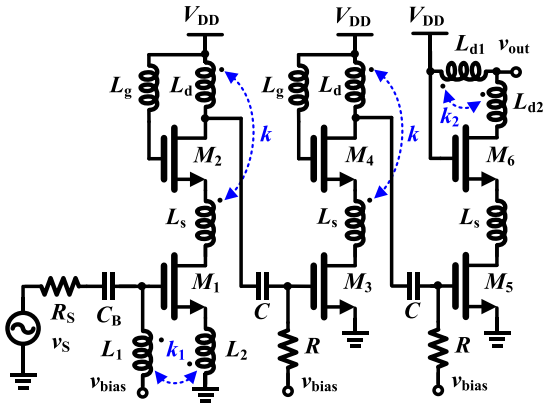


Fig. 16. Schematic of the three-stage LNA with pole converging and drain–source transformer feedback.

including the parasitic inductance of interconnections and the load capacitor from the next stage. As can be seen in (4), the magnetic coupling introduces additional zeros by the fourth term, thus the input impedance bandwidth is enlarged. However, when k changes to zero, the input impedance turns out to be the following equation, thus the bandwidth is reduced:

$$Z'_{\text{in}}(s) = \left[\beta g_{m2} + \beta s C_{gs2} + \frac{1}{sL_s}\right]^{-1}. \tag{7}$$

As illustrated in Fig. 15(a), with the increasing of k, the matching bandwidth becomes much better than that of the amplifier without magnetic coupling. However, if the magnetic coupling becomes too strong, the negative transformer feedback may make the amplifier oscillate at the second pole, as indicated in Fig. 9. Therefore, cares should be taken when using this transformer feedback to avoid unstable operation.

Further to the magnetic coupling coefficient, the G_m-boosting coefficient β also exhibits great effects on the input matching. Note that the gate inductor boosts not only the effective transconductance of M_2 but also the effective gate–source capacitance. Due to the boosted effective gate–source capacitance, the charging process becomes much slower. Thus, the input matching bandwidth is reduced, as shown in Fig. 15(b). In brief, gate inductor enhances the power gain but reduces the input matching bandwidth; nevertheless, the bandwidth is compensated by the drain–source transformer to some extent.

III. Wideband Low-Noise Amplifier Design

A. Design Methodology

The proposed pole-converging intrastage bandwidth extension technique is adopted to extend the bandwidth of amplifiers in cascode topology. Compared to CG and CS amplifiers, cascode amplifiers provide better reverse isolation, higher power gain, and simultaneous noise and power matching over a wideband bandwidth. A design methodology has been developed for the implementation of a CMOS cascode LNA with pole-converging and negative drain–source transformer-feedback techniques shown in Fig. 12(a).

Step 1: Choose the minimum length to maximize power gain and set the bias to the optimum NF_{MIN} current density (J_{OPT}) to minimize transistor noise. The J_{OPT} is about 0.15 mA/μm, which is independent of CMOS technology node [31].

Step 2: Choose the optimal W_f to minimize NF_{MIN}. For 65/90-nm CMOS, W_f is 0.7–1.5 μm [32].

Step 3: Choose the number of fingers (N_f) with respect to the specification of current consumption.

Step 4: Find the optimal value of L_s for the cascode by plotting the f_T of the cascode versus L_s through simulation under the condition of no drain–source coupling ($k = 0$). Note that the value of L_s scales with N_f^{-1}.

Step 5: Based on (2), estimate the value of L_1 assuming that $k_1 = 0.5$ and $n_1 = 1$.

Step 6: Find the optimal value of L_2 by plotting the S_{11} of the cascode versus L_2 through simulation and optimize the value of L_1.

Step 7: Design the shunt-series transformer with the optimized L_1 and L_2.

Step 8: Find the optimal value of L_d to maximize the power gain at frequencies of interest under the condition of no drain–source coupling ($k = 0$).

Step 9: Design the drain–source transformer with maximum coupling coefficient based on the values of L_s and L_d achieved in Steps 4 and 8, respectively.

Step 10: Add the gate inductor L_g to boost the power gain and converge two dominant poles in the transfer function. Optimize the value of L_g to achieve a flat gain response over a widebandwidth through simulation.

Step 11: Return to Steps 6 and 7 to optimize the shunt-series transformer to improve the input matching with the consideration of effects from Steps 9 and 10.

Step 12: Optimize the biasing voltage, and make a tradeoff between minimizing the NF and maximizing the power gain.

Step 13: After completing the layout and parasitic parameters extraction, further optimize the shunt-series transformer, drain–source transformer, and gate inductor.

Following this design methodology, a wideband amplifier with a flat gain-frequency response can be achieved.

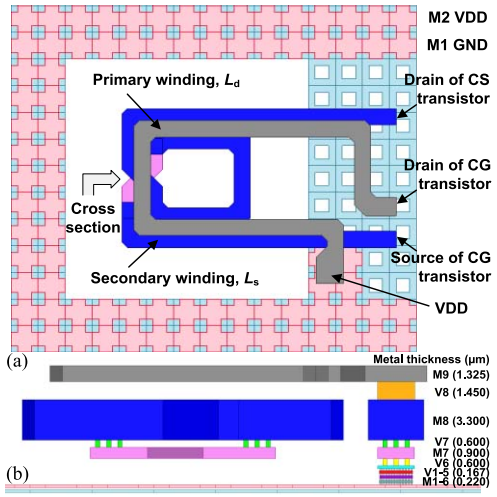


Fig. 17. Layout of the implemented drain–source transformer. (a) Top view (mesh reference [33], [34]). (b) Cross-section view.

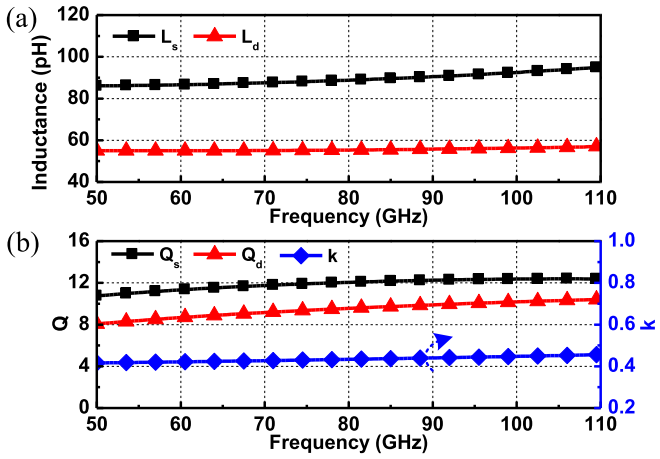


Fig. 18. EM simulation results of the drain–source transformer. (a) Inductances. (b) Quality factors and magnetic coupling coefficient.

B. Circuit Implementation

A three-stage cascode LNA with the proposed pole converging and negative drain–source transformer feedback has been designed in a 65-nm CMOS technology, as shown in Fig. 16. All the transistors have a finger width of 1 μm with the minimum gate length, which results in a good compromise between the gate-resistance reducing and f_T degradation due to the gate-bulk capacitance. The input stage adopts shunt-series feedback to provide wideband input matching and the last stage with asymmetric T-coil peaking works as a wideband output buffer. The parasitic capacitances of testing pads are designed as part of the input and output matching networks. The pole-converging and negative drain–source transformer-feedback techniques for intrastage bandwidth extension are implemented in the first two stages, and L-type interstage matching network is adopted. The drain–source transformer is implemented in a stacked topology for a high magnetic coupling coefficient and a small footprint. As shown in Fig. 17, top two metals with thickness of 1.325 and 3.3 μm are stacked for the primary and secondary windings, respectively. Fig. 18 shows the EM simulation results of the effective inductances and quality factors for the primary and secondary windings of the drain–source transformer. L_d and L_s are 55 and 88 pH, respectively, and the quality factors are above nine with a coupling coefficient of 0.41 at 80 GHz. The top thick metal has been used to implement the gate inductors and interconnections in order to reduce the loss. All inductors, transformers, and testing pads are custom designed with interconnections and simulated in the 3-D EM simulator ANSYS High-Frequency Structure Simulator. Table I lists the optimized parameters of circuit elements in the three-stage cascode LNA.

TABLE I
DESIGN PARAMETERS OF THE THREE-STAGE CASCODE LNA

@80GHz	L_1	L_2	L_3	L_g	L_s	L_d	L_{d1}	L_{d2}
Ind. (pH)	45	27	89	71	88	55	39	63
Q	10.3	13.7	12.1	13.3	15.1	9.6	12.6	13.2
	k	k_1	k_2	R	C	M_1-M_6	V_{DD}	V_{bias}
	0.43	0.41	0.31	18 kΩ	176 fF	25 μm	1.8 V	0.8 V

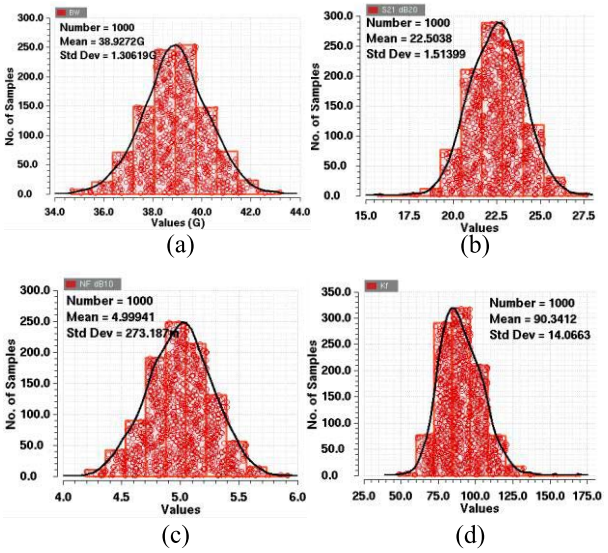


Fig. 19. Monte Carlo simulation of the proposed LNA. (a) 3-dB bandwidth. (b) $|S_{21}|$ at 80 GHz. (c) NF at 80 GHz. (d) K factor at 80 GHz.

Postlayout simulation of the proposed three-stage LNA provides a 3-dB bandwidth of 38 GHz with a peak gain of 22 dB at 1.8 V. Monte Carlo simulation with consideration of mismatch and process variations have also been performed to verify the robustness of the proposed design technique. Fig. 19 shows the Monte Carlo simulation results of 1000 runs of the proposed LNA at nominal corner. The 3-dB bandwidth exhibits a mean value of 38.9 GHz with a standard deviation of 1.3 GHz. The mean value and standard deviation of $|S_{21}|$ at 80 GHz are 22.5 and 1.5 dB, respectively, while those values of NF are 5.0 and 0.27 dB, respectively. Stability across process variations is also investigated. The mean value and standard deviation of stability factor are 90.3 and 14.1, respectively.

IV. EXPERIMENTAL RESULTS

The proposed broadband LNA was fabricated using GLOBALFOUNDRIES 65-nm CMOS technology. Fig. 20 shows the die micrograph of the broadband LNA.

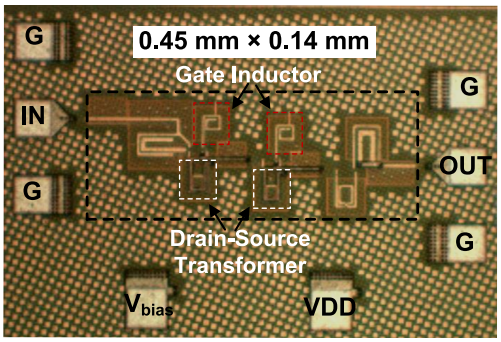


Fig. 20. Die micrograph of the ultrawideband LNA.

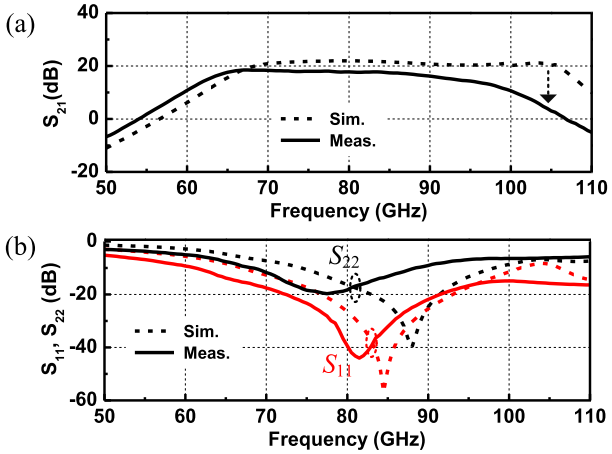


Fig. 21. Simulated and measured S-parameters in high-gain mode.

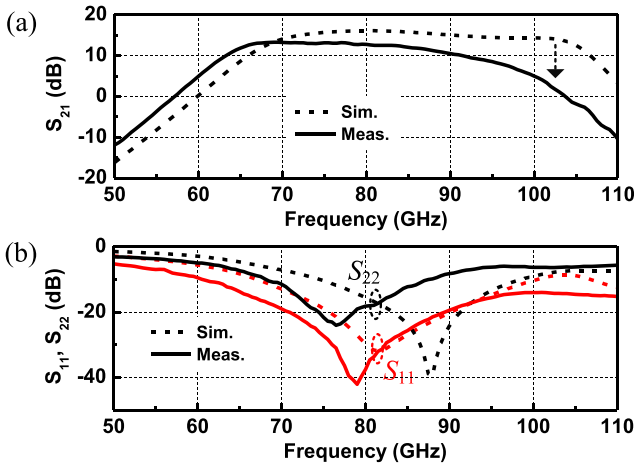


Fig. 22. Simulated and measured S-parameters in low-power mode.

This amplifier presents a core circuit size of only 0.06 mm^2 and occupies a silicon area of 0.24 mm^2 including all the pads. The LNA draws 15.2 mA from a 1.8 V supply (hereinafter, "high-gain mode"), while it has a power consumption of 12 mW under the nominal supply voltage of 1.2 V (hereinafter, "low-power mode").

The LNA was measured through on-wafer testing by using Cascade Microtech Elite 300 probe station and Agilent N5247A PNA-X microwave network analyzer with N5256A

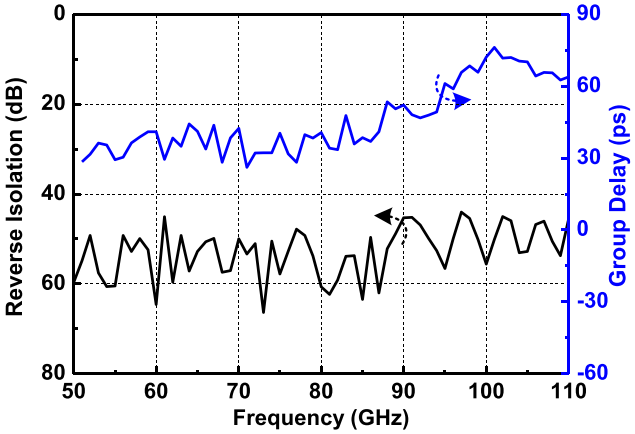


Fig. 23. Measured reverse isolation and group delay in high-gain mode.

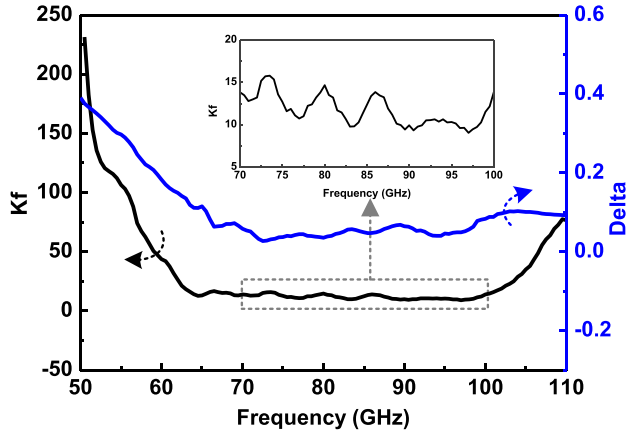


Fig. 24. Measured stability factors K and Δ in high-gain mode.

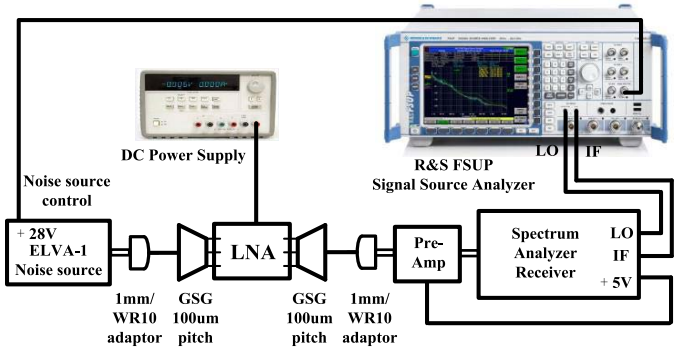


Fig. 25. NF measurement setup.

mm-wave head controller. The measured S-parameters of high-gain mode are plotted in Fig. 21. The prototype achieves a 3-dB bandwidth from 62.5 to 92.5 GHz with a peak gain of 18.5 dB at 68 GHz. The input return loss is better than 10 dB from 60.5 GHz to beyond 110 GHz, while the output return loss is better than 6 dB within the entire 3-dB bandwidth. When there is a constraint on the power consumption, the proposed LNA can provide a peak power gain of 13.3 dB at 69 GHz with a 3-dB bandwidth from 63.5 to 91 GHz in the low-power mode, as depicted in Fig. 22. Wideband input and output matching are also obtained, $|S_{11}| < -12.1$ dB and $|S_{22}| < -6.5$ dB in the 3-dB bandwidth. Compared to

TABLE II
PERFORMANCE SUMMARY AND COMPARISON TO STATE-OF-THE-ART WIDEBAND mm-WAVE LNAS

Reference	Technology	Topology	Gain (dB)	BW† (GHz)	NF (dB)	Power (mW)	V_{DD} (V)	Size (mm^2)	FBW(1) (%)	FoM
[5] JSSC′10	70-nm GaAs mHEMT	4-stage CS	25	40* (70-110)	2.5-2.7	40	1.3	6.00	44.4	20.63-22.85
[7] TMTT′15	0.10-μm GaAs pHEMT	3-stage CS	23	28 (11-39)	2.1-3.0	80	2.0	1.70	112	4.97-7.95
[36] MWCL′10	0.18-μm SiGe	2-stage cascode	14.5	14.5 (69-83.5)	6.9-8.0	37	3.3	0.41	19.0	0.39-0.53
[37] JSSC′11	0.18-μm SiGe	5-stage CE	19	19# (70-89)	8.0-12#	63	1.8	1.00	23.9	0.18-0.51
[2] JSSC′13	0.13-μm SiGe	2-stage cascode	22.5	30 (47-77)	6.0-7.2#	52	2.5	0.52	48.4	1.81-2.58
			25	70# (70-140)	6.2-9.0#	54	2.5	0.33	66.7	3.32-7.27
[11] JSSC′07	0.18-μm CMOS	Distributed	20	39.4 (DC-39.4)	8.0-9.4	250	2.8	2.24	200	0.20-0.30
[12] TMTT′13	0.18-μm CMOS	Distributed	24	33 (1.5-34.5)	6.5-7.5	238	2.8	0.83	183.3	0.48-0.63
[13] TMTT′12	65-nm CMOS	Distributed	22	65 (DC-65)	6.9-7.9	97	1.3	0.93	200	1.63-2.16
[1] MWCL′16	65-nm CMOS	5-stage cascode	16.7	21.5 (88.5-110)	7.2-9	48.6	1.8	0.29	21.7	0.44-0.71
[21] JSSC′11	65-nm CMOS	3-stage cascode	28	13 (55-68)	5.2-6.0	18	-	-	21.1	6.09-7.85
[17] JSSC′08	65-nm CMOS	3-stage cascode	13.5	20 (72-92)	6.4-9.0#	-	1.5	-	24.4	-
[19] JSSC′10	65-nm CMOS	5-stage cascode	27	13.5# (80.5-94)	6.8-9.0#	36	1.2	-	15.5	1.21-2.22
[30] ISSC′15	65-nm CMOS	2-stage cascode	13.1	15 (69-84)	7.0-7.2#	24	1.5	0.17	19.6	0.66-0.70
[38] TMTT′12	45-nm CMOS	3-stage CS	10.7	18 (89-107)	6.0-11	52	1.4	0.32	18.4	0.10-0.40
[39] TMTT′15	28-nm CMOS	2-stage cascode	13.8	18 (55-73)	4.0-5.8	24	2.0	0.38	28.1	1.31-2.43
[40] ISSCC′09	65-nm CMOS	4-stage CS	14.8	21 (82-103)	7.5-9.0#	86	1.2	0.33	22.7	0.19-0.29
[41] JSSC′11	65-nm CMOS	3-stage cascode	15	12 (81-93)	7.0-10#	42	1.2	-	13.8	0.18-0.40
This Work	**65-nm CMOS**	**3-stage cascode**	**13.3**	**27.5 (63.5-91)**	**6.4-8.5**	**12**	**1.2**	**0.24**	**35.6**	**1.73-3.12**
			18.5	**30 (62.5-92.5)**	**5.5-7.9**	**27**	**1.8**		**38.7**	**1.78-3.62**

† 3-dB bandwidth; # estimated value from figures;

(1) $\text{FBW} = \dfrac{BW}{f_c}$, where f_c is the center frequency of the 3-dB bandwidth.

simulated results, the measured 3-dB bandwidth reduces by ∼8 GHz mainly due to the degradation of magnetic coupling coefficient of the drain–source transformer (as illustrated in Fig. 10). Such degradation is caused by randomized dummy metal fills, which are used to satisfy the design rule of minimum metal density. The dummy metal fills introduce additional parasitic capacitance, degrading the inductance and quality factor, which were not fully considered in EM simulation. Fig. 23 shows the measured reverse isolation and group delay of the proposed wideband LNA. Within the entire 3-dB bandwidth, the isolation is better than 45 dB, and the group delay is 40 ps with a variation of ±10 ps. Fig. 24 illustrates the measured Rollett's stability factors K and Δ, which indicates stability of the proposed LNA.

Fig. 25 demonstrates the NF measurement setup. This measurement setup utilizes Y-factor method through turning on and off a noise source, which delivers a uniform level of noise power spectral density with a typical excess noise ratio of 12 dB within the full W-band. The setup consists of a W-band noise source, a W-band preamplifier, a spectrum analyzer receiver (SAR), and an FSUP signal source analyzer. The preamplifier is used to improve the sensitivity level. The SAR down-converts the W-band frequencies and converts the waveguide interface to coaxial interface for the Local Oscillator (LO) and IF connections. The FSUP, equipped with LO/IF option for external mixer, provides a control voltage of 28 V to the noise source and measure the NF of the LNA. To obtain a more accurate NF, a sec-

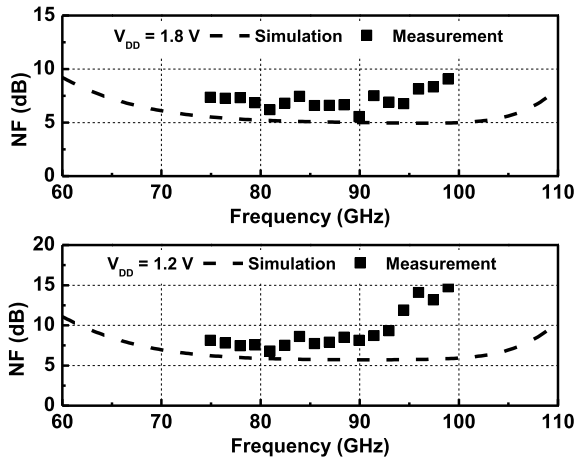


Fig. 26. Simulated and measured NFs in high-gain mode and low-power mode.

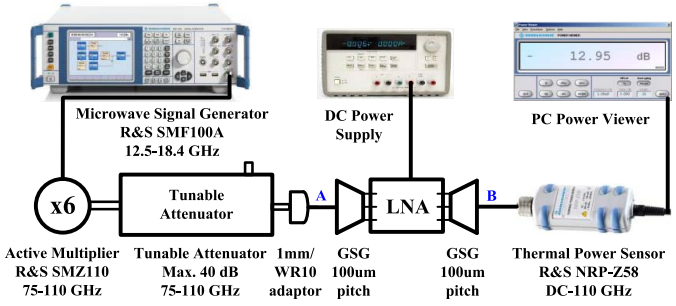


Fig. 27. Large-signal measurement setup.

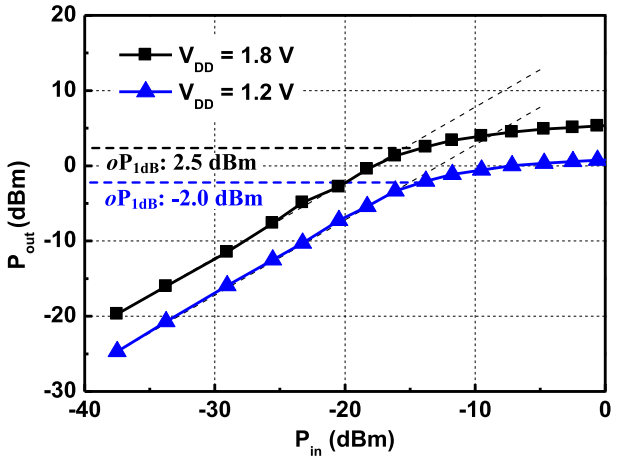


Fig. 28. Measured output power versus input power at 80 GHz.

ond stage calibration was performed to remove the NF of the spectrum analyzer, and the average of 20 measurements was taken. Due to the limitation of measurement setup, NF was measured from 75 to 100 GHz. The average NF of the high-gain mode is 6.8 dB with a minimum value of 5.5 dB at 90 GHz, while the LNA in the low-power mode exhibits an average NF of 7.6 dB with a minimum value of 6.4 dB at 82 GHz, as depicted in Fig. 26.

Fig. 27 demonstrates the large-signal measurement setup. This setup is composed of a microwave signal generator, an active multiplier (×6) with output power of ∼12 dBm, a tunable attenuator with maximum attenuation of 40 dB, and a thermal power sensor. Before testing the LNA, point A was directly connected to point B to measure the input power. By tuning the attenuator, different levels of input power were obtained. Then the output power of the LNA was measured through on-wafer testing. After de-embedding the insertion losses of the GSG pads and cables, large-signal characterizations of the amplifier were achieved, as illustrated in Fig. 28. The proposed amplifier exhibits an output-referred $P_{1\ dB}$ of 2.5 dBm in high-gain mode, while that in low-power mode is −2.0 dBm.

Table II summaries the performance of the proposed broadband LNA and other state-of-the-art LNAs. The bandwidth of proposed LNA is significantly extended by the proposed pole-converging and negative drain–source transformer-feedback techniques without increasing the power consumption and die size. A commonly used figure of merit (FoM) [15] is adopted for comparison in the table, which takes the power gain, 3-dB bandwidth, noise factor, and power consumption into account, defined as

$$\text{FoM} = \frac{Gain[\text{abs.}] \times \text{BW[GHz]}}{(F-1) \times P_{\text{DC}}[\text{mW}]}. \tag{8}$$

V. Conclusion

A pole-converging technique for intrastage bandwidth extension has been proposed and analyzed in this paper, and a design methodology for wideband amplifiers based on this technique was developed. By employing gate inductors and negative drain–source transformers in the intrastages, the transfer function of each stage exhibits two dominant poles, achieving a flat gain-frequency response over an ultrawide bandwidth. A three-stage cascode LNA based on the pole-converging technique is designed and implemented in a 65-nm CMOS technology. Since the gain is boosted in a passive way and stacked transformers are adopted, the 3-dB bandwidth is greatly extended without increasing the power consumption and the chip area. The prototype achieves peak power gain of 18.5 dB, minimum NF of 5.5 dB, and 3-dB bandwidth of 30 GHz with low power consumption of 27 mW. This technique can be combined with other interstage bandwidth enhancement techniques to achieve greater improvement. Furthermore, although this paper is about mm-wave LNA design, the design methodology can be extended to wideband amplifier design at lower frequencies. In addition, an amplifier with variable gain or bandwidth can be achieved, if the gate inductor is switchable or the magnetic coupling coefficient of the drain–source transformer is reconfigurable.

Acknowledgment

The authors thank Prof. S. Liter and L.-T. G. Eng in VIRTUS, Nanyang Technological University, for supporting the chip measurement.

References

[1] G. Feng, C. C. Boon, F. Meng, X. Yi, and C. Li, "An 88.5–110 GHz CMOS low-noise amplifier for millimeter-wave imaging applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 2, pp. 134–136, Feb. 2016.

[2] G. Liu and H. Schumacher, "Broadband millimeter-wave LNAs (47–77 GHz and 70–140 GHz) using a T-type matching topology," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2022–2029, Sep. 2013.
[3] Y.-A. Li, M.-H. Hung, S.-J. Huang, and J. Lee, "A fully integrated 77GHz FMCW radar system in 65nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 216–217.
[4] S. Rangan, T. S. Rappaport, and E. Erkip, "Millimeter-wave cellular wireless networks: Potentials and challenges," *Proc. IEEE*, vol. 102, no. 3, pp. 366–385, Mar. 2014.
[5] W. Ciccognani, E. Limiti, P. E. Longhi, and M. Renvoise, "MMIC LNAs for radioastronomy applications using advanced industrial 70 nm metamorphic technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 2008–2015, Oct. 2010.
[6] G. Moschetti *et al.*, "A 183 GHz metamorphic HEMT low-noise amplifier with 3.5 dB noise figure," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 9, pp. 618–620, Sep. 2015.
[7] G. Nikandish and A. Medi, "Transformer-feedback interstage bandwidth enhancement for MMIC multistage amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 441–448, Feb. 2015.
[8] P. Smith *et al.*, "A 50nm MHEMT millimeter-wave MMIC LNA with wideband noise and gain performance," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2014, pp. 1–4.
[9] A. Tang, Q. J. Gu, and M.-C. F. Chang, "CMOS receivers for active and passive mm-wave imaging," *IEEE Commun. Mag.*, vol. 49, no. 10, pp. 190–198, Oct. 2011.
[10] G. Feng, C. C. Boon, F. Meng, and X. Yi, "A 100-GHz 0.21-K NETD 0.9-mW/pixel charge-accumulation super-regenerative receiver in 65-nm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 7, pp. 531–533, Jul. 2016.
[11] J.-C. Chien and L.-H. Lu, "40-Gb/s high-gain distributed amplifiers with cascaded gain stages in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2715–2725, Dec. 2007.
[12] J.-C. Kao, P. Chen, P.-C. Huang, and H. Wang, "A novel distributed amplifier with high gain, low noise, and high output power in 0.18-μm CMOS technology," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 4, pp. 1533–1542, Apr. 2013.
[13] A. Jahanian and P. Heydari, "A CMOS distributed amplifier with distributed active input balun using GBW and linearity enhancing techniques," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 5, pp. 1331–1341, May 2012.
[14] T.-Y. Huang, Y.-H. Lin, J.-H. Cheng, J.-C. Kao, T.-W. Huang, and H. Wang, "A high-gain low-noise distributed amplifier with low DC power in 0.18-μm CMOS for vital sign detection radar," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2015, pp. 1–3.
[15] S. Shekhar, J. S. Walling, and D. Allstot, "Bandwidth extension techniques for CMOS amplifiers," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp. 2424–2439, Nov. 2006.
[16] B. Cetinoneri, Y. A. Atesal, A. Fung, and G. M. Rebeiz, "*W*-band amplifiers with 6-dB noise figure and milliwatt-level 170-200-GHz doublers in 45-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 3, pp. 692–701, Mar. 2012.
[17] M. Khanpour, K. W. Tang, P. Garcia, and S. P. Voinigescu, "A wideband W-band receiver front-end in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 8, pp. 1717–1730, Aug. 2008.
[18] R. Sananes and E. Socher, "52–75 GHz wideband low-noise amplifier in 90 nm CMOS technology," *Electron. Lett.*, vol. 48, no. 2, pp. 71–72, Jan. 2012.
[19] A. Tomkins, P. Garcia, and S. P. Voinigescu, "A passive W-band imaging receiver in 65-nm bulk CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 1981–1991, Oct. 2010.
[20] D. Fritsche, G. Tretter, C. Carta, and F. Ellinger, "Millimeter-wave low-noise amplifier design in 28-nm low-power digital CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 6, pp. 1910–1922, Jun. 2015.
[21] F. Vecchi *et al.*, "A wideband receiver for multi-Gbit/s communications in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 551–561, Mar. 2011.
[22] A. Y.-K. Chen, Y. Baeyens, Y.-K. Chen, and J. Lin, "A low-power linear SiGe BiCMOS low-noise amplifier for millimeter-wave active imaging," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 2, pp. 103–105, Feb. 2010.
[23] D.-R. Lu, Y.-C. Hsu, J.-C. Kao, J.-J. Kuo, D.-C. Niu, and K.-Y. Lin, "A 75.5-to-120.5-GHz, high-gain CMOS low-noise amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2012, pp. 1–3.
[24] L. Gilreath, V. Jain, and P. Heydari, "Design and analysis of a W-band SiGe direct-detection-based passive imaging receiver," *IEEE J. Solid-State Circuits*, vol. 46, no. 10, pp. 2240–2252, Oct. 2011.
[25] D. Sandstrom, M. Varonen, M. Karkkainen, and K. Halonen, "W-band CMOS amplifiers achieving +10dBm saturated output power and 7.5dB NF," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 486–487 and 487a.
[26] A. V. Oppenheim, A. S. Willsky, and S. H. Nawab, *Signals and Systems*. Englewood Cliffs, NJ, USA: Prentice-Hall, 1997, pp. 674–683.
[27] D. J. Cassan and J. R. Long, "A 1-V transformer-feedback low-noise amplifier for 5-GHz wireless LAN in 0.18μm CMOS," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 427–435, Mar. 2003.
[28] X. Li, S. Shekhar, and D. J. Allstot, "G_m-boosted common-gate LNA and differential colpitts VCO/QVCO in 0.18μm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2609–2619, Dec. 2005.
[29] H. F. Leung and H. C. Luong, "A 1.2-6.6GHz LNA using transformer feedback for wideband input matching and noise cancellation in 0.13μm CMOS," in *Proc. IEEE RF Integr. Circuits Symp.*, Jun. 2012, pp. 17–20.
[30] D. Pepe and D. Zito, "72 GHz CMOS LNA with transformer-based input integrated matching," in *Proc. 26th Irish Signals Syst. Conf. (ISSC)*, Jun. 2015, pp. 1–5.
[31] T. Yao *et al.*, "Algorithmic design of CMOS LNAs and PAs for 60-GHz radio," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1044–1057, May 2007.
[32] S. Voinigescu, *High-Frequency Integrated Circuits*. Cambridge, MA, USA: Cambridge Univ. Press, 2013, pp. 374–551.
[33] S. T. Nicolson, P. Chevalier, B. Sautreuil, and S. P. Voinigescu, "Single-chip W-band SiGe HBT transceivers and receivers for Doppler radar and millimeter-wave imaging," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2206–2217, Oct. 2008.
[34] A. M. Mangan, S. P. Voinigescu, M.-T. Yang, and M. Tazlauanu, "De-embedding transmission line measurements for accurate modeling of IC designs," *IEEE Trans. Electron Devices*, vol. 53, no. 2, pp. 235–241, Feb. 2006.
[35] L. Zhou, C.-C. Wang, Z. Chen, and P. Heydari, "A W-band CMOS receiver chipset for millimeter-wave radiometer systems," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 378–391, Feb. 2011.

Guangyin Feng (S'12–M'16) received the B.Eng. degree from Northeastern University, Shenyang, China, in 2010, and the Ph.D. degree from Nanyang Technological University, Singapore, in 2016.

Since 2016, he has been a Research Fellow with Nanyang Technological University. His research interests include millimeter-wave/terahertz integrated circuits and systems for wireless communications, radars, and bioapplications.

Chirn Chye Boon (M'09–SM'10) received the B.E. (Hons.) and Ph.D. degrees in electrical engineering from Nanyang Technological University (NTU), Singapore, in 2000 and 2004, respectively.

He was with Advanced RFIC, NTU, where he was a Senior Engineer. Since 2005, he has been with NTU, where he is currently an Associate Professor. He is involved in radio frequency & mm-wave circuits and systems design for biomedical and communications applications. He has conceptualized, designed, and silicon-verified 80 circuits/chips for biomedical and communication applications. Since 2010, he has been the Program Director of RF and mm-wave research in the S$50 million research center of excellence, VIRTUS, NTU. He is the Principal Investigator for Industry/Government Research Grants of S$8,646,178.22. He has authored over 100 refereed publications in the fields of RF and mm-wave. He has authored the book: *Design of CMOS RF Integrated Circuits and Systems* (World Scientific Publishing).

Dr. Boon was a recipient of the year-2 Teaching Excellence Award and the Commendation Award for Excellent Teaching Performance from the School of Electrical and Electronic Engineering, NTU. He serves as a Committee Member for various conferences. He is an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS and Golden Reviewer for the IEEE ELECTRON DEVICES LETTERS.

Fanyi Meng (S'11–M'16) received the B.Eng. and Ph.D. degrees in electrical and electronic engineering from Nanyang Technological University (NTU), Singapore, in 2011 and 2016, respectively.

He joined NTU as a Research Fellow in 2015, and has served as the Co-Principal Investigator for several research projects. He is currently an Associate Professor with the University of Electronic Science and Technology of China, Chengdu, China. His current research interests include radio frequency, millimeter-wave, and terahertz integrated circuits and systems.

Dr. Meng was a recipient of the IEEE Solid-State Circuits Society Student Travel Grant Award in 2015. He serves as a reviewer and Technical Program Committee Member for several IEEE journals and conferences.

Xiang Yi (S'11–M'13) received the Ph.D. degree from Nanyang Technological University (NTU), Singapore, in 2014.

He is currently a Research Fellow with NTU. His current research interests include RF and millimeter-wave frequency synthesizers and transceiver systems.

Dr. Yi was a recipient of the International Solid-State Circuits Conference Silkroad Award and the Solid-State Circuits Society Travel Grant Award in 2013. He is a Technical Reviewer for several IEEE journals.

Kaituo Yang (S'15) received the B.S. and M.S. (Hons.) degrees from the School of Information Science and Technology, University of Science and Technology of China, Hefei, China, in 2011 and 2014, respectively. He is currently pursuing the Ph.D. degree with Nanyang Technological University (NTU), Singapore.

Since 2014, he has been with NTU as a Researcher Associate, involved in designing carrier-aggregation receiver chip for 802.11ax applications. He holds several patents in the field of RF-CMOS design. His current research interests include analog and RF integrated circuits and systems for wireless communications.

Chenyang Li (S'13) received the B.Eng. and M.Eng. degrees in electronic science and technology from the University of Electronic Science and Technology of China, Chengdu, China, in 2009 and 2012, respectively. He is currently pursuing the Ph.D. degree in electrical engineering with Nanyang Technological University, Singapore.

His current research interests include high-linear power amplifier design for Wi-Fi systems.

Howard C. Luong (M'91–SM'02–F'14) received the B.S., M.S., and Ph.D. degrees in electrical engineering and computer sciences from the University of California, Berkeley, CA, USA, in 1988, 1990, and 1994, respectively.

Since 1994, he has been an EEE Faculty Member at the Hong Kong University of Science and Technology, Hong Kong, where he is currently a Professor. He has coauthored three technical books entitled *Design Techniques for Transformer-Based VCOs and Frequency Dividers, Low-Voltage RF CMOS Frequency Synthesizers,* and *Design of Low-Voltage CMOS Switched-Opamp Switched-Capacitor Systems*. His current research interests include RF and analog integrated circuits and systems for wireless and portable applications.

Prof. Luong was an IEEE Solid-State Circuits Society Distinguished Lecturer and an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I (TCAS-I) AND TCAS-II. He currently serves as an Associate Editor of the IEEE RFIC VIRTUAL JOURNAL and a Technical Program Committee Member of the IEEE International Solid-State Circuits Conference.