A Low-Noise Area-Efficient Chopped VCO-Based CTDSM for Sensor Applications in 40-nm CMOS

Chih-Chan Tu, Yu-Kai Wang, and Tsung-Hsien Lin, *Senior Member, IEEE*

***Abstract*— An area-efficient voltage-sensing readout circuit employing chopped voltage-controlled oscillator (VCO)-based continuous-time delta-sigma modulator (CTDSM) is presented in this paper. This VCO-based CTDSM features direct connection to sensors to eliminate pre-amplifier for achieving better hardware efficiency. The VCO is designed as a trans-conductor current-controlled oscillator, which is a fully differential G_m stage cascaded with two CCOs, to provide a high-input impedance to sense the voltage signals from sensors. Analysis shows that the main noise and offset contributor is the G_m stage. This problem is mitigated by employing choppers at critical location within the circuit. The VCO-based CTDSM is implemented in a 40-nm CMOS process. The power consumption is 17 μW under 1.2-V supply. With a 4-mV$_{\mathrm{p}}$ (8-mV$_{\mathrm{pp}}$) input, it achieves 61.85-dB signal-to-noise-and-distortion ratio over a 5-kHz bandwidth and the total harmonic distortion is -70.8 dB. The input-referred noise is 32 nV/$\sqrt{\text{Hz}}$. The chip area is only 0.0145 mm^2.**

***Index Terms*— Analog front end, chopper, sensor, trans-conductor current-controlled oscillator (G_m-CCO), voltage-controlled oscillator (VCO)-based continuous-time delta-sigma modulator (CTDSM).**

I. Introduction

PRECISION sensor readout circuits are required in many applications, such as bio-potential sensing [1], electronic compasses [2] [3], and thermistor bridges [4]. These applications usually have input signal in the range of millivolts, bandwidth ranges from several hertz to kilohertz, and requires microvolt-level resolution. For example, typical design requirements of an electrocardiography signal readout circuit include a 5-mV$_{\mathrm{pp}}$ dynamic range (with the electrode offset removed), input-referred noise less than 100 nV/$\sqrt{\text{Hz}}$, and a signal bandwidth around 150 Hz. As another example, the Hall sensor for the electronic compass presented in [2] outputs a 0.3-mV signal with 25-nV/$\sqrt{\text{Hz}}$ input-referred noise and 85-ms measurement time. Among various applications, accuracy is often the most important design consideration for industrial or automotive applications; while for portable applications or Internet of Things sensors, low-power consumption, compact form factor, and low cost are required.

Conventionally, the precision sensor readout circuit comprises a high-input impedance analog front-end amplifier, and an analog-to-digital converter to digitize the signal. In [5], for high-accuracy applications, a precision current-feedback instrumentation amplifier with discrete-time (DT) delta-sigma modulator successfully achieves a 20-bit resolution and an integral non-linearity of 6 ppm. While high performance is demonstrated, this design is rather complex and occupies large circuit area. For medium accuracy requirement such as bio-potential readout applications, an SAR-analog-to-digital converter (ADC) with an instrumentation amplifier is commonly adopted [1]. In both implementations, the IA and ADC are designed separately as two independent circuits. Intuitively, if the instrumentation amplifier (IA) and ADC can be merged into one single circuit, as conceptually illustrated in Fig. 1, the overall hardware can be considerably reduced. In this topology, the ADC needs to digitize the sensor signal directly at a smaller, non-amplified, input signal dynamic range. Furthermore, it requires the same input-referred noise and linearity performance as that of an IA. It also needs to have a high-input impedance to directly interface with the sensors.

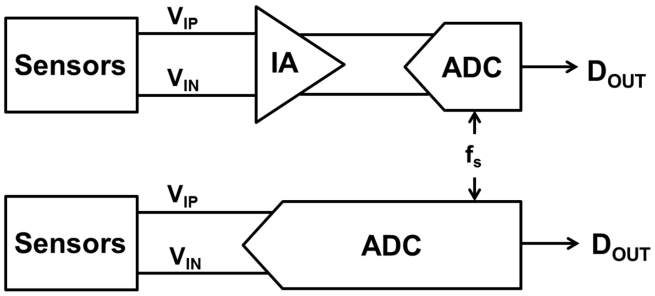

Fig. 1. (Top) Conventional sensor readout approach consisting IA + ADC; (Bottom) Sensor readout circuit directly use the ADC without pre-amplifier.

Considering the design of such an ADC, the continuous-time topology may be preferred over the DT approach, such as SAR-ADC and discrete-time delta-sigma modulator (DTDSM). A DT ADC faces the tradeoff among noise-aliasing issue and other design considerations. To lower the fundamental noise, characterized as input-referred noise power spectral density (PSD), 2kT/Cf_s, both C and f_s should be increased. However, this leads to reduced input impedance, larger chip area, and higher power consumption. In continuous-time approaches, considering the input impedance requirement, the G_m-C continuous-time delta-sigma modulator (CTDSM) is preferred over the active-*RC* CTDSM, as it can provide a high-input impedance. In [6], a G_m-C CTDSM successfully achieves similar performance compared to that of the conventional approach [5]. However, for linearity requirements, a large passive second-order low-pass filter with 200-pF capacitor is added in the feedback path.

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The authors are with the Department of Electrical Engineering, Graduate Institute of Electronics Engineering, National Taiwan University, Taipei 10617, Taiwan (e-mail: d02943008@ntu.edu.tw).

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Moreover, to limit the voltage signal swing inside the CTDSM, the capacitors in the loop filter are also in the order of 200 pF. These large capacitors consume considerable chip area.

To save the circuit area and reduce design complexity, the time-domain voltage-controlled oscillator (VCO)-based sensor readout (or ADC) topology offer an attractive alternative. There are a few advantages of a VCO-based ADC. First, a VCO circuit achieves infinite dc gain without stacking transistors as required in conventional amplifiers. Second, a VCO-based ADC converts a voltage-domain signal to a phase-domain signal, where the phase signal swing is not limited by the supply voltage. This implies that large RC or C/G_m value required in a voltage-mode integrator to optimize the signal swing is no longer a design constraint. Third, VCO-based ADCs are mainly comprised of inverters and digital circuits only, which can potentially benefit from the process scaling.

Various VCO-based circuit architectures have been proposed previously [7]–[11]. For example, a bang–bang phase-locked loop-based Wheatstone interface has been reported in [7] to facilitate voltage-domain sensing. In [8], a VCO-based closed-loop architecture with $\Delta\Sigma$-digital-to-analog converter (DAC) is adopted for current sensors [8]. For voltage-domain sensing, the VCO-based ADC has been used in neural signal readout [9]. Furthermore, in [10], a calibration technique is proposed to improve the signal dynamic range. However, the existing solutions mentioned above did not focus on addressing the flicker noise issue, which is a critical factor that limits the resolution in low-frequency applications. Chopping technique is often adopted to suppress the flicker noise in a continuous-time circuit. In [10], the chopping technique is not applied to the noise-dominating input trans-conductor (G_m) stage due to the input impedance consideration. As a result, the input-referred noise is not well-suppressed. On the other hand, in [11], although the noise of the VCO-based ADC is buffered by a chopped pre-amplifier stage, the overall linearity degrades due to the larger input signal.

In this paper, we proposed a chopped VCO-based sensor readout circuit. It features direct digitization of the input voltage without extra amplification. We show that the G_m stage dominates the noise performance. By applying the chopping technique to the G_m stage, the flicker noise is considerably suppressed. As a result, the proposed VCO-based ADC achieves a good input-referred noise performance comparable to those of prior works.

This paper is organized as follows. In Section II, the proposed architecture is introduced. In Section III, the fundamental structure of the adopted G_m current-controlled oscillator (G_m-CCO) is presented, including its operation principle and noise analysis. The detailed circuit designs are described in Section IV. In Section V, experimental results will be shown. A brief conclusion is given in Section VI.

II. Circuit Architecture

A. Introduction to VCO-Based ADCs

A VCO-based signal condition circuit converts the input voltage/current signal into a phase signal and processes the output phase of a VCO, Φ_{VCO}. The phase information Φ_{VCO} is then extracted by a quantizer and generates digitized output Φ_{VCOQ}. Such signal conditioning approach finds applications in many areas. In [12], an analog filter is implemented using VCO-based integrators, as conceptually illustrated in Fig. 2(a), where the final analog output is obtained by inserting a DAC after Φ_{VCOQ}. If Φ_{VCOQ} is sampled by a clock signal f_s, a VCO-based ADC is attained. It can be implemented in the closed-loop topology [7], [8], [13], as depicted in Fig. 2(b); or the open-loop VCO-based topology [9]–[11], [14], as shown in Fig. 2(c). The closed-loop VCO-based ADC achieves better linearity, with the price of increased design complexity of inserting a feedback network suitable for sensor input. In this paper, our main goal is to design a compact, low-noise sensor readout circuit with a moderate dynamic range requirement. Therefore, the open-loop architecture is chosen for this implementation.

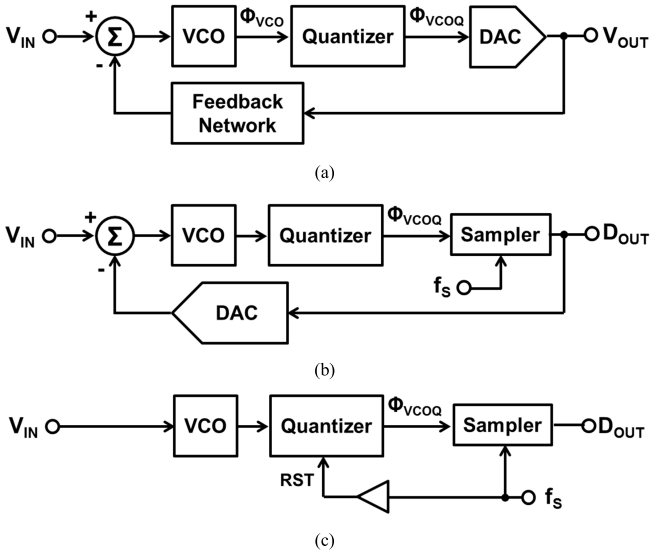


Fig. 2. Application of VCO-based integrators. (a) Analog filter. (b) Closed-loop VCO-based ADC. (c) Open-loop VCO-based ADC.

There are several approaches in implementing the quantizer for an open-loop VCO-based ADC. In [10], the quantizer is implemented with a multi-bit counter. In this prior design, all 29 phases are used. It allows a low sampling frequency while keeping the quantization error lower than the circuit noise. In contrast, in this implementation, for low-complexity low-power consideration, the design is based on a simple three-stage ring VCO. The simplified architecture is shown in Fig. 3, along with illustrations of its operation. As shown in Fig. 3, the output phase is extracted by directly sampling the VCO outputs (V_0, V_1, and V_2); the $1 - z^{-1}$ differentiation operation is performed at the sampled phases. Since no counter is employed, the frequency of the sampling clock (f_S) needs to be at least twice faster than the VCO output frequency, to capture possible transitions between samples. Here, a sampling frequency four times the VCO free-running frequency is chosen to obtain maximum allowable swing.

The signal gain from input voltage to digital output of the open-loop VCO-based ADC can be expressed as

$$\frac{D_{OUT}}{V_{IN}} = \frac{2\pi K_{VCO}}{s}\frac{NP}{2\pi}\frac{s}{f_S} = NP\frac{K_{VCO}}{f_S}. \quad (1)$$

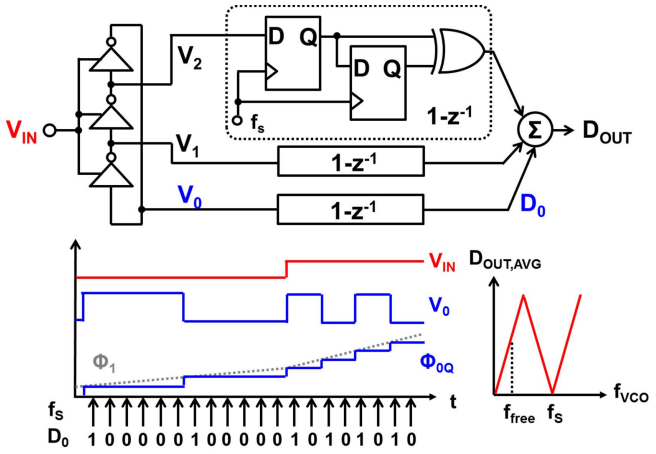


Fig. 3. Operation of multiphase and single-bit open-loop VCO-based ADC.

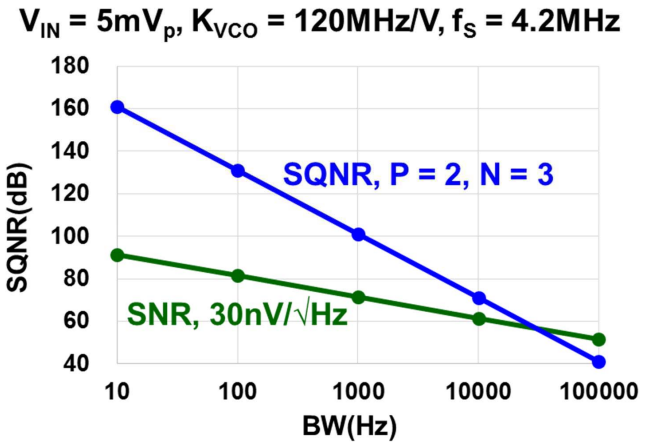


Fig. 4. Calculated SNR and SQNR of the proposed design.

In (1), $2\pi K_{\mathrm{VCO}}/s$ accounts for the VCO operation (N is the total number of VCO phases; $N = 3$ in this paper), $NP/2\pi$ is the inverse of the phase quantization step, where P denotes the rising/falling edges used in the quantizer (both rising and falling edges are used in this design; hence, $P = 2$). The differentiation operation, $1 - \mathrm{z}^{-1}$, is approximated to be s/f_S in low frequencies.

Examining D_{OUT}, the phase-domain single-sideband (SSB) quantization noise PSD over the bandwidth of 0 to $f_s/2$ with a step size of 1 is $1/6f_S$. The overall SSB output quantization noise PSD after differentiation is $S_Q = (2\pi^2 f^2)/(3f_S^3)$, which shows the first-order noise-shaping characteristic. With a desired signal bandwidth f_B, the total output quantization noise is expressed as $(2\pi^2/9)(f_B/f_S)^3$. Assuming an input signal amplitude A, the total input signal power is $\mathrm{A}^2/2$. The signal-to-quantization-noise ratio (SQNR) is calculated to be

$$\mathrm{SQNR}=9A^2\left(\frac{NP}{2\pi}K_{\mathrm{VCO}}\right)^2\frac{f_S}{f_B^3}. \tag{2}$$

The result is similar to that derived in [15] with different approaches.

Fig. 4 shows the calculated SNR under different signal bandwidth, assuming an input-referred noise of 30 nV/$\sqrt{}$Hz, resulting from circuits. The SQNR is estimated from (2), with the following parameters: $K_{\mathrm{VCO}} = 120$ MHz/V, $f_S = 4.2$ MHz, input $(A) = 5$ $\mathrm{mV_p}$. It can be observed that even we choose the simplest quantizer shown in Fig. 3 with the minimum number of phases $N = 3$ and $P = 2$, the overall SNR is limited by the circuit noise, not by the quantization noise, at low frequencies. This suggests that a low-noise VCO design is key to an overall low-noise VCO-based ADC.

B. Topologies of VCO Cells for Sensor Applications

In low-frequency sensor applications, the *LC* VCO is not preferred as it occupies a large chip area if the *LC* tank is to be integrated on chip. Hence, the ring VCO architecture is chosen in this implementation. The frequency of a ring oscillator can be controlled via several approaches, as conceptually illustrated in Fig. 5. The first one is to control the supply voltage [12] or the buck voltage [17] of a ring oscillator, termed as *modulate voltage* in Fig. 5. However, as this approach does not provide high-input impedance in direct sensor readout applications, it's not suitable here. The second one is to modulate the supply current of a ring oscillator. A G_m stage is utilized to convert the input voltage to the controlling current [7]–[11]. Termed as the G_m-CCO structure in this paper, it features high-input impedance and is suitable for voltage sensing applications. The last type relies on varying the loads of the delay cells to control the oscillation frequency. It is inherently more suited for resistive or capacitive sensors. Base on the above discussion, the G_m-CCO structure is chosen to implement the VCO.

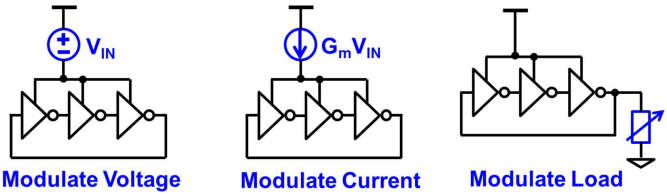


Fig. 5. Different possible realizations of VCO-based ADCs for sensors.

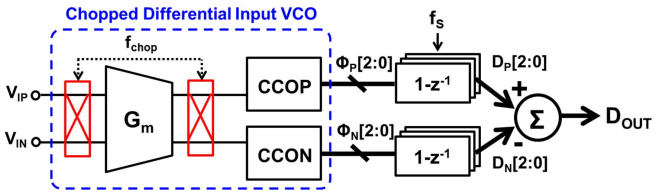


Fig. 6. Proposed circuit architecture with a Chopped G_m-CCO as VCO-based integrator, and a multi-phase single-bit quantizer.

C. Proposed Architecture

The proposed overall readout circuit architecture is shown in Fig. 6. The G_m-CCO-based VCO is realized with a fully differential input G_m stage followed by two CCOs in a pseudodifferential manner. Each phase signal of CCO outputs (Φ_{P} [2:0], Φ_{N} [2:0]) is processed by a 1-bit quantizer.

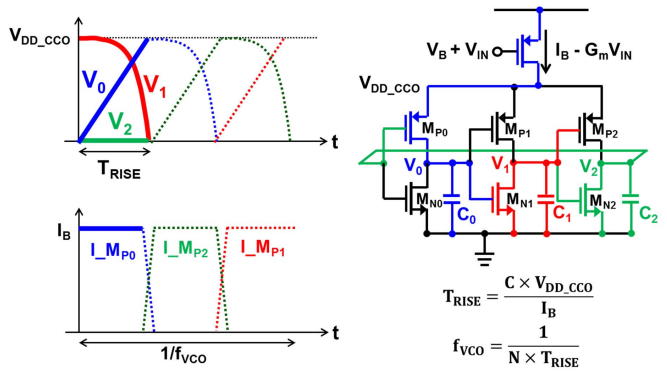


Fig. 7. Behavior operation of the fundamental G_m-CCO structure.

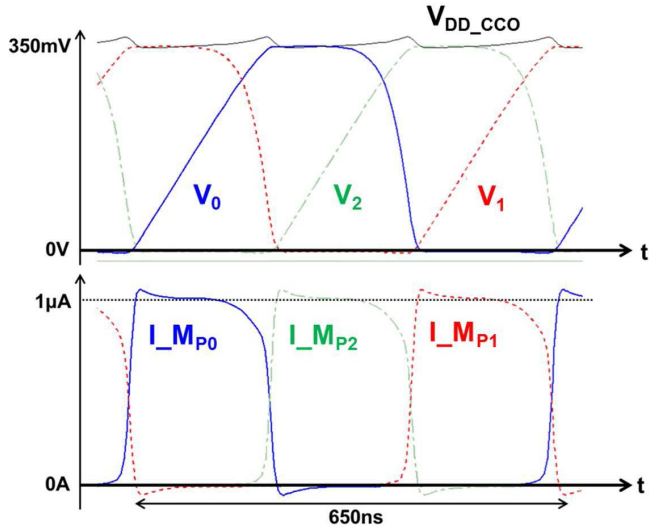


Fig. 8. Simulated waveform with the circuit in Fig.7.

The sum of the quantized CCON output (D_N [2:0]) is then subtracted from the sum of the CCOP output (D_P [2:0]) to obtain the output data, D_{OUT}.

As the VCO is implemented as a G_m stage followed by CCOs, the noise of the G_m stage has highest impact on the overall noise performance. This is addressed by applying choppers around the noise-dominating G_m stage to suppress the flicker noise. An alternative is to place the second chopper after the entire VCO rather than at the output of G_m stage [10]. In this approach, the demodulation can be performed in the digital domain, since the quantization noise does not exceed the circuit thermal noise floor over the Nyquist band. However, in the proposed design, the quantization noise dominates at high frequencies, which will be modulated to baseband if the demodulation is performed in digital domain (after the VCO). The choice of performing chopping on the G_m stage only cannot address the CCO mismatch problem, which is the fundamental limit of our purposed structure. In the following section, the G_m-CCO structure will be examined in detail.

III. GM-CCO Structure

A. Operation Principle

The simplified G_m-CCO structure is shown in Fig. 7. It contains a G_m stage, controlled by the input voltage V_{IN}, and a ring oscillator driven by the current provide from the G_m stage. The bias current I_B sets the free-running frequency; the oscillating frequency is tuned by $G_m V_{\mathrm{IN}}$. To gain insight to the circuit operation, the circuit analysis is simplified with the followings. First, for sensor applications, the required current is typically small, in the nanoampere to microampere range. All devices are biased in the weak inversion region. Second, the drain voltage of the current source, which is the supply voltage of the CCO, $V_{\mathrm{DD\_CCO}}$, remains constant. Third, the current I_B flows into either branch of M_{P0}, M_{P1}, and M_{P2} at a given time, and charges the capacitors C_0, C_1, and C_2 sequentially.

The operation principle is described as follows. Assume the input voltage is zero, and the current I_B is determined by the gate bias voltage V_B. As the example waveforms illustrated in Fig. 7, V_2 is at the ground voltage initially. The transistor M_{P0} is turned on and the current I_B starts to charge C_0, causing V_0 to rise linearly. As V_0 rises, transistor M_{N1} is gradually turned on and M_{P0} is turned off, these results in the discharging of capacitor C_1 and the exponential falling of V_1. As V_1 approaches zero, it turns on M_{P2} to start another phase of the charging/discharging behavior. Each charging phase takes a duration of $CV_{\mathrm{DD\_CCO}}/I_B$, and one VCO cycle contains N charging phases, which yields the oscillating frequency of

$$f_{\mathrm{VCO}} = \frac{I_B}{NCV_{\mathrm{DD\_CCO}}}. \tag{3}$$

Considering V_{IN}, the I_B term in (3) is replaced with I_B–$G_m V_{\mathrm{IN}}$. It is straightforward to see that f_{VCO} is linearly controlled by V_{IN}. The VCO tuning gain, K_{VCO}, can be expressed as

$$K_{\mathrm{VCO}} = \frac{G_m}{NCV_{\mathrm{DD\_CCO}}}. \tag{4}$$

The value of $V_{\mathrm{DD\_CCO}}$ is approximately the $|V_{\mathrm{GS}}|$ required to conduct I_B current for transistors M_{P0} to M_{P2}.

Fig. 8 shows the simulated waveforms of the circuit in Fig. 7. The capacitance C is chosen to be 520 fF, implemented by Metal-Oxide-Metal Capacitor (MOMCAP); transistors M_P and M_N are sized at 24 μm/500 nm with a total gate capacitance of 73 fF, and $I_B = 1$ μA. The simulated VCO oscillation period is 650 ns, while the estimated result using (3) and (4) is 623 ns. The simulated $V_{\mathrm{DD\_CCO}}$ is approximately 350 mV.

B. Noise

In a VCO-based ADC, the timing uncertainties at the output of VCO cause the sampler to sample wrong values. The timing uncertainties are caused by the phase noise, which is originated from the device noise in the VCO. To discuss the noise effect in a VCO-based ADC, we begin with the followings. First, the relationship between the VCO output phase noise S_Φ(f) and the input-referred noise S_{VIN}(f) can be expressed as

$$S_{\mathrm{VIN}}(f) = S_\Phi(f)\frac{f^2}{K_{\mathrm{VCO}}^2}. \tag{5}$$

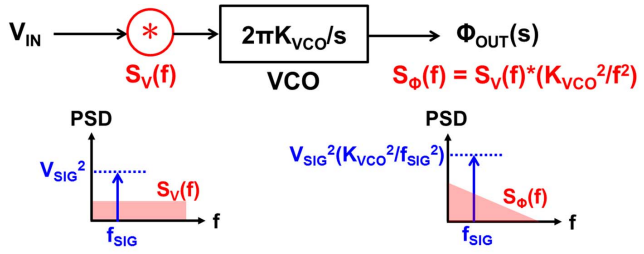


Fig. 9. Relationship between VCO input-referred noise and output phase noise.

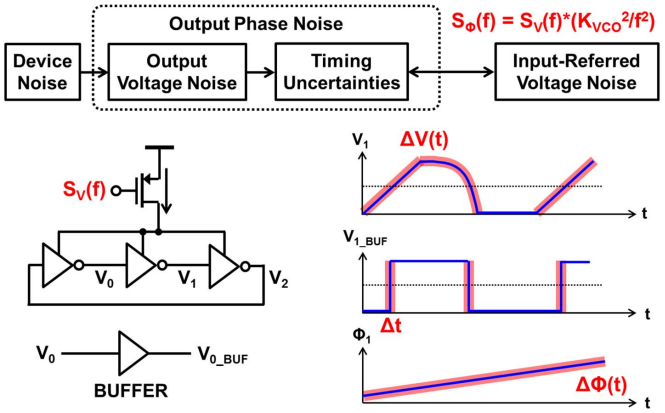


Fig. 10. Noise behavior in VCO-based integrators.

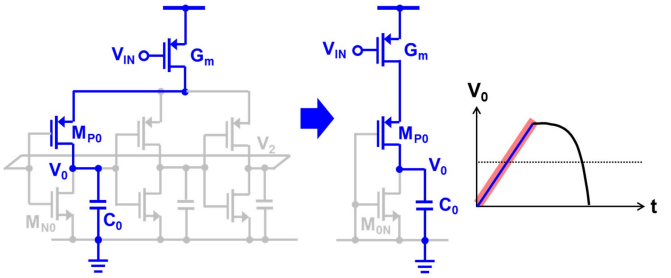


Fig. 11. Output noise contributors when V_0 is rising.

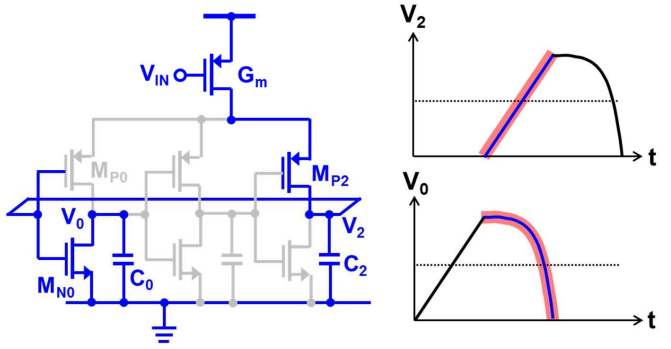


Fig. 12. Output noise contributors when V_0 is falling.

With (5), the phase noise of a ring oscillator can be referred to VCO input. This is illustrated in Fig. 9. Second, the output phase noise, which exhibits as timing uncertainties after buffering (Fig. 10), is originated from VCO output voltage noise [19]. This voltage noise comes from the charging/discharging operation of the G_m to load capacitors. By analyzing the contributions of noise sources, i.e., G_m stage and PMOS/NMOS of CCO in the charging and discharging phases, the noise of the VCO-based ADC can be estimated and optimized. Both the rising edge and the falling edge of the inverter stage of CCO should be examined in the phase noise analysis, as they both influence the rising/falling edges of the next stage. In the following analysis, we focus on the output noise of V_0, as the noise of V_1 and V_2 is the same as that of V_0.

First, we examine the condition when V_0 is rising (V_2 remains zero), as illustrated in Fig. 11. In this case, only G_m and M_{P0} contributes to the output voltage noise at V_0. Since M_{P0} is in the cascaded configuration, its noise is attenuated by the output resistance of G_m, and thus the G_m is the major noise contributor in this state.

Next, the case when V_0 is falling is examined: during this time, V_2 is in its charging phase, as shown in Fig. 12. In this case, there are three noise contributors: G_m, M_{P2}, and M_{N0}, where G_m and M_{P2} contributes to the noise in V_2 that control the gate voltage of M_{N0}, and M_{N0} itself also generates noise to V_0. For simplicity, we discuss the total input-referred noise of M_{N0}, which is the noise of V_2. Similar to that of the previous case, M_{P2} contributes negligible noise due to the degeneration from the G_m. The output noise spectrum at V_2 contributed by G_m can be expressed as

$$S_{V2,\mathrm{G_m}}(f) = (G_m R_{o2})^2 \left(\frac{K}{C_{ox} W_{G_m} L_{G_m}} \frac{1}{f} + \frac{4kT\gamma}{G_m}\right) \times \left(\frac{1}{1+4\pi^2 R_{o2}^2 C_2^2 f^2}\right) \quad (6)$$

where the R_{o2} denotes the total output resistance of node V_2, which is usually with the order of megohm range. Together with C_2 in the order of sub-pF range, the low-pass corner is beyond the target signal bandwidth, and the low-pass factor can be ignored. The noise contributed by M_{N0} can be expressed as

$$S_{V2,MN0}(f) = \frac{K}{C_{\mathrm{ox}} W_{\mathrm{MN0}} L_{\mathrm{MN0}}} \frac{1}{f} + \frac{4kT\gamma}{g_{m,\mathrm{MN0}}}. \quad (7)$$

Now we compare (6) to (7). In general, the $(G_m R_{o2})^2$ term is rather large, which implies (6) is larger than (7). This suggests that most of noise comes from the G_m rather than M_{N0}. In particular, at low frequencies, the flicker noise of the G_m dominates the noise performance.

The above observation led us to the proposed implementation strategy: applying choppers to mitigate the G_m noise, while for the design of the CCO cells, choosing reasonably large devices is enough to keep its noise in check.

The analysis above is based on small-signal operation. In reality, the circuit operation condition changes over time. R_{O2} degrades at the end of the V_0 discharging (V_2 charging) phase as M_{P0} enters the triode region, and $g_{m,MN0}$ increases with V_2. Nonetheless, the analysis provides a simplified view to observe the behavior of the G_m-CCO architecture.

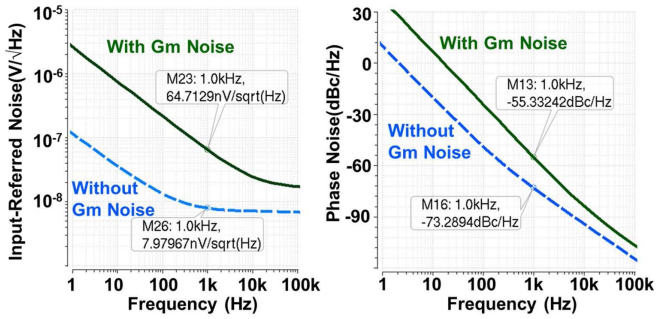


Fig. 13. Simulated input-referred and phase noise of G_m-CCO structure in Fig. 7 with and without G_m noise contribution.

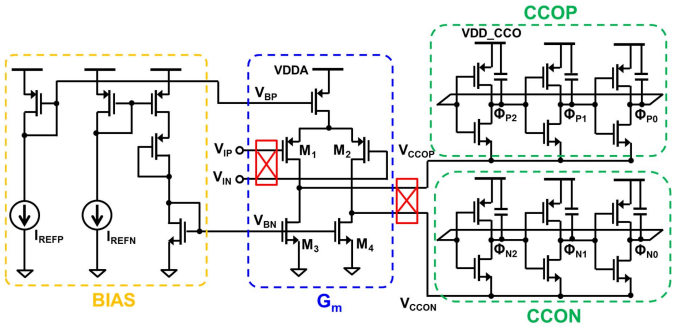


Fig. 14. Proposed circuit implementation of the chopped G_m-CCO.

The above discussions are verified in simulation. Fig. 13 shows the simulation results based on the circuit depicted in Fig. 7, with the design parameters mentioned in the previous section. It is observed that in the low-frequency band of interest, the G_m stage contributes significant flicker noise and severely raise the noise.

IV. Circuit Implementation

The schematic of the implemented chopped G_m-CCO is depicted in Fig. 14. Based on the idea described in Fig. 7, the G_m is implemented as a differential common-source stage; while the CCOs are folded connected to the G_m stage. In the G_m stage, thick-oxide transistors are used for input devices, M_1 and M_2, to prevent leakage current issue which occurs in the 40-nm CMOS process. In contrast to the conceptual design illustrated in Fig. 7, the flipped-up CCO topology is adopted. In this topology, the V_{DD_CCO} is separated from V_{DDA} which can be used to facilitate the control of the output common-mode level of G_m. The output buffers of CCOs use NMOS with high threshold voltage and PMOS with low threshold voltage, to convert the limited CCO swing to full rail for subsequent processing in following digital circuits.

Fig. 15 shows the detailed design considerations and operation. The current flowing through a single CCO (e.g., $I_{CCOP(N)}$) is the difference between I_L and I_{GMP}. If all the G_m current is injected into CCO, higher oscillation frequency (with the same K_{VCO}) is expected, and this leads to higher power consumption for the subsequent digital signal processing. Note that the output of G_m (drain nodes of M_1 and M_2) sees low

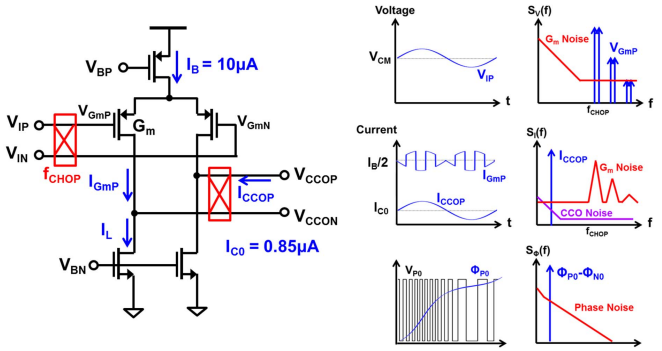


Fig. 15. (Left) Illustration of the biasing condition of G_m-CCO. (Right) Time-domain and frequency-domain behavior of signal and noise.

impedance from the source terminal of NMOS transistors of CCO, which is similar to that of the folded-cascode structure; hence, the common-mode feedback circuit is not required. In Fig. 15, $I_{GMP} = 5\ \mu$A, $I_L = 4.15\ \mu$A and $I_{C0} = 0.85\ \mu$A. The deviation of current difference between I_{GMP} and I_L can be regarded as variation of I_{CCOP}, and this is controlled by varying I_{REFP} and I_{REFN} through off-chip tuning during measurement. In practice, if only one reference current is allowed, a 1% deviation of I_{GMP} with I_L fixed results in 6% I_{CCOP} error, which is tolerable in this design. A careful current mirror design considering the effects of mismatch and channel length modulation can minimize this error.

In this design, the g_m/I_D value of input transistors M_1/M_2 are approximately 20 with input size of $80/2\ \mu$m, and M_3/M_4 have $56/10\ \mu$m in order to suppress the flicker noise. For a G_m of 100 μS and with a 4-mV_p (8 mV_{pp}) signal at G_m input, I_{CCOP} and I_{CCON} will have a swing of 400 nA_{pp} under 850-nA biasing current. This translates to $\pm 23.5\%$ frequency swing range in each CCO output. The CCO is designed with 15 μm/500 nm PMOS and 5 μm/500 nm nMOS as delay stages with total gate capacitance of about 20 fF. The load capacitors of CCO are implemented with MOMCAP to have approximately 520-fF capacitance, and the parasitic capacitance of each delay stage is about 73 fF. The CCO center frequency is approximately 1.05 MHz with 450-mV output swing. The simulated THD is about -80 dB under this input level (4 mV_p), and is degraded to about -52 dB under 14-mV_p input.

The noise profile is also shown in Fig. 15. The input voltage signal is modulated by the chopper; since I_{GMP} is modulated, the flicker noise of the G_m stage (contributed from M_1 to M_4) is mitigated. The signal is demodulated by the second chopper and fed to the CCOs. Although the flicker noise of the CCO is not solved, its contribution to the overall noise is not dominating, as analyzed in the previous section. The overall input-referred noise density $S_{VIN}(f)$ is thus mostly contributed from the thermal noise of G_m

$$S_{VIN}(f) = 8kT\gamma\left(\frac{1}{g_{m1}} + \frac{g_{m3}}{g_{m1}^2}\right). \tag{8}$$

From above, and assume M_3 and M_1 have the same g_m/I_D ratio, the calculated noise PSD is 23 $nV/\sqrt{Hz}$.

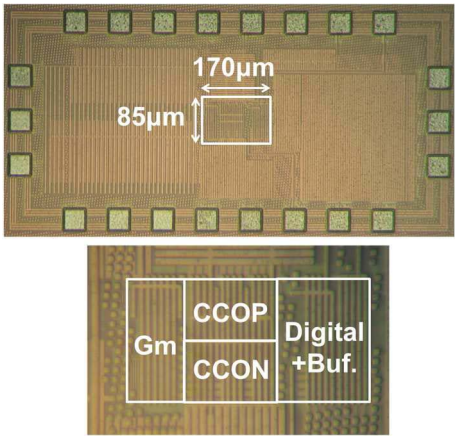
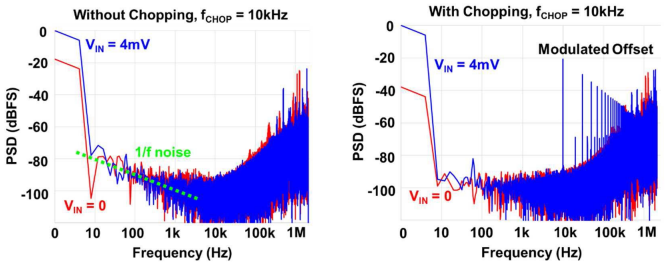


Fig. 16. Chip Microphotograph.



(a) (b)

Fig. 17. Output spectrum with a 4-mV_{DC} input (blue) and zero input (red). (a) Without chopping function. (b) With chopping function.

V. Measurement Results

The proposed VCO-based CTDSM is implemented in the TSMC 40-nm CMOS process; the chip micrograph is shown in Fig. 16, where the circuit core area is 0.0145 mm^2. The proposed circuit is measured with the following conditions. The input common-mode voltage V_{CM} is set to 0.3 V. Under this biasing condition, the VCO free-running frequency is approximately 1.05 MHz. The sampling frequency f_S is chosen to be 4.2 MHz (2^{23} Hz), and the chopping frequency f_{CHOP} is 10 kHz.

Fig. 17 shows the output 2^{21}-point FFT result (with Hanning windowing) measured with two input levels: zero input and 4-mV DC input, with the chopping function disabled [Fig. 17(a)] and enabled [Fig. 17(b)]. In Fig. 17(a), it is observed that with the chopping function disabled, the flicker noise dominates the noise performance below 1-kHz frequencies, and the extracted input-referred offset (DC tone with zero-input measurement) is approximately 487 μV. With chopping enabled, as shown in Fig. 17(b), most of the flicker noise is mitigated, and the input-referred offset is reduced to about 50 μV. The simulated 1-sigma offset is 55μV. Fig. 18 shows the measured input-referred offset voltage with and without the chopping function across five chip samples. With chopping, the worst case of residual offset is $+50/-67$ μV. The residue offset is mainly attributed to the mismatch of the two CCOs, since they are not chopped. Fig. 19 shows the DC SNR comparison versus different

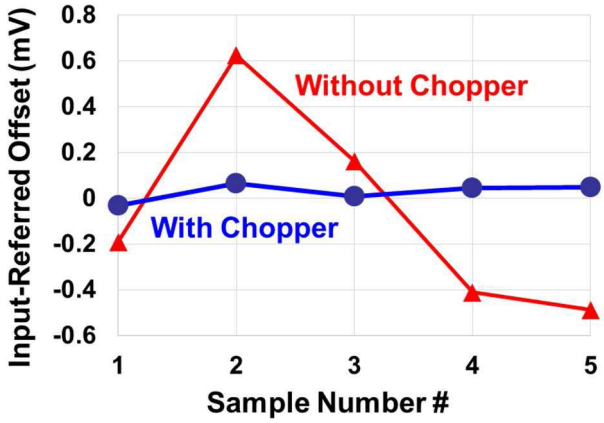


Fig. 18. Measured input-referred offset under different samples.

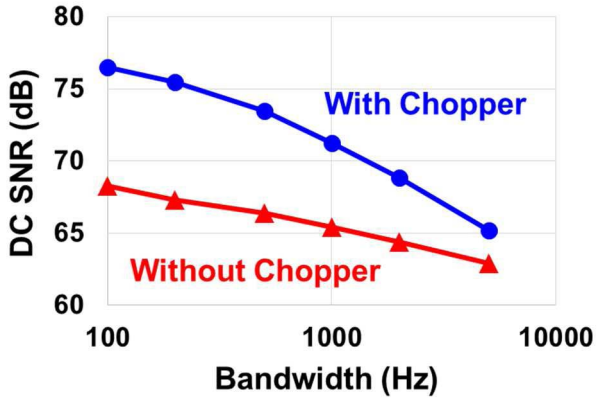


Fig. 19. Measured SNR with 4-mV_{DC} input under different bandwidth.

bandwidth, with and without the chopping function. The SNR improvement of activating choppers becomes more significant as the bandwidth is narrower.

Fig. 20 shows the FFT result with input signal frequency f_{IN} = 220 Hz and V_{IN} = 4 mV_p (8 mV_{pp}). A single-ended signal is generated from R&S UPV audio signal analyzer, and then transform to balanced differential form through a balun. The common-mode voltage is supplied from an external LDO voltage regulator. The measured signal-to-noise-and-distortion ratio (SNDR) under this condition is 61.85 dB and the SNR is 62.44 dB over a 5-kHz bandwidth. The THD is 70.8 dB. The circuit can support an input swing larger than 4 mV_p with slightly increased in-band noise floor and nonlinearity. The dynamic range plot is shown in Fig. 21. The peak SNDR is 64.83 dB with V_{IN} = 14 mV_p (28 mV_{pp}), and the THD is -66 dB in this case. Under this condition, the CCO experiences large current excursion, roughly $\pm 80\%$ of biasing condition. As V_{IN} is further increased to 16 mV_p, the measured SNDR degrades to 55 dB. This circuit is also tested with various input frequencies from 48 Hz to 1600 Hz at 4-mV_p input, and the SNDR ranges from 60 to 62 dB. This result demonstrates that the proposed circuit functions properly over different input frequencies.

Fig. 22 shows the measured input impedance under different chopping frequencies. This test is conducted by applying a

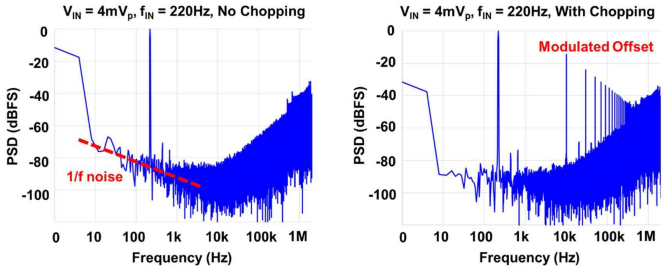


Fig. 20. Output spectrum with a 4 mV_p (8 mV_{pp}), 220-Hz sinusoidal input. (a) Without chopper. (b) With chopper.

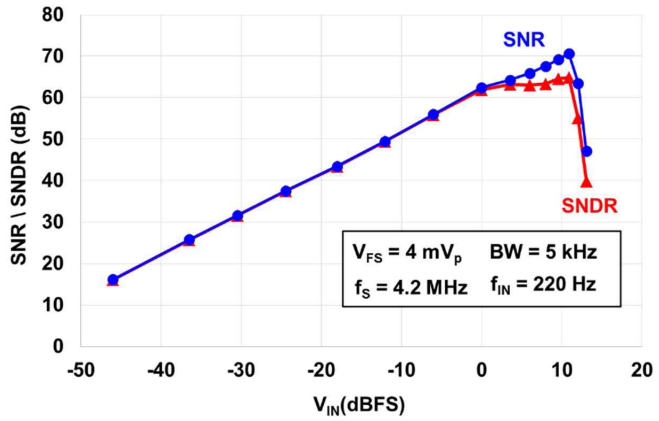


Fig. 21. Dynamic range plot of the VCO-based ADC.

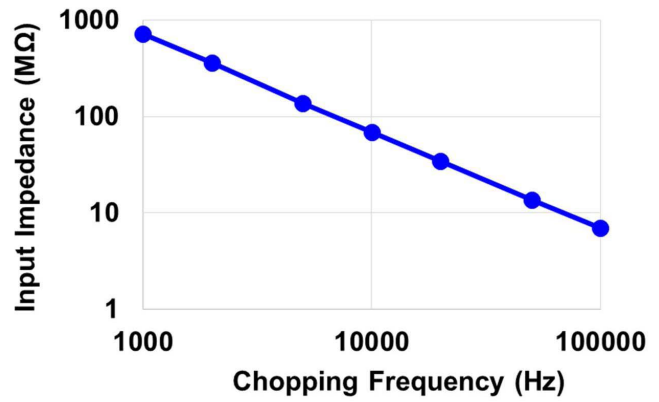


Fig. 22. Measured input impedance under different choppoing frequencies.

20-mV DC input to the G_m stage, and measures the input current using Keysight 34470A digital multi-meter. The input impedance of the circuit is measured to be 70 MΩ under a 10-kHz f_{chop}, which is close to the simulated value of about 90 MΩ. The finite input impedance is originated from the G_m input capacitance of 550 fF and $Z_{\text{in}} = 1/2 f_{\text{chop}} C_{\text{in}}$.

Fig. 23 shows the measured input-referred offset versus different input common-mode voltage V_{CM}, CCO supply voltage $V_{\text{DD\_CCO}}$, and G_m stage supply voltage V_{DDA}, to determine the input common-mode range (ICMR), common-mode rejection ratio (CMRR), and power supply rejection ratio (PSRR). Fig. 24 shows the SNDR versus the same parameters (V_{CM}, $V_{\text{DD\_CCO}}$, and V_{DDA}) as those appear in Fig. 23. The measured ICMR is from 0.15 to 0.65 V with fairly consistent SNDR performance. For the input common-mode voltage

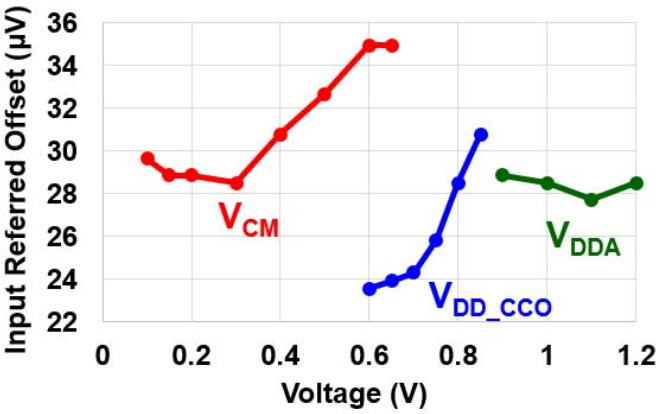


Fig. 23. Measured input-referred offset under different V_{CM}, $V_{\text{DD\_CCO}}$, and V_{DDA}.

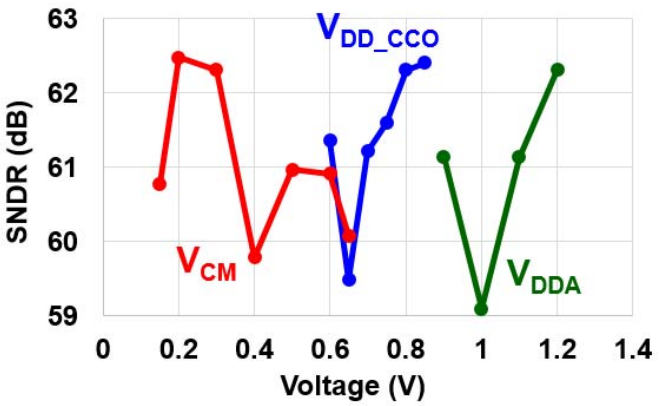


Fig. 24. Measured SNDR under 4-mV_p input and different V_{CM}, $V_{\text{DD\_CCO}}$, and V_{DDA}.

lower than 0.15 V, the input pair enters triode region; on the other hand, if the input common mode is higher than 0.65 V, the tail current source of G_m enters triode region. Across the valid ICMR (0.15–0.65 V), the input-referred offset varies by 6.5 μV (28.5–35 μV) over the 500-mV V_{CM} range. This implies that the CMRR is around 97 dB. Similarly, the PSRR is extracted by observing the variation of the input-referred offset under a certain range of $V_{\text{DD\_CCO}}$ variation. Form Fig. 23, for a $V_{\text{DD\_CCO}}$ variation range of 0.6 to 0.85 V, the offset varies by 7.2 μV. This suggests a 91-dB PSRR. The effect of V_{DDA} variation is not as significant as that of the $V_{\text{DD\_CCO}}$ variation. The main reason is that CCOs are not chopped; hence, the input-referred offset mainly comes from the CCOs, rather than the G_m stage.

The whole VCO-based ADC consumes 17 μW. Among which, the G_m stage draws 10 μA from a 1.2-V V_{DDA}; the CCOs consumes 1.7 μA with $V_{\text{DD\_CCO}}$ of 0.8 V. The digital circuits dissipate about 3.5 μA dynamic current from a 1-V V_{DDD}. The power from I/O buffers is excluded. Table I compares this paper to other sensor readout circuits, including VCO-based ADCs, time-domain ADCs, and conventional analog approaches. Thanks to the chopping technique, this paper achieves competitive low-frequency input-referred noise density of 32 nV/$\sqrt{\text{Hz}}$. The signal bandwidth can be extended to 5 kHz with a peak SNDR over 60 dB. Compared to other prior approaches, this design achieves similar performance with

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH SENSOR READOUT CIRCUITS

	This Work	JSSC 2015 [11]	JSSC 2017 [10]	JSSC 2015 [8]	CICC 2014 [21]	JSSC 2013 [7]	JSSC 2017 [20]	TCASI 2014 [22]	JSSC 2012 [5]	ESSCIRC 2012 [6]	ESSCIRC 2012 [23]
Typology	VCO-Based						Time Domain		CFIA+ DTDSM	Gm-C CTDSM	DTDSM
Tech.	40 nm	65 nm	40 nm	180 nm	65 nm	130 nm	40 nm	180 nm	700 nm	700 nm	350 nm
VDD	1.2 V	0.5 V	1.2 V	1.8 V	1.2 V	1 V	0.6 V	1.5 V	5 V	5 V	2.8 V
Power	17 µW	2.3 µW	7 µW	340 µW	36 µW	125 µW	3.3 µW	15 µW	1.35 mW	1.2 mW	42 µW
FSR	8 mV_{pp}	1 mV_{pp}	100 mV_{pp}	4 μA_{DC}	2 mV_{pp}	100 mV_{pp}	40 mV_{pp}	130 mV_{pp}	80 mV_{pp}	80mV_{pp}	60 mV_{pp}
BW	5 kHz	500 Hz	200 Hz	1.25 Hz	10 kHz	10 kHz	150 Hz	2.267 kHz	10 Hz	2 kHz	0.5 Hz
f_{SAMPLE}	4.2 MHz	1 kHz	3 kHz	10 MHz	300 kHz	10 MHz	25 MHz	5.5 kHz	10 kHz	5 MHz	500 kHz
Noise PSD	**32 nV/√Hz**	58 nV/√Hz	424 nV/√Hz	868 pA/√Hz	100 nV/√Hz	212 nV/√Hz	600 nV/√Hz	3.97 µV/√Hz	16 nV/√Hz	20 nV/√Hz	756 nV/√Hz
SNDR	61.85 dB	48.7 dB	74 dB	73 dB	43 dB	55.5 dB	40 dB	47.7 dB	126 dB*	90 dB**	101 dB*
THD (f_{in})	-70.8 dB (220Hz)	-52 dB (10Hz)	-79 dB (203Hz)	--	-56.7 dB	--	-40 dB (11Hz)	-58 dB	6 ppm (INL)	-102 dB (10Hz)	±4 ppm (INL)
FoMs	146.5 dB	132.1 dB	148.6 dB	108.6 dB	127.4 dB	143.4 dB	116.6 dB	129.5 dB	153.7 dB	152.2 dB	141.8 dB
FoMw	1.68 pJ	10.3 pJ	4.27 pJ	37.3 nJ	158.4 pJ	12.8 pJ	135 pJ	14 pJ	147 pJ	11.6 pJ	458 pJ
Area(mm^2)	0.0145	0.025	0.135	0.36	0.258	0.2	0.015	0.057	6	6	0.32

$$\text{FoMs} = \text{SNDR} + 10\log\left(\frac{\text{BW}}{\text{Power}}\right) \qquad \text{FoMw} = \frac{\text{Power}}{2^{\text{ENOB}} \times 2\text{BW}}$$

lower power consumption and smaller chip area [5], [6]. The proposed circuit can accommodate an input signal swing up to 28 mV_{pp} with 10–12 bit ENOB under various bandwidths. This allows the circuit to be directly interface to variable sensing applications. To allow an even larger input swing, a feedback loop [6] or calibration technique [10] can be implemented to improve the non-linearity and maintain SNDR.

Since the CCOs are not chopped, the suppression of input-referred offset is limited by this design choice. For low-frequency applications, this issue can be further improved by applying a system chopper [5] (or called nested chopper) with a low-chopping frequency, or by using the architecture similar to [10] to place the demodulation chopper after CCOs. Although the open-loop architecture might be prone to gain variations, for applications with ratiometric design, such like electronic compasses [2], can easily eliminate this problem.

VI. CONCLUSION

A simple yet efficient sensor readout circuit is presented in this paper. The VCO-based structure processes the signal in the phase domain, and is adopted to directly interface with the sensors. In this paper, the VCO is implemented as a G_m-CCO. From circuit analysis, it shows that the G_m stage dominates the noise performance. This issue is mitigated by applying the chopping technique to the G_m stage to remove its $1/f$ noise. On the other hand, this approach does not address the mismatch between the two CCOs, which manifests itself as a residual offset. Measurement shows that the input-referred noise PSD is only 32 nV/$\sqrt{}$Hz. The resulting circuit figure-of-merits are comparable to other state-of-the-art VCO-based ADCs.

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Chih-Chan Tu received the B.S. degree in electrical engineering and the M.S. degree in electronics engineering from National Taiwan University, Taipei, Taiwan, in 2010 and 2013, respectively, where he is currently pursuing the Ph.D. degree.

In 2014, he joined TSMC as an Intern, where he was involved in the phase-locked loop design. His current research interests include sensor readout circuits and systems, and the applications include bio-potential monitoring and magnetic field sensing.

Mr. Tu was a recipient of the Taiwan Engineering Medicine Biology Association Annual Outstanding Master Thesis Award in 2014. He is also honored with TSMC scholarship from 2013 to 2014. He serves as a reviewer for the IEEE SENSORS JOURNAL. He is the moderator of the discussion board "Electronics" in ptt.cc, the largest and most active BBS forum in Taiwan.

Yu-Kai Wang was born in Taipei, Taiwan, in 1992. He received the B.S. degree in electrical engineering from National Taiwan University (NTU), Taipei, Taiwan, in 2014, and the M.S. degree from the Graduate Institute of Electrical Engineering, NTU, in 2017.

He is currently with MediaTek, Hsinchu, Taiwan, where he is involved in mixed-signal and RF circuits design.

Tsung-Hsien Lin (M'03–SM'09) received the B.S. degree in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Los Angeles, CA, USA, in 1997 and 2001, respectively.

In 2000, he joined Broadcom Corporation, Irvine, CA, USA, where he was a Senior Staff Scientist, where he was involved in wireless transceiver developments. In 2004, he joined the Graduate Institute of Electronics Engineering, Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan, where he is currently a Professor. His current research interests include the design of wireless transceivers, clock and frequency generation systems, delta-sigma modulators, and transducer interface circuits.

Dr. Lin was a recipient of the Best Presentation Award for his paper presented at the 2007 IEEE VLSI-DAT Symposium, the Teaching Excellence Award from National Taiwan University in 2007, 2008, 2014, and 2015, and the Exceptional Teaching Excellence Award in 2009, and the co-recipient of the Best Paper Award at the IEEE VLSI-DAT Symposium in 2015. He served on the IEEE Asian Solid-State Circuit Conference (A-SSCC) Technical Program Committee (TPC) from 2005 to 2011 and was the TPC Vice-Chair for 2011 A-SSCC. He was a Guest Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC) in 2012 and was an Associate Editor of the IEEE JSSC from 2013 to 2015. He served on the ISSCC International Technical Program Committee (ITPC) from 2010 to 2016, and was the FE Regional Committee Chair in 2016 ISSCC. He is the TPC Chair of 2017 A-SSCC.