A 75-MHz Continuous-Time Sigma–Delta Modulator Employing a Broadband Low-Power Highly Efficient Common-Gate Summing Stage

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***Abstract*— A wide-bandwidth (BW) power-efficient continuous-time ΣΔ modulator (CTΣΔM) is presented. The modulator introduces a third-order filter implemented with a lossless integrator and a multiple-feedback single-amplifier biquadratic filter with embedded loop stability compensation. An active summing block is implemented by employing a common-gate current buffer followed by a transimpedance amplifier. This combination relaxes the specification requirements of the operational amplifier by making its required BW independent of the closed-loop gain. The proposed technique achieves optimum BW with reduced power consumption, making it functional for over gigahertz operation. Fabricated in a standard 40-nm CMOS technology, and clocked at 3.2 GHz, the CTΣΔM achieves a signal-to-noise-and-distortion ratio of 65.5 dB over 75-MHz BW while consuming 22.8 mW of power. The obtained Walden's figure of merits is 98 fJ/conv-step.**

***Index Terms*— Analog-to-digital converters (ADCs), broadband ADCs, current buffer, low power, oversampling ADCs, sigma–delta modulators, single amplifier biquad (SAB), transimpedance amplifiers (TIAs).**

I. Introduction

HIGH data rates required for emerging wireless standards demand continuous-time ΣΔ modulators (CTΣΔMs) with a bandwidth (BW) higher than 20 MHz [1]–[10], which correspondingly increases the modulator's power consumption. Among other challenges, the increased power consumption due to higher loop filter requirements is one of the most critical one. In order to address this issue, filter architectures based on single amplifier biquad (SAB) realizations have been previously proposed to reduce static power [11]–[13]. However, architectures that implement excess loop delay (ELD) compensation with a fast path around the quantizer demand more power consumption from the operational amplifiers (OpAmps).

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Feedforward (FF) CTΣΔMs are the architectures of choice for low-power implementations. However, the use of an active summing amplifier required for the realization of the FF coefficients paths and ELD compensation path [14] is not very attractive due to the excessive power required by the OpAmp. To overcome this drawback, the use of passive networks for the implementation of the FF paths and ELD compensation path has been recently implemented [2], [6]. Even though a passive summing network enables high operating frequencies, the lack of an active summing amplifier limits the FF paths coefficients to be less than unity. Reference [2] uses capacitors to implement the FF paths; the coefficient value is defined by the ratio of an FF capacitor and the total capacitance at the quantizer input. Therefore, the FF coefficients are less than unity, then demanding more gain and signal swing at the output of the filter OpAmps to compensate for the FF coefficient value. Moreover, the use of a current steering digital-to-analog coverter (DAC) becomes more challenging due to the lack of a true OpAmp virtual ground to inject the current. Dong *et al.* [6] present similar characteristics as [2] with the difference that the passive summing node is implemented employing resistors and capacitors to increase system BW. Alternatively, digital compensation can also be embedded in the quantizer [15], [16] to eliminate the summing node. However, this increases the signal swing at the quantizer input by one plus the gain of the feedback ELD coefficient, thereby burdening the linearity of the OpAmp driving the quantizer, and limiting signal-to-noise ratio (SNR). Moreover, if a loop filter topology without a summing amplifier is desired, the zero-order path can be implemented using differentiated DACs at the input of the last integrator [17]. This solution requires two fast path DACs to perform the differentiation. Finally, lead compensation can be used to implement the zeroth-order path [7], [8]. However, due to the increase of extra paths at the input of the last integrator, the power consumption from the last OpAmp is similar or larger than the power of the first OpAmp.

Previous efforts intended to reduce the power consumption of the summing amplifier by increasing its feedback factor have been made earlier. Reference [18] implemented the FF coefficients using GM-cells in order to reduce the effect of loading from resistors in both loop filter and summing amp. However, this approach requires extra power consumption and silicon area for the GM-cells, and for high operating frequencies, the power reduction on the summing amp is overshadow by the power consumption required by the

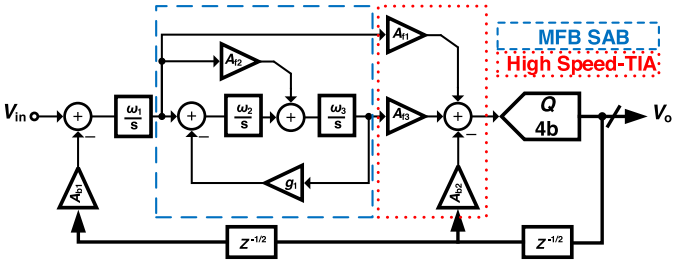

Fig. 1. Proposed architecture for the third-order 4-b CTΣΔM.

GM-cells. Reference [19] proposed the replacement of the traditional summing amp and voltage mode quantizer by a common gate buffer and a current-mode quantizer. The current buffer collects the current generated by the FF resistors and fast path DAC, and it passes the collected current into a current mirror that amplifies and copies the current for further comparison. Although, very efficient for midrange sampling frequencies (<1000 MHz) for higher operating frequencies, the implementation is limited by the parasitic poles due to the current mirroring operations needed. Alternative solutions may offset this issue in advanced technologies. Notice that the current mode quantizer requires additional static power consumption to generate the current comparison references. Since the demand of higher BWs is always increasing, it is important to propose a voltage-mode solution that can achieve higher sampling rates employing conventional voltage-mode flash analog-to-digital converters (ADCs).

This paper presents a summing amplifier based on a common-gate current buffer that decouples the dependency of the closed-loop gain and the design specifications of the summing amplifier OpAmp. This approach enables high-frequency operation for closed-loop transimpedance amplifiers (TIAs) and relaxes the power consumption requirements. Moreover, the addition of the current buffer provides an extra degree of freedom for the design of a closed-loop OpAmp with optimum step response for high-frequency operation. Detailed analysis of design for the optimum phase margin and its best step response is presented. This simple approach avoids adding extra capacitors for phase margin compensation, which introduces additional delay that limits the performance at gigahertz operation.

This paper is organized as follows. Section II presents the implemented architecture and discusses associated system-level details. Section III presents an analysis for optimum step response of a closed-loop summing stage. Section IV presents the detailed circuit implementation of the most relevant blocks. Section V discusses the obtained measurement results. Finally, Section VI presents a summary of the results and conclusions.

II. Modulator's Architecture

The selected CTΣΔM architecture shown in Fig. 1 utilizes a third-order filter and a 4-b quantizer. FF topology is selected due to its simplicity and robustness. Fig. 2(a) shows the selected filter architecture with a conventional summing amplifier, for which the specifications of A_{v3} are defined by the FF gain factors, ELD compensation coefficient, clock frequency, and quantizer's input load, which make this implementation unpractical for gigahertz-range clock frequencies. Fig. 2(b) shows the filter architecture, including the conceptual proposed current buffer. The second-order portion of the filter is implemented employing a multiple feedback (MFB) SAB and is formed by R_2, R_3, R_4, C_y, C_2, and A_{v2}; one of the FF path coefficients is embedded on the SAB and realized with a single capacitor C_x. The overall transfer function for the MFB SAB is given in (1). The remaining two FF paths implemented by R_{f1} and R_{f2}, and the ELD compensation fast-DAC (FDAC) are combined at the low impedance nodes available at the output of the current buffer block and the input of the TIA formed by A_{v3} and R_{fb}. The quantizer uses a 4-b flash. Also, the main-DAC (MDAC) and FDAC were implemented with current steering architectures. Flip-flops sample the output data from the quantizer to synchronize the feedback data with the desired clock edge [2]

$$\frac{V_{ox,,2}}{V_{ox,,1}} = -\frac{(1+sR_2C_x)\left(\frac{1}{R_3R_2(C_x+C_y)C_2}\right)}{s^2+s\frac{\left(\frac{R_3R_4}{R_2}C_2+R_3C_2+R_4C_2\right)}{R_3R_4(C_x+C_y)C_2}+\frac{1}{R_3R_4(C_x+C_y)C_2}}. \tag{1}$$

The proposed current-mode adder (implementation details are given in Section IV) isolates the resistors and the input of the amplifier A_{v3}. Connecting R_{f1} and R_{f2} directly to the amplifier's input used in conventional solutions [Fig. 2(a)] reduces the feedback factor (β) and then demands more dc gain and BW from A_{v3} to maintain loop functionality. Furthermore, since A_{v3} processes the pulsed signal generated by FDAC, it requires a very fast transient response. If implemented with a single dominant pole, the settling time of A_{v3} is inversely proportional to the amplifier's transconductance and feedback factor β[18], and proportional to the load impedance. For high sampling rates (smaller time for settling) and small β, the OpAmp specifications steadily increase in both circuit complexity and power consumption. In the proposed solution, the current-mode buffer isolates the FF resistors from the TIA input. If the buffer provides a current gain of one, the FF coefficient gain is defined by the ratio of resistors as in the conventional summing amplifier. However, the selected closed-loop gain does not define the specifications for A_{v3}, since $\beta$is defined by R_{fb} and the output impedance from the current buffer. To ensure Av_3 stability, the impedance looking back at the current buffer and FDAC is adjusted to make β close to the optimum value. The latter enables fast settling time and power consumption reduction while ensuring loop functionality.

The implementation of an active summing amplifier with high gain can also help to relax the specifications from other building blocks. Fig. 3(a) shows the effect of a passive summing node that provides attenuation; hence, as the swing at the internal nodes of the loop filter and FDAC increase, more current and a larger output swing range is required from the OpAmps. However, if an active architecture with gain is used as shown in Fig. 3(b), the output swings at the internal nodes of the filter are reduced demanding less output current, and the swing specifications are relaxed allowing lower voltage operation with superior linearity.

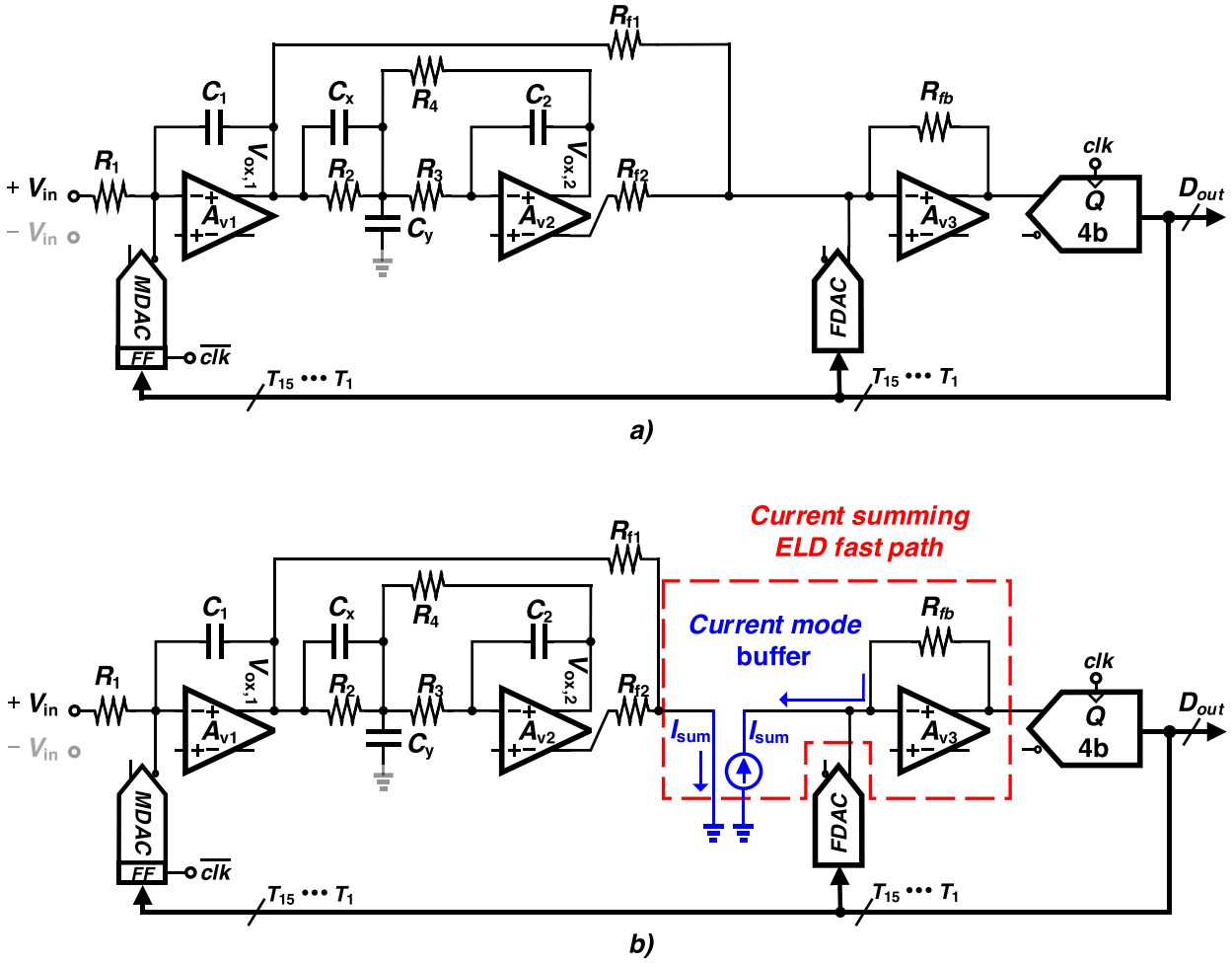

Fig. 2. (a) The block diagram of a CTΣΔM with conventional summing amplifier. (b) The block diagram of the selected CTΣΔM architecture with summing amplifier and conceptual current buffer.

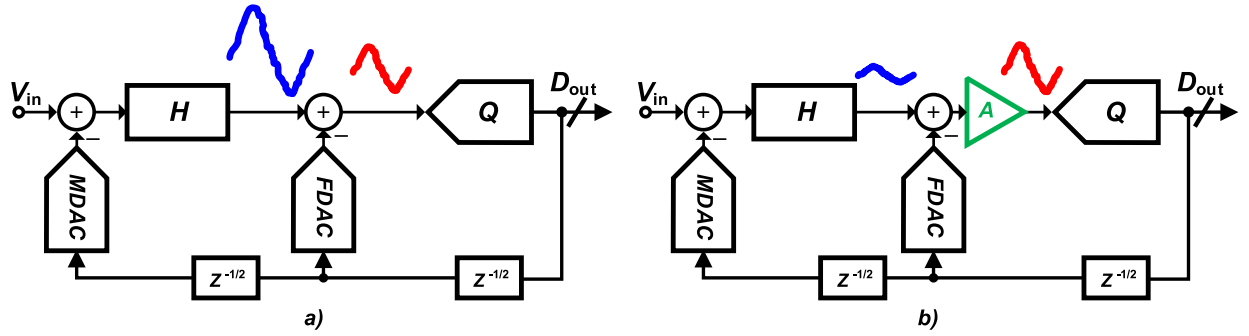

Fig. 3. CTΣΔM voltage swing. (a) Passive summing node implementation with attenuation. (b) Active summing amplifier with gain.

III. High-Frequency Current-Mode Buffer and ELD Implementation

This section discusses the design specifications for the power optimization of closed-loop OpAmps operating in the gigahertz range. The small-signal model of the ELD circuit with current buffer for the OpAmp and FDAC is shown in Fig. 4. R_{buf} represents the impedance looking back into the current buffer, R_{fb} is the OpAmp resistor in feedback, OpAmp A_{v3} is represented by the voltage-controlled current source $g_m \cdot V_x$ and the output resistor R_o, the load capacitor C_L is dominated by the input capacitance of the quantizer, I_{FDAC} represents FDAC output current, and C_{in} is the parasitic capacitance at node V_x composed by the input capacitance of A_{v3} and the parasitics from FDAC and current buffer.

The conventional analysis of OpAmp circuits with passive components connected in feedback normally yields a first-order solution if the input parasitic capacitance C_{in} is very small compared with the load capacitor ($C_L \ll C_{\text{in}}$). The step response is then characterized by a first-order differential equation, where the small signal transconductance required for a settling time error ε within a time period $T = 1/2f_s$ leads to the following result [20]:

$$g_m = \frac{2\ln\left(\frac{1}{\varepsilon}\right) C_L f_s}{\beta} - \frac{1}{\beta R_L} \tag{2}$$

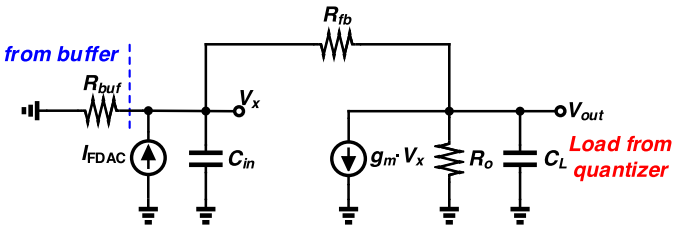

Fig. 4. Small signal model of summing amp with current buffer included.

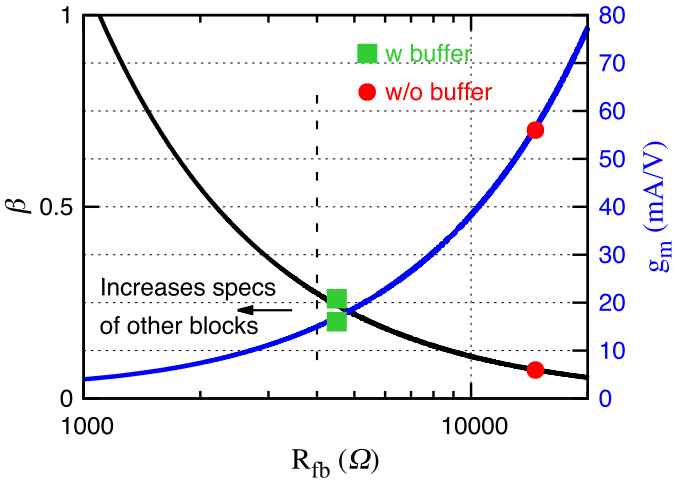

Fig. 5. Optimum feedback factor and transconductance required versus feedback resistor sweep while maintaining $\zeta = 0.9$.

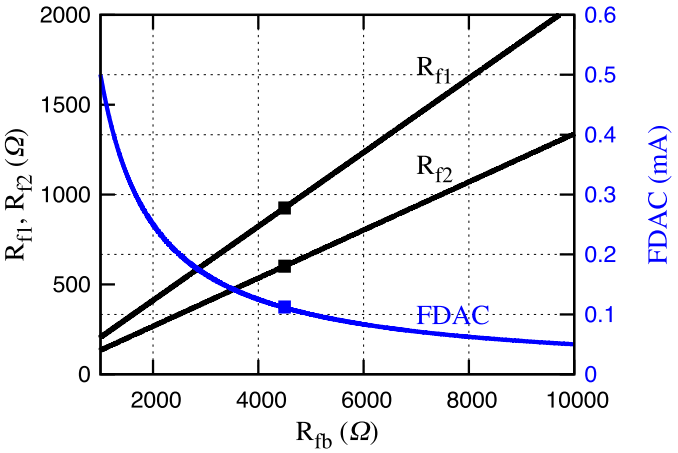

Fig. 6. Feed forward resistors and FDAC current versus R_{fb} value.

where f_s is the sampling frequency at which the pulses from the FDAC are received, ε is the desired settling error, R_L is the output resistance, including the loading effect from R_{fb}. $R_L = R_o \| R_{fb}$ and β represent the feedback factor, $\beta = R_{buf}/(R_{buf} + R_{fb})$. The use of the current buffer allows us to increase the value of β since R_{buf} can be made very large. It is clear from (2) that when β is maximum (closer to one) the minimum transconductance gain is needed. This makes the implementation of the current buffer very attractive for low-power applications. For high-frequency operation, a more complete analysis needs to be performed to ensure amplifier stability.

For higher frequencies and advanced process technologies, C_{in} can be within one order of magnitude smaller than C_L.

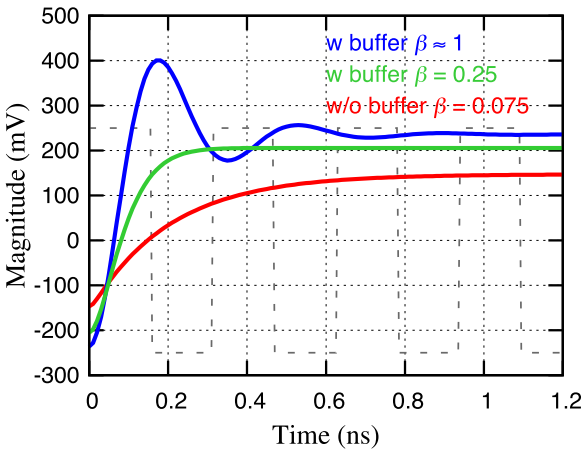

Fig. 7. ELD step response: no buffer (red), with buffer (blue), and with buffer using controlled output impedance (green).

Thus, including the effect of C_{in} leads to a second-order transimpedance function

$$\frac{V_{out}}{I_{FDAC}} = -\frac{\left(g_m - 1/R_{fb}\right)\frac{1}{C_{in}C_L}}{s^2 + s\left(\frac{1}{R_{fb}C_{in}\beta} + \frac{1}{C_L R_L}\right) + \frac{1}{\beta R_{fb} R_L C_{in} C_L} + \frac{\left(g_m - 1/R_{fb}\right)}{R_{fb}C_{in}C_L}}. \tag{3}$$

According to this result, the natural frequency and damping factor can be obtained as

$$\omega_n^2 = \frac{1+\beta R_L\left(g_m - 1/R_{fb}\right)}{\beta R_{fb} R_L C_{in} C_L} \approx \frac{g_m}{R_{fb}C_{in}C_L} \tag{4}$$

$$\zeta = \frac{\frac{1}{R_{fb}C_{in}\beta} + \frac{1}{C_L R_L}}{2\cdot\sqrt{\frac{1+\beta R_L\left(g_m - 1/R_{fb}\right)}{\beta R_{fb} R_L C_{in} C_L}}} \approx \frac{\frac{1}{R_{fb}C_{in}\beta} + \frac{1}{C_L R_L}}{2\sqrt{\frac{g_m}{R_{fb}C_{in}C_L}}}. \tag{5}$$

The step response is a strong function of the damping factor ζ. The best tradeoff between settling time and overshoot is obtained when a damping factor between 0.7 and 1 is used, which is equivalent to having a loop phase margin in the range of 65° to 76°. In this design, we selected a nominal $\zeta = 0.9$ for a peaking within 2% of the final value maintaining a safety range to accommodate phase margin degradation due to PVT variations between 65° and 76°.

For an underdamped system ($\zeta < 1$), the settling time is computed as follows [21]:

$$t_s = \frac{-\ln(\varepsilon\sqrt{1-\zeta^2})}{\zeta\omega_n}. \tag{6}$$

In this equation, ε and t_s are usually defined by system-level specifications, such as allowed settling error and clock frequency, respectively. Since ζ is set at 0.9 for the fastest settling time, the only design variable that needs to be calculated is the natural frequency ω_n

$$\omega_n = \frac{-f_s \ln(\varepsilon\sqrt{1-\zeta^2})}{\zeta}. \tag{7}$$

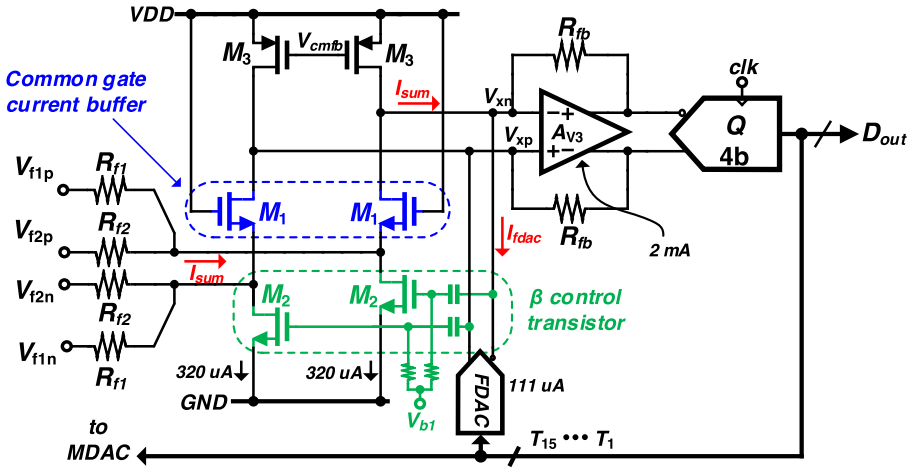

Fig. 8. Current buffer and ELD path implementation.

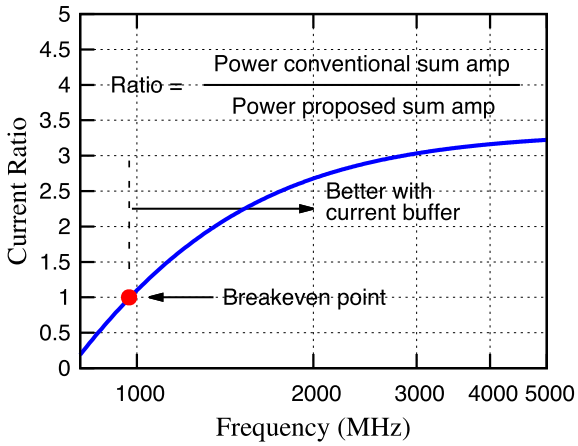

Fig. 9. Current ratio between conventional summing amp and proposed summing amp with current buffer.

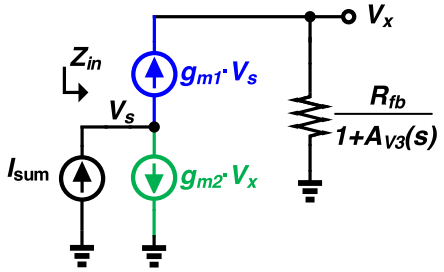

Fig. 10. Small-signal model, common gate buffer with bias transistor diode connected.

Once ω_n is found, the design component values can be calculated from (4) and (5). From these equations, some variables are fixed and can be estimated from some of the components in the design, i.e., C_L is mainly dominated by the parasitic capacitance at the input of the quantizer and layout trace parasitics, and C_{in} is dominated by the parasitic capacitance from the FDAC.

The following equation is obtained from (5):

$$\beta_{\text{optimal}} \cong \frac{1}{C_{\text{in}} R_{\text{fb}} \left(2\zeta\omega_n - \frac{1}{C_L R_L}\right)}. \tag{8}$$

This result shows that, in a second-order system, $\beta = 1$ is not necessarily the optimum value in terms of settling time for a step response. The optimal value of β is the one that optimizes loop response for the desired $\zeta = 0.9$ value; hence, the optimal value for $\beta = \beta_{\text{optimal}}$ can be plotted with respect to R_{fb} as shown in Fig. 5 (black line).

Also, from (4), the amplifier's transconductance can be obtained as

$$g_m \cong \omega_n^2 R_{\text{fb}} C_{\text{in}} C_L - \frac{1}{\beta_{\text{optimal}} R_L} + \frac{1}{R_{\text{fb}}}. \tag{9}$$

The required transconductance is a nonlinear function of R_{fb} as shown in Fig. 5 (blue line). A comparison of β and g_m values needed for the selected damping factor with respect to R_{fb} is shown. The parameter values were obtained from layout extraction, $C_L = 400$ fF, $C_{\text{in}} = 40$ fF, and $R_L = 5$ KΩ. As expected, the smaller the value for R_{fb}, the smaller the required g_m will be, and the closer to one the value of β is. If an ideal current buffer is considered, the ideally large output impedance will make $\beta = 1$, which will also require less transconductance. However, Fig. 5 shows that for the desired damping factor, R_{fb} is fixed to a small value. For a practical implementation, there is a limit on how small R_{fb} can be. A very small resistor value will produce excessive loading, not only on the summing amplifier OpAmp but also on the loop filter OpAmps since the FF coefficients are determined by the ratio of R_{fb} and $R_{f1,2}$. Also, a small value of R_{fb} will require a large current value for FDAC to recover a full-scale signal, which increases the modulator's power consumption and silicon area. Therefore, it is desired to have some control on the output impedance of the buffer to define R_{fb} and β_{optimal} to improve power efficiency and maintain the desired step response.

Fig. 5 also shows the value of g_m for the cases with and without buffer for selected step response in both cases. The reduction of transconductance needed is significant from 58 mA/V down to 16.8 mA/V. For the case without the current buffer, β is fixed by the FF coefficients which are defined by system level design specifications of the loop filter. Therefore, R_{fb} and g_m need to be adjusted accordingly to obtain the desired damping factor and maintain the desired step response. Without the buffer to maintain $\zeta = 0.9$, the required g_m is 58 mA/V and R_{fb} is in the range of 15 kΩ.

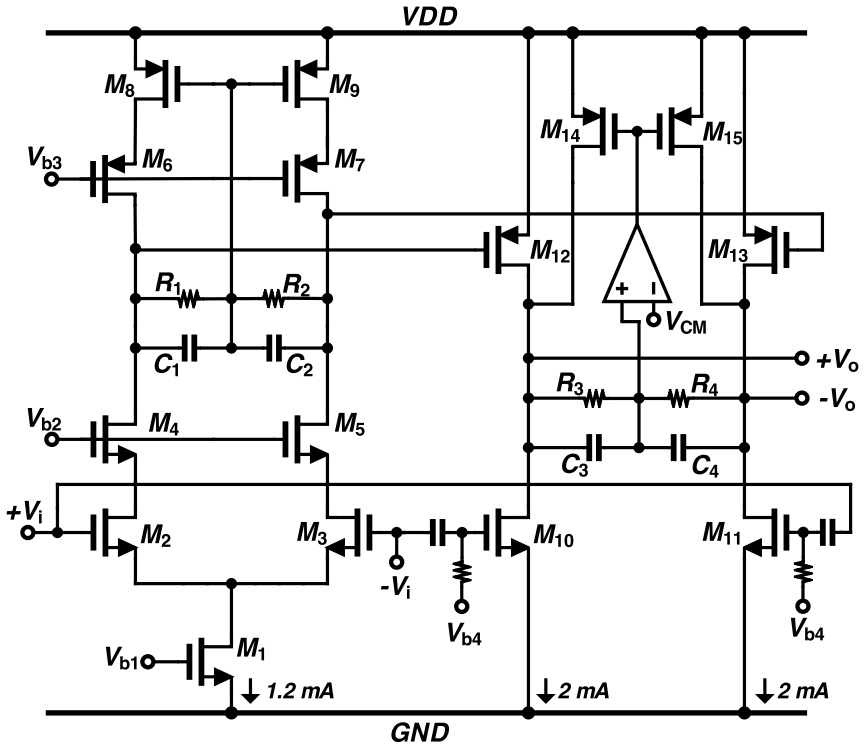

Fig. 11. Two-stage OpAmp used in the analog loop filter.

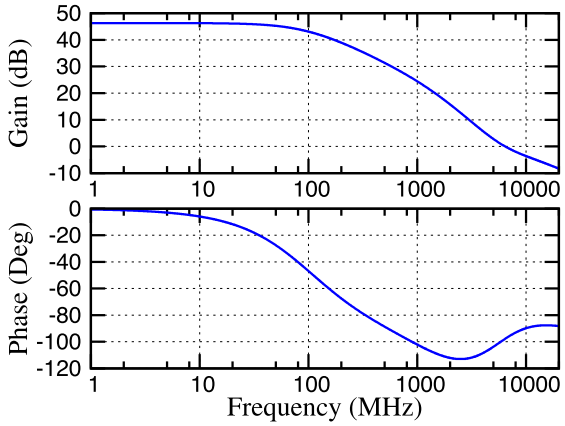

Fig. 12. Gain and phase response for the amplifier used in the first stage; A_{v1} in Fig. 1.

With the buffer implementation, the preferred $R_{\rm fb}$ was as small as possible to reduce current without affecting the design of other blocks. Also, β was adjusted accordingly by adjusting the output impedance of the buffer. The use of the proposed current buffer adds an extra degree of freedom since β can be adjusted independently of the FF coefficients. Since both equations are quadratic and inversely proportional, an increase in β will generate a significant reduction of g_m.

Fig. 6 shows the effect of $R_{\rm fb}$ on the FF resistors $R_{f1,2}$ and on the FDAC current. The selected $R_{\rm fb}$ value of 4500 Ω was chosen mainly to avoid having $R_{f1,2}$ values lower than 500 Ω, which can add loading to the loop filter OpAmps. Also, as is shown a smaller resistor will require more current from the FDAC this could increase the silicon area needed.

Section IV discusses the implementation and details on how to adjust the impedance looking back at the current

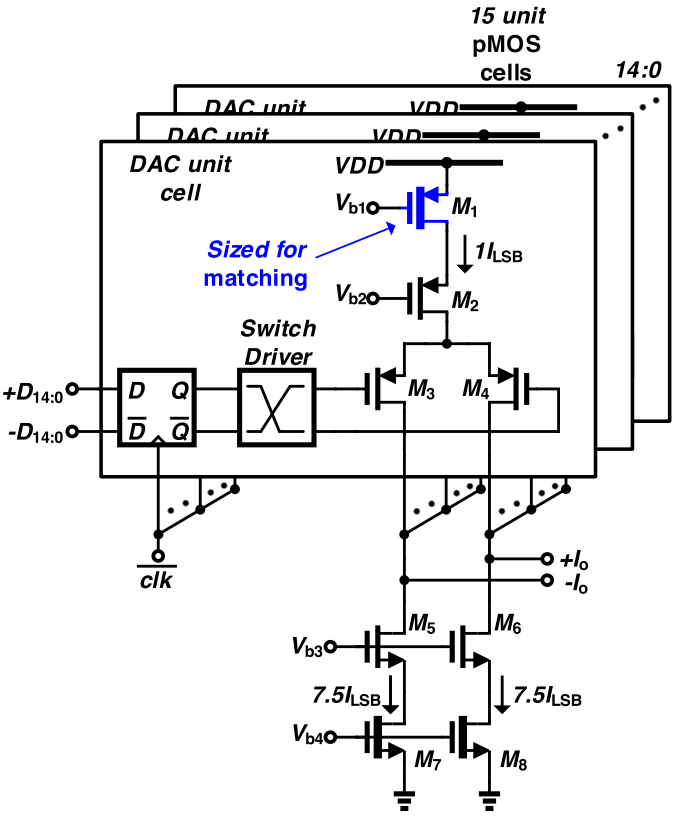

Fig. 13. Current steering MDAC and FDAC implementation.

buffer to control β. Fig. 7 shows the effect of β to a current step response for three different cases: 1) without the current buffer; 2) with a high output impedance buffer; and 3) with a controlled output impedance buffer. For all these cases, the transconductance gain was set at 16.8 mA/v and $R_{\rm fb}$

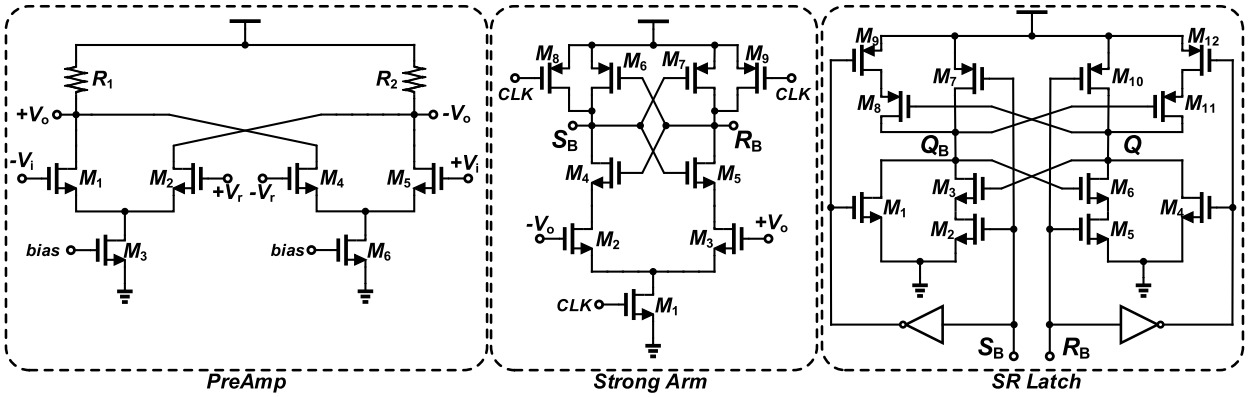

Fig. 14. 4-b quantizer building blocks.

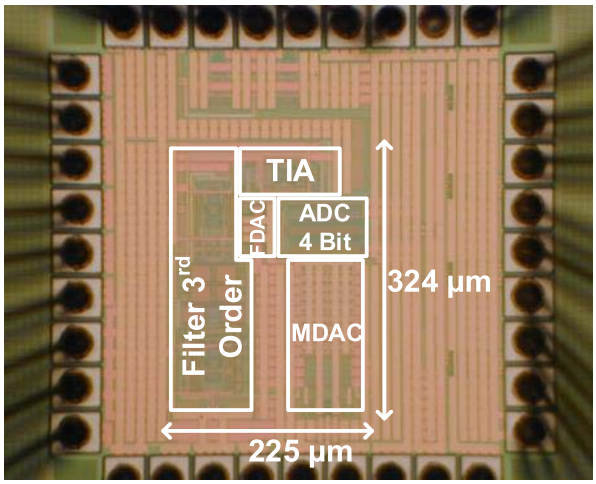

Fig. 15. Chip microphotograph.

was fixed. The dashed line indicates the available clock period; for proper operation, it was targeted 50% of the clock period for the OpAmp to settle, to allow the other 50% for quantizer and FDAC delays. $\beta = 1$ reduces the damping factor and degrades the phase margin, producing ringing that drastically affects its settling time. Without a buffer, the settling error is 30 %. With the buffer and adjusted β, the amplifier settles with less than a 3 % error.

IV. Circuit Implementation

A. Common Gate Current Buffer With Output Impedance Control

Fig. 8 shows the implementation of the current buffer ELD summing amplifier. The current buffer is implemented with a common gate (M_1) configuration. A_{v3} and $R_{\rm fb}$ implements the TIA that converts the current difference from the current buffer and FDAC to voltage, and drives the quantizer. Transistors M_2 and M_3 provide the bias current for the current buffer M_1. M_2 also controls the impedance looking back at the output of the current buffer; the gate of M_2 is ac coupled to the output of the current buffer. This connection creates an equivalent impedance at medium and high frequencies of $\sim 1/gm_2$, therefore, $R_{\rm buf} = 1/gm_2$. For the selected $R_{\rm fb} = 4500\ \Omega$ and the β value shown in Fig. 5 for the desired damping factor, the optimum output impedance from the buffer is $R_{\rm buf} = 1420\ \Omega$. Since M_2 was needed already to provide the bias current for M_1, no extra current was added for β control. Fig. 8 also shows the power consumption for each of the blocks. The bias current for the buffer is 640 μA, with 320 μA in each arm. The buffer's current consumption is small compared with the current saved in A_{v3}, which was reduced from 7.5 mA without the buffer down to 2.05 mA with the buffer. The differential pair transistors in A_{v3} are designed with a transconductance efficiency of $g_m/I_d = 16$ to make sure that the transistor have a small $V_{\rm dsat}$ for low voltage operation, but still operates in saturation region. In order to maintain M_1 in saturation, the common mode voltage from A_{v3} ($V_{\rm cm} = V_{\rm dd}/2 + 50$ mV) is above the midrail. The amplifiers from the filter A_{V1} and A_{V2} have a common mode below midrail ($V_{\rm dd}$/2–50 mV). Even though the common mode from the filter is reduced, it remains a bit higher than the voltage at the source of M_1, which is set by $V_{\rm dd}$–$V_{\rm gs1}$. Therefore, an small dc current flows through R_{f1} and R_{f2}, around 60 μA total. The increase of $V_{\rm cm}$ on A_{v3} also helps to relax the operation of the comparators in the quantizer. Moreover, the low voltage swing at the output of the filter OpAmps allows the reduction of $V_{\rm cm}$ without any penalty.

The current buffer reduces the power consumption of the summing amplifier but there are some characteristics that need to be consider. The current buffer increases system's thermal noise. However, since the buffer is located after the loop filter, the noise is shaped by loop gain. Also, the extra bias current used in the current buffer needs to be consider when comparing this topology with a conventional summing amp. Fig. 9 shows the ratio between the current of a conventional summing amp, and the current needed for the proposed summing amp with current buffer as function of frequency of operation. Equation (6) was used to compute current values; for the case of the summing amp with current buffer the dc current of the buffer is 640 μA. The resistor values used in this computation were exactly the same found in Fig. 5, only ω_n was adjusted to maintain similar step response. At the point in which the current ratio is one, the current required for both architectures is the same, with the specifications defined by this design, the breakeven point is located at 970 MHz; if the sampling frequency is around this frequency both architectures

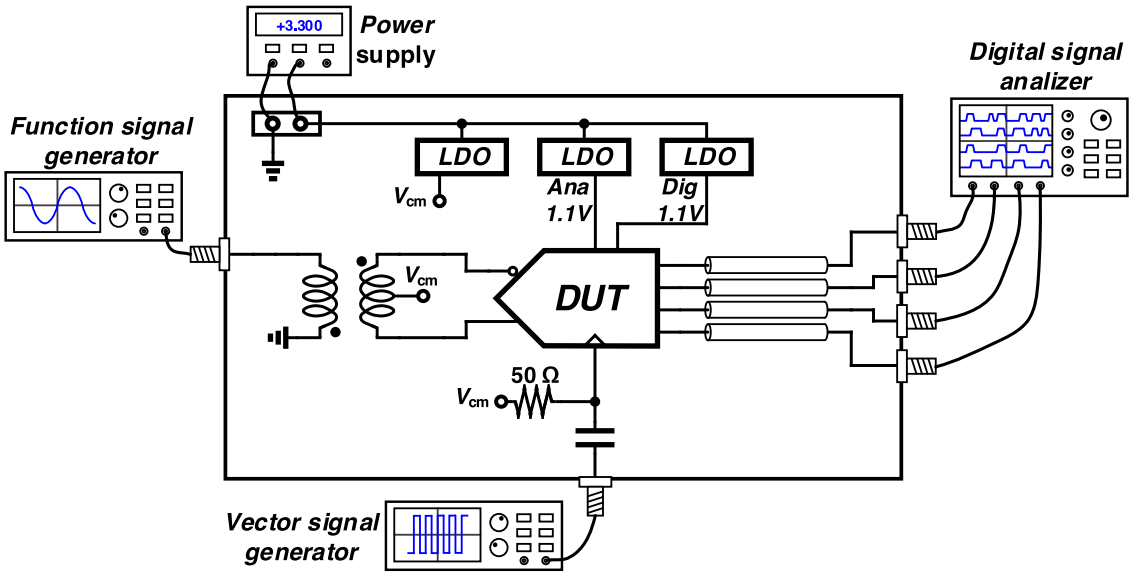

Fig. 16. ADC measurement setup.

will require the same bias current. Moreover, if the current ratio becomes larger than unity the proposed summing amp with current buffer is more power efficient. At 3.2 GHz, the proposed approach is three times more power efficient.

In terms of circuit sensitivity to PVT variations, the main issues are the variations of gm_2 and $R_{\rm fb}$ which define β and, therefore, the damping factor and transconductance as shown by (8) and (9). For gm_2, we can expect variations in the range of $\pm 10\%$, and for $R_{\rm fb}$, we expect variations in the range of $\pm 20\%$. However, simulation showed that the damping factor remained between 0.7–1 maintaining good system performance. Also, in case the ELD coefficient needs to be adjusted due to PVT variations for this prototype, external trimming of the bias current for FDAC is available.

B. Current Buffer Input Impedance

The accuracy of the FF coefficient values depends on the proper generation of a low impedance node at the source of M_1, e.g., $Z_{\rm in} \ll R_{f1}||R_{f2}$. M_2 generates a loop that decreases the impedance seen by the FF resistors. Fig. 10 shows the small signal for the input impedance of the used current buffer, including the effect of M_2. The small signal input impedance can be approximated as follows:

$$Z_{in} = \frac{V_s}{I_\Sigma} \approx \frac{1}{g_{m1}\left(1+g_{m2}\left(\frac{R_{fb}}{1+A_{v3}(s)}\right)\right)} \tag{10}$$

where $A_{v3} \cong (g_{m3} - 1/R_{\rm fb})(R_o||R_{\rm fb})$ is the gain of amplifier Av_3. As shown in (10), g_{m2} helps to reduce the input impedance of the buffer, and then improves the accuracy of the FF coefficients. If the feedback capacitors attached to the gate of M_2 are removed, the current buffer's high frequency input impedance is approximately $Z_{\rm in} \approx 1/g_{m1}$.

C. Analog Loop Filter Operational Amplifier

The filter's OpAmps were implemented employing a two-stage topology with FF frequency compensation for a high-frequency operation [20], with Fig. 11 showing the schematic. The input stage formed by M_{1-9} is a cascode architecture to provide high gain. The common mode feedback is self-biased using $R_{1,2}$; $C_{1,2}$ are used to ensure the CMFB loop stability. Transistors M_{12-13} implement the second stage, and transistors M_{10-11} implement the FF path with a pseudodifferential pair that reuses the current used in M_{12-13}. The input signal is ac-coupled to the gate of M_{10-11} to optimize the amplifier frequency response. Active common-mode feedback is used in the second stage to have better control of the output common mode level. The entire amplifier consumes a total of 5.9 mW, including the common-mode feedback.

The gain and phase responses of the amplifier are shown in Fig. 12, where the first OpAmp (A_{v1} in Fig. 1) provides a dc gain of 46 dB with a GBW of 7.8 GHz and a phase margin of 81°, the OpAmp is loaded with the next stage input load and the integrator capacitor. It was verified by simulation that the obtained gain is sufficient to reduce the noise from the backend circuits. The high frequency zero, due to the FF frequency compensation, is visible over 2 GHz, and it does not significantly affect amplifiers settling time. The second amplifier A_{v2} is a scaled version of the first one and consumes a total power of 1.9 mW.

D. Current Steering DAC

The 4-b main feedback DAC employs 15 cells of pMOS cascode current source $M_{1,2}$ and a pair of current-steering switches $M_{3,4}$, as shown in Fig. 13. Each current source cell $M_{1,2}$ is designed to carry a nominal current of 67 μA (1 $I_{\rm LSB}$). The current source device, M_1 was sized to achieve a device matching better than 0.5% (3σ); behavioral simulations show that these tolerances could reduce modulator's SNDR down to 64 dB for 5 of every 100 parts. For the case 1σ variations in DAC transistors, the harmonic distortion is still under -70 dB. If the same linearity wants to be maintained for a yield of 2σ or higher most likely some matching calibration methodologies would be required. Transistor M_2 was included to increase the output resistance of each cell and to decouple the large parasitic capacitor of M_1 from the current steering-

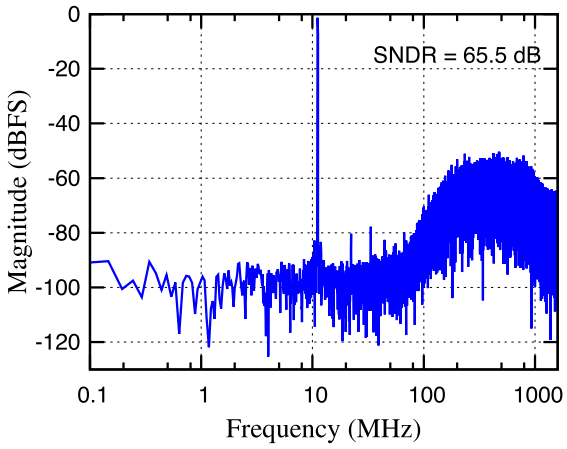

Fig. 17. Measured output spectrum with −1 dBFS input signal at 10.5 MHz; measured SNDR = 65.5 dB.

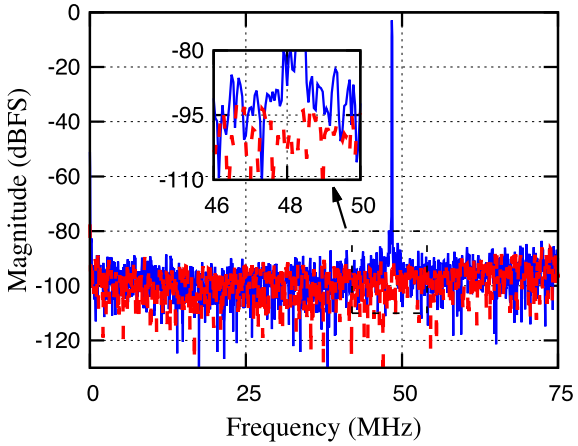

Fig. 18. Measured output spectrum with −1 dBFS at 48.5-MHz input signal versus no input signal.

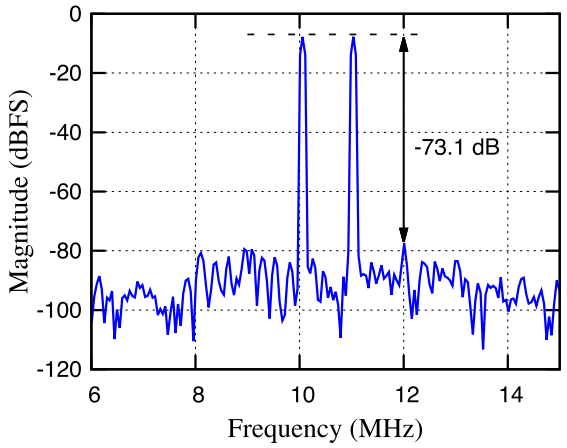

Fig. 19. Measured output spectrum with two tone test.

switches, $M_{3,4}$, for high-speed operation. A pair of nMOS cascade current sources $M_{5,7}$ and $M_{6,8}$ were each designed to carry a nominal current of 500 μA (7.5 I_{LSB}), which ensures an equal common-mode level between the CT$\Sigma\Delta$M's input and DAC's output. With 500 Ω of CT$\Sigma\Delta$M's input resistors, the equivalent CT$\Sigma\Delta$M's full-scale differential input range is 1 V_{pp}.

The current-steering switches, $M_{3,4}$, are designed to operate in saturation region to improve DAC output impedance.

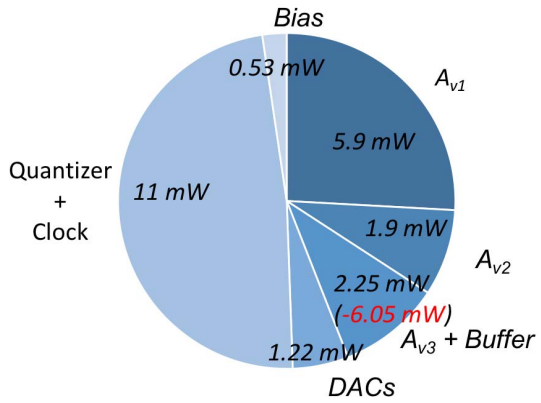

Fig. 20. Current consumption break down, including the current reduction on A_{v3} from 8.3 mW down to 2.25 mW.

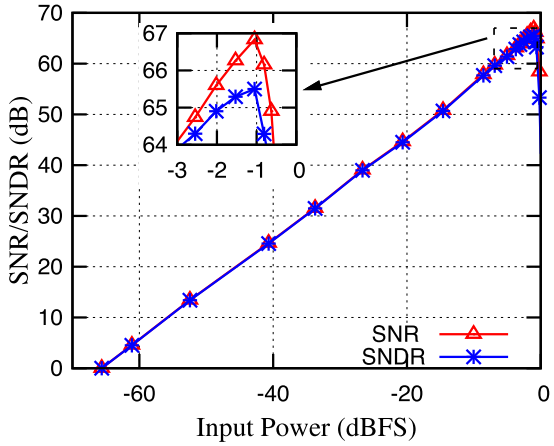

Fig. 21. SNR/SNDR versus input signal power.

In addition, these transistors are driven by a low-crossing switch driver [22] to ensure that none of them turns OFF completely during switching. This design choice minimizes feed-through current from parasitic gate to drain capacitances C_{gd} of $M_{3,4}$. FDAC is a scaled version of MDAC, where the individual cell currents and area were reduced by a factor of 9.

E. 4-b Quantizer

The 4-b quantizer incorporates a flash-type ADC running at a 3.2-GHz sampling frequency. The flash converter consists of 15 identical slices, as shown in Fig. 14. Each slice is composed of a preamplifier, a strong-arm comparator and an SR-Latch. The preamplifier compares the input to one of 15 differential reference levels generated by a resistive ladder. The value of the unit resistor is selected such that it minimizes the reference ripples to below one fourth of the LSB level. Kick-back noise from the sampling clock is further attenuated by the preamplifier, which provides isolation between the input and the sampling stage. The preamplifier input pair sizing is selected to minimize the effect of offset and the cross-connection of differential inputs and reference inputs is used to minimize common mode variations at the comparator input.

The comparator used here is a strong-arm latch [23], followed by a balanced SR-latch [24]. The comparator architecture is selected to achieve optimal delay-power tradeoff, where the comparator consists of one stage that performs both signal

TABLE I
RESULT SUMMARY AND COMPARISON TABLE

Publication	**This Work**	[2]	[4]	[3]	[6]	[9]	[8]
		JSSC11	ISSCC12	JSSC12	JSSC14	JSSC15	JSSC15
Architecture	**Single**	Single	Single	Single	MASH	Single	MASH
Process (nm)	**40**	45	45	65	28	20	28
Order	**3**	4	3	6	0-3	4	3-1
FS (GHz)	**3.2**	4	6	4	3.2	2.184	1.8
BW (MHz)	**75**	125	60	75	53.3	80	50
SNR(dB)	**66.8**	65.5	61.5	--	83.1	70	76.8
SNDR (dB)	**65.5**	65	60.6	--	71.4	67.5	74.9
VDD (V)	**1.1**	1.1/1.8	--	1.0/2.5	0.9/1.8/-1	--	--
Power (mW)	**22.8**	260	20	750	235	23	80.4
Area (mm^2)	**0.072**	0.9	0.49	5.5	0.9	0.1	0.34
FoM_1 (fJ/conv bit)	**98**	715	190	--	726	74.2*	177
FoM_2 (dB)	**163**	157	160	159	171.6	168	172.9
FoM_3 (dB)	**161**	152	155	--	155	163	171

*After off-line digital calibration
FoM_1=Power/(2·BW·$2^{(SNDR-1.76)/6.02}$)
FoM_2=DR+10·$\log_{10}$(BW/Power)
FoM_3=SNDR+10·$\log_{10}$(BW/Power)

amplification and latch regeneration. Since the quantizer is in the modulator's high-speed feedback path and is used to fulfill loop stability requirements, the signal delay through the quantizer needs to be less than 125 ps. Therefore, low-threshold transistors are employed in the design to achieve this delay requirement.

V. MEASUREMENT RESULTS

A prototype of the proposed CT$\Sigma\Delta$M was fabricated in a 40-nm LP8M process. The chip microphotograph is shown in Fig. 15. The chip active area is 0.072 mm^2. The modulator consumes 22.85 mW, including the digital power, with most of this power consumed by the input integrator (A_{v1} in Fig. 1) and the flash quantizer.

Fig. 16 shows the measurement setup. On-board low dropout regulators were used to generate a low-noise 1.1-V reference for the analog and digital blocks. The test input signal was generated from a Rohde&Schwarz SMB100A signal generator. Passive bandpass filters were used to minimize the noise contribution from the signal generator.

A low jitter 3.2-GHz differential clock signal was provided from Agilent N4965A. This instrument provides a low swing clock and an rms jitter of around 0.8 ps. The 4-b data comes out of the chip at the 3.2-GHz clock frequency. Transmission lines were carefully designed to ensure good data integrity. LVPECL output drivers were implemented on chip to drive the four channels of an Agilent DSA91304A digital signal analyzer with 40-GS/s maximum operation rate. The data channels were captured and postprocessed using MATLAB.

Fig. 17 shows the measured output spectrum of the modulator for a 10.5-MHz input signal with -1 dBFS input power. The measured SNDR over the 75-MHz BW was 65.5 dB, and the total harmonic distortion for a single tone test is under -76.3 dB. According to these results, the modulator's performance is limited by thermal and quantization noise with an SNR of 66.8 dB. The out-of-band noise shape is the result of an increase of the loop delay due to increased delay from the comparator and flip-flops in the quantizer.

Fig. 18 shows the modulator's performance for a higher frequency input; a 48.5 MHz with -1 dBFS input tone. The output power spectrum for an out-of-band very small input signal is shown as an overlaid in Fig. 18. The noise floor level is almost the same for both cases.

The linearity of the loop and MDAC was tested employing the two-tone test at 10 and 11 MHz, as shown in Fig. 19. Each tone magnitude was -7 dBFS, and the measured IM3 was –73.1 dB. If a higher resolution is required, it will demand more silicon area from MDAC to suppress the remainder nonlinearity or have to include a calibration scheme. Fig. 20 shows the current consumption for each building block; the current consumption on A_{v3} reduces from 8.3 mW of the conventional case down to 2.25 mW for the proposed architecture. Fig. 21 shows a comparison of the SNR and SNDR performances with respect to input signal power. As expected, since the system is limited by noise, the SNDR plot has a maximum degradation of less than 1 dB compared with the SNR plot. This plot includes the thermal noise contribution of the input signal that is not suppressed by the external bandpass filter.

Table I summarizes the performance of the fabricated chip and compares the results with recent state-of-the-art publications of CT$\Sigma\Delta$M's with BW $>$ 50 MHz. This paper presents the best Walden's figure of merit (FoM) (FoM_1) reported for uncalibrated broadband CT$\Sigma\Delta$M implementations without any off-chip data postprocessing. The FoM values are $FoM_1 =$ 98(fJ/conv bit), $FoM_2 = 163$ (dB), and $FoM_3 = 161$ (dB).

VI. CONCLUSION

In this paper, we have described a power-efficient CT$\Sigma\Delta$M. The proposed implementation of a fast-path ELD compensation circuit based on a low-power current buffer

can perform at gigahertz sampling frequencies. The implementation of the active fast path that provides gain allowed the reduction of analog power consumption from the loop filter then making the architecture more power efficient. The proposed summing amplifier with current buffer demonstrated that the realization of closed-loop amplifiers operating at gigahertz frequencies with low power consumption is feasible; the proposed approach can also be used in other architectures. The proposed architecture is very competitive when compared with previously reported state-of-the-art publications, and achieves the best power efficiency figure (Joules per conversion bit) for uncalibrated architectures for CT$\Sigma\Delta$M with BW $>$ 50 MHz.

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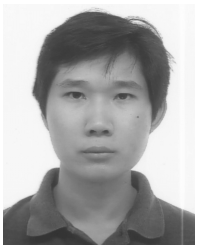

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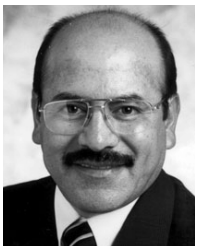

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