

Design and Self-Calibration Techniques for Inductor-Less Millimeter-Wave Frequency Dividers

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Abstract—This paper presents several design techniques to widen the operating frequency range and increase the locking range of dynamic current-mode latch-based inductor-less millimeter-wave frequency dividers. A self-calibration technique is introduced to guarantee frequency locking over a wide frequency range with low-input amplitude and over process, voltage, and temperature variations, thereby optimizing power consumption and ensuring robustness. Three divide-by-four prototypes incorporating the aforementioned techniques are designed to cover a frequency range exceeding 16–67 GHz. Fabricated in a 65-nm CMOS technology, the prototypes achieve min-average-max increases of 10%–47.5%–121.4% in fractional bandwidth over the state of the art. The first and third prototypes consume 3.7/6.2 mA (min/max) from a 1-V supply and achieve a figure of merit of 4.1/7.15 GHz/mW (min/max), while the second prototype consumes 3.9/6.7 mA (min/max) from a 1.1-V supply and achieves a figure of merit of 3/6.98 GHz/mW (min/max). The prototypes occupy the active areas of $11 \times 42/11 \times 53 \mu\text{m}^2$ (min/max). Finally, with the self-calibration scheme, the dividers operate with input power less than -10 dBm , supply voltage variation of $\pm 100 \text{ mV}$.

Index Terms—Current-mode logic, dynamic latch, frequency divider, inductor less, millimeter-wave (mm-wave) frequency synthesizer, ultra-wideband.

I. INTRODUCTION

THE millimeter-wave (mm-wave) frequency bands have gained wide acceptance in current applications, such as short-range wireless personal and local area networks, and automotive radar. The mm-wave standards are also being developed to serve new applications including cellular communication and wireless backhaul in several new bands including 28, 36, 45, 73, and 79 GHz. Frequency synthesizers with wide tuning range, high-resolution, low cost, and low power consumption are essential components in such applications [1]–[6], and are therefore of high current interest. In mm-wave transceivers, common approaches to local oscillator (LO) generation include fundamental frequency LO generation [7]–[10] and two or three times frequency multiplication [11], [12]. Also, automotive mm-wave radar transceivers typically use direct frequency modulation using fundamental frequency synthesizers [4].

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In all such transceivers, the high-speed frequency divider is a key constituent block that poses serious design challenges in terms of power/area consumption and operating range at mm-wave frequencies. Injection locked frequency dividers (ILFD) [13]–[16] can operate at high frequency with low power consumption, but suffer from large area, limited division ratio, and narrow locking range which is further reduced at higher division ratios [17], [18]. Current mode logic (CML) dividers [19]–[21] are another popular choice, but are very power hungry at mm-wave. The Miller divider [22], [23] is another candidate that can operate at high frequency with low power consumption, but suffers from smaller locking range compared to CML dividers. In [24], a new class of high speed inductor-less frequency dividers based on dynamic CML (DCML) latches [Fig. 1(a)] was introduced to achieve wide operating range and low power consumption with small die area. In [25] and [26], the load modulation technique was introduced into the DCML latches to improve their locking range and extend the minimum operating frequency (F_{\min}). However, both these dividers suffer from several shortcomings. First, the leakage (OFF-current) of the tail current source (M_{N1}) and finite OFF-resistances of the load transistors (M_{P1}, M_{P2}) significantly increase F_{\min} , thus degrading the locking range. Second, the operating frequency range ($F_{\max} - F_{\min}$) is extremely sensitive to parasitic capacitance and resistance, and to process, voltage, and temperature (PVT) variations. Third, the operating characteristic of the divider is divided into several narrow “sensitivity bands” [27, Fig. 8]; wideband operation is achieved by tuning the bias currents and the loads separately for each band. This adjustment is performed manually in [24] and [27], which is impractical in an mm-wave frequency synthesizer. Fourth, the sensitivity bands in the topology of [24] and [27] become narrower at lower input amplitudes that are typically produced by the LO buffer in a practical mm-wave synthesizer. Nonetheless, it is worth noting that the performance of this divider improves with technology scaling [26], [27].

This paper introduces several design techniques to increase the operating range under small input amplitude conditions, and demonstrates their effectiveness through three prototype topologies. In Section II, an accurate time-domain analysis of current DCML dividers [24], [27] is presented in order to elucidate their limitations. Based on these insights, several new design techniques are proposed and applied to three different topologies, as described in Section III. In the first topology, current bleeding and inter-latch source coupling are introduced

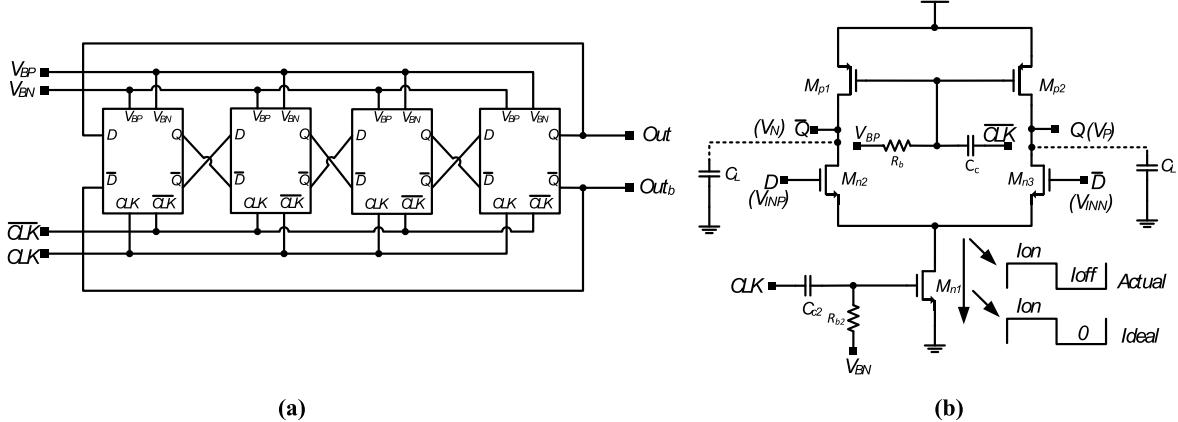


Fig. 1. (a) Schematic of divider-by-four circuit. (b) Schematic of the load modulated dynamic CML latch.

to increase F_{\max} and decrease F_{\min} . The second topology judiciously mixes devices with different threshold voltages to maximize the locking range. The third topology introduces bulk modulation of the tail transistor and adaptive bulk biasing of the load transistors to increase locking range and F_{\max} , respectively. Despite these improvements, several bands with individually optimized biases and loads are necessary to cover a wide frequency range. In order to address this issue, a calibration technique is introduced that automatically adjusts bias and load conditions, thereby enabling the divider to lock over an extremely wide frequency range while minimizing power consumption and enhancing robustness over PVT variations. This is described in Section IV. Characterization of the three 65-nm CMOS prototypes, presented in Section V, proves robust self-calibrated operation from 16 to 67 GHz with input amplitude as low as 100 mV (-10 dBm). Section VI compares the proposed divider topologies, and Section VII concludes this paper.

II. LIMITATIONS OF THE CONVENTIONAL INDUCTOR-LESS FREQUENCY DIVIDER

A. Effect of Leakage Current (I_{OFF}) and Finite OFF-Resistance (R_{OFF})

The load-modulated latch used in the DCML divider [26] is shown in Fig. 1(b). For a given input amplitude, the bias voltages of the tail current source (V_{BN}) and the PMOS loads (V_{BP}) determine the maximum injection current (I_{ON}) and the minimum ON-resistance (R_{ON}) of the PMOS loads, respectively. The baseline DCML divider using load-modulated latches was analyzed in [26] under the assumption that the tail current source and output PMOS transistors are completely turned OFF during the hold phase (i.e., $R_{OFF} = \infty$ and $I_{OFF} = 0$). In this section, we present a more accurate time-domain analysis including these effects that provides additional insights necessary to further enhance the operating frequency range.

Waveforms of a load-modulated latch in a locked DCML divider [Fig. 1(a)] at low-input frequency are shown in Fig. 2(a) by dotted lines for the ideal case, and by solid lines for the case with finite I_{OFF} and R_{OFF} . Each latch has two

read phases when the tail current source is on and the load capacitances (C_L) (dis)charge causing the outputs to change according to the input data; for the first and third latches in Fig. 1(a), the read phases are $(t_0 - t_1)$ and $(t_2 - t_3)$, during which CLK is high. During the read phases, assuming that the input differential voltage is sufficiently large to commutate the current in the differential pair completely, the differential output voltage ($V_P - V_N$) tends toward an amplitude $I_{ON}R_{ON}$ with time constant $R_{ON}C_L$. Each latch also has two hold phases, during which the tail current source and PMOS loads are turned OFF and the load capacitances maintain their output voltages; for the first and third latches, the hold phases are $(t_1 - t_2)$ and $(t_3 - t_4)$, during which CLK is low.

To ensure correct operation of the divider, the differential output voltage at the end of each read and hold phase should be higher than the voltage V_{SW} required to switch the following latch. In addition, to achieve lock at high frequency with a practically feasible input amplitude, the bias voltage V_{BN} should be set sufficiently high to increase the injection current during the read phases, while V_{BP} should be small enough to decrease the equivalent resistance of the load transistors. However, for a given input amplitude, this results in a significantly large I_{OFF} and low R_{OFF} during the hold phase, which in turn degrades (i.e., increases) F_{\min} . It can be observed from Fig. 2(a) that the output waveforms with finite I_{OFF} and R_{OFF} are similar to the ideal case during the read phases, albeit with different voltage levels. However, during the second hold phase ($t_3 - t_4$), when the inputs exchange states, the differential output voltage ($V_P - V_N$) decreases toward $-I_{OFF}R_{OFF}$ with time constant $R_{OFF}C_L$, thus leading to an increase in F_{\min} . An expression for F_{\min} can be derived with reference to Fig. 2(b), where the second hold phase (t_3, t_4) is divided into two regions: 1) the switching region (t_3, t_{3x}) during which $(V_{INP} - V_{INN})$ changes from $-V_{SW}$ to V_{SW} and output voltages (V_P, V_N) remain approximately constant and 2) the decaying region (t_{3x}, t_4) where the $(V_P - V_N)$ starts to decay toward $-I_{OFF}R_{OFF}$ instead of remaining at $I_{ON}R_{ON}$ as in the ideal case. F_{\min} can be expressed in terms of the switching time T_{SW} and the decaying time T_{decay} as $F_{\min} = 0.5/(T_{decay} + T_{SW})$; T_{SW} and T_{decay} can be found using first-order RC equivalent circuit analysis (see the Appendix).

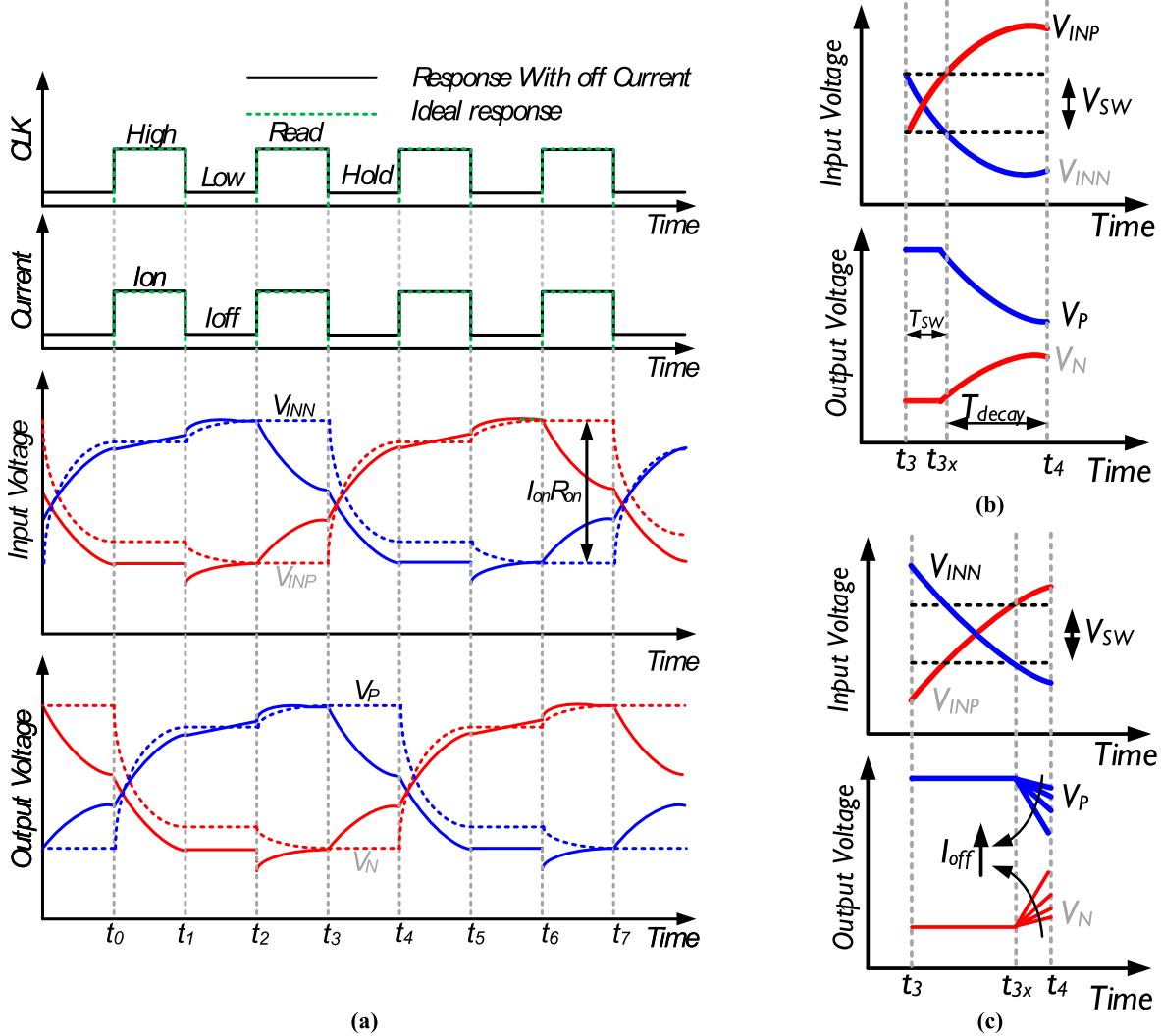


Fig. 2. (a) Timing diagram of DCML latch when embedded in divider by four: ideal response (dotted line), and with finite OFF-current (solid line). (b) Second holding phase in case of low-input frequency. (c) Second holding phase in case of high-input frequency.

Assuming that $T_{\text{decay}} \gg T_{\text{SW}}$ in case of low-input frequency, and that V_{SW} is between $0.25I_{\text{ON}}R_{\text{ON}}$ and $0.75I_{\text{ON}}R_{\text{ON}}$ [26] which are both realistic assumptions in the DCML latch, an approximate expression for F_{\min} can be written as follows:

$$F_{\min} = \frac{V_{\text{SW}} + I_{\text{OFF}}R_{\text{OFF}}}{2R_{\text{OFF}}C_L(I_{\text{ON}}R_{\text{ON}} - V_{\text{SW}})}. \quad (1)$$

Equation (1) reveals that F_{\min} increases approximately linearly with I_{OFF} of the tail current source.

Although I_{OFF} degrades F_{\min} , it improves the F_{\max} slightly. Fig. 2(c) plots the second hold phase in case of high-input frequency where the switching time is much longer than decaying time. It can be observed that for given R_{OFF} , higher I_{OFF} during the decaying period leads to smaller differential voltage at the end of second hold phase ($t_3 - t_4$). This, in turn, decreases the time required for differential output voltage to exceed V_{SW} during the next read phase ($t_4 - t_5$) which increases the F_{\max} . Neglecting I_{OFF} , a simple expression can be derived

for F_{\max}

$$F_{\max} = \frac{1}{2R_{\text{ON}}C_L \text{Cosh}^{-1} \left(\frac{I_{\text{ON}}R_{\text{ON}}}{I_{\text{ON}}R_{\text{ON}} - V_{\text{SW}}} \right)}. \quad (2)$$

Fig. 3(a) compares the analytical expression (1) against simulations of a divide-by-four using idealized DCML latches wherein PMOS loads were switched dynamically between explicit resistors R_{ON} (during read phase) and R_{OFF} (during hold phase), the tail current source was switched dynamically between ideal current sources I_{ON} (during read phase) and I_{OFF} (during hold phase), and actual transistors were used for input transistors (M_{n2} , M_{n3}). It can be observed that the maximum error between the analytical expression and the simulation is $\pm 7.1\%$. Fig. 3(b) plots the simulated F_{\min} and F_{\max} versus I_{OFF} , and highlights the significant effect of I_{OFF} on F_{\min} . The simulation also reveals a gradual increase in F_{\max} as I_{OFF} increases. In fact, an accurate, but complicated expression for F_{\max} can be derived including I_{OFF} , however, this is not presented here since it offers little insight compared to (2).

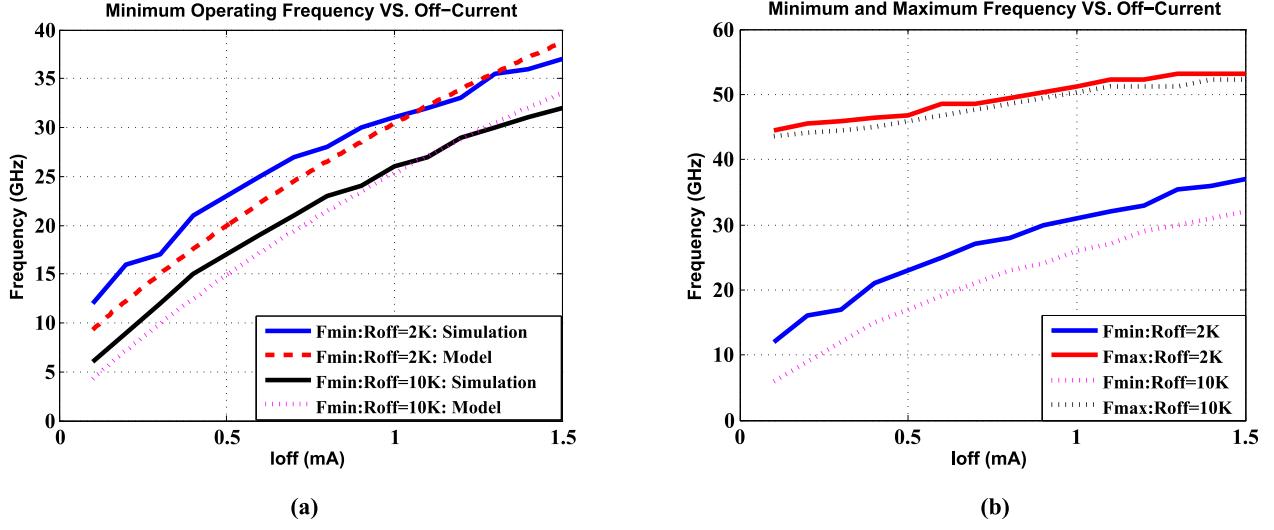


Fig. 3. (a) Comparison between analytical and simulated minimum operating frequency versus OFF-current. (b) Simulated maximum and minimum operating frequency versus OFF-current.

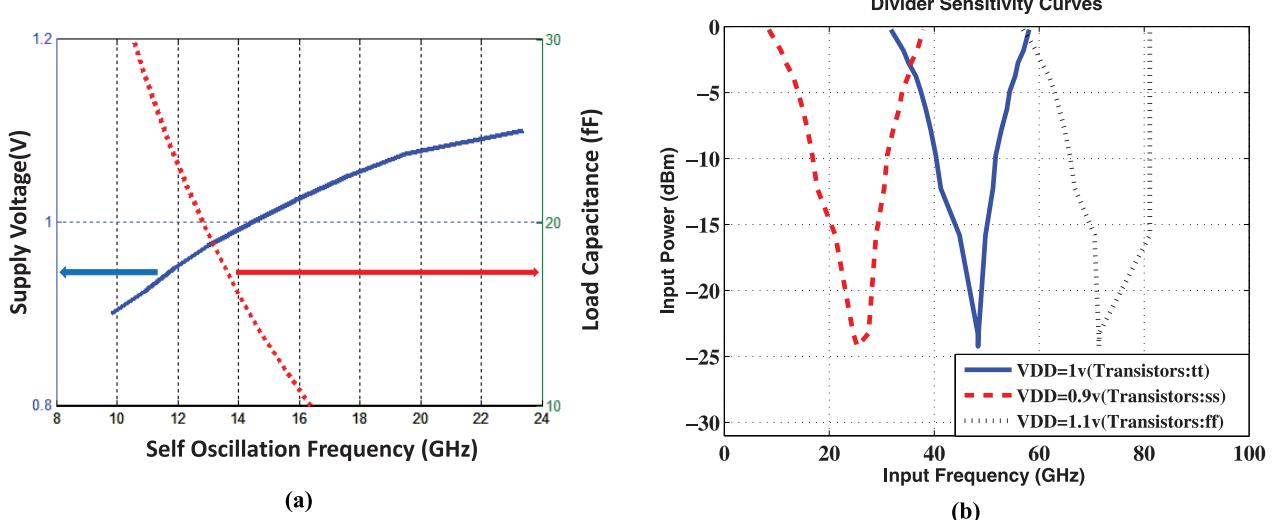


Fig. 4. (a) Self-oscillation frequency variation with supply voltage (solid line) and parasitic capacitance (dotted line). (b) Simulated sensitivity curve for different supply voltages and process corners.

B. Effect of PVT Variations

Equations (1) and (2) show that the operating range of the DCML divider is highly sensitive to the parasitic capacitance and resistance of the load transistors. The former is exacerbated from modeling/extraction uncertainties while the latter varies with supply voltage, threshold voltage and process parameters. Fig. 4(a) shows the simulated variation in self-oscillation frequency (F_{OSC}) of the DCML divider (Fig. 1) with supply voltage and load capacitance (C_L). The bias voltages of the tail current source (V_{BN}) and the PMOS loads (V_{BP}) are set to 650, and 325 mV, respectively. Load capacitance is swept with the supply voltage held at 1 V, and supply voltage is swept with an extra 15 fF (as an estimated of layout parasitic) added to the 43 fF intrinsic capacitance at the output nodes. It can be seen that variations as small as a few millivolts in supply voltage or a few femto-farads in C_L , cause shifts of several GHz in F_{OSC} . In addition, for given input amplitude, process and temperature variations affect the threshold voltage, which in turn causes variations in

the maximum injection current, the switching threshold V_{SW} of the differential pair, and equivalent resistance of output transistor. Fig. 4(b) shows that, according to simulations, the sensitivity curve can shift by more than 25 GHz over process and typical supply voltage variations (100 mV). This underscores the need for automatic calibration. Furthermore, it is seen that the operating range becomes narrower at higher V_{DD} and at the fast-fast corner; this is due to: 1) higher I_{OFF} of the tail current source and load transistors which increase F_{min} and 2) higher V_{OV} of the differential pair which limits F_{max} . Moreover, PVT and mismatch variations degrade the input duty cycle which in turn degrades both F_{max} and F_{min} due to decrease the available time for the read or hold phases.

III. PROPOSED WIDE LOCKING RANGE FREQUENCY DIVIDER TOPOLOGIES

A. First Topology DIVI: Current Bleeding and Source Coupling

Fig. 5(a) shows the schematic of the DCML divide-by-four circuit employing source coupled DCML latches, each

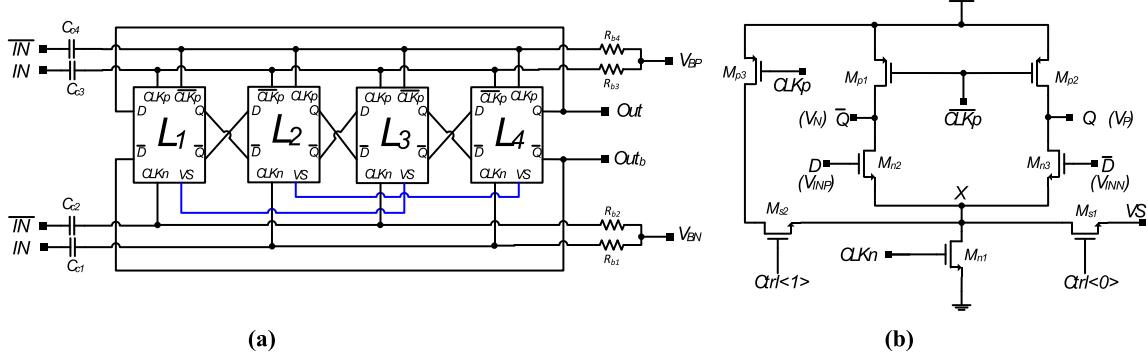


Fig. 5. (a) DCML divider using source coupling and current bleeding. (b) Latch schematic: the configurations DIV1-0, DIV1-SC, DIV1-CB, and DIV1-SC+CB can be realized by turning on the switches \$MS1\$ or \$MS2\$.

incorporating current bleeding. The input signals (\$IN, \overline{IN}\$) are ac coupled to the latch cores via common \$RC\$ networks with appropriate bias levels \$V_{BN}\$ and \$V_{BP}\$. The modified DCML latch [Fig. 5(b)] can be configured in one of four modes: 1) baseline mode (DIV1-0) with both \$MS1\$ and \$MS2\$ off; 2) source-coupled mode (DIV1-SC) with \$MS1\$ on and \$MS2\$ off; 3) current bleeding mode (DIV1-CB) with \$MS1\$ off and \$MS2\$ on; and 4) combined current bleeding and source coupled mode (DIV1-CB+SC) with both \$MS1\$ and \$MS2\$ on. The baseline DIV1-0 latch and the resulting divider provide a reference to compare the proposed dividers in the same technology node. DIV1-0 has been designed to maximize locking range for a given power consumption; the methodology described in [26] and [27] is used to size the output loads, tail current source, and input differential pair.

As noted in the Section II, the time required for the differential output voltage to exceed \$V_{SW}\$ during the read phase (\$t_0 - t_1\$) should be reduced in order to increase the operating frequency. This can be done by increasing the injection current (\$I_{ON}\$), but in order to do so without increasing the overall current consumption, the sources of the differential pairs of alternate latches driven by the same clock (i.e., \$L_1 - L_3\$ and \$L_2 - L_4\$) are coupled as shown in Fig. 5(a). The operation of this technique can be understood by examining the idealized waveforms of latch \$L_3\$ during \$L'_3\$'s critical read phase (\$t_0 - t_1\$), as shown in Fig. 6(a). During this period, \$L_1\$ is in its non-critical read phase, while \$L_2\$ and \$L_4\$ are in their hold phases. In essence, source coupling results in using a fraction of the tail current of \$L_1\$ to provide the injection current in \$L_3\$ during \$L'_3\$'s critical read phase (\$t_0 - t_1\$). This is achieved at the expense of less injection current in \$L_3\$ during its non-critical read phase (\$t_2 - t_3\$).

Conceptually, there are two reasons why source coupling increases injection current and therefore \$F_{max}\$, as described next. To understand the first reason, refer to Fig. 6(b) which shows the input pairs and voltages of \$L_1\$ and \$L_3\$ during \$(t_0 - t_1)\$ before the instant \$t_s\$ when the outputs of \$L_3\$ switch states. Before the instant \$t_s\$, the differential input voltage of \$L_1\$ (\$V_{IN1}\$) is higher than the differential input voltage of \$L_3\$ (\$V_{IN3}\$). Therefore, in the baseline divider where the sources are not coupled, the voltage at node \$X_{L1}\$ is higher than that at node \$X_{L3}\$. Hence, the injection current in \$L_1\$ is higher than that in \$L_3\$. However, this simply increases power consumption without increasing

\$F_{max}\$ since \$L_1\$ is in its *non-critical* read phase while \$L_3\$ is in its *critical* read phase. On the other hand, in DIV1-SC where the source nodes \$X_{L1}\$ and \$X_{L3}\$ are coupled to each other, the voltage at the coupled node attains a level between the levels of \$X_{L1}\$ and \$X_{L3}\$ in the un-coupled case. Therefore, for the same power consumption, higher injection current is available to \$L_3\$ compared to the baseline case. This, in turn, increases \$F_{max}\$.

To understand the second reason, refer to Fig. 6(c) which shows the input pairs and voltages of \$L_2\$ and \$L_4\$ during \$(t_0 - t_1)\$ before the instant \$t_s\$ when the outputs of \$L_3\$ switch states. The latches \$L_2\$ and \$L_4\$ are in their hold phases during this interval. Due to the non-zero tail current, the differential output of \$L_2\$ increases during \$(t_0 - t_1)\$, whereas the differential outputs of \$L_4\$ decrease slowly since its inputs—\$L'_3\$'s outputs—are switching states. Before switching instant \$t_s\$, the differential input voltage of \$L_4\$ (\$V_{IN4}\$) is higher than differential input voltage of \$L_2\$ (\$V_{IN2}\$). Therefore, in the baseline divider, node \$X_{L4}\$ is at a higher voltage than \$X_{L2}\$. When \$X_{L2}\$ and \$X_{L4}\$ are coupled as in DIV1-SC, the voltage at the coupled node is lower than the voltage at \$X_{L4}\$ in the baseline divider. Therefore, the average current flowing into \$L_4\$ (which is in its second hold phase) during \$(t_0 - t_1)\$ is lower than the baseline case, while the average current flowing into \$L_2\$ (which is in its first hold phase) is higher than the baseline case. Therefore, the differential output of \$L_2\$ (differential input of \$L_3\$) increases faster than in the baseline case, which increases the source voltage of input pairs of \$L_3\$. This, in turn, leads to higher injection current in \$L_3\$ due to channel length modulation of the tail transistor in \$L_3\$. The insights gained above are verified by simulation. Fig. 7(a) compares the rms on-current \$I_{L3}\$ during first and second read phases of DIV1-0 and DIV1-SC when the tail current source is biased at 600 mV and driven by 66-GHz signal. As predicted by the above analysis, the source coupled case achieves higher injection current in the critical read phase, and lower injection current in the non-critical read phase, thereby leading to an increase in \$F_{max}\$ without increasing overall power consumption.

The source coupling technique nonetheless suffers from a drawback for low-input frequency. Due to faster switching in the first read phase, the differential output voltage at the end of this phase is higher in DIV1-SC than in DIV1-0, as shown in Fig. 6(a). Since this is the second hold phase of

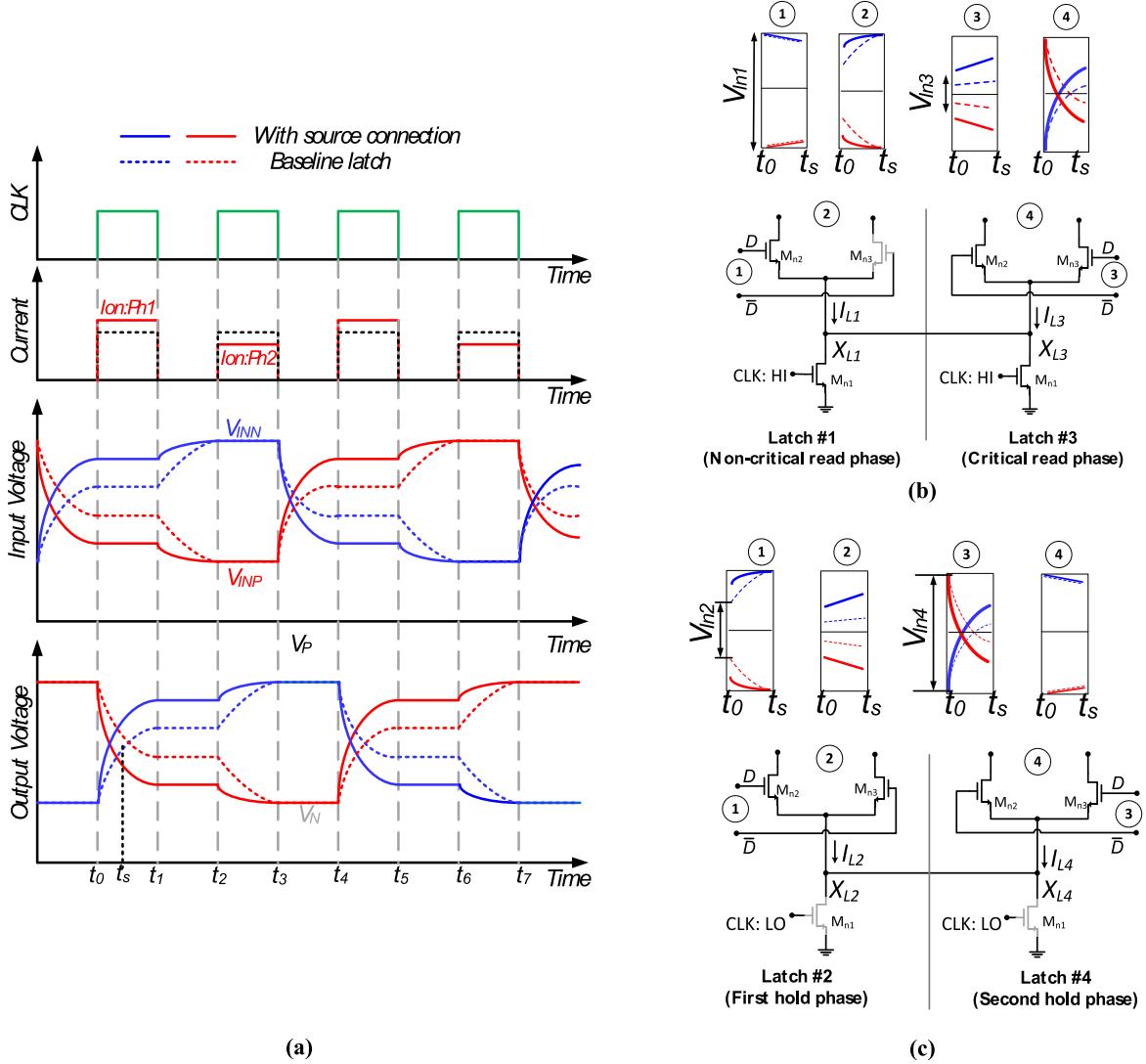


Fig. 6. (a) Timing diagram of DCML latch (L3) when embedded in divider by 4: ideal response with $R_{OFF} = \infty$ and $I_{OFF} = 0$ (dotted line) for the baseline divider, and with source connection (solid line). (b) L1 and L3 during first read phase. (c) L2 and L4 during first read phase. In (b) and (c), all bounding boxes for the waveforms represent the same scale.

the following latch (L_4 in this discussion), it exacerbates the effect of I_{OFF} for the following latch (Fig. 2). However, as discussed in the previous paragraph, the OFF-current that flows through the source of the input pairs of any latch in DIV1-SC (i.e., L_4 in this discussion) decreases during the second hold phase; this partially alleviates the impact of source coupling on F_{min} . The combined effect of these two effects is a small increase in F_{min} in DIV1-SC.

In order to extend downward the operating frequency range, a current bleeding transistor M_{P3} is introduced next (DIV1-CB). During the read phase, with CLK_n low and CLK_p high, M_{P3} is turned OFF and the latch operates as before. During the hold phase, M_{P3} is turned on and absorbs most of I_{OFF} . This helps maintain the correct output state, thereby decreasing F_{min} . The size of M_{P3} has an important effect on the operating frequency range. Increasing the size of M_{P3} helps to absorb a larger I_{OFF} which enhances F_{min} . However, this increases leakage current through M_{P3} during the read phase and adds capacitance at the source of the input pair, which absorbs a part of the injection current during the read

phase. Post-layout simulations of DIV1-CB conducted with different sizes for M_{P3} resulted in an optimum device size of 4 $\mu\text{m}/60\text{ nm}$ transistor.

In order to improve both F_{max} and F_{min} , source coupling and current bleeding were combined, resulting in DIV1-CB+SC. Fig. 7(b) compares the simulated average rms current flowing in the input pair during the hold phases of the four DIV1 configurations. It can be observed that the current bleeding technique reduces I_{OFF} significantly and this reduction increases with increasing input amplitude. This in turn decreases F_{min} . For example, examination of Fig. 7(b) together with Fig. 3(a) reveals that at 100-mV input amplitude, current bleeding decreases I_{OFF} from 1.22 mA to 800 μA , resulting in a decrease in F_{min} of more than 8 GHz.

B. Second Topology (DIV2): Mixed V_t Design

The second proposed latch topology, shown in Fig. 8, uses devices with different threshold voltages. Low- V_t (LVT) devices are used in: 1) the tail current source to increase the

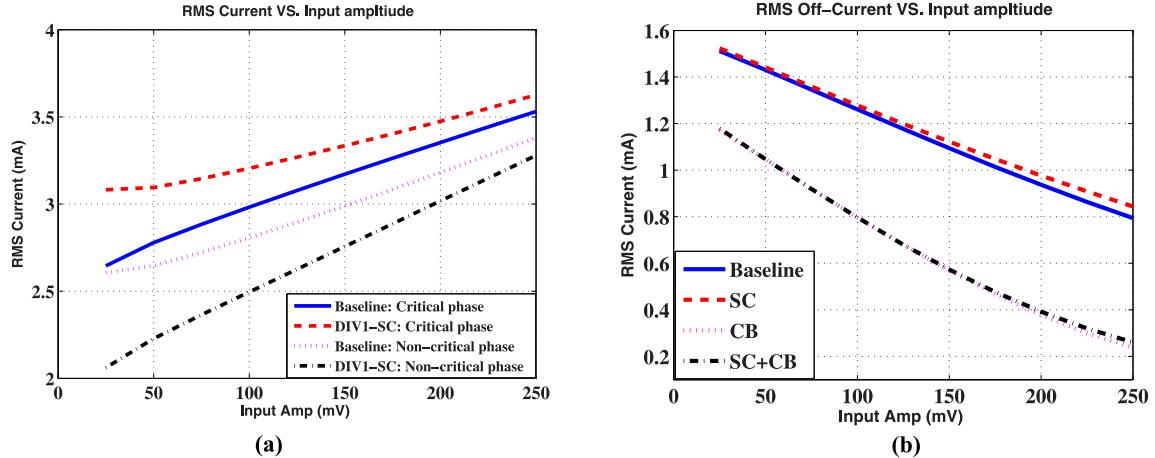


Fig. 7. (a) Comparison between rms ON-current of DCML latch without and with source connection. (b) Comparison between rms OFF-current of first architecture in all possible configurations.

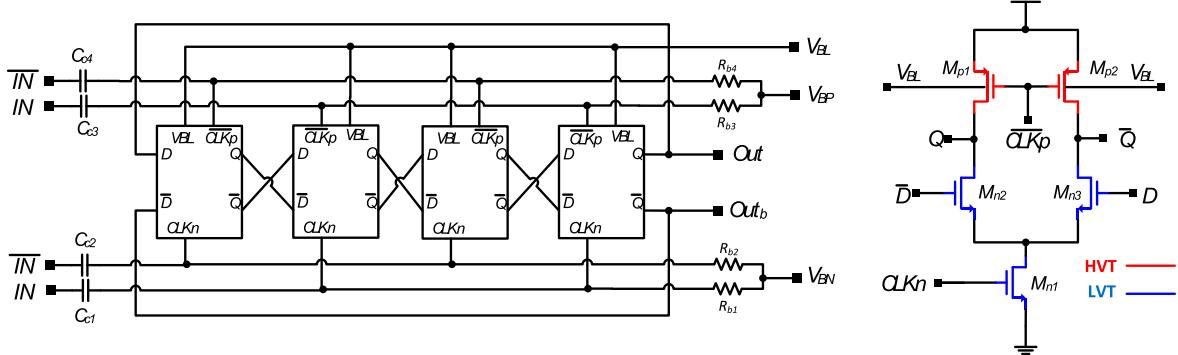


Fig. 8. Second architecture of DCML divider based on HVT and LVT devices.

injection current and 2) the input differential pair to commutate current completely faster than regular- V_t (RVT) devices. From (2), this increases F_{\max} for a given input amplitude and input capacitance. In a mm-wave divider, the bias voltage V_{BP} of the PMOS loads is usually made small (e.g., <300 mV) to decrease the load time constant. However, for practical input amplitudes, the PMOS loads do not turn completely OFF resulting in a relatively small equivalent resistance during the hold phase. This degrades F_{\min} and results in narrow locking range. To mitigate this degradation, high- V_t (HVT) devices are used for the PMOS loads. Fig. 9 compares simulated OFF and ON resistances of different V_t devices versus gate voltage; the OFF and ON resistances are calculated with V_{DS} of 1 V and 150 mV, respectively. For the same gate voltage, it can be seen that the OFF resistance of HVT devices is much higher, at the expense of slightly higher on resistance. Thus, using HVT loads, F_{\min} decreases significantly while F_{\max} decreases slightly. To compensate the degradation in F_{\max} , higher injection current or higher supply voltage can be used at the expense of power consumption. Alternatively, as shown in Fig. 8, PMOS bulk adaptation (V_{BL}) is proposed to change the effective R_{ON} and R_{OFF} of the PMOS loads. Fig. 10 compares the simulated OFF and ON resistances of different V_t devices versus their bulk voltage. The OFF and

ON resistances are calculated with ($V_{SD} = 1$ V and $V_{GS} = 0$) and ($V_{DS} = 150$ mV and $V_{GS} = 1$ V), respectively. Clearly, decreasing the bulk voltage slightly results in smaller R_{ON} of HVT device which in turn increases F_{\max} . For example, in order to have the same F_{\max} (i.e., R_{ON}) using RVT device with bulk voltage (V_{BLR}) of 1.1 V, the bulk voltage of HVT transistors (V_{BLH}) should be connected to 0.7 V.

It can be seen from (1) and (2) that the ratio F_{\max}/F_{\min} is proportional to the ratio by R_{OFF}/R_{ON} of the PMOS loads [26]. Fig. 11(a) compares R_{OFF}/R_{ON} of different V_t devices versus their bulk voltages. It can be seen that HVT devices have higher R_{OFF}/R_{ON} ratio for the same F_{\max} . For example, with $V_{BLR} = 1.1$ V and $V_{BLH} = 0.7$ V, the R_{OFF}/R_{ON} of a HVT device is 1.27 times that of an RVT device, which results in wider locking range. Figs. 10 and 11(a) show that, for a divider with any of the aforementioned latch topologies and for given power budget, bulk biasing can be used to increase F_{\max} at the expense of narrower locking range, or to widen the locking range for lower operating frequencies.

C. Third Topology (DIV3): Bulk Modulation and Bulk Control

As discussed in Section III.B, for a given tail transistor size and bias, using an LVT device increases F_{\max} . On other hand,

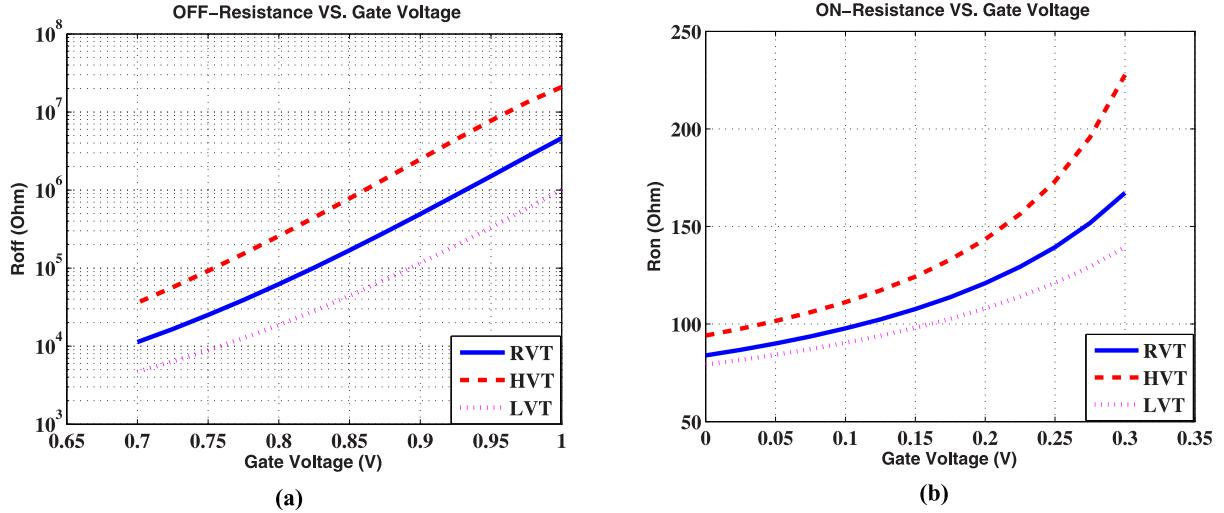


Fig. 9. Comparison between (a) OFF- and (b) ON-resistances versus gate voltage for different PMOS devices: RVT (solid line), HVT (dashed line), and LVT (dotted line).

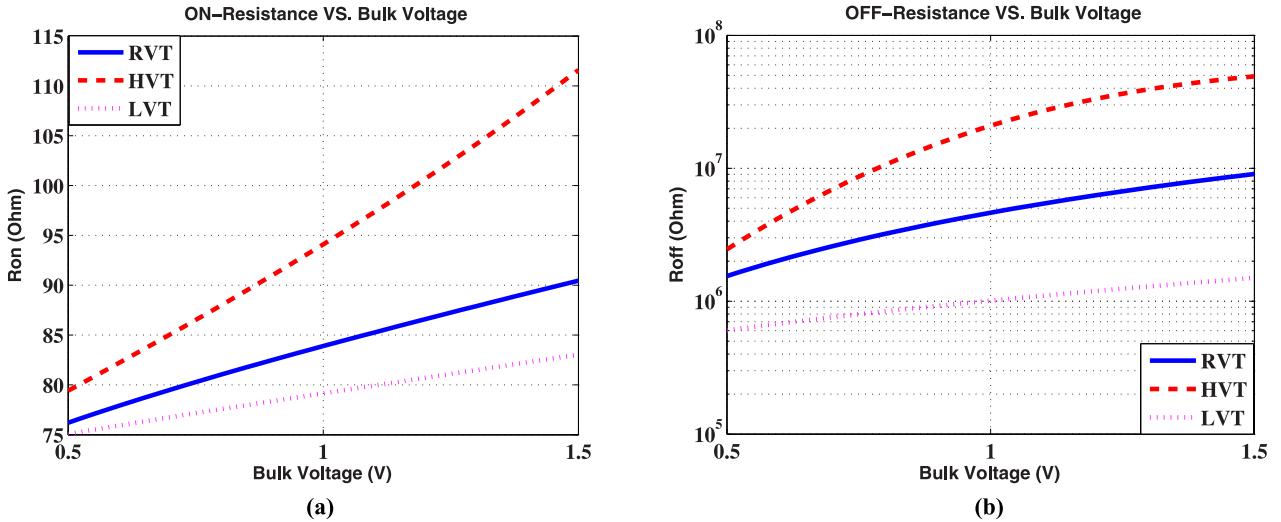


Fig. 10. Comparison between (a) ON- and (b) OFF-resistances versus bulk voltage for different PMOS devices: RVT (solid line), HVT (dashed line), and LVT (dotted line).

F_{\min} also increases due to large leakage current during the hold phase. To overcome this tradeoff, bulk modulation is introduced in the tail current source, as shown in Fig. 12. Here, the clock is applied to the bulk of the tail transistor with a bias voltage V_{BLn} , which is different from the gate bias V_{BN} , as shown in Fig. 12(c). During the read phase, with CLK_n high, the bulk voltage of tail current increases which decreases the threshold voltage and in turn increases the maximum injection current. During the hold phase, with CLK_n low, threshold voltage increases, thus reducing the minimum leakage current. The post-layout simulated threshold voltage variation was found to be -200 mV/V.

The bulk modulation technique improves both F_{\min} and F_{\max} . Fig. 11(b) compares the average ON and OFF current of the tail current source ($10 \mu\text{m}/60 \text{ nm}$), biased in saturation, with and without bulk modulation when it is driven by 40-GHz clock. For example, as shown in Fig. 11(b), with 150-mV input amplitude, bulk modulation increases the average I_{ON} from 3.23 to 3.79 mA, and decreases the average

I_{OFF} from 690 to $495 \mu\text{A}$. From (1) and (2), this improves F_{\max} and F_{\min} by 8 and 4.2 GHz, respectively. Note that the average power consumption of the divider with and without bulk modulation is approximately the same. Additionally, the designed DIV3 incorporates bulk control (V_{BL}) of the PMOS loads, as discussed in the Section III.B.

IV. SELF-CALIBRATION AND CURRENT MINIMIZATION

Despite the enhancement achieved by the aforementioned techniques in the frequency range covered by each sensitivity band, setting an appropriate bias current and load bias voltage is necessary to enable ultra-wideband coverage. Moreover, as discussed in Section II, the operating frequency and locking ranges of all proposed divider topologies are extremely sensitive to PVT variations which necessitate different optimal bias settings depending on PVT conditions. These challenges are exacerbated when the input amplitude to the divider is small; in practice, this amplitude—produced by a voltage-controlled oscillator buffer—will also vary with PVT. In order

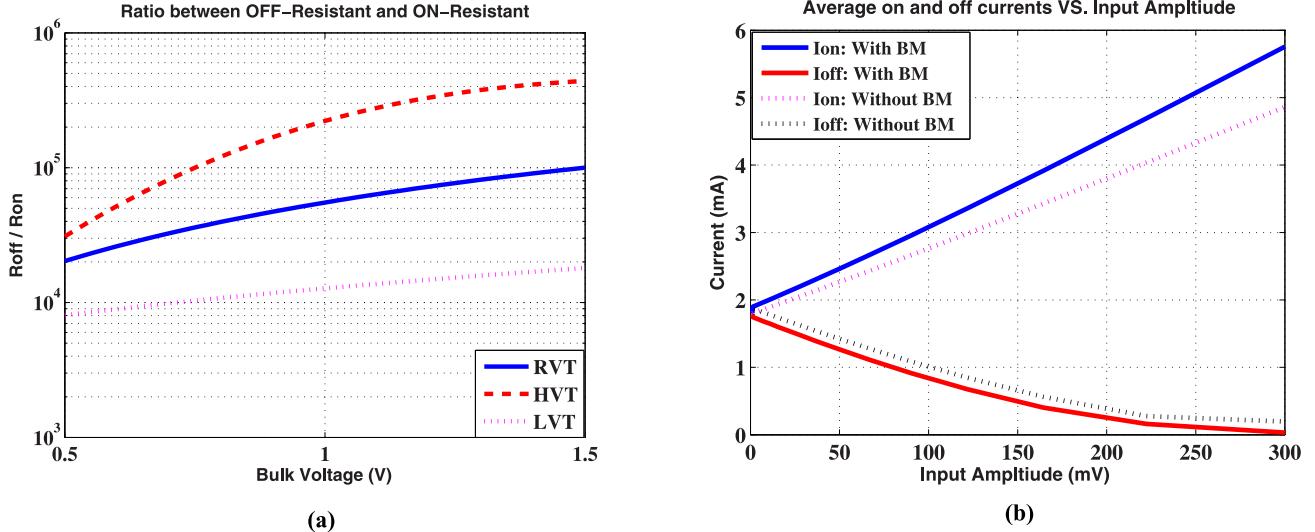


Fig. 11. (a) Ratio between OFF- and ON-resistances versus bulk voltage for different PMOS devices: RVT (solid line), HVT (dashed line), and LVT (dotted line). (b) Comparison between average ON-current and OFF-current of tail current source with BM (solid line) and without BM (dotted line).

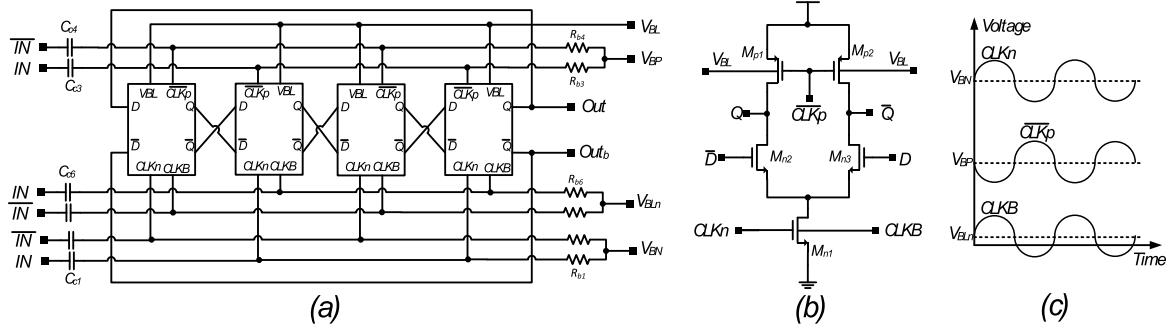


Fig. 12. (a) Third topology (DIV3) of DCML divider based on bulk modulation. (b) Schematic of latch. (c) Input waveforms of one of the latches

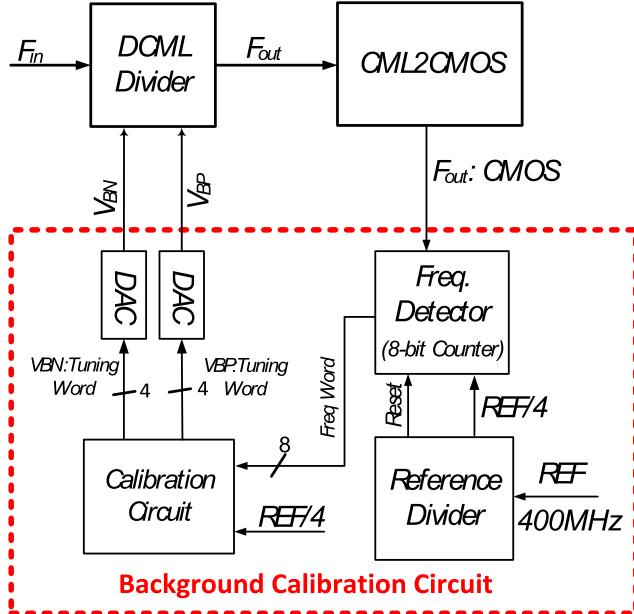


Fig. 13. Block diagram of proposed background calibration engine.

to facilitate practical applicability of the divider in a wide variety of usage scenarios, a self-calibration scheme that sets optimal bias conditions regardless of input frequency and

PVT conditions is proposed in this section. The calibration circuit, shown in Fig. 13, implements two algorithms—frequency calibration and current minimization, and comprises a high-speed frequency detector, reference frequency divider, resistive Digital to analog converters (DAC's), and a fully synthesized digital controller. Frequency detection is realized using an 8-bit synchronous counter which generates an 8-bit digital word representing the ratio of the divider output frequency and the reference frequency (F_{Ref}). Fig. 14(a) and (b) shows the implementation of the 8-bit counter and its timing diagram, respectively. The 8-bit high-speed counter is based on a binary ripple carry incrementer. The incrementer is split to two smaller incrementers (mod-4 and mod-64) to achieve sufficient timing margin over PVT variations [28]. The first incrementer generates the trigger of the higher incrementer once its count reaches “10” as shown in truth table (Fig. 14) to add extra timing margin [28] for counter's critical path (i.e., gating logic in Fig. 14). The True Single-Phase Clock flip-flops in the counter are periodically reset by a signal generated by the reference divider, which also generates the reference signal F_{Ref} for the counter from a 400-MHz source. The counter outputs are sampled by retimed version of F_{Ref} as shown in Fig. 14. The frequency detector has been verified to function robustly up to an input frequency of 18 GHz over all PVT corners. The high-speed

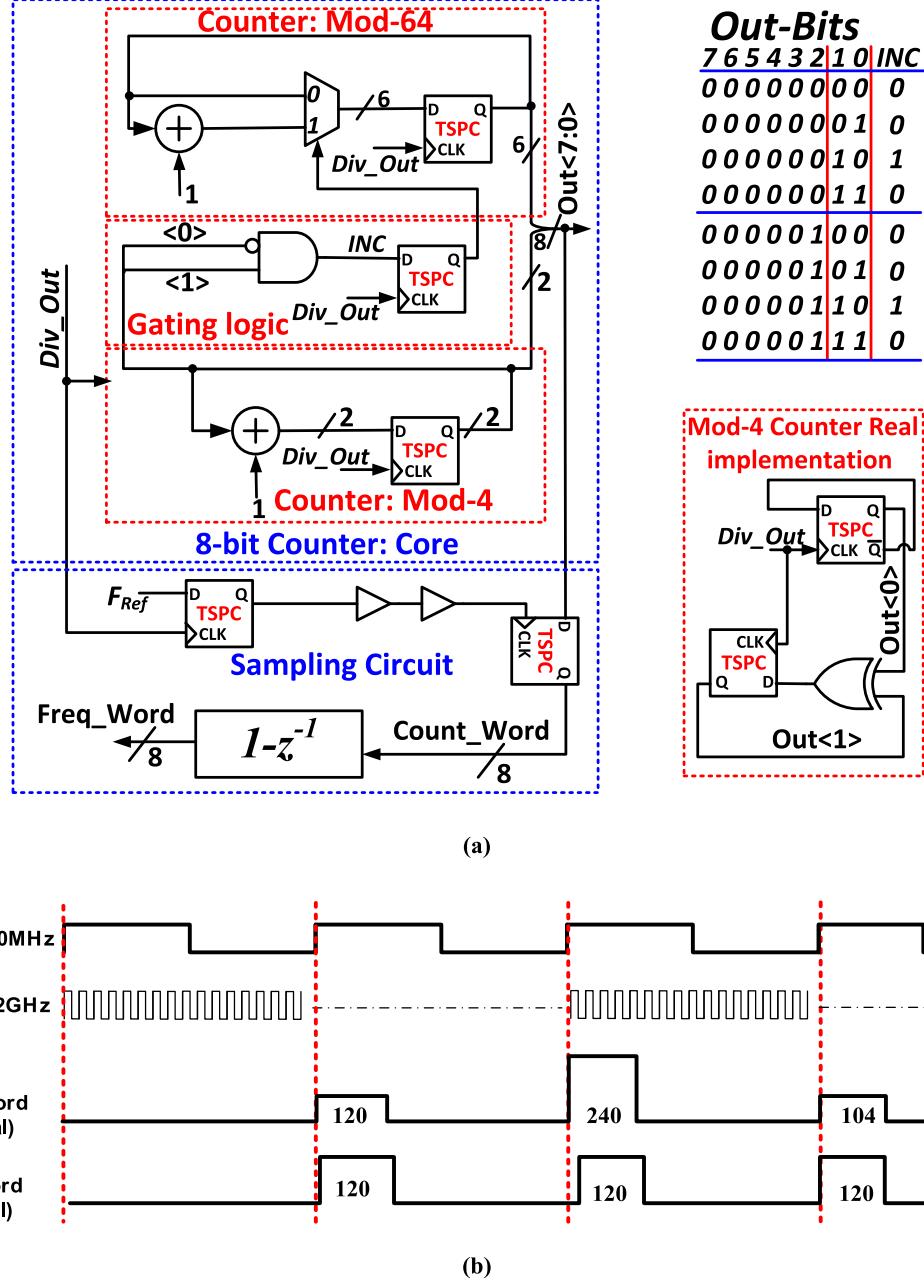


Fig. 14. (a) Detailed block diagram of high-speed counter with sampling circuit. (b) Timing diagram of high-speed counter.

counter and reference divider consume 2.6 mA from a 1-V supply.

A. Frequency Calibration and Current Minimization Algorithms

The frequency calibration and current minimization algorithms are illustrated in the flowcharts shown in Fig. 15(a) and (b). Initially, the digital words controlling the bias voltages V_{BP} and V_{BN} of the PMOS loads and tail current sources (Fig. 5) are preset to their highest value, thereby setting V_{BP} and V_{BN} to their minimum and maximum value, respectively. This initializes the divider to operate in

the sensitivity curve with highest frequency and maximum injection current. For frequency calibration (load modulation state), the difference between current and previous frequency words generated by the high-speed counter is compared with a programmable value (*Abs_error*) to detect the change in output frequency. The frequency change is averaged over a large programmable number (*Max_cycles*) of reference cycles. The calibration engine detects the state of frequency unlocking if the averaged frequency change exceeds a certain level (*Max_Errors*). If unlocked, the digital word controlling V_{BP} is decreased and other calibration state variables are reset. The above procedure is repeated until the divider locks to the right sensitivity curve and the frequency change become

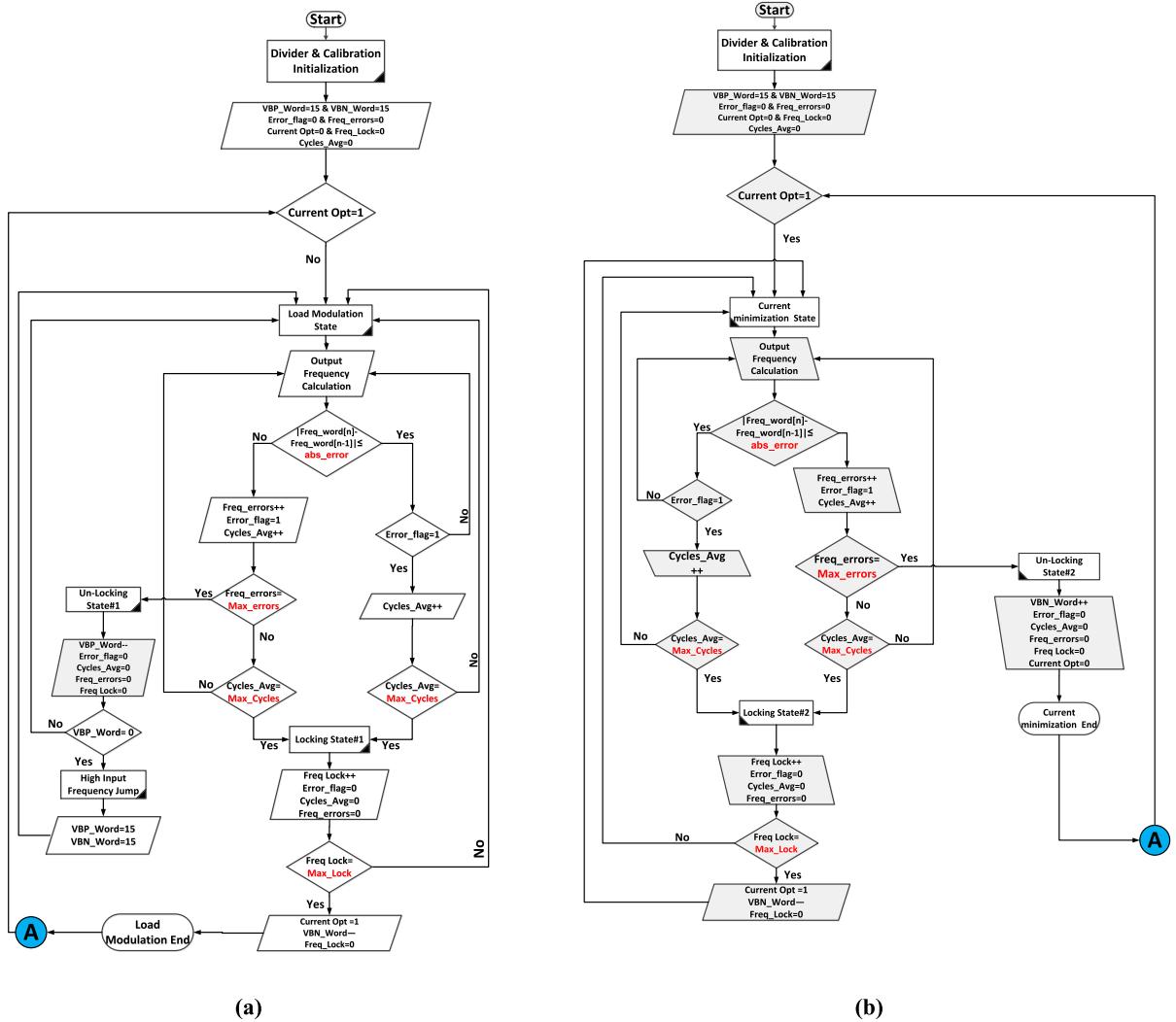


Fig. 15. Flowchart of background calibration scheme. (a) Frequency calibration via load modulation. (b) Current minimization algorithm.

negligible (i.e., less than reference frequency). Then, before switching to the current minimization algorithm, the frequency comparison is repeated for *Max_lock* reference cycles to ensure locking.

In the current minimization phase, the digital word corresponding to V_{BN} is decreased and frequency lock detection is repeated. If the divider still remains in lock after (*Max_lock* \times *Max_cycles*) reference cycles, V_{BN} is again decreased until a frequency unlocked state is detected. Finally, to return to the locked state with minimum current consumption, the digital word controlling V_{BN} is increased by one step, whereafter the calibration engine resets and resumes monitoring the output frequency variation. The operation of the self-calibration is described in detail below for two cases under different PVT conditions.

Case 1 (Abrupt Frequency Decrease): Fig. 16 shows the simulation results of the calibration scheme when a 50 GHz, 100-mV input signal is applied initially to DIV1-CB with supply voltage of 1 V, temperature of 27 °C, and typical process corner. Table I shows the nominal values of the programmable calibration parameters. The calibration operation can be divided into several regions, as shown in Fig. 17.

Initially, the divider operates at the highest sensitivity curve and calibration begins in the load modulation mode. The calibration engine modulates the output load by decreasing bias voltage V_{BP} to move across the sensitivity curves, as shown by (1) in Fig. 17(a). Once locking is achieved, the calibration engine switches to the current minimization mode. In this mode, shown by (2) in Fig. 17(b), the bias voltage V_{BN} is progressively decreased thereby decreasing the injection current in the divider and effectively narrowing the sensitivity curve. Eventually, divider loses lock, whereupon the calibration engine switches V_{BN} to back its previous value causing lock to be achieved once again, as shown by (3) in Fig. 17(b). This results in minimum power consumption at 50 GHz under the specific PVT condition. Next, the input frequency is switched to 28 GHz which causes the divider to lose lock. The calibration engine responds by setting the injection current to its highest value and updating V_{BP} to modulate the load until the lock is achieved once again [(4) and (5) in Fig. 17(c)]. Thereafter, the calibration engine switches to the current minimization mode as described previously.

Case 2 (Duty Cycle Variation and Abrupt Frequency Decrease): In this case, the duty cycle of the input waveform

TABLE I
SIMULATION PARAMETERS OF BACKGROUND CALIBRATION SCHEME

Parameter	Abs_error	Max_cycles	Max_errors	Max_lock
Value (Case1)	1	15	8	4
Value (Case2)	2	15	4	4

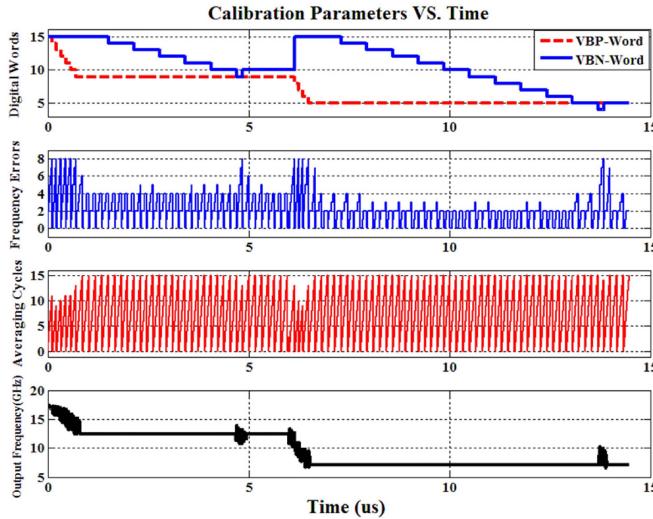


Fig. 16. Simulation results of background calibration scheme for Case1: DIV-CB at (typical process corner, Temp = 27 °C, and V_{DD} = 1 V).

is reduced to below 50% followed by an abrupt increase in frequency. The operation of the calibration is illustrated for divider DIV3 which is assumed to operate initially with a 36-GHz, 150-mV input at 85 °C in the fast-fast process corner with a supply voltage of 0.9 V. Simulation results are shown in Fig. 18. The divider is assumed to have initially settled into an “optimally” locked condition with digital words $V_{BP} = 7$ and $V_{BN} = 12$ [i.e., Point X in Fig. 18(b)]. When the duty cycle of input signals is switched from 50% to 40%, the sensitivity curves become narrower and the divider becomes unlocked. The calibration engine responds by setting the bias current to its maximum value (by changing V_{BN}) and then updates V_{BP} and V_{BN} until lock is achieved once again [(1) in Fig. 18(b)]. When the input frequency is switched abruptly to 60 GHz [region (2) in Fig. 18(c)], the calibration engine searches for the optimal sensitivity curve by first decreasing the digital word controlling V_{BP} down to its lowest value and then resetting to its maximum value.

B. Calibration Parameters

Calibration accuracy depends on the parameters *Abs_error* and *Max_Errors*. Ideally, when divider is locked, these values should converge to zero. In practice, due to PVT variations and supply voltage noise of frequency detector, the counter output toggles about the correct value. Therefore, programmable parameters *Abs_error* and *Max_Errors* are used to increase margin for PVT variation. Extensive post-layout simulations of the divider with a semi-behavioral model of the calibration

loop (where only the high-speed counter is replaced with an extracted circuit) under PVT variations have been used to set the values of *Abs_error* and *Max_Errors*; the calibration has been verified to operate correctly for settings of 1/8, 2/4, and 4/2.

In addition, to improve calibration operation and reduce the effect of parameters on calibration performance, the impact of supply variation can be alleviated by using on-chip supply regulator for frequency detection circuit and by increasing averaging time (*Max_cycles*). The calibration time can be reduced by decreasing the number of averaging cycles and locking cycles, or by increasing the reference frequency. However, this reduction will be achieved at the expense of calibration accuracy, higher power consumption and complexity of the fully synthesized digital controller. Calibration performance can also be improved by adapting *Max_Errors* after locking is detected (i.e., decreasing the value of *Max_Errors* during locking to improve calibration accuracy). Finally, it is noted that this calibration scheme can be scaled to accommodate dividers with moduli greater than four by changing the number of bits in the high-speed counter. The minimum number of bits for frequency detector can be expressed as $K_{\min} > \log_2(F_{in}/N \cdot F_{Ref})$ where F_{in} and N are input frequency of divider and division ratio, respectively.

V. CHARACTERIZATION AND DISCUSSION

A chip (Fig. 19) with three prototypes using the proposed techniques was fabricated in a 65-nm CMOS process. The core of each divider has dimensions of $11 \mu\text{m} \times 43 \mu\text{m}$. A top level schematic representative of all three prototypes is shown in Fig. 20. The input is provided externally via an on-chip balun. The divider outputs are converted to CMOS levels by a two-stage CML-to-CMOS converter which comprises a differential amplifier followed by CMOS inverters that are coupled using back-to-back inverters to maintain 50% duty cycle. A buffer chain is used to drive 50- Ω measurement loads. The supply voltage for the divider core is provided by an on-chip Low dropout regulator, while the supply voltage for digital circuits is provided from an external dc source. All measurements were performed using on-wafer probing.

It is noted that a separate “conventional” divider (Fig. 1) with devices M_{S1} , M_{S2} , and M_{P3} removed from the layout was not implemented on the test chip in order to save silicon area. However, in order to verify that DIV1-0 provides a fair reference for comparison, the locking ranges of DIV1-0 and the conventional DCML divider were compared using post-layout simulation. The input capacitance and capacitance at node X [Fig. 5(b)] of DIV1-0 were estimated to be 80 and 156 fF, compared to their respective values of 77 fF, and

TABLE II
COMPARISON BETWEEN ALL POSSIBLE CONFIGURATIONS OF DIV-1

Configuration	Original	Source coupled	Current bleeding	Both
LR: low band (GHz)	24.75-42.5	24-46.75	19-43	19-44.75
FBW: low band (%)	52.5	63.84	76.98	80.7
LR: High band(GHz)	45-63.25	45.75-67	39.5-61.5	40-66.5
FBW: High band (%)	35.6	38.58	44.71	51.1

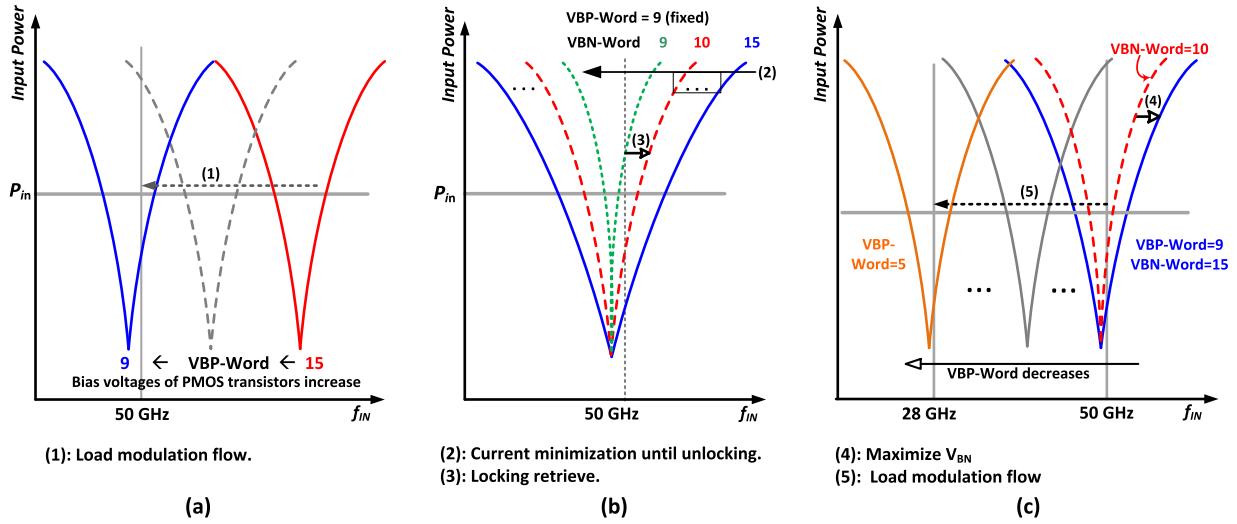


Fig. 17. Illustration of calibration shown movement across sensitivity curves (Case 1). (a) Load Modulation flow. (b) Current minimization flow until unlocking. (c) Input frequency change to lower value (28 GHz).

TABLE III
COMPARISON BETWEEN DIV1-0, DIV2, AND DIV3.

Architecture	DIV1-0	DIV2 (VDD=1.1V)	DIV3
LR(GHz): Lower band (V_{BP}=525mV)	18.25-31	20.75-38.25	16.75-34
FBW: Lower band (%)	51.7	59.4	67.9
LR(GHz): Middle band (V_{BP}=350mV)	28.5-50.25	29-59	25.5-53
FBW: Middle band (%)	55.1	68.2	70
LR(GHz): Higher band (V_{BP}=275mV)	44.75-64	45-67	41.5-67
FBW: Higher band (%)	35.6	39.1	47.1

151 fF for a conventional divider. The locking ranges of DIV1-0 and the conventional divider were estimated from post layout simulation as (41.75–71 GHz) and (41.5–71.25 GHz) at 0-dBm input power. Their lock ranges at –10 dBm input power were (51.5–64.5 GHz), and (51.4–64.8 GHz).

Fig. 21(a) compares measurements and post-layout simulations of the self-oscillation frequency F_{osc} of three samples of the baseline topology DIV1-0. The simulations—conducted on an *RC*-extracted divider core with EM-modeled supply, ground and output signal paths—indicate that by changing the PMOS bias voltage V_{BP} , the F_{osc} can vary from 5 to 20 GHz, which indicates an F_{max} of 80 GHz. Fig. 21(b) compares the measured and post-layout simulated sensitivity curves of

DIV1-0 for different bias voltages V_{BP} . A standalone on-chip balun was characterized for the purpose of de-embedding test setup losses. Maximum/minimum losses of the overall test setup were measured to be 24/18.2 dB at 16/45 GHz and they have been de-embedded. The measured sensitivity curves, which are in good agreement with simulations, span 18–64.2 GHz with fractional bandwidths of 51.7%, 56.1%, and 35.6%, respectively. At the low end, the measurement is limited by the bandpass nature of the on-chip balun. At the high end, although the divider was not characterized beyond 67 GHz due to signal generator limitations, the good agreement between the simulated and measured F_{osc} indicates that the divider is capable of operation beyond 67 GHz.

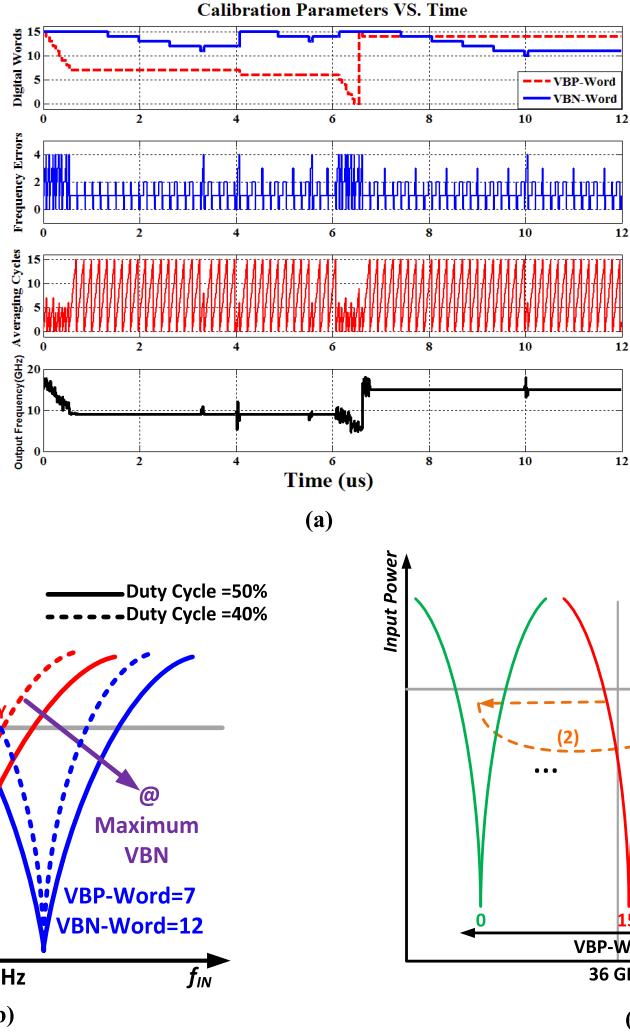


Fig. 18. (a) Simulation results of background calibration scheme for Case 2: DIV-3 at (fast-fast process corner, Temp = 85 °C, and $V_{DD} = 0.9$ V). Illustration of calibration shown movement across sensitivity curves (Case 2). (b) Duty cycle changes to 40%. (c) Input frequency change to higher value (64 GHz).

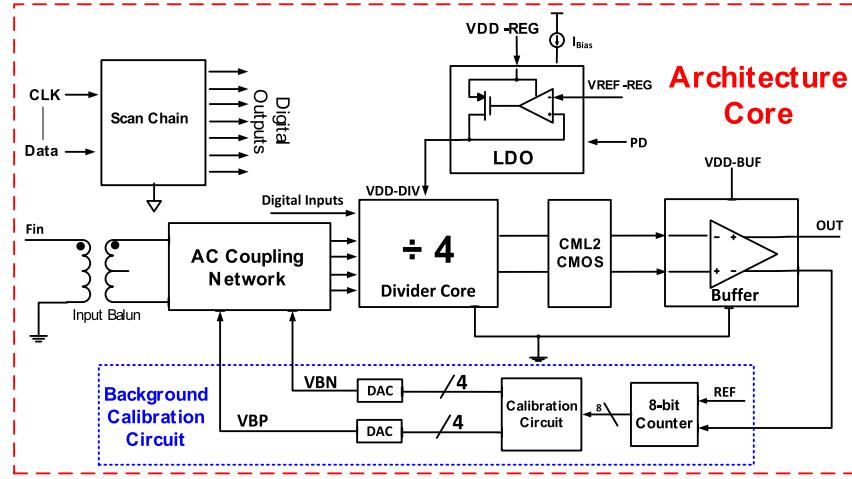


Fig. 19. Block diagram of prototype divider chip.

Fig. 22(a) compares two measured sensitivity bands of the four configurations of DIV1 with V_{BP} set to 425 and 275 mV.

Table II compares the locking range and fractional bandwidth of DIV1 for the sensitivity curves reported in Fig. 22(a).

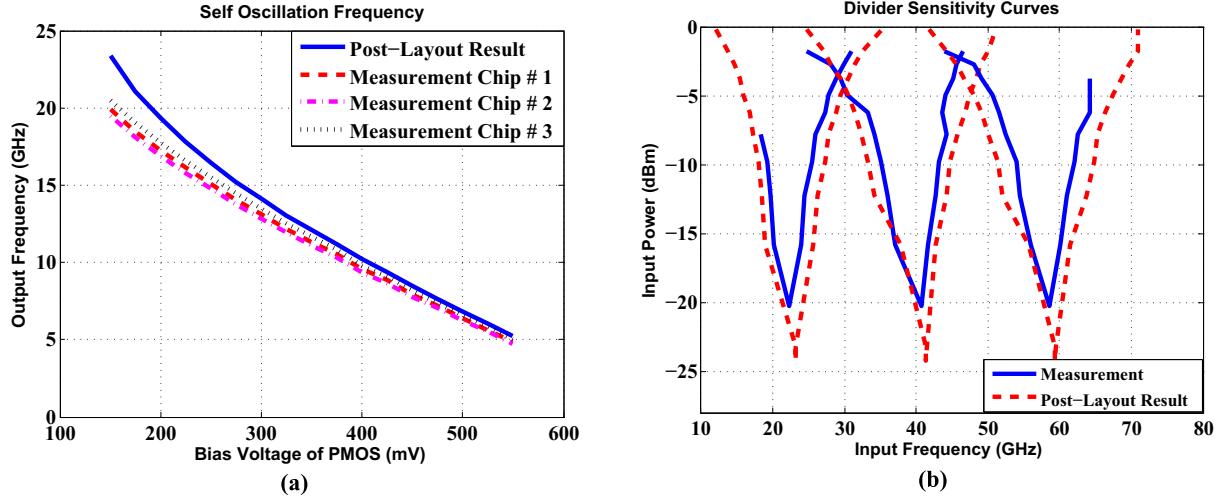


Fig. 20. (a) Measured and simulated self-oscillation frequency of first architecture divider versus bias voltage of PMOS output load. (b) Measured (solid line) versus simulated (dashed line) sensitivity curves for first architecture (control word = 00) with different bias voltage levels (525 mV: lower frequency band, 400 mV: middle frequency band, and 275 mV: higher frequency band).

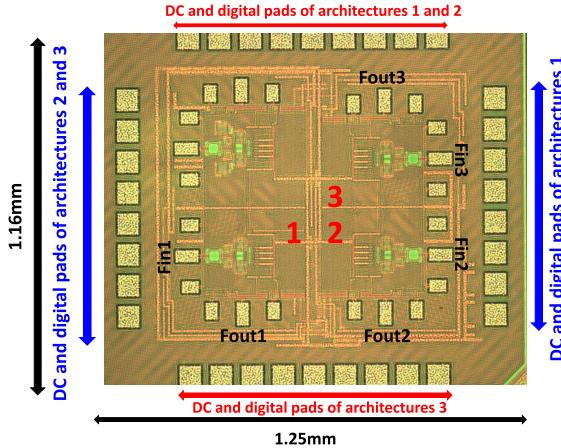


Fig. 21. Die photograph of fabricated chip.

It can be observed that the locking range is improved by more than 5 GHz when the current bleeding or source coupling techniques are used separately. Examination of Table II reveals that current bleeding along (DIV1-CB), F_{\min} decreases significantly, while F_{\max} is not affected significantly. On the other hand, source coupling alone (DIV1-SC) enables a significant increase in F_{\max} while affecting F_{\min} slightly. These observations are consistent with the analysis in Section II. Combining current bleeding and source coupling (DIV1-CB+SC) improves the locking range by 4.75 and 3.25 GHz at input power of -5 and -10 dBm, respectively. The measured locking range improvement of the DIV1-CB+SC configuration is observed to be less than the analytical prediction of Sections II and III; this is due to unaccounted capacitance at node X in Fig. 5 resulting from devices M_{n1} , M_{S1} , and M_{S2} . This capacitance absorbs a fraction of the injection current and hence decreases the operating range.

Fig. 22(b) compares DIV2 with DIV1-0 for different bias voltages V_{BP} . A 1.1-V V_{DD} is used in DIV2, so that it operates in roughly the same frequency bands as DIV1-0 or given V_{BP} ; this increases the power consumption of

DIV2 from 6.2 to 7 mW. In the low/mid/high sensitivity bands, DIV2 extends the locking range by 4.75/8.25/2.75 GHz and achieves fractional bandwidth of 59.4%/68.2%/39.1% compared to 51.7%/54.1%/35.6% for DIV1-0. Note that the improvements in the highest and lowest curves in Fig. 22(b) are limited by signal generator and on-chip balun limitations, respectively.

Fig. 23(a) compares the measured sensitivity curves of DIV3 and DIV1-0 for different bias voltages V_{BP} . It is seen that bulk modulation improves both F_{\min} and F_{\max} , as discussed in Section III, and extends the locking range by 4.5/5.75/6.25 GHz at low/medium/high curve; correspondingly, the fractional bandwidth has been improved from 51.7%/55.1%/35.6% to 67.9%/70%/47.1% in the three bands. The measured locking range and fractional bandwidth of DIV1-0, DIV2, and DIV3 are summarized in Table III; examination of this table highlights the large improvements that are enabled by the proposed circuit design techniques.

Fig. 23(b) shows the variation in F_{OSC} of DIV3 with the bulk bias voltage V_{BL} for $V_{BP} = 350$ mV. The sensitivity of F_{OSC} to V_{BL} is -5.3 GHz/V; this provides another method to shift the sensitivity curve by more than 20 GHz for a given current consumption.

The phase noise at the input and the output of the divider (DIV2) are measured using a Keysight E5052B signal source analyzer, and are shown in Fig. 24(a) and (b), respectively for 52-GHz input frequency. Fig. 25 and Table IV compare the measured phase noise of proposed architectures with input frequency of 44 GHz. Since DCML divider is a synchronous divide-by-four, it does not suffer from jitter accumulation. The output phase noise is reduced by roughly 12 dB compared to the input. This reduction extends to about 2-MHz offset from the carrier frequency beyond which amplitude noise from the buffers starts to dominate. As expected, the phase noise of proposed DIV2, DIV3 is better than DIV1-0, since the phase noise of a DCML latch is proportional to (C_L/I_{ON}^2) [27].

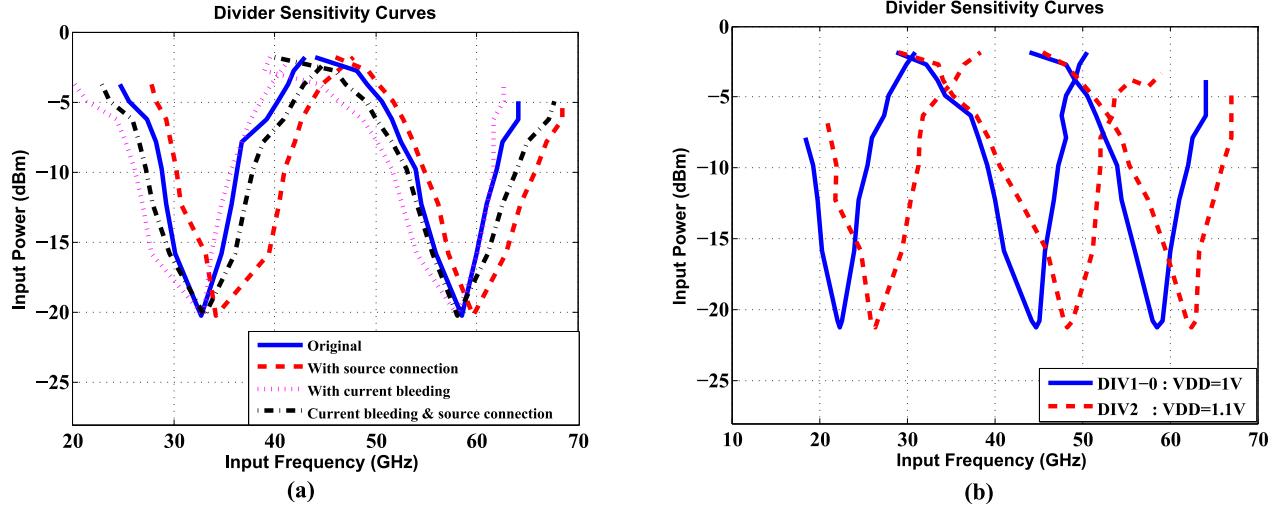


Fig. 22. (a) Measured sensitivity curves of first architecture with different bias voltage levels and control words. Note that only two sensitivity curves are reported due to figure's clarity. (b) Measured sensitivity curves of conventional DCML divider (solid line) versus measured sensitivity curves of second architecture (dashed line) with combination of HVT and LVT devices with different bias voltage levels (note: for clarity, only a few sensitivity curves are shown here.)

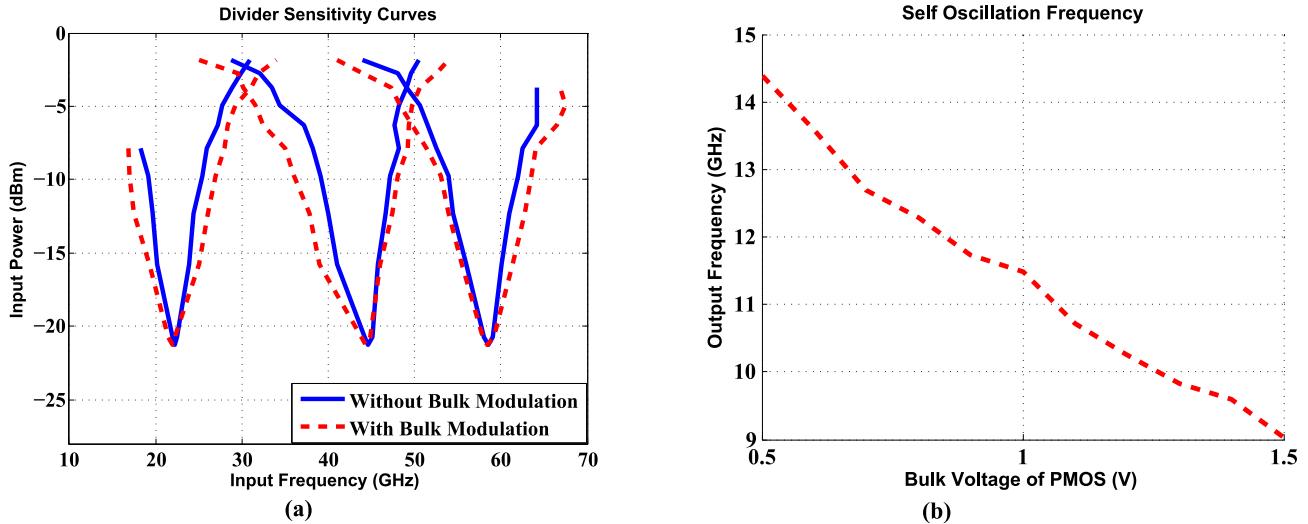


Fig. 23. (a) Measured sensitivity curves of DIV1-0 (solid line) versus measured sensitivity curves of DIV3 (dashed line) with bulk modulation for different bias voltage levels. (b) Measured self-oscillation frequency of third architecture versus bulk voltage of PMOS load.

TABLE IV
COMPARISON BETWEEN PHASE NOISE OF PROPOSED ARCHITECTURES

	Frequency Offset (Hz)	1K	10K	100K	1M	2M	10M
Phase noise (dBC/Hz)	Input signal (44GHz)	-69.34	-82.93	-78.14	-101.1	-105.8	-126.1
	DIV1-0	-80.72	-94.13	-89.5	-110.3	-113.1	-124.5
	DIV1+ CB+SC	-80.63	-94.39	-89.27	-110.81	-113.25	-126.3
	DIV2	-81.05	-94.62	-89.4	-110.52	-113.72	-127
	DIV3	-80.61	-94.2	-89.38	-111.2	-112.9	-127.7

Fig. 26 shows the operation of the calibration engine. Calibration was characterized for all divider topologies, and behaves as expected; however, characterization results are presented herein only for DIV1-CB+SC. Fig. 26(a) shows the locked output spectrum at 1-V V_{DD} for a 52 GHz, -10 dBm input. When the V_{DD} is decreased by 100 mV, the divider

loses lock, as shown in Fig. 26(b). The calibration circuit is then enabled, whereupon the divider regains lock by changing the bias voltage V_{BP} and moving to a different sensitivity curve; this is shown in Fig. 26(c). The input frequency is then changed abruptly to 24 GHz; Fig. 26(d) shows the output spectrum as the calibration engine enables the divider to regain

TABLE V
MEASUREMENT SUMMARY AND COMPARISON WITH THE STATE OF THE ART

Ref.	$\frac{F_{in}}{F_{out}}$	F _{min} -F _{max} (GHz)	FBW ^(a) (%)	FBW ^(b) (%)	Power (mW)	Suppl y(V)	Area (μm^2)	Tech (nm)	FOM ^(c) (Min/Max)	FOM _P ^(d) (Min/Max)
[13]*	4	62.9-71.6	2.2	1.13	2.8	0.5	110x130	90	0.21/0.57	4.3/11.4
[14]	4	79.7-81.6	2.4	0.87	12	0.56	106x330	65	0.16	2.34
[15]	2	82.5-89	7.6	5.1	3	0.5	220x290	90	2.17	28.67
[16]	2	53.4-79.4	39.2	8.4	2.9	0.8	420x300	65	8.97	37.93
[17]*	3	48.8-54.6	3.5	3.1	3	0.9	300x300	65	0.27/0.57	6/16
[18]	4	58.5-72.9	21.9	6.8	2.2	0.6	260x160	65	6.54	81.8
[19]	2	31-47	41.1	20.3	24	1.2	260x350	90	0.67	7.083
[24]*	4	20-70	9.7	4.52	6.5	1	15x30	65	0.46/1	6.15/15.4
[26]*	4	14-70	90	63.4	1.3/4.8	1	18x55	32	6.7/17.5	83.3/399
[27]*	4	25-102	42.2	16.67	2.8/5.6	0.9	25.6x25	28	0.71/8.57	28.4/142
[29]	3	58.6-67.2	13.7	6.25	5.2	1	170x220	65	1.65	23.1
[30]	4	67-72.4	7.7	0.3	15.5	1.2	870x760	90	0.35	0.516
[31]*	2	35-59.5	32	8.8	3.9	1.1	630x90	130	2.4/4.2	23.1/24.6
This Work*: DIV1-0	4	18-65**	55.1	23.3	3.7- 6.2	1	11x52	65	3/5.8	51.6/67
This Work*: DIV1- CB+SC	4	16-67**	81.2	49.8	3.7- 6.2	1	11x52	65	4.4/7.03	66.4/113
This Work*: DIV2	4	16-67**	68.2	38.7	4.3- 7.4	1.1	11x43	65	3/6.98	56.8/105
This Work*: DIV3	4	16-67**	70	45.4	3.85- 6.25	1	11x43	65	4.1/7.15	67.2/104
This Work: DIV1- CB+SC Calibration	4	16-67**	122	110.5	6.2- 8.7	1	52x60	65	5.87	202.3/ 283.8
This Work: DIV2- Calibration	4	16-67**	122	104.2	6.75- 9.65	1.1	52x60	65	5.285	188.6/ 269.7
This Work: DIV3- Calibration	4	16-67**	122	114.8	6.42- 8.82	1	52x60	65	5.782	199.5/ 274.14
$FBW \text{ (%)} = \frac{2(F_{\max} - F_{\min})}{(F_{\max} + F_{\min})}$			$FOM \text{ (GHz / mW)} = \frac{F_{\max} \text{ (GHz)} - F_{\min} \text{ (GHz)}}{P_{diss} \text{ (mW)}}$			$FOM_p \text{ (GHz / } \mu\text{W}^2) = \frac{F_{\max} \text{ (GHz)} - F_{\min} \text{ (GHz)}}{P_{diss} \text{ (mW)} P_{in} \text{ (mW)}} X \frac{F_{in}}{F_{out}}$				

(a) Reported locking range at maximum reported input power. (For all cases except the last row, in which calibration is enabled, the FBW is defined as the best amongst the FBW's of all sensitivity curves).

(b) Best FBW, among all reported sensitivity curves, at input power of -10dBm.

(c) Best/Worst FOM among all reported sensitivity curves. Locking range is calculated at maximum reported input power of each sensitivity curves.

(d) Best/Worst FOM_P, among all reported sensitivity curves, at input power of -10dBm.

* Covers the whole locking range (F_{min}-F_{max}) by multiple sensitivity curves.

** Limited by on-chip balun and available equipment

lock. It can be observed that spurs appear at $F_{out} \pm nF_{Ref}$ after calibration; these are caused by clock feedthrough from the calibration engine that generates the digital word that

controls (through a DAC) the bias voltages V_{BP} in the latches. Simulations with carefully extracted parasitics show that these spurs can be eliminated by either gating the clock of these

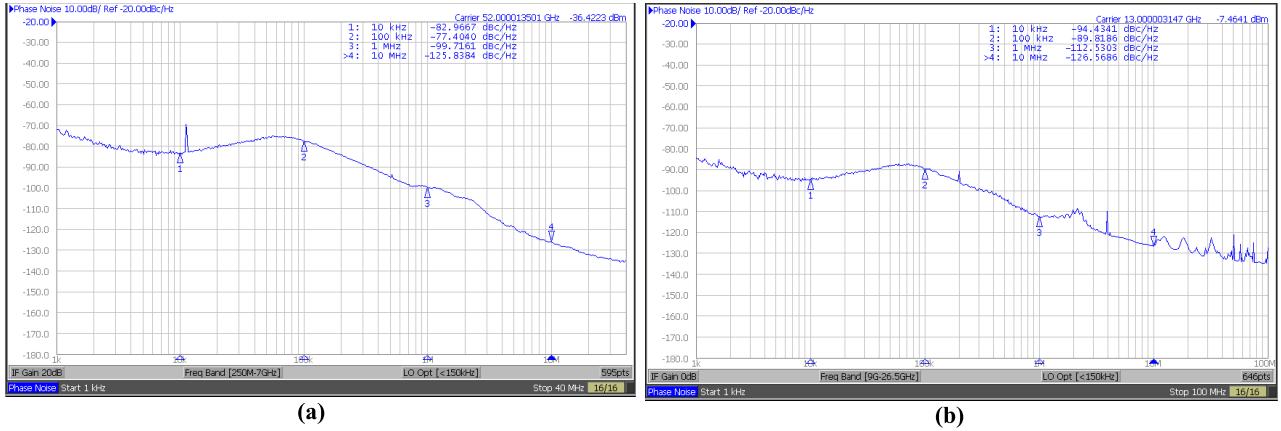


Fig. 24. Phase noise measurement. (a) input signal ($F_{\text{in}} = 52 \text{ GHz}$). (b) output signal ($F_{\text{out}} = 13 \text{ GHz}$).

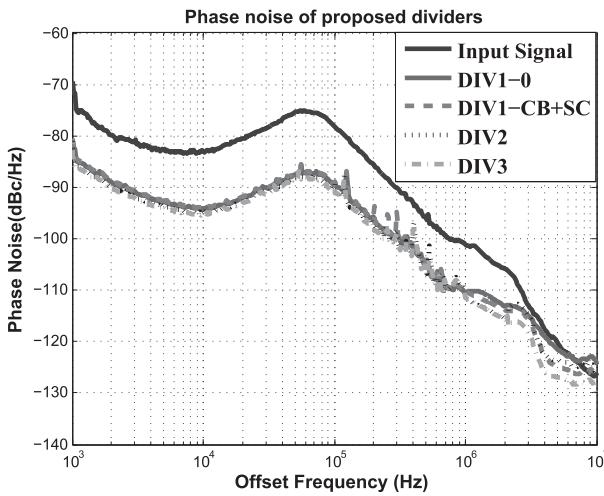


Fig. 25. Comparison between measured phase noise of proposed dividers with input signal of 44 GHz.

latches after calibration or by buffering them prior to the DAC controlling V_{BP} .

Measurement results and benchmarks are summarized in Table V. For the dividers with multiple sensitivity curves, Figure of merit (FOM) and Fractional bandwidth (FBW) of each curve are calculated at maximum reported input power of each benchmark. In order to make a fair comparison with dividers with moduli other than four, and to explicitly account for the fact that achieving a target locking range becomes harder at low-input amplitude, it was necessary to define a new figure-of-merit as follows:

$$\text{FOM}_P(\text{GHz}/\mu\text{W}^2) = \frac{F_{\text{max}} \text{ (GHz)} - F_{\text{min}} \text{ (GHz)}}{P_{\text{diss}} \text{ (mW)} P_{\text{in}} \text{ (mW)}} \times \frac{F_{\text{in}}}{F_{\text{out}}} \quad (3)$$

Three main conclusions are drawn from Table V: 1) the proposed techniques significantly enhance performance and robustness in practical applications; 2) in contrast to previous designs, the proposed designs demonstrate little locking range degradation at low-input amplitude compared to the maximum achievable locking range at high-input amplitude; and 3) Using the calibration scheme, the proposed dividers cover widest locking range reported to date (16–67 GHz) without any

manual tuning which results in highest FOM_P to date.

It is worth noting that the divide-by-two ILFD in [16] features the highest FOM in Table V. This is due to the combined advantage of injection locking to a resonant circuit using a strong second harmonic rather than a weak fourth harmonic in divide-by-four. However, this advantage vanishes when FOM_P is used for comparison, as seen in Table V.

Table V also underscores the scaling-friendly nature of the DCML approach, as evidenced by the fact that the divide-by-four designs [26], [27] with superior FOM are designed in more advanced CMOS technologies. Note, however, that advanced technologies (especially 32 nm and below) vary widely in terms of process type and flavor. Such considerations, as well as the availability of process features chosen for a particular application can heavily influence design choices. Therefore, the circuit techniques proposed herein (or combinations thereof), and the self-calibration scheme are highly relevant even in more advanced technologies.

VI. COMPARISON AND EXTENSIONS OF DIVIDER TOPOLOGIES

In this section, the proposed divider topologies are compared based on the analysis and measurements presented in Section II and Section V, respectively. Several observations and conclusions can be drawn as follows.

- 1) In low-cost CMOS designs without additional process options such as multiple V_t devices or triple well, source coupling alone can be used to increase F_{max} , while current bleeding alone can be used to decrease F_{min} . Combining the two techniques improves F_{max} and F_{min} despite a small increase in the input capacitance.
- 2) In designs using technologies where devices with different V_t and/or triple well are available, DIV2 and DIV3 can improve locking range at the expense of slightly higher power consumption and input capacitance, respectively.
- 3) Certain combinations of the proposed techniques can be used to further improve the locking range. For example, source coupling can be combined with HVT loads to improve both F_{max} and F_{min} with approximately the same input capacitance and power consumption. Bulk

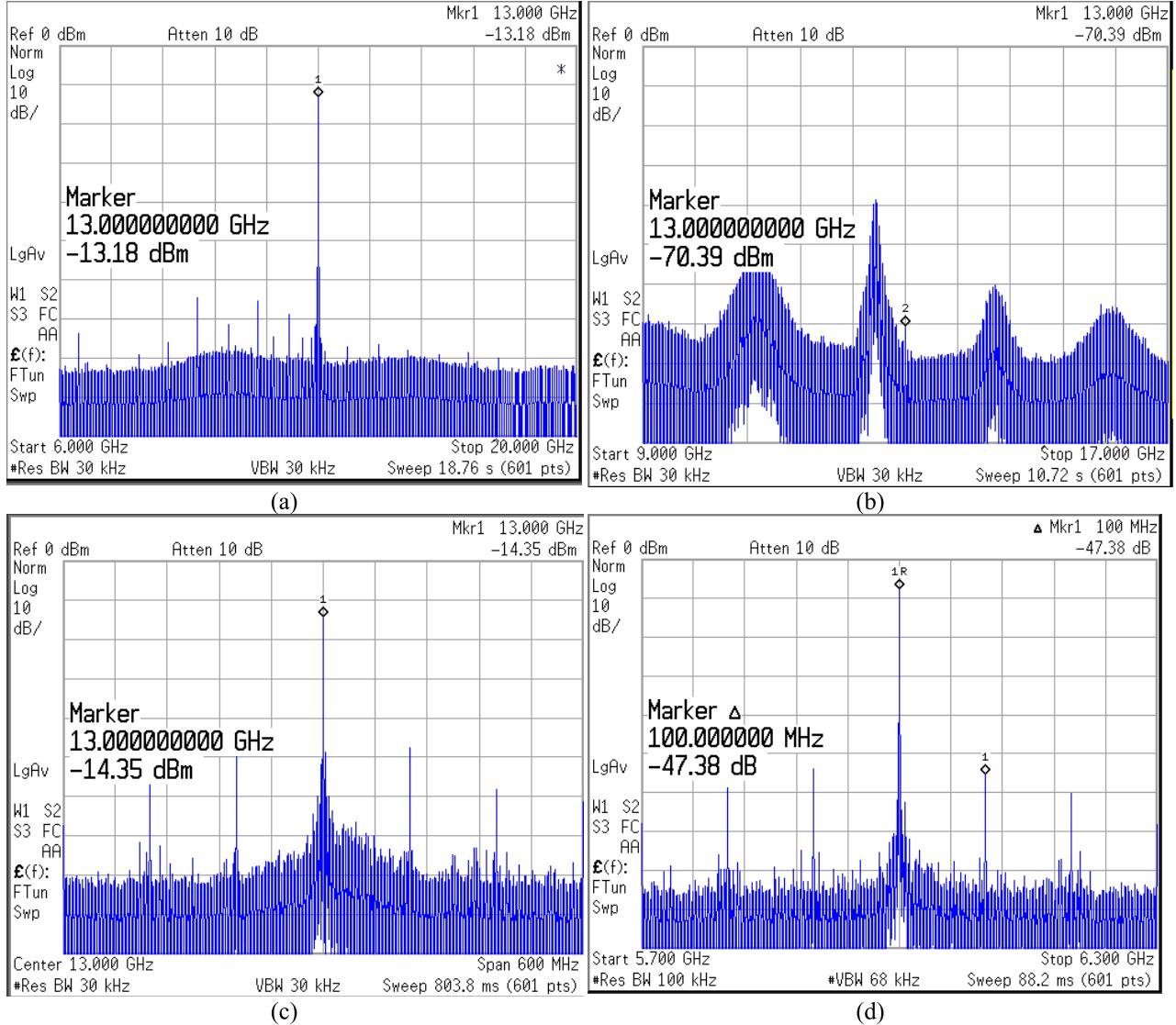


Fig. 26. Output spectrum of DIV1-0 with self-calibration scheme. (a) $F_{in} = 52$ GHz, $V_{DD} = 1$ V, and $\text{Cal_EN} = 0$ (Locked). (b) $F_{in} = 52$ GHz, $V_{DD} = 0.9$ V, and $\text{Cal_EN} = 0$ (Unlocked). (c) $F_{in} = 52$ GHz, $V_{DD} = 0.9$ V, and $\text{Cal_EN} = 1$ (Locked). (d) $F_{in} = 24$ GHz, $V_{DD} = 0.9$ V, and $\text{Cal_EN} = 1$ (Locked).

modulation and current bleeding can be combined to further reduce F_{min} .

- 4) Combining all of the above techniques can further improve locking range; however a price is paid in terms of higher input capacitance and power consumption. In other words, overall performance improvement can be achieved if the input amplitude is low, but such improvement is diminished when higher input amplitude can be delivered. For example, the effectiveness of combining current bleeding, HVT loads and bulk modulation in reducing I_{OFF} is diminished when the input amplitude is increased. Similarly, the effectiveness of combining source coupling, LVT tail transistor and bulk modulation in increasing I_{ON} is diminished at higher input amplitude. Nevertheless, the improvements offered by combining all techniques can result in a reduction of overall system power, especially at high

mm-wave frequencies, since the swing at the output of the LO buffer can now be smaller, thereby reducing its current consumption.

VII. CONCLUSION

We have proposed several new design techniques to enhance the operating frequency range and locking range of inductorless mm-wave frequency dividers. These techniques are informed by a more refined analysis of the divider than available in the literature. The proposed design techniques, namely source coupling, current bleeding, multi- V_t design, adaptive bulk biasing and bulk modulation are demonstrated via three prototype designs. A calibration scheme is proposed to adaptively tune and optimize bias settings for a given input frequency, thereby enhancing robustness, reducing power consumption and resulting in a practically usable divider.

All proposed techniques are demonstrated through extensive characterization.

APPENDIX TIME DOMAIN ANALYSIS OF MINIMUM OPERATING FREQUENCY

From Figs. 1 and 2, the latch output voltages V_P and V_N during the read phases (t_0, t_1) , and (t_2, t_3) can be expressed as

$$\begin{aligned} V_P(t) &= V_{DD} + (V_{Pi} - V_{DD})e^{-\frac{t-t_i}{R_{ON}C_L}} \\ V_N(t) &= V_{DD} - I_{ON}R_{ON} + (V_{Ni} - V_{DD} + I_{ON}R_{ON})e^{-\frac{t-t_i}{R_{ON}C_L}}. \end{aligned} \quad (4)$$

In addition, during the decaying region (t_{3x}, t_4) , when the differential output voltage $(V_P - V_N)$ starts to decay toward $-I_{OFF}R_{OFF}$ instead of remaining at $I_{ON}R_{ON}$ as in the ideal case, the latch outputs can be expressed as

$$\begin{aligned} V_P(t) &= V_{DD} - I_{OFF}R_{OFF} \\ &\quad + (V_{P3x} - V_{DD} + I_{OFF}R_{OFF})e^{-\frac{t-t_{3x}}{R_{OFF}C_L}} \\ V_N(t) &= V_{DD} + (V_{N3x} - V_{DD})e^{-\frac{t-t_{3x}}{R_{OFF}C_L}}. \end{aligned} \quad (5)$$

In order to maintain frequency lock, the differential output voltage $(V_P - V_N)$ should be higher than V_{SW} at the end of decaying region. In other words, the following condition should be satisfied

$$V_{SW} \geq -I_{OFF}R_{OFF} + (I_{ON}R_{ON} + I_{OFF}R_{OFF})e^{-\frac{T_{decay}}{R_{OFF}C_L}} \quad (6)$$

where T_{decay} , the maximum allowable decaying time to ensure proper operation can be derived as

$$T_{decay} = t_4 - t_{3x} = R_{OFF}C_L \cdot \ln \left(\frac{I_{ON}R_{ON} + I_{OFF}R_{OFF}}{V_{SW} + I_{OFF}R_{OFF}} \right). \quad (7)$$

By defining the minimum operating frequency F_{min} as $0.5/(T_{decay} + T_{SW})$, and by deriving $T_{SW} = t_{3x} - t_3$ from (1), F_{min} can be expressed as

$$F_{min} = \frac{1}{2R_{OFF}C_L \cdot \ln \left(\frac{I_{ON}R_{ON} + I_{OFF}R_{OFF}}{V_{SW} + I_{OFF}R_{OFF}} \right) + 4R_{ON}C_L \cdot \ln \left(\frac{V_{SW}}{I_{ON}R_{ON}} + 1 \right)}. \quad (8)$$

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