A 312-GHz CMOS Injection-Locked Radiator With Chip-and-Package Distributed Antenna

Liang Wu, *Member, IEEE*, Shaowei Liao, *Senior Member, IEEE*, and Quan Xue, *Fellow, IEEE*

***Abstract*— This paper presents an injected-locked THz radiator integrating a half-quadrature voltage-controlled oscillator (HQVCO), four injection-locked frequency quadruplers (ILFQs), and a chip-and-package distributed antenna (DA). At the system level, an architecture based on injection locking is employed to allow individual optimization of the output power and the phase noise. At the circuit level, intrinsic-delay compensation and harmonic boosting techniques are proposed to optimize the phase noise of the HQVCO and the output power of the ILFQs, respectively. The proposed DA composed of four exciting elements on silicon chip and a primary radiator in low-temperature co-fired ceramic (LTCC) package features a wide bandwidth of 13% and a gain of 3.8 dBi without using lens at 312 GHz. Implemented in a 65-nm CMOS process, the radiator system occupying a core area of 0.36 mm^2 achieves output frequency from 311.6 to 315.5 GHz and maximum equivalent isotropically radiated power (EIRP) of 10.5 dBm while consuming 300 mW. The output phase noise measures −109.3 dBc/Hz at 10-MHz offset and the dc-to-THz efficiency is 0.42%.**

***Index Terms*— Distributed antenna (DA), equivalent isotropically radiated power (EIRP), harmonic boosting, injection locking, intrinsic-delay compensation, phase noise, positive feedback, radiator, terahertz (THz).**

I. Introduction

As ONE of the least tapped regions in electromagnetic (EM) spectrum, the terahertz (THz) band from 0.3 to 3 THz is gaining increasing research interest due to the numerous potential applications uniquely enabled by such short wavelengths including imaging, spectroscopy, and high-speed wireless communications [1]–[4]. In reality, a technology vacuum known as "terahertz gap" exists [5], [6], inducing major challenges in implementing radiation sources with sufficient output power to overcome the severe path loss at such high frequencies. Currently, most THz sources rely on photonic devices such as quantum cascade lasers or compound semiconductor devices such as Gunn and resonant tunneling diodes, which are bulky and expensive [7]–[9]. On the other hand, as the cutoff frequency (f_T) of nanometer-scale CMOS devices gradually approaches sub-THz, fully integrated CMOS solutions with compact form factor, high reliability, and low cost are becoming increasingly promising. Recent works have successfully demonstrated sources and radiators from sub-THz to THz in bulk CMOS [7], [10]–[15] and SiGe BiCMOS [16]–[19]. In [10], a 280-GHz radiator based on 16 distributed active radiating elements is reported, achieving output power of 0.19 mW and equivalent isotropically radiated power (EIRP) of 9.4 dBm. In [12], a 288-GHz signal source with 0.38-mW output power is presented. In [13], the novel self-feeding oscillator array obtains 1.12-mW output power and 15.4-dBm EIRP at 260 GHz. Additionally, the radiator array using 16 coupled oscillators in [14] achieves 338-GHz output with RF power of 0.81 mW and EIRP of 17.1 dBm. In these works, high-order harmonic extraction approach is widely employed to overcome f_T limitations and realize radiation frequency far beyond that achievable from fundamental oscillation. By combining signal powers from a number of integrated elements, either on-chip or in free space, the overall EIRP can be increased to a useful level.

Despite the remarkable progress achieved in maximizing the output power and EIRP, the inadequate f_T of CMOS transistors significantly limit the dc-to-RF conversion efficiency. For example, to generate frequency above 300 GHz, most existing signal sources typically rely on fourth-order harmonics, due to the insufficient fundamental oscillation frequency for lower-order harmonic extraction [15]. As a result, the power efficiency is typically as low as 0.05%. In addition to the output power, the phase noise is another important requirement for THz sources to enable applications such as imaging and time-domain spectroscopy [20], [21]. Fortunately, the strong fundamental oscillation which consumes a large power for harmonic extraction automatically benefits the phase noise. Typical values around 300 GHz are within −78 to −85 dBc/Hz at 1-MHz offset. Further phase noise improvement would mandate some novel circuit techniques. In [14], an array of 16 oscillators coupled together achieves phase noise of −93 dBc/Hz at 1-MHz offset. For signal sources composed of only a few elements, phase noise improvement remains a problem.

In radiators, antennas are necessary to radiate the electrical signal generated from the on-chip signal sources into free space as an EM wave. At THz frequencies, however, the use of off-chip antennas is not feasible due to the severe interconnection loss and the high packaging cost. To avoid this issue, on-chip antennas can be integrated with the signal source on the same die, but the lossy silicon substrate and the metal/dielectric structure theoretically impose an upper limit on the antenna performance in terms of radiation efficiency, gain, and bandwidth. Attaching a lens onto the substrate for backside radiation can increase the antenna gain [12], [13].

Manuscript received January 12, 2017; revised April 8, 2017; accepted July 10, 2017. Date of publication July 31, 2017; date of current version October 23, 2017. This work was supported by the Research Grants Council of the Hong Kong Special Administrative Region under the General Research Funds under Grant GRF 11266416. This paper was approved by Associate Editor Hossein Hashemi.

The authors are with the State Key Laboratory of Millimeter Waves, City University of Hong Kong, Hong Kong (e-mail: liang.wu@cityu.edu.hk; eeqxue@cityu.edu.hk).

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Digital Object Identifier 10.1109/JSSC.2017.2727046

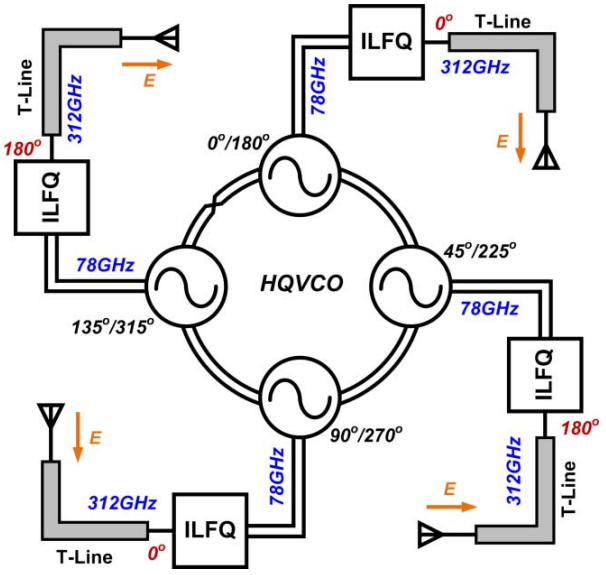


Fig. 1. System architecture of the proposed 312-GHz injection-locked radiator.

However, the lens is costly and the antenna efficiency degrades as the chip area increases [22]. To address these issues, metal plated trenches are implemented on the chip's backside such that an antenna gain of ~4 dBi can be achieved [22]. The drawback is that post-processing of the wafer including backside slicing and metal filling is required.

This paper describes the design and characterization of a 312-GHz injection-locked radiator composed of a half-quadrature voltage-controlled oscillator (HQVCO), four injection-locked frequency quadruplers (ILFQs) and an antenna array. The injection locking architecture decouples the power generation and the phase noise improvement. Furthermore, intrinsic-delay compensation and harmonic boosting techniques are proposed to optimize the phase noise of the HQVCO and the output power of the ILFQs, respectively. For the antenna, a distributed structure with exciting elements on chip and the primary radiator in low-temperature co-fired ceramic (LTCC) package featuring 3.5–5.5-dBi gain and >13% bandwidth is integrated. Implemented in a 65-nm CMOS, the prototype achieves an EIRP of 10.5 dBm, phase noise of –109 dBc/Hz at 10-MHz offset and dc-to-THz efficiency of 0.42% while consuming 300 mW.

This paper is organized as follows. Section II describes the system architecture of the injection-locked radiator. Section III discusses the intrinsic-delay compensation technique for the HQVCO and the circuit implementation. The ILFQ with harmonic boosting is presented in Section IV. In Section V, the proposed chip-and-package distributed antenna (DA) is discussed in detail. The experimental results are presented in Section VI. Finally, Section VII concludes the paper.

II. System Architecture

The proposed radiator system consists of a HQVCO, four ILFQs, and a DA with four exciting elements, as shown in Fig. 1. The HQVCO operates at a center frequency of ~78 GHz and is composed of four identical oscillation cells coupled together in a ring such that their output phases are evenly spaced from 0° to 315°. Each of the four outputs injection locks an ILFQ which multiplies both the frequency and the phase by four. In total, this results in four single-ended outputs at $4f_0$ (~312 GHz) spaced 180° apart. Afterward, they feed four exciting elements of the DA to excite EM waves for radiation and spatial power combining. When injection-locked, both the frequency and the phase noise of the radiated signal are defined by the HQVCO. Additionally, since the HQVCO's oscillation amplitude is relatively constant, the output power of the radiator is mainly determined by the ILFQs. As such, the frequency and the power generation are decoupled from each other, yielding several advantages. First, the frequency tuning can be accomplished by the HQVCO and thus low-Q tuning varactors are avoided in the ILFQs. Second, the radiator could simultaneously achieve low phase noise and high output power by optimizing the HQVCO and the ILFQs independently.

In addition to achieving low phase noise for the HQVCO and high output power for the ILFQs, there are some other requirements in designing the building blocks. First, the locking range of the ILFQs should be designed wide enough to cover the frequency tuning range of the HQVCO with enough margin to tolerate the frequency shifts due to process, voltage and temperature variations. Second, the feeding network and the polarization of the four antenna exciting elements should be able to accommodate the 0° /180° phases of the ~312-GHz outputs for constructive power combining. And finally, in order to optimize the overall EIRP for the system, both the antenna's efficiency and gain should be maximized. In the following sections, each of these requirements will be addressed.

III. HQVCO With Intrinsic-Delay Compensation

Conventional mmW *LC* VCOs typically suffer from limited phase noise performance primarily due to the use of low-Q varactors for frequency tuning. As a result, several varactor-less tuning techniques have been investigated in recent years [23]–[25], demonstrating substantial phase noise improvement. On the other hand, the intrinsic time delay of the transistors has been overlooked in conventional *LC* VCOs as well as in varactor-less VCOs. At radio frequencies, the delay is minimal and thus can be ignored. However, as the frequency goes up, it could contribute significant phase shift. Periodic steady-state simulations in SpectreRF indicate that the delay of a 65-nm NMOS device with size of 12μm/60nm is around 0.7 ps, which corresponds to a phase shift of −20° at 78 GHz, as plotted in Fig. 2(a). As such, for a cross-coupled *LC* VCO, there is a negative phase shift of $-\varphi_t = -(\varphi_d + \varphi_p)$ between the self-oscillating current i_a and the transistor's input voltage, where $-\varphi_d$ and $-\varphi_p$ represent the phase delay contributed by the transistor and the routing parasitics of the layout, respectively, as shown in Fig. 2(b). In order to fulfill the phase condition for oscillation, the *LC* tank must therefore contribute a positive phase shift. Consequently, the oscillation frequency would be displaced from the resonant frequency (ω_0) of the *LC* tank, resulting in a reduced output amplitude and a lower effective tank Q, as illustrated in Fig. 2(c). From [26], the effective Q can be derived as

$$Q_{\text{eff}} = Q_0 \cdot \cos(\varphi_d + \varphi_p) \quad (1)$$

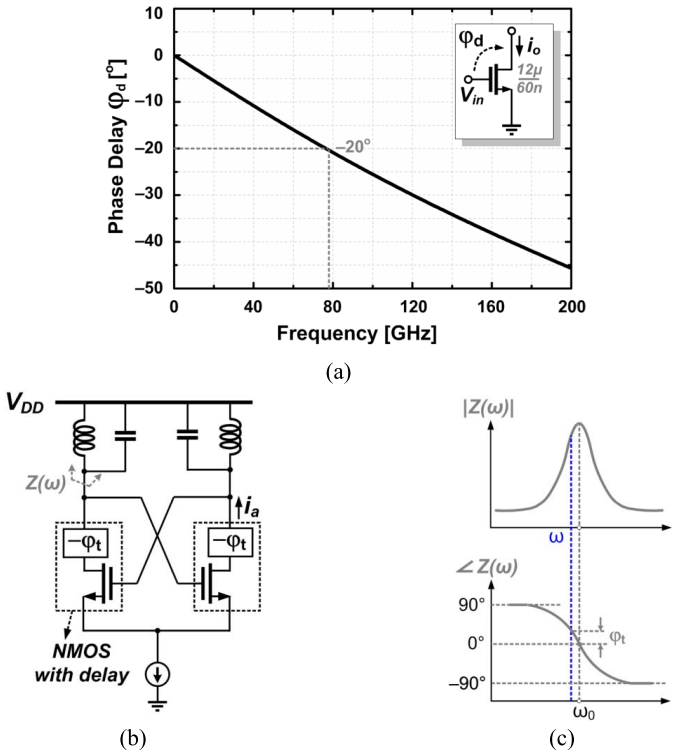


Fig. 2. (a) Simulated intrinsic phase delay in an NMOS transistor at different frequencies. (b) Schematic of conventional *LC* VCOs considering the phase delay. (c) Tank impedance plot.

where Q_0 denotes the intrinsic Q of the *LC* tank at its resonant frequency. Since the phase noise is proportional to $1/Q_{\text{eff}}^2$ or $1/Q_{\text{eff}}^3$, the Q reduction will inevitably degrade the phase noise [27].

As illustrated in Fig. 3(a), the phase delay of i_a could be compensated if another current i_b with phase advance is injected into the *LC* tank such that their resulting y-axis current components have equal, but opposite magnitudes. Meanwhile, the x-axis component of i_b adds up with that of i_a, which counteracts the tank loss and sustains oscillation. The required phase-advanced signal can be provided by utilizing multi-phase oscillation. Considering the magnitude of the phase delay, eight-phase oscillation is chosen such that the phase difference between i_a and i_b is 45°. In the circuit implementation, i_a is generated by the cross-coupled transistors while the current injection of i_b is accomplished by a differential pair, as shown in Fig. 3(b). Four of these oscillation cells are connected together in a ring. As the current injection provides sufficient coupling between neighboring oscillator cells, an HQVCO is formed and eight-phase oscillation is obtained, as illustrated in Fig. 3(c). The injection devices are designed to be of the same size as the cross-coupled pairs and their dc operating points are optimized to make the oscillator operate in the boundary between the current-limit and voltage-limit regimes [28]. To facilitate the interconnection from the HQVCO to the ILFQs, the resonant tank uses transformers with input and output ports on opposite sides. Each transformer is composed of a single-turn primary coil (L_p) interleaved with a two-turn secondary coil (L_s) to maximize their magnetic coupling. From EM simulations in HFSS, L_p and L_s are 46 and 105 pH with quality factor of 10 and 16, respectively. Their coupling factor is around 0.4 at 78 GHz.

Comparatively, the proposed HQVCO above consumes up to four times the power of a single differential VCO. Fortunately, the effective tank Q is quadrupled to be $4Q_0$, resulting in significant improvement on the phase noise [26]. If perfect intrinsic-delay compensation is not required and little phase noise degradation is allowed, then frequency tuning can be achieved by changing the phase of the total injection current i_t, which can be simply implemented by varying the dc current bias I_1 and I_2 of the cross-coupled pairs and the current-injection devices and thus the magnitude of i_b. Mathematically, by summing up the phase of i_t with the phase shift contributed from the *LC* tank and then equating it to zero to fulfill the phase condition mentioned earlier [23], the oscillation frequency can be calculated as

$$\omega = \omega_0 \cdot \left[1 - \frac{i_a \sin(\varphi_d + \varphi_p) - i_b \sin(45^\circ - \varphi_d - \varphi_p)}{i_a \cos(\varphi_d + \varphi_p) + i_b \cos(45^\circ - \varphi_d - \varphi_p)} \cdot \frac{1}{2Q_0}\right] \tag{2}$$

where ω_0 represents the resonant frequency of the *LC* tank. To verify the capability of frequency tuning, SpectreRF simulations are performed. With I_1 fixed and I_2 varied from $0.2I_1$ to I_1, the oscillation frequency can be tuned by ~1.6% while the phase noise degradation is within 1.8 dB.

IV. ILFQ With Forth-Order Harmonic Boosting

The ILFQ is implemented with an injection-locked oscillator whose self-oscillation frequency is around $f_0 = 78$ GHz. As shown in Fig. 4, the ILFQ is composed of a cross-coupled pair (M_1 and M_2) to sustain the self-oscillation and a differential pair (M_3 and M_4) for input injection. Additionally, two transmission lines are used to implement the inductive load while another two are connected to the gate nodes of the cross-coupled pair for impedance transformation, as discussed below. When injection-locked, the ILFQ's oscillation frequency is exactly the same as its input which comes from the HQVCO. By extracting the fourth-order harmonic at the output common-mode node, frequency quadrupling can be realized. Since the injection is at the fundamental frequency f_0 instead of the fourth-harmonic frequency $4f_0$, the issue of frequency alignment between the HQVCO and the ILFQ is greatly alleviated. In the circuit design, power enhancement of the fourth harmonic and efficient delivery to the antenna are the two most critical considerations.

Although the ILFQ oscillates at the fundamental frequency, harmonic currents exist at the outputs of the transistors due to their nonlinear transconductance characteristics. Unfortunately, the desired fourth-order harmonic current is very small. Simulations in SpectreRF indicate that for an NMOS transistor with size of 32μm/60nm, the output current at 312 GHz is only ~0.7 mA when the amplitude of the 78-GHz input is 1 V. Increasing the input voltage amplitude could be one effective way to enhance the output harmonic current at the expense of more power consumption, but the device breakdown would be an issue. In order to identify the underlying limiting factor, it is useful to analyze the harmonic V–I conversion

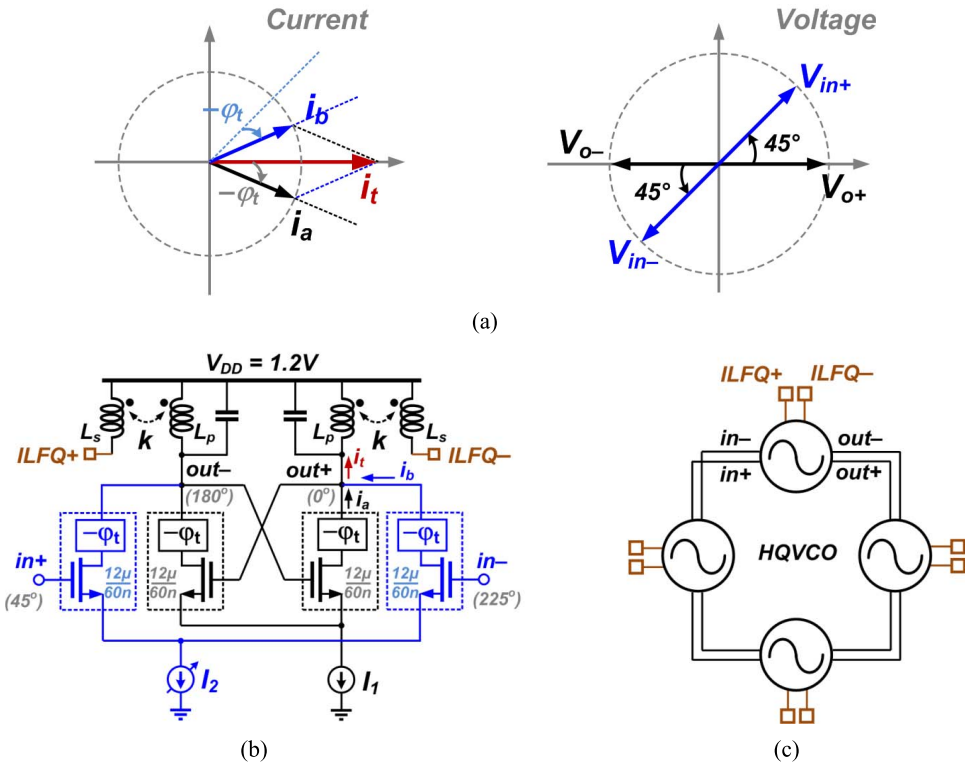


Fig. 3. Proposed HQVCO with intrinsic-delay compensation (a) phasor diagram, (b) schematic of the oscillation cell, and (c) connecting four identical oscillation cells to form a HQVCO for 45° phase.

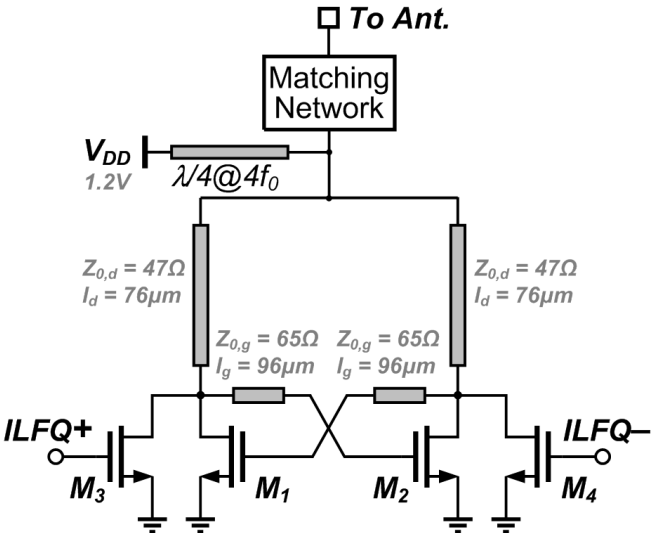


Fig. 4. Schematic of the proposed ILFQ.

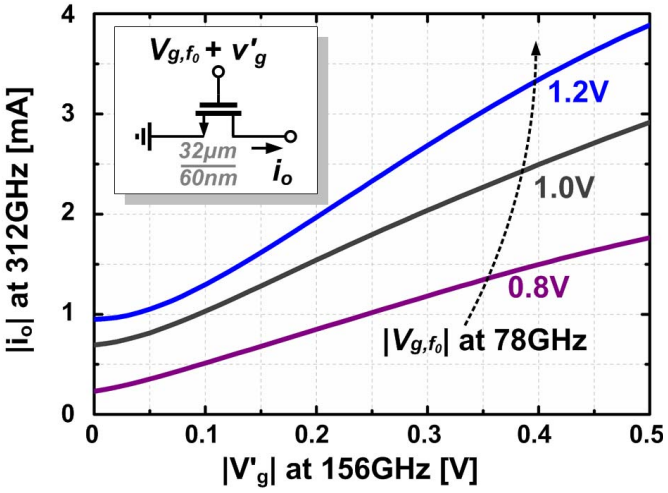


Fig. 5. Simulated output current at 312 GHz versus different $|v'_g|$ at 156 GHz and $|v_{g,f_0}|$ at 78 GHz for an NMOS transistor with size of 32 μm/60 nm acting as a gate-pumped harmonic mixer.

mechanism mathematically. When the ILFQ is oscillating, the cross-coupled transistors are switched ON/OFF and thus their transconductance is periodically modulated. Since the oscillation is at f_0, the transconductance can be expressed by the Fourier series as [29]

$$g_m(t) = \frac{g_0}{2} + \sum_{k=1}^{\infty} g_k \cos\ (2\pi k f_0 t) \tag{3}$$

where g_0 and g_k are the Fourier coefficients. By neglecting the fifth and other higher harmonic terms which are minimal due to their high frequencies, (3) can be approximated as

$$g_m(t) \approx \frac{g_0}{2} + \sum_{k=1}^{4} g_k \cos\ (2\pi k f_0 t). \tag{4}$$

From (4), it can be seen that the nonlinear transconductance can be decomposed into multiple terms with different frequencies. Accordingly, by mixing the fourth-harmonic term with the effective dc voltage at the gate, the desired output

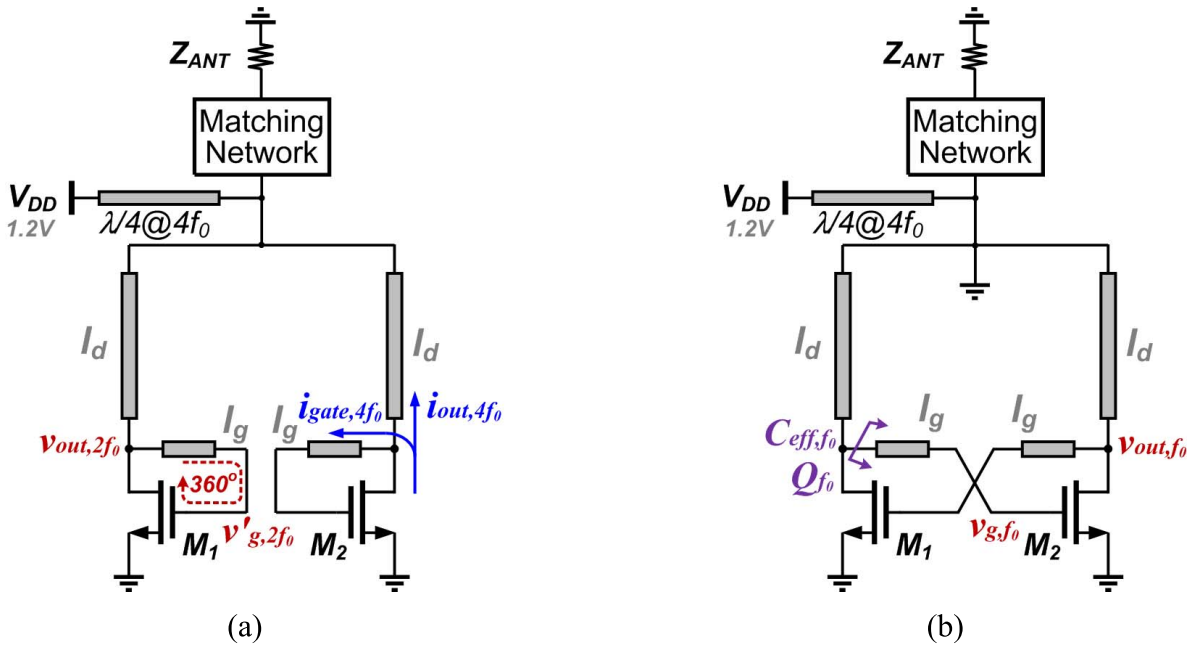


Fig. 6. Equivalent circuit of the ILFQ with $M_{3,4}$ ignored (a) in even mode and (b) in odd mode.

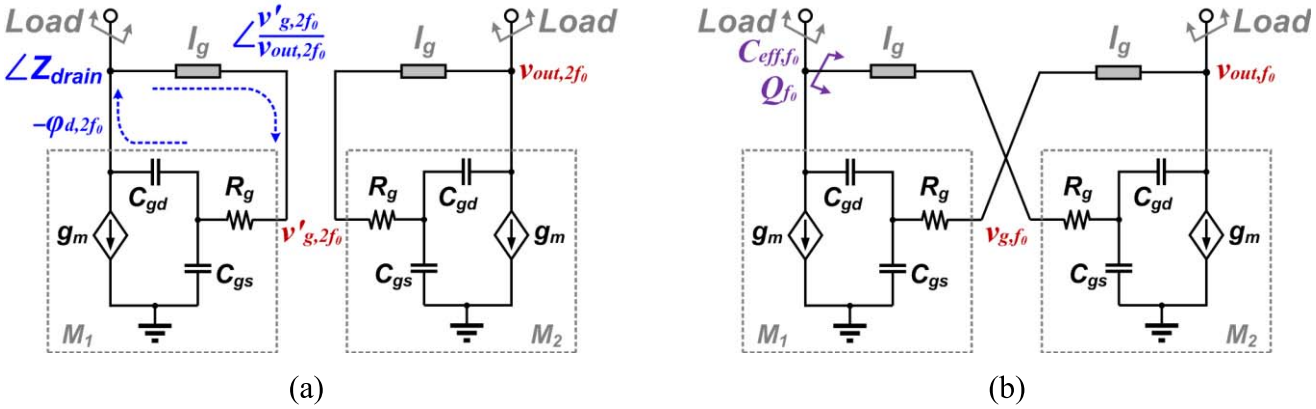


Fig. 7. Simplified model of the equivalent ILFQ circuits in Fig. 6 (a) in even mode and (b) in odd mode.

current $i_{o,4f_0}(t)$ at $4f_0$ is produced. However, as the fourth-harmonic frequency is far above the device's f_T (~180 GHz) and thus g_4 is very small, the resultant mixing product cannot be large. In fact, this is the reason for the extremely low efficiency in generating the fourth-harmonic current at the output. As such, enhancement of the desired output current would have to rely on a more efficient mixing operation. Interestingly, if a voltage signal $v'_g(t)$ with amplitude reasonably lower than the fundamental oscillation is introduced at the gate, then each switching transistor will behave as a gate-pumped mixer [29] such that some additional mixing products are generated as follows:

$$i'_o(t) = g_m(t)v'_g(t) \approx \left[\frac{g_0}{2} + \sum_{k=1}^{4} g_k \cos(2\pi k f_0 t)\right] v'_g(t). \quad (5)$$

Then, by properly choosing the frequency of $v'_g(t)$, an output current at the desired frequency $4f_0$ can be obtained. In order to maximize its amplitude, the device's fundamental limit on the operating frequency should be taken into account. To be more specific, the effective transconductance degrades substantially when the frequency gradually approaches and exceeds f_T. Therefore, any mixing associated with g_3 and g_4 in (5) is not preferred. Undoubtedly, the frequency of $v'_g(t)$ is desired to be lower than f_T also. Otherwise, it would be problematic to generate and sustain $v'_g(t)$ with reasonable amplitude. As a result, the frequency of $v'_g(t)$ is designed to be $2f_0$ and thus the desired harmonic tone from (5) can be derived as

$$i'_{o,4f_0}(t) = g_1|v_g{}'|\cos\ (2\pi f_0 t)\cos\ (2\pi f_0 t + \theta) \quad (6)$$

where $|v'_g|$ and θ denote the amplitude and the phase of the voltage signal $v'_g(t)$, respectively. Assuming $\theta = 0°$ for simplicity, the total output current amplitude of $|i_{o,4f_0}(t) + i'_{o,4f_0}(t)|$ versus different $|v'_g|$ obtained from simulations is plotted in Fig. 5. With $|v'_g|$ of 300 mV, the resulted fourth-harmonic current can be significantly boosted to ~2 mA

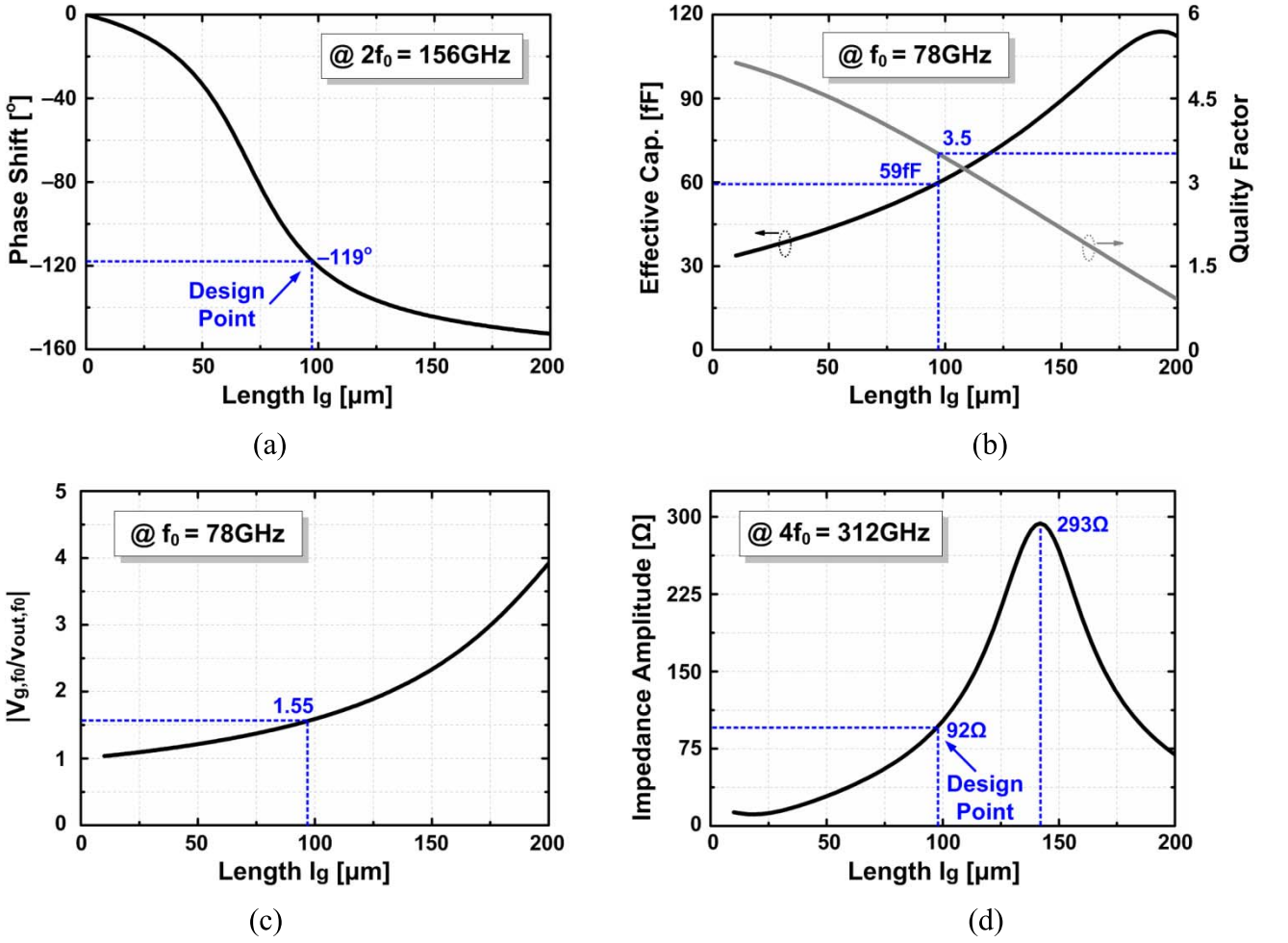


Fig. 8. Optimizing the length of the transmission line l_g in the ILFQ. (a) Phase shift of $\angle\,(v'_{g,2f_0}/v_{\text{out},2f_0})$ at $4f_0$. (b) Effective capacitance looked into the gate from the drain at f_0 (C_{eff,f_0}) and the quality factor (Q_{f_0}). (c) Voltage swing ratio $|v_{g,f_0}/v_{\text{out},f_0}|$ at f_0. (d) Amplitude of the impedance looked into the gate from the drain at $4f_0$.

under the same fundamental oscillation amplitude of 1 V, as compared to the original value of ~0.7 mA mentioned above.

The presence of $v'_g(t)$ can be realized with a positive feedback at $2f_0$ inside the ILFQ. To implement this, two transmission lines are utilized to cross-connect the gate and the drain nodes of the two cross-coupled transistors, as depicted in Fig. 4. At the second harmonic, the circuit operates in even mode and its equivalent circuit is shown in Fig. 6(a). The left and right half-circuits are identical and thus can be connected together. By designing the length of the transmission line (l_g), a 360° loop at $2f_0$ can be formed and thus the positive feedback helps sustain the second-harmonic voltage at the gate of the transistor. Furthermore, the output fourth-harmonic current is optimally delivered to the antenna by conjugate impedance matching between the antenna and the oscillator. Meanwhile, at the fundamental frequency, the ILFQ works in odd mode and the equivalent circuit is depicted in Fig. 6(b). The oscillation frequency should be at f_0 to ensure proper injection-locked operation. Intuitively, with the two different transmission lines designable, both the positive feedback at $2f_0$ and the fundamental oscillation at f_0 could be satisfied simultaneously. In the following paragraphs, the design procedure will be addressed based on detailed circuit analysis.

The loop around the transistor in Fig. 6(a) is composed of three sections: 1) the I–V conversion at the drain; 2) the voltage signal transmission from the drain to the gate; and 3) the V–I conversion by the transconductor. From the simplified model shown in Fig. 7(a), it can be observed that the impedance performing I–V conversion at the drain equals to the impedance looked into the load, the gate, and the drain connected in parallel. Since $|v'_g|$ is desired to be large, the impedance should be around its peak. As such, the phase shift contributed is relatively small and thus can be ignored for simplicity. For the voltage transmission, it can be modeled as a voltage divider and calculated as

$$\frac{v'_{g,2f_0}}{v_{\text{out},2f_0}} = \frac{Z_{g,2f_0}}{Z'_{g,2f_0}} = \frac{Z_{g,2f_0}}{Z_{0,g}} \cdot \frac{1-\Gamma_{g,2f_0}e^{-j2\beta_{g,2f_0}l_g}}{1+\Gamma_{g,2f_0}e^{-j2\beta_{g,2f_0}l_g}} \tag{7}$$

where $Z_{g,2f_0}$ is the gate impedance of the transistor, $\Gamma_{g,2f_0}$ is the reflection coefficient at the gate, $Z'_{g,2f_0}$ represents the equivalent gate impedance seen from the drain, and $Z_{0,g}$, $\beta_{g,2f_0}$, and l_g are the characteristic impedance, the propagation constant, and the length of the transmission line, respectively,

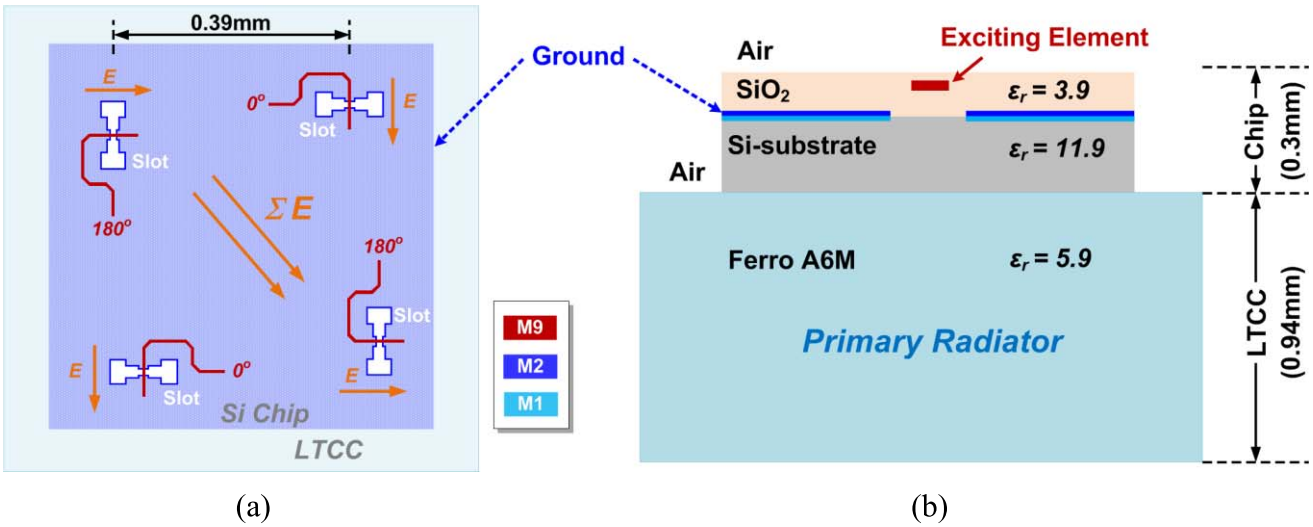


Fig. 9. Proposed antenna with four exciting elements on chip and a primary radiator in LTCC package. (a) Top view. (b) Cross-sectional view.

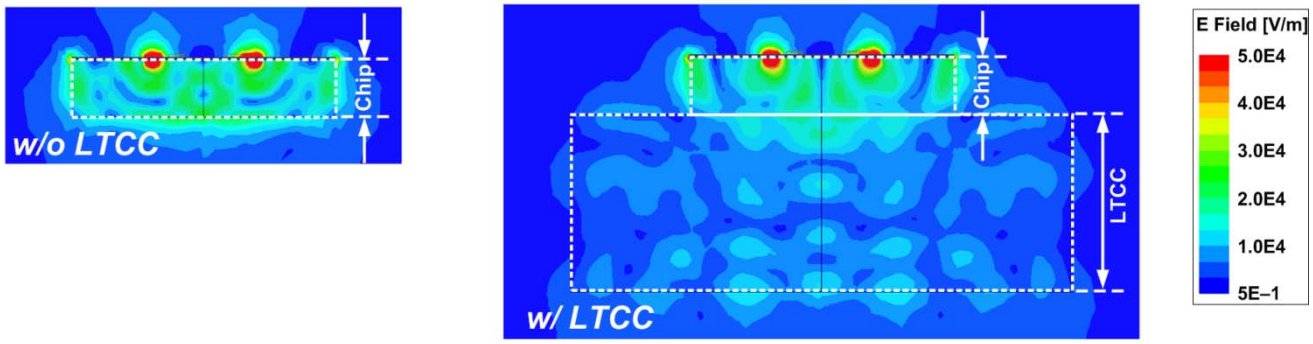


Fig. 10. Simulated complex magnitude of the electric filed before and after attaching the LTCC slab.

all at the frequency $2f_0$. The simulated phase of $v'_{g,2f_0}/v_{\text{out},2f_0}$ versus different l_g is plotted in Fig. 8(a), which indicates that the phase shift can be controlled by adjusting l_g. As mentioned above in Section III, the transistor has intrinsic delay and thus the V–I conversion contributes a phase shift of $(180°-\varphi_{d,2f_0})$, where $-\varphi_{d,2f_0}$ represents the phase delay of the transistor at $2f_0$. Therefore, in order to obtain 360° phase shift along the loop at $2f_0$, the length of the transmission line (l_g) is designed to fulfill $\angle\,(v'_{g,2f_0}/v_{\text{out},2f_0}) = 180° + \varphi_{d,2f_0}$. This is the first step in the design procedure.

Next, the two transmission lines with length of l_d, which behave as inductive loads, are optimized to enable fundamental oscillation at frequency f_0. As shown in Fig. 7(b), in the presence of the transmission line in series with the gate, the impedance transformation would affect the effective gate capacitance C_{eff,f_0} and the equivalent quality factor Q_{f_0}. Simulations show that an increase of C_{eff,f_0} and ~30% Q degradation are induced at f_0, as plotted in Fig. 8(b). Consequently, more power will need to be consumed for oscillation. Fortunately, the Q reduction benefits the locking range of the ILFQ. In addition, the transmission line (l_g) partially resonate with the gate capacitance, resulting in ~50% higher voltage swing at the transistor gate (v_{g,f_0}) compared to that at the output (v_{out,f_0}) as illustrated in Fig. 8(c). Accordingly, a stronger fourth-harmonic current component is generated, as indicated by Fig. 5. Finally, the output impedance seen from the common-mode node at $4f_0$ is conjugately matched to the antenna with the output matching network. The V_{dd} is supplied through a transmission line with length of $\lambda/4$, where λ denotes the wavelength corresponding to the frequency $4f_0$. As the matching network is connected to the common-mode node which appears as ac ground at f_0 and odd harmonic frequencies, fundamental oscillation will not be affected.

As shown in Fig. 6(a), the output fourth-harmonic current from the transistor is divided into two branches, $i_{\text{out},4f_0}$ flowing to the load and $i_{\text{gate},4f_0}$ returning to the gate. Fortunately, the transmission line at the gate significantly boost $|Z_{g,4f_0}|$ to be $|Z'_{g,4f_0}|$, as plotted in Fig. 8(d). Though $|Z'_{g,4f_0}|$ is not the maximum and around ~65% lower, $i_{\text{gate},4f_0}$ is still much smaller than $i_{\text{out},4f_0}$. Surprisingly, owing to the transmission lines which were optimized for the aforementioned positive feedback at $2f_0$, the phase shift around the loop happens to be close to 360° around $4f_0$, which in turn can help recycle part of the fourth-harmonic power fed into the gate. Compared to [11] which attempts to maximize the effective

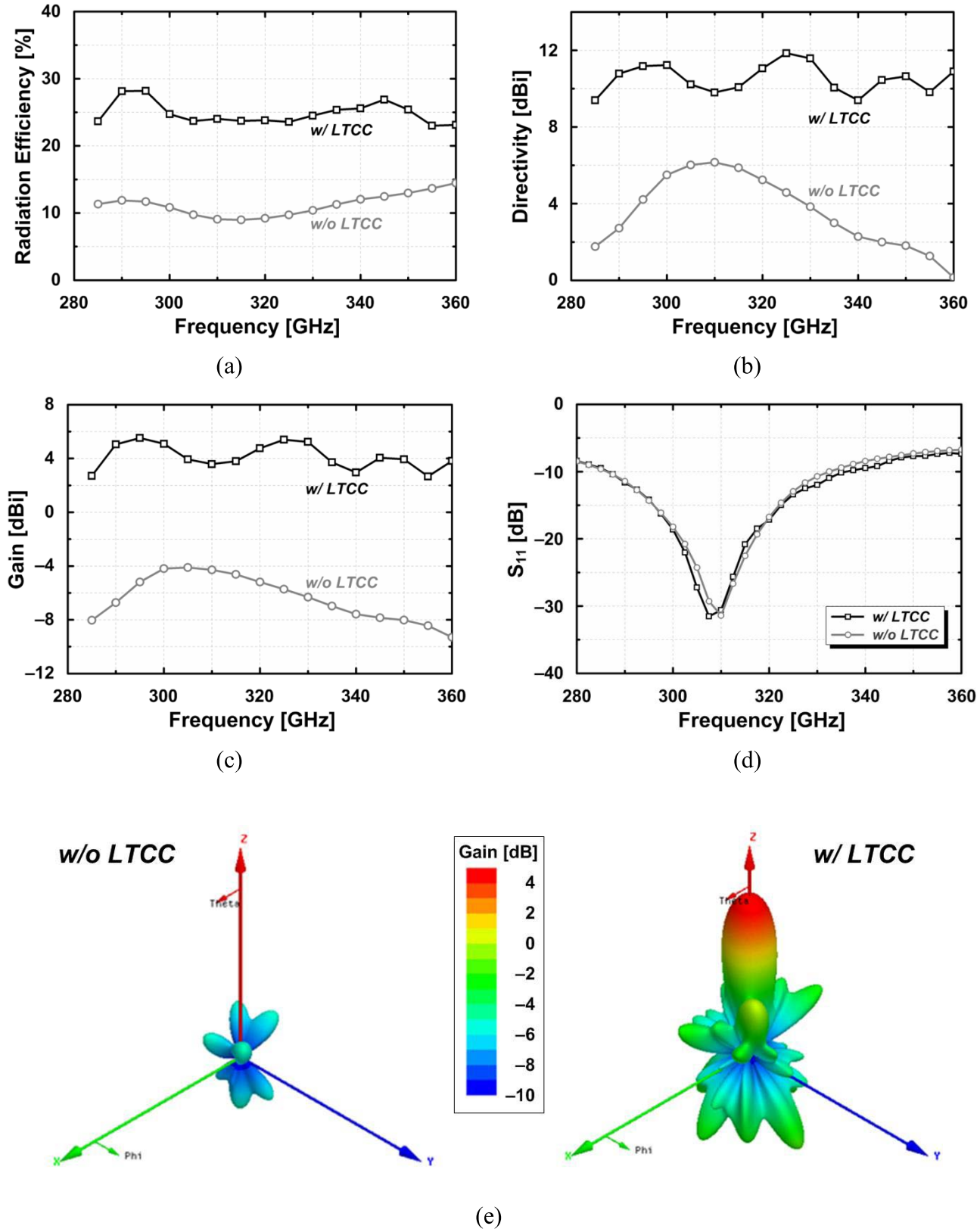


Fig. 11. Simulation results of the antenna before and after attaching the LTCC slab. (a) Radiation efficiency. (b) Directivity. (c) Realized gain. (d) S_{11}. (e) Radiation pattern.

gate impedance by resonating the gate inductance with the capacitance at $4f_0$, the second-order harmonic voltage at the gate is boosted from ~100 mV to ~350 mW with the positive feedback loop at $2f_0$, as obtained from SpectreRF simulations. Consequently, the overall desired output power fed to the antenna is ~4.5 dB higher. At the common-mode

node where the fourth harmonic is extracted, the fundamental tone as well as all of the odd harmonics do not exist due to the differential structure used. For the undesired second-order harmonic at $2f_0$, simulations indicate that the power is ~9 dB higher than the desired tone at $4f_0$ because of its much lower frequency. Therefore, it must be suppressed substantially somehow while being radiated. Fortunately, since the four ILFQs in the radiator system are driven by a HQVCO and thus the phase interval of their second-harmonic outputs is 90° which is different from that of the desired fourth harmonics, the antenna elements can be properly oriented to cancel the unwanted signals at $2f_0$. As discussed later in Section V, the antenna is able to suppress the harmonics at $2f_0$ by 34.5 dB as compared to the desired tone at $4f_0$. Consequently, the radiated power at $2f_0$ is 25.5 dB lower than that at $4f_0$. For the other higher even-order harmonics, they are negligibly small due to the much higher frequencies and the bandpass characteristic of both the matching network and the antenna.

V. Chip-and-Package Distributed Antenna

Theoretically, a high-gain antenna requires large physical aperture size, high aperture efficiency, and high antenna efficiency. At THz frequencies, the wavelength is small such that the physical apertures of on-chip antennas can be reasonably large at the expense of chip area. By properly shaping the radiator, high aperture efficiency can also be obtained. However, on-chip antenna efficiencies are typically low due to the high silicon substrate loss. To mitigate this issue, microstrip patch antennas with ground plate above the substrate are employed in [30] to shield the radiation from penetrating through to the lossy silicon substrate, achieving an efficiency of 21% and a gain of ~5 dBi. However, the achieved bandwidth is narrower than 2.5% because of the close proximity (<8 μm) between the antenna and the ground plate. This paper proposes a novel antenna featuring both large bandwidth and high gain.

For EM wave exciting, an array of four exciting elements based on slot-antenna structure is implemented on chip, each of which is driven by an ILFQ output, as illustrated in Fig. 9(a). A parallel combination of two bottom metal layers M1 and M2 is used for the ground plane where the slots are formed while the top thickest metal layer M9 is for the feedlines to minimize the resistivity. Unlike regular rectangle shapes, the slot in each element is tapered to maximize the bandwidth. Intuitively, this advantage can be understood by approximating the tapered slot as the complementary of a bow-tie antenna which inherently features a wide impedance bandwidth [31]. Symmetrically from the two ends to the center, the width of the three slot segments is designed to be 40, 20, and 10 μm while the length is 26, 21, and 8 μm, respectively. As these segments are all in rectangle shape, the design rules for the metal layers are not violated. Additionally, the slots and the feedlines of the four exciting elements are oriented carefully. As illustrated in Fig. 9(a), the slots of the two elements driven by the 0° phase are placed horizontally and their feedlines are in the same vertical direction. For the other two elements fed by the 180° phase, they can be obtained by a 90° counterclockwise rotation of the above

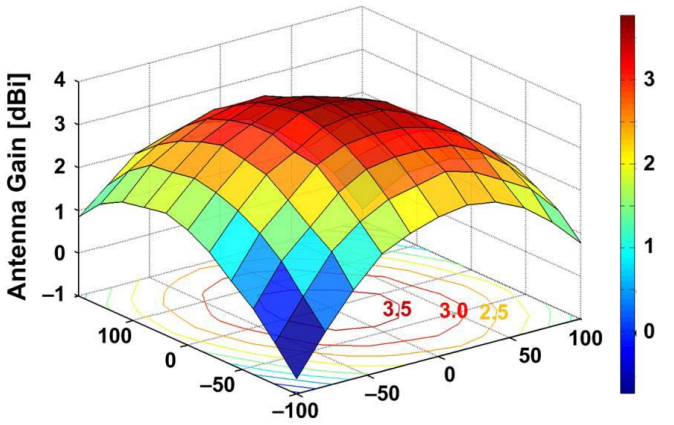


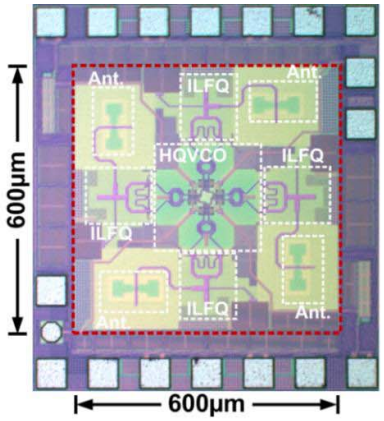
Fig. 12. Simulated antenna gain versus mounting errors along x- and y-axes.

two elements around their center. As such, the 180° phase interval of the driving signals at $4f_0$ is accommodated and their radiated power is constructively combined such that the polarization of the whole array is along a diagonal direction. As a contrary, for the unwanted harmonics at $2f_0$ whose phases are in a sequence of 0°/90°/180°/270°, the radiated power is combined destructively and thus they are suppressed substantially. HFSS simulation indicates that the antenna efficiency is only 9.1% while the gain is limited to −4.7 dBi at 312 GHz, which are mainly attributed to the residence of EM fields inside the lossy silicon substrate as mentioned earlier. If the region housing the EM fields can be extended into a low-loss dielectric, then the power loss in the substrate would be reduced and thus the antenna efficiency could be increased. This idea can be implemented by attaching an LTCC slab onto the silicon substrate, as shown in Fig. 9(b). The slab is made of Ferro A6M material featuring low loss and dielectric constant ϵ_r of 5.9. Before and after attaching the LTCC, the complex magnitude of the electric field in the cross section along the polarization direction is compared in Fig. 10, verifying the effectiveness in re-distributing the EM power and reducing the loss in the silicon substrate. For the slot-antenna structure implemented on chip, the EM waves excited by the slot-antenna structures are radiated bidirectionally from both the top side and the back side. Assuming the thickness of the LTCC slab is much larger than the wavelength in the dielectric, their power ratio can be approximately expressed as [32], [33]

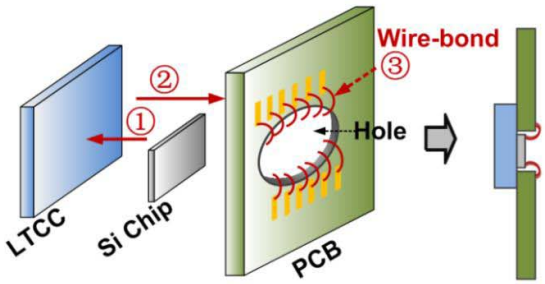
$$\frac{P_{\text{air}}}{P_{\text{diel}}} = \frac{1}{\varepsilon_{\text{eff}}^{3/2}} \tag{8}$$

where P_{air} and P_{diel} are power radiated into the air and into the dielectrics, respectively, and ε_{eff} is the effective dielectric constant of the dielectrics including the silicon substrate and the attached LTCC. From (8), it can be derived that the power radiated into the dielectrics is much higher than that into the air. Therefore, the backside radiation through the substrate and the LTCC is adopted.

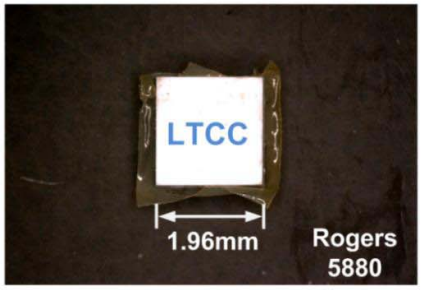
With the exciting elements on chip and the LTCC in package, a DA is formed. The exciting elements work in resonance mode and their excited power is combined within



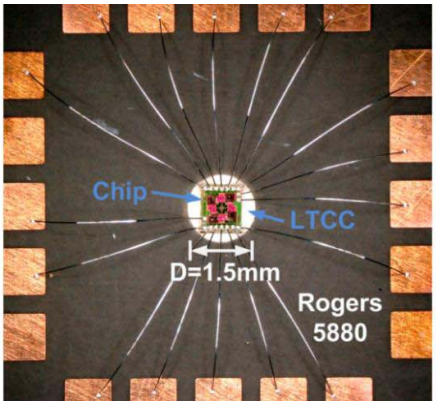
(a)



(b)



(c)



(d)

Fig. 13. (a) Chip micrograph. (b) System packaging procedure. (c) Front side of the radiator system showing the attached LTCC. (d) Back side of the radiator system showing the CMOS chip and the wire-bonding.

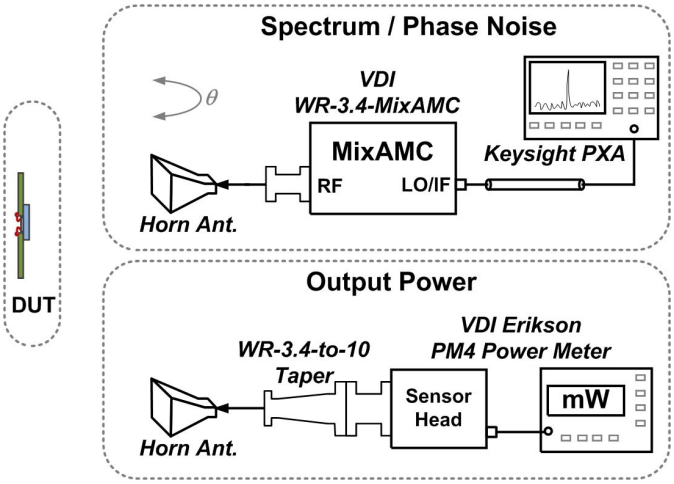
TABLE I

PERFORMANCE SUMMARY OF THE PROPOSED DISTRIBUTED ANTENNA AND COMPARISON WITH EXISTING SOLUTIONS

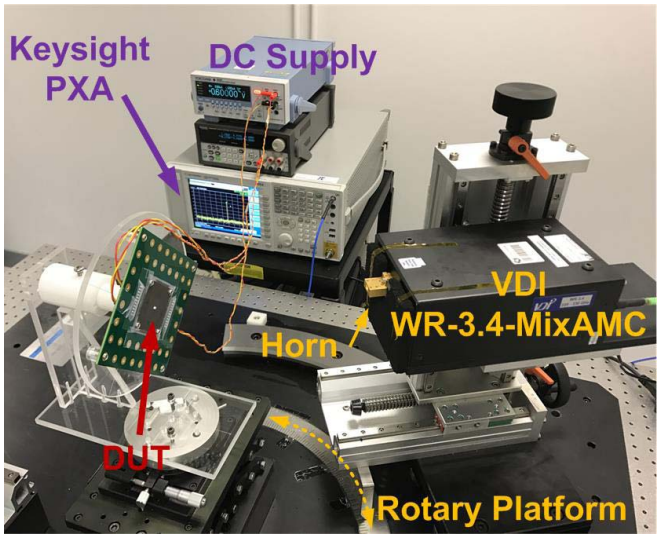
References	[12] JSSC '13	[13] ISSSC '13	[14] JSSC '15	[22] ISSCC '16	This Work
Frequency [GHz]	288	260	338	285	312
Structure	On-chip Diff. Ring + Lens	On-chip Slot + Lens	On-chip Patch	On-chip Loop + metal plated trenches	Chip-and-Package Distributed
Gain [dBi]	18.3 *	7.6 *	6 #	4.5 *	3.0–5.5 *
Radiation Efficiency	65% *	42% *	N/A	40% *	28% *
Bandwidth (–3dB Gain)	N/A	N/A	N/A	56 GHz *	> 75 GHz *
Bandwidth (S_{11} < –10dB)	N/A	60 GHz *	~ 7 GHz *	80 GHz *	~ 45 GHz *
Cost	High	High	Low	High	Medium

* From simulation # Inferred from measurement

the dielectrics. On the other hand, the LTCC simultaneously serves as a directing dielectric to attract the excited EM waves and acts as a primary radiator. Its dimension is optimized such that the EM waves inside are mostly in traveling-wave mode to minimize the loss and to broaden the impedance bandwidth. The performance of the proposed DA obtained

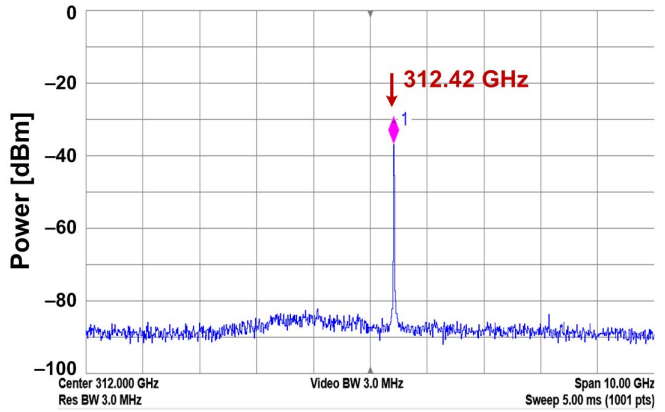


(a)

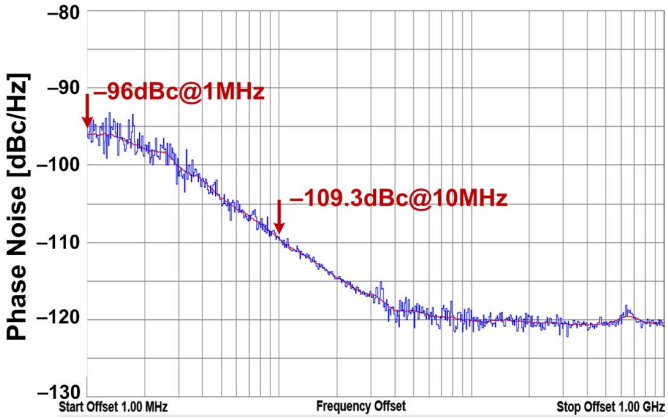


(b)

Fig. 14. (a) Measurement setup for the 312-GHz radiator and (b) using a rotary platform to measure antenna pattern.



(a)



(b)

Fig. 15. (a) Measured output spectrum. (b) Measured phase noise plot.

from HFSS simulations is plotted in Fig. 11. For a frequency range from 290 to 350 GHz, the efficiency is improved to be 23.5%–28%. In addition, the directivity and the realized gain are 9.4 to 11.9 dBi and 3 to 5.5 dBi, as compared with 1.8 to 6.1 dBi and −8 to −4.2 dBi before attaching the LTCC slab, respectively. Meanwhile, since the LTCC is outside the chip, the input matching is negligibly affected. As shown in Fig. 11(d), the S_{11} is below −10 dB for the frequency from 287 to 332 GHz. The simulated radiation pattern before and after attaching the LTCC slab is compared in Fig. 11(e), from which the improvement can be easily identified. To evaluate the performance robustness in the presence of errors when mounting the chip onto the LTCC, parametric simulations are performed and the results are plotted in Fig. 12. For the errors within ±50 μm along both x- and y-axes, the antenna gain at 312 GHz varies from 3.2 to 3.8 dBi. With the antenna fed by four signals whose phase interval is 90°, the simulated gain is as low as −31 to −28 dB in the frequency range from 145 to 175 GHz, demonstrating good suppression to the unwanted second-order harmonics generated by the ILFQs.

With such a distributed configuration, the chip area occupied can be small while the relatively large space and the low-loss material in package are leveraged to enhance the antenna's performance. Compared to Si lenses [12], [13], the manufacturing and assembling of the LTCC is fully compatible with standard IC packaging. Additionally, the antenna can be scaled up by adjusting the LTCC design according to the size of on-chip elements. Table I summarizes the simulated performance of the proposed antenna and compares with existing solutions integrated in THz radiators.

VI. Prototype and Experimental Results

The four-element radiator in Fig. 1 is implemented in a 65-nm CMOS process with one polysilicon and nine metal layers. Fig. 13(a) shows the micrograph of the chip, which occupies a core area of 0.6 × 0.6 mm^2 excluding the pads. The HQVCO is located at the center of the die and surrounded by the four ILFQs while the antenna exciting elements are placed at the four corners. The system packaging is shown in Fig. 13(b). First, the back side of the silicon chip is mounted onto the LTCC slab with size of ∼2 mm× ∼2 mm and thickness of ∼0.94 mm using a non-conductive die attach film adhesive. The thickness of the film is as thin as 10 μm such that it has minimal effect on the radiator system. Second, the LTCC slab together with the chip is glued to a printed circuit

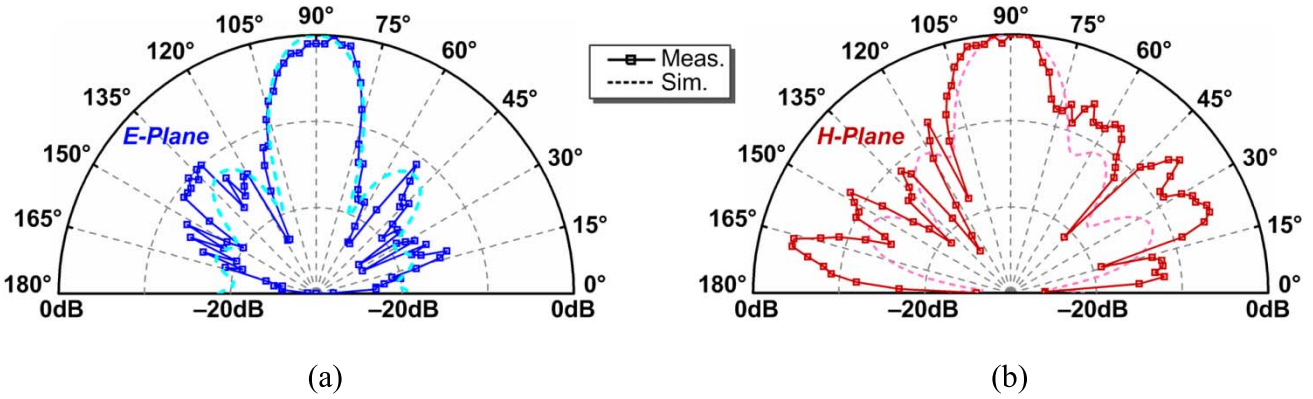


Fig. 16. Measured radiation pattern. (a) E-plane. (b) H-plane.

TABLE II

PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART THz RADIATORS

References	[10] JSSC '12	[12] JSSC '13	[13] ISSSC '13	[14] JSSC '15	[19] ISSCC '15	This Work
Frequency [GHz]	280	288	260	338	317	312
Radiated Power [mW]	0.19	0.38	1.12	0.81	3.3	1.2 †
Element No.	16	1	8	16	16	4
Radiating Element	On-chip Metal Loop **	On-chip Ant. + Lens	On-chip Ant. + Lens	On-chip Ant.	On-chip Ant. + Lens	Chip-and-Package Distributed Ant.
Antenna Gain [dBi]	N/A	N/A	7.6	6	N/A	3.8
EIRP [dBm]	9.4	N/A	15.4	17.1	22.5	10.5
Harmonic Out	2nd	3rd	2nd	4th	2nd	4th
Freq. Tuning [GHz/%] *	3.2 / 1.1	0 / 0	3.6 / 1.4	2 / 0.6	0 / 0	3.9 / 1.3
Phase Noise [dBc]	N/A	–87@1MHz	–78@1MHz	–93@1MHz	–79@1MHz	–96@1MHz –109@10MHz
DC Power [mW]	820	280	800	1540	610	18 (HQVCO) 280 (ILFQs)
DC-to-RF Efficiency [%] #	0.023	0.14	0.14	0.053	0.54	0.42
Area [mm^2]	7.29	0.32	2.25	3.9	2.08	0.36
Technology	45nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	130nm SiGe	65nm CMOS

† Calculated based on simulated directivity * Without tuning the supply voltage

** With wafer thinning # Efficiency = Radiated Power / DC Power

board (PCB) with a hole. The diameter of the hole is sized to be ∼1.5 mm which is slightly larger than the chip, so that the front side of chip is exposed on the other side of the PCB. Finally, the chip is wire bonded to the metal leads on the PCB, where both the dc power and biases are supplied. Since signal is radiated through the backside of the chip, it is not interfered by the bond wires. Fig. 13(c) and (d) shows the top view and the bottom view of the packaging, respectively. The radiator chip consumes 300 mW from a 1.2-V supply.

The measurement setup is illustrated in Fig. 14. The output THz signal from the radiator system is received by a horn antenna with gain of 26.5 dBi. For frequency and phase noise measurement, the received signal is down-converted by a mixer–amplifier–multiplier-chain module (VDI WR-3.4-MixAMC) whose local oscillator input and intermediate frequency output are both connected to a Keysight PXA signal analyzer. The MixAMC module uses the 24th harmonic of the LO for down-conversion, and the undesired tones generated by mixing with other harmonics are automatically identified and not displayed in the PXA. Fig. 15(a) shows the measured spectrum when the radiator output is at 312 GHz. By varying the dc current bias I_2 in

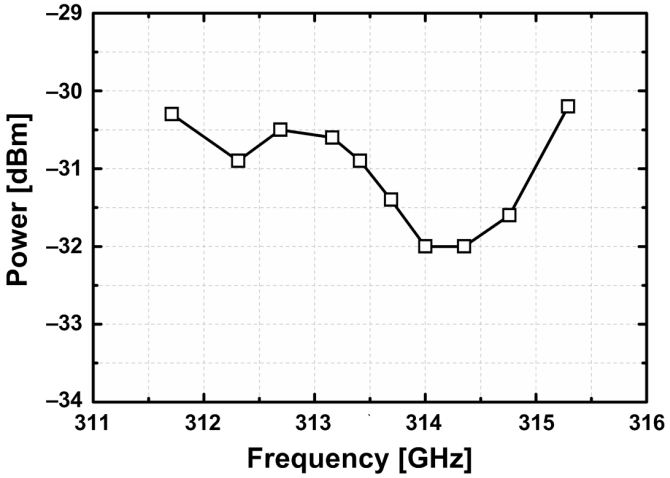


Fig. 17. Measured received power at different frequencies.

the HQVCO, the output frequency is tuned from 311.6 to 315.5 GHz, which corresponds to a 1.3% tuning range. Fig. 15(b) shows the measured phase noise plot, in which the phase noise reads −96 dBc/Hz at 1-MHz offset and −109.3 dBc/Hz at 10-MHz offset. Afterwards, to measure the radiation pattern, the horn antenna and the MixAMC module are mounted on a rotary measurement platform, as illustrated in Fig. 14(b). Fig. 16 shows the measured radiation patterns in the E-plane and H-plane.

Finally, the absolute power received by the horn antenna is measured by an Erikson calorimeter (VDI PM4). As shown in Fig. 14(a), a WR-3 to WR-10 waveguide taper is employed to connect the horn and the sensor head of the PM4. For the horn antenna with an aperture diameter $D_h = 8$ mm, the minimum far-field distance in free space estimated by $2D_h^2/\lambda_0$ [34] is around 13.5 cm, where λ_0 is the wavelength. Accordingly, the horn antenna is aligned to the DUT and placed at a distance of ∼18 cm. Using the Friis transmission formula [35], the maximum EIRP is calculated to be 10.5 dBm. Since the simulated directivity is ∼9.5 dBi as mentioned in Section V, the total radiated power is around 1 dBm (EIRP–Directivity). Accordingly, the dc-to-THz efficiency is 0.42%. Fig. 17 shows the measured received power over the tunable frequency range, indicating variations within ±1 dBm.

In Table II, the performance of the proposed radiator system is summarized and compared with recently published state-of-the-art THz radiators in silicon which are able to generate THz signals without using any off-chip high-frequency input. With EIRP of 10.5 dBm at 312 GHz and frequency range of 1.3%, the radiator in this work achieves the best phase noise of −96 dBc at 1-MHz offset and −109 dBc at 10-MHz offset while the dc-to-THz conversion efficiency of 0.42% is among the highest. In particular, the phase noise at 1-MHz offset is around 3 dB better than state of the arts.

VII. Conclusion

In this paper, a THz radiator system integrating a four-element CMOS source and a chip-and-package antenna is demonstrated. By decoupling the frequency generation and power generation using injection locking architecture at the system level, the proposed intrinsic-delay compensation and harmonic boosting techniques have successfully enabled the system to achieve state-of-the-art performance in terms of phase noise (−109.3 dBc/Hz at 10-MHz offset) and dc-to-THz efficiency (0.42%). In addition, a novel THz antenna which is distributed among the chip and the LTCC package is developed, demonstrating the feasibility and usefulness of leveraging both the low-loss material and the relatively large space in package to overcome the constraints on silicon chips for antenna performance enhancement.

Acknowledgment

The authors would like to thank Dr. K. M. Shum for his support on the measurement setup and the E-PACK Laboratory at The Hong Kong University of Science and Technology, Hong Kong, for the chip packaging.

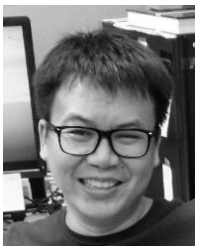
References

[1] P. H. Siegel, "Terahertz technology in biology and medicine," *IEEE Trans. Microw. Theory Techn.*, vol. 52, no. 10, pp. 2438–2447, Oct. 2004.
[2] P. U. Jepsen, D. G. Cooke, and M. Koch, "Terahertz spectroscopy and imaging—Modern techniques and applications," *Laser Photon. Rev.*, vol. 5, pp. 124–166, Jan. 2010.
[3] Z. Wang, P.-Y. Chiang, P. Nazari, C.-C. Wang, Z. Chen, and P. Heydari, "A CMOS 210-GHz fundamental transceiver with OOK modulation," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 564–580, Mar. 2014.
[4] H.-J. Song, J.-Y. Kim, K. Ajito, M. Yaita, and N. Kukutsu, "Fully integrated ASK receiver MMIC for terahertz communications at 300 GHz," *IEEE Trans. THz Sci. Technol.*, vol. 3, no. 4, pp. 445–452, Jul. 2013.
[5] P. H. Siegel, "Terahertz technology," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 3, pp. 910–928, Mar. 2002.
[6] C. M. Armstrong, "The truth about terahertz," *IEEE Spectr.*, vol. 49, no. 9, pp. 36–41, Sep. 2012.
[7] D. Huang *et al.*, "Terahertz CMOS frequency generator using linear superposition technique," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2730–2738, Dec. 2008.
[8] V. Radisic *et al.*, "Demonstration of a 311-GHz fundamental oscillator using InP HBT technology," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 11, pp. 2329–2335, Nov. 2007.
[9] M. Seo *et al.*, ">300 GHz fixed-frequency and voltage-controlled fundamental oscillators in an InP DHBT process," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2010, pp. 272–275.
[10] K. Sengupta and A. Hajimiri, "A 0.28 THz power-generation and beam-steering array in CMOS based on distributed active radiators," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3013–3031, Dec. 2012.
[11] Y. M. Tousi, O. Omeed, and A. Hajimiri, "A novel CMOS high-power terahertz VCO based on coupled oscillators: Theory and implementation," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3032–3042, Dec. 2012.
[12] J. Grzyb, Y. Zhao, and U. R. Pfeiffer, "A 288-GHz lens-integrated balanced triple-push source in a 65-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1751–1761, Jul. 2013.
[13] R. Han and E. Afshari, "A CMOS high-power broadband 260-GHz radiator array for spectroscopy," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3090–3104, Dec. 2013.
[14] Y. Tousi and E. Afshari, "A high-power and scalable 2-D phased array for terahertz CMOS integrated systems," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 597–609, Feb. 2015.
[15] O. Momeni and E. Afshari, "High power terahertz and millimeter-wave oscillator design: A systematic approach," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 583–597, Mar. 2011.
[16] U. R. Pfeiffer *et al.*, "A 0.53 THz reconfigurable source array with up to 1 mW radiated power for terahertz imaging applications in 0.13 μm SiGe BiCMOS," in *IEEE Int. Solid-State Circuit Conf. Dig. Tech. Papers*, Feb. 2014, pp. 256–257.
[17] P. Y. Chiang, Z. Wang, O. Momeni, and P. Heydari, "A silicon-based 0.3 THz frequency synthesizer with wide locking range," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2951–2963, Dec. 2014.

[18] T. Chi, J. Luo, S. Hu, and H. Wang, "A multi-phase sub-harmonic injection locking technique for bandwidth extension in silicon-based THz signal generation," *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 1861–1873, Aug. 2015.
[19] R. Han *et al.*, "A SiGe terahertz heterodyne imaging transmitter with 3.3 mW radiated power and fully-integrated phase-locked loop," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2935–2947, Dec. 2015.
[20] Keysight Inc. *Understanding Phase Noise Needs and Choices in Signal Generation*, accessed on 2012. [Online]. Available: http://www.keysight.com/
[21] H.-J. Song and T. Nagatsuma, *Handbook of Terahertz Technologies: Devices and Applications*. Singapore: Pan Stanford Publishing, 2015.
[22] S. Jameson, E. Halpern, and E. Socher, "A 300 GHz wirelessly locked 2×3 array radiating 5.4 dBm with 5.1% DC-to-RF efficiency in 65 nm CMOS," in *IEEE Int. Solid-State Circuit Conf. Dig. Tech. Papers*, Feb. 2016, pp. 348–349.
[23] S. Rong and H. C. Luong, "Design and analysis of varactor-less interpolative-phase-tuning millimeter-wave LC oscillators with multiphase outputs," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1810–1819, Aug. 2011.
[24] X. Yi, C. C. Boon, J. F. Lin, and W. M. Lim, "A 100 GHz transformer-based varactor-less VCO with 11.2% tuning range in 65 nm CMOS technology," in *Proc. IEEE Eur. Solid-State Circuit Conf.*, Sep. 2012, pp. 293–296.
[25] L. Wu and H. C. Luong, "A 49-to-62 GHz quadrature VCO with bimodal enhanced-magnetic-tuning technique," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 10, pp. 3025–3033, Oct. 2014.
[26] J. V. D. Tang, P. V. D. Ven, D. Kasperkovitz, and A. V. Roermund, "Analysis and design of an optimally coupled 5-GHz quadrature LC oscillator," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 657–661, May 2002.
[27] Q. Huang, "Phase noise to carrier ratio in LC oscillators," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 47, no. 7, pp. 965–980, Jul. 2000.
[28] E. Hegazi, H. Sjoland, and A. A. Abidi, "A filtering technique to lower LC oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1921–1930, Dec. 2001.
[29] R. A. Pucel, D. Masse, and R. Bera, "Performance of GaAs MESFET mixers at X band," *IEEE Trans. Microw. Theory Techn.*, vol. 24, no. 6, pp. 351–360, Jun. 1976.
[30] R. Han *et al.*, "A 280-GHz Schottky diode detector in 130-nm digital CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2602–2612, Nov. 2011.
[31] W. L. Stutzman and G. A. Thiele, *Antenna Theory and Design*, 3rd ed. Hoboken, NJ, USA: Wiley, 2012.
[32] D. B. Rutledge *et al.*, "Integrated-circuit antennas," *Infrared and Millimeter Waves*. New York, NY, USA: Academic, 1983, pp. 1–90.
[33] A. Babakhani, G. Xiang, A. Komijani, A. Natarajan, and A. Hajimiri, "A 77-GHz phased-array transceiver with on-chip antennas in silicon: Receiver and antennas," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2795–2806, Dec. 2006.
[34] C. A. Balanis, *Antenna Theory: Analysis and Design*. New York, NY, USA: Harper & Row, 1982.
[35] H. T. Friis, "A note on a simple transmission formula," *Proc. IRE*, vol. 34, no. 5, pp. 254–256, May 1946.

Liang Wu (S'10–M'13) received the B.S. and M.S. degrees in materials science from Fudan University, China, in 2004 and 2007, respectively, and the Ph.D. degree in electronic and computer engineering from The Hong Kong University of Science and Technology, Hong Kong, in 2012.

Since 2013, he has been with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, as a Research Assistant Professor and served as the Deputy Director of HKUST-Qualcomm Joint Innovation and Research Laboratory. Since 2015, he has been a Senior Research Fellow with the State Key Laboratory of Millimeter Waves, City University of Hong Kong, Hong Kong. His current research interests include RF and millimeter-wave integrated circuits and systems for wireless applications, CMOS-integrated terahertz systems, and mixed-signal system-on-chip for visible light communications.



Shaowei Liao (M'13–SM'16) received the Ph.D. degree in electromagnetic fields and microwave technology from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2010.

From 2007 to 2009, he was a Research Assistant with the Department of Electronics, Carleton University, Ottawa, ON, Canada. In 2011, he was a Lecturer with the School of Electronic Engineering, UESTC, Chengdu. From 2011 to 2012, he was a Senior Research Associate with the Department of Electronic Engineering, City University of Hong Kong, Hong Kong. From 2012 to 2013, he was a Research Scientist with the Bell Labs Research China, Alcatel-Lucent Shanghai Bell Co., Ltd., Shanghai, China. He is currently an Engineer with the State Key Laboratory of Millimeter Waves, City University of Hong Kong, Hong Kong. He has authored or co-authored more than 20 internationally referred papers on IEEE journals. He is a Co-Inventor of five granted US/European/international patents, in addition with six filed patents. His current research interests include various antennas, computational electromagnetics, microwave components, and metamaterials.

Dr. Liao is the reviewer for the IEEE TRANSACTIONS ON ANTENNAS AND PROPAGATION, the IEEE ANTENNAS AND WIRELESS PROPAGATION LETTERS, and the IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS.

Quan Xue (M'02–SM'04–F'11) received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 1988, 1991, and 1993, respectively.

In 1993, he joined the UESTC, Chengdu, as a Lecturer, and became a Professor in 1997. From 1997 to 1998, he was a Research Associate and then a Research Fellow with The Chinese University of Hong Kong, Hong Kong. In 1999, he joined the City University of Hong Kong, Hong Kong, where he is currently a Chair Professor of Microwave Engineering. From 2011 to 2015, he served the City University of Hong Kong as the Associate Vice President (Innovation Advancement and China Office) and is currently the Director of Information and Communication Technology Center, and the Deputy Director of the State Key Laboratory of Millimeter Waves. He has authored or co-authored over 300 internationally referred journal papers and over 130 international conference papers. He is Co-Inventors of five granted Chinese patents and 15 granted US patents, in addition with 26 filed patents. His current research interests include microwave/millimeter-wave/THz passive components, active components, antenna, and microwave monolithic integrated circuits (MMIC and radio frequency integrated circuits).

Prof. Xue served the IEEE as an AdCom Member of MTT-S from 2011 to 2013. He was the Associate Editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES from 2010 to 2013, the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS from 2010 to 2015, and the IEEE TRANSACTIONS ON ANTENNA AND PROPAGATIONS in 2016, and the Editor of the *International Journal of Antennas and Propagation* from 2010 to 2013.