A 5.28-Gb/s LDPC Decoder With Time-Domain Signal Processing for IEEE 802.15.3c Applications

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***Abstract*— This paper presents a high-throughput, energy-efficient, and scalable low-density parity-check (LDPC) decoder with time-domain (TD) signal processing. The proposed arbiter-based minimum value finder is able to support practical long codes. The latency for determining the first two minimum values required in the check node unit is significantly reduced through TD processing. A layered *Q*-based decoding architecture together with the associated scheduling is proposed in order to reduce the amount of memory used for check node storage. Multimode operations are supported by leveraging the structure of the base matrices and the proposed scalable minimum finder architecture. As a proof of concept, a TD-based multimode LDPC decoder for high-speed IEEE 802.15.3c is designed and fabricated in a 90-nm CMOS process. The LDPC decoder integrates 495k logic gates in 2.25 mm^2 and achieves a throughput of 5.28 Gb/s at 157 MHz from a 1.05 V supply voltage. The power and normalized energy dissipation are 182 mW and 34.47 pJ/b, respectively. The proposed LDPC decoder is more hardware and energy efficient than previous digital counterparts and is able to support long codes for practical applications, which is still infeasible for the state-of-the-art TD-based LDPC decoders.**

***Index Terms*— CMOS integrated circuits, IEEE 802.15.3c, layered scheduling, low-density parity-check (LDPC) code, time-domain (TD) signal processing, wireless personal area network.**

I. Introduction

LOW-DENSITY parity-check (LDPC) codes [1], [2] have become increasingly popular since these codes are able to approach the Shannon limit and high-throughput decoders are realizable. Many commonly implemented communication standards, such as the IEEE 802.15.3c (wireless personal area network), IEEE 802.11ad (WiFi), and IEEE 802.3 (10 GBASE-T) standards, include LDPC codes, where gigabytes per second throughput is required. In order to achieve a high throughput, high-parallelism decoder architectures [3]–[9] can be used to reduce the critical path of the decoder. For decoders based on the normalized min-sum (NMS) algorithm [10], the critical path usually occurs in the minimum value and index generator (MVIG), which determines the first two minimum values and the associated first minimum index. Consequently, Kumawat *et al.* [7], Lee *et al.* [11], and Wey *et al.* [12] focused on efficient algorithms and architectures for the MVIG. To avoid the complexity involved in finding the second minimum, modified NMS algorithms were used in [11]–[13]; nevertheless, these methods will result in a loss in bit error rate (BER) performance. It is worth noting that each of the methods mentioned above was realized using digital processing.

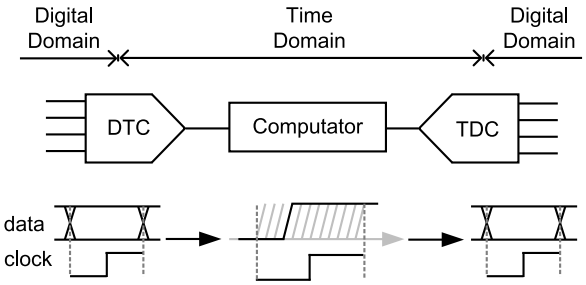

Fig. 1. Conceptual view of TD signal processing. The signal is processed in the TD so as to enhance the processing speed.

Compared with digital processing, analog processing is more area and energy efficient. As a result, analog LDPC decoders were proposed in [17] and [18]. However, it has been observed that analog computation has some limitations. First, digital-to-analog converters and analog-to-digital converters must be inserted as the interfaces, which consequently reduces the area efficiency gain from implementing analog processing. Second, reducing mismatch issue is necessary, consequently resulting in a larger area overhead and higher power consumption. Third, analog computation does not offer any increased benefit from the current electronic design automation (EDA) flow for VLSI systems. Without the aid of EDA tools, the scalability of analog LDPC decoders is limited.

To address these issues, Miyashita *et al.* [19] proposed an LDPC decoder architecture that was implemented based on time-domain (TD) processing. Fig. 1 shows the basic concept, where the digital-to-time converter (DTC) and the time-to-digital converter (TDC) are used as the interfaces. The TD-based approach is applicable to LDPC decoding algorithms where some inaccuracies and mistakes are acceptable. However, since only the first minimum value can

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be determined using the TD minimum value finder (MVF) proposed in [19], a degree-d_c check node unit (CNU) must be implemented using d_c TD MVF, consequently limiting any scalability of the decoder. As demonstrated in [19], only a single-mode short (32, 24) LDPC code can be processed.

In this paper, we propose an efficient TD-based MVIG that has a shorter latency and a smaller area compared with the digital implementations proposed in [7], [11], and [12]. Since each CNU only requires a single MVIG, the limitations to scalability encountered in [19] are avoided. Moreover, the TDC is not required in the proposed MVIG, and hence the matching problem between DTC and TDC is also prevented. Matching between multiple signals in TD is ensured through extensive Monte Carlo simulations and careful place and route. In order to achieve a high throughput, parallel block-row layered scheduling is adopted so as to update each layer in a single cycle. The pipelining technique, which can reduce the critical path of the CNU, is not an option here because of the data dependency between layers. We also propose a modified layered decoder architecture together with the associated scheduling such that the memory required for check node storage can be reduced by one layer. In order to demonstrate the scalability of the proposed techniques, we design a TD-based layered decoder chip for IEEE 802.15.3c applications, where four codes with length 672 are supported. This chip was fabricated using a 90-nm CMOS process and can operate at a clock frequency of 157 MHz from a 1.05 V supply voltage. A maximum (MAX) throughput of 5.28 Gb/s can be achieved with a power consumption of 182 mW. Compared with the analog and TD decoders presented in the previous literature, the proposed TD decoder architecture is able to support long codes in practical communication systems. Compared with the digital decoders presented in the previous literature, the proposed TD decoder achieves greater hardware and energy efficiencies.

The remainder of this paper is organized as follows. A review of the NMS-based layered LDPC decoding and CNU implementations is provided in Section II. The proposed TD-based CNU and the optimization methodology are described in Section III. The proposed multimode layered decoder architecture and associated scheduling are discussed in Section IV. The results of the chip implementation are presented in Section V. Finally, Section VI concludes this paper.

II. Review of Layered LDPC Decoding

A. NMS-Based Layered LDPC Decoding

In layered decoding [3], [20], the parity-check matrix (PCM) is horizontally divided into L layers. The messages are updated between variable nodes and check nodes layer by layer. After the messages in the same layer are completely updated, the decoding process for the next layer can begin. The *a posteriori* log likelihood ratio (LLR) for the nth variable node is denoted by Λ_n. The check to-variable (C2V) message from the mth check node to the nth variable node and the variable-to-check (V2C) message from the nth variable node to the mth check node are denoted by R_{mn} and Q_{mn}, respectively. The NMS-based layered decoding technique is presented as follows.

Initialization: The *a posteriori* LLR values for all the received code bits are equal to the channel LLR values. At the same time, all the C2V and V2C values are reset.

Iterative Decoding: The message updating and syndrome checks are executed iteration by iteration and layer by layer until the decoded word satisfies all the parity-check equations or the MAX number of iteration ($I_{\max}$) is reached. The operations for the ith iteration, $1 \le i \le I_{\max}$, and the gth layer, $(0 \le g \le L-1)$, are detailed as follows.

1) *V2C Updating:* For each variable node (VN) n involved in the gth layer, compute $Q_{mn}^{(i,g)}$ corresponding to each of its check node neighbors m in the gth layer according to
$$Q_{mn}^{(i,g)} = \Lambda_n - R_{mn}^{(i-1,g)}. \tag{1}$$
2) *C2V Updating:* For each check node m in the gth layer, compute $R_{mn}^{(i,g)}$ corresponding to each of variable node neighbors n, i.e., $n \in N(m)$, according to
$$R_{mn}^{(i,g)} = \alpha \times S_{mn}^{(i,g)} \times \min_{n' \in N(m)\backslash n} (|Q_{mn'}|) \tag{2}$$
$$S_{mn}^{(i,g)} = \prod_{n' \in N(m)\backslash n} \operatorname{sgn}(Q_{mn'}^{(i,g)}) \tag{3}$$
where $0 < \alpha < 1$ is a normalization factor.
3) *LLR Updating:* For each variable node n involved in the gth layer, compute Λ_n corresponding to each of its check node neighbors m in the gth layer according to
$$\Lambda_n = Q_{mn}^{(i,g)} + R_{mn}^{(i,g)}. \tag{4}$$
4) *Hard Decision and Syndrome Calculation:* At the end of the processing for each layer, a hard decision for each VN is made based on the sign of the *a posteriori* LLR and then the syndrome values are calculated.

It can be seen that the up-to-date V2C messages can be used in the C2V updating and hence the convergence rate can be increased. Compared with the flooding scheduling used in [6] and [19], layered decoding is able to achieve twice the convergence rate in error performance.

B. Check Node Unit

The C2V message can be calculated directly from (2) and (3). That is, an MVF that can determine the minimum value among $d_c - 1$ V2C magnitudes and a $(d_c - 1)$-input XOR gate are required, where $d_c = |N(m)|$. This direct calculation method can be efficiently realized using analog or TD circuits [17]– [19]. However, for a degree-d_c check node, (2) and (3) must be executed d_c times in order to yield d_c C2V messages, and hence, the computational complexity involved for each check node is high. In addition, each C2V message R_{mn} must be stored, resulting in a large area overhead. As a result, the scalability of the architecture proposed in [17]–[19] is limited. Consequently, the analog and TD decoders presented in [17]–[19] were only realized for a very short LDPC code, e.g., (32, 8) code.

It can be seen from (2) that $|R_{m,n}^{i,g}|$, $n \in N(m)$, is either $\alpha M1$ or $\alpha M2$, where $M1$ and $M2$ denote the first and second

minimum values among d_c V2C magnitudes, respectively. If $M1$, the index of $M1$ (Idx1), and $M2$ can be efficiently determined, the complexity involved in calculating the d_c C2V magnitudes can be significantly reduced. In addition, it can be seen from (3) that if the total sign of the d_c V2C signs are determined first, then the sign of each C2V sign can be determined using a two-input XOR gate. A major challenge when using this indirect calculation approach for high-throughput designs is the need to find the first two minimum values from d_c inputs within a single cycle. To address this issue, Kumawat *et al.* [7], Lee *et al.* [11], and Wey *et al.* [12] proposed solutions based on digital logic. After calculating the C2V messages, either the direct C2V message R_{mn} or the compressed messages (including $M1$, Idx1, $M2$, and the total sign) can be stored. The direct storage method has the advantage of having a shorter critical path, but at the cost of requiring a larger storage area compared with the compressed storage method [3]. Taking the IEEE 802.15.3c rate-7/8 LDPC code as an example, if the compressed-storage method is used, only 40% of the storage area is required compared with if the direct storage method is used. However, the compressed storage method creates an additional latency of 1.4 ns in a 90-nm CMOS process based on synthesis estimates.

III. TD-Based CNU

The computational complexity and memory storage of the CNUs can be significantly reduced by an approach based on the indirect calculation and compressed storage. However, realization of these two approaches based on digital logic inevitably results in a long critical path, thereby limiting the decoder throughput. An indirect-calculation-based CNU design with TD signal processing is proposed in order to reduce the critical path. Integrated with the compressed-storage approach, the proposed TD-based CNU can be used to realize high-throughput and area-efficient decoders with a large code length.

A. Conventional TD-Based MVF

The TD-based MVF presented in [19] is based on the concept shown in Fig. 1, where the DTC and the TDC are used as interfaces between the TD and digital domain. The circuit diagram of an atomic DTC is shown in Fig. 2(a). When clk switches from low to high, the DTC unit converts a digital signal V_{in} into a TD signal T_{out}. Functionally, the clk signal propagates over the DTC unit through two possible paths according to the value of the binary input V_{in}. When $V_{in} = 0$, the clk signal passes through a path that does not contain a delay cell (DLY). In contrast, when $V_{in} = 1$, the clk passes through a path that contains a DLY, where an additional latency of T is introduced by the DLY. A k-b DTC consists of k cascaded atomic DTC with respective delays of $1T, 2T, \ldots,$ and $2^{k-1}T$. The series connection of such k DLYs creates 2^k distinct time delays that are controlled by the k-b input V ($V[k\text{-}1{:}0]$), as shown in Fig. 2(b).

Fig. 2(c) shows the MVF for the LDPC decoder presented in [19] for d_c inputs. Only the *fastest* DTC output, which is generated from the minimum k-b V_i, can propagate through the OR gate and will be converted back into a digital value through a TDC. This MVF can be used to realize a direct-calculation-based CNU, but it is not able to support a compressed storage method. This limits the scalability of the decoder. For an LDPC decoder with a large number of the TDCs, the TDC clock inputs introduce extra clock loading. For the most important reason of all, the MVF presented in [19] is not suitable for indirect-calculation-based CNUs since the associated index of the minimum value is not propagated.

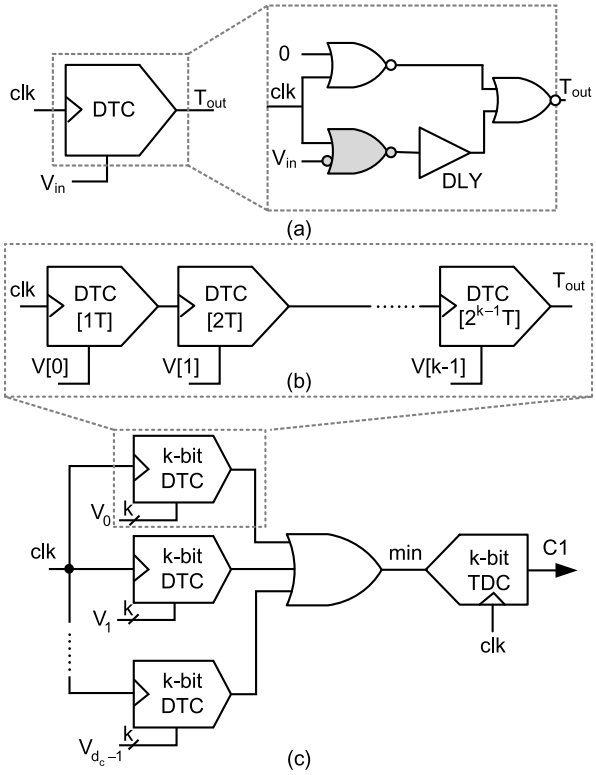

Fig. 2. (a) Atomic DTC. (b) k-b DTC, where [T] indicates the delay of the associated DLY. (c) MVF proposed in [19].

B. Proposed TD-Based MVIG

An MVIG that supports indirect-calculation-based CNUs is proposed. In addition to $M1$, the index of $M1$ and $M2$ are also found. The index of $M1$ can be extracted using an arbiter circuit, which can be used for detecting the leading input. As shown in Fig. 3(a), Idx indicates which input arrives first ("1" for B and "0" for A). A two-input TD comparator can be constructed by integrating two DTCs and one arbiter, as shown in Fig. 3(b). If V_1 is larger than V_0, $Idx = 0$; otherwise, $Idx = 1$. Fig. 3(c) shows the simulation waveforms of the two-input TD comparator in a 90-nm CMOS process. The concept can be extended to identify the index of the minimum value among multiple inputs. Fig. 3(d) shows the circuit for the proposed minimum-index generator. The output of the OR gate becomes high when any of its input signals becomes high. The d_c arbiters compare the arrival time between the min and the d_c DTC outputs in parallel in order to find the index of the minimum value among d_c inputs. Therefore, $Idx[d_c\text{-}1{:}0]$ can be used as an index indicator for the minimum value. For example, $Idx[0] = 1$ indicates that the minimum value is V_0.

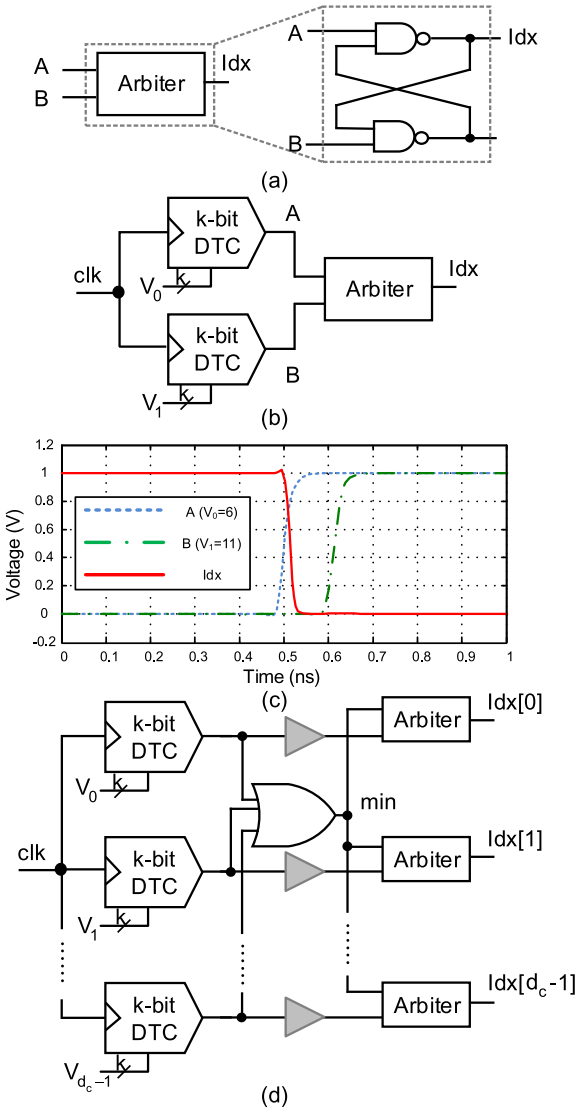

Fig. 3. (a) Arbiter circuit diagram. (b) Block diagram of a two-input TD comparator. (c) Simulation waveforms of the two-input TD comparator. (d) Block diagram of the minimum index generator with d_c inputs. The matching cells are shaded in gray.

Since the d_c input OR gate in Fig. 3(d) itself introduces a delay, matching DLYs (shaded in gray) are inserted into other paths to balance the delay of all paths. However, a careful investigation shows that the matching delay has to be slightly smaller. When both input signals of the arbiter rise from 0 to 1 simultaneously, this causes metastability and the arbiter spends an extended time to return to a stable state. To avoid metastability, the arrival times of the two inputs with the same value are slightly offset. Distinct loadings of the two inputs of the arbiter lead to different signal slopes. Note that the metastability is actually mitigated if different input signal slopes exist. The unit delay T is set to 60 ps. According to simulation, the timing offset of the two inputs must be at least 10 ps in the worst case.

An MVIG that can yield $M1$ and $M2$ and the associated indices ($Idx1$ and $Idx2$) from the d_c inputs is constructed on the minimum index generator shown in Fig. 3(d). Fig. 4(a) shows the proposed MVIG. The flag $Idx1[d_c\text{-}1{:}0]$ in the first arbiter array is used to mask the signal that has the minimum value through an AND array. Then, the second arbiter array is used to determine $Idx2[d_c\text{-}1{:}0]$, which is an index indicator for $M2$. With the $M1$ and $M2$ indices provided by $Idx1[d_c\text{-}1{:}0]$ and $Idx2[d_c\text{-}1{:}0]$, the values of $M1$ and $M2$ can be easily determined by using the minimum value selector, as shown in Fig. 4(b). These operations can be performed efficiently within one cycle due to message parallel processing. It is worth noting that $M1$, $M2$, and $Idx1$ are represented in a digital format, meaning that accurate TDCs are not required here. This eliminates the need for the device matching between the TDC and the DTC that is encountered by the existing TD-based MVF [19]. In order to ensure the functionality, the unit delay in TD-MVIG must be two times larger than the delay variation itself. As shown in Fig. 5, the DLY cell has the shortest delay 54 ps ($T = 60$ps) and the delay variations of 8.21 ps through Monte Carlo simulation. A larger process variation is expected at a more advanced technology node. A relatively larger unit delay [normalized to the associated fanout-of-4 (FO4) delay] has to be chosen to mitigate the variation.

C. Area- and Time-Efficient MVIG

The area and latency of the proposed MVIG is dominated by the k-bit DTC arrays, especially for a large k. For a k-b DTC, as shown in Fig. 2(b), the DLY associated with the MSB (most significant bit) dominates the area and latency. In this paper, the k-b DTC array in Fig. 4(a) can be replaced by a $(k-1)$-b DTC array so as to significantly minimize both the area and the delay by leveraging the MSB characteristic of the d_c inputs that are used for finding Idx1 and Idx2.

Fig. 6(a) shows the proposed $(k-1)$-b DTC array. The functionality of the TD comparator here is to inspect whether $N_0(d_c) \geq 2$ in the TD. That is, the TD comparator counts the number of 0s in the MSB of the d_c inputs and detects whether the number is larger or equal to 2. Compared with the general TD comparator [as shown in Fig. 3(b)], this TD comparator is designed only for comparing with one. Therefore, the k-b DTC (in Fig. 2) is replaced with one 1T DTC in the second path. Inverse inputs (as indicated with bubbles) are required to ensure the functionality since the number of 0s, rather than 1s, is compared. Matching delays in the second branch are required to balance the delay of two branches. R_{DET} is the signal to indicate if the comparison result is valid (i.e., $R_{\mathrm{DET}} = 1$ if $N_0(d_c) \geq 2$; otherwise, $R_{\mathrm{DET}} = 0$). It is used to mask the paths in which the signals have longer delays than M_1 and M_2. If $N_0(d_c) = 0$, the MSB of each input (V[MSB]) is 1, which is redundant for finding Idx1 and Idx2. After being converted into the TD T_{out}, all the inputs propagate to the succeeding Min1 and Min2 finders, as depicted in Fig. 4(a). If $N_0(d_c) = 1$, the input where MSB $= 0$ is $M1$, and $M2$ is the *minimum value* in the remaining $d_c - 1$ inputs. A fast signal R_{Det} propagates through the multiplexer to indicate Idx1 in the following Min1 finder. Then Idx2 will be successfully found in the Min2 finder. Fig. 6(b) shows the timing diagram of the modified DTC array with four inputs, where V_1 (0100) is $M1$ and V_3 (1000) is $M2$.

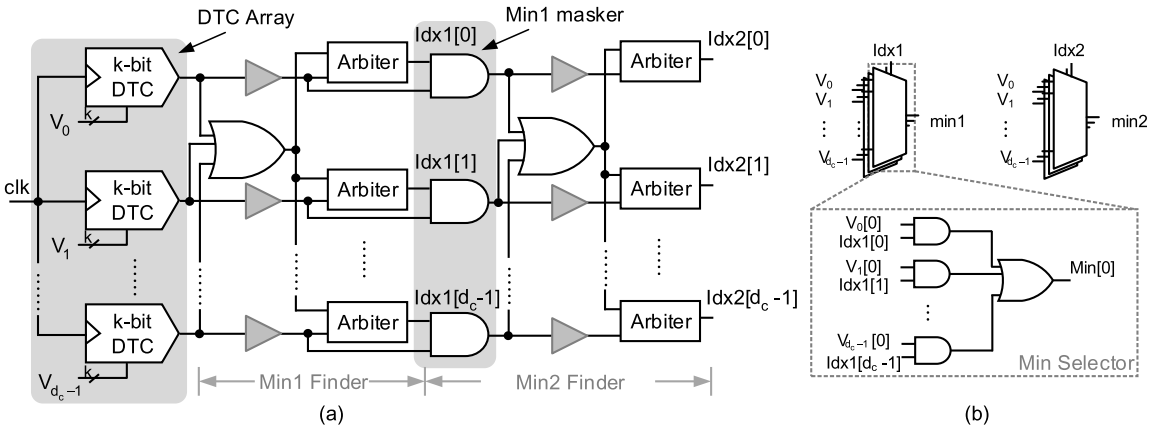

Fig. 4. Architecture for the proposed MVIG. (a) Minimum index generator. (b) Minimum value selector.

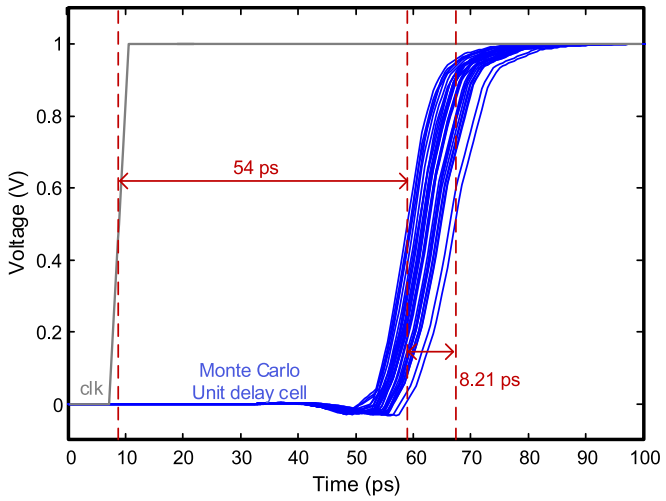

Fig. 5. Delay variation of the unit DLY through Monte Carlo simulations.

If $N_0(d_c) \geq 2$, only the inputs with MSB $= 0$ need to be considered as candidates of $M1$ and $M2$ and need to be propagated to the succeeding Min1 and Min2 finders; the others can be masked by setting the corresponding DTC output signals (Slt) to zero. The functionality of the k-b DTCs is retained using only $(k-1)$-b DTCs through the masking technique, reducing the largest delay element from $2^{(k-1)T}$ to $2^{(k-2)T}$. The signal mapping for the proposed DTC array is summarized in Table I.

The area and latency of the DTC array can be reduced by 18.9% and 52%, respectively, when $d_c = 32$ thanks to the removal of the largest cells for MSB in the 4-b DTC array. The inverters for $d_c + 1$ 1T DTC cells in the TD comparator, as shown in Fig. 6(a), can be further removed by replacing the shaded cell in the DTC cell, in Fig. 2(a), with an NOR gate to achieve the same functionality. This reduces the area required for the TD comparator by 22%.

Table II shows a comparison between the circuit area and the critical path delay for the proposed MVIG and [7], [11], and [12]. The values of the area and the delay are either cited as reported or estimated. The TD-based MVF [19] is not included for comparison since it is only able to yield $M1$.

TABLE I
SIGNAL MAPPING FOR THE MODIFIED DTC ARRAY

$N_0(d_c)$	R_{Det}	V[MSB]	XNOR output	Slt
< 2	1	0	0	R_{Det}
		1	1	T_{out}
≥ 2	0	0	1	T_{out}
		1	0	0

TABLE II
COMPARISON AMONG MVIGS (IN 90nm CMOS) FOR THE REJECTION-BASED SCHEME, THE SEARCHING MODULE (SMod), AND THE TREE STRUCTURE

	[7]	[11]	[12]	This work
Architecture	RS	SMod	TS	TD
Num. of inputs	32			
Data width (bit)	5	4	6	4
Area (μm^2)	5,130.4	5,889	41,226	4,769
Delay (ns)	5.3	2.9	2.73	1.2
Area-time product (μm^2·ns)	27,191	17,078	112,547	5,722

As can be seen, the proposed TD-based MVIG provides the shortest latency with the smallest area, which is suitable for high-throughput LDPC decoders.

D. Hardware-Efficient CNU

The memory storage for the CNU can be further reduced in order to improve area efficiency. For the C2V message, a balanced quantization scheme, in which the number of quantization bits used for $M1$ and $M2$ is the same, is used.

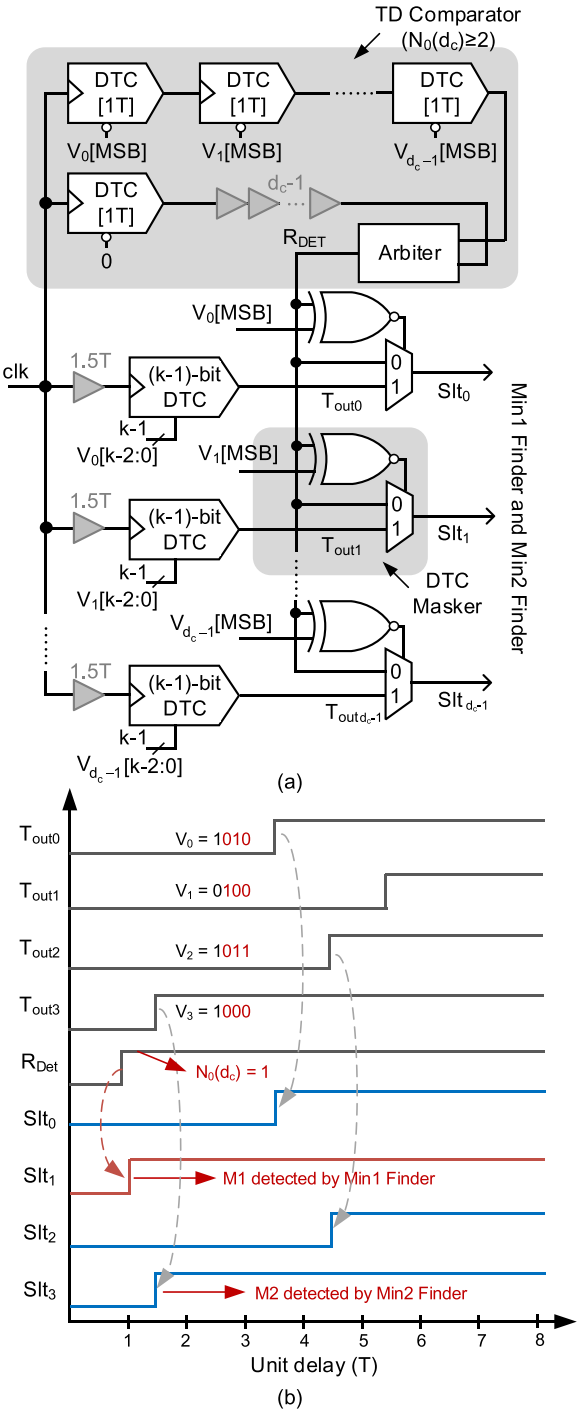

Fig. 6. (a) Modified DTC array with a $N_0(d_c)$ detector and d_c selectors. (b) Timing diagram of the modified four-input DTC array when $V_0 = 1010$, $V_1 = 0100$, $V_2 = 1011$, and $V_3 = 1000$.

Moreover, if a normalization factor of 0.75, i.e., $\alpha = 0.75$, is used, the number of quantization bits used for both $M1$ and $M2$ can be reduced by 1 compared with that used for Q magnitude. In order to advance the reduction in C2V registers, a memory reduction scheme was proposed for C2V messages in [17] by applying a dynamic normalization factor. However, this method cannot be applied to the proposed TD-based CNU because it requires a massive number of subtractions in order to calculate the difference, together with

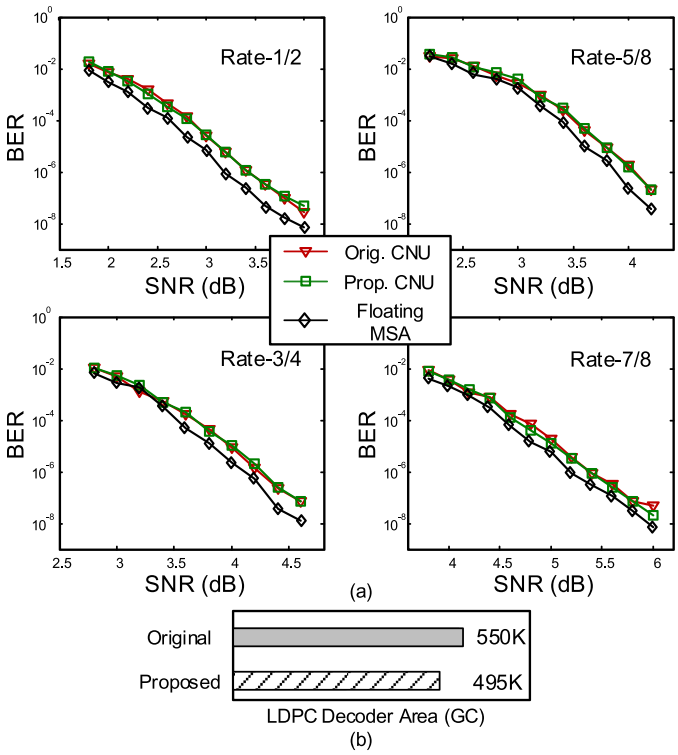

Fig. 7. (a) Performance evaluation for the CNU with a reduction in memory size for the four supported rates. (b) Total gate count for the LDPC decoder when comparing the original CNU and the proposed CNU.

frequent factor normalization based on the difference, resulting in a large area overhead when implemented in a TD-based approach.

In this paper, different numbers of quantization bits are considered for $M1$ and $M2$ since $M1$ is not larger than $M2$. This unbalanced quantization scheme can be achieved using a smaller clipping threshold for $M1$ while using a larger threshold for $M2$. If the threshold for $M1$ is set to be half of $M2$, the number of quantization bits for $M1$ can be reduced by 1 compared with that for $M2$. Fig. 7(a) shows the BER performance for the rate-1/2, rate-5/8, and rate-3/4 and rate-7/8 LDPC codes that are specified in the IEEE 802.15.3c standard. It can be observed that by applying the proposed unbalanced quantization scheme, the number of quantization bits for $M1$ can be reduced by 1 without notable degradation in error rate performance, thereby reducing the memory storage required for $M1$. Also included in Fig. 7(a) are the floating point results when using the conventional NMS algorithm. It can be observed that satisfactory error rate performance can be achieved using the proposed quantization scheme.

In the proposed decoder implementation, a (4,1) quantization scheme is used for both APP magnitude and Q magnitude, which means that a 4-b integer and a 1-b fraction are used to represent each APP magnitude and each Q magnitude, respectively. In addition, (2,1) and (3,1) quantization schemes are used for $M1$ and $M2$, respectively. From logic synthesis estimates, a saving of 50k equivalent logic gates can be achieved using the proposed unbalanced quantization scheme as shown in Fig. 7(b) without notable BER degradation

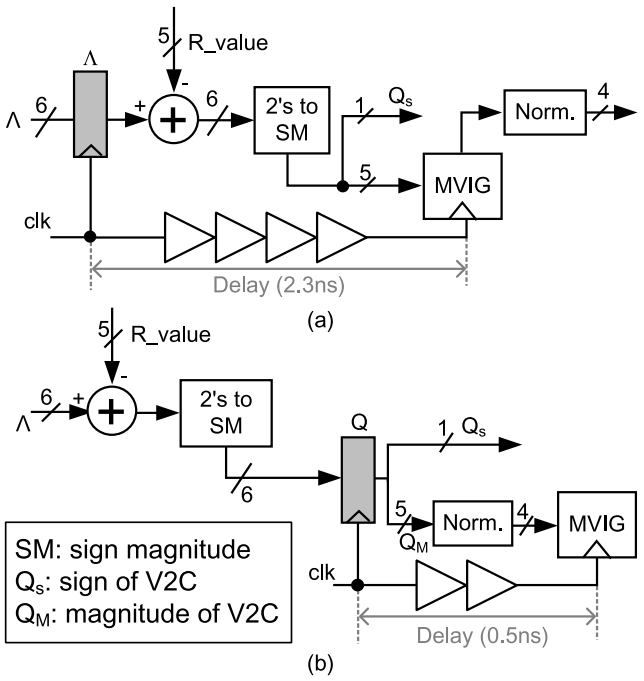

Fig. 8. (a) Λ-based VNU architecture. (b) Q-based VNU architecture.

compared with the balanced quantization scheme using the (3,1) quantization scheme for both $M1$ and $M2$.

IV. TD-Based Multimode LDPC Decoder

An LDPC decoder for IEEE 802.15.3c applications is designed so as to demonstrate the proposed TD signal processing techniques and related circuits. In order to facilitate the TD signal processing, a Q-based layered decoder architecture is proposed. Furthermore, MVIG, CNU, and outing networks are properly tailored in order to support the requirements of multimode operations specified in the IEEE 802.15.3c standard.

A. Q-Based Layered Decoder Architecture

Conventionally, a parallel block-row layered decoder architecture is used for high-throughput LDPC decoders [3], [22], [23], in which the *a posteriori* LLR values, i.e., Λ_n, for each code bit need to be stored. However, several constraints make a direct-mapped Λ-based architecture for TD LDPC decoders not feasible. Fig. 8(a) shows a conventional Λ-based architecture. A trigger signal derived from the clock with a large delay is necessary to ensure that the MVIG actives only when the correct inputs are ready. The computation path prior to the MVIG consists of a 6-b adder and a 2's complement to a sign–magnitude (SM) representation converter. According to the synthesis estimate in a 90-nm CMOS process, a 2.3-ns DLY must be inserted in order to match the delay between the Λ register and the MVIG. The insertion of this DLY also introduces an additional area overhead.

In order to reduce the latency, a modified variable node unit (VNU) architecture is proposed, as shown in Fig. 8(b), where the V2C messages, i.e., Q_{mn}, are stored rather than the Λ values. Note that it is not necessary to store all the V2C magnitudes corresponding to all connecting edges of the decoding graph. The size of the memory for storing the V2C magnitudes in this Q-based architecture is the same as that for Λ magnitudes in the Λ-based architecture. Since the normalization factor (α) determined by this code is 0.75, using the hardware-efficient CNU described in Section III-D, the magnitude of the MVIG can be reduced by 1 b. Therefore, a normalization unit is moved from the output of the TD-MVIG to the input of the TD-MVIG, meaning that the area of the DTC is reduced. The simulation results show that the delay can be reduced to 0.5 ns, translating into an area reduction by 78.3% for the delay chain.

For the Q-based architecture, the VNU is divided into two parts: the Q-value update unit (QVU) and the Λ-value update unit (ΛVU), which, respectively, execute the operations defined in (1) and (4). In addition, the layered scheduling is modified, as shown in Fig. 9, where $L = 4$ is considered. The Q-value and the Λ-value are updated in each cycle based on an interleaved way. It can be seen that the updating of the Λ-value lags the updating of the Q-value by one cycle for each layer. Since the Q-value and the Λ-value for the same layer are updated during different cycles, three layers of the compressed C2V messages ($M1$, $M2$, Idx1, and total sign) need to be stored than the four layers when $L = 4$. In contrast, the signs of all V2C messages need to be stored in order to recover the signs of the C2V messages.

Fig. 10 shows the architecture of the proposed layered decoder, where the IEEE 802.15.3c rate-7/8 code is considered. Initially, both the compressed C2V messages (stored in the C2V register) and the V2C signs for all layers (stored in the Q_s register) are set to zero. The decoding process starts by passing the channel LLR values y_n through the V2C routing network. The channel LLR values are used as the initial *a posteriori* LLR values Λ_n. After the V2C messages Q_{mn} are computed by QVUs, the magnitudes and signs of the V2C messages are, respectively, stored in the Q_M and Q_s registers. In the next cycle, the C2V calculation unit, which includes an MVIG and an XOR gate, calculates the compressed C2V messages. Then, the compressed C2V messages are stored in the C2V register and also fed to ΛVU in order to calculate Λ_n. The latest Λ_n values are passed through the C2V routing networks. The decoding process is repeated until it ends. The sign of Λ_n is also stored in the output buffer so that it can be used to check for early termination. A layered-based early termination check is performed in order to see whether a legal codeword is obtained or not, where the check sum values corresponding to all the check nodes are evaluated at the end of each layered processing. Consequently, a received frame may be correctly decoded without accomplishing a full iteration and it is able to improve decoding throughput. For our four-layer decoder, a possible *equivalent* number of iterations can be 0 or multiples of 0.25.

Fig. 11(a) and (b) shows the 4×32 and 16×32 base matrices of the rate-7/8 code and rate-1/2 code, respectively. The corresponding PCM can be obtained by replacing each element in the base matrix by a $z \times z$ circulant permutation matrix, where the element value is the shift index of the circulant permutation matrix. The circulant size specified in the

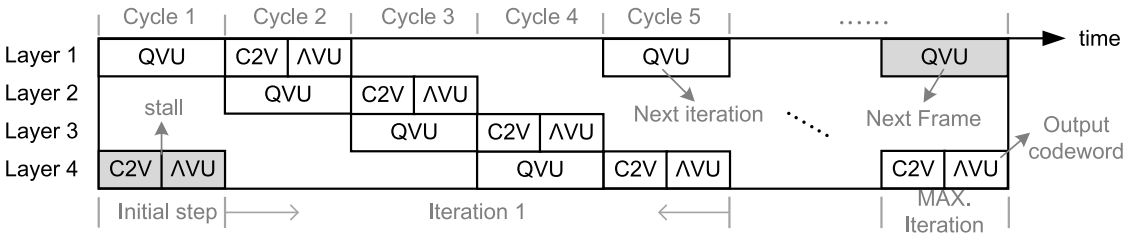

Fig. 9. Decoding flow for the Q-based layered decoding approach.

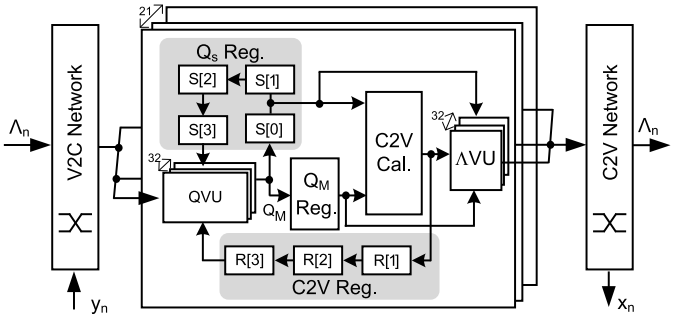

Fig. 10. Proposed Q-based layered decoder architecture for the rate-7/8 LDPC code.

standard is 21×21, i.e., $z = 21$. Since there are four rows in the rate-7/8 base matrix, a four-layer ($L = 4$) decoder architecture is appropriate. The check node degree (d_c) is 32. Therefore, there are $d_c \times z$, i.e., 32×21, QVUs and ΛVUs. In addition, there are 21 C2V calculation units and each C2V calculation unit consists of a 32-input MVIG and a 32-input XOR gate. Although there are 16 rows in the rate-1/2 base matrix, a four-layer ($L = 4$) decoder architecture is still appropriate using the structure relationship between the rate-7/8 and rate-1/2 base matrices.

Table III shows the comparison of the storage requirements for the Λ-based architecture [3] and the proposed Q-based architecture for the rate-7/8 LDPC code. The direct storage method described in Section II-B is used in [3] in order to reduce the delay of the critical path. Thanks to the TD signal processing, the critical path (and, hence, the MAX clock frequency) of the two decoders are nearly the same, but the proposed Q-based architecture needs only around 40% of memory storage compared with [3].

TABLE III
MEMORY STORAGE FOR THE Λ-BASED AND THE Q-BASED LAYERED DECODERS ($N = 672$, $L = 4$, $z = 21$, $d_c = 32$, $k_\Lambda = k_Q = 5$, AND $k_R = 4$)

	[3]	This work
Architecture	Λ-based	Q-based
Λ magnitude	$N \times k_\Lambda$ (672 × 5)	-
Λ sign	N (672)	-
Q magnitude	-	$N \times k_Q$ (672 × 5)
Q sign	-	$d_c \times z \times L$ (32 × 21 × 4)
R value	$N \times L \times (k_R$+Rsign) (672 × 4 × (4+1))	-
Compressed C2V Message	-	$(L$-1) × z × $(2k_R$+6) (3 × 21 × (2×4+6))
Total	17,472	6,930

B. Multimode Decoder Architecture

The IEEE 802.15.3c standard specifies that multimode operations are required in order to support 1/2, 5/8, 3/4, and 7/8 code rates. Each code has the same code length of $N = 21 \times 32 = 672$ b. Fig. 11(a) shows the base matrix of the rate-7/8 code, where the base matrix consists of eight 4×4 circulant matrices. The rate-1/2 base matrix can be generated from the rate-7/8 base matrix as shown in Fig. 11, where each 1×4 block in the rate-7/8 base matrix is extended to a 4×4 block in the rate-1/2 base matrix. Note that columns are not allowed to be exchanged in the extension procedure. The resultant rate-1/2 base matrix is shown in Fig. 11(b). Using the same procedure, rate-5/8 and rate-3/4 base matrices can be obtained.

The structure of the four base matrices can be leveraged to facilitate the decoder design. Fig. 12 shows the proposed multimode decoder architecture for IEEE 802.15.3c applications. Each of the V2C routing networks, the C2V routing networks, the C2V registers, QVUs, and the ΛVUs is partitioned into four groups based on the structure as analyzed by Chen *et al.* [4], so as to achieve a high throughput. Hence, there are 21×8 groups that perform Q-value updates (QVGs) and 21×8 groups that perform Λ value updates (ΛVGs). Each QVG consists of eight QVUs and one C2V register, which stores the corresponding compressed C2V messages. Each ΛVG consists of eight ΛVUs. Compared to the rate-7/8 single-mode architecture, additional 21×12 C2V registers are required in the multimode architecture so that the number

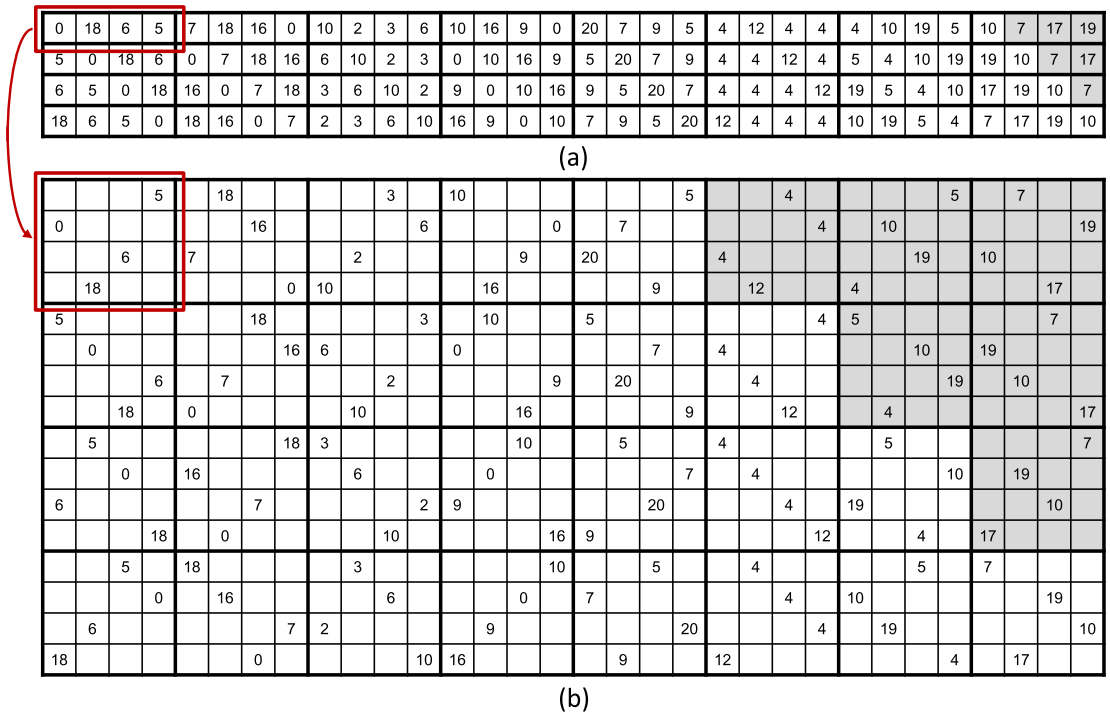

Fig. 11. Special of the IEEE 802.15.3c matrix. The outlined area indicates the relation of expanded version and the shaded part represents the virtual block. (a) Rate-7/8 base matrix. (b) Rate-1/2 base matrix.

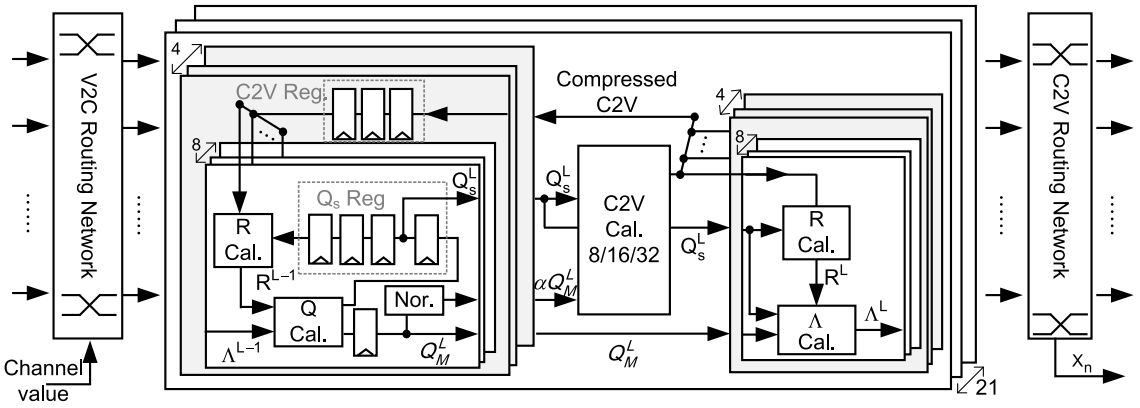

Fig. 12. Architecture of the proposed multirate TD LDPC decoder.

of C2V registers can equal the number of rows for the rate-1/2 PCM.

The single-mode MVIG is also extended to support multiple modes. A multimode MVIG needs to support 8, 16, and 32 inputs. As shown in Fig. 13(a), a three-stage sorting architecture is adopted. In this architecture, eight-input, two-input, and two-input OR gates are arranged in order to determine the first minimum value among the 32 inputs. The subsequent MUX gates are used to select the desired minimum value based on the operating code rate. Since the OR gates introduce delays in the signal paths, additional DLYs are inserted in the correct positions so as to match the delays.

Since the LDPC codes specified in the IEEE 802.15.3c standard are not regular, the proposed decoder should be sufficiently flexible to allow for alternative input ranges. For example, the rate-1/2 code (with the check node degree of five to eight) requires five to eight inputs for the MVIG (8-DTC array). A direct-mapped masking controller is shown in Fig. 13(b), where the MUX gates are used to select either the MAX value or the original input values (V_0–V_7). A modified index generator is proposed in order to avoid selecting the index associated with the MAX input values. Fig. 13(c) shows the modified masking controller, where the AND gates are used to mask the clock signal *clk* to the DTCs. Since the ith DTC is disabled when $ctr[i]$ is zero, the succeeding index selector is similarly deactivated. Also, further power saving can be achieved thanks to the clock-gated gates.

C. Chip Implementation

This chip is mostly designed with the synthesis and place-and-rout tools and only the timing-critical TD-MVIG

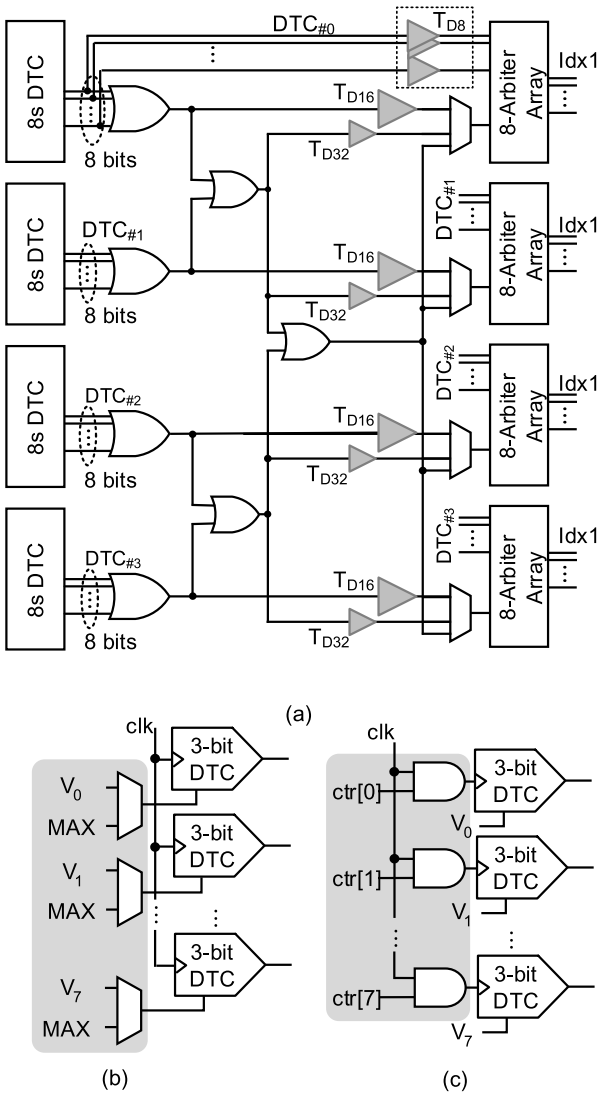

Fig. 13. (a) 8/16/32 minimum finder architecture. (b) Irregular controller. (c) Irregular controller using digital processing.

is optimized manually. The arbiter is the only customized cell since it is not included in the standard cell library. In order to facilitate cell placement, the height of the arbiter's layout is drawn as the same as that of other standard cells. The TD-MVIG is placed and routed manually to address the matching issue between multiple signals. The delay chain used to trigger the TD-MVIG is also included to ensure the timing accuracy. The functionality of the TD-MVIG is verified by Monte Carlo simulations. Compared with the TDC-based decoder presented in [19], the proposed arbiter-based decoder has lower clock loading because the proposed decoder does not require additional 294 ($7 \times 2 \times 21$) clock inputs for TDCs. The timing information of the TD-MVIG is extracted from its longest TD computation latency. The TD-MVIG is then packed as a macro and integrated with remaining logic cells through automatic tools in the synthesis and place-and-route stages.

V. Chip Verification

The multimode LDPC decoder that includes TD signal processing for the IEEE 802.15.3c standard was fabricated

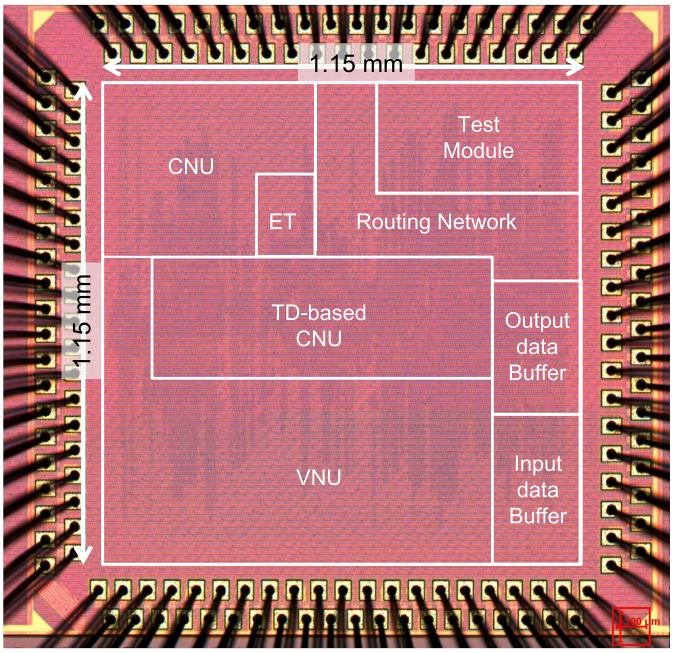

Fig. 14. Microphotograph of the LDPC decoder chip.

TABLE IV
Chip Summary

Technology	CMOS 1P9M 90nm			
Die Size (mm^2)	2×2			
Core Size (mm^2)	1.5×1.5			
Supply Voltage (V)	1.05			
Clock Frequency (MHz)	157			
Code Rate	1/2	5/8	3/4	7/8
Power (mW)	229	232	234	236
Throughput (Gbps) w/ ET @(BER = 10^{-5})	10.55	17.584	21.62	30.08
Throughput (Gbps) w/o ET	5.28			

using a 90-nm 1P9M CMOS process. Fig. 14 shows the chip microphotograph, and a summary of the chip specifications is presented in Table IV. The chip includes an LDPC decoder, a test module, and input/output data buffers in a core area of 2.25 mm^2. The input/output data buffers are included due to the limited number of I/O pads. The FO4 delay of the adopted 90-nm technology is 27.8 ps. Considering the critical path of our design is 6.37 ns, the logic depth is estimated to be 229, which is a technology independent term to describe the level of logic in the critical path. Power breakdown is analyzed through simulation with respect to the LDPC decoder, the testing module, and the input/output data buffers.

TABLE V
PERFORMANCE COMPARISON

	JSSC'11 [18]	JSSC'14 [19]	JSSC'14 [5]	ASSCC'15 [24]	ISSCC'14 [25]	JSSC'12 [3]	This work
Technology	0.5 μm	65 nm	65 nm	28 nm	28 nm	65 nm	90 nm
Signal Processing	Analog	TD	Digital	Digital	Digital	Digital	TD
Code Specification	(32,24)		(672,366)	(672,K) K=336,420,504,546		(672,K) K=336,420,504,588	
Decoding Algorithm	MP	NMS	offset-MS	NMS	NMS	NMS	NMS
Scheduling	Flooding	Flooding	Layered	Layered	Flooding	Layered	Layered
Decoder Gate Count	-	-	-	-	-	647K	495K
Core Area (mm^2)	5.4 [0.17]	0.063 [0.12]	1.6 [3.06]	0.78 [8.06]	0.63 [6.51]	1.56 [2.99]	2.25
Number of Iterations	-	5	10	2[b]	3.75[b]	5	5
Supply Voltage (V)	3.3	1.2	1.15	0.9	1.1	1.0	1.05
Clock Frequency (MHz)	-	240 [173.3]	540 [260.6]	470 [146.22]	260 [80.89]	197 [142.3]	157
Throughput (Gbps)	0.0128 [0.07]	0.38 [0.27]	9.0 [6.5]	18.4 [5.72]	12 [3.73]	6.62[c][4.78]	5.28
Power (mW)	1.25	4	782.9	166	180	361	182
Normalized Energy (pJ/bit)	97.66 [17.58]	10.53 [14.57]	86.99 [120.45]	9.02 [29.00]	15.00 [48.21]	54.53 [75.51]	34.47
Hardware Efficiency ($Gb/s/mm^2$)	<0.01 [0.41]	6.03 [2.27]	5.63 [2.12]	23.59 [0.71]	19.05 [0.57]	4.24 [1.60]	2.35

[*] Numbers in the bracket are normalized to the 90nm technology.

Energy/bit (in 90nm) = Energy/bit $\times \frac{90\text{ nm}}{\text{Technology}}$, Hardware Efficiency (in 90nm) = Hardware Efficiency $\times (\frac{90\text{ nm}}{\text{Technology}})^3$.

[b] Average number of iterations is applied.

[c] Information-bit throughput is scaled to code-bit throughput.

[d] Energy and hardware efficiency are computed based on the code-bit throughput.

The LDPC decoder accounts for 77% of the entire power. All the messages are stored in registers. The registers, TD MVIG, and remaining logic circuits account for 57.1%, 7.8%, and 35.1%, respectively, of the power dissipated by the LDPC decoder.

Fig. 15 shows the measured MAX clock frequencies with pressure voltage temperature (PVT) variation of five chips. A MAX clock frequency of 161.5 MHz is achieved at -25 °C and 1.2 V. At 25 °C and 1.05 V, the LDPC decoder can operate at 157 MHz, delivering a throughput of 5.28 Gb/s with five iterations. The chip dissipates 229, 232, 234, and 236 mW for the code-rate 1/2, 5/8, 3/4, and 7/8 modes, respectively. Fig. 16 shows the measured and simulated BERs for the (672, 588) code. The measured BER results match the simulated results well before BER $= 10^{-5}$ under the testing limitation. Fig. 16 also shows the associated throughput for the same code. Since a layered-based early termination scheme is used in the proposed decoder, most of the received frames can be corrected within a single iteration at high SNR. At BER $= 10^{-5}$, the LDPC decoder achieves a MAX throughput of 30.08 Gb/s at a clock frequency of 157 MHz.

A comparison of the performance with that of the chips described in the previously published literature is summarized in Table V and Fig. 17. The normalized energy and hardware efficiency without technology scaling is shown in Table V. It is known that comparing designs at different technology nodes is difficult because the impact of scaling in deep-submicrometer technology is not well defined. Especially, the TD-based circuits may have different scaling behavior from the conventional digital logic realizations with respect

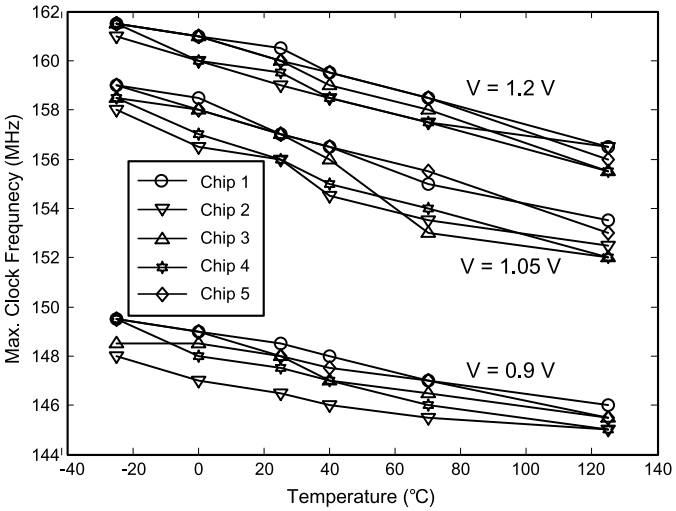

Fig. 15. Measurement results with the PVT variation of five chips.

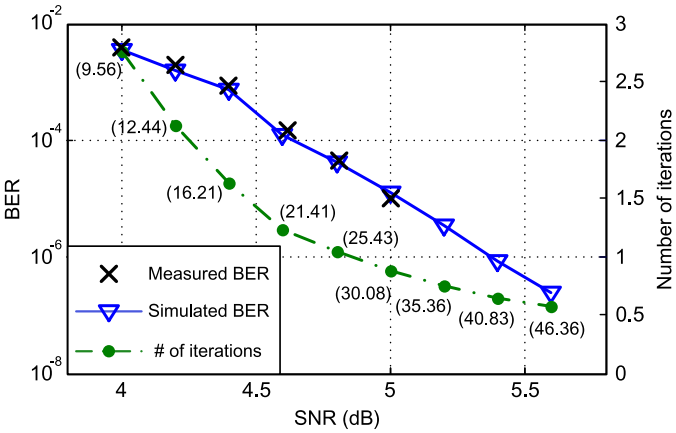

Fig. 16. Measured and simulated BER results and throughput with early termination for the (672, 588) code. The values in the brackets indicate the throughput in gigabits per second under a clock frequency of 157 MHz.

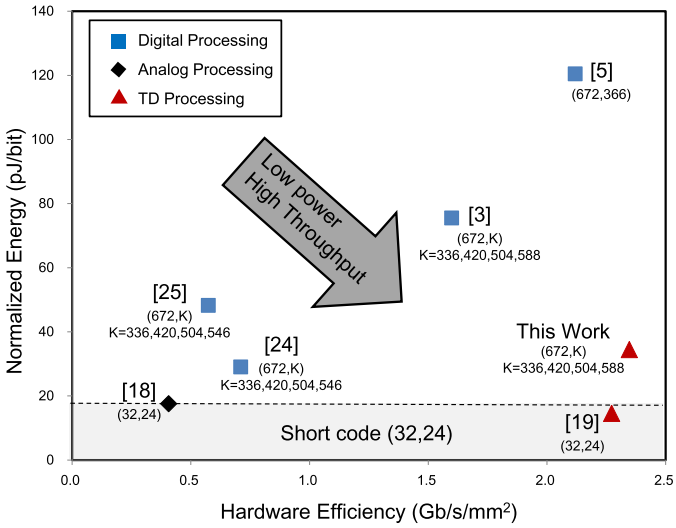

Fig. 17. Comparison of the hardware efficiency and the normalized energy. The values in the brackets indicate the code length. The chip presented in this paper achieves the highest hardware efficiency with the lowest normalized energy for practical long LDPC codes.

to scaling. To present a fairer comparison, however, all chips are still normalized to the 90-nm process. In [18] and [19], analog and TD signal processing techniques were utilized in order to minimize the power consumption. However, the high energy efficiency is gained at the expense of reduced scalability since the signal processing is performed in an analog format. Only a (32, 24) short code can be supported, which is not feasible for practical applications. Considering other designs that are capable of supporting long codes, a decoder architecture containing embedded DRAM cells so as to reduce the power consumption was proposed in [5]. A decoder that uses the pipelining technique to improve the energy efficiency is presented in [24]. The design in [25] reduces the power consumption through a 28-nm ultrathin body and BOX fully depleted SOI technology. In [3], a decoder architecture reduces the computation load and the critical path by storing all C2V messages. Among the decoders that are able to support long codes, the proposed work achieves the lowest normalized energy dissipation and the highest hardware efficiency. The scalability for multiple long codes is significant improved thanks to the proposed TD MVIG that operates in a more digital fashion. The hardware efficiency achieved in this paper is also enhanced through the Q-based layered decoder architecture. If the critical path needs to be further reduced, the technique proposed in [3] can be applied to the proposed TD-based decoder. The estimated latency of the critical path is then reduced to 5 ns, translating into a clock frequency of 200 MHz, in the 90-nm process. However, the hardware efficiency will also reduce to 2.24 Gb/s/mm^2 and hence the associated architecture is not considered in this paper.

VI. Conclusion

An efficient and scalable MVIG that is achieved by employing TD signal processing is presented for NMS-based LDPC decoders. The issue related to matching between DTC and TDC that limits the possibility of scalability in conventional TD decoders is eliminated thanks to the proposed arbiter-based circuit. The first two minimum values and the associated indices can be determined in a single cycle, resulting in a high throughput. The memory storage required for check node processing is significantly reduced through the layered decoder architecture that stores one-layer of V2C messages, together with the associated scheduling scheme. The multimode feature specified in the standard for practical applications can also be supported by extending the TD MVF. The proposed techniques have been demonstrated through a TD-based LDPC decoder that is designed to comply with the IEEE 802.15.3c standard. Fabricated using a 90-nm process, the multimode LDPC decoder integrates 495k logic gates in an area of 2.25 mm^2 and achieves a MAX throughput of 30.08 Gb/s when operated at 157 MHz with a BER of 10^{-5}. The chip dissipates power at 182 mW and has 34.47 pJ/b of normalized energy. This paper demonstrates the potential for practical applications of analog-assisted digital signal processing that can achieve high energy efficiency and high throughput. Maintaining the scalability while allowing mismatch errors in the TD signal processing is certainly a point of future work.

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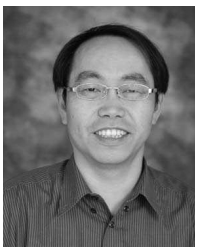

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