Comments and Corrections

Corrections to "A 10/20/30/40 MHz Feed-Forward FIR DAC Continuous-Time ΔΣ ADC With Robust Blocker Performance for Radio Receivers"

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In [1], Table I compares the state of the art in CT ΔΣ ADCs. Unfortunately, due to a mistake, the FOM [Schreier] (dB) reported is 3 dB below its actual value. Table I in [1] is reprinted as Table I. The authors regret their mistake.

REFERENCES

[1] S. Loeda, J. Harrison, F. Pourchet, and A. Adams, "A 10/20/30/40 MHz feedforward FIR DAC continuous-time ΔΣ ADC with robust blocker performance for radio receivers," *IEEE J. Solid-State Circuits*, vol. 51, no. 4, pp. 860–870, Apr. 2016.

[2] Y.-S. Shu, J.-Y. Tsai, P. Chen, T.-Y. Lo, and P.-C. Chiu, "A 28 fJ/conv-step CT ΔΣ modulator with 78 dB DR and 18 MHz BW in 28 nm CMOS using a highly digital multibit quantizer," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Sep. 2013, pp. 268–269.

[3] C.-L. Lo, C.-Y. Ho, H.-C. Tsai, and Y.-H. Lin, "A 75.1 dB SNDR 840 MS/s CT ΔΣ modulator with 30 MHz bandwidth and 46.4 fJ/conv FOM in 55 nm CMOS," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2013, pp. C60–C61.

[4] R. S. Rajan and S. Pavan, "Design techniques for continuous-time ΔΣ modulators with embedded active filtering," *IEEE J. Solid-State Circuits*, vol. 49, no. 10, pp. 2187–2198, Oct. 2014.

TABLE I

CT ΔΣ ADC State of the Art. FOM*$[sBWeq] = (\text{Power} - 1\,\text{mW} \times (1 - f_{\text{clk}}/2.4\,\text{GHz}))/2/\text{BW}/2^{\text{ENOB}}$

	This work				[2]	[3]	[4]
Process	40nm				28nm	55nm	90nm
Active Area	0.0194mm^2				0.08mm^2	0.071mm^2	0.12mm^2
fclk (GHz)	0.6	1.2	1.8	2.4	0.64	0.84	3.6
Power(mW)	1.94	3.24	4.30	5.25	3.9	13	15
BW(MHz)	10.0	20.0	30.0	40.0	18.0	30	36
DR(dB)	68.7	70.0	68.2	67.8	78.1	77.1	83
Peak SNDR(dB)	67.4	69.4	67.7	66.9	73.6	75.1	70.9
FOM[Walden] (fJ/cs.)	50.5	33.6	36.1	36.3	27.7	46.6	72.7
FOM[Schreier] (dB)	164.5	167.3	166.1	165.7	170.2	168.7	164.7
FOM*[sBWeq] (fJ/cs.)	**31.0**	**28.4**	**34.0**	**36.3**	27.7	46.6	72.7