

# A Fully Integrated Reconfigurable Self-Startup RF Energy-Harvesting System With Storage Capability

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**Abstract**—This paper introduces a fully integrated RF energy-harvesting system. The system can simultaneously deliver the current demanded by external dc loads and store the extra energy in external capacitors, during periods of extra output power. The design is fabricated in 0.18- $\mu\text{m}$  CMOS technology, and the active chip area is 1.08 mm<sup>2</sup>. The proposed self-startup system is reconfigurable with an integrated LC matching network, an RF rectifier, and a power management/controller unit, which consumes 66–157 nW. The required clock generation and the voltage reference circuit are integrated on the same chip. Duty cycle control is used to operate for the low input power that cannot provide the demanded output power. Moreover, the number of stages of the RF rectifier is reconfigurable to increase the efficiency of the available output power. For high available power, a secondary path is activated to charge an external energy storage element. The measured RF input power sensitivity is –14.8 dBm at a 1-V dc output.

**Index Terms**—Charge pump, clamper, CMOS, compensation rectifier, controller, dual-path energy, extra energy, fully integrated, Internet of Things, LC matching, nonoverlapping cross-coupled level shifters, portable, power management, reconfigurable, RF energy harvesting, RF rectifier, self-sustainable, stages, storage capacitor, tunable, ultralow power.

## I. INTRODUCTION

ENERGY harvesting from available sources in nature is one of the current research trends that avoids the use of external batteries and/or connection to a wired permanent power source. However, this technology is not yet mature enough for commercial use. Among the energy-harvesting sources, RF energy harvesting is a promising renewable energy source with the prime advantages of flexibility and portability with respect to other sources. The system consists of a receiving antenna and an RF rectifier to convert the RF energy into dc energy. The dc energy can be used by resistive demand loads or stored for later use in capacitors and/or

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rechargeable batteries. Power management is needed to control the energy flow mandates of a self-startup feature that can provide the control circuits with the needed dc power without any power overhead from external sources. The needed dc load power defines the sensitivity of the RF harvesting system, and it is lower when only one capacitive load (open circuit) is charged. The RF energy is reported to have the lowest average power density [1]. Moreover, for a specific frequency band, the RF power varies dynamically according to three parameters: the change of transmitted power, the distance between the transmitter and the receiver, and the RF wireless link.

In order to tackle the variable nature of the input power, [2] proposed a dual-mode reconfigurable RF rectifier to widen the operating power range. The reported sensitivity was obtained for open circuit loads with no control circuits. From a top level point of view, [3]–[5] describe harvesting systems in which the power management is incorporated and only resistive loads are supported by the RF energy harvesting front ends. In [3], an off-chip matching network and a differential RF single stage rectifier with a cascaded boost converter are used. The harvested power is delivered to a resistive load, and the boost converter presents an adaptive resistive load for the rectifier. In [4], RF harvesting was used to kick-start both the control and the boost converter for thermoelectric and solar energy harvesting. Even though the RF energy harvesting does not provide a demand load with dc power, it provides power to the control of the chip in the vicinity of other sources. In [5], RF harvesting is incorporated to provide the control circuits with the needed dc power. This enables the thermoelectric harvesting to operate at lower voltages with higher power conversion efficiency (PCE).

Therefore, for variable input power, a reconfigurable system architecture is important to accommodate the different RF power conditions, while the extra harvested energy can be stored in external storage elements. For the RF energy-harvesting systems, full integration and self-startup are key attributes. In this paper, an RF energy harvesting system is proposed and the contributions of this paper are as follows: 1) a fully integrated system with an RF matching network, RF rectifier, and power management/control circuitry; 2) a self-startup operation while minimizing the dc power overhead from the controller with 66–157-nA current consumption; 3) a reconfigurable system to increase the available output power with the different input power levels with an RF rectifier

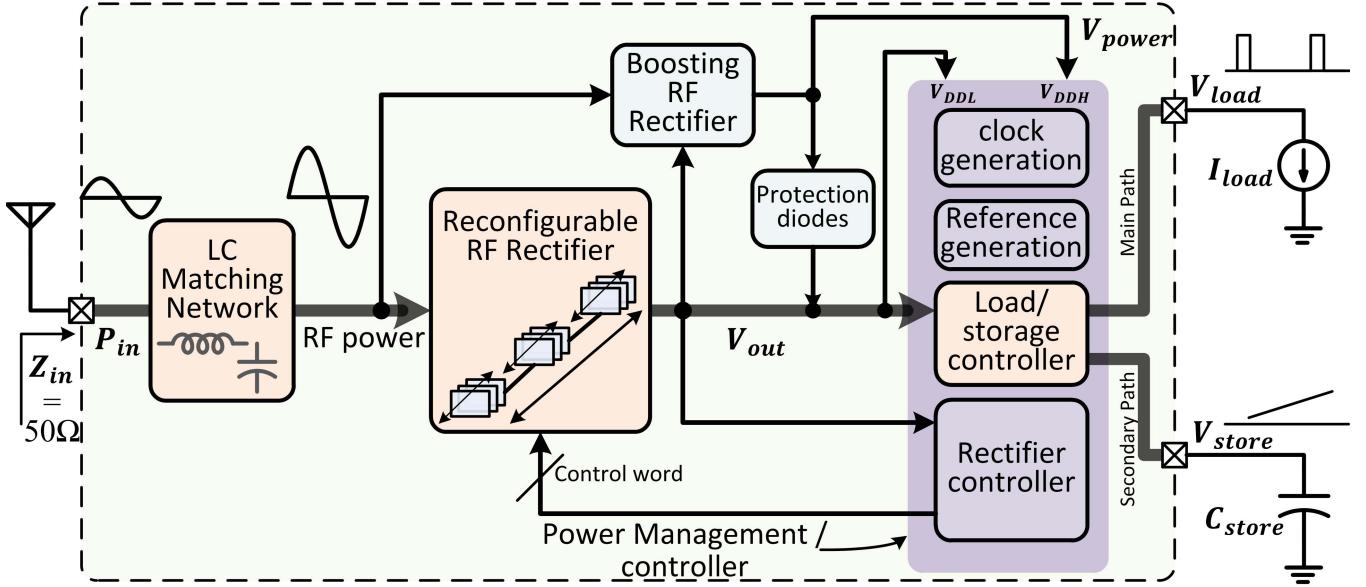


Fig. 1. Reconfigurable RF energy harvesting system with power management/controller.

with a modular design for a general number of stages  $N$ , while using all subblocks at the same time—specifically, the implementation of one-two-four-eight-stage configurations; 4) a proposed hardware solution to deliver the harvested power to different paths, such that a demand-resistive load with duty cycle capability and a storage capacitor for extra power are simultaneously supported with priority to the resistive load; and 5) the proposed nonoverlapping input/output level shifters to minimize the shoot-through power loss. The sensitivity of the total system is  $-14.8$  dBm at a 1-V dc output.

This paper is organized as follows. Section II describes the proposed RF energy-harvesting system and the main building blocks. Section III shows the circuit implementation for the main building blocks. Section IV discusses the RF rectifier and the matching network and shows the effect of the reconfiguration on the parameters of the RF front end. Section V shows the measurement results for the RF energy-harvesting systems. Finally, Section VI discusses the conclusions.

## II. DESCRIPTION OF THE RF ENERGY-HARVESTING SYSTEM

The proposed system is shown in Fig. 1. It integrates the RF circuits, the controllers, and the power management. The RF energy is received by an off-chip antenna tuned at the band of interest, which is 915 MHz. The antenna converts the electromagnetic energy, which propagates through the space, into electric energy. For maximum power transfer from the antenna, an *LC* matching network is inserted between the antenna and an RF reconfigurable rectifier. The RF reconfigurable rectifier is an ac-to-dc converter, which can be reconfigured to enhance the overall system efficiency as a function of the input power. The nominal output voltage  $V_{out}$  is used for dc energy delivery to the main load  $I_{load}$  and the storage capacitor  $C_{store}$  for the extra power through the main and secondary

paths, respectively. Moreover,  $V_{out}$  acts as a low-supply  $V_{DDL}$  for the power management/controller block. An auxiliary boosting rectifier is used to generate a voltage  $V_{power}$  higher than the nominal voltage  $V_{out}$ . The voltage  $V_{power}$  is the voltage  $V_{DDH}$  for the power management/controller block and is used for high voltage control. Protection diodes are used between the voltage  $V_{power}$  and the voltage  $V_{out}$  to limit the maximum value of  $V_{power}$  without affecting the reliability of the devices. The power management/controller has four main ultralow power blocks: the clock generation, the voltage reference generation, the load/storage controller, and the rectifier controller. The clock generation is used by all digital logic circuits. The reference generation is used to generate a constant voltage  $V_{BG}$  that is robust with variation in supply voltage, temperature, and process. This is the only analog block contributing to the overall static power. The load/storage controller is responsible for delivering the dc energy to both the load  $I_{load}$  and the storage capacitor  $C_{store}$ . It has latched comparators as well as digital logic to take the appropriate decisions to control the system. Last, depending on the estimation of the open circuit value of the output voltage  $V_{out}$ , the rectifier controller sends a binary control word to the RF reconfigurable rectifier in order to choose the state of the rectifier (the number of stages) yielding the desired output voltage. The flow of extra power is limited by the secondary path maximum extraction capability, which suggests that multiple secondary paths could be used in the future for handling larger input power.

In Sections II.A and II.B, the reconfigurable RF rectifier is presented along with illustrations on how to generalize for  $N$  number of stages while using all subblocks. Then, the energy delivery through the main and secondary paths is discussed.

### A. Reconfigurable RF Rectifier

The reconfigurable rectifier is shown in Fig. 2 where the number of subblocks  $N$  is kept constant for all

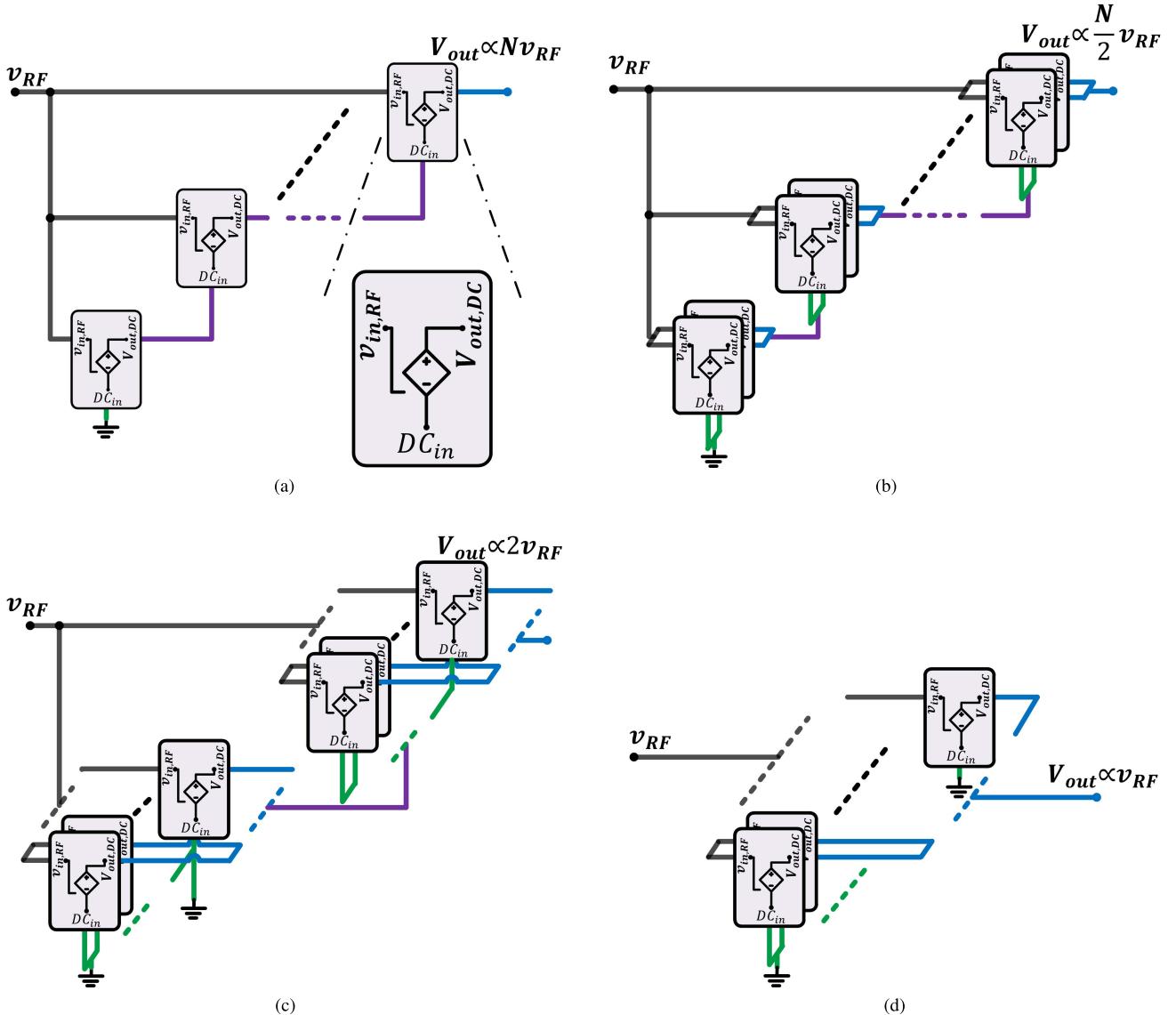


Fig. 2. Conceptual reconfigurable RF rectifier with the total number of subblocks  $N$ . (a)  $N$  number of stages in series. (b)  $N/2$  number of stages in series with two parallel subblocks for each. (c) Two stages in series with  $N/2$  parallel subblocks for each. (d) One stage with  $N$  parallel subblocks for each.

different configurations. The typical configuration consists of  $N$  number of stages in a series, as shown in Fig. 2(a). Each stage/subblock takes a sinusoidal input  $v_{RF}$ , rectifies it to a dc output voltage, and places it in series with the output voltage  $dc_{in}$  of the previous stage. Thus, the final output voltage  $V_{out}$  is proportional to  $N$ . The first stage is connected to the reference ground and all the stages are connected to the RF port  $v_{RF}$ . As the input amplitude of  $v_{RF}$  increases, the required number of stages can be lowered to maintain the same output voltage  $V_{out}$  while increasing the supported maximum output current. This last property means that the diodes switches or the stage sizing should be larger. If the  $N/2$  number of stages in series and two subblocks in parallel are used, as shown in Fig. 2(b), the stages are rearranged, such that the sizing of each stage is doubled, compared with the typical configuration in Fig. 2(a). The higher the input amplitude of  $v_{RF}$ , the fewer stages appear in series, and the more subblocks appear in parallel, the larger each stage becomes. This can increase the available output

power as will be shown in the measurements. Fig. 2(c) and (d) shows the case where two stages and one stage are obtained with the reconfiguration of the same rectifier, respectively.

The proposed scheme reconfigures the number of stages of the RF rectifier while using all subblocks that are already connected to the RF port. Additionally, as shown in Section III, the reconfiguration can be done on the dc side of the RF rectifier to avoid the losses on the RF side. In general, using  $N$  number of subblocks, the number of configurations is up to  $\text{floor}\{\log_2(N)\} + 1$  where  $\text{floor}\{\cdot\}$  is the integer of the argument. The preferred choice of  $N$  is from the geometric sequence  $\{1, 2, 4, 8, 16, \dots\}$ .<sup>1</sup> The circuit of the reconfigurable RF rectifier is shown in Section III.

<sup>1</sup>In order to get the minimum transition between the minimum number of stage configurations and the next configuration, a base-2 log is used, which results in a transition from 1 to 2. If a base-3 log was used, this transition would have been from 1 to 3 and  $N$  would have been preferably chosen from the geometric series  $\{1, 3, 9, \dots\}$ .

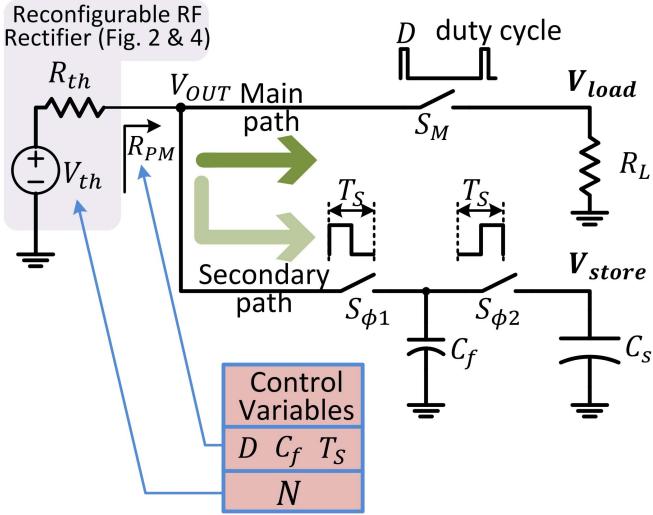


Fig. 3. Scheme used to control the power flow to the load demand and the storage capacitor.

#### B. Load/Storage Control Scheme

The reconfigurable RF rectifier, as shown in Fig. 2, is represented by its Thevenin equivalent circuit: an open circuit voltage source  $V_{th}$  and a series resistance  $R_{th}$ . The energy flow from the rectifier to the main load demand  $R_L$  and the remaining power to charge the storage capacitor  $C_{store}$  is controlled through the main and the secondary paths, respectively. Fig. 3 shows how the two power flow paths interact. For maximum power transfer between the rectifier and the subsequent blocks, assume that the desired output voltage from the rectifier is  $V_{out}$  equal to  $V_{dc,desired}$  as

$$R_{PM} = R_{th} \quad (1)$$

$$V_{th} = NV_{th,stage} = 2V_{dc,desired} \quad (2)$$

where  $R_{PM}$  is the parallel input resistance of the subsequent blocks and  $V_{th,stage}$  is the Thevenin voltage of any stage.  $V_{th}$  can be estimated for an open circuit condition and used to control the number of stages of the RF rectifier.

Now, we consider how to control the value of  $R_{PM}$ . The main path always has the higher priority to deliver energy to the resistive load. In the case of extra energy, the secondary path can take the remaining energy, while conditions (1) and (2) are satisfied. The first situation is when the available energy from the RF rectifier is less than the load demands, and the ratio of  $R_L/R_{th}$  is less than one, where the load demand is characterized by a specific  $R_L$  value. In order to increase the equivalent input resistance  $R_{PM}$ , the duty cycle control scheme is utilized to satisfy the  $V_{dc,desired}$  and the load demand simultaneously with a duty cycle less than 100%. The second situation occurs when there is more available energy than the load demands and the ratio of  $R_L/R_{th}$  is greater than one; hence, the secondary path is activated to satisfy (1). One possible implementation of the secondary path is shown in Fig. 3. The secondary path charges the capacitor  $C_f$  for half of the period, and for the other half, the charge of the capacitor  $C_f$  is dumped to the storage capacitor  $C_{store}$ . Thus, using this scheme, the parallel input resistance can be

expressed as

$$R_{PM} = \frac{R_L}{D} \parallel R_{second} = \frac{R_L}{D} \parallel \frac{T_s}{C_f} \quad (3)$$

where  $R_{second}$  is the equivalent input resistance of the secondary path,  $D$  is the duty cycle from 0% to 100%, and  $\parallel$  indicates the parallel equivalent resistance. For the specific implementation of the secondary path, the switched capacitor circuit [6] has an input resistance  $R_{second}$  that is inversely proportional to the capacitance value  $C_f$  and the operating frequency  $f_s$  (proportional to period  $T_s$ ) of the two phases,  $\phi_1$  and  $\phi_2$ . Therefore, these signals are used to tune  $R_{second}$ . Finally, in the proposed architecture, there is no specific relationship between the frequencies of the signals,  $S_{\phi_1}$  ( $S_{\phi_2}$ ) and  $S_M$ . The circuit implementation of the control circuit may impose some relationship between both as will be mentioned in Section III.

#### III. CIRCUIT IMPLEMENTATION OF THE PROPOSED SYSTEM

Fig. 4 shows the proposed reconfigurable RF front end. The *LC* matching network consists of two stages with digitally tunable capacitors to support different bands. The reconfigurable RF rectifier provides the dc energy to the load (resistive) and capacitive storage. As shown, an auxiliary boosting rectifier generates a second dc voltage  $V_{power}$ . Thus, there are two supplies: a nominal output voltage  $V_{DDL} = V_{out}$  and a higher voltage  $V_{DDH} = V_{power}$ . Protection diodes are used between  $V_{power}$  and  $V_{out}$  in order to prevent the voltage difference from going beyond a certain limit to comply with the reliability of the devices and provide the extra current to the load so as not to waste it. There is a tradeoff in the design of the stack of protection diodes: the more diodes used, the less effect on low voltage differences at the output (and this will affect the voltage difference of the boosting RF rectifier at the low voltage range, which is proportional to the open circuit voltage, as will be shown), but higher protection voltage is imposed (in the order of the number of diodes  $\times 0.7$  V). For the current design, only two diodes are used for extra protection of the devices. A reconfigurable eight-stage (extendable to more, if needed) RF rectifier is utilized. The pMOS devices are used for compatibility with the standard CMOS technology. The nature of the voltages of each stage is: ac with no dc shift at the RF input side, an ac superimposed on a one time dc shift at the intermediate node, and two times shifted dc with no ac at the output node. Moreover, level-one compensation [7] is incorporated. In the conventional diode-connected realization of diodes, the gate and the drain are tied together as in [8] and device  $M_{X1}$  in Fig. 4. Introducing a positive (negative) voltage difference between these two nodes for nMOS (pMOS) device can mitigate the threshold voltage constraint of the devices. In order to realize this floating voltage  $V_B$ , as shown in Fig. 4, the connection between the gate of the nMOS (pMOS, for example  $M_{X4}$ ) device in the current stage and the drain of the similar nMOS (pMOS) device in the next (previous) stage is used. Hence, the value of  $V_B$  is the dc shift from each stage to the next. The connection should be between nodes of the same voltage nature. If the connection is taken from  $m$ -stages away from the current stage, this is called level- $m$  compensation [7].

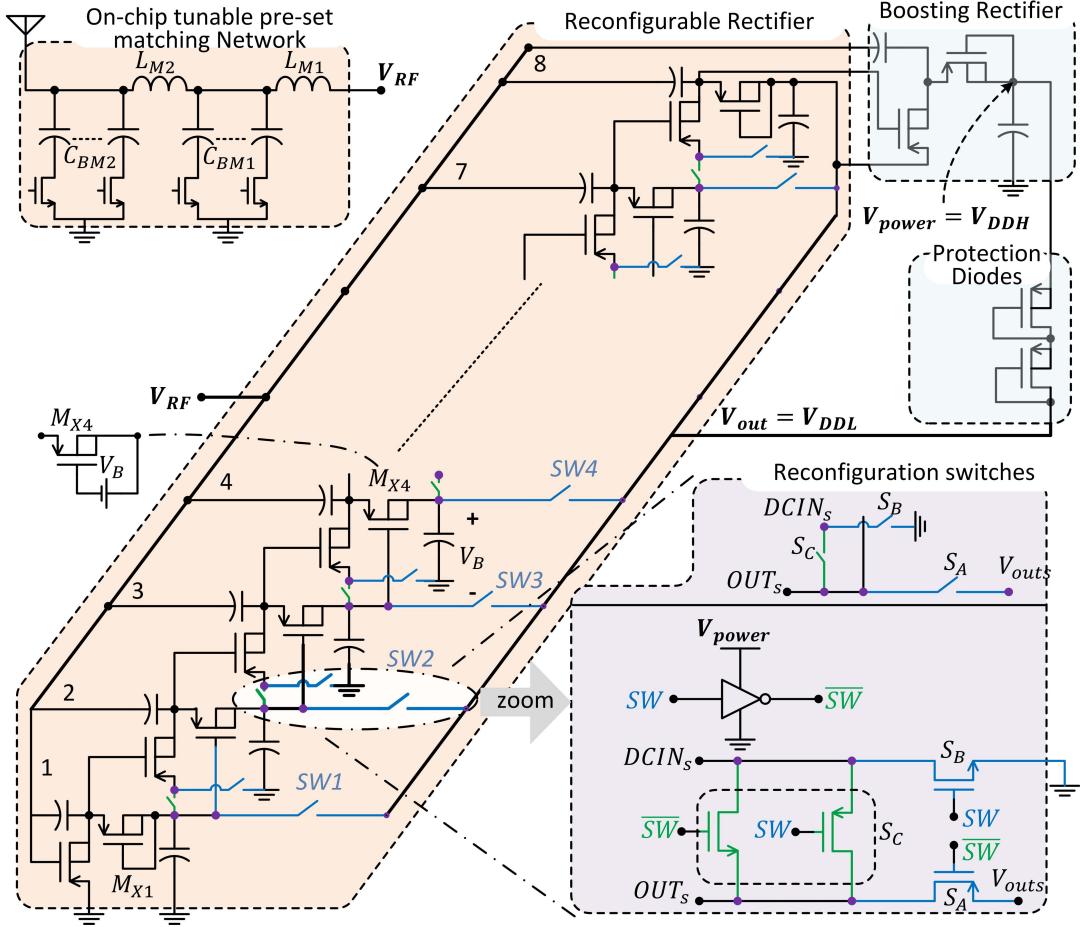


Fig. 4. Reconfigurable eight-stage level-one compensated RF rectifier and cascaded one stage with limiting/protection diodes.

The reconfiguration switches are also shown in the lower right-hand side of Fig. 4, where an  $SW$  signal controls the state of each subblock either in series or in parallel. Each switch network consists of three switches: pMOS switch  $S_A$ , nMOS switch  $S_B$ , and a transmission gate  $S_C$ . This scheme reconfigures the number of stages of the RF rectifier while using all subblocks that are already connected to the RF port. Moreover, it is implemented completely on the dc side of the RF rectifier where the reconfiguration switches are not affecting the parasitic capacitance on the RF side. Since the switches are on the dc side, the conduction loss is dominant and the switching loss is expected to be small. The ON-resistance  $R_{ON}$  is inversely proportional to  $V_{GS}$  of the switch. However, the current flow  $I_{load}$  is small, and therefore, the conduction loss is  $I_{load}^2 R_{ON}$ , and can be made small. As the input power increases, the value of  $R_{ON}$  decreases quickly with the increase of  $V_{power}$ , where the conduction loss is once again small. Unlike [9] where stages are skipped (which is only acceptable for low frequency operation), here all existing subblocks are used in an efficient way. This way, the available output power from the RF rectifier is increased.

Fig. 5 shows the power management block, which is part of Fig. 1, except for the controller of the RF rectifier, which will be discussed in Section III. It consists of a clock generation circuit, a voltage reference circuit [10], and the

load/storage controller.  $V_{DDL}$  is connected to the reference generation blocks, all the digital circuitry, and the latched comparators, while  $V_{DDH}$  is connected to the reference generation block and the level shifters (LS1, LS2, and LS3). The level shifters (LS1 and LS2) are used to control the switches in both the reconfigurable RF rectifier and the main and secondary paths of the dc energy delivery to  $I_{load}$  and  $C_{store}$ , respectively. The proposed nonoverlapping level shifter (LS3) to shift the clock signals will be discussed. The main path has latched comparators as well as digital logic to reconfigure the system for different input power levels. The secondary path transfers the remaining power to  $C_{store}$  through a tunable capacitor  $C_f$ , as shown in Fig. 5, and the switches  $M_2$  and  $M_3$ , which operate at a frequency  $f_s$ . The higher the value of  $f_s$  and  $C_f$ , the more energy is transferred through the secondary path.

To control the *main path*, half of the output voltage  $V_{out}$  is compared with  $V_{BG}$ . The comparison is done through two comparators with  $\phi_1$  and  $\phi_2$  (see also Fig. 3) to effectively operate twice as fast, compared with a single comparator. When  $V_{load}$ , which is the same as  $V_{out}$ , and  $I_{load}$  are specified and the output power of the RF rectifier is not capable of yielding the load power demand, the duty cycle operation is activated. Hence, the delivered power to the load is lowered by the value of the duty cycle while meeting the load requirements for specific periods. To control the power flow to the load, the

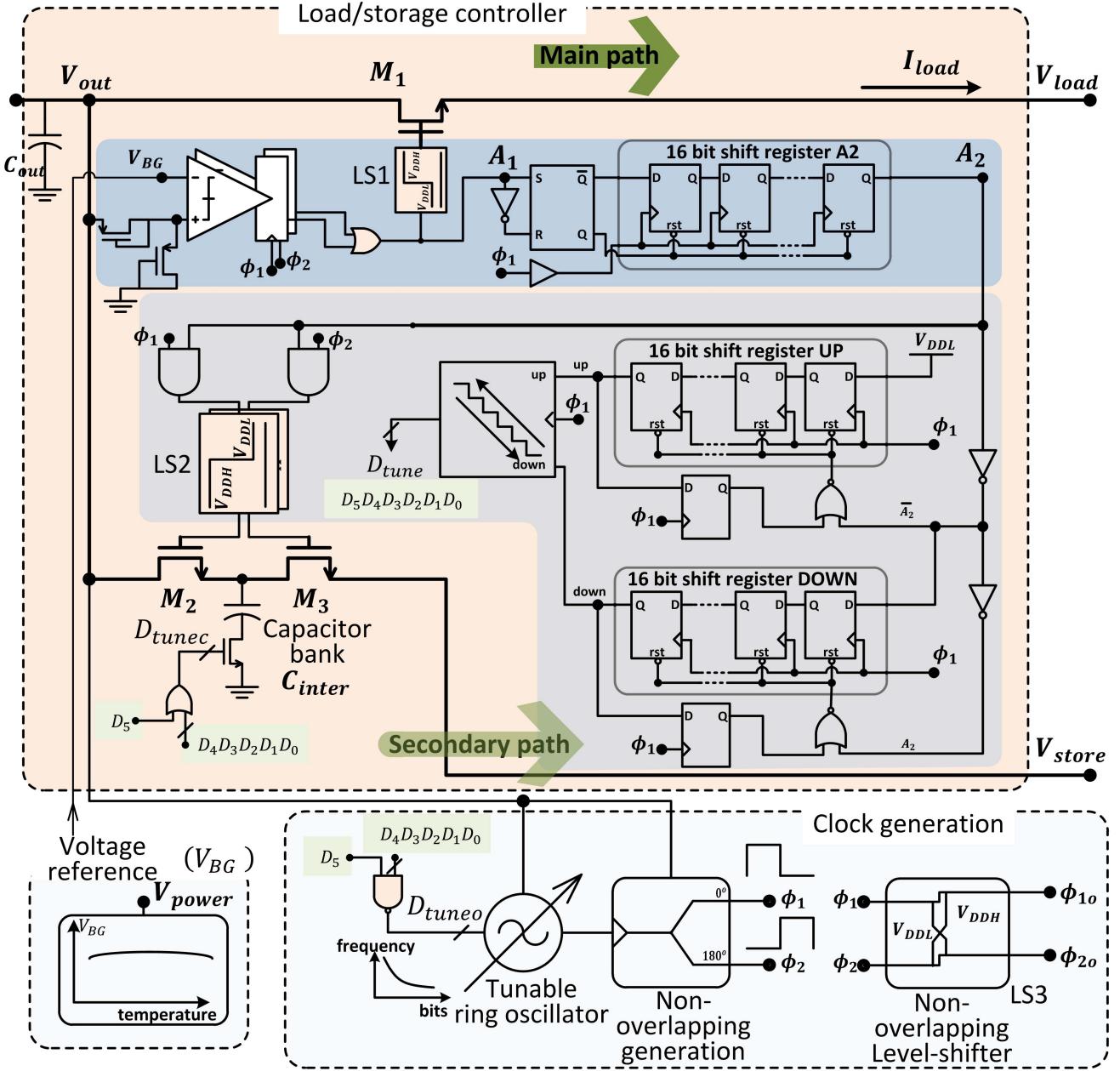


Fig. 5. Power management/controller: clock generation, voltage reference, and power storage controller.

gate of device  $M_1$  at the top of Fig. 5 is switched through a level shifter. As the available output power is high enough, signal  $A_1$  is sensed for being high for a period of time, specified here by a 16-b shift register A2. As a result, signal  $A_2$  goes to high, which activates the *secondary path*. If the value of  $A_1$  drops to zero, a reset is used for the shift registers, and the system waits again to raise the signal  $A_2$ . If the signal  $A_2$  is high, the delay of the 16-b shift register UP is used to check that  $A_2$  is being high for this time. After that delay, the signal *up* goes to high; otherwise, a reset to the shift register UP is used. When the signal  $A_2$  is low, the delay of the 16-b shift register DOWN is used to make sure that  $A_2$  is being low during this time. Then, the signal *down* goes to high; otherwise, a reset to the shift register

DOWN is used. The *up* and *down* signals control a 6-b binary counter that is implemented with maximum–minimum limiter logics. The control output word  $D_{tune}$  (at the middle of Fig. 5) of the counter is used to generate the control word  $D_{tuneo}$  and  $D_{tunec}$  to control the oscillator frequency and the value of  $C_{inter}$ , respectively (at the bottom left of Fig. 5). The frequency of the oscillator is inversely proportional to the equivalent digital number of the control bits; hence, a NAND gate is used to invert the logic signals. When  $D_5$  is low, the capacitor  $C_{inter}$  is proportional to the value of the vector  $D_4D_3D_2D_1D_0$ , and the minimum frequency is used. When  $D_5$  is high, the maximum capacitance is used, while the frequency is tuned with a frequency proportional to the value of the same vector.

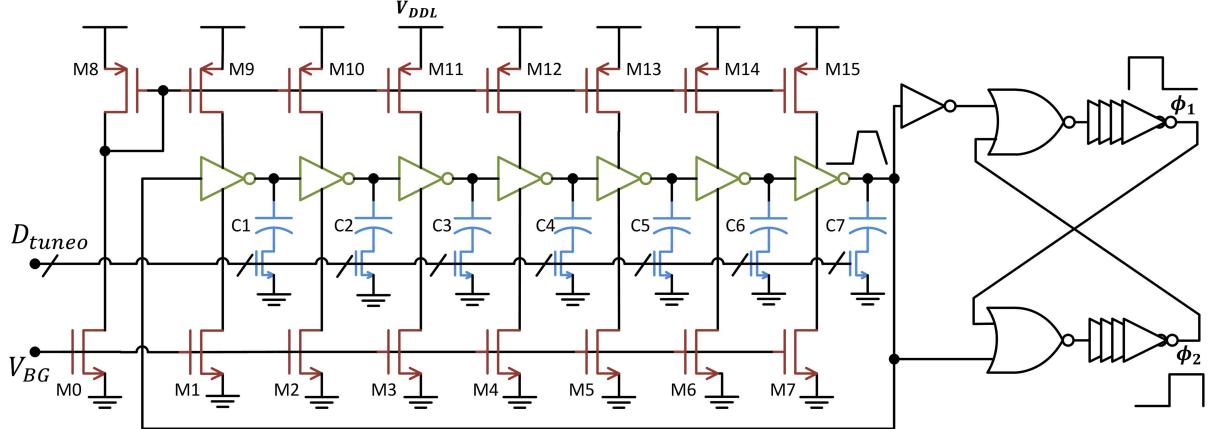


Fig. 6. Tunable ring oscillator and nonoverlapping clock generation.

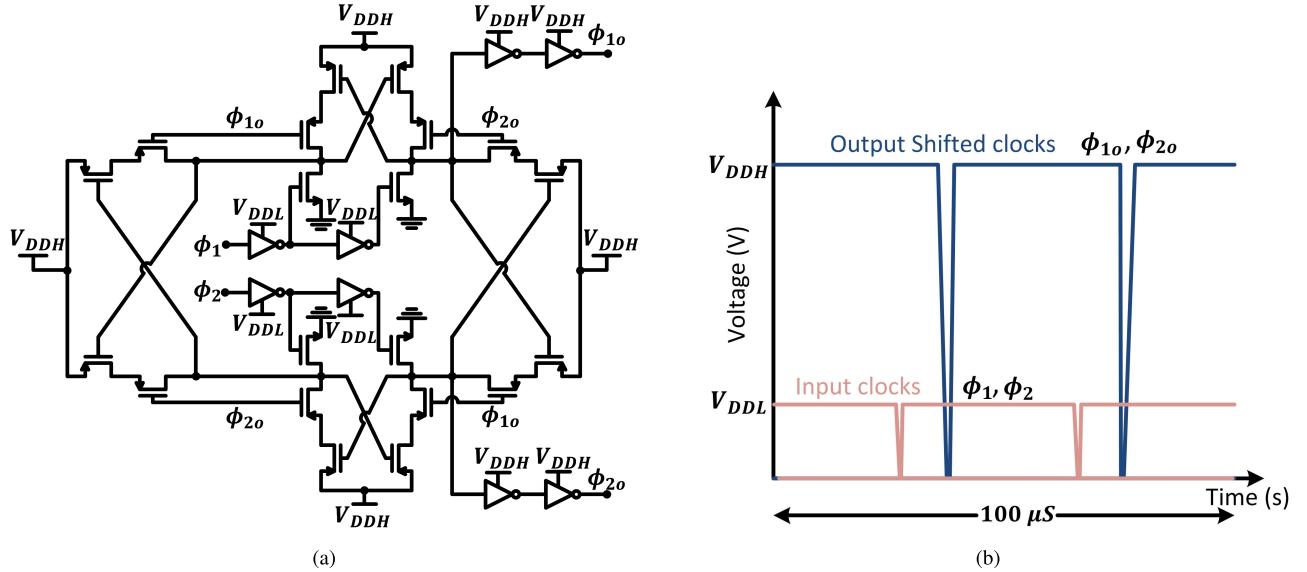


Fig. 7. Proposed nonoverlapping cross-coupled level shifter. (a) Circuit. (b) Simulation with exaggerated rise/fall times for illustration.

A tunable ultralow power current-starved ring oscillator is shown in Fig. 6. The oscillator frequency is tuned through the digital capacitor bank  $C_1$ - $C_7$ . The voltage of the current-starved devices,  $M_1$ - $M_7$  and  $M_9$ - $M_{15}$ , is obtained from the  $V_{BG}$ , which is low when the available output power is small, and the oscillator takes less current at start-up. The oscillator feeds a nonoverlapping clock generation block that produces two phases,  $\phi_1$  and  $\phi_2$ . The clock generation chain with the oscillator consumes 26 and 117 nA for the lowest and highest frequencies, respectively. Fig. 7(a) shows the proposed nonoverlapping level shifter (LS3) to shift  $\phi_1$  and  $\phi_2$  to  $\phi_{1o}$  and  $\phi_{2o}$ , respectively. The block takes nonoverlapping input signals and produces level-shifted versions, as shown in Fig. 5. The implementation is done through cross coupling of the two level shifters. The use of two regular level shifters cannot guarantee the nonoverlapping operation of the output clocks, which is important to minimize the losses in the digital circuits. Simulation results for the nonoverlapping behavior are shown in Fig. 7(b). The nonoverlapped high voltage signals

$\phi_{1o}$  and  $\phi_{2o}$  are used for the implementation of the controller of the RF rectifier as will be shown.

In Fig. 8, the voltage reference [10] is shown, which is all-CMOS design. Moreover, it is the only analog block, which consumes static power.  $M_{11}$ ,  $M_{12}$ , and  $M_{33}$ - $M_{35}$  are used for start-up, and the remaining devices are the core circuit of the reference generator. The reference voltage output  $V_{BG}$  is 0.52 V, where the load capacitance at the output will affect the start-up time, which is critical from a system point of view. This design was optimized for low power consumption with 40-nA current consumption. Other implementations can be used for better accuracy at the expense of consuming more power.

Table I shows the truth table for the signals of the control switches of the reconfigurable RF rectifier. A 1-b per subblock  $SW(1, 2 \dots 7)$ , shown in Fig. 4 in the bottom right side, is needed. The bits are generated by three independent signal controls,  $N_0$ ,  $N_1$ , and  $N_3$ . Signal  $N_3$  is used, instead of  $N_2$ , to highlight that  $N_2$  will be redundant and is equal to  $N_0$ . The

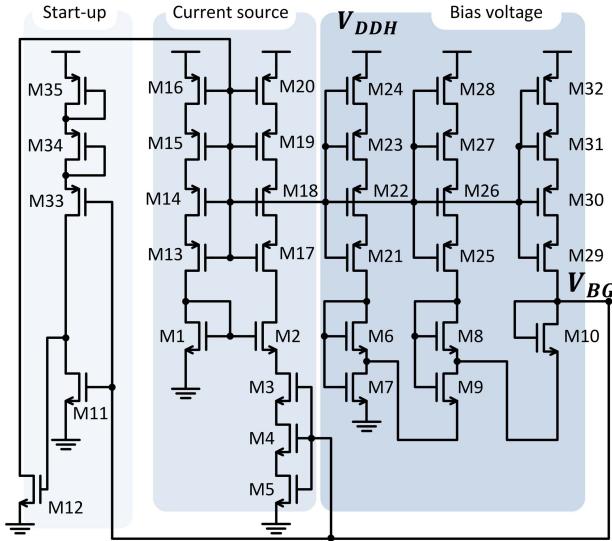


Fig. 8. Voltage reference generation.

TABLE I

TRUTH TABLE FOR THE SIGNALS OF THE CONTROL SWITCHES OF THE RECONFIGURABLE RF RECTIFIER

Switch Signals (in Fig. 4)		SW7	SW6	SW5	SW4	SW3	SW2	SW1
Control bits		$N_0$	$N_1$	$N_0$	$N_3$	$N_0$	$N_1$	$N_0$
$N$	8	0	0	0	0	0	0	0
	4	0	0	0	1	0	0	0
	2	0	1	0	1	0	1	0
	1	1	1	1	1	1	1	1

implementation of the controller of the RF rectifier circuit is shown in Fig. 9. The controller of the RF rectifier senses the voltage of the last nonreconfigurable stage  $V_{\text{th},\text{stage}}$ , which is proportional to the open circuit voltage of one stage and, then, compares it with different threshold levels. As the available output power and the value of  $V_{\text{th},\text{stage}}$  increase, fewer stages are used to obtain better efficiency. The value of  $V_{\text{BG}}$  is designed to be 1/4 of the desired open circuit voltage  $V_{\text{th}}$ , for this  $N = 8$  design, where scaling is used between the values of  $V_{\text{th},\text{stage}}$  and  $V_{\text{BG}}$  in order to maintain low voltage operation. The estimation of  $V_{\text{th}}$  by a multiple value of  $V_{\text{th},\text{stage}}$  is valid, given that the loading current from the auxiliary RF rectifier is small, compared with the current supplied by the main RF rectifier. The switching signals SW1, SW3, SW5, and SW7 are the same, since all odd stages shall be either connected to the output or to the next stage. For the switching signals connected to even stages, there should be symmetry in control signals between the beginning and the ending of the reconfigurable RF rectifier; hence, SW2 and SW6 have the same signals. A switched capacitor  $C_1$  voltage difference circuit is used to measure the voltage  $V_{\text{th},\text{stage}}$  periodically, and a deep-subthreshold voltage divider is used to get  $V_{\text{th},\text{stage}}/2$  and  $V_{\text{BG}}/2$ . High voltage clocks are needed for sampling, and the nonoverlapping level shifted signals  $\phi_{1o}$  and  $\phi_{2o}$  are used. This prevents the shoot-through current loss. Moreover, latched

comparators, logic circuits, and shifters generate the required control bits to decide the number of stages. There is no direct interaction between the controller of the RF rectifier and the power management/controller, as shown in Fig. 5. However, the former circuit, with a fast path, directly controls the final open-circuit voltage of the RF rectifier, which indirectly affects the signals of the latter. The loop of the control of the RF rectifier has a faster response by having less delay than the loop of the power management/controller.

#### IV. BEHAVIOR OF THE RF RECTIFIER FRONT END

As shown in Fig. 2, the RF rectifier is composed of a cascade of multiple ac-to-dc conversion stages. Each stage converts the ac input and feeds its dc output  $V_{\text{dc}}$  into the next stage [8]. The dc voltage is accumulated from one stage to the next. The final dc output voltage  $V_{\text{out}}$  is related to the number of series stages  $N$  by the relation:  $V_{\text{out}} = NV_{\text{dc}}$ . The main parameters of the RF rectifier are: harmonic content, input admittance ( $Y_{\text{in}} = G_{\text{in}} + jB_{\text{in}}$ ), output dc current ( $I_{\text{dc}}$ ), and PCE ( $\text{PCE}_{\text{rect}}$ ).

The input admittance is the parallel combination of a resistive part  $G_{\text{in}} = 1/R_{\text{rect}}$  and a reactive part  $B_{\text{in}} = 1/X_{\text{rect}}$ . The value of  $R_{\text{rect}}$  is related to  $V_{\text{in}}$  and  $I_{\text{in}}$ , which are the fundamental amplitudes of the input ac voltage and current, respectively. It should be noted that  $R_{\text{rect}}$  is the ac equivalent input resistance, while the Thevenin equivalent resistance  $R_{\text{th}}$ , shown in Fig. 3, is the dc output equivalent resistance.  $R_{\text{rect}}$  is analyzed using the nonlinear operation of the diodes. The nonlinear voltage-dependent capacitance of the p-n junctions, which is part of the diode-connected devices, contributes to the input capacitance of the RF rectifier. The average value of the nonlinear capacitance, as discussed in [11], is dependent on the voltage swing and the power levels across the p-n junctions. This will affect the Thevenin equivalent resistance  $R_{\text{th}}$ , the matching network performance, and will introduce mismatch. In [12], an automatic tuning feedback loop was introduced. Here, the matching network is preset for the low input power levels. The PCE is given by

$$\text{PCE} = \frac{P_{\text{dc,out}}}{P_{\text{in,fundamental}}} \quad (4)$$

where  $P_{\text{dc,out}}$  is the delivered dc output power and  $P_{\text{in,fundamental}}$  is the fundamental ac input power to the RF rectifier. Moreover, the total input admittance of the  $N$ -stage RF rectifier is the parallel combination of the resistance of each stage [8], where the outputs of the subblocks of the RF rectifier are ac ground.

When the input power is low, both the RF current and voltages at the input terminal of the RF rectifier are sinusoidal. As the input power increases, while the current is approximately sinusoidal, the voltage waveform starts to deviate from the sinusoidal behavior, and the RF rectifier operates in a current-mode operation. Harmonic balance should be used where nonlinearities of both currents and voltages appear dominant. Thus, the rectifier can operate in two modes [13]: the voltage-mode and the current mode, which are equivalent to low-input power and high-input power modes, respectively. The modeling of the RF rectifier is described elsewhere [14].

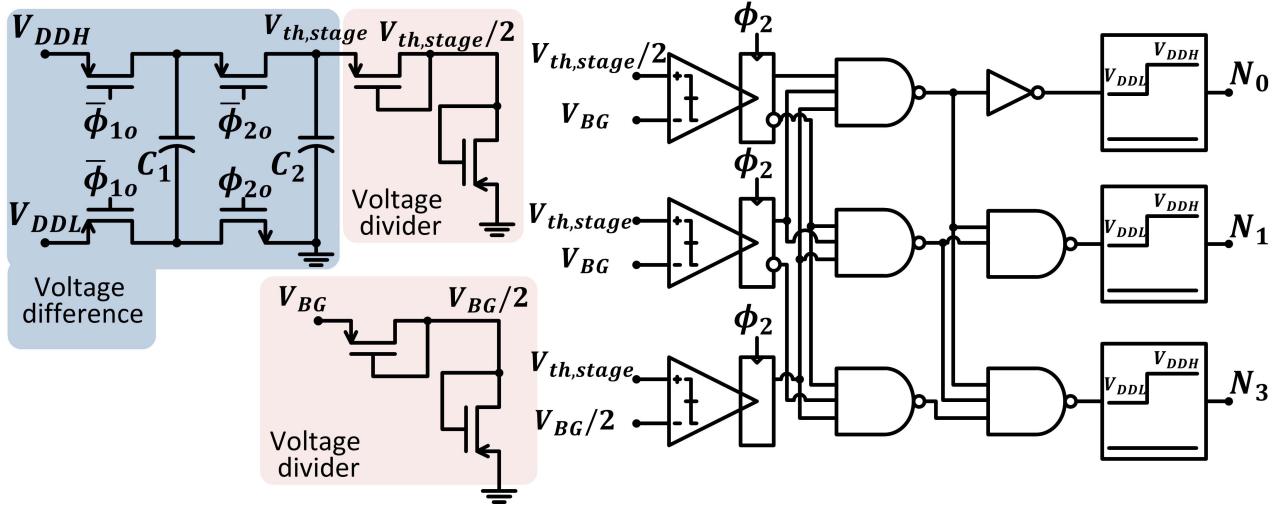


Fig. 9. Controller of the RF rectifier circuit implementation.

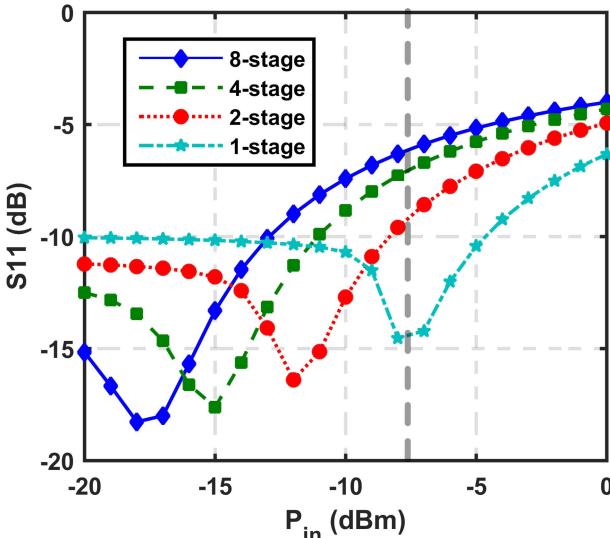


Fig. 10. Large-signal S-parameter simulation, while input power is varied.

#### A. Number of Stages and Input Amplitude Effects

As shown in Fig. 10, a large-signal S-parameter transistor level simulation is plotted for different stage configurations. The return loss  $S_{11}$  of the RF front end is plotted while sweeping input power, maintaining a constant output voltage of 1 V and using a preset configuration for the matching network. The system shows that the input matching can be maintained over a wider input range compared with a single configuration. For example, at  $P_{\text{in}} = -7.5$  dBm, the use of an eight-stage configuration yields a return loss of  $-6$  dB, which results in a reflection loss of  $1.26$  dB, while the use of a one-stage configuration yields a reflection loss of  $0.14$  dB. This directly affects the efficiency of the RF front end with the percentages of  $86.5\%$  for the former case and  $98.4\%$  for the latter case. Thus, reconfiguration can maintain the input matching conditions and reduce reflection loss. We concluded that automatic tuning of the matching network does not satisfy the overhead and, thus, can be omitted.

The PCE increases (or decreases) as the number of stages decreases (or increases) while using all subblocks. It is desirable to have the lowest number of stages in order to increase the available output power. On the other hand, a minimum number of stages must be used to get sufficient dc output voltage for small inputs. Thus, as the input amplitude increases (or decreases), the number of stages should decrease (or increase) and the rectifier is required to have more (or less) stages to generate a required dc output voltage.

#### B. Matching Network Design

The tunable matching network can be considered as a cascade of three  $L$  matching sections [15], as shown in Fig. 4 at the top right side: the first section is composed of the input capacitance  $C_{\text{rect}}$  of the rectifier and  $L_{M1}$ , while the second section is represented by  $C_{BM1}$  and  $L_{M2}$ . The third section consists of  $C_{BM2}$  and the bonding wire with any parasitic inductance to the source. The objective of the matching network is to transform the source (antenna) impedance, which is  $50 \Omega$ , to the rectifier input resistance  $R_{\text{rect}}$ , while absorbing the value of  $C_{\text{rect}}$  into the design. The desired impedance to each  $L$  section is  $R_s$ . Moreover, each  $L$  section is loaded by  $R_p$ , where  $R_p$  is the input impedance of the next  $L$  section, and the loaded quality factor is  $Q_i$ . Hence, the design equations [15] are

$$R_p = (1 + Q_i^2) R_s \quad (5)$$

$$Q_i = \frac{\omega_o L_{Mi}}{R_s} \quad (6)$$

$$L_{Mi} C_{Mi} = \omega_o^2 \quad (7)$$

where  $\omega_o$  is the operating frequency (900 MHz is used), and  $C_{Mi}$  and  $L_{Mi}$  are the capacitance and inductance of each section, respectively and  $i = 1, 2, \dots, n$ . The total efficiency is the product of the efficiencies of the individual sections. Due to the limited quality factor  $Q_L$  of the on-chip inductors, which are typically between 6 and 7, [16] showed that in order to maximize the total efficiency, the values of  $Q_i$  should be

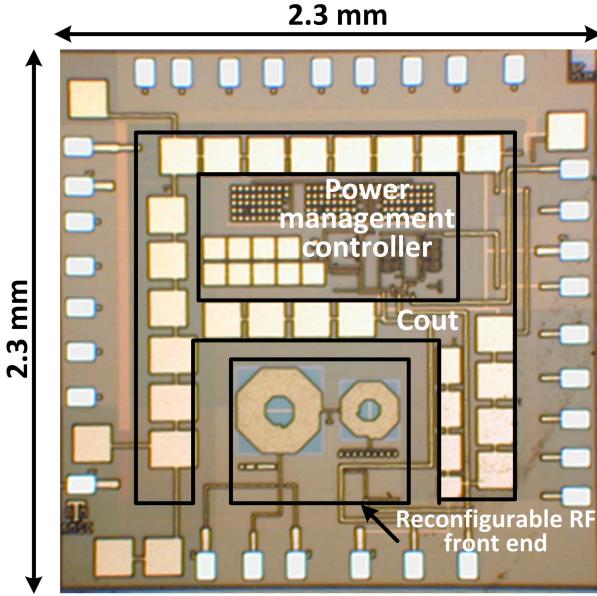


Fig. 11. Micrograph of the RF energy harvesting system prototype IC.

equal. This imposes a constraint on the interface impedance between the sections. Thus,  $Q_i$  will be

$$Q_i = \sqrt{\left(\frac{R_{\text{rect}}}{R_{s,50}}\right)^{1/n} - 1} \quad (8)$$

and the overall efficiency would be

$$\eta = 1 - \frac{n}{Q_L} \sqrt{\left(\frac{R_{\text{rect}}}{R_{s,50}}\right)^{1/n} - 1} \quad (9)$$

where  $n = 3$  and the first section, composed of  $L_{M1}$  and  $C_{\text{rect}}$  is not fully controllable, since  $C_{\text{rect}}$  is defined by the input capacitance of the RF rectifier. The expected voltage boosting of the matching network is given by  $(R_{\text{rect}}/R_{s,50})^{1/2}$ .

## V. EXPERIMENTAL RESULTS

The proposed RF energy harvesting system was designed and fabricated using the 0.18- $\mu\text{m}$  CMOS technology. The die photo is shown in Fig. 11, the active chip area is  $1.08 \text{ mm}^2$  where the area of the reconfigurable RF front end is  $0.756 \times 0.624 \text{ mm}^2$ , and the power management/controller takes  $1.084 \times 0.56 \text{ mm}^2$ .

The RF front end consists of the  $LC$  matching network and the reconfigurable RF rectifier. The values of  $L_{M1}$  and  $L_{M2}$  are, respectively, 12.6 and 30 nH with the chip areas of  $260 \times 260 \mu\text{m}^2$  and  $360 \times 360 \mu\text{m}^2$ . On the antenna side, the loaded quality factor is small, which permits the use of lower quality factor with a higher inductance value  $L_{M2}$  to achieve the input matching. On the other hand, the loaded quality factor on the input of the rectifier is high, so  $L_{M1}$  is chosen for maximum quality factor  $Q_L$  (about 8). The maximum values of the tunable capacitors  $C_{BM1}$  and  $C_{BM2}$  are 300 fF and 5.7 pF, respectively, excluding the parasitic capacitance at the inductor terminals. The test setup for the RF front end is shown in Fig. 12(a). Moreover, Fig. 12(b) shows the test

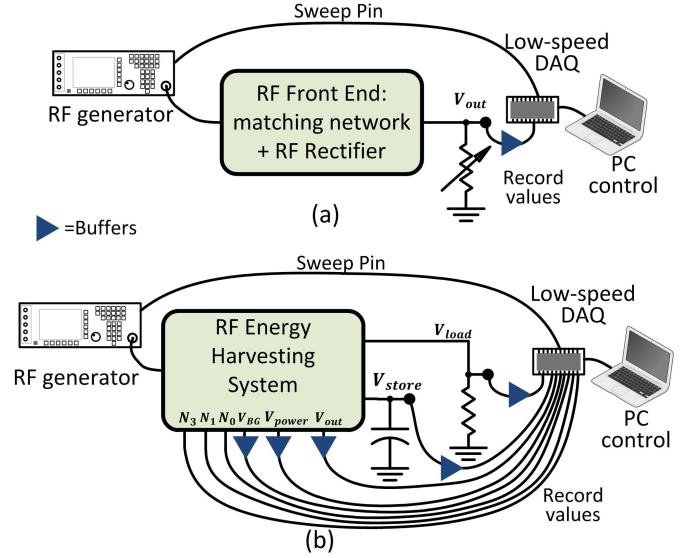


Fig. 12. Test setup for (a) RF front end and (b) RF energy-harvesting system.

setup for the total system, which will be described shortly. A data acquisition (DAQ) card is used to control the input power sweep of the RF generator and to record the values of the output voltages. The RF front end is measured for all configurations of the RF rectifier in Fig. 13. Note that the right vertical axes have ranges that are different for the subfigures. Output voltage versus input power for different load currents is plotted. This test measurement was conducted for a range of load resistances from  $2 \text{ k}\Omega$  to  $10 \text{ M}\Omega$ . It was done with external switching signals with a 1.8-V supply level. In Fig. 13(a), an eight-stage configuration is used. When  $P_{\text{in}} = -18 \text{ dBm}$ , the RF front end will provide a 1-V dc output voltage for a load resistance of  $10 \text{ M}\Omega$ . Note that the delivered current range is from 0 to  $120 \mu\text{A}$  for the input power range from  $-25$  to  $2.5 \text{ dBm}$ . In Fig. 13(b), with the use of four-stage configuration, the delivered current range extends from 0 to  $220 \mu\text{A}$  for the same input power range while delivering an output voltage of 1 V at higher input power range than shown in Fig. 13(a). The use of two-stage and one-stage in Fig. 13(c) and (d), respectively, widens the current delivery to ranges between 0 and  $380 \mu\text{A}$  and between 0 and  $500 \mu\text{A}$  while delivering an output voltage of 1 V for the high input power ranges. At the lowest load and high power delivery, the switching signals at the gate of the switches are not high anymore with respect to the source/drain, and that is why, the output voltage is almost unchanged. With ideal switches, the output voltage of the RF rectifier is expected to rise monotonically, as the number of stages increases despite maintenance of the same input power, which raises reliability issues of the fabricated chip. For nonideal switches, the voltage output voltage is decreased by the values of the voltage drop across the switches, which is proportional to  $I_{\text{out}} R_{\text{ON}}$  and the configured number of stages (one, two, four, or eight).

It is appropriate here to consider the PCE of the main load path compared with the previous results. But when the two paths are considered, due to nonideal losses, the PCE is degraded (as will be shown). The PCE versus input power,

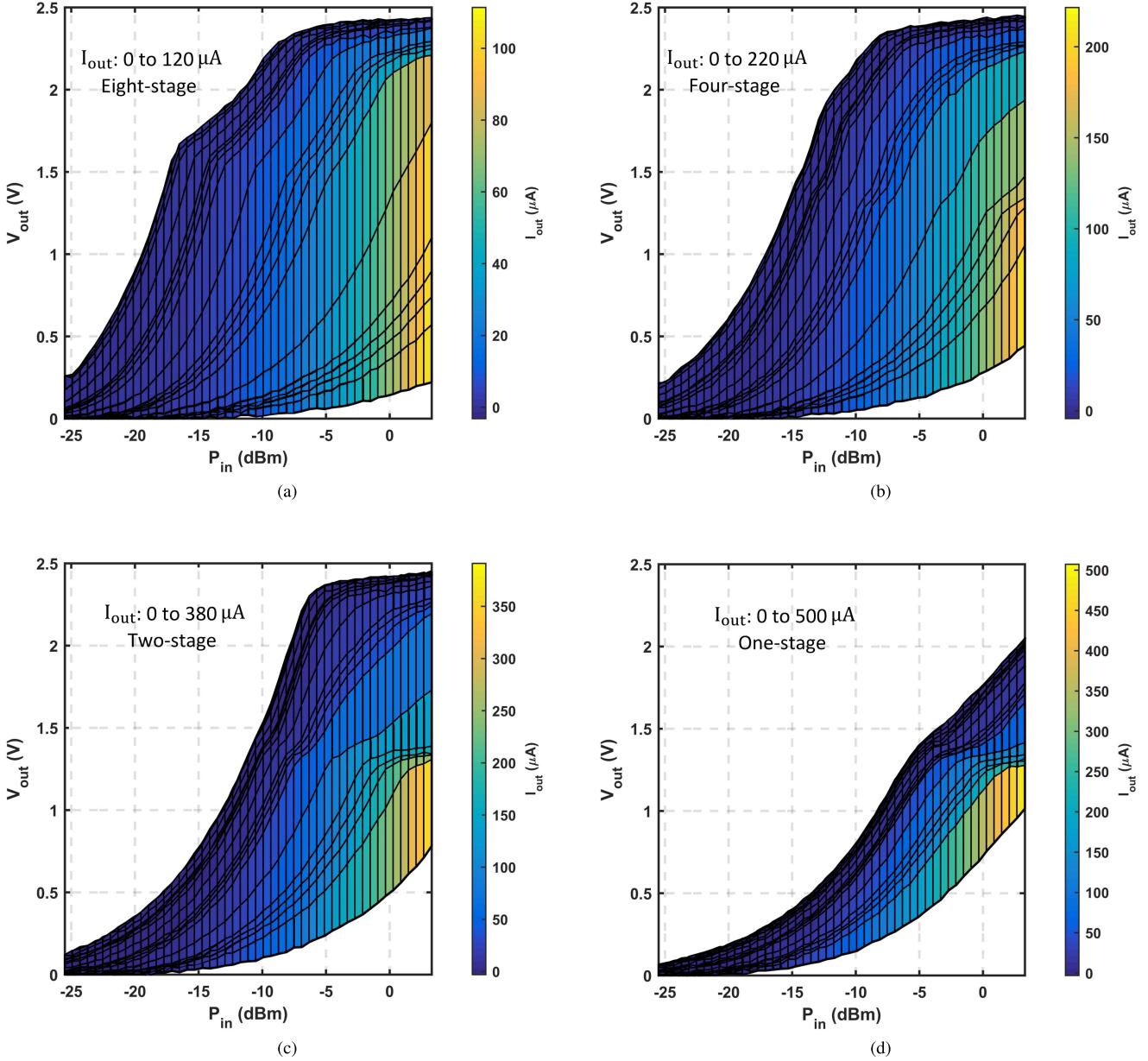


Fig. 13. Steady-state measurements of the output voltage for the cascade of the reconfigurable RF rectifier and the on-chip matching network versus the input power  $P_{\text{in}}$  for different output currents  $I_{\text{out}}$  (more current obtained for fewer stages). (a) Eight-stage. (b) Four-stage. (c) Two-stage. (d) One-stage.

considering only the main path, is shown in Fig. 14 where the PCE is plotted for output voltage greater than 1 V. This constraint on the output voltage is arbitrary, and depends on the system design of the power management circuit succeeding the RF rectifier. When the output voltage is less than 1 V, the PCE is plotted as zero. The plot shows that at low input power, a higher number of stages are required to get the sufficient output voltage. As the input power increases, fewer stages are needed. Moreover, each configuration of the RF rectifier has an input power range, where the PCE is maximal. The total PCE is defined as

$$\text{PCE} = \eta_{\text{matching}} \text{PCE}_{\text{rect}} \quad (10)$$

where  $\eta_{\text{matching}}$  is the efficiency of the matching network and  $\text{PCE}_{\text{rect}}$  is the PCE of the RF rectifier.  $\eta_{\text{matching}}$  is dependent

on the quality factor of the matching elements, where off-chip equivalent elements for a non  $50\text{-}\Omega$  antenna/rectifier interface [12] and potential system-in-package elements [17] give an advantage. On the other hand,  $\text{PCE}_{\text{rect}}$  is process dependent, where the characteristics of the diodes, mainly the threshold voltage and leakage current, affect this number. Different processes, such as silicon-on-insulator and high-performance customized processes [17], give performance advantage, where similar results for RF power amplifiers are published in the literature. The product [17] has a higher PCE with a large package of  $0.625 \times 0.53 \text{ in}^2$ , and the details of the design and the fabrication technology are not published. Therefore, it is difficult to compare with the proposed design.

In addition to that, the reconfiguration of the number of stages of the RF rectifier introduces ohmic losses on the

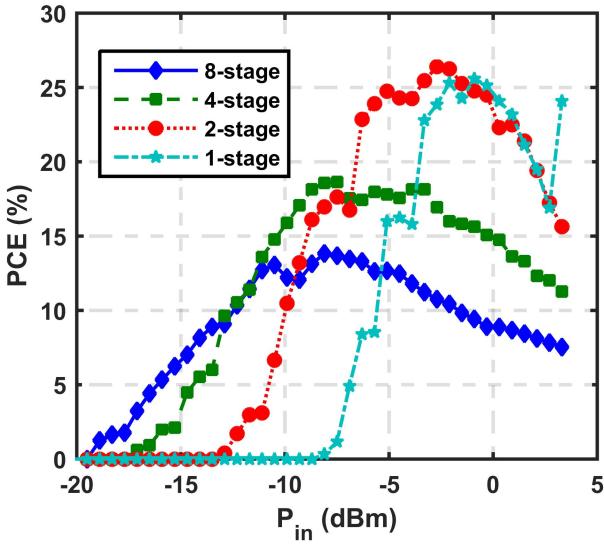


Fig. 14. PCE, including the matching network and the RF rectifier, versus input power  $P_{in}$  for different stage configurations for output voltage greater than 1 V.

dc side of the rectifier, which should be, by careful design of the reconfiguration switches, small; however, they eventually contribute to the losses of the RF rectifier.

The total RF energy harvesting system is measured at startup conditions to show the duty cycling capability of the system as shown in Fig. 15 where the load voltage  $V_{load}$  starts from 0% duty cycle to 100% at a sufficient input power. The steady-state duty cycle is plotted versus the input power. The test setup for the RF energy harvesting system is shown in Fig. 12(b). The DAQ card is used for recording values of different signals, and sending control signals to the RF generator. Then, the transient measurement results of the system are shown in Fig. 16 for different wider ranges  $P_{in}$  with a demand current of 1  $\mu$ A represented by 1-M $\Omega$  resistance and a  $C_{store}$  of value 100  $\mu$ F. The measurement results are obtained by sweeping input power in 2.5-dB steps from -19.2 to 0.8 dBm, where each lasts for 10 s. At low power, the controller circuit powers up, and the sensitivity for that is measured at -14.8 dBm, when the load begins to receive the duty cycled current. As  $P_{in}$  increases, the number of stages decreases. The voltage reference is constant with  $V_{power}$  except for supplies exceeding 3 V.  $V_{load}$ , the storage capacitor voltage  $V_{store}$ ,  $V_{out}$ , and  $V_{power}$  are shown in Fig. 16. At low input power and low available output power, the load current is duty cycled and no power is delivered to  $C_{store}$ . As the input power increases, the load current is continuous, the output voltage is designed to be regulated to twice  $V_{BG}$ , and charges are transferred to  $C_{store}$ , where the secondary path is used to absorb the extra energy. The values of the maximum frequency  $f_s$  and maximum capacitance  $C_f$  limit the maximum extra absorbed energy where in simulations, larger  $C_f$  capacitance helps to maintain the regulation at high input power levels. For the current design of the secondary path, the power extraction through this path is bounded to a value proportional to  $(1/2)C_f f_s V_{out}^2$  and the energy flow through this path saturates when the maximum  $C_f$  and  $f_s$

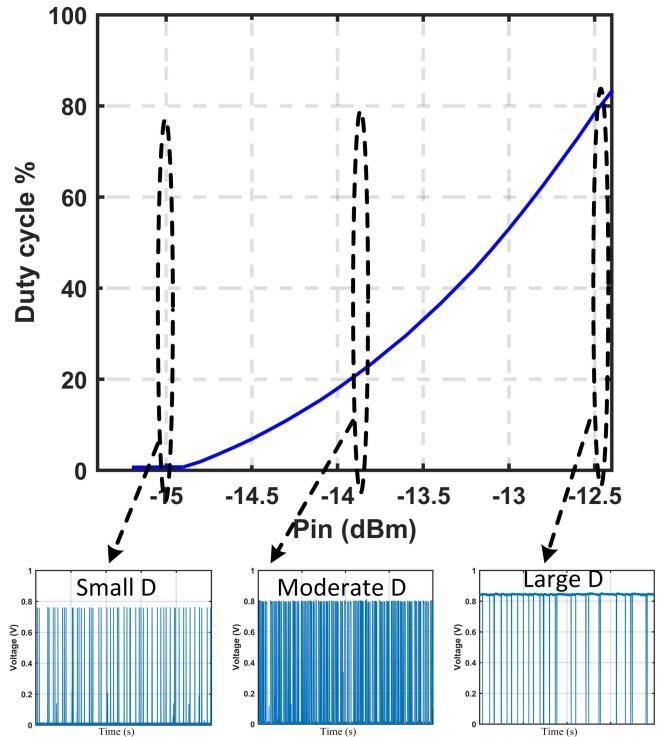


Fig. 15. Measurements of the start-up of the system versus input power with small steps to show the duty cycling feature (duty cycle D) of the system.

TABLE II  
HARVESTED ENERGY AND CONSUMPTION IN  $\mu$ JOULE FOR DIFFERENT INPUT POWER LEVELS FOR 10-s DURATION

$P_{in}$ , dBm	-15	-12.5	-10	-7.5	-5	-2.5	0
Bandgap	0.48	0.52	0.64	0.76	0.8	0.8	0.92
clock gen	0.66	0.726	0.96	1.4	1.755	1.755	1.872
harvested	6.4	8.5	11.2	16.4	25.3	26.1	30.0

are used. Therefore, the extra power needs to go somewhere, which is shown here to be a higher value of  $V_{out}$  voltage than 1 V and  $P_{out} = V_{out} I_{load}$ . The increase of  $V_{load}$  also affects the efficiency of the RF rectifier (the reported PCE in Fig. 14 is for specific loads), which will affect the end-to-end efficiency. A potential solution is to cascade a low dropout regulator (LDO) to filter any variation, since the maximum capability of the secondary path will be reached when the maximum power extraction capability is reached. This will be at the expense of more complexity and power consumption. For simplicity, no LDOs were used in the current implementation. At very high input power, higher than 0.8 dB, the secondary path reaches a higher voltage than its maximum capability, and the dc voltages start to increase; particularly, the reference voltage, which causes all the other voltages to increase at the same rate. This is a typical case for nonreconfigurable RF rectifiers, where the output voltage increases as the input power increases. But here, this is prevented from happening until a very high input power is reached, where higher maximum values of operating frequency and/or  $C_{store}$  should be used to further improve the design. The RF rectifier switches back and forth between two-stage

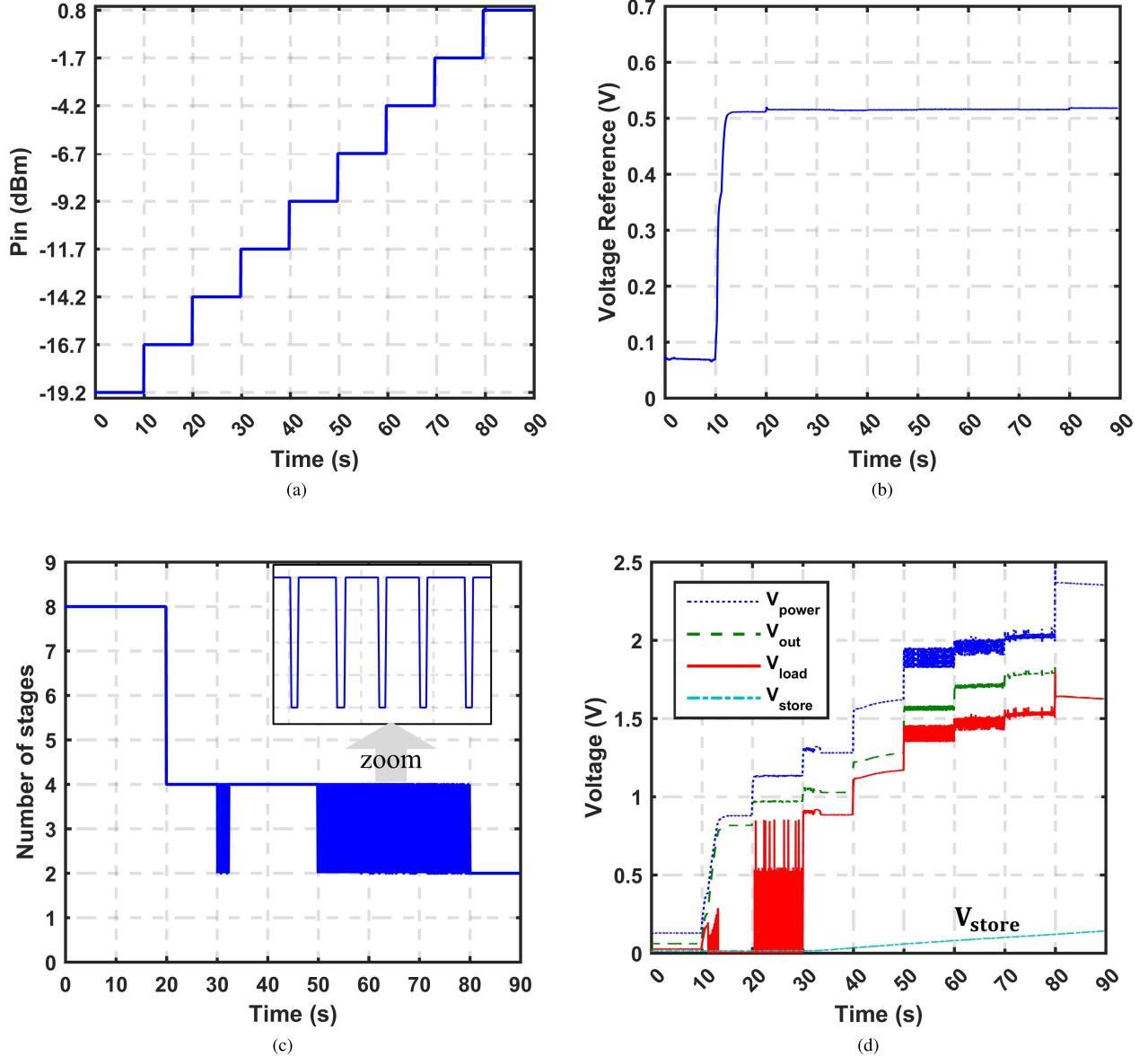


Fig. 16. Transient measurement results for sweeping input power in 2.5-dB steps from  $-19.2$  to  $0.8$  dBm, where each lasts for 10 s. (a) Sweep of the input power. (b) Startup of the reference voltage. (c) Change of the number of stages. (d) Different dc output voltages.

and four-stage configurations when the input power is between  $-6.7$  and  $-1.7$  dBm. The difference between  $V_{power}$  and  $V_{load}$  is around  $0.5$  V. The loading effect of the protection diodes introduces some errors in the estimation of the open-circuit voltage. This switching action increases the ripples on the output voltages of the system in these regions of operation, and the efficiency is degraded from the optimal value due to this estimation. More protection diodes in series will decrease this toggling error, but since a standard CMOS process, with no high voltage devices, was used, the number of series protection diodes was limited to only two, which prevented the value of  $V_{power}$  to reach high voltage. The effect of the error, due to the protection diodes, was to shift the decision points of the number of stages to be used. According to our simulations, when protection diodes are omitted (or the use of more stack of diodes), the  $(V_{power} - V_{out})$  can go to twice  $V_{out}$ . Table II shows

an estimation of the amount of harvested energy and energy consumption (power multiplied by duration) of the main building blocks at different input power levels, assuming a 10-s period. The consumption of the level shifters is not taken into account, since it is negligible provided that nonoverlap clocking is guaranteed. The harvested energy is calculated for both the load  $I_{load}$  and the storage capacitor  $C_{store}$ . To the best of our knowledge, the proposed work is the first work to harvest the extra power in an RF energy harvesting system. For the case of a fixed load shown here as  $1\text{ M}\Omega$ , about three times power is extracted at  $0$  dBm with respect to the fixed load. The limited value of  $(V_{power} - V_{out})$  will introduce losses in the switches and especially the switches near the end. Therefore, the performance of the switches suffers resulting in a poor efficiency. Also, higher values of  $V_{out}$  will degrade the RF energy harvesting front end. The  $I-V$  curve of the rectifier

TABLE III  
COMPARISON TABLE WITH THE STATE OF THE ART

	ESSCIRC2012[4]	TCAI2013[5]	JSSC2015[6]	JSSC2013[7]	This Work
Power output usage	Load	Start-up, load	Start-up	Start-up, control	<b>Start-up, power management, load</b>
Simultaneous capacitor charging and load powering	No	No	No	No	<b>Yes for extra power</b>
Bounded output voltage	No	N.A.	No	N.A.	Yes*
Frequency	915 MHz	830 MHz	915 MHz	433 MHz	915 MHz
Matching network	Off-chip	Off-chip	No matching	Off-chip	<b>On-chip and tunable</b>
Extra off-chip inductors	Yes	Yes	No	Yes	<b>No</b>
Number of stages of the RF rectifier	1-2	1**	30	6	<b>1-2-4-8</b>
Control to handle different loads	No	Yes	No	No	Yes
Sensitivity	-17 dBm @ 1.8 V (capacitive load)	-17 dBm @ 0.5 V*** (1 MΩ load)	-14.5 dBm @ 0.55 V (capacitive load)	-10 dBm @ 1.35 V (capacitive load)	<b>-14.8 dBm @ 1 V (1 MΩ load)</b>
Maximum PCE of RF rectifier+matching network	40%, 60% **** (@ -12, -2 dBm)	53% **** (@ -15 dBm)	-	-	<b>14, 18, 25, 25% (@ -11, -8, -5, 0 dBm)</b>
Current consumption	-	1560 nA	300 nA	N.A.	<b>66-157 nA</b>
CMOS technology	130 nm	180 nm	130 nm,ZVT*****	130 nm	180 nm

\*: Valid below 0.8 dBm input power.

\*\*: Differential stage and uses a boost converter (with another external power inductor) in cascade.

\*\*\*: Measurement reported @ -10 dBm & dc voltage at the output of the rectifier.

\*\*\*\*: Only RF rectifier with off-chip matching

\*\*\*\*\*:Zero Threshold Voltage devices.

has the maximum efficiency at the point where the voltage starts to decrease, and maximum current can be obtained. The maximum capability of the secondary path limits the extracted power of this path. More extracted energy can be obtained at high input power with the use of larger values of  $C_f$  in the secondary path or multiple secondary paths.

If the input power becomes low or is absent, storage capacitor  $C_{store}$ , after some charging time passes, can be used to feed the demand current, which is represented by the 1 MΩ. The off-chip capacitor  $C_{store}$ , which is an aluminum electrolyte with a value of 100 μF, is switched with an external switching circuit for the purposes of proof of concept. A low leakage switch, with leakage in the range of 1–2 nA, is also used. Fig. 17 shows the different time loading cases for 8 h. First, no power is delivered to the load and leakage effects are observed. After 8 h, the voltage across the storage capacitor is reduced by 15%. For a 10-s periodic time and the duty cycles of the 0.01%, 0.1%, and 1%, the storage capacitor is able to support the demand of the load with different lifetimes. The lifetime will be dependent on how low voltage the load can operate with. For instance, for 0.01% duty cycle, the voltage is reduced by 20% after nearly 5 h. Using lower leakage capacitors, such as film capacitors or supercapacitors, can prolong the operation of the system.

Table III shows how the design is compared with other designs in the literature. The proposed design is reported to be self-starting, incorporates power management, and delivers power to a load where previous works used RF energy harvest-

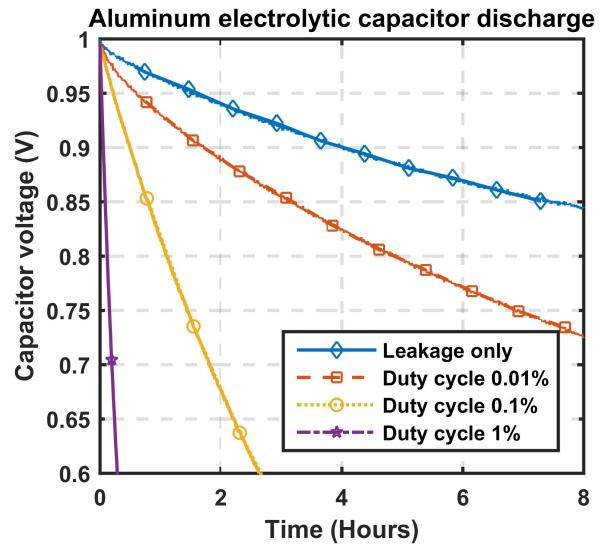


Fig. 17. Experimental results for storage capacitor delivering power to load.

ing either to start up or deliver power to a load. Simultaneous delivery of power to the load and a storage capacitor with two different paths is a unique practical feature. This can allow the separate optimization of the two paths, where the former is real time, and the latter is slow and used for long-term operation. The output dc voltage is bounded, and the design is reconfigurable to maximize the PCE. No extra off-chip inductors are used, and the passives are integrated on-chip with

tuning capability. The process is a standard 0.18- $\mu\text{m}$  CMOS, and the reported sensitivity is for a 1-V output voltage where the system startup happened and the controller is operating and taking a very low current of 66 nA for low oscillator frequency operation and it increases to 157 nA for the highest oscillator frequency. Lower voltage operation and newer technologies, with lower channel length or lower threshold voltage devices, enable better sensitivity.

## VI. CONCLUSION

A fully integrated system with an *LC* matching network, RF rectifier, clock generation, voltage reference, and power management/control circuitry is presented in this paper, yet the system features a self-startup operation with no external supply help. The full integration of all functionalities on a single CMOS chip proves to be a promising low-cost solution. In order to increase the available output power, a novel reconfigurable modular RF rectifier circuit is presented. The dc power is delivered to the load only when the voltage on the load can reach the desired voltage; otherwise, the power management waits until this condition is satisfied and delivered power is duty cycled. Moreover, the extra available output power can be stored for future usage. This two-path power delivery scheme enables the support of real-time loads, increases the extracted power from the RF front end, and stores the extra power in external storage elements. For the proof of concept, only one secondary path is used, but multiple secondary paths can be incorporated to enhance the extraction capability of the extra available power at the expense of more complex logic circuits. Finally, a new circuit for nonoverlapping level shifters is proposed and used in the design to overcome shoot-through power loss.

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