

# A 0.92-THz SiGe Power Radiator Based on a Nonlinear Theory for Harmonic Generation

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**Abstract**—We propose a nonlinear device model and a systematic methodology to generate maximum power at any desired harmonic. The proposed power optimization technique is based on the Volterra–Wiener theory of nonlinear systems. By manipulating the device nonlinearity and optimizing the embedding network, optimum conditions for harmonic power generation are provided. Using this theory, a 920–944-GHz frequency quadrupler is designed in a 130-nm SiGe:C process. The circuit achieves the peak output power of  $-17.3$  and  $-10$  dBm of effective isotropic radiated power and consumes 5.7 mW of dc power. To the best of our knowledge, this circuit demonstrates the highest generated power among Si/SiGe-based sources at this frequency range.

**Index Terms**—Device nonlinearity, frequency multiplier, frequency quadrupler, harmonic power, optimum activity conditions, power maximization, power radiators, SiGe, terahertz (THz).

## I. INTRODUCTION

**A**GROWING interest in submillimeter-wave (0.3–3 THz) circuits and systems has been witnessed within the last decade. This is mainly due to the plethora of opportunities within this previously unexplored electromagnetic spectrum [1]–[4]. The characteristic of absorption profiles and proliferation of molecular resonances make this region of spectrum a unique platform of material spectroscopy. A higher spatial resolution compared with lower frequency ranges and the nonionizing nature compared with the higher frequency radiations (e.g., the X ray) adds to the exclusive features of the terahertz (THz) frequency window for imaging applications [4]–[6].

At the early stages of investigation, compound semiconductors [7]–[15], gifted with a high-speed operation potential ( $f_{\max} > 300$  GHz) and quantum cascade lasers [16], brought the hope of THz power generation. However, they did manifest challenges such as stringent operation requirements (e.g., the low temperature) and high cost. CMOS circuits were investigated as the next platform due to their lower cost and integration capability. The first CMOS millimeter-wave circuits were high bandwidth transceivers and imaging/sensing circuits [17]–[33].

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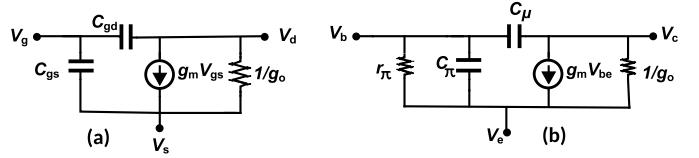


Fig. 1. Simplified circuit models of (a) MOS transistor and (b) BJT transistor.

After the successful demonstration of CMOS millimeter-wave circuits, fundamental and harmonic oscillators [34]–[47] were designed to reach a higher operation frequency. Due to the insufficient dc-to-RF efficiency and the limited bandwidth of the oscillators, frequency multipliers were explored to boost the performance [48]–[52]. Despite the high output power of passive and active CMOS frequency multipliers, frequency tuning [53], phase-locked operation [54], [55], and closer to  $f_{\max}$  operation [56], [57] were the pending milestones before a submillimeter-wave transceiver could be demonstrated.

In a parallel route, the feasibility of on-chip antenna demonstration opened the path for THz radiators [58], [59] and detectors [60]–[63]. The novel radiation techniques introduced in [60]–[64] were later used in phased arrays [65].

At the THz range where CMOS has limited capabilities, the BiCMOS technologies joined the relay and ignited the path toward higher power generation [55], [64]. The higher breakdown voltage, the higher operational frequency ( $f_{\max} > 300$  GHz), and the more nonlinear  $I$ – $V$  characteristic were the assets that CMOS lacked. Taking advantage of these unique features in [55], 3.3 mW of power was achieved at 320 GHz in a ( $f_T/f_{\max} = 220/280$  GHz) process. Similarly, in [64], 1 mW of power was generated at 0.53 THz inside a reconfigurable array.

In all the mentioned beyond  $f_{\max}$  demonstrations, the power extraction is through the harmonics of the fundamental frequency. Previous works on maximizing the fundamental power [57], [59] could enhance the harmonic power significantly due to the operation in a more nonlinear region. However, the power generation at higher harmonics still requires a thorough modeling of the harmonic signal. A systematic design methodology to generate maximum harmonic power based on a nonlinear model remains as the missing piece before circuit designers could demolish the obstacle of beyond 1 THz operation using the existing transistor technologies.

In order to push the operation limits of electronic circuits, a systematic design approach is required. The proposed design methodology should provide an accurate model of the

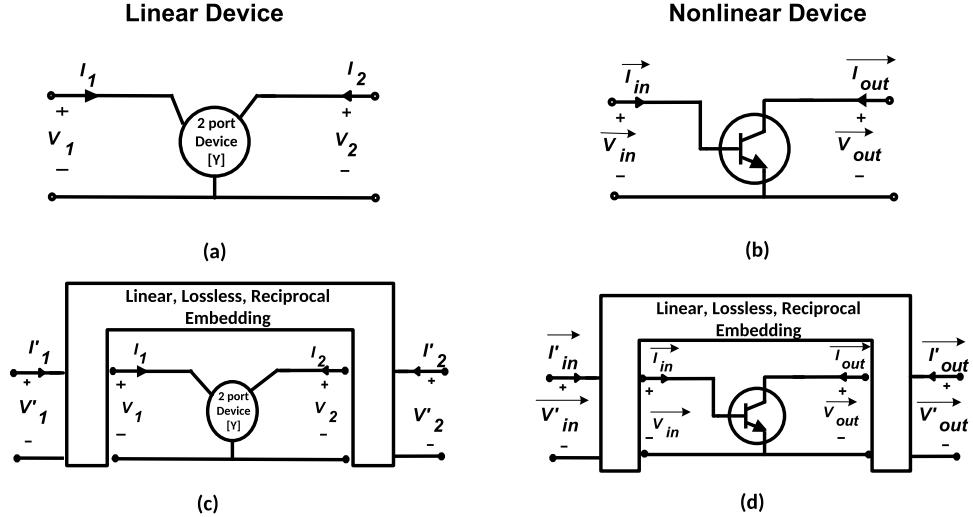


Fig. 2. (a) Three-terminal linear two-port device. (b) Three-terminal nonlinear two-port device. (c) Linear device embedded in a four-port network. (d) Nonlinear device embedded in a four-port network.

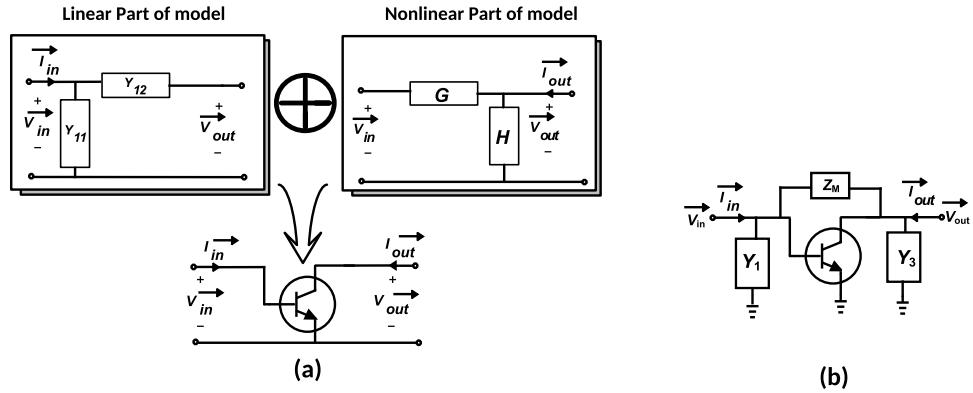


Fig. 3. (a) Nonlinear two-port representation of device and (b) that embedded with a general passive network.

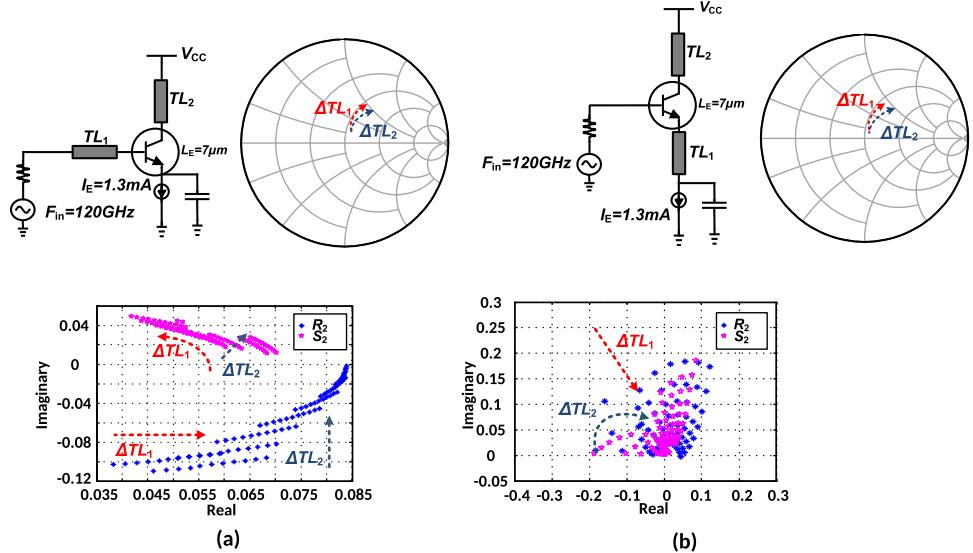


Fig. 4. (a) Variations of  $R_2$  and  $S_2$  with respect to the illustrated changes of  $TL_1$  and  $TL_2$ . (b) Similar variations on the transmission line values in a different topology. For an identical transistor, the topology determines the behavior of the ratio functions.

nonlinear device. Moreover, the effect of circuit topology and the embedding network on the harmonic power should be characterized. This is the main intention behind the proposed

design approach in this paper. We introduce a nonlinear characteristic of the active device based on the Volterra theory [67], which can be exploited to model any arbitrary

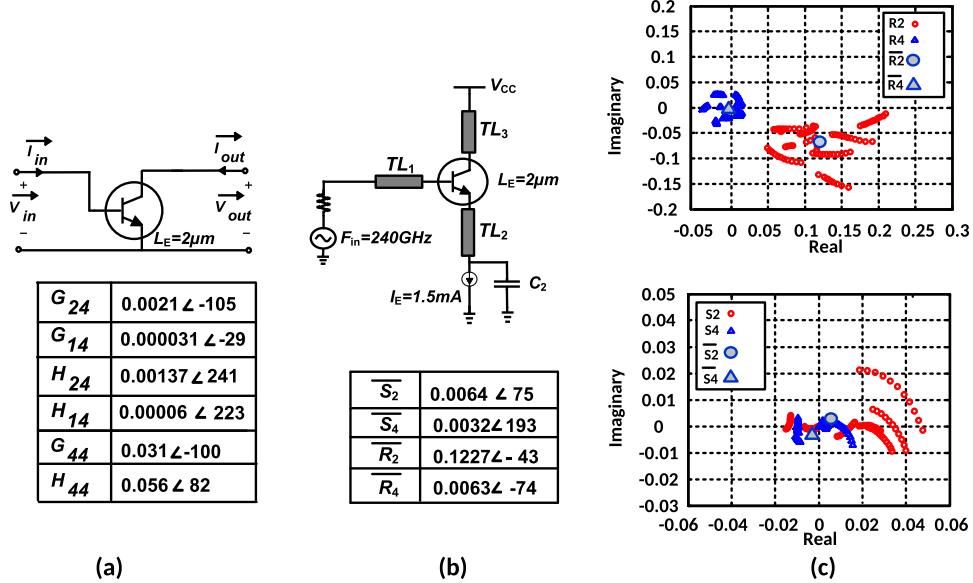


Fig. 5. (a) Selected transistor size and the corresponding  $G$  and  $H$  coefficients. (b) Topology of the frequency quadrupler. (c) Variations of the topology  $R_i$  and  $S_i$  functions by changing  $TL_1$ ,  $TL_2$ , and  $TL_3$ . The mean value of the functions and their relative location on the real–imaginary axis are also shown.

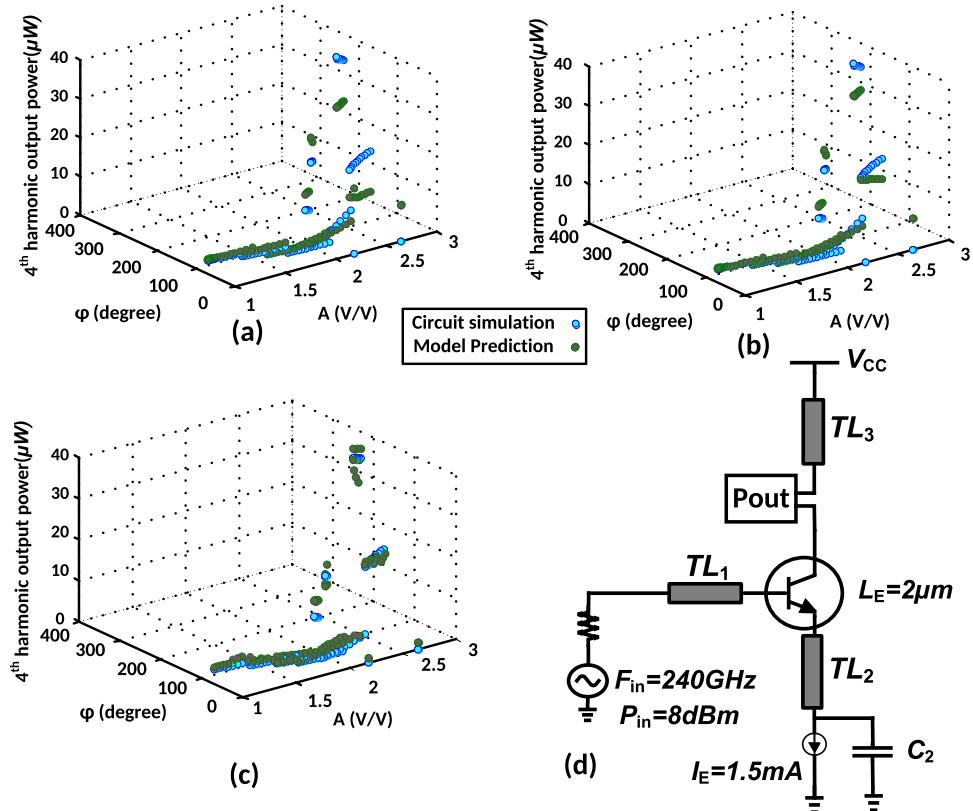


Fig. 6. (a) Harmonic power prediction using the approximate model (26) compared with the circuit simulations. (b) Harmonic power prediction using the moderate model (24) compared with the circuit simulations. (c) Harmonic power prediction using the accurate model (20) compared with circuit simulations. (d) Circuit schematic used in these simulations.

nonlinear component. Based on the proposed model, the optimum embedding network and the nonlinearity enhancement techniques are proposed, which yield to a high harmonic power.

Using a 130-nm SiGe:C BiCMOS process ( $f_T/f_{\max} = 220/280$  GHz and  $V_{ceo} = 1.6$  V [66]), a frequency quadrupler

radiator at 0.92–0.944 THz is designed. The circuit achieves a generated output power of  $-17.3$  dBm at .928 THz, which results in  $-10$  dBm of effective isotropic radiated power and stands among one of the highest frequency radiators in Si/SiGe processes. The nonlinear model of the active device is presented in Section II. The harmonic power optimization is

presented in Section III. Section IV covers the design of a high power frequency quadrupler. The measurement results and a comparison with the state-of-the-art methods are presented in Section V, and the paper is concluded in Section VI.

## II. NONLINEAR MODEL OF THE TWO-PORT DEVICE

An accurate model of transistor or any nonlinear component is essential to determine the mechanisms of harmonic signal generation. The proposed model should easily cope with arbitrary embedding networks and also encapsulate the variations of device behavior, e.g., the frequency dependence of the nonlinear profile. In this section, we propose a model based on the Volterra–Weiner theory [67], which meets the desired criteria.

### A. Review of Volterra–Weiner Theory of Nonlinear Devices

In 1958, Weiner rearranged the nonlinear series that Volterra had found in 1887 and that is why engineers mostly refer to the Volterra–Weiner theory [67]. These series capture different linear and nonlinear effects that contribute to output components. Both time-domain and frequency-domain representations of these series exist; however, we are interested in frequency-domain equations as we would like to capture the dynamics of harmonic variations. Utilizing the multidimensional Fourier transform, the frequency correspondence of each kernel [67]  $k_i$  is defined as

$$K_i(j\omega_1, \dots, j\omega_i) = \int_{\mathbb{R}} \dots \int_{\mathbb{R}} k_i(\tau_1 \dots \tau_i) e^{-j(\omega_1 \tau_1 + \dots + \omega_i \tau_i)} d\tau_1 \dots d\tau_i. \quad (1)$$

As an example, for  $i = 1$ , the Fourier transform of linear system  $K_1(j\omega)$  is obtained, that is

$$Y_1(j\omega) = K_1(j\omega)X(j\omega). \quad (2)$$

Similarly, for a  $P$ th-order operator, utilizing the  $P$ -dimensional Fourier transform

$$Y_P(j\omega_1 + \dots + j\omega_P) = K_P(j\omega_1, \dots, j\omega_P)X(j\omega_1) \dots X(j\omega_P). \quad (3)$$

Equation (3) is the general form of an intermodulation. As an example, for a 2nd-order input signal, containing  $\omega_0$  and  $2\omega_0$  components,  $K_2(j\omega_0, j2\omega_0)$  represents the fundamental and second harmonic intermodulations to generate the third harmonic component of the output. For identical  $\omega_i$ 's,  $K_P$  represents the  $P$ th-order nonlinear transfer of  $\omega_i$  at the input to  $P\omega_i$  at the output. For  $P = 1$ , (3) is a linear operator.

We are mostly interested in the response of the system to a periodic time domain signal

$$x(t) = \sum_{i \leq L} c_i \cdot \cos(i\omega_0 t) \quad (4)$$

which is a real periodic signal that contains the harmonics up to the  $L$ th order. For this input, the output time domain signal  $y(t)$  is the combination of linear, nonlinear,

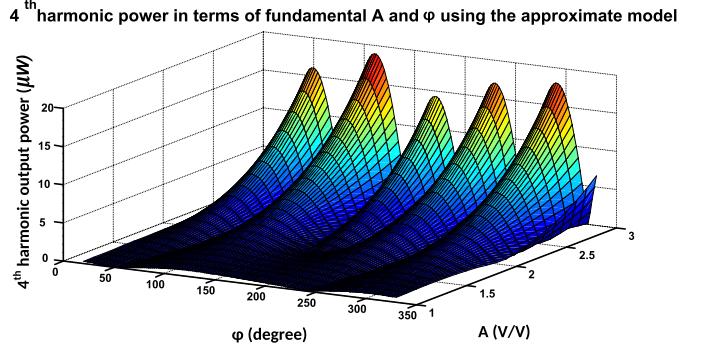


Fig. 7. According to the approximate model, we can find the location of optimum harmonic conditions in the  $[A, \Phi]$  plane. In order to maximize the harmonic power, the transmission lines are selected to reach these optimum conditions.

and intermodulation operators. For example, the response of a second-order system to the input  $A \cos(\omega_0 t)$  is

$$y(t) = 2 \left( \frac{A}{2} \right)^2 \operatorname{Re}\{K_2(j\omega_0, j\omega_0)e^{j2\omega_0 t}\} + A \operatorname{Re}\{K_1(j\omega_0)e^{j\omega_0 t}\} + 2 \left( \frac{A}{2} \right)^2 \operatorname{Re}\{K_2(j\omega_0, -j\omega_0)\} \quad (5)$$

where the first term represents the second-order operator from  $\omega_0$  to  $2\omega_0$ , the second term is the linear response of the system at  $\omega_0$ , and the last term is the intermodulation. Without showing the complex general expression for the case of multiharmonic input signal applied to a higher order nonlinear system [67], we will introduce a two-port nonlinear model in the next section.

### B. Nonlinear Two-Port Device Modeling

To propose a general nonlinear model, we should capture the important nonlinear mechanisms in different types of transistors, e.g., MOS and BJT. The standard simplified circuit models of these devices are shown in Fig. 1. According to these models, the three-port device can be modeled with two ports if the voltage variations at the third port (the emitter in BJT or source in MOS) are negligible.

The linear two-port model of transistors is shown in Fig. 2(a). Based on what Mason [68] introduced, the activity condition of this three-terminal (two-port) device is defined by an invariant function  $U$ . In this terminology, the three-terminal device is embedded in a four-port linear lossless reciprocal network, as shown in Fig. 2(c). Based on the method proposed in [57], the net power flowing out of the device determines the device activity. Moreover, optimum conditions to generate maximum power at the oscillation frequency are calculated in [57]. The elements of the admittance ( $Y$ ) matrix determine the values of these optimum conditions.

The linear two-port model fails to address the harmonic generation due to the device nonlinearity. Therefore, we would like to find a two-port model that can capture the major nonlinear mechanisms in the transistor. By selecting invariant dc conditions across the transistor, the variations in the device capacitors can be almost negligible [69]. However, for a fixed

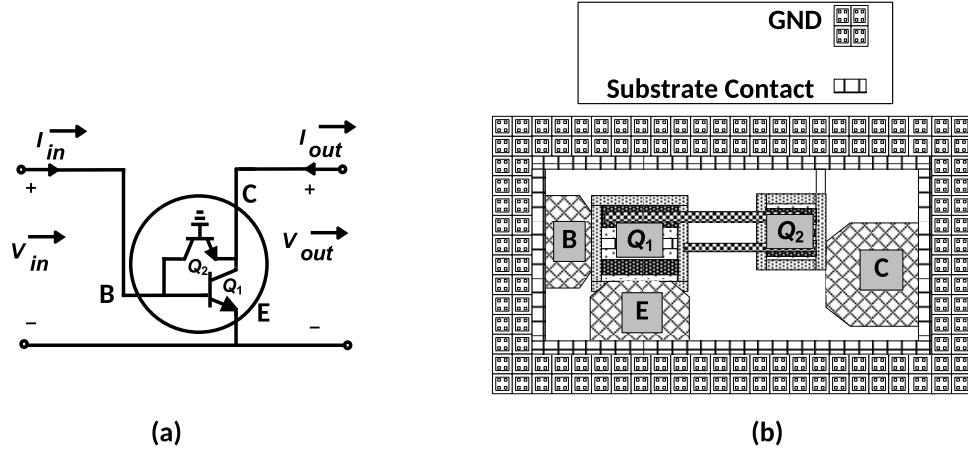


Fig. 8. (a) Nonlinearity manipulation by adding transistor  $Q_2$ . (b) Layout of the  $Q_1$  and  $Q_2$  transistor combination.

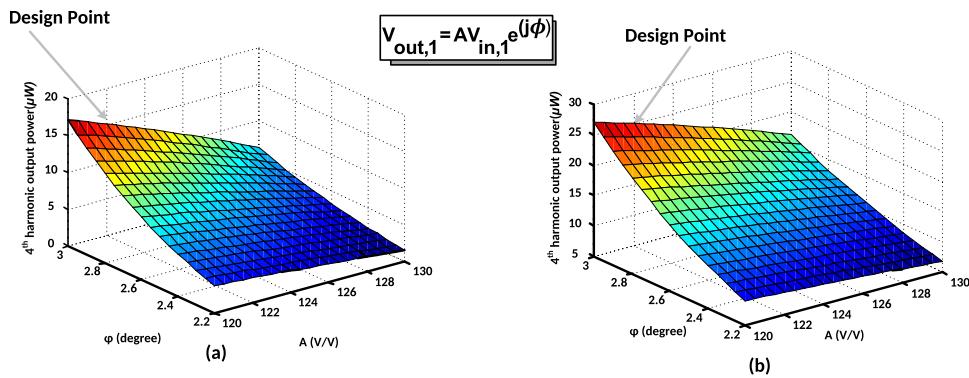


Fig. 9. Model prediction of the harmonic power in the vicinity of optimum point for the selected topology when (a)  $Q_1$  is the only nonlinear component and (b)  $Q_1$  and  $Q_2$  combination is the nonlinear component.

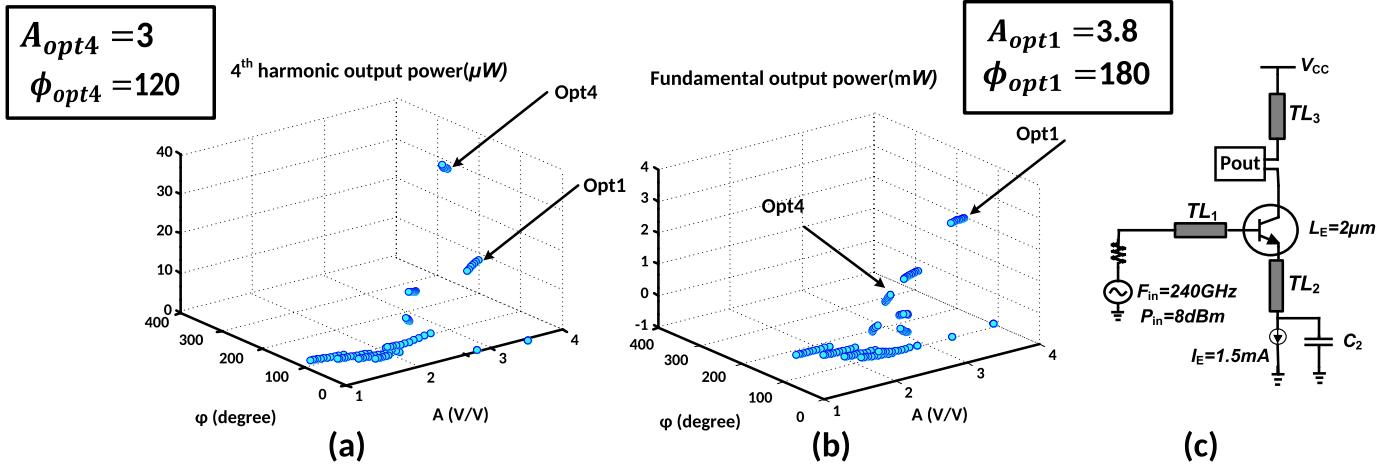


Fig. 10. Circuit simulations of the (a) fourth harmonic output power and (b) simulated fundamental power. It is clear that the optimum conditions of the fundamental and fourth harmonics, Opt1 and Opt4, are different. (c) Simulation test bench.

dc condition, the transistor still exhibits nonlinear performance due to the current distortion of the output channel. The output channel distortion is mainly due to the transconductance  $g_m$  and the output conductance  $g_o$ . For the two-port model in this paper, we would consider a nonlinear profile for any element of Y matrix, which contains  $g_m$  or  $g_o$ , and leave the rest simply

as linear parameters. The reader can verify that  $Y_{21}$  and  $Y_{22}$  of the active devices in Fig. 1 contain terms from  $g_m$  and  $g_o$ , while  $Y_{11}$  and  $Y_{12}$  do not.

Therefore, similar to the terminology of [68], in this paper, the transistor is modeled as a two-port network, as shown in Fig. 2(b). Consequently, the transistor can be embedded

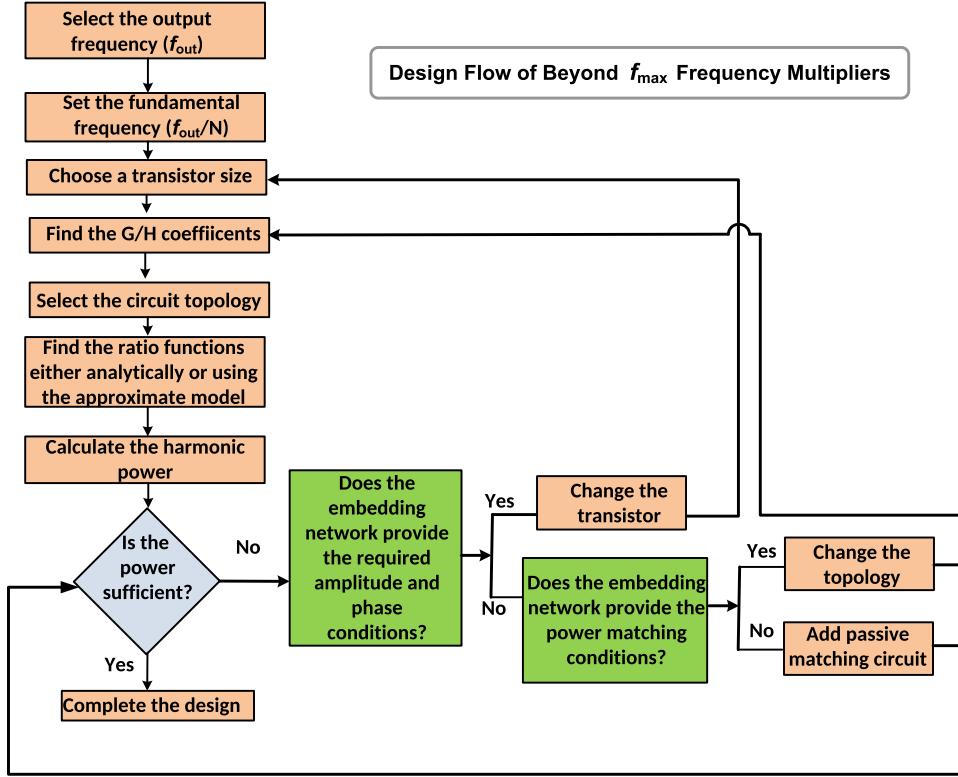


Fig. 11. Summary of the proposed design flow for THz-frequency multipliers.

in a linear reciprocal network as shown in Fig. 2(d). The multiharmonic arrays of voltage and current  $\vec{I}$  and  $\vec{V}$  are considered in this model to mention the fact that current and voltage components at any harmonic is dependent on components from other harmonics.

The current generation mechanisms in transistors dictate a nonlinear relationship between the output current  $\vec{I}_{\text{out}}$  and input/output voltages ( $\vec{V}_{\text{in}}$  and  $\vec{V}_{\text{out}}$ ). However, the input admittance ( $Y_{11}$ ) and the feedback admittance ( $Y_{12}$ ) of the transistor are still considered as linear functions. In the proposed model of Fig. 2(a), the  $G$  and  $H$  functions represent the different order transconductance functions of  $\vec{V}_{\text{in}}$  to  $\vec{I}_{\text{out}}$  and conductances of  $\vec{V}_{\text{out}}$  to  $\vec{I}_{\text{out}}$ , respectively. The coefficient  $G_{ij}$  is defined as the gain from the  $i$ th harmonic of the input voltage to the  $j$ th harmonic of the output current. Similarly,  $H_{ij}$  is defined as the gain from the  $i$ th harmonic of the output voltage to the  $j$ th harmonic of the output current. It is easily induced that for identical  $i$  and  $j$ , the operator is linear, and for different  $i$  and  $j$ , it is a nonlinear or intermodulation operator. If  $j$  is a multiple of  $i$ , the  $G_{ij}$  and  $H_{ij}$  coefficient represent a  $j/i$ -order nonlinear operator, that is

$$G_{ij}(i\omega_0, j\omega_0) = \frac{\Delta I_{\text{out},j\omega_0}}{\Delta V_{\text{in},i\omega_0}^{j/i}} \quad (6)$$

$$H_{ij}(i\omega_0, j\omega_0) = \frac{\Delta I_{\text{out},j\omega_0}}{\Delta V_{\text{out},i\omega_0}^{j/i}}. \quad (7)$$

It is noteworthy that each coefficient is calculated when the other voltage terms are held constant. We have to mention that the proposed model has a major difference with

broadband polyharmonic model [70]. The assumption of dominant fundamental signal in [70] is essential to use the harmonic superposition principle [71]. Therefore, the coefficients in [70] are dependent on the amplitude of the fundamental voltage. However, in the proposed model, the voltage variations are captured in the calculation scheme of coefficients; hence, the  $G$  and  $H$  coefficients are assumed amplitude independent. The values of nonlinear operators are calculated for a fundamental frequency of  $\omega_0$  and we simply denote them by  $G_{ij}$  and  $H_{ij}$  coefficients. In case  $j$  is not a multiple of  $i$ , the  $G$  and  $H$  are intermodulation operators. Based on (3), there are many intermodulations between any two harmonics. As an example,  $H_2(2\omega_0, \omega_0)$ ,  $H_3(2\omega_0, 3\omega_0, -2\omega_0)$ ,  $H_4(2\omega_0, 3\omega_0, -\omega_0, -\omega_0)$  all relate the second harmonic of the output voltage and the third harmonic of the output current in a transistor with fourth-order nonlinearity. However, as we simulated, the numerical values of the intermodulation components at higher frequencies are small; hence, we neglect the effect of intermodulation terms. In contrast, for low-frequency highly nonlinear circuits such as mixers, these coefficients should be considered for the analysis of mixing products. In [67], the calculation of these intermodulation coefficients is shown.

### C. Combination of Linear Passive Network and Nonlinear Device

As shown in [67], the interconnection of two nonlinear systems is the sum value of the corresponding kernels in time domain, which translates into summation of transfer functions in frequency domain. Based on (2), a linear system

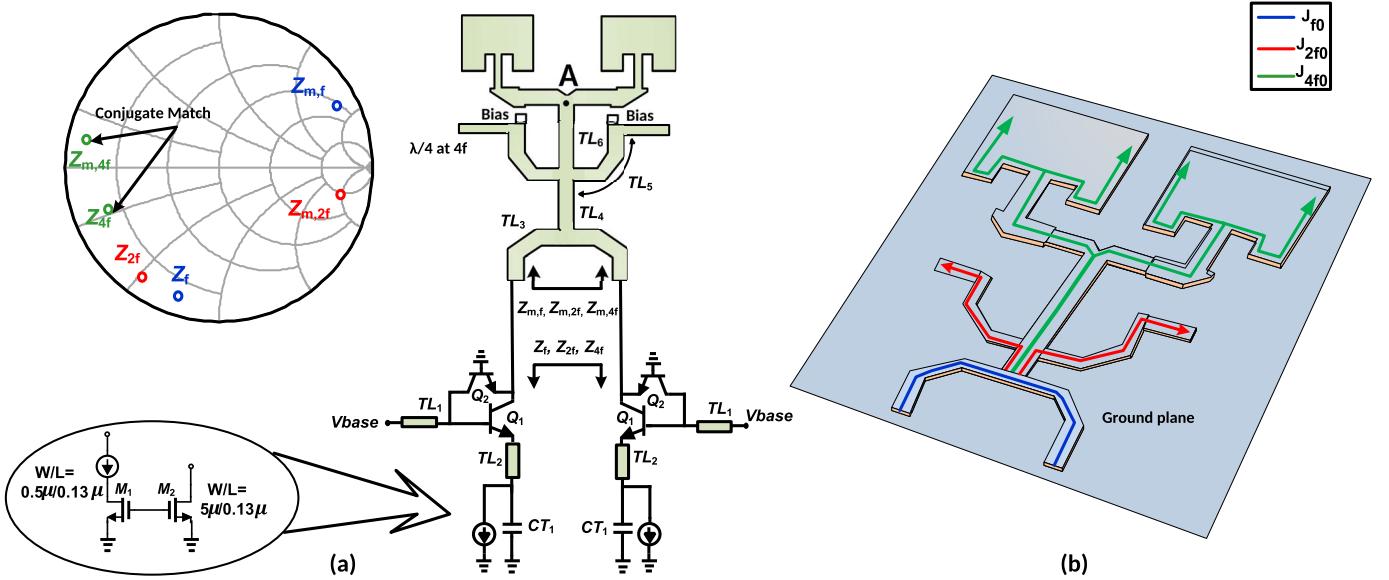


Fig. 12. (a) Frequency quadrupler schematic and the matching conditions at different harmonics. (b) Distribution of the current intensity of the harmonics.

can be considered as a first-order nonlinear system. Therefore, by placing the transistor in a linear embedding network, the linear operators of the device ( $Y_{11}$ ,  $Y_{12}$ ,  $G_{ii}$ , and  $H_{ii}$ ) are updated accordingly; however, the nonlinear coefficients remain unchanged. For example, by placing the transistor in the general embedding network of Fig. 2(b), the new linear operators of transistor, are updated accordingly, that is

$$Y_{11}^N(j\omega) = Y_{11}(j\omega) + Y_{11,M}(j\omega) + Y_1(j\omega) \quad (8)$$

$$G_{ii}^N(j\omega) = G_{ii}(j\omega) + Y_{21,M}(j\omega) \quad (9)$$

$$Y_{12}^N(j\omega) = Y_{12}(j\omega) + Y_{12,M}(j\omega) \quad (10)$$

$$H_{ii}^N(j\omega) = H_{ii}(j\omega) + Y_{22,M}(j\omega) + Y_3(j\omega). \quad (11)$$

In these equations,  $Y_{ij,M}$  are the elements of the  $Y$  matrix of  $Z_M$ , which are calculated to be

$$Y_M(j\omega) = \begin{bmatrix} \frac{1}{Z_M(j\omega)} & -\frac{1}{Z_M(j\omega)} \\ -\frac{1}{Z_M(j\omega)} & \frac{1}{Z_M(j\omega)} \end{bmatrix}. \quad (12)$$

Based on (8)–(11), the proposed nonlinear model is utilized inside any arbitrary circuit topology. Using this result, the nonlinear harmonic power optimization is performed in the next section.

### III. NONLINEAR HARMONIC POWER OPTIMIZATION

When the transistor operates at a fundamental frequency of  $\omega_0$ , the nonlinear operators generate components at different harmonics, i.e.,  $n\omega_0$ . For a more nonlinear device, the higher order operators appear and contribute to power generation at higher harmonic index. The frequency dependence of the  $G$  and  $H$  operators takes into account the variations of device characteristic by frequency. In order to evaluate the device performance at a certain harmonic, the real power flowing out of the device at the particular harmonic is defined as

$$P_{R,i} = \text{Re}\{V_{\text{in},i}^* I_{\text{in},i} + V_{\text{out},i}^* I_{\text{out},i}\}. \quad (13)$$

The expression in (13) consists of two power terms at the input and output ports of the device. This definition is more comprehensive for oscillators, where the total power determines the dc-to-RF efficiency. However, in circuits with input, such as frequency multipliers, the transistor is fed with RF power at  $\omega_0$  and the output power is extracted at a certain harmonic of the fundamental frequency. Therefore, we solely consider the real power at the output port

$$P_{R,\text{out},i} = \text{Re}\{V_{\text{out},i}^* I_{\text{out},i}\}. \quad (14)$$

Based on the harmonic index  $i$ , particular nonlinear operators that generate  $I_{\text{out},i}$  are considered. The general expression of (14) is written as

$$P_{R,\text{out},i} = \text{Re}\{V_{\text{out},i}^* [G(\vec{V}_{\text{in}}) + H(\vec{V}_{\text{out}})]\} \quad (15)$$

where  $G(\vec{V}_{\text{in}})$  and  $H(\vec{V}_{\text{out}})$  represent the contribution of input voltage array and output voltage array on  $I_{\text{out},i}$ , respectively. As an example, if the harmonic content up to the fourth order is considered in a nonlinear transistor, operating at the fundamental frequency of  $\omega_0$

$$\begin{aligned} I_{\text{out},4} = & G_{14}V_{\text{in},1}^4 + G_{24}V_{\text{in},2}^2 + G_{44}^NV_{\text{in},4} + H_{14}V_{\text{out},1}^4 \\ & + H_{24}V_{\text{out},2}^2 + H_{44}^NV_{\text{out},4} \end{aligned} \quad (16)$$

represents the major terms that generate the harmonic current  $I_{\text{out},4}$ . It is noteworthy that the third harmonic and higher harmonics impact the output current at the fourth harmonic, only through intermodulation terms. As mentioned before, based on the discussion on the relative value of these terms compared with that in (16), the intermodulation terms are neglected. The expression in (16) contains different voltage components and the power optimization is not trivial. Moreover, the  $N$  exponent on the linear Volterra coefficients exhibits the variation of these coefficients by the linear passive network. Therefore, we need to reduce the number of voltage components and simplify the harmonic current expression.

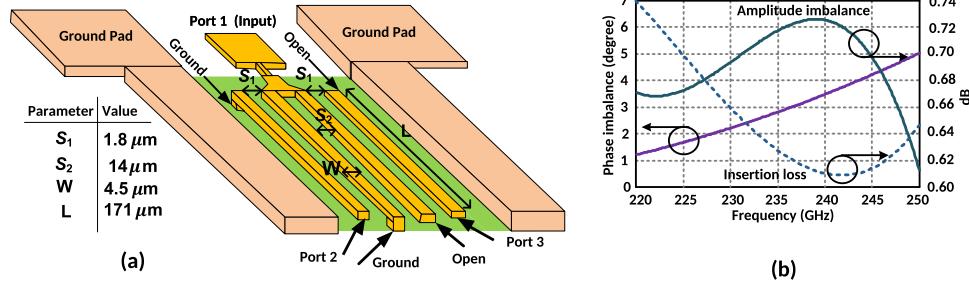


Fig. 13. (a) Layout of the input balun. (b) Performance summary of the microwave short–open structure.

Simultaneously, the impact of the selected circuit topology on the nonlinear device should be characterized.

#### A. Impact of Circuit Topology and the Ratio Functions

The number of independent parameters in (16) can be reduced by relating the harmonic components and fundamental components. However, the ratio of harmonic voltage components and the fundamental components are determined by the circuit topology. In other words, the structure of passive network, the initial dc conditions, and transistor size determine the ratio of the harmonic and the fundamental signals at the input and output ports of the device.

*1) Accurate Model:* For any fixed circuit topology (invariant passive network with variable values, constant bias conditions, and invariant transistor), the “ratio functions” are defined as

$$V_{\text{in},i} = R_i(V_{\text{in},1}) \quad (17)$$

$$V_{\text{out},i} = S_i(V_{\text{out},1}) \quad (18)$$

and for the fourth harmonic current

$$\begin{aligned} I_{\text{out},4} &= G_{14}V_{\text{in},1}^4 + G_{24}R_2^2(V_{\text{in},1}) + G_{44}^N R_4(V_{\text{in},1}) \\ &\quad + H_{14}V_{\text{out},1}^4 + H_{24}S_2^2(V_{\text{out},1}) + H_{44}^N S_4(V_{\text{out},1}) \end{aligned} \quad (19)$$

$$P_{R,\text{out},4} = \mathbf{Re}\{S_4^*(V_{\text{out},1}^*)I_{\text{out},4}\}. \quad (20)$$

By changing the values of passive components around the transistor in a fixed topology, the values of the ratio functions change. More importantly, as shown in Fig. 4, for a certain transistor, the ratio functions behave completely different when the topology is changed. This is why the topology invariance constraint is imposed in this paper to simplify the power optimization.

In the Appendix, an analytical study of ratio functions is shown for the circuit of Fig. 4(a). The amplitude and phase of each harmonic voltage component inside this simple circuit is dependent on many parameters, e.g., the width of transmission lines, the input source impedance, and the transistor linear/nonlinear operators. The trend and closed form expressions can become very complicated in circuits with more passive components. Therefore, we would like to find a simpler way to perform the power optimization. In the next two sections, we will introduce two simpler approximations, which can be used as an estimation to find the optimum conditions of harmonic power.

*2) Moderate Model:* As the values of the passive components change, the ratio values also change slightly for a fixed topology (Fig. 3). In addition, based on (8)–(11), the variation of passive components changes \$G\_{ii}\$ and \$H\_{ii}\$. We prefer an easier power optimization and substitute the ratio functions with a fixed value (e.g., ratio constant) for the selected topology. Without loss of generality, the mean value of the ratio values (\$\bar{R}\_i\$ and \$\bar{S}\_i\$) is selected to be the ratio constant, as shown in Fig. 5(c), that is

$$R_{i,m} = \bar{R}_i \quad (21)$$

$$S_{i,m} = \bar{S}_i \quad (22)$$

$$\begin{aligned} I'_{\text{out},4} &= G_{14}V_{\text{in},1}^4 + G_{24}R_{2,m}^2 V_{\text{in},1}^2 + G_{44}^N R_{4,m} V_{\text{in},1} \\ &\quad + H_{14}V_{\text{out},1}^4 + H_{24}S_{2,m}^2 V_{\text{out},1}^2 + H_{44}^N S_{4,m} V_{\text{out},1} \end{aligned} \quad (23)$$

$$P_{R,\text{out},4} \simeq \mathbf{Re}\{S_{4,m}^* V_{\text{out},1}^* I'_{\text{out},4}\}. \quad (24)$$

*3) Approximate Model:* Taking into account the variations of the linear coefficients with the passive components in (20) and (24) adds to the complexity of the power expression. To achieve a faster power estimation, we sacrifice the accuracy by neglecting this effect. As shown later, this approximate version still guides us through the maximum power location. Therefore, we neglect the impact of passive component variations on the linear coefficients, that is

$$\begin{aligned} I''_{\text{out},4} &= G_{14}V_{\text{in},1}^4 + G_{24}R_{2,m}^2 V_{\text{in},1}^2 + G_{44}R_{4,m} V_{\text{in},1} \\ &\quad + H_{14}V_{\text{out},1}^4 + H_{24}S_{2,m}^2 V_{\text{out},1}^2 + H_{44}S_{4,m} V_{\text{out},1} \end{aligned} \quad (25)$$

$$P_{R,\text{out},4} \simeq \mathbf{Re}\{S_{4,m}^* V_{\text{out},1}^* I''_{\text{out},4}\}. \quad (26)$$

The final simplified harmonic power expression is obtained by substituting \$V\_{\text{out},1} = A\_1 V\_{\text{in},1}\$, where \$A\_1 = Ae^{j\phi}\$ is a complex gain. This enables us to find the optimum conditions of harmonic power generation in terms of \$A\$ and \$\phi\$. Therefore, the harmonic power is related to the circuit topology (ratio constants), the transistor nonlinearity (\$G\_{ij}\$ and \$H\_{ij}\$ coefficients), and the fundamental frequency gain \$A\_1\$. Moreover, the dependency on the amplitude of \$V\_{\text{in},1}\$ captures the harmonic power variations by changing the input power at the fundamental frequency.

#### IV. DESIGN OF A HIGH POWER FREQUENCY QUADRUPLER

Based on the developed model in the previous section, we design a high power THz frequency quadrupler.

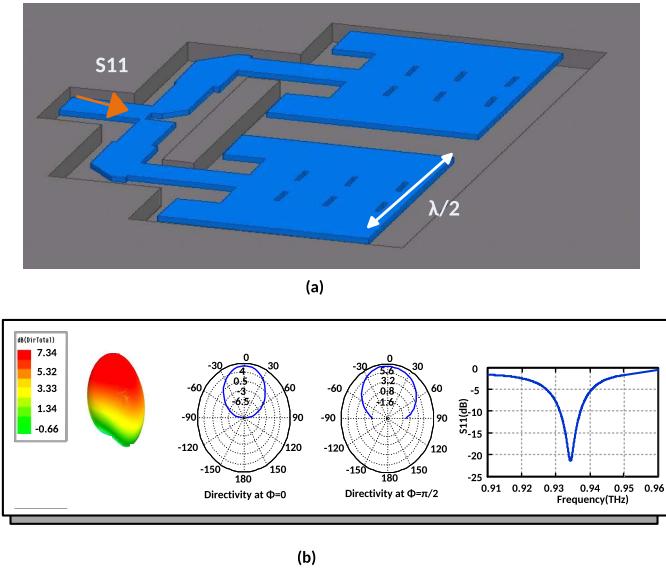


Fig. 14. (a) Layout structure of the patch antenna array. (b) Simulated performance summary of the radiator.

The utilized technology (BiCMOS 130-nm SiGe:C) has a  $f_{\max}$  of 280 GHz [66]; hence, the input frequency is selected below  $f_{\max}$  to sustain the high swing of fundamental frequency. For a target output frequency of 0.92–0.96 THz, by extraction of the fourth harmonic, an input frequency of 230–240 GHz is selected.

#### A. Transistor Selection

In selection of the transistor, the major consideration is regarding the parasitics and current drive. For THz operation, the transistor size is selected to be small in order to shrink the parasitic resistance and capacitance. On the other hand, the smallest possible width for MOS or emitter length for BJT does not provide sufficient transconductance to generate high output power. This is the main reason that a bipolar transistor ( $Q_1$ ) with an emitter length of  $2\mu\text{m}$  is selected as shown in Fig. 5(a). The Volterra coefficients of the selected transistor are also listed in Fig. 5(a).

#### B. Circuit Topology and Optimum Embedding Network

Among different circuit configurations for a bipolar transistor, the common-emitter (CE) topology of Fig. 5(b) is selected. Due to the extraction of the output current from the collector node, the CE topology conserves the nonlinear profile of the device and generates high power harmonics. The second reason is about the matching feasibility and the power extraction. The base transmission line  $TL_1$  and the junction capacitor of  $Q_1$  are used for the input power matching. On the other hand, adding the  $TL_1$  transmission line at the base determines the value of ratio constants (i.e.,  $R$  and  $S$ ) at the input. By adding the  $TL_2$  at the emitter, the values of  $R_i$  and  $S_i$  constants are changed again. Consequently, the addition of  $TL_2$  transmission line transforms the impedance seen by the current source and the bypass capacitor ( $C_2$ ) to a smaller value. For the selected transistor and topology, by changing the characteristic of  $TL_1$ ,  $TL_2$ , and  $TL_3$ , the

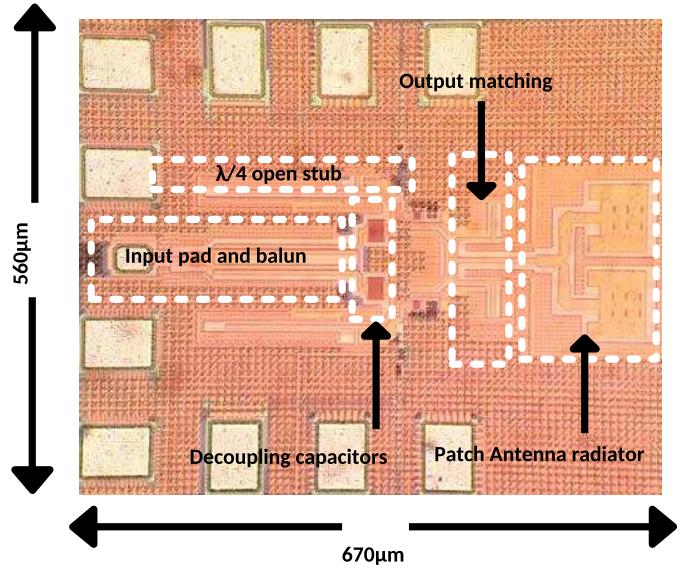


Fig. 15. Die photograph.

ratio functions and corresponding mean values (ratio constants) are shown in Fig. 5(b) and (c). The power expressions in (20), (24), and (26) are used to predict the harmonic power for the circuit topology of Fig. 5. As the results in Fig. 6 illustrate, all the three different models exhibit a close match to the circuit simulations. This is the main reason that the simplified expression in (26) is used in Fig. 7 to find the location of maximum fourth harmonic power. In order to reach these optimum conditions, transmission lines can be selected similar to [57].

#### C. Device Characteristic Manipulation

Besides the passive component effects, the nonlinear device can be manipulated to further increase the harmonic power. As shown in Fig. 2(b), by adding a parallel component with the transistor, the linear operators, i.e.,  $G_{ii}$  and  $H_{ii}$ , are manipulated. This is particularly important for operation at higher harmonics where multiple harmonics are involved in the power generation and more adjustments are required before reaching the optimum power. Based on the value of the  $G$  and  $H$  functions and the  $S$  and  $R$  coefficients of the selected topology in Fig. 4, to achieve a higher fourth harmonic power: 1) the magnitude of  $G_{44}$  should be increased and 2) the value of  $S_2$  and  $R_2$  at the output and input ports of device should be preserved. The first condition is satisfied by adding a passive component that exhibits a low impedance (high admittance) at the fourth harmonic frequency. However, the selected component has to provide a high impedance (ideally zero admittance) at the fundamental and second harmonic frequencies in order to preserve the  $R_2$  and  $S_2$  constants. Therefore, we have to add a small capacitor in parallel with the transistor. Since it is not straightforward to design small capacitors at the THz-frequency range, a bipolar transistor in the cut-off region is utilized instead. The selected  $0.6\text{-}\mu\text{m}$  transistor exhibits a high impedance at the lower harmonics and low impedance at the fourth harmonic. In order to minimize the parasitics of the combination of the two transistors, the substrate contact of the

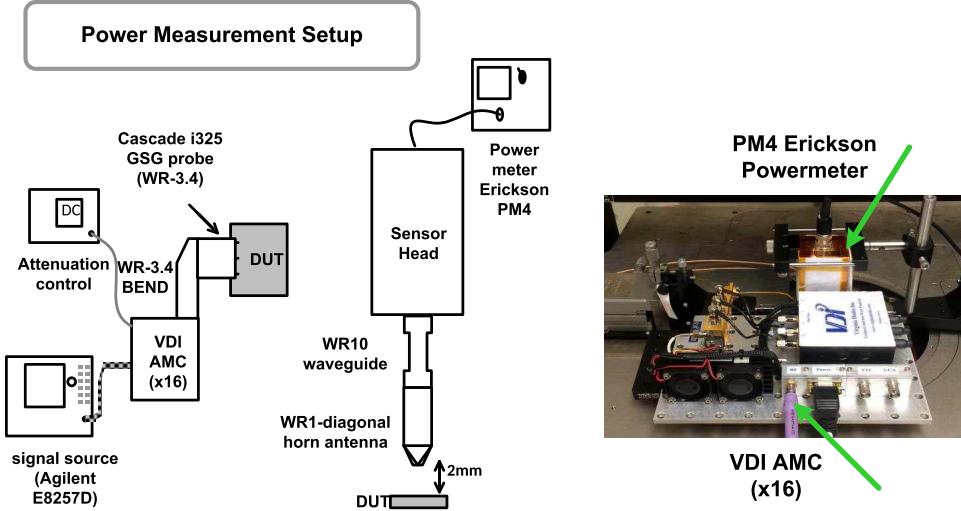


Fig. 16. Implemented power measurement setup.

confined transistors is redrawn inside a compact structure as shown in Fig. 8. As shown in Fig. 9, by the combination of  $Q_1$  and  $Q_2$ , the predicted harmonic power at the design point increases by 2.2 dB, compared with the case that  $Q_2$  is not added. In the circuit simulations, a 2-dB power increment is achieved.

In order to design close to the optimum point, it is noted that no extra passive components are allowed, as the circuit topology changes and the ratio constants have to be updated. However, as it is verified by the circuit simulations in Fig. 5, there exists a combination of  $TL_1$ ,  $TL_2$ , and  $TL_3$ , which operates close to the optimum point of Fig. 7. This point is indicated as Opt4 in Fig. 10. On the other hand, due to the nonlinear profile of transistors, the harmonic power is not maximized by providing the optimum fundamental conditions. This phenomenon is illustrated in Fig. 10, where the fundamental and fourth harmonic output powers reach a maximum at different points. This means that utilizing a linear assumption fails to guide us toward the optimum point for the harmonic power. And finally, it is noteworthy that based on the proposed theory, the maximum harmonic power is found for a particular topology. This is the main difference of this model with previous linear model techniques. The proposed systematic design flow of THz frequency multipliers is shown in Fig. 11.

#### D. Matching Conditions

The output embedding at the collector side is selected such that a large fundamental voltage swing is achieved for the selected transistor size. It should also provide the matching conditions for the output signal and block the current flow of unwanted harmonic components to the output. For this particular frequency quadrupler, the output network is expected to provide the conjugate matching condition for the fourth harmonic signal. In addition, the harmonic components that are crucial for the power generation at the output frequency are kept confined at the transistor.

As illustrated in Fig. 12, by differential operation, the powerful fundamental current does not flow toward the common

node and remains inside the transistor. However, the second harmonic currents of the two transistors in a differential circuit are in phase and can potentially flow toward the output antenna feed point (node A). To block the flow of second harmonic, a matching network is utilized in the circuit that provides high impedance to the second harmonic current and blocks it before reaching the output node. This condition is provided by adding the stub transmission lines ( $TL_5$ ). On the other hand, the impedance of the stub is seen high at the fourth harmonic and the corresponding current component has to flow through  $TL_6$  and reach node A.

#### E. Single to Differential Power Conversion

Based on the mentioned advantage of differential operation, the input power coming from the external source is converted into differential form, using a balun [74]. There are mainly three considerations on the selected structure of this balun: 1) it has to be wideband; 2) it should exhibit a low conversion loss; and 3) the selected architecture should embed in the layout pattern imposed by the rest of the circuit. Therefore, a microwave passive short-open balun [75] is designed as shown in Fig. 13. The selected balun has a low conversion loss (<0.8 dB) and preserves the phase/amplitude match at the input.

#### F. Output Power Extraction

The generated harmonic power of the frequency multiplier has to be extracted using an efficient scheme. In practice, there are two major techniques for THz-wave measurement: 1) design of low-capacitance pads and probing the output signal and 2) radiation of the THz wave with an on-chip antenna. The probe solution faces challenges in terms of designing low-loss pads (due to the substrate capacitance) and the sensitive performance of the probe. However, by probing, a wideband measurement is feasible due to the broad transmission  $S_{21}$  profile of the THz probes.

The alternative to the probing solution is the wave radiation. By approaching THz frequencies, the substrate thickness and wavelength become comparable and energy is lost in substrate

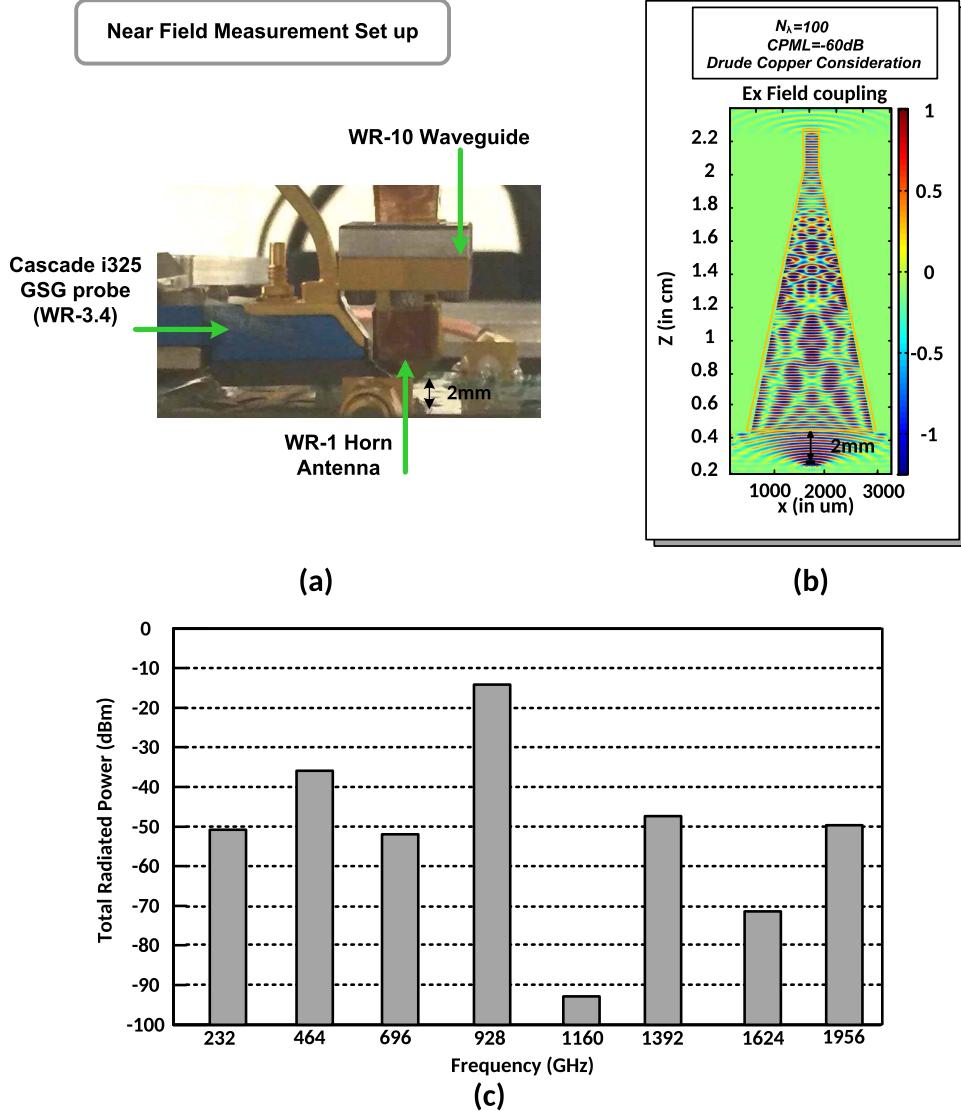


Fig. 17. (a) Implemented near-field power measurement. (b) Diagonal horn antenna near field coupling ( $d = 2$  mm), simulated by an accurate FDTD solver. (c) Simulated total radiated power at different harmonics for an input at 232 GHz.

modes. Extra wafer thinning and matched silicon lens are utilized to cancel the unexpected substrate loss [39], [59], [58]. However, in this design, to avoid this issue, a two-element patch antenna array with broadside radiation from the top of the chip is utilized as shown in Fig. 14. Due to the limited distance between the top metal layer and ground shield layer ( $<5 \mu\text{m}$ ), the antenna bandwidth is limited. The simulated performance of the antenna is shown in Fig. 14 and 72% radiation efficiency at 960 GHz and 7.3 dBi of directivity are achieved. Since the characteristic impedance of patch antenna is high ( $100\sim200 \Omega$ ), an array of two antennas is designed for a better matching.

## V. MEASUREMENT RESULTS

The chip prototype is fabricated in a  $0.13\text{-}\mu\text{m}$  SiGe:C BiCMOS technology from STMicroelectronics. The circuit contains the microwave balun, the input matching network, the frequency quadrupler, and the patch antenna array. The chip occupies a small area ( $0.37 \text{ mm}^2$ ) as shown in Fig. 15 and draws 3 mA of current from a 1.9 V supply. The measurement

setup is shown in Fig. 16. A conventional measurement of THz radiators is by placing the receiver antenna at far-field distance and approximating the transmitted power using the Friis equation. In addition, the design of diagonal horn antennas is optimized for the coupling of plane waves [76]. However, the drawback of the far-field measurement is the propagation loss, which lowers the received power level significantly below the transmitted power ( $\propto 1/d^2$ ). For this chip, a near-field power measurement is performed due to the limited power and insufficient sensitivity of the power meter. As shown in Fig. 17(a), the WR-1 horn antenna at a spacing of 2 mm on top of the radiator collects the radiation. Based on FDTD simulations with a precise EM solver, a power coupling efficiency of 9.8% is achieved (10 dB of power loss) for the fourth harmonic radiation from the chip to the input of the WR-10 waveguide in the near-field measurement scheme. In addition, the WR-10 waveguide after the horn antenna adds a propagation loss of 1 dB, measured using a vector network analyzer. Combined with the horn antenna coupling

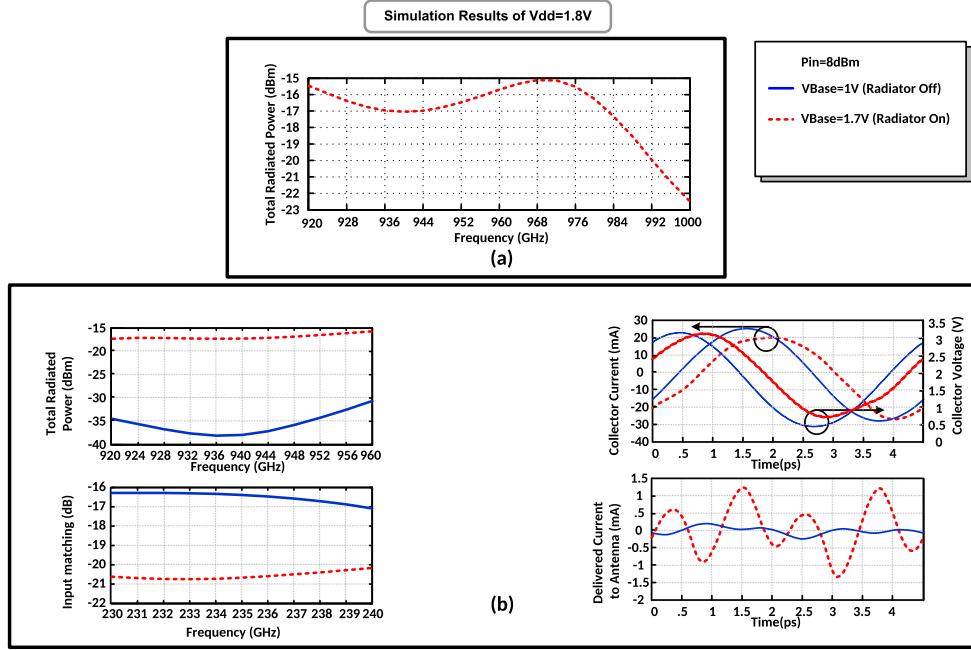


Fig. 18. (a) Simulation results of the wideband power generation and (b) circuit simulated operation in “radiator ON” and “radiator OFF” modes.

loss, a total power loss of 11 dB is considered. The rectangular waveguide of the horn antenna enforces an exponential decay of lower harmonics radiation. On the other hand, the WR-10 waveguide passes the smaller wavelengths and in particular the THz wave. Moreover, as illustrated in Fig. 17(c), the simulated total radiated power of the fourth harmonic is significantly higher than the other harmonics. This further guarantees that the unwanted radiations are not coupled to the power meter.

One of the important considerations in measurement of THz waves is the characterization of the blackbody radiation. Therefore, to perform an accurate power measurement, the THz radiated power and the thermal emission should be distinguished. The blackbody emission is particularly important when the silicon die is large and consumes a high dc power. In this measurement, we rely on an operational feature of the chip, which helps the calibration of the blackbody power. In principle, the quadrupler operation is divided into two different modes: “radiator ON” and “radiator OFF,” as shown in Fig. 18. Except the base voltage of  $Q_1$  ( $V_{\text{Base}}$  in Fig. 12), all the voltages are kept constant in the two cases. By changing the base voltage, the junction capacitors of  $Q_1$  and the  $G$  and  $H$  coefficient are changed accordingly. However, due to the constant bias of the tail current source and the constant value of  $V_{\text{dd}}$ , the dc power consumption of the circuit does not change. On the other hand, the variation of the  $G$  and  $H$  coefficients changes the radiated power at the fourth harmonic by around 15 dB [Fig. 18(b)]. Based on this phenomenon, by measuring the coupled power in the “radiator off” mode, the coupled power to the power meter is effectively the thermal radiation. In the “radiation on” mode, the coupled power to the power meter corresponds to the summation of the direct THz coupled power and the same blackbody emission. It is clear that the power difference of the two cases is not related to thermal variations as the power consumption

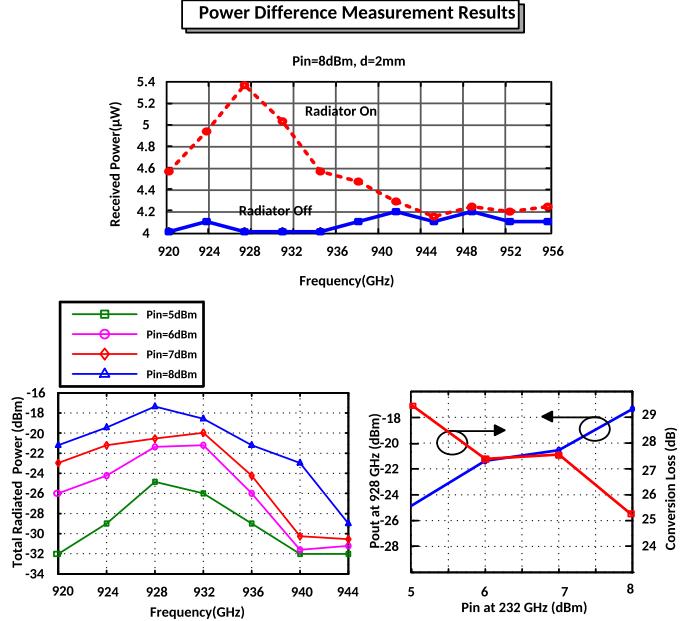


Fig. 19. Measurement results. The power difference technique is utilized to measure all data points.

is the same. As it is seen in the measurement results of Fig. 19, the coupled power exhibits a jump within the lower frequency band of measurement when the radiator is turned ON and remains unchanged out of this band. This validates that the temperature variation is not the cause of these changes. Moreover, based on the bandwidth of the designed antenna, we expect to observe the THz power radiation in a limited bandwidth, which is also the case in our measurement. The simulated antenna with HFSS has a slightly higher bandwidth, which is due to the solution of the antenna based on the surface current components.

TABLE I  
COMPARISON WITH STATE-OF-THE-ART METHODS

Reference	Technology	Source type	Output Freq (GHz)	Generated Power (dBm)	Conversion Loss (dB)	Pdc (mW)	EIRP (dBm)	Remarks
This work	130 nm SiGe	Quadrupler	920-944/ 920-1000*	-17.3	25.3	5.7	-10 **	Radiator/ no lens
JSSC 2011 [11]	250 nm InP HBT	Oscillator	573	-19.2	15.35	115	NA	NA
MTT 2010 [12]	Planar GaAs Schottky diode	Multiplier	840-900	1.4	15.35	NA	NA	NA
ISSCC 2011 [38]	250 nm SiGe	Multiplier	820-845	-17	NA	3700	NA	Radiator/no lens
MTT 2013 [48]	45 nm CMOS	Quadrupler	390-440	-10	19.5	700	3	Radiator/ Quartz sub.
ISSCC 2015[55]	130 nm SiGe	Oscillator	320	5.18	NA	610	22.5	Radiator/ with lens
JSSC 2011[56]	90 nm BiCMOS	Oscillator	480-510	-16.6	NA	400	NA	Probed
JSSC 2011[57]	65 nm CMOS	Oscillator	482	-7.9	NA	61	NA	Probed
ISSCC 2012[58]	45 nm CMOS	Oscillator/doubler	270-280	-7.2	NA	810	9.4	Radiator/ no lens
VLSI 2015[72]	65 nm CMOS	Quintupler	650-730	-21.3	33.8	0	-22	Radiator/ no lens
ISSCC 2016[73]	65 nm CMOS	Multiplier	1290-1440	-22.7	40	0	-13	Radiator/ no lens

\* put frequency range. The second frequency range is based on simulation.

\*\* Based on simulated far-field antenna directivity

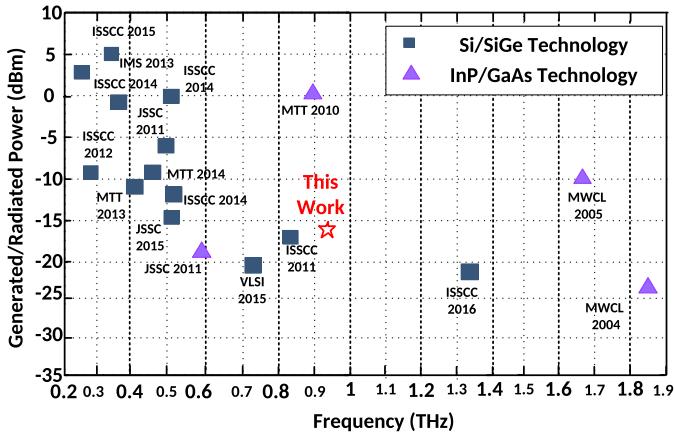


Fig. 20. Performance summary of state-of-the-art THz sources.

Taking into account the power coupling loss, the radiated power at different frequencies is calculated. As shown in Fig. 19, the circuit radiates a peak power of  $-17.3$  dBm at  $0.928$  THz and the antenna bandwidth will block the radiations above  $0.944$  THz. As we are exciting the input power from an external source by a probe waveguide and the power meter sensitivity is insufficient, the  $E/H$  plane radiation pattern measurement is not possible for this radiator. Therefore, based on the simulated antenna directivity ( $7.3$  dBi),

the circuit exhibits a peak equivalent isotropic radiated power of  $-10$  dBm at  $0.928$  THz.

The output power radiation of this source is from  $0.92$  to  $0.944$  THz due to the limited bandwidth of the antenna. However, the quadrupler is in principle very wideband and exhibits only  $8$  dB of power variation within an  $80$ -GHz bandwidth ( $920$ – $1000$  GHz) as the simulation results in Fig. 18 verify. According to Fig. 20, the design methodology introduced here can boost the generated power and the operation frequency of electronic circuits. To the best of our knowledge, this circuit demonstrates one of the highest frequency radiators among all Si/SiGe sources. Table I compares the performance of this THz power radiator with state-of-the-art Si/SiGe sources.

## VI. CONCLUSION

In order to generate power at the higher end of THz-frequency range, there are fundamental limits imposed by the existing technology. In order to extract the full potential of devices, an accurate model of power generation at the harmonics of the operation frequency ( $f_0 < f_{\max}$ ) is required. In this paper, we propose a novel nonlinear model of harmonic power generation in electronic circuits that can be used in THz circuits. Based on the introduced model, a  $0.92$ – $0.944$  THz-frequency quadrupler is designed, which demonstrates a radiated power level that is beyond the reach of

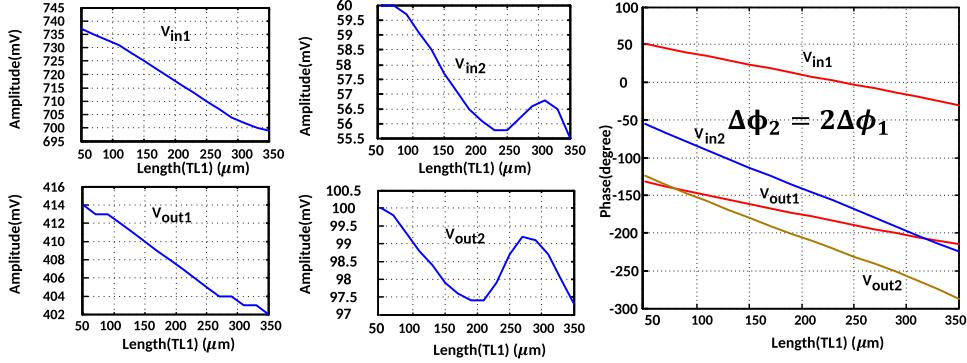


Fig. 21. Simulated variation of amplitude and phase of the input and output voltage components by variations of length of  $TL_1$ .

conventional circuits. The proposed design methodology paves the path toward higher power generation as well as reaching higher operational frequencies.

#### APPENDIX ANALYTICAL STUDY OF RATIO FUNCTIONS

In this section, we show how the variations of device embedding in the simple circuit of Fig. 4(a) can impact the ratio functions. Based on the results of these analyses, the reader may conclude that the analytic derivation of ratio functions in some circuits might not be straightforward and simpler approaches similar to those in Section II can be used. For simplicity, we consider the case of lossless transmission lines since they can be designed to exhibit a high quality factor.

We assume an input power source with a delivered power of  $P_0$  and a corresponding voltage of  $V_S$  across a source impedance of  $Z_{0S}$ . There are two possibilities for the base transmission line,  $TL_1$ .

##### A. No Reflection From Source

This case happens when the input line impedance is identical with the source internal impedance, that is

$$Z_{0L1} = Z_{0S} \quad (27)$$

which leads to  $\Gamma_s = 0$ . The amplitude of fundamental voltage at the base of transistor ( $V_{in1}$ ) is expressed in terms of load reflection coefficient, that is

$$V_{in1} = V_{inL1} = V_0^+ (1 + \Gamma_L) \quad (28)$$

where

$$\Gamma_L = \frac{Z_{inL1} - Z_{0L1}}{Z_{inL1} + Z_{0L1}} \quad (29)$$

$$V_0^+ = V_S \frac{Z_{inS}}{Z_{inS} + Z_{0S}}. \quad (30)$$

This voltage will generate output fundamental voltages of  $V_{out1}$  and  $V_{out2}$  where

$$V_{out1} \approx jZ_{0L2} V_{in1} G_{11} \tan(\beta_1 L_2) \quad (31)$$

$$V_{out2} \approx jZ_{0L2} (V_{in1}^2 G_{12} + H_{12} V_{out1}^2) \tan(\beta_2 L_2). \quad (32)$$

It is noteworthy that  $\beta_1$  and  $\beta_2$  are the propagation constants at the first and second harmonics, respectively. The output harmonic voltage will generate an input current at  $2f_0$  by the linear feedback admittance, that is

$$V_{in2} = Z_{inL1@2f_0} Y_{12@2f_0} V_{out2}. \quad (33)$$

According to (28)–(32), the ratio functions can be found in terms of the device properties and the embedding network parameters. By changing the length of  $TL_1$ , the phase of  $V_{in1}$  changes according to (30). This phase variation is linear up to the first order and is equal to  $\beta_1 \Delta L_1$ , which results in the same phase variation at  $V_{out1}$ . However, the second harmonic voltages are determined by second powers of  $V_{in1}$  and  $V_{out1}$ ; hence, their phases change by  $2\beta_1 \Delta L_1$ . Similarly, for any higher harmonic  $n$ , the phase of harmonic voltages change by  $n\beta_1 \Delta L_1$ . In addition, for a limited range of variations on the length of transmission lines, the amplitude of (30) does not change significantly and the amplitude of voltages can be approximated as constants. Therefore, by changing the length of  $TL_1$ , the amplitudes of second harmonic ratio functions  $R_2$  and  $S_2$  are almost preserved; however, their phases change by  $\beta_1 \Delta L_1$ . Fig. 21 (b) illustrates the simulated amplitude and phase of input and output voltages that match with the theory.

On the output side, by changing the length or  $Z_0$  of  $TL_2$ , the output voltages  $V_{out1}$  and  $V_{out2}$  change according to (31) and (32). In addition, the second harmonic voltage at the input  $V_{in2}$  changes according to (33). Finally, the fundamental voltage at the input  $V_{in1}$  changes according to (29), where the input impedance is impacted by the variations of the load impedance, that is

$$Z_{inL1} \simeq \frac{1}{Y_{11}} \parallel \left\{ \frac{-G_{11}}{Y_{11}H_{11} - Y_{12}G_{11}} + Z_L \parallel \frac{1}{H_{11}} \right\} \quad (34)$$

where the  $Y$  parameters of the transistor and the load impedance of  $Z_L = jZ_{0L2} \tan(\beta_1 L_2)$  appear. Since the trigonometric functions operate differently at  $f_0$  and  $2f_0$  in (31) and (32), the amplitude and phase of output ratio functions change this time. Similarly, according to (31) and (32), the amplitude and phase of ratio functions at the input port also change. Fig. 22 illustrates the amplitude and phase variations of fundamental and harmonic voltages as well as the ratio functions.

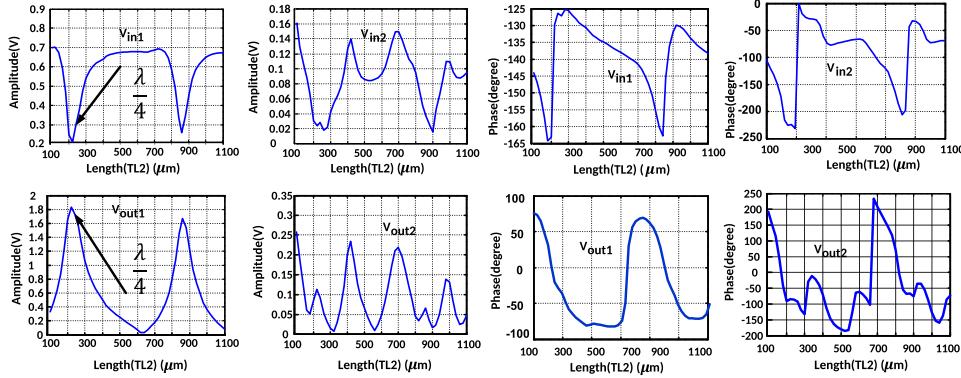


Fig. 22. Simulated variation of amplitude and phase of the input and output voltage components by variations of length of  $TL_2$ .

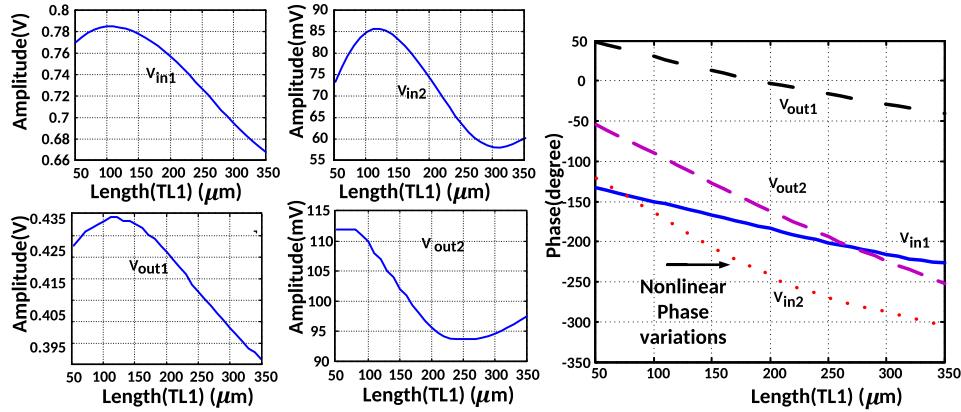


Fig. 23. Simulated variation of amplitude and phase of input and output voltage components by variations of length of  $TL_1$  when there is source reflection.

### B. Reflection From the Source

This condition happens when the internal impedance of the source  $Z_{0s}$  and the characteristic impedance of the base transmission line  $TL_1$  are different. This condition is undesired if the source reflection leads to a poor power delivery at the fundamental frequency. However, we would analytically consider the slight variations from the identical  $Z_{0s}$ . More importantly, the relative phase and amplitude of fundamental and harmonic voltages can change differently in this case, which could lead to a higher harmonic power.

As it is shown in [74], for this case,  $V_0^+$  is impacted by  $\Gamma_S = ((Z_{0s} - Z_{0L1})/(Z_{0s} + Z_{0L1}))$ , that is

$$V_0^+ = V_s \frac{Z_{0L1}}{Z_{0s} + Z_{0L1}} \frac{e^{-j\beta_1 l}}{1 - \Gamma_L \Gamma_S e^{-2j\beta_1 l}}. \quad (35)$$

By the combination of (28) and (35), the fundamental input voltage is determined. In this case, the length variation of  $TL_1$  impacts the amplitude and phase of the fundamental voltage  $V_{in1}$  significantly. By applying (31)–(33), the amplitude and phase variations of other voltage components are also determined. The results in Fig. 23 illustrate the simulated ratio functions for this case.

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