A 16 b Multi-Step Incremental Analog-to-Digital Converter With Single-Opamp Multi-Slope Extended Counting

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***Abstract*— This paper presents a multi-step incremental analog-to-digital converter (IADC) using multi-slope extended counting. Only one active integrator is used in the three-step conversion cycle. The accuracy of the IADC is extended by having it configured asmulti-slope ADCs in two additional steps. The proposed IADC uses the same circuitry as a first-order IADC (IADC1), but it exhibits better performance than a second-order IADC. For the same accuracy, the conversion cycle is shortened by a large factor (by more than 2^9 for the implemented device) compared with that of a conventional single-step IADC1. Fabricated in 0.18 μm CMOS process, the prototype ADC occupies 0.5 mm^2. With a 642 kHz clock, it achieves an SNDR of 52.2 dB in the first step. The SNDR is boosted to 79.8 dB in the second step and to 96.8 dB in the third step, over a 1 kHz signal band. The power consumption is 35 μW from a 1.5 V power supply. This gives an excellent Schreier figure of merit of 174.6 dB.**

***Index Terms*— $\Delta\Sigma$ analog-to-digital converter (ADC), chopper stabilization, extended counting, incremental ADC (IADC), instrumentation and measurement, multi-slope ADCs, multi-step operation, sensor interface circuits.**

I. Introduction

SENSORS have been used in many applications, such as instrumentation and measurements, biosensors, MEMS, and image sensors. Integrated sensor interface circuits process and digitize the analog sensor output for digital signal processing. In some applications, such as image sensors, one single sensor interface needs to be multiplexed among many sensor channels to achieve both high accuracy and good power efficiency. Analog-to-digital converter (ADC) architectures available for high-accuracy requirements are dual-slope Nyquist-rate ADC and $\Delta\Sigma$ ADCs. However, dual-slope ADCs are slow, and can convert only signals with very narrow bandwidths. $\Delta\Sigma$ ADCs rely on both analog and digital memory to achieve high accuracy, and therefore are not suitable multiplexing among channels. Furthermore, they introduce considerable latency between analog input and digital output, due to the complex digital filters needed for decimation.

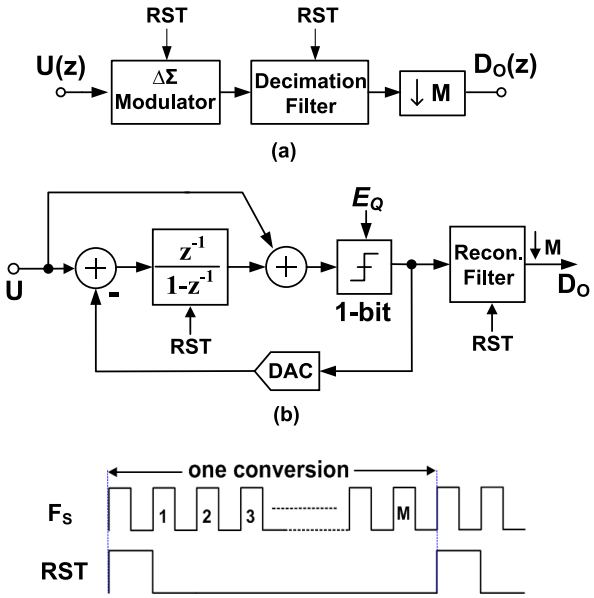

Fig. 1. Block diagram of a (a) conceptual incremental ADC and (b) first-order incremental ADC.

Incremental ADCs (IADCs) represent an excellent choice for use in low-frequency high-accuracy sensor interfaces [1]–[10]. The conceptual block diagram of an IADC is shown in Fig. 1(a). It uses an embedded $\Delta\Sigma$ modulator, and thus applies noise shaping to achieve high accuracy. However, after each conversion cycle lasting for M clock periods, a reset signal *RST* clears all the memory elements (integrators in the $\Delta\Sigma$ modulator and storage registers in the decimation filter). Therefore, unlike $\Delta\Sigma$ ADCs, the IADC operates intermittently, and provides a sample-by-sample conversion. This feature allows IADCs to be efficient in applications where a multiplexed low-frequency signal with high accuracy is converted. In addition, IADCs are immune to idle tones [11], and are more stable than $\Delta\Sigma$ ADCs.

Fig. 1(b) shows a first-order IADC (IADC1) with a wideband topology, which operates like a dual-slope ADC with integration and subtraction intermixed in time. An IADC1 has the simplest form and is unconditionally stable within the nonoverloading input range. Furthermore, it has the minimum

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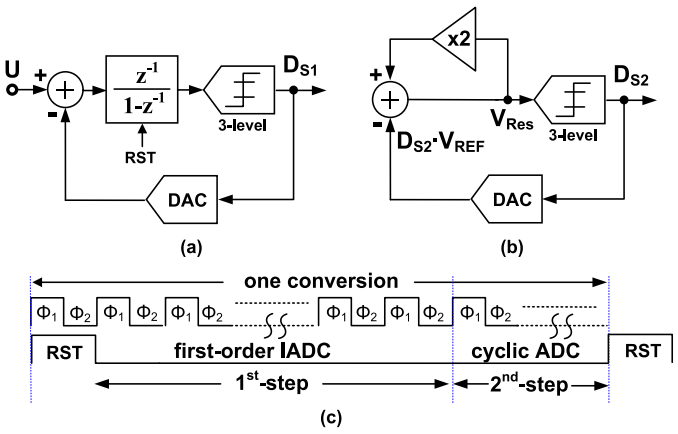


Fig. 2. Prior art of IADC with extended counting [4]. (a) First step: configured as an IADC1 for coarse quantization. (b) Second step: reconfigured as a cyclic ADC to extend the accuracy. (c) Timing diagram and two-phase clocks for one conversion.

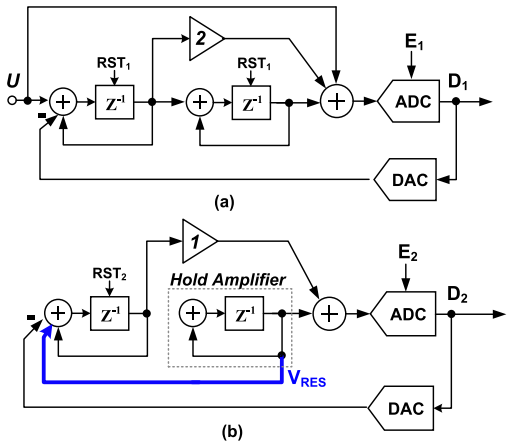


Fig. 3. Prior art of two-step IADC [16]. (a) First step: IADC2. (b) Second step: reconfigured as an IADC1 to achieve one extra order of noise shaping.

thermal noise penalty factor of one, compared with IADCs with high-order loops [12].

However, an IADC1 needs 2^N clock periods to achieve an N b resolution [13]. Hence, higher order implementations with single-loop or multistage noise shaping (MASH) were proposed earlier [1], [12]. These schemes suffer either from potential instability or from poor noise cancellation due to mismatch between analog and digital circuitry. A "zoom" scheme with high power efficiency was reported in [9], but the ADC converted only dc signals; an extension to time-varying signals was reported in [14]. Hybrid schemes with multi-step extended counting [3]–[5], [15] and high-order multi-step IADCs [16]–[19] have also been introduced. These schemes used multi-step operation, and achieved extended accuracy by recycling the residue voltage of the coarse quantization.

This paper presents a multi-step IADC that extends the accuracy using multi-slope extended counting [20], [21], which was first proposed in [21]. It cancels the residue voltage of the coarse quantization without transmitting it to the next stage [22], and is hence more robust than earlier extended counting ADCs. The remainder of this paper is organized as follows. Section II gives a brief overview of the reported multi-step IADCs, and introduces the proposed architecture. Circuit implementation details are described in Section III. The measurement results from the prototype test chip are provided in Section IV. Finally, Section V concludes this paper.

II. Proposed Architecture

A. Overview of Multi-step IADCs

In multi-step IADCs, to enhance the power efficiency, each conversion cycle is divided into separate steps, and therefore the hardware can be reused. A two-step design example [4] is shown in Fig. 2. In the first step, the IADC1 performs a coarse quantization, and the integrator stores the quantization residue. In the second step, the circuit operates as a 10 b cyclic ADC that converts the residue. Hence, the accuracy is extended, and the power efficiency significantly improved by reusing the hardware. However, the precision of sampling the residue from the prior step and the required multiplications by a factor of two limit the achievable accuracy [15].

Another IADC with multi-step operation [16], [17] is shown in Fig. 3. For the first step of operation, the second-order loop with an input feedforward path shapes the quantization noise. At the end of the first step, the residue voltage is stored at the second integrator output. During the second step, the second-order IADC (IADC2) is reconfigured as an IADC1, while the second integrator works as a holding amplifier, providing the residue voltage as a dc input. Thus, the two-step IADC2 achieves third-order performance sharing the same circuitry. However, the extra order of noise shaping is obtained by recycling the residue voltages from the prior step.

In both schemes, the accuracy is enhanced by delivering residue error to the next stages. Hence, the fine quantization step is vulnerable to nonideal effects in switched capacitor circuits, such as switches charge injection, clock feedthrough, and coupling through parasitics. Therefore, they require careful shielding and buffering of the quantization residue in order to achieve high accuracy.

The proposed scheme keeps the integrator operating in the same environment, and cancels the residue error only by detecting the polarity of the quantization residue, rather than transferring the coarse residue error for finer quantization.

B. Proposed IADC With Multi-slope Extended Counting

A multi-slope extended counting technique is proposed [20], [21]. It is shown in Fig. 4(a), where the proposed IADC is reconfigured in multi-step operation to extend its accuracy. The timing diagram of the multi-step operation is given in Fig. 4(b). Each conversion cycle between adjacent resets is split into three steps. The numbers of the clock periods assigned to the three steps are M_1, M_2, and M_3, respectively. During the first step, as shown in Fig. 5(a), the IADC uses a first-order $\Delta\Sigma$ loop with input feedforward architecture [23]. For high linearity, a single-bit quantizer is used, and an FIR feedback path $F(z) = 0.5 + 0.5z^{-1}$, together with the compensation path $C(z) = 0.5z^{-1}$ is introduced to reduce the voltage step at the integrator output V_{RES} [24]. A feedforward path $J(z) = 0.5z^{-1}$ is used to cancel the input signal content introduced by $C(z)$, and therefore to maintain the signal transfer function of the IADC to be close

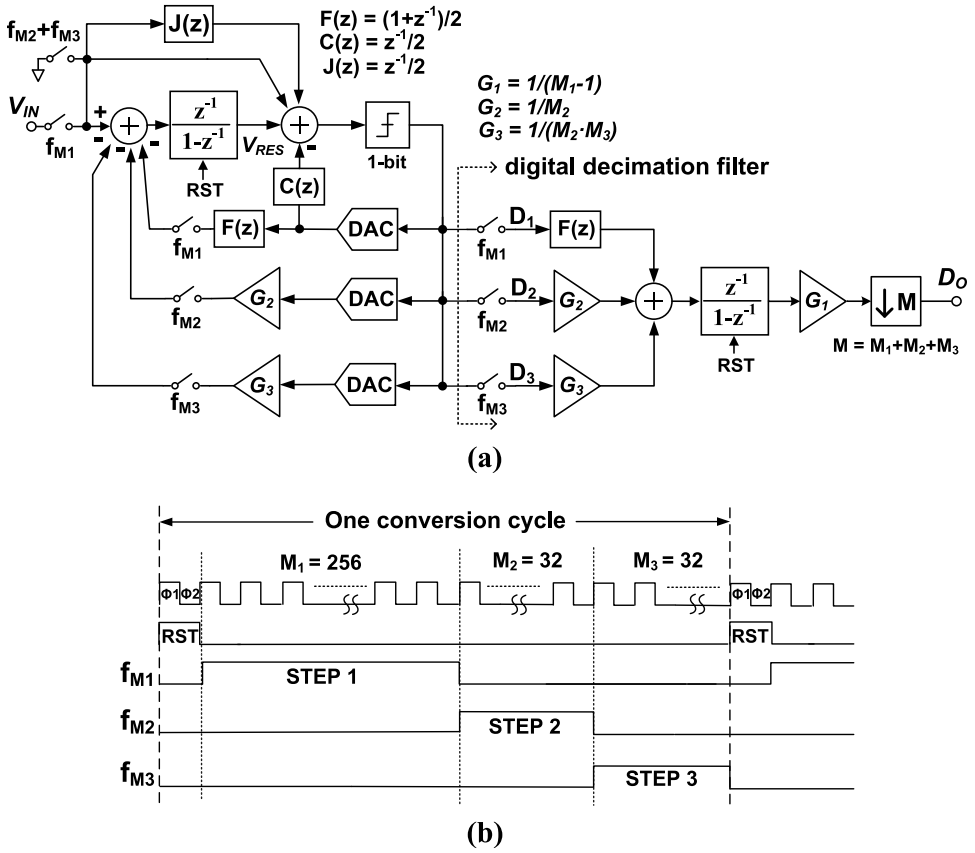


Fig. 4. (a) Block diagram of the proposed multi-step IADC with multi-slope extended counting. (b) Simplified timing diagram.

to unity within the signal bandwidth. As in a conventional feedforward IADC1, the integrator in the loop filter processes only the first-order shaped quantization noise, and it stores the quantization residue at its output V_{RES} after clock period M_1. Its magnitude is

$$|V_{\mathrm{RES}}[M_1]| = \left| \sum_{i=1}^{M_1-1} V_{\mathrm{IN}}[i] - F(z) \cdot V_{\mathrm{REF}} \sum_{i=1}^{M_1-1} D_1[i] \right| \leq V_{\mathrm{REF}}. \quad (1)$$

Note that the quantization residue is bounded by the reference voltage V_{REF}.

Next, $V_{\mathrm{RES}}[M_1]$ is stored at the integrator output for the second-step quantization. In the second step, as shown in Fig. 5(b), the input path is disconnected and the IADC is configured to cancel the quantization residue by counting with a slope coefficient $G_2 = 1/M_2$. Accordingly, the DAC step size is scaled to V_{REF}/M_2. The residue $V_{\mathrm{RES}}[M_1]$ at the integrator output is therefore quantized by a predetermined step size V_{REF}/M_2. At the end of the second step, the quantization residue is bounded by V_{REF}/M_2

$$|V_{\mathrm{RES}}[M_1 + M_2]| = \left| V_{\mathrm{RES}}[M_1] - G_2 \cdot V_{\mathrm{REF}} \sum_{i=1}^{M_2-1} D_2[i] \right| \leq \frac{V_{\mathrm{REF}}}{M_2}. \quad (2)$$

Similarly, for the final step, the circuit remains configured as a counting ADC, and it quantizes the quantization residue with a finer step size $V_{\mathrm{REF}}/(M_2 \cdot M_3)$, resulting in a slope coefficient $G_3 = 1/(M_2 \cdot M_3)$, as shown in Fig. 5(c). The residue V_{RES} is then reduced to less than one $LSB = V_{\mathrm{REF}}/(M_2 \cdot M_3)$ after M_3 additional steps

$$|V_{\mathrm{RES}}[M_1 + M_2 + M_3]| = \left| V_{\mathrm{RES}}[M_1 + M_2] - G_3 \cdot V_{\mathrm{REF}} \sum_{i=1}^{M_3-1} D_3[i] \right| \leq \frac{V_{\mathrm{REF}}}{M_2 \times M_3}. \quad (3)$$

Thus, in this process, the quantization residue is not recycled as in [4] and [16], but is gradually canceled by a coarse and fine DAC step size. It is connected only to the quantizer for polarity decisions. This makes the process robust. From (1) to (3), assuming that V_{IN} is constant during one conversion cycle, the digital representation of the average input signal $\overline{V_{\mathrm{IN}}}$ can be estimated from

$$\overline{V_{\mathrm{IN}}} = \frac{V_{\mathrm{REF}}}{M_1 - 1} \times \left[F(z) \cdot \sum_{i=1}^{M_1-1} D_1[i] + G_2 \cdot \sum_{i=1}^{M_2-1} D_2[i] + G_3 \cdot \sum_{i=1}^{M_3-1} D_3[i] \right] + \frac{V_{\mathrm{REF}}}{(M_1 - 1) \times M_2 \times M_3}. \quad (4)$$

The first term on the right-hand side (RHS) of (4) determines the digital decimation filtering needed to reconstruct the input signal from the bit-streams $D_k[i]$ of the three steps.

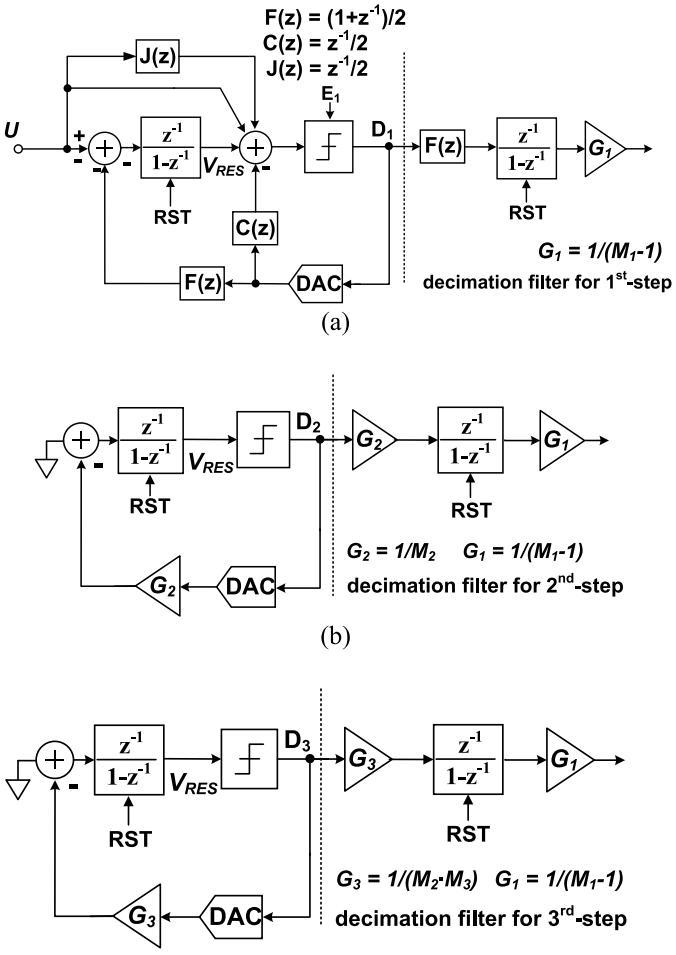


Fig. 5. (a) First step: an IADC1 with FIR feedback path. (b) Second step: reconfigured as a slope ADC with a coarse slope coefficient $G_2 = 1/M_2$. (c) Third step: reconfigured as a slope ADC with a reduced slope coefficient $G_3 = 1/(M_2 \cdot M_3)$.

As Fig. 4(a) shows, a single digital counter can be shared among all three steps for signal reconstruction. The second term on the RHS of (4) gives the equivalent quantization error after three-step operation. It gives $SQNR \approx 20\log_{10}(M_1 \cdot M_2 \cdot M_3)$. For such accuracy, a single-step IADC1 requires $(M_1 \cdot M_2 \cdot M_3)$ clock periods for each conversion cycle, whereas the proposed IADC needs only $(M_1 + M_2 + M_3)$ ones. The ENOB of the SQNR for this ADC is designed to be 18 b. Since the empirical element matching accuracy is usually as high as 10 b, the second and third steps are designed to realize 10 b accuracy. As a result, $M_2 = M_3 = 2^5$ gives the minimal total clock cycles for the additional two steps and M_1 is therefore assigned 2^8. This reduces the length of the conversion cycle by a large factor (in our device, by more than 2^9) for the same accuracy, compared with single-step IADC1.

A comparison of SQNRs as functions of the OSR for the proposed architecture and single-step IADCs of different orders is illustrated in Fig. 6. For the same OSR, the proposed multi-step IADC using one single integrator can achieve higher SQNR than a single-step IADC2. This indicates a significant power efficiency enhancement. The waveforms of the quantization residues of the steps at the integrator output

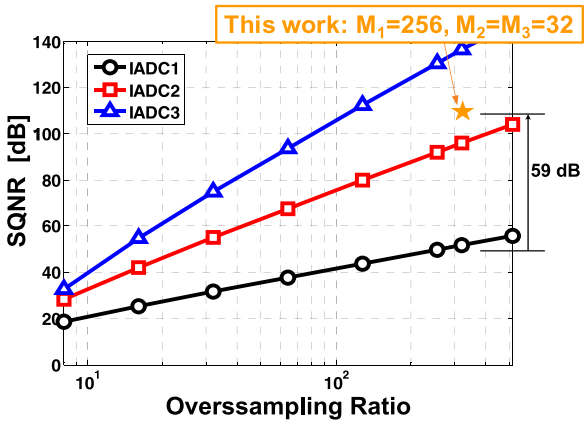


Fig. 6. Comparison of the proposed architecture with single-step IADCs. IADC3: third-order IADC.

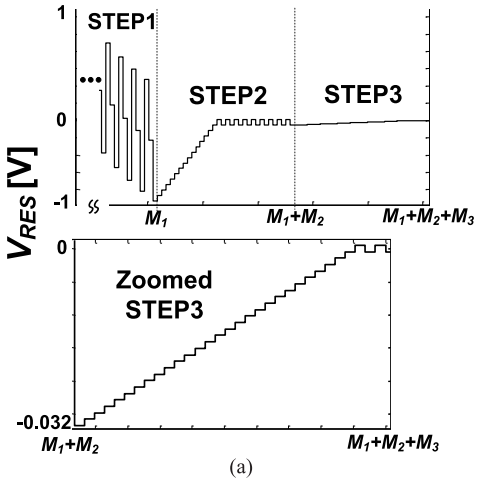


Fig. 7. (a) Simulated waveform of the residue at the integrator output during each step. (b) Simulated histogram of the voltage step at the integrator output with and without FIR feedback.

are illustrated in Fig. 7(a), where the first part of the waveform for the first step was left out. The residue error from the first step is quantized in the second and third steps, until it becomes smaller than one LSB due to the multi-slope extended counting. The FIR filtering feedback path $F(z)$ reduces the voltage step size at the integrator because it distributes the energy of the DAC signal over time [24]. This relaxes the slewing requirements of the opamp used in the integrator, as illustrated in the histograms of the voltage step sizes shown in Fig. 7(b).

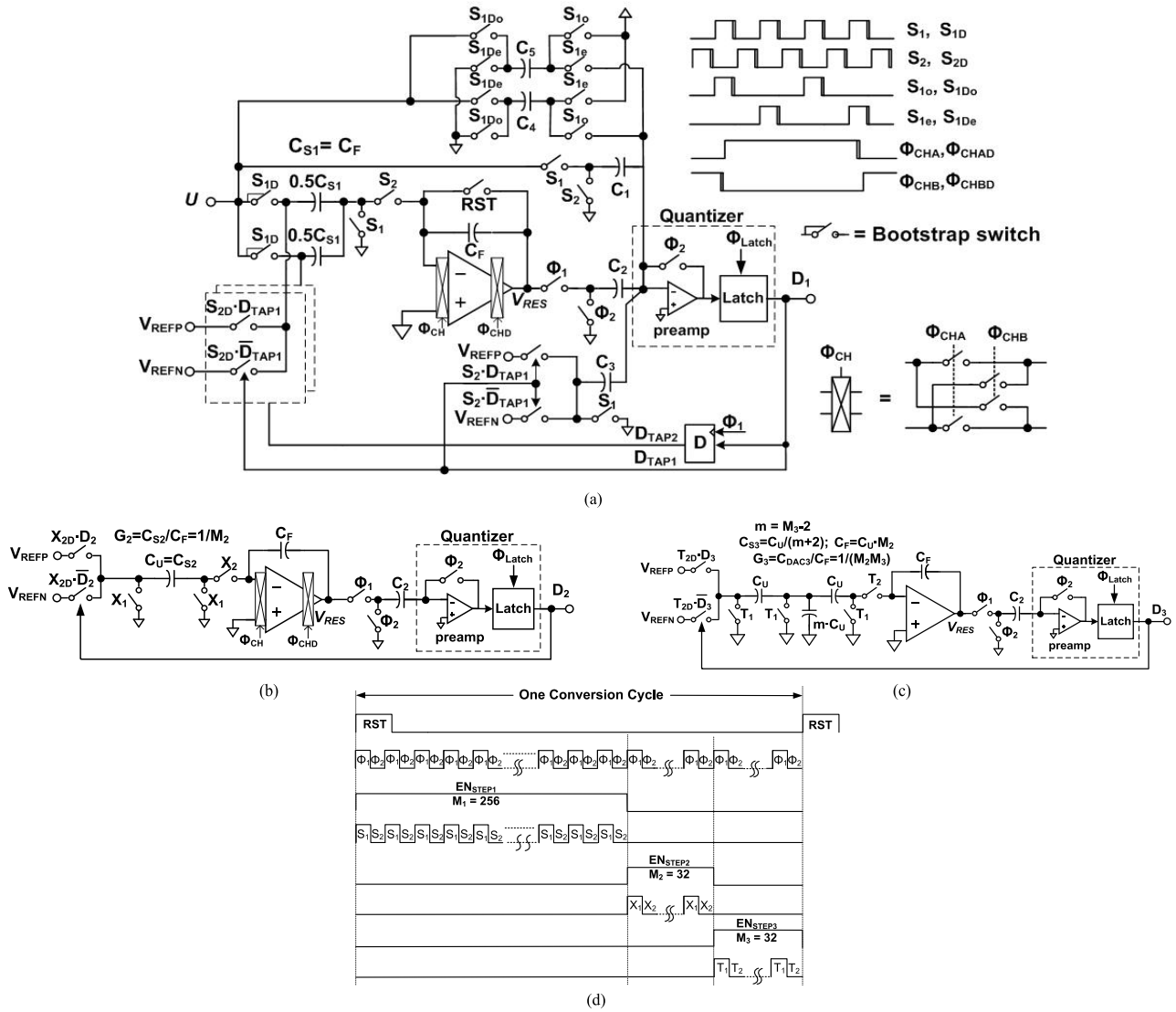


Fig. 8. Switched-capacitor implementation of the proposed IADC. (a) First step: an IADC1 with FIR feedback and compensation path. (b) Second step: reconfigured as a slope ADC with $G_2 = 1/M_2$. (c) Third step: using a capacitive T-network to implement the smaller slope coefficient $G_3 = 1/(M_2 \cdot M_3)$. (d) Simplified timing diagram for all steps.

III. Circuit Implementation

A. Switched-Capacitor Circuitry

The switched-capacitor implementation of the proposed IADC is illustrated step by step in Fig. 8(a)–(c). In the first step, the circuit is configured as an IADC1 with a low-distortion feedforward topology, shown in Fig. 8(a). It contains a single integrator with chopper stabilization, a two-tap (D_{TAP1} and D_{TAP2}) FIR feedback DAC with its compensation path containing a capacitor C_3, a full-cycle analog delay circuit comprising C_4 and C_5, and a passive summation network (C_1–C_5) feeding the single-bit quantizer. A single-ended implementation is shown for simplicity, but the actual implementation is fully differential.

The integrator sampling and integration phases are defined by the nonoverlapping clock phases $\Phi_1(S_1)$ and $\Phi_2(S_2)$. The integrator input sampling switches employ bootstrapped nMOS switches [25] for high linearity. Bottom-plate sampling is used to minimize the signal-dependent charge injection. Thus, switches connected to the top plate of the sampling capacitor and the virtual ground of the integrator are turned off slightly before those connected to the bottom plate. The sizes of the switches are kept minimal to reduce the channel charge and the nonlinear parasitic junction capacitance. All switches are single-channel devices. The reset operation controlled by *RST* is performed by shorting the integration capacitor C_F.

The FIR filtering feedback path $F(z) = 0.5 + 0.5z^{-1}$ is implemented by the sampling capacitor C_{S1} and the integration capacitor C_F. The compensation path $C(z) = 0.5z^{-1}$ is realized by the feedback network around the quantizer. The delayed input feedforward compensation path $J(z) = 0.5z^{-1}$ consists of capacitors C_4 and C_5. It is implemented by interleaving the sampling on the two capacitors. The present input is sampled onto one of the capacitors when the previous sample held on the other capacitor is quantized. The four switches are controlled by $S_{1\mathrm{o}}$ and $S_{1\mathrm{e}}$, working alternately. A capacitive passive adder using C_1–C_5 performs the summation at the quantizer input. The effect of the resulting signal

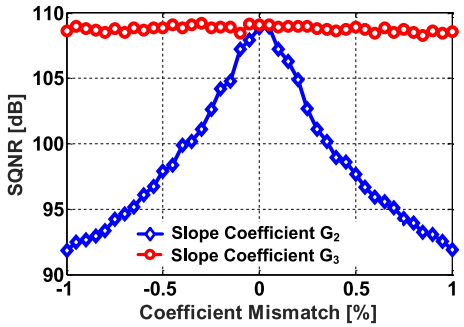


Fig. 9. Simulated SQNR of the proposed IADC as a function of mismatch errors in the slope coefficients G_2 and G_3.

attenuation is mitigated by the use of offset cancellation in the following quantizer.

The chopper scheme shown in Fig. 8(a) is used in the opamp to reduce its input-referred offset and suppress the flicker noise. In this design, the chopping operates in the middle of the sampling phase Φ_1 to prevent the integrator from sampling additional noise [26]. The input pair of the chopper network is cut off earlier than the output pair by Φ_{CHD}. This ensures that the signal-dependent charge is not injected into the opamp input when the output chopper network is turned off. Furthermore, the chopping switch network needs to be well balanced and carefully shielded to minimize unwanted noise coupling into the opamp's virtual ground node [27].

During the second step, as shown in Fig. 8(b), the two phases S_1 and S_2 used in the first step are disabled, while X_1 and X_2 are activated to reconfigure the circuit as an ADC with extended counting. The sampling capacitor C_{S2} is reduced to C_U, which results in a slope coefficient $G_2 = C_U/C_F = 1/M_2$, and a fixed step size V_{REF}/M_2 is used to quantize the residue voltage from the prior step. This operation causes the integrator output V_{RES} to decrease below V_{REF}/M_2 after M_2 steps, and the quantizer repeatedly decides the polarity of V_{RES}.

In the third step, illustrated in Fig. 8(c), the quantization residue is reduced by a finer step size $V_{\mathrm{REF}} \cdot G_3$, where $G_3 = 1/(M_2 \cdot M_3)$. This small coefficient is implemented by a capacitive T-network [29]. By setting the factor m in the T-pad to $M_3 - 2$, the equivalent capacitor C_{S3} in the DAC for the third step is equal to $C_U/(m+2)$. As a result, the coefficient G_3 can be realized by the capacitor ratio $C_{S3}/C_F = 1/(M_2 \cdot M_3)$. This avoids the use of impractically small capacitors to realize such a small ratio. At the end of this step, the residue voltage of V_{RES} is bounded by $V_{\mathrm{REF}}/(M_2 \cdot M_3)$. Fig. 8(d) gives the detailed timing for each step. An external 1.284 MHz clock is used to generate the control signal *RST* and $EN_{STEP1-3}$. The two-phase nonoverlapping clock phases Φ_1 and Φ_2 are used in all three steps, whereas the clock phases S_{1-2}, X_{1-2}, and T_{1-2} are generated specifically for each step. The IADC operates at $f_S = 642$ kHz and the chopper circuitry at $f_S/4$.

B. kT/C Thermal Noise and Mismatch Effects

During the third step, the accumulated noise power $\overline{V_{N,RES}^2}$ at the differential output of the integrator can be found as

$$\overline{V_{N,RES}^2} = \left(\frac{2kT}{C_U}\right)\left[\left(1+\left(\frac{1}{m+1}\right)^2\right) \times \left(1+\frac{m+1}{m+2}+\frac{1}{(m+1)(m+2)}\right)\right]\left(\frac{C_U}{C_F}\right)^2 \cdot M_3 \approx \left(\frac{4kT}{C_U}\right)\left(\frac{C_U}{C_F}\right)^2 \cdot M_3 \quad (5)$$

where $m = 30$ and the unit capacitor C_U in the capacitive T network is sized so that after M_3 clocks, the *rms* value of the noise power $\overline{V_{N,RES}^2}$ would be bounded by half of the finest step size

$$\sqrt{\overline{V_{N,RES}^2}} = \sqrt{\frac{4kT \cdot M_3}{C_U}} \cdot \frac{C_U}{C_F} = \sqrt{\frac{4kT}{C_U M_3}} \le \frac{V_{FS}}{2 \cdot M_2 \cdot M_3} \quad (6)$$

where $C_U/C_F = 1/M_2$ and (6) gives that $C_U \ge 2.2$ fF. The sampling capacitor C_{S1} for the first step ($M_1 = 256$) is designed to be 3.2 pF, resulting in $C_F = 3.2$ pF and SNR = 104 dB with only *kT/C* thermal noise considered. The second step uses $M_2 = 32$ and the ratio $G_2 = C_{S2}/C_F = 1/M_2$ leads to the sampling capacitor $C_U = C_{S2} = 100$ fF. Care must also be taken in setting the *rms* value of the noise power contributed by the comparator to make sure that it is less than the finer step size.

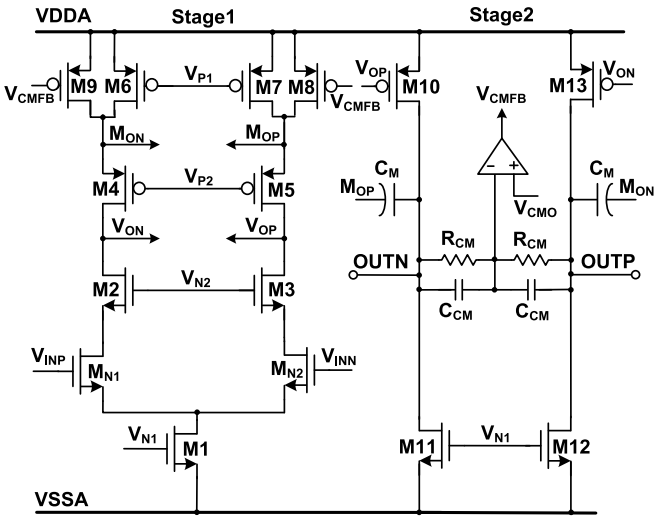


Fig. 10. Opamp circuit used in the integrator.

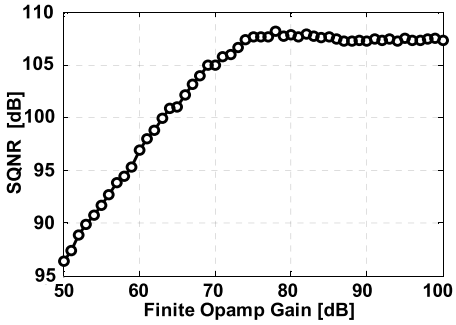


Fig. 11. Simulated SQNR of the proposed IADC as a function of finite opamp gain.

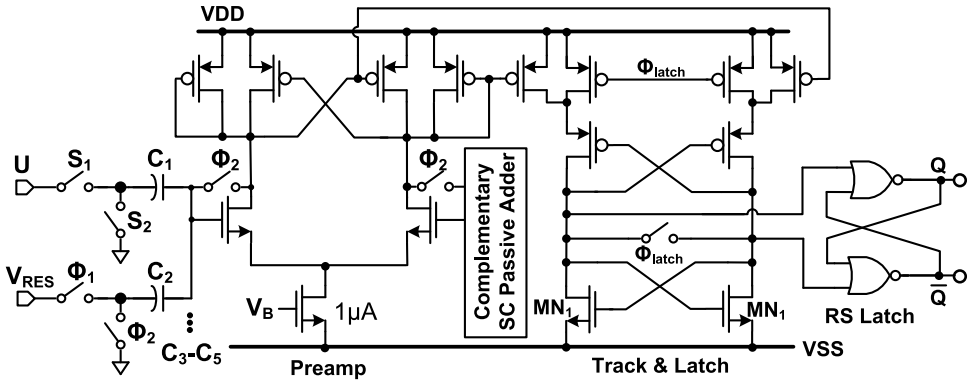


Fig. 12. Circuit diagram of the passive adder and the comparator circuit used in the quantizer.

Since the slope coefficients G_2 and G_3 are realized by capacitor ratios, the errors of these ratios will produce mismatch of the coefficients between the analog and digital domains, thus causing performance degradation. Fig. 9 plots the simulated SQNR as a function of errors of the slope coefficients G_2 and G_3. Fig. 9 shows that the IADC is more sensitive to the error of G_2, since it introduces error in the coarse quantization. No visible degradation in the performance of the IADC was found due to the error of G_3 for practical error values. Behavioral simulations indicate that with an error of G_2 as large as $\pm 0.5\%$, the IADC can achieve SQNR higher than 100 dB. In a 0.18 μm CMOS process, it is not difficult to meet such error requirements.

C. Integrator Opamp

Since the ADC is configured for a three-step operation, the opamp in the integrator may experience varying output loading condition. Hence, a two-stage topology was selected because then the dominant pole is decided by the Miller capacitor, instead of the output loading capacitor as in single-stage topology. The unity gain bandwidth of the opamp was designed to be 4.7 MHz. The fully differential opamp used in the integrator is shown in Fig. 10. A telescopic cascode amplifier is used in the first stage, and the second stage is implemented with a common-source amplifier that can provide an output swing as high as ± 1 V. The opamp employs the cascode Miller compensation technique [28] for stabilization. This technique blocks the feedforward path and therefore eliminate the left-hand plane zero. The common-mode voltage is sensed by the *RC* network and applied to a common-mode amplifier, which regulates the common-mode output. The opamp consumes 16 μA and achieves a dc gain of 82 dB with a 1.5 V power supply.

The finite dc gain of the integrator is critical in MASH $\Delta\Sigma$ modulators [29], [30], since the topology requires a noise cancellation logic in the digital domain. The finite opamp gain creates mismatch between the analog and digital realizations of the noise transfer function $(1-z^{-1})^N$. To achieve a 16 b SNR for a MASH $\Delta\Sigma$ ADC, the opamp gain is typically required to be no less than 90 dB [30]. However, in the proposed multi-step IADC, no noise cancellation logic is needed in the digital reconstruction, and therefore the dc gain requirement

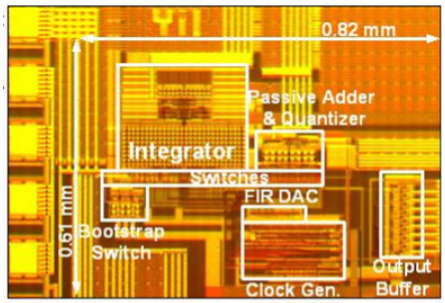


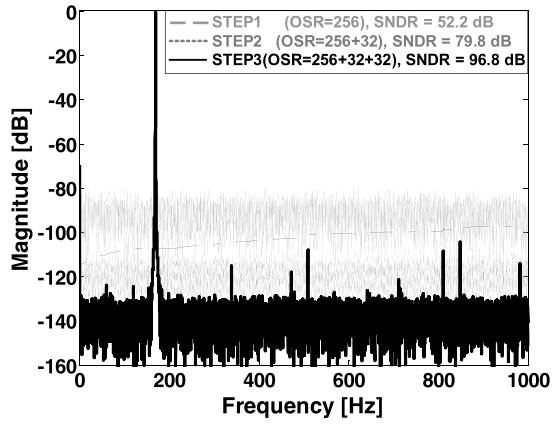
Fig. 13. Chip micrograph of the prototype IADC.

of the opamp can be relaxed. Estimation and analysis of the required opamp gain requirement can be found in [31] and [32]. Fig. 11 plots the simulated SQNR of the proposed IADC as a function of the opamp dc gain. It shows that the SQNR begins to drop only when the gain of the opamp is less than 75 dB.

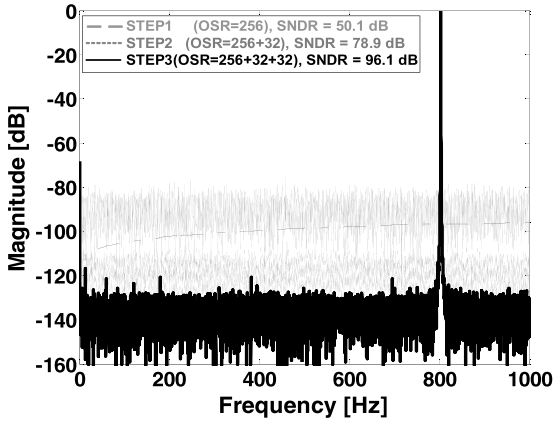
D. Passive Adder and Comparator

The comparator used in the quantizer consists of a preamplifier stage biased with 1 μA of tail current, a regenerating latch, and an RS latch, as shown in Fig. 12. A switched-capacitor passive adder is used at the input of the quantizer to combine the input, integrator output, and compensation feedback path signals. Due to charge sharing, signal attenuation takes place at the quantizer input. Therefore, a preamplifier is used. It applies an auto-zeroing technique to achieve a low comparator input-referred offset [33]. During Φ_2, the comparator offset is sampled onto the summing capacitors C_1–C_5. This stored offset is canceled during the quantization phase Φ_1. Due to the use of the auto-zeroing technique, the offset error is no longer a critical issue. In addition, the static offset error does not limit the relative accuracy; instead, it affects the absolute accuracy of the conversion and appears as a tone at dc in the output spectrum.

The preamplifier utilizes a negative transconductance and diode-connected load to enhance the equivalent dc gain. Careful sizing was used to prevent positive feedback. After each quantization phase Φ_1, the comparator enters the tracking mode by closing the switch controlled by Φ_{latch}. The dynamic offset is reduced by having the two terminals of the switch



(a)



(b)

Fig. 14. Measured PSDs for the three steps, with a −0.44 dBFS sine-wave input signal. (a) 170 Hz input frequency. (b) 800 Hz input frequency (2^{14}-point FFT). Top: first step. Middle: second step. Bottom: third step.

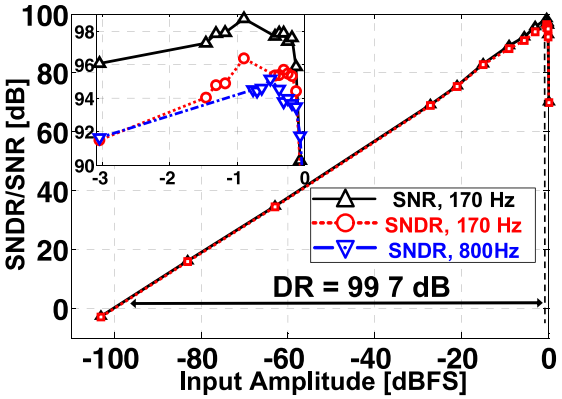


Fig. 15. Measured SNR/SNDR versus the input amplitude for 170 and 800 Hz inputs.

biased around the V_{GS} of MN_1 instead of sitting at the rail, at the cost of consuming some static power [34]. The following RS latch maintains the valid CMOS levels during the full clock cycle.

IV. Measurement Results

The prototype test chip was fabricated in a 0.18 μm CMOS process. It occupies an active area of 0.5 mm^2. The chip micrograph is shown in Fig. 13. The die is packaged in a 48-pin QFN. Clocked at 642 kHz, the proposed IADC consumes 35 μW. Both analog and digital blocks use a 1.5 V supply. A common-mode voltage of 0.75 V was used, and the differential full-scale range of the IADC is 2 V_{PP}. The achieved PSRR at 50 Hz line frequency is at least 102 dB.

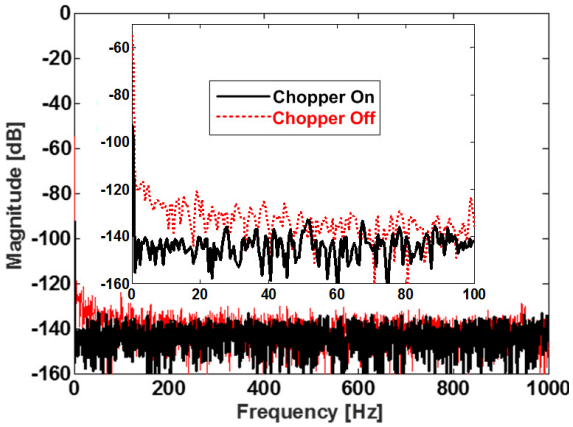


Fig. 16. Measured spectra with the chopper turned on versus chopper turned off. Input terminals are shorted when measured.

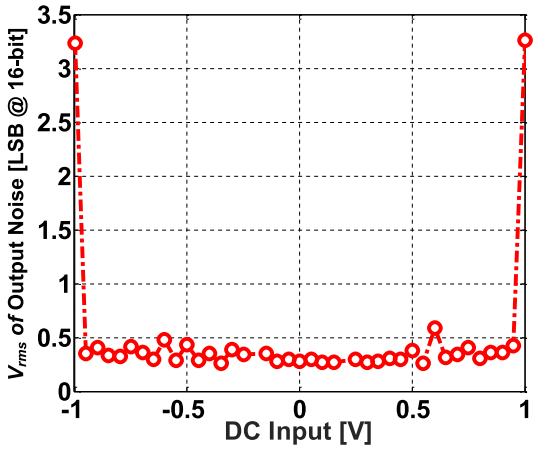


Fig. 17. Measured output noise of the prototype IADC with dc input.

An Audio Precision Sys-2722 was used to provide the differential input signal tone to the IADC. Fig. 14(a) shows the measured output power spectral densities (PSDs) for the three steps with a 170 Hz −0.44 dBFS input sinusoid signal. It indicates that the IADC achieves an SNDR of 52.2 dB over a 1 kHz bandwidth during the first step. The extended multi-slope counting in the second and third steps then enhance the SNDR to 79.8 and 96.8 dB, respectively.

The measured PSD for an 800 Hz sinusoid signal is shown in Fig. 14(b). A Hanning window was used, and the number of the fast Fourier transform (FFT) points within the 1 kHz bandwidth was 2^{14}. The SNR and SNDR are plotted as functions of the input amplitudes for 170 and 800 Hz inputs in Fig. 15. The IADC achieves the dynamic range of 99.7 dB, and the peak SNR is 98.4 dB. Trimming of the coefficient G_2 was performed in the postprocessing. However, little enhancement was observed before and after the fine trimming, since the overall ADC is dominated by the thermal noise. The input-referred opamp thermal noise is believed to be the dominant noise source and, it limits the IADC performance.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS WORK

Parameter	This Work	Chen, JSSC 2015 [2]	Agah JSSC 2010 [3]	Chen ISSCC 2013 [37]	Tao TCASI 2015 [36]	Rombouts JSSC 2001 [4]	Goenen ISSCC 2016 [14]	Rombouts ESSCIRC 2012 [5]	Ha ESSCIRC 2013 [35]
Architecture	**IADC1 + Multi-Slope**	IADC2 +IADC1	IADC2 + SAR	Single IADC2	CT IADC	IADC1 + Cyclic	Zoom ADC	IADC1+ Cyclic	SAR+ IADC1
Technology(nm)	**180**	65	180	160	180	800	160	180	600
Area (mm^2)	**0.5**	0.2	3.5	0.45	0.337	1.3	0.16	0.031	1.64
V_{DD} (V)	**1.5**	1.2	1.8	1	1.2/1.8	1.2	1.8	3.3	3.3
Diff. input range (V_{PP})	**2**	2.2	2	0.7	-	2.4	3.5	-	2
Sampling Freq. (MHz)	**0.642**	0.192	45	0.75	0.32	0.256	11	13	0.5
BW (kHz)	**1**	0.25	500	0.667	4	8	20	500	9.75
Power (μW)	**34.6**	10.7	38100	20	34.8	150	1650	1600	64
SNDR (dB)	**96.8**	90.8	86.3	81.9	75.9	80	98.3	74.5	70.7
Peak SNR (dB)	**98.4**	-	89.1	-	76.6	-	104.4	-	-
DR (dB)	**99.7**	99.8	90.1	81.9	85.5	82	107.5	78	84.6
FoM^1_W (pJ/conv)	**0.32**	0.76	1.46	1.48	0.85	1.15	0.32	0.39	1.17
FoM^2_S (dB)	**174.6**	173.5	161.3	157.1	166.1	159.3	178.3	159.4	166.4

1. FoM_W = Power/($2^{(SNDR-1.76)/6.02}$ x 2 x BW). 2. FoM_S = DR + 10 x $\log_{10}$(BW / Power)

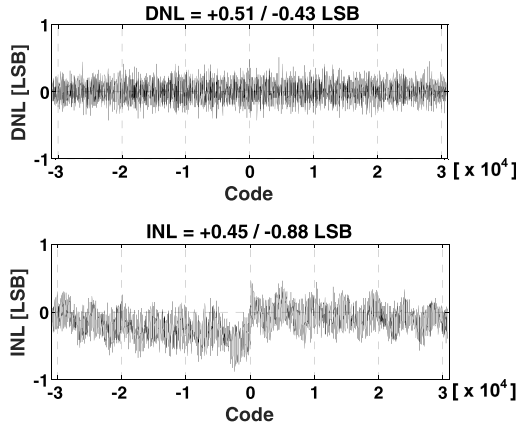


Fig. 18. Measured INL/DNL in 16 b accuracy LSBs.

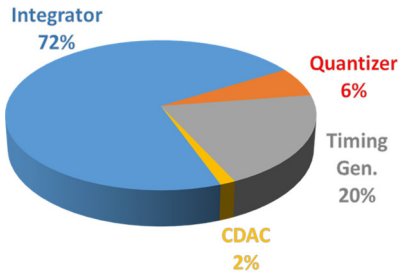


Fig. 19. Power summary of the prototype IADC.

The measured power at dc was around −68 dBFS, which corresponds to a 0.7 mV offset. This offset was found to result from the instrumentation, not from the IADC itself.

With the input terminals shorted to the common-mode voltage 0.75 V, the measured PSDs with the chopper turned ON and OFF are illustrated in Fig. 16. The chopper stabilization reduced the flicker noise significantly, and decreased the measured output noise from 7.54 to 3.76 μV_{RMS}. The measured dc offset was reduced from −56 (3.2 mV) to −92 dBFS (50.2 μV) by the chopper stabilization.

A dc input was swept within the full-scale range of the IADC, and the output noise was measured and plotted in terms of 16 b LSB, as shown in Fig. 17. The spurs at two ends are due to the overloading of the IADC. The idle tones, which commonly exist in low-order ΔΣ ADCs, are not found in the IADC [11], [29]. This can be intuitively understood as follows: when a dc input is applied to the IADC, the output sample taken from each reset window tends to stay the same if the white thermal noise is not considered. Hence, no repetitive pattern forms, as does in ΔΣ ADCs. The DNL/INL errors determined by the histogram testing with a sinusoidal input signal are shown in Fig. 18. A power pie chart is given in Fig. 19. It shows that the integrator requires most of the power consumption.

Table I summarizes the measured performance, and compares it with state-of-art IADCs of earlier architectures. The Walden and Schreier figures of merits (FoM_W and FoM_S) were calculated using the formulas

$$FoM_W = \frac{\text{Power}}{2^{\text{ENOB}} \cdot 2\text{BW}} \tag{7}$$

$$FoM_S = \text{DR} + 10 \cdot \log \frac{\text{BW}}{\text{Power}}. \tag{8}$$

The prototype ADC divides one conversion cycle into three steps and extends the accuracy by reusing the same integrator, which keeps this integrator operating in the same environment during the additional steps. Instead of transferring the residue error to other stages, it cancels the error simply by the polarity decision of the quantizer, making the ADC operation more robust and linear. As a result, it achieved an FoM_W of 0.32 pJ/conv-step and an FoM_S of 174.6 dB, both among the best values for state-of-art IADCs. Both FoMs were included for a more complete comparison, although the FoM_W is less meaningful for low-frequency high-resolution ADCs.

V. Conclusion

A multi-step IADC with multi-slope extended counting technique was proposed for integrated sensor interface circuits. Each conversion cycle is divided into three steps, and a single active integrator is reused in each step to quantize the residue voltages. The accuracy is extended by configuring the IADC as multi-slope ADCs in additional steps. The slope coefficients are realized by capacitor ratios, which achieved good matching accuracy. For a given OSR, the proposed multi-step IADC achieved a better efficiency than a single-step IADC2, at the reduced cost of only one active component. A prototype test chip was fabricated in 0.18 μm process. It occupies an active area of 0.5 mm^2. It is clocked at 642 kHz, and consumes 35 μW with a 1.5 V power supply. It achieves an SNDR of 52.2 dB for the first step; after the second step, the SNDR becomes 79.8 dB; and after the third step, the SNDR reaches 96.8 dB over a 1 kHz bandwidth. The implemented ADC achieves an FoM_W of 0.32 pJ/conv-step and an FoM_S of 174.6 dB. The proposed multi-step IADC appears to be a highly power-efficient solution for integrated sensor interfaces.

Acknowledgment

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References

[1] V. Quiquempoix *et al.*, "A low-power 22-bit incremental ADC," *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1562–1571, Jul. 2006.

[2] C.-H. Chen, Y. Zhang, T. He, P. Chiang, and G. C. Temes, "A 11μW 250 Hz BW two-step incremental ADC with 100 dB DR and 91 dB SNDR for integrated sensor interfaces," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, San Jose, CA, USA, Sep. 2014, pp. 1–4.

[3] A. Agah, K. Vleugels, P. B. Griffin, M. Ronaghi, J. D. Plummer, and B. A. Wooley, "A high-resolution low-power incremental $\Sigma\Delta$ ADC with extended range for biosensor arrays," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1099–1110, Jun. 2010.

[4] P. Rombouts, W. D. Wilde, and L. Weyten, "A 13.5-b 1.2-V micropower extended counting A/D converter," *IEEE J. Solid-State Circuits*, vol. 36, no. 2, pp. 176–183, Feb. 2001.

[5] P. Rombouts, P. Woestyn, M. Bock, and J. Raman, "A very compact 1MS/s Nyquist-rate A/D converter with 12 effective bits," in *Proc. Eur. Solid-State Circuits Conf. (ESSCIRC)*, 2012, pp. 213–216.

[6] C.-H. Chen, J. Crop, J. Chae, P. Chiang, and G. C. Temes, "A 12-bit 7 μW/channel 1 kHz/channel incremental ADC for biosensor interface circuits," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2012, pp. 2969–2972.

[7] J.-H. Kim *et al.*, "A 14b extended counting ADC implemented in a 24MPixel APS-C CMOS image sensor," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 390–391.

[8] Y. Oike and A. El Gamal, "CMOS image sensor with per-column $\Sigma\Delta$ ADC and programmable compressed sensing," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 318–328, Jan. 2013.

[9] J. Y. Chae, K. Souri, and K. A. Makinwa, "A 6.3 μW 20 bit incremental zoom-ADC with 6 ppm INL and 1 μV offset," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3019–3027, Dec. 2013.

[10] C.-H. Chen, T. He, Y. Zhang, and G. C. Temes, "History, present state-of-art and future of incremental ADCs," in *Proc. Eur. Solid-State Circuits Conf. (ESSCIRC)*, 2016, pp. 83–86.

[11] S. Kavusi, H. Kakavand, and A. El Gamal, "On incremental sigma-delta modulation with optimal filtering," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 5, pp. 1004–1015, May 2006.

[12] T. C. Caldwell and D. A. Johns, "Incremental data converters at low oversampling ratios," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 7, pp. 1525–1537, Jul. 2010.

[13] J. Markus, J. Silva, and G. C. Temes, "Theory and applications of incremental delta sigma converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 4, pp. 678–690, Apr. 2004.

[14] B. Goenen, F. Sebastiano, R. Veldhoven, and K. Makinwa, "A 1.65 mW 0.16 mm^2 dynamic zoom-ADC with 107.5 dB DR in 20 kHz BW," in *IEEE ISSCC Dig. Tech. Papers*, Jan./Feb. 2016, pp. 282–283.

[15] G. Mulliken, F. Adil, G. Cauwenberghs, and R. Genov, "Delta-sigma algorithmic analog-to-digital conversion," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2002, pp. 687–690.

[16] C.-H. Chen, Y. Zhang, T. He, P. Chiang, and G. C. Temes, "A micro-power two-step incremental analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 1796–1808, Aug. 2015.

[17] C.-H. Chen, Y. Zhang, Y. Jung, T. He, J. L. Ceballos, and G. C. Temes, "Two-step incremental analogue-to-digital converter," *Electron. Lett.*, vol. 49, no. 4, pp. 250–251, Feb. 2013.

[18] T. He, Y. Zhang, X. Meng, G. Temes, and C.-H. Chen, "A 16-bit 1KHz bandwidth micro-power multi-step incremental ADC for multi-channel sensor interface," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2015, pp. 1018–1021.

[19] C. H. Chen, Y. Zhang, T. He, and G. C. Temes, "Two-step multi-stage incremental ADC," *Electron. Lett.*, vol. 51, no. 24, pp. 1975–1977, 2015.

[20] Y. Zhang, C. H. Chen, T. He, and G. C. Temes, "A 35μW 96.8dB SNDR 1 kHz BW multi-step incremental ADC using multi-slope extended counting with a single integrator," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2016, pp. 24–25.

[21] C.-H. Chen, Y. Jung, J. L. Ceballos, and G. C. Temes, "Multi-step extended-counting analogue-to-digital converter," *Electron. Lett.*, vol. 49, no. 1, pp. 30–31, Jan. 2013.

[22] Y. Zhang, C.-H. Chen, T. He, and G. C. Temes, "Multi-step incremental ADC with extended binary counting," *Electron. Lett.*, vol. 52, no. 9, pp. 697–699, 2016.

[23] J. Silva, U.-K. Moon, J. Steensgaard, and G. C. Temes, "A wideband low-distortion delta-sigma ADC topology," *Electron. Lett.*, vol. 37, no. 12, pp. 737–738, 2001.

[24] O. Oliaei, "Sigma-delta modulator with spectrally shaped feedback," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 50, no. 9, pp. 518–530, Sep. 2003.

[25] M. Dessouky and A. Kaiser, "Very low-voltage digital-audio $\Sigma\Delta$ modulator with 88-dB dynamic range using local switch bootstrapping," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 349–355, Mar. 2001.

[26] Y. Yang, A. Chokhawala, M. Alexander, J. Melanson, and D. Hester, "A 114-dB 68-μW chopper-stabilized stereo multibit audio ADC in 5.62 mm^2," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2061–2068, Dec. 2003.

[27] R. Wu, Y. Chae, J. H. Huijsing, and K. A. A. Makinwa, "A 20-b $\pm$40-mV range read-out IC with 50-nV offset and 0.04% gain error for bridge transducers," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2152–2163, Sep. 2012.

[28] B. K. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers," *IEEE J. Solid-State Circuits*, vol. 18, no. 6, pp. 629–633, Dec. 1983.

[29] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*. Piscataway, NJ, USA: Wiley, 2005.

[30] I. Fujimori *et al.*, "A 90-dB SNR 2.5-MHz output-rate ADC using cascaded multibit delta–sigma modulation at 8$\times$ oversampling ratio," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1820–1828, Dec. 2000.

[31] R. Harjani and T. A. Lee, "FRC: A method for extending the resolution of Nyquist rate converters using oversampling," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 45, no. 4, pp. 482–494, Apr. 1998.

[32] C.-H. Chen, T. He, Y. Zhang, and G. C. Temes, "Incremental analog-to-digital converter for high-resolution energy-efficient sensor interfaces," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 5, no. 4, pp. 612–623, Dec. 2015.

[33] C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Auto-zeroing, correlated double sampling, chopper stabilization," *Proc. IEEE*, vol. 84, no. 11, pp. 1584–1614, Nov. 1996.

[34] I. Mehr and D. Dalton, "A 500-MSample/s, 6-bit Nyquist-rate ADC for disk-drive read-channel applications," *IEEE J. Solid-State Circuits*, vol. 34, no. 7, pp. 912–920, Jul. 1999.

[35] S. Ha, J. Park, Y. M. Chi, J. Viventi, J. Rogers, and G. Cauwenberghs, "85 dB dynamic range 1.2 mW 156 kS/s biopotential recording IC for high-density ECoG flexible active electrode array," in *Proc. Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2013, pp. 141–144.

[36] S. Tao and A. Rusu, "A power-efficient continuous-time incremental sigma-delta ADC for neural recording systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 6, pp. 1489–1498, Jun. 2015.

[37] C. Chen, Z. Tan, and M. A. P. Pertijs, "A 1V 14b self-timed zero-crossing-based incremental $\Sigma\Delta$ ADC," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 274–275.

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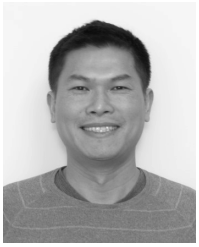

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