A Hybrid Switched-Capacitor Battery Management IC With Embedded Diagnostics for Series-Stacked Li–Ion Arrays

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***Abstract*— This paper presents a small form factor dc–dc converter that can be used in a ladder architecture to provide state-of-charge equalization for large-scale lithium-ion arrays. A resonant switched-capacitor converter is implemented in a 180-nm bulk CMOS process that uses a merged-interleaving architecture to affect two-phase interleaving with only a single inductor. The approach has the advantage of reducing passive component volume for a given efficiency and voltage ripple constraint. A bidirectional current-mode control scheme is outlined that uses regulated zero-current switching and partial zero-voltage switching. The design also supports electrochemical diagnostic functions through a fully digital spectroscopic perturbation of cell current. Cell voltage and current are digitized through 10-b SAR analog to digital converters (ADCs), filtered and decimated for off-chip impedance extraction. The converter achieves 94.8% conversion efficiency in 1:1 balancing mode with a total board area less than 1 cm^2, and supports bidirectional power transfer >3.7 W.**

***Index Terms*— Battery management, dc–dc converters, power integrated circuits, switched capacitor.**

I. Introduction

ELECTROCHEMICAL energy storage is positioned as a critical technology in coming decades due to the growing adoption of electrified transportation and increasing penetration of renewable generation in the electrical grid [1]–[3]. These trends have created an acute need for electronics that manage energy flow in large electrochemical arrays, where groups of cells are configured in large series strings [4]–[7]. The series connection is notoriously problematic: in unbalanced arrays, the capacity of the pack may be limited by the weakest cell. Without correction, the capacity reduction is incurred in both charge and discharge cycles, and ultimately, because of the relatively more aggressive use of weaker cells, they tend to age more rapidly, compounding mismatch over time [3].

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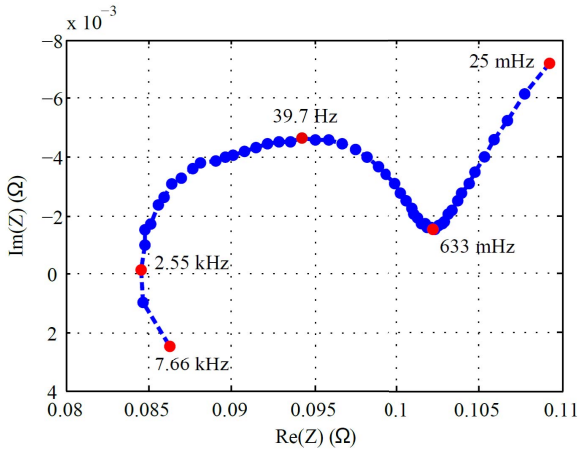

Fig. 1. Representative Nyquist plot (EIS signature) for a Panasonic 18650 Li–ion cell (3400 mAh) from [7].

Mismatch, variability, and nonuniform cell degradation play a major role in the overall rated capacity and lifetime of most large-scale battery packs. In automotive applications, uncertainty in the operating states of individual cells and the pack as a whole lead to system overdesign in terms of capacity, cost, weight, and power density [2]. Therefore, in addition to better methods to manage energy flow within the pack, there is a need to improve diagnostic capabilities in electrochemical systems. Typical metrics in most systems include state of charge (SOC) which is an estimate of available energy capacity, and state of health, an estimate of remaining useful life [8], [9]. The most common (commercially deployed) state estimation techniques use very accurate voltage and current measurement (coulomb counting) and extensive look up tables or complex behavioral models [10], [11].

However, impedance-based state and health estimation techniques are also well known in the electrochemistry literature [8], [10], [12]. In particular, electrochemical impedance spectroscopy (EIS) is widely used at the laboratory benchtop as it can characterize specific phenomena through their underlying dynamical properties. As shown in Fig. 1, the common output of an EIS characterization is an "inverted" Nyquist plot of cell impedance. Typical regimes of interest include the mass-transport region at low frequencies (mHz–μHz), double layer capacitive effects at the anode and cathode (Hz–kHz), and electromagnetic effects (>kHz). The EIS perspective is

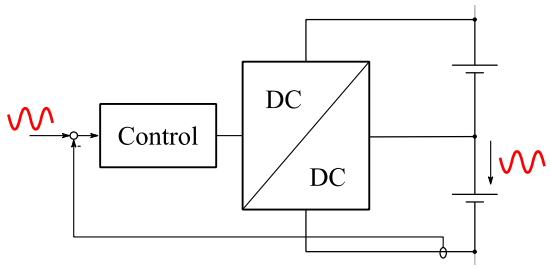

Fig. 2. Conceptual illustration of management and diagnostic scheme developed in this paper.

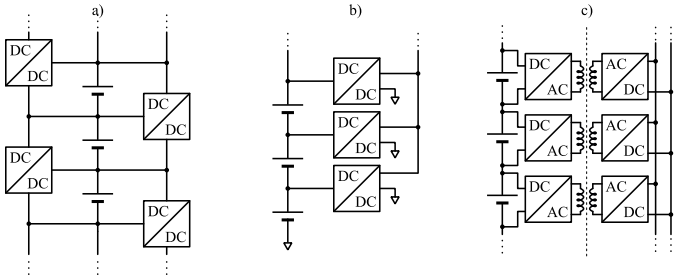

Fig. 3. Representative active balancing architectures. (a) Ladder Architecture. (b) DC to Bus Architecture. (c) Auxiliary (isolated) bus Architecture.

often helpful to gain insight into the underlying electrochemistry of a given cell through a single-port, non-destructive means, and is suitable for implementing with a variety of external electronic hardware.

While EIS is most commonly explored with an expensive benchtop equipment (impedance analyzers, potentiostats, and galvanostats), recent efforts have explored embedding spectroscopic diagnostics into the battery management system (BMS) [7], [12], [13]. In principle, this could provide a great volume of diagnostic information, especially if it can be practically and cost effectively embedded at the cell or module level in a large battery array. The most direct use could be for state of health, failure and fault detection. However, other research has explored EIS as a tool to estimate SOC and other metrics [14], [15]. Conceptually illustrated in Fig. 2, the goal of this paper is to highlight the prospects for real-time impedance-based diagnostics, implemented in a low cost, near-monolithic (mm-scale) dc–dc converter that can also be used for bidirectional balancing. As such, we will focus less on the electrochemical details and more on the circuit and system implementation.

The specific hardware implementation presented in this paper is based on a resonant switched-capacitor (ReSC) dc–dc converter. The converter operates in a quasi-resonant mode to provide the bidirectional current-mode regulation. We demonstrate an integrated circuit version of the "merged-interleaved" topology, first outlined in [16], due to its benefits in reducing total passive component volume. The design leverages the benefits of the ReSC approach in operating with high efficiency and high power density. Ultimately, the goal is to demonstrate a solution that is: 1) effective in balancing the state of charge of series-connected Li–ion cells at a power level that is common in automotive applications; 2) includes the additional diagnostic capabilities discussed above as a value add to the core power management functions; and c) uses high-level integration to suggest a roadmap toward true viability in highly cost-sensitive applications (automotive and grid energy storage).

II. Cell Balancing Architectures

As problems with mismatch and variation in series-connected batteries are well known, many cell balancing architectures have been proposed in the past decades. The most common cell equalization methods use resistive shunt circuits in parallel with each group of parallel-connected cells [17]. In practice, the shunt method is used to bleed charge from cells that have reached their rated peak capacity, allowing other cells in the series string to complete the charging process. However, while the resistive shunt method is relatively low cost, it is only effective in charge cycles, and dissipates power to provide equalization.

Other methods that use efficient dc–dc converters (here termed active balancing) are known [4]–[7]. Shown in Fig. 3, a range of architectures have been proposed. In the ladder architecture Fig. 3(a), an array of bidirectional dc–dc converters are configured in a ladder network in parallel with the string of cells. Typical dc–dc topologies for the individual converters have included conventional buck–boost [5], [18], [19], switched capacitor [4], or resonant switched capacitor [20]. The advantage of the ladder architecture is that it is scalable and can be implemented with a stacked configuration of low-voltage-rated stages. However, a disadvantage is that it must "shuffle" power up and down the series string in accordance with where that power is needed.

Fig. 3(b) shows an alternative termed the dc-bus architecture, [21]. Here, dc–dc converters interface from individual taps on the electrochemical string and can move power to and from the high-voltage dc bus. An advantage here is that the converters do not need to "shuffle" energy, instead they interface directly with the centralized bus; in principle this can reduce loss due to the current conduction in multiple stages. However, the dc-bus architecture requires a high voltage rating for all converters, or possibly an isolated (transformer-based) topology which can impact performance and increase complexity.

Fig. 3(c) shows a recently proposed architecture that leverages an auxiliary bus to transfer power among different taps in the electrochemical stack [6], [22]. In automotive applications, the 12-V-peripheral bus may be used as the auxiliary [6]. This architecture is attractive due to the simplified power-flow path, and also because it provides a link between the electrochemical stack and the 12-V lead-acid system. However, it requires an isolated (transformer-coupled) topology to manage the large common-mode differences between domains. This poses challenges such as the cost and weight of the transformer, additional control complexity such as the possible need to communicate across the isolation boundary, and large common-mode voltage differences of active devices at the cell and bus sides.

III. Converter Topology

As outlined in the previous section, the ladder architecture has a number of characteristics that make it favorable for

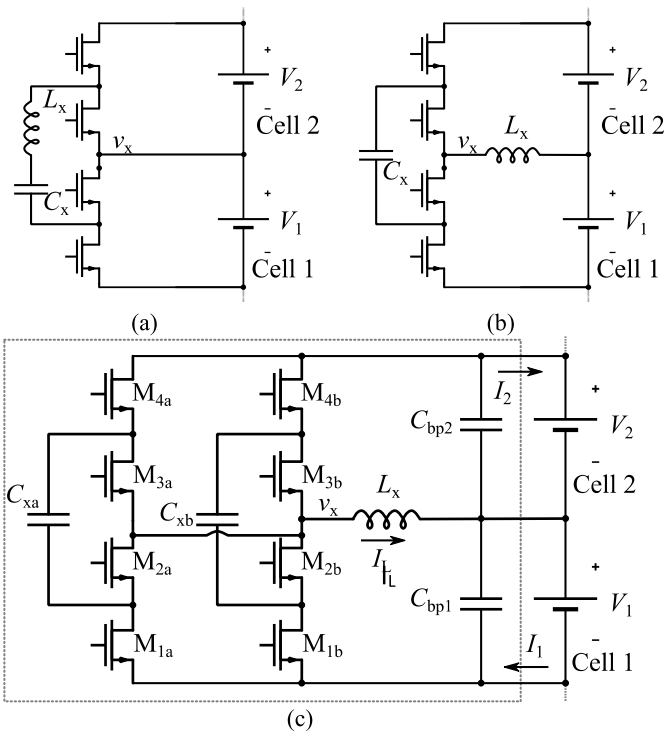

Fig. 4. Representative ReSC topologies and proposed. (a) ReSC: indirect conversion. (b) ReSC: direct conversion. (c) This work: merged two-phase interleaved direct converter.

a scalable integrated circuit implementation. This includes a uniform low-voltage rating for all active and passive devices, and that it does not require isolation and can be implemented with an array of cascaded converter stages.

A variety of converter topologies have been proposed for balancing applications as a basic building block in the ladder architecture. However, ReSC approaches have a number of advantages. Compared to pure switched-capacitor (SC) converters, e.g., [4], they can operate with higher efficiency as the inductive impedance can be used to shape the current waveform in a way that eliminates charge-sharing losses [23], [24]. They also provide capabilities to implement efficient voltage regulation as discussed in [25]. Compared to buck or boost converters, they can operate with much smaller inductance as the switched-capacitor stage effectively reduces the energy-storage requirements (volt-second product) needed in the inductor [26].

Past examples of ReSC converters used for balancing applications include [27] and [28], among others by the same authors. The basic converter schematic for these past works is shown in Fig. 4(a). Fig. 4(c) shows the topology that is chosen in this paper. This is an extension of the topology in Fig. 4(b), where two SC stages are "merged" to provide effective two-phase interleaving. Here, we borrow the "direct" and "indirect" conversion terminology from [16]. For example, in Fig. 4(a), the current waveform in the inductor is bidirectional. (In high-Q resonant operation, it approaches a sine wave.) In Fig. 4(b), the inductor current is unidirectional (full-wave rectified) and always flows toward the output, much like in a conventional buck converter. In fact, the direct topology may be appreciated by many readers as the same as the three-level buck converter, when used in non-resonant operating modes [29], [30]. The direct topology has certain advantages as compared to the indirect topology. As outlined in [16], with a unidirectional inductor current waveform, 80% of the spectral power is concentrated at dc. Thus, compared with the indirect topology, where (ideally) 100% of the power is the fundamental resonant frequency, high-frequency losses due to skin, proximity, and core loss effects are significantly reduced.

TABLE I

COMPARISON OF TOPOLOGIES BASED ON VOLTAGE RIPPLE, TOTAL CAPACITANCE, AND INDUCTOR VOLUME

FOM	Single phase	Conventional 2-phase	Merged 2-phase
$\Delta V \cdot C_T \cdot L_V$ (normalized)	1.0	0.4	0.2

The "merged-interleaved" topology was also discussed in [16] due to its potential to reduce total passive component volume. The converter can be constructed by noting symmetries in a conventional two-phase interleaved direct ReSC converter. Specifically, conventional two-phase interleaving would require two inductors and two flying capacitors. Assuming that flying capacitors operate with a median voltage of $V_{\text{in}}/2$, then it would be seen at the switching node V_x for either stage, that the voltage trajectory would be the same regardless of whether C_x was connected between $V_{\text{in}} - V_x$ or $V_x - \text{gnd}$. Thus, if the switching nodes are connected together, there are neither any charge-sharing losses nor asymmetries in the nominal two-phase operation. The insight in [16] was that these two stages could be merged into a single SC stage which is interleaved by 180° and coupled to a single inductor, L_x between the switching node V_x and output terminal V_{out}.

A comparison of resonant loops in the merged-interleaved and single-phase topology is shown in Fig. 5. In the single-phase topology, it can be seen that the current waveform only links the output (ground-referenced) bypass capacitor in one phase each switching cycle. However, the merged-interleaved current splits equally between the two bypass capacitors, linking the output bypass capacitor in each switching phase. Thus, it accomplishes effective two-phase interleaving and reduces the voltage ripple at the output (by $\sim 5\times$) for a common switching frequency and capacitance allocation, [31].

Next, in the merged-interleaved topology, the flying capacitors (or total loop capacitance containing the bypass capacitance) are effectively in parallel. Therefore, compared to a conventional two-phase interleaved approach, the equivalent capacitance seen by the inductor is doubled. Thus, to achieve the same (resonant) frequency, the inductance can be halved. Assuming a simplified scaling model for an air-core solenoid inductor [32], it can be shown that the inductor volume can also be reduced by 1/2 while maintaining the same total loss due to the effective series resistance (ESR). Thus, as shown in Table I, a simplified comparison can be made that relates the voltage ripple ΔV total bypass capacitance, $C_T = C_{\text{bp1}} + C_{\text{bp2}}$, and total inductor volume, L_V. This figure of merit assumes operation at the same resonant frequency for all topologies, and the same total ESR in the inductor component. The total capacitance can be reflected in terms of volume or area through

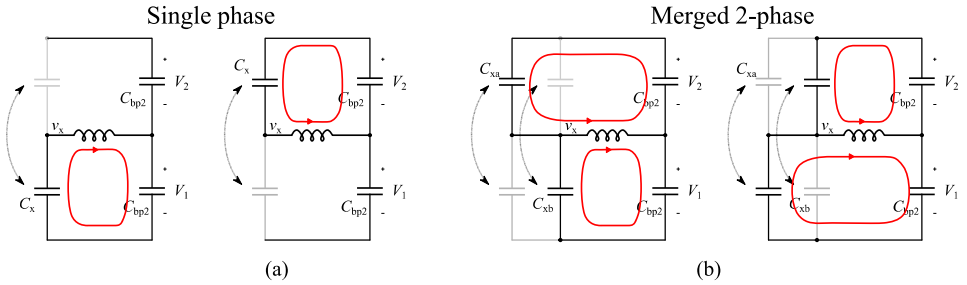

Fig. 5. Comparison of the resonant loops in (a) single-phase direct ReSC and (b) merged two-phase interleaved topology.

knowledge of the capacitance density of a given technology. Ultimately, the benefit of the merged-interleaved topology is significant in terms of the passive component utilization, thus reducing the size and the cost.

IV. Control and Regulation

In certain battery chemistries, notably lead acid, voltage equalization has been shown to be an effective and simple method to equalize state-of-charge [4], [17]. However, in most lithium-based battery technologies, uniform voltage equalization may be insufficient for true SOC equalization [2], [8]. This is because variations in series resistance can result in unequal charge distribution even when (instantaneous) measurable cell voltages are equal. Therefore, in most Li–ion battery systems, the BMS must support some form of accurate variable regulation to move power in accordance with the capacity rather than the instantaneous cell potential. To accomplish bidirectional current regulation, we used properties of ReSC converters originally detailed in [25]. Note that these converters can be operated with a conversion ratio around the nominal 1:1 level but inserting a "buck" or "boost" mode in sequence with nominal resonant switching cycles. The result of this process is that the converter will operate in a quasi-resonant mode which is a mixture of resonant transitions and hard-switching (inductive) transitions. The following sections detail the specifics of the control process for the merged-interleaved converter design.

A. Bidirectional Quasi-Resonant Regulation

Fig. 6 shows a representation of the merged-interleaved converter operating in a buck-like quasi-resonant mode. Here, the switching period is segmented into four sequential switching states, A–C–B–C, and the respective current flow paths and inductor current waveform is shown for each state. State-A provides a nominal resonant transition, where energy is transferred from the flying capacitors (which have a median voltage of $V_{\text{in}}/2$). State-C is a hard-switching transition where the inductor is directly connected to gnd. State-B is the complementary resonant switching state where energy is sourced again from flying capacitors, but the polarity of current through the flying capacitors is reversed to maintain the net charge balance. State-C proceeds each of states A and B in order to maintain symmetry in the overall operation.

From the waveforms in Fig. 6, it can be appreciated that the "buck" switching state effectively reduces the average voltage on the switching node V_x. For a resistive load network, this would drive a decrease in the average output voltage.

Fig. 7 represents the opposite scenario: boost-mode operation. Here, in between resonant transitions, the inductor is connected to V_{in} (the sum of the series-connected battery voltages). Thus, it can be appreciated that the "boost" state effectively increases the average voltage of the switching node V_x. Again, for a resistive load network, this would increase the average output voltage.

In practical applications, it is important to note that the load comprises two battery cells in series. In this case, the load impedance is in fact very low and the main impact of adjusting the average voltage $\bar{V}_x$ is that it will drive current either positively or negatively in the direction of the common cell junction. Thus, several scenarios are possible, depending on the conversion ratio $k = \bar{V}_x/V_2$ and the actual ratio of cell voltages: V_1/V_2. For example, if $\bar{V}_x = V_1$, it can be appreciated that no current will flow $I_1 = I_2 = 0$, where I_1 and I_2 are the currents flowing in cells 1 and 2, respectively.[1] However, through adjusting the ratio k an arbitrary load current can be forced to flow regardless of the actual cell voltages or their ratios. Alternately phrased, if the switching process adjusts k (through the relative time durations of states A–C, B–C or A–D, B–D) such that the average switching node voltage $\bar{V}_x < V_1$ then the average inductor current $\bar{I}_L$ will be negative; in the complementary scenario, if $\bar{V}_x > V_1$ the inductor current will be positive (flowing toward the cell junction). Thus, the buck and boost modes can be used to implement a form of bidirectional current-mode regulation that can be maintained regardless of the actual state of the cell voltages or their ratio V_1/V_2.

To implement bidirectional current-mode regulation, a true four-quadrant control scheme is needed. This is to support balancing currents that are independent of the actual voltage levels of the series-connected cells. For example, it enables the possibility of either positive or negative current flow for V_1/V_2 ratios above or below unity. As will be discussed in the following, this feature is also necessary to support sinusoidal perturbations used to extract cell impedance regardless of the state of the cells.

Fig. 8 shows an example of the bidirectional current waveforms in the inductor when operating in buck or boost modes. It also shows a block diagram of the control system implemented on chip to regulate the dc current levels. Here, the regulated parameter is I_1, the balancing current flowing

[1]Note that in this discussion we are referencing the voltage V_x to the negative plate of cell 1; hence when $V_x = V_1$ it can be appreciated that there is no voltage across the inductor.

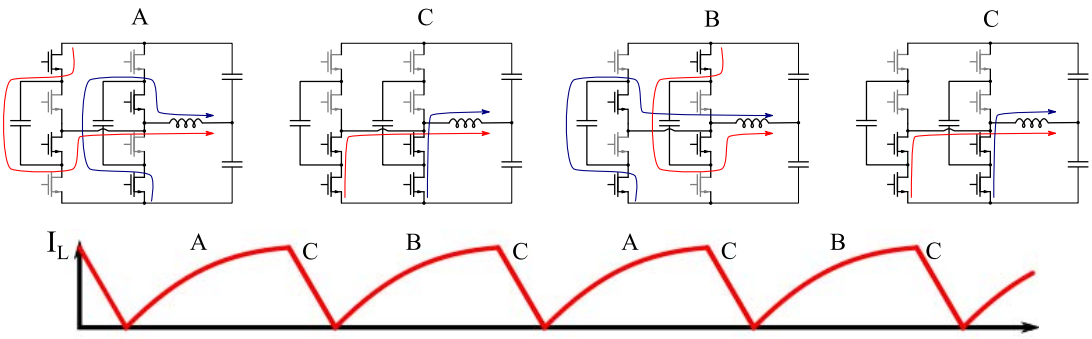

Fig. 6. Quasi-resonant operation for variable regulation: buck mode.

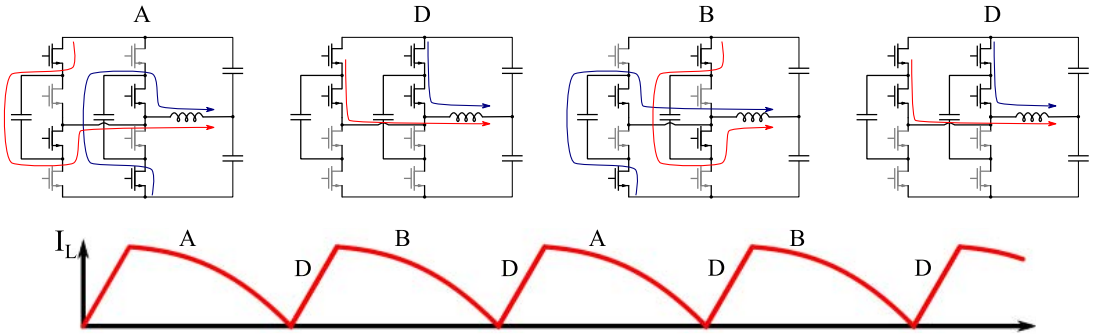

Fig. 7. Quasi-resonant operation for variable regulation: boost mode.

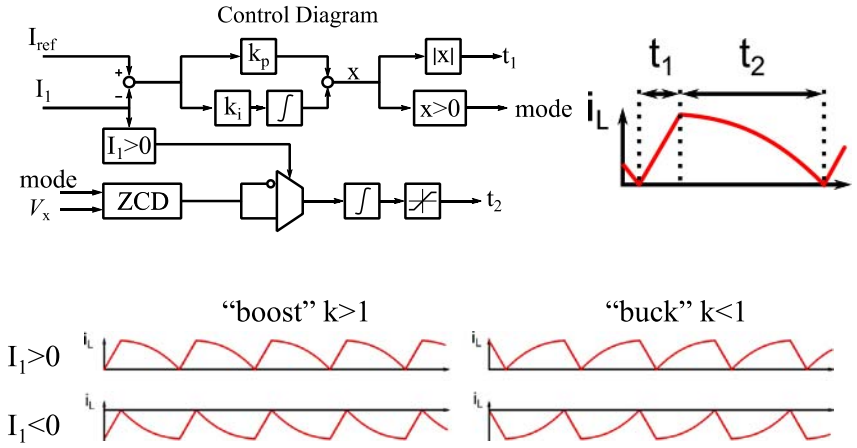

Fig. 8. Control block diagram, key control variables, and examples of four-quadrant inductor current waveforms.

in cell 1. Regulated current-mode control is implemented in a digital control scheme that sets the duration of the hard-switching state t_1. The time duration of the resonant state (A or B) is controlled through a zero-current detection scheme and nested integral regulation which enforces the zero-current switching process. A digitized measurement of the actual dc current I_1, flowing through cell 1, is compared to a reference command and processed by a P-I control loop. A mode-detection circuit determines in which quadrant the circuit is operating to adjust the timing and detection threshold for the zero-current detection circuit.

The sign of t_1 defines the operating mode ($k > 1$ or $k < 1$) while the absolute value defines the length of the period, which allows the controller to seamlessly transition between both operating modes. This way, the whole current range from -1 to $+1$ A can be covered. For low currents the controller automatically switches to a continuous conduction mode by saturating the time t_2 at a lower limit. This prevented the converter from switching at arbitrarily high frequencies at low currents. While in principle, a burst mode or dynamic off-time mode (e.g., [33]) could have been used for the light-load transition, the extra complexity was not needed in this application.

B. Zero-Current Detection

Zero-current detection is achieved by sampling the switching node during the dead-time interval at the end of a relevant switching state. As can be appreciated from Fig. 8, the exact switching state during which the current returns to zero depends on the operating quadrant. Additionally, the signature

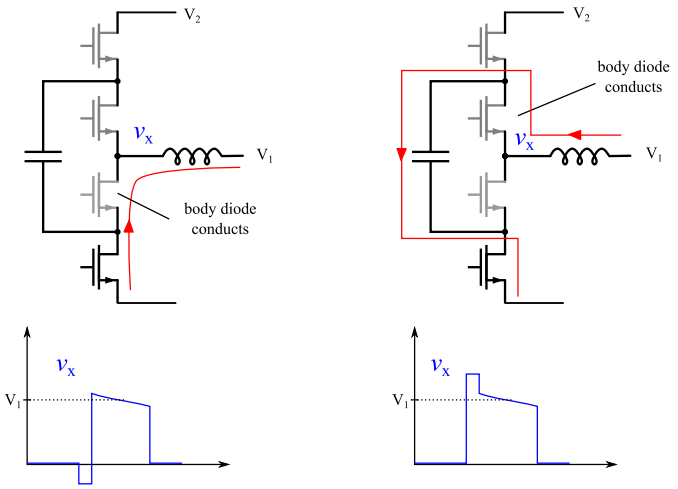

Fig. 9. Zero-current switching signature: buck mode with positive or negative residual current.

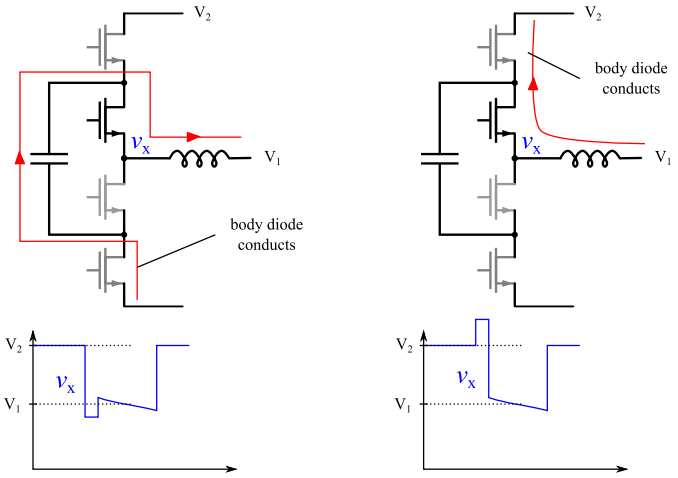

Fig. 10. Zero-current switching signature: boost mode with positive or negative residual current.

that would identify non-zero current switching is dependent on the load current. Thus, the exact operating mode is needed in order to determine the appropriate time interval to detect the zero-current transition and the reference that would indicate the zero current switching (ZCS) state.

Fig. 9 shows the ZCS scenario for buck mode with positive or negative residual current in the inductor. Fig. 10 shows the same scenarios for a converter in boost mode. In either scenario, it can be appreciated that with non-zero current, the switching node will be charged or discharged, ultimately resulting in body diode conduction of some transistor(s) in the power train. The difference between positive current and negative current is that the switching node will decrease or increase, respectively, in the dead-time interval. Thus, zero-current detection can be implemented in a simple fashion by using a sampled comparator that is clocked at an appropriate time during the dead-time interval, as shown in Fig. 11. To facilitate zero-current detection in both boost and buck modes, the comparator used a multiplexor to select the appropriate reference: $V_{\text{ref}} > (V_1 + V_2)/2$ for boost mode, and $V_{\text{ref}} < (V_1 + V_2)/2$ for buck mode.

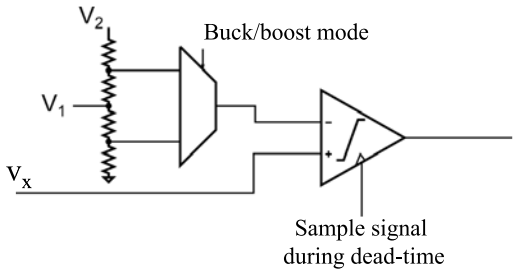

Fig. 11. ZCD sampled comparator with multiplexed reference: for boost mode, reference is > (V1 + V2)/2 for buck mode, reference is < (V1 + V2)/2.

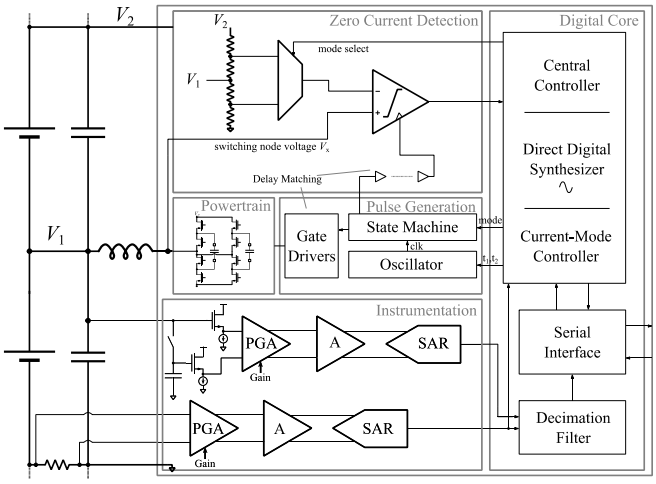

Fig. 12. System block diagram.

A secondary benefit of the zero current detection (ZCD) regulation scheme is that in closed loop, it regulates the state of the switching node voltage V_x to the respective reference threshold: in boost mode, roughly the midpoint between V_1 and V_2; in buck mode, roughly $V_1/2$. Thus, while Figs. 9 and 10 show a diode conduction interval, in practice, diode conduction is unlikely to occur. Instead, the switching node is either charged or discharged by any residual inductor current such that it is maintained near the respective ZCD reference. While this does not provide true zero-voltage switching (ZVS), it does allow partial soft charging of V_x thus reducing switching losses. A similar ZVS scheme was used and discussed in [38].

V. Converter Implementation

The converter was implemented in a 180-nm bulk-CMOS process. All power-train devices, M_{1-4} in Fig. 4(c), were implemented with 5-V lateral nMOS devices. All of the control, instrumentation, and timing blocks used nominal 1.8-V CMOS devices. Fig. 12 shows a block diagram of the IC. Included on chip were the power train, gate drivers and level shifter, timing and synchronization circuitry, voltage and current instrumentation. The instrumentation blocks (discussed in the following) used 10-bit capacitive successive approximation register (SAR) ADCs to digitize the voltage and current signals for use in impedance extraction and digital current-mode

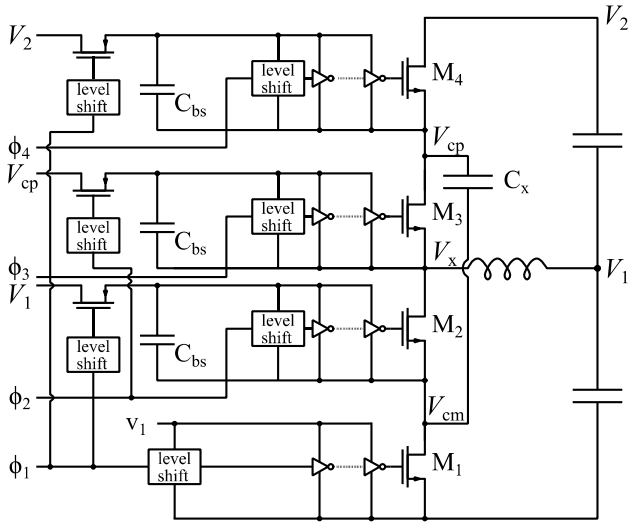

Fig. 13. Gate-drive scheme for a symmetric half of the converter in Fig. 4(c).

control. The digital blocks on the chip included both the control scheme for the converter, and also a direct digital synthesis block which created sinusoidal perturbations of the reference command for the current waveform. A decimation filter was used to process, normalize, and condition the instrumentation data to be transferred off-chip for impedance extraction. The dominant passive components including flying and bypass capacitance and the inductor were included off-chip. The only other off-chip component was a sense resistor, placed in series with the low-side current-return path.

A. Gate-Drive, Level-Shift, and Timing

As the power train used all nMOS devices, the gate-drive scheme used bootstrapping to ensure an effective and uniform drive strength for all power devices. Fig. 13 shows a schematic of the gate-drive architecture for one half of the merged-interleaved power train. As each of devices M_2–M_4 was floating with respect to its source terminal, it required a source-referenced drive circuit and a bootstrap capacitor. As M_1 is ground referenced, it does not require bootstrapping, but was driven with the same circuitry as the other devices to maintain symmetry.

The bootstrapping process for the power train was implemented as follows. Device M_2 was bootstrapped from node V_1. To charge the bootstrap capacitor, a pMOS device was turned on, synchronous with the gate signal for device M_1. Device M_3 was bootstrapped directly from the flying capacitor, C_x and its bootstrap capacitor was charged synchronously with the gate signal for M_2. Device M_4 was bootstrapped from node V_2 and its bootstrap capacitor was charged synchronously with the gate signal for M_1. The bootstrap capacitors were of value ~800 pF in order to support the gate charge of the 5-V power-train devices. The metal–insulator–metal capacitors used for bootstrapping had density of 6.6 nF/mm^2 such that the area per capacitor was roughly 0.12 mm^2.

Level shifters were used to interface between the low-voltage (1.8 V) domain and the high-voltage domain. In a worst case, assuming each battery cell was at ~4 V, the gate of M_4 would need to be driven to ~12 V, so sufficient compliance was required. The level shifter used for each power device is shown in Fig. 14. A linear (non-latching) level shifter was used to ensure uniform latency of the switching signals, independent of the common mode. Variation in latency through the level shifter can be a major problem as it impacts the duration of dead times and other key signals after they are generated in the low-voltage domain by the digital blocks. The level shifter works by coupling a differential current that is generated by two high-voltage (15-V LDMOS) devices M_{xa} and M_{xb} to a floating, diode-connected pair of 5-V lateral pMOS devices at nodes V_a and V_b. This differential voltage signal is amplified by a 4T-OTA to provide a single-ended drive voltage for the floating inverter chain that drives the nMOS power device.

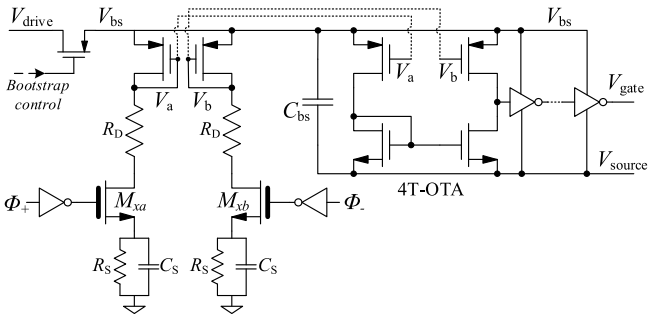

Fig. 14. Level-shift schematic and boostrapped gate drivers.

As this structure consumes dc power (in either state, one of M_{xa} or M_{xb} is on, and thus sinks current from the $V_{\rm bs}$ terminal), degeneration resistors R_s are used to limit this current flow to a known level. To reduce power consumption without incurring a reduction in switching latency, source-coupled capacitive degeneration C_s is used. During a change in state of the low voltage differential signals Φ_+ and Φ_-, an initial current spike passes through C_s and initiates rapid switching of the $V_{\rm gate}$ signal. However, when C_s is fully charged, the residual dc current is limited by R_s. An extra, drain-coupled resistor R_d is used to limit the peak current during the initial switching phase, and also filters out any unwanted high-frequency coupling through the gate–drain capacitance of M_{xa} and M_{xb}.

B. Signal Instrumentation

The IC also included signal instrumentation and data conversion of both voltage and current. Digitized current instrumentation was needed for the current-mode digital controller. As will be discussed in the following section, both voltage and current measurements were needed to determine the cell impedance.

The current instrumentation circuit is shown in Fig. 15. As the regulation parameter for the controller was the current I_1 flowing through cell 1, a suitable location for a sense resistor is in series with the low-side current-return path that links cell 1. This scheme avoids inserting a sense resistor in series with the main power-flow path through the cells: this would lead to a significant increase in power loss in a scaled

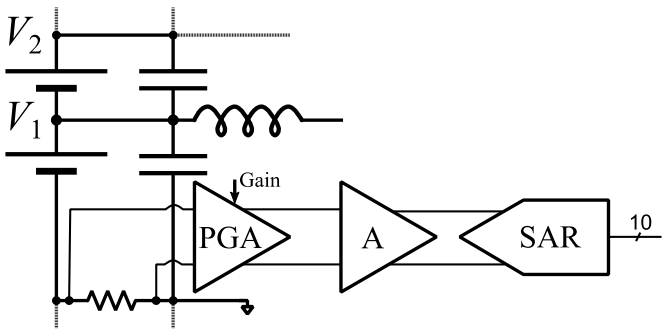

Fig. 15. Current instrumentation and data conversion.

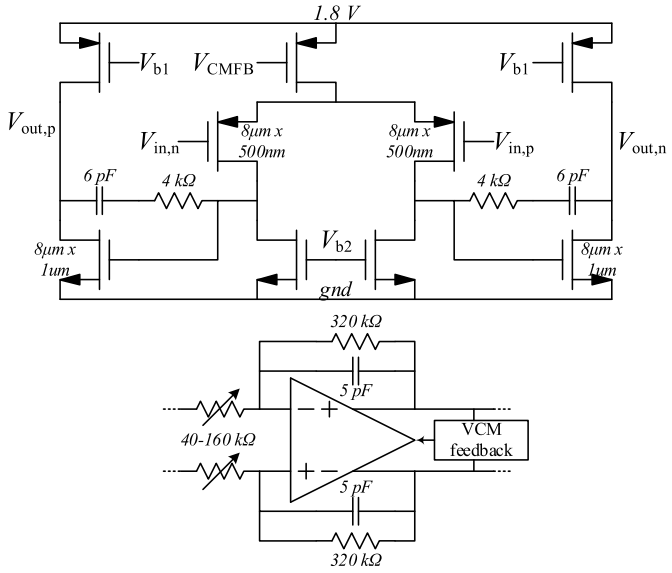

Fig. 16. Schematic of amplifier stages used in instrumentation chain.

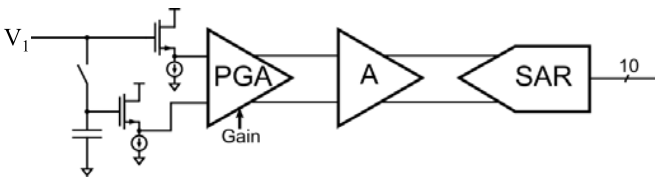

Fig. 17. Voltage instrumentation and data conversion.

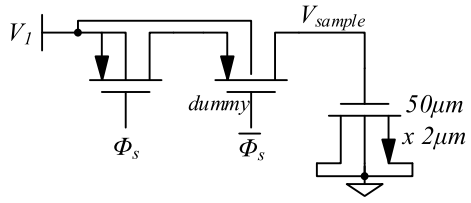

Fig. 18. Sampling switch in Fig. 17.

up solution. The sense resistor is also located on the battery side of the bypass capacitor to provide significant filtering of the current waveform. This was also important for EIS measurements since the impedance of the bypass capacitor can be low enough to affect the measurement at high frequencies.

The gain stage comprised a chain of differential amplifiers, each with the schematic shown in Fig. 16. The instrumentation amplifiers were implemented with a two-stage fully differential topology. A pMOS input stage was used to support the low common-mode input of the sense resistor voltage. The amplifiers were configured with a resistive feedback network to provide a gain of between 16 and 64 for the full analog chain. A variable gain stage was used to adjust the gain in binary intervals: 16, 32, and 64 to adjust the dynamic range of the signal for the ADC. Programmable gain was achieved by configuring the resistive feedback network in the fully differential topology. It should be noted that while the gain stage was designed for low offset, a secondary offset calibration procedure was used in the digital domain to reduce any residual dc offset. This was accomplished by setting the dc–dc power train to high impedance (no current flow) and measuring the residual output of the current sense instrumentation chain including amplifiers and data conversion. The corresponding digital code was sampled for 16 cycles, averaged, and stored as the zero-current level and used as the reference for current measurements going forward. In principle this can reduce offset to within the quantization (or noise) resolution of the ADC, but does require periodic updating to adjust for drift.

Two SAR ADCs were designed and included on chip. The fully differential SAR ADC provided a 10-bit quantization and used a capacitive redistribution architecture. The ADCs were sampled at 100 kS/s to provide sufficient oversampling of frequency content for both the feedback control system and the fastest spectroscopic perturbation signals. As the instrumentation chain was needed for both feedback regulation and measuring small perturbations applied to the cell voltage and current, the filtering process required careful consideration. The gain stages provided 2nd-order lowpass filtering to prevent aliasing of high-frequency noise in particular, the switching noise from the power train of the dc–dc converter.

As shown in Fig. 16, each of the gain stages included a lowpass filter with a ∼50 kHz corner frequency. This provided two poles at the Nyquist sampling frequency of the ADC to sufficiently attenuate unwanted spectral content. While a more aggressive filtering scheme could have been used, or a lower cutoff frequency to more effectively reduce aliased spectral content, a primary tradeoff was the impact of the antialias filter on the measured amplitude and phase of the impedance spectroscopy waveforms. For example, any differential phase shift in the voltage and current instrumentation paths results in an error in the spectroscopic measurement. However, it should be noted that because the current and voltage signals both propagate through identical instrumentation chains, it is only the mismatch in the corner frequencies of these filters that impact the eventual impedance measurement. For example, it was calculated that 10% variation in the relative corner frequency resulted in less than 2° of phase error at 10 kHz.

Fig. 17 shows the architecture for the voltage instrumentation circuit. In this paper, voltage instrumentation was primarily used to measure the value of a small signal perturbation (discussed further in the following section). To separate the small signal perturbation from the dc voltage of the cell V_1 we used a sampling method to implement ac coupling. The sampling method was used to enable measuring perturbation

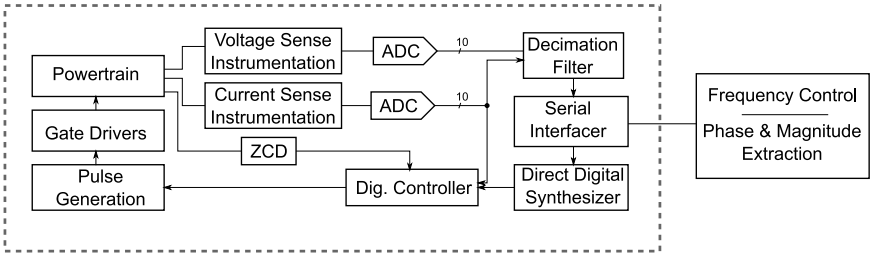

Fig. 19. Block diagram of EIS system.

signals well below 1 Hz; if a simple ac-coupling method were used, this would have required prohibitive values for the ac-coupling capacitance.

The sampling circuit is shown in Fig. 18. A sampling switch, consisting of a 5-V pMOS device operates in a track and hold mode for voltage V_1 passing the voltage to a MOS capacitor. When signal Φ_s goes high, the voltage V_{sample} is held in its current state. A dummy element operates on the opposite phase of Φ_s to cancel the residual charge injection. Note that the body terminals of the sampling switch and dummy device are connected to V_1. Because the perturbation magnitude is small, it was hypothesized that there would be only very small voltage applied across the body diode during a perturbation, and thus very low leakage through the diode. However, in the final circuit, it was realized that an asymmetry in leakage through the body diode led to drift of the sampled voltage. This ultimately limited the perturbation frequency to a limit at around 1 Hz. This design issue will be discussed in Section VI.

C. Spectroscopic Perturbation

To implement real-time spectroscopic diagnostic capabilities in the integrated converter, we leveraged the bidirectional regulation functions of the control system, and synthesized a digital perturbation controller and back-end signal processing circuitry. Fig. 19 shows the block diagram of the digital capabilities of the IC. The spectroscopic perturbation was generated on chip through a direct digital synthesizer. A sinusoidal perturbation was synthesized using a modified Sunderland algorithm [34]. The implementation used a 9-bit quarter-period phase register, and a 10-bit signal magnitude. While an uncompressed quarter-period sine wave would result in a $2^9 \times 9 = 4608$ bit lookup table, the algorithm here used only one $2^6 \times 9 = 576$ bit lookup table and one $2^6 \times 4 = 256$ bit lookup table. This gave a quarter-period compression ratio of 5.54:1, and a full period compression of 22.2:1.

To facilitate off-chip processing for phase and magnitude extraction, the measured voltage and current information was filtered and decimated to a common sampling rate. Here, we used a cascaded integrator-comb (CIC) filter to process the measured voltage and current data and provide a normalized sampling rate. This process was useful because in practice, the spectroscopic perturbation covers a wide bandwidth; very low-frequency perturbations, for example, would be significantly oversampled compared to high-frequency perturbations. The CIC decimation filter helped to reduce on-chip storage and streamline the data transfer process through the serial interface circuitry, making it more direct to handoff to off-chip processing circuitry.

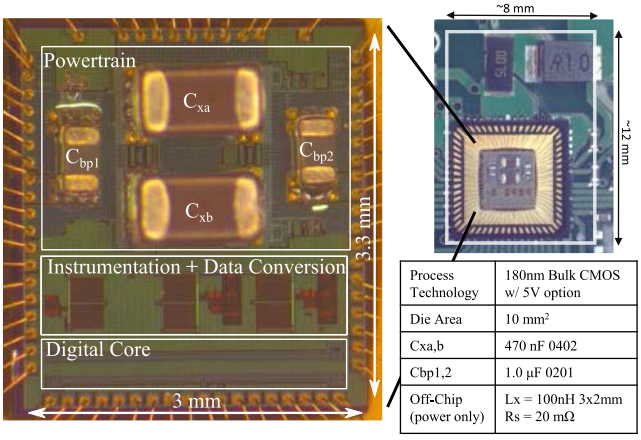

Fig. 20. Die photograph and implementation details.

Ultimately, the spectroscopic perturbation functionality was initiated by an off-chip interface to a field-programmable gate array (FPGA). For example, the FPGA was used to set the converter into perturbation mode and sweep the frequency command across a range of spectrum. However, the IC performed all timing, synchronization, perturbation, instrumentation, and data processing. The main functions of the FPGA were, therefore, to provide a reference clock signal, set the operating mode, and receive the decimated data for magnitude and phase extraction.

VI. IC Implementation

Fig. 20 shows the die photograph and details of the assembly. The chip was designed in a 180-nm bulk-CMOS process with a 5-V option for power devices. The total die area was 10 mm^2, including the padring. The off-chip components that were used included two 0402 ceramic flying capacitors with a rated value of 470 nF, and two (0201) bypass capacitors with a rated value of 1 μF. The capacitors were attached directly to the die using a gold-stud solder reflow process, as in [33]. This helped to reduce the total form factor and also the parasitic inductance in series with the flying capacitor loops. The other off-chip components shown in Fig. 20 are the inductor and sense resistor. The inductor was of value 100 nH (TDK NLCV32T-R10M) with dimensions 3 mm $\times$ 2 mm. The value of the sense resistor was 20 mΩ. Total board area for the solution was 8 mm $\times$ 12 mm or roughly 1 cm^2.

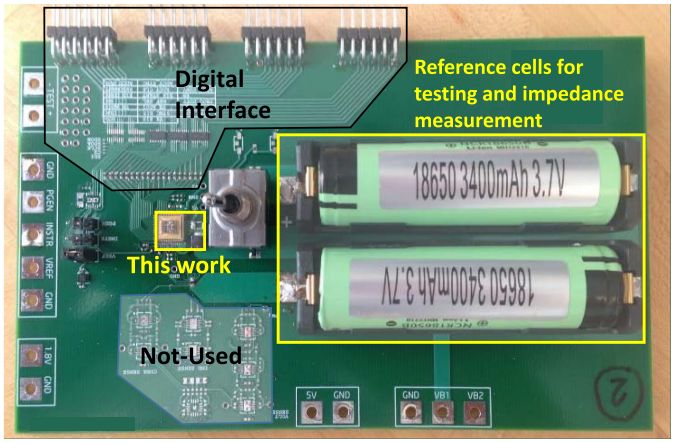

Fig. 21. Photograph of the test assembly showing the converter in Fig. 20, the circuitry used to interface to the FPGA, and 18650 Li–ion cells.

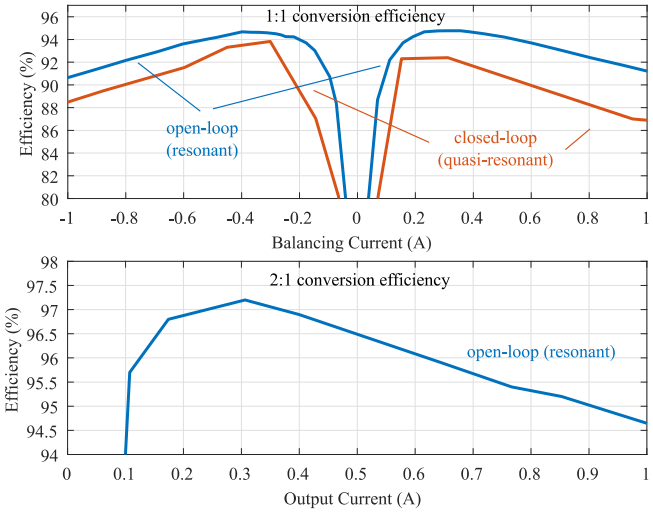

Fig. 22. Measured efficiency of the converter in 1:1 (balancing mode) and 2:1 (power delivery mode).

VII. Experimental Results

Fig. 21 shows the circuit board used for the test assembly. This board included the converter in Fig. 20, a digital interface to the FPGA, and two series-connected 18650 lithium-ion cells used for benchmarking and validation. The 3400 mAh off-the-shelf lithium-ion battery cells are similar to those used in automotive and grid storage applications, and thus provide a representative load for a single stage of a ladder converter in Fig. 3(a). It should be noted that while here we are designing and testing a single dc–dc stage, the solution is scalable for larger arrays, much like the design presented in [27]. The differences that would be required in a scaled up ladder converter would relate to the control scheme: here we are regulating the current delivered to cell 1, whereas in a full ladder implementation the control must regulate many cells in series. A treatment for the multiple-input, multiple-output control scheme for a similar case is presented in [35]. It is also the case that the converter is only performing impedance spectroscopy on cell 1 (referring to Fig. 4). While it would be possible for a single stage to also measure V_2 and I_2, and the impedance Z_2 of cell 2, in principle this would be left to the adjacent converter in the stack. This scheme is fully scalable for large arrays of cells, with the caveat that the final (highest voltage) cell in the stack would need its own instrumentation chain to measure both cell 1 and cell 2. A scheme where both cells are instrumented is probably desirable in a realistic setting and the additional data conversion is not seen as a major addition to the work presented here.

Here, we are primarily focused on the efficiency of the single dc–dc converter stage, its regulation capability, and perturbation functions that can be used to extract cell impedance. Measured efficiency of the converter is shown in Fig. 22. Efficiency measurements were taken with power supplies and an electronic load to bias the voltages of the respective stages to nominal 3.7 V level, such that a 1-A load current corresponds to roughly 3.7-W power.

In 1:1 open-loop resonant operation, the converter achieves a peak efficiency of 94.8% at ±0.35 A, and maintains above 91% up to ±1 A. In closed-loop quasi-resonant operation

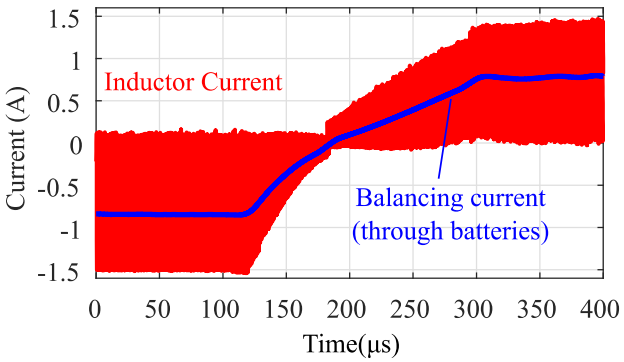

Fig. 23. Transient step on current reference: dynamic response of inductor current and balancing current through the batteries.

when current is regulated to a digitally programmed reference, the peak efficiency is 93.8% at ±0.35 A of balancing current and remains above 87% for ±1 A. For better comparison with power delivery literature, the 2:1 conversion efficiency was also tested in resonant mode, where the converter achieves a peak efficiency of 97.2% at 0.3 A and above 94.5% at 1 A load current. Here, it may be noted that it is common for 2:1 power delivery mode to have higher efficiency than 1:1 balancing as the rms current in the switching stages is lower in 2:1 mode due to the step-down transformation process.

Functionality of the digital current-mode controller was tested by applying a step to the digitally programmable reference. Fig. 23 shows a reference step from −0.8 to +0.8 A of balancing current. Both the inductor current and the balancing current are plotted. The waveforms show that the controller can smoothly transition from negative to positive current while maintaining zero-current switching in the inductor through most of the range, except around zero current, where the converter enters continuous conduction mode operation.

Fig. 24 offers a closer look at the inductor current waveforms in resonant and quasi-resonant operation along with output voltage ripple. Voltage ripple is approximately 60 mV

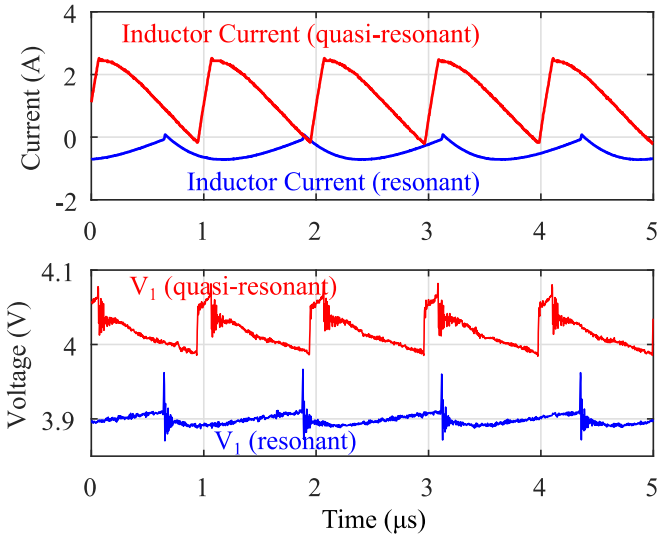

Fig. 24. Closer inspection of inductor current and output voltage (V_1) during resonant and quasi-resonant operation.

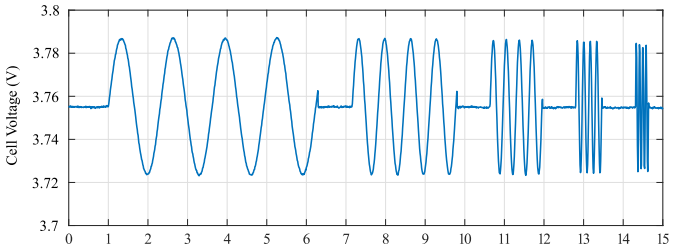

Fig. 25. Cell voltage (measured on an oscilloscope) during an EIS sweep.

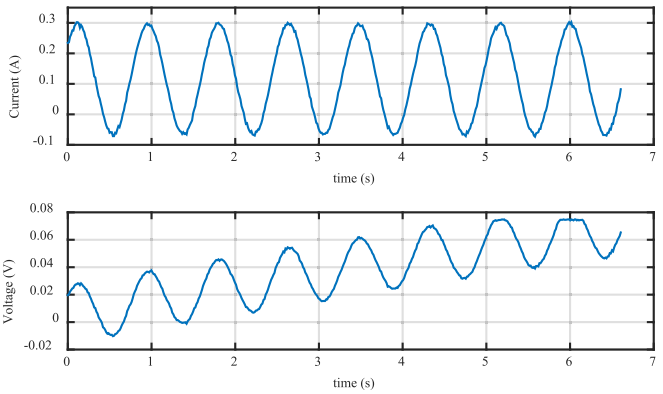

Fig. 26. Example raw data provided from current and voltage instrumentation during a frequency perturbation at 1.2 Hz.

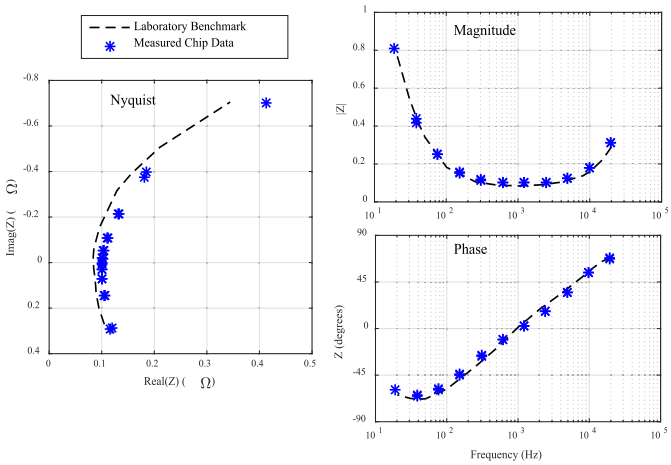

Fig. 27. Measured impedance data from the chip compared to a calibrated laboratory benchmark, frequency spans 15 Hz to 20 kHz.

in quasi-resonant operation, this can be achieved with fairly small bypass capacitance of 1 μF due to the benefits of merged interleaving. Here, it can be seen that the zero-current state is regulated in both cases. The slight offset from zero current at the switching interval is because the ZCD circuit will use a slightly non-zero inductor current to precharge the switching node voltage in the dead-time interval (partial zero-voltage switching).

Note that the current waveforms in Fig. 24 show two quadrants of operation: in resonant operation the inductor current is slightly negative. This is simply because the state of the cells in open loop is such that V_1 is slightly higher than V_2 in the test case. In quasi-resonant operation, the converter is in fact forcing current to flow out of cell 2 and into cell 1 despite this mismatch in cell potential. Thus, it demonstrates the capability to move current regardless of the actual state of the cell potentials.

Based on the ability of the current-mode controller to enforce arbitrary currents through the battery cells, the converter was used to perturb the cells with sinusoidal currents at various frequencies and measure the response with on-chip instrumentation. Fig. 25 shows the battery voltage during an EIS sweep. A chirp-like current is injected in the battery: here, five cycles of sinusoidal current perturbation are injected at incrementally higher frequency. To achieve a logarithmic spacing of frequency vectors, the converter uses a simple binary (octave) increment. The actual signal used for EIS measurements used eight full sinusoidal cycles to improve accuracy. While a longer interval (more cycles) would provide higher accuracy, at low frequencies it would also require more time to complete a full perturbation. Thus, eight cycles was chosen as a tradeoff between time and accuracy.

Frequencies as high as 10 kHz and as low as 1 Hz were tested. While the converter is able to perform perturbation at lower frequencies as well, the voltage response cannot be measured below 1 Hz due to the limitation of the ac-coupling method. Leakage through the sampling switch causes the sampled dc battery voltage reference to drift over time until the amplifiers saturate. An example of a raw data set is shown in Fig. 26 for a perturbation frequency of 1.2 Hz. Here, it can be seen that while the current measurement is stable, the voltage measurement drifts over time. This is because of the asymmetric leakage through the body diode of the sampling switch in Fig. 18. This is not a limitation of the method itself but rather of the specific switch implementation. A different configuration of the sampling switch (e.g., back to back switches with the body diodes connected in the middle, a lower leakage switch, or larger sampling capacitor) could extend the useful EIS frequency range into the MHz range.

TABLE II
COMPARISON TO PAST WORK

	[6]	[36]	[7]	[37]	[27]	**This work**
Topology	Dual Active Bridge (isolated)	Buck/boost (nonisolated)	Buck/boost (nonisolated)	SC (nonisolated)	ReSC (nonisolated)	Quasi-resonant SC (nonisolated)
Feedback Control	Yes	Yes	Yes	No	No	Yes
Inductance	260 µH*	800 nH	10 µH	-	50 nH (6x6mm)	100 nH (3x2mm)
Flying cap.	-	-	-	6 x 4.3 µF 6 x 1.0 µF	8 x 1.0 µF (0805)	2x 470 nF (0402)
Bypass cap.	400 µF	NR	4 x 4.7 µF	6 x 4.3 µF	16 x 4.7µF (1206)	2 x 1 µF (0201)
Converter Area	NR	NR	~5 cm^2	~0.8 cm^2	~10 cm^2	~0.96 cm^2
Peak Eff.	93 %	89 %*	95.7%*	95%*	96.3 %	94.8 %
Max current	10 A	±1.5 A	±1 A	±1 A	±4 A	±1 A
Notes	Discrete implementation; *transformer primary	Discrete passive components *Efficiency reported in 2:1 mode			discrete power train & passive components	Die attach caps, discrete inductor

In order to verify the accuracy of the on-chip instrumentation in converter with the converter as a perturbation source, a reference impedance was measured and compared to measured data from a calibrated impedance analyzer. Fig. 27 shows a plot of the resulting magnitude and phase of the chip data compared to the benchmark, as well as a plot showing the inverted Nyquist representation. The Nyquist plot shows roughly the higher-frequency portion of a typical EIS signature (e.g., Fig. 1). Unfortunately, due to the leakage in the ac-coupling circuit, lower frequency measurements (below around 1 Hz) were not possible with the IC prototype. However, at high frequency, it can be seen that the chip data is in good agreement with the calibrated laboratory measurement.

Table II shows a comparison to the past work. Included in the comparison are designs that provide 1:1 balancing operation for both battery and photovoltaic applications, as well as designs that were used for power delivery with a nominal 2:1 conversion ratio. Compared to previous designs, this work was able to operate with a much smaller inductor (in terms of inductance and component volume), and smaller flying and bypass capacitors. However, the design achieves high efficiency despite the small form factor. This is also the first ReSC IC to provide full closed-loop regulation and the first integrated circuit demonstration of spectroscopic diagnostic capabilities embedded in a BMS.

VIII. CONCLUSION

This paper presented a small form factor dc–dc converter used for bidirectional balancing in series-connected lithium-ion battery strings. The topology used merged multi-phase interleaving to reduce passive component volume substantially compared to conventional single and two-phase interleaved designs. A method for implementing 4-quadrant bidirectional current-mode regulation was discussed, and details of supporting circuitry including zero-current detection and regulation were provided. The IC was implemented in a 180-nm bulk-CMOS process with a 5-V option for power devices to support the range of lithium-ion cell potentials. The chip also included a significant digital portion to support spectroscopic diagnostics on cell impedance. While the instrumentation circuitry was limited to frequencies above ∼1 Hz due to a leakage issue in a sample and hold block, experimental results showed effective impedance measurements from ∼15 Hz to 20 kHz. The dc–dc converter was able to operate with up to 94.8% conversion efficiency in 1:1 balancing mode, and 97.2% efficiency in 2:1 step-down mode.

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