

# An 80-mV<sub>pp</sub> Linear-Input Range, 1.6-GΩ Input Impedance, Low-Power Chopper Amplifier for Closed-Loop Neural Recording That Is Tolerant to 650-mV<sub>pp</sub> Common-Mode Interference

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**Abstract**—Closed-loop neuromodulation is essential for the advance of neuroscience and for administering therapy in patients suffering from drug-resistant neurological conditions. Neural stimulation generates large differential and common-mode (CM) artifacts at the recording sites, which easily saturate traditional recording front ends. This paper presents a neural recording chopper amplifier capable of handling in-band 80-mV<sub>pp</sub> differential artifacts and 650-mV<sub>pp</sub> CM artifacts while preserving the accompanying small neural signals. New techniques have been proposed that introduce immunity to CM interference, increase the input impedance of the chopper amplifier to 1.6 GΩ, and increase the maximum realizable resistance of duty-cycled resistors (DCR) to 90 GΩ. These techniques enable our recording front-end to achieve a dynamic range of 74 dB (200 Hz–5 kHz) and 81 dB (1–200 Hz). Implemented in a 40-nm CMOS process, the prototype occupies an area of 0.069 mm<sup>2</sup>/channel, and consumes 2.8 μW from a 1.2-V supply. The input-referred noise is 5.3 μV<sub>rms</sub> (200 Hz–5 kHz) and 1.8 μV<sub>rms</sub> (1–200Hz). The total harmonic distortion for a 40-mV<sub>p</sub> input at 1 kHz is –76 dB. This work improves the input impedance by 5.3× for chopped front-ends, linear-input range by 2×, maximum resistance of DCR by 32×, and tolerance to CM interferers by 6.5×, while maintaining comparable power and noise performance.

**Index Terms**—Chopper amplifier, closed-loop, common-mode interference, dynamic range, electrode offset, front-end, harmonic distortion, input impedance, large time constants, linearity, low-noise, low-power, multi-rate duty-cycled resistor (MDCR), neuromodulation, pseudo-resistors, neural recording.

## I. INTRODUCTION

NEURAL recordings are known to contain bio-markers for diagnosing neurological conditions, in the creation of brain-machine interfaces, and for neuro-prosthetic technologies to aid paralyzed patients [1]–[4]. However, neural stimulation is necessary to administer therapy in patients suffering from neurological ailments that do not respond to pharmacological treatment [5], [6]. Neural stimulation is

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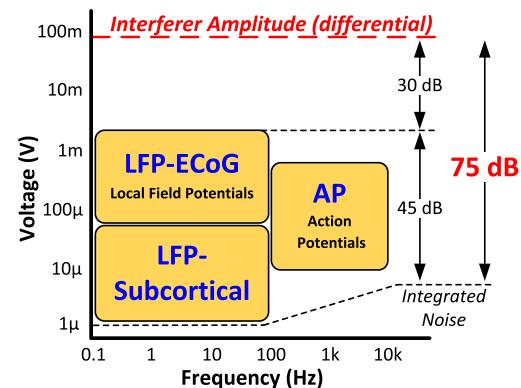


Fig. 1. Amplitude and frequency characteristics of recorded neural signals. The interferer denotes stimulation artifacts.

performed by sending controlled current pulses into specific regions of the brain to modulate brain activity. Existing stimulation therapies rely on continuous open-loop stimulation. Open-loop stimulation, though useful, can have detrimental side effects [7], [8] while losing its efficacy over time due to plasticity and other changes in the brain. Hence, neuroscientists aim to perform closed-loop stimulation where stimulation parameters are adapted in real time using recorded neural signals as feedback. This ensures that stimulation is applied only when necessary and with the required intensity, mitigating the undesirable effects of open-loop stimulation while maximizing the therapeutic benefits. Feedback also allows the stimulation parameters to track the dynamics of the brain, thus maintaining the therapeutic effects over time. Apart from therapy, a closed-loop neuromodulation system provides neuroscientists with an investigative tool to explore the workings of the brain. The next generation of neuromodulation systems requires implantable devices capable of closed-loop operation with hundreds of recording channels.

The neural signals of interest that are recorded by the electrodes occupy a frequency band from 1 Hz to 5 kHz. The various types of neural signals, along with their bandwidths and amplitudes are shown in Fig. 1 [2], [8], [9]. The local field potentials (LFPs) occupy a frequency band from 1 to 200 Hz, and the action potentials (APs) occupy a frequency band from 200 Hz to 5 kHz. The peak amplitude of LFPs is about 1 mV, and the peak amplitude of APs is about 100 μV.

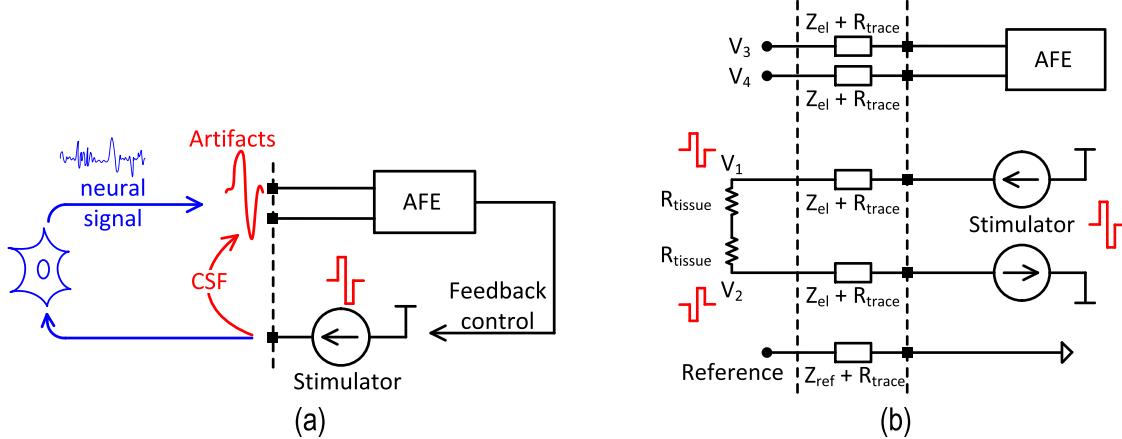


Fig. 2. (a) Simultaneous stimulation and recording, leading to artifacts in closed-loop neuromodulation systems. (b) Simplified equivalent circuit to estimate artifact amplitudes at the recording sites.

The thermal and biological background noise picked up by the electrodes is about  $10 \mu\text{V}_{\text{rms}}$  [22]. Thus, a recording front-end with 7–8 effective number of bits (ENOB) would suffice to faithfully digitize neural signals.

Fig. 2(a) shows a typical setup for closed-loop neural recording. Due to direct conduction paths through the cerebrospinal fluid (CSF), and capacitive coupling between traces from the electrodes to the recording electronics, large stimulation artifacts could appear at the recording sites. To estimate the amplitude of these stimulation artifacts, we use a simplified equivalent circuit [Fig. 2(b)] for simultaneous differential stimulation and recording. For peak stimulation current amplitudes of 3 mA, and assuming that the tissue impedance between two local stimulation sites is about 600–800  $\Omega$  [denoted by  $2R_{\text{tissue}}$  in Fig. 2(b)] [41], the maximum voltage swing generated in the tissue ( $V_1$  or  $V_2$ ) is 0.9–1.2 V. Note that the stimulator compliance voltage will be much higher to support the voltage drops across the electrode and trace impedances. These stimulation-induced tissue voltages will generate artifacts at the recording sites. However, since differential stimulation is employed (i.e.,  $V_1 = -V_2$ ), there will be partial cancellation of the artifacts appearing at the recording sites. Based on path mismatches due to electrode positions, tissue non-homogeneity, etc., the residual artifact amplitude can be estimated. Assuming a maximum path-mismatch impedance of 50%, the residual artifact amplitude is 450–600 mV<sub>pp</sub>. Differential recording (or recording with respect to a local reference electrode) further attenuates artifact amplitudes in the sensing signal path. However, this attenuation is also limited due to mismatches in the CSF and electrode impedances. Assuming that the worst case attenuation of common-mode (CM) artifacts due to differential recording is about 20 dB, the differential artifact amplitude ( $V_3 - V_4$ ) is 45–60 mV<sub>pp</sub>. Hence, the differential signal at the recording sites ( $V_3 - V_4$ ) will contain large stimulation artifacts along with the neural signals of interest. Since these artifacts occupy the same frequency band as the neural signals (Fig. 1), conventional up-front filtering cannot be used to attenuate these artifacts. To ensure simultaneous recording during stimulation (which is necessary for closed-

loop operation), the recording front-end must digitize neural signals to the required resolution of 7–8 bits in the presence of stimulation artifacts. Hence, the required signal-to-noise and distortion ratio (SNDR) for differential signals is >12 bits. Also, the recording front-end must achieve a 12-bit SNDR in the presence of 450–600 mV CM artifacts. This is a non-trivial requirement, since front-ends are usually susceptible to large CM signals. This susceptibility is explained later in Section IV-A. State-of-the-art implantable recording front ends saturate beyond an input amplitude of  $\sim 5$  mV and have limited linearity, making them incapable of handling stimulation artifacts. “Blanking” has been proposed in [10] and [11] to prevent saturation. However, the neural signals of interest are lost during the presence of artifacts. Also, stimulation artifacts could last for several milliseconds or more when burst or periodic stimulation pulses are used, which would result in severe loss of neural data if blanking is used. Another technique [12] attempts to estimate the artifact using an adaptive filter in the digital domain, and cancel the artifact in the analog domain using mixed-signal feedback. Artifact cancellation using feedback would significantly reduce the required dynamic range of the front-end, but this technique was demonstrated for artifacts less than 3 mV which is insufficient for closed-loop recording.

To ensure minimal signal loss in the presence of large artifacts, a high dynamic range recording front-end is required. Neural recording front-ends (Fig. 3) typically consist of a low-noise amplifier followed by an analog-to-digital converter (ADC). The amplifier gain can be limited to 30 dB to prevent saturation for large inputs, but this would require a high-resolution (>12 bits) ADC. Low-power ADCs with an ENOB of 13–14 bits have been published [13], but to the authors’ knowledge there is no implantable low-power neural recording amplifier that achieves a 12-bit SNDR in the presence of CM artifacts. This work presents a neural recording chopper amplifier capable of handling up to 80-mV<sub>pp</sub> in-band differential artifacts in the presence of 650-mV<sub>pp</sub> CM interferers, while maintaining the resolution of the accompanying neural signals. A large linear input signal range preserves

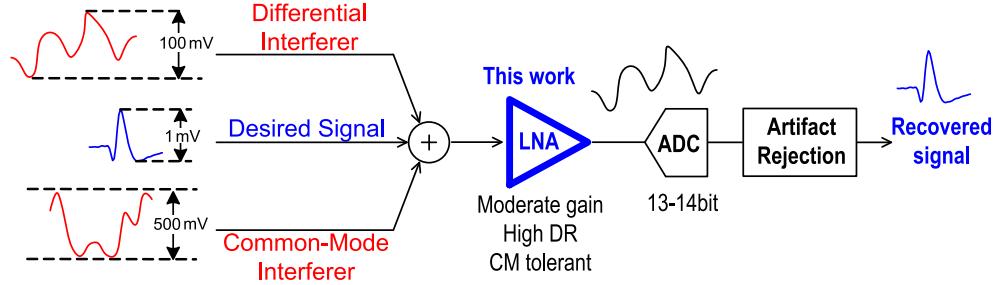


Fig. 3. Neural recording front-end for closed-loop recording. Conventional front-ends use a high-gain LNA with limited DR, which saturates in the presence of artifacts. This work presents a high-DR LNA tolerant to CM interference, with a large linear input signal range to accommodate artifacts.

TABLE I  
SYSTEM REQUIREMENTS AND SUMMARY OF THE STATE-OF-THE-ART

Parameter	JSSC 2007	JSSC 2011	ISSCC 2014	ISSCC 2016	Required
<b>Power (<math>\mu\text{W}</math>)</b>	2	1.8	2.3	2	<b>&lt; 5</b>
<b>BW (Hz)</b>	180	700	300	5k	<b>1-5k</b>
<b>Noise (<math>\mu\text{V}_{\text{rms}}</math>) over BW</b>	0.95	6.7	1.3	7	<b>4-8</b>
<b>DR (dB)</b>	67	--	50	69	<b>75</b>
<b>THD (dB)</b>	-60	--	-48	-74	<b>-75</b>
<b>I/P swing (<math>\text{mV}_{\text{pp}}</math>)</b>	10	--	1	40	<b>100</b>
<b>CM Tolerance</b>	No	No	No	No	<b>Yes</b>
<b>DC <math>Z_{\text{in}} (\Omega)</math></b>	8M	6M	28M	300M	<b>&gt; 1G</b>
<b>Area/Ch (<math>\text{mm}^2</math>)</b>	1.7	0.1	0.025	0.071	<b>&lt; 0.1</b>

the neural signals of interest, which can be subsequently extracted in the digital domain by performing adaptive artifact rejection (see Fig. 3).

## II. SYSTEM REQUIREMENTS

An implantable neural recording system needs to satisfy many design specifications to ensure functionality, patient safety, implantability, and prolonged battery life. The requirement of a 12-bit SNDR in the presence of CM interferers has been explained in Section I. The other requirements have been discussed in [14]–[16], which are summarized here. The power consumption of the neural recording front-end is limited by thermal dissipation constraints to prevent tissue damage [17], battery-life constraints, the number of recording channels used, and the dissipation capabilities of the implant. Studies in [39] and [40] suggest that dissipation of 10 mW for a  $6 \times 6 \times 2 \text{ mm}^3$  implant was low enough to avoid tissue damage. Assuming 50% power for stimulation and 50% for power conversion efficiency, the power consumption of the neural recording front-end should be less than  $10 \mu\text{W}$  per channel for a few hundred recording channels. Since the background noise picked up by the electrodes in the AP band is about  $10 \mu\text{V}_{\text{rms}}$ , the input-referred noise of the recording front-end in the AP band should be  $4-8 \mu\text{V}_{\text{rms}}$ . LFPs are known to have amplitudes ranging from  $10 \mu\text{V}-1 \text{ mV}$  (cortical recordings), to  $5-100 \mu\text{V}$  (sub-cortical recordings) [18].

Given the range of amplitudes, and assuming a minimum SNR of 0 dB, the front-end noise in the LFP band should be around  $2-3 \mu\text{V}_{\text{rms}}$ . Apart from neural signals and stimulation artifacts, a large dc offset appears at the recording electrodes due to the electrochemical effects at the electrode-tissue interface [14]. This offset needs to be rejected to prevent saturation. The value of this offset for differential recording from nominally identical electrodes can be up to 50 mV [18]. Thus a high-pass filter with a corner frequency less than 1 Hz is necessary to preserve the neural signals while attenuating the electrode offset. The electrode offset can create dc currents at the electrode due to the finite dc input impedance of the recording front-end. Prolonged presence of dc currents at the electrode can cause tissue damage. A dc input impedance  $Z_{\text{in}}$  larger than  $1 \text{ G}\Omega$  is required, since this limits the dc current to 50 pA for an offset voltage of 50 mV, which is sufficiently low for most applications [19]. Also, the input impedance in the frequency range of interest (1 Hz–5 kHz) needs to be much larger than the Thevenin impedance of the electrode ( $\sim 5 \text{ nF}$ ) to prevent signal attenuation [20], [21]. These requirements are summarized in Table I.

## III. REVIEW OF STATE-OF-THE-ART

There have been a large number of publications in the past two decades on neural recording front-ends. The capacitively coupled inverting amplifier [Fig. 4(a)] is among the most

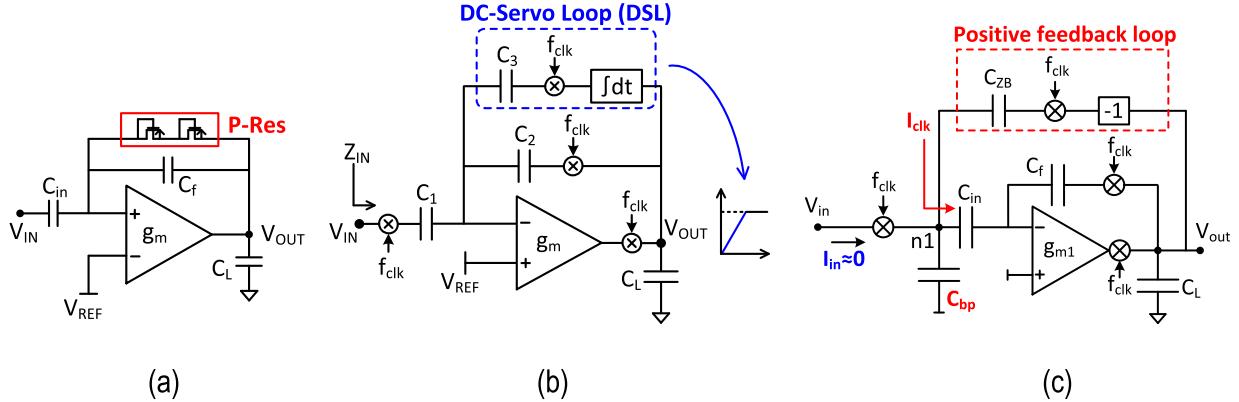


Fig. 4. (a) Capacitively coupled amplifier with pseudo-resistors. (b) Chopper amplifier with capacitive feedback and a servo-loop. (c) Positive feedback to boost the input impedance of a chopper amplifier.

popular topologies used [14], [22]–[25]. Capacitive coupling ensures that  $Z_{in}$  is large, and sizing the input capacitance smaller than 100 pF ensures negligible signal attenuation at the electrode. This topology has been optimized for power and noise, as discussed in [14]. The input devices are sized to have a large area to minimize their flicker noise contribution. To achieve low-frequency high-pass corners, pseudo-resistors are used [14], as they are an area-efficient way to realize very-low-frequency high-pass corners. However, pseudo-resistor nonlinearity limits the linearity of the front-end to 8 bits [24]. Pseudo-resistors are also very sensitive to process and temperature, as their resistance can vary by a factor of 100. In addition, any bulk leakage currents in the pseudo-resistor can create large dc bias shifts, leading to poor control of bias points in the front-end. These issues make the pseudo-resistor unreliable in a clinical setting [19].

The chopper-stabilized amplifier [Fig. 4(b)] is another popular front-end topology for neural recording [18], [26]–[28], as chopping is an effective way to mitigate the low-frequency flicker noise of the opamp. A servo-loop is usually employed to create a high-pass filter that attenuates the electrode offset at the output  $V_{out}$ . However, chopping reduces  $Z_{in}$  since the passive mixer at the input along with the capacitance  $C_{in}$  [Fig. 4(b)] form a switched-capacitor resistance. For  $C_{in}$  of 10 pF and  $f_{clk}$  of 20 kHz (typical values for this application),  $Z_{in}$  is limited to 2.5 MΩ, which is significantly lower than the required 1 GΩ. Off-chip coupling capacitors can be used to increase  $Z_{in}$  [29], but they become impractical for a miniaturized implant with a large number of recording channels. To boost  $Z_{in}$ , a positive feedback loop [Fig. 4(c)] has been used in [26]. However, this technique has significant drawbacks, as discussed in [30] and [31] that make it unsuitable for neural recording chopper amplifiers. Recently, a chopper amplifier with the “auxiliary path” was proposed [30], [31] to boost  $Z_{in}$ . However, this technique achieved a limited impedance boost and could cause large dc voltages and low-frequency noise to appear at the electrodes. These issues are discussed in Section IV-C. Another critical limitation of prior works is their susceptibility to large CM interference. This issue is discussed

in Section IV-A. The current state-of-the-art in neural recording is summarized in Table I. The state-of-the-art has successfully addressed power and noise, but is significantly lacking in the linear input range, input impedance, and tolerance to CM interferers.

#### IV. HIGH DYNAMIC-RANGE NEURAL RECORDING CHOPPER AMPLIFIER

##### A. Tolerance to CM Interference

The susceptibility of conventional recording front-ends to CM interference is explained using a typical chopper amplifier as an example. The amplifier is implemented using capacitive feedback [Fig. 5(a)] in the “inverting” topology. Chopping is implemented using passive mixers at the input and feedback arms of the capacitive-feedback network. The demodulation mixer is placed within the opamp  $g_m$ , usually in-between the first and second stages of a two-stage opamp. The signals appearing at the electrode inputs, as discussed before, consist of a differential signal with amplitudes <100 mV, and a CM signal with amplitudes around 500 mV. Passive mixers allow the CM signal to pass unaltered. The opamp used in the chopper amplifier is usually designed to respond only to differential signals while having high CM rejection. This is accomplished by using a differential-pair with a high-impedance tail current source. Also, CM feedback (CMFB) loops are used to set the bias voltages at the outputs of  $g_m$ . Hence, for CM signals, the CMFB loops create low-impedance connections to ac-ground at the output of  $g_m$ . To set the CM dc bias at the input of the opamp, large resistors [ $R_B$  in Fig. 5(a)] are used. The equivalent CM circuit for the chopper amplifier is shown in Fig. 5(b). The transfer function from the CM input at the electrode  $E_{CM}$  to the opamp input  $V_{in,CM}$  is found to be

$$\frac{V_{in,CM}}{E_{CM}} = \frac{\omega C_{in} R_B}{1 + \omega(C_{in} + C_f)R_B}. \quad (1)$$

The above transfer function is plotted in Fig. 5(c). We see that  $V_{in,CM}/E_{CM}$  is a first-order high-pass filter, with the corner frequency set by the capacitance  $C_{in} + C_f$  and the resistor  $R_B$ . To ensure proper functioning of the chopper amplifier, this

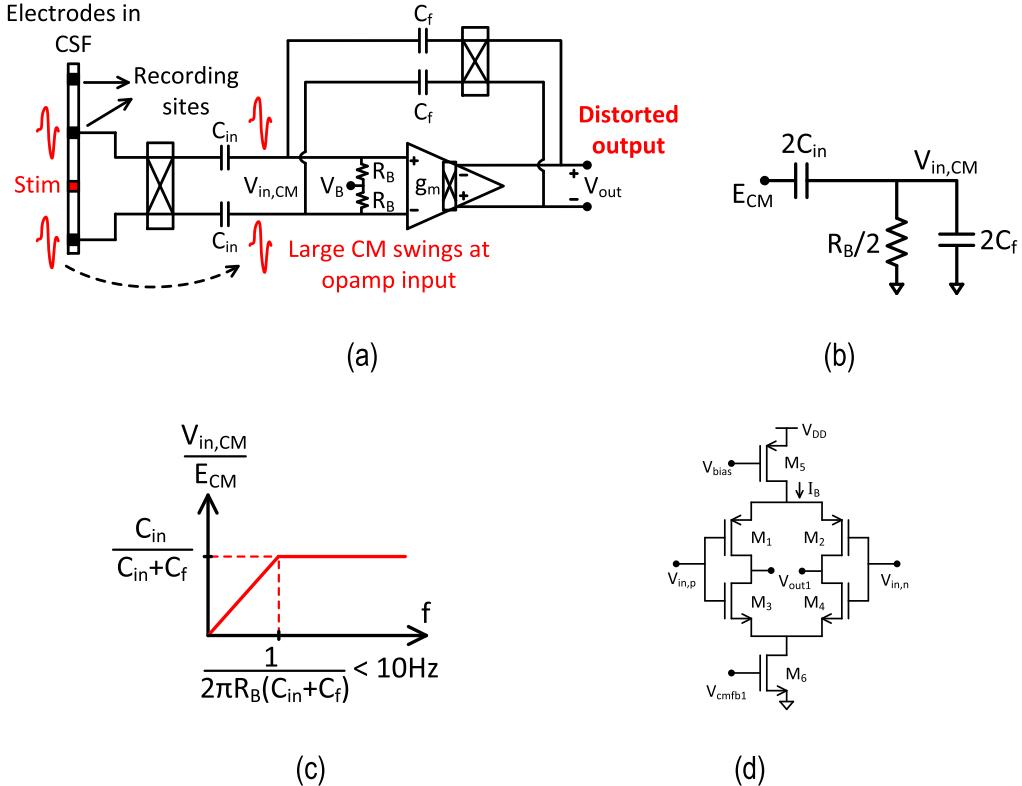


Fig. 5. (a) Response of a chopper amplifier to CM inputs. (b) Equivalent circuit of the chopper amplifier for CM signals. (c) Transfer function from  $E_{CM}$  to  $V_{in,CM}$ . (d) Current-reuse opamp.

corner frequency is usually set to  $<10$  Hz [32]. Hence, CM signals beyond 10-Hz pass unattenuated to the input of the opamp, which could cause the differential response of a power-optimized amplifier to show significant departures from the expected response. Consider the current-reuse differential-pair as shown in Fig. 5(d), which is the most common topology (due to its favorable power-noise tradeoff) used for the first stage of the opamp  $g_m$ . To ensure sufficient headroom for the tail current sources, the gate bias  $V_{in,CM}$  of the input transistors  $M_{1-4}$  must be within the following range:  $V_{ov6} + V_{GS3,4} < V_{in,CM} < V_{DD} - V_{ov5} - V_{GS1,2}$ , where  $V_{DD}$  is the supply voltage,  $V_{ov5,6}$  are the overdrive voltages of the tail current sources, and  $V_{GS1-4}$  are the required gate-source voltages for transistors  $M_{1-4}$  to carry a bias current of  $I_B/2$ . Assuming  $V_{DD} = 1.2$  V,  $V_{ov1,2} = 0.1$  V and  $V_{GS1-4} = 0.45$  V (typical values), the range for  $V_{in,CM}$  is  $0.55$  V  $< V_{in,CM} < 0.65$  V. Hence the input CM range (ICMR) is limited to be less than 100 mV. This range is significantly lower than the CM swings (500 mV) that are expected at the electrodes. To estimate the distortion caused by CM artifacts, the chopper amplifier in Fig. 5(a) was simulated with a differential input of 80 mV<sub>pp</sub> at 1 kHz, along with a CM interferer of 500 mV<sub>pp</sub> amplitude at 900 Hz. The total harmonic distortion (THD) degraded from  $-74$  to  $-43$  dB when the CM interferer was enabled, thus exposing the severity of the problem.

A simple solution to the CM-interferer problem would be to use an opamp with a large ICMR, such as a folded-cascode topology. Although the folded-cascode would consume more

than twice the power as compared to the current-reuse opamp (for the same noise), the immunity to CM interference could be worth the power penalty. However, it must be noted that these CM interferers are not “slow” signals. Since the CM interferers have the same bandwidth (BW) as the differential signals of interest, large CM swings at the input of opamps could lead to distortion. This is particularly significant when the opamp is designed for low-noise and low-power operation, i.e., the input devices (and possibly others) are biased in weak inversion, where they are most nonlinear. To verify this, we simulated a folded-cascode opamp (similar to [22]) with an nMOS input diff-pair, from a 1.2-V supply with an ICMR of 0.7 V. We set up a similar scenario as before—differential input of 40 mV<sub>pp</sub> at 1 kHz, along with a CM interferer of 500 mV<sub>pp</sub> amplitude at 900 Hz. Since the CM interferer (0.5 V) is smaller than the ICMR (0.7 V), the linearity of the front-end could be preserved in the presence of the CM interferer. However, the THD degraded from  $-78$  to  $-62$  dB when the CM interferer was enabled. Thus we see that a simple folded-cascode with its large ICMR is insufficient.

From the previous discussion, we see that the presence of large CM swings at the opamp input  $V_{in,CM}$  leads to distorted outputs. We propose a feed-forward CM cancellation (CMC) path to attenuate the CM swings at  $V_{in,CM}$ , which would restore the linear operation of the front-end for differential signals [33]. The concept of the CMC path is shown in Fig. 6(a). The CM signal at the electrodes is sensed and amplified by the opamp  $g_{ma}$  and capacitors  $C_a$  and  $C_b$ . This amplified

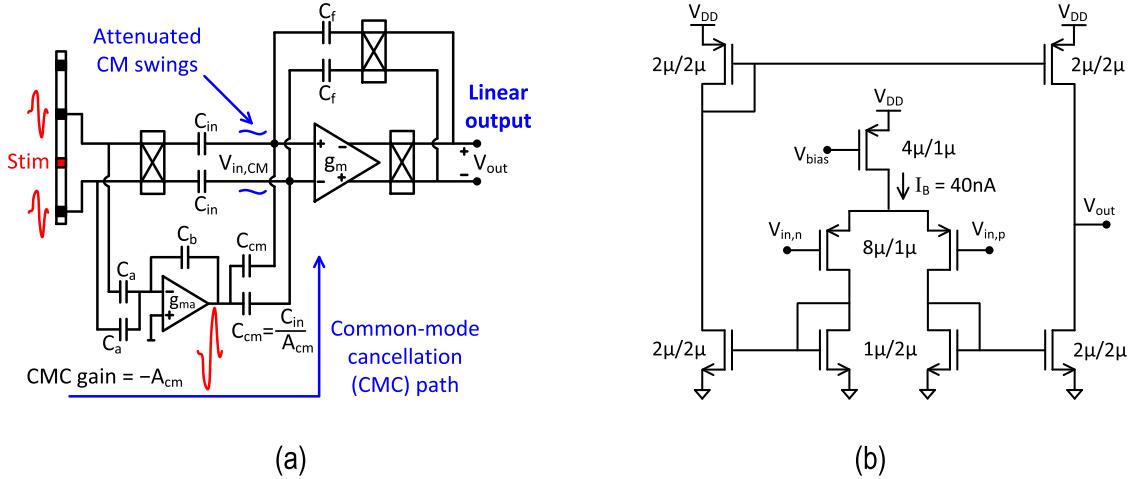


Fig. 6. (a) Proposed CMC path. (b) Opamp used in  $g_{ma}$ .

CM signal is then subtracted from  $V_{in,CM}$  through capacitors  $C_{cm}$ . The gain in the CMC path is set by the capacitor ratio  $A_{cm} = 2C_a/C_b$ . If  $C_{cm}$  is sized to be  $C_{in}/A_{cm}$ , then the CM signals at the input of the opamp  $V_{in,CM}$  are ideally cancelled to zero. Any mismatches in the ratio of  $C_{in}/C_{cm}$  would lead to residual CM swings at  $V_{in,CM}$ . However, since  $g_m$  is immune to small CM swings (<20 mV), a cancellation accuracy of 2% is sufficient. This can be easily achieved by matching the capacitors  $C_{in}$  and  $C_{cm}$ . However, the presence of the capacitors  $C_{cm}$  leads to an increase in the input-referred noise of the front-end, as shown by the following equation:

$$v_{n,in} = v_n \left[ 1 + \frac{C_{in} + C_{cm}}{C_f} \right]. \quad (2)$$

Here,  $v_n$  is the input-referred noise of the opamp  $g_m$ . To minimize the increase in the input-referred noise,  $C_{cm}$  should be sized smaller than  $C_{in}$ . This requirement leads to a larger gain  $A_{cm}$  in the CMC path. However, increasing  $A_{cm}$  results in larger signal swings at the output of  $g_{ma}$ , which will cause saturation due to limited headroom at the output of  $g_{ma}$ . This will prevent the CMC path from cancelling the CM swings at  $V_{in,CM}$ . To increase the headroom at the output of  $g_{ma}$ , we integrate a 50% efficient charge-pump on-chip to generate a local 1.8-V supply for  $g_{ma}$  from the available 1.2-V supply. Thus, with the CMC gain  $A_{cm} = 2$ , CM signals as large as 650 mV<sub>pp</sub> can be easily cancelled at  $V_{in,CM}$ , while the noise contribution of  $g_m$  is kept low. To ensure accurate cancellation, the bandwidth of the CMC path must be well beyond the expected bandwidth of the CM artifacts. Since we expect CM artifacts in the entire neural signal band up to 5 kHz, the CMC-path bandwidth is set to 30 kHz. This sets the requirement of  $g_{ma}$  as follows:

$$g_{ma} \left( \frac{C_b}{C_b + 2C_a} \right) \frac{1}{2\pi(C_b + 2C_{cm})} > 30 \text{ kHz}. \quad (3)$$

Hence, for  $C_a = C_b = 1 \text{ pF}$  and  $C_{cm} = 0.5 \text{ pF}$ ,  $g_{ma}$  should be larger than  $1.13 \mu\text{A/V}$ . The schematic of the opamp used to realize  $g_{ma}$  is shown in Fig. 6(b). A current of 120 nA was sufficient to achieve the required  $g_{ma}$ , which is a small fraction of the overall power budget. Hence a relatively low

efficiency (50%) charge-pump design was chosen for simplicity and reducing design time, since the power overhead is negligible.

Although the CMC-path attenuates CM swings at  $V_{in,cm}$ , mismatches in  $C_{cm}$  could degrade CMRR. However, since  $C_{cm}$  is large (0.5 pF), good matching (<0.1%) between  $C_{cm}$  can be achieved by using common-centroid layout techniques. Any residual mismatches in  $C_{cm}$  would indeed convert a CM signal at the electrode into a differential signal flowing out of the CMC path. However, note that there is no chopping at the output of the CMC path. Hence, the CM-to-DM signal at the CMC output remains at baseband, as compared to the up-modulated differential signal of the electrode. Thus, the CM-to-DM component remains separate (in frequency) from the desired differential signal, which ensures negligible impact to CMRR.

### B. Realizing Very-Low Corner Frequencies

As discussed in Section II, the neural signals at the electrodes (<1 mV) are accompanied by electrode offsets as large as 50 mV. Hence, any amplification must be applied only to the neural signals while attenuating the offset to prevent saturation. Since the signals of interest occupy frequencies as low as 1 Hz, a high-pass filter is necessary with a corner frequency less than 1 Hz. Such low corner frequencies can be difficult to implement as they usually require very-large resistors and capacitors, making it prohibitively area expensive. Conventional capacitive-feedback amplifiers have been reported in [14], [23], and [24] that use “pseudo-resistors” as large resistors to realize sub-hertz high-pass corners. However, as discussed in Section III, pseudo-resistors are unreliable due to its nonlinearity and sensitivity to process and temperature variations.

In chopper amplifiers, a dc-Servo loop can be used [26] to realize the required high-pass corner frequency. The dc servo-loop consists of a low-bandwidth integrator that is placed in a negative feedback loop around the chopper amplifier [see Fig. 4(b)]. The high loop-gain of the servo-loop attenuates low-frequency signals at the output  $V_{out}$ , thus

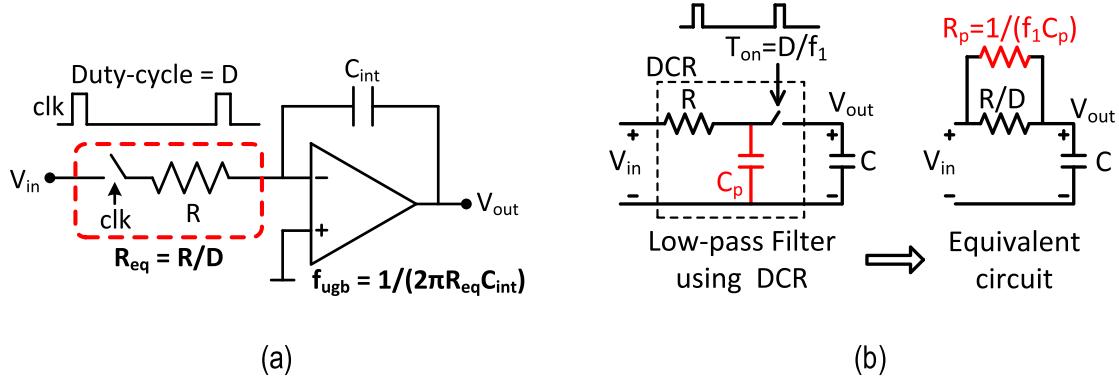


Fig. 7. (a) Low-BW integrator using the conventional DCR. (b) Equivalent circuit of an LPF using the DCR.

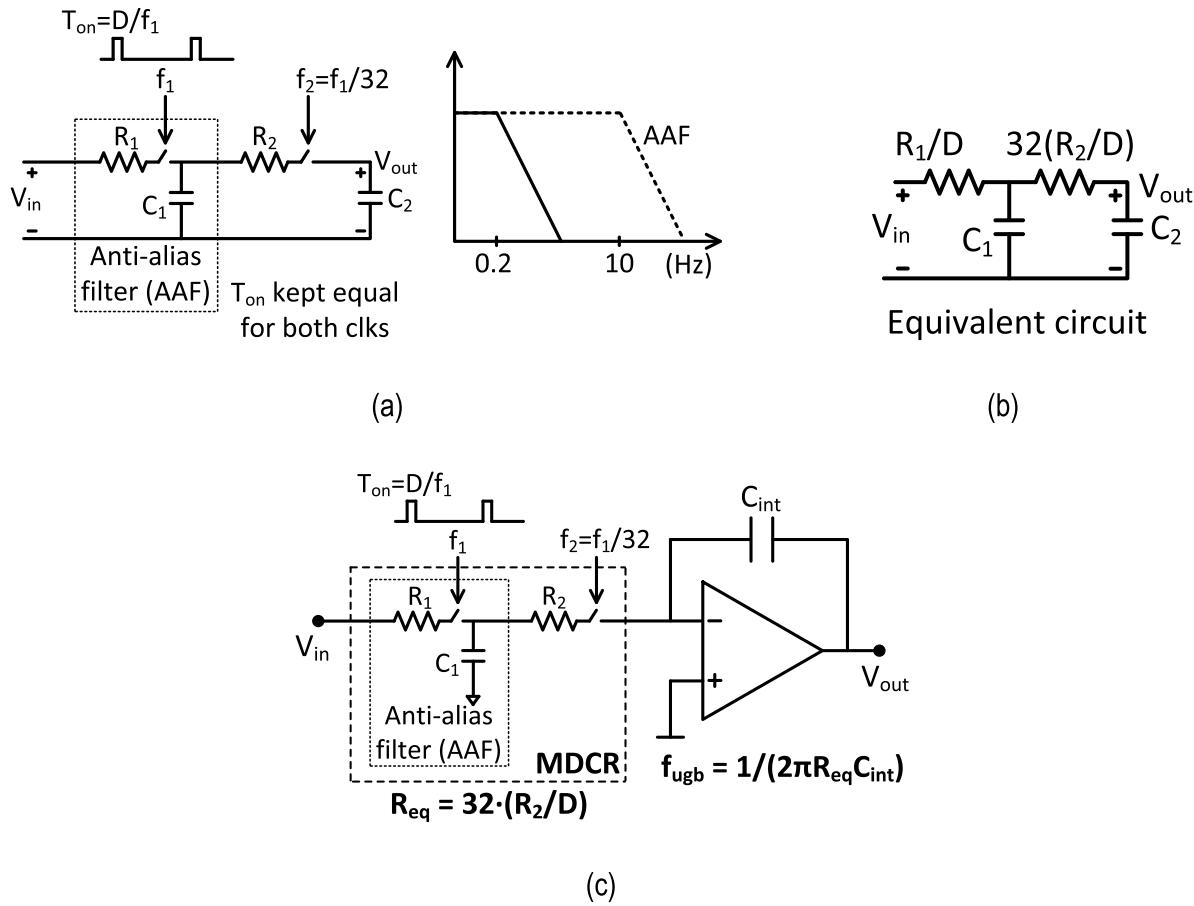


Fig. 8. (a) Proposed MDCR to realize large resistance while overcoming the limitation due to parasitic capacitance. (b) Equivalent circuit of the LPF in (a). (c) Low-BW integrator using the proposed MDCR.

realizing the required high-pass corner. For frequencies beyond the unity-gain bandwidth (UGB) of the servo-loop, the servo-loop is effectively broken. Hence, since the signal band of interest lies beyond the servo-loop UGB, the output noise of the servo-loop integrator in the signal band will be amplified by  $C_3/C_2$  and appear at  $V_{out}$  [see Fig. 4(b)]. The noise analysis of the servo-loop is presented in [18].

However, to achieve a sub-hertz high-pass corner frequency, a very-low bandwidth integrator is necessary in the servo-loop [26], [34]. Prior work has used duty-cycled resistors (DCR) [31] to realize such low-bandwidth integrators

[see Fig. 7(a)]. The DCR consists of a passive resistor  $R$  in series with a switch. When the switch is driven by a clock with a duty-cycle factor of  $D$ , the average resistance is amplified by  $1/D$  [31], [35]. This amplified resistance can be used to realize the required low-bandwidth integrator for the servo-loop. From discussions in [31], we see that the in-band noise contribution (when referred to the electrodes) of the DCR in the servo-loop can be reduced by realizing larger equivalent resistances  $R/D$ . Similar arguments can also be used to show that the in-band noise of the DCR  $R_B$  [Fig. 5(a)] can be reduced by realizing larger equivalent resistances. However, the

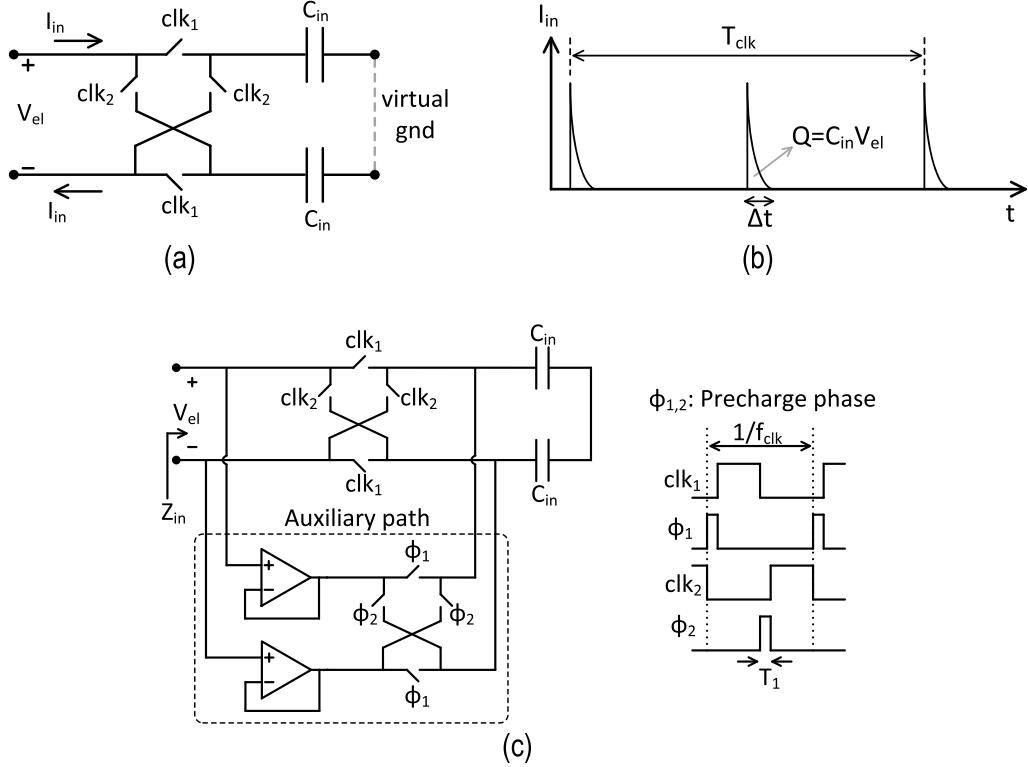


Fig. 9. (a) Input branch of the chopper amplifier. (b) Current provided by the electrode during chopping. (c) Auxiliary-path technique proposed in [31].

maximum resistance of the DCR is limited by the parasitic capacitance that appears in-between the passive resistor  $R$  and the switch [see Fig. 7(b)]. This parasitic capacitance results in an equivalent switched-cap resistor  $R_p$  that appears in parallel across the amplified resistance  $R/D$ , thus limiting the maximum equivalent resistance to  $R_p$ . The value of  $R_p$  is given by  $1/(f_1 C_p)$ , where  $C_p$  is the value of the parasitic capacitance and  $f_1$  is the switching frequency of the DCR. As an example, for  $C_p = 5\text{fF}$  and  $f_1 = 25\text{ kHz}$  (both being typical values),  $R_p$  is set to  $8\text{ G}\Omega$ . To increase  $R_p$ , either  $f_1$  or  $C_p$  can be reduced. However,  $C_p$  is limited by the substrate capacitance of the resistance  $R$ , while  $f_1$  must be greater than twice the signal bandwidth to avoid aliasing. Thus it would seem that the maximum resistance is limited to  $8\text{ G}\Omega$ . We propose the multi-rate duty-cycled resistor (MDCR) to solve this problem [33]. The MDCR is shown in Fig. 8(a). Let's assume that we need to realize a  $0.2\text{-Hz}$  low-pass filter. Since such a low corner frequency would require an exceptionally large resistance [much larger than  $R_p$  from Fig. 7(b)], we instead first realize a low-pass filter with a moderately low corner frequency of  $10\text{ Hz}$ . This low-pass filter, termed the anti-alias filter (AAF) in Fig. 8(a), is realized by the DCR formed by  $R_1$  switching at  $f_1$ , and the capacitor  $C_1$ . The AAF is followed by a second low-pass filter formed by the DCR  $R_2$  switching at  $f_2$ , and the capacitor  $C_2$ . The AAF allows for a significantly reduced switching frequency  $f_2$ , as the AAF reduces the bandwidth of the signal flowing into the second low-pass filter. The lower limit on the switching frequency  $f_2$  is determined by the bandwidth  $f_{\text{aaf}}$  of the AAF and the required attenuation of the

aliased components. For this work, we chose to have  $f_2/f_{\text{aaf}}$  to be greater than  $64$ , which provides sufficient attenuation to the aliased components. Hence, in the second low-pass filter, we have circumvented the limitation of the minimum required switching frequency by using the AAF, thus increasing the maximum realizable resistance of the DCR (formed by  $R_2$  switching at  $f_2$ ) by a factor of  $f_1/f_2$ . The equivalent circuit of this composite low-pass filter is shown in Fig. 8(b). The ON duration of the switches  $T_{\text{ON}}$  is  $5\text{ns}$ , and  $f_1$  was set to  $23.44\text{ kHz}$ . This results in a duty-cycle factor  $D$  of  $1/8530$  for the DCR formed by  $R_1$  switching at  $f_1$ .  $R_1$  and  $R_2$  were set to  $350\text{ k}\Omega$ , which leads to the equivalent resistance  $R_{1,\text{eq}} = R_1/D = 3\text{ G}\Omega$ . Thus,  $R_{1,\text{eq}}$  along with  $C_1 = 6\text{ pF}$  leads to an anti-alias corner frequency  $f_{\text{aaf}}$  of  $10\text{ Hz}$ . In the second low-pass filter,  $f_2$  is set to be  $f_1/32 = 732.5\text{ Hz}$ . This leads to the equivalent resistance  $R_{2,\text{eq}} = (R_2/D) \times 32 = 90\text{ G}\Omega$ . Hence,  $R_{2,\text{eq}}$  along with  $C_2 = 12\text{ pF}$  leads to the required low-pass corner frequency of  $0.15\text{ Hz}$ . Thus by using the MDCR, a  $350\text{-k}\Omega$  resistance has been amplified to  $90\text{ G}\Omega$ .

Though the above example is a passive low-pass filter, the MDCR can also be used as a large resistor to realize low-bandwidth integrators, as shown in Fig. 8(c). The transfer function and noise analysis of the conventional DCR have already been discussed in [31], and the results directly translate to the MDCR. Hence, the noise contribution of the MDCR is nearly identical to the noise contributed by the equivalent amplified resistance. By using the MDCR, we have realized a much larger resistance than what was possible using the

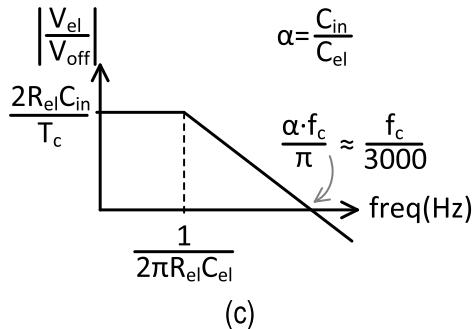
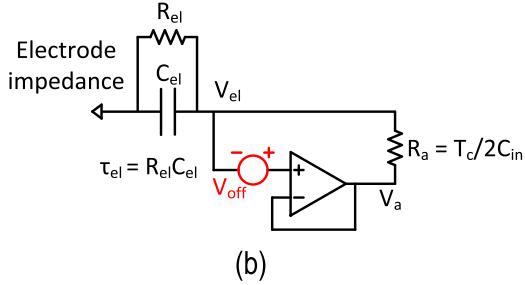
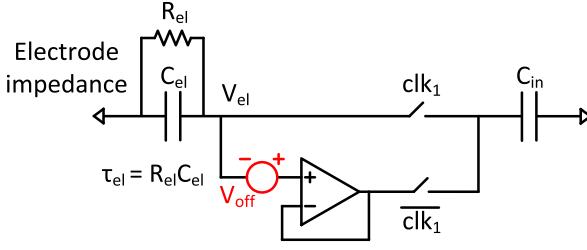


Fig. 10. (a) Half-circuit of the auxiliary path to analyze positive feedback. (b) Equivalent circuit using switched-cap approximation. (c) Transfer function from  $V_{off}$  to  $V_{el}$  due to positive feedback, leading to amplified buffer offset and flicker noise appearing at  $V_{el}$ .

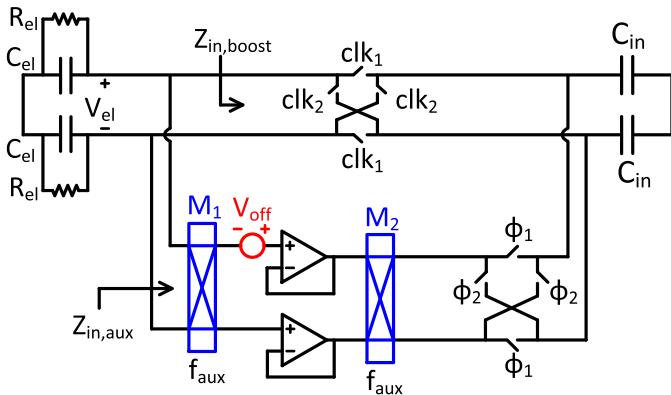


Fig. 11. Proposed auxiliary-path chopping using mixers  $M_{1,2}$  to mitigate the effect of positive feedback.

conventional DCR, leading to lower noise in the front-end. Also, the MDCR can be realized in a small chip area, and there's no penalty on linearity unlike the pseudo-resistor.

Since the MDCR is equivalent to a cascade of two low-pass filters [Fig. 8(b)], it could cause instability when used in a feedback loop since it introduces two poles. The servo-loop

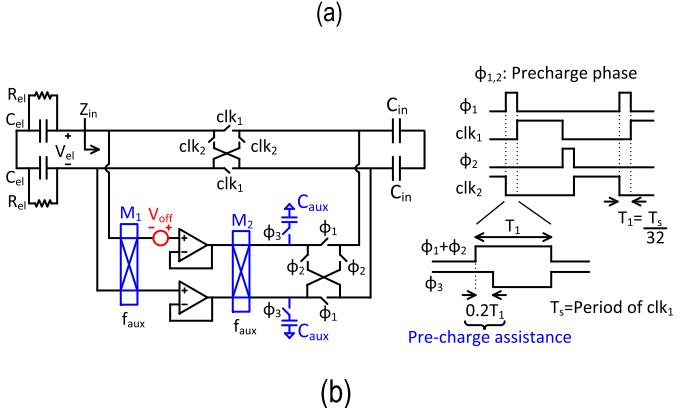
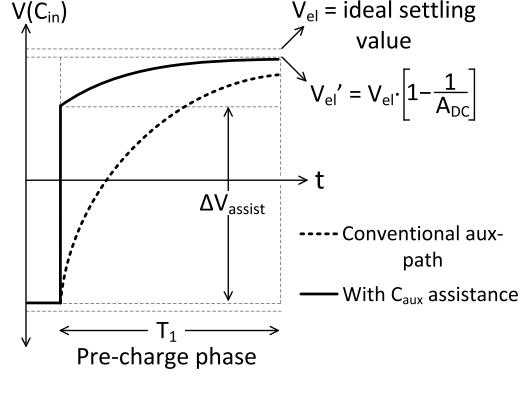


Fig. 12. (a) Settling errors in the precharge phase [referring to Fig 9(c)] leading to limited  $Z_{in}$ -boost using the auxiliary path. (b) Implementation of auxiliary-buffer assistance using storage caps  $C_{aux}$ .

UGB sets the high-pass corner  $f_{HP}$  of the signal transfer function [see Fig. 4(b)]. Let the servo-loop integrator have a UGB of  $f_{ugb,dsl}$ . Hence, from Fig. 4(b),  $f_{HP} = f_{ugb,dsl}(C_3/C_2)$ . To ensure stability, we must choose the AAF corner to be much larger than  $f_{HP}$ . We return to this point in Section V.

### C. Auxiliary Path for Boosting Input Impedance

The auxiliary path to boost the input impedance  $Z_{in}$  of a chopper amplifier has been discussed in [31]. The input arm of the chopper amplifier, consisting of capacitors  $C_{in}$  and the passive mixer is shown in Fig. 9(a). The charge provided by  $V_{el}$  is limited to a narrow time window [ $\Delta t$  in Fig. 9(b)] at the beginning of every chopping phase. If an alternate reservoir of charge (as opposed to the electrodes) could provide the charge required by  $C_{in}$ , then  $Z_{in}$  can be increased. This concept led to the auxiliary-path technique [31], [37], [38] [see Fig. 9(c)]. The advantage of this technique over the positive feedback loop in [26] is that the auxiliary path can be used simultaneously with the servo-loop, unlike the positive feedback loop which is rendered inoperative by the servo-loop at low frequencies [31]. The auxiliary path is also immune to parasitic capacitance, which limits the maximum impedance that can be achieved by the positive feedback loop [26]. However, this technique has two limitations. First, it provided insufficient boost to  $Z_{in}$ , as Chandrakumar and Marković [31] reported a boosted  $Z_{in}$  of 300 MΩ while we require  $Z_{in}$  larger than 1 GΩ.

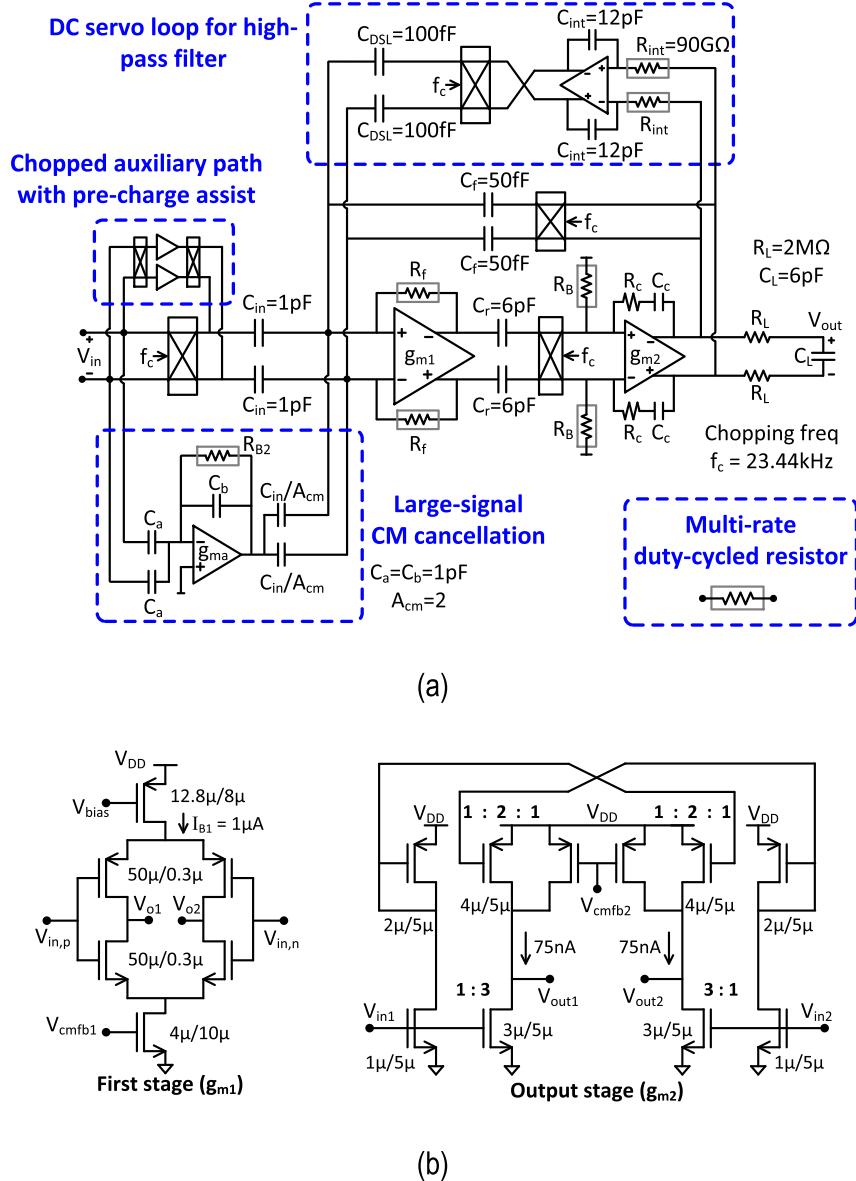


Fig. 13. (a) Complete implementation of the proposed front-end. Passives  $C_r$  and  $R_f$  are included for ripple-rejection [32]. (b) Schematics of transconductance  $g_{m1}$  and  $g_{m2}$  used in (a).

The second limitation is that this technique forms a positive feedback loop around the auxiliary path (not to be confused with the positive feedback loop discussed in [26]), since the electrode is not an ideal voltage source. It can be shown that this positive feedback will cause the dc offset and flicker noise of the auxiliary-path buffers to be amplified and appear at the electrodes. Thus, the amplified offset could cause saturation, and the amplified flicker noise will degrade the performance of the front-end since it adds directly at the input of the front-end. The positive feedback in the auxiliary path is analyzed below. The differential half-circuit of the auxiliary path along with the input arm of the chopper amplifier is shown in Fig. 10(a). The offset and flicker noise of the buffer is modeled as a voltage source  $V_{off}$ , while the electrode impedance is modeled by the impedance  $R_{el}||C_{el}$ . For simplicity, we assume  $R_{el}$  is infinite. In the pre-charge phase, the buffer charges the

capacitor  $C_{in}$  to  $V_{el} + V_{off}$ . At the end of the pre-charge phase,  $C_{in}$  is re-connected back to  $V_{el}$ , and the electrode voltage is given by

$$V_{el}(n+1) = V_{el}(n) + \left( \frac{C_{in}}{C_{in} + C_{el}} \right) \cdot V_{off}(n). \quad (4)$$

From (4), we see that the transfer function from  $V_{off}$  to  $V_{el}$  is identical to that of an ideal first-order integrator. Hence for a non-zero dc value of  $V_{off}$ ,  $V_{el}$  will go to infinity. To get a more accurate description of the positive feedback, the effect of a finite  $R_{el}$  is considered next. From Fig. 10(a), the capacitance  $C_1$  is periodically switched between the buffer output and the electrode. Hence, this switching capacitance forms an equivalent resistance [Fig. 10(b)] with a value of  $R_a = T_c/(2C_{in})$ , where  $T_c$  is the chopping period. Thus the buffer output  $V_a = V_{el} + V_{off}$ , and  $V_{el} = V_a \cdot Z_{el}/(Z_{el} + R_a)$ .

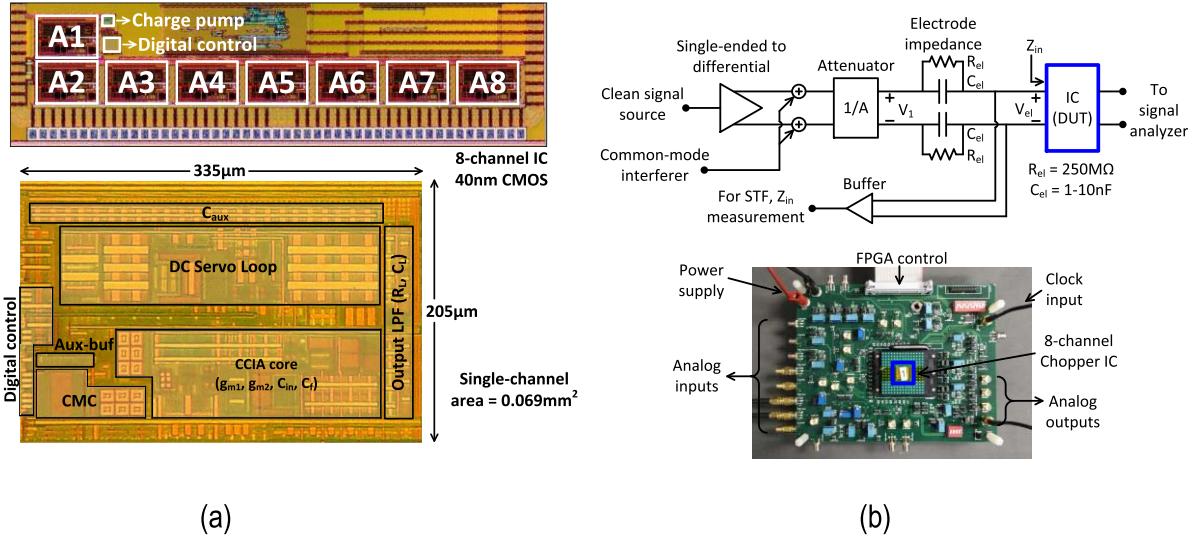


Fig. 14. (a) Micrograph of the fabricated prototype showing eight chopper amplifiers implemented in 40-nm CMOS. (b) Test setup for characterizing the fabricated chopper amplifier.

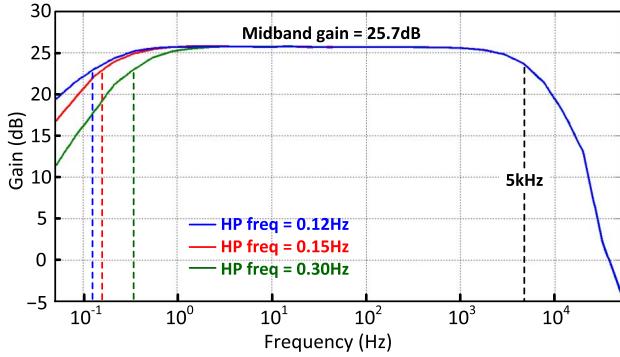


Fig. 15. Measured signal transfer function of fabricated chopper amplifier, with programmable high-pass corner frequency.

Using these two equations, the transfer function  $V_{el}/V_{off}$  is determined to be

$$\frac{V_{el}}{V_{off}}(s) = \frac{2R_{el}C_{in}}{T_c(1 + sR_{el}C_{el})}. \quad (5)$$

The above transfer function is shown in Fig. 10(c). The dc gain is given by  $2R_{el}C_{in}/T_c$ . Assuming  $R_{el} = 200 \text{ M}\Omega$ ,  $C_{in} = 1 \text{ pF}$ ,  $C_{el} = 1 \text{ nF}$ , and  $T_c = 40 \mu\text{s}$  (all typical values), the dc gain from  $V_{off}$  to  $V_{el}$  is 10. Hence, a 5-mV auxiliary-buffer offset is amplified to a 50-mV dc voltage by the positive feedback in the auxiliary path, and this voltage appears at the electrodes. Also, from the transfer function in Fig. 10(c), we see that low-frequency components of  $V_{off}$ , for example the flicker noise of the auxiliary buffers, will also be amplified and appear at the electrodes, thus degrading the low-frequency noise performance of the front-end.

A solution to this problem can be determined by taking a closer look at the transfer function in Fig. 10(c). The UGB of this transfer function is given by  $\alpha f_c/\pi$ , where  $\alpha$  is the ratio given by  $C_{in}/C_{el}$ . For the above-chosen typical values of  $C_{in}$  and  $C_{el}$ , the UGB of  $V_{el}/V_{off}$  is approximately given by  $f_c/3000$ . Thus, if  $V_{off}$  can be up-modulated to a frequency

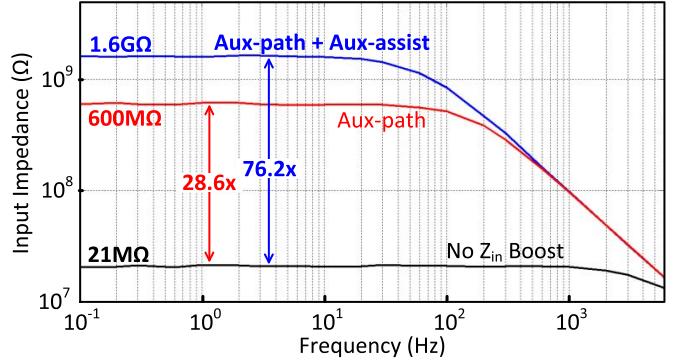


Fig. 16. Measured input impedance of the chopper amplifier using different impedance boost techniques.

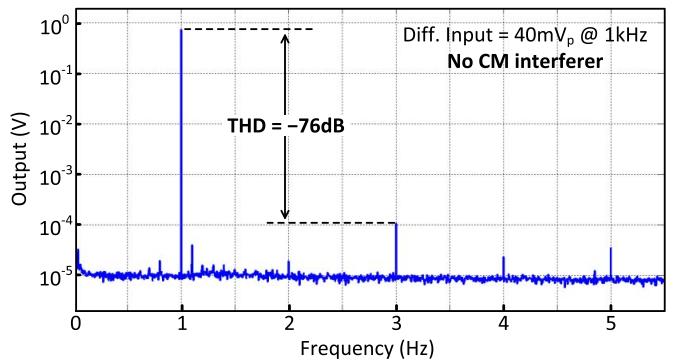


Fig. 17. Measured harmonic distortion of the chopper amplifier for a 40-mV<sub>p</sub> input at 1 kHz.

that is much larger than  $f_c/3000$ , then  $V_{off}$  will appear as tiny ripples at the electrode instead of a large dc voltage. This is realized by introducing passive mixers  $M_{1,2}$  in the auxiliary path (see Fig. 11) [33]. The frequency of the ripple at the electrodes will be equal to the clock frequency  $f_{aux}$  used in the mixers  $M_{1,2}$ . To ensure that these ripples remain outside the

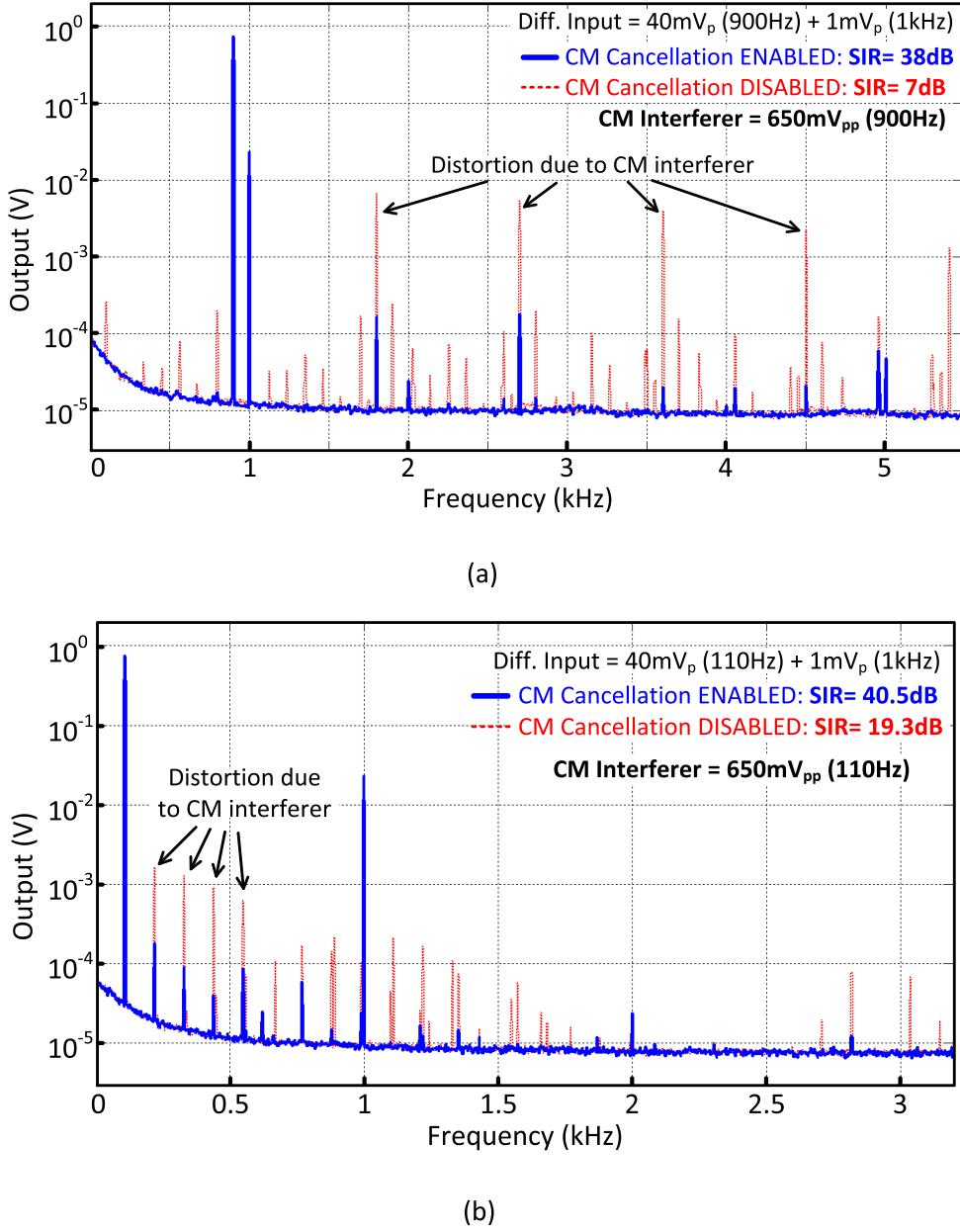


Fig. 18. Response of the front-end to two-tone tests with a large CM interferer, showing the severity of distortion (without CMC), and the efficacy of the CMC path in reducing distortion. (a) With a high-frequency interferer. (b) With a low-frequency interferer.

frequency band of interest,  $f_{aux}$  should be larger than 5 kHz. The amplitude of the ripples can be determined to be

$$V_{\text{ripple}} \approx V_{\text{off}} \left( \frac{4}{\pi^2} \right) \frac{\alpha f_c}{f_{aux}}. \quad (6)$$

Although introducing mixers  $M_{1,2}$  can mitigate the amplification of  $V_{\text{off}}$ , it will reduce the input impedance of the front-end. This is because the gate capacitance of the auxiliary-path buffers along with the mixer  $M_1$  will appear as a switched-cap resistance  $Z_{\text{in},\text{aux}}$  at the input of the front-end. Hence the input impedance of the front-end is now given by  $Z_{\text{in},\text{boost}} \parallel Z_{\text{in},\text{aux}}$ , where  $Z_{\text{in},\text{boost}}$  is the boosted input impedance achieved by the auxiliary path (see Fig. 11). To achieve the required 1-GΩ dc input impedance,  $Z_{\text{in},\text{aux}}$  must be significantly larger than

1GΩ.  $Z_{\text{in},\text{aux}}$  is given by  $1/(2C_{\text{auxbuf}} \cdot f_{aux})$ , where  $C_{\text{auxbuf}}$  is the gate capacitance of each auxiliary-path buffer. Since  $f_{aux}$  has a minimum value of 5 kHz,  $C_{\text{auxbuf}}$  must be reduced to achieve the required value of  $Z_{\text{in},\text{aux}}$ . However, reducing  $C_{\text{auxbuf}}$  is achieved by reducing the area of the input transistors of the auxiliary buffers, which will lead to a larger value of  $V_{\text{off}}$  due to increased mismatch. This will cause larger ripples at the electrode [from (6)] which is undesirable. Hence while sizing the input transistors of the auxiliary buffers, the tradeoffs for the input impedance and the ripple amplitudes at the electrode must be considered together.  $V_{\text{off}}$  is proportional to  $1/\sqrt{C_{\text{auxbuf}}}$  and the ripple amplitude is proportional to  $V_{\text{off}}/f_{aux}$ . Thus, accounting for all tradeoffs, the ripple amplitude  $V_{\text{ripple}}$  is proportional to  $Z_{\text{in},\text{aux}} \cdot \sqrt{C_{\text{auxbuf}}}$ . Hence for a given  $Z_{\text{in},\text{aux}}$ ,

TABLE II  
COMPARISON WITH THE CURRENT STATE-OF-THE-ART

Spec	[18] JSSC'07	[26] JSSC'11	[36] JSSC'12	[27] ISSCC'14	[31] JSSC'17	This work
<b>Power/Ch</b>	2 $\mu\text{W}$	1.8 $\mu\text{W}$	5.04 $\mu\text{W}$	2.3 $\mu\text{W}$	2 $\mu\text{W}$	<b>2.8 <math>\mu\text{W}</math></b>
<b>Supply</b>	1.8 V	1 V	0.5 V	0.5 V	1.2 V	<b>1.2 V</b>
<b>Signals <sup>a</sup></b>	LFP	LFP	AP + LFP	LFP	AP + LFP	<b>AP + LFP</b>
<b>Peak Input</b>	5 mV <sub>p</sub>	---	---	0.5 mV <sub>p</sub>	20 mV <sub>p</sub>	<b>40 mV<sub>p</sub></b>
<b>Input-referred noise (V<sub>rms</sub>)</b>	LFP: 1 $\mu\text{V}$	LFP: 6.7 $\mu\text{V}$	AP: 4.7 $\mu\text{V}$ LFP: 4.3 $\mu\text{V}$	LFP: 1.3 $\mu\text{V}$	AP: 7 $\mu\text{V}$ LFP: 2 $\mu\text{V}$	<b>AP: 5.3 <math>\mu\text{V}</math> LFP: 1.8 <math>\mu\text{V}</math></b>
<b>NEF</b>	LFP: 4.6	LFP: 14	AP: 5.99 LFP: 30	LFP: 4.76	AP: 4.9 LFP: 7	<b>AP: 4.4 LFP: 7.4</b>
<b>DC Input-impedance</b>	8 M $\Omega$	6 M $\Omega$	$\infty$	28 M $\Omega$	300 M $\Omega$	<b>1.6 G<math>\Omega</math></b>
<b>Off-chip caps</b>	Yes	Yes	No	Yes	Yes	<b>No</b>
<b>Dynamic Range <sup>b</sup></b>	67 dB (LFP)	---	$\sim$ 35 dB	50 dB (LFP)	69 dB (AP) 78 dB (LFP)	<b>74 dB (AP) 81 dB (LFP)</b>
<b>Total Harmonic Distortion</b>	-60 dB	---	-37 dB	-48 dB	-74 dB	<b>-76 dB</b>
<b>Tolerance to large-signal CM</b>	No	No	No	No	No	<b>Up to 650 mV<sub>pp</sub></b>
<b>Area/ch</b>	1.7 mm <sup>2</sup>	0.1 mm <sup>2</sup>	0.013 mm <sup>2</sup>	0.025 mm <sup>2</sup>	0.071 mm <sup>2</sup>	<b>0.069 mm<sup>2</sup></b>
<b>Technology</b>	0.8um	65nm	65nm	65nm	40nm	<b>40nm</b>

<sup>a</sup> LFP: Local Field Potentials, AP: Action Potentials

<sup>b</sup> Calculated for distortion power = noise power

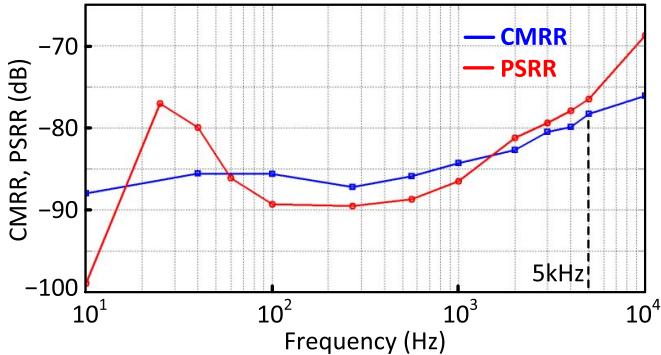


Fig. 19. CMRR and PSRR measurements of the complete front-end chopper amplifier.

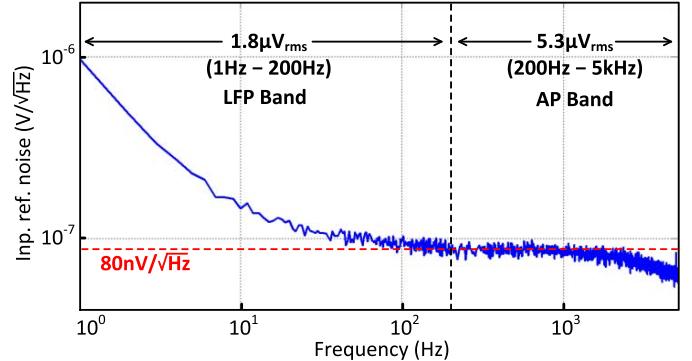


Fig. 20. Measured input-referred noise of the chopper amplifier.

$C_{auxbuf}$  must be minimized to reduce ripple amplitudes at the electrodes. This corresponds to using minimum-sized devices for the input transistors of the auxiliary buffers.  $C_{auxbuf}$  will ultimately be limited by routing capacitance. Hence, a practical solution would be to reduce the gate capacitance of the input devices of the auxiliary buffers to match the routing capacitance between the gate and the mixer  $M_1$ . The mixers  $M_{1,2}$  are driven with a clock frequency of  $f_c/4$ , where  $f_c = 23.44$  kHz is the chopping frequency of the chopper amplifier. The input transistors of the auxiliary buffers are sized such that  $C_{auxbuf}$

(including routing capacitance) is about 15 fF, which sets  $Z_{in,aux}$  to be about 6 G $\Omega$ . Hence  $Z_{in,aux}$  is sufficiently large to achieve the required input impedance of the front-end.

As discussed before, a limitation of the auxiliary path was the limited boost to  $Z_{in}$  [31]. This limitation was due to the limited bandwidth of the auxiliary buffers, which caused a non-zero settling error in the pre-charge phase. The finite gain of the opamp used in the auxiliary buffers also leads to a non-zero settling error in the pre-charge phase [31]. This is illustrated in Fig. 12(a) [with reference to Fig. 9(c)]. The input impedance at dc was derived in [31], and is restated here

Channel #	1	2	3	4	5	6	7	8	9	10	11	12
Measured electrode offset (mV)	7.5	9.1	36	45	6.1	7.6	5.7	21.4	2.8	12.6	3.6	18

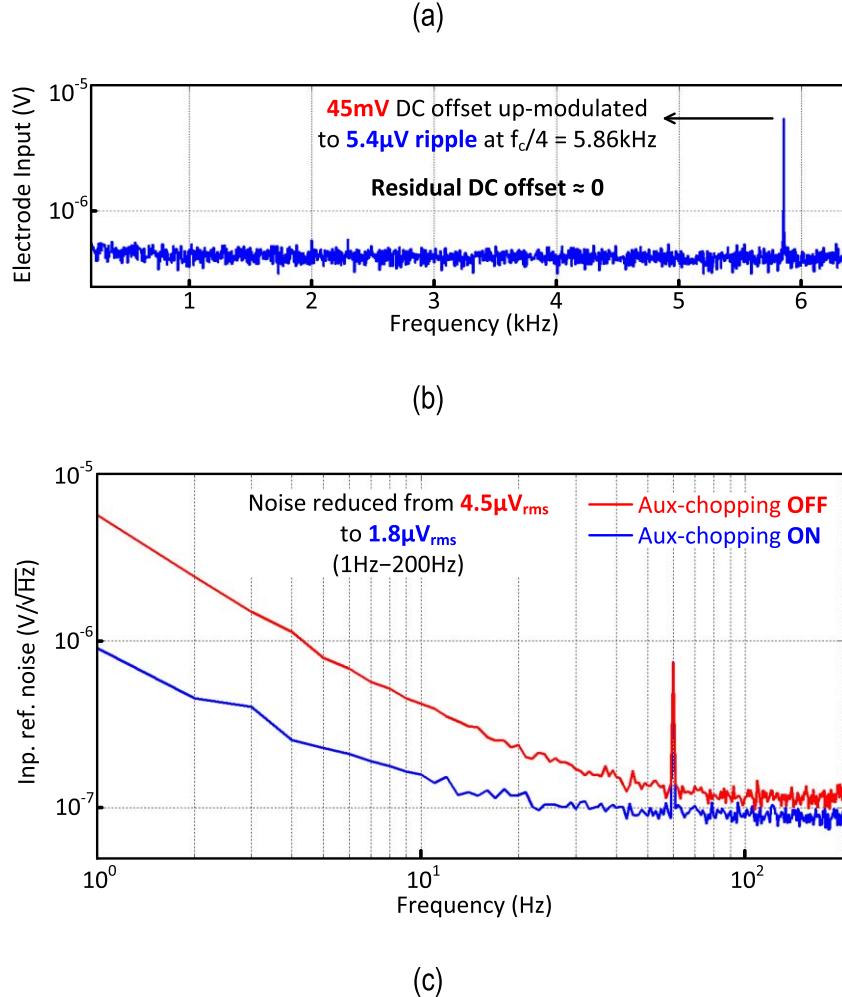


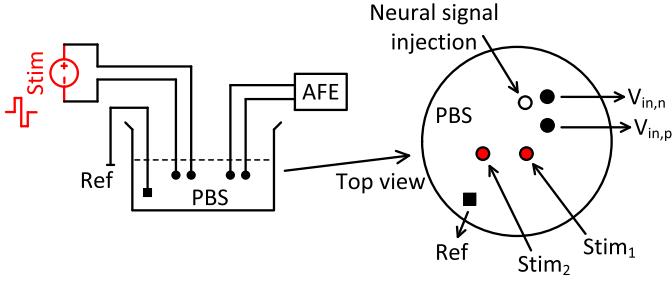
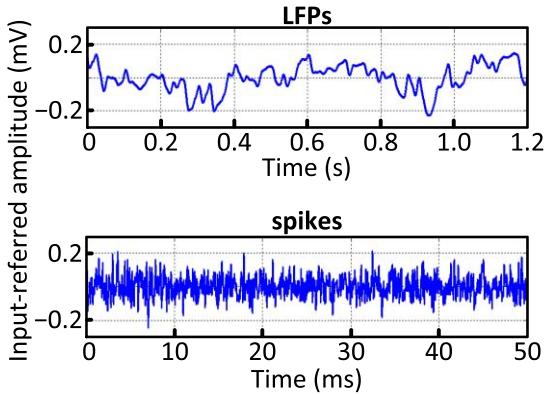
Fig. 21. Benefits of auxiliary-path chopping. (a) Large offsets observed at the electrode when aux-path chopping is disabled. (b) Measured electrode input when aux-path chopping was enabled. (c) Measured input-referred noise showing reduced aux-buffer flicker noise when auxiliary-chopping is enabled.

for completeness

$$Z_{in,DC} = \frac{1}{2C_{in}f_{clk}} \left( \frac{1}{1/A_{DC} + \exp(-T_1/\tau)} \right) = Z_0 \cdot \frac{A_{DC} \exp(T_1/\tau)}{A_{DC} + \exp(T_1/\tau)}. \quad (7)$$

In the above equation,  $\tau^{-1}$  rad/sec is the bandwidth of the auxiliary buffer, and  $A_{DC}$  is the open-loop dc gain of the buffer, which is usually around 40 dB. This implies that the maximum achievable boost to  $Z_{in}$  is limited to a factor of 100. To ensure that we get most of this impedance boost, the settling error due to the finite bandwidth of the auxiliary buffer must be minimized. This can be done by increasing

the transconductance of the auxiliary buffers, which would increase power consumption. A simple alternative is to use storage capacitors  $C_{aux}$  [Fig. 12(b)] to assist the auxiliary buffers [33]. At the beginning of the pre-charge phase [as shown in the timing diagram in Fig. 12(b)],  $C_{aux}$  is allowed to charge-share with  $C_{in}$ . If  $C_{aux}$  is sized to be significantly larger than  $C_{in}$ , then most of the pre-charging of  $C_{in}$  [labeled as  $\Delta V_{assist}$  in Fig. 12(a)] is complete in this charge-sharing phase. Hence the auxiliary buffers now only need to complete the remainder of the pre-charging of  $C_{in}$ . This reduces the settling error in the pre-charge phase, leading to a larger  $Z_{in}$  without increasing power consumption.  $C_{aux}$  was set to  $8 \cdot C_{in}$ , and the dc current in the auxiliary buffers was 150 nA. This was sufficient to provide an impedance boost by 2.7×, as we shall see in Section V. From Fig. 12(b), when  $\phi_{1,2} = 0$ , the auxiliary-buffer bias currents are reduced to 25 nA to

Fig. 22. *In vitro* measurement setup.Fig. 23. *In vitro* measurements using pre-recorded human neural recordings (no stimulation).

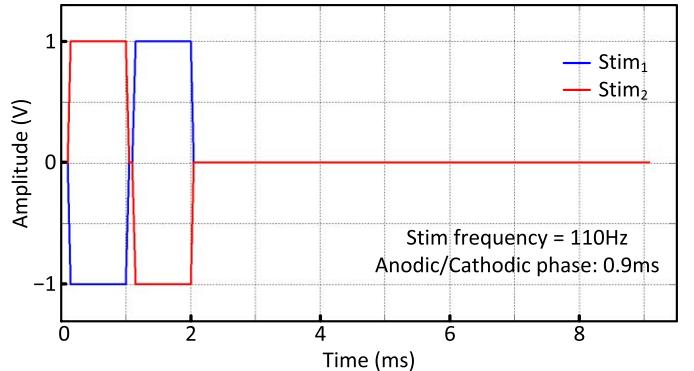
save power while ensuring that  $C_{aux}$  tracks  $V_{el}$  till the next pre-charge phase.

## V. EXPERIMENTAL RESULTS

The proposed Capacitively-coupled Chopper Instrumentation Amplifier (CCIA) is shown in Fig. 13(a), and the schematics for  $g_{m1}$  and  $g_{m2}$  are shown in Fig. 13(b). The amplifier was implemented in a 40-nm CMOS technology. Fig. 14 shows the chip micrograph and the measurement setup with provisions to emulate the electrode impedance. The amplifier occupies an area of  $0.069 \text{ mm}^2/\text{ch}$  and the total power consumed from a 1.2-V supply is  $2.8 \mu\text{W}$ . The transconductances  $g_{m1}$  and  $g_{m2}$  consume  $1.2$  and  $0.25 \mu\text{W}$ , respectively. The servo-loop, aux-path buffers, and the CMC path consume  $0.36$ ,  $0.2$ , and  $0.3 \mu\text{W}$ , respectively. Biasing and control-signal generation consumes  $0.45 \mu\text{W}$ .

The measured signal transfer function is shown in Fig. 15. The mid-band gain was  $25.7 \text{ dB}$  and the low-pass corner was  $5 \text{ kHz}$ . The servo-loop UGB sets the high-pass corner of the signal transfer function. From Fig. 13(a), we see that  $f_{HP} = 2f_{UB,DSL}$ . The high-pass corner  $f_{HP}$  was programmable from  $0.12$  to  $0.3 \text{ Hz}$  by varying the duty-cycle factor in the MDCR. The AAF corner frequency in the MDCR was chosen to be  $10 \text{ Hz}$  (Section IV-B). Hence, the pole associated with the AAF will be a nondominant pole since it is far away from the unity-gain frequency  $f_{HP}$  of the servo-loop, and the phase margin of the servo-loop will be close to  $90^\circ$  ensuring stability.

The measured input impedance of the front-end is shown in Fig. 16. When the auxiliary path was disabled,  $Z_{in}$  was

Fig. 24. Stimulation waveforms used for *in vitro* measurements.

$21 \text{ M}\Omega$ . When the auxiliary path was enabled,  $Z_{in}$  was boosted to  $600 \text{ M}\Omega$ , which further increased to  $1.6 \text{ G}\Omega$  when the auxiliary-buffer assistance was enabled. Hence  $Z_{in}$  has been boosted by a factor of  $76.2$ , with the storage capacitors  $C_{aux}$  providing a  $2.7\times$  boost.

The linearity measurements of the chopper amplifier are shown in Fig. 17. For a differential input sinusoid of  $40 \text{ mV}_p$  (or  $80 \text{ mV}_{pp}$ ) at  $1 \text{ kHz}$  with no CM interferer, the measured THD was  $-76 \text{ dB}$ . To measure the front-end performance in the presence of CM interference, we performed two-tone tests. Realistic stimulation artifacts have significant power at multiple harmonics of the stimulation frequency due to their pulse-like nature [29]. Hence, immunity to CM interference must be measured for frequencies up to several harmonics of the stimulation frequency. Stimulation is usually performed at frequencies below  $150 \text{ Hz}$ . Hence, we measure performance with CM interference up to  $900 \text{ Hz}$ . The two-tone test is conducted as follows. The differential input to the front-end consists of the sum of a  $40 \text{ mV}_p$  sinusoid at  $900 \text{ Hz}$  and a  $1-\text{mV}_p$  sinusoid at  $1 \text{ kHz}$ . A CM interferer of  $650 \text{ mV}_{pp}$  is also applied at  $900 \text{ Hz}$ . The  $900\text{-Hz}$  tones represent the stimulation artifacts, while the  $1\text{-kHz}$  tone represents the neural signal of interest. Fig. 18(a) shows the measured results of the two-tone tests. When the CMC path was disabled, we see significant distortion components at the output. We define the signal-to-interferer ratio (SIR) as the power of the desired signal (in this case, at  $1 \text{ kHz}$ ) divided by the power of the harmonics created by distortion. The SIR was only  $7 \text{ dB}$  when the CMC path was disabled. However, when the CMC path was enabled, there is significant suppression of the distortion components and the SIR improves to  $38 \text{ dB}$ . When the CM interferer was disabled, the SIR was  $44 \text{ dB}$ . Hence for a CM interferer of  $650 \text{ mV}_{pp}$ , the SIR degrades from  $44$  to  $38 \text{ dB}$  with the CMC enabled, a  $6\text{-dB}$  drop which we assume to be an acceptable degradation. Thus, our front-end can tolerate CM interferers up to  $650 \text{ mV}_{pp}$ . When the frequency of the stimulation tones is lowered to  $110 \text{ Hz}$  [Fig. 18(b)], the SIR improves from  $19.3$  to  $40.5 \text{ dB}$  when the CMC path is enabled. These measurements show the efficacy of the CMC path in maintaining linearity in the presence of large CM interferers. The CMRR and PSRR were also measured, and the results are shown in Fig. 19. The CMRR and PSRR

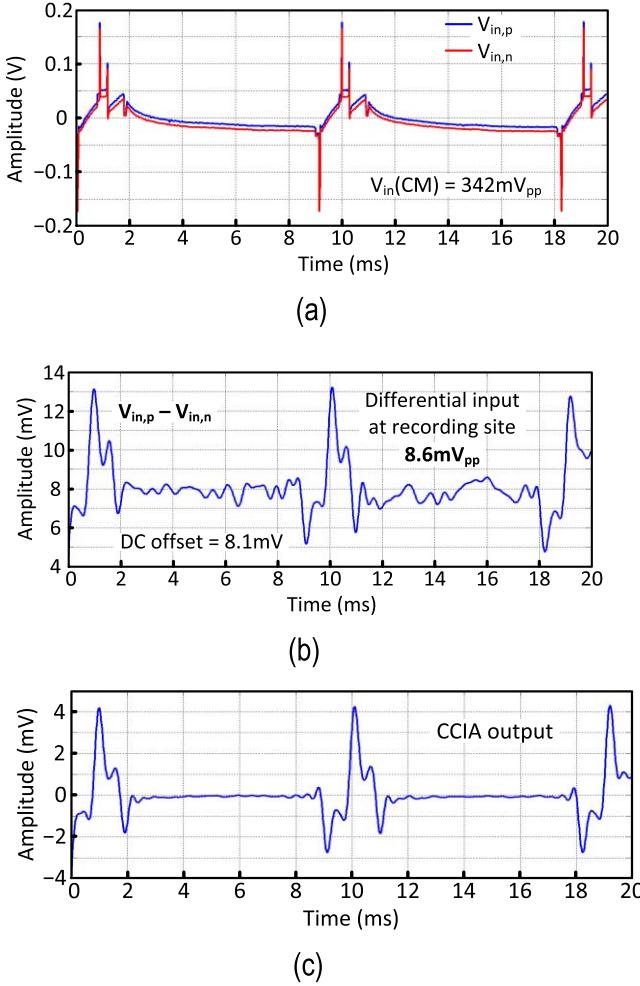


Fig. 25. Measured waveforms when differential stimulation is enabled without injecting pre-recorded neural signals. (a) Recording site waveforms. (b) Differential signal at recording site. (c) Measured output using CCIA (gain normalized to unity).

are better than  $-78$  and  $-76$  dB, respectively, in the signal band (1 Hz–5 kHz).

The input-referred noise was measured to be  $1.8 \mu\text{V}_{\text{rms}}$  in the LFP band (1–200 Hz), and  $5.3 \mu\text{V}_{\text{rms}}$  in the AP band (200 Hz–5 kHz), as shown in Fig. 20. To show the benefits of chopping in the auxiliary path, the offset appearing at the electrode was measured. When chopping in the auxiliary path (mixers \$M\_{1,2}\$ in Fig. 11) was disabled, large offsets were observed at the electrode [Fig. 21(a)], and the worst case offset was 45 mV. When the auxiliary-path chopping was enabled, the 45-mV offset reduced to zero and a  $5.4\text{-}\mu\text{V}$  ripple was observed at 5.86 kHz [see Fig. 21(b)]. This is expected from the discussions in Section IV-C. The input-referred noise in the 1–200 Hz band also reduced from 4.5 to  $1.8 \mu\text{V}_{\text{rms}}$  when the auxiliary-path chopping was enabled [see Fig. 21(c)].

*In vitro* measurements were performed using our front-end to record signals from electrodes dipped in phosphate-buffered saline (PBS). Fig. 22 shows the measurement setup. A pair of electrodes (\$\text{Stim}\_1\$ and \$\text{Stim}\_2\$) was used to deliver stimulation into the PBS solution, while another pair of electrodes (\$V\_{in,p}\$ and \$V\_{in,n}\$) were used as sensing electrodes

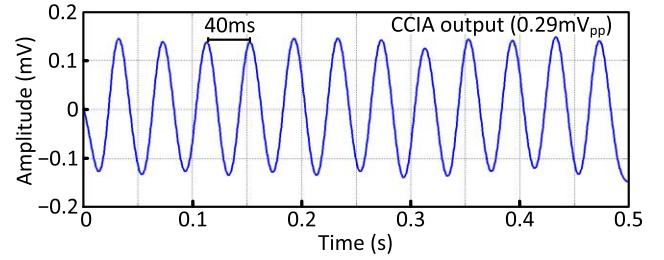


Fig. 26. Measured output (LP filtered up to 50 Hz) of CCIA during stimulation; A 25-Hz sinusoid was injected to represent a neural signal.

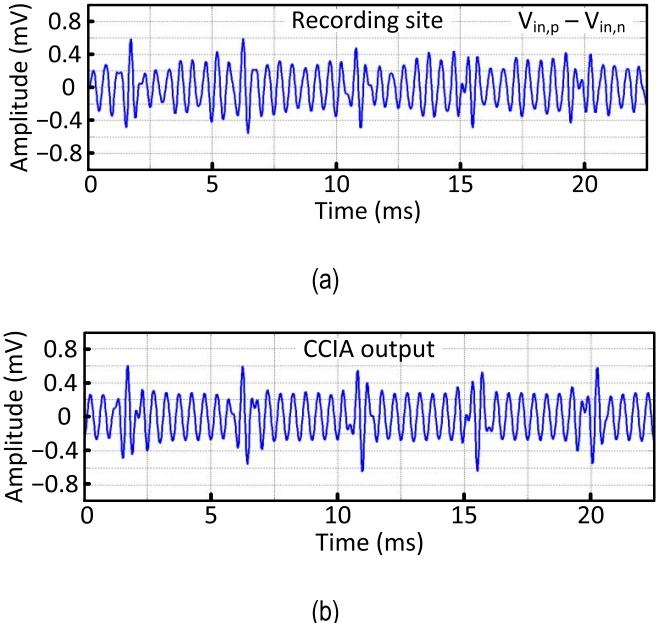


Fig. 27. Measured waveforms (HP filtered from 800 Hz) during stimulation. (a) Recording site. (b) CCIA output; A 1-kHz sinusoid was injected to represent a neural signal.

connected to our front-end. A separate electrode was used to inject neural signals into the PBS solution. Fig. 23 shows the measured output of the CCIA when pre-recorded human neural signals were injected while stimulation was disabled. To assess the magnitude of differential and CM artifacts due to stimulation, stimulation waveforms (Fig. 24) were injected into the PBS solution without neural signals, and the measured waveforms are shown in Fig. 25. The CM artifact at the recording site is  $342\text{mV}_{pp}$  [Fig. 25(a)], while the differential artifact is  $8.6\text{ mV}_{pp}$  [see Fig. 25(b)]. The measured output of the CCIA matches the differential artifact at the recording site as expected [see Fig. 25(c)]. Next, a 25-Hz sinusoid (representing a neural signal) was injected into the PBS solution along with the stimulation waveforms. The measured output of the CCIA, after LP filtering up to 50 Hz, shows a 25-Hz signal (see Fig. 26). The injected sinusoid frequency was changed to 1 kHz, and the corresponding measurements, after HP filtering from 800 Hz, are shown in Fig. 27. The differential signal at the recording site [Fig. 27(a)] matches the output of the CCIA [see Fig. 27(b)].

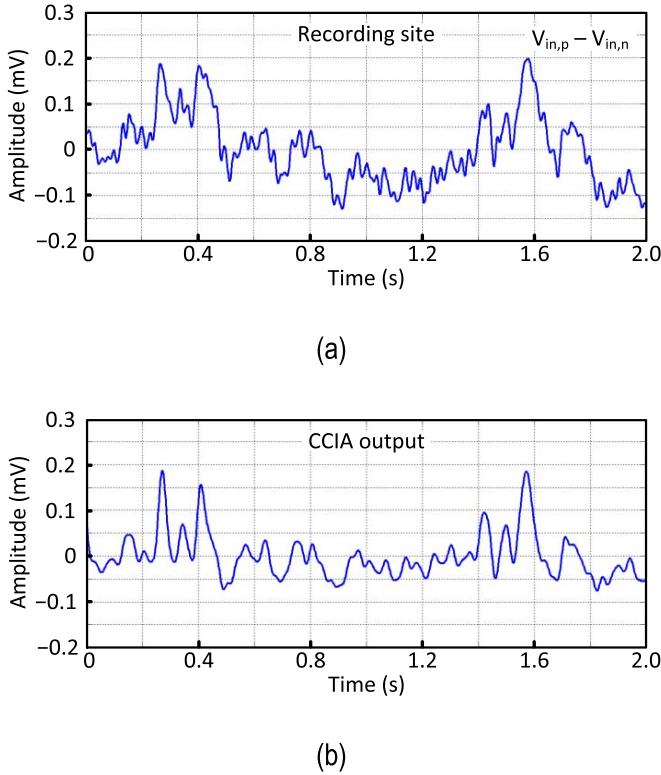


Fig. 28. Measured waveforms (LP filtered up to 50 Hz) during stimulation. (a) Recording site, (b) CCIA output; Pre-recorded human neural recordings were injected to emulate the neural signal.

Since the stimulation waveform has power at the harmonics of 110 Hz, the HP-filtered outputs show residual stimulation artifacts (see Fig. 27). Finally, the injected sinusoid is replaced with a pre-recorded human neural signal, and stimulation remains enabled. The measured waveforms (LP filtered up to 50 Hz) are shown in Fig. 28. The differential signal at the recording site [Fig. 28(a)] matches the CCIA output [see Fig. 28(b)]. Hence, the proposed front-end is capable of recording neural signals in the presence of stimulation artifacts.

Table II compares our work with the current state of the art. Our work improves  $Z_{in}$  by  $5.3\times$  for chopped front-ends, the linear-input range by  $2\times$ , the maximum resistance of DCRs by  $32\times$ , and introduces tolerance to 650-mV<sub>pp</sub> CM interferers, while maintaining comparable power and noise performance.

## VI. CONCLUSION

This work presents a chopper amplifier capable of closed-loop neural recording in the presence of large differential and CM stimulation artifacts. The assisted auxiliary-path technique enables our front-end to achieve a dc input impedance of  $1.6\text{ G}\Omega$ , removing the need for off-chip ac-coupling capacitors, making this front-end implantable. The linear input range is increased to 80 mV<sub>pp</sub> (with THD of  $-76\text{ dB}$ ) and the CMC path introduces tolerance to 650 mV<sub>pp</sub> CM interferers. The MDCR is introduced, which enables us to realize a much larger equivalent resistance ( $90\text{ G}\Omega$ ) as compared to the conventional DCR, allowing us to maintain low noise

and low area. Finally, the positive feedback problem in the auxiliary path has been addressed by introducing chopping in the auxiliary path. These improvements have been made while ensuring that our front-end achieves comparable power and noise performance to the state-of-the-art.

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