A 2.4-GHz 1.5-mW Digital Multiplying Delay-Locked Loop Using Pulsewidth Comparator and Double Injection Technique

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***Abstract*— In this paper, we propose a low-jitter low-power digital multiplying delay-locked loop (MDLL) with a self-calibrated double reference injection scheme. To reduce jitter, the noisy edge of the oscillator is replaced by both the rising and falling edges of the clean reference, which results in 6-dB reduction in phase noise compared with a conventional single-edge injection MDLL. Reference spur caused by a frequency error of the oscillator, duty-cycle error of the reference, and circuit imperfection, such as offset and mismatch, is removed by employing three background feedback loops with a shared analog pulsewidth comparator. Implemented in 28-nm CMOS, the proposed digital MDLL generates 2.4-GHz clock and achieves a spur of −51.4 dBc and an rms jitter of 699 fs_{rms} while consuming 1.5 mW from 1-V supply.**

***Index Terms*— Double injection, duty-cycle corrector (DCC), injection-locked oscillator, multiplying delay-locked loop (MDLL), offset cancellation, pulsewidth comparator (PWC), spur reduction, time-to-voltage converter (TVC).**

I. Introduction

LOW-JITTER low-power clock generation is becoming increasingly more important as electronic devices try to achieve higher performance and lower power consumption. Ring-oscillator-based clock generators are especially of much interest, as they require small silicon area compared with the LC-oscillator counterpart. Unfortunately, achieving a low-jitter clock from a ring oscillator is difficult due to the lack of high-Q components [1], and thus, jitter suppression must be obtained through an elaborate circuit design around the ring oscillator [2]–[4]. The most widely used solution to reduce jitter is to employ a phase-locked loop (PLL) that creates a high-pass filter for the oscillator phase noise. Although the PLL is effective in this regard, the amount of jitter suppression is limited by the PLL loop bandwidth, which must be less than a tenth of the reference frequency (i.e., $f_{ref}/10$) for a commonly used type-II PLL [5]. A promising technique that can overcome this bandwidth limitation is injection locking for LC oscillators [6]–[8] or multiplying delay-locked loop (MDLL) [9]–[14] for ring oscillators. In an MDLL, the accumulated jitter of the ring oscillator is periodically cleaned up by the reference as shown in Fig. 1, which effectively results in a large loop bandwidth. It is shown that the MDLL filters the phase noise of a ring oscillator with a bandwidth of about $f_{ref}/4$, which is 2.5× larger than the PLL maximum loop bandwidth [15].

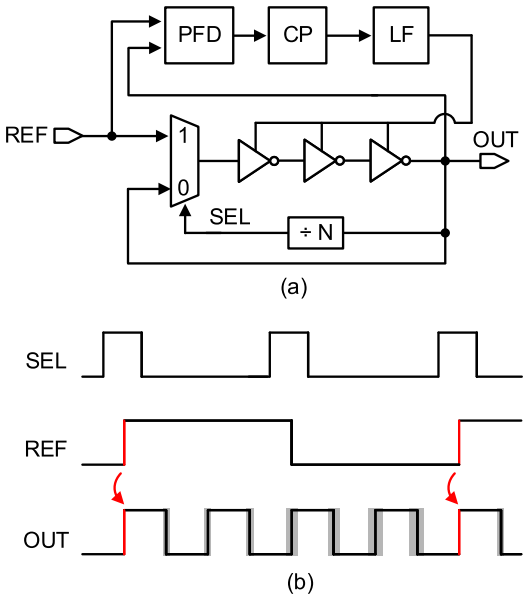

Fig. 1. (a) Block diagram and (b) timing diagram of a conventional MDLL.

As having a wide loop bandwidth is advantageous in reducing the phase noise of the oscillator, some of the previous MDLLs used high reference frequency and low multiplication factor [11], [12]. That is, if we increase the reference frequency by two times, then the filtering bandwidth is also increased by two times. Therefore, the phase noise of the ring oscillator at the output of the MDLL will be decreased by about 6 dB. For a given phase noise requirement, less power is necessary in

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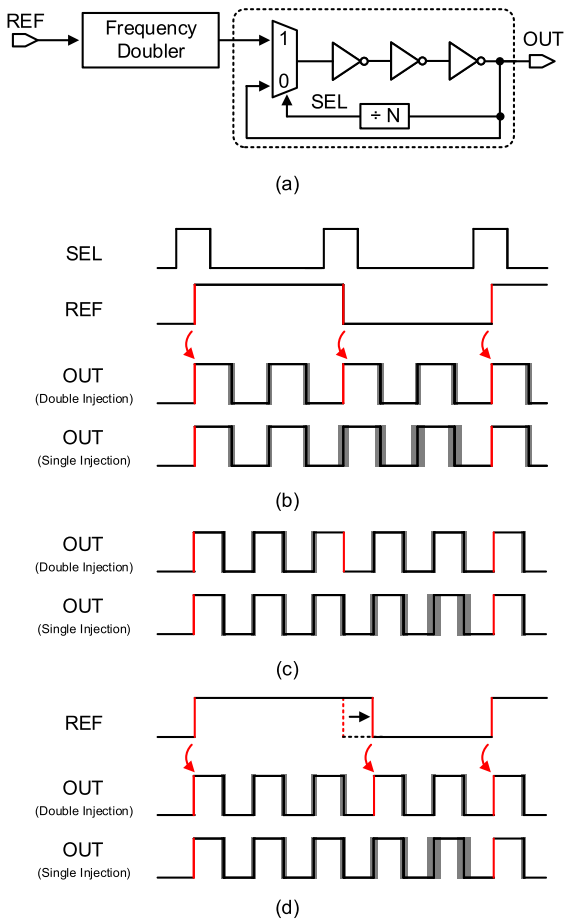

Fig. 2. (a) Concept of double edge injection. (b) Timing diagram of the double injection scheme in when N is even case. (c) When N is odd and reference edge replaces the falling edge of the VCO. (d) When N is odd and reference edge replaces the rising edge of the VCO.

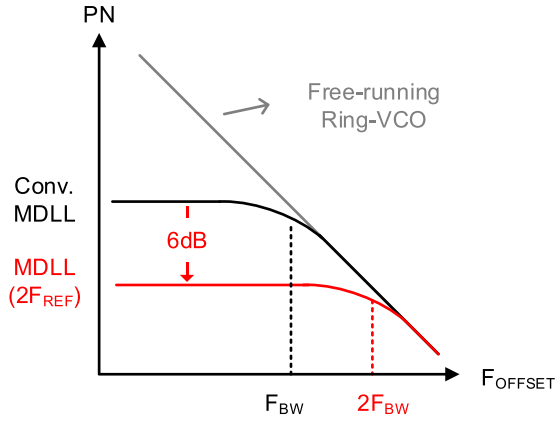

Fig. 3. Phase noise of the double injection technique.

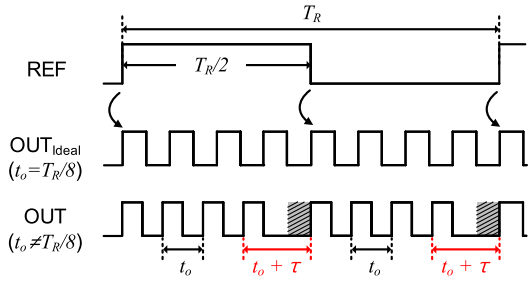

Fig. 4. Timing diagram when the frequency of the VCO is different from the desired frequency.

the oscillator. In this paper, a falling edge of the reference clock is exploited to double the reference and halve the division factor [13]. As a result, the MDLL bandwidth is increased to $f_{\text{ref}}/2$, which is twice that of the conventional MDLL and five times the PLL. In this paper, the reference doubled MDLL is explained in a more detailed manner and more experimental results.

The rest of this paper is organized as follows. The double injection technique is presented in Section II. Also, more details on background calibration using pulsewidth comparator (PWC) is explained in Section III. Then, the architecture of the proposed digital MDLL is introduced in Section IV. Next, the circuit implementation details of key building blocks are discussed in Section V. Section VI shows the experimental results obtained from the prototype chip implemented in 28-nm CMOS, followed by conclusions.

II. Double Injection Technique

The concept of the proposed double injection technique is shown in Fig. 2, where we assume that the multiplication factor, N, is 4 and the reference has 50% duty cycle and that the free-running frequency of the voltage-controlled oscillator (VCO) is exactly at four times the reference frequency. The reference clock goes into a frequency doubler, which basically changes the falling edges of the reference into the rising edges. These edges go into the MDLL, which replaces the noisy edge of the VCO not only with the rising edge but also with the falling edge. Therefore, the filtering bandwidth is doubled, and thus, the VCO phase noise can be suppressed by 6 dB more than a conventional MDLL, as shown in Fig. 3.

It is important to note that there is a couple of important assumptions that has been made. First is that the reference frequency has 50% duty cycle and second is that the VCO frequency is exactly four times the reference. If any of these conditions is not met, then the performance of the proposed MDLL will be degraded. Furthermore, circuit imperfections, such as offset, will worsen the problem.

In our prototype, the double injection technique is applicable only when N is even. However, it is possible to make it work for odd N as well. There are two ways of implementation. The first method is to use the falling edge of the reference to replace the falling edge of the VCO, as shown in Fig. 2(c). The second method is to change the duty cycle of the reference so that the falling edge of the reference edge replaces the rising edges of the VCO unevenly, as shown in Fig. 2(d) (e.g., for $N = 5$, the falling edge is inserted when the divider count is 3, and the next rising edge is inserted when the divider count is 5). The first method requires that the VCO output has 50% duty cycle, which will be difficult to guarantee. The second method requires a duty-cycle control circuit for the reference, which will be explained in Section III.

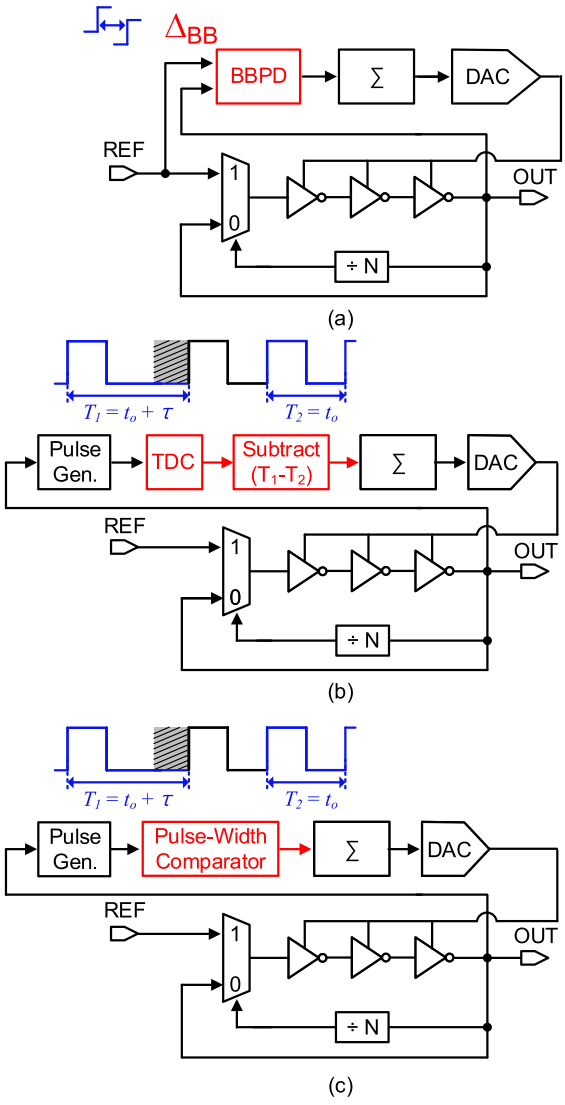

Fig. 5. Block diagram of (a) BBPD-based MDLL, (b) TDC-based MDLL, and (c) proposed MDLL using PWC.

III. Coping With Non-Idealities Using Analog Pulsewidth Comparator

A. Frequency Error

To look at how the non-idealities affect the performance, let us consider the first case when the VCO frequency is different from the desired target frequency as shown in Fig. 4, where T_R and t_o represent the period of the reference and the oscillator, respectively. It is assumed that the multiplication factor is 8 and $T_R/8 > t_o$. As can be seen, the output period of the VCO is abruptly changed when the reference edge is injected to the VCO, which results in a static phase offset of τ added t_o. Such a periodic change in the VCO output results in a large reference spur. Note that when the frequency error is positive, then the static phase offset τ is also positive and vice versa.

There have been previous works that provided solution to this frequency error [11], [14]. In [11], a bang-bang phase detector (BBPD)-based MDLL is proposed as shown in Fig. 5(a), where the BBPD detects the time difference between the VCO and the reference edge, and the feedback loop minimizes this time difference by controlling the VCO frequency to the desired value. The advantage of this scheme is that a low-power operation is possible by using a simple BBPD. However, its performance is limited by practical issues. First, the offset of a BBPD will limit the accuracy to which the VCO output and reference is aligned. Likewise, the parasitic RC delay mismatch between the BBPD and MUX paths will also limit the accuracy. This results in static phase offset that increases the reference spur. Previous works that rely on this scheme achieved the reference spurs of -55.6 dBc at 1.5-GHz output, which correspond to -51.5 dBc when the output frequency normalized to 2.4 GHz. In [14], a TDC-based MDLL is proposed as shown in Fig. 5(b), where the static phase τ is obtained using a high-resolution TDC. In this scheme, the output period of the VCO with and without the offset (i.e., T_1 and T_2) is quantized by the TDC and subtracted in a digital domain to achieve τ. Since there is only one TDC that is used to measure both T_1 and T_2, this paper does not suffer from offset or mismatch. It achieves a low reference spur of -54.7 dBc when normalized to 2.4 GHz. However, in order to obtain the static phase offset very precisely, a sub-picosecond high-resolution TDC is required, which consumes a large amount of power [14].

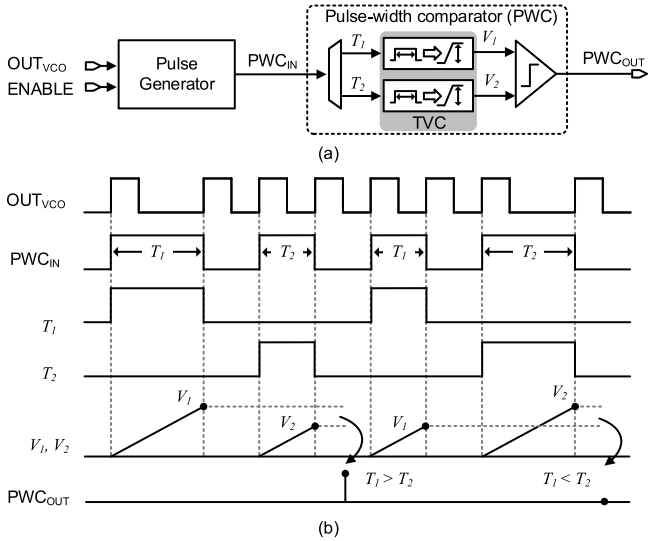

Fig. 6. (a) Block diagram and (b) timing diagram of the proposed PWC.

B. Pulsewidth Comparator

In this paper, we propose a low-power, low-spur technique that does not require high-resolution TDC and does not suffer from offset or mismatch. Our approach is similar to the TDC-based technique, which directly measures the output period. However, instead of using a high-resolution TDC and a digital subtractor to obtain the phase offset τ, an analog PWC is used, as shown in Fig. 5(c). It compares the pulsewidths in an analog fashion without quantization and produces binary out based on which pulse is larger or smaller. As high-performance TDC is not required, a low-power operation can be achieved.

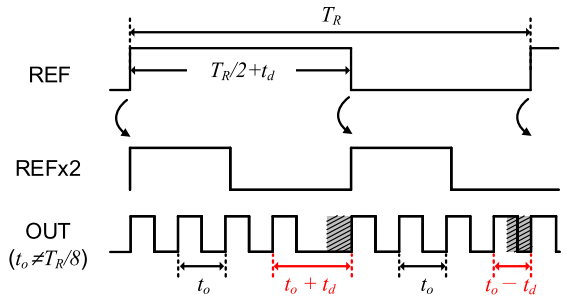

Fig. 7. Timing diagram when the reference clock does not have 50% duty cycle.

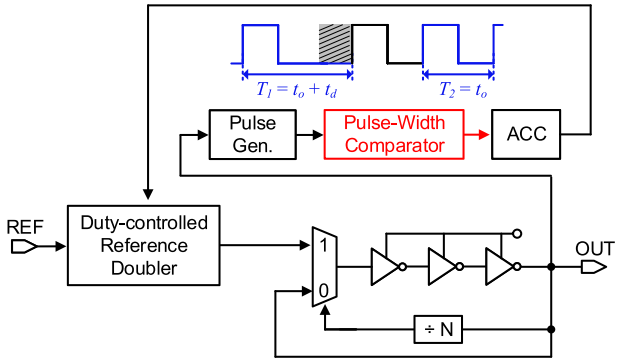

Fig. 8. Block diagram of the proposed MDLL using duty-controlled reference doubler.

A detailed operation principle of the PWC is shown in Fig. 6. The PWC is composed of two time-to-voltage converters (TVCs) and a comparator. First, a pulse generator produces pulses whose width is equal to the VCO period. Next, the pulses are converted into voltages proportional to the pulsewidths by the TVC and are compared by the voltage comparator. The PWC produces 1 or 0 depending on which pulse is wider, indicating whether the static phase offset and frequency error are positive or negative. The 1-bit output of the PWC is fed to a digital accumulator, which controls the VCO frequency so that two periods with and without the offset (i.e., T_1 and T_2) are the same, thus removing static phase offset and frequency error, as shown in Fig. 5(c). The PWC consumes much smaller power of 50 μW compared with the high-resolution TDC used in [14] that consumes 1.2 mW [14].

C. Duty-Cycle Error of the Reference Clock

If the reference clock does not have 50% duty cycle, there will also be change in the VCO period when the reference edge is injected, as shown in Fig. 7. Again, this will appear as a large reference spur in the output spectrum. Note that this will occur even when the VCO does not have a frequency error mentioned in the previous section.

To solve this issue, we propose a duty-controlled reference doubler to ensure that duty-cycle error does not appear at the output of the doubler. Similar to what is done to overcome the frequency error, the polarity of the duty-cycle time error t_d can be obtained by directly measuring the output periods of the VCO using the PWC. The effect of duty-cycle error can be removed by feeding the output of the PWC to

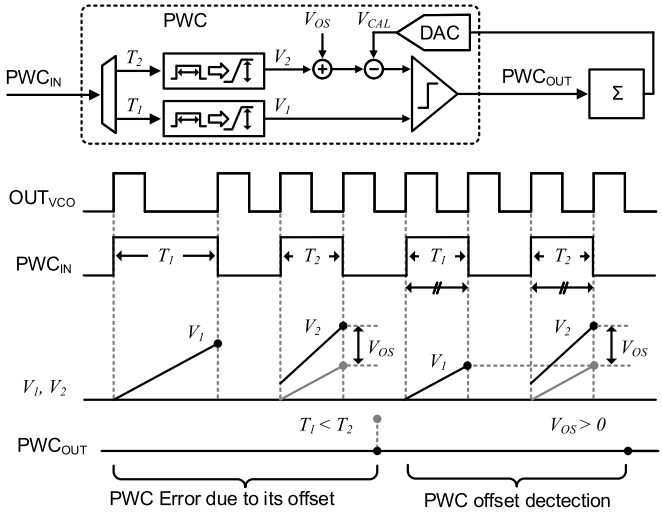

Fig. 9. Effect of PWC offset and offset calibration.

an accumulator, which controls the duty-cycle corrector in the reference doubler, as shown in Fig. 8. When the feedback loop settles, the duty-cycle time error t_d will be removed. Note that the PWC used for the duty-cycle correction (DCC) can be the same one used for the frequency error removal, and thus, a PWC can be shared by both the frequency and the duty-cycle error correction with appropriate timing.

D. Offset of the Pulsewidth Comparator

While the previously suggested techniques can remove the errors associated with frequency and duty cycle, their performance is limited to how accurately the circuits can be implemented in practice. Among various circuit imperfections, the offset in the PWC is especially important as it will cause errors in duty-cycle correction and frequency tuning. Note that the offset in the PWC is inevitable as there will be mismatch between the TVCs and offset in the comparator. To remove the PWC offset, an offset cancellation loop is proposed, as shown in Fig. 9. By exploiting the fact that there are VCO periods that are unaffected by the reference injection, we select these two pulses that inherently have the same pulsewidth. By putting these pulses into the PWC, the offset (V_{os}) can be detected and canceled by the feedback loop.

IV. Proposed Digital MDLL

A. Digital MDLL With Background Calibration Circuits

Based on the aforementioned techniques, a digital MDLL with duty-cycle corrected double injection technique can be implemented, as shown in Fig. 10. It consists of a reference doubler, an MDLL core, a pulse generator, an enable logic, the PWC, and three feedback loops that remove a frequency error, duty-cycle error, and offset all in background, while the MDLL is running. The MDLL core is composed of a VCO, a MUX select, and a divider. The noisy edge of the VCO is replaced by the output of the reference doubler that contains the rising and falling edges of the clean reference using a selection signal, SEL. Thus, the MDLL operates as

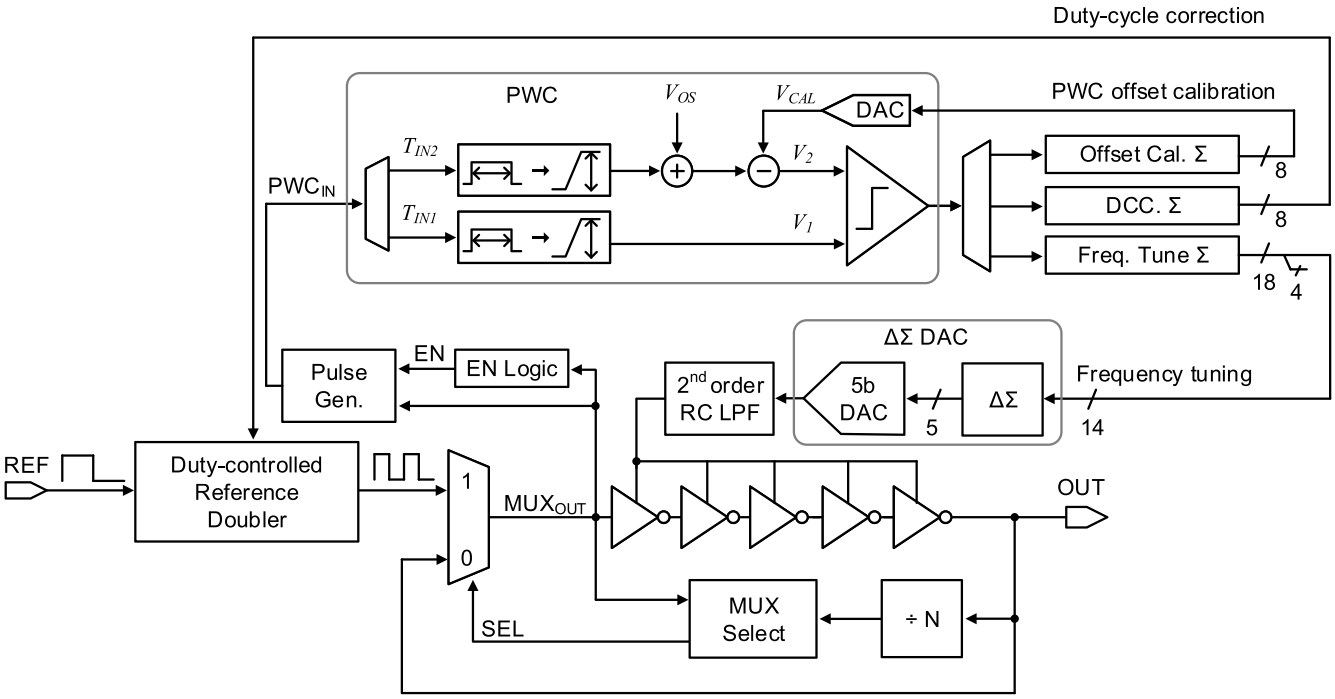

Fig. 10. Block diagram of the proposed MDLL with the double injection technique.

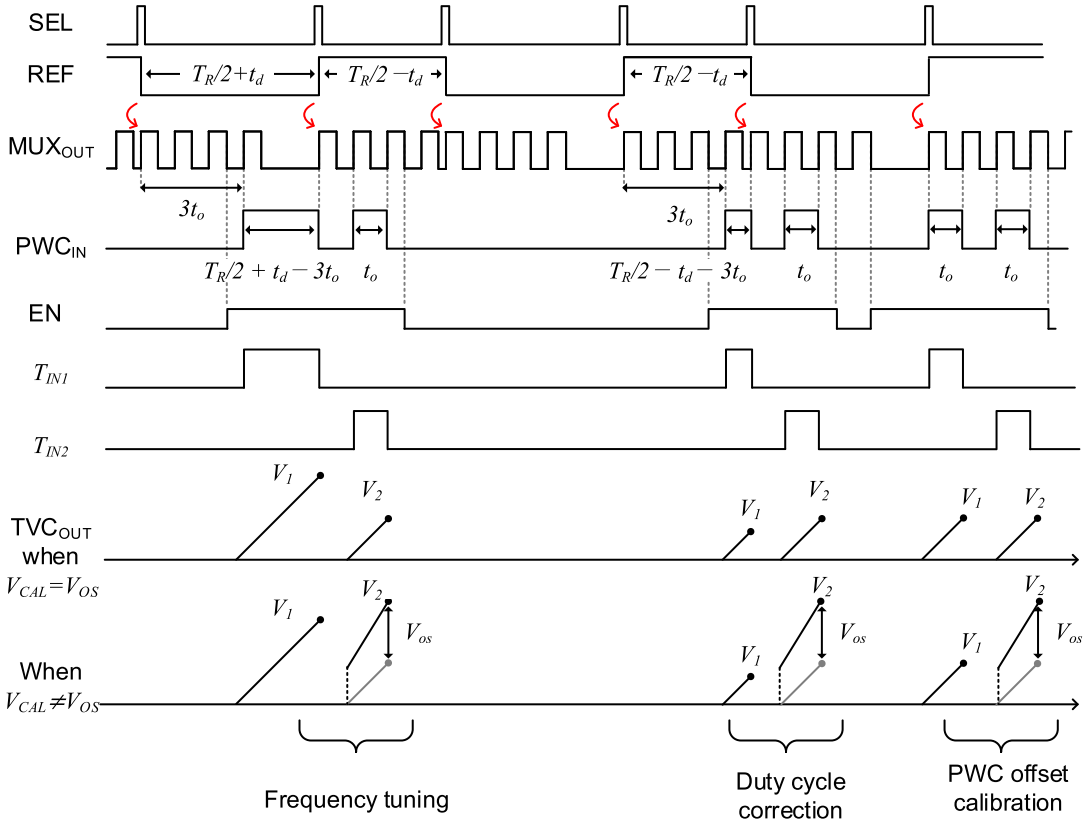

Fig. 11. Operation of the proposed MDLL with the double injection technique.

if the multiplication factor is halved of reference frequency doubled. The pulse generator changes MUX$_{OUT}$ into pulses when the enable signal, EN, is high. These pulses go into the PWC, and the outputs of the PWC are fed to the three feedback loops. The frequency of the VCO is controlled by a digital $\Delta\Sigma$ modulator and a 32-level current-mode DAC followed by the

second-order RC low-pass filter to reduce quantization noise from the $\Delta\Sigma$ modulator.

How the three calibration loops run in conjunction with each other is shown in Fig. 11, where T_R is the reference period, t_d is the duty-cycle time error, t_o is the VCO period, and $V_{\rm os}$ is the offset of the PWC in the voltage domain. It is assumed that the multiplication factor is 8. For VCO frequency tuning, the enable logic selects clock period when the rising edge of the reference is injected to the VCO (i.e., $T_R/2 + t_d - 3t_o$) and the period that follows (i.e., t_o). These periods are turned into pulses by the pulse generator and fed to the PWC where they are converted into voltage and compared with each other. The output of the comparator is fed to an accumulating loop filter that controls the VCO period, t_o, so that the two pulsewidths are equal, as described in the following, where $t_{\rm os}$ is the offset of the PWC in the time domain:

$$T_R/2 + t_d - 3t_o = t_o + t_{\rm os}. \tag{1}$$

Likewise for DCC, the enable logic selects the clock period when the falling edge of the reference is injected (i.e., $T_R/2 - t_d - 3t_o$) and the one that follows (i.e., t_o). The output of the PWC is accumulated and fed to the duty-controlled reference doubler, which corrects the duty cycle of the reference so that the two pulsewidths are equal as described in the following:

$$T_R/2 - t_d - 3t_o = t_o + t_{\rm os}. \tag{2}$$

For the offset calibration, two periods that are unaffected by injection are selected and compared. The output is accumulated and fed back to the DAC in the PWC so that $t_o = t_o + t_{\rm os}$. When all feedback loops settle, a solution to (1) and (2) is reached, which is $t_d = 0$, $t_o = T_R/8$, and $t_{\rm os} = 0$ indicating that duty-cycle error and offset are removed and the VCO is locked to the desired frequency. Note that the timing constraint of EN is that it must be set to high before the pulse ($\rm PWC_{IN}$) is generated by a margin of half a VCO period and it must be set to low when pulse is not generated by a margin of half a VCO period. Fortunately, this can be kept easily due to the fact that the enable logic and the pulse generator use the same clock source, $\rm MUX_{OUT}$.

The behavioral simulation result of the double-injected MDLL is shown in Fig. 12, where $\rm DCC_{IN}$, $\rm OFF_{IN}$, and $\rm FREQ_{IN}$ represent digital output code of the DCC, offset calibration, and frequency tuning accumulator, respectively. The initial condition of the circuits was $F_{\rm out} = 2450$ MHz, duty-cycle time error = 34 ps, PWC offset = 18 ps, and digitally controlled delay line (DCDL) and calibration step = 200 fs. Under these conditions, it can be seen that the offset correction loop settles first, while the duty-cycle correction loop (DCCL) and frequency tuning loop (FTL) settle together. This is because offset correction loop is independent of duty cycle or frequency error, while DCCL and FTL are affected by one another as can be seen in (1) and (2). Note that the reason why $\rm DCC_{IN}$ is initially stuck at zero is because there was an underflow in the DCC accumulator whose output range is from 0 to 255.

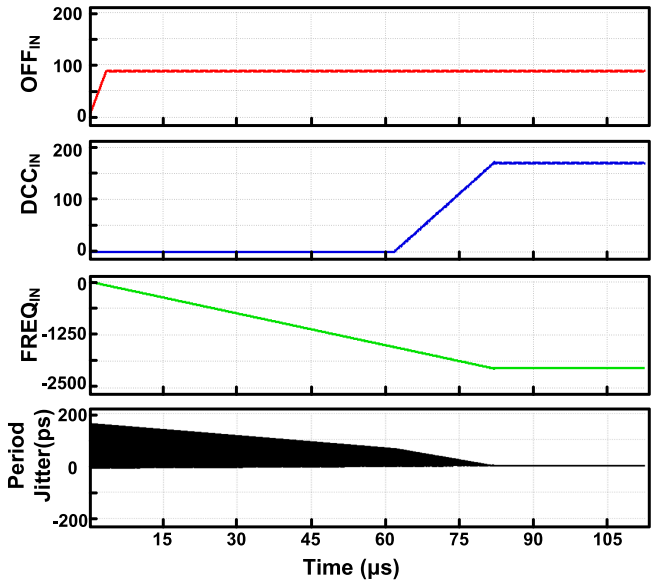

Fig. 12. Simulation result of the locking behavior of the double-injected MDLL.

B. Effect of Quantization Noise

In general, having a digital feedback loop introduces a quantization noise that affects the overall jitter performance. In the proposed MDLL, a quantization noise has three effects; it affects the in-band phase noise, creates limit cycle, and limits the amount of spur reduction. First, the in-band phase noise is largely determined by the quantization noise generated by the PWC in the FTL. To minimize the noise, the bandwidth of the FTL is aggressively lowered by minimizing dc gain of FTL and using the second-order RC low-pass filter following the $\Delta\Sigma$ DAC, as shown in Fig. 10. Unlike a PLL, such reduction in bandwidth will not affect the amount of VCO phase noise suppression due to reference injection. Second, the limit cycle is created in both the FTL and DCCL, since the FTL has a large loop delay caused by the second-order RC filter. Although the DCCL has negligible loop latency compared with the FTL, the limit cycle jitter of the FTL is also detected during duty-cycle correction and, thus, creates limit cycle in the DCCL as well. Hence, these limit cycles generate deterministic jitter at the output of both the reference doubler and the VCO. In the proposed DMDLL, the limit cycle is suppressed by discarding the last four LSBs of the 18-bit accumulator [16] and feeding the 14 bit to the $\Delta\Sigma$ DAC, as shown in Fig. 10. Note that the accumulator has been deliberately designed to have four more bits than necessary so that the resolution of the DAC does not degrade even if the 4 LSBs are thrown away. Last, the quantization noise of the MDLL limits the amount of spur reduction. In the proposed implementation, the resolutions of duty and offset correction are about 200 fs, and that for the FTL is about 150 fs. These values set a lower bound of spur to about −457 dBc, based on the following equation [17]:

$$\text{Spur} = 20\log_{10}\left(\frac{\text{Static phase offset}}{\text{T}_{\rm VCO}}\right). \tag{3}$$

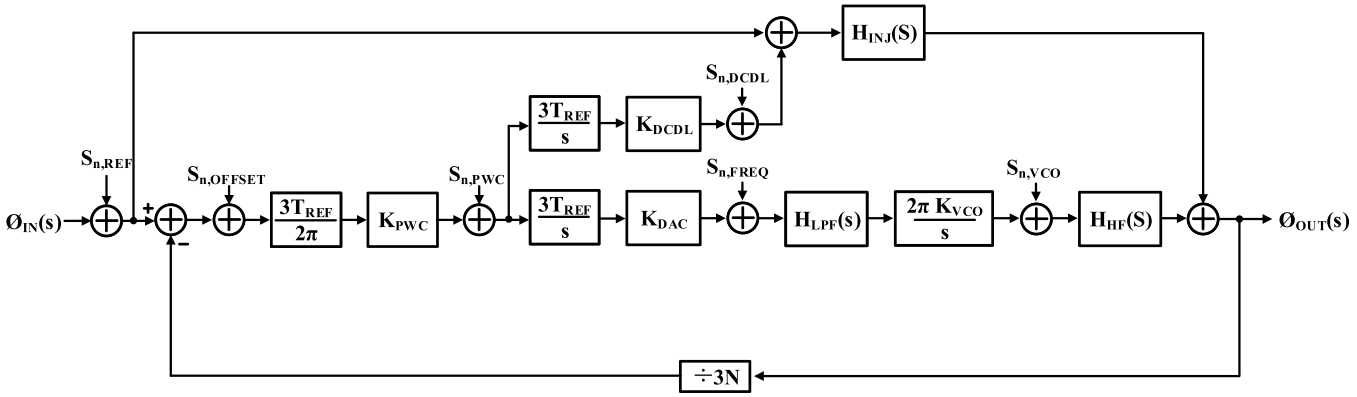

Fig. 13. Generalized model of the double-injected MDLL.

It should be noted that spur is also affected by other practical issues. For example, there are charge injection and switching noise in the select MUX that cause the phase shift of the VCO, which show up as the static phase offset.

C. Analysis of S-Domain Noise Model

The noise model of the proposed MDLL is shown in Fig. 13, where a reference injection model from [15] is adopted to our double injection scheme. Although the double injection technique can reduce the VCO phase noise by 6 dB, the noise introduced by the DCDL appears at the output of the VCO through the reference injection path. Therefore, the duty-cycle control loop (DCCL) and its noise are modeled in the reference injection path. Two H_{ACC} values represent integrator in the two feedback loops, and K_{DCDL} and K_{DAC} are the gain of DCDL and DAC, respectively. The noise of the PWC, DAC, and DCDL that include random and quantization noise is modeled as $S_{n,\mathrm{PWC}}$, $S_{n,\mathrm{DAC}}$, and $S_{n,\mathrm{DCDL}}$, respectively, while the noise of the reference and VCO is denoted as $S_{n,\mathrm{REF}}$ and $S_{n,\mathrm{VCO}}$, respectively. $H_{\mathrm{INJ}}(s)$ is the transfer function where reference and DCDL noise is upconverted due to reference injection and $H_{\mathrm{HF}}(s)$ is the transfer function of a high-pass filter of VCO due to reference injection [15]

$$H_{\mathrm{INJ}}(s) = \frac{N}{2} \times e^{\frac{-sT_{\mathrm{REF}}}{4}} \times \frac{\sin\left(\left|\frac{sT_{\mathrm{REF}}}{4}\right|\right)}{\left|\frac{sT_{\mathrm{REF}}}{4}\right|} \tag{4}$$

$$H_{\mathrm{HF}}(s) = 1 - e^{\frac{-sT_{\mathrm{REF}}}{4}} \times \frac{\sin\left(\left|\frac{sT_{\mathrm{REF}}}{4}\right|\right)}{\left|\frac{sT_{\mathrm{REF}}}{4}\right|}. \tag{5}$$

It can be seen that the due to double injection, $T_{\mathrm{REF}}/4$ instead of $T_{\mathrm{REF}}/2$ appears in the equation, and hence, the bandwidth of $H_{\mathrm{HF}}(s)$ is the twice that of the conventional MDLL [11]. In addition, the gain of $H_{\mathrm{INJ}}(s)$ is halved, which reduces reference noise upconverted at the MDLL output about 6 dB. Due to the reference injection which has much higher bandwidth than the DCCL and FTL, the output noise due to the reference and VCO is mainly determined by (4) and (5), respectively. The noise from DCDL, $S_{n,\mathrm{DCDL}}$, is upconverted to the output through the injection path, $H_{\mathrm{INJ}}(s)$. To minimize the quantization noise from DCDL, K_{DCDL} has been reduced. To lower the noise from PWC which is low-pass filtered by the FTL, K_{VCO} and K_{DAC} are designed to have a low value. Even though the PWC noise is integrated and upconverted through the DCCL and $H_{\mathrm{INJ}}(s)$, it is negligible at the output due to the reduced K_{DCDL}.

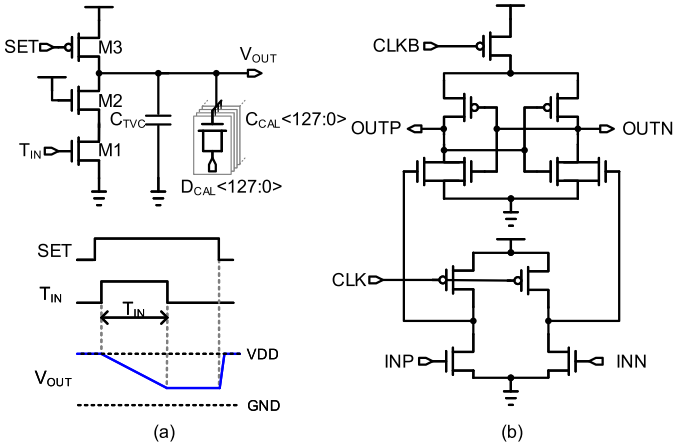

Fig. 14. Schematics of (a) TVC and (b) comparator.

V. Building Blocks

A. Pulse-Width Comparator

The PWC shown in Fig. 6 is composed of two TVCs and a comparator, whose circuit schematics are shown in Fig. 14. In the TVC, the input pulsewidth is converted into voltage by discharging a capacitor (C_{TVC}) that is pre-charged to supply [18]. It should be noted that the TVC is non-linear, as M1 and M2 are not an ideal current source. However, non-linearity of the TVC does not affect the operation of the proposed MDLL, since the correction loop only detects the polarity whether a pulsewidth is larger or smaller than the other. The comparator that follows the TVC is based on a voltage sense amplifier proposed in [19]. The clock signal for the comparator is the divided clock of MDLL output whose frequency is the same as F_{REF}.

The offset of the PWC is caused by comparator offset and the mismatch between the two TVCs that lead to different TVC gains. Both of these can be removed by an 8-bit capacitor

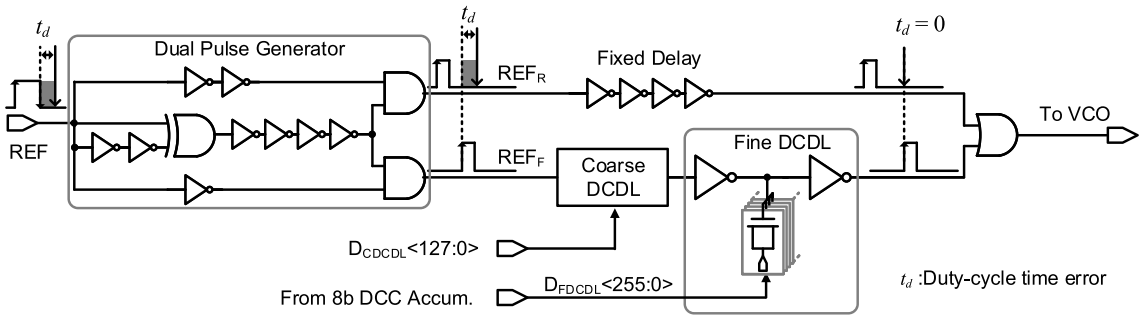

Fig. 15. Schematics of the duty-controlled reference doubler.

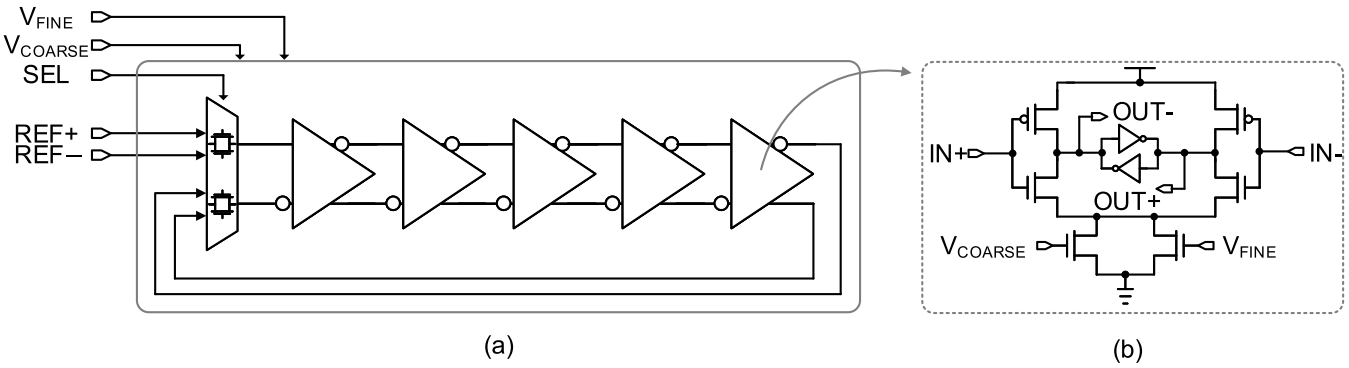

Fig. 16. Schematics of (a) voltage-controlled ring oscillator and (b) delay cell.

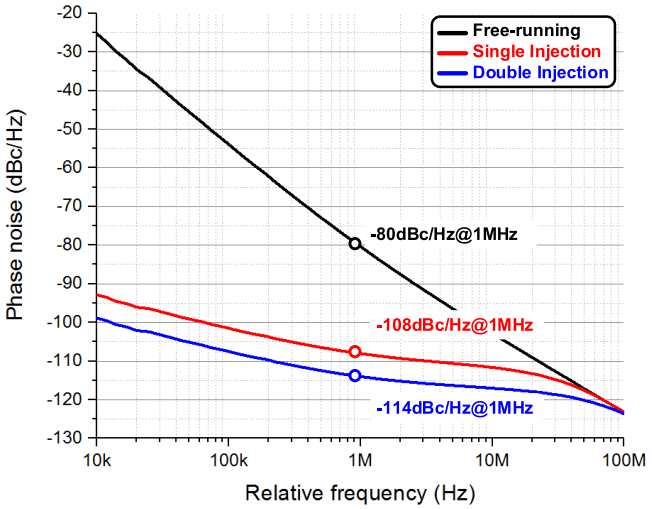

Fig. 17. Simulated phase noise for the VCO in single and double injection mode.

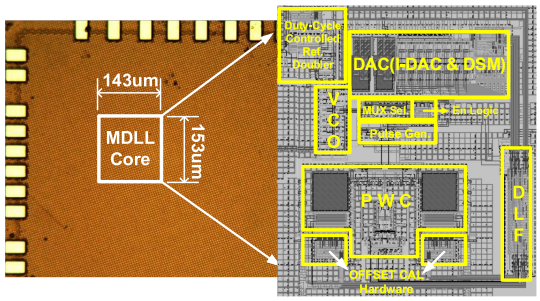

Fig. 18. MDLL die photograph.

array in the TVC, which is controlled by the offset calibration loop. The calibration range is about 51 ps to cover the three-sigma variation of the PWC offset, and the calibration resolution is set to about 0.2 ps/LSB. Such resolution was chosen so that it is below the random noise of the PWC, which is about 0.24 ps in the time domain from simulation. The proposed PWC consumes about 50 μW that is much lower than the technique shown in [14], which requires a high-resolution and wide dynamic range TDC that consumes a large power of 1.2 mW. Note that the proposed PWC will consume low power in other CMOS processes above 28 nm, since the circuit power is dominated by charging the load capacitor (C_{TVC}) of 1 pF.

B. Duty-Cycle-Controlled Reference Doubler

The circuit schematic of the duty-controlled reference doubler is shown in Fig. 15. It is composed of a dual pulse generator and a DCDL. By using two AND gates and an XOR-based frequency doubler, pulse from the rising and falling edges is separated. The pulse due to rising edge goes through a fixed delay of about 700 ps, while the pulse due to falling edge goes through a series of coarse and fine DCDL, which is controlled by the duty-cycle correction loop so that the final output exactly has twice the reference frequency. Similar to the TVC, the DCDL is implemented using an 8-bit

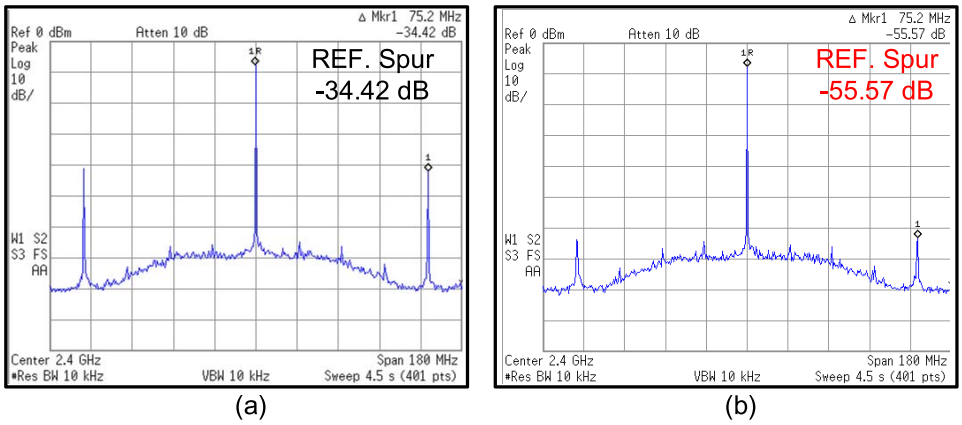

Fig. 19. Measured spectrum of the single injection spectrum when the PWC offset calibration is enable or disable.

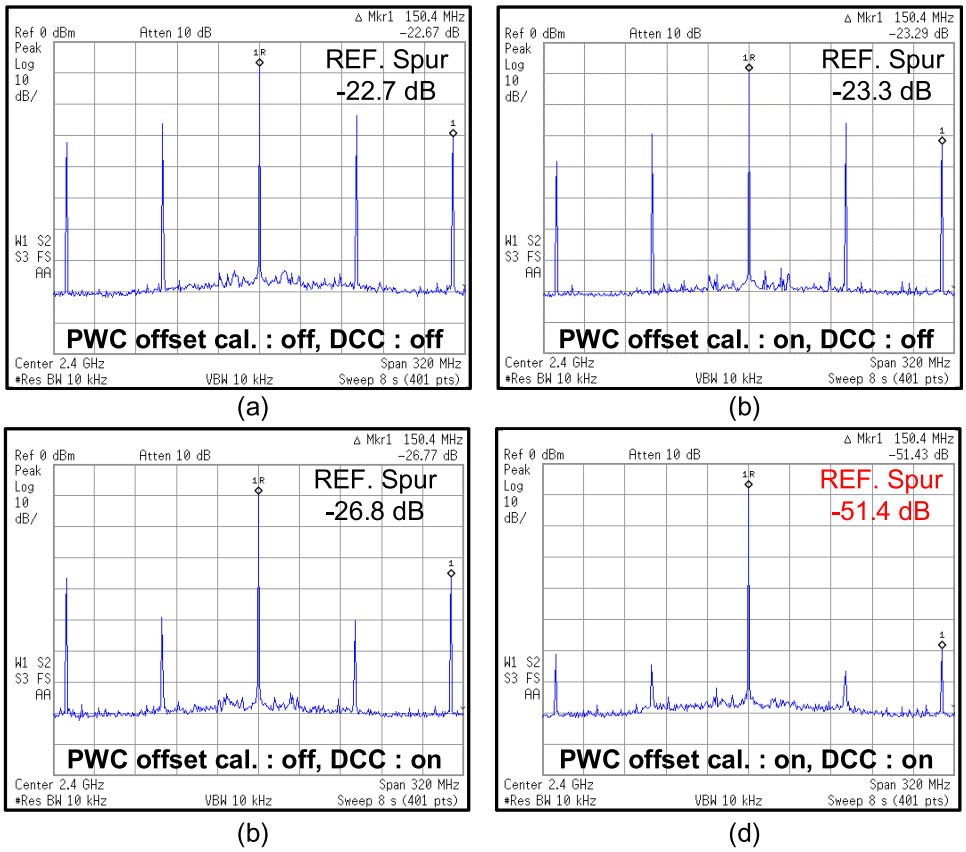

Fig. 20. Measured spectrum of the double injection spectrum when the DCC and the PWC offset calibration is enable or disable

capacitor array. The resolution of the fine DCDL is set to about 0.2 ps/LSB to reduce a quantization error below random jitter. The 8-bit coarse DCDL is composed of NAND-based delay cell and its resolution is set to 30 ps to cover the total dynamic range of the fine DCDL.

C. Voltage-Controlled Ring Oscillator

The schematic of the VCO is shown in Fig. 16. It is composed of a transmission gate-based multiplexer and five stages of pseudodifferential delay cells. The pseudodifferential delay cells are implemented using CMOS inverters coupled by latches for differential operation. Frequency tuning is achieved by two NMOS tail transistors of a different size controlled by coarse and fine frequency tuning words, where the coarse is for wide tuning range, and the fine is for the MDLL frequency correction loop. The small gain of the fine-tuning words makes it easy to reduce the loop bandwidth of the MDLL tuning loop, which helps to reduce the degradation of phase noise. The simulated phase noise plots of the ring oscillator at 2.4 GHz in free running, single injection, and double injection are shown in Fig. 17. The VCO phase noise

TABLE I
MEASURED POWER BREAKDOWN

Block	Power	Ratio
Duty-cycle controlled Ref. Doubler	$87\mu W$	6%
Freq. tuning DAC	$108\mu W$	7%
MUX Select and Enable logic	$110\mu W$	7%
Pulse generator	$63\mu W$	4%
Digital loop filter	$18\mu W$	1%
Time-to-voltage converter	$35\mu W$	3%
Comparator	$15\mu W$	1%
VCO	$1080\mu W$	71%
Total	$1.51mW$	100%

is −80 dBc/Hz at 1-MHz offset while consuming 1 mW, which results in an FOM of −148 dBc/Hz. With an estimated MDLL loop bandwidth of 18.75 MHz for single reference injection, the phase noise at 1 MHz is expected to decrease by about 28 dB to −108 dBc/Hz. When double injection is enabled, 6 dB more suppression is expected, which would result in −114 dBc/Hz according to Fig. 17.

VI. EXPERIMENTAL RESULTS

The proposed MDLL has been fabricated in a 28-nm CMOS process, and the die photograph is shown in Fig. 18. It occupies an active area of 143 × 153 μm^2. Note that the PWC offset calibration, including DAC and decoder, occupies 1020 μm^2, which means that the calibration loop occupy 4% of the total active area, as shown in Fig. 18. The prototype chip receives 75-MHz reference clock from an external crystal oscillator and multiplies it by 32, producing a 2.4-GHz output. It runs under a power supply of 1 V and consumes 1.51 mW, where 1.08 mW is consumed in the VCO, 87 μW is consumed in the duty-controlled reference doubler and 50 μW is consumed in the PWC. A breakdown of the power is summarized in Table I, where it can be seen that the additional hardware to achieve reference double injection consumes less than 10% of the overall power.

The prototype chip has first been tested in a single injection mode, and thus, the reference doubler and duty-cycle correction loop are unnecessary and disabled. The measured output spectrum of the proposed DMDLL is shown in Fig. 19, when the background PWC offset calibration is enable and disabled. It has been measured using Keysight Spectrum Analyzer E4404B. It should be note that the FTL is running in both cases to ensure correct frequency output. Due to the PWC offset that result from mismatch between the two TVCs and comparator offset, a large reference spur of −34.42 dBc at 75-MHz offset can be seen in Fig. 19(a), which is when the PWC offset calibration is disabled. The PWC time offset is estimated as 8 ps based on (3). On the other hand, the reference spur is suppressed to −455.57 dBc when the PWC offset calibration technique is enabled. Even though the offset calibration enabled, a lower bound of the static phase offset exists due to the resolution of FTL and offset calibration. The calculated static phase offset is 0.7 ps based on (3), which is

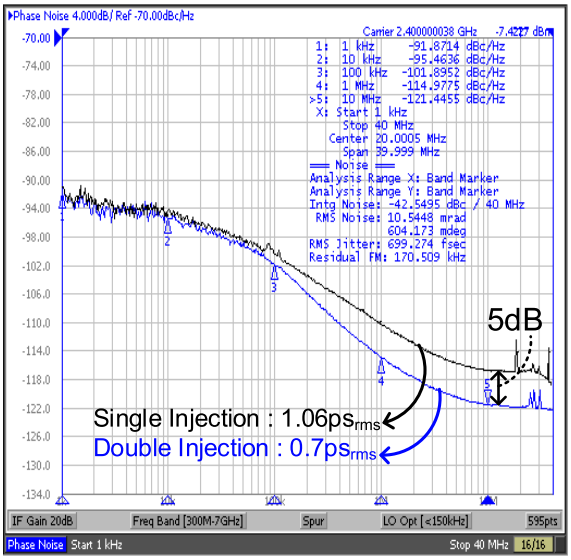

Fig. 21. Measured phase noise of the MDLL output when the double injection technique is enable or disabled.

larger than a lower bound from a simulation result, 0.35 ps. Next, the prototype chip is tested for double injection scheme, which includes reference doubler and duty-cycle calibration loop. The measured spectrum of the reference double-injected DMDLL is shown is Fig. 20, when DCC and PWC offset calibration are enabled and disabled, with the FTL running in background. The spurs at 150 and 75 MHz are due to the doubled reference and duty-cycle error, respectively. When both calibration loops are enabled, spurs at 150 and 75 MHz are reduced from −22.7 and −16.7 to −51.4 dBc and −58 dBc, respectively. The calculated duty-cycle time error is 56 ps according to Fig. 20(b) where the spur level at 75 MHz is −17.4 dBc. This is because the spur level at 75 MHz indicates the duty-cycle time error of the reference. The duty-cycle time error is reduced to 0.5 ps, and the static phase offset is decreased to 1.1 ps according to Fig. 20(d) when all calibration is ON. The measured phase noise and integrated rms jitter from 1 kHz to 40 MHz are shown in Fig. 21, when the proposed double injection is enabled and disabled. It was measured by Keysight Signal Source Analyzer 5052A. It can be seen that the double injection technique suppresses the out-of-band phase noise by about 5 dB, which is close to the theoretical value and reduces the integrated rms jitter from 1.07 to 0.7 ps$_{rms}$. The time-domain jitter of the proposed digital MDLL has also been measured using Keysight Oscilloscope DCA-J86100C with jitter measurement option enabled, as shown in Fig. 22. By taking the measurement jitter of 1.4 ps into account, the jitter of the MDLL is about 1 and 0.6 ps for single and double-injected MDLL, respectively, which shows similar results compared with the phase noise measurement.

The performance of the proposed DMDLL is compared with other state-of-the-art MDLLs in Table II. Recently, the proposed double injection technique was also used in injection-locked clock multiplier in [22]. The concept of double injection and background DCC technique is almost the same except for the way of positioning the reference edges.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	This Work			[11]	[12]	[14]	[20]	[21]	[22]	
Technology	28nm			130nm	65nm	130nm	65nm	65nm	65nm	
Output freq.[GHz]	2.4			1.5	4.6	1.6	1.6	1.2	5	
Ref freq.[MHz]	75			375	575	50	50	120	125	
Multiplication factor	32			4	8	32	32	10	40	
Injected reference edge	Rise and fall		Rise	Rise	Rise	Rise	Rise	Rise	Rise and fall	
Ref. spur[dBc]	@75M	@150M	-55.6	-55.6	-46	-58.3	-55.3	-53	@125M	@250M
	-58	-51.4							-53.5	-46
Ref. spur normalized to F_{OUT} = 2.4GHz	@75M	@150M	-55.6	-51.5	-51.1	-54.7	-51.8	-47	@125M	@250M
	-58	-51.4							-60	-53.5
Integ RMS jitter[ps]	0.7		1.08	0.4	N/A	0.68	0.47	0.185	0.34	
In-bang phase noise [dBc/Hz] @10kHz	-95.5		-95	-97.5	N/A	-98	-106 @30kHz	-120	-100	
Total Power(P_{TOTAL})	1.51mW		1.45mW	0.89mW	6.8mW	9.2mW	2.4mW	9.5mW	5.3mW	
Osc. Power(P_{OSC})	1.08mW		1.08mW	0.29mW	N/A	3.1mW	1.4mW	N/A	N/A	
P_{OSC}/P_{TOTAL}x100[%]	72		74	32	N/A	33	58	N/A	N/A	
Power without Osc.	0.43mW		0.37mW	0.6mW	N/A	6.1mW	1mW	N/A	N/A	
Implementation	DMDLL			BB-DMDLL	AMDLL	TDC-DMDLL	DMDLL	ILPLL	DILPLL	
Area[mm^2]	0.024			0.25	0.025	0.76	0.09	0.06	0.09	

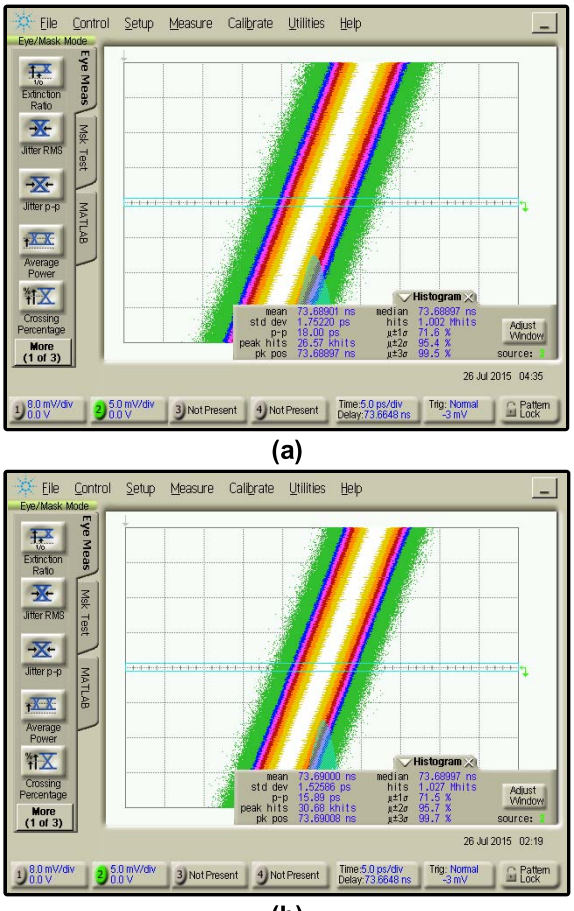

Fig. 22. Measured jitter of the MDLL output when the double injection technique is enable and disabled.

Both the rising edges and falling edges are controlled by fine DCDL in [22]. On the other hand, only the falling edges are controlled by fine DCDL in the proposed work. In addition, a spur reduction technique [23] is used for an FTL in [22]. However, the PWC-based spur reduction technique [13] is proposed for an FTL in this paper. In terms of a spur performance, [22] is slightly better than the proposed work about 1–2 dBc. Note that in our work, a large portion of the total power is consumed in the oscillator to reduce the effect of large $1/f$ noise in a 28-nm process, since the effective loop bandwidth of our design was limited by a larger multiplication factor and smaller reference frequency. It can be seen that the proposed double injection and calibration scheme using PWC is very effective in achieving low-power, low-jitter, and low-spur DMDLL with a large multiplication factor.

VII. CONCLUSION

In this paper, we presented a low-jitter low-power MDLL with a double reference injection scheme using an analog PWC. The bandwidth of the proposed MDLL is a twice that of the conventional MDLLs due to the double injection scheme. Non-idealities, such as frequency error, duty-cycle error, and offset, are eliminated using a background self-calibration. The proposed MDLL achieves a spur of −51.4 dBc and an rms jitter of 0.7 ps_{rms} while consuming 1.51 mW at 2.4 GHz.

While these numbers are the state of the art, the proposed work has some room for improvement. First, it was found through exhaustive verifications that the limitation in spur is primarily due to the coupling between the MUX and VCO when MUX changes its input from the VCO to the reference. We believe that an on-chip supply regulation and VCO shielding will improve the spur. Second, the proposed PWC is not a differential circuit and, thus, is sensitive to supply noise. While a regulator could solve this issue, a differential circuit is ultimately desired in the future research.

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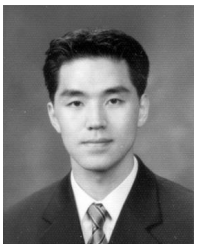

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