Patent Abstracts

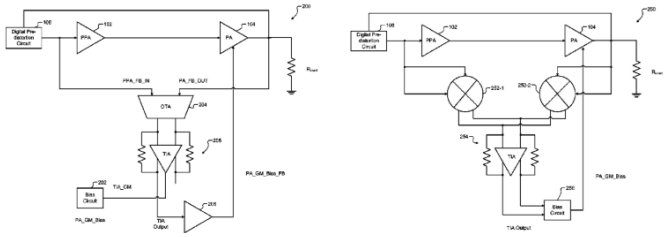
The Patent Abstracts cited are intended to provide the minimum information necessary for determining interest. The full text and images can be obtained from the U.S. Patent Office at http://www.uspto.gov.

9,385,666 July 5, 2016

Power Amplifier With Wideband AM–AM Feedback and Digital Predistortion

Inventors: Sai-Wang Tam (Sunnyvale, CA), Alden Chee Ho Wong (Hayward, CA), Yuan Lu (Sunnyvale, CA), David M. Signoff (Santa Clara, CA), Li Lin (Saratogoa, CA)
Assignee: Marvell World Trade Ltd. (St. Michael, BB)
Filed: December 3, 2014

Abstract— A system including an amplifier circuit configured to amplify an input and generate an output, a bias circuit configured to bias the amplifier circuit, and a feedback circuit configured to generate feedback based on the input and the output, and to adjust the bias of the amplifier circuit based on the feedback to reduce amplitude nonlinearity in the output. A digital predistortion circuit is configured to reduce phase nonlinearity in the output.

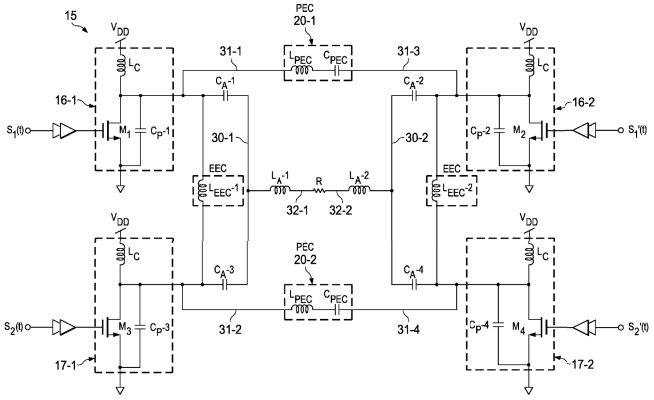


9,385,669 July 5, 2016

Class-E Outphasing Power Amplifier With Efficiency and Output Power Enhancement Circuits and Method

Inventors: Aritra Banerjee (Dallas, TX), Joonhoi Hur (Dallas, TX), Baher Haroun (Allen, TX), Nathan Richard Schemm (Rowlett, TX), Rahmi Hezar (Allen, TX), Lei Ding (Plano, TX)
Assignee: Texas Instruments Incorporated (Dallas, TX)
Filed: June 23, 2014

Abstract— An outphasing amplifier includes a first class-E power amplifier (16-1) having an output coupled to a first conductor (31-1) and an input receiving a first RF drive signal [S.sub.1(t)]. A first reactive element (C.sub.A-1) is coupled between the first conductor and a second conductor (30-1). A second reactive element (L.sub.A-1) is coupled between the second conductor and a third conductor (32-1). A second class-E power amplifier (17-1) includes an output coupled to a fourth conductor (31-2) and an input coupled to a second RF drive signal [S.sub.2(t)], and a third reactive element (C.sub.A-3) coupled between the second and fourth conductors. Outputs of the first and second power amplifiers are combined by the first, second, and third reactive elements to produce an output current in a load (R). An efficiency enhancement circuit (L.sub.EEC-1) is coupled between the first and fourth conductors to improve power efficiency at back-off power levels. Power enhancement circuits (20-1,2) are coupled to the first and fourth conductors, respectively.



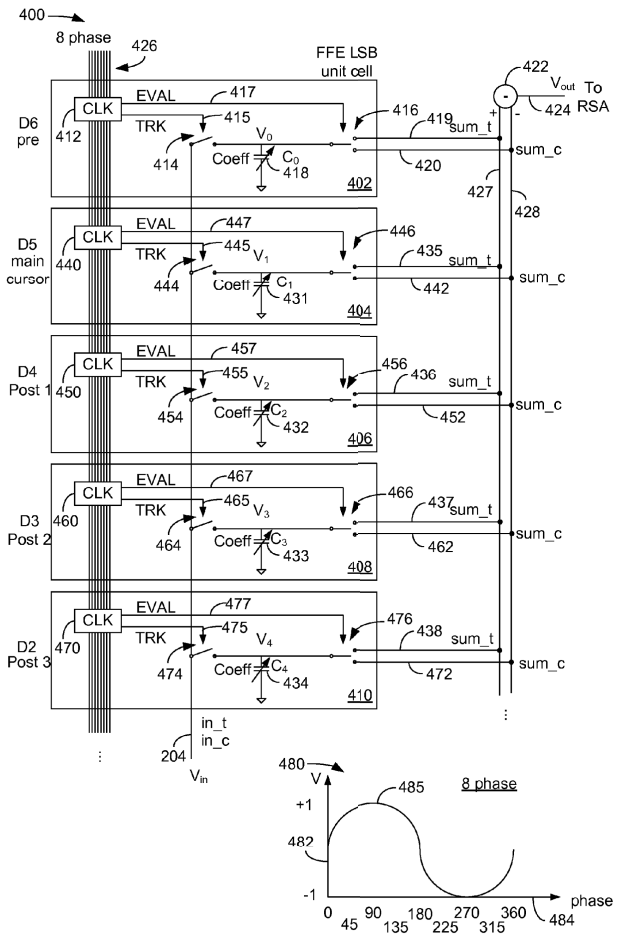
9,385,898 July 5, 2016

Pipelined Programmable Feedforward Equalizer (FFE) for a Receiver

Inventors: Jade Michael Kizer (Windsor, CO), Robert B. Roze (Fort Collins, CO)
Assignee: Avago Technologies General IP (Singapore) Pte. Ltd. (Singapore, SG)
Filed: May 30, 2013

Abstract— A programmable feedforward equalizer (FFE) includes a plurality of unit cells, each unit cell comprising a capacitive element coupled to an input connection by a first switch and coupled to an output connection by a second switch. The FFE also comprises clock logic configured to control the first switch and the second switch, so that a selected voltage signal is applied to the capacitive element at a selected time, such that the selected voltage signal defines a capacitance of the capacitive element, the clock logic causing the second switch to couple the capacitive element to the output connection so as to apply the selected voltage signal as a filter coefficient to a summing element.

Digital Object Identifier 10.1109/JSSC.2017.2648618

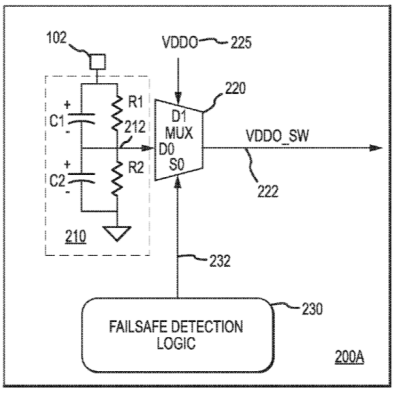


9,391,618 July 12, 2016

High Voltage Fail-Safe IO Design Using Thin Oxide Devices

Inventors: Darrin Robert Benzer (Chandler, AZ)
Assignee: Broadcom Corporation (Irvine, CA)
Filed: August 28, 2014

Abstract— A high-voltage fail-safe input/output (I/O) interface circuit includes a voltage-divider circuit coupled to an I/O pad of the I/O interface circuit, and a selector circuit configured to couple to a power supply line of the I/O interface circuit one of an output of the voltage-divider circuit or and I/O supply voltage. The voltage-divider circuit and the selector circuit are implemented on the same chip with the I/O interface circuit.

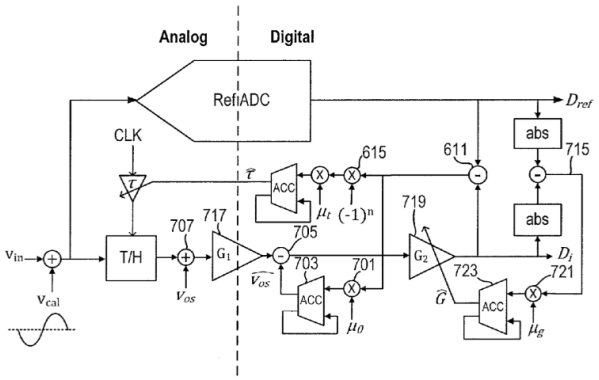


9,401,726 July 26, 2016

Background Calibration of Time-Interleaved Analog-to-Digital Converters

Inventors: Kareem A. Ragab (Austin, TX), John Khoury (Austin, TX)
Assignee: Silicon Laboratories Inc. (Austin, TX)
Filed: November 26, 2014

Abstract— A robust and fast background calibration technique for correction of time-interleaved ADC offset, gain, bandwidth, and timing mismatches is proposed. The technique combines the use of a calibration signal and a reference ADC. The calibration signal enhances robustness and makes the technique independent of the input signal's statistics. The reference ADC speeds up convergence and enables the use of a small amplitude calibration signal that does not significantly reduce the input signal dynamic range. The calibration signal can be subtracted or filtered from the ADC output and is, therefore, invisible to the ADC user.

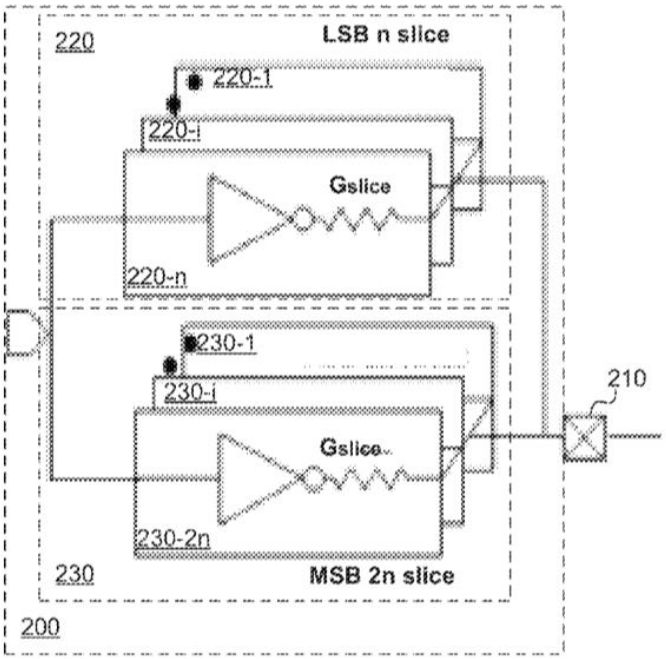


9,413,381 August 9, 2016

High-Speed, Low-Power Reconfigurable Voltage-Mode DAC-Driver

Inventors: Anand Jitendra Vasani (Irvine, CA), Ali Nazemi (Aliso Viejo, CA), Jun Cao (Irvine, CA), Afshin Momtaz (Laguna Hills, CA)
Assignee: Broadcom Corporation (Irvine, CA)
Filed: February 6, 2015

Abstract— A low-power reconfigurable voltage-mode digital-to-analog converter (DAC) driver circuit includes a first and a second supply voltage and a number of DAC units. Each DAC unit is coupled to a respective bit of a digital input. The DAC units are configured to maintain a constant output impedance. Each DAC unit includes one or more complementary switch pairs that couple first nodes of one or more respective impedances to one of the first or the second supply voltage, based on the respective bit of the digital input. Second nodes of the one or more respective impedances are coupled to an output node.

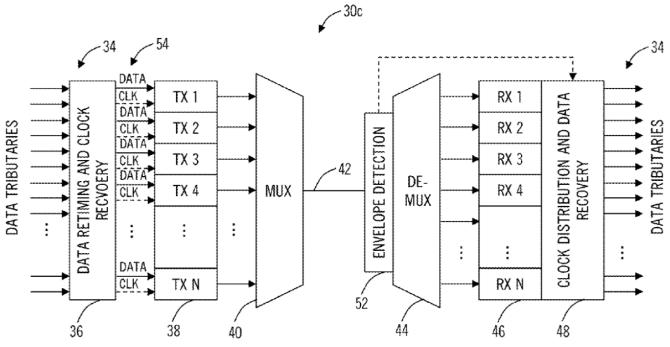


9,413,520 August 9, 2016

Optical Transceiver and Method With Channel Binding, Clock Forwarding, and Integrate-and-Dump Receivers

Inventors: Vladimir Pelekhaty (Baltimore, MD), Michael Y. Frankel (Baltimore, MD)
Assignee: Ciena Corporation (Hanover, MD)
Filed: December 12, 2013

Abstract— An optical transceiver includes *N* transmitters each transmitting one of *N* transmitted optically bound channels; a clock forwarding mechanism to transmit a transmitted optical clock signal to an opposing optical receiver; *N* receivers each receiving one of *N* received optically bound channels; and a clock recovery mechanism to receive a received optical clock signal from the opposing optical transmitter. A method and a photonically integrated system are also disclosed. The optical transceiver, method, and system optimize system design of WDM highly parallelized transceivers with optical bound channels, a simplified clocking architecture, and boosted receiver sensitivity. The optical transceiver, method, and system include clock recovery followed by data recovery and can utilize integrate-and-dump optical receivers with a recovered clock.

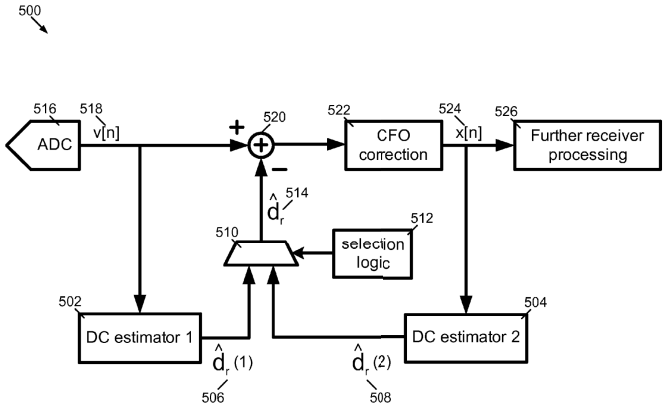


9,413,574 August 9, 2016

Systems and Methods for DC Offset Correction

Inventors: Sergey Timofeev (Santa Clara, CA), Swaroop Venkatesh (Dublin, CA), Atul Salhotra (Santa Clara, CA), Rohit U. Nabar (Sunnyvale, CA)
Assignee: Marvell International Ltd. (Hamilton, BM)
Filed: July 31, 2013

Abstract— Systems and methods for removing dc offset from a signal are provided. A radio frequency signal is received at a receiver. The radio frequency signal is converted into a digital signal including a periodic component with a period. A carrier frequency offset is removed from the digital signal to generate a frequency-shifted digital signal. The frequency-shifted digital signal is filtered to remove a dc offset in the digital signal. The filtering includes applying a moving average filter matched to the period to remove the periodic component from the frequency-shifted digital signal. The moving average filter generates a set of average values based on the frequency-shifted digital signal. The filtering also includes taking a difference between consecutive values of the set of average values to determine the dc offset, where the dc offset is introduced at the receiver.

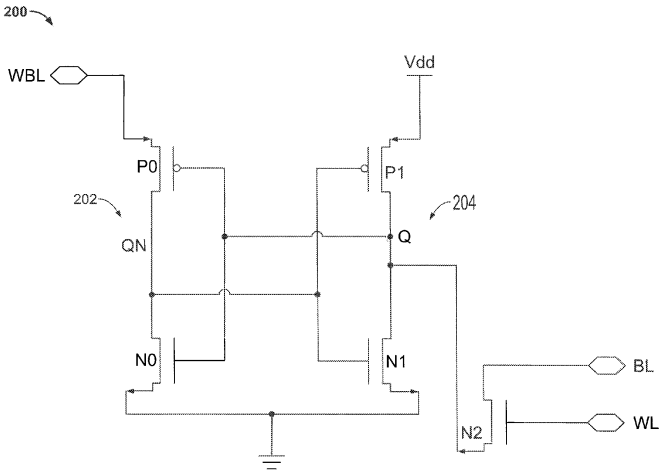


9,418,727 August 16, 2016

Five-Transistor SRAM Cell

Inventors: Sushil Sudam Sakhare (Mumbai, IN)
Assignee: Broadcom Corporation (Irvine, CA)
Filed: July 30, 2012

Abstract— A five-transistor static random-access-memory (SRAM) cell is disclosed, which can be made part of an SRAM array to provide an improved reduction in size. The cell includes two cross-coupled inverters, each having two complementary transistors, and an n-channel transistor switch connected to a bit line (BL) and a word line. The p-channel element of one of the inverters is connected to a power supply, and the p-channel transistor of the other inverter is coupled to a write BL (WBL). By varying the voltage levels on the BL and WBL lines, the biasing of the individual n-channel transistors of each of the inverters can be changed based on the data to be written to the cell. Various biasing systems are presented, such that the SRAM cell memory state can be changed without requiring larger transistor elements to overpower the cell state.

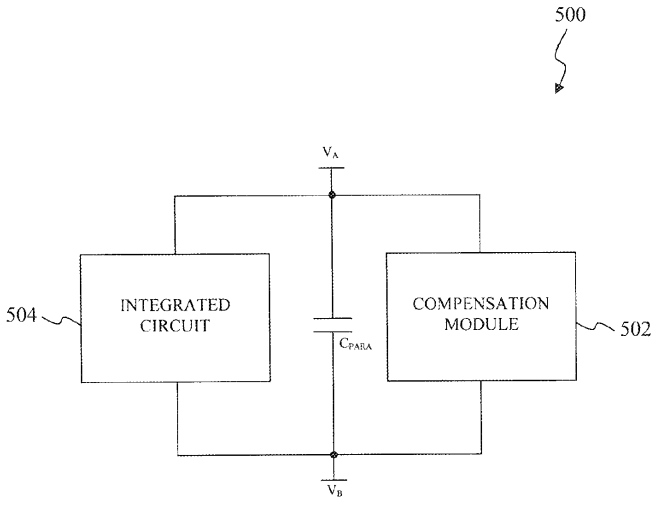


9,432,038 August 30, 2016

Digital-to-Analog Converter Using Nonlinear Capacitance Compensation

Inventors: Christopher Ward (The Netherlands, NL), Klaas Bult (Bosch en Duin, NL), Iniyavan Elumalai (Utrecht, NL)
Assignee: Broadcom Corporation (Irvine, CA)
Filed: May 7, 2015

Abstract— A semiconductor device fabrication operation is commonly used to manufacture one or more integrated circuits onto a semiconductor substrate. The semiconductor device fabrication operation forms one or more transistors onto an arrangement of fabrication layers to form the one or more integrated circuits, which introduces unwanted capacitances, often referred to as parasitic capacitances, into the one or more transistors. The one or more integrated circuits include one or more compensation modules that, when combined with the parasitic capacitances of the one or more transistors, ideally linearizes the nonlinearity caused by the parasitic capacitances of the one or more transistors. For example, the one or more compensation modules incorporate a nonlinear or a piecewise linear transfer function that is inversely related to the parasitic capacitances of the one or more transistors.

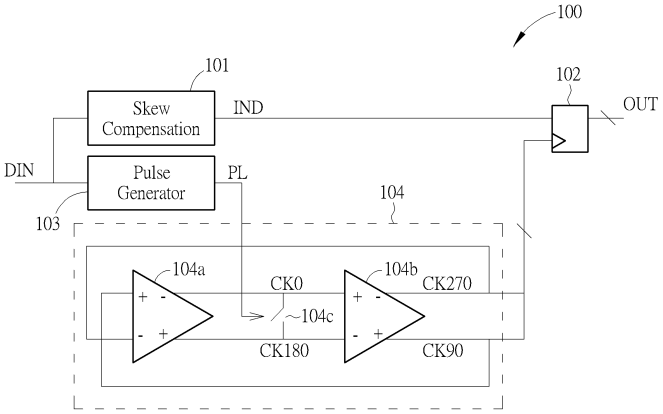


9,432,178 August 30, 2016

Clock and Data Recovery Circuit Using an Injection Locked Oscillator

Inventors: Shiue-Shin Liu (HsinChu, TW), Chih-Chien Hung (Hualien County, TW), Shao-Hung Lin (Kaohsiung, TW)
Assignee: Mediatek Inc. (Hsin-Chu, TW)
Filed: March 16, 2015

Abstract— A clock and data recovery circuit includes a sampler, a skew compensation block, a pulse generator, and an injection locked oscillator. The injection locked oscillator generates a recovered clock signal, the pulse generator generates a pulse signal according to input data for controlling the injection locked oscillator, the skew compensation block compensates the input data and generate compensated data, and the sampler samples the compensated data according to the recovered clock signal.

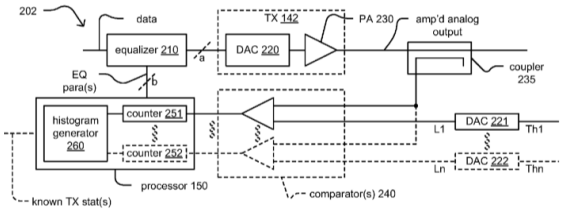


9,432,222 August 30, 2016

Broadband Amplifier Linearization Using Captured Histogram Data

Inventors: Ramon Alejandro Gomez (San Juan Capistrano, CA), Bruce Joseph Currivan (Los Altos, CA), Lin He (Irvine, CA), Thomas Joseph Kolze (Phoenix, AZ), Franciscus Maria Leonardus van der Goes (The Hague, NL), Jun Wang (Los Angeles, CA)
Assignee: Broadcom Corporation (Irvine, CA)
Filed: December 26, 2013

Abstract— A transmitter's operation is characterized using components having relatively low cost and low complexity. A device includes comparator(s) that compare a transmitter's analog output to predetermined level(s) to generate count(s) associated with analog output range bin(s). Each of the predetermined levels is associated with a corresponding one of the analog output range bins. A transfer function of the transmitter is generated using the comparison count values associated with the analog output range bin(s). A histogram may be generated from the comparison count values associated with the various analog output range bins. An equalizer is implemented to process data that will be transmitted by the transmitter. The equalizer uses equalizer parameter(s) that are selected based on the characterization of the transmitter (e.g., its transfer function, its histogram, and so on). The equalizer may use default or start-up parameters until the transmitter's operation is characterized.

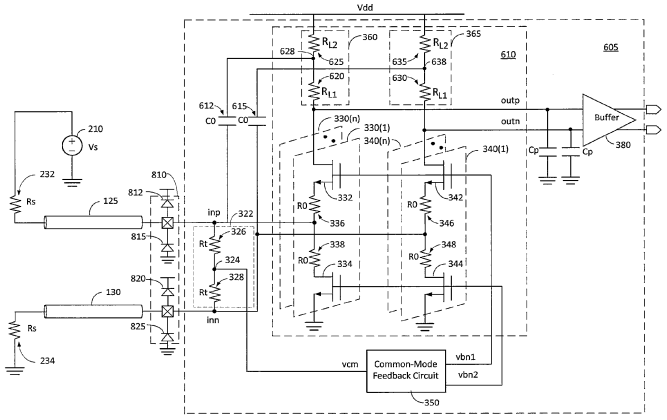


9,438,188 September 6, 2016

Common-Gate Amplifier for High-Speed DC-Coupling Communications

Inventors: Miao Li (San Diego, CA), Li Sun (San Diego, CA), Zhi Zhu (San Diego, CA)
Assignee: Qualcomm Incorporated (San Diego, CA)
Filed: September 15, 2014

Abstract— In one embodiment, a receiver comprises a differential common-gate amplifier having a differential input and a differential output, wherein the differential input comprises a first input and a second input, and the differential common-gate amplifier is configured to amplify an input differential signal at the differential input into an amplified differential signal at the differential output. The receiver also comprises a common-mode voltage sensor configured to sense a common-mode voltage of the input differential signal, a replica circuit configured to generate a replica voltage that tracks a direct current (dc) voltage at least one of the first and second inputs, and a comparator configured to compare the sensed common-mode voltage with the replica voltage, and to adjust a first bias voltage input to the differential common-gate amplifier based on the comparison, wherein the dc voltage depends on the first bias voltage.

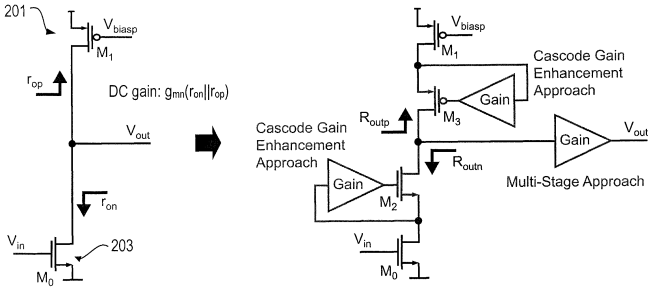


9,444,406 September 13, 2016

Amplifier Topology Achieving High DC Gain and Wide Output Voltage Range

Inventors: Michael H. Perrott (Nashua, NH), Srisai R. Seethamraju (Nashua, NH), Timothy A. Monk (Hudson, NH)
Assignee: Silicon Laboratories Inc. (Austin, TX)
Filed: December 31, 2015

Abstract— An amplifier topology achieves and enhances dc gain to improve linearity while maintaining a good signal-to-noise ratio. The amplifier includes an amplifier output stage that supplies an amplifier output signal. The amplifier also includes a sense amplifier that augments the output stage. The sense amplifier is coupled to the amplifier input to control current through the output stage in order to achieve reduced voltage variation at the amplifier input as a function of the amplifier output signal voltage as compared with a basic common source amplifier, and thereby enhances dc gain of the amplifier.

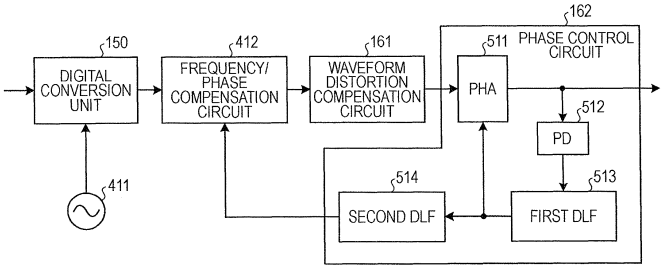


9,444,554 September 13, 2016

Digital Coherent Receiving Apparatus

Inventors: Nobukazu Koizumi (Kawasaki, JP), Takeshi Hoshida (Kawasaki, JP), Takahito Tanimura (Kawasaki, JP), Hisao Nakashima (Kawasaki, JP), Koji Nakamuta (Kawasaki, JP), Noriyasu Nakayama (Kawasaki, JP)
Assignee: Fujitsu Limited (Kawasaki, JP)
Filed: September 27, 2013

Abstract— A digital coherent receiving apparatus includes a first oscillator for outputting a local light signal of a fixed frequency, a hybrid unit mixing the local light signal with a light signal received by a receiver, a second oscillator for outputting a sampling signal of a sampling frequency, a converter for converting the mixed light signal into digital signal synchronizing with the sampling signal, a waveform adjuster for adjusting a waveform distortion of the converted digital signal, a phase adjustor for adjusting a phase of the digital signal adjusted by the waveform adjustor, a demodulator for demodulating the digital signal adjusted by the phase adjuster, a phase detector for detecting a phase of the digital signal adjusted by the phase adjuster, and a control signal output unit for outputting a frequency control signal on the basis of the detected phase signal to the second oscillator.



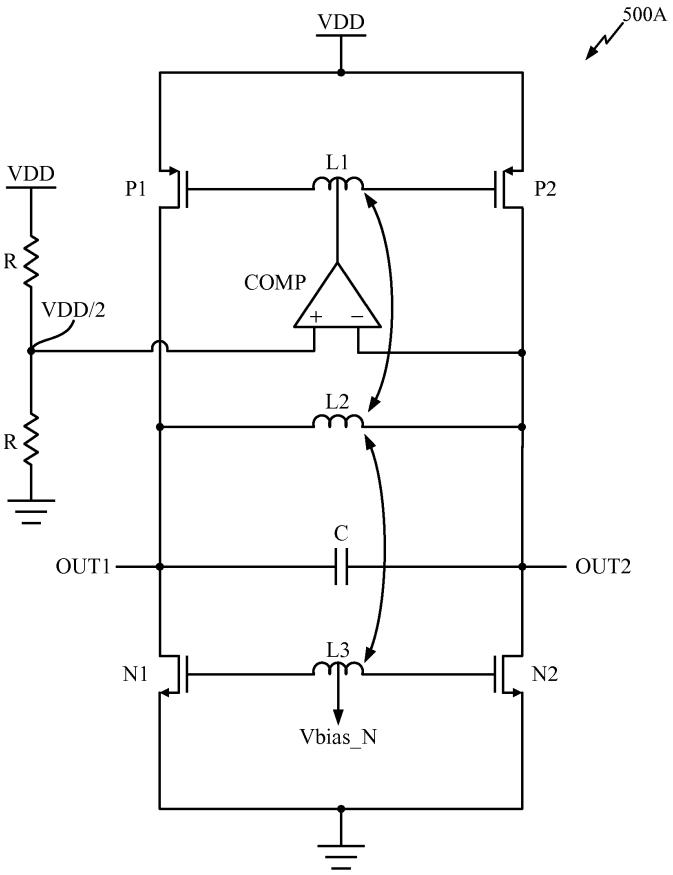
9,461,652 October 4, 2016

Transformer-Based CMOS Oscillators

Inventors: Mazhareddin Taghivand (San Diego, CA)
Assignee: Qualcomm Incorporated (San Diego, CA)
Filed: April 11, 2014

Abstract— Techniques for providing transformer-based CMOS oscillators are capable of operation with low voltage power supplies. In an exemplary embodiment, an *LC* tank is provided at the drains of a transistor pair, and the

inductance of the *LC* tank is mutually magnetically coupled to an inductance between the gates of the transistor pair. A separate complementary transistor pair is also coupled to the *LC* tank. A further exemplary embodiment provides an *LC* tank at the gates of a transistor pair, as well as for three-way coupling among a tank inductance, an inductance between the gates of the transistor pair, and an inductance between the gates of a complementary transistor pair.

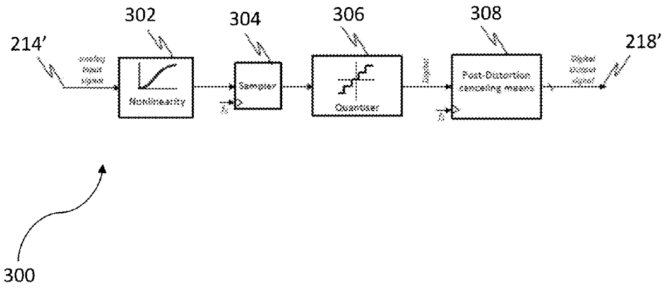


9,461,660 October 4, 2016

Digitally Corrected Analog-to-Digital Converters

Inventors: Khurram Muhammad (Winston-Salem, NC), Chi-Lun Lo (Yangmei, TW), Frank Op 't Eynde (Wilsele, BE), Michael A. Ashburn, Jr. (Groton, MA), Tien-Yu Lo (Hsinchu, TW)
Assignee: Mediatek Inc. (Hsin-Chu, TW)
Filed: November 11, 2015

Abstract— A method and an apparatus for a digitally corrected analog-to-digital converter are disclosed. The apparatus comprises a nonlinearity generator that generates one or more nonlinear characteristics of a time-varying input signal and that causes unwanted signal components at frequencies other than a frequency of the time-varying input signal, a frequency response modifier coupled to the nonlinearity generator that modifies the unwanted signal components by altering an amplitude of the unwanted signal components, a frequency response compensator coupled to the frequency response modifier, wherein the frequency response compensator compensates for the modification introduced by the frequency response modifier to provide a filtered digital signal, and an inverse nonlinearity generator coupled to the frequency response compensator for receiving the filtered digital signal, wherein the inverse nonlinearity generator compensates for the one or more nonlinear characteristics.

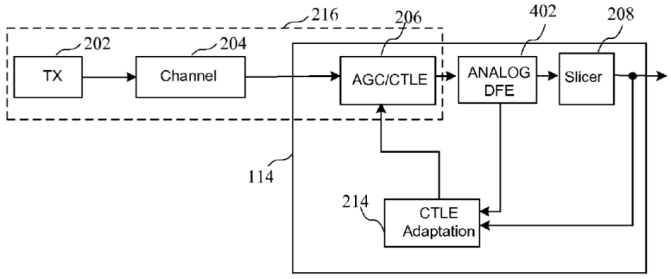


9,461,851 October 4, 2016

Circuits for and Methods of Robust Adaptation of a Continuous Time Linear Equalizer Circuit

Inventors: Yu Liao (Longmont, CO), Geoffrey Zhang (San Jose, CA)
Assignee: Xilinx, Inc. (San Jose, CA)
Filed: October 16, 2015

Abstract— A circuit for enabling an adaptation of an equalization circuit is described. The circuit comprises a continuous time linear equalizer configured to receive an input data signal and generate an equalized input data signal; a decision circuit configured to receive the equalized input data signal, wherein the decision circuit generates an estimate of the input data signal; channel estimation circuit configured to receive the estimate of the input data signal and an error signal to generate an impulse response estimate of an equivalent channel; a frequency response computation circuit configured to receive the impulse response estimate of the equivalent channel and generate a channel frequency response; and a continuous time linear equalizer control circuit configured to receive the channel frequency response and to generate a CTLE adaptation signal for controlling the continuous time linear equalizer.

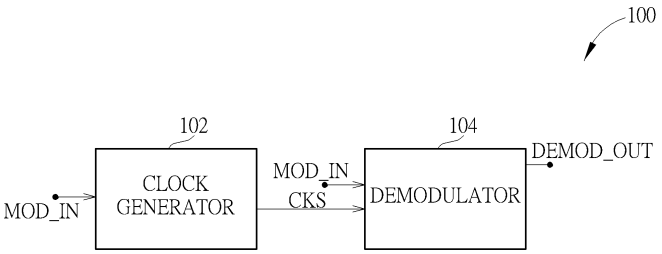


9,461,852 October 4, 2016

Signal Demodulation Apparatus and Signal Demodulation Method

Inventors: Uday Dasgupta (Singapore, SG)
Assignee: MediaTek Singapore Pte. Ltd. (Singapore, SG)
Filed: July 20, 2015

Abstract— A signal demodulation apparatus includes a clock generation device arranged to generate a clock signal according to an inputting modulation signal and a demodulation device arranged to demodulate the inputting modulation signal to generate a demodulation signal according to the clock signal, wherein a signal edge of the clock signal substantially aligns to a turning point of the inputting modulation signal.

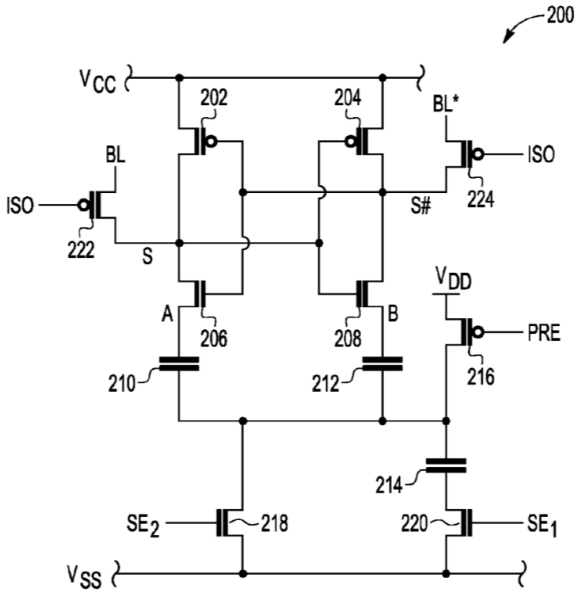


9,466,394 October 11, 2016

Mismatch-Compensated Sense Amplifier for Highly Scaled Technology

Inventors: Perry H. Pelley (Austin, TX), Ravindraraj Ramaraju (Round Rock, TX)
Assignee: Freescale Semiconductor, Inc. (Austin, TX)
Filed: April 9, 2015

Abstract—Circuits and methods are provided for compensating an offset voltage measured between a first transistor and a second transistor of a sense amplifier circuit that is configured to sense a bit line signal during a sensing phase. The first transistor and the second transistor are cross coupled. The first transistor is coupled to a first capacitor and the second transistor is coupled to a second capacitor. The first capacitor is further coupled to the second capacitor, and the first and second capacitors are coupled to a third transistor. The first capacitor applies a first bias voltage to the first transistor during a presensing phase prior to the sensing phase, and the second capacitor applies a second bias voltage to the second transistor during the presensing phase.

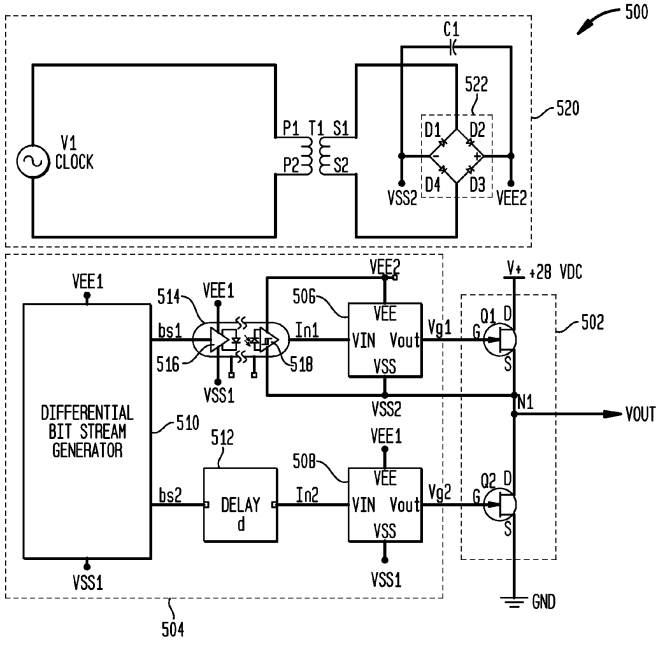


9,473,086 October 18. 2016

High-Voltage Voltage-Switched Class-S Amplifier

Inventors: Donald R. Laturell (Oak Hill, FL), Said E. Abdelli (Minneapolis, MN), Peter Kiss (Basking Ridge, NJ), James F. MacDonald (Mendota Heights, MN), Ross S. Wilson (Menlo Park, CA)
Assignee: 14/380 823
Filed: January 18, 2013

Abstract—A voltage-switched class-S amplifier circuit includes an output stage configured to receive at least one control signal and operative to generate an output signal as a function of the at least one control signal. The amplifier circuit further includes a driver circuit coupled with the output stage. The driver circuit is configured to receive an input bitstream signal and is operative to generate the control signal as a function of the input bitstream signal in such a manner that a common mode component is eliminated from the control signal.



9,479,202 October 25, 2016

System and Method for Burst Mode Amplifier

Inventors: Inventors: Koen Mertens (Villach, AT), Thomas Poetscher (Villach, AT)
Assignee: Assignee: Infineon Technologies AG (Neubiberg, DE)
Filed: Filed: February 19, 2008

Abstract—Embodiments related to burst mode amplifying are described and depicted.