

A Wide Linear Dynamic Range Image Sensor Based on Asynchronous Self-Reset and Tagging of Saturation Events

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Abstract—We report a high dynamic range (HDR) image sensor with a linear response that overcomes some of the limitations of sensors with pixels with self-reset operation. It operates similar to an active pixel sensor, but its pixels have a novel asynchronous event-based overflow detection mechanism. Whenever the pixel voltages at the integration capacitance reach a programmable threshold, the pixels self-reset and send out asynchronously an event indicating this. At the end of the integration period, the voltage at the integration capacitance is digitized and readout. Combining this information with the number of events fired by each pixel, it is possible to render linear HDR images. Event operation is transparent to the final user. There is no limitation for the number of self-resets of each pixel. The output data format is compatible with frame-based devices. The sensor was fabricated in the AMS 0.18- μm HV technology. A detailed system description and experimental results are provided in this paper. The sensor can render images with an intra-scene dynamic range of up to 130 dB with linear outputs. The pixels' pitch is 25 μm and the sensor power consumption is 58.6 mW.

Index Terms—Address event representation (AER), event, high dynamic range (HDR), image sensor, linear response, octopus retina.

I. INTRODUCTION

HIGH dynamic range (HDR) operation is desired for many applications with image sensors: surveillance, quality imaging, and drone vision. In general, it is always mandatory in scenarios without controlled illumination conditions. In this sense, designers try to maximize the dynamic range when designing image sensors, to amplify its range of applicability.

The classic active pixel sensor (APS) has a limited dynamic range. For a fixed integration time, the lowest lower photocurrent value that can be sensed is limited by the quantization

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noise or the read noise of the analog-to-digital-converter. The largest photocurrent value is usually limited by the full well capacity. By increasing the integration time, it is possible to sense lower photocurrent values, but the highest photocurrent that can be gauged will be lower. If the integration time is decreased, it will be possible to operate with higher illumination, but precision within lower illuminated areas will be lost. Therefore, the dynamic range is inherently limited by the sensor and cannot be extended by globally adjusting the integration time. Typically, APS sensors DR is limited to values below 70 dB [1]. If we compare this feature with the performance of the human eye, it is sensibly worse. Our eyes can sense images with an intra-scene dynamic range of over six decades [2]. Typical natural scenes can reach a DR of 120 dB [1]. Therefore, there is a need for HDR operation to render images with a precision close to our human perception.

There are several techniques to extend the dynamic range [1], [3], [4]. Maybe the most popular is to capture images with multiple integration times and then combine them [5]–[9]. This approach has expensive requirements regarding computational load, hardware, and power consumption. First, dedicated algorithms have to be programmed to combine the different images (irradiance maps) and render the final HDR photo [10]. Before combining the different frames, they have to be captured as individual images and stored in the memory. Thus, the frame rate (FR) will be lowered, and the power consumption increased. Furthermore, multiple captures with misaligned integration times can generate nonexistent edges and distort the interpretation of the scene [11].

Another option to extend the dynamic range is to use tone mapping (TM) algorithms [4], [12], [13]. Based on image histograms, gray levels are assigned with more precision to the values that are more frequent in the visual scene. Thus, there is a non-linear relation between the pixel photocurrents and the gray levels assigned to each pixel. The resulting HDR images have a low number of bits to encode illumination. There are sensors that implement TM algorithms on chip [13]. The approach produces quality HDR images. Unfortunately, all illumination levels are not encoded with the same accuracy and there is a loss of information. The choice of the TM curves is not trivial, and conditions the quality of the final image. Hence, the process of TM is not reversible once a frame has been rendered, implementing this technique on chip. Moreover, in machine vision applications where precise contrast

information or high speed is required, these calculation-based methods can be inadequate [1].

More recently, several event-based image sensors with inherent HDR operation have been reported [14]–[19]. They try to mimic biological systems. They usually employ a logarithmic compression of the illumination values to extend the dynamic range. They also try to perform the same kind of in-pixel processing, typically spatio-temporal contrast detection. Their approach is effective, but their event-based description of the scene is not easily compatible with the most widely employed frame-based displays and conventional frame-based image processing algorithms as in [20]. Many applications just require to encode intensity levels of the visual scene.

In this paper, we describe in detail a novel concept of an image sensor with an HDR linear output. A preliminary theoretical circuit analysis was already advanced [21]. The sensor combines classic APS pixel operation with event-based overflow detection. Its pixels never overflow during the integration time. Every time the voltage at the integration capacitance reaches a limit, the pixel resets itself and continues integrating charge again. Events are sent out to indicate how many times a pixel has overflowed. Ideally, high illuminated pixels will never be overexposed. The selection of the integration time determines the minimum illumination values that can be sensed. Knowing the number of events (if any), associated with each pixel and the digitized voltage at the end of the integration period, it is possible to obtain digital words whose value is proportional to illumination. Sensor outputs are compatible with frame-based displays and processing algorithms. Event operation is totally transparent. All the illumination values are encoded with the same precision. The user can trade between FR, the amount of memory dedicated to store the event information, and the maximum intra-scene dynamic range that can be sensed.

The pixel self-resetting mechanism is not new and has already been proposed in [22]–[25], to mention but a few. It leads to pixels with linear output, high SNR, and HDR. However, the reported pixels require in-pixel counters to store the number of pulses. This limits the number of pixel resets that can be sensed. Extra time is required to readout the in-pixel memories after the integration time, lowering the FR. To the best of our knowledge, image sensors that combine APS readout with a self-resetting mechanism, based on an address event representation (AER) [26], [27], high speed asynchronous arbitration scheme have not been reported yet. With this new approach the number of times that a pixel can overflow is not limited by a pixel memory. Low illumination values can be sensed with the APS readout. Large illumination values are sensed activating an independent event-based data flow.

II. PIXEL OPERATION

A. Operation Principle

Fig. 1 shows the new pixel operation concept to extend the dynamic range. Pixel voltage at the integration capacitance never overflows. If it reaches a voltage threshold, V_{bot} , the pixel will reset itself and continue integrating charge again

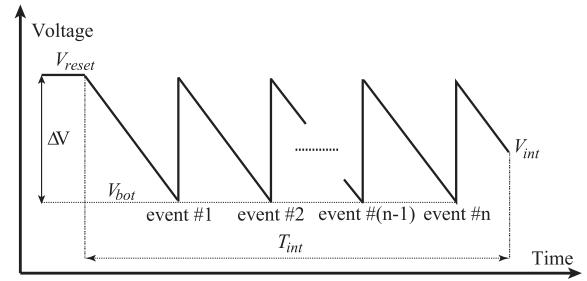


Fig. 1. High dynamic range extension approach. The transient voltage at the integration capacitance of one pixel is shown. After the initial reset, the voltage drops with a slope proportional to illumination. If the voltage reaches the value V_{bot} , the pixel self-resets, sends an event, and continues integrating charge immediately after. At the end of the integration period T_{int} , the final voltage V_{int} is readout.

immediately after. Every time (if any) the integration voltage reaches the value V_{bot} , an event will be sent out of the chip. We will refer in this paper to the event data flow as the “event readout.” At the end of the integration period T_{int} , the voltage at the integration capacitance, V_{int} will be digitized, stored in a memory, and will send out the chip. We will denote this output data flow as the “APS readout.” Both data flows are independent and can be merged to render HDR images. The sensor pixel output values will be proportional to their local illumination

$$I_{ph} \propto (V_{reset} - V_{int}) + (V_{reset} - V_{bot}) \cdot (\#events). \quad (1)$$

The intra-scene dynamic range of a visual scene can be defined as the ratio between the highest and the lowest illumination values that can be sensed within the visual scene. It is usually expressed in decibels as

$$DR = 20 \cdot \log_{10} \left(\frac{I_{ph_{max}}}{I_{ph_{min}}} \right). \quad (2)$$

If we represent the photocurrent values with binary words of N_{bits} , the dynamic range of the sensor is given by

$$DR = 20 \cdot \log_{10}(2^{N_{bits}}) = 20 \cdot \log_{10}(2^{(N_b+N_s)}) \quad (3)$$

where N_b is the resolution of the analog-to-digital-converter, and N_s is the number of bits dedicated to store the number of times that a pixel has spiked.

The novelty of this image sensor over previous ones based on self-reset operation [22], [24], [25] is that the pixel overflow events are not stored in in-pixel memories. We use AER communication to transmit asynchronously the address of the pixels that overflow every time this event occurs. The AER point-to-point communication scheme is depicted in Fig. 2. When the sender is ready to send information and has granted access to the AER bus, a *Request* signal is sent to the receiver. In our case, the senders will be the different pixels sharing the AER bus. The receiver is a digital FSM that stores pixel addresses in a memory. Then, the pixel address is placed on the shared AER bus. When the receiver has received the information, it sends back an *Acknowledge* signal. For a detailed explanation of modern AER communication schemes and their performance, we refer the reader to [26] and [28]. Specific details about the AER circuitry described in this paper can be found in [27].

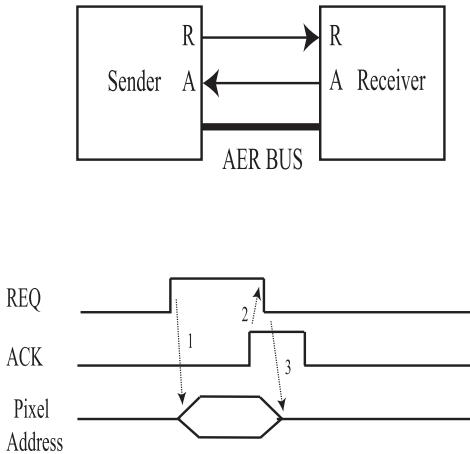


Fig. 2. AER point-to-point communication scheme between a sender and a receiver.

B. New Pixel's Concept

Fig. 3 displays the pixels schematics. On the left, there is circuitry to implement the classic APS operation and readout. In the middle, there is an astable oscillator. It pulses with a frequency that is proportional to the input photocurrent, performing a light to frequency conversion. On the right, there is specific asynchronous circuitry that handles the event communication and has been reported elsewhere [27]. We will refer to it in this paper as the AER logic. Whenever the voltage at the integration capacitance reaches the value V_{bot} , the voltage V_{ph} should be reset as fast as possible to minimize the error introduced by the reset operation. To avoid waiting for the acknowledgment signals to reset the integration capacitance, event requests are stored on the capacitor C_1 until they can be acknowledged. The event handshaking cycle under normal circumstances is much faster (nanoseconds scale) than the event output frequency (milliseconds scale), even under high illumination. Therefore, the probability of spiking before a previous event request has not been attended is very low and, for a preliminary circuit analysis, we will consider that the AER logic does not introduce any error in the light sensing.

Fig. 4(a) shows a timing chart with the pixel control signals. Initially, all the pixels are reset simultaneously. Then, they integrate charge during T_{int} . During the integration period, pixels that over-flow send events through the shared AER bus. At the end of the integration period, the voltage V_{int} is stored. Then, different pixel rows (96 in this implementation) are readout sequentially and the different V_{int} voltages of each column are digitized and stored in a memory.

In Fig. 4(b) there is a timing chart with the pixel signals involved in the asynchronous event communication during T_{int} . Every time a pixel overflow happens, the signals involved in the AER communication are activated as it is depicted. At the bottom of Fig. 4(b), there are external signals involved in the entire pixel array communication. Since the AER bus is shared by all the pixels, there is arbitration circuitry to assure that only one pixel has access to the bus at some moment (see details in Section III-A). The amount of time required to transmit one event, $T_{\text{handshake}}$, depends on the bus congestion. Typical values are $T_{\text{handshake}} = 100\text{--}200$ ns. If the sensor is

not exposed to intense light, the handshaking cycle is much lower than the pixels oscillation period.

Let us analyze the astable oscillator. It generates pulses with a period that is approximately

$$T = \frac{C \cdot (V_{\text{reset}} - V_{\text{bot}})}{I_{\text{ph}}} + T_d + T_{\text{reset}} \approx \frac{C \cdot \Delta V}{I_{\text{ph}}} \quad (4)$$

where $T_d \approx 25$ ns is the controlled delay introduced to make the oscillator stable. $T_{\text{reset}} \approx 400$ ns is the amount of time required by the transistor M_{p3} in Fig. 3 to reset the integration capacitance with $\Delta V = 4$ V. For simplicity, for a preliminary circuit analysis, its value can be neglected because it is much lower than the oscillation period. Under high illumination, pixel spiking frequencies are in milliseconds scale. For a given value of the integration period depicted in Fig. 1 ($T_{\text{int}} = 1/\text{FR}$), the minimum detectable photocurrent provokes a voltage decrement of 1 LSB of the analog-to-digital-converter, that is

$$I_{\text{ph}_{\min}} = \frac{C \cdot \Delta V \cdot \text{FR}}{2^{N_b}}. \quad (5)$$

Therefore, combining (2) and (5), the dynamic range expressed as a function of the maximum photocurrent that can be measured ($I_{\text{ph}_{\max}}$) and the FR is

$$\text{DR} = 20 \cdot \log_{10} \left(\frac{2^{N_b} \cdot I_{\text{ph}_{\max}}}{\text{FR} \cdot C \cdot \Delta V} \right). \quad (6)$$

One practical limitation of our approach is that the arbitration system can handle a maximum output event rate $\text{MAX}_{\text{BR}} = 1/T_{\text{handshaking}}$ that depends on the amount of time required by the arbitration logic to complete the event communication cycle depicted as

$$M \cdot N \cdot f_{\max} < \text{MAX}_{\text{BR}} \quad (7)$$

where f_{\max} is the maximum average spiking frequency when the array is illuminated uniformly. This depends on ΔV . For a given illumination value, we can control the global event rate by adjusting ΔV . We can lower the event rate by increasing $\Delta V = V_{\text{reset}} - V_{\text{bot}} = V_{\text{DD}} - V_{\text{bot}}$. In our particular case, we have implemented a pixel matrix in the AMS 0.18- μm HV standard technology that offers transistors with thicker gate oxide that can reach voltages up to 5 V. Hence, pixels use these transistors to minimize the event rate, maximizing the value of ΔV .

Let us analyze the error introduced by the proposed self-resetting mechanism. The error is mainly due to the amount of time needed to reset the integration capacitance, T_{reset} . The controlled delay at the output of the astable oscillator (T_d) also contributes. Such errors are approximately $T_d \approx 25$ ns and $T_{\text{reset}} \approx 400$ ns (see (4)). In the worst case, during the integration period T_{int} , a pixel can spike a maximum of 2^{N_s} times. Hence, the total accumulated error will be $T_{d_T} = (T_d + T_{\text{reset}}) \cdot 2^{N_s}$. The relative error is $\epsilon = (T_{d_T}/T_{\text{int}}) = (T_d + T_{\text{reset}}) \cdot 2^{N_s} \cdot \text{FR}$. If we assume an FR of $\text{FR} = 25$ frames/s and $N_s = 12$ bits, the maximum possible relative error introduced by the self-reset operation will be $\epsilon = 4.3\%$. In real operation scenarios, all the pixels will not be exposed to the maximum illumination value. Therefore, the expected error will be lower

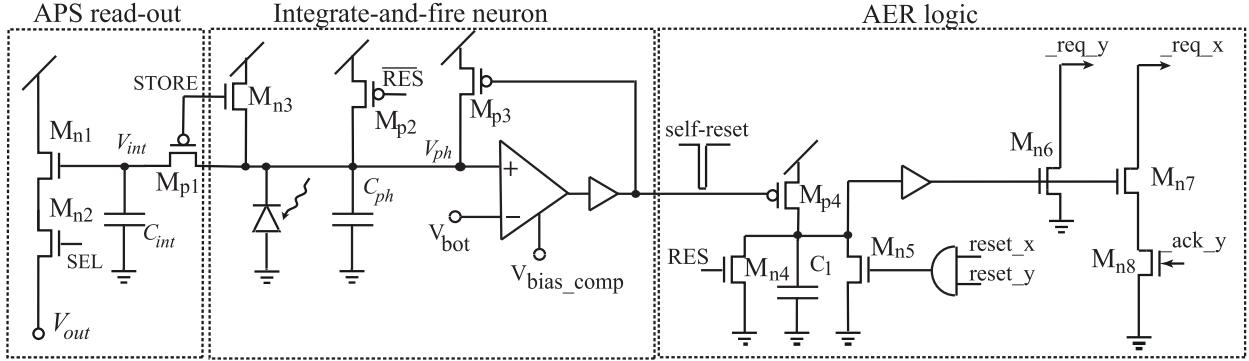


Fig. 3. Pixel's schematics. Left: pixel's analog readout circuitry. Center: astable oscillator that spikes with a frequency proportional to illumination. Right: asynchronous circuitry to handle the event communication. Transistor sizes are (W/L, $\mu\text{m}/\mu\text{m}$): $M_{n1} = 1/3.5$, $M_{n2} = 0.5/0.7$, $M_{p1} = 0.5/0.7$, $M_{n3} = 0.5/0.7$, $M_{p2} = 1/1$, $M_{p3} = 3/1$, $M_{p4} = 0.5/1$, $M_{n4} = 0.5/0.7$, $M_{n5} = 0.7/0.7$, $M_{n6} = 1/0.7$, $M_{n7} = M_{n8} = 0.5/0.7$, and $C_{int} = C_1 = 40 \text{ fF}$, $C_{ph} = 5 \text{ fF}$. Bias voltages: $V_{bot} = 1 \text{ V}$, $V_{bias_comp} = 4.3 \text{ V}$.

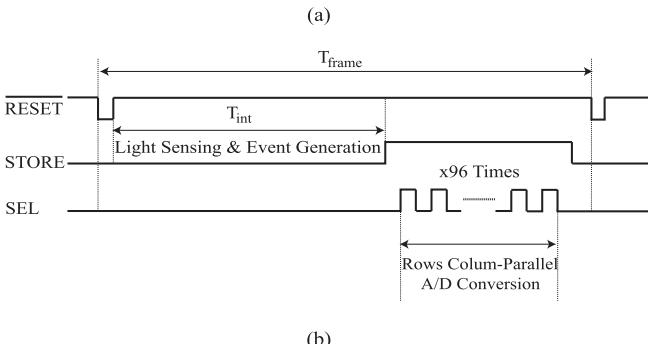


Fig. 4. (a) Timing chart with the pixel control signals. (b) Timing chart with the signals involved in the event communication every time the event is generated during T_{int} .

than ϵ . By lowering the FR, the error will also be lower. By increasing the width of transistor M_{p3} in Fig. 3, T_{reset} will be reduced. The penalties have greater area consumption and higher transistor leakage. This error analysis is valid in all the scenarios where we tested the sensor. In the particular case of heavy AER bus congestion due to high event activity, the arbitration periphery may introduce additional errors due to event loss. This effect will be shown with the experimental data in Section IV-C.

C. Trade-Offs Between Dynamic Range and Frame Rate

The dependence between the FR and the dynamic range is governed by (6). $I_{ph_{max}}$ is the maximum photocurrent that

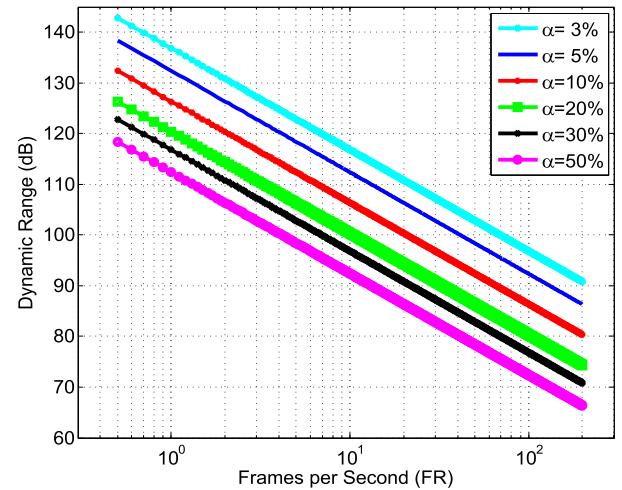


Fig. 5. Dependence between the FR and the maximum intra-scene dynamic range that can be sensed. There is a trade-off between both parameters. The FR can be adjusted depending on the requirements of dynamic range. The parameter α indicates the percentage of pixels firing with the maximum average output frequency (f_{max}) that the peripheral circuitry can cope.

we can measure without saturating the arbitration periphery. Combining (7) and (4), it is possible to express $I_{ph_{max}}$ as a function of the maximum average spiking frequency f_{max} that the sensor can process

$$I_{ph_{max}} = f_{max} \cdot C \cdot \Delta V = \frac{\text{MAX}_{\text{BR}} \cdot C \cdot \Delta V}{M \cdot N \cdot \alpha} \quad (8)$$

where α is a parameter that indicates the percentage of pixels that are exposed to $I_{ph_{max}}$. If $\alpha = 1$, it means that all the pixels are exposed to $I_{ph_{max}}$. This situation is very pessimistic. In real scenes with large intra-dynamic range, α will be lower than one. Combining (6) and (8), it is possible to express the dependence between the FR and the dynamic range

$$\text{DR} = 20 \cdot \log_{10} \left(\frac{2^{N_b} \cdot \text{MAX}_{\text{BR}}}{\text{FR} \cdot M \cdot N \cdot \alpha} \right). \quad (9)$$

As long as the number of bits dedicated in memory ($N_b + N_s$) to store the intensity levels is high enough, the dynamic range only depends on the maximum event rate that the peripheral circuitry can cope, the total number of pixels,

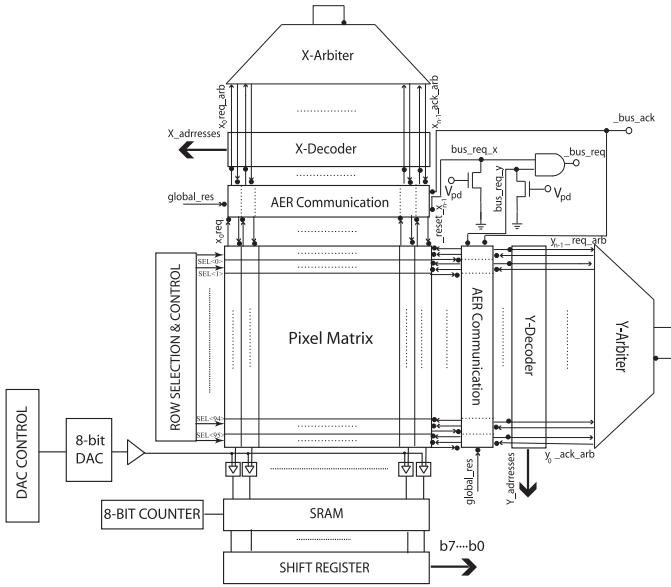


Fig. 6. System block diagram. Center: pixel array. Top-right: event asynchronous readout. Bottom-left: synchronous circuitry for the APS pixel operation and readout.

and the FR. Fig. 17 displays such dependence for different values of α . Thus, there is a trade-off between the maximum event rate that the sensor can handle, the dynamic range, and the FR.

III. SYSTEM LEVEL DESCRIPTION

Fig. 6 displays the complete system block diagram. In the middle, there is the pixel array made up of 96×128 pixels. On the periphery, we have placed the event and APS readouts. Both operate independently to generate two output data flows. The event flow occurs during the integration time as it is depicted in Fig. 1. The APS readout is ready after the end of the integration period.

A. Event Readout Circuitry

The circuitry dedicated to handle the event communication corresponds to the blocks plotted on the top and right sides of Fig. 6. A detailed description of the AER blocks and its interconnectivity was presented in [27]. It has also been reported elsewhere in other sensor implementations [19], [28]. It can handle event rates up to 10 Meps for pixels of different rows, and 2 Meps for pixels of the same row. In the chip implementation, row petitions are arbitrated first, with the peripheral circuitry of the right side. Afterward, columns petitions are arbitrated. Finally, an external _bus_req signal and the address of the pixel that has spiked are sent out of chip, until the _bus_ack signal is received. Thereafter, the next event is attended.

B. APS Readout Circuitry

The circuitry necessary to make the pixel operate as an APS CMOS pixel has been placed at the bottom-left in Fig. 6. The block on the left generates the row selection signals to select the different array rows sequentially for the analog-to-digital conversion. Signals RESET and STORE are activated globally. Hence, there is no rolling shutter implemented. At the bottom,

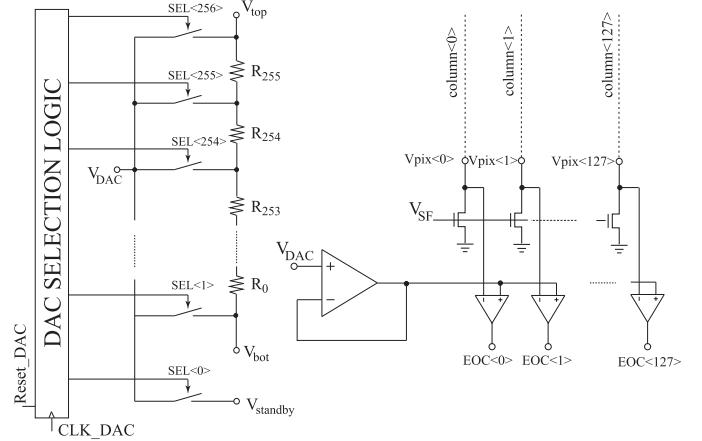


Fig. 7. Block diagram of the column parallel converters. We display the resistive DAC employed to generate the reference voltages, the digital block to control it, the analog buffers that buffer the DAC output voltages, and the column comparators that indicate when the reference voltage (V_{DAC}) reaches the pixel output voltages V_{pix} . $R_i = 107 \Omega$. Bias voltages: $V_{SF} = 700$ mV, $V_{top} = 3.4$ V, and $V_{bot} = 600$ mV.

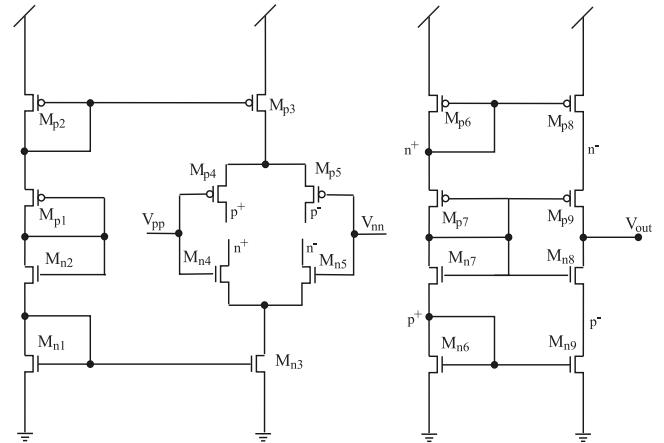


Fig. 8. Schematics of the analog buffer that drives the reference voltages V_{DAC} to the column comparators. Transistor sizes are (W/L, $\mu\text{m}/\mu\text{m}$): $M_{p1} = M_{n2} = 5/1$, $M_{n1} = M_{p2} = 7.5/1$, $M_{n3} = M_{p3} = 5/1$, $M_{n4} = M_{n5} = M_{p4} = M_{p5} = 5/2$, $M_{p6} = M_{p7} = M_{p8} = M_{p9} = 2.5/1$, $M_{n6} = M_{n7} = M_{n8} = M_{n9} = 3/1$. $V_{DD} = 5$ V. Its power consumption is approximately 90 μ A.

there is the circuitry for the column parallel analog-to-digital-conversion. We have implemented 128 column parallel ramp converters (see details in Fig. 7). Fig. 8 displays the circuitry of the analog buffers that drives the DAC output voltages to the ramp converter comparators. It is a simplified version of the wide range operation buffer proposed in [29]. Furthermore, an SRAM memory and shift registers were implemented on chip to save the APS data and serialize it.

C. Off-Chip Data Processing and Storage

The output data flows are stored off-chip. There is an external XC7K160T Opal Kelly board with a Kintex 7 FPGA that merges the event data flow and the digitized values of the readout voltages at the end of the integration period. Fig. 9 shows the communication between the sensor and Opal Kelly board. It has an external DDR3 SDRAM memory to store frames at video rates and higher. The FPGA internal clock is 200 MHz. To process the data flow, two simple FSMs were

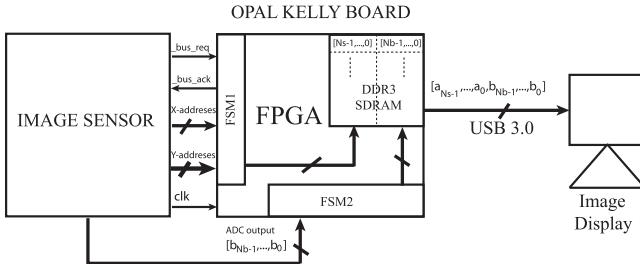


Fig. 9. Diagram of the communication flow between the sensor, an XC7K160T Opal Kelly board, and a PC. The Opal Kelly board merges and stores the event and the ADC outputs associated with each pixel. Its outputs are digital words with $N_s + N_b$ bits that are transmitted to a PC through a high-speed USB 3.0 port.

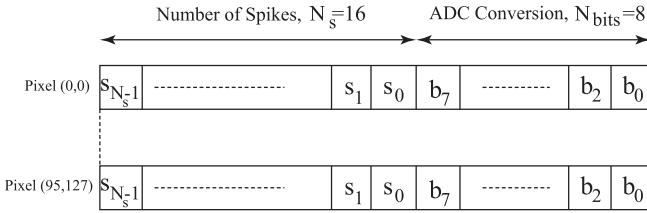


Fig. 10. Detail of how the pixel output data is stored in memory. The most representative $N_s = 16$ bits correspond to the event information. The less significant bits $N_b = 8$ correspond to the A/D conversion of the APS outputs. The event operation is transparent to the final user. Data format is the same as conventional frame-based image sensors.

implemented on the FPGA. The first FSM handles the AER communication. The second reads and stores in memory the digitized pixel outputs (APS readout).

Fig. 10 depicts how pixel output data is stored in memory. The $N_s = 16$ most representative bits correspond to the number of events associated with each pixel. The less significant $N_b = 8$ bits are the results of the A/D conversion of the APS outputs. The external memory has words of 32 bits. The value of N_s can be selected accordingly, taking into account the desired dynamic range. With $N_s + N_b = 16 + 8 = 24$ bits, we set a theoretical maximum value for the intra-scene dynamic range of 145 dB.

IV. EXPERIMENTAL RESULTS

A. Experimental Setup and Interface

Fig. 11(a) and (b) displays the experimental setup. We designed a custom PCB to test the sensor and a lens holder to hold the optics. The PCB is attached to an XEM7350 board. Since the sensor event operation is independent of the frame-based operation, we have added to the sensor's PCB an IDC 40-pin connector compatible with the USBAERmini datalogger that is commonly extended among the AER community [30], [see Fig. 11(b)]. The interface can monitor the event rate between frames, indicating if there is AER bus activity overload.

A custom interface (see Fig. 12) was programmed to test the sensor and display real-time images. It has several operation modes to represent pixel intensities in different ways: color scale, TM, APS, or event flow independently.

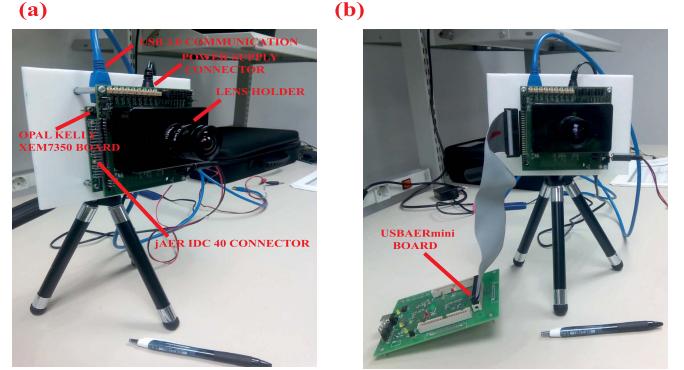


Fig. 11. (a) Experimental setup. A custom PCB and a lens mount were designed to test the system. The PCB is attached to an Opal Kelly XEM7350 board. The sensor PCB also has an optional IDC 40-pin connector compatible with the USBAERmini board [30]. (b) Details of the optional interconnection of our system PCB with the USBAERmini board.

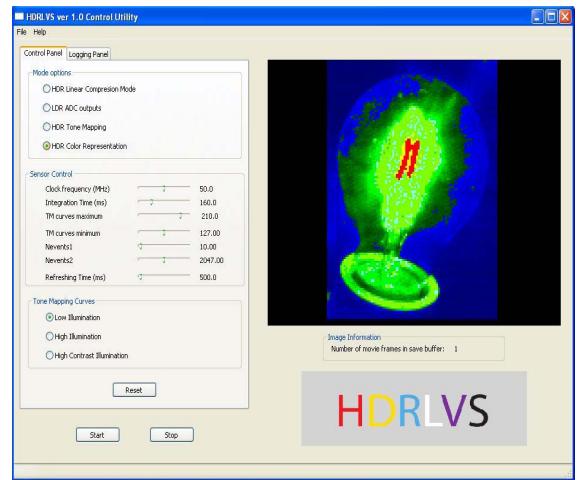


Fig. 12. Custom interface programmed to test the sensor and display real-time images. The interface allows to select different ways of representing the sensor output data. (a) Intensity levels displayed with a color map. A maximum of 24 bits can be used to encode gray levels. (b) TM: the user can define a custom TM curve to map the measured intensity levels to a gray scale with 256 intensity levels. (c) Conventional imager operation. The ADC outputs are represented by a grayscale. Operation is similar to a classic imager. (d) Octopus operation. Gray levels are encoded using the event output with PDM; in the example, a 125-dB-dynamic-range image is shown.

B. Chip Microphotograph and Pixel Layout

The sensor was fabricated in the AMS 0.18- μ m HV technology. The technology has transistors available with thick gate oxide that can operate up to 5 V. Increasing ΔV , the event flow is reduced and the accumulated error due to the self-resetting mechanism when events are sent out too (see quantitative analysis in Section II). To save area and power consumption, the digital circuitry was designed with nominal technology transistors that operate at 1.8 V. Fig. 13(a) and (b) shows a chip microphotograph and the pixel layout.

C. Pixel Response to Illumination

Fig. 14 displays the sensor digital outputs (DN) versus the relative illumination values over five decades. To take the measurements, a region of the sensor was illuminated with a very bright light source. The rest of the pixels were not

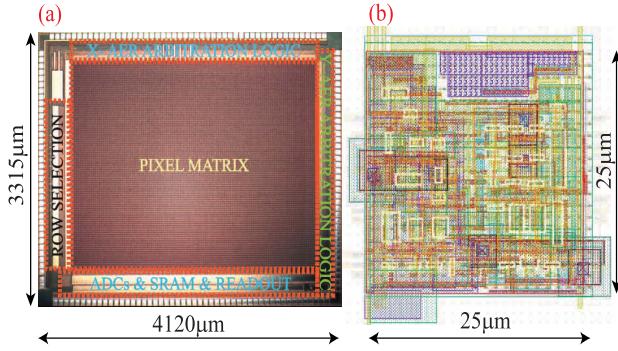
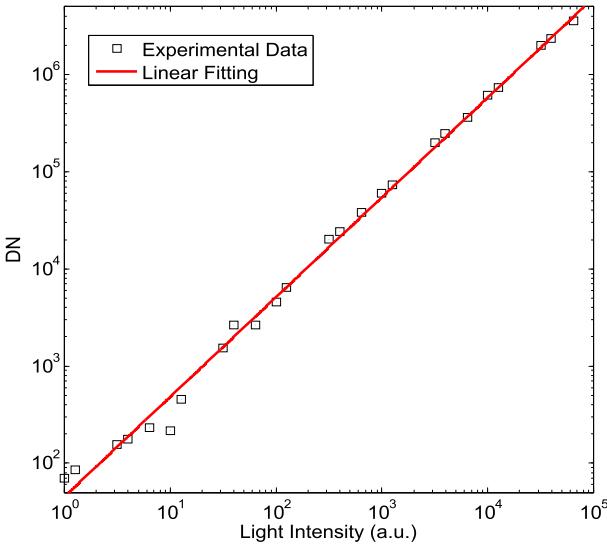


Fig. 13. (a) Chip microphotograph. (b) Pixel layout.

Fig. 14. Measured sensor outputs (DN) versus illumination over five decades. Red lines indicate the linear data fitting. The determination coefficient is $r^2 = 0.9961$.

exposed to light to avoid saturating the AER communication circuitry. Neutral density filters were put in between the source and the sensor to gauge the sensor outputs for different illumination values. The dependence between the output code and illumination is highly linear in the entire operation range. We computed the determination coefficient, obtaining $r^2 = 0.9961$. Linearity is an advantage of this sensor over other based on multiple exposition times or [5]–[9].

We studied the sensor response with low illumination, which is not entirely linear in these circumstances. The reason is that, in Fig. 3, the transistors M_{n3} , M_{p2} , and M_{p3} current leakage and the photodiode dark current are comparable to the photocurrent. That limitation is mainly imposed by the technology. Hence, under very low illumination conditions the oscillation period can be approximated by

$$T = \frac{C \cdot \Delta V}{I_{ph} + I_{dark} - I_{leakage}} = \frac{C \cdot (V_{DD} - V_{bot})}{I_{ph} + I_{dark} - I_{leakage}} \quad (10)$$

where I_{dark} is the photodiode dark current, and $I_{leakage}$ is the current leakage due to transistors M_{n3} , M_{p2} , and M_{p3} in Fig. 3. To illustrate the effect, we measured under very low illumination conditions (scene illumination was below 5 lux)

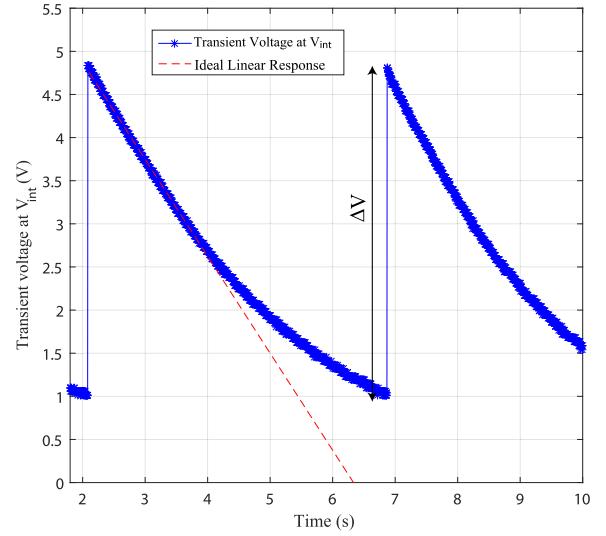
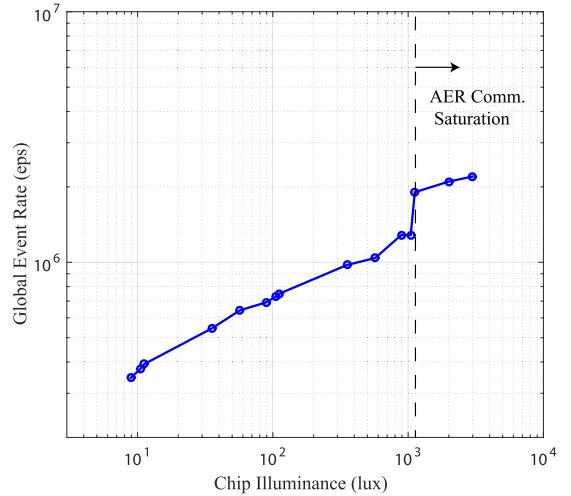


Fig. 15. Measured transient voltage at the integration capacitance of one pixel under low illumination conditions. Scene illumination was below 5 lux.

Fig. 16. Measurements taken with high illumination to illustrate how the AER communication circuitry delays limit the maximum illumination values that can be sensed. The whole pixel array was illuminated uniformly removing the optics. An infinite integration time was set. Pixel event rates were measured for different illumination values. ΔV was set to 1 V. Above certain illumination values, the event rate reaches its maximum value, leading to a non-linear dependence between event rate and illumination.

the transient voltage at the integration capacitance of a test pixel, placed in one corner of the pixel array. Its integration capacitance was connected to a scan buffer as that depicted in Fig. 8. The pixel response is plotted in Fig. 15 in blue trace. The red dotted lines plot the expected behavior. It can be seen that when the voltage at the integration capacitance decreases, $I_{leakage}$ has a higher impact on pixel performance leading to a nonlinear pixel response. Therefore, $I_{leakage}$ depends on the value that is set by the user to ΔV . The higher the ΔV is set, the higher the transistor leakage impact will be under low illumination. If we decrease ΔV , the event rate will increase. Thus, there is a trade-off between pixel linearity under low illumination and the event rate. Note that long integration times had to be set to observe the situation depicted in Fig. 15. Pixel sensitivity could be enhanced using a dedicated

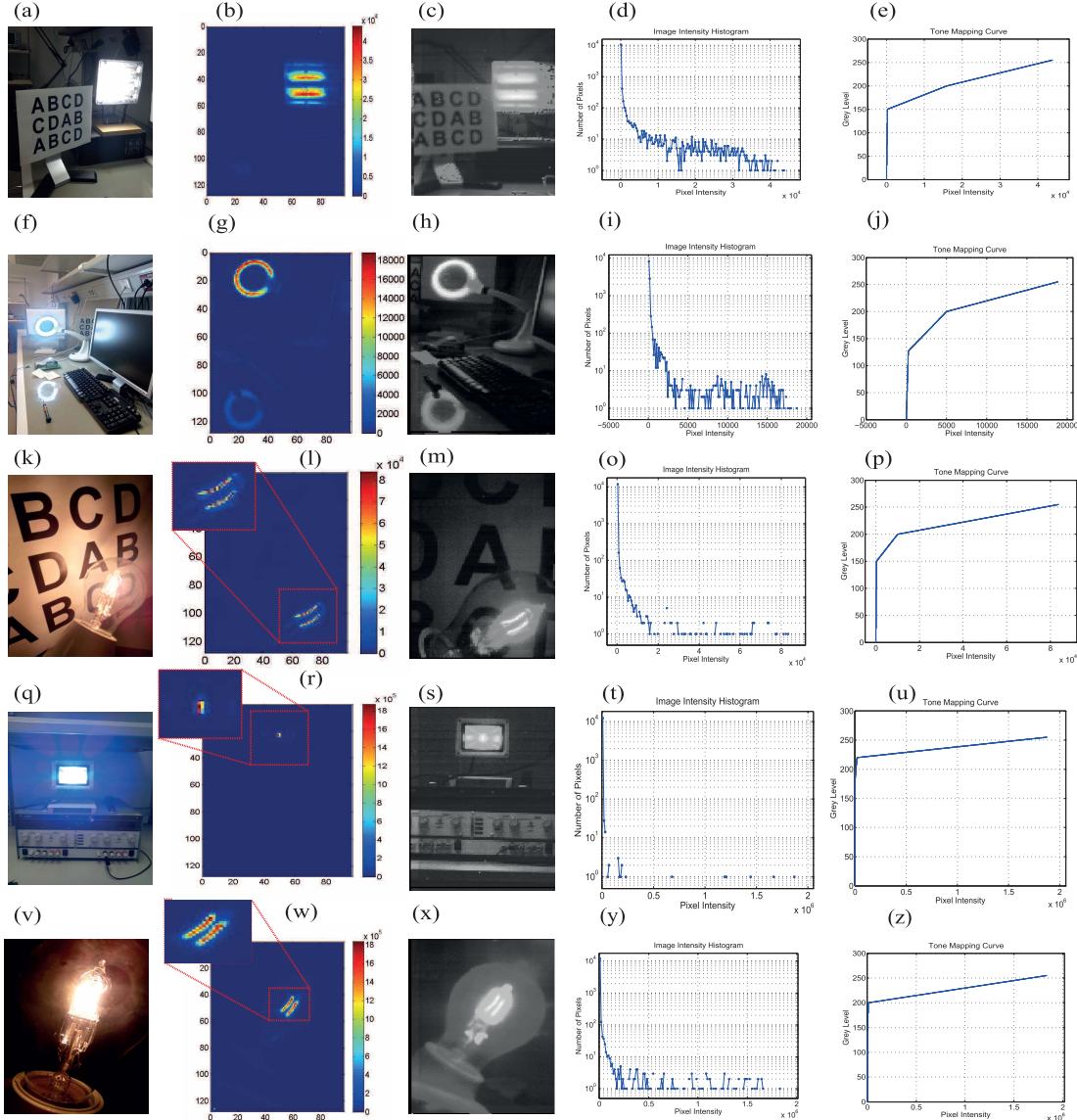


Fig. 17. From left to right: sample HDR images. (a), (f), (k), (q), and (v) Snapshots of HDR scenes taken with a BQ AQUARIS E4.5 smartphone operating in HDR mode. (b), (g), (l), (r), and (w) Outputs of our sensor using a thermal code to encode intensity levels. (c), (h), (m), (s), and (x) Same images after processing them with a TM algorithm. (d), (i), (o), (t), and (y) Image histograms. (e) (j) (p) (u) and (z) TM curves employed to encode gray levels for each image. Measured intra-scene dynamic ranges were 93, 86, 99, 125, and 126 dB for visual scenes (a), (f), (k), (q), and (v), respectively. We set an integration time $T_{int} = 110$ ms to capture all the images. Event rates were 87, 60, 300, 59, and 435 keps for visual scenes (a), (f), (k), (q), and (v), respectively.

CIS technology or by reducing the sensing capacitance. The penalty will be faster event rates with the same illumination.

As discussed in Section II-C, the arbitration delays of the peripheral circuitry limits the maximum illumination values that can be sensed. Fig. 16 illustrates this effect. We illuminated the whole sensor array with uniform light and we set an infinite integration time. The optics was removed. Thus, all pixels were spiking with a frequency proportional to light. When the event rate reaches a certain value, the dependence between event rate and illumination is not linear. Some rows are the only ones that are able to send events out of the chip [27]. For this reason, there is a fast growth on the dependence between illumination between the event rate when the chip luminance is close to 1 klux. Events of pixels of the same rows can be arbitrated faster. Then the event rate cannot

grow above a certain limit. Under these circumstances, not all the pixels will be able to transmit events off-chip. Hence, the values of illumination related to such pixels will not be correct. This is an unfavorable scenario. In practical situations, all the pixels will not be exposed to high illumination simultaneously. Event activity can be monitored with our interface. Faster AER arbitration circuitry that can reach 20 Meps is also reported elsewhere [26], [31].

D. Performance and Sample Images

A video showing some of the sensor capabilities is available [32]. Furthermore, Fig. 17 displays several samples of HDR images taken with the sensor. For comparison purposes, in the first column we show the same visual scene captured with a smartphone camera operating in HDR mode.

Its sensor was overexposed within the high illuminated regions of all the snapshots. In the second column, we display the intensity levels measured with our sensor. We have employed a linear thermal code to encode the linear sensor outputs. Using the three different color channels of the display, there are available up to 24 bits to encode illumination values linearly. Although this image representation is not close to our human perception of the visual scene, all the information provided by the sensor is preserved. It can be useful to operate with the raw data provided by the sensor in applications related to machine vision and pattern recognition. In the third column in Fig. 17, we display images rendered with our sensor after processing its output data with a TM algorithm. In the fourth column, we show the image histograms. In the right column, we display the non-linear law used to encode gray levels. We assign more gray levels in the resulting image to the illumination values that are more frequent in the visual scene. The user has total freedom to customize the TM curves. For the sake of simplicity, we have defined curves based on a piecewise approximation. The computation of the dynamic range of the sample images is straightforward according to (2). We measured intra-dynamic ranges of 93, 85, 99, 125, and 126 dB for the visual scenes (a), (f), (k), (q), and (v), respectively. We used a 6-mm C-mount lens to capture all the images, except image (s) that was taken with a 25-mm C-mount objective. An integration time, $T_{\text{int}} = 110$ ms was set to capture all the snapshots. The maximum spiking frequency for an individual pixel that we could measure was $f_{\text{peak}} = 55$ keps in the visual scene depicted in Fig. 17.(v). Such a pixel value corresponds to the illumination of the bulb filament in a very specific localization. If we take into account the maximum event rate that can tolerate the AER bus, the maximum number of pixels that could fire simultaneously at such speed is $\text{MAX}_{\text{BR}}/f_{\text{peak}} \approx 182$, that is, 1.5% the size of the pixel array.

E. Practical Application Scenarios

The event output data flow sends out the chip before the integration time is finished. Hence, it is possible to use this event information to display preliminary images before the final one is rendered. Fig. 18 illustrates it. An integration time $T_{\text{int}} = 110$ ms was set to capture an HDR scene. Preceding images were rendered with the events received at different time stamps. Gray levels were encoded using pulse density modulation (PDM). Higher illuminated pixels can be displayed first, only a few milliseconds after resetting the integration capacitance. On the right-bottom corner in Fig. 18, the resultant image is displayed. The sensor is potentially useful for application scenarios where a fast preview of the visual scene is required before rendering detailed images.

In Fig. 19, the sensor is used to detect transient illumination variations of a very bright source within an HDR scene that cannot be tracked with our eye or with a conventional camera. A neon tube circular lamp was placed in the scene. It has a radiance of 32 klux. In Fig. 19(a), a picture of the visual scene taken with a cell phone camera in HDR mode is shown. In this case, it is not possible to detect transient variations of intensity levels after turning on the lamp. We can appreciate

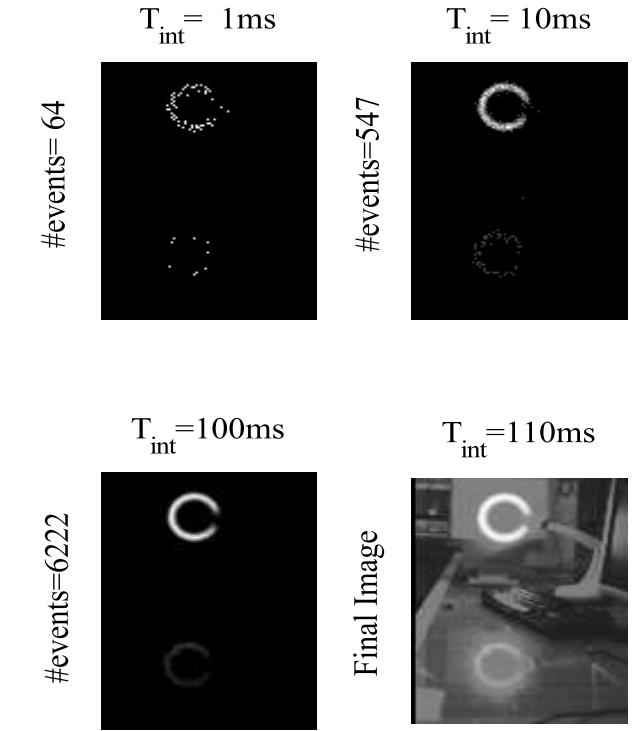


Fig. 18. Representation of the sensor event output data on several time stamps before the integration time is finished. Bottom-right corner: final resultant image.

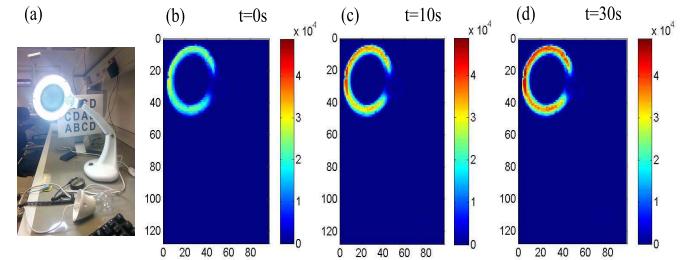


Fig. 19. Detection of transient illumination variations of a very bright source. (a) Capture of the original scene taken with a commercial camera in HDR mode. Illumination variations could not be detected after turning on the lamp. (b)–(d) Snapshots taken with the sensor at different time intervals. Variations of highest illuminated regions can be detected. The lamp radiance was 32 klux.

the transient evolution of the intensity levels emitted by the source [see Fig. 19(a)–(c)]. The maximum intensity level is not reached until 30 s after turning on the lamp.

F. Power Consumption

Chip power consumption depends on the frame and event rates, as depicted in Fig. 20. The main sources of power dissipation are the column-parallel ramp ADCs, and the source followers of each column (see Fig. 6). This is a static power that is always dissipated unless we disable the APS output. Moreover, there is a dynamic power consumption that depends on the FR (see Fig. 20, top). The digital circuitry is dedicated to store and send out the chip; the stored ADC outputs increase its consumption with the FR. Such dependence is approximately linear. Additionally, there is digital power consumption that depends on the event rate as displayed in Fig. 20,

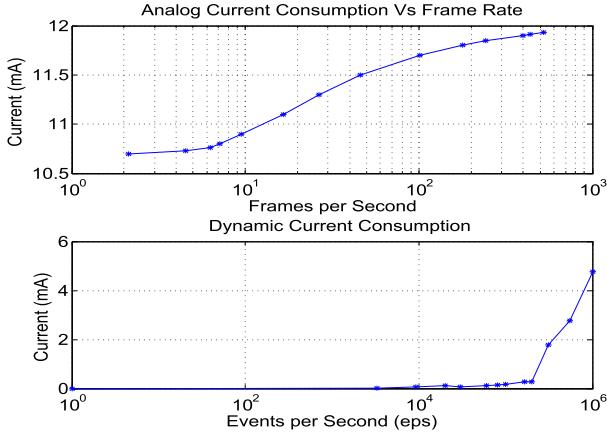


Fig. 20. Chip current consumption. Top: analog current consumption for different FRs. Bottom: digital current consumption (event outputs). It grows approximately linearly with the event rate.



Fig. 21. Captures rendered with the jaER interface and the sensor operating only with the event output data flow. In this operation mode, gray levels are encoded using PDM.

bottom. Digital chip current consumption is below 4 mA under normal operation event rates. Above 40 keps, the digital power dissipation grows exponentially because the periphery has to handle multiple simultaneous requests from different pixels. Examining both graphs, we can expect a total current consumption below 16 mA with the sensor operating in most illumination conditions. The analog power consumption is lower than 12 mA with FRs below 100 frames/s. The total power dissipation is approximately 58.6 mW.

G. Fixed Pattern Noise, Read Noise, and SNR

The sensor photo response non-uniformity (PRNU) of the APS readout was measured illuminating the sensor with a white Lambertian source. The measured value for the APS output (half range) is 3.5%. The integration time was set to avoid firing events during the integration period. To measure other sensor parameters, such as the read noise and the conversion gain, we use the photon transfer curve method proposed in [33]. The results are reported in Table I. In parallel, we measured the FPN of the event output. We followed the same procedure as in the previous experiment, but we increased the integration time to make all the pixels fire. The measured event output deviation with $\Delta V = 4$ V was 2.6%. Such pixel mismatch feature is mainly provoked by the offset of the oscillator comparator, the variations of the capacitor resetting time, and the variations of the reset amplitude. The last source of mismatch can be reduced with a thoughtful design of the

TABLE I
SENSOR FEATURES

Technology	AMS 0.18μm HV
Power Supply	1.8V/5V
Chip Dimensions	4120μm × 3315μm
Pixel Size	25μm × 25μm
Number of Pixels	96×128
Pixel Complexity	34 Transistors + 2 Capacitors
Fill Factor	10%
Dynamic Range	125dB@3fps, 105dB@30fps
Frame Rate (APS readout)	0.1-200fps
Event sensitivity	963events/(s-lux) with $\Delta V=1$ V
Power Consumption	58.6mW@100frames/s, 200keps
APS Conversion Gain	$8e^-/DN$
APS Read Noise	$22e^-$
Sense Node Capacitance	45fF
SNR APS readout	35dB
PRNU (APS)	3.5%
FPN (event output)	2.6%
Max. event rate	2Meps (same row), 10Meps (different rows)
ADCs conversion speed	3.5MSamples/s

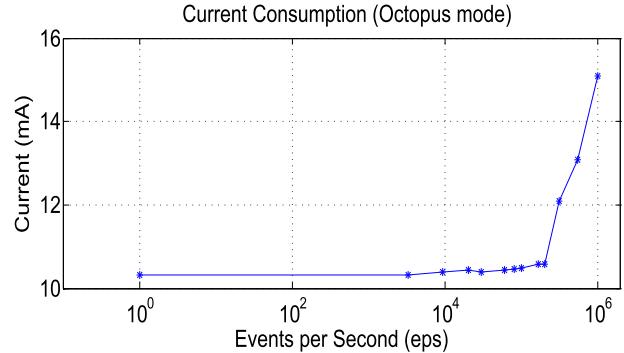


Fig. 22. Chip current consumption versus event rate with the sensor operating in octopus mode and with the APS readout disabled. There is a fixed standby power consumption. Beyond it, the power consumption is approximately proportional to the event rate.

pixel reset transistor (M_{p3} in Fig. 3). On the one hand, the aspect ratio should be as high as possible to minimize T_{reset} . On the other hand, the transistor length should be high enough to minimize the mismatch impact.

H. Event-Based Operation

The sensor can also operate just using the event data flow performing a light to frequency conversion. In this operation mode, gray levels are encoded using PDM. Pixels spike asynchronously with a frequency proportional to light intensity [18], [28]. The concept of frame is abandoned. To operate in this way, we set $\Delta V = V_{DD} - V_{bot} = 1$ V. The APS readout circuitry can be disabled. We have also added to our PCB an IDC-40 output compatible with the USBAERmini datalogger and the jaER interface [34]. See details of the board's connectivity in Fig. 11(b). Fig. 21 shows several snapshots taken in this operation mode with the jaER interface. The advantages of this operation mode are low

TABLE II
STATE-OF-THE-ART COMPARISON

Work	DR (Light Intensity Detection)	Technique	Off-chip Processing Required	Linear Intensity Output	Pixel Size	Output Format	Power Consumption	Fill Factor	Frame Rate
Sasaki 2007 [5]	88.5dB	Multi-exposure (long exposure + multiple short exposures)	No	No	10μm × 10μm	APS	ND	ND	30fps
Mase 2005 [6]	119dB	Multi-exposure (4 exposures)	Yes	No	10μm × 10μm	APS	130mW	54.5%	20-30fps
Yamada 2008 [8]	140dB	Multi-exposure (in-pixel)	No	No	8μm × 8μm	APS	ND	ND	30fps
Orly 1997 [7]	109dB	Multi-exposure (2 exposures)	Yes	No	20.4μm × 20.4μm	APS	19.5mW	15%	ND
Akahane 2006 [9]	207dB	Multi-exposure & logarithmic compression	Yes	No	20μm × 20μm	APS	ND	ND	ND
Vargas 2014 [13]	151dB@0.125fps, 123.3dB@25fps, 121.7dB@30fps	Tone Mapping (on chip)	Yes	No	33μm × 33μm	APS	111.2mW	0.8%	0.125-30fps
Hamamoto 2001 [22]	> 56dB	Self-reset mechanism. Local adaptation to light and motion (1-bit pixel memory)	No	Yes	85μm × 85μm	APS or Transient Difference	150mW	14%	ND
Yuan 2009 [25]	95.3dB	No	Yes	Self-reset mechanism (1-bit pixel memory)	25μm × 25μm	APS	316 μW	27%	15fps
Sasagawa 2016 [24]	ND	Yes	Yes	Self-reset mechanism without pixel memory	15μm × 15μm	Transient Difference	185mW	31%	300fps
This work	130dB@0.7fps, 125dB@3fps, 105dB@30fps	Linear Response (self-resetting mechanism)	No	Yes	25μm × 25μm	APS and/or Event-based	58.6mW@ 100fps, 200keps	10%	0.5-200fps

power consumption, good temporal resolution, and speed. The drawbacks are less image quality and less intra-scene dynamic range. Fig. 22 displays the dependence between the event rate and the chip current consumption in octopus mode. It can be noted that there is a static standby power consumption that does not depend on the event rate. The dependence between the event rate and the digital power consumption is approximately linear above 100 keps. The dynamic range is limited by the maximum data throughout the arbitration system and the desired speed to obtain a response from the sensor with low illumination. If we target for pixel responses above 1 frame/s, the dynamic range in this operation mode is about 70 dB. The maximum illumination values that we have measured are about 15 klux, without saturating the arbitration periphery.

V. BENCHMARKING AND COMPARISON

Table II summarizes the features of relevant HDR image sensors. The top ones [5]–[9], [13] are APS sensors. Devices [5]–[9] employ multi-exposure techniques to increase the dynamic range. Their outputs are not linear because several frames captured with different integration times are combined to render one. Methods based on multi-exposure to extend the dynamic range with APS sensors are implemented at the expense of sacrificing the output linearity, and increasing the sensor complexity. Some of them require external off-chip processing to render the final image. The sensor proposed by Vargas-Sierra *et al.* [13] implements on-chip TM compression, achieving HDR at video rates, with a low number of bits to encode light intensity. Its outputs are neither linear with illumination. Off-chip processing is required to compute image histograms before rendering the final frame [6], [7].

Finally, sensors [22], [24], [25] use a self-resetting mechanism as that described in this paper. The first two sensors implement 1-bit-pixel memories, at the expense of increasing the pixel size and lowering the FR. The last sensor [24],

avoids pixel memories to keep a competitive pixel pitch. The penalty is that the number of self-resets of each pixel cannot be determined to render HDR images. The sensor is conceived to compute the transient difference between consecutive frames. The proposed sensor is the only one that offers linear output compatible with frame-based devices with HDR of operation. It also offers the possibility of operating as an octopus retina [18], [28] or as a classic APS sensor.

Compared to prior image sensors based on multi-exposure [5]–[9], the main advantage of our sensor is the possibility of rendering directly HDR images with only one integration time and without further frame post-processing. Output data format directly encodes the illumination values and it is compatible with frame-based devices and algorithms. For instance, we have demonstrated how TM algorithms can be used to process the sensor outputs. Sensor outputs are linear with illumination. Machine vision and applications that require a linear encoding of illumination can benefit from our sensor. Usually, merging different frames of stems based on multi-exposures create image artifacts like false edges and distort the interpretation of the visual scene [11]. The new sensor also offers a good trade-off between dynamic range, FR, power consumption, and pixel complexity.

If we refer to sensors with TM compression [13] or pure event-based sensors [14]–[19], the strength of our device is that its output data format is compatible with frame-based displays and algorithms. The final user does need to be aware of the inner event operation. Optionally, our sensor can operate as a pure event-based sensor, offering more flexibility.

Finally, sensors based on self-reset operation [22], [24], [25] can handle a limited number of over-exposures per pixel. The novel idea of using external AER communication to handle the pixel saturation has two straightforward advantages: first, we avoid internal pixel memories and counters, saving pixel area, and not limiting the maximum number of saturation times per pixel. Second, the event readout is made during the

integration period. It is not necessary to read in-pixel memories at the end of the integration time. Thus, pixel operation is faster.

With regard to the sensor limitations, our pixel architecture is a more complicated classic APS pixel. That could be a limitation for applications that require sensors with a large number of pixels with a fine pixel pitch. However, the development of 3-D design technologies could make this approach competitive in terms of area requirements. Currently, the highest illumination values that can be sensed are limited by the AER communication circuitry. Faster arbitration schemes are reported in the literature and could be easily adapted to our sensors because their pixel connectivity and area requirements are similar to ours [26], [31]. It would also be possible to split the pixel array into two subarrays with independent AER logic. Thus, by merging the two independent event data flows, the maximum event rate could be doubled.

VI. CONCLUSION

We have presented the very first image sensor whose pixels implement self-reset operation based on asynchronous event communication. The sensor has APS pixel operation combined with event-based pixel overflow detection. It has two independent data flows that can be either combined to render HDR images or displayed independently. Event operation is transparent to the final user. We have demonstrated that its outputs are linear with illumination. Its output data can be processed in multiple ways. There is a trade-off between dynamic range and speed that the user can exploit, according the desired maximum intra-scene dynamic range that can be measured. The sensor can achieve a DR higher than 130 dB. Power consumption is 58.6 mW. Its main advantages are its linearity, and its output data format is compatible with frame-based displays and algorithms. Possible practical application scenarios have been demonstrated. The proposed approach solves some of the limitations that previous pixels with self-reset operation have, i.e., the need for in-pixel memories and a limited number of self-resets per pixel.

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