A 25 Gb/s 1.13 pJ/b −10.8 dBm Input Sensitivity Optical Receiver in 40 nm CMOS

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***Abstract*— This paper describes the design of a 25 Gb/s energy-efficient CMOS optical receiver with high input sensitivity. By incorporating a current-boosting preamplifier with a dual-path time-interleaved integrating-type optical receiver, it provides 1:2 demultiplexing operation with a tolerance to lower bandwidth photodiodes. The bandwidth of current amplifier is chosen as 0.35× operating data rate for maximizing the receiver signal-to-noise ratio. Experimental results show that the receiver can achieve 25 Gb/s operation when integrated with a 9 or 17 GHz GaAs photodiode. Input sensitivities in the two cases are −7.2 dBm (w/i a 9 GHz photodiode) and −10.8 dBm (w/i a 17 GHz photodiode), respectively, for a bit error rate of less than 10^{-12}. In addition, a single-tap decision-feedback equalizer (DFE) is embedded to compensate photodiode bandwidth and improve input sensitivity. Integrated with a low-cost 9 GHz photodiode, the input sensitivity and timing margin of the receiver are improved by 2 dB and 0.25 UI, respectively, after DFE compensation. By utilizing a current integrator and time-interleaved comparators, its energy efficiency is 1.13 pJ/b at 25 Gb/s under a 1.2 V power supply. Fabricated in a 40 nm bulk-CMOS technology, the core circuit occupies a chip area of 0.007 mm^2 only.**

***Index Terms*— Comparator, current amplifier (CA), decision-feedback equalizer (DFE), integrating-type receiver, optical receiver, photodetector.**

I. Introduction

As THE applications of cloud service become pervasive in daily life, high-density and energy-efficient data links bridging computing and storage devices are demanding to accommodate the explosive bandwidth of data center. In contrast to electrical cables, optical interconnects enable lighter weight with wider channel bandwidth and lower electromagnetic interference. Conventionally, an optical receiver adopts a transimpedance amplifier (TIA) and a postlimiting amplifier (LA) to convert the photocurrent into logic-level voltage swing for postprocessing [1]–[3]. To achieve high input sensitivity, the TIA is made up of a voltage amplifier with large shunt-shunt-feedback resistors. As the TIA bandwidth is limited by the parasitic photodiode capacitance (C_{PD}), its power dissipation would be increased dramatically along with the data rate. On the other hand, a multistage LA also becomes more and more power hungry to meet the gain–bandwidth requirement for over 10 Gb/s operation.

Recently, comparator-based optical receivers [4]–[9] have attracted many research interests and demonstrated superior energy and area efficiency compared with conventional TIA + LA-based counterparts. In the receiver front-end, they can be realized by using either a photocurrent integrator [4]–[7] or a TIA stage [8], [9] followed by voltage samplers and comparators.

As is proposed in [4] [or Fig. 5(a)], the photocurrent is integrated over a sampling capacitor (C_S) in parallel with the parasitic C_{PD}, so as to convert it into voltage form directly. As the integration time is inversely proportional to operating data rate, the integrating voltages as well as the corresponding signal-to-noise ratio (*SNR*) are severely limited by the integrating capacitances ($C_S + C_{PD}$) at high-speed operation. Furthermore, an integrating-type optical receiver is less tolerant to run length of consecutive identical digit (CID) bits. This problem can be circumvented by shunting an input resistor in parallel with a photodiode [5] [or Fig. 5(b)], but it unavoidably introduces excess noise associated with the bleeding resistor to the receiver. Also, in order to ensure equal voltage swing across a string of identical consecutive bits, it requires additional circuit functionality to dynamically modulate slicer offset (DOM). Another approach to circumvent CID issue is by periodically resetting the integrators, but they also suffer from sensitivity degradation owing to either shorter integration time (0.5 UI in [6] or Fig. 6) or larger integrating capacitances [7]. By these means, a photodiode with a small C_{PD} is crucial for a high input sensitivity at a high-speed operation. As a compromise between input sensitivity and power consumption, [8] and [9] used TIAs in front of the comparators to avoid meta-stability, but with different strategies for TIA bandwidth design. Liu *et al.* [8] used a wide-bandwidth TIA, while Raj *et al.* [9] proposed a low-bandwidth TIA with DOM to resolve the exponential settling behavior.

To overcome the aforementioned shortcomings in the prior art [4]–[9], this paper proposes a high input sensitivity optical receiver with a tolerance to lower bandwidth photodiodes, which is composed of a current-boosting preamplifier followed by a dual-path time-interleaved DFE embedded integrating-type demultiplexer. By utilizing a current amplifier (CA) in the front-end, the photocurrent is first boosted up before being fed into the following current integrators for demultiplexing. In contrast to [8] and [9] that used a TIA to decouple a voltage sampler and a photodiode, a CA is utilized in this design to buffer the input signal and the current integrator. Also,

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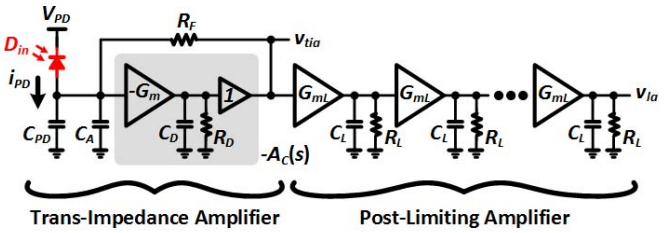

Fig. 1. Conventional TIA + LA optical receiver front-end.

compared with conventional integrating-type optical receivers in [4]–[7], the proposed architecture decouples the sampling capacitor (C_S) with the C_{PD} for a higher *SNR*. Moreover, the receiver is highly tolerant to photodiode and CA bandwidth by the current-integrating scheme. Thus, the CA current gain can be maximized to improve input sensitivity. In addition, a single-tap DFE is embedded to compensate for bandwidth imperfection associated with the photodiode and the CA.

This paper is organized as follows. Section II reviews the merits and demerits of conventional optical receivers in the literature, including TIA, LAs, and integrating-type counterparts. Section III describes the proposed CA-based time-interleaved integrating-type optical receiver. Design considerations in terms of bandwidth and *SNR* optimization are also discussed. Section IV presents the system implementation and design details of the low-noise CA, clocked comparator, and single-tap DFE. Section V summarizes the measurement results, and Section VI draws the conclusion.

II. Conventional Optical Receiver Front-End

A. TIA + LA Receiver Front-End

Typically, the optical receiver analog front-end is composed of a TIA followed by a LA, as shown in Fig. 1 [1]–[3]. The TIA first converts photocurrent (I_{PD}) into voltage domain (v_{TIA}), and then the post-LA enlarges the output voltage (v_{LA}) swing into logic level for succeeding clock-and-data recovery circuit. Let $v_{n,A}$ and $v_{n,LA}$, respectively, represent the input-referred noise voltage PSD of the TIA's core amplifier [$A_c(s)$] and the LA, and R_F is the TIA's feedback resistor, the input-referred noise current PSD ($i_{n,RX}$) of the optical receiver can be derived as

$$\overline{i_{n,RX}^2} = \frac{4kT}{R_F} + \frac{\overline{v_{n,A}^2}}{R_F^2} + \frac{\omega^2 C_{tot}^2 \overline{v_{n,A}^2}}{R_F^2} + \frac{\overline{v_{n,LA}^2}}{|T_Z^2|} \tag{1}$$

where $C_{tot} = C_{PD} + C_A$ and T_Z denotes the TIA gain. As is shown in Fig. 1, assuming that $A_c(s)$ is approximated as a single-pole voltage amplifier, the T_Z can be derived as

$$T_Z(s) = \frac{R_F}{\frac{R_F C_{tot} C_D}{G_m} s^2 + \frac{R_F C_{tot} + R_D C_D}{G_m R_D} s + \frac{1}{G_m R_D} + 1}. \tag{2}$$

For a maximally flat gain response ($\zeta = 0.707$), the TIA's 3 dB bandwidth (ω_{TIA}) can be derived as [10]

$$\omega_{TIA} = \frac{\sqrt{2} G_m R_D}{R_F C_{tot}} \tag{3}$$

where $G_m R_D$ is the dc gain of $A_c(s)$, whose 3 dB bandwidth (ω_A) should be chosen as

$$\omega_A = \frac{1}{R_D C_D} = \sqrt{2}\omega_{TIA}. \tag{4}$$

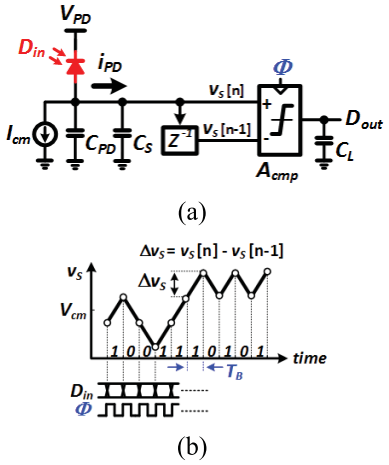

Fig. 2. (a) Conventional integrating-type optical receiver front-end, and (b) its corresponding integrating voltage.

According to (1) and (3), it can be seen that the TIA's input-referred noise current and its 3 dB bandwidth trade off against each other. Also, the gain–bandwidth requirement ($\omega_{T,A}$) of $A_c(s)$ becomes

$$\omega_{T,A} = (G_m R_D)\omega_A = R_F C_{tot} \omega_{TIA}^2. \tag{5}$$

As the TIA's power consumption is dominated by $A_c(s)$, given C_{tot} and R_F, we have

$$I_{TIA} \propto \omega_{T,A}^m \propto \omega_{TIA}^{2m}. \tag{6}$$

Theoretically, m is between 1 and 2. Thus, the estimated power dissipation would be increased significantly along with the TIA's bandwidth (or its data rate).

On the other hand, considering an N-stage cascaded LA, if each stage is modeled as a single-pole gain cell with a voltage gain of $G_{mL}R_L$ and a 3 dB bandwidth of ω_{cell}, its overall gain (A_{LA}) and bandwidth (ω_{LA}) can be approximated as

$$A_{LA} = (G_{mL} R_L)^N \tag{7}$$

$$\omega_{LA} = \omega_{\text{cell}} \sqrt{2^{1/N} - 1}. \tag{8}$$

The total current dissipation of the LA can be approximated as

$$I_{LA} \propto N(A_{LA})^{2/N} \left(\frac{\omega_{LA}}{\sqrt{2^{1/N} - 1}} \right)^m. \tag{9}$$

Similar to (6), m is between 1 and 2. According to (6) and (9), it can be seen that the power dissipation of both the TIA and the LA will increase drastically at high-speed operation, and leads to energy inefficiency. Shunt-peaking inductors are commonly utilized for bandwidth enhancement, and somewhat reduce power dissipation at the expense of larger chip area. They can hardly be applied in high-density optical links.

B. Integrating-Type Receiver Front-End

Recently, integrating-type optical receivers [4]–[7] have drawn many research attentions and demonstrated superior energy and area efficiency compared with conventional TIA + LA-based architectures. As is shown in Fig. 2, it is composed of a current integrator followed by a full-rate clocked comparator. By differentiating $v_S[n]$ and $v_S[n-1]$ through a comparator, the input data can be recovered by detecting the polarity of integrating voltage (Δv_S), which is

$$\Delta v_S = v_S[n] - v_S[n-1]. \tag{10}$$

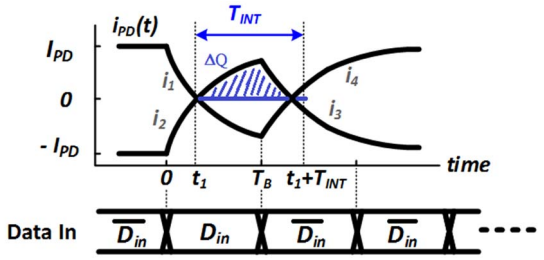

Fig. 3. Worst case scenario for the integrating voltage (Δv_s).

When data ONE are received, v_S will be charged during the bit time, such that $\Delta v_S > 0$. On the contrary, v_s will be discharged when data ZERO are received, thus $\Delta v_S < 0$. Taking the photodiode bandwidth into account, Δv_S in 1 *UI* integration time can be described as

$$\Delta v_S = \frac{\int i_{PD}(t)dt}{C_{PD}+C_S} = \frac{\alpha_{INT} I_{PD} T_B}{C_{PD}+C_S} \tag{11}$$

where α_{INT} is a photodiode bandwidth-dependent coefficient, T_B is the bit time, and $i_{PD}(t)$ and I_{PD}, respectively, represent the instantaneous and the dc photocurrent over the integration time, which are both bandwidth-limited.

To characterize α_{INT}, the photodiode bandwidth is modeled as a single-pole low-pass filter for simplicity. The worst case integrating voltage (Δv_s) occurs when a ZERO (or ONE) pulse is received after a long run of ONEs (or ZEROs). As shown in Fig. 3, the minimum integrating voltage can be found as the total charge ΔQ (the enclosed shadowed area) divided by the total integrating capacitance ($C_{PD}+C_S$). Here i_1 and i_2(i_3 and i_4) are the differential input currents of the integrator. Assuming that the photocurrent bandwidth (ω_p) is approximated by a single-pole model, we have

$$\Delta Q = \int_{t_1}^{T_B} i_2(t)dt + \int_{T_B}^{t_1+T_{INT}} i_3(t)dt \tag{12}$$

$$i_2(t) = I_{PD}(1-2e^{-\omega_p t}) \tag{13}$$

$$i_3(t) = I_{PD}(-1+2(1-e^{-\omega_p T_B})e^{-\omega_p(t-T_B)}). \tag{14}$$

For a 1 *UI* integration time, the maximum integrating voltage can be derived as

$$\Delta v_S = \frac{I_{PD}T_B}{C_{PD}+C_S} \times \left[1-2\frac{t_1}{T_B}+\frac{2}{\omega_p T_B}(1-2e^{-\omega_p t_1}+e^{-\omega_p T_B}e^{-\omega_p t_1})\right] \tag{15}$$

where

$$t_1 = \frac{1}{\omega_p}\ln(2-e^{-\omega_p T_B}) \tag{16}$$

$$\alpha_{INT} = 1-2\frac{t_1}{T_B}+\frac{2}{\omega_p T_B}(1-2e^{-\omega_p t_1}+e^{-\omega_p T_B}e^{-\omega_p t_1}). \tag{17}$$

To investigate the impacts of the photodiode bandwidth on the integration voltage, the α_{INT} under different photodiode bandwidths (in terms of data rate) is shown in Fig. 4. For $\alpha_{INT} > 0$, the photocurrent bandwidth should be higher than 0.15 D_R.

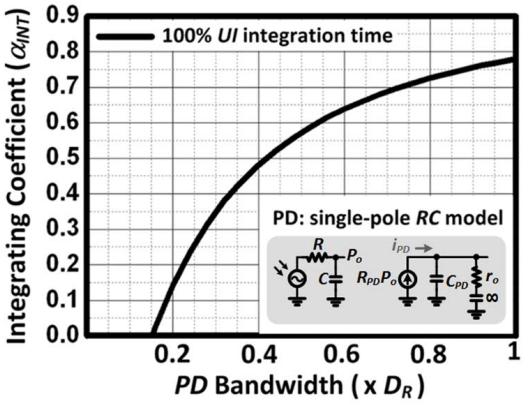

Fig. 4. α_{INT} versus I_{PD} bandwidth with single-pole *RC* model.

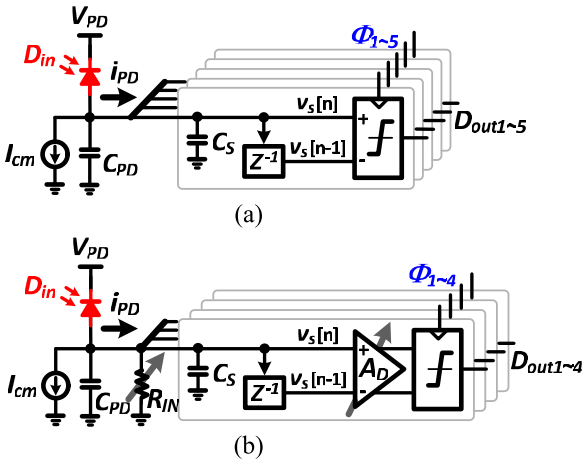

Fig. 5. Time-interleaved integrating-type optical receiver (a) without and (b) with shunting an input resistor [5].

By cascading a current integrator with a dynamic comparator, the effective transimpedance gain (A_{RX}) can be derived as

$$A_{RX} = \frac{v_{\text{out}}}{I_{PD}} = \left(\frac{\alpha_{INT}T_B}{C_P+C_S}\right) exp\left(\frac{g_m T_R}{C_{\text{out}}}\right) \tag{18}$$

where g_m is the transconductance gain of the dynamic comparator, T_R is the regeneration time of the latch, and C_{out} denotes the parasitic capacitance at the comparator output. According to (18), A_{RX} can be boosted exponentially by increasing g_m and T_R. To achieve a higher input sensitivity and relax the speed requirement of the clocked comparator, a common approach is to extend the T_R by using a time-interleaved architecture [4]–[9], as is shown in Fig. 5(a).

A major drawback of the integrating-type receivers is that they are less tolerant of CIDs, which may overload the integrator. To circumvent the CID issue, [5] shunts an input resistor, R_{IN}, in parallel with photodiodes, as is shown in Fig. 5(b). It prevents voltage overload while receiving long-run CID bits. However, the receiver sacrifices data-dependent integrating voltage across a string of CID bits [5]. Thus, it requires additional circuit functionality to dynamically vary the slicer's offset voltage to maintain a constant slicer input swing. Also, the bleeding integrator unavoidably introduces excess noise into the receiver, which might degrade its input sensitivity.

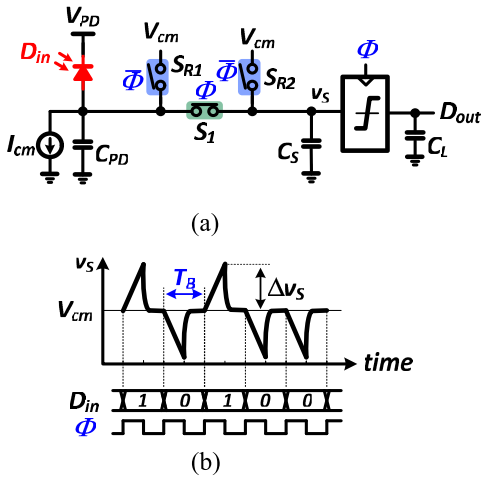

Fig. 6. (a) Resettable integrating-type optical receiver front-end, and (b) its corresponding integrating voltage.

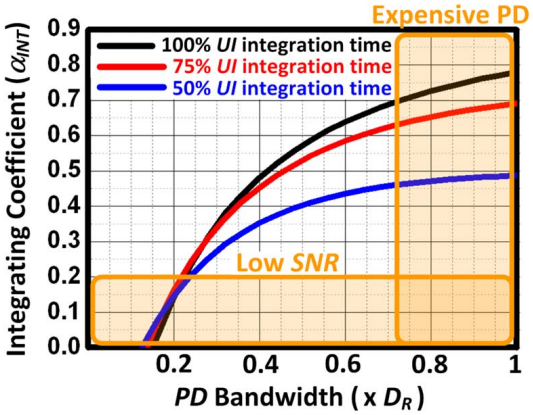

Fig. 7. α_{INT} versus I_{PD} bandwidth under different integration times.

C. Resettable Receiver Front-End

Another approach to eliminate CID issue is by periodically resetting both the sampling capacitor C_S and C_{PD}, before integrating the photocurrent [6], [7]. Fig. 6(a) shows the resettable receiver front-end. During $\Phi = 0$, both v_s and the input node are reset to V_{cm} through switches S_{R1} and S_{R2}. On the other hand, C_S starts to integrate photocurrent when switch S_1 is enabled during $\Phi = 1$. Fig. 6(b) illustrates the timing diagrams. The integration time is reduced by half, so is v_s and the corresponding *SNR*. Besides, a fast comparator is needed to resolve triangular wave v_s. Fig. 7 shows the maximum α_{INT} under different integration time (1, 0.75, and 0.5 *UI*) and with different photodiode bandwidths in terms of data rate (D_R). With a photodiode of 1 D_R bandwidth and a current integrator with 0.25 *UI* reset time, the α_{INT} is reduced by 10% for 0.75 *UI* integration time compared with that with 1 *UI* integration time. The difference of α_{INT} for 1 and 0.75 *UI* integration time is negligible. On the other hand, if the photodiode bandwidth is reduced to 0.3 D_R, the α_{INT} is reduced by half compared with that with a wide-bandwidth photodiode (1 D_R). As the photodiode bandwidth is less than 0.2 D_R, the integration time becomes less relevant to α_{INT}, but a smaller value would degrade the overall *SNR*.

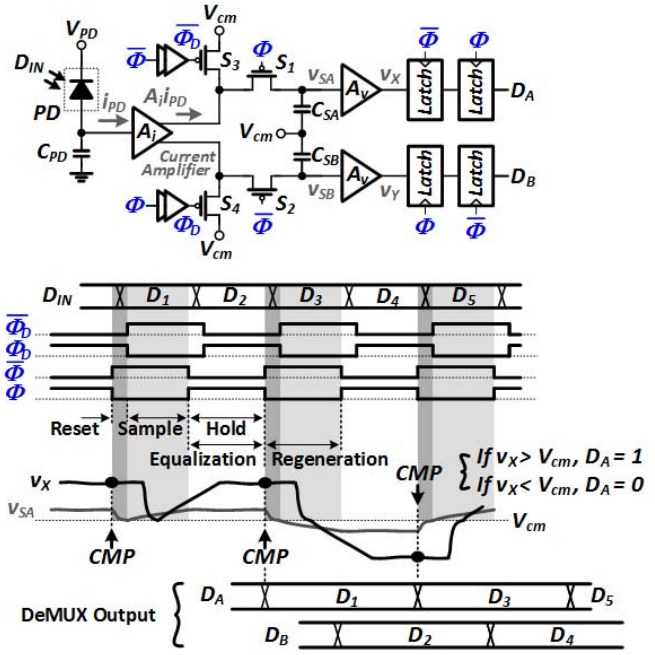

Fig. 8. Proposed CA-based time-interleaved integrating-type optical receiver.

III. Current-Amplifier-Based Optical Receiver

According to (18), the effective transimpedance gain in an integrating-type receiver shrinks as T_B is decreased. Meanwhile, the transimpedance gain is also limited by the parasitic capacitance associated with the photodiode. To overcome the aforementioned shortcomings, this paper proposes a CA combining with a time-interleaved integrating-type optical receiver. Fig. 8 illustrates the receiver architecture and the corresponding timing diagram. The input current (i_{PD}) generated from a photodiode is boosted by a CA (A_i). Then the switches (S_1, S_2) convey the amplified currents onto the sampling capacitors (C_{SA}, C_{SB}) alternatively. It also performs 1:2 demultiplexing through the preamplifier and the clocked comparator. The dual-path current integrators are operated in a ping-pong mode, and periodically reset to a common-mode voltage (V_{cm}) before sampling the input data. The switches (S_1, S_2) and (S_3, S_4) are driven by clocks (Φ, $\bar{\Phi}_D$) and ($\bar{\Phi}$, Φ_D), respectively, which provides reset/integrate/hold tristate operation [11]. The proposed scheme not only eliminates the CID issue but also relaxes the comparator speed requirement.

In this design, Φ_D lags Φ by about 10 ps, and the on-resistance of S_{1-4} is about 50 Ω, which is able to fully reset charges from C_{SA} and C_{SB} at 25 Gb/s operation. Thus, it provides 1 *UI* for CA reset, 0.25 *UI* for sampling charge reset, 0.75 *UI* for current integration, followed by 1 *UI* for latch regeneration. The corresponding α_{INT}, including CAs of either 17 GHz of 9 GHz −3 dB bandwidths, are about 0.63 and 0.41, respectively.

A. CA Bandwidth Optimization Under a Constant Gain–Bandwidth Product

The CA is made up of a transimpedance stage (T_Z) followed by dual-output transconductance stages (G_M), as is shown in

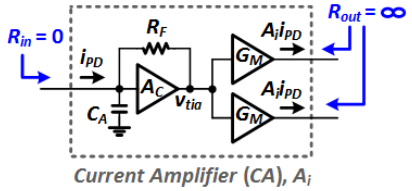

Fig. 9. Dual-path CA.

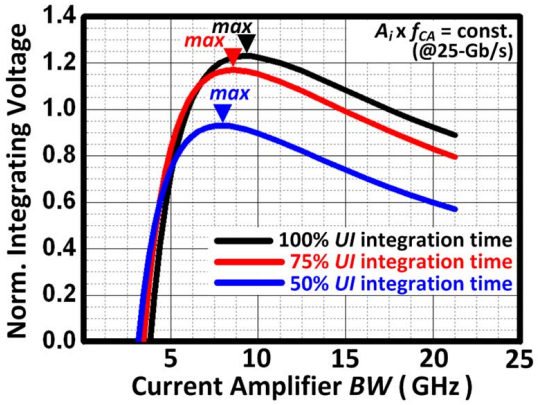

Fig. 10. CA bandwidth optimization.

Fig. 9. Fig. 10 illustrates the normalized integrating voltages versus CA bandwidth under a constant gain–bandwidth product. Compared with conventional TIA + LA-based optical receivers, where the TIA bandwidth is about 0.7 D_R, the proposed CA (TIA + G_M) can provide a higher gain with a lower bandwidth (0.35 D_R) for a maximizing integrating voltage. For a comparator-based receiver, its eye opening before slicer is critical to the overall input sensitivity. Thus, it is preferable to have a current-boost amplifier with a high gain and a relatively low bandwidth. On the other hand, it may impose a tighter timing margin for the sampling clock due to the remaining ISI effect. To overcome this issue, a single-tap DFE is incorporated in this design.

B. Input-Referred Noise

With a large R_F, the input sensitivity and the input-referred noise current of the optical receiver are generally dominated by the TIA. The input-referred noise current PSD of the receiver in (1) can be approximated as

$$\overline{i_{n,RX}^2} \approx \frac{4kT}{R_F} + \frac{\overline{v_{n,A}^2}}{R_F^2}. \tag{19}$$

By integrating (19) over its noise bandwidth (∼1.22 f_{3dB} for a maximally flat-band second-order TIA), the equivalent input-referred noise current ($i_{n,RX(rms)}$) can be approximated as

$$i_{n,RX(rms)} \approx \sqrt{\frac{4kT}{R_F} \cdot \left(1.22 \cdot \frac{1}{2\pi} \cdot \frac{\sqrt{2} G_m R_D}{R_F C_{tot}}\right)} = \frac{1}{R_F}\sqrt{\frac{kTG_m R_D}{C_{tot}}}. \tag{20}$$

A lower-bandwidth TIA allows a larger R_F, and thus benefits from a better input sensitivity. In contrast to conventional TIA and LA, the proposed receiver front-end (TIA + G_M) incorporates a lower-bandwidth (reduced from 0.7 D_R to 0.35 D_R) and a higher-gain (2X) TIA with a current integrator, and benefits from 2× (3 dB in power) input sensitivity improvement. By simulation, the equivalent input-referred noise current is about 1.33 μA_{rms}, which results in an input sensitivity of 18.6 μA_{pp} at a bit error rate (BER) of less than 10^{-12}. The dark currents of commercial GaAs photodiodes are about several nanoamperes only. They can be negligible in considering the input sensitivity in this design.

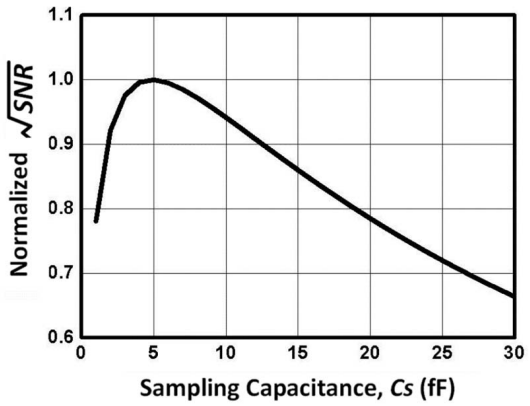

Fig. 11. S/N magnitude ratio versus sampling capacitance C_S.

C. C_S Optimization

In an integrating-type receiver, the sampling clock timing jitter (σ_{CK}), CA (σ_{CA}) output noise, thermal noise of sample and hold (σ_S), and input-referred noise of comparator (σ_C) will lead to the degradation of SNR. The corresponding SNR can be expressed as

$$SNR = \frac{v_S^2}{\sigma_S^2 + \sigma_C^2 + \sigma_{CA}^2 + \sigma_{CK}^2}. \tag{21}$$

The jitter-induced noise voltage is contributed by the skew variation between the input data (I_{CA}) and the sampling clock [12]. By simulation, σ_{CK} is about 0.5 mV_{rms} considering a clock jitter of 0.5 ps_{rms}.

As the CA's output impedance is finite at a high-frequency operation, the noise contribution from a fully differential sample/hold circuit is less than (the worst case scenario)

$$\sigma_S = \sqrt{\frac{2kT}{C_S}}. \tag{22}$$

Assume that the CA provides an output current of I_{CA} and a parasitic capacitance of C_P at the output nodes. By (11), the integrating voltage at CA's output can be revised as

$$v_S = \frac{\alpha_{INT} T_B I_{CA}}{C_P + C_S}. \tag{23}$$

Here α_{INT} includes the bandwidth limitation of both the photodiode and CA. By substituting (22) and (23) into (21), we arrived at

$$\sqrt{SNR} = \frac{\alpha_{INT} T_B I_{CA}}{(C_P + C_S)\sqrt{\frac{2kT}{C_S} + \sigma_C^2 + \sigma_{CA}^2 + \sigma_{CK}^2}}. \tag{24}$$

Device	Size
$W/L_{1\sim2}$	4.8µ/60n
$W/L_{3\sim4}$	0.4µ/60n
$W/L_{5\sim6}$	4.8µ/60n
I_{B1}	1.2 mA
I_{B2}	100 µA
$R_{B1\sim2}$	12 kΩ
I_{CM}	50 µA
$W/L_{MS1\sim2}$	6.0µ/40n
W/L_{MS3}	3.0µ/40n
$C_{SA1\sim2}$	16 fF
$I_{OS1\sim2}$	0~50 µA
$R_{F1\sim2}$	3 kΩ

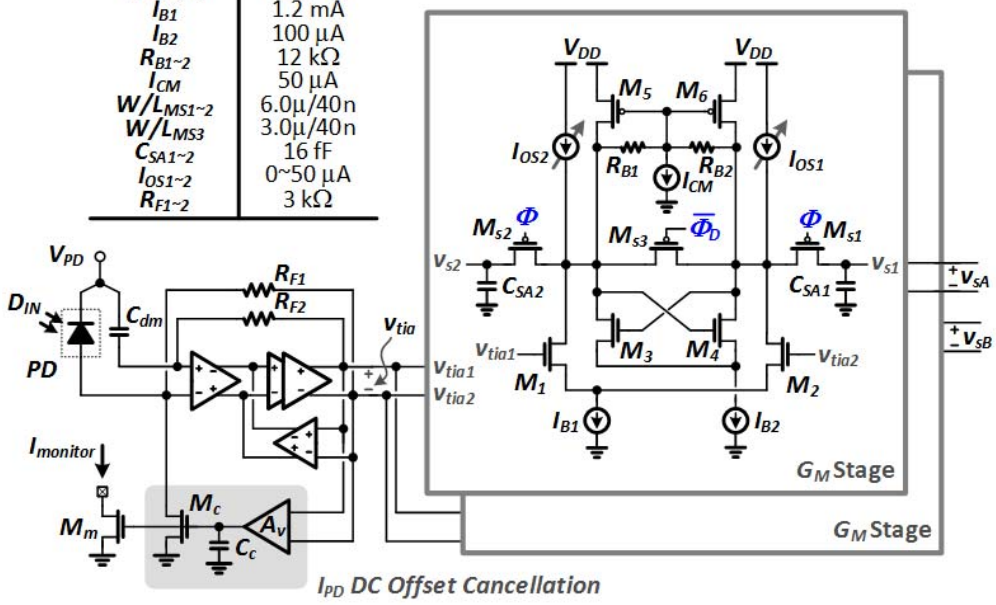

Fig. 12. Low-noise CA with current integrator.

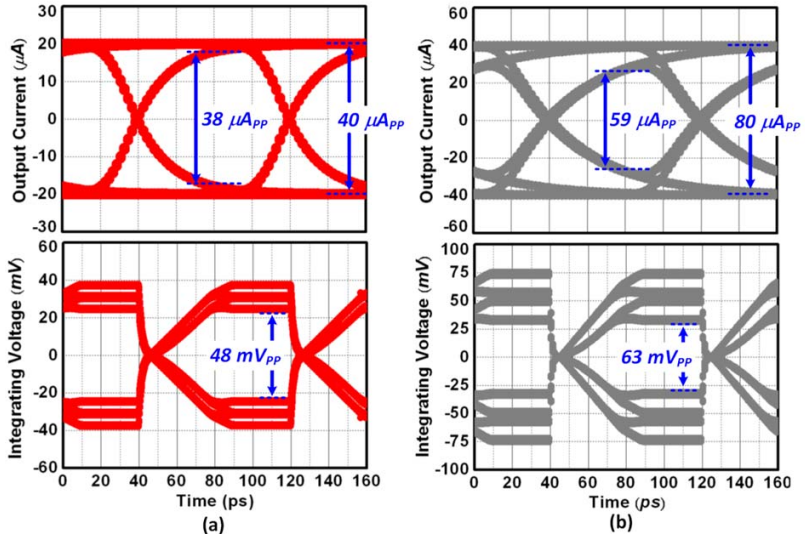

Fig. 13. CA output current and integrating voltage eye diagrams under different gains, bandwidths, and equal power consumption. (a) $I_{PD} = 25\ \mu A_{pp}$ and CA with 18 GHz BW and 4 A/A current gain. (b) $I_{PD} = 25\ \mu A_{pp}$ and CA with 9 GHz BW and 8 A/A current gain.

The optimal C_S can be chosen by maximizing $\sqrt{SNR}$, and can be derived as

$$C_{S(opt)} = \sqrt{\eta^2 + C_P\eta} - \eta \tag{25}$$

where

$$\eta = \frac{kT}{2(\sigma_C^2 + \sigma_{CA}^2 + \sigma_{CK}^2)}. \tag{26}$$

By (24), it can be seen that C_S will degrade $\sqrt{SNR}$ in the extreme cases of a large (signal swing limited) and a small (thermal noise limited) capacitance value. Given C_P of about 30 fF, Fig. 11 illustrates the normalized $(SNR)^{1/2}$ versus sampling capacitance C_S. The optimal sampling capacitance $C_{S(\text{opt})}$ is about 5 fF for a higher *SNR*. Considering the Charge injection and clock feedthrough effect in a practical implementation, a 16 fF *Cs* is chosen. The expected *SNR* reduction is about 1.5 dB compared with that using the theoretically optimum value (5 fF).

IV. Detail Circuit Implementation

A. Low-Noise Current Amplifier

Fig. 12 shows the circuit schematic of the CA, which consists of a TIA cell followed by a dual-output G_M stage. The TIA is based on a nested-feedback architecture with a dc offset cancellation circuit for low-noise operation [13]. The G_M stage is composed of a source-coupled pair (M_1, M_2) with active loads (M_5, M_6, R_{B1}, R_{B2}). To enhance the

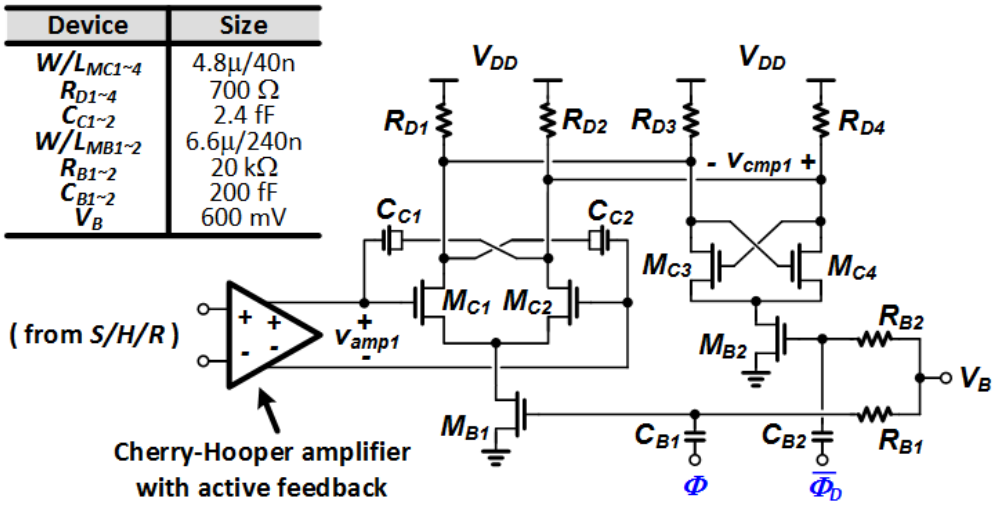

Fig. 14. Current-mode latch of the clocked comparator.

output impedance of CA so as to avoid current leakage, a negative-impedance converter (M_3, M_4) is added in parallel. Besides, the offset voltages of G_M stages and the succeeding comparators are foreground calibrated by the compensation current (I_{OS1}, I_{OS2}). By the proposed receiver scheme, a 9 GHz bandwidth (BW) photodiode can be utilized for 25 Gb/s operation with a superior sensitivity compared with the prior art in [1], [2], [12], and [14]. The input sensitivity can be potentially improved by 2× (or 3 dB) under a fixed power consumption. In this design, the gain and bandwidth of CA are about 18 dB and 9 GHz, respectively. Thus, no peaking inductors are needed at 25 Gb/s operation for an area-efficient implementation.

Fig. 13 illustrates the simulated eye diagrams of the output currents and the integrating voltages at 25 Gb/s operation under a constant gain–bandwidth product (i.e., a relatively constant power consumption) of CA. To investigate the integrator's output swing under different CA bandwidths, the photodiode bandwidth is ideal (5 ps T_R/T_F) with a photocurrent level of 25 μA_{pp}. The current gain (A_i) and 3 dB bandwidth (f_{3dB}) of CA in Fig. 13(a) and (b) are 8-A/A, 9 GHz and 4-A/A, 18 GHz, respectively. Thanks to the periodically resettable switches, the integrators are fully reset to zero at the end of the reset phase. The integrating voltage is increased by 1.31× by choosing a lower-bandwidth (9 GHz) and a higher gain (8 A/A) CA. Though the postintegrating voltage may have a higher ISI reflecting in different voltage levels, it can be eliminated by a clocked comparator.

B. Clocked Comparator

The 12.5 GS/s clocked comparator is composed of a preamplifier stage followed by two cascaded latches. The preamplifier is based on Cherry–Hooper amplifier with active feedback [15], which decouples the kick-back noise associated with the dynamic comparator. The circuit schematic of the current-mode latch is shown in Fig. 14, where the negative capacitors (M_{c9} and M_{c10}) are adopted to neutralize the Miller capacitors of M_{c1} and M_{c2} and alleviate the kickback noise.

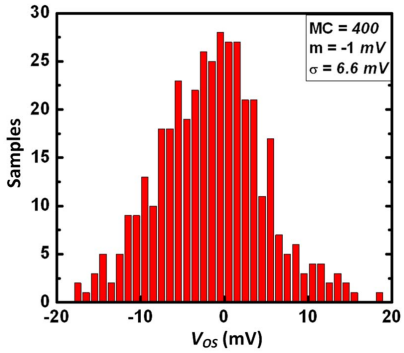

Fig. 15. Monte Carlo simulation of the clocked comparator.

In this design, the preamplifier provides a conversion gain of 19 dB and a bandwidth of 14 GHz to enable latch regeneration within 1 *UI* at the input sensitivity level of about 6 mV_{pp}. The comparator's offset voltage is characterized by Monte Carlo simulation, as is shown in Fig. 15. To compensate for $\pm 3\sigma$ offset spread under PVT variations, it is foreground calibrated in the integrating stage with offset currents I_{OS1} and I_{OS2}, as is shown in Fig. 12.

C. Decision-Feedback Equalizer

Another important advantage of the time-interleaved optical receiver is that a half-rate decision-feedback equalizer (DFE) [16], [17] can be easily embedded in it, so as to alleviate multimode fiber (MMF) dispersion, and also bandwidth imperfection of photodiode and CA. As is shown in Fig. 16, a single-tap DFE is incorporated through dual tunable g_{mf} feedback paths. The slow rolloff of input current may induce a residual charge (Q_R) to the succeeding integrating voltage. By adjusting g_{mf} to generate the compensation current (i_{DFE}) and charge ($-Q_R$) through sampling capacitor (C_S), the postcursor ISI of input current ($A_i \times i_{PD}$) can be eliminated. Fig. 17(a) and (b), respectively, illustrates the simulated eye diagrams without and with equalization. With a photodiode bandwidth of 9 GHz and a photocurrent

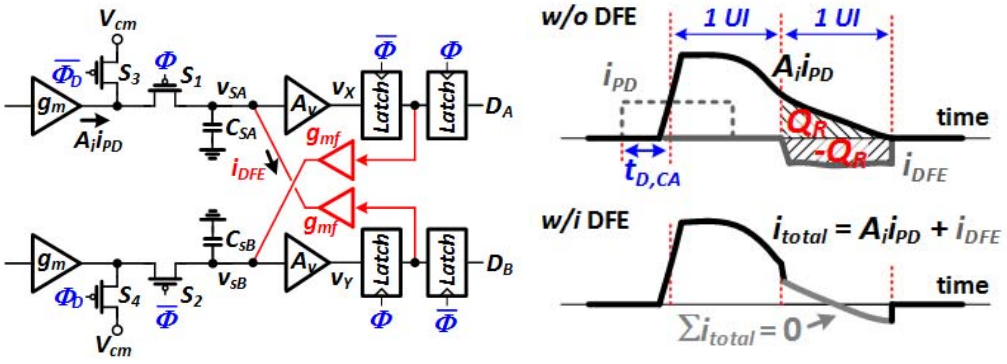

Fig. 16. DFE-IIR equalization.

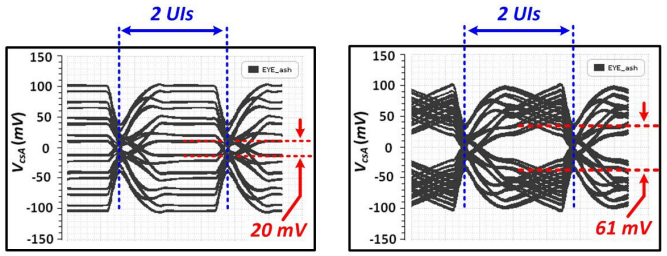

Fig. 17. Simulated eye diagrams of integrating voltage at 25 Gb/s data rate operation. (a) Without DFE-IIR. (b) With DFE-IIR.

of 25 μA_{pp}, the simulated eye height is 20 mV_{pp} before equalization, and can be improved to 60 mV_{pp} by enabling the single-tap DFE. Thus, the input sensitivity would lead to 3× (or 4.8 dB in power) improvement. By measurement results, the *SNR* improvement is less than the expected value due to the following reasons. First, a single-pole photodiode model is utilized in the simulation, which may overlook the slow response time of a real photodiode. Thus, the effect of equalization using a single-tap DFE becomes less pronounced. Second, the DFE is enabled at the sensitivity level, which may contribute additional thermal noise to the summer node and somewhat degrade its input sensitivity.

V. Experimental Results

To demonstrate the operating principles, a 25 Gb/s optical receiver is implemented in a 40 nm bulk-CMOS process. Fig. 18 shows the chip micrograph and photodetector assembly. The chip is operated under a 1.2 V power supply, and the core area is only 0.007 mm^2. Two photodiodes with different bandwidths (a 17 GHz photodiode from Albis and a 9 GHz photodiode from TrueLight) are integrated with the proposed receiver through bonding wire for optical test. The light source with a 6 dB extinction ratio is generated from an 850 nm 30 GHz bandwidth VCSEL. The optical power can be varied by a digital optical attenuator, and then coupled to the photodiode through optical lens probe. OM3-MMFs of 2 m are utilized for interconnection. As the extra power loss due to the limited aperture size is 1.5 dB (about 70%), the receiver's input sensitivity can be even better than the following reported data by circumventing the imperfect optical coupling. The input sensitivity measurements are taken by applying a $2^{15} - 1$ PRBS test pattern operating at 25 Gb/s.

Fig. 19 shows the measured input sensitivity of the receiver. Fig. 20 shows the bathtub curves measured at OMA of −6 dBm. Integrated with a 17 GHz photodiode, the input sensitivity is −10.8 dBm for a BER of less than 10^{-12} without turning on the DFE. The timing margin is about ±0.3 *UI*. Replaced by a 9 GHz photodiode, the input sensitivity becomes −7.2 dBm at 25 Gb/s operation without resorting to DFE compensation, and the timing margin is about ±0.12 *UI*. It can be recovered to −9.7 dBm by enabling the on-chip DFE, and the timing margin is extended to about ± 0.25 *UI*. The power breakdown of this receiver at 25 Gb/s is shown in Fig. 21, where the CA, comparators, and clock distribution network, respectively, dissipate about 30%, 30%, and 40% of total power. In the experimental prototype, the sampling clock is applied externally. The total power dissipations with and without clock buffers and distribution networks are 39.6 and 27.6 mW, respectively. At the input sensitivity level, the measured eye diagrams at dual channel output are shown in Fig. 22. The data jitter is about 3.4 ps_{rms}.

Table I shows the performance benchmark with the prior art. By de-embedding the photodiode responsivity, the proposed receiver improves the input sensitivity in terms of photocurrent by 3×–5× compared with the previous integrating-type receivers [4], [12]. On the other hand, it manifests 1/45 smaller chip area compared with the conventional voltage-mode (TIA + LA) architectures [1], [2]. As the area of analog circuits does not scale as aggressively as their digital counterparts when using more advanced process, it is expected that the area saving can be even more significant by using a digitally intensive design. This paper also manifests the best input sensitivity reported to date. Considering input sensitivity, parasitic C_{PD}, and energy efficiency, it provides figure of merits of 10.6 (for FoM_1) and 0.6 (for FoM_2).

VI. Conclusion

This paper describes a 25 Gb/s high input sensitivity photodiode bandwidth-tolerant (from 9 to 17 GHz) CMOS optical receiver. By incorporating a low-noise CA with a dual-path time-interleaved current integrator, it demonstrates an input sensitivity of −10.8 dBm and an energy efficiency of 1.13 pJ/b at 25 Gb/s operation. The CA bandwidth is optimized to about

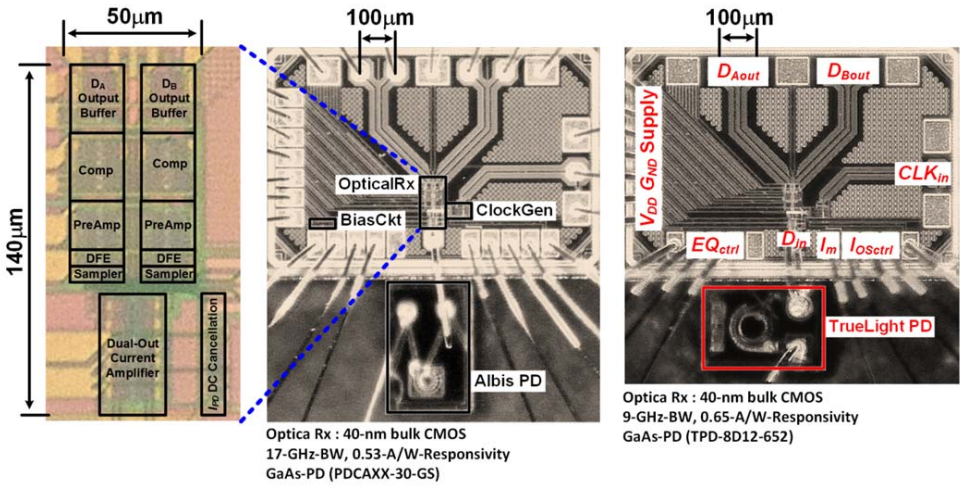

Fig. 18. Micrograph of chip and photodetector assembly.

TABLE I
PERFORMANCE BENCHMARK

Specification	[4]	[12]	[14]	[2]	[18]	This Work
Architecture	S/H + CMP	S/H + CMP	TIA + LA	TIA + LA	LBTIA + LA	CA + CMP
Data Rate	16 Gb/s	24 Gb/s	28 Gb/s	28 Gb/s	25 Gb/s	25 Gb/s
Data Type	8B/10B	PRBS15	PRBS9	PRBS7	PRBS15	PRBS15
Optical Sensitivity P_{AVG}	-5.4 dBm	-4.7 dBm	-7.8 dBm	N/A	N/A	-10.8 dBm
Optical Sensitivity OMA	569 μW_{PP}	570 μW_{PP}	151 μW_{PP}	200 μW_{PP}+	32 μW_{PP}++	100 μW_{PP}
Optical Sensitivity μA_{PP}	284 μA_{PP}	160 μA_{PP}+	121 μA_{PP}	80 μA_{PP}+	25 μA_{PP}+	53 μA_{PP}
PD capacitance	440 fF	> 200 fF	N/A	100 fF	> 25 fF	100 fF
Energy Efficiency	1.44 pJ/bit	0.4 pJ/bit	3.25 pJ/bit	1.03 pJ/bit	0.17 pJ/bit	1.13 pJ/bit
Chip Area (Rx)	0.025 mm^2	0.003 mm^2	0.32 mm^2	0.318 mm^2	0.0018 mm^2	0.007 mm^2
CMOS Process	90-nm	65-nm	65-nm	28-nm	28-nm	40-nm
FoM_1*	71	32.7	22.9	15.1	5	10.6
FoM_2**	0.93	0.32	N/A	8.2	0.17	0.6

* : $FOM_1 = \frac{i_{sensitivity}[\mu A_{PP}]}{\sqrt{D_R[Gb/s]}}$ from [14] ** : $FOM_2 = \frac{Power\,[mW] \cdot i_{sensitivity}[\mu A_{PP}]}{D_R[Gb/s] \cdot C_{PD}[fF]}$

+ : electrical (or emulated PD) test

++ : coupling loss of 6 dB is considered

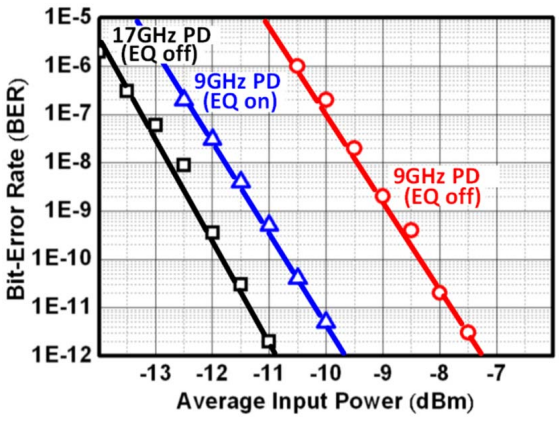

Fig. 19. Measured input sensitivity at 25 Gb/s.

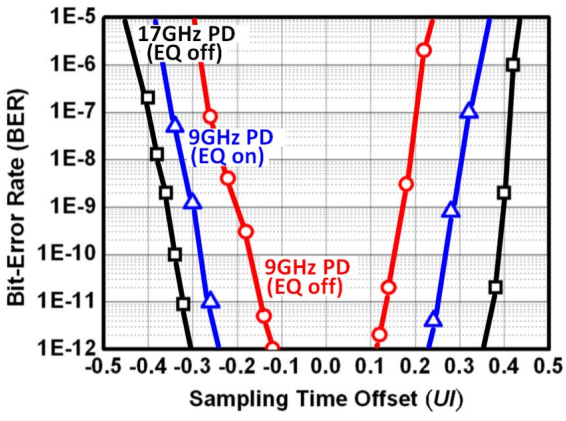

Fig. 20. Measured bathtub curves at 25 Gb/s and −6 dBm average power.

0.35× data rate for the maximum integrating voltage. A single-tap DFE is also embedded to improve the sampling timing margin. The receiver demonstrates over 5 dB improvement in input sensitivity compared with the prior art, and the chip area is only 2% that of conventional TIA + LA-based architectures. It shows strong potential for high-density and short-reach optical interconnects.

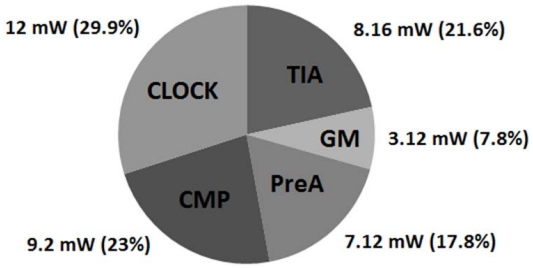

Fig. 21. Power breakdown at 25 Gb/s.

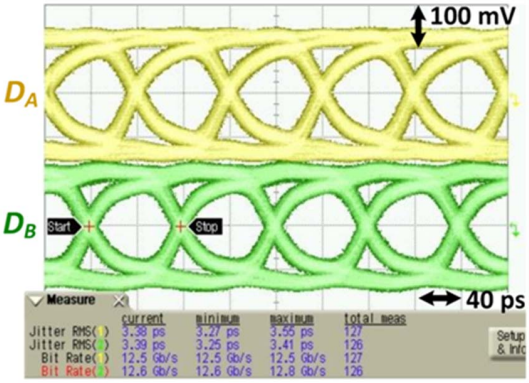

Fig. 22. Measured 1:2 demultiplexer output at 25 Gb/s.

ACKNOWLEDGMENT

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