A 43-mW MASH 2-2 CT ΣΔ Modulator Attaining 74.4/75.8/76.8 dB of SNDR/SNR/DR and 50 MHz of BW in 40-nm CMOS

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***Abstract*— This paper proposes a multistage noise-shaping continuous-time sigma-delta modulator (CTΣΔM) with on-chip *RC* time constant calibration circuits, multiple feedforward interstage paths, and a fully integrated noise-cancellation filter (NCF). The core modulator architecture is a cascade of two single-loop second-order CTΣΔM stages, each of which consists of an integrator-based active-*RC* loop filter, current-steering feedback digital-to-analog converters, and a 4-b flash quantizer. On-chip *RC* time constant calibration circuits and high-gain multistage operational amplifiers are realized to mitigate quantization noise leakage due to process variation. Multiple feedforward interstage paths are introduced to: 1) synthesize a fourth-order noise transfer function with dc zeros; 2) simplify the design of NCF; and 3) reduce signal swings at the second-stage integrator outputs. Fully integrated in 40-nm CMOS, the prototype chip achieves 74.4 dB of signal-to-noise-and-distortion ratio (SNDR), 75.8 dB of signal-to-noise ratio, and 76.8 dB of dynamic range in 50.3 MHz of bandwidth (BW) at 1 GHz of sampling frequency with 43 mW of power consumption (P) from 1.1/1.15/2.5-V power supplies. It does not require external software calibration and possesses minimal out-of-band signal transfer function peaking. The figure-of-merit (FOM), defined as $\mathrm{FOM} = \mathrm{SNDR} + 10 \times \log_{10}(\mathrm{BW}/\mathrm{P})$, is 165.1 dB.**

***Index Terms*— Active filters, analog–digital conversion, calibration, CMOS integrated circuits, delta-sigma modulation, noise cancellation, operational amplifiers, sigma-delta modulation.**

I. Introduction

ANALOG-TO-DIGITAL converters (ADCs) in a long-term-evolution advanced (LTE-A) direct conversion receiver need at least 50 MHz of bandwidth (BW) for the receiver to obtain 100 MHz of RF BW with minimum analog baseband complexity [1]. In this wireless application, a continuous-time sigma-delta modulator (CTΣΔM) is the ADC architecture of choice to meet the stringent specifications of high resolution, wide BW, and low power consumption. In addition, it possesses an inherent alias rejection and tolerance for out-of-band blockers, which are unique features beneficial for this application.

As an alternative to the wide BW single-loop CTΣΔM architecture [2]–[14], the multistage noise-shaping (MASH) CTΣΔM architecture [1], [15]–[22] has recently gained popularity due to its wide BW capability [21], low power potential [22], and capacity for integration in an LTE-A base-station transceiver [1]. Nevertheless, the single-loop CTΣΔM architecture is usually preferred over the MASH CTΣΔM architecture due to the problems of quantization noise leakage and nonideal interstage interfacing.

The problem of quantization noise leakage is more severe in MASH CTΣΔM compared to that in its discrete time counterpart, requiring calibration [15]–[17], [21]. Digital correction of the modulator output [15], [21], can be too power hungry to implement at high sampling frequency (f_s). Since analog *RC* time constant calibration is already a requirement for modulator stability over process corners, it can be implemented with sufficient accuracy to also satisfy the quantization noise leakage specification [16], [17]. However, the digital calibration algorithm in [15], [16], and [21] is complex, whereas that in [17] consumes a large amount of power consumption.

Accurate analog *RC* time constant calibration can be avoided for the MASH 0-X [19] and the sturdy MASH (SMASH) [20], [23] architectures. However, these architectures suffer from systematic first-stage quantization noise leakage [19], [23]. In addition, the SMASH architecture is more prone to overload compared with the MASH architecture, as it is essentially a single-loop architecture in disguise employing a MASH 0-X quantizer.

In addition to the problem of quantization noise leakage, interstage connection in MASH CTΣΔM is not as straightforward as that in its discrete time counterpart. Shown in Fig. 1, delay in the interstage digital-to-analog converter (DAC) causes out-of-band peaking for both the input signal and the first-stage quantization noise, which are processed in the second stage. This situation is exacerbated if the second stage

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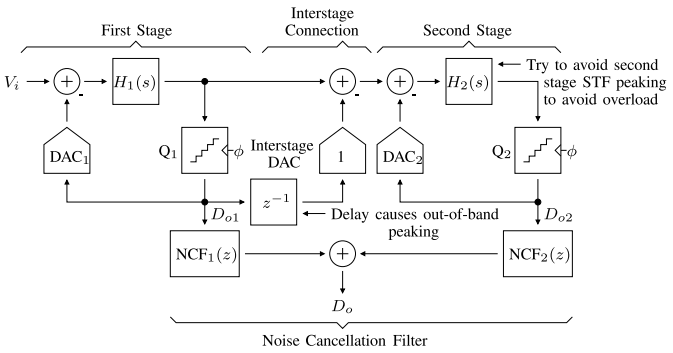


Fig. 1. Two-stage MASH CTΣΔM architecture with one clock cycle delay interstage DAC.

has out-of-band peaking in its signal transfer function (STF). In most cases, using a multibit quantizer in the first stage is necessary, as the second stage is already prone to overload from the first-stage quantization noise alone.

Due to this nonideal interstage connection, early MASH CTΣΔM designs [15]–[17] require a complex and power hungry noise cancellation filter (NCF) for equalization. An external coaxial cable [19], a low-pass filter [20], and a lattice filter [21] have been earlier proposed as an analog delay element in the interstage connection of MASH CTΣΔM. The effectiveness of these solutions to suppress out-of-band STF peaking still need improvement.

The MASH 2-2 CTΣΔM proposed in this paper solves all the aforementioned problems. Quantization noise leakage is minimized by on-chip *RC* time constant calibration, which is possible due to the low oversampling ratio (OSR), as well as employing high-gain multistage operational amplifiers (OAs) in the loop filters. In [24], it is shown that it is theoretically possible to synthesize MASH CTΣΔM from its discrete time counterpart prototype using feedforward interstage paths. The synthesis method proposed in this paper reduces the number of feedforward interstage paths necessary accounting for excess loop delay (ELD) while presenting minimal loading to the second stage and reducing its signal swing without out-of-band peaking. The NCF integrated in this design is also simple, low power, and capable of high-speed operation. To increase the suitability of this design for wireless applications, the modulator adopts feedback topology to provide STFs free from out-of-band peaking at the digital and integrator outputs.

This paper is organized as follows. Section II discusses the architecture of the proposed MASH 2-2 CTΣΔM. Section III describes critical circuits for the modulator operation. Section IV reports the measurement results. Section V provides the conclusion and comparison with the state of the art.

II. Architecture

Figs. 2–4 show the proposed MASH 2-2 CTΣΔM architecture block diagram, simplified model, and schematic, respectively. The modulator core consists of two single-loop CTΣΔM stages and an NCF. Each stage comprises two integrators, DACs, and a quantizer. Bias and *RC* time constant calibration circuits provide support for each stage.

TABLE I
IMPULSE-INVARIANT TRANSFORM ANALYSIS OF THE SINGLE-LOOP CTΣΔM STAGES

DAC	z	$H(s)$	$H(z)$
DAC$_1$	z^{-2}	$\frac{1}{s^2T_s^2}$	$\frac{1}{2}\frac{z^{-3}+z^{-4}}{(1-z^{-1})^2}$
DAC$_2$	z^{-2}	$\frac{1}{2}\frac{1}{sT_s}$	$\frac{1}{2}\frac{z^{-3}}{1-z^{-1}}$
DAC$_3$	z^{-1}	$-\frac{1}{sT_s}$	$-\frac{z^{-2}}{1-z^{-1}}$
DAC$_4$	$z^{-1/2}$	$\frac{4}{sT_s}$	$\frac{2(z^{-1}+z^{-2})}{1-z^{-1}}$
$H_1(z)$ (Total)			$\frac{2z^{-1}-z^{-2}}{(1-z^{-1})^2}$
NTF$_1(z) = \frac{1}{1+H_1(z)}$			$(1-z^{-1})^2$

DAC	z	$H(s)$	$H(z)$
DAC$_6$	z^{-1}	$\frac{1}{s^2T_s^2}$	$\frac{1}{2}\frac{z^{-2}+z^{-3}}{(1-z^{-1})^2}$
DAC$_8$	z^{-1}	$-\frac{3}{2}\frac{1}{sT_s}$	$-\frac{3}{2}\frac{z^{-2}}{1-z^{-1}}$
DAC$_9$	$z^{-1/2}$	$\frac{4}{sT_s}$	$\frac{2(z^{-1}+z^{-2})}{1-z^{-1}}$
$H_2(z)$ (Total)			$\frac{2z^{-1}-z^{-2}}{(1-z^{-1})^2}$
NTF$_2(z) = \frac{1}{1+H_2(z)}$			$(1-z^{-1})^2$

A. Proposed Single-Loop CTΣΔM Stage Architecture

Both stages implement a second-order noise transfer function (NTF) with dc zeros as demonstrated by the impulse invariant analysis shown in Table I. Feedback topology is adopted to avoid out-of-band peaking of the input signal for the first stage and amplification of the first-stage quantization noise for the second stage. The loop filters are realized using active-*RC* topology with digitally tunable capacitors. High-gain multistage OAs are implemented to satisfy both the loop filter linearity and the quantization noise leakage specifications.

DAC$_4$ and DAC$_3$ provide the half and one clock cycle delay feedback paths in the first stage, respectively. This ELD compensation scheme provides better power efficiency compared with using the zeroth-order feedback path [25]–[27] and lower quantizer complexity compared with using digital ELD compensation [28]. It resembles the ELD compensation scheme based on differentiator DAC [29], in which one of the differentiator DAC (DAC$_3$) coefficients is reduced by four times to save the area and power consumption thanks to the feedback topology. Furthermore, the delay of DAC$_1$ is extended to two clock cycles to accommodate data weighted averaging (DWA) [30] and thermometer-to-binary encoder based on Wallace-tree adder to minimize the quantizer metastability. The change in the loop filter impulse response caused by this additional delay is compensated by adding DAC$_2$ and reducing the first integrator coefficient by 40%.

DAC$_9$ and DAC$_8$ fulfill the same roles as DAC$_4$ and DAC$_3$ in the second stage, respectively. As second-order noise-shaping for error in DAC$_6$ is sufficient, a one clock cycle delay is used for DAC$_6$ as DWA is not necessary. All the

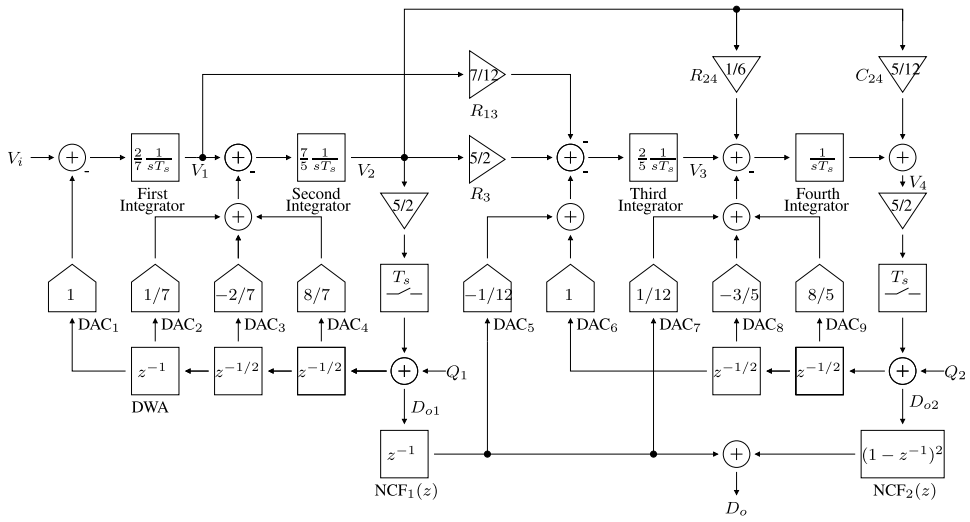


Fig. 2. Block diagram of proposed MASH 2-2 CTΣΔM architecture.

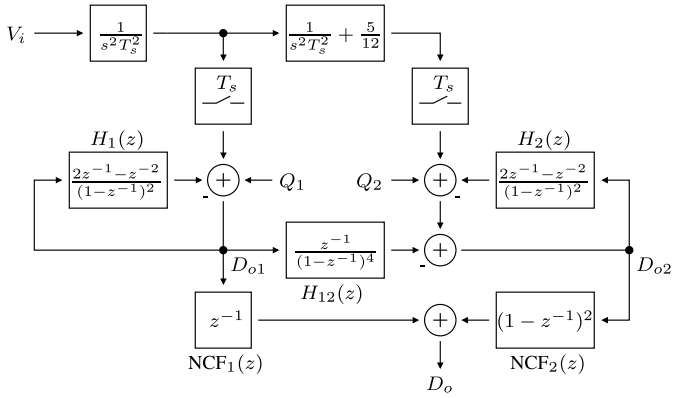


Fig. 3. Simplified model of proposed MASH 2-2 CTΣΔM.

DACs use nonreturn-to-zero pulse shaping to reduce jitter sensitivity. DAC bias currents track the value of replica loop filter resistors.

Two 4-b flash quantizers provide an amplification factor of 2.5 V/V to reduce the signal swing and BW of the second and fourth integrators by the same amount. This is achieved by reducing the full scale of the quantizers with respect to that of the modulator [31].

B. Proposed MASH CTΣΔM Architecture

In addition to the main interstage path through R_3, five additional feedforward interstage paths are added through R_{13}, R_{24}, C_{24}, DAC$_5$, and DAC$_7$. Four, five, or six feedforward interstage paths are necessary for a MASH 2-2 CTΣΔM with zero, one, or two clock cycle ELDs, respectively. Without all these additional paths, the second stage needs to process the input signal without any attenuation and the NCF needed to cancel the first-stage quantization noise is complex [17]. Although the in-band input signal processed by the second stage can be canceled using DAC$_5$ [15], [16], this leads to out-of-band peaking of the input signal and the first-stage quantization noise at the second-stage output. This out-of-band peaking can be solved by minimizing the DAC$_5$ delay or implementing an analog delay element in the main interstage path [19]–[21].

By removing the constraint on the second-stage STF compared with that in [24], this allows a search for the optimized feedforward interstage path's combination and reduces its number by one. The design options considered were: 1) four loop filter feedforward interstage paths, one of which is the unused resistive connection from the first-integrator output to the fourth-integrator input and 2) two interstage DACs from the first-stage output to the third- and fourth-integrator inputs with one, one and a half, or two clock cycle delays. All the topologies were then compared based on the second-stage STF and the value of the coefficients to minimize the second stage loading.

Using the impulse invariant transform analysis as exemplified in Table II and the simplified MASH 2-2 CTΣΔM model in Fig. 3, the feedforward interstage coefficients are chosen to satisfy

$$\text{NTF}(z) = (1-z^{-1})^4 \tag{1}$$

$$\text{NTF}_{12}(z) = -z^{-1} \tag{2}$$

where NTF(z) and NTF$_{12}(z)$ are the transfer functions from the first-stage quantization noise to the NCF and the second-stage outputs, respectively. As implied by (2), the NCF in this design is simple compared with those used in the state-of-the-art CMOS MASH CTΣΔMs [15]–[17], [21].

C. Noise Transfer Function

The theoretical quantization noise floors of the second- and fourth-order NTFs with dc zeros, 4-b quantizer, and OSR of 10 are −63.0 and −85.7 dBFS, respectively. The simulated maximum stable amplitude (MSA) is −0.6 dBFS.

D. Signal Transfer Function

Fig. 5 shows the theoretical and simulated STFs of the MASH 2-2 CTΣΔM at the digital and integrator outputs. The STF possesses a notch at 247 MHz generated from the

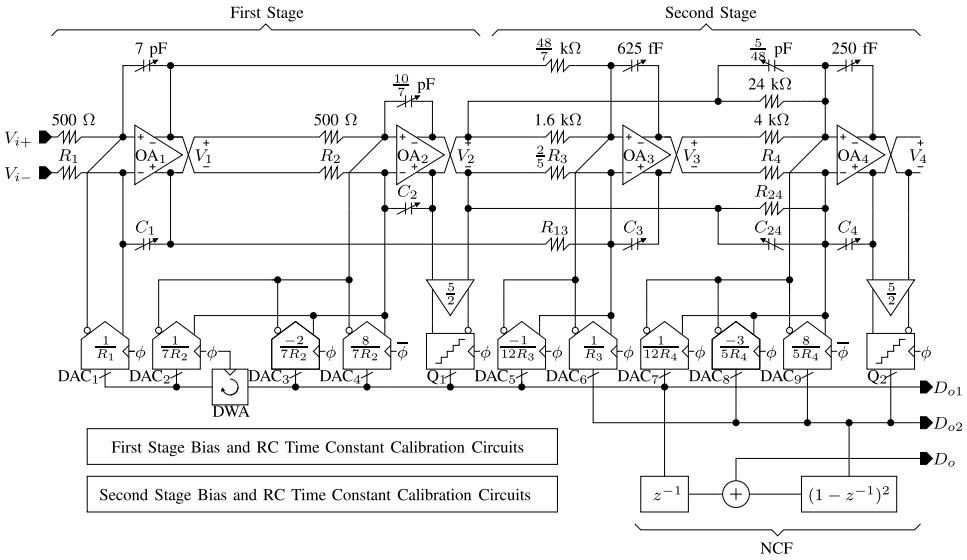


Fig. 4. Schematic of proposed MASH 2-2 CTΣΔM.

TABLE II
IMPULSE-INVARIANT TRANSFORM ANALYSIS OF THE FEEDFORWARD INTERSTAGE PATHS

DAC	z	$H(s)$	$H(z)$
DAC_1	z^{-2}	$\frac{1}{s^4T_s^4}+\frac{5}{12}\frac{1}{s^2T_s^2}$	$\frac{1}{4}\frac{z^{-3}+z^{-4}+z^{-5}+z^{-6}}{(1-z^{-1})^4}$
DAC_2	z^{-2}	$\frac{1}{2}\frac{1}{s^3T_s^3}+\frac{1}{12}\frac{1}{s^2T_s^2}+\frac{5}{24}\frac{1}{sT_s}$	$\frac{1}{12}\frac{4z^{-3}-z^{-4}+3z^{-5}}{(1-z^{-1})^3}$
DAC_3	z^{-1}	$-\frac{1}{s^3T_s^3}-\frac{1}{6}\frac{1}{s^2T_s^2}-\frac{10}{24}\frac{1}{sT_s}$	$-\frac{1}{6}\frac{4z^{-2}-z^{-3}+3z^{-4}}{(1-z^{-1})^3}$
DAC_4	$z^{-1/2}$	$\frac{4}{s^3T_s^3}+\frac{2}{3}\frac{1}{s^2T_s^2}+\frac{5}{3}\frac{1}{sT_s}$	$\frac{1}{6}\frac{6z^{-1}+9z^{-2}+4z^{-3}+5z^{-4}}{(1-z^{-1})^3}$
DAC_5	z^{-1}	$-\frac{1}{12}\frac{1}{s^2T_s^2}$	$-\frac{1}{24}\frac{z^{-2}+z^{-3}}{(1-z^{-1})^2}$
DAC_7	z^{-1}	$\frac{5}{24}\frac{1}{sT_s}$	$\frac{5}{24}\frac{z^{-2}}{1-z^{-1}}$
$H_{12}(z)$ (Total)			$\frac{z^{-1}}{(1-z^{-1})^4}$
$\text{NTF}_{12}(z)=-H_{12}(z)\text{NTF}_1(z)\text{NTF}_2(z)$			$-z^{-1}$

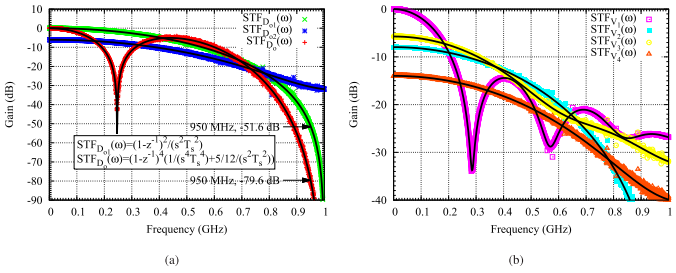


Fig. 5. Theoretical (black line) and simulated STFs of the MASH 2-2 CTΣΔM at the (a) digital and (b) integrator outputs.

second-order feedforward interstage path through C_{24} and cancellation of the third-order feedforward interstage paths through R_{13} and R_{24}. The in-band input signal swings at first through the fourth integrator outputs are 0, −7.96, −5.74, and −14.0 dB, respectively. This design is free from internal out-of-band peaking. The in-band second-stage STF is −6.02 dB.

Note that it is not possible to synthesize a MASH CTΣΔM where the later stage does not process any input signal in-band and out-of-band. This implies that the STF of the MASH CTΣΔM is that of the first stage. Thus, the later stage is unable to cancel the alias generated by the first stage. This violates the assumption of quantization noise cancellation condition, as alias is virtually indistinguishable from quantization noise.

To control the signal swing at the second stage output, feedforward input paths [11], [28] are recommended instead of additional feedforward interstage paths [24]. This directly controls the overall STF that can be more intuitively derived [32]. The second-stage STF is given as

$$\text{STF}_2(j\omega)=\frac{\text{STF}(j\omega)-\text{STF}_1(j\omega)\text{NCF}_1(j\omega)}{\text{NCF}_2(j\omega)} \tag{3}$$

which implies that the second-stage STF is indirectly controlled by the overall STF if the first-stage STF and the NCF transfer functions are fixed.

As an example, a feedforward resistive path from the modulator input to the third-integrator input can be used

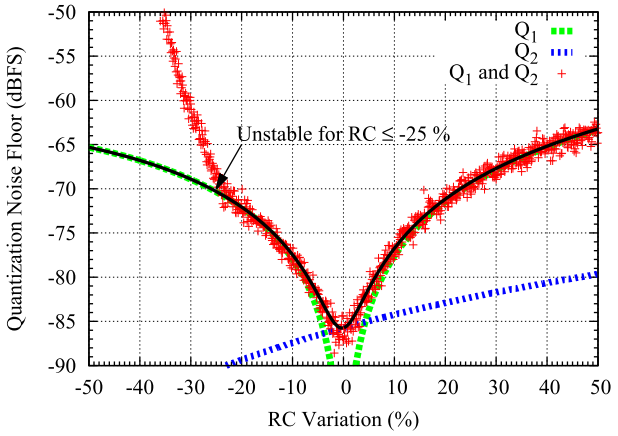


Fig. 6. Theoretical (black line) and simulated quantization noise floor of the MASH 2-2 CTΣΔM versus *RC* time constant variation.

to cancel the second-order feedforward path through C_{24}. In this case, the in-band input signal swings at the third-integrator output and the second-stage output are −20.0 and −21.6 dB, respectively. Thus, it allows room for interstage gain to further reduce quantization noise contribution of the second stage. Without any integrator rescaling, this gain is limited to 2 V/V as the out-of-band input signal swing at the third-integrator output is similar to that in the current design. As the current design allocates some quantization noise leakage budget as a conservative measure, this modification is deemed not necessary. It can be attractive for future designs with more accurate *RC* time constant calibration.

E. Process Variation

The impact of process variation was determined by analyzing the global and local sensitivities of each component or parameter to the quantization noise floor of the modulator. Fig. 6 shows the theoretical and simulated quantization noise floor of the MASH 2-2 CTΣΔM versus *RC* time constant variation with the ideal OA model. In this example, up to ±3% *RC* time constant variation can be tolerated for less than −83.5 dBFS of quantization noise budget. Calibration is necessary since the worst case variation on the values of R and C is ±20% based on technology specifications.

Analyses were done for both global and local variations of R, C, DAC coefficient, DAC delay, quantizer sampling instance, and quantizer gain. Besides *RC* time constant variation, DAC coefficient variation is also a contributor to quantization noise leakage and minimized by proper biasing. The quantization noise floor of the design is not sensitive to DAC delay, quantizer sampling instance, quantizer gain, and feedforward interstage path coefficient variations.

F. Circuit Thermal Noise

The full scale of the modulator corresponds to a differential sinusoid input signal with an amplitude of 687.5 mV (peak-to-peak of 1.375 V) or 0 dBFS. The noise contributions from R_1, OA_1, and DAC_1 are calculated to be −84.7, −86.3, and −86.2 dBFS, respectively, which bring the noise floor up to −80.9 dBFS for the first integrator. The suppressions for

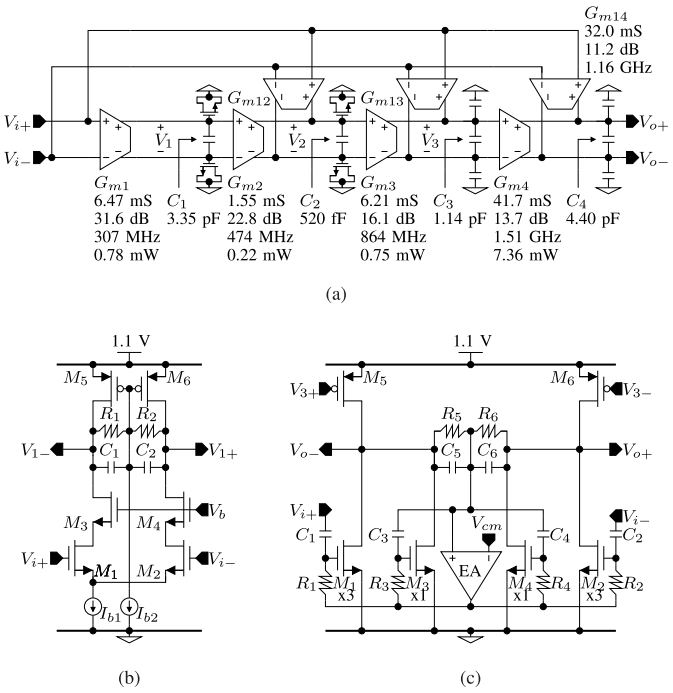


Fig. 7. (a) OA architecture and its design parameters for OA_1. (b) Schematic of G_{m1}. (c) Schematic of G_{m4} and G_{m14} used in OA_1.

the input-referred thermal noise of the first through fourth integrators were calculated to be 0.2, 4.2, 19.3, and 30.8 dB, respectively. Both the integrators in each stage are chosen to be scaled equally, whereas the integrators in the second stage are scaled to be eight times smaller compared with those in the first stage. The total noise floor of the modulator is −79.1 dBFS.

G. Clock Jitter

The prototype chip relies on the performance of an external clock source to achieve the required clock jitter budget. Using the analysis in [33], the theoretical noise floors due to white clock jitter mixing with quantization noise and a worst case sinusoid input signal with −1 dBFS of amplitude at band edge are found to be −83.0 and −81.0 dBFS, respectively, for 1-ps rms of white jitter in DAC_1. If the clock jitter is dominated by its near-carrier component with a very narrow BW compared with that of the modulator, the worst case theoretical noise floor becomes −71.0 dBFS for 1-ps rms of low-frequency sinusoid jitter approximation in DAC_1.

III. Circuit Implementation

A. Operational Amplifier

Fig. 7(a) shows the OA architecture and its design parameters for OA_1. It has four gain stages compensated using the no-capacitor feedforward (NCFF) scheme [34], making high gain OA practical in deep submicrometer CMOS. The transconductors G_{m2} and G_{m12}, as well as G_{m3} and G_{m13}, are designed to be identical in order to balance the gain. Additional nMOS capacitors are added at the output terminals of the first and second stages to lower their BW. Their nonlinearity is not a concern due to the small signal swings

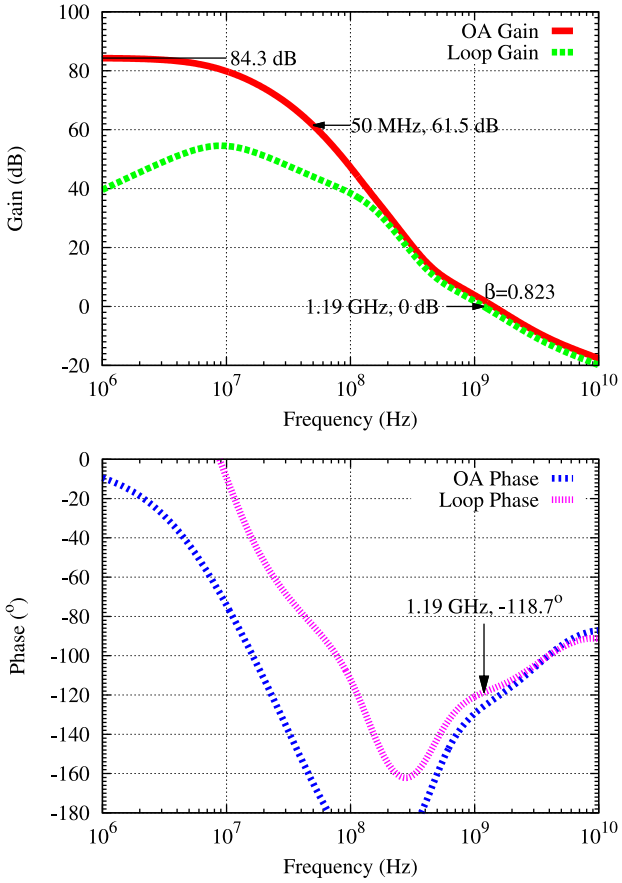


Fig. 8. Postlayout simulated OA_1's (a) gain and (b) phase.

they experience. The third stage directly drives the parasitic input capacitances of the output stage. The estimated load capacitance of the output stage annotated in Fig. 7(a) includes the parasitic capacitances of the digitally tunable capacitor, OA input capacitance, and DAC output capacitance, which effectively load the OA.

Fig. 7(b) shows the schematic of G_{m1}. It is a telescopic cascode amplifier with noncascoded load transistors, a self-biased common-mode feedback (CMFB), and a current source common-mode level shifter. Fig. 7(c) shows the schematic of G_{m4} and G_{m14} as the output stage. It is a current-reuse amplifier with an ac coupling for G_{m14} and a two-stage NCFF CMFB. Pseudo differential topology is chosen to accommodate the limited transistor headroom of 206 mV. As the signal swings at the second through fourth integrator outputs are reduced, and the pseudo differential output stage in OA_1 is replaced by its fully differential version for the rest of the OAs.

Fig. 8 shows the postlayout simulated OA_1 Bode plot. The loop gain is obtained by Cadence stb analysis when OA_1 is used in closed loop as the first integrator, whereas OA gain is obtained when OA_1 is used in open loop including the integrator feedback network as its load. The feedback factor, indirectly measured from the ratio of the loop and OA unity gain frequencies (UGFs), is 0.823 due to the capacitive division between the integrating capacitor and the parasitic capacitances at the OA virtual ground including that of DAC_1. OA_1 achieves 84.3 dB of dc gain, 61.5 dB of gain at a

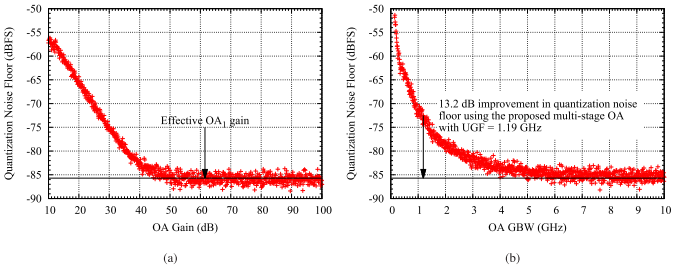


Fig. 9. Simulated quantization noise floor of the MASH 2-2 CTΣΔM versus (a) OA gain with infinite GBW and (b) OA GBW with infinite gain for a single-pole OA model.

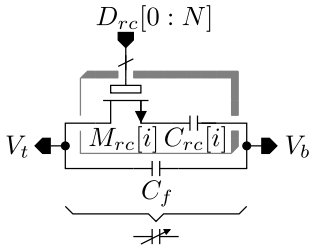


Fig. 10. Schematic of digitally tunable capacitor.

frequency of 50 MHz, 1.19 GHz of loop UGF, 61.3° of loop phase margin, and 3.4 nV/rtHz of input-referred voltage noise density. All the OAs achieve greater than 60 dB of gain at a frequency of 50 MHz, which is equivalent to greater than 50 GHz of gain-BW (GBW) product for OA with single-pole roll-off. The loop UGFs of OA_2, OA_3, and OA_4 are 1.20 GHz, 1.81 GHz, and 964 MHz, respectively. The simulated nominal power consumption of OA_1, OA_2, OA_3, and OA_4 are 10.8, 6.5, 3.6, and 3.5 mW, respectively. Due to the limited design time, OA_3 was overdesigned and its power consumption and loop UGF can potentially be reduced further.

The advantage of the proposed OA is apparent when evaluating the required OA specifications as shown in Fig. 9. Single-pole OAs with dc gain and GBW larger than 40 dB and 5 GHz, respectively, are needed to minimize the quantization noise leakage. This rules out the possibility of low gain OA [13]. Transient simulation of the modulator using the proposed OAs shows that the ideal quantization noise floor remains intact. On the other hand, using conventional OA with single-pole roll-off with the same UGF of 1.19 GHz as the proposed OA suffers from degradation in quantization noise floor by 13.2 dB. No GBW tuning or loop filter compensation is needed as the proposed OA performance meets the specifications for all the process corners.

B. Digitally Tunable Capacitor

Fig. 10 shows the digitally tunable capacitor schematic used in the loop filter and the *RC* time constant calibration circuit. It was designed to have 63.3% and 163.3% of the nominal capacitance value when the thick oxide switches M_{rc} are completely turned OFF and ON, respectively, to cover individual R and C variations of ±20%. The high threshold voltage of the thick oxide switches M_{rc} ensures that they are never turned ON when the floating nodes are at low voltages. The capacitors in the first and second stages are controlled by 98 and 120-level thermometer codes, respectively. The

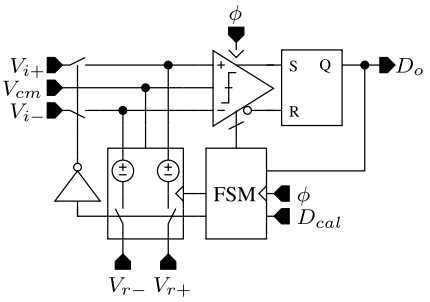


Fig. 11. Comparator schematic used in the 4-b flash quantizer.

quantization noise leakage budget of ±3% *RC* time constant variation tolerates up to two LSBs of error in the digital code.

C. Bias and RC Time Constant Calibration Circuits

The bias circuit in each stage provides bias currents inversely proportional to the value of the replica loop filter resistor to the DACs, OAs, and *RC* time constant calibration circuit. Error in DAC coefficient of less than 1% is achieved to minimize quantization noise leakage. During startup, the *RC* time constant calibration circuit in each stage measures the rise time of a ramp waveform generated by a replica integrator and DAC. The digitally tunable capacitor is tuned until the desired rise time of the ramp is achieved. The *RC* time constant variation over temperature is +0.15% and +0.64% at 125 °C and −40 °C, respectively, compared with the nominal *RC* time constant at 27 °C. Thanks to the low temperature coefficients of the nonsilicide p-type polysilicon resistor and the finger metal capacitor, startup calibration is sufficient.

D. Quantizer

Fig. 11 shows the comparator schematic used in the 4-b flash quantizer. During startup, the sense amplifier input terminals are connected to the resistive ladder via a switched-capacitor common-mode level shifter. The finite-state machine calibrates the sense amplifier offset to the differential reference voltage of the resistive ladder. During normal operation, the resistive ladder can be turned OFF. Fig. 12 shows the sense amplifier schematic used in the comparator. The classic topology in [35] is modified by adding a digitally controlled dynamic differential pair formed by transistors M_{6-10}. It generates dynamic offset current, which also contributes to the latch transconductance to offset the effect of additional parasitic capacitance that minimizes the degradation of the regeneration time constant.

Fig. 13(a) shows the postlayout simulated sense amplifier offset versus digital code for all the corners. The effect of nonlinearity on this curve is minimized by sweeping both the positive and negative digital codes during the calibration. The maximum sense amplifier offset is greater than the desired maximum differential reference voltage for all the corners to give some margin for random transistor mismatch. After calibration, the simulated integral and differential nonlinearities of the quantizer are less than a quarter of LSB. By modeling the comparator offset to be random with a standard deviation of a quarter of LSB, 1000-run Monte Carlo simulations as shown in Fig. 13(b) predict that the quantization noise floor

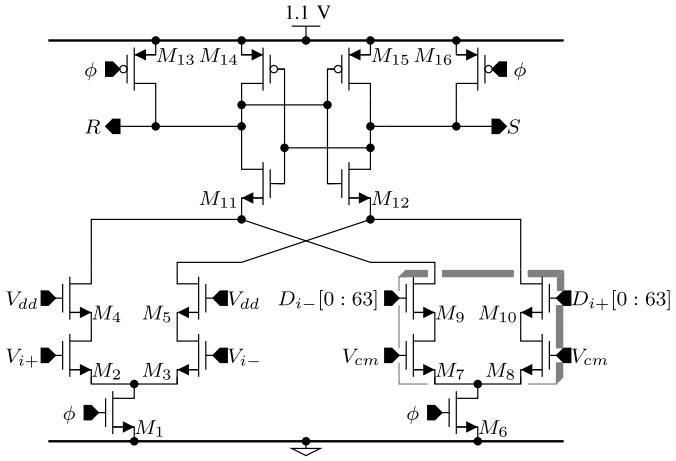


Fig. 12. Schematic of sense amplifier used in the comparator.

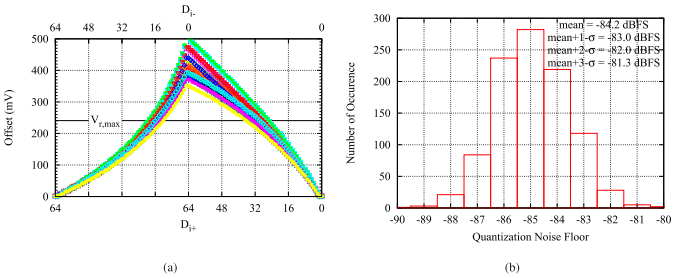


Fig. 13. (a) Postlayout simulated sense amplifier's offset versus digital code for all the corners. (b) 1000-run Monte Carlo simulations of quantization noise floor versus random comparator offset standard deviation of a quarter of LSB.

increases to −81.3 dBFS for the case where the quantization noise power is higher than its mean value by its 3-σ value.

The quantizer also includes a thermometer-to-binary encoder based on Wallace-tree adder and DWA. The simulated nominal digital power consumption of the quantizer is 2.5 mW.

E. DAC

Fig. 14(a) and (b) shows the pMOS and nMOS DAC cell schematics, respectively. Both consist of the current source transistor M_1, cascode transistor M_2, and current switch transistors $M_{3\text{-}4}$. The bias current carried in each DAC cell is given by $G_m V_{fs}/16$, where G_m is the DAC transconductance annotated in Fig. 4. External 10-μF ceramic capacitors are used to decouple the DAC bias voltages V_{b1} to reduce DAC noise floor from biasing by 7.5 dB during large signal condition.

The pMOS DAC cell uses a 2.5 V power supply and thick oxide current source transistor M_1, whose drain is biased at 1.1 V to provide low noise and good matching. It is used in DAC_1, DAC_4, DAC_6, and DAC_9. The rest of the DACs use the nMOS DAC cell. The common-mode DAC currents help to raise the OA input common-mode voltages and provide bias currents to the OA output stages and the circuit driving the modulator input terminals.

The standard deviation of DAC_1 cell current mismatch is slightly less than 0.05%. From 1000-run Monte Carlo simulations, this corresponds to averaged second- and third-order harmonic distortions of 84.8 and 88.6 dB, respectively.

TABLE III
COMPARISON WITH STATE-OF-THE-ART CTΣΔMS

	This Work	[14]	[21]	[13]	[12]	[11]	[20]	[9]	[8]	[19]	[4]	[3]	[2]
f_s (GHz)	**1.000**	6.000	6.000	2.880	1.200	2.400	1.800	1.280	2.184	3.200	4.000	3.600	4.000
BW (MHz)	**50.3**	60.0	350.0	160.0	50.0	40.0	50.0	50.0	80.0	53.3	150.0	36.0	125.0
DR (dB)	**76.8**	76.0	72.8	72.1	72.0	67.8	85.0	75.0	73.0	88.0	73.0	83.0	70.0
Peak SNR (dB)	**75.8**	68.8	66.8	68.1	71.7	N/A	76.8	71.0	70.0	83.1	71.0	76.4	65.5
Peak SNDR (dB)	**74.4**	67.6	64.8	65.3	71.5	66.9	74.9	64.0	67.5	71.4	N/A	70.9	65.0
Power Consumption (P) (mW)	**43.0**	13.3	756.0	40.0	54.0	5.25	80.4	38.0	23.0	235.0	750.0	15.0	260.0
Power Supplies (V)	**1.1**	1.4	-1.0	0.8	N/A	N/A	1.3	1.2	1.0	-1.0	-2.5	1.2	1.1
	1.15		1.0	1.4			1.5	1.5	1.2	0.9	1.0		1.8
	2.5		1.8	1.5					1.5	1.8	2.5		
FOM[a](dB)	**165.1**	164.1	151.5	161.3	161.2	161.8	162.8	155.2	162.9	154.9	N/A	164.7	151.8
FOM_S[b](dB)	**167.5**	172.5	159.5	168.1	161.7	162.7	172.9	166.2	168.4	171.5	156.0	176.8	156.8
FOM_W[c](fJ/step)	**99.8**	56.5	761.1	82.8	176.0	36.3	177.1	293.6	74.2	730.8	N/A	72.7	716.3
Area (mm^2)	**0.265**	0.070	1.400	0.155	0.500	0.019	0.337	0.490	0.100	0.900	5.500	0.120	0.880
Technology (nm)	**40**	65	28	16	65	40	28	65	20	28	65	90	45

[a] $\text{FOM} = \text{SNDR} + 10 \times \log_{10}\left(\frac{\text{BW}}{\text{P}}\right)$

[b] $\text{FOM}_S = \text{DR} + 10 \times \log_{10}\left(\frac{\text{BW}}{\text{P}}\right)$

[c] $\text{FOM}_W = \frac{\text{P}}{2 \times \text{BW} \times 2^{\frac{\text{SNDR} - 10 \times \log_{10}(1.5)}{20 \times \log_{10}(2)}}}$

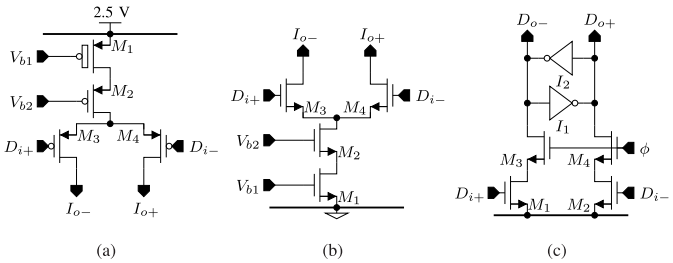


Fig. 14. (a) Schematic of pMOS DAC cell. (b) Schematic of nMOS DAC cell. (c) Schematic of DAC latch cell.

DWA is expected to improve harmonic distortion by 10.0 dB at band edge.

Fig. 14(c) shows the DAC latch cell schematic, which has low crossing switching. It is used to drive the pMOS DAC cell, whereas inverters are added to its outputs to drive the nMOS DAC cell for high crossing switching. These switching schemes, combined with ensuring fast transition times, minimize the effects of DAC glitch and intersymbol interference (ISI).

The simulated nominal analog power consumptions of the DACs in the first and second stages are 7.5 and 1.1 mW, respectively. The simulated nominal digital power consumptions of the DACs in the first and second stages are 3.2 and 1.7 mW, respectively.

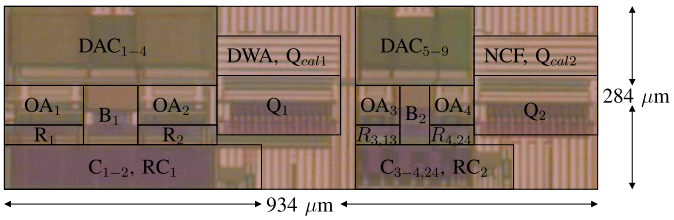


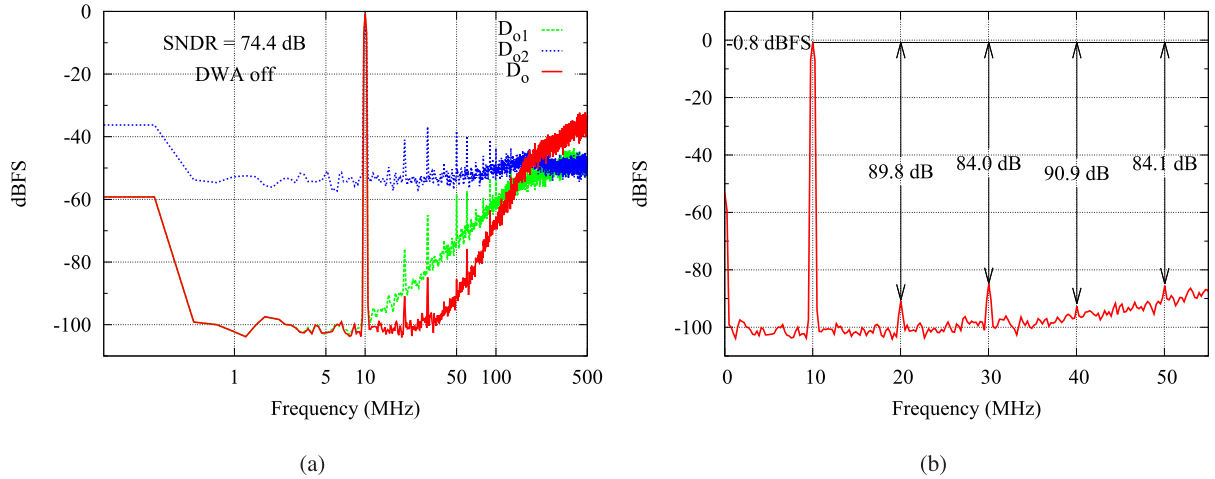
Fig. 15. Chip microphotograph.

F. Floorplan

The modulator is implemented in the TSMC 40-nm low-power CMOS process. Fig. 15 shows the chip microphotograph. The area occupied by the modulator is 0.265 mm^2. Passives of each stage are placed close to each other. Separate power supplies between the analog and digital blocks are used. Guard rings are used extensively to protect sensitive analog circuits. Unused areas are for power supply decoupling capacitors.

IV. MEASUREMENT RESULTS

Fig. 16 shows the measured fast Fourier transform (FFT) spectrums for a single-tone sinusoid input signal at a frequency of 10 MHz. The peak signal-to-noise-and-distortion ratio (SNDR), peak signal-to-noise ratio (SNR), and spurious-free dynamic range (SFDR) are 74.4, 75.8, and 84.0 dB, respectively, at an input amplitude of −0.8 dBFS. Noise and



(a) (b)

Fig. 16. Measured (a) full-band and (b) in-band FFT spectrums (average of 125 4096-point FFT) at peak SNDR condition for single-tone sinusoid input signal with 10 MHz of frequency.

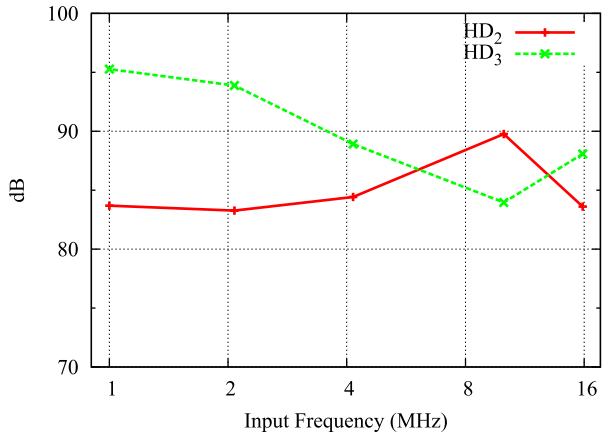


Fig. 17. Measured second- and third-order harmonic distortion versus single-tone sinusoid input signal frequency with an amplitude of −0.8 dBFS.

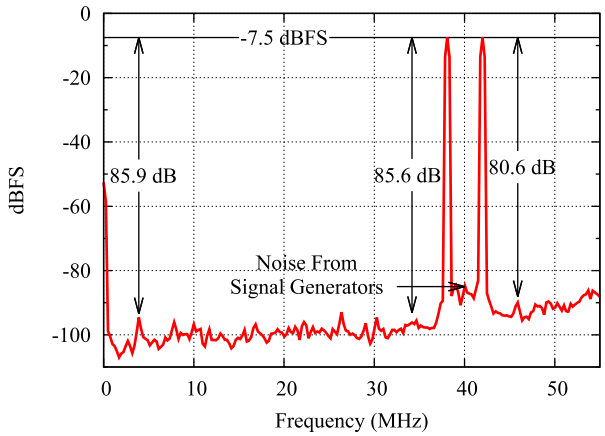


Fig. 18. Measured FFT spectrum (average of 125 4096-point FFT) at peak SNDR condition for two-tone sinusoid input signals with 38 and 42 MHz of frequencies.

distortion cancellation of 20.0 dB was observed. The harmonic components visible in the first stage output, which are canceled by the second stage, indicates that the first stage is very close to overload as the MSA is −0.7 dBFS. The BW of the modulator is 50.3 MHz to include the fifth-order harmonic component.

Fig. 17 shows the measured second- and third-order harmonic distortion versus single-tone sinusoid input signal frequency with an amplitude of −0.8 dBFS. The harmonic distortion is limited by intrinsic DAC matching and ISI as DWA was found to reduce the SFDR due to interaction between parasitic DAC capacitances and parasitic DAC routing resistances to the OA input terminals. All the measurements shown correspond to the case when DWA is turned OFF.

Fig. 18 shows the measured FFT spectrum for two-tone sinusoid input signals at frequencies of 38 and 42 MHz with −7.5 dBFS of amplitude, each of which corresponds to peak SNDR condition. The two-tone MSA is −6.5 dBFS. These input signals located near the edge of the modulator BW represent the worst case two-tone linearity test due to reduced gain at high frequencies. The second- and third-order intermodulations are 85.9 and 80.6 dB, respectively. Residual noise from the signal generators, which was filtered by an external bandpass filter with 4 MHz of BW, was observed from the 38 to the 42-MHz band.

Fig. 19 shows the measured SNDR and SNR versus single-tone sinusoid input signal amplitude at a frequency of 10 MHz. The dynamic range (DR), defined as the ratio between the maximum and minimum input signal amplitudes where SNDR $>$ 0 dB, is 76.8 dB. The modulator always recovered from overload and startup conditions without the need for reset mechanisms.

Fig. 20 shows the measured noise floor versus digital code controlling the first-stage digitally tunable capacitors. The digital codes obtained by startup *RC* time constant calibration were found to be close to optimum for both the first and second stages. Compared with the nominal digital codes, the digital codes after calibration differ by +2 and −1 LSBs for the first and second stages, respectively. Meanwhile, the measured value of input resistors R_1 in this test chip is 475 Ω, which is about 5% less than its nominal value.

Fig. 21 shows the measured STF. The STF in-band is flat with less than 0.1 dB of variation. The STF peaking is 4.1 dB at a frequency of 320 MHz. The alias suppression is 52.4 dB at a frequency of 950 MHz. The STF peaking, degraded alias suppression, and shallow STF notch are attributed to poor matching at high frequency due to finite OA gain and BW, finite switch ON-resistance, and component mismatch. These

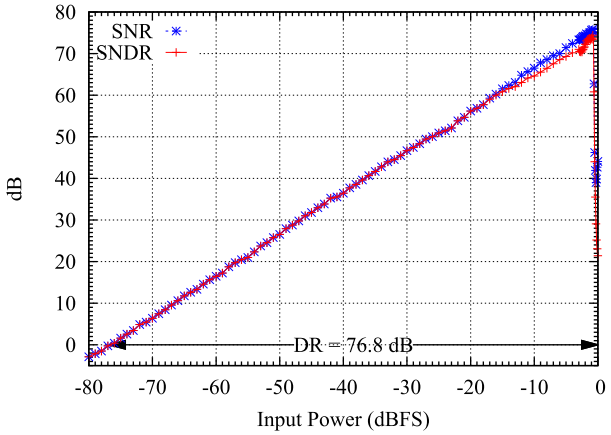


Fig. 19. Measured SNDR versus single-tone sinusoid input signal amplitude with 10 MHz of frequency.

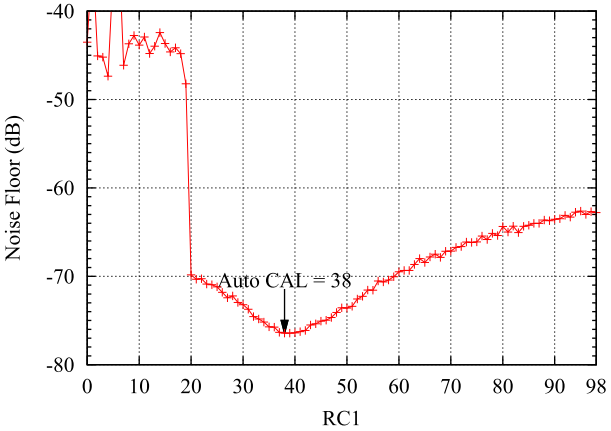


Fig. 20. Measured noise floor versus digital code controlling the first stage's digitally tunable capacitors.

degradations were also observed by transient simulations of the modulator at the critical frequencies. Nevertheless, the increased DR required by the STF peaking is safely accommodated by the NCF and the only peaking worth considering is the 2.1 dB of the first-stage STF peaking at a frequency of 170 MHz. The reduction of input signal swing at the second-stage output is degraded to 3.4 dB compared with the theoretical value of 6.0 dB due to quantizer gain error attributed to the switched-capacitor common-mode level shifter during quantizer calibration.

Fig. 22 shows the measured power consumption breakdown. The power consumption is 43 mW composed of 30.6 and 12.4 mW of analog and digital power consumption, respectively.

V. Conclusion

This paper demonstrates a fully integrated MASH 2-2 CTΣΔM possessing minimal STF out-of-band peaking without any external digital postprocessing or calibration. These features are enabled by the proposed combination of feedforward interstage paths, high-gain multistage OA, and startup *RC* calibration. The prototype chip fabricated in 40-nm CMOS achieves 74.4 dB of SNDR, 75.8 dB of SNR, and 76.8 dB of DR in 50.3 MHz of BW with a power consumption (P) of 43.0 mW. The figure-of-merit (FOM), defined as FOM $=$ SNDR $+ 10 \times \log_{10}$(BW/P), is 165.1 dB which

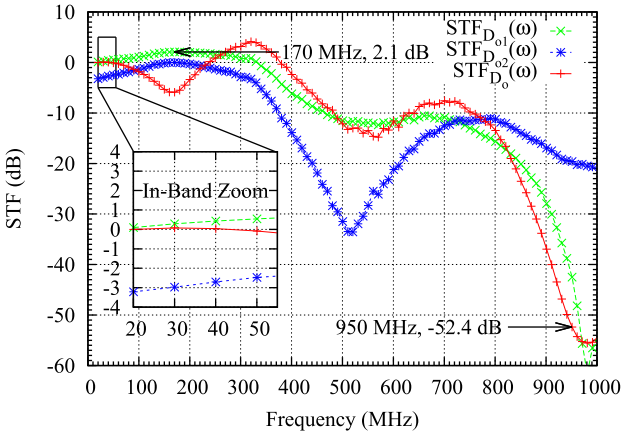


Fig. 21. Measured STF.

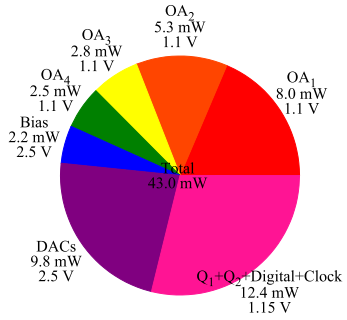


Fig. 22. Measured power consumption breakdown.

is competitive compared with the state-of-the-art CTΣΔMs shown in Table III.

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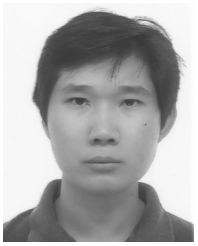

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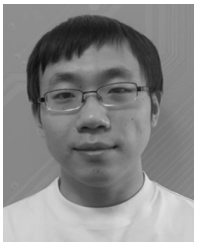

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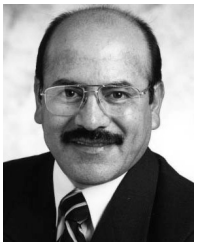

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