DPLL for Phase Noise Cancellation in Ring Oscillator-Based Quadrature Receivers

Zuow-Zun Chen, *Student Member, IEEE*, Yen-Cheng Kuan, *Member, IEEE*, Yilei Li, *Student Member, IEEE*, Boyu Hu, *Student Member, IEEE*, Chien-Heng Wong, *Student Member, IEEE*, and Mau-Chung Frank Chang, *Fellow, IEEE*

***Abstract*— In this paper, a low overhead phase noise cancellation technique for ring oscillator (RO)-based quadrature receivers is presented. The proposed technique operates in background and extracts RO phase noise as well as supply-induced phase noise from the digital phase-locked loop. The obtained phase noise information is then used to restore the randomly rotated baseband signal in digital domain. A receiver prototype is fabricated in standard 65-nm CMOS technology. It demonstrates a phase noise reduction from −88 to −109 dBc/Hz at 1-MHz offset and an integrated phase noise reduction from −16.8 to −34.6 dBc when operating at 2.4 GHz.**

***Index Terms*— Digital phase-locked loop (DPLL), frequency synthesizer, phase noise cancellation, radio receiver, ring oscillator (RO), sub-sampling time-to-digital converter (TDC).**

I. Introduction

RING oscillators (ROs) have gained increasing interest for applications in radio receivers due to their small area, wide tuning range, and multiphase output. However, compared with *LC* oscillators, ROs have higher phase noise and higher sensitivity to supply noise that may seriously deteriorate the received signal during the mixer down-conversion process. As shown in Fig. 1, there are two effects. The first one occurs, where the noisy LO signal mixes with the wanted signal. As shown in Fig. 1(a), this leads to LO close-in phase noise falling inside the signal bandwidth (BW) and degrading the signal-to-noise ratio (SNR). The second mechanism is the reciprocal mixing of interference signal. In a wireless environment, in addition to the wanted signal, various interference signals can also enter the receiver front end. As shown in Fig. 1(b), the LO signal mixes with the interference signal and causes phase noise to fold back on top of the wanted signal and thus degrades the SNR. While the reciprocal mixing noise can be canceled using the symmetrical property of phase noise [1], [2], canceling the close-in phase noise remains a challenge. The main focus of this paper is to alleviate the close-in phase noise effect in the RO-based quadrature receivers.

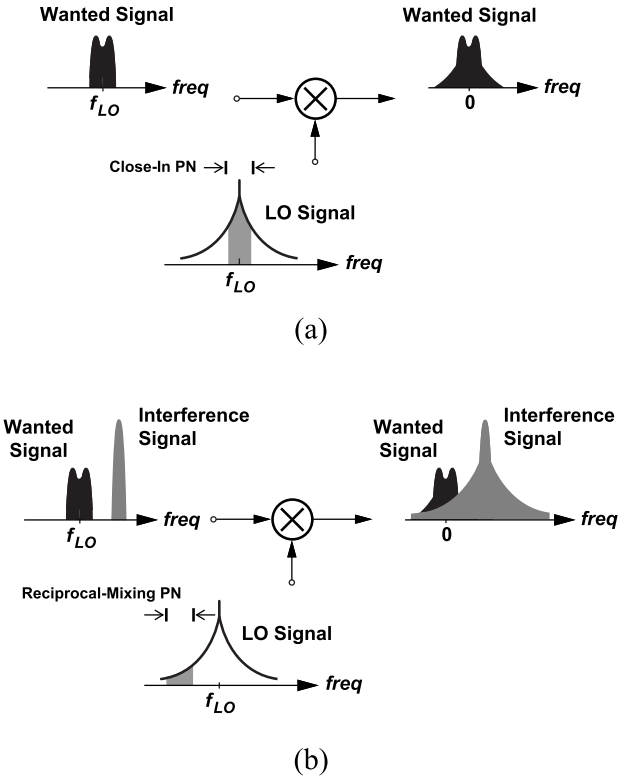

Fig. 1. Effect of LO phase noise in radio receivers. (a) Close-in phase noise effect. (b) Reciprocal-mixing phase noise effect.

Increasing phase-locked loop (PLL) BW can reduce the close-in phase noise of ROs [3]. Since voltage-controlled oscillator phase noise is high-pass filtered when appearing at the PLL output, larger BW results in more suppression on RO close-in phase noise. This relationship holds true for digitally controlled oscillators (DCOs) in digital PLLs (DPLLs) as well. Nevertheless, the BW is limited to 1/10 of the reference frequency (F_{REF}) in conventional type-II PLLs due to stability concerns. Moreover, increasing BW inevitably reduces the suppression of the spurious tones originated from the nonlinear behavior of either the time-to-digital converter (TDC) in DPLLs, or phase-frequency detector and charge pump circuits in analog PLLs. A delay-discriminator-based technique was proposed to cancel RO phase noise [4]. However, the technique showed limited jitter [or integrated phase noise

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Z.-Z. Chen, Y. Li, B. Hu, C.-H. Wong, and M.-C. F. Chang are with the High Speed Electronics Laboratory, University of California at Los Angeles, Los Angeles, CA 90095 USA (e-mail: zzchen@g.ucla.edu; mfchang@ee.ucla.edu).

Y.-C. Kuan and M.-C. F. Chang are with National Chiao Tung University, Hsinchu 30010, Taiwan.

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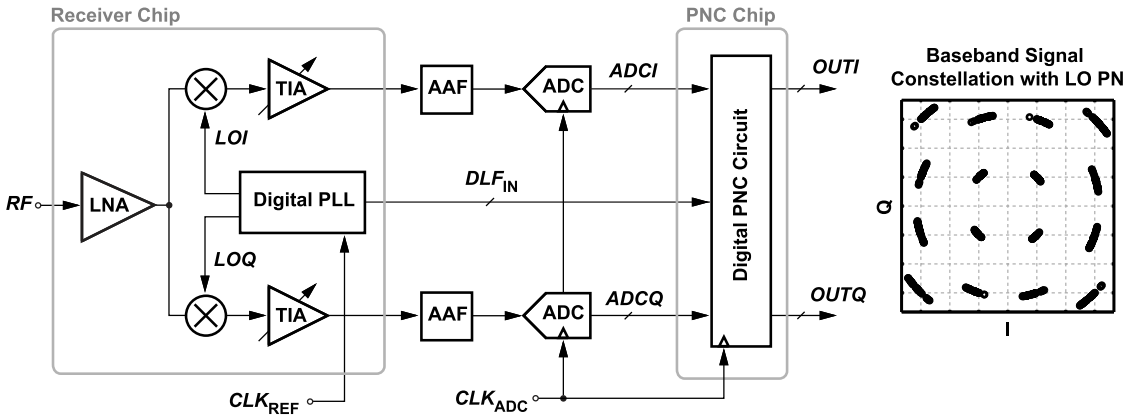


Fig. 2. Proposed PNC quadrature receiver system diagram and the baseband signal constellation affected by LO phase noise.

(IPN)] improvement, and is conducted in the analog domain. To circumvent the aforementioned constraints, here we present a digital phase noise cancellation technique capable of reducing both RO close-in and supply-induced phase noise for RO-based quadrature receivers.

This paper is organized as follows. Section II introduces the proposed receiver architecture. Section III explains how phase noise information is extracted from DPLL, followed by the detailed description of the phase noise cancellation circuit in Section IV. Section V shows the measurement results. Finally, this paper is concluded in Section VI.

II. Phase-Noise Canceling Receiver Architecture

Fig. 2 shows the block diagram of the proposed phase-noise-canceling (PNC) receiver [5]. The receiver system employs a common-gate low-noise amplifier (LNA) followed by quadrature passive mixers. The mixers' outputs are buffered by transimpedance amplifiers (TIAs), which convert current into voltage. The following anti-aliasing filters (AAFs) reject the out-of-channel noise, and then a pair of baseband ADCs (BBADCs) quantizes the analog quadrature baseband signals into digital. Furthermore, the digitized signals are applied to the digital PNC circuit for phase noise cancellation. The quadrature LO signals are generated from the DPLL, which employs an RO as the DCO. The idea behind the proposed PNC technique can be explained by observing the effect of LO close-in phase noise in time domain. Assume that the receiver input RF signal has the mathematical form of $RF(t) = I(t)\cos(\omega_{\mathrm{RF}}t) + Q(t)\sin(\omega_{\mathrm{RF}}t)$, where $I(t)$ and $Q(t)$ represent the wanted analog baseband signals and ω_{RF} is the RF frequency. The quadrature LO signals can be written as $LOI(t) = \cos(\omega_{\mathrm{LO}}t + \phi_{\mathrm{LO}}(t))$ and $LOQ(t) = \sin(\omega_{\mathrm{LO}}t + \phi_{\mathrm{LO}}(t))$, where $\phi_{\mathrm{LO}}(t)$ and ω_{LO} are the LO phase noise and the LO frequency, respectively. In zero-IF receiver, ω_{RF} equals to ω_{LO}. After mixer down conversion and BBADC digitization, the baseband signal in complex form can be expressed as

$$BB[n] = V_a(I[n] + jQ[n])\exp(j\omega_{\mathrm{LO}}[n]) \tag{1}$$

where V_a denotes the signal amplitude. $I[n]$ and $Q[n]$ are the digitized quadrature baseband signals, and $\phi_{\mathrm{LO}}[n]$ is the digitized LO phase noise. As shown in (1), the wanted signal is multiplied by a phase noise term, which causes random rotation on the constellation (Fig. 2). In order to restore the deteriorated baseband signal, we can first find a replica version of the phase noise information (e.g., $\phi_{\mathrm{NC}}[n]$) and apply a complex multiplication of $\exp(-j\phi_{\mathrm{NC}}[n])$ with $BB[n]$. In the proposed PNC technique, this replica phase noise information is extracted from the DPLL, and then used to counteract the random rotation in the digital PNC circuit.

Contrary to research in the past, which concentrates more on reducing phase noise from a DPLL circuitry perspective, this paper tackles the problem from a receiver system level point of view. It is not limited to RO-based DPLLs only but can be applied to *LC*-based DPLLs as well. In conventional DPLL approach, it requires large loop BW to suppress DCO phase noise. With the proposed PNC technique, the DPLL no longer needs large BW, but can rely on the phase noise cancellation loop to reduce DCO phase noise. This prevents the BW from being unacceptably large, which causes stability problems and less suppression on spurious tones at the DPLL output. In wireless applications, it is important to reduce the level of spurious tones in the LOs, because the interference signal can mix with these spurs and get down-converted right on top of the wanted signal. Since interference signal usually has larger power compared with the wanted signal, the spurs level needs to be much lower than the main LO tone. This requirement has motivated several research works to reduce PLL output spurs, such as linearization method, dithering method, and spurs cancellation technique [6]–[8]. A simple yet efficient way is by decreasing the DPLL BW. Although lower BW increases DCO close-in phase noise, this part of noise can be removed by the proposed PNC technique. Lower BW also slows down DPLL settling behavior. Nonetheless, this can be resolved by switching to type-I PLL for fast settling, and then switch back to type-II configuration after the loop settles [9].

III. Phase Noise Extraction

DPLLs are known for their compact digital loop filter (DLF) and reconfigurability of loop parameters. The latter feature, as shown in Fig. 3, comes from the fact that the digital signal in the feedback loop can be readily accessed and analyzed by a digital ASIC to obtain information regarding the loop

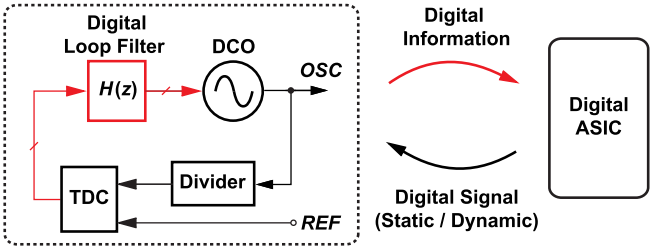


Fig. 3. DPLL reconfigurability.

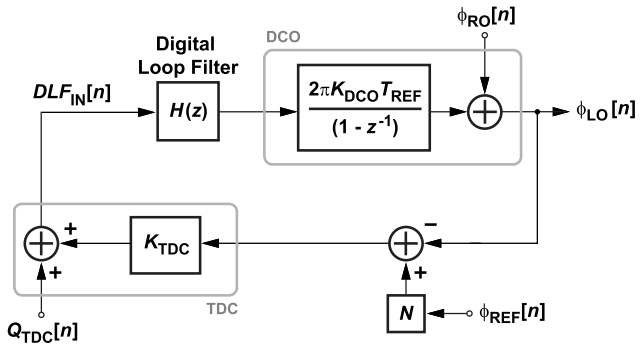
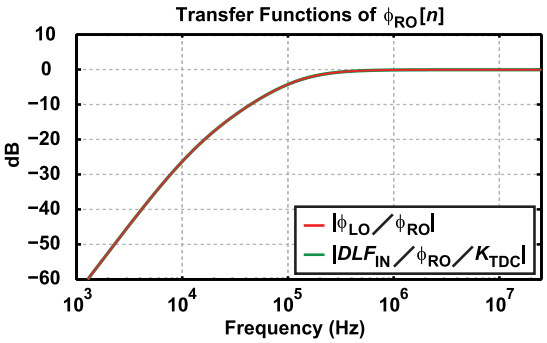
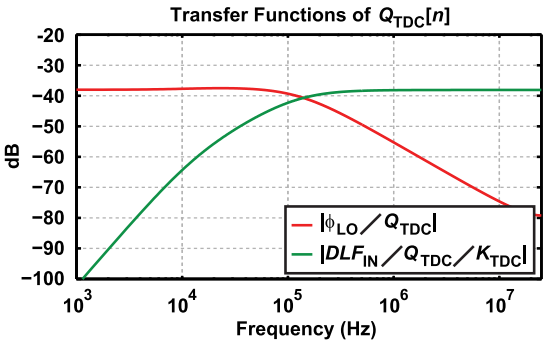


Fig. 4. DPLL discrete-time phase-domain model.



(a)



(b)

Fig. 5. (a) Transfer functions of $\phi_{\mathrm{RO}}[n]$ to PLL output and DLF input. (b) Transfer functions of $Q_{\mathrm{TDC}}[n]$ to PLL output and DLF input.

dynamics, including circuit impairments. The digital ASIC can then send either static control signals back into the loop to change the parameters, or dynamic calibration signals to mitigate the impairments. This property has been utilized to alleviate several DPLL nonidealities [10]–[13]. In this paper, we take advantage of the reconfigurability feature to extract RO phase noise. But instead of sending correction signal back to the DPLL, our approach applies the extracted RO phase noise information to digital baseband and cancels the phase noise effect in digital domain. In order to understand how RO phase noise is obtained, we examine the noise transfer functions of the DPLL. Fig. 4 shows a DPLL discrete-time phase-domain model [13], [14]. $H(z)$ is the DLF transfer function. The operation of the RO-based DCO is modeled as an integrator. K_{DCO} [Hz/s] and K_{TDC} [1/rad] are the gain of the DCO and TDC, respectively. $T_{\mathrm{REF}} = (1/F_{\mathrm{REF}})$ [s] is the period of the reference clock. The transfer functions for RO phase noise to PLL output and DLF input ($DLF_{\mathrm{IN}}[n]$) can be derived as

$$\frac{\phi_{\mathrm{LO}}(z)}{\phi_{\mathrm{RO}}(z)} = \frac{1}{1 + A(z)} \tag{2}$$

and

$$\frac{DLF_{\mathrm{IN}}(z)}{\phi_{\mathrm{RO}}(z)} = \frac{-K_{\mathrm{TDC}}}{1 + A(z)} \tag{3}$$

where $A(z) = 2\pi K_{\mathrm{TDC}} K_{\mathrm{DCO}} T_{\mathrm{REF}} H(z)/(1 - z^{-1})$ is the open-loop transfer function. As shown in Fig. 5(a), the RO phase noise encounters a high-passed transfer function at the PLL output and more more interestingly, it equals to the transfer function of RO phase noise to DLF input multiplied by $(-1/K_{\mathrm{TDC}})$. This means RO phase noise in $\phi_{\mathrm{LO}}[n]$ can be eliminated in principle by subtracting it with $(-DLF_{\mathrm{IN}}[n]/K_{\mathrm{TDC}})$. In addition, the phase noise extraction concept also applies to RO supply noise. Fluctuations on RO supply alter the oscillation frequency and further transfer into phase noise at the RO output. The transfer function of supply noise to DCO output phase noise can be modeled as $[2\pi K_{\mathrm{supply}} T_{\mathrm{REF}}/(1 - z^{-1})]$, where K_{supply} [Hz/V] is the pushing factor defined as the oscillation frequency change versus supply voltage change [15]. Since supply-induced phase noise and RO intrinsic phase noise are indistinguishable, both of them are captured in $DLF_{\mathrm{IN}}[n]$ and canceled through the noise subtraction process conducted in the digital PNC circuit. Beside these two noise sources, the DCO quantization noise also contributes to the RO output phase noise. K_{DCO} was designed to be 180 kHz/s, and is dithered by a first-order sigma-delta modulator clocked at around 312 MHz. This corresponds to -144.5 dBc/Hz at 1-MHz frequency offset [16]. Because DCO quantization noise is much lower than the RO intrinsic phase noise, it is neglected in the future RO phase noise discussion.

Other than RO phase noise, the TDC quantization noise ($Q_{\mathrm{TDC}}[n]$) should also be carefully considered in DPLL. The transfer functions of $Q_{\mathrm{TDC}}[n]$ to PLL output and DLF input are derived below

$$\frac{\phi_{\mathrm{LO}}(z)}{Q_{\mathrm{TDC}}(z)} = \frac{A(z)}{K_{\mathrm{TDC}}(1 + A(z))} \tag{4}$$

and

$$\frac{DLF_{\mathrm{IN}}(z)}{Q_{\mathrm{TDC}}(z)} = \frac{1}{1 + A(z)}. \tag{5}$$

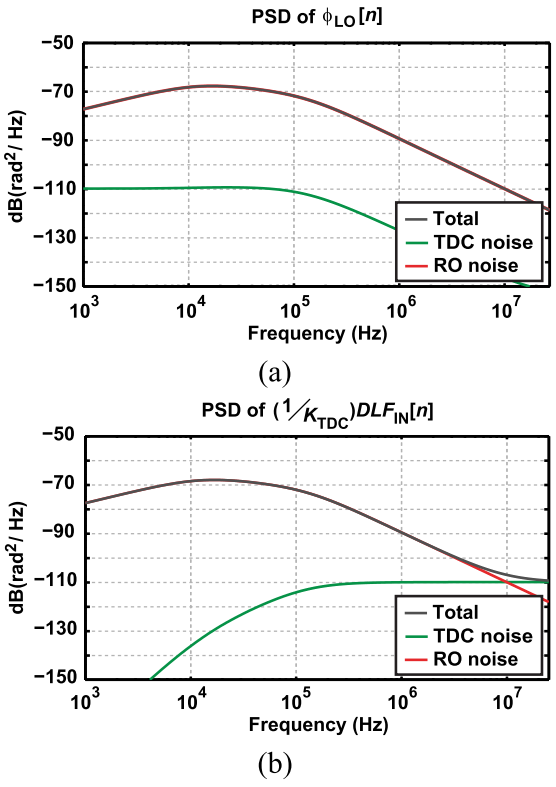


Fig. 6. (a) Calculated PSD of $\phi_{LO}[n]$. (b) Calculated PSD of $(DLF_{IN}[n]/K_{TDC})$.

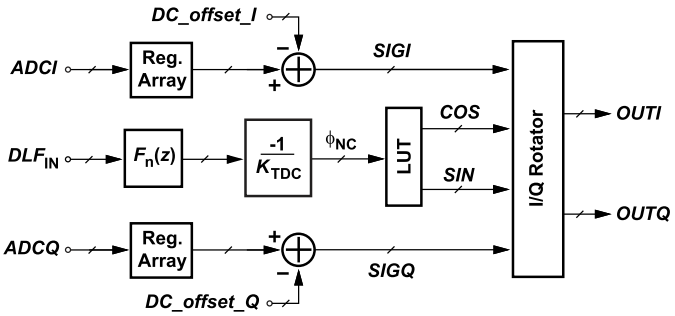


Fig. 7. Digital PNC circuit block diagram.

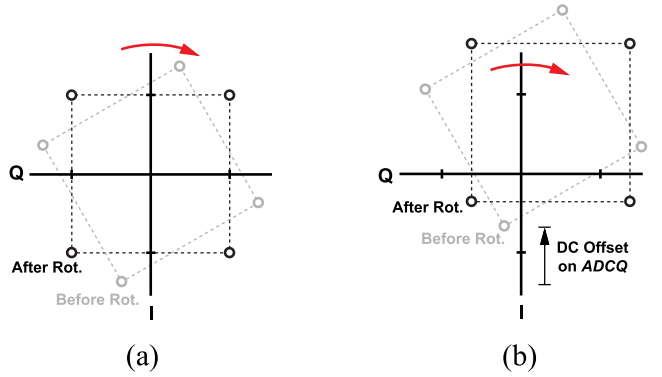


Fig. 8. (a) Correct I/Q rotation without dc offset. (b) Incorrect I/Q rotation with dc offset on $ADCQ[n]$.

As plotted in Fig. 5(b), the TDC quantization noise encounters a low-passed transfer function at the PLL output, but a high-passed transfer function at the DLF input. Fig. 6 shows the calculated DPLL noise spectrum. It can be seen that the RO phase noise at PLL output and DLF input is the same. However, the TDC quantization noise shows a low-passed shape at PLL output but a high-passed shape at DLF input. This indicates that while utilizing $DLF_{IN}[n]$ for phase noise cancellation, RO phase noise can be removed but TDC quantization noise still remains. For this reason, the sub-sampling TDC technique proposed in [17] is employed here in the DPLL. The sub-sampling TDC directly samples the high-frequency signal of the DPLL via an SAR-ADC and extracts the timing information that is embedded in voltage domain. The technique achieves a high resolution time-to-digital conversion and thus low TDC noise. This helps to improve the overall noise performance after phase noise cancellation.

IV. Phase Noise Cancellation

Fig. 7 shows the block diagram of the digital PNC circuit. The input signal $DLF_{IN}[n]$ from DPLL is first applied to a digital LPF $F_n(z)$ to filter out the high frequency part of TDC noise [see Fig. 6(b)]. Afterward, the digital LPF output is scaled by $(-1/K_{TDC})$ and sent to the LUT to generate the digital sine and cosine signals. The I/Q rotator then calculates the complex multiplication of $(SIGI[n] + jSIGQ[n])$ and $[\cos(\phi_{NC}[n]) - j\sin(\phi_{NC}[n])]$, where $SIGI[n]$ and $SIGQ[n]$ are the digital baseband signals after dc offset removal. As shown in Fig. 8, the dc offsets on the baseband signal paths need to be removed for correct rotation. Register arrays are implemented on the ADC input signal paths to adjust their delay. More detailed descriptions of the effect of delay difference between the ADC and $DLF_{IN}[n]$ signals will be explained later in this section. The time-domain expression for the output of the digital PNC circuit can be written as

$$OUT[n] = V_a'(I[n] + jQ[n])\exp(j\phi_{LO\_NC}[n]) \tag{6}$$

where $\phi_{LO\_NC}[n] = (\phi_{LO}[n] - \phi_{NC}[n])$ is the remaining noise that affects the baseband signal. From (2) and (3), the transfer function of $\phi_{RO}[n]$ to $\phi_{LO\_NC}[n]$ can be derived as

$$\frac{\phi_{LO\_NC}(z)}{\phi_{RO}(z)} = \frac{1}{1+A(z)} - \frac{F_n(z)}{1+A(z)}. \tag{7}$$

Similarly, the transfer function of $Q_{TDC}[n]$ to $\phi_{LO\_NC}[n]$ can be obtained with the aid of (4) and (5) as

$$\frac{\phi_{LO\_NC}(z)}{Q_{TDC}(z)} = \frac{A(z)}{K_{TDC}(1+A(z))} + \frac{F_n(z)}{K_{TDC}(1+A(z))}. \tag{8}$$

Fig. 9 shows the transfer functions of $\phi_{RO}[n]$ and $Q_{TDC}[n]$ to $\phi_{LO\_NC}[n]$. Fig. 10 shows the calculated noise spectrum of $\phi_{LO\_NC}[n]$. Compared with Fig. 6(a), the RO close-in phase noise is greatly reduced. The remaining noise is the TDC quantization noise and the residue of RO phase noise. Furthermore, let $\Phi_{TDC}(f)$ and $\Phi_{RO}(f)$ represent the TDC quantization noise and DCO phase noise spectrum, respectively. The IPN contributed by RO phase noise can be calculated as

$$\text{IPN}_{RO} = \int_{-F_{REF}/2}^{F_{REF}/2} \left|\frac{1-F_n(f)}{1+A(f)}\right|^2 \Phi_{RO}(f)df \tag{9}$$

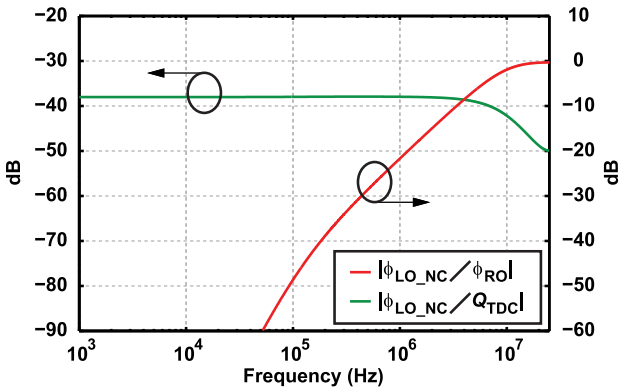


Fig. 9. Transfer functions of $\phi_{\mathrm{RO}}[n]$ to $\phi_{\mathrm{LO\_NC}}[n]$ and $Q_{\mathrm{TDC}}[n]$ to $\phi_{\mathrm{LO\_NC}}[n]$.

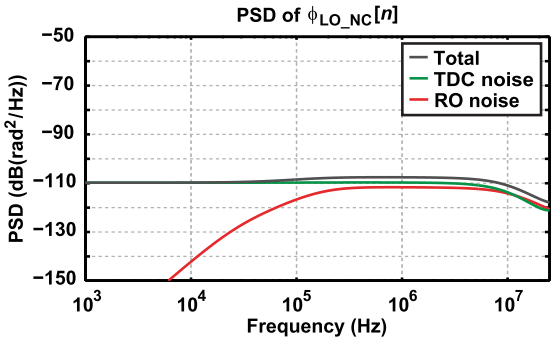


Fig. 10. Calculated PSD of $\phi_{\mathrm{LO\_NC}}[n]$.

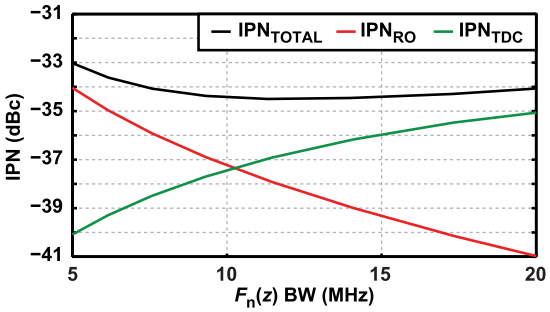


Fig. 11. Effect of $F_n(z)$ BW on the overall IPN.

and the IPN contributed by TDC noise can be found as

$$\mathrm{IPN_{TDC}} = \frac{1}{K_{\mathrm{TDC}}^2}\int_{-F_{\mathrm{REF}}/2}^{F_{\mathrm{REF}}/2}\left|\frac{A(f)+F_n(f)}{1+A(f)}\right|^2 \Phi_{\mathrm{TDC}}(f)df. \tag{10}$$

Fig. 11 shows the simulated IPN with respect to the different $F_n(z)$ BW while DPLL BW is fixed at 140 kHz. A smaller $F_n(z)$ low-pass corner reduces the TDC noise but increases the residue of RO phase noise after cancellation. On the other hand, a larger $F_n(z)$ low-pass corner reduces the RO phase noise but increases the TDC noise. In order to optimize the overall IPN, $F_n(z)$ BW should be set at the frequency where RO and TDC noise spectra intersect [18]. This renders both noise sources to have approximately equal contributions to IPN. In the design, $F_n(z)$ BW is set at around 12 MHz.

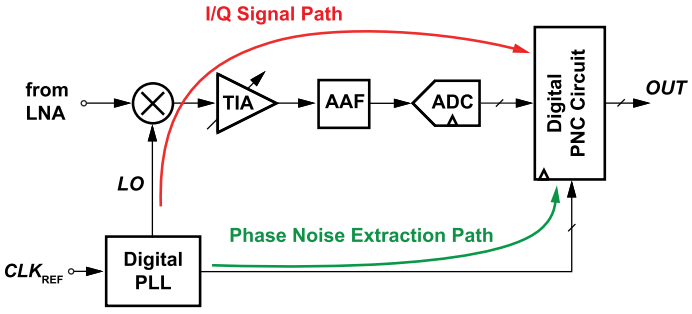


Fig. 12. Two delay paths. I/Q signal path and phase noise extraction path.

Note that in the conventional DPLL approach, the only way to achieve the optimum IPN is by setting the DPLL BW at the frequency where RO and TDC noise spectra intersect. This may not be applicable as the target BW can be larger than $F_{\mathrm{REF}}/10$, especially in RO-based DPLLs. Even more, larger BW reduces the suppression of spurious tones caused by TDC nonlinearity at the DPLL output. With the proposed PNC technique, the DPLL BW can be designed to have lower BW to provide more suppression on LO spurious tones, regardless of the tradeoff between TDC and DCO IPNs. The additional phase noise cancellation path with the $F_n(z)$ filter helps maintain the optimized IPN. The LUT size limits the PNC receiver to operate within $-(\pi/3)$ to $(\pi/3)$ [rad] of phase noise and about -10 dBc of IPN before phase noise cancellation. However, the operation range can be extended by increasing the LUT memory with the cost of larger area. Moreover, the signal $\phi_{\mathrm{NC}}[n]$ also contains spurious tones originated from the nonlinear behavior of the sub-sampling TDC. Although these spurs affect the wanted signal during the complex multiplication operation, they are not as critical as the spurs that appear in the LO signal. This can be observed from the receiver block diagram in Fig. 2. The interference signal at the receiver input can be very large compared with the wanted signal. But after down conversion, the interference signal will be greatly attenuated by the baseband AAFs thus significantly relaxes the spurs requirement for $\phi_{\mathrm{NC}}[n]$.

In noise canceling systems, the delay difference τ between the disturbing noise which deteriorates the wanted signal and the replica noise which is used to restore the wanted signal can greatly affect the system performance. The simplified PNC receiver block diagram with two important delay paths highlighted is plotted in Fig. 12. The first one is the I/Q signal path where the disturbing RO phase noise travels from the DPLL, through the mixer and BBADC, and ends up at the I/Q rotator in the digital PNC circuit. The second delay path is the phase noise extraction path, where the replica phase noise information is extracted from DPLL and sent to the I/Q rotator for noise cancellation. It is important to minimize the delay difference between these two paths. Fig. 13 shows the simulation results of the IPN after phase noise cancellation under different τ values. The IPN degrades as the delay increases. When the delay becomes greater than 10 μs, the disturbing noise and the replica noise become uncorrelated. Thus, subtracting the two would actually cause

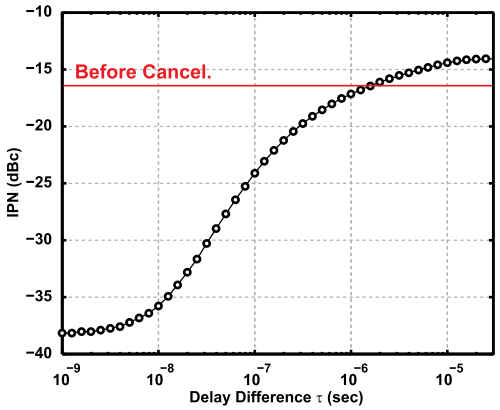


Fig. 13. Effect of delay difference τ on the overall IPN.

3-dB degradation compared with the case where no phase noise cancellation is applied. On the low delay difference end, the overall IPN would not be infinitely small but limited by the remaining TDC noise and RO phase noise (see Fig. 10).

The delay difference is constant in receiver systems, which have equal PLL reference clock ($CLK_{\rm REF}$) and BBADC sampling clock ($CLK_{\rm ADC}$) frequencies. It can be tuned out by adding analog delay cells on the leading delay path. However, in receiver systems that have different clock frequencies [19], [20], the delay difference is not constant but varies. In the proposed PNC quadrature receiver, the DPLL reference clock and the BBADC sampling clock frequencies are 49 and 62 MHz, respectively. In order to minimize the delay difference, the delay of each path is digitally controlled through register arrays implemented inside the DPLL and digital PNC circuit. In the following, the time varying delay difference and the operation of register arrays are explained in detail. Fig. 14(a) and (b) shows the timing diagram of $DLF_{\rm IN}[n]$ and $ADC[n]$ and the sampling clocks $CLK_{\rm REF}$ and $CLK_{\rm ADC}$. $DLF_{\rm IN}[n]$ is first delayed by K $CLK_{\rm REF}$ cycles in DPLL, and then resampled by the digital PNC circuit. On the other hand, $ADC[n]$ is delayed by M $CLK_{\rm ADC}$ cycles inside the digital PNC circuit, and then along with the resampled $DLF_{\rm IN}[n]$, both signals are sent to the I/Q rotator. In Fig. 14(a), $K = 5$ and $M = 7$. The first sample edge of $CLK_{\rm REF}$ leads the first sample edge of $CLK_{\rm ADC}$ by $dt1$. Because $DLF_{\rm IN}[0]$ is used to cancel phase noise in $ADC[0]$, the delay difference of this case equals to $dt1$. Fig. 14(b) plots another example with the first sample edges separated by $dt2$. Here, $dt2$ is greater than $T_{\rm X} = ((K+1)\times T_{\rm REF} - M\times T_{\rm ADC})$ but less than $T_{\rm REF}$. Under this condition, $DLF_{\rm IN}[1]$ is used to cancel phase noise in $ADC[0]$ and the delay difference here equals to $(dt2 - T_{\rm REF})$. Fig. 14(c) shows the relationship between dt and τ, where dt represents the time difference between the first sample edges. It is found that τ is actually periodic with respect to dt, indicating that τ is confined between $-\alpha T_{\rm REF}$ s and $(1-\alpha)T_{\rm REF}$ s, and

$$\alpha = \frac{T_{\rm ADC}}{T_{\rm REF}} M - K. \tag{11}$$

The minimum values of τ happen when α equals to 1/2. Moreover, the time delay Δ originated from the TIAs and

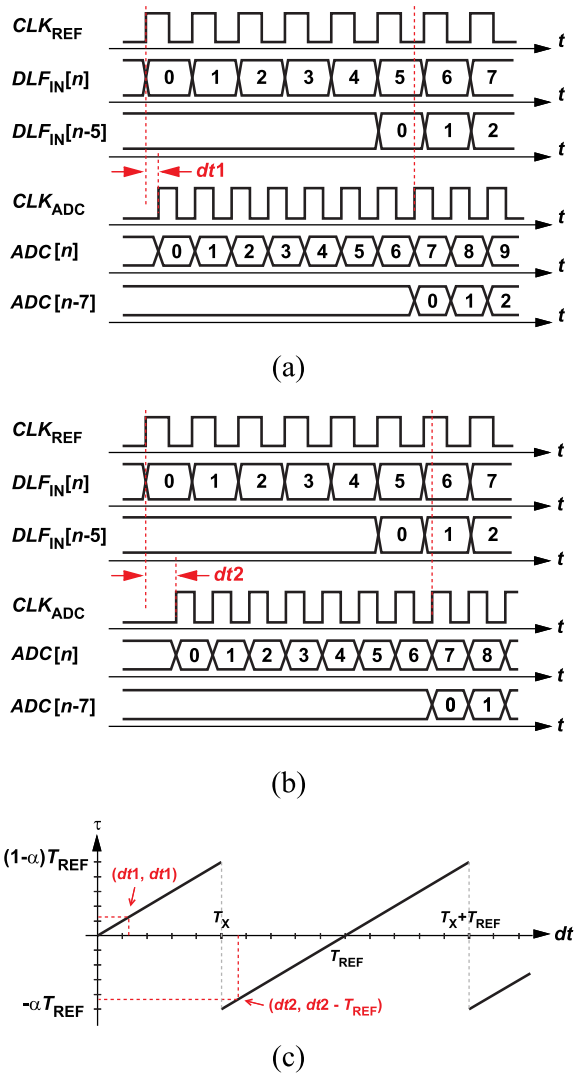


Fig. 14. Delay difference timing diagram. (a) Case 1: $0 \le dt < T_{\rm X}$. (b) Case 2: $T_{\rm X} \le dt < T_{\rm REF}$. (c) Delay difference τ with respect to dt.

the AAFs should also be taken into account. The effect of this delay causes the curve in Fig. 14(c) to down shift by Δ, and τ to fall between $-(\alpha T_{\rm REF} + \Delta)$ s and $[(1-\alpha)T_{\rm REF} - \Delta]$ s. In order to minimize the delay difference, α should be equal to $(1/2 - \Delta/T_{\rm REF})$, which becomes 1/2 when Δ is 0. From TIA circuit simulation and AAF data sheet, the delay Δ is about 20.1 ns, thus the target α is -0.48. With the aid of (11), the registers in DPLL and digital PNC circuit are set as $K = 6$ and $M = 7$. The delay difference range would fall between -10 and $+10$ ns. This corresponds to an rms τ of 5.8 ns and an IPN around -36 dBc.

V. Measurement Results

The PNC quadrature receiver prototype consists of two chips: a receiver chip and a PNC chip. Fig. 15 shows the die photos. The receiver chip contains the RO-based DPLL, LO buffers, and receiver chain (LNA, mixers, and TIAs). Its core area is 0.91 mm $\times$ 0.52 mm. The PNC chip contains the digital PNC circuit with a core area of 0.11 mm $\times$ 0.34 mm. Both chips are fabricated in a 65-nm CMOS technology and tested

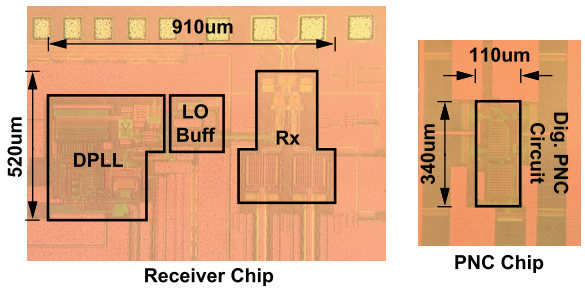


Fig. 15. Die photos of receiver chip and PNC chip.

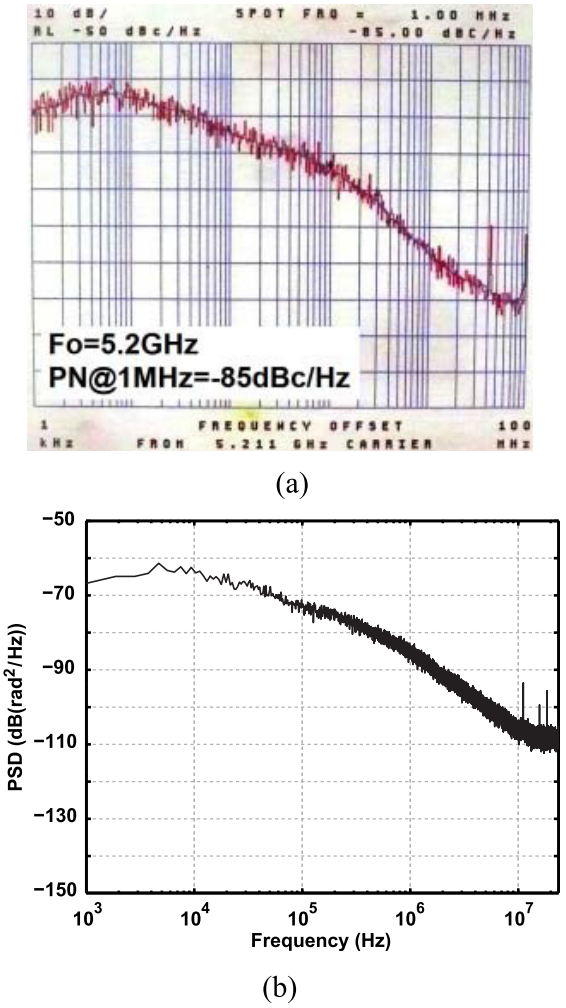


Fig. 16. Measurement results. (a) PLL output phase noise at 5.2 GHz. (b) PSD of $(DLF_{\mathrm{IN}}[n]/K_{\mathrm{TDC}})$.

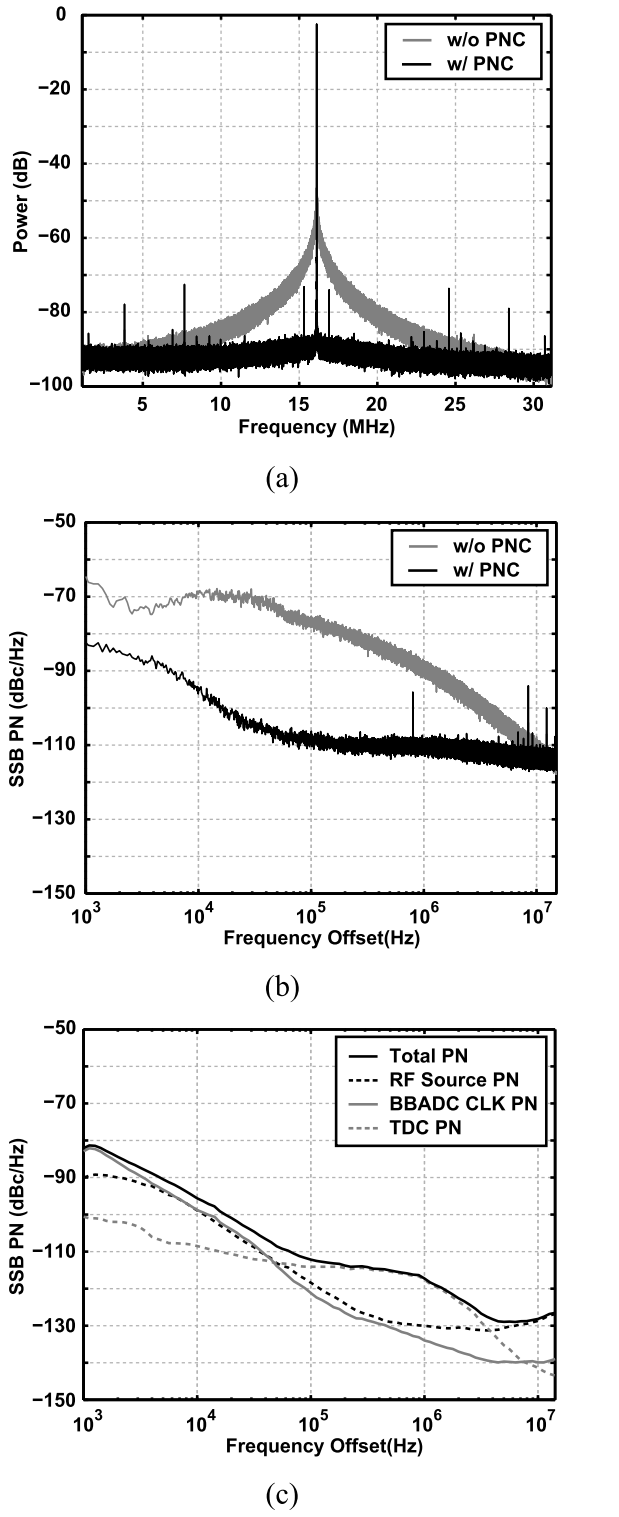


Fig. 17. 2.4-GHz single-tone input signal test. (a) Power spectrum of the digitized baseband signal. (b) SSB phase noise of the digitized baseband signal. (c) Phase noise contribution of RF source, BBADC sampling clock, and TDC noise.

together with off-chip AAFs and BBADCs. This arrangement allows more flexibility during test chip measurement and also avoids unwanted noise coupling between the DPLL and BBADCs.

The DPLL performance is characterized from a stand-alone chip. The measured DPLL output frequency is from 4.5 to 6.5 and 2.25 to 3.25 GHz through a divide-by-2 and multiplexing circuit at the DPLL output. The measured phase noise results along with the extracted $(DLF_{\mathrm{IN}}[n]/K_{\mathrm{TDC}})$ spectra are reported in Fig. 16. The DPLL BW is set at 140 kHz. As shown, the two noise spectra match up to around 12 MHz ($\approx F_{\mathrm{REF}}/4$), and after that, TDC high-passed noise dominates the high frequency spectrum of $(DLF_{\mathrm{IN}}[n]/K_{\mathrm{TDC}})$.

To verify the phase noise cancellation concept, the PNC quadrature receiver is first tested by receiving a 2.4-GHz

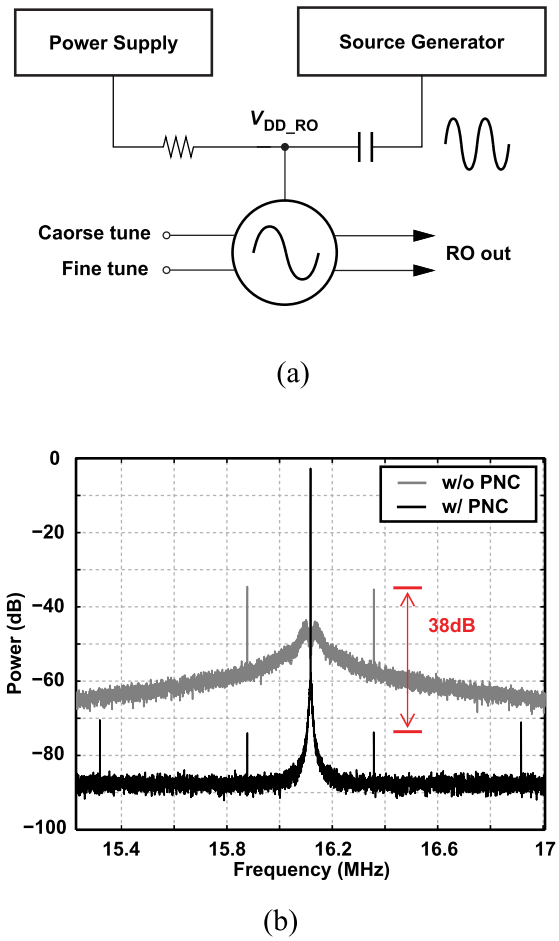


Fig. 18. 2.4-GHz single-tone input signal test with supply noise injection. (a) Test setup. (b) Power spectrum of the digitized baseband signal.

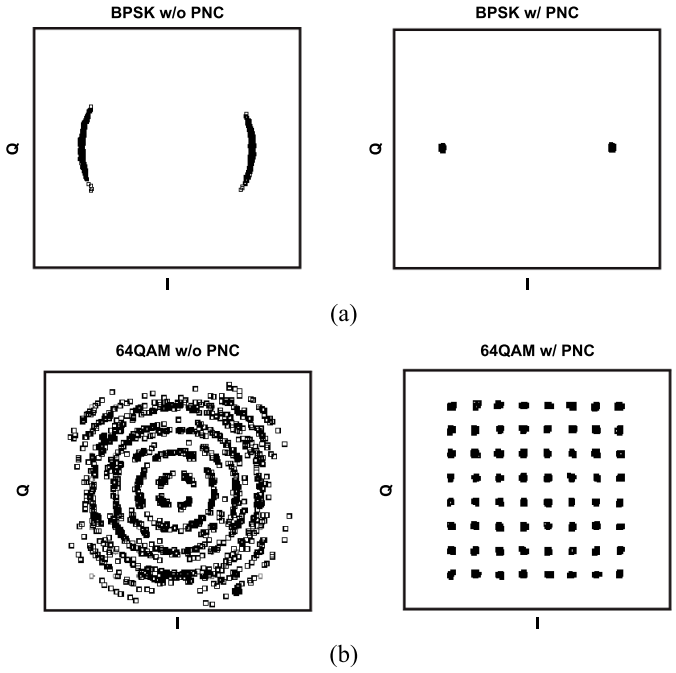


Fig. 19. Measured constellation with and without PNC. (a) BPSK signal. (b) 64QAM signal.

single-tone signal. Fig. 17(a) and (b) shows the power spectrum and single sideband (SSB) phase noise of the digitized baseband signal. With PNC, the spot phase noise at 1-MHz offset is reduced by 21 dB, from −88 to −109 dBc/Hz. The IPN integrated from 1-kHz to 15-MHz frequency offset is improved by 17.8 dB from −16.8 to −34.6 dBc. The noise sources that contribute to the phase noise at low frequency offset are the RF source, BBADC sampling clock, and the sub-sampling TDC noise. Fig. 17(c) shows their phase noise profile at low frequency offset. The RF source phase noise is found from direct measurement. The BBADC clock phase noise is scaled down by $20\log_{10}(62/16\ \text{MHz}) = 11.7$ dB from test result. Because the DPLL output phase noise is dominated by RO phase noise, it is not possible to directly measure TDC noise. Therefore, it is estimated from [17] and referred to 2.4 GHz. On the other hand, in Fig. 17(b), there is no evident roll-off after 12 MHz, which was predicted in Fig. 10. It is found that the receiver noise floor is around −117 dBc/Hz, which limited the phase noise performance at high frequency offset.

The pushing factor of the RO is measured to be 1500 MHz/V. The high pushing factor is due to the current-mode logic (CML) delay cells employed in the RO-based DCO. Neither LDOs nor components with negative supply sensitivity were used. To verify the PNC technique on supply noise reduction, a 240-kHz sinusoidal tone is injected onto RO supply. Fig. 18(a) shows the test setup. The test result is shown in Fig. 18(b). The injected supply noise causes a −33-dBc spurious tone at 240 kHz. With PNC, the supply-induced phase noise is suppressed by 38 dB to −71 dBc. Because there was no supply monitor, the actual on-chip supply fluctuation is predicted from circuit simulation and is estimated to be 14 μV_{p-p}. Note that the supply noise cancellation is frequency-dependent. In conventional DPLLs, it is related to the transfer function of DCO phase noise to DPLL output phase noise, as shown in Fig. 5(a). However, in the proposed phase noise cancellation technique, it is determined by the transfer function of the DCO phase noise to the digital PNC circuit output phase noise, as shown in Fig. 9. If we compare the amount of attenuation at 240 kHz, the proposed phase noise cancellation technique achieves 38 dB more supply noise suppression compared with the original DPLL, which is verified from the measurement result. Fig. 19 shows the measured constellation of receiving BPSK and 64QAM signals with 10 Msymb/s of data rate and carrier frequency around 2.4 GHz. The error vector magnitude (EVM) improvement demonstrates that the proposed PNC technique greatly reduces RO phase noise, achieving an EVM of −36.8 and −37.5 dB for BPSK signal and 64QAM signal, respectively.

The supply voltages are 1 V for the DPLL, LO buffer, and digital PNC circuit, and 1.2 V for the receiver chain. The total power consumption, excluding off-chip AAFs and BBADCs, is 46.5 mW, where 32.5 mW is consumed by the receiver chain, and 14 mW from the DPLL, including the digital PNC circuit. The DPLL consumes 12 mW of power, 6 mW for the sub-sampling TDC, 5.5 mW for the RO, and 0.5 mW for

TABLE I
PERFORMANCE SUMMARY

		This Work	[4]	[11]
Topology	Noise Extraction	Digital PLL	Delay Discriminator	Test-Signal Based
	Noise Cancellation	Digital PNC Circuit	NC Delay Cell	NC Transistors[5]
Operation Freq. (GHz)		2.25~3.25, 4.5~6.5	3.5~7.1	0.4~3
Spot PN w/o PNC (dBc/Hz)		-88@1MHz	-92.5@1MHz	N/A
Spot PN w/i PNC (dBc/Hz)		-109@1MHz	-105@1MHz	N/A
IPN w/o PNC (dBc)		-16.8 (1K~15M)	-15.7 (10K~10M)[1]	-18.0 (50K hits)[1]
IPN w/i PNC (dBc)		-34.6 (1K~15M)	-18.5 (10K~10M)[1]	-22.5 (50K hits)[1]
Core Area (mm^2)		0.47[2] / 0.17[3] / 0.04[4]	0.12[3]	0.08[3]
Power (mW)		46.5[2] / 14[3] / 2[4]	29.6[3]	3.1[3]
Supply (V)		1 / 1.2	1.2	1
Technology (nm)		65	90	130

[1]Calculated from jitter [2]Off-chip AAFs and ADCs excluded [4]Digital PNC circuit
[3]PLL circuit including noise extraction & cancellation [5]Supply noise cancellation

the DLF. The digital PNC circuit itself consumes 2 mW of power and 0.04 mm^2 of area. Table I summarizes the system performance.

VI. CONCLUSION

A digital PNC technique for RO-based quadrature receivers is presented in this paper. The RO phase noise information is extracted from the DPLL, and then used to restore the randomly rotated baseband signal in digital domain. The proposed technique enables RO-based LO to be used in complex modulation systems, which are more sensitive to phase noise. In practice, the overall noise performance is limited by the TDC noise and the delay difference between the I/Q signal path and the phase noise extraction path. However, it is believed that the TDC resolution can continue to be improved as CMOS processes advance. The delay difference limitation can be further mitigated through digital interpolation filters. The digital-intense and background processing natures of the proposed PNC technique allow it to be easily implemented in parallel with reciprocal mixing noise cancellation techniques, to reduce both close-in and out-of-band phase noise.

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Zuow-Zun Chen (S'16) was born in Taipei, Taiwan. He received the B.S. degree in computer science and information engineering and the M.S. degree in electronics engineering from National Taiwan University, Taipei, in 2005 and 2008, respectively. He is currently pursuing the Ph.D. degree in electrical engineering with the University of California at Los Angeles (UCLA), Los Angeles, CA, USA.

In 2013, he joined Broadcom Corporation, Irvine, CA, USA, as a Mixed-Signal IC Design Intern. His current research interests include mixed-mode and RF circuit design.

Mr. Chen was a recipient of the UCLA-Mediatek Fellowship from 2014 to 2015.

Yen-Cheng Kuan (M'12) received the B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, and the M.S. and Ph.D. degrees in electrical engineering from the University of California at Los Angeles, Los Angeles, CA, USA.

From 2004 to 2007, he was a System Engineer with Realtek Semiconductor Corporation, Irvine, CA, USA, where he was involved in the design of ultrawideband system-on-a-chip. From 2009 to 2016, he was a Research Scientist with HRL Laboratories, Malibu, CA, USA, where he was involved in software-defined radios, compressed-sensing receivers, multirate signal processing for high-speed ADCs, and image processors. He is currently the MediaTek Junior Chair Professor with the International College of Semiconductor Technology, National Chiao Tung University, Hsinchu, Taiwan. He holds over 20 U.S./international granted/applied patents. His current research interests include low-power architecture design and system level design for various DSP applications.

Dr. Kuan was a recipient of the HRL new inventor award for his invention contribution.

Yilei Li (S'14) received the B.S. and M.S. degrees in microelectronics from Fudan University, Shanghai, China, in 2009 and 2012, respectively. He is currently pursuing the Ph.D. degree with the University of California at Los Angeles, Los Angeles, CA, USA.

His current research interests include circuit and system design for emerging applications, including software-defined radio, multiband RF interconnect, and terahertz imaging systems.

Mr. Li was a recipient of the Henry Samueli Fellowship in 2012 and the Broadcom Foundation Fellowship in 2015.

Boyu Hu (S'13) received the B.Sc. degree (Hons.) from the Chu Kochen Honors College, Zhejiang University, Hangzhou, China, in 2008, the M.S. degree from the Institute of VLSI Design, Zhejiang University, in 2011, and the Ph.D. degree from the University of California at Los Angeles, Los Angeles, CA, USA, in 2016.

In 2011, he was an RF/Mixed-Signal IC Designer with Marvell, Shanghai, China, where he was involved in low-power wireless transceivers. He was a Mixed-Signal IC Design Intern with Broadcom, Irvine, CA, USA, where he was involved in high-precision mixed-signal audio products. His current research interests include high-speed/high-precision mixed-signal integrated circuit and system, hardware mapping of complex algorithms, and its related very large scale integration architecture and design.

Dr. Hu was a recipient of the Broadcom Foundation Fellowship in 2014.

Chien-Heng Wong (S'14) received the B.S. and M.S. degree in electrical engineering from National Taiwan University (NTU), Taipei, Taiwan, in 2008 and 2011, respectively. He is currently pursuing the Ph.D. degree at the University of California at Los Angeles, Los Angeles, CA, USA.

From 2011 to 2012, he was a Mixed-Signal Engineer with Faraday Technology. From 2012 to 2013, he was a Research Assistant with NTU. His current research interests include mixed-signal circuits, such as phase-locked loops, ADCs, and wireline transceivers.

Mau-Chung Frank Chang (M'79–SM'94–F'96) is currently the President of National Chiao Tung University, Hsinchu, Taiwan, and the Wintek Chair Professor of Electrical Engineering with the University of California at Los Angeles, Los Angeles, CA, USA. His current research interests include the development of high-speed semiconductor devices and high-frequency integrated circuits for radio, radar, and imaging system-on-chip applications up to the terahertz frequency regime.

Dr. Chang is a member of the U.S. National Academy of Engineering, a fellow of the U.S. National Academy of Inventors, and an Academician with the Academia Sinica of Taiwan. He was a recipient of the IEEE David Sarnoff Award in 2006 for developing and commercializing GaAs HBT and BiFET power amplifiers for modern high-efficiency and high-linearity smart-phones in the past 2.5 decades.