A 1.2-GS/s 8-bit Two-Step SAR ADC in 65-nm CMOS With Passive Residue Transfer

Hai Huang, *Student Member, IEEE*, Ling Du, and Yun Chiu, *Senior Member, IEEE*

***Abstract*— A high-speed 2b–1b/cycle two-step successive-approximation-register analog-to-digital converter (ADC) exploiting the passive residue transfer technique is reported. The removal of the residue amplifier results in savings in the time and power consumed by the residue transfer process. The kT/C noise and potential bandwidth mismatch associated with the passive residue transfer are analyzed and also verified by circuit simulations. The use of the 2b–1b/cycle hybrid conversion scheme with an appropriate resolution partition further enhances the conversion speed. Fabricated in a 65-nm CMOS process, the prototype ADC measured a signal-to-noise plus distortion ratio of 43.7 dB and a spurious-free dynamic range of 58.1 dB for a near-Nyquist input. The total power consumption of the ADC is 5 mW and the achieved figure of merit is 35 fJ/conversion-step, all measured at a sample rate of 1.2 GS/s.**

***Index Terms*— 2b–1b/cycle conversion scheme, analog-to-digital conversion, high-speed successive-approximation-register (SAR) architecture, passive residue transfer, two-step SAR.**

I. Introduction

COMMUNICATION systems such as ultra-wideband radios, serial link, and broadband Ethernet transceivers demand high-speed and medium-resolution analog-to-digital converters (ADCs) with low power consumption. The successive-approximation-register (SAR) conversion architecture is an attractive option for these applications due to its low analog complexity and excellent power efficiency. However, compared to the flash and pipeline architectures, the serial conversion process of the SAR ADC still dramatically limits its conversion speed. In recent years, a few speed-acceleration techniques for non-interleaved, single-channel SAR ADC have been reported [1]–[7], which will be briefly reviewed below.

First, an asynchronous clocking scheme was used in [1] and [2] to reduce the SAR loop delay. In the conventional synchronous design, the time allocated to all bit cycles is the same and decided by the slowest cycle, resulting in some idle time in the faster bit cycles. In contrast, for asynchronous clocking, the time for each SAR cycle is independently assigned based on the comparator's decision delay in this cycle, therefore eliminating the wasted time and increasing the overall conversion speed.

Second, resolving multiple bits in each SAR cycle is a popular way of increasing the ADC throughput [3], [4]. Ideally, the conversion speed (excluding the input sampling time) of a multi-bit SAR ADC can be improved by a factor equal to the number of bits resolved in each cycle. One drawback of this architecture is that its resolution is restricted by the comparator offset—just like the flash ADC, it is necessary to limit the comparator offset to less than half an LSB in each conversion cycle to avoid any gross conversion errors. In addition, a multi-bit SAR ADC also requires two digital-to-analog converters (DACs), i.e., a signal DAC (SIG-DAC) and a reference DAC (REF-DAC). The former is used to perform the sampling and successive approximations of the signal, whereas the latter is to supply multiple threshold voltages for all the comparators involved during the SAR cycles. Naturally, this setup invites a mismatch problem between the SIG-DAC and the REF-DAC [4].

Third, the two-step pipeline SAR is another structural extension to the conventional SAR ADC for breaking the speed limit [5], [6]. Its overall quantization is partitioned into two steps and an accurate amplifier is needed to transfer the conversion residue from the first stage to the second. Typically, the conversion throughput and power consumption of the two-step approach are limited in part by the achievable bandwidth and power efficiency of the residue amplifier, respectively. This is particularly true for ultra-high-speed scenarios, wherein the parasitic capacitance of the amplifier is comparable to its capacitive loading so burning more power to increase the bandwidth becomes ineffective.

In this paper, an asynchronous 2b–1b/cycle two-step SAR architecture exploiting the passive residue transfer technique is presented in an attempt to push the conversion speed further [8]. Benefiting from the passive residue transfer, the bandwidth-limiting amplifier is removed and a faster residue transfer that also consumes less power is obtained. Additionally, an asynchronous 2b–1b/cycle conversion scheme with an appropriate resolution partition further improves the conversion throughput. A prototype ADC was designed and implemented in a 65-nm CMOS process. At a sample rate of 1.2 GS/s, the ADC measured a signal-to-noise plus distortion ratio (SNDR) of 43.7 dB and a spurious-free dynamic range (SFDR) of 58.1 dB for a near-Nyquist input while consuming a total power of 5 mW, culminating in a Walden figure of merit (FoM) of 35 fJ/conversion-step.

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H. Huang and Y. Chiu are with the Texas Analog Center of Excellence, University of Texas at Dallas, Richardson, TX 75080 USA (e-mail: haihuang1965@gmail.com).

L. Du is with Chengdu MECS Microelectronics Technology, Chengdu 611731, China.

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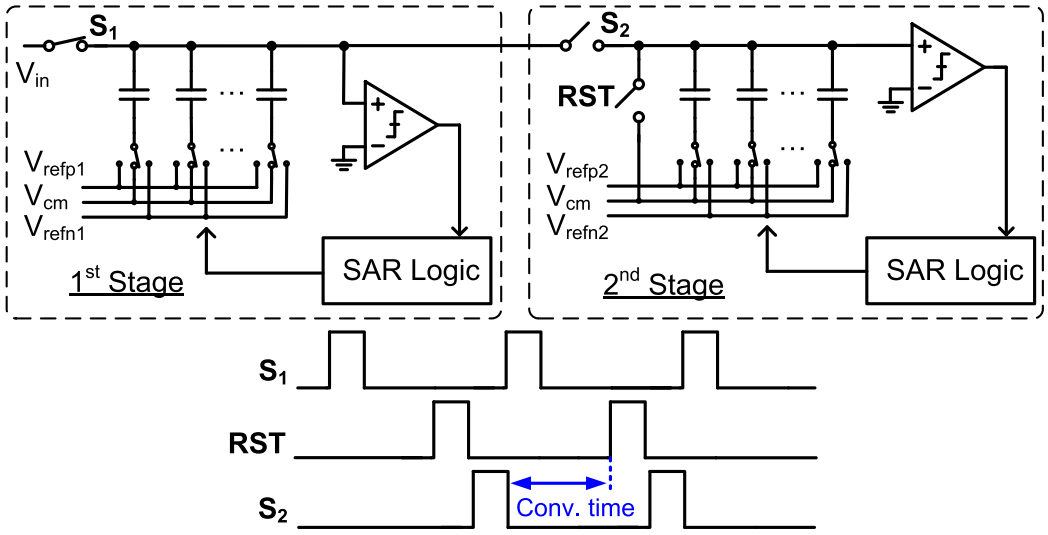

Fig. 1. Schematic and timing diagram of attenuated passive residue transfer.

This paper is organized as follows. First, the operation principles of passive residue transfer are presented in Section II. Second, the kT/C noise and the possible bandwidth mismatch issue of the passive residue transfer technique are analyzed in Section III. Third, the prototype ADC design with circuit implementation details is described in Section IV. Last, Section V showcases the measurement results and Section VI concludes this paper.

II. Passive Residue Transfer

In general, there are two approaches to transfer the residue voltage passively. One is termed the *attenuated* passive residue transfer while the other one is the *non-attenuated* passive residue transfer. In the following sections, the operation principles, advantages, and disadvantages of the two approaches will be introduced.

A. Attenuated Passive Residue Transfer

The working principle of the attenuated passive residue transfer is illustrated in Fig. 1. First, the sampling switch S_1 turns on and the first-stage DAC samples the input signal. Then, the first stage performs the coarse conversion. Once the conversion is done, the residue voltage will be generated by the first-stage DAC while the second-stage DAC is reset. After that, the transfer switch S_2 turns on and the second-stage DAC is utilized to share the charge stored on the first-stage DAC. Last, when the switch S_2 turns off, the second stage starts the fine conversion.

A critical problem associated with this approach is the residue signal attenuation stemming from the charge sharing between the two DACs. Obviously, the signal attenuation brings about a stringent constraint on the noise of the second-stage comparator, thereby dictating more power consumption. The signal attenuation also reduces the input voltage of the second-stage comparator and increases the decision time inevitably. Furthermore, this method needs an explicit clock phase for resetting the DAC, potentially reducing the timing budget of the second stage (see Fig. 1).

B. Non-Attenuated Passive Residue Transfer

The non-attenuated passive residue transfer, as shown in Fig. 2, is to employ two DACs in a ping-pong configuration to alternately transfer the residue voltage from the first stage to the second [9], [10]. To begin with, both the sampling switch S_1 and transfer switch S_{2a} or S_{2b} turn on and the input signal is sampled by the DACs of both stages. Then the sampling switch S_1 turns off and the first stage performs the coarse conversion as well as the generation of the residue voltage. Note that, in this period, the second stage A or B is idle and its DAC just appears as a "parasitic capacitor" to the first-stage DAC. Once the residue generation completes, the transfer switch S_{2a} or S_{2b} turns off and the residue is acquired by the second stage immediately. Finally, the second stage A or B is activated for the fine conversion. This process is repeated with alternate participation of different second stages A and B.

Because the DAC in the second stage does not need to be reset explicitly before transferring the residue, the second stage can utilize the whole period to quantize the residue voltage (see Fig. 2) and its timing burden can be effectively alleviated. Since the residue signal is not attenuated, this technique not only accelerates the decision of the second-stage comparator but also provides some SNR benefit relative to the attenuated passive residue transfer. For power consumption, considering that the ping-pong stages work alternately (i.e., one works while the other is mostly idle), the total power of its comparators and SAR logic are similar to that of the conventional structure without ping-pong. For a two-step ADC, the noise of the first-stage comparator impacts the residue voltage and the first-stage digital output equally but with opposite polarity, resulting in a noise cancellation in the overall digital output of the ADC [11]. As the noise of the first-stage comparator does not contribute to the overall noise budget of the ADC, it can be reasonably downsized to save power. In summary, this approach does not suffer too much power penalty in comparison to the one-step conventional SAR structure.

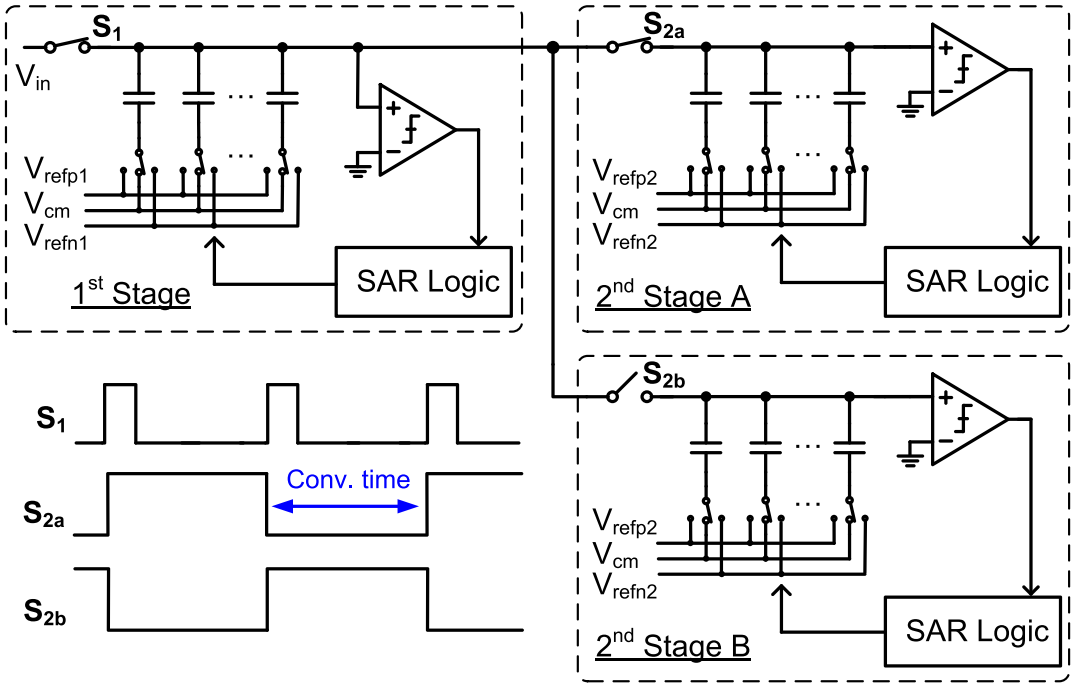

Fig. 2. Schematic and timing diagram of non-attenuated passive residue transfer.

A drawback of this technique is the area overhead due to the ping-pong second stages. In addition, when the first stage is quantizing the sampled input, the second-stage DAC just appears as a "parasitic capacitor" to the first stage. Naturally, the reference level of the first stage is attenuated by the second-stage DAC during the bit cycles. Fortunately, for high-speed ADCs, the input signal swing is normally restricted by the linearity of the S/H instead of the reference swing [3], [7], so the reference attenuation problem has a minor effect on the overall ADC accuracy. However, for high-resolution ADC, the reference attenuation problem may limit the ADC's input swing and finally reduce the input swing of the second-stage comparator. This means the second-stage comparator in this structure need to consume more power than that in conventional SAR ADC to achieve the same noise performance. Note that the input parasitic capacitors of the comparators attenuate the reference levels of the first and the second stages by different factors, which equivalently modify the exact value of the interstage gain and dictate a gain calibration.

Due to its speed and SNR benefits, this approach is utilized in the prototype ADC for transferring the residue voltage passively. As a consequence of the non-attenuated passive residue transfer, no bandwidth-limiting amplifier is employed in the design and a fast, as well as power efficient, residue transfer is attained.

III. Noise and Bandwidth Mismatch Analysis

A. kT/C Noise Analysis

For the non-attenuated passive residue transfer, two sampling operations are involved in one conversion cycle. Its kT/C noise is supposedly different from that of the conventional sampling scheme and needs to be investigated [9]. The analysis can be approached by the circuit model shown in Fig. 3,

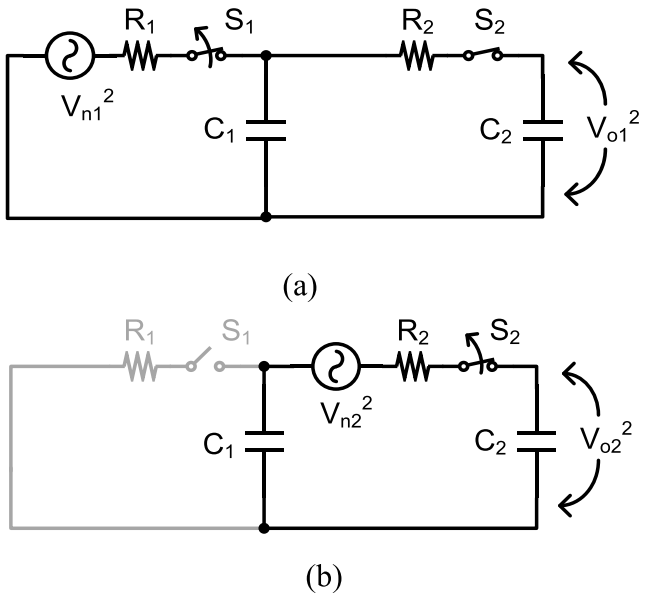

Fig. 3. Circuit model for the kT/C noise analysis of passive residue transfer. (a) Sampling. (b) Residue transfer.

where C_1 and C_2 are the total DAC capacitances of the first and second stages, respectively. For a two-step ADC, only the output noise stored on C_2 contributes to the overall noise budget. The output noise on C_2 consists of the noise due to the sampling switch S_1 (V_{o1}) and that induced by the transfer switch S_2 (V_{o2}). To simplify the analysis, these two parts of output noise are studied separately. In Fig. 3(a), when the sampling switch S_1 turns off, the output noise power can be derived as

$$\overline{V_{o1}^2} = \frac{kT}{C_1 + C_2}. \tag{1}$$

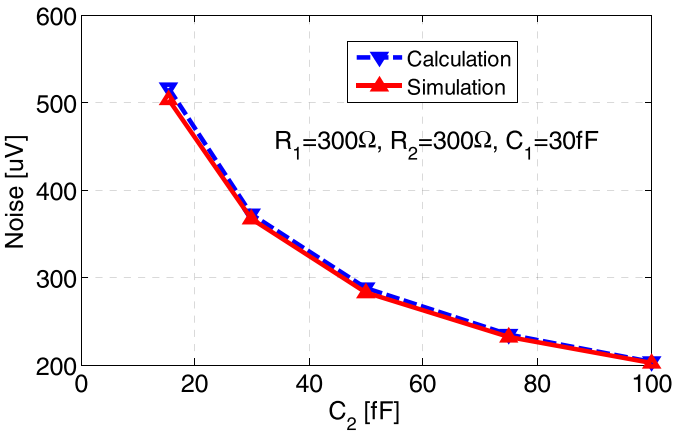

Fig. 4. Simulated kT/C noise and the calculated kT/C noise.

In Fig. 3(b), the noise power equals to

$$\overline{V_{n2}^2} = \frac{kT(C_1+C_2)}{C_1C_2} \tag{2}$$

so the output noise power V_{o2}^2 coming from the transfer switch S_2 is expressed as

$$\overline{V_{o2}^2} = \left(\frac{C_1}{C_1+C_2}\right)^2 \overline{V_{n2}^2} = \frac{kTC_1}{(C_1+C_2)C_2}. \tag{3}$$

The total output noise power on C_2 is the summation of the noise power in (1) and (3) and can be simplified to

$$\overline{V_{on}^2} = \overline{V_{o1}^2} + \overline{V_{o2}^2} = \frac{kT}{C_2}. \tag{4}$$

Interestingly, (4) indicates that the total noise power is unrelated to the capacitance C_1 and only decided by C_2! This simple result can also be explained using the so-called equipartition theorem from statistical mechanics [12], [13]. According to the equipartition theorem, any energy storage element (capacitors in Fig. 3) in thermal equilibrium keeps an average noise energy with a value of kT/2. As a result, for the circuit in Fig. 3, we can easily obtain

$$\overline{\frac{1}{2}C_2V_{\text{on}}^2} = \frac{kT}{2} \tag{5}$$

$$\overline{V_{\text{on}}^2} = \frac{kT}{C_2}. \tag{6}$$

It can be seen clearly from Fig. 4 that the aforementioned noise analysis matches the PNOISE simulation results of the circuit in Fig. 3 accurately. Guided by (4), C_2 in the prototype ADC is chosen to be 15.5 fF and the corresponding kT/C noise power is roughly equal to half of the quantization noise power.

B. Bandwidth Mismatch Analysis

For non-attenuated passive residue transfer, the DAC of the second stage participates in the sampling of the input signal. Consequently, the input signal alternately sees one of two second-stage DACs in the sampling phase through the transfer switches S_{2a} or S_{2b}. As shown in Fig. 5, any mismatch between the two DACs and/or between S_{2a} and S_{2b} will contribute to the bandwidth mismatch of the sampling network. Typically, the DACs' mismatch is much smaller than

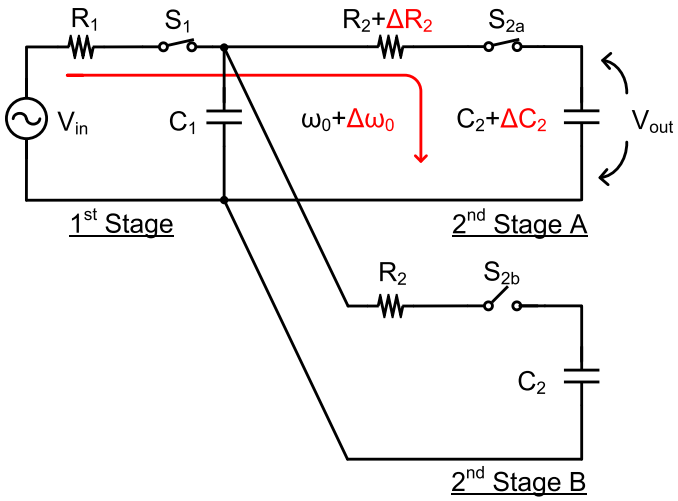

Fig. 5. Bandwidth mismatch of the sampling network with non-attenuated passive residue transfer.

the mismatch of the transfer switches, so the latter dominates the bandwidth mismatch here, which in turn brings about the gain and timing mismatch problems to the sampling network. For a broadband ADC, the error resulting from the timing mismatch is proportional to the input frequency and is usually much larger than the error caused by the gain mismatch at high frequencies. Therefore, the following analysis only focuses on the timing mismatch due to the mismatch between the two transfer switches.

The transfer function of the sampling network in Fig. 5 can be derived as

$$H(s) = \frac{1+sR_2C_{\text{SER}}}{\left(\frac{s}{\omega_n}\right)^2 + \frac{s}{\omega_0} + 1} \tag{7}$$

where ω_n and ω_0 are

$$\omega_n = \frac{1}{\sqrt{R_1R_2C_1C_2}} \tag{8}$$

$$\omega_0 = \frac{1}{R_1C_1 + (R_1+R_2)C_2} \tag{9}$$

and C_{SER} is the capacitance in series

$$C_{\text{SER}} = \frac{C_1C_2}{C_1+C_2}. \tag{10}$$

The phase shift of the sampling network can be calculated and simplified to (for $\omega << \omega_0$, it can be observed that ω is also much smaller than ω_n)

$$\begin{aligned}\varphi(\omega) &= \arctan\omega R_2C_{\text{SER}} - \arctan\frac{\omega/\omega_0}{1-(\omega/\omega_n)^2} \\ &\approx \arctan\omega R_2C_{\text{SER}} - \arctan\frac{\omega}{\omega_0}.\end{aligned} \tag{11}$$

The relative phase shift stemming from the on-resistance mismatch (ΔR_2) between the two transfer switches is

$$\begin{aligned}\Delta\varphi(\omega) &\approx \left[\frac{\omega C_{\text{SER}}}{1+\omega^2R_2^2C_{\text{SER}}^2} - \frac{\omega C_2}{1+(\omega/\omega_0)^2}\right]\Delta R_2 \\ &\approx \left(\frac{\omega C_{\text{SER}}}{1+\omega^2R_2^2C_{\text{SER}}^2} - \omega C_2\right)\Delta R_2.\end{aligned} \tag{12}$$

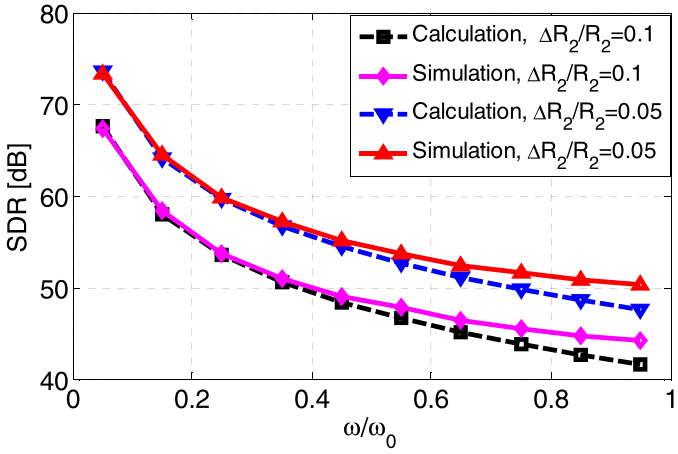

Fig. 6. Simulated SDR and the SDR calculated from (14).

So the corresponding timing mismatch can be expressed as

$$\Delta t(\omega) \approx \left(\frac{C_{\text{SER}}}{1+\omega^2 R_2^2 C_{\text{SER}}^2} - C_2\right)\Delta R_2 \approx -C_2\left(1 - \frac{1}{\left(1+\frac{C_2}{C_1}\right)\left[1+\omega^2 R_2^2\left(\frac{C_1 C_2}{C_1+C_2}\right)^2\right]}\right)\Delta R_2. \quad (13)$$

For a sinusoidal input signal the signal-to-distortion ratio (SDR) due to the timing mismatch can be expressed as [14]

$$\text{SDR} = -20\log\omega\Delta t(\omega) \approx -20\log\left[\omega\left(\frac{R_2 C_{\text{SER}}}{1+\omega^2 R_2^2 C_{\text{SER}}^2} - R_2 C_2\right)\frac{\Delta R_2}{R_2}\right]. \quad (14)$$

In order to verify the aforementioned analysis, the SDRs calculated from (14) and acquired from circuit simulations are plotted in Fig. 6 for contrast. It can be seen that the model matches the circuit simulation results with less than 1-dB deviation as ω/ω_0 approaches 0.5. In (13), it is interesting to note that the timing mismatch $\Delta t(\omega)$ is reduced with a decreasing value of C_2 or R_2. An intuitive way to understand this is that for a small C_2 or R_2 the common first stage (R_1 and C_1) effectively constitutes a relatively large portion of the time constant of the sampling network [see (9)], resulting in a small bandwidth sensitivity on the on-resistance mismatch. As we discussed in the last section, C_2 determinates the kT/C noise and it cannot be too small. In the prototype design, the transfer switches are bootstrapped for a small on-resistance, which guarantees a sufficient SDR for an 8-bit ADC according to (14).

IV. Prototype ADC Design

A. 2b–1b/Cycle Conversion Scheme

The architecture of the prototype ADC with non-attenuated passive residue transfer is illustrated in Fig. 7. To further enhance the conversion speed, a 2b/cycle conversion scheme is utilized in the first stage. In the prototype design, comparator offsets are calibrated in a foreground manner to remove their impact on the overall conversion accuracy. The 2b/cycle scheme requires two DACs, i.e., an SIG-DAC and a REF-DAC, to implement the 2 bit quantization per cycle. Without doubt, this setup introduces a potential mismatch issue between the two DACs. In Fig. 7, the SIG-DAC is loaded with four comparators whereas the REF-DAC is only connected to two comparators. The input parasitic capacitance of the comparators causes a systematic gain mismatch between the SIG-DAC and the REF-DAC. Hence, two dummy comparators (not shown in Fig. 7) are connected to the output node of the REF-DAC to avoid the systematic mismatch. The random mismatch between the capacitors in SIG-DAC and REF-DAC is normally bounded by 1% (causing a 0.16-LSB error on the residue) [18]. Therefore, the interstage redundancy with a value of ±4 LSBs can tolerate this error induced by any small random mismatch between the two DACs.

From the speed standpoint, making both the first and second stages 2b/cycle will probably deliver the highest conversion speed. However, due to the lack of residue amplification, the LSB size of the second stage is much smaller than that of the first stage. The comparator offsets and the mismatch between the SIG-DAC and the REF-DAC will make it difficult for the second stage to achieve the desired resolution. As an alternative, a 1b/cycle conversion scheme is applied to the second stage in this paper, in which the single comparator offset does not bring about any differential nonlinearity (DNL) errors but merely an input-referred offset.

Besides the conversion scheme, the resolution partition between the 2b/cycle first stage and 1b/cycle second stage also affects the overall throughput significantly. Considering that a 1b redundancy is needed to absorb the decision error in the first stage and the kickback noise of the second-stage comparator, there are two options for this partition: 1) 3 × 2b for the first stage and 3 × 1b for the second and 2) 2 × 2b for the first and 5 × 1b for the second. While option 1) appears to be more balanced (i.e., resolving 3 cycles for each stage), the 2b/cycle operation consumes more time than the 1b/cycle counterpart because of the increased logic complexity; and besides some additional time needs to be allocated to the first stage for sampling. Thus, the first stage becomes the speed bottleneck and some conversion time of the second stage is wasted, as Fig. 8 illustrates. Circuit simulation reveals that the maximum throughput for this option is limited to 1 GS/s.

The prototype ADC is realized with option 2), in which the first stage resolves 4 bits and the remaining 5 bits are assigned to the second stage. The second stage becomes the speed bottleneck in this scenario. Fortunately, the asynchronous time allocation enables time borrowing and somewhat relieves the timing burden of the second stage. This is depicted in Fig. 9, wherein once the last cycle of the first stage completes, the residue transfer is triggered and the second stage starts conversion immediately after that. Typically, the two conversion cycles of the first stage complete before the next sampling edge arrives, thus the rest of the time can be lent to the second stage. Unlike the first option, there is no conversion time wasted in this case. According to simulation, the ADC can be clocked maximally at 1.3 GS/s, which is significantly improved relative to the first option.

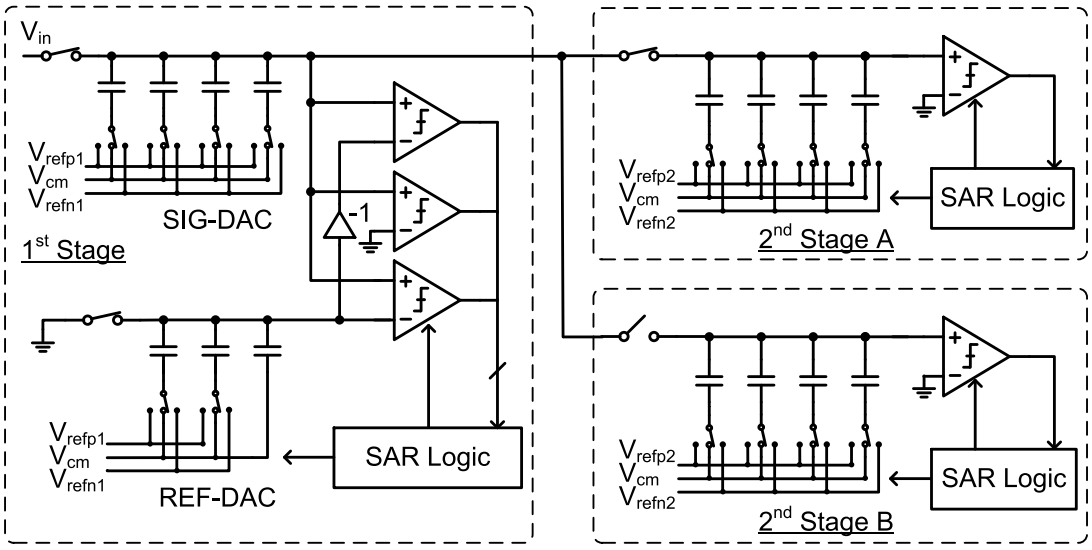

Fig. 7. Architecture of the 2b–1b/cycle two-step SAR ADC with passive residue transfer (a single-ended version is shown for simplicity).

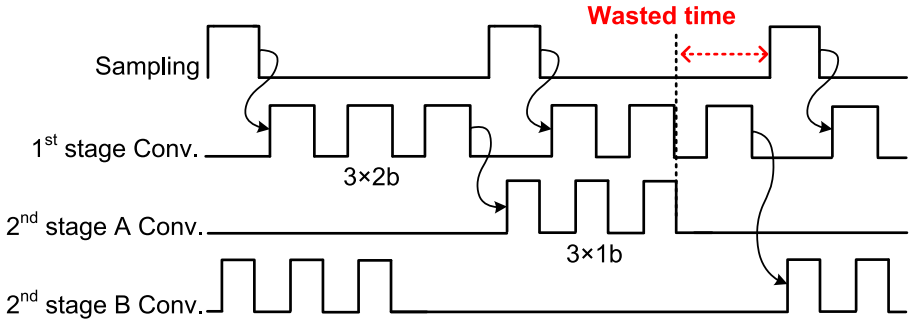

Fig. 8. Timing diagram of the first resolution partition: 3 × 2b for the first stage and 3 × 1b for the second stage.

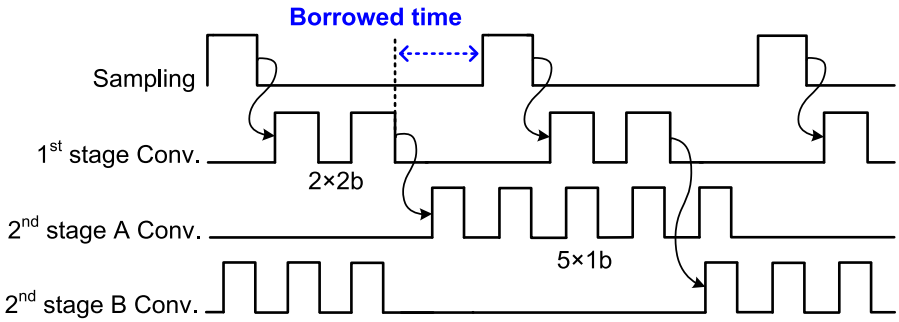

Fig. 9. Timing diagram of the second resolution partition: 2 × 2b for the first stage and 5 × 1b for the second stage.

B. Capacitive DACs

The schematic of the capacitive DACs is depicted in Fig. 10. As mentioned in Section II, the total capacitance of the second-stage DAC is chosen to be 15.5 fF for the sake of kT/C noise. Because of this small capacitance, the DAC becomes vulnerable to the kickback noise of the second-stage comparator. The kickback noise is injected into the DAC output only when the comparator is activated and the impact disappears once the comparator is reset, implying that the effect is memory-less (i.e., confined to the current bit cycle only) and can be considered as a form of DAC incomplete settling error. Therefore, the second-stage DAC employs a non-binary structure with an LSB capacitor of 1.5 C to tolerate the kickback noise [15], [16] (maximally tolerating ±1.5-mV differential kickback noise). Owing to the absence of residue gain, the quantization range of the second stage needs to be scaled down to roughly align with the residue voltage range. A large scaling capacitor could be added in the second-stage DAC to downscale the reference voltage [6], which unfortunately enlarges the input capacitive loading dramatically. In this design, a second reference V_{ref2}

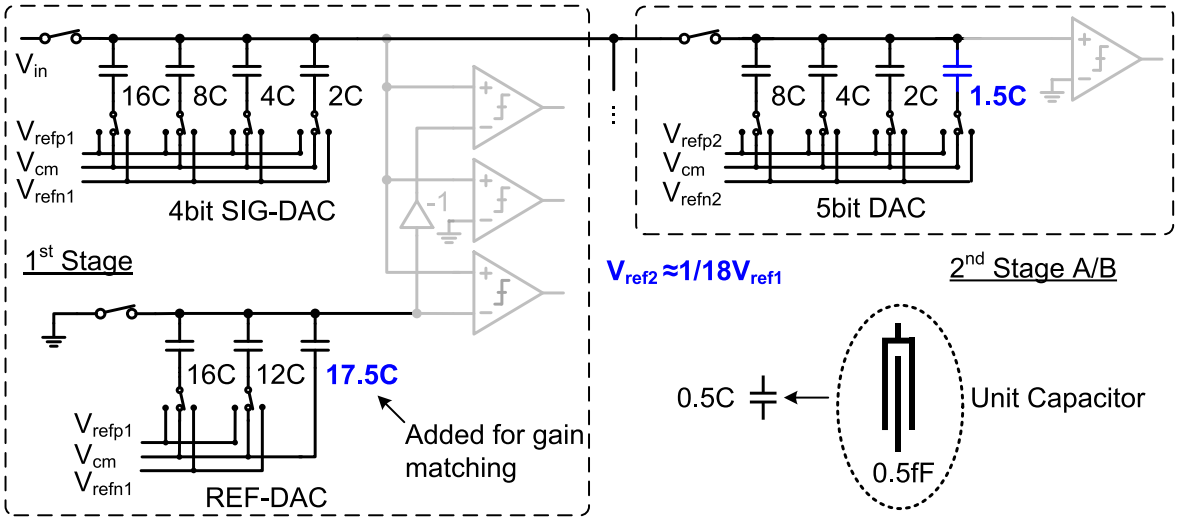

Fig. 10. Schematic of capacitive DACs in the prototype ADC.

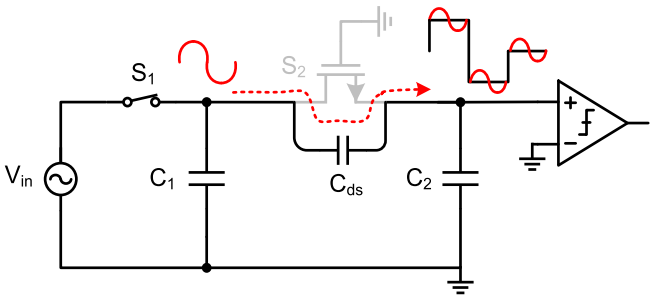

Fig. 11. Signal feed-through caused by the drain–source capacitance of the transfer switch.

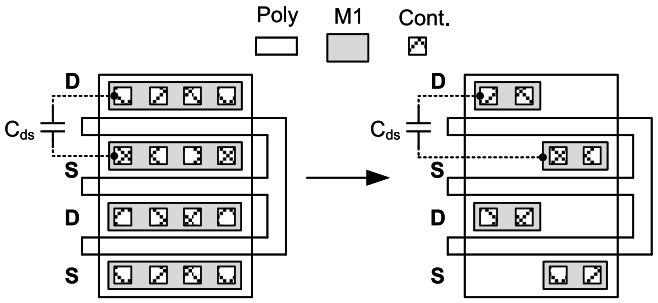

Fig. 12. Layout of transfer switch with small drain–source capacitance.

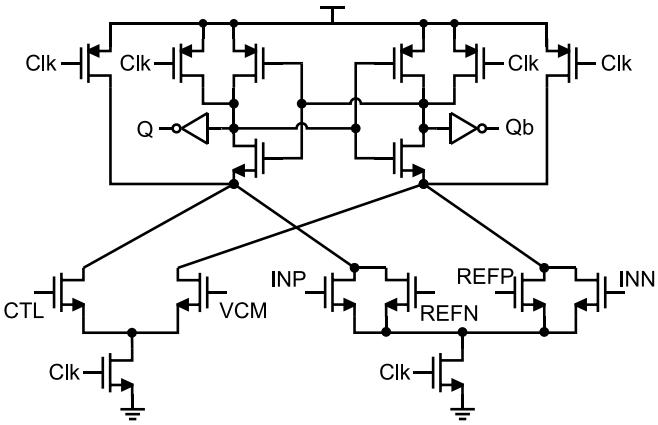

Fig. 13. Dynamic comparator with an extra input pair for offset calibration.

is applied to the second stage, obviating the large input loading issue. The calibrated reference V_{ref2} is chosen to be about $1/18V_{ref1}$, which introduces a redundancy of about ± 4 LSBs (± 15 mV) to tolerate the error resulting from any random mismatch between the SIG-DAC and the REF-DAC and any potential DAC settling errors during the coarse cycles.

Since the reference level of the first-stage SIG-DAC is attenuated by the second-stage DAC, it is desirable to choose a large ratio for the DAC sizes between the first and second stages. On the flip side, however, considering the input loading and the performance of the S/H, the capacitance of the first-stage DAC should not be too large. In this paper, this capacitance is chosen to be twice as large as the second-stage DAC, resulting in a reference attenuation factor of 2/3. To obtain a nominally identical attenuation factor as that of the SIG-DAC, a scaling capacitor of 17.5 C is added to the REF-DAC.

The unit capacitors in the DACs are realized with fringing metal capacitors of 0.5 fF [17]. The LSB capacitor has a capacitance of 1.5 fF and it is supposed to achieve good matching for an 8-bit ADC [18]. In the prototype, we also exploited the fact that the DACs of the two stages are independent to minimize the capacitance spread, which is 8 (16C/2C) instead of 64 given an overall 8-bit resolution [7]. This small capacitance spread not only leads to a small input capacitive loading of 45.5 fF, but also reduces the overall area of the DACs significantly.

C. Transfer Switch

As analyzed earlier, the smaller the on-resistance of the transfer switch, the better the bandwidth matching becomes. Moreover, because the second-stage DAC participates in the coarse conversion via the transfer switch, it is preferred to

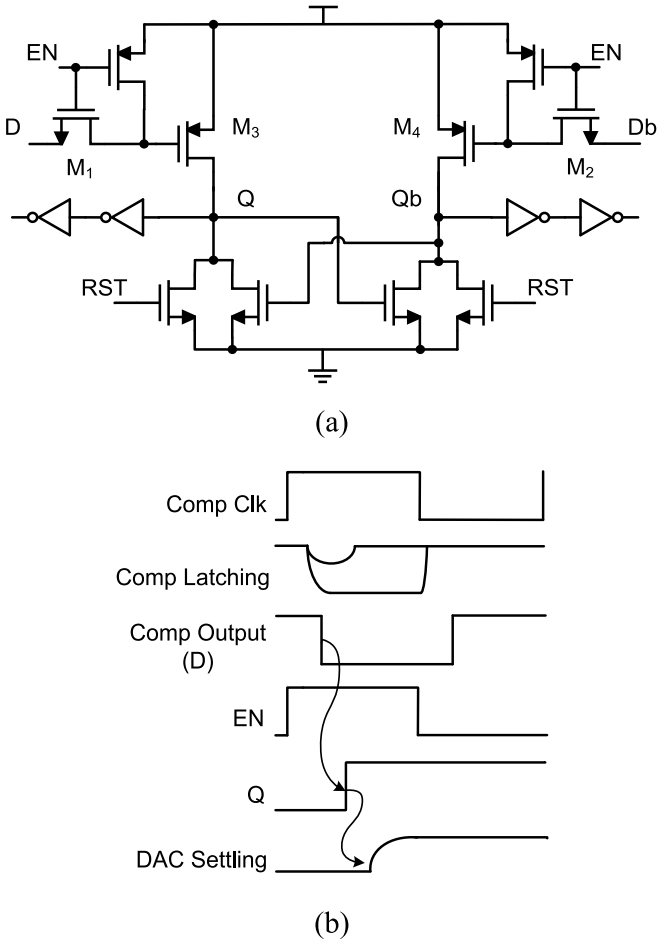

Fig. 14. (a) Schematic of the dynamic register. (b) Timing diagram of the dynamic register.

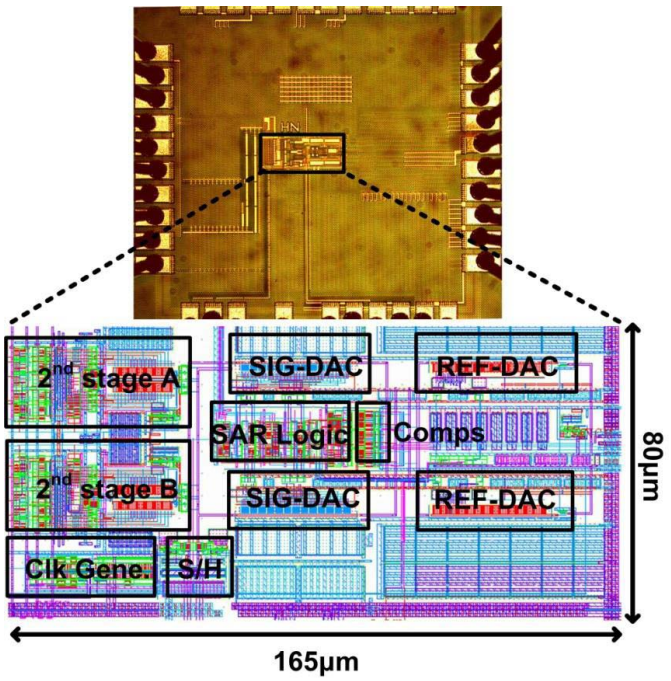

Fig. 15. Die photograph.

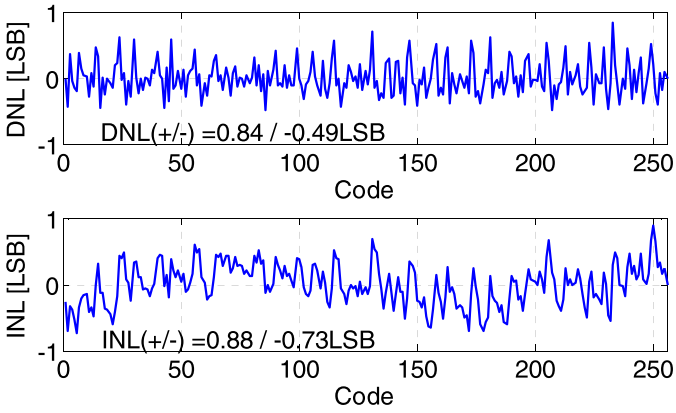

Fig. 16. Measured DNL and INL profiles.

lower its on-resistance to reduce the impact on the DAC settling accuracy. Therefore, in the prototype design, boot-strapped switches with a reasonably large size are utilized to lower the on-resistance. In addition, the interstage redundancy can partly alleviate DAC settling errors during the coarse cycles due to the impact of the transfer switch.

Another potential issue related to the transfer switch is the signal feed-through. As illustrated in Fig. 11, when the transfer switch is off, the signal on the summing node of the first-stage DAC will couple to the summing node of the second stage through the C_{ds} of the transfer transistor. This interference can potentially cause dynamic offsets for the second stage and degrade its conversion accuracy. T-switch is one option for isolating the off-switch coupling, but it exhibits a large on-resistance due to the series connection of transistors. Dummy switch that cross-connect the summing nodes of the first stage and the second stage are added to cancel the signal feed-through error [19]. Naturally, the effect of the feed-through compensation depends highly on the matching between the dummy switch and the transfer switch and it is not guaranteed over manufacturing variations. To further mitigate the feed-through problem, some source and drain contacts in the layout of the transfer switch and dummy switch are removed (as shown in Fig. 12), resulting in a more than 10 × reduction of C_{ds} [20]. Additionally, one can also add ground shields over the source and drain regions without contacts to achieve a more than 30 × reduction [21].

D. Comparator

The strong-arm latch in Fig. 13, which exhibits a high regeneration speed and consumes only dynamic power, is used as the comparators in this paper. An extra differential pair is introduced to facilitate the foreground offset calibration. To reduce the impact of the calibration pair on the speed and noise performance of the comparator, its size is set to a quarter of the main input pair. Since the comparator decision time constitutes a critical part of the SAR loop delay, its input common-mode voltage is set to 800 mV to boost the regeneration speed [22]. The input-referred noise power of the comparator in the second stage is designed to be half

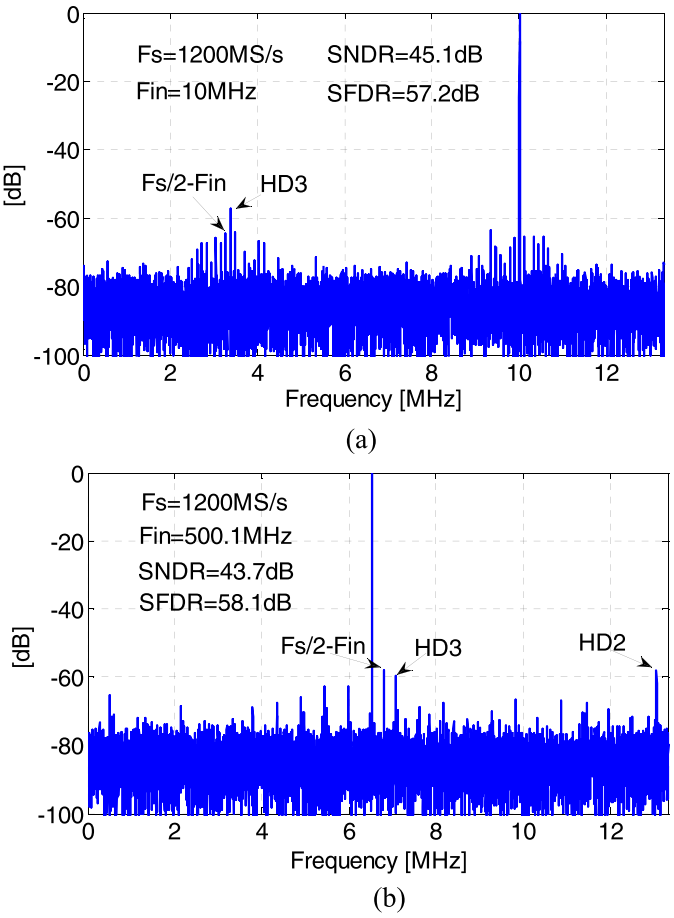

Fig. 17. Measured ADC spectra at 1.2 GS/s with (a) a near-DC input and (b) a near-Nyquist input (both decimated by 45×).

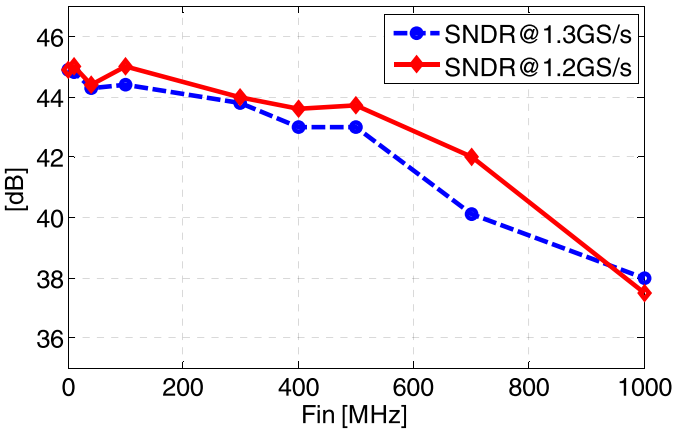

Fig. 18. Measured SNDR at 1.3 and 1.2 GS/s versus input frequency.

of the quantization noise power. So, the comparator noise and the kT/C noise together lead to an SNR degradation of 3 dB to the overall ADC.

E. Dynamic register

To implement the successive approximation operation, a set of registers are required to store the comparator outputs and feed the comparator decisions back to the capacitive DAC as quickly as possible. The delay from the comparator output to the DAC switches is also a critical part of the SAR loop delay. In this design, the dynamic register in Fig. 14 (modified from [4] and [23]) is adopted to minimize this delay. Unlike the conventional D-flip-flop, this dynamic register is directly triggered by the comparator output (i.e., level sensitive) instead of by an additional latching clock, so the extra delay from the comparator output to the latching clock is removed. Furthermore, in each bit cycle only one dynamic register is enabled (EN = 1) and connected to the comparator through M_1 and M_2, leading to a small capacitive loading to the comparator. When the dynamic register completes regeneration, it will be disconnected from the comparator (EN = 0) and the gates of M_3 and M_4 will be pulled up to V_{DD}, making the register insensitive to the interference from the comparator output.

TABLE I
POWER CONSUMPTION BREAKDOWN

Sample Rate @ Supply	1.2 GS/s @ 1.25 V	1.3 GS/s @ 1.3 V
Analog Circuits	2.3 mW (46%)	2.71 mW (47%)
Digital Circuits	2.42 mW (48%)	2.8 mW (48%)
DAC Reference	0.28 mW (6%)	0.29 mW (5%)
Total	5 mW	5.8 mW

TABLE II
PERFORMANCE SUMMARY

CMOS Tech. [nm]	65	
Resolution [bits]	8	
Supply Voltage [V]	1.25	1.3
Sample Rate[GS/s]	1.2	1.3
Power [mW]	5	5.8
Area [mm^2]	0.013	
DNL [LSBs]	+0.84/-0.49	
INL [LSBs]	+0.88/-0.73	
SNDR [dB] @fin=500MHz	43.7	43.1
SFDR [dB] @fin=500MHz	58.1	57.8
FoM [fJ/conv.step]	35	38

V. MEASUREMENT RESULTS

The prototype ADC was fabricated in a 65-nm CMOS process. A die photo is shown in Fig. 15. The ADC occupies an active area of 165 μm × 80 μm. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) profiles after comparator offset calibration are shown in Fig. 16. The maximum DNL and INL are +0.84/−0.49 LSBs and +0.88/−0.73 LSBs, respectively.

The dynamic performance of the ADC after static radix calibration (including interstage gain calibration) and ping-pong gain mismatch calibration is shown in Fig. 17; the

TABLE III
PERFORMANCE COMPARISON

Works	JSSC'15 Yoshioka [24]	VLSI'12 Chan [25]	VLSI'12 Lien [26]	JSSC'15 Hong [4]	JSSC'13 Kull [7]	This work	
Architecture	Subrange, TI	2b/cycle SAR,TI	2b/cycle SAR	2b/cycle SAR	SAR	Two-step SAR	
CMOS Tech.[nm]	65	65	28	45	32 SOI	65	
Resolution[bits]	7	8	8	7	8	8	
Sample Rate[GS/s]	1.23	1	0.75	1	1.2	1.2	
Power [mW]	8.11	4	4.5	7.2	3.1	5.0	
Area [mm^2]	0.0875	0.013	0.004	0.016	0.0015	0.013	
SNDR [dB]	36.2	42.8	43.2	40.8	39.3	43.7	42.5†
SFDR [dB]	46.2	58.5	57.5	50.6	50	58.1	56.8†
FoM [fJ/conv.step]	125	34	41	80	34	35	39†

† Measured with only offset calibration

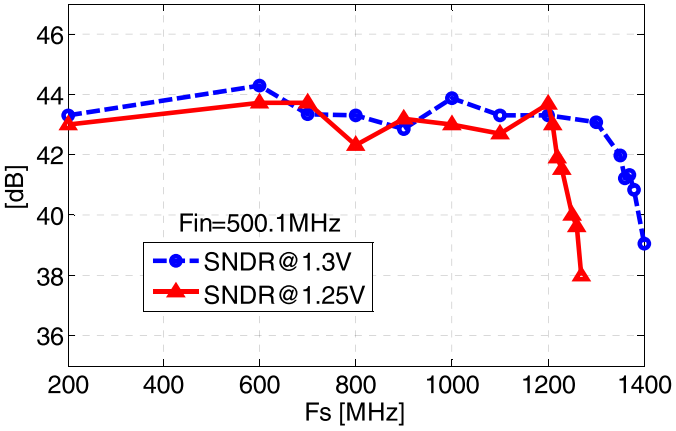

Fig. 19. Measured SNDR at 1.3 and 1.25 V supplies versus sampling frequency.

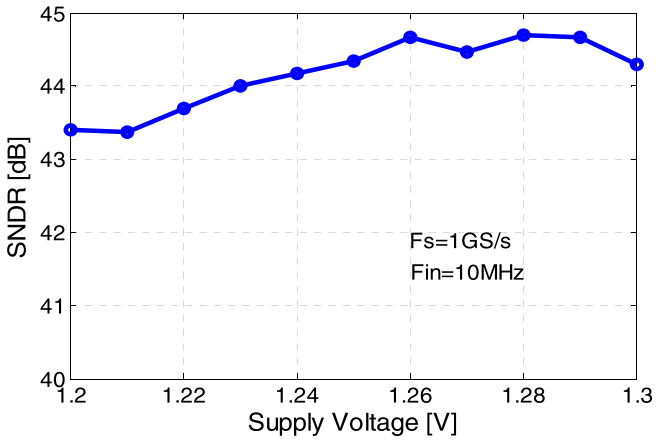

Fig. 20. Measured SNDR versus supply voltage.

achieved SNDR is 45.1 dB and the SFDR is 57.2 dB for a 10-MHz input. For a 500.1-MHz input, the measured SNDR is 43.7 dB and the SFDR is 58.1 dB (42.5 dB and 56.8 dB with only offset calibration, respectively). The spurious tone produced by bandwidth mismatch limits the SFDR when the input frequency approaches the Nyquist value, at which the second harmonic also pops up, most likely induced by the phase imbalance between the differential input traces. Fig. 18 summarizes the measured SNDR for various input frequencies at 1.25-V and 1.3-V supply voltages. The effective resolution bandwidth of the ADC is larger than 600 MHz and the effective number of bits remains above 6 bits with even a 1-GHz input. Fig. 19 plots the measured SNDR with a 500.1-MHz input at 1.25-V and 1.3-V power supplies versus the sampling frequency. The SNDR fluctuation is suspected to be caused by the input signal coupling through the C_{ds} of the sampling switch. Limited by the comparator speed, the SNDR starts to drop rapidly around 1.2- and 1.3-GS/s sample rates. During the test, the power supply voltage and the temperature were also swept to check the robustness of this design. When the supply voltage varies from 1.2 to 1.3 V, the measured SNDR fluctuates by 1.3 dB (see Fig. 20). Fig. 21 shows the temperature dependence of the measured SNDR. The SNDR variation between 5° and 95° is around 0.8 dB. The small SNDR fluctuations demonstrated in Figs. 20 and 21 also prove that the advocated non-attenuated passive residue transfer has a stable gain response over supply voltage and temperature variations.

Table I presents the breakdown of the power consumption. 46% of the power (2.3 mW) is consumed by the comparators and the bootstrapped circuits while 48% (2.42 mW) is spent on the clock generator and the SAR logic. The power consumption of the DAC references only takes 6% of the total (0.28 mW). Table II summarizes the performance of the prototype ADC at 1.25-V and 1.3-V power supplies. Clocked at 1.2 GS/s, the ADC achieves an SNDR of 43.7 dB and consumes a total power of 5 mW, culminating in a conversion FoM of 35 fJ/conversion-step.

Table III compares this work to some state-of-the-art designs reported recently. Thanks to the passive residue transfer and

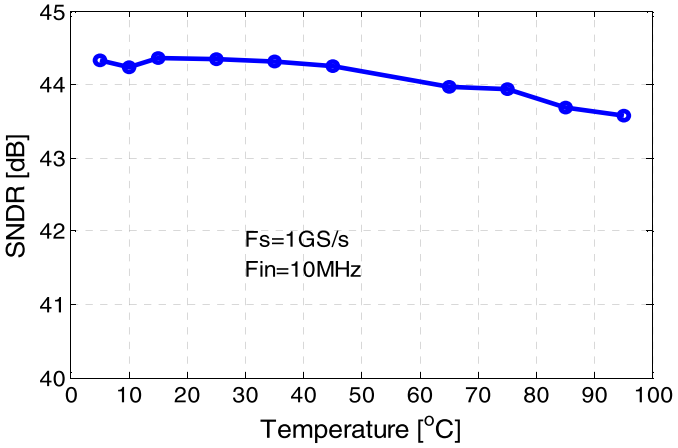

Fig. 21. Measured SNDR versus ambient temperature.

the 2b–1b/cycle conversion scheme, this paper achieves the highest conversion speed among the high-speed SAR ADCs published recently. One point should be noted is that even with a 65-nm bulk process the prototype ADC still achieves a comparable speed to another design fabricated in a 32-nm SOI process. As illustrated in the table, this paper also attains a very similar SNDR and power efficiency as the best counterpart designs.

VI. Conclusion

A 1.2 GS/s, 8-bit two-step SAR ADC based on passive residue transfer and a 2b–1b/cycle conversion scheme has been reported in this paper. Attributing to the passive residue transfer, the time and power consumption associated with residue production are mostly removed and the SAR ADC can further improve its throughput, manifested by the comparison with recently reported high-speed SAR ADCs of similar resolutions. The kT/C noise of this technique and its bandwidth-mismatch issue are analyzed and verified by circuit simulations. Meanwhile, a 2b–1b/cycle conversion scheme with a proper resolution partition is employed to further enhance the conversion speed. Fabricated in a 65-nm CMOS process, the prototype ADC achieves an SNDR of 43.7 dB and an FoM of 35 fJ/conversion-step at a sample rate of 1.2 GS/s with a near-Nyquist frequency input.

Acknowledgment

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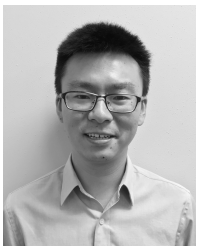


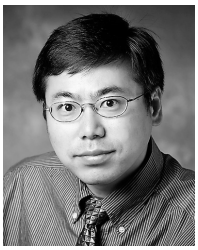
Hai Huang (S'16) received the B.S. and M.Sc. degrees in electrical engineering from the University of Electronic Science and Technology of China, Chengdu, China, in 2010 and 2013, respectively. He has been pursuing the Ph.D. degree with the University of Texas at Dallas, Richardson, TX, USA, since 2013.

His current research interests include data converters and emerging low-power amplifiers.

Mr. Huang received the first prize of the National Undergraduate Electronic Design Contest in Sichuan Section in 2009. He was also a recipient of the Analog Devices Outstanding Student Designer Award in 2014.

Ling Du received the Ph.D. degree in microelectronics and solid-state electronics from the University of Electronic Science and Technology of China, Chengdu, China, in 2016.

He was a Visiting Student at the University of Texas at Dallas, Richardson, TX, USA, from 2014 to 2015. He is currently with Chengdu MECS Microelectronics Technology Co., Ltd, Chengdu, China. His current research interests include the design of high-speed high-resolution analog-to-digital converters (ADCs), especially SAR ADC, pipelined ADC, and hybrid ADC.



Yun Chiu (S'97–M'04–SM'10) received the B.S. degree in physics from the University of Science and Technology of China, Hefei, China, the M.S. degree in electrical engineering from the University of California, Los Angeles, CA, USA, and the Ph.D. degree in electrical engineering and computer sciences from the University of California, Berkeley, CA, USA.

He was a Senior Staff Member of Cond or Vision Technology Inc., Los Angeles, CA, USA, from 1997 to 1999, in charge of developing analog and mixed-mode circuits for CMOS digital imaging products. From 1999 to 2004, he was with the Berkeley Wireless Research Center, University of California, Berkeley, where he worked on low-power and low-voltage CMOS data converters. In 2004, he joined the Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Champaign, IL, USA, as an Assistant Professor, where he received the tenure offer in 2010. He is currently a Full Professor and the Erik Jonsson Distinguished Professor with the Department of Electrical Engineering, University of Texas at Dallas, Richardson, TX, USA, where he also the Director of the Analog and Mixed-Signal Laboratory of the Texas Analog Center of Excellence.

Dr. Chiu was a recipient of the Foreign Scholar Award at UCLA, the Regents' Fellowship, the Intel Foundation Fellowship, the Cal View Teaching Fellow Award at Berkeley, and two awards from the Ministry of Education of China. He was also a co-recipient of the Jack Kilby Outstanding Student Paper Award from the 2004 International Solid-State Circuits Conference, the 46th ISSCC/DAC Student Design Contest Award in 2009, and the Best Regular Paper Award from the 2012 Custom Integrated Circuits Conference (CICC). He was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS from 2007 to 2009, and serves on the technical program committees of several IEEE solid-state circuits conferences including the CICC, the Asian Solid-State Circuits Conference, and the Symposium on Very Large Scale Integration Circuits.