

In Vitro Multi-Functional Microelectrode Array Featuring 59 760 Electrodes, 2048 Electrophysiology Channels, Stimulation, Impedance Measurement, and Neurotransmitter Detection Channels

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Abstract—Biological cells are characterized by highly complex phenomena and processes that are, to a great extent, interdependent. To gain detailed insights, devices designed to study cellular phenomena need to enable tracking and manipulation of multiple cell parameters in parallel; they have to provide high signal quality and high-spatiotemporal resolution. To this end, we have developed a CMOS-based microelectrode array system for in vitro applications that integrates six measurement and stimulation functions, the largest number to date. Moreover, the system features the largest active electrode array area to date ($4.48 \times 2.43 \text{ mm}^2$) to accommodate 59 760 electrodes, while its power consumption, noise characteristics, and spatial resolution (13.5- μm electrode pitch) are comparable to the best state-of-the-art devices. The system includes: 2048 action potential (AP, bandwidth: 300 Hz–10 kHz) recording units, 32 local-field-potential (LFP, bandwidth: 1 Hz–300 Hz) recording units, 32 current recording units, 32 impedance measurement units, and 28 neurotransmitter detection units, in addition to the 16 dual-mode voltage-only or current/voltage-controlled stimulation units. The electrode array architecture is based on a switch matrix, which allows for connecting any measurement/stimulation unit to any electrode in the array and for performing different measurement/stimulation functions in parallel.

Index Terms—Extracellular recording and stimulation, high channel count, high-density microelectrode array (HD-MEA), impedance spectroscopy, low noise, low power, multi-functionality, neural interface, neurotransmitter detection, pre-charging, pseudo-resistor, switch matrix.

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I. INTRODUCTION

LECTROGENIC cells, such as neuronal, cardiac, and pancreatic cells are capable of generating and transmitting electrical signals. The flow of ions through the cell membrane generates changes in electrical potentials that can be measured using standard electronic circuitry. Apart from electrical signals, cells also use chemical compounds for signaling, as it is the case in neuronal synapses (contacts between neuronal cells). The chemicals that transmit signals across the synaptic cleft, so-called neurotransmitters, play a significant role in brain diseases, such as schizophrenia, Alzheimer’s, and Parkinson’s disease [1]; electrochemical methods, such as cyclic voltammetry are commonly used to detect their presence [2]–[4]. To study cell network dynamics, a bidirectional interaction, which also includes electrical stimulation of cells, is desired. To ensure precise and selective stimulation of individual neurons, characterization of the electrodes [5], the cell-electrode attachment, and the cell morphology [6] is first performed, typically by means of impedance spectroscopy [7]. This method can also be used for investigation of anisotropic and inhomogeneous electrical conductivity of tissue and culture medium, label-free detection of cancer [8], [9] and studies of neurodegenerative diseases [10]. Simultaneous examination of electrical and chemical cell signaling noninvasively over extended periods of time, performing targeted electrical stimulation, and tracking cellular movements or changes in the electrical interface via changes of impedance, will provide valuable insights in the behavior of individual cells and cell ensembles and help diagnose and treat different disorders.

Microelectrode arrays (MEAs) are well-established platforms for *in vitro*, extracellular investigation of electrogenic cells that feature multiple electrodes for parallel electrical recording and stimulation [11]–[21]. They are widely used for investigations of cell cultures and cell tissues, such as organotypic brain slices and retinae [14], [15]. Various MEA systems have been developed to date, featuring different substrates, numbers of electrodes, and electrode pitches [22]. Owing to the small feature size of CMOS technology, recent CMOS-based MEA systems comprise thousands of electrodes at pitches of tens of micrometer, down to a few micrometer [17]–[21], which is crucial to obtain detailed

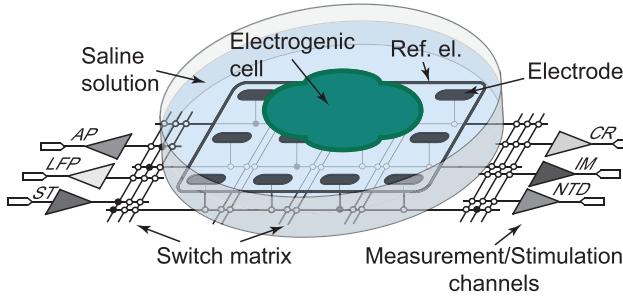


Fig. 1. Illustration of the multi-functional, switch-matrix-based HD-MEA system featuring action potential (AP) readout, local field potential (LFP) readout, current readout (CR), impedance measurement (IM), neurotransmitter detection (NTD) and stimulation (ST) channels

insights into cellular and sub-cellular phenomena [23]. The two most common CMOS-MEA architectures base either on the in-pixel front-end amplifiers [18]–[20], or on the switch matrix [17], [21], where the amplifiers reside outside of the electrode array and are connected to the electrodes via a programmable matrix of switches. Both approaches have been detailed and compared in [22].

Contemporary MEAs feature up to three different types of measurement/stimulation functions. The high-density (HD) MEAs in [17]–[21] feature only voltage recording and/or voltage/current stimulation; they are limited either in the noise performance [18]–[20], spatial resolution [19], or number of readout channels [17]–[21]. The systems in [2]–[4] and [6] feature a combination of neurotransmitter, impedance, and/or electrophysiology measurement functions, however, they have a very low number of channels, low-spatial resolution and no stimulation capabilities.

In this paper, we present a HD-MEA system that allows performing multiple measurement/stimulation functions in parallel (Fig. 1). The implemented switch-matrix approach [17], [21] allows connecting any electrode to any of the measurement/stimulation channels. Moreover, the system significantly advances some of the characteristic MEA features.

This paper is organized as follows. The system architecture, its functional units, and their integration into a single system are described in Sections II–IV, the electrical and biological measurements are described in Sections V and VI, while Section VII gives a detailed comparison to the state-of-the-art and concludes the paper.

II. SYSTEM ARCHITECTURE

A list of the different functional units integrated in the system, as well as of the respective design requirements, is given in Table I. The number of measurement/stimulation channels is limited by the chip area and overall power consumption. The processes of neuronal cells can extend over a few hundred micrometer (Purkinje neurons) and more, hence, to explore functional connections in fairly distant regions of tissue slices (mm distance), we have opted for at least $4 \times 2 \text{ mm}^2$ of active electrode array area. The data sampling frequency of 20 kS/s has been chosen based on the frequency range of extracellular signals of different cells, including neuronal action potentials (APs), 300 Hz–10 kHz, neuronal

local field potentials (LFPs), 1–300 Hz, and cardiac APs, 1 Hz–1 kHz. To prevent cells heating by more than 2 °C, the targeted power consumption was below 100 mW.

The block diagram of the overall system is depicted in Fig. 2. The details on each of the functional units are given in the next section, with the exception of the current recording unit, which will not be covered here due to space limitations.

III. FUNCTIONAL UNITS

A. Electrode Array

The electrode array features 59 760 microelectrodes ($3 \times 7.5 \mu\text{m}^2$), distributed over 332×180 pixels, at a $13.5 \mu\text{m}$ pitch ($5487 \text{ electrodes/mm}^2$), covering an area of $4.48 \times 2.43 \text{ mm}^2$. The underlying electrode routing in the electrode array was switch-matrix-based [17], [21], and organized in pixels, whose block diagram is shown in Fig. 3. Each pixel contained four transmission gates with approximately 600Ω on-resistance, and three SRAM cells. The SRAM cells were used to set the state of three switches (SW0–SW2) that connected either the electrode to a signal wire, or pairs of wires. The fourth switch (SW3) was used to connect the electrode to a stimulation unit using a low-impedance routing path, which contained only two switches. The largest electrode block providing maximum spatial resolution consisted of 45×45 electrodes or pixels ($607.5 \times 607.5 \mu\text{m}^2$, 2025 pixels), containing four times more pixels and covering twice the area of the largest HD block in [21]. The more advanced features of this switch matrix came from the more advanced CMOS technology used ($0.18 \mu\text{m}$, instead of $0.35 \mu\text{m}$), and from the particular switch arrangement implemented.

The arrangement of the switches in the electrode array achieved a maximal routing flexibility, so that any electrode could be connected to any measurement/stimulation channel. Additionally, different electrodes can be simultaneously routed to different measurement/stimulation units, which enables conducting complex experiments, targeting different cell features in parallel. The array switch pattern also allows for locally connecting multiple electrodes (e.g., 4, 9, or 16 electrodes) to obtain a sensing area of rectangular shape and arbitrary size. These pseudo-large electrodes enable charge integration over a large area, which can be used in recording LFPs and may prove beneficial in neurotransmitter detection (NTD).

The physical layout of the array was generated using a custom C++ application that described the switch matrix as a mathematical graph. An electrode routing configuration was generated by means of Integer Linear Programming, where the routing was mapped into a max-flow, min-cost problem, similar to [17] and [21]. The reconfiguration of the entire array takes up to 4.5 ms.

B. Voltage Recording Channels

The 2048 AP recording channels were organized in 32 recording blocks [Fig. 4(a)]. Each block consisted of 64 AP channels, including 64 continuous-time (CT) first-stage and second-stage amplifiers, eight switched-capacitor (SC) third-stage amplifiers, one SC fourth-stage

TABLE I
OVERVIEW OF DESIGN REQUIREMENTS FOR DIFFERENT MEASUREMENT/STIMULATION UNITS

Function	Application	Spatial Resolution	Signal Level	Signal Frequency	Noise & Linearity	Number of Channels
AP Readout	Electrical: Action-potential recording	Sub-cellular ^{a, b}	Neuronal AP: <1 mV	Neuronal AP: 300 Hz-6 kHz	<5 $\mu\text{V}_{\text{RMS}}^{\text{c}}$	Thousands
LFP Readout	Electrical: Local-field potential recording	Few hundred μm^{d}	Neuronal LFP: <5 mV. Cardiac/pancreatic AP/LFP: tens of mV	Neuronal LFP: ~1 Hz - 300 Hz, Cardiac AP: ~1Hz-1 kHz	<10 μV_{RMS}	Few tens
Neurotransmitter Detection	Electrochem: Neurotransmitter detection	Sub-cellular/cellular ^a	nA - μA	~10 kHz for FSCV	<0.5 nA _{RMS}	Few tens
Impedance Meas.	Electrical/Electrochem: Cell-electrode interface characterization	Sub-cellular ^a	10 k Ω -10 G Ω	1 Hz-1 MHz	<1.0 pA _{RMS}	Few tens
Stimulation	Electrical: Evoking activity by applying voltage/current pulse	Sub-cellular ^a	Voltage: ±1.3 V Current: ±30 μA in low range, ±300 μA in high range ^e	10 kHz – 100 kHz for single electrode	>9 bit linearity	Few tens
Current Readout	Electrical: Current recording	Sub-cellular ^a	pA	-	<100 fA _{RMS}	Few tens

^a Cell diameters: few μm to few tens of μm .

^b To closely approach axons (weak signals, ~20 μV , [25]) and track cellular morphological changes (e.g., axonal initial segment [24]).

^c Level comparable to neuronal background activity and electroe noise (e.g., ~80 nV/ $\sqrt{\text{Hz}}$ at 1 kHz, for Pt electrodes of 25 μm diameter [28]). To reveal weak axonal signals [25].

^d LFPs spread up to 2-3 mm, measured *in vivo* in [26], [27]

^e [50], [51]

amplifier, and one successive-approximation-register (SAR) analog-to-digital converter (ADC). Inside each block, bias circuitry and digital control logic were shared among 16/64 channels. Weak extracellular signals were amplified by the four amplification stages, with a programmable gain from 29 to 77 dB (steps of 6 dB), after which they were sampled at 20 kS/s and digitized by the 10-bit 1.28-MS/s SAR ADC. To suppress interferences from power supplies and substrate, the whole signal chain of the AP recording channel featured fully differential structure.

As the noise performance of the signal chain was mostly determined by the first stage, about half of the total recording channel power (~8.6 μW) was allocated to this stage

to achieve a low noise level. To further reduce the noise, a resistively loaded open-loop amplifier topology has been adopted [28]–[30] [Fig. 4(b)]. Traditional CMOS neural amplifiers employ closed-loop topologies with high-gain operational transconductance amplifiers (OTAs) [31], which use pMOS input differential pairs and nMOS active loads. nMOS transistors normally have a much higher flicker noise level than pMOS transistors, and, thus, add substantial noise in the AP band. In contrast, the resistive loads do not generate flicker noise and contribute less thermal noise, if the voltage drop across the two types of loads is equal. Therefore, the proposed open-loop topology achieved a lower noise level (<3 μV_{RMS}) than traditional topologies with similar power consumption.

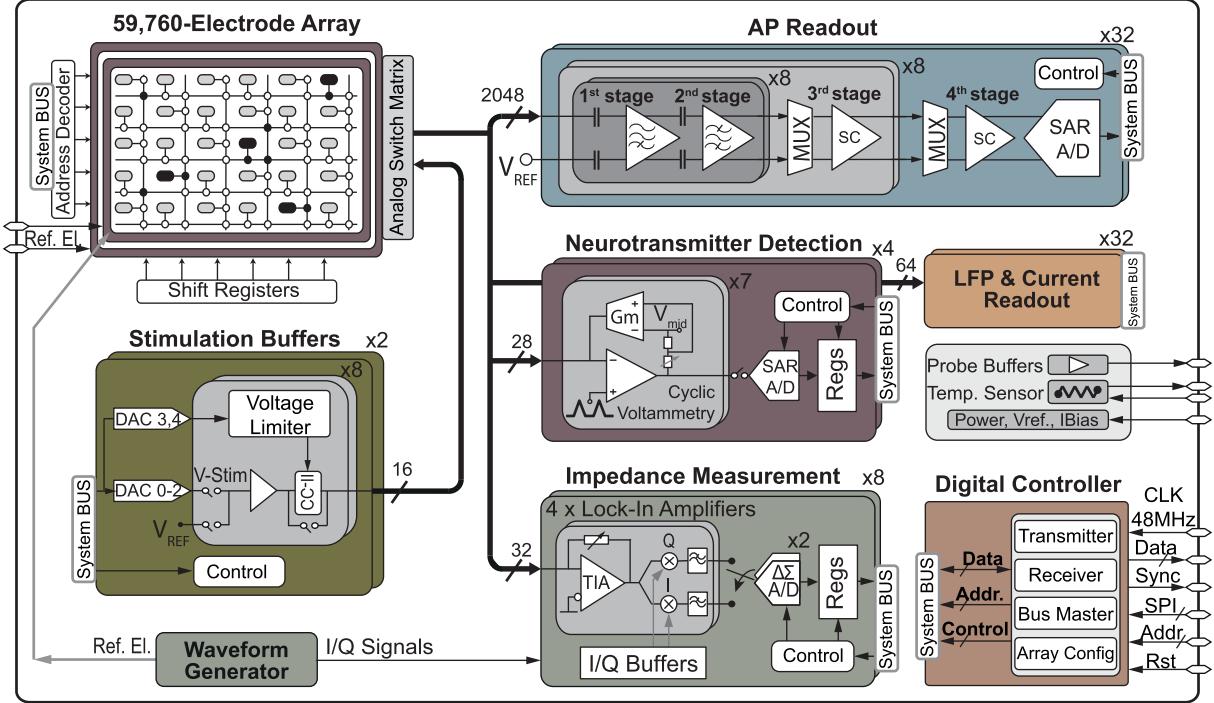
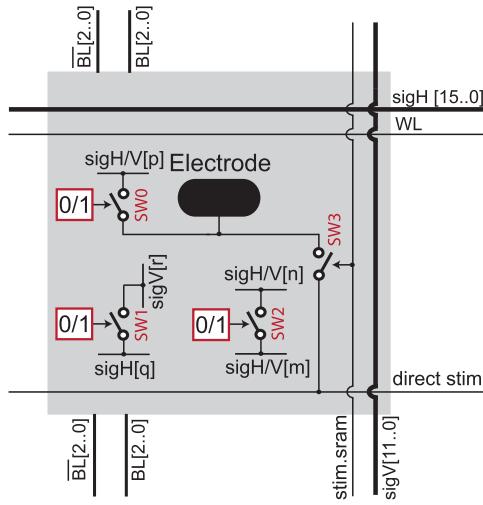


Fig. 2. Block diagram of the multi-functional MEA system.

Fig. 3. Block diagram of an array pixel. Switch SW0 connects the electrode to either a horizontal (sigH) or a vertical (sigV) wire. SW1 connects two intersecting wires, SW2 connects a pair of parallel wires. $m, n, p, q \in [0, 15]$, $r \in [0, 11]$.

However, one drawback of this topology is that its gain can vary significantly due to process and temperature (PT) variations. To keep such variations low, a constant- g_m biasing circuit was used to generate the tail current of the amplifier A_1 [Fig. 4(b)]. By matching the pMOS transistors (M_1 , M_2 , and M_4) and the resistors (R_{L1} , R_{L2} , and R_{B1}) in both A_1 and the biasing circuit, a uniform gain was achieved.

The second stage [Fig. 4(a)] employed a closed-loop structure, which provided an accurate gain of $A_{V2} = C_2/C_3$ (programmed by tuning C_2) and could handle a large swing.

Owing to the relaxed noise requirements, the g_m of its input transistors was reduced to cut power consumption, and thus less load capacitance was required to realize the anti-aliasing filtering. The load capacitor, C_4 , can be tuned to set the low-pass corner frequency to around 6 kHz.

In addition to achieving low noise, the two CT stages had to remove low-frequency (< 1 Hz) electrode potential drifts and control their offsets to avoid saturating succeeding amplifiers in large-gain configurations. Therefore, a high-pass filter (HPF, C_1 and R_{PR1}) has been implemented in front of the first stage to remove the electrode potential drifts, and the HPF (C_3 and R_{PR2}) in the second stage to null the first-stage offset. Due to the dc feedback through R_{PR2} , the offset of the amplifier A_2 was divided by A_{V2} when referred to the input of the second stage, and further divided by the first-stage gain when referred to the electrode.

Both HPFs had to have very low corner frequencies ($f_{HPF} < 10$ Hz) to avoid filtering out AP signals and adding excessive noise into the AP band. Nonetheless, C_1 and C_2 had to be around a few picofarad due to area constraints, and, thus, R_{PR1} and R_{PR2} had to be in the TΩ range. Such large resistances are usually realized with so-called “pseudo-resistors,” i.e., MOS transistors biased in the weak inversion region. However, in conventional structures, the transistor gates are biased with fixed voltages, so that the threshold voltage (V_T) may significantly vary due to PT variations, which yields a large spread in resistances. To guarantee a good uniformity of f_{HPF} , two pseudo-resistor structures have been devised [29], [30] [Fig. 4(c)]. R_{PR1} consisted of a pMOS (M_1) and an nMOS (M_2) transistor connected like a transmission gate. Their gates were biased by a pMOS and an nMOS current mirror, respectively. Hence, the first-order dependence of their

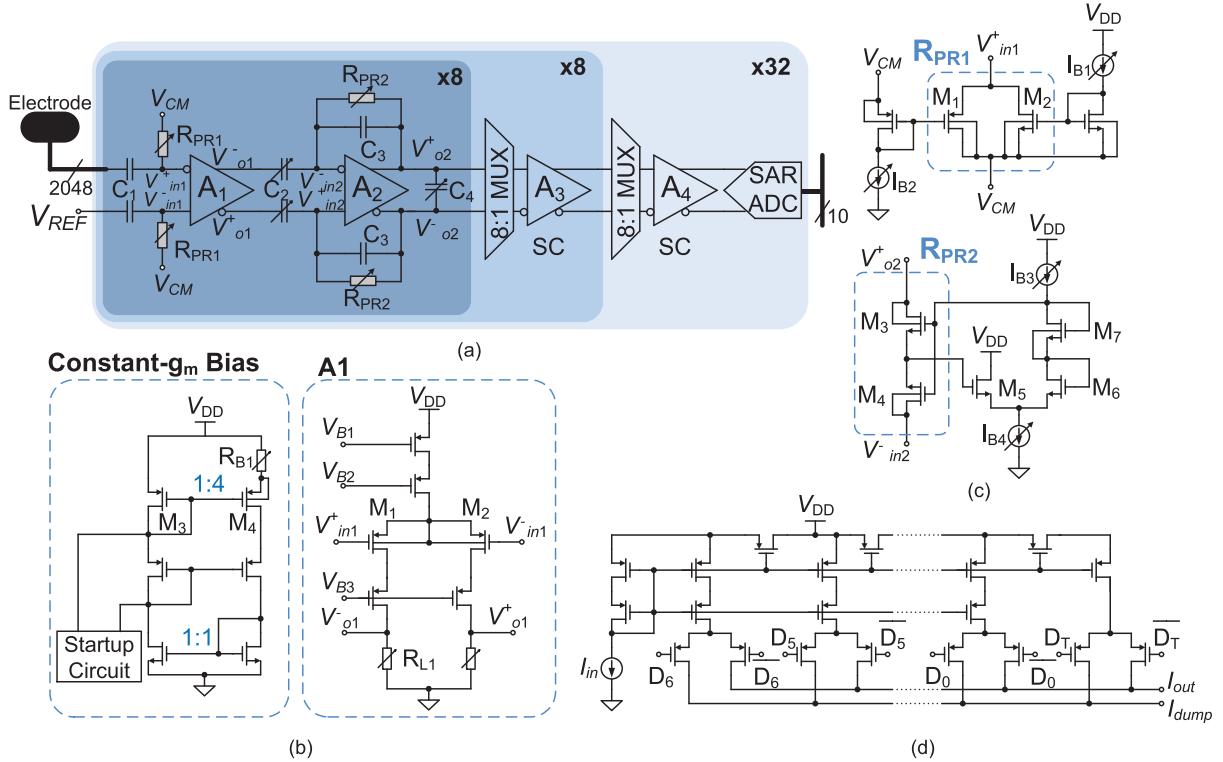


Fig. 4. AP recording channels. (a) Block diagram of the 2048 AP recording channels. (b) Open-loop amplifier (A_1) used in the first stage and its constant- g_m bias circuit. (c) Two types of pseudo-resistors and their bias circuits. (d) MOSFET-only R-2R current DAC for tuning high-pass corner frequencies.

overdrive voltages (V_{OV}) on V_T has been cancelled. For R_{PR2} a similar structure as in [32] was adopted, which consists of two nMOS transistors (M_3 and M_4) connected in series. Here, an nMOS-only level shifter (M_5 , M_6 , and M_7) was used to bias the gates of M_3 and M_4 , instead of a pMOS level shifter in [32], to obtain a better process tracking. V_{OV3} was approximately equal to $(V_{OV6} + V_{OV7} - V_{OV5}) + (V_{T6} + V_{T7} - V_{T5} - V_{T3})$, and had a weak dependence on V_T . Thus, resistance variations of both R_{PR1} and R_{PR2} were substantially smaller than those of the conventional structures. In addition, both R_{PR1} and R_{PR2} were designed symmetrically around their common-mode voltages, which entailed a good linearity. Furthermore, the two resistances were inversely proportional to the bias currents ($I_{B1} - I_{B4}$), which can be tuned to adjust f_{HPF} for compensating PT variations and to accommodate different experimental scenarios. This adjustability was realized by using two 7-bit current DACs [shared by 16 channels, Fig. 4(d)] for two stages. The DACs relied on the current-division principle of MOS transistors and were realized using a compact MOSFET-only R-2R ladder structure [33].

To reduce area and power consumed by the last two stages and the ADCs, 8-to-1 multiplexing has been realized in front of both stages. To ease the implementation of multiplexing and handle large signal swings, the SC topology has been chosen. With a large gain (~ 47 dB) provided by the two CT stages, the sampling noise of the two SC amplifiers is negligible when referred to the electrode. However, when the CT output of the second-stage amplifier, V_{O2_i} , was connected to an input capacitor of the SC third stage [e.g., C_{1_i} in Fig. 5(a)], V_{O2_i} got disturbed and could not settle to a 10-bit accuracy

within the tracking phase ($\sim 47 \mu\text{s}$), as the second-stage bandwidth was limited to around 6 kHz. To solve this issue a CT buffer could have been added after each second-stage amplifier, but this would have entailed additional power consumption. In this paper, a pre-charging amplifier, A_{Pre} , was connected to V_{O2_i} at the beginning of the tracking phase and drove C_{1_i} [Fig. 5(a)]. Thus, V_{O2_i} was disturbed only by a small capacitor (input capacitance of $A_{Pre} \ll C_{1_i}$). At the end of pre-charging, the voltage of C_{1_i} was already quite close to V_{O2_i} [Fig. 5(b)], so that V_{O2_i} could settle to the required accuracy in the remaining tracking phase. As A_{Pre} was shared among eight channels, the power overhead was negligible.

The LFP and AP channels shared a similar topology. The 32 LFP channels have been divided into four blocks, each containing 8 CT first- and second-stage amplifiers, one SC third-stage amplifier, and one SAR ADC. The two CT stages featured the same topologies as the AP channels, with high-pass corner frequencies lower than 1 Hz. The third stage and the ADC were the same as those in the AP channels with a reduced clock rate.

C. Neurotransmitter Detection Channels

The NTD circuit is based on the fast-scan cyclic voltammetry (FSCV) technique [34]–[38]. This technique relies on applying a triangular-shape voltage signal with gradients of more than 100 V/s between a working and a reference electrode, and measuring the resulting current flowing through the working electrode. The trace of the measured current versus the applied voltage, i.e., cyclic voltammogram (CV),

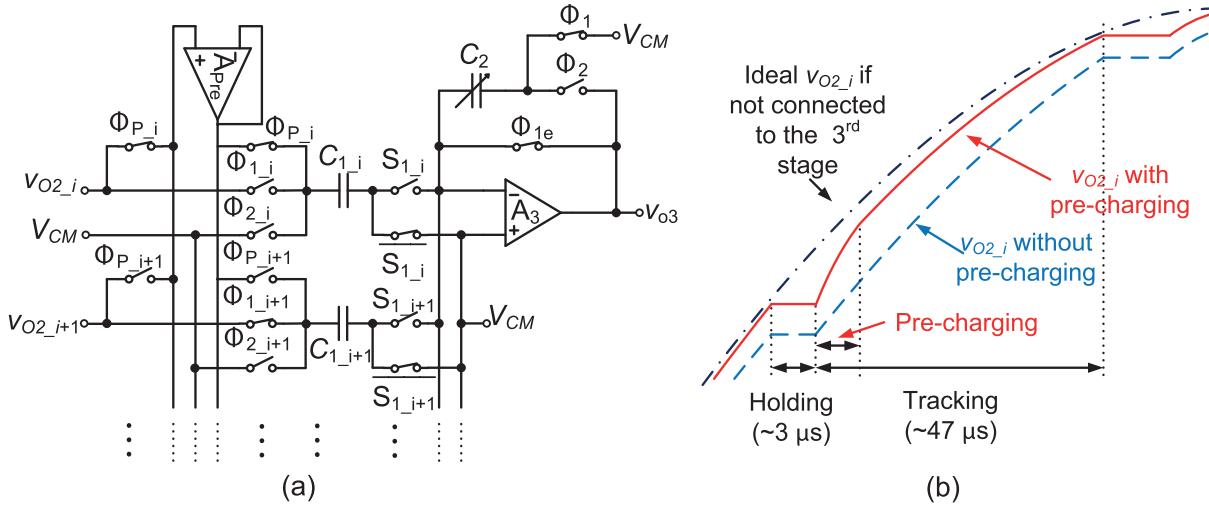


Fig. 5. Pre-charging technique. (a) Schematic of a portion of the SC third-stage amplifier, drawn as single-ended circuit for brevity. (b) Sketch of $V_{O2,i}$ with/without using the pre-charging technique.

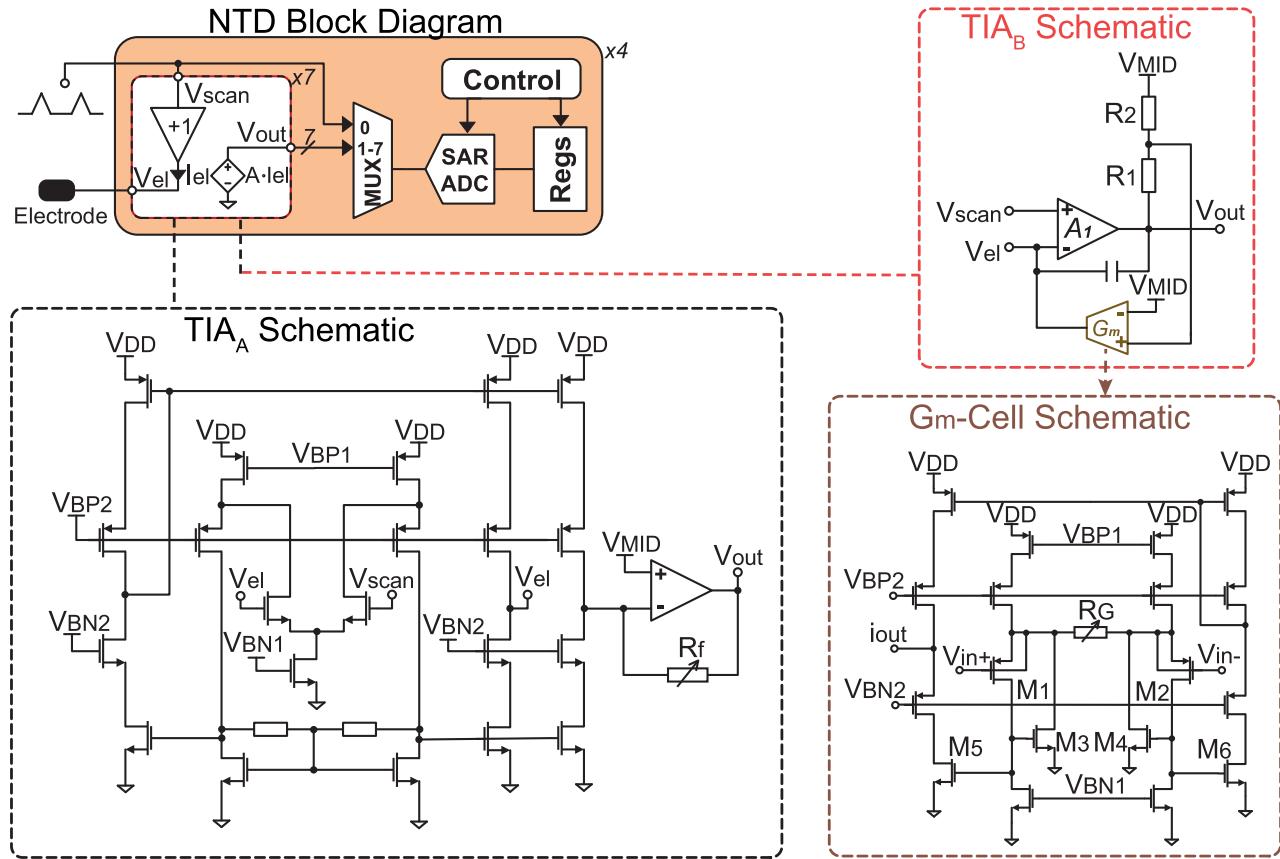


Fig. 6. Block diagram of the neurotransmitter detection (NTD), channel and schematics of TIA_A, TIA_B, and the G_m cell.

provides information about the electrochemical properties of the analytes in the cell medium. In this realization, the reference electrode potential was kept constant while the working electrode potential was swept to minimize disturbances to the other measurement units on the chip.

The NTD channels were grouped into four blocks, each block consisting of seven transimpedance amplifiers (TIAs), which were designed to copy the CV scan voltage to the electrode and measure the electrode current. To maintain the

timing information, the scan voltage and the seven current signals were multiplexed and then sampled at 20 kS/s by a 10-bit SAR ADC.

Two novel TIA circuit topologies were developed: TIA_A was designed to record from large electrodes, and TIA_B, which featured low noise levels, was tailored to record from small electrodes. Both topologies could scan the working electrode potential within a 2-V window and record currents on the order of microampere, at a 10-bit resolution (Fig. 6).

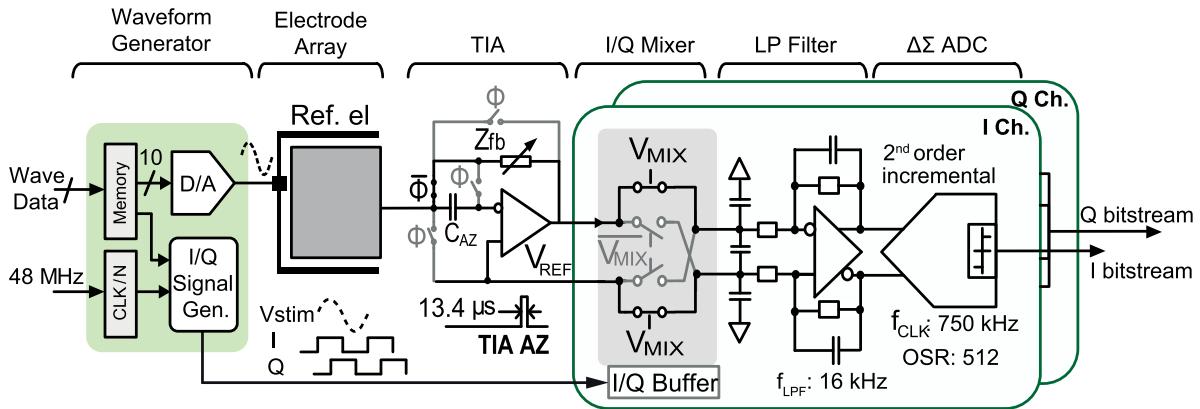


Fig. 7. Schematic of the lock-in-amplifier-based IM channel.

TIA_A included a local common-mode feedback (LCMFB) OTA, configured in a unity-gain feedback to buffer the input scan voltage, and a resistive TIA. The cascode transistors in the current mirror ensured that the mirrored current closely followed the electrode current (I_{el}), irrespective of the voltage difference between the electrode and V_{MID} . The TIA_A output voltage (V_{out}) was equal to $R_f I_{el}$, where R_f could be configured as 1 or 3 MΩ. The OTA inside the TIA_A had its dominant pole at the output stage and remained stable even for very large capacitances of the aforementioned pseudo-large electrodes, and rendered slow-rate CV applications possible.

TIA_B was composed of a two-stage Miller-compensated opamp (A_1) and a G_m cell. This topology resembled a resistive TIA, but the feedback resistor was replaced with a linear G_m cell. The G_m cell eliminated the feedforward path passing through the feedback resistor and thus prevented the scan voltage appearing at the output. The linearity of the G_m cells (Fig. 6) was significantly improved by avoiding the body effect of M_1 and M_2 , and keeping V_{GS1} and V_{GS2} constant by a local feedback around M_1 , M_3 and M_2 , M_4 [39]. Therefore, the input differential voltage was almost entirely applied across R_1 and converted to a current. This current flowed through M_3 and M_4 and then got mirrored to the output branch. The cascode transistors at the output branch reduced the output current variation due to the scan voltage. The output current of the G_m cell can be calculated as

$$i_{out} = 2 \cdot \frac{(W/L)_5}{(W/L)_3} \cdot \frac{1}{R_G} \cdot \frac{R_2}{R_1 + R_2} \cdot v_{out} = \frac{2}{R_G} \cdot \frac{R_2}{R_1 + R_2} \cdot v_{out}$$

where $(W/L)_5$ was equal to $(W/L)_3$ for this design. Since the input impedance of A_1 was very high, i_{out} had to exactly match the electrode current. Consequently, the transimpedance of TIA_B, R_{TIA} , can be calculated as $R_{TIA} = v_{out}/i_{in} = (R_G/2) \cdot [(R_1 + R_2)/R_2]$, which can be tuned according to the experimental conditions.

D. Impedance Measurement Channels

The main challenge in integrating many impedance measurement (IM) channels with limited silicon area is to achieve simultaneously low noise level, high dynamic range, and low power consumption. The state-of-the-art IM systems typically tradeoff large area per channel and power for low noise [40].

Most systems feature exclusively IM channels [10], and only few systems combine both electrophysiology and IM [6], [41]. While [41] reports electrode IM only, [6] reports IM of cardiac cells, however, with a poor spatial resolution.

To run IM in real time, a waveform generator with a programmable frequency (1 Hz–1 MHz) and amplitude (set by a 10-bit DAC) was integrated on chip (Fig. 7). The generated sinusoidal voltage (V_{Stim}) was applied between the reference electrode and the selected working electrodes. The resulting current signal from each working electrode ($I_{el} = V_{Stim}/Z_{el}$) was converted into a voltage, and the impedance magnitude and phase were reconstructed with a lock-in-amplifier, realized by a low-noise TIA and two quadrature phase mixers, followed by a low-pass filter (LPF). The implemented TIA can be programmed with either resistive feedback for measuring large electrodes (impedance < 100 MΩ) or capacitive feedback for measuring electrodes smaller than 10-μm diameter (impedance > 100 MΩ). For the capacitive feedback TIA, a periodic reset [42] was used to avoid the amplifier going to saturation and keep the electrode potential at the reference voltage, V_{REF} . To mitigate the drift of the electrode-electrolyte interface capacitor C_e , and the amplifier offset, the TIA circuitry included an auto zeroing (AZ) function. The amplifier offset was first stored in C_{AZ} (200 fF) during the reset phase, so that during the measurement phase the voltage stored in C_{AZ} cancelled the offset and low-frequency drift from the electrode (Fig. 7). The TIA's output signal was mixed with the in- and quadrature-phase (I/Q) signals, which were generated by the waveform generator and phase-locked with V_{Stim} to produce I/Q demodulated impedance signals. A double-balanced passive mixer architecture was selected, since passive mixers normally show higher linearity and negligible 1/f noise compared to their active counterparts [43]. An active differential LPF was used to filter out higher order harmonics and intermodulation products before the A/D conversion. The LPF can be bypassed or its gain set to 1 or 5 by tuning the feedback resistor. The cut-off frequency of the LPF was set to 16 kHz, which was about 1/46 of the sampling frequency of the ΔΣ ADC. The I/Q output of the lock-in-amplifier was digitized by the incremental single-bit SC ΔΣ ADC, consisting of an on-chip ΔΣ modulator and an off-chip decimation filter. To handle large input signal swing,

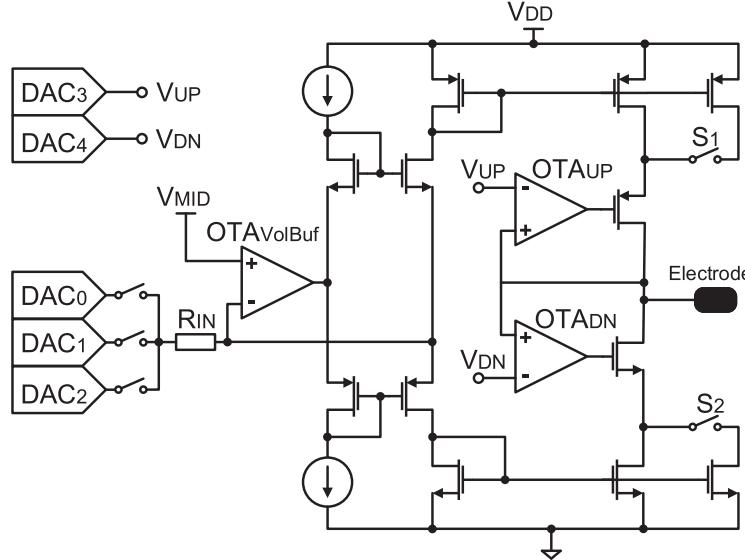


Fig. 8. Schematic of the current/voltage-controlled stimulation buffer.

while relaxing the slewing requirements of the integrators, cascade-of-integrators with feed-forward (CIFF) topology was employed [44]. Setting the sampling frequency to 750 kHz relaxed the anti-aliasing requirement, and the oversampling ratio was high enough to guarantee a resolution of 14 bits and a temporal resolution of 10 ms upon using proper filtering [40]. To reduce kT/C noise, a large sampling capacitor (1.6 pF) was used. The flicker noise and the offset contributed by the first-stage integrator opamp were suppressed by the AZ technique [45].

E. Stimulation Channels

Sixteen stimulation buffers were integrated on the chip, grouped into two blocks of eight. Additionally, each block contained three DACs for producing the stimulation waveforms and two DACs for setting the limiting voltages, all five DACs shared by the eight stimulation buffers. Each buffer can be configured as voltage-only or current/voltage-controlled buffer. Most reported stimulation buffers provide either voltage- or current-controlled stimulation pulses [46]. Here, the current/voltage-controlled buffers can simultaneously control both the output current and the output voltage. Current-controlled stimulation is desirable for precise charge delivery, independent of the electrode impedance, whereas controlling the stimulation voltage is needed to avoid tissue damage upon exceeding safe stimulation range. Fig. 8 shows the schematic of the stimulation buffer configured in the current/voltage-controlled mode. The core of this circuit is a positive current conveyor of type II (CCII+), an improved version of [47], which converts DAC voltages into electrode currents. The default current range can be increased by closing S_1 and S_2 , which increases the gain of the current mirror in the output stage from 1 A/A to about 11 A/A. R_{IN} had a value of 50 k Ω , therefore ± 1.5 V DAC signal produced ± 30 μ A in the low-current mode and ± 330 μ A in the high-current mode. The voltage controllability was realized by OTA_{UP} and

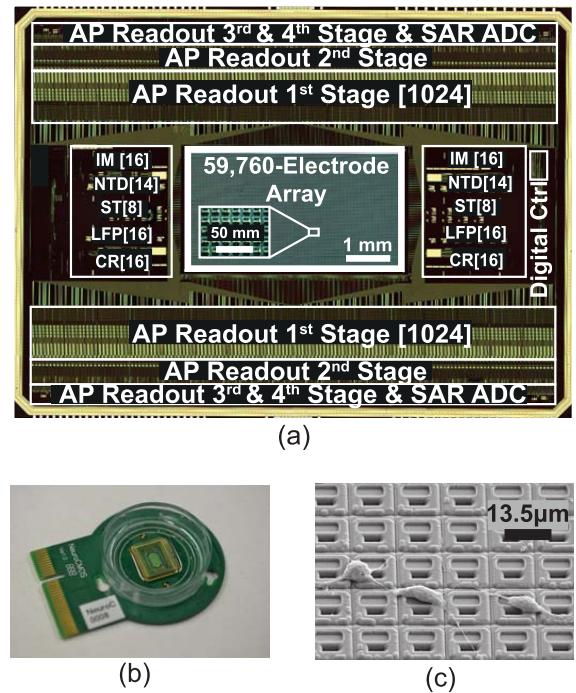


Fig. 9. (a) Chip micrograph; the die size is 12×8.9 mm 2 . (b) Biocompatible chip packaging and PCB. (c) SEM image of the chip surface, showing in-house post-processed Pt-electrodes and dissociated primary rat cortical neurons, cultured on top.

OTA_{DN}, which turned off either the positive or the negative output current, when the output voltage reached the predefined values of V_{UP} or V_{DN} , respectively. For the voltage-only controlled stimulation, OTAVolBuf was configured in the unity-gain feedback and directly connected to the output. OTAVolBuf used the LCMFB technique as well, and had the dominant pole located at the output node, suited to drive the mainly capacitive electrodes.

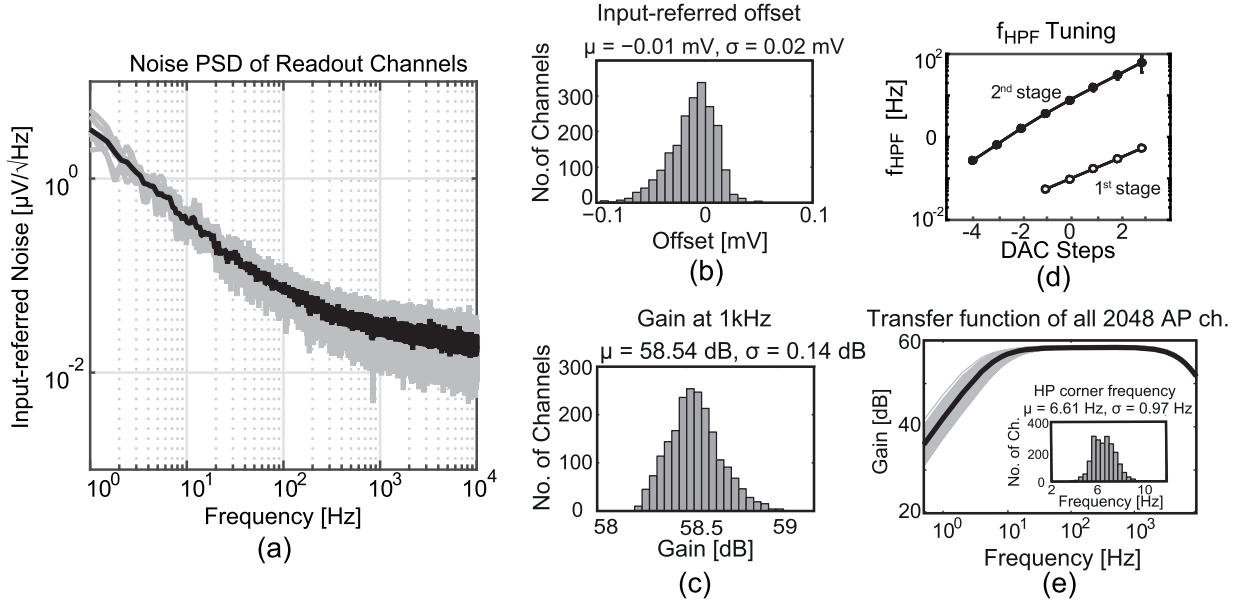


Fig. 10. (a) Noise power spectral density of the AP recording channel including the ADC. (b) Input-referred offset distribution of the 2048 AP channels. (c) Gain distribution of the 2048 AP channels. (d) First- and second-stage HPF corner frequency (f_{HPF}) tuned by the current DAC. (e) Transfer function of all 2048 AP ch.

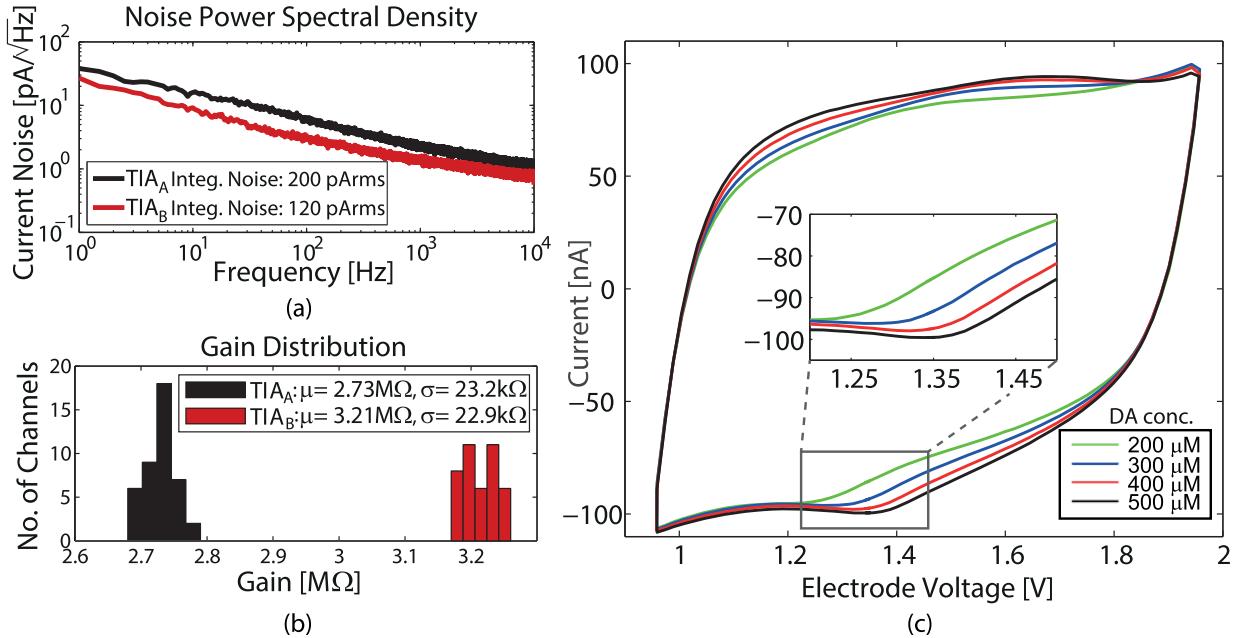


Fig. 11. (a) Noise power spectral density of TIA_A and TIA_B including multiplexer and ADC. b) Gain distribution across three chips. (c) Recorded FSCV results for concentrations of 200, 300, 400, and 500 μM DA in 0.1-M PBS. TIA_B connected to a single electrode has been used. Each of the curves is an average over 98 scans applied within 1 s.

IV. SYSTEM INTEGRATION

A. Digital Control

A 48-MHz-serial peripheral interface (SPI) interface was used to stream the configuration data to the chip, followed by an on-chip cyclic redundancy check (CRC). The measurement/stimulation units and the electrode array were grouped into 26 independently addressable blocks that were interfaced by the on-chip controller using an addressing scheme. As the

chip extended over $12 \times 8.9 \text{ mm}^2$, to guarantee the settling times of the 10-bit-word data generated by the different measurement blocks, the system Read Data Bus was divided into two busses, both running at 24 MHz. The data from the busses were fetched by the controller in an alternating manner at 48 MHz and sent off chip. The order in which the data generated by the measurement units were allocated on the two data busses was defined by the Bus Master module of the digital controller. To avoid data collision, an OR-tree

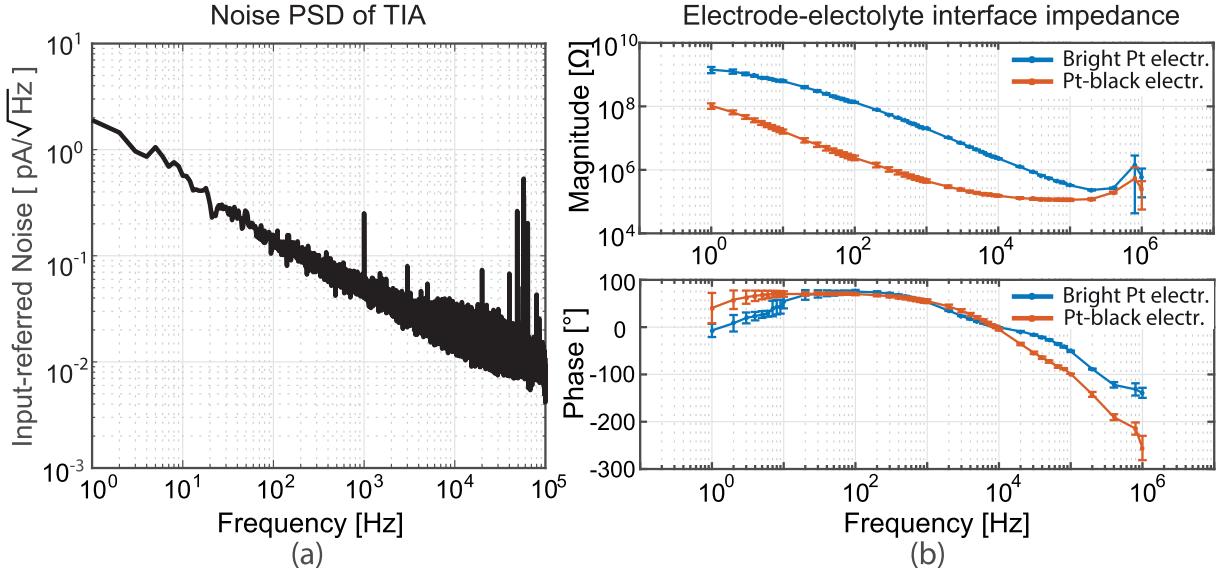


Fig. 12. (a) Noise power spectral density of the TIA with $R_f = 10 \text{ M}\Omega$. (b) Magnitude and phase of the bright Pt and Pt-black electrode impedance in a frequency range between 1 Hz and 1 MHz, averaged over 6 and 8 electrodes for bright Pt and Pt-black, respectively.

was inserted between the busses and the measurement units. The chip output data was organized in packages, aligned with the sampling cycles, each featuring 2400 10-bit words, ending with a 20-bit CRC checksum.

B. Chip Layout and Fabrication

The chip was fabricated in a 0.18- μm CMOS technology (2P6M) and has a size of $12 \times 8.9 \text{ mm}^2$. The platinum electrodes were post-processed at wafer level by means of ion beam deposition and etching. In the same step, two Pt-resistors used as on-chip temperature sensors were fabricated and implemented in four-terminal sensing configurations. A multilayer $\text{SiO}_2/\text{Si}_3\text{N}_4$ passivation stack was deposited by plasma-enhanced chemical vapor deposition, on the one hand, to protect the CMOS circuits against the saline solution that was used as cell culture medium, and, on the other hand, to prevent the release of toxic aluminum and copper from the CMOS metal layers into the cell culture. Openings in the passivation, defining the electrode areas and wire bonding contacts, were fabricated in a reactive-ion etching step. A shifted-electrode layout [48] was employed to ensure a tight seal between the electrodes in the liquid phase and the CMOS metal layers and circuitry in the chip. Fig. 9 shows the micrograph of the chip, bio-compatible chip packaging, and an SEM image of the post-processed array surface with rat cortical neurons.

V. ELECTRICAL CHARACTERIZATION

A. Voltage Recording Channels

The integrated input-referred noise of an AP recording channel, including the ADC, was $2.4 \mu\text{V}_{\text{RMS}}$ in the AP band (300 Hz–10 kHz), and $5.4 \mu\text{V}_{\text{RMS}}$ over the full band (1 Hz–10 kHz) [Fig. 10(a)]. The noise of an LFP recording channel was $3.6 \mu\text{V}_{\text{RMS}}$ in the LFP band (1–300 Hz), and $4.3 \mu\text{V}_{\text{RMS}}$ over the full band (1 Hz–10 kHz). The

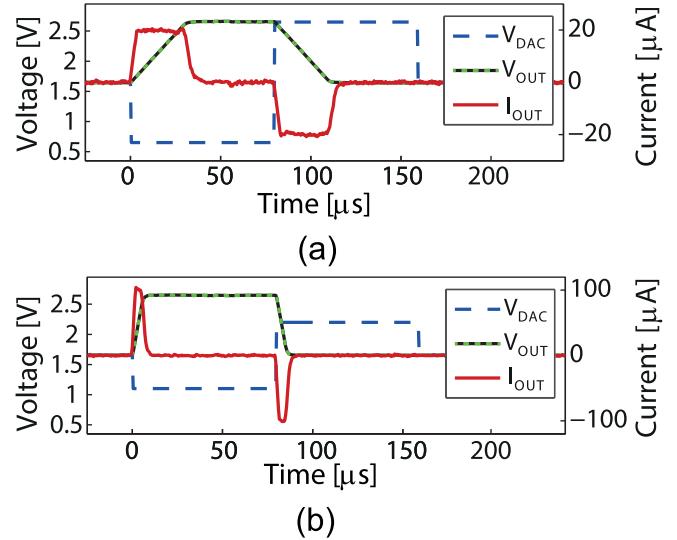


Fig. 13. Voltage (black-green dotted line) and current (red bold line) waveforms, generated by the stimulation buffer operated in current/voltage-controlled mode and connected to a 610-pF external load. The blue dashed line indicates the input waveform. (a) Low-current mode configuration. (b) High-current mode configuration.

measured maximum input-referred offset ranged from -110 to $70 \mu\text{V}$, which was achieved without dedicated offset compensation/calibration circuitry [29], [30] [Fig. 10(b)]. The measured maximum gain of the recording channel was 76.4 dB. An excellent gain uniformity of $\sigma = 0.14 \text{ dB}$ [Fig. 10(c)] was measured by applying a common sinusoidal signal to all inputs. The two tuning curves of the first-and second-stage HPF corner frequency (f_{HPF}) are illustrated in Fig. 10(d). Fig. 10(e) shows the overall transfer function of all 2048 AP recording channels. The histogram inset demonstrates a good uniformity of $f_{\text{HPF}}(\sigma = 0.97 \text{ Hz})$, which indicates a good matching of the pseudo-resistors across all channels. Moreover, the SAR ADC achieved an SNDR

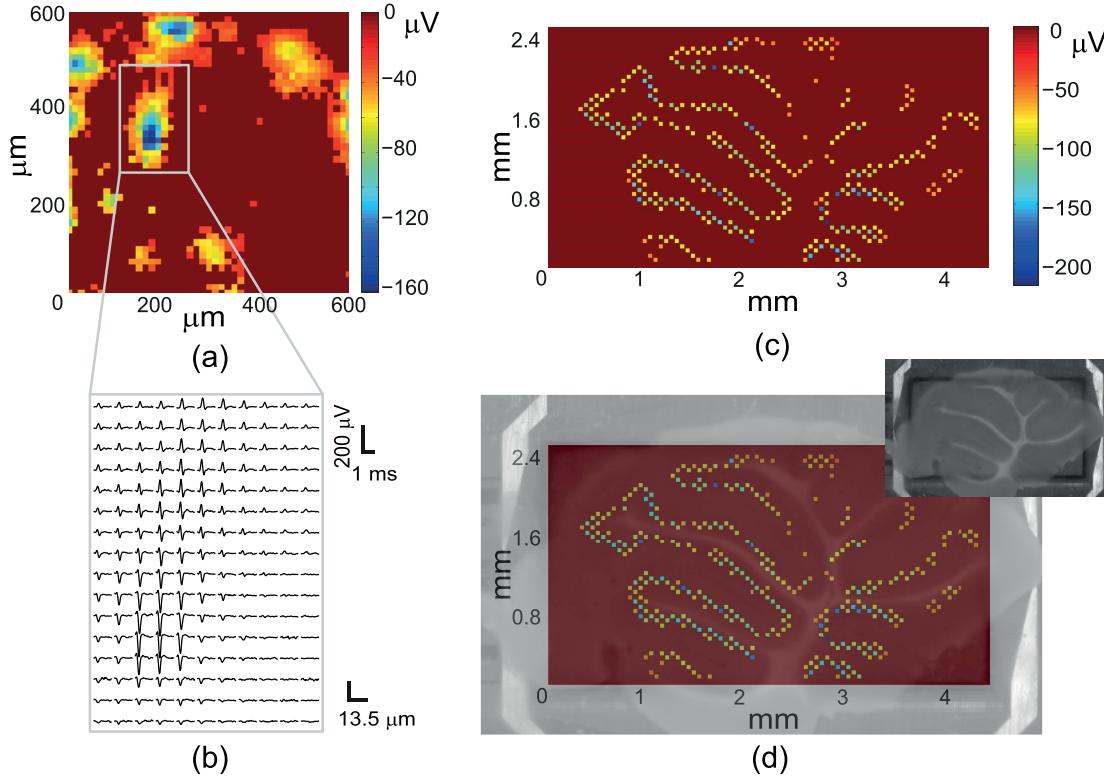


Fig. 14. (a) Average negative peak amplitudes, recorded by an HD electrode configuration (45×45 pixels, $607.5 \times 607.5 \mu\text{m}^2$) from dissociated primary rat cortical neurons. Each pixel in the image corresponds to an electrode. (b) AP waveforms, recorded in a sub-region of (a), averaged 20 times. (c) Mouse cerebellar slice electrical activity, recorded with a single sparse configuration of 2000 electrodes. The recording electrodes are displayed nine times larger than their original size for visual clarity. (d) Overlap of (c) and a microscopy image of the slice (inset).

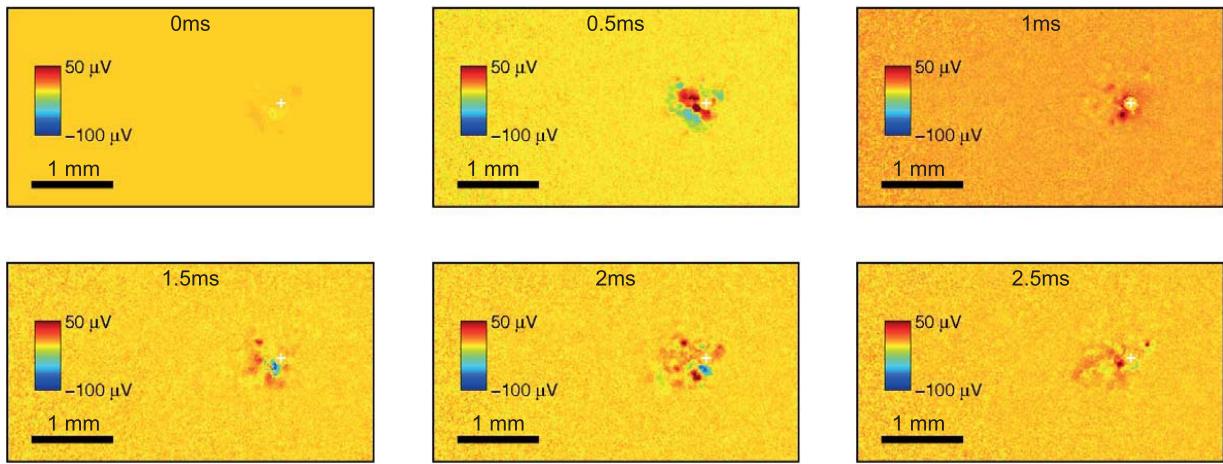


Fig. 15. Six frames showing 2.5 ms of evoked neuronal activity from a culture of dissociated rat cortical neurons. A biphasic voltage-controlled pulse (300-mV phase amplitude and 200-μs phase duration) was applied to a single electrode (white cross), while the other electrodes were scanned in recording mode from the entire array ($4.48 \times 2.43 \text{ mm}^2$) at full spatial resolution (13.5-μm electrode pitch). 100 averages were computed for each electrode and temporally aligned with respect to the stimulation pulses.

of 56.2 dB at a sampling rate of 1.28 MS/s and with an input signal frequency of 1.1 kHz. Finally, the measured power consumption of each AP channel was around $16 \mu\text{W}$.

B. Neurotransmitter Detection Channels

The area per neurotransmitter channel was 0.04 mm^2 (TIA_A) and 0.047 mm^2 (TIA_B), whereas the power consumption amounted to $222 \mu\text{W}$ (TIA_A) and $178 \mu\text{W}$ (TIA_B).

The integrated input-referred noise of TIA_A and TIA_B , including the multiplexer and the ADC, was 200 and 120 pA_{rms}, respectively [Fig. 11(a)]. The gain distribution is depicted in Fig. 11(b). In Fig. 11(c), FSCV at 300 V/s using the TIA_B was conducted to measure four different concentrations of dopamine (DA) in phosphate-buffered saline (PBS, a saline which has similar electrical properties as physiological solution).

TABLE II
COMPARISON TO STATE-OF-THE-ART *in vitro* MEA SYSTEMS

Reference	[18]	[6]	[20]	[21]	This work
Type	In-pixel Amp	In-pixel Amp	In-pixel Amp	Switch Matrix	Switch Matrix
Technology	0.5 μm	0.13 μm	0.18 μm	0.35 μm	0.18 μm
Active Area	2.28 \times 1.14 mm^2	9 pixel groups of 0.128 mm^2	1 \times 1 mm^2 / 2 \times 2 mm^2	3.85 \times 2.10 mm^2	4.48 \times 2.43 mm^2
No. Transducers	32768	144	4225 / 1024	26400	59760
No. Different Measurement Modes	1	4	1	1	5
Pixel Pitch	8.775 μm	89.4 / 357.8 μm^d	16 / 32 μm	17.5 μm	13.5 μm
Transducers/ mm^2	12987	125 / 7.8	977,3906	3265	5487
No. Voltage Readout Channels	32768	144	4225	1024	2048 AP + 32 LFP
A/D Conversion	128 pipeline	Off chip	Off chip	1024 single-slope	32 + 4 SAR
ADC Resolution	9 bit	-	-	10 bit	10 bit
Sampling Rate	2.4 kS/s ^a	-	77 (25) kS/s ^a	20 kS/s	20 kS/s
Input-referred Noise	-	12.7 μVrms^e	44 μVrms^b	2.4 $\mu\text{Vrms}^{b,c}$	2.4 $\mu\text{Vrms}^{b,c}$ 3.6 $\mu\text{Vrms}^{c,f}$
Total Power	4 W	-	-	75 mW	86 mW
Die Size	9.5 \times 9.5 mm^2	2.2 \times 2 mm^2	-	10.1 \times 7.6 mm^2	12 \times 8.9 mm^2

^a When reading out all channels.

^b Noise integration over 300 Hz-10 kHz, for AP recording channels.

^c Including ADC.

^d Equivalent square-shaped pixel dimension, for the same spatial density.

^e Noise integration over 0.5 Hz-10 kHz.

^f Noise integration over 1 Hz-300 Hz, for LFP recording channels.

C. Impedance Measurement Channels

The integrated input-referred noise (1 Hz–100 kHz) of the TIA with a 10-M Ω feedback resistor was 6.4 pA_{RMS} [Fig. 12(a)]. The area and power consumption of the IM channel amounted to 0.1 mm^2 and 412 μW , respectively, whereas the waveform generator occupies an area of 0.012 mm^2 and

consumes 1.1 mW at 3.3 V supply voltage for driving a load of 10 nF at 1-MHz frequency. Pt-electrode-electrolyte interface was characterized in PBS, in a frequency range between 1 Hz and 1 MHz [Fig. 12(b)]. The same measurement was repeated after Pt-black electroplating, which was done by driving the current from an external Pt electrode (immersed into the

Pt working solution) to the array electrodes, which were shorted to the chip's probe pad (current sink). As expected, in the frequency range from 10 Hz to 10 kHz the impedance showed a 1/f roll-off behavior, which evidenced the dominance of the double-layer capacitance. The predominantly capacitive behavior was also indicated by the phase angle, which ranged between 60°–80°. At frequencies over 10 kHz, spreading resistance started dominating the impedance, as the phase angle moved toward zero [48]. The effect of Pt-black deposition was 30–40 fold reduction of impedance magnitude.

D. Stimulation Channels

The area of a stimulation channel was 0.046 mm². The power consumption was measured to be 251 and 306 μW per current/voltage-controlled stimulation buffer in the low- and high-current mode, respectively. Fig. 13 shows generated current/voltage-controlled pulses using the on-chip stimulation buffers with a load of 610 pF. The output current was switched off when the output voltage reached the predefined limits, in this case 2.65 V for V_{UP} and 1.65 V for V_{DN} . A ±1 V DAC signal resulted in ±20 μA output current for the low-current mode and a ±0.55 V DAC signal resulted in ±100 μA output current for the high-current mode [Fig. 13(a) and (b)]. The linearity of the circuit was measured by running a DC sweep, which evidenced a 10-bit linearity for the low-current mode in the range of ±30 μA and a 9-bit linearity for the high-current mode in the range of ±300 μA. The linearity of the voltage-only controlled stimulation was measured to be 10-bit in the range of ±1.45 V.

VI. BIOLOGICAL MEASUREMENT RESULTS

The presented HD-MEA system was verified in *in vitro* measurements. Fig. 14(a) depicts average spike amplitudes of dissociated rat cortical neurons (Wistar) recorded by an HD 45 × 45 pixels electrode block connected to 2025 AP channels. A close-up of the spatial distribution of average AP waveforms, which most likely belong to a single neuron, is plotted in Fig. 14(b). Fig. 14(c) depicts the average activity in a mouse cerebellar slice (C57Bl6J), recorded over the entire array by using a sparse electrode configuration (2000 AP channels, in a honey-comb configuration with an average of ~5.5 pixels spacing between the recording electrodes). Fig. 14(d) shows a superposition of the recorded electrical activity map with a microscopy image of the cerebellar slice. The large number of AP channels featured on the chip enabled a quick overview of the tissue activity by using a single, sparse electrode configuration, which revealed the locations of the electrically active Purkinje neurons [49].

Stimulus-evoked average activity of dissociated rat cortical neurons, triggered by a biphasic voltage pulse of 300-mV amplitude, was recorded over the entire electrode array area at full-spatial resolution and depicted in Fig. 15.

VII. CONCLUSION

The presented HD-MEA system includes the largest number of measurement/stimulation functions to date, comprising electrophysiology readout, impedance measurement, and

neurotransmitter detection, as well as stimulation capabilities (Table II). At the same time, it features the largest active electrode array area (10.9 mm²) to date, whereas the number of voltage recording channels (2048 AP + 32 LFP), the spatial resolution (13.5 μm electrode pitch), the noise characteristics, and the power consumption are comparable to those of the best state-of-the-art MEA systems. Any measurement/stimulation unit can be connected to any electrode on the array owing to the flexible electrode routing via the switch matrix. The possibility to perform different measurement/stimulation functions in parallel will pave the way to complex experiments that target multiple cellular parameters at once.

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