Insights Into Phase-Noise Scaling in Switch-Coupled Multi-Core *LC* VCOs for E-Band Adaptive Modulation Links

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***Abstract*— High-capacity wireless links at millimeter-Waves are candidate for backhaul infrastructure to small-cell mobile networks. However, the use of high-order modulation schemes sets challenging phase-noise specifications for integrated frequency synthesizers. Moreover, the use of adaptive modulation suggests local oscillators exploiting noise scaling, up to several decibel depending on channel conditions. In this paper, multi-core switch-coupled *LC* voltage-controlled oscillators are proposed to achieve ultra-low phase noise and scalable noise performance according to system requirements in a power-efficient way. A theoretical model investigating the effect of *LC* core component mismatches shows very good agreement with experiments. Design insights are provided, key in order to take effective advantage from the proposed low-noise technique. A quad-core ∼20 GHz oscillator prototype, followed by a frequency quadrupler, has been realized in 55-nm BiCMOS technology. Measured performances are ∼70-to-81 GHz frequency range with −106.5-dBc/Hz minimum phase noise at 1-MHz offset from an 80-GHz carrier with 50-mW power consumption and 1.2-V supply. To authors' knowledge, this is the lowest phase noise measured in the E-Band using integrated technologies and CMOS-compatible supplies. When noise requirements are relaxed, auxiliary cores are turned off rising phase noise by 6 dB but with power consumption reduced down to 18 mW only.**

***Index Terms*— Backhaul, BiCMOS, coupledoscillators, E-Band, millimeter-waves, multi-core, phase-noise scaling, switch-coupled, voltage-controlled oscillator (VCO).**

I. Introduction

THE ever increasing mobile data traffic, expected to grow by $>8\times$ from 2015 to 2020 [1], is driving continuous innovation in wireless communications, and next-generation mobile networks (i.e., 5G and beyond) are expected to provide several gigabit per second user data rate [2]. To increase the channel capacity beyond the levels offered by long term evolution, industry, and academia are investigating several techniques such as beamforming, multiple-input-multiple-output communications, cell coverage area reduction, and millimeter-wave wireless links [2], [3]. All these techniques require a drastic increase in the base-transceiver-station (BTS) density, leading to small-cell or pico-cell networks to leverage spatial diversity and compensate propagation losses at millimeter-waves. While small-cell backhaul infrastructures using wired optical links are expensive and difficult to implement, especially in urban environments, high-capacity point-to-point (PtP) millimeter-wave links are currently being investigated to provide a cheap and flexible wireless backhaul to small-cell networks [2], [4]. In the E-band in particular, 71–76 and 81–86 GHz frequency ranges have been allocated by both FCC and European Electronic Communications Committee as light-licensed bands for PtP wireless links. E-Band PtP channels provide gigabit per second, kilometer-range wireless communication, suitable for small-cell backhaul infrastructure [2], [5]. Small-cell transceivers have to be more compact, cheap, and energy-efficient compared to the traditional BTS counterpart. This motivates a shift toward high-volume CMOS and BiCMOS technologies, and the use of low-power design techniques [2].

In this paper, we address the design of BiCMOS integrated circuits for frequency synthesis in E-Band backhaul transceivers. Currently proposed microwave and millimeter-wave PtP links employ adaptive modulation standards so as to change the modulation order according to channel quality [6], [7]. In high-SNR conditions, spectrally efficient modulations like 64 QAM and beyond are employed. Instead, if the received SNR is poor (e.g., during heavy rain outage), simpler modulations such as QPSK are used. The modulation order sets phase noise requirements for the local oscillator (LO). Indeed, integrated LO phase noise has a significant impact on error vector magnitude (EVM) degradation [8]. Since high-order modulations mandate lower EVM, they also demand a more stringent phase-noise specification.

Voltage-controlled oscillators (VCOs) operating above 20 GHz suffer from severe phase noise degradations due to the poor quality factor of integrated capacitors at millimeter-wave [9], [10]. Therefore, the proposed VCO produces

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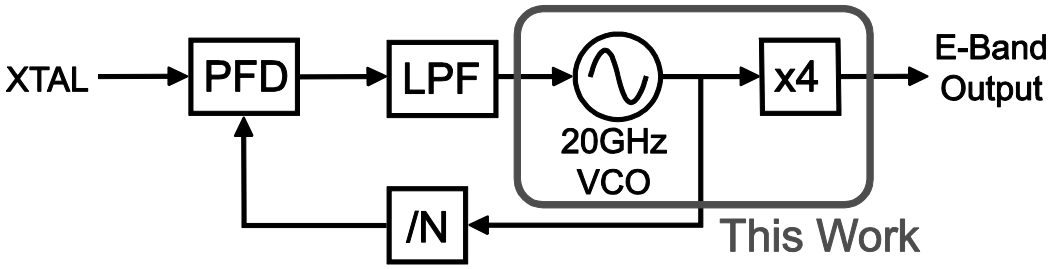

Fig. 1. Proposed E-Band frequency synthesizer architecture.

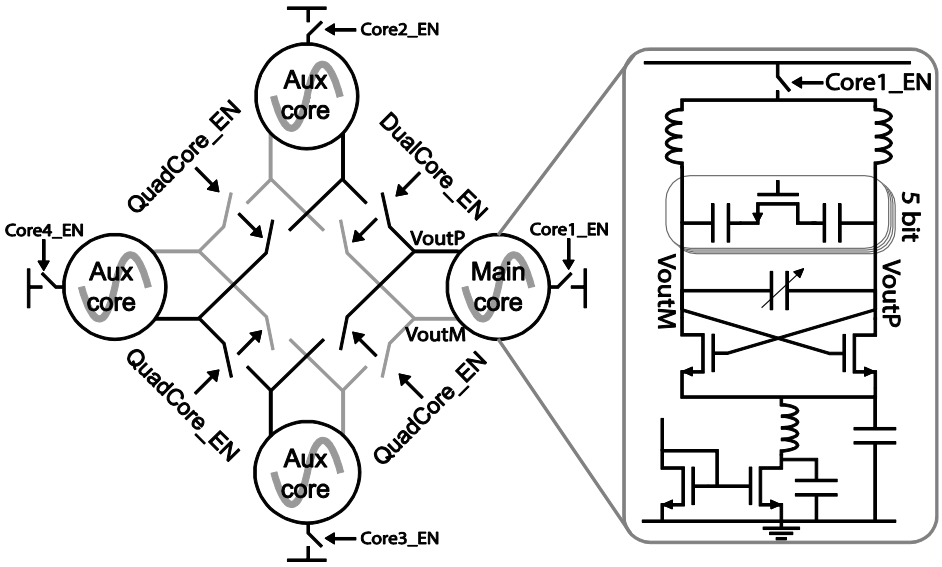

Fig. 2. Proposed multi-core VCO.

a ∼20 GHz tone, and it is followed by a frequency quadrupler generating the E-Band reference, as shown in Fig. 1. In order to efficiently scale noise and power according to modulation order, we propose the multi-core VCO shown in Fig. 2 [11]. Four oscillators are connected together through switches and selectively turned on and off according to the required phase-noise performance. When all the cores are oscillating, phase noise is reduced by 6 dB, compared to a single oscillator, meeting the low-noise performance dictated by 64 QAM. Auxiliary cores are turned off when simpler modulations are employed in order to save power.

Results achieved in this work are particularly relevant if we consider that ultra-low phase-noise integrated millimeter-wave VCOs presented so far are mostly based on SiGe Colpitts oscillators, and exploit the relatively high supply voltage (i.e., >3 V) of SiGe bipolar devices to maximize the oscillation swing and minimize phase noise [12]–[14]. Instead, the proposed design achieves similar phase-noise levels while adopting a CMOS-compatible supply voltage and furthermore allows power-efficient noise scaling.

The paper is organized as follows. In Section II, a system-level analysis for E-Band PtP links is described, leading to phase noise specifications for the VCO. In Section III, the idea behind the multi-core VCO and performance limits due to component mismatches are discussed in detail. In Section IV, circuit design details are outlined. An improved VCO core design with respect to [11] is presented. In Section V, measurement results on BiCMOS 55-nm prototypes are shown. Finally, Section VI draws conclusions.

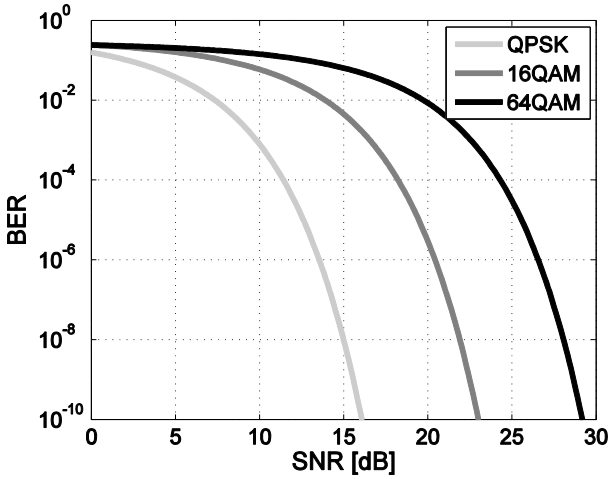

Fig. 3. BER curves for QPSK, 16QAM, and 64QAM according to (1).

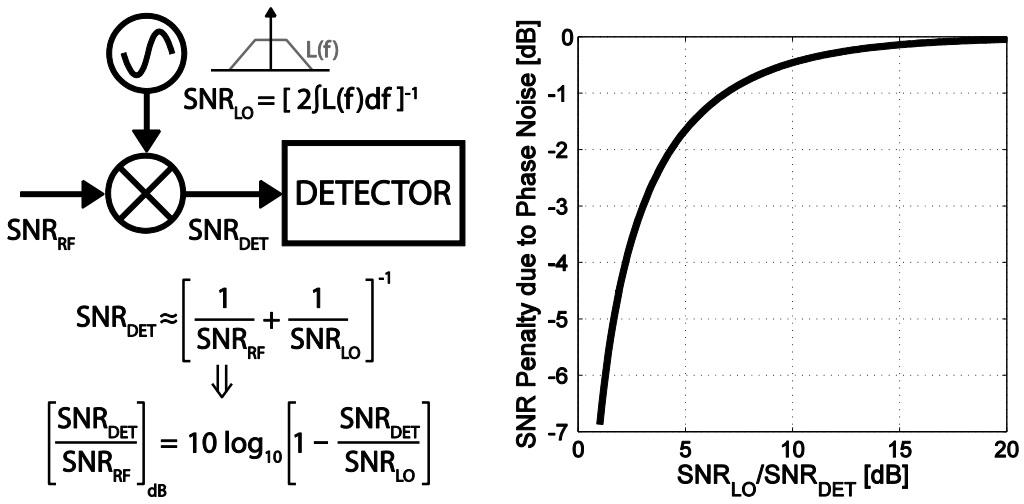

Fig. 4. SNR degradation due to LO phase noise.

II. System-Level Analysis

In even-order M-QAM modulations, the bit-error rate (BER) is linked to the signal-to-noise ratio at the detector ($\mathrm{SNR_{DET}}$) by the formula [15]

$$\mathrm{BER} \approx \frac{1}{\log_2 M} 4 \left(1 - \frac{1}{\sqrt{M}}\right) Q\left(\sqrt{\frac{3}{M-1}\mathrm{SNR_{DET}}}\right) \quad (1)$$

where Q is the well-known Q-function. BER curves for QPSK, 16QAM, and 64QAM are plotted in Fig. 3. It can be noticed that if M is multiplied by four the SNR has to increase by ~6 dB to achieve the same error probability. For example, assuming BER $= 10^{-6}$, the minimum $\mathrm{SNR_{DET}}$ requirement is approximately 13.6 dB for QPSK, 20.4 dB for 16QAM, and 26.6 dB for 64QAM.

As shown in Fig. 4, assuming an ideal mixer and a noisy LO, the LO integrated phase noise can be approximated as an uncorrelated noise process which degrades the received signal SNR according to the equation in the figure [16]. The SNR degradation resulting from the mixing process can be calculated as a function of $\mathrm{SNR_{LO}/SNR_{DET}}$, where $\mathrm{SNR_{LO}} = [2\int_0^{\mathrm{BW_{CH}}/2} L(f)df]^{-1}$, and $\mathrm{BW_{CH}} = 250$ MHz is the channel bandwidth [7]. As plotted in Fig. 4, to guarantee negligible noise degradation (i.e., <0.5 dB) $\mathrm{SNR_{LO}}$ has to be at least 10 dB higher than $\mathrm{SNR_{DET}}$. At given BER, high-order modulations set a more challenging requirement for $\mathrm{SNR_{LO}}$.

To derive VCO phase noise requirements from $\mathrm{SNR_{LO}}$, two main aspects have to be considered. The first is the bandwidth of the phase-locked loop (PLL), which is assumed to be realized through an analog second-order loop. The second is the bandwidth of the carrier phase estimator, included in the baseband digital front-end. In PtP transceivers, this function is usually performed by a data-aided second-order tracking loop. The loop evaluates the phase error of the received constellation and counter rotates the baseband data stream through a digital phase shifter. Therefore, it acts as an additional PLL which high-pass filters the LO phase noise using the received data as a phase reference [17]. A wideband tracking loop is desirable to filter out most of the synthesizer phase noise.

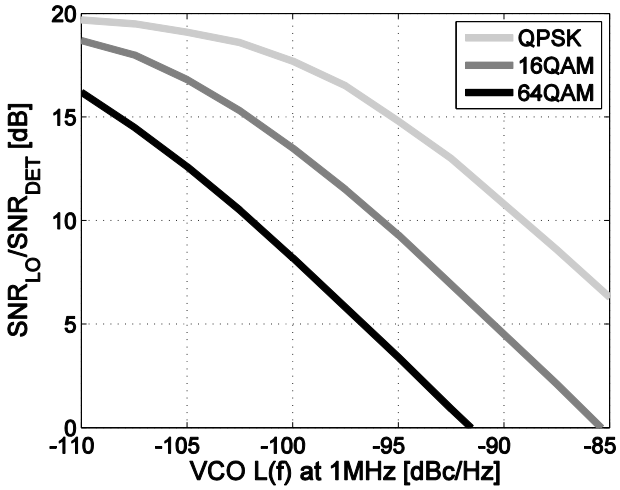

Fig. 5. Simulated $\mathrm{SNR_{LO}/SNR_{DET}}$ versus VCO phase noise at 1-MHz offset for different M-QAM modulations, assuming a narrowband PLL, a second-order phase-tracking loop with $\mathrm{BW_{TL}} = 750$ kHz and $\mathrm{SNR_{DET}}$ equal to the minimum requirement for 10^{-6} BER with the corresponding modulation.

However, the tracking loop bandwidth $\mathrm{BW_{TL}}$ is limited by two main issues. First, for proper operation, $\mathrm{BW_{TL}}$ has to be $<<\mathrm{BW_{CH}}$. Also, if the bandwidth is too high, a considerable amount of the additive white Gaussian noise channel noise is converted into phase noise, leading to an overall noise penalty [17].

In our case, $\mathrm{BW_{TL}} \approx 750$ kHz was chosen as a suitable value according to system-level simulations. Since the VCO phase noise is filtered by the tracking loop up to $\mathrm{BW_{TL}}$, a narrowband PLL (i.e., $\mathrm{BW_{PLL}} < 100$ kHz) can be employed, reducing the in-band noise contribution of loop components and crystal reference, that become significant at millimeter-waves [18].

As a result, $\mathrm{SNR_{LO}/SNR_{DET}}$ is plotted in Fig. 5 versus VCO phase noise at 1-MHz offset from an 80-GHz carrier, assuming $\mathrm{SNR_{DET}}$ equal to the minimum SNR requirement for BER $= 10^{-6}$ with the corresponding modulation. VCO $1/f^3$ noise is not considered in the simulation since,

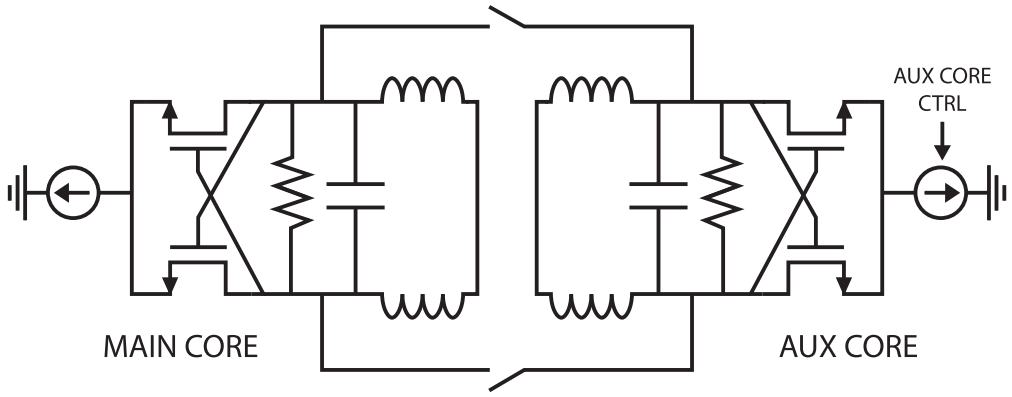

Fig. 6. Schematic of a dual-core noise-scalable VCO.

as long as the flicker corner is below or close to BW_{TL}, it has a negligible impact on SNR_{LO}. To keep SNR_{LO}/SNR_{DET} above 10 dB, the VCO has to achieve around -102 dBc/Hz phase noise for 64QAM and -90 dBc/Hz for QPSK. The phase-noise specification for 64QAM is challenging for millimeter-wave CMOS synthesizers, and requires to burn a significant fraction of the transceiver power in LO generation. Conversely, a synthesizer meeting 64QAM specifications would be widely overdesigned when lower-order modulations are employed. Trading LO noise and power in an efficient way according to the modulation order is therefore key.

III. Phase-Noise-Scalable Multi-Core VCO

A. Principle of Operation

Phase noise $L(f)$ in an LC-tank oscillator in the $1/f^2$ region can be described with good approximation by [19]–[21]

$$L(f) = 10\log\left[(1+F)\frac{4kTR_T}{A_0^2}\left(\frac{f_0}{2Qf}\right)^2\right] \tag{2}$$

where f is the frequency offset from the carrier, f_0 is the oscillation frequency, k is Boltzmann's constant, T is the absolute temperature, Q is the tank's quality factor, A_0 is the differential oscillation swing, and R_T is the tank's parallel resistance. Neglecting noise from biasing circuits, F is equal to the noise coefficient γ of active devices, under reasonable assumptions [21]. Equation (2) may be rewritten by replacing $A_0 = R_T I_{\omega 0}$, where $I_{\omega 0}$ is the fundamental-harmonic component of the tank current, and expressing $I_{\omega 0} = \eta_I I_{\rm dc}$ (where $I_{\rm dc}$ is the dc current drawn by the oscillator and η_I is a current-efficiency coefficient which depends on the oscillator topology [22])

$$L(f) = 10\log\left[(1+F)\frac{4kT}{R_T\eta_I^2 I_{\rm dc}^2}\left(\frac{f_0}{2Qf}\right)^2\right]. \tag{3}$$

The oscillator's figure of merit $\text{FoM} = L(f)(P_{\rm dc}/(1\text{mW}))((f/f_0))^2$, where $P_{\rm dc}$ is the power consumption [23], achieves a minimum when $I_{\rm dc}$ is chosen such that the oscillation swing reaches the saturation level [24]. For example, if current consumption is halved, the FoM is degraded by 3 dB.

Noise scaling at constant FoM in (2) is instead achieved through reduction of the tank impedance R_T, while keeping the oscillation swing A_0 constant [25]. $L(f)$ is linearly proportional to R_T, thus if the impedance is reduced by a factor N, phase noise is scaled down by N. On the other hand, since $A_0 \sim R_T I_{\rm dc}$, the dc current has to be increased by N in order to keep the oscillation swing constant. As a result, noise and power can be efficiently traded.

To lower R_T at constant Q, reactive components values have to be scaled down, as in Fig. 6, where an auxiliary LC tank is connected through switches to the main core. An additional cross-coupled pair is also placed in parallel with the auxiliary tank, in order to keep A_0 and the loop gain constant. When the switches are turned on, the tank impedance is halved and phase noise is reduced by 3 dB. The idea can be extended to multiple oscillators. In the proposed noise-adjustable oscillator [11], depicted in Fig. 2, single, double, and quad-core configurations are possible, leading to 3- and 6-dB phase-noise improvement, respectively. It is worth noticing that in this way we can also realize low tank impedance without sacrificing Q. On the contrary, a spiral inductor in a single-core VCO would suffer from a Q penalty when reducing inductance, due to both magnetic coupling between the two halves of the inductor and interconnection parasitic resistance [25], [26].

Multi-core LC VCOs employing parallel coupling for noise reduction were presented before, although without noise-scaling capability. Both dual- and quad-core configurations, employing resistive [25], capacitive [27], magnetic [28], and active [29] coupling, were demonstrated at RF frequencies. At millimeter-wave, a magnetically-coupled 50-GHz oscillator array was presented [30]. Noise tunability through parallel oscillator coupling was also included in a 0.25–4 GHz digital PLL presented in [31], where three inverter-based ring oscillators are connected through switches.

In switch-coupled multi-core LC VCOs, exploited in this work, the ON resistance of the switches has to be carefully selected in order to allow phase-noise reduction without penalizing the tuning range, especially at millimeter-waves. Indeed, mismatches between the oscillator tanks lead to a phase-noise penalty that can be minimized by selecting a low coupling resistance. On the other hand, this requires large switches, resulting in capacitive parasitics and tuning-range reduction. Furthermore, the switch capacitance changes between ON and OFF states, resulting in a shift of the central frequency from single to quad-core configuration. As a result, the effective

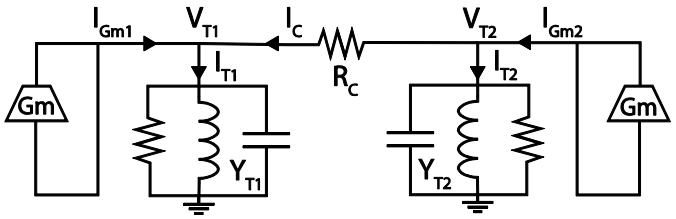

Fig. 7. Schematic of a dual-core resistively-coupled oscillator system.

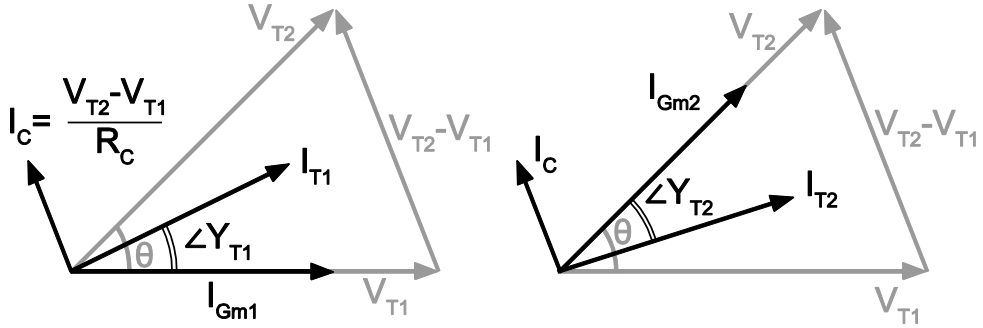

Fig. 8. Voltage (gray) and current (black) phasors in the dual-core system.

tuning range where all the configurations overlap in frequency is reduced further. To gain more insight in the noise degradation phenomenon and derive reliable design choices, we develop a model to describe the behavior of the resistively coupled multi-core oscillator in presence of component mismatches.

B. Effect of Component Mismatches

Literature on in-phase passively coupled oscillator systems is scarce and fragmentary. In the 90 s, York [32] and Chang *et al.* [33] studied arrays of coupled discrete microwave oscillators in presence of resonance frequency mismatch. However, their analysis is based on the assumption of weak coupling between oscillators, only considering phase dynamics. Conversely, in resistively coupled oscillators coupling can be strong and, as will be shown in the following, amplitude dynamics plays a key role in describing the system behavior. A recent linear time-invariant analysis of in-phase resistively coupled oscillators is provided in [25], where authors show how a non-zero coupling resistance sets a finite bandwidth BW_C to the coupling transfer function between oscillators. As a consequence, phase noise is only scaled down up to an offset BW_C from the carrier. Although this effect has to be taken into account, in our case it is a second-order limitation when compared to another effect, namely, noise degradation in presence of oscillation frequency mismatch. A linear time-variant model taking it into account is developed here.

A dual-core single-ended oscillator system, as shown in Fig. 7, is considered first. When the resonance frequencies f_{01} and f_{02} of the two *LC* tanks are the same, the oscillators are in phase at steady state, and no signal current flows in the coupling path. The oscillation amplitude is $A_0 = \eta_I I_{\mathrm{dc}} R_T$ and the circuit behavior is independent of the coupling resistance R_C. If a mismatch $\Delta f_0 = f_{01} - f_{02}$ is present, the two oscillators may still be frequency locked, and oscillate at a frequency f_{osc} between f_{01} and f_{02}. Both oscillators work off-resonance, meaning that $\angle Y_T \neq 0$, where Y_T is the tank admittance given by

$$Y_T = \frac{1}{R_T} + j\frac{Q}{R_T}\left(\frac{f_{\mathrm{osc}}}{f_0} - \frac{f_0}{f_{\mathrm{osc}}}\right) \cong \frac{1}{R_T} + j\frac{2Q}{R_T}\frac{f_{\mathrm{osc}} - f_0}{f_0} \tag{4}$$

where the approximation holds provided $\delta f = f_{\mathrm{osc}} - f_0 \ll f_0$. As a result, the tank voltage V_T and the tank current I_T are phase shifted, as shown in Fig. 8. The tank current in turn is the sum of two components. The first is the current provided by the transconductor $I_{\mathrm{Gm}} = \eta_I I_{\mathrm{dc}}$, which is in phase with V_T. The second is the coupling current I_C, given by $(V_{T2} - V_{T1})/R_C$. As shown in Fig. 8, $I_C \neq 0$ requires a non-null phase shift θ between the tank voltages V_{T1} and V_{T2}.

The steady state under locking condition can be found by setting $I_T = I_{\mathrm{Gm}} + I_C$ and $I_T = Y_T V_T$ for both tanks. Solutions for magnitude and phase, reported in Appendix A, yield

$$f_{\mathrm{osc}} = (f_{01} + f_{02})/2 \tag{5}$$

$$\theta = \sin^{-1}(K \cdot r) \tag{6}$$

$$|V_{T1}| = |V_{T2}| = aA_0a = \left[1 + \frac{1}{r} - \frac{\sqrt{1 - (K \cdot r)^2}}{r}\right]^{-1} \tag{7}$$

where $r = R_C/R_T$ and $K = Q(\Delta f_0/f_0)$. $Q_1 \cong Q_2 = Q$ and $\Delta f_0 \ll f_0$ were assumed. Solutions exist provided the following condition is satisfied:

$$\Delta f_0 < \Delta f_{0,\max} = \frac{f_0}{Qr}. \tag{8}$$

According to (6) and (7), a resonance frequency mismatch between the cores causes a reduction of the oscillation swing and a phase difference between the oscillator voltage waveforms. Both effects depend on R_C/R_T, and become negligible for $R_C << R_T$. The circuit in Fig. 7 was simulated in Cadence Virtuoso introducing a difference between the two tank inductances, at constant Q, to force a resonance mismatch Δf_0. Simulation results are compared with values

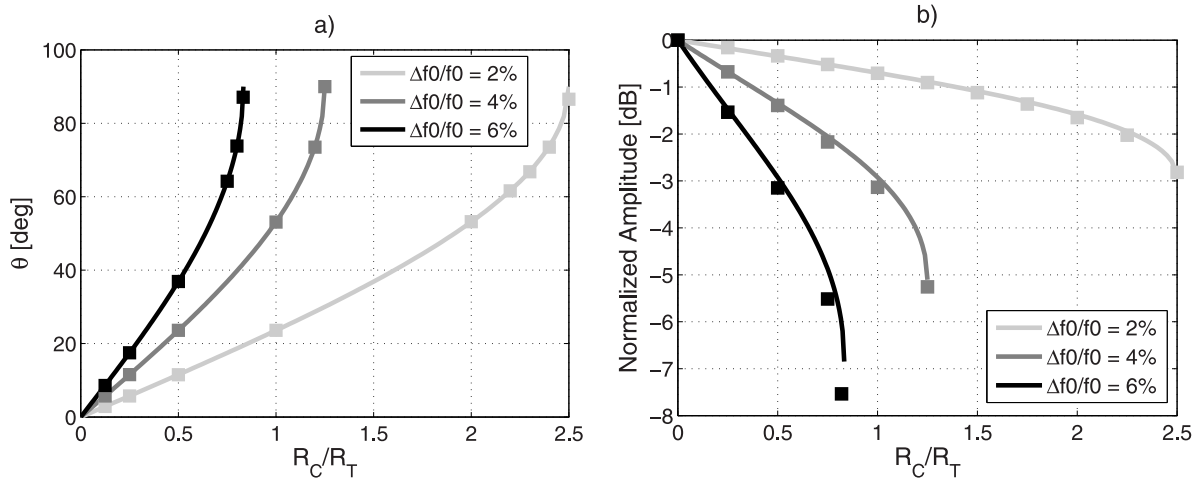

Fig. 9. (a) Phase shift between tank voltages and (b) amplitude reduction in a dual-core resistively-coupled oscillator system with $Q = 20$. Comparison between (6), (7) (solid lines) and circuit simulations (squares). Curves stop where the system loses locking.

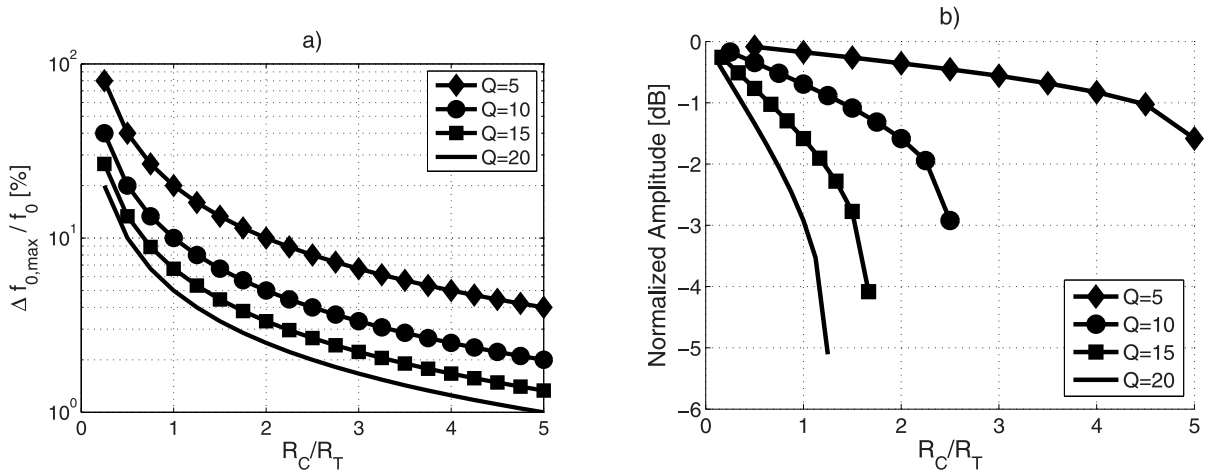

Fig. 10. (a) Calculated locking range and (b) calculated oscillation amplitude reduction in a dual-core resistively coupled oscillator as a function of R_C/R_T for different values of tank quality factor. For figure (b), $\Delta f_0/f_0 = 4\%$ was assumed, and curves stop where the system loses locking.

from (6) and (7) in Fig. 9 for 2%, 4%, and 6% frequency mismatch, showing very good agreement. Fig. 10 shows locking range and oscillation swing reduction as a result of (8) and (7), for different values of tank quality factor. Higher Q leads to lower locking range and higher swing drop, at given R_C/R_T.

Amplitude reduction and phase shift both lead to a phase-noise penalty. The effect of the amplitude reduction, leading to a phase noise penalty proportional to $1/a^2$, is evident from (2). To take into account the effect of phase shift, the phase-noise contributions from both tank resistance and cross-coupled pair were calculated for the dual-core oscillator in Fig. 7, following the approach presented in [34] and [21]. Detailed calculations are provided in Appendix B. It is found out that the phase shift among oscillators affects the Impulse Sensitivity Function [35] and yields an additional phase noise penalty approximately proportional to $1/a$.

Combining the two effects leads to the following expression for the dual-core phase noise $L_{2\text{core}}$:

$$\begin{aligned} L_{2\text{Core}}(f) &\cong L_{1\text{Core}}(f) - 3\text{dB} - 30\log a \\ &= L_{2\text{Core,Ideal}}(f) - 30\log a. \end{aligned} \tag{9}$$

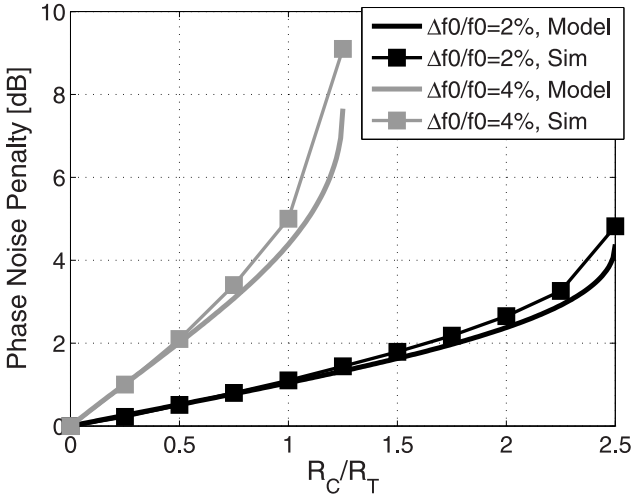

Fig. 11. $1/f^2$ phase noise penalty for a dual-core oscillator system with $Q = 20$ in presence of mismatch and finite coupling resistance. Comparison between results from (9) (solid lines) and circuit simulations (squares).

Equation (9) is compared with simulations in Fig. 11, where the phase-noise penalty versus R_C/R_T with 2% and 4% mismatch, respectively, is plotted, with very good agreement. The

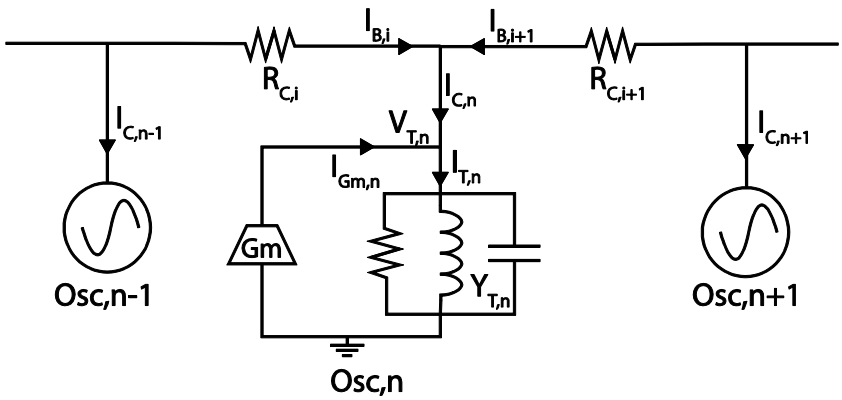

Fig. 12. Schematic of a portion of an N-core resistively-coupled oscillator system.

analysis can be extended to differential oscillators, where r is still the ratio between the coupling resistance and the single-ended tank resistance. Simulations also show a $1/f^3$ noise penalty, as in the case of QVCOs [36]. This penalty rises with tank mismatch but becomes negligible as well for low R_C/R_T values.

The dual-core model allows to gain useful insight to analyze N-core systems, where each core is connected to more than one oscillator. As shown in Fig. 12, the current $I_{C,n}$ required to shift the oscillation frequency of the nth tank from resonance is provided by the adjacent cores and satisfies

$$I_{C,n} = I_{T,n} - I_{\mathrm{Gm},n} = Y_{T,n}V_{T,n} - I_{\mathrm{Gm},n} \approx \left[\frac{1}{R_T} + j\frac{2Q}{R_T}\frac{\delta f_n}{f_{0,n}}\right]A - I_{\mathrm{Gm},n} \quad (10)$$

where $\delta f_n = f_{\mathrm{osc}} - f_{0,n}$ and $f_{0,n}$ is the resonance frequency of the nth tank. For simplicity, it was arbitrarily assumed that the tank voltage waveform $V_{T,n} = A$ is purely real. Expressing $A = aA_0 = aI_{\mathrm{Gm},n}R_T$, (10) can be simplified as

$$I_{C,n} = \frac{A_0}{R_T}\left[(a-1) + ja2Q\frac{\delta f_n}{f_{0,n}}\right]. \quad (11)$$

Now, we consider for simplicity the case of the oscillator being far from the locking-range limit, namely, $a \approx 1$. Thus, the coupling current required by the nth tank can be approximated as

$$I_{C,n} \approx j\frac{A_0}{R_T}2Q\frac{\delta f_{0,n}}{f_{0,n}}. \quad (12)$$

Therefore, each oscillator behaves as a current source which sinks or injects a current proportional to the mismatch between its resonance frequency and the overall oscillation frequency of the system. KCL implies $\sum_n I_{C,n} = 0$, from which $f_{\mathrm{osc}} = [\sum_n f_{0,n}]/N$ easily follows. Therefore, the oscillation frequency does not depend on the interconnection topology.

The coupling currents $I_{C,n}$ are distributed in the branches of the interconnection network. The current $I_{B,i}$ flows in the ith branch if the two cores connected by the branch experience a phase shift θ_i with respect to each other. This can be calculated inverting (A5), yielding

$$\theta_i = \sin^{-1}\left[\frac{R_{C,i}|I_{B,i}|}{A}\right] \approx \frac{R_{C,i}|I_{B,i}|}{A} \quad (13)$$

where the approximation holds for small θ_i. Equation (12) and (13) provide useful insights to compare different interconnection strategies in N-core oscillators to minimize phase shifts. Indeed, simulations show how minimizing the worst-case phase shift in the system leads to improved locking range and lower phase noise penalty. In Fig. 13, three different interconnection networks for the quad-core oscillator (i.e., nearest-neighbor chain coupling, nearest-neighbor ring coupling, and global coupling) are compared.[1] Each core is modeled as a current source, whose current $I_{C,n}$ is calculated through (12). The currents $I_{B,i}$ flowing in the branches of the interconnection network are derived using simple circuit analysis. Finally, according to (13), the phase shift between two adjacent cores is proportional to the voltage drop across the resistor connecting them. Resonance frequency mismatch distributions leading to worst-case phase shifts are shown in Fig. 13. The chain topology leads to $2\times$ phase shift in the central connection with respect to the ring, and it is therefore less robust. The global connection network leads to a slight improvement in worst-case phase shifts compared to the ring topology, at expense of increased complexity. Phase shift, locking range and phase-noise results have been verified through circuit simulations.

Finally, it is interesting to notice that the worst-case configuration for ring coupling in Fig. 13(b) corresponds to two identical mismatched dual-core systems coupled together [11]. Therefore, amplitude and noise penalty in the quad-core ring-coupled system can still be described by (7) and (9).

IV. Circuit Design

In the proposed 20-GHz multi-core VCO, a ring quad-core topology as shown in Fig. 13(b) was employed as a compromise between reduced phase shifts and low complexity. When designing the circuit, 5% of worst-case tank components mismatch, leading to ~2.5% relative frequency mismatch, was considered. This captures both process-dependent mismatches and systematic differences due to layout asymmetries. Simulated phase noise penalty is plotted versus size of the coupling

[1]For fair comparison, since in the network in Fig. 13(c) each core has three connections instead of two, coupling resistances have been increased by 50% with respect to Fig. 13(a) and (b), assuming interconnection switch width is reduced so as to keep the same capacitive parasitics.

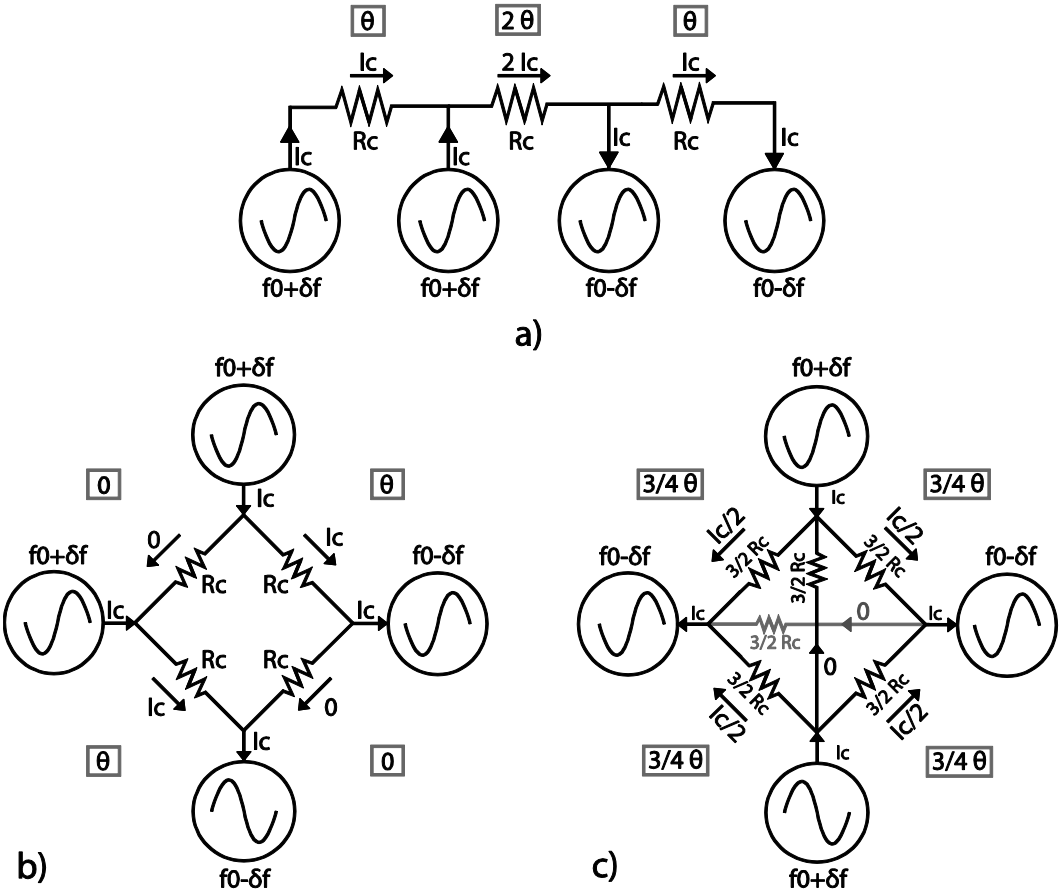

Fig. 13. Comparison between three different single-ended quad-core oscillator systems. (a) Nearest-neighbor chain coupling. (b) Nearest-neighbor ring coupling. (c) Global coupling. In each case, coupling currents are shown for the worst-case resonance frequency mismatch distribution, i.e., the one leading to the highest phase shifts. Phase shifts between voltage waveforms of neighboring cores, calculated through (13), are shown in the gray squares, assuming θ is the phase shift resulting from a current of amplitude I_C flowing in a resistance R_C.

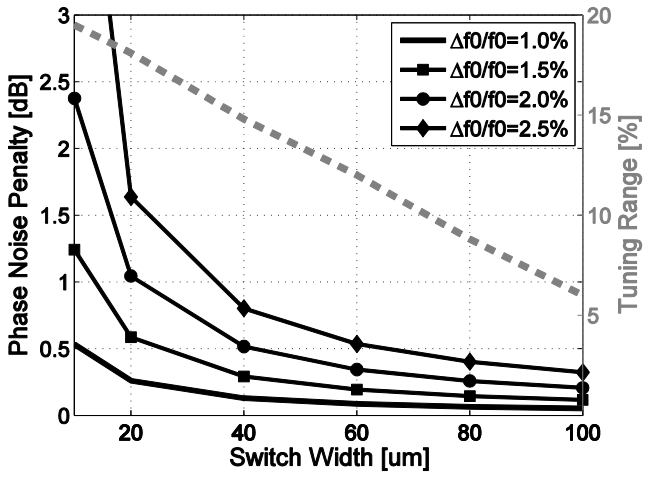

Fig. 14. Simulated phase noise penalty (black solid curves) and tuning range (gray dashed curve) of the quad-core 20-GHz oscillator when varying the coupling-switch width.

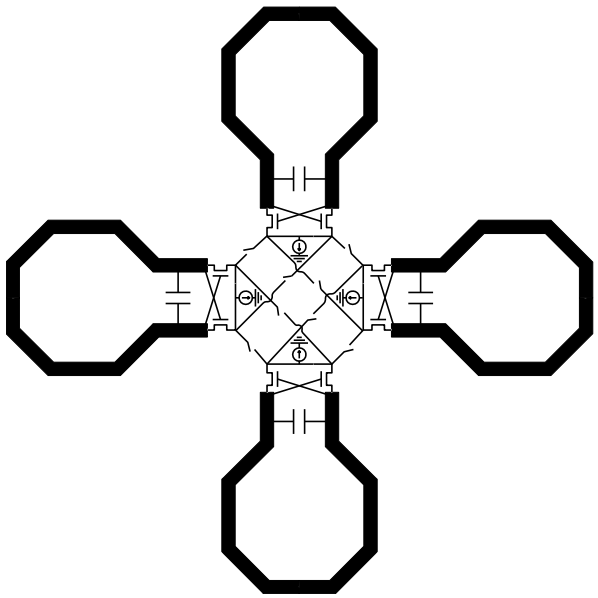

Fig. 15. Centrosymmetric layout sketch of the quad-core oscillator, without tail filters.

switches in Fig. 14, together with the tuning-range degradation due to switch capacitive parasitics. A 40 μm wide switch can keep the worst-case noise penalty below ~0.8 dB. Wider switches show only a slight reduction of noise penalty, but they significantly impact on tuning range.

Each VCO core is based on a class-B topology with tail filter [37], which allows maximum swing, and phase-noise levels close to the theoretical limit [38], [39]. Introducing millimeter-wave tail filters in the quad-core oscillator presents some implementation issues. A convenient layout for the quad-core system is depicted in Fig. 15. The centrosymmetric

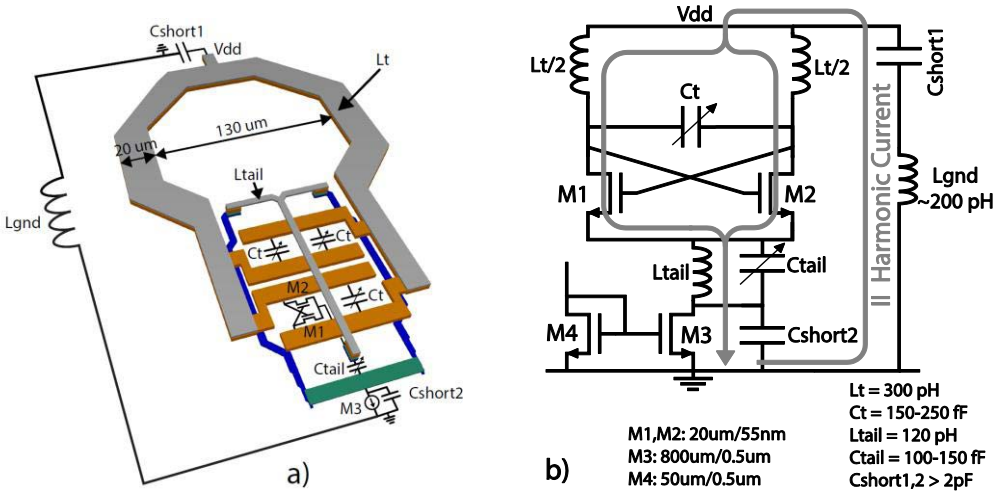

Fig. 16. (a) Layout of the resonant tail filter VCO as implemented in [11]. (b) Related oscillator schematic.

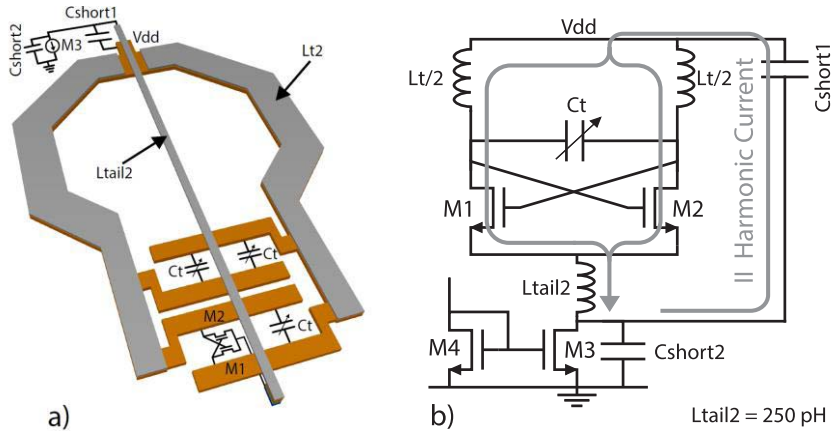

Fig. 17. (a) Layout of the inductive tail filter VCO implemented in the new prototype. (b) Related oscillator schematic.

arrangement allows minimizing interconnection length, reducing footprint, and achieving maximum symmetry. On the other hand, there is no space in the middle for tail filters.

A first solution, adopted in [11], is flipping the tail inductor on top of the capacitor bank, as shown in Fig. 16. The inductor resonates at $2f_{\rm osc}$ with the parasitic source capacitance of the cross-coupled pair and a ~100-fF tunable capacitor bank. However, this implementation presents two main drawbacks. First, the symmetric tail inductor forms a shorted loop which magnetically couples with the tank inductor on the fundamental harmonic, reducing the tank's quality factor by ~10%. Second, the ground return inductance $L_{\rm GND}$, which is hard to model and located close to the oscillator because of layout constraints, can couple with the VCO inductors and generate additional unwanted resonances, that can detune the tail resonator.

A better solution implemented in a new test chip is shown in Fig. 17. Instead of using an *LC*-shunt resonator, a ~250 pH inductor is introduced between the VCO tail node and the current source. Resonating with capacitive parasitics at the tail node at $\sim 3f_{\rm osc}$, its impedance at the second-harmonic frequency is still mostly inductive. At 40 GHz, its impedance $|Z_{L\rm Tail}| \approx 100\ \Omega$ is high enough to provide common-mode degeneration to the cross-coupled pair. The tail inductor also acts as an escape path from the center of the quad-core structure, where the cross-coupled pair is, to the outer region. The current source is hence located close to the tank inductor's center tap, minimizing the ground return inductance. In addition, the tail inductor is a straight strip lying in the middle of the tank inductor, thus not degrading the tank's quality factor.

Simulated phase noise is plotted for *LC* oscillators with different impedance conditions on the tail node, assuming an ideal current source in Fig. 18.[2] A big capacitor $C_{\rm SH}$ in parallel with the current source lowers the tail common-mode impedance (b), resulting in ~8 dB 1/f^2 noise penalty due to

[2]In all the simulations in Fig. 18, a purely single-ended tank capacitance was considered. Simulations show that a floating differential tank capacitance can lead to a slight phase noise improvement for both the resonant and inductive tail oscillator. In particular, flicker noise upconversion for an inductive-tail VCO with only (or mostly) differential tank capacitance is significantly lower than in the case depicted in Fig. 18. However, this is a rather unlikely case in high-frequency oscillators, where a significant portion of the tank capacitance is due to layout and transistor parasitics, which are mostly inherently single-ended.

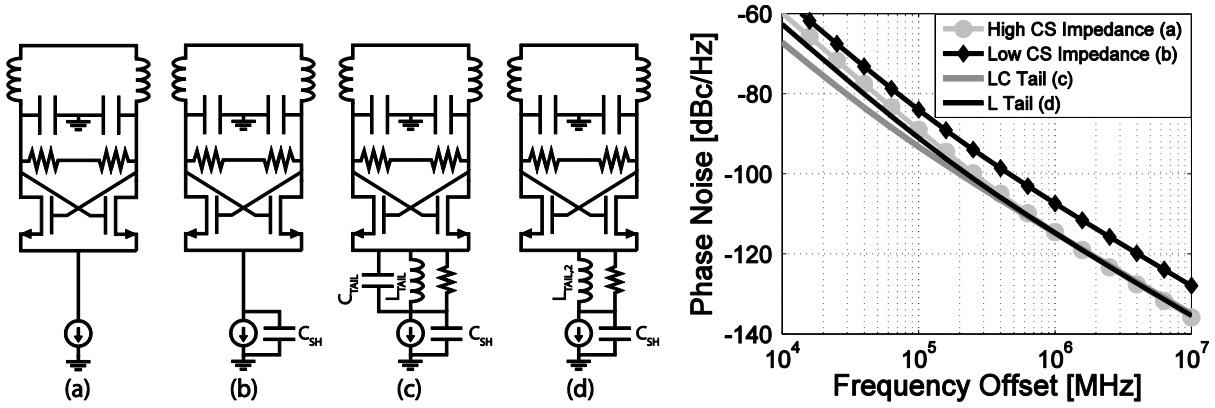

Fig. 18. Simulated phase noise spectrum for different LC oscillators at 20 GHz f_{osc}. Comparison between an oscillator with (a) ideal current source with infinite output impedance, (b) current source with a shunt capacitance $C_{SH} = 10$ pF setting a low impedance condition on the tail, (c) *LC* shunt tail filter with $L_{TAIL} = 100$ pH, resonance frequency 40 GHz (including transistor parasitics) and $Q_{TAIL} = 10$ at 40 GHz and (d) inductive tail filter with $L_{TAIL,2} = 250$ pH and $Q_{LTAIL,2} = 15$ at 40 GHz. 5-mA dc current and $Q_T = 20$ at 20 GHz was employed in all the simulations.

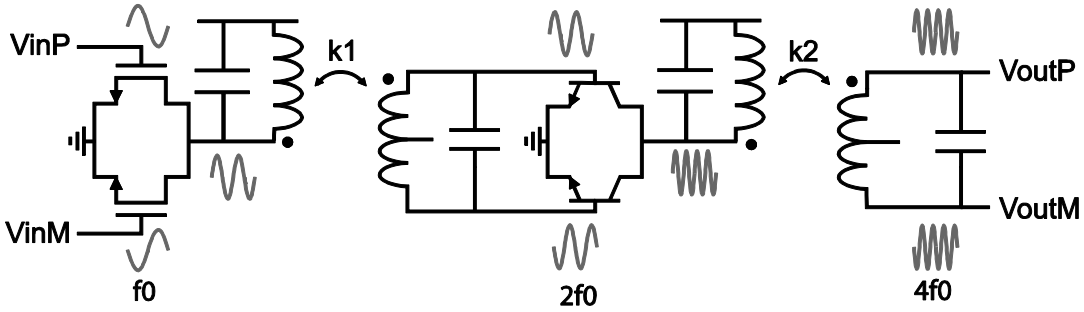

Fig. 19. Schematic of the frequency quadrupler.

loading of the tank when transistors enter triode operation [37]. Both an *LC*-shunt filter (c) or a tail inductor (d) restore a high-impedance condition on the tail node, resulting in a $1/f^2$ noise performance close to the ideal case (a). Considering further non-idealities and coupling effects cited above, the inductive tail filter as shown in Fig. 17 is more convenient in high-frequency multi-core VCOs. The *LC* shunt filter leads to lower flicker noise corner, although this effect is narrowband and highly sensitive to precise frequency alignment [40], [41].

In both prototypes, frequency control is performed through a 5-bit switched-capacitor bank, and a small varactor for fine tuning. The tank inductance is ∼300 pH, and the tank's quality factor $Q \approx 20$. Thin-oxide CMOS transistors were used for crossed-coupled pairs and tail current sources, while thick-oxide pMOS transistors are employed as coupling switches. The single-ended voltage waveform in optimal operation conditions is a sinusoid with amplitude ∼0.9 V_{DD},0-pk. Reliability issues due to time-dependent dielectric breakdown were checked using the technique and data reported in [26] and [42], resulting in > 10-year lifetime at 0.01% failure rate at 125 °C. The current waveform flowing in the cross-coupled pair is close to a square wave. Therefore, transistors are mostly turned off when the drain voltage swings above supply V_{DD}, and hot carrier injection is not expected to lead to significant performance degradation over time [42].

The VCO is followed by a frequency quadrupler, shown in Fig. 19, to generate the E-Band LO signal. The multiplier is a chain of two push-push frequency doublers. Transformer-coupled resonators are used as interstage and output networks, for bandwidth enhancement and single-ended-to-differential conversion. Details on the quadrupler design are reported in [43].

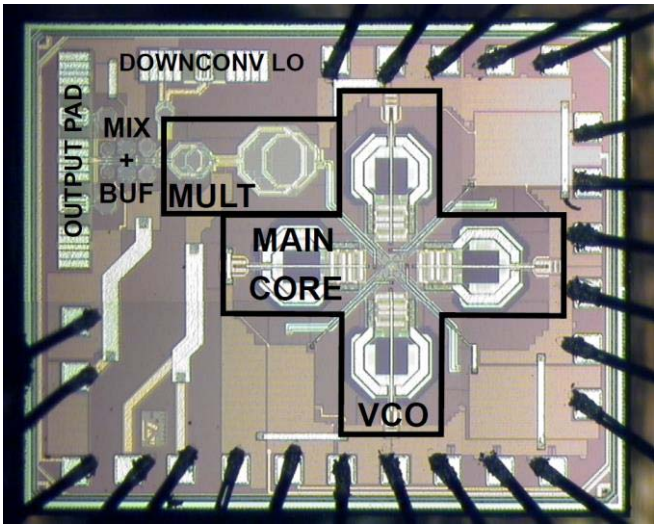

Fig. 20. Chip micrograph.

V. Measurements

Prototypes were fabricated in a 55-nm BiCMOS process by STMicroelectronics. The chip is shown in Fig. 20. Independent test structures for VCO and multipliers, not shown in the picture, were also realized. The core area is 830 × 720 μm^2. The VCO draws 9, 18, and 36 mA from 1.2-V supply in single, dual, and quad-core mode, respectively, while the frequency

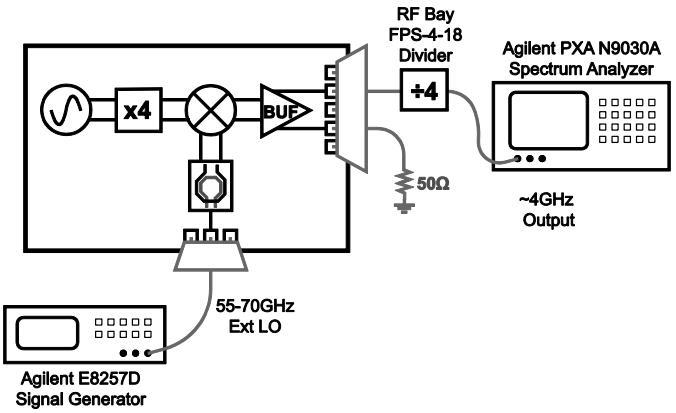

Fig. 21. Measurement setup.

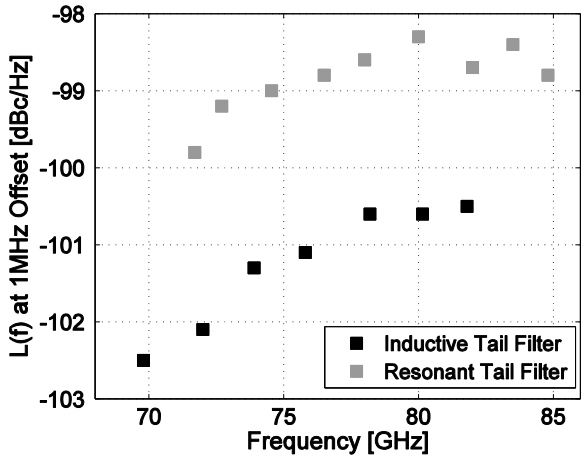

Fig. 22. Measured phase noise at 1-MHz offset over the tuning range in single-core configuration: comparison between the first design with resonant tail filter as in Fig. 16 (gray) and the second design with inductive tail filter as in Fig. 17 (black).

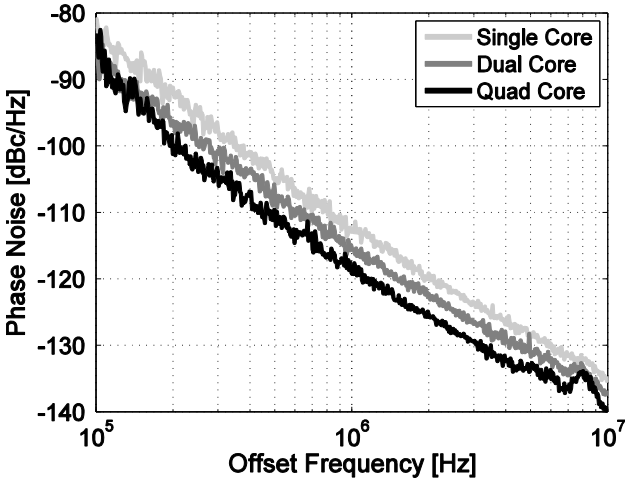

Fig. 23. Measured phase noise spectra of the VCO and multiplier chain, after downconversion and frequency division by four, at center frequency in single, dual, and quad-core configurations.

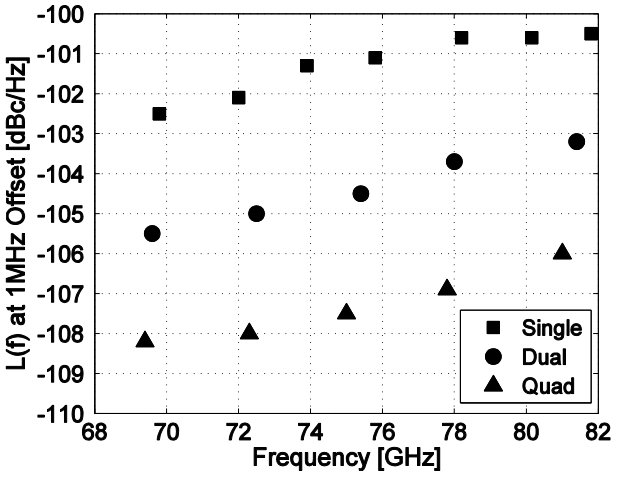

Fig. 24. Measured phase noise at 1 MHz offset over the tuning range in single (squares), dual (circles), and quad (triangles) core configuration, after external frequency divider de-embedding.

quadrupler consumes 7 mW. The E-Band output is fed to an on-chip mixer and downconverted to ∼15 GHz for measurement purposes, as shown in Fig. 21. A 55–70 GHz tone from an external signal generator is used for downconversion. The 15-GHz output is amplified by a buffer and fed to an external frequency divider-by-four, which is connected to a spectrum analyzer.

Measurements shown in this paper were performed on the chip with inductive tail filter as shown in Fig. 17. As shown in Fig. 22, this design achieves ∼2 dB lower phase noise at 1 MHz than prototype in [11], shown in Fig. 16, over the whole frequency range.

Phase-noise spectra at the divider output, with VCO working at center frequency in single, dual, and quad-core configuration are shown in Fig. 23. Significant noise reduction resulting from multi-core operation is verified. Spot phase noise at 1-MHz offset from the carrier over the tuning range, after divider de-embedding, is shown in Fig. 24. The VCO tuning range is 15%, and noise performance varies by ∼2 dB over oscillation frequency. On average, the circuit achieves −101 dBc/Hz phase noise at 1 MHz offset in single-core mode and −107 dBc/Hz in quad-core mode. Proper coupling-switch sizing results in nearly-ideal 3 and 6 dB noise reduction in dual- and quad-core operation over the tuning range, while using the same frequency tuning control for all the cores. The FoM, including power consumption of the multiplier, is plotted in Fig. 25(a) over the tuning range. Since the multiplier power is selected independently of VCO setting for noise scaling, the FoM is slightly better in quad-core configuration, where the quadrupler consumption is a smaller fraction of the total. Subtracting the multiplier power consumption from the FoM calculation, the VCO FoM has comparable values for single, dual, and quad-core configurations, as shown in Fig. 25(b).

The frequency quadrupler was also tested stand-alone, using an external signal generator as input. It achieves 27% bandwidth around 74 GHz, with ∼8 dB conversion loss and negligible phase-noise degradation. A complete measurement overview is reported in [43]. Adding a buffer stage to compensate the multiplier losses is expected to rise the synthesizer

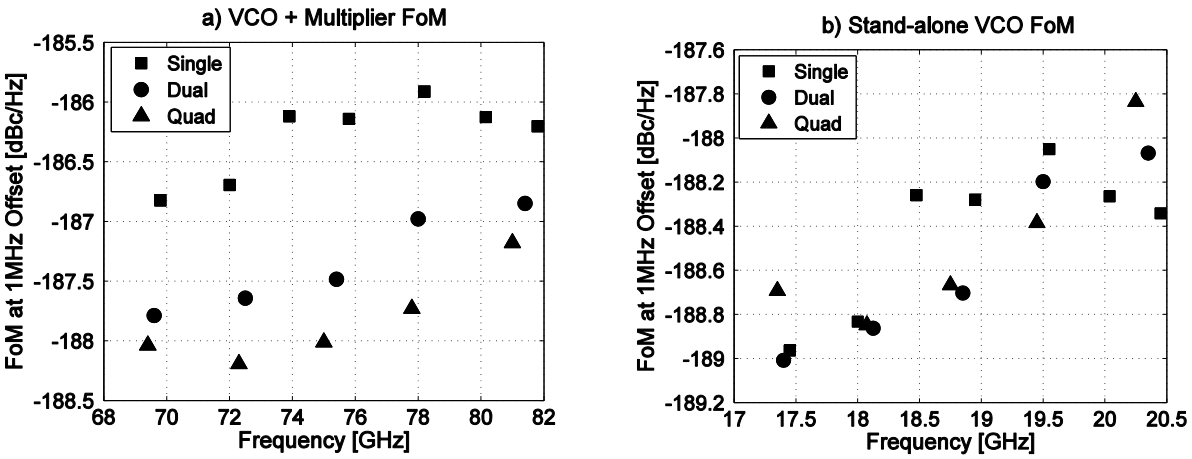

Fig. 25. (a) Measured FoM for the VCO + multiplier chain and (b) stand-alone VCO over the tuning range in single (squares), dual (circles), and quad-core (triangles) configurations.

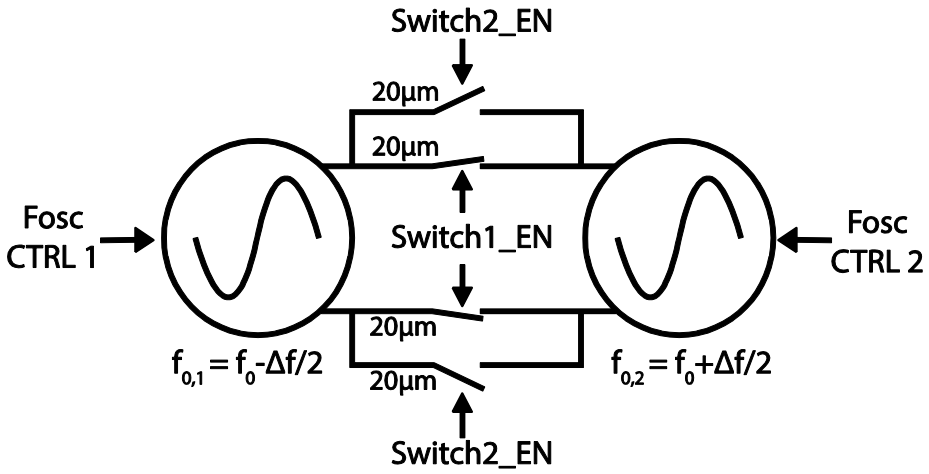

Fig. 26. Independent resonance-frequency control and coupling-switch width selection employed in the mismatch tests.

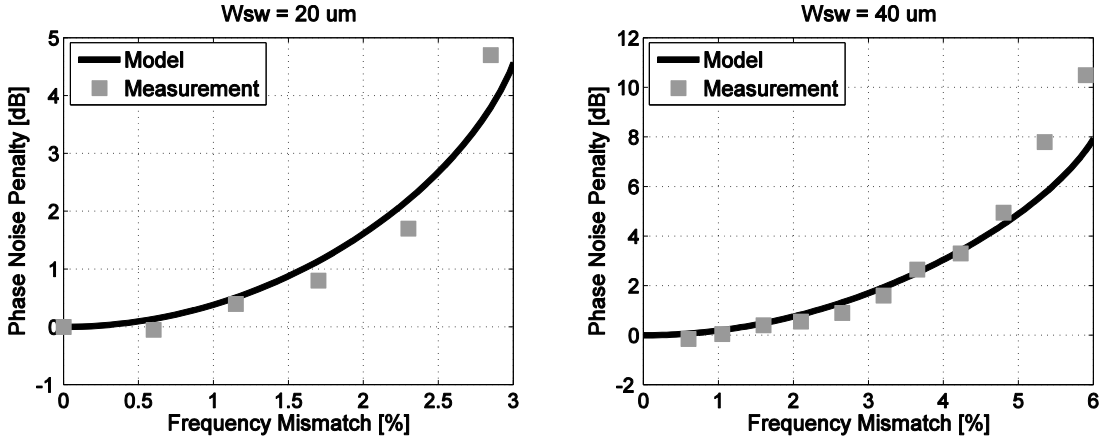

Fig. 27. Phase-noise penalty at 5-MHz offset versus resonance frequency mismatch in the dual-core oscillator, for 20 and 40 μm wide coupling switches: comparison between measured data (gray squares) and calculated values through (9) (black line). Data stop where the system loses locking.

power consumption by ~10 mW, resulting in a FoM penalty of 2 and 1 dB in single and quad-mode respectively.

As shown in Fig. 26, each VCO core has an independent control of the resonance frequency, such that a mismatch can be forced to provide experimental verification of results in Section III-B. The coupling-switch width can also be changed between 20 and 40 μm, thus varying the coupling resistance. The measured phase-noise penalty in the dual-core VCO is plotted versus frequency mismatch in Fig. 27. For both 20 and 40 μm wide switch, measured data match the model very well. Furthermore, as predicted by (8), when the switch width W_{SW} is doubled the locking range is increased

TABLE I
PERFORMANCE OVERVIEW AND COMPARISON

	This work (single)	**This work (quad)**	[12]	[13]	[14]	[10]	[45]	[46]
Tech	**BiCMOS 55nm**	**BiCMOS 55nm**	BiCMOS 130nm	BiCMOS 180nm	BiCMOS 130nm	CMOS 130nm	CMOS 90nm	CMOS 40nm
Fout [GHz]	**80**	**80**	62	52.5	92.7	53.6	57.6	60
Tuning Range	**15%**	**15%**	4.7%	26.5%	8.3%	16.8%	9%	25%
Phase Noise at 1MHz [dBc/Hz]	**-100.5**	**-106.5**	-106	-108	-102	-100.6	-102	-100
Eq. Phase Noise° at 1MHz from 80GHz [dBc/Hz]	**-100.5**	**-106.5**	-103.8	-104.3	-103.3	-97.1	-99.2	-97.5
Vdd [V]	**1.2**	**1.2**	3	3	3.3	1.2	0.6	0.7/1
Pdc [mW]	**18**	**50**	39	132	90	7.6	7.2	24
FoM [dBc/Hz]	**-186**	**-187.5**	-185.6	-181.2	-181.8	-186.3	-189	-181.5
FoM_T [dBc/Hz]	**-189.5**	**-191**	-179	-189.6	-180.2	-190.85	-188	-189.6
Output	**Diff**	**Diff**	SE	SE	Diff	Diff	Diff	Diff
Area [mm^2]	**0.6**	**0.6**	0.17	0.1*	0.05*	0.2	0.035	0.13

° EqPhaseNoise=PhaseNoise@1MHz+$20\log_{10}$(80GHz/Fosc)

* Estimated from chip photograph

FoM = PhaseNoise - $20\log_{10}(f_0/\Delta f)$ + $10\log_{10}$(Pdc/1mW)

FoM_T = FoM + $20\log_{10}$(TR/10)

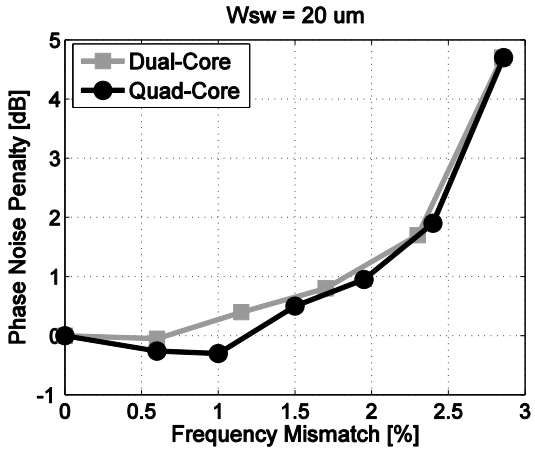

Fig. 28. Measured phase-noise penalty at 5-MHz offset versus resonance frequency mismatch, for 20 μm wide coupling switches: comparison between dual-core (gray) and quad-core mode (black). The worst-case mismatch distribution shown in Fig. 13(b) was used for the quad-core oscillator.

by ~2. Mismatch tests were performed at both minimum and maximum oscillation frequency, showing consistent results. Finally, noise penalty versus frequency mismatch in quad-core configuration, using the worst-case configuration in Fig. 13(b) is plotted in Fig. 28. Measurements confirm that the worst-case noise penalty for a ring-coupled quad-core VCO is comparable to the one of a dual-core system.

Table I reports comparison with state of the art. Phase-noise performance reported in literature has been normalized at 1 MHz offset from 80-GHz carrier. Mm-Wave synthesizers displaying phase noise below or close to −100 dBc/Hz are reported. The proposed circuit achieves the lowest equivalent phase noise at 80 GHz, with very competitive FoM and FoM_T. Moreover, the circuit features noise scaling up to 6 dB, with only 1.5-dB FoM variation.

VI. CONCLUSION

A 20-GHz quad-core VCO followed by a frequency quadrupler for E-Band frequency generation in 55-nm BiCMOS is presented. The system achieves very-low-noise performance at mm-Waves and meets requirements for E-Band 64QAM communications with 4–5 dB margin, enough to guarantee negligible SNR degradation over process corners. The proposed multi-core VCO allows power-efficient noise scaling, a useful feature in adaptive-modulation wireless links.

Multi-core VCOs were studied in depth, developing an analytical model to understand and predict the effect of component mismatch on phase-noise performance. The model also provides useful insights on how to compare different interconnection strategies in resistively-coupled oscillators. The proposed design is scalable to even larger oscillator arrays, leading to 3-dB phase-noise improvement every 2x increase in the number of cores, at expense of additional area consumption and complexity.

APPENDIX A

In this appendix, (5)–(8) are derived. Referring to Fig. 8 and assuming $Q_1 \cong Q_2 = Q$ and $|I_{Gm1}| = |I_{Gm2}| = |I_{Gm}|$, the following equations link the *LC*-tank voltages and currents:

$$I_{T1} = I_{Gm1} + I_C = V_{T1}Y_{T1} \tag{A1}$$

$$I_{T2} = I_{Gm2} - I_C = V_{T2}Y_{T2} \tag{A2}$$

where Y_T is given by (4) and $I_C = (V_{T2} - V_{T1})/R_C$. Two conditions follow from (A1) and (A2):

$$\angle Y_{T1} = -\angle Y_{T2} \tag{A3}$$

$$|V_{T1}Y_{T1}| = |V_{T2}Y_{T2}|. \tag{A4}$$

Equation (A3) and (4) yield $\delta f_1 = -\delta f_2$, leading to (5). This result proves that the oscillation frequency, and therefore $\angle Y_T$, does not depend on the coupling resistance. Also,

combining (A4), (4), and (5) we obtain $|V_{T1}| = |V_{T2}| = A$, as in (7).

Choosing the tank voltage phases such that $V_{T1} = A$ and $V_{T2} = Ae^{j\theta}$, the coupling current is

$$I_C = 2\frac{A}{R_C}\sin\left(\frac{\theta}{2}\right)e^{j\left(\frac{\pi}{2}+\frac{\theta}{2}\right)}. \tag{A5}$$

Replacing (A5) in (A1), and solving (A1) for magnitude and phase yields

$$\frac{\sin\theta}{\frac{r}{a}-1+\cos\theta} = K \tag{A6}$$

$$\left[\frac{1}{a}+\frac{\cos\theta-1}{r}\right]^2+\left[\frac{\sin\theta}{r}\right]^2 = 1+K^2 \tag{A7}$$

where $K = Q(\Delta f/f_0)$, $r = R_C/R_T$ and $a = A/A_0$. The system can be solved analytically, leading to (6) and (7) for θ and a. Solutions are found provided $r \le 1/|K|$, from which (8) follows.

APPENDIX B

In this appendix, the phase-noise expression in (9) is derived. First, we derive expressions for the tank ISF, following the approach proposed in [34] for a QVCO, based on Kärtner's phase noise theory [44]. State variables in the dual-core oscillator of Fig. 7 are capacitor voltages $V_{C1,2}$ and inductor currents $I_{L1,2}$. We define $V_{C1,2-0}$ and $I_{L1,2-0}$ the corresponding variables at steady state. The oscillator is described by the following set of differential equations:

$$\dot{V}_{C1} = \frac{1}{C_1}\left[-\frac{V_{C1}}{R_1}+I_{\mathrm{Gm1}}(V_{C1})\right]-\frac{I_{L1}}{C_1}+\frac{1}{C_1}\left[\frac{V_{C2}-V_{C1}}{R_C}\right] \tag{B1}$$

$$\dot{I}_{L1} = \frac{1}{L_1}V_{C1} \tag{B2}$$

$$\dot{V}_{C1} = \frac{1}{C_2}\left[-\frac{V_{C2}}{R_2}+I_{\mathrm{Gm2}}(V_{C2})\right]-\frac{I_{L2}}{C_2}-\frac{1}{C_2}\left[\frac{V_{C2}-V_{C1}}{R_C}\right] \tag{B3}$$

$$\dot{I}_{L2} = \frac{1}{L_2}V_{C2}. \tag{B4}$$

At steady state, tank voltages V_{C1-0} and V_{C2-0} can be derived from (5)–(7), yielding

$$V_{C1-0} = aA_0\sin(\omega_{\mathrm{osc}}t) \tag{B5}$$

$$V_{C2-0} = aA_0\sin(\omega_{\mathrm{osc}}t+\theta) \tag{B6}$$

where $\omega_{\mathrm{osc}} = 2\pi f_{\mathrm{osc}}$, whereas currents I_{L1-0} and I_{L2-0} can be calculated by integrating (B2) and (B4). Next, we derive from simulations the following guess solutions for the ISF on the two tanks:

$$\Gamma_1 = B\cos(\omega_{\mathrm{osc}}t+\psi) \tag{B7}$$

$$\Gamma_2 = B\cos(\omega_{\mathrm{osc}}t+\theta-\psi) \tag{B8}$$

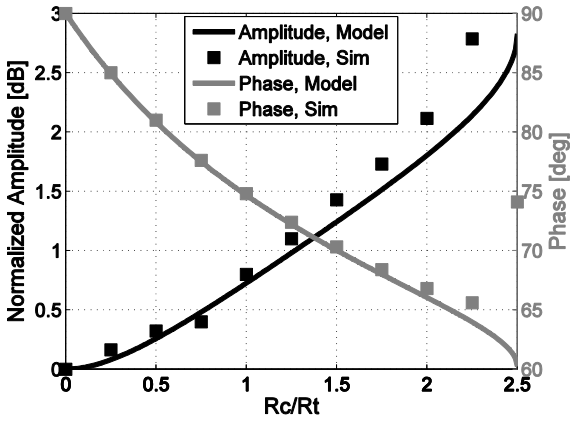

Fig. 29. Tank ISF fundamental-harmonic phase (gray) and magnitude (black) in a resistively coupled dual-core oscillator with $\Delta f/f_0 = 2\%$ and $Q_T = 20$: comparison between (B7), (B9), (B10) and circuit simulations.

where B and ψ are unknown terms varying with mismatch and coupling resistance.[3] Following [34], replacing the QVCO expressions for state variables and ISF with (B1)–(B8), it is verified that (B7) and (B8) solve Kärtner's equations, and the following solutions for B and ψ are derived:

$$\psi = \tan^{-1}\left[\frac{2K}{1+\frac{1}{r}+\frac{\sqrt{1-(\mathrm{Kr})^2}}{r}}\right] \tag{B9}$$

$$B = \frac{1}{2\cos\psi}. \tag{B10}$$

As verified in Fig. 29, results agree very well with circuit simulations. Equation (B7)–(B10) show that in a resistively-coupled dual-core oscillator the ISF is no more in quadrature with the tank voltage in presence of mismatches. Following [35], the ith tank resistor contribution to phase noise, usually referred to as effective noise, is calculated as

$$N_{L,R} = \frac{1}{T_0}\int_0^{T_0} i_{n,i}^2\Gamma_i^2 dt = \frac{kT}{R_T}\frac{1}{2(\cos\psi)^2} \approx \frac{kT}{R_T}\frac{1}{2a} \tag{B11}$$

where we assumed $R_1 \approx R_2 = R_T$ and $(\cos\psi)^2 \approx a$ as follows from (B9) assuming $\Delta f_0/f_0 << 1$.

Calculation of the phase-noise contribution of the transconductor is more involved, since the time-variant transconductance $G_m(t)$ yields a cyclo-stationary noise power spectral density (PSD) $i_{n,\mathrm{Gm}}^2$. Following [21] and considering a generic periodic current waveform $I_{\mathrm{Gm}} = \sum_n I_n\cos(n\omega_{\mathrm{osc}}t+\phi_n)$ flowing in each transconductor, the noise PSD can be calculated as

$$\begin{aligned} i_{n,\mathrm{Gm}}^2 &= 4kT\gamma\, G_m(t) = 4kT\gamma\frac{\partial I_{\mathrm{Gm}}}{\partial V_T} \\ &= 4kT\gamma\frac{\sum_n nI_n\cos(n\omega_{\mathrm{osc}}t+\phi_n)}{aA_0\cos(\omega_{\mathrm{osc}}t)}. \end{aligned} \tag{B12}$$

[3] It is interesting to notice from (B7), (B8) that, unlike in QVCOs, the ISFs of the two tanks in a frequency-mismatched resistively-coupled dual-core oscillator experience opposite-polarity phase shifts with respect to the tank voltage waveform. It is also verified that ISFs with equal phase shift for both tanks, like the ones derived for QVCOs in [44], do not solve Kärtner's equations for the system we are considering.

We may now calculate $N_{L,\mathrm{Gm1}}$ for tank 1 replacing (B12) in the integral of (B11), yielding

$$N_{L,\mathrm{Gm1}} = \frac{4kT\gamma}{4(\cos\psi)^2}\frac{1}{T_0}\int_0^{T_0}\frac{\sum_n nI_n\cos(n\omega_{\mathrm{osc}}t+\phi_n)}{aA_0\cos(\omega_{\mathrm{osc}}t)} \times[\cos(\omega_{\mathrm{osc}}t+\psi)]^2dt. \quad \text{(B13)}$$

Assuming the fundamental harmonic of I_{Gm} is in phase with V_T, i.e., $\phi_1 = 0$, after trigonometric expansion and integration (B13) can be rewritten as

$$N_{L,\mathrm{Gm1}} = \frac{4kT\gamma}{4(\cos\psi)^2} \times\left\{\frac{I_1}{2aA_0}[(\cos\psi)^2-(\sin\psi)^2] +(\sin\psi)^2\frac{1}{T_0}\int_0^{T_0}G_m(t)dt\right\}. \quad \text{(B14)}$$

Assuming hard-switching transconductors, I_{Gm} is a square wave, i.e., the transconductor is on only during zero crossings, and $G_m(\varphi)$ can be written as [34]

$$G_{m,\mathrm{HardSwitch}} = \frac{\pi}{2}\frac{I_1}{aA_0}\left[\delta(\varphi)+\delta\left(\varphi-\frac{\pi}{2}\right)\right]. \quad \text{(B15)}$$

Replacing (B15) in the integral in (B14) yields

$$N_{L,\mathrm{Gm1,HardSwitch}} = \frac{4kT\gamma}{4(\cos\psi)^2}\frac{I_1}{2aA_0}(\cos\psi)^2 = \frac{kT\gamma}{2}\frac{I_1}{aA_0} = \frac{kT}{R_T}\frac{\gamma}{2a}. \quad \text{(B16)}$$

The ratio between noise contribution of transconductor and tank is therefore given by

$$\frac{N_{L,\mathrm{Gm}}}{N_{L,R}} = \gamma\frac{(\cos\psi)^2}{a}\approx\gamma. \quad \text{(B17)}$$

The phase noise of the dual-core oscillator, neglecting the contribution from biasing components well rejected by the tail filter, can now be calculated as [35]

$$L(f) = 10\log\left[\frac{2(N_{L,R}+N_{L,\mathrm{Gm}})}{2\omega_{\mathrm{osc}}^2A^2C_T^2}\right] = 10\log\left[\frac{1}{2}\frac{4kTR_T}{A_0^2}\left(\frac{f_{\mathrm{osc}}}{2Qf}\right)^2\frac{1}{a^3}(1+\gamma)\right] \quad \text{(B18)}$$

from which (9) follows.

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