

# A Compact Broadband Mixed-Signal Power Amplifier in Bulk CMOS With Hybrid Class-G and Dynamic Load Trajectory Manipulation

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**Abstract**—This paper presents a mixed-signal power amplifier (PA) with real-time hybrid Class-G and dynamic load trajectory manipulation (DLTM) operation that achieves PA efficiency enhancement into the deep power back-off (PBO) region. Moreover, we dynamically manipulate the PA load impedance trajectory that travels from the optimum output power ( $P_{out}$ ) load impedance to the optimum efficiency load impedance during PBO, which creates PA PBO efficiency peaking. The introduced digitally intensive mixed-signal PA architecture enables precise and optimum real-time hybrid PA operation and ensures both PA output amplitude and phase accuracy. DLTM operation also extends the PA RF carrier bandwidth. A prototype PA is fully integrated in a standard 65-nm bulk CMOS process. Its load modulation network is realized by an on-chip compact transformer balun and two on-chip switch-controlled capacitors. The PA achieves +24.6-dBm (+24.4-dBm) peak  $P_{out}$  and 45.6% (45.8%) maximum drain efficiency (DE) at 2.4 GHz (2.8 GHz). DLTM operation extends the PA  $P_{out}$  and 1-dB bandwidth from 41.7% to 53.8%. By combining the real-time hybrid Class-G and DLTM operation with mixed-signal linearization, the PA delivers +17.6/+17.3-dBm (+17.3/+17-dBm) 10M-Sym/s 64QAM/256QAM at 2.4 GHz (2.8 GHz) with 27.5/26.7% (26.2/24.1%) DE, -29.2/-30.4-dB (-31.3/-31.5 dB) rms error vector magnitude (EVM), and -25.3/-25.1-dBc (-26.4/-26.1-dBc) adjacent channel leakage ratio (ACLR). The total chip area is 1.9 mm<sup>2</sup>.

**Index Terms**—Broadband, Class-G, CMOS integrated circuits, compact, efficiency, hybrid, linearity, load modulation (LM), mixed signal, polar modulation, power amplifier (PA), power back-off (PBO), reconfigurable, transformer.

## I. INTRODUCTION

TO ACHIEVE high data rates with limited spectrum resources, modern wireless standards often employ spectrally efficient modulations such as high-order quadrature amplitude modulation (QAM) and orthogonal-frequency-division modulation (OFDM) [1], [2]. These modulations may likely be further exploited in next-generation wireless

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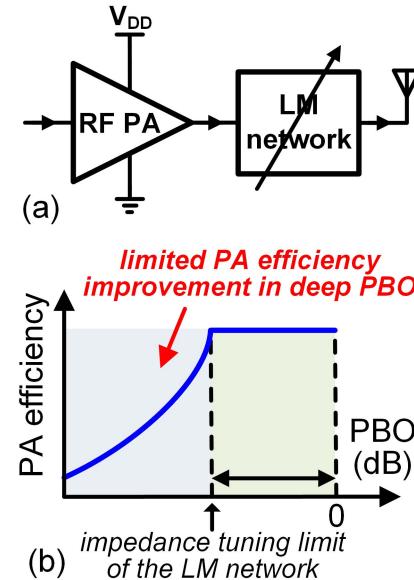


Fig. 1. (a) Diagram of a conventional LM PA. (b) Theoretical PA efficiency curve of a LM PA using a LM network with a finite ITR.

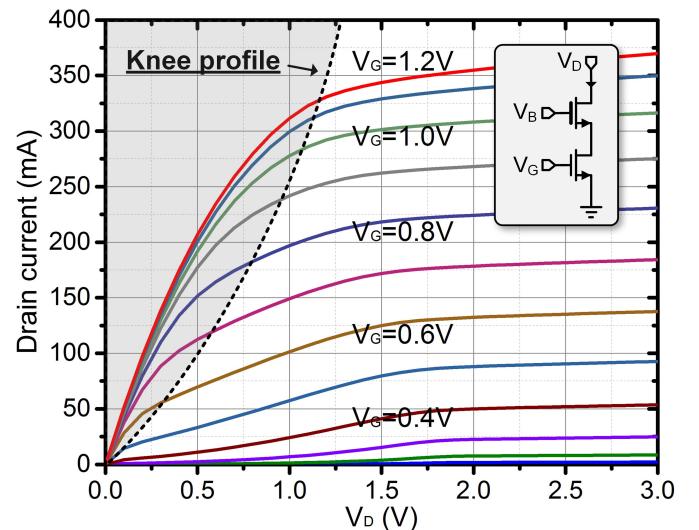


Fig. 2. Simulated  $I$ - $V$  characteristic of a cascode MOSFET circuit.

links such as fifth-generation (5G) systems [3]. However, these modulations exhibit large peak-to-average power ratios (PAPRs). Moreover, additional power back-off (PBO) for transmitter power control is often required [4]. Thus, modern

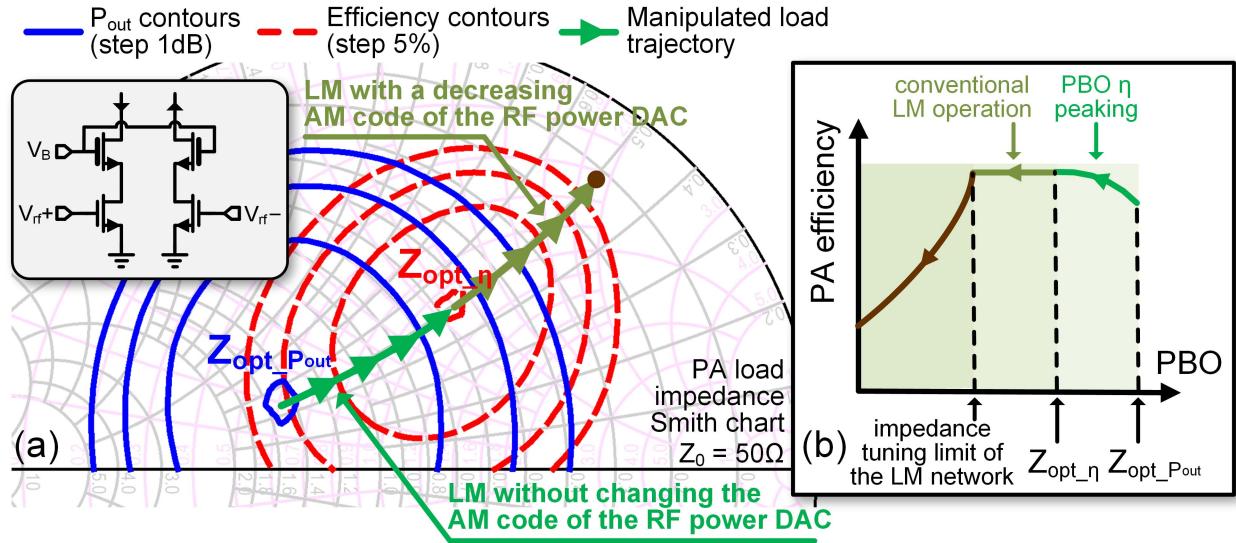


Fig. 3. (a) DLTM operation achieving PA PBO efficiency peaking and (b) its theoretical efficiency curve. The large-signal load-pull simulation results of the cascode circuit in Fig. 2 are used here for illustration. The circuit operates in a push-pull Class-D<sup>-1</sup> configuration at 2.4 GHz.

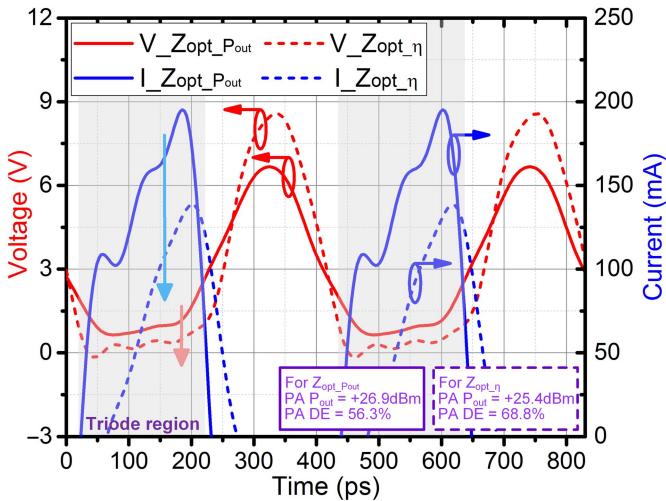


Fig. 4. Simulated drain current and voltage waveforms of the cascode circuit in Fig. 2 when it operates in the push-pull Class-D<sup>-1</sup> configuration. Results for  $Z_{\text{opt},\eta}$  and  $Z_{\text{opt},P_{\text{out}}}$  as the fundamental load impedance are compared. Even and odd harmonics are terminated as open and short-to-ground up to the sixth and fifth harmonics, respectively.

wireless transmitters routinely operate in PBO, or even deep PBO, necessitating high power amplifier (PA) PBO efficiency and linearity that ensure the battery life and quality of service (QoS) of mobile devices [1], [2].

Classic PA PBO efficiency enhancement techniques achieve limited efficiency enhancement in deep PBO in practice. Analog PAs with dynamic biasing [5], [6] and basic digital PAs using RF power digital-to-analog converters (DACs) [7]–[12] reduce PA dc current in PBO and achieve limited PBO efficiency enhancement. For example, an RF power DAC only achieves Class-B-like PBO efficiency. Direct polar (DP) [13]–[16] and envelope tracking (ET) [17]–[20] PAs save the PA dc power consumption in PBO by dynamic power supply [21]. However, linear supply modulators entail

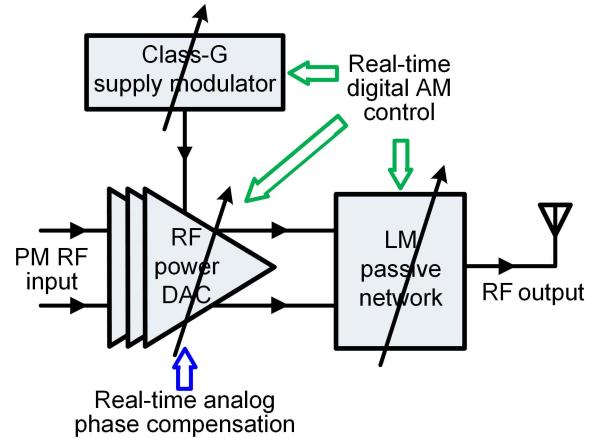


Fig. 5. Mixed-signal hybrid Class-G and DLTM PA architecture.

stringent design trade-offs among efficiency, dynamic range, and speed in practice [22]–[24]. As a result, amplifying high-PAPR signals with large modulation rates has become increasingly challenging for DP and ET PAs. Outphasing PAs [25]–[30] suffer the overhead of generating high-speed outphasing signals. Moreover, non-isolating outphasing networks are preferred for higher power combining efficiency in PBO, which, however, often lead to degraded PA linearity in PBO. Doherty [31]–[39] and load modulation (LM) PAs [40]–[53] adjust the PA load impedance during PBO to boost the PA efficiency, either by active load pulling or tunable passive networks. Conventional Doherty PAs suffer non-ideal cooperation between the main and auxiliary paths in practice. Although this is addressed by digital Doherty PA architectures [36]–[38], the commonly used two-way Doherty topology has inherently limited efficiency enhancement in deep PBO and requires a footprint of at least two transformers in state-of-the-art on-chip Doherty output network designs [38], [39]. Modified Doherty topologies such

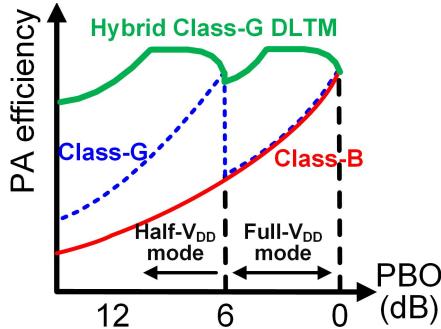


Fig. 6. Theoretical efficiency curve of the hybrid Class-G and DLTM PA.

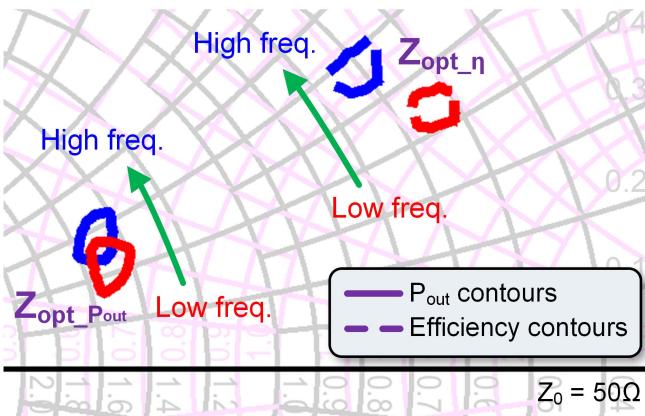


Fig. 7. Load-pull simulation results at different carrier frequencies (2.1 and 2.8 GHz) for the cascode circuit in Fig. 2 when it operates in the push-pull Class-D<sup>-1</sup> configuration.

as multi-way and multi-stage Doherty PAs [32]–[35] improve the deep PBO efficiency at the expense of more complicated, lossy, and area-extensive output networks. LM PAs entail stringent design trade-offs among the complexity, area, loss of the LM passive networks and the PA efficiency-enhanced power range [42], [50]. Moreover, conventional LM operation often causes substantial gain and phase nonlinearity, resulting in the limited success of reported LM PAs for sophisticated and high-speed modulations.

Recently, there is an increasing interest in exploring hybrid PA architectures that synergistically combine multiple PA techniques in one PA design and achieve superior PA performance [54]–[61]. To address the challenges of PBO efficiency/linearity and to further explore the potential of hybrid PAs, we introduce a mixed-signal PA architecture with the real-time hybrid operation of Class-G and dynamic load trajectory manipulation (DLTM) [62]. The introduced hybrid technique brings the following advantages. First, Class-G operation substantially relaxes the required impedance tuning range (ITR) of the LM network, allowing for a compact and low-loss transformer-based LM network that occupies only a single-transformer footprint. Second, DLTM enables PA efficiency enhancement in both Class-G supply modes. Furthermore, a new DLTM operation achieves PA efficiency peaking during PBO as well as PA carrier bandwidth extension. Mixed-signal digitally intensive PA operation

ensures the PA output accuracy, including both amplitude and phase aspects. Section II presents the PA architecture. Sections III and IV show the implementation details and measurement results, respectively.

## II. MIXED-SIGNAL HYBRID CLASS-G AND DLTM PA ARCHITECTURE

### A. Review of Class-G and LM PAs

Different from DP and ET PAs that use linear supply modulators for analog dynamic supply, a Class-G PA switches its supply among discrete voltage levels based on the instantaneous PA output power ( $P_{\text{out}}$ ) [63]–[65]. Such digitized supply modulation scheme simplifies the design and potentially allows high modulation rates. However, there is no PBO efficiency improvement in each Class-G supply mode. Moreover, Class-G supply switching often adversely impacts PA linearity by causing gain and phase discontinuities, which require significant linearization circuit overhead in analog Class-G PAs [66].

LM PAs improve PA PBO efficiency by directly changing the PA load impedance using tunable LM passive networks [Fig. 1(a)] [40]. For a PA with a fixed load, a decreasing RF voltage swing at the device output in PBO leads to its efficiency degradation. For example, (1) shows the theoretical efficiency of a Class-B PA, in which  $v_{\text{output}}$  is the RF voltage amplitude at the device output, and  $\eta_{\text{peak}}$  is the PA efficiency at the peak  $P_{\text{out}}$ . The PBO efficiency of a Class-B PA is proportional to  $v_{\text{output}}$ , i.e., the square root of the PBO ratio ( $P_{\text{out}}/P_{\text{peak}}$ ). LM PAs enhance the PA PBO efficiency by changing the PA load impedance in PBO and maintaining a constant  $v_{\text{output}}$ . Thus, the PA load impedance of a LM PA approximately moves along a constant-susceptance circle on the Smith chart during PBO.

$$\eta = (v_{\text{output}}/V_{\text{DD}}) \cdot \eta_{\text{peak}} = \sqrt{P_{\text{out}}/P_{\text{peak}}} \cdot \eta_{\text{peak}} \quad (1)$$

Doherty and outphasing PAs need the cooperation of at least two power amplification paths, necessitating complex power combining networks. However, LM PAs only need one signal path, substantially simplifying the design. In addition, LM PAs potentially enhance the PA efficiency to very large PBO levels, which is challenging even for ideal Doherty PAs.

However, in practice, the efficacy of a LM PA is constrained by various design limitations, particularly the LM network design. The efficiency-enhanced power range of a LM PA is directly determined by the LM network's ITR [Fig. 1(b)]. Using a LM network capable of tuning the load conductance by  $c \times$ , a LM PA theoretically enhances the efficiency up to  $10\log_{10}c$  dB PBO. This leads to practical design trade-offs among the complexity, area, and loss of the LM network together with the PA efficiency-enhanced power range [42], [50]. A simple  $L$ -network can perform load tuning within only a single-inductor footprint but with very limited load tuning capability [67]. By adding a second tuning capacitor, a  $\Pi$ - or  $T$ -network has a substantially extended ITR. However, it often exhibits high passive loss to achieve a large ITR, since its intermediate impedance need to travel through the high-Q region on the Smith chart [67]. A high-order ladder

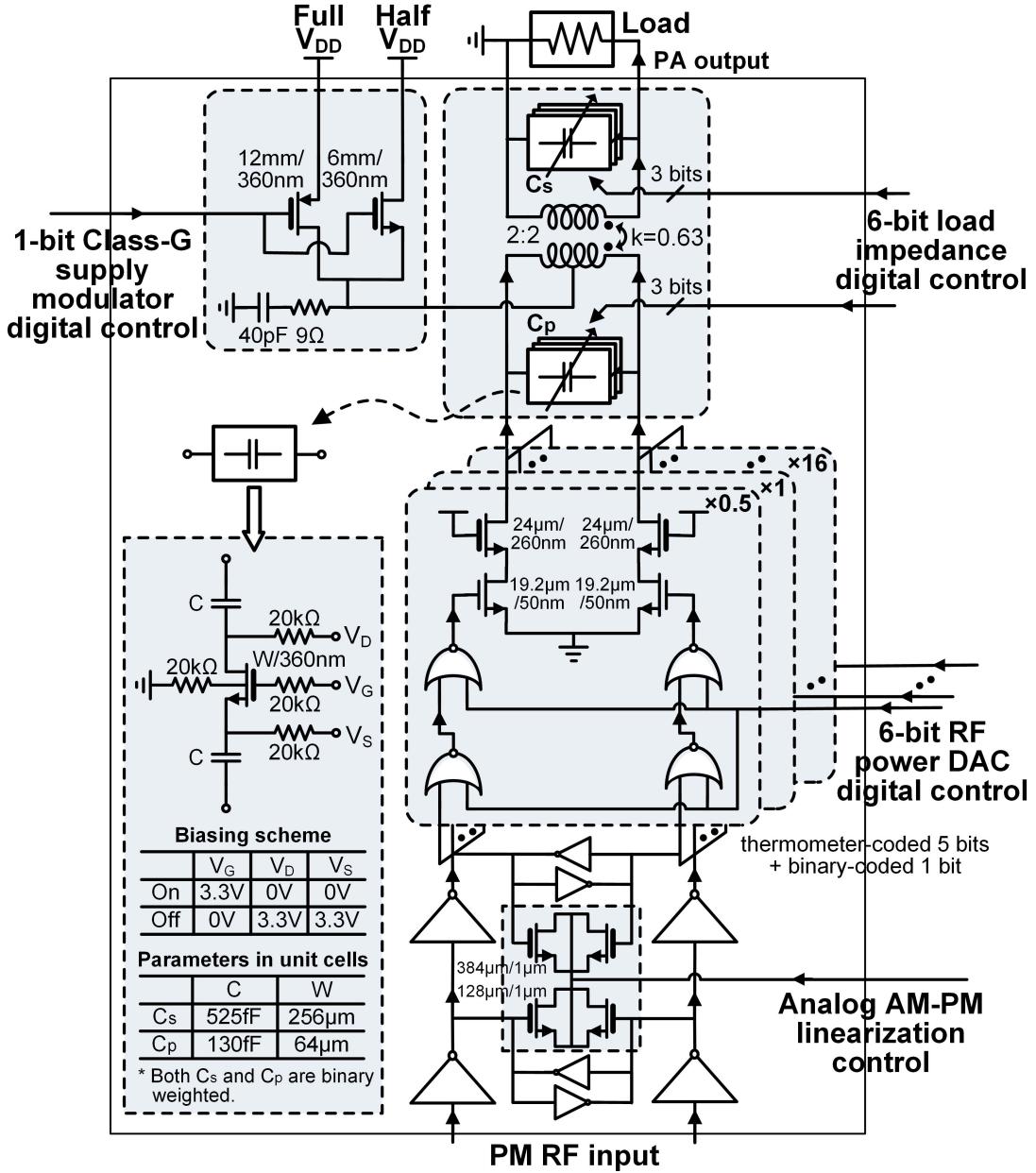


Fig. 8. Simplified schematic of the PA prototype implementation in a standard 65-nm CMOS process.

network using several  $L$ -networks in cascade mitigates this issue at the expense of a larger footprint. A transformer-based LM network can form a high-order network within only a single-transformer footprint, outperforming  $L$ -,  $\Pi$ -, and  $T$ -networks. However, its ITR is still limited when considering the passive loss, which is particularly important in LM PA designs.

In addition, the PA LM network should properly handle the large voltage swing at the PA output to ensure PA reliability and linearity. Therefore, many PA LM networks are realized in technologies that are not compatible with bulk CMOS, e.g., microelectromechanical system [41], silicon on glass [42], and silicon on insulator [44].

More importantly, LM PAs often exhibit compromised gain and phase linearity in practice. Imperfect cooperation between

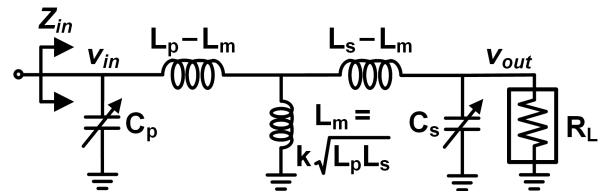


Fig. 9. Analysis model of the on-chip transformer-based LM network.

the PA core and the LM network directly leads to PA amplitude modulation (AM)-AM distortions. The phase response of the LM networks often varies drastically during LM operation, resulting in PA AM-phase modulation (PM) distortions. Phase-invariant LM networks are often complicated, bulky, and not suitable for CMOS integration [42]. As a result,

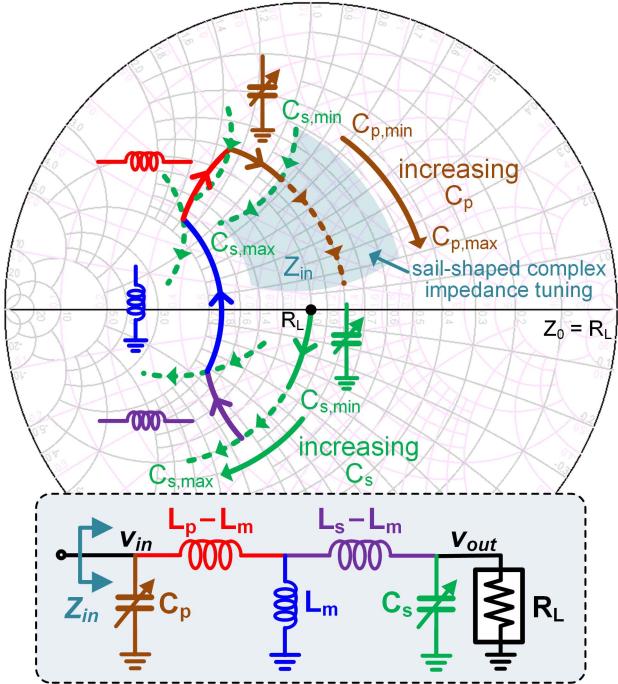


Fig. 10. Smith chart illustration for the impedance tuning characteristic of the transformer-based LM network. The network is assumed to be lossless in this figure for simplicity.

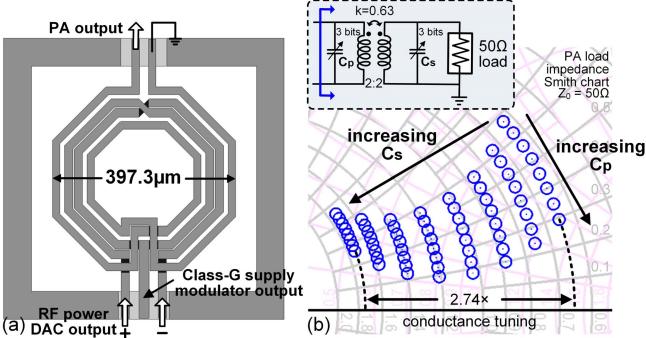


Fig. 11. (a) EM structure of the transformer. (b) Simulated ITR of the LM network.

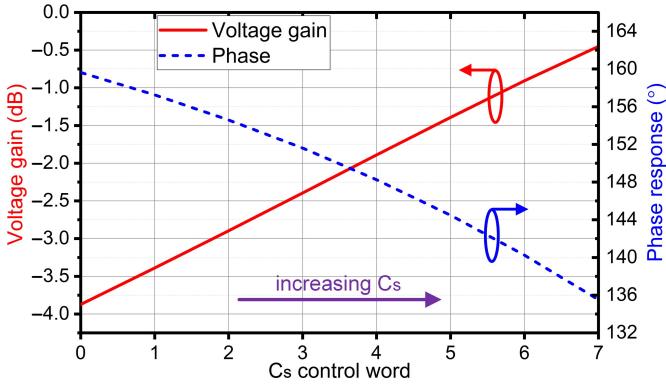


Fig. 12. Simulated voltage gain and phase responses of the LM network when  $C_s$  is tuned.

elaborate linearization techniques are often needed for LM PAs [68].

In the next two sections, we first present a new LM scheme that realizes PA PBO efficiency peaking. Then,

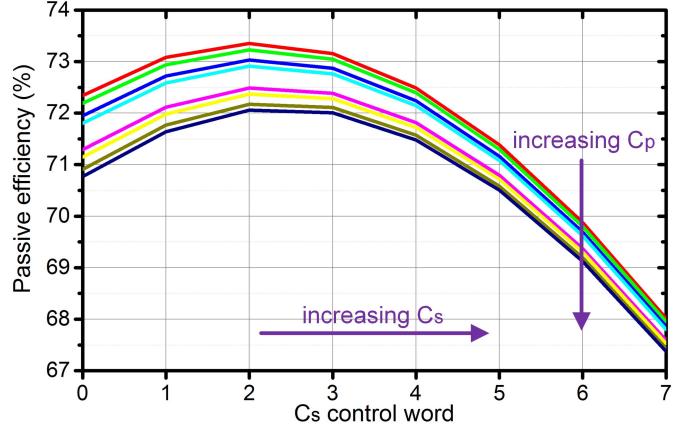


Fig. 13. Simulated PE of the LM network for all the digital settings.

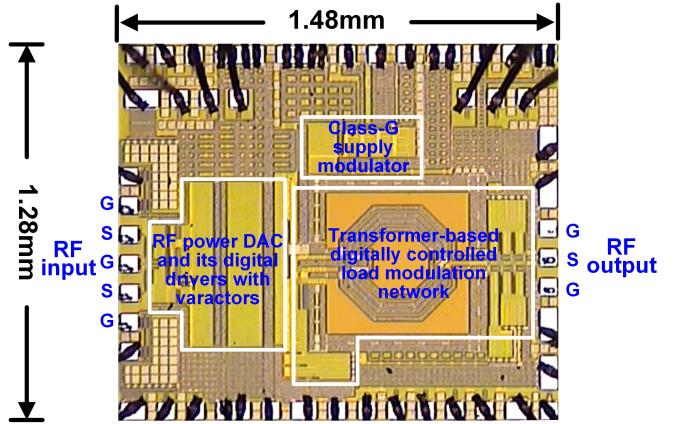


Fig. 14. Chip microphotograph.

we synergistically combine this LM scheme with the Class-G operation. The introduced hybrid architecture leverages the advantages of both Class-G and LM techniques, overcomes their drawbacks, and significantly improves the PA average efficiency for high-PAPR signals without a demanding ITR requirement of the LM network.

#### B. DLTm Scheme Achieving PA PBO Efficiency Peaking

In a typical current-mode PA, the PA load impedance for the optimum efficiency ( $Z_{opt,\eta}$ ) is usually different from the PA load impedance for the maximum  $P_{out}$  ( $Z_{opt,P_{out}}$ ) [1].  $Z_{opt,\eta}$  often has a smaller conductance than  $Z_{opt,P_{out}}$ , resulting in a larger voltage swing at the device output. This enhances the PA efficiency by reducing the dc power waste due to the reduced overlap of current and voltage waveforms. Meanwhile, due to the knee voltage, the boosted voltage swing by  $Z_{opt,\eta}$  results in a reduced fundamental output current and thus reduced  $P_{out}$  [1]. For field-effect transistors (FETs), the output current is a function of both the device input and output voltages. Fig. 2 shows the simulated  $I-V$  characteristic of a cascode MOSFET circuit as a PA stage. When the output voltage swings down to the knee voltage during large-signal operation, the common-gate transistor (or even both common-gate and common-source transistors) enters the triode region, leading to a lower output impedance, a substantially reduced

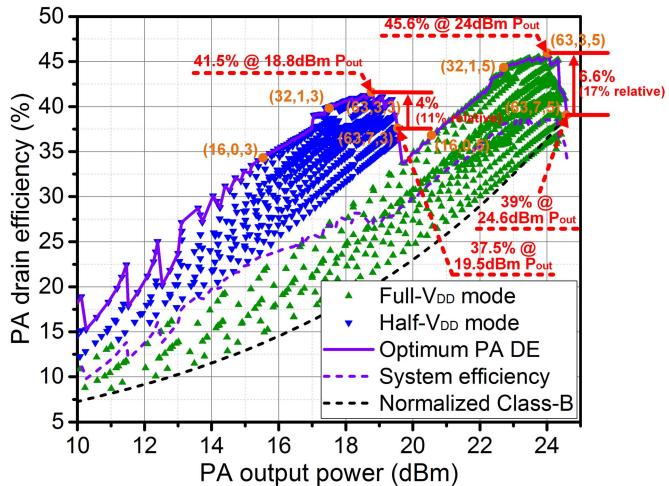


Fig. 15. Measured PA DE at 2.4 GHz versus PA  $P_{\text{out}}$ . Representative control words are shown, and they are formed as (RF power DAC code,  $C_s$  code,  $C_p$  code).

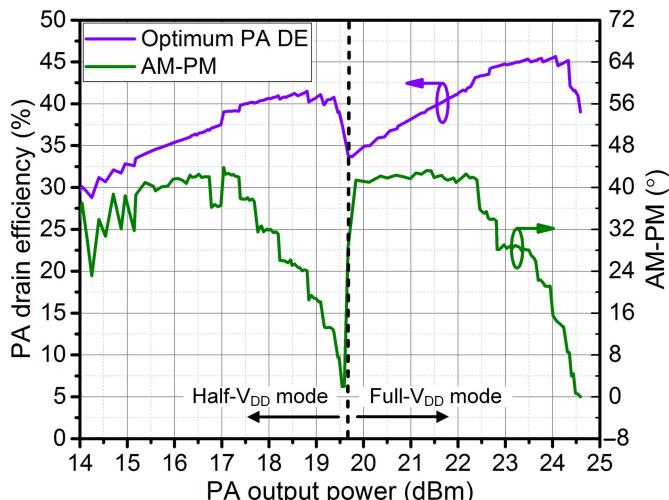


Fig. 16. Measured PA AM-PM of the efficiency-optimum settings at 2.4 GHz.

output current at the fundamental frequency, and therefore a decreased PA  $P_{\text{out}}$ .

We exploit the different impedance values of  $Z_{\text{opt\_}P_{\text{out}}}$  and  $Z_{\text{opt\_}\eta}$  and devise a new DLTM scheme that achieves PA PBO efficiency peaking. For illustration, we use the large-signal load-pull simulation results of the previous cascode circuit when it is implemented as an RF power DAC and operates in a push-pull Class-D<sup>-1</sup> configuration at 2.4 GHz [Fig. 3(a)]. The introduced DLTM operation is comprised of two PBO sections. First, the PA performs its PBO by manipulating the PA load impedance that travels from  $Z_{\text{opt\_}P_{\text{out}}}$  to  $Z_{\text{opt\_}\eta}$ , without changing the AM code of the RF power DAC. During this PBO process, the PA load consecutively meets  $Z_{\text{opt\_}P_{\text{out}}}$  and then  $Z_{\text{opt\_}\eta}$ , and the PA PBO efficiency peaks up [Fig. 3(b)] in contrast to many conventional PA designs. Next, the conventional LM operation is performed for larger PBO levels, in which the PA scales down its RF output current by decreasing the AM code of the RF power DAC,

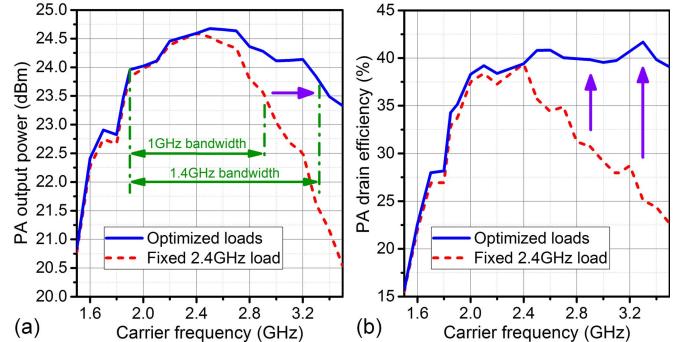


Fig. 17. PA carrier bandwidth extension by LM in the CW measurement for (a) PA  $P_{out}$  and (b) PA DE.

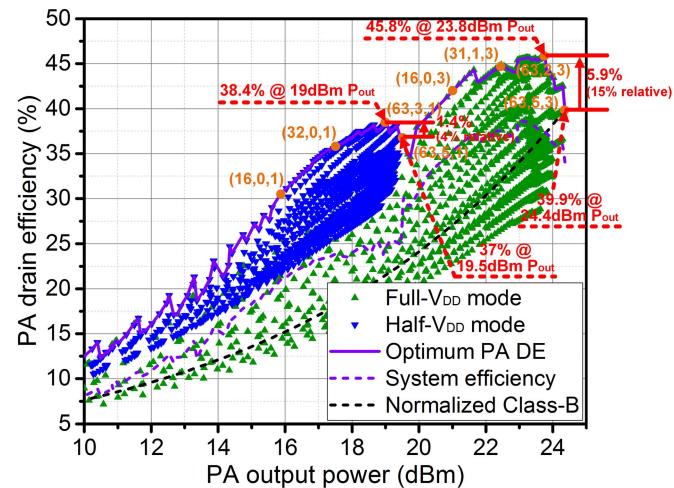


Fig. 18. Measured PA DE at 2.8 GHz versus PA  $P_{\text{out}}$ . Representative control words are shown, and they are formated as (RF power DAC code,  $C_s$  code,  $C_p$  code).

and the PA load impedance is simultaneously adjusted by the LM network to achieve a decreasing conductance along a constant-susceptance circle. During this PBO process, the PA PBO efficiency is maintained until the tuning limit of the LM network is reached [Fig. 3(b)].

Sufficient power and efficiency differences between  $Z_{\text{opt-}\eta}$  and  $Z_{\text{opt-}P_{\text{out}}}$  are desired to enhance the effectiveness of the introduced DLTM scheme. These often exist in the battery-powered PAs in mobile devices, in which the knee voltage is a considerable percentage of the PA supply voltage, e.g., about 23% in Fig. 2. Moreover, if the PA operates in the device triode region for a considerable amount of time, it tends to present large differences between  $Z_{\text{opt-}\eta}$  and  $Z_{\text{opt-}P_{\text{out}}}$ . Most switching-mode PAs ideally operate in the device triode region for the half of a period, making them good candidates for the introduced DLTM scheme. Take the cascode circuit in Fig. 2 again as an example, and assume that it operates in the push-pull Class-D<sup>-1</sup> configuration. Fig. 4 compares the simulated PA output voltage and current waveforms when the PA is loaded by  $Z_{\text{opt-}P_{\text{out}}}$  or  $Z_{\text{opt-}\eta}$  at the fundamental frequency. The even and odd harmonics are terminated as open and short-to-ground up to the sixth and fifth harmonics, respectively. These two cases show significant differences in their voltage and current waveforms. The case of  $Z_{\text{opt-}P_{\text{out}}}$  has +26.9-dBm PA  $P_{\text{out}}$  and 56.3% peak PA drain

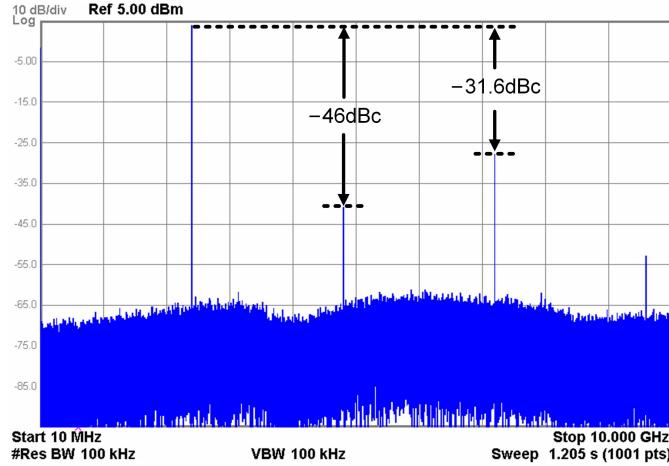


Fig. 19. Measured PA output spectrum for the peak CW  $P_{\text{out}}$  at 2.4 GHz without any additional filtering. A 20-dB attenuator is used at the PA output in this measurement.

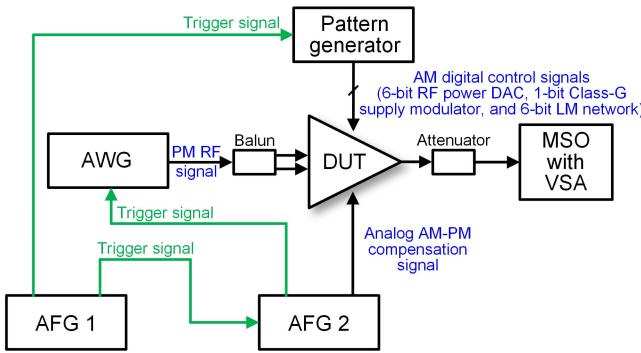


Fig. 20. Simplified modulation measurement setup.

efficiency (DE), while the case of  $Z_{\text{opt},\eta}$  has +25.4-dBm PA  $P_{\text{out}}$  and 68.8% peak PA DE [Fig. 3(a)]. It is clearly shown that the case of  $Z_{\text{opt},\eta}$  exhibits a higher device output voltage swing, more operating time in the device triode region, and a smaller fundamental RF output current, agreeing well with the analysis.

#### C. Mixed-Signal Hybrid Class-G and DLTm PA Architecture

To further improve PA efficiency in deep PBO, we combine the introduced new DLTm scheme with Class-G operation. Fig. 5 shows the mixed-signal hybrid Class-G and DLTm PA architecture, which comprises an RF power DAC, a Class-G supply modulator, and an on-chip digitally controlled LM network. The introduced PA operates in a polar fashion (Fig. 5). The RF power DAC is driven by the PM RF signal, and the AM is synthesized by dynamically programming the RF power DAC, Class-G modulator, and LM network together. The Class-G operation provides two supply modes for different real-time PA PBO levels. In the high-power region, the PA is in the full- $V_{\text{DD}}$  mode. In deep PBO, the PA is in the half- $V_{\text{DD}}$  mode for PA efficiency enhancement. Within each supply mode, the new DLTm operation is performed by the RF power DAC and LM network to enhance PA PBO efficiency.

The hybrid real-time Class-G and DLTm operation for PA PBO efficiency enhancement is explained in detail as

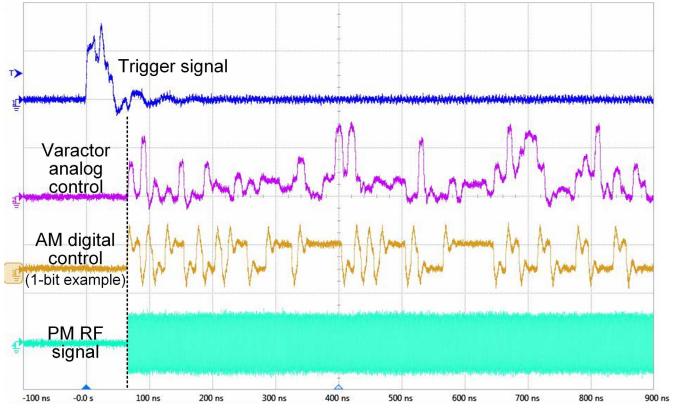


Fig. 21. Waveform examples of the synchronized PM RF signal, digital AM control signal, and dynamic varactor analog control signal at a sampling rate of 100 MSa/s.

follows. At the peak PA  $P_{\text{out}}$  (0-dB PBO), the PA supply voltage is in the full- $V_{\text{DD}}$  mode, and the PA load impedance is set to  $Z_{\text{opt},P_{\text{out}}}$  by the LM network for maximum PA  $P_{\text{out}}$ . Without changing the AM code of the RF power DAC, the PA first performs its PBO operation by manipulating the load that travels from  $Z_{\text{opt},P_{\text{out}}}$  to  $Z_{\text{opt},\eta}$ . As explained previously, the PA efficiency peaks and reaches the maximum value through this process. For larger PBO levels, the RF power DAC decreases its AM code, and the load is simultaneously adjusted by the LM network that provides proper conductances along a constant-susceptance circle and cancels the output capacitance of the RF power DAC. The PA PBO efficiency is enhanced until the load tuning limit is reached. At 6-dB PBO, the Class-G operation sets the supply to the half- $V_{\text{DD}}$  mode. The above DLTm operation is then repeated for the PBO levels beyond 6 dB. Note that the digitally intensive and reprogrammable nature of the RF power DAC, Class-G supply modulator, and digitally controlled on-chip LM network enables their well-synchronized and optimum cooperation in the introduced hybrid PA architecture, which cannot be easily achieved by conventional analog PAs.

Fig. 6 shows the theoretical PBO efficiency curve of the hybrid Class-G and DLTm PA that greatly enhances the PA average efficiency for high-PAPR signals. Compared with a Class-G PA, the hybrid Class-G and DLTm operation enhances the PA PBO efficiency within each supply voltage mode. Different from a conventional LM PA, the hybrid operation substantially extends the effective LM range by using only a 1-bit Class-G supply modulator. This leads to superior PA efficiency in deep PBO and relaxes the required ITR, allowing for simplified, compact, and low-loss LM network designs.

The mixed-signal PA operation also ensures the accuracy of the PA output signal. Our PA minimizes AM-AM distortions by selecting proper digital control codes for the RF power DAC, Class-G supply modulator, and LM network at different  $P_{\text{out}}$  levels. At the same time, AM-PM distortions are compensated by the dynamic analog tuning of the varactors in the digital driver chain [61]. The advantages of this real-time AM-PM linearization technique include sufficient phase correction, negligible impact on PA  $P_{\text{out}}$  and efficiency,

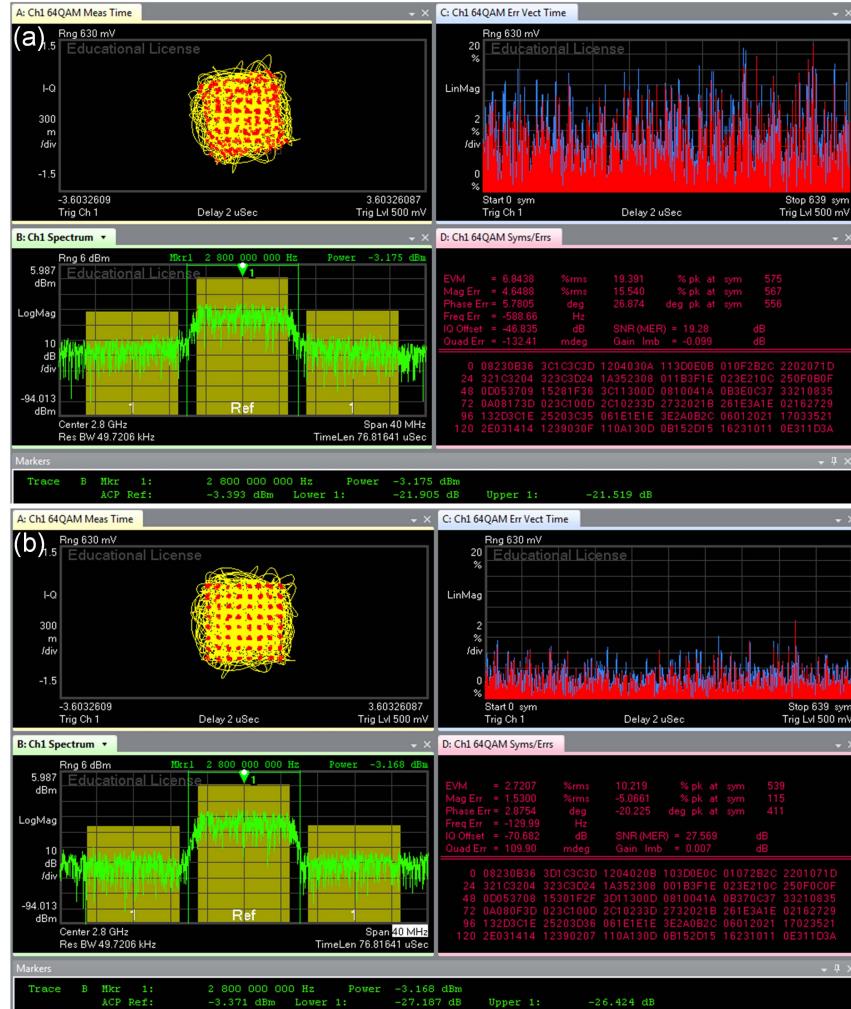


Fig. 22. Measurement results for 10M-Sym/s 64QAM at 2.8 GHz: (a) with a constant varactor control voltage (+17.3-dBm average PA  $P_{\text{out}}$ , 25.5% PA DE) and (b) with the dynamic analog tuning of the varactor control voltage (+17.3-dBm average PA  $P_{\text{out}}$ , 26.2% PA DE).

a  $P_{\text{out}}$ -independent phase compensation lookup table (LUT), low PM-AM distortions, and no reliability degradation [61].

In addition, our PA architecture extends the PA carrier bandwidth. For a given current-mode PA, its optimum load impedances for the same PA  $P_{\text{out}}$  at different carrier frequencies approximately have the same conductance but different susceptances that cancel the device output capacitance (Fig. 7) [69]. Thus, the PA carrier bandwidth is extended by adjusting the PA load impedance along a constant-conductance circle for different carrier frequencies.

### III. PA IMPLEMENTATION DETAILS

#### A. RF Power DAC and Class-G Supply Modulator

Fig. 8 shows the proof-of-concept PA in a standard 65-nm bulk CMOS process. The PA output stage is a 6-bit binary-weighted cascode push-pull RF power DAC operating in the Class-D<sup>-1</sup> mode [12], [70], [71]. The top five most significant bits are thermometer-coded for enhanced matching, and the least significant bit is binary-coded to extend the dynamic range of the PA  $P_{\text{out}}$ .

The RF power DAC is driven by a four-stage 1.2-V digital driver chain. Varactors are used at the outputs of the first two digital driver stages to provide real-time analog AM-PM

linearization. They are properly sized to offer sufficient phase compensation with negligible PM-AM distortions.

The 1-bit Class-G supply modulator uses NMOS and PMOS switches for 2.8-V  $V_{\text{DD}}$  (full- $V_{\text{DD}}$  mode) and 1.55-V  $V_{\text{DD}}$  (half- $V_{\text{DD}}$  mode), respectively. The half- $V_{\text{DD}}$  value is chosen to be slightly higher than the half of the full- $V_{\text{DD}}$  value to compensate the PA knee voltage, whose effects are more pronounced in the half- $V_{\text{DD}}$  mode. The simulated on-resistances of the NMOS and PMOS switches are 0.36 and 0.35  $\Omega$  at their operating voltage levels, respectively, ensuring negligible PA efficiency degradation. The simulated efficiency of the Class-G supply modulator is better than 96.3% and 95% for all the PA  $P_{\text{out}}$  levels in the full- $V_{\text{DD}}$  and half- $V_{\text{DD}}$  modes, respectively.

#### B. On-Chip Transformer-Based LM Network

The hybrid Class-G and DLTM operation relaxes the ITR requirement of the LM network. An on-chip transformer-based LM network is adopted in our design (Fig. 8). It achieves differential to single-ended conversion and complex impedance tuning with compactness and low passive loss.

The LM network is comprised of an on-chip transformer and two tuning capacitors on its primary and secondary sides (Fig. 8), which form a fourth-order network. We will

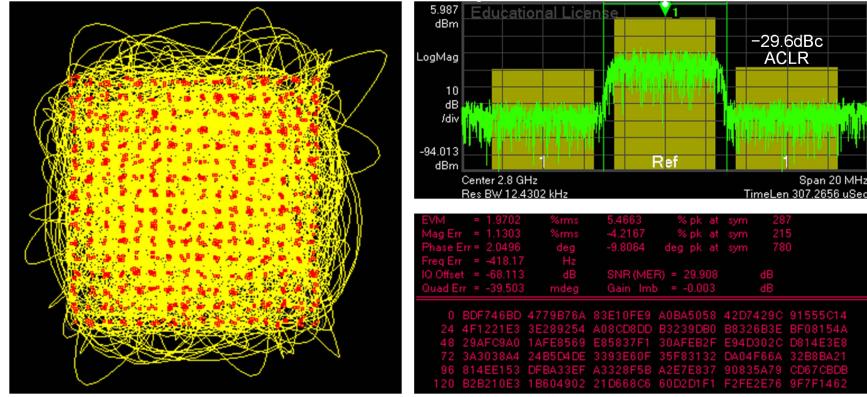


Fig. 23. Measurement results for 5M-Sym/s 256QAM at 2.8 GHz with +17-dBm average PA  $P_{\text{out}}$  by employing the dynamic analog tuning of the varactor control voltage.

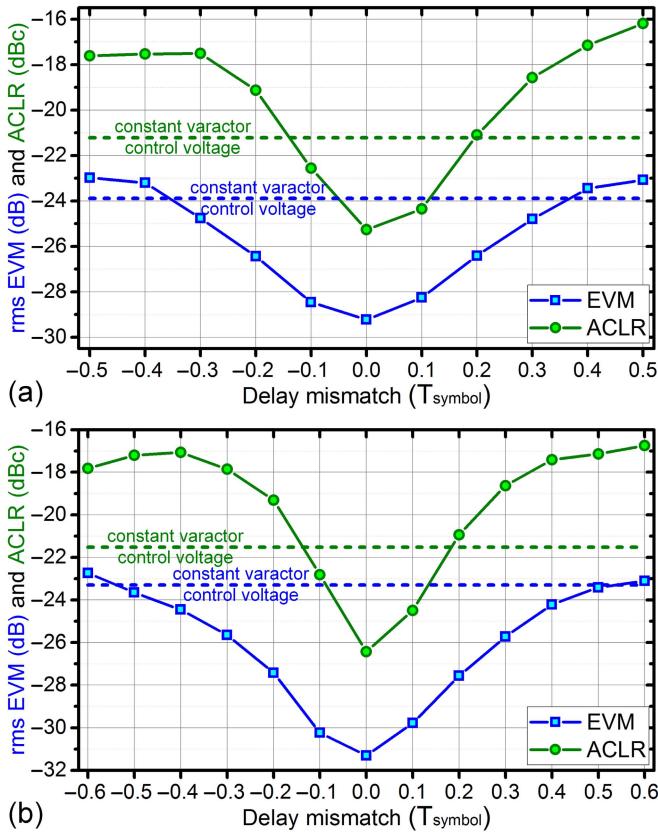


Fig. 24. Measurement with deliberately misaligned dynamic varactor analog control at (a) 2.4 GHz and (b) 2.8 GHz. The rms EVM/ACLR results for a constant varactor control voltage are shown as dashed lines. 10M-Sym/s 64QAM (symbol period  $T_{\text{symbol}} = 100$  ns) is used.

use the equivalent circuit model in Fig. 9 [72] for the following analysis. A single-ended circuit is used here for simplicity.  $L_p$  and  $L_s$  are the self-inductances of the primary and secondary windings, respectively.  $L_m$  is their mutual inductance with a magnetic coupling coefficient of  $k$ .  $C_p$  and  $C_s$  are the tuning capacitances on the primary and secondary sides, respectively. Although on-chip transformers have been extensively used in PA designs, including LM PAs [44], [45], [49], [52], we will focus on the

characteristics in dynamic load tuner applications, which have not been fully explored in literature.

First, the impedance tuning capability of the transformer-based LM network is studied. The load impedance  $Z_{\text{in}}$  is derived as

$$\begin{aligned}
 Z_{\text{in}} &= [s^3 R_L C_s (L_p L_s - L_m^2) + s^2 (L_p L_s - L_m^2) + s R_L L_p] \\
 &\quad / [s^4 R_L C_p C_s (L_p L_s - L_m^2) + s^3 C_p (L_p L_s - L_m^2) \\
 &\quad \quad \quad + s^2 R_L (C_p L_p + C_s L_s) + s L_s + R_L] \\
 &= [s^3 R_L C_s L_p L_s (1 - k^2) + s^2 L_p L_s (1 - k^2) + s R_L L_p] \\
 &\quad / [s^4 R_L C_p C_s L_p L_s (1 - k^2) + s^3 C_p L_p L_s (1 - k^2) \\
 &\quad \quad \quad + s^2 R_L (C_p L_p + C_s L_s) + s L_s + R_L] \quad (2)
 \end{aligned}$$

where  $s = j2\pi f$ , and  $f$  is the operating frequency. Equation (2) suggests that  $Z_{\text{in}}$  depends on both  $C_p$  and  $C_s$ . For more design insights, we use the Smith chart for explanations (Fig. 10).

The effect of tuning  $C_p$  is straightforward since it moves  $Z_{\text{in}}$  along constant-conductance circles on the Smith chart. For a given device with a fixed biasing and driving condition, the load-pull impedance at a higher operating frequency has a larger susceptance. In order to extend the carrier bandwidth,  $C_p$  should be decreased at higher operating frequencies (Fig. 10). Fig. 10 also shows how tuning  $C_s$  impacts  $Z_{\text{in}}$ . Due to the impedance transformations of one series inductor ( $L_s - L_m$ ), one shunt inductor ( $L_m$ ), and the other series inductor ( $L_p - L_m$ ),  $Z_{\text{in}}$  moves approximately along constant-susceptance circles when  $C_s$  is adjusted. During PA PBO, a reduced conductance is desired for efficiency enhancement, and  $C_s$  should be decreased (Fig. 10). In summary, the tunings of  $C_p$  and  $C_s$  create a “sail-shaped” complex impedance coverage on the Smith chart.

Next, the transfer function of the transformer-based LM network is analyzed. The analytical result of  $v_{\text{out}}/v_{\text{in}}$  as labeled

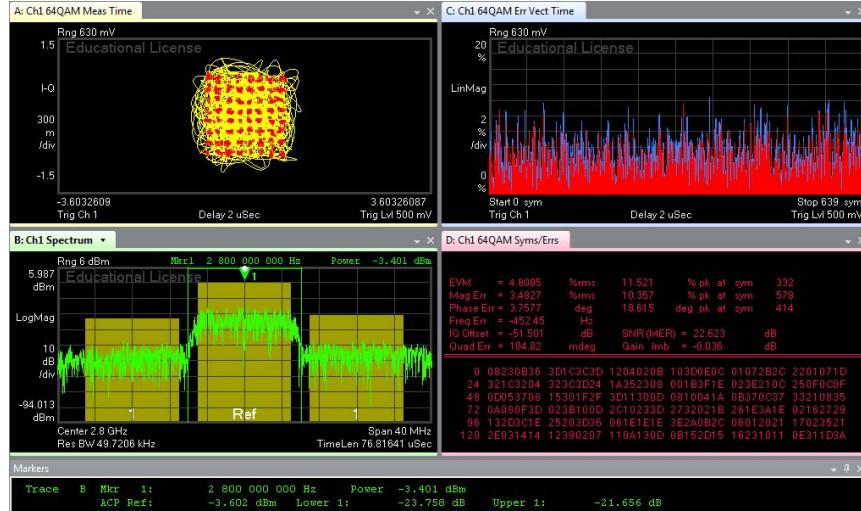


Fig. 25. Measurement results for 10M-Sym/s 64QAM at 2.8 GHz when using LUTs for 2.4 GHz. Comparison with the optimum performance at 2.8 GHz using 2.8-GHz LUTs [Fig. 22(b)] verifies that the mixed-signal reconfiguration of the PA achieves performance optimization at different carrier frequencies.

in Fig. 9 is derived as

$$\begin{aligned} \frac{v_{\text{out}}}{v_{\text{in}}} &= \frac{R_L L_m}{s^2 R_L C_s (L_p L_s - L_m^2) + s(L_p L_s - L_m^2) + R_L L_p} \\ &= \frac{k R_L \sqrt{L_p L_s}}{s^2 R_L C_s L_p L_s (1 - k^2) + s L_p L_s (1 - k^2) + R_L L_p}. \end{aligned} \quad (3)$$

Equation (3) offers two important design insights. As mentioned,  $C_s$  should be decreased during PBO so that the PA efficiency is enhanced. First, (3) shows that  $|v_{\text{out}}/v_{\text{in}}|$ , i.e., the passive voltage gain, monotonically decreases during this process. This behavior fundamentally makes it possible to maintain the voltage swing at the device output during PBO for efficiency enhancement, while the voltage swing at the final load resistor decreases for PBO. Second, (3) shows that the phase of  $v_{\text{out}}/v_{\text{in}}$  monotonically increases when  $C_s$  decreases at a given operating frequency. This combines with the PA device AM-PM distortions and constitutes the total PA AM-PM nonlinearity. These two AM-PM distortions may add constructively or destructively, depending on the PA mode, device technology, and circuit topology. In our design, these two AM-PM sources add constructively, and the total PA AM-PM is compensated by the dynamic tuning of the varactors in the digital driver chain.

In our proof-of-concept PA, the transformer has a 2:2 turn ratio [Fig. 11(a)]. Its geometry (outer diameter = 397.3  $\mu\text{m}$ ) and magnetic coupling coefficient ( $k = 0.63$ ) are carefully designed so that a compact layout with a sufficient load tuning range and high passive efficiencies across the load tuning settings is achieved. The tuning capacitors on the two sides of the transformer are each 3-bit binary-weighted switch-controlled metal-oxide-metal capacitor arrays. There are in total 6 bits for the LM network configuration. Switches are designed to withstand large voltage swings with low distortions (Fig. 8). They use deep  $N$ -well thick-oxide transistors, and their gate and bulk are dc biased using large resistors (20  $\text{k}\Omega$ ), which makes these two terminals semi-open and ac boot-strapped

to relieve the stress [73]. Furthermore, the dc biases of both source and drain are set differently in on and off switch states (Fig. 8) [47], [74]. Since a switch-controlled capacitor is most vulnerable to large voltage swings in its off state [47], [74], this biasing scheme prevents the off switch transistors from forming an undesired channel and enhances its resilience to large voltage swings.

Fig. 11(b) shows the simulated ITR of the implemented on-chip transformer-based LM network, which achieves 2.74 $\times$  conductance tuning. Fig. 12 shows the simulated gain and phase responses when adjusting  $C_s$ , which align well with the theoretical analysis. The simulated AM-PM due to the LM network is 24.1° for the whole ITR. The simulated passive efficiency (PE) of the LM network is better than 67.4% for all the impedance settings (Fig. 13). During PBO,  $C_s$  decreases, and the PE first increases and then slightly decreases, which is mainly caused by the decreased and then increased impedance transformation ratio in our LM network design. Such PBO PE peaking helps with the PA PBO efficiency enhancement.

#### IV. MEASUREMENT RESULTS

The PA is fully integrated in a standard 65-nm bulk CMOS process with a total chip area of only 1.9  $\text{mm}^2$  (Fig. 14).

##### A. Continuous-Wave Measurement

The PA is first characterized using continuous-wave (CW) signals. Fig. 15 shows the measurement results at 2.4 GHz. Each symbol represents one combined digital setting for the RF power DAC, Class-G supply modulator, and LM network. Efficiency-optimum settings are selected for different  $P_{\text{out}}$  levels (Fig. 15). The PA achieves 39% PA DE at +24.6-dBm peak  $P_{\text{out}}$  with a peak DE of 45.6% at +24-dBm  $P_{\text{out}}$ , showing 6.6% (17% relative) efficiency peaking at 0.6-dB PBO in the full- $V_{\text{DD}}$  mode. Similarly, a PA efficiency peaking of 4% (11% relative) is achieved at 0.7-dB PBO in the half- $V_{\text{DD}}$  mode. The measured DE at 3/6/9/12-dB PBO is 39.9/41.2/34.5/21.8% with 1.45/2.12/2.49/2.18 $\times$  improvement

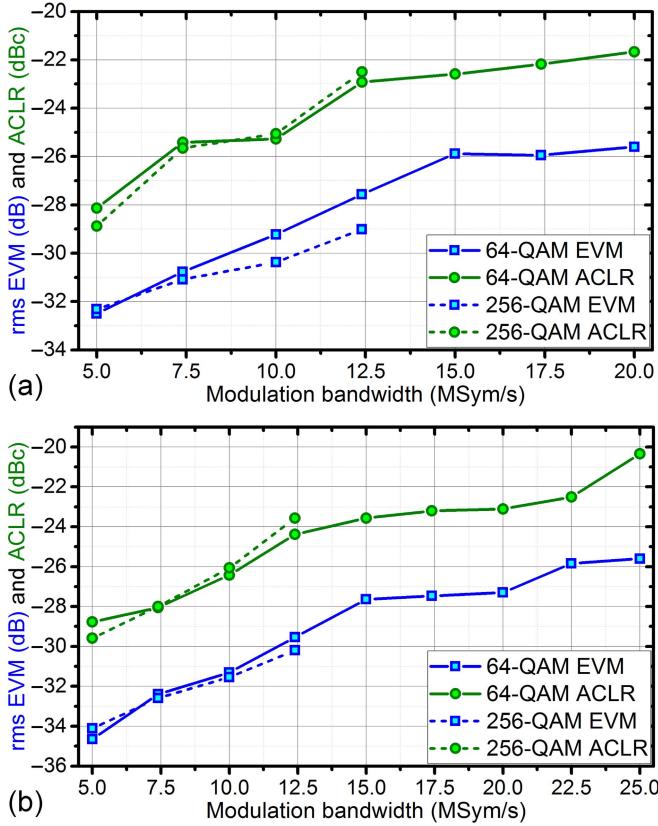


Fig. 26. Measurement results for 64QAM and 256QAM with different symbol rates at (a) 2.4 GHz and (b) 2.8 GHz.

over an ideal Class-B PA, respectively. These measurement demonstrates the PA PBO efficiency peaking and deep PBO efficiency enhancement by the hybrid Class-G and DLTM operation, agreeing well with our theoretical analysis.

Fig. 16 shows the measured PA AM-PM of the efficiency optimum settings. Class-G supply switching causes an evident phase jump at the full- $V_{DD}$ /half- $V_{DD}$  mode transition [61]. Meanwhile, staircase-shaped AM-PM behaviors are observed in both Class-G supply modes. This is due to the monotonic AM-PM of the LM network, which is discussed in Section III-B. The PA phase response of different varactor control voltages is characterized at peak  $P_{out}$ , which forms the AM-PM compensation LUT for the dynamic measurement. Note that the LUT generation is  $P_{out}$ -independent for our AM-PM compensation technique, since the varactors at the digital drivers' outputs experience a constant-envelope PM driving signal during PBO [61]. Such  $P_{out}$ -independent LUT significantly reduces the implementation complexity.

Fig. 17 shows the measured PA  $P_{out}$  and DE at different carrier frequencies when the RF power DAC is fully turned on. For the load setting achieving the maximum  $P_{out}$  at 2.4 GHz, the PA has a 1-dB  $P_{out}$  bandwidth of 1.9–2.9 GHz, i.e., 41.7% fractional bandwidth [Fig. 17(a)]. By selecting the optimum loads for maximum  $P_{out}$  at different carrier frequencies, the 1-dB  $P_{out}$  bandwidth is extended to 1.9–3.3 GHz, i.e., 53.8% fractional bandwidth [Fig. 17(a)]. Substantial PA DE improvement over the bandwidth is also achieved [Fig. 17(b)]. This demonstrates the carrier bandwidth extension by the LM

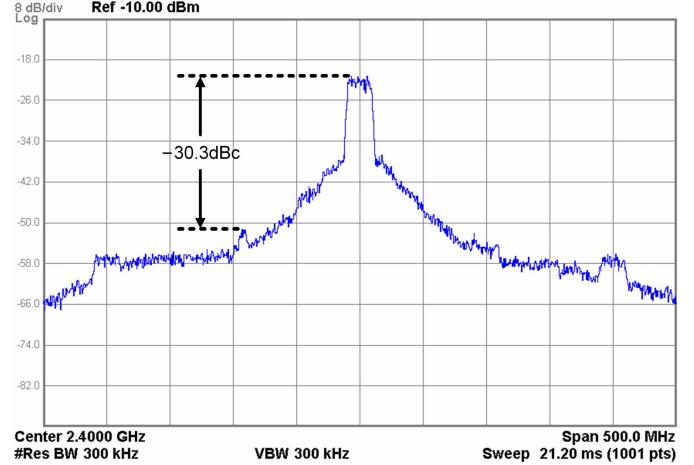


Fig. 27. Measured far-out-of-band spectrum for +17.5-dBm 20M-Sym/s 64QAM at 2.4 GHz.

operation. Moreover, the PA PBO efficiency enhancement by the hybrid Class-G and DLTM operation is maintained in a wide carrier frequency range. Fig. 18 shows the CW measurement results at 2.8 GHz and demonstrates 1.53/1.87/1.99/1.81× PA DE improvement over an ideal Class-B PA at 3/6/9/12-dB PBO, verifying the frequency agility of the reconfigurable mixed-signal PA.

The measured second/third harmonic rejections at peak  $P_{out}$  are  $-46/-31.6$  and  $-38.8/-34.1$  dBc at 2.4 and 2.8 GHz without additional filtering (Fig. 19).

### B. Modulation Measurement

Fig. 20 shows the setup for the modulation tests. The PM RF signal, digital AM control signals, and dynamic varactor analog control signal are generated by an arbitrary waveform generator (AWG), a pattern generator, and an arbitrary function generator (AFG), respectively. These three instruments are synchronized with a timing resolution of 1 ps by independently tuning the delays of their trigger signals from AFGs (Figs. 20 and 21). The PA output signal is demodulated by an oscilloscope with a vector signal analysis (VSA) software. 5× sampled 64QAM (7-dB PAPR) up to 25 MSym/s (150 Mb/s) and 256QAM (7.3-dB PAPR) up to 12.5 MSym/s (100 Mb/s) are used in the measurement. No additional predistortion or feedback linearization is applied.

1) *Dynamic AM-PM Linearization:* Real-time AM-PM linearization by the dynamic analog tuning of the varactor control voltage is first measured. Compared with a constant varactor control voltage, dynamic analog tuning substantially reduces the rms error vector magnitude (EVM) and adjacent channel leakage ratio (ACLR) by 10.4/5.3/2.2 and 6.8/4.1/2.2 dB for 5/10/20M-Sym/s 64QAM at 2.4 GHz. These EVM and ACLR improvement values are 10.8/8/4.5 and 8.4/4.9/2.3 dB for 5/10/20M-Sym/s 64QAM at 2.8 GHz, showing consistent improvement in a wide carrier frequency range.

Fig. 22 compares the measured demodulation results for 10M-Sym/s 64QAM at 2.8 GHz. Before applying dynamic AM-PM linearization, the outer constellation points rotate with respect to the inner points [Fig. 22(a)], showing

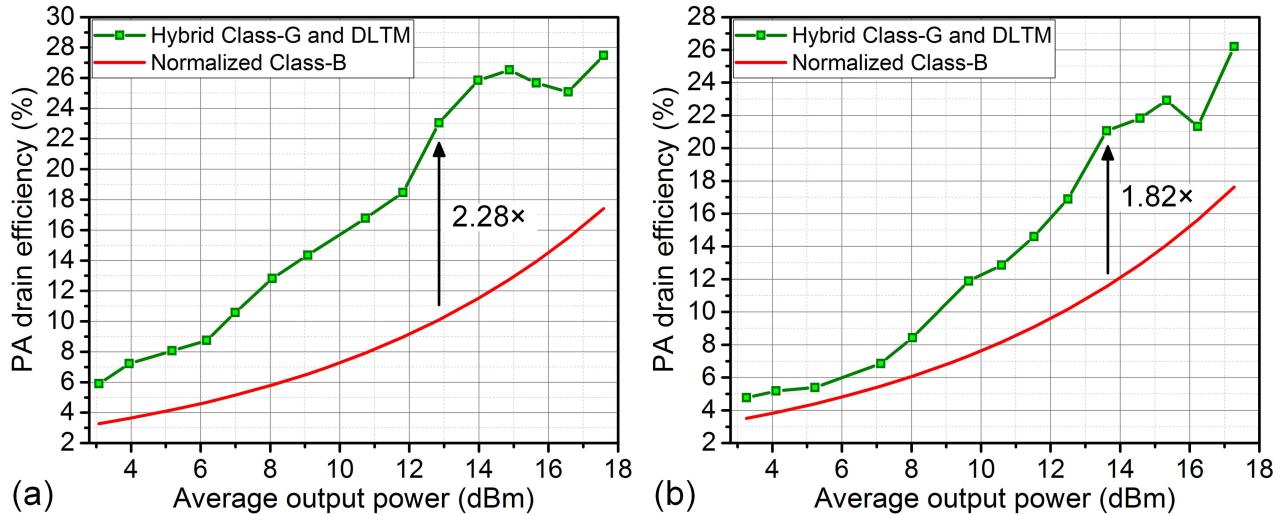


Fig. 28. Measured PA DE when backing off the average  $P_{out}$  for 10M-Sym/s 64QAM at (a) 2.4 GHz and (b) 2.8 GHz.

AM-PM nonlinearity. This is corrected, together with improved ACLR, by applying the dynamic analog tuning of the varactor control voltage [Fig. 22(b)]. Meanwhile, there is negligible change on the PA  $P_{out}$  and efficiency due to this AM-PM linearization. Moreover, 256QAM is successfully demodulated after applying dynamic AM-PM linearization (Fig. 23), while the demodulated constellation cannot be locked by the VSA software if using a constant varactor control voltage.

With dynamic AM-PM linearization at 2.4 GHz, the PA delivers +17.6/+17.3-dBm 10M-Sym/s 64-QAM/256-QAM signals with 27.5/26.7% PA DE, 22.2/21.6% system efficiency including all the on-chip power consumption, -29.2/-30.4-dB rms EVM, and -25.3/-25.1-dBc ACLR. At 2.8 GHz, the PA delivers +17.3/+17-dBm 10M-Sym/s 64-QAM/256-QAM signals with 26.2/24.1% PA DE, 20.9/19.3% system efficiency, -31.3/-31.5-dB rms EVM, and -26.4/-26.1-dBc ACLR. These are the results for the average  $P_{out}$  without backing-off the PA peak  $P_{out}$ .

AM-PM linearization with deliberate timing mismatch is also characterized. In this measurement, the PM RF signal and AM digital controls remain aligned, while the timing of the dynamic varactor analog control signal is adjusted by tuning the delay of its trigger signal. Fig. 24(a) and (b) show the results at 2.4 and 2.8 GHz, respectively. The rms EVM is < -24.8/-25.6 dB up to  $\pm 0.3 \times$  symbol period at 2.4/2.8 GHz. Significant timing mismatch leads to degraded EVM and ACLR, which can be even worse than the case with a constant varactor control voltage, i.e., no dynamic AM-PM compensation (Fig. 24). This is because the phase adjustment by the dynamic varactor analog control is equivalently additive phase distortions when its timing is excessively misaligned.

2) *Carrier Bandwidth Extension by Mixed-Signal Reconfiguration:* Reconfiguring the LUTs of both the AM digital controls and dynamic varactor analog tuning optimizes the performance of our PA at different carrier frequencies, which includes the PA  $P_{out}$ , efficiency, and linearity. For example, Fig. 25 shows the measurement results at 2.8 GHz when using the LUTs that are optimized for 2.4 GHz. Compared with

Fig. 22(b), 0.23-dB PA  $P_{out}$ , 5.2% PA DE, 4.9-dB rms EVM, and 4.8-dB ACLR enhancement are achieved after mixed-signal reconfiguration. This demonstrates that the introduced PA can be in-field digitally reconfigured to deliver its optimum performance at different carrier frequencies.

3) *Other Performance at Peak Average PA  $P_{out}$ :* Fig. 26(a) and (b) show the measured linearity for 64-QAM/256-QAM signals with different symbol rates at 2.4 and 2.8 GHz, respectively. The rms EVM of 64QAM is below -25 dB up to 20 and 25 MSym/s at 2.4 and 2.8 GHz, respectively. No drastic linearity degradation is observed, and the linearity at higher symbol rates can be further improved by refining the setup that provides better timing alignment among mixed-signal paths, including AM digital controls and analog varactor control.

Fig. 27 shows the measured far-out-of-band spectrum of our PA. Sampling images are suppressed below -30.3 dBc. The out-of-band noise and the ACLR degradation due to the supply switching can be improved by further reducing the duration and amplitude of the glitches at the Class-G supply modulator output via design optimizations [75].

4) *Modulation Performance When Backing-Off the Average PA  $P_{out}$ :* Finally, the average PA  $P_{out}$  is reduced to examine the modulation performance in deep PBO. Figs. 28 and 29 show the efficiency and linearity results for 10M-Sym/s 64QAM, respectively. Superior PA average efficiency is achieved up to deep PBO. At 2.4/2.8 GHz, the PA average DE is 23/21.1% at +12.8/+13.6-dBm average PA  $P_{out}$ , which achieves 2.28/1.82 $\times$  enhancement over Class-B operation. The rms EVM is lower than -25 dB up to the 14-dB PBO of average  $P_{out}$  at both 2.4 and 2.8 GHz, showing excellent in-band linearity performance. EVM and ACLR degradations are observed in deep PBO (Fig. 29). This is mainly due to AM quantization errors at low PA  $P_{out}$  levels, which can be improved by increasing the bit number of the RF power DAC.

Compared with recent CMOS PAs with PBO efficiency enhancement (Table I), our design advances the state-of-the-art PBO efficiency enhancement with high linearity and a compact area.

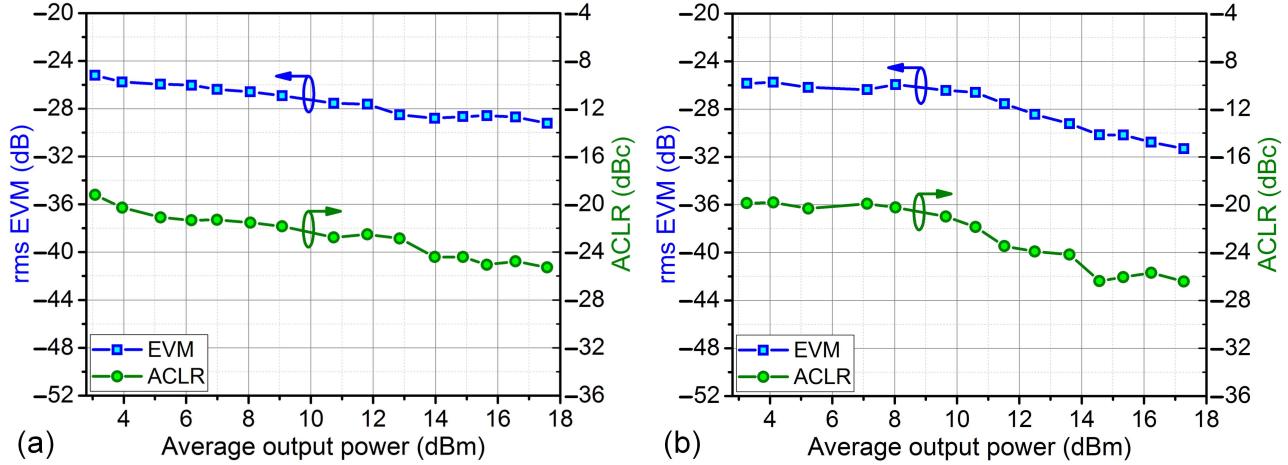


Fig. 29. Measured rms EVM and ACLR when backing off the average  $P_{\text{out}}$  for 10M-Sym/s 64QAM at (a) 2.4 GHz and (b) 2.8 GHz.

TABLE I  
PERFORMANCE COMPARISON WITH OTHER PBO EFFICIENCY ENHANCED CMOS PAs

|                    | Freq.<br>(GHz) | Peak<br>$P_{\text{out}}$<br>(dBm) | Peak<br>$\eta$<br>(%) | $\eta$ at 6-dB<br>PBO (%)            | $\eta$ at 12-dB<br>PBO (%)           | $\eta$ imp.<br>at 6-dB<br>PBO $\ddagger$ | $\eta$ imp.<br>at 12-dB<br>PBO $\ddagger$ | Average<br>$P_{\text{out}}$<br>(dBm) | Average<br>$\eta$<br>(%) | $\eta$ imp. for<br>modulated<br>signals $\ddagger$ | EVM<br>(dB)       | ACLR<br>(dBc)     | Area<br>(mm $^2$ ) | CMOS<br>technol. | Mode<br>switching | PBO efficiency<br>enhancement<br>technique |
|--------------------|----------------|-----------------------------------|-----------------------|--------------------------------------|--------------------------------------|--|---|--------------------------------------|--------------------------|--|-------------------|-------------------|--------------------|------------------|-------------------|--|
| [20]*<br>T-MTT '13 | 1.85           | 30.2                              | 48<br>(PAE)           | 46 $\dagger$ , 7 $\ddagger$<br>(PAE) | 37 $\dagger$ , 7 $\ddagger$<br>(PAE) | 1.9 $\times$                             | 3.1 $\times$                              | 26<br>16QAM                          | 34.1 (PAE)<br>16QAM      | 1.2 $\times$                                       | -31.1             | -34.2             | 2.42               | 180nm            | dynamic           | ET   |
| [38]<br>JSSC '15   | 3.8            | 27.3                              | 30.2<br>(DE)          | 21.5<br>(DE)                         | 9.6<br>(DE)                          | 1.4 $\times$                             | 1.3 $\times$                              | 21.8<br>16QAM                        | 22.1 (DE)<br>16QAM       | 1.4 $\times$                                       | -25               | -21.8             | 2.1                | 65nm             | dynamic           | Doherty                                    |
| [52]<br>JSSC '13   | 2.2            | 23.3                              | 43<br>(DE)            | 33 $\dagger$<br>(DE)                 | 15 $\dagger$<br>(DE)                 | 1.5 $\times$                             | 1.4 $\times$                              | 16.8<br>64QAM                        | 24.5 (DE)<br>64QAM       | 1.2 $\times$                                       | -28               | WLAN<br>mask      | 6.25<br>(TX)       | 65nm             | dynamic           | 1-bit LM                                   |
| [65]*<br>JSSC '13  | 2.15           | 24.3                              | 43.5<br>(PAE)         | 36.5<br>(PAE)                        | 17.8 $\dagger$<br>(PAE)              | 1.7 $\times$                             | 1.6 $\times$                              | 16.8<br>64QAM                        | 33 (PAE)<br>64QAM        | 1.8 $\times$                                       | -30.8             | N.A.              | 1.68               | 65nm             | dynamic           | 1-bit Class-G supply                       |
| [66]<br>ISSCC '13  | 1.8            | 27.2                              | 30<br>(PAE)           | 22 $\dagger$<br>(PAE)                | 9 $\dagger$<br>(PAE)                 | 1.5 $\times$                             | 1.2 $\times$                              | 21.3<br>64QAM                        | 18 (PAE)<br>64QAM        | 1.2 $\times$                                       | -22               | -30               | 5.2                | 65nm             | dynamic           | 1-bit Class-G supply<br>(equivalent)       |
| [57]<br>JSSC '12   | 2.4            | 31.5                              | 27<br>(PAE)           | 20<br>(PAE)                          | 10.8 $\dagger$<br>(PAE)              | 1.5 $\times$                             | 1.6 $\times$                              | 22.7<br>16QAM                        | 12 (PAE)<br>16QAM        | 1.2 $\times$                                       | -28               | WLAN<br>mask      | 3.12               | 45nm             | dynamic           | outphasing<br>+ 3-bit current              |
| [59]*<br>JSSC '12  | 2.4            | 27.7                              | 45.1<br>(PAE)         | 38 $\dagger$<br>(PAE)                | 22 $\dagger$<br>(PAE)                | 1.7 $\times$                             | 2 $\times$                                | 20.2<br>64QAM                        | 27.6 (PAE)<br>64QAM      | 1.5 $\times$                                       | -31.4             | N.A.              | 4                  | 65nm             | dynamic           | + 2-bit Class-G supply                     |
| [60]<br>JSSC '15   | 1.9            | 28.0                              | 34.0<br>(PAE)         | 25.5<br>(PAE)                        | 19.7<br>(PAE)                        | 1.5 $\times$                             | 2.3 $\times$                              | 23.4<br>16QAM                        | 23.3 (PAE)<br>16QAM      | 1.2 $\times$                                       | -23               | -30               | 3                  | 40nm             | static            | Doherty<br>+ 1-bit LM                      |
| [61]<br>JSSC '16   | 3.7            | 26.7                              | 40.2<br>(DE)          | 37.0<br>(DE)                         | 26.2<br>(DE)                         | 1.8 $\times$                             | 2.6 $\times$                              | 20.8<br>16QAM                        | 28.8 (DE)<br>16QAM       | 1.4 $\times$                                       | -24               | -21               | 3.2                | 65nm             | dynamic           | Doherty<br>+ 1-bit Class-G supply          |
|                    | 4.3            | 26.1                              | 36.2<br>(DE)          | 29.3<br>(DE)                         | 23.6<br>(DE)                         | 1.7 $\times$                             | 2.8 $\times$                              | 20.1<br>16QAM                        | 27.2 (DE)<br>16QAM       | 1.6 $\times$                                       | -30               | -26.5             |                    |                  |                   |  |
| This work          | 2.4            | 24.6                              | 45.6<br>(DE)          | 41.2<br>(DE)                         | 21.8<br>(DE)                         | 2.1 $\times$                             | 2.2 $\times$                              | 17.6<br>64QAM                        | 27.5 (DE)<br>64QAM       | 1.6 $\times$                                       | -29.2<br>10MSym/s | -25.3<br>10MSym/s | 1.9                | 65nm             | dynamic           | 1-bit Class-G supply<br>+ DLTM (6-bit LM)  |
|                    | 2.8            | 24.4                              | 45.8<br>(DE)          | 37.5<br>(DE)                         | 18.4<br>(DE)                         | 1.9 $\times$                             | 1.8 $\times$                              | 17.3<br>256QAM                       | 26.7 (DE)<br>256QAM      | 1.6 $\times$                                       | -25.6<br>20MSym/s | -21.7<br>20MSym/s |                    |                  |                   |  |
|                    |                |                                   |                       |                                      |                                      |  |   | 17.3<br>64QAM                        | 26.2 (DE)<br>64QAM       | 1.5 $\times$                                       | -30.4<br>10MSym/s | -25.1<br>10MSym/s |                    |                  |                   |  |
|                    |                |                                   |                       |                                      |                                      |  |   | 17<br>256QAM                         | 24.1 (DE)<br>256QAM      | 1.4 $\times$                                       | -31.3<br>10MSym/s | -26.4<br>10MSym/s |                    |                  |                   |  |
|                    |                |                                   |                       |                                      |                                      |  |   |                                      |                          |  | -25.6<br>25MSym/s | -20.3<br>25MSym/s |                    |                  |                   |  |
|                    |                |                                   |                       |                                      |                                      |  |   |                                      |                          |  | -31.5<br>10MSym/s | -26.1<br>10MSym/s |                    |                  |                   |  |

\* using off-chip components for PA output matching.  $\ddagger$  in comparison with the Class-B operation.

$\dagger$  estimated from the reported figures.  $\dagger\dagger$  not including the power consumption of the supply modulator.

## V. CONCLUSION

We present a mixed-signal PA with hybrid real-time Class-G and DLTM operation. The hybrid PA operation enhances the PA efficiency in deep PBO. Moreover, a new DLTM scheme is introduced to achieve PA PBO efficiency peaking. The real-time mixed-signal PA operation ensures the accuracy of the PA output signal. The digitally controlled LM network substantially extends the PA carrier bandwidth. The introduced PA architecture is particularly suitable for system-on-chip integrations in deeply scaled CMOS processes, which readily

offer mixed-signal controls with fine timing resolutions [7]. We demonstrate a prototype in a standard 65-nm bulk CMOS process. This is the first LM PA fully integrated in CMOS supporting 256QAM.

## ACKNOWLEDGMENT

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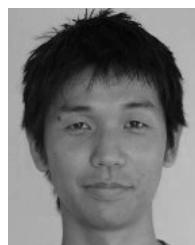
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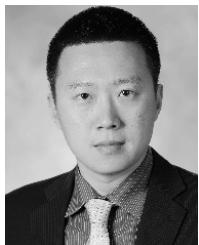
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