A High-Gain mm-Wave Amplifier Design: An Analytical Approach to Power Gain Boosting

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***Abstract*— In this paper, a general embedding is proposed to boost the power gain of any device to the maximum achievable gain ($G_{\max}$), which is defined as the maximum theoretical gain of the device. Using a gain-plane based analysis, two linear-lossless-reciprocal embeddings are used to perform a movement from the coordinate of the transistor to the coordinate that corresponds to $G_{\max}$. The proposed embedding is applied to a 10 μm common-source NMOS transistor, and the theoretical and simulation results are presented and compared. The properties of the embedded transistor are inspected, and the few issues in implementation are investigated and addressed. Finally, using the proposed general embedding, an amplifier is implemented in a 65 nm CMOS process with a measured power gain of 9.2 dB at 260 GHz, which is the highest frequency reported in any silicon-based amplifier.**

***Index Terms*— Embedding, maximum achievable gain ($G_{\max}$), millimeter-wave and terahertz (THz), power gain, stability.**

I. Introduction

SUBMILLIMETER-WAVE and terahertz (THz) frequencies have found various applications in different fields from commercial to security and medicine [1]–[11]. In most of these applications, transceivers are the vital part of the system. One of the most important issues in transceiver design is signal amplification. Amplification is important since it improves the signal-to-noise ratio and data rate as well as the transceiver range. Signal amplification at submillimeter-wave and THz frequencies, however, is challenging. On the one hand, these frequencies are very close to $f_{\max}$ of active devices [12]–[16], meaning the available gain from the active device is low. On the other hand, high losses of input and output matching networks reduce the total power gain of the amplifier even further. Therefore, at these frequencies, the total power gain is very close to, or even less than, unity.

To address the power gain issue, designers usually unilateralize the active two-port (A2P), which is usually a single transistor, to improve stability and increase the power gain to unilateral power gain (U) of the A2P [17]–[24]. Nevertheless, this technique suffers from a few drawbacks. Unilateralization may not increase the power gain very much, and in some cases, U is even less than the maximum available gain (G_{ma}) of the A2P. Moreover, even if unilateralization improves the gain slightly in theory, the loss of passive components used for unilateralization neutralizes the gain-boosting effect of this technique.

It has been shown that maximum achievable gain ($G_{\max}$) of an embedded A2P is considerably higher than its U [25]–[28]. Hence, a promising solution to the problem of power gain at frequencies near $f_{\max}$ is boosting the power gain to $G_{\max}$ using an appropriate embedding. As proposed in [26], two different embeddings are discussed to improve the power gain by movement in a gain-plane. However, it does not provide an analytical solution to increase the power gain to $G_{\max}$.

In this paper, for the first time, we propose a general embedding with its exact derivations and calculations to boost the power gain of an embedded A2P to $G_{\max}$. The embedding is used to create the required movement in the gain-plane, which is used to visualize the effect of the embedding. The only information that is used to find the elements of the embedding is the Y-parameters of the A2P. Moreover, the proposed technique makes it possible to design the embedding to achieve any arbitrary power gain up to $G_{\max}$ of the A2P. The proposed embedding is applied to a 10 μm common-source NMOS transistor in a 65 nm CMOS process with an $f_{\max}$ of 352 GHz to implement a four-stage amplifier. The amplifier features a power gain of 9.2 dB at 260 GHz that shows a significant improvement compared with the state of the art.

The remainder of this paper is organized as follows. Section II gives a short review of three basic power gain definitions that are used in Section III. In Section III, the gain-plane and its properties are studied. The embedding elements values are calculated and derived for any desired gain including $G_{\max}$. Section IV studies the practical limitations of such gain boosting. In Section V, a four-stage embedded amplifier at 260 GHz is presented using the proposed embedding, and the measurement results are illustrated. Finally, Section VI concludes this paper.

II. Basic Gain Definitions

In this section, we review three basic power gain definitions for a two-port, and their relationships. This review proves useful when we maximize the power gain in Section III.

A. Maximum Available Gain (G_{ma})

Maximum available gain (G_{ma}) of a two-port is defined as the ratio of the available power from the output port of the two-port to the available power from the source. G_{ma} is achieved when the source and load impedances are conjugate-matched to the input and output ports of the two-port simultaneously.

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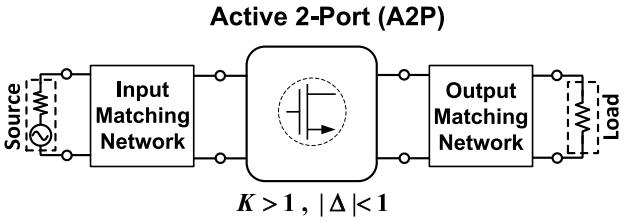


Fig. 1. Conditions under which maximum available gain (G_{ma}) is defined for a two-port (an A2P here).

Simultaneous matching is possible only when the two-port is unconditionally stable [29].

Fig. 1 shows a two-port that is active and unconditionally stable. The A2P in Fig. 1 is shown as a black box and represents any active transistor-based circuit combination throughout this paper. The simple and popular combinations are common–emitter and common-source amplifiers. For an amplifier to be unconditionally stable, the amplifier's stability measures K and Δ must satisfy $K > 1$ and $|\Delta| < 1$ conditions [29]. G_{ma} of an A2P can be written as a function of its parameters:

$$G_{ma} = |A|(K - \sqrt{K^2 - 1}), \quad \text{where } A = \frac{Y_{21}}{Y_{12}} = \frac{Z_{21}}{Z_{12}}. \quad (1)$$

Z_{ij} is the Z-parameter of the A2P, and $i, j = 1, 2$. Fig. 2(a) shows G_{ma} of a 10 μm common-source NMOS transistor in a 65 nm CMOS process versus frequency. Fig. 2(b) shows that G_{ma} is only defined at frequencies higher than 255 GHz in which both the stability measures are satisfied.

B. Unilateral Power Gain (U)

This power gain is defined as G_{ma} of an A2P that is unilateralized using a linear-lossless-reciprocal (LLR) embedding. Fig. 3 shows the conditions under which U is defined. U is given below as a function of the Y-parameters of the A2P:

$$U = \frac{|Y_{21} - Y_{12}|}{4(\mathrm{Re}[Y_{11}] \cdot \mathrm{Re}[Y_{22}] - \mathrm{Re}[Y_{12}] \cdot \mathrm{Re}[Y_{21}])}. \quad (2)$$

Fig. 2(a) shows U of the same 10 μm transistor. The figure depicts that U is defined even at frequencies in which $K < 1$. Moreover, U is invariant under LLR embedding [30]. In other words, U is only a function of the A2P parameters and LLR embedding does not change it. Fig. 2(a) shows that U of the transistor is just slightly larger than its G_{ma} in a limited frequency range (271–352 GHz). In practice, the loss of the embedding reduces the power gain of the unilateralized transistor well below the theoretical U in this frequency range.

C. Maximum Achievable Gain ($G_{\max}$)

Maximum achievable gain ($G_{\max}$) is the maximum G_{ma} of an LLR embedded A2P. In other words, if we embed an A2P by a tunable LLR embedding and match the input and output of the resulting two-port, as shown in Fig. 4, $G_{\max}$ is the maximum power gain, and is given as [26]

$$G_{\max} = (2U - 1) + 2\sqrt{U(U - 1)}. \quad (3)$$

This equation depicts that $G_{\max}$ is only a function of U and similar to U, is an inherent characteristic of any A2P. In addition, $G_{\max} \approx 4U$ (6 dB larger than U) when $U \gg 1$. This can be clearly seen in Fig. 2(a). This difference is more important at submillimeter-wave and THz frequencies where G_{ma} and U of the A2P drop significantly. It shows that boosting the power gain to $G_{\max}$ is a promising solution to high-gain amplifier design at frequencies near $f_{\max}$.

III. T-Embedding: A General Solution to Reach $G_{\max}$

In this section, a general LLR embedding called T-embedding is proposed by which G_{ma} of the LLR-embedded A2P is boosted exactly to $G_{\max}$. To this end, G_{ma} of a two-port is described as a function of its U and A, and gain-plane is defined accordingly. LLR embedding is then interpreted as a movement in the gain-plane, and by an appropriate movement, G_{ma} is boosted to $G_{\max}$.

A. Gain-Plane and Maximum G_{ma}

G_{ma} of a two-port can be written as a function of its U and A as [26]

$$\frac{G_{ma}}{U} = \left| \frac{A - G_{ma}}{A - 1} \right|^2, \quad (4)$$

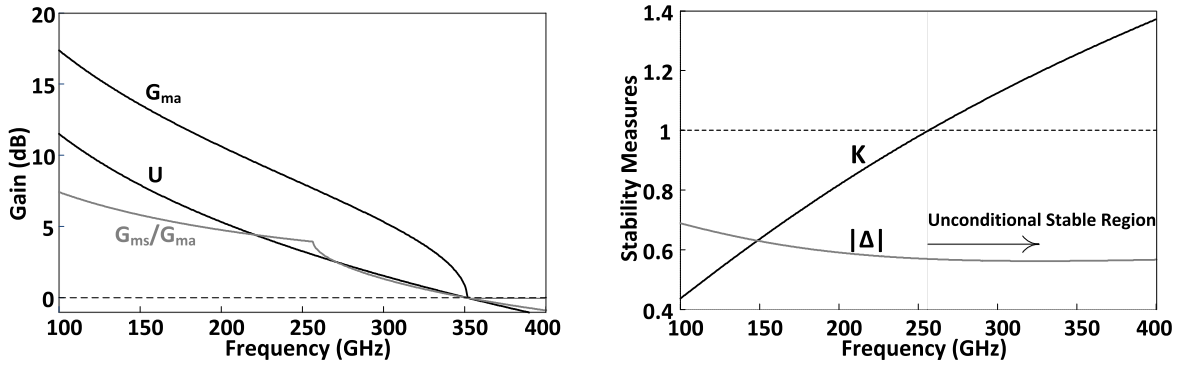
which suggests that we can change G_{ma} by changing A and/or U. To minimize the added loss to the network and to take advantage of a constant U, LLR embeddings are chosen to change G_{ma}. Thus, U is constant, and the problem of finding an LLR embedding that maximizes G_{ma} can be reduced to finding an LLR embedding that changes A in such a way that maximizes G_{ma} in (4) to reach $G_{\max}$. For the sake of brevity, "LLR embedding" is referred to as "embedding" in the rest of this paper.

As defined in (1), A is a complex number, while both G_{ma} and U are positive real numbers. Accordingly, G_{ma} of an embedded A2P is a function of two variables: the real part of A, and the imaginary part of A (U is constant). Assuming $|A| \gg 1$, (4) can be simplified to

$$\frac{U}{G_{ma}} = \left(\mathrm{Re}\left(\frac{U}{A}\right) - \frac{U}{G_{ma}} \right)^2 + \left(\mathrm{Im}\left(\frac{U}{A}\right) \right)^2. \quad (5)$$

The derivation of (5) is shown in Appendix B. This equation describes the locus of a group of equi-gain circles in a plane whose horizontal axis is $\mathrm{Re}(U/A)$ and vertical axis is $\mathrm{Im}(U/A)$. This plane is called the gain-plane. Each circle has a center at $((U/G_{ma}), 0)$ and a radius of $\sqrt{U/G_{ma}}$. These circles are shown in Fig. 5 for $G_{ma} = U$, $2U$, and $3U$, and an arbitrary value less than U. It will be shown that only an arc of each circle is acceptable as an equi-gain locus. Thus, the first three equi-gain circles are reduced to their acceptable arcs in Fig. 5. Each two-port corresponds to a coordinate in the gain-plane based on its U and A. The position of the 10 μm common-source NMOS transistor is shown in Fig. 5 as a black dot. Changing A by applying an embedding moves the corresponding point in the gain-plane. This interpretation will be used to boost G_{ma} to $G_{\max}$.

The basic limitation on the equi-gain arcs is stability. To find the stable region, (4) can be used in conjunction with



(a) (b)

Fig. 2. Power gains and the stability measures of a 10 μm common-source NMOS transistor in a 65 nm CMOS process. (a) G_{ma}, U, and $G_{\max}$. (b) K and $|\Delta|$.

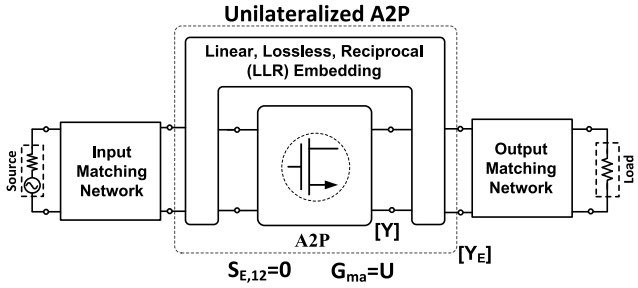


Fig. 3. Unilateralized A2P. $S_{E,12} = 0$.

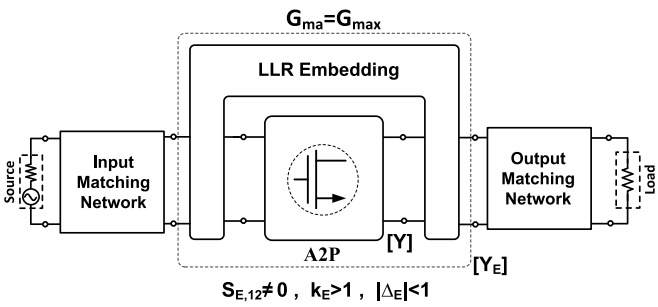


Fig. 4. LLR embedding that increases G_{ma} to $G_{\max}$. The embedded A2P is unconditionally stable.

inequality $K > 1$. The boundary that represents $K = 1$ is a parabola when $|A| \gg 1$. The equation that expresses the parabola in the gain-plane is

$$\left(\mathrm{Im}\left(\frac{U}{A}\right)\right)^2 = \mathrm{Re}\left(\frac{U}{A}\right) + 1/4. \tag{6}$$

The inside and outside regions of this parabola correspond to $K > 1$ and $K < 1$, respectively. Although $|\Delta|$ satisfies the stability criteria in most practical applications, it must be checked to guarantee unconditional stability inside of the parabola.

Each circle in Fig. 5 is tangential to this parabola at two points. These points split each circle into two arcs: the left arc and the right arc. Only the left arc of each circle is acceptable as a locus of equi-gain coordinates. Moving from a tangential point on an arbitrary circle increases K from 1. Therefore, on the right arc, $K - \sqrt{K^2 - 1}$ and $|A|$ decrease simultaneously (K and $|(U/A)|$ both increase). Referring to (1), this simultaneous decrease reduces G_{ma}, and hence, the right arcs do not represent locus of constant G_{ma}, and hence is not acceptable.

Fig. 5 shows that as G_{ma} increases, the corresponding equi-gain arc moves to the left in the gain-plane, and hence, the coordinate that corresponds to the maximum G_{ma} is $(-(1/4), 0)$ assuming $|A| \gg 1$, and is shown by a gray dot in Fig. 5. G_{ma} at this point is equal to $4U$, and therefore, $G_{\max} = 4U$. However, this number is an approximation, since (5) and (6) are found assuming $|A| \gg 1$. To find the exact value of $G_{\max}$, (4) should be simplified using the following two conditions at $G_{\max}$: $\mathrm{Im}(A) = 0$ and $K = 1$. The resulting equation is shown in (3), and therefore, the exact coordinate of the point that corresponds to $G_{ma} = G_{\max}$ is $\left(-\frac{U}{(2U-1)+2\sqrt{U(U-1)}}, 0\right)$ as shown in Fig. 5.

It must be noted that as the frequency increases and becomes closer to $f_{\max}$, both U and $(2U-1)+2\sqrt{U(U-1)}$ decrease and become closer to unity. Therefore, as the frequency goes up, the assumption of $|A| \gg 1$ is not correct anymore, and the point that corresponds to $G_{\max}$ deviates from $(-(1/4), 0)$, moves to the left, and reaches $(-1, 0)$ at $f_{\max}$.

B. Movement in the Gain-Plane and T-Embedding

After locating the exact coordinate of the point that corresponds to $G_{\max}$ in the gain-plane, the next step is finding an embedding that causes a movement from the coordinate of the A2P to that of $G_{\max}$. This movement provides us with two numbers: one is the change in the real part of A and the other is the change in the imaginary part of A. These two numbers will be used to find the embedding that boosts G_{ma} to $G_{\max}$. Here, we study two embeddings, called parallel and series embeddings, and the movements that they cause.

Fig. 6(a) shows the parallel embedding. The embedding is done by adding a passive element with an admittance of jB_P between the input and output terminals of the A2P. It can be simply shown that

$$\mathbf{Y_{EP}} = \mathbf{Y} + \begin{bmatrix} jB_P & -jB_P \\ -jB_P & jB_P \end{bmatrix} \tag{7}$$

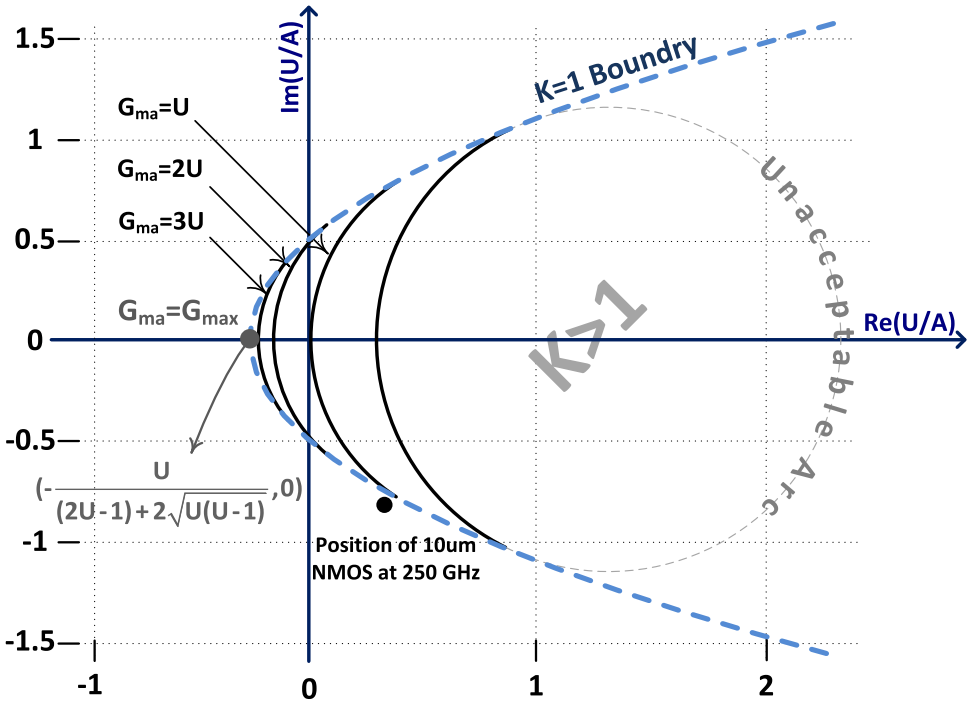
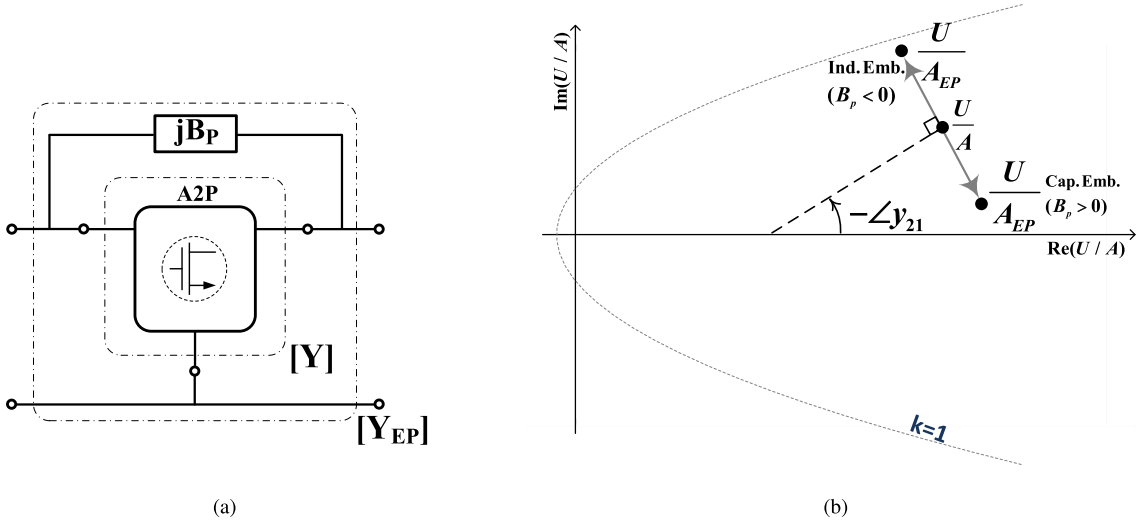


Fig. 5. Gain-plane and the constant G_{ma} arcs inside of $K > 1$ region. U is constant everywhere in the gain-plane.



(a) (b)

Fig. 6. (a) A2P embedded by a parallel inductor or capacitor. (b) Movements caused by these embeddings in the gain-plane.

where $\mathbf{Y}$ and $\mathbf{Y_{EP}}$ are the admittance matrices of the A2P and embedded A2P, respectively. To calculate the movement caused by this embedding, we need to find the coordinate of the embedded A2P. Assuming $|B_P| \ll |Y_{21}|$, the coordinate is

$$\frac{U}{A_{EP}} \simeq U \cdot \left(\frac{1}{A} - \frac{jB_P}{Y_{21}}\right) = \frac{U}{A} - \frac{jB_p \cdot U}{Y_{21}}. \tag{8}$$

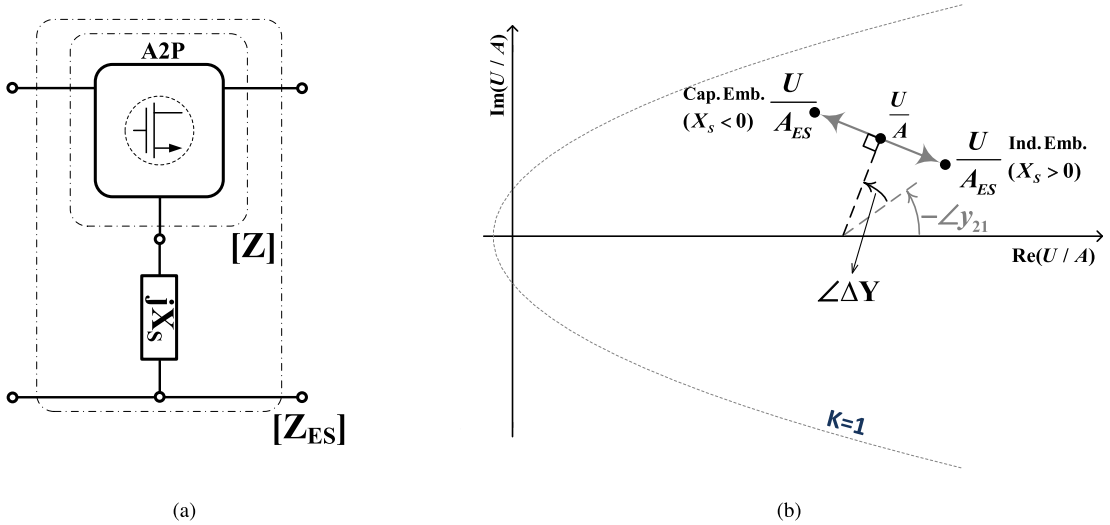
According to (8), below, for small values of B_P, the magnitude of this movement is $U \cdot |(B_P\ /Y_{21})|$, and its phase is $\pm(\pi/2) - \angle Y_{21}$. For an inductive parallel embedding ($B_P < 0$), the phase of the movement is $+(\pi/2) - \angle Y_{21}$, and when it is capacitive ($B_P > 0$), the phase is $-(\pi/2) - \angle Y_{21}$. These movements are shown in Fig. 6(b) for an arbitrary $\mathbf{Y}$ and B_P.

Fig. 7(a) shows the series embedding. The embedding is done by adding a passive element with an impedance of jX_S in series with the common terminal of the A2P. $\mathbf{Z}$ (or $\mathbf{Y^{-1}}$) and $\mathbf{Z_{ES}}$ are the impedance matrices of the A2P and the embedded A2P, respectively. It can be shown that the impedance matrix of the embedded A2P is

$$\mathbf{Z_{ES}} = \begin{bmatrix} \frac{Y_{22}}{\Delta Y} + jX_S & \frac{-Y_{12}}{\Delta Y} + jX_S \\ \frac{-Y_{21}}{\Delta Y} + jX_S & \frac{Y_{11}}{\Delta Y} + jX_S \end{bmatrix} \tag{9}$$

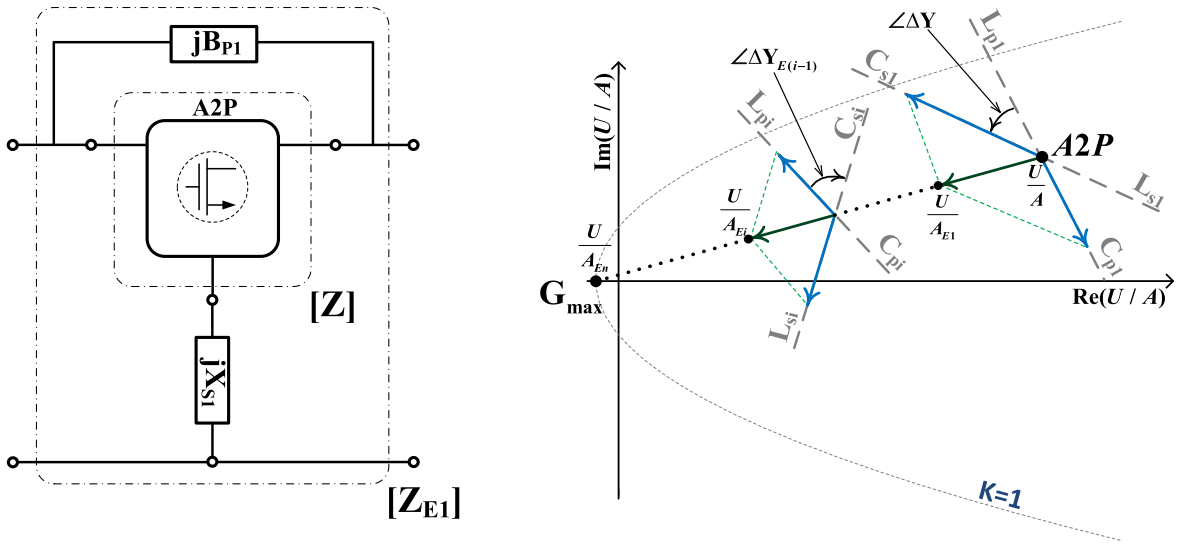
where ΔY is $\Delta Y = Y_{11} \cdot Y_{22} - Y_{12} \cdot Y_{21}$. Assuming $|X_S| \ll |(Y_{21}/\Delta Y)|$, the coordinate of the embedded A2P by the series embedding in the gain-plane is

$$\frac{U}{A_{ES}} \simeq \frac{U \cdot Y_{12}}{Y_{21}} - \frac{jX_S \cdot \Delta Y \cdot U}{Y_{21}} = \frac{U}{A} - \frac{jX_S \cdot \Delta Y \cdot U}{Y_{21}}. \tag{10}$$



(a) (b)

Fig. 7. (a) A2P embedded by a series inductor or capacitor. (b) Movements caused by these embeddings in the gain-plane.



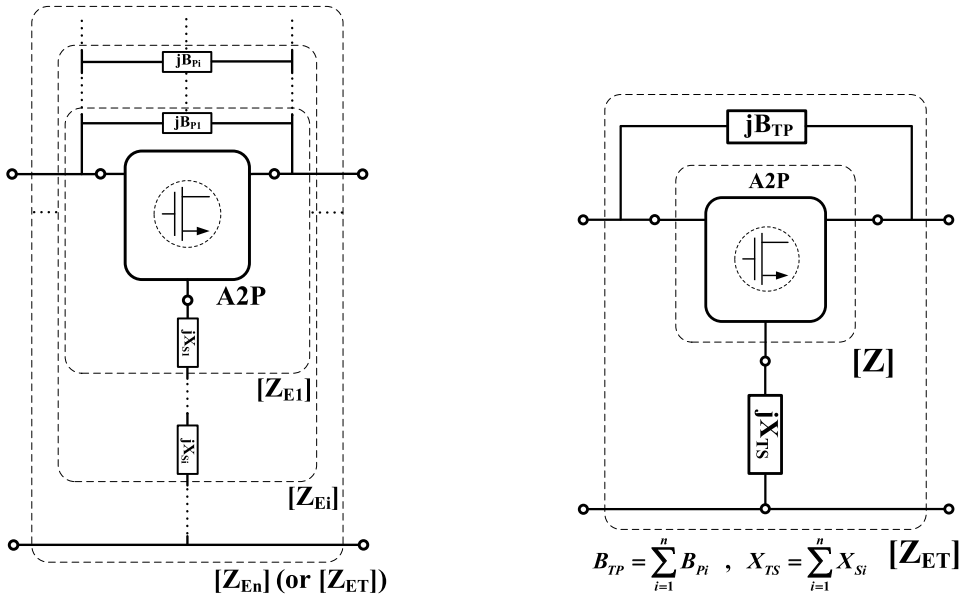
(a) (b)

Fig. 8. (a) A2P embedded by parallel and series embeddings simultaneously. (b) Movement due to B_{P1} and X_{S1} is toward the coordinate of $G_{\max}$. The movement can be done n times to reach $G_{\max}$.

The amplitude of the movement is $|((X_S \cdot \Delta Y \cdot U)/Y_{21})|$, and its phase is $\pm(\pi/2) - \angle Y_{21} + \angle \Delta Y$. Plus and minus signs are for capacitive and inductive embeddings, respectively. These movements are shown in Fig. 7(b) for an arbitrary $\mathbf{Y}$ and X_S. The phases of the movements in this case are different from that of the parallel embedding by $\angle \Delta Y$. This phase difference makes it possible to select any arbitrary direction for the movement in the gain-plane when both parallel and series embeddings are applied to A2P. This feature proves useful when considering the fact that the coordinate of the A2P can be anywhere in the gain-plane.

The superposition of the movements caused by these embeddings results in an omnidirectional movement in the gain-plane. Fig. 8(a) shows the A2P embedded simultaneously by parallel and series embeddings, and Fig. 8(b) shows the movement due to these simultaneous embeddings. In Fig. 8(b), L and C specify whether the embeddings are inductive or capacitive, and the subscripts p and s represent whether the embedding is parallel or series, respectively. In this figure, the coordinate of the A2P is $\frac{U}{A}$, which is the starting point of the movement toward $G_{\max}$. The figure depicts that by a correct choice of B_{P1} and X_{S1}, a small movement is feasible toward any arbitrary point in the gain-plane, including $G_{\max}$, independent of the A2P coordinate. As shown in the figure, the embedded A2P has moved to a new point, (U/A_{E1}), toward the coordinate of $G_{\max}$.

However, these movements are relatively small to satisfy the assumptions behind our derivations. Therefore, multiple small movements should be made to reach $G_{\max}$ exactly. Fig. 8(b) also shows the movement due to the ith embedding. Since the starting point of this movement is different from the original A2P, the required embedding to have the same



(a) (b)

Fig. 9. (a) A2P embedded n times by parallel and series embeddings. (b) Embeddings are combined and simplified to two embedding elements $B_{\rm TP}$ and $X_{\rm TS}$.

movement in the same direction will be different. This fact is graphically illustrated in this figure. For example, if the first movement needed two capacitors, the ith movement may need two inductors to move toward $G_{\max}$.

By a large number of small movements (n times), the coordinate of the starting point, the coordinate of A2P, can be changed to that of $G_{\max}$. These movements correspond to n different embeddings and are shown in Fig. 9(a). As shown in the figure, by combining all the small embeddings, we arrive at one single parallel and series passive element that boost the gain to $G_{\max}$. $B_{\rm TP}$ and $X_{\rm TS}$ are the sum of B_{Pi} and X_{Si} values, respectively. In Section III-C, the elements of this T-shape embedding, $B_{\rm TP}$ and $X_{\rm TS}$, are derived as a function of the Y-parameters of the A2P.

C. T-Embedding: Elements Derivation and Verification

To derive the embedding elements $B_{\rm TP}$ and $X_{\rm TS}$ shown in Fig. 9(b), $\mathbf{Z_{ET}}$, the impedance matrix of the final embedded A2P, is calculated using $B_{\rm TP}$, $X_{\rm TS}$, and the Z-parameters of the A2P. Next, A of the embedded A2P, A_{ET}, is found from $\mathbf{Z_{ET}}$. From the gain-plane, the following conditions are required at $G_{\max}$:

$$\mathrm{Re}\left(\frac{U}{A_{ET}}\right) = -\left(\frac{U}{G_{\max}}\right) \ \ \& \ \mathrm{Im}\left(\frac{U}{A_{ET}}\right) = 0. \tag{11}$$

After applying these conditions to A_{ET}, $X_{\rm TS}$ and $B_{\rm TP}$ are obtained as

$$\begin{aligned} X_{\rm TS} &= \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \\ B_{\rm TP} &= -\frac{R_{21} + G_{\max} R_{12}}{(1 + G_{\max}(\mathrm{Im}(\Delta Z) + X_{\rm TS} M))} \end{aligned} \tag{12}$$

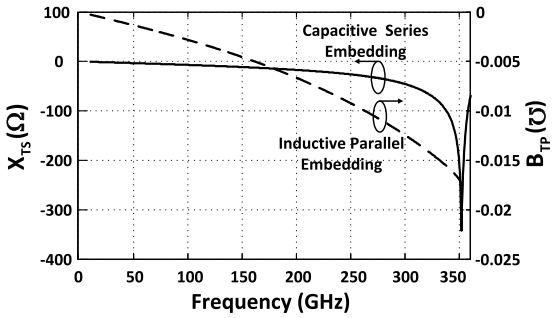


Fig. 10. Calculated $B_{\rm TP}$ and $X_{\rm TS}$ for the 10 μm common-source transistor to achieve $G_{\max}$.

where

$$\begin{aligned} a &= (1 + G_{\max})M \\ b &= (X_{21} + G_{\max} X_{12})M + (R_{21} + G_{\max} R_{12})N + (1 + G_{\max}) \\ &\quad \times \mathrm{Im}(\Delta Z) \\ c &= (R_{21} + G_{\max} R_{12})\mathrm{Re}(\Delta Z) + (X_{21} + G_{\max} X_{12})\mathrm{Im}(\Delta Z) \end{aligned} \tag{13}$$

and

$$\begin{aligned} \Delta Z &= Z_{11} Z_{22} - Z_{12} Z_{21} \\ M &= R_{11} + R_{22} - R_{12} - R_{21} \\ N &= X_{12} + X_{21} - X_{11} - X_{22}, \\ Z_{ij} &= R_{ij} + j X_{ij} \quad \& \ i, j = 1, 2. \end{aligned} \tag{14}$$

Z_{ij} are the elements of impedance matrix of the A2P. The complete derivation of (12)–(14) is given in Appendix A. These equations show that only the Z-parameters of the A2P are used to calculate $B_{\rm TP}$ and $X_{\rm TS}$. Although the square root term in (12), $b^2 - 4ac$, is positive for most transistors, for the

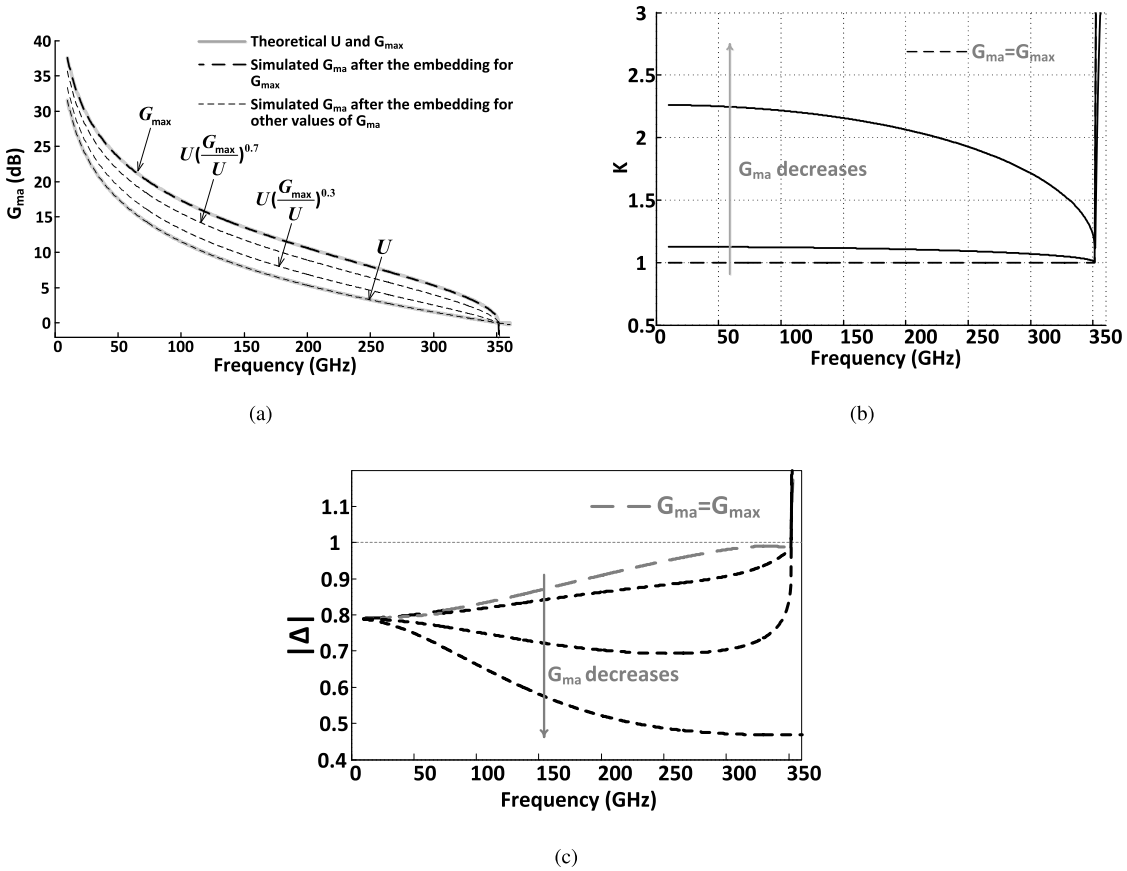
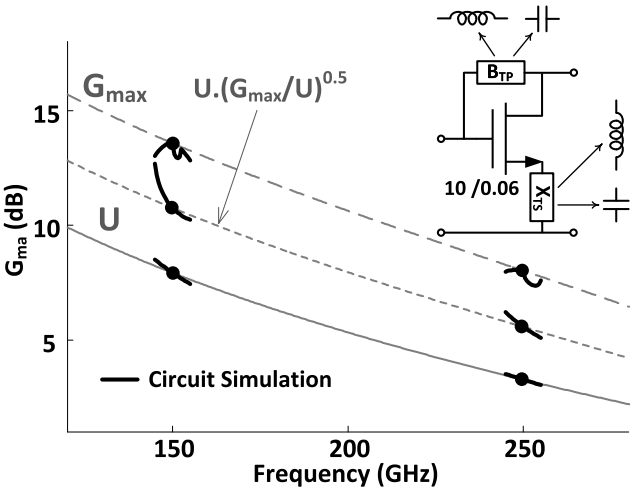


Fig. 11. (a) Theoretical and simulated G_{ma} values for the same 10 μm transistor embedded by T-embedding. (b) Corresponding K values (K of $G_{ma} = U$ is infinity). (c) Corresponding $|\Delta|$ values.

rare cases that it is less than zero, it can be made positive using pre-embedding, which is discussed in Section IV.

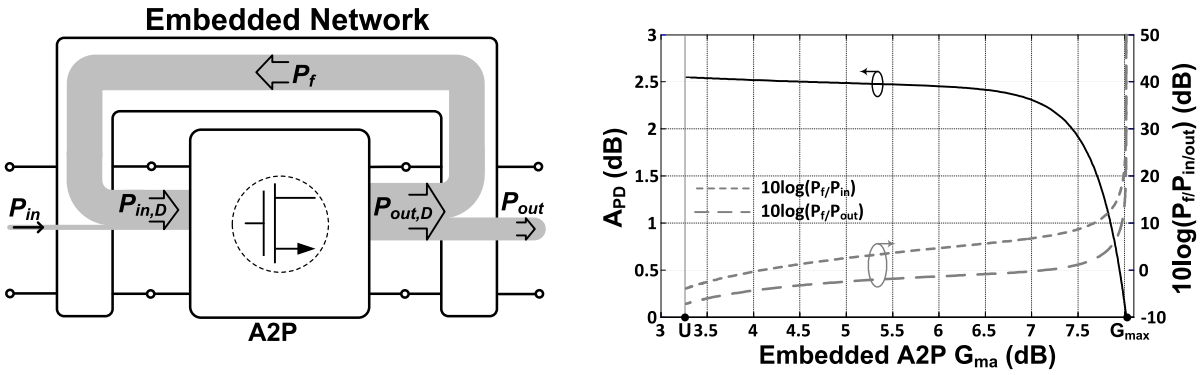
Reaching any arbitrary G_{ma} up to $G_{\max}$ can be done using the proposed embedding as well. From a stability viewpoint, the crossing point of the equi-gain arc and the horizontal axis is targeted to reach G_{ma}. It can be shown that to reach such a point (e.g., G_{ma}), we only need to substitute the $G_{\max}$ term in (12) and (13) with $U \cdot (\sqrt{(U/G_{ma})} - (U/G_{ma}))^{-1}$. The proposed technique guarantees that after embedding $K > 1$. The embedding process is independent of $|\Delta|$, and it has to be less than one only after embedding to make certain the amplifier is unconditionally stable. Therefore, the value of $|\Delta|$ has to be checked after embedding. In practice, one of the two solutions in (12) results in an unconditionally stable amplifier. The embedding has been applied to several A2Ps, including BJT and CMOS transistors with various sizes and pin arrangements. In all of these cases, $|\Delta|$ is always smaller than one.

To verify the proposed embedding, the same 10 μm common-source NMOS transistor is used as the A2P. Using its Z-parameters, the embedding elements of T-embedding, B_{TP} and X_{TS}, are calculated to reach $G_{\max}$ at all frequencies. These values are shown in Fig. 10. Fig. 11(a) shows the simulated G_{ma} of the transistor embedded by B_{TP} and X_{TS} shown in Fig. 10 to reach $G_{\max}$ (the thick black dashed line). It can be seen that T-embedding boosts G_{ma} to the theoretical $G_{\max}$. For the same transistor, and using the corresponding embeddings, G_{ma} is also boosted to U, $U \cdot (G_{\max}/U)^{0.3}$, and $U \cdot (G_{\max}/U)^{0.7}$. Here, for all the simulations, minus sign is selected in (12) as it leads to $|\Delta| < 1$.



Gma / Freq.	U	U.(U/Gmax)^0.5	Gmax
150 GHz	B_{TP}: L= 308.30 pH X_{TS}: L= 8.39 pH	B_{TP}: L= 245.90 pH X_{TS}: C= 175.52 fF	B_{TP}: L= 232.80 pH X_{TS}: C= 93.39 fF
250 GHz	B_{TP}: L= 127.06 pH X_{TS}: L= 5.02 pH	B_{TP}: L= 77.42 pH X_{TS}: C= 52.36 fF	B_{TP}: L= 68.95 pH X_{TS}: C= 24.32 fF

Fig. 12. Theoretical and circuit simulation results comparison of three different G_{ma} values of the same 10 μm embedded transistor at 150 and 250 GHz.



(a) (b)

Fig. 13. (a) Quantitative illustration of the power flow in a gain-boosted embedded A2P. (b) Input and output powers normalized to the feedback power and A2P power gain of the same 10 μm transistor at 250 GHz.

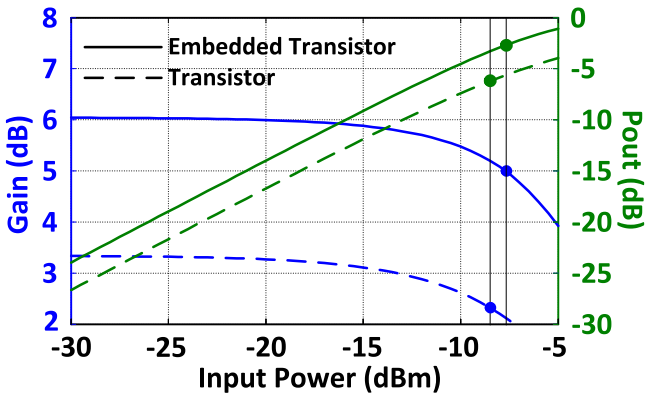


Fig. 14. Maximum available gain and 1-dB compression point of a 10 μm NMOS transistor with/without embedding at 260 GHz.

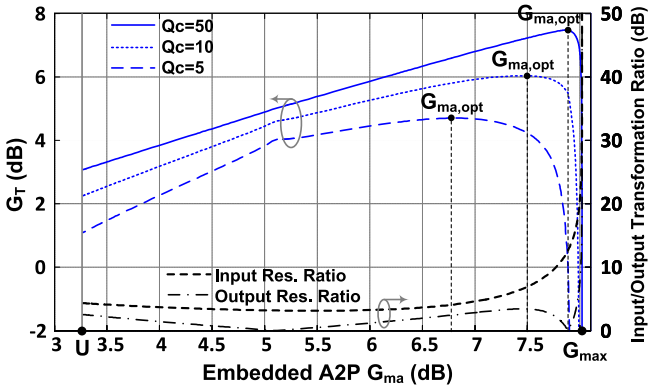


Fig. 15. Input/output resistance transformation ratio ($10 \times \log_{10}(T_{\text{in/out}})$), and the total power gain (G_T) versus G_{ma} of the embedded transistor.

Fig. 11 (b) and (c) shows the simulated stability measures of the embedded transistors versus frequency. Circuit simulation is done to verify T-embedding properties. To perform circuit simulation, the embedding elements B_{TP} and X_{TS} are calculated at two frequencies (150 and 250 GHz) for three different values of G_{ma} (U, $U \cdot (G_{\max}/U)^{0.5}$, and $G_{\max}$). The equivalent inductances or capacitances of B_{TP} and X_{TS} are calculated and given in Fig. 12. The transistor is embedded by the resulting capacitors and inductors, and G_{ma} values of the embedded A2Ps are simulated. The simulation results and the calculated values shown in Fig. 12 are in perfect agreement.

IV. Practical Design Considerations in a Gain-Boosted Amplifier

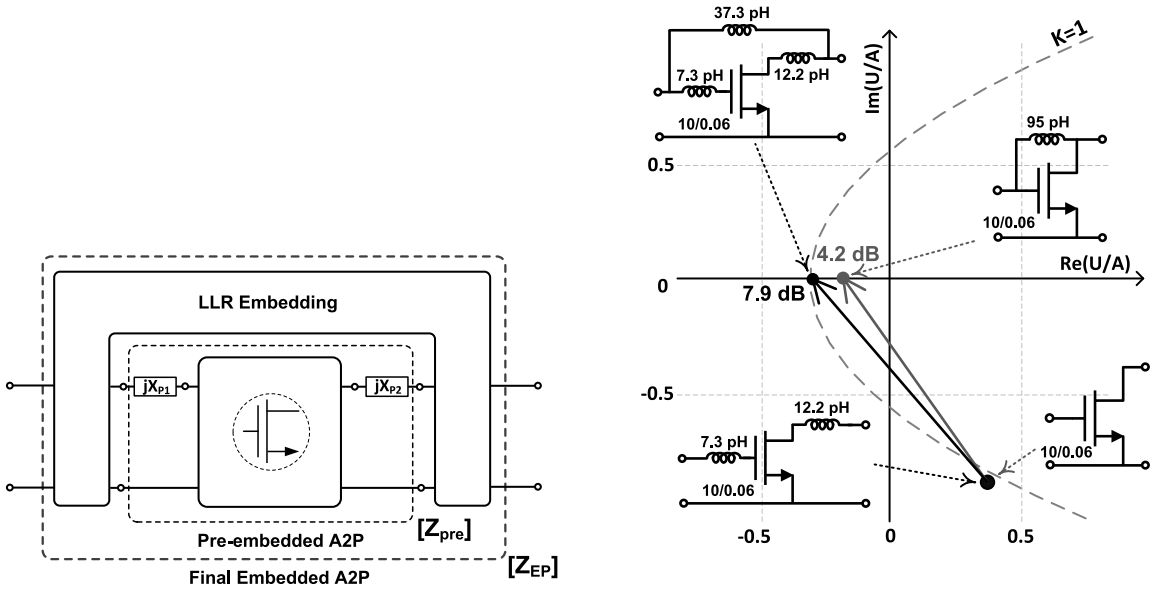
A. Power Flow in a Gain-Boosted Amplifier

Fig. 13(a) shows a quantitative illustration of the power flow in a generic gain-boosted embedded A2P, where P_f is the feedback power via the T-embedding. In such a situation, the power gain of the A2P ($P_{\text{out},D}/P_{\text{in},D}$) can be much smaller than the power gain of the amplifier ($P_{\text{out}}/P_{\text{in}}$). This is evident from the power gain derivation shown in the following:

$$A_{\text{PD}} = \frac{P_{\text{out},D}}{P_{\text{in},D}} = \frac{P_{\text{out}} + P_f}{P_{\text{in}} + P_f} = \frac{\frac{P_{\text{out}}}{P_{\text{in}}} + \frac{P_f}{P_{\text{in}}}}{\frac{P_{\text{in}}}{P_{\text{in}}} + \frac{P_f}{P_{\text{in}}}} = \frac{G_{ma} + \frac{P_f}{P_{\text{in}}}}{1 + \frac{P_f}{P_{\text{in}}}}. \tag{15}$$

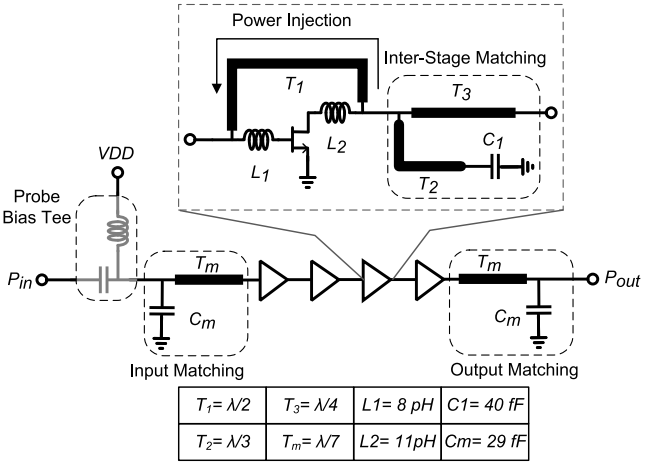
Here, P_{in}, P_{out}, and P_f are the input power and output power of the embedded A2P, and the feedback power via T-embedding, respectively. $P_{\text{in},D}$ and $P_{\text{out},D}$ are the input and output power of the A2P, respectively.

In the right-hand side of (15), both P_f and P_{in} are positive numbers. Therefore, for any $G_{ma} > 1$, it can be simply shown that $A_{\text{PD}} < G_{ma}$. The larger the ratio P_f/P_{in} is, the bigger the difference between A_{PD} and G_{ma} will be. Simulated P_f/P_{in}, P_f/P_{out}, and A_{PD} are plotted versus G_{ma} in Fig. 13(b) for the same embedded 10 μm common-source NMOS transistor at 250 GHz. As G_{ma} gets closer to $G_{\max}$, P_f/P_{in} and P_f/P_{out} increase, and at $G_{ma} = G_{\max}$, they become very large. A very large P_f/P_{in} results in $A_{\text{PD}} \simeq 1$ based on (15), when $G_{ma} = G_{\max}$. As shown in Fig. 13(b), simulated A_{PD} goes to 0 dB as it is expected. This means in practice due to high feedback power, boosting the gain to exactly $G_{\max}$ may not be feasible. This is because the



(a) (b)

Fig. 16. (a) A2P preembedded by X_{P1} and X_{P2}. (b) Gain boosting with/without pre-embedding when the series capacitor is removed.



T_1= λ/2	T_3= λ/4	L1= 8 pH	C1= 40 fF
T_2= λ/3	T_m= λ/7	L2= 11pH	Cm= 29 fF

Fig. 17. Circuit schematic of the proposed four-stage embedded amplifier for maximum gain boosting.

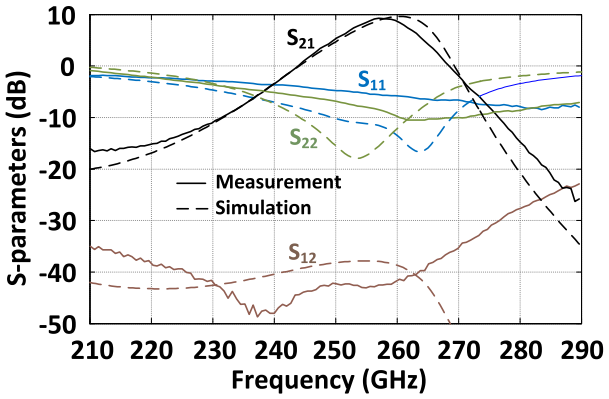


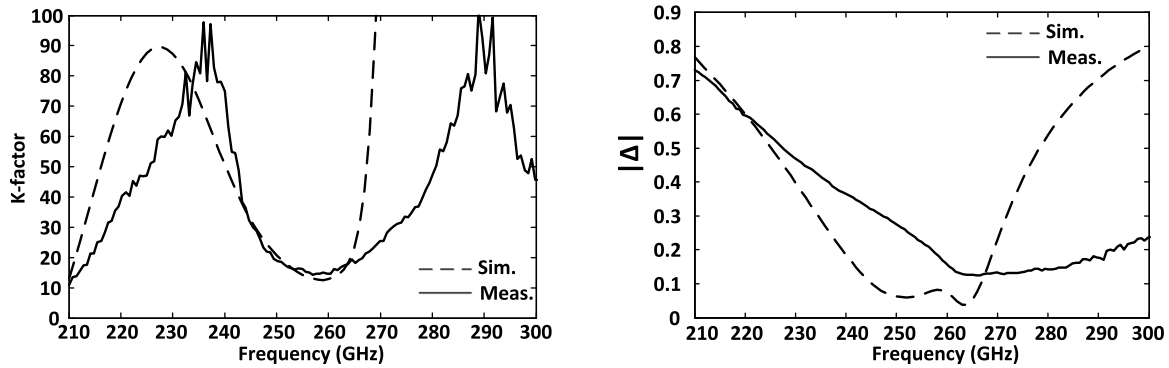
Fig. 18. Simulated and measured S-parameters of the proposed gain-boosted amplifier.

high power flow in real embedding elements results in high power loss, which significantly reduces the overall power gain. However, it is practical to get reasonably close to $G_{\max}$, as shown in Fig. 13(b).

One may speculate that the feedback power through T-embedding network degrades the linearity of the embedded A2P by decreasing its input 1-dB compression point. However, the linearity of an embedded amplifier is a function of several parameters, including the input power of A2P as well as the impedances seen by the input and output ports of the A2P. Since the proposed gain boosting technique changes the impedances seen by the input and output ports of A2P, it cannot be concluded that gain boosting necessarily degrades linearity. For example, a 10 μm common-source NMOS transistor is simultaneously matched to the source and load at 260 GHz where it is unconditionally stable, and features a G_{ma} of 3.3 dB. As shown in Fig. 14, its simulated input and output 1-dB compression points are -8.5 and -6.2 dBm, respectively. Then, the transistor is embedded using T-embedding to boost G_{ma} to 6 dB at 260 GHz. In this case, the simulated input and output 1-dB compression points are -7.95 and -2.95 dBm, respectively. This shows that the linearity has improved after gain boosting, verifying that linearity does not necessarily degrade with gain boosting.

B. Effect of the Matching Loss on the Maximum Power Gain

T-embedding feeds back a part of output power of the A2P to its input. This in turn reduces the real part of the input impedance of the embedded A2P. Accordingly, an embed-



(a) (b)

Fig. 19. Stability measures simulation and measurement results. The amplifier is unconditionally stable.

ded A2P with higher G_{ma} has a smaller input resistance. Assuming a constant load and source, reduction in the real part of the input impedance increases the resistance transformation ratio. The loss of a matching network is worse when the resistance transformation ratio is higher. Therefore, there must be an optimum G_{ma} that maximizes the total power gain from the source to the load (G_T).

To investigate this effect and find the optimum value of G_{ma}, the total gain which includes the input and output matching networks losses is calculated. Here, we assume the matchings are done using an L-match structure that consists of a capacitor and an inductor. The quality factor of the inductors is neglected as inductors at millimeter-wave and THz frequencies have much higher quality factors than capacitors. It can be shown that the power efficiency of an L-match network, η, is [31]

$$\eta_{\text{in/out}} = 1 - \frac{\sqrt{T_{\text{in/out}} - 1}}{Q_C} \tag{16}$$

where Q_C is the quality factor of the capacitor used in the matching networks. T is the resistance transformation ratio and is given as

$$T_{\text{in/out}} = \frac{R_{\text{port}}}{R_0} \quad \text{if } R_{\text{port}} > R_0$$
$$T_{\text{in/out}} = \frac{R_0}{R_{\text{port}}} \quad \text{if } R_{\text{port}} < R_0. \tag{17}$$

For the input matching network (T_{in}), R_{port} is the input resistance of the embedded A2P, and R_0 is the source resistance. For the output matching network (T_{out}), R_{port} is the output resistance of the embedded A2P and R_0 is the load resistance. Supposing η_{in} and η_{out} are the power efficiencies of the input and output matching networks, respectively, the total power gain, G_T, can be written as

$$G_T = \eta_{\text{in}} \cdot G_{ma} \cdot \eta_{\text{out}} \tag{18}$$

η_{in} and η_{out} are functions of the resistance transformation ratios, T_{in} and T_{out}, respectively, and these resistance transformation ratios change when G_{ma} changes. Hence, both η_{in} and η_{out} are functions of G_{ma}. Accordingly, for a given source, load, and capacitor quality factor, G_T is only a function of G_{ma}.

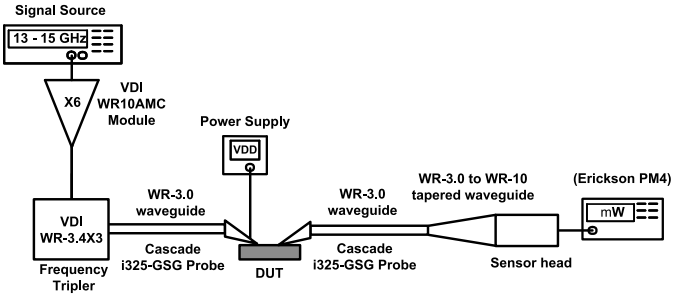


Fig. 20. Test setup for large-signal measurements. The internal Bias Tee of Cascade i325-GSG Probe is used to bias the amplifier.

G_{ma} of an embedded A2P is swept from U to $G_{\max}$ by changing the embedding. The total power gain, G_T, is then plotted versus G_{ma} of the embedded A2P for three different Q_C values in Fig. 15. The A2P is selected to be the same 10 μm transistor. It can be seen, for $Q_C = 5$, the optimum G_{ma} is 6.8 dB, which is very different from $G_{\max}$.

C. Pre-embedding

In practice, the calculated T-embedding may impose some limitations in terms of loss or dc bias and/or isolation on the embedded A2P. For example, Fig. 10 shows that the series embedding of the 10 μm common-source NMOS transistor is a capacitor at 250 GHz, which can be very lossy. Moreover, this mandates the need for a bypass inductor for dc current, which is also very lossy. To overcome this issue, it is desirable to remove the capacitor. To do so, pre-embedding can be used. As shown in Fig. 16(a), for the 10 μm transistor, the pre-embedding is selected to consist of two passive elements jX_{P1} and jX_{P2}. The pre-embedding shown in this figure does not alter A and hence does not change the coordinate of the two-port in the gain-plane. However, it changes the direction of the movement by the same embedding element. Using (10), it can be shown that the direction of the movement changes by $\Delta\varphi = \angle\Delta Z - \angle\Delta Z_{\text{pre}}$, where ΔZ and ΔZ_{pre} are the determinants

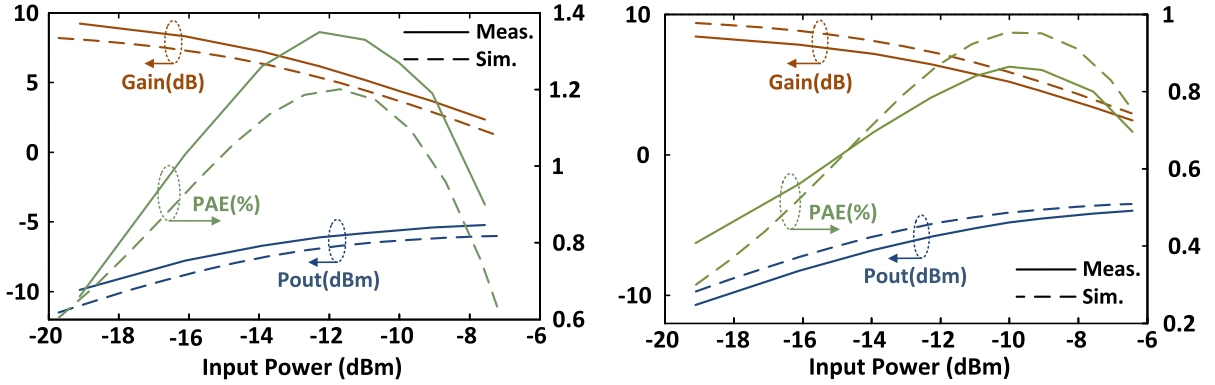


Fig. 21. Power added efficiency, output power, and large-signal gain of the amplifier for (a) $V_{DD} = 0.8$ V and (b) $V_{DD} = 1$ V.

of the impedance matrices of the A2P and the preembedded A2P, respectively.

To verify the pre-embedding shown in Fig. 16(a), the series capacitor is removed and the transistor is embedded by parallel embedding with and without pre-embedding. The movements with and without pre-embedding are shown in Fig. 16(b). The figure illustrates that the final power gain is 3.7 dB lower if the pre-embedding is not used. The transistor with pre-embedding reaches almost $G_{\max}$ of 8 dB at 250 GHz.

V. Implemented Amplifier and Measurement Results

To show the feasibility of the proposed embedding in boosting G_{ma}, a four-stage embedded amplifier is fabricated in a 65 nm CMOS technology at 260 GHz. To increase $f_{\max}$, two 5 μm NMOS transistors are used in parallel to achieve an $f_{\max}$ of 352 GHz, and they are used as the core of the embedded amplifier stages. Fig. 17 shows the circuit schematic of the proposed four-stage embedded amplifier. G_{ma} and $G_{\max}$ of this transistor are 3.6 and 7.5 dB at 260 GHz, respectively. Simulations show that the series embedding that is needed to reach $G_{\max}$ is capacitive, and it is desirable to eliminate it and use pre-embedding as discussed in Section III-C. To boost G_{ma} to 7.4 dB at 260 GHz, the lossless pre-embedding elements, X_{P1} and X_{P2}, and the parallel embedding are found to be 7, 12.3, and 37.5 pH, respectively. As shown in Fig. 17, the real pre-embedding elements are lossy, and hence slightly different from the calculated lossless elements. The parallel embedding T_1 is implemented using a microstrip transmission line and behaves as a 50 pH inductor in the circuit. The pre-embedding along with T_1 boosts G_{ma} to 6 dB, which is 2.4 dB higher than G_{ma} of the transistor.

In this design, input/output matching and interstage matchings introduce the loss of 1.8 and 3.6 dB, respectively. Therefore, the total simulated power gain of the amplifier is 9.6 dB. All of the components that are used for embedding and impedance matching are implemented using microstrip transmission lines and metal–oxide–metal (MOM) capacitors.

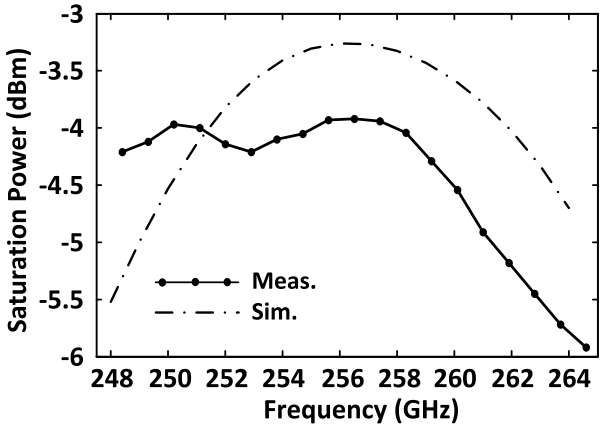


Fig. 22. Simulated and measured saturated output power as a function of frequency.

As shown in Fig. 18, the amplifier has a maximum measured small-signal gain of 9.2 dB at 257 GHz and the input and output reflection coefficients of -5.5 and -8.5 dB, respectively. Fig. 19 shows that the proposed amplifier is unconditionally stable in simulation and measurement. The chip consumes 27.6 mW of power from a 1-V supply in Figs. 18 and 19.

Fig. 20 shows the setup that is used for large-signal measurements. As shown in Fig. 21, at 255 GHz, the maximum power-added efficiency (PAE) is 1.35% with VDD = 0.8 V, and the maximum output saturated power (P_{sat}) is -3.9 dBm with VDD = 1 V. The amplifier consumes 13.7 and 27.6 mW at VDD = 0.8 V and VDD = 1 V, respectively. Fig. 22 shows the simulation and measurement results of saturation power as a function of frequency when VDD = 1 V.

The die micrograph is shown in Fig. 23, and the chip size is 800 $\times$ 180 μm^2. Table I presents a summary of the implemented four-stage amplifier and compares its performance with the state-of-the-art. The amplifier has the highest operation frequency among the reported amplifiers in any silicon technology. The saturated output power (P_{sat}) of the amplifier is higher than any silicon-based amplifier

TABLE I
COMPARISON OF THE FABRICATED AMPLIFIER WITH STATE-OF-THE-ART

Ref.	Tech.	f_{max} (GHz)	Freq. (GHz)	Gain (dB)	3-dB BW (GHz)	Sup. Vol. (V)	P_{1-dB} (dBm)	P_{sat} (dBm)	Peak PAE (%)	P_{DC} (mW)	Topology	Area (mm^2)
[15]	25 nm InP HEMT	1500	1000	9	100[1]	N/A	N/A	N/A	N/A	N/A	10 CS stages	N/A
[32]	130 nm SiGe HBT	435	220	16	28	3.6	N/A	N/A	N/A	144	3 Diff. Cascode Stages	0.45
[33]	250 nm InP DHBT	550	324	4.8	3 (2-dB)	1.4	N/A	1.1	0.6	16.8	1 CB stage	0.12
[34]	50 nm InP HEMT	1200	340	15	25[1]	2.2	N/A	10	N/A	294.8	4 CE stages	0.49
[35]	40 nm CMOS	275	213.5	10.5	13	0.8	-7.2	-3.2	0.75	42.3	9 CS stages	0.013
[36]	50 nm InP HEMT	N/A	220	10.4	30	2.2	18	N/A	3.7	2165	4 CS stages 8 power comb.	0.96
[37][2]	250 nm InP HBT	700	190-260	28	70	N/A	19[3]	N/A	4.5	1770	3 Cascode stages 4 power comb.	1.536
[38] [2]	130 nm InP DHBT	1100	670	24	150	1.8	N/A	-4	N/A	N/A	9 CB stages	0.3123
[39]	32 nm SOI CMOS	320	210	15	14	1	2.7	4.6	6	40	3 Neutralized diff. stages	0.06
This work	**65 nm CMOS**	**345 GHz**	**257**	**8.5**	**12.2**	**0.8**	**-8**	**-5.5**	**1.3**	**13.7**	**4 CS stages**	**0.14**
This work	**65 nm CMOS**	**352 GHz**	**257**	**9.2**	**12.2**	**1**	**-8**	**-3.9**	**0.8**	**27.6**	**4 CS stages**	**0.14**

[1] Estimation from the reported results.
[2] High-gain version.
[3] Maximum output power.

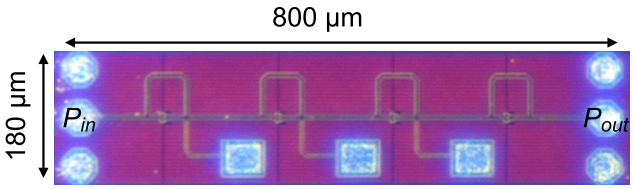


Fig. 23. Chip microphotograph.

beyond 220 GHz. Other specifications are comparable with amplifiers in compound semiconductors with considerably higher $f_{\max}$.

VI. CONCLUSION

A general embedding is proposed to boost the power gain of an embedded A2P to $G_{\max}$. The proposed technique utilizes movement in the defined gain-plane to boost the power gain. The required movements are achieved by only two passive components as parallel and series embeddings. These embeddings are analyzed and calculated for any given A2P using only its Z-parameters. Implementation issues are investigated as well as the circuit characteristics of the embedded network. To show the feasibility of the proposed embedding, a four-stage embedded amplifier is implemented in a 65 nm CMOS technology with a power gain of 9.2 dB at 260 GHz.

APPENDIX A
EMBEDDING ELEMENTS CALCULATION

To calculate the value of the final embeddings, X_{TS} and B_{TP}, we start with calculating A of the embedded A2P, A_{ET}, and we select the values of the embeddings such that the coordinate of the embedded A2P in the gain-plane is $(-(U/G_{\max}), 0)$. We suppose that the A2P in Fig. 9(b) is embedded first by X_{TS}, then by B_{TP}. Using (7) and (9), it can be shown that

$$A_{ET} = \frac{Y_{ET,21}}{Y_{ET,12}} = \frac{\left(-\frac{Z_{21}+jX_{\mathrm{TS}}}{\Delta Z_{ES}}\right)+jB_{\mathrm{TP}}}{\left(-\frac{Z_{12}+jX_{\mathrm{TS}}}{\Delta Z_{ES}}\right)+jB_{\mathrm{TP}}} = \frac{Z_{21}+jX_{\mathrm{TS}}-jB_{\mathrm{TP}}\cdot\Delta Z_{ES}}{Z_{12}+jX_{\mathrm{TS}}-jB_{\mathrm{TP}}\cdot\Delta Z_{ES}} \tag{19}$$

where Z_{ij} is the element of the A2P impedance matrix ($\mathbf{Z}$), and ΔZ_{ES} is given by

$$\Delta Z_{ES} = (Z_{11}+jX_{\mathrm{TS}})\cdot(Z_{22}+jX_{\mathrm{TS}}) - (Z_{12}+jX_{\mathrm{TS}})\cdot(Z_{21}+jX_{\mathrm{TS}}). \tag{20}$$

At the coordinate that corresponds to $G_{\max}$, $(-(U/G_{\max}), 0)$, we have $A_{ET} = -G_{\max}$, therefore

$$-G_{\max} = \frac{Z_{21}+jX_{\mathrm{TS}}-jB_{\mathrm{TP}}\cdot\Delta Z_{ES}}{Z_{12}+jX_{\mathrm{TS}}-jB_{\mathrm{TP}}\cdot\Delta Z_{ES}}. \tag{21}$$

Equation (21) in fact consists of two equations: one the real part and the other one the imaginary part. These equations are

found to be

$$B_{\mathrm{TP}} \cdot \mathrm{Im}(\Delta Z_{ES}) \cdot (1 + G_{\max}) + R_{12} \cdot G_{\max} + R_{21} = 0 \quad (22)$$

and

$$j[B_{\mathrm{TP}} \cdot \mathrm{Re}(\Delta Z_{ES}) \cdot (1 + G_{\max}) + X_{\mathrm{TS}} \cdot (1 + G_{\max}) + G_{\max} \cdot X_{12} + X_{21}] = 0. \quad (23)$$

Solving (22) and (23) for X_{TS} and B_{TP} results in (12).

APPENDIX B
PROOF OF EQUATION OF $K > 1$ BOUNDARY

For $K = 1$, we have [26]

$$K - \sqrt{K^2 - 1} = 1 \quad (24)$$

or

$$G_{ma} = |A|. \quad (25)$$

Recalling (5), on the boundary of $K > 1$, we have

$$\frac{|A|}{U} = \left| 1 - \frac{|A|}{U} \cdot \mathrm{Re}\left(\frac{U}{A}\right) - j\frac{|A|}{U} \cdot \mathrm{Im}\left(\frac{U}{A}\right) \right|^2. \quad (26)$$

Hence

$$\frac{|A|}{U} = 1 - 2\left|\frac{A}{U}\right| \cdot \mathrm{Re}\left(\frac{U}{A}\right) + 1 \quad (27)$$

that is

$$\frac{1}{2} = \left|\frac{U}{A}\right| - \mathrm{Re}\left(\frac{U}{A}\right) \quad (28)$$

that is

$$\left(\frac{1}{2} + \mathrm{Re}\left(\frac{U}{A}\right)\right)^2 = \left|\frac{U}{A}\right|^2 \quad (29)$$

which results in

$$\frac{1}{4} + \mathrm{Re}\left(\frac{U}{A}\right) = \left(\mathrm{Im}\left(\frac{U}{A}\right)\right)^2. \quad (30)$$

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