

A 0.065-mm² 19.8-mW Single-Channel Calibration-Free 12-b 600-MS/s ADC in 28-nm UTBB FD-SOI Using FBB

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Abstract—A 0.065-mm² single-channel calibration-free 12-b analog-to-digital converter (ADC) sampling at 600 MS/s in 28-nm ultrathin body bias fully depleted silicon on insulator (FD-SOI) is presented. The selected hybrid architecture, incorporating pipelined and asynchronous successive approximation register ADC, demonstrates advantages and suitability of different design techniques utilizing forward body bias (FBB) capability of FD-SOI. Using an FBB voltage range of 0–1.8 V has enabled an signal-to-noise plus distortion ratio (SNDR) improvement of more than 9 dB. An integrated body bias generator ensures the required voltages for FBB. This paper demonstrates 61.5-dB and 60.7-dB SNDR at low and Nyquist input frequency, respectively, at 600-MS/s sampling frequency. The Walden FoM of 37.2 fJ/conv-step and Schreier FoM of 162.5 dB at 600 MS/s are achieved in Nyquist conditions. Speed robustness of the architecture has been demonstrated by achieving 57-dB SNDR at 800MS/s, >50-dB SNDR up to 950 MS/s, and 58.5-dB SNDR till 500-MHz input frequency at 600 MS/s.

Index Terms—Analog-to-digital converter (ADC), asynchronous successive approximation register (ASAR), body bias generator (BBGEN), forward body bias (FBB), fully depleted silicon on insulator (FD-SOI), split reference architecture, ultrathin body bias (UTBB), unity gain frequency (fu).

I. INTRODUCTION

LOW power and low area are key requirements in most of the modules of communication systems, starting from the base stations to the hand-held devices. Analog-to-digital converters (ADCs) often dominate the overall performance of communication system modules. Various ADC architectures are available to address performance metrics area, power, and speed. For instance, one of the most widely used technique to improve ADC speed is time interleaving [1]. The speed gain achieved by time interleaving is primarily limited by the speed and area of a single-channel ADC. Larger dimensions of the single-channel ADC result in long routing traces of clock and

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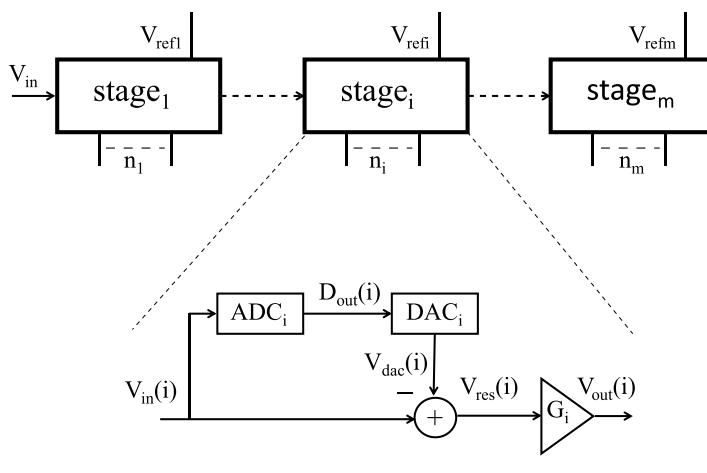
input signals across channels, which result in more parasitic capacitances and resistances when increasing the number of ADC channels. Furthermore, the parasitic capacitances and resistances increase with scaling down of CMOS technology. This limits the maximum number of channels that can be interleaved. In this paper, we focus on maximizing the performance of single-channel ADCs in terms speed, power, and area.

There has been a lot of work [2]–[6] on improving the speed of single-channel pipelined ADCs where some innovative techniques are already published. The hybrid ADC approach as demonstrated in [7]–[10] is another way to improve performance metrics of the ADC. Our work is also based on a hybrid converter architecture [11].

The ultrathin body bias fully depleted silicon on insulator (UTBB FD-SOI) technology lends itself to very simple ways to implement novel design techniques that exploit bulk biasing of the MOS transistor [12]–[14]. The bulk terminal of the MOS transistor can be isolated, and driven easily up to few volts in the positive and negative direction. In some publications, various digital processing SOCs, employing adaptive body biasing, achieve very good power efficiency [15]–[19]. This further entails the need to work on bulk biasing in the analog domain to attain better performance metrics. Adaptive body biasing facilitates the use of smaller switches and MOS devices by lowering the MOS threshold voltage.

This paper has been implemented in 28-nm UTBB FD-SOI technology; exploiting its forward body biasing (FBB) feature. This lowers the threshold voltage of transistors by approximately 85 mV/V, boosting the switching performance of logic gates. FBB also lowers the switch resistance in switched capacitor circuits enabling smaller switch transistors. Small switch transistors increase sampling speed thanks to a lower and more linear switch resistance. Small switches also reduce parasitic and decrease the MOS gate loading capacitance. These effects together help in improving the speed and limit the power of clock drivers and operational transconductance amplifier (OTA), which further translates to better performance. Other circuit innovations introduced in this design are a split reference scheme, an OTA with improved common-mode feedback circuit and an 8-bit asynchronous successive approximation register (ASAR)-based hybrid architecture.

This paper is organized as follows. Sections II and III discuss pipelined ADC and the architecture of this hybrid ADC.



V_{refi}	Reference voltage to stage i
ADC_i	The sub ADC of stage i
DAC_i	The sub DAC of stage i
$V_{\text{res}}(i)$	Residue in stage i
$V_{\text{in}}(i)$	Analog input to stage i
$V_{\text{out}}(i)$	Analog output of stage i
$D_{\text{out}}(i)$	The digital out of stage i
D_{out}	Total digital output of ADC
$V_{\text{dac}}(i)$	The output of the dac of stage i
n_i	Number of output bits in stage i
n_{tot}	Total number of bits of th ADC
N_i	Number of output codes in ADC_i
N_{tot}	Total number of output codes of ADC
G_i	Residue gain in stage i
m	Number of stages

Fig. 1. Pipelined ADC.

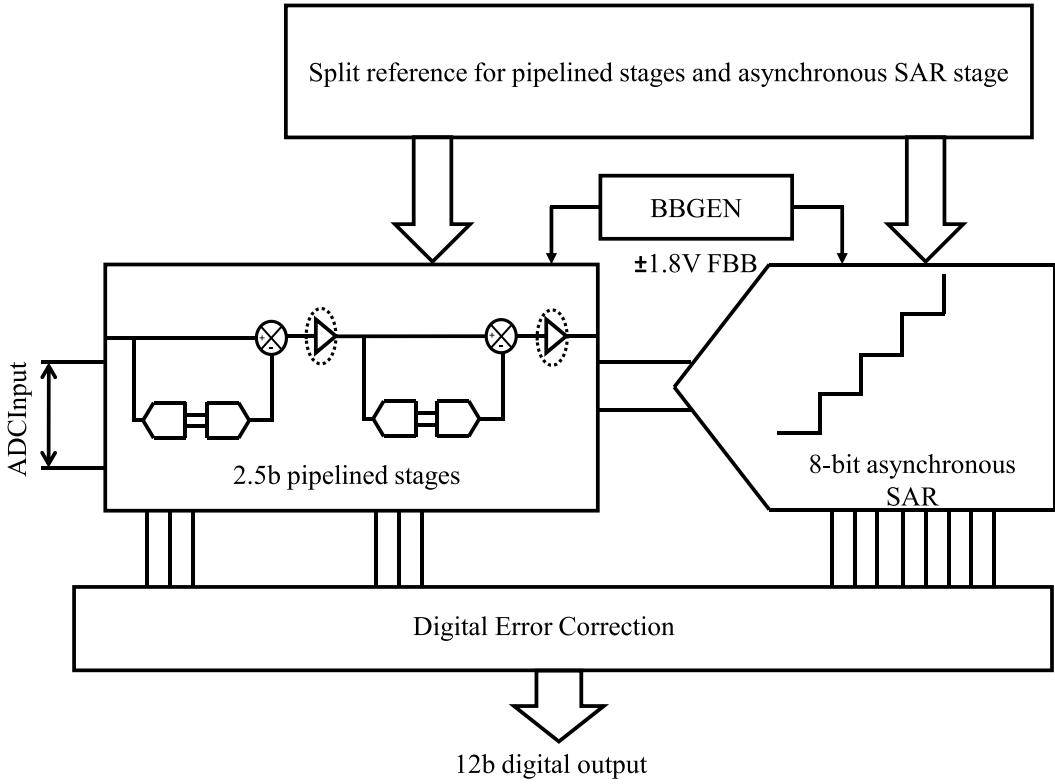


Fig. 2. ADC architecture.

The split reference voltage generation scheme is presented in Section IV. Section V discusses details of the use of forward bias schemes and analyzes the advantages of using FBB compared to the classical bootstrap switch-based design. Section VI discusses the internal body bias generator (BBGEN). Section VII explains the operational amplifier architecture and sharing scheme. Section VIII elaborates the details of asynchronous SAR and decide-right switching scheme [20]. Section IX discusses the design robustness from transistor leakage and the reliability concerns resulting

from FBB. Measurement results are presented in Section X. Section XI concludes the paper.

II. PIPELINED ADC ARCHITECTURE

Pipelined ADCs [21] consist of multiple stages and each stage has a coarse ADC and a multiplying DAC (MDAC). The latter consists of a subtractor and a residue gain amplifier as shown in Fig. 1. The output code of the ADC is given by

the following expression [22]:

$$D_{\text{out}} = \sum_{i=1}^m \left(D_{\text{out}}(i) \cdot \frac{N_m}{N_i} \cdot \prod_{k=i}^{m-1} G_k \right). \quad (1)$$

The symbols used in the equations are listed in Fig. 1. The equivalent input voltage of the corresponding output code is given by

$$V_{\text{in}} = \frac{\sum_{i=1}^m (D_{\text{out}}(i) \cdot V_{\text{ref}}(i) \cdot \frac{N_m}{N_i} \cdot \prod_{k=i}^{m-1} G_k)}{N_{\text{tot}}}. \quad (2)$$

Total number of output codes of the overall ADC, where $G_i = N_i$, are

$$N_{\text{tot}} = \prod_{i=1}^m N_i. \quad (3)$$

Most of the pipelined stages share the same voltage reference because all of them run at the same frequency, which is the desired sampling frequency of the overall ADC. The last stage of the pipelined ADC comprises only the sub ADC. The equivalent input voltage to the corresponding output code of the pipelined ADC is calculated as

$$V_{\text{in}} = V_{\text{ref}} \cdot \frac{\sum_{i=1}^m (D_{\text{out}}(i) \cdot \prod_{k=i+1}^m N_k)}{N_{\text{tot}}}. \quad (4)$$

Here all the pipelined stages share the same voltage reference and the residue gain of a stage is equal to the number of output codes of that particular stage.

III. ADC ARCHITECTURE

This paper presents a 12-bit calibration-free ADC, shown in Fig. 2, with two 2.5-bit pipelined stages followed by one 8-bit ASAR. This hybrid architecture uses a two-stage OTA which is shared between both the pipelined stages. Voltage references to the pipelined stages and asynchronous SAR stage are supplied by a new split reference scheme. FBB has been extensively used in this ADC architecture for logic gates and switch transistors which comprise large part of the asynchronous SAR and pipelined stages. An integrated BBGEN is used for the generation of the FBB voltage. Each 2.5-bit pipelined stage runs at a sampling frequency of 600 MHz and the ASAR at ~ 10 GHz. The SAR resolves 8-bits in half cycle of 600-MHz clock. The sampling capacitors of the first and second pipelined stages are 1.2 and 0.3 pF, respectively, whereas it is 64 fF for the asynchronous SAR stage.

IV. SPLIT REFERENCE ARCHITECTURE

All the stages of the pipelined ADC run at the same sampling rate; hence, traditionally a single voltage reference is shared among them. This hybrid ADC architecture is taking advantage of the high throughput of pipelined stages and zero dc power of SAR stage. It becomes difficult to design a single voltage reference to mitigate the high frequency switching transients of the later stage and this creates significant accuracy challenges for the integrated reference drivers. These high-frequency switching transients disturb the reference voltage of the ADC as shown in Fig. 3. There are multiple solutions to build accurate references for high frequency and high

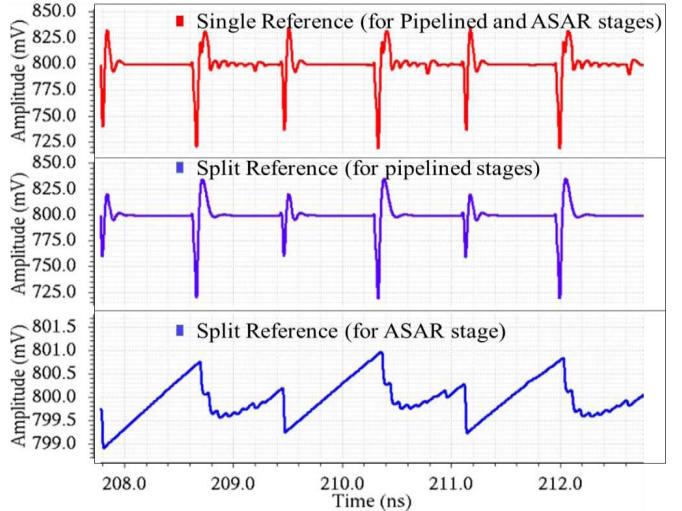


Fig. 3. Single reference versus split reference's transient response.

resolution ADCs. Each option is a trade-off between area and power. One of the solutions is to supply all required charge with large decoupling capacitor [8] at the cost of silicon area and the other one is to use a sufficiently high bandwidth reference driver, at the cost of more current consumption, to enable full settling of the switching transients at the desired sampling rate. However, for this, the high-bandwidth reference driver designed for the 1.5-pF capacitor of pipelined stages switching at a frequency of 600 MHz gets disturbed by the SAR stage, if this one is also connected to the same reference. The overall 12-bit accurate settling behavior of the reference voltage required for the pipelined stages deteriorates drastically as shown in Fig. 3.

In [23], the SAR ADC uses a dual reference scheme for MSB and LSB capacitors. The present design employs a similar approach of having separate reference drivers for different stages of the ADC. Reference signals provided to one stage of the hybrid ADC may suffer from interference caused by the other stages. In a classical dual reference scheme as shown in Fig. 4(a), the high-frequency interfering signals generated from ASAR switching may couple to the higher resolution reference signal of the pipelined ADC. To avoid such interference, a new split reference scheme is proposed. Two different drivers and a low-pass filter are arranged as shown in Fig. 4(b) to satisfy the specific reference requirements of both pipelined and ASAR stages.

The pipelined stage's reference voltage is low pass filtered and then applied as input to the reference drivers of the ASAR stage. As a result, the input to the ASAR reference drivers will be free from the large transient spikes as shown in Fig. 3. These spikes are attributed to the capacitor switching of the pipelined stages. This split reference scheme also eliminates the interference noise feedthrough generated by the ASAR as shown in Fig. 3, which is present in a single reference structure.

The digital output of this ADC, with digital error correction, is calculated as

$$D_{\text{out}} = D_{\text{out}}(1) \cdot 2^9 + D_{\text{out}}(2) \cdot 2^7 + D_{\text{out}}(3). \quad (5)$$

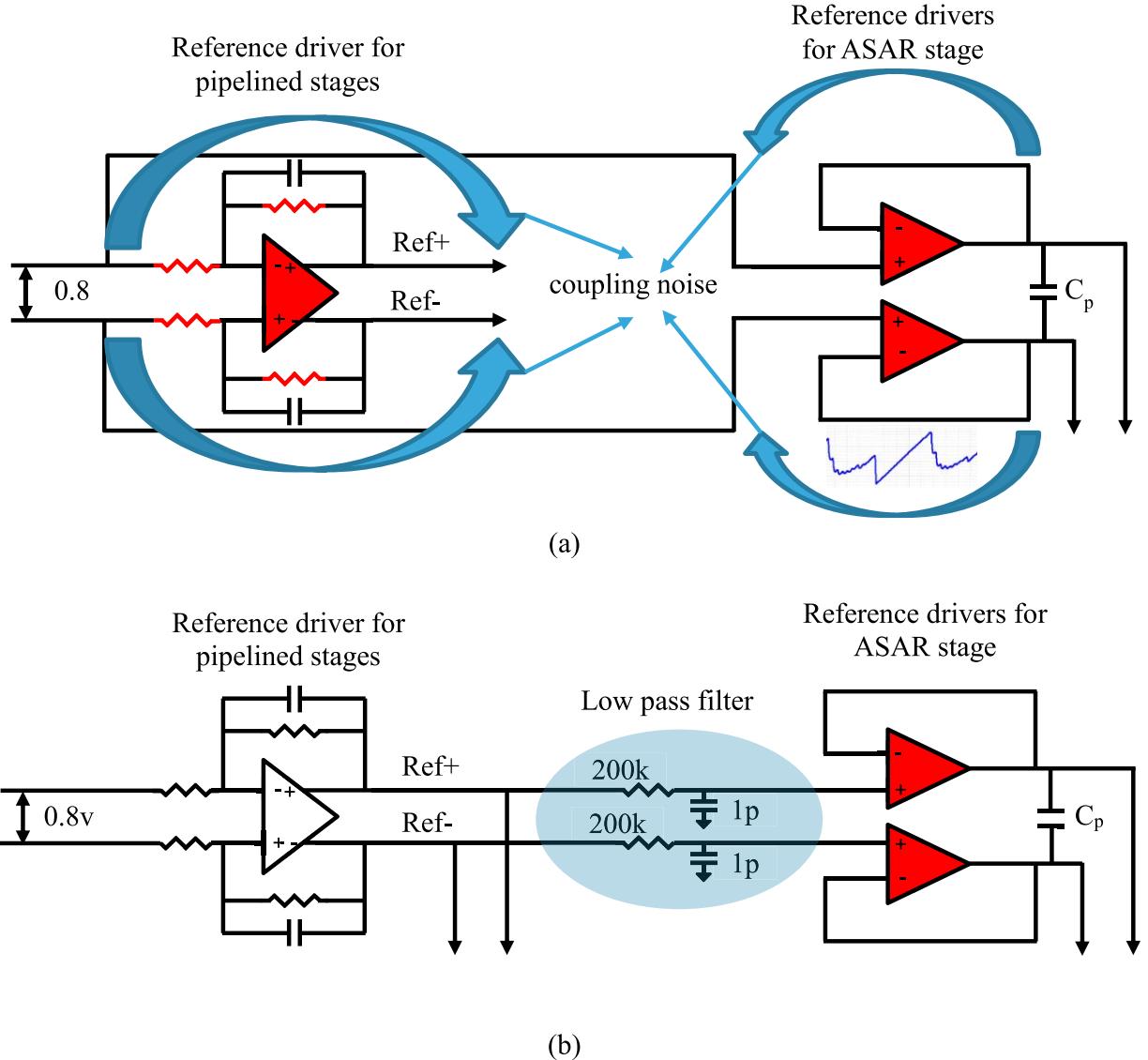


Fig. 4. (a) Classical way of splitting the reference. (b) Proposed split reference scheme.

$D_{\text{out}}(1)$ and $D_{\text{out}}(2)$ are digital outputs of first and second pipelined stage of the ADC. $D_{\text{out}}(3)$ is the digital output of the 8-bit asynchronous SAR stage. Since both pipelined stages share the same reference voltage $V_{\text{ref}1}$ and the ASAR stage has reference voltage $V_{\text{ref}2}$, the equivalent input voltage of the corresponding output code, for this 12-b ADC, will be

$$V_{\text{in}} = \frac{D_{\text{out}}(1) \cdot 2^9 \cdot V_{\text{ref}1} + D_{\text{out}}(2) \cdot 2^7 \cdot V_{\text{ref}1} + D_{\text{out}}(3) \cdot V_{\text{ref}2}}{N_{\text{tot}}} \quad (6)$$

The difference between the reference voltages *viz.* $V_{\text{ref}1}$ and $V_{\text{ref}2}$ gives rise to a gain mismatch error between the different stages of the ADC. Two pipelined stages before ASAR stage relax the matching requirement between the split references. Only 7.5-bit matching ($\sim \pm 0.5\%$ i.e., ± 8 mV with 1.6 Vp-p) is required between split references to achieve 72-dB SNDR as shown in Fig. 5.

The proposed split reference technique has an advantage in terms of the mismatch sources as compared to the

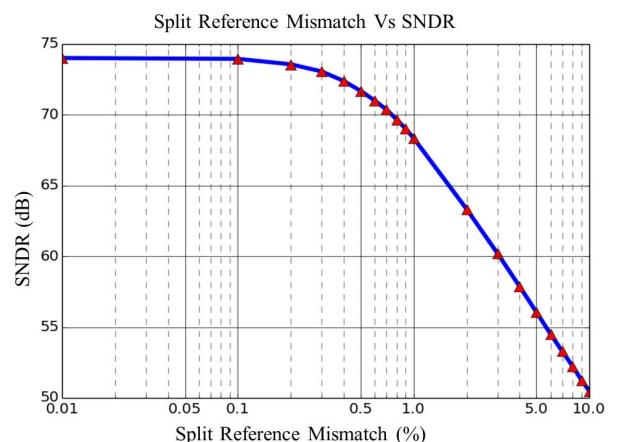


Fig. 5. SNDR versus split reference mismatch error (%).

classical technique. The mismatch sources of classical and split reference driver schemes are shown in Fig. 4(a) and (b), respectively, highlighted in red color. This clearly illustrates

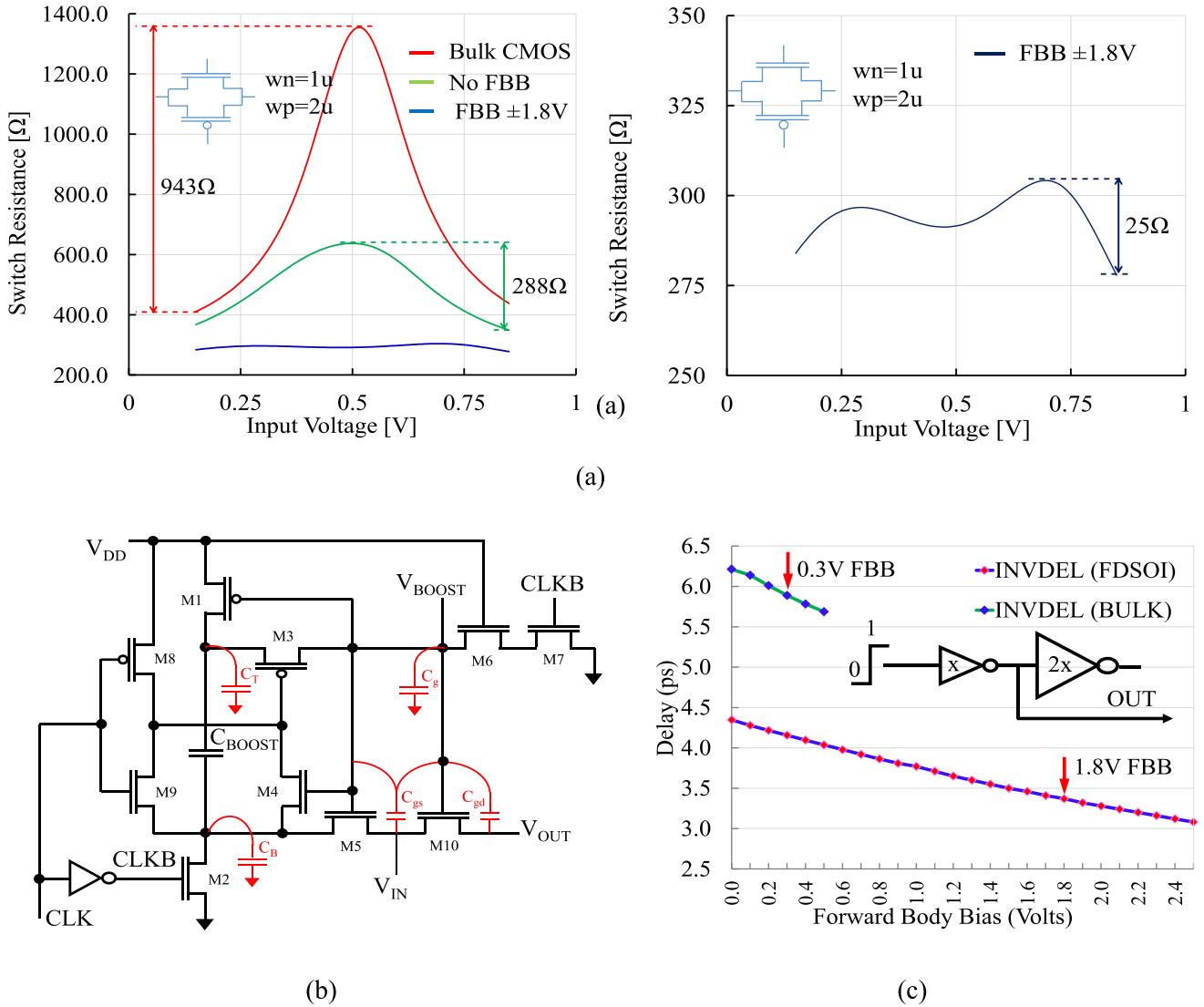


Fig. 6. (a) Switch resistance variation across whole input voltage range. (b) Conventional NMOS bootstrapped switch. (c) Inverter delay of bulk CMOS and UTBB FD-SOI technology with FBB.

the stringent requirements of the classical technique on gain, offset and resistor mismatch errors for first stage of the references, making it difficult to achieve a high bandwidth and high-resolution reference voltage. There is only one mismatch source between the reference voltage drivers in the proposed scheme. Therefore, the required matching between the references can be easily achieved for pipelined and ASAR stages. The total deviation ($\pm 3\sigma$) for ASAR reference gain and offset error is estimated to be ± 4.8 mV in computer-aided design (CAD) simulations, which is in the allowed range of ± 8 mV. Because of this split reference scheme, the ASAR references can be designed to have a low bandwidth capacitive load driver. Also, a 32-pF capacitor is used to provide charge to the 64-fF digital-to-analog converter (DAC) capacitor switched at ~ 10 GHz for more than 8-bit accuracy with the help of the decide-right scheme [20]. Finally, a high-bandwidth reference driver for the pipelined stages is designed easily to achieve the required settling on 1.5-pF pipelined stage capacitors switched at 600 MHz, without having to cope with interference by the ASAR switching as shown in Fig. 3. The low-pass filtered

value of the pipelined stages reference will be exactly the same as its cycle to cycle final settled value. Therefore, there is no need to have any external supply [9] for references, thus eliminating the need for any calibration requirement as in [9] for reference gain mismatch spurs between pipelined and ASAR stages.

V. FORWARD BODY BIAS

The threshold voltage of the MOS transistors can be adjusted by adaptively biasing its bulk terminal. The speed of the transistors can be increased by the FBB technique and this has already been exploited in bulk CMOS technology by digital processing system designers. The FBB is limited to 300 mV [24] due to the presence of the junction diode. Latch up risk also increases at higher voltage and temperature. Moreover, the body effect becomes weaker with technology scaling. The effective threshold voltage change in 130-nm CMOS technology is 210 mV/V [24], while it has been reduced to 25 mV/V [12] in 28-nm bulk CMOS. UTBB FD-SOI offers a very wide FBB range with the help of

flipped-well design technique and gives about 85 mV/V change in transistor threshold. In the flipped-well design technique [12], nMOS is implemented in N-well and pMOS in P-well. To achieve the full benefit of the extended range of the FBB, a deep N-well layer is used to separate the P-well from the p-substrate which is mostly connected to ground.

The ADC presented in this paper is extensively using the FBB feature of 28-nm UTBB FD-SOI. In this design, FBB of +1.8 V for nMOS and -1.8 V for pMOS is used to reduce the threshold voltage of the transistors, hence improving the linearity and speed of the switched capacitor blocks. MOS switch resistance variation across the whole voltage range improves by a factor of 40 as compared to the standard bulk CMOS process as shown in Fig. 6(a). This helps to have smaller switches with smaller parasitic capacitances to quickly switch between sample and hold mode and also reduce the loading of the amplifiers.

Switch resistance in switched capacitor circuits can also be improved by using bootstrapped switches. A conventional nMOS bootstrap switch [25] is shown in Fig. 6(b). When CLK is low, transistors M6 and M7 discharge the gate of M10 to ground. During this time, capacitor C_{BOOST} is charged to V_{DD} by M1 and M2. When CLK goes high, the gate of the transistor M10 (V_{BOOST}) tracks the input voltage shifted by V_{DD} . Ideally the gate to source voltage of transistor M10 should be equal to V_{DD} , making its ON resistance constant. The bottom and top plate parasitic capacitances (C_B , C_T) associated with the capacitor C_{BOOST} , gate capacitance C_g of M10 and overlap capacitance C_{gs} , C_{gd} makes the ON resistance of M10 input dependent. The boosted voltage (V_{BOOST}) at the gate of the transistor M10 is given by

$$V_{\text{BOOST}} = \frac{(C_T + C_{\text{BOOST}})}{C_{\text{TOT}}} V_{\text{DD}} - \frac{(C_T + C_g)}{C_{\text{TOT}}} V_{\text{IN}} - \frac{C_{\text{gs}}}{C_{\text{TOT}}} V_{\text{IN}} - \frac{C_{\text{gd}}}{C_{\text{TOT}}} V_{\text{OUT}}. \quad (7)$$

The parasitic capacitances C_B , C_T , C_g , C_{gs} , and C_{gd} [Fig. 6(b)] load the input, which in fact degrades the speed of the circuit. Bootstrapped switches used as feedback switches of the MDAC and input sampling switches of the second stage will load the amplifier and hence cannot be used everywhere in the switched capacitor circuits. In such cases FBB gives a clear advantage in terms of lower switch resistance variation and minimum loading due to low parasitic capacitances as compared to the bootstrap switches.

In addition, FBB saves significant amount of power wasted in clocking the switching controls of the pipelined stages and ASAR stage. FBB also significantly improves the speed of critical timing parts, dynamic latch and digital logic used to generate the internal clock for the ASAR. The delay of a minimum strength inverter, shown in Fig. 6(c), is improved by applying ± 1.8 -V FBB. It has shown 2x logic speed improvement as compared to the standard bulk CMOS process having the same feature size.

VI. BODY BIAS GENERATOR

The nMOS transistors are forward body biased at 1.8 V which is provided by the power supply. An integrated BBGEN

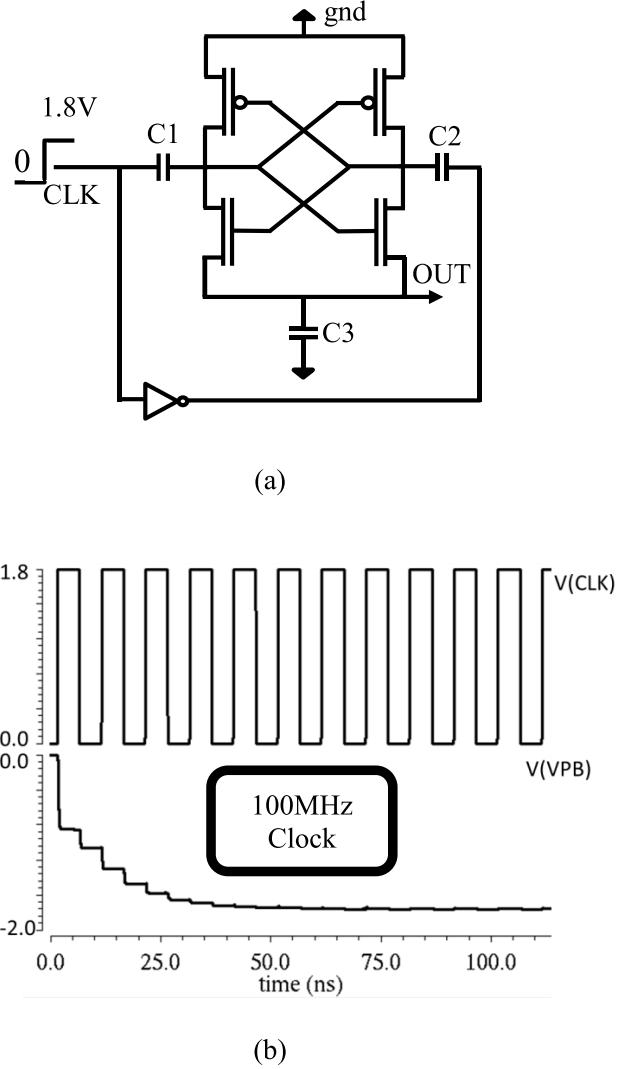


Fig. 7. (a) Charge-pump like BBGEN. (b) Charge pump clock and negative bias waveforms which is generated for pMOS.

is used to generate the negative voltage (-1.8 V) for pMOS. Since these voltages are connected to the bulk of the respective MOS transistors, almost zero static current is consumed through these voltages. An inverting charge pump like structure, as shown in Fig. 7(a), is used to generate -1.8 V and all the switching current is provided by the capacitor at the output of the charge pump. The BBGEN is designed using thick-oxide transistors in flipped well implementation. P-well and N-well of these transistors are both connected to ground, to avoid the forward biasing of well diodes. A 100-MHz clock shown in Fig. 7(b) is used to drive the charge-pump and almost no change is observed in the measurement results by varying the clock frequency from 10 to 200 MHz. The effect of transient disturbance, at the output of the BBGEN, is not seen in any of the measured results because these disturbances are very small. The fully differential structure of the ADC is also helping in canceling it by a great margin.

VII. TWO STAGE AMPLIFIER WITH PROPOSED CMFB CIRCUIT

Most of the high speed pipelined ADCs use single stage amplifiers [3] for high bandwidth and higher supply for more

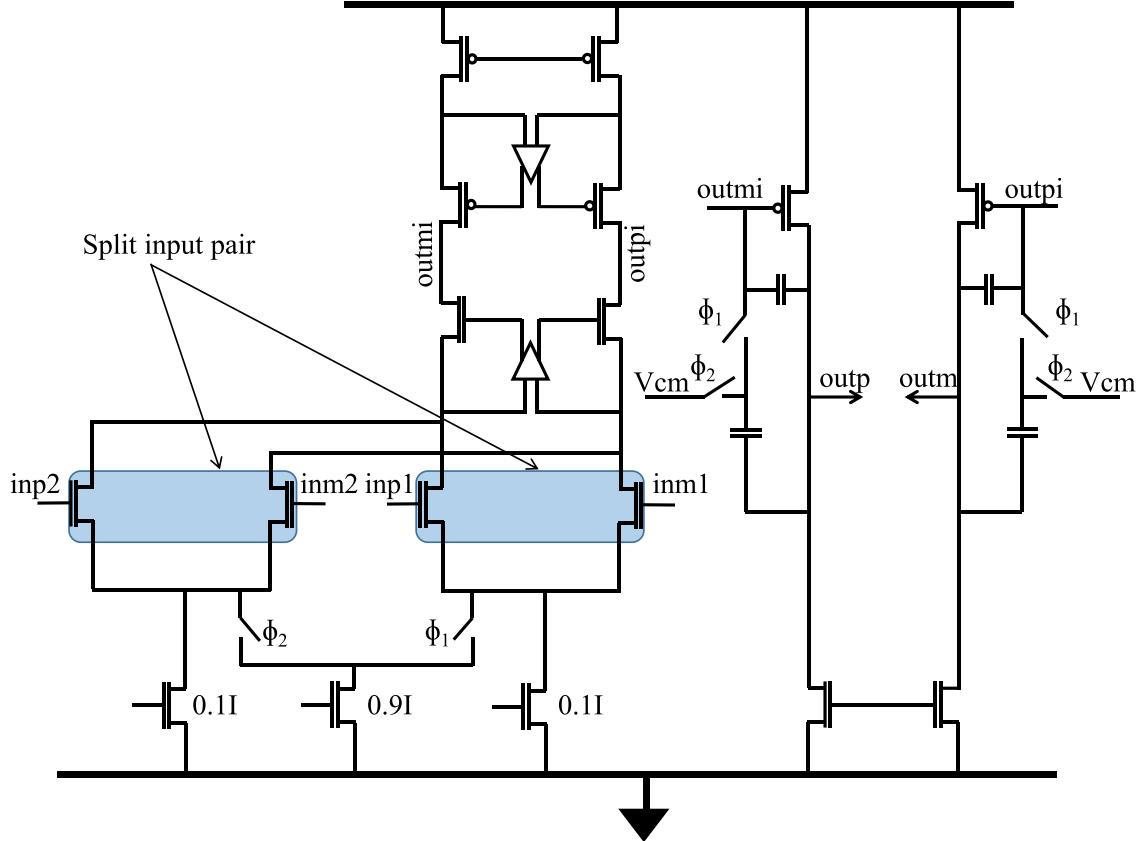


Fig. 8. Two-stage opamp with split input pair and Miller capacitors.

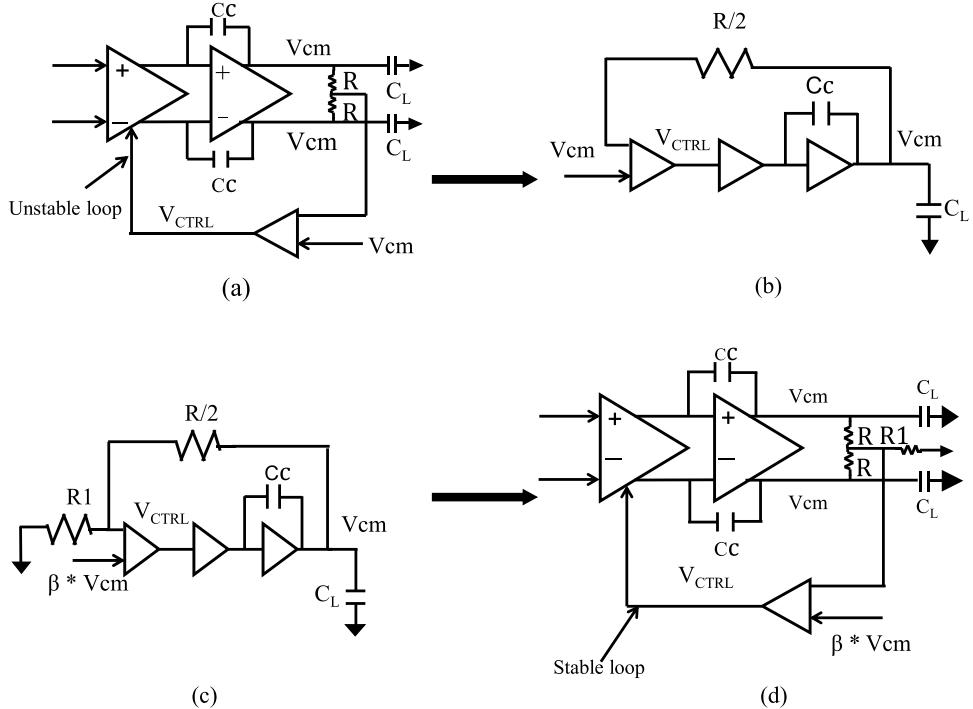


Fig. 9. (a) Two stage opamp with common-mode feedback circuit. (b) Common-mode equivalent circuit of two stage opamp. (c) Proposed common-mode equivalent circuit. (d) Two-stage opamp with proposed common-mode feedback circuit.

output swing, with the known disadvantage of closed loop bandwidth loss for low feedback factor (β) circuits. In case of 2.5-bit per stage, the inter-stage gain is 4 and β factor

is approximately 1/4. Loop gain stability, achieved at gain point (1/ β), results in larger phase margin at the cost of closed loop bandwidth ($\beta * f_u$). In a single stage amplifier the control

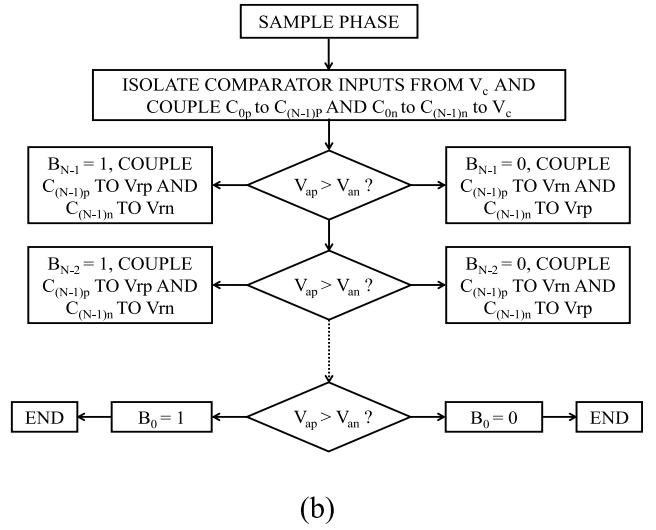
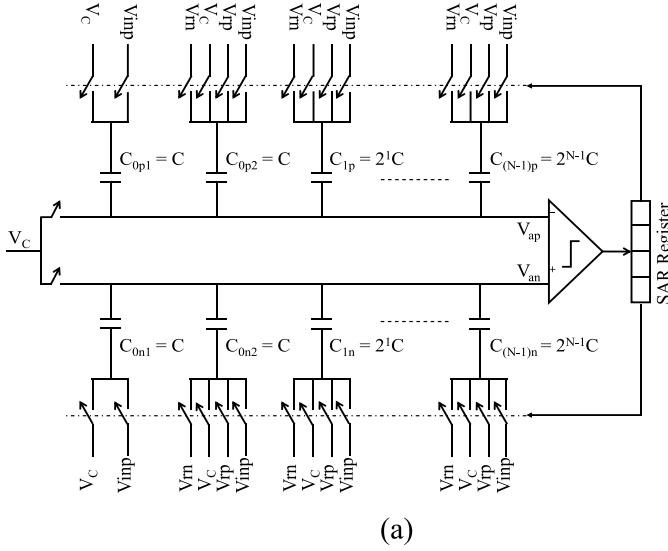


Fig. 10. (a) N-bit ASAR ADC, based on decide right switching scheme. (b) Flow diagram of decide right switching scheme.

on phase margin is limited, because the dominant pole is decided by the load capacitor which is fixed because of thermal noise and matching constraints. Two stage amplifiers have the flexibility of optimal placement of the load capacitor pole as non-dominant. This ADC uses a single two stage opamp, shown in Fig. 8, which is shared between both pipelined stages. The first stage of the amplifier is a gain-boosted telescopic structure and the second stage is a class-A structure. With this configuration, the phase margin can be traded off with bandwidth by moving the dominant pole from the first stage toward the non-dominant pole by reducing the Miller compensation capacitor. The two stage amplifier serves two purposes; more swing without the need of higher supply and higher closed loop bandwidth as compared to single stage amplifier for low β applications. The common-mode feedback loop becomes difficult to stabilize while increasing the differential bandwidth in the two stage amplifier by reducing the Miller compensation capacitor. Fig. 9(a) and (b) shows the block diagram of the two stage amplifier and its common-mode equivalent circuit. The common-mode feedback loop has marginality in stabilization due to the reduction of the Miller capacitor C_c . Traditionally, this common-mode loop can be stabilized either by feeding more power to the error amplifier or by using two common-mode feedback loops; one for each stage, increasing area and power. In this design, the three stage common-mode loop is stabilized by introducing a feedback factor (β), by adding a resistor $R1$ as shown in Fig. 9(c). Now, the reference point of the common-mode output voltage will change from V_{cm} to $(\beta * V_{cm})$, where β is given by the formula shown in

$$\beta = \frac{R1}{R1 + (R||R)}. \quad (8)$$

As shown in Fig. 9(d), the common-mode detector is having an extra resistor $R1$ with this scheme. By introducing the common-mode feedback factor (β), the common-mode loop becomes stable at a gain point ($1/\beta$). This gives extra phase

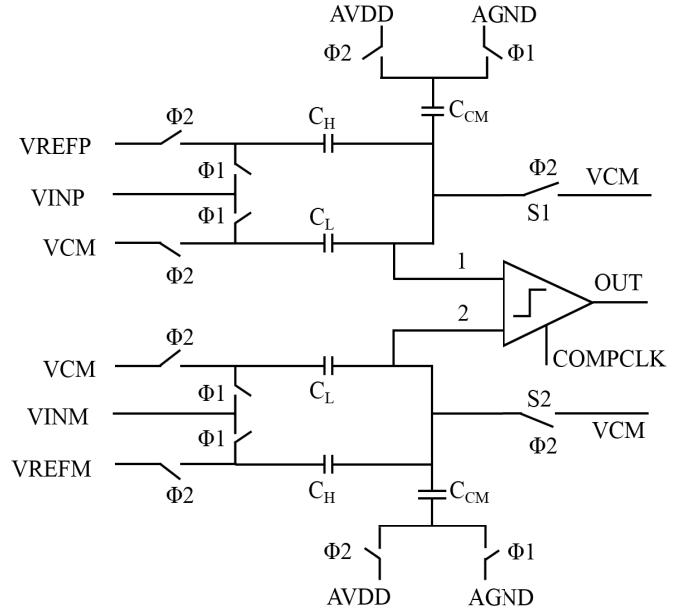


Fig. 11. Switched capacitor implementation of comparator of pipelined stage's sub ADC.

margin at the cost of common-mode loop bandwidth, which is not as stringent as differential bandwidth, provided differential matching is good. With this technique, the common-mode error is amplified by the factor $(1/\beta)$, which is easily tolerable in the design.

The opamp is shared between two pipelined stages with split input pairs as shown in Fig. 8, one for each pipelined stage, to improve the saturation recovery time. For a given out of range input, the opamp is saturated and it does not have the intended gain and closed loop bandwidth. If it is followed by an input signal, which is within allowed input range, the opamp tries to come out of saturation with the limited gain and closed loop bandwidth. Therefore, the ADC takes a lot of time (multiple clock cycles) to recover from saturation. Traditionally, the saturation recovery problem is

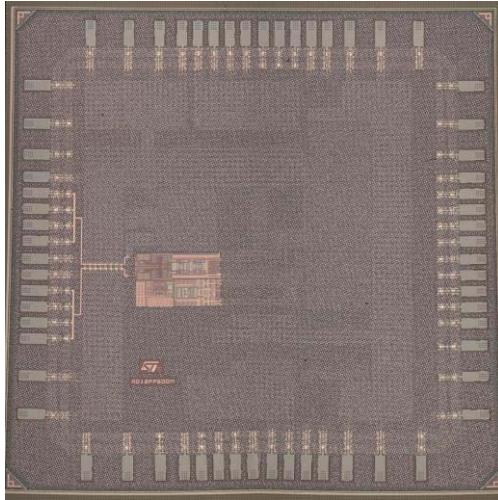


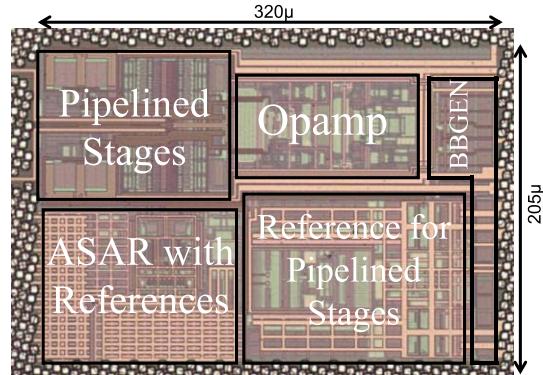
Fig. 12. Chip micrograph.

solved by not sharing the opamp. But this is a huge cost in terms of area and power. In this design, the saturation recovery time is improved by splitting the input pair of the opamp. When one input pair is in the feedback loop, the other input pair is connected to a common-mode voltage. Most of the current is steered to the input pair which is in the feedback loop and leaves a small amount of current to bias the other input pair. This technique saves a good amount of power while improving the saturation recovery time issue, caused by sharing the amplifier. The compensation capacitor (C_c) is also split between clock phases Φ_1 and Φ_2 to optimize the phase margin and closed loop bandwidth.

VIII. 8-BIT ASYNCHRONOUS SAR

The last stage consists of an 8-bit asynchronous SAR, which eliminates the high frequency clock requirement and saves system power. The split reference scheme requires matching between both references. The static mismatch between these references is discussed in Section IV and is taken care of with proper design. The top plate sampling introduces a large amount of gain error. Therefore, it is not suitable for the split reference technique. To avoid any further mismatch between split references, bottom-plate sampling technique is used in this design. All DAC capacitors are binary weighted, with the smallest capacitor designed to be 250 aF.

Switching transients on the ASAR reference can also produce mismatch spurs. Many energy efficient switching schemes are present in [26] and [27]. Fig. 10(a) shows the circuit diagram of the N-bit ASAR ADC. This design is using the decide-right switching scheme [20] based on an intermediate voltage (V_c), high reference voltage (V_{rp}), and low reference voltage (V_m). Fig. 10(b) is the flow diagram, showing the steps to perform analog-to-digital conversion according to this scheme. This scheme uses an extra intermediate voltage V_c , which makes switching operation symmetrical and draws the same current from the references, independent of the decision. The accuracy of this intermediate voltage is not as important as the other two reference voltages, V_{rp} and V_m . The decide-right DAC switching saves decoupling capacitor area of the



ASAR reference by a significant reduction in the needed reference current as compared to the classical, set and correct, switching scheme based on two reference voltages (V_{rp} , V_m). In general, the ASAR takes advantage of duty cycle to get more conversion time, but this design uses 50% duty cycle clock to allow for optimum settling time in the pipelined stages and conversion time in the ASAR stage. FBB of ± 1.8 V enables an 8-bit conversion of ASAR in less than 700 ps.

IX. IMMUNITY TO FBB ARTIFACTS (LEAKAGE AND RELIABILITY)

UTBB FD-SOI significantly reduces transistor variability and improves its electrostatic behavior, which governs the I_{ON} and I_{OFF} currents. This leads to a significant improvement of the sub-threshold slope and drain-induced barrier lowering (DIBL) [28], [29]. Further reducing the threshold voltage of transistors with the help of FBB improves the speed but increases drain to source leakage too. Two blocks of this ADC have high sensitivity to transistors leakage. These are shown in Figs. 10(a) and 11. The switched capacitor implementation of one of the six comparators of the sub-ADC used in the pipelined stages is shown in Fig. 11. Terminals 1 and 2 of Fig. 11 are floating in one of the clock phases and can leak their charge through the V_{cm} switches S1 and S2. Therefore, these switches are not using FBB and the PWELL of pMOS and NWELL of nMOS are both connected to ground potential, minimizing the leakage effect. This is also proven by the experimental results, where the ADC achieves around 64.5-dB SNDR at a very low sampling frequency of 10 MHz. The ADC is also working in simulations across PVT at 10 MHz, proving the immunity to leakage.

The terminals V_{ap} and V_{an} , shown in Fig. 10(a), are also floating in the conversion phase. But the conversion of the bits is done asynchronously with the decision of the dynamic latch [30]. Therefore, the conversion of the bits of the ASAR does not depend on the frequency of the clock. In this ADC, conversion of the ASAR stage is given half clock period and the remaining half clock period is used to sample the signal onto the sampling capacitor of the ASAR stage.

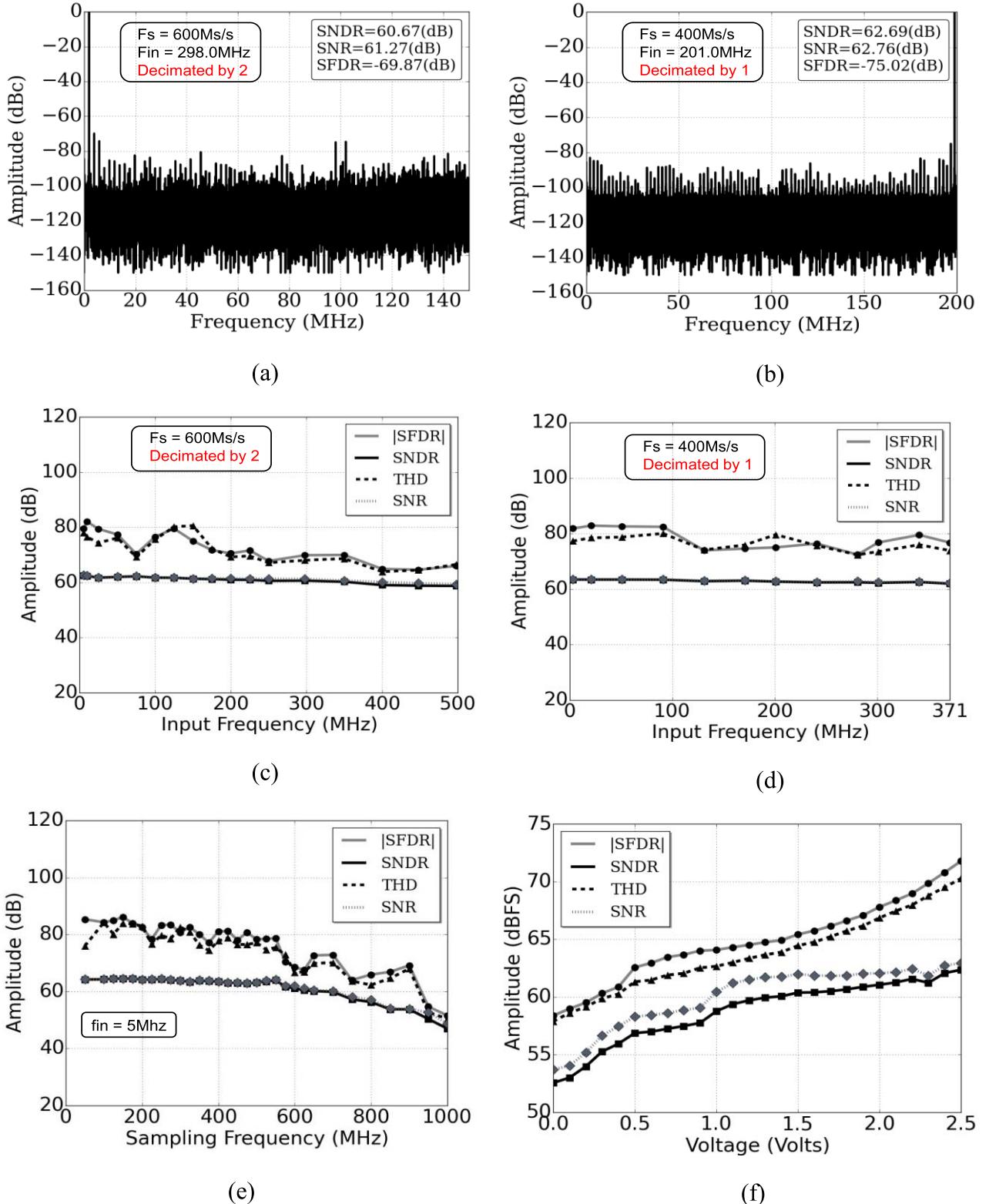


Fig. 13. (a) ADC output spectrum at $F_s = 600\text{ MS/s}$ and $F_{in} = 298\text{ MHz}$. (b) ADC output spectrum at $F_s = 400\text{ MS/s}$ and $F_{in} = 201\text{ MHz}$. (c) ADC performances at 600 MS/s with input frequency. (d) ADC performances at 400 MS/s with input frequency. (e) ADC performances at $F_{in} = 5\text{ MHz}$ with sampling frequency. (f) ADC performances at $F_s = 600\text{ MS/s}$ and $F_{in} = 5\text{ MHz}$ with FBB voltage.

The ASAR stage generates its 8-bits in approximately 700 ps, which means that ASAR stage is running at around 10 GHz in the conversion phase of the clock. A single conversion takes less than 100 ps. The conversion time of the ASAR stage for 8-bits will remain same even at lower frequencies.

Therefore, the leakage at these terminals has no effect on the operation and performance of the ASAR stage.

The FD-SOI technology is enabling the flexibility to incorporate transistors with FBB and without FBB in the design. This flexibility, together with few architectural choices which

	[2] [Chiang] JSSC 2014	[3] [Boo] ISSCC 2015	[9] [Brandolini] ISSCC 2015	[10] [Venca] ISSCC 2016	[32] [Mulder] ISSCC 2015	This Work
Technology	65nm CMOS	65nm CMOS	28nm CMOS	28nm CMOS	28nm CMOS	28nm FD-SOI
Power Supply [V]	1.0	1.2	1.0	1.2/1.5	1.0/1.8	1.1
Area [mm²]	0.18	0.59	0.22*	0.076	0.13	0.065
Resolution	10b	12b	10b	12b	13b	12b
Sampling rate (MS/s)	800	250	2.5K*/5K	600	800	600
SNDR@Nyq [dB]	52.2	65.7	52.2	58	57.2	60.7
Power [mW]	19	49.7	150	26.5**	76.4**	19.8
FoMw [fJ/conv-step]	71.4	126.2	95.8	68**	162.4**	37.2
FoMs [dB]	155.4	159.7	154.2	158.5**	154.2**	162.5
Calibration	yes	no	yes	yes	yes	no
Interleaving	no	no	yes	yes	yes	no

Fig. 14. Performance summary (*area and speed of single ADC, **PGA power and area included).

are inherently leakage free (e.g., DAC of the asynchronous SAR working at very high frequency), enables the wide frequency range of operation for this hybrid ADC.

The FD-SOI technology proves also to be an attractive and reliable solution for high speed and low power designs. Reliability of FD-SOI technology at various back bias voltages is compared with that of bulk technology in [31]. Various tests show that FBB does not impact the reliability of the transistors.

X. MEASUREMENT RESULTS

This ADC is implemented in 28-nm UTBB FD-SOI using ten metal layers. It occupies an area of 0.065 mm² including voltage references, core ADC and BBGEN. The chip micrograph of the ADC is presented in Fig. 12, showing most of the ADC blocks. It operates at 1.1-V supply consuming 19.8 mW at 600 MS/s. Voltage references and core ADC are consuming 6 and 12 mA, respectively. BBGEN is working at 1.8-V supply and consumes around 300- μ A current. This ADC achieves 1.6-Vp-p input swing from 1.1-V supply. Measurement results are presented in Fig. 13, showing the output spectrums, sampling frequency, input frequency, and BBGEN voltage sweeps. The SNDR is 61.5 and 60.7 dB at input frequency of 5 and 298 MHz, respectively, at 600 MS/s. This paper is also achieving 58.5-dB SNDR at 500-MHz input frequency at 600 MS/s. It achieves Walden and Schreier FoM of 37.2 fJ/conv-step and 162.5 dB, respectively, at 298-MHz input frequency running at 600 MS/s.

Almost 10-dB SNDR improvement is seen by varying the supply of the BBGEN from 0 to 1.8 V. This ADC also achieves 57-dB SNDR at 800 Ms/s and more than 50-dB SNDR till 950 MS/s. The performance of this work is summarized in

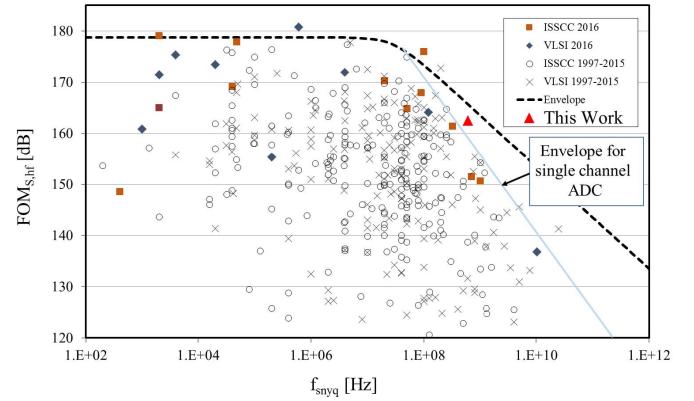


Fig. 15. Nyquist Schreier FoM versus Nyquist sampling frequency for single-channel ADCs published at ISSCC and VLSI between 1997 and 2016 [33].

a table shown in Fig. 14 and compared to other ADCs of similar performance. It is also evident from Fig. 15 that according to the Schreier FoM, this work is showing best-in-class performance as a single-channel ADC in its frequency range.

XI. CONCLUSION

This paper demonstrates a single-channel 12-bit 600-MS/s calibration free ADC in 28-nm UTBB FD-SOI technology that achieves 60.7-dB SNDR till Nyquist frequency. It also achieves \sim 59 dB SNDR till 500-MHz input frequency. The split reference architecture enables this performance in a very low area of 0.065 mm², which is a significant advantage in terms of cost when multiple ADCs are needed. Performance gain in the switched-capacitor analog circuits is demonstrated with the change in FBB voltage. The pipelined/Asynchronous

SAR architecture of this ADC takes full advantage of digital as well as analog circuit improvements enabled by FBB, avoiding any of the usual interleaving artifacts and also removing any kind of calibration making this work very efficient and robust.

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