A Mostly Digital VCO-Based CT-SDM With Third-Order Noise Shaping

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***Abstract*— This paper presents the architectural concept and implementation of a mostly digital voltage-controlled oscillator-analog-to-digital converter (VCO-ADC) with third-order quantization noise shaping. The system is based on the combination of a VCO and a digital counter. It is shown how this combination can function as a continuous-time integrator to form a high-order continuous-time sigma–delta modulator (CT-SDM). The counter consists only of digital building blocks, and the VCOs are implemented using ring oscillators, which are also digital-friendly. No traditional analog blocks, such as opamps, OTAs, or comparators, are used. As a proof of concept, we have implemented a third-order VCO-based CT-SDM for a 10-MHz bandwidth in the low-power version of a 65-nm CMOS technology. This prototype shows a measured performance of 71/66.2/62.5-dB DR/SNR/SNDR at a 10-MHz bandwidth while consuming 1.8 mW from a 1.0-V analog and 1.9 mW from a 1.2-V digital supply. With digital calibration, the nonlinearity could be pushed below the noise level, leading to an improved peak SNDR of 66 dB.**

***Index Terms*— Analog-to-digital converter (ADC), low-voltage design, quantization noise shaping, ring oscillator, sigma–delta modulator, time-domain signal processing, voltage-controlled oscillator (VCO).**

I. Introduction

TRADITIONALLY high-performance analog-to-digital converters (ADCs) have heavily relied on conventional analog building blocks, such as operational amplifiers, transconductors, and comparators [1]–[7]. Unfortunately, in today's ultradeep submicrometer technologies, these building blocks become increasingly difficult to design because of limited voltage headroom due to the low supply voltage combined with reduced raw "analog" performance of the elementary transistors (e.g., gain, matching, and $1/f$ noise) [8]. Moreover, these analog circuits have poor portability to other technology nodes, and efficient testing is a specialty in itself [9].

For this reason, researchers have attempted to find more "digital" solutions for these traditional analog blocks. A promising approach here is the voltage-controlled oscillator (VCO)-based ADCs [10]–[21]. If the VCO core is a ring oscillator, this corresponds to a "nearly digital" implementation. Such a VCO-ADC was shown to exhibit first-order quantization noise shaping and to have very similar behavior as a first-order $\Sigma\Delta$ modulator [14]. However, in the vast majority of the VCO-ADC designs that have been published, the VCO is still combined with sophisticated analog building blocks (i.e., opamps, transconductors, and so on) [10]–[13]. The reason for this is twofold. First, most VCO-ADCs suffer from nonlinearity problems, because the linearity of the voltage to frequency conversion of most VCOs is very poor. This problem can be tackled by combining the VCO-ADC with established analog techniques such as feedback. However, there are also digital-friendly solutions such as digital (self)-calibration [18]–[23]. And of course, the simplest solution would be to start from a VCO-ADC that has sufficient linearity. This was explored in [24], where a ring-oscillator VCO circuit with enhanced linearity was proposed. Compared with prior ring-oscillator VCOs, this circuit achieves greatly improved linearity, but unfortunately, even with this improved circuit, the linearity is limited to around 10.5 bits. Since this paper does not focus on enhancing the linearity, this VCO circuit is still used in this paper and as a result, the linearity of our proposed ADC is limited to around 10.5 bits. However, the techniques that we will propose in the following can be combined with other (proven) linearization techniques, such as the ones of [17]–[23], and hence this paper is orthogonal to this other work.

The second reason why most VCO-ADCs are combined with analog techniques is that, to the best of our knowledge, all publications of implemented mostly digital VCO-ADC prototypes only exhibit first-order quantization noise shaping [18]–[23]. This paper deals with this aspect and presents the design of—and measurements on—a "mostly digital" VCO-ADC with third-order quantization noise shaping. The core idea is inspired on related theoretical concepts that have been proposed in [25] and were developed independently in [26].

The rest of this paper is organized as follows: Section II introduces the system level concepts that are at the basis of our high-order noise-shaping VCO-ADC. Section III describes several simplifications to the overall system and how these simplifications enable a very efficient implementation. Section IV describes the VCOs in more detail. Section V presents the measured results on our implemented prototype, and Section VI concludes this paper.

II. System Level Concepts

A. First-Order VCO-Based ADC

It is well known how a VCO can be used to implement an ADC with first-order quantization noise shaping. A conceptual

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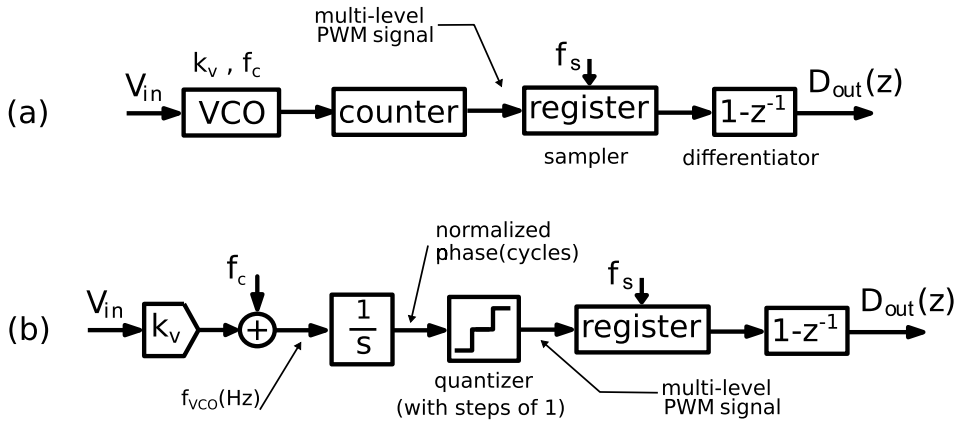

Fig. 1. (a) Conceptual realization of a VCO-ADC with first-order quantization noise shaping, and (b) its equivalent model.

realization is shown in Fig. 1(a). Here, the VCO converts the input voltage, V_{in}, to a square wave of which the instantaneous frequency is a linear function of the input voltage. Then the counter counts the number of rising edges, and its output is sampled and differentiated to obtain the digital output signal D_{out}.

An equivalent model is shown in Fig. 1(b) [27]. Here, the integrator models the conversion from frequency to phase. The quantizer represents the fact that we do not have full access to the output phase of the VCO, but only to its (rising) edges. Due to this, the counter output will only increment when the phase increase corresponds to one full VCO cycle. In other words, the up/down counter is acting as a continuous-time phase quantizer. Note that we will normalize the phase such that a clock cycle corresponds to a unity phase increase (in order to avoid factors 2π). After sampling, the output is differentiated in the digital domain.

The combination of the quantizer and the sampler introduces a loss of information, which is commonly modeled as an additive *quantization error* Q. By inspection, it is clear that the contribution of this *quantization error* will be differentiated in the output signal, and hence such a VCO-ADC provides first-order quantization noise shaping.

A key element to this paper has to do with the counter output signal of Fig. 1(a), which is an integer, and hence is inherently quantized. Nevertheless, this signal is not quantized in time and hence needs to be considered as a continuous-time signal. This is explicitated in Fig. 1(b), where the counter output signal corresponds to the continuous-time quantizer output signal. In a way, such a signal can be thought of as a multi-level pulsewidth-modulated (PWM) signal.

In spite of the quantization of the signal level, for a wide class[1] of input signals, this quantized counter output signal has the property that it still contains most of the signal information. This property can be understood intuitively from the observation that the information is stored in the position of the edges. The property was proven rigorously for the case of an input sine wave in [28] and for a more general class of bandwidth limited signals in [29]. In particular, for our case of an oversampling converter, extensive simulations confirmed that the property was valid for signals in the signal band. In this case, the signal prior to quantization can be reconstructed by low-pass filtering the quantized signal, and the quantized signal consists of a useful low-frequency component and high-frequency modulation spurs (which are at integer multiples of the VCO frequency) [28].

Note that the conceptual realization of Fig. 1(a) has the problem that the output of the counter is not bounded. Therefore, an actual realization will typically be based on a reset counter, which is shown in Fig. 3(b), and which has a strictly equivalent input/output behavior.

B. VCO-Based Integrator and DAC for the CT-SDM Application

If we want to extend the noise-shaping order of VCO-ADCs, clearly the open-loop concept of Fig. 1 is not sufficient anymore and we need to think of a way to incorporate feedback from the overall discrete-time digital output signal $D_{\text{out}}(z)$, where the dependence on z is added to emphasize its discrete-time nature. In this context, the structure of Fig. 2(a) was studied in [25]. In addition to the normal continuous-time analog input, V_{in}, there is now also a discrete-time digital input, which will be driven by the overall ADC's output signal D_{out}.

As in Fig. 1, the analog input voltage, V_{in}, is applied to a VCO_1 with a gain K_{v1} and a carrier frequency f_{c1}. However, the VCO now drives a more complex digital block: i.e., an "up–down counter." This up–down counter behaves differently on its positive (up) input (driven by the VCO) and negative (down) input (driven by the discrete-time digital signal D_{out}). It functions as follows: at every rising edge of the VCO, its output is incremented by 1, which is identical as the conventional counter of Fig. 1(a). Additionally, at every rising edge of the sampling clock, the counter output is decreased by the instantaneous value of the digital output D_{out} (which is a multi-bit integer).

[1]This property is not true for every input signal, e.g., consider a small input signal of which the integral satisfies the condition that it is zero at the VCO edges. Such an input signal will not affect the position of the VCO edges and hence cannot be recovered. However, such a signal is definitely not in the useful signal band of our modulator. A detailed study of the structure's rejection of such out-of-band signals is out of the scope of this paper.

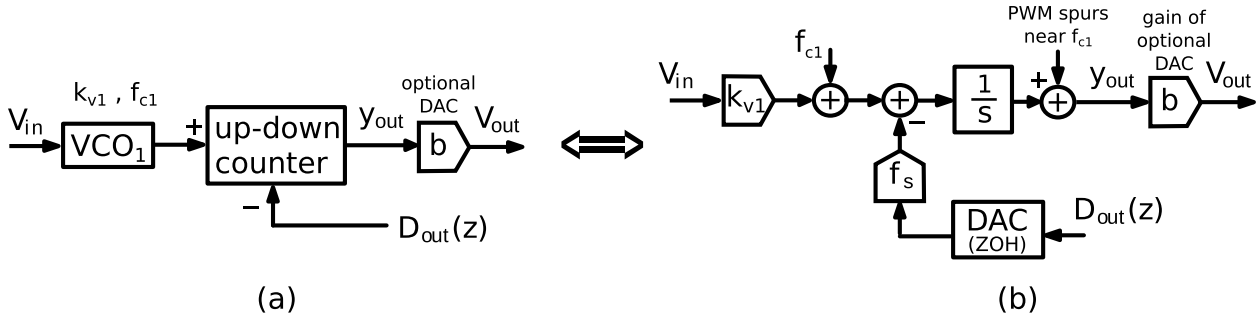

Fig. 2. (a) VCO-based input stage of a CT-SDM consisting of an integrator combined with the global feedback from the discrete-time digital output signal D_{out}) and (b) its equivalent system level model.

The output y_{out} of the up–down counter is a (multi-bit integer) digital signal. However, it does not only change at the clock edges: just as in the case of the counter output of Fig. 1, the information is encoded in the position of the edges and hence, it can also be viewed as a multi-level PWM signal [25]. If a true analog output is needed, a digital-to-analog converter (DAC) with a normalizing gain b can be added. We will see later on that this component can usually be merged into successive building blocks or even omitted. As such in practice, this DAC does not add to the complexity of this solution.

The proposed digital block of Fig. 2(a) implements the feedback DAC operation needed in a continuous-time sigma–delta modulator (CT-SDM) as well as the corresponding integration. Its equivalent model is shown in Fig. 2(b). As explained previously, the output of this stage is provided as a multi-level PWM. Due to this, there are high-frequency PWM modulation-spurs at its output. Also, there is a fixed input-referred contribution from the VCO carrier frequency. Clearly, the fact that there are high-frequency modulation spurs is a disadvantage. Nevertheless, since we want to use this block in a CT-SDM, we can expect that this will not be a severe problem, because these high-frequency spurs normally will be rejected by the inherent anti-aliasing filtering of the CT-SDM [30]. However, in a final design, it must be confirmed by system level simulations that this rejection is sufficient. It is obvious that the implementation of the integrator and DAC shown in Fig. 2(a) is much more digital-friendly than conventional analog integrator and DAC designs based on opamps, especially if the optional DAC block can be omitted. This integrator is a core ingredient of the high-order noise-shaping ADC in this paper.

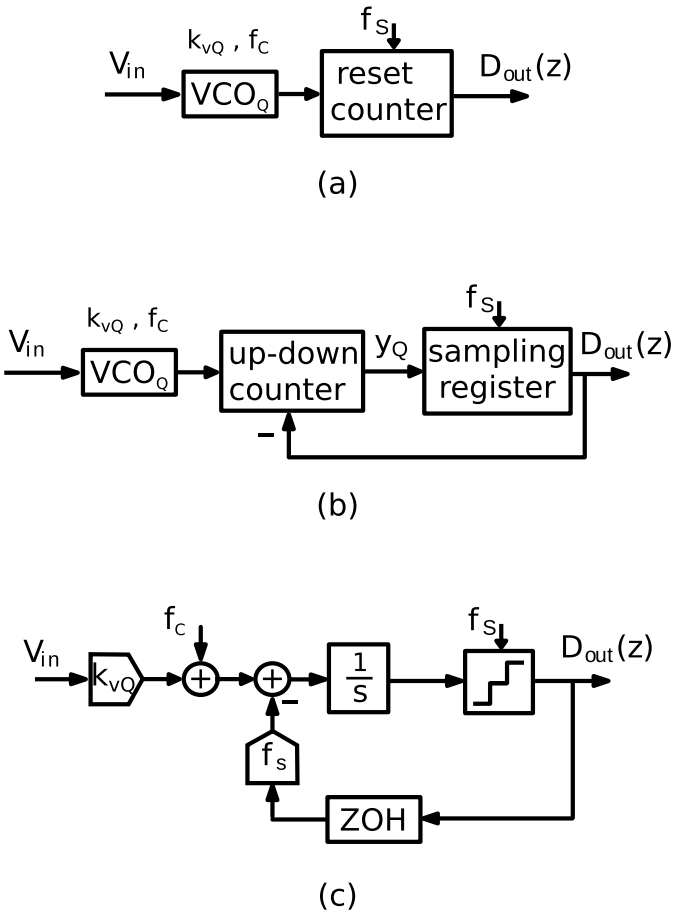

Fig. 3. (a) First-order noise-shaping quantizer consisting of a VCO and a reset counter. (b) Alternative implementation with the same behavior. (c) Equivalent continuous-time model.

C. VCO-Based Sampling Quantizer

A second core building block in a noise-shaping ADC is a sampling quantizer. For this, the conceptual structure of Fig. 3(a) has widely been used [31]–[33]. This structure performs the sampling and the quantization and, in addition, provides a first-order noise shaping of the quantization noise. This way, this structure can be used inside a $\Sigma\Delta$ loop and also as a stand-alone first-order VCO-ADC. An alternative implementation that is closer to the implementation of Fig. 2 is proposed in Fig. 3(b). It consists of an up–down counter (as the integrator of Fig. 2) and a sampling register, which samples at the sampling frequency f_s. The main advantage of this alternative implementation is that the input signal of the quantizer y_Q is now available. It will be shown in the following that this signal can be used to provide local feedback in an all-VCO CT-SDM.

By observing that sampling the multi-level PWM signal at the counter output corresponds to a (time-domain) quantization of the integrator output, we can obtain the equivalent model of Fig. 3(c). Here the quantizer's quantization step is equal

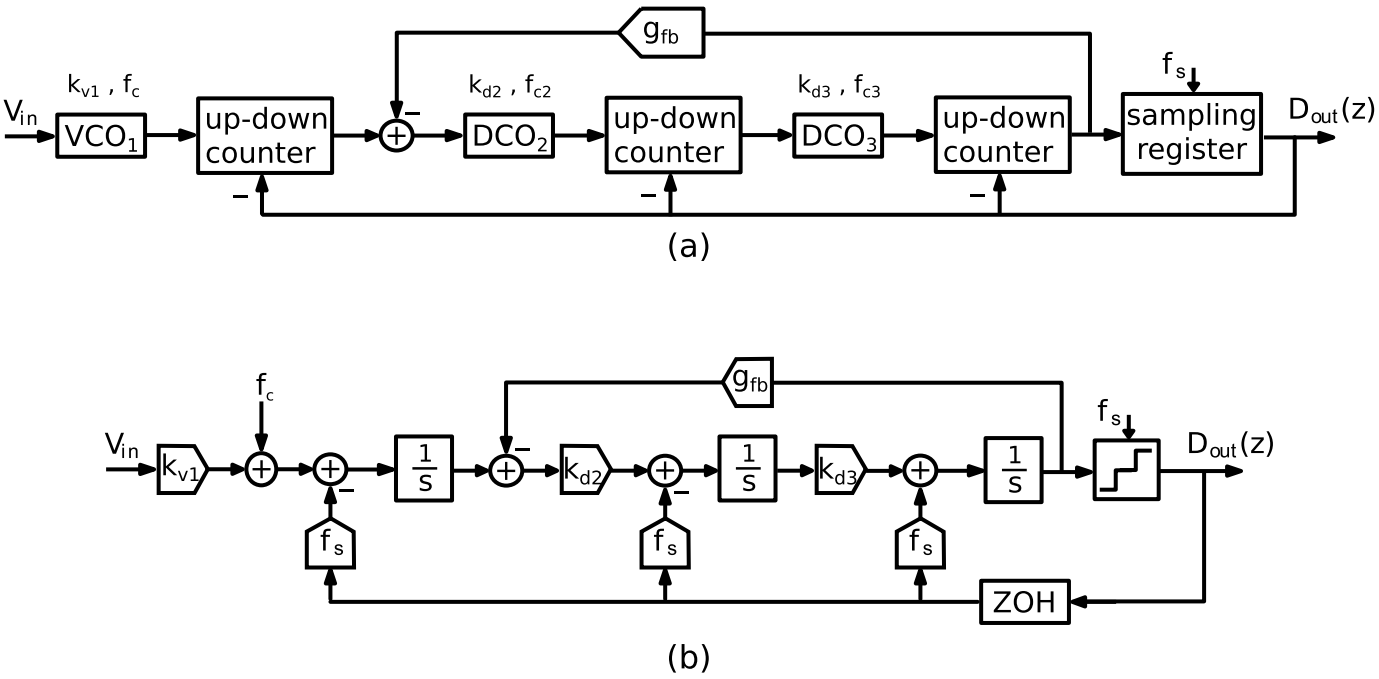

Fig. 4. (a) Proposed architecture of a third-order all-VCO CT-SDM and (b) its equivalent CT-SDM.

to the counter step, which is 1 in this diagram, where the instantaneous counter output is an integer. This block diagram illustrates the equivalence between a VCO quantizer and a first-order $\Sigma\Delta$ modulator, which was also established in several prior works [14].

D. General All-VCO CT-SDM Architecture

Based on our VCO-based integrator and quantizer, we can now develop a VCO-ADC with noise shaping of arbitrary order. As an example of the proposed scheme, a third-order all-VCO CT-SDM is shown in Fig. 4(a). As Fig. 4(a) shows, the (continuous time) digital output signals of the up–down counters directly drive the succeeding block without the optional DAC of Fig. 2. Due to this, the second and third controlled oscillators do not have a voltage mode input and, hence, are not VCOs. Instead they have an (integer) digital input, and hence are digitally controlled oscillators (DCOs). Therefore, the gains of these two DCOs, k_{d1} and k_{d2}, have the dimension *Hz per digit* (or simply Hz) and the output frequency of DCO_3 equals: $f_{DCO3} = f_{c3} + d \cdot k_{d3}$, where d stands for the digital input signal of the DCO, which is also the output signal of the second up–down counter.

We will show, in the following, that in our design, the implementation of these DCOs is not more complex than the implementation of a conventional voltage input VCO. The optional coefficient g_{fb} is a small (dimensionless) number, and can be added to optimize the position of the NTF zeros [30].

By using the equivalence setup in Figs. 2 and 3, an equivalent CT-SDM of the proposed system can be obtained, which is shown in Fig. 4(b). The carrier frequency of the first VCO appears on the equivalent system in Fig. 4(b) as a dc bias added to the input branch.

The carrier frequencies of DCO_2 and DCO_3 do not contribute to the output signal of the modulator, because, when referred to the input, they become zero. Therefore, the adding branches that should represent them are not shown in Fig. 4(b). In order not to overload Fig. 4(b), the extra branches corresponding to the PWM spurs, similar to the one in Fig. 2(b), are not shown either in Fig. 4(b). This is justified by the fact that a CT-SDM provides anti-aliasing filtering, which will suppress these PWM spurs to a large extent. The following sections III and IV, this is confirmed by system level simulations.

III. Simplified Implementation

Many circuit level implementations can be developed for the noise-shaping system shown in Fig. 4(a). In this section, we will impose several restrictions, which will enable a very efficient circuit implementation. In doing so, we sacrifice design freedom at the system level. In our implementation, one of the main parameters that we will put a limit on is the gain and carrier frequency of the oscillators. As will become clear later on, lowering the VCO gain will limit the quantization noise-shaping performance of the system, but as we will show, the resulting structure still has adequate performance.

A. Implementation for a Single-Phase VCO

As most VCO-ADCs, our design is based on a ring-oscillator VCO, which provides multiple phase-shifted versions of its output. We will also use these multiple output phases, but for easier understanding, we will first explain our implementation for the case of a VCO with only one output phase. To simplify the system, we first set the parameters f_{c2} and f_{c3} in Fig. 4(a) equal to zero. This will ensure that the output values of the first and second up–down

counter (which drive DCO_2 and DCO_3) are always positive integers. Assuming that k_{d2} and k_{d3} are also positive, this can be understood by observing that the output frequency of the DCOs can only assume positive values. Moreover, by inspection of Fig. 4, we can conclude that the output of the modulator, D_{out}, will be a digitized version of the first VCOs instantaneous frequency f_1 divided by f_s and hence cannot be negative. So, D_{out} and as a result also the output of the last up–down counter will also be nonnegative.

To further simplify the system, we will assume, for the moment, that f_c is much smaller than f_s. This will ensure that D_{out} (the digitized value of f_1/f_s) can only have the instantaneous values of 0 and 1. Moreover, under this assumption, also the first counter can only take the instantaneous values of 0 or 1. This can be understood from the following reasoning: let us assume that the loop starts in a "rest" state: i.e., the output $D_{\text{out}} = 0$ and also the counter values are 0. Now, every time VCO_1 generates a rising edge, the first up–down counter will go from 0 to 1. This creates a pulse in the loop, which will be processed, and after some time, create a "1" in D_{out}. This will reset the first up–down counter to "0." Since we have assumed that $f_s \gg f_1$, the loop's processing time is much smaller than the pulse duration of VCO_1. Hence, it is guaranteed that the counter will be reset before it could have been incremented from 1 to 2 by VCO_1. Due to this, the first counter can only take the values 0 or 1. Under these constraints (i.e., $f_s \gg f_c$ and $f_{c2} = f_{c3} = 0$), the up–down counter can be implemented as shown in Fig. 5(a). The corresponding timing diagram in Fig. 5(b) shows how it is triggered to be set and reset by the rising edges of the VCO and D_{out}, respectively.

The loop of the modulator will dictate DCO_2 and DCO_3 to have the same average frequency as VCO_1. Hence, if the global loop filter is not too aggressive (and hence the quantization noise in the loop is limited), the other counters in the loop will also only take the values 0 and 1. Thanks to this, in our circuit, the second counter can use the same structure as the first. The implementation for the third (last) up–down counter [see Fig. 4(a)] is slightly different, because it is implemented together with the sampling register. This circuit, shown in Fig. 6(a), consists of two parts: an up–down counter, and a DFF as the sampling register. The up–down counter is very similar to the one shown in Fig. 5(a) with the small difference that here one of the DFFs can be replaced by a D-latch. The timing diagram of this block is shown in Fig. 6(b).

The circuit of Fig. 6(a) has the same functionality as the reset counter commonly used in VCO-ADCs [14], but, for our purposes, this structure has two advantages over prior reset counters. First, it allows access to the last integrator's output signal, which can be used to optimize the NTF's zeros by incorporating "local feedback" in the modulators [30]. Second, unlike most prior implementations, this reset counter does not add loop-delay to the overall VCO-based CT-SDM.

B. Multi-Phase Implementation

In a ring-oscillator VCO with n elements, each element provides a phase-shifted version of the output signal. It is well known that if we use these multiple output phases (instead of only one VCO output signal), this effectively increases all VCO parameters by a factor n [14]. This idea can also be applied to the VCO and DCOs in our new high-order CT-SDM structure of Fig. 4(a). In the most general case of this structure, the VCO and the DCOs could each have different values for n, f_c, and k_v (or k_d). As a result, we obtain the "effective" values for the ith VCO (or DCO) as: $k_{\text{vi,eff}} = k_{\text{vi}} \cdot n_i$ and $f_{\text{ci,eff}} = f_{\text{ci}} \cdot n_i$. However, in order to simplify the implementation, we have set the number of phases in all the VCO/DCOs to the same value, n. With this simplification, the single-phase implementations (Figs. 5 and 6) can be extended toward a multi-phase implementation, by simply placing n single-phase blocks in parallel. The output of each counter is then provided in thermometer code at the n parallel outputs. The overall output signal D_{out} is a sampled version of the last counter output, and hence is also available in thermometer code to drive the "down" inputs of the counter blocks. The resulting circuit is shown in Fig. 7. Here the blocks RO1, RO2, and RO3 correspond to ring oscillators, which are discussed in more detail in the following. The first ring oscillator (RO1) is controlled through the resistive network $R_1 - R_2$ and operates as a VCO. The other ring oscillators (RO2 and R03) operate as DCOs and are controlled by arrays of n matched switched current sources. Each of these arrays is driven by n thermometer encoded digital signals.

To understand that these n parallel single-phase blocks indeed implement the correct up–down counter functionality, we can consider the first up–down counter block. Here, the n "up" inputs are driven by the n output phases of the first VCO, while the "down" inputs are driven by the (thermometer encoded) representation of D_{out}. Under the constraints described previously (i.e., the loop must be stable and $f_s \gg f_c$ and $f_{c2} = f_{c3} = 0$), again it can be understood that every block that will be set to 1 by a rising edge on the corresponding VCO phase will be reset to 0 shortly afterward by 1 on the corresponding D_{out} wire. This implies that each of the n parallel single-phase blocks can only take the output values 0 or 1. As a result, the overall counter output is also available as n thermometer encoded parallel bits. If the quantization noise in the loop is not too large, similar arguments can be made for the second counter and the third counter. Hence we can conclude that, with this condition, the counter will operate correctly and will not saturate.

The small *feedback switched current sources* are optional and can be used to obtain optimized NTF zeros. Fig. 7 clearly shows the power of this "digital" continuous-time sigma–delta modulation ADC: i.e., there are no conventional analog blocks and all the internal signals are digital. It should be noted that, except the sampled overall output signal D_{out} (which can only change at an edge of the sampling clock), all the signals in the structure are continuous-time signals (i.e., they can have transitions at any moment and not only on clock edges).

The behavior of the circuit of Fig. 7 with regard to thermal noise performance is very similar to a conventional CT-SDM: i.e., the overall thermal noise contribution of the first VCO will dominate, since the input referred noise contributions of

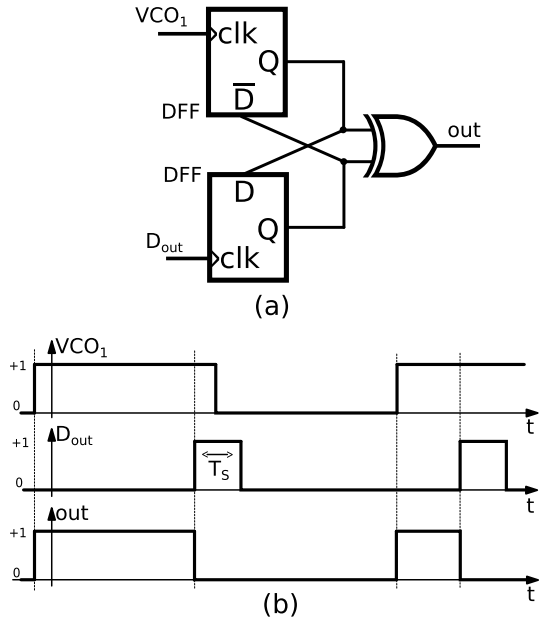

Fig. 5. (a) Proposed implementation of a single-phase up–down counter and (b) its timing diagram.

the second and third VCOs are shaped by the gain of the preceding integrators. Hence the first VCO should be sized for adequate noise performance. The noise level of this first VCO is determined by its impedance level, which for a given value of f_c is defined by the values of the input resistors R_1 and R_2, and can be approximated by $\alpha kT/(R_1 + R_2)$. Here α is a constant, which depends on the ring-oscillator design and which indicates the input referred noise contribution of the devices in the ring. This way, the value of the input resistor $R_{\text{in}} = R_1 + R_2$ should be scaled according to the allowable thermal noise level and W/L of the transistors in the ring should be scaled (inversely proportional to R_{in}) to restore the correct value of f_c.

C. Reduced Degree of Freedom System

In order to further simplify the design, all oscillators in the loop were sized to operate at the same oscillation frequency in the idle channel condition, f_c. For this, the current-sources driving RO2 and RO3 were sized such that for a mid-level input signal (i.e., $n/2$), the corresponding oscillation frequency was equal to the free running frequency of the first VCO (called simply f_c from now on). This implies that

$$k_{d1} = k_{d2} = k_d = \frac{f_c}{n/2}.$$

Taking into account that we are having an n phase design, this leads to the equivalent CT-SDM of Fig. 8, where the quantization step in the quantizer is 1.

Although the modulator of Fig. 8 has three poles in its NTF, there are only two design parameters (i.e., f_s and f_c) to set them. This means that we have lost the full control over the NTF. However, we will see that the system still has enough design freedom to size the loop for adequate quantization noise shaping.

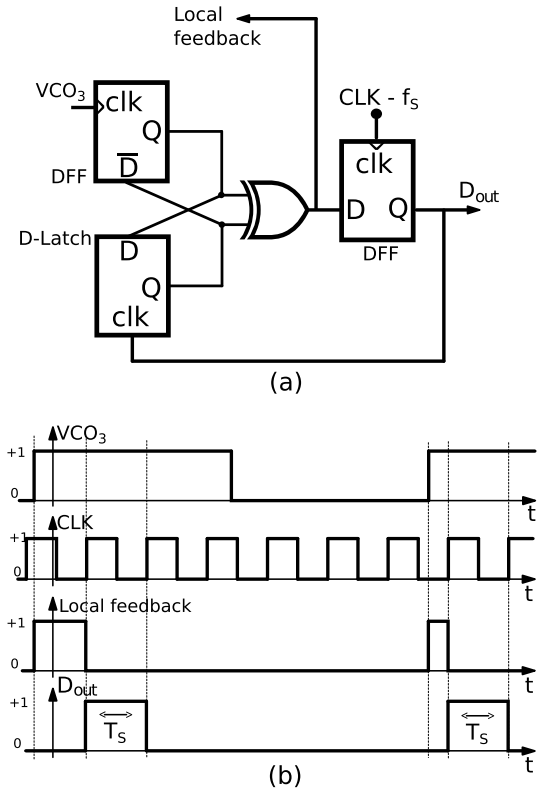

Fig. 6. (a) Proposed implementation of a reset counter and (b) its timing diagram.

The number of VCO phases n sets the ratio of the quantization step to the modulator's full scale range, which corresponds to the effective number of quantizer levels $N_{\text{lev}} = 2\ n(f_c/f_s)$ [14]. This way, there is a tradeoff with regard to this parameter: increasing n will improve the quantization noise performance; however, this will also increase the complexity of the associate digital circuits. While this tradeoff already existed as well in prior VCO-ADCs, most previous "digital" VCO-ADCs did not allow exploiting this degree of freedom. The reason for this is that the noise shaping in these prior designs was fixed to only first order. This way, the only way to improve the quantization noise performance was to increase n (the number of VCO phases), and designers tended to go for the maximum feasible value of n. However, with our high-order quantization noise-shaping structure, adequate quantization noise performance can also be achieved for a low value of n. In our design, we have exploited this freedom by choosing a very small value of $n = 9$. As will be demonstrated later, this leads to a circuit with a very small chip area.

A drawback of our simplified implementation is that it introduces a hard limit on the ratio f_c/f_s. To understand this, we should recall that the ideal up–down counter operation is that the counter output should be diminished by 1, if the value at the "down" input is equal to "1" on an edge of the clock (f_s). Now, the edge-triggered circuit of Fig. 5 realizes this behavior if there are never two consecutive "1" values on the "down" input, which is driven by D_{out}. However, if there are two consecutive "1" values in the corresponding phase of D_{out}, there will be only one edge, and hence the

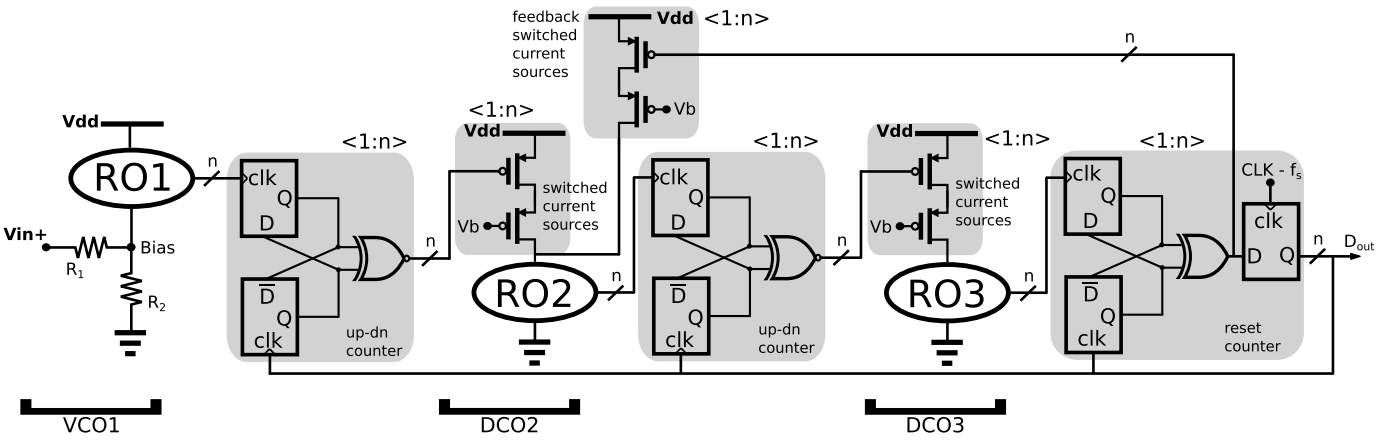

Fig. 7. Proposed implementation of a high-order VCO-ADC (with local feedback), where the digital signals are represented by n parallel thermometer encoded bits.

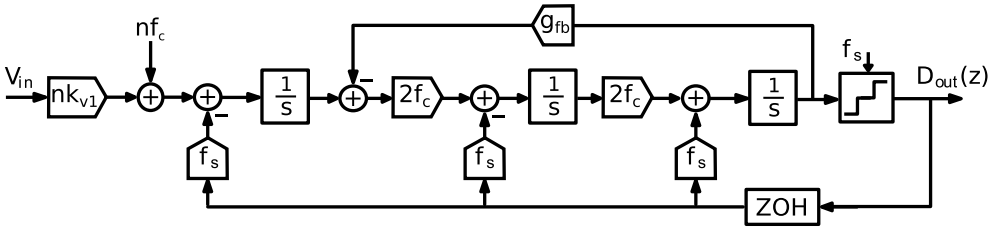

Fig. 8. Equivalent CT-SDM of our implemented VCO-ADC with reduced degree of freedom.

counter will count down only once instead of twice. This gives complete anomalous behavior and destroys the modulator operation. Now if we investigate the timing of the reset counter, we see that two consecutive '1's will occasionally occur when $f_{\mathrm{VCO3}} \geq f_s/2$. Since the oscillation frequency of VCO3 goes from 0 to $2f_c$, this leads to a hard limit for f_c:

$$f_c < 0.25 f_s. \tag{1}$$

Another important observation that can be made through inspection of Fig. 8 is that the integrator coefficients are essentially proportional to f_c/f_s. This introduces the well-known performance/stability tradeoff for the ratio f_c/f_s: for good quantization noise performance, this ratio should be large, while for robust stability, this ratio should be small [30]. In order to achieve good robustness, we worked with a ratio of around 1/6, which is tighter than the hard limit of (1).

In order to assess the noise-shaping capabilities as well as the equivalence between our new structure of Fig. 7 and the conventional modulator of Fig. 8, several behavioral simulations were performed. Typical results for the case of a 3-MHz sinusoidal input signal are shown in Fig. 9. Both the cases corresponding to the actual implementation according to Fig. 7 as well as the equivalent continuous-time system of Fig. 8 are shown. In the simulation, the local feedback coefficient g_{fb} was set to zero, $f_s = 1.6$ GHz and $f_c = 250$ MHz. We see that both systems indeed achieve third-order quantization noise shaping. For an OSR of 80, the newly proposed system achieves an SQNR of 88.5 dB, while the equivalent CT-SDM achieves an SQNR of 89.7dB. From this, we can conclude that with this sizing, none of the counters in our modulator overloads. Also, we see that both systems match quite well, which indicates that the differences between our newly proposed structure and the equivalent ideal continuous-time sigma–delta are small. Additionally, the simulation illustrates that the PWM spurs can indeed be neglected in this case.

IV. VCO and DCOs

As explained previously, the VCO and DCOs are based on a ring-oscillator core, which is shown in Fig. 10. It consists of n differential delay elements that are placed in a feedback loop. This oscillator core has two frequency control terminals ($Ctrl+$ and $Ctrl-$). It can be controlled from either or both these terminals. The differential delay element is shown in Fig. 11.

One of the main issues with the proposed system in Fig. 4 is the fact that the linearity of the system is limited by that of the first VCO. In the past, several solutions for this were proposed: calibration [18]–[23], PWM pre-coding [34], and input swing reduction by adding a coarse first stage [17]. All these techniques could be combined with the concepts described in this paper. However, in our proof-of-concept implementation, we retained the very simple concept of [24] for the first VCO. Here the ring-oscillator core is controlled through a resistive network consisting of R_1–R_2 at the $Ctrl-$ terminal (shown in Fig. 7). It was shown that this circuit can provide over 11-bit linearity for differential input signals up to 450 mVpp if it is used in a pseudo-differential configuration. For this reason, we have also used a pseudo-differential configuration, and the final implementation of the

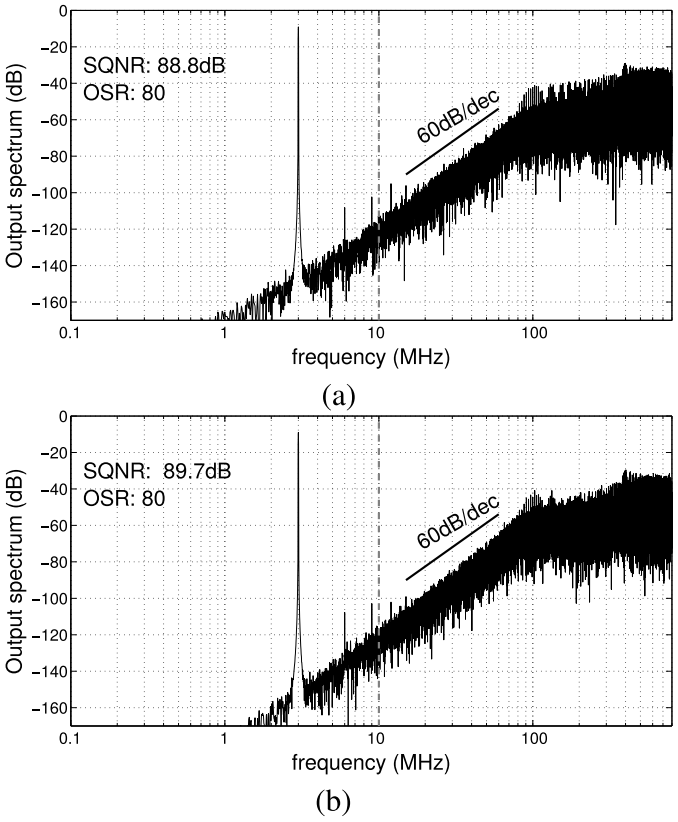

Fig. 9. Output spectrum (160K pt FFT) of a behavioral simulation result for the case $f_s = 1.6$ GHz, $f_c = 250$ MHz, and n = 9. (a) Actual structure of Fig. 7. (b) Equivalent continuous-time model of Fig. 8.

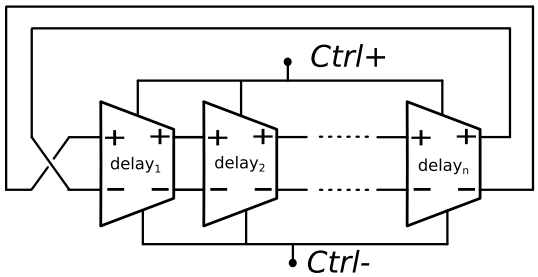

Fig. 10. Ring-oscillator core.

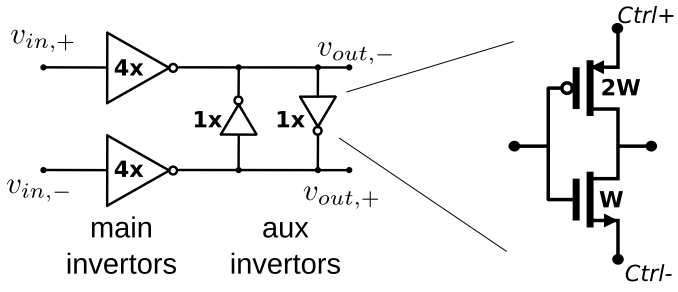

Fig. 11. Differential delay element used in the Ring-oscillator core.

overall ADC consists of two independent parallel channels processing the two differential inputs, $V_{\text{in}+}$ and $V_{\text{in}-}$. The resistors R_1–R_2 were sized 770 Ω. The delay cells were sized such that they provide the correct delay to obtain the desired oscillation frequency range. Since the delay in this circuit is essentially set by the cell's input capacitance, this can simply be done by appropriately setting the transistor dimensions [24].

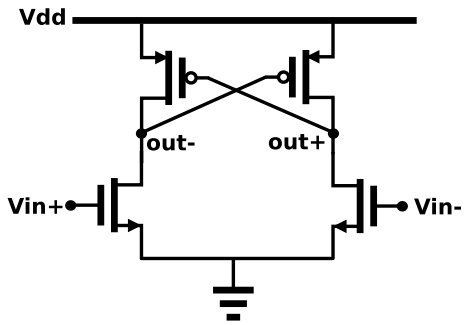

Fig. 12. Level shifter for RO2 and RO3.

The DCOs (DCO_2 and DCO_3) are controlled by current control through their top control terminal $Ctrl+$ (see Fig. 7). The linearity of this control strategy is not as good as that of the resistive input circuit, but the nonlinearity error is suppressed by the gain of the preceding integrator. The thermometer-encoded output of the previous stages directly drives an array of nominally matched unit current sources. Since the voltage across a properly designed ring oscillator does not vary much [24], the current sources do not need to have a very high output impedance, and a simple structure without cascodes can be used (see Fig. 7). Note that any mismatch between the n switched current sources that drive the ROs, RO1 and RO2, is alleviated by the inherent data weighted averaging in the system.

Our ring-oscillator implementation will be operated at a low voltage of 1 V. This introduces the problem that the delay elements in the ring (Fig. 11) have limited voltage headroom and their output swing is typically only around $V_{\text{dd}}/2$ (which is barely above the threshold voltage in our technology). This voltage swing is not enough to drive the following digital blocks. Therefore, a level shifter is needed. The variant corresponding to RO2 and RO3 is shown in Fig. 12 (the one for RO1 is flipped). Unfortunately, this block has a severe tradeoff between its propagation delay and power consumption. In order to limit the power consumption, we had to allow a rather high propagation delay for the level shifter, which in worst case can be as high as 700 ps.

It is well known that delay in a CT-SDM affects its stability. However, the coefficients in our design are not very aggressive, such that even this large delay does not make the loop unstable or degrade the signal-to-noise ratio (SNR) performance. However, it clearly alters the out-of-band shape of the NTF. This is illustrated in the simulation result of Fig. 13, which apart from the delay is equivalent to Fig. 9(a). Note that if the VCO's have a finite bandwidth in their input to output frequency response, this will give a similar effect, but in our implementation, the finite VCO bandwidth effect is negligible relative to this delay effect.

V. Experimental Results

A pseudo-differential implementation consisting of two independent parallel channels of the circuit shown in Fig. 7

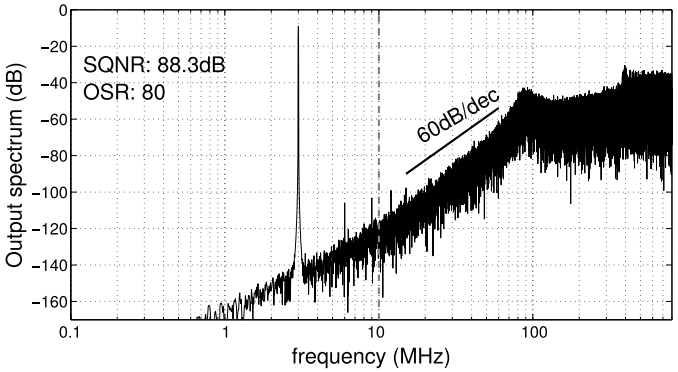

Fig. 13. Output spectrum (160 K pt FFT) of a behavioral simulation result for the case $f_s = 1.6$ GHz, $f_c = 250$ MHz, and n = 9, where a level shifter delay of 700 ps is inserted after each VCO.

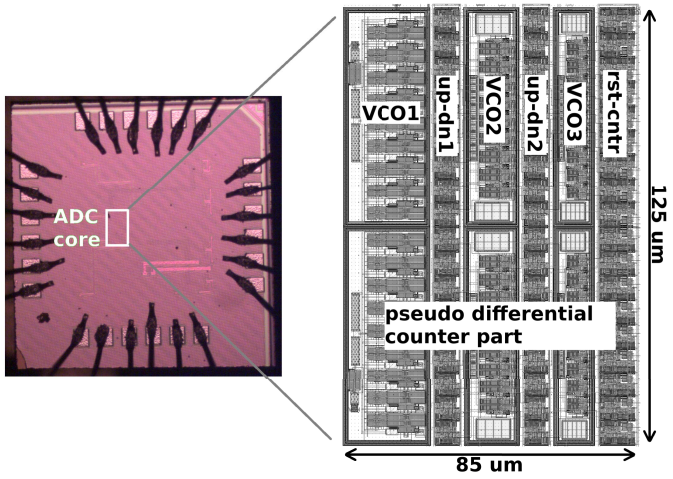

Fig. 14. Chip microscope photograph with annotated layout.

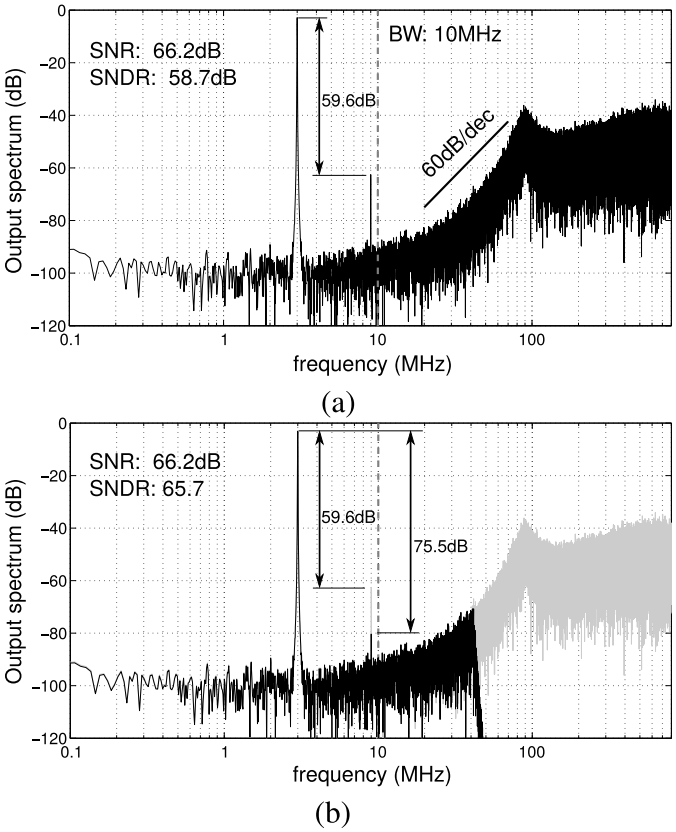

Fig. 15. Measured output spectrum (160K pt FFT) for the case of $f_c = 250$ MHz and $f_s = 1.6$ GHz with a 3-MHz input tone with an amplitude of a 650 mVpp differentially. (a) Normal (pseudo-differential) output and (b) partially decimated (pseudo-differential) output with off-line digital calibration overlayed on the raw output.

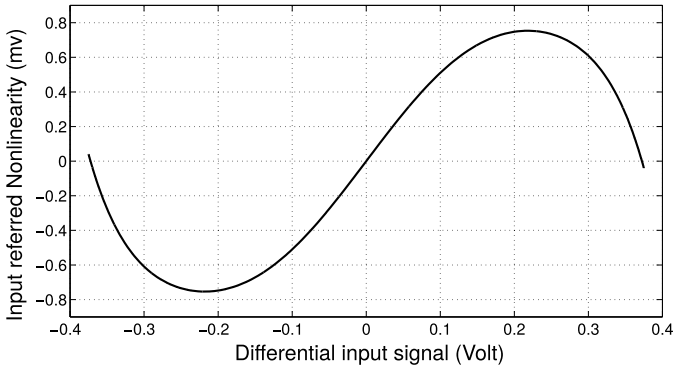

Fig. 16. Static nonlinearity plot of the ADC for the case of of $f_c = 250$ MHz and $f_s = 1.6$ GHz in the pseudo-differential configuration.

was prototyped in the low-power flavor of a 65-nm CMOS technology. The transistors in our circuits have a threshold voltage (V_{th}) around 400 mV.

In principle, the digital circuitry of our implementation (Fig. 7) could be designed through a standard digital flow. However, at the time of this design, we did not have access to digital libraries for our target technology and hence the digital cells were designed by hand. In this proof-of-concept circuit, not much effort was done to optimize these cells in terms of power, nor area. Due to this, more than half of our prototype's power is consumed in these circuits (more details on the power consumption follow), but this could be significantly reduced by an improved design. The digital blocks were designed for a 1.2-V supply (which is the technology's recommended supply voltage). In a mixed-signal design, the analog supply is typically the bottle-neck and it is normally equal to, or higher than, the digital supply. But in our design, the analog circuits (VCO, DCOs, level shifters, current sources, biasing, and so on) were designed for a supply voltage of only 1 V, which is enabled by the fact that there are no traditional (high-performance) analog components at all.

A photograph of the fabricated die and the annotated layout is shown in Fig. 14. We can clearly distinguish the two channels and how the area is distributed over the different blocks. The resulting circuit measures 85×125 μm^2 $= 0.01$ mm^2. This surprisingly small silicon area is thanks to the fact that the number of VCO phases was set as low as $n = 9$. This can be done in this architecture, where the performance is achieved through high-order noise shaping and not by using a large number of VCO phases.

The presented prototype was designed such that it can operate under different sampling rates with different coefficients in the integrating VCO's. Therefore, the local feedback path corresponding to the coefficient g_{fb} shown in Fig. 7

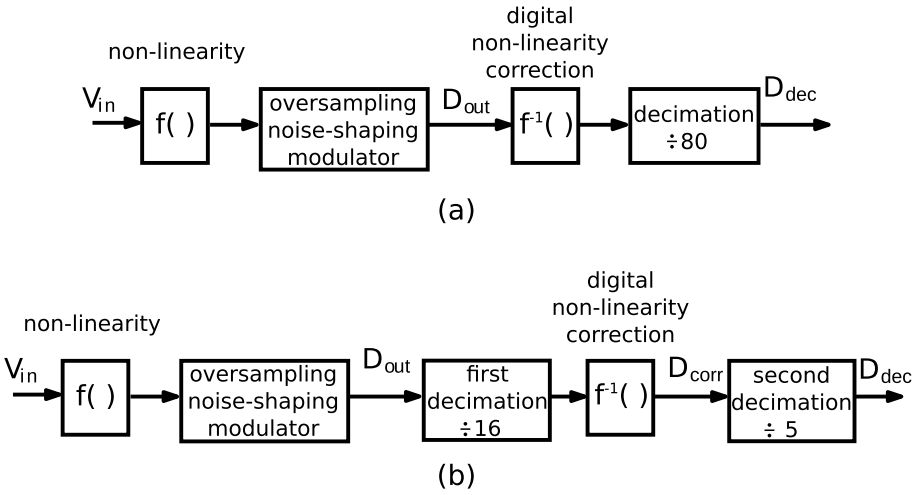

Fig. 17. Block diagram of an oversampling converter with off-line digital calibration. (a) Conventional setup of [18]. (b) Setup used in this paper.

was omitted to simplify the reconfigurability of this ADC. As explained in Section III-C, in our system (with reduced degree of freedom), the modulator coefficients are set by the oscillator central frequency f_c and the sampling frequency f_s. The central frequency in the DCOs (DCO_2 and DCO_3) can be reconfigured by adjusting the bias current in the bias network. To reconfigure the first VCO, a tuning current can be injected into its control terminal ($Ctrl-$). In our prototype, the same effect can also be achieved by adjusting the biasing common mode voltage at the overall ADC input.

In a first batch of measurements, the circuit was configured for a carrier frequency $f_c = 250$ MHz and a sampling frequency $f_s = 1.6$ GHz. The bandwidth was set to 10 MHz, corresponding to an OSR $= 80$. In this mode, the analog power consumption was 1.8 mW. The digital power consumption (flipflops, latches, and XOR gates) was slightly higher, i.e., 1.9 mW, but it is expected that this could be cut significantly through an optimized re-design.

An output spectrum for the case of a 3-MHz input tone with an amplitude of 650 mVpp differentially is shown in Fig. 15(a). This amplitude is deliberately chosen above the designed linear operating range of the VCO (which is 450 mVpp differentially), such that it creates large harmonics. The plot clearly exhibits the expected peaking in the noise transfer function, which is due to the large delay of the VCO read-out circuits (see Section IV). As expected for low frequencies, we can see a white noise floor. For this case, the SNR is 66 dB. Thanks to the pseudo-differential setup, where the outputs of both independent channels are subtracted from each other, there is no even order distortion, which confirms the effectiveness of this scheme and is consistent with the measurements of [24]. However, there is a large third harmonic, which limits the signal-to-noise + distortion ratio (SNDR) in this case to 59 dB. As explained previously, this large third harmonic is due to the limited linearity of the first VCO in the system. To assess this, the static nonlinearity of the overall ADC was measured, by sweeping the input signal and averaging the ADCs output over a long time. The result is shown in Fig. 16.

As mentioned previously, our new high-order noise-shaping technique can also be combined with digital calibration techniques, similar to [18]–[20]. Although not the focus of this paper, a first assessment of the effectiveness of an off-line calibration technique such as the one of [18] was also performed based on the measured nonlinearity data of Fig. 16. The core idea of such an off-line calibration technique is shown in Fig. 17. It is based on the observation that the nonlinearity of the VCO occurs at the input of the system (shown as the nonlinear function $f(\cdot)$ in Fig. 17). If the nonlinearity is known, it can be inverted at the digital output of the converter (shown as the nonlinear function $f^{-1}(\cdot)$ in Fig. 17). In the conventional scheme, shown in Fig. 17(a), the nonlinearity correction is performed directly on the raw undecimated modulator digital output signal D_{out}. However, in this paper, this conventional scheme was found to increase the baseband noise level significantly. The reason for this is that in our modulator, there is a large amount of shaped quantization noise, which after passing through the nonlinearity correction block is in part converted to white noise which in turn partially falls in the baseband. Therefore, the modified setup of Fig. 17(b) was used, where first the bulk of the shaped quantization noise is removed in a first coarse decimation step. Then on this relatively clean signal, the nonlinearity correction is applied, and then passed for further decimation. This modified setup with the nonlinearity correction at an intermediate decimation step is preferred over performing the nonlinearity correction on the overall decimated output D_{dec}, to avoid that the baseband signals would be partially filtered (phase shifted or slightly attenuated) prior to the nonlinearity correction. This scheme was implemented in software (off-chip) and the result is shown in Fig. 15(b). As Fig. 15(b) shows, the distortion is now reduced to a level where it does not affect the SNDR anymore, leading to an SNDR, which is virtually equal to the SNR. Since our implementation is in software off-chip, we did not study the power nor area for a full silicon realization. However, it was already shown in [18] that interpolating the correction terms from a tiny lookup-table of only 11 data points was sufficient in practice. Moreover, in our scheme where the

TABLE I
COMPARISON WITH RELATED WORK

	This work		[18]	[19]		[20]		[33]	[35]	[31]	[22]
Process	65nm LP		65nm	65nm G+		65nm LP		65nm	90nm	90nm	65nm
Area (mm^2)	**0.010**		0.020	0.075		0.070		0.150	0.170	0.120	0.026
Fs (MHz)	1600	1000	300	1600	2400	500	1152	250	480	300	205
Fc (MHz)	250	133	–	–	–	–	–	–	–	–	–
BW (MHz)	10	10	30	12.5	37.5	3.9	18	20	10	8.5	25.62
peak SNR (dB)	66.2	60.5	–	75	71	71.5	70	62	72.3	69.3	52.8
peak SNDR (dB)	62.5	55.1	–	74	70	71	67.3	60	70.3	67.2	50.3
peak $SNDR^*_L$	65.7	60	64								
DR (dB)	71	63	–	77	73	70	68	68	75	73	–
Supply (V), a/d	1/1.2	0.8/1.1	–	1	1.2	2.5/1.2	2.5/1.2	1.3/1.2	1.2	1.4/1.2	1.2
Power (mW), a+d	1.8+1.9	0.71+0.77	11.4	17.5	39	8	17	10.5	14.3	4.3	3.3
FOM^{**}_{SNDR} (dB)	157	153.5	–	162.5	160	158	157.5	153	158.5	160	149
$FOM^{*}_{SNDR,L}$	160	158.5	158								
FOM_{DR} (dB)	165.3	161.3	–	165.5	162.8	156.9	158.3	160.8	163.5	166	–

* $SNDR_L$ is the SNDR after calibration, which was done off-chip. Therefore its power and area is not included.
** FOM = (SNDR or DR) + $10\log(\mathrm{BW}/Power)$, [30]

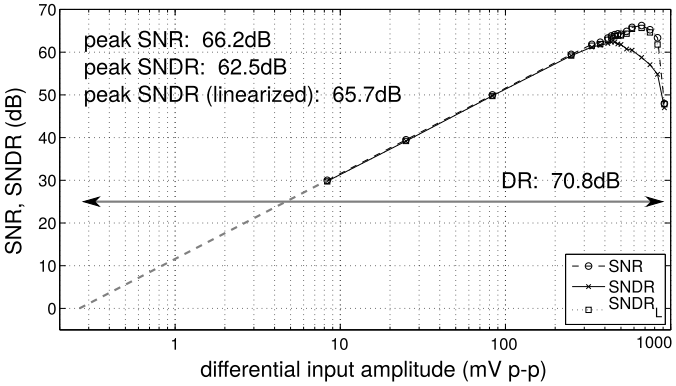

Fig. 18. Dynamic range plot for the case of $f_c = 250$ MHz, $f_s = 1.6$ GHz, and 10-MHz bandwidth.

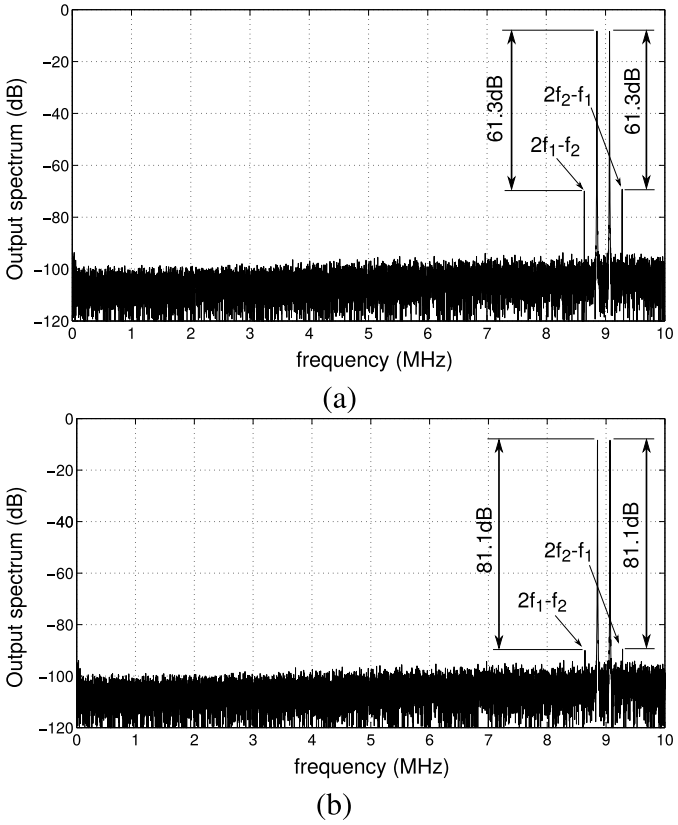

Fig. 19. Baseband FFT plot for the case of two-tone input signal of two tones near 9 MHz with the same peak-to-peak signal level as for the plot of Fig. 15 (650 mVpp differentially). (a) Normal (pseudo-differential) output and (b) (pseudo-differential) output with off-line digital calibration.

correction is performed at an intermediate decimation step, this correction can be performed at a relatively low speed. For this reason, we expect that the implementation overhead should be modest.

Experiments as described previously were repeated for varying input amplitudes. The results are shown in Fig. 18. For the implemented chip (which does not have the calibration on board), the SNDR starts to drop above a differential input amplitude of 450 mV_{pp}, which is consistent with the designed linear input range of the first VCO [24]. The corresponding peak SNDR equals 62.5 dB. The peak SNR is 66.2 dB and the dynamic range (DR) is 71 dB. The SNDR for the case of the off-line (and off-chip), digital calibration is plotted as well and it is nearly identical to the SNR, indicating that digital calibration works over the entire signal range. The corresponding peak SNDR for this case equals 65.7 dB.

To further asses the digital calibration scheme also, a two-tone test was performed where the input signal is the sum of two sine waves with the same amplitude and input frequencies near the band edge (here: 8.855 and 9.068 MHz). The result for the case of a signal level of 650 mVpp differentially (identical to the case shown in Fig. 15) is shown in Fig. 19, both for the case without and with the digital calibration. Clearly, also in this case, the calibration can significantly suppress the effect of the distortion.

A drawback of the described digital calibration scheme is that it has problems to deal with interferers that are above $f_s/32$ (50 MHz in our case), e.g., consider the case of an

interferer at 100 MHz and another one at 205 MHz. Due to the nonlinearity of the VCO, this will inject an intermodulation spur at 5 MHz, which is exactly in the intended signal band. However, in our digital correction scheme, all interferers above 50 MHz are removed before the correction and hence the corresponding intermodulation tones will not be corrected. Therefore, the digital scheme should not be used in the proposed form shown in Fig. 17(b) if large out-of-band interferers are expected.

As was explained previously, the proposed implementation can work under multiple sampling frequencies and can have multiple operation modes by adapting the VCO free running frequency values (and corresponding VCO gain values). To illustrate this, the same batch of experiments as described previously was repeated for the case where the sampling frequency was set to $f_s = 1$ GHz and the VCO central frequency f_c to 133 MHz. It was found that at this lower operating frequency, the circuit was still functional also at reduced supply voltages: i.e., 0.8-V analog and 1.1-V digital. In this configuration, the accuracy performance (SNR and SNDR) was decreased but also the power consumption was more than halved. The results for both cases as well as a comparison with other related works about digital-friendly ADCs are summarized in Table I. From Table I, we can see that our proof-of-concept circuit has a performance that is comparable to the state of the art, while it has a significantly reduced silicon area.

VI. Conclusion

We have demonstrated the first implementation of a mostly digital VCO-ADC with third-order quantization noise shaping. For this, we have derived the structure of Fig. 4(a) and proposed the efficient implementation of Fig. 7. The resulting circuit occupies a surprisingly small area of only 0.01 mm^2. This is an inherent advantage of our approach, because it achieves its performance thanks to the high-order noise shaping, and hence unlike most other designs does not require a high number of VCO phases with their associate read-out circuitry. Although our prototype was only a proof of concept where several potential optimizations and tweaks were not implemented, it exhibits an adequate performance with a peak SNDR of 62 dB and a dynamic range of 71 dB over a 10-MHz bandwidth at a power consumption of 3.7 mW. One potential improvement, i.e., the use of digital calibration, was already investigated and was shown to push the nonlinearity below the noise level, leading to an improved peak SNDR of 66 dB. Also, the digital circuits (e.g., the DFFs) were designed *ad hoc* in this proof-of-concept prototype and due to this, these circuits consume more than half of the overall power budget. By an optimized design, the associate power could be greatly reduced.

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