Current-Mode Full-Duplex Transceiver for Lossy On-Chip Global Interconnects

Nijwm Wary and Pradip Mandal

***Abstract*— This paper presents an energy efficient full-duplex (FD) current-mode transceiver for on-chip global interconnects. As it shares the same signaling port for transmitting and receiving signal, the wire efficiency is increased by 2× compared to unidirectional transceivers. The proposed hybrid transceiver has a directional inverter/buffer (DIB) circuit which inverts the outbound signal whereas conveys the incoming signal maintaining the same phase with a gain greater than one. As a result, the incoming signal is seamlessly separated from the strong outbound signal just by weighted addition of the two compound signals on the either sides of the DIB by a transconductor (gm) circuit. This is in contrast to existing subtraction based signal dissociation architecture. Importantly, the inbound signal retrieval process is a constructive one where the two components of the incoming signal are added up to provide inherent gain, making it suitable for lossy on-chip link. Moreover, the DIB circuit has very low active impedance at its input/output node and hence supports high bandwidth transmission without using any passive terminator. A prototype design has been implemented in 0.18-μm CMOS process for a global interconnect of 5 mm length. Measured results give an efficiency of 0.19 pJ/b/mm for an FD operation of 4.0 Gb/s.**

***Index Terms*— Bi-directional, current-mode, full-duplex transceiver (FDT), global interconnects, high speed, network-on-chip (NoC), on-chip interconnects, multi-chip modules (MCMs).**

I. Introduction

With the advancement in fabrication technology multiple digital cores are getting integrated on a single die, leading to multi-processor systems-on-chip (MPSoCs). Energy efficient data sharing among the cores through networks-on-chip (NoCs) are becoming popular in MPSoCs. The performance of NoC is highly dependent on the speed and power consumption of data transmission across the global interconnects. As the global interconnects are lossy links, it is a challenge to transmit high speed data efficiently across them. To have energy efficient data communication, full swing signaling across the long interconnects with repeaters is replaced by low swing signaling across repeaterless link. In recent times, several such low swing high speed signaling techniques have been proposed for serial communication across the lossy interconnect. Some of them are capacitively driven line [1]–[5], current-mode signaling [6]–[11], and resistive termination [12]–[15]. The popular techniques used to increase the performance of serial transceivers for off-chip link have also been deployed for on-chip interconnects. Some of them are cross-talk compensation and decision feedback equalization [16], feed forward equalization [6], continuous time linear equalization [17], loss-compensation by negative impedance converters [18], wire twisting [19], and modulation [20].

Besides the energy efficiency improvement, there are several attempts to decrease the link area of the NoC. For example in [1], 16 data streams are serialized into one data stream to reduce the link area. Similarly, two data streams are transmitted over a single wire using 4-level pulse-amplitude modulation (PAM4) communication [21]. For two-way data communication, two dedicated unidirectional links may be used as shown in Fig. 1(a). The other option is to use a half-duplex signaling scheme as shown in Fig. 1(b), where the same link can be time shared for data transmission in two directions. Use of a bi-directional link to support half-duplex signaling has better utilization of the link area [11], [22]–[24], however, at the cost of independency of data transmission in opposite directions. The link utilization may be doubled by using a full-duplex (FD) signaling scheme where the data flow can take place across the same link in both the direction simultaneously as illustrated in Fig. 1(c). Moreover, it helps to maintain independency of the data communication in opposite directions. However, FD signaling requires special hybrid transceivers at the two ends of the link to dissociate the "outbound" signal (transmitting signal) and the "inbound" signal (received signal). In this paper, we propose a current-mode transceiver for FD signaling across on-chip interconnect.

Similar to core-to-core communication within a die, for short distance die-to-die communication through silicon interposers [7], [25] in multi-chip modules (MCMs) reduction of the number of link lines is necessary as it helps to increase the level of integration. In these MCMs, the dies are flipped and are connected through silicon interposers and micro bumps. Since the number of bumps per unit area is limited, there is a trend to decrease the number of link line. For example, Dehlaghi and Carusone [25] have used single-ended communication to manage with less number of bumps in the system. Our proposed differential FD transceiver (FDT) may be directly used for such MCMs interconnects.

FDTs are recently being explored for on-chip interconnects [26], [27], however, they are more popular and have been extensively explored for off-chip PCB/cables [28]–[32]. But off-chip FDTs are power hungry and they cannot be directly deployed for on-chip interconnects as the power budget for on-chip link is much lower. Moreover, on-chip

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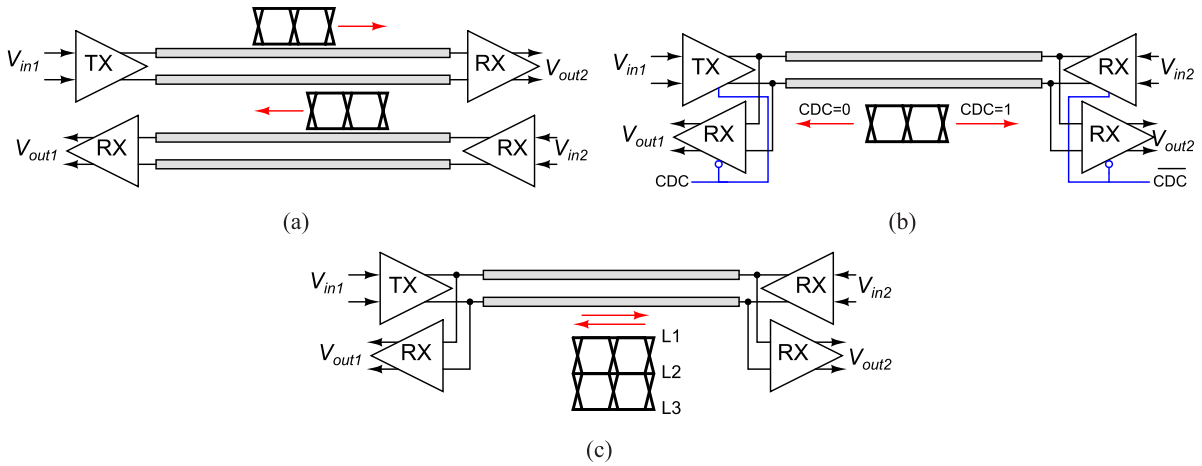


Fig. 1. Different signaling techniques. (a) Unidirectional. (b) Half-duplex. (c) FD.

link has different characteristic compared to that of off-chip interconnects and hence, require different techniques to make them energy efficient. Off-chip interconnects consist of high frequency loss whereas, for dc the loss is negligible. On the other hand, for on-chip interconnects both high frequency and dc loss are significant. For instance, the link resistance of the global interconnect (M5) is around 31 Ω/mm for a width of 2 μm in 0.18-μm technology. This is hundred times larger than the resistance of the typical off-chip links per cm [23]. Also, in current mode signaling, the on-chip interconnects are terminated at the receiving end with low impedance for high bandwidth of the link [6], [7], [11]. Hence, the signal has larger swing at the transmitting end of the interconnect and its swing reduces significantly by the time it reaches the other end of the interconnect. As a result, at the input/output node of a transceiver, the magnitude of the outbound signal is much larger than the inbound signal. Hence, for on-chip interconnect, the transceiver should have a high gain for the inbound signal and at the same time, it should also ensure high bandwidth and low power consumption to get good energy efficiency.

In this paper, a current-mode transceiver has been proposed for FD communication suitable for on-chip global interconnects. The proposed transceiver reduces the link area by 50% compared to the existing unidirectional schemes. To achieve FD communication, the separation of the inbound and the outbound signal in the transceiver is done by a directional inverter buffer circuit and an addition based transconductor circuit. The proposed circuit has higher inherent gain for the inbound signal compared to the existing subtraction based resistor transconductor (R-gm) hybrid transceiver architecture used for low loss off-chip link [28]. As a result, based on this implementation, the power efficiency of the transmitter and the receiver/transconductor of the proposed transceiver are, respectively, 1.3× and 12× higher compared to those of the R-gm hybrid. This makes the proposed transceiver suitable for lossy on-chip link. Moreover, because of having very low impedance at the input/output node of the proposed transceiver, it eliminates the requirement of passive terminator for achieving high bandwidth link.

Section II discusses about the existing FDTs and introduces the proposed FDT architecture. Section III discusses the circuit design of the proposed transceiver and its analysis. Section IV discusses the implementation and simulated performance. Section V presents measured results followed by the conclusion in Section VI.

II. Full-Duplex Signaling in Serial Link

In FD binary signaling, the associated transceiver should be able to work in FD mode and to do so, it should successfully separate the inbound signal from the outbound signal. The primary objective in design of an FDT is reducing the interference induced by the outbound signal into the received signal. The induced signal acts like a noise and degrades the quality of the received signal. The challenge in FDT design is making this noise much lower compared to the received signal in presence of process variations and device mismatches to achieve the target bit error rate (BER). Before introducing the proposed FDT and its advantages, let us discuss the existing FDT architectures.

A. Conventional Full-Duplex Transceivers

One of the architectures of FDT for off-chip interconnect is the replica driver hybrid as shown in Fig. 2(a) [29]–[32]. It consists of a main transmitter driver (TX), a replica driver, and a subtractor. In addition, the link is terminated by a resistor Z_o matching characteristic impedance of the link to avoid reflection (except in [32] where Z_o is active impedance). TX generates the outbound signal $V_{\rm ob}$ to be transmitted across the link which is terminated at the far end too. The voltage signal V_A at input/output node A contains both the outbound signal $V_{\rm ob}$ and inbound signal $V_{\rm ib}$ originated from the far end transceiver. In order to retrieve the inbound signal $V_{\rm ib}$ from V_A $(= V_{\rm ib} + V_{\rm ob})$, a replica signal $V_{\rm rep}$ of $V_{\rm ob}$ is generated by the replica driver and then it is subtracted from V_A. This operation can be mathematically written as

$$V_{\rm rx} = V_A - V_{\rm rep} = V_{\rm ib} + \Delta V_{\rm er} \tag{1}$$

where $\Delta V_{\rm er} = V_{\rm ob} - V_{\rm rep}$ is the error voltage due to mismatch between $V_{\rm rep}$ and $V_{\rm ob}$. In a good transceiver, $\Delta V_{\rm er} \ll V_{\rm ib}$.

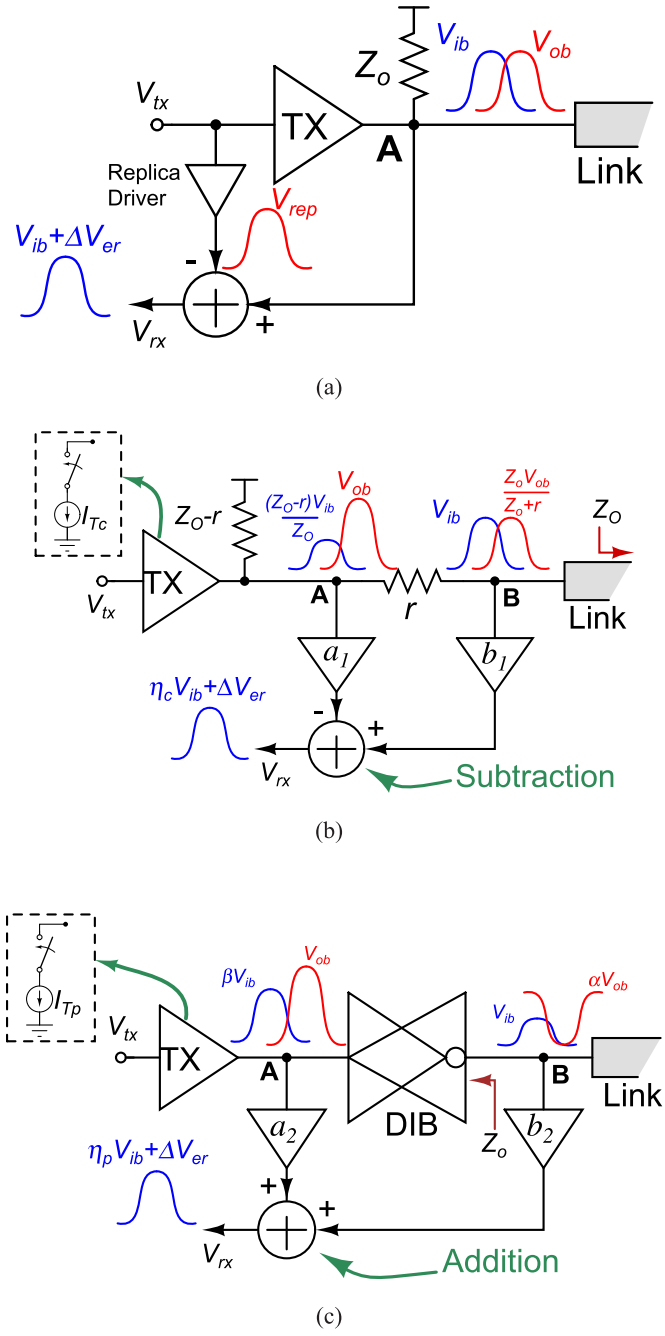


Fig. 2. FDTs. (a) Replica driver. (b) Resistor transconductor (R-gm hybrid) [28]. (c) Proposed technique (DIB-gm hybrid).

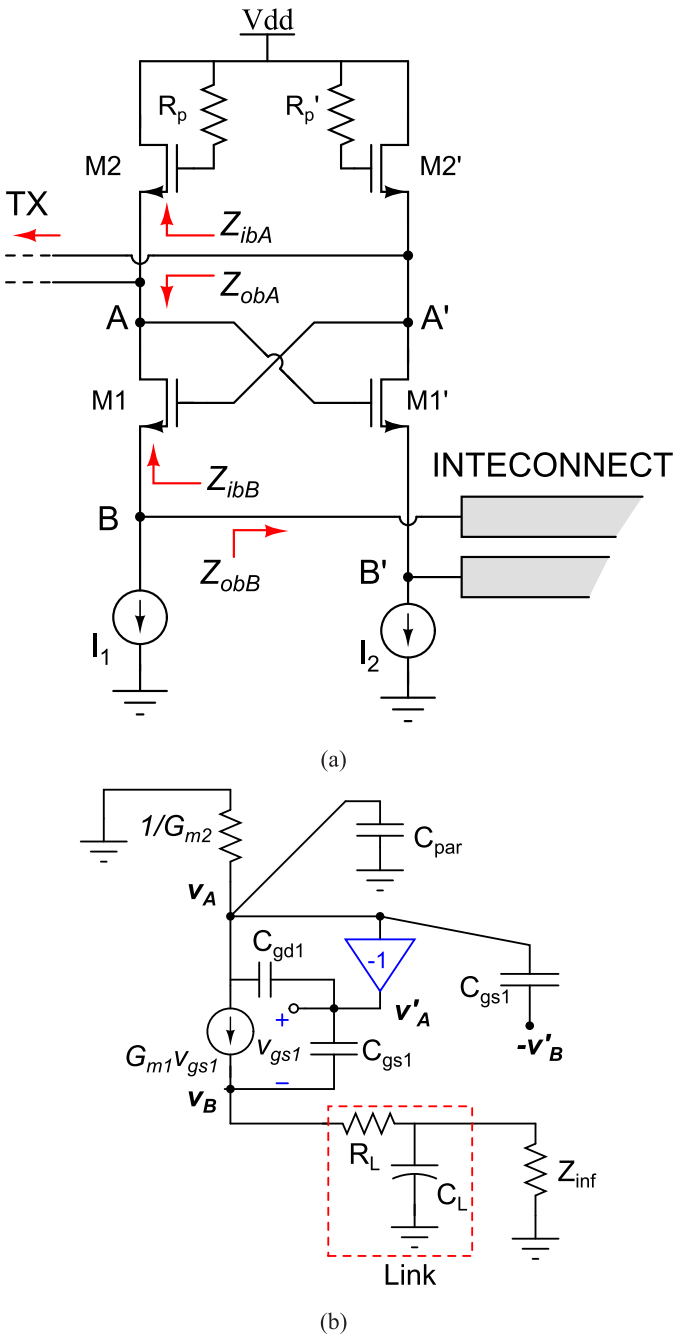
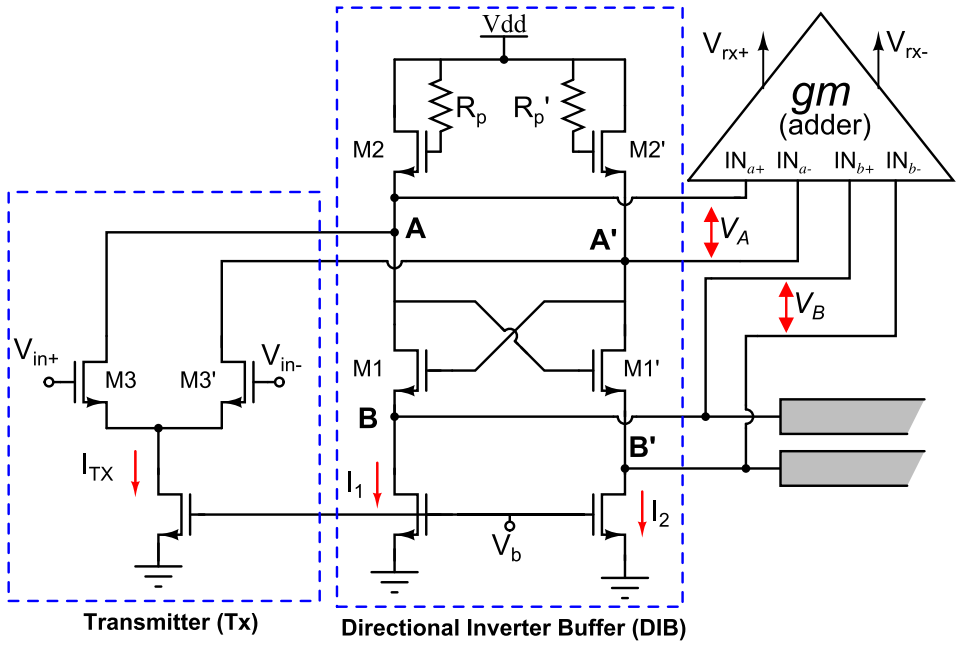


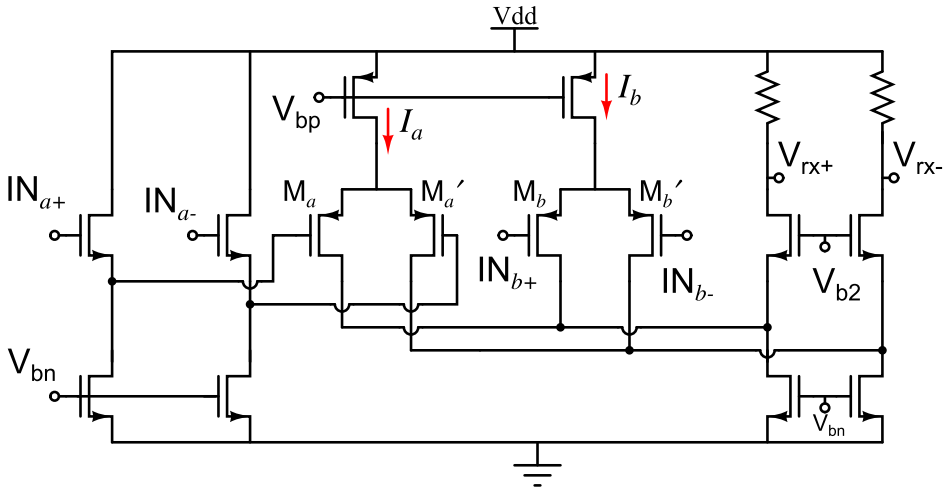
Fig. 3. DIB. (a) Circuit diagram. (b) High frequency small signal equivalent circuit.

In this architecture, the primary sources of $\Delta V_{\rm er}$ are the mismatch of gains between the TX and the replica driver, and the timing mismatch between $V_{\rm rep}$ and $V_{\rm ob}$ at the input of the subtractor.

An alternate architecture of FDT for off-chip link is shown in Fig. 2(b). This architecture has a lower $\Delta V_{\rm er}$ than that of the replica driver hybrid called the R-gm hybrid [28]. In this transceiver, the terminator Z_o is split into two parts, namely, r and $Z_o - r$. The current mode transmitter (TX) generates the outbound signal $V_{\rm ob}$ which propagates through resistor r. So, the amplitude of the outbound signal at the two ends of the resistor r (i.e., node A and node B) are different. The outbound signal $V_{\rm ob}$ at node A is reduced to $[Z_o/(Z_o + r)]V_{\rm ob}$ at the node B, whereas the inbound signal at node A is $(Z_o - r)/Z_o$ times lower than that of the inbound signal $V_{\rm ib}$ at node B. Because of the opposite nature (in terms of magnitude) of the inbound and outbound signals at the two nodes, it is possible to eliminate the outbound signal at the receiving port by suitably subtracting the signal V_A (at node A) from the signal V_B (at node B). To completely eliminate the outbound signal in $V_{\rm rx}$, the transconductor first equalizes the magnitude of the outbound signals through the multipliers a_1 and b_1 for signals V_A and V_B, respectively, and then subtracts the resulting signals. In this subtraction process, however, part



(a)



(b)

Fig. 4. (a) Implementation of the proposed FDT. (b) Addition-based transconductor circuit.

of the inbound signal remains in $V_{\rm rx}$. This process can be mathematically expressed by the following equation:

$$V_{\rm rx} = b_1 V_B - a_1 V_A = \left(\frac{Z_o}{Z_o + r} \cdot b_1 - a_1\right) V_{\rm ob} + \left(b_1 - \frac{Z_o - r}{Z_o} \cdot a_1\right) V_{\rm ib}. \quad (2)$$

To eliminate $V_{\rm ob}$, a_1 and b_1 are chosen such that $(a_1/b_1) = (Z_o/Z_o + r)$. With this, we get

$$V_{\rm rx} = \frac{2r}{Z_o} \cdot a_1 V_{\rm ib} + \Delta V_{\rm er}. \quad (3)$$

So, the gain of the receiver or the transconductor part is directly proportional to the coefficient a_1 and the ratio (r/Z_o). Practically the signal $V_{\rm rx}$ in the receiving port may contain unwanted outbound signal $\Delta V_{\rm er}$ which is primarily due to mismatches of (a_1/b_1) and $(Z_o/Z_o + r)$. So, sources of $\Delta V_{\rm er}$ in this case is the variation of the ratio of a_1 and b_1, and also the mismatch of the Z_o and r with their differential counterpart.

It has been demonstrated in [28] that for 10% mismatches in the critical parameters of the sources of $\Delta V_{\rm er}$ both in replica driver hybrid and R-gm hybrid, the latter has a better eye opening of the received signal compared to that of the former. Hence, in terms of robustness, R-gm hybrid is a better technique than the replica driver hybrid. However, R-gm hybrid is not an energy efficient transceiver for a lossy link. With increase in link resistance (R_L), the energy efficiency of both the transmitter and the receiver degrades. Following are the reasons for the degradation of the energy efficiency.

1) The part of the signal current of the transmitter going into the link $(i_{\rm sig})$ in terms of the bias current of

transmitter I_{Tc} is given by

$$i_{\mathrm{sig}} = \frac{Z_o - r}{2Z_o + R_L} \cdot I_{\mathrm{Tc}}. \quad (4)$$

In presence of large R_L, to get good current efficiency of the transmitter ($i_{\mathrm{sig}}/I_{\mathrm{Tc}}$), r should be a small part of Z_o. This requirement directly affects the receiver gain ($V_{\mathrm{rx}}/V_{\mathrm{ib}}$) since from (3), we have seen that the receiver gain is directly proportional to r/Z_o. So, there is a trade-off between efficiency of the transmitter and the gain of the receiver.

2) To improve over-all efficiency, the present trend is to decrease the swing of the outbound signal on the link to a low level (typically, few tens of millivolts). In addition, with increase of R_L, the relative swing of the inbound signal with respect to that of the outbound signal at node B further reduces. As a result, to get a sufficient received signal amplitude, gain of the receiver should be high. Since, gain cannot be increased by increasing (r/Z_o) beyond a certain point (due to the trade-off), a_1 needs to be increased. This increases the power requirement in the transconductor, thereby lowering the overall energy efficiency.

To summarize, for lossy on-chip interconnect, the R-gm hybrid is not a suitable architecture and that is mainly due to its direct trade-off between the receiver gain and current efficiency of the transmitter. In this implementation, this trade-off has been eliminated by replacing the resistive divider with an active circuit which has a directional phase shift property, namely, it inverts the phase of the outbound signal whereas allows the inbound signal to pass with the same phase. This directional property of the active circuit replaces the subtraction based elimination of the outbound signal from the inbound signal by addition based elimination. The active circuit ensure low impedance (Z_o) at node B but high impedance at node A. The low impedance at node B helps to terminate the link without using passive terminator. The high impedance at node A not only helps to increase the efficiency of the transmitter but also increase the gain for the inbound signal from node B to node A. So, the output of the receiver is sum of inbound signal with large amplitude at node A and the inbound signal at node B. As a result, the overall gain for the inbound signal is higher than that of the R-gm hybrid.

B. Proposed Full-Duplex Transceiver

The proposed FDT is shown in Fig. 2(c). It consists of a current-mode transmitter (TX), a directional inverter/buffer (DIB), and a transconductor circuit (gm) performing the weighted addition operation. The TX generates the outbound signal for the data V_{tx} to be transmitted. In this proposed FDT, the DIB plays an important role. It has a special functionality of inverting the phase of the outbound signal and simultaneously allowing the inbound maintain its phase (i.e., buffer mode). More specifically, the outbound signal going from A to B is inverted by 180° whereas the inbound signal passing from B to A maintains its phase. The gains of DIB are $-\alpha$ from node A to node B and β from node B to node A. As the outbound signals at nodes A and B are out of phase to each other, they can be added to zero by equalizing their amplitudes with the weights a_2 and b_2. Due to this operation, on the other hand, the inbound signals at the two nodes are added up. Mathematically, the final received signal V_{rx} is given by

$$V_{\mathrm{rx}} = a_2 V_A + b_2 V_B = (a_2\beta + b_2)V_{\mathrm{ib}} + (a_2 - \alpha b_2)V_{\mathrm{ob}}. \quad (5)$$

From this expression of V_{rx}, it is clear that the outbound signal V_{ob} can be eliminated from the received signal by making its coefficient zero. This can be done by fulfilling the following condition:

$$\alpha = \frac{a_2}{b_2}. \quad (6)$$

With this condition, the expression of the final received signal becomes

$$V_{\mathrm{rx}} = a_2(\beta + \alpha^{-1})V_{\mathrm{ib}} + \Delta V_{\mathrm{er}}. \quad (7)$$

In our implementation, both β and α^{-1} are higher than one, so gain of receiver is high. To compare the performance of the R-gm hybrid transceiver and that of the proposed transceiver, we can find the ratio of the parameters a_1 and a_2 required to get an equal gain of the corresponding receiver for the inbound signal and it is given by

$$\frac{a_1}{a_2} = (\beta + \alpha^{-1}) \cdot \frac{Z_o}{2r}. \quad (8)$$

Moreover, the quiescent current of each of the transconductor circuits (implementing the coefficients a_1, b_1, a_2, and b_2) is square of the coefficient values. So, power of the two transconductor circuits in R-gm hybrid (P_r) is proportional to $a_1^2 + b_1^2$. Similarly, for DIB-gm, the power of transconductor circuits (P_{DIB}) is proportional to $a_2^2 + b_2^2$. So, the ratio of the power in the transconductor circuits of the two transceivers for an equal gain of the inbound signal is given by

$$\frac{P_r}{P_{\mathrm{DIB}}} = \frac{I_{a_1} + I_{b_1}}{I_{a_2} + I_{b_2}} = \frac{1 + \left(\frac{Z_o + r}{Z_o}\right)^2}{1 + \frac{1}{\alpha^2}} \cdot \left(\frac{a_1}{a_2}\right)^2. \quad (9)$$

By taking $r = (Z_o/2)$ as suggested in [28] and with practical values of β (= 2.9) and α^{-1}(= 2.8) in our implementation, this ratio becomes 12. Hence, the receiver or transconductor of the proposed DIB-gm hybrid is much more power efficient compared to that of the R-gm hybrid.

Another aspect of the DIB is that small signal impedance at node B is low while that at node A is high. So, when the DIB is connected to the interconnect at its low impedance node B, it helps to enhance the bandwidth of link for both transmitting and receiving mode without any passive terminator. The high impedance at node A helps to receive the inbound current signal in amplified voltage form and also increases the efficiency of the transmitter. High impedance of the output port of the current-mode TX helps to maintain the net impedance at node A high. The signal current generated by the TX is

$$i_{\mathrm{sig}} = \frac{\alpha Z_A}{Z_o + R_L} \cdot I_{\mathrm{Tp}} \quad (10)$$

where Z_A is the impedance at node A as seen by the TX. From (4) and (10), the ratio of the current required by the

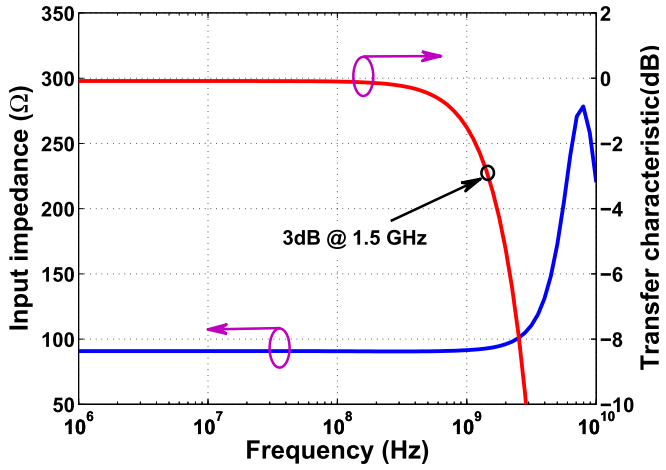


Fig. 5. Impedance at node B of the transceiver and transfer characteristic of the signaling system.

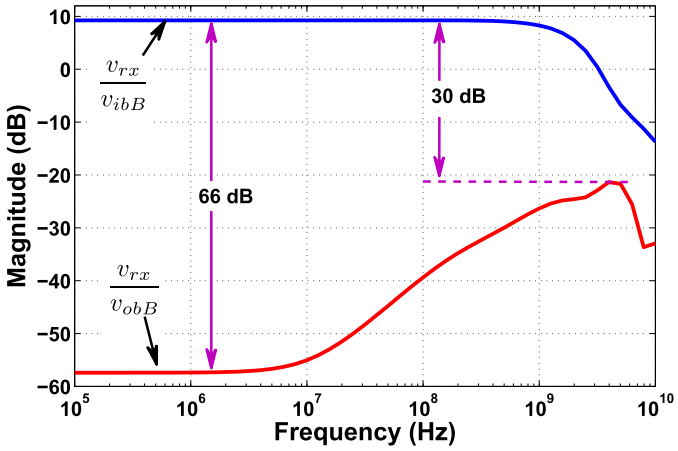


Fig. 6. Ratio of received signal with respect to the inbound and outbound signal at the input/output node B of the transceiver.

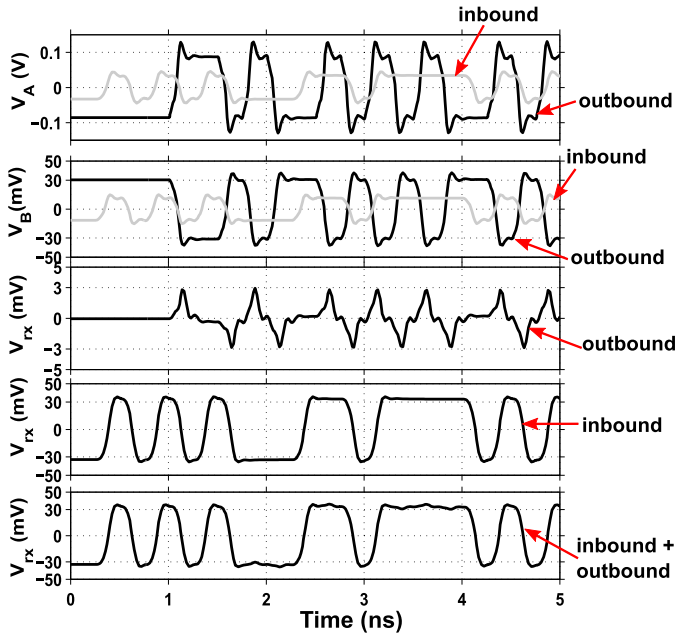


Fig. 7. Inbound and outbound signals at node A, node B, and output of transconductor of the transceiver.

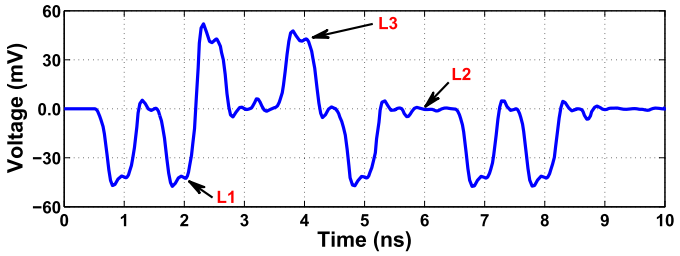


Fig. 8. Signal at the middle of the interconnect.

transmitter of R-gm and that of DIB-gm to achieve the same signal current can be calculated and it is given by

$$\frac{I_{\mathrm{Tc}}}{I_{\mathrm{Tp}}} = \frac{\alpha Z_A(2Z_o + R_L)}{(Z_o - r)(Z_o + R_L)}. \tag{11}$$

In our implementation, Z_A = 450 Ω, Z_o = 90 Ω, and R_L = 155 Ω, with which the current ratio becomes 4.9. From this, it can be concluded that the transmitter in the proposed transceiver also has better power efficiency compared to that in the R-gm hybrid architecture. It is to be noted that DIB being an active circuit, requires static bias current close to $2.8I_{\mathrm{Tp}}$ for our implementation. Considering this quiescent current, it is observed that TX in the proposed FDT is more efficient that the TX in R-gm hybrid by 1.3×.

III. Analysis and Circuit Design of the Proposed Transceiver

A. Directional Inverter/Buffer

Transistor level implementation of the DIB is shown in Fig. 3(a). It has two cross-coupled transistors M1 and M1′ driving two diode connected active inductive peaking loads M2 and M2′. As discussed before, one of the important property of DIB is low impedance at its differential port B-B′. To justify this property, we have considered the small signal equivalent circuit shown in Fig. 3(b). In this equivalent circuit, we assume M1-M1′ and M2-M2′ are identical. The single ended small signal impedance seen by the inbound signal at node B is given by

$$Z_{ibB} = \frac{1}{G_{m1}} - \frac{1}{G_{m2}} \tag{12}$$

where $G_{m1} \approx g_{m1} + g_{mb1}$ and $G_{m2} = g_{m2} + g_{mb2}$ for the transistors M1 and M2, respectively. So, the impedance at node B can be made very small by adjusting the value of this difference even though both $1/G_{m1}$ and $1/G_{m2}$ are significantly larger. Hence, inbound signal current sees a very low impedance at node B but sees a relatively larger impedance $Z_{ibA} = 1/G_{m2}$ at node A. For stability of DIB, Z_{ibB} should be positive.

On the other hand, the single ended impedance seen by the outbound signal current going from A to B is

$$Z_{obA} = -\frac{1}{G_{m1}} - R_L - Z_{\mathrm{inf}} \tag{13}$$

where R_L is the resistance of the interconnect and Z_{inf} is the input impedance of the similar transceiver sitting at the

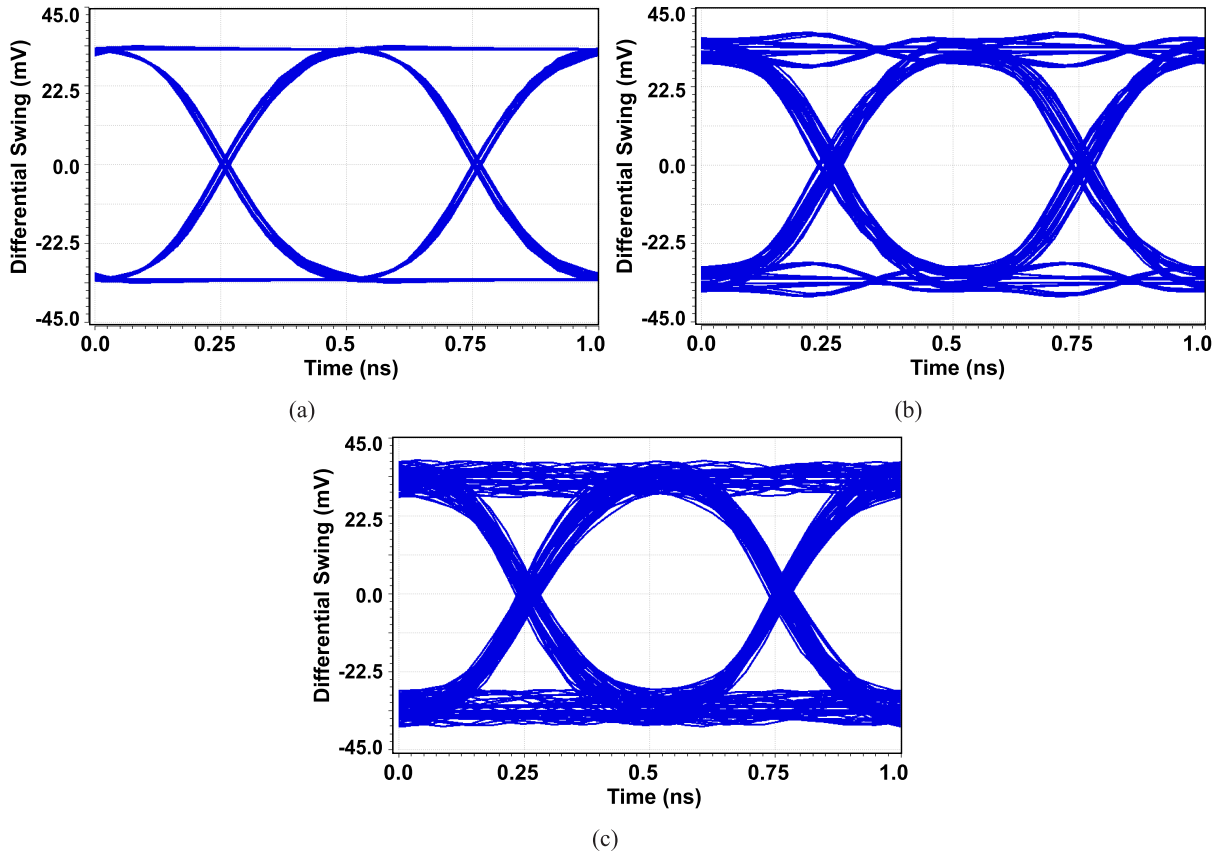


Fig. 9. (a) Half-duplex signaling of 2 Gb/s. (b) FD signaling with a data transmission of 2 Gb/s from transceivers at both the ends. (c) FD signaling with a data transmission of 2 and 2.1 Gb/s from the far end and the near end transceivers, respectively.

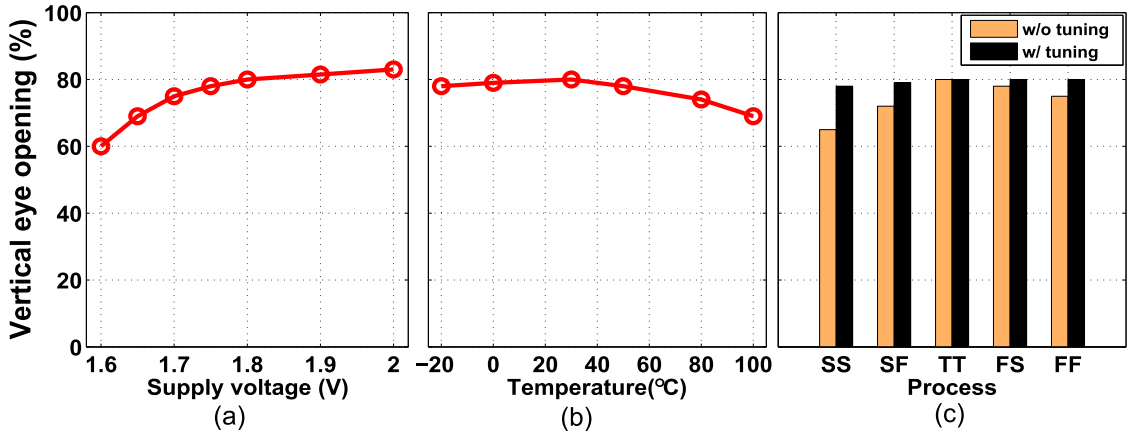


Fig. 10. Variation of vertical eye opening with PVT variations.

far end of the link. The outbound signal faces the negative impedance Z_{obA} at node A whereas it sees a positive resistance $Z_{obB}= R_L + Z_{\text{inf}}$ at node B. Because of this, the outbound signals at nodes A and B are out of phase to each other by 180°. The values of two gains α and β of the DIB with this implementation is

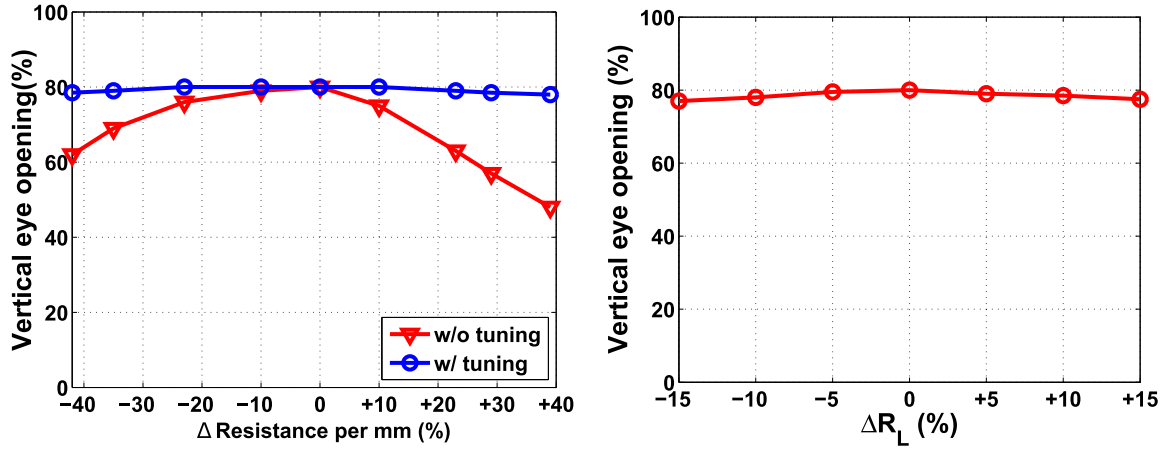
$$\alpha = \frac{R_L + Z_{\text{inf}}}{\frac{1}{G_{m1}} + R_L + Z_{\text{inf}}} \tag{14}$$

$$\beta = \frac{G_{m1}}{G_{m2} - G_{m1}}. \tag{15}$$

From these two equations, we can conclude that $\alpha < 1$ and $\beta > 1$ for the proposed DIB.

B. DIB-gm Hybrid

The transistor level circuit diagram of the proposed FDT consisting of the DIB, the transmitter (TX), and the transconductor (gm) (working as receiver) is shown in Fig. 4(a). The CML based transmitter has been used to generate high speed outbound signal. In TX, the two transistors M3 and M3′ steer the current I_{TX} either in node A or node A'



(a) (b)

Fig. 11. Variation of eye opening. (a) With variation of link resistance per mm. (b) In presence of link mismatch.

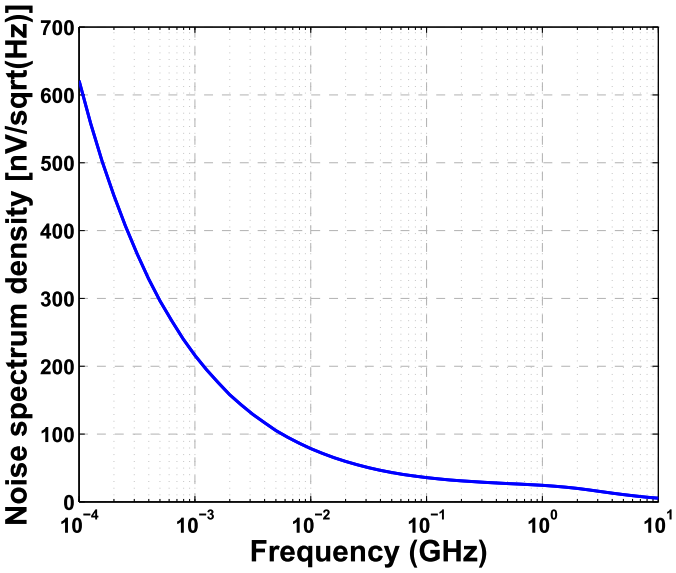


Fig. 12. Output noise spectrum density of the transceiver.

depending on the logic signal to be transmitted. The circuit diagram of the transconductor for performing addition is shown in Fig. 4(b). The two differential signals V_A and V_B are fed to the two differential input ports IN_a and IN_b of the transconductor. The two differential voltages are first converted into current signals, which are then added by flowing them through a common load. The added currents are then converted back to voltage by the common gate stage. It may be noted that before feeding to the adder, the common mode level of signal V_A is shifted to a lower level using the common drain stage. With this implementation, the ratio of the coefficients of addition [earlier denoted by a_2 and b_2 in Fig. 2(c)] is given by

$$\frac{a_2}{b_2} = A_{\text{cd}} \cdot \sqrt{\frac{W_a L_b}{W_b L_a}} \cdot \sqrt{\frac{I_a}{I_b}} \tag{16}$$

where A_{cd} is the gain of the common drain stage, and W_a/L_a and W_b/L_b are the width/length of the transistors M_a and M_b,

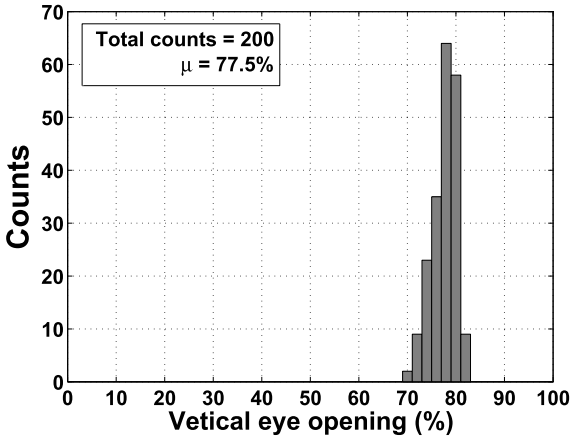


Fig. 13. Monte Carlo simulation for the vertical eye opening.

respectively. From (6), (14), and (16), the condition to be satisfied to eliminate the outbound signal at the output node of the transconductor can be obtained as

$$\sqrt{\frac{I_a}{I_b}} = A_{\text{cd}}^{-1} \cdot \sqrt{\frac{W_b L_a}{W_a L_b}} \cdot \frac{(R_L + Z_{\text{inf}})}{\left(\frac{1}{G_{m1}} + R_L + Z_{\text{inf}}\right)}. \tag{17}$$

As satisfying this equality condition is crucial to avoid the outbound signal at the receiver output, we kept tuning option for the I_a/I_b ratio to counter any process variation in the right-hand side of this equation.

IV. Implementation and Simulated Performance

In order to verify the operation of the proposed transceiver, it has been designed in the 0.18-μm UMC CMOS process. Simulated performance using the Cadence Spectra has been reported in this section.

The length of the global interconnect that we have considered is 5 mm. The second top metal M5 has been used for implementing the differential signal line having the width and spacing of 2 and 1.5 μm, respectively. The top and the adjacent bottom metal layers are filled by ground strips following the Manhattan routing style. The normalized transfer function

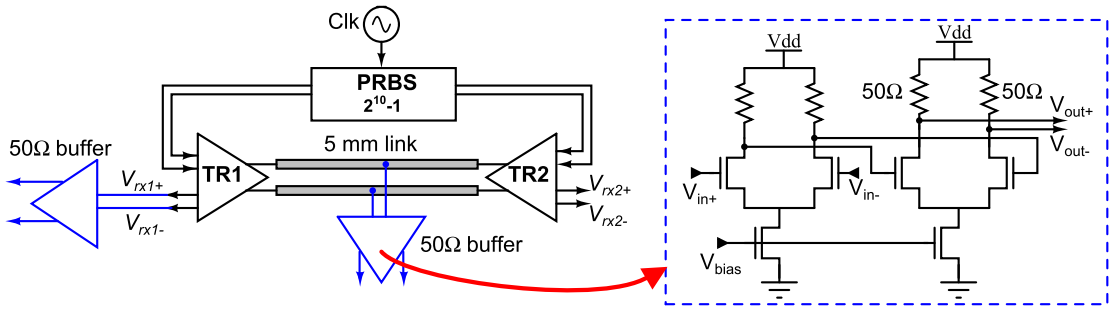


Fig. 14. Test setup of the prototype design.

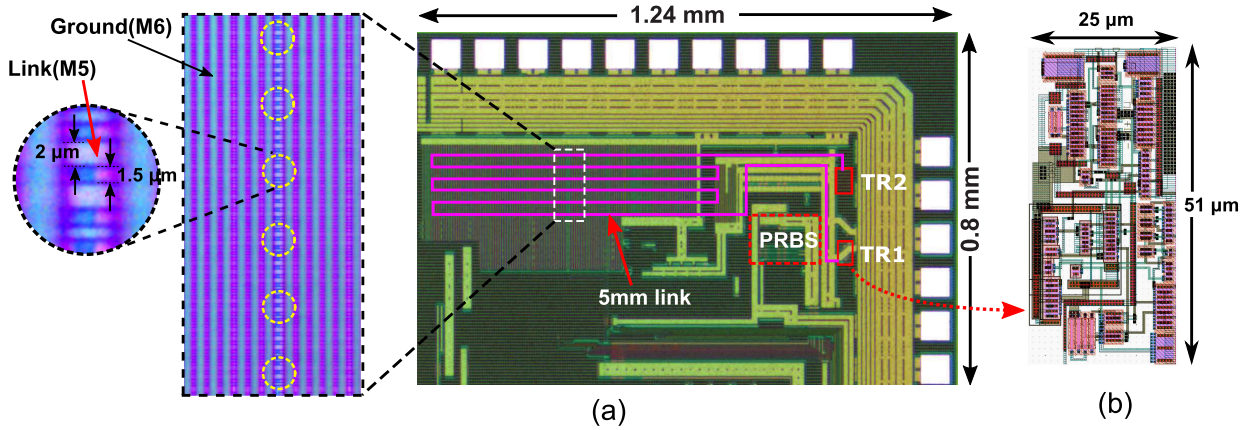


Fig. 15. (a) Die photograph of the test chip. (b) Layout of transceiver.

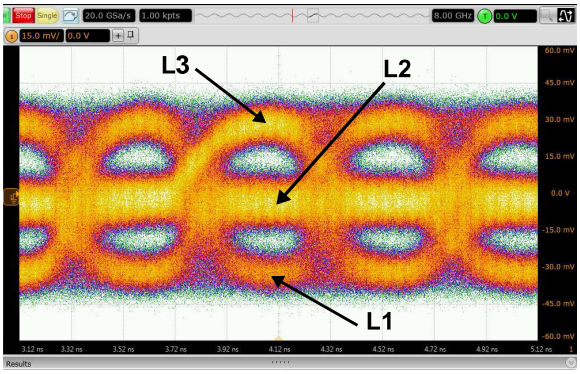
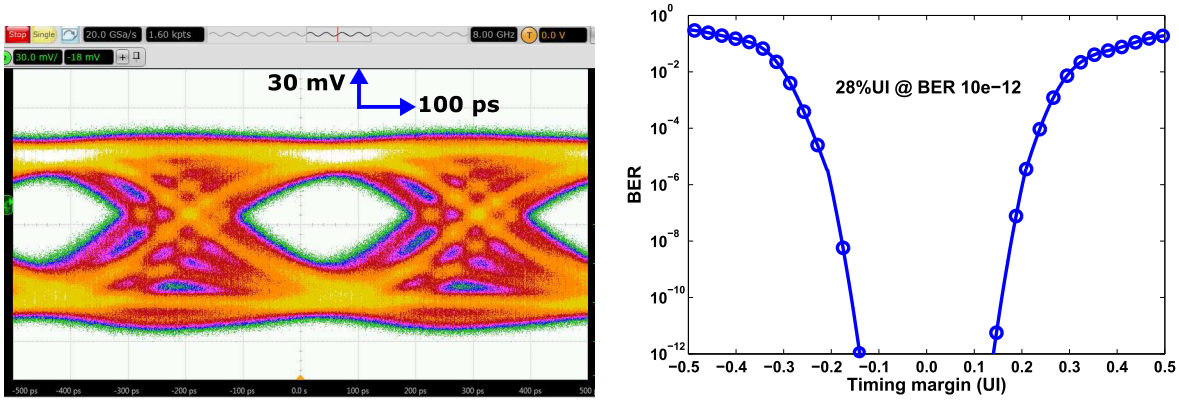


Fig. 16. Measured eye at the middle of the link for an FD signaling of 4.0 Gb/s.

from input of the transmitter of the near end transceiver to the receiver's output of the far end transceiver including the link and the post layout parasitics of transceiver has been shown in Fig. 5. The transfer function has a 3 dB cutoff point at 1.5 GHz. In the same figure, the single ended impedance of the link port (input/output node B) of the transceiver is shown. The impedance is adjusted to 90 Ω. The magnitude of the ratio of $V_{\rm rx}$ to both the inbound (V_{ibB}) and the outbound (V_{obB}) signals at input/output node B of the transceiver has been plotted against frequency as shown in Fig. 6. In low frequency range, $V_{\rm rx}$ has inbound signal 66 dB higher than the outbound signal. The component of the outbound signal rises up with increase in frequency up to 4 GHz, however, it is still 30 dB lower from than the component of inbound signal.

In order to see the transient response of the transceiver, a bit pattern is transmitted from near end toward the far end. Likewise, another bit pattern from the far end is transmitted toward the near end. The inbound signal component and the outbound signal component of the signal at node A (V_A), node B (V_B) and the receiver output ($V_{\rm rx}$) of the transceiver have been plotted in Fig. 7. As expected, the outbound signals at node A and B are out of phase by 180° whereas the inbound signals at these two nodes are in phase. The corresponding directional gains α and β are 0.36 and 2.9, respectively. At $V_{\rm rx}$, the peak to peak error voltage (due to outbound signal only) is 5.8 mV, whereas the inbound signal has a differential amplitude of 67 mV. So, in FD operation, small ripples of the error voltage are observed in $V_{\rm rx}$. Fig. 8 shows the differential signal at the middle of the interconnect for the FD operation. This signal consists of three levels L1, L2, and L3 as it is superposition of two non-return-to-zero (NRZ) signals having the same amplitude at this point.

The eye diagram of the data stream received by one of the two transceivers ($V_{\rm rx}$) is plotted for three different situations as shown in Fig. 9. Fig. 9(a) is the plot of half-duplex signaling when only the far end transceiver is transmitting a data stream at 2.0 Gb/s data rate. Fig. 9(b) gives the plot of FD operation when both the transceivers at the two ends are transmitting data streams at the rate of 2.0 Gb/s. It may be observed from the eye diagrams of the two cases that the jitter in FD signaling increases to 0.11 UI from 0.05 UI in case of half-duplex signaling. Fig. 9(c) shows the eye diagram when the near end transceiver is transmitting at 2.0 Gb/s data rate, whereas the far end transceiver is transmitting 2.1 Gb/s at data rate. In this case the jitter is 0.12 UI. It may be observed that the quality of the eye diagram in Fig. 9(b) is practically same as that of the



(a) (b)

Fig. 17. Measurement of the received data streams by TR1 for an FD signaling of 4 Gb/s. (a) Eye diagram (2 Gb/s). (b) Bathtub curve.

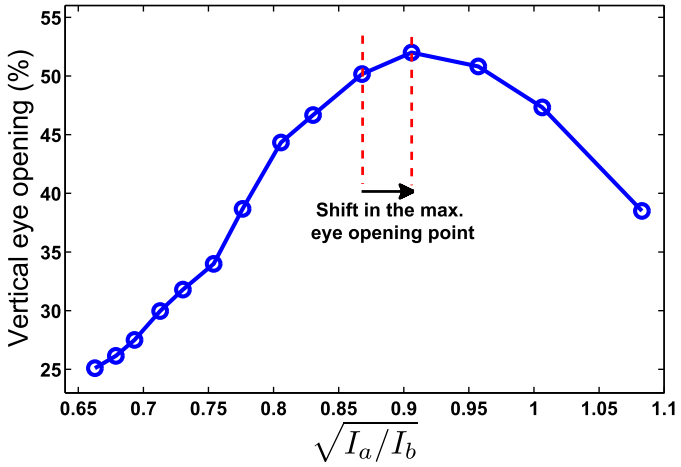


Fig. 18. Measured variation of vertical eye opening with changing the ratio of I_a and I_b.

eye diagram in Fig. 9(c). Hence, we may conclude that the two transceivers can communicate with each other asynchronously. In this context, we would like to mention that the separation of the inbound signal from the outbound signal is done in a continuous time domain. So, it is possible to incorporate pre-emphasis driver in the transmitter to maintain the speed for longer links. However, it is beyond the scope of this paper.

A. Effects of PVT Variations and Mismatches

In the proposed FDT, we are matching two parameters defined by (6) to remove the outbound signal from inbound signal. So, it is important to analyze the performance of the circuit in presence of process, supply voltage, and temperature (PVT) variations and also with link mismatch and device mismatch. Fig. 10 gives the variation of the vertical opening of the eye in FD operation at 2 × 2.0 Gb/s with the PVT variations. By lowering the supply voltage from 1.8 to 1.65 V, the eye closes by 10% only. However, for supply voltage higher than 1.8 V, the eye opening remains practically constant. Similarly, increasing the temperature to 80 °C from room temperature, the eye closes by 6% only, whereas, the eye opening remains almost constant for lower temperature. Likewise, for different process corners the eye opening slightly reduces with respect to that in typical corner. The worst case eye opening occurs in the case of slow–slow (SS) corner where it decreases by 15%.

As (6) is also involves on the link resistance, the vertical eye opening also depends on it. The link resistance per mm of the metal layer used for the implementation of the link may vary due to variation of width, height, and resistivity. The variation of the eye opening with change in the resistance of the link per mm is shown in Fig. 11(a). For 15% increase in the link resistance, the eye opening decreases by 10%, whereas for 15% decreases in link resistance, it decreases by 2% only. The variation of the vertical eye opening with the mismatch of the differential link is shown in Fig. 11(b). The eye opening almost remains constant with ±15% mismatch between the two lines.

In order to estimate the BER for the worst case eye opening, the noise spectrum density at the output of the receiver has been simulated and it is shown in Fig. 12. The total integrated noise of this graph is 1.5 mV rms. The worst case eye opening occurs when the process, voltage and temperature are SS, 1.65 V and 80 °C, respectively, and link resistance is increased by 15%. In this worst case eye opening, the BER is $< 10^{-16}$ for 39% UI. It is to be noted that the process variation of transistors and the variation of the link resistance per mm may be compensated by silicon tuning option. This has been done by tuning the ratio of I_a and I_b to get the maximum eye opening as shown in Figs. 10(c) and 11(a). Considering this silicon tuning, BER for the worst case situation is $< 10^{-16}$ for 54% UI.

The vertical eye opening of the proposed transceiver is fairly robust to device mismatches. Fig 13 gives the variation of the vertical eye opening for 200 runs of Monte Carlo simulation. It may be seen that 83% of the total samples have vertical eye opening greater than 75%.

V. Measurement Results

The block diagram of the test-setup for evaluating the proposed transceiver has been shown in Fig. 14. A pseudorandom binary sequence (PRBS) generating two channels of high speed data streams of length $2^{10} - 1$ each and having 180° shift between the two patterns has been designed using the architecture demonstrated in [33]. The two data channels are fed to the two FDTs TR1 and TR2, which are connected across

TABLE I
COMPARISON OF THE PROPOSED ARCHITECTURE WITH THE RECENT LITERATURE

Ref	Tech (nm)	TX Type	RX Type	Length (mm)	Link Type	Supply (V)	Speed (Gbps)	BER	Efficiency (pJ/b)	Efficiency (pJ/b/mm)	Area(μm²) (TX+RX)
[1]	65	Cap.	CT	6	Uni-directional	1.2	10.0	$<10^{-12}$	1.04	0.17	11570[a]
[27]	65	CM	CM	5	Full-Duplex	1.0	10.0[b]	-	0.38[b]	0.076[b]	-
[23]	90	CM	RT	5	Half-Duplex	1.0	8.0	$<10^{-12}$	0.9	0.18	2000
[6]	90	CM	CM	10	Uni-directional	1.2	6.0	$<10^{-4}$	0.63	0.063	1760
[21]	130	VM	RT	5	Uni-directional	1.2	6.0	$<10^{-10}$	0.7	0.14	-
[19]	130	VM	AT	10	Uni-directional	1.2	3.0	$<10^{-12}$	2.0	0.20	1300
[5]	180	Cap.	CT	10	Uni-directional	1.8	1.0	$<10^{-11}$	2.8	0.28	-
[5]*	180	VM	VM	10	Uni-directional	1.8	1.0	-	11.0	1.1	-
[20]	180	VM	VM	20	Uni-directional	1.8	2.0	-	8.05	0.40	-
[15]	180	VM	RT	3	Uni-directional	1.8	8.0	$<10^{-14}$	3.1	1.03	-
[26]	180	VM	VM	5	Full-Duplex	1.8	0.92	-	9.48	1.89	2100
This Work	180	CM	AT	5	Full-Duplex	1.8	4.0	$<10^{-12}$	0.95	0.19	1275

CM: Current Mode, VM: Voltage Mode, CT: Capacitive terminated, RT: Resistive terminated, AT: Active terminated
[a]including SerDes, [b]simulated, *CMOS repeater based baseline design.

a 5 mm link. 50 Ω buffer circuits have been used to observe the signals at the middle of the link and received signal of TR1. Fig. 15 shows the die photograph of the fabricated test chip. The link implemented with M5 has a width of 2.0 μm and a spacing of 1.5 μm. The top metal M6 and the lower metal M4 have been filled with ground strips. QFN 48 pins package has been used to package the die. The area occupied by one transceiver is 51 μm $\times$ 25 μm.

Two data streams of rate 2.0 Gb/s each have been generated by the PRBS generator and fed to the two transceivers. So, the total FD data rate is 4.0 Gb/s across the link. The signal at the middle of the link is measured through the 50 Ω buffer using Agilent oscilloscope DSA-X92504Q. Eye diagram of the observed signal is shown in Fig. 16. The eye diagram clearly shows the superposition of two equally strong NRZ signals and hence has three levels in the FD operation. It is to be noted that in the process of measurement, significant noise is added which degrades the quality of the low swing signal. However, this signal is much cleaner on the link. The received signal by the transceiver TR1 has been shown in Fig. 17(a). The corresponding bathtub curve having an UI of 28% at BER of 10^{-12} is shown in Fig. 17(b). The vertical eye opening has been measured by varying the ratio of I_a and I_b as shown in Fig. 18. The required value of $(I_a/I_b)^{1/2}$ at which the eye has maximum vertical opening shifts to a little higher value by 4.5% compared to its nominal value set in design. This shift is due to variation in α. The total overall energy efficiency at this data rate is 0.19 pJ/b/mm.

Table I gives the comparison of the performance of the proposed transceiver with that of designs in the literature, which are implemented across different technology nodes. It may be noted that the link architectures in the literature are mostly unidirectional and only few recent works are on bidirectional link. As expected, the implementation technology node has a big impact on the achieved energy efficiency. It may be seen that the energy efficiency of our proposed design is superior to the designs implemented in 180-nm technology. Also, the area occupied by the proposed transceiver is smaller than that of the literature designs, even if they are implemented on lower technology node. The speed and the energy efficiency of the proposed transceiver scales with the technology. The simulated data rate for the same link length and for the same amount of total static current consumption in 65-nm technology with a supply of 1.0 V is 10 Gb/s. So, the simulated energy efficiency of the design in 65-nm is 0.1 pJ/b.

VI. CONCLUSION

In this paper, a current-mode transceiver for FD data communication across on-chip global interconnects has been presented. The proposed transceiver can transmit and receive data simultaneously over the same interconnect. The separation of the inbound signal and the outbound signal is done by the combination of a DIB circuit and a transconductor circuit. The active low impedance at the input/output node of the transceiver helps to enhance the bandwidth of transmission without any passive terminator. The proposed transceiver architecture has been implemented in 0.18-μm, 1.8 V CMOS process for a global interconnect of 5 mm length. The transceiver has an efficiency of 0.19 pJ/b/mm for a data rate of 4.0 Gb/s FD data transmission. The FDT offers a factor of two better wire efficiency while a factor of ten better energy efficiency.

While the efficacy of the proposed FDT has been demonstrated for lossy on-chip link, the proposed transceiver can be directly used for die-to-die communication through silicon interposers. It also can be deployed for off-chip interconnects (PCB/cables).

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