A 950 nW Analog-Based Data Reduction Chip for Wearable EEG Systems in Epilepsy

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***Abstract*— Long-term electroencephalogram (EEG) monitoring is an important tool used for the diagnosis of epilepsy. Truly Wearable EEG can be considered as the future of ambulatory EEG units, which are the current standard for long-term EEG monitoring. Replacing these short lifetime, bulky units with long-lasting miniature and wearable devices which can be easily worn by patients will result in more EEG data being acquired for longer monitoring periods. This paper presents an analog-based data reduction integrated circuit that would reduce the amount of power required to transmit EEG data by identifying the sections of data that are interesting for diagnostic purposes while discarding the background activity. Using the data reduction system as part of a miniature wireless, EEG monitoring unit would yield significant reductions in power consumption since the transmitter will only be switched ON based on the data reduction system output. A system prototype chip has been fabricated in a 0.35 μm CMOS process. The system consumes 760 nA from a 1.25 V supply and is able to achieve a sensitivity of 87%, while transmitting 45% of the overall EEG data.**

***Index Terms*— Continuous wavelet transform (CWT), data reduction, electroencephalogram (EEG), epilepsy, epileptic spike detection, long-term EEG monitoring, low-power electronics, spikes, wearable EEG (WEEG).**

I. Introduction

EPILEPSY is a serious neurological disease affecting 60 million patients globally. Despite this large number of sufferers, accurate diagnosis of the disease remains challenging with 20%–30% of sufferers being misdiagnosed.

The electroencephalogram (EEG) is typically used for epilepsy diagnosis by monitoring the brain activity from the scalp. Epileptic EEG traces can be categorized into two phases: ictal (seizure activity) and interictal (spikes and spike and wave activity occurring between seizures). Interictal activity is more frequent than ictal activity; 50% of patients present interictal discharges in their first EEG session. Furthermore, interictal discharges can provide useful information for clinical diagnosis, such as seizure type and the likelihood of recurrence [1].

Traditionally, EEG monitoring is performed in an inpatient setting and lasts for 20–30 min. Since the test is performed in a clinic, patients are not monitored in their natural environment and are not subjected to stimuli that may lead to indicative activity. Furthermore, events may not be recorded due to the short duration of the tests.

Ambulatory EEG (AEEG) performs the monitoring task in the comfort of the patients' home and has certain benefits in comparison to inpatient monitoring, such as lower cost and longer duration recordings [2]. However, AEEG units in their current form have certain limitations [3].

1) They are bulky and heavy (over 500 g) for the patient to carry during routine activities.
2) Long wires connecting the electrodes to the recording unit result in limited patient movement.
3) They have a short battery lifetime (2–3 days) due to the power consumption required to record EEG data.
4) Specialist analysis of the recorded EEG data is time consuming, taking approximately 2 h per 24 h of recorded data.

Therefore, there is a clear need for a non-invasive, wireless, light-weight and low-power Wearable EEG (WEEG) unit that can be comfortably worn by the patient for long time periods. For a 1 cm^3 WEEG unit consisting of at least an instrumentation amplifier (IA), an analog-to-digital converter (ADC), and a transmitter to run continuously on a Li-battery with an energy storage of 100 mWh for 30 days, the average power consumption must be lower than 140 μW [4]. A number of suitable IAs and ADCs have been recently reported and closely followed the technical requirements for recording EEG signals provided by the International Federation of Clinical Neurophysiology (IFCN) [5]. For example, the IA presented in [6] consumes 1.62 μW and a 12-bit ADC consuming 200 nW for a sampling rate of 500 S/s, has been reported in [7].

Table I summarizes the performance of various state-of-the art low-power transceivers. Based on the values of energy used per bit transmitted (e_t) for the commercially available CC2500 [8] and nRF24L01+ [9], 40 nJ/bit has been taken as a conservative figure, achievable over most wearable environments for short-range communication. A lower bound of 4 nJ/bit has been considered for e_t based on the performance of the bluetooth low energy CC2640R2F [10] and the recently published works of [11] and [12], which are comparable to the mentioned commercial transmitters in terms of transmitter output power and data rate. Based on the mentioned figures for e_t, to continuously transmit the EEG data in a 32 channel WEEG unit (sampled at 500 Hz with a resolution of 12 bits to meet the standards of [5]) the transmitter would consume 7.5 mW in the conservative case and 768 μW, if the lower bound for e_t is considered. It is therefore clear that the WEEG unit power

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TABLE I
SUMMARIZED PERFORMANCE OF STATE-OF-THE-ART TRANSCEIVERS

	CC2500 [8]	nRF24L01+ [9]	CC2640R2F [10]	Huang JSSC'12, [11]	Sayilir JSSC'14, [12]
Data rate (Mb/s)	0.5	1	1	0.1	1
Maximum Tx power (dBm)	1	0	5	-6	-4.4
Tx power consumption (mW)	38.7 (1.8 V)	21.5 (1.9 V)	11 (1.8 V)	0.89 (1 V)	4.5 (1 V)
Tx energy per bit (nJ/bit)	77.4	21.5	11	8.9	4.5

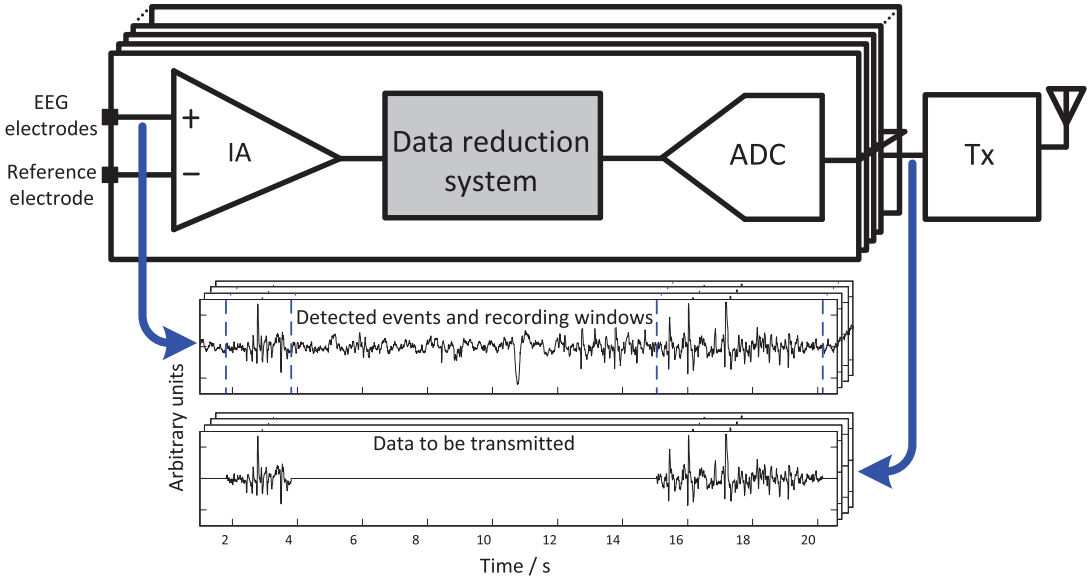

Fig. 1. Conceptual implementation of wireless WEEG unit incorporating a data reduction stage.

consumption would be dominated by the transmitter, due to the continuous transmission of raw EEG data.

A number of recent publications have focused on reducing the power consumed by the transmitter, or completely eliminating this module, by detecting the ictal activity present within EEG traces locally. The ictal activity detection system reported in [13] reduces the transmitter data rate (i.e., power consumption) by only transmitting feature-vectors, representing underlying seizure activity, rather than raw EEG data obtained from the scalp. The resulting 14× reduction in system power consumption allows for the integrated circuit to be utilized as part of a chronic treatment system. Wireless transmission has been avoided in the systems presented in [14] and [15] by performing seizure detection and storing the sections of EEG data indicative of seizures on-chip, requiring later manual data retrieval by a neurologist. On-chip feature extraction and classification of seizures have been combined with a non-invasive transcranial electrical stimulator in [6]. Therefore, a transmitter is not incorporated in the system due to the close-loop form of the system, which is required to suppress seizure activity in real time.

For the first time, this paper presents a scalable EEG data reduction system that would continuously select sections of data containing likely interictal activity present within EEG traces. Therefore, the transmitter would only be required to transmit these sections, which can result in significant reductions in the overall WEEG unit power consumption. Simultaneously, the data reduction system would reduce the amount of time required by neurologists to review the transmitted data, but does not replace their role in diagnosis.

Since both interictal and ictal phases present within EEG traces are highly relevant in the context of epilepsy diagnosis, a WEEG unit designed for this purpose should ideally be capable of selecting all epileptiform activities present within the EEG data for transmission and not only the interictal segments. It should also be noted that interictal activity detection blocks generally do not perform strongly in detecting ictal activity and vice versa. Therefore, the authors believe that by combining the ultra-low power chip proposed in this paper together with the ictal activity detection sections proposed in [6], [13]–[15], a full WEEG solution to aid epilepsy diagnosis can be realized.

The remainder of this paper has been organized as follows. The concept of the data reduction in the context of epilepsy monitoring has been explained in Section II. This is followed by the architecture of the system together with individual circuits used in the system in Section III. The front-end and biasing circuits have been presented in Section IV followed by the measured performance of the fabricated chip in Section V.

II. DATA REDUCTION IN WEEG

A WEEG unit incorporating the data reduction system proposed in this paper has been shown in Fig. 1. Using the

TABLE II
POWER COMPARISON OF CONVENTIONAL WIRELESS EEG (NO DATA REDUCTION) AND WEEG INCORPORATING DATA REDUCTION STAGE

	Conventional wireless EEG	**Wearable EEG** ($C = 0.5$)
IA array [6]	51.9 μW	51.9 μW
ADCs (12b, 500 S/s) [7]	6.4 μW	6.4 μW
Data reduction array	-	30.4 μW
Transmitter [10] Active: 192Kbps$\times$11nJ/b	2112 μW	2112 μW$\times$0.5
Total	2171 μW	1145 μW

data reduction approach, the final output of the system is not "marked" data, but rather raw EEG signals with a higher probability of clinical significance. Hence, the final decision on whether a certain section of the transmitted EEG does contain a given epilepsy feature is carried out by the neurologist. This will minimize the risk of misclassifying less typical seizure manifestations in the EEG data.

The total power consumption of the system can be calculated as

$$P_{\text{sys}} = NP_{\text{IA}} + NP_{\text{ADC}} + CP_t + NP_c \tag{1}$$

where P_{IA}, P_{ADC}, P_t, and P_c are the power consumption values for the IA, ADC, wireless transmitter, and data reduction stages, respectively. The number of channels within the unit is N and C is the data reduction factor. In order for the incorporation of the data reduction system in a WEEG unit to be advantageous in terms of reducing the overall power, $CP_t + NP_c$ must be smaller than the power consumed by the transmitter in the case of continuous transmission (i.e., without data reduction). It can also be noted that the benefits of the data reduction system in terms of power are independent of P_{IA} and P_{ADC}. Therefore, future improvements in the performances of the IA and ADC blocks will only improve the operating lifetime of the WEEG unit without obviating the need for the data reduction system.

The benefits of the data reduction stage in terms of power savings have been illustrated in Table II, by comparing power figures for a 32 channel conventional wireless EEG unit (with no data reduction) and a WEEG unit with the same number of channels utilizing the data reduction system. It has been assumed that both units have 32 channels consisting of an array of IAs, ADCs and a transmitter, with the only difference of an array of data reduction blocks providing 50% data reduction ($C = 0.5$) utilized in the WEEG unit. Power figures for the data reduction stages are based on our actual measurements assuming 32 channels. The power numbers for the IA and ADC arrays are taken from [6] and [7], respectively, while the transmitter is assumed to be the commercially available CC2640R2F [10]. It can be noted that the presence of the data reduction stage in the WEEG unit allows for 47% reduction in the overall system power consumption in comparison to the conventional device.

The data reduction algorithm used as a foundation for this paper utilizes the continuous wavelet transform (CWT) to identify interictal activity [16], [17]. Other automated interictal activity detection algorithms, implemented in software, have been reported in [18]–[20]. The algorithms presented in [18] and [19] were based on artificial neural networks (ANN). These reported sensitivities of 90% and 93%, and false positive rates (FPR) of 6.1% and 26%, respectively. Note, however, that these performance metrics are not directly comparable to the work in this paper, since these algorithms focused on automatic feature detection as opposed to data selection. Furthermore, ANNs generally have high computational complexity and are not suitable for hardware implementations with stringent power budgets [21]. A discrete wavelet transform (DWT)-based approach, also for automatic detection as opposed to data selection, with a sensitivity of 91.7% and FPR of 10.7% was reported in [20]. Although algorithms based on DWT could potentially be more power efficient than those based on ANNs, a low-power implementation of the DWT reported in [22] (not specific for epilepsy) consumed over 25 times more power than the work presented in this paper.

The operation of the algorithm implemented in this paper is based on the CWT at two different scales together with a threshold, as shown in Fig. 2. The CWT operation is based around a mother wavelet $\psi(t)$, which extracts signal frequency content at a particular time. The CWT of a signal $x(t)$ is given by

$$W(a,b) = \frac{1}{\sqrt{a}} \int_{-\infty}^{\infty} x(t)\psi^* \left(\frac{t-b}{a}\right) dt \tag{2}$$

where ψ^* is the complex conjugate of the mother wavelet, a is the analysis scale and b is the time at which the transform is performed. Scales 5 and 20 are used for the CWT and amongst the different choices of mother wavelets available, the Mexican hat mother wavelet [defined as (3)] has been chosen due to its proven suitability for studying epileptic events [21], [23]

$$\psi(t) = \frac{2}{\pi^{1/4}\sqrt{3}}(1-t^2)e^{-t^2/2}. \tag{3}$$

After calculating the CWT (Fig. 2), the normalized wavelet powers are evaluated to account for changes in EEG amplitude. The EEG signal variance (σ), needed for this, is calculated over pre-defined time intervals.

Possible interictal spikes are identified with the help of thresholding. An event is chosen as a potential interictal spike if the wavelet power at scale 5 (P_5) is greater than a user set

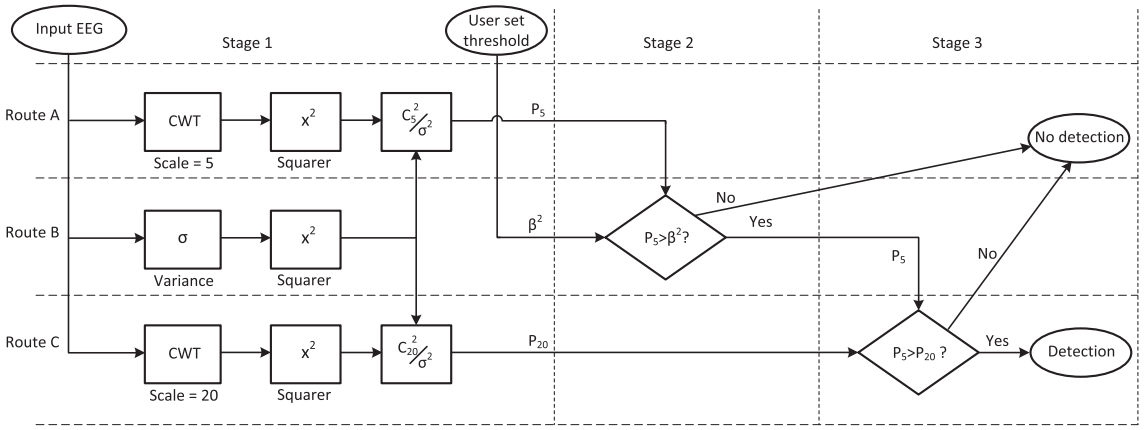

Fig. 2. Detailed operation of data reduction algorithm [21].

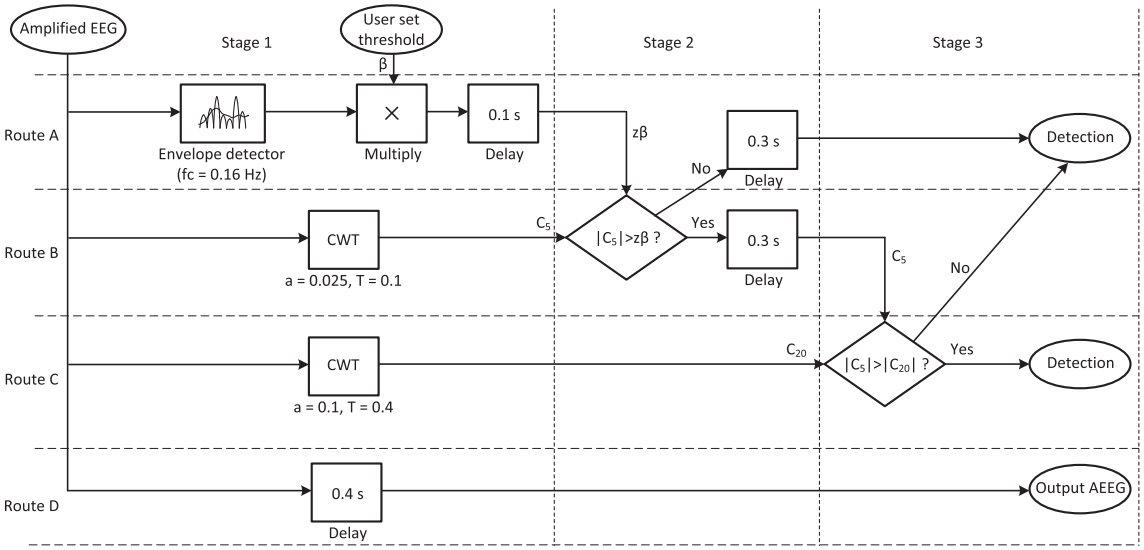

Fig. 3. Overview of modified data reduction algorithm for hardware implementation [16].

threshold ($\beta^2 = \{0.1 - 0.9\}$). The wavelet power at scale 20 (P_{20}) is added as a rule to reject artifacts.

The algorithm in the form of Fig. 2 is, however, not optimized for a hardware implementation that operates in real time for two reasons. First, the variance is calculated over blocks of EEG data and should be replaced with a normalizing factor that can be calculated on-the-fly. Furthermore, in practical terms, the CWT is the convolution of the signal $x(t)$ with an impulse response $h(t)$, where $h(t)$ is defined as

$$h(t) = \frac{1}{\sqrt{a}}\psi\left(\frac{-t}{a}\right). \tag{4}$$

Since $\psi(t)$ is centered around $t = 0$ and is non-causal, a hardware implementation with an impulse response derived based on (3) will have poles in the right hand complex plane and will be unstable. A stable transfer function approximation that would allow for the CWT to be implemented as a filter can be realized by introducing a time shift (T) in (3) [24]. The introduced time shift would result in a delay in the output of the final filter implementation. This delay must be compensated to allow for the real-time operation of the algorithm.

The algorithm, modified to allow for a hardware implementation, has been shown in Fig. 3 and is partitioned into three main stages (Stages 1–3) and four routes (Routes A–D). A real-time averaging operation is performed in Route A by calculating the input signal envelope with a cutoff frequency of 0.16 Hz. The output of the envelope detector is then multiplied by a user set threshold (β). The multiplication block is subsequently followed by a constant delay of 0.1 s, added to compensate for the delay resulting from the CWT blocks placed in the following routes and the parallel signal processing nature of the algorithm. The normalization performed in Route A ensures that the spikes are identified later in the algorithm independent of changes in the EEG signal amplitude occurring between different patients or due to the quality of the electrodes. Routes B and C consist of the CWT approximations (C_5 and C_{20}). C_5 is at scale 0.025 ($T = 0.1$), while C_{20} is at scale 0.1[1] ($T = 0.4$). The comparisons of

[1]The algorithm has originally been implemented in MATLAB and, therefore, the analysis scale has been altered based on the sampling frequency (200 Hz) using: MATLAB scale = Wanted scale (a) × Sampling frequency.

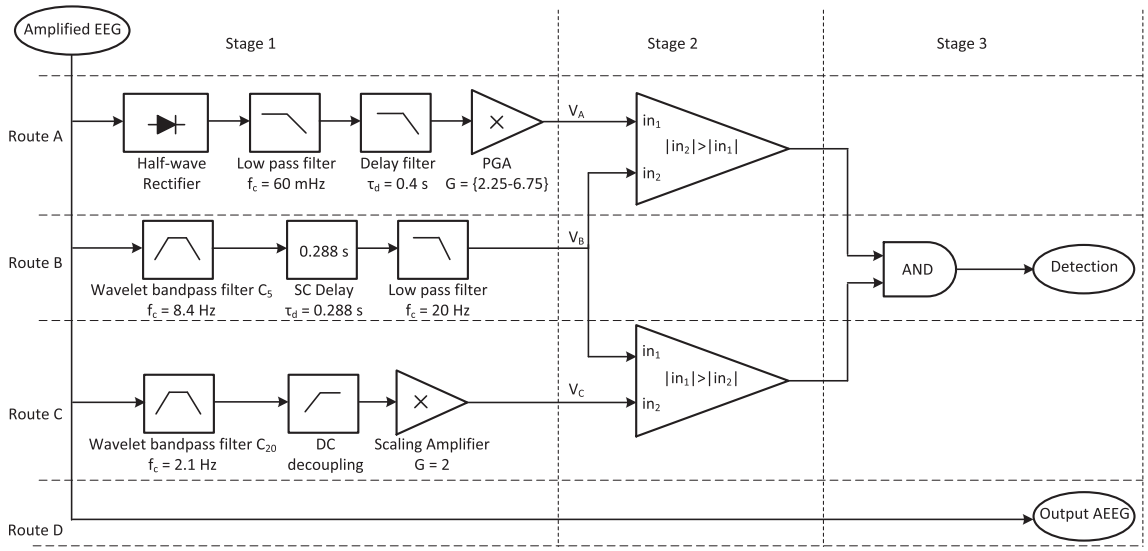

Fig. 4. Top level data reduction system architecture.

normalized wavelet powers performed in Stages 2 and 3 have been replaced with absolute value comparisons ($|C_5| > |z\beta|$ and $|C_5| > |C_{20}|$).

The largest amount of delay present in the algorithm results from the C_{20} wavelet operation ($T = 0.4$) and therefore, two 0.3 s delay blocks have been included in Stage 2 to equalize the total amount of delay present within the algorithm routes. The reader should note that the delay blocks have been placed after the comparison stage in Stage 2 as the analog or digital nature of the signals being processed has not been considered in the algorithm description of Fig. 3.

Finally, Route D delays the raw EEG input signal by 0.4 s so that the correct section of the signal corresponding to the detections is passed to the transmitter.

The algorithm is scalable in that a copy of the algorithm, when implemented in the form of an ASIC (Section III), will be incorporated in each channel of a WEEG unit. Furthermore, taking the union of the detection results of the algorithm copies will ensure that a single detection at the output of one of the channels results in the corresponding section of EEG data from all channels to be recorded prior to transmission. In response, a set period of the EEG signal before and after the detection will be recorded (the recording window), requiring a buffer memory to store the signal from before the detection for a duration of half the recording window (recording window/2). By using the algorithm, only the signals within the recording window are sent to the transmitter for transmission. Consequently, the overall amount of data to be transmitted is reduced. The algorithm achieves a sensitivity of 90% for a 50% reduction in transmitted data.

III. System Architecture

A number of top level specifications must be considered prior to examining the circuit level design strategy.

The dynamic range recommended by the IFCN for human interpretation of EEG signals is 72 dB with respect to a noise floor of 0.5 μV_{rms}. The data reduction algorithm has proven robust to dithering as its performance is not degraded for noise levels below 20 μV_{rms} [25]. Therefore, significantly relaxing the system dynamic range requirement from 72 dB down to 40 dB. The low dynamic range and low power requirements of our system allow for an analog design approach to be used in our system implementation [26].

As previously stated, $CP_t + NP_c$ must be smaller than the power consumed by the transmitter in case of no data reduction present. Considering a data reduction (C) of 50%, and P_t of 768 μW (lower bound of P_t), provides a power budget of 384 μW for all present data reduction stages. Assuming a channel count of 32 and reserving 50% of the mentioned power budget (192 μW) for buffering data before and after a detection will result in less than 6 μW of power available per channel for implementation of the data reduction system.

A top level block diagram showing the system architecture design has been shown in Fig. 4. The analog signal processing circuitry has been arranged in Stage 1. This has been followed by Stage 2 in which comparison operations are performed using two absolute value comparators operating in parallel and in real time. Stage 3 combines the outputs of the two comparators, using a simple two-input AND gate, to produce a final detection flag output.

A. Route A

Since full-wave rectifiers effectively calculate the absolute value of a given signal, perfect matching between both polarities is required in a circuit level implementation to maximize accuracy. This often leads to using more complex circuitry that would demand higher power consumption. As a result, a half-wave rectifier has been used within the implemented envelope detector. Signal rectification is performed, as shown in Fig. 5, using a comparator, and the following digital inverter that would either select V_{in} or a dc reference voltage (V_{ref}) to be passed on to the output. The switches, designed as minimum sized NMOS transistors, provide a low impedance path to the output while isolating V_{in} and V_{ref} from noise generated by

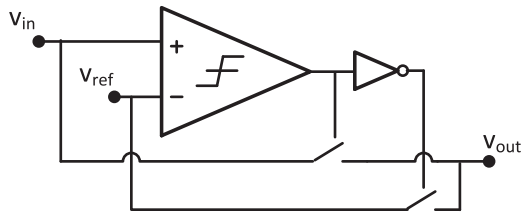

Fig. 5. Half-wave rectifier circuit topology adapted from [35].

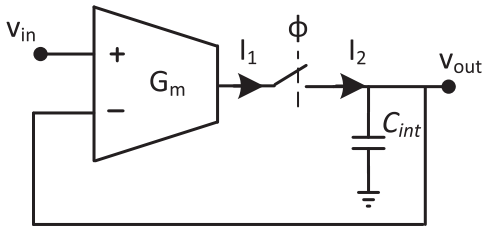

Fig. 6. Low-pass filter with a cutoff frequency proportional to the duty cycle of the clock signal (ϕ) [28].

the comparator and digital inverter. The rectifier achieves a dynamic range of 80 dB.

Replacing the full-wave rectifier in the envelope detector with a half-wave rectifier, without supplementary modifications to the system, can result in performance degradation. Half-wave rectifiers only pass the positive sections of the input signal to the output resulting in signal power loss. Furthermore, extra unwanted frequency components closer to the wanted near-dc terms, will be present at the output [27]. Assuming a single tone sine wave input at frequency f, the output of the full-wave rectifier will have frequency components including the dc term and even harmonics of the input signal. The half-wave rectifier output frequency content will, however, contain the dc term and input harmonics including f, requiring a lower cutoff frequency for the subsequent low-pass filter to separate the dc information.

As a result of the above-mentioned issues, the cutoff frequency of the low-pass filter following the half-wave rectifier in Fig. 4 has been set to 60 mHz (chosen empirically). An extra gain factor ($\times 2$) has also been incorporated into the following programmable gain amplifier (PGA) by modulating the user set thresholds to compensate for the signal power loss.

The low-cutoff frequency (60 mHz) of the low-pass filter is realized by continuously clocking the output of an OTA cell, as proposed in [28]. The filter operation principle has been shown in Fig. 6 and as can be seen, the OTA output current (I_1) can flow into the capacitor (C_{int}) only when the switch is closed. Assuming δ as the duty cycle of the clock signal (ϕ), the effective current flowing into C_{int} can be defined as

$$I_2 = \delta \times I_1. \tag{5}$$

The low-pass filter tolerates a maximum input signal amplitude of 140 mV_{pp} and has a dynamic range of 64 dB. A 128 Hz clock signal with a duty cycle of 1% has been used in this paper to set the filter cutoff frequency to 60 mHz.

The 0.4 s delay block following the filter has been created by cascading two first-order $\text{G}_\text{m}\text{C}$ low-pass filters. Group delay,

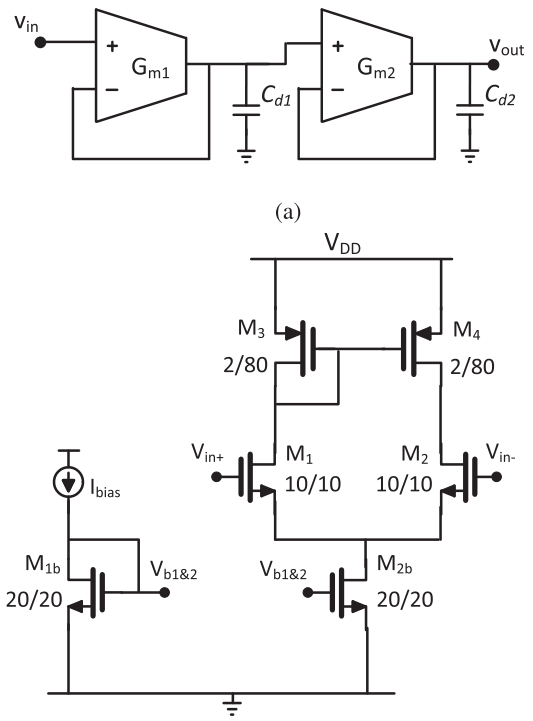

Fig. 7. 0.4 s $\text{G}_\text{m}\text{C}$ delay filter suitable for processing signals below 60 mHz, realized by cascading two single-stage low-pass filters. (a) Delay filter structure (b) OTA circuit topology.

which is a measure of the amount of phase distortion seen at the output of a filter as a function of frequency is defined as

$$\tau_g = -\frac{1}{360} \cdot \frac{d\phi}{df}. \tag{6}$$

A suitable delay filter must exhibit constant magnitude and a linear phase response with negative slope over the signal bandwidth.

Generally, a higher count of poles and zeros in the filter transfer function is required to create large delays for wideband input signals, resulting in more complex circuitry. However, since the input signal to the delay block in this paper is significantly band-limited (60 mHz), a delay filter with a smaller number of low-frequency poles can be utilized to generate the 0.4 s delay. Two $\text{G}_\text{m}\text{C}$ low-pass filters have been cascaded as shown in Fig. 7(a) to create an overall delay filter with a nearly constant group delay of 0.4 s with a variation of 0.5% over the 0 to 60 mHz bandwidth. The two single-stage OTAs ($G_{m1} - G_{m2}$), shown in Fig. 7(b), are biased with a current (I_{bias}) of 6.5 pA placing all transistors in the deep weak inversion region. Fairly large devices are used in the OTAs to improve matching. The parasitic capacitance introduced by these devices does not distort the delay filter bandwidth, which is much smaller than that of the individual OTAs. Two 20 pF integrated capacitors (C_{d1} and C_{d2}) have been used to place the cutoff frequency of the delay filter at 0.5 Hz. This circuit also removes any high-frequency artifacts resulting from the clock signal used in the low-pass filter preceding the delay filter.

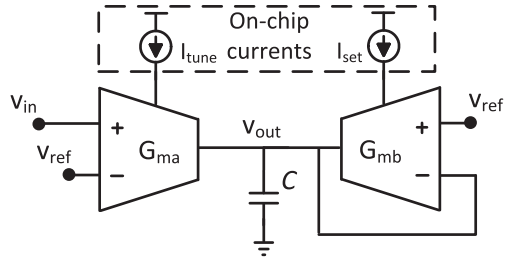

Fig. 8. Topology of PGA. Gain is set by the ratio of currents ($I_{\text{tune}}/I_{\text{set}}$). The two currents I_{tune} and I_{set} are provided by an on-chip current reference circuit.

The distortion introduced by the delay filter is minimized since the inputs to the OTAs used in this circuit closely follow each other for low-frequency signals. A total harmonic distortion of 1.01% was achieved for an input signal of 140 mV_{pp} at 500 mHz and this is reduced to 0.02% for an input signal with the same amplitude at 50 mHz. The inband noise was 25 μV_{rms} and 8.6 μV_{rms} integrated over the 1 to 500 mHz and 1 to 60 mHz bands, respectively. Taking the worst case figures for the maximum input signal and integrated noise of 140 mV_{pp} and 25 μV_{rms} results in a dynamic range of 66 dB for the delay filter.

The PGA following the delay filter consists of two single-stage OTAs ($G_{ma} - G_{mb}$), as shown in Fig. 8. The gain of the amplifier is set by the ratio of the biasing currents ($I_{\text{tune}}/I_{\text{set}}$), and must represent the user set threshold values (β). The β values are multiplied by a factor of 2 to compensate for signal power loss resulting from the half-wave rectifier in Fig. 4. Furthermore, an extra factor of 3.56 is incorporated into the new β values to correct for signal amplification resulting from the circuit level implementation of the CWT (C_5), as will be seen later in Section III-B. Since the values of β^2 originally varied between 0.1 and 0.9, the PGA gain settings must be programmable between 2.25 and 6.75. This is realized by setting the current I_{set} to 5 nA and turning I_{tune} between 11.25 and 33.75 nA. After deciding on the specific performance tradeoff between sensitivity and amount of data reduction, the two currents I_{tune} and I_{set} are generated on-chip using a current reference circuit, which has been described later in Section IV.

B. Route B

A 7th order $\text{G}_{\text{m}}\text{C}$ bandpass filter is used to approximate the CWT operation. Detailed analysis and design of the filter has been presented in [29]. A biasing current of 26.5 pA is used to set the center frequency of the C_5 filter in Route B to 8.4 Hz. The filter has a dynamic range 43 dB and input referred noise of 51 μV_{rms}, integrated over the 6–10 Hz passband.

The gain of the CWT is dependent on the analysis scale, as seen in the mathematical representation of (2). However, the bandpass filter approximation has a center frequency gain of approximately 0 dB, due to the LC ladder implementation. For the case of the C_5 filter, there is a factor of 3.56 attenuation between the center frequency gain of the implemented circuit and the ideal transfer function, together with a 180° phase shift. The negative sign is inconsequential since only the absolute value of the filter output will be used for comparison in Stage 2 of the system. However, the factor of 3.56 gain loss must be accounted for in the PGA gain settings of Route A.

The 0.3 s delay block following the C_5 wavelet filter must delay the filter output, which is strongly attenuated around 8.4 Hz, by almost three full cycles. Utilizing a continuous time delay filter to generate the 0.3 s delay is not appealing since such a filter will require 12 poles. The switched-capacitor (SC) delay circuit of [30] has been modified to be suitable for adaptation in this paper. A unity gain buffering stage is added between the C_5 filter and the SC delay circuit to isolate the filter output from the switching transients. The delay circuit operates by cascading multiple delay cells each consisting of two SC sections controlled by complementary clock signals ϕ_1 and ϕ_2 (see Fig. 9(a))

$$d = 2\big(1-D\big)T \tag{7}$$

where T and D are the clock period and duty cycle, respectively.

Offset voltages are generated at the output of each cell, due to mismatch between the specific currents of transistors M_1–M_4. The compounded effect of offset voltages will result in signal distortion at the delay circuit output. Therefore, the authors of [30] recommend placing an offset correction cell incorporating floating gate transistors, as shown in Fig. 9(b), within the delay line. Systematic offset from previous cells can be corrected by appropriately adjusting V_A and V_B. However, individual tuning of the offset correction cells in each delay circuit may not be a scalable solution. Furthermore, a significant loss of gain (−10.33 dB) has been reported in [30], due to the parasitic capacitance at the floating gate nodes in the offset correction cells.

An alternative solution for offset correction is to have dc blocking sections, as shown in Fig. 9(c), which can be placed intermediately within the delay line to reject the offset voltages. This modification does come at the cost of the added area required by the dc blocking circuitry. Each section is essentially a high-pass filter with a sub-Hz corner frequency, created using a 10 pF capacitor and a (0.4 /0.35 μm) PMOS transistor acting as a quasi-infinite resistor (M_{QIR}).

In this paper, the delay generated by the delay line is 0.288 s (32 cells). A low-pass filter ($f_c = 20$ Hz), placed after the delay line, reduces the distortion resulting from the clock signal frequency component and its harmonics.

C. Route C

The center frequency of the C_{20} filter, which has a structure identical to the C_5 filter, has been set to 2.1 Hz with a biasing current of 6.5 pA. A factor of two difference in mid-band gains of the C_5 and C_{20} filters must be present based on the ideal transfer functions. As previously mentioned, the circuit level implementation of the wavelet filters results in a mid-band gain of 0 dB for both C_5 and C_{20}. The output of the C_{20} filter has been scaled to compensate for the difference in gain using a non-inverting amplifier.

D. Stages 2 and 3

The use of full-wave rectifiers has been avoided in the absolute value offset-compensated comparators, shown in Fig. 10, by utilizing two normal comparators with reconfigured inputs and a XOR gate [31].

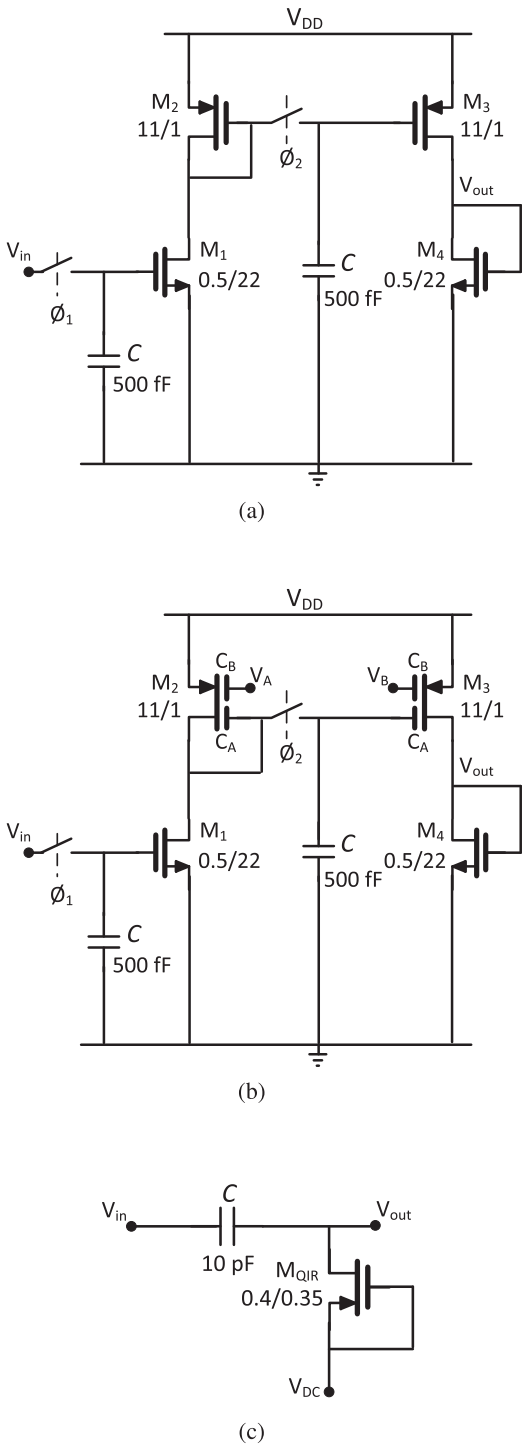

Fig. 9. SC delay circuit. (a) Circuit architecture of normal delay cell. (b) Circuit architecture of offset correction cell presented in [30]. (c) Proposed dc blocking section.

The output of the AND gate in Stage 3 represents the detection flag and will only turn to "VDD" when interictal activity is detected by the system (i.e., $|C_5| > |z\beta|$ and $|C_5| > |C_{20}|$).

IV. System Front-end and Biasing

The IA has been designed based on the topology of [32], achieving a mid-band gain of 39 dB and input referred noise of 2.7 μV_{rms} (integrated over 0.5–100 Hz).

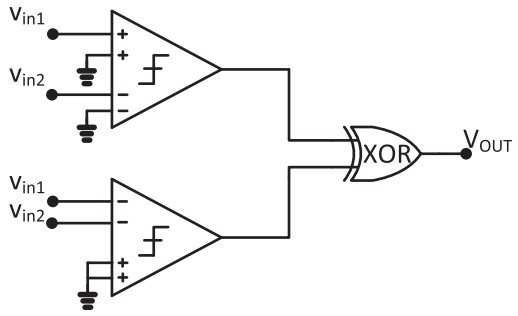

Fig. 10. Absolute value comparator performing a comparison between absolute values of the two input signals [31].

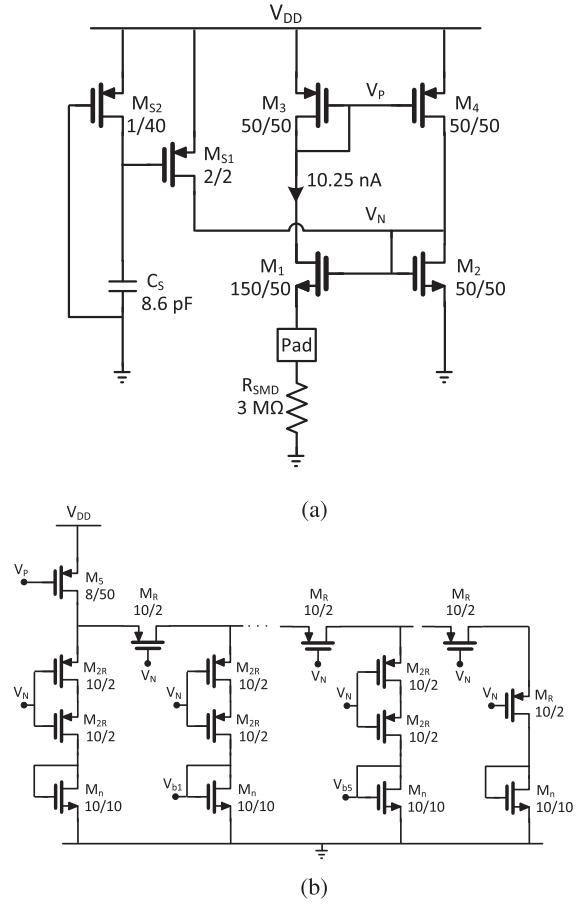

Fig. 11. Current reference. (a) Core and startup circuitry. (b) Splitter circuit.

The currents required by the system have been generated using a proportional-to-absolute temperature current reference circuit, shown in Fig. 11(a), and on-chip current scaling circuitry. The circuit generates a 10.25 nA reference current using an off-chip 3 MΩ surface mount resistor. The circuit obtains a correct operating point at startup with the help of the current injected by transistors M_{S1} and M_{S2}. The use of traditional current scaling circuitry to create the pA currents is not practical due to the large aspect ratio spread required. The $R-2R$ current splitting method reported in [33] and [34] (shown in Fig. 11(b)) has been utilized in six stages to produce the pA currents from a scaled down version of the reference current.

TABLE III
SUMMARY OF DATA USED FOR TESTING THE DATA REDUCTION SYSTEM PERFORMANCE

Patient	Age at test	Gender	Type of recording	Marked interictal events	Recording duration	T_{ev}(%)
0	Unknown	Unknown	fMRI/EEG	644	00:36:55	14.5
1	24	Male	Long term monitoring	49	03:58:15	0.2
2	47	Female	AEEG	7	02:00:11	0.04
3	33	Female	AEEG	52	06:00:33	0.12
4	51	Unknown	AEEG	12	04:00:22	0.04
5	23	Female	AEEG	11	04:00:22	0.04
6	44	Female	Routine EEG	0	00:46:19	0
7	43	Male	Routine EEG	2	00:18:30	0.09
8	46	Male	AEEG	26	02:00:11	0.18
9	45	Male	Long term monitoring	30	04:00:22	0.1
10	23	Female	AEEG	45	04:00:22	0.15
11	53	Female	AEEG	8	02:00:11	0.05
12	27	Female	Long term monitoring	0	02:00:11	0
13	21	Female	AEEG	12	02:00:12	0.08
15	33	Unknown	Routine EEG	1	00:10:53	0.07
19	Unknown	Unknown	AEEG	28	22:57:05	0.01
20	Unknown	Unknown	AEEG	15	22:06:23	0.01
21	Unknown	Unknown	AEEG	40	21:05:43	0.02
Total	-	-	-	982	104:03:00	0.13

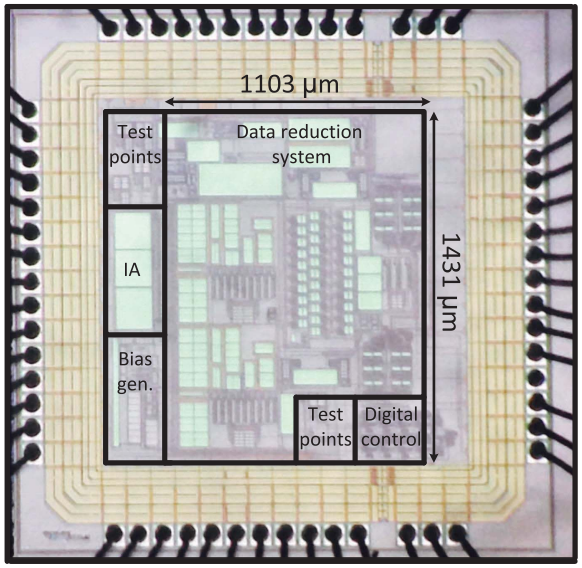

Fig. 12. Micrograph of fabricated chip.

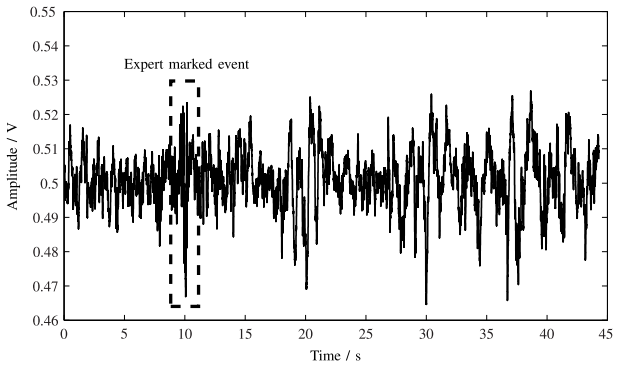

Fig. 13. Forty five seconds section of input EEG data processed by the system.

V. EXPERIMENTAL RESULTS

A. Chip Fabrication

The data reduction system has been fabricated using a 0.35 μm AMS, 2 poly, 4 metal CMOS process. The chip micrograph has been shown in Fig. 12. The active area consumed by the system is 1.57 mm^2.

The digital portion of the system has been restricted to the right side of the chip and the chip pad ring has been partitioned into two separate parts in order to isolate the sensitive analog circuitry from the noisy digital sections.

B. Test Setup And Measurements

Input signals to the chip have been generated by a National Instruments USB-6259 data acquisition board and the same device was used to collect the detection flag output together with analog intermediate testpoint signals V_A, V_B, and V_c in Fig. 4.

The data set used for testing the chip performance contained 982 interictal events in over 4 days of data from 18 patients. Table III summarizes the data set details per patient together with the number of marked events and total duration of events normalized by the recording duration (T_{ev}). The number of channels present in all recordings was not equal and, therefore, 10 channels common to all recordings have been selected to be processed by the chip. Marking of the interictal events was performed by an expert from the Epilepsy Society, U.K.

An illustration of the system behavior with 45 s of EEG signal containing an interictal event at the 10 s time mark is shown in Fig. 13. The EEG trace has been obtained from the data file belonging to channel F7 of patient 1. Measured outputs of the three intermediate test points V_A, V_B, and V_c have been shown in Fig. 14(a)–(c), respectively, and follow the

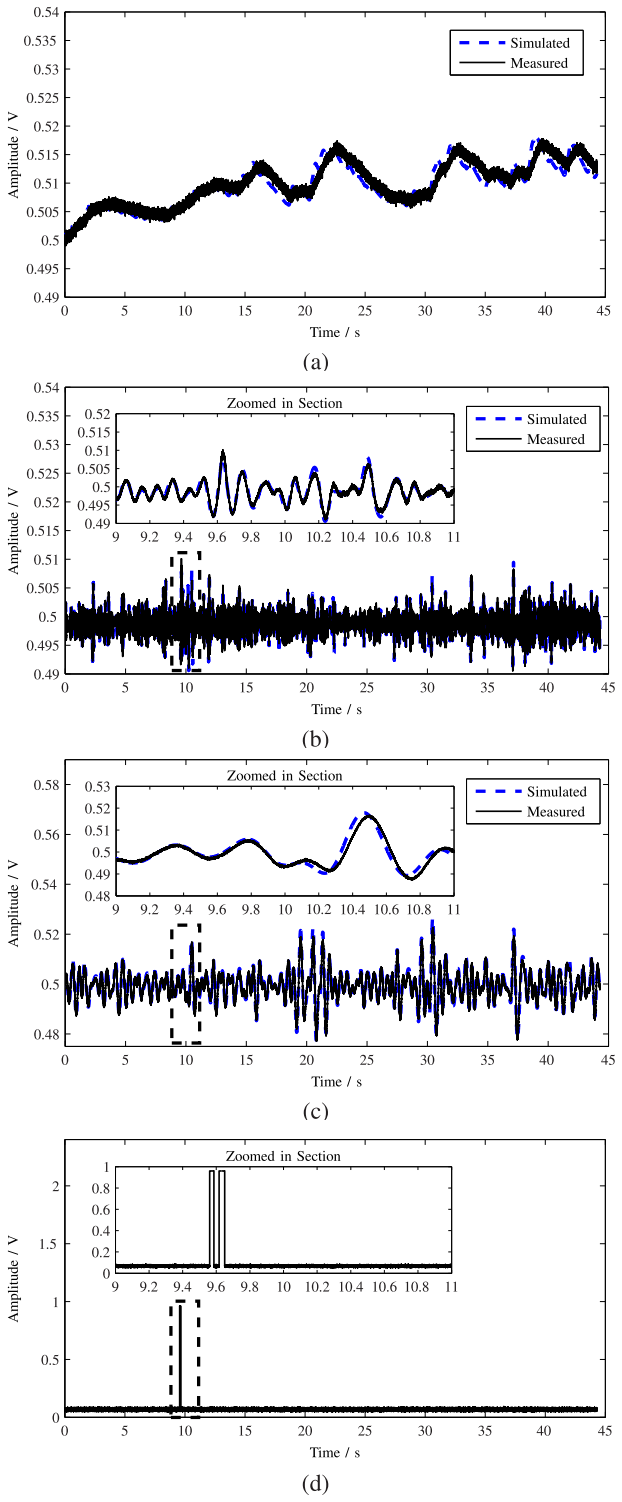

Fig. 14. System outputs in response to input EEG trace. (a) Output of Route A (V_A). (b) Output of Route B (V_B). (c) Output of Route C (V_c). (d) Decision flag output.

broad shape of the simulated results. As seen in Fig. 14(d), the state of the detection flag signal has changed twice from "low" to "high" around the 9.6 s time mark since the condition for an interictal event to be detected by the system (i.e., $|V_B| > |V_A|$ and $|V_B| > |V_c|$) has been satisfied.

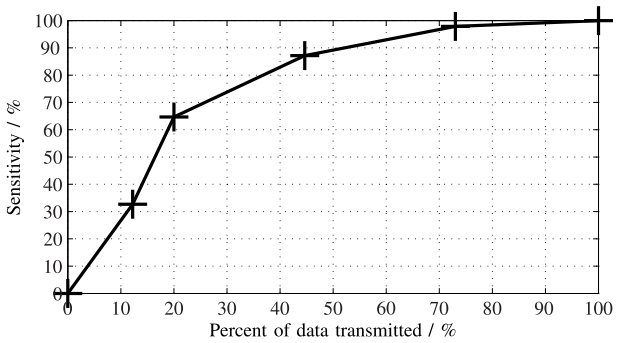

Fig. 15. System performance tradeoff curve showing the tradeoff between sensitivity and amount of transmitted data.

The total noise contributed by the data reduction system integrated over the algorithm operating band (referred to the IA input) is 1.5 μV_{rms}, which is inline with the noise specifications mentioned in Section III. The system noise is dominated by thermal noise components and only 1% of the total noise is attributed to flicker noise.

System performance has been evaluated using the Sensitivity and the percentage of data transmitted indices, to allow for direct comparison with the work of [16]. The sensitivity is the percentage of events that are correctly identified by the system and is calculated as

$$\text{Sensitivity} = \frac{\text{TP}}{\text{TP} + \text{FN}} \times 100\%. \tag{8}$$

In order to allow for direct comparison of the fabricated system performance with [16], an event detected by the system has been deemed a true positive (TP) if detected within a 2 s window of an expert marked event. Marked events left undetected by the system have been considered as false negatives (FN). The percentage of data transmitted has been calculated assuming a 5 s window of EEG data stored for transmission in response to a detected event. Higher sensitivity together with a lower percentage of data transmitted would indicate better system performance.

The performance indices have been calculated for individual records for each PGA gain setting and then combined to produce the curve of Fig. 15. A set of four tuning currents ($I_{\text{tune}} = \{16, 23, 28, 31.9\ \text{nA}\}$) have been used to produce the desired PGA gains, while keeping the testing process across the entire database tractable.

The data reduction system achieves a sensitivity of 87.17% for a percentage of data transmitted of 44.65%, as seen in Fig. 15. The area under the curve (AUC) is calculated to quantify the overall system performance and is found to be 0.774, a difference of 5.2% compared with the AUC of 0.816 achieved for the mathematical implementation of the data reduction algorithm.

The FPR achieved by the fabricated system corresponding to the four mentioned threshold values are 72%, 44%, 19.8%, and 12.8%. In comparison, the FPR corresponding to the same threshold values achieved by the mathematical implementation of the data reduction algorithm in MATLAB are 65.45%, 31.8%, 18.5%, and 12.3%. False positives are defined as

TABLE IV
SUMMARY OF SYSTEM PERFORMANCE

CMOS Process	0.35 μm	
Area	1.57 mm^2	
Supply Voltage	1.25 V	
Sensitivity	87%	
Data reduction	45%	
Current consumption (nA)	Envelope detector	76.5
	Delay filter	0.02
	PGA (I_{tune} = 23 nA)	54
	Wavelet filter (C_5)	0.24
	SC delay	360
	Low-pass filter (f_c = 20 Hz)	0.3
	Wavelet filter (C_{20})	0.06
	Scaling amplifier	30
	Absolute value comparator	113.5 ($\times$2)
	Digital circuitry	11
	Total	760

background EEG data that is incorrectly identified as interictal activity.

The system performance has been summarized in Table IV. The system consumes 760 nA from a supply voltage of 1.25 V, resulting in a power consumption figure of 950 nW. The power consumed by the IA and current generation circuitry has been excluded from this figure. As mentioned in Section II, the benefits of the reported system are independent of the power consumed by the IA. Furthermore, the WEEG unit would utilize one copy of the current generator to bias all copies of the system, regardless of the channel count. The power consumed by the data reduction system is only 16% of the available power budget of 6 μW, calculated in Section III.

VI. CONCLUSION

Developing truly WEEG monitoring devices with long operating lifetime is an open challenge due to the power hungry nature of wireless transmitters, which dominate the device power consumption. This paper discussed the design and results for a low-power scalable data reduction system that would benefit the realization of truly WEEG devices for monitoring of epilepsy. The system significantly reduces the amount of EEG data to be transmitted by selecting sections of data that likely contain interictal events for transmission, while rejecting background activity. The analog-based design approach allows for the system power consumption to be negligible compared with the power consumed by the transmitter in the case of continuous transmission, allowing for the operating lifetime of a WEEG device to be significantly extended. Furthermore, as a result of the data reduction performed by the system, the amount of data presented to the neurologists is also reduced, reducing the amount of time required for the diagnosis process.

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