

A 60-GHz Dual-Vector Doherty Beamformer

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Abstract—In this paper, we demonstrate a 60-GHz transmit beamformer implemented in 130-nm SiGe BiCMOS technology which includes a Doherty amplifier driven by a dual-vector phase rotator (DVR). In addition, a benchmarking circuit comprising another DVR followed by two class-AB amplifiers, each nearly identical to the carrier amplifier within the Doherty, is included which allows us to measure the Doherty improvement in terms of efficiency and output power over conventional approaches. The dual-vector Doherty element achieves 28-dB gain with an output 1-dB compression point of +16.7 dBm. A power-added efficiency (PAE) of 16.5% is realized at 1-dB compression, with 10.8% and 7% PAE at 3- and 6-dB back-off, respectively. A stand-alone Doherty amplifier achieves a 17.1-dBm output 1-dB compression point at 23.7% PAE and a 6-dB back-off PAE of 13%. The DVR performs the phase shifting for each phased-array element necessary for beamforming, as well as providing tunable amplitude balance and phase separation between input signals to the Doherty amplifier. This allows optimization of both linearity and efficiency profiles across frequency. The Doherty element is capable of generating full 360° phase shifts with 5-b accuracy having root-mean-squared errors less than 0.6 dB in amplitude and 6° in phase from 60 to 66 GHz.

Index Terms—60 GHz, millimeter-wave, phased array, transmitter, Doherty amplifier, phase shifter.

I. INTRODUCTION

PHASED arrays provide a way to overcome increased free-space path loss resulting from smaller antenna apertures at millimeter-wave (mm-wave) frequencies. In recent literature, transmit arrays for 60-GHz communications have used 16–32 elements [1]–[3] to achieve the effective isotropic radiated power (EIRP) needed to support multigigabit-per-second links. While these transmitters achieve impressive performance, the large number of elements translates into larger die size, larger package size, likely longer testing times, and thus, altogether higher cost.

The large number of transmit elements required is tied to the low power efficiency of mm-wave transmitter circuits. To see this, let us first define an array front-end power efficiency as $\eta_{bo} = P_{RF}/P_{DC,\text{array}}$, where P_{RF} is the RF power level necessary to achieve linear operation (i.e., backed off from 1-dB compression), and $P_{DC,\text{array}}$ is the power consumption of all array elements when operated at the backed-off condition.

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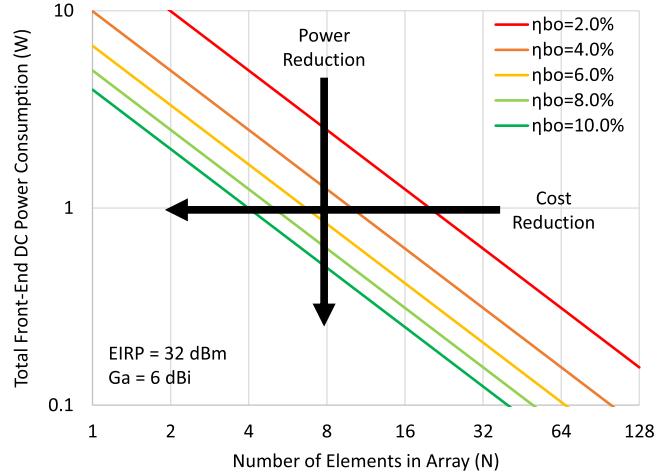


Fig. 1. Required front-end power consumption versus number of array elements for varying efficiencies to achieve 32-dBm EIRP using 6-dBi unit antennas. For fixed array size, improved efficiency results in reduced power consumption. For fixed power consumption, improved efficiency results in reduced array size.

The number of elements necessary to achieve a given EIRP for a given dc power budget is

$$N = \frac{EIRP}{\eta_{bo} \cdot G_a \cdot P_{DC,\text{array}}} \quad (1)$$

where G_a is the unit antenna gain. This tradeoff between power consumption, array size (cost), and efficiency is illustrated in Fig. 1 for EIRP of +32 dBm¹ and G_a of 6 dBi. For example, if $P_{DC,\text{array}}$ is constrained at 1.0 W for this EIRP and G_a , then 40 elements are required for $\eta_{bo} = 1\%$, reducing to 6 elements for $\eta_{bo} = 7\%$. As can be seen, improved back-off efficiency is therefore critical to realizing more cost-effective mm-wave phased-array transmitters.

Considerable attention has been devoted to developing PAs with high peak power-added efficiency (PAE), where state-of-the-art silicon 60-GHz PA designs have achieved output 1-dB compression points (P_{1dB}) of 11–20 dBm and a PAE at P_{1dB} from 17% to 27% [4]–[7]. These efficiencies drop considerably when backed off from P_{1dB} (e.g., a 3x reduction in PAE at 6-dB back-off is common [4]–[6]). Further reductions are seen when the power consumption of the full element is considered, including predrivers, RF phase shifters, and bias circuits. For example, the back-off power efficiencies of complete 60-GHz beamformers are estimated to be as low as 1%–3% at 6-dB back-off in [1]–[3].

¹An EIRP of 32 dBm corresponds to ranges of 35 m at 1.9 Gb/s and 10.6 m at 5.7 Gb/s. These assume 15-dB link margin, 12-dBi receive antenna gain, 1.76-GHz receive bandwidth, and OFDM symbols for 802.15.3c AV PHY

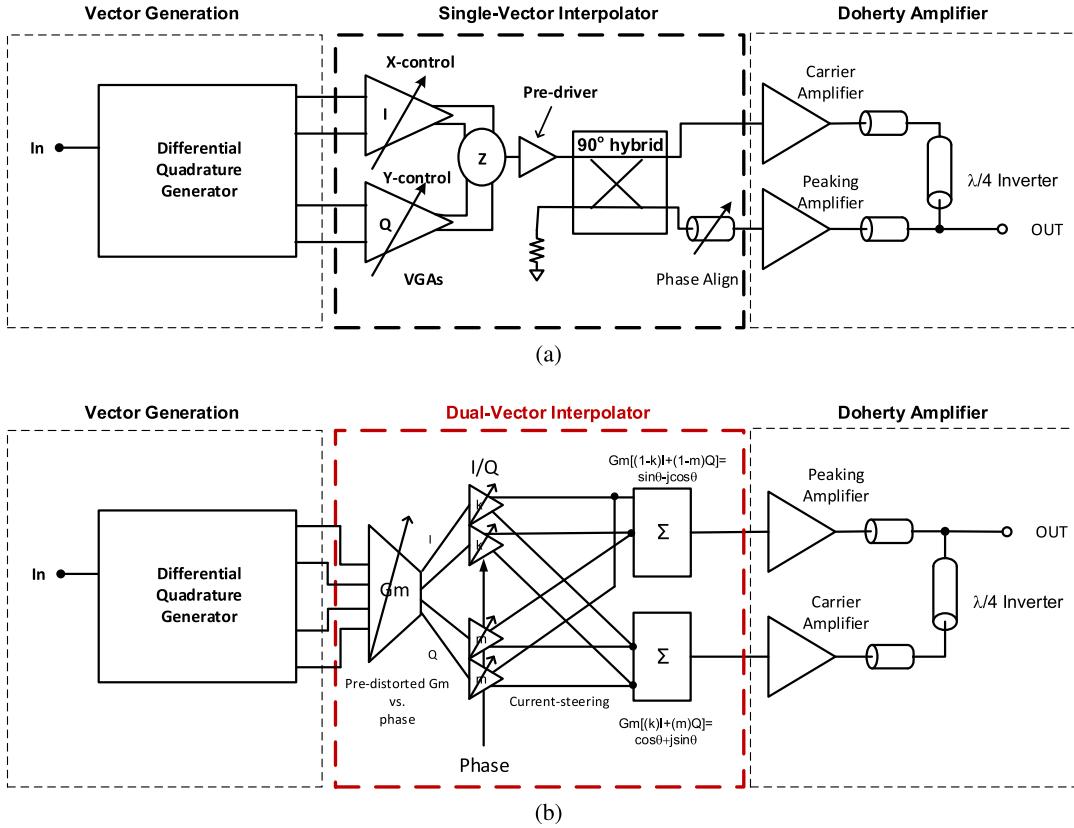


Fig. 2. (a) Block diagram of Doherty beamforming element with conventional architecture. (b) Block diagram of dual-vector Doherty beamformer.

It is critical to investigate topologies that specifically target improvement in back-off efficiency to realize phased arrays with fewer elements, such as envelope tracking (ET) [8]–[12], outphasing [13]–[15], and Doherty [16]. While both ET and outphasing have demonstrated improvements in back-off efficiency for stand-alone amplifiers, they present challenges for mm-wave phased-array application. Applying ET to 60-GHz phased-array systems would require considerable improvements to supply modulators to support gigabits/second data rates. Also, precise timing alignment between the RF and supply-modulator paths is necessary; otherwise, a large penalty in error-vector magnitude (EVM) will ensue [17]. The challenges faced in outphasing are similar. Two constant-envelope outphased baseband signals must be up-converted and distributed to each RF element, and locally phase shifted. All the while, the integrity of the outphasing angle must be preserved to avoid an EVM penalty (e.g., 6° error causing 20-dB degradation of EVM in [15]).

The Doherty topology avoids many of these issues while directly improving output power and efficiency—both metrics that lead to reductions in array size for a given EIRP. Doherty mm-wave structures in silicon have recently been investigated [18]–[20], with the best *amplifier-only* efficiency result demonstrated to date without the use of manual bias adjustments being 7% PAE at 6-dB back-off and 19.2-dBm $\text{oP}_{1\text{dB}}$ [19]. To the best of the authors' knowledge, no work has been completed which considers the modifications necessary and performance which can be achieved when Doherty amplifiers

are used within integrated phased arrays—the topic discussed herein.

II. DUAL-VECTOR DOHERTY BEAMFORMING ELEMENT

A. Element Topology

A block diagram of one approach to realize a Doherty-based beamforming element with a vector-interpolating phase shifter is shown in Fig. 2(a). In this topology, there exist two sets of RF power splitting and combining between the vector interpolator and Doherty amplifier. The redundant use of the “combine-and-split” approach is inefficient, requiring additional space, incurring loss, and ultimately leading to higher power consumption in surrounding amplifiers.

In Fig. 2(b), we present an alternative approach we refer to as a “dual-vector Doherty” beamformer. Here, the vector interpolating phase shifter and the following quadrature hybrid are replaced by a dual-vector phase rotator (DVR). The “combine-and-split” function has now been subsumed within the interpolator, saving both power and area. Furthermore, the DVR can provide adjustable phase and amplitude offset between the two signals driving the Doherty, allowing for adjustment of efficiency and/or linearity.

B. Dual-Vector Rotator

1) Theory: A common form of active phase shifting is vector interpolation, where two quadrature phase signals

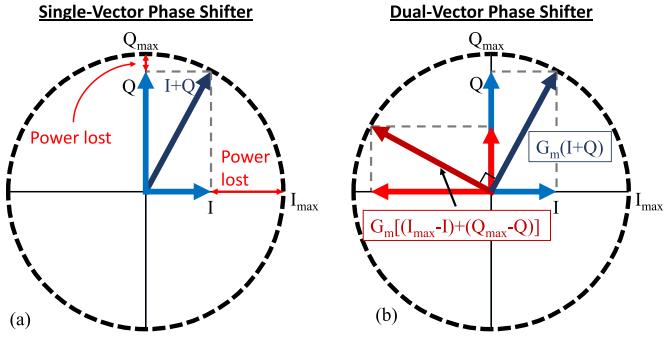


Fig. 3. Illustration of (a) traditional single-vector interpolation and (b) dual-vector interpolation.

(I and Q) with appropriate weightings are combined to produce the desired phase shift. This method is described by

$$\begin{aligned} A \cdot a(t) \cos(\omega t + \psi(t) - \theta) \\ = A \cos(\theta) \cdot \underbrace{a(t) \cos[\omega t + \psi(t)]}_{I(t)} \\ + A \sin(\theta) \cdot \underbrace{a(t) \sin[\omega t + \psi(t)]}_{Q(t)} \end{aligned} \quad (2)$$

where ω is the angular frequency of operation, A is the gain of the phase shifter, $a(t)$ and $\psi(t)$ are the modulated amplitude and phase of the signal, respectively, and θ is the desired phase shift. The weighting functions are typically realized with variable-gain amplifiers that can take the form of a variable transconductance as seen in [21] or a cross-coupled Gilbert cell topology as in [22]. As is shown in Fig. 3(a), RF power must be canceled from one or both vectors to generate the proper weighting. A DVR circuit instead uses the discarded RF power resulting from conventional vector interpolation to generate a second output, first introduced in [23]. This concept is illustrated in Fig. 3(b) where the weighting function is applied as an adjustable current division, achieved here through current steering. The power discarded on the I -axis in the single-vector implementation has instead been used as a component to form the second output in the dual-vector approach. Similarly, the power discarded on the Q -axis is also used in the formation of the second output. From these images, we see that the magnitude of discarded power and those forming the second output are unequal, pointing to a need for amplitude correction represented by a transconductance function (G_m).

To begin, we introduce the desired output vectors of the DVR as two phase-shifted currents in phase quadrature, described as follows:

$$\begin{aligned} I_{\text{out},A} &= g_m \cdot a(t) \cos[\omega t + \psi(t) - \theta] \\ &= g_m [\cos(\theta) \cdot I(t) + \sin(\theta) \cdot Q(t)] \end{aligned} \quad (3)$$

$$\begin{aligned} I_{\text{out},B} &= g_m \cdot a(t) \sin[\omega t + \psi(t) - \theta - \phi] \\ &= g_m [-\sin(\theta + \phi) \cdot I(t) + \cos(\theta + \phi) \cdot Q(t)] \end{aligned} \quad (4)$$

where g_m represents the transconductance in the circuit, $a(t)$ is an input voltage amplitude, ϕ represents the phase offset from quadrature, and $I(t)$, $Q(t)$, and θ are defined in (2).

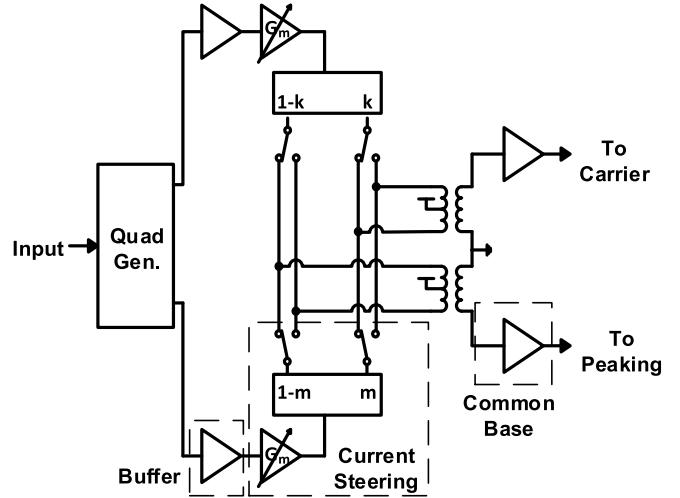


Fig. 4. Block diagram of the circuits used within the DVR.

Overall gain (A) of the circuit will be equal to g_m times the load impedance at the output of the rotator. Consider first the magnitude of the two weighting functions for $Q(t)$ described by $\sin(\theta)$ and $\cos(\theta + \phi)$ for outputs A and B, respectively. The addition of these two functions results in a value that is not constant for all θ and ϕ meaning that current steering alone cannot generate both weightings simultaneously (since the sum of both currents in current division must be constant). Therefore, a two-stage approach of amplitude predistortion and current steering is necessary to equalize the separate outputs' magnitudes across each phase setting. Replacing weighting functions in (3) and (4) with these new functions results in

$$I_{\text{out},A} = G_{mi} \cdot k \cdot [\pm I(t)] + G_{mq} \cdot m \cdot [\pm Q(t)] \quad (5)$$

$$I_{\text{out},B} = G_{mi} \cdot (1 - k) \cdot [\pm I(t)] + G_{mq} \cdot (1 - m) \cdot [\pm Q(t)]. \quad (6)$$

Here, $G_{mi/q}$ represents an amplitude predistortion

$$G_{mi}(\theta, \phi) = g_m (|\cos(\theta)| + |\sin(\theta + \phi)|) \quad (7)$$

$$G_{mq}(\theta, \phi) = g_m (|\cos(\theta + \phi)| + |\sin(\theta)|) \quad (8)$$

and k and m represent current steering functions

$$k(\theta, \phi) = \frac{|\cos(\theta)|}{|\cos(\theta)| + |\sin(\theta + \phi)|} \quad (9)$$

$$m(\theta, \phi) = \frac{|\sin(\theta)|}{|\cos(\theta + \phi)| + |\sin(\theta)|}. \quad (10)$$

From these, we see that the two outputs are both phase shifted by θ with a nominally quadrature relationship, but can be phase offset from this by ϕ through control of the prescaling and current-steering functions. Note that absolute values are required above since these predistortion and current-steering functions apply weightings which repeat across all four quadrants. Sign switches are then used to select the desired quadrant, i.e., by inverting the $I(t)$ and/or $Q(t)$ signals, as indicated in (6) and (6).

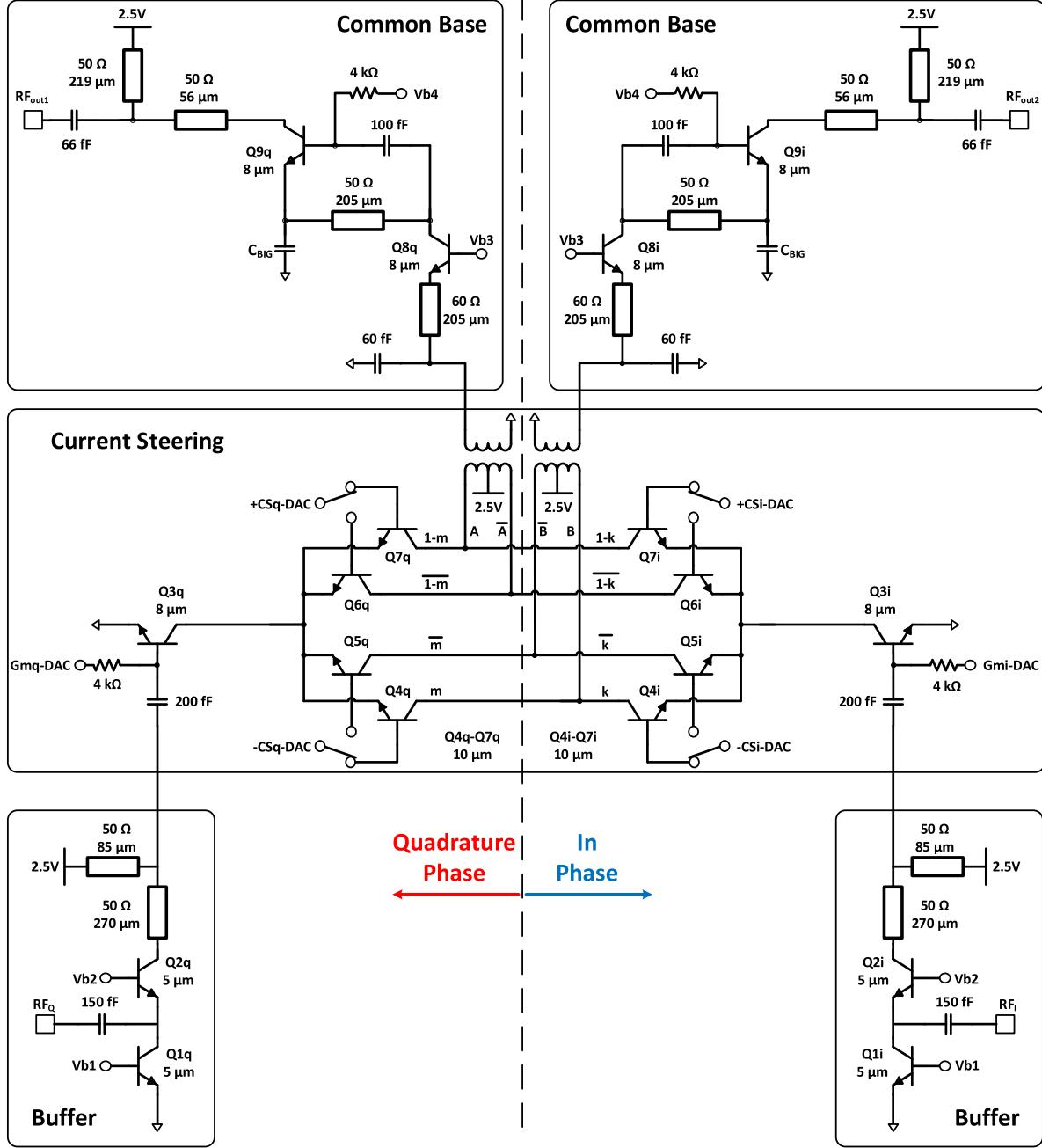


Fig. 5. Schematic of the DVR circuit with key blocks outlined.

2) *DVR Circuit Design:* A block diagram of the DVR is shown in Fig. 4, and the circuit details are provided in Fig. 5. Typical of most vector interpolators, the input signal is initially divided into in-phase and quadrature components. A Lange coupler is chosen for this task due to its compact size at 60 GHz in comparison with other topologies, such as the branch-line coupler. The hybrid is shown in Fig. 6 and was simulated in HFSS [24]. The total length of the coupling section is 575 μm , linewidth is 2 μm , and line spacing is 4 μm . The coupled lines are realized in the top metal layer (AM), whereas the ground plane is implemented in metal 1 (M1). HFSS simulations predict <0.6-dB insertion loss, <0.1-dB amplitude variation, and an 87° phase difference between both

outputs from 57 to 66 GHz. To maintain quadrature accuracy, two common-base buffers load the through and coupled ports, presenting a broadband 50- Ω load to the Lange coupler. The buffer is designed to consume minimal power, biased to draw 1 mA of current with transistors sized appropriately to yield an input impedance of 50 Ω .

A current-steering cell follows the buffer, including a variable G_m and a switchable current division. All adjustments related to predistortion and current steering are generated using current-based digital-to-analog converters (DACs). The G_m of transistor Q3 is set by a 4-b DAC realizing a discrete version of the pre-distortion functions described in (7) and (8). Portions of the in-phase current, k , and quadrature-phase current, m , are

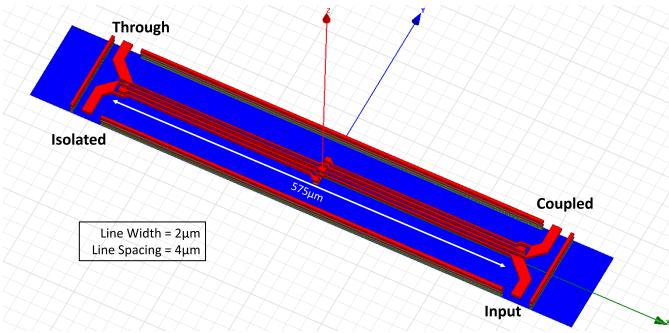


Fig. 6. Illustration of the 3-D view of the folded Lange coupler used to generate the two quadrature signals at the input of the DVR. For EM simulations, the ground plane has been simplified to a solid sheet, whereas in the actual structure, the ground plane is slotted.

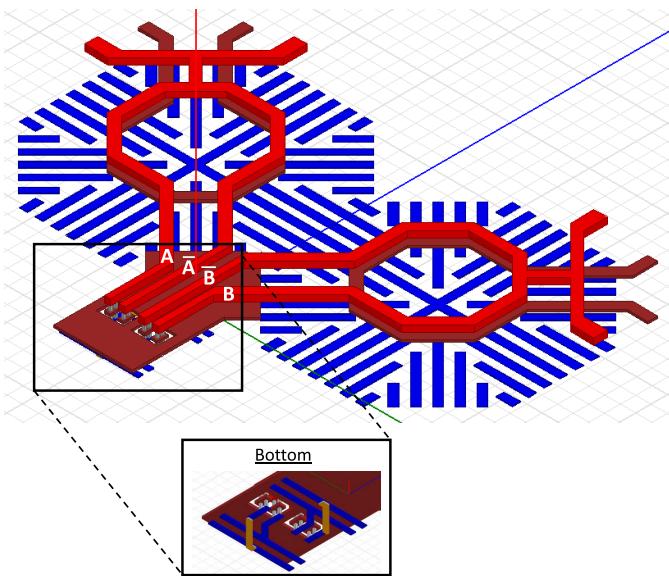


Fig. 7. Illustration of the 3-D view of the current combing node at the output of the current steering and the switchable transformers. The bottom view shows where currents from the in-phase and quadrature-phase halves are combined using inverted transmission line structures.

then steered to one output with the rest, $(1 - k)$ and $(1 - m)$, going to the second. Functions k and m given in (10) and (10) are realized using 5-b DACs to generate the differential bias voltage with a 6th bit for choosing the sign of I or Q . This sign bit determines whether or not to steer weighted I and Q currents into the positive or negative terminal of the transformer, allowing full 360° phase shifts. By generating the in-phase and quadrature-phase compliments in this manner, the number of transistors in the current-steering circuit is halved over that in [23] (from 16 to 8 transistors), leading to simplifications in layout and thus a substantial reduction in parasitic capacitance. The structure used to realize this technique is shown in Fig. 7.

The current-combination nodes located between the current steering and switchable transformer are designed with inverted microstrip transmission lines, where the signal is located beneath the ground plane. These inverted transmission lines combine the in-phase and quadrature-phase currents to

form outputs A , \bar{A} , B , and \bar{B} . To maintain the quadrature relationships between these nodes, the centers of these lines are tapped and fed upward through a hole in the ground plane to a noninverted microstrip transmission line which connects to the appropriate terminal of the transformer (as shown in the inset of Fig. 7). Symmetric routing with equal-length lines is used to maintain the quadrature phase relationship all the way to the Doherty input.

The switchable transformer is loaded by a common-base amplifier on the unbalanced port presenting a low impedance for the current combination node necessary for linear addition of the in- and quadrature-phase currents. A low input impedance allows the currents from both the in- and quadrature-phase halves to combine linearly. In an ideal scenario, the output impedance of both halves of the current steering cell would be infinite, resulting in current flowing only into the external load. This is not the case, especially at mm-wave, where the transistor's output impedance due to parasitics can be of comparable magnitude to the load, which in turn leads to part of the current flowing into the opposing side. The output impedance changes as a function of the phase setting as a result of the transistor's changing dc collector current. Combining these signals into a low-impedance load helps to minimize these errors.

The common-base amplifier is followed by an additional common-emitter amplifier which is stacked on top and reuses the same dc current. Use of two output amplifiers allows the resonant frequency of each to be tuned for different frequencies, yielding a wider 3-dB bandwidth of operation ranging from 53 to 69 GHz in simulation. The DVR output P_{1dB} is simulated to be 0 dBm, which is designed to be 3-dB higher than the input P_{1dB} of the Doherty amplifier.

3) Benchmarking of Dual-Vector Doherty Element: The use of a DVR can provide two nominally quadrature phase-shifted output vectors for the power consumption and area overhead of a single phase shifter. To test this claim, the authors have compared three approaches for Doherty beamforming in [23] for a 28-GHz transmit chain. Specifically, using transistor-level simulations in SiGe 8HP, we compared the following: 1) the use of the dual-vector rotator; 2) a single-vector rotator followed by a quadrature splitter for Doherty drive; and 3) two single-vector rotators for providing quadrature phase-shifted signals to the carrier and peaking amplifiers individually. For this comparison, each option is designed for the same output P_{1dB} to properly drive the PA. The results are found in [23, Table 1], and summarized here. The DVR approach required 0.45 mm² and 52.5 mW; the single phase shifter with quadrature splitter required 51 mW and 0.44 mm²; the two phase shifter approach required 72 mW and 1.17 mm². From this, we see that the DVR has comparable power and area to a single phase-shifter solution while providing adjustable output vectors and is therefore an excellent candidate for Doherty beamforming.

C. Doherty Amplifier

The overall Doherty is designed to achieve a +17-dBm P_{1dB} , with saturated output power very close to P_{1dB} .

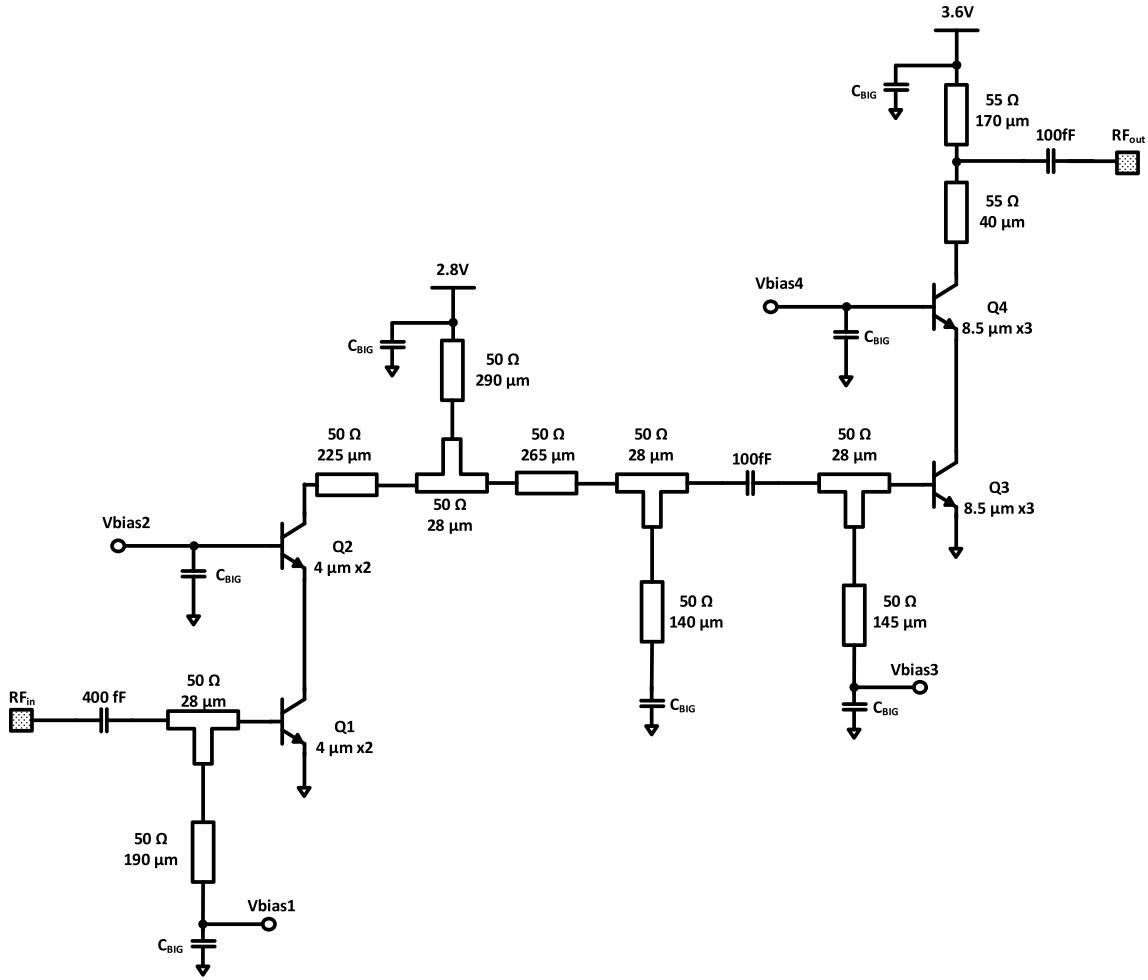


Fig. 8. Schematic of the carrier path of the Doherty amplifier.

Two-stage amplifiers are used for both the carrier and peaking amplifier paths to realize the Doherty operation. Two-stage designs result in high gain and high reverse isolation, and relax the output power requirements of the preceding DVR circuit. Identical transistor sizes and nearly identical matching networks are used for both paths, with the main difference being the output match of either driver stage. The symmetry of these designs helps to minimize parasitic mismatch between the paths that can result in a misalignment in phase of the RF currents at the output combination node. Both, however, must be biased in different regions of operation to achieve Doherty operation. The carrier amplifier is biased in a class-AB region, whereas the peaking amplifier is biased in class-C. Differences in these bias conditions will impact the phase response through each path requiring that the input signals be driven at a phase offset from the nominal 90°. In this design, simulation indicated that optimal performance occurs when the two paths are driven with a phase separation of 60°. Through the use of the DVR circuit, this phase separation is easily achievable and can be tuned to compensate for any additional mismatch between the simulated devices and physical hardware.

Both stages of the carrier PA use a cascode topology with differing device sizes as shown in Fig. 8.

Three n-p-n transistors connected in parallel are used for the carrier's driver stage with device sizes chosen such that sufficient RF current is generated to realize a +14-dBm $P_{1\text{dB}}$. Similarly, the predriver stage uses two n-p-n transistors in parallel with reduced size, as marked. An interstage matching network consisting of alternating series and shunt transmission lines (TL1–TL4) is used to transform the low input impedance at the driver to the high output impedance of the predriver. This method of matching yields a wider bandwidth response in comparison with a simple L-type matching network. The driver and predriver stages of the carrier amplifier are biased with current densities of 0.4 and 0.22 mA/ μm , respectively. Based upon simulated load-pull analysis, peak efficiency is achieved at 6-dB back-off when the carrier amplifier is loaded with 60 Ω . This impedance is provided through the quarter-wave transformer.

The peaking PA follows the same architecture as the carrier but with changes to the bias settings and to the output matching network to present a high impedance at the power combining node when off. The driver and predriver stages of the peaking PA are operated with current densities of 0.18 and 0.1 mA/ μm , respectively, such that the devices conduct low current at backed-off power levels. However, some conduction still

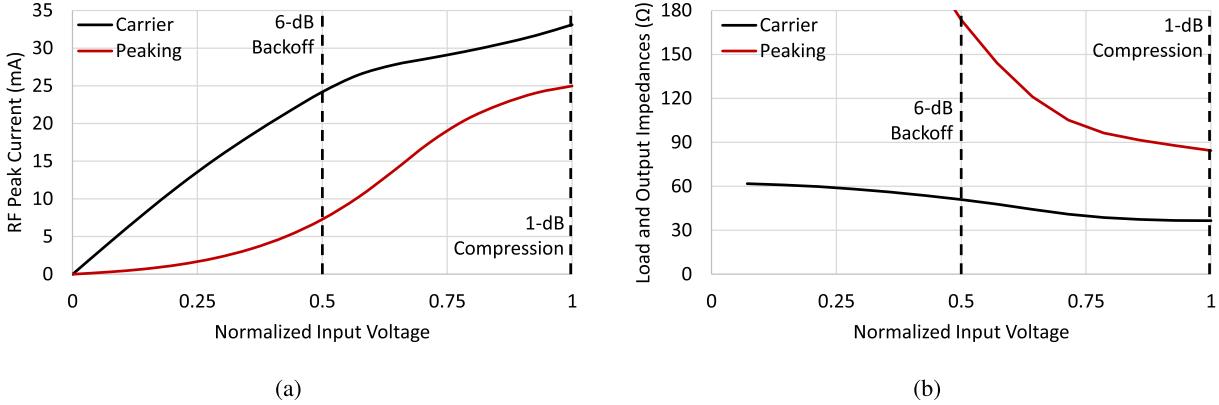


Fig. 9. Simulated large-signal results of the Doherty amplifier as a function of the normalized RF input voltage at 60 GHz. (a) Peak RF currents output from both the carrier and peaking amplifiers. (b) Load modulation on the carrier amplifier and output impedance of the peaking amplifier.

occurs at back-off, limited by the need to avoid excessive gain expansion at power levels near $P_{1\text{dB}}$. The output impedance of the peaking PA is increased using a shunt-L series-C network to approximately $220\ \Omega$ for very low input power levels. Under ideal circumstances, the peaking PA would appear as an open circuit for low input powers; however, this is limited by the finite quality factor of the output transmission-line stub.

The carrier and peaking amplifier outputs are combined using a quarter-wave transformer following the topology shown in Fig. 2(b). The transformer has a characteristic impedance of $55\ \Omega$ and an insertion loss of 0.25 dB. Note that it is possible to realize a more compact power combiner using a transformer, as demonstrated in [20].

The load-modulated impedance response of the Doherty structure can be predicted with the help of theory presented in [25]. Namely, the impedance presented to the carrier amplifier (Z_{carrier}) can be expressed as

$$Z_{\text{carrier}} = \frac{Z_m^2}{R_L \parallel R_{\text{peaking}}} - Z_m \left| \frac{i_{\text{peaking}}}{i_{\text{carrier}}} \right| \quad (11)$$

where Z_m is the characteristic impedance of the quarter-wave transformer, R_{peaking} is the output impedance of the peaking amplifier ($220\ \Omega$), R_L is the $50\text{-}\Omega$ load impedance, and i_{peaking} and i_{carrier} are the carrier and peaking amplifier currents, assumed to be 90° out of phase. The simulated current magnitudes of the carrier and peaking amplifiers are presented in Fig. 9(a) as a function of normalized input voltage for the dc current densities indicated previously. Clearly, the peaking amplifier does not exhibit an abrupt conduction at 6-dB back-off. Instead, a gradual conduction is used to avoid excessive gain expansion in the overall Doherty response. For our design, the peaking amplifier is designed to conduct about 30% of the carrier amplifier current at 6-dB back-off, increasing to about 75% at 1-dB compression. Using (11), we can thus calculate Z_{carrier} to be approximately $57\ \Omega$ at 6-dB back-off, decreasing to $33\ \Omega$ at 1-dB compression. These correspond to the preferred loading conditions for our carrier amplifier obtained from load-pull analysis.

To validate this impedance response, we performed a large-signal simulation on the full Doherty amplifier [block diagram shown in Fig. 2(b)], including the carrier amplifier, peaking amplifier, output transformer, and output load. The simulated

large-signal impedances looking into the quarter-wave transformer and looking into the peaking amplifier are plotted in Fig. 9(b) as a function of the normalized input voltage. These impedances are obtained by taking the ratio of RF voltage to RF current (flowing in either amplifier) at the output of the carrier and peaking amplifiers using periodic steady-state analysis.

From this plot, we see that the carrier is presented with a load impedance of about $55\ \Omega$ at 6-dB back-off and modulated down to $35\ \Omega$ at 1-dB compression. Also, the peaking amplifier presents an active impedance much larger than the $50\text{-}\Omega$ load at 6-dB back-off but cannot be represented by an ideal open circuit. This results in a portion of the power generated by the carrier being delivered to the output of the peaking amplifier for low power levels, thus reducing efficiency at backed-off power levels in comparison with ideal Doherty operation. The efficiency at 6-dB back-off is no longer set by the carrier alone but rather by a weighted average of both the carrier and peaking amplifiers' efficiency which is determined by the ratio of their current contributions to the load. This results in a deviation from the sharp peak in efficiency at 6-dB back-off for the ideal Doherty response. Instead, the efficiency now degrades at a slower rate for higher levels of back-off, but still results in improved back-off efficiency when compared with the stand-alone carrier amplifier response.

III. ARRAY IMPLEMENTATION AND MEASUREMENTS

A three-element 60-GHz phased array was designed in GlobalFoundries 130-nm SiGe BiCMOS 8HP technology. The array targets a 1-dB bandwidth of operation from 57 to 66 GHz. A block diagram of this array is shown in Fig. 10, and a die micrograph is shown in Fig. 11. The total area of the chip, including pads, is $1.6 \times 1.9\ \text{mm}^2$, and the area of one dual-vector Doherty element is $0.8 \times 1.2\ \text{mm}^2$. In this array, two DVR circuits are included, driven through an input Wilkinson splitter. One DVR is used to drive a Doherty amplifier where that Doherty amplifier includes both a carrier and peaking amplifier whose outputs are combined using a quarter-wave transformer, as indicated in Fig. 10. A second DVR drives two independent single-path PAs, which are each replicas of the carrier amplifier in the Doherty path. Including the two single-path PAs enables an accurate benchmarking of

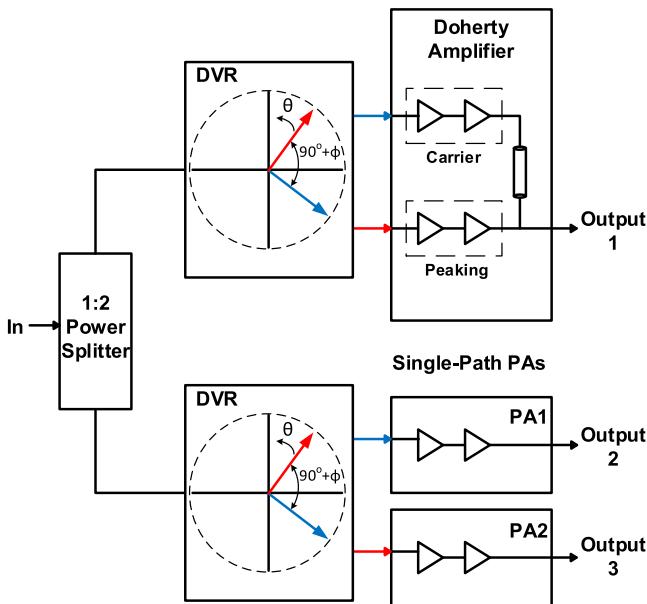


Fig. 10. Block diagram of the 60-GHz phased array consisting of a Doherty PA and two conventional class-AB PAs both driven by DVR circuits.

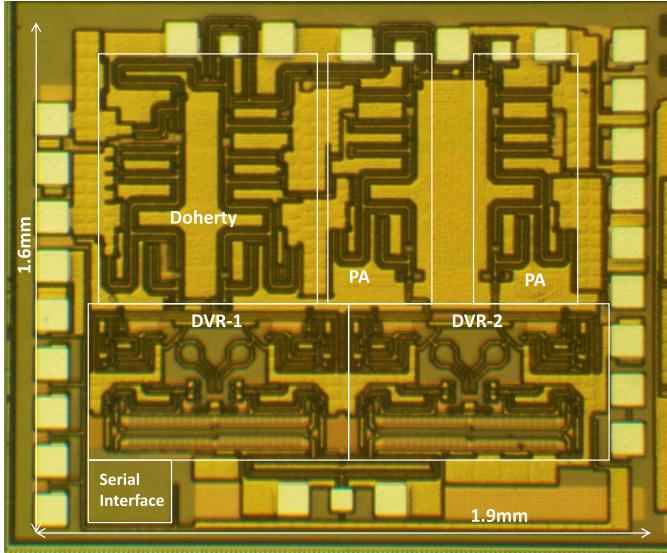


Fig. 11. Die photo of the dual-vector Doherty array.

the Doherty versus a conventional PA in the same process for the same bias conditions, as well as providing a means to measure the amplitude and phase responses of the DVR.

Five chip samples were measured at room temperature by wafer probing and all achieve comparable performance. S-parameter measurements and amplitude-modulation to phase-modulation (AM-PM) measurements are taken with an Agilent two-port Agilent E8361C network analyzer. Swept-power measurements are taken with an Agilent E8257D signal generator providing the input and an Agilent N1913A power meter and an Agilent N8488A power sensor for the output. Finally, third-order intermodulation (IM3) measurements are taken using a Rohde and Schwarz FSUP-43 signal-source analyzer with a V-band harmonic mixer.

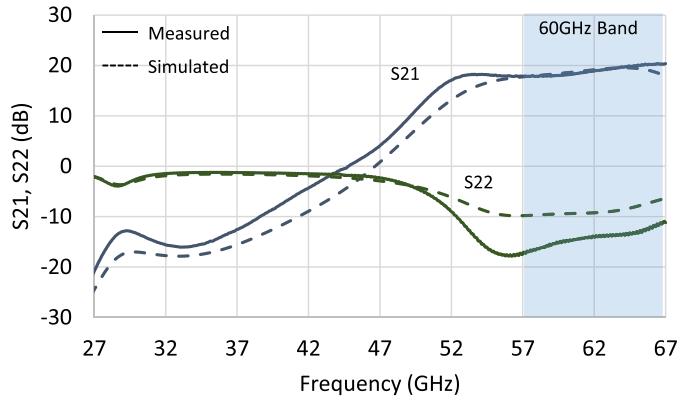


Fig. 12. Measured S-parameters of the Doherty amplifier breakout with input signals generated by a Lange coupler.

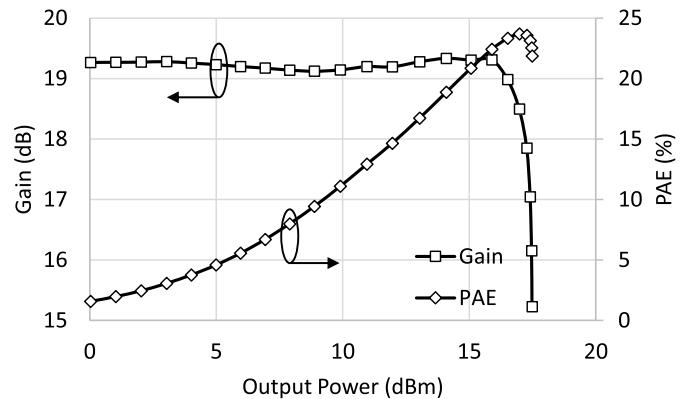


Fig. 13. Measured swept power performance of the Doherty amplifier breakout with input signals generated by a Lange coupler.

A. Doherty Amplifier Breakout Results

A stand-alone break-out circuit for the Doherty amplifier was implemented and measured using the same Lange coupler from the DVR for generating the quadrature input signals. The measured and simulated s-parameters of the Doherty breakout agree well and are presented in Fig. 12. The measured response achieves a 3-dB bandwidth between 53 and 67 GHz with an average gain of 19 dB. Some additional peaks in the gain response occur near 52 and 67 GHz as a result of the improved output match compared with simulation.

The swept-power response of the stand-alone Doherty amplifier is shown in Fig. 13 indicating an output-referred $P_{1\text{dB}}$ ($\circ P_{1\text{dB}}$) of +17.1 dBm. Peak PAE is 23.7%, and the 6-dB back-off PAE is 13% at 62 GHz. For power levels below $P_{1\text{dB}}$, the gain response exhibits less than 0.3-dB variation through the combined gain compression of the carrier amplifier and gain expansion of the peaking amplifier. Although the ideal Doherty back-off efficiency peak is not present, for reasons described earlier, back-off efficiency is still improved.

Table I compares the performance of our Doherty with recently published results. To the best of the authors' knowledge, these results represent the best to-date in 6-dB back-off efficiency for the 60-GHz band in silicon for amplifiers which do not use manual bias adjustment as a function of input power. The 6-dB back-off efficiency for the Doherty amplifier presented here demonstrates a four to seven percentage-point

TABLE I
COMPARISON OF HIGH-EFFICIENCY mm-WAVE POWER AMPLIFIERS IN SILICON

Reference	Technology	Architecture	Freq. (GHz)	$\text{oP}_{1\text{dB}}$ (dBm)	PAE @ $P_{1\text{dB}}$	PAE @ 6-dB OBO	Gain (dB)	Area (mm ²)
This Work	130-nm SiGe BiCMOS	Doherty	62	17.1	23.7%	13%	19	0.6
[7] Larie, ISSCC'15	28-nm CMOS	Transformer Based	60	18.2	21%	11%**	15.4	0.16
[20] Kaymaksut, TMTT'15	40-nm CMOS	Doherty	72	19.2	12.4%	7%	18.7	0.19
[6] Kulkarni, ISSCC'15	40-nm CMOS	Push-Pull	60	13.9	18.9%	7%*	22.4	0.08
[28] Moret, SiRF'15	65-nm CMOS	1-stage Cascode	57	11	11.5%*	8%*	14	0.4
[19] Agah, JSSC'13 [#]	45-nm SOI	Doherty, Manual Bias [#]	45	17**	20%**	21%***, #	8	0.45***
[29] Zhao, JSSC'13	40-nm CMOS	Class-AB Dual Mode	60	13.8	21.6%	7%*	17	0.074
[5] Ogunnika, RFIC'13	32-nm CMOS	2-stage	60	10.9*	27%*	8%*	10	0.6***
[15] D. Zhao, JSSC'12	40-nm CMOS	Outphasing	60	15.6**	25%**	8%*	15	0.33
[4] Y. Zhao, RFIC'11	130-nm SiGe BiCMOS	3-stage	60	19.9	17.5%*	6%*	20.5*	0.25
[30] Chen, ISSCC'10	65-nm CMOS	Transformer Based	60	15	6.5%*	1.5%*	20.3	0.28***
[31] Siligaris, JSSC'10	65-nm SOI	2-stage	60	12.7	22%*	8%*	16	0.57***
[32] Law, ISSCC'10	90-nm SOI	4-way Power Combined	60	18.2	13%*	11%*	20.6	1.75***

* Estimated from paper/plots

** Reference to P_{sat}

***includes pads

Peaking amplifier bias is manually adjusted across input powers

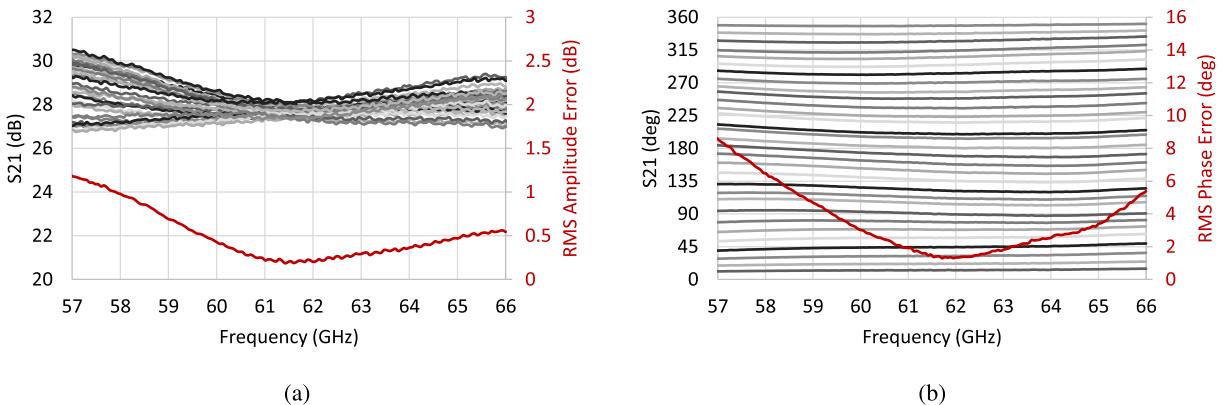


Fig. 14. Measured small signal (a) gain and (b) phase responses over 32 phase settings for the Dual-Vector Doherty element, when rotator is calibrated for 62-GHz operation.

improvement over most other reported power amplifiers with the exception of [7] and [19]. One key difference is that our Doherty amplifier includes a predriver stage to lower the input-referred $P_{1\text{dB}}$ ($iP_{1\text{dB}}$) to -3 dBm to align with the $\text{oP}_{1\text{dB}}$ of the preceding DVR stage. The works presented in [7] and [19] demonstrate an $iP_{1\text{dB}}$ of +3.8 and +10 dBm, respectively, which will require the preceding stage to generate higher RF output powers and reduce the efficiency of the transmit chain. Also, the work presented in [19] implements a manual bias adjustment for different power levels. While this leads to large

improvements in efficiency for backed-off power levels, the ripple in the gain response can vary between 1 and 3 dB as a function of input power and the impact on linearity is uncertain.

B. Small-Signal Results for Array Elements

The DVR-Doherty element was characterized over a wide range of DAC settings for controlling the current steering and G_m cells. Here, the current steering is primarily used to generate the desired phase shift and the G_m to equalize the gain

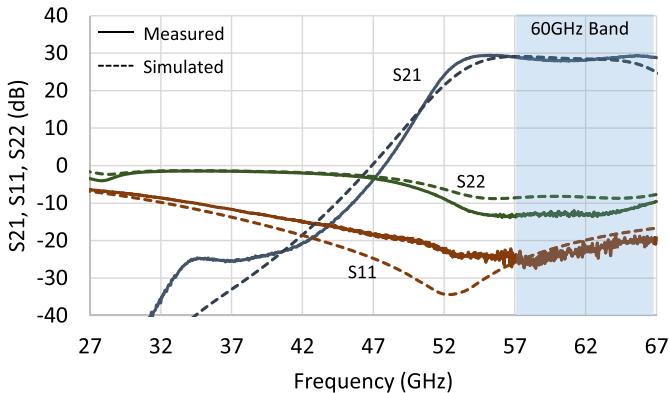


Fig. 15. Measured and simulated s-parameters for the dual-vector Doherty beamformer element for the 0° phase setting.

across each phase setting. From these, the 32 settings (i.e., 5-b accuracy) which minimized root-mean-squared (RMS) errors near 62 GHz for both amplitude and phase were chosen. These responses are presented in Fig. 14 along with the corresponding RMS errors. The RMS amplitude and phase error are less 0.6-dB and 6° , respectively, between 60 and 66 GHz. Near the lower side of the band at 57 GHz, these RMS errors rise to 1.2 dB and 8.5° as a result of error in the differential-quadrature circuits formed by the Lange coupler and switched baluns in the DVR. The s-parameters versus frequency for the zero-degree phase setting are compared versus the simulated results in Fig. 15 displaying excellent agreement. This setting shows less than 1-dB gain variation from 57 to 66 GHz.

The phase and amplitude responses for the axis settings (i.e., 0° , 90° , 180° , and 270°), shown in Fig. 16, reveal up to ± 1 -dB amplitude variation and $\pm 8^\circ$ quadrature error at 57 GHz. This accounts for the variation in gain seen at this frequency in the full 5-b responses. These plots show a clear deviation in measured results from the simulation. One key impact of this error is that the phase separation and amplitude balance between the two DVR outputs will differ across the frequency band. The phase separation directly influences the phase in which the carrier and peaking amplifier signals combine and thus results in a larger error than simply the amplitude variation of the differential quadrature. It is possible, however, to choose settings which minimize errors at these frequencies allowing a channel-selective form of optimization, but at the detriment of increased error at higher frequencies. A full-band single-calibration response could be obtained by correcting the Lange coupler and balun dimensions to yield more accurate differential quadrature in a future design.

C. Power and Efficiency of Array Elements

Swept-power measurements were conducted for both the Doherty element and the single-path PA using the same bias conditions for each. For the single-path PA measurement, the DVR is configured to operate in a single-vector interpolation mode where the current steering directs all RF power to a single output. The dc powers included in the PAE calculation are those in the full RF path, including the power amplifiers (Doherty/single-path PA) and the full DVR.

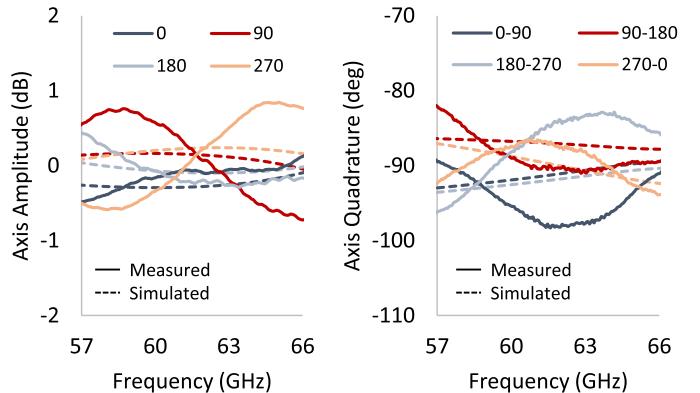


Fig. 16. Measured and simulated differential-quadrature accuracy of the Lange coupler and switched baluns characterized by steering all power in the DVR to a single output.

The swept-power responses in terms of gain and PAE versus output power are presented in Fig. 17(a) and (b) for the Doherty and single-path PA element, respectively. These plots indicate a 4-dB increase in oP_{1dB} for the Doherty element, where the Doherty and single-path elements achieve an oP_{1dB} of +17 and +13 dBm, respectively. As expected, the Doherty circuit exhibits higher output power, with 3 dB coming from the combination of two output amplifiers and an additional 1 dB coming from gain expansion in the peaking amplifier chain compensating for gain compression in the carrier amplifier chain. This form of compensation results in an oP_{1dB} for the Doherty amplifier very close to the saturated output power, whereas using the carrier bias for the single-path element results in an oP_{1dB} approximately 1 dB lower than the saturated output power.

Another indication of Doherty operation is illustrated by the PAE profiles of both the Doherty element and single-path PA shown in Fig. 18. The Doherty element achieves a peak PAE of 17% and a 6-dB back-off PAE of 7.8%, whereas the single-path element achieves a peak PAE of 12% and a 6-dB back-off PAE of 4.5%. Similar to the break-out circuit, the PAE of the Doherty element decays at a slower rate for increasing levels of back-off in comparison with the single-path PA, indicating the impact of active load modulation of the carrier PA. In this instance, the Doherty element achieves a 3%-point improvement in PAE at 6-dB output-referred back-off and a 5%-point improvement in PAE at P_{1dB} in comparison with the single-path element.

Our results show that the single-path PA (which is nearly identical to the carrier amplifier within the Doherty) achieves a lower peak PAE compared with the Doherty PA. This difference is due to a couple of factors. First, the PAE we report is for the full beamforming element, including output PA, predriver stage, and active phase shifter. When the DVR is used to drive a single output, it behaves like a traditional vector interpolator. In this mode, its power efficiency is reduced; hence, the overall efficiency of the transmit chain is degraded. Second, the peak collector efficiency of the Doherty stage is 23%, whereas the peak collector efficiency of the single-path PA is 17.4%. This 5.6-point difference in efficiency has been studied in simulation and is attributed in part to local differences within the supply plane and output matching net-

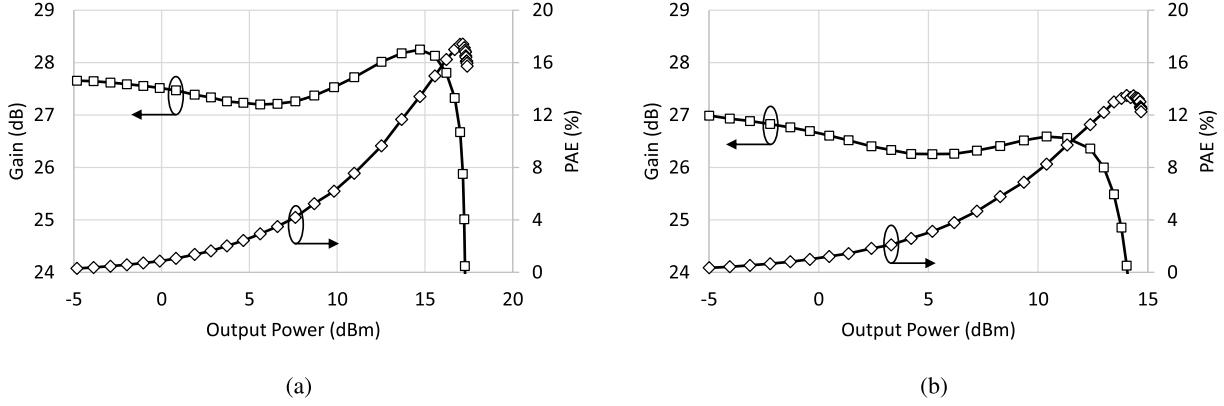


Fig. 17. Measured swept power and PAE of (a) dual-vector Doherty element and (b) single-vector element having conventional vector-interpolator phase shifter and single PA.

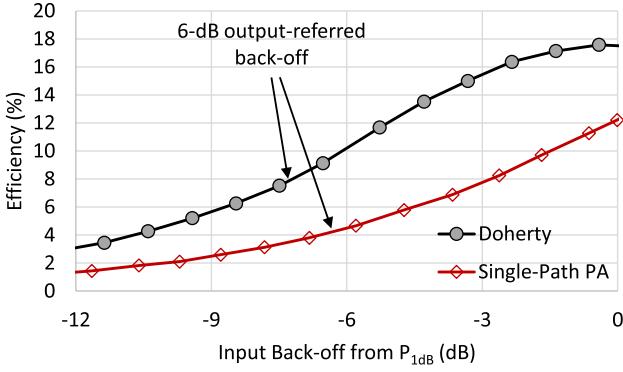


Fig. 18. Comparison of measured PAE of dual-vector Doherty and single-vector PA relative to input power back-off from 1-dB compression.

work for the single-path driver stage. Additional supply-plane resistance results in a lower local supply voltage which reduces the output power and degrades efficiency. Also, the single-path PA's output matching network was modified to directly drive the pad and external 50Ω load. A suboptimal output match resulted in further reduction in collector efficiency. For these reasons, we also compute the normalized efficiency, where the 6-dB back-off efficiency is 0.46 times peak PAE for the Doherty element and 0.38 times peak PAE for the single-path element.

The measured $\text{o}P_{1\text{dB}}$ versus frequency for the Doherty element's 0° setting is shown in Fig. 19. For frequencies greater than 63 GHz, the carrier amplifier begins to compress at a lower input power before gain expansion of the peaking amplifier begins to compensate. By adjusting the bias of the predrivers for both carrier and peaking paths, it is possible to realign these points to maintain the $\text{o}P_{1\text{dB}}$ produced at lower frequencies. Measurements were also conducted at 62 GHz for phase settings covering the full 360° phase-shift range showing less than 0.3-dB variation in $\text{o}P_{1\text{dB}}$ and less than 1% point in PAE.

D. Linearity of Array Elements

Due to equipment limitation, AM-PM and two-tone IM3 measurements were performed in place of EVM.

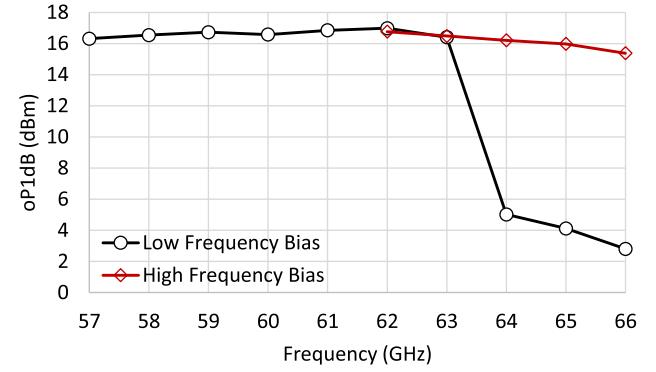


Fig. 19. Measured $\text{o}P_{1\text{dB}}$ for the 0° phase setting across frequency using two different bias conditions to cover the entire frequency band.

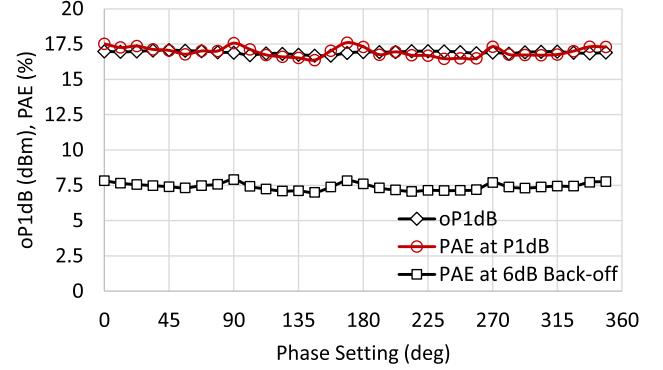


Fig. 20. Measured $\text{o}P_{1\text{dB}}$ and PAE at $\text{o}P_{1\text{dB}}$ and 6-dB output back-off.

The measured AM-PM distortion of both the Doherty and single-path PA across each phase setting as a function of output back-off level at 62 GHz is shown in Fig. 21. From these responses, it is clear that the Doherty amplifier exhibits a higher phase distortion in comparison with the single-path PA and also a greater variation in phase distortion among the different phase settings. The increased magnitude of phase distortion can be attributed to added nonlinearity of the class-C biased peaking amplifier turning on at these higher input power. The variation between the phase settings, however, is a result of these settings being chosen to minimize RMS phase and amplitude errors. This has resulted in some of the

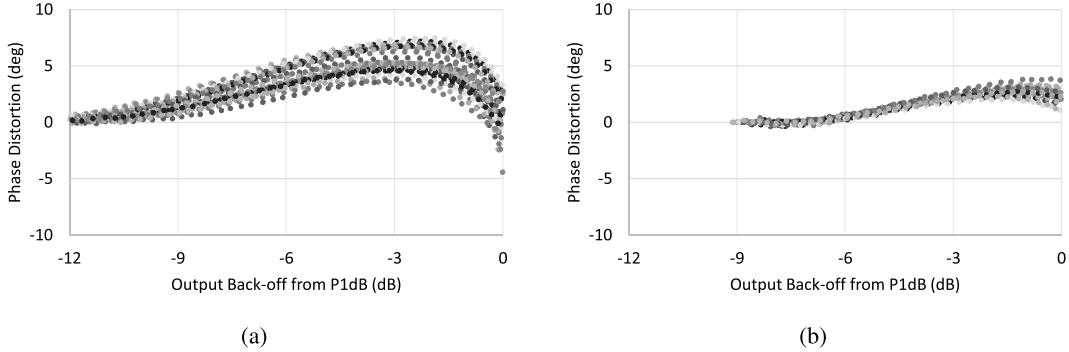


Fig. 21. Measured AM-PM distortion at 62 GHz relative to output power back-off of each phase setting for the (a) dual-vector Doherty path and (b) single-vector PA path.

TABLE II
COMPARISON OF DUAL-VECTOR DOHERTY BEAMFORMER WITH EXISTING 60-GHz PHASED-ARRAY TRANSMITTER FRONT-ENDS

Reference	This Work		[3] Boers ISSCC'14	[33] Vidojkovic ISSCC'14	[27] Chen ISSCC'13	[2] Cohen TMTT'13	[1] Valdes-Garcia ISSCC'10
Technology	130-nm SiGe BiCMOS		40-nm CMOS	40-nm CMOS	65-nm CMOS	90-nm CMOS	130-nm SiGe
TX Architecture	Doherty Mode	Single-Vector Mode	Traditional	Traditional	Quad. Spatial Combining	Traditional	Traditional
$\text{oP}_{1\text{dB}}$ (dBm)	16.7	11.8	5.2	10.8	9.6	0.5	13.5
DC PWR at $\text{oP}_{1\text{dB}}$ (mW)	271	126	45	181 *	52 *	22	313
PAE at $P_{1\text{dB}}$	16.5%	12%	7.4%	6.6%*	17.4%*	5.1%*	7.1%*
PAE at 3-dB oBO	10.8%	8.0%	—	—	—	—	—
PAE at 5-dB oBO	8.0%	5.0%	—	1.7%*	—	—	—
PAE at 6-dB oBO	7.0%	4.2%	—	—	7.0%	—	—
Element Area (mm^2)	0.96	—	1	1.5	0.63*	—	1.2*

* Estimated from plots/papers

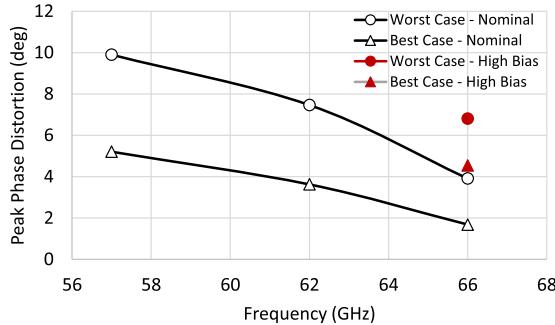


Fig. 22. Peak AM-PM distortion of the Doherty element across the 60-GHz frequency band for the best and worst case phase settings.

phase settings deviating from the ideal 90° phase separation and equal amplitude of the driving signals for the Doherty. Applying the same settings to the single-path PA elements determined the phase separation of the driving signals were near 75° , resulting in the increased phase distortion. Furthermore, the peak AM-PM distortion up to the 1-dB compression point of the Doherty element has been measured at the upper

and lower edges of the frequency band. These results are presented in Fig. 22.

As described earlier, the DVR has the ability to tune the phase separation between the two outputs to allow for optimization of Doherty performance across process, temperature, frequency, and voltage. The use of this tuning is shown in Fig. 23(a) where the DVR tunes the phase separation of the signals driving the carrier and peaking amplifiers. Through this adjustment, it is possible to correct for some of the phase distortion present in the different phase settings with negligible impact to the efficiency and output power. Similarly, the amplitude difference between the two driving signals can also be adjusted. Shifting more of the power to the carrier amplifier results in the AM-PM distortion approaching that of the single-path PA as demonstrated in Fig. 23(b), but at the cost of efficiency. When the offset between the carrier and peaking amplitudes reaches 4 dB, the PAE at $P_{1\text{dB}}$ and 6-dB back-off reduces to 13% and 5%, respectively. These results indicate that the Doherty amplifier can be transitioned to a more linear mode

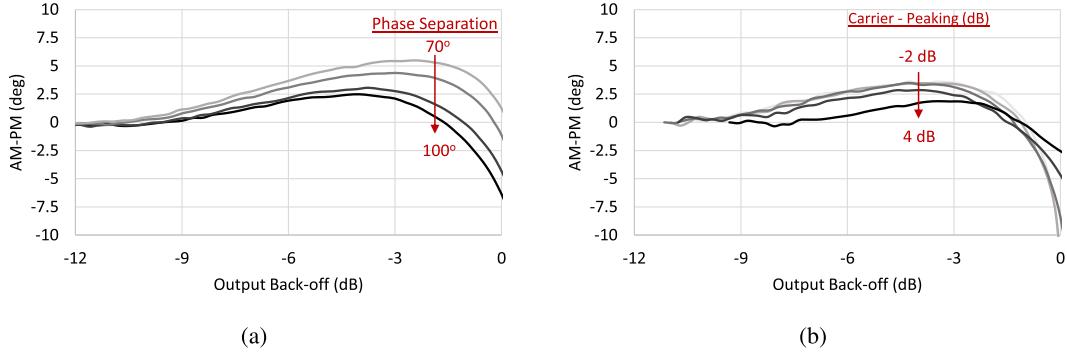


Fig. 23. Measured AM-PM distortion as a function of (a) phase separation and (b) amplitude difference of signals driving the carrier and peaking paths for the Doherty amplifier.

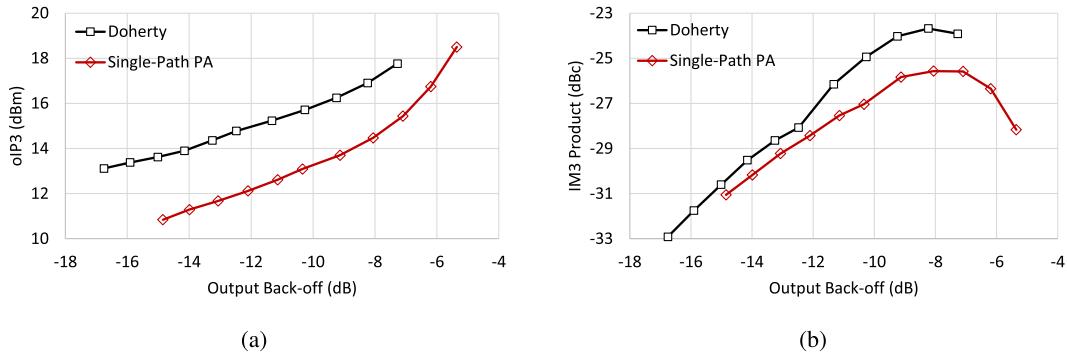


Fig. 24. Measured two-tone linearity for both the dual-vector Doherty path and single-vector PA path as (a) output-referred third-order intercept point and (b) IM3 product power relative to the fundamental frequency output power.

of operation enabling a tradeoff between the efficiency and linearity.

Two-tone IM3 measurements were conducted for the same phase settings. The two tones, located at 62 and 62.1 GHz, were combined using an external 3-dB Wilkinson combiner. The results are shown in Fig. 24 comparing the Doherty and the single-path PA. In comparison with the single-path PA on-chip, the Doherty amplifier demonstrates a higher output-referred IP3. This is attributed to a partial cancellation of IM3 distortion occurring within the Doherty structure, i.e., from the gain compression in the carrier amplifier having positive α_3 and the gain expansion in the peaking amplifier having a negative α_3 , where α_3 represents third-order power-series coefficient. Simulations reveal a similar IM3 cancellation, but for a 100° separation between the Doherty drive signals, compared with the nominally 90° separation used in measurements. The two-tone measurements for both Doherty and the single-path PA reveal asymmetric responses in the upper and lower products indicative of memory effects [26].

IV. CONCLUSION

The dual-vector Doherty element and single-vector mode PA presented here have been compared versus state-of-the-art for silicon technologies in Table II. Compared with other reported 60-GHz beamformers, the dual-vector Doherty achieves a higher output power with $\text{o}P_{1\text{dB}}$ of +16.7 dBm. In addition, a PAE for the complete beamformer (active phase

shifter, predrivers, and final Doherty stage) at 1-dB compression of 16.5% and at 6-dB back-off of 7% has been achieved. The efficiency at 6-dB back-off results in 3–4x improvement versus most other reported works, with the exception of Chen *et al.*'s work [27]. Chen's approach with quadrature spatial combining relies on separate in-phase and quadrature-phase paths where data can be decoded only in a specified spatial direction. This form of modulation demonstrates similar improvements in back-off efficiency to the dual-vector Doherty architecture presented here but could be difficult to use in phased-array applications requiring flexible beam patterns.

Referring to the tradeoff between output power, size, and power efficiency in Fig. 1, the dual-vector Doherty described here having +16.7-dBm $\text{o}P_{1\text{dB}}$ and 7% back-off efficiency would allow a six-element array to achieve 32-dBm EIRP at 6-dB back-off for a dc power consumption of 1 W. This smaller size will reduce the cost of the phased-array transmitter and make it more amenable for integration into systems having limited space. The efficiency improvement realized through the use of the Doherty architecture comes at the cost of reduced linearity in terms of AM-PM distortion. Through the use of the dual-vector rotator, it is possible to offset some of the penalties through control of the Doherty driving vectors. This enables the user to exchange the efficiency enhancement resulting from Doherty operation for improved linearity of a single-path PA and *vice versa*. Future work will consist of further investigating the Doherty element's linearity in terms of EVM and also

implementing an efficient means for calibrating a dual-vector phased-array architecture.

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