A 174.3-dB FoM VCO-Based CT ΔΣ Modulator With a Fully-Digital Phase Extended Quantizer and Tri-Level Resistor DAC in 130-nm CMOS

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***Abstract*— This paper presents a high dynamic range (DR) power-efficient voltage-controlled oscillator (VCO)-based continuous-time ΔΣ modulator. It introduces a robust and low-power fully-digital phase extended quantizer that doubles the VCO quantizer resolution compared to a conventional XOR-based phase detector. A tri-level resistor digital-to-analog converter is also introduced as complementary to the new quantizer, enabling high DR while creating a dynamic power saving mechanism for the proposed design. Fabricated in 130-nm CMOS, the analog-to-digital converter achieved peak Schreier Figure-of-Merit (FoM) of 174.3 dB with a high DR of 89 dB over 0.4-MHz BW, consuming only 1 mW under 1.2-V power supply. It also reaches a peak Walden FoM of 59 fJ/conv with 74.7-dB signal-to-noise-and-distortion ratio over 2-MHz BW.**

***Index Terms*— Analog-to-digital converter, continuous-time ΔΣ modulator, intrinsic dynamic element matching (DEM), phase detector (PD), phase-domain analog signal processing, pulsewidth-modulation (PWM), time-domain (TD) analog-to-digital converter (ADC), VCO-based ADC.**

I. Introduction

THE economic superiority and market success of system-on-a-chip (SoC) drive analog-to-digital interfaces to follow the trend of technology scaling. Unlike digital circuits, which naturally improve with smaller transistor size, many conventional voltage-domain mixed-signal architectures see little benefit or even suffer from migration into advanced processes due to reduced supply voltage and transistor intrinsic gain. This fact calls for a new design framework for key mixed-signal building blocks that leverages the properties of CMOS scaling instead of being limited by them. One of these frameworks is time-domain (TD) analog signal processing and quantization techniques for analog-to-digital converter (ADC) design. By representing and processing signals using time related variables, such as frequency, phase, and pulsewidth, TD techniques are much more low-voltage tolerant. Also, TD techniques benefit from transistor scaling, as time information can be processed through mostly digital structures. As part of this framework, continuous-time ΔΣ modulators (CTDSMs) that employ ring voltage-controlled oscillators (VCOs) as TD integrator and quantizer have been reported in [1]–[21]. There are several key merits of a ring VCO-based integrator and quantizer as follows.

1) It utilizes the inherent integration from frequency to phase, thus providing infinite dc gain with little voltage headroom and intrinsic gain limitation.
2) Multilevel quantization can be obtained by simply sampling all nodes of the ring VCO, removing the need for precise reference level generation and relaxing the comparator design.
3) It is built with inverters, thus is highly scaling-friendly and easy to design.

Despite these advantages, the highly non-linear voltage to frequency conversion of the VCO raises practical concerns and challenges for designing a VCO-based CTDSM, especially for those that use frequency as the output. The open-loop architectures proposed in [10] and [15] tackled this issue with digital calibration [Fig. 1(a)]. But the effectiveness of the digital calibration relies on the replica path matching, which is difficult to guarantee over process variation. Straayer and Perrott [6] embedded the VCO quantizer in a ΔΣ loop and highlighted intrinsic dynamic element matching (DEM) using frequency feedback [Fig. 1(b)]. This work relied on the front-end integrator to attenuate the VCO non-linearity; but such method did not work well for low oversampling ratio due to reduced integrator gain at high frequency. Another work proposed to place the VCO quantizer at the latter stage of a sub-ranging architecture to minimize its input [13] [Fig. 1(c)]. But the overall performance was limited by the digital-to-analog converter (DAC) mismatch in the coarse stage and the gain error between stages, which needed to be tackled by extra hardware complexity.

Another main category of VCO-based CTDSM uses phase as its output. They harness the integrating behavior of phase-based quantizers to minimize the VCO input swing, leading to high linearity of the VCO-based quantizer. The architecture proposed in [7] highlighted the use of an XOR-based phase detector (PD), which can efficiently convert the quantized phase into a thermometer code for direct DAC control [Fig. 1(d)]. The drawback of this architecture is that it requires explicit DEM. Lee *et al.* [17] proposed a dual-VCO architecture [Fig. 1(e)]. This scheme promotes lower VCO noise and power as it allows "arbitrary" VCO

Manuscript received November 27, 2016; revised February 6, 2017 and March 22, 2017; accepted March 28, 2017. Date of publication April 8, 2017; date of current version June 22, 2017. This paper was approved by Guest Editor Eugenio Cantatore. *(Corresponding author: Shaolan Li.)*

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Digital Object Identifier 10.1109/JSSC.2017.2693244

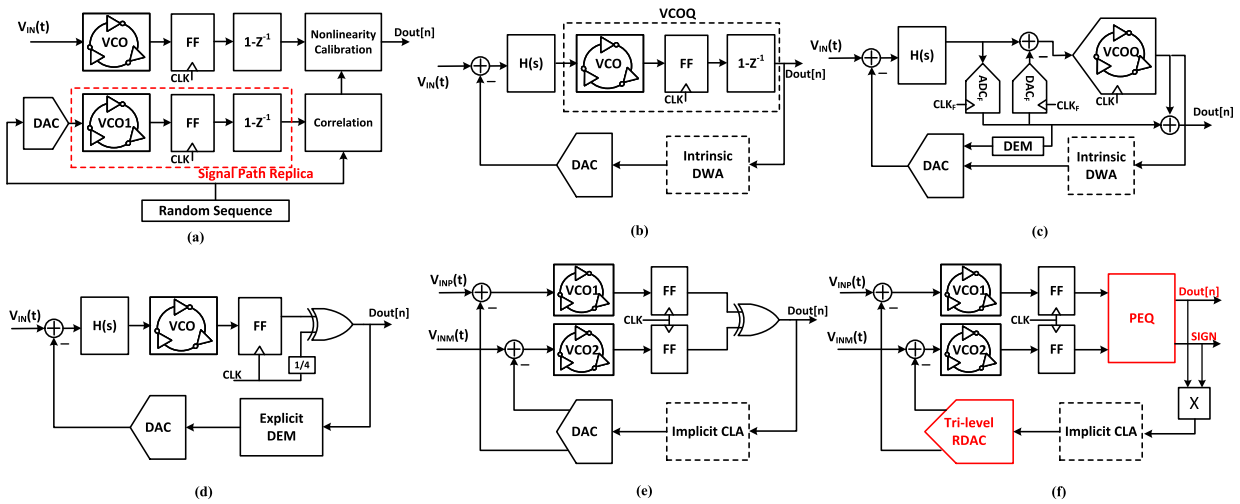


Fig. 1. (a) Open-loop VCO-based CTDSM with non-linearity correction. (b) Closed-loop architecture using frequency feedback. (c) Residue canceling architecture. (d) Closed-loop architecture using phase-feedback. (e) Dual-VCO architecture. (f) Proposed dual-VCO architecture with PEQ and tri-level DAC.

center frequency and, importantly, introduces intrinsic clocked averaging (CLA)-based DEM. However, it doubled the number of flip flops in the sampler, limiting the overall power benefit. Another recent work [19] combined both phase and frequency as the output, which struck a balance between the power and linearity tradeoff.

The best dynamic-range-based Schreier Figure-of-Merit (FoM) achieved by state-of-the-art VCO-based CTDSMs is around 170 dB. Through exploring the possibilities to advance the state-of-the-arts, we identified two limitations in the phase-based architectures reported so far that deserve further refinement. First, similar to a basic flash ADC, VCO-based quantizers using an XOR PD requires 2^N stages to produced N-bit resolution. The power efficiency of such quantizers are subpar considering the resolution it can provide. Second, though the XOR PD naturally facilitates thermometer-coded bi-level control for the feedback DAC, the power of a bi-level DAC can be large when designing for high dynamic range (DR) because the current consumption is constant and equal the maximum signal swing. We thereby inferred that with an improved quantization scheme as well as a DAC control scheme with relaxed power requirement, great power efficiency improvement for VCO-based CTDSMs can be realized.

This paper proposes a closed-loop CT VCO-based DSM featuring a purely-digital power-efficient phase extended quantizer (PEQ). On top of implementing the XOR-based phase detection, it uses simple combinational logic gates to extract the lead-lag information of the dual VCO. The lead-lag information is used as an additional bit for the VCO quantizer, which essentially doubles the resolution without doubling the power and hardware. With this technique, we implemented a 5-b VCO-based quantizer with only 15 ring stages, demonstrating great utilization of hardware. The outputs of the PEQ readily facilitate a tri-level DAC control pattern and, importantly, also maintain an intrinsic CLA capability, removing the need for explicit DEM. Since, the proposed PEQ is purely digital, it is highly compatible with the scaling friendly merits of TD signal processing. The simplified architecture is shown in Fig. 1(f).

The proposed work also highlights the use of a tri-level resistor DAC (RDAC). The combination of the PEQ's tri-level pattern and an RDAC creates a dynamic power saving mechanism that automatically reduces the power consumption when input amplitude is low. With this feature, the DAC only burns power when it is needed which greatly relaxes the power consumption compared to a bi-level DAC. In addition, the RDAC exhibits better matching and lower noise compared to a standard current steering DAC current DAC (IDAC), enabling us to reach high DR with low power. The combination of PEQ and tri-level RDAC bestows this work with a 2.5× power efficiency improvement in terms of Schreier FoM over prior arts.

This paper is an extension of a previous work reported in [21] and is organized as follows. In Section II will briefly review the dual-VCO quantization scheme. Section III will introduce and analyze the proposed extended phase detection scheme. Discussion regarding dynamic power saving and the tri-level RDAC will be addressed in Section IV. Section V presents the circuit implementation details and addresses design concerns. The measurement results of the prototype will be demonstrated in Section VI. We then brought up the conclusion in Section VII.

II. Review of Dual-VCO Scheme

To provide a foundation for the proposed work, this section briefly reviews the operating principle and properties of the dual-VCO phase quantizer with XOR-based PD. Fig. 2(a) depicts an exemplary 5-stage dual-VCO phase quantizer (sampling block not explicitly shown). By detecting the logic level difference of corresponding nodes in the ring pair, the XOR gates produce waveforms whose pulsewidth represents the phase difference. Assuming the gate delay of each ring stage is identical (which is also practically desired), the outputs of the XOR gates have evenly spaced phase

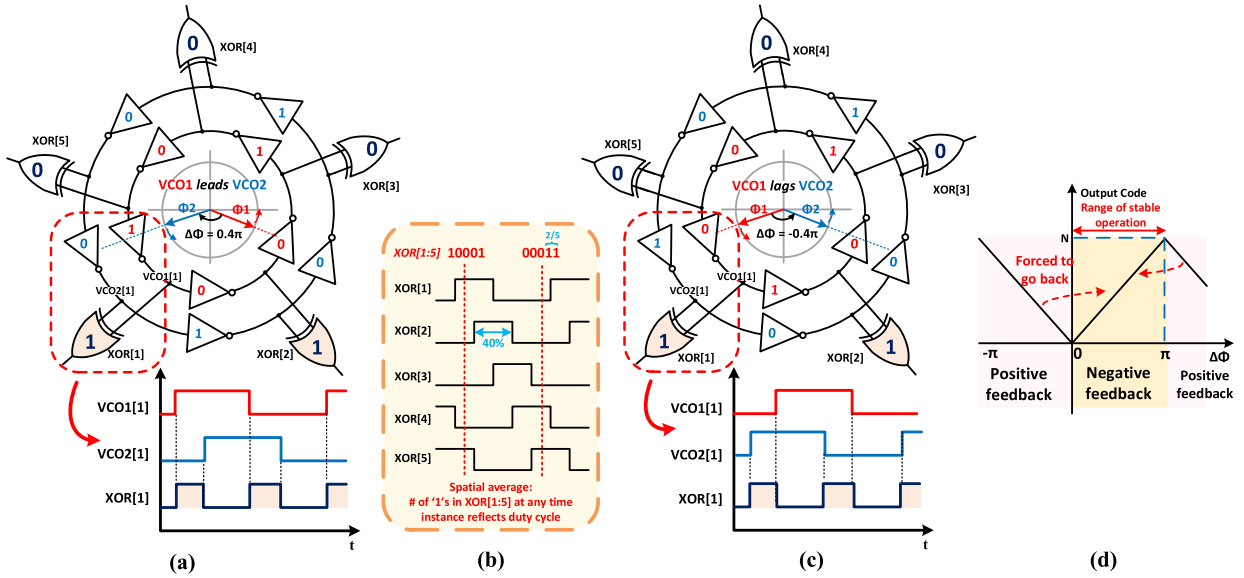


Fig. 2. (a) Example operation of the dual-VCO scheme with XOR PD. (b) Illustration of spatial average of pulsewidth. (c) Example of VCO1 in lag status. (d) Phase-output transfer curve of the XOR PD.

delay, therefore they naturally provide a thermometer code that represents a quantized spatial average of the pulsewidth (i.e., phase difference), as shown in Fig. 2(b). With larger number of stages, the phase difference will be quantized with finer steps. Without any extra logic, each XOR output can be directly used to control a thermometer DAC element.

Reference [17] qualitatively proved that the XOR waveform, and eventually the input of each DAC element, is essentially a pulsewidth-modulation (PWM) of the ADC input with a carrier frequency at $2f_{\mathrm{vco}}$. Thanks to this property, the DAC mismatches are up modulated to $2f_{\mathrm{vco}}$, and thus are prevented from creating in-band signal harmonics. This intrinsic DEM mechanism has been identified as a key advantage of the dual-VCO scheme. In addition, as the phase in the dual-VCO scheme is self-referenced, the free-running frequency of the VCOs can be set "arbitrarily," as long as the PWM artifacts of the mismatch are kept out of band. This allows the VCO to operate at a low frequency, which lowers the bias power and especially phase noise [22].

Despite its merits of simplicity and mismatch tolerance, the dual-VCO scheme is still subject to the limitation of the XOR PD. An XOR gate detects phase through the voltage level difference between two VCO nodes, but its memoryless nature renders it unable to distinguish lead-lag status of the input phases. As depicted in Fig. 2(c), although the lead-lag status of the two VCOs is flipped compared to Fig. 2(a), the outputs of the PD in both cases are identical, suggesting a non-monotonic phase to output transfer curve, as shown in Fig. 2(d). Noted that the slope is negative when the phase difference is between $-\pi$ and 0. This indicates that if VCO1 is in lag, the feedback becomes positive and eventually enforces VCO1 to always be in lead such that the loop is stabilized with negative feedback. For this reason, a dual-VCO quantizer with the XOR PD is using only half of the information available in the system, or equivalently, only using half of the reference levels in analogy to a flash quantizer. If the lead and lag status

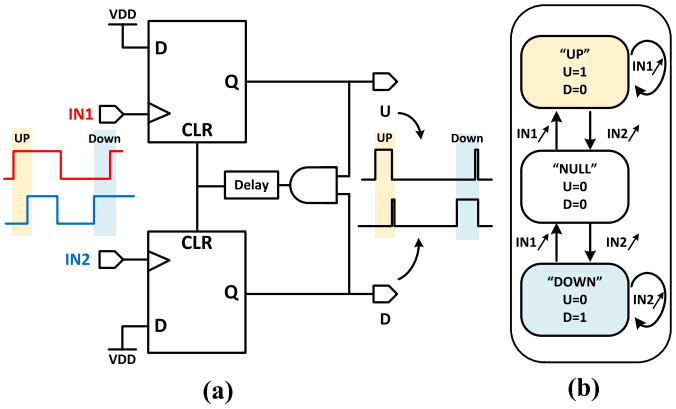


Fig. 3. (a) schematic and (b) state diagram of the PFD.

can be extracted and utilized as a sign bit, the linear phase range can be extended to the negative side and the rest of the reference levels can be spanned. This can effectively double the resolution without extra VCO stages and simultaneously double the signal swing in the time domain. By guaranteeing the lead-lag detection is implemented with reasonably low hardware and power overhead, significant improvement in DR and power efficiency can be achieved. This potential improvement was the motivation for the proposed extended phase detection scheme.

III. Extended Phase Detection Scheme

This section addresses the practical design considerations for implementing phase range extension using lead-lag status. We start with the discussion on the conventional lead-lag detection method using the phase-frequency detector (PFD), and illustrate its deficiency in the context of CTDSM. A CTDSM-compatible and pure combinational PEQ will be subsequently proposed and analyzed.

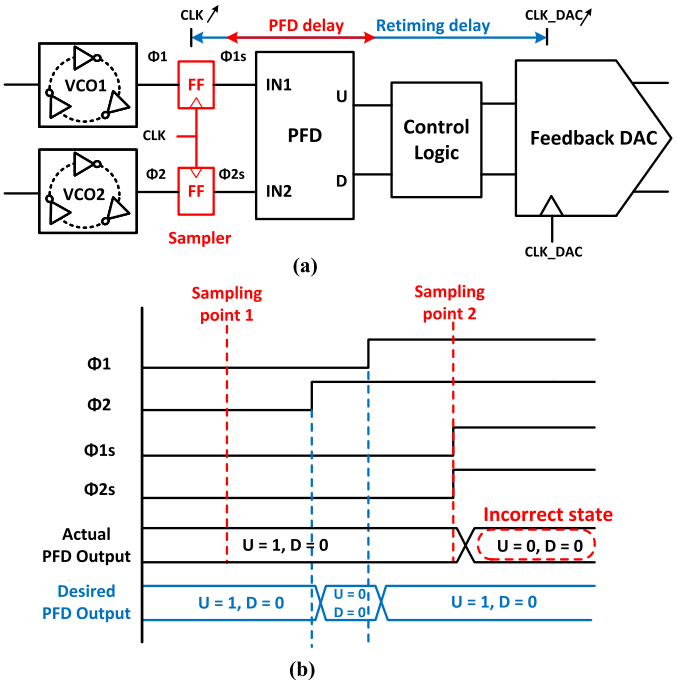


Fig. 4. (a) Configuration with PFD after the sampler. (b) Illustration of incorrect state transition due to the configuration in (a).

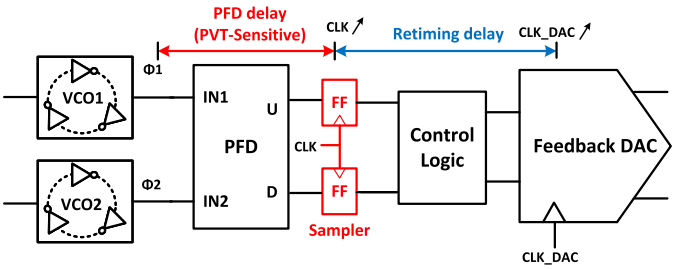


Fig. 5. Configuration with PFD before the sampler. The total ELD becomes PVT-sensitive.

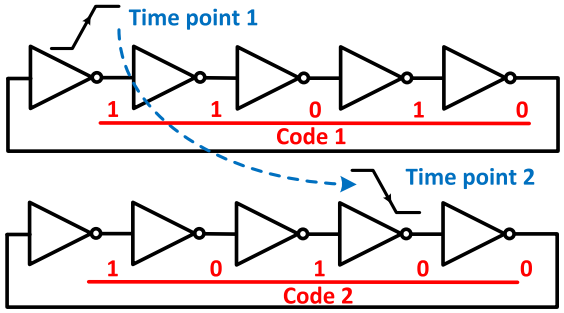


Fig. 6. Example of time-space encoding of a ring VCO.

A. Phase Frequency Detector

The PFD is essentially a finite state machine triggered by the edges of the input signals. A conceptual diagram of the PFD is shown in Fig. 3. Assuming, it is initialized to the "Null" state (U = 0 and D = 0), a rising edge from either input, depending on whoever arrives first, triggers a state transition to either "UP" (U = 1 and D = 0) or "DOWN" (U = 0 and D = 1). The PFD will stay at these states until a rising edge of the other input is detected. Intuitively, the resulting waveform of the PFD output is also shown in Fig. 3(a). If IN1 leads IN2, U will be high in between their rising edges and D remains low, and vice versa. Like the XOR-based PD, the PFD modulates the phase difference into pulsewidth of the output. In addition, it also utilizes the lead-lag status of inputs to govern which output (U or D) to activate. Therefore, it can distinguish the polarity of the phase difference, monotonizing the phase-output transfer curve. The separate outputs also readily facilitate DAC control with feedback direction awareness.

However, the mixed continuous-discrete timing nature of a CTDSM causes issues for the PFD to serve as a reliable phase quantizer. This can be explained by two possible design cases. Depicted in Fig. 4(a), the first case configures the PFD after the sampling block. In this case, the inputs to the PFD are sampled versions of the VCO outputs. Due to sampling, the original rising edges of the VCO outputs are modified and forced to be synchronized to the sampling clock. This causes loss of phase details, leading to incorrect state transitions and errors at the phase quantizer output. For instance, as shown in Fig. 4(b), we consider a scenario where ϕ_1 is leading ϕ_2 (by close to 2π) and the PFD is initially showing the correct state (U = 1 and D = 0). At sampling instant 2, it misses the time difference between the rising edge of ϕ_1 and ϕ_2, the PFD thus changes to an undesired state. In the other case, the PFD is placed before the sampler, as shown in Fig. 5. This configuration leaves the inputs of the PFD untouched, thus guarantees the accuracy of the PFD outputs. However, the logic delay of the PFD is not absorbed into the retiming delay between the sampler and the feedback DAC. This adds extra process-voltage-temperature (PVT)-sensitive excess loop delay (ELD) on top of the retiming delay. As the output swing of the VCO is usually low (e.g., 0.5–0.6 V), the speed of the PFD is limited in this configuration. This configuration may work for low-speed low-voltage applications where all digital blocks are slow, as the delay introduced by the PFD is minor. But for high-speed design, this configuration may fail. This is because the PFD's PVT-sensitive delay becomes significant compared to the retiming delay, making the ELD difficult to be compensated reliably over corners. In conclusion, using the PFD as a PD for VCO-based CTDSMs is a suboptimal design choice in general due to its lack of robustness for high-speed operations. A more broadly reliable implementation of lead-lag detection is preferred for VCO-based CTDSMs.

B. Phase Extended Quantizer

The key requirement for lead-lag detection is that there are memories in the system capturing what has happened. Interestingly, the ring VCO itself already has this memory built in, because each node maintains the logic level since the last transition and will only be flipped when a new transition arrives. Therefore, the time information of a ring VCO has been intrinsically recorded into the bit pattern of its nodes in the space domain, as illustrated in Fig. 6. By processing the bit patterns, we can extract the location of the transition edges and subsequently obtain the lead-lag status. In other works, as long as we can access all nodes of the VCO, lead-lag detection can

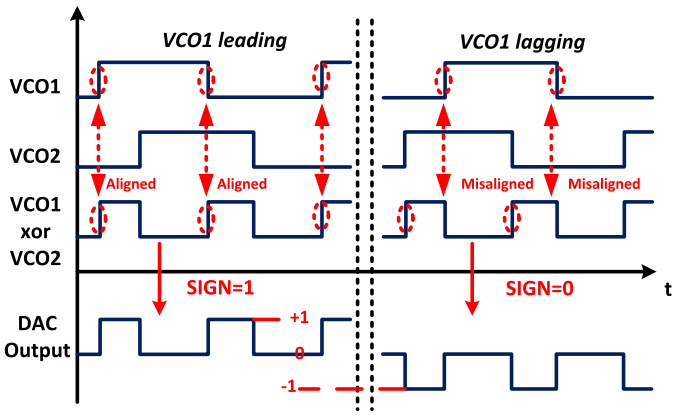


Fig. 7. Conceptual representation of the proposed lead-lag detection method.

be implemented by pure combinational logics. This logic can thus be placed after the sampler and absorbed into the retiming delay, leading to a highly reliable system.

As suggested by Fig. 6, the location of a transition edge is essentially represented by an encoded binary string. Direct computation of the distance of the transition locations involves extensive decoding and calculation, thus it is not a smart approach to detect lead lag. In this paper, we propose a hardware and power efficient approach for lead-lag detection other than relying on brute-force location comparison. This method can be viewed as an extension of the XOR PD. The conceptual mechanism is illustrated in Fig. 7. In this method, instead of focusing on both VCOs' edges, we pay attention to the alignment between the rising edge of the XOR PD output and the transition edge of VCO1. This is because, assuming we know that the phase difference is within $-\pi$ to π, the XOR output will always rise together with the leading phase transition. Thus, using a proof by contradiction notion, by inspecting whether the edge of VCO1 aligns with the rising of the XOR gates, we can tell the lead-lag status of the two VCOs. (i.e., if they align, VCO1 is leading, and if they misalign, VCO1 is lagging.) Note that although we depict this method in a TD manner in Fig. 7, the alignment check is actually implemented in space-domain, which is straightforward and low cost.

To promote a better understanding for this method, Fig. 8 provides pseudo code describing the logic flow in (a), along with two example scenarios using gate level schematics in (b) and (c). The numbers in Fig. 8(b) and (c) represent the logic level of the gates at a certain sampling instant. These two graphs serve as a space-domain representation of Fig. 7. As suggested by Fig. 8, the transition points (TP1/TP2) of the VCOs are signified by adjacent cells that share the same logic levels. Similarly, the frontal edge (FE) of the XOR thermometer code can be indicated by a "1–0" pattern in the current and next XOR gates. From Fig. 8(b) and (c), we can see that when VCO1 is in the leading state, TP1 is always in alignment with FE. If TP1 and FE are misaligned, VCO1 is in the lagging state. To inspect this alignment, we can use a one-hot vector $\overrightarrow{tp1}$, which is generated by performing XNOR operations on consecutive VCO nodes [Fig. 8(a) line 1], to represent the TP1 location. Then we map the FE location to another one-hot vector $\overrightarrow{fe}$, which is produced from the logic operation of line 2 in Fig. 8(a). Mathematically, as $\overrightarrow{tp1}$ and $\overrightarrow{fe}$ belong to the same orthogonal set, the alignment can be obtained directly from the dot product of $\overrightarrow{tp1}$ and $\overrightarrow{fe}$ [Line 3 and 4 in Fig. 8(a)]. When VCO1 leads, $\overrightarrow{tp1}\cdot\overrightarrow{fe}=1$, and when VCO1 lags, $\overrightarrow{tp1}\cdot\overrightarrow{fe}=0$. As the vectors are one-hot, the summing operation in the dot product can be simplified as OR logic. Therefore, this proposed lead-lag detection method requires only four steps of basic combinational logic operations and wiring between adjacent nodes. In addition, the dot product $\overrightarrow{tp1}\cdot\overrightarrow{fe}$is inherently a sign bit representing the polarity to the XOR PD output, thus readily facilitating post processing and DAC control. As a result, the proposed PEQ demonstrates great hardware and power efficiency.

From the DAC control perspective, the introduction of the sign bit transforms the control scheme into tri-level. In this tri-level scheme, each XOR PD output still controls a single DAC element, but with the sign as a global modifier. As illustrated in Fig. 7, when the corresponding XOR output of a DAC cell is "1," the DAC cell will be activated, and either source or sinks current depending on sign. A DAC element will be deactivated, i.e., neither sourcing or sinking current, if the corresponding XOR output is "0." With this configuration, the negative phase range can be utilized without resulting in positive feedback. The feedback will manage to pull any phase difference back to zero to achieve differential symmetry. The phase to output transfer curve of the PEQ is depicted in Fig. 9. Compared to that of the conventional XOR PD, the PEQ resides at zero phase difference when quiescent instead of $\pi/2$. In subsequent discussion, we will show that the elimination of the static phase error enables dynamic power saving, another key merit of the PEQ.

IV. Analysis of the Tri-Level RDAC

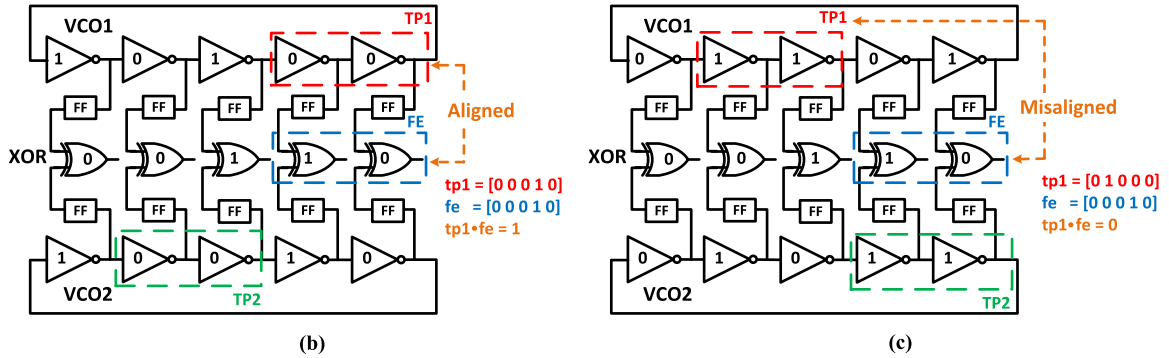
A. Dynamic Power Saving

The outputs of the XOR gates falling between the transition points of the VCOs are always logic "1" while the outputs falling outside are always logic "0." Therefore, the PD output manifests as barrel-shifted thermometer codes. When input amplitude is low, the conventional XOR PD maintains about half of the bits "1" due to the phase error of $\pi/2$ [17]. On the other hand, as the static phase error of the proposed PEQ is zero, at low input the transition points of the dual VCO are very close to each other, making the thermometer code mostly "0" with only a few occasional "1"s. This suggests that the activity rate of the PEQ output naturally reduces when the input amplitude goes from high to low, as illustrated in Fig. 10. This input-dependent activity reduction can facilitate dynamic power saving in two aspects as follows.

1) The number of logic transitions between samples is reduced when the input is inactive. This in fact lowers the switching activity in the retiming latches and DAC drivers, thus bringing down the digital power in these parts.
2) As mentioned in the previous discussion, since the DAC is now tri-level controlled, it only needs to provide

```
1   tp1          = xnor(VCO1[1:5], VCO1[2:5,1]);   %%Point to TP1
2   fe           = and(XOR[1:5], not(XOR[2:5,1])); %%Point to FE
3   tp1Dotfe     = and(tp1, fe);                   %%Compute dot product
4   sign         = sum(tp1Dotfe);                  %%of vector tp1 and fe
```

(a)



(b) (c)

Fig. 8. (a) Pseudo code describing the proposed lead-lag detection flow. Example scenarios for (b) lead and (c) lag cases.

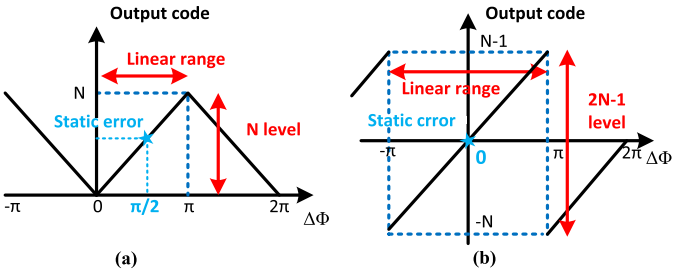


Fig. 9. Phase-output transfer curve comparison for (a) XOR PD and (b) proposed PEQ.

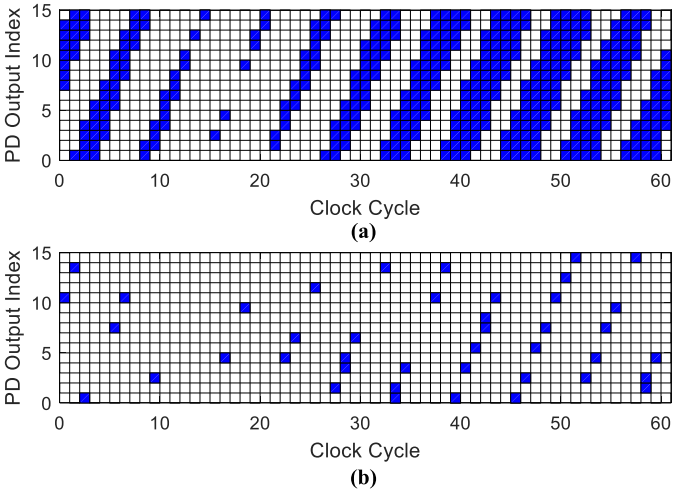


Fig. 10. Simulated output bit pattern of the PEQ at (a) −3 dBFS and (b) −23 dBFS input.

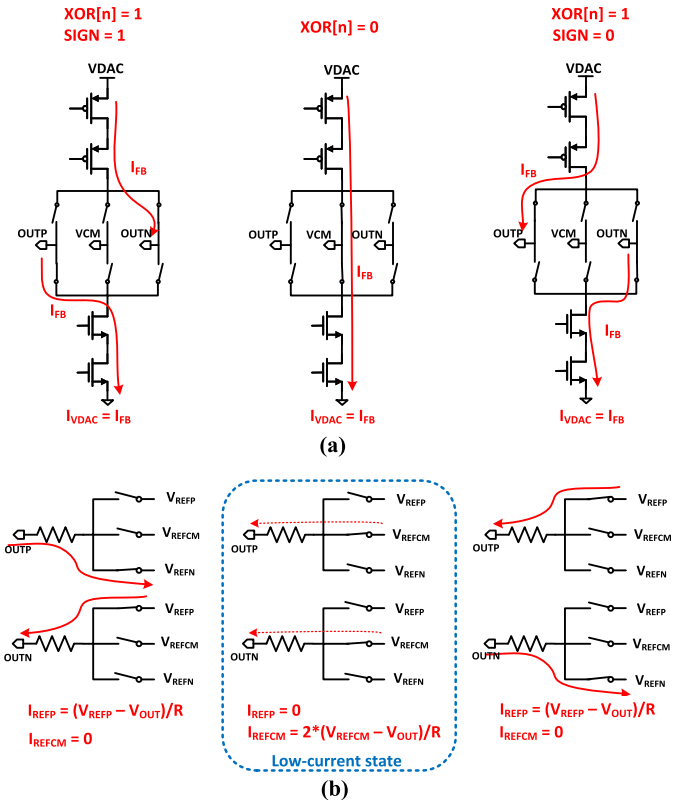


Fig. 11. Current consumption versus input. (a) Tri-level IDAC is input independent while. (b) Tri-level RDAC is input dependent.

feedback when the corresponding thermometer bit is high and remains inactive when the bit is low. The DAC power consumption with low input can be minimized by implementing a tri-level DAC that burns very low power in the inactive state@comma since the majority of the PEQ outputs are “0” at low input.

A standard tri-level IDAC, as shown in Fig. 11(a), consumes constant current across all input cases. Thus it cannot take advantage of the PEQ’s output pattern to save power. For this reason, we choose to implement the DAC with resistors. By using resistors, we have the option to place the switches on the reference side, such that the current consumption of the RDAC can be input dependent. The simplified schematic of a

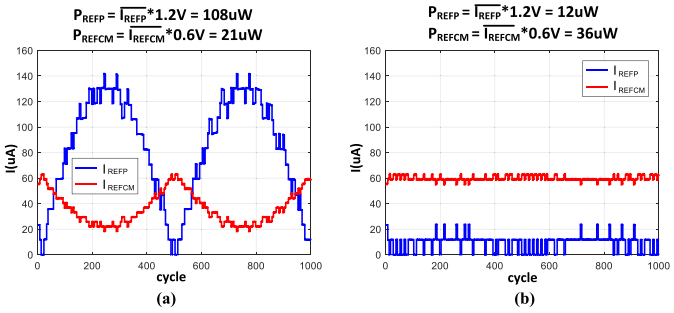


Fig. 12. Simulated waveform of the current drawn from V_{REFP} and V_{REFCM} at (a) −3 dBFS and (b) −23 dBFS input.

tri-level RDAC element is shown in Fig. 11(b). When the input is "0" (i.e., XOR = 0), the resistors are connected between the feedback point and V_{REFCM}. As the average dc level of the feedback node is usually close to V_{REFCM} by design and does not vary by much due to multi-level feedback, the current consumed by the RDAC in the inactive state is thus relatively lower than in the active state. Therefore, the proposed RDAC is able to leverage the PEQ's output pattern to achieve dynamic power saving. The simulated current profiles of the RDAC references with sinusoidal inputs are shown in Fig. 12, where the dynamic scaling of DAC current can be visualized. The total DAC power ($P_{REFP} + P_{REFCM}$) drops by 62% when input goes from −3 dB [Fig. 12(a)] to −23 dB [Fig. 12(b)] in this design example.

Noteworthily, Fig. 12(a) reveals that the current of the tri-level RDAC resembles a rectified version of the input, suggesting that the dynamic power saving mechanism is also functioning as a built-in duty cycling. Hence, the power efficiency of the DAC (and the DAC-related digital circuitry) gets improved not only at low input, but also at full scale.

B. Merits and Drawbacks of RDAC

Apart from facilitating dynamic power saving, there are two additional advantages of using an RDAC.

First, an RDAC produces noticeably lower noise than an IDAC [23]–[25]. Define $\overline{i}^2_{n,\mathrm{RDAC}}$ and $\overline{i}^2_{n,\mathrm{IDAC}}$ as the thermal noise current of an RDAC and IDAC element, respectively. Following the analysis in [25], the ratio of the noise power can be estimated by:

$$\frac{\overline{i}^2_{n,\mathrm{RDAC}}}{\overline{i}^2_{n,\mathrm{IDAC}}} = \frac{V_{\mathrm{OV}}}{2\gamma\, V_{\mathrm{step}}} \tag{1}$$

where V_{OV} is the overdrive voltage of the IDAC tail device and V_{step} is the voltage step between the tri-level RDAC references. For the 130 nm process, we are working with, the maximum V_{step} can be 0.6 V (half of the 1.2-V core voltage). Due to voltage headroom limitations, our design only allows a maximum V_{OV} of about 0.3–0.4 V for an IDAC with cascoded tail device. Assuming γ is 1, (1) suggests that the noise contributed by an RDAC element in this paperis about 5–6 dB lower than the IDAC counterpart. Second, an RDAC exhibits better raw matching compared to an IDAC. To verify this, a Monte Carlo simulation was performed to extract the

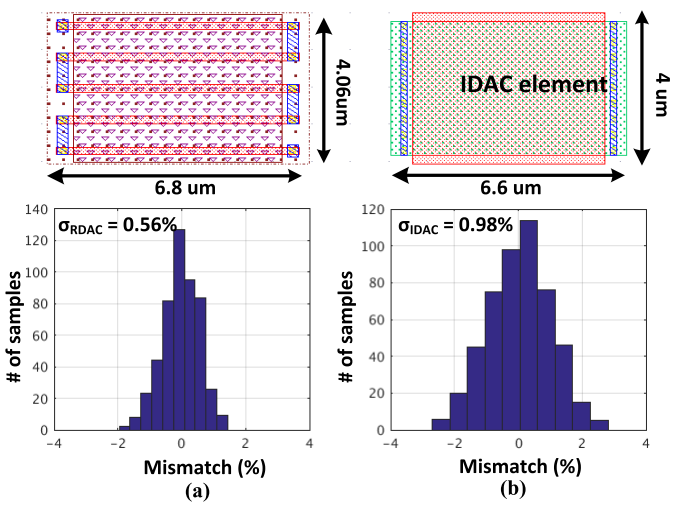


Fig. 13. Current mismatch histogram for (a) RDAC and (b) IDAC from 500 Monte Carlo runs.

current variations of a RDAC element (6.8 by 4.06 μm) and a geometrically-similar IDAC element (6.6 by 4 μm). The IDAC is biased at 0.3V V_{OV}. The histograms showing current variation for both DACs generated from 500 Monte Carlo run is plotted in Fig. 13. The standard deviation of the RDAC mismatch is about 2 times smaller than that of the IDAC, which is essentially a 6 dB improvement.

On the other hand, there are a few drawbacks associated with RDAC that merit a discussion. To begin with, as suggested by Fig. 12. the reference buffer needs to handle the signal-dependent current profile. Special awareness is thus needed to ensure a low buffer output impedance over the signal band to prevent distortion of the feedback current. Also, the tri-level RDAC requires an extra reference buffer for V_{REFCM}, which brings in extra power consumption. Nevertheless, this reference buffer does not need to have the same driving capability as the source for V_{REFP}, as the current going through V_{REFCM} has a much lower peak value and is less transient-demanded. With careful design, the power overhead for generating V_{REFCM} will not be significant. Another drawback of using the RDAC is that it introduces extra resistive loading to the virtual ground node. This effect is known for degrading the noise of an active-*RC* integrator. In this design, the feedback node is directly connected to a current-starved VCO instead of an active-*RC* integrator, thus the resistive loading directly affects the modulator's loop gain, leading to degradation on the in-band noise shaping. This can be compensated by increasing the VCO's tuning gain. Overall, these drawbacks are minor compared to the benefits of dynamic power saving.

C. Analysis on Tri-Level CLA

In this section, we show that our proposed PEQ scheme retains the intrinsic CLA mechanism that was mentioned to have been presented in a bi-level controlled dual-VCO based design. To analyze this, let us first visualize the phase-domain operation of the proposed design using Fig. 14. ϕ_1 and ϕ_2 represent the phase of VCO1 and VCO2, respectively. The

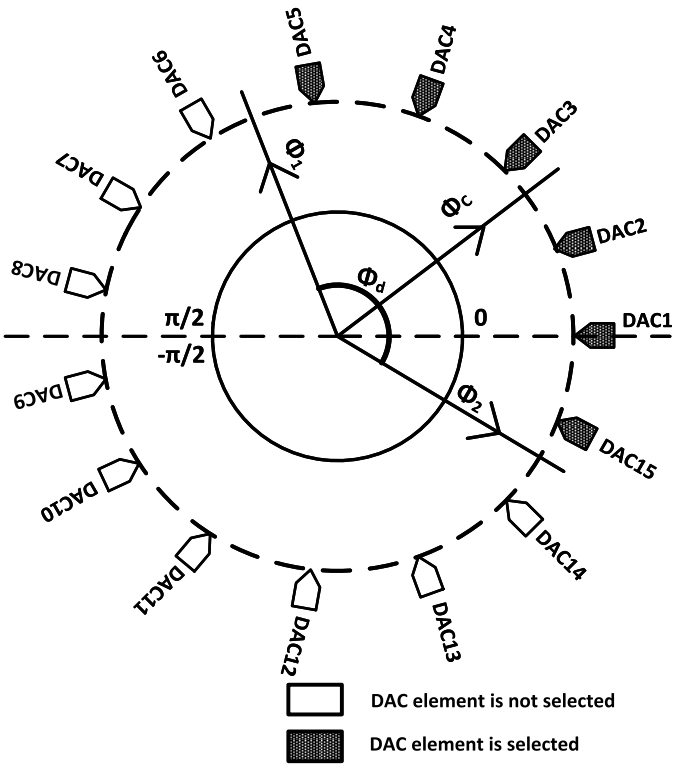


Fig. 14. DAC selection viewed in phase domain.

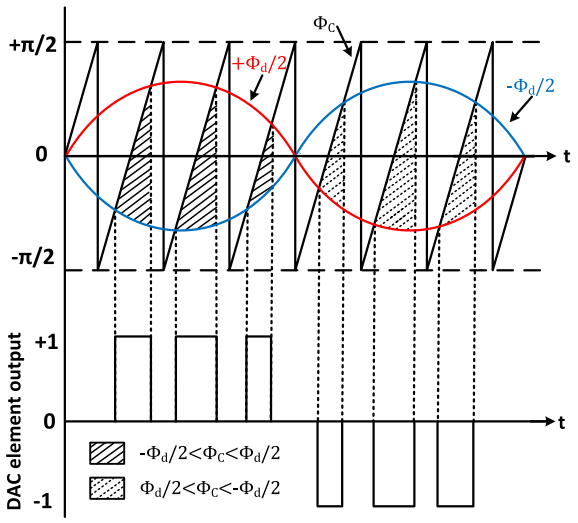


Fig. 15. TD representation of (3).

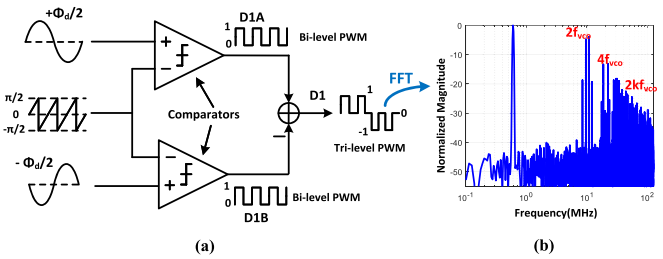


Fig. 16. (a) Equivalent voltage-domain model for generating the input of a DAC element. (b) Simulated PSD of a single DAC element input.

center phase, $\phi_c = (\phi_1 + \phi_2)/2$, propagates at a constant common mode frequency, $f_c = (f_1 + f_2)/2$, where f_1 and f_2 are the instantaneous frequencies of the two VCOs. Since the dual VCOs are controlled differentially, f_c is constant and equal to the VCOs' zero-input frequency. The phase difference between the two VCOs is represented as $\phi_d = (\phi_1 - \phi_2)$. Since the XOR PD can only recognize a maximum phase difference of π, for ease of analysis we define all phases to be bounded within $-\pi/2$ to $\pi/2$. The tri-level DAC elements are uniformly arranged around the phase circle. As we use 15 VCO stages in this prototype, 15 DAC elements are drawn here for consistency. At any sampling instant, only those DAC elements which lie in between ϕ_1 and ϕ_2 are selected. For the sake of representation, the following sign convention is adopted: if VCO1 leads VCO2, the output of the selected tri-level DAC elements is represented by 1; if VCO1 lags VCO2, then the output of the selected DAC elements is denoted by -1; and the DAC elements which are not selected are their output is denoted by 0. Now, let us consider DAC1 in Fig. 14. DAC1 output can be represented as follows:

$$\text{DAC1} = \begin{cases} 1 & \text{when } \phi_1 > 0 \text{ and } \phi_2 < 0 \\ -1 & \text{when } \phi_1 < 0 \text{ and } \phi_2 > 0 \\ 0 & \text{otherwise.} \end{cases} \quad (2)$$

Substituting $\phi_1 = \phi_C + (\phi_d/2)$ and $\phi_2 = \phi_C - (\phi_d/2)$ in (2), the expression for DAC1 can be rewritten as follows:

$$\text{DAC1} = \begin{cases} 1 & \text{when } \phi_d/2 < \phi_c < \phi_d/2 \\ -1 & \text{when } \phi_d/2 < \phi_c < -\phi_d/2 \\ 0 & \text{otherwise.} \end{cases} \quad (3)$$

The TD representation of $\phi_d(t)/2$, $-\phi_d(t)/2$ and $\phi_C(t)$ is plotted in Fig. 15. The shaded area is where the inequalities in (3) are satisfied, and the output of DAC1 will be set to the corresponding level. The generation of DAC1 waveform can be equivalently modeled by the operations, as shown in Fig. 16(a). The saw-tooth wave in Fig. 16 represents $\phi_C(t)$. This model is well matched with the PWM generation mechanism. Thus, the output of a unit element DAC1 [shown as D1 in Fig. 16(a)] can be thought of as the subtraction of two PWM waveforms, D1A and D1B. D1A and D1B are obtained by comparing the saw-tooth waveform $\phi_C(t)$ with $\phi_d(t)/2$ and $-\phi_d(t)/2$, respectively. D1A and D1B are bi-level waveforms (either 1 or 0). D1 = (D1A–D1B) is a tri-level waveform which can take values of {1, 0, −1}. Using the properties of pulsewidth modulation, we infer that the spectrum of D1A, D1B, and D1 consists of tones centered around $kf_{\text{saw}}(k = 1,2,3\ldots)$, where $f_{\text{saw}}(= 2f_c)$ is the frequency of the saw-tooth waveform. Fig. 16(b) shows the output spectrum of a single DAC element as obtained from behavioral simulation of the proposed DSM, from which we confirm that tones are observed at even multiples of the VCO center frequency.

Fig. 17(a) shows the equivalent voltage-domain model for the complete DAC input generation, which essentially is also the voltage-domain equivalent of the PEQ. The spectrums of all unit elements have PWM tones of the same magnitude but with evenly spaced phase offsets. In the absence of any

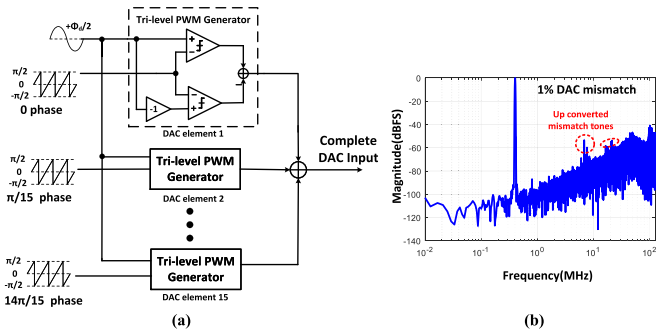


Fig. 17. (a) Equivalent voltage-domain model of the complete DAC input generation. (b) Simulated PSD of the DSM output with 1% DAC element mismatch.

mismatch between DAC unit elements, when the spectrums of all DAC unit elements are added, the vector sum of the PWM tones is zero. Thus, the up-converted PWM tones do not appear in the DAC output spectrum in absence of mismatch between DAC unit elements. However, in presence of static mismatch between DAC unit elements, the DAC's output spectrum will show some residual tones at $2f_c, 4f_c, 6f_c$, and so on, as shown in Fig. 17(b). This explains how static mismatch in DAC unit elements are pulsewidth modulated to even multiples of the VCO's center frequency, thereby performing intrinsic CLA.

V. Proposed ADC Design

A. Top-Level Overview

The simplified top-level schematic of the proposed VCO-based CTDSM is shown in Fig. 18. It adopts the dual-VCO phase-output architecture, which provides superior forward path linearity due to minimum VCO input swing and the cancellation of the VCO's even-order non-linearity. The differential input voltage is first turned into current by R_{in} and subtracted by the DAC current before being fed into two 15-stage current-starved VCOs, or simply CCOs. The CCOs perform current-frequency translation as well as the inherent frequency to phase integration. Sense amplifier flip flops (SAFFs) are used to sample each node of the CCOs. The current-controlled oscillator (CCO) nodes are buffered before being sampled to prevent the large kick-back noise of the comparator in the SAFFs from corrupting the phase. The topology of the CCO delay cell and buffer cell are both pseudo differential inverter pairs as shown in the red circle in Fig. 18, as such structure provides better immunity against clock feed-through and kick-back noise from the SAFFs as well as removes the need for an extra reference level for the SAFF. The sampled phases of the 2 CCOs are then processed by the PEQ to quantize the phase difference as a thermometer code (D [14:0]) and, importantly, to extract the lead-lag status (sign). The quantized phase difference is then multiplied with the sign to generate tri-level controls (S_{+1}, S_0, and S_{-1}) that govern the tri-level RDAC operation.

Since the CCO's input is physically the supply rail of an inverter chain, as shown in Fig. 18, it has non-zero small-signal impedance. Therefore, the feedback node is not a "true virtual ground" in this paper. Note that such feedback configuration can be problematic when the quantizer resolution is low. As the input impedance of the CCO is non-linear, sufficiently large voltage ripple on the feedback node may drastically change the impedance and modulate the feedback factor, resulting in noise fold back and even instability. In this paper, thanks to the PEQ which provides a 30-level quantization, the voltage ripples at the feedback node is highly suppressed ($\sim$20 mV_{PP}). The CCO input impedance functions sufficiently linear under this amount of perturbation, thus does not cause major impact on the performance of the modulator. The CCOs' current-to-frequency tuning gain non-linearity is also suppressed by the same mechanism. An imperfect virtual ground may also modulate with the output impedance of a multi-bit RDAC that are input dependent, causing distortion in the feedback current. Since the tri-level RDAC in this paper adopts "reference side switching," its output impedance is constant. Hence, the proposed RDAC does not suffer from this issue.

The mismatch between the dual VCO can also be a source of performance degradation. The center frequency mismatch manifests as a constant offset, which degrades signal swing of the modulator. The mismatch in the tuning curve will lead to even-order non-linearity "leaking through." Nevertheless, simulation reveals that it requires about 30% mismatch in center frequency and tuning curve coefficients between the two CCOs to introduce 1 dB degradation in DR. In practice, the mismatch is usually less than 10% for carefully laid out VCOs. Therefore, the degradation due to mismatch is expected to be minor.

B. Implementation of the PEQ

The detailed implementation of the PEQ is also shown in the highlighted area of Fig. 18. XOR1 serves as the conventional PD, which outputs the magnitude of the phase difference. An XNOR gate (XNOR2) is inserted between adjacent CCO_P nodes to detect the transition point of CCO1 and produce pointer $\overrightarrow{tp1}$. Adjacent XOR1 outputs are also fed to AND1 to detect the front edge of D [14:0], generating pointer $\overrightarrow{fe}$. For simplicity, the adjacent wirings are represented as "shift right" operation in the schematic. AND2 and OR_SUM then compute the dot product of $\overrightarrow{tp1}$ and $\overrightarrow{fe}$, as previously described in Fig. 8, to extract the lead-lag status. To be precise, when there is alignment between $\overrightarrow{tp1}$ and $\overrightarrow{fe}$, AND2 will produce a bit stream that contains a logic "1," where the "1"s location indicates the alignment point. If there is no alignment between TP1 and FE, AND2 will produce a string that contains only logic "0." We then use a one-hot adder, which is simply OR logic, to check whether the AND2 output contains logic "1" and produce the lead-lag indicator sign. As mentioned in Section III, when CCO_P leads CCO_N, sign is designated high, and vice versa. The Tri-level Gen block then combines the D [14:0] and sign to create the DAC control signals.

C. Implementation of the Tri-Level RDAC

The DAC adopts the non-return-to-zero (NRZ) scheme. Although return-to-zero (RZ) scheme can alleviate dynamic error, it has a much worst jitter tolerance and does not work

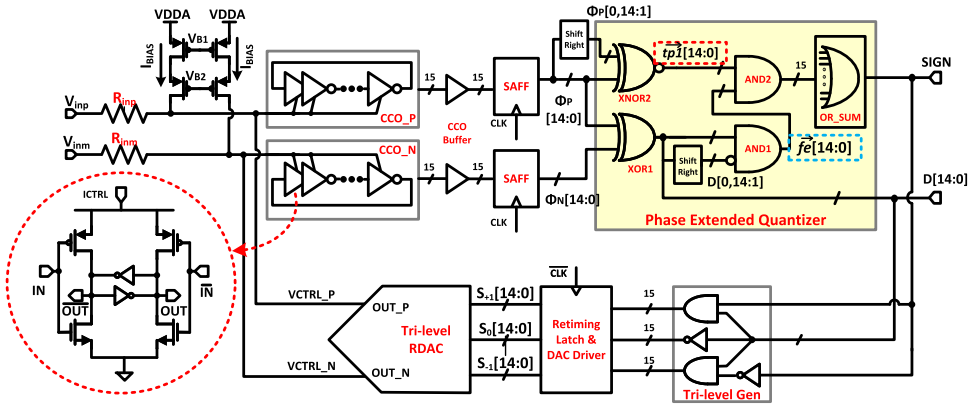


Fig. 18. Top-level schematic of the proposed VCO-based CTDSM.

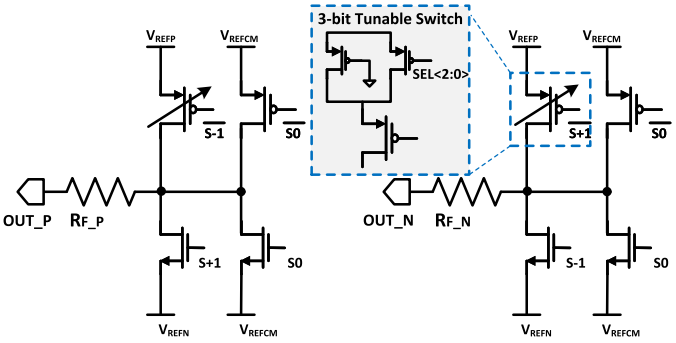


Fig. 19. Schematic of the tri-level RDAC.

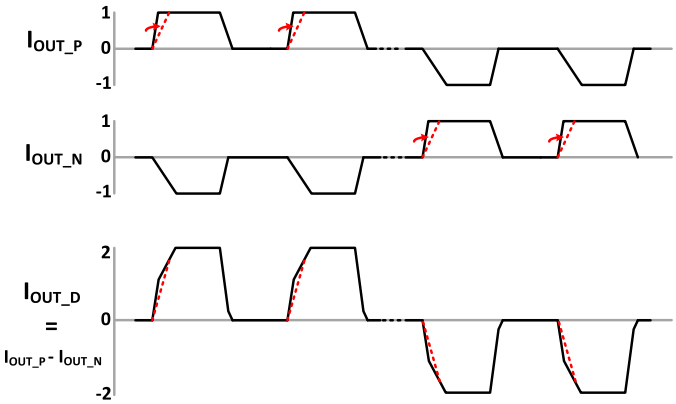


Fig. 20. Illustration of dynamic error tuning in the proposed tri-level RDAC.

well without a virtual ground due to its pulsing nature. The schematic of a tri-level RDAC element is presented in Fig. 19. Depending on the combination of D and sign, one side of the resistors will be switched between V_{REFP}, V_{REFCM}, and V_{REFN} to provide proper feedback current. While the switches connecting to V_{REFP} and V_{REFN} are single-type, the switches for V_{REFCM} are designed as complementary to compensate for the low overdrive voltage at this state, such that they can provide lower resistance and balance the rising and falling speed. Although in practice it is hard to enforce the on-resistance of all three switches to be identical, 20% to 30% of variation can be tolerated under fully differential structure for a spurious-free dynamic range (SFDR) target of 90 dB.

While a fully differential bi-level DAC is low in dynamic error as the rising and falling transition is intrinsically symmetrical with careful design [26], a tri-level DAC loses this advantage due to an extra reference level. Fig. 20 illustrates both the single-ended and differential output pulses of a tri-level DAC with exaggerated transition imbalance. Although the positive and negative pulse shape is symmetrical for the differential output (assuming no mismatch between the two single-ended outputs), the rising and falling of a pulse can still be quite imbalance. To guarantee sufficiently small dynamic error over process variation, the PMOS switches for V_{REFP} are designed to be tunable. As shown in Fig. 20, the strength of the "0 to 1" transition is sufficient to affect the "rising" of a differential pulse and make it match better to the "falling," leading to reduction of dynamic error. The strengths of these switches are adjusted by digitally controlled MOS resistors connected in series, as illustrated in Fig. 19. The tuning is applied globally. A one-time calibration is performed externally to set the value for the switch control for optimum signal-to-noise-and-distortion ratio (SNDR).

To achieve a total harmonic distortion lower than −85 dB, the in-band output impedance of the reference buffer for V_{REFP} is required to be below 5 Ω given the RDAC resistance in this paper. The impedance requirement for V_{REFCM} is much more relaxed as it does not supply any differential signal-related current. In this design, the reference generators for the RDAC are not implemented on chip.

D. Thermal Noise Analysis and Jitter Tolerance

Four components contribute to the thermal noise of this CTDSM: the input $V-I$ resistor R_{in}, the feedback RDAC, the CCO biased current source, and the CCO. Since the operation of the proposed work is current-domain oriented, we thereby compute the input referred noise current. The noise current from R_{in}, the RDAC and the CCO bias current source adds directly to the input. The noise contribution from R_{in} and the RDAC in total is equal, and their noise current power spectral density (PSD) is given by $4\,kT/R$. The noise current for the CCO bias is given by $4\,kT\gamma\,g_m$, where g_m is the transconductance of the output tail device. The calculated differential noise PSDs for R_{in}, the RDAC and the CCO bias are 2.88 pA/$\sqrt{\mathrm{Hz}}$, 2.88 pA/$\sqrt{\mathrm{Hz}}$, and 3.2 pA/$\sqrt{\mathrm{Hz}}$, respectively. The VCO phase noise is −118 dBc/Hz at 1 MHz offset, which translates to 4.3 pA/$\sqrt{\mathrm{Hz}}$ of input referred noise [17], [27]. With this, we have a total input referred noise of 8.5 pA/$\sqrt{\mathrm{Hz}}$. Assuming a 2 MHz bandwidth and 2.2 V_{pp}

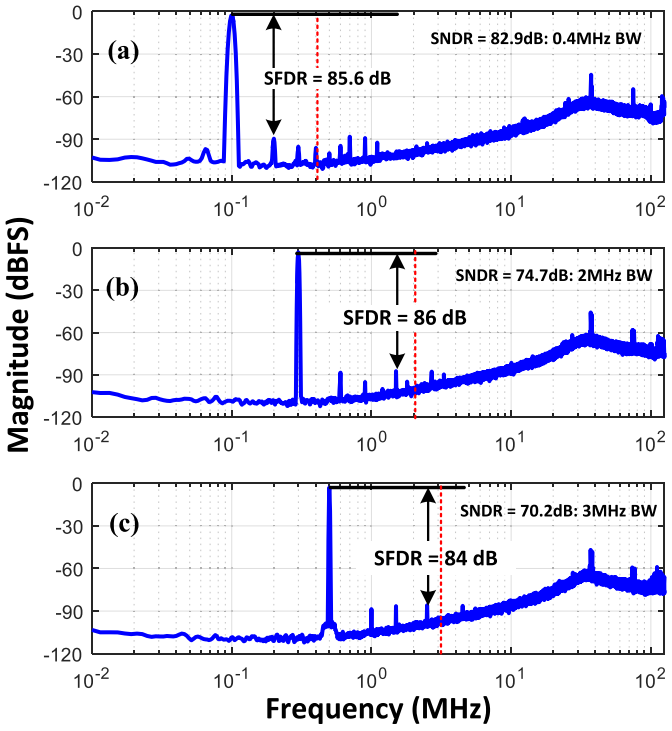


Fig. 21. Measured 2^{17}-point, 16×-averaged output PSD for (a) 100 kHz, (b) 300 kHz, and (c) 500 kHz input tones.

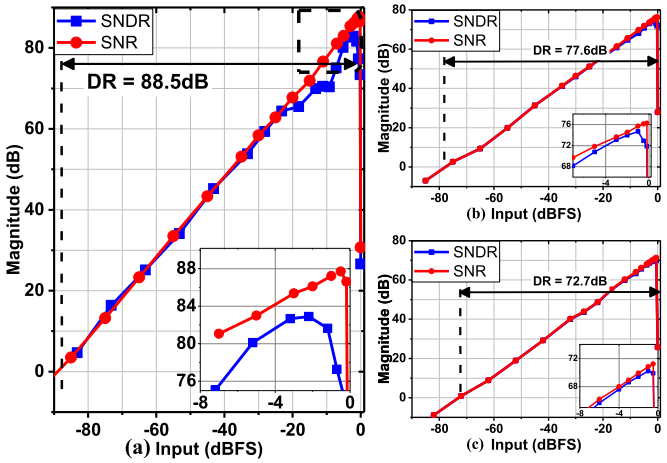


Fig. 22. Measured SNDR/SNR vs input for (a) 0.4 MHz BW, (b) 2 MHz BW, and (c) 3 MHz BW.

(equivalently $550\mu A_{pp}$) full scale input, the peak SNR limited by thermal noise is 86 dB. The calculated SNR at 0.5 MHz is 92 dB, which is well matched with the measured DR.

Similar to voltage-domain CTDSMs adopting the multi-level NRZ scheme, this design has a relatively good jitter tolerance. Simulation indicates that when sampling at 250 MHz and with 40 ps rms clock jitter, the jitter-limited signal to noise ratio of this work is 78.5 dB for 2 MHz bandwidth. This number matches well with the calculation results using the model provided in [28]. The TD nature and the use of PEQ in this work does not degrade the jitter tolerance.

VI. Measurement Results

The proposed work was fabricated in 130 nm 1P8M CMOS process and occupied an active area of 0.13 mm^2. Running

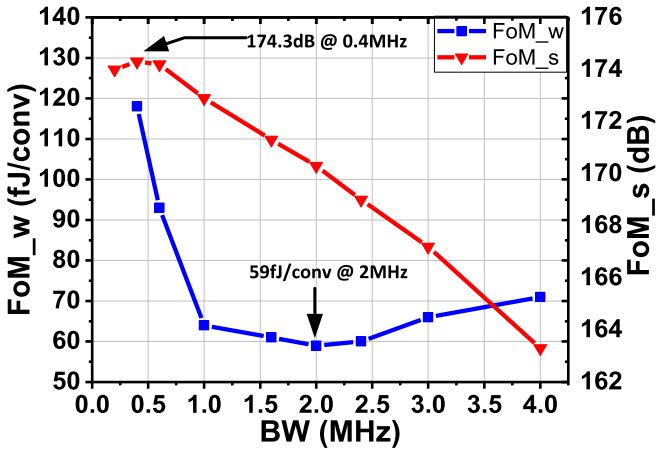


Fig. 23. Measured Walden (blue) and DR-based Schreier (red) FoM versus BW.

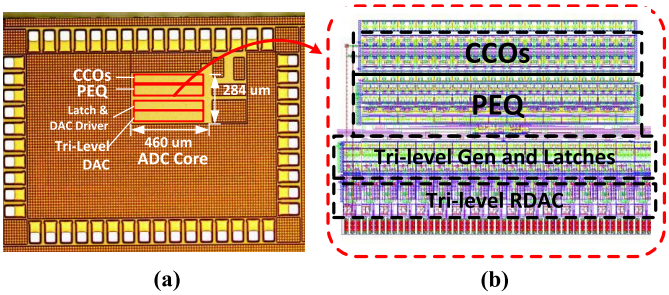


Fig. 24. (a) Die photograph. (b) ADC core layout.

at 250 MS/s, it consumes 1.05 mW under 1.2 V with full input signal swing, out of which 0.78 mW is from digital and 0.27 mW is from analog (including CCO and DAC reference power). The nominal voltage of V_{REFP}, V_{REFCM}, and V_{REFN} are 1.2, 0.6, and 0 V, respectively. The measured output PSD is shown in Fig. 21 for 100, 300, and 500 kHz input tones, respectively. The SFDR is over 84 dB across different input cases. The SNDR and SNR versus input magnitude plots for three different bandwidths are shown in Fig. 22. The best DR performance is obtained at 0.4 MHz bandwidth. We are able to reach 88.5 dB DR, which corresponds to a 174.3 dB peak DR-based Schreier FoM. The plot of FoM versus bandwidth is shown in Fig. 23. Best Walden FoM of 59 fJ/conv with SNDR of 74.7 dB is achieved at 2 MHz. We believe that the linearity may be limited by the incomplete removal of the DAC dynamic error. Another potential cause for the observed tones may stem from the systematic mismatch between the differential half DAC cells, which reduces the ADC's tolerance on the resistance variation in the reference switches.

The die photo of the prototype is presented in Fig. 24. The dynamic power saving mechanism is also validated. Measured power as a function of input amplitude is plotted in Fig. 25. We can see that the total power drops from 1.05 to 0.6 mW when the input goes from full scale to −40 dBFS, achieving a 40% reduction. The detailed power breakdown of −1 and −40 dBFS cases are also shown in Fig. 24. We can see that the DAC power is reduced by about 2.6 times while digital power dropped nearly by half.

TABLE I

PERFORMANCE SUMMARY AND COMPARISON TO STATE-OF-THE-ART CTDSMs

	Architecture	Process (nm)	Area (mm^2)	Fs (MS/s)	Power (mW)	BW (MHz)	SNDR (dB)	DR (dB)	FOM_w* (fJ/conv.)	FOM_s1** (dB)	FOM_s2*** (dB)
[7]	OTA+VCO	130	0.45	900	87	20	78	80	330	162	164
[10]	VCO	65	0.075	1300	11.5	5.08	75	78	246	161	164
[12]	PWM+VCO	90	0.1	640	4.3	8	59.1	65.6	366	151.8	158.3
[13]	OTA+VCO	90	0.36	600	16	10	78.3	83.5	120	166.3	171.5
[15]	VCO	90	0.16	640	4.1	5	74.7	77	92	165.6	167.9
[16]	OTA+VCO	65	0.49	1280	38	50	64	75	294	155.2	166.2
[17]	VCO	130	0.03	300	1.75	2	66.5	70	250	157.1	160.6
[18]	VCO	130	0.04	250	0.91	1.67	70.6	74	98	163.2	166.6
[19]	OTA+VCO	65	0.5	1200	54	50	71.5	72	176	161.2	161.7
[29]	OTA+SAR	40	0.051	65	1.91	1.92	79.6	83.4	64	169.6	173.4
[30]	OTA+TDC	90	0.12	300	4.3	8.5	67.2	69.3	135	160.1	162.2
[31]	OTA+Flash	130	0.33	256	5	2	74.4	82	291.4	160.4	168
[32]	TIA+Flash	40	0.085	246	2.8	1.92	78	83	110	166.4	171.4
[33]	OTA+Flash	180	0.99	57.6	21	0.6	90	-	678.2	164.6	-
This work	**VCO**	**130**	**0.13**	**250**	**1.05**	**0.4**	**82.9**	**88.5**	**118**	**168.7**	**174.3**
						2	**74.7**	**77.6**	**59**	**167.5**	**170.4**
						3	**70.2**	**72.7**	**66.2**	**164.8**	**167.3**

**FoM_w = Power/(2^{ENOB}*2*BW)*
***FoM_s1 = SNDR + 10*log10(BW/Power)*
****FoM_s2 = DR + 10*log10(BW/Power)*

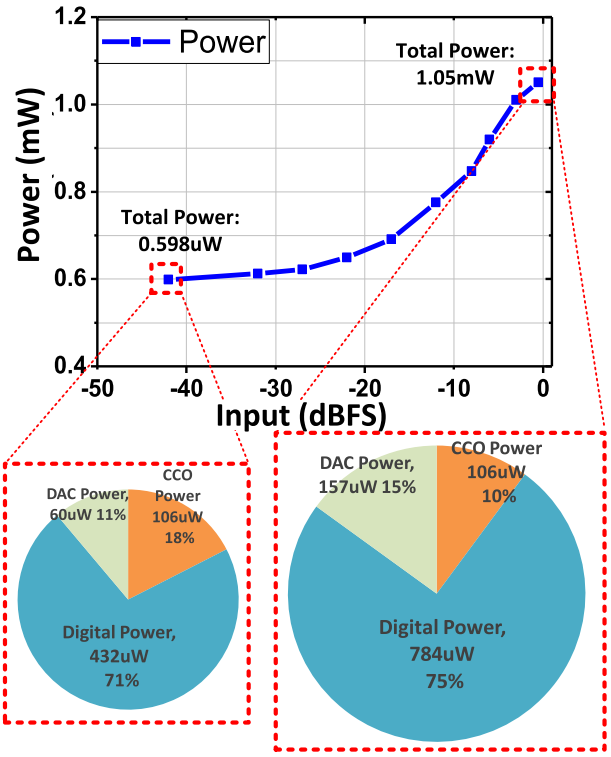


Fig. 25. Measured power versus input amplitude.

A comparison with existing VCO-based CTDSMs, as well as non-VCO-based CTDSMs with similar bandwidth is provided in Table I. It demonstrates that the performance of this paperis on-par with state-of-the-art CTDSMs. To the authors' best knowledge, it outperforms all existing VCO-based ΔΣ ADCs in dynamic-range-based Schreier FoM, achieving a 2.5× power efficiency improvement, despite the relatively old 130 nm process. We strongly believe that the scaling-friendly nature will bring substantial performance improvement for our ADC in advanced processes.

VII. CONCLUSION

This paper presents a CT VCO-based DSM with the highlight of a power efficient, resolution doubling PEQ and tri-level RDAC. The techniques introduced are mostly digital and scaling-friendly. Our work not only maintains the merits of prior phase-output VCO-based CTDSMs, but also addresses their limitation in the quantizer power efficiency as well as reducing DAC power, and advances state-of-the-art with a dynamic-range-based FoM of 174.3 dB. A prototype chip was fabricated in 130 nm technology, with measurement results demonstrating the high performance brought by the proposed techniques. The scaling friendly and dynamic power saving nature of the proposed ADC makes it a very good candidate for future SoC, mobile, or IoT applications in advanced technology nodes.

ACKNOWLEDGMENT

The authors would like to thank the MOSIS Educational Program for supporting chip fabrication.

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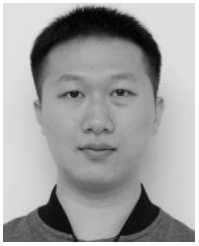

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