

A 144-MHz Fully Integrated Resonant Regulating Rectifier With Hybrid Pulse Modulation for mm-Sized Implants

Chul Kim, *Student Member, IEEE*, Sohmyung Ha, *Member, IEEE*, Jiwoong Park, *Student Member, IEEE*, Abraham Akinin, *Student Member, IEEE*, Patrick P. Mercier, *Member, IEEE*, and Gert Cauwenberghs, *Fellow, IEEE*

Abstract—This paper presents a fully integrated resonant regulating rectifier (IR^3) with an on-chip coil used to wirelessly power mm-sized implants. By combining rectification and regulation in a single stage, and controlling this stage via a hybrid pulse-width modulation and pulse-frequency modulation (PFM) feedback scheme, the IR^3 avoids efficiency-limiting cascaded losses while enabling tight voltage regulation with low dropout and ripple. The IR^3 is implemented in 0.078 mm^2 of active area in 180-nm Silicon oxide insulator (SOI) CMOS, and achieves a $1.87\% \Delta V_{DD}/V_{DD}$ power supply regulation ratio with a 1-nF decoupling capacitor despite a tenfold load current variation from 8 to $80 \mu\text{A}$. A 0.8-V V_{DD} is maintained at a $8\text{-k}\Omega$ load for 144-MHz RF inputs ranging from 0.98 to 1.5 V. At 1-V regulation, the voltage conversion efficiency is greater than 92% with less than 5.2-mV_{pp} ripple, while the power conversion efficiency is 54%. The measured overall wireless power transfer system efficiency, from the primary coil to V_{DD} output of the IR^3 , is 2% at $160\text{-}\mu\text{W}$ load, and reaches 5% at $700 \mu\text{W}$.

Index Terms—mm-sized implant, on-chip coil, pulse-frequency modulation, pulse-width modulation (PWM), regulating rectifier, wireless power transfer (WPT).

I. INTRODUCTION

MINIATURIZED, highly energy-efficient wireless power transfer (WPT) integrated circuits are critical components in the development of fully encapsulated implanted brain–computer interface systems that will, through additional advances in improved spatial resolution and coverage of neural recording and stimulation electrodes, enable the

Manuscript received December 13, 2016; revised April 4, 2017 and June 8, 2017; accepted July 24, 2017. Date of publication August 21, 2017; date of current version October 23, 2017. This paper was approved by Associate Editor Yogesh Ramadas. This work was supported in part by the University of California (UC) Multicampus Research Programs and Initiatives, in part by the DARPA NESD Program, and in part by the UC San Diego Center for Brain Activity Mapping. (Corresponding author: Chul Kim.)

C. Kim, A. Akinin, and G. Cauwenberghs are with the Department of Bioengineering, University of California at San Diego, La Jolla, CA 92093 USA (e-mail: chk079@ucsd.edu).

S. Ha was with the Department of Bioengineering, University of California at San Diego, La Jolla, CA 92093 USA. He is now with the Electrical and Computer Engineering Division of Engineering, New York University Abu Dhabi, Abu Dhabi 129188, United Arab Emirates.

J. Park and P. P. Mercier are with the Electrical and Computer Engineering Department, University of California at San Diego, La Jolla, CA 92093 USA.

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2017.2734901

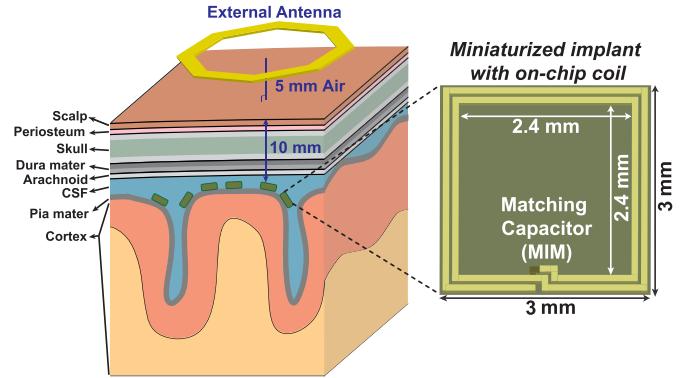


Fig. 1. Transcutaneous wireless power delivery to mm-sized distributed implants on the cortical surface, each with an integrated power RX coil.

next-generation neuroscience and neurology experimentation. As an example, modular mm-sized wireless implants, which lie directly on the cortical surface, as shown in Fig. 1, can support more accurate recording of local brainwaves and a higher spatial resolution ($\leq 1 \text{ mm}$) than conventional electrocorticography (ECoG) approaches [1], [2]. In addition to spatial coverage and density benefits, recent studies have suggested that small devices can reduce the incidence of tissue inflammation, astroglial scarring, and cell death [3]–[6], thereby underscoring the need to miniaturize implants.

Since the size of miniaturized implanted devices is often limited by the size of the embedded WPT coil and corresponding power management and energy-storage circuitry, significant research efforts have been directed at reducing the size of such components. For example, it has been shown that increasing the RF carrier frequency used for WPT can yield a reduction in receiver size [7]–[11], since a higher resonant frequency: 1) increases induction via a higher rate of incident magnetic flux over a small receiving (RX) coil [12], [13]; 2) increases the quality factor (Q) of both power transmitting (TX) and RX coils [6], [12]; and 3) reduces the area required of the resonant matching capacitor.

On the other hand, tissue absorption of electromagnetic waves increases with frequency, resulting in additional tissue losses that ultimately limit the efficiency of WPT. Making matters worse, increased tissue absorption also limits the amount of allowable transmit power due to regulations on

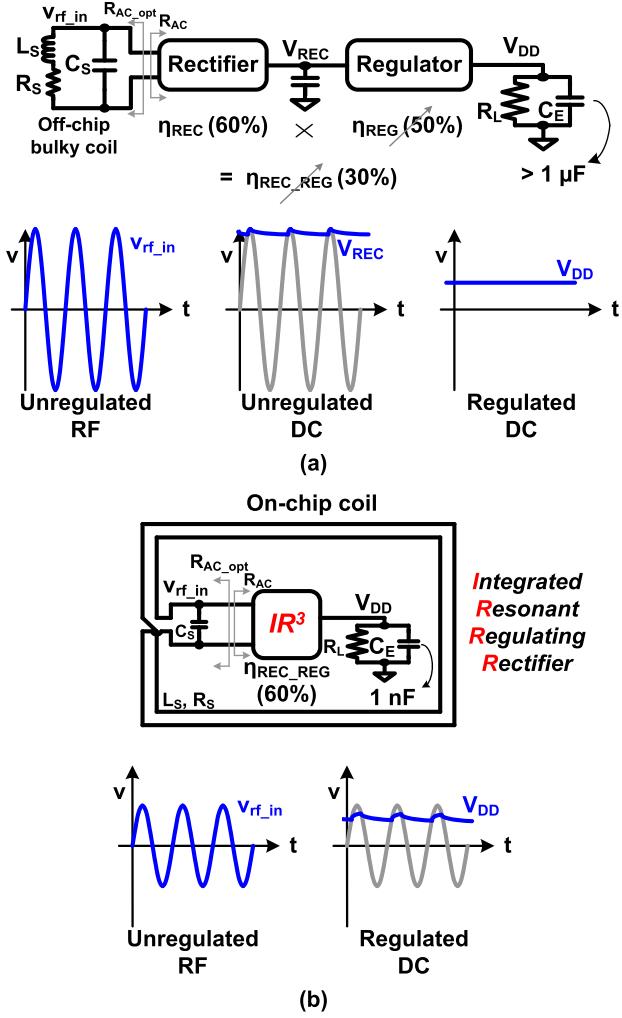


Fig. 2. Rectification and regulation methodology comparison; (a) Conventional separate rectification and regulation conversion. (b) Integration of rectification and regulation for one-step conversion without cascaded loss in PCE and voltage conversion efficiency (VCE).

the specific absorption rate (SAR) of RF power in human tissue. Balancing of these considerations leads to optimal resonant frequencies in the 100 MHz–1 GHz range under various conditions, enabling the design of mm-sized implants that can efficiently receive sufficient power to operate load circuits under SAR constraints [6], [12]–[15].

The pursuit of implant miniaturization also requires research on miniaturizing the rest of the power management and energy storage circuitry. For example, the most conventional wirelessly powered implants utilize a segmented architecture, where the WPT coil is physically separated from the rectifying and regulating circuits. Such an approach requires complex interconnect, packaging, and discrete components that occupy unwanted volume and increase cost [12].

To address these issues and enable further miniaturization of wirelessly powered implants, this paper presents the design of a fully integrated resonant regulating rectifier (IR³) that performs voltage and power conversion from an integrated 3 mm × 3 mm on-chip coil to loads; no external components are required for operation. By combining rectification and regulation into a single stage, as shown in Fig. 2(b),

the proposed IR³ eliminates the conventionally required inter-stage decoupling capacitance, saving significant volume and eliminating cascaded losses for high efficiency. A hybrid pulse modulation (HPM) control scheme is also proposed to enable power efficient rectification and regulation over a large range of RF input amplitude and load current.

Simplified circuit schematics and initial measurement results of the IR³ were presented in [16]. This paper presents analysis and optimization of system-level parameters, significantly more detailed circuit schematics, and measurements and characterization of IR³ performance under varying input and load conditions. This paper is organized as follows: limitations of conventional segmented architectures motivating the integration of resonant rectification and regulation are discussed in Section II. The proposed operation of IR³ with hybrid pulse-frequency modulation and pulse-width modulation (PWM) is outlined in Section III, with circuit details elaborated in Section IV, and simulated and measured results presented in Section VI. Finally, the conclusions are given in Section VII.

II. ARCHITECTURAL CONSIDERATIONS

The purpose of this section is to show that performing combined rectification and regulation with an integrated coil is not only advantageous from a size perspective, but that merging these two functions into a single stage has tangible system-level efficiency benefits. To demonstrate this, we first show that to maximize overall system efficiency in mm-sized systems, it is necessary to maximize not only power conversion efficiency (PCE), but also VCE. Then, we show how maximizing both VCE and PCE in conventional cascaded systems is difficult while attaining high efficiency can be more easily achieved by merging rectification and regulation.

A. Importance of Voltage and Power Conversion Efficiency

The WPT system efficiency (WSE, the net power gain from the transmitted power at the TX coil to the RX load after the regulation) and the magnitude of power delivery to the load are limited by the size of the RX coil [12], [13]. Furthermore, in the case shown in Fig. 1, where multiple implants receive power from a single external power transmitter, it is infeasible to control the received power level at each implant individually by adjusting the shared transmitted power. As such, the spread in distances between the external transmitter and the implants (and thereby, the range of coupling coefficients) becomes an efficiency limiting factor. Therefore, particularly, for multiple mm-sized WPT implants with on-chip coils, it is important to maximize both the WSE and magnitude of delivered power. It can be shown that, to a first order, maximum efficiency and maximum power in a WPT system, when operating at low coupling coefficients, k , are achieved at the same optimal load of the secondary LC tank, R_{ac_opt} [17]. Specifically

$$R_{ac_opt} \approx \frac{L_S}{C_S R_S} \approx Q_{coil}^2 R_S \quad (1)$$

where L_S , C_S , and R_S are inductance and capacitance of the secondary LC tank, and the parasitic series resistance of the RX coil as shown in Fig. 2. Q_{coil} is $\omega_o L_S / R_S$, where $\omega_o \approx 1/(L_S C_S)^{1/2}$ at the parallel tuned LC tank.

By a series-to-parallel impedance transformation [18], [19], the output impedance of the parallel tuned LC tank is the same R_{ac_opt} . Hence, both the efficiency and the amount of power are maximized through *impedance matching* between the receiver LC tank and the subsequent IR³ circuitry. Several recent designs control matching capacitance or inductance in the secondary LC tank to adjust R_{ac_opt} according to (1), either to improve power transfer efficiency [7], [20] or to increase the amount of power delivery [17]. These improvements come at the expense of some additional implant area and power loss due to the addition of series switches connecting to several separate capacitors in parallel or the inductor in series.

The IR³ equivalent input resistance, R_{ac} shown in Fig. 2, can be found by relating the ac power consumption at its input $P_{in} = v_{rf_in_peak}^2/2R_{ac}$, where $v_{rf_in_peak}$ is the peak voltage in the secondary LC tank, to the output dc power $P_L = V_{DD}^2/R_L$ delivered to a load with resistance R_L . In terms of the PCE, $PCE = P_L/P_{in}$, and voltage conversion efficiency, $VCE = V_{DD}/v_{rf_in_peak}$ of the combined rectifier and regulator, this becomes

$$R_{ac} = \frac{PCE}{2VCE^2} R_L. \quad (2)$$

Equation (2), together with (1), underscore the importance of maintaining high VCE in maximizing overall WSE through impedance matching. Indeed, typical on-chip inductors with quality factor $Q_{coil} = 12$ and series resistance $R_S = 3.5 \Omega$ yield an optimal LC tank load R_{ac_opt} roughly 500Ω . In turn, a typical ECoG application [1], [2] incurs a load $R_L = 2 \text{ k}\Omega$ at $PCE = 0.5$. Under these conditions, the equivalent input resistance R_{ac} (2) is perfectly matched to this optimal load when $VCE = 1$. Conversely, when $VCE = 0.2$, R_{ac} becomes $12.5 \text{ k}\Omega$, substantially off from the optimal load R_{ac_opt} . Hence, in general, mm-sized WPT receivers with less than 1-mW dc load require not only high PCE, but also high VCE.

B. Limitations of Conventional Cascaded Rectification and Regulation

Achieving both high PCE and high VCE is challenging with conventional WPT receivers, which employ a cascaded two-step conversion approach: RF-dc rectification followed by dc regulation. For rectification, the simplest design is a passive rectifier built with diode-connected MOS transistors, although at low PCE and VCE due to an inherent V_{TH} voltage drop across the diodes. Alternatively, active rectifiers with high-speed comparators for active low-voltage diodes yield improved VCE, as well as PCE [21]. Both the passive and active rectifier operate, essentially, by tracking the envelope of the RF input and pulling up the output voltage whenever it is lower. As such, the rectified output tends to the peak voltage of the RF input *regardless of the required output voltage*. Hence, variations in the received RF input amplitude due to changes in coupling conditions (and thereby, coupling coefficient) between the TX and RX coils during movement require regulation of the rectified voltage for stable operation of the implant circuits. A conventional WPT receiver accomplishes this through a separate additional regulation stage.

For this purpose, low-dropout (LDO) regulators have been widely adopted [1], [7]–[9], [22].

The separation between rectification and regulation functions incurs several inefficiencies as shown in Fig. 2(a). To support this two-step conversion, two large supply-decoupling capacitors are required before and after regulation to reduce voltage ripple and improve regulation feedback stability. Full on-chip integration of two large capacitors in an mm-sized implant is prohibitive not only because of the large silicon area required, but also because of eddy currents induced by the RF magnetic field in large solid metal planes, which substantially reduce WSE. High-speed LDO regulators permit lowering the size of the two decoupling capacitors [22], though this is achieved by increasing the bandwidth of the LDO and, therefore, quiescent power consumption.

In addition, the cascaded rectification-regulation two-step conversion leads to multiplicative losses in conversion efficiencies: $\eta_{REC_REG} = \eta_{REC} \times \eta_{REG}$, both for VCE and PCE. This is particularly problematic with LDO linear regulators for which both VCE_{REG} and PCE_{REG} are limited by the ratio of regulated to rectified voltage

$$PCE_{REG} \leq VCE_{REG} = \frac{V_{DD}}{V_{REC}} \quad (3)$$

which can be arbitrarily low depending on RF input conditions. In the case of a single implant, regulator efficiencies can be improved by dynamically adjusting the transmitted RF power at the external antenna to control V_{REC} slightly greater than V_{DD} [10], [11]. However, in the case of multiple implants as shown in Fig. 1, the minimum level of transmitted RF power is set by the weakest link (generally, the farthest implant from the external TX antenna). As a result, a uniformly high VCE and PCE cannot be guaranteed across all implants when using cascaded conversion with LDO linear regulators. Furthermore, it is important to note that the dropout voltage ($V_{REC} - V_{DD}$) is generally greater than a few hundred millivolts and increases its portion as the supply voltage is scaled down [23]. As such, an LDO regulator is the most static power-consuming block in several mm-sized implantable designs [8], [24].

III. INTEGRATED RESONANT RECTIFICATION AND REGULATION

To address the disadvantages of cascaded two-stage conversion, this paper proposes a fully integrated solution to combine rectification and regulation by directly coupling the on-chip resonant tank to the on-chip load via hybrid pulse-width and frequency modulation of the conductive path between the tank and the load.

A. Benefits of Integration

Combination of rectification and regulation functions within a single stage offers greater integration density as well as high efficiencies [16], [25]–[28]. For further improvement in size and efficiencies, the RX coil is also integrated on-chip such that the integrated resonant regulating rectifier (IR³) presented here directly converts the induced RF power at the integrated coil to the regulated dc supply driving on-chip loads

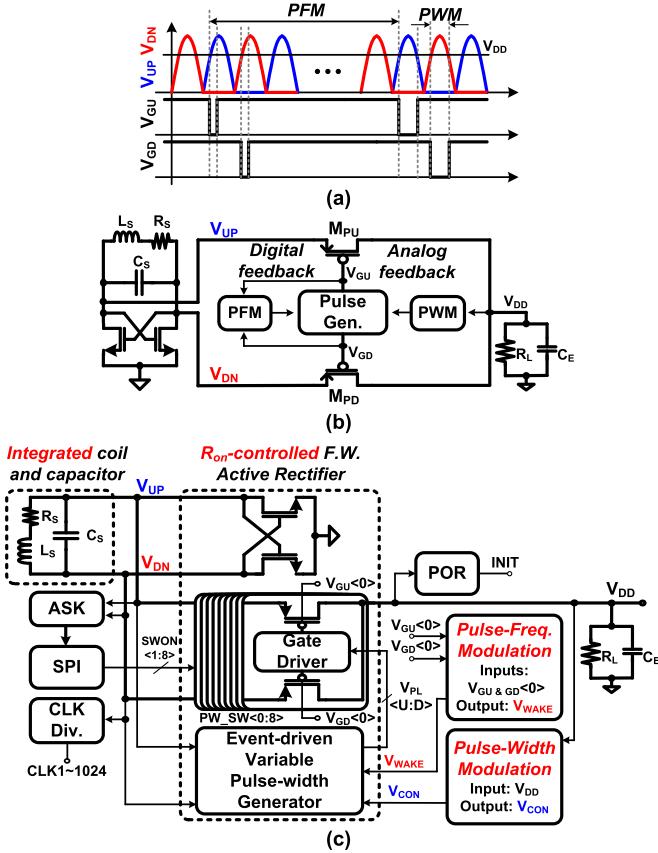


Fig. 3. HPM with combined PWM and pulse-frequency modulation (PFM) for integrated resonant rectification and regulation. (a) Conceptual operation and timing diagram. (b) Analog PWM and digital PFM feedback loops. (c) Block-level IR^3 circuit diagram.

without cascaded losses in overall VCE and PCE, as shown in Fig. 2(b). Hence, the IR^3 is capable of attaining high PCE and VCE not limited by the two-stage inefficiencies in (3). In particular, owing to the improved overall VCE (greater than 90%, Fig. 13) by combining two functions into a single stage, the equivalent input resistance of the IR^3 , R_{ac} , is close to the optimal LC tank load, R_{ac_opt} , leading to the improved overall WSE. While not implemented here, real-time R_{ac_opt} tracking functionality can be included with IR^3 for further improvement in overall WSE.

In addition to removing cascaded losses in efficiencies, full monolithic integration also reduces parasitic capacitance and inductance in the LC tank interfacing to the IR^3 .

To support full integration in an mm-sized implant, decoupling capacitance is reduced to 1 nF, which is adequate for regulation within 5-mV ripple (Fig. 11).

B. Hybrid Pulse Modulation

The IR^3 performs simultaneous rectification and regulation by controlling the amount of power transferred from the RF input to the regulated dc output, V_{DD} , through an HPM scheme that combines PWM and pulse-frequency modulation (PFM), as shown in Fig. 3(a). Each pulse activates a conductive path between the resonant tank and the load, accomplishing both rectification and regulation in one step. For rectification,

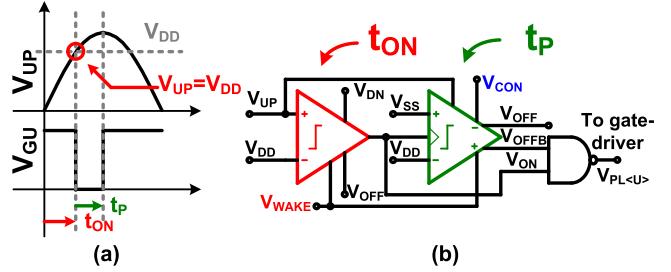


Fig. 4. Event-driven variable pulse-width generator driven by V_{CON} PWM and V_{WAKE} PFM controls. (a) Timing diagram. (b) Simplified circuit diagram. Only the upper half (V_{UP} controlling V_{GU}) of the circuit is shown; the other half (V_{DN} controlling V_{GD}) is identical.

the pulse generator in Fig. 3(b) activates the up-rectifying power PMOS transistor, M_{PU} , by lowering V_{GU} when its RF input, V_{UP} , exceeds V_{DD} . Conversely, the down-rectifying power PMOS transistor, M_{PD} , is activated by lowering V_{GD} when its RF input, V_{DN} , exceeds V_{DD} in the opposite RF phase for full-wave rectification. For regulation, the width of the activation pulse is controlled by PWM through analog feedback [29], and its pulse-frequency is controlled by PFM through digital feedback.

The PWM module regulates V_{DD} simultaneously with rectification, by adjusting the pulse-width based on comparison of V_{DD} with a predefined reference voltage. Owing to large loop gain at dc in purely analog feedback [Fig. 7 and (5)], the PWM mode offers accurate regulation of V_{DD} . However, due to a dominant pole compensation for stability of the analog feedback, the response time of PWM analog feedback is relatively slow: in the range of several hundred microseconds. In addition, due to timing constraints in the rectification of the RF input, pulse-widths themselves are very short: in the range of a few nanoseconds at tank resonant frequencies above 100 MHz.

Hence, considering typical rise and fall times in V_{GU} and V_{GD} in the upper hundreds of picoseconds range, the dynamic range of pulse-width control is very limited, and PWM alone is insufficient for accurate regulation across varying input and output power conditions. Furthermore, narrow pulse-widths prohibit the IR^3 from achieving high PCE at light load conditions.

To address these challenges and provide rapid digital feedback covering wide dynamic range, another PFM regulation loop is included in addition to and in tandem with PWM. The PFM module increases the pulse-frequency of V_{GU} and V_{GD} when either pulse-width being regulated by PWM reaches an upper threshold; conversely, the pulse-frequency is decreased when either pulse-width reaches a lower threshold. As such, PFM together with PWM provides broad-range and rapid regulation and improved PCE at light load conditions [30], [31].

Fig. 3(c) shows the block-level circuit diagram of the IR^3 . The analog output V_{CON} of the PWM module and the digital output V_{WAKE} of the PFM modules control the width and frequency of the pulsed waveforms $V_{PL<U>}$ and $V_{PL<D>}$ driving the gates of up to nine parallel-connected power PMOS transistors. The LC tank recovered clock signal is binary divided to provide various clocks (CLK1–1024) for the entire

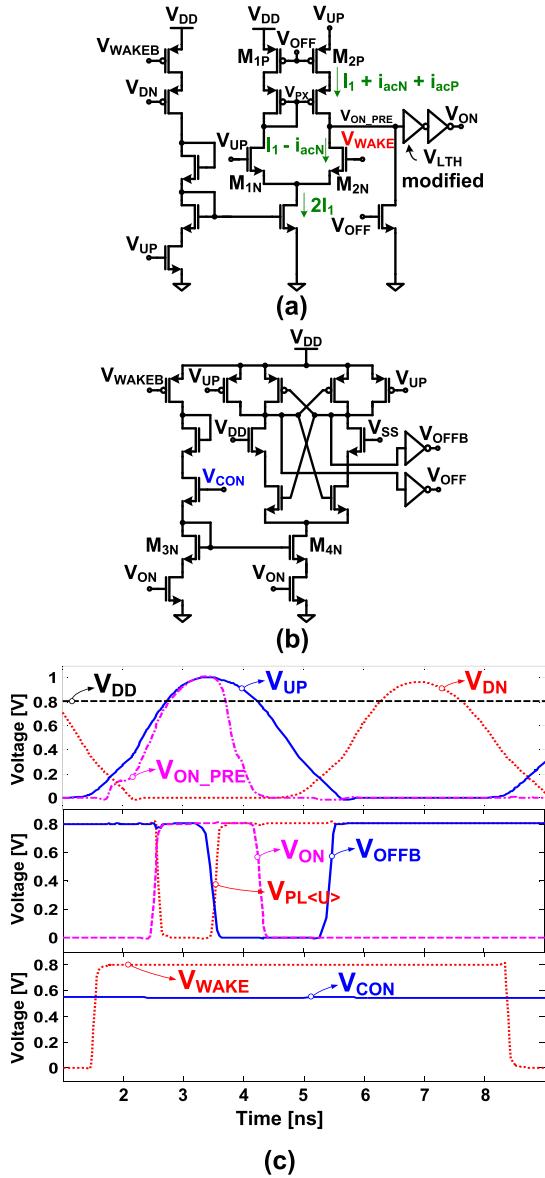


Fig. 5. Circuit implementation of the pulse-width generator in Fig. 4. (a) Event-driven dynamically biased t_{ON} comparator. (b) Triggered variable delay t_P element. (c) Simulated time domain waveforms.

system including the PFM module and other on-chip loads. A power-on-reset generates an INIT signal forcing the IR³ into passive mode with diode-connected PMOS transistors and initializing digital state variables in the PFM module during startup [21]. Circuit implementation and operation of various blocks are detailed in Section IV.

IV. CIRCUIT IMPLEMENTATION

A. Event-Driven Variable Pulse-Width Generator

The schematic of the event-driven variable pulse-width generator is shown in Fig. 4 for half of a cycle (i.e., the positive phase of full-wave rectification). This block produces the pulse waveform $V_{PL<U>}$ from the analog PWM control V_{CON} and event-driven digital PFM control V_{WAKE} shown in Fig. 3(c). It comprises a fast comparator defining the turn-on time,

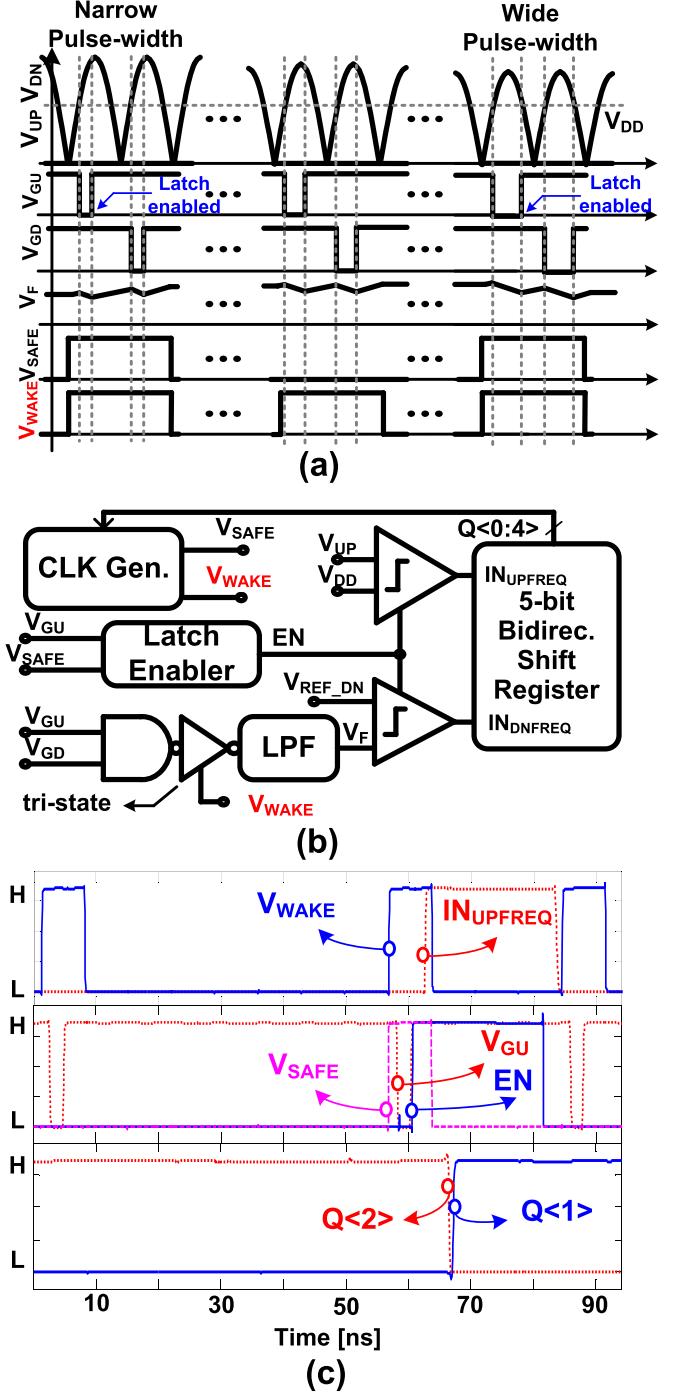


Fig. 6. Pulse-frequency modulation (PFM) module supplying the periodic V_{WAKE} signal gating the pulse generator for rapid digital feedback. (a) Pulse-frequency is decreased at a critically narrow pulse-width reaching a minimum threshold, while pulse-frequency is increased at a critically wide pulse-width, where V_{UP} (or V_{DN}) reaches below V_{DD} . (b) PFM module block diagram. (c) Simulated time domain waveforms of the PFM module when pulse-frequency is increased.

t_{ON} , when V_{UP} exceeds V_{DD} , followed by a triggered (i.e., zero idle power) variable delay element defining the pulse-width, t_P , and synthesizes the overall pulse through a NAND gate. Voltage control V_{CON} over the delay variable t_P establishes PWM control over a 0.4–2.5 ns range. For PFM control and to reduce power consumption, the entire pulse generator

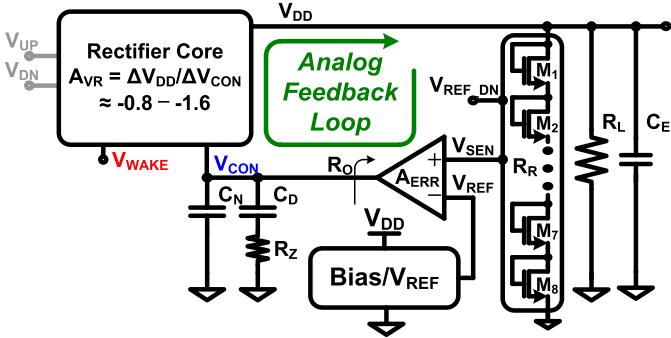


Fig. 7. PWM module for precise analog feedback.

circuit is gated by the V_{WAKE} digital signal, which powers up the comparator and delay element only when actively pulsed. The PFM power gating is especially effective at light loads to alleviate active power by lowering the operating frequency of the pulse generator and gate driver.

Low-power design of the t_{ON} comparator is critical in the overall energy efficiency of the WPT receiver, as it operates at up to 144 MHz. Prior-art high-performance comparators consume on the order of 100–800 μ W at 13.56 MHz [21]; a similar approach at 144 MHz would lead to prohibitively high comparator power in the 1–10 mW range, drastically limiting the PCE [32]

$$PCE = \frac{P_L}{P_L + P_{\text{comp}} + P_{\text{other}}} \quad (4)$$

where P_L , P_{comp} , and P_{other} are the portions of power consumed by the dc load, the comparator, and other blocks, respectively. For example, a typical dc load of $P_L = 10 \mu\text{W}$ with conventional comparator power $P_{\text{comp}} = 1 \text{ mW}$ would limit PCE below 1% even if the power consumed by all other blocks were negligible.

For a workable alternative offering fast decision at low power consumption, a bias-point-assisted dynamic comparator is proposed in Fig. 5(a). The proposed dynamic t_{ON} comparator is active only when V_{WAKE} goes high to eliminate static power consumption. Since V_{WAKE} rises all the way to V_{DD} , dynamic t_{ON} comparison is accomplished by detecting the time at which V_{UP} exceeds V_{WAKE} . As V_{UP} reaches its peak, V_{ON_PRE} also approaches its optimal bias point for fast and accurate comparison, with V_{PX} near the logic-threshold of the following inverter chain [as shown in Fig. 5(c)]. To compensate for gate driver delay (around 200 ps in simulation), the logic threshold V_{LTH} of the first inverter is adjusted for a faster decision. Further dynamic enhancement in comparator speed is accomplished with a current-reuse active g_m cell composed of M_{1N} and M_{2N} , in addition to the PMOS pair M_{1P} and M_{2P} , to dynamically increase the output current to $2i_{acN} + i_{acP}$ for fast voltage slew in V_{ON_PRE} while retaining low dc current consumption. In contrast, current state-of-the-art comparators limit the available current for voltage slew to i_{acP} . As such, the simulated average power consumption of the comparator reduces to 0.15–1.5 μW from a 0.8-V supply across all operating frequencies up to 144 MHz.

The variable delay circuit generates a pulse of width t_P as controlled by V_{CON} , when triggered by V_{ON} . Its schematic is

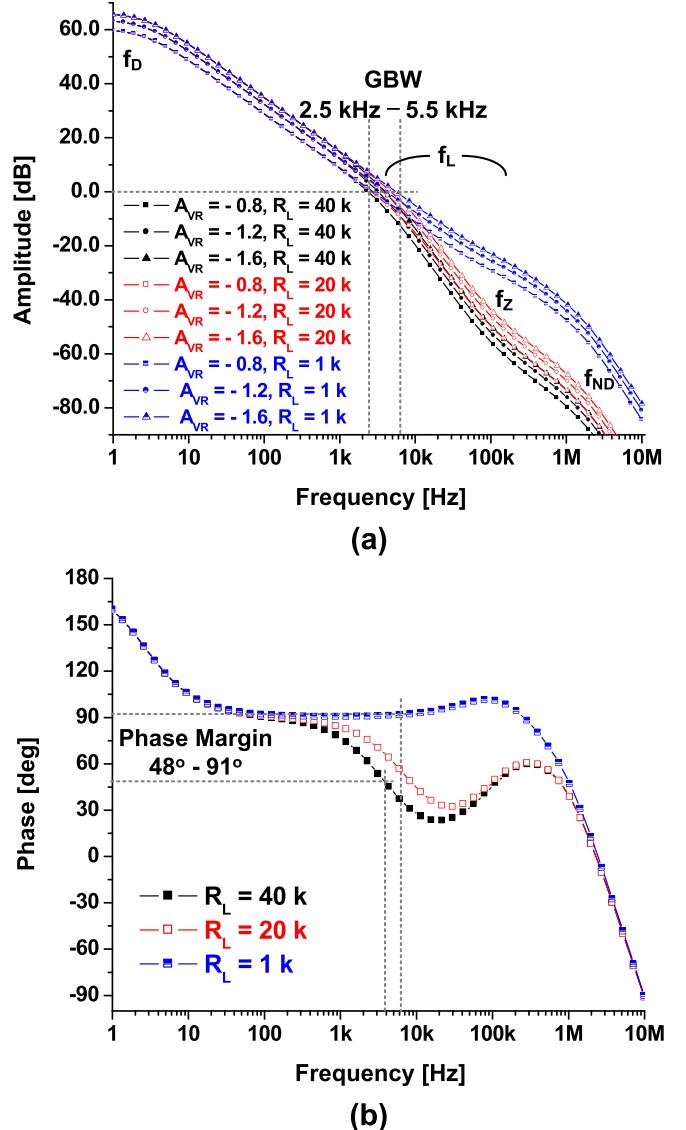


Fig. 8. Loop gain of regulator feedback with the PWM of Fig. 7. Simulated (a) amplitude and (b) phase are obtained with $A_{ERR} = G_m R_O = 68.2 \text{ dB}$, $C_D = 22 \text{ pF}$, $R_Z = 88.6 \text{ k}\Omega$, $C_N = 0.6 \text{ pF}$, $C_E = 1 \text{ nF}$, and $R_L = 1\text{--}40 \text{ k}\Omega$.

shown in Fig. 5(b). Here, V_{CON} controls the transconductance of a dynamic latch triggered by V_{ON} to provide precise short delays (0.4–2.5 ns). Simulated averaged power consumption of the delay element for 1.5 ns t_P is 0.056–1.32 μW from a 0.8-V supply, across all operating pulse-frequencies from 4.5 to 144 MHz.

B. Pulse-Frequency Modulation (PFM) Control Module

The block diagram of the PFM module is shown in Fig. 6 along with operational timing diagrams. Under light load conditions, pulse-frequency is decreased to counteract critically narrow pulse-widths that would otherwise limit the resolution in PWM mode, thereby reducing the overall switching power losses [the left side of Fig. 6(a)]. Conversely, under heavy load conditions, pulse-frequency is increased to avoid reverse currents from load to the tank at critically wide pulse-widths [the right side of Fig. 6(a)]. The PFM module considers

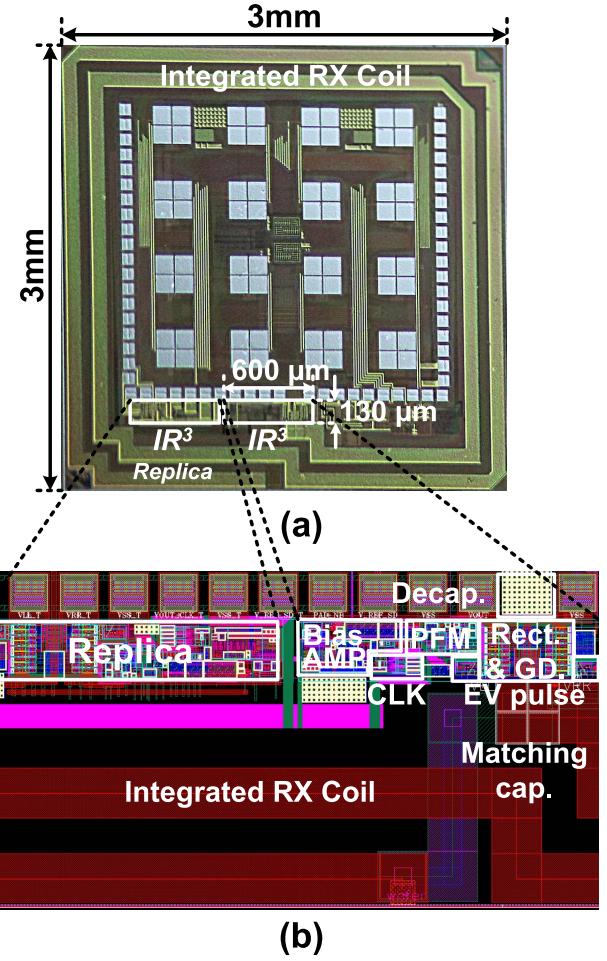
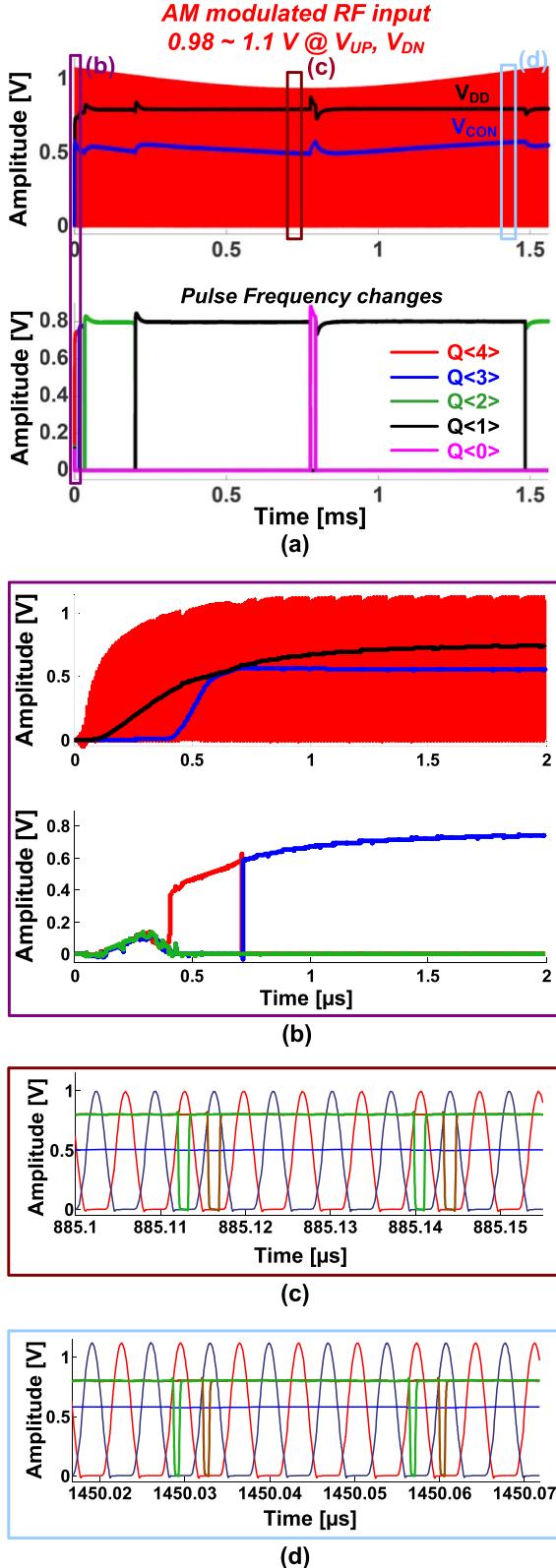


Fig. 10. (a) Microphotograph of the presented IR^3 integrated as part of an mm-sized electrocortical neural interface chip [2] with recording, stimulation, and communication circuits comprising the IR^3 load. (b) Layout detail of the IR^3 part.

Fig. 9. Integrated rectification and regulation with HPM under amplitude modulated RF input. (a) Pulse-frequency is dynamically adjusted based on the pulse-width by changing $Q_{<0:4>}$. (b) Initial power build-up waveforms (purple inset). Pulse-frequency and pulse-width waveform detail at (c) low RF input voltage (brown inset) and (d) high RF input voltage (cyan inset).

either critical action by monitoring pulse-width on a periodic 140-kHz V_{SAFE} schedule. Correspondingly, at the first rising edge of the active-low pulse V_{GU} when V_{SAFE} is active as

shown in Fig. 6(a), the latch enabler in Fig. 6(b) triggers two latched comparators to detect two types of threshold events on the pulse-width. Critically wide pulse-widths are detected by comparing V_{UP} against V_{DD} , thereby avoiding reverse current by maintaining $V_{UP} \geq V_{DD}$ throughout pulse activation. The two comparators are latched on the EN signal to reduce power and to control the updates in pulse-frequency by shifting a one-hot representation, $Q_{<0:4>}$, in a 5-bit bidirectional shift register. The pulse-frequency of V_{WAKE} in the clock generator is decided based on 5-bit outputs $Q_{<0:4>}$ of the shift register. The PFM control module shown in Fig. 6(b) in turn controls the operating frequency of the IR^3 . The simulated time domain waveforms for a critically narrow pulse-width case are shown in Fig. 6(c).

C. Pulse-Width Modulation Control Module

The PWM module shown in Fig. 7 provides a feedback signal, V_{CON} , to the rectifier core, which contains an event-driven variable pulse generator and power transistors. A voltage divider, comprising a double chain of 4 + 4 nMOS transistors, used to construct a centered sensing voltage as half of the supply voltage $V_{SEN} = V_{DD}/2$, at the expense

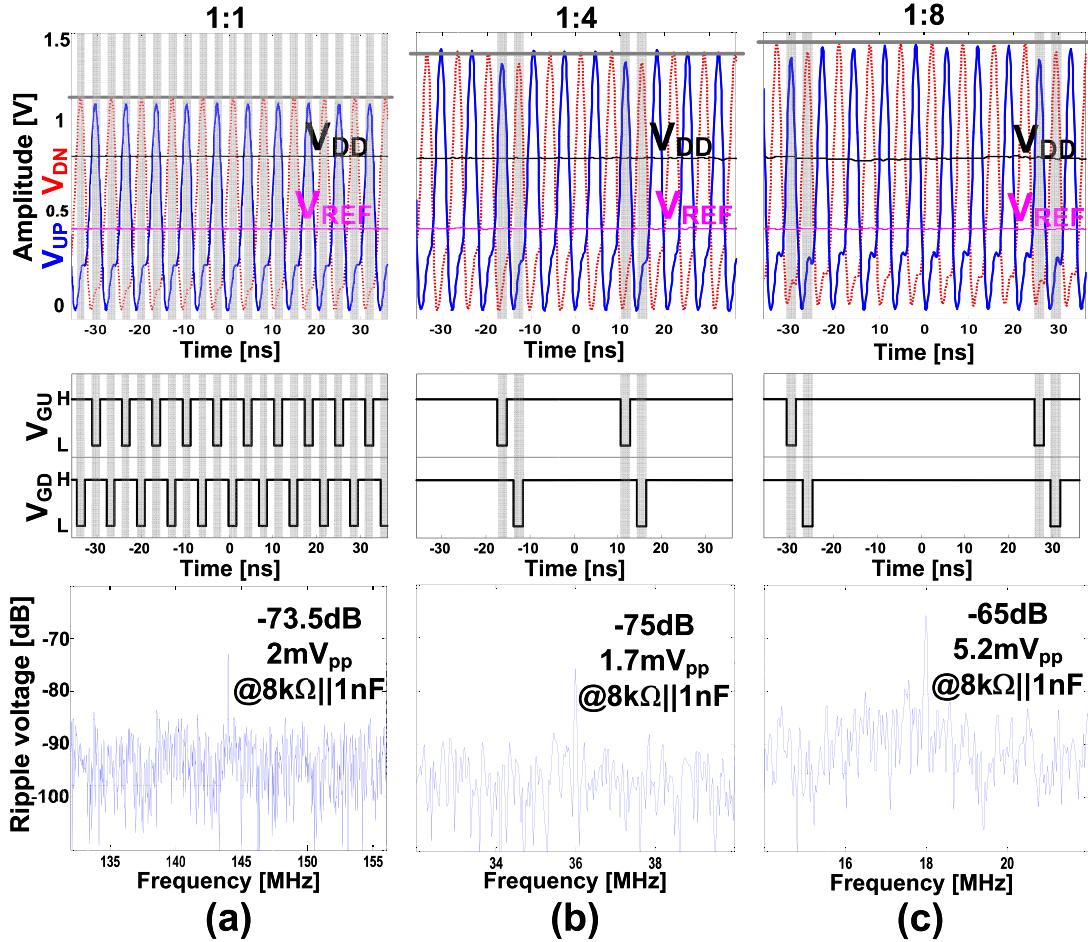


Fig. 11. Measured RF inputs, V_{UP} and V_{DN} , and dc-regulated output V_{DD} under $8\text{-k}\Omega \parallel 1\text{-nF}$ load operating in (a) $Q<0>(144\text{ MHz})$ mode, (b) $Q<1>(144\text{ MHz}/4)$ mode, and (c) $Q<2>(144\text{ MHz}/8)$ mode. Arrows indicate active cycles and show RF input loading at the regulation pulse-frequency. Spectra for voltage ripple in the regulated output V_{DD} , peaking at the pulse-frequency, are shown below for each.

of 6-dB loop gain loss. The quiescent current of the divider is around 40 nA, resulting in $R_R \approx 20\text{M}\Omega$ at $V_{DD} = 0.8\text{ V}$. Negative feedback around the error amplifier, A_{ERR} , comparing V_{SEN} with a locally generated reference, V_{REF} , regulates the rectified supply V_{DD} near $2V_{REF}$. The current consumption of the reference generator block for V_{REF} is 600 nA when V_{DD} is 0.8 V.

Large loop gain plays a significant role in reducing the regulation error. As such, a two-stacked folded-cascode amplifier offering 68-dB open-loop gain at dc consuming 240 nA at V_{DD} of 0.8 V is chosen for the error amplifier. Stability of the analog feedback in supply regulation requires both dominant-pole and zero compensation in the loop. The dominant pole is set by an inserted capacitance, C_D , loading the error amplifier along with its output impedance, R_O . Asserting the dominant pole independent of load conditions requires that $R_0 C_D \gg R_{L,\text{MAX}} C_E$, where $R_{L,\text{MAX}}$ is the minimum load from the supply and C_E is the supply decoupling capacitance. For sufficient phase margin, a zero is inserted at $f_Z = 1/2\pi R_Z C_D$ by adding a resistor R_Z in series with C_D . To mitigate the resulting increase in high-frequency noise, an additional small capacitor, C_N , is inserted in parallel with C_D and R_Z , contributing a nondominant pole at $f_N = 1/2\pi R_Z C_N$.

The small-signal voltage gain of the rectifier core, A_{VR} , ranges between -0.8 and -1.6 depending on input and load conditions through PFM in the V_{WAKE} waveform. The first-order analysis gives the loop gain of

$$A_L = \frac{1/2 \cdot A_{ERR} \cdot A_{VR} \cdot (1 + SR_Z C_D)}{(1 + SR_O C_D)(1 + SR_Z C_N)(1 + SR_L C_E)}. \quad (5)$$

Accommodating a broad range of load resistances, R_L , the load pole $f_L = 1/2\pi R_L C_E$ varies from 4 to 160 kHz as shown in Fig. 8. Owing to the dominant pole and zero compensation, the phase margin is guaranteed greater than 48° for loads heavier than $40\text{ k}\Omega$, ensuring the stability of the analog feedback over the operating range.

V. HYBRID PULSE MODULATION UNDER RF INPUT VARIATION

To prove the efficacy of the proposed HPM, the IR³ is simulated with a time-varying RF input voltage as shown in Fig. 9. Here, a 144-MHz RF input is AM with a 0.1 AM modulation index at 0.4 kHz, resulting in an amplitude variation from 0.98 to 1.1 V at the half-waved rectified voltage, V_{UP} and V_{DN} . After V_{DD} initially develops owing to a passive

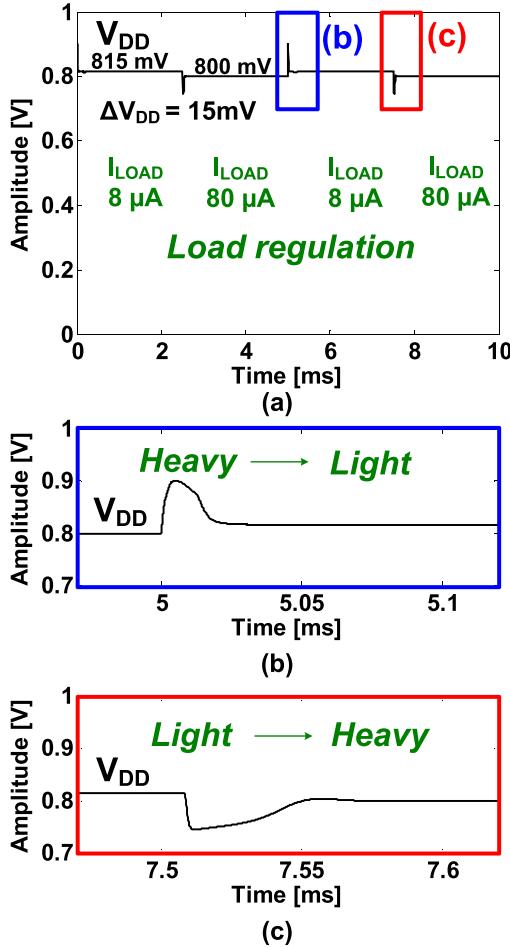


Fig. 12. (a) Measured dynamic load regulation of V_{DD} with I_{LOAD} alternating between 8 and 80 μA with a 1-nF decoupling capacitor at V_{DD} node. PFM improves the regulation speed by changing the pulse-frequency at (b) heavy-to-light load transition and (c) light-to-heavy load transition.

diode-connected rectification mode, the HPM starts rectification and regulation simultaneously on V_{DD} by changing, first, V_{CON} for the pulse-width and, later, $Q < 1:4 >$ for the pulse-frequency as shown in Fig. 9(a). This can be more clearly seen in Fig. 9(b) and (c). At decreasing RF input voltages, the PWM control circuit accordingly widens the pulse-width via analog feedback at the fixed $Q < 1 >$ mode. At its maximum pulse-width shown in Fig. 9(b), the PFM increases the pulse-frequency to the $Q < 0 >$ mode. After reaching its minimum, the RF input voltage begins to increase again. As such, the pulse-width is getting narrowed and the pulse-frequency is back to $Q < 1 >$ mode for regulation under increasing RF input. When critically narrowed pulse-width is detected by the PFM module, the pulse-frequency is increased to the $Q < 2 >$ mode to avoid degradation in PCE and failure of regulation.

VI. MEASUREMENT RESULTS

A microphotograph of an electrocortical neural interface chip [2] internally powered by the presented IR^3 is shown in Fig. 10(a). The active area of the IR^3 part of the chip, presented here, is 0.078 mm^2 in 180-nm 1P4M SOI. An on-chip RX coil is implemented at the chip edge so as to maximize its

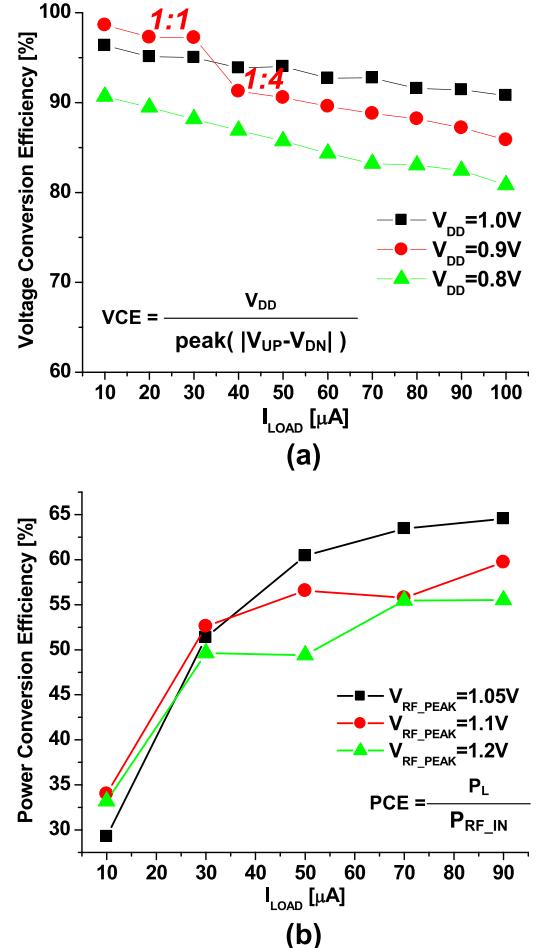


Fig. 13. (a) Measured voltage conversion efficiency and (b) simulated PCE of the IR^3 under varying external load current, target regulation voltage, and RF input conditions.

area with two turns of top metal for 23.7 nH of inductance. The top metal width of the coil is 100 μm to ensure a small series resistance, R_S . As such, HFSS electromagnetic simulation shows that Q_{coil} of the RX coil is 12 at 144 MHz. As shown in Fig. 10(b), the rectifier core in the IR^3 is placed physically adjacent to a matching resonant capacitor to reduce parasitics. To mitigate high-frequency switching noise, sensitive analog blocks in the PWM module are placed far from the rectifier core.

For the isolated characterization of RF input regulation, load regulation, and conversion efficiencies of the IR^3 circuit independent of the integrated RX coil, a printed circuit board (PCB) RF transformer (TC1-1G2+, Mini-Circuits) is initially used to bypass the on-chip LC tank and directly supply V_{UP} and V_{DN} as differential RF sinusoidal signals from a vector signal generator (Keysight N5181A).

Fig. 11 shows the measurements of the IR^3 regulating V_{DD} at 0.8 V within 5.2-mV_{pp} ripple at various RF input levels representative of typical link distance variations, with correspondingly varying frequency modulations. As expected, the rate of rectification (i.e., PFM frequency) is maximum (i.e., 144 MHz) at the lowest RF input voltage amplitude, as the rectifier goes active every RF cycle (maximum PFM) to

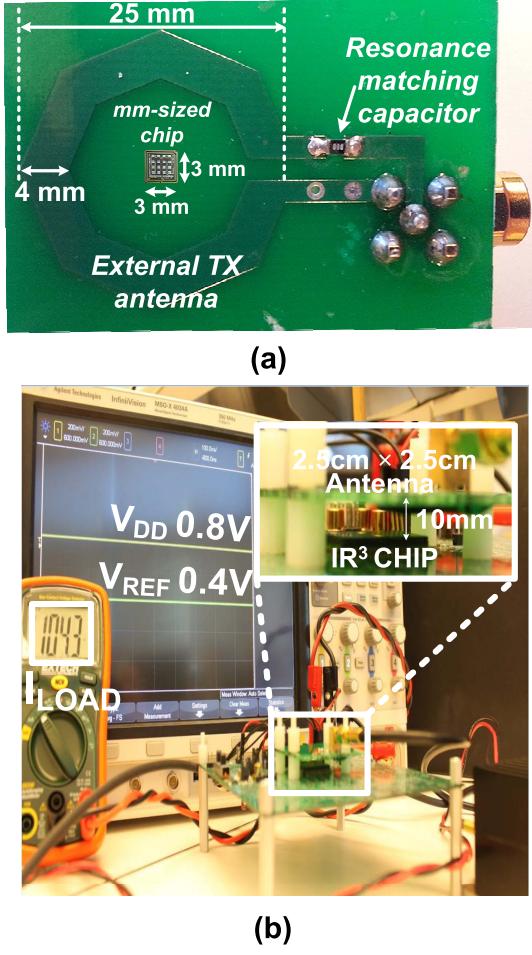


Fig. 14. Test setup for WSE system validation. (a) External $2.5\text{ cm} \times 2.5\text{ cm}$ TX coil with matching network. The mm-sized implant chip with the presented IR^3 shown in Fig. 10(a) is superimposed in the center for size comparison. (b) WPT at 1-cm distance between TX and on-chip RX coils.

extract as much power from the input as possible [Fig. 11(a)]. Conversely, the rectifier skips several cycles (lower PFM) at high RF input levels [Fig. 11(b) and (c)], as a sufficient amount of energy can be extracted from the input over fewer RF cycles. To characterize ripple, FFT spectra of the regulated voltage V_{DD} , shown at the bottom of Fig. 11(a)–(c), reveal a peaking tone at the pulse-frequency. Note that 144-MHz RF energy coupling through parasitics on the PCB also partially couples to V_{DD} such that Fig. 11(a) shows slightly higher ripple voltage than Fig. 11(b) despite higher pulse-frequency. Altogether, the measurements demonstrate the effectiveness of the proposed HPM technique under various RF input voltages.

The presented IR^3 powers a neural interface system having very different static power-consuming levels according to two main operational modes, stimulation versus recording [2]. To evaluate the capability of the IR^3 accommodating a large dynamic range in static power levels, V_{DD} is measured while changing I_{LOAD} from 8 to 80 μA . Owing to the proposed HPM in the IR^3 regulation functionality, a tenfold change in I_{LOAD} incurs less than 15-mV static variation in V_{DD} as shown in Fig. 12(a). This static variation could be further improved by increasing loop gain with a higher gain error amplifier.

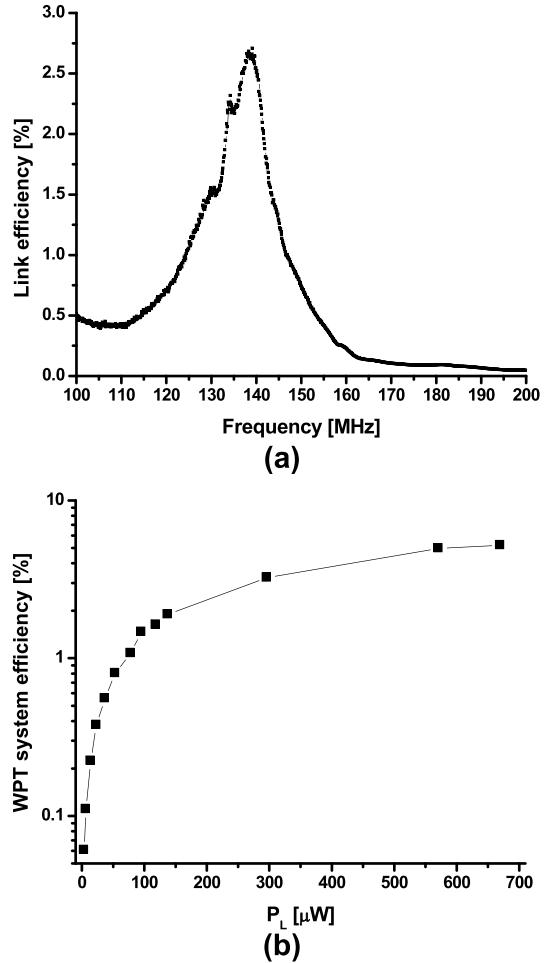


Fig. 15. Measured WPT power efficiencies with an external $2.5\text{ cm} \times 2.5\text{ cm}$ TX coil. (a) Link efficiency between the external TX coil and the RX two-turn on-chip coil with ac resistance $R_{ac} = 4.3\text{ k}\Omega$. (b) WSE = P_L/P_{TX} at 1-cm distance between TX and on-chip RX coils. The IR^3 maintains a constant 800-mV V_{DD} for loads up to 700 μW .

PFM effectiveness in transient regulation response under rapid load transitions is shown in Fig. 12(b) and (c).

Since the IR^3 performs rectification and regulation simultaneously, voltage conversion efficiency and PCE from both rectification and regulation are reported as shown in Fig. 13(a) and (b). Compared with advanced active rectifier designs [32], [33] achieving around 80% of VCE from only rectification, greater than 80% of VCE is observed across the range of load conditions at various target supply voltage V_{DD} levels, controlled by an externally supplied, bypassed reference V_{REF} . At $V_{DD} = 1\text{ V}$, the lowest measured VCE is 92%. As shown in Fig. 13(b), PCE is higher than 30% even under 8- μW load. As such, the total power consumption of the IR^3 , including power losses from the power transistors, is less than 20 μW at 144 MHz. The low power consumption is achieved mainly because of the proposed bias point-assisted dynamic t_{ON} comparator. PCE improves at increasing load currents, since the portion of the power consumed by control blocks of the IR^3 is independent of load changes. At maximum load, the integral PCE of the IR^3 , combining rectification and regulation, reaches 60%. In contrast, power converters in the state-of-the-art mm-sized implants [7], [8] achieve around 60%

TABLE I
PERFORMANCE COMPARISON

	[1] Muller	[7] O'Driscoll	[8, 9] Mark	[12, 22] Zargham	This Work
RX Coil	Off-chip/ 32 nH	Off-chip/ N/R	Off-chip/ 5.73 nH	On-chip/ 130 nH	On-chip/ 23.7 nH
Area of RX coil [mm²]	42.25	4	1	4.36	8.64
Res. Freq. [MHz]	300	915	535	160	144
Regulator	Separated LDO	Separated LDO	Separated LDO	Separated LDO	Regulating rectifier
Regulation* [%]	N/R	N/R	N/R	N/R	1.87
Decoupling Cap. [nF]	4	N/R	1.39	0.02	1
Process	65 nm 1P7M CMOS	0.13 μm CMOS	65 nm CMOS	0.13 μm 1P8M CMOS	0.18 μm 1P4M CMOS SOI
Overall WSE (TX to V_{DD}) [%]	1.19^a	0.048 (-33.2 dB)	0.02 (-37 dB)	0.62^b	2.04^c
Distance [mm]	12.5	15	13	10	10
WSE FOM**	8.46	20.25	43.94	68.1	80.3

^aestimated from provided data

transmit PW: 13mW, received PW: 0.225mW (simulated link gain, -16.5 dB)
and P_L: 0.160mW

^bestimated from provided data

provided efficiency from TX to the output of rectifier: 0.9 %, calculated
efficiency of LDO: 68 % (V_{DD}: 3.1 V, V_{REC2}: 4.5 V)

^cmeasured TX power: 7.87mW and P_L: 0.160mW

*defined by [25], Regulation = Static ΔV_{DD} / nominal V_{DD}

**modified from [12], WSE FOM = $\frac{\text{Overall WSE} \times \text{Distance}^3}{\text{Area of RX coil}^{1.5}}$

of PCE for rectification, in cascade with 50%–80% of PCE for regulation, for a net 30%–50% combined PCE.

The wireless inductive link efficiency and overall WSE with the RX integrated on-chip coil connected to the IR³ are characterized using a 2.5 cm × 2.5 cm, single-turn TX coil integrated with a passive matching network on a PCB as shown in Fig. 14(a). Quality factor of the TX coil is greater than 70 at the resonance frequency. The TX coil inductively couples to the on-chip two-turn (2.4 mm × 2.4 mm inner loop and 2.9 mm × 2.9 mm outer loop) RX coil over 1-cm distance as shown in Fig. 14(b). In this setup, S-parameters between the TX coil and the RX integrated on-chip coil are measured with a network analyzer (Keysight, E5080A), and converted to Z-parameters. Parasitics from the matching network, PCB traces, Subminiature version A connectors, and cables are measured and de-embedded [6], [34] to obtain the accurate link efficiency showing the net power gain from the transmitted power at the TX coil (P_{TX}) to the received power at a 4.3-kΩ ac load R_{ac} to the RX

coil. According to (2), 4.3-kΩ of ac load R_{ac} is equivalent to 8.9 kΩ of R_L with 0.82 of VCE and 0.65 of PCE (Fig. 13), rendering a 90-μW load to V_{DD}. With this load, the peak link efficiency across various RF frequencies is 2.7% at the RX coil resonance frequency as shown in Fig. 15(a). Measured overall WSE (P_L/P_{TX}) under various load conditions is shown in Fig. 15(b). The IR³ maintains a constant 800-mV V_{DD} for loads up to 700 μW. Greater than 2%, overall WSE from TX coil to the regulated dc is demonstrated with a 160-μW load over air while, at the same input power to the TX coil, 8-dB additional power loss is measured in a more realistic biomedical setting implemented by inserting 1 cm of porcine fatty abdominal tissue.

Table I summarizes key performance measures of the IR³ in comparison with the state-of-the-art designs for mm-sized implants. Among these, only IR³ utilizes a regulating rectifier to improve PCE and, thus, WSE. The tabulated figure-of-merit (FoM) is based on the one proposed by Zargham and Gulak [12], considering that for mm-sized RX

coils (in the mid-field regime), the TX–RX link efficiency is inversely proportional to the cube of the inter-coil distance [13] and the cube of the square root of RX coil area [12]. In the comparison of Table I, we extend this FoM from TX–RX link efficiency to overall WSE also accounting for the implant PCE, of the form

$$\text{WSE FoM} = \frac{\text{WSE} \times D^3}{A^{1.5}} \quad (6)$$

where D is the distance between TX and RX coils, and A is the outer-loop area of the RX coil.

VII. CONCLUSION

This paper has shown the first fully integrated mm-sized WPT receiver for micropower mm-sized biomedical implants operating without off-chip components. Higher resonant frequencies, such as 144 MHz demonstrated here, support full integration of the RX coil with reduced size matching capacitor, and offer higher link efficiency. Crucially, the integration of rectification and regulation yields substantially higher PCE and VCE along with savings in silicon area by avoiding the need for decoupling capacitors in mm-sized implants. The unique combination of RF inductive resonant power transfer, rectification, and hybrid PWM-PFM regulation of the IR³ offers superior voltage conversion efficiency and PCE alleviating severe powering conditions of deep mm-size biomedical implants. As suggested in Fig. 1, we envision tiled arrays of mm-sized implants distributed across the surface of cortex with fully integrated IR³s for power reception and with data transceivers for data communication, performing simultaneous parallel power delivery and data telemetry using a single external loop antenna driven by a beamforming transceiver IC [35], [36].

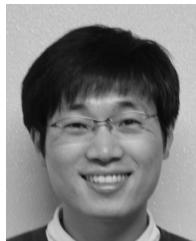
ACKNOWLEDGMENT

The authors would like to thank S. Dayeh, V. Gilja, E. Halgren, B. McNaughton, and other researchers on the ENIAC Memory Prostheses Team for valuable interactions and collaborations.

REFERENCES

- [1] R. Muller *et al.*, “A Minimally Invasive 64-Channel Wireless μECOG Implant,” *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 344–359, Jan. 2015.
- [2] S. Ha *et al.*, “Silicon-Integrated High-Density Electrocortical Interfaces,” *Proc. IEEE*, vol. 105, no. 1, pp. 11–33, Jan. 2017.
- [3] H. Lee, R. V. Bellamkonda, W. Sun, and M. E. Levenston, “Biomechanical Analysis of Silicon Microelectrode-Induced Strain in the Brain,” *J. Neural Eng.*, vol. 2, no. 4, pp. 81–89, 2005.
- [4] G. C. McConnell, H. D. Rees, A. I. Levey, C.-A. Gutekunst, R. E. Gross, and R. V. Bellamkonda, “Implanted Neural Electrodes Cause Chronic, Local Inflammation That Is Correlated With Local Neurodegeneration,” *J. Neural Eng.*, vol. 6, no. 5, p. 056003, Aug. 2009.
- [5] L. Karumbaiah *et al.*, “Relationship Between Intracortical Electrode Design and Chronic Recording Function,” *Biomaterials*, vol. 34, no. 33, pp. 8061–8074, Nov. 2013.
- [6] D. Ahn and M. Ghovanloo, “Optimal Design of Wireless Power Transmission Links for Millimeter-Sized Biomedical Implants,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 1, pp. 125–137, Feb. 2016.
- [7] S. O’Driscoll, A. S. Y. Poon, and T. H. Meng, “A mm-Sized Implantable Power Receiver With Adaptive Link Compensation,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2009, pp. 294–295.
- [8] M. Mark, “Powering mm-Size Wireless Implants for Brain-Machine Interfaces,” Ph.D. dissertation, Dept. Elect. Eng. Comput. Sci., Univ. California Berkeley, Berkeley, CA, USA, Dec. 2011.
- [9] M. Mark *et al.*, “A 1mm³ 2 Mbps 330fJ/b Transponder for Implanted Neural Sensors,” in *Proc. Symp. VLSI Circuits (VLSI Circuits)*, Jun. 2011, pp. 168–169.
- [10] X. Li, C.-Y. Tsui, and W.-H. Ki, “Wireless Power Transfer System Using Primary Equalizer for Coupling- and Load-Range Extension in Bio-Implant Applications,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 228–229.
- [11] X. Li, X. Meng, C. Y. Tsui, and W. H. Ki, “Reconfigurable Resonant Regulating Rectifier With Primary Equalization for Extended Coupling- and Loading-Range in Bio-Implant Wireless Power Transfer,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 9, no. 6, pp. 875–884, Dec. 2015.
- [12] M. Zargham and P. Gulak, “Fully Integrated on-Chip Coil in 0.13 μm CMOS for Wireless Power Transfer Through Biological Media,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 9, no. 2, pp. 259–271, Apr. 2015.
- [13] A. S. Y. Poon, S. O’Driscoll, and T. H. Meng, “Optimal Frequency for Wireless Power Transmission Into Dispersive Tissue,” *IEEE Trans. Antennas Propag.*, vol. 58, no. 5, pp. 1739–1750, May 2010.
- [14] M. Zargham and P. G. Gulak, “Maximum Achievable Efficiency in Near-Field Coupled Power-Transfer Systems,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 3, pp. 228–245, Jun. 2012.
- [15] J. M. Rabaey *et al.*, “Powering and Communicating With mm-Size Implants,” in *Proc. Design, Autom. Test Eur.*, Mar. 2011, pp. 1–6.
- [16] C. Kim, S. Ha, J. Park, A. Akinin, P. Mercier, and G. Cauwenberghs, “A 144 MHz Integrated Resonant Regulating Rectifier With Hybrid Pulse Modulation,” in *Proc. Symp. VLSI Circuits (VLSI Circuits)*, Jun. 2015, pp. 284–285.
- [17] P. P. Mercier and A. P. Chandrakasan, “Rapid Wireless Capacitor Charging Using a Multi-Tapped Inductively-Coupled Secondary Coil,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 9, pp. 2263–2272, Sep. 2013.
- [18] R. Sarpeshkar, *Ultra Low Power Bioelectronics*. Cambridge, U.K.: University Press, 2010.
- [19] P. P. Mercier and A. P. Chandrakasan, *Ultra-Low-Power Short-Range Radios*. Cham, Switzerland: Springer, 2015.
- [20] B. Lee, P. Yeon, and M. Ghovanloo, “A Multicycle Q-Modulation for Dynamic Optimization of Inductive Links,” *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 5091–5100, Aug. 2016.
- [21] H. M. Lee and M. Ghovanloo, “A High Frequency Active Voltage Doubler in Standard CMOS Using Offset-Controlled Comparators for Inductive Power Transmission,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 3, pp. 213–224, Jun. 2013.
- [22] M. Zargham and P. G. Gulak, “A 0.13 μm CMOS Integrated Wireless Power Receiver for Biomedical Applications,” in *Proc. ESSCIRC(ESSCIRC)*, Sep. 2013, pp. 137–140.
- [23] W.-C. Chen, S.-Y. Ping, T.-C. Huang, Y.-H. Lee, K.-H. Chen, and C.-L. Wey, “A Switchable Digital-Analog Low-Dropout Regulator for Analog Dynamic Voltage Scaling Technique,” *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 740–750, Mar. 2014.
- [24] J. Charthad, M. J. Weber, T. C. Chang, and A. Arbabian, “A mm-Sized Implantable Medical Device (IMD) With Ultrasonic Power Transfer and a Hybrid Bi-Directional Data Link,” *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 1741–1753, Aug. 2015.
- [25] J.-H. Choi, S.-K. Yeo, S. Park, J.-S. Lee, and G.-H. Cho, “Resonant Regulating Rectifiers (3R) Operating for 6.78 MHz Resonant Wireless Power Transfer (RWPT),” *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 2989–3001, Dec. 2013.
- [26] X. Li, C.-Y. Tsui, and W.-H. Ki, “A 13.56 MHz Wireless Power Transfer System With Reconfigurable Resonant Regulating Rectifier and Wireless Power Control for Implantable Medical Devices,” *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 978–989, Apr. 2015.
- [27] L. Cheng, W. H. Ki, T. T. Wong, T. S. Yim, and C. Y. Tsui, “A 6.78MHz 6W Wireless Power Receiver With a 3-Level 1 × 1/2 × 1/0 × Reconfigurable Resonant Regulating Rectifier,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan. 2016, pp. 376–377.
- [28] H. M. Lee, C. S. Juvekar, J. Kwong, and A. P. Chandrakasan, “A Nonvolatile Flip-Flop-Enabled Cryptographic Wireless Authentication Tag With Per-Query Key Update and Power-Glitch Attack Countermeasures,” *IEEE J. Solid-State Circuits*, vol. 52, no. 1, pp. 272–283, Jan. 2017.
- [29] H. M. Lee, H. Park, and M. Ghovanloo, “A Power-Efficient Wireless System With Adaptive Supply Control for Deep Brain Stimulation,” *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2203–2216, Sep. 2013.
- [30] B. Sahu and G. A. Rincon-Mora, “An Accurate, Low-Voltage, CMOS Switching Power Supply With Adaptive on-Time Pulse-Frequency Modulation (PFM) Control,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 2, pp. 312–321, Feb. 2007.

- [31] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. New York, NY, USA: Springer, 2001.
- [32] H.-M. Lee and M. Ghovanloo, "An Integrated Power-Efficient Active Rectifier With Offset-Controlled High Speed Comparators for Inductively Powered Applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 8, pp. 1749–1760, Aug. 2011.
- [33] G. Bawa and M. Ghovanloo, "Active High Power Conversion Efficiency Rectifier With Built-in Dual-Mode Back Telemetry in Standard CMOS Technology," *IEEE Trans. Biomed. Circuits Syst.*, vol. 2, no. 3, pp. 184–192, Sep. 2008.
- [34] A. Ibrahim and M. Kiani, "A Figure-of-Merit for Design and Optimization of Inductive Power Transmission Links for Millimeter-Sized Biomedical Implants," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 6, pp. 1100–1111, Dec. 2016.
- [35] C. Kim, S. Joshi, C. M. Thomas, S. Ha, L. E. Larson, and G. Cauwenberghs, "A 1.3 mW 48 MHz 4-Channel MIMO Baseband Receiver With 65 dB Harmonic Rejection and 48.5 dB Spatial Signal Separation," *IEEE J. Solid State Circuits*, vol. 51, no. 4, pp. 832–844, Apr. 2016.
- [36] D. Seo *et al.*, "Ultrasonic Beamforming System for Interrogating Multiple Implantable Sensors," in *Proc. 37th Annu. Int. Conf. IEEE Eng. Med. Biol. Soc. (EMBC)*, Aug. 2015, pp. 2673–2676.



Chul Kim (S'12) received the B.S. degree in electrical engineering from Kyungpook National University, Daegu, South Korea in 2007 and the M.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2009. He is currently pursuing the Ph.D. degree with the Bioengineering Department, University of California at San Diego, La Jolla, CA, USA.

During 2009–2012, he was with SK HYNIX, Icheon, South Korea, where he designed power management circuitry for dynamic random-access memory. His current research interests include designing micropower integrated circuits for biomedical applications and brain-machine interfaces.

Mr. Kim was a recipient of Gold Prizes in the 16th Human-Tech Thesis Prize Contest from Samsung Electronics, Suwon, South Korea, in 2010.



Sohmyung Ha (S'05–M'16) received the B.S. (*summa cum laude*) and M.S. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2004 and 2006, respectively, and the M.S. and Ph.D. degrees in biomedical engineering from the Department of Bioengineering, University of California at San Diego, La Jolla, CA, USA, in 2015 and 2016, respectively.

From 2006 to 2010, he was an Analog and Mixed-Signal Circuit Designer with Samsung Electronics, Yongin, South Korea, where he was a part of the engineering team responsible for several of the world best-selling multimedia devices, smartphones, and TVs. After an extended career in industry, he returned to Academia as a Fulbright Scholar. Since 2016, he has been with New York University Abu Dhabi, Abu Dhabi, United Arab Emirates, where he is currently an Assistant Professor of electrical and computer engineering.

Dr. Ha received the Best Ph.D. Thesis Award for biomedical engineering from the Department of Bioengineering, University of California at San Diego.



Jiwong Park (S'15) received the B.Sc. degree in electronic and computer engineering from Hanyang University, Seoul, South Korea, in 2012, and the M.S. degree in electrical and computer engineering from the University of California at San Diego, La Jolla, CA, USA, in 2014, where he is currently pursuing the Ph.D. degree.

His current research interests include the design of ultralow-power body area network systems and the design of miniaturized wireless power transfer systems for biomedical implants.



Abraham Akinin (S'13) was born in Caracas, Venezuela. He received the B.S. degree in biomedical engineering and physics from the University of Miami, Coral Gables, FL, USA, in 2010. He is currently pursuing the Ph.D. degree with the Bioengineering Department, Institute for Neural Computation, University of California at San Diego, La Jolla, CA, USA.

His current research interests include the design of implantable closed-loop neuroprosthetics and biomedical instrumentation to restore sensory and cognitive function.



Patrick P. Mercier (S'04–M'12) received the B.Sc. degree in electrical and computer engineering from the University of Alberta, Edmonton, AB, Canada, in 2006, and the M.S. degree in electrical engineering and the Ph.D. degree in computer science from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2008 and 2012, respectively.

He is currently an Assistant Professor in electrical and computer engineering with the University of California at San Diego (UCSD), where he is also

the Co-Director of the Center for Wearable Sensors. He has co-edited the books *Ultra-Low-Power Short Range Radios* (Springer, 2015) and *Power Management Integrated Circuits* (CRC Press, 2016). His current research interests include the design of energy-efficient microsystems, focusing on the design of RF circuits, power converters, and sensor interfaces for miniaturized systems and biomedical applications.

Dr. Mercier received a Natural Sciences and Engineering Council of Canada (NSERC) Julie Payette Fellowship in 2006, the NSERC Postgraduate Scholarships in 2007 and 2009, an Intel Ph.D. Fellowship in 2009, the 2009 IEEE International Solid-State Circuits Conference (ISSCC) Jack Kilby Award for Outstanding Student Paper at ISSCC 2010, a Graduate Teaching Award in Electrical and Computer Engineering at UCSD in 2013, the Hellman Fellowship Award in 2014, the Beckman Young Investigator Award in 2015, the DARPA Young Faculty Award in 2015, and the UCSD Academic Senate Distinguished Teaching Award in 2016. He has served as an Associate Editor of the *IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION* from 2015 to 2017. He currently serves as a member of the ISSCC technical program committee (Technology Directions sub-committee) and as an Associate Editor of the *IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS* (2013–present).



Gert Cauwenberghs (S'89–M'94–SM'04–F'11) received the Ph.D. degree in electrical engineering from the California Institute of Technology, Pasadena, CA, USA, in 1994.

He was a Professor of electrical and computer engineering with Johns Hopkins University, Baltimore, MD, USA, and a Visiting Professor of brain and cognitive science with the Massachusetts Institute of Technology, Cambridge, MA, USA. He co-founded Cognionics Inc., San Diego, CA, USA, and chairs its Scientific Advisory Board. He

is currently a Professor of bioengineering and a Co-Director of the Institute for Neural Computation, University of California at San Diego, La Jolla, CA, USA. His current research interests include micropower biomedical instrumentation, neuron-silicon and brain-machine interfaces, neuromorphic engineering, and adaptive intelligent systems.

Dr. Cauwenberghs was a Francqui Fellow of the Belgian American Educational Foundation, and is a fellow of the American Institute for Medical and Biological Engineering. He received the NSF Career Award in 1997, the ONR Young Investigator Award in 1999, and the Presidential Early Career Award for Scientists and Engineers in 2000. He served the IEEE in a variety of roles, including as a Distinguished Lecturer of the IEEE Circuits and Systems Society, as the General Chair of the 2011 IEEE Biomedical Circuits and Systems Conference, San Diego, as the Program Chair of the 2012 IEEE Engineering in Medicine and Biology Conference, San Diego, and as the Editor-in-Chief of the *IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS*.