

Multiple-Loop Design Technique for High-Performance Low-Dropout Regulator

Quoc-Hoang Duong, Huy-Hieu Nguyen, Jeong-Woon Kong, Hyun-Seok Shin, Yu-Seok Ko, Hwa-Yeol Yu, Yong-Hee Lee, Chun-Hyeon Bea, and Ho-Jin Park

Abstract—A new multiple-loop design technique for high-performance low-dropout (LDO) regulator designs has been proposed and successfully implemented in many commercial products for portable smart phone and tablet PC applications. The proposed LDO is composed of five loops that allows designers to obtain a good tradeoff between quiescent current and other performances, such as undershoot, overshoot, and so on. A total of one bandgap reference and 38 LDOs (including n-type and p-type LDOs, which will be named NLDO and PLDO, respectively) were integrated in one power-management IC chip for powering an application processor inside mobile devices. The proposed LDO has been fabricated based on 0.13- μm CMOS process and supplies various current capacities from 50 to 600 mA; 38 LDOs have been designed and supply different output voltage levels from 0.7 to 3.0 V. One of the proposed NLDOs consumes 14 μA of the quiescent current and features under 56/24 mV of undershoot/overshoot at $\text{VOUT} = 1\text{V}$ as the load current steps up from 0 to 300 mA with 300 mA/1 μs on a 1- μF output capacitor. The measured output load and line regulations are 1.8 and 0.4 mV, respectively. The measured integrated output noise from 10 Hz to 100 kHz at $\text{ILOAD} = 10\%$ of maximum current shows 80 μVrms . The package chip size is 6.25 \times 6.25 mm² with 169 balls.

Index Terms—Dynamic biasing, fast transient response, LDO regulator, low dropout (LDO), low quiescent current, power management IC (PMIC).

I. INTRODUCTION

IN PORTABLE mobile devices, the power management IC (PMIC) unit requires many low-dropout (LDO) regulators with different output voltages and load current capacities to support many applications, such as application processor (AP), camera, memory, radio-frequency integrated circuit (RFIC) transceivers, universal serial bus (USB), and so on, as shown in Fig. 1(A) [1]–[6]. Since there is only one battery with a fixed voltage range for supplying all these applications as shown in Fig. 1(B) and (C), a large numbers of switching dc–dc converters (buck, boost, or buck–boost) are used to convert battery voltage to different output levels. These converters usually provide significant voltage ripple at the output, which degrades the performance of precision analog and radio-frequency circuits [1]–[8]. Consequently, many LDOs

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The authors are with the Device Solution Division, Power Device Development Team, Samsung Electronics, Hwaseong 18448, South Korea (e-mail: hoangdq@yahoo.com).

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are cascaded at the output of switching dc–dc converters as shown in Fig. 1(C). As the final blocks in power supplier, excellent-performance LDOs are required, especially undershoot/overshoot, quiescent current, and so on.

In Fig. 1(A), the AP PMIC usually requires more than 30 LDOs, camera PMIC may require 18 LDOs, communication processor PMIC is integrated with up to 14 LDOs, organic light-emitting diode and multimedia card PMICs may need up to six LDOs, and so on. Consequently, the total number of LDOs for mobile applications can be up to 80, which requires a huge quiescent current that critically degrade battery life time. Fig. 1(B) shows a floor plan of the AP PMIC, which includes 38 LDOs, one bandgap reference (BGR), 11 bucks, one backup charger, and others. In Fig. 1(B), Buck1 and Buck2 generate 1.5-A output load for memory interface card (MIF) application, while Buck5 outputs 1.5 A of load current for display and camera applications, and so on. The connection of BGR, LDOs, and buck converters in the system is shown in Fig. 1(C), where the BGR generates a reference voltage for all internal LDOs. In Fig. 1(C), each buck converter will supply power to many LDOs with different load current capacities. For example, the buck outputs 1.2 V so that LDO can be usually designed with a maximum voltage output of around 1–1.1 V; however, load currents from 50 to 600 mA are designed.

As discussed previously, portable smart phone applications require a huge number of LDO blocks such that the required quiescent current becomes very big that may degrade battery life time. There is a critical tradeoff between quiescent current and other LDO's characteristics, especially, undershoot, overshoot, and so on. This paper proposed a new multiple-loop design technique for LDO that offers a low bias current with excellent performance improvement compared with prior reported works in terms of undershoot, overshoot, noise, and so on. This paper is organized as follows. Section II describes conventional LDO design limitations and state-of-the-art low-bias fast-transient LDO designs, Section III presents our new design technique, Section IV provides the detailed circuit implementations and stability analysis, Section V discusses measurement results, and Section VI concludes this paper.

II. STATE-OF-THE-ART LDO DESIGNS

A. Conventional LDO Designs

Fig. 2(A.1) and (A.2) shows a block diagram of a conventional LDO and its transient response to a step output load current, respectively. As shown in Fig. 2(A.1), there is a big parasitic capacitance introduced at the gate of the

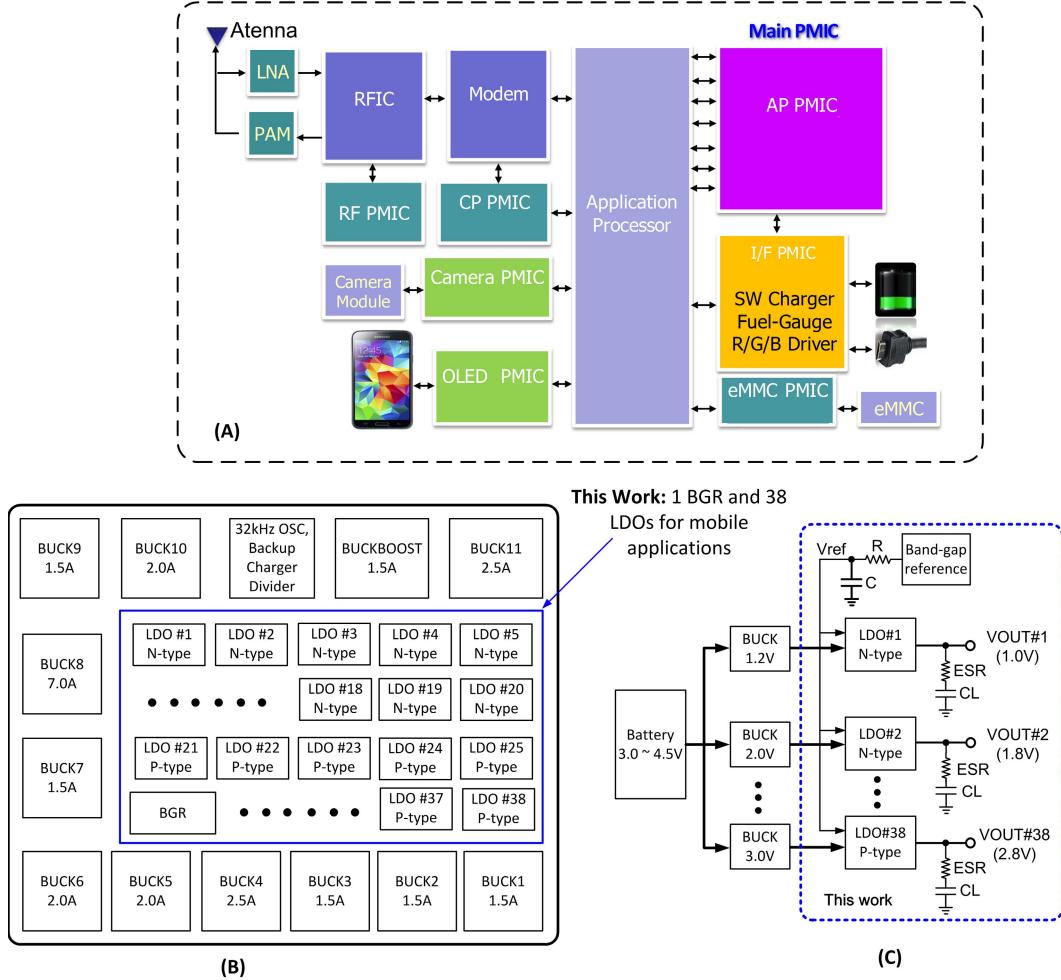


Fig. 1. (A) Implementation of PMIC units in mobile phone applications. (B) Floor plan of AP PMIC. (C) Connection diagram of bucks, LDOs, and BGR in the AP PMIC shown in (A).

power transistor M_{NP} . Consequently, a step output current load results in a big undershoot/overshoot due to long time response (Δt_1) for charging and discharging the parasitic capacitance, which is explained by the following equation [1]:

$$\Delta t_1 \approx \frac{1}{BW_{CL}} + C_{par} \times \frac{\Delta V_{par}}{I_{sr}} \quad (1)$$

where BW_{CL} , C_{par} , ΔV_{par} , and I_{sr} are the closed loop bandwidth, parasitic capacitance at the gate of M_{NP} , the voltage variation at C_{par} , and slewing current for driving C_{par} , respectively. From (1), to reduce undershoot (i.e., short Δt_1), the LDO requires bigger slewing current I_{sr} , wider bandwidth BW_{CL} , and less parasitic capacitance. These requirements result in a bigger bias current of the LDO.

In Fig. 2(B), to obtain a better driving capacity for the power transistor M_{NP} , the LDO is inserted with a buffer in between Opamp and M_{NP} . The buffer introduces high input impedance and low output impedance to improve the load transient characteristic. However, the addition of this buffer requires more bias current, which is not desired in mobile applications. Even with the insertion of a buffer into the LDO as shown in Fig. 2(B), the bandwidth of the LDO is still bottlenecked at the buffer output due to big parasitic capacitance introduced

by M_{NP} as shown in Fig. 2(C). Consequently, the output ripple is amplified by the Opamp so that a bigger ripple is created at the EAO node as shown in Fig. 2(C), but only a small ripple is generated at the gate node, slowing down the response of the system.

The LDO system as shown in Fig. 2(B) introduces one zero and three poles P_1 , P_2 , and P_3 , where P_1 is designed to be the dominant pole, P_3 is the load pole, which varies with load current I_{LOAD} , and P_2 is the output buffer pole. These poles and zero are given as

$$P_1 = \frac{1}{2\pi \times R_{out-EAO} \times C_{1\text{parasitic}}} \quad (2)$$

$$P_2 = \frac{1}{2\pi \times R_{out-GATE} \times C_{2\text{parasitic}}} \quad (3)$$

$$P_3 = \frac{1}{2\pi \times (R_{LOAD}/R_{equ}) \times CL} \quad (4)$$

$$Z_1 = \frac{1}{2\pi \times ESR \times CL} \quad (5)$$

where $R_{out-EAO}$, $R_{out-GATE}$, and R_{LOAD} are resistances seen at the output terminals of Opamp, BUFFER, and VOUT,

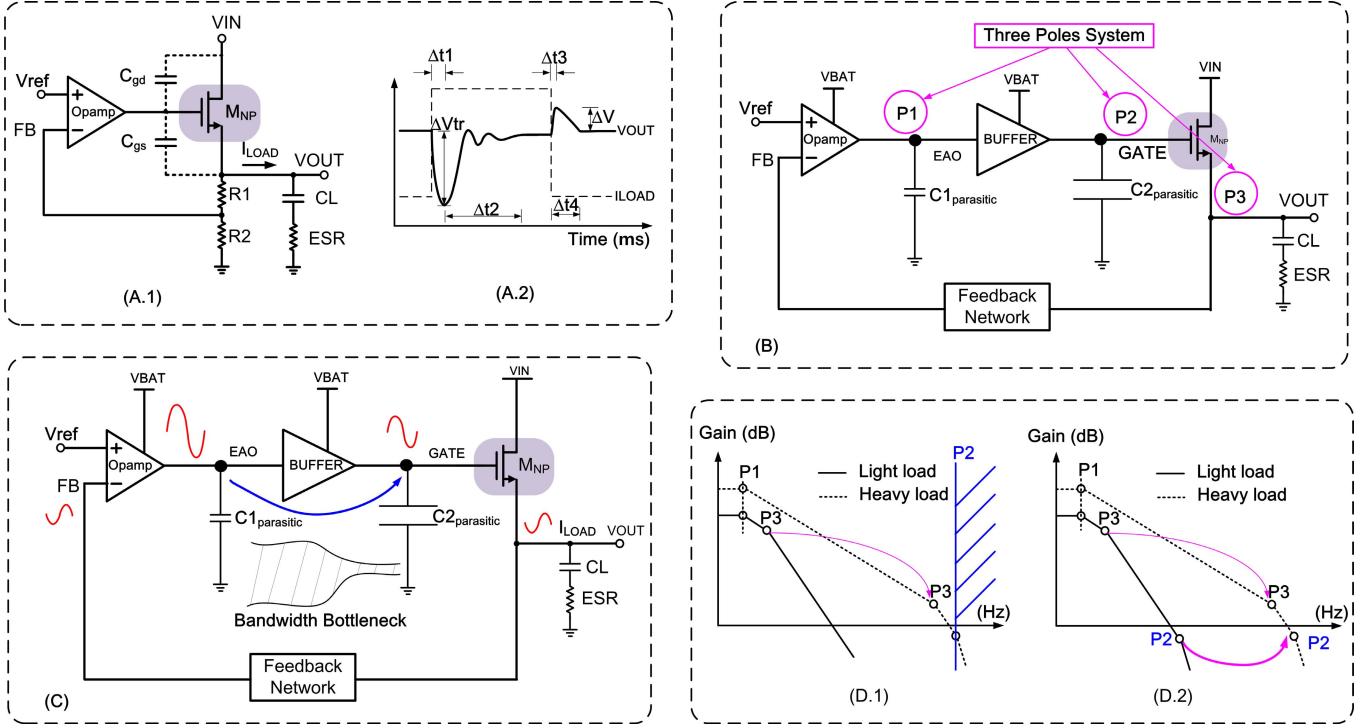


Fig. 2. (A.1) Conventional LDO design. (A.2) Typical transient response. (B) Block diagram of the LDO with a buffer for better driving capacity. (C) Bandwidth bottleneck in LDO design. (D) Poles movement of the LDO with I_{LOAD} for the case of (D.1) without dynamic-bias and (D.2) with dynamic-biasing technique.

respectively. R_{equ} is the equivalent resistance looking into the feedback network and the source of the power transistor M_{NP} . $C_{1\text{parasitic}}$ and $C_{2\text{parasitic}}$ are parasitic capacitances introduced at the output of Opamp and BUFFER, respectively.

Fig. 2(D) shows the pole locations of the LDO shown in Fig. 2(B) for two cases; light- and heavy-load conditions. Since the pole at V_{OUT} ($P3$) varies with output current load, to maintain the stability of the LDO system, the pole at $P2$ must be located at a higher frequency than that of $P3$ at maximum I_{LOAD} and there must be a zero compensation added to the systems to cancel the pole $P3$. The pole $P2$ is proportional to the output impedance of the buffer and $C_{2\text{parasitic}}$. Usually, the output impedance of the buffer is designed to be inversely proportional to buffer's bias current as will be explained in Section IV. Therefore, to locate $P2$ at higher frequency as shown in Fig. 2(D.1), the LDO requires a very big bias current for the buffer, which is not desired in portable applications. Consequently, the dynamic-biasing technique is usually adopted that dynamically biases the buffer based on the load current such that the pole $P2$ moves together with load current as shown in Fig. 2(D.2) [4]–[19]. The dynamic-biasing technique is excellent to reduce the required bias current; however, the speed limitation of current sense generates other design problems, such as oscillation during transient response to a step output load, which increase undershoot/overshoot as will be explained in Section III [1].

B. State-of-the-Art LDO Designs

In the state-of-the-art low quiescent current and fast-transient LDO design, there are many reported works

recently [1]–[19]. However, many of them find limitations in system-on-chip (SoC) portable commercial product adoptions, where the output load current may be up to 600 mA with very low dropout voltage for system efficiency optimization. Additionally, a huge number of LDOs is demanding with low quiescent current while featuring excellent load/line transients as well as load/line regulations. Reference [2] reported a fast-transient LDO design, where the output ripple is amplified and fed back to the gate terminal of the power transistor for rapidly charging and discharging the parasitic capacitor such that fast transient response is obtained. However, the proposed idea finds difficulties in commercial low-quiescent product adoptions, because the Opamp still requires a high bias current, since there is no dynamic-biasing technique. Reference [3] reported a fast-transient LDO architecture that divides the power transistor M_{NP} into many sub-transistors with smaller sizes to reduce the parasitic capacitance at the gate terminal so that fast transient response can be obtained. However, the division of M_{NP} into many sub-transistor blocks and the requirement of many buffers results in bigger bias current. To overcome the limitation of the above-mentioned topologies, Kadanka reported a new topology [2] that includes the dynamic-biasing technique and output ripple detection circuits for rapidly biasing the internal circuits for better load transient. However, the current sense in this topology may suffer from speed limitation that result in output voltage ringing during transient response as will be explained in Section III. Another LDO topology that features dynamic-biasing and low quiescent current has been reported in [5]. The reported LDO can obtain low bias current, which is

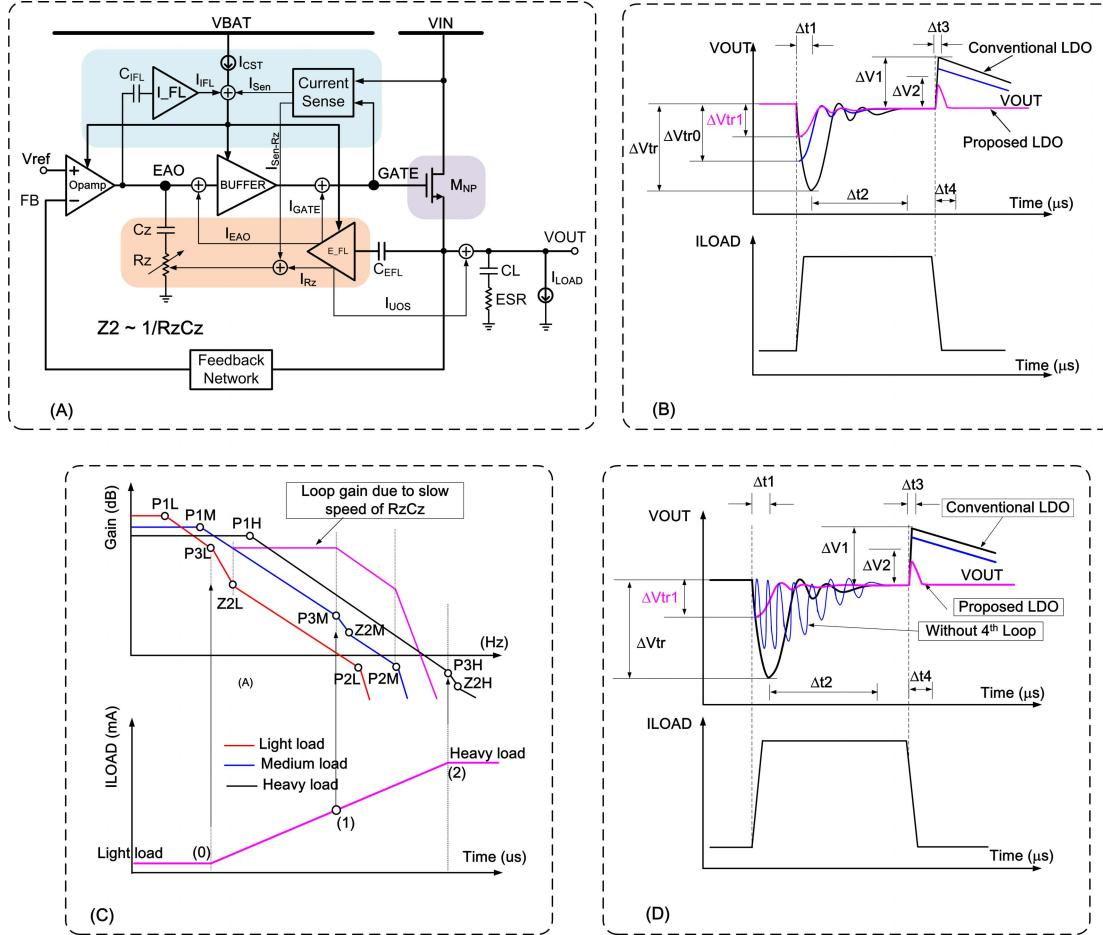


Fig. 3. (A) Proposed multiple-loop n-type LDO block diagram. (B) Load transient improvement by different loops. (C) Poles and zero vary with I_{LOAD} . (D) Fourth loop for ringing suppression.

suitable for mobile application; however, the LDO offers 24 mV of transient response as load current steps from 0 to 50 mA, which is not suitable for applications that require fast transient response, such as memory applications. Another LDO topology with wide-bandwidth and utilizing multiple feedback loops is proposed by Hong and Cho [6]. However, the proposed LDO in [6] shows big undershoot (96 mV) and overshoot (120 mV) characteristics as load current steps from 0 to 150 mA with 150 mA/ μ s. The load-transient characteristic of [6] may not be suitable for portable applications where a fast transient response is required, such as memory, dynamic random-access memory (DRAM), MIF, and so on. Other capless LDOs have been reported in [8], [10], and [13], designing for a load current up to around 200 mA. The limited load current mainly due to big undershoot/overshoot at the output of the LDO due to no capacitor is inserted at the output terminal. These capless LDOs usually show poor performances in terms of load and line regulations as can be seen in [8], [10], and [13]. Moreover, the load current for SoC portable applications can be required up to 600 mA such that these capless LDOs may introduce very big load/line transient ripple, which is problematic in SoC portable applications.

As discussed previously, there are many proposed LDO topologies in the state of the art, which feature capless, fast

transient, low bias current, low noise, and so on [2]–[19]. However, for SoC portable commercial product developments, LDOs are required to supply up to 600 mA of the load current at a very stable operation over a wide range of operating conditions. Additionally, the LDOs are required to offer excellent performance with a minimum bias current, and more importantly, the circuit operation/analysis must be simple enough for easy design verifications. Consequently, this paper proposed a new multiple-loop design technique for LDO that offer a low quiescent current with excellent performance improvement compared with prior reported works in terms of undershoot, overshoot, and so on. The proposed LDO includes five feedback loops; however, the design and analysis is very simple that it can be easily implemented by designers for commercial product developments. The design has been adopted for many commercial products of Samsung.

III. BLOCK DIAGRAM OF THE PROPOSED MULTIPLE-LOOP LDO DESIGNS

Fig. 3(A) shows the proposed multiple-loop LDO block diagram, which features very low quiescent current and small undershoot/overshoot characteristics. Similar to Fig. 2(B), the LDO in Fig. 3(A) offers three poles and two zeros, which are given in (2)–(5). Another zero is formed by a series

connection of R_z and C_z , which is designed to track the load pole ($\omega_{z2} = 1/C_z \times R_z$). The resistor R_z is controlled by two bias currents, which are $I_{\text{Sen}-R_z}$ and I_{R_z} as shown in Fig. 3(A). The combination of the I_{FL} and E_{FL} blocks results in a low bias-current requirement which still offers excellent load transient characteristic as will be explained later. In Fig. 3(A), the proposed LDO includes five loops, which are briefly described as follows.

- 1) The first loop includes circuit blocks, such as Opamp, BUFFER, power transistor M_{NP} , and the feedback network. This main loop maintains V_{OUT} as a function of the reference voltage (V_{ref}). As shown in Fig. 3(A), the bias current for Opamp, BUFFER, and external fast loop blocks is the sum of three current signals: a constant bias current (I_{CST}), the sensing current I_{Sen} , and the current coming from internal fast loop (I_{IFL}). Detailed circuit description of the Opamp, BUFFER, and feedback network will be given in Section IV-A.
- 2) The second loop includes the current-sense block that senses the output load current I_{LOAD} and generates I_{sen} , which is proportional to I_{LOAD} . This loop dynamically biases the LDO with minimum bias current at no load condition. At no load condition, to minimize the bias current of the overall LDO system, only a small bias current from M_{NP} flows into the feedback network; therefore, the pole at V_{OUT} terminal (P3) moves closely to dominant pole (P1). The zero generated by R_z and C_z is required to move to very low frequency to cancel P3 such that the resistance R_z and capacitor C_z are required to be very big.
- 3) The third loop is an external fast loop (E_{FL}) that senses and amplifies the output voltage ripple through an on-chip capacitor C_{EFL} to generate four current signals I_{GATE} , I_{EAO} , I_{R_z} , and I_{UOS} for rapidly charging/discharging the parasitic capacitors at the GATE/EAO/RZ/VOUT node, respectively. Note that, different from prior arts [2]–[5], this loop speeds up the operation of all internal circuits with minimum bias currents. Consequently, the LDO can obtain very fast transient response with low quiescent current. Detailed schematic and circuit operation of the E_{FL} block will be offered in Section IV-A.
- 4) The fourth loop is the sum of the second and third loops to provide two current signals ($I_{\text{Sen}-R_z}$ and I_{R_z}) for controlling the resistance R_z to rapidly move the zero Z_2 together with load's pole such that suppressing the output voltage ringing during load transient operation as will be explained in detail in Section IV-A.
- 5) The fifth loop as shown in Fig. 3(A) includes the I_{FL} block that senses the ripple at EAO node to generate a high-speed slewing current I_{IFL} for eliminating the bottleneck effect of the BUFFER. As shown in Fig. 2(C), there is a big parasitic capacitor at the GATE node, which is introduced by the power transistor M_{NP} ; however, the driving capacity of the BUFFER is limited due to a minimized bias current. Consequently, there is a bandwidth bottleneck at the BUFFER output. The

fifth loop takes the advantage of a fast-transient ripple at the Opamp output terminal (thanks to a small parasitic capacitor) to generate a high-speed slewing bias current for the BUFFER. Consequently, the fifth loop improves the driving capacity of the BUFFER to eliminate the bottleneck effect. The Opamp block amplifies the output ripple such that relaxing the gain/bandwidth requirement of the I_{FL} block. Therefore, there is a minimum required quiescent current for operating the I_{FL} block, leading to a minimum bias current for the LDO system. The detailed schematic and circuit operation will be presented in Section IV-A.

Fig. 3(B) briefly explains how each loop help to improve load-transient characteristic of the proposed LDO. In Fig. 3(B), without internal and external fast loops (I_{FL} and E_{FL} blocks), a fast step output load introduces a big undershoot and overshoot due to a long time (Δt_1) that is required to charge and discharge the capacitor C_{par} at the GATE terminal. The conventional LDO shows big load transient response as shown in Fig. 3(B) (black curve). In our proposed LDO, by using the E_{FL} circuit, the load transient is improved from the black curve to the blue curve as shown in Fig. 3(B). Moreover, by utilizing both the E_{FL} and I_{FL} blocks, the load transient can be improved from the black to the pink curves as shown in Fig. 3(B), corresponding to output ripple improvement from ΔV_{tr} to $\Delta V_{\text{tr}1}$ and ΔV_1 to ΔV_2 for undershoot and overshoot voltages, respectively.

Fig. 3(C) shows the poles and zero locations of the proposed LDO in Fig. 3(A) for three conditions: light (L), medium (M), and heavy (H) loads. Note that the poles and the zero are given in (2)–(5). Due to the dynamic-biasing loop formed by the current sense circuit, the dominant pole P1 is varied from P1L to P1H for light and heavy loads, respectively. Similarly, P2,3 and the zero Z2 are also varied based on the sensing current I_{sen} as shown in Fig. 3(A) and (C). In Fig. 3(C), as a fast-step load current is applied at V_{OUT} , if the speed of zero (Z2) is slower than that of the output pole (P3), then the overall system loop gain follows the pink curve as shown in Fig. 3(C), which introduces three poles and just one zero (unstable system). Consequently, the LDO introduces poor phase margin, which leads to output voltage ringing during undershoot operation as shown in Fig. 3(D) (blue curve). In our design, the fourth loop is utilized to move Z2 together with P3 versus load current variation such that the output ringing is removed as explained in Fig. 3(D) (pink curve). In Fig. 3(A), with a minimum quiescent current, the output pole (P3) is closed to the dominant pole (P1) at no load condition. Consequently, a big size of C_z and R_z is required to place the zero (Z2L) closed to P3 as shown in Fig. 3(C) (red line). As C_z and R_z become bigger it takes more time to move this zero as output load current varies. However, the fourth loop uses E_{FL} amplifier to generate currents for rapidly changing the value of R_z such that moving the zero ($1/R_z C_z$) with a higher speed together with the output pole. Consequently, the LDO system returns to two poles and one zero system, which is stable and there is no voltage ringing at V_{OUT} .

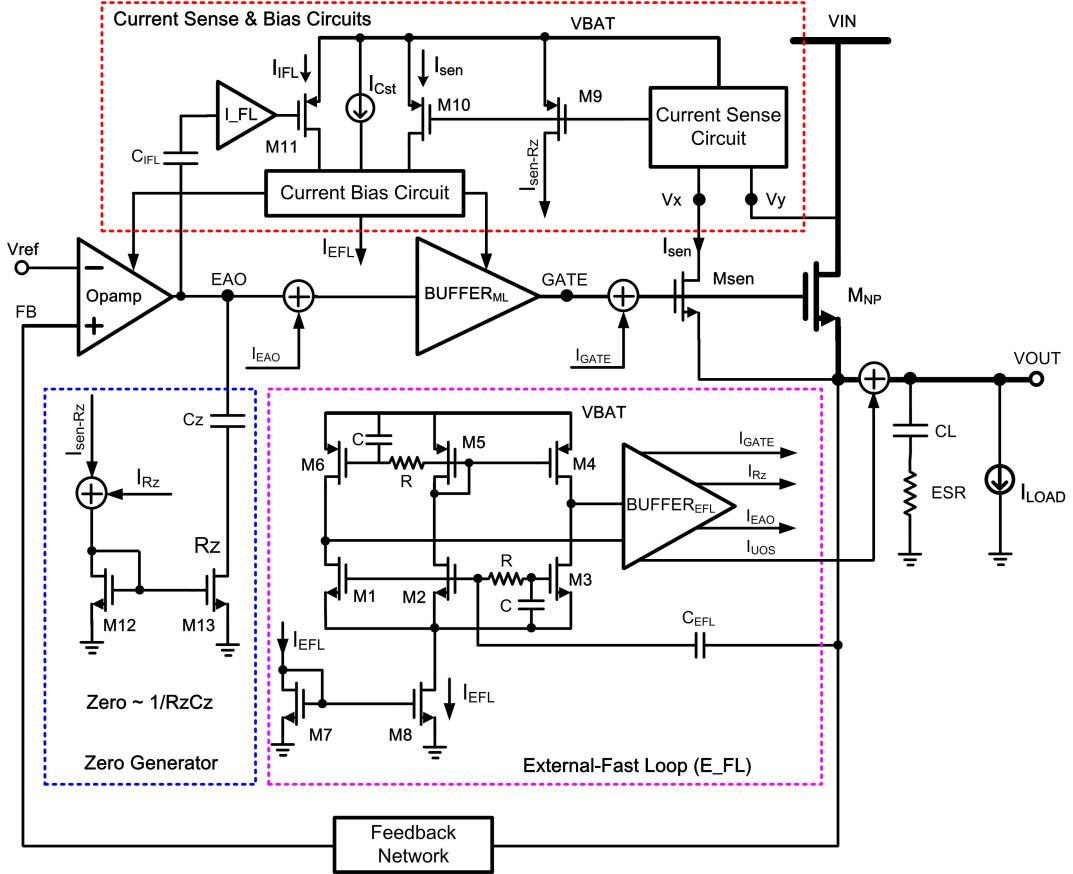


Fig. 4. Simplified schematic implementation of the proposed LDO shown in Fig. 3(A).

IV. SCHEMATIC IMPLEMENTATIONS AND STABILITY ANALYSIS

A. Schematic Implementations

The proposed LDO as shown in Fig. 3(A) has many feedback loops; therefore, for simple circuit analysis, the overall LDO system is broken into many sub-circuits. Fig. 4 shows an overall simplified schematic implementation of the proposed multiple-loop LDO as given in Fig. 3(A). The schematic of Opamp, buffer, current sense, feedback network, and current bias circuits will be described in detail in this section. Additionally, the zero generator block is simplified with a summing of two currents $I_{\text{Sen}-Rz}$ and I_{Rz} that flows into the diode-connected transistor M12, which generates the bias voltage for biasing transistor M13. The resistance Rz is taken from drain to source of M13. The transistor Msen is utilized to sense the load current (I_{LOAD}) flowing through the power transistor M_{NP} . In Fig. 4, the current sense circuit forces the voltages V_x and V_y to be equal such that the current sense error due to the drain-to-source voltage difference between Msen and M_{NP} is minimized. As shown in Fig. 4, the bias current for all internal circuits are the sum of the sense current I_{sen} , the constant bias current I_{Cst} , and a current signal generated by the internal fast loop I_{IFL} .

In Fig. 4, the external fast loop is composed of transistors from M1–M8, R , C , and the buffer (BUFFER_{EFL}) to generate four currents I_{GATE} , I_{Rz} , I_{EAO} , and I_{UOS} . As shown in Fig. 4,

the transistors M1–M3 require a bias voltage which is not shown here. Note that, if VOUT is directly connected to the gate of M_{NP} , then VOUT serves as the voltage bias for M1–M3. The detailed circuit operation of the external fast loop will be explained in more detail in Figs. 5–7 in this section.

Fig. 5 shows the schematic of the current sense, the internal fast loop, and the current bias circuit blocks as briefly given in Fig. 4. As shown in Fig. 5(A), the current sense block is composed of transistors Msen, MS1–MS4, M9, and M10, and two bias currents (IB1). The sensing ratio is defined as $K = M_{\text{NP}} / M_{\text{sen}}$ and $I_{\text{sen}} = I_{\text{LOAD}} / K$, where M_{NP} and M_{sen} are aspect ratios of M_{NP} and M_{sen} , respectively. In Fig. 5(A), the transistors MS1 and MS2 form a current mirror and being biased by the same bias current IB1. All bias currents are flowing into resistors divider $R2/R1$. In the case of no load current ($I_{\text{LOAD}} = 0$), the bias current flowing into resistor divider $R2/R1$ is equal to $\text{VOUT}/(R1 + R2)$. Consequently, the bias current IBIAS can be calculated as

$$\text{IBIAS} = \frac{\text{VOUT}}{(R1+R2)} = 2 \times \text{IB1} + I_0 \left(1 + \frac{1}{K} \right). \quad (6)$$

Usually, circuit designers try to minimize the bias current IBIAS to improve efficiency at light load operation. In our designs, the IB1 is biased with $0.5 \mu\text{A}$ such that the speed of the current sense block as shown in Fig. 5(A) is dramatically limited, leading to big load transient characteristic. Fortunately, the combination of I_{FL} and E_{FL} blocks helps

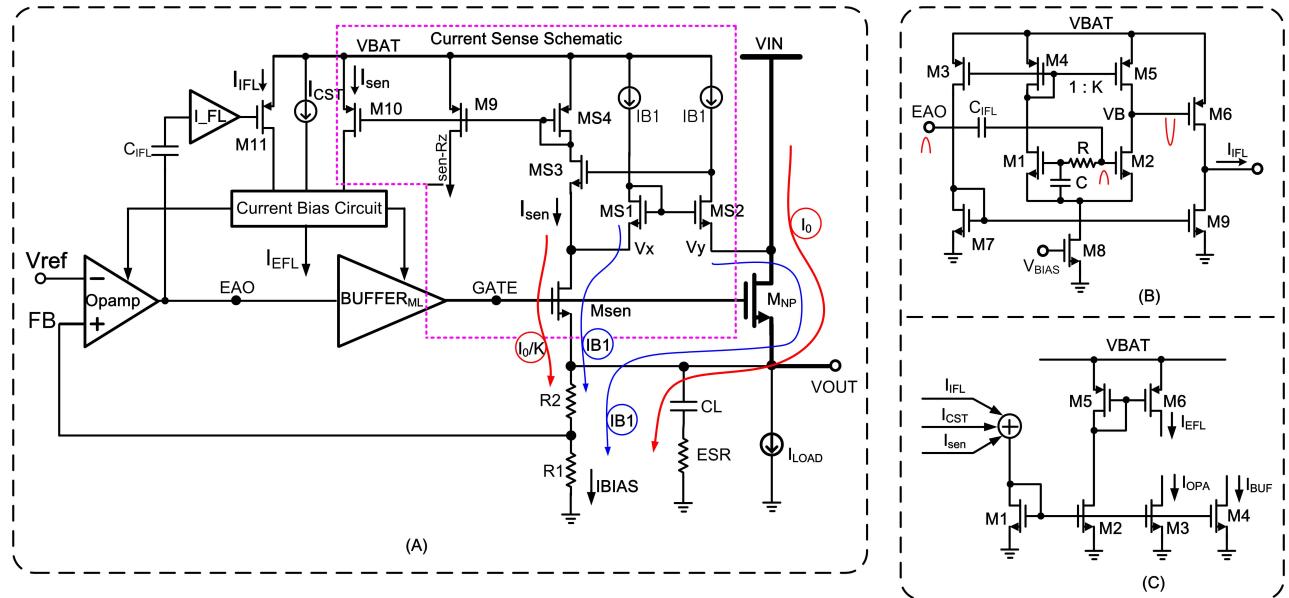


Fig. 5. (A) Schematics of the current sense in Fig. 4. (B) Schematics of the internal fast loop in Fig. 4. (C) Schematic of the current bias circuit as shown in Fig. 4.

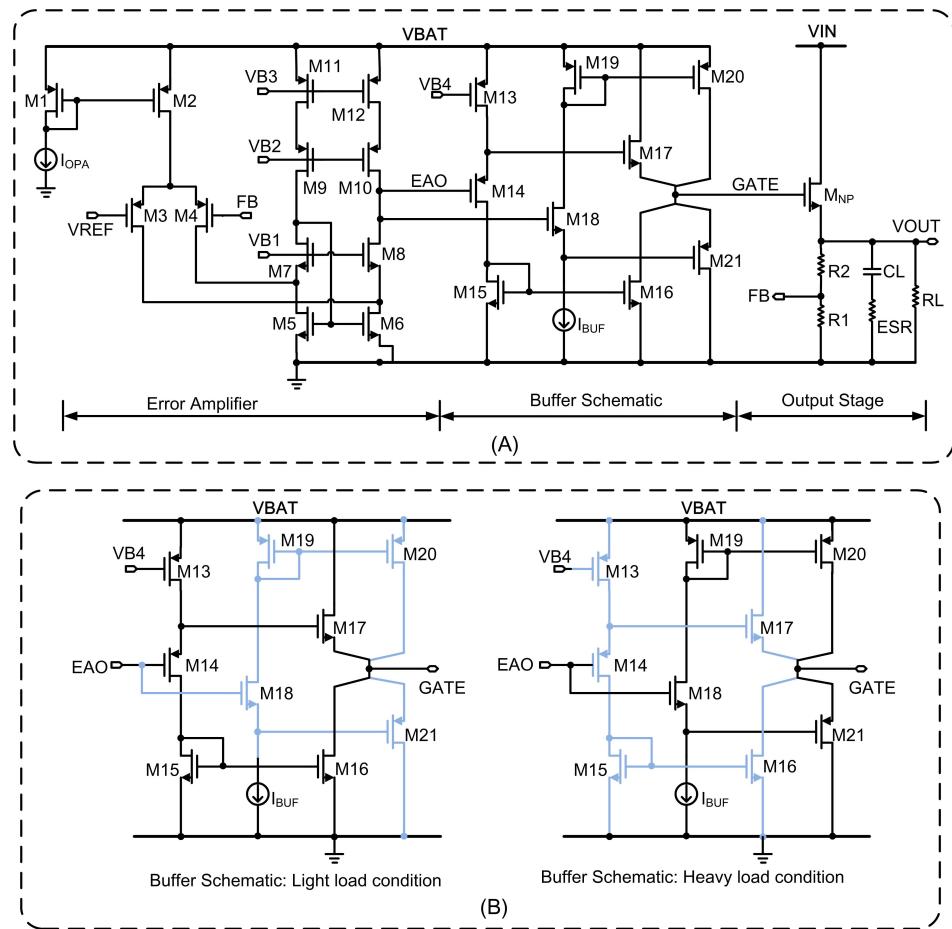


Fig. 6. (A) Detailed schematics of the error amplifier and buffer as shown in Fig. 4. (B) Buffer operation for light load and heavy load.

to speed up the current bias circuit block such that even with a minimum quiescent current, the LDO still offers excellent load transient characteristic. The reason is as follows: since

the LDO adopting dynamic biasing technique, the sensing current I_{sen} is proportional to the current I_{LOAD} . In Fig. 5, the voltage at GATE node defines the sensing current I_{sen}

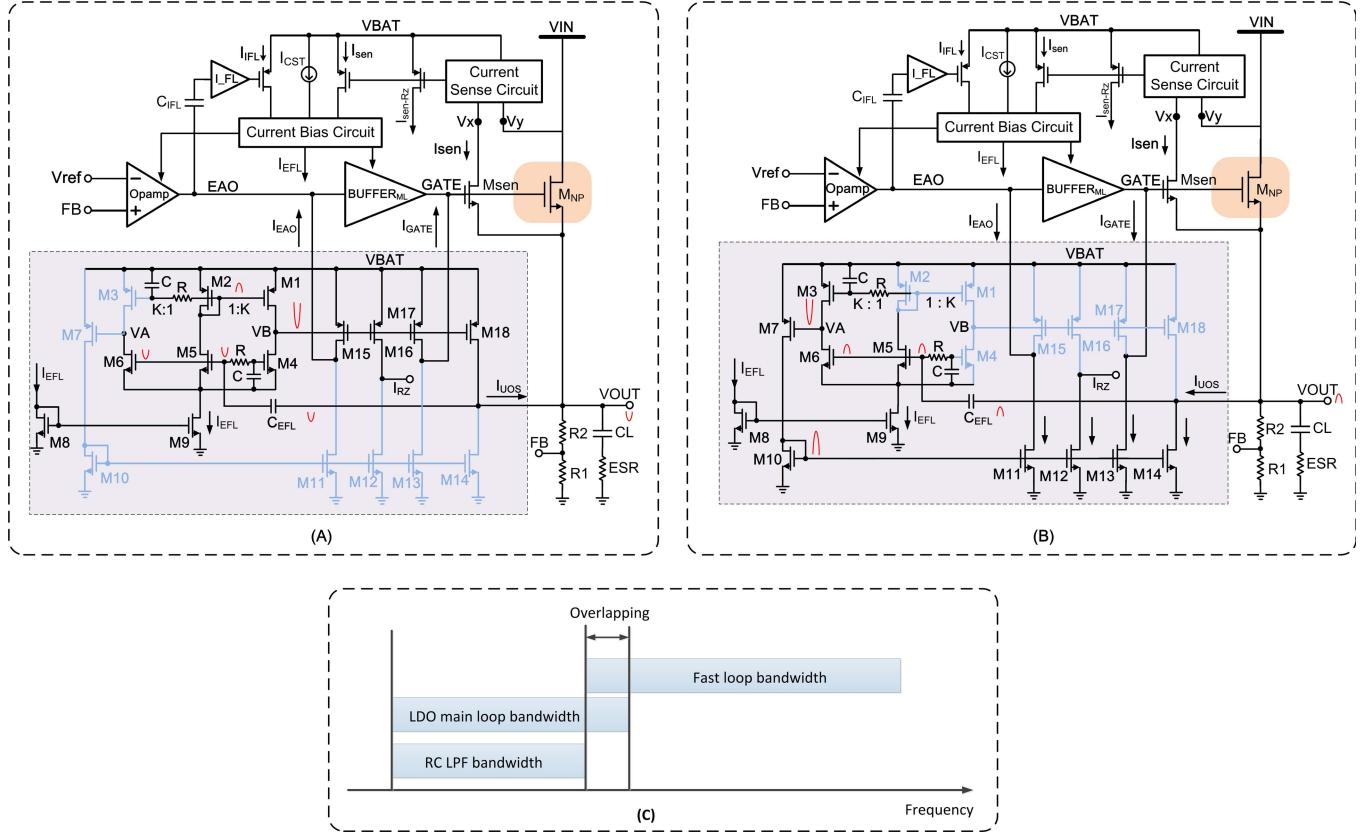


Fig. 7. Schematic of the external fast loop (E_{FL}) for (A) undershoot suppression, (B) overshoot suppression, and (C) Bandwidth descriptions for RC calculation.

flowing through Msen. Unfortunately, there is a big parasitic capacitor introduced at the GATE node due to a big layout size of M_{NP} and the slewing current for charging/discharging this capacitor comes only from the BUFFER_{ML} with a limited current driving capacity. Consequently, the voltage at GATE node slowly responses to the variation of I_{LOAD} , leading to slow speed of the current sense. In our proposed topology, the external fast loop (E_{FL}) and the internal fast loop (I_{FL}) generate a high speed current to charge/discharge the gate parasitic capacitance of M_{NP} in response to the load transient current. Consequently, the response speed of the voltage at GATE node to the load current transient becomes faster; therefore, the current sense I_{sen} is rapidly generated and finally the current bias circuit becomes faster.

Fig. 5(B) shows the schematic of the internal fast loop block, which amplifies the voltage ripple at EAO node and outputs a current signal I_{IFL} for biasing internal circuits. Consequently, this circuit block can be designed as a transconductance amplifier as shown in Fig. 5(B). In Fig. 5(B), the filter formed by R and C suppresses the signal path from EAO to the gate of M1. As shown in Fig. 5(B), if the undershoot occurs at VOUT node, the EAO node voltage will be increased so that the voltage at VB is pulled down. Consequently, the current I_{IFL} flows from VBAT through M6 to the current bias circuit block. I_{IFL} rapidly increases the bias current for all internal circuits such that increasing the bandwidth of the LDO and finally suppress the undershoot ripple at the output terminal.

Fig. 5(C) shows the schematic of the current bias circuit block, where the three currents $I_{IFL}/I_{CST}/I_{sen}$ are summed and flow into the transistor M1. Through current mirrors by M2–M6, the corresponding bias current for Opamp, BUFFER, and external fast loop is generated.

Fig. 6(A) shows the schematic of the Opamp (error amplifier) and BUFFER_{ML} of the proposed LDO shown in Fig. 4. The bias currents I_{OPA} and I_{BUF} are from the bias circuit block as shown in Fig. 5(C). The error amplifier use PMOS transistors M3 and M4 as the input-different pair and the cascode current mirror for current summing. The cascode current mirror structure (M5–M12) is utilized to obtain high impedance at EAO node so that the dominant pole (P1) is located at very low frequency for easy loop compensation. The buffer schematic block adopts a push-pull structure and features high input impedance and low output impedance. The output impedance of the Buffer (R_{buffer}) is proportional to $(1/gm\text{-}M17)/(1/gm\text{-}M21)$, where $gm\text{-}M17$ and $gm\text{-}M21$ are trans-conductances of transistors M17 and M21.

Fig. 6(B) explains the operation of the buffer shown in Fig. 6(A) for the conditions of light- and heavy-load operations. In the case of light-load operation, the EAO and GATE voltages are very low such that transistors M18–M21 are turned OFF so that the dominant signal path is formed by transistors M13–M17. In this condition, the buffer bias current I_{BUF} is the lowest, since I_{LOAD} is low. Differently, Fig. 6(B) (right) shows buffer's operation in heavy load condition. As the load current increase, the buffer current

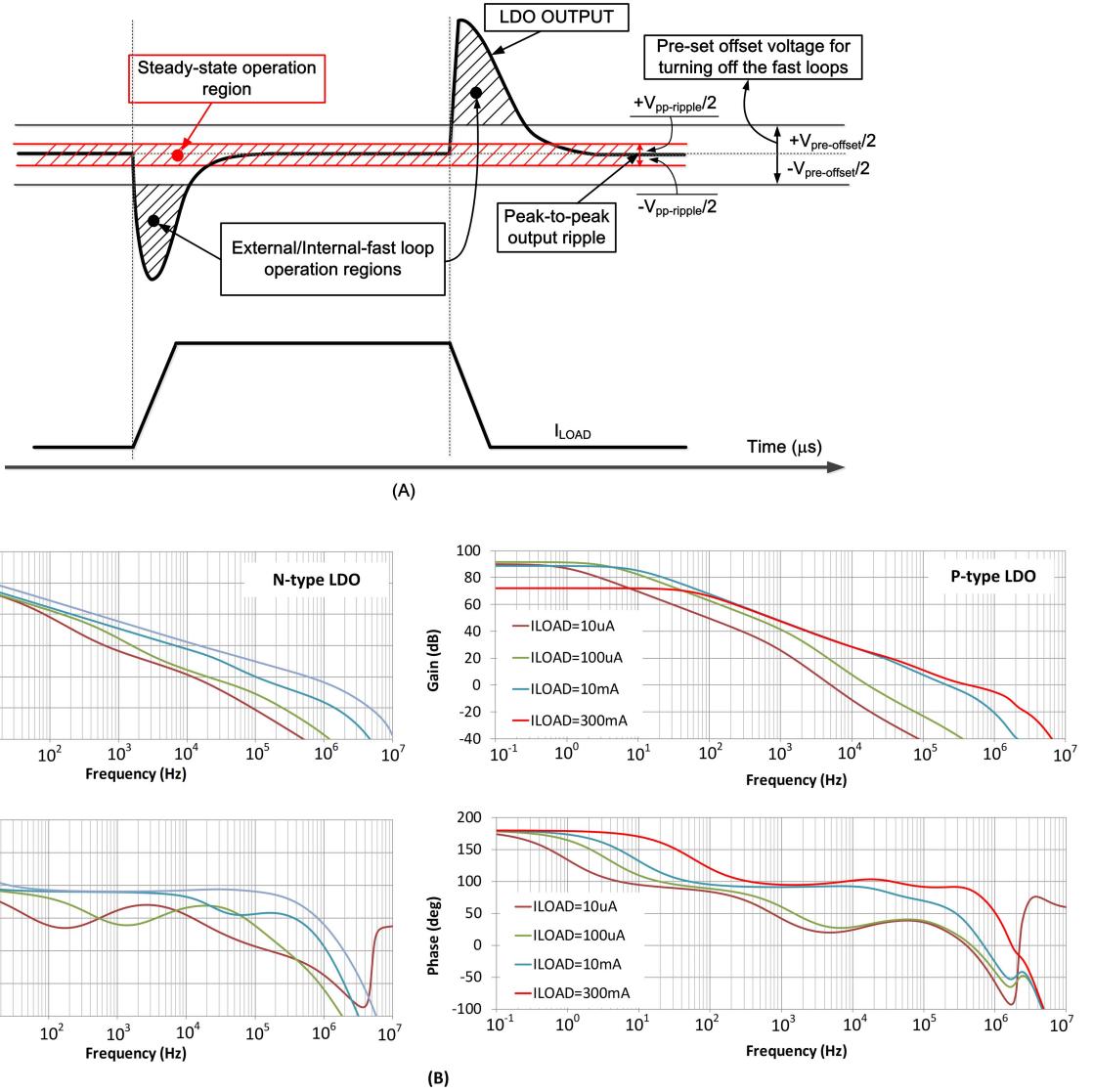


Fig. 8. (A) Operation regions of the proposed LDO at steady-state and undershoot/overshoot conditions. (B) Simulation results of gain/phase of the proposed n-type and p-type LDOs.

I_{BUF} is also increased and the EAO voltage is increased such that the transistors M18–M21 are gradually turned ON. At heavy load condition, the voltage at node EAO moves closely to VBAT such that M18 is fully turned ON while M14 is fully turned OFF. Consequently, the dominant signal path for heavy load condition comes from EAO through M18–M21 to the GATE. As the load condition changes from light to heavy or heavy to light, the EAO node voltage smoothly moves from high to low or low to high such that the operation transitions are simultaneous. At middle load condition, both the circuits in Fig. 6(B) are simultaneously operating. The push–pull structure of the buffer is adopted for faster load transient response.

Fig. 7 shows the schematic of the external fast loop block, which is composed of transistors from M1 to M18. The circuit operation for suppressing output undershoot and overshoot ripples is given in Fig. 7(A) and (B), respectively. The output ripple is coupled to the gate of transistors M5 and M6 through

the capacitor C_{EFL} , and is amplified to provide a bigger output ripple at VA and VB terminals. The resistor R and capacitor C form two low-pass filters with a frequency cutoff of $1/(2\pi RC)$ to block the output ripple coming to the gate terminal of transistors M3 and M4. In other words, with the help of RC filter, stable dc bias voltages are supplied to the gate terminals of M3 and M4, which are equal to the dc bias voltages at the gate terminals of M2 and M5, respectively. The bigger the value of RC , the better that it can suppress the ripple coming to the gate of M3 and M4. However, the minimum value of RC should be calculated with respect to the minimum bandwidth of the fast loop or the maximum bandwidth of the LDO as shown in Fig. 7(C). For example, if the LDO main loop bandwidth is around 300 kHz, then the fast loop should be designed with operating from around 250 kHz (50 kHz overlapping). The cutoff frequency of RC should be lower than 250 kHz. One can choose the values of $R = 500 \text{ k}\Omega$ and $C = 2 \text{ pF}$ such that the LPF with a cutoff frequency

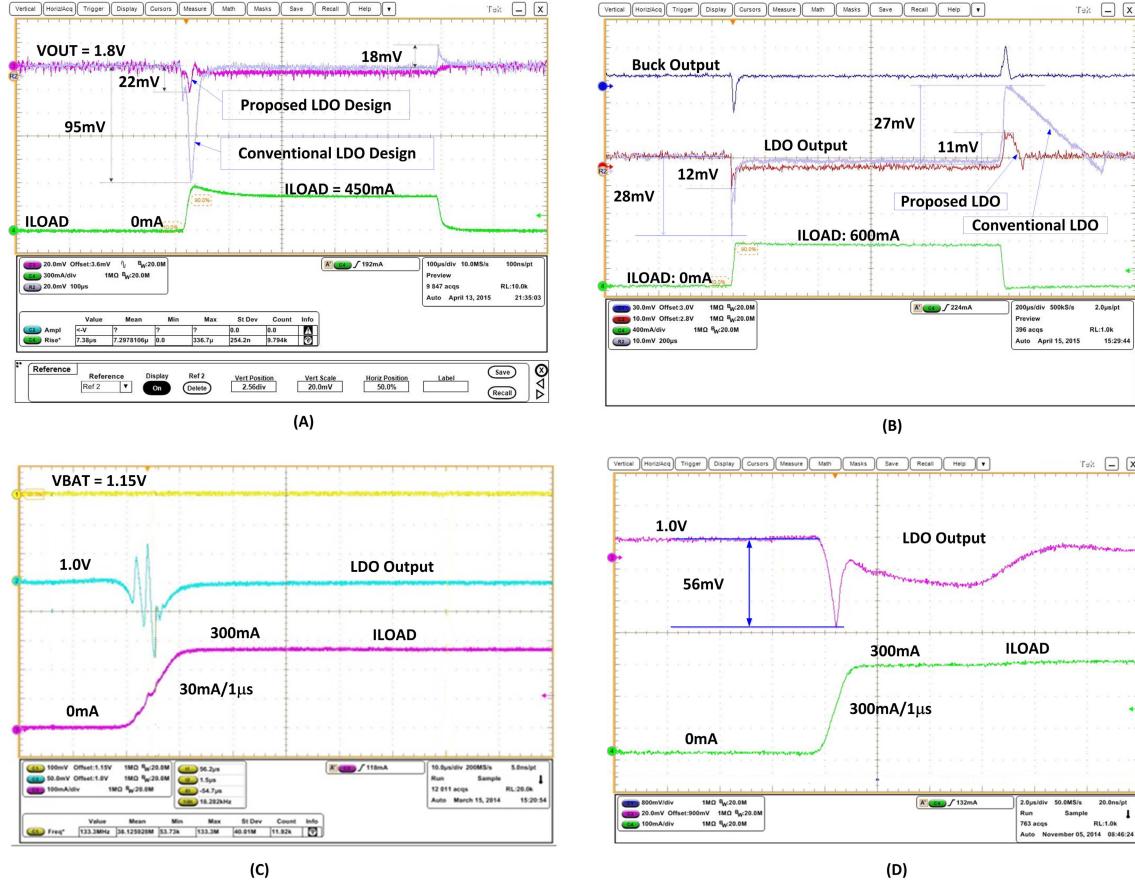


Fig. 9. (A) Measured load transient responses of the proposed n-type LDO with and without the proposed techniques. (B) Measured load transient response of the proposed p-type LDO with and without the proposed techniques. (C) Output ringing of n-type LDO without fourth loop operation. (D) Measured load transient of the n-type LDO at $V_{OUT} = 1$ V and $300 \text{ mA}/1 \mu\text{s}$ of I_{LOAD} .

of $1/(2\pi RC) \sim 160$ kHz, which is good enough for this application.

The current bias for M4–M6 is from a current mirror formed by transistors M8 and M9, where the bias current I_{EFL} is coming from the current bias circuit block as shown in Fig. 4. Note that, for simple analysis and operation, the bias current I_{EFL} can be replaced by a fixed current source. The PMOS transistors M1–M3 are sized with a ratio $1:K$, where K is greater than unity to ensure that the voltage at nodes VA and VB are biased closely to the battery voltage V_{BAT} so that transistors M7, M15, M16, and M18 are turned OFF at steady-state operation condition. Consequently, the currents $I_{EAO}/I_{GATE}/I_{RZ}/I_{UOS}$ are equal to zero at steady-state operation, meaning that this loop is isolated from the LDO system when there is no ripple at the output node. This bias operation method is used to simplify the LDO system with many loops for relaxing design challenges for commercial product developments.

In Fig. 7(A), as output ripple is undershoot, due to the RC filter, the ripple is amplified through M5, M2, and M1 such that the ripple at VB node is significantly amplified. As shown in Fig. 7(A), as VB node voltage is pulled down, the currents $I_{EAO}/I_{GATE}/I_{UOS}$ flow from V_{BAT} through transistors M15–M18 to compensate the voltage drops at EAO/GATE/V_{OUT} terminals, respectively. Consequently, the

output undershoot is suppressed. Note that the V_{BAT} is much higher than V_{OUT} for n-type LDO so that even with a small size of M18, the current I_{UOS} can be very big for suppressing undershoot at the output node. Similarly, Fig. 7(B) explains circuit operation for overshoot suppression. In Fig. 7(B), as an overshoot signal occurs at the output terminal. Due to the RC filters, the transistors M1, M2, M4, and M15–M18 are in idle mode of operation and show negligible affection to the LDO. As shown in Fig. 7(B), the voltage VA is significantly amplified such that currents $I_{EAO}/I_{GATE}/I_{RZ}/I_{UOS}$ discharge to ground through M11–M14 to suppress overshoot ripple at the output.

B. Stability Analysis

The proposed LDO system as shown in Figs. 3(A) and 4 is composed of five loops. For relaxing design challenges in commercialized product implementations, a pre-set offset voltage ($V_{pre-offset}$) is inserted into the I_{FL} and E_{FL} loops such that these circuits are turned OFF at steady-state operation conditions. Fig. 8(A) shows the load transient behavior of the proposed LDO at a steady-state operation and during undershoot/overshoot conditions. As shown in Fig. 8(A), at the steady-state operation condition, the output of the LDO represents a range of output ripple voltage, which is coming

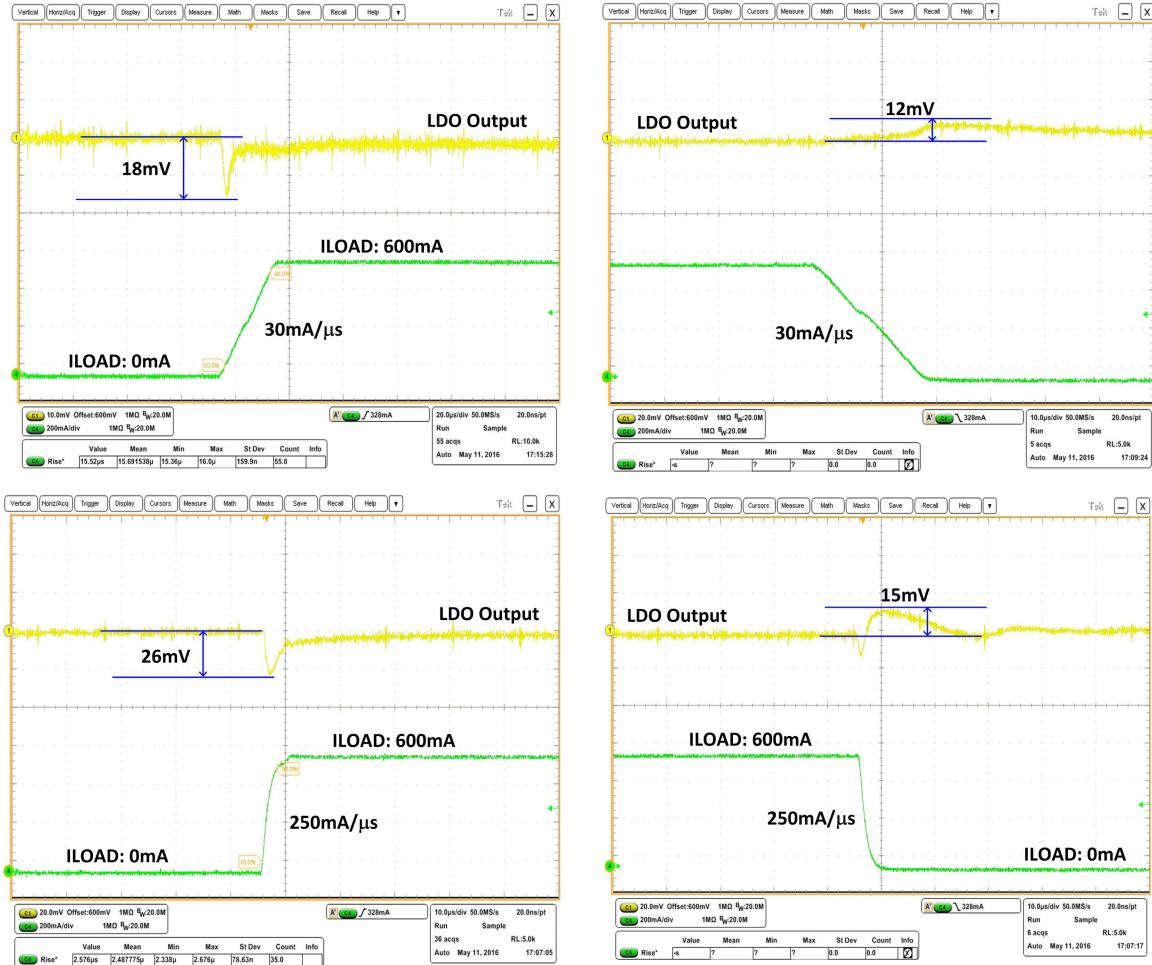


Fig. 10. Measured load transient responses for one of the n-type LDOs for DRAM applications with 30 and 250 mA/μs.

from the noises of reference voltage, Opamp, buffer, VIN, VBAT, and so on. The output peak-to-peak ripple is represented by a voltage range of $\pm V_{\text{pp-ripple}}/2$ in Fig. 8(A) and the real measured results for one of the prototype LDOs at a different set of conditions are given in Fig. 11(B). As will be discussed in Fig. 11(B), the peak-to-peak ripple in our design is within $(1/2) \times V_{\text{pp-ripple}} < \pm 3.1$ mV (peak-to-peak is under 6.2 mV) and the $(1/2) \times V_{\text{pre-offset}}$ is set at a much higher value of around ± 10 mV. As shown in Fig. 8(A), the pre-set offset voltage $V_{\text{pre-offset}}$ in our design is chosen to be always bigger than $V_{\text{pp-ripple}}$ with considering many design variation factors, such as process, temperature, VBAT, VIN, and so on. Consequently, the proposed design method ensures that at steady-state operation condition, the I_FL and E_FL loops are always turned OFF and have no effect on the loop gain and phase margin of the LDO. In Fig. 8(A), as the undershoot and overshoot falls out of the pre-set offset region, the I_FL and E_FL loops are turned ON to suppress the output ripple. In these operation regions, the LDO operation should be treated with large signal more than small signal behaviors, wherein the fast loops provide high speed slewing currents to charge/discharge the parasitic capacitors and/or bias the internal circuit blocks.

To insert the pre-set offset voltage to the fast loops, the aspect ratios of transistors M5/M4 in Fig. 5(B) and M1,3/M2 in Fig. 7 are sized to be greater than unity ($K > 1$). As shown in Fig. 5, if the size of M5 is bigger than that of M4, the voltage VB is moved toward VBAT turning OFF transistor M6, meaning that the I_FL loop is turned OFF. Similarly, the size of M1 and M3 in Fig. 7 is bigger than that of M2 so that the voltages VA and VB are biased closely to VBAT, turning OFF the E_FL loop. Consequently, the proposed LDO, as shown in Figs. 3(A), 4, and 7, is similar to the one shown in Fig. 2(B) at steady-state operation condition, which also introduces three poles and two zeros as explained in Section II-A. The first zero is generated at the output terminal and is given in (5). The other zero is generated by a series connection of Rz and Cz and is given as

$$Z2 = \frac{1}{2 \times \pi \times Rz \times Cz} \quad (7)$$

where Cz is an on-chip compensation capacitor with a value of around 10 pF, and Rz is the drain-to-source resistance of the transistor M13 as shown in Fig. 4. The small signal transfer

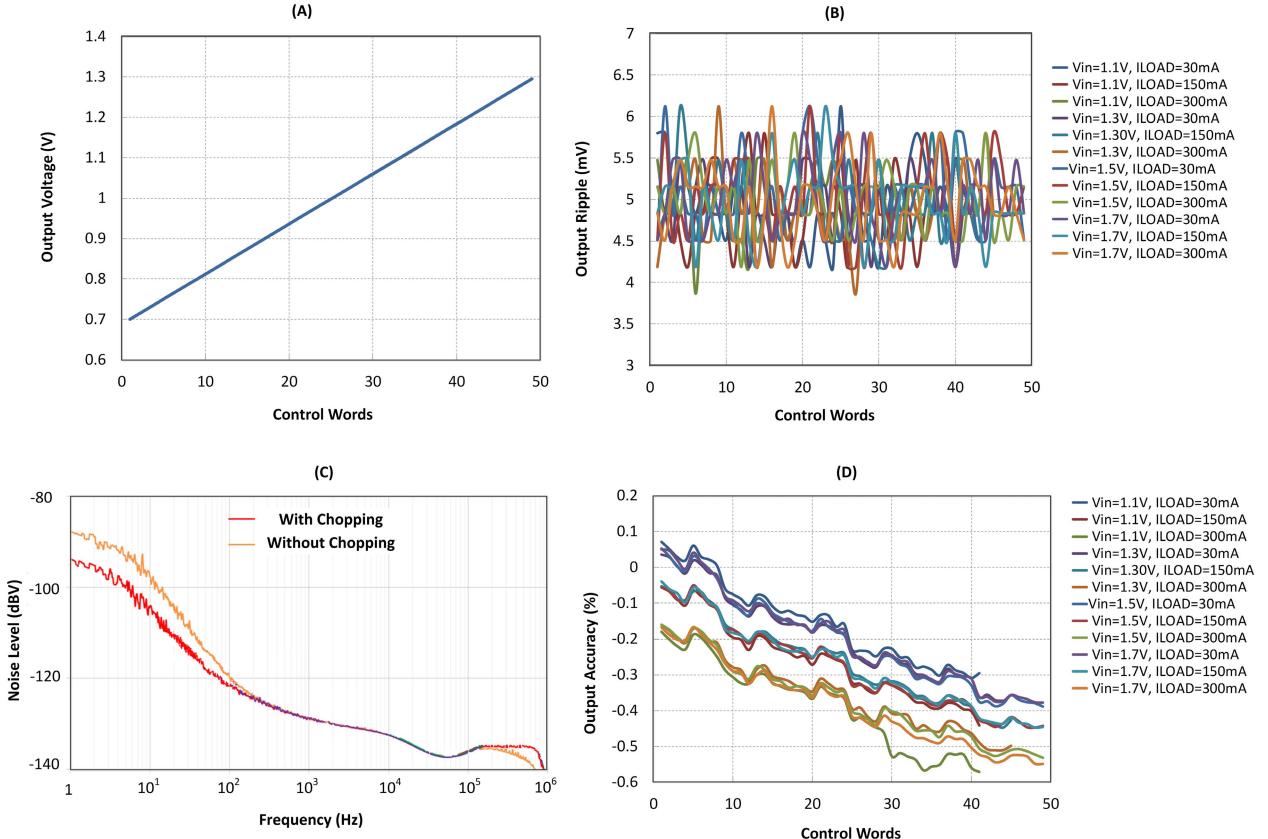


Fig. 11. (A) Measured V_{out} as function of the control bits. (B) Measured output peak-to-peak ripple at $V_{out} = 1$ V and different conditions of V_{in} and I_{load} . (C) Measured output noise level with and without chopping techniques. (D) Measured output voltage accuracy at $V_{out} = 1$ V and different conditions of V_{in} and I_{load} .

function of the proposed LDO is given as follows:

$$A_V = \frac{A_{dc} \times \left(1 + \frac{s}{Z_1}\right) \left(1 + \frac{s}{Z_2}\right)}{\left(1 + \frac{s}{P_1}\right) \left(1 + \frac{s}{P_2}\right) \left(1 + \frac{s}{P_3}\right)} \quad (8)$$

where P_1 , P_2 , P_3 , Z_1 , and Z_2 are given in (2)–(5) and (7), respectively. And, A_{dc} is the low-frequency gain, which is given as

$$A_{dc} = A_{EA} \times A_{BUFFER} \times A_{POWER} \quad (9)$$

where A_{EA} , A_{BUFFER} , and A_{POWER} are the gains of Opamp, BUFFER, and power transistor M_{NP} , respectively.

The gain/phase of the proposed LDOs has been simulated based on 0.13- μ m CMOS process. Fig. 8(B) shows the simulation of gain/phase for two LDOs, where one LDO is based on n-type and the other is based on p-type, respectively. The simulation conditions are $V_{BAT} = 3.0\text{--}4.5$ V, V_{IN} of n-type and p-type LDOs are 1.2 and 2.0 V, corresponding to V_{out} of 1.0 and 1.8 V, respectively. The simulations are conducted at I_{LOAD} of 10 μ A, 100 μ A, 10 mA, and 300 mA. Our design optimizations ensure the worst phase margin of 45° for all load conditions.

V. MEASUREMENT RESULTS

A total of 38 n-type and p-type LDOs with different load current capacities and output voltages were integrated in one PMIC chip for powering the AP processor as shown in Fig. 1.

The proposed LDO can supply currents I_{LOAD} of 50, 100, 150, 300, 450, and 600 mA with very fast transient response. The proposed LDO was verified based on 0.13- μ m CMOS process and the quiescent current for each LDO is optimized based on the maximum load current as well as the required undershoot/overshoot characteristic for different applications. The following measurement results of the LDOs for different applications will be presented.

Fig. 9(A) shows the measured load transient for one of the n-type LDOs with and without the proposed techniques for supplying the CODEC block inside the AP as shown in Fig. 1. The measured conditions are $V_{BAT} = 4$ V, $V_{IN} = 2$ V, $V_{out} = 1.8$ V, $C_L = 2.2$ μ F, and I_{LOAD} rising slope of 30 mA/ μ s. As shown in Fig. 9(A), as I_{LOAD} steps from 0 to 450 mA, the LDO with and without the proposed techniques offers 22 and 95 mV of the undershoot/overshoot voltage, respectively. Additionally, the LDO without proposed techniques introduces 18 mV of the overshoot while the proposed one shows significant improvement. The proposed LDO consumes 20 μ A of quiescent current; where the total quiescent current of the error amplifier, the buffer, and the output stage blocks in Fig. 6(A) consumes 13 μ A. The remaining circuits, such as the current sense, I_{FL} , E_{FL} , and so on, are biased with 7 μ A.

Fig. 9(B) shows the measured transient response of the proposed p-type LDO with and without the proposed techniques

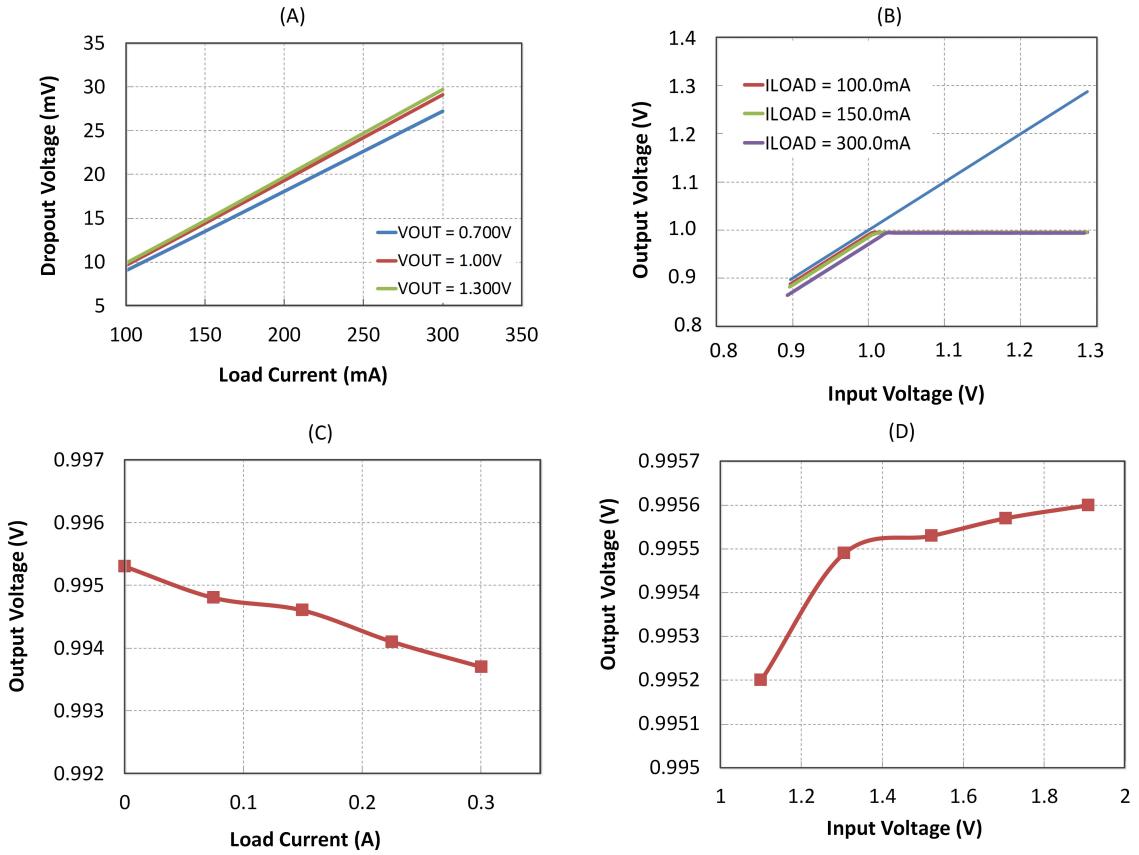


Fig. 12. (A) Measured dropout voltage at different conditions of V_{OUT} and I_{LOAD} . (B) Measured dropout voltage at $V_{OUT} = 1$ V and different I_{LOAD} conditions. (C) Measured load regulation at $V_{OUT} = 1$ V and I_{LOAD} from 0 to 300 mA. (D) Measured line regulation at $V_{OUT} = 1$ V, V_{IN} from 1.1 to 1.9 V at $I_{LOAD} = 30$ mA.

for the conditions of $V_{IN} = 3.2$ V, $V_{OUT} = 3$ V, $CL = 4.7 \mu F$, and I_{LOAD} rising slope of 30 mA/1 μs for a load current up to 600 mA. As shown in Fig. 9(B), input voltage of the LDO is from the buck converter and the undershoot/overshoot of the LDO with and without the proposed techniques offers 28/27 mV and 12/11 mV, respectively.

Fig. 9(C) demonstrates the above-mentioned ringing phenomena at the output of the n-type LDO that offers $V_{OUT} = 1$ V and I_{LOAD} steps from 0 to 300 mA with 30 mA/1 μs . As shown in Fig. 9(C), as the fourth loop is turned OFF, the LDO features ringing at the output node, which leads to big undershoot. Fig. 9(D) shows that the load transient in terms of undershoot for the same LDO for the case of a fast load current step is applied. The measured conditions are $V_{BAT} = 3.8$ V, $V_{IN} = 1.2$ V, $V_{OUT} = 1$ V, $CL = 1 \mu F$, and I_{LOAD} rising slope of 300 mA/1 μs . The measured undershoot shows 56 mV for the n-type LDO that consumes a total of 14 μA of the quiescent current.

Fig. 10 shows the measured load transient with slow and fast load steps for one of the n-type LDOs that supplies power to the memory application inside the AP as shown in Fig. 1. The load transient characteristic is very important for stable memory circuit operation; therefore, the quiescent current for this LDO is higher to obtain small undershoot/overshoot. The maximum load current is required to be up to 600 mA. As shown

in Fig. 10, the measured output undershoot/overshoot with I_{LOAD} rising/falling slope of 250 mA/1 μs are 26 and 15 mV, respectively. The measured conditions are $V_{BAT} = 3.8$ V, $V_{IN} = 0.8$ V, $V_{OUT} = 0.6$ V, and $CL = 2.2 \mu F$, and the LDO consumes a total of 32 μA quiescent current.

For a full verification of the proposed LDO with all measured results, the n-type LDO that output $V_{OUT} = 1$ V at maximum load current of 300 mA with load transient characteristic as shown in Fig. 9(C) and (D) will be presented. As shown in Fig. 5(A), the output voltage of the LDO can be programmable by controlling the value of the resistor R_2 . In this design, the value of R_2 is controlled by six digital bits, and the output voltage can be programmed from 0.7 to 1.3 V. Fig. 11(A) shows the measured V_{OUT} as function of the control words with 12.5 mV per one control step. Fig. 11(B) shows the measured output peak-to-peak ripple of the proposed LDO at steady-state operation conditions versus the control words for all output voltage from 0.7 to 1.3 V. The measurements are at different conditions of V_{IN} of 1.1/1.3/1.5/1.7 V and the load current of 30/150/300 mA. As shown in Fig. 11(B), the maximum output peak-to-peak ripple at steady-state operation is under 6.2 mV, which is much smaller than the pre-set offset voltage for the E_{FL} and I_{FL} loops to be operated. The measured results in Fig. 11(B) re-confirm that at steady-state operation, the E_{FL} and I_{FL} loops are designed to be always OFF since the pre-set offset voltages for these loops are more

TABLE I
SUMMARY OF THE PERFORMANCE OF THE PROPOSED N-TYPE LDO

Parameters	Test Conditions	Measurement	Unit
Input Voltage (VIN)	Operating voltage range is good under 2.0V.	1.05~2.0	V
Battery Voltage (VBAT)	VBAT is usually from 3.0 ~ 4.5V.	3.0~5.0	V
Output Voltage Range	Can be programmed by 6bits.	0.7~1.3	V
Output Voltage Accuracy	VBAT = 3.8V, VOUT = 1.0V, VIN = 1.1 ~ 1.7V, and I_{LOAD} = 30~300mA.	< 0.6	%
Output peak-to-peak ripple	VBAT = 3.8V, VOUT = 1.0V, VIN = 1.1 ~ 1.7V, and I_{LOAD} = 30 ~ 300mA.	< 6.3	mV
Dropout Voltage	VBAT = 3.8V, VOUT = 0.7 ~ 1.3V, and I_{LOAD} = 100 ~ 300mA.	< 29.7	mV
Quiescent Current	I_{LOAD} = 0, VBAT = 3.8V, VIN = 1.1V, and VOUT = 1.0V.	14	μ A
Maximum Load Current	VBAT = 3.8V and VIN = 1.03V.	300	mA
Output Load Transient Undershoot	I_{LOAD} = 0 to 300mA with 300mA/1 μ s.	56	mV
Output Load Transient Overshoot	I_{LOAD} = 300mA to 0 with 300mA/1 μ s.	24	mV
Output Line Transient	VIN from VOUT+0.3V to VOUT+0.8V to VOUT+0.3V; I_{LOAD} =300mA; Rising/Falling=5 μ s.	4	mV
Load Regulation	VBAT = 3.8V, VIN = 1.1V, I_{LOAD} = 0 to 300mA.	0.006	mV/mA
Line Regulation	VBAT = 3.8V, I_{LOAD} = 1mA; VIN = 1.1~2.0V.	0.44	mV/V
Power Supply Rejection (PSR)	I_{LOAD} = 300mA; Frequency = 1KHz VIN = 1.1V + 50mVpp; VBAT = 3.8V. Frequency = 10KHz Frequency = 100kHz	71 50 28	dB
Output Noise	Integrated from 10Hz to 100kHz at I_{LOAD} = 30mA, VBAT = 3.8V, VIN = 1.1V, VOUT = 1.0V. Without chopping technique With chopping technique	80 62	μ Vrms
Output Capacitance	Bigger Capacitor is better in term of undershoot/overshoot.	1.0	μ F

than 10 mV, which is much higher than output peak-to-peak voltage ripple.

Fig. 11(C) shows the measured output noise level of the proposed LDO with and without applying the chopping technique as reported in [9]. The measured integrated output noise from 10 Hz to 100 kHz at I_{LOAD} = 10% of maximum current shows 80 and 62 μ Vrms with and without chopping technique, respectively. Fig. 11(D) shows the measured output voltage accuracy for VOUT from 0.7 to 1.3 V, which is corresponding to the control words from 0 to 48. The measured output voltage accuracy is at conditions of VIN of 1.1/1.3/1.5/1.7 V and I_{LOAD} of 30/150/300 mA. As shown in Fig. 11(D), the maximum output voltage deviation from its nominal value is under 0.6% for full output voltage range from 0.7 to 1.3 V.

Fig. 12(A) shows the measured dropout voltages of the proposed LDO as a function of I_{LOAD} from 100 to 300 mA and VOUT of 0.7/1.0/1.3 V. As shown in Fig. 12(A), the maximum dropout voltage is under 30 mV at the maximum I_{LOAD} of 300 mA. Fig. 12(B) provides a more detail of dropout voltage measurement for the proposed LDO at VOUT = 1 V and different I_{LOAD} values. Fig. 12(C) and (D) shows the measured load and line regulations of the proposed LDO, respectively. Finally, Fig. 13 shows the measured PSR of

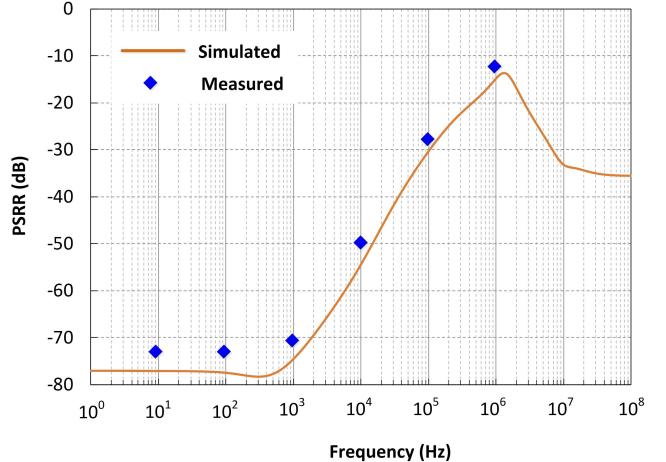


Fig. 13. Measured PSR of the n-type LDO at I_{LOAD} = 300 mA and VOUT = 1 V.

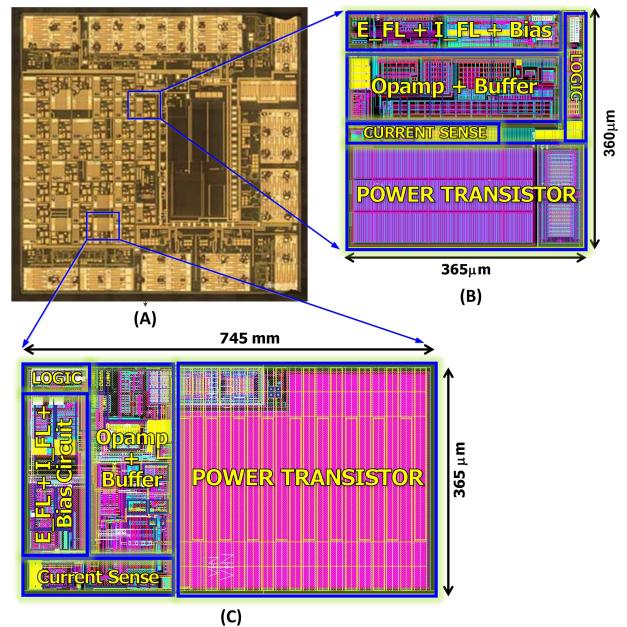


Fig. 14. (A) Microphotograph of the PMIC with the chip size of 5.25×5.25 mm 2 . (B) Layout photograph of the LDO that features 150 mA of maximum load current. (C) Layout photograph of the LDO that features 600 mA of maximum load current.

the proposed LDO in comparison with simulated results. The summary of the performance of the proposed n-type LDO is given in Table I.

Fig. 14 shows the micro-photographs of the fabricated chip and layout. The package chip includes 169 balls with a size of 6.25×6.25 mm 2 . The layout size is 5.25×5.25 mm 2 . Fig. 14(B) and (C) shows the layout sizes for two LDOs, which can support maximum load currents of 150 and 600 mA, respectively. As shown in Fig. 14(B) and (C), the layout sizes for LDOs with 150 and 600 mA of the maximum load currents are 365×365 μ m 2 and 365×745 μ m 2 , respectively.

In order to provide a clearer picture of the performance improvement of the proposed LDO with the state-of-the-art designs, a comparison with some of the prior reported LDOs is given in Table II. A figure of merit (FOM) from [15] is

TABLE II
COMPARISON OF THE PROPOSED LDO WITH STATE-OF-THE-ART DESIGNS

References	[15]	[16]	[17]	[18]	[19]	[5]	This works
Year	JSSC 2007	TCASII 2008	TPE 2010	JSSC 2010	TPE 2016	TPE 2017	2017
Technology (μm)	0.35	0.35	0.35	0.09	0.18	0.18	0.13
Chip area (mm^2)	0.264	0.409	0.146	0.00274	0.024	0.0285	0.1825
Input voltage range V_{in} (V)	2.0-5.5	2.0	2.0-4.5	1.0-1.2	1.2-1.8	1.4-1.8	1.05-2.0
Typical Output Voltage V_0 (V)	1.8	1.8	1.8	0.9	1.0	1.2	1.0
Dropout voltage (mV)	200	200	200	100	200	200	29.7
Max. Load current (mA)	200	150	200	50	100	50	300
Quiescent Current I_0 (μA)	20-340	27	30-75	9.3	135.1	1.6-200	14-120
Max. Current Efficiency (%)	99.8	99.9	99.9	99.9	99.86	99.6	99.96
Load Regulation (mV/mA)	0.17	0.11	0.09	0.082	0.075	0.1	0.006
Line Regulation (mV/V)	2	1.38	6	14	22.7	5.5	0.44
Output Capacitor C_0 (μF)	1	1	1	1	1	1	1
Load Transient Undershoot (mV)	20	65	30	6	25	24	56
Load Transient Overshoot (mV)	34	70	65	12.1	7.5	5	24
Max. Load Current Step (mA)	200	100	160	50	100	50	300
PSR (dB) (at frequency)	<-45 (20kHz)	<-40 (kHz)	N/A	<-54 (100kHz)	<-35 (100kHz)	<-30 (10MHz)	-50 (10kHz)
Output Integrated Noise (μVRms)	N/A	N/A	N/A	N/A	N/A	N/A	80 (10Hz-100kHz)
FOM (ps)	27	364.5	111.3	67.3	439	18.5	12.44

adopted to compare the transient response of different LDOs, which is given as

$$\text{FOM} = \frac{\text{CL} \times \Delta V_{\text{out}} \times I_q}{I_{\text{LOAD},\text{max}}^2} \quad (10)$$

where CL , ΔV_{out} , I_q , and $I_{\text{LOAD},\text{max}}^2$ are the output capacitor, the peak-to-peak output transient due to undershoot and overshoot, the quiescent current, and the maximum load current, respectively. The smaller the FOM, the better the transient response the LDO achieves [15]. For a fair comparison, the prior LDOs for portable applications with similar output capacitor of $1 \mu\text{F}$ are utilized. Note that the capless LDOs as reported in [6]-[8], [10], and [13] are not suitable for our comparison, because our proposed LDOs use big output capacitors. As shown in Table II, the proposed LDO in this paper obtain the smallest FOM factor.

VI. CONCLUSION

A new multiple-loop design technique for high performance LDO designs is presented. The proposed technique offers designers with a good tradeoff in LDO design with a low bias current while obtaining excellent performances in terms

of undershoot, overshoot, and so on. The proposed LDO topology as well as the detailed schematics have been presented. A total of one BGR and 38 LDOs (including NLDO and PLDO) were integrated in one power-management IC chip for powering an AP inside mobile devices. The design has been verified based on $0.13-\mu\text{m}$ CMOS technology and requires $14 \mu\text{A}$ of bias current. The proposed LDO features under $56/24$ mV of undershoot/overshoot at $V_{\text{OUT}} = 1 \text{ V}$ as the I_{LOAD} steps up from 0 to 300 mA with 300 mA/ $1 \mu\text{s}$ on a $1-\mu\text{F}$ output capacitor. The measured output load/line regulations are $1.8/0.4$ mV, respectively. The measured integrated output noise from 10 Hz to 100 kHz at $I_{\text{LOAD}} = 10\%$ of maximum current shows $80 \mu\text{VRms}$. The package chip size is $6.25 \times 6.25 \text{ mm}^2$ with 169 balls.

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Quoc-Hoang Duong was born in Bac Ninh, Vietnam. He received the B.S. degree from the Hanoi University of Technology, Hanoi, Vietnam, in 2001, and the M.S. and Ph.D. degrees from the Korean Advanced Institute of Science and Technology, Daejeon, South Korea, in 2004 and 2007, respectively.

From 2002 to 2006, he was engaged in silicon technology-based analog/RF circuit designs, such as bias references, variable gain amplifier, automatic gain control, trans-impedance amplifier, low-pass filter, and baseband transceivers. From 2007 to 2013, he was with Siliconworks/HTCKorea, Daejeon, and the Electronics and Telecommunications Research Institute, Daejeon, where he was involved in analog/RF and power management integrated circuit (PMIC) designs for automotive and liquid crystal display (LCD) applications. In 2013, he joined Samsung Electronics, Hwaseong, South Korea, where he is currently a Principal Engineer, designing analog and PMIC for portable mobile applications.



Huy-Hieu Nguyen was born in Vietnam in 1980. He received the B.S. degree from the Hanoi University of Technology, Hanoi, Vietnam, and the Ph.D. degree in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2003 and 2010, respectively.

From 2010 to 2012, he was with Siliconworks, Daejeon, where he was involved in CMOS analog and power management integrated circuit design for LCD applications. Since 2013, he has been with Samsung Electronics, Hwaseong, South Korea, as a Senior Design Engineer, where he has been involved in power management integrated circuit design for portable mobile applications.



Jeong-Woon Kong received the B.S. degree in electric wave engineering from Kwangwoon University, Seoul, South Korea, in 2010, and the M.S. degree in electronic engineering from Sogang University, Seoul, in 2012.

In 2012, he joined Samsung Electronics, Hwaseong, South Korea, where he is engaged in power management integrated circuit designs. His current research interests include analog and mixed signal circuits for mobile applications.



Hyun-Seok Shin was born in Seoul, South Korea. He received the B.S. degree from Konkuk University, Seoul, in 2010.

In 2010, he joined Samsung Electronics, Hwaseong, South Korea, where he is involved in designing analog and power management integrated circuits for portable mobile applications.



Yu-Seok Ko was born in Seoul, South Korea. He received the M.S. and Ph.D. degrees from the Department of Electrical and Computer Engineering, University of Florida, Gainesville, FL, USA, in 2000 and 2005, respectively.

In 2006, he joined Samsung Electronics, Hwaseong, South Korea, where he is currently a Principal Engineer with the Power Development Team. From 2006 to 2008, he was involved in RF integrated circuit (IC) design and RF related product developments. Since 2009, he has been focused on designing power management IC (PMIC) and PMIC related product development for mobile applications.



Hwa-Yeol Yu received the B.S. and M.S. degrees in electronics engineering from Inha University, Seoul, South Korea, in 1999 and 2001, respectively.

In 2001, he joined Samsung Electronics, Hwaseong, South Korea, where he is currently a Principal Engineer. From 2001 to 2010, he participated in the design of sigma-delta FN synthesizer, and VCO and DCXO for RF transceivers for CDMA and GSM/GPRS mobile phones. Since 2011, he has been designing power management integrated circuits for mobile phones.



Yong-Hee Lee received the M.S. degree in electronics engineering from Sungkyunkwan University, Seoul, South Korea.

Since 1993, he has been engaged in the design of the mixed signal circuits with Samsung Electronics, Suwon, Korea. He has a variety of experience as a designer of audio converters. His technical interests include delta-sigma converters, and digital filter architecture with low power consumption and power management systems.



Chun-Hyeon Bea received the B.S. degree from Kyungpook National University, Daegu, South Korea, in 2004, and the M.S. and Ph.D. degrees from the Pohang University of Science and Technology, Pohang, South Korea, in 2007 and 2012, respectively, all in electronic and electrical engineering.

In 2012, he joined Samsung Electronics, Hwaseong, South Korea, as a Senior Engineer. He is currently with the Power Device Development Team, Device Solution Department, Samsung

Electronics, as a Circuit Designer of power management integrated circuits for mobile applications, and leads the design of low-dropout regulators and bandgap reference circuits. His current research interests include power and signal integrity.



Ho-Jin Park received the B.S. degree in electrical engineering from Hanyang University, Seoul, South Korea, in 1986.

Since 1989, he has been with Samsung Electronics, Hwaseong, South Korea, where he is currently a Vice President in charge of the Mixed Signal Core Design Team. He was engaged in the research and development of analog and mixed circuits for digital TV and mobile devices. Since 2016, he has been with the Power Device Development Team, Samsung Electronics. His current research interests include high-speed data converters, high-resolution sigma-delta modulators, ultra-low power analog circuits, low-jitter phase-locked loops (PLLs), all-digital PLLs, power management circuits, sensors, and analog baseband/RF front-end circuits for wireless communications.