A Voltage Multiplier With Adaptive Threshold Voltage Compensation

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***Abstract*— A voltage multiplier (VM) with adaptive threshold voltage compensation is presented to enhance the power conversion efficiency (PCE). It is fabricated in a 0.18-μm CMOS process. With the input frequency of 402 MHz and a load resistor of 30 kΩ, this VM achieves the PCE of 31.9% with the input power of −1 dBm, and the PCE is maintained above 20% with 10-dB input range from −11 to −1 dBm.**

***Index Terms*— Adaptive threshold voltage compensation, voltage multiplier (VM).**

I. Introduction

The RF-powered applications are receiving significant attention, such as implantable medical devices, wearable devices, and wireless sensors. To convert the RF power into a dc voltage, the voltage multiplier (VM) [1] using the diode-connected MOS transistors are widely adopted. However, the threshold voltage ($V_{\rm TH}$) of a transistor causes a large forward voltage drop. It reduces the output voltage and decreases the power conversion efficiency (PCE) of the VM. To compensate the $V_{\rm TH}$, a mirror-like $V_{\rm TH}$ canceller is used to generate the compensation voltages to the transistors in [2]. However, while the output voltage of the VM is increased, the compensation voltages will be also increased. It increases the reverse leakage current of the transistors and degrades the PCE of the VM.

The multi-stage VM with the $V_{\rm TH}$ self-compensation is presented in [3] and [4]. In [3], the gate terminal of the transistor M_k is connected to the voltage, V_{k+1}, of an adjacent stage, where $k = 1$–3, as shown in Fig. 1(a). However, if the amplitude of $\rm RF_{IN}$ is small, the V_{k+1} may not properly compensate the $V_{\rm TH}$ of M_k. It increases the forward voltage drop across the transistor and degrades the PCE. If the amplitude of $\rm RF_{IN}$ is large, the $V_{\rm k+1}$ may be higher than the $V_{\rm TH}$ of M_k. It increases the reverse leakage current and also degrades the PCE. Fig. 1(b) shows a $V_{\rm TH}$ self-compensation VM with the tunable compensation order [5]. One of the voltages, V_{2k}, V_{2k-2}, and V_{2k+2}, will be connected to the gate of M_{2k+1}, where $k = 1$–N. It increases the output voltage $V_{\rm REC}$; however, one of two transistors for each stage is not compensated. In [6], the floating gate transistors are used to store the compensation voltages in a VM. Nevertheless, this method needs the high-voltage pulses to pre-charge the floating gate devices. Fig. 1(c) shows a VM with the voltage distributors (VDs) [7]. To compensate the $V_{\rm TH}$, a pulse generator and a dc voltage source V_C are required to bias the drain-to-gate voltage of M_1 and M_2. In [6] and [7], the compensation voltage V_C is fixed, but the $V_{\rm TH}$ of the transistors may be altered due to the body effect. While $V_{\rm TH} > V_C$, a forward voltage drop of the transistor is increased and the output voltage $V_{\rm REC}$ is decreased. When $V_{\rm TH} < V_C$, the reverse leakage current of the transistor is enlarged to reduce $V_{\rm REC}$. Both the forward voltage drop and the reverse leakage current degrade the PCE of the VM.

In this paper, a VM with adaptive $V_{\rm TH}$ compensation is presented. The compensation voltage V_C is adjusted in the background to compensate the $V_{\rm TH}$ of the transistors. It not only increases the output voltage, but also enhances the PCE of the VM. In addition, the high-PCE range is also extended. This paper is organized as follows. The circuit description is given in Section II. Section III shows the experimental results. Finally, the conclusions are given in Section IV.

II. Circuit Description

Fig. 2(a) shows the proposed VM. It consists of a three-stage VM with an individual body bias [8], six VDs [7], a load capacitor C_L, a load resistor R_L, a toggle switch, and an adaptive threshold voltage canceller (ATVC). The transistors in the VM core use the individual body biasing to reduce the $V_{\rm TH}$ variation among the different stages in the chain [4], [8]. The VM receives an ac signal $\rm RF_{IN}$, and outputs a dc voltage $V_{\rm REC}$ to supply the ATVC, the toggle switch, and R_L. The ATVC is mostly realized by digital circuits. A passive toggle switch generates Ena to enable and disable the ATVC, respectively. When Ena is low, the ATVC is disabled. While $V_{\rm REC} \geq 0.38$ V, the ATVC will be enabled as Ena becomes high. The ATVC monitors $V_{\rm REC}$ and outputs a compensation voltage V_C and two pulse signals, Φ_{1+} and Φ_{2+}. Then, the VDs transfer the V_C to the VM.

The ATVC is composed of an oscillator (Osc.), a timing controller, four clock boosting circuits, two sample-and-hold circuits SAH1 and SAH2, a latch comparator (CMP), a D-flip-flop (DFF1), a controller, and a digital-to-analog converter (DAC). A relaxation oscillator generates a clock CLK for a timing controller. The timing controller realizes six pulses, $\Phi_1 \sim \Phi_2$ and P_1–P_4. Φ_1 and Φ_2 drive the clock boosting circuits to control the VDs. P_1 and P_3 drive the clock boosting circuits to control SAH1 and SAH2. Then, SAH1 and SAH2 sample $V_{\rm REC}$ to be $V_{\rm S1}$ and $V_{\rm S2}$, respectively. By comparing $V_{\rm S1}$ and $V_{\rm S2}$, the CMP generates an output

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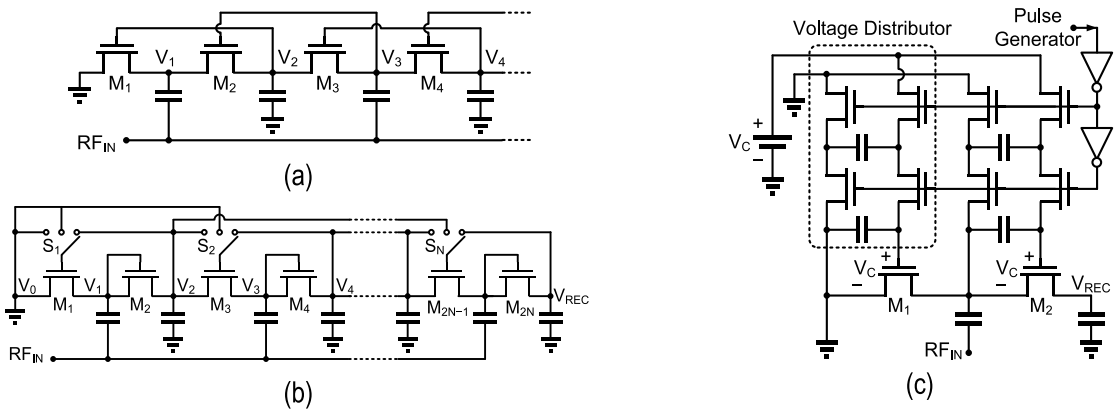

Fig. 1. VM with (a) threshold self-compensation [3], (b) tunable compensation order [5], and (c) VDs [7].

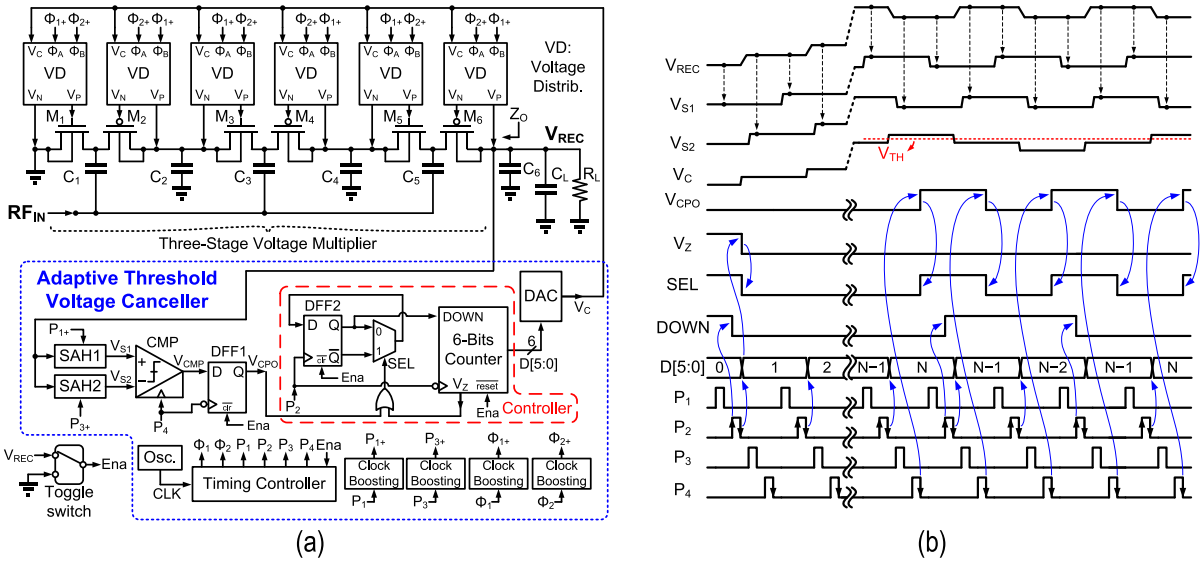

Fig. 2. (a) Proposed VM with an ATVC and (b) its timing diagram.

voltage V_{CMP}. To deglitch V_{CMP}, DFF1 is used to re-sample V_{CMP} by P_4 where the output V_{CPO} is sent to the controller. The controller is composed of a D-flip-flop (DFF2), a multiplexer, an OR gate, and a 6-bits counter. While the signal DOWN is low, the output code D[5:0] of the counter is increased. When DOWN is high, the code D[5:0] is decreased. While the 6-bits counter is underflow, i.e., D[5:0] = [00…0], V_Z goes high. According to D[5:0], a DAC generates the compensation voltage V_C to the VDs.

The timing diagram of the proposed VM is shown in Fig. 2(b). Initially, V_Z, SEL, and DOWN are high, V_{CPO} is low, D[5:0] = 0, and V_C is zero. As P_1 is active, SAH1 samples V_{REC} and holds it as V_{S1}. As P_2 goes high, DOWN becomes low. While P_2 goes low, D[5:0] is increased by one LSB and both V_Z and SEL become low. When $V_C < V_{TH}$ and V_C is increased, V_{REC} will be increased. As P_3 is active, SAH2 samples V_{REC} and holds it as V_{S2}. Since $V_{S2} > V_{S1}$, V_{CPO} is kept low when P_4 goes low. While both SEL and DOWN are low, the above procedure is repeated and D[5:0] is increasing until D[5:0] = N. Assume that if D[5:0] = N, $V_C > V_{TH}$. The corresponding V_{REC} is reduced owing to

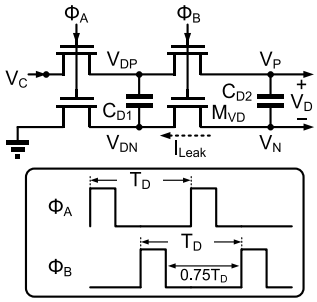

Fig. 3. VD.

the reverse leakage current. As P_3 is active, V_{S2} is lower than V_{S1}. When P_4 goes low, both V_{CPO} and SEL go high. As the next P_2 becomes high, DOWN goes high. While P_2 becomes low, D[5:0] is decreased by one LSB; i.e., D[5:0] = N − 1. Then, V_C is decreased and V_{REC} will be increased again. Since DOWN is high, D[5:0] is decreased by one LSB; i.e., D[5:0] = N − 2. In the above procedure, the CMP will compare V_{S1} and V_{S2} to update V_{CPO},

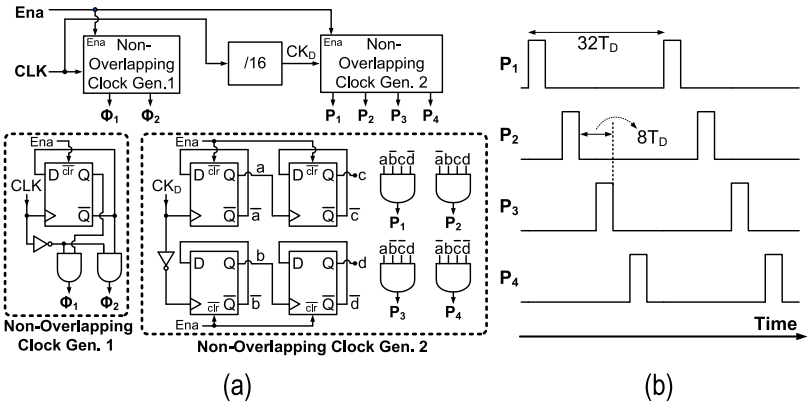

Fig. 4. (a) Timing controller and (b) timing diagram of P_1–P_4.

SEL, and DOWN. In the steady state, D[5:0] switches among N − 1, N, N − 1, and N − 2. Finally, the whole process will be repeated. This ATVC keeps V_{REC} as high as possible in background.

A. Voltage Distributor

Fig. 3 shows a VD [7]. It consists of four nMOS transistors, and two capacitors C_{D1} and C_{D2}. While Φ_{A} is high, $V_{\mathrm{DN}} = 0$ and $V_{\mathrm{DP}} = V_C$. The charge $\mathrm{Q_1}$ on C_{D1} is given as $C_{D1} \cdot V_C$. When Φ_{B} goes high and the charges on C_{D1} and C_{D2} is re-distributed. Assuming $V_P - V_N = V_D$. After the k-times charge re-distribution, the voltage $V_{D,k}$ is given as

$$V_{D,k} = C_{D1} \cdot V_C \cdot \sum_{i=1}^{k} \frac{C_{D2}^{i-1}}{(C_{D1} + C_{D2})^i}. \tag{1}$$

In (1), assuming $k = 8$, $V_C = 0.4$ V, and $|V_C - V_{D,8}|/V_C \leq 0.1\%$, $C_{D1} = 2 \cdot C_{D2}$ is chosen. In Fig. 2(a), the capacitors $C_{2\mathrm{n}-1}$, where $n = 1$–3, and the parasitic capacitors $C_{\mathrm{gs,m}}$ of the transistor M_{m}, where $m = 1$–6, may couple $\mathrm{RF_{IN}}$ into C_{D2} to cause the ripple V_{ripple}. For example, assuming $n = 3$, $m = 6$, $C_5 >> C_{\mathrm{gs,6}}$, and $C_L >> C_{D2}$, $\mathrm{V_{ripple}}$ is approximated as

$$V_{\mathrm{ripple}} = RF_{\mathrm{IN}} \cdot [C_{\mathrm{gs,6}}/(C_{\mathrm{gs,6}} + C_{D2})]. \tag{2}$$

For $V_{\mathrm{ripple}}/\mathrm{RF_{IN}} \leq 1\%$ and $\mathrm{C_{gs,6}} = 15.1$ fF, C_{D2} is chosen as 2.87 pF. The voltage $\Delta V_{D,k}$ is defined as the difference between V_C and $V_{D,k}$ and it is derived as

$$\Delta V_{D,k} = V_C \left[1 - C_{D1} \cdot \sum_{i=1}^{k} \frac{C_{D2}^{i-1}}{(C_{D1} + C_{D2})^i} \right] + \frac{0.75 \cdot T_D \cdot I_{\mathrm{Leak}}}{C_{D2}} \tag{3}$$

where T_D is the period of Φ_A and Φ_B. It is affected by both the re-distribution index k and the leakage current I_{Leak}. While a transistor M_{VD} is turned off and a voltage across M_{VD} is 0.4 V, the simulated leakage current I_{Leak} is 48.6 pA. For a specified $\Delta V_{D,k}$, T_D should be as long as possible to reduce the power consumption. For example, when $V_C = 0.4$ V, $\Delta V_{D,k} \leq 1$ mV, and $k = 8$, T_D should be less than 77.8 μs. In this paper, $T_D = 71.4\mu$s is chosen, and the corresponding frequency of Φ_A and Φ_B is 14 kHz.

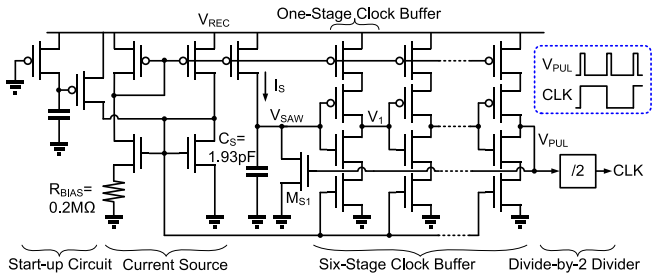

Fig. 5. Relaxation oscillator.

B. Timing Controller and Oscillator

A timing controller is shown in Fig. 4(a). While Ena is high, the timing controller is enabled. The first non-overlapping clock generator with a divide-by-2 divider is used to generate Φ_1 and Φ_2. Since $k = 8$ for the VDs is chosen, the falling edges between P_2 and P_3 should be $8\mathrm{T_D}$, as shown in Fig. 4(b). To realize P_1–P_4, the CLK is divided by 64 by using a divide-by-16 divider and the second non-overlapping clock generator with a divide-by-4 divider.

A relaxation oscillator is shown in Fig. 5. It is mainly composed of a start-up circuit, a current source, a six-stage clock buffer, and a divide-by-2 divider. The voltage $\mathrm{V_{SAW}}$ on a capacitor C_S is charged by a current I_S. While $V_{\mathrm{SAW}} > 0.5V_{\mathrm{REC}}$, V_1 is switched from high to low. After the delay time of the six-stage clock buffer, which is equal to $6\tau_{\mathrm{D}}$, V_{PUL} becomes high. Then, M_{S1} is turned on to quickly discharge C_S, and V_{SAW} becomes zero. After $6\tau_{\mathrm{D}}$, V_{PUL} is switched from high to low. M_{S1} is turned off and $\mathrm{C_S}$ will be charged again. The pulse V_{PUL} is divided by 2 to realize a clock CLK, which frequency f_{CLK} is given as

$$f_{\mathrm{CLK}} \approx 0.5/[(0.5V_{\mathrm{REC}} \cdot C_S)/I_S + 12\tau_D]. \tag{4}$$

The I_S and C_S are chosen as 205 nA and 1.93 pF, respectively, to realize f_{CLK} of 28 kHz, when $V_{\mathrm{REC}} = 1.8$ V.

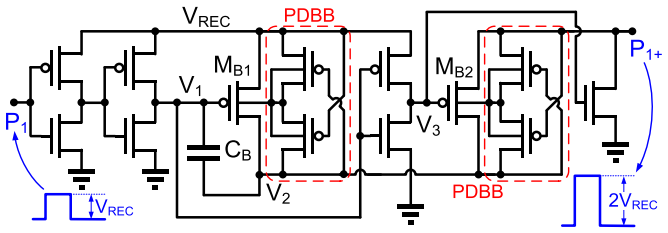

Fig. 6. Clock boosting circuit.

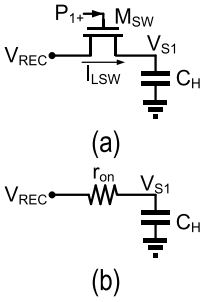

Fig. 7. (a) Sample-and-hold circuit and (b) its equivalent model while M_{SW} is turned on.

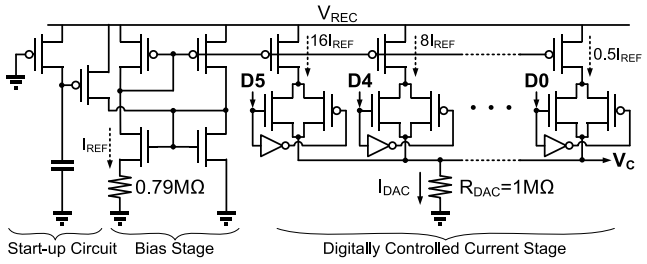

Fig. 8. DAC.

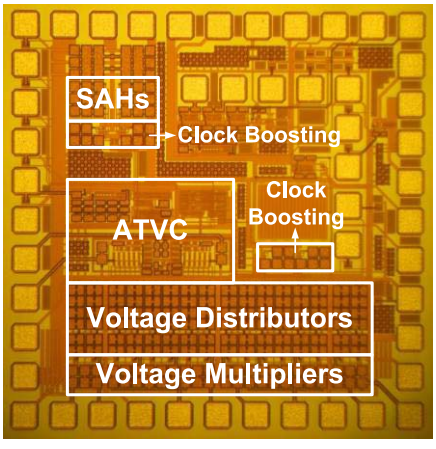

Fig. 9. Photograph of chip.

C. Clock Boosting Circuit and a Sample-and-Hold Circuit

To driving the SAHs and the VDs, clock boosting circuits are adopted to increase the amplitudes of the pulses P_{1+},P_{3+},Φ_{1+}, and Φ_{2+}. A clock boosting circuit is shown in Fig. 6. While P_1 goes low, V_1 will become low and M_{B1} will be turned on. Then, V_3 goes high and M_{B2} will be turned off. The capacitor C_B is charged and V_2 becomes to V_{REC}. When P_1 goes high, V_1 will become V_{REC} and M_{B1} will be turned off. Meanwhile, V_2 is boosted to $2V_{REC}$. Finally, V_3 goes low and M_{B2} will be turned on to output P_{1+} with amplitude of $2V_{REC}$. To avoid the body leakage current, two p-type dynamic body bias (PDBB) circuits [9] are used to bias the body voltages for M_{B1} and M_{B2}.

A sample-and-hold circuit is shown in Fig. 7(a). It is composed of a switch M_{SW} and a capacitor C_H. While M_{SW} is off and the voltage across M_{SW} is 0.5 V, the simulated leakage current I_{LSW} is 27 pA. The leakage current induces a voltage error on V_{S1}. To keep this voltage error less than 10 mV, a C_H of 8.56 pF is chosen. When P_{1+} goes high, M_{SW} will be turned on. The equivalent model is shown in Fig. 7(b), where r_{on} is an on-resistance of M_{SW}. Assuming $V_{REC} = 0.5$ V, $V_{S1} = 0$ V, and $P_{1+} = 1$ V, the simulated r_{on} is 2.99 kΩ. Since r_{on} and C_H operate as a lowpass filter to suppress the voltage ripple of V_{S1}, this ripple is attenuated by

$$20 \cdot \log[1/(\omega \cdot C_H \cdot r_{on} + 1)]. \quad (5)$$

When the frequency of the ripple is 402 MHz, the calculated attenuation is −36.3 dB.

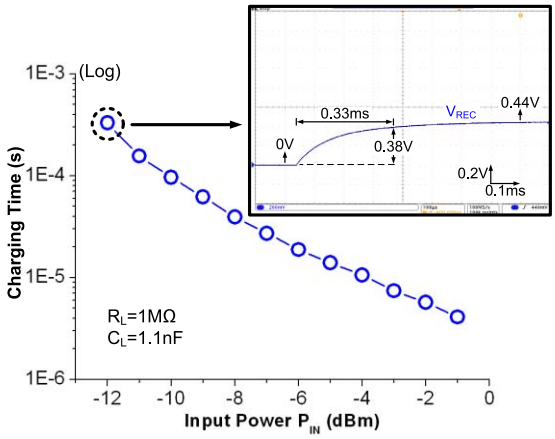

Fig. 10. Measured charging time versus input power while an ATVC is disabled.

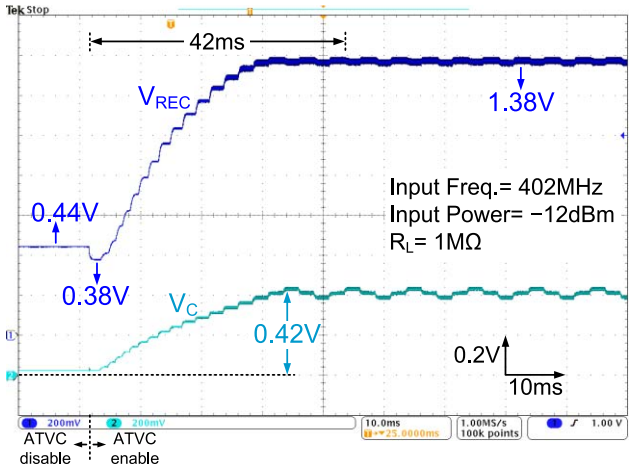

Fig. 11. Measured output voltage V_{REC} and compensation voltage V_C.

TABLE I
SIMULATED PCES OF THE PROPOSED VM AND A DICKSON VM [1] FOR DIFFERENT CORNERS AND TEMPERATURES

Corner		TT @ 27°C	FF @ 0°C	SS @ 80°C	FS @ 80°C	SF @ 80°C
PCE	Proposed VM	38.9% @ V_C=0.42V	41.3% @ V_C=0.38V	35.2% @ V_C=0.43V	32.9% @ V_C=0.37V	31.8% @ V_C=0.35V
	Dickson VM [1]	0.15% @ V_C=0V	0.33% @ V_C=0V	0.19% @ V_C=0V	0.57% @ V_C=0V	0.92% @ V_C=0V

*Input amplitude is 0.3V, Input frequency is 402MHz, R_L=30kΩ.

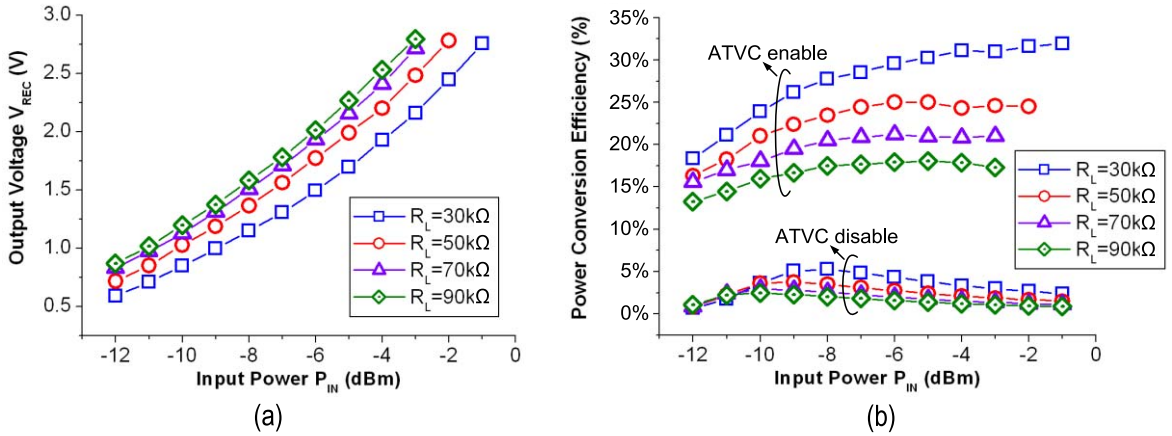

Fig. 12. (a) Measured output voltage V_{REC} and (b) measured PCE versus the input power of $\mathrm{RF_{IN}}$.

D. Digital-to-Analog Converter

A DAC is shown in Fig. 8. It is mainly composed of a start-up circuit, a bias stage, a digitally controlled current stage, and a resistor R_{DAC}. The bias stage generates a reference current I_{REF}. The output voltage V_C is determined by a digitally controlled current I_{DAC} and a resistor R_{DAC}. To cover the threshold voltages of the transistors in the VM, while V_C ranges from 0 to 0.8 V, the required code of a DAC is calculated from

$$V_{\mathrm{CR}}/(0.5I_{\mathrm{REF}} \cdot R_{\mathrm{DAC}}) \tag{6}$$

where V_{CR} is the range of V_C, and $0.5I_{\mathrm{REF}} \cdot R_{\mathrm{DAC}}$ is an output voltage step of a DAC. While 0.5 $I_{\mathrm{REF}} = 24$ nA and $R_{\mathrm{DAC}} = 1$ MΩ, the required code is calculated as 34. Hence, the required bits of the DAC are six.

E. Settling Times of the VM and ATVC

To consider C_L and R_L, the required setting time of a VM is analyzed. For a start, assuming Z_{O} in Fig. 2(a) is an output impedance of the VM, and it is approximated as

$$Z_O \approx r_{\mathrm{on},M6} + [1/(j\omega \cdot C_5)] \tag{7}$$

where $r_{\mathrm{on,M6}}$ is the on-resistor of the transistor M_6. Since the capacitor C_5 is 1.9 pF with an angular frequency $\omega = 2 \cdot \pi \cdot 402$ Mrad/s, an impedance of C_5 is much smaller than $r_{\mathrm{on,M6}}$. Z_{O} is dominant by $r_{\mathrm{on,M6}}$. Then, while V_C is altered, the transient response of V_{REC} is modeled as a first-order RC circuit. As the percentage of the voltage error of a step response is less than 1%, the settling time $t_{S,VM}$ is given as

$$t_{S,\mathrm{VM}} \geq 4.7 \cdot (r_{\mathrm{on},M6}//R_L) \cdot (C_6//C_L). \tag{8}$$

Assuming $r_{\mathrm{on,M6}} = 46.2$ kΩ, $R_L = 1$ MΩ, $C_6 = 3.8$ pF, and $C_L = 1.1$ nF, $t_{S,VM}$ should be 0.23 ms at least. In this paper, an operation frequency of a DAC $f_{\mathrm{DAC}} = 438$ Hz is chosen and its corresponding $t_{S,\mathrm{VM}} = 2.28$ ms, which satisfies the required $t_{S,\mathrm{VM}}$. It makes sure that the VM with an ATVC will be stable. For the ATVC, an output voltage step of the DAC is designed as $0.5I_{\mathrm{REF}} \cdot R_{\mathrm{DAC}}$. While V_C is altered form 0 V to V_{TH}, the operation times of the DAC is calculated as $V_{\mathrm{TH}}/(0.5I_{\mathrm{REF}} \cdot R_{\mathrm{DAC}})$. The required setting time of the ATVC is estimated as

$$t_{S,\mathrm{ATVC}} \approx \left(\frac{V_{\mathrm{TH}}}{0.5I_{\mathrm{REF}} \cdot R_{\mathrm{DAC}}} + 4\right) \cdot \frac{1}{f_{\mathrm{DAC}}}. \tag{9}$$

Since D[5:0] switches among N − 1, N, N − 1, and N − 2, the additional factor of 4 is added to the second term in (9). Assume $V_{\mathrm{TH}} = 0.42$ V, $I_{\mathrm{REF}} = 48$ nA, $R_{\mathrm{DAC}} = 1$ MΩ, and $f_{\mathrm{DAC}} = 438$ Hz, $t_{S,\mathrm{ATVC}}$ is calculated as 49.1 ms.

III. EXPERIMENTAL RESULTS

A VM with the ATVC is fabricated in a 0.18-μm CMOS process. Assuming the input amplitude is 0.3 V, input frequency is 402 MHz, and R_L is 30 kΩ, the simulated PCEs of the proposed VM and a Dickson VM [1] for different process corners and temperatures are listed in Table I. Both are the three-stage VMs with the same transistor model and capacitance per stage. The PCEs of the proposed VM are improved by 34 times at least, compared with the Dickson VM.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

Reference	[4]	[5]	[6]	[7]	[8]	[10]#	[11]	[12]	**This Work**
Technology	90nm	65nm	0.25μm	0.3μm	0.13μm	65nm	0.25μm	0.18μm	**0.18μm**
Frequency (MHz)	915	904.5	906	950	915	900	450	915	**402**
Transistor type in a VM core	NMOS	NMOS	PMOS	NMOS	NMOS and PMOS	Low V_{TH} NMOS and PMOS	Low V_{TH} PMOS	Native NMOS	**NMOS and PMOS**
Special Requirements	No	Control loop	Pre-charge pulses	Battery needed	No	Control loop	No	No	**Control loop**
Loading	500kΩ	500kΩ	330kΩ	Battery loading	1MΩ	147kΩ	1MΩ	21.6kΩ	**30 kΩ**
Peak Output Power	8.32μW @-5dBm	2.1μW@ -14dBm	128μW @1.5dBm	N/A	11.7μW @-4dBm	53.3μW @-3dBm	6.9μW @-12dBm	1.09mW @4dBm	**253.4μW @-1dBm**
Peak PCE	16.1% @ -15.83dBm	5.3% @ -14dBm	30% @ -8dBm	11% @ -6dBm	22.6% @ -16.8dBm	35% @ -9.5dBm	10.9% @ -12dBm	32.5% @ 0dBm	**31.9%@ -1dBm**
Input Power Range (PCE>20%)	0dB*	0dB*	8dB	0dB*	2dB	11dB	0dB*	6dB	**10dB**
Sensitivity	-18.83dBm@ R_L=1MΩ, V_{REC}=1.2V	-20dBm	-19dBm@ R_L=1.32MΩ, V_{REC}=1V	-16dBm, V_{REC}= 1.22V	-21.7dBm@ R_L=1MΩ, V_{REC}=1V	-17.7dBm @ R_L=∞, V_{REC}=1V	-19.6dBm, V_{REC}=1V	-10dBm@ R_L=1MΩ, V_{REC}= 1.3V	**-12dBm@ R_L=1MΩ, V_{REC}= 1.38V**

* PCE<20%, # Differential structure.

For the proposed VM, the maximum PCE variation for several process corners and temperatures is around 9.5%. However, the threshold voltages of nMOS and pOMS transistors are different for different process corners and temperatures. A single V_C used to compensate the threshold voltages may degrade the PCE. Fig. 9 shows the die photograph and its chip area is 1.44 mm^2. To measure the lowest input power of the VM, R_L of 1 MΩ is chosen according to [4], [8], and [12]. Since an ATVC only works when $V_{\rm REC} \geq 0.38$ V, Fig. 10 shows the measured charging time of $V_{\rm REC}$ from 0 to 0.38 V while an ATVC is disabled and an input frequency is 402 MHz. As $P_{\rm IN} = -12$ dBm, the charging time is 0.33 ms. The measured transient responses of $V_{\rm REC}$ and the compensation voltage V_C are shown in Fig. 11. When the ATVC is disabled, $V_{\rm REC}$ is 0.44 V. While the ATVC is enabled, $V_{\rm REC}$ drops to 0.38 V. Then, V_C is increased and $V_{\rm REC}$ will be increased. As V_C is close to 0.42 V, $V_{\rm REC}$ is kept as high as possible, which is 1.38 V. The corresponding PCE is around 3%. The measured settling time is 42 ms, which is shorter than a theoretical value of 49.1 ms. This is because the oscillator has a higher output frequency while $V_{\rm REC}$ is below 1.8 V. Hence, $f_{\rm DAC}$ in (9) is increased and $t_{S,\rm ATVC}$ is decreased. Fig. 12(a) shows a measured $V_{\rm REC}$ versus $P_{\rm IN}$ at the different R_L. While $P_{\rm IN} = -3$ dBm, a peak $V_{\rm REC}$ is 2.8 V with R_L of 90 kΩ. Fig. 12(b) shows measured PCE versus $P_{\rm IN}$ for different R_L, where the power loss of the passive toggle switch and the power consumption of an ATVC are included. For $R_L = 30$ kΩ and $P_{\rm IN} = -8$ dBm, the measured PCEs are 5.3% and 27.8% while ATVC are disabled and enabled, respectively. When the ATVC is enabled, the PCE is increased by a percentage of 22.5. Assuming the power consumption of the ATVC is a constant, a lower R_L induces the higher output power, which may increase PCE. The PCE is dependent on the load resistance.

IV. CONCLUSION

In this paper, the proposed VM with the ATVC is presented. Its performance summary and comparison are listed in Table II. The threshold voltages of the nMOS and pMOS transistors are compensated by the ATVC to increase the output voltage and PCE. The PCE improvement is mainly because of the ATVC rather than a difference in transistors. For PCE > 20%, the input power is from −11 to −1 dBm with a range of 10 dB. This VM with a wide input power range is suitable for the RF energy-harvesting applications, such as IMDs and wearable devices.

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