A Wide Dynamic Range Buck Converter With Sub-nW Quiescent Power

Arun Paidimarri, *Member, IEEE*, and Anantha P. Chandrakasan, *Fellow, IEEE*

***Abstract*— A buck converter in 65-nm CMOS is optimized for a low quiescent power of 240 pW. It operates with input 1.2–3.3 V and regulates the output from 0.7–0.9 V. Control circuits are designed for low leakage and static current, and scale in power over a hertz to megahertz frequency range, resulting in a wide load current dynamic range of 2×10^6. With a 2-V input, the converter has a peak efficiency of 89% and delivers load currents of 500 pA to 1 mA with efficiency better than 50%. The peak efficiency is 92% for a 1.2-V input.**

***Index Terms*— Buck converter, dynamic range, efficiency, energy harvesting, Internet of Things (IoT), low leakage, output regulation, picowatt, pulse generation, quiescent power, *RC* delay, scalable frequency generation, zero current switching (ZCS).**

I. Introduction

THE Internet of Things (IoT) aims to improve safety, health, and efficiency in industrial systems, home automation, personal fitness, medicine, as well as environmental monitoring. These systems are most useful when operating energy-autonomously or while possessing tens of years of battery lifetime. In these increasingly energy-constrained systems, efficient power converters are critical to convert disparate battery and energy harvester voltages to the operating points of the load circuits. It is critical that these converters have lower quiescent power and wider dynamic range of power than both the loads and sources in order to not limit the operation and lifetime of the full system. In this paper, we design an inductive buck converter for such energy-constrained systems. In the following, we characterize both sources and loads to motivate the specifications.

A. Low Quiescent Power, Wide Dynamic Range Sources

Thin-film batteries such as [1] can provide high peak pulsed currents up to 10 mA, and also have a low self-discharge rate as low as a nanoampere, giving a 1×10^7 dynamic range. Harvesting sources such as solar power have an intrinsically wide dynamic range of available power, with differences between indoor and outdoor lighting of 10 lx to 100 klx, giving a dynamic range of about 1×10^4. Additionally, weak energy harvesting sources such as biological batteries [2] with around 1 nW of available power further motivate low-quiescent converter designs.

B. Low Quiescent Power, Wide Dynamic Range Loads

Heavily duty cycled IoT loads have seen significant advances in both leakage optimization and dynamic range. Recent works include radios such as [3] with 400-pW leakage and ON/OFF power ratio of 7.6×10^7, ultra-low-leakage processors such as [4] at 30 pW, scalable ADCs such as [5] with 600-pW leakage and 10^4 dynamic range, clocking systems such as [6] with 5-pW leakage and 5×10^7 dynamic range, and always-on wake-up radios with sub-10-nW operating power [7]. These circuits strongly motivate the design of wide dynamic range and low quiescent power converters.

As shown above, energy sources with sub-nW standby and greater than 10^7 dynamic range are feasible, and similarly, loads with pW-leakage and dynamic range close to 10^6 are feasible. However, existing converters operate over limited dynamic ranges, limited to 2×10^5 as in [8] and quiescent power limited to 0.5 nW [2]. In this paper, we aim to bridge the gap in the power converter space with the design of a buck converter with 240-pW quiescent power and a dynamic range of 2×10^6 and a peak efficiency of 92%. The converter operates over $V_{IN} = 1.2$–3.3 V and $V_{OUT} = 0.7$–0.9 V. This paper expands on work initially presented in [9].

II. Converter Design Overview

A. Prior Art

We summarize some of the recent low quiescent and/or wide dynamic range converters and their key insights. TPS62736 from Texas Instruments [10] is one of the lowest quiescent commercial chip, and covers 1-μA to 100-mA load currents. The design uses hysteretic control, pulse frequency modulation (PFM) operation, and a duty-cycled voltage reference scheme [11] to minimize control power.

In [12], the authors present a complete solar energy harvesting and battery management IC with a 3.2-nW quiescent power and operation from 10 nW to 1 μW. The authors minimize switching power through an asynchronous control scheme that results in transitions only when a pulse of energy is transferred. Extending the dynamic range using this approach requires tunable bias currents that adjust the control circuit bandwidth.

In [2], the authors present a 1.1-nW energy harvesting boost converter (40 mV to 0.8 V) with a quiescent power

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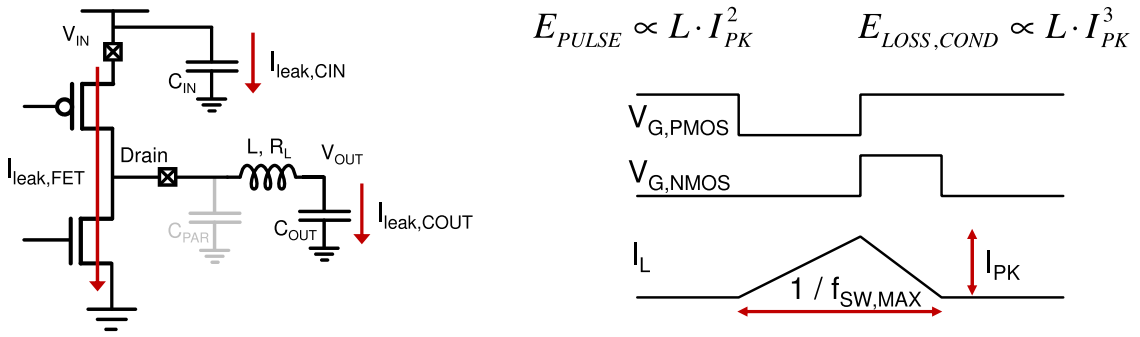


Fig. 1. Power stage and ideal waveforms for a buck converter, with key leakage paths highlighted.

of 544 pW. They identify power FET leakage and ceramic capacitor leakage as limiting constraints at these low power levels. It includes fixed frequency operation (12.8 Hz), because the input power is constant, and an implicit output voltage regulation scheme.

A self-oscillating switched capacitor converter design is presented in [13], where a 10^3 dynamic range and 1.7-nW quiescent power is achieved. It demonstrates adaptive frequency of operation as a key idea to minimize control power losses. Similarly, [14] presents an inductive converter with adaptive frequency generation in order to expand its dynamic range of conversion.

Converters such as [8] and [15] have shown wide dynamic range through multi-mode operation, with PFM at low power and pulse width modulation (PWM) operation at higher power levels. Power gating of the PWM control circuits is applied to reduce overhead at low powers.

In this paper, we design an inductive buck converter in PFM operation, and aim to achieve a wide dynamic range and low quiescent power while maximizing efficiency. Some of the key insights from the above-mentioned works inform the design choices, as described in the rest of the paper.

B. Design of the Power Stage

Fig. 1 shows the power stage and ideal waveforms of a buck converter operating in discontinuous conduction mode (DCM). The power delivered to the output is traditionally given by

$$P_{\mathrm{OUT}} = \eta_{\mathrm{Pwrstg}} \cdot f_{\mathrm{SW}} \cdot E_{\mathrm{Pulse}} \tag{1}$$

where E_{Pulse} is the energy per pulse drawn from the input, η_{Pwrstg} is the efficiency of the power stage, and f_{SW} is the effective switching frequency of the converter.

However, Fig. 1 also highlights leakage paths that are important because of the low-quiescent requirement. The tradeoffs are discussed below for the nominal operating point of $V_{\mathrm{IN}} = 2$ V and $V_{\mathrm{OUT}} = 0.8$ V. Our measurements show that the ceramic decoupling capacitors C_{OUT} and C_{IN} are limited to 350 and 150 nF, respectively, for their leakage to be lower than 50 pW. Typical PFM converters use larger decoupling around 1–22 μF in order to minimize voltage ripple. The step change in output voltage due to a pulse of energy E_{Pulse}, drawn from the input, is given by

$$\Delta V_{\mathrm{OUT}} = \frac{\eta_{\mathrm{Pwrstg}} \cdot E_{\mathrm{Pulse}}}{C_{\mathrm{OUT}} \cdot V_{\mathrm{OUT}}}. \tag{2}$$

This implies that for around 5-mV voltage step, E_{Pulse} should be as low as 1.5 nJ. A low C_{OUT} also imposes a more stringent specification on the output regulation circuits, as the bandwidth of the control needs to be close to the maximum switching frequency of operation.

A second significant source of leakage is the power FETs themselves. As shown in Section III-A, power FETs optimized under leakage constraints lead to switch R_{ON} of 3–5 Ω for a leakage of about 40 pW. The limited on-resistance specification implies that the inductor peak current I_{PK} should be well below 10 mA in order to limit conduction losses.

Hence, the constraints for the converter are that E_{Pulse} is about 1–2 nJ, switch R_{ON} is about 3–5 Ω, and inductor peak current I_{PK} is under 10 mA. These key design constraints couple with traditional design tradeoffs, such as inductor size, pulse widths, and associated frequency-dependent core losses and wiring losses in the inductor. Our optimized design uses a 47-μH inductor operating with pulse widths around 240 and 360 ns for the PMOS and NMOS devices, respectively, yielding a maximum switching frequency of $f_{\mathrm{SW,MAX}} = 1.6$ MHz.

Thus, we now have a power stage design with under 100-pW leakage and a maximum switching frequency of about 1 MHz and an energy per pulse of 1–2 nJ. The lower end of the frequency of operation of the converter is well below 1 Hz. This results in intrinsically wide dynamic range in addition to low quiescent power.

C. Design of the Control Circuits

Since the power stage is optimized for a given energy per pulse E_{Pulse} with an efficiency η_{pwrstg}, f_{SW} is nominally (excluding control losses) given by rewriting (1)

$$f_{\mathrm{SW}} = \frac{P_{\mathrm{OUT}}}{\eta_{\mathrm{pwrstg}} \cdot E_{\mathrm{Pulse}}}. \tag{3}$$

If the dynamic energy per cycle of the control circuits is E_{Ctrl} and the control circuit operates at f_{CLK}, the overall efficiency is expressed as[1]

$$\eta_{\mathrm{sys}} \approx \frac{f_{\mathrm{SW}} \cdot \eta_{\mathrm{Pwrstg}} \cdot E_{\mathrm{Pulse}}}{f_{\mathrm{SW}} \cdot E_{\mathrm{Pulse}} + P_{\mathrm{Leakage}} + f_{\mathrm{CLK}} \cdot E_{\mathrm{Ctrl}}}. \tag{4}$$

[1]This equation assumes that all control circuits operate from V_{IN} and all switch at f_{CLK}. This will be adjusted to account for implementation details in (7)

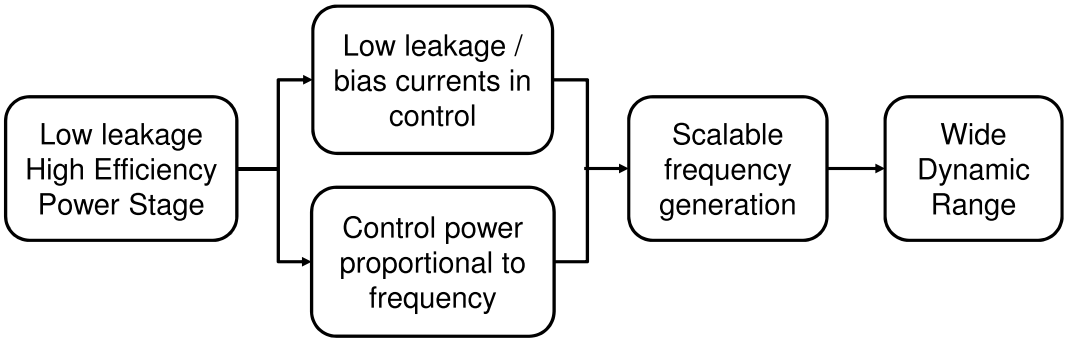


Fig. 2. Design philosophy for a low quiescent power wide dynamic range buck converter.

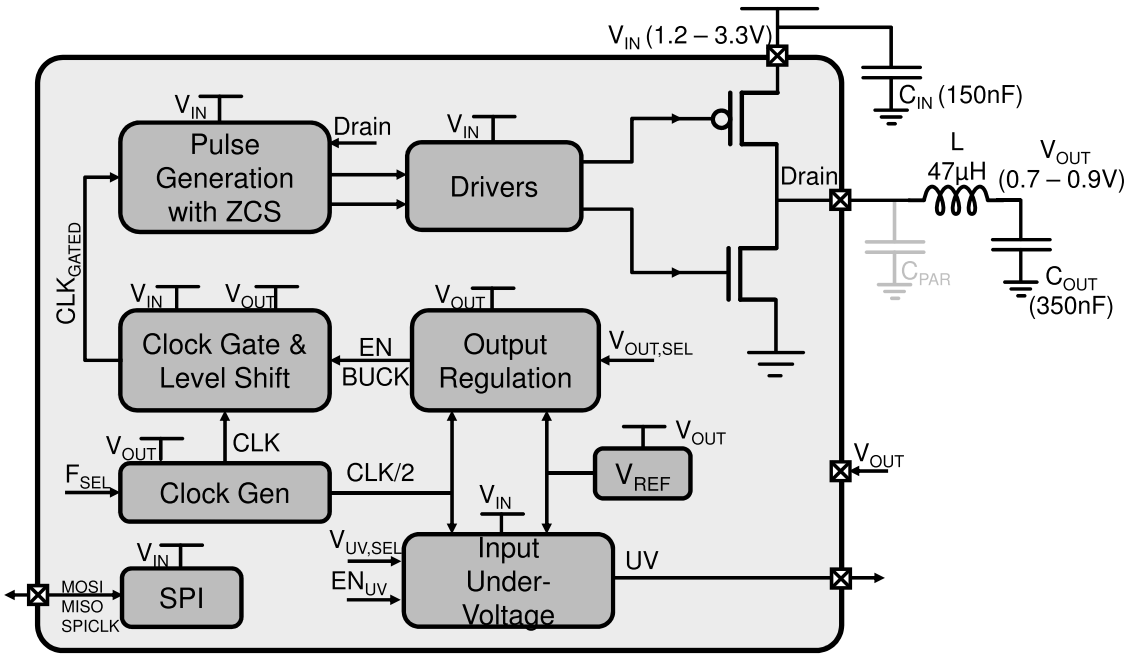


Fig. 3. System Architecture for a low quiescent power wide dynamic range buck converter.

Thus, in order to achieve high efficiency across a wide range of f_{SW}, in this paper, the following design philosophy is applied for control circuits. First, all control circuits are designed for low leakage and low bias/static currents. Second, the control circuits should have scalable power consumption proportional to the frequency of operation with valid operation over the full frequency range up to 1 MHz. Third, a scalable frequency generation circuit efficiently generates a system frequency f_{CLK} close to the optimum f_{SW} ($f_{CLK} > f_{SW}$). This is captured in Fig. 2.

D. Architecture

Fig. 3 shows the complete block diagram of the converter. The power stage is preceded by driver circuits and pulse generation blocks, including zero current switching (ZCS) for efficiency maximization. The output regulation block generates a gating signal that clock gates the pulse generation and driver circuits. A clock generation block generates the system clock f_{CLK} and a divided version for output regulation. It can be seen that the clock gating leads to $f_{SW} < f_{CLK}$. The chip

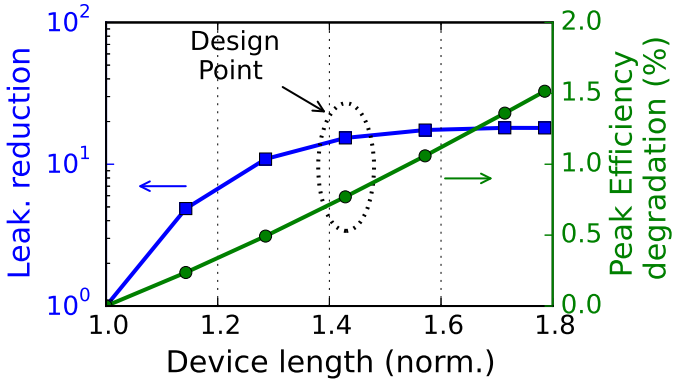


Fig. 4. Leakage optimization for the power FET.

also includes an optional input under-voltage checking circuit for use with, as an example, battery monitoring [12]. A serial interface (SPI) is used to set the configuration bits for the converter. In this paper, the system frequency f_{CLK} is programmed externally, but works such as [14] show techniques for self-tuning depending on load currents.

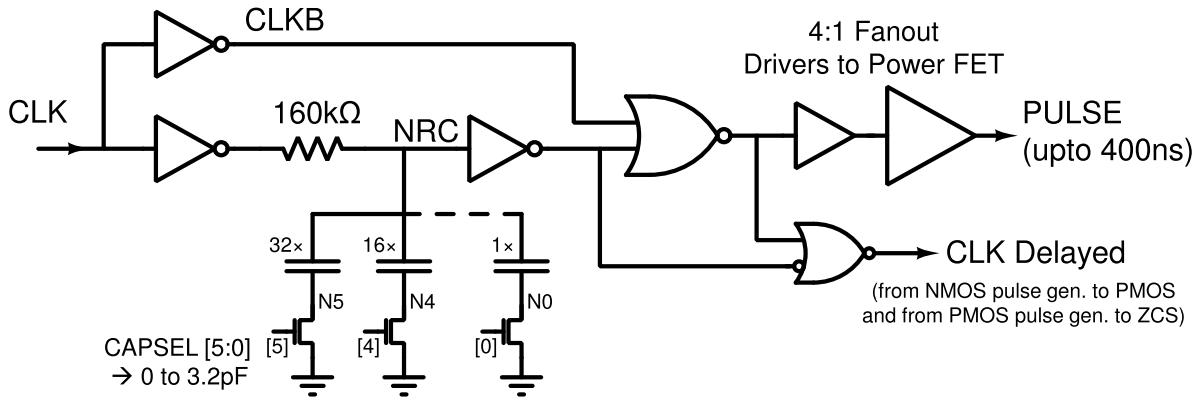


Fig. 5. Circuit implementation of a tunable pulsewidth generator with scalable frequency of operation.

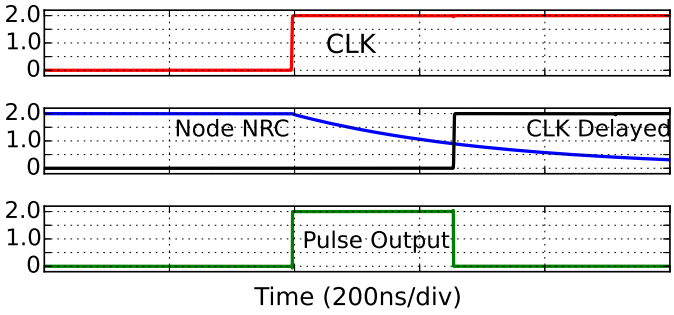


Fig. 6. Simulation waveforms for the pulse generation circuit.

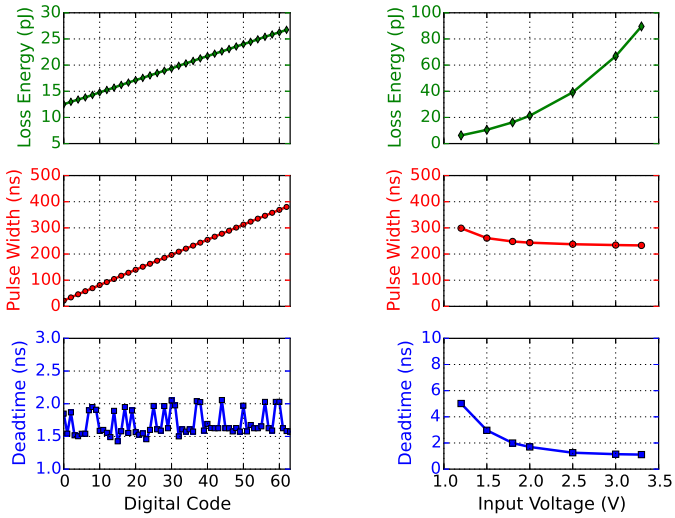


Fig. 7. Measurements of pulsewidth, deadtime, and energy loss in the pulse generation and driver circuits. They show (a) digital tuning pulsewidth and (b) pulsewidth variation with V_{IN}.

The clock generation and output regulation blocks run from the output voltage V_{OUT} to minimize switching power consumption. The pulse generation circuits and drivers are powered from the input voltage V_{IN}. The gated clock is level shifted up from V_{OUT} up to V_{IN}. These additional losses and resulting system efficiency are

$$P_{\mathrm{lossVIN}} = P_{\mathrm{LeakVIN}} + f_{\mathrm{SW}} \cdot E_{\mathrm{Pulsegen}} \tag{5}$$

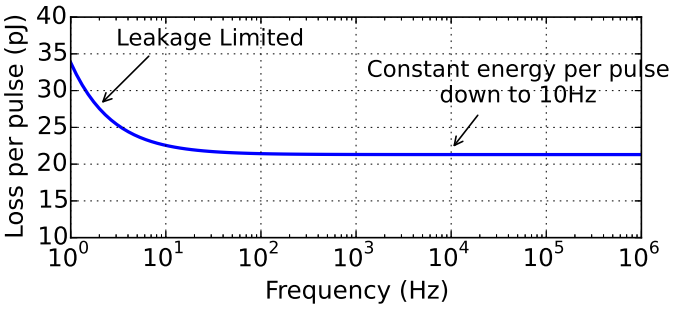


Fig. 8. Measurement of frequency scalable operation of the pulse generation and driver circuits. Energy per cycle is constant down to 10 Hz.

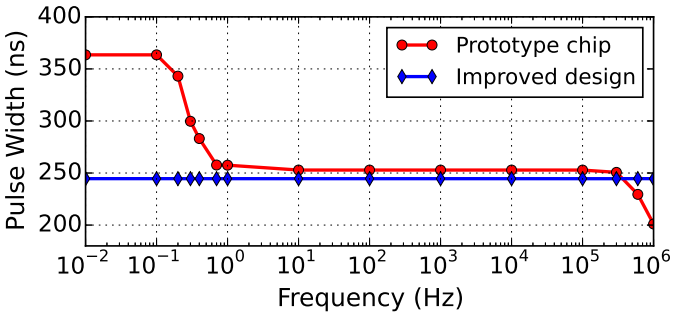


Fig. 9. Simulated pulsewidth with frequency scaling shows non-ideal behavior at the extreme ends of frequencies. Also shown is the simulation with an improved design (Fig. 10).

$$P_{\mathrm{lossVOUT}} = P_{\mathrm{LeakVOUT}} + f_{\mathrm{CLK}} \cdot E_{\mathrm{Clkgen}} + \frac{f_{\mathrm{CLK}}}{2} \cdot E_{\mathrm{OutputReg}} \tag{6}$$

$$\eta_{\mathrm{total}} = \frac{f_{\mathrm{SW}} \cdot \eta_{\mathrm{Prwstg}} \cdot E_{\mathrm{Pulse}} - P_{\mathrm{lossVOUT}}}{f_{\mathrm{SW}} \cdot E_{\mathrm{Pulse}} + P_{\mathrm{lossVIN}}}. \tag{7}$$

E_{Pulsegen} also includes driver and ZCS energy. The efficiency is a more accurate version of (4) with voltage domains and clock gating due to voltage regulation taken into account.

An alternative implementation could also power the pulse generation also from V_{OUT} for lower power consumption, and then level shift the resulting pulses to the drivers. However, this was avoided due to the mismatch in level shifter delays and the larger deadtime, between the NMOS and PMOS pulses, that would be required to maintain efficient operation.

The dynamic range could be further enhanced with additional control circuits for a continuous conduction mode

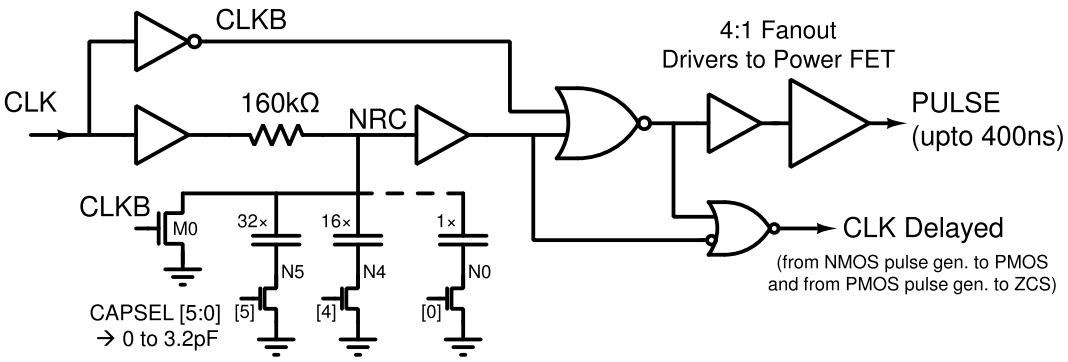


Fig. 10. Design of an improved pulse generation circuit (not implemented).

operation for high power levels, as was demonstrated in [8] and [15]. This requires no modifications to the power stage, while the added control circuits could be power gated in the DCM mode so as to not affect quiescent power.

Section III discusses the various blocks in Fig. 3, with system measurements in Section IV.

III. Circuit Design

A. Power FET Optimization

Design of the power FETs for the buck converter trades off switch resistance (and associated conduction losses), switch gate capacitance (and associated switching losses), and the leakage (affecting quiescent power).

Power FET leakage was optimized in [2] through the use of negative V_{GS} biasing in the off-state to strongly turn off the device. We avoid this approach, because: 1) negative V_{GS} results in reduced V_{IN} range of operation and 2) the overhead of the bias generators and the level converters required for the drivers, higher switching losses, and the added design complexity for wide frequency range of operation.

We apply an alternative leakage reduction approach through the use of longer length FET devices. Fig. 4 captures these key tradeoffs. This shows that a 40% increase in channel length for both FETs results in a 15× leakage reduction,[2] for the same switch resistance. The resulting degradation in the peak efficiency of the converter, due to increased gate drive losses, is less than 1%. The resulting sizing leads to switches with R_{ON} of 3–5 Ω with a leakage power of 40 pW. This approach does not degrade V_{IN} range and does not require any additional bias circuits.

B. Pulse Generation and Drivers

The pulse generation circuits generate the PMOS and NMOS pulses (up to 400 ns wide) with a guard time to prevent shoot-through currents. It operates from the gated clock. Fig. 5 shows the implementation. The pulsewidth is determined by the RC time constant at the node NRC. A 6-bit binary-weighted capacitor tunes the pulsewidth with a step size of 6 ns. A fan-out-of-4 buffer chain drives the power FET. The circuit also generates a delayed version of the clock aligned with the falling edge of pulse. The delayed clock from the PMOS pulse generator drives the NMOS pulse generator, which then drives the ZCS circuits (Section III-E). Fig. 6 shows simulated waveforms with a system frequency of 10 kHz.

[2]This is simulated for a typical corner. This leakage reduction varies from 7× in slow corner to 28× for fast corner, for the same 1% degradation in peak efficiency.

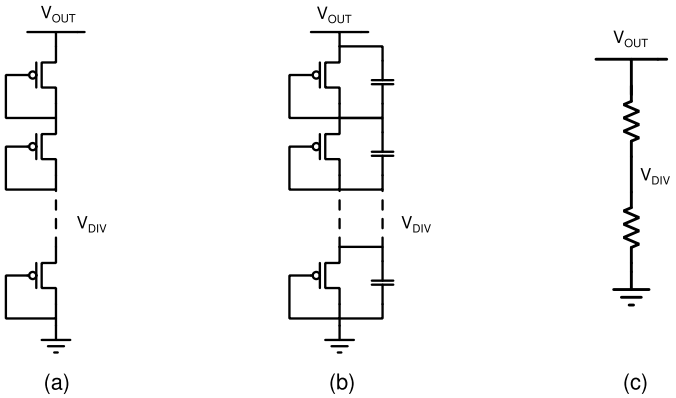


Fig. 11. Divider circuits for output regulation. (a) Diode-divider. (b) Diode-divider with parallel capacitive divider. (c) Resistor-divider.

This implementation is particularly well-suited for this paper. There are no bias currents, and low-leakage sizing of the gates leads to a leakage of 12.5 pW. Thick-oxide, high-V_T devices are used to reduce the leakage. The pulsewidth and step is

$$t_{\text{pulse}} = R \cdot C \cdot \ln(2) \tag{8}$$

$$t_{\text{step}} = R \cdot \Delta C \cdot \ln(2) \tag{9}$$

and is independent of the supply voltage, to the first order. The small step-size of 6 ns is achieved with $\Delta C = 50$fF, well within the mismatch limits of MIM capacitors, ensuring linearity and monotonicity over the 6-bit capacitor bank. Fig. 7(a) shows this with measurements at 2V operation, along with the switching energy per cycle (including the fixed 13 pJ of gate drive losses). Also shown is the deadtime between the NMOS and PMOS pulses, under 2 ns. Fig. 7(b) shows operation across varying V_{IN}. The losses are proportional to V_{IN}^2 and the deadtime is below 6 ns even down to 1.2-V operation.

Fig. 8 shows the energy per pulse over the frequency range of 1 Hz to 1 MHz. It shows constant energy per pulse down to 10 Hz, below which the 12.5-pW leakage begins to dominate.

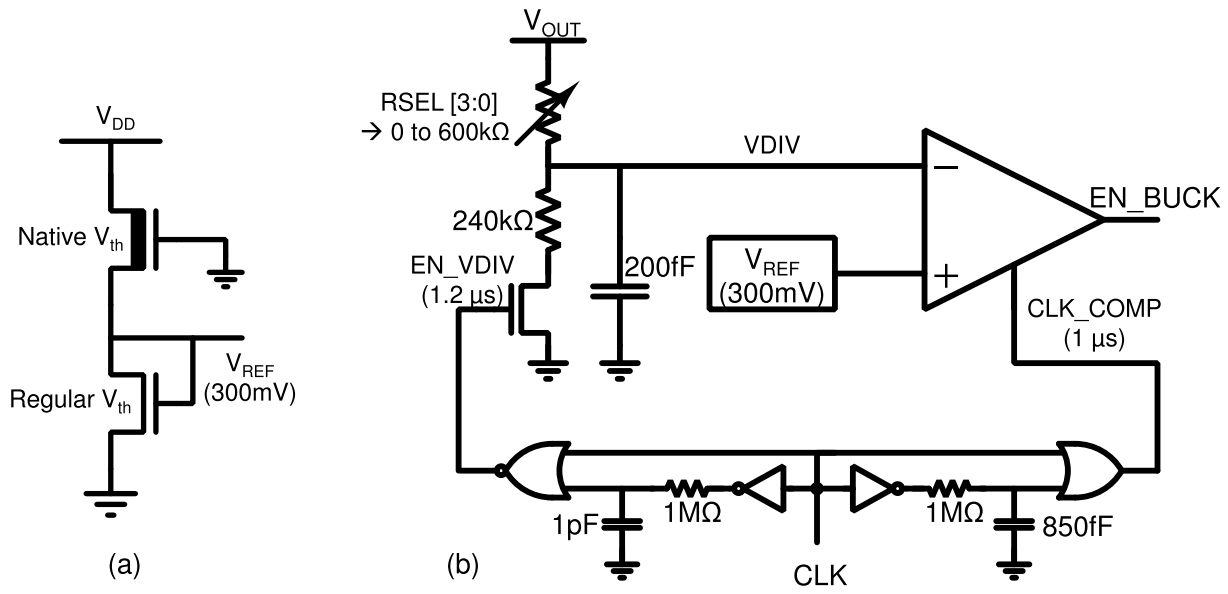


Fig. 12. Implementations of (a) picowatt-level voltage reference providing 300-mV output. (b) Output regulation circuit using a duty cycled voltage divider and the picowatt voltage reference.

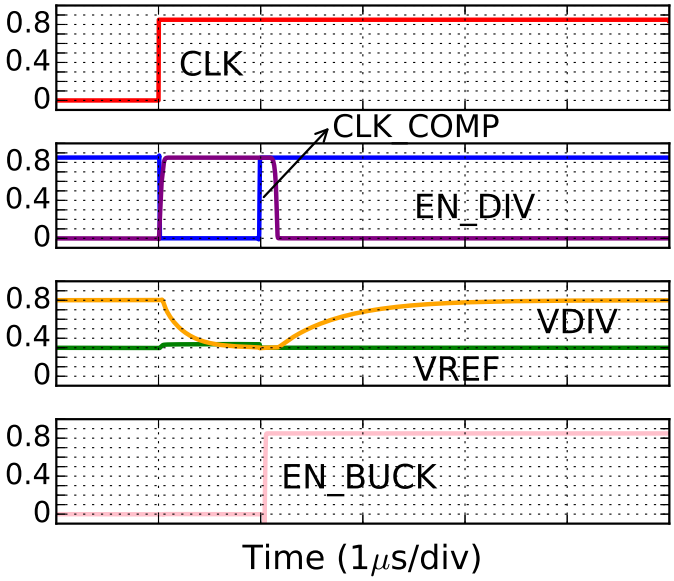


Fig. 13. Simulation waveforms showing the functionality of the output regulation circuit.

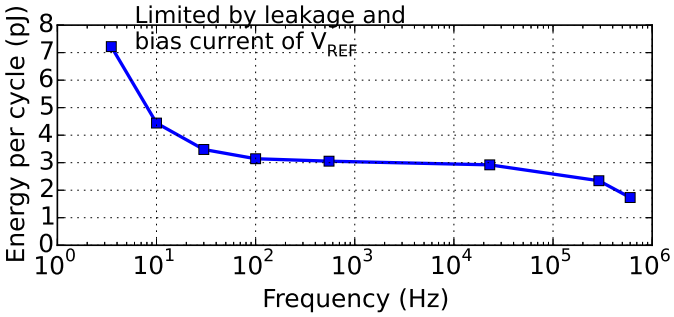


Fig. 14. Measurement of the frequency scalable operation of the output regulation circuits showing constant energy per cycle.

Finally, the simulated pulsewidth as a function of frequency is shown in Fig. 9. Two non-idealities can be observed. At the high-frequency end, the node NRC never settles to V_{DD} or V_{SS}, leading to shortening of the pulses.[3] At the low-end, below 1 Hz, the pulsewidth increases. This is due to the floating nodes N5–N0 in the capacitor bank (when digital bit is OFF, see Fig. 5). At these low frequencies, these nodes settle down to 0 V due to switch leakage. As node NRC decays, capacitive coupling leads to negative voltage, turning on the body diode, thus delaying the pulse by up to 110 ns. As this effect is only observed below 1 Hz,[4] the resulting efficiency degradation only affects quiescent-mode or at load currents well below 1 nA.

1) Improved Pulse Generation: Fig. 10 shows an improved design for pulse generation. This circuit was not included in the test-chip, but the simulation result of Fig. 9 shows how it could be used to improve the non-idealities discussed previously. The polarity of the NRC pulse is reversed, thereby preventing the body-diode turning on during pulse generation. Second, transistor M0 resets the capacitor bank to 0 V on the falling edge of CLK, thus always ensuring a 0-V initial condition on node NRC even up to 1-MHz operation.

C. Output Regulation

The output regulation circuit monitors the output voltage and generates the clock gating signal for the pulse generation block. The key requirement is that at high load currents, and thus high system frequency of operation, the circuit needs to have high bandwidth (up to 1 MHz) in order to limit the output ripple under the constraint of low C_{OUT}, as described in Section II. On the other hand, at the low end of system frequencies, ultra-low power operation (pW) is required; however, low bandwidth operation is sufficient. Output regulation

[3]This reduces the energy conversion per pulse, thereby reducing efficiency, but by less than 2% in this design.

[4]As sub-1-Hz operation was not simulated before the tape-out, this phenomenon was not observed.

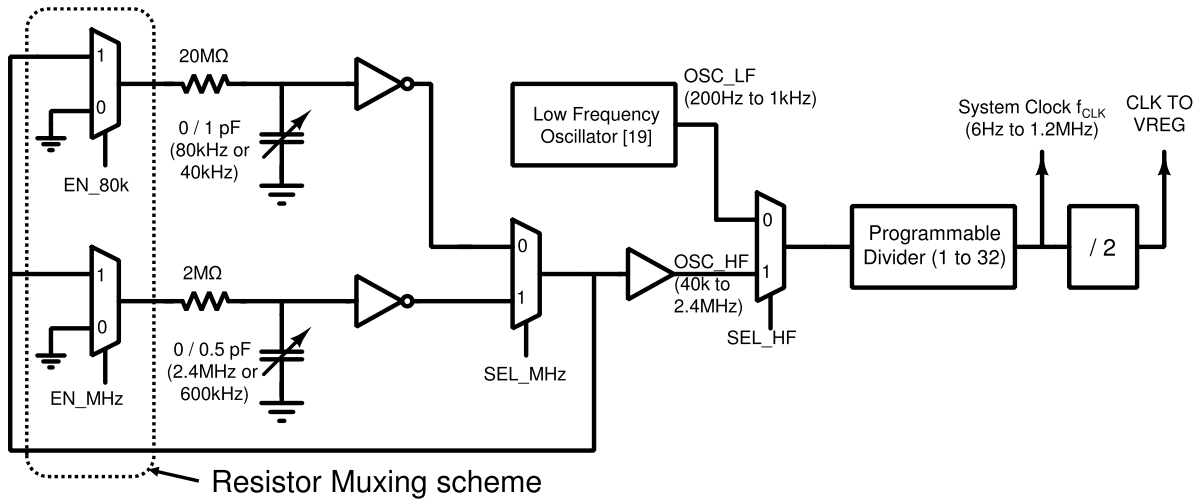


Fig. 15. Circuit implementation of the scalable frequency generation.

requires a voltage reference, a programmable voltage divider and a comparator.

Fig. 11 shows options for the divider. A diode divider provides low-power operation (under 10 pA in [12] and [16]), but it has a low bandwidth and does not respond at high load currents. A diode divider coupled with a capacitive divider again has low-power operation, and ideally provides good ac-response (under well-matched no-load conditions) to step transients [13]. However, it has poor dc settling response and poor immunity to capacitive coupling. Simulations indicate greater than 100 mV uncertainty in output voltage regulation. Finally, a true resistive divider can be sized for a given bandwidth requirement, but it does not scale for wide frequency ranges, due to static current.

Fig. 12 shows the implementation of output regulation using a duty-cycled resistive divider. Fig. 13 shows simulated waveforms. On the rising edge of clock, the comparator is reset and the divider is enabled for 1.2 μs (through an RC delay). After allowing 1 μs of divider settling time, the comparator is triggered. The additional 0.2 μs is a guard-time to account for RC-delay mismatch and comparator settling. The comparator output EN_BUCK is the clock gating signal for the pulse generation block. The strong-arm comparator [17] is designed to provide symmetric coupling onto the VDIV and VREF nodes, thus eliminating systematic errors.

A voltage reference of 300 mV is produced using a two-transistor circuit from [18]. This consumes only 11 pW and is thus not duty cycled like in [11]. Also, the voltage reference is not a dynamic node, and thus does not require high bandwidth. The output voltage is regulated to

$$V_{\text{OUT}} = 300\ \text{mV} \cdot \frac{\text{RSEL} \cdot 40\ \text{k}\Omega + 240\ \text{k}\Omega}{240\ \text{k}\Omega} = 50\ \text{mV} \cdot (\text{RSEL} + 6) \quad (10)$$

leading to voltage step of 50 mV.

All circuits except the voltage reference have zero static current and the total leakage of the circuit is only 14 pW. The resistor divider is on for a fixed duration every cycle, leading to a fixed energy per pulse of about 1 pJ. Similarly the RC-delay circuits also consume a fixed energy per

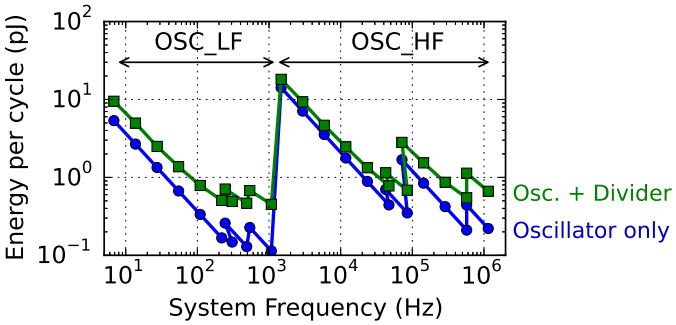


Fig. 16. Measurements of the energy per cycle for frequency generation.

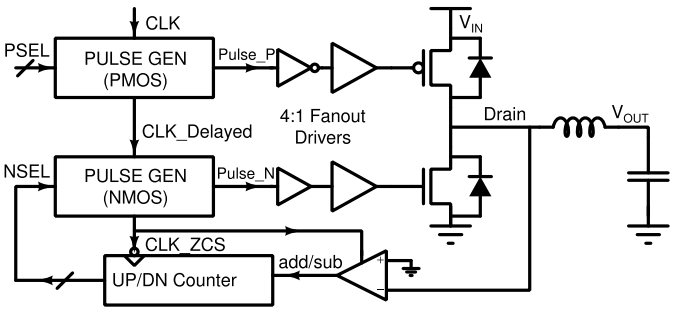


Fig. 17. Implementation of ZCS.

pulse (1 pJ each), leading to a total of 3 pJ. This is seen in the measurement results of Fig. 14 over the frequency range of output regulation (half the system clock frequency f_{CLK}, see Fig. 3). The leakage starts dominating below 10-Hz operation.

A similar circuit is used for optionally checking input undervoltage conditions (Fig. 3) and shares the voltage reference. The resistors in the voltage divider are modified to support the larger range of voltages for V_{IN} from 1.2 to 3.3 V. Due to the higher voltage of operation, this circuit consumes 10 pJ/cycle when enabled, and adds less than 10-pW leakage when disabled.

D. Scalable Frequency Generation

The frequency generation block is required to produce a wide range of frequencies with low energy per cycle. Fig. 15 shows the architecture used to produce a system clock

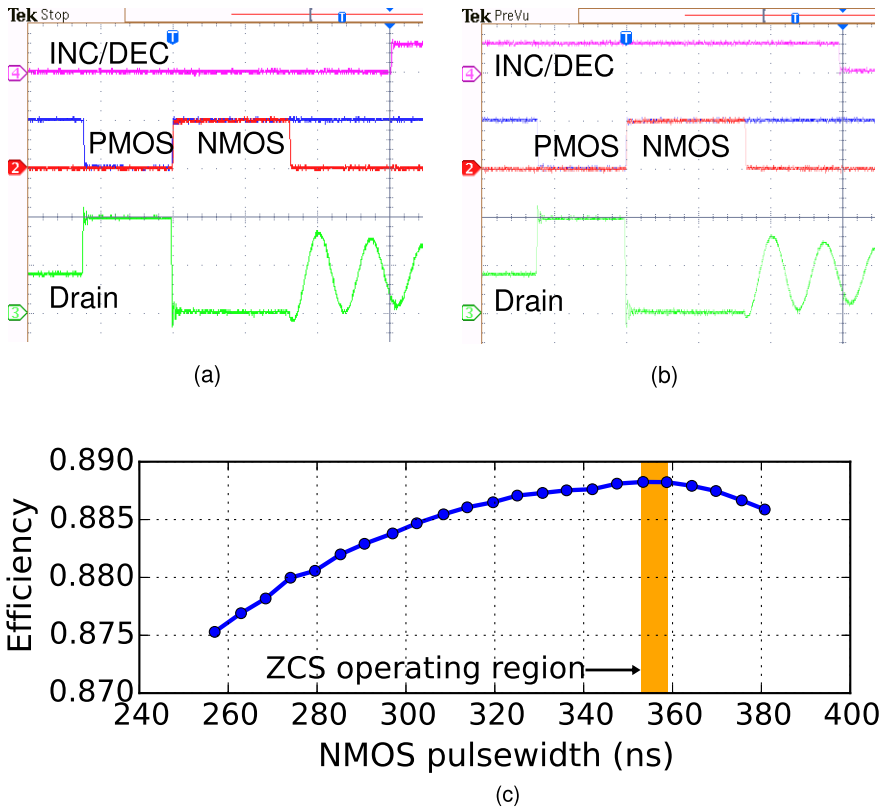


Fig. 18. Measurements of ZCS. Shown are the two states that the circuit dithers between in steady state. Waveforms for (a) pulsewidth (353 ns, code = 58) too low digital code increases for the next cycle and (b) pulsewidth (358 ns, code = 59) too high digital code decreases for the next cycle. (c) Efficiency plot showing peak efficiency operation with ZCS.

from 6 Hz up to 1.2 MHz. It uses a combination of digitally multiplexed oscillators and digital frequency dividers.

Low frequencies (up to 1 kHz) are generated by a gate-leakage-based oscillator described in [19]. Capacitive tuning in the circuit provides frequency tuning from 200 Hz to 1 kHz.

High frequencies (up to 2.4 MHz) are generated with an RC-based relaxation oscillator. Capacitive tuning can provide limited frequency tuning before CV^2 energy overhead dominates. Thus, tuning of the resistor is also employed. However, as is typical, if an analog switch is used to multiplex resistors, frequency tuning is achieved, but the parasitic capacitance of the resistor is still switched, leading to energy loss. However, a digital mux can be employed (as shown in Fig. 15) to provide up to 2.5× power reduction, in simulations. This, however, requires a replica of the capacitor bank in the two multiplexed paths. The 2-MΩ path provides 2.4-MHz and 600-kHz clocks, while the 20-MΩ path provides 80- and 40-kHz clocks.

Finally, the intrinsic oscillators are multiplexed to a programmable digital divider (up to 32×) in order to achieve the low frequencies and for more fine-grained clock frequency control. Overall, these options achieve 6-Hz to 1.2-MHz system clocks.

Fig. 16 shows the measured energy efficiency of the clocking system. The digital divider leads to proportional worsening of the energy per cycle due to the fixed power of the oscillator (for a given oscillator mode). The energy per cycle is less than 20 pJ across the entire frequency range. The gate-leakage oscillator itself is as low as 120 fJ/cycle at 1 kHz and the RC oscillator is as low as 110 fJ/cycle at 2.3 MHz.

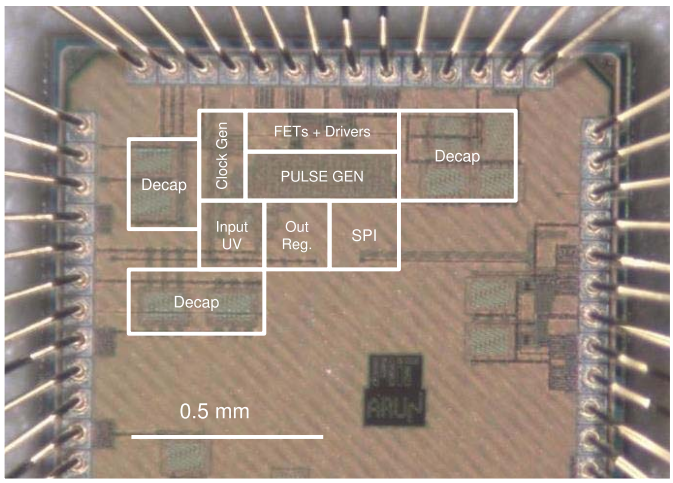


Fig. 19. Die photograph of the buck converter fabricated in 65-nm CMOS.

Some recent ultra-low-energy wide frequency range oscillators could also potentially replace this clocking architecture. For example, [6] presents a ring oscillator with a constant 0.8-pJ/cycle operation over 21 Hz–60 MHz and also includes a digital frequency tuning capability. A second example is presented in [20] with frequency proportional to bias current, achieving sub-3-pJ/cycle operation over 10 Hz–1 MHz.

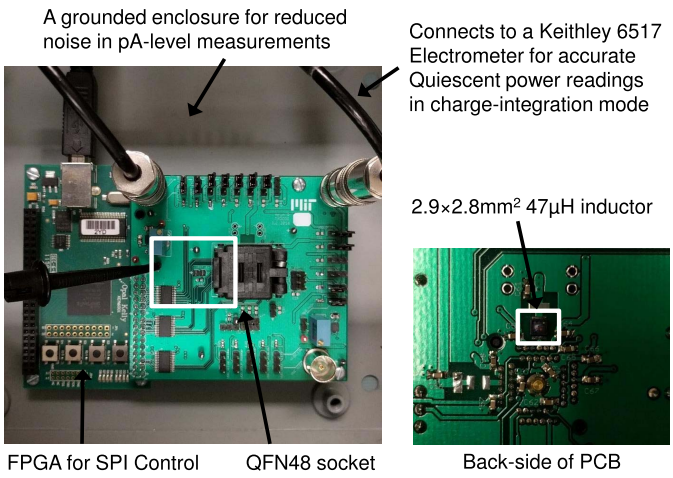


Fig. 20. Measurement setup and PCB used for measurement. Also shown is the inductor.

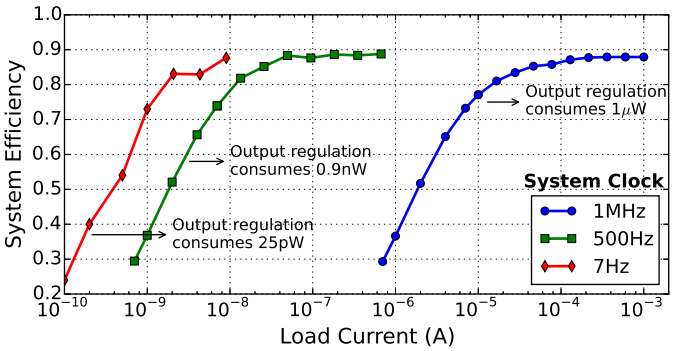


Fig. 21. Efficiency measurement of the buck converter with fixed frequency of operation.

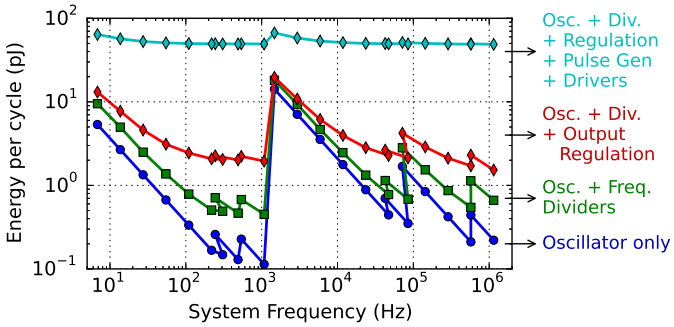


Fig. 22. On-chip loss components per cycle for the converter at optimum frequency of operation.

However, this design requires a variable bias current generator.

E. Zero Current Switching

The ZCS implementation is shown in Fig. 17. It is similar to the schemes used in [2] and [21]. It uses an iterative scheme to converge on the optimal NMOS pulse widths. The direction of inductor current at the end of the NMOS pulse is sensed based on the drain voltage. Positive current causes the NMOS body diode to turn on, leading to negative gate voltage, requiring an increase in the pulsewidth for the next cycle; a negative inductor current causes the drain voltage to be positive, and requires a decrease in the pulsewidth.

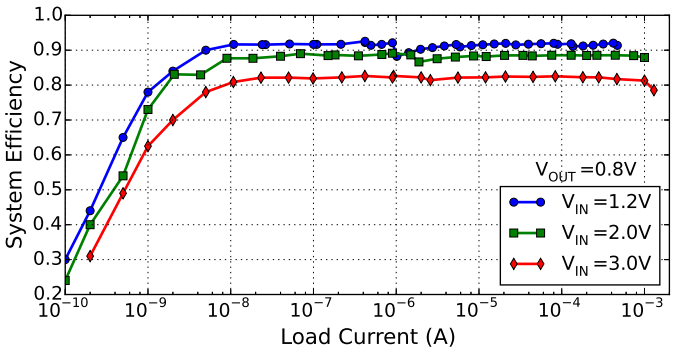


Fig. 23. Measurements of efficiency with variable system frequency operation.

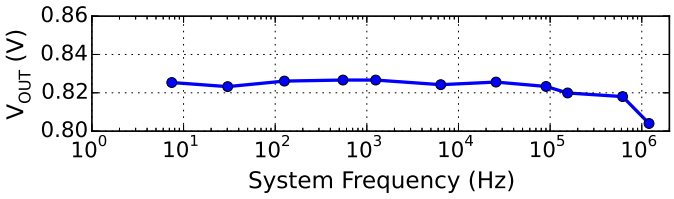


Fig. 24. Measured output regulation as a function of the system frequency.

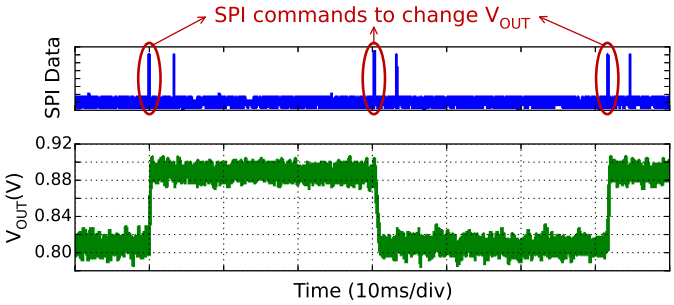


Fig. 25. Measurements of the output regulation showing response when an SPI command requests change of V_{OUT} from 0.8 to 0.9 V.

A clocked comparator compares the drain voltage to 0 V and adds or subtracts 1 using a counter. The circuit is ideal for this converter, because it requires no bias currents or reference voltages. The switching power is negligible in comparison with the gate driver and pulse generation losses. Measurements with $I_{OUT} = 85\ \mu$A and CLK = 45 kHz are shown in Fig. 18. The NMOS pulsewidth dithers between codes 58 and 59, both of which are close to the peak of the efficiency curve as is highlighted, demonstrating the optimality of the ZCS scheme.

IV. System Measurements

The design was fabricated in a 65-nm CMOS process. The die photograph is shown in Fig. 19 and the core area is 0.32 mm^2.

The measurement setup used is shown in Fig. 20. All the measurements were performed with a 48-pin QFN package using a socket, on a 62-mil four-layer printed circuit board. All measurements are performed using an 2.9 mm × 2.8 mm × 2.0 mm 47-μH inductor from Coilcraft (1008LS-473XJLB). The inductor has a dc resistance of 10.7 Ω and Q of about 35 at 2 MHz. Appendix V presents additional inductor measurements. The ground plane under the inductor is removed in order to minimize the capacitance of

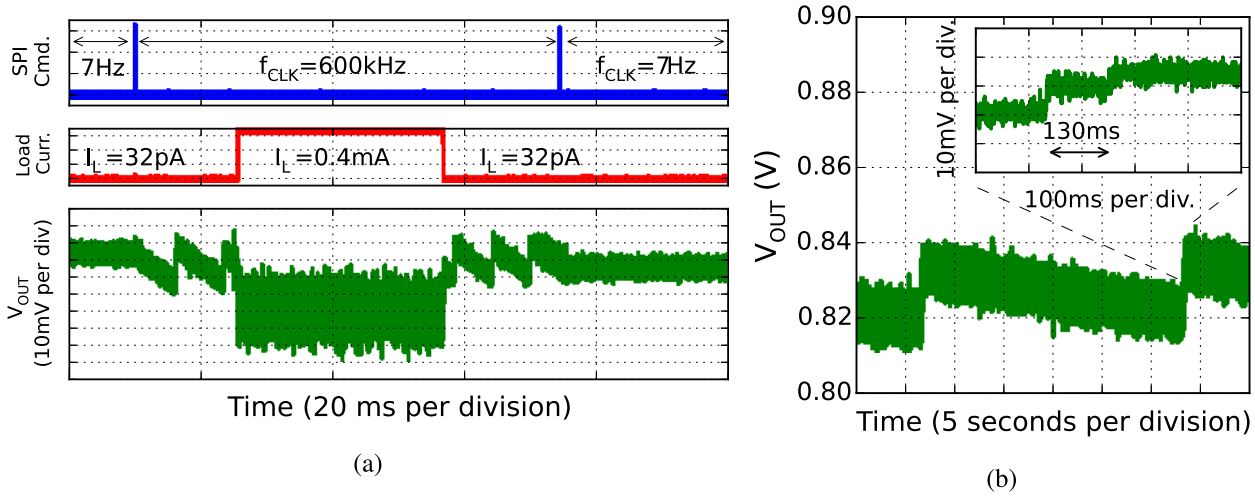


Fig. 26. Measurement of (a) near-zero to near-full-load transient response with I_{Load} switching from 32 pA to 0.4 mA. SPI commands updating system clock frequency f_{CLK} are also shown. (b) V_{OUT} in steady-state quiescent operation.

the switching node. A grounded enclosure is used to reduce noise in pA-level measurements. An field programmable gate array is used to control the SPI interface of the chip. This SPI interface is used, among other things, to externally set the system frequency.

A. Fixed Frequency Operation

Fig. 21 shows efficiency measurements for the converter with $V_{\text{IN}} = 2$ V and $V_{\text{OUT}} = 0.8$ V in fixed system frequency operation mode, similar to conventional converters. In this mode, the clock generation and the output regulation circuits consume a fixed amount of power, while the pulse generation, drivers, and ZCS circuits operate from a gated clock. For example, with 1-MHz operation, output regulation consumes 1 μW, and the converter supports load current from 1 mA down to about 1 μA, or close to three orders of magnitude of dynamic range. The peak efficiency is 88%, but drops to 50% at 2-μA load.

At a much lower system frequency like 500 Hz, the baseline power consumed by clock generation and output regulation drops to 0.9 nW, the peak efficiency climbs back up to 89%, and the converter operates over another three orders of magnitude of load current. Finally, at the lowest system frequency of 6 Hz, the output regulation drops to 25 pW, and is ultimately limited in load current range due to leakage power consumed by all the remaining blocks in the design.

This demonstrates that if the system frequency f_{CLK} is at the optimal value f_{SW}, the overhead of the output regulation blocks can be made negligible, thus achieving the highest efficiency operation. However, when the system frequency is not optimal, the regulation and clock generation loss components dominate (due to gating of the pulse generation and drivers), thereby resulting in efficiency degradation [see (7)].

This is further highlighted in the measurements of Fig. 22 where all the losses in the converter are plotted for operation at the optimal system frequency. It can be seen that the output regulation and clock generation are negligible compared with the losses due to pulse generation and drivers, for a total loss around 50–70 pJ per cycle. This energy is in comparison with the 1–2 nJ of energy processed by the buck converter each cycle. This also shows that all the control circuits demonstrate effective frequency scaling, thus enabling efficient buck conversion over a wide dynamic range of load currents.

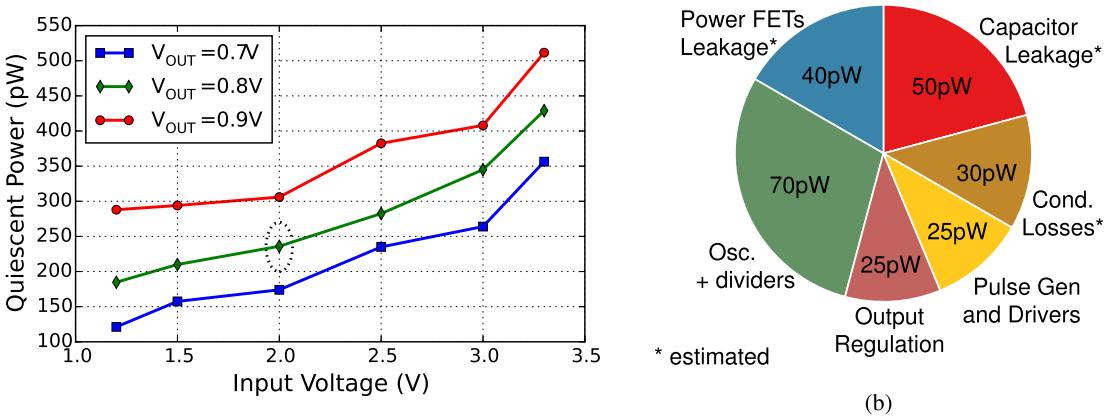
B. Variable Frequency Operation

Fig. 23 shows the full system efficiency measurements across the load current range, with variable frequency operation at the optimal values. Shown are the measurements with $V_{\text{OUT}} = 0.8$ V and V_{IN} of 1.2, 2.0, and 3.0 V. At $V_{\text{IN}} = 2$ V, the circuit delivers 500 pA up to 1 mA with an efficiency greater than 50% (a 2×10^6 dynamic range). It maintains an efficiency greater than 80% at all loads above 4 nA, with a peak efficiency of 89%. For $V_{\text{IN}} = 1.2$ V, the peak efficiency improves to 92%, while at $V_{\text{IN}} = 3$ V, it is 80%. Overall, the converter is operational down to 100-pA load currents (efficiency about 25%).

When the clock generation switches from the *RC* oscillator to the gate leakage oscillator, the loss components decrease significantly as shown in Fig. 22 and this is also evident in the discontinuity in system efficiency. At the high-end of the load currents, the system frequency is close to 1.2 MHz; and as was noted in Fig. 9, the decreased pulsewidths result in a slight drop in efficiency by 1%–2%.

Fig. 24 shows the measured regulated voltage as a function of system frequency at no-load conditions. The variation is under 20 mV. Fig. 25 shows transient operation of output regulation with load current of 40 μA and $f_{\text{CLK}} = 90$ kHz. It shows steady-state ripple of about $\pm$10 mV. Also, when an SPI command requests a step-up/step-down in the output voltage, the circuit responds immediately; and as expected with a PFM mode buck converter, the system shows no overshoot.

Fig. 26(a) shows the full system operation with load transients. With $V_{\text{IN}} = 2$ V and $V_{\text{OUT}} = 0.8$ V, the load current is switched from near-zero load of 32 pA to near-peak load of 0.4 mA, a 10^7 ratio, using an external low-leakage switch. The SPI commands update the system clock frequ-



(a) (b)

Fig. 27. Quiescent power measurements. (a) Measurement of the quiescent power of the converter. Highlighted is the nominal operating point of 240 pW. (b) Pie chart showing the split of the various sources of loss in the system at the nominal operating point.

TABLE I
COMPARISON WITH THE STATE-OF-THE-ART LOW-QUIESCENT AND/OR WIDE DYNAMIC RANGE CONVERTERS

Ref	TI TPS62736 [10]	Chen JSSC'16 [8]	Jung ISSCC'14 [13]	Bandyopahyay JSSC'14 [2]	El Damak JSSC'16 [12]	This Work
Topology	Buck	Tri-mode buck	Self-osc. Switched cap	Boost	Boost and Buck	Buck
Tech. (nm)	-	180	180	180	130	65
η_{max} (%)	94	92	50	53	87	92
V_{IN} (V)	2.0–5.5	0.55–1.0	0.14–0.5	0.02–0.07	2.9–4.1	1.2–3.3
V_{OUT} (V)	1.3–5.0	0.35–0.5	2.2–5.2	0.8–1.1	1.0	0.7–0.9
P_{OUT}	1.3 µW–130 mW	50 nW–10 mW	5 nW–5 µW	544 pW–4 nW	10 nW–1 µW	400 pW–0.8 mW
Dynamic Range	1×10^5	2×10^5	1×10^3	1×10^1	1×10^2	2×10^6
$P_{Quiescent}$ (nW)	760	N/R	1.7	0.544	3.2	0.24

ency f_{CLK} between 7 Hz in the no-load state and 600 kHz in the high-load state. These commands are artificially delayed 20 ms before and after the load current steps to clearly illustrate the intermediate states of the system. The output voltage V_{OUT} is shown to be regulated as expected.

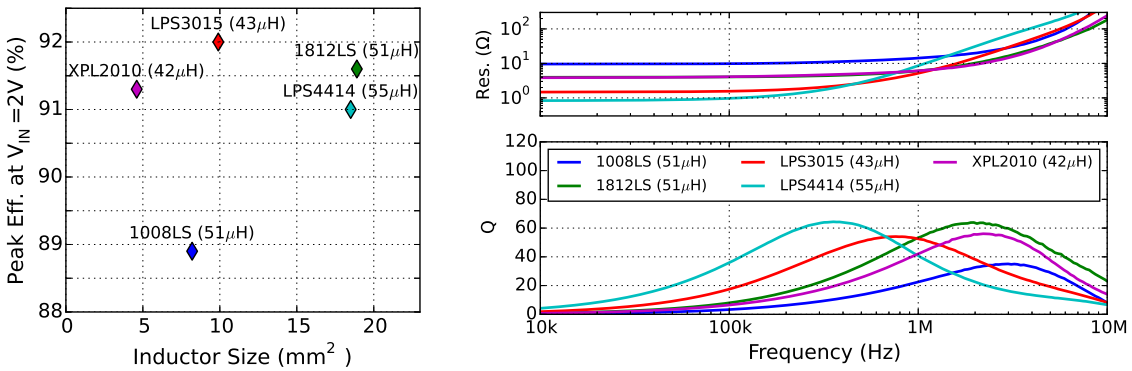
C. Quiescent Power

The quiescent power of the converter is measured as the power drawn from V_{IN} when the load current is 0 A. The system frequency is configured at the lowest value of 7 Hz. The measurements are made across the range of V_{IN} and V_{OUT} values showing values from 120 up to 500 pW [Fig. 27(a)]. At the nominal operating point of $V_{IN} = 2$ V and $V_{OUT} = 0.8$ V, the total quiescent power is 240 pW, with Fig. 27(b) showing the steady-state waveform for V_{OUT}. This shows f_{CLK} to be 7 Hz (130-ms period) with two pulses of energy transferred to the output every 28 s, leading to an effective switching frequency around 0.07 Hz. Given this, the quiescent power is measured by averaging over 3–5 min. Also, in order to accurately measure the combined leakage and intermittent pulses of currents, an electrometer in charge integration mode is employed (Fig. 20). Fig. 27(b) shows a pie chart showing an estimate of the split between major quiescent power components. The total is distributed relatively uniformly between the various components, with no one source being dominant, showing optimality of the design for the chosen system architecture.

Table I compares this paper with the state-of-the-art low quiescent power and/or wide dynamic range power converters, and includes buck and/or boost topologies. This paper presents one of the lowest quiescent power and one of the highest dynamic ranges while maintaining high efficiency, output voltage regulation and support for a wide input voltage range.

V. CONCLUSION

This paper presented the design and measurement results for a low quiescent power, wide dynamic range buck converter for emerging energy-constrained IoT systems. This is achieved through three key techniques. A power stage is simultaneously optimized for low leakage and high efficiency, thus providing a converter with an intrinsic wide dynamic range. Then, scalable control circuits, including output regulation, pulse generation, drivers, and zero current switching, are designed with low leakage, minimal or no static bias currents, and



(a) (b)

Fig. 28. Measurements with five different inductors. (a) Efficiency versus size. (b) Resistance and quality factor of the inductors.

with power consumption proportional to frequency. Third, a scalable frequency generation circuit is designed to drive the system with a variable system frequency from 6 Hz to 1 MHz. Together, these techniques result in one of the lowest reported quiescent power levels of 240 pW while also supporting a wide dynamic range of 2×10^6 in load currents from 500 pA up to 1 mA. The converter also achieves a peak efficiency of 92%.

Appendix
Inductor Choices

While all the measurements presented through this paper were with the Coilcraft inductor 1008 LS (2.9 mm × 2.8 mm × 2.0 mm), we present measurements with four additional inductors from Coilcraft with different sizes, which provide improved efficiencies. Fig. 28(a) shows the peak efficiency of the converter versus inductor size with $V_{\rm IN} = 2$ V. Fig. 28(b) shows measurement of the series resistance and quality factor as a function of frequency for all these inductors. The smallest inductor, XPL2010, is only 2.0 mm × 1.9 mm × 1.0 mm while providing a peak efficiency of 91.3% for $V_{\rm IN} = 2$ V. The most efficient inductor, LPS3015 (3.0 mm × 3.0 mm × 1.5 mm) while providing a peak efficiency of 92%. This is an additional efficiency improvement of 2%–3% over the measurements in Section IV.

The $f_{\rm SW,MAX}$ of the converter is 1.6 MHz and indicates the rise and fall times of the inductor current and corresponding magnetic flux. The inductor with the highest Q at 1.6 MHz, 1812LS, however, is not the most efficient due to a larger dc resistance. Among the measured inductors, LPS3015 provides the best tradeoff between dc and ac resistances.

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