

# Watt-Level mm-Wave Power Amplification With Dynamic Load Modulation in a SiGe HBT Digital Power Amplifier

Kunal Datta, *Student Member, IEEE*, and Hossein Hashemi, *Senior Member, IEEE*

**Abstract**—Performance limits and design techniques for Watt-level power amplification at millimeter-wave (mm-wave) frequencies using silicon germanium (SiGe) HBT Class-E power amplifiers (PAs) is presented in this paper. A Class-E power modulator architecture is proposed for demonstrating high-speed data transmission using ASK modulation at mm-wave frequencies. Several of these 1-b power modulators are power combined to realize a Watt-level digital PA with several levels of output amplitude at mm-wave frequencies. A dynamic load modulation concept is proposed to mitigate the effect of load pulling in the digital PA at power back-off. A tunable transmission line architecture with variable characteristic impedance is proposed to realize this dynamic load modulation network and enable efficiency enhancement at power back-off levels in the Watt-level digital PA. Watt-level power generation at mm-waves was demonstrated in a eight-way combined digital PA with dynamic load modulation, fabricated in a 0.13- $\mu\text{m}$  SiGe BiCMOS process with  $\approx 29$  dBm (0.8 W) measured output power at 46 GHz, 18.4% peak power-added-efficiency, and 60% of the peak efficiency at 6-dB power back-off.

**Index Terms**—Class-E, HBT, millimeter-wave (mm-wave), power amplifier (PA), silicon germanium (SiGe).

## I. INTRODUCTION

IN RECENT years, efficient Watt-level power generation at millimeter-wave (mm-wave) frequencies in silicon technologies has become important to support high-speed wireless communications, high-resolution radar, and imaging in military and commercial applications. Typical breakdown voltage of fast transistors ( $\sim 1\text{--}3$  V) and comfortable impedance levels ( $\sim 10\text{--}50 \Omega$ ) limit the output power of single-transistor mm-wave amplifiers to less than 20 dBm. Recent efforts at Watt-level power generation in both silicon CMOS and HBT technologies have relied on large-scale power combining of such  $<20$  dBm amplifier unit cells with  $<10\%$  overall power-added-efficiency (PAE) [1]–[3]. Reported integrated mm-wave power DACs capable of supporting modulation and power

Manuscript received March 8, 2016; revised July 22, 2016 and October 1, 2016; accepted October 25, 2016. Date of publication November 18, 2016; date of current version January 30, 2017. This paper was approved by Associate Editor Kenichi Okada. This work was supported by the DARPA ELASTx Program.

K. Datta is with Skyworks Solutions, San Jose, CA USA.

H. Hashemi is with the Department of Electrical Engineering-Electrophysics, University of Southern California, Los Angeles, CA 90089 USA (e-mail: hosseinh@usc.edu).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2016.2622710

control have peak output power of around 24 dBm and average PAE of less than 7% [2], [4].

Utilizing the previously reported performance limits of single-stage mm-wave Class-E power amplifiers (PAs) [5], the efficiency limits for Watt-level power generation at mm-wave frequencies are presented in this paper. This paper also provides detailed design techniques for implementing an mm-wave silicon germanium (SiGe) HBT digital PA capable of power control with several levels of output amplitude while achieving 18.4% peak PAE with 0.8-W peak output power [6]. Focus is also given on high-speed ASK data transmission using a Class-E power modulator architecture and a dynamic load modulation technique for enhancing efficiency at backed-off power levels. Section II covers the performance limits of multistage Class-E amplifier chains at mm-wave frequencies. Section III covers the theoretical maximum achievable PAE for Watt-level power generation in a SiGe HBT process for different power combining/stacking architectures. In Section IV, a technique for transmitting high-speed data using ASK modulation at mm-wave frequencies is introduced utilizing a switching Class-E amplifier topology. Section V highlights the effect of load pulling in a digital PA on Class-E amplifier performance and the resultant system efficiency at backed-off power levels. Section VI discusses a transmission line structure capable of changing its characteristic impedance and its utility in maintaining optimum impedance to the unit Class-E amplifiers under load pulling in the digital PA. Section VII describes the eight-way combined Watt-level digital PA and the operation of the proposed dynamic load modulation network using variable characteristic impedance transmission lines. The proof of concept prototype implementation details and measurement results are covered in Section VIII. Section IX concludes this paper.

## II. MULTISTAGE CLASS-E AMPLIFIER CHAIN

Switching amplifiers such as Class-E [Fig. 1(a)] [7] enable highly efficient power amplification by ensuring nonoverlapping collector voltage and current waveforms. This is true even at mm-wave frequencies as evident from the reported mm-wave Class-E PAs [10], [12] with higher PAE than mm-wave linear Class-A, Class-AB amplifiers [13]. Other switching amplifiers, such as Class-D and inverse Class-D amplifiers, have also been demonstrated in recent years [8], [9]. However, realizing Class-D amplifiers

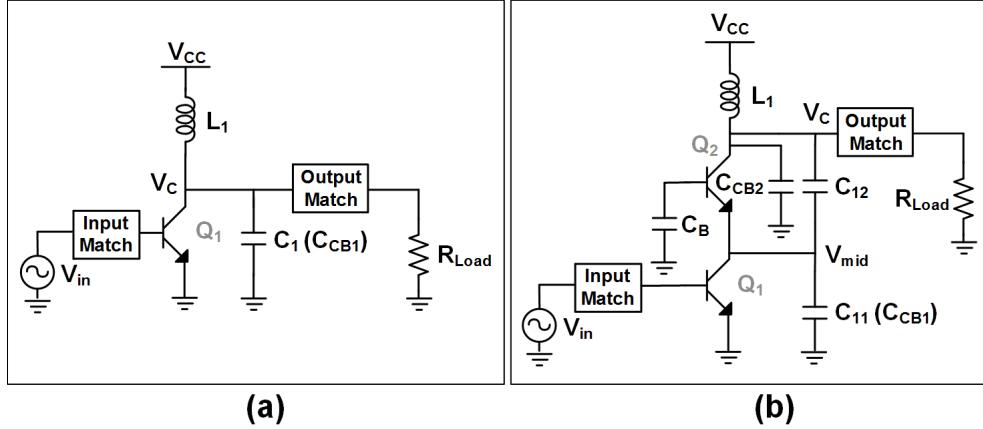


Fig. 1. Simplified schematic of (a) mm-wave Class-E PA and (b) mm-wave double-stacked Class-E PA.

TABLE I  
TECHNOLOGY PARAMETERS FOR SOME REPRESENTATIVE SiGe HBT PROCESSES

Technology	HBT	$BV_{CEO}$ (V)	$BV_{CBO}$ (V)	Peak $f_T$ (GHz)	$J_c$ Peak $f_T$ (mA/ $\mu m^2$ )	Peak $f_{max}$ (GHz)	$J_c$ Peak $f_{max}$ (mA/ $\mu m^2$ )	$\tau_{in}$ (ps)	$\tau_{out}$ (ps)	$G_{in}$ ( $pF/\mu m^2$ )	$C_{out}$ ( $fF/\mu m^2$ )	$\alpha$ ( $C_{in}/C_{out}$ )	$I_{dc,Q}$ (mA/ $\mu m^2$ ) ( $V_B = 0.75$ V)
0.25 $\mu m$ 7WL	High $f_T$	3.3	11	60	3.5	100	3.5	22	0.53	0.68	4	172	0.035
0.13 $\mu m$ 8HP	High $f_T$	1.7	5.9	220	14	280	12.5	8	0.22	0.325	9.76	33.3	0.07
	High BV	3.55	12	60	1.4	120	1.2	18	1.6	0.68	9.76	69	0.035
90 nm 9HP	High $f_T$	1.5	5.3	300	20	350	20	5	0.1	0.4	12	33.3	0.22

are difficult in SiGe process due to the absence of fast p-n-p transistors. The presence of the parasitic collector/drain-to-bulk capacitors of the transistors also distorts the Class-D waveforms resulting in efficiency degradation. Inverse Class-D amplifiers, on the other hand, require a differential implementation necessitating a balun at the output, which results in additional loss. In contrast, Class-E amplifiers can be realized using SiGe HBTs in a single-ended implementation, although Class-E design requires more precise matching networks as the collector voltage can swing  $\sim 3$  times the supply voltage. The parasitic collector-bulk capacitors of the transistors can also be incorporated into the Class-E load-line, preserving the Class-E nonoverlapping voltage-current waveforms for achieving high efficiency [7]. Another important advantage of switching Class-E amplifiers especially in SiGe HBT processes is the higher achievable breakdown voltage  $BV_{CBO}$  compared with the nominal  $BV_{CEO}$  breakdown voltage limit. Since the avalanche breakdown mechanism in bipolar transistor depends on the collector current density [14], the low collector current density during high voltage swing in the Class-E cycle allows the SiGe HBTs to tolerate voltages up to  $BV_{CBO} = 6$  V compared with 1.8 V nominal breakdown voltage, and thus enables the generation of high power with high efficiency at mm-wave frequencies [5].

The mm-wave Class-E design equations have been extensively analyzed in [5] to provide PA performance metrics, such as output power  $P_{out}$ , power gain  $G_P$ , collector efficiency  $\eta$  and PAE versus frequency of operation  $\omega$ , and load termination  $R_{Load}$  in terms of process technology parameters, such as

breakdown voltage  $BV_{CBO}$ , input time constant  $\tau_{in}$ , and output time constant  $\tau_{out}$ . For convenience, the Class-E performance limit equations from [5] are repeated here

$$\left\{ \begin{array}{l} P_{out,max} = \frac{1}{2} \frac{BV_{CBO}^2}{R_{Load}} \psi^2 \approx \frac{BV_{CBO}^2}{9.75 R_{Load}} \\ \eta_{max} = \frac{1}{1 + \chi \times \omega \times \tau_{out}} \approx \frac{1}{1 + 4.6 \times \omega \tau_{out}} \\ G_{P,max} = \left[ \frac{1}{\omega} \right] \left[ \frac{BV_{CBO}^2}{\tau_{in} \alpha} \right] \left[ \frac{\psi^2}{K_C(q_{max}) V_T^2} \right] \\ \times \left[ \ln(BV_{CBO}) + \ln(\omega) + \ln(K_{ClassE}) + \ln \left( \frac{C_1/\mu m^2}{I_{dc,Q}/\mu m^2} \right) \right]^{-2} \\ PAE_{max} = \left( 1 - \frac{1}{G_{P,max}} \right) * \eta_{max}. \end{array} \right. \quad (1)$$

where  $V_T = 0.025$  V,  $\psi \approx 0.453$ ,  $\chi \approx 0.1267$ ,  $K_C(q_{max}) \approx 0.6765$ , and  $K_{ClassE} \approx 1.484$  are the constants introduced in [5], and remaining terms are the technology parameters shown in Table I.

For the 0.13- $\mu m$  SiGe BiCMOS process used for generating Watt-level power in this paper, the process technology parameters shown in Table I can be used to further simplify the Class-E PA performance metrics of (1) and express the performance metrics as a function of only circuit parameters, such as  $R_{Load}$  and operational frequency in radians  $\omega$ . The simplified performance metrics for a single-stage Class-E PA [5] are then

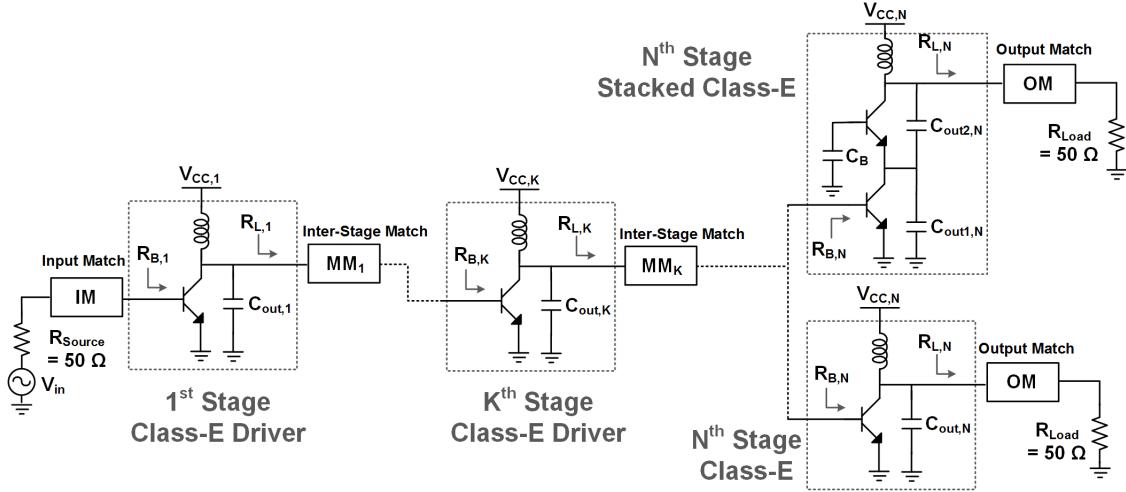


Fig. 2.  $N$ -stage mm-wave Class-E amplifier chain with either a nonstacked Class-E or a stacked Class-E as the output stage.

given as

$$\left\{ \begin{array}{l} P_{\text{out,max}}^{\text{Class-E}} = \frac{3.7}{R_{\text{Load}}} \\ \eta_{\max}^{\text{Class-E}} = \frac{1}{1 + 10^{-12} \times \omega} \\ G_{P,\max}^{\text{Class-E}} = \frac{65.5 \times 10^{12}}{\omega [\ln(\omega) - 20.5]^2} \\ \text{PAE}_{\max}^{\text{Class-E}} = \left(1 - \frac{1}{G_{P,\max}^{\text{Class-E}}}\right) * \eta_{\max}^{\text{Class-E}}. \end{array} \right. \quad (2)$$

At 45 GHz, using ideal passive components for input and output matching network, this translates into  $G_{P,\max} = 8$  dB,  $\eta_{\max} = 78\%$ , and maximum achievable  $\text{PAE}_{\max} = 67\%$ .

Stacking of transistors in a Class-E configuration [Fig. 1(b)] is another technique to increase both output power and power gain [5]. For mm-wave switching Class-E PAs, the stacked transistor configuration of Fig. 1(b) consists of SiGe HBT transistors that are connected in series with appropriately chosen capacitor values  $C_{12}$  and  $C_{B2}$ . During large-signal switching mode operation, the intrinsic HBT parasitics ( $C_{CB1,2}$  and base-emitter capacitors  $C_{CBE1,2}$  of  $Q_1$  and  $Q_2$ ) in conjunction with the added capacitors ( $C_{12}$  and  $C_{B2}$ ) ensure that each transistor operates within the 6 V  $\text{BV}_{\text{CBO}}$  breakdown limit while resulting in an increase of the overall breakdown voltage of the stacked transistor configuration. In the stacked Class-E architecture, the capacitor network  $C_{12} - C_{11}$  ensures that the collector voltage  $V_C$  is equally divided between the top and bottom HBTs  $Q_1 - Q_2$ , while the  $C_{B2} - C_{BE2}$  network ensures that the base-emitter voltage  $V_{BE2}$  of the stacked HBT  $Q_2$  swings in synchrony with the input swing  $V_{BE1}$  of the bottom HBT  $Q_1$ . Thus, the series-connected HBTs  $Q_1$  and  $Q_2$  operate as a single switch but with twice the breakdown voltage and generate significant higher output power for the same output load  $R_{\text{Load}}$  compared with a nonstacked Class-E design. Since this increased output power can be obtained for almost the same input swing  $V_{\text{in}}$  to the base of the bottom HBT  $Q_1$ , a stacked Class-E architecture can achieve higher power gain as well leading to improvement in PAE for larger output power levels. The stacked Class-E architecture and its

merits and demerits vis-a-vis a nonstacked Class-E design at mm-waves have been extensively studied as well in [5]. For the current design objective, the stacked Class-E performance limits can be similarly simplified [as in (2) for the nonstacked Class-E PA] by using the technology parameters of the 0.13- $\mu\text{m}$  SiGe BiCMOS process. The simplified performance metrics for the double-stacked single-stage Class-E design in the 0.13- $\mu\text{m}$  SiGe BiCMOS process are given by

$$\left\{ \begin{array}{l} P_{\text{out,max}}^{\text{Stacked Class-E}} = \frac{1}{(1 - \gamma)^2} P_{\text{out,max}}^{\text{Class-E}} \\ \eta_{\max}^{\text{Stacked Class-E}} = \frac{1}{1 + 2 \times 10^{-12} \times \omega} \\ G_{P,\max}^{\text{Stacked Class-E}} = \frac{65.5 \times 10^{12}}{\omega (1 - \gamma)^2 [\ln(\omega) - 20.5 - \ln(1 - \gamma)]^2} \\ \text{PAE}_{\max}^{\text{Stacked Class-E}} = \left(1 - \frac{1}{G_{P,\max}^{\text{Stacked Class-E}}}\right) * \eta_{\max}^{\text{Stacked Class-E}}. \end{array} \right. \quad (3)$$

At 45 GHz,  $\gamma = ((V_{\text{mid}})/V_c) \approx 0.33$  [5] leading to 3.5-dB output power improvement over a nonstacked Class-E design with  $G_{P,\max} = 11.3$  dB,  $\eta_{\max} = 64\%$ , and  $\text{PAE}_{\max} = 59\%$ . Assuming  $R_{\text{Load}} = 50 \Omega$ , the calculated maximum output power of the Class-E and the double-stacked Class-E amplifiers are around 18.7 and 22.2 dBm, respectively.

For Watt-level power generation with moderate passive power combining on a single chip, several of these 20–23 dBm unit Class-E amplifiers must be power combined. To enable sufficient gain for the entire power combined system, the single-stage Class-E and stacked Class-E PAs need to be cascaded with Class-E driver amplifiers. For a multistage Class-E amplifier chain, the losses in the input matching, output matching, and interstage matching network with finite quality factor passive component become significant. Fig. 2 shows the schematic of an  $N$ -stage mm-wave Class-E amplifier chain with the  $K$ th stage amplifier metrics denoted as load resistance  $R_{L,K}$ , input resistance  $R_{B,K}$ , output power  $P_{\text{out},K}$ , and input power  $P_{\text{in},K}$ . The efficiency of the matching networks is denoted as  $OM$  for the final-stage

output matching network,  $IM$  for the first-stage input matching network, and  $MM_K$  for the  $K$ th interstage matching network. The performance metrics of the  $N$ -stage Class-E amplifier chain shown in Fig. 2 can be summarized as in (4), as shown at the bottom of this page.

When the final output-stage amplifier is a stacked Class-E PA driven by “ $N-1$ ” nonstacked Class-E driver stages (Fig. 2), the performance metric for that amplifier chain configuration can be similarly summarized as in (5), as shown at the bottom of this page.

In both the cases, the two-element matching network efficiency expressions are given by [15]

$$\left\{ \begin{array}{l} OM = \frac{1}{1 + \frac{2}{Q_{\text{Passive}}} \sqrt{\frac{R_{\text{Load}}}{R_{L,N}}} - 1} \\ MM_{K:K \in 1:N-1} = \frac{1}{1 + \frac{2}{Q_{\text{Passive}}} \sqrt{\frac{R_{L,K}}{R_{B,K+1}}} - 1} \\ IM = \frac{1}{1 + \frac{2}{Q_{\text{Passive}}} \sqrt{\frac{R_{\text{Source}}}{R_{B,1}}} - 1} \end{array} \right. \quad (6)$$

The aforementioned expressions, assuming a realizable passive quality factor  $Q_{\text{Passive}} \approx 15$  at 45 GHz, are used to plot the performance metrics of a three-stage PA chain both with a nonstacked Class-E and a stacked Class-E output stage at 45 GHz for different values of final-stage load resistance  $R_{L,3}$  [Fig. 3(a)]. It can be observed that even though the individual collector efficiency (64%) of the stacked Class-E amplifier is lower than that of a nonstacked Class-E design (78%) at 45 GHz, the 3.5-dB power improvement in a stacked design enables the stacked Class-E amplifier chain configuration to achieve better PAE for the same output power levels above 20 dBm compared with a nonstacked Class-E amplifier chain. The PAE for the stacked Class-E PA peaks around 22 dBm, since the output load is 50 Ω and there is no output matching loss for this power level. For all the other power levels, the output load needs to be either upconverted or downconverted from 50 Ω leading to additional loss in the output matching network and thus lower efficiency and PAE.

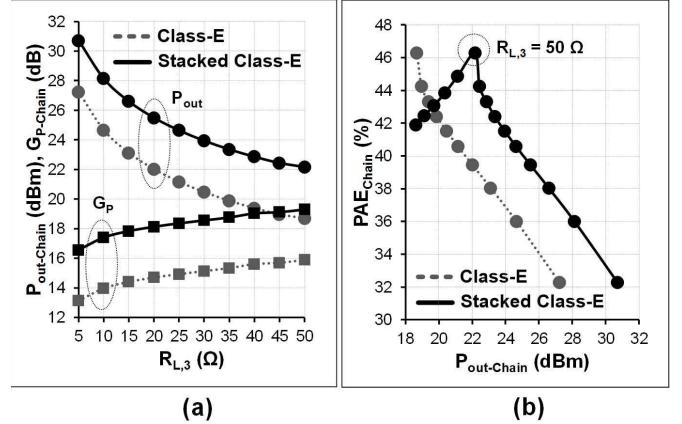


Fig. 3. (a) Maximum achievable output power ( $P_{\text{out}}$ ) and power gain ( $G_P$ ) in a 45-GHz three-stage Class-E PA chain versus load resistance of the output stage ( $R_{L,3}$ ). (b) Maximum achievable PAE versus  $P_{\text{out}}$  of the three-stage Class-E amplifier chain.

In Section III, for Watt-level power generation at mm-wave frequencies, the maximum achievable system performance by passive power combining of the stacked Class-E amplifier chains will be discussed.

### III. WATT-LEVEL mm-WAVE POWER COMBINING

In recent years, various power combining schemes have been reported in the literature for achieving higher output power by power-combining [17], voltage-combining [18], and current-combining [2]. Historically, transmission lines have been used for realizing power-combining networks in mm-wave frequencies, but in recent years, transformer combiners have also been used for area reduction [18]. The mm-wave spatial power-combining using multiple on-chip antennas has also been reported to achieve high output power [20]. However, in this paper, the design methodology for realizing a Watt-level digital PA has been studied, where several independently controlled Class-E amplifier chains of Section II would be to achieve Watt-level power at mm-wave frequencies. In such a scheme, power control is achieved

$$\left\{ \begin{array}{l} P_{\text{out,max}}^{\text{N-Stage}} = OM \times P_{\text{out,max}}^{\text{Class-E}} \\ G_{P,\text{max}}^{\text{N-Stage}} = [G_{P,\text{max}}^{\text{Class-E}}]^N \times OM \times IM \times MM_{N-1} \times MM_{N-2} \times \dots \times MM_2 \\ \eta_{\text{max}}^{\text{N-Stage}} = \frac{\eta_{\text{max}}^{\text{Class-E}} \times OM}{1 + \frac{1}{[G_{P,\text{max}}^{\text{Class-E}}] \times MM_{N-1}} + \frac{1}{[G_{P,\text{max}}^{\text{Class-E}}]^2 \times MM_{N-1} \times MM_{N-2}} + \dots + \frac{1}{[G_{P,\text{max}}^{\text{Class-E}}]^N \times MM_{N-1} \times MM_{N-2} \times \dots \times MM_2}} \end{array} \right. \quad (4)$$

$$\left\{ \begin{array}{l} PAE_{\text{max}}^{\text{N-Stage}} = \left( 1 - \frac{1}{G_{P,\text{max}}^{\text{N-Stage}}} \right) \times \eta_{\text{max}}^{\text{N-Stage}} \\ P_{\text{out,max}}^{\text{N-Stage}} = OM \times P_{\text{out,max}}^{\text{Stacked Class-E}} \\ G_{P,\text{max}}^{\text{N-Stage}} = [G_P^{\text{Stacked Class-E}}]^N \times [G_P^{\text{Class-E}}]^{N-1} \times OM \times IM \times MM_{N-1} \times MM_{N-2} \times \dots \times MM_2 \\ \eta_{\text{max}}^{\text{N-Stage}} = \frac{\eta_{\text{max}}^{\text{Stacked Class-E}} \times OM}{1 + \frac{\eta_{\text{max}}^{\text{Class-E}} \times [G_{P,\text{max}}^{\text{Stacked Class-E}} \times G_{P,\text{max}}^{\text{Class-E}}] \times MM_{N-1}}{\eta_{\text{max}}^{\text{Stacked Class-E}} \times [G_{P,\text{max}}^{\text{Stacked Class-E}}]^2 \times [G_{P,\text{max}}^{\text{Class-E}}]^{N-1} \times MM_{N-1} \times MM_{N-2} \times \dots \times MM_2}} \end{array} \right. \quad (5)$$

$$\left\{ \begin{array}{l} PAE_{\text{max}}^{\text{N-Stage}} = \left( 1 - \frac{1}{G_{P,\text{max}}^{\text{N-Stage}}} \right) \times \eta_{\text{max}}^{\text{N-Stage}} \end{array} \right.$$

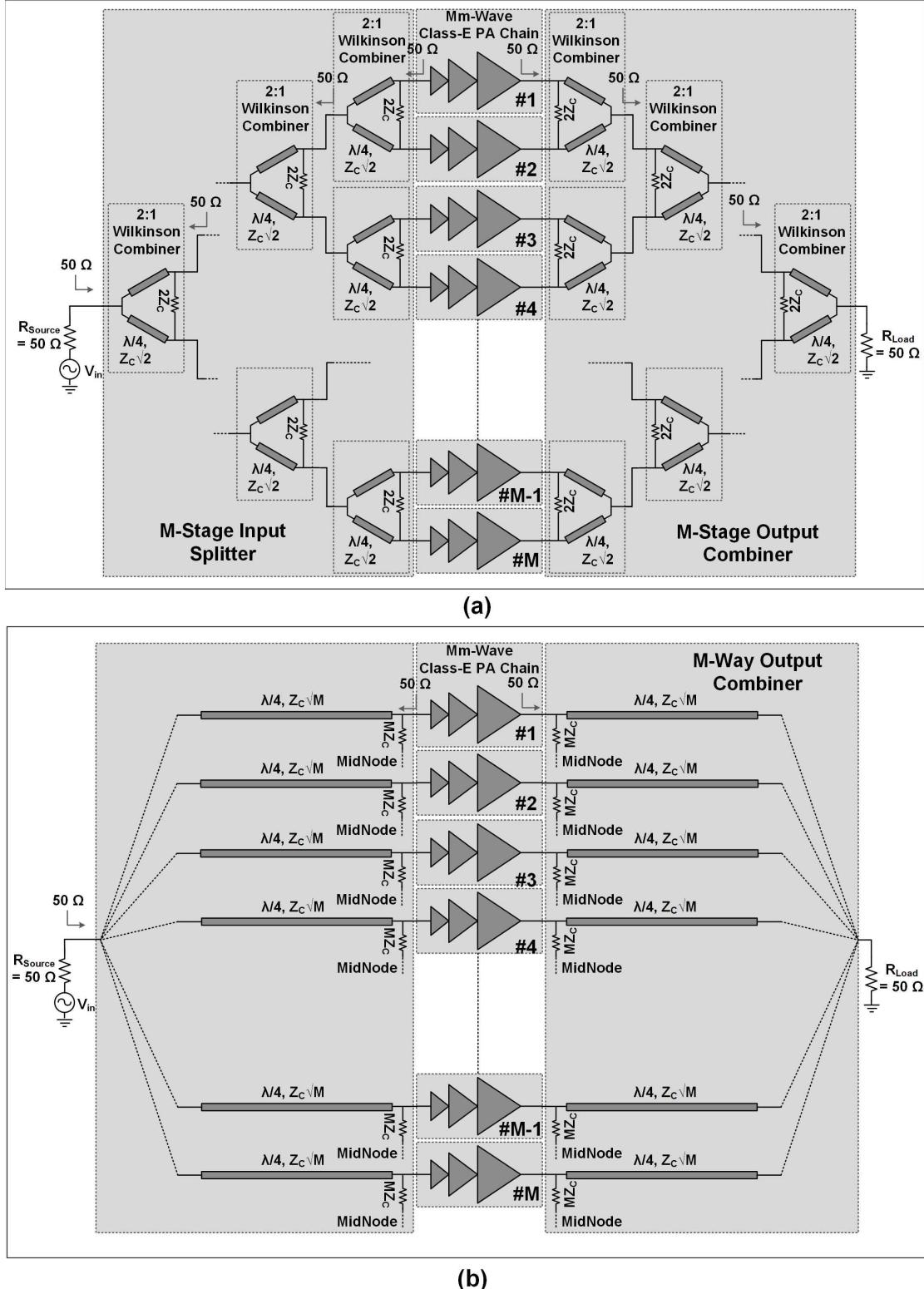


Fig. 4. (a)  $M$ -stage power combining of  $M$  mm-wave Class-E PA chains using two-way 50- $\Omega$  Wilkinson combiners. (b) Power combining of  $M$  mm-wave Class-E PA Chains using an  $M$ -way 50- $\Omega$  Wilkinson combiner.

by changing the number of active power-combined amplifier chains to realize different output amplitude levels. In such an architecture, isolating the active unit PA units from the inactive ones is critical to maintaining performance at different amplitude levels. In such a scenario, transform-combined

power-combining schemes suffer from additional conduction loss in the inactive windings apart from low isolation between active and inactive PA modules. Spatially power-combined systems enjoy excellent isolation; however, the low efficiency of the on-chip antennas [21] as well the large area

requirement for multiple on-chip antennas to achieve multi-level output amplitude are significant drawbacks. On the other hand, quarter wavelength ( $\lambda/4$ ) transmission line segments are especially useful in preventing load pulling in digital PAs by isolating the different unit PAs, as will be discussed in Section VII. Hence, the power combining structures considered in this section are limited to isolating transmission line quarter wavelength ( $\lambda/4$ ) power combiners. In this section, the power combining efficiency of a corporate  $M$ -stage Wilkinson power-combiner architecture [Fig. 4(a)] [15] is compared with that of an  $M$ -way Wilkinson power-combiner [Fig. 4(b)]. For ease of comparison, each power combiner structure is assumed to be designed for 50- $\Omega$  input and output impedance and as such can be directly used by the 50- $\Omega$  input-output Class-E amplifier chains discussed previously. For the 50- $\Omega$  input-output binary Wilkinson combiner architecture in Fig. 4(a),  $2^{M-1}$  two-way 50- $\Omega$  Wilkinson power combiners, each with  $70 \Omega$   $\lambda/4$  microstrip transmission lines, are used. The simulated insertion loss for a 70- $\Omega$  on-chip microstrip transmission line versus frequency is shown in Fig. 5. Fig. 6(b) shows the estimated power combining loss of the  $M$ -stage Wilkinson power combiner as the combining ratio is varied from 1 to 16. For the  $M$ -way Wilkinson power-combiner,  $M$  transmission line segments each with transmission line characteristic impedance  $Z_C = 50\sqrt{M} \lambda/4$  must be used. Fig. 6(a) shows the insertion loss of the  $\lambda/4$  microstrip transmission line for different values of characteristic impedance  $Z_C$  at 45 GHz. It can be observed that for the signal and ground plane metal options chosen in Fig. 5(a), the insertion loss of the quarter wavelength segment of the transmission line increases with higher impedance, as thinner metal traces need to be used to realize higher  $Z_C$ . Fig. 6(b) shows the insertion loss comparison of the corporate  $M$ -stage Wilkinson combiner with the  $M$ -way Wilkinson combiner at 45 GHz. It can be observed that while for moderate combining  $< 4:1$  combining, the  $M$ -way combiner seems to have better power-combining efficiency; for higher combining ratios, the high insertion loss of high  $Z_C$  transmission lines makes  $M$ -stage corporate combiners a more amenable solution. Interestingly, as shown in Fig. 6(b), a hybrid solution of two-way and four-way combiners [Fig. 7(a)] offers the lowest insertion loss for eight-way power combining. This observation has been used to design the prototype Watt-level mm-wave digital PA in Section VIII. Likewise, a cascaded connection of four-way combiners [Fig. 7(b)] results in a lower insertion loss, compared with the aforementioned approaches, for 16-way power combining. The overall system output power  $P_{out}$  and PAE of a 1-W power combined system is shown in Fig. 6(c), including the calculated efficiencies of Class-E amplifier chains and power combiners. It can be observed that while smaller output power Class-E PA chains were previously shown to have higher efficiency, after including the combiner loss, the overall PAE for one-way to eight-way combined systems remains nearly constant at 34%. Beyond 16:1 combined systems, the overall PAE drops as the power combiner loss becomes dominant.

Even though, from the preceding analysis, a single noncombined 1-W Class-E PA chain results in the same performance

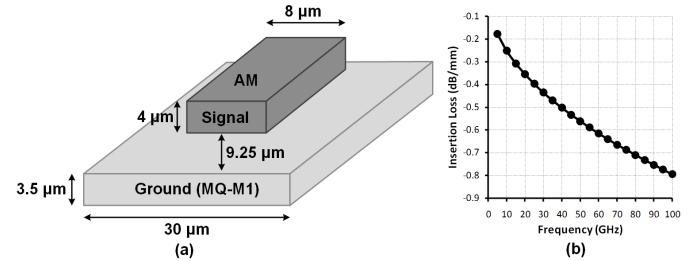


Fig. 5. (a) 70- $\Omega$  microstrip transmission implemented in the  $0.13\text{-}\mu\text{m}$  SiGe BiCMOS process. (b) Insertion loss of the 70- $\Omega$  microstrip transmission line versus frequency.

as a eight-way combined system, there are several reasons for preferring an eight-way distributed Watt-level power generation. First, a single Watt-level Class-E PA chain requires very large SiGe HBT transistors for the final output stage. The large collector-base capacitances of these large HBTs reduce the reverse isolation significantly and lead to stability concerns. For practical implementations, small- and large-signal stabilities of such large transistors are usually mitigated by resistive ballasting at the base. Since the base resistance  $R_B$  of these large transistors is very small, any base ballasting further reduces the power gain of the stage and leads to further degradation of the PAE. Second, since for the Class-E amplifier chains,  $R_B$  of the final output stage needs to matched to  $R_L$  of the previous stage using interstage matching, the very small  $R_B$  of the  $>27$  dBm unit output stages makes the interstage networks extremely narrowband. An overall narrow-band response of the PA chains is not suitable for the mm-wave high data rate transmitter applications with requirement of several gigahertz of  $P_{-1 \text{ dB}}$  bandwidth. Finally and most importantly, in this paper, a Watt-level digital PA architecture is discussed with several levels of independent amplitude control. As explained in detail in Section V, this is achieved by independently controlling each unit Class-E amplifier chains to turn on and off. For improved linearity of the digital PA, it is better to have larger number of independently controlled amplifier chains. However, keeping in mind the aforementioned tradeoffs, an 8:1 power combined mm-wave PA has been chosen for implementation.

#### IV. mm-WAVE CLASS-E POWER MODULATOR

High-speed data transmission at mm-wave frequencies is usually achieved by using quadrature amplitude modulation (QAM) schemes in linear mm-wave PAs [16]. However, the low efficiency of mm-wave linear PAs at both peak and backed-off power levels under QAM modulation significantly degrades the overall transmitter efficiency. In recent years, research has focused mm-wave digital polar transmitters (DPTs) for achieving high transmitter efficiency while supporting several gigabits per second of data rate at mm-wave frequencies [4], [23]. A simplified mm-wave DPT architecture is shown in Fig. 8. In an mm-wave DPT, the baseband QAM information is separated into amplitude and phase information using a Cartesian-to-polar digital scheme. The separated phase information is then first phase modulated into the mm-wave carrier frequency by a phase modulator before it can be transmitted by the highly efficient mm-wave

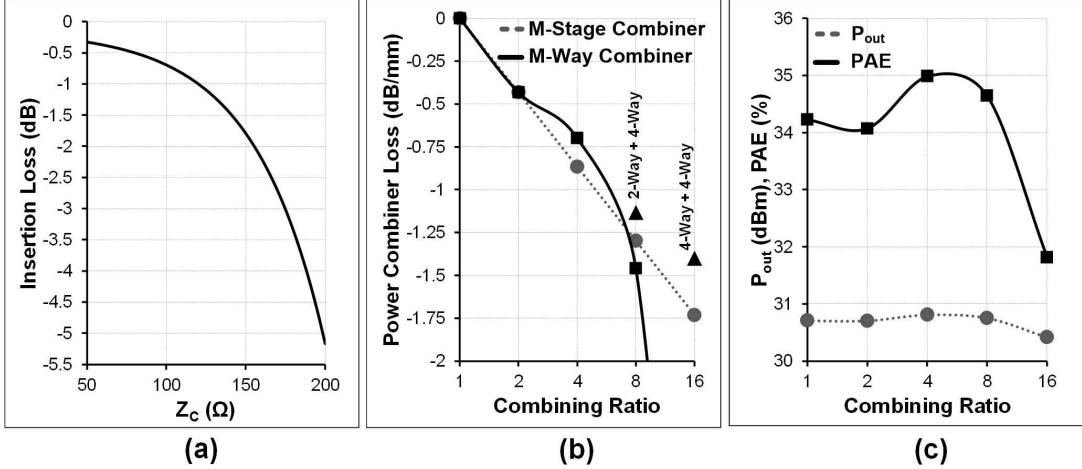


Fig. 6. (a) Insertion loss of quarter wavelength microstrip transmission line at 45-GHz versus transmission line characteristic impedance ( $Z_C$ ). (b) Power combiner loss for different combining ratios using  $M$ -stage or  $M$ -way or a hybrid combiner architecture. (c) Overall  $P_{out}$  and PAE for the power combined 1-W mm-wave Class-E PA.

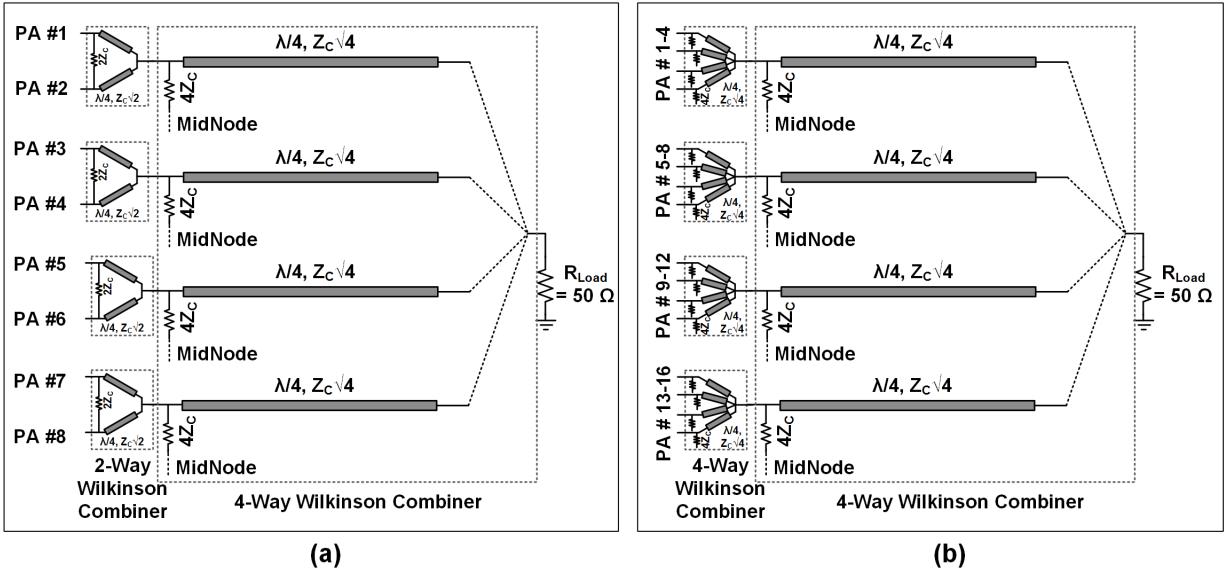


Fig. 7. (a) Eight-way combiner comprising of two-way and four-way Wilkinson combiner. (b) 16-way combiner comprising of four-way and four-way Wilkinson combiner.

Class-E PAs discussed previously using constant envelope phase modulation. To support QAM modulation, the amplitude information is utilized to control how many of the phase-modulated Class-E PAs need to be activated, so that the overall power-combined phase-modulated output amplitude also tracks the baseband QAM input. Needless to say, the most important blocks of a DPT scheme are the mm-wave Class-E amplifier chains capable of turning on-off fast to support high data rates while still generating  $\approx 23$ -dBm output power for Watt-level peak output power. These 1-b mm-wave Class-E “power modulators” [22] are discussed in this section, while the issues with power combining these fast switching modulators are discussed in Section V.

The operation of the Class-E power modulator architecture relies on the switching nature of the Class-E  $P_{out} - P_{in}$  transfer curve. As shown in Fig. 9(a), if the input power to a stacked Class-E unit PA can be attenuated by 10 dB, the

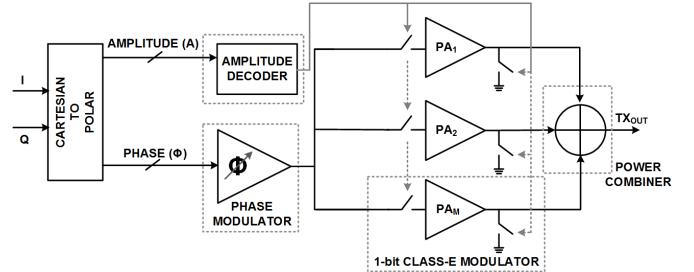


Fig. 8. Simplified schematic of an mm-wave DPT.

output power drops by  $\approx 40$  dB, effectively shutting down that particular Class-E amplifier chain in a power-combined system. A Class-E PA chain comprising of cascade of several such Class-E amplifiers has an even sharper  $P_{out} - P_{in}$  transfer curve, similar to a digital inverter. More importantly, as shown

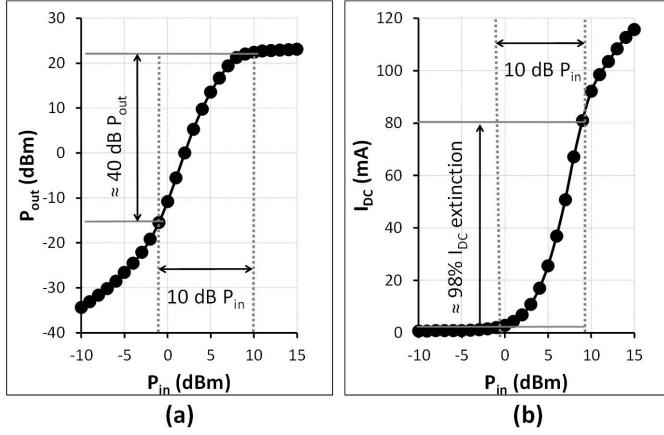


Fig. 9. Large-signal transfer curves of mm-wave stacked Class-E amplifiers. (a)  $P_{out}$  versus  $P_{in}$ . (b)  $I_{dc}$  versus  $P_{in}$ .

in Fig. 9(b), since the dc current consumption under large-signal operation in a Class-E sharply tracks the output power generation, when the mm-wave Class-E PAs are shut down by input power attenuation, the dc current drawn from the supply becomes negligible. The  $I_{dc,\text{Quiescent}} \approx 0$  feature is extremely important in maintaining high average efficiency in a DPT, as no dc power is dissipated in any amplifier chains when it is not generating power. In contrast, linear mm-wave amplifiers with significant quiescent current biasing need to have supply switching schemes for application in a DPT architecture. Supply switching schemes not only lead to efficiency degradation due to the presence of switch ON-resistance on the collector current path, but also dissipate large amount of digital power, when the large supply switches need to be modulated at a higher speed [24]. In comparison, the small switches used at the input of the Class-E amplifiers only marginally degrade the power gain of the system and dissipate less digital power under high-speed switching.

Fig. 10(a) shows a simplified schematic of the input-modulated Class-E power modulator, while a detailed schematic, including several features for enhanced operation at mm-wave frequencies, is highlighted in Fig. 10(b). The design of the series input switch network [Fig. 11(a)] is important in realizing high modulation, low insertion loss in the ON-state, and high signal isolation in the OFF-state. In particular, the isolation of the series input switch ( $M_{IN-SW1}$ ) is enhanced by resonating out the OFF capacitance by using a shunt inductance  $L_{parallel} = 60$  pH. The enhancement of isolation in the frequency band of interest is shown in Fig. 11(b). The size of the series input switch  $M_{IN-SW1}$  also needs to be carefully chosen to ensure good tradeoff between insertion loss and isolation. A 250- $\mu$ m finger width is chosen based on the 1.2 dB of insertion loss when the series switch is ON and at least 20 dB of signal isolation when the series switch is OFF, as shown in Fig. 11(b). A shunt complementary switch  $M_{IN-SW2}$  ensures that the input matching is always maintained under modulation. To enhance the extinction ratio of the ON-to-OFF amplitudes, a stacked switch scheme implemented using thick-oxide MOSFETs is used to further attenuate the output amplitude during the OFF-state, as shown in Fig. 12(a).

Choosing the right MOSFET sizes for the output switches is also an important design criterion in the isolation versus insertion loss tradeoff, as shown in Fig. 12(b). Output stacked switches, each of total size 100- $\mu$ m finger width is chosen to ensure 6–7-dB additional extinction ratio at the cost of 0.7-dB insertion loss. A high ON/OFF extinction ratio is needed to ensure proper identification of “1” and “0” bit in a 1-b modulation. In the presence of any intersymbol interference and other nonidealities, a higher ON/OFF extinction ratio results in better eye-diagram [and bit error rate (BER)] in a 1-b ASK modulation. The quality and BER of an 1-b ASK modulation is determined by a quantity known as “quality factor” defined as  $Q = ((|\mu_1 - \mu_0|)/(\sigma_1 - \sigma_0))$ , where  $\mu_1$  and  $\mu_0$  are the average values of the “1” and “0” bit levels and  $\sigma_1$  and  $\sigma_0$  are the standard deviations of the “1” and “0” bit levels due to bit transmission nonidealities [25]. The BER for 1-b ASK modulation is given by  $BER = 0.5 \times \text{erfc}(Q/\sqrt{2})$  [25]. A higher ON/OFF extinction ratio ensures a much larger  $\mu_1 - \mu_0$  and thus higher  $Q$ -factor and better BER for the same  $\sigma_1 - \sigma_0$  transmission nonidealities. For achieving BER of  $10^{-12}$  or better,  $Q$ -factor  $\approx 7$ , requiring the extinction ratio to approach 40 dB [25].

The ON- and OFF-state equivalent circuits for the mm-wave Class-E power modulator are shown in Fig. 13, while the simulated transient waveforms under 1-b ASK modulation at 1 Gb/s are shown in Fig. 14. The 1-b Class-E power modulator implementation details and measurement results are discussed in Section VIII.

## V. LOAD PULLING IN CLASS-E

To realize an mm-wave Watt-level digital PA with several levels of output amplitude, several of the 1-b Class-E power modulators can be power combined using the  $M$ -way combiner schemes discussed in Section III. However, since each of the Class-E PA chains in this power-combined system needs to be independently turned on-off to realize the discrete output amplitudes, the common mode resistors in the  $M$ -stage corporate Wilkinson combiner or the  $M$ -way  $\lambda/4$  Wilkinson need to be removed as otherwise they will dissipate a significant portion of the generated power during the unbalanced combining modes during amplitude modulation. One such power combining scheme was demonstrated in [2], where eight Class-E PAs were power combined using a  $\lambda/4$  combining scheme, as shown in Fig. 15. In this approach, power back-off is achieved by switching OFF some of the unit PA chains and then shorting those  $\lambda/4$  transmission line branches, so that active unit PAs are isolated from the inactive ones [Fig. 15(b)]. One major disadvantage of this scheme, however, is that, as the different Class-E PA chains/modulators are switched ON-OFF to realize different output amplitude levels, the impedance seen by the remaining active Class-E modulators will change as a function of the number of active PAs/output amplitude levels in a phenomenon known as “load pulling.” For example, the eight-way power-combined system in Fig. 15(a) is designed to present an optimum impedance  $Z_{OPT}$  to the unit PA chains for maximum PAE in the peak power generation mode. However, as some of them are turned

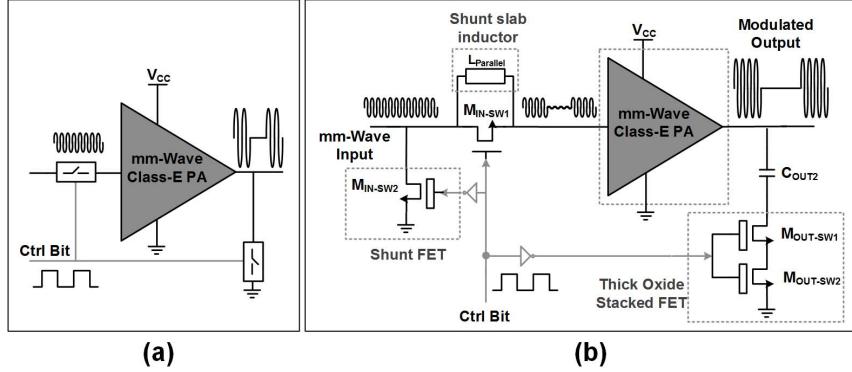


Fig. 10. (a) Simplified 1-b mm-wave Class-E modulator architecture. (b) Detailed mm-wave modulator schematic.

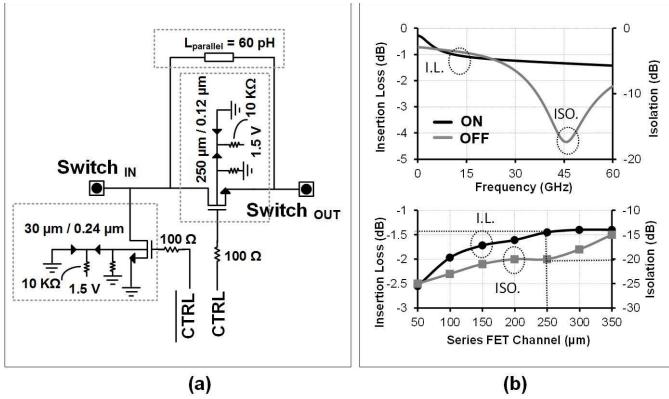


Fig. 11. (a) Input switch network schematic. (b) Isolation and insertion loss tradeoff versus frequency and  $M_{IN-SW1}$  switch size.

off to achieve power back-off in Fig. 15(b), the impedance seen by the remaining active PA chains becomes much larger than the previously designed  $Z_{OPT}$ . Specifically, as shown in Fig. 15(c), for an eight-way combined system, realized using  $\lambda/4$  transmission line combiners,  $Z_{PA}$  can scale from  $Z_{OPT}$  to  $8 \times Z_{OPT}$  leading to efficiency degradation. Fig. 16 shows the effect of changing impedance on a stacked Class-E output power and PAE. It can be observed that unless  $Z_{PA}$  under all switching configurations can be limited to  $0.6Z_{OPT}$  to  $1.5Z_{OPT}$ , there will be significant degradation in PAE at backed-off power levels and can even lead to catastrophic transistor breakdown because of nonoptimal load conditions.

## VI. VARIABLE CHARACTERISTIC IMPEDANCE TRANSMISSION LINES

One way to mitigate this ‘‘load pulling’’ problem in digital PAs is to design a ‘‘reconfigurable’’ power-combining network capable of automatically reoptimizing the impedance presented to the unit Class-E modulators ( $Z_{PA}$ ) back to  $Z_{OPT}$  as a function of output amplitude level. For the  $\lambda/4$  transmission line-based scheme discussed here, this is possible by engineering a variable characteristic impedance ( $Z_C$ ) transmission lines. Tunable transmission lines having variable phase shifts while maintaining a constant  $Z_C$  have been demonstrated before [26], [27]. However, the tunable transmission line structure shown in Fig. 17(a) addresses the converse problem

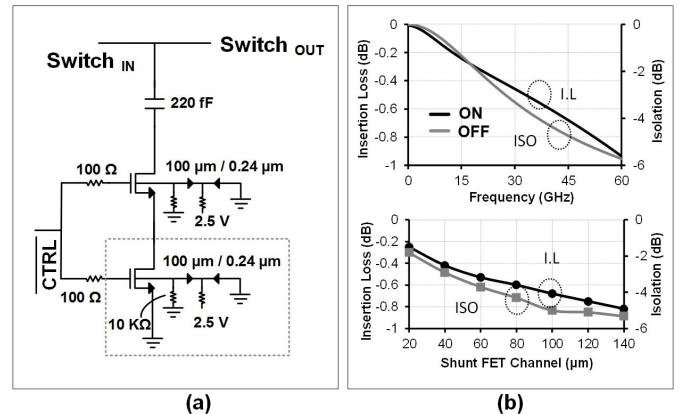


Fig. 12. (a) Output switch network schematic. (b) Isolation and insertion loss tradeoff versus frequency and  $M_{OUT-SW1,2}$  switch size.

of digitally controlling the characteristic impedance of the transmission lines while keeping a constant phase shift. In microstrip transmission line, the characteristic impedance is primarily controlled by the relative spacing of the signal and ground planes. Therefore, a microstrip with several switch-connected metal layers that are either connected to ground or floating can have variable characteristic impedance. Since the electrical length (phase shift) of the transmission line is only controlled by the dielectric constant of the silicon substrate, the isolating action of the  $\lambda/4$  transmission line combiners remains intact in this tunable transmission line structure. In this particular implementation of a dual-state transmission line [Fig. 17(a)], the thick top metal AM is used as the signal line and the stacked metals M1-MQ as the fixed ground plane. The metal layer LY is used as the floating plane digitally controlled by thick-oxide MOSFET switches to ensure voltage handling capability when used for power combining the unit Class-E modulator outputs. When the MOSFET switches are turned off, the LY layer is floating, giving a characteristic impedance of  $\approx 50 \Omega$ . However, when all the MOSFET switches are turned on simultaneously electrically shorting the LY layer to ground, the ground plane virtually moves, reducing the separation between the signal and ground plane and lowering the  $Z_C$  to  $\approx 35 \Omega$ , as shown in Fig. 18(b). Having a tunable transmission line comes at

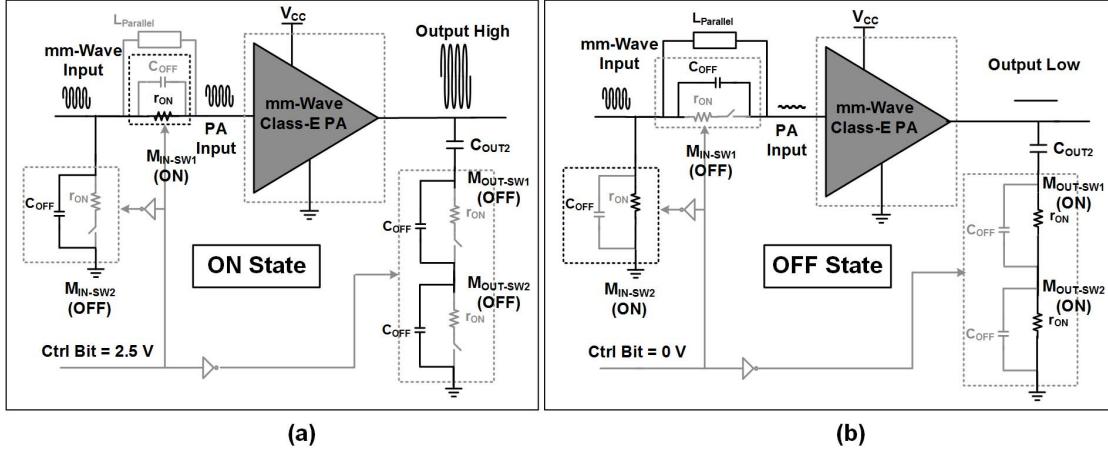


Fig. 13. 1-b Class-E modulator equivalent circuit. (a) ON-state. (b) OFF-state.

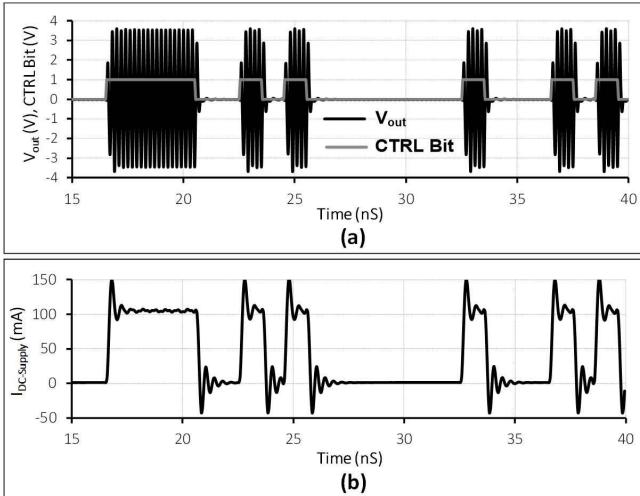


Fig. 14. Large-signal transient waveforms of the Class-E modulator. (a) Input control-bit and output voltage versus time. (b)  $I_{\text{dc-Supply}}$  versus time.

the cost of higher insertion loss in the low  $Z_C$  mode, as the ON-resistance of the MOSFET switches in the return path contributes to a larger attenuation constant, as shown in Fig. 18(c). These dual-state transmission lines have been used to realize a two-way  $\lambda/4$  transmission line combiner at 45 GHz (Fig. 19), which are used in the eight-way dynamic load modulation discussed in Section VII. Although more lossy, these tunable transmission lines improve system performance in power back-off significantly.

## VII. DYNAMIC LOAD MODULATION NETWORK IN mm-WAVE DIGITAL POWER AMPLIFIER

Transmission lines having variable characteristic impedance can be used for solving the “load pulling” problem in digital PAs by performing “dynamic load modulation.” The objective of dynamic load modulation is to ensure that as different numbers of unit PA modules are turned off in a digital PA, the impedance presented to the remaining active unit PAs ( $Z_{\text{PA}}$ ) remains close to  $Z_{\text{OPT}}$  to ensure high efficiency at power back-off. A hypothetical case where variable characteristic

impedance transmission lines can be used in an eight-way current combined system to achieve perfect dynamic load modulation is shown in Fig. 20. In order to achieve perfect dynamic load modulation in the eight-way combined system, i.e., to maintain  $Z_{\text{PA}} = Z_{\text{OPT}}$  irrespective of the number of unit PAs being turned off, it requires the variable characteristic impedance  $\lambda/4$  transmission lines to have eight distinct impedance states. In the peak power mode shown in Fig. 20(a), the dynamic load modulation system operates similar to fixed  $Z_C \lambda/4$  combining. At power back-off modes [Fig. 20(b)], however, as “ $m$ ” of the unit PA modules are turned off, to achieve dynamic load modulation, the characteristic impedance of the variable  $Z_C$  transmission line also needs to change proportionally. Thus, if the characteristic impedance  $Z_C$  of the variable impedance transmission line can change over eight distinct values, as shown in Fig. 20(c); then,  $Z_{\text{PA}}$  can be maintained constant to  $Z_{\text{OPT}}$ .

Practical implementations of low-loss variable  $Z_C$  transmission lines having multiple characteristic impedance value using a similar structure, as in Section VI, are difficult due to the unavailability of enough thick metals in silicon processes. However, the dual-mode transmission line introduced in Section VI can still be used to perform dynamic load modulation in an eight-way combined system by modifying the power combining architecture, as shown in Fig. 21. In this architecture, the dual-mode transmission line-based two-way  $\lambda/4$  combiner is used in conjunction with a 4:1 slow wave  $\lambda/4$  combiner to realize an eight-way dynamic load modulation network, as shown in Fig. 21. The dual-mode transmission lines can only switch between “high  $Z_C$ ” mode and “low  $Z_C$ ” mode (instead of eight distinct impedance modes). Thus, the operating mode of the tunable transmission line combiner (low  $Z_C$  or high  $Z_C$  mode) needs to be correctly synchronized with the order, in which the eight unit PA modules needs to be turned on/off, as shown in Fig. 22. The combination of the dual-mode  $Z_C$  variation along with Class-E modulator ON/OFF algorithm ensures that the impedance seen by the active unit PAs ( $Z_{\text{PA}}$ ) always remains close to  $Z_{\text{OPT}}$  irrespective of the switching states [Fig. 21(c)]. The order in which the unit PA modules are turned on/off in the Watt-level digital

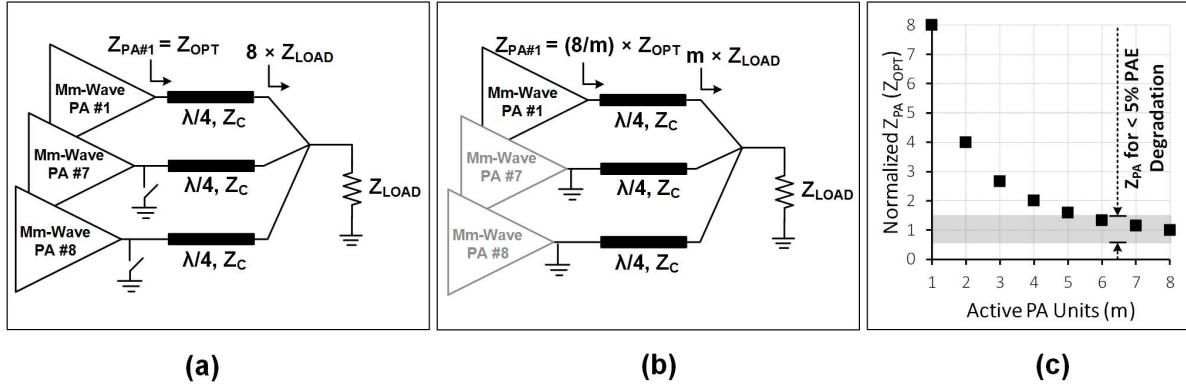


Fig. 15. Load modulation in an eight-way current combined PA with fixed  $Z_C$   $\lambda/4$  transmission lines under power back-off. (a) Peak power operation. (b) Power back-off operation when  $m$  out of eight unit PAs are active. (c) Variation of  $Z_{PA}$  with power back-off.

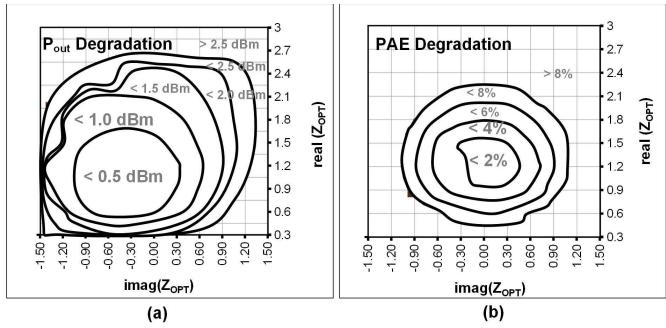


Fig. 16. Performance of mm-wave stacked Class-E amplifier under load pulling. (a) Variation of  $P_{out}$  with  $Z_{OPT}$ . (b) Variation of PAE with  $Z_{OPT}$ .

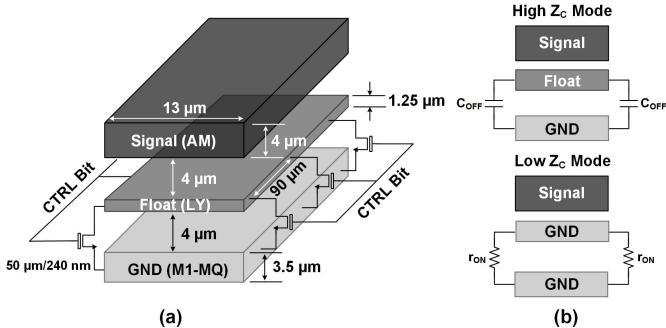


Fig. 17. Variable characteristic impedance ( $Z_C$ ) microstrip transmission line. (a) Proposed architecture. (b) Equivalent model in the “high  $Z_C$ ” and “low  $Z_C$ ” mode of operation.

PA along with the “high  $Z_C$ ” and “low  $Z_C$ ” mode for each of the dual-mode transmission lines under different amplitude codes is highlighted in Fig. 22. The impedance presented to each of the active unit PAs ( $Z_{PA}$ ) as the other unit PAs are slowly turned off is also highlighted in Fig. 22. It can be observed that  $Z_{PA} \in 0.5 - 1.25 \times Z_{OPT}$  for most of the amplitude codes [Fig. 21(c)].

The schematic for the practical implementation of the mm-wave Watt-level eight-way combined digital PA with dynamic load modulation is shown in Fig. 23. The implemented system comprises eight unit three-stage Class-E modulators designed for  $Z_{OPT} = 35 \Omega$  with input and output switch control.

The input switch is used to control power generation from the Class-E modulators, while the output switch network shorts the output to low impedance for the  $\lambda/4$  tunable transmission lines connected to the inactive modulator during switching operation, thus providing isolation to the active modulator chains. The output dynamic load modulation network comprises the dual-state transmission line base two-way  $\lambda/4$  combiner and a 4:1 slow-wave combiner for presenting the  $35\Omega$  optimum impedance to each of the eight unit PA chains under different switching configurations. The 4:1 slow-wave combiner is realized with  $\lambda/4$  slow-wave transmission lines with slotted ground planes for low insertion loss shown in Fig. 23 (inset). Since the input impedance of the Class-E modulators remains constant due to the complementary input switch network of each Class-E modulator, a low-loss zero-phase transmission line based 8:1 splitter has been used on the input side [1]. Finally, an additional Class-E driver is used for additional power gain of the system and to provide enough power to saturate the Watt-level digital PA. Each unit PA chain is designed to have a peak efficiency of 28% for  $Z_{OPT} = 35 \Omega$ , including the layout parasitics. The operation of the dynamic load modulation network as the different unit PAs are switched OFF is shown in Fig. 22. It can be observed that by correctly choosing the operating mode of the dual-state transmission line combiners as well as the pattern of unit PA switching, the system becomes balanced again when four unit

PA are switched OFF, thereby achieving peak efficiency at back-off, and then, the previous cycle of switching OFF the remaining PAs can be repeated. To compare the efficacy of the dynamic load modulation technique for amplitude control and enhanced back-off efficiency in an mm-wave digital PA, the proposed system is compared with the well-known Doherty amplifier load modulation curve assuming ideal lossless transmission line implementation in Fig. 22(f). The resultant efficiency curve versus power back-off in this proposed dynamic load modulation network is similar to that achieved by a Doherty amplifier architecture but with much flatter efficiency response for the 0 to  $-6$ -dB power control range and much smoother efficiency degradation at further back-off levels. In addition, since Doherty amplifiers typically use less efficient Class-AB

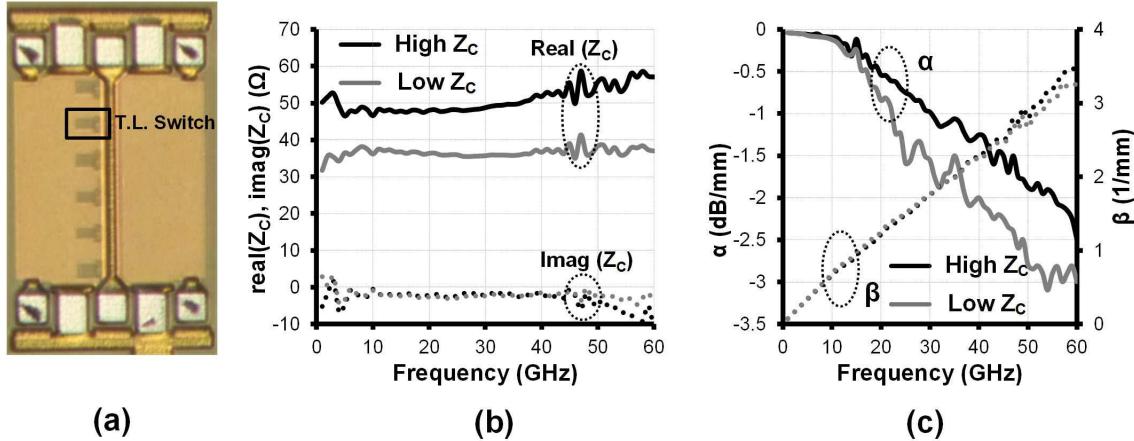


Fig. 18. Variable  $Z_C$  characteristics. (a) Fabricated test structure. (b)  $Z_C$  versus frequency. (c) Attenuation constant  $\alpha$  and propagation constant  $\beta$  versus frequency.

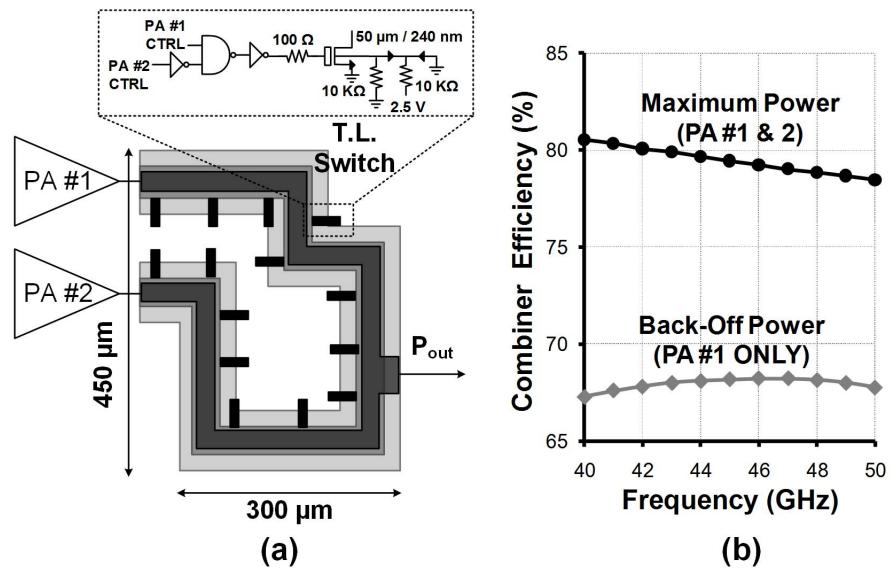


Fig. 19. (a) Two-way  $\lambda/4$  combiner using variable  $Z_C$  transmission lines. (b) Power combining efficiency under different operating modes.

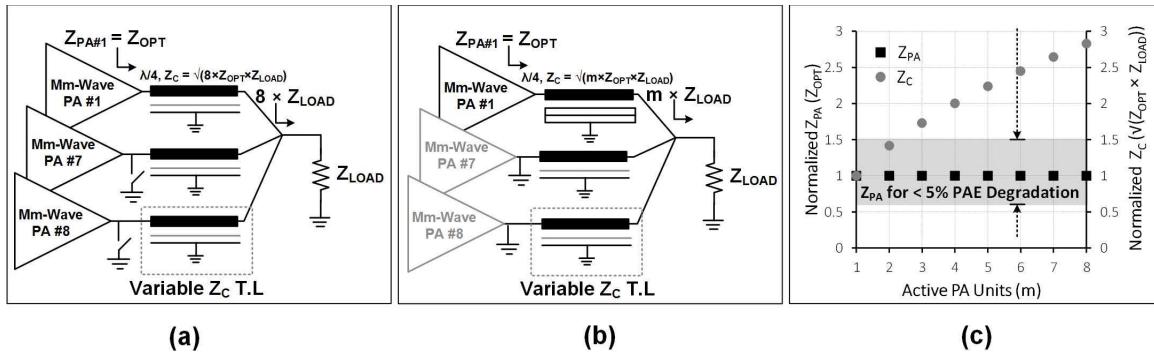


Fig. 20. Ideal dynamic load modulation network in an eight-way combined PA using variable  $Z_C$  transmission line with eight distinct  $Z_C$  values. (a) Peak power operation. (b) Back-off power operation when  $m$  out of eight unit PAs are active. (c) Constant  $Z_{PA}$  with power back-off by ensuring  $Z_C$  of  $\lambda/4$  transmission line is changing accordingly.

amplifiers as the main amplifier and the less efficient Class-C amplifiers as the peaking amplifier, the overall system efficiency of this efficient Class-E amplifier-based dynamic

load modulation network can be significantly better. In addition, at deeper back-off, the proposed load modulation system gives better efficiency than a Doherty amplifier.

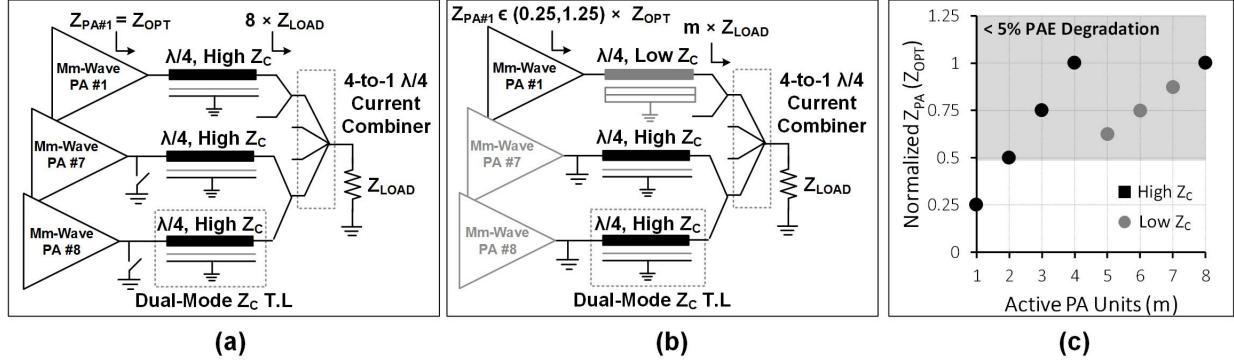


Fig. 21. Dynamic load modulation in a two-way + four-way combined PA with the proposed dual-mode  $\lambda/4$  transmission lines. (a) Peak power operation. (b) Back-off power operation when  $m$  out of eight unit PAs are active. (c) Variation of  $Z_{PA}$  with power back-off when operation mode (high  $Z_C$  or low  $Z_C$  mode) of the dual-state transmission line is appropriately chosen.

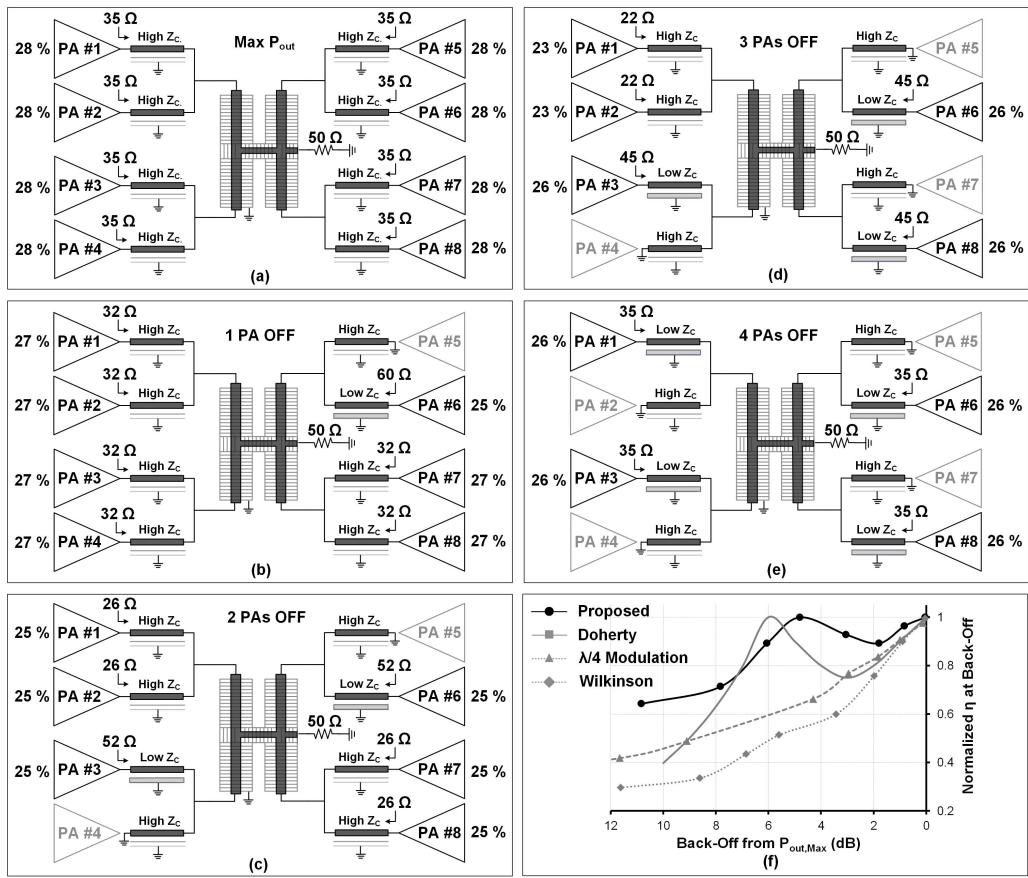


Fig. 22. Operation of the dynamic load modulation network. (a) Peak power operation, power control by (b) one PA OFF, (c) two PAs OFF, (d) three PAs OFF, and (e) four PAs OFF. (f) Power back-off efficiency comparison between different schemes.

This is because while at deep back-off, the Doherty amplifier efficiency profile is primarily the Class-AB slope, the dynamic load modulation network in conjunction with  $R_{Ballast}$  can still provide close to optimum impedance for the active unit Class-E PA chains for high efficiency. However, in contrast to Doherty amplifier with continuous back-off characteristics, the proposed digital PA can only achieve distinct points in the power back-off curve (eight for the implemented 3-b design). To take advantage of the improved back-off

characteristics especially at deep back-off in this dynamic load modulation combining scheme, a much higher resolution digital PA needs to be designed. It can also be observed that the efficiency at back-off for the proposed system is better than using a  $\lambda/4$  load modulation with fixed  $Z_C$  transmission lines.

Compared with the theoretical maximum achievable PAE of 34% for an eight-way combined system in Fig. 6(c), the achieved PAE for the eight-way digital PA is lower

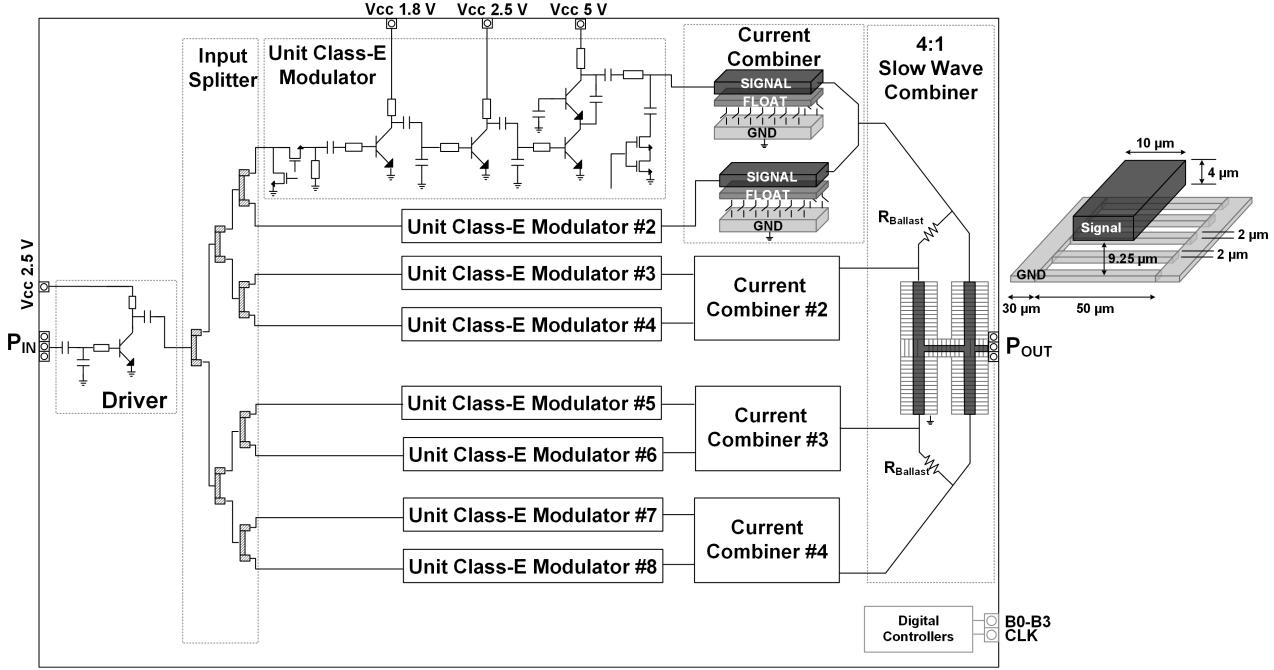


Fig. 23. Schematic of the mm-Wave Watt-level eight-way combined digital PA with dynamic load modulation network.

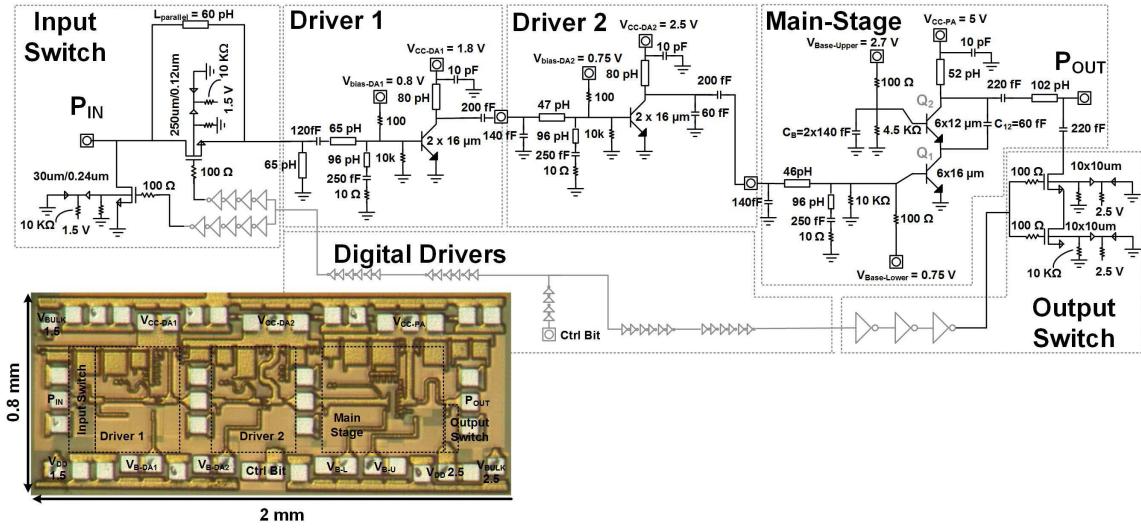


Fig. 24. 1-b mm-Wave Class-E power modulator. (a) Schematic. (b) Chip microphotograph.

at  $\approx 18.5\%$ . First, compared with the theoretical maximum PAE of a stacked Class-E PA at 59% based on the technology parameters, a real HBT implementation achieves 50% PAE primarily due to the unavailability of the higher harmonics of 45 GHz in the right amplitude and phase [28]. Second, to realize the Class-E modulator action with a lossy output switch network, the overall three-stage PA modulator efficiency again drops to 28% compared with the theoretical 45% for only a three-stage amplifier. Finally, compared with the theoretical eight-way combining loss of  $-1.2$  dB by using a hybrid two-way and four-way combining [Fig. 6(b)], the dynamic load modulation network with tunable transmission lines has a higher insertion loss of  $\approx 2$  dB, which further reduces

the overall system peak PAE to 18.5% [6]. However, in return, the chosen architecture can achieve high efficiency at backed-off power levels with several levels of output amplitude control.

## VIII. IMPLEMENTATION AND MEASUREMENT RESULTS

The proposed concepts are validated through silicon die implementations in a 0.13-μm SiGe BiCMOS process with seven metal layers. The large power transistors have been realized by parallel connection of smaller HBT devices from the process design kit. The capacitively coupled intradevice parasitics are modeled from standard  $RC$  extraction tools, while the large vias for the top metal layers have been modeled

TABLE II  
PERFORMANCE COMPARISON WITH SOME REPORTED STATE-OF-THE-ART mm-WAVE PAs AND POWER DACs

Performance Metric	Our Work		ISSC 2013	RFIC 2013		JSSC 2013	IMS 2014	ISSCC 2016	TMTT 2016
	Digital PA	1-bit Modulator		PA	Power DAC				
Continuous Wave Operation									
Frequency (GHz)	46	46	42	46	42.5	42.5	45	55	76
P <sub>out</sub> (dBm)	28.9	21.8	28.4	27.2	23.4	24.3	28	23.6	27.3
G <sub>p</sub> (dB)	13	10	18.5	19.5	11.9	18.4	N/R	19	19.3
Peak PAE (%)	18.4	18.5	10	10.7	6.7	14.6	13.5	27.7	12.4
Power Control Operation									
Amplitude Levels (Bits)	3	1	N/A	N/A	3	2	N/A	Analog PA	N/A
Total Efficiency @ 6dB Back-Off (%)	11	N/A	N/A	N/A	4.9	N/R	5	14	4
Modulation Speed (Gbps)	N/A	1.25 (ASK)	N/A	N/A	N/R	2.5 (BPSK)	N/A	3 (64-QAM)	N/A
Architecture	8-way Load Modulation	Class-E Modulator	16-way combined	8-way combined	1/4 load modulated	2-bit Power DAC	4-way spatially combined	2-way asymmetric combined	16-way combined
Area (mm <sup>2</sup> )	13.7	1.6	5.55	4.2	4.2	0.77	11.25	1.02	6.48
Technology	0.13 μm SiGe HBT	0.13 μm SiGe HBT	45 nm CMOS SOI	45 nm CMOS SOI	45 nm CMOS SOI	0.13 μm SiGe HBT	90 nm SiGe HBT		

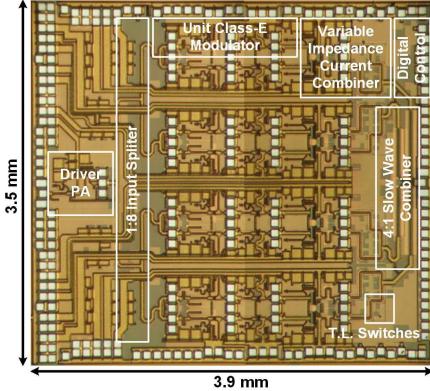


Fig. 25. Die microphotograph of the Watt-level eight-way combined digital PA.

as parasitic inductances using HyperLynx 3-D electromagnetic (EM) simulator [31]. The passive components, including MIM capacitors, microstrip line-based slab inductors, and the tunable transmission lines, have been modeled using EM simulation software [31]. Test GSG pads are placed between various stages of the designs for debugging (Figs. 24 and 25). Detailed design and layout principles concerning each of the individual designs are available in [6] and [22].

The absence of spurious oscillations under large-signal operation [29], [30] is ensured by monitoring the output via a spectrum analyzer. The output power measurements are validated both from the spectrum measurements as well as a thermocouple power sensor. The measurement setup loss at both the input and output is deembedded by scalar “through” measurements.

#### A. 1-Gb/s 46-GHz Class-E Power Modulator

To demonstrate high-speed data transmission using an input-modulated Class-E power modulator, a high-speed

1-b three-stage Class-E power modulator is implemented in the SiGe BiCMOS process using the SiGe HBTs for power generation at mm-wave frequencies and the 130-nm CMOS FETs for digital control of the input and output switch networks. The schematic and die microphotograph of the Class-E power modulator are shown in Fig. 24(a) and (b), respectively. The measured peak output power under static continuous wave operation is 21.8 dBm with 18.5% peak PAE at 46 GHz [22]. The 1-b ASK-modulated dynamic operation is shown in Fig. 26(a), where the transient waveform at 46-GHz carrier frequency captured using a sampling oscilloscope demonstrates a rise and fall time of 450 and 250 ps, respectively. The measured ON/OFF extinction ratio from Fig. 26(b) is estimated to be 30 dB. The reconstructed eye-diagram obtained by downconverting the modulated waveform is shown in Fig. 26(b) under 500 Mb/s and 1.25-Gb/s 1-b ASK modulation. The power modulator was tested under different data rates and the captured measured bit-streams were postprocessed using the MATLAB commscope-eyediagram toolbox [32] to estimate the BER to be  $1.6 \times 10^{-10}$  at 500 Mb/s,  $0.9 \times 10^{-6}$  at 1 Gb/s, and  $1.53 \times 10^{-6}$  at 1.25 Gb/s. The average power measurements under different modulation data rates are shown in Fig. 26(c) and show  $\approx 3$  dB lower measured power corresponding to 50% duty cycle and PAE varying between 12% and 10% for different modulation speeds.

#### B. 29-dBm 46-GHz Digital Power Amplifier

To demonstrate Watt-level power generation at mm-wave frequencies and enhanced efficiency under power back-off, an eight-way combined digital PA with integrated dynamic load modulation network was fabricated in the SiGe BiCMOS process [6]. The die microphotograph of the fabricated chip, including a number of internal pads for testability, is shown in Fig. 25. To validate the mm-wave modeling of the passives and actives for this multistage power combined system, a small signal s-parameter measurement was conducted under

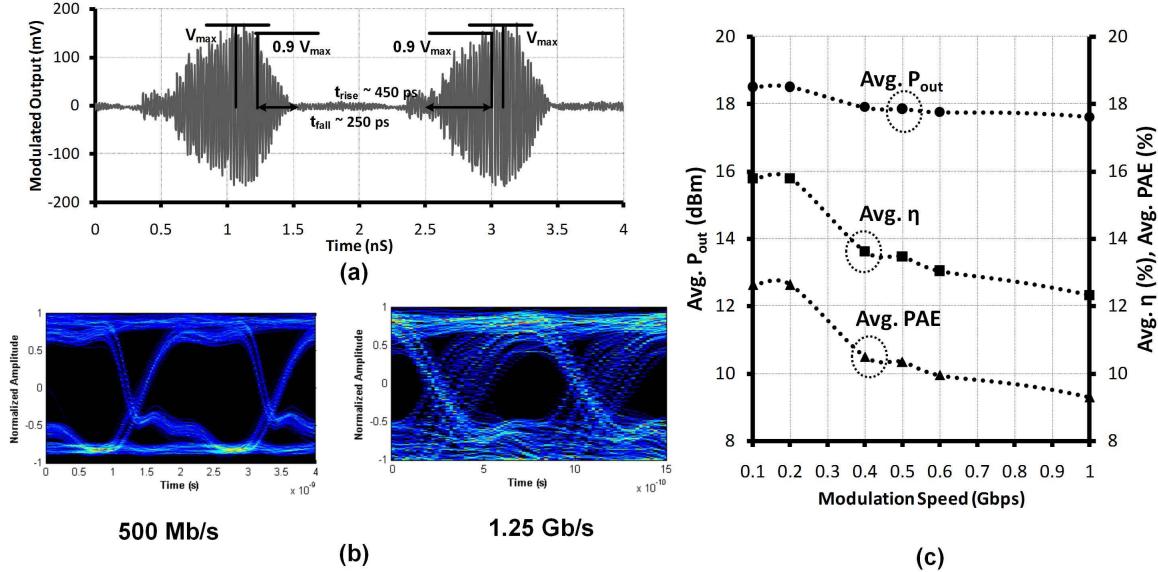


Fig. 26. 1-b Class-E modulator large-signal measurement under ASK modulation at 46 GHz. (a) Measured transient waveforms. (b) Recovered eye-diagram at 500 Mb/s and 1.25 Gb/s. (c) Average  $P_{out}$  and PAE versus modulation speed.

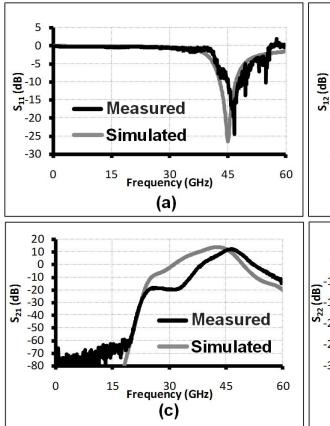


Fig. 27. Small signal s-parameter measurement of the digital PA under Class-A bias.

Class-A biasing, showing good correlation of input matching and gain transfer function between measurement and simulation (Fig. 27). Watt-level power generation in a silicon process at mm-waves was demonstrated by turning on all the unit Class-E PA chains by making the control bits B3-B0 high, and providing a continuous wave input at mm-wave frequencies. Fig. 28 shows the measured large-signal performance of the prototype with 28.9-dBm peak output power at 46 GHz with 18.4 % peak PAE and 13 dB of large-signal power gain. The power control operation of the digital PA was tested by cycling through different combinations of the control bits B3-B0 with a 46-GHz input signal. Fig. 29(a) shows the measured efficiency versus back-off power levels, as the output power level scales down for the different control bits. A -6-dB back-off efficiency of 11% is reported, which is 60% peak efficiency. It can be observed that the measured efficiency at -6-dB back-off is worse compared with the

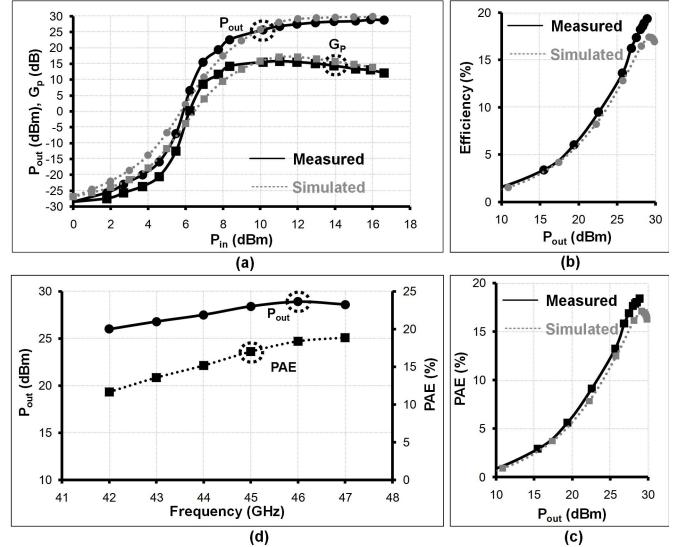


Fig. 28. Large-signal measurement of the Watt-level digital PA at 46 GHz. (a)  $P_{out}$ ,  $G_p$  versus  $P_{in}$ . (b) Efficiency versus  $P_{out}$ . (c) PAE versus  $P_{out}$ . (d) Performance across frequency.

expected 100% peak efficiency when all the four unit PAs are turned off, as shown in Fig. 22(f). This is primarily because of the higher insertion loss of the tunable transmission line when they operate in the low  $Z_C$  mode at -6-dB back-off point. In addition, there is some additional power loss and efficiency degradation due to nonideal  $\lambda/4$  termination of the inactive PA chains. The linearity of the system while not a primary design objective is tested by converting the measured output power on a 50- $\Omega$  load into output voltage amplitude and plotted in Fig. 29(b). The nonlinearity at the middle of control code sequence reflected by the highest DNL in Fig. 29(c) is again due to the balanced state that the dynamic load modulation network achieves at the code midpoint.

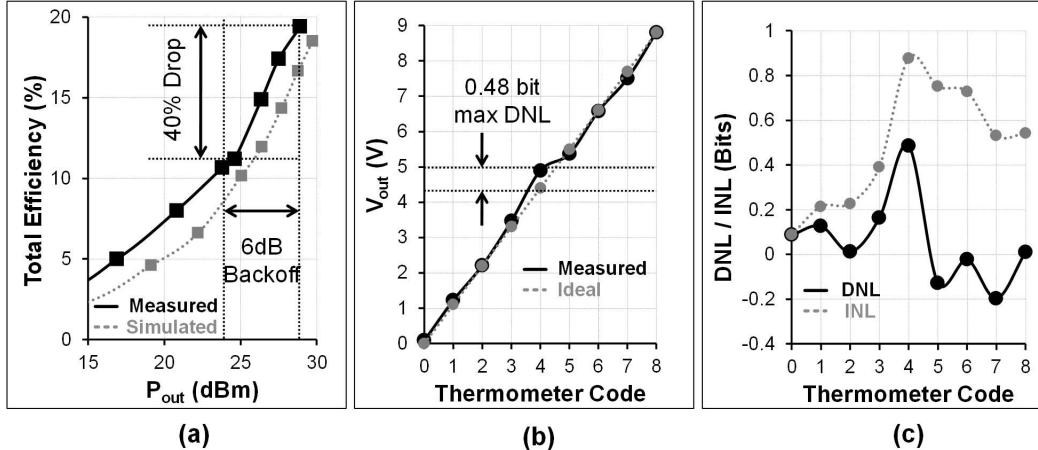


Fig. 29. Power control operation of the digital PA. (a) System efficiency versus power back-off. (b) Output voltage amplitude versus amplitude control code. (c) DNL/INL versus amplitude control code.

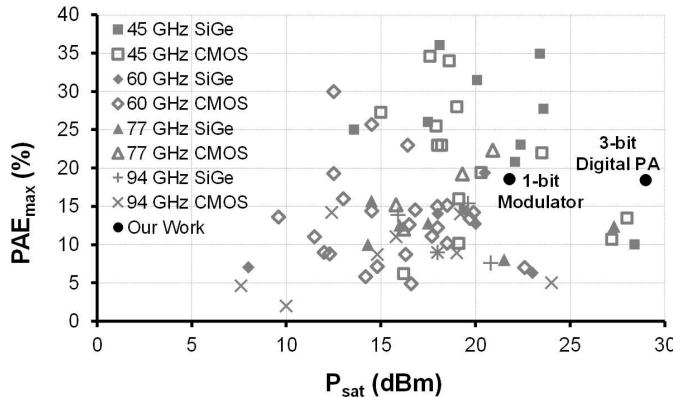


Fig. 30. Summary of PAE at  $P_{\text{sat}}$  for reported silicon mm-wave PAs.

## IX. CONCLUSION

In this paper, Watt-level power generation at mm-wave frequencies utilizing SiGe HBT Class-E PAs in different power combining architectures is discussed. High-speed data transmission using amplitude modulation in Class-E amplifiers is introduced. Several of these Class-E modulators are used in an eight-way combined digital PA to generate Watt-level output power. A tunable transmission line-based dynamic load modulation network is proposed to mitigate the effect of load pulling in this digital PA and ensure high efficiency under backed-off power levels. Prototypes demonstrating the highlighted concepts were fabricated in the 0.13- $\mu\text{m}$  SiGe BiCMOS process achieving the highest reported output power at mm-wave frequencies with the highest peak PAE for both SiGe and CMOS SOI technologies. A performance comparison with the reported state-of-the-art Q-band PA and power DACs is shown in Table II. Fig. 30 shows the saturated output power and PAE of the reported state-of-the-art mm-wave silicon PAs.

The high-power, high-efficiency amplifiers and modulators discussed in this paper can achieve high data rates in mm-wave DPTs by supporting complex signal constellations like 64-QAM with more bits per communication symbol. In a DPT scheme, generating more complex signal

constellations requires either more digital unit cell amplifiers (binary or nonbinary weighted) or oversampling the amplitude levels with fewer unit cell amplifiers. Both schemes pose implementation challenges at mm-waves and subject to further investigation.

## ACKNOWLEDGMENT

The authors would like to thank the technical discussions with J. Roderick (Teledyne Technologies), H. Krishnaswamy (Columbia University), and R. Worley (Airforce Research Laboratory).

## REFERENCES

- [1] W. Tai, L. R. Carley, and D. S. Ricketts, "A 0.7W fully integrated 42GHz power amplifier with 10% PAE in 0.13  $\mu\text{m}$  SiGe BiCMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 142–143.
- [2] R. Bhat, A. Chakrabarti, and H. Krishnaswamy, "Large-scale power-combining and linearization in watt-class mmWave CMOS power amplifiers," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2013, pp. 283–286.
- [3] H. Lin and G. M. Rebeiz, "A 70–80-GHz SiGe amplifier with peak output power of 27.3 dBm," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 7, pp. 2039–2049, Jul. 2016.
- [4] A. Balteanu *et al.*, "A 2-bit, 24 dBm, millimeter-wave SOI CMOS power-DAC cell for watt-level high-efficiency, fully digital m-ary QAM transmitters," *IEEE J. Solid-State Circuits*, vol. 48, no. 5, pp. 1126–1137, May 2013.
- [5] K. Datta and H. Hashemi, "Performance limits, design and implementation of mm-Wave SiGe HBT Class-E and stacked Class-E power amplifiers," *IEEE J. Solid-State Circuits*, vol. 49, no. 10, pp. 2150–2171, Oct. 2014.
- [6] K. Datta and H. Hashemi, "A 29 dBm 18.5% peak PAE mm-Wave digital power amplifier with dynamic load modulation," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 1–3.
- [7] N. O. Sokal and A. D. Sokal, "Class E-A new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE J. Solid-State Circuits*, vol. 10, no. 3, pp. 168–176, Jun. 1975.
- [8] I. Sarkas, A. Balteanu, E. Dacquay, A. Tomkins, and S. Voinigescu, "A 45nm SOI CMOS Class-D mm-Wave PA with >10 V<sub>pp</sub> differential swing," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 88–90.
- [9] S. V. Thyagarajan and A. M. Niknejad, "Efficient switching power amplifiers using the distributed switch architecture," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 10, pp. 2774–2787, Oct. 2013.
- [10] K. Datta, J. Roderick, and H. Hashemi, "Analysis, design and implementation of mm-Wave SiGe stacked Class-E power amplifiers," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2013, pp. 275–278.

- [11] A. Valdes-Garcia, S. Reynolds, and U. R. Pfeiffer "A 60GHz Class-E power amplifier in SiGe," in *IEEE ASSCC Dig. Tech. Papers*, Nov. 2006, pp. 199–202.
- [12] A. Chakrabarti and H. Krishnaswamy, "High power, high efficiency stacked mmWave Class-E-like power amplifiers in 45nm SOI CMOS," in *Proc. IEEE CICC*, Sep. 2012, pp. 1–4.
- [13] A. Agah, H. Dabag, B. Hanafi, P. Asbeck, L. Larson, and J. Buckwalter, "A 34% PAE, 18.6dBm 42–45GHz stacked power amplifier in 45nm SOI CMOS," in *IEEE RFIC Symp. Dig. Papers*, Jun. 2012, pp. 57–60.
- [14] C. M. Grens, P. Cheng, and J. D. Cressler, "Reliability of SiGe HBTs for power amplifiers—Part I: Large-signal RF performance and operating limits," *IEEE Trans. Device Mater. Rel.*, vol. 9, no. 3, pp. 431–439, Sep. 2009.
- [15] D. Pozar, *Microwave Engineering*, 4th ed. New York, NY, USA: Wiley, 2011.
- [16] J. Chen *et al.*, "A digitally modulated mm-Wave cartesian beamforming transmitter with quadrature spatial combining," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 232–233.
- [17] J.-W. Lai and A. Valdes-Garcia, "A 1V 17.9dBm 60GHz power amplifier in standard 65nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 424–425.
- [18] J. Chen and A. M. Niknejad, "A compact 1V 18.6dBm 60GHz power amplifier in 65nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 432–433.
- [19] C. R. Chappidi and K. Sengupta, "A frequency-reconfigurable mm-Wave power amplifier with active-impedance synthesis in an asymmetrical non-isolated combiner," in *IEEE ISSCC Dig. Tech. Papers*, Jan./Feb. 2016, pp. 344–345.
- [20] B. Hanafi, O. Gurbuz, H. Dabag, S. Pornpromlikit, G. Rebeiz, and P. Asbeck, "A CMOS 45 GHz power amplifier with output power >600 mW using spatial power combining," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2014, pp. 1–3.
- [21] A. Babakhani, X. Guan, A. Komijani, A. Natarajan, and A. Hajimiri, "A 77-GHz phased-array transceiver with on-chip antennas in silicon: Receiver and antennas," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2795–2806, Dec. 2006.
- [22] K. Datta and H. Hashemi, "A mm-Wave Class-E 1-bit power modulator," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2014, pp. 1–4.
- [23] K. Khalaf, V. Vidojkovic, J. R. Long, and P. Wambacq, "A 6x-oversampling 10GS/s 60GHz polar transmitter with 15.3% average PA efficiency in 40nm CMOS," in *Proc. IEEE ESSCIRC*, Sep. 2015, pp. 348–351.
- [24] A. Chakrabarti and H. Krishnaswamy, "Design considerations for stacked Class-E-like mmWave high-speed power DACs in CMOS," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2013, pp. 1–4.
- [25] W. Freude *et al.*, "Quality metrics for optical signals: Eye diagram, Q-factor, OSNR, EVM and BER," in *Proc. IEEE ICTON*, Jul. 2012, pp. 1–4.
- [26] W. H. Woods, A. Valdes-Garcia, H. Ding, and J. Rascoe, "CMOS millimeter wave phase shifter based on tunable transmission lines," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2013, pp. 1–4.
- [27] T. LaRocca *et al.*, "Millimeter-wave CMOS digital controlled artificial dielectric differential mode transmission lines for reconfigurable ICs," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2008, pp. 181–184.
- [28] F. H. Raab and N. O. Sokal, "Transistor power losses in the class E tuned power amplifier," *IEEE J. Solid-State Circuits*, vol. 13, no. 6, pp. 912–914, Dec. 1978.
- [29] A. Suarez and R. Quere, *Stability Analysis of Nonlinear Microwave Circuits*, 1st ed. Boston, MA, USA: Artech House, 2003.
- [30] A. Anakabe *et al.*, "Analysis of odd-mode parametric oscillations in HBT multi-stage power amplifiers," in *Proc. IEEE GAAS Symp.*, Oct. 2003, pp. 533–536.
- [31] *IE3D*, accessed on Mar. 16, 2016. [Online]. Available: <http://www.mentor.com/pcb/hyperlynx/3d-em/>
- [32] *Matlab*, accessed on Mar. 16, 2016. [Online]. Available: <http://www.mathworks.com/products/matlab/>



**Kunal Datta** (S'11) received the B.Tech. degree (Hons.) in electronics and electrical communications engineering from the IIT Kharagpur, Kharagpur, India, in 2010, and the Ph.D. degree in electrical engineering from the University of Southern California, Los Angeles, CA, USA, in 2016.

He was a Ming Hsieh Institute Scholar from 2014 to 2015. He is currently with Skyworks Solutions, San Jose, CA, USA. His current research interests include integrated radiofrequency and millimeter-wave power amplifiers and transmitters.

Mr. Datta was a recipient of the USC Provost Fellowship from 2010 to 2014, the IEEE Microwave Theory and Techniques Society Graduate Fellowship Award in 2014, and the IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award in 2014.



**Hossein Hashemi** (SM'08) received the B.S. and M.S. degrees in electronics engineering from the Sharif University of Technology, Tehran, Iran, in 1997 and 1999, respectively, and the M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology, Pasadena, CA, USA, in 2001 and 2003, respectively.

In 2003, he joined the Ming Hsieh Department of Electrical Engineering–Electrophysics, University of Southern California (USC), Los Angeles, CA, USA, where he is currently a Professor, a Ming Hsieh Faculty Fellow, and the Co-Director of the Ming Hsieh Institute. His current research interests include span mathematics, physics, and realization of integrated electrical and optical systems.

Dr. Hashemi served as a Distinguished Lecturer of the IEEE Solid-State Circuits Society from 2013 to 2014. He was a member of the Technical Program Committee of the IEEE International Solid-State Circuits Conference from 2011 to 2015, and the IEEE Compound Semiconductor Integrated Circuits Symposium from 2010 to 2014. He has been a member of the IEEE Radio Frequency Integrated Circuits Symposium since 2011. He was an Associate Editor of the *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS* from 2006 to 2007, and the *IEEE Transactions on Circuits and Systems II: Express Briefs* from 2004 to 2005. He has been an Associate Editor of the *IEEE JOURNAL OF SOLID-STATE CIRCUITS* since 2013. He was a Guest Editor of the *IEEE JOURNAL OF SOLID-STATE CIRCUITS* in 2013. He was a recipient of the 2015 IEEE Microwave Theory and Techniques Society Outstanding Young Engineer Award, the 2008 Defense Advanced Research Projects Agency Young Faculty Award, and the National Science Foundation CAREER Award. He was also a recipient of the USC Viterbi School of Engineering Junior Faculty Research Award in 2008, and was recognized as a Distinguished Scholar for Outstanding Achievement in Advancement of Engineering by the Association of Professors and Scholars of Iranian Heritage in 2011. He was a co-recipient of the 2004 JSSC Best Paper Award for A Fully Integrated 24-GHz 8-Element Phased-Array Receiver in Silicon and the 2007 IEEE ISSCC Lewis Winner Award for Outstanding Paper for A Fully Integrated 24-GHz 4-Channel Phased-Array Transceiver in 0.13- $\mu$ m CMOS based on a Variable Phase Ring Oscillator and PLL Architecture. He is the Co-Editor of the books *Millimeter-Wave Silicon Technology: 60 GHz and Beyond* (Springer, 2008) and *mm-Wave Silicon Power Amplifiers and Transmitters* (Cambridge University Press, 2015).