

A 7.9-GHz Transformer-Feedback Quadrature Oscillator With a Noise-Shifting Coupling Network

Bingwei Jiang and Howard C. Luong, *Fellow, IEEE*

Abstract—A noise-shifting coupling network is proposed for nonlinear passively coupled quadrature voltage-controlled oscillators (QVCOs). Both detailed analysis and circuit implementation demonstrate that the noise contribution by the coupling network can be minimized by re-aligning the phases of the noise modulation function and the impulse sensitivity function with a reduced magnitude. In addition, the QVCO with the proposed coupling network also incorporates the transformer-feedback technique to improve its performance in terms of phase noise, quadrature phase error, and low supply voltage. Fabricated in a 65-nm CMOS process, the QVCO prototype operating at 7.9-GHz measures phase noise at 10-MHz offset frequency of -143 dBc/Hz and minimum quadrature phase error of 0.23° while consuming 27.2 mW with a 0.8-V supply voltage.

Index Terms—In-Phase/Quadrature-Phase (IQ), noise shifting, passive coupling, phase error, phase noise, quadrature oscillator, quadrature voltage-controlled oscillator (QVCO), transformer feedback.

I. INTRODUCTION

TWO LC oscillators can be coupled together by a coupling network to generate quadrature outputs, but there exists serious tradeoff between the IQ phase accuracy and the phase noise [1]. The coupling network affects the phase noise performance through two mechanisms: reducing the effective quality factor (Q) of LC tanks and generating additional noise sources [2]. In the parallel-coupled quadrature oscillator [3], the transistors are used as the coupling network, which unfortunately consumes extra power, contributes significant noise, and degrades the effective- Q . To avoid Q -degradation, a phase shift can be introduced to the parallel-coupling current using phase shifting circuits [4], [5] or by shaping the current waveform [6]. However, the parallel-coupling paths still burn extra power and introduce additional noise sources. With the same current consumption, the series-coupled quadrature oscillator [7] achieves lower phase noise at the cost of lower voltage swing and thus worse phase noise for the same supply voltage unless the devices are very large, in which case the tank effective- Q would be significantly degraded.

Instead of using active coupling devices, passive coupling techniques are expected to contribute less noise and have no

extra power penalty. Transformer-coupled quadrature oscillators [quadrature voltage-controlled oscillators (QVCO)] [8] can achieve higher swing, lower supply voltage, lower noise, and lower power consumption, but the performance is sensitive to the transformer coupling coefficient, which may not be well controlled. In [9]–[12], the passive coupling devices form a bridge which consumes zero dc voltage headroom, as shown in Fig. 1(a), and avoid the degradation of the tank effective- Q due to off-resonance oscillation. For linear capacitive coupling [12], the small second-harmonic component of the LC -tank voltage [12] and the insufficient delay of negative- G_m cross-coupled pairs [13] cause large IQ phase error. Relying on the odd-order nonlinearity, compared to capacitive coupling, diode coupling can generate more accurate IQ phases with the same oscillation amplitude [9]. However, to achieve high phase accuracy, large coupling diodes are required, which in turn contribute significant phase noise.

In [14], a noise-shifting coupling network is proposed to reduce its phase noise contribution without extra power consumption and thus to improve the QVCO's overall power efficiency. Additionally, the transformer-feedback technique is also applied to further improve the performance to achieve a peak figure of merit (FoM) of -186.6 dB with minimum IQ phase error of 0.23° . This paper is significantly expanded from [14] to include more comprehensive analysis, design considerations, tradeoffs, and measurement results.

The rest of this paper is organized as follows. Section II reviews and clarifies previous phase noise analyses of diode-coupled quadrature networks. In Section III, the proposed noise-shifting coupling network is introduced, and quantitative analysis on the phase noise contribution of coupling devices compared to that of a conventional diode-coupling network is presented. The design of a QVCO prototype with the proposed noise-shifting coupling network and transformer feedback is detailed in Section IV. Section V presents the measurement results, and conclusions are drawn in Section VI.

II. PHASE NOISE FROM A DIODE-COUPLING NETWORK

Our proposed techniques are aiming at retaining the phase accuracy and power efficiency properties of a diode-coupling network while reduce the noise contribution from the noisy devices from such a coupling network. Before the discussion of the proposed noise-shifting coupling network, the quantitative analysis of phase noise from a diode-coupling network is first reviewed. The analysis is based on the time-variant model of the oscillator [15], which predicts the phase variation $\phi_n(t)$ induced by the cyclo-stationary noise

Manuscript received February 26, 2017; revised May 11, 2017; accepted May 31, 2017. Date of publication July 26, 2017; date of current version September 21, 2017. This paper was approved by Guest Editor Jaeha Kim. This work was supported by the Hong Kong Innovation and Technology Fund under Grant ITS/119/13FP. (Corresponding author: Bingwei Jiang.)

The authors are with the Department of Electronics and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong (e-mail: bjiangac@ust.hk; eeluong@ust.hk).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2017.2715855

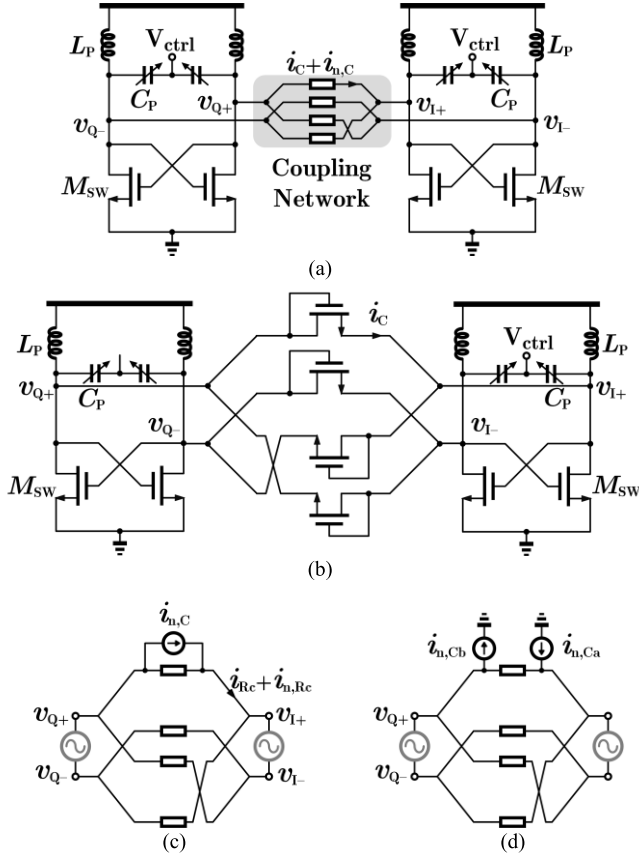


Fig. 1. (a) Schematic of a voltage-biased quadrature oscillator with a general passive coupling network. (b) Diode-coupled voltage-biased quadrature oscillator. (c) Coupling devices with current noise sources. (d) Circuits for ISF calculation.

current $i_n(t) = i_{n0}(t) \cdot \alpha(\omega_0 t)$ as

$$\begin{aligned} \phi_n(t) &= \frac{1}{q_{\max}} \int_{-\infty}^t \Gamma(\omega_0 \tau) \cdot i_n(\tau) d\tau \\ &= \frac{1}{q_{\max}} \int_{-\infty}^t \Gamma(\omega_0 \tau) \cdot \alpha(\omega_0 \tau) \cdot i_{n0}(\tau) d\tau \end{aligned} \quad (1)$$

where q_{\max} is the maximum charge displacement during the oscillation period across the capacitor on the node, ω_0 is the oscillation frequency, $\Gamma(\omega_0 t)$ is the impulse sensitivity function (ISF) associated with the noise current injected into the node, $\alpha(\omega_0 t)$ is the noise modulation function (NMF), and $i_{n0}(t)$ is the current noise source represented by a white stationary process. Denoting $\Gamma_{\text{eff}}(\omega_0 \tau) = \Gamma(\omega_0 \tau) \cdot \alpha(\omega_0 \tau)$ as the effective impulse sensitivity, the phase noise is given by

$$\mathcal{L}\{\Delta\omega\} = \frac{\overline{i_{n0}^2}/\Delta f}{2q_{\max}^2} \cdot \frac{\Gamma_{\text{eff,rms}}^2}{\Delta\omega^2} \quad (2)$$

where $\Delta\omega$ is the offset frequency from the carrier, $\overline{i_{n0}^2}/\Delta f$ is the power spectral density (PSD) of $i_{n0}(\tau)$, and $\Gamma_{\text{eff,rms}}$ is the rms value of $\Gamma_{\text{eff}}(\omega_0 \tau)$.

Fig. 1(b) shows a voltage-biased QVCO with a diode-coupling network. With the same method as in [16], the current noise $i_{n0,C}$ of the coupling device in Fig. 1(c) is modeled as two fully correlated grounded current noise sources $i_{n,Ca}$ and $i_{n,Cb}$ to simplify the ISF calculation. As shown in Fig. 1(d),

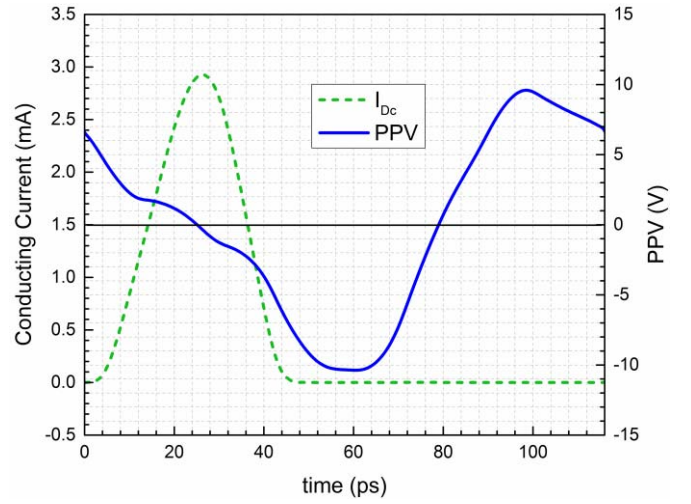


Fig. 2. Simulated PPV and conducting current of the coupling transistor in Fig. 1(a) with $C_P = 500$ fF, $L_P = 300$ pH.

$i_{n,Ca}$ and $i_{n,Cb}$ are separately injected into $I+$ node and pulled out of $Q+$ node. The sinusoidal output voltages at the $I+$ and $Q+$ nodes are represented by $A_0 \cos(\phi)$ and $A_0 \sin(\phi)$, respectively, where A_0 is the oscillation amplitude of the single-ended output, and $\phi \in [0, 2\pi]$ is used instead of $\omega_0 t$. In [14], the locking condition of the two coupled oscillators is used to estimate the abrupt voltage variance caused by the charge injected into the opposite tank. Based on this assumption, the disturbance causes that any phase variance at one oscillator output would cause a reverse phase variance at the output of the other oscillator [5]. However, in the steady state, the phase variances of the two oscillators finally become the same through the locking dynamics to stabilize the I/Q phases, and consequently, the ISFs associated with $i_{n,Ca}$ and $i_{n,Cb}$ are given by

$$\Gamma_{Ca}(\phi) = -\frac{1}{4} \cdot \sin \phi, \quad \Gamma_{Cb}(\phi) = -\frac{1}{4} \cos \phi \quad (3)$$

where the ratio 1/4 accounts for the four single-ended resonant tanks [2]. As a result, using the in-phase oscillator as reference, the overall ISF for $i_{n,C}$, $\Gamma_C(\phi)$, is given by

$$\Gamma_C(\phi) = \Gamma_{Ca}(\phi) + \Gamma_{Cb}(\phi) = -\frac{\sqrt{2}}{4} \cos\left(\phi - \frac{\pi}{4}\right). \quad (4)$$

Similarly, the ISF referred to the quadrature-phase oscillator is also given by $\Gamma_C(\phi)$.

With the above ISF, to calculate the effective ISF and its rms value, the NMF can be found using proper device models. With the same assumption in [16], the current noise PSD $\overline{i_{n,C}^2}/\Delta f$ can be derived to be [9]

$$\begin{aligned} \overline{i_{n,C}^2}/\Delta f &= 4k_B T \gamma g_C \\ &= 4\sqrt{2} k_B T \gamma \beta A_0 \left[\cos\left(\phi + \frac{\pi}{4}\right) - \cos(\Phi) \right] \end{aligned} \quad (5)$$

where $\beta = \mu_0 C_{ox} W/L$, γ is the channel current noise factor, and $\Phi = \cos^{-1}(V_T/\sqrt{2}A_0)$ is half the conduction angle.

From (4) and (5), the NMF of the coupling diode is orthogonal to the corresponding ISF, and this is verified by the simulation results shown in Fig. 2. In [14], the phase-domain model of ISF and its computation method

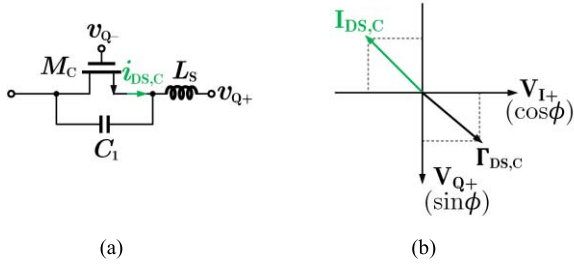


Fig. 3. (a) Coupling circuits with a reduced magnitude of ISF associated to the current noise of the coupling transistor, and (b) the corresponding phasor diagram.

in [17] were used to estimate ISF. In this simulation, the perturbation projection vector (PPV) method [18], [19] in the Spectre simulator is used to predict the ISF to avoid any post-processing of the simulated data. Assigning the NMF as $\alpha(\phi) = (\cos(\phi + \pi/4) - \cos(\Phi))^{1/2}$, the effective ISF $\Gamma_{C,\text{eff}}(\phi)$ and its square rms value become

$$\begin{aligned} \Gamma_{C,\text{eff}}(\phi) &= \alpha(\phi) \cdot \Gamma_C(\phi) \\ &= \frac{\sqrt{2}}{4} \cos\left(\phi - \frac{\pi}{4}\right) \sqrt{\cos(\phi + \pi/4) - \cos(\Phi)} \quad (6) \\ \Gamma_{C,\text{eff},\text{rms}}^2 &= \frac{1}{2\pi} \int_{-\Phi-\pi/4}^{\Phi-\pi/4} \Gamma_{C,\text{eff}}^2(\phi) d\phi \\ &= \frac{1}{16\pi} \left[\sin(\Phi) - \frac{1}{3} \sin^3(\Phi) - \Phi \cos(\Phi) \right]. \quad (7) \end{aligned}$$

Substituting (7) into (3), the phase noise contribution of the coupling devices is given by

$$\begin{aligned} \mathcal{L}\{\Delta\omega\} &= 4 \cdot \frac{i_{n0,C}^2 / \Delta f}{2q_{\text{max}}^2} \cdot \frac{\Gamma_{C,\text{eff},\text{rms}}^2}{\Delta\omega^2} \\ &= \frac{\sqrt{2}k_B T \gamma \beta A_0}{2\pi q_{\text{max}}^2 \Delta\omega^2} \left[\sin(\Phi) - \frac{1}{3} \sin^3(\Phi) - \Phi \cos(\Phi) \right]. \quad (8) \end{aligned}$$

The loading effect of large diodes reduces the oscillation amplitude and thus q_{max} , which is proportional to the oscillation amplitude, and finally induces a high phase noise. Consequently, enhancing the oscillation amplitude is an effective way to improve the phase noise. In addition, from (1), with certain current noise PSD, there are two approaches to further reduce the phase noise contribution from the coupling transistors: reducing the magnitude of the corresponding ISF, and shifting the phases of ISF and NMF to be orthogonal with each other. Both methods result in a reduced scalar product of ISF and NMF. In the diode-coupling network, the ISF and NMF are orthogonal to each other, and to reduce the phase noise contributed by the coupling diodes, the magnitude of ISF and the conducting current of coupling transistor should be scaled properly so that the 90° phase difference between ISF and NMF and the IQ phase accuracy are not affected.

III. PROPOSED NOISE-SHIFTING COUPLING NETWORK

A. Phase Noise From the Noise-Shifting Coupling Network

As shown in Fig. 3, large L_S is added to reduce the magnitude of the voltage across C_1 and M_C . With the same

equivalent LC tank as the diode-coupled quadrature oscillator, the magnitude of ISF associated with the current noise of M_C is consequently reduced. Since the source node voltage coupled from Q_+ node is small with a large L_S , a diode connection of M_C could not provide enough effective coupling current, and thus v_{Q-} is applied to the gate node to guarantee the quadrature coupling.

From (26) in Appendix A, the magnitude of ISF is reduced by about $\sqrt{2}/(\omega_0^2 L_S C_1 - 1)$ compared to the ISF associated with the current noise injected into the output nodes. However, such coupling circuits cause an in-phase relationship between ISF and NMF of the noisy coupling transistor as shown in the phasor diagram in Fig. 3(b), where ISF phase is given by $\phi - (\pi/4)$ (as derived in Appendix A). The NMF phase can be approximated by the phases of the gate-to-source voltage $v_{GS,C}$ and of the conducting current $i_{DS,C}$ of the coupling transistors which are given by

$$v_{GS,C} \approx -v_{Q+} - v_{I+} = -\sqrt{2}A_0 \cos\left(\phi - \frac{\pi}{4}\right) \quad (9)$$

$$i_{DS,C} = \frac{\beta}{2} \left[-\sqrt{2}A_0 \cos\left(\phi - \frac{\pi}{4}\right) - V_T \right]^2. \quad (10)$$

Since too large on-chip inductors are difficult to implement, coupling circuits shown in Fig. 3(a) with practical on-chip inductors would increase the magnitude of ISF, and together with the in-phase relationship between ISF and NMF, the conversion from the current noise of the coupling transistors to the phase noise would be large. Based on the concept of cyclo-stationary noise alignment [20], shifting the NMF and ISF to be orthogonal to each other is an effective approach to minimize this conversion. To shift the conducting current and ISF to realize a phase difference of 90° between each other, in addition to the coupling circuits shown in Fig. 3(a), another capacitor C_2 is added to scale the voltage at the source node of the coupling transistors. This results in the proposed noise-shifting coupling network, as shown in Fig. 4(a). For $v_{I+} = A_0 \cos(\phi)$ and $v_{Q+} = A_0 \sin(\phi)$, the gate-to-source voltage $v_{GS,C}$ and the conducting current $i_{GS,C}$ are now given by

$$\begin{aligned} v_{GS,C} &= -\frac{\omega_0^2 L_S (C_1 + C_2) - 2}{\omega_0^2 L_S (C_1 + C_2) - 1} \cdot V_{Q+} - \frac{\omega_0^2 L_S C_1}{\omega_0^2 L_S (C_1 + C_2) - 1} \cdot V_{I+} \\ &= -k A_0 \cos(\phi - \phi_1) \quad (11) \end{aligned}$$

$$i_{DS,C} = \frac{\beta}{2} [-k A_0 \cos(\phi - \phi_1) - V_T]^2 \quad (12)$$

$$\begin{aligned} \phi_1 &= \tan^{-1}\left(\frac{k_1}{k_2}\right) = \tan^{-1}\left(\frac{1}{n} - \frac{2}{\omega_0^2 L_S C_1}\right) \\ n &= \frac{C_1}{C_1 + C_2}, \quad k^2 = k_1^2 + k_2^2. \quad (13) \end{aligned}$$

The phasor diagram in Fig. 4(b) shows that the scaled source voltage realizes a scaled projection on the horizontal axis of $i_{DS,C}$ and thus a larger ϕ_1 in (12). From the ISF derived in Appendix A, with C_2 applied to the source node, the ISF is shifted toward the phasor of $-\sin(\phi)$. As a result, the phasors $i_{DS,C}$ and $\Gamma_{DS,C}$ tend to get closer to each other with a smaller phase difference by increasing C_2 . From (11) and (25) in Appendix A, the phase difference between $i_{DS,C}$ and Γ_C is

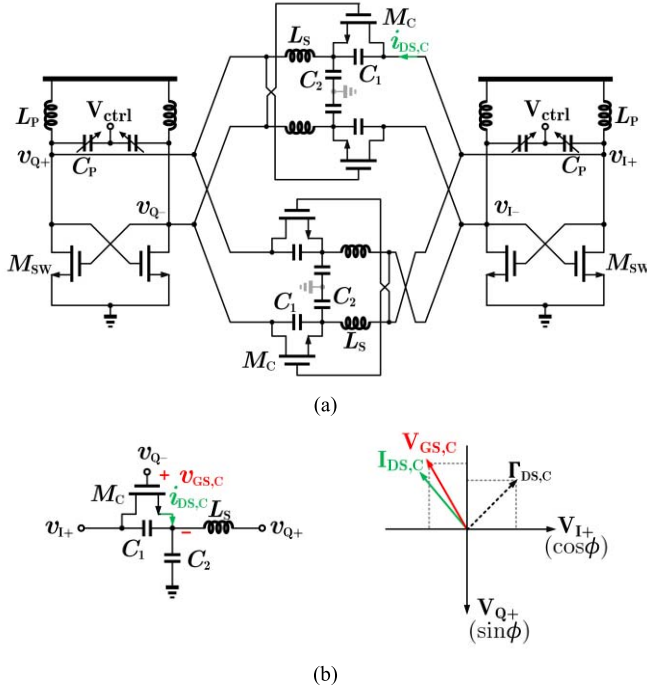


Fig. 4. (a) Proposed noise shifting coupling network, and (b) the corresponding phasor diagram.

given by

$$\Delta\phi = \pi - \tan^{-1}(\omega_0^2 L_S C_2 - 1) - \tan^{-1}\left(\frac{1}{n} - \frac{2}{\omega_0^2 L_S C_1}\right) - \Delta\phi_{vi} \quad (14)$$

where $\Delta\phi_{vi}$ is the switching delay after M_C is turned on and begins to charge the capacitors. To swap the I/Q phases in the above analysis, another possible phase difference $\Delta\phi'$ between I_C and Γ_C is obtained as

$$\Delta\phi' = \tan^{-1}(\omega_0^2 L_S C_2 - 1) + \tan^{-1}\left(\frac{1}{n} - \frac{2}{\omega_0^2 L_S C_1}\right) - \Delta\phi_{vi}. \quad (15)$$

From (14) and (15), for both possible phase sequences between two oscillators, the optimal phase difference can be achieved with the following equation:

$$\tan^{-1}(\omega_0^2 L_S C_2 - 1) + \tan^{-1}\left(\frac{1}{n} - \frac{2}{\omega_0^2 L_S C_1}\right) - \Delta\phi_{vi} = \frac{\pi}{2}. \quad (16)$$

Neglecting $\Delta\phi_{vi}$, (16) can be simplified as

$$\frac{1}{\omega_0^2 L_S C_2 - 1} = \frac{1}{n} - \frac{2}{\omega_0^2 L_S C_1}. \quad (17)$$

With a fixed C_1 , the capacitance C_2 affects both the phase difference and oscillation frequency. With several design iterations for the target oscillation frequency, which will be discussed in detail in the next section, the optimal value of C_2 can be obtained. In Fig. 5(a), the PPV and the conducting current, which correspond to the schematic in Fig. 3(a), in which C_2 are not added, are near in-phase with each other.

Fig. 5(b) and (c) shows the two possible phase differences that exist in a quadrature oscillator with the proposed coupling network. Fig. 5(d) shows the switching time of M_C follows its gate-to-source voltage except an switching delay from $v_{GS,C}$ to $i_{DS,C}$. From the simulation result, a switching delay around 10° is observed, and such a delay should be taken into account for an optimized phase difference for both phase sequences. By sweeping C_2 , two sets of phase differences can be obtained from the simulation and are summarized in Fig. 6. From Fig. 6, the simulated phase difference between $I_{DS,C}$ and PPV is close to the value predicted by (14) and (15). The overestimated phase difference with a large C_2 is due to the simplified analysis of ISF. Intuitively, with an infinite large C_2 , the coupling circuits become equivalent to a parallel coupling topology, for which the phase shift of ISF is affected by the coupling strength [21].

With an optimized phase difference between ISF and NMF, assigning NMF as $\alpha(\phi) = (-\cos(\phi - \phi_1) - \cos(\Phi))^{1/2}$, where $\Phi = \cos^{-1}(V_T/kA_0)$, and assuming that $[\omega_0^2 L_S (C_1 + C_2) - 1]^2$ is much larger than 1, the effective ISF and the phase noise contribution of the coupling transistors can be calculated as

$$\begin{aligned} \Gamma_{DS,C,eff,rms}^2 &= \frac{1}{2\pi} \int_{-\Phi+\phi_1-\pi}^{\Phi+\phi_1-\pi} \Gamma_{DS,C,eff}^2(\phi) d\phi \\ &\approx \frac{(1-n)^2}{16\pi} \left[\sin(\Phi) - \frac{1}{3}\sin^3(\Phi) - \Phi \cos(\Phi) \right] \quad (18) \\ \mathcal{L}\{\Delta\omega\} &= 4 \cdot \frac{i_{n0,DS,C}^2 / \Delta f}{2q_{max}^2} \cdot \frac{\Gamma_{DS,C,eff,rms}^2}{\Delta\omega^2} \\ &= \frac{k(1-n)^2 k_B T \gamma \beta A_0}{2\pi q_{max}^2 \Delta\omega^2} \\ &\quad \times \left[\sin(\Phi) - \frac{1}{3}\sin^3(\Phi) - \Phi \cos(\Phi) \right]. \quad (19) \end{aligned}$$

Comparing (7) and (19), owing to the scaled magnitude of the ISF, with the same q_{max} , the proposed coupling network contributes less phase noise compared to a nonlinear coupling network implemented by diode-connected MOSFETs. As discussed later, the coupling strength in the proposed coupling network will be linearly reduced with an increasing n . Since the phase error is inversely proportional to the effective coupling current [9], the coupling transistors can be sized up to achieve the same coupling strength and thus the same phase error while the phase noise contributed by the coupling transistors can still be reduced owing to the quadratic reduction of the phase noise with the scaling ratio, assuming that the oscillation amplitude and the 90° phase difference between ISF and NMF vary little. As compared to scaling down the size of diodes, both the phase noise and the effective coupling strength are linearly reduced if the loading effect is small. Consequently, with the same phase error, reducing the size of diodes in diode-coupling network cannot achieve the same phase noise performance as compared to using larger M_C in the proposed coupling network. As such, our proposed noise-shifting coupling network benefits from both the reduced ISF magnitude and the phase re-alignment.

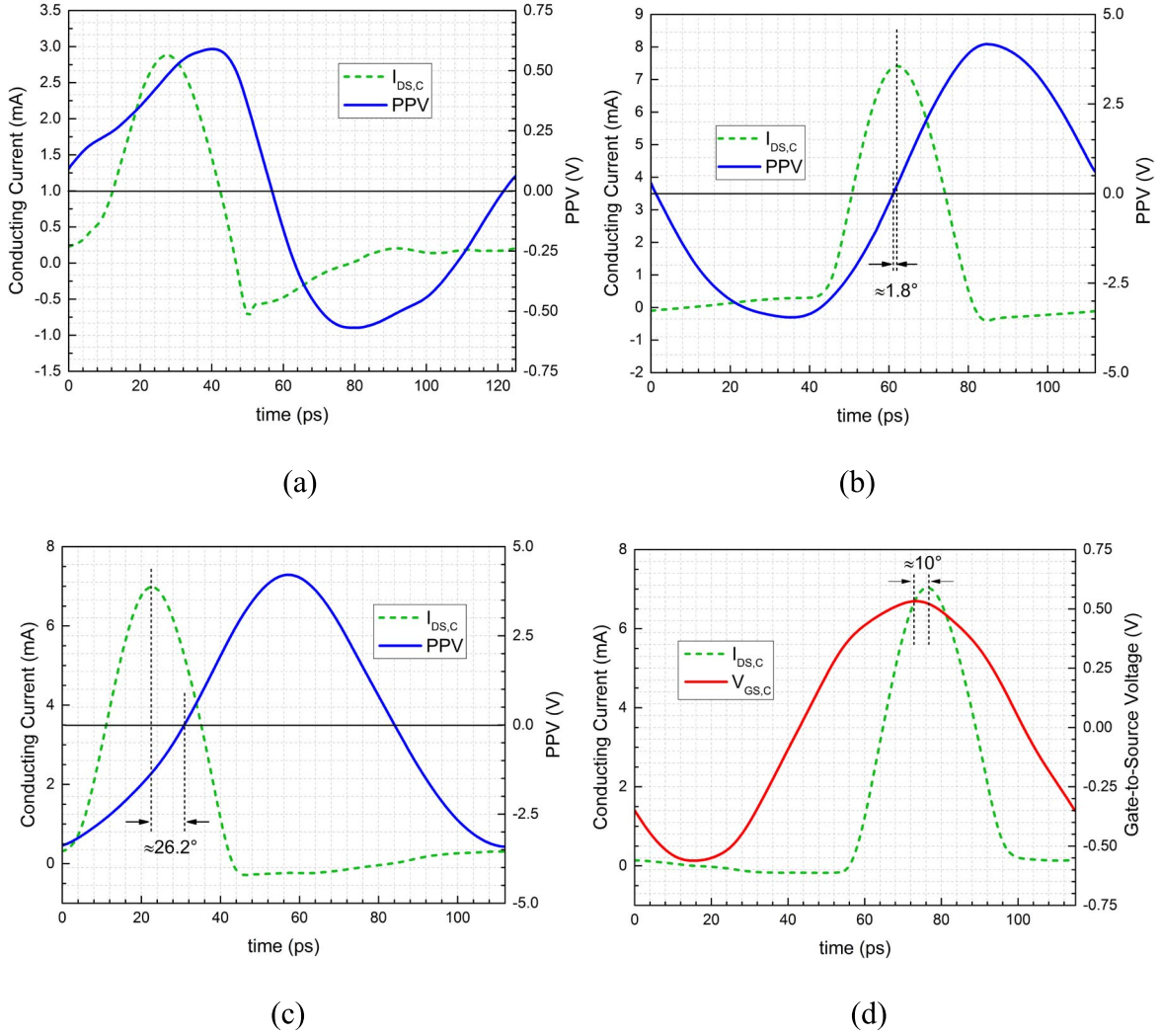


Fig. 5. Simulated conducting current and PPV corresponding to Fig. 4(a) with $C_P = 500$ fF, $L_P = 600$ pH, $Q = 20$, and different combinations of: (a) $C_1 = 600$ fF, $L_S = 10$ nH, $C_2 = 0$, (b) $C_1 = 600$ fF, $L_S = 900$ pH, $C_2 = 1.2$ pF, and $\Delta\phi = 88.2^\circ$, (c) $C_1 = 600$ fF, $L_S = 900$ pH, $C_2 = 1.2$ pF, and $\Delta\phi = 116.2^\circ$, and (d) simulated current and voltage waveforms.

B. Oscillation Frequency

The accurate explicit equation for the oscillation calculation is difficult to obtain since the inductors and capacitors in the coupling network appear as part of the resonator. The quadrature oscillator with the proposed coupling network is modeled as a ring with four identical unit cells for oscillation-frequency analysis [13], [22], as shown in Fig. 7(a), and the effect of the coupling transistors is neglected for simplicity. For the circuit operation, the series inductor L_S senses a voltage divided from the output of the preceding stage. From another perspective, the capacitive dividing circuits, together with a transformed impedance from L_S , load to the output node, and the equivalent circuit is redrawn as Fig. 7(b). For quadrature-phase generation, the phase difference between each cell is automatically 90° , and therefore, to ensure that the energy stored in L_S is unchanged, $L_{S,eq}$ and $C_{P,eq}$ are given by

$$L_{S,eq} = \sqrt{\frac{2}{1+n^2}} L_S, \quad C_{P,eq} = C_P + nC_2. \quad (20)$$

Then, the oscillation frequency is approximated by

$$\omega_0 \approx \frac{1}{\sqrt{\frac{L_{S,eq} L_P}{L_{S,eq} + L_P} \cdot C_{P,eq}}} = \frac{1}{\sqrt{\frac{\sqrt{\frac{2}{1+n^2}} L_S L_P}{\sqrt{\frac{2}{1+n^2}} L_S + L_P} \cdot (C_P + nC_2)}}. \quad (21)$$

Fig. 7(c) shows the calculated and simulated oscillation frequencies, from which the oscillation frequency predicted by (21) agrees quite well with the simulated results.

I/Q phase error is caused by mismatches between the two coupled oscillators and matching networks. Although the proposed coupling circuits introduce more mismatch sources compared to a simple diode-coupling network, the extra passive devices used in the proposed coupling network with large sizes have much less effects on the phase error than other devices with small sizing. However, the proposed coupling network reduces the coupling strength, and thus the phase accuracy becomes worse compared to that of a quadrature oscillator coupled by diode-connected transistors with the same size. To get the same effective voltage for phase correction that

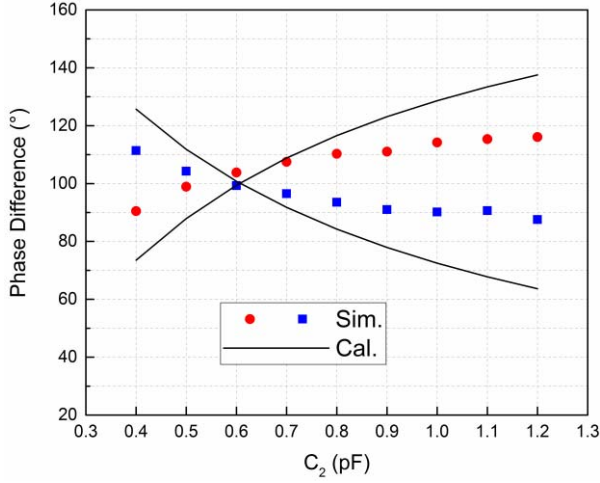


Fig. 6. Simulated and calculated phase difference between ISF and NMF with different C_2 .

generated by a current i_{eq} which is directly injected into the tank output node, for instance I_+ , the effective coupling current $i_{DS,C}$ should be increased by about $1/(1-n)$, which corresponds to the ratio between the transimpedance transfer function from i_{eq} to v_{I+} and that from the current input at M_C branch to the output. Using the phasors of the circuit variables shown in Fig. 7(a), the transimpedance transfer functions are given by (22), as shown at the bottom of this page.

Furthermore, from (14)–(16), the phase alignment will be limited by a large n , and the output loading is increased by sizing up the coupling transistor to maintain the same phase error performance. Consequently, a too large $n = C_1/(C_1 + C_2)$ is avoided during the design. To find the optimal ratio n at the 8.5-GHz operating frequency with $C_P = 600$ fF, by varying C_1 and C_2 only to vary the ratio of n , the phase noise and worst-case phase error performances of QVCO with the proposed noise-shifting coupling network are simulated with the 0.5% capacitance mismatch, as shown in Fig. 8. From the simulation results, as expected, the phase noise performance is improved with increasing n . On the other hand, with n being larger than 0.5, the phase error becomes worse. To achieve a good tradeoff between the phase noise and the phase error, the optimal ratio n can be found around 0.35.

IV. QUADRATURE OSCILLATOR DESIGN

According to (12) and (19), increasing the oscillation amplitude increases the maximum stored charge q_{max} and the conducting current of the coupling transistor $i_{DS,C}$, and finally results in a simultaneous improvement of the phase noise and the phase error. In this design, in addition to the

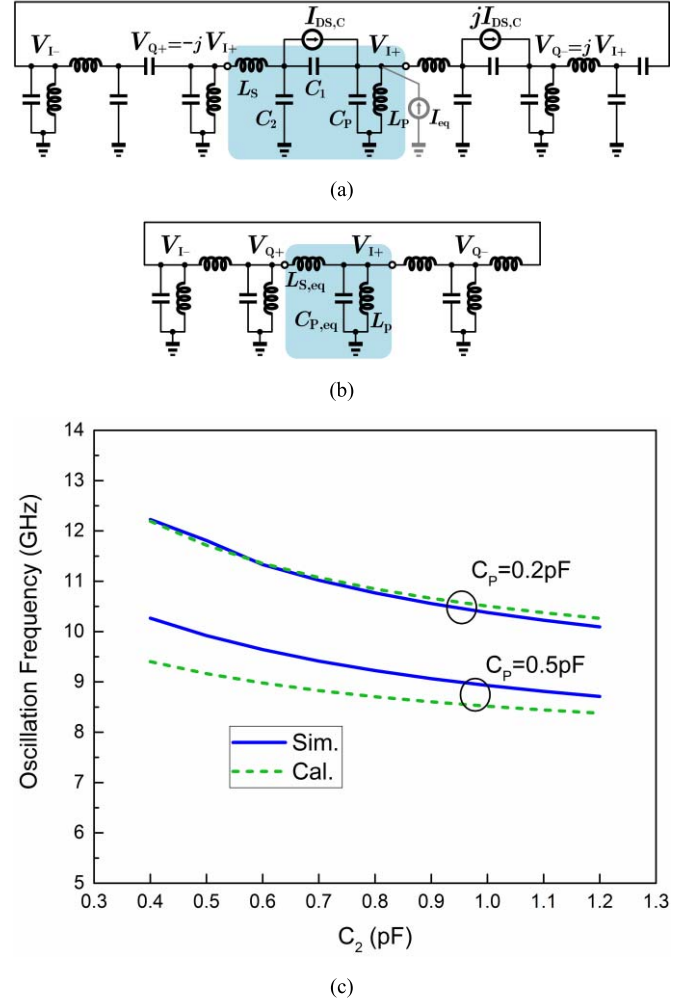


Fig. 7. (a) Small signal ring-model of the circuit in Fig. 5(a). (b) Its simplified model. (c) Comparison between simulated and calculated oscillation frequency.

proposed noise-shifting coupling network, the transformer-feedback technique [23] is also applied to boost up the oscillation amplitude to improve the performance in terms of low phase noise, high frequency, and low supply voltage, as shown in Fig. 9. The coupling factor k_m between 660 pH L_1 and 220 pH L_2 is 0.68, and the maximum oscillation amplitude is increased to $1.39 \times 2 V_{DD}$, where 1.39 is from $1 + k_m \cdot \sqrt{L_2}/L_1$ [23]. After the optimization of the individual oscillators with transformer feedback, the noise-shifting coupling network is designed with an optimal capacitance ratio n . In the coupling network, as shown in Fig. 9, to avoid complex layout of four inductors in the coupling network, two groups of coupled coils are implemented for the inductors L_S , and the

$$\begin{aligned} \frac{V_{I+}}{I_{eq}} &= \frac{j[\omega^2 L_S(C_1 + C_2) - 1]\omega L_P}{\omega^4 L_S L_P C_1(C_2 + C_P) - \omega^2[L_S(C_1 + C_2) + L_P(2C_1 + C_2 + C_P)] + 1} \\ \frac{V_{I+}}{I_{DS,C}} &= \frac{j[\omega^2 L_S C_2 - 1 - j]\omega L_P}{\omega^4 L_S L_P C_1(C_2 + C_P) - \omega^2[L_S(C_1 + C_2) + L_P(2C_1 + C_2 + C_P)] + 1} \end{aligned} \quad (22)$$

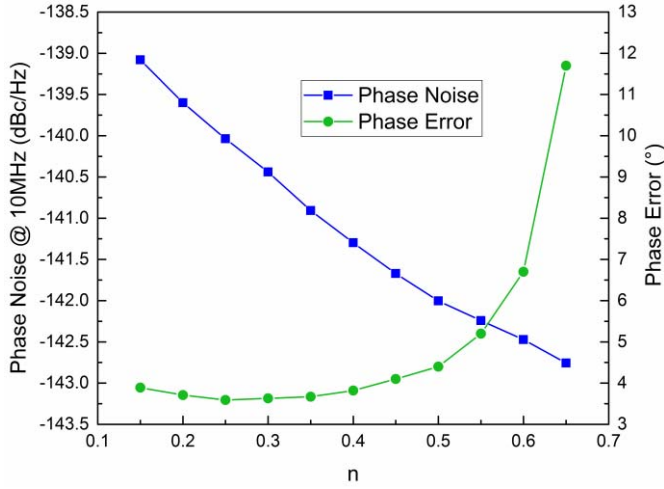


Fig. 8. Simulated phase error and phase noise of QVCO in Fig. 4(a) with different ratio n .

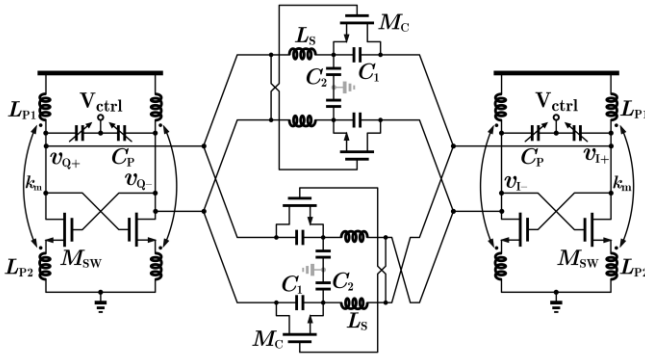


Fig. 9. Schematic of the QVCO prototype with the proposed noise-shifting coupling network.

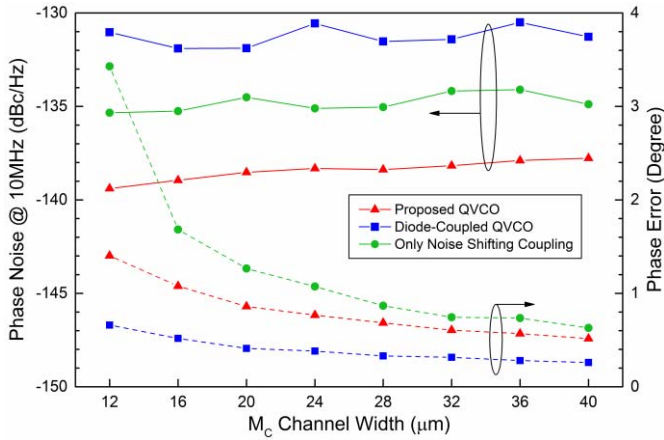


Fig. 10. Comparison of simulated phase noise (solid) and phase error (dashed) of the conventional diode-coupled voltage biased quadrature oscillator and the proposed quadrature oscillator with and without transformer feedback.

equivalent single-ended inductance L_S equals 864 pH. Both the transformers in the coupling network and in the individual oscillators are fully custom designed, and the quality factors of 20 and 16 are achieved for L_P and L_S , respectively, through

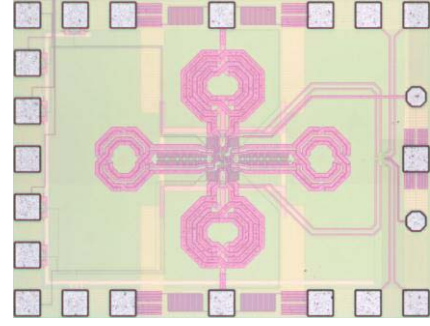


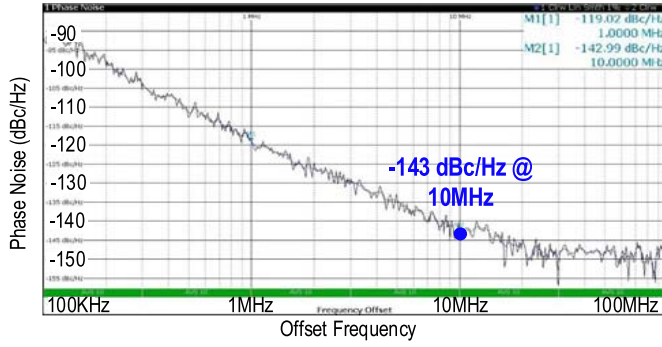
Fig. 11. Chip photo of the proposed quadrature oscillator.

electromagnetic simulations. With the polarity shown in Fig. 9, the transformers with a negative coupling coefficient used for the coupling network implement larger inductors with a more compact layout and less substrate loss. The parasitic capacitors coupled to substrate are also reduced by adopting a transformer implantation. However, the inter-winding capacitance of the transformer would add more parasitic and increase C_2 . To keep the same desired capacitance ratio $n = C_1/(C_1 + C_2)$, C_1 should be increased accordingly, which in turn would reduce the operation frequency. In this paper, a moderate coupling coefficient of -0.44 is designed for the transformer as a tradeoff. Using a switched-capacitor array (SCA), the nominal capacitance ratio n can be tuned from 0.3 to 0.5 with C_1 of 608 fF. With the parasitic capacitance from the transformers taken into account, the ratio n is around the optimized value of 0.35 as discussed above.

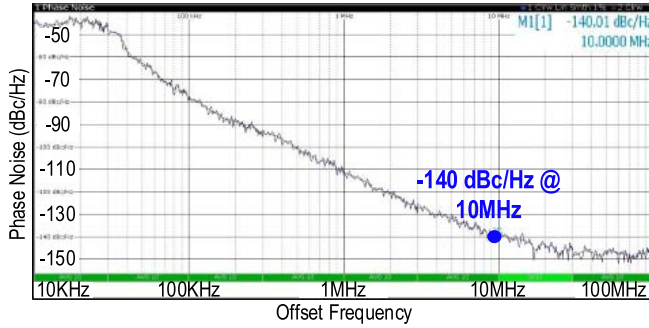
For comparison, both the proposed QVCO and the conventional diode-coupled voltage-biased quadrature oscillator are designed and simulated with 0.5% capacitance mismatch. For a fair comparison, with the same tank Q , the capacitance mismatch should introduce the same resonant frequency difference between the two individual oscillators. Based on the analysis for frequency analysis described above, a scaled L_P and the same tank Q are chosen for the diode-coupled quadrature oscillator. The parasitic capacitance of the coils is omitted to avoid any error sources, and the two oscillators are designed to operate at the same oscillation frequency of 11.8 GHz with the same supply voltage of 0.6 V. As discussed in Section III, to achieve the same phase error, M_C needs to size up. As shown in Fig. 10, with larger M_C for the same phase error, the proposed QVCO still achieves >6 dB improvement of the phase noise for the same phase error, out of which roughly 3 dB is from the proposed noise-shifting coupling technique and ~ 3 dB is from the transformer feedback. From the noise summary, as compared to the traditional diode-coupling network, using the proposed coupling network with M_C being ~ 3 times to achieve the same phase error of 1° , the noise contribution of M_C is reduced from 5.2×10^{-15} to 1.16×10^{-15} V²/Hz at 10-MHz offset frequency.

V. MEASUREMENT RESULTS

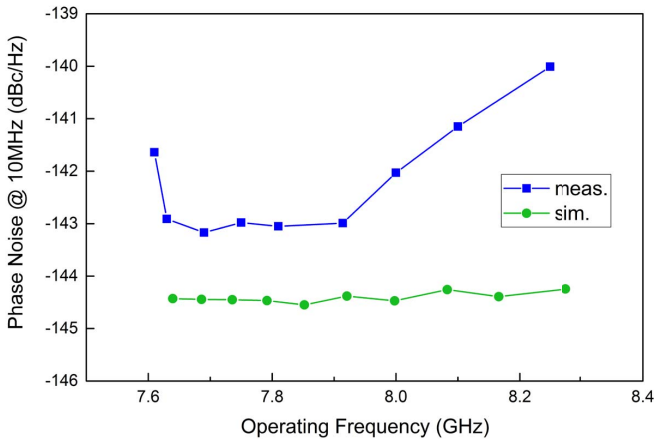
The proposed quadrature oscillator is fabricated in 65-nm CMOS technology. Fig. 11 shows the micro-photo of the chip with a core area of $630 \times 540 \mu\text{m}^2$. With a supply



(a)



(b)



(c)

Fig. 12. Measured phase noise at 10-MHz frequency offset: (a) at 7.91 GHz, (b) at 8.26 GHz, and (c) with comparison to simulation results over the entire frequency range.

voltage of 0.8 V, the proposed quadrature oscillator consumes a 34-mA dc current, which corresponds to a power consumption of 27.2 mW and is required in order to obtain a target phase noise as low as -140 dBc/Hz at 10-MHz offset.

The measured phase noise at the center frequency of 7.91 GHz is shown in Fig. 12(a). The phase noise at 10-MHz offset frequency is -143 dBc/Hz, which corresponds to an FoM of 186.6 dB. Through tuning of C_2 , the quadrature oscillator operates at different frequencies and presents a phase noise performance from -140 to -143 dBc/Hz at 10-MHz

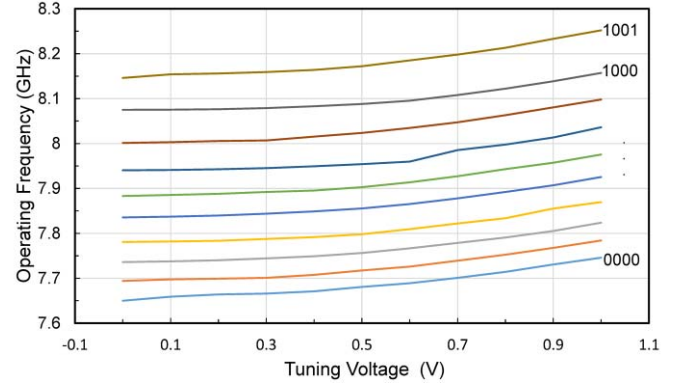


Fig. 13. Measured frequency tuning curve.

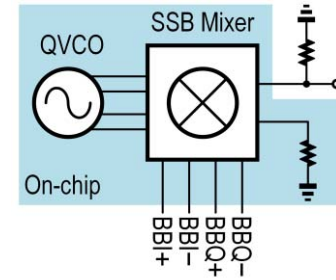


Fig. 14. Phase error measurement setup.

offset frequency. At the operating frequency of 8.26 GHz, the worst phase noise at 10-MHz offset frequency is about -140 dBc/Hz, as shown in Fig. 12(b). From Fig. 12(b), the phase noise at lower offset frequency is high, and between 300-KHz and 3-MHz offset frequency, the phase noise has a slope close to 40 dB/decade. This unexpected $1/f^4$ phase noise is observed when the highest bit switch is turned off and mainly from the SCA. As discussed in Appendix-B, although the detailed mechanism is unknown, with proper design of SCA, the generation of such phase noise can be avoided. Both the simulated phase noise and measured phase noise with different oscillation frequencies are shown in Fig. 12(c), and the optimal phase noise is measured at around 7.8 GHz. Due to the unexpected phase noise presents at higher offset frequency when the highest bit switch is turned off, the phase noise at the larger operating frequency becomes even worse than the simulation results. The measured tuning frequency with different control voltage and control bits within the desired range of capacitance ratio n is shown in Fig. 13.

We employ an on-chip passive single-sideband mixer and 40-MHz baseband IQ signals generated from a Rohde & Schwarz SMU200A for the phase error measurement. In the testing setup shown in Fig. 14, one output is connected to a spectrum analyzer to measure the single-sideband rejection ratio (SBR), while the other output is loaded with a 50- Ω on-chip resistor. From the three measured samples, the SBR ranges from -54 to -36 dB which corresponds to the phase error of 0.23° – 1.8° , and the minimum SBR measurement result is shown in Fig. 15.

The performance of the proposed QVCO is summarized in Table I and compared to state-of-the-art QVCOs.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO THE STATE-OF-THE-ART QVCOs

	Coupling Approach	CMOS Tech. (nm)	Power (mW)	Supply (V)	Freq. (GHz)	Phase Noise at 10MHz (dBc/Hz)	Phase Error (°)	FoM* (dB)	Area (mm ²)
[12]	Capacitor	130	3.2	0.8	4.5	-132	3.6	181	0.278
[10]	MOS Varactor	65	16.8	1.2	6.6	-137	<0.3	181	0.11
[11]	Diode	65	11.4	1.2	62.7	-114	0.7	180	0.039
[9]	Bidirectional Diode	65	11.8	1	26	-119	0.36	176	0.024
[8]	Transformer	180	5	1	17	-130	1.4	187.6	0.126
[24]	Transformer	65	12.3	0.6	8.2	-120.9 (1MHz)	0.7	188.4	0.38
[28]	2nd Harmonic	65	2.1	0.35	5	-137.1 (3MHz)	7	198.3	0.35
[6]	Parallel	130	4.2	1	5	-121 (1MHz)	0.6	189	0.27
This Work	Noise-Shifting	65	27.2	0.8	7.9	-143	<1.8	186.6	0.34

$$*FoM = 20\log \frac{f_{osc}}{\Delta f} - 10\log \frac{P_{DC}}{1mW} - \mathcal{L}(\Delta f) \text{ (dB)}$$

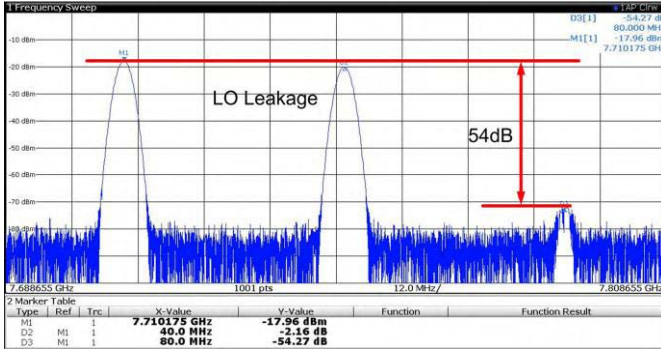


Fig. 15. Measured SBR at 7.75 GHz.

Compared to the conventional diode-coupling and capacitive-coupling QVCOs, the proposed QVCO achieves FoM of ~ 6 dB better with comparable phase error. The nonlinear capacitive coupling [10] has the most accurate I/Q phases but a poorer phase noise. From the comparison, the FoM of the proposed QVCO is close to the transformer coupling in [8] and the class-F quadrature harmonic oscillator [24]. Using harmonic oscillator design techniques [25]–[27], the class-D quadrature oscillator in [28] suffers from large phase error while achieving the lowest power and the highest FoM.

VI. CONCLUSION

A noise-shifting coupling network consuming zero-dc voltage headroom is proposed. The phase noise contribution of

the noisy coupling transistor is reduced through the capacitive feedback, and the conversion of the current noise to the phase noise is minimized by shifting the NMF and ISF to be orthogonal to each other. Transformer-feedback technique is also applied to further improve the phase noise and the phase error. Compared to the state-of-the-art QVCOs, the proposed QVCO prototype achieves at least 6 dB phase noise improvement with better or comparable other performance in terms of IQ phase error and low supply voltages.

APPENDIX

A. ISF Associated With the Coupling Transistor in Proposed Coupling Network

The ISF can be derived by the steady-state vector \vec{X} of the system [2], [15]. With an appropriate normalization factor [2], the ISF can be approximated by

$$\Gamma_i = \frac{2\pi}{T} \cdot \frac{q_{\max}}{\Delta q_i} \cdot \frac{\Delta \vec{X}_i \cdot \dot{\vec{X}}}{|\dot{\vec{X}}|^2} \quad (23)$$

where Δq_i is a current pulse applied to introduce the perturbation vector $\Delta \vec{X}_i$. For conventional quadrature oscillators, normalized waveforms across the four resonant tanks can be used [2]. In the proposed quadrature oscillator, the state vector for ISF calculation can be composed of the state variables corresponding to the voltages on the capacitors and the currents flowing through the inductors. If L_S is small and M_C is not cross connected, the coupled oscillator will

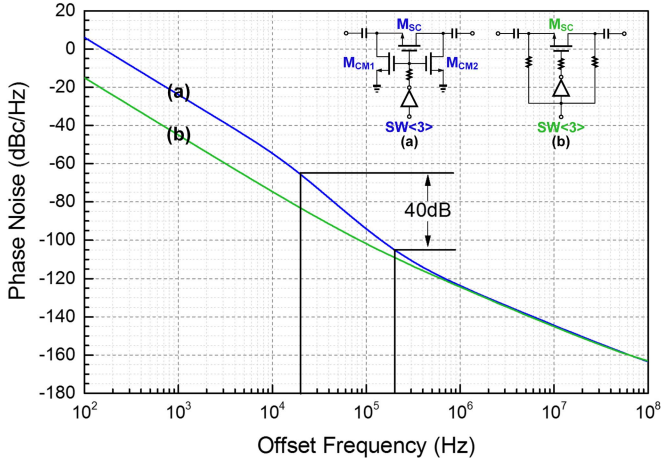


Fig. 16. Unexpected phase noise at low offset frequency.

operate through the capacitive coupling with IQ phases. In this case, the coupled oscillators resonate with the left-handed mode [13], [22]. The resonant mode can be verified by an increasing oscillation frequency when the number of coupling oscillator cells increases. However, as discussed in [9], [12], and [13] and Section I, two oscillators coupled with I/Q phases using linear capacitive coupling suffers a poor phase error performance. Thus, in this design, the left-handed resonant mode is avoided by using a relative large inductor L_S , and with large L_S the system operation is approximated as a second-order system, the first derivative of the waveform can be applied for approximation of the ISF [2], [15]. For further simplification, the phase shift of ISF [21] caused by the coupling through M_C is neglected. Using the phasor representation of I/Q voltages in steady state, $A_0 e^{j\phi}$ and $A_0 e^{j(\phi - (\pi/2))}$, the voltage across C_1 and its first derivative are given by

$$V_{C_1} = \frac{\omega_0^2 L_S C_2 - 1 - j}{\omega_0^2 L_S (C_1 + C_2) - 1} A_0 e^{j\phi} \quad (24)$$

$$\begin{aligned} \dot{V}_{C_1} &= \frac{1 + j(\omega_0^2 L_S C_2 - 1)}{\omega_0^2 L_S (C_1 + C_2) - 1} A_0 e^{j\phi} \\ &= A_0 \frac{\sqrt{1 + (\omega_0^2 L_S C_2 - 1)^2}}{\omega_0^2 L_S (C_1 + C_2) - 1} e^{j[\phi + \tan^{-1}(\omega_0^2 L_S C_2 - 1)]}. \end{aligned} \quad (25)$$

Thus, comparing $\Gamma_{I+}(\phi) = -(1/4) \cdot \sin \phi$, the ISF associated with $i_{n,DS,C}$ is approximated by

$$\begin{aligned} \Gamma_C(\phi) &= \frac{1}{4} \frac{\sqrt{1 + (\omega_0^2 L_S C_2 - 1)^2}}{\omega_0^2 L_S (C_1 + C_2) - 1} \\ &\quad \cdot \cos[\phi + \tan^{-1}(\omega_0^2 L_S C_2 - 1)]. \end{aligned} \quad (26)$$

B. Low-Frequency Noise From the Coupling Network

Through (amplitude modulation) AM-to-PM (phase modulation) conversion and Groszkowski effect [29], the low-frequency noise is converted to the phase noise at low offset frequencies. In this paper, the low-frequency noise is expected to be low owing to the orthogonality of the ISF and NMF

phases [29], and the reduced magnitude of ISF. However, in the SCA, if the small-size transistors, $M_{CM1,2}$, in the schematic shown in Fig. 16(a) used to define the common mode (CM) level are turned on by duration of the oscillation period, it would also contribute to significant phase noise at a lower offset frequency. This case is prone to occur when the voltage swing below ground and the highest bit switch is turned off. Thus, the drain and source voltages of the switch M_{SC} can also have a voltage swing below ground. From the simulated result shown in Fig. 16, the unexpected $1/f^4$ phase noise, with a 40 dB/decade decay of the phase noise from 20- to 200-KHz offset frequency, is between the $1/f^3$ and $1/f^2$ region. From the noise summary, the unexpected phase noise is contributed by the thermal noise of $M_{CM1,2}$. The mechanism is still unknown, but to avoid this unexpected phase noise, instead of using $M_{CM1,2}$ to define the CM level of the switch, a large resistor can be used to connect the switch source/drain node and the control bit input, as shown in Fig. 16(b). From the simulation results, the $1/f^4$ phase noise disappears and the low-frequency noise is dominated by coupling transistors and the cross-coupled pair in each oscillator cell.

REFERENCES

- [1] B. Razavi, *RF Microelectronics*, 2nd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 2011.
- [2] P. Andreani and X. Wang, "On the phase-noise and phase-error performances of multiphase LC CMOS VCOs," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1883–1893, Nov. 2004.
- [3] A. Rofougaran, J. Rael, M. Rofougaran, and A. Abidi, "A 900 MHz CMOS LC-oscillator with quadrature outputs," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 1996, pp. 392–393.
- [4] J. V. D. Tang, P. V. D. Ven, D. Kasperkovitz, and A. V. Roermund, "Analysis and design of an optimally coupled 5-GHz quadrature LC oscillator," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 657–661, May 2002.
- [5] A. Mirzaei, M. E. Heidari, R. Bagheri, S. Chehrizi, and A. A. Abidi, "The quadrature LC oscillator: A complete portrait based on injection locking," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1916–1932, Sep. 2007.
- [6] Y.-C. Lo and J. Silva-Martinez, "A 5-GHz CMOS LC quadrature VCO with dynamic current-clipping to improve phase noise and phase accuracy," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 7, pp. 2632–2640, Jul. 2013.
- [7] P. Andreani, A. Bonfanti, L. Romano, and C. Samori, "Analysis and design of a 1.8-GHz CMOS LC quadrature VCO," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1737–1747, Dec. 2002.
- [8] A. W. L. Ng and H. C. Luong, "A 1-V 17-GHz 5-mW CMOS quadrature VCO based on transformer coupling," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1933–1941, Sep. 2007.
- [9] N. C. Kuo, J. C. Chien, and A. M. Niknejad, "Design and analysis on bidirectionally and passively coupled QVCO with nonlinear coupler," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 4, pp. 1130–1141, Apr. 2015.
- [10] K. Bhardwaj, S. Seth, B. Murmann, and T. H. Lee, "A 0.11 mm², 5.7-to-6.7 GHz, parametrically pumped quadrature LC-VCO with digital outputs," in *Proc. Symp. VLSI Circuits (VLSIC)*, Jun. 2013, pp. C138–C139.
- [11] X. Yi, C. C. Boon, H. Liu, J. F. Lin, J. C. Ong, and W. M. Lim, "A 57.9-to-68.3 GHz 24.6 mW frequency synthesizer with in-phase injection-coupled QVCO in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 56, Feb. 2013, pp. 354–355.
- [12] C. T. Fu and C. Howard, "A 0.8-V CMOS quadrature LC VCO using capacitive coupling," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2007, pp. 436–439.
- [13] G. Li and E. Afshari, "A low-phase-noise multi-phase oscillator based on left-handed LC-ring," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1822–1833, Sep. 2010.

- [14] B. Jiang, C. Chen, J. Ren, and H. C. Luong, "A 7.9-GHz transformer-feedback quadrature VCO with a noise-shifting coupling network," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2016, pp. 353–356.
- [15] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.
- [16] P. Andreani, X. Wang, L. Vandi, and A. Fard, "A study of phase noise in colpitts and LC-tank CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1107–1118, May 2005.
- [17] S. Levantino, P. Maffezzoni, F. Pepe, A. Bonfanti, C. Samori, and A. L. Lacaita, "Efficient calculation of the impulse sensitivity function in oscillators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 10, pp. 628–632, Oct. 2012.
- [18] A. Demir, A. Mehrotra, and J. Roychowdhury, "Phase noise in oscillators: A unifying theory and numerical methods for characterization," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 47, no. 5, pp. 655–674, May 2000.
- [19] S. Levantino and P. Maffezzoni, "Computing the perturbation projection vector of oscillators via frequency domain analysis," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 31, no. 10, pp. 1499–1507, Oct. 2012.
- [20] R. Aparicio and A. Hajimiri, "A noise-shifting differential colpitts VCO," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1728–1736, Dec. 2002.
- [21] P. Andreani, "A time-variant analysis of the $1/f^2$ phase noise in CMOS parallel LC-tank quadrature oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 8, pp. 1749–1760, Aug. 2006.
- [22] A. H. T. Yu *et al.*, "A dual-band millimeter-wave CMOS oscillator with left-handed resonator," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 5, pp. 1401–1409, May 2010.
- [23] K. Kwok and H. C. Luong, "Ultra-low-voltage high-performance CMOS VCOs using transformer feedback," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 652–660, Mar. 2005.
- [24] H. Jia, B. Chi, and Z. Wang, "An 8.2 GHz triple coupling low-phase-noise class-F QVCO in 65 nm CMOS," in *Proc. 41th Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2015, pp. 124–127.
- [25] M. Babaie and R. B. Staszewski, "A class-F CMOS oscillator," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3120–3133, Dec. 2013.
- [26] L. Fanori and P. Andreani, "Class-D CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3105–3119, Dec. 2013.
- [27] A. Mazzanti and P. Andreani, "Class-C harmonic CMOS VCOs, with a general result on phase noise," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2716–2729, Dec. 2008.
- [28] A. G. Roy, S. Dey, J. B. Goins, T. S. Fiez, and K. Mayaram, "350 mV, 5 GHz class-D enhanced swing differential and quadrature VCOs in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 1833–1847, Aug. 2015.
- [29] F. Pepe, A. Bonfanti, S. Levantino, C. Samori, and A. L. Lacaita, "Analysis and minimization of flicker noise up-conversion in voltage-biased oscillators," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 6, pp. 2382–2394, Jun. 2013.



Bingwei Jiang received the B.Eng. degree in electronic science and technology from the University of Electronic Science and Technology of China, Chengdu, China, in 2011, and the M.Eng. degree in circuit and system from Southeast University, Nanjing, China, in 2014.

He is currently with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, where he is involved in frequency generation circuit design and its applications.



Howard C. Luong (F'14) received the B.S., M.S., and Ph.D. degrees in electrical engineering and computer sciences from the University of California, Berkeley, CA, USA, in 1988, 1990, and 1994, respectively.

Since 1994, he has been with the Faculty of Electrical and Electronics Engineering, The Hong Kong University of Science and Technology, Hong Kong, where he is currently a Professor. He has co-authored three technical books: *Design Techniques for Transformer-Based VCOs and Frequency*

Dividers, *Low-Voltage RF CMOS Frequency Synthesizers*, and *Design of Low-Voltage CMOS Switched-Opamp Switched-Capacitor Systems*. His current research interests include RF and analog integrated circuits and systems for wireless and portable applications.

Dr. Luong was an IEEE Solid-State Circuits Society Distinguished Lecturer from 2012 to 2014, and an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I (TCAS-I) AND TCAS-II from 1999 to 2002 and from 2010 to 2012. He is currently serving as an Associate Editor of the IEEE VIRTUAL JOURNAL ON RFIC and a Technical Program Committee Member of the IEEE International Solid-State Circuits Conference and the IEEE Custom Integrated Circuits Conference.