A Performance-Aware Low-Quiescent Headphone Amplifier in 65-nm CMOS

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***Abstract*— A low-quiescent high-performance class-AB headphone amplifier is presented. The effect of the input-referred offset on the quiescent power of audio power amplifier (APA) that drives very small resistive load is described and analyzed. A digitally assisted offset calibration-based APA topology together with improved frequency compensation is proposed. This permits the use of low quiescent power and small compensation capacitance. Implemented in 65-nm CMOS technology, the amplifier occupies an area of 0.15 mm^2 and consumes 0.4 mW at ±1 V supplies. At the load of 16 Ω//200 pF, the gain–bandwidth product is 1.78 MHz using a total compensation capacitance of 8.5 pF. Other performance metrics are measured with −89-dB total harmonic distortion (THD+N), 93.5-dB signal-to-noise ratio, 84-dB power supply rejection ratio (PSRR+), and 105-dB PSRR− @217 Hz. It can deliver a peak power of 35 mW (1.5 V_{pp} swing) to the above load, yielding the best figure-of-merit (FOM) = (peak load power/quiescent power) and the best FOM2 = [peak load power/quiescent power ∗ (THD+N)%] with respect to other reported representative works.**

***Index Terms*— Audio power amplifier (APA), class-AB amplifier, frequency compensation, headphone amplifier, input-referred offset, low-quiescent power, offset calibration.**

I. Introduction

In RECENT years, the demand for the battery-powered devices has been increasing rapidly. At the same time, the requirements for the headphone amplifier also extend to hi-fi quality music playback. In order to achieve high run time per charge for the portable devices, the quiescent power of amplifier should be made as low as possible [1]. As such, the quiescent power becomes one of the most important items in the design agenda. Compared with the switching amplifier (i.e., class-D amplifier), the linear amplifier has the key advantages of high power supply rejection ratio (PSRR), low total harmonic distortion plus noise (THD+N), no switching noise, and no electromagnetic interference [2]–[4]. With the continual decrease in device sizes and supply voltage in nanometer CMOS technologies, the per-stage gain decreases, and multistage amplifier topologies are required to achieve sufficient dc gain and linearity. This is of another key concern in the circuit topology for driving very low resistive load in audio amplifier. Fig. 1 shows the foundation circuit topology for portable headphone applications [5]. It is largely based on differential inputs with single-ended output to drive the headphone load. In addition, the commercial headphone amplifiers should be able to drive the cable capacitance with at least few hundreds of picofarad or above [6]–[8]. Therefore, the frequency compensation technique is important to be addressed in low-quiescent audio power amplifier (APA) design in the context of low resistive load in parallel with high capacitive load.

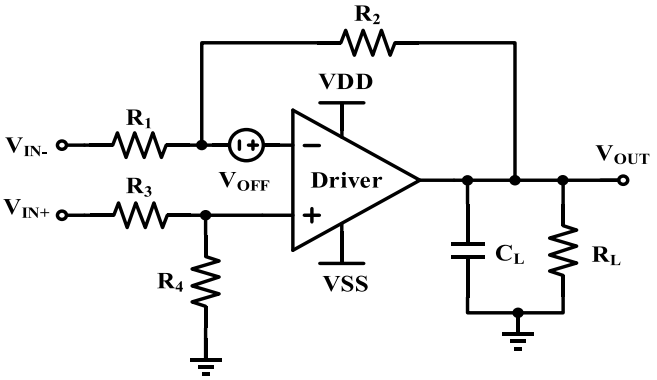

Fig. 1. Configuration of headphone amplifier with differential inputs and input-referred offset.

This paper is organized as follows. Section II reviews the low-quiescent headphone amplifier design issues. Section III presents the proposed low-quiescent power design techniques, which include a digitally assisted offset calibration circuit and an improved frequency compensation in Type-II realization. This is called nested Miller compensation with feedforward stage and nulling resistors (NMCFNR2). Section IV describes the details pertaining to the transistor level implementation of class-AB amplifier. The measurement results of the fabricated prototype are discussed in Section V. Finally, the concluding remarks are given in Section VI.

II. Low-Quiescent Headphone Amplifier Design Issues

The quiescent power of class-AB headphone amplifier is significantly dictated by the topology of the core amplifier, frequency compensation technique, and the quiescent current control circuit for class-AB push–pull stage [9]–[13]. On top of that, the target specifications arising from the input-referred noise, the amount of open-loop gain and so forth also demand certain level of quiescent power. Of particular interests, several class-AB headphone amplifiers having good

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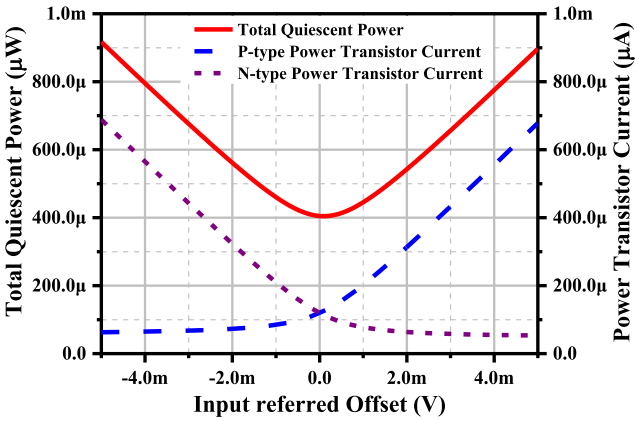

Fig. 2. Total quiescent power and output transistor current versus the input-referred offset of an exemplary headphone amplifier in this paper.

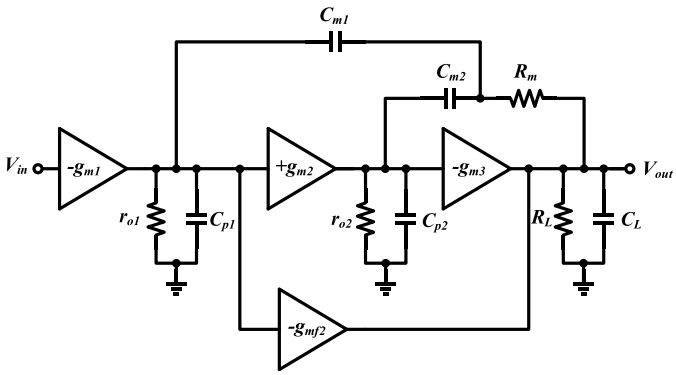

Fig. 3. Topology of the three-stage NMCFNR amplifier.

performance in PSRR, THD and signal-to-noise ratio (SNR) were reported in [5] and [13]–[17]. However, they suffer from high quiescent power consumption. This raises the motivation for the design of low-quiescent headphone amplifier while providing comparable performance metrics with respect to the reported works.

A. Input-Referred Offset in Headphone Amplifier

When the APA is used to drive very low resistive load in direct-coupled topology, the input offset of amplifier system becomes the design problem, because it plays another part of contributions to the quiescent power. In particular, this becomes a significant issue when the amplifier is targeted for low-quiescent specifications in nanometer CMOS technology [12], which is subject to the increase of mismatch with the decrease of device channel length. Refer to Fig. 1, in the presence of input-referred offset, the output voltage is obtained as

$$V_{\mathrm{OUT}} = \frac{R_2 + R_4}{R_1 + R_3}(V_{\mathrm{IN}+} - V_{\mathrm{IN}-}) - \left(\frac{R_2 + R_4}{R_1 + R_3} + 1\right) V_{\mathrm{OFF}} \tag{1}$$

where the symbols have their usual meanings. When the four resistors are assumed identical in design, the input offset will be amplified by two times. Using the proposed amplifier (to be described in Section III and Section IV) as an illustration example, Fig. 2 shows the variations of the amplifier's output stage current and the amplifier's quiescent power against the change of input-referred offset. As can be observed, both the output stage current and the quiescent power will increase sharply with the increase of offset voltage. In practical amplifier design and layout, a typical output offset ranging from a few millivolts to 10 mV is possible, depending upon the closed-loop gain and the layout matching issue.

In order to achieve high-precision APAs, the trimming technique can be implemented to calibrate the input-referred offset. Compared with the dynamic offset cancellation techniques, the trimming technique is easy to implement and it will not introduce switching noise which may degrade the audio quality. Many state-of-the-art works which employed trimming techniques in [18]–[21] provide an efficient method to reduce the offset. However, the bulk voltage trimming in [18] and [19] may suffer from the reliability issue due to the possibility of latch up from the forward-biased body of MOSFET transistors. This turns out that the current control offset calibration [20], [21] is preferred to minimize the input-referred offset on the basis of simplicity. Regarding the unbalanced single-ended current injection [20], it can degrade the PSRR. The active resistor load trimming [21] with ping-pong topology for continuous-time offset calibration will introduce potential switching noise and increase the area and power by two times.

B. Frequency Compensation Techniques in Headphone Amplifier

The frequency compensation scheme plays the key role in multistage amplifier design. The NMC amplifier [11], [22] is the foundation circuit, which serves as the benchmark for other multistage amplifiers. Unfortunately, an NMC amplifier suffers from the bandwidth reduction, many frequency compensation techniques have been reported in [23]–[28] to improve the power-bandwidth efficiency. They can be applied in three-stage class-AB headphone amplifier to extend its gain–bandwidth product (GBW). Among the amplifiers, the NMCFNR topology [24] is preferred due to its low power topology using the nulling resistor method. The topology of three-stage NMCFNR amplifier is shown in Fig. 3. The small-signal analysis of its usage as the headphone amplifier is similar to that of the capacitive driven op-amp except that the third-stage gain of headphone amplifier tends to be small due to very low resistive load. The output resistances, equivalent transconductance, and

$$A(s) = \frac{g_{m1}g_{m2}g_{m3}r_{o1}r_{o2}R_L\left(1 + s\left(R_m(C_{m1} + C_{m2}) + \frac{(g_{mf2} - g_{m2})C_{m2}}{g_{m2}g_{m3}}\right) + s^2\frac{(g_{mf2} + g_{m3})R_mC_{m1}C_{m2}}{g_{m2}g_{m3}}\right)}{(1 + sC_{m1}g_{m2}g_{m3}r_{o1}r_{o2}R_L)\left(1 + s\frac{(g_L + g_{m3})C_{m2} - g_{m2}g_LR_mC_{m2}}{g_{m2}g_{m3}} + s^2\frac{C_{m2}C_L - g_{m2}R_mC_{m2}C_L}{g_{m2}g_{m3}}\right)} \tag{2}$$

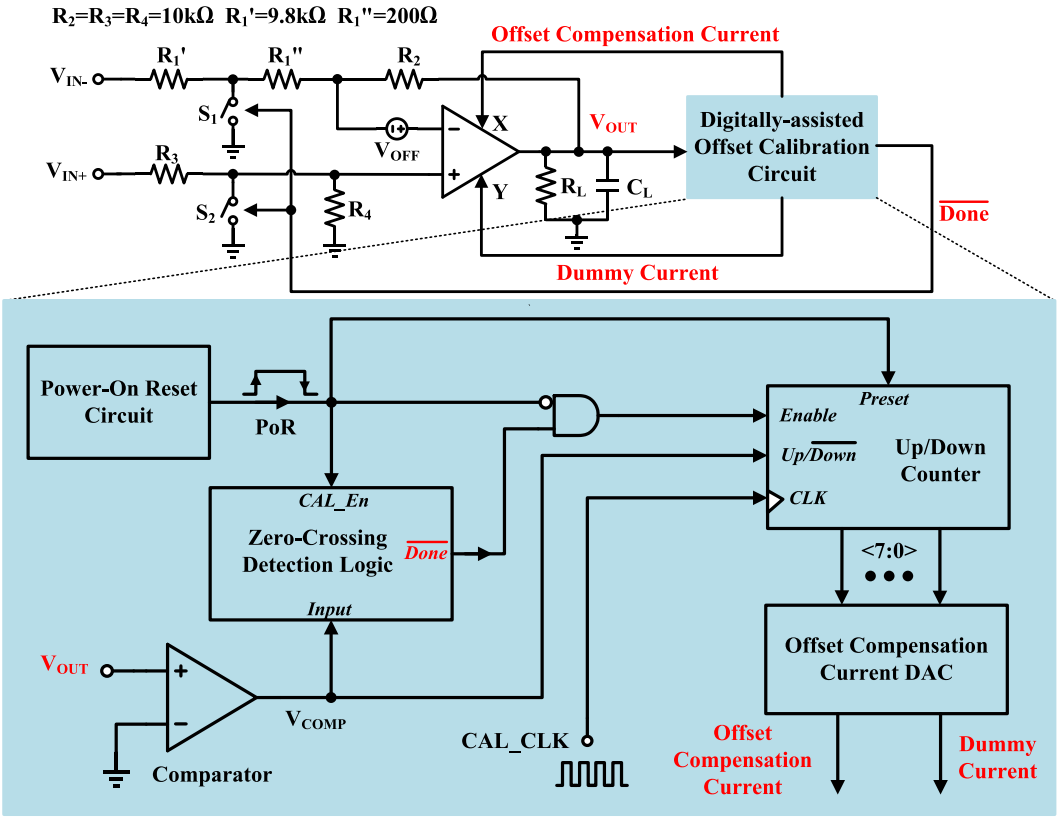

Fig. 4. Headphone amplifier with the proposed digitally assisted offset calibration circuit.

lumped parasitic capacitances of each gain stage are denoted by r_{oi}, g_{mi}, and C_{pi}, respectively. C_{m1} and C_{m2} are the Miller capacitors. R_m and R_L are the nulling resistor and resistive load, respectively. Assume that the gain for the first and second stages is much larger than one and C_L, $C_{mi} \gg C_{pi}$, the transfer function of NMCFNR headphone amplifier is shown in (2), shown at the bottom of the previous page.

Since the nondominant high-frequency zeros and poles are far away from the unity-gain frequency (UGF), one can obtain the first zero and second pole as follows:

$$z_1 = \frac{-g_{m2}g_{m3}}{g_{m2}g_{m3}R_m(C_{m1}+C_{m2}) + (g_{mf2}-g_{m2})C_{m2}} \quad (3)$$

$$p_2 = \frac{-g_{m2}g_{m3}}{(g_L+g_{m3})C_{m2} - g_{m2}g_L R_m C_{m2}}. \quad (4)$$

For the feedforward transconductance $g_{mf2} > g_{m2}$ in (3), the left-half-plane (LHP) zero is created. The price paid for the large g_{mf2} is that it will increase the power consumption. If $g_{mf2} < g_{m2}$ is made for low-power criteria, the control of LHP zero will rely on the increased value of nulling resistor R_m [24]. However, the disadvantage is that the LHP pole in (4) has the possibility to become a right-half-plane (RHP) pole when there is a substantial increase of the product $g_L R_m$. To avoid the formation of RHP pole and permit the better placement of the second pole close to the first zero, a three-stage NMCFNR headphone amplifier will be resorted to the trade off design among the extra power needed for g_{mf2} and the allowable resistance range of R_m. As a result, the constraint value for R_m will result in the decrease of the GBW. The outcome is the increase of Miller compensation capacitors, C_{m1} and C_{m2}, to guarantee the stability if low-power design is of concern.

III. Proposed Low-Quiescent Headphone Amplifier Design Techniques

The effect of the input-referred offset and frequency compensation issue on the impact of quiescent power in the class-AB headphone amplifier have been described and analyzed in Section II. In order to minimize the power and offer good performance metrics, two low-quiescent design techniques are proposed.

A. Digitally Assisted Offset Calibration Circuits

Fig. 4 shows the basic circuit blocks for the proposed offset calibration circuit in the APA system. During the offset calibration mode, the amplifier is set to the default dc gain of 51 to amplify the input offset, so that the resolution is not significantly degraded by the comparator's offset.

The offset calibration automatically starts at the beginning of power-up action with the Power-on Reset (PoR) signal going logic high. At this juncture, the zero-crossing detection logic sets "$\overline{\text{Done}}$" to be high to close the switches S_1 and S_2. Meanwhile, the up–down-counter is preset with the middle logic output value of 10 000 000. When the PoR signal goes low, it activates up–down-counter which is driven by the calibration clock of 50 kHz in the offset calibration. The input

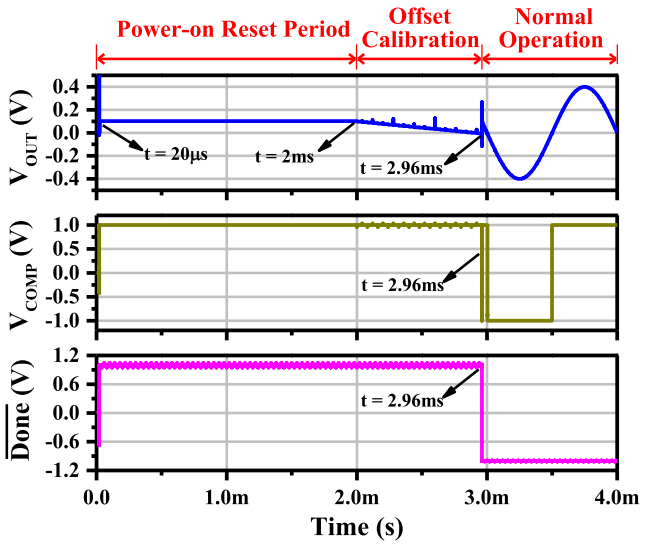

Fig. 5. Simulated transient response of the important signals in the offset calibration system.

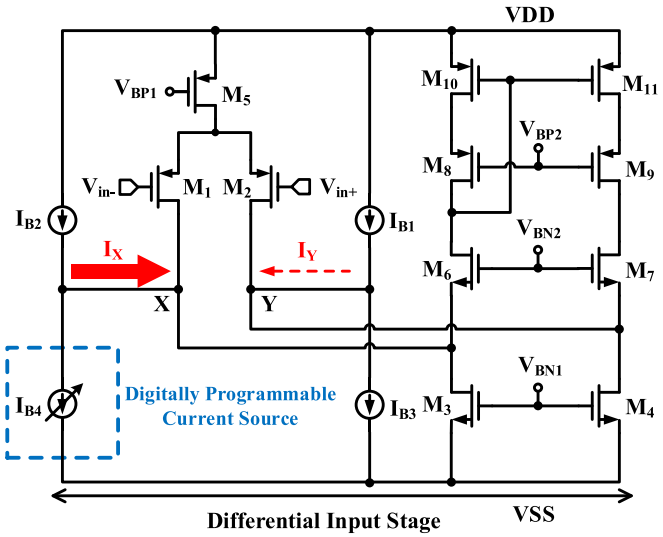

Fig. 6. Concept of the proposed offset compensation current injected into differential input stage.

offset is digitally calibrated by adjusting the injected current. The calibration direction is determined by the up/$\overline{\text{down}}$ control signal. Upon detecting the terminating transition at the input of zero-crossing detection logic, the "$\overline{\text{Done}}$" output signal is asserted low to disable the counter. At this time, the headphone amplifier starts to enter the normal operation mode.

Fig. 5 shows the simulated transient responses of the key signals in the offset calibration system. The zoomed-in view of the output signal shows that V_{OUT} settles to the value of -4.1 mV. This is translated to the input offset voltage of -80.4 μV based on the closed-loop gain of 51 in offset calibration mode. For V_{COMP}, there exist several transitions which come from the system start-up, the end of offset calibration, and the switching toward normal operation mode.

Fig. 6 shows the concept of offset compensation current and the dummy current injected into the differential stages.

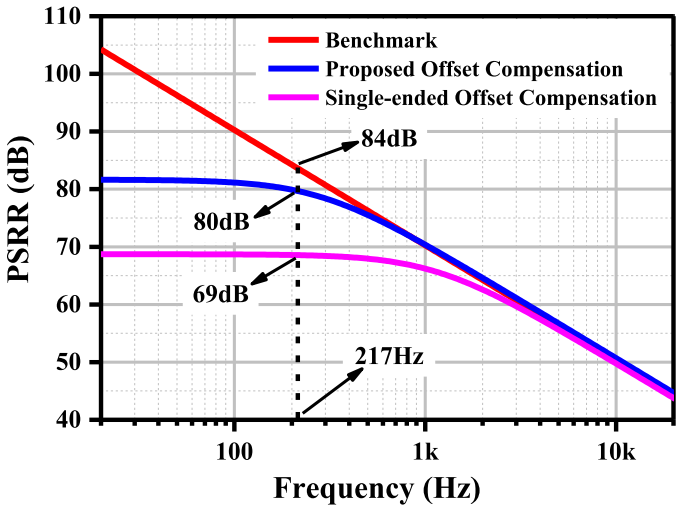

Fig. 7. Simulated PSRR for the proposed offset compensation circuit and the conventional counterpart with respect to the benchmark.

I_{B1}–I_{B3} represent three identical constant current sources. I_{B4} is a digitally programmable current source, which can be varied from 0 to 5.12 μA through the digital outputs of the up–down-counter. The theoretical resolution of the compensated input-referred offset can be obtained as follows:

$$V_{\text{OFFmin}} = \frac{I_{B4}}{2^N * g_{m1}}. \tag{5}$$

For an 8-bit current DAC and the differential input stage transconductance $g_{m1} = 234$ μS, the resolution of compensated input-referred offset is about 85 μV. The stacked dummy current sources, I_{B1} and I_{B3}, establish a close-level impedance from the right-hand side with respect to that of the stacked current sources in the left-hand side. Therefore, the current I_Y is almost zero. This current injection topology has offered two key advantages. First, since the high-impedance offset compensation current sources are injected into two low-impedance nodes of folded-cascode input stage, it will not significantly degrade the gain of first stage. Second, the dummy branch provides an additional supply noise counteract path for the differential input stage, hence reducing the degradation of PSRR in amplifier. Fig. 7 shows the comparative PSRR simulation results for the single-ended current injection circuit based on the proposed work and the conventional counterpart [20] with respect to the benchmark amplifier (Fig. 14) without current injection circuit. After the maximum input offset is calibrated, the amplifier using the conventional circuit technique drops by 15 dB in PSRR with reference to that of the benchmark. However, the proposed circuit with dummy branch only drops by 5 dB in PSRR, confirming that the dummy branch to reduce the supply noise.

B. Improved Frequency Compensation Topology

Refer to the multipath NMC amplifier in [11] and [28], it requires the substantial increase of g_{mf1} in order to push the first zero close to the second pole. Unfortunately, it may lead to large power consumption if the second pole is located at low frequency. Fig. 8 shows the improved frequency compensation

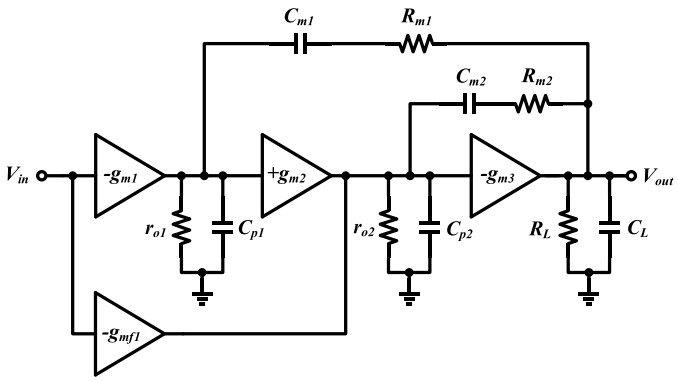

Fig. 8. Topology of the proposed three-stage NMCFNR2 amplifier.

topology, called NMCFNR2, which is the Type-II implementation of NMCFNR amplifier. It utilizes the nulling resistors to serve as the main assist for pushing the first LHP zero to low frequency. As a result, it permits low quiescent bias for the feedforward transconductance g_{mf1} in NMCFNR2 amplifier, thus saving power consumption. Comparing this topology with that of NMCFNR, the separate nulling resistor and capacitor compensation network replaces the merged compensation network. Besides, the feedforward transconductance stage is rearranged across the first and second gain stages instead of that across the second and third gain stages. Based on the same assumptions in Section II, the transfer function of NMCFNR2 amplifier is obtained and shown in (6), which is shown at the bottom of this page.

With other nondominant zeros and poles outside the UGF, the first zero and the second pole of NMCFNR2 amplifier are given as

$$z_1 = \frac{-g_{m1}g_{m2}}{g_{m1}g_{m2}\left(R_{m1}C_{m1} + R_{m2}C_{m2}\right) + g_{mf1}C_{m1}} \tag{7}$$

$$p_2 = \frac{-g_{m2}g_{m3}}{(g_L + g_{m3})C_{m2} + g_{m2}g_{m3}R_{m2}C_{m2}}. \tag{8}$$

Refer to (7) and (8), there is no negative sign in respective denominator for the first zero and the second pole. This indicates that LHP zero and LHP pole are valid for all design conditions. This turns out that there is no possibility to generate the RHP pole in the NMCFNR2 amplifier. As such, the location of the first zero can be designed with larger freedom through the choice of nulling resistors R_{m1} and R_{m2}, and the feedforward transconductance g_{mf1}. It is apparent that no significant restriction using larges values for R_{m1} and R_{m2}. This supports low-power design strategy. For instance, z_1 can be made small with small value of g_{mf1} and large values of the nulling resistors without creating the RHP pole as implied in (4). Besides, the rearrangement of feedforward topology in APA design causes $g_{mf1}C_{m1}/g_{m1}g_{m2}$ in (7) $>$ $(g_{mf2} - g_{m2})C_{m2}/g_{m2}g_{m3}$ in (3). Therefore, relative smaller Miller capacitor C_{m1} can be employed for defining the first LHP zero location according to (7). This gives the advantages of small compensation capacitance as well as improved GBW.

Fig. 9 shows the simulated open-loop gain and phase responses with different nulling resistors for the NMCFNR2 and NMCFNR amplifiers. They are based on the fixed Miller capacitors ($C_{m1} = 4.91$ pF and $C_{m2} = 1.78$ pF in NMCFNR2 and $C_{m1} = 20.7$ pF and $C_{m2} = 2.5$ pF in NMCFNR) and the load of 16 Ω//200pF. The results have validated that the large nulling resistors in NMCFNR amplifier will introduce the RHP pole, causing the stability problem. Compared with the NMCFNR counterpart, the NMCFNR2 amplifier can improve the phase margin (PM) with large nulling resistive values whilst providing adequate gain margin (GM).

Table I lists the calculated value for each pole and zero under two frequency compensation schemes in the APA design. In order to achieve a PM of 60° at the identical power, the design parameters are that $R_m = 5$ kΩ and $C_{m1} = 20.7$ pF are used in NMCFNR amplifier, whereas $R_{m1} = 15$ kΩ, $R_{m2} = 14$ kΩ, and$C_{m1} = 4.91$ pF are used in NMCFNR2 amplifier. Due to the constraint of the second pole location in NMCFNR amplifier, R_m cannot be made too large, and hence, the large value of C_{m1} is needed to push LHP zero to low frequency for partial cancellation of the second pole. Turning to the NMCFNR2 amplifier, smaller Miller capacitor C_{m1} and relatively larger nulling resistors, R_{m1} and R_{m2}, can be used to enhance the GBW in low-power design. The simulation results have confirmed that the GBW of NMCFNR and NMCFNR2 is 0.614 and 1.777 MHz, respectively, at identical quiescent power and PM. In order to evaluate the stability, the process Monte Carlo simulations are conducted for the two amplifiers and their histograms for PM and GM are shown in Fig. 10. It has revealed that the improved frequency compensation is robust against the process variation. Fig. 11 shows the simulated PM for $R_L = 16$, 32, and 50 Ω under different C_L values. Since large C_L will push p_3 in NMCFNR2 amplifier close to the UGF, the PM will decrease with the increase of C_L. Observing the PM relationship with R_L and C_L, the PM is regarded as the tradeoff design parameter between the two variables.

A headphone load will display both inductive and capacitive effects in a form of resonant circuit, which is reported as the approximated headphone load model [29]. In this design, the impedance of 16-Ω headphone model, having a resonant frequency of 2 MHz, is adopted. The circuit model is shown in Fig. 12, with $R_A = 5$ Ω, $C_L = 332$ pF, $R_L = 17$ Ω, $R_B = 340$ Ω, and $L_L = 20$ μH. To assess the stability, Fig. 13 shows the simulated open-loop gain and phase responses of amplifier with the approximated headphone load, yielding GBW = 6.7 MHz, PM = 41°, and GM = 9.5 dB. This amplifier system is considered stable because of having adequate GM. Of particular interest, the GBW is enhanced due to the additional high-frequency zero caused by the

$$A(s) = \frac{g_{m1}g_{m2}g_{m3}r_{o1}r_{o2}R_L\left(1 + s\left(R_{m1}C_{m1} + R_{m2}C_{m2} + \frac{g_{mf1}C_{m1}}{g_{m1}g_{m2}}\right) + s^2\left(R_{m1}R_{m2}C_{m1}C_{m2} + \frac{g_{mf1}R_{m2}C_{m1}C_{m2}}{g_{m1}g_{m2}}\right)\right)}{\left(1 + sC_{m1}g_{m2}g_{m3}r_{o1}r_{o2}R_L\right)\left(1 + s\frac{(g_{m3}+g_L)C_{m2}+g_{m2}g_{m3}R_{m2}C_{m2}}{g_{m2}g_{m3}} + s^2\frac{C_{m2}C_L}{g_{m2}g_{m3}}\right)} \tag{6}$$

TABLE I
COMPARISON OF POLES AND ZEROS FOR TWO FREQUENCY COMPENSATION TECHNIQUES WITH ESTIMATED CALCULATION VALUES

NMCFNR2			
Poles	**Pole frequency**	**Zeros**	**Zero frequency**
$p_{-3dB}=\dfrac{-1}{C_{m1}g_{m2}g_{m3}r_{o1}r_{o2}R_L}$	-13.5Hz	–	–
$p_2=\dfrac{-g_{m2}g_{m3}}{(g_L+g_{m3})C_{m2}+g_{m2}g_{m3}R_{m2}C_{m2}}$	-0.305MHz	$z_1=\dfrac{-g_{m1}g_{m2}}{g_{m1}g_{m2}\left(R_{m1}C_{m1}+R_{m2}C_{m2}\right)+g_{mf1}C_{m1}}$	-0.833MHz
$p_3=\dfrac{-((g_L+g_{m3})C_{m2}+g_{m2}g_{m3}R_{m2}C_{m2})}{C_{m2}C_L}$	-7.53MHz	$z_2=\dfrac{-(g_{m1}g_{m2}\left(R_{m1}C_{m1}+R_{m2}C_{m2}\right)+g_{mf1}C_{m1})}{g_{m1}g_{m2}R_{m1}R_{m2}C_{m1}C_{m2}+g_{mf1}R_{m2}C_{m1}C_{m2}}$	-4.32MHz
NMCFNR			
Poles	**Pole frequency**	**Zeros**	**Zero frequency**
$p_{-3dB}=\dfrac{-1}{C_{m1}g_{m2}g_{m3}r_{o1}r_{o2}R_L}$	-3.2Hz	–	–
$p_2=\dfrac{-g_{m2}g_{m3}}{\left(g_L+g_{m3}\right)C_{m2}-g_{m2}g_LR_mC_{m2}}$	-0.476MHz	$z_1=\dfrac{-g_{m2}g_{m3}}{g_{m2}g_{m3}R_m\left(C_{m1}+C_{m2}\right)+\left(g_{mf2}-g_{m2}\right)C_{m2}}$	-1.124MHz
$p_3=\dfrac{-((g_L+g_{m3})C_{m2}-g_{m2}g_LR_mC_{m2})}{C_{m2}C_L-g_{m2}R_mC_{m2}C_L}$	-5.374MHz	$z_2=\dfrac{-(g_{m2}g_{m3}R_m\left(C_{m1}+C_{m2}\right)+\left(g_{mf2}-g_{m2}\right)C_{m2})}{\left(g_{mf2}+g_{m3}\right)R_mC_{m1}C_{m2}}$	-5.535MHz

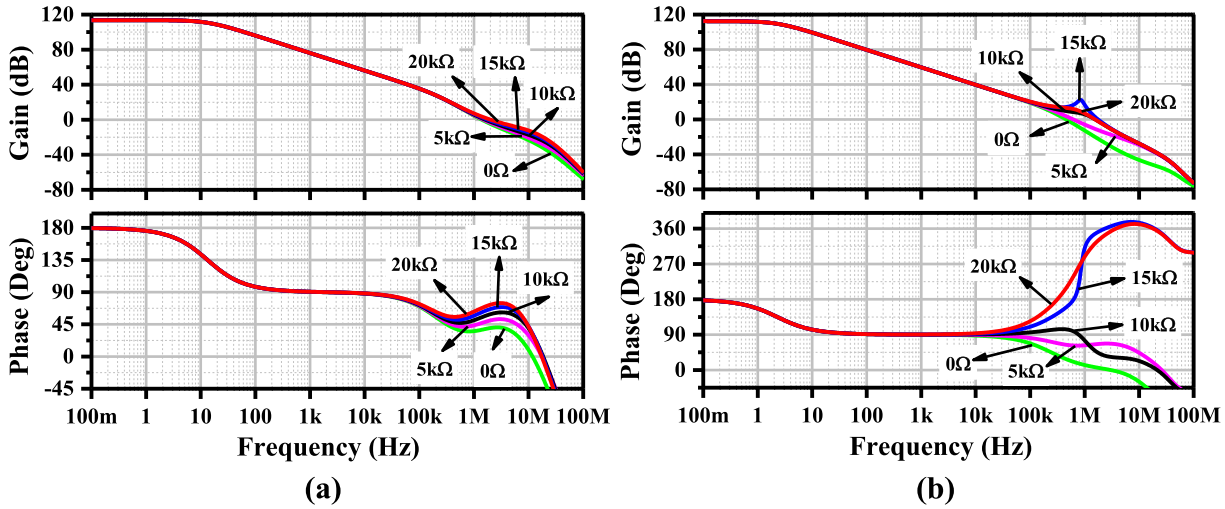

Fig. 9. Simulated open-loop gain and phase with different nulling resistors for (a) NMCFNR2 amplifier and (b) NMCFNR amplifier.

inductive effect. To further improve the PM by 10° at the expense of silicon area, a 20 pF can be added across the feedback resistor R_2 in Fig. 4.

The simulation result of NMCFNR2 amplifier correlates well with the theory. Due to the relaxation in the design tradeoff, this explains why the GBW can be enhanced with the improved scheme.

IV. REALIZATION OF THE PROPOSED HEADPHONE AMPLIFIER

The proposed class-AB headphone amplifier is shown in Fig. 14, which consists of a folded-cascode differential input stage, a noninverting gain stage, and a push–pull output stage. The detailed design considerations of each stage are discussed in Sections IV-A–IV-C.

A. Input Stage

The first stage is realized using folded-cascode topology, which is formed by transistors M_1–M_{11}. The topology can provide an enhanced output resistance, resulting in a higher dc gain. The input stage determines many performance metrics of an amplifier, including input-referred offset, input-referred noise, GBW, dc gain, and so forth. In order to obtain high current efficiency of transconductance, the input pair M_1 and M_2 are biased in the subthreshold region with large aspect ratios. The transconductance for current source pair

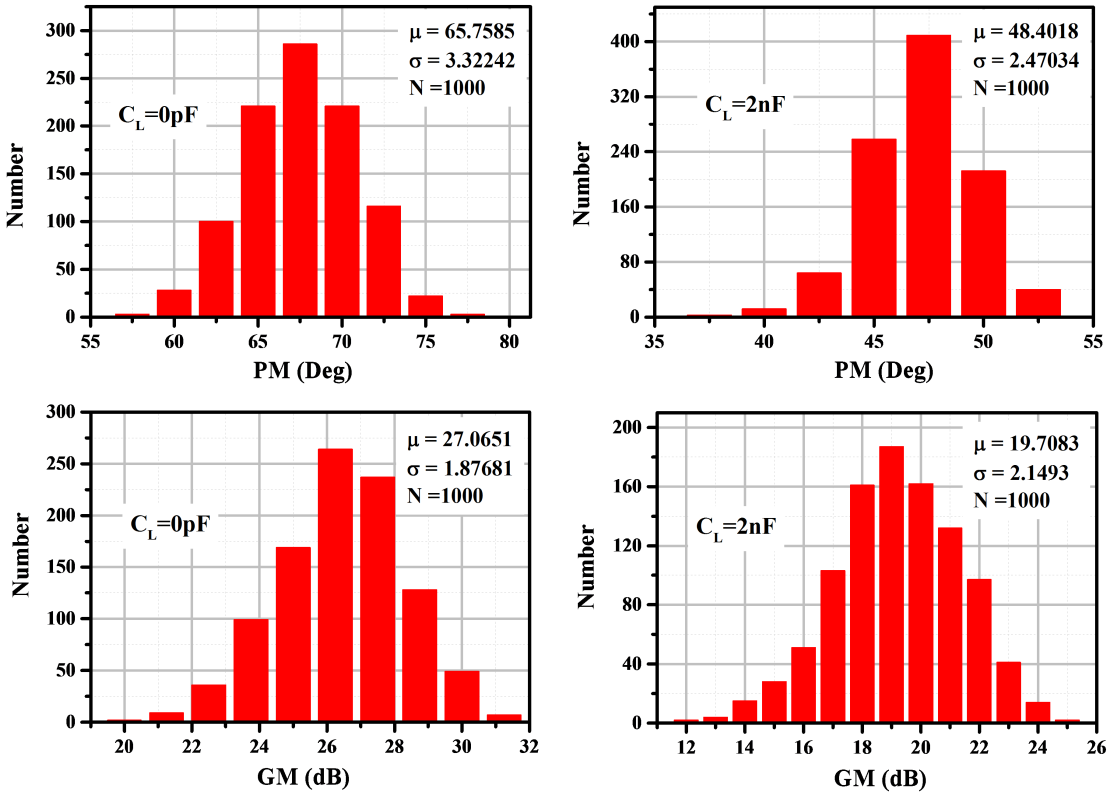

Fig. 10. Process Monte Carlo histograms for PM and GM with the respective load of 16Ω//0pF and 16 Ω/2 nF.

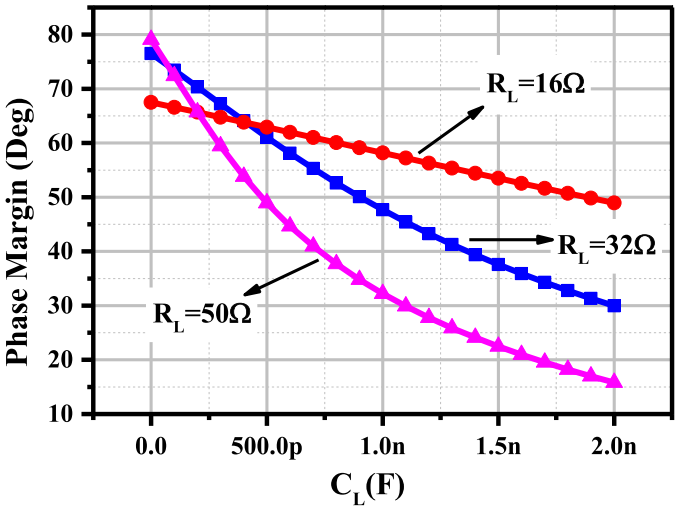

Fig. 11. Simulated PM for R_L = 16, 32, and 50 Ω when sweeping C_L from 0 pF to 2 nF.

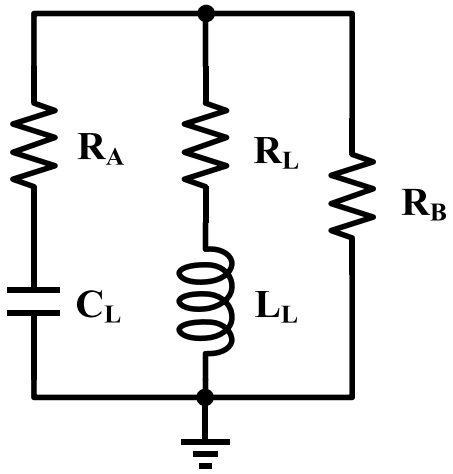

Fig. 12. Approximated headphone impedance model [29].

transistors, M_3 and M_4 and the mirror active load transistors, M_{10} and M_{11}, are made small through the use of long channel length. Not only does this arrangement increase the device matching characteristics, it also reduces the flicker noise and the threshold voltage mismatch. In addition, the use of folded-cascode topology provides high output swing as well as high input common-mode range. The bias voltages V_{BP1}, V_{BP2}, V_{BN1}, and V_{BN2} are generated by the simple low-voltage cascode bias generators (not shown in Fig. 14).

B. Second Gain Stage

The second gain stage of headphone amplifier is made up of transistors M_{12}–M_{17}. The dual-input noninverting gain stage is realized by active load, M_{14} and M_{15}, which have a current mirror gain of 4. The transistors M_{16} and M_{17} form the floating voltage biasing source. They are of great importance for biasing the output stage and controlling its quiescent current. In this circuit, they will be biased by the channel-length-modulation reduced (CLM-reduced) class-AB bias generation circuit. Since the second stage is just a common source stage

TABLE II
PERFORMANCE COMPARISON OF REPORTED PRIOR-ART RESULTS

Parameters	[6] Maxim'02	[31] ESSCIRC'06	[14] JSSC'09	[17] JSSC'12	[16] TCASII'12	[5] JSSC'14	This work
Process	NA	65 nm	0.13 µm	130 nm	0.5 µm	40 nm	**65 nm**
Supply (V)	3.0	2.5	1.2/2.0	1.5	3.0	3.1/4.5	**2.0**
Resistive Load (Ω)	16	16	16	16	16	16	**16**
Capacitive Load (F)	0-300p	0-12n	1pF-22n	NA	10p-5n	NA	**0-2n**
Gain (dB)	60	NA	NA	NA	51.5	NA	**113**
Phase Margin (°)	40	NA	>45	NA	72	NA	**> 45**
GBW (MHz)	2.5	NA	4	NA	1.23	NA	**1.78**
PSRR@ 217Hz (dB)	90	NA	NA	NA	70	110*	**84**
Slew Rate (V/µs)	0.8	NA	0.4	NA	1.2	NA	**1.1**
Quiescent Power (mW)	12.0	12.5	1.2	1.5	1.43	3.8	**0.4**
Output Voltage (V_{PP})	2.5	1.85	1.6	2.5	2.45	3.24	**1.5**
SNR (A-weighted) (dB)	95	NA	92	98	79.9	100	**93.5**
Peak THD+N (dB)	-90	-68	-84	-72	-77.9	-84	**-89**
Total Compensation Capacitance (pF)	NA	35	14	NA	16.3	NA	**8.5**
FOM1 &	8.1	4.3	33.3	65.3	65.8	43.4	**87.9**
FOM2 #	2561	108	5278	2600	5167	6878	**24774**

*: Powered by LDO regulator and charge pump
&: FOM1=(Peak load power)/(Quiescent power)
#: FOM2=(Peak load power)/[Quiescent power*(THD+N)%]

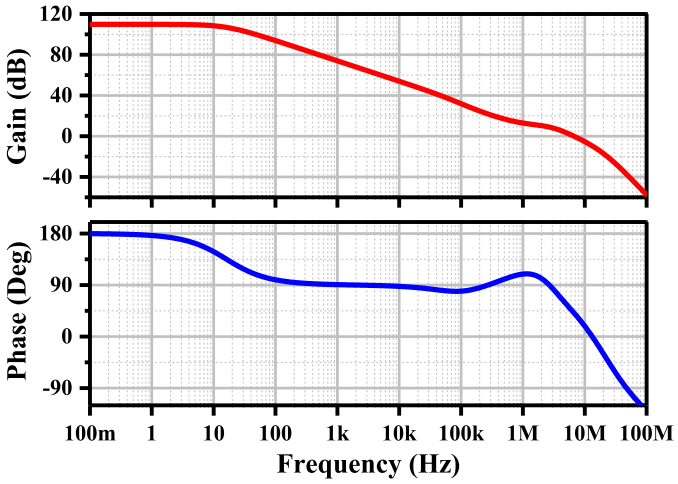

Fig. 13. Simulated open-loop gain and phase for headphone amplifier using the approximated headphone impedance load model.

without cascode topology to enhance the output impedance, its gain is lower than that of the first stage.

C. Output Stage

The transistors M_{18} and M_{19} realize the output stage g_{m3}, as shown in Fig. 14. Since the amplifier is required to drive small resistive load and large capacitive load, the aspect ratios for M_{18} and M_{19} are made very big and the smallest channel length is utilized to provide adequate current sourcing or sinking from the load. This will also minimize the silicon area as well as the parasitic capacitances. However, the price paid for small channel length transistors is the increase of CLM effect, causing the inaccuracy of the biasing current in the output transistors.

The CLM-induced error in the class-AB push–pull stage can be minimized by the proposed CLM-reduced bias generation circuit, as shown in Fig. 15. The drain–source voltage of n-type replica output transistor $M_{19'}$ is established via the level-shift voltage V_{gs} of $M_{17'}$, such that $V_{ds19'} = V_{gs19'} + V_{gs17'} \approx 1/2(V_{DD} - V_{SS})$ which is about 1 V at the ±1 V supply in this design example. Since the transistor $M_{18''}$ is a replica of the p-type output transistor M_{18}, the drain–source voltage of $M_{17'}$ is close to that of M_{17}.

The similar biasing network is applied for biasing the p-type output transistor M_{18} of headphone amplifier. Therefore, the improved bias generation circuit permits the output stage drawing current very close to the quiescent current of design value. In order to implement a symmetrical output stage, the quiescent current drive to the output transistors needs to be balanced. Since the mobility of electron is about three times of the holes in 65-nm CMOS technology, the width of

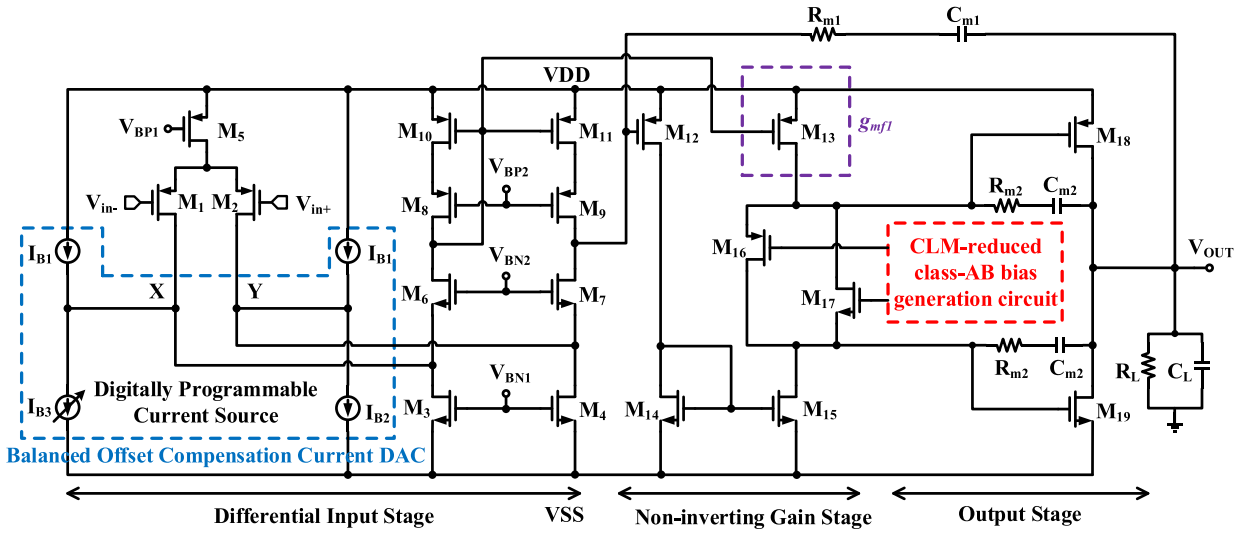

Fig. 14. Simplified schematic of the proposed amplifier with embodiment of the proposed offset compensation circuit and NMCFNR2 frequency compensation topology.

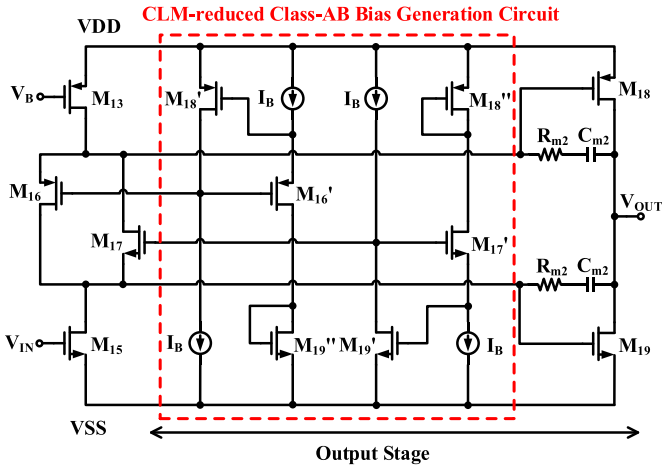

Fig. 15. CLM-reduced class-AB bias generation circuit.

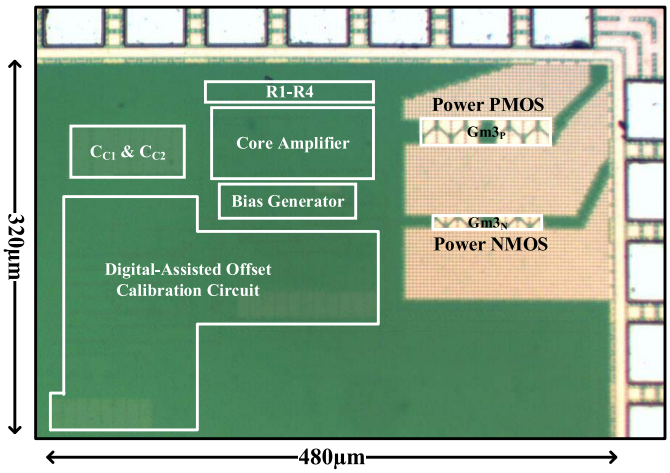

Fig. 16. Micrograph of the proposed headphone amplifier.

p-type output transistor is set as three times of the n-type output transistor for a symmetrical output swing.

V. Measurement Results

The proposed headphone amplifier is implemented and fabricated in 65-nm CMOS technology, and the micrograph of the amplifier is shown in Fig. 16. The total area of the circuit is about 0.15 mm^2 (480×320 μm), of which the digital blocks and the power transistors contribute to about two thirds. Since the power transistors sink or source large current, they are placed close to the pad while far away from the core amplifier. The measurement results have shown that the input-referred offset of ten chips can be calibrated to be less than 85 μV when compared with the maximum offset of 2.25 mV without offset calibration. Fig. 17 shows the measured quiescent power of ten chips with/without offset calibration. The average power of the ten chips with and without offset calibration is about 0.4 and 0.46 mW, respectively. Of particular interest, without calibration, the power consumption of the ten chips varies from 0.39 to 0.56 mW. The four chips out of ten chips display the substantial increase of quiescent power from 25% or above with respect to that with calibration. It has validated that the offset calibration can reduce the induced quiescent power due to the input-referred offset.

The test chips are measured by the *Stanford Research System* SR1 audio analyzer. Fig. 18 shows the FFT output signal of the amplifier with the 1-kHz sinusoidal input signal of 1.5 V_{pp}. It is noted that 0 dBr in the vertical axis represents 1 V_{rms} (0 dB) in the vertical axis. All the harmonics are less than -100 dB. The headphone amplifier has achieved -91 dB THD at peak load power. Finally, the A-weighted THD+N and SNR at peak load power in the 20 Hz–20 kHz bandwidth are measured with -89 and 93.5 dB, respectively.

Fig. 19 shows the measured A-weighted THD+N versus the output amplitude for 1 kHz input signal. For low output signal, its harmonics amplitude will be below the noise floor [14], [30]. Based on this reason, when the output

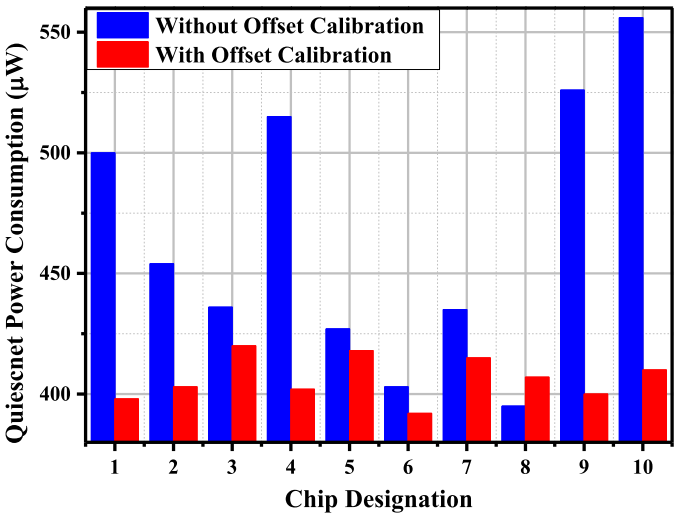

Fig. 17. Measured quiescent power consumption of ten chips with/without offset calibration.

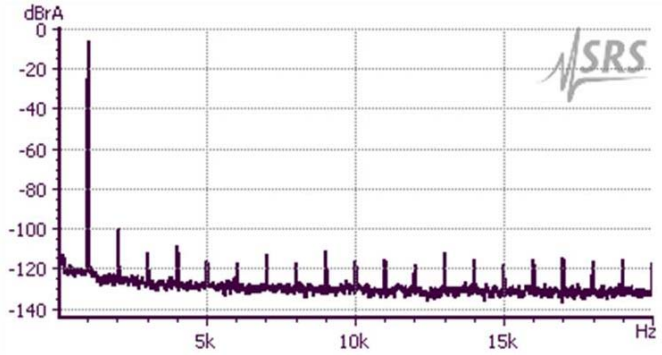

Fig. 18. Measured output signal in FFT with the 1.5 V_{PP} 1 kHz input sinusoidal wave.

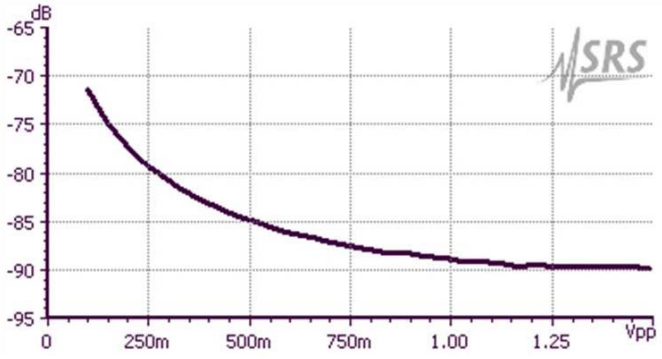

Fig. 19. Measured THD+N versus output amplitude for 1 kHz input signal.

signal amplitude reduces, the decreasing SNR will degrade the THD+N. With the increase of input signal, the SNR will increase, thus resulting in lower THD+N.

Fig. 20 shows the A-weighted THD+N having different signal frequencies at peak load power. For the low-frequency signal, the flicker noise of amplifier deteriorates the SNR, but displaying better linearity. The combined effect results in lower THD+N at low frequencies. On the other hand, with increasing the input signal frequency, the distortion increases

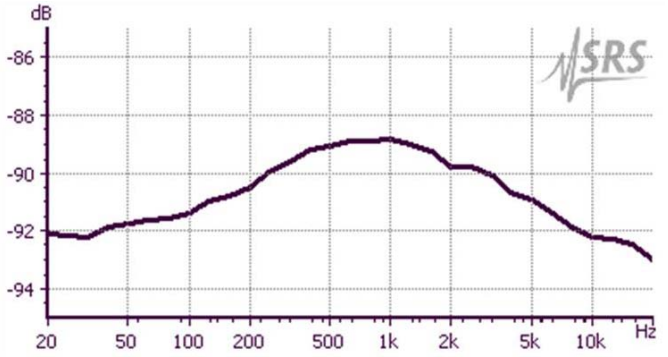

Fig. 20. Measured THD+N versus signal frequency with 1.5 V_{PP} input sine-wave signal.

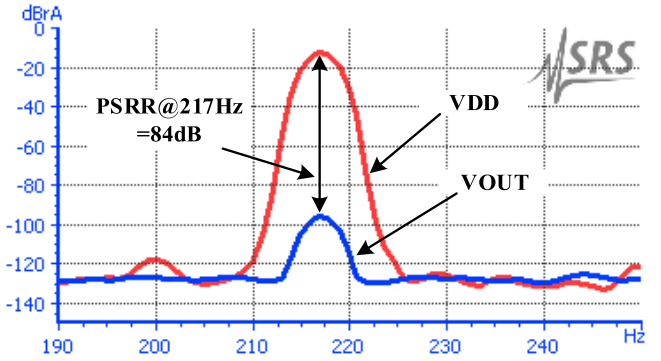

Fig. 21. Measured PSRR+ at 217 Hz with 700 mV_{PP} on the 1 V positive supply.

due to the drop of open-loop gain. Finally, the high-frequency harmonics in the audio band decreases with the increasing frequency, thus contributing to the improved THD+N if the distortion does not significantly degrade the SNR [14], [30].

Fig. 21 shows the FFT plot of the amplifier's output in response to the 700 mV_{PP} 217 Hz input signal, which is applied on the positive power supply of amplifier. The measured PSRR+ is 84 dB. Similar measurement is also conducted on the negative power supply of amplifier, which shows that the PSRR− is 105 dB at 217 Hz in Fig. 22. Fig. 23 shows the large-signal pulse responses of the amplifier at different capacitive loads in parallel with the resistive load. The amplifier can drive the maximum load of 2 nF//16 Ω with the slew rate of 1.1 V/μs.

Table II shows the performance comparison of the proposed headphone amplifier with the recently published state-of-the-art works. Among the topologies, the proposed amplifier consumes the quiescent power of 0.4 mW and requires a total compensation capacitance of 8.5 pF, which are considered as the lowest values. At the same juncture, it also provides the comparable performance metrics, such as PSRR, SNR, and THD+N. The figure-of-merit (FOM1), which is defined as the ratio of the peak power over the quiescent power, is obtained as 87.9. Another FOM2, which is defined as the ratio of FOM1 over THD+N in percentage, is compared. Both FOM1 and FOM2 have displayed the highest values among those of the reported works, demonstrating the effectiveness of two circuit

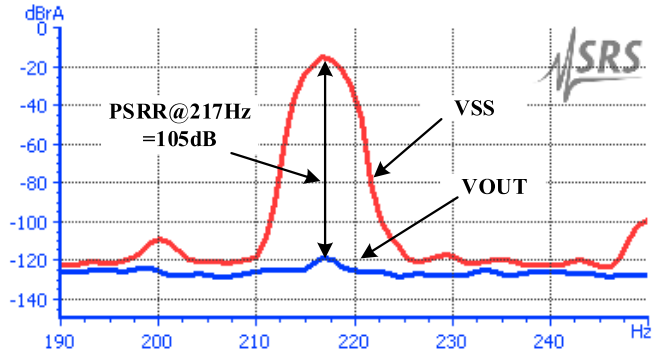

Fig. 22. Measured PSRR- at 217Hz with 700 mV_{PP} on the 1V negative supply.

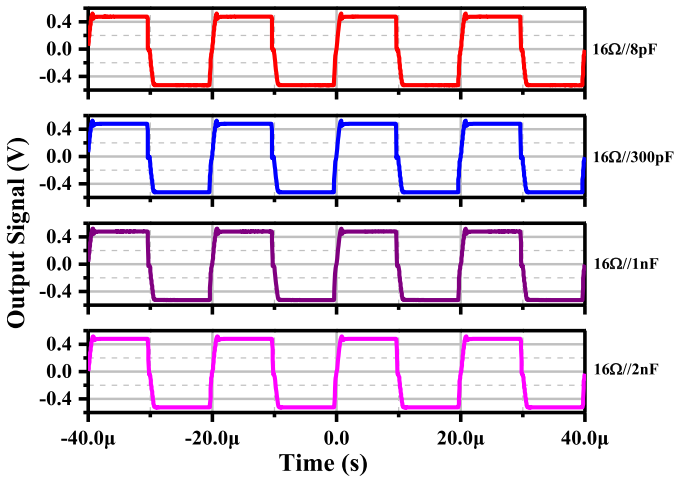

Fig. 23. Pulse response of the headphone amplifier with the respective load of 16 Ω/8pF, 16 Ω/300pF, 16 Ω/1nF, and 16 Ω/2nF.

techniques in the low-quiescent high-performance headphone amplifier design. Future work will focus on the glitch reduction circuit techniques for the power-ON startup and the calibration circuit.

VI. Conclusion

A performance-aware low-quiescent class-AB headphone amplifier has been presented together with the detailed analysis. Two key circuit techniques have been introduced. First, the digitally assisted offset calibration circuit architecture is able to reduce the mismatch-induced quiescent current caused by the input-referred offset of amplifier without jeopardizing the PSRR as well as dc gain. Second, the improved frequency compensation permits the amplifier to drive the worst case the load of 16 Ω//2 nF while sustaining good stability and providing good GBW at low power. Other performance metrics, such as PSRR, THD+N, and SNR, are obtained with comparable performance. The amplifier outperforms the prior-art works by achieving the best power-related FOM1 and power-(THD+N) related FOM2, demonstrating the efficiency from quiescent state to full power state and the efficiency for low THD with low power, respectively.

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