

A Multiphase Class-D Automotive Audio Amplifier With Integrated Low-Latency ADCs for Digitized Feedback After the Output Filter

Daniel Schinkel, *Member, IEEE*, Wouter Groothedde, *Member, IEEE*, Fred Mostert, Marto-Jan Koerts, Eric van Iersel, Daniel Groeneveld, *Student Member, IEEE*, and Lucien Breems, *Senior Member, IEEE*

Abstract—A 5×80 W class-D audio power amplifier for automotive applications is presented. The amplifier is implemented in a 140-nm bipolar CMOS DMOS SOI. Configurable digital-loop filters can compensate for a range of LC output filters and their high loop gain (>50 dB between 20 Hz and 20 kHz) suppresses non-idealities of the output filter and enables low-cost output filter components. Key elements are the integrated low-latency $\Delta\Sigma$ analog to digital converters (ADCs) which digitize the output signals directly at the speaker load, after the output filter. The ADCs use filtering finite impulse response digital to analog converters in their feedback path to create an input–output transfer with a negative group delay at low frequencies. The ADCs have 116-dBA DR and -108 dB total harmonic distortion (THD). The bridge-tied load amplifier supports multiphase pulse-width modulation for lower electromagnetic interference. It operates with supplies from 6 to 25 V and with loads down to $1\ \Omega$ and achieves $19\text{-}\mu\text{V}$ idle noise (Awtd) and 0.004% THD + N.

Index Terms—Audio power amplifier, bipolar CMOS DMOS (BCD), class-D amplifier, delta-sigma analog to digital converter (ADC), multiphase, SOI.

I. INTRODUCTION

SWITCHING class-D amplifiers have become the preferred topology for contemporary audio amplifiers because of their high power efficiency. They have largely replaced the traditional class-AB amplifiers in mobile, consumer, and automotive applications. However, from an application point of view, they are more costly than their traditional linear counterparts, because they usually require output filters to reconstruct the output, suppress the switching components, and prevent electromagnetic interference (EMI). Only in low-power (mobile) applications, the less stringent EMI requirements and the short distance between the class-D amplifier and its load enable “filterless” application.

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D. Schinkel is with Teledyne DALSA Semiconductors, 7521PT Enschede, The Netherlands, and also with NXP Semiconductors, 6534AE Nijmegen, The Netherlands (e-mail: d.schinkel@electronics.net).

W. Groothedde and D. Groeneveld are with Teledyne DALSA Semiconductors, 7521PT Enschede, The Netherlands (e-mail: wouter.groothedde@teledyne.com).

F. Mostert, M.-J. Koerts, and E. van Iersel are with NXP Semiconductors, Nijmegen, The Netherlands.

L. Breems is with NXP Semiconductors, 5656AE Eindhoven, The Netherlands (e-mail: lucien.breems@nxp.com).

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In automotive applications, which are the field of this work, the more stringent EMI regulations and long speaker lead do require a well-designed *LC* output filter of at least second order. This *LC* filter can be a significant cost factor, especially for the inductor, as all its desirable characteristics, such as a high current rating, large inductance, low series resistance (for good efficiency), and very linear behavior also add to its price. As an automotive amplifier typically uses a “bridge-tied load” (BTL) configuration, the component count and cost of the *LC* filter doubles.

The frequency response of the *LC* filter is influenced by the load and can show quite a bit of HF peaking for inductive speaker loads. To get a better defined damped response, passive damping networks are usually added (often referred to as Boucherot cells or Zobel networks, but sometimes as Snubber networks [1]). In a BTL configuration, such damping networks also help to dampen the common-mode (CM) behavior, which otherwise have very high Q and can give significant ringing at the *LC* resonance frequency. However, passive damping networks are only partly effective and the more they damp the response, the higher their influence is on the bill of material and power losses.

A solution that not only mitigates the influence of the *LC* filter components on the frequency transfer function but suppresses its non-linearities as well is the use of feedback after the output filter. This has long been a desired feature for switching (class-D) amplifiers [2], but the problem is that it requires a compensation of this *LC* filter to keep such a loop stable. In the analog domain, this is not a simple task, as the design not only has to cope with different *LC* filters but also with variability in the loop filter components. The proposed analog approaches so far involve the use of multiple feedback loops both before and after the output filter [1], [3]. In these approaches, the outer loop can have only limited gain to maintain stability. For example, in the integrated amplifier from [1], the loop gain of the outer loop is only about 10 dB at 20 kHz, which is not enough for proper error signal suppression.

Compensation of the (*LC*) output filter can be done more effectively in the digital domain, as digital filters are easy to reprogram for (or adapt to) different *LC* filters and digital time constants have no variability. Digital filters are also easy to test in an industrial environment and their loop filter area scales down with technology.

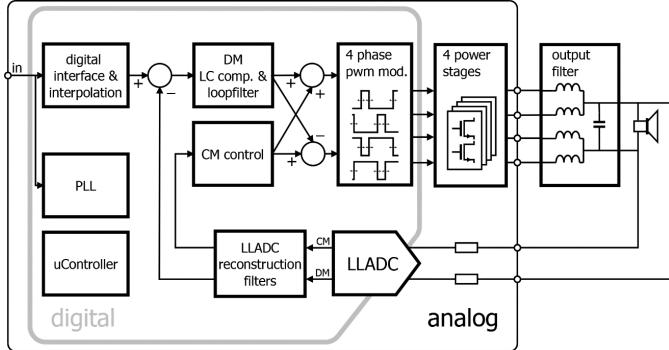


Fig. 1. Block diagram of one channel of the class-D amplifier.

In [4], it was first demonstrated that digital feedback is possible in a single loop with full global feedback after the output filter. However, the feedback does require a wideband analog to digital converter (ADC) with low latency, and the commercially available ADC that was used had a 2.5-MHz signal bandwidth with 950 mW of power consumption. In this paper, we show that a low-latency $\Delta\Sigma$ ADC (LLADC) that is tailored to the application enables digital feedback at a fraction of the power (30 mW per ADC).

In this paper, we present a five channel amplifier with the ADCs, digital, and power parts all integrated on the same die [5]. An overview of one channel of the amplifier is shown in Fig. 1. After the digital audio input interface, the input signal is up sampled and fed into a high-gain loop filter and *LC* compensation filter, followed by pulse-width modulation (PWM). As the BTL amplifier can be used in a multiphase configuration [6], there are four pulse-width modulators and four power stages per channel. The signal across the load is sensed with the LLADC and fed back into the digital-loop filter. The CM of the output is also sensed by the LLADC and controlled. Apart from the main signal path, there is a phase-locked loop to synchronize the system clock to the input sample rate (44.1 or 48 kHz or multiples). A microcontroller facilitates the configuration of the chip and manages the various operational modes (e.g., shutdown, standby, startup, and load detection). The microcontroller also monitors and controls circuit blocks for protection and diagnostics of which there are many given the automotive application.

This paper is organized as follows. In Section II, analog and digital class-D control strategies are analyzed. In Section III, the low-latency ADC that is used for the digital feedback after the output filter is described. In Section IV, the power stage and its use in a multiphase configuration are shown. Measurement results and comparisons are given in Section V, and the paper ends with conclusions in Section VI.

II. CLASS-D CONTROL STRATEGIES

An overview of class-D control strategies is given in Fig. 2. The traditional class-D amplifiers as shown in Fig. 2(a) have no feedback at all and consists only of a pulse-width modulator (or occasionally a pulse-density modulator) and a power stage, followed by the output filter and the load. Their major drawback is that any disturbances that originate from the

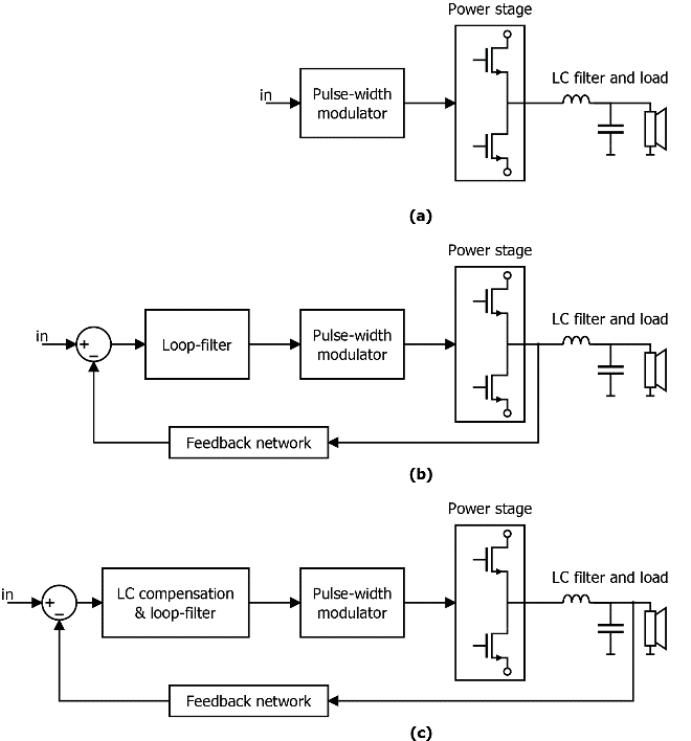


Fig. 2. Class-D topologies overview. (a) Open loop, (b) with feedback after the power stage, and (c) with feedback after the output filter.

supply or from the power stages (non-perfect switching edges) immediately lead to noise and distortion in the output signal. Open-loop amplifiers can reach good performance when used with high-quality digital pulse-width modulators [7], [8]. But they also require a (costly) low noise, low-impedance supply, and a power stage that has very well defined switching edges with minimal dead time and signal dependence.

A. Feedback Before the Output Filter

To alleviate the supply and power stage requirements, closed-loop class-D amplifiers with feedback after the power stage can be used, as shown in Fig. 2(b). With this type of feedback, power-supply noise is suppressed [power-supply rejection (PSR) becomes proportional to the loop gain] as are power stage (switching) artifacts. This type of feedback has become the workhorse of integrated class-D audio amplifiers [9]. Variations of this control topology work with PWM input signals [10], [11] and make the closed-loop power stage compatible with its open-loop counterpart.

A further step is the digitization of the feedback signal from the power stage [12]–[14], which omits the need for an analog re-modulating feedback loop. Such amplifiers also automatically provide digital inputs, with the ADC in the feedback loop omitting the need for a digital to analog converter (DAC) in the feedforward path. Recently, integrated circuits for digitized feedback of the power stage in mobile amplifiers were presented [15], [16]. Both [12], [13], [16] use passive low-pass filters prior to the ADC to attenuate the power of the switching components, but when output filters are present, they can be used for this purpose, as is done in this paper.

B. Analog Feedback After the Output Filter

Feedback after the output filter is conceptually depicted in Fig. 2(c). The first amplifier prototype with analog feedback after the filter was presented in [3], with an integrated amplifier following in [1] and [17]. Various self-oscillating class-D topologies have also incorporated the output filter in their feedback loop [18]–[20]. These self-oscillating amplifiers typically have a varying switching frequency (f_{PWM}), which can pose several problems [21]. For automotive systems, a big drawback is the unpredictable EMI. In this paper, we therefore concentrate on amplifiers with carrier-based PWM where the carrier might still have some deliberate (but well controllable) spread-spectrum characteristics for electromagnetic compatibility.

As is described in [21], the loop-gain that is available depends somewhat on the choice between self-oscillating or carrier-based approaches, but in all cases the unity-gain frequency (f_{UG}) of the loop needs to be lower than the f_{PWM} to maintain a stable loop. A more influential factor for the loop gain (especially for the loop-gain at the edge of the audio band) is the order of the loop filter, which determines how fast the loop can transition from its high in-band gain down to its f_{UG} . As such, class-D amplifiers with third-order [22] or fourth-order [23] analog loop filters have been presented, and even a fifth order for a self-oscillating amplifier [24].

However, for analog feedback after the output filter, the outer feedback loop has so far been limited to just first order [1]. Higher order loops require compensation of the LC output filter, which is complicated with analog time constants that can also vary themselves.

C. Digital Feedback After the Output Filter

That high-order digital-loop filters can compensate the LC filter was first shown in [4]. In this paper, we also use a fifth-order loop filter and a second-order LC compensation filter. We have furthermore designed the system to be robust for a wide range of load conditions (from an open load down to 1Ω) and supply levels.

The effect that this fifth-order filter has on the loop gain is visible in Fig. 3. The loop filter is based on a fifth-order Chebyshev noise transfer function (NTF), with design and implementation techniques similar to those used in higher order digital $\Delta\Sigma$ modulators [25]. The loop filter contains an integrator and two resonators and provides a loop-gain that exceeds 50 dB across the audio band and peaks to infinity at the resonance frequencies. Fig. 3 also shows the loop gain of a classical second-order analog loop filter that uses feedback before the filter [9]. Although this second-order loop filter is designed with the same f_{UG} (100 kHz) and the same phase margin (60°) as the fifth-order digital filter, its loop gain at 20 kHz is only 23 dB. Last, Fig. 3 shows the loop gain that [1] achieves in its outer loop, which is only of first order and has a lower f_{UG} (to keep this outer loop that includes the LC filter stable), with only 10-dB gain at 20 kHz as a consequence.

Note that the transfer of the LC compensation that is used in this paper is not visible in the loop gain of Fig. 3 because

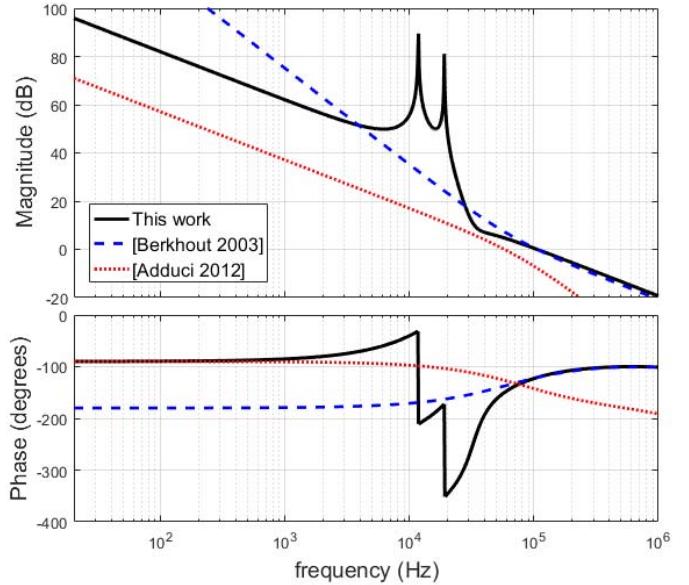


Fig. 3. Open-loop gain and phase of class-D loop filters.

its transfer is nominally cancelled by the LC transfer. Margins were incorporated in the loop design to cope with deviations between the two. As will be discussed next, the presence of the LC compensation filter also influences the ADC requirements.

III. LOW-LATENCY DELTA-SIGMA CONVERTER

To digitize the feedback signal, a $\Delta\Sigma$ ADC would be the natural choice because of the high-accuracy requirements. However, the compensation of the LC filter poles results in boosting of the high-frequency quantization noise (Q_N), which degrades the performance of the PWM modulation. High-level simulations with the amplifier loop showed that the ADC requires at least 8 bit of quantizer resolution to get less than -110 dB of mixed-down Q_N in the audio band, while contemporary $\Delta\Sigma$ ADCs generally only offer 4–6 bit of wideband resolution. The addition of a digital reconstruction filter to attenuate the Q_N also adds latency (phase shift) which degrades loop stability when combined with a normal $\Delta\Sigma$ ADC.

Therefore, for this work we developed a special 1-bit $\Delta\Sigma$ modulator that has, in combination with its reconstruction filter, no net phase shift (at least not up to the f_{UG} of the amplifier loop filter). The results are a low-latency ADC (LLADC) with low out-of-band Q_N that can be used in a feedback loop without stability problems. To achieve this, a $\Delta\Sigma$ modulator with an extrapolating signal transfer function (STF) is designed. Specifically, the STF has two dominant zeros at $f_C = 60$ kHz. This enables the use of a second-order low-pass reconstruction filter with two poles at this f_C , which cancel with the zeros from the $\Delta\Sigma$ modulator STF. The reconstruction filter attenuates the HF quantization noise with 48 dB, equivalent to the Q_N of an 8-b quantizer.

The architecture of the LLADC is shown in Fig. 4. The LLADC has a filtering finite impulse response DAC (FIRDAC) [26] in the feedback path, which enables high-accuracy D/A conversion while being highly insensitive

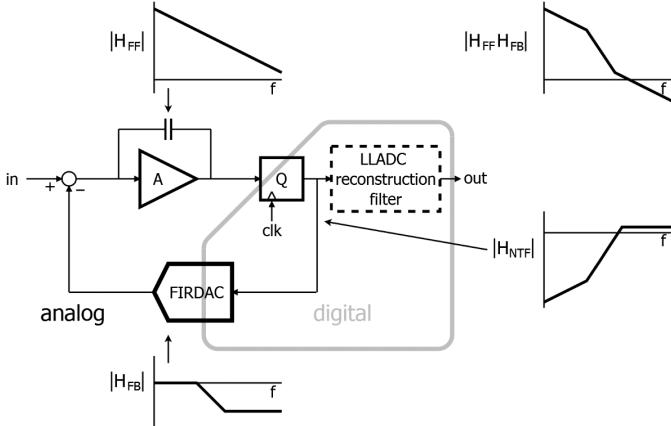


Fig. 4. Overview of the LLADC and its transfer functions.

to component mismatch and clock jitter. Fig. 4 also shows the various transfer functions in the LLADC loop. To ensure that the product of the feedback filter transfer H_{FB} and the transfer in the forward path (H_{FF}) give proper noise-shaping behavior, they are derived from a stable NTF: $H = H_{FB} \times H_{FF} = 1/H_{NTF} - 1$. The procedure is similar to the design procedure for a normal $\Delta\Sigma$ modulator, except that a number of zeros in the NTF are restricted to damped locations. The result is that the H_{FB} IIR filter prototype has a damped impulse response, which can be approximated with a FIRDAC [27]. The NTF used in this design is shown in Fig. 5.

The STF of the linear model of the $\Delta\Sigma$ modulator can be derived to be: $H_{STF} = H_{FF} \times H_{NTF} = H_{FF}/(1 + H_{FB} \times H_{FF})$. The STF approximates to $1/H_{FB}$ for those frequencies where the loop has gain. The two poles in H_{FB} thus create the zeros in the STF and give the STF a second-order high-shelving filter characteristic with its +3dB corner at $f_C = 60$ kHz, as is also shown in Fig. 5. The high-shelving characteristic realizes an extrapolating or predictive ADC behavior at low frequencies. This is reflected in the negative group delay as plotted in the bottom graph in Fig. 5. The group delay equals the negative derivative of the phase shift, and although the phase shift is small, its derivative equals $-3\ \mu s$ at low frequencies and only becomes positive above 250 kHz. This explains why the combination of the $\Delta\Sigma$ modulator and its digital reconstruction filter has no net latency at low frequencies. For high frequencies, where the loop has no gain, the STF becomes proportional to the integrating filter in the feedforward path, which is why the STF starts roll off above 1.5 MHz as visible in Fig. 5.

The behavior of the $\Delta\Sigma$ ADC is similar to that of a tracking ADC and does require that the dominant input power is limited to frequencies below f_C , which is in this application ensured by the filtering function of the LC output filter.

Because the feedback filtering also participates in the noise shaping, the forward path H_{FF} can be kept simple and only consists of a first-order integrating amplifier in the implemented ADC. The amplifier uses chopping to minimize $1/f$ noise. Single-bit quantizers ensure that there are no gain and linearity requirements at the output of the integrating amplifier, as long as its zero-crossings match those of a linear

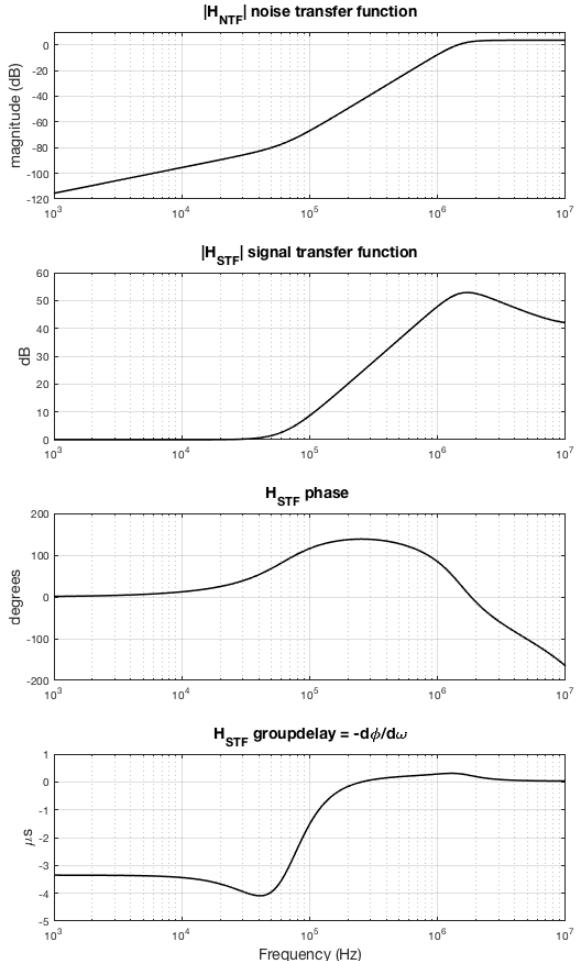


Fig. 5. Closed-loop LLADC transfer functions.

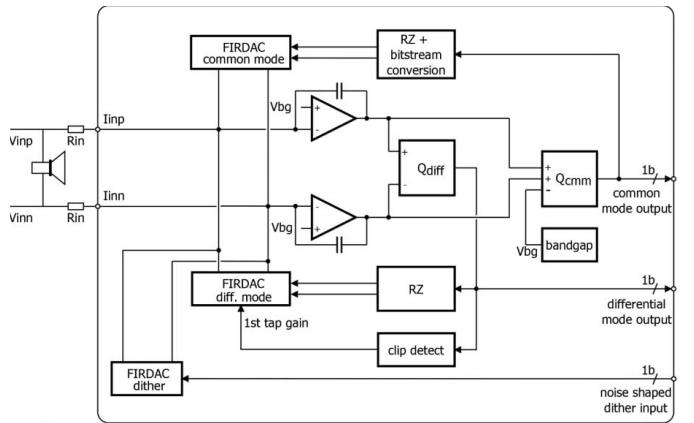


Fig. 6. Low-latency $\Delta\Sigma$ A/D converter.

integrator. This permits the use of nonlinear gate-oxide integration capacitors with high capacitance density (an optimization that has previously also been applied in analog class-D feedback loops [28]).

The detailed ADC architecture is shown in Fig. 6. The actual ADC uses two feedback loops: one to convert the CM and one to convert the differential-mode (DM) input signal, with only the DM loop requiring high accuracy. The ADC core has current inputs into a virtual ground biased at 0.9 V,

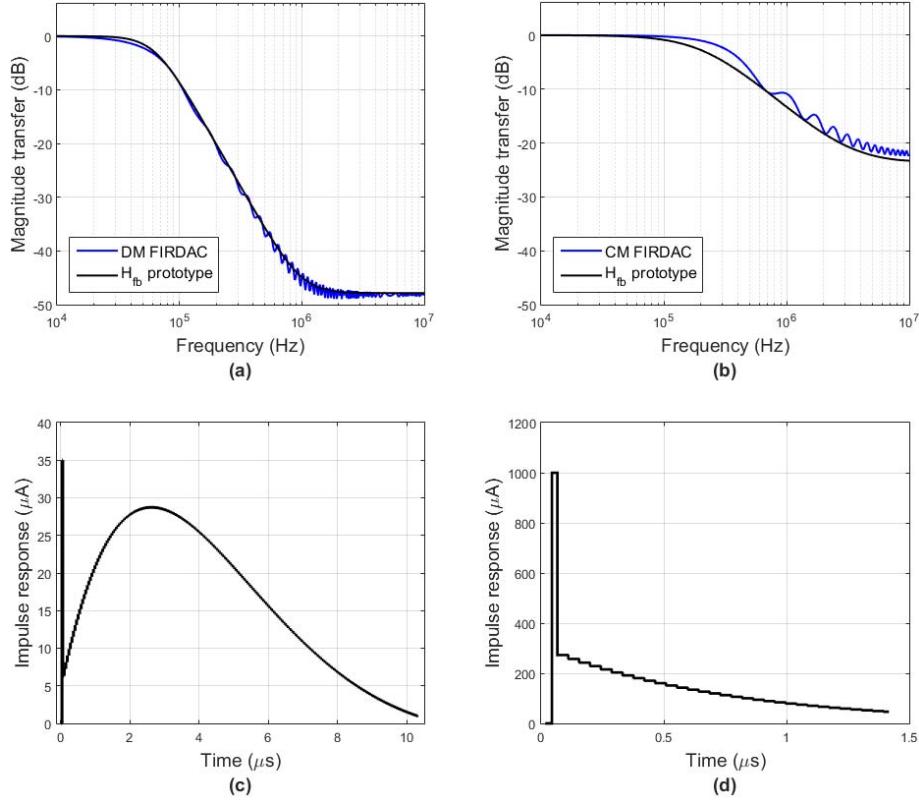


Fig. 7. Magnitude frequency transfer of (a) DM FIRDAC and (b) CM FIRDAC, and (c) and (d) corresponding impulse responses.

with bi-directional current inputs due to the combination of the current-sourcing CM loop and the current-sinking DM loop. The ADC uses 1.8-V CMOS transistors and supply while the V/I conversion resistors at its input allow for conversion of voltage levels far beyond its supply rails. In nominal operation, the conversion resistors also level-shift between the amplifiers operating point (half of the V_p) and the ADCs operating point (0.9 V) and the resistors deliver most of the current for the DM loop. At startup, when the amplifier outputs are still at ground level, the CM loop sources all the current.

The DM loop is designed to reach a signal to quantization noise ratio of 126 dB. This is achieved at an over-sampling ratio of 512 and third-order noise-shaping characteristic of which two orders are implemented in the DM FIRDAC. The impulse response of the DM FIRDAC is shown in Fig. 7(c) (note the large first tap which is needed because of the zeros in H_{FB}). At a length of 466 taps, the impulse response of the original second-order H_{FB} IIR prototype can be cut off with only minor differences in the resulting signal transfer, as is visible in Fig. 7(a). This signal transfer also indicates the frequency dependent maximum input signal level that the ADC can handle without clipping.

The DM loop is conditionally stable. To recover from instability and its unwanted low-frequent limit cycles, clip detection, and recovery mechanisms are added to the DM FIRDAC. The CM loop is designed to reach 80-dB DR, which can be obtained with a 64 taps FIRDAC that behaves as a first-order filter, as is shown in Fig. 7(b) and (d). Overall, the CM loop filter is of second order and needs no further

measures to maintain stable operation. The CM bitstream can be fed directly to the amplifier's CM controller without the need for a reconstruction filter because of the lower requirements on the CM control. Besides the main FIRDACs, there is also a short 2 taps dither FIRDAC implemented, to suppress tonal limit cycles in the DM bitstream. The dither FIRDAC is supplied with a pseudorandom bit sequence that is noise shaped to limit the in-band noise contribution.

Transistor level schematics of a CM and DM FIRDAC tap are shown in Fig. 8. The FIRDACs use dynamic flip-flops for the digital delay line, similar to [26], but with the difference that the P and N side of the differential switch pair now both have their own flip-flop. This double row of flip-flops increases symmetry and enable the use of return to zero (RZ) code to avoid non-linear inter-symbol interference. To implement the RZ behavior, the FIRDAC delay lines are clocked at twice the quantizer's sample rate and each symbol starts with an inactive part (where both the $P(n)$ and $N(n)$ signal are zero), followed by an active part (a one in either the $P(n+1)$ or the $N(n+1)$ signal).

To avoid that the RZ technique changes the filter characteristic, pairs of adjacent filter taps (with equal weight) are used to implement filter coefficients. The resulting behavior is similar to interleaved RZ [29]. The first coefficient is not implemented with a pair of taps, but is only active in the second half of the period, to give the quantizer time to make a decision.

For the CM FIRDAC, each tap consists of two current sources (as visible in Fig. 8), because CM currents needs to be sourced in both P and N simultaneously. A simple dynamic

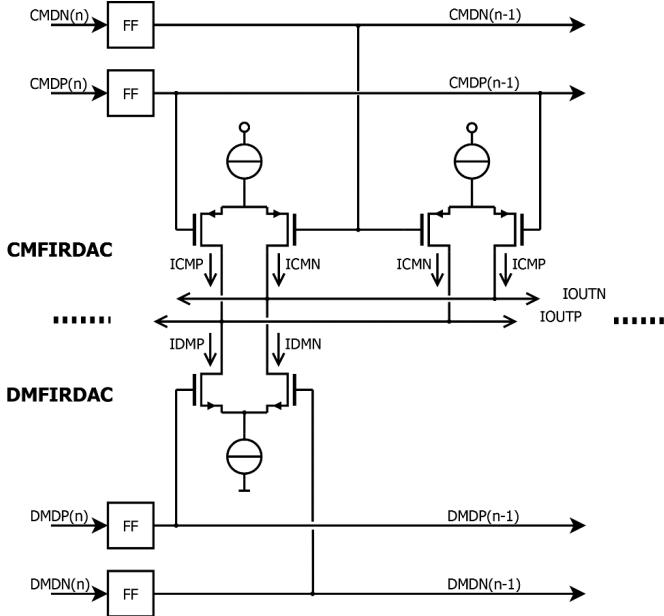


Fig. 8. Schematic of a single tap of the CM (top) and DM (bottom) FIRDACs.

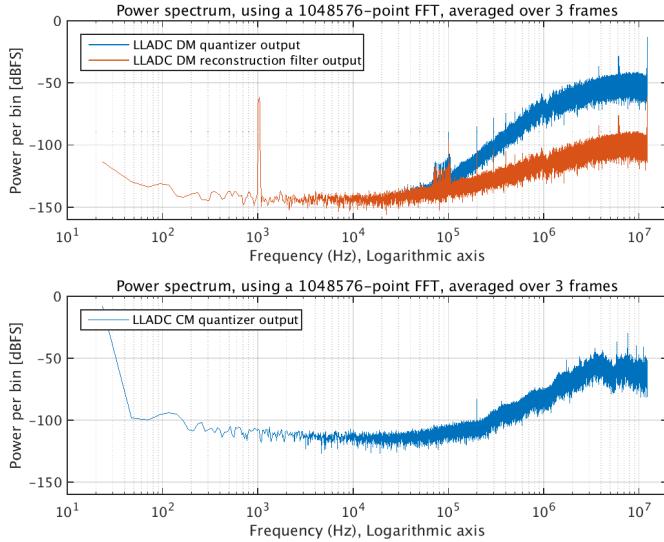


Fig. 9. Measured spectra of the LLADC outputs.

element matching noise shaper converts the CM quantizer bitstream into P and N codes with equal average use of both, to minimize in-band DM effects from CM mismatch.

Fig. 9 shows the measured spectra of the DM and CM bitstream outputs at -60 dBFS DM input level, as well as the DM output after the digital reconstruction filter. The tones at multiples of 100 kHz are due to the chopping in the integrating amplifier. The DM of the ADC has a dynamic range of 116 dB (A-weighted) and a total harmonic distortion (THD) below -108 dB (at 4 -V inputs). The ADCs are integrated together with a bandgap reference with 90 -dB SNR. At large inputs, the SNR of the complete amplifier reaches a plateau at this 90 dB as the reference noise manifests itself as a multiplicative noise source that mixes with the ADCs input signal.

The shared reference consumes 7 mW and each of the five ADCs consumes 30 mW of power. In contrast, the

commercially available ADC that was used in [4] consumes 950 mW of power as it is designed for wideband (2.5 MHz BW) applications. This even excludes an external reference and driving amplifier. The LLADC developed in this work requires no external components and has more than a factor 30 lower power consumption as it is optimized for application in the feedback loop of a power amplifier.

IV. POWER TOPOLOGY

A. Power Stage

Fig. 10 shows one of the 20 power stages. It uses identical high-side (HS) and low-side (LS) high-voltage N-MOST transistors. A charge pump creates a voltage of V_{CP} is 6 V above the power-supply V_{DDP} for HS gate drive. Switching high currents up to 10 A with 10 ns slopes will generate voltage spikes as high as 10 V across the bond wires ($L_{BONDING}$). To avoid oxide damage from these spikes, each power transistor uses its own floating voltage domain with the power supply as in [30]. The level-shift circuits adapt the control signals to the floating domain, where they are latched to reduce disturbance from switching transients. To turn ON the power transistor, more than 100 mA flows into the gate-source capacitor. The current multiplier takes only a fraction of this current from the floating supply while the rest is delivered by the charge-pump V_{CP} . This enables small buffer capacitors in the floating supply. The adaptive gate drive [31] reduces EMI by preventing reverse recovery and also avoids dead time. Protection circuits as described in [32] limit the output current and in case of sustained limiting, shut down the power stage.

B. Multiphase PWM Theory

Two PWM techniques, multilevel and multiphase PWM, are often used to reduce high-frequency switching components and lower EMI. These techniques are well known from dc–dc converter applications, [33]–[40]. In class-D audio amplifiers, the multiphase concept was first introduced in [6]. In [6], multiple output stages are placed in parallel, connected at the load with each output stage having its own phase-shifted triangular reference as is shown in Fig. 11(a). A functionally equivalent technique is multilevel PWM [23], [35], [37], [40], which uses multiple voltage levels and associated switches.

This work uses the multiphase approach which does not require additional voltage levels, has lower complexity [6] and can also be used with conventional PWM. The signal at the load in a multiphase system is graphically depicted by the single-ended 4-phase example in Fig. 11. The contribution of the 4-PWM signals are added via the inductors L_1 to L_4 and result in the sum current I_{SUM} shown in Fig. 11(b). The sum current has an N -times higher ripple frequency ($N \cdot f_{PWM}$) and an N^2 -times lower maximum ripple amplitude than the individual coil currents. As such, a higher effective PWM frequency is obtained without the increased switching losses that actual higher switching frequencies would give. Ideally, all ripple components below $N \cdot f_{PWM}$ are cancelled in the sum. In practical applications with coil mismatch, some residue will remain, but at a reduced magnitude. For example, in typical

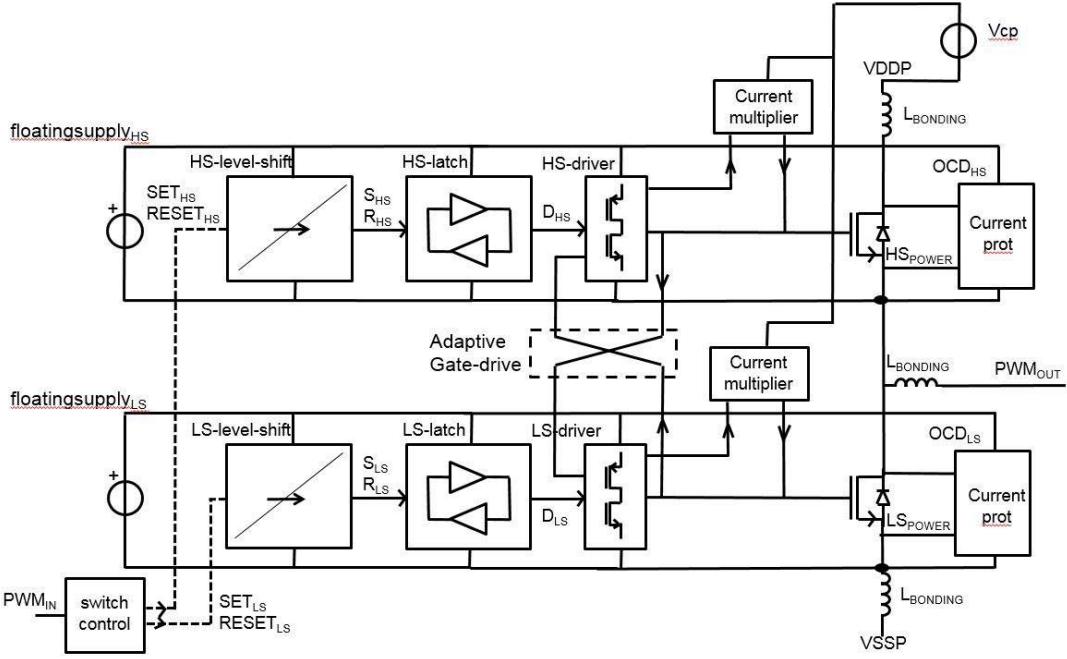


Fig. 10. Single-ended class-D power stage.

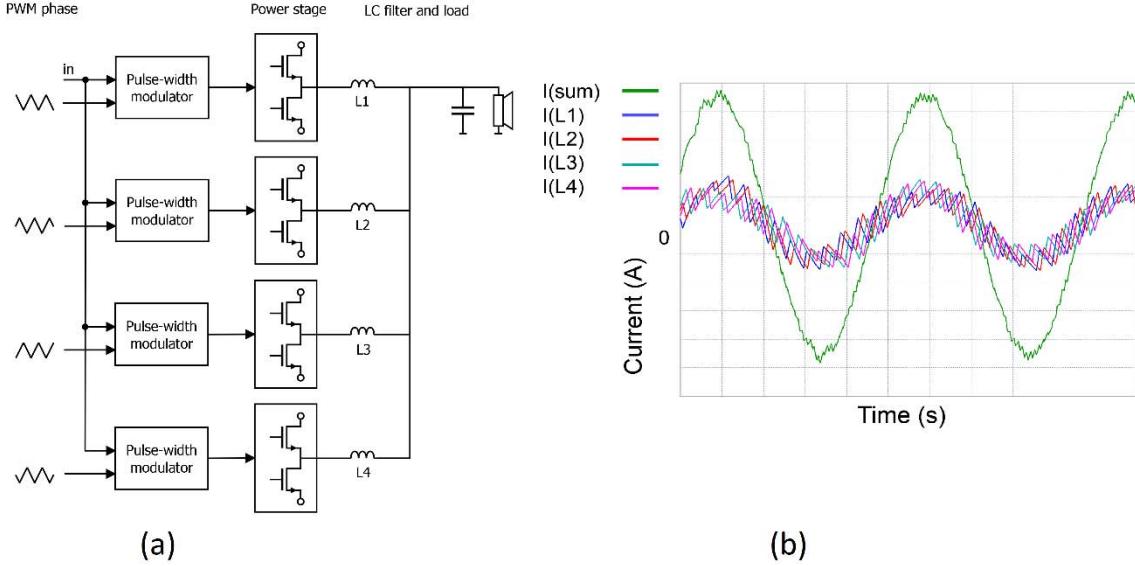


Fig. 11. Multiphase output stage. (a) Functional schematic. (b) Output current waveforms.

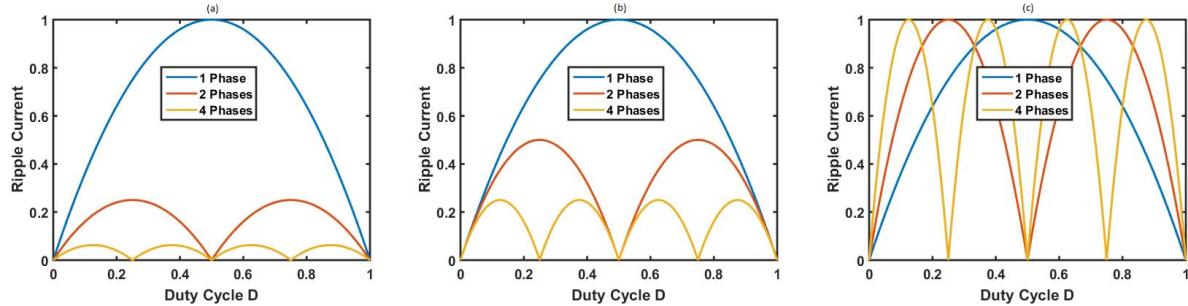


Fig. 12. Ripple currents with multiphase output stages and scaled inductors. (a) Scaled for original bandwidth and minimal ripple. (b) No scaling. (c) Scaled for cheapest and smallest inductance.

measurements with this system, the $1 \times f_{\text{PWM}}$ ripple component is reduced by about 30–40 dB as can be observed in the measured spectral density plots of Fig. 17.

Within a multiphase system a tradeoff can be made between bandwidth, total inductance, and maximum ripple magnitude. Fig. 12 illustrates this by showing the normalized peak-to-peak

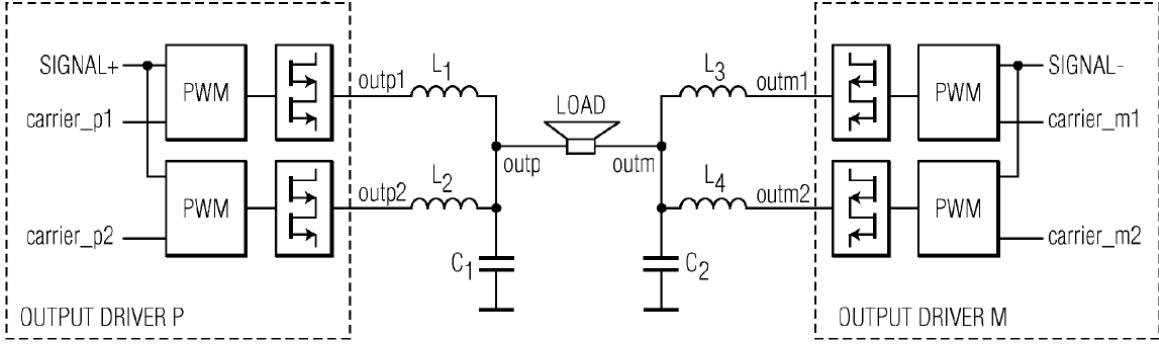


Fig. 13. BTL implementation of this paper [32].

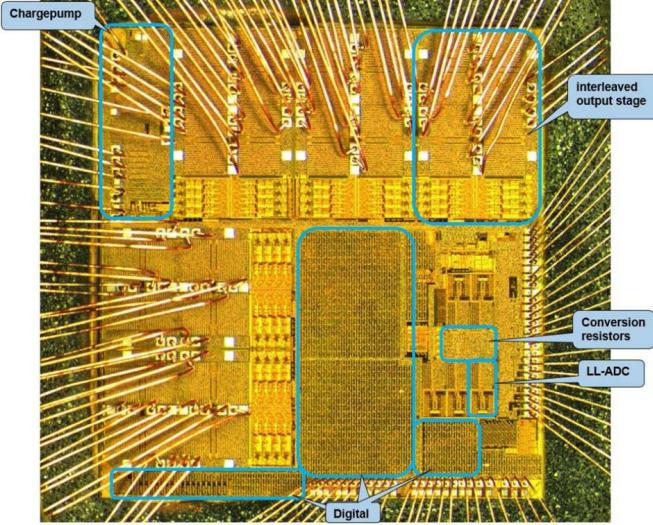


Fig. 14. Die micrograph.

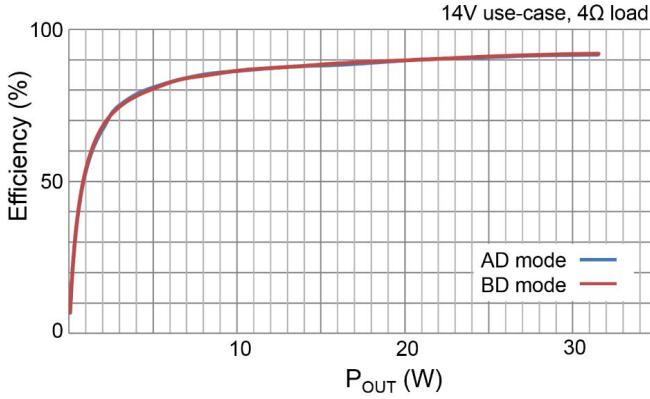


Fig. 15. Efficiency for two modulation schemes with five active channels.

ripple in sum current versus duty cycle for a 1-, 2-, and 4-phase system for various inductance values. To keep the bandwidth constant, as was done in Fig. 11, the inductance per branch has to be increased by a factor N, resulting in a significant ripple reduction of N^2 [see Fig. 12(a)]. Alternatively, when the inductance for each branch is kept equal to the 1-phase equivalent system, the ripple reduces by a factor N as is shown in Fig. 12(b), while the bandwidth is increased by \sqrt{N} .

The most cost effective use case is to reduce the inductors by a factor N, which keeps the maximum ripple magnitude

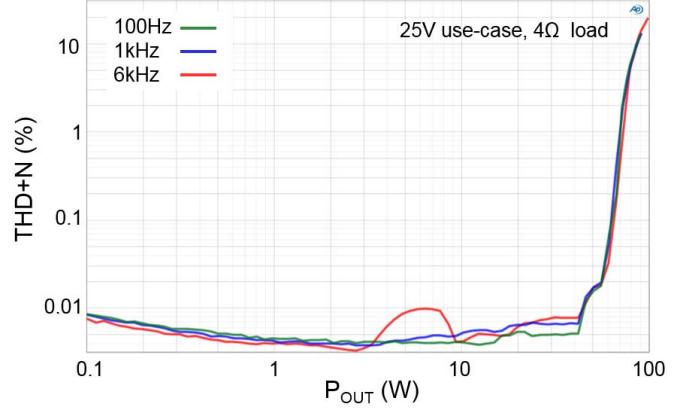


Fig. 16. Measured THD+N versus output power.

the same as in the 1-phase equivalent, as shown in Fig. 12(c). Inductor costs are related to their current rating and inductance value, which together determine their energy storage and volume. For this use case the energy per coil can be expressed as follows:

- 1) Single-phase system: $E_{COIL} = I_{TOT}^2 \times L$;
- 2) Multiphase system: $L_N = L/N$, $I_N = I_{TOT}/N$; \rightarrow
- 3) $E_{COIL_N} = I_N^2 \times L_N = (I_{TOT}/N)^2 \times L/N = (I_{TOT}^2 \times L)/N^3$.

So in this use case the energy stored in each inductor reduces by a factor N^3 . Multiphase PWM therefore allows for less expensive coils with lower inductance value, lower current rating, smaller individual core volume, and associated footprint.

Note that even when the maximum ripple amplitude is kept constant, a multiphase PWM system still has lower ripple around zero signal levels, which are the most likely signals in audio content. The ripple current in the summation over the load cancels completely when the input signal equals zero as is shown in Fig. 12.

C. Multiphase PWM Implementation

The digital multiphase pulse-width modulator has a configurable fPWM (between 460 kHz and 1 MHz, typically 501 kHz) as well as programmable phase relations. The power stages operate in BTL configuration, as shown in Fig. 13 [32] and enable both AD (1-phase), BD (2-phase) and several

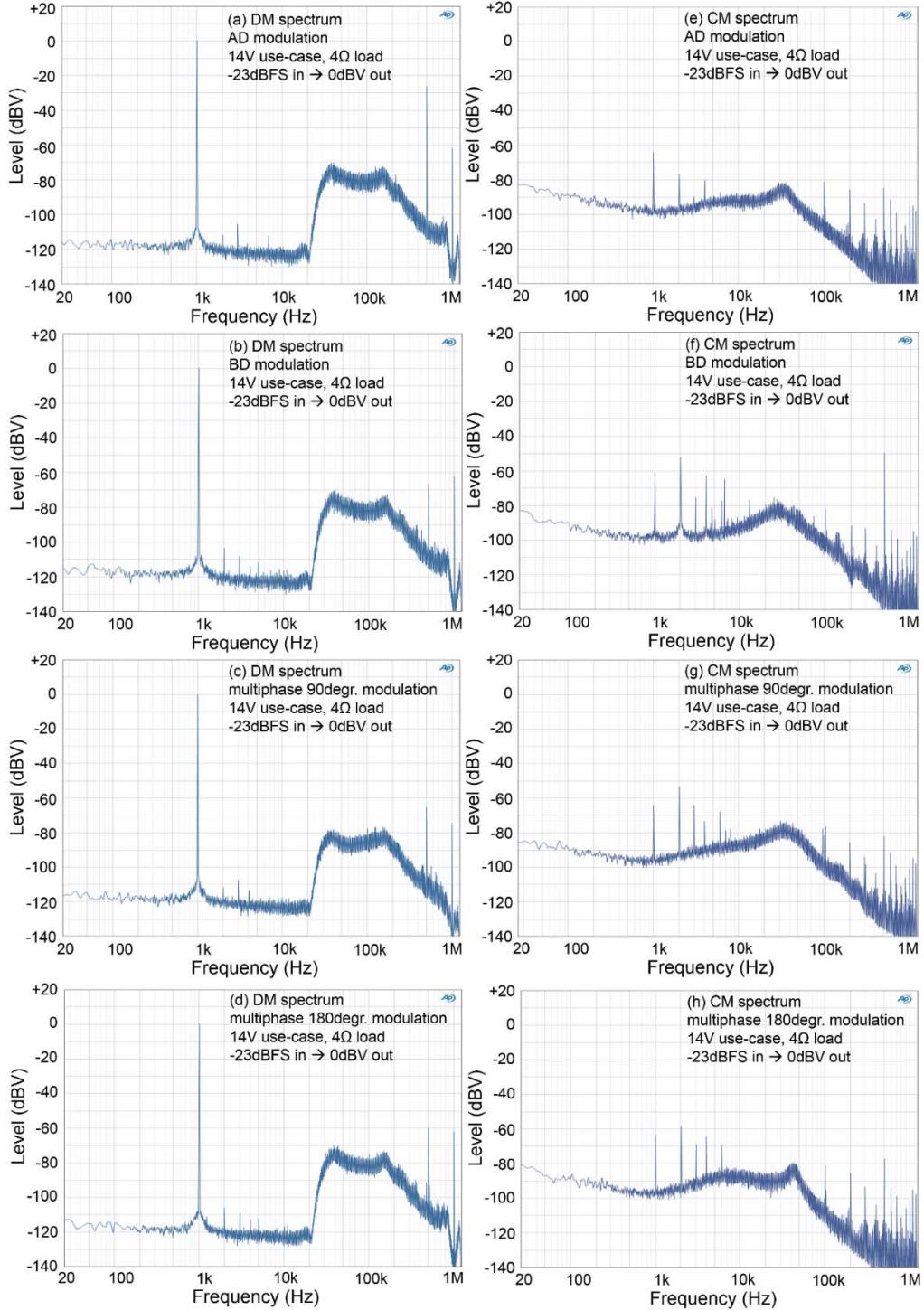


Fig. 17. Measured spectra for both DM with (a) AD modulation, (b) BD, multiphase 90°. (c) and (d) multiphase 180° with 2 phases for DM and 2 for CM and (e)–(h) accompanying CM spectra.

4-phase operations. In 4-phase operation, the phase distribution between the various legs influences the amount of DM versus CM ripple. For automotive applications low CM ripple can be even more important than DM ripple, because the long speaker wires can be good CM radiators.

A point of attention in a multiphase system is the potential for large circulating currents [6]. Voltage offsets between the

different output stages can create these circulating currents between stages. In analog loops, a way to reduce these currents is to use a current-balance control loop, which usually requires some sort of current sense mechanism in each of the class-D output stages. With digital PWM we can omit actual measurements of the analog outputs and instead use digital integrators within the pulse-width modulator to ensure that all outputs

TABLE I
PERFORMANCE TABLE AND COMPARISON TO PRIOR WORK

Parameter (condition)	This work	[1] Adduci & ST datasheet part FDA4100LV	[4] Mouton	[31] Berkhouit	[23] Hoyerby	[30] Ma	Maxim datasheet part MAX13301
THD+N (BTL, 4Ω)	0.004% @ 1W 0.005% @ 10W (full audio band)	0.04% @ 5W, 1kHz 0.2% @ 10W, 10kHz	30W, 1kHz 0.0058% @ 30W, 10.5kHz	0.016% @ 3W, 1kHz, 8Ω	0.003% @ 10W, 1kHz 0.01% @ 10W, 6kHz	0.03% @ 6VA, 1kHz 0.05% @ 3VA, 2kHz (3Ω-2.2μF)	0.04% @ 10W, 1kHz
Dynamic Range (A-weighted)	115 dBA	108 dBA			110 dBA		102 dB
Output noise (A-weighted)	19 uVrms @ 14V 34 uVrms @ 25V	60 uVrms			65 uVrms		100 uVrms
PSRR	88 dB @ 100Hz 70 dB @ 1kHz	85 dB @ 1kHz					60 dB @ 100-10k Hz
Feedback topology	digital FeedBack- AfterFilter	analog FeedBack- AfterFilter	digital FeedBack- AfterFilter	analog FeedBack- BeforeFilter	analog FeedBack- BeforeFilter		analog FeedBack- AfterFilter
Power stage supply voltage	14.4V or 25V	25V	25V	85V	24V	80V	24V
Max output power/channel @ 10%THD, 4Ω, BTL	80W	100W	30W	460W	70W	45VA	80W
Max total output power (sum of all channels)	400W	400W	30W	460W	140W	45VA	320W
Process	140nm BCD SOI	BCD SOI	non silicon integrated system	BCD SOI	180nm BCD dual-oxide	140nm BCD SOI	

get equal signal levels [41]. As such, this digital pulse-width modulator offers a simple and cost effective way to prevent circulating currents in multiphase systems.

V. EXPERIMENTAL RESULTS

The amplifier is fabricated in 140-nm bipolar CMOS DMOS SOI technology. A die micrograph is shown in Fig. 14. Each of the 5 multiphase channels is buildup of 4 power stages and can deliver up to 8 A current at 25-V supply. The efficiency of the amplifier system, including energy losses in the filters, is plotted in Fig. 15 and surpasses 90% at maximum output power.

Fig. 16 shows the measured THD+N results for three different input frequencies; 100 Hz, 1 kHz, and 6 kHz. The loop gain that is high over the entire audio band gives good performance at all three frequencies. The amplifier has a THD+N of 0.004% at 1 W and 0.005% at 10 W for all three frequencies. The floor in the THD+N is determined by the noise of the integrated ADC reference. The maximum output power, measured at 10% THD, is 80 W per channel. The idle noise of the amplifier is 19 μV (Awtd, at 14.4 V), resulting in a DR of 115 dBA for the complete system.

DM and CM spectra measured at the load are shown in Fig. 17 for four different PWM configurations. Fig. 17(a) and (e) shows AD mode, which corresponds to a 2-level PWM output signal and therefore shows a high (-30 dBV) f_{PWM} frequency component at 501 kHz in the DM spectrum, while the CM spectrum is very clean. The 3-level PWM configuration, also referred to as BD modulation, is shown in Fig. 17(b) and (f) and shows a reduction in DM f_{PWM} of more than 40 dB. For BD modulation, the CM

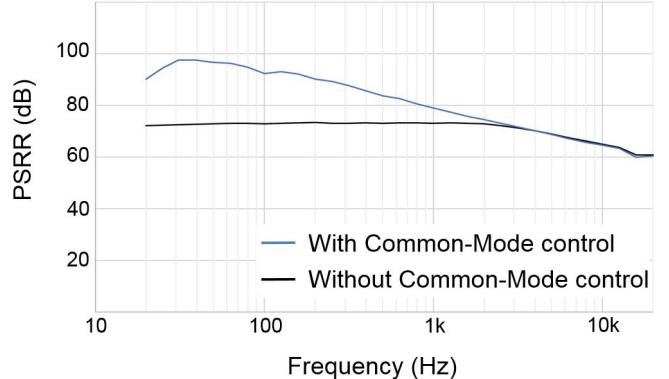


Fig. 18. PSSR.

does exhibit a significantly larger f_{PWM} component [6]. Fig. 17(c) and (g) shows a multiphase configuration with each PWM phase shifted by 90°. In this mode, the DM spectrum has a reduced ripple at 1 and 2 times f_{PWM} as well as a 6 dB reduction of the out-of-band quantization noise. The CM PWM components now resemble that of AD modulation. The last configuration [Fig. 17(d) and (h)] shows a multiphase variation with 180° phase shift between the phases, intended to further reduce the CM EMI (the noise part) at the cost of slightly increased DM EMI.

Fig. 18 shows the measured PSR ratio (PSRR) of the amplifier. With the CM loop inactive, PSRR reaches a plateau at 70 dB due to mismatch between the conversion resistors. As discussed in [42], PSRR can be improved with the addition of a CM control loop. In this paper, activation of the second-order CM feedback loop improves the PSRR to 88 dB at 100 Hz.

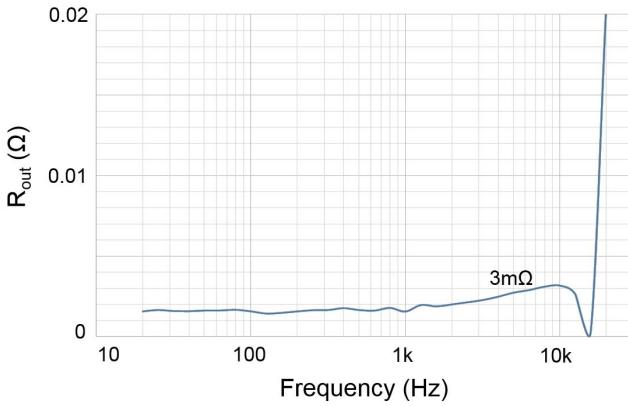


Fig. 19. Output impedance.

Fig. 19 shows the output impedance. The feedback after the output filter topology results in only $1.5 \text{ m}\Omega$ at 1 kHz and $3 \text{ m}\Omega$ at 16 kHz. These impedances are measured at the load and result in high damping factors, with an input–output transfer that is independent on actual load conditions.

Table I shows that the presented amplifier achieves the lowest output noise combined with the highest dynamic range of all integrated amplifiers. At comparable supply levels, it has 2 times lower noise. Compared to the other integrated amplifier that uses feedback after the output filter [1], the THD + N is a factor 10 lower at 1 kHz and even a factor 40 at higher frequencies, where the loop-gain in [1] is low. The amplifier prototype with digital feedback from [4] also shows good performance, but with an expensive, power hungry, commercially available ADC. The multilevel amplifier from [23] shows on par performance at lower input frequencies, but with reduced performance at 6 kHz.

VI. CONCLUSION

In this paper, we have presented the first integrated class-D amplifier that uses digitized feedback after the output filter. The digital fifth-order loop filter has >50 dB loop gain over the whole audio band, which creates high PSRR and mitigates the influence of the *LC* filter on the transfer and the linearity. The cost of these filter components can thus be reduced as some non-linear filter effects (e.g., mild core saturation) become tolerable.

To digitize the signal at the load, a special low-latency $\Delta\Sigma$ ADC was developed. The ADC uses filtering in its feedback path to create an extrapolating behavior with negative group delay at low frequencies, such that a subsequent digital low-pass filter can reduce the quantization noise without creating a net delay (as delay would compromise loop stability).

The amplifier can also be configured for multiphase operation in which case it uses four inductors per channel. The multiphase operation can be applied to increase the effective fPWM and reduce the ripple, but without the switching loss and EMI drawbacks that a higher actual switching frequency would give. It can also be applied to further reduce inductor costs, because for a given output ripple, both the value and current rating of the inductors can be decreased when using multiple phases.

The result is an amplifier that has state-of-the-art noise performance of $19 \mu\text{V}$ at 14.4-V supply, more than 90% system efficiency and 10 times lower THD+N than its closest competitor [1].

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Daniel Schinkel (S'03–M'08) received the M.Sc. (Hons.) degree in electrical engineering and the Ph.D. degree in high-speed on-chip communication from the University of Twente, Enschede, The Netherlands, in 2003 and 2011, respectively.

His Ph.D. research was carried out between 2003 and 2007 at the IC-Design Group, Enschede, headed by Bram Nauta. He is one of the founders of Axiom IC, Enschede, an IC-design company that started in 2007, which focused on the design of data-converters and mixed-signal systems. Axiom IC was acquired in 2013 by Teledyne DALSA. Since 2013, he has been an Independent Research Consultant with IC companies as well as for the University. He has authored or co-authored about 25 papers and holds four patents. His current research interests include analog, digital, and mixed-signal circuit design, sigma-delta data converters, class-D power amplifiers, and high-speed communication circuits.



Wouter Groothedde (S'02–M'16) was born in Purmerend, The Netherlands, in 1977. He received the M.Sc. degree in electrical engineering from the University of Twente, Enschede, The Netherlands, in 2003.

From 2003 to 2007, he was with National Semiconductor, Delft, The Netherlands, involved in developing delta-sigma modulator ADCs for audio subsystems and digital microphones. In 2007, he joined the startup Axiom IC, Enschede. In 2013, Teledyne DALSA, Enschede, acquired Axiom IC, where he is currently a System Architect in high-resolution data converters. He holds patents in the area of digital microphones and low-latency AD converters. His current research interests include high-resolution (audio) DACs, ADCs, and digital class-D amplifiers.



Fred Mostert was born in Groningen in 1959. He received the B.Eng. degree from HTS, Groningen, The Netherlands.

From 1982 to 1999, he was an IC Designer at Philips, involved in CCD filters, modems, PLL, and transceivers. In 1999, he joined the Automotive Audio Amplifier Group, Philips/NXP, Nijmegen, The Netherlands, as an IC designer/Architect.



Marto-Jan Koerts was born in Haasten, The Netherlands, in 1967. He received the Ing. degree from the Hogeschool Rotterdam, Rotterdam, The Netherlands, in 1993.

From 1994 to 2001, he was with ABB, Delft, The Netherlands. He is currently a Mixed Signal Design Engineer with NXP, Nijmegen, The Netherlands.



Eric van Iersel was born in Waalwijk, The Netherlands, in 1966. He received the Ing. degree in electrical engineering from HTS, 's-Hertogenbosch, The Netherlands, in 1988.

He was a Test Developer and a Product Engineer with Philips Semiconductors, Nijmegen, The Netherlands, from 1990 to 2000. Since 2000, he has been an IC Designer and an IC Architect with the Automotive Audio Amplifier Group, Philips/NXP, Nijmegen.



Daniel Groeneveld (S'10) was born in Goor, The Netherlands, in 1986. He received the M.Sc. degree in electrical engineering from the University of Twente, Enschede, The Netherlands, in 2010.

In 2010, he joined Axiom IC, Enschede. In 2013, Teledyne DALSA, Enschede, acquired Axiom IC, where he is currently an Analog Design Engineer.



Lucien Breems (S'97–M'00–SM'07) received the M.Sc. (*cum laude*) and Ph.D. degrees in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 1996 and 2001, respectively.

From 2000 to 2007, he was with Philips Research, Eindhoven, The Netherlands. Since 2011, he has been a part-time Professor with the Technical University of Eindhoven, Eindhoven. He is currently a Fellow with NXP Semiconductors, Eindhoven. His current research interests include wireless receivers

and data converters.

Prof. Breems is a Technical Program Committee Member of the Internal Solid-State Circuits Conference, the European Solid-State Circuits Conference, the Symposium on VLSI Circuits, and the IEEE International Symposium on Low Power Electronics and Design. From 2009 to 2014, he has been an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and served as a Guest Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-II, in 2008–2009. He has been an IEEE Distinguished Lecturer (2012–2013) and a co-recipient of the ISSCC “Jan van Vesse” Outstanding Paper Award in 2001, 2011, and 2016, the IEEE Journal of Solid-State Circuits Best Paper Award in 2011, and the RFIC Industry Best Paper Award in 2016.