## IEEE JOURNAL OF

## SOLID-STATE CIRCUITS

A PUBLICATION OF THE IEEE SOLID-STATE CIRCUITS SOCIETY



OCTOBER 2017 VOLUME 52 NUMBER 10 IJSCBC (ISSN 0018-9200)

Introducing Our Sister Publication: IEEE Solid-State Circuits Letters J. R. Long, J Craninckx, and B. Razavi	2519
SPECIAL SECTION ON THE 2016 ASIAN SOLID-STATE CIRCUITS CONFERENCE (A-SSCC 2016)	
SPECIAL SECTION PAPERS	
Introduction to the Special Section on the 2016 Asian Solid-State Circuits Conference (A-SSCC 2016)	2521
A Low-Noise Area-Efficient Chopped VCO-Based CTDSM for Sensor Applications in 40-nm CMOS	2523
Multiple-Loop Design Technique for High-Performance Low-Dropout Regulator	
QH. Duong, HH. Nguyen, JW. Kong, HS. Shin, YS. Ko, HY. Yu, YH. Lee, CH. Bea, and HJ. Park Triple-Mode, Hybrid-Storage, Energy Harvesting Power Management Unit: Achieving High Efficiency Against	2533
Harvesting and Load Power Variabilities	2550
60-dB SNDR 100-MS/s SAR ADCs With Threshold Reconfigurable Reference Error Calibration	2563
	2576
A 41.3/26.7 pJ per Neuron Weight RBM Processor Supporting On-Chip Learning/Inference for IoT	2589
Applications	2601
V. Derudder, U. Ahmad, A. Spagnolo, I. Ocket, A. Bourdoux, P. Wambacq, J. Craninckx, and W. Van Thillo A 1.9-mW 750-kb/s 2.4-GHz F-OOK Transmitter With Symmetric FM Template and High-Point	2613
Modulation PLL	2627
B. Jiang and H. C. Luong Fractional-N DPLL-Based Low-Power Clocking Architecture for 1–14 Gb/s Multi-Standard Transmitter	2636
M. Hossain, W. El-Halwagy, A. K. M. D. Hossain, and Aurangozeb A 32.75-Gb/s Voltage-Mode Transmitter With Three-Tap FFE in 16-nm CMOS	2647
Y. Frans, J. Im, P. Upadhyaya, S. W. Lim, A. Roldan, N. Narang, C. Y. Koay, H. Zhao, PC. Chiang, and K. Chang A Neuromorphic Chip Optimized for Deep Learning and CMOS Technology With Time-Domain Analog and Digital	2663
Mixed-Signal Processing	2679
A 1.1-mW Ground Effect-Resilient Body-Coupled Communication Transceiver With Pseudo OFDM for Head and Body Area Network	2690

(Contents Continued on Back Cover)



## (Contents Continued from Front Cover)

Energy-Efficient Reconfigurable SRAM: Reducing Read Power Through Data Statistics	2702
A 2-GS/s 8-bit Time-Interleaved SAR ADC for Millimeter-Wave Pulsed Radar Baseband SoC	2703
T. Miki, T. Ozeki, and Ji. Naka	2712
REGULAR PAPERS	
A 170-GHz Fully Integrated Single-Chip FMCW Imaging Radar With 3-D Imaging Capability	
A. Mostajeran, A. Cathelin, and E. Afshari	2721
A 48-MHz Differential Crystal Oscillator With 168-fs Jitter in 28-nm CMOS	
Y. Rajavi, M. M. Ghahramani, A. Khalili, A. Kavousian, B. Kim, and M. P. Flynn	2735
An Inductorless Bias-Flip Rectifier for Piezoelectric Energy Harvesting	2746
An Efficient Buck/Buck-Boost Reconfigurable LED Driver Employing SIN <sup>2</sup> Reference	
K. Cho and R. Gharpurey	2758
A 65-nm ReRAM-Enabled Nonvolatile Processor With Time-Space Domain Adaption and Self-Write-Termination	
Achieving >4× Faster Clock Frequency and >6× Higher Restore Speed	
Z. Wang, Y. Liu, A. Lee, F. Su, CP. Lo, Z. Yuan, J. Li, CC. Lin,	
WH. Chen, HY. Chiu, WE. Lin, YC. King, CJ. Lin, P. Khalili Amiri, KL. Wang, MF. Chang, and H. Yang	2769