

# A 10-bit DC-20-GHz Multiple-Return-to-Zero DAC With >48-dB SFDR

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**Abstract**—A dc-20-GHz multiple-return-to-zero digital-to-analog converter (DAC) is proposed for direct radio frequency synthesis. To minimize frequency-dependent amplitude and phase errors in the output summing node, which can dominate linearity performance at GHz and mm-wave frequencies, a vertically stacked tree (VST) and feed-forward (FF) path are proposed. While the VST minimizes variation in frequency response among the MSBs, the FF path improves matching between the MSBs and LSBs, providing up to 21-dB improvement in simulated spurious-free dynamic range (SFDR) at 20 GHz. To account for additional errors introduced by process variation, the DAC utilizes per-cell calibration of both amplitude and timing. The DAC is implemented in a 0.13- $\mu\text{m}$  SiGe process with an area of 6.25 mm<sup>2</sup> and consumes 1.91 W. After amplitude and timing calibration, >48-dB SFDR and lesser than -46 dBc intermodulation distortion are achieved from dc to 20 GHz.

**Index Terms**—Current-steering (CS), digital-to-analog converter (DAC), direct digital-to-RF, high linearity, high speed, multiple Nyquist, return-to-zero (RZ), RF-DAC.

## I. INTRODUCTION

DEMAND for 5G communications, military radars, and arbitrary waveform generators has expanded into the mm-wave (mmW) spectrum while requiring GHz of instantaneous bandwidth. Traditionally, high-frequency synthesis is achieved via a baseband digital-to-analog converter (DAC) followed by a mixer. However, wideband linearization of the mixer  $g_m$  stage, and the need for a local oscillator (LO) that is swept through the full frequency range, compounds the design challenges in the push to mmW [1]. To remove the mixer bottleneck, direct radio frequency (RF) synthesis has been proposed, placing strict demands on the high-frequency linearity performance of the DAC [2].

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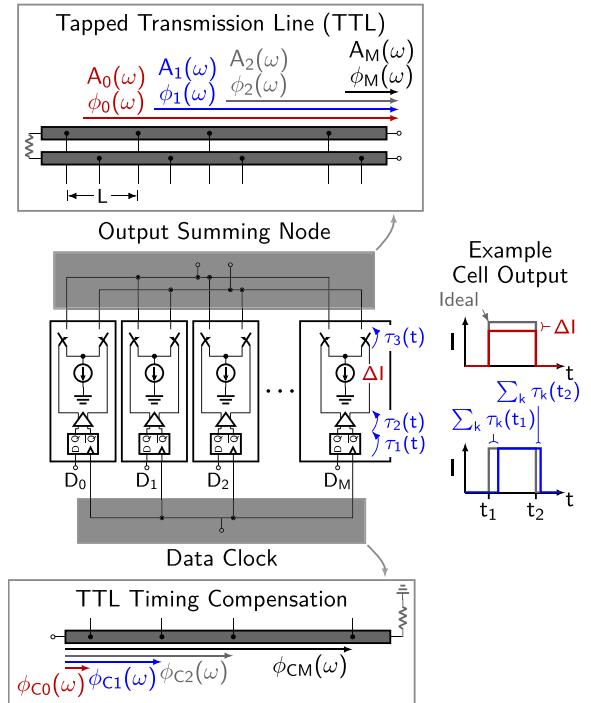


Fig. 1. Block diagram of a CS DAC showing sources of amplitude ( $\Delta I$ ) and timing [ $\tau_k(t)$ ] variation within the cell. The TTL used for the summing node induces additional amplitude [ $A_i(\omega)$ ] and phase variation [ $\phi_i(\omega)$ ]. TTL timing compensation [ $\phi_{Ci}(\omega)$ ] on the clock distribution network can be used to partially compensate for phase variation in the summing node.

For direct RF synthesis, the current-steering (CS) DAC architecture, shown in Fig. 1, is preferred for its high-speed operation. The CS DAC is comprised of an array of weighted current switching cells, which are combined at the output summing node (OSN). The linearity of the DAC is determined by the matching of amplitude and timing among current cells, whereas amplitude errors (e.g.,  $\Delta I$ ), arising from current cell variations, can limit the spurious-free dynamic range (SFDR) at all frequencies, timing errors have an increasing impact with frequency [3]–[6]. These timing errors are introduced by skewed propagation delay and data-dependent deterministic jitter (DJ) in the retiming flip-flop (RTFF) and data driver, as well as threshold modulation in the switch pair [4]. Moreover, as the DAC physical size approaches the wavelength of the output frequency, variations in amplitude and phase in the OSN and clock distribution introduce frequency-dependent errors, which further degrade SFDR [3], [7], [8]. While the static (i.e., time-invariant)

portion of mismatch can be calibrated, dynamic (i.e., time-variant) errors, such as DJ, can be difficult to correct. For example, in non-return-to-zero (NRZ) CS DACs with sample rates up to 56 GS/s, data path jitter limits SFDR to 31 dB at 27 GHz [9], [10].

To improve high-frequency SFDR performance, recently reported GHz DACs have focused on techniques to mitigate the expanding impact of DJ on SFDR as sample rates increase [5], [6]. Return-to-zero (RZ) techniques can be used to de-glitch the data path, both reducing these dynamic errors and allowing synthesis in the second Nyquist zone (NZ). Unfortunately, dynamic errors still affect a sizable portion of the clock period, limiting reported RZ DACs to 7-GHz and 55-dB SFDR [11]–[15]. To further alleviate sampling requirements, time interleaving has been proposed, demonstrating 50- and 27-dB SFDR at 5.5 and 25 GHz, respectively [16]–[20]. However, interleaving spurs can limit SFDR, while the increased DAC area can exacerbate inter-DAC timing skew. Alternatively, the output frequency can be decoupled from the sample rate via a mixing DAC to perform direct up-conversion of the signal, yielding 50-dB SFDR across the NZ at 5 GHz and 1.75 GS/s [7], [21], [22]. Unfortunately, mixing DACs do not perform de-glitching and require careful alignment of the sample and mixing clocks, creating a tradeoff between sample rate, output frequency, and SFDR. To address these shortcomings, the multiple-return-to-zero (MRZ) approach combines RZ and mixing to simultaneously suppress DJ and enable direct up-conversion [23], [24]. Recently, an MRZ DAC has achieved 42-dB SFDR at 9.45 GHz and 2.7 GS/s without calibration, making it a promising approach for mmW synthesis [24].

In addition to the DAC architecture, the process technology is critical to achieving high linearity. Although CMOS scaling has benefited from reduced parasitic and fast switching, limited output impedance results in large dynamic errors within the cell circuitry [10], [16], [17]. Alternatively, SiGe and InP HBTs enable highly linear current cells due to their higher output impedance and switching speeds, however, the large device footprint exacerbates mismatches in the clock distribution and OSN [13]–[15]. This effectively shifts the dominant source of nonlinearity to the clock and output nodes, thereby offsetting any improvements from the linearized cells.

To further improve linearity, calibration techniques can be applied to correct mismatches in the clock distribution network and unit cell transistors [6]. While amplitude calibration has been extensively studied [25]–[30], timing calibration has received less attention, especially when operating at mmW. Recently proposed methods for timing calibration include per-cell programmable delay [31] and mapping techniques [22], [32], [33]. Both methods have limited applicability to mmW operation as the former limits clock slew rates while the latter depends on a statistically significant number of ( $\geq 64$ ) current cells, increasing the cell array size and precluding its application to SiGe or InP DACs. Unfortunately, none of these approaches account for frequency-dependent variations induced by the OSN, thus requiring careful analysis and optimization to maximize SFDR across frequency. For example, the simulation of the OSN with

*RC* parasitic has shown a variation of 7–20 fs for a CMOS mixing DAC at 5 GHz [7]. However, the shrinking wavelength at mmW requires EM modeling and simulations to account for inductive effects, thereby enabling thorough mitigation OSN errors.

This paper presents a 10-bit 3.35-GS/s MRZ DAC capable of synthesizing frequencies from dc to 20 GHz with >48-dB SFDR in a 0.13- $\mu\text{m}$  SiGe process. The design introduces a vertically stacked tree (VST) structure that minimizes amplitude and phase mismatches in the OSN, thereby mitigating the impact of the large array size on SFDR. An analysis shows that the VST improves SFDR at frequencies above 1 GHz and provides a 21-dB improvement at 20 GHz. Additionally, the DAC utilizes per-cell amplitude and timing calibration to correct errors introduced by process variation. Measurement results show up to 7-dB improvement in SFDR at 20 GHz with calibration. The combination of the VST and calibration techniques yields the highest reported SFDR at 20 GHz while synthesizing the highest instantaneous bandwidth among RF DACs with output frequencies above 5 GHz.

The MRZ DAC architecture is discussed in Section II. Section III provides an analysis of errors that arise from the OSN and proposes an optimized structure to maximize 20-GHz performance. Section IV covers the implementation details, including a per-cell timing adjustment circuit. Measurement results are detailed in Section V, with concluding remarks in Section VI.

## II. MRZ DAC ARCHITECTURE

As noted earlier, the MRZ architecture is a composite of RZ and mixing DAC techniques. The three architectures can be conceptualized as an NRZ DAC followed by multiplication with an RZ or LO waveform. As shown in Fig. 2(a), the RZ DAC multiplies the output with zero for half of each clock period ( $f_{RZ} = f_s = 1/T_s$ ), while the data are switched, blocking DJ from the output. Moreover, the RZ frequency response, shown in Fig. 3, locates the first null at  $2 f_s$ . This enables synthesis in the second NZ, relaxing the required sample rate by  $2\times$  for a given output frequency ( $f_{OUT}$ ) at the cost of a 6-dB reduction in output power ( $P_{OUT}$ ) at dc compared with NRZ. However, to achieve  $f_{OUT} = 20$  GHz, a sample rate of >20 GS/s is still required to place the signal within the second NZ, limiting SFDR due to coupling of high-speed data-dependent nodes to the RZ clock. To further reduce  $f_s$  independently of  $f_{OUT}$ , the RZ clock can be replaced with an LO ( $f_{LO} = m_{mx} f_s$ ), as shown in Fig. 2(b), to realize a mixing DAC. The frequency response of a mixing DAC, shown in Fig. 3 for  $m_{mx} = 3$ , exhibits a lobe centered at  $f_{LO}$  with a peak amplitude of -3.8 dB relative to the DAC full-scale range (FSR). While the mixing DAC can achieve arbitrarily high  $f_{OUT}$  for a given  $f_s$ , DJ from the data path feeds directly to the output, creating a tradeoff between sample rate and linearity. Additionally, the SFDR performance depends on the alignment between DCLK and LO. It has been shown that an alignment of  $<20^\circ$  of the LO is required, exacerbating timing requirements with increasing  $f_{OUT}$  [7].

The MRZ architecture solves several shortcomings of RZ and mixing DACs by increasing the RZ frequency

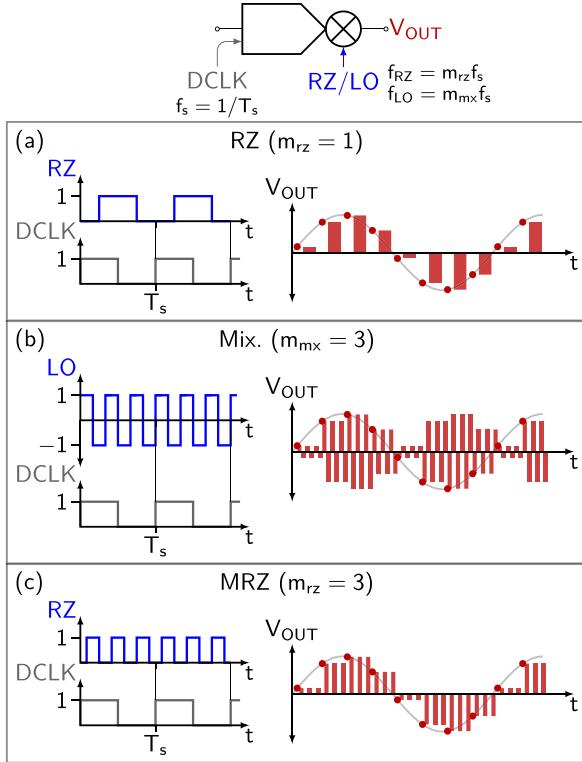


Fig. 2. Example clock and output waveforms for (a) RZ DAC, (b) mixing DAC with  $m_{mx} = 3$ , and (c) MRZ DAC with  $m_{rz} = 3$ .

( $f_{RZ} = m_{rz}f_s$ ), as shown in Fig. 2. Note that RZ is a special case of MRZ in which  $m_{rz} = 1$ . As with the RZ DAC, the MRZ approach mitigates DJ by resetting the output, while the data are switched, and only ideally requires DCLK alignment to within  $180^\circ$  of  $f_{RZ}$ . Assuming an RZ clock with duty cycle,  $d$ , the MRZ frequency response can be derived as

$$H_H(\omega) = \frac{dT_s}{m_{rz}} \cdot \text{sinc}\left(\frac{dT_s\omega}{2m_{rz}}\right) \cdot \frac{\sin(0.5\omega T_s)}{\sin(0.5\omega T_s/m_{rz})} \cdot e^{-\frac{j\omega T_s}{2}}. \quad (1)$$

At 50% duty cycle ( $d = 0.5$ ),  $|H_H(\omega)|$  exhibits a major lobe centered on  $f_{RZ}$ , with a peak amplitude of  $-9.8$  dB normalized to the FSR, as shown in Fig. 3 for  $m_{rz} = 3$ . Compared with a mixing DAC, this results in a 6-dB reduction in  $P_{OUT}$ . Nonetheless, the mitigation of DJ and relaxed clock alignment make MRZ a compelling option for achieving high linearity at mmW.

The proposed 10-bit DAC architecture is shown in Fig. 4, wherein the MRZ operation is performed via local RZ switches in each cell. In contrast to global RZ, local switching divides the RZ process into linear 1-bit operations [12], [34]. The linearity then largely depends on amplitude and phase matching in the OSN and clock distribution. As a trade-off between area,  $P_{OUT}$ , and current matching, the DAC is segmented into 15 unary MSB cells and 6 binary LSBs. Binary scaling is achieved using an  $R-2R$  network, which provides a  $100\Omega$  differential termination [12], [15], [24]. The  $R-2R$  scaling enables the use of identical cells for MSBs and LSBs, minimizing timing mismatch by ensuring uniform RZ clock loading. Furthermore, the  $R-2R$  network is advantageous in HBT designs, where the minimum device

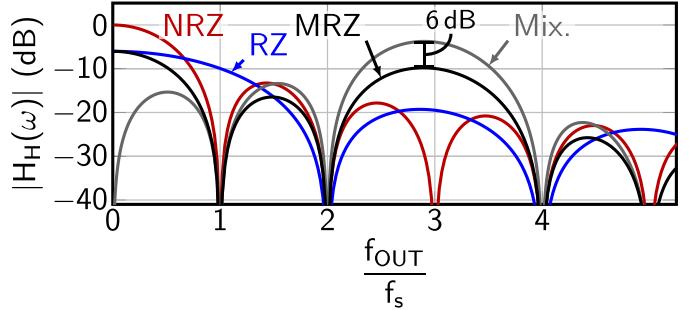


Fig. 3. Magnitude of the frequency response for NRZ, RZ, mixing ( $m_{mx} = 3$ ), and MRZ waveforms ( $m_{rz} = 3$ ), normalized to the FSR.

size is much larger than that of CMOS. Conventional binary scaling results in small LSB cell currents, yielding low  $f_T$  in a minimum-size HBT and hence slower switching than in MSBs. In contrast,  $R-2R$  scaling allows for uniform current density, and hence switching speed, throughout all cells. Note that each LSB propagates through a different number of  $R-2R$  stages, incurring amplitude, and phase variations due to the  $RC$  time constant of each stage. However, ensuring that  $f_{OUT} \ll (2\pi RC)^{-1}$  results in a minor deterministic effect that can be calibrated, as detailed in Section IV.

### III. OUTPUT SUMMING NODE

As the wavelength of operation approaches the DAC physical size, variations in amplitude and phase shift in the OSN can lead to frequency-dependent errors among MSB cells, which end up dominating SFDR. The measurement, and therefore calibration, of such errors over large bandwidths is quite challenging. Instead, Section III-B introduces an alternative OSN structure, which minimizes mismatch across frequency, enhancing linearity and relaxing calibration requirements.

#### A. Tapped Transmission Line

A simple way to sum the MSB output currents is to connect them to a transmission line at a uniform spacing,  $L$ , forming the tapped transmission line (TTL) shown in Fig. 1. The TTL is terminated by the  $R-2R$  network on one side and connects to the output pads on the other. This approach is advantageous at GHz and mmW, where each cell capacitance can be absorbed into the distributed capacitance of the TTL, yielding a simple characteristic impedance that can be designed for minimal attenuation and reflections. The TTL has been used in DACs with output frequencies up to 9.45 GHz employing III-V technologies, where  $L$  must accommodate the large footprint of the devices, resulting in a large cell array relative to the wavelength [15], [24].

Although the TTL minimizes attenuation and reflections in the OSN, unequal path lengths between each cell and the output lead to variations in attenuation and phase that degrade SFDR. To quantify the performance of the TTL, the combined frequency-domain output,  $Y(\omega)$ , of a DAC with  $M$  unary ( $m = 0 \dots M - 1$ ) and  $N$  binary ( $n = 0 \dots N - 1$ ) cells can be decomposed into the contribution from the output of

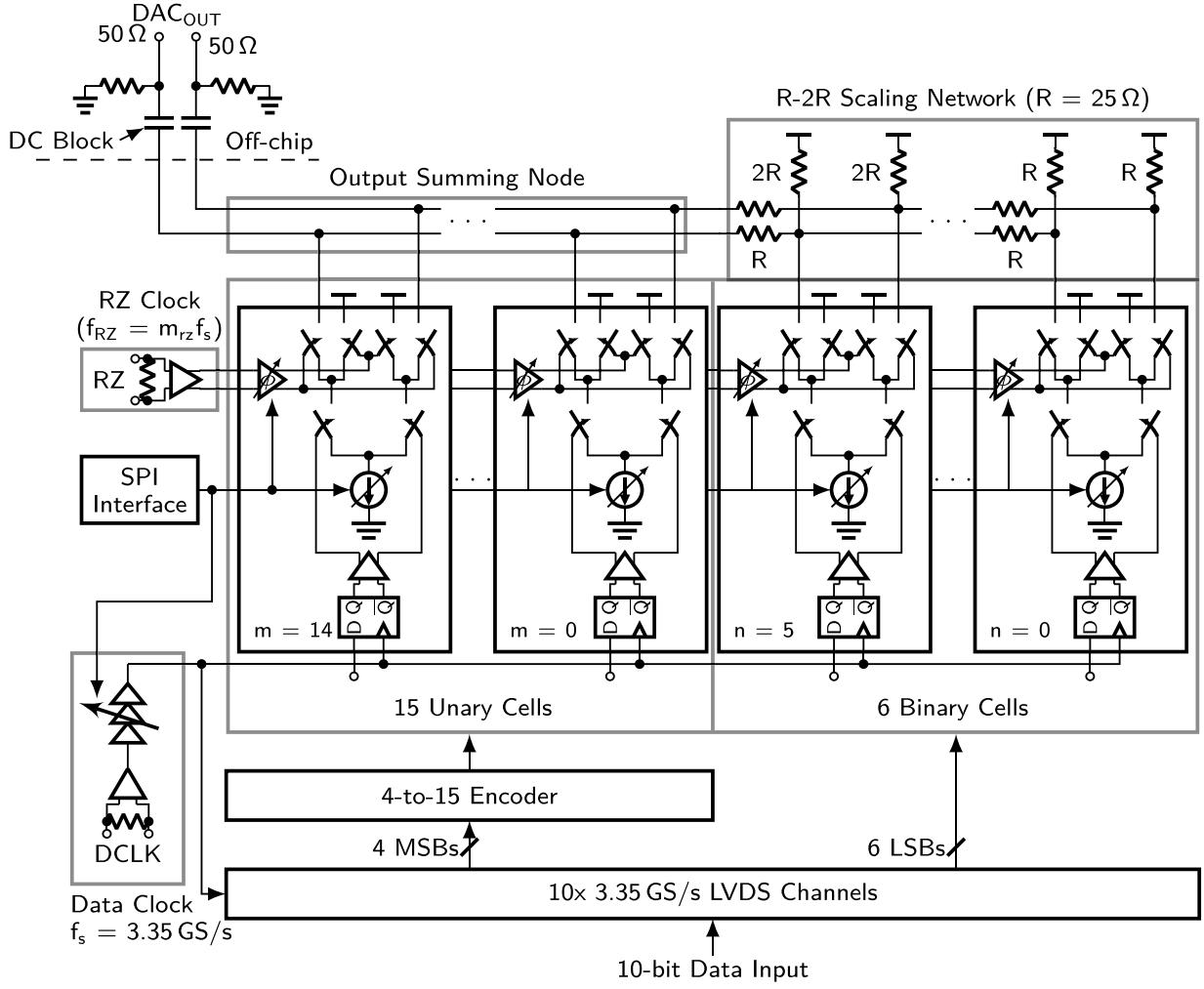
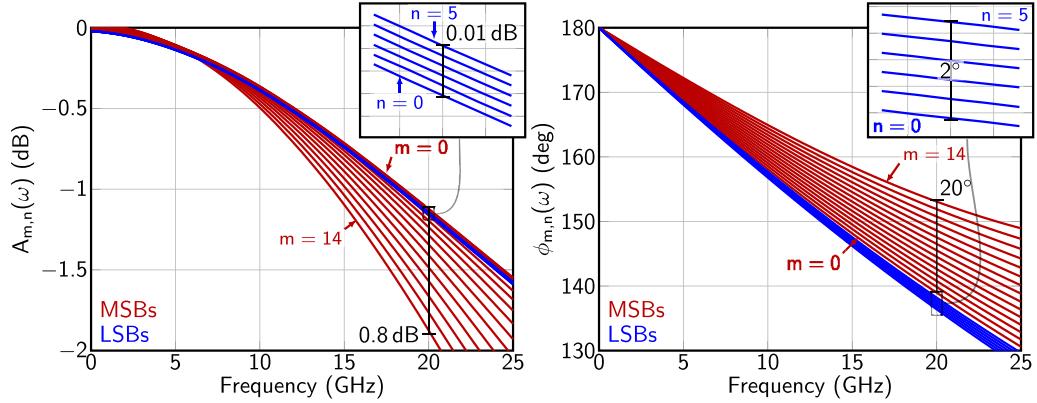


Fig. 4. Block diagram of the 10-bit MRZ DAC.

Fig. 5. Frequency response of each cell in the TTL summing node for  $L = 25 \mu\text{m}$ .

each cell  $[X_{\{m,n\}}(\omega)]$  such that

$$Y(\omega) = \sum_{m=0}^{M-1} A_m(\omega) e^{j\phi_m(\omega)} X_m(\omega) + \sum_{n=0}^{N-1} \frac{1}{2^{N-n}} A_n(\omega) e^{j\phi_n(\omega)} X_n(\omega) \quad (2)$$

where  $A_{\{m,n\}}(\omega)$  and  $\phi_{\{m,n\}}(\omega)$  are the amplitude and phase response, respectively, for each cell. Fig. 5 shows the simulated frequency response of each cell in the proposed 10-bit DAC

( $M = 15$  and  $N = 6$ ) using an EM model of the TTL with  $L = 25 \mu\text{m}$ . The LSBs exhibit a small variation in attenuation and phase (0.01 dB, 2° at 20 GHz), indicating that the  $RC$  time constant of each  $R-2R$  stage is small relative to  $f_{\text{OUT}}$ . However, among the 15 MSB cells, the TTL displays a peak-to-peak variation of 0.8 dB and 20° at 20 GHz. To illustrate the performance impact of this variation, SFDR is simulated for various  $L$  and the results are displayed in Fig. 6(a). For  $L = 25 \mu\text{m}$ , the SFDR degrades by 48 dB at 20 GHz from the ideal case ( $L = 0 \mu\text{m}$ ). It is worth noting that even with

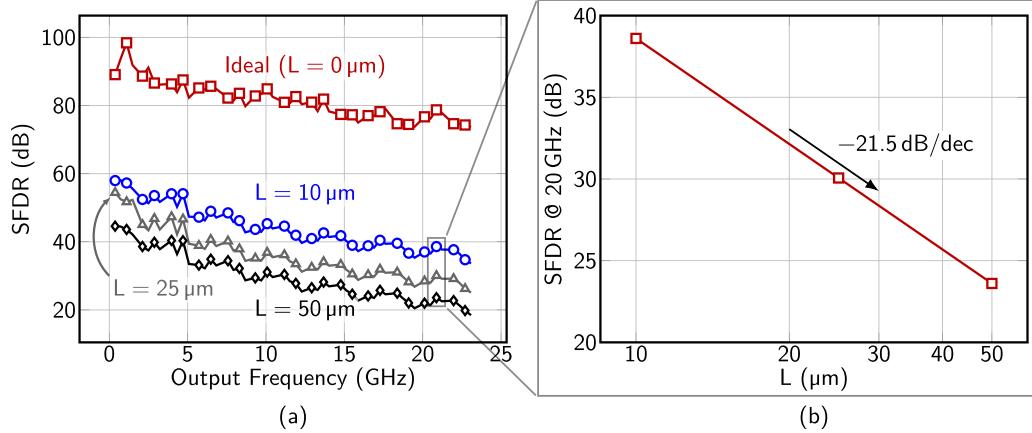


Fig. 6. Simulated SFDR performance of the TTL across (a) frequency and (b) cell spacing,  $L$ , at 20 GHz.

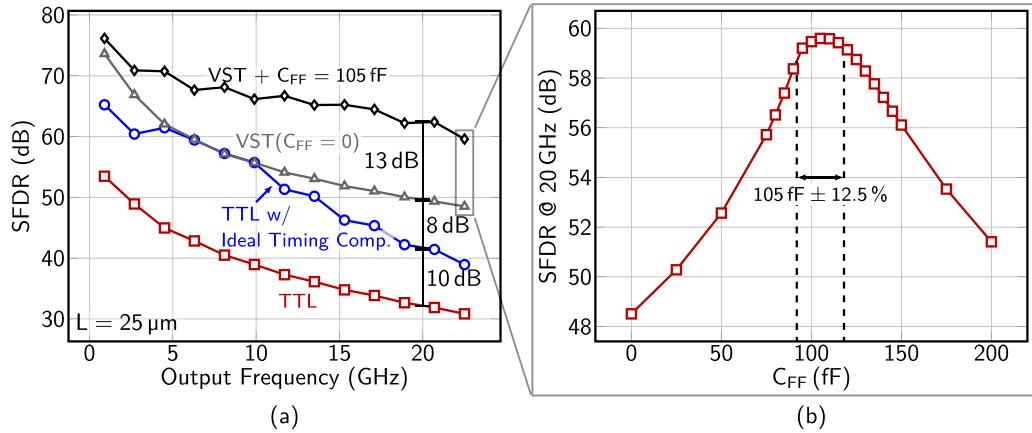


Fig. 7. Simulated (a) SFDR performance of the TTL, TTL with ideal timing compensation, standalone VST, and VST with  $C_{FF} = 105 \text{ fF}$ , all at  $L = 25 \mu\text{m}$ , and (b) SFDR at 20 GHz versus  $C_{FF}$ .

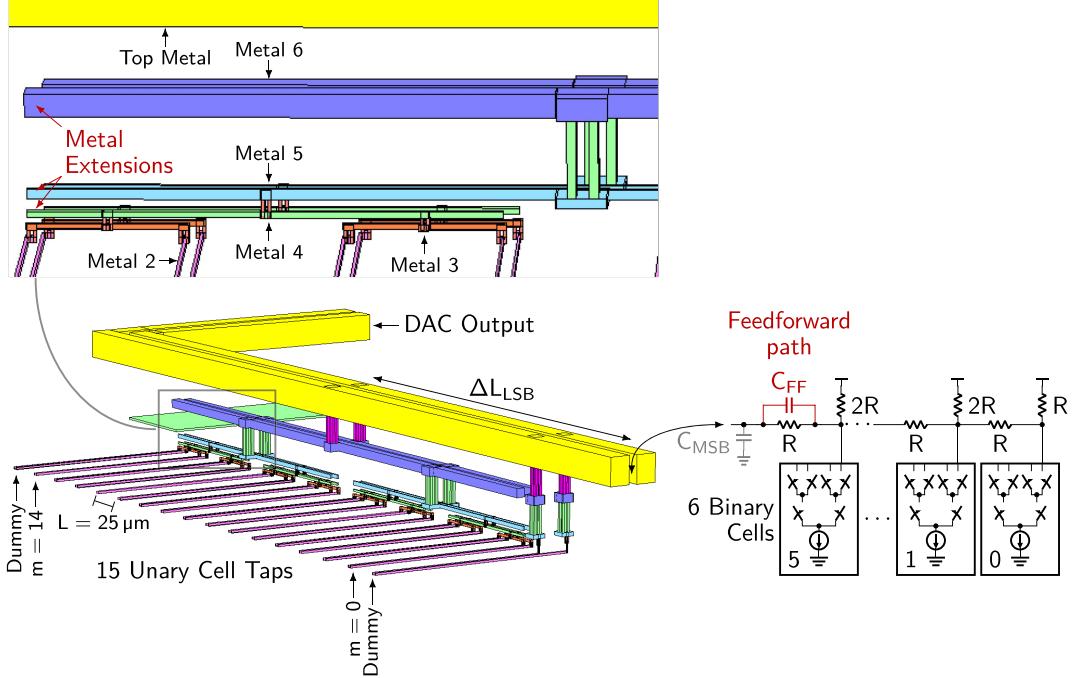


Fig. 8. Illustration of the VST structure and FF path.

a small  $L = 10 \mu\text{m}$ , the SFDR still degrades by 40 dB from the ideal at 20 GHz. Fig. 6(b) plots the SFDR near 20 GHz across  $L$ , showing a trend of  $-21.5 \text{ dB/decade}$ .

It is possible to compensate for the phase variation in the OSN by distributing the clock with an identical TTL structure. The total phase shift of each cell,  $\phi'_m(\omega)$ , then

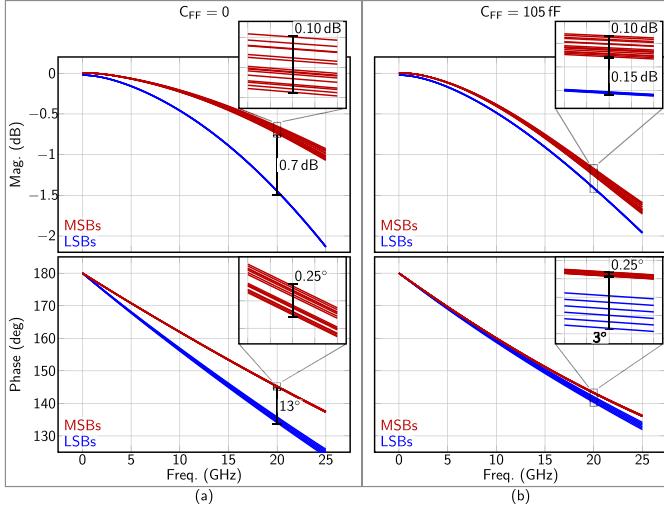


Fig. 9. Frequency response of the VST summing node for  $L = 25 \mu\text{m}$  with (a)  $C_{FF} = 0$  and (b)  $C_{FF} = 105 \text{ fF}$ .

becomes

$$\phi'_m(\omega) = \phi_{c,m}(\omega) + \phi_m(\omega) \quad (3)$$

where  $\phi_{c,m}(\omega)$  is the phase shift in the clock for cell  $m$ . Ideal timing compensation occurs when  $\phi_{c,m}(\omega)$  is designed such that  $\phi'_m(\omega) = \phi_{tc}(\omega)$  for all  $m$ , where  $\phi_{tc}(\omega)$  is a common phase shift among every cell. Fig. 7(a) plots the SFDR performance of the TTL ( $L = 25 \mu\text{m}$ ) with ideal timing compensation, showing a 10-dB improvement at 20 GHz. Despite the ideal compensation of phase variations in the TTL, the amplitude errors remain, limiting the overall SFDR to 50 dB. In practice, dissimilar capacitive loading between the flip-flop clock and cell output prevents ideal compensation, especially approaching mmW, placing the achievable SFDR at 20 GHz between 31 and 41 dB. Note that the simulations for Fig. 7(a) only model the impact of errors induced by the OSN and neglect amplitude and timing errors that occur within the current cells. Therefore, no enhancement to the current cell circuitry or clock distribution will improve the SFDR beyond this limit when the TTL is used, illustrating the critical importance of the OSN on DAC linearity.

#### B. Vertically Stacked Tree and Feed-Forward Path

To minimize frequency response variations among cells, the VST structure, shown in Fig. 8, is proposed. The VST taps the MSB cells on the second metal layer and then forms an H-tree to provide identical path lengths for each cell, thereby minimizing variations in amplitude and phase in a manner similar to commonly used clock trees. Each level of the tree is implemented in the metal directly above the preceding level, minimizing capacitive loading on the DAC output. Additionally, metal extensions at each level equalize capacitive coupling between adjacent levels of the tree. Due to the binary nature of the H-tree, it naturally provides 16 taps, of which 15 are used to connect to the MSB cells. To ensure that the tree is balanced, a dummy cell occupies the 16th tap and an additional dummy tap, connected directly to the top level, is provided at the opposite end. The  $R$ - $2R$  network is tied to the VST with the top metal, forming a transmission line

that connects to the output pads. Fig. 9(a) plots the frequency response of a VST EM model for  $L = 25 \mu\text{m}$ . The VST achieves a significant reduction in variations among MSBs compared with the TTL, resulting in 0.1 dB and 0.25° of amplitude and phase mismatch at 20 GHz. To further highlight the benefit of the VST, Fig. 7(a) shows an 8-dB improvement in SFDR at 20 GHz compared with the TTL with ideal timing compensation.

While the VST ensures tight matching among MSBs, there is a significant mismatch of 0.7 dB and 13° between LSBs and MSBs, as shown in Fig. 9(a). This mismatch is attributed to: 1) a low-pass filter formed between the last  $R$ - $2R$  resistor and the capacitance of the MSB cells and VST ( $C_{MSB}$ ), and 2) loss and delay in the transmission line ( $\Delta L_{LSB}$ ) between LSB and MSB cells, as shown in Fig. 8. To align the frequency responses of MSB and LSB cells, a feed-forward (FF) capacitor ( $C_{FF}$ ), shown in Fig. 8, is added to advance the phase of the LSBs and further attenuate the MSBs. To demonstrate the benefit of  $C_{FF}$ , Fig. 9(b) shows the VST frequency response with  $C_{FF} = 105 \text{ fF}$ . Compared with the standalone VST, the addition of  $C_{FF}$  reduces peak-to-peak amplitude and phase mismatch to 0.25 dB and 3.25° at 20 GHz. This tight matching of the frequency response yields a 13-dB SFDR improvement over the standalone VST, for a total SFDR of 62 dB at 20 GHz, as shown in Fig. 7(a). Compared with the TTL with ideal timing compensation, a 21-dB SFDR improvement is observed at 20 GHz.

Although the FF path improves the high-frequency SFDR, the technique depends upon the absolute value of  $C_{FF}$ . To verify that this approach will remain effective in the presence of process variations, Fig. 7(b) plots the SFDR across  $C_{FF}$ , demonstrating <2-dB reduction from nominal for a  $\pm 12.5\%$  tolerance.

## IV. CIRCUIT IMPLEMENTATION

A schematic of the DAC unit cell and its data path is shown in Fig. 10. The cells utilize HBTs for the switch pairs which, although large, exhibit superior switching speeds and output impedance compared with CMOS counterparts. Fig. 11 plots the output impedance ( $Z_{CELL}$ ) of the current cell, with the data switches on ( $D = 1$ ) and off ( $D = 0$ ). At low frequency,  $Z_{CELL} > 2 \text{ M}\Omega$  is achieved, sufficient for 12-bit static performance [35]. At 20-GHz,  $Z_{CELL}$  is dominated by the 3.2-fF collector capacitance of the RZ switches. The HBTs are biased at a current density of  $1 \text{ mA}/\mu\text{m}$  to provide an  $f_T = 190 \text{ GHz}$ . To improve current matching, a large ( $W/L = 600/5 \mu\text{m}$ ) CMOS current source is implemented with interdigititation and common-centroid layout techniques. The drain of each current source is then cascoded with an HBT to enhance its impedance and isolate the data switches from the current source routing and drain capacitance.

#### A. Local RZ Driver With Timing Control

While the proposed VST structure and FF capacitance minimize the frequency-dependent mismatches in the OSN, mismatches within the RZ switches and clock distribution introduce additional static timing errors. The impact of these

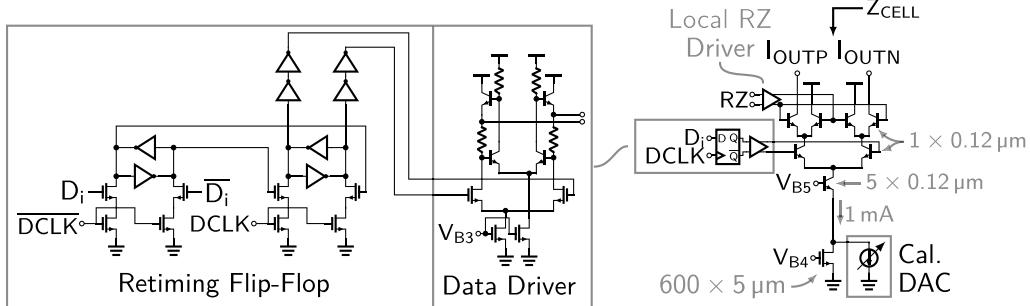


Fig. 10. Schematic of the DAC unit cell and data path.

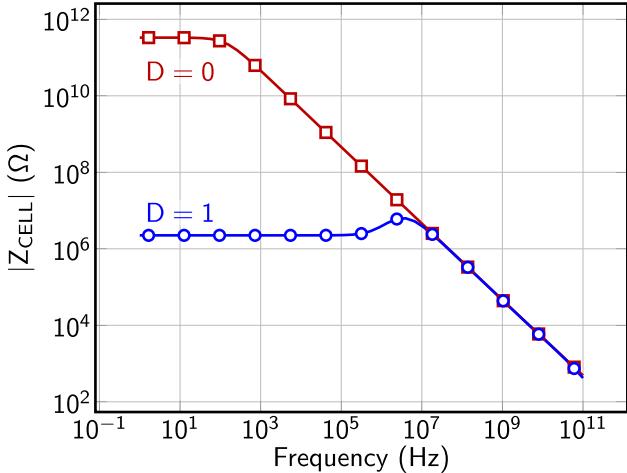
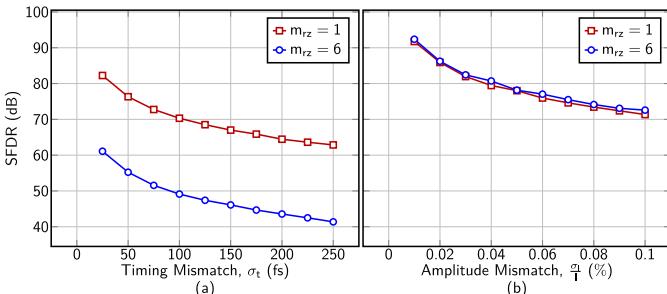
Fig. 11. Simulated output impedance of the DAC unit cell with the data switch off ( $D = 0$ ) and on ( $D = 1$ ).

Fig. 12. Behavioral simulation of the 99.73% SFDR yield (95% confidence level) in the presence of Gaussian-distributed (a) static timing mismatches and (b) static amplitude mismatches.

errors is shown in Fig. 12(a), where Monte Carlo (MC) simulations of a behavioral DAC model are used to plot the 99.73% SFDR yield (95% confidence level) with varying Gaussian-distributed timing mismatch ( $\sigma_t$ ). As expected, the impact of these errors varies with frequency, resulting in a 20 dB reduction from  $m_{rz} = 1$  ( $f_{rz} = 3.35$  GHz) to  $m_{rz} = 6$  ( $f_{rz} = 20.1$  GHz), and requiring  $\sigma_t = 75$  fs to achieve an SFDR > 50 dB. To ensure this performance level, each DAC cell utilizes a local RZ clock driver with programmable delay, which is designed for a maximum delay step of < 225 fs to bound the timing error to  $\pm 1.5\sigma_t$ .

A block diagram of the local RZ driver is shown in Fig. 13(a). The input global RZ clock ( $RZ_G$ ) is buffered and then used to generate in-phase ( $I$ ) and quadrature ( $Q$ ) components via phase shifters formed by  $R_D$  and  $C_D$ . The  $I$  and  $Q$  signals are weighted by  $A_I$  and  $A_Q$ , respectively,

and summed to produce the output. The transfer function for the local RZ driver is given by

$$H_{RZ}(\omega) = \frac{RZ}{RZ_G} = A_I \frac{1}{1 + s R_D C_D} + A_Q \frac{s R_D C_D}{1 + s R_D C_D} \\ = A_I \frac{1 + s R_D C_D \frac{A_Q}{A_I}}{1 + s R_D C_D}. \quad (4)$$

The delay introduced by the driver is obtained from the phase of 4

$$t_d = \frac{\angle H_{RZ}(\omega)}{\omega} = \frac{1}{\omega} \arctan \left[ \frac{\omega R_D C_D (A - 1)}{1 + \omega^2 R_D^2 C_D^2 A} \right] \quad (5)$$

where  $A = (A_Q/A_I)$ . Assuming  $0 \leq A \leq 1$ , the FSR of the timing adjustment ( $FSR_t$ ) is

$$FSR_t = t_d|_{A=1} - t_d|_{A=0} = \frac{1}{\omega} \arctan(\omega R_D C_D). \quad (6)$$

The timing adjustment step size is found by determining the change in delay with respect to  $A$

$$\Delta t(A) = \frac{1}{2^{N_t} - 1} \cdot \frac{\partial t_d}{\partial A} = \frac{1}{2^{N_t} - 1} \cdot \frac{R_D C_D (1 + \omega^2 R_D^2 C_D^2)}{(1 + \omega^2 R_D^2 C_D^2)^2 + \omega^2 R_D^2 C_D^2 (A - 1)^2} \quad (7)$$

where  $N_t$  is the number of timing control bits. Insight into 7 can be obtained by evaluating the precision at the extremes of the control ratio,  $A = 0$  and  $A = 1$

$$\Delta t(0) = \frac{R_D C_D}{2^{N_t} - 1} \quad \Delta t(1) = \frac{1}{2^{N_t} - 1} \cdot \frac{R_D C_D}{1 + \omega^2 R_D^2 C_D^2}. \quad (8)$$

Note that as  $R_D C_D$  becomes large,  $\Delta t(1)$  tends toward zero, rendering the upper portion of the control range ( $A \rightarrow 1$ ) ineffective. As a tradeoff between a wide  $FSR_t$  and this diminishing return on control circuit complexity, letting  $(R_D C_D)^{-1} \approx \omega_{max}$  yields

$$\Delta t(1) = 0.5 \cdot \Delta t(0) \quad FSR_t|_{\omega=\omega_{max}} = \frac{\pi}{4\omega_{max}} \quad (9)$$

where  $\omega_{max}$  is the maximum operating frequency. For additional margin on the maximum RZ clock frequency, the DAC uses  $\omega_{max} = 2\pi \cdot 25$  GHz,  $R_D = 100 \Omega$ , and  $C_D = 64$  fF. Additionally, to minimize the control circuit complexity, the range of weights is reduced to  $A = 0 \dots 0.77$ , resulting in a theoretical  $FSR_t = 4.4$  ps,  $\Delta t(0) = 206$  fs, and  $\Delta t(0.77) = 149$  fs at 20 GHz.

In addition to  $FSR_t$  and the precision of the timing adjustment, the duty cycle of the RZ clock is critical to SFDR.

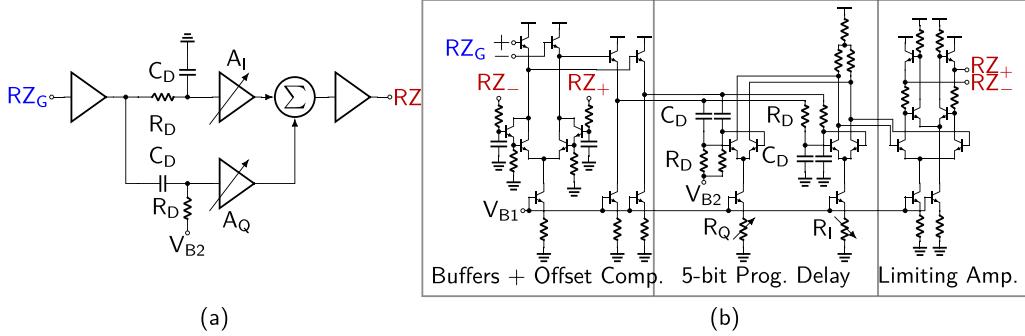


Fig. 13. (a) Block diagram of the local RZ clock driver and (b) transistor-level implementation.

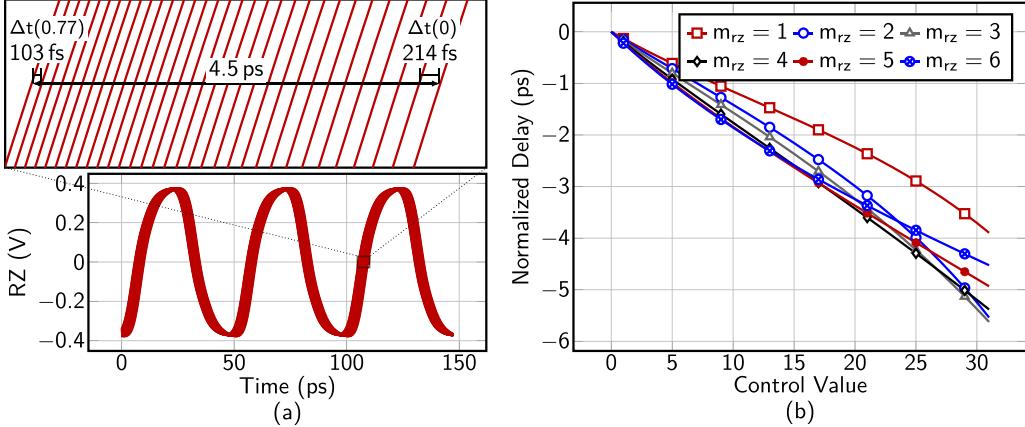


Fig. 14. (a) Transient simulation of the local RZ clock driver circuit for each control value. (b) Normalized delay versus control value for  $m_{RZ} = 1 \dots 6$  ( $f_{RZ} = 3.35 \dots 20.1$  GHz).

As shown in 1, the MRZ  $P_{OUT}$  is proportional to the duty cycle,  $d$ . Hence, duty cycle mismatch manifests as an amplitude mismatch for the cell. To minimize this error, the design targets a 50% duty cycle for the local RZ driver and compensates for additional mismatch due to process variations by calibrating the amplitude within each NZ (Section IV-B).

Fig. 13(b) shows the schematic of the local RZ driver. The input includes two stages of emitter-follower amplifiers, the first biased by an offset compensation circuit to minimize duty cycle mismatch. The following stage implements a 5-bit programmable delay, wherein  $A_I$  and  $A_Q$  are implemented via parallel differential pairs with switched bias resistors,  $R_I$  and  $R_Q$ , respectively. Given the linear relationship between bias current and HBT  $g_m$ ,  $A_I \propto R_I^{-1}$  and  $A_Q \propto R_Q^{-1}$ , resulting in  $A = R_I/R_Q$ . To ensure that the weighted sum maintains a consistent output swing,  $R_I$  and  $R_Q$  are switched in opposite directions such that the sum of bias currents is constant. Finally, the output stage uses a Cherry-Hooper amplifier to ensure sharp edges for the RZ switches of the unit cell.

Fig. 14(a) shows a transient simulation of the local RZ driver at 20 GHz for each control value. The circuit exhibits an  $FSR_t$  of 4.5 ps,  $\Delta t(0)$  of 214 fs, and  $\Delta t(0.77)$  of 103 fs, showing close agreement with theoretical analysis. The maximum delay step of 214 fs meets the target of 225 fs needed to achieve >50-dB SFDR at 20 GHz. Additionally, the edge rate is independent of control value, ensuring that all cells exhibit identical switching speeds. In Fig. 14(b), the delay for each control value and  $m_{RZ}$  setting is shown. Across  $m_{RZ}$ , the  $FSR_t$  ranges from 3.9 to 5.5 ps,

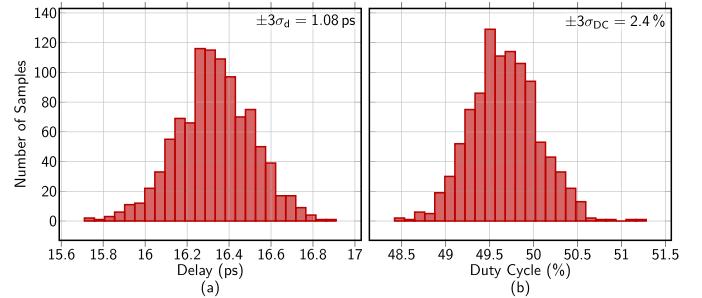


Fig. 15. MC simulation of (a) delay and (b) duty cycle of the local RZ clock driver at the middle control value.

with the lowest  $FSR_t$  corresponding to  $m_{RZ} = 1$ , where less critical.

In addition to calibrating for the static timing mismatch of each DAC cell,  $FSR_t = 4.5$  ps must also account for the delay mismatch in the local RZ driver itself. Fig. 15(a) shows an MC simulation of the driver at the middle control value for  $m_{RZ} = 6$ . The local driver delay varies by  $\pm 3\sigma_d = 1.08$  ps, leaving 3.4 ps of usable control range to calibrate the static timing mismatches within the clock routing, output node, and current cell. Fig. 15(b) shows an MC simulation of the driver duty cycle, exhibiting  $\pm 3\sigma_{dc} = 2.4\%$  variation, corresponding to 0.21 dB of amplitude mismatch, which is subsequently removed using amplitude calibration circuitry.

### B. Amplitude Calibration

In addition to timing constraints, the DAC faces strict demands on amplitude matching among cells. An MC sim-

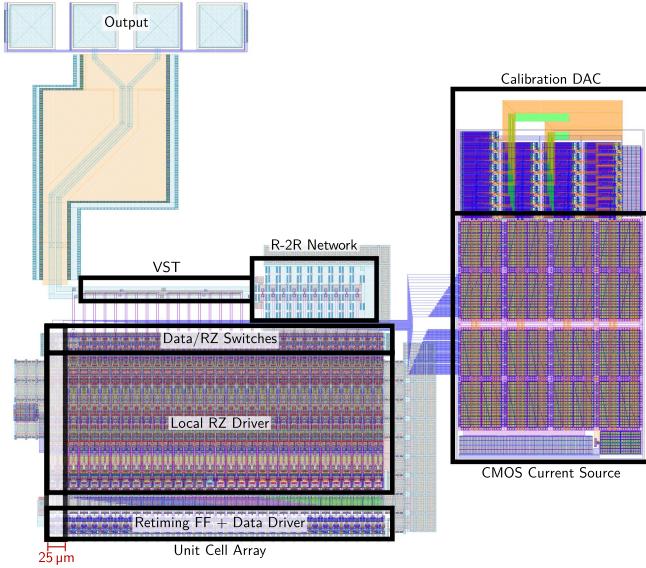


Fig. 16. Layout of the DAC core.

ulation with static current mismatch shows that a variation of  $\sigma_I/I < 0.1\%$  is needed for a 70-dB SFDR, as shown in Fig. 12(b). To achieve this within a reasonable area, the current source is designed for 0.3% mismatch and augmented by a 9-bit calibration DAC (CAL-DAC), shown in Fig. 10. To account for additional mismatches in the  $R$ - $2R$  network, HBT base currents, and RZ duty cycle, the CAL-DAC has an FSR of 10% of the primary cell current.

### C. Data Path

A primary benefit of the MRZ approach is the relaxation of DJ requirements in the data path. As long as the peak-to-peak DJ is less than the width of the RZ pulse, the output will be largely unaffected. The data path, shown in Fig. 10, includes a CMOS RTFF to synchronize the data at each cell. The CMOS implementation yields significant power savings for both the RTFF and clock distribution by avoiding current-mode logic circuits [18]. The RTFF is followed by a data driver, implemented as a Cherry–Hooper limiting amplifier to level-shift the data and ensure full commutation within one RZ pulse.

### D. Layout Considerations

At  $f_{\text{OUT}} = 20$  GHz, the layout of the DAC core, shown in Fig. 16, plays an important role in its performance. The unit cell array comprises 25 active current cells and 7 dummy cells, each with a width of 25  $\mu\text{m}$ . The total of 32 cells enables balanced clock distribution trees, which minimize timing errors. The CMOS current source and CAL-DAC are located outside of the cell array to allow for compact interdigitation with matched routing to each cell, minimizing drain-induced current variations. Decoupling capacitors are distributed throughout each unit cell to minimize the DJ created by cell-dependent supply and bias variations.

## V. MEASUREMENT RESULTS

The 10-bit MRZ DAC is fabricated in a 0.13- $\mu\text{m}$  SiGe process. The chip, pictured in Fig. 17(a), measures 6.25 mm<sup>2</sup>

TABLE I  
POWER CONSUMPTION OF CIRCUIT BLOCKS IN THE DAC

Circuit	Supply (V)	Power (W)
Current Cells	3.5	0.10
Data Drivers	2.0	0.28
RZ Drivers	4.0	1.12
Digital	1.5	0.41
<b>Total</b>		<b>1.91</b>

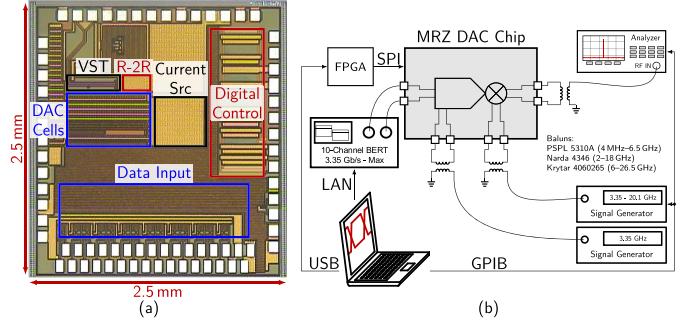


Fig. 17. (a) Photograph of the DAC chip and (b) its measurement setup.

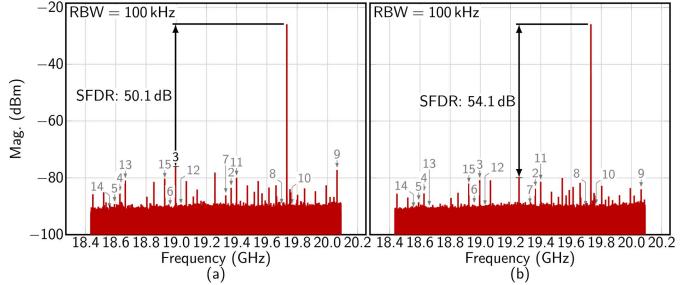


Fig. 18. Measured single-tone spectrum for a signal in the 12th NZ ( $m_{\text{rz}} = 6$ ) (a) before and (b) after calibration. Spurs from the first 15 harmonics are labeled. Losses from the measurement setup are included.

and integrates ten low-voltage differential signaling channels, the MRZ DAC with VST and FF path, and an SPI for the calibration control. Table I summarizes the power consumption of the major DAC circuit blocks with a total of 1.91 W. The 20-GHz RZ drivers utilize nearly 60% of the total power due to the elevated power supply and bias current required for high-frequency performance.

During testing, the DAC is mounted on a probe station and connected via a probe card to the test equipment. The test setup, shown in Fig. 17(b), utilizes an Agilent 81250 ParBERT to feed 10-bit data to the DAC. Although the chip was designed for 4 GS/s, the ParBERT capability limits testing to 3.35 GS/s. The data and RZ clocks are generated and manually aligned by two Agilent E8267D signal generators. Three baluns perform differential to single-ended conversion for the DAC clocks and output. To cover dc-20-GHz, three balun variants are required [see Fig. 17(b)].

The DAC calibration is performed externally using an Agilent N9030A PXA spectrum analyzer as the measurement device, and is automated via Python scripts with GPIB and LAN control of the test equipment. The amplitude and timing of each DAC cell are adjusted by programming the CAL-DAC and local RZ driver controls. Amplitude calibration measurements are obtained by applying a square wave to one

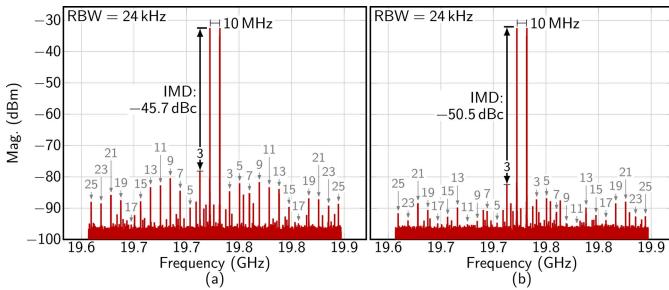


Fig. 19. Measured two-tone spectrum for a signal in the 12th NZ ( $m_{rz} = 6$ ) (a) before and (b) after calibration. The first 25 intermodulation products are labeled. Losses from the measurement setup are included.

bit at a time, measuring the amplitude of its fundamental component, and tuning the CAL-DAC for each bit. The effectiveness of this measurement is limited by the 0.1-dB power spectral density resolution of the spectrum analyzer, yielding a maximum achievable SFDR of  $\sim 55$  dB in practice. Timing errors are calibrated by first generating a single-tone spectrum in the desired NZ. Next, a single cell is calibrated by performing a coarse and fine search through its delay control and recording the delay that gives the highest SFDR. These steps are repeated for each cell in the DAC to obtain the optimal SFDR for the DAC. For each  $m_{rz}$  setting, the DAC is calibrated in both NZs adjacent to  $m_{rz} f_s$  to properly account for the remaining frequency-dependent amplitude and timing variations in the OSN, as well as duty cycle errors in the local RZ drivers.

Fig. 18(a) shows the DAC output prior to calibration/de-embedding for a single-tone spectrum in the 12th NZ ( $m_{rz} = 6$  and  $f_{rz} = 20.1$  GHz). The DAC exhibits an SFDR of 50.1 dB and is dominated by the images of the third and ninth harmonics. Applying amplitude and timing calibration yields a reduction in all odd-order spurs, resulting in a 4-dB SFDR improvement, as shown in Fig. 18(b). Note that the dominant post-calibration tone is not harmonically related to the desired signal and is likely due to the mixing of an internal DAC node with the RZ clock.

Fig. 19(a) shows the two-tone response of the uncalibrated DAC with a 10-MHz spacing in the 12th NZ. The DAC exhibits an intermodulation distortion (IMD) of  $-45.7$  dBc, dominated by the third-order product. After amplitude and timing calibration, the two-tone spectrum, shown in Fig. 19(b), exhibits a significant reduction in all intermodulation products, improving the IMD by 4.8 dB to  $-50.5$  dBc.

To characterize the performance of the DAC across the entire frequency range, an input from dc to  $0.4 f_s$  is provided, while the RZ clock is swept from  $m_{rz} = 1 \dots 6$ , generating signals from the 1st to the 13th NZ. Fig. 20 shows both the simulated and measured  $P_{OUT}$ . The simulation uses an  $RC$  extraction of the full DAC array, including power, ground, and clock nets, as well as the output pads. Although an EM model of the VST OSN would further improve simulation accuracy, it was excluded due to prohibitively long simulation time. To accurately characterize  $P_{OUT}$ , losses in the cables, connectors, and baluns are de-embedded. However, some parts of the measurement setup could not be completely de-embedded, such as the custom-built probe card, and spectrum analyzer frequency response [36]. The measured  $P_{OUT}$  exhibits a variation

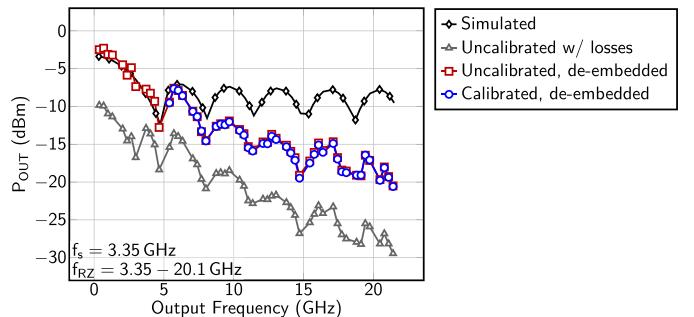


Fig. 20. Simulated and measured output power for signals swept through the first 13 NZs ( $m_{rz} = 1 \dots 6$ ). Simulation includes an  $RC$  extracted model of the full DAC cell array and output node.

of  $\sim 4$  dB within each NZ with a peak dc power of  $-3$  dBm, closely matching simulations. At 20 GHz,  $P_{OUT}$  falls  $\sim 8$  dB below simulation to  $-18$  dBm. This discrepancy is attributed to: 1) remaining test setup losses and 2) neglected inductance in the  $RC$  model. Following amplitude and timing calibration, no change in  $P_{OUT}$  is observed, as shown in Fig. 20.

Fig. 21(a) and (b) shows the simulated and measured SFDR, respectively. The simulated SFDR ranges from 72 dB at dc to 47 dB at 20 GHz. Prior to calibration, the measurements show a maximum SFDR of 63 dB at low frequency. This discrepancy is due to the absence of device mismatch in the simulation. At 5 GHz and above, the uncalibrated DAC exhibits  $>45$ -dB SFDR and matches within 5 dB of simulation. It is worth noting that the VST and FF path allow the uncalibrated DAC to achieve 4 dB better SFDR at 20 GHz than an ideal DAC with TTL and ideal timing compensation [see Fig. 7(a)]. After calibration, an SFDR improvement of up to 7 dB is observed, yielding  $>48$ -dB SFDR from dc to 20 GHz. In addition to random process mismatches, the calibration also compensates for the deterministic amplitude and timing mismatches induced by the  $R-2R$  network (discussed in Section II), resulting in higher SFDR from 103 to 20 GHz than in simulation. Note that due to the aforementioned limitations in the external amplitude measurement, calibration was only performed above 5 GHz, where the uncalibrated results fall below 55-dB SFDR. Fig. 22 shows the measured IMD across  $f_{OUT}$ . Prior to calibration, a worst case IMD of  $-42$  dBc is observed. Calibration provides up to 6-dBc improvement in IMD, yielding a worst case of  $-46$  dBc from dc to 20 GHz.

Fig. 23 and Table II show a comparison of recently reported GHz and mmW DACs. Three of the DACs achieve SFDR  $>50$  dB across the NZ, however, their  $f_{OUT}$  is limited to  $<6$  GHz [14], [16], [22]. In [24], the SFDR drops to 42 dB at 10 GHz. The implemented DAC achieves  $>48$ -dB SFDR up to 20 GHz, where other DACs are limited to 31 dB [9], [17]. Furthermore, the highest sample rate, and thus, the largest synthesizable bandwidth, is achieved among RF DACs [22], [24].

## VI. CONCLUSION

A 10-bit MRZ DAC, utilizing a VST OSN structure and capacitive FF network to minimize amplitude and phase mismatch, is presented. The proposed OSN enables the use of SiGe HBTs in the unit cell, despite their large footprint,

TABLE II  
PERFORMANCE COMPARISON WITH RECENTLY PUBLISHED DACS

	This	[9]	[17]	[24]	[10]	[13]	[14]	[16]	[22]*
Tech. [nm]	130	65	28	500	28	1000	130	28	65
BiCMOS	CMOS	CMOS	CMOS	InP	CMOS	InP	BiCMOS	CMOS	CMOS
Resolution [bits]	10	6	8	12	8	6	12	9	16
Pwr [W]	1.91	0.75	2.5	1.6	0.144	0.95	8.3	0.11	0.38
$P_{out}$ [dBm]	-18	-3.5	-5	-15	-0.97	-10	1	-6.5	-8
$f_s$ [GS/s]	3.35	56	100	2.7	18	28	12	11	1.75
$f_{out}$ [GHz]	20.0	26.9	25	9.45	8	6.7	6	5.5	5.26
Min. SFDR [dB]	48	31	27	42	36	36	55	50	50
IMD [dBc]@[GHz]	48@20	—	—	—	—	—	—	51@5.5	58@5

\* Reported results using the full Nyquist zone without the dither band

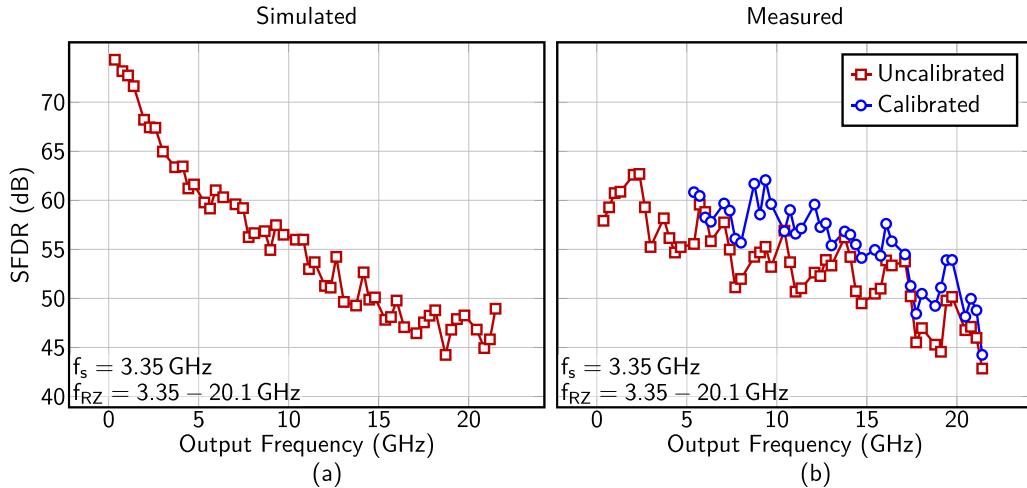


Fig. 21. (a) Simulated and (b) measured SFDR for signals swept through the first 13 NZs ( $m_{rz} = 1 \dots 6$ ). Simulation includes an RC extracted model of the full DAC cell array and output node.

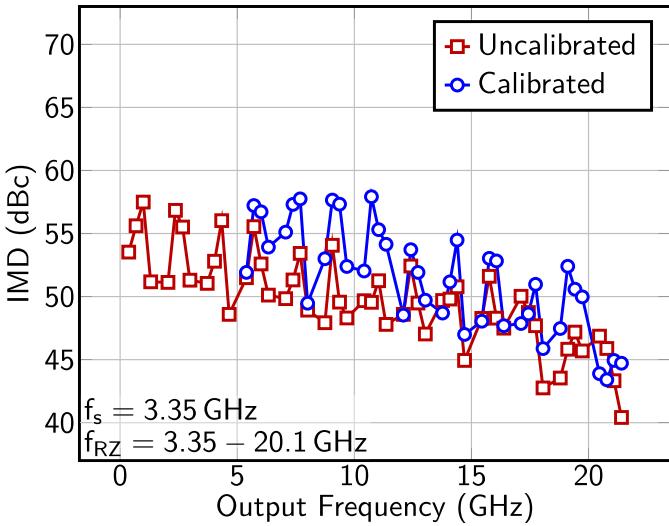


Fig. 22. Measured IMD for signals swept through the first 13 NZs ( $m_{rz} = 1 \dots 6$ ).

yielding a 21-dB SFDR improvement over the conventional TTL structure. Additionally, the DAC utilizes per-cell amplitude and timing calibration to correct additional errors induced by process variation. Implemented in a  $0.13\text{-}\mu\text{m}$  SiGe technology, the DAC achieves  $>48$ -dB SFDR and lesser than  $-46$  dBc IMD from dc to 20 GHz after calibration

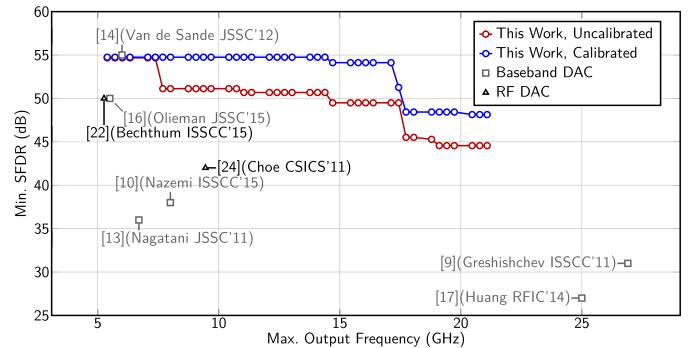


Fig. 23. SFDR comparison with recently published DACs. Each point corresponds to the reported worst case SFDR from dc to the maximum output frequency.

at 3.35 GS/s. Compared with the recently reported DACs, the highest SFDR performance above 6 GHz is achieved while supporting the largest instantaneous bandwidth among RF DACs.

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