

A 28-GHz Phased-Array Receiver Front End With Dual-Vector Distributed Beamforming

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Abstract—This paper presents a 28-GHz four-channel phased-array receiver in 130-nm SiGe BiCMOS technology for fifth-generation cellular application. The phased-array receiver employs scalar-only weighting functions within each receive path and then global quadrature power combining to realize beamforming. We discuss both the theory and nonidealities of this architecture and then circuit design details for our phased-array front-end prototype. Differential low-noise amplifiers and dual-vector variable-gain amplifiers are used to realize each front end in a compact area of 0.3 mm². Across 4-b phase settings, each array element achieves 5.1–7 dB noise figure, −16.8 to −13.8 dBm input-referred 1-dB compression point, and −10.5 to −8.9 dBm input-referred third-order intercept point. The average gain per element is 10.5 dB at 29.7 GHz, whereas the 3-dB bandwidth is 24.5% (26.5–33.9 GHz). Root-mean-squared gain and phase errors are less than 0.6 dB and 5.4° across 28–32 GHz, respectively, and all four elements provide well-matched and well-isolated responses. Power consumption is 136 mW per element, equaling 546 mW for the four-element array.

Index Terms—28 GHz, basestation, beamforming, beamsteering, dual-vector, fifth-generation (5G), integrated circuits, millimeter-wave, phase shifter, phased array, receiver, SiGe BiCMOS, Wilkinson power combiner.

I. INTRODUCTION

FUTURE cellular systems will support higher capacity along with faster peak- and edge-data rates. This need has the potential to be partially met by shifting toward millimeter-wave frequencies [1], [2]. In particular, the 28-GHz frequency band is an attractive candidate for fifth-generation (5G) networks due to available spectrum, favorable channel characteristics [3], [4], and the ability to realize highly integrated high-performance hardware in silicon [5]–[8]. Link budgets for 28 GHz [1] suggest moderate beamforming for user equipment (one to eight elements) and stronger beamforming at the basestation (up to hundreds of elements).

For 5G basestations, multiple beams will be required to service multiple users concurrently. While this could be supported by pure digital beamforming in a massive multi-input multioutput (MIMO) system, the power consumption and back-end digital processing associated with hundreds

Manuscript received August 16, 2016; revised October 25, 2016; accepted November 21, 2016. Date of publication December 26, 2016; date of current version April 20, 2017. This paper was approved by Guest Editor Danilo Manstretta.

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Digital Object Identifier 10.1109/JSSC.2016.2635664

of data converters each supporting up to a gigahertz of bandwidth is prohibitive [9]. As such it is anticipated that systems will use a hybrid approach composed of multiple subarrays employing analog beamforming, which are then connected to radio frequency (RF) transceiver chains which can then be controlled digitally [10]. For this hybrid architecture, the subarrays will feature larger beamwidths and will therefore be subject to multiple signals within the same beam, meaning spatial filtering alone cannot be relied upon to suppress interferers. As a result, high dynamic range is required for the full RF transceiver chain, including the phased-array front end. Additionally, low-area and scalable phased-array architectures are desirable to allow multiple subarrays to be implemented together in a cost-effective manner.

In this paper, we expand upon our earlier publication [11] and present a 28-GHz four-element receive beamformer which employs scalar-only weighting functions within each front-end and global quadrature combining to realize a beamforming concept we refer to as “dual-vector distributed beamforming.” Such scalar front ends can be both area-efficient and wide bandwidth, and could be useful for 28-GHz 5G basestations. We demonstrate our concept with the realization of a four-element phased-array receive beamformer in SiGe BiCMOS operating at 28 GHz.

II. SYSTEM ARCHITECTURE

For the 5G basestation application, we choose an RF phase shifting and combining architecture to achieve both a small chip area and high dynamic range. RF phase shifters can be realized using a number of topologies. A passive approach composed of cascaded switched high-pass/low-pass inductor–capacitor (LC) networks [12], [13] can achieve high linearity and accurate discrete phase shifts; however, the cascading of multiple stages can result in a large area, leading to very large chip sizes for arrays which require many elements. Furthermore, the passive phase shifter can exhibit a loss which depends on phase setting, necessitating variable-gain compensation [14], [15]. Another passive phase shifter is the reflective-type phase shifter (RTPS) employing varactor-based tunable reflectors [16]. The RTPS can achieve a large phase shift range in a compact structure; however, the changing quality-factor of the varactor versus its capacitance can introduce phase-dependent loss if the reflective load is not properly matched, once again necessitating variable-gain compensation [17]. When gain compensation is introduced to either of the above-mentioned topologies, the original passive bidirectional circuit becomes active and unidirectional.

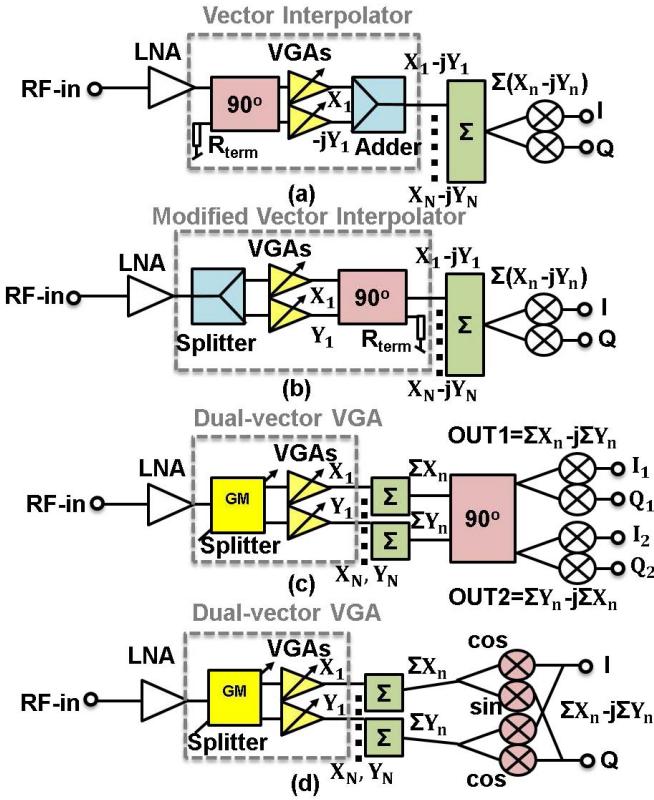


Fig. 1. Architectures for N -element phased array. (a) Traditional vector interpolation, (b) modified vector interpolation with quadrature splitter and power combiner locations swapped, (c) proposed dual-vector distributed beamformer, and (d) dual-vector distributed beamformer employing mixer-based quadrature combining. Note that X_n and Y_n refer to signals within the n th element, amplitude weighted according to (1).

An alternative active phase shifter is the vector interpolator which creates phase shift and variable gain using weighted in-phase (I) and quadrature-phase (Q) vectors [18], as shown in Fig. 1(a). Similar to the gain-compensated RTPS, the interpolator requires both a quadrature generator and variable-gain amplifier (VGA), and therefore, as shown in [19], the noise figure (NF) and the output-referred linearity are similar for both topologies. The avoidance of varactors, though, results in an arguably simpler structure. Interpolators have drawbacks, however. First, the need for quadrature generation within each phase shifter imposes an area penalty. For example, in [8], the 28-GHz quadrature hybrid occupied one-third of the total front-end area. A second limitation is crosstalk between the I and Q signal vectors, where the variable gain of one component (I or Q) can depend on the value of the other component (Q or I). This results in phase and amplitude variation across settings, complicating the control scheme. This issue worsens at higher frequencies due to the reduced output impedance of the transconductors used to form the VGA.

These limitations can be addressed by altering the architecture of the vector-interpolating front end, as shown in Fig. 1(b) and (c). Key functions are color-coded to highlight their new location within the system. First, the position of the input quadrature splitter and output combiner is swapped, allowing the outputs of the interpolator to be isolated from

each other and reducing crosstalk. A drawback of placing the quadrature combiner last, though, is a 3-dB drop in gain, as only half the signal power is provided to the desired output. This gain reduction impacts NF. Therefore, second, the quadrature combiner is moved out of each individual element to a single global location. After power combining, the signal-to-noise ratio has been increased by the number of elements in the array; hence, a gain reduction here has less impact on NF. Furthermore, use of a global quadrature combiner saves area within the array. One consequence of global interpolation is that now dual power-combiner structures are needed, incurring an area penalty which depends upon the combiner topology. Finally, as will be shown, the use of a global interpolator allows two simultaneous beams to be supported at the beamformer output, one directed at a given angle and another reflected across broadside which we refer to as the “image” pattern.

We refer to this architecture as *dual-vector distributed beamforming*. Dual vector refers to the fact that two signals are generated within each front end. Distributed refers to the fact that the overall beamforming operation is subdivided between scaling functions within each front end and a global interpolation function located after the power combiners. A similar approach was proposed in [20], where the quadrature function was instead realized through a pair of quadrature downconversion mixers [shown in Fig. 1(d)]. A benefit of the mixer-based approach is that direct-conversion receivers already must generate accurate quadrature local-oscillator signals, and these can be leveraged to provide the quadrature solution for beamforming. A drawback is that the mixers are exposed to spatial signals located either within the desired beam location or the image location. In contrast, when a quadrature hybrid is used, two concurrent beams are provided and the undesired lobe is eliminated prior to downconversion.

We now review the beamforming operation to show both dual-beam support and the aforementioned image pattern. The array factor, $F(\theta)$, as a function of angle-of-arrival θ (zero corresponds to broadside) for an N -element linear array is [21]

$$\begin{aligned} F(\theta) &= \sum_{n=0}^{N-1} e^{jnkd \sin(\theta)} a_n e^{-j\alpha_n} \\ &= \sum_{n=0}^{N-1} \left(\underbrace{a_n e^{jnkd \sin(\theta)} \cos(\alpha_n)}_{X_n} - j \underbrace{a_n e^{jnkd \sin(\theta)} \sin(\alpha_n)}_{Y_n} \right) \end{aligned} \quad (1)$$

where κ equals $2\pi/\lambda$, d is the antenna spacing, a_n is the amplitude shift per element, and α_n is the phase shift per element. Phasors X_n and Y_n are the Cartesian expansions of the amplitude shift and phase shift for the n th element, depicting vector interpolation.

For dual-vector distributed beamforming, we apply the summation to all X and Y signals and then pass these summations through a global 90° hybrid coupler [Fig. 1(c)]. For the first coupler output, $\sum Y$ undergoes a -90° phase shift, yielding

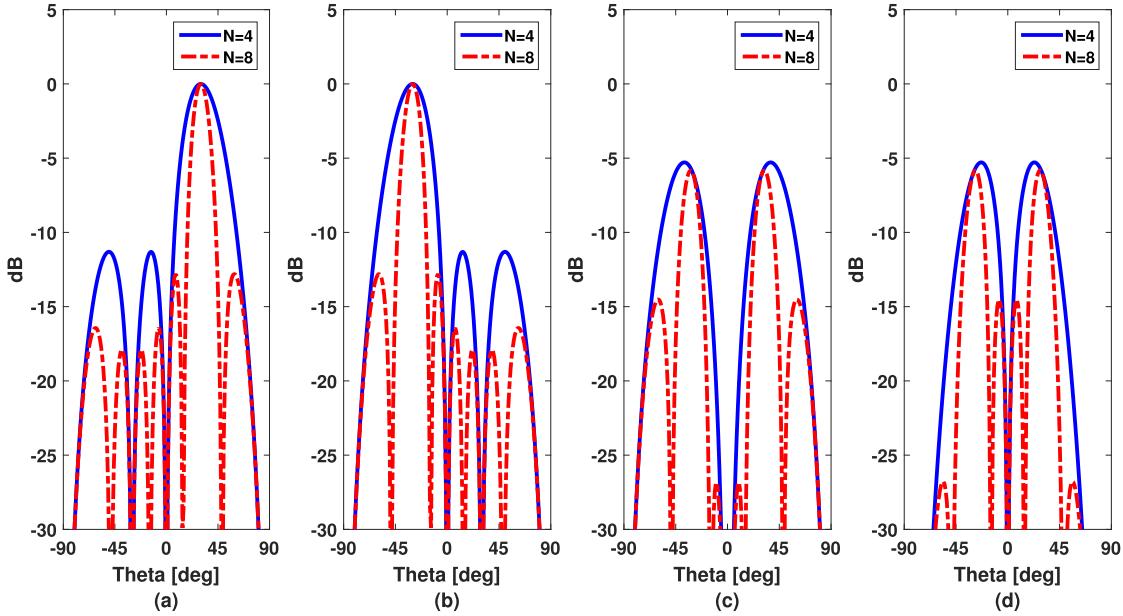


Fig. 2. Calculated (a) F_1 , (b) F_2 , (c) $\sum X$, and (d) $\sum Y$, when beam one is steered to 30° for $\lambda/2$ -spaced linear array with $N = 4$ and $N = 8$. All patterns normalized by N .

a first array factor

$$F_1(\theta) = \frac{\sqrt{2}}{2} \left(\sum X_n - j \sum Y_n \right) \quad (2)$$

where summation bounds have been dropped and where the $\sqrt{2}/2$ accounts for the power split in the quadrature combiner. This response is equivalent to that in (1) with the addition of a scaling factor. To steer the main beam to angle θ_0 , the phase shifters are set to $\alpha_n = nkd \sin(\theta_0)$, leading to a peak directivity of N at angle θ_0 [21]. For the second coupler output, $\sum X$ undergoes a -90° phase shift, yielding a second, “image” array factor

$$\begin{aligned} F_2(\theta) &= \frac{\sqrt{2}}{2} \left(\sum Y_n - j \sum X_n \right) \\ &= \frac{-j\sqrt{2}}{2} \left(\sum X_n + j \sum Y_n \right). \end{aligned} \quad (3)$$

This image pattern is the conjugate of the F_1 pattern multiplied by a global -90° phase shift. As such, for the same phase shifter settings described earlier, output two exhibits a peak directivity of N at angle $-\theta_0$, i.e., reflected across broadside. As can be seen, this architecture can simultaneously support two conjugate beams. This can provide additional capabilities for an MIMO system employing hybrid analog/digital precoding [10], wherein the dual-vector distributed beamformers serve as dual-beam subarrays for the system. Multiple dual-output subarray responses can be combined to synthesize desired patterns. Additionally, a fast, switched-beam capability can be provided, wherein the receiver can quickly switch between two available patterns.

Fig. 2(a) and (b) shows example normalized patterns from MATLAB for F_1 and F_2 , respectively, for four and eight-element linear arrays ($\lambda/2$ spacing) controlled such that beam one steers to $+30^\circ$. Fig. 2(c) and (d) shows example patterns for $\sum X$ and $\sum Y$, respectively, for these same scenarios,

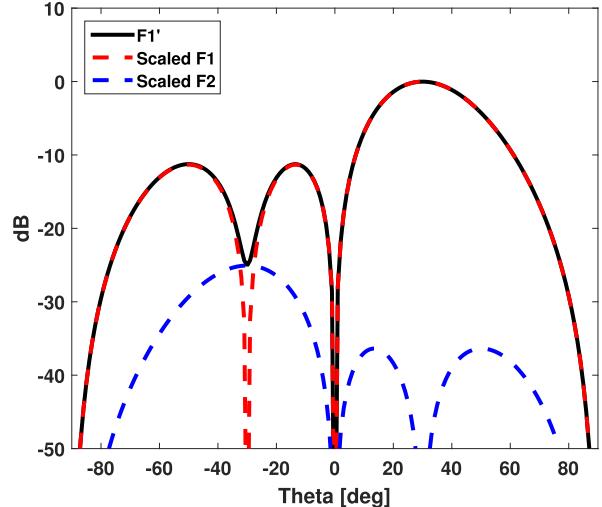


Fig. 3. Skewed F_1 pattern (F'_1) with phase skew of 6.4° for four-element array steered to 30° . Scaled versions of the ideal F_1 and F_2 patterns according to (5) included to show the components of the skewed pattern.

indicating that both exhibit peaks at both desired and conjugate angles.¹

With this foundation, we can now discuss nonidealities for this system. First, both individual X and Y signals must ideally be in-phase or 180° out of phase to realize four-quadrant phase shifting. Any *local* phase deviation incurred as the gain is varied constitutes an effective quadrature error for that individual element, leading to phase and gain errors. Second, the

¹The reasoning follows. Since X and Y involve cosine- and sine-weighted signals, Euler’s equation tells us these can be decomposed into phasors directed at both $+\alpha$ and $-\alpha$; hence, two beams are present. Alternatively, one can simply solve (2) and (3) for $\sum X$ and $\sum Y$, which will be functions of both F_1 and F_2 ; hence, $\sum X$ and $\sum Y$ have peaks at both θ_0 and $-\theta_0$.

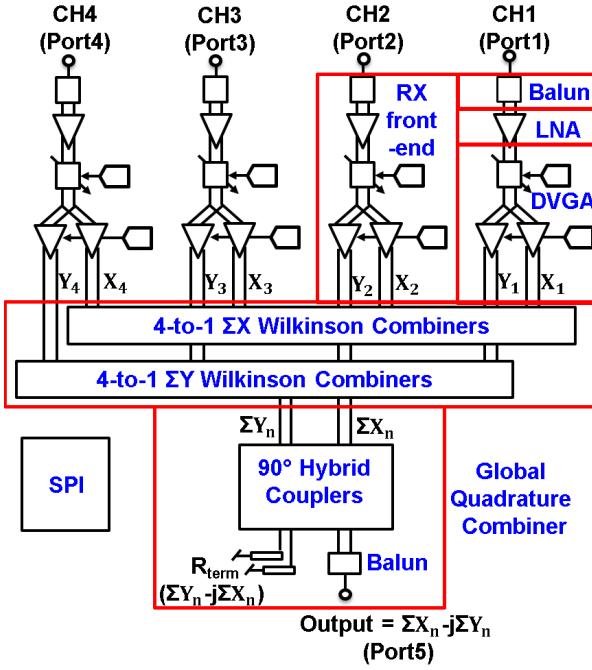


Fig. 4. Block diagram of realized four-element phased-array front end employing dual-vector distributed beamforming.

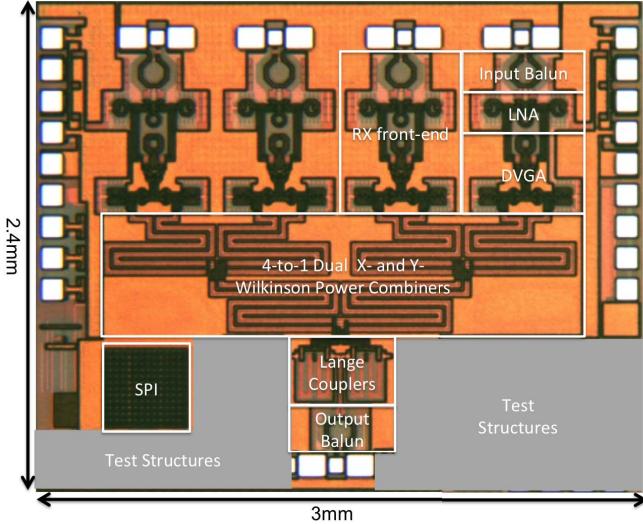


Fig. 5. Die micrograph of phased-array receiver. Die size is $3 \times 2.4 \text{ mm}^2$.

$\sum X$ and $\sum Y$ signals must also not experience any *global* phase error; hence, the power combiners for each must be phase coherent. Any global phase skew, δ , would result in imperfect cancellation of the undesired pattern. Introducing this skew arbitrarily to the $\sum Y$ component in (2), we find

$$\begin{aligned} F'_1(\theta) &= \frac{\sqrt{2}}{2} \left(\sum X_n - j e^{j\delta} \sum Y_n \right) \\ &= F_1(\theta) \frac{(1 + e^{j\delta})}{2} + F_2(\theta) \frac{(1 - e^{j\delta})}{2} \end{aligned} \quad (4)$$

where F'_1 represents the skewed array factor for output one and F_1 and F_2 represent the ideal array factors

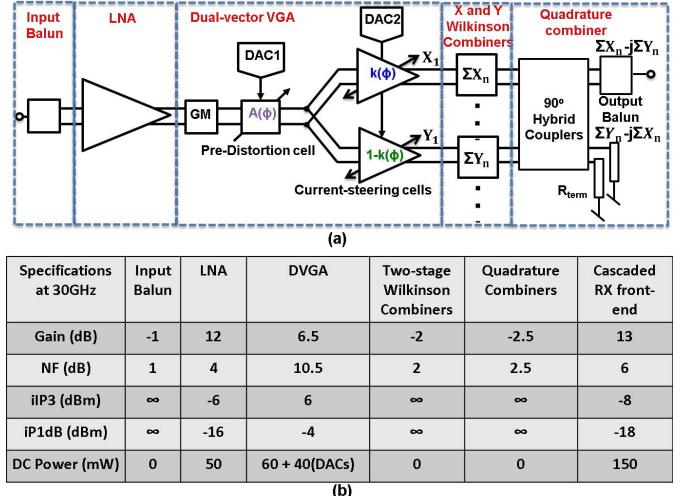


Fig. 6. (a) Detailed block diagram of receiver front end. (b) Performance specifications.

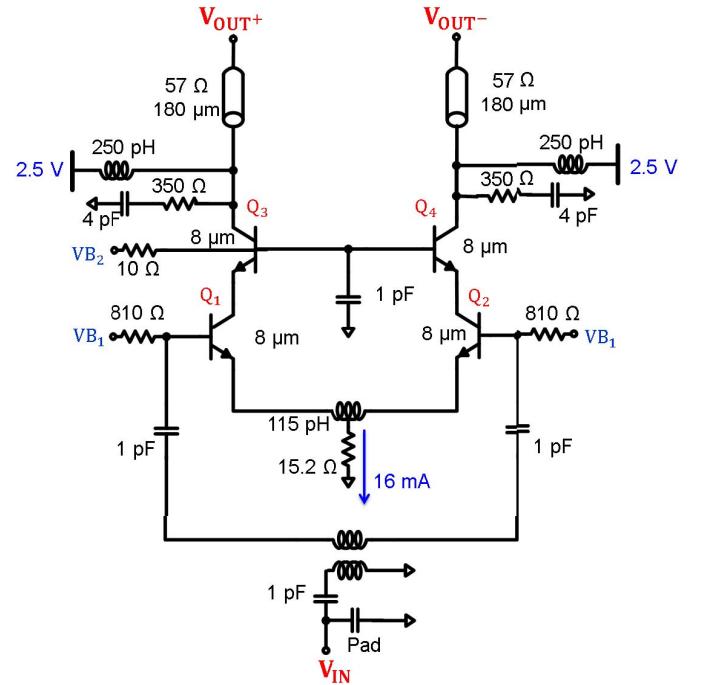


Fig. 7. Simplified schematic of LNA.

without skew. Using this expression, we can solve for a value of δ that results in a contribution from the undesired pattern which is R dB below the main desired beam. Note that this contribution can add together with an existing sidelobe at that position, degrading the overall sidelobe performance. Taking the ratio of desired to undesired beam magnitudes and solving for δ , it can be shown that

$$\delta = \cos^{-1} \left(\frac{1 - 10^{-R/10}}{1 + 10^{-R/10}} \right). \quad (5)$$

To keep the undesired pattern 25 dB below desired, the global skew between $\sum X$ and $\sum Y$ must be below 6.4° . Fig. 3 shows

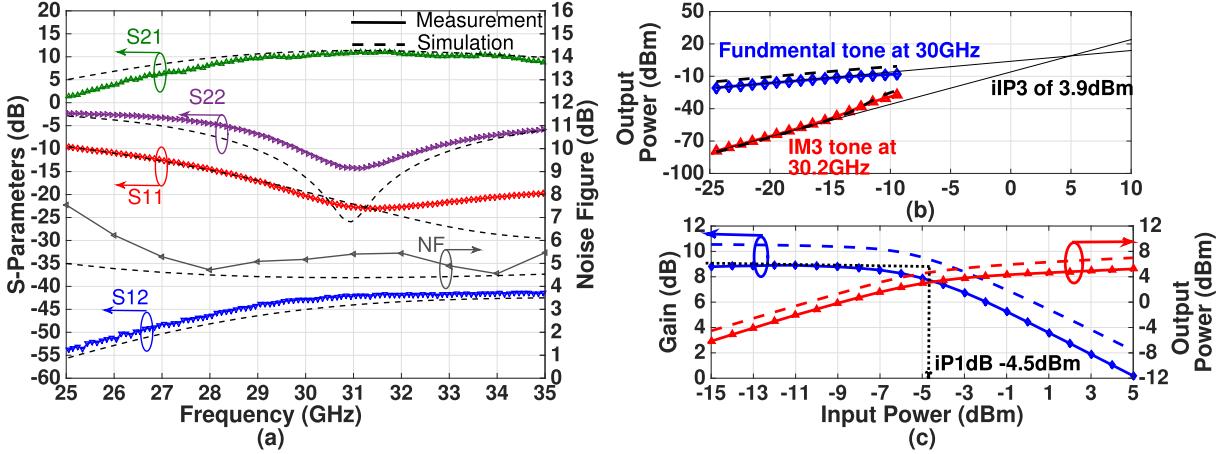


Fig. 8. Measured and simulated LNA results. (a) S-parameters and NF. (b) iIP₃ at 30 GHz. (c) iP₁ dB at 30 GHz.

the pattern for F'_1 and the scaled versions of F_1 and F_2 according to (5) with a 6.4° skew for a four-element array steered to 30°. For this simulation, each element's performance is assumed ideal. Neither quantization error nor statistical variations within each element is included, since both will impact F_1 and F_2 patterns in the same way. Fig. 3 shows how the F'_1 pattern is composed of the addition of scaled versions of F_1 and F_2 . A skew less than 6.4° is achievable in dual power-combiner designs.

III. RECEIVER ARRAY

Our four-element receiver array has been implemented in 130-nm SiGe BiCMOS 8HP technology from Global-Foundries. The array block diagram is shown in Fig. 4. Four front ends are combined using a dual-differential Wilkinson power combiner structure. The ΣX and ΣY outputs are then combined using a differential hybrid coupler. To simplify testing, we have only included the ability to measure output one from the coupler, where output two is terminated on chip. Simulations verify that outputs one and two perform as predicted in (2) and (3). Indeed, the F_2 response can be obtained from output one by swapping our definitions, and thereby weighting factors, applied to X and Y. A chip micrograph is shown in Fig. 5. The die size is 7.2 mm² including pads and the array area is 3.7 mm² excluding pads. A single element (excluding input balun) occupies 0.3 mm². The chip consumes 97.5 mW for each front end and another 40 mW per element for digital-to-analog converters (DACs) which were not power optimized. The total power dissipation is 546 mW.

A more detailed block diagram of the RF front end is shown in Fig. 6(a). Each front end requires a low-noise amplifier (LNA) and a dual-vector VGA (DVGA). A fully differential architecture was selected to reduce the impact of finite supply plane impedance on circuit performance and stability, at the cost of nearly a doubling of the front-end power consumption for the same transistor current density. Fig. 6(b) summarizes the performance targets for each element in the front end to achieve a high dynamic range for the projected

5G basestation application. The following sub-sections III-A-D describe design details for each element in the system.

A. Low-Noise Amplifier

The fully differential LNA is designed for moderate linearity and low noise, and the schematic is shown in Fig. 7. A spiral transformer is used for an input balun and has a measured insertion loss of 0.8 dB. This balun would likely be eliminated in a final system packaged with differential antennas, although the loss is not deembedded from our measurement results. A cascode topology is used in the LNA to achieve high gain and high reverse isolation. Finally, the output LC matching network is designed to directly drive the DVGA input impedance of 54-j108 Ω at 28 GHz and includes a shunt resistor to broaden the bandwidth.

A stand-alone breakout of the LNA has been realized, where the LNA output match is modified to 50 Ω to facilitate measurement. Fig. 8(a) shows both the simulated and measured scattering parameters and NF versus frequency. Model-to-hardware correlation is good, with a slight deviation in S_{22} coming from the bondpad model. The LNA breakout achieves 10-dB gain, 5-dB NF, and better than 10-dB input return loss at 28 GHz. The 5-dB NF translates to a 4.2-dB NF for the LNA without the balun. Linearity results are shown in Fig. 8(b) and (c), indicating greater than -5-dBm input-referred 1-dB compression point (iP₁ dB) and +3.9-dBm input-referred third-order intercept point (iIP₃). The differential LNA draws 18.5 mA from a 2.5 V supply (46.3 mW).

B. Dual-Vector VGA

Two variable-gain functions are needed for interpolation. These are realized with a single-input, dual-output structure to save both space and power—the DVGA, the schematic of which is shown in Fig. 9. The DVGA structure was originally proposed in [22], but is modified here to work with a single input. The circuit should provide one differential output (X) which is weighted according to a $\cos(\alpha)$ function and another differential output (Y) which is weighted according to a $\sin(\alpha)$ function. This is realized within the circuit through a cascade

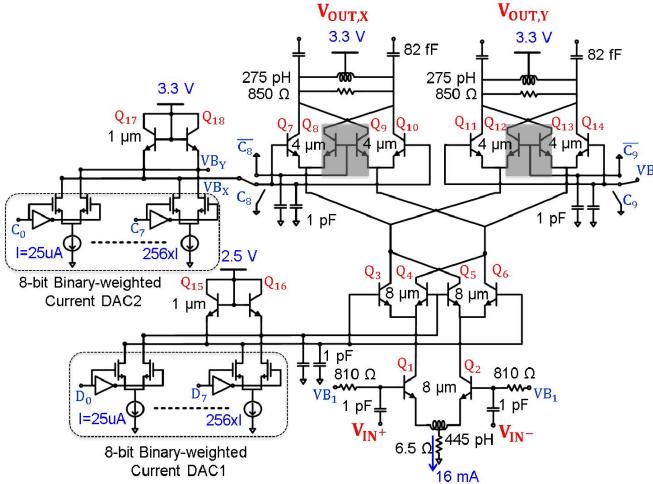
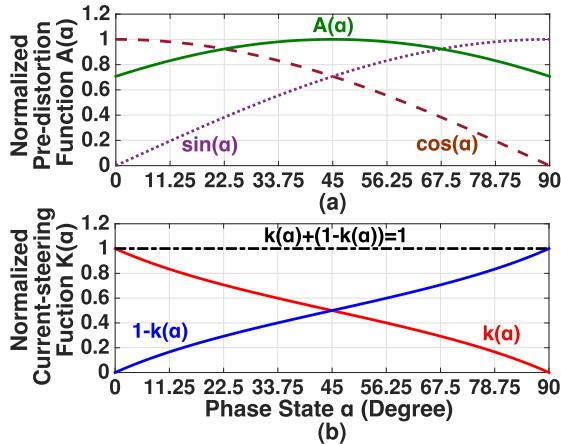


Fig. 9. Simplified schematic of DVGA.

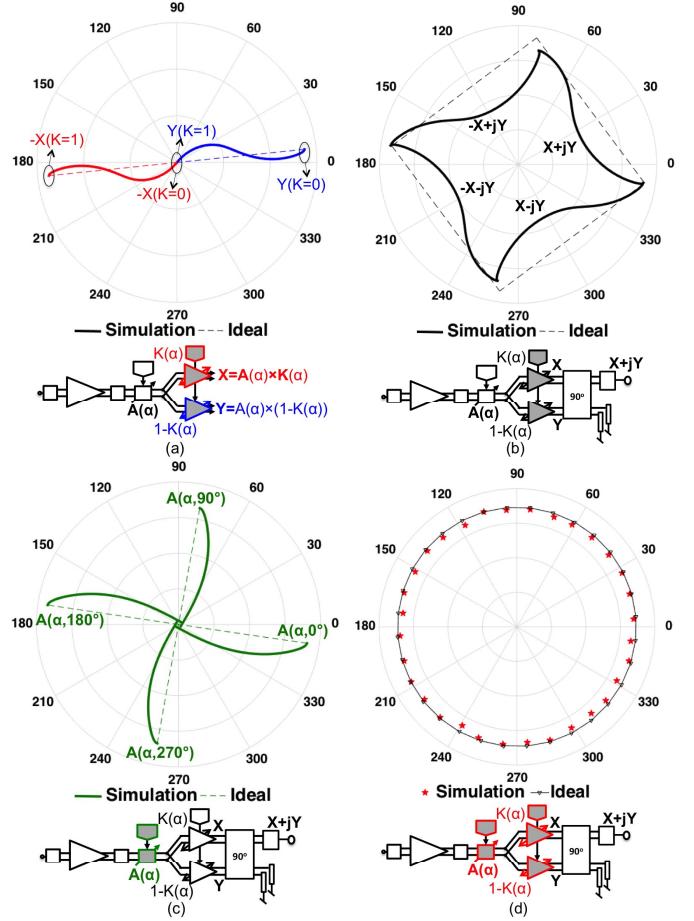
Fig. 10. (a) Ideal predistortion function $A(\alpha)$ across one quadrant according to (6). (b) Ideal current-steering functions $k(\alpha)$ and $1 - k(\alpha)$ across one quadrant according to (7).

of a transconductance and two current-steering operations. The first current-mode stage provides a predistortion of

$$A(\alpha) = G_m \cdot \frac{\sqrt{2}}{2} (|\cos(\alpha)| + |\sin(\alpha)|) \quad (6)$$

where G_m represents the transconductance provided by $Q1$ and $Q2$, and α is the desired phase shift for a given element. Fig. 10(a) shows $A(\alpha)$ across a single quadrant normalized to the maximum value. Predistortion is provided by $Q3-Q6$ and controlled through an 8-b DAC and inverse-tanh cell ($Q15$ and $Q16$). The $\sqrt{2}/2$ in (6) ensures that the current-steering function ($|\cos(\alpha)| + |\sin(\alpha)|$) has a maximum value of one. Finally, the absolute values indicate that the function is identical for all four quadrants, with sign switching handled elsewhere. A second level of current steering is used to direct the current to either outputs X or Y . This is ideally realized with a steering function equal to

$$k(\alpha) = \frac{|\cos(\alpha)|}{|\cos(\alpha)| + |\sin(\alpha)|} \quad (7)$$

Fig. 11. Ideal (dashed line) and simulated (solid line) vector response of front end at 30 GHz with radial axis in linear scale. (a) X and Y current-steering function, $k(\alpha)$ and $1 - k(\alpha)$, without 90° hybrid combiner, illustrating AM-PM errors in $k(\alpha)$. (b) $X + jY$ using only current steering together with 90° hybrid combiner, indicating need for amplitude predistortion. (c) $X + jY$ response as $A(\alpha)$ is varied from zero to full scale for $0^\circ/90^\circ/180^\circ/270^\circ$ states, illustrating AM-PM errors in $A(\alpha)$. (d) Final phase-shifted results across 32 phase settings, demonstrating equalized response.

realized with transistors $Q7-Q14$. Fig. 10(b) shows k and $1 - k$ across a single quadrant. The k -function is controlled through a separate 8-b DAC and inverse-tanh cell ($Q17$ and $Q18$). Output X is given by the cascade of A and $\pm k$ to realize $\pm\sqrt{2} \cdot G_m Z \cos(\phi)/2$, while output Y is given by the cascade of A and $\pm(1 - k)$ to realize $\pm\sqrt{2} \cdot G_m Z \sin(\phi)/2$, where Z represents the impedance of the output network. To achieve four-quadrant operation, sign inversion is included within both the X and Y paths using cross-coupled transistors (shown in the shaded region of Fig. 9).

We now evaluate nonidealities within the DVGA response. Fig. 11(a) shows the simulated transfer function of the DVGA to outputs X and Y on a polar plot when A is fixed, the sign of X is inverted, and when k is varied from zero to one. The ideal response is a straight line. As can be seen, the phase deviates as the amplitude is scaled, introducing an amplitude-modulation to phase-modulation (AM-PM) error. This error arises primarily in our circuit due to a changing output impedance of $Q7-Q14$ as a function of control current. Fig. 11(b) shows the polar response of the DVGA across α

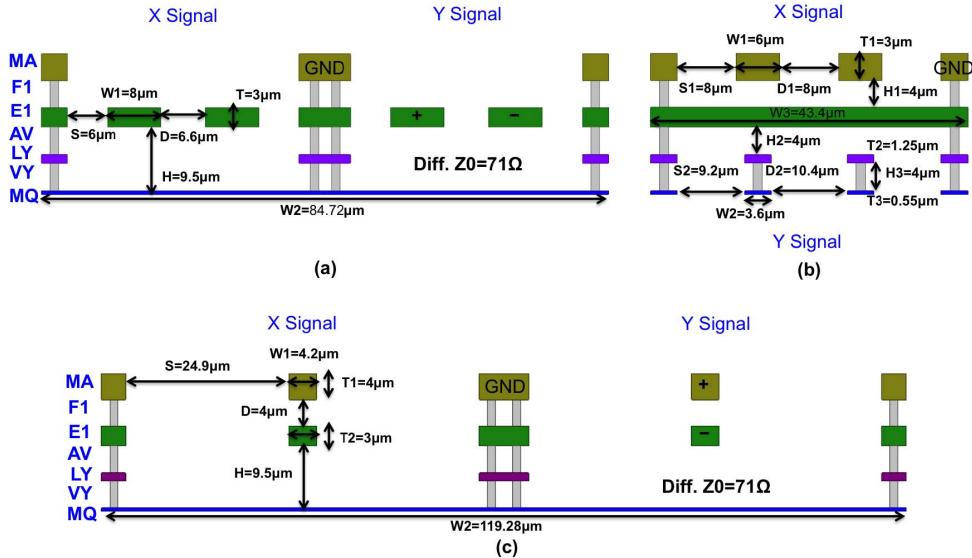


Fig. 12. Cross sections for possible X and Y power combiners to realize $71\Omega Z_{0,\text{diff}}$. (a) Parallel edge-coupled CPW with back-side ground (chosen in our design). (b) Inverted/noninverted edge-coupled CPW. (c) Stacked coupled lines.

when only current-steering function $k(\alpha)$ is applied and when outputs X and Y are combined using our hybrid coupler. The ideal response is diamond-shaped. From Fig. 11(b), we clearly see the need for amplitude predistortion. Fig. 11(c) shows the polar response of the DVGA for the four axis settings (0° , 90° , 180° , and 270°), as the predistortion function, A , is varied from zero to full scale. This indicates an AM–PM error introduced by $A(\alpha)$. Phase errors introduced in both k and A can be compensated by adjusting $k(\alpha)$. Fig. 11(d) shows the polar plot for 5-b phase resolution when predistortion is applied and modified k values are used for compensation, indicating a final equalized response.

The overall circuit was designed to support 5-b phase resolution, with phase states including the axis settings. Since $A(\alpha)$ has its minimum value at 0° , 90° , 180° , and 270° , NF of the DVGA will be the highest for these axis settings. Simulations indicate that the DVGA without predistortion applied shows 5.3-dB gain at 0° setting and -2.3 dB gain at 45° setting, where the ideal difference between having all versus half of the current directed to an output would be 6 dB. For these same settings, NF is 8.6 and 14.5 dB, and iP_{1dB} is +2.7 and +0.9 dBm, respectively. The DVGA draws 16 mA from a 3.3 V supply (52.8 mW).

C. Dual Power Combiner

The X and Y signals from each front end are individually power combined to provide ΣX and ΣY signals. These summations are realized using a two-stage dual-differential Wilkinson structure. Compared with an active combiner structure, passive structures can provide high linearity, high isolation between inputs, bidirectionality, and zero dc power consumption. Key design considerations for the power combiner are achieving: 1) identical electrical performances for X and Y signals; 2) high isolation between X and Y traces; and 3) small area.

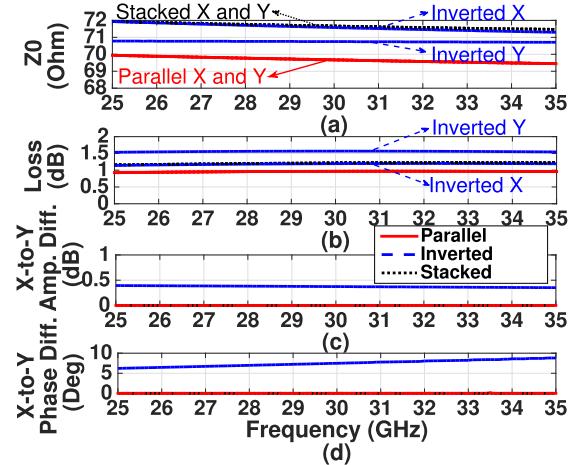


Fig. 13. Simulated results for X and Y parallel edge-coupled (chosen in our design), inverted, and stacked transmission lines for length = $\lambda/4$. (a) Z_0,diff . (b) Loss. (c) Amplitude difference between X and Y . (d) Phase difference between X and Y .

Three possible transmission-line structures have been evaluated using the EMX electromagnetic simulator [23]. The first is shown in Fig. 12(a), where two edge-coupled coplanar waveguide (CPW) with backside ground are placed side-by-side with a ground shield in between. The second is shown in Fig. 12(b), where Y signals are realized in an inverted edge-coupled CPW with a ground plane above the signals. This is then stacked beneath the X structure to achieve a smaller area. The third is shown in Fig. 12(c), where both the X and Y lines are realized with stacked coupled lines and isolated from each other with a center ground shield. The dimensions of each X and Y coupled line in these three structures are chosen to realize a 71Ω differential characteristic impedance ($Z_{0,\text{diff}}$).

Fig. 13 compares the simulated responses for X and Y differential transmission-line test structures of length $\lambda/4$. We

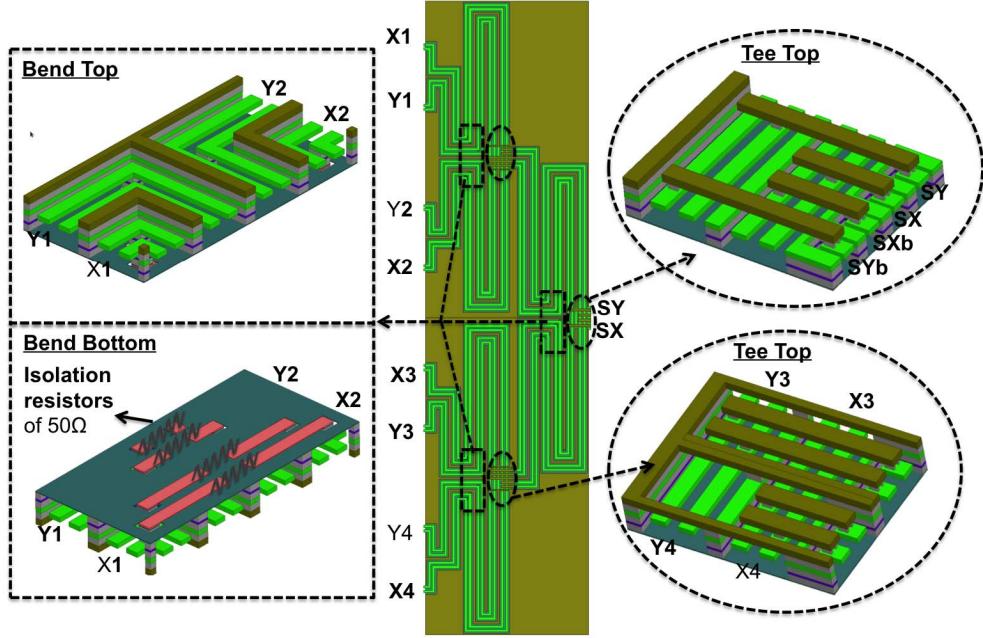


Fig. 14. Illustration of top-level layout of dual-differential X and Y Wilkinson combiners, 3-D views of bends (top and bottom), including isolation resistors, and 3-D view of tee junction at the combining nodes.

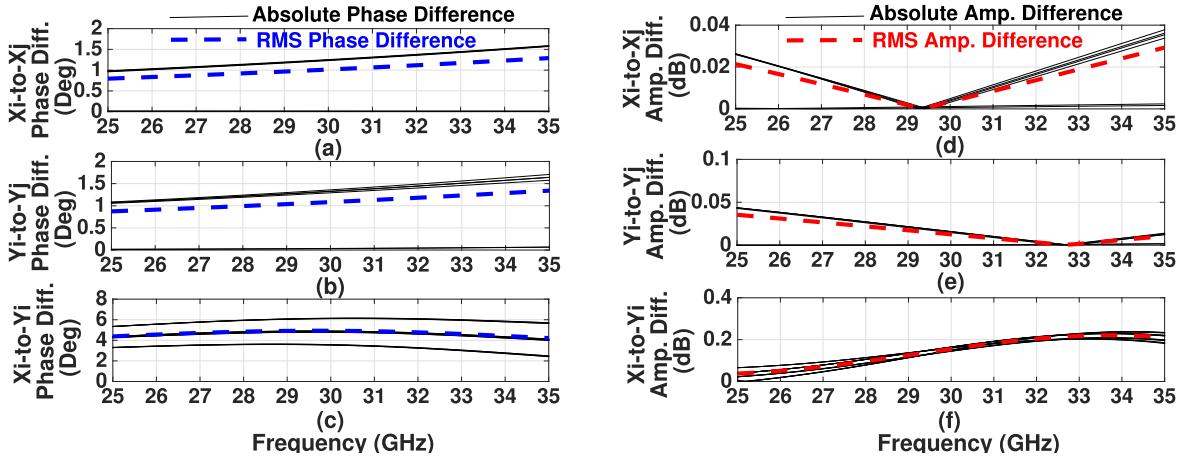


Fig. 15. Simulated mismatch results for X and Y dual two-stage Wilkinson power combiner. (a) X_i -to- X_j phase difference. (b) Y_i -to- Y_j phase difference. (c) X_i -to- Y_i phase difference. (d) X_i -to- X_j amplitude difference. (e) Y_i -to- Y_j amplitude difference. (f) X_i -to- Y_i amplitude difference. Indices i and j refer to any of the four possible input ports for X or Y .

compare $Z_{0,\text{diff}}$, the loss of the X and Y lines, and the amplitude and phase differences between X and Y lines. The stacked inverted structure [Fig. 12(b)] can achieve half the cross-sectional area for the same $Z_{0,\text{diff}}$ of $71\ \Omega$; however, the simulations show that the X and Y lines have a different loss and phase shift since the lower lines are exposed to the silicon substrate, impacting phase velocity, and are realized in thinner metals, increasing loss. In contrast, both the edge-coupled [Fig. 12(a)] and stacked [Fig. 12(c)] coupled lines can achieve identical electrical performance for X and Y due to identical cross sections. Since the stacked structure is larger, we choose the edge-coupled CPW structure.

Fig. 14 shows the layout of the two-stage dual-differential power combiner, along with details on the junctions and

crossovers for this structure. The overall area impact of having parallel power combiners necessary for dual-vector distributed beamforming rather than a single power combiner used for traditional beamforming is estimated to be an approximate doubling of the combiner area for 28 GHz. Having two side-by-side couplers prevents us from realizing as tight of a meandering. The area penalty depends on the amount of meandering applied to the transmission lines, where less meandering is required at higher frequencies (due to reduced wavelength); hence, the penalty is reduced as you move toward higher frequencies. This area penalty can be eliminated by shifting from a parallel combiner to a series-combiner structure and has been incorporated in a follow-on design of our beamformer.

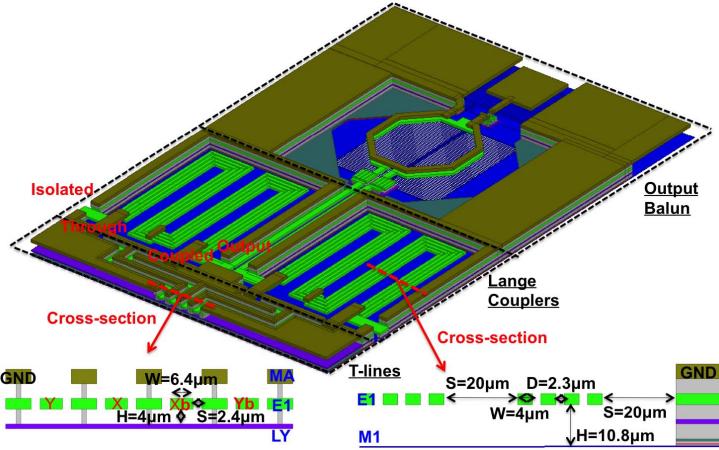


Fig. 16. Illustration of top-level layout of quadrature combiner composed of an input distribution network, a pair of Lange couplers, and an output transformer. Cross sections provided for the input feed and the Lange.

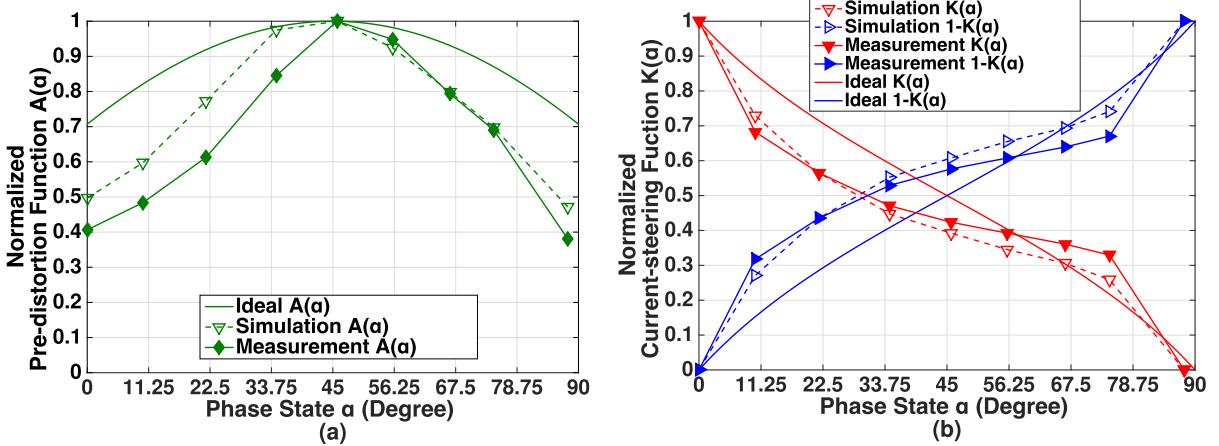


Fig. 17. Comparison between ideal, simulated, and measured (a) predistortion function $A(\alpha)$ and (b) current-steering functions $k(\alpha)$ and $1 - k(\alpha)$ over eight phase states of α within one quadrant.

EMX simulations indicate a total insertion loss of less than 2.3 dB and return loss for all ports better than 10 dB across 25–35 GHz. Amplitude and phase differences between any input and the σX and σY outputs are 0.3 dB and 4.3° , respectively. These errors are shown in Fig. 15, illustrating phase and amplitude differences between all X responses, all Y responses, and between X and Y responses. Errors are depicted in both absolute and root-mean squared (rms) terms. The phase error is due to slightly different lengths of coupled lines at the bends and junctions, but this skew is sufficiently low to keep the unwanted conjugate sidelobe 27 dB below the main lobe, using (5). Isolation between individual X (or Y) inputs and between X and Y inputs exceeds 19 and 45 dB at 30 GHz, respectively.

D. Quadrature Combiner

The global quadrature combiner is realized using a balanced pair of 90° Lange couplers for differential quadrature summation and then a spiral transformer balun. This topology was chosen over lumped or distributed branchline couplers

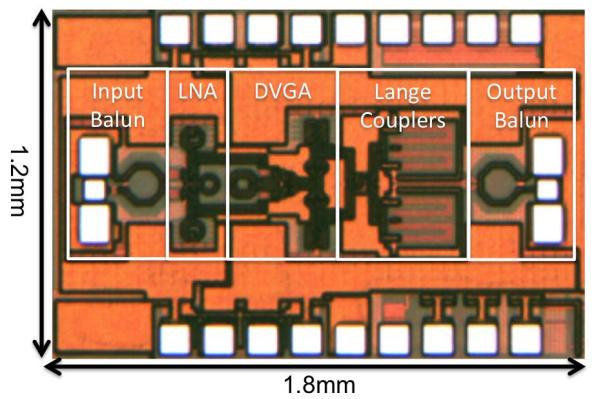


Fig. 18. Die micrograph of receiver front end. Die size is $1.8 \times 1.2 \text{ mm}^2$.

to achieve a smaller area and chosen over an all-pass filter topology [24] to provide less sensitivity to capacitive loading effects. A drawing of the quadrature combiner with output balun is shown in Fig. 16. First, an input distribution network

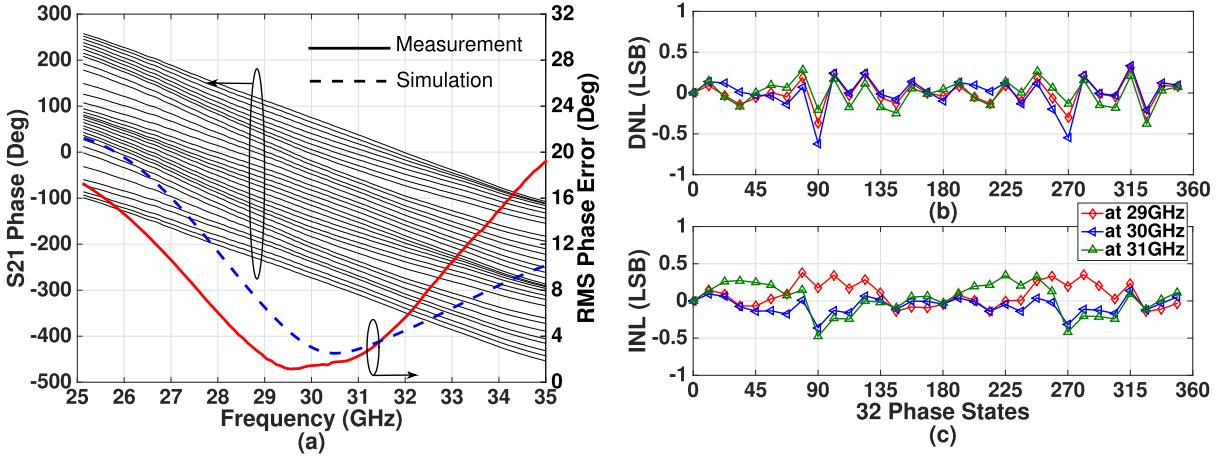


Fig. 19. Measured (a) S_{21} phase response and rms phase errors versus frequency across 32 phase settings for the receiver front end with DVGA calibrated for 30-GHz operation. (b) S_{21} phase DNL. (c) S_{21} phase INL.

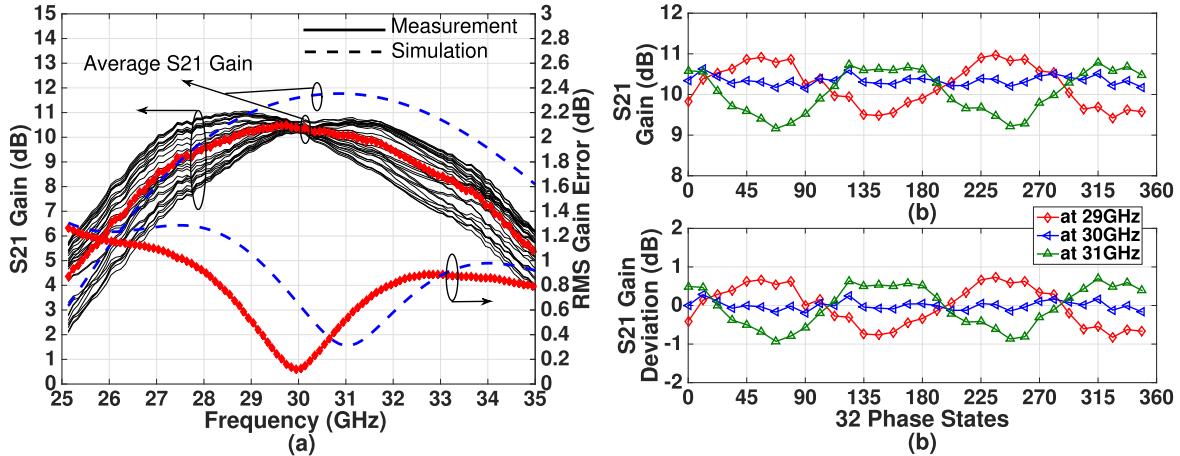


Fig. 20. Measured (a) S_{21} gain response and rms gain errors versus frequency across 32 phase settings for the receiver front end with DVGA calibrated for 30-GHz operation. (b) S_{21} gain. (c) Gain deviation.

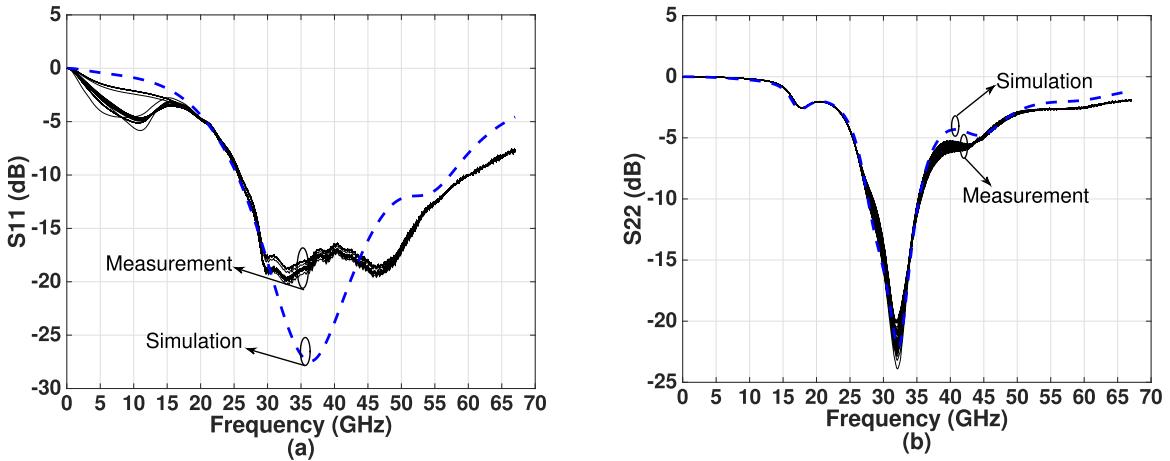


Fig. 21. Measured (a) S_{11} and (b) S_{22} magnitude responses over 32 phase settings for the receiver front end.

is included to fan-out the dual-differential outputs (X , \bar{X} , Y , and \bar{Y}) to the couplers, with X and Y provided to one Lange and \bar{X} and \bar{Y} provided to the other. Each Lange coupler is

realized with four interdigitated coupled lines on the second-to-top metal layer (E1) over a metal-1 ground plane. This layer has a smaller pitch than the top layer (MA) and can

therefore realize higher coupling. Total (unwound) length of each Lange coupler is 1.25 mm, each linewidth is 4 μm , and line spacing is 2.3 μm . Each Lange coupler is meandered to save area. The total area of the quadrature combiner is 0.35–0.19 mm^2 coming from the two Lange couplers and 0.16 mm^2 coming from the balun. EMX simulation results indicate a 2.6-dB insertion loss (1.1 dB from coupler and 1.5 dB from balun), 89° phase difference between outputs, and 1-dB amplitude difference between inputs across 25–35 GHz, all when the coupler is loaded with ideal terminations on all ports. The surrounding circuits, however, provide more narrow-band terminations; hence, the quadrature accuracy is reduced. This accuracy will be demonstrated in the measurement section by comparing amplitude and phase between axis settings.

IV. MEASURED RESULTS

A. Calibration Methodology

The phase and amplitude of each element is controlled through two 8-b DACs to realize predistortion and current-steering functions. Here, we describe our methodology for determining the proper control settings. During the measurement, we first choose DAC settings of the current-steering function $k(\alpha)$ to achieve the desired 5-b phase response without turning on predistortion. Once the minimum gain is determined from these 32 responses, we then equalize all other gains to this lower value using the predistortion control DAC for $A(\alpha)$. Since there is slight phase deviation due to the predistortion [shown in Fig. 11(c)], the current-steering function is adjusted accordingly, where the amount of adjustment is only a few least significant bits (LSBs).

Fig. 17(a) and (b) shows the comparison between ideal, simulated, and measured predistortion and current-steering functions over eight phase states within one quadrant, where the other three quadrants have the similar result. The current settings for the measurements are plotted assuming ideal DAC performance (25- μA LSB). From Fig. 17, we can conclude a few things. First, the overall amplitude is set by the front-end's gain at 45°. Second, the amount of predistortion needed for the axis settings is larger than predicted, which will lead to poorer NF performance along the axes (0°, 90°, 180°, and 270° phase settings). This reduction comes from lower signal amplitude at the 45° setting arising from the phase deviations of X and Y as a function of $k(\alpha)$. This phase offset between X and Y reduces the amplitude of the combined signal. With lower amplitude at 45°, the axis settings must be reduced further to equalize. Finally, at 45°, the required weighting between X and Y is unequal. This accounts for the amplitude-phase dependence within the DVGA, shown in Fig. 11.

B. Single Front-End Characterization

A single front-end breakout was realized for test purposes. This breakout includes the active front end plus the differential quadrature power combiner. A die micrograph of the breakout is shown in Fig. 18. The area of the front end including the quadrature hybrid is 1.08 mm^2 without pads. Notably, the area of the combiner is nearly identical to that of the active circuits,

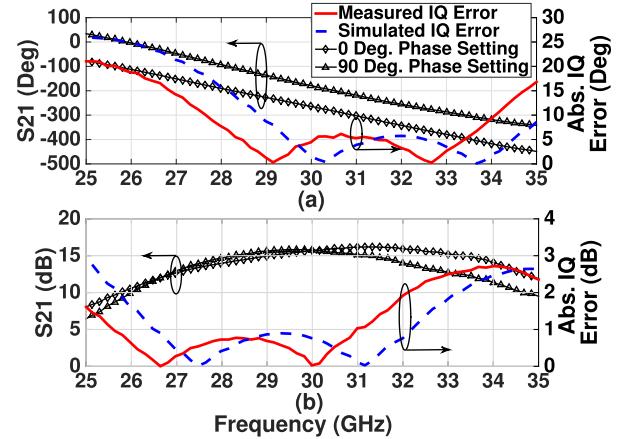


Fig. 22. Measured *IQ* phase and amplitude errors for the front end at 0° and 90° phase settings without predistortion.

pointing to the front-end area savings possible by switching to dual-vector distributed beamforming.

Fig. 19(a) shows the measured phase of S_{21} of the single-channel receiver front end across phase settings. The rms phase error after calibration is <5.4° at 28–32 GHz. Fig. 19(b) shows the differential nonlinearity (DNL) and integral nonlinearity (INL) of the phase responses, indicating errors less than ± 0.5 LSB. The measured gain ($|S_{21}|$) across 32 phase states is shown in Fig. 20(a) indicating an average peak gain of 10.5 dB at 29.7 GHz with a 24.5% 3-dB bandwidth of 26.5–33.9 GHz. The rms gain error after calibration is <0.9 dB across 25–35 GHz. Fig. 20(b) and (c) shows the magnitude of S_{21} and gain deviation from the average gain over 32 phase settings at 29–31 GHz. The gain deviation is less than ± 1 dB and can be improved by further adjustment of the predistortion. Input and output return losses are greater than 10 dB across the band, shown in Fig. 21. The measured s-parameters match simulations, with all simulation results shown in these Figs. 19–22. with dashed lines. Finally, to evaluate the quadrature accuracy within the front end, we compare the amplitude and phase difference between axis settings (0° and 90°). Fig. 22 (a) and (b) shows measured phase error less than 5° and amplitude error less than 0.8-dB from 28.5 to 30 GHz.

As indicated earlier, the noise performance along the axis settings will be worse due to the attenuation needed for predistortion, which accentuates the noise in the final current-steering stage. This issue can be mitigated by avoiding the axis settings altogether, as we reported in [11]. Thus, we can revert the array to 4-b performance and skip every other state to reduce the maximum NF by about 1 dB. Here, we present both the 5-b and 4-b results to illustrate the tradeoffs. Fig. 23(a) shows the simulated and measured NF versus frequency across all 32 states (5 b). The measured NF is 5.6–8.6 dB. Fig. 23(b) shows the NF across both 4-b (solid symbols) and 5-b (empty plus solid symbols) phase settings at 29–31 GHz, clearly indicating how the NF rises for settings closer to the axes. To improve the noise performance, the DVGA architecture could be altered such that the predistortion function is realized with increased G_m rather than decreasing RF current, although

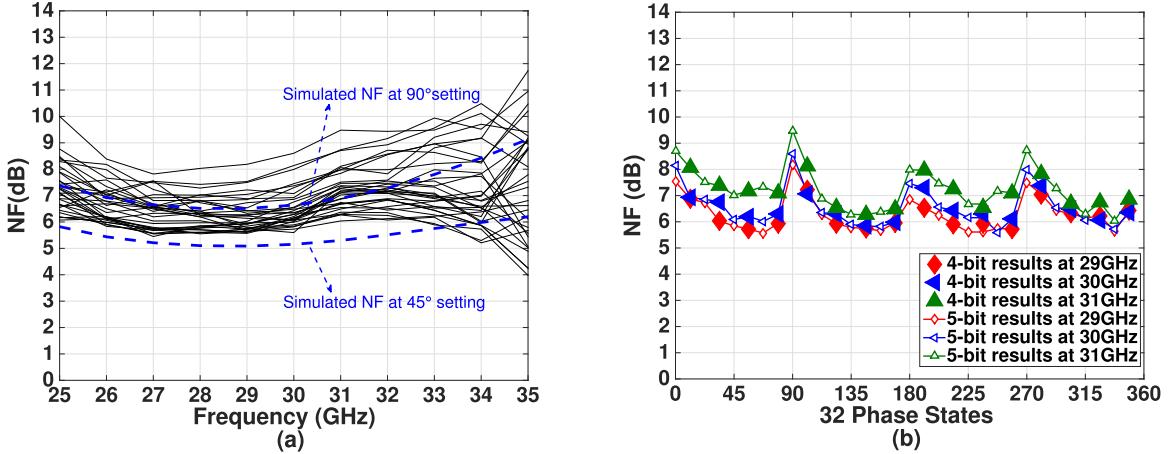


Fig. 23. Measured and simulated (a) NF across frequency over 32 phase settings and (b) NF across 32 phase settings at 29–31 GHz (solid symbols are for 4-b results and empty symbols are for 5-b results).

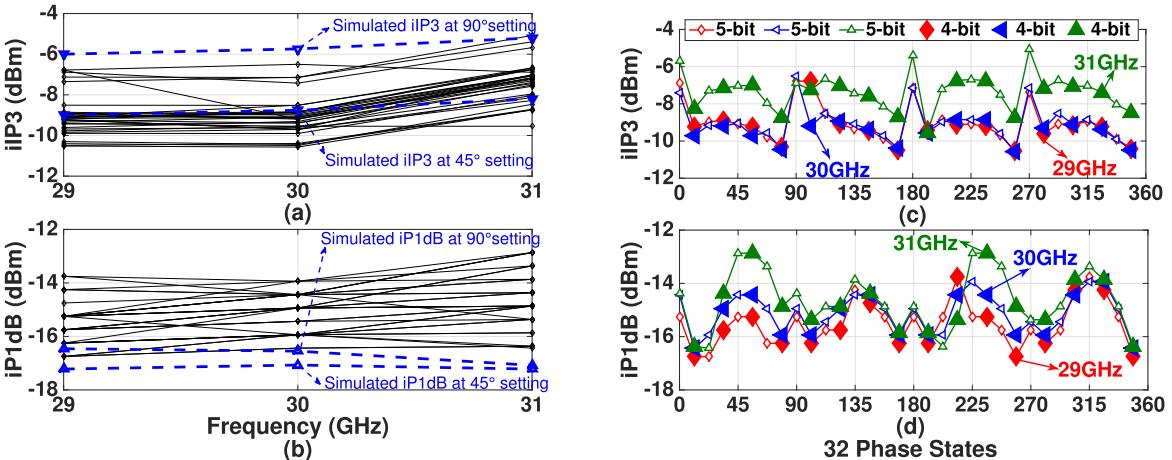


Fig. 24. Measured and simulated (a) iIP₃ and (b) iP_{1dB} across frequency over 32 phase settings. Measured (c) iIP₃ and (d) iP_{1dB} across 32 phase settings at 29–31 GHz (solid symbols are for 4-b results and empty symbols are for 5-b results).

this would slightly impact the interstage matching between the LNA and DVGA.

As shown in Fig. 24(a) and (b), the measured iIP₃ and iP_{1dB} of the front end are -10.6 to -5.7 dBm and -16.8 to -12.9 dBm, respectively. Fig. 24(c) and (d) shows iIP₃ and iP_{1dB} across both 4-b (solid symbols) and 5-b (empty plus solid symbols) phase settings at 29–31 GHz. The iIP₃ behavior is inverse to that of the NF behavior, indicating that the overall dynamic range of the front end is relatively constant across 32 phase settings.

C. Four-Element Receiver Array Characterization

The block diagram and the die photograph for the four-element receiver array are shown in Figs. 4 and 5, respectively. Now that individual front-end element is fully characterized, we measure the element-to-element matching as well as the isolation between elements. First, for matching, we compare the responses of all four chains at 90° phase setting. The results are shown in Fig. 25, where the data are normalized to the response in the first element. This indicates rms phase and gain mismatch errors of $< 5^\circ$ and 0.6 dB, respectively. Low rms

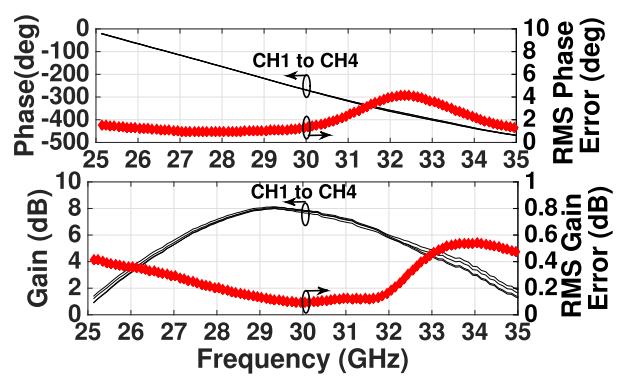


Fig. 25. Measured element-to-element phase and gain matching, channels 1–4, at 90° setting.

phase and gain mismatch errors are achieved due to low mismatch between each receive channel and low amplitude and phase imbalance in the two-stage dual X and Y Wilkinson power combiners.

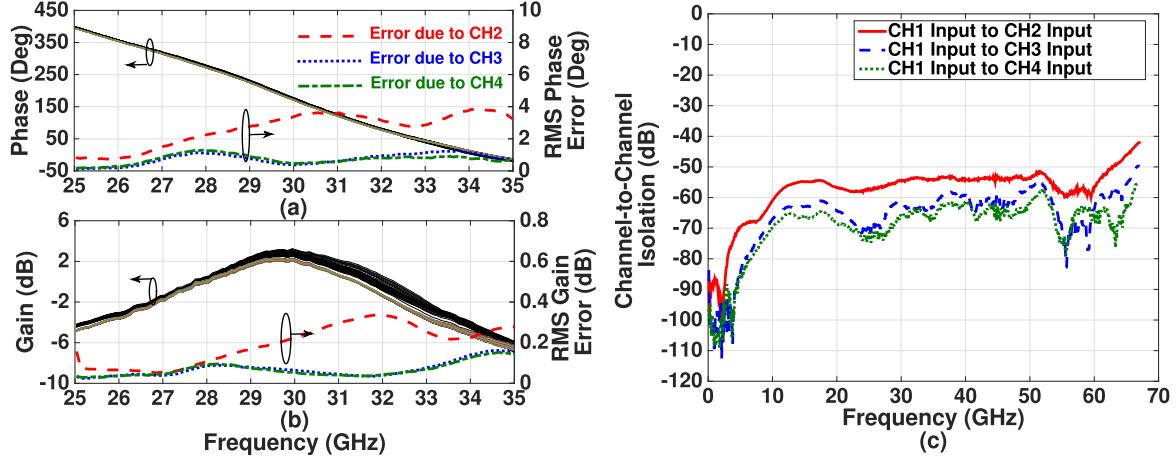


Fig. 26. Channel-to-channel isolation demonstrated through measured phase and gain errors in channel 1 as channels 2–4 are swept across all phase settings. Channel 1 is held at 0° setting.

TABLE I
COMPARISON OF RF PHASED-ARRAY RECEIVER FRONT-ENDS

Reference	This Work	[25] Yu RFIC'09	[15] Kodak RFIC'16	[13] Min JSSC'08	[17] Natarajan VLSI'09	[26] Natarajan ISSCC'07
Technology	130-nm SiGe	130-nm CMOS	45nm SOI CMOS	120-nm SiGe	130-nm SiGe	130-nm SiGe
Phase Shifting Method	Dual Vector Interpolator	Vector Interpolator	Switched LC	Switched LC	RTPS	Varactor- Loaded Line
Diff. /Single-ended	Diff.	Diff.	Single-ended	Diff.	Single-ended	Single-ended
Frequency (GHz)	28-32	24-27	26-28	33-35	60	60
Phase Resolution	4-bit	4-bit	5-bit	4-bit	$V_{Control}$	$V_{Control}$
Phase Error (°)	< 5.4	< 6	< 4	< 1	< 3.9	-
Average Gain (dB)	10.5	15	12.2	10	14	20
Gain Error (dB)	< 0.6	< 0.5	< 0.6	< 0.35	< 0.5	-
NF (dB)	5.1-8.5	7.8-9.5	4-4.7	3.8	6	5.3-6.9
P_{1dB} (dBm)	-16.4 to -12.9	-22 to -19	-8	-28	-34 to -26	-33.5
iIP ₃ (dBm)	-10.4 to -6.8	-12 to -9	0.5	-20	-	-
DC Power (mW)	136.5 (97.5 w/o DACs)	230	42	33	48.6	66.3
Front-end Area (mm^2)	0.3**	0.34**	1.24*	0.33*	0.77*	0.68*

* Estimated area per front-end element.

** Estimated area excluding any input balun per front-end element.

Isolation measurements demonstrate how the phase settings of an adjacent (aggressor) element affects the phase response of a given (victim) element. The coupling errors are obtained by measuring the response of element two at 0° phase setting when the settings of element one are changed across 32 phase states. The measured results in Fig. 26(a) and (b) show <4.2° of rms phase isolation error and <0.5 dB of rms gain isolation error at 25–35 GHz. In addition, Fig. 26(c) shows the isolation between nonadjacent elements, which improves, as expected.

V. CONCLUSION

In this paper, we have demonstrated a dual-vector four-element phased-array receiver in 130-nm SiGe BiCMOS technology operating from 25 to 35 GHz. The design relies on dual-vector scalar-only weighting functions within each front end to reduce size to 0.3 mm² per chain and increase fractional bandwidth to 24.5%. Each array element achieves 5.1 to 7 dB (5.1 to 8.5 dB) NF, -16.8 to -13.8 dBm

(-16.4 to -12.9 dBm) iP₁ dB, and -10.5 to -8.9 dBm (-10.4 to -6.8 dBm) iIP₃ across 4-b (5-b) phase settings. Average gain is 10.5 dB at 29.7 GHz and power consumption is 136 mW per element. Compared with other front ends in Table I, this paper achieves among the lowest area and among the highest fractional bandwidths. As can be expected, active phase shifter topologies will consume more power over passive approaches. While dual-vector distributed beamforming eliminates the quadrature coupler from each front end, this area savings may be negated by the increased area in a dual parallel power combiner. In the future work, we are investigating the use of a dual series-combiner structure which has the potential to eliminate this area overhead and thereby dramatically reduce the size of the array.

ACKNOWLEDGMENT

The authors would like to thank N. Cahoon and GlobalFoundries for providing SiGe 8HP chip fabrication,

Analog Devices Inc., for project support, UT Dallas for use of their noise diode, and Kevin Greene from NCSU for the helpful discussions on the dual-vector variable-gain amplifier.

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