Embedded Memory and ARM Cortex-M0 Core Using 60-nm C-Axis Aligned Crystalline Indium–Gallium–Zinc Oxide FET Integrated With 65-nm Si CMOS

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***Abstract*— Low-power embedded memory and an ARM Cortex-M0 core that operate at 30 MHz were fabricated in combination with a 60-nm c-axis aligned crystalline indium–gallium–zinc oxide FET and a 65-nm Si CMOS. The embedded memory adopted a structure wherein oxide semiconductor-based 1T1C cells are stacked on Si sense amplifiers. This memory achieved a standby power of 3 nW while retaining data and an active power of 11.7 μW/MHz by making each bitline as short as each sense amplifier. The Cortex-M0 core adopted a flip-flop (FF) in which an oxide semiconductor-based 3T1C cell is stacked on the Si scan FF cell without area overhead, and achieved a standby power of 6 nW while retaining data. This combination of embedded memory and Cortex-M0 core can provide high-performance as well as low-power operation, which is essential for Internet of Things devices.**

***Index Terms*— C-axis-aligned crystalline indium–gallium–zinc oxide (CAAC-IGZO), dynamic oxide semiconductor random access memory (DOSRAM), OFF-state current, oxide semiconductor flip-flop (OS-FF), power gating.**

I. Introduction

MICROCONTROLLER units (MCUs) for Internet of Things (IoT) devices require low power consumption to achieve long battery life as well as some amount of computation power when they are active. For sensor applications, the proportion of module standby time is much greater than that of module active time; thus, the proportion of standby power to total power consumption can be high. Therefore, MCUs for IoT devices require reduced standby as well as active power as much as possible.

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Power gating is effective in reducing standby power. When MCUs are power gated, state-retention flip-flops (SR-FF) or nonvolatile memory are used to prevent data loss [1]–[3].

In contrast, decreasing drive load is the simplest and favorable way to reduce active power. Power supply voltage could be lowered to decrease power consumption; however, there is a tradeoff between operating speed and power supply voltage. In order to satisfy different product requirements, both high operating speed and low power consumption are required.

To reduce both standby power and active power, the use of c-axis aligned crystalline indium–gallium–zinc oxide (CAAC-IGZO) FETs has been considered in this paper. The CAAC-IGZO is a new channel material that exhibits very low OFF-state current. Previously, we have reported an OFF-state current of 3.8×10^{-22} A/μm in a single FET with a channel width W/channel length $L = 40/100$ nm [4]. The OFF-state current of the FET is approximately ten orders of magnitude less than that of a commonly used Si-FET. CAAC-IGZO FETs are commonly used in display fields; however, they are used less frequently in LSI. The characteristics of CAAC-IGZO FETs have also been demonstrated in a 20-nm node, and it is anticipated that CAAC-IGZO FETs will be applicable to LSI [5].

We have previously reported DRAM-like memory that has a CAAC-IGZO FET and a storage capacitor [6]. We refer to this type of memory dynamic oxide semiconductor random access memory (DOSRAM). The write energy of the DOSRAM would be lower than that of current-driven emerging memory, because data are written to a cell by storing charge into a small storage capacitor. In a recent study, we confirmed retention for more than 1 h at 85 °C with a 60-nm CAAC-IGZO FET at a cell level with no Si circuit [7]. There is also an earlier report on an ARM Cortex-M0 core with CAAC-IGZO FETs [8]. This chip was fabricated by the laboratory level process, and 60-nm CAAC-IGZO FETs were stacked on a 180-nm Si CMOS to form an SR-FF. This chip could perform low-power operations by reducing static power with fine-grained power gating. In this paper, to investigate the possibility of using CAAC-IGZO FETs with LSI, we have

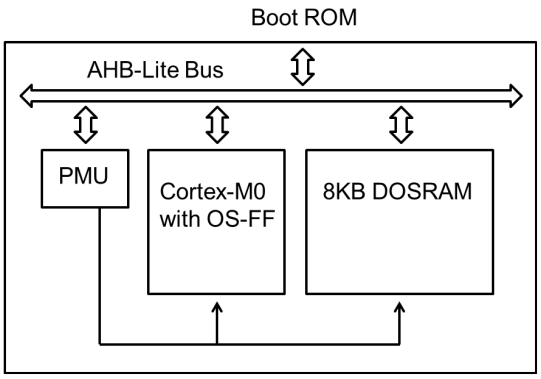

Fig. 1. Block diagram of a fabricated chip.

combined foundry-fabricated Si CMOSs with CAAC-IGZO FETs to fabricate memory and a core.

II. CAAC-IGZO FET Circuit Design

The circuit design of CAAC-IGZO FETs and circuit features are explained in this section. First, an overview of the fabricated chip is presented. Then, embedded memory and an FF in the microcontroller core are described in detail.

A. Fabricated Chip

Fig. 1 is the block diagram of the fabricated chip. The chip consists of a Cortex-M0 core, an AHB-Lite bus, an 8-kB DOSRAM as memory, and a power management unit (PMU). Each of a DOSRAM cell and the FF in the Cortex-M0 core includes a CAAC-IGZO FET and a storage capacitor (1OS1C), which is the smallest unit of a CAAC-IGZO memory cell. The power supply voltage of a logic component is 1.1 V, and the power supply voltage of a CAAC-IGZO FET gate is 3.3 V. Power gating of these two blocks is controlled by the PMU. The chip has three standby modes: a normal mode without low-power operation (i.e., the core performs an NOP operation), a clock gating mode in which the supply of clocks to the core and the memory is stopped, and a power gating mode in which the supply of power to the core and the memory is stopped.

B. Dynamic Oxide Semiconductor Random Access Memory

In this section, DOSRAM, which has a CAAC-IGZO FET and a storage capacitor, is described. First, basic cell operation is described, and a circuit diagram is provided. Next, the advantages of DOSRAM in terms of low power consumption are explained. Finally, the 8-kB array configuration of the fabricated chip is shown.

A DOSRAM cell circuit diagram and the peripheral circuits used in this prototype are shown in Fig. 2. The DOSRAM cell operation is basically the same as the DRAM operation, i.e., charging and discharging of a storage capacitor by an access transistor. A Si circuit has a basic and simple configuration. Fig. 3 is a timing diagram of the DOSRAM operation. In a standby mode, BL and BLB are precharged to VDD/2 and short-circuited by an equalizing transistor. In a data read

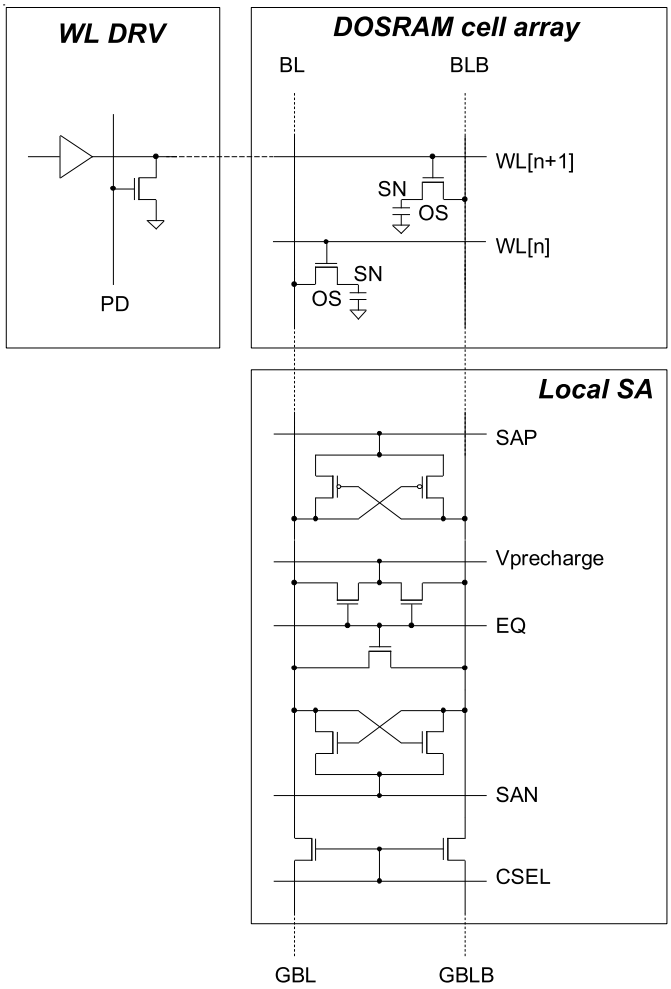

Fig. 2. Circuit diagram of a DOSRAM cell, a sense amplifier, and a multiplexer.

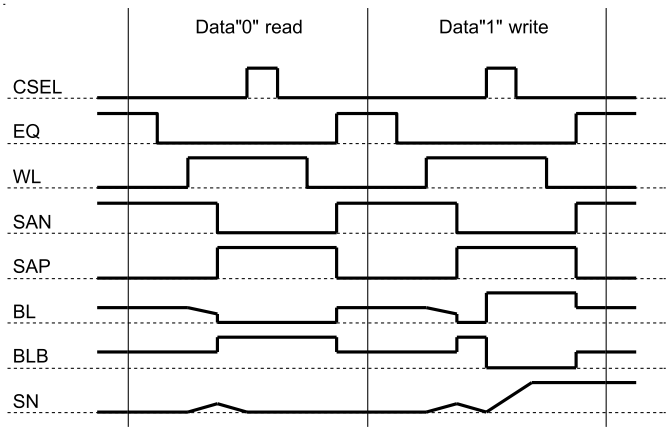

Fig. 3. Timing diagram of DOSRAM operation.

operation, an EQ signal is set at a low state in a selected local array, and BLs and BLBs enter a floating state. Then, a selected WL is opened, and charge is transferred between the storage capacitor in the cell and a BL or BLB. A read signal generated from the charge transfer is amplified by a sense amplifier in the next step. The selected sense amplifier is connected to a global BL (GBL) by a column select

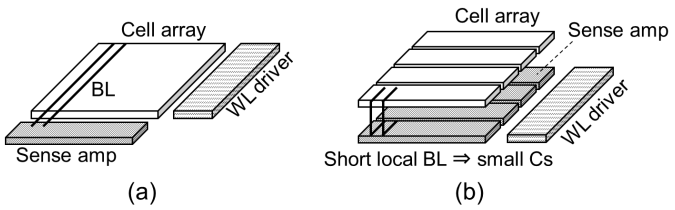

Fig. 4. Shortening BL by a stack structure. (a) Without the stack structure. (b) With the stack structure.

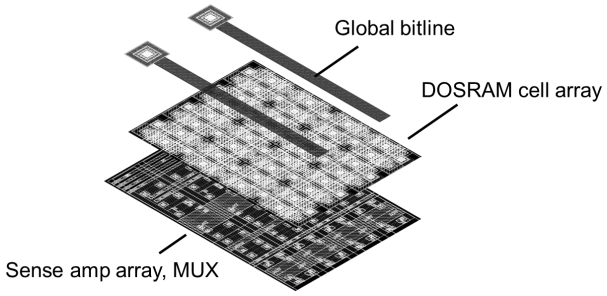

Fig. 5. Layout of a DOSRAM cell array and a sense amplifier array.

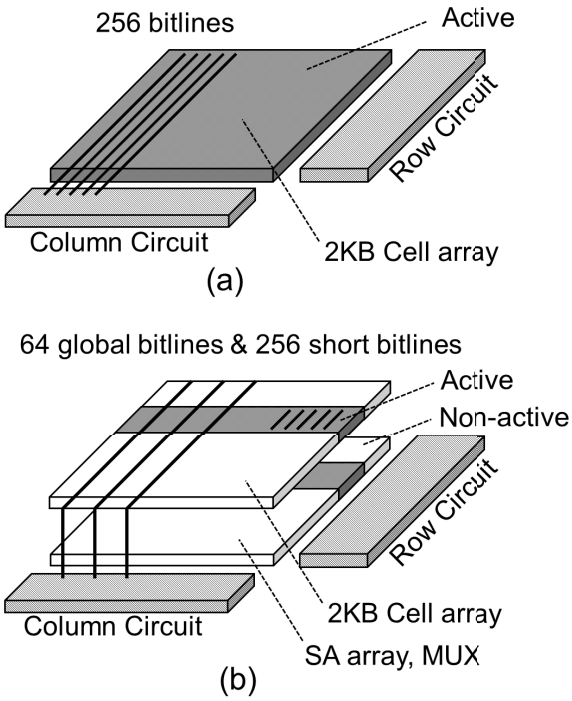

Fig. 6. Active regions during access. (a) Without a stack structure. (b) With a stacked array.

signal (CSEL), and data are read to a column circuit through the GBL. Then, the data are restored, and control signals, other than the EQ signal, are negated sequentially; thus, BLs and BLBs are precharged again. Data write operation is the same as the data read operation until data are read to a local sense amplifier. When the GBLs are connected to the sense amplifier by a CSEL, write data are given to GBLs from the column circuit, and data of the selected sense amplifier are rewritten. Then, the rewritten data are written to the cell, and the data write operation is completed. Finally, the signals, other than the EQ signal, are negated, and the DOSRAM cell is set to the standby mode in which the BL is precharged. In the case of power gating, a signal for WL pull-down (PD) is input from the PMU to prevent noise from being added to a WL. Then, the mode is switched between the power gating mode and the other standby modes simply by turning the power OFF or ON.

Next, we explain why DOSRAM is effective in reducing power consumption. One advantage of DOSRAM is that, given the stack structure, BLs are shortened. Fig. 4(a) shows a general DRAM subarray. BL length influences the chip cost and performance. If BLs are short, the BL load is reduced. Thus, the storage capacitance required to obtain read signals is also reduced. Therefore, the drive load related to the array operations is reduced and the performance levels are increased. However, if BLs are short and the number of small separated arrays increases, the proportion of the area of peripheral circuits to the total chip area increases; as a result, bit cost increases. On the other hand, if the DOSRAM cell is fabricated in back end of line process, it is possible to stack the cell array on the sense amplifier by layout design change. That is, as shown in Fig. 4(b), the array can be divided in the BL direction without any area overhead as long as the size of the array does not exceed the size of the sense amplifier. In other words, given the DOSRAM stack structure, the BL load and the storage capacitance can be reduced, which, in turn reduces active power requirements.

An example DOSRAM layout is presented in Fig. 5. The DOSRAM cell array is stacked on the sense amplifier and a multiplexer. In this example, the local BL has a length of four cells of a folded array. In this prototype, the sense amplifier and the multiplexer are placed per local array. Therefore, the number of GBLs is decreased, and the drive load per bit is further reduced. Fig. 6 is a conceptual diagram of load per bit. Without the stack structure [Fig. 6(a)], a large number of long dense BLs must be driven to read data from the cell. On the other hand, with the stack structure [Fig. 6(b)], there is a large number of short dense local BLs and a small number of long loose GBLs. Therefore, with the stack structure, the drive load per bit is decreased. The contribution of the stack structure to reduction in energy consumption was estimated by simulation (Fig. 7). In a 2-kB subarray without the stack structure, 256 BLs and a storage capacitance (Cs) of 30 fF were assumed. With the stack structure, 256 BLs, Cs of 3.5 fF, and 64 GBLs were assumed. The simulation results indicate that energy consumption is reduced by more than 70% with the stack structure, because the load of the BLs and Cs is reduced.

Fig. 8 shows the configuration of the 8-kB DOSRAM included in the fabricated chip. The cell size is 2.9 μm^2. Cs is 3.5 fF, and the capacitor area is 1.2 μm^2. The large cell size is due to the wide margins for additional design rules that are introduced for the new process. The additional design rules are mainly design rules for the connection between UMC's foundry line and our prototype line and the limitation of equipment in the prototype line, and substantially unrelated to IGZO FETs. The cell size can be reduced easily after the foundry process is established. Sixteen local arrays with the stack structures are arranged in eight WLs by 256 BLs to form

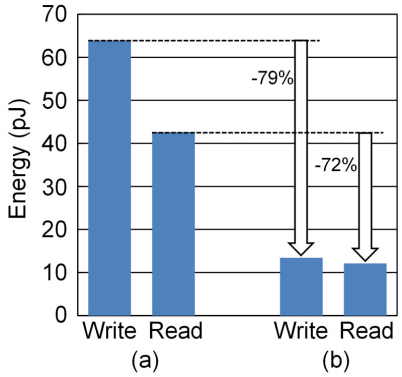

Fig. 7. Active energy simulation results of 2-kB DOSRAM macros.

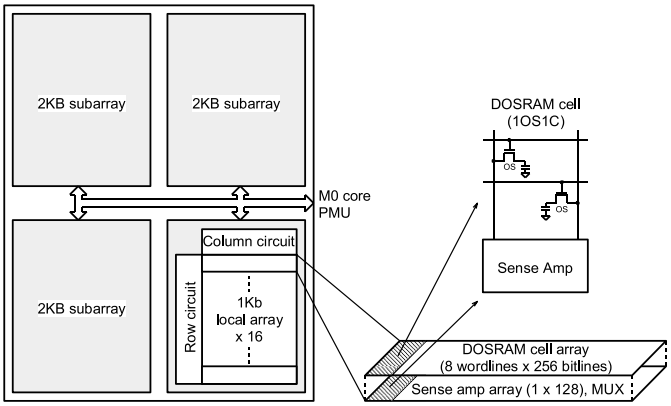

Fig. 8. 8-kB DOSRAM configuration.

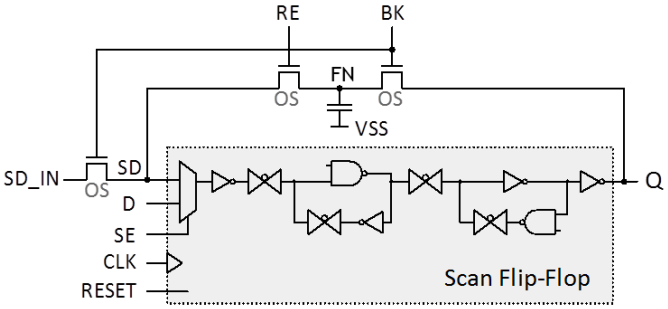

Fig. 9. OS-FF circuit diagram.

the 2-kB subarray. The BL length of this subarray is one-sixteenth of that of the subarray without any stack structure. Each local array is connected to the column circuit through a GBL. Four subarrays construct the 8-kB DOSRAM. The data bus width is 32 b.

C. Oxide Semiconductor Flip-Flop

An SR-FF using CAAC-IGZO FETs is described in this section. The SR-FF is fabricated without any performance or area overhead using foundry's standard cell.

Fig. 9 is a circuit diagram of the SR-FF. The SR-FF is fabricated by adding three CAAC-IGZO FETs and one capacitor to UMC's scan FF cell. By adding only the CAAC-IGZO FETs and the capacitor, an oxide semiconductor FF (OS-FF) can be achieved without any change to the original circuit. The storage capacitance of the added capacitor is 15 fF,

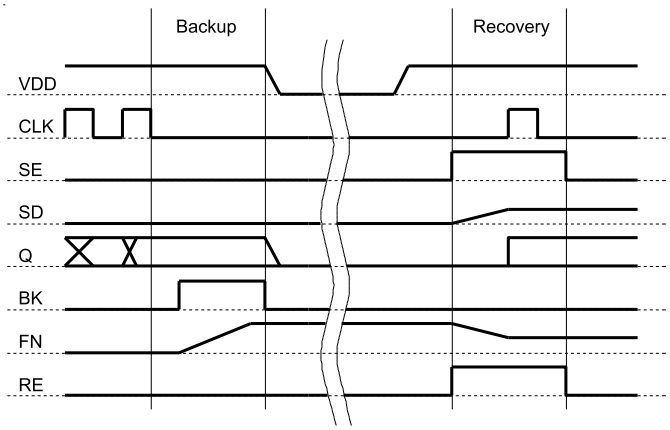

Fig. 10. Timing diagram of OS-FF operation.

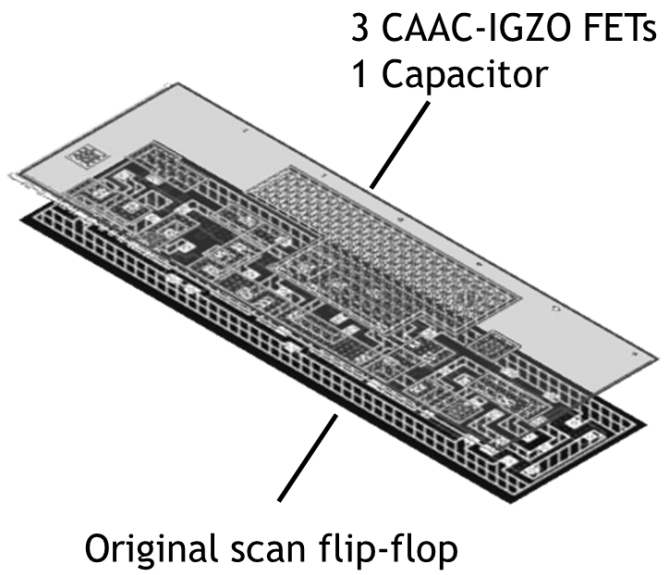

Fig. 11. OS-FF layout.

and the capacitor area is 8.3 μm^2. Fig. 10 is a timing diagram of the OS-FF operation. The OS-FF uses a D terminal in normal operation; thus, the OS-FF operation is the same as the original scan FF operation, i.e., the overhead in normal operation is negligible. In backup operation, first, the CLK supply is stopped. Data are backed up from "D" to "FN" by inputting a BK signal. Data are retained by setting the BK signal to a low level before turning OFF the power. Charge is retained by the extremely low OFF-state current of the CAAC-IGZO FET during power gating. In data recovery operation, first, the charge of "FN" is transferred to "SD" by raising "RE" and "SE." Next, the data of "SD" are recovered to the master side of the FF by clock input. Finally, data recovery is finished after "RE" and "SE" fall.

Fig. 11 shows the OS-FF layout. The layout of the original cell is unchanged. The footprint of the cell is unchanged before and after the implementation of the OS-FF; therefore, there is no cell area overhead. The area of the Coretex-M0 core with the original cell was compared by simulation with the area of the Coretex-M0 core with the OS-FF. Given that the area of the Coretex-M0 core with the original cell is 1, the area of the Coretex-M0 core with the OS-FF is 1.03. Consequently, due

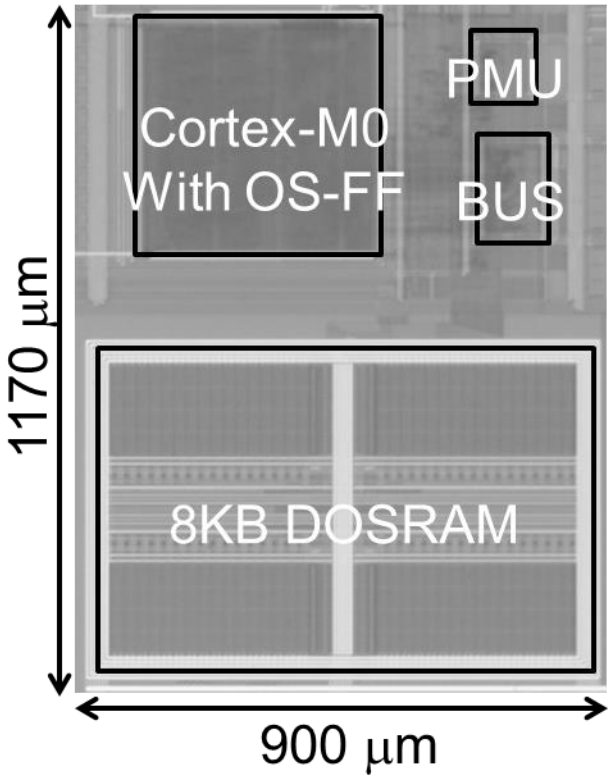

Fig. 12. Die photograph of the fabricated chip.

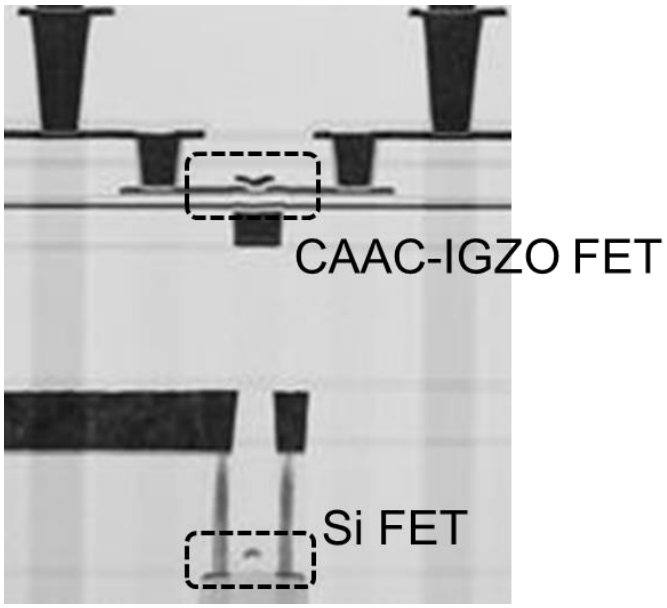

Fig. 13. Cross-sectional image of the fabricated chip.

to the OS process, the SR-FF is fabricated with substantially no operating speed penalty and area overhead.

III. Measurement Results and Discussion

In this section, an overview of the fabricated chip is given, and then, measurement results and the detailed discussion of the chip are presented. Figs. 12 and 13 show a die photograph and cross-sectional image of the fabricated chip, respectively. The Si-FET and wirings up to M2 metal are fabricated by the UMC 65-nm process, and the CAAC-IGZO FET and

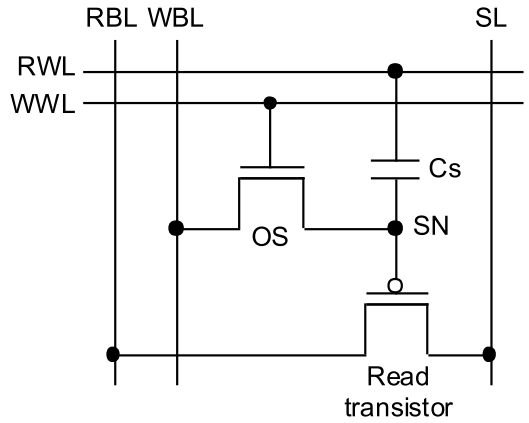

Fig. 14. 1-b CAAC-IGZO memory cell circuit diagram for measuring endurance.

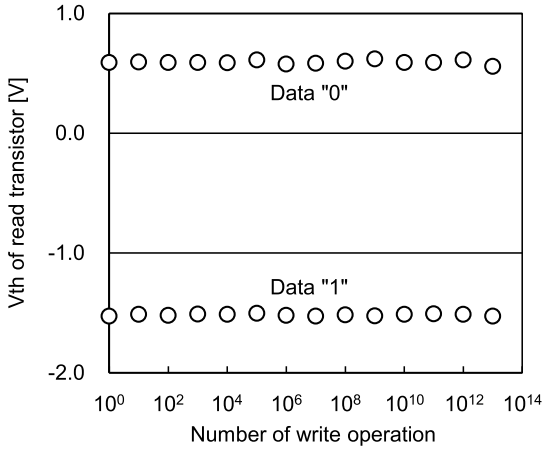

Fig. 15. Endurance of the CAAC-IGZO memory cell.

TABLE I
Operating Mode and Power Consumption of the Chip

	Active (μW/MHz)	Clock Gating (μW)	Power Gating (μW)
Coretex-M0	16.5	11.6	0.006
8KB DOSRAM	11.7	1.43	0.003

other wirings are stacked. There is no significant difference in the characteristics of the Si-FET and the CAAC-IGZO FET between the hybrid process and the original Si or OS process [9].

First, the endurance measurement results of a memory cell are described. Fig. 14 is a circuit diagram of a 1-b memory cell used for the measurement. The storage capacitance is 1.0 fF. The gate voltages (WWL voltages) are 3.3 and 0 V, and the write voltages (WBL voltages) are 1.2 and 0 V. These voltage conditions are the same as those of the chip. The data of the memory cell are judged by the threshold voltage $V_{\rm th}$ of a read p-channel transistor that is obtained by sweeping of RWL while WWL is 0 V. Fig. 15 indicates that the threshold voltages $V_{\rm th}$ of the read transistor for data "0" and data "1" are not changed after data rewriting at least 10^{13} times at room temperature with the WWL pulse width of 5 ns.

Fig. 16 shows the Shmoo plot of the chip including memory operation at room temperature. The chip operated at 30 MHz when the supply voltages of Si and OS were

TABLE II
CHARACTERISTICS OF THE CHIP DEVELOPED IN THIS STUDY COMPARED WITH OTHER TECHNOLOGIES

	ISSCC 2013 [1]	ISSCC 2014 [2]	ISSCC 2015 [3]	Micro 2014 [8]	This work
Technology (Si)	130nm HVT	90nm MVT	90nm SVT, HVT	180nm	65 nm LL
Memory device	FRAM	SpinRAM	N/A	CAAC-IGZO memory	CAAC-IGZO memory
Supply Voltage (V)	1.5	1.0 (VCORE) 1.8 to 3.3 (D_{VCC})	0.72	1.1 (Si) -1.0/3.3 (CAAC-IGZO)	1.1 (Si) 3.3 (CAAC-IGZO)
Clock frequency (MHz)	8	20	16	30	30
Active Power (μW/MHz)	170	145	28.3	225.8	28.2
Standby Power (μW)	0	1.22	0.32	0.05	0.009
100K-cycle in 1sec (μW)	17.00	15.71	3.15	22.63	2.83
10K-cycle in 1sec (μW)	1.70	2.67	0.60	2.31	0.29
1K-cycle in 1sec (μW)	0.17	1.36	0.35	0.28	0.04

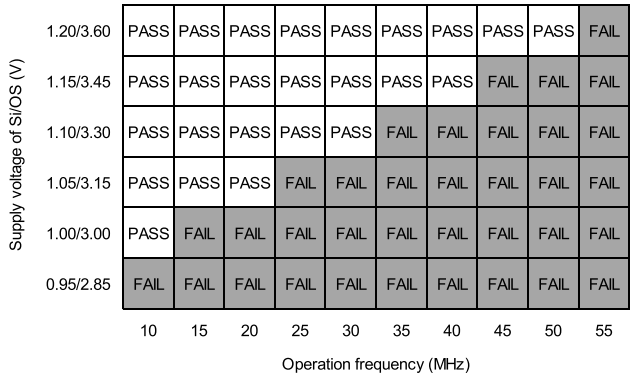

Fig. 16. Shmoo plot of the chip.

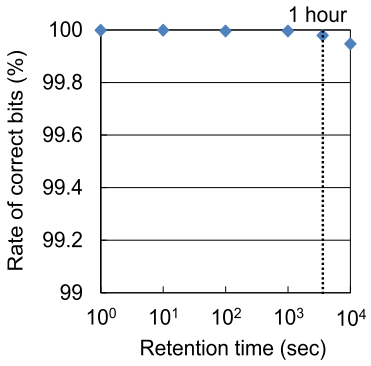

Fig. 17. 8-kB DOSRAM retention characteristics.

1.1 and 3.3 V, respectively. Although the ON-state current of the CAAC-IGZO FET is approximately one-tenth of that of the Si-FET [9], operation at higher than 30 MHz is possible, which is most likely due to the small drive load. For example, the storage capacitance of the DOSRAM is less than half that of the conventional DRAM.

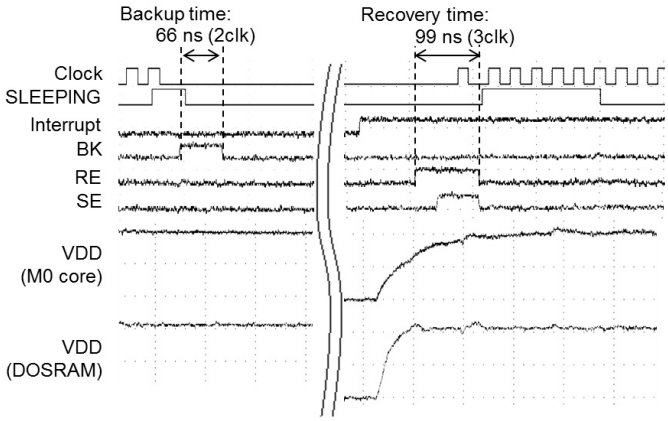

Fig. 18. Waveforms of chip backup and recovery operation.

Fig. 17 shows the 8-kB DOSRAM retention characteristics. The clock frequency is 30 MHz, and the measurement temperature is 85 °C. Retention tests were performed by writing "1" or "0" to all memory cells. The rate of correct bits is 99.995% after retention for 1000 s. If the refresh rate is 1000 s, refresh power is negligible. In other words, unlike DRAM, there is no need to worry about energy loss due to refresh operation even when the memory capacity increases significantly. For commercialization, the rate of correct bits after retention should be 100%. First, it would be interesting to find out how much variation and characteristics could be improved when all processes are performed in a foundry.

Fig. 18 shows the measurement results of power gating the chip at room temperature at a clock frequency of 30 MHz. The core backs up data in two clock cycles and recovers the data in three clock cycles, as shown by the BK and RE signals. Furthermore, as shown in the VDD (Cortex-M0 core) waveform, even after the power is turned OFF, the data can

be recovered correctly at 85 °C even after retention for 1 h. Moreover, as shown in the VDD (DOSRAM) waveform, the power gating operation of the DOSRAM has been confirmed by powering OFF the memory.

The measurement results of power consumption of the chip at room temperature are shown in Table I. To measure the active power, a closed-loop program with nine clock cycles was used. Here, 32-b data were read seven times from the DOSRAM, and 32-b data were written twice to the DOSRAM at 30-MHz clock frequency, and VDD = 1.1 V. The active power of the core and the active power of the 8-kB DOSRAM were 16.5 and 11.7 μW/MHz, respectively. The static power of the core in clock gating and the static power of the 8-kB DOSRAM in clock gating were 11.6 and 1.43 μW, respectively. Static power in clock gating in the DOSRAM is lower than that in the core. This is because the DOSRAM cell has no Si transistors, and thus has no static leakage. The static power of the core in power gating and the static power of the 8-kB DOSRAM in power gating were 6 and 3 nW, respectively. Consequently, power gating drastically reduced the static power.

Table II compares our chip and other low-power MCUs. The clock frequency, active power, and standby power of our chip are superior to the other low-power MCUs. Regardless of whether the active-standby ratio is high or low, this chip achieves the lowest power consumption. For example, assuming that a battery-driven IoT device employs our chip and the chip operates at 10k clock cycles in 1 s, the lifetime of such an IoT device is more than twice as long as those of the previous studies. This indicates that the OS technology enables the fabrication of a broad range of low-power applications.

IV. Conclusion

The DOSRAM as embedded memory and Cortex-M0 core with an OS-FF as an SR-FF were fabricated by a hybrid process, where CAAC-IGZO FETs are stacked on an UMC Si CMOS. Charge in a storage node is retained for a significant period due to the extremely low OFF-state current of the CAAC-IGZO FETs. Therefore, the chip standby power is reduced by power gating of the memory and the core during data retention. Moreover, with the stack structure of the Si CMOS and the CAAC-IGZO FETs, the drive load per bit is reduced. Therefore, the active power of the memory is reduced without any area overhead. The chip with reduced standby power and active power is compatible with a broad range of active standby power ratios, which suggests that this technology would be effective as low-power technology for IoT devices.

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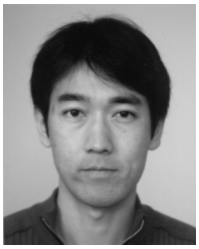

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