A 190-GHz VCO With 20.7% Tuning Range Employing an Active Mode Switching Block in a 130 nm SiGe BiCMOS

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***Abstract*— A voltage controlled oscillator (VCO) incorporating a system of coupled oscillators with two active mode switching (AMS) blocks is presented. The AMS blocks excite the main VCOs to operate in two distinct frequency bands. An overlap between the two frequency bands has extended the tuning range of the VCO. By turning the AMS blocks off, low-loss and low-capacitance behaviors of these blocks result in wide tuning range and high harmonic output power at high millimeter-wave frequencies. On the other hand, by turning the AMS blocks on, their loss-canceling and capacitance-tuning behaviors yield to higher power and wider tuning range with a lower center frequency. By having sufficient frequency overlap between the two modes, the implemented VCO achieves record tuning range of 20.7% at 190.5 GHz with a maximum output power of −2.1 dBm. This tuning range is significantly higher than reported silicon-based VCOs with center frequencies higher than 120 GHz.**

***Index Terms*— BiCMOS integrated circuits, millimeter-wave (mm-wave) integrated circuits, varactors, voltage-controlled oscillators.**

I. Introduction

MILLIMETER-WAVE (mm-wave) and terahertz spectroscopy for the detection of gas molecules requires wideband signal sources [1]. In addition, high frequency radars also demand wideband signal sources for high range resolution [2], [3]. Recently, solid-state circuits have drawn significant attention to develop such signal sources due to their low-cost and compact features. Despite recent advancements in generating high power signal sources on chip [4]–[11], poor performance of the silicon-based devices at high mm-wave frequencies have been a serious obstacle to develop wideband signal sources on-chip. For example, mm-wave voltage controlled oscillators (VCOs) are one of the main blocks for signal generation. However, poor quality factor of the varactors in addition to relatively large parasitic capacitors of transistors compared with the varactors has been limiting the tuning range of silicon-based VCOs. The quality factor of a varactor can be as low as 3 at 100 GHz in a typical 130-nm CMOS process.

In order to remedy the frequency tuning challenges of VCOs at high mm-wave frequencies, Sarmah *et al.* [12] and Lin and Rebeiz [13] have used wideband VCOs at relatively lower frequencies, followed by amplifier and multiplier chain to generate wideband signals at high frequencies. However, this approach demands high power consumption in addition to large chip area. In another approach, Adnan and Afshari [14] and Tousi *et al.* [15] have tuned the frequency at higher frequencies by varying the coupling delay between multiple oscillators. Nonetheless, this approach increases the tuning range by only a few percent. In order to overcome this challenge, Zhang *et al.* [16] has designed an oscillator at lower mm-wave frequencies and extracted the fourth harmonic of the oscillator to reach frequencies around 100 GHz. With this approach, wider bandwidth at high mm-wave frequencies can be covered. Because frequency tuning is done at lower frequencies, achieving wide tuning ranges is typically less challenging. However, output power is relatively low as the extracted harmonic number increases. Despite all the recent efforts, tuning range of silicon-based oscillators has been yet less than 15% in frequencies above 120 GHz. As a result, careful study and unique design of high mm-wave oscillators are demanded in order to develop wideband VCOs at these frequencies.

Mode switching techniques have been widely used at lower RF frequencies to achieve wide tuning ranges [17], [18]. However, these methods are not suitable for mm-wave frequencies. Large parasitic capacitors of the mode-switching devices in addition to their lossy behavior deteriorate the tuning range and oscillation amplitudes at mm-wave frequencies. This paper presents a novel technique to address these issues. By coupling two heterojunction bipolar transistor (HBT)-based Colpitts oscillators and exploiting two novel active mode switching (AMS) blocks, 20.7% of tuning range is achieved at a center frequency of 190.5 GHz. This is a significant increase in frequency tuning among high mm-wave oscillators.

In Section II, we study the unique features of HBT-based Colpitts oscillators and compare it with the MOS-based Colpitts oscillators. In Section III, we propose our novel mode-switching architecture to extend the tuning range much above the existing reported oscillators. Section IV reviews the design features and the experimental results of the implemented oscillator, and finally, Section V summarizes this paper.

II. HBT-Based Versus MOS-Based Colpitts Oscillators for the Core VCO

In order to achieve mode-switching operation, two core VCOs are coupled by two novel AMS blocks. Fig. 1 shows

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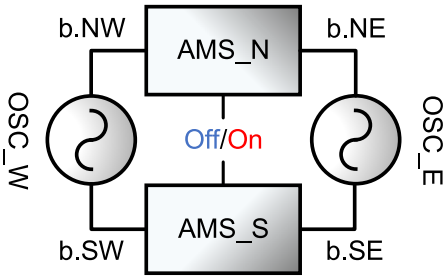


Fig. 1. Block diagram of the proposed mode-switching VCO.

the block diagram of the VCO. By turning the AMS blocks on or off, the mode of oscillation and, thus, center frequency of oscillation changes. In each mode, the two core VCOs, i.e., OSC-West (OSC-W) and OSC-East (OSC-E) in Fig. 1 are responsible for frequency tuning. Therefore, the stand-alone core VCOs should be wideband and have more than 10% of tuning range so that the entire mode-switching system yields more than 20% of tuning range. This requires careful study and design of the core VCOs.

As mentioned earlier, VCO design for tuning ranges more than 10% is highly challenging at high mm-wave frequencies due to the limited quality factor of the varactors. Fig. 2 shows the capacitance and quality factor of an MOS-based varactor in a 130-nm CMOS technology. It clearly shows how quality factor drops with frequency. This makes frequency tuning of oscillators very challenging specially at high frequencies. For $(C_{\max}/C_{\min})$ ratio of 2.4 at 100 GHz, the quality factor varies between 10.2 and 2.9 depending on the biasing voltage, V_{tune}. These low quality factor values at higher mm-wave frequencies necessitate VCO architectures where the loss of varactors does not directly deteriorate tank impedance, while the tuning range remains high at the same time.

Colpitts oscillators are widely implemented using the MOS and HBT transistors [14], [19]. A differential Colpitts structure is shown in Fig. 3. The base inductors resonate with the input capacitors at the bases. These Colpitts oscillators usually have inductive loads at the collectors, because they help with a stronger oscillation [5], [20]. Moreover, degeneration capacitors at emitters are essential components, since they provide required negative conductance at base for oscillation startup [21]. The topology of Fig. 3 has been widely used in SiGe technologies and has shown promising tuning range capabilities at mm-wave frequencies [19], [21]. Varactors can be used as the degeneration capacitors and, thus, contribute to tuning range without lowering the center frequency of oscillation. Moreover, these varactors are not on the harmonic extraction path when extracting harmonic power from the collectors, and hence, harmonic power is preserved. Furthermore, this topology can potentially demonstrate low phase noise performance [19], [22]. Having all these unique features, Colpitts structure has been used as the main topology for the core oscillators of Fig. 1, i.e., OSC-W and OSC-E. In order to achieve the highest possible tuning range in cost effective silicon-based technologies, the 130-nm SiGe and the 65-nm CMOS are compared in the context of Colpitts oscillators.

The equivalent half circuit of the core VCO is shown in Fig. 4. The input capacitor, C_{in}, is one of the significant factors in determining the frequency of oscillation by resonating with the base inductor. In this equivalent circuit, the parasitic base–collector capacitor is neglected for simplicity. Based on Fig. 4, C_{in} can be calculated as

$$C_{\text{in}} = \frac{C_\pi C_{\text{deg}}(C_\pi + C_{\text{deg}})\omega^2}{gm^2 + (C_\pi + C_{\text{deg}})^2\omega^2}. \tag{1}$$

r_π in Fig. 4 is neglected, since its impedance is much higher than C_π at mm-wave frequencies. By replacing C_π by C_{gs}, (1) can also be used for an MOS-based Colpitts structure. In order to achieve a wide frequency tuning range at high mm-wave frequencies, the degeneration varactors at emitter/source of the transistors should be able to alter C_{in}, significantly.

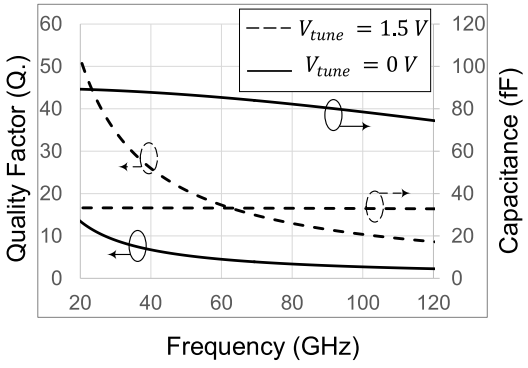
C_π (or C_{gs}) of both the transistors can be approximated by [23]

$$C_\pi \simeq \frac{gm}{2\pi f_t} \tag{2}$$

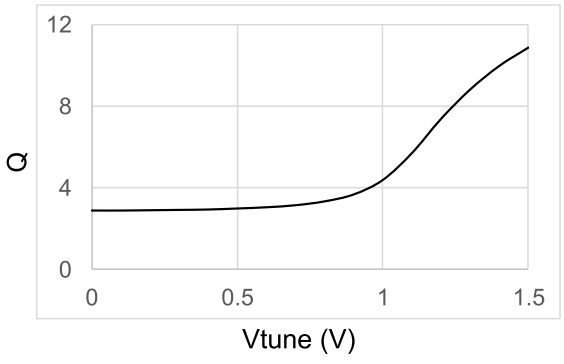
where f_t is the unity current gain frequency of the transistor. To appropriately compare the tuning behavior of the MOS and HBT transistors, we rewrite the value of C_{in} by replacing C_π with $(gm/2\pi f_t)$. Consequently, C_{in} can be derived as

$$C_{\text{in}} \simeq \frac{\frac{gm}{2\pi f_t} C_{\text{deg}} \left(\frac{gm}{2\pi f_t} + C_{\text{deg}}\right) \omega^2}{gm^2 + \left(\frac{gm}{2\pi f_t} + C_{\text{deg}}\right)^2 \omega^2}. \tag{3}$$

The HBT and MOS transistors with the same f_t have different gm values. However, the power consumption of the device can change these values. Table I compares different transistors in different process technologies. In order to have a fair comparison between these technologies, it is assumed that the dc power consumption is similar for these devices. The device sizes are chosen by maximizing f_t for a constant power consumption. Now, assume a varactor with variable capacitance, C_{var} $((C_{\text{var,max}}/C_{\text{var,min}}) = (72/30\ \text{fF}))$ is placed as the degeneration capacitor, C_{deg} at emitter/source of the equivalent circuit in Fig. 4. The device characteristics, such as gm and f_t, are assumed for three parallel transistors for each of the HBT or MOS transistors in Table I. In such case, C_{in} varies between $C_{\text{in,max}}$ and $C_{\text{in,min}}$ for varactor biased at its maximum and minimum capacitance, respectively. The calculated ratio of these maximum to minimum capacitance is shown in Fig. 5 at 100 GHz as a function of gm and f_t of transistors. As illustrated in this graph, $(C_{\text{in,max}}/C_{\text{in,min}})$ is generally higher for larger values of f_t for any given gm and proper choose of varactor sizes. The approximate location of the transistors in Table I is also shown in Fig. 5. It is easy to see that with a similar power consumption, n-p-n HBT transistors in 130-nm SiGe technology have much higher gm and higher f_t than NMOS transistors in 65- and 130-nm CMOS technologies. Therefore, as seen in Fig. 5, wider tuning ranges are expected from HBT transistors. Although the 65-nm NMOS transistor has higher $f_{\max}$ and can sustain oscillation at higher frequencies, it provides lower tuning range in a Colpitts structure, because tuning range is mostly a function of f_t rather than $f_{\max}$. Intuitively speaking, higher gm increases the current flow in the circuit. This increases voltage variation across the varactor; therefore, varactors store more capacitive



(a)



(b)

Fig. 2. (a) Simulated capacitance and quality factor of an MOS-based varactor in a 130-nm BiCMOS technology. (b) Quality factor of the varactor at 100 GHz as a function of Vtune.

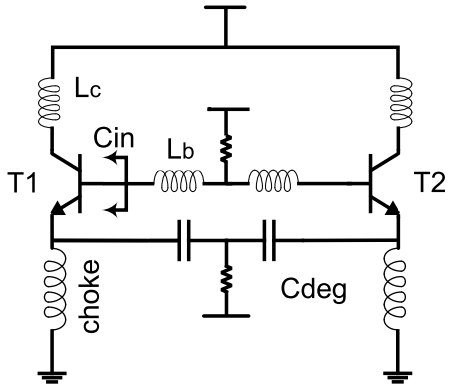


Fig. 3. Differential Colpitts oscillator.

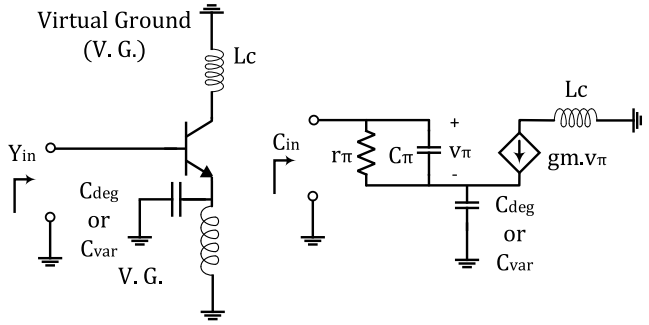


Fig. 4. Equivalent half circuit of a Colpitts oscillator.

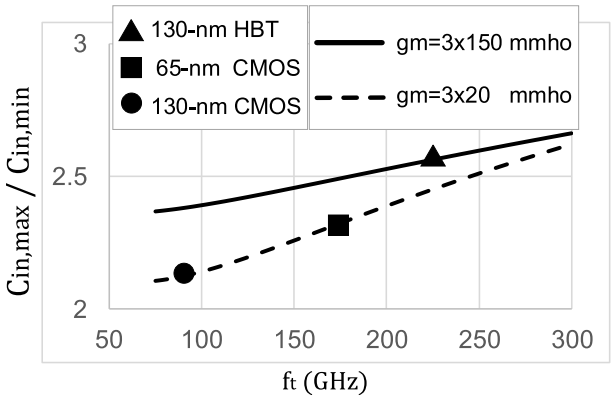


Fig. 5. Ratio of maximum to minimum input capacitance at 100 GHz as a function of f_t for a (72/30 fF) varactor.

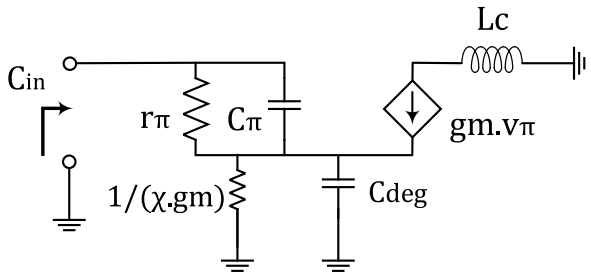


Fig. 6. Equivalent half circuit of a Colpitts oscillator considering the body effect.

energy and they will have more effect on the oscillation frequency.

In addition to higher f_t and gm, HBT transistors lack body effect which is another significant difference between the HBT and MOS transistors. Body factor, χ, is the ratio between bulk transconductance gm_b and gm [23]. χ in HBT transistors is zero, whereas MOS transistors have a nonzero χ. For instance, the 65-nm nFET in Table I has a χ of 0.2. Considering this effect, the equivalent half circuit of a Colpitts oscillator is modified as given in Fig. 6. The input capacitor, C_{in} can be rewritten as

$$C_{\text{in}} \simeq \frac{gm^2\chi(1+\chi)\frac{gm}{2\pi f_t} + \frac{gm}{2\pi f_t}C_{\text{var}}\left(\frac{gm}{2\pi f_t} + C_{\text{var}}\right)\omega^2}{gm^2(1+\chi)^2 + \left(\frac{gm}{2\pi f_t} + C_{\text{var}}\right)^2\omega^2}. \quad (4)$$

Similar gm and f_t values as used in Fig. 5 are used to examine the influence of body effect on tuning range. Fig. 7 shows the ratio of the maximum to minimum of the C_{in} values as a function of χ. This graph clearly shows that as χ increases, $(C_{\text{in,max}}/C_{\text{in,min}})$ decreases. Due to no body effect in HBT transistors, they always operate on the very left side of the plot and have higher tuning ranges as shown in Fig. 7. In a Colpitts structure, χ of the MOS transistors are always nonzero. Therefore, they are not able to operate on the very left side of Fig. 7 and eventually, they will have lower tuning ranges.

Intuitively, in an emitter/source follower circuit, base-to-emitter voltage gain in HBT transistors is higher than

TABLE I
SIMULATED COMPARISON OF THE gm, f_t, AND χ OF DIFFERENT TRANSISTORS WITH SIMILAR POWER CONSUMPTION IN DIFFERENT PROCESS TECHNOLOGIES

Process Technology	size	ft / fmax	DC Power	gm	χ
0.13 μm CMOS	$\frac{30\mu m}{120nm}$ NFET	80 GHz / 145 GHz	7.8 mA x 1.5 V	20.6 mmho	0.2
65 nm CMOS	$\frac{20\mu m}{60nm}$ NFET	170 GHz / 280 GHz	8.3 mA x 1.2 V	21 mmho	0.2
0.13 μm SiGe	$4.7\mu m$ npn	225 GHz / 210 GHz	6.5 mA x 1.5 V	150 mmho	0

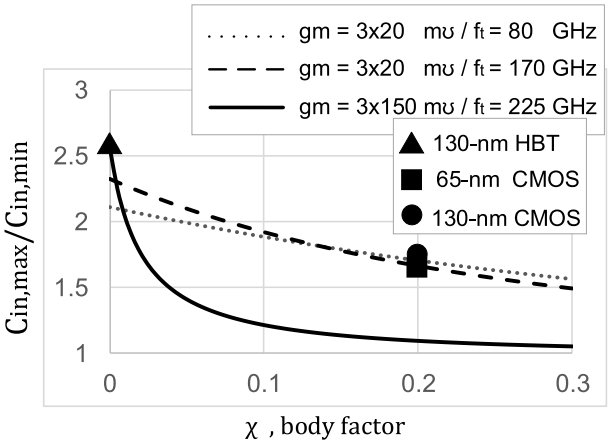


Fig. 7. Ratio of maximum to minimum input capacitance at 100 GHz as a function of χ for a (72/30 fF) varactor.

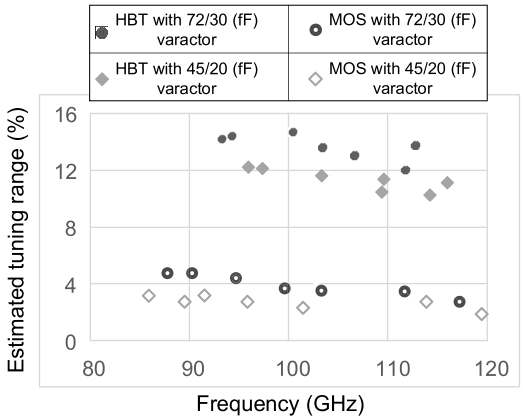


Fig. 8. Simulated tuning range versus center frequency for the HBT-based and MOS-based Colpitts oscillators with different inductor loadings at base/gate and collector/drain. Collector inductor values (L_c) are 20 or 35 pH and base inductor values (L_b) are 12, 20, 30, or 45 pH.

gate-to-source voltage gain in MOS transistors. This is mainly due to the loss that body effect adds to source as shown in Fig. 6. As a result, emitter voltage amplitudes are relatively higher than source voltage amplitudes in typical Colpitts oscillators. This means relatively more electric energy is stored in the emitter varactors compared with the source varactors. As a result, a change in varactor's capacitance in an HBT configuration results in a higher variation in the total reactive energy stored in the circuit. Hence, higher tuning range can be achieved in an HBT configuration than an MOS configuration.

In the above-mentioned analysis, gate–drain capacitor or C_μ was ignored. This parasitic capacitor often increases the C_{in} of the transistor and lowers the tuning range. Moreover, the load at collector changes the loading effect of C_μ on C_{in}. However, the general behavior of tuning range is dominated by f_t, gm, and χ as described. To verify this fact, Fig. 8 compares the simulated tuning ranges of HBT-based and MOS-based Colpitts oscillators of the form of Fig. 3. Three multiples of the same 130-nm HBT and 65-nm CMOS devices in Table I are used in this simulation. This graph marks the tuning range as a function of the center frequency of oscillators with various values of L_b, e.g., 12, 20, 30, and 45 pH and various values of L_c, e.g., 20 and 35 pH. Two sets of varactors with different ($C_{\max}/C_{\min}$) values are also used to see the effect. The simulation results show that significantly wider tuning ranges are achievable with HBT-based Colpitts oscillators. Our additional simulation with even other sizes of MOS transistors and various power consumption did not show tuning ranges more than 6% in the 65-nm CMOS. This difference between the tuning ranges of the MOS-based and HBT-based Colpitts structures can also be traced in some published papers as well [14], [19], [21], [24], [25].

III. PROPOSED MODE-SWITCHING VCO

Two Colpitts oscillators are coupled using two AMS blocks as shown in Fig. 1. The goal for such a system is that the oscillator operates in two modes with distinct center frequencies. This is achieved by the unique design of the AMS blocks. By turning these blocks off or on, the core oscillators; that is, OSC-W and OSC-E operate in-phase (even mode) or out-of-phase (odd mode), respectively. Each of these modes covers a specific bandwidth. By having a frequency overlap between the two modes, a wider tuning range can be achieved.

Circuit-level diagram of the proposed oscillator is given in Fig. 9. The base nodes are named as b.SW, b.SE, b.NW, and b.NE. The AMS blocks are connected directly to these base nodes. Q1, Q2, Q3, and Q4 are used as the core transistors and provide negative conductance to the base inductors. The even mode is excited by turning off the AMS blocks and forcing the two oscillators to operate in-phase. The odd mode is activated by turning on the AMS blocks and making the two oscillators to operate out-of-phase. The block diagram of the VCO in different modes is shown in Fig. 10. The AMS blocks are designed to address the challenges of the parasitic capacitors and lossy behavior of the mode-switching

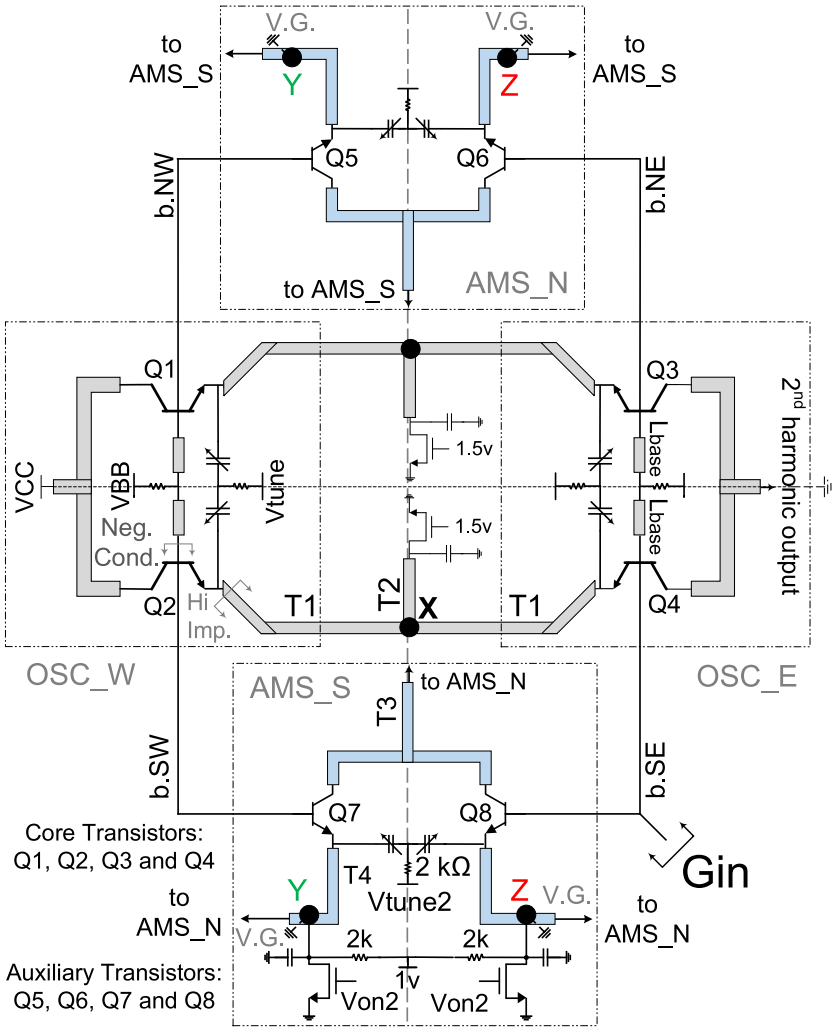


Fig. 9. Circuit diagram of the proposed VCO.

devices in high-frequency VCOs. In the even mode, the AMS blocks load each of the core oscillators with a low-loss and low-capacitance admittance. This results in strong oscillation startup, high harmonic generation, and wide tuning range at the higher frequency mode. In the odd mode, AMS blocks cancel loss in the circuit and contribute to the tuning as well. Consequently, oscillation amplitude and tuning range enhance significantly at the lower frequency mode. Details of the design is covered in Sections III-A and III-B.

A. Even Mode

This mode is aimed to excite fundamental oscillation at the center frequency of 104 GHz. This mode covers the higher frequency band of oscillation than the odd mode, which will be discussed in Section III-B. Even mode is invoked when the AMS blocks are turned off by pulling V_{ON2} to ground. If the two core oscillators, OSC-W and OSC-E, operate in-phase as shown in Fig. 10, the 2-kΩ resistor used to bias the varactors of the AMS block breaks into two 4-kΩ series resistors as shown in the equivalent circuit of the VCO in Fig. 11. Therefore, the core oscillators are not significantly affected by the loss

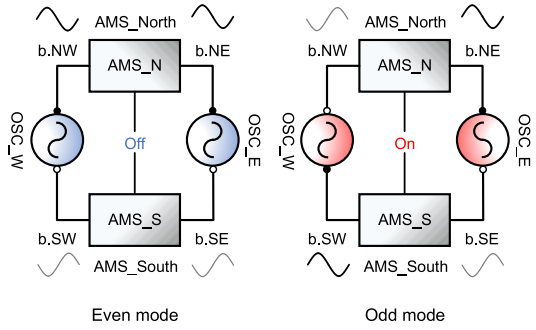


Fig. 10. In-phase or even mode of operation. Out-of-phase or odd mode of operation.

and capacitive loading of the AMS blocks. As a result, this mode can have higher frequency of oscillation than when the oscillation is out-of-phase. In order to ensure in-phase oscillation between OSC-W and OSC-E, the line, T2, is employed at the emitters of Q2/Q4 and Q1/Q3 as shown in Fig. 9. With in-phase oscillation, T2 is shared between the emitters of the core transistors at common mode node X, and therefore,

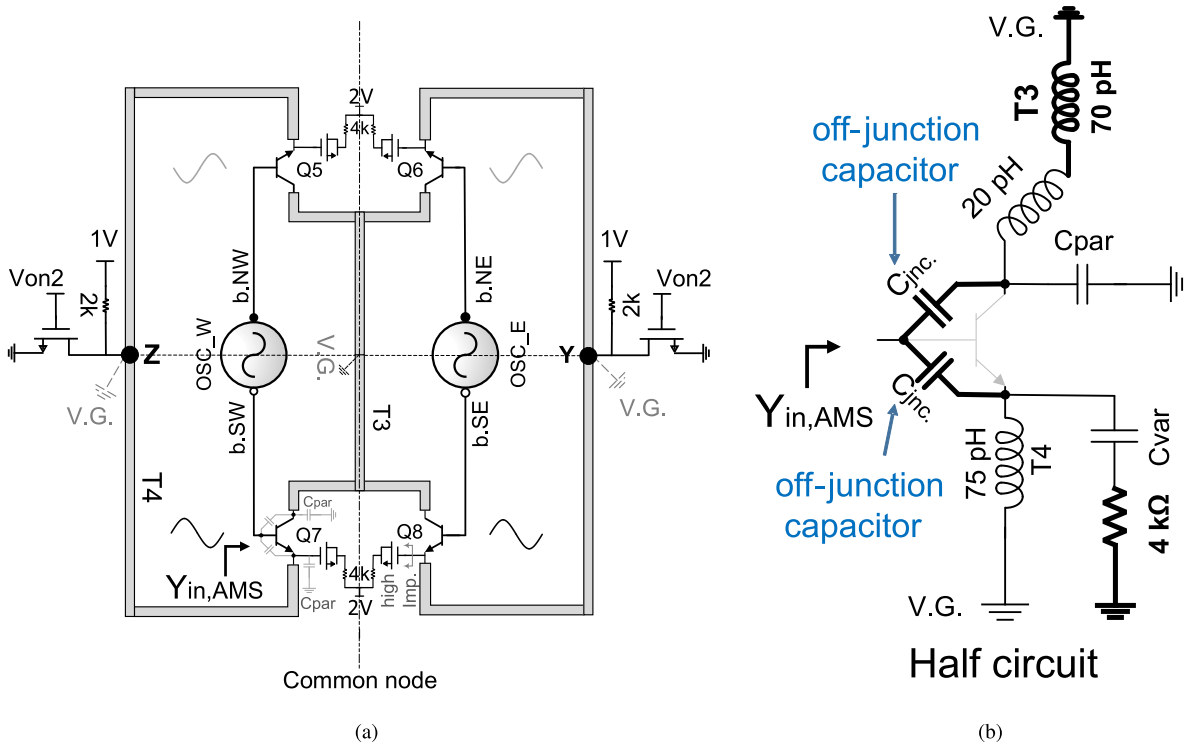


Fig. 11. Equivalent circuit diagram of the VCO in even mode. (a) In-phase operation in even mode. (b) Equivalent half circuit of the AMS block.

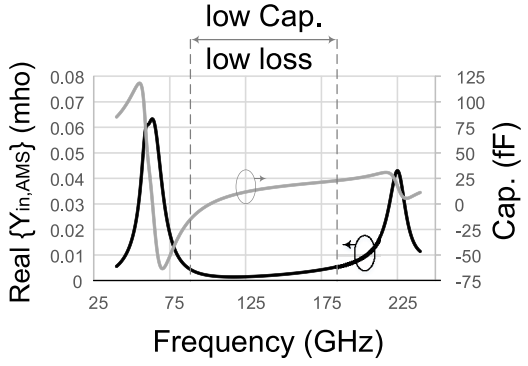


Fig. 12. Input admittance of the AMS blocks in the even mode.

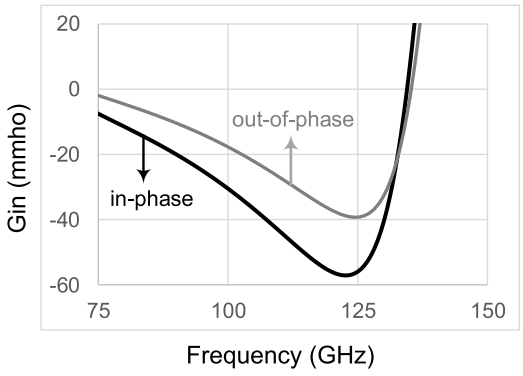


Fig. 13. Total input conductance (G_{in}) of a core VCO and an AMS block when AMS blocks are off.

it increases the impedance of the branch containing T1 and T2. This results in higher negative conductance generation by the core transistors. In this oscillator, only the modes that can compensate more loss in the circuit can survive. Here, in-phase mode of oscillation survives, because this mode has more strength for loss-cancellation.

Q5, Q6, Q7, and Q8 are called auxiliary transistors. Nodes Y and Z shown in Fig. 9 are virtual ground, because Q5 and Q7 are connected to Q2 and Q1 that are oscillating differentially in a Colpitts structure. This is valid in both the modes of operation when the AMS blocks are either on or off. In the even mode, every node on the line of symmetry of the AMS blocks (e.g., vertical dashed line) is common mode node. The varactors in the AMS blocks are not used for tuning in this mode and are biased at their minimum capacitance for minimum loss. This along with large biasing resistors reduces the lossy and capacitive loading of these varactors on the core oscillators. In even mode, V_{ON2} is pulled to ground to turn off the AMS blocks. As a result, the 2-kΩ resistors at the emitters of the auxiliary transistors pull up the bias voltage of the emitters to 1 V, while the bias voltage at the bases of the transistors is near 1.5 V. This leaves a small off-junction capacitor between base and emitter of the auxiliary transistors. This is also the case for the base–collector junction capacitor, since the collector is connected to $V_{\text{cc}} = 2.1$ V. Given the two small junction capacitors, the capacitive and lossy loadings of the AMS blocks are further reduced on the core oscillators. Input capacitance and input conductance of the AMS blocks are further reduced by resonating the parasitic capacitors at the collector of the auxiliary transistors. With in-phase oscillation, T3 is shared between the collectors of Q7/Q8 and Q5/Q6. As a result, effective inductance at the collectors of the auxiliary transistors increases as shown in Fig. 11(b). The total inductor

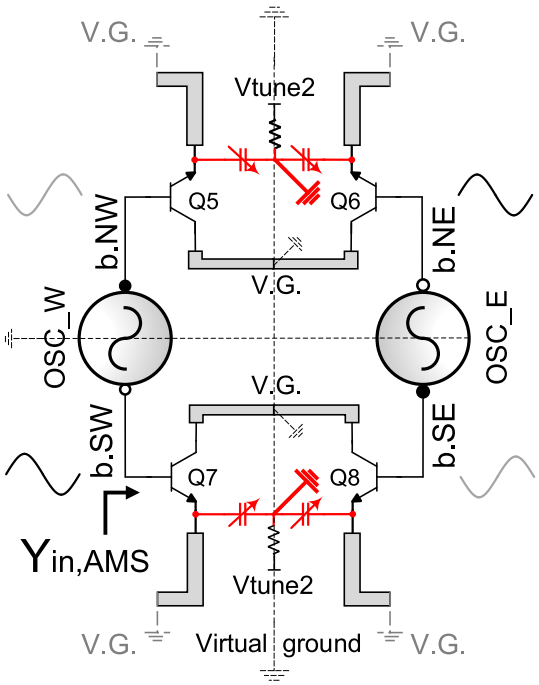


Fig. 14. Equivalent circuit diagram of the VCO in the odd mode.

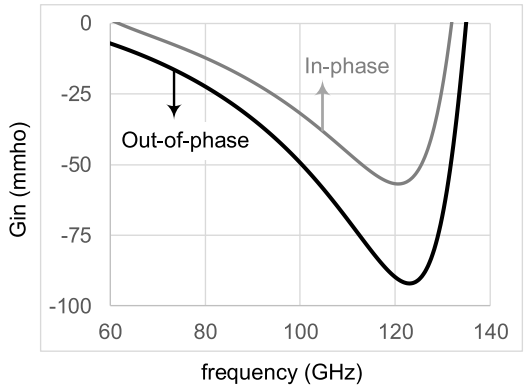


Fig. 15. Total input conductance (G_{in}) when auxiliary transistors are turned on. In-phase operation (black line) versus out-of-phase operation (gray line).

resonates with the parasitic capacitors at the collector nodes of the auxiliary transistors. For in-phase operation, the input admittance of the AMS blocks is low-loss and low-capacitive over a wide frequency range as shown in Fig. 12. The design of the AMS blocks enables the VCO to maintain its strong oscillation for high harmonic power and to maintain its tuning range at higher frequencies as the AMS blocks have negligible loading effect on the main oscillators. Fig. 13 shows the total input conductance of the auxiliary and the core transistors, G_{in}, shown in Fig. 9 (bottom-right). This graph shows that with in-phase oscillation, the absolute value of the input conductance increases. This means stronger negative conductance, and consequently stronger oscillation is achievable.

B. Odd Mode

Odd mode is excited by turning the AMS blocks on. This can be done by setting V_{ON2} in Fig. 9 to 1.5 V. The design goal for this mode is to excite out-of-phase oscillation between OSC-W and OSC-E and achieve fundamental oscillation frequency, centered at 95 GHz, which is lower than the even mode. With out-of-phase oscillation, the common node between the varactors of the AMS blocks becomes virtual ground as shown in Fig. 14. Hence, larger junction capacitors along with the AMS varactors increase the input capacitance of the AMS blocks. This lowers the frequency of oscillation compared with the even mode. Here, we will discuss why by turning the AMS blocks on, out-of-phase operation is enforced and stronger oscillation, i.e., higher oscillation amplitudes are achieved.

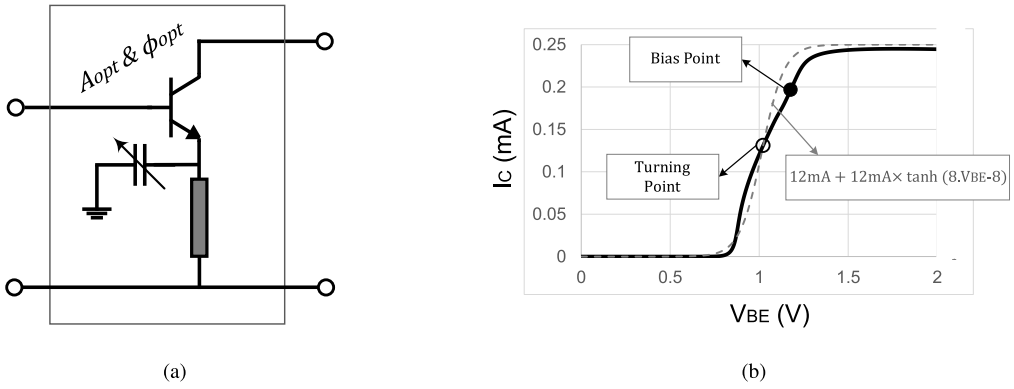
By setting V_{ON2} to 1.5 V and turning on the AMS blocks, the tail current-sources set the biasing voltages at the emitters of the auxiliary transistors and the 2-kΩ resistors can be ignored. The equivalent circuit of the VCO in the odd mode is shown in Fig. 14. If the two oscillators operate out-of-phase, the auxiliary transistors will have degeneration capacitors. This capacitive degeneration results in negative input conductance of the AMS blocks. Fig. 15 compares the total input conductance of a core transistor and an auxiliary transistor when the AMS blocks are in two different modes of operation, i.e., in-phase and out-of-phase. This graph shows that out-of-phase operation has higher negative conductance. Thus, transistors can compensate for more loss in the circuit and out-of-phase operation is enforced. Odd mode consumes more dc power than the even mode but at the same time has larger oscillation amplitudes and higher second harmonic output power.

In this mode, the AMS varactors contribute to the frequency tuning, and hence, wider tuning range is expected, compared with the even mode. The line of symmetry of the AMS blocks (e.g., vertical dashed line) in Figs. 9 and 14 is virtual ground. Hence, the relatively long line, T3, does not load the collectors of the auxiliary transistors anymore. The inductor values at the collector of the auxiliary transistors in addition to the varactor sizes of the AMS blocks control the frequency overlap between the even mode and the odd mode for a continuous tuning range. Degeneration capacitors are the main reason for negative input conductor of the AMS transistors, and consequently, out-of-phase operation in the odd mode.

C. Power Extraction

Fig. 16(a) is used to derive the optimum conditions [4] (i.e., A_{opt} and ϕ_{opt}) for the core transistor, loaded with its varactor and emitter line. For the transistor in Fig. 16(a), optimum condition at the center frequency of this oscillator shows A_{opt} of 1.4 and ϕ_{opt} of 185°. These conditions can be achieved by loading the collector with a proper inductive network. However, tuning range drops by providing the optimum conditions because of the higher Miller effect of C_μ on the input capacitance of the base. Therefore, the collector lines in the core oscillators are designed on a tradeoff between tuning range and optimum conditions so that acceptable tuning range and proper output power can be achieved, simultaneously.

The second harmonic power was extracted only from OSC-E in Fig. 9. Fig. 16 shows the I–V curve of the 16.5-μm transistor used in the core oscillators. This curve can be



(a) (b)

Fig. 16. (a) Deriving optimum conditions for the core transistors. (b) Simulated I–V curve of the core transistors and a tanh function curve-fit.

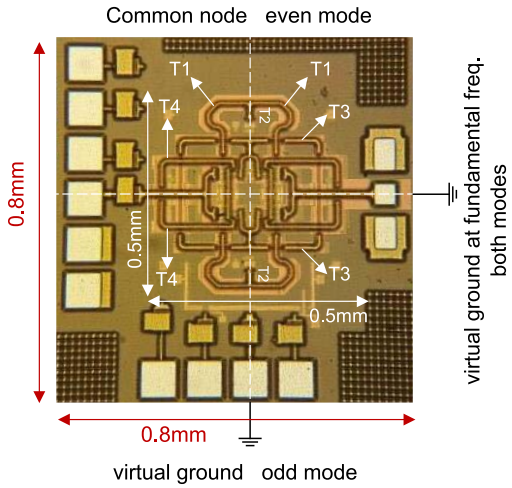


Fig. 17. Chip micrograph.

approximated with a tanh function. This is an odd function around its turning point. Using Fourier theorem, it can be shown that odd functions have no even harmonics with a single-tone input. Hence, if the transistors were biased at the turning point of the tanh curve, the second harmonic generation could be lower. Therefore, the transistors are biased away from this point for sufficient second harmonic power generation. For bias currents below the turning point, there is not enough gain for oscillation startup. On the other hand, large bias currents close to the saturation current of the transistors result in a drop in oscillation frequency because of an increase in the parasitic capacitors of the transistors. Consequently, core transistors are each biased at 20 mA.

IV. Implementation and Experimental Results

The VCO is implemented in a 130-nm BiCMOS technology. This process has seven metal layers total. The R–C extracted HBT transistors up to the fifth metal layer have a simulated $f_{\max}$ of 210 GHz. Three parallel 5.5-μm HBTs are used for the core transistors and two parallel 6-μm HBTs are used for the auxiliary transistor. Wider emitter width for the HBTs was avoided to ensure reliable modeling of the R–C extracted transistors at high mm-wave frequencies. The VCO layout is symmetric vertically and horizontally as shown in Fig. 17. The horizontal line is always virtual ground in both modes, whereas the vertical line is virtual ground in the odd mode only. This assists with a sturdy operation of the two modes. By making use of the virtual ground nodes, some bypass capacitors needed for the dc-decoupling of the AMS collectors were avoided. Furthermore, the bias routings of these collector biasing lines to the pads became cleaner, which minimized any signal coupling between these dc routing lines and other transmission lines in the circuit. Moreover, the 2-$k\Omega$ resistors for emitter biasing of the auxiliary transistors in even mode are located at the virtual ground nodes. This minimizes the loss they add to the oscillator.

The inductors implemented by microstrip lines are shown in Fig. 17. The biasing circuitry of the auxiliary transistors is located at virtual ground nodes in both the modes. The VCO has an area of 0.25 mm^2 excluding the dc pads. The bottom two metal layers were used as ground plane. All the microstrip lines were implemented using the top two metal layers. The distance of the highest metal layer to the ground plane is 12 μm, which helps with a higher Z_0 for the lines. In order to take advantage of the virtual ground nodes, overlaps between T1, T2, T3, and T4 were inevitable. Hence, all the overlaps were implemented orthogonally to minimize the coupling between the lines. All the lines and their overlaps were fully simulated using 3-D Electromagnetic simulator. The auxiliary and the core transistors are biased using nFETs as current sources; 100-fF metal–oxide–metal capacitors were placed in parallel with the MOS current sources of the core oscillators in order to filter the white noise of the current sources around the second harmonic.

Fig. 18 shows the measurement setup. For frequency measurement, signal is picked up by a WR-5.1 probe. The probe is connected to a harmonic mixer. A diplexer feeds the required Local Oscillator to the mixer. The mixer downconverts the signal by the 12th harmonic of the LO. For power measurement, a taper waveguide is used to convert WR-5.1 to WR-10.1, which is suitable for the PM4 power meter by Ericsson.

Measured results for tuning range are given in Fig. 19. Higher tuning range is achieved in the odd mode, since the varactors of the AMS blocks contribute to the tuning range. Mea-

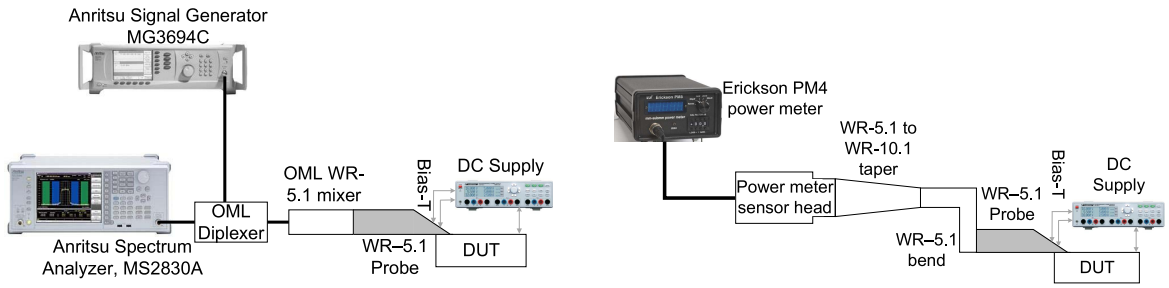


Fig. 18. Measurement setup. (a) Setup for frequency and phase noise measurement. (b) Setup for power measurement.

TABLE II
COMPARISON WITH PRIOR ARTS

Reference	**This Work**	[25]	[27]	[28]	[24]	[29]	[30]
Center Freq. (GHz)	**190.5**	256	239	290	247.5	215	210
Tuning-Range	**20.7%**	6.5%	12.5%	8%	10.9%	0.7%	10.6%
Max. output power (dBm)	**-2.1**	4.1	-4.8	-14	7.2	5.6	1.4
Power Consumption (mW)	**183 / 294**	227	18.5	105.6	386	79	61
DC-to-RF Efficiency (%)	**0.22**	1.14	1.8	0.04	1.36	4.6	2.4
Phase-Noise (dBc/Hz)	**-102.6 @10 MHz**	-94 @1 MHz	-110.9 @10 MHz	-80.3 @1 MHz	-104 @10 MHz	-94.6 @1 MHz	-87.5 @1 MHz
$FOM_T^{(a)}$ (dBc/Hz)	**-171.8 @10 MHz**	-174.8 @1 MHz	-187.7 @10 MHz	-167.3 @1 MHz	-166.7 @10 MHz	-159.1 @1 MHz	-176.5 @1 MHz
Technology, f_{max}	**0.13-μm SiGe 210 GHz**	65-nm CMOS (N/A)	65-nm CMOS (N/A)	90-nm SiGe 315 GHz	55-nm SiGe	65-nm CMOS 265 GHz	0.13-μm SiGe (N/A)
Circuit Description	**mode-switching**	coupled oscillators	single oscillator	single oscillator	VCO+Ampl. +Doubler	single oscillator	single oscillator
Chip Area (mm^2)	**0.64**	0.43	0.18	N/A	N/A	0.08	0.027

$^{(a)}$ FOM_T calculated for the best phase noise at even mode. FOM_T = L[Δf] + 20 log($\frac{\Delta f}{f_0}$.$\frac{FTR}{10}$) + 10 log($\frac{Power}{1mW}$)

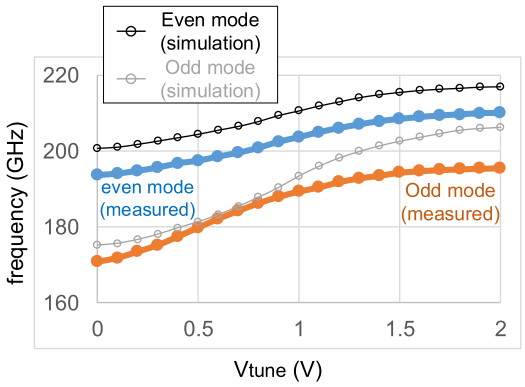
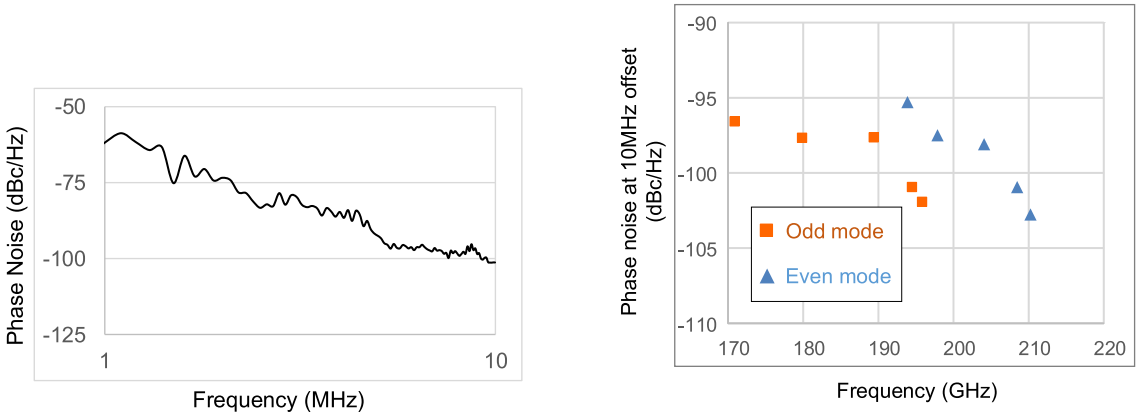


Fig. 19. Simulated and measured frequency tuning range as a function of the varactor bias point in the odd and even modes.

sured results show frequency tuning from 170.8 to 195.6 GHz in the odd mode, which corresponds to 13.6% of tuning range. Due to the unwanted squegging effects [26], we were not able to exploit the full tuning capability of the AMS varactors. Our proposed oscillator has a tail current source with parasitic capacitors. This capacitor along with the large capacitance of the varactors can be the reason for instability in oscillation amplitude known to be the squegging effect. Thus, the measured tuning range in odd mode is less than its simulation. Measured results in even mode showed frequency tuning from 193.5 to 210.1 GHz, which corresponds to 8.3% of tuning range. Measured frequencies have dropped compared with the simulation results. This can be mostly due to the extracted modeling of the transistors at high mm-wave frequencies. By combining the two modes, continuous tuning range of 20.7% at center frequency of 190.5 GHz is measured. Frequency overlap between the two modes is 2.1 GHz to ensure continuous tuning range from the oscillator. Output phase-noise is reported in Fig. 20. Phase-noise performance is better when varactors are biased at their minimum capacitance.

Output power results are shown in Fig. 21. The maximum output power is −2.1 dBm at 194.8 GHz in the odd mode.



(a) (b)

Fig. 20. Phase noise measurement results. (a) Phase noise for the downconverted 210-GHz signal. (b) Measured phase noise at 10-MHz offset as a function of frequency in the odd and even modes.

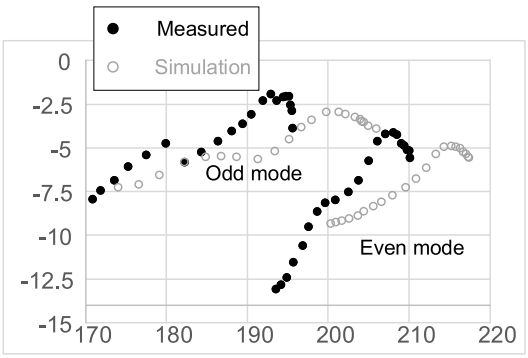


Fig. 21. Measured and simulated harmonic output power as a function of frequency in the odd and even modes.

This mode has more output power in general due to the loss-canceling feature of the AMS blocks. This results in higher oscillation amplitudes and higher harmonic generation. Nevertheless, even mode has acceptable output power owing to the low-loss behavior of the AMS blocks in this mode. Output power in each mode drops as varactors' capacitance increases and their quality factor decreases. Complicated interactive simulations between EM-simulator and circuit simulator were conducted for this design. The extracted s-parameters from the EM-simulator were used in circuit simulator for time-domain/harmonic-balance simulations. The VCO dissipates maximum dc-power of 294 mW in the odd mode and 183 mW in the even mode from a 2.1-V supply. Table II summarizes the performance of this VCO and compares it with related arts. To the best of our knowledge, this paper has the highest reported tuning range among reported VCOs with center frequencies of 120 GHz and higher.

V. Conclusion

A study on HBT-based Colpitts oscillators was presented and compared with MOS-Based Colpitts oscillators. This paper showed that the body effect and cutoff frequency of the transistors have a strong impact on the tuning range of the mm-wave Colpitts oscillators. By coupling two HBT-based Colpitts oscillators and using AMS blocks, a wideband oscillator was presented. By exploiting the virtue of in-phase oscillation, the loss and capacitance of the AMS blocks were reduced, and hence, wide tuning range and high output power were attained in the even mode. On the other hand, when the AMS blocks were turned on, the degeneration capacitors of the AMS blocks reduced the oscillation frequency and led to a better loss-cancellation and capacitance tunability. Thus, stronger oscillation in addition to wider tuning range was achieved in this mode. A small frequency overlap between the two modes brought about the record tuning range of 20.7% at 190.5 GHz.

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