A High Dynamic-Range Neural Recording Chopper Amplifier for Simultaneous Neural Recording and Stimulation

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***Abstract*— Closed-loop neuromodulation is essential for the advance of neuroscience and for administering therapy in patients suffering from drug-resistant neurological conditions. Neural stimulation generates large artifacts at the recording sites, which easily saturate traditional recording front ends. This paper presents a neural recording chopper amplifier capable of handling in-band artifacts up to 40 mV_{pp} while preserving the accompanying small neural signals. New techniques have been proposed that solve the issues of low input impedance and electrode-offset rejection, which enable a DC input impedance of 300 MΩ and a dynamic range of 69 dB (200 Hz–5 kHz) and 78 dB (1–200 Hz). Implemented in a 40-nm CMOS process, the prototype occupies an area of 0.071 mm^2/channel, and consumes 2 μW from a 1.2 V supply. The input-referred noise is 7 μV_{rms} (200 Hz–20 kHz) and 2 μV_{rms} (1–200 Hz). The total harmonic distortion for a 20-mV_p input at 1 kHz is −74 dB. This paper improves the linearity by 14–26 dB, dynamic range by 11–28 dB, and input-impedance for chopped front ends by a factor of 11 as compared with the current state of the art, while achieving similar power and noise performance.**

***Index Terms*— Chopper amplifier, chopper ripple, closed loop, duty-cycled resistor, dynamic range, electrode offset, front end, harmonic distortion, input impedance, large time constants, linearity, low noise, low power, neuromodulation, neural recording, pseudoresistors, servo-loop.**

I. Introduction

RECORDINGS of the electrical activity of neurons have been among the most important tools available in decoding the functioning of the brain [1]. These recordings are indispensable for understanding and diagnosing neurological disorders like epileptic seizures, in the creation of brain–machine interfaces and for neuroprosthetic technologies to aid paralyzed patients [2]–[4]. Though neural recordings are invaluable, neural stimulation is necessary to administer therapy in patients that do not respond to pharmacological treatment [5], [6]. Neural stimulation is performed by sending controlled current pulses into specific regions of the brain to modulate brain activity. Existing stimulation therapies rely on continuous open-loop stimulation. Open-loop stimulation, though useful, can have detrimental effects like mania, depression, apathy, panic, impulsivity, anxiety, and hallucinations [7], [8]. In addition, open-loop stimulation loses its efficacy over time due to plasticity and other changes in the brain, requiring periodic recalibration of stimulation parameters. Hence, neuroscientists aim to perform closed-loop stimulation, where stimulation parameters are adapted in real time using recorded neural signals as feedback. This ensures that stimulation is applied only when necessary and with the required intensity, mitigating the undesirable effects that accompany open-loop stimulation, while maximizing the therapeutic benefits. Feedback also allows the stimulation parameters to track the dynamics of the brain, thus maintaining the therapeutic effects over time. Apart from therapy, a closed-loop neuromodulation system provides neuroscientists with an investigative tool to further explore the workings of the brain. The next generation of neuromodulation systems will require fully implantable devices capable of closed-loop operation with hundreds of recording channels.

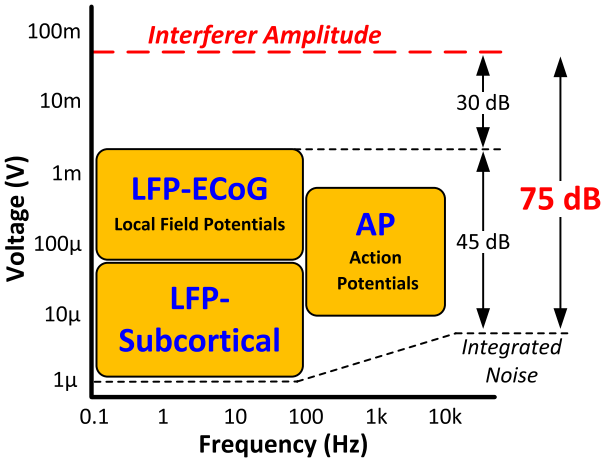

Fig. 1. Amplitude and frequency characteristics of recorded neural signals. The interferer denotes stimulation artifacts.

In a closed-loop neuromodulation system, it is required to simultaneously record neural signals while applying neural stimulation. The neural signals of interest that are recorded by the electrodes occupy a frequency band from 1 Hz to 5 kHz. The various types of neural signals along with their bandwidths and amplitudes are shown in Fig. 1 [2], [8], [9]. The local field potentials (LFPs) and action potentials (APs) have been shown to contain biomarkers that are useful in therapy and basic neuroscience research. The LFPs occupy a frequency

Manuscript received August 14, 2016; revised November 15, 2016; accepted December 21, 2016. Date of publication January 27, 2017; date of current version March 3, 2017. This paper was approved by Associate Editor Azita Emami. This work was supported by the Defense Advanced Research Projects Agency (DARPA) through DARPA's Restoring Active Memory (RAM) Program under Cooperative Agreement N66001-14-4029 issued by SPAWAR contracting office.

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Digital Object Identifier 10.1109/JSSC.2016.2645611

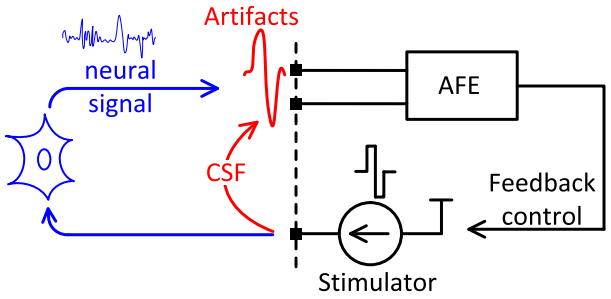

Fig. 2. Simultaneous stimulation and recording leading to artifacts in closed-loop neuromodulation systems.

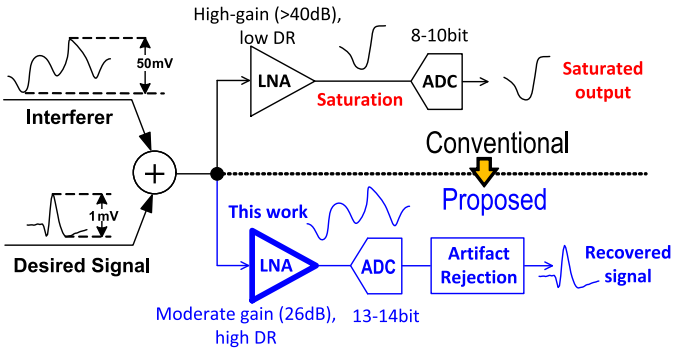

Fig. 3. Comparison of conventional and proposed recording front ends. Conventional front ends use a high-gain LNA with limited DR, which saturates in the presence of artifacts. This paper presents a high-DR LNA with a large linear input signal range to accommodate artifacts.

band from 1 to 200 Hz, and the APs occupy a frequency band from 200 Hz to 5 kHz. The peak amplitude of LFPs is about 1 mV, and the peak amplitude of APs is about 100 μV. The thermal and biological background noise picked up by the electrodes is about 10 μV_{rms}. Thus, a recording front end with 7–8 effective number of bits (ENOB) would suffice to faithfully digitize neural signals. However, along with the desired neural response, stimulation also generates large in-band artifacts at the recording sites, as shown in Fig. 2, due to direct conduction paths from the stimulation sites to the recording sites through the cerebrospinal fluid. These unwanted artifacts can be 10–20 times larger than the neural signals of interest (Fig. 1). The presence of large in-band artifacts at the recording sites poses a big challenge, as the sensing front end needs to maintain the signal integrity of the small neural signals in the presence of large artifacts. For example, to digitize a 1-mV neural signal with 8-b resolution in the presence of a 20-mV artifact, the front end requires a signal to noise and distortion ratio (SNDR) of 12 b. The state-of-the-art implantable recording front ends saturate beyond an input amplitude of $\sim$ 5 mV and have limited linearity, making them incapable of handling stimulation artifacts. Saturation leads to a loss of information, and the recording circuitry may require a long period of time to recover from artifacts. To avoid saturation, some recording systems implement a technique known as blanking [10], [11] where up on the detection of large signals, the front ends are disconnected from the electrodes. Though blanking prevents saturation, the neural signals of interest are lost during the presence of artifacts. In addition, stimulation artifacts could last for several milliseconds or more when burst or periodic stimulation pulses are used, which would result in severe loss of neural recording if blanking is used. Another technique recently published [12] attempts to estimate the artifact using an adaptive filter in the digital domain and cancel the artifact in the analog domain using mixed-signal feedback. Artifact cancellation using feedback would significantly reduce the required dynamic range of the recording front end, but this technique was demonstrated for artifacts less than 3 mV, which is insufficient for closed-loop recording.

To ensure minimal signal loss in the presence of large artifacts, a high dynamic range recording front end is required. Neural recording front ends typically consist of a low-noise amplifier followed by an analog to digital converter (ADC), as shown in Fig. 3. The amplifier gain can be reduced to $\sim$30 dB to prevent saturation for large input signals, but this would require a high-resolution (>12 b) ADC. Low-power ADCs with an ENOB of 13–14 b have been published [13], but to the best of our knowledge, there is no implantable low-power neural recording amplifier that achieves an SNDR of 12–14 b. This paper presents a neural recording chopper amplifier capable of handling up to 40-mV_{pp} in-band artifacts, while maintaining the resolution of the accompanying small neural signals. A large linear input-signal range preserves the neural signals of interest, which can subsequently be extracted in the digital domain by performing adaptive artifact rejection, as shown in Fig. 3.

The rest of this paper is organized as follows. The sensing front-end requirements are discussed in Section II. Section III reviews the current state of the art and summarizes the key advances and shortcomings of the prior work. Section IV presents our sensing front end and highlights the new techniques and design choices used to achieve the requirements outlined in Section II. Measurement results using a fabricated prototype and comparisons with the state of the art are presented in Section V. Section VI concludes this paper.

II. Recording System Requirements

An implantable neural recording system needs to satisfy many design specifications to ensure functionality, patient safety, implantability, and prolonged battery life. The requirement of a high SNDR of 12 b has been explained in Section I. The other requirements have been discussed in [14]–[16], which are summarized here. To support a large number of recording channels, the power consumption of the neural recording front end should be less than 10 μW per channel to avoid tissue damage due to heating [17] and to prolong battery life. The input-referred noise of the recording front end should be 4–8 μV_{rms} for the AP band, and 2–3 μV_{rms} for the LFP band. This agrees with the fact that the background noise picked up by the electrodes is about 10 μV_{rms}. Apart from neural signals and stimulation artifacts, a large dc offset appears at the recording electrodes, which needs to be rejected to prevent saturation. The value of this electrode offset for differential recording from nominally identical electrodes can be up to 50 mV [18]. Thus, a high-pass filter with a corner frequency less than 1 Hz is necessary to preserve the neural

TABLE I

SUMMARY OF THE PERFORMANCE OF THE CURRENT STATE-OF-THE-ART NEURAL AMPLIFIERS, AS COMPARED WITH THE REQUIRED PERFORMANCE FOR CLOSED-LOOP OPERATION

Parameter	JSSC 2003	TBCAS 2007	JSSC 2007	ISSCC 2014	Required
Power (μW)	80	7.6	1.8	2.3	**< 10**
BW (Hz)	7.2k	5.32k	180	300	**1-5k**
Noise (μV_{rms})	2.2	3.06	0.95	1.3	**4-8**
DR (dB)	55	50	66	50	**75**
THD (dB)	–40	–40	–60	–48	**–75**
I/P swing (mV_{pp})	16.7	7.3	10	1	**50**
DC Z_{in} (Ω)	∞	∞	8M	28M	**> 100M**

signals while attenuating the electrode offset. The electrode offset can create dc currents at the electrode due to the finite dc input-impedance of the recording front end. Prolonged presence of dc currents at the electrode has detrimental effects and can cause tissue damage. A dc input impedance larger than 100 MΩ is required, since this limits the dc current to 500 pA for an offset voltage of 50 mV, which is sufficiently low for most applications [19]. In addition, the input impedance in the frequency range of interest (1 Hz–5 kHz) needs to be much larger than the Thevenin impedance of the electrode to prevent signal attenuation. The maximum impedance of the electrode corresponds to a capacitance of 5 nF [20], [21]. The requirements for a neural recording front end capable of being used in a closed-loop system are summarized in Table I.

III. REVIEW OF CURRENT STATE OF THE ART

There have been a large number of publications in the past two decades on neural signal recording front ends. The capacitively coupled inverting amplifier [Fig. 4(a)] is among the most popular topologies used [14], [22]–[25]. Capacitive coupling ensures a large dc input impedance, and sizing the input capacitance smaller than 100 pF ensures negligible signal attenuation at the electrode. This topology has been optimized for power and noise, as discussed in [14]. The input devices are sized to have a large area to minimize their flicker noise contribution. To achieve low-frequency high-pass corners, pseudoresistors are used [14], as they are an area-efficient way to realize very-low frequency high-pass corners. However, pseudoresistors are very nonlinear, and since they experience the full output swing V_{out}, they limit the linearity of the front end to about 8 b [24]. Pseudoresistors are also very sensitive to process and temperature variation, as their resistance can vary by a factor of 100. In addition, any bulk leakage currents in the pseudoresistor can create large dc bias shifts, leading to poor control of bias points in the front end. These issues make the pseudoresistor unreliable in a clinical setting [19].

The chopper-stabilized amplifier [Fig. 4(b)] is another popular front-end topology for neural recording [18], [26]–[28], as chopping is an effective way to mitigate the low-frequency

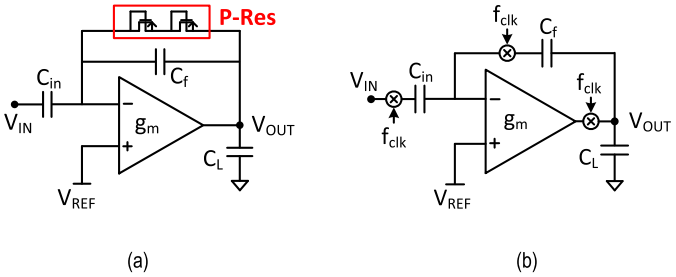

Fig. 4. Popular topologies for neural recording amplifiers. (a) Capacitively coupled amplifier with pseudoresistors. (b) Chopper amplifier with capacitive feedback.

flicker noise of the opamp. A servo-loop is usually employed Fig. 5(a) to attenuate the electrode offset at the output V_{out}, thus creating the required high-pass filter. However, chopping reduces the dc input impedance, since the passive mixer at the input along with the capacitance C_{in} [Fig. 4(b)] forms a switched-capacitor resistance. For C_{in} of 10 pF and f_{clk} of 20 kHz (typical values for this application), the dc input impedance is limited to 2.5 MΩ, which is significantly lower than the required 100 MΩ. Off-chip coupling capacitors can be used to increase the dc input impedance [29], but they become impractical for a miniaturized implant with a large number of recording channels. To boost the input impedance, a positive-feedback loop Fig. 5(b) has been used in [26]. The positive feedback path provides the required dc current to the switched-capacitor resistor at the input, which otherwise would have been supplied by the electrodes, thus boosting the dc input impedance to infinity. However, the positive feedback loop is sensitive to parasitic capacitance appearing at node n1 [denoted by C_{bp} in Fig. 5(b)], which limits the realized impedance boost to a factor of 5 as opposed to the targeted boost of a factor of 100 in [26]. Another critical problem with this technique is that the positive feedback loop is driven by the output V_{out}. Any practical neural recording front end would attenuate the dc signal at the output V_{out}. Thus, the positive feedback loop is rendered inoperative at dc, where it is most needed.

The current state of the art in neural recording is summarized in Table I. The state of the art has successfully met the power and noise requirements, but there is a significant performance gap in linearity, dynamic range, and input impedance.

IV. HIGH DYNAMIC-RANGE NEURAL RECORDING CHOPPER AMPLIFIER

The proposed chopper stabilized neural recording amplifier is shown in Fig. 6. It is capable of recording large signals with high linearity, high dc input impedance, and simultaneous electrode offset filtering [30]. The problems of low-frequency high-pass filtering without pseudoresistors and the upmodulated chopper ripple are also addressed. The positive-feedback loop is included in this paper to compare its performance to our input impedance boosting technique, which will be discussed later in this section. The core of the chopper amplifier consists of a two-stage opamp, labeled as g_{m1} and g_{m2} in Fig. 6, with the demodulation mixer placed before the second stage.

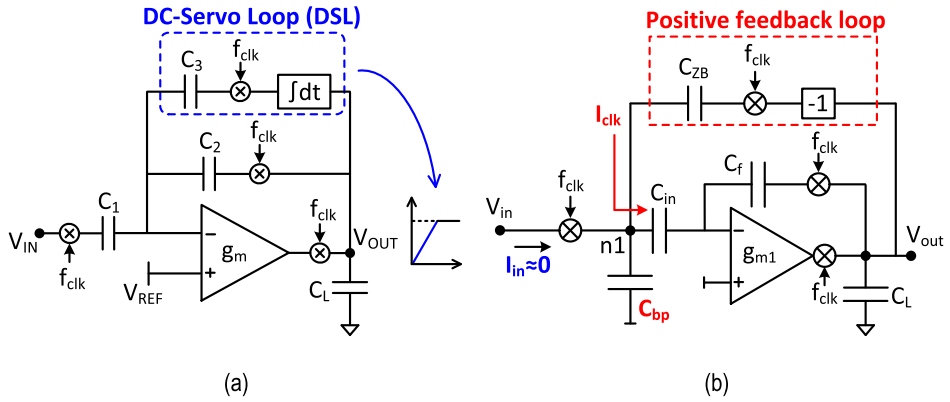

Fig. 5. (a) Servo-loop to create a high-pass transfer function. (b) Positive feedback to boost the input impedance of a chopper amplifier.

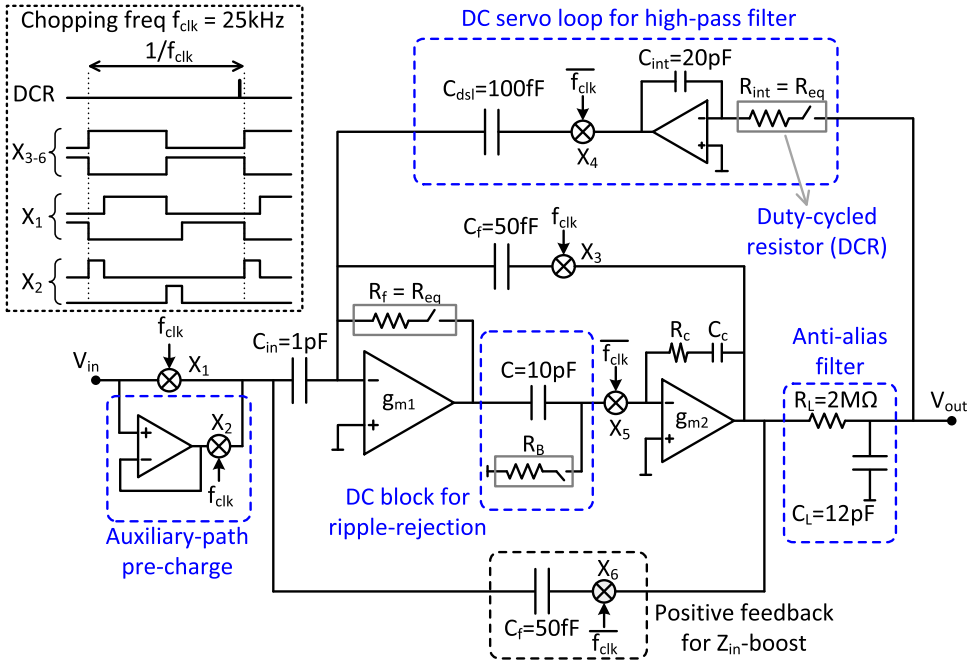

Fig. 6. Complete implementation of the proposed chopper amplifier, with mixer and DCR-clock waveforms shown (top-left). Single-ended version shown for simplicity, fully differential version was implemented.

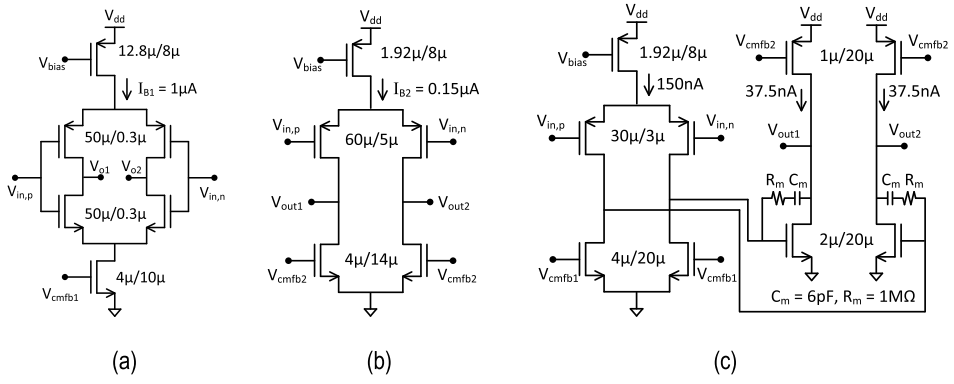

Fig. 7. Schematic of (a) transconductor g_{m1}, (b) output stage g_{m2}, and (c) servo-loop-integrator opamp used in the proposed chopper amplifier.

The schematics of g_{m1} and g_{m2} are shown in Fig. 7. The bias currents of g_{m1} and g_{m2} are 1 and 0.15 μA, respectively. Miller compensation is implemented to ensure closed-loop stability. The midband gain is set by the ratio of capacitors C_{in} and C_f, which are set to 1 pF and 50 fF, respectively, setting the midband gain to 20.

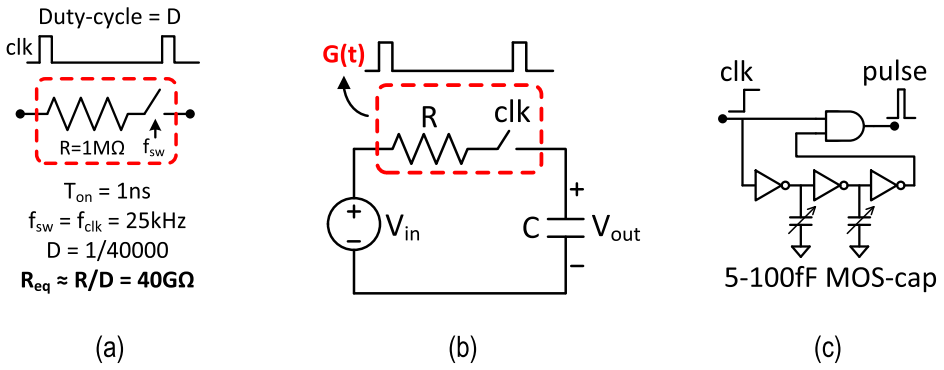

Fig. 8. (a) Concept of a duty-cycled resistor to realize a large resistance. (b) Low-pass filter using a duty-cycled resistor. (c) Programmable pulse (1–15 ns) generator to drive duty-cycled resistor switches.

A. DC Servo-loop

The dc servo-loop is a negative feedback loop that attenuates low-frequency signals at the output V_{out}. To achieve high loop gain at low frequencies, a low-bandwidth integrator is used in the servo-loop [Fig. 5(a)]. The capacitor C_{dsl} is kept small to reduce the in-band noise contribution of the servo-loop integrator and g_{m1} [18]. The minimum value of C_{dsl} is limited by the maximum electrode offset that needs to be attenuated [26]. C_{dsl} is chosen to be $C_{\text{in}}/10$, which is sufficient to attenuate differential electrode offsets up to ±50 mV. For a high-pass corner frequency of f_{HP} in the signal transfer function $V_{\text{out}}/V_{\text{in}}$, the unity-gain bandwidth of the servo-loop integrator is given by $f_{\text{dsl,ugb}} = f_{\text{HP}}(C_{\text{f}}/C_{\text{dsl}})$. Hence for f_{HP} of 1 Hz, the servo-loop unity-gain bandwidth should be 0.5 Hz. As discussed in Section III, pseudoresistors are not viable in a closed-loop neural recording application. To realize such low corner frequencies in a reasonable chip area, switched-capacitor techniques [31] have been used in the prior work [26]. However, switched-capacitor integrators significantly increase the noise of the recording front end. When the servo-loop was enabled in [26], the measured input-referred noise increased from 0.7 to 6.7 μV_{rms} in the band of 0.5–100 Hz. The wideband noise of the opamp and switches used in the switched-capacitor integrator gets aliased down to baseband, which results in a large in-band noise contribution from the servo-loop integrator. Hence, switched-capacitor integrators, though an effective way to realize low-frequency corners in a small chip area, prove to be detrimental to the noise performance of the recording front end.

In this paper, we propose to use duty-cycled resistors [30], [32], [33] to realize very-low bandwidth integrators. The following analysis shows that the duty-cycled resistors are an effective way to realize large linear resistors in a small chip area. Since duty-cycled resistors are inherently time varying, the analysis needs to account for frequency translations and aliasing effects. A duty-cycled resistor, shown in Fig. 8(a), consists of a passive poly-resistor placed in series with a switch. When the switch is driven by a clock with a duty-cycle factor of D, then the average resistance observed across the terminals is given by R/D. This can be shown by analyzing the circuit in Fig. 8(b). If G(t) is the time-varying conductance of the duty-cycled resistor, then using KVL,

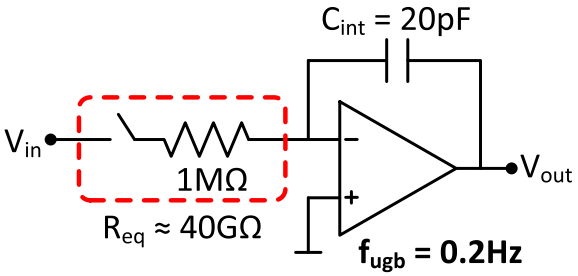

Fig. 9. Opamp-based integrator realized using duty-cycled resistors.

the behavior of the circuit in Fig. 8(b) can be described as

$$V_{\text{in}}(t) \cdot G(t) = V_{\text{out}}(t) \cdot G(t) + C\frac{dV_{\text{out}}}{dt}. \tag{1}$$

To get meaningful insight, we move to the frequency domain. The Fourier transform of G(t) is given by $G(j\omega) = \sum_{k=-\infty}^{\infty} g_k \delta(\omega - k\omega_o)$, where $g_o = D/R$ and $g_k = (1/|k|R\pi) \cdot \sin(Dk\pi)$ are the Fourier coefficients corresponding to the waveform G(t). Hence, taking the Fourier transform of (1) leads to the following:

$$g_o V_{\text{in}}(j\omega) + \sum_{\substack{k=-\infty \\ k\neq 0}}^{\infty} g_k V_{\text{in}}(j(\omega - k\omega_o))$$
$$= (g_o + j\omega C)V_{\text{out}}(j\omega) + \sum_{\substack{k=-\infty \\ k\neq 0}}^{\infty} g_k V_{\text{out}}(j(\omega - k\omega_o)). \tag{2}$$

We use two assumptions to simplify (2). If RC ≫ DT, where T is the period of the clock driving the switch in Fig. 8(b), then $V_{\text{out}}(\omega)$ is a low-frequency signal and the last term in (2) can be approximated to zero. Assuming that $V_{\text{in}}(\omega)$ is a low-frequency signal, $V_{\text{in}}(\omega - k\omega_o)$ can be neglected for $|\omega| > \omega_o/2$. Since $g_o = D/R$, (2) can be simplified to

$$\frac{V_{\text{out}}}{V_{\text{in}}}(j\omega) = \frac{1}{1 + j\omega C\frac{R}{D}}. \tag{3}$$

Equation (3) shows that if the two abovementioned assumptions are true, then the circuit in Fig. 8(b) is identical to a

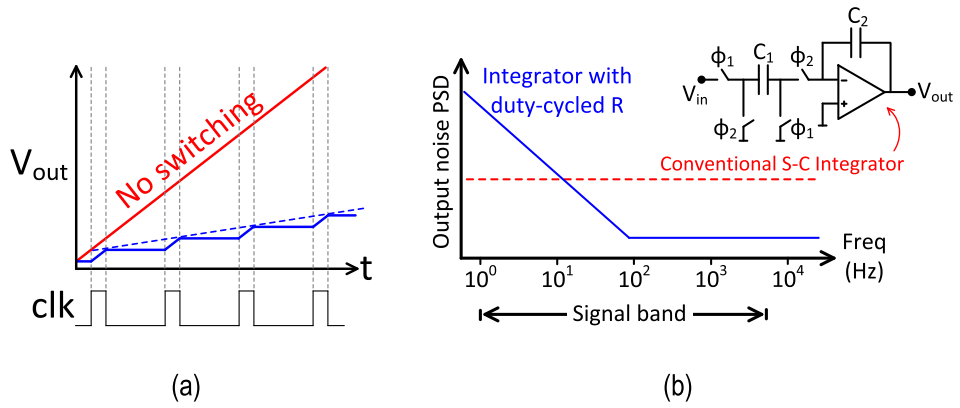

Fig. 10. (a) Step response of the integrator shown in Fig. 9. (b) Typical output thermal noise PSD of low unity-gain bandwidth integrators.

low-pass filter formed by a capacitor C and an equivalent resistor R/D. Thus, the resistance R is boosted by a factor of 1/D. A simple antialiasing filter can be used before the integrator to satisfy the assumption of $V_{\text{in}}(\omega)$ being a low-frequency signal, as shown in Fig. 6. With a pulse width of a few nanoseconds, and for a sampling clock frequency of 25 kHz, it is possible to achieve duty-cycle factors of 1/20 000. Such small duty-cycle factors also ensure that the assumption of $RC \gg$ DT is satisfied. Hence, a 1-MΩ poly-resistor can be boosted to 20 GΩ. Poly-resistor resistance can vary by 25% across process corners. A pulse generator, as shown in Fig. 8(c), can be used to realize pulse widths of a few nanoseconds, with a pulsewidth variation less than 10% across process corners. Thus, the overall variation of duty-cycled resistors is 35%, as compared to 100 times variation for pseudoresistors. Hence, duty-cycled resistors are a more reliable method to realize large resistors. Since the poly-resistor is inherently linear, the duty-cycled resistor achieves high linearity. By using variable capacitor loads in the pulse generator, the duty-cycle factor can be varied by a factor of 10, which translates to a 10 times variation in the equivalent resistance, or a 10 times variation in the corner frequency.

Since Fig. 8(b) is a switched-capacitor circuit, it may suffer from the same noise degradation due to aliasing as seen in conventional switched-capacitor integrators. Hence, it is essential to analyze the noise contribution of this circuit. The noise power spectral density (PSD) of the resistance R is given by 4 kTR V^2/Hz. Since the input V_{in} is now a wideband noise signal, (3) is not valid, and (2) can be written as

$$\sum_{k=-\infty}^{\infty} g_k V_{\text{in}}(j(\omega - k\omega_o)) = (g_o + j\omega C)V_{\text{out}}(j\omega). \quad (4)$$

The frequency-translated versions of $V_{\text{out}}(\omega)$ are approximately zero if $RC \gg$ DT. The left-hand side of (4) represents the resistor noise $V_{\text{in}}(t)$ multiplied with $G(t)$, and the right-hand side represents the result of $V_{\text{out}}(t)$ being passed through a filter with a frequency response of $g_o + j\omega C$. Hence, (4) can be simplified to the following:

$$4kTR\left(\sum_{k=-\infty}^{\infty} g_k^2\right) = |g_o + j2\pi f C|^2 V_{\text{out}}^2(f) \quad (5)$$

where $V_{\text{out}}^2(f)$ is the output noise PSD. Since $\sum g_k^2 = D/R^2$, (5) further simplifies to

$$V_{\text{out}}^2(f) = \frac{4kT\frac{R}{D}}{\left|1 + j\omega C\frac{R}{D}\right|^2}. \quad (6)$$

Thus, (6) shows that the output noise PSD of the circuit in Fig. 8(b) is identical to an RC low-pass filter, with capacitance of C and resistance of R/D. The integrated noise $\int V_{\text{out}}^2(f)df$ is equal to kT/C, which is similar to the noise of a switched-capacitor integrator. However, the noise PSD given by (6) is predominantly confined to frequencies below the corner frequency $D/(2\pi RC)$. Thus, by setting the corner frequency 3–4 times lower than 1 Hz, the noise contribution in the neural signal band (1 Hz–5 kHz) is negligible.

The duty-cycled resistor is used to realize a low unity-gain bandwidth integrator, as shown in Fig. 9. With an integration capacitor C_{int} of 20 pF, and $T_{\text{ON}} = 1$ ns, f_{HP} is set to 0.4 Hz.Though the signal transfer function analysis and noise analysis were performed on the circuit shown in Fig. 8(b), the results directly translate to the integrator shown in Fig. 9. Thus, the integrator in Fig. 9 behaves identical to an integrator with a resistor of R/D. The opamp used to realize this integrator is shown in Fig. 7(c). The step response of the integrator is shown in Fig. 10(a) when the duty-cycled resistor is driven with a dc signal and a clock, respectively. The slope of the step response is significantly lowered when the duty-cycled resistor is driven with a clock as compared with a dc signal, which shows the reduced unity-gain bandwidth as predicted by (3). The output thermal noise PSDs of low unity-gain bandwidth integrators are shown in Fig. 10(b). The plot shows that an integrator implemented with duty-cycled resistors has large noise contribution below the signal band of interest, but the in-band noise contribution is significantly lower than a conventional switched-capacitor integrator.

B. Auxiliary Path for Boosting Input Impedance

The input branch of the chopper amplifier is redrawn in Fig. 11(a). For a dc input V_{in}, the current supplied by the input voltage source is shown in Fig. 11(b). The charge supplied in one period of the chopping clock f_{clk} is $Q = 2C_{\text{in}}V_{\text{in}}$. Hence, the dc input impedance is given by $Z_0 = 1/(2C_{\text{in}}f_{\text{clk}})$. For C_{in}

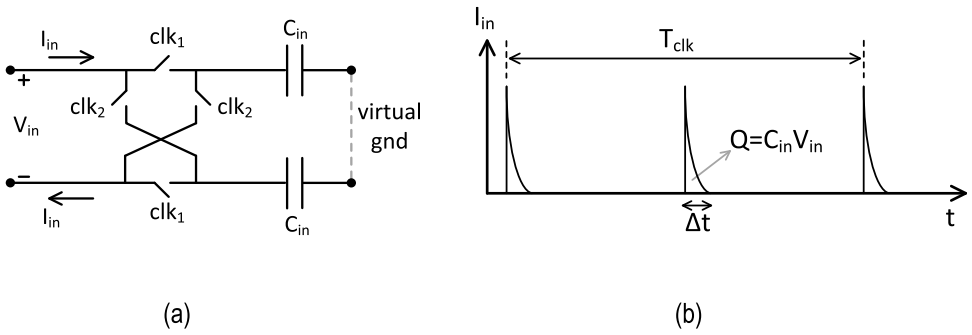

Fig. 11. (a) Input branch of the chopper amplifier. (b) Waveform of the current I_{in} provided by a dc input V_{in} in (a).

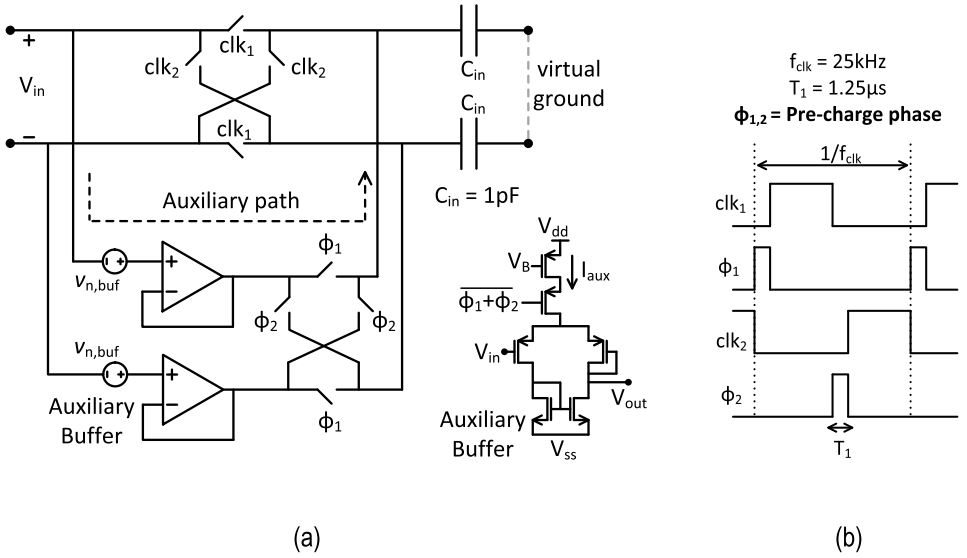

Fig. 12. (a) Auxiliary path precharge technique to boost the input impedance of a chopper amplifier. (b) Control signal waveforms for the auxiliary path technique.

of 1 pF, and a chopping clock frequency f_{clk} of 25 kHz, the dc input impedance Z_0 is 20 MΩ. Fig. 11(b) shows that the input voltage source V_{in} provides charge in a narrow region of time, labeled as Δt. If an alternate reservoir of charge could be used to supply charge to the input capacitors C_{in} for the duration Δt, then the dc current provided by V_{in} is reduced to zero, boosting the dc input impedance to infinity. This concept [36], [37] is realized as a circuit in Fig. 12(a), with the control waveforms shown in Fig. 12(b). At the beginning of every chopping phase, denoted as the precharge phase $\varphi_{1,2}$, the input capacitors are precharged to the input voltage V_{in} through buffers in an auxiliary path. At the end of the precharge phase, the input capacitors are reconnected back to the input port. Since the capacitors C_{in} have been charged to V_{in}, there is no charge flow when the capacitors are reconnected to the input port. Thus, the dc current provided by V_{in} is reduced to zero, boosting the dc input impedance to infinity. However, due to finite gain and finite bandwidth of the auxiliary buffer, a nonzero error is made during the precharge phase. If the auxiliary buffer bandwidth is τ^{-1} rad/sec, and the precharge duration is T_1 sec, then the error made in the precharge phase ΔV is given by

$$\Delta V \approx 2V_{\text{in,DC}} \cdot \left[\alpha + \exp\left(-T_1/\tau\right)\right] \tag{7}$$

where α is the gain error of the auxiliary path buffer. Hence, at the end of the precharge phase, due to the error ΔV, the input V_{in} has to provide some residual charge required by C_{in}. The input impedance is now given by

$$Z_{\text{in,DC}} = \frac{1}{2C_{\text{in}} f_{\text{clk}}} \left(\frac{1}{\alpha + \exp\left(-T_1/\tau\right)}\right) = Z_O \cdot \frac{\exp\left(T_1/\tau\right)}{1 + \alpha \exp\left(T_1/\tau\right)}. \tag{8}$$

As an example, assuming that T_1 is large enough for 1% settling, and if the dc gain of the opamp used in the auxiliary buffer is 30 dB (both being reasonable assumptions), then from (8), the dc input impedance is boosted by a factor of 25. Thus, the dc input impedance of 20 MΩ can be boosted to 500 MΩ by employing the auxiliary path.

The power consumption of the auxiliary buffers [Fig. 12(a)] and the precharge time T_1 can be determined as follows. Let the auxiliary path duty-cycle factor $T_1/(0.5T_{\text{clk}})$ be denoted by d_{aux}. Also, let the bandwidth of the auxiliary buffers allow for k time constants of settling in the precharge phase. Thus, the bandwidth of the auxiliary buffers τ^{-1} is given by k/T_1. Let I_{aux} be the current consumed by each buffer during the

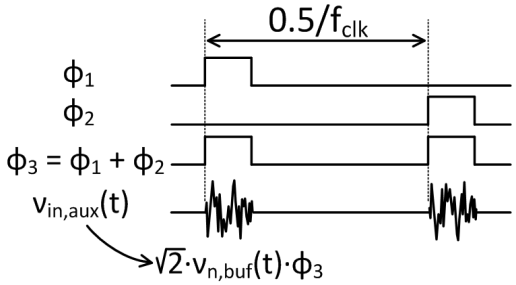

Fig. 13. Input-referred noise contribution of the auxiliary path buffers.

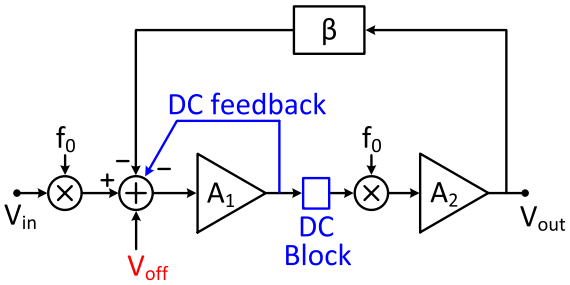

Fig. 14. Ripple-rejection implementation without using additional active elements [34].

precharge phase. To reduce power consumption, the auxiliary buffer bias currents are disabled in-between precharge phases. Assuming that the input devices of the auxiliary buffers are biased in weak inversion, i.e., $g_{m,\text{aux}}/I_{\text{aux}} \approx 25$, then the total dc current consumed by both auxiliary buffers is given by

$$I_{\text{aux,DC}} = \frac{8kC_{\text{in}}}{25T_{\text{clk}}}. \tag{9}$$

For $C_{\text{in}} = 1$ pF, $f_{\text{clk}} = 25$ kHz, and 6τ settling, (9) gives $I_{\text{aux,DC}} = 48$ nA, which is negligible.

The noise contribution of the auxiliary buffers is determined as follows. The noise PSD of the auxiliary buffers in the precharge phase is denoted by $v_{n,\text{aux}} = \sqrt{2}\cdot v_{n,\text{buf}}$, as shown in Fig. 12(a). Since the auxiliary buffer noise is duty cycled when referred to the input, as shown in Fig. 13, the contribution to the input-referred noise PSD is given by $v^2_{\text{in,aux}} = d_{\text{aux}}(v^2_{n,\text{aux}})$. By ensuring that $v^2_{in,aux}$ is 10 times lower than the noise PSD of the first opamp stage g_{m1}, the auxiliary path noise contribution can be made negligible. This leads to the following duty-cycle requirement:

$$d^2_{\text{aux}} \approx \frac{kC_{\text{in}}}{(25T_{\text{clk}})(5I_B)} \tag{10}$$

where I_B is the bias current of g_{m1}. Equation (10) assumes that the input devices of g_{m1} were biased in weak inversion, which is required for a power-optimized design. From (10), for $I_{\text{B}} = 1\ \mu$A, $d_{\text{aux}} = 1/28$. For the ease of digital implementation, d_{aux} is set to 1/16. Hence, the auxiliary path consumes very low power as compared with the first stage of the chopper opamp, while its noise contribution is also kept small. However, from Fig. 13, $v^2_{\text{in,aux}}$ has power at multiples of $2f_{\text{clk}}$, leading to output ripples at $2f_{\text{clk}}$. These ripples are expected to be small due to the limited bandwidth of the front end.

The auxiliary-path impedance-boosting technique has two critical advantages over the positive feedback loop employed in [26]. As discussed in Section III, the positive-feedback loop is rendered inoperative at dc if a servo-loop is used. This is because the positive-feedback loop is driven by the output V_{out}, and the servo-loop attenuates the dc signal at V_{out}. In contrast, the auxiliary path is driven by the voltage appearing at the input V_{in}. Hence, the auxiliary-path technique can be employed simultaneously with a dc servo-loop, which is necessary in a practical neural recording front end. Another key advantage of the auxiliary-path technique is its insensitivity to parasitic capacitance. The positive-feedback technique is very sensitive to parasitic capacitance appearing at the bottom plate of C_{in}, as discussed in [26]. When the auxiliary-path technique is used, any parasitic capacitance appearing at the bottom plate of C_{in} reduces the bandwidth of the auxiliary path buffer, which increases the error ΔV [see (7)] due to insufficient settling time in the precharge phase. For a typical bottom-plate capacitance of $C_{\text{in}}/5$, increasing the bandwidth of the auxiliary path buffer by 20% compensates for the bottom-plate capacitance. Since the power consumed by the auxiliary buffers is very low compared with g_{m1}, increasing the bandwidth of the buffers by 20% results in negligible additional power consumption. Hence, this technique can be made insensitive to parasitic capacitance.

C. Chopper Ripple Rejection

The upmodulated dc offset and flicker noise of the first opamp stage g_{m1} can appear as large ripples at the amplifier output. These ripples can significantly reduce the available linear swing at the output, as discussed in [26], thus reducing the dynamic range of the front end. By placing a dc-blocking impedance after g_{m1}, as shown in Fig. 14, the chopper ripples at the output V_{out} can be attenuated without additional power consumption. A dc-feedback loop is necessary to establish a stable input bias voltage for the first opamp stage. This ripple-rejection technique is discussed in [34]. Referring to [34, Fig. 2], the ripple attenuation is given by g_{m1}R. However in this paper, there is no path for dc current to flow from g_{m1} to g_{m2} (Fig. 6), or referring to [34, Fig. 3], the resistance R is infinite. Thus, the expected attenuation of ripples caused by the dc offset of g_{m1} is infinite. To attenuate ripples caused by the flicker noise of g_{m1}, the unity-gain frequency (referring to [34, Fig. 3.]) of the transfer function $[V_{\text{out}}(f_{\text{clk}} + f)/v_n(f)]/A_o$, which is given by $\omega_{\text{ugbf}} = [A_o\omega_{\text{clk}}C_C/(R_f(C_{\text{in}} + C_f + C_{\text{dsl}})C)]^{0.5}$, should ideally be larger than the flicker-noise corner frequency of g_{m1}. Here, $A_o = C_{\text{in}}/C_f$ is the closed-loop gain. For $C_c = 2$ pF, $R_f = 20$ GΩ, and $C = 10$ pF, f_{ugbf} is 830 Hz, while the simulated flicker-noise corner of g_{m1} was 3.4 kHz. Either R_f or C can be reduced to increase f_{ugbf}, but reducing R_f would increase its in-band noise contribution, while reducing C would increase signal swings at the output of g_{m1}. Due to these considerations, f_{ugbf} was kept at 830 Hz, since this is sufficient to attenuate the majority of the flicker noise of g_{m1}.

V. Experimental Results

The proposed chopper amplifier was fabricated in a 40-nm CMOS technology. Fig. 15 shows the chip micrograph, and the

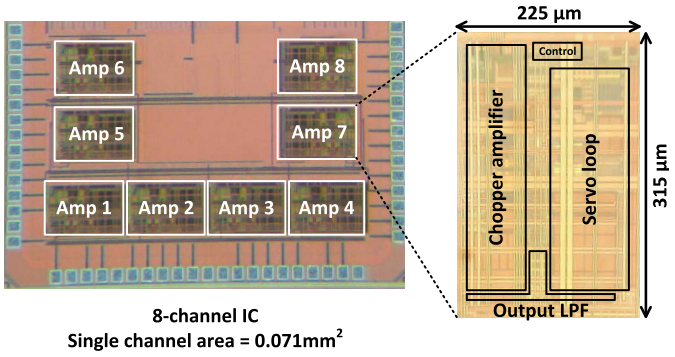

Fig. 15. Micrograph of the fabricated prototype showing eight chopper amplifiers implemented in 40-nm CMOS.

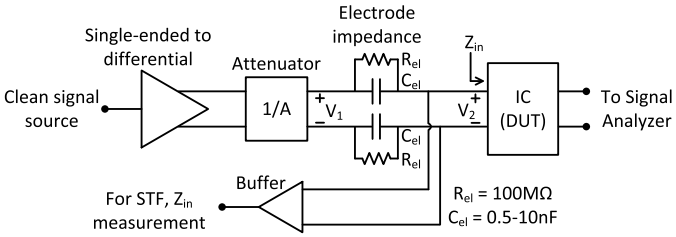

Fig. 16. Test setup for characterizing the fabricated chopper amplifier.

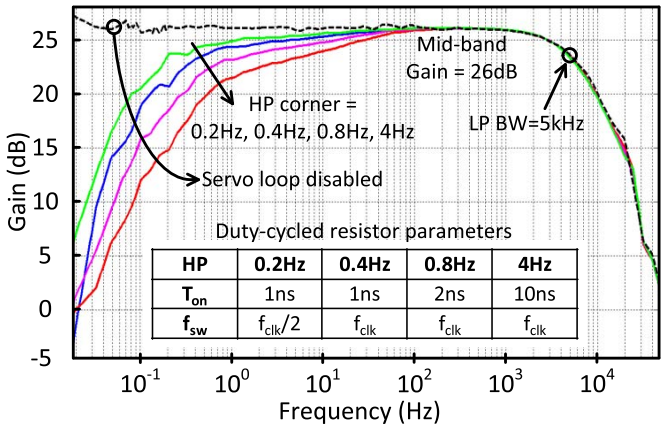

Fig. 17. Measured signal transfer function of fabricated chopper amplifier, with programmable high-pass corner frequency.

experimental setup for characterizing the fabricated prototype is shown in Fig. 16. The electrode impedance is emulated on the PCB with a parallel-*RC* impedance to mimic realistic scenarios. The single-channel area is 0.071 mm^2, and the total power drawn from a 1.2 V supply is measured to be 2 μW. The opamps used in g_{m1}, g_{m2}, servo-loop, and the auxiliary path consume 1.2, 0.18, 0.36, and 0.12 μW, respectively. Digital control logic consumes 0.12 μW. The measured signal transfer functions are shown in Fig. 17. The midband gain is 26 dB with a low-pass cutoff of 5 kHz. The high-pass corner is programmable from 0.2 to 4 Hz by varying the duty-cycle factor of the resistors in the servo-loop integrator. Fig. 17 shows unexpected drooping in the high-pass shape of the signal transfer function. We suspect that the substrate capacitance of the poly-resistor (in the DCR) used to realize R_{int} in the servo-loop contributes to additional filtering.

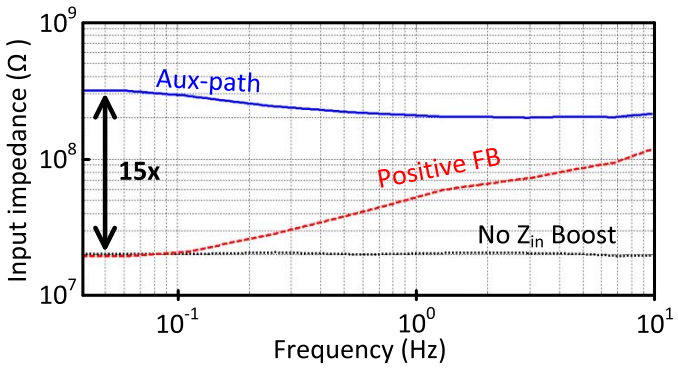

Fig. 18. Measured input impedance of the chopper amplifier using different impedance-boost techniques.

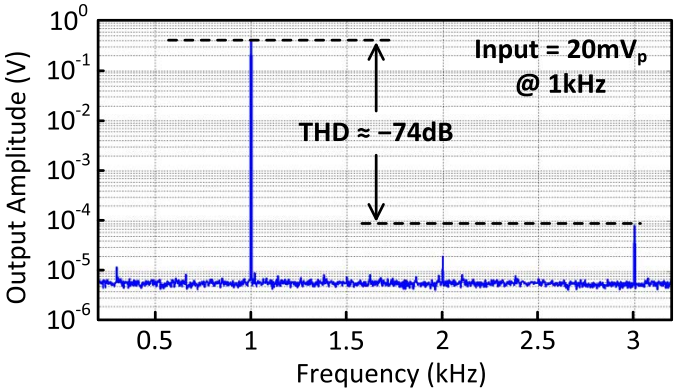

Fig. 19. Measured harmonic distortion of the chopper amplifier for a 20-mVp input at 1 kHz.

The input impedance of the chopper amplifier is measured as follows. From Fig. 16, since $V_2/V_1 = Z_{\text{in}}/(Z_{\text{in}} + Z_{\text{el}})$, where Z_{el} is the parallel-*RC* impedance formed by R_{el} and C_{el}, measuring V_2 is sufficient to determine Z_{in}. The measured input impedance of the front end is shown in Fig. 18. The input impedance is 20 MΩ when all the impedance boosting techniques are disabled. When the positive feedback loop is enabled, the plot in Fig. 18 clearly shows that there is no impedance boost at dc, since the servo-loop attenuates the dc signal at V_{out}. When the auxiliary path is enabled, the dc input impedance is boosted to 300 MΩ, which is 15 times higher than the nominal impedance of 20 MΩ. This demonstrates the fact that the auxiliary path can be used simultaneously with the servo-loop. The input impedance is lower than the expected value (400 MΩ) from simulations and (8). We suspect this is due to increased settling errors in the precharge phase due to the duty cycling of bias currents in the auxiliary-path buffers.

For an input tone of 20 mV$_{\text{p}}$ at 1 kHz, the total harmonic distortion is −74 dB, as shown in Fig. 19. The input-referred noise density is shown in Fig. 20(a), and the integrated noise is 7 μV$_{\text{rms}}$ in the AP band and 2 μV$_{\text{rms}}$ in the LFP band. The noise bandwidth for integration in the LFP and AP band is 1–200 Hz and 200 Hz–20 kHz, respectively. The servo-loop is enabled for all measurements. The output spectrum of the front end beyond the signal band is shown in Fig. 20(b). The ripple around the chopping clock frequency ($f_{\text{clk}} = 25$ kHz) is only 12.6 μV, which demonstrates the efficacy of the ripple-rejection technique. Unfortunately, no provision was made to disable the ripple-rejection technique to measure the

TABLE II
COMPARISON WITH THE CURRENT STATE OF THE ART

Spec	[18] JSSC'07	[26] JSSC'11	[35] JSSC'12	[27] ISSCC'14	This work
Power/Ch	2 µW	1.8 µW	5.04 µW	2.3 µW	**2 µW**
Supply	1.8 V	1 V	0.5 V	0.5 V	**1.2 V**
Signals [a]	LFP	LFP	AP + LFP	LFP	**AP + LFP**
Peak Input	5 mV_p	Not specified	---	0.5 mV_p	**20 mV_p**
Input-referred noise (V_{rms})	LFP: 1 µV	LFP: 6.7 µV [b]	AP: 4.7 µV LFP: 4.3 µV	LFP: 1.3 µV	**AP: 7 µV LFP: 2 µV**
NEF	LFP: 4.6	LFP: 14 [b]	AP: 5.99 LFP: 30	LFP: 4.76	**AP: 4.9 LFP: 7**
DC Input-impedance	8 MΩ	6 MΩ [b]	∞	28 MΩ	**300 MΩ**
Dynamic Range [c]	67 dB (LFP)	---	~35 dB	50 dB (LFP)	**69 dB (AP) 78 dB (LFP)**
Total Harmonic Distortion	–60 dB	Not specified	–37 dB	–48 dB	**–74 dB**
Area/ch	1.7 mm^2	0.1 mm^2	0.013 mm^2	0.025 mm^2	**0.071 mm^2**
Technology	0.8um	65nm	65nm	65nm	**40nm**

[a] LFP: Local Field Potentials, AP: Action Potentials
[b] Servo loop enabled
[c] Calculated for distortion power = noise power

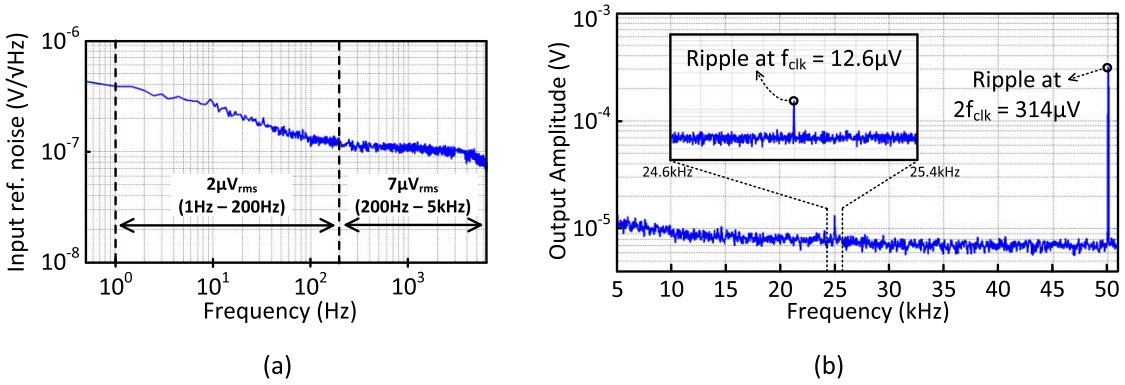

Fig. 20. (a) Measured input-referred noise. (b) Output ripples of the chopper amplifier.

ripple attenuation. The auxiliary-buffer offset gets upmodulated to $2f_{clk}$ and appears as a 314-μV ripple at the output, as discussed in Section IV-B. When the auxiliary path was disabled, the ripple at $2f_{clk}$ reduced to 14 μV, confirming our reasoning. Since the output ripples are small compared with the output signal swings (~400 mV_p), the ripples will not degrade the dynamic range of the front end. To demonstrate the robustness of this front end in the presence of large in-band interferers, a two-tone test is performed. A large-amplitude tone, denoting the interferer, is used along with a small-amplitude tone, denoting the neural signal of interest. The measured outputs for the two-tone tests are shown in Fig. 21. The intermodulation tones are at least 56 dB lower than the signal of interest, which is sufficient for digitizing the signal of interest with a 7–8-b ENOB. This measurement shows that the proposed front end can be used in the presence of artifacts as large as 40 mV_{pp}. For a 20-mV_p input swing, the dynamic range of the front end is 69 dB in the AP band and 78 dB in the LFP band. The prototype was used to sense prerecorded human LFP and AP signals using microelectrodes dipped in a phosphate-buffered saline solution. The recorded outputs are shown in Fig. 22, demonstrating that the proposed front end can work with real electrodes.

Table II summarizes the measured performance of our front end, and compares the performance with the current state of the art. Our work significantly improves the

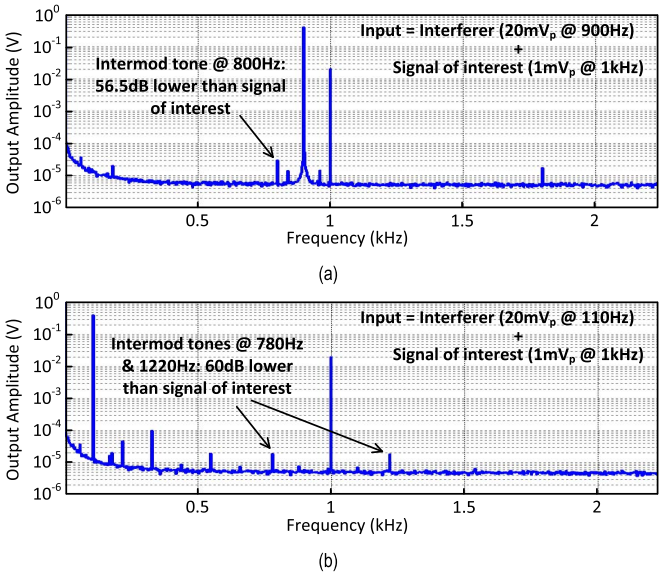

Fig. 21. Measured performance of the chopper amplifier for two input tones, with a large tone signifying an interferer and a small tone signifying a neural signal. (a) High-frequency interferer. (b) Low-frequency interferer.

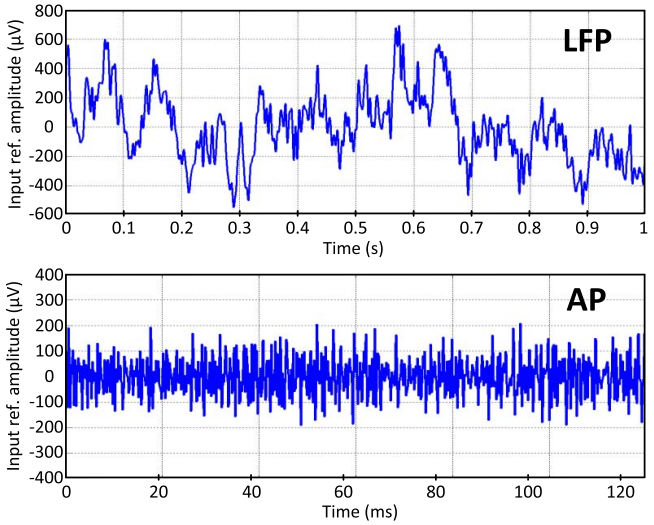

Fig. 22. *Invitro* measurements using prerecorded human neural recordings.

linearity (by 14–26 dB), dynamic range (by 11–28 dB), and input-impedance for chopped front ends (by >11 times), while achieving the state-of-the-art power and noise performance.

VI. Conclusion

This paper presents a chopper stabilized front end capable of closed-loop neural recording in the presence of large in-band stimulation artifacts up to 40 mV_{pp}. New techniques have been presented to solve critical problems, such as the auxiliary path technique to boost the input impedance of chopper front ends, and employing duty-cycled resistors to realize very-low bandwidth integrators for electrode-offset rejection. These techniques enable a dc input impedance of 300 MΩ, a reliable and programmable high-pass corner frequency from 0.2 to 4 Hz, and a total harmonic distortion (THD) of −74 dB for a 40-mV_{pp} input, while maintaining the state-of-the-art power and noise performance. Unlike the prior work, these techniques can be used along with the servo-loop and are immune to parasitic capacitance, ensuring that all the performance requirements outlined in Table I can be achieved simultaneously, which enables a robust neural recording front end capable of closed-loop operation.

Acknowledgment

The views, opinions, and/or findings expressed are those of the authors and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government.

The authors would like to thank Dr. V. Karkare for technical discussions, V. Hokhikyan for testing support, Dr. I. Fried, Prof. N. Suthana, and Prof. R. Staba for human single unit and local-field potential data, Lawrence Livermore National Laboratory for electrodes, and Dr. Y. Toriyama for reviewing the manuscript.

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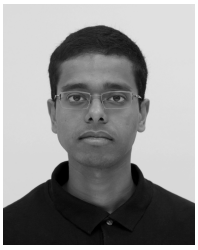

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