

# A MEMS-Assisted Temperature Sensor With 20- $\mu\text{K}$ Resolution, Conversion Rate of 200 S/s, and FOM of 0.04 pJK $^2$

Meisam Heidarpour Roshan, Samira Zaliasl, Kimo Joo, Kamran Souri, Rajkumar Palwai, Lijun (Will) Chen, Amanpreet Singh, Sudhakar Pamarti, Nicholas J. Miller, Joseph C. Doll, Carl Arft, Sassan Tabatabaei, Carl Sechen, *Fellow, IEEE*, Aaron Partridge, and Vinod Menon

**Abstract**—This paper presents a dual-microelectromechanical system (MEMS) resonator-based temperature sensor. In this sensor, the readout circuit estimates the temperature by measuring the frequency ratio of the two clocks generated by separate resonators with different temperature coefficients. The circuit is realized in a 0.18- $\mu\text{m}$  CMOS process and achieves a resolution of 20  $\mu\text{K}$  over a bandwidth of 100 Hz while consuming 19 mW of power, leading to a resolution FOM of 0.04 pJK $^2$ . It enables us to implement a MEMS-based programmable oscillator with an Allan deviation of  $<1\text{e}^{-10}$  over 1 s averaging time, and a frequency stability of  $<\pm 0.1$  parts per million in the temperature range from  $-45^\circ\text{C}$  to  $105^\circ\text{C}$ . Such oscillators are key building blocks in telecom, datacom, and precision timekeeping applications.

**Index Terms**—Dual-microelectromechanical system (MEMS) resonator temperature-to-digital converter (TDC), MEMS-based programmable oscillator, temperature-compensated MEMS oscillator (TCMO).

## I. INTRODUCTION

THERE are many applications requiring precision oscillators with various levels of requirements for jitter, frequency stability over temperature and during thermal transient, power consumption, and so on. For example, consumer electronics, such as wireless USB, need  $<\pm 30$  parts per million (ppm) [2], commercial GPS requires  $<\pm 2.5$  ppm [3], and telecom applications demand  $<\pm 0.1$  ppm frequency stability [4], [5]. Appropriate clocks are usually made with either quartz or microelectromechanical system (MEMS) resonators. Recent advances in the MEMS technology have allowed MEMS oscillators to replace quartz oscillators that had been dominant for several decades [6]–[14]. Quartz and MEMS offer similar resonator quality factor, a key parameter required

Manuscript received May 9, 2016; revised September 2, 2016; accepted October 13, 2016. Date of publication November 16, 2016; date of current version January 4, 2017. This paper was approved by Guest Editor Roman Genov.

M. Heidarpour Roshan is with SiTime, Santa Clara, CA 95054 USA, and also with the University of Texas, Dallas, TX 75080 USA.

S. Zaliasl, K. Joo, K. Souri, R. Palwai, L. Chen, A. Singh, N. J. Miller, J. C. Doll, C. Arft, S. Tabatabaei, A. Partridge, and V. Menon are with SiTime, Santa Clara, CA 95054 USA.

S. Pamarti is with the University of California at Los Angeles, Los Angeles, CA 90095 USA.

C. Sechen is with the University of Texas at Dallas, Richardson, TX 75080 USA.

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2016.2621035

to achieve low phase noise (PN), and integrated phase jitter [35]. In addition, both can demonstrate a temperature sensitivity as low as 1 ppm/K, which is needed to achieve accurate and stable clock frequencies across temperature. MEMS oscillators are growing in importance due to benefits they have over quartz oscillators [12]–[15]. For example, they leverage semiconductor processes and packaging, resulting in a smaller size and lower cost [16], [17]. MEMS oscillators also exhibit higher immunity to shock and vibration, which makes them a suitable choice for applications with low PN requirement in adverse environments, such as mobile devices and industrial equipment, where the oscillator may be subject to substantial external vibration [18], [19].

Both types of oscillators are available in temperature-compensated and temperature-uncompensated variants. The uncompensated versions are typically stable to within tens or a hundred parts per million over temperature. To achieve sub-10 ppm stability, their frequencies must be compensated over temperature [9], [15]. Traditionally, the uncompensated and compensated quartz oscillators are referred as XOs, and TCXOs, respectively. The timing community identifies MEMS oscillators as XOs and TCXOs as well, but instead occasionally has used the terms MOs and TCMOs, although the latter is becoming uncommon.

As shown in Fig. 1, a MEMS-based programmable oscillator package contains three elements: a MEMS die, a CMOS die, and a leadframe. As illustrated in Fig. 2(a), the MEMS die only carries resonators, while the CMOS die includes the electronics, such as the oscillator sustaining circuit, frequency synthesizer, and post-divider, that are necessary to sustain the oscillation of the MEMS resonator and to output a clock at the desired frequency  $F_{\text{out}}$ , which in XO mode, *i.e.*, without temperature-compensation, can be expressed as

$$F_{\text{out}} = F_{\text{ref}} \times \text{PFM} / N_{\text{Pdiv}} \quad (1)$$

where  $F_{\text{ref}}$  is the PLL reference clock frequency, PFM is the programmable frequency multiplier, and  $N_{\text{Pdiv}}$  is the postdivider value. In this temperature-uncompensated mode, the output clock stability over temperature is set by that of the MEMS resonator. The TCXO described in this paper employs a temperature sensor, whose output is properly scaled by a polynomial to generate the inverse error of  $F_{\text{ref}}$  at each temperature, thereby adjusting the PFM value to maintain the

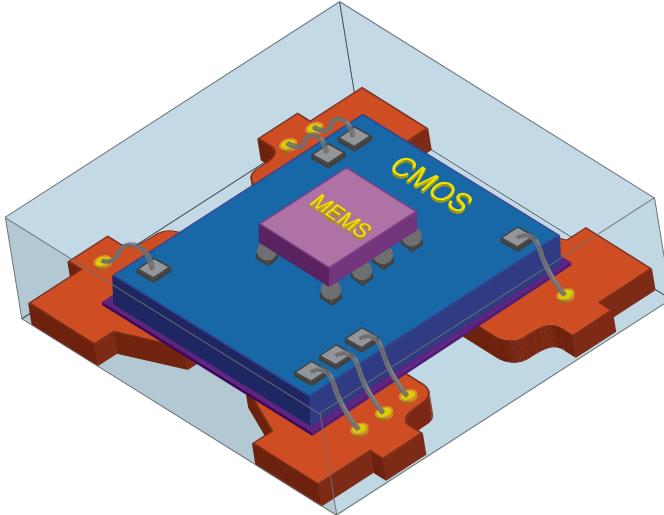


Fig. 1. MEMS-based programmable oscillator includes a CMOS die, a MEMS die, and a leadframe in a single package.

output clock frequency stable [Fig. 2(b)]. Therefore

$$F_{\text{out}} = F_{\text{ref}} \times (1 + \text{TDC}_{\text{out}}) \times \text{PFM}/N_{\text{Pdiv}} \quad (2)$$

where  $\text{TDC}_{\text{out}}$  is a scaled output of the temperature-to-digital converter (TDC). This technique, however, introduces the TDC as another contributor to the output clock PN. Thus, it should have enough resolution to keep its noise within the acceptable range for the targeted clock jitter.

In this paper, a MEMS-based programmable oscillator suitable for telecom applications is presented [1]. The reference clock of the frequency synthesizer ( $\text{Clk}_{\text{TF}}$ ) is generated by a Temp-Flat MEMS (MEMS<sub>TF</sub>) resonator operating at  $f_{\text{TF}} = 47$  MHz, which exhibits  $<\pm 50$  ppm frequency stability over a temperature range from  $-45$  °C to  $105$  °C. In this application, the clock is required to have an Allan Deviation (ADEV) [20], [21] of  $< 1e^{-10}$  in 1 s of averaging time, even under breezy conditions where the oscillator experiences relatively fast temperature variation.

Although the oscillator in the XO mode theoretically meets the ADEV requirement, any temperature variation leads to the target ADEV violation due to a nonzero temperature sensitivity of  $\text{Clk}_{\text{TF}}$ . Hence, temperature compensation is essential to achieve the telecom applications critical clock requirement of  $< \pm 0.1$  ppm frequency error across temperature and ADEV. However, the TDC should have enough resolution, so that its noise does not degrade the output clock PN. A maximum temperature sensitivity of 1 ppm/K for MEMS<sub>TF</sub> and the ADEV target imply that for it to not dominate the output clock PN, its resolution should be much less than [9]

$$0.1 \text{ ppb(rms)} \frac{1}{1 \frac{\text{ppm}}{K}} = 100 \mu\text{K(rms)}. \quad (3)$$

This means that a TDC resolution of less than  $50 \mu\text{K}$  assures a negligible impact on the output clock PN. This resolution, however, should be achieved in a bandwidth (BW) of  $\geq 100$  Hz (*i.e.*, a conversion rate of 200 S/s) to maintain ADEV in the presence of fast temperature variation. By assuming a power consumption of  $< 20$  mW, another constraint set by

the application, the TDC should achieve a resolution FOM (Energy/Conversion  $\times$  Resolution<sup>2</sup>) [22] of  $< 0.25 \text{ pJK}^2$ .

For integrated temperature sensors published to date, the best reported resolution is  $100 \mu\text{K}$  (rms) at 10 S/s with a FOM of  $13 \text{ pJK}^2$ , as presented in [9]. It was employed to support a previous generation MEMS oscillator in our group. Scaling this work to meet the target requirements would necessitate a power consumption of 1 W. The sensor in [23] achieves the best energy-efficiency so far evidenced by a FOM of  $0.65 \text{ pJK}^2$ , but at a resolution of  $10 \text{ mK}$  (rms), which is prohibitively insufficient for our application. Further, both of those optimal examples are thermistor-based and are unlikely to meet the  $\pm 0.1$  ppm stability requirement (including hysteresis) over lifetime of the sensor. Other TDC types, *e.g.*, BJT-based sensors, have not yet achieved the required resolution and energy efficiency [22]. The best reported FOM for this type of sensors is  $3.2 \text{ pJK}^2$ , which is obtained at a resolution of  $3 \text{ mK}$  and a conversion rate of 455 S/s [25].

This paper presents a dual-MEMS-resonator temperature sensor. It achieves  $20 \mu\text{K}$  resolution over a 100 Hz BW, while dissipating 19 mW power, resulting in a resolution FOM of  $0.04 \text{ pJK}^2$ . This is the best energy-efficiency reported for integrated temperature sensors to date. It enables a MEMS-based programmable oscillator suitable for telecom applications. The rest of this paper is organized as follows. Section II explains the path taken toward designing the topology of the temperature sensor presented in this paper. Both system- and circuit-level implementation details are discussed in Section III. Section IV is devoted to realization and measurement results. Finally, the conclusion is presented in Section V.

## II. ARCHITECTURAL DESIGN

### A. Background

As stated above, this temperature sensor is needed to compensate for the frequency variation of a MEMS resonator across temperature. In order to maintain the frequency stability in the presence of rapid temperature fluctuations, it is important to maximize thermal coupling between the sensor front-end and the resonator itself. The work in [33] employs a MEMS resonator, which has two fundamental modes of oscillation with different temperature coefficients. Thus, temperature can be found by measuring the ratio of the frequency variation of each mode. In this architecture, the sensor front end is part of the resonator, which results in tight thermal coupling. However, the potential for modal interaction in such a resonator limits design freedom, and may not be optimal for low PN. The sensor in [34] utilizes two resonators with frequencies of  $f_1$  and  $f_2$ , and different temperature coefficients, encapsulated in a low-power micro-oven fabricated on silicon. A PLL regulates the oven temperature by locking the phases of the signals with frequencies of  $f_1 - f_2$  and  $f_1/N$ , in which  $N$  is chosen properly, such that the two signals have identical frequencies at a certain temperature. Using this topology, which in fact should be categorized as an oven-controlled MEMS oscillator, the authors could successfully achieve a frequency stability of  $< \pm 1$  ppm. However, similar

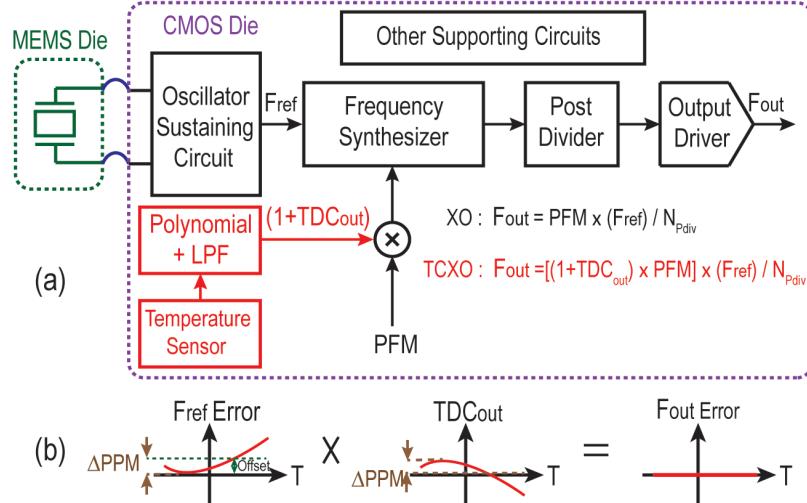


Fig. 2. (a) MEMS-based programmable oscillator architecture in both XO and TCXO modes. (b) In a TCXO device, the output clock frequency remains stable through multiplying the PFM value by a properly scaled TDC output.

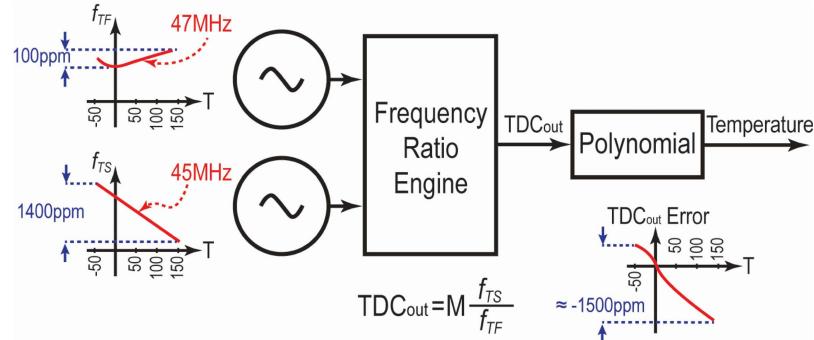


Fig. 3. General architecture of a temperature sensor operating based on measuring the ratio of the frequencies of two oscillators with different temperature coefficients.

to the previous example, to avoid modal interaction between the resonators through the oven, they may not be optimized for the best PN.

As depicted in Fig. 3, measuring the frequency ratio of two on-chip oscillators with different temperature sensitivities is a well-known approach to realize a temperature sensor [26]–[28]. The resolution of such a sensor is determined by the PN of the oscillators as well as the random and/or quantization noise of the frequency ratio engine itself. Employing low-jitter MEMS-generated clocks, together with a low noise frequency ratio engine, can be considered as a solution toward achieving the target resolution. Therefore, besides MEMSTF, a Temp-Sense MEMS (MEMSTS) resonator with a temperature coefficient of  $-7$  ppm/K is also employed to generate  $Clk_{TS}$ , the second input clock for the frequency ratio engine, that oscillates at  $f_{TS} = 45$  MHz. As shown in Fig. 4, both resonators are placed next together to maximize their thermal coupling. Each resonator includes four rings, which are used for capacitive actuation and sensing, and coupled by cross-members [35]. Both resonators achieve a typical quality factor of 150 000. Their temperature sensitivities are tightly controlled by manipulating the mechanical properties of the resonators. In this scheme, the challenge of designing the TDC is practically narrowed down to realizing a frequency ratio

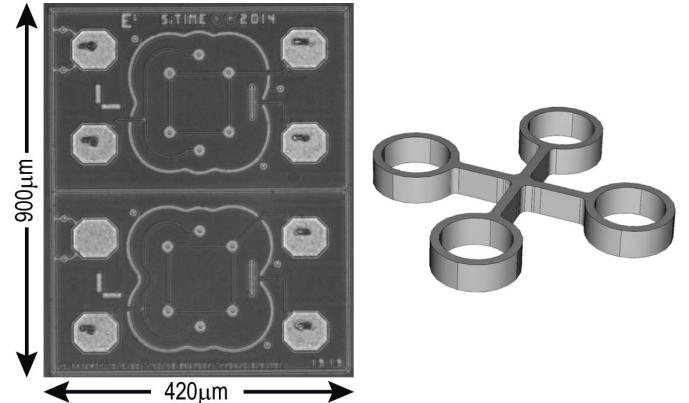


Fig. 4. 3-D view of both MEMSTF and MEMSTS resonators and the MEMS die photo.

engine, whose output noise is dominated by the PN of its two input clocks.

Fig. 5(a) illustrates the most straightforward architecture of measuring the ratio of the two frequencies. As shown, a number of cycles that are generated by the clock  $f_1$  are counted during a gate time set by a divided version of another clock, *i.e.*,  $f_2/M$  [29], [30]. Therefore, the counter value changes proportional to the ratio of the two frequencies.

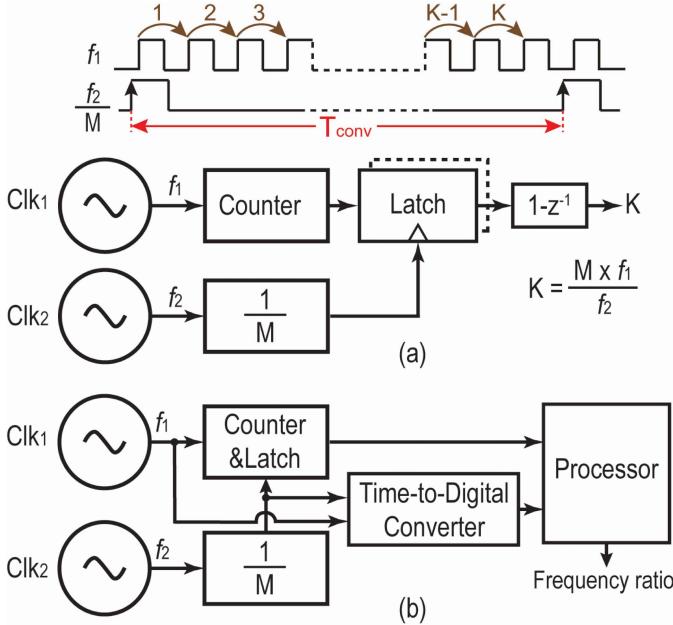


Fig. 5. (a) Reciprocal counting method. (b) Employing a time-to-digital converter to improve the speed of the reciprocal counting method.

However, this topology is extremely slow to achieve high resolutions. For instance, in this paper, a  $50-\mu\text{K}$  change in temperature causes the  $\text{Clk}_{\text{TS}}$  period  $T_{\text{TS}}$  change by

$$\begin{aligned}\Delta T_{\text{TS}} &\approx 7 \left( \frac{\text{ppm}}{K} \right) \times 50 \mu\text{K} \times T_{\text{TS}} \times 10^{-6} \\ &\approx 7.78 \times 10^{-18} \text{ s.}\end{aligned}\quad (4)$$

Since the smallest detectable time change by the counter is  $T_{\text{TS}}$ , assuming a period of  $T_{\text{TF}}$  for  $\text{Clk}_{\text{TF}}$ , the minimum required conversion time  $T_{\text{conv}}$  to detect such small temperature change is given by

$$T_{\text{conv}} = \frac{T_{\text{TS}}}{\Delta T_{\text{TS}}} \times T_{\text{TF}} \approx 60.7 \text{ s} \quad (5)$$

which is impractically large and cannot be afforded in most applications.

As shown in Fig. 5(b), in a different approach, a TDC can be used in order to detect the accumulated phase change by  $\Delta T_{\text{TS}}$  during the sensor's full conversion time, e.g., 5 ms in this paper, resulting in a required time resolution  $T_{\text{res}}$  of

$$T_{\text{res}} \approx \frac{T_{\text{conv}}}{T_{\text{TS}}} \times \Delta T_{\text{TS}} \approx 1.75 \text{ ps} \quad (6)$$

which is not easily achievable in the  $0.18-\mu\text{m}$  CMOS process used in this paper. It should be noted that the results in (5) and (6) by themselves are optimistic as they do not consider the noise contribution by the two clocks. A key observation is that in both of these approaches, the information on all the edges of  $\text{Clk}_1$  and  $\text{Clk}_2$  is lost between the sampling points. From an information perspective, a loss of information inherently translates to a reduction in performance when at the limit of the data in the signal.

### B. New Frequency Ratio Engine Architecture

As demonstrated in Fig. 6(a), a new approach is presented in this paper, which operates based on measuring the time differences  $\Delta T_i$  between the rising edges of the two clocks, thereby

exploiting the information available on all the transition points. By passing the resulting  $\Delta T$  sequence through an optimal filter, the ratio between the two frequencies can be measured with the desired resolution and speed. The optimal filter could be a high-order low-pass filter or a least mean square adaptive filter. Plotted in Fig. 6(b), this idea can be implemented by employing a high-speed ring oscillator, followed by two-phase quantizers. Each of the phase quantizers measures the phase travelled by the ring oscillator during every period of its input clock. Thus, the ratio between the output of the two quantizers is a unit-less number, containing the frequency ratio information that can be extracted with the target resolution after proper filtering. The higher the oscillation frequency of the ring, the higher the resolution the time-to-digital converter achieves, thus leading to a better frequency ratio estimation. Although this topology works fine, it suffers from all the downsides of a free running ring oscillator, e.g., frequency drift over a long time.

Illustrated in Fig. 6(c), in order to overcome the aforementioned issue, the free running ring oscillator is placed inside a phase-locked loop to lock its phase to  $\text{Clk}_{\text{TF}}$ . Therefore, only one phase quantizer is needed for  $\text{Clk}_{\text{TS}}$ , since  $\text{Clk}_{\text{TF}}$  has already been phase-locked to the ring oscillator. In this scheme, the phase quantizer measures the phase travelled by the ring oscillator during each  $\text{Clk}_{\text{TS}}$  period, from which the frequency ratio can be estimated after a proper filtering. The performance of this viable architecture can be further improved by locking the ring oscillator to the scaled frequency ratio of the input clocks. As shown in Fig. 6(d), this topology forms a new PLL with a reference of  $\text{Clk}_{\text{TS}}$ , in which the other PLL is nested inside it, acting as a digitally controlled oscillator (DCO) for the outer loop. For this idea to work, the ring oscillator must be placed inside a fractional-N PLL, as the frequency ratio is a noninteger quantity. This topology is the core idea of the frequency ratio engine used in this paper, leading us to measure the temperature with high resolution in a short conversion time. The key advantage of this architecture is that it extracts all the temperature information available on the edges of the two input clocks, and in fact, that is how it enables meeting the target resolution and speed specifications simultaneously.

## III. IMPLEMENTATION

### A. System Level

Fig. 7 shows the block-level architecture of the presented frequency ratio engine. It consists of an analog  $\Sigma\Delta$  fractional-N PLL referenced to  $\text{Clk}_{\text{TF}}$ , nested in a digital PLL referenced to  $\text{Clk}_{\text{TS}}$ . Assuming a fixed  $f_{\text{TF}}$ , the analog PLL behaves like a DCO, since its output frequency  $f_{\text{DCO}}$  is set by the fractional divider input value  $\text{DCO}_{\text{in}}$ , which is a digital number. Hence

$$f_{\text{DCO}} = f_{\text{TF}} \times \text{DCO}_{\text{in}}. \quad (7)$$

On the other hand, the digital PLL employs a feedback divider value of 10, and thus

$$f_{\text{DCO}} = f_{\text{TS}} \times 10. \quad (8)$$

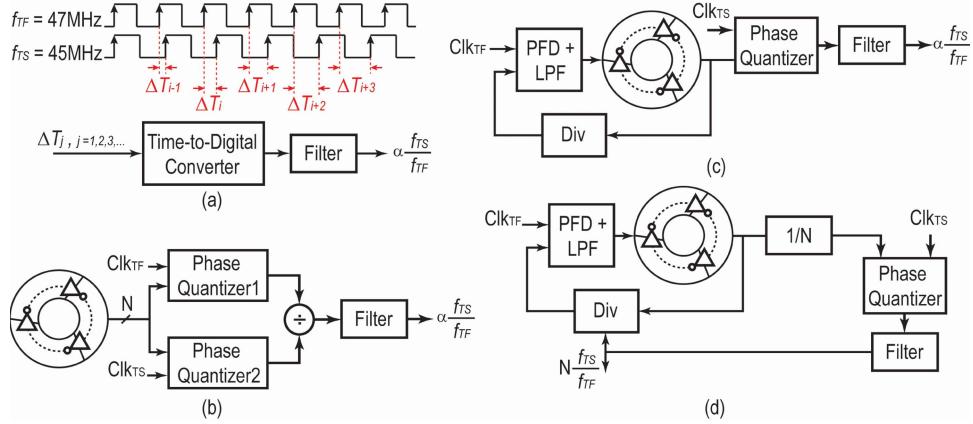


Fig. 6. (a) Architecture of a temperature sensor operating based on computing the frequency ratio of two clocks using a time-to-digital converter and a filter. (b) Implementing the time-to-digital converter by utilizing a ring oscillator and two-phase quantizers. (c) Ring oscillator is phase locked to \$Clk\_{TF}\$. (d) Oscillator runs at the scaled ratio of the frequencies of the input clocks.

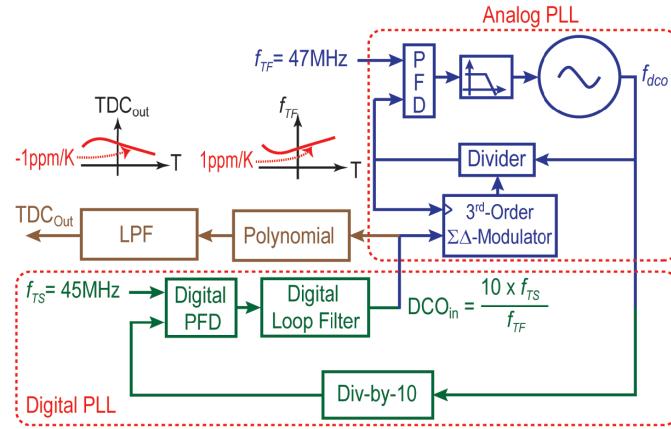


Fig. 7. Block diagram of the presented dual-MEMS-resonator temperature sensor.

Therefore, by combining (7) and (8), the fractional divider input value is expressed as

$$DCO_{in} = \frac{10 \times f_{TS}}{f_{TF}}. \quad (9)$$

The feedback loops force \$DCO\_{in}\$ to be always a scaled ratio of the input clock frequencies. Thus, temperature can be read out by postprocessing the \$DCO\_{in}\$ value. Similar to Fig. 5, the voltage-controlled oscillator (VCO) of the analog PLL is part of a time-to-digital converter used in the digital phase quantizer. The higher the frequency it oscillates, the less the noise the digital PFD injects into the loop. According to the noise analysis described in Section IV, a divide value of 10 makes the resolution target attainable without imposing too much complexity on the digital PFD, while keeping the VCO power consumption in a reasonable range. Since this temperature sensor is aimed to compensate for the MEMS<sub>TF</sub> frequency variation, as shown in Fig. 7, its output is properly scaled to exhibit the inverse characteristic of the \$f\_{TF}\$ error across temperature. To do so, \$DCO\_{in}\$ is applied to a digital block, so called TDC datapath, composed of a digital seventh-order polynomial followed by a low-pass filter. The polynomial order is chosen based on the level of the non-linearity of the two resonators and the target output frequency stability. Its coefficients are also individually set for each device after characterizing the resonators over temperature.

The low-pass filter cuts the noise of the TDC above the desired BW.

#### B. Noise Analysis and Circuit-Level Implementation

The key target in the design of the TDC is that the frequency ratio engine has sufficiently high BW to track rapid temperature variation while having a negligible impact on the TDC output noise at close-in. Fig. 8 illustrates the block-level model of the frequency ratio engine shown in Fig. 7, along with the major noise sources present in the system. As introduced earlier, the digital PLL is composed of a clock divider, a time-to-digital converter operating as a PFD, a digital loop filter \$L(z)\$, and a DCO. The digital loop filter output, which is the output of the frequency ratio engine, tracks the phase variation of \$Clk\_{TS}\$ within the digital PLL BW that occurs due to ambient temperature fluctuation. Thus, a BW of 5 kHz is considered for this loop to ensure the engine is sufficiently fast for the target temperature sensor BW. The DCO is an analog \$\Sigma\Delta\$ fractional-N PLL that includes an XOR PFD, a loop filter, a fractional divider, and a VCO. Besides \$Clk\_{TF}\$ PN, the \$\Sigma\Delta\$-modulator quantization noise as well as the VCO PN are the main contributors for the DCO output noise. In this design, a third-order \$\Sigma\Delta\$-modulator is employed to both reduce the in-band noise contribution of the fractional divider and also to increase the far-out noise power of the DCO that in practice dithers more the DCO output clock edge,

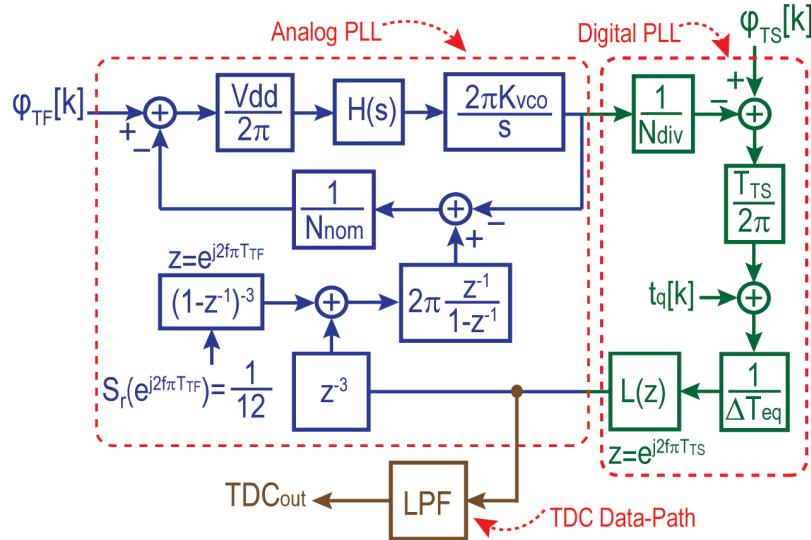


Fig. 8. Frequency-domain model of the frequency-ratio-engine.

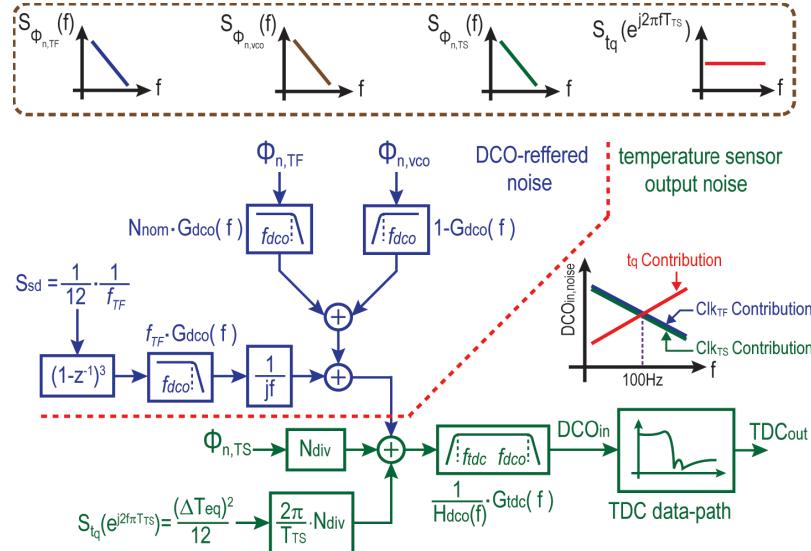


Fig. 9. Detailed view of the major noise sources present in the system and their transfer function toward the output of the temperature sensor.

and hence improves the effective resolution of the subsequent time-to-digital converter. Fig. 9 shows the major noise sources along with their shape across frequency and transfer function toward the TDC output [31], in which

$$A_{\text{dco}}(f) = \frac{\text{vdd}}{2\pi} \times H(s) \times \frac{K_{\text{vco}}}{jf} \times \frac{1}{N_{\text{nom}}} \quad (10)$$

$$G_{\text{dco}} = \frac{A_{\text{dco}}}{1 + A_{\text{dco}}} \quad (11)$$

where  $A_{\text{dco}}(f)$  is the analog PLL loop gain, vdd is the PFD's supply voltage,  $H(s)$  is the transfer function of the loop filter,  $N_{\text{nom}}$  is the analog PLL nominal divide value, and  $G_{\text{dco}}(f)$  is a base function defined by  $A_{\text{dco}}(f)$ . Since  $A_{\text{dco}}(f)$  has a low-pass behavior with a pole at the origin,  $G_{\text{dco}}(f)$  also has the shape of a low-pass filter with a BW of the DCO loop  $f_{\text{dco}}$ , around 2 MHz. The DCO transfer function can be expressed as

$$H_{\text{dco}}(f) = f_{\text{TF}} \times G_{\text{dco}}(f) \times \frac{1}{jf}. \quad (12)$$

Similarly, the digital PLL loop gain can be found as

$$A_{\text{tdc}}(f) = \frac{T_{\text{TS}}}{2\pi} \times L(s) \times H_{\text{dco}}(f) \times \frac{1}{N_{\text{div}}} \quad (13)$$

$$G_{\text{tdc}}(f) = \frac{A_{\text{tdc}}}{1 + A_{\text{tdc}}} \quad (14)$$

where  $L(s)$  is the digital loop filter transfer function in the Laplace domain,  $N_{\text{div}}$  is the divide value, which is set to 10 in this design, and  $G_{\text{tdc}}(f)$  is a base function defined by  $A_{\text{tdc}}(f)$ . According to the definition of  $A_{\text{tdc}}(f)$ ,  $G_{\text{tdc}}(f)$  has a low-pass filter shape whose BW is equal to the digital PLL BW  $f_{\text{tdc}}$ , about 5 kHz. As far as the temperature sensor is concerned, the output noise power at frequencies below 100 Hz is important. Among the noise sources shown in Fig. 8, the  $\Sigma\Delta$ -modulator noise and the VCO PN have minimal impact on the output noise within that range. That is because inside the DCO, former is aggressively shaped by the modulator noise transfer function and the latter is attenuated by a high-pass transfer function. They both are further suppressed by the high-pass transfer function from the DCO output to the loop filter output

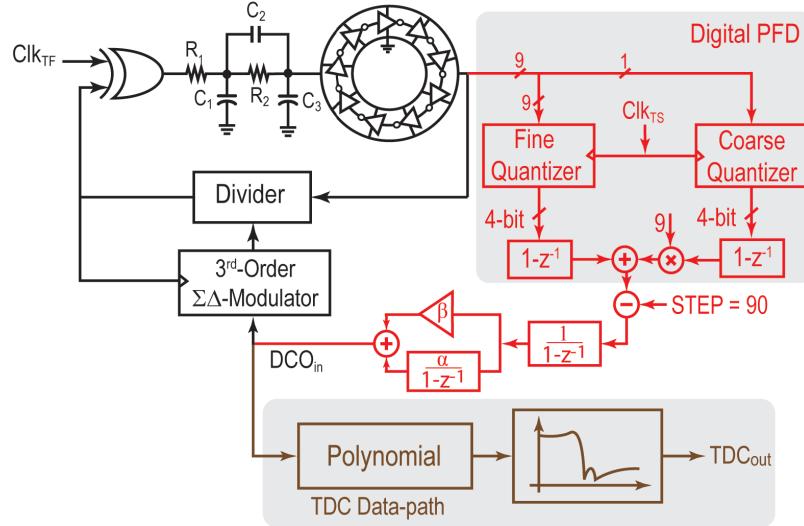


Fig. 10. Building blocks utilized to implement the frequency ratio engine and the TDC datapath.

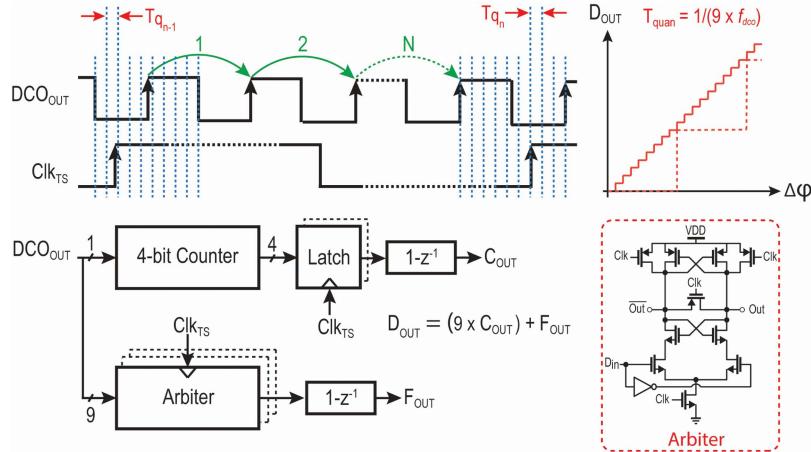


Fig. 11. Digital PFD architecture, composed of a coarse and a fine section.

of the digital PLL. The  $\text{Clk}_{\text{TF}}$  PN  $\emptyset_{n,\text{TF}}$ , however, is first amplified by  $N_{\text{nom}}$  within the DCO and then is attenuated by the high-pass shape of the transfer function from the DCO to the engine output. The  $\text{Clk}_{\text{TS}}$  PN  $\emptyset_{n,\text{TS}}$  passes through the same transfer function set by the digital PLL, while being gained up by  $N_{\text{div}}$  as well. Since the  $N_{\text{div}}$  and  $N_{\text{nom}}$  values are very close together in steady state, it is a fair statement that both  $\emptyset_{n,\text{TS}}$  and  $\emptyset_{n,\text{TF}}$  show up at the engine output with the same gain.

The last noise source is the quantization noise of the time-to-digital converter. It is assumed to have a noise power spectral density of  $(\Delta T_{\text{eq}})^2 / 12$  that goes through a transfer function similar to that of  $\emptyset_{n,\text{TS}}$ , but with a different dc gain. Hence, this noise has a negligible impact at very low frequencies. However, it is important to ensure it is going to stay below the noise contributed by the input clocks within the sensor BW. This model suggests a  $\Delta T_{\text{eq}} < 250$  ps to guarantee the minimal impact on the output noise at frequencies below 100 Hz.

Fig. 10 shows the frequency ratio engine in more detail. The PFD in the digital loop, which computes the DCO phase variation at every  $\text{Clk}_{\text{TS}}$  period, is composed of a coarse and a

fine section. As demonstrated in Fig. 11, the coarse quantizer is a 4-b counter that continuously counts the rising edges of the VCO output, which according to (7) runs at 450 MHz in the locked condition, and thus has a resolution of around 2.22 ns. To achieve a resolution of <250 ps, a fine quantizer is utilized to latch the state of the ring oscillator at every rising edge of  $\text{Clk}_{\text{TS}}$  through the arbiters connected to all of its internal phases. Theoretically, by considering both transitions of each phase in a VCO cycle, a quantizer in this configuration is capable of achieving a time resolution of  $T_{\text{VCO}}/2N_S$  [32], in which  $T_{\text{VCO}}$  and  $N_S$  are the clock period and the number of stages of the VCO, respectively. Hence, a five-stage single-ended ring oscillator seems a proper choice as it offers a resolution of 220 ps. However, the inequality between the rising-to-falling and falling-to-rising delays of each stage that changes across process, voltage, and temperature creates a nonlinear quantizer and will cause the DCO output noise to fold to the baseband. To avoid this problem, the VCO is designed with nine stages and instead only rising transitions are considered, as their time differences remain constant across all conditions, at around 245 ps. As shown in Fig. 10, the output of the coarse section is then multiplied by nine before

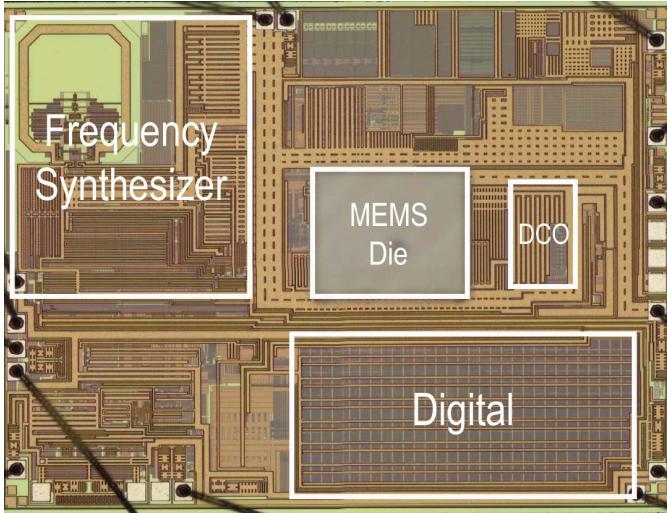


Fig. 12. Chip micrograph of the MEMS-based programmable oscillator.

being added to that of the fine quantizer output. Therefore, the digital PFD output  $D_{\text{OUT}}$  can be expressed as

$$D_{\text{OUT}} = (9 \times C_{\text{OUT}}) + F_{\text{OUT}} \quad (15)$$

where  $C_{\text{OUT}}$  and  $F_{\text{OUT}}$  are the outputs of the coarse and the fine quantizers, respectively. The VCO phase error, which is found by subtracting  $D_{\text{OUT}}$  from 90 steps (the desired phase travelled by the ring in the locked condition as computed by the digital PFD), is then fed to the digital loop filter. In fact, since the digital PLL forces the VCO phase error to be zero, this subtraction acts as a divide by 10. The digital loop filter output, whose coefficients are chosen for a 5-kHz BW, is applied to the  $\Sigma\Delta$ -modulator input of the DCO to close the loop and also to the TDC datapath for further processing and generating the proper correction value to compensate for the  $\text{Clk}_{\text{TF}}$  frequency error at each temperature. It is important that the digital circuitry has sufficient operand width, so that the truncation errors do not dominate the TDC output noise.

#### IV. REALIZATION AND MEASUREMENTS

Fig. 12 shows a chip micrograph of the MEMS-based programmable oscillator, in which the MEMS die is flipped and attached to a 0.18- $\mu\text{m}$  CMOS die. The oscillator sustaining circuits are placed under the MEMS die. The analog section of the frequency ratio engine is shown as DCO in this photo and the digital portion of the sensor is part of the chip digital block. The MEMS die carries both resonators:  $\text{MEMS}_{\text{TF}}$  and  $\text{MEMS}_{\text{TS}}$ . The resonators are physically placed as close as possible to maximize their thermal coupling. This is to ensure the TDC can accurately track any temperature fluctuations. The entire temperature sensor, including the MEMS die, the oscillator sustaining circuits for both resonators, and the frequency ratio engine followed by the TDC data-path, occupies around 0.54-mm<sup>2</sup> area and consumes about 19 mA of current from a 1.6 V regulated supply voltage. The polynomial coefficients for each part are calculated off-chip based on  $\text{Clk}_{\text{TF}}$ ,  $\text{Clk}_{\text{TS}}$ , and the output clock frequency

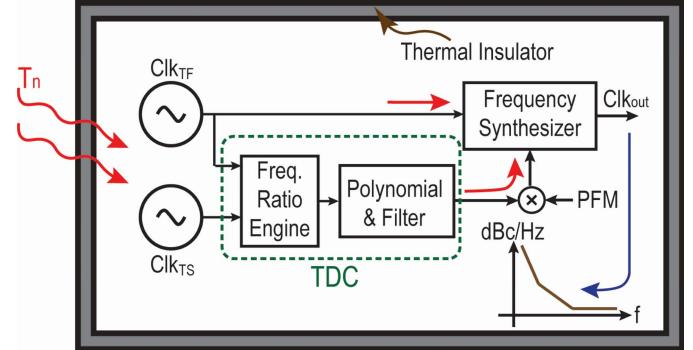


Fig. 13. Test setup for measuring the resolution of the temperature sensor.

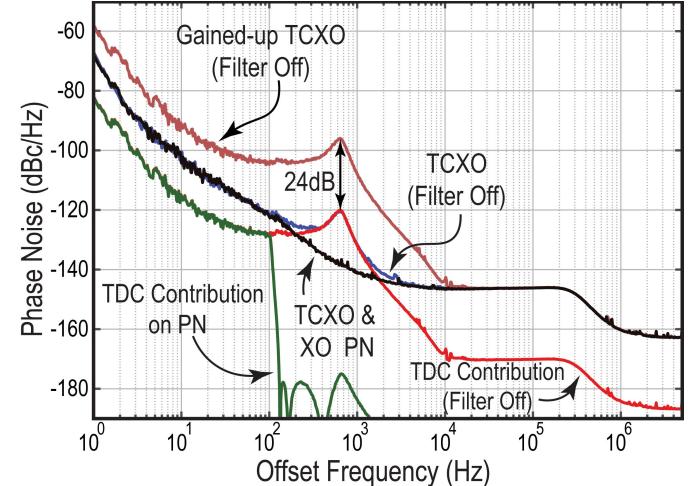


Fig. 14. Measured PN for a 20-MHz output clock in different operation modes as well as the estimated contribution of the temperature sensor on the output clock PN.

over temperature, and burned into nonvolatile memory in each device.

##### A. Resolution Measurement

In order to measure the resolution of a temperature sensor, normally, the device is encapsulated inside a thermal insulator to bring the environmental temperature variation well below the expected sensor resolution. Since this TDC's resolution is at the tens of  $\mu\text{K}$  level, measuring its performance in a standalone fashion is not trivial, due to the various sources of on- and off-chip thermal drifts present in the measurement setup and the climate chamber. However, in a TCXO device, as illustrated in Fig. 13, temperature variation appears as a common-mode noise for the frequency synthesizer, and thus, it does not show up at its output clock frequency and phase. Therefore, instead of stabilizing the temperature for reliably reading out the TDC, the output clock PN is measured to indirectly determine the TDC's output noise spectrum.

In a proper design, however, the TDC noise is too low that it does not emerge at the output. As shown in Fig. 14, the PNs of the output clocks are identical for both XO and TCXO modes, thus proving that the TDC noise does not change the output clock PN. To make the TDC noise measurable, the low-pass filter in the TDC data-path was initially bypassed to make its contribution observable in the frequency range from 200 to 2 kHz. As depicted in Fig. 15(a), in order to make the TDC noise the dominant source over the entire desired

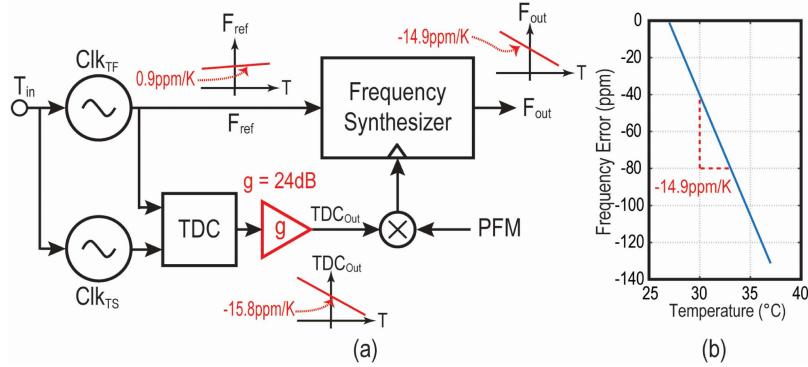


Fig. 15. (a) Frequency stability of a TCXO device with a gained up TDC output. (b) Output clock frequency drift versus temperature for the gained up TDC.

TABLE I  
PERFORMANCE COMPARISON WITH PREVIOUS BEST REPORTED TEMPERATURE SENSORS

	This Work	[Ref 23]	[Ref 29]	[Ref 9]	[Ref 25]
Sensor Type	Dual-MEMS Resonator	Resistor	Resistor	Resistor	BJT
CMOS Technology	$0.18\mu\text{m}$	$0.18\mu\text{m}$	$0.18\mu\text{m}$	$0.18\mu\text{m}$	$0.7\mu\text{m}$
Area	$0.54\text{ mm}^2$	$0.43\text{ mm}^2$	$0.09\text{ mm}^2$	$0.18\text{ mm}^2$	$0.8\text{ mm}^2$
Power Consumption	$19\text{ mW}$	$64.5\text{ }\mu\text{W}$	$31\text{ }\mu\text{W}$	$13\text{ mW}$	$159\text{ }\mu\text{W}$
Temperature Range	-45 to $105^{\circ}\text{C}$	-45 to $125^{\circ}\text{C}$	-40 to $85^{\circ}\text{C}$	-40 to $85^{\circ}\text{C}$	-45 to $130^{\circ}\text{C}$
Conversion Time	5ms	0.1ms	32ms	100ms	2.2ms
Resolution	$0.02\text{ mK}$	$10\text{ mK}$	$2.8\text{ mK}$	$0.1\text{ mK}$	$3\text{ mK}$
FOM	$0.04\text{ pJK}^2$	$0.65\text{ pJK}^2$	$8\text{ pJK}^2$	$13\text{ pJK}^2$	$3.2\text{ pJK}^2$

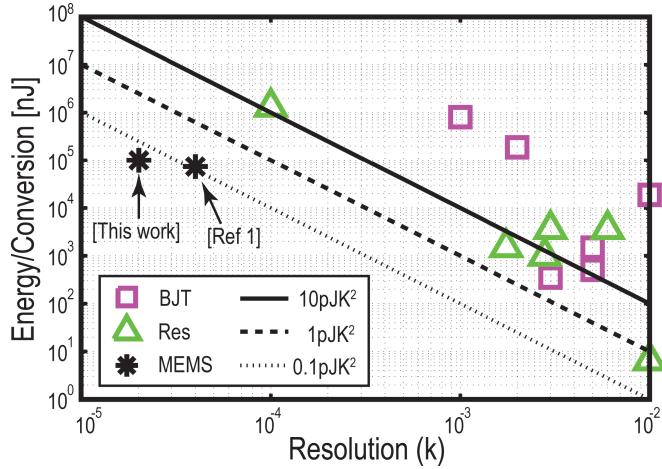


Fig. 16. Energy/conversion versus resolution for different types of high-resolution temperature sensors.

frequency range, its contribution was amplified through a digital gain stage in the TDC datapath. For the device under test,  $Clk_{TF}$  has a temperature sensitivity of  $0.9\text{ ppm/K}$ , requiring a slope of  $-0.9\text{ ppm/K}$  at the TDC output to ensure that

the output clock frequency remains stable. A 24-dB gain in the TDC datapath changes this sensitivity to  $-15.8\text{ ppm/K}$ , resulting in an output frequency stability of  $-14.9\text{ ppm/K}$ . This analysis is verified by slightly varying temperature and measuring the output frequency, as shown in Fig. 15(b). Furthermore, the output clock PN measurement in this mode also confirms the existence of 24 dB higher noise between 200 Hz and 2 kHz, which can be extended to low offset frequencies as well. Thus, by subtracting 24 dB from this PN and applying the effect of the low-pass filter, which was bypassed during this measurement, the exact TDC contribution can be found.

This measurement precisely reveals the relationship between the environmental temperature variation and the output clock frequency and phase. Hence, the TDC's resolution can be accurately estimated by passing the TDC noise contribution into this transfer function to find out its input referred noise. Accordingly, the dual-MEMS-resonator temperature sensor proves to have a resolution of  $20\text{ }\mu\text{K}$  over a BW of 100 Hz, resulting in a resolution FOM of  $0.04\text{ pJK}^2$ . Compared with our previous work [1], this chip represents a  $3\times$  improvement, which results from reducing the contribution of the oscillators' sustaining circuits on the TDC output noise. This is achieved by optimizing the size of the devices used in the voltage

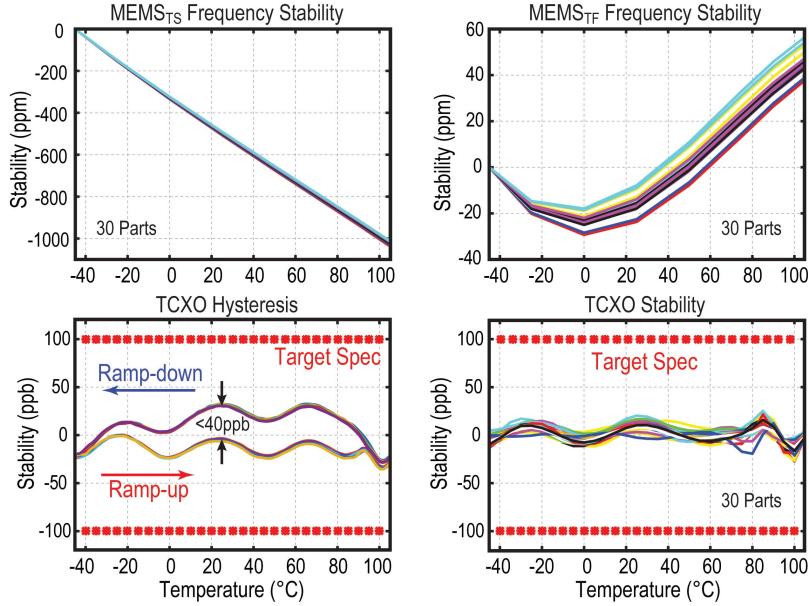


Fig. 17. Measurement results for MEMSTF, MEMSTS, and the output clock frequency stability for TCXO parts as well as the hysteresis test result for the output clock frequency of a TCXO device.

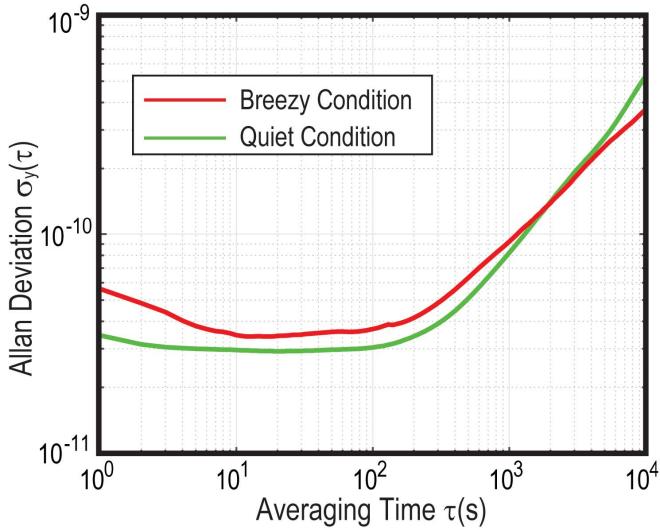


Fig. 18. ADEV measurement result for a TCXO device in both breezy and quiet environments.

regulators of the oscillators for better noise performance. It also exhibits a  $16\times$  improvement, when compared with the state-of-the-art temperature sensor, published to date [23]. Fig. 16 demonstrates the position of this work in the resolution FOM plot along with the other high-resolution temperature sensors. As shown, this TDC simultaneously improves both the resolution and the temperature tracking BW. Its detailed performance is summarized in Table I and compared with other best-in-class temperature sensors.

#### B. Programmable Oscillator's Performance Measurement

Fig. 17 depicts the measured stability for both the MEMSTF and MEMSTS resonators for 30 parts over a temperature range from  $-45^{\circ}\text{C}$  to  $105^{\circ}\text{C}$ . In XO mode, the output clock

stability follows the MEMSTF stability, around  $\pm 50$  ppm. However, based on the measurement result plotted in Fig. 17, the programmable oscillator in the TCXO mode successfully achieves a stability of  $<\pm 0.1$  ppm over the entire temperature range. Fig. 17 also includes the hysteresis measurement result for one TCXO device, over six temperature cycles with a temperature ramp rate of  $1^{\circ}\text{C}/\text{min}$ , which shows a window of less than 40 ppb. Fig. 18 plots the ADEV measurement results for one TCXO part in both breezy and quiet environmental conditions. According to the result, the oscillator achieves an ADEV of  $0.3\text{e}^{-10}$  over 1 s averaging time in quiet conditions. This number increases to  $0.5\text{e}^{-10}$  when the part is exposed to the oven airflow, still well below the  $1\text{e}^{-10}$  target ADEV. The ADEV degradation is mainly due to high-frequency temperature noise content present in the climate chamber that the TDC cannot track.

## V. CONCLUSION

This paper presented the first fully integrated dual-MEMS-resonator temperature sensor. It achieves a resolution of  $20\ \mu\text{K}$  over a BW of 100 Hz and results in a resolution FOM of  $0.04\ \text{pJ}\text{K}^2$ . It enabled us to realize a MEMS-based programmable oscillator suitable for telecom applications. The sensor front-end in this TDC is composed of two MEMS resonators, MEMSTF and MEMSTS, with different temperature coefficients. A frequency ratio engine consisting of an analog PLL referenced to  $\text{Clk}_{\text{TF}}$  that is nested inside a digital PLL, and referenced to  $\text{Clk}_{\text{TS}}$  measures the frequency ratio of those two clocks. A polynomial is applied to the engine's output to extract the temperature information and properly adjust the PFM value of the frequency synthesizer in order to compensate for the variation of  $\text{Clk}_{\text{TF}}$  across temperature. A digital low-pass filter after the polynomial is used to attenuate the TDC noise above the desired BW. The key benefit of this technique

is the fact that the output noise of the temperature sensor is only set by the PNs of the input clocks and not by the frequency ratio engine, thereby offering a high resolution. In addition, this topology is robust against aging, as it operates based on two feedback loops that force the output to be always a function of the frequencies of the input clocks. This unique specification makes this circuit a reliable candidate for critical applications like base stations, where the part must work over a long time without any drift.

## REFERENCES

- [1] M. H. Roshan *et al.*, "Dual-MEMS-resonator temperature-to-digital converter with 40  $\mu\text{K}$  resolution and FOM of 0.12  $\text{pJ}\text{K}^2$ ," in *IEEE ISSCC Dig. Tech. Papers*, Jan. 2016, pp. 200–201.
- [2] *WirelessUSBTM Crystal Guidelines, AN19219*. [Online]. Available: <http://www.cypress.com/file/134326/download>
- [3] *Datasheet, ASTXR-12*. [Online]. Available: <http://www.abracon.com/Oscillators/ASTXR-12.pdf>
- [4] M. Weiss. (2012). *Telecom Requirements for Time and Frequency Synchronization*. [Online]. Available: <http://www.gps.gov/cgsic/meetings/2012/weiss1.pdf>
- [5] *IEEE 1588TM Telecommunications Applications*. [Online]. Available: <http://www.nist.gov/el/isd/ieee/upload/tutorial-telcom.pdf>
- [6] D. Ruffieux, F. Krummenacher, A. Pezous, and G. Spinola-Durante, "Silicon resonator based 3.2  $\mu\text{W}$  real time clock with  $\pm 10$  ppm frequency accuracy," *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 224–234, Jan. 2010.
- [7] D. Ruffieux *et al.*, "A  $3.2 \times 1.5 \times 0.8 \text{ mm}^3$  240 nA 1.25-to-5.5V 32 kHz-DTCXO RTC module with an overall accuracy of  $\pm 1$  ppm and an all-digital 0.1 ppm compensation-resolution scheme at 1 Hz," in *IEEE ISSCC Dig. Tech. Papers*, Jan. 2016, pp. 208–209.
- [8] S. Zaliasl *et al.*, "A 3 ppm  $1.5 \times 0.8 \text{ mm}^2$  1.0  $\mu\text{A}$  32.768 kHz MEMS-based oscillator," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 291–302, Jan. 2015.
- [9] M. H. Perrott *et al.*, "A temperature-to-digital converter for a MEMS-based programmable oscillator with  $<\pm 0.5$ -ppm frequency stability and  $<1$ -ps integrated jitter," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 276–291, Jan. 2013.
- [10] H. Lee, A. Partridge, and F. Assaderaghi, "Low jitter and temperature stable MEMS oscillators," in *Proc. IEEE Int. Freq. Control Symp. (FCS)*, May 2012, pp. 1–5.
- [11] A. Kourani, E. Hegazi, and Y. Ismail, "RF MEMS reference oscillator platform with  $\pm 0.5$ ppm frequency stability for wireless handsets," in *Proc. Int. Symp. Signals, Circuits Syst. (ISSCS)*, Jul. 2015, pp. 1–4.
- [12] A. Partridge, H.-C. Lee, P. Hagelin, and V. Menon, "We know that MEMS is replacing quartz. But why? And why now?" in *Proc. Joint Eur. Freq. Time Forum Int. Freq. Control Symp.*, Jul. 2013, pp. 411–416.
- [13] Electronic Design. *MEMS Oscillators Replace Quartz Crystal Oscillators*. [Online]. Available: <http://electronicdesign.com/communications/mems-oscillators-replace-quartz-crystal-oscillators>
- [14] SiTime Corp. *MEMS First Process*. [Online]. Available: <http://www.sitime.com/support2/documents/AN20001-MEMS-First-Process.pdf>
- [15] X. Huang, D. Liu, Y. Wang, P. Chen, and W. Fu, "100-MHz low-phase-noise microprocessor temperature-compensated crystal oscillator," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 7, pp. 636–640, Jul. 2015.
- [16] Solid State Technology. (2009). *MEMS Resonators Vs. Crystal Oscillators for IC Timing Circuits*. [Online]. Available: <http://electroiq.com/blog/2009/01/mems-resonators-vs-crystal-oscillators-for-ic-timing-circuits/>
- [17] Digi-Key. (2014). *MEMS Oscillators Challenge Quartz Crystals in RF Applications*. [Online]. Available: <http://www.digikey.com/en/articles/techzone/2014/oct/mems-oscillators-challenge-quartz-crystals-in-rf-applications>
- [18] SiTime. *Shock and Vibration Performance Comparison of MEMS and Quartz-Based Oscillators*. [Online]. Available: <http://www.sitime.com/support2/documents/AN10032-Shock-Vibration-Comparison-MEMS-and-Quartz-Oscillators.pdf>
- [19] SiTime. *Resilience and Reliability of Silicon MEMS Oscillators*. [Online]. Available: <http://www.sitime.com/support2/documents/AN10045-SiTme-Resilience-Reliability-MEMS-Oscillators.pdf>
- [20] S. Bregni, "Clock stability characterization and measurement in telecommunications," *IEEE Trans. Instrum. Meas.*, vol. 46, no. 6, pp. 1284–1294, Dec. 1997.
- [21] Allan's TIME. *The Allan Variance*. [Online]. Available: <http://www.allanstime.com/AllanVariance/>
- [22] K. A. A. Makinwa. *Smart Temperature Sensor Survey*. [Online]. Available: [http://ei.ewi.tudelft.nl/docs/TSensor\\_survey.xls](http://ei.ewi.tudelft.nl/docs/TSensor_survey.xls)
- [23] C.-H. Weng, C.-K. Wu, and T.-H. Lin, "A CMOS thermistor-embedded continuous-time delta-sigma temperature sensor with a resolution FoM of 0.65  $\text{pJ} \text{ }^\circ\text{C}^2$ ," *IEEE J. Solid-State Circuits*, vol. 50, no. 11, pp. 2491–2500, Nov. 2015.
- [24] C.-H. Weng, C.-K. Wu, and T.-H. Lin, "A CMOS thermistor-embedded continuous-time delta-sigma temperature sensor with a resolution of 0.01  $^\circ\text{C}$ ," in *Proc. IEEE ASSCC*, Nov. 2014, pp. 149–152.
- [25] A. Heidary, G. Wang, K. Makinwa, and G. Meijer, "A BJT-based CMOS temperature sensor with a 3.6pJ-K<sup>2</sup>-resolution FoM," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 224–225.
- [26] E. J. Ng, H. K. Lee, C. H. Ahn, R. Melamud, and T. W. Kenny, "Stability of silicon microelectromechanical systems resonant thermometers," *IEEE Sensors J.*, vol. 13, no. 3, pp. 987–993, Mar. 2013.
- [27] J. R. Vig, "Dual-mode oscillators for clocks and sensors," in *Proc. IEEE Ultrason. Symp.*, Oct. 1999, pp. 859–868.
- [28] A. Partridge, B. Boser, C. Y. Lu, M. Lutz, and P. M. Hagelin, "Microelectromechanical oscillator and method of operating same," U.S. Patent 7,369,004, May 6, 2008.
- [29] P. Park, D. Ruffieux, and K. A. A. Makinwa, "A thermistor-based temperature sensor for a real-time clock with  $\pm 2$  ppm frequency stability," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1571–1580, Jul. 2015.
- [30] T. Anand, K. A. A. Makinwa, and P. K. Hanumolu, "A self-referenced VCO-based temperature sensor with 0.034  $^\circ\text{C}/\text{mV}$  supply sensitivity in 65 nm CMOS," in *VLSI Circuits Symp. Dig.*, Jun. 2015, pp. C200–C201.
- [31] M. H. Perrott, M. D. Trott, and C. G. Sodini, "A modeling approach for  $\Sigma$ - $\Delta$  fractional- $N$  frequency synthesizers allowing straightforward noise analysis," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 1023–1038, Aug. 2002.
- [32] M. S.-W. Chen, D. Su, and S. Mehta, "A calibration-free 800MHz fractional- $N$  digital PLL with embedded TDC," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 472–473.
- [33] M. Koskenvuori, V. Kaajakari, T. Mattila, and I. Tittonen, "Temperature measurement and compensation based on two vibrating modes of a bulk acoustic mode microresonator," in *Proc. IEEE 21st Int. Conf. Micro Electro Mech. Syst. (MEMS)*, Jan. 2008, pp. 78–81.
- [34] J. C. Salvia, R. Melamud, S. A. Chandorkar, S. F. Lord, and T. W. Kenny, "Real-time temperature compensation of MEMS oscillators using an integrated micro-oven and a phase-locked loop," *J. Microelectromech. Syst.*, vol. 19, no. 1, pp. 192–201, Feb. 2010.
- [35] R. Melamud *et al.*, "MEMS enables oscillators with sub-ppm frequency stability and sub-ps jitter," in *Proc. Hilton Head*, 2012, pp. 66–69.



**Meisam Heidarpour Roshan** received the B.S. degree from the University of Mazandaran, Babol, Iran, in 2006, the M.S. degree from the Sharif University of Technology, Tehran, Iran, in 2008, and the Ph.D. degree from The University of Texas at Dallas, Richardson, TX, USA, in 2016, all in electronics engineering.

He was a Design Engineer with Dongbu Hitek, Dallas, TX, USA, from 2011, where he was involved in developing high-performance hybrid TV tuners. Since 2014, he has been serving as a Senior Analog/Mixed Signal IC Designer at SiTime, Sunnyvale, CA, USA, designing frequency synthesizers and temperature sensors for high-precision MEMS-based programmable oscillators. His current research interests include the design of precision analog/mixed signal integrated circuits, frequency synthesizers, and high-speed data converters.



**Samira Zaliasl** received the B.S. degree in electrical and computer engineering from the University of Tehran, Tehran, Iran, in 2008, and the Ph.D. degree in electrical engineering from Oregon State University, Corvallis, OR, USA, in 2014. Her doctoral dissertation focused on architectural solutions for nonidealities in delta-sigma-based modulators.

She joined SiTime Corporation, Sunnyvale, CA, USA, in 2012, where she developed analog/mixed signal circuitry for high-performance

MEMS timing references. Since 2014, she has been with the Wearable Health Solution Division, imec, Eindhoven, The Netherlands, developing new monitoring technology for ultralow-power biomedical applications.



**Kimo Joo** received the B.S.E.E. degree in computer engineering from Pusan National University, South Korea, in 1994.

Since 1994, he has been a Digital Design Engineer with several companies. He was with Samsung Electronics, South Korea, for eight years, where he mainly developed sigma-delta ADC/DAC for audio applications. He was also with Eastman Kodak for two years in charge of image

signal processing development for CMOS sensors. In 2011, he joined SiTime Corporation, Sunnyvale, CA, USA, designing MEMS-based high-performance CMOS circuits for timing reference chips. He is currently working on temperature compensation and sigma-delta modulators for fractional PLL.



**Kamran Souri** received his M.Sc. (*cum laude*) from the Electronic Instrumentation Laboratory, Delft University of Technology, in 2009. Between 2009 and 2014 he was a Ph.D. candidate in the same faculty, focusing on the design of ultralow-power/energy-efficient CMOS smart temperature sensors for RFID applications.

He is currently a Principal Circuit Designer with SiTime Corporation, Sunnyvale, CA, USA, where he is working on circuit design for MEMS-based (temperature-compensated) oscillators. His current

research interests include the design of low-power, energy-efficient sensor interfaces, data converters, precision analog and reference circuits.

Dr. Souri was a recipient of the IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award, 2012–2013.



**Rajkumar Palwai** received the M. Eng. degree from the Indian Institute of Science, Bengaluru, India, in 2007.

He joined Texas Instruments, Bengaluru, India, where he worked on PLLs based on LC and ring VCOs as well as high-speed pipeline ADCs. He is currently with SiTime Corporation, Sunnyvale, CA, USA, where he is working on the development of high-performance and low-power fractional PLLs and MEMS-based oscillators. His current research interests include high-speed and precision analog circuits in general and more specifically PLLs, oscillators, and temperature-to-digital converters.



based high-performance

**Lijun (Will) Chen** received the B.S.E.E. degree from Xian Jiaotong University, Xi'an, China, in 1995, and the M.S.E.E. degree from Tsinghua University, Beijing, China, and Oregon State University, Corvallis, OR, USA, in 1998 and 2000, respectively.

Since then, he has held analog/RF design positions with various companies, including Xicor, Chrontel, Entropic Communications, Sigma designs, and Siport. He is currently with SiTime Corporation, Sunnyvale, CA, USA, where he is designing MEMS-CMOS circuits for timing reference chips.



**Amanpreet Singh** received the B.Tech. degree in electronics and communication engineering from Punjab Technical University, Jalandhar, India, and the M.S. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA.

He has held several analog design engineering positions with Semtech Inc., San Jose, CA, USA, AMD Inc., Santa Clara, CA, and Freescale Semiconductors Ltd., Noida, India. He is currently with SiTime Corporation, Sunnyvale, CA, where he is working on low-power analog and high-speed drivers. His current research interests include analog and digital PLLs, high-speed transceivers, and low-power data converters.



**Sudhakar Pamarti** received the Bachelor degree in electronics and electrical communication engineering from IIT Kharagpur, Kharagpur, India, in 1995, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, San Diego, CA, USA, in 1999 and 2003, respectively.

He is currently an Associate Professor of electrical engineering with the University of California, Los Angeles, CA, USA. He was with Rambus Inc. from 2003 to 2005 and Hughes Software Systems from 1995 to 1997 developing high-speed I/O circuits and embedded software and firmware for a wireless-in-local-loop communication system.

Dr. Pamarti was a recipient of the National Science Foundation CAREER Award for developing digital signal conditioning techniques to improve analog, mixed-signal, and radio frequency integrated circuits. He currently serves as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS.



**Nicholas J. Miller** received the B.S.E. degree in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2003, and the M.S. and Ph.D. degrees in mechanical engineering from Michigan State University, East Lansing, MI, USA, in 2007 and 2012, respectively.

He was previously a Post-Doctoral Researcher with Carnegie Mellon University, Pittsburgh, PA, USA. He has been a MEMS Development Engineer with SiTime, Sunnyvale, CA, USA, since 2013. His current research interests include nonlinear dynamics in microelectromechanical resonators.



**Joseph C. Doll** received the B.S. degree in mechanical engineering from the University of California, Berkeley, Berkeley, CA, USA, in 2006, and the M.S. and Ph.D. degrees in mechanical engineering from Stanford University, Stanford, CA, USA, in 2009 and 2012, respectively. His research was supported by a National Science Foundation Fellowship and National Defense Science and Engineering Graduate Fellowship.

He was a MEMS Designer with SiTime from 2012 to 2016, and is currently a Sensor System Architect with Apple.



**Carl Arft** received the B.S. degree in electrical engineering from Michigan Technological University, Houghton, MI, USA, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Davis, CA, USA.

He has over 15 years of experience with microelectromechanical systems (MEMS) research and development. He served as a Faculty Fellow with the University of California. He held technology development roles at several optical MEMS start-up companies, including C Speed

Corporation and Newport Opticom. He is currently a Senior Director of Systems Engineering with SiTime Corporation, and the World Leader in MEMS-based timing devices.



**Sasan Tabatabaei** received the Ph.D. degree in electrical engineering from the University of British Columbia, Vancouver, BC, Canada, in 2000.

He has been with SiTime for eight years. He has been directing circuit design with SiTime since 2014, where he is responsible for IC architectural definitions and development of various timing products, including uW TCXOs for mobile as well as precision TCXO for telecom applications. He held executive and technical management positions at a several start-up companies before joining SiTime in US patents. His current research interests include circuit design/architecture, signal integrity, timing, jitter, clocking analysis, instrumentation, and test.

2008. He holds several analog and mixed-signal US patents. His current research interests include circuit design/architecture, signal integrity, timing, jitter, clocking analysis, instrumentation, and test.



**Carl Sechen** (F'02) received the B.E.E. degree from the University of Minnesota, Minneapolis, MN, USA, the M.S. degree from the Massachusetts Institute of Technology, Cambridge, MA, USA, and the Ph.D. degree from the University of California, Berkeley, CA, USA, in 1975, 1977, and 1986, respectively.

He was an Assistant and then Associate Professor with the Department of Electrical Engineering, Yale University, New Haven, CT, USA, in 1986. From 1992 to 2005, he was an Associate Professor and then Professor with the Department of Electrical Engineering, University of Washington, Seattle, WA, USA. Since 2005 he has been a Professor with the Electrical Engineering Department, University of Texas at Dallas, Richardson, TX, USA. He directs the Nanometer Design Laboratory at UT Dallas, which includes eight Ph.D. students. In 30 years as a Professor, he has graduated 28 Ph.D. students. He has authored one book, two patents, and authored or co-authored over 180 research papers. His current research interests include the design and computer-aided design of digital and analog integrated circuits.

Dr. Sechen received the Distinguished Teaching Award for the Erik Jonsson School of Engineering and Computer Science, University of Texas at Dallas, 2014, the Distinguished Teacher of the Year Award, Department of Electrical Engineering, Erik Jonsson School of Engineering and Computer Science, University of Texas at Dallas in 2008, the Semiconductor Research Corporation's Inventor's Recognition Award in 2001 for his development of output prediction logic, the 1994 SRC Technical Excellence Award, the Semiconductor Research Corporation's 1988 SRC Inventor's Award, and the Outstanding Research Advisor Award from the Department of Electrical Engineering, University of Washington, in 2002. He is a co-founder of TimberWolf Systems Inc. He also received the Best Project Award from the National Science Foundation's Center for the Design of Digital and Analog ICs in 2002. He developed the first version of the TimberWolf placement and routing package in 1983. Versions of TimberWolf that he developed at UC Berkeley, Yale University, and the University of Washington were used in production at more than 20 companies and were used at more than 25 universities.



**Aaron Partridge** received the B.S., M.S., and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 1996, 1999, and 2003, respectively. His thesis was on MEMS accelerometers for the NASA X-33 space plane and the first thin-film encapsulated piezoresistive accelerometers.

From 1987 to 1991, he was a founder and Chief Scientist of Atomis, Inc., Berkeley, CA, USA, a manufacturer of scanning tunneling microscopes, atomic force microscopes, and ballistic emission electron microscopes. From 2001 to 2004, he was a Project Manager with the Robert Bosch Research and Technology Center, Palo Alto, CA, USA, where he coordinated the MEMS resonator and packaging research. He is currently a founder and Chief Scientist of SiTime Corporation, Sunnyvale, CA, USA, where he guides the technological direction. He has authored or co-authored 30 scientific papers and holds 70 patents.

Dr. Partridge has served on the IEEE International Solid-State Circuits Conference Imagers, MEMS, Medical and Displays Subcommittee. He is the Editorial Chair of the IEEE International Frequency Control Symposium, and is an Associate Editor of the IEEE TRANSACTIONS ON ULTRASONICS, FERROELECTRICS, AND FREQUENCY CONTROL.



**Vinod Menon** received the B.Tech. degree in electrical engineering from IIT Mumbai, Mumbai, India, and the M.S. degree in electrical and computer engineering from the University of California, Santa Barbara, CA, USA.

Since 2012, he has been an Executive Vice President of Engineering at SiTime. He has over 30 years of semiconductor industry experience leading international IC development organizations and delivering innovative high-value products. He was the VP, Serial Interface & Protocols Solutions at LSI Corporation acquired by Avago, now Broadcom, where he led High-Speed SerDes, Analog Mixed-Signal, Ethernet PHY, and Protocol IP developments for 65/40/28 nm ASICs and ASSPs. Before joining LSI, he was a Business Unit and Engineering Director with National Semiconductor (acquired by Texas Instruments), where he led the successful turnaround of the Interface Division and delivered multiple generations of high-performance analog BiCMOS and CMOS products, including precision timing solutions. He directed product developments for wired and wireless networking, and storage connectivity at Advanced Micro Devices.