

# Frequency Reconfigurable mm-Wave Power Amplifier With Active Impedance Synthesis in an Asymmetrical Non-Isolated Combiner: Analysis and Design

Chandrakanth R. Chappidi, *Student Member, IEEE*, and Kaushik Sengupta, *Member, IEEE*

**Abstract**—A frequency reconfigurable millimeter-wave (mm-wave) power amplifier (PA), which can be programmed to operate efficiently for a wide swathe of the spectrum, approaching an universal transmitter, can enable a wide range of novel applications in high-speed communication, sensing, and imaging. Classical techniques to allow large operating range either rely on broadband higher order output combining networks or tunable passives, both of which tradeoff directly with output power and efficiency. In this paper, we present an active impedance synthesis methodology that exploits the interaction of multiple unit PA cells in an asymmetrical non-isolated combiner to synthesize complex mm-wave impedances in a programmable fashion. This allows the interacting power cells to see their optimal load-pull impedances for high-efficiency frequency-reconfigurable operation in an efficient combiner network with no lossy variable passives. Compared to a symmetrical combiner, this enables the network to break the strong tradeoffs between output power, efficiency, and frequency reconfigurability, allowing it to achieve  $N$  times the Bode-Fano bound compared with an  $N$ -way symmetrical architecture. As a proof of concept, an integrated PA, which is in a  $0.13\text{-}\mu\text{m}$  SiGe process, is demonstrated to achieve  $P_{\text{sat}}$  of  $23.6\text{ dBm}$  at a power-added efficiency (PAE) of  $27.7\%$  at  $55\text{ GHz}$  with a frequency reconfigurable  $P_{\text{sat},-1\text{ dB}}$  bandwidth of  $25\text{ GHz}$  ( $40\text{--}65\text{ GHz}$ ) and a PAE, $-1\text{ dB}$  bandwidth of  $20\text{ GHz}$  ( $40\text{--}60\text{ GHz}$ ). Multi-Gbps data rates are demonstrated with non-constant envelope modulations across the frequencies  $40\text{--}60\text{ GHz}$ .

**Index Terms**—Bandwidth, Bode-Fano, broadband, combiner, load-pull, loss, millimeter-wave (mm-wave), multi-port, networksynthesis, power amplifier (PA), SiGe.

## I. INTRODUCTION

THE rapid evolution of millimeter-wave (mm-wave)-integrated technology has demonstrated tremendous application potential across multiple fields from sensing and imaging, gesture recognition to short-range high-speed data communication, mobile backhauls, and last-mile connectivity [1]. With the future deployment of 5G mm-wave wireless communication, continued evolution of 60-GHz short-range high-speed wireless links, 77-GHz automotive radar

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The authors are with the Integrated Micro-system Research Lab, Department of Electrical Engineering, Princeton University, Princeton, NJ 08544 USA (e-mail: chappidi@princeton.edu; kaushiks@princeton.edu).

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and sensing, the mm-wave spectrum is expected to experience proliferation in its usage spanning over a large portion. As an example, as larger non-contiguous chunks of the mm-wave spectrum open up for communication, deploying large-scale MIMO arrays with dedicated, multiple, narrow-band Tx architectures to address the various bands is inefficient and non-scalable. In addition to the availability of wide bandwidth at a single carrier frequency, hyper-spectral imaging and multi-band communication can also fuel novel application development in the frequency range. In order to fully utilize the mm-wave spectrum with high efficiency for all these applications, frequency-reconfigurable transceiver architectures are needed, which can be programmed to operate efficiently across a broad swathe of the frequency range, in the limit approaching universal front ends. This paper focuses on a programmable transmitter architecture, particularly the power amplifier (PA). We propose methods to enable frequency-flexible PA architectures, which can be reconfigured to operate near-optimally over a wideband of mm-wave frequencies without lossy variable passive elements, and does not suffer from the usual tradeoffs between output power, efficiency, and frequency reconfigurability.

Lower breakdown voltages of active devices, lower  $f_t$  and  $f_{\text{max}}$ , and lower power gain and quality factor of on-chip passives in silicon make efficient and high-power on-chip signal generation at mm-wave frequencies with high linearity extremely challenging. In general, for optimal power generation, the load-pull impedance for the PA is transformed from  $50\ \Omega$  through a passive matching network, which limits the bandwidth and frequency of operation of a PA [2]–[4]. This transformation ratio increases for higher power generation with multiple combining cells, which typically degrades operable bandwidth as well as the efficiency of the matching network [5]. These result in strong tradeoff between output power, efficiency, and bandwidth. Fig. 1(a) shows a typical combining architecture where multiple identical PAs are driven symmetrically through a passive combiner to achieve power combination and impedance transformation simultaneously at the desired frequency of operation [6]–[10]. Ideally, with variable passive elements, the matching network can be tuned over the frequency of operation. However, the loss and tuning range of variable passive elements at mm-wave frequencies are prohibitive and severely limit efficiency and frequency reconfigurability [4]. An alternative method to realize efficient

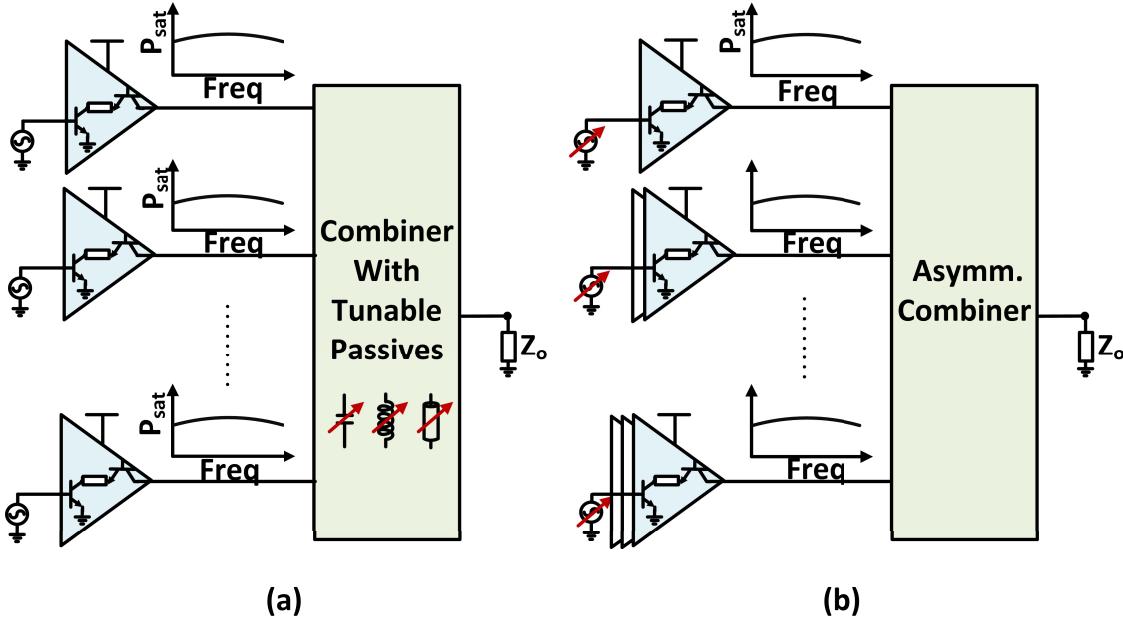


Fig. 1. (a) Classical symmetrical combining architecture with variable tunable passives for frequency-reconfigurable operation. (b) Proposed asymmetrical architecture with programmable driving conditions to enable active impedance synthesis for optimal frequency-reconfigurable operation without lossy variable passives.

operation across frequencies for the aforementioned applications is to enable instantaneous broadband operation. This is achieved by employing higher order networks at the output that enable passive synthesis of the optimal load-pull impedance across the frequencies [11], [12]. However, realizing such complex combiner networks with a larger number of passives, also typically trades off with efficiency. In addition these, can induce undesirable mutual coupling and be area-intensive. Techniques such as staggering and distributed amplification for PAs can also be inefficient at mm-wave frequencies [13], [14]. To mitigate these issues, we propose a network synthesis approach to achieve a programmable transmitter front end. The contribution of this paper is as follows.

- 1) We propose an active impedance synthesis method over an asymmetrical combining PA architecture that can be programmed to operate near-optimally over a wide range of mm-wave frequencies with a low-order and efficient output combiner. The architecture allows us to actively reconfigure the output impedances of the combining cells to match their optimal load-pull impedances over the operable spectrum for high-efficiency power generation [Fig. 1(b)], enabling simultaneously a frequency-programmable, efficient, and high-power PA.
- 2) We show analytical methods for the proposed network synthesis approach and demonstrate illustrative examples to highlight the key features.
- 3) The proposed architecture is extensively compared with the traditional symmetrical combining approach, focusing on the classical tradeoffs between power, efficiency, and frequency reconfigurability. The Bode–Fano limit of an  $N$ -way asymmetrical architecture is shown to be  $N$  times that of a symmetrical architecture, which allows the frequency reconfigurability property.

- 4) As a proof-of-concept, a silicon-based integrated PA in a  $0.13\text{-}\mu\text{m}$  SiGe process is demonstrated to achieve  $P_{\text{sat}}$  of  $23.6\text{ dBm}$  at a power-added efficiency (PAE) of  $27.7\%$  at  $55\text{ GHz}$  with a frequency reconfigurable  $P_{\text{sat},-1\text{ dB}}$  bandwidth of  $25\text{ GHz}$  ( $40\text{--}65\text{ GHz}$ ) and a PAE $_{-1\text{ dB}}$  bandwidth of  $20\text{ GHz}$  ( $40\text{--}60\text{ GHz}$ ). Multi-Gbps data rates are demonstrated with non-constant envelope modulations across the frequencies  $40\text{--}60\text{ GHz}$ .

This paper is organized as follows. Section II presents the limitations of traditional architectures and methods for frequency-flexible operation of PAs. Section III describes the concept of active impedance synthesis and frequency re-configurability. Section IV discusses the methodology of synthesis of such an architecture, while Section V discusses the design tradeoffs and properties. The design and implementation of a proof-of-concept PA in  $0.13\text{-}\mu\text{m}$  SiGe BiCMOS process and measurement results are described in Sections VI and VII, respectively.

## II. ARCHITECTURES FOR FREQUENCY-RECONFIGURABLE OPERATION

Fig. 2 shows the output power ( $P_{\text{out}}$ ) and PAE of reported state-of-the-art mm-wave PAs in silicon processes [6]–[43]. While recent works have demonstrated mm-wave power generation near the Watt-level range, the operable frequency ranges of these topologies are still limited by the bandwidth of the output matching network [2]. For a PA to generate maximum power with the highest efficiency over a wide range of the spectrum, it needs to see the changing optimal load-pull impedance over that range. This can be achieved with a multi-order broadband impedance transformation network that allows the impedance presented to the PA cells to be moved closer to the load-pull path as shown in Fig. 3. Synthesis of such multi-order wideband network is not unique but can

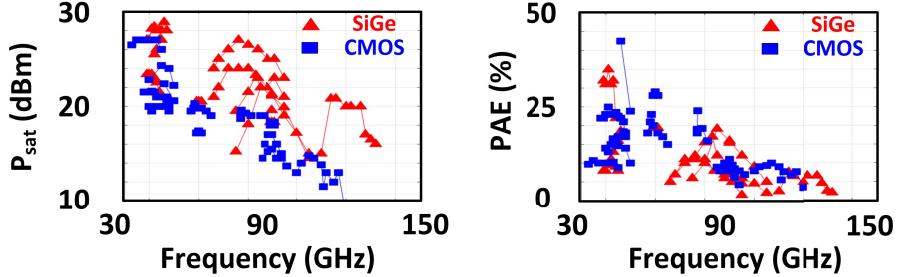


Fig. 2. Output power and PAE of the reported state-of-the-art mm-wave PAs in silicon. The solid line corresponds to the data from one PA.

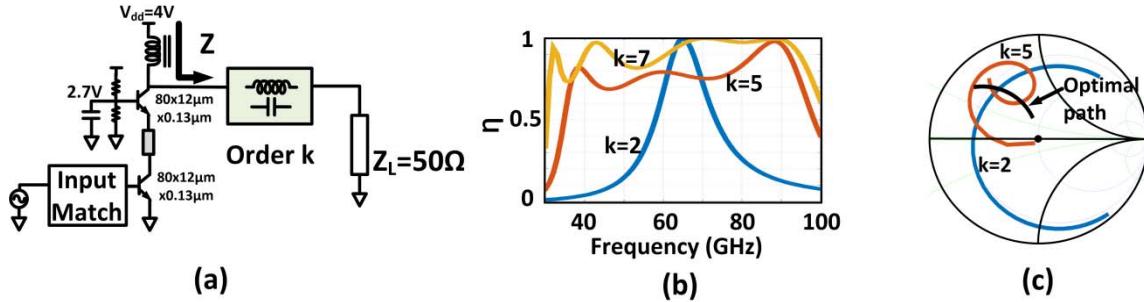


Fig. 3. Broadband design of PA. (a) Example of a unit PA cell with stacked architecture with simulated optimal  $P_{\text{out}} \approx 4\text{W}$  at 55 GHz. (b) Variation of power delivery efficiency ( $\eta = \frac{P_L}{P_{\text{av}}}$ ) for lossless networks of different orders ( $k$ ) across frequencies from the unit PA cell. (c) Optimal load-pull path against frequency. The figure also shows impedance paths followed by matching networks with increasing order  $k$ . The higher order networks converge to the optimal path demonstrating broadband operation.

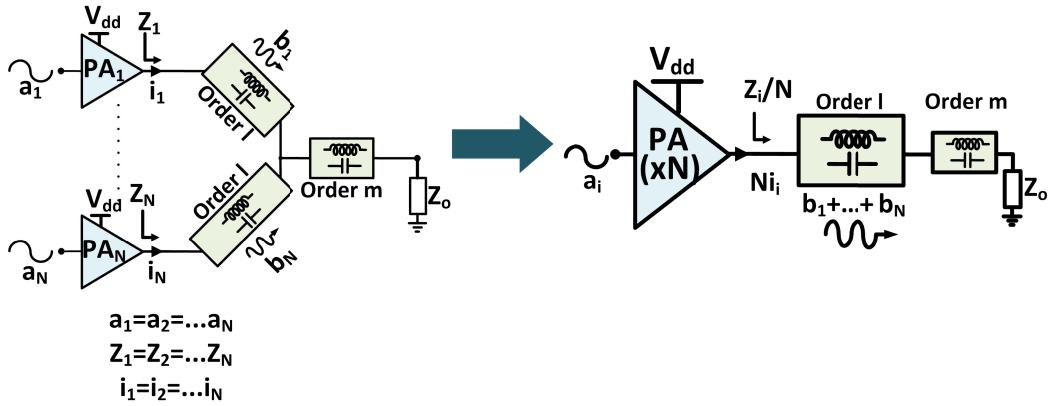


Fig. 4. Traditional current combined  $N$ -way symmetrical PA architecture is functionally similar to a single larger PA (of size  $xN$ ) with a matching network of order  $k = l + m$ .

be realized with known filter synthesis methods [44]–[47]. However, it is also known that, for lossy passives, the efficiency of the network, typically, trades off with the order of the network, especially for the higher impedance transformation ratio required for high output power. In general, there exists strong tradeoffs between  $P_{\text{out}}$ , efficiency ( $\eta$ ), and the frequency range of operation.

#### A. Broadband Multi-Order Symmetrical Power-Combining Architecture

Before, we elaborate on the concept of active impedance synthesis, let us review a classical symmetrical power combining architecture. At mm-wave frequencies, due to the

limited output power available from a single device, multiple identical PA unit cells are driven symmetrically and power is combined through a symmetrical combining network either in voltage or current domain. Fig. 4 shows such an example of an  $N$ -way current-combined architecture with the matching networks of order  $l$  in each branch and of order  $m$  after the combined node. It can be noted that due to the symmetry of operation and architecture, the voltages and currents at all the intermediate nodes are identical, which allows the network to be functionally identical to one large PA ( $xN$  times the size of each unit cell) followed by the matching network of order  $l + m$ . Therefore, the design of such an architecture, which operates efficiently over a broad range

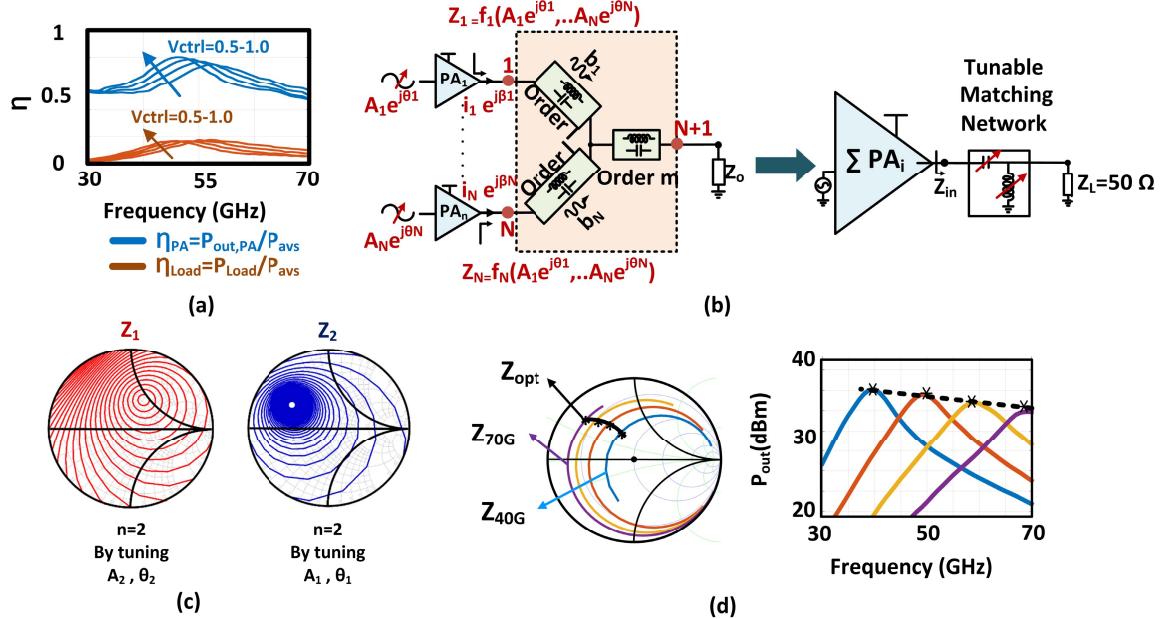


Fig. 5. (a) Efficiency degradation and tunability of PA with varactors. (b) Asymmetrical PA architecture with actively synthesized impedances for the combining cells that allows frequency-reconfigurable operation. (c) Example of impedance variation of one PA cell as the driving condition of the other PA cell is varied in an A-combiner. (d) Conceptual representation of the impedance variation and output power for the frequency-reconfigurable PA, which allows the architecture to trace the peaks of the individual plots for optimal operation across the range.

of mm-wave frequencies, suffers from the same tradeoffs between output power ( $P_{\text{out}}$ ), efficiency ( $\eta$ ), and the frequency range of operation.

### B. Tunable Matching Network

Ideally, a frequency reconfigurable PA could also be realized with a tunable matching network, which can be reconfigured to present the optimal impedance over the frequency range. However, at mm-wave frequencies, tuning elements, such as varactors, are extremely lossy ( $Q \approx 2$  for the NCap varactors in the mm-wave range), which significantly limits the range of tunability of such architecture. Hence this topology trades off directly with output power, efficiency, and tunability [Fig. 5(a)].

## III. FREQUENCY RECONFIGURABILITY THROUGH ACTIVE IMPEDANCE SYNTHESIS

### A. Concept of Active Impedance Synthesis

The identical nature of the symmetrical power combining architecture (S-combiner) and a single PA of size  $xN$  arises due to the symmetry of the combining network and the symmetry of the drive signals. The central concept behind active impedance synthesis is to forgo the symmetry of the architecture, the driving signals of the unit cells, and any isolation between them. As shown in Fig. 5(b), the complex RF currents from each PA cell combine in an asymmetrical network, which leads to the impedance seen by each cell as a function of the driving conditions of all the cells, i.e.,  $Z_i = f_i(A_1e^{j\theta_1}, A_2e^{j\theta_2}, \dots, A_Ne^{j\theta_N})$ . Therefore, the impedance at each port can be reconfigured by programming the RF driving conditions of the PA cells, and complex RF impedances can be synthesized actively at each output [48], [49]. The variation

is, of course, a function of the combiner itself, and the central premise of this paper addresses the design and analysis of such asymmetrical combining architectures that allow the required programmable impedance synthesis for frequency-reconfigurable operation. Fig. 5(c) shows an example of such impedance coverage with a two-way Asymmetrical combiner (A-combiner) with a stacked SiGe topology as a unit cell. We will discuss the synthesis of the combiner in Section IV; but as shown here, the impedance seen by one cell can be actively reconfigured over the entire Smith chart by controlling the driving condition of the other cell. Fig. 5(d) shows the conceptual representation of the impedance variation and output power ( $P_{\text{out}}$ ) of such a frequency-reconfigurable PA for various reconfiguration states across the range of operation. The goal is, for the PA, to be able to be programmed to trace the peaks of the individual efficiency curves for optimal operation across the range.

It can be understood that Doherty also exploits a specific form of dynamic interaction between two PA cells with a particular combiner topology to improve back-off efficiency. Therefore, such architectures and all variations of them are specific embodiments of possible networks, but of course, not necessarily the most optimal network for either back-off or for frequency reconfiguration, when losses are taken into account. This paper presents the generalized treatment of a class of frequency-reconfigurable networks, based on interacting PA cells in an  $N + 1$  port network, and presents its analysis, synthesis, properties, and bounds (Bode–Fano limit), including optimal driving conditions and extensive comparison with symmetrical networks.

In order to get some intuition, we first explore if a classical symmetrical architecture designed optimally at a given

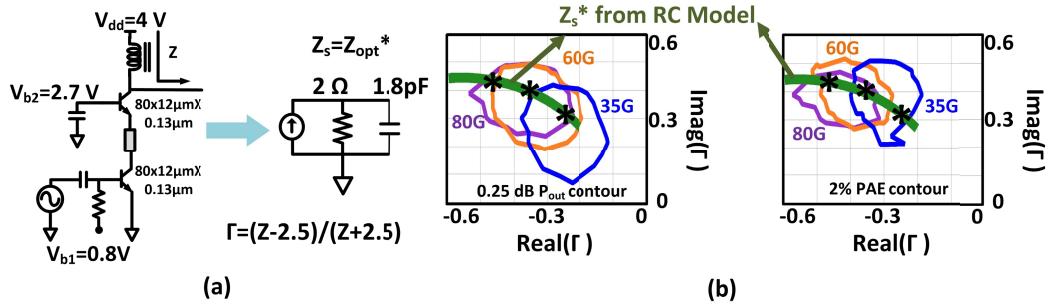


Fig. 6. (a) Linearized model of a PA output cell consisting of a stacked SiGe topology with intra-transistor matching for output network analysis and synthesis. (b) Comparison of optimal load-pull path ( $Z_{opt}$ ) obtained through nonlinear simulations against  $Z_s^*$  showing close correspondence and validity of the model for predicting  $Z_{opt}$  against frequency.

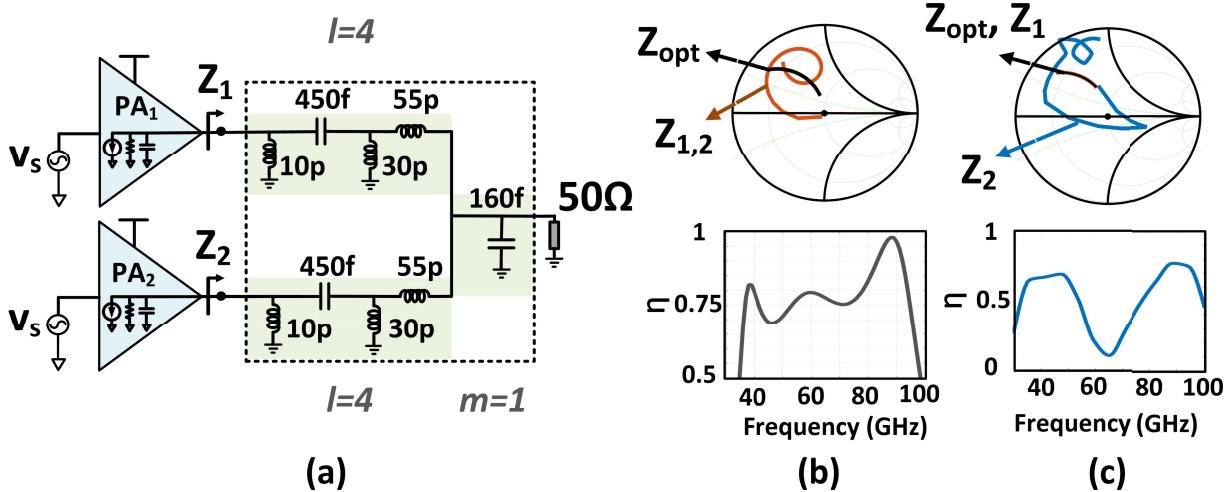


Fig. 7. (a) Example of an optimized two-way symmetrical architecture with a fifth order lossless network ( $k = l + m = 5$ ) with combined PA cell size identical to the one in Fig. 6. (b) Identical impedance path seen by each PA with symmetric excitation and efficiency of power delivery to the load. (c) Paths followed by the two PAs under asymmetric excitation when one PA cell is presented the optimal load-pull path. The deviation of the other PA from the ideal path results in degradation of net efficiency implying symmetric excitation is optimal at any frequency for symmetric combiners.

frequency can be programmed to operate more efficiently with asymmetrical excitation at a different frequency. In order to simplify analysis, we first linearize the operation of a PA cell as an output current source with complex *RC* impedance, where  $Z_s = Z_{opt}^*$ , where  $Z_{opt}$  is the optimal load-pull impedance of the central frequency, as shown in Fig. 6(a). This allows us to model the PA over a broad frequency range and Fig. 6(b) shows the close correspondence between the simulated and modeled optimal impedance for the stacked topology between 30 and 100 GHz. With this linearization, Fig. 7 shows a broadband two-way mm-wave PA with an optimized symmetrical multi-order ( $k = 5$ ) lossless combining network designed to operate between 40 and 100 GHz. As shown in Fig. 7(b), the impedances seen by the two cells are identical with symmetric excitations and they closely follow the optimal impedance path over a portion of the frequency range. By reconfiguring the driving conditions, if the impedance seen by one cell is made to follow exactly on the optimal load-pull path, the impedance seen by the other cell will deviate strongly, resulting in the degradation of net efficiency [Fig. 7(c)]. In essence, the optimal driving

condition for a symmetrical network is always identical excitations (equi-amplitude and equi-phase) independent of the frequency. However, this generalization does not hold for asymmetrical networks<sup>1</sup>.

### B. Optimal Driving Conditions for a Combiner

*1) Maximum Collective Efficiency of Combiner:* Consider an  $(N + 1)$ -port lossless passive combining network, where  $N$  amplifier cells with complex output impedance  $Z_{s,i}$  and available power  $|p_i^2|$  combine their power at the  $(N + 1)^{th}$  port, as shown in Fig. 5. Understandably, power transmitted to the load is a function of the collective impedance mismatches and therefore, is dependent on the driving conditions of the amplifiers ( $A_i e^{j\theta_i}, 1 \leq i \leq N$ ). We will analyze the optimal driving conditions that minimize the collective mismatches at a given frequency, and leads to optimal power efficiency given

<sup>1</sup>While the linearized analysis does not capture the possible voltage saturation effects for *non-optimal* loads, the modeling enables us to provide an intuitive and analytical approach towards network synthesis for optimal load presentation. Non-linear effects of a PA can be added into the modeling for a more complete description.

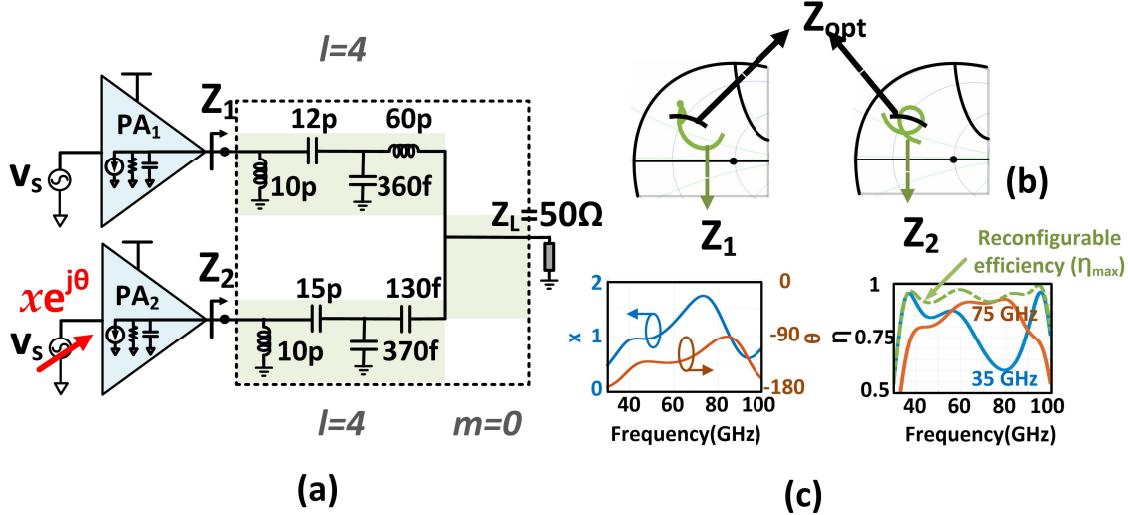


Fig. 8. (a) Example of a two-way asymmetrical architecture with the same PA cells as in Fig. 7. (b) Impedance paths followed by both the cells follow closely the load-pull path when driven optimally. (c) Optimal driving conditions ( $x, \theta$ ) across frequencies and the efficiency of power delivery when re-configured for two sets of driving conditions at 35 and 75 GHz. Achievable maximum efficiency traces the peaks of all such frequency-specific configured curves as seen by the dotted line.

the combiner network. If the S-parameters of the combiner are defined with respect to the complex terminating impedances, its efficiency can be expressed as [50]

$$\eta = \frac{P_{\text{load}}}{P_{\text{avs}}} = \frac{\left| \sum_{i=1}^N S_{N+1,i} \cdot p_i \right|^2}{\sum_{i=1}^N |p_i|^2} \quad (1)$$

where  $p_i$  represents the power-wave at the  $i$ th port. By Cauchy–Schwartz inequality, it can be shown that

$$\begin{aligned} \eta &= \frac{\left| \sum_{i=1}^N S_{N+1,i} \cdot p_i \right|^2}{\sum_{i=1}^N |p_i|^2} \leq \frac{\sum_{i=1}^N |S_{N+1,i}|^2 \cdot \sum_{i=1}^N |p_i|^2}{\sum_{i=1}^N |p_i|^2} \\ &= \sum_{i=1}^N |S_{N+1,i}|^2 = 1 - |S_{N+1,N+1}|^2. \end{aligned} \quad (2)$$

The upper bound or optimal efficiency is achieved when each PA cell is driven as

$$p_i \propto S_{N+1,i}^*. \quad (3)$$

The design of the frequency-reconfigurable PA, therefore, relies on the co-design of the combiner and the PA cells that allow the existence of such an optimal driving condition that can synthesize the optimal load-pull impedances across all the cells over the frequency range.

**2) Efficiency of Each Driving Source:** The efficiency of the  $i^{\text{th}}$  source is given by  $\eta_i = 1 - |r_i|^2$ , where  $|r_i|^2$  is the fraction of power delivered to the other ports and  $r_i$  is given by  $r_i = (\sum_{j=1}^N S_{i,j} p_j)/p_i$ . Therefore, under optimal driving conditions,  $r_i = \sum_{j=1}^N S_{i,j} \cdot (S_{N+1,j}/S_{N+1,i})^*$ . For a passive lossless  $(N + 1)$ -port network, we know that  $S S^H = I_{N+1}$  (i.e.,  $\sum_{j=1}^{N+1} S_{i,j} S_{N+1,j}^* = 0$ ), which implies  $\sum_{j=1}^N S_{i,j} S_{N+1,j}^* = -S_{i,N+1} S_{N+1,N+1}^*$ . This gives

$$r_i = \frac{\sum_{j=1}^N S_{i,j} \cdot S_{N+1,j}^*}{S_{N+1,i}^*} = -\frac{S_{i,N+1} S_{N+1,N+1}^*}{S_{N+1,i}^*}. \quad (4)$$

Therefore, the efficiencies of all the sources under optimal driving conditions are identical and is given by

$$\eta_i = 1 - |r_i|^2 = 1 - |S_{N+1,N+1}|^2 = \sum_{i=1}^N |S_{N+1,i}|^2 = \eta. \quad (5)$$

### C. Frequency Reconfigurability by Reconfiguring Driving Conditions

The bound expressed in (2) gives the maximum achievable efficiency at a given frequency obtained by reconfiguring the driving conditions of the combining cells according to (3) that minimizes the collective mismatches of all the unit cells. The expressions in (3)–(5) prove our previous observation that, for a symmetric combiner ( $S_{N+1,i}$  identical for all  $i$ ), the optimal driving conditions at any frequency are equi-amplitude and equi-phase, and higher power cannot be extracted by deviating from this condition. Evidently, this does not hold for an asymmetrical network. Fig. 8 shows this concept with the identical PA cells shown in Fig. 7, where the symmetrical combiner has been modified to introduce asymmetry. As shown in Fig. 8(b) and (c), by reconfiguring its driving condition (power-wave) as  $p_2/p_1 = xe^{j\theta} = (S_{32}/S_{31})^*$ , the PA can be operated with higher efficiency over a much broader range of frequencies, compared with a higher order symmetrical combiner. In essence, a reconfigurable quasi-higher order network is synthesized with a lower number of passives as shown in the comparison in Figs. 8(b) and 8(c) between the S-combiner ( $l = 4$  and  $m = 1$ ) and A-combiner ( $l = 4$  and  $m = 0$ ). As also seen in Figs. 8(b) and 8(c), the impedances seen by the cells are not identical, but closely trace the optimal path resulting in higher overall efficiency over the frequency range. It is important to note that in this example, as the PA is reconfigured for optimal operation across frequencies, both the PA cells do not deliver the same output power [Fig. 8(c)], but collectively maintains the overall

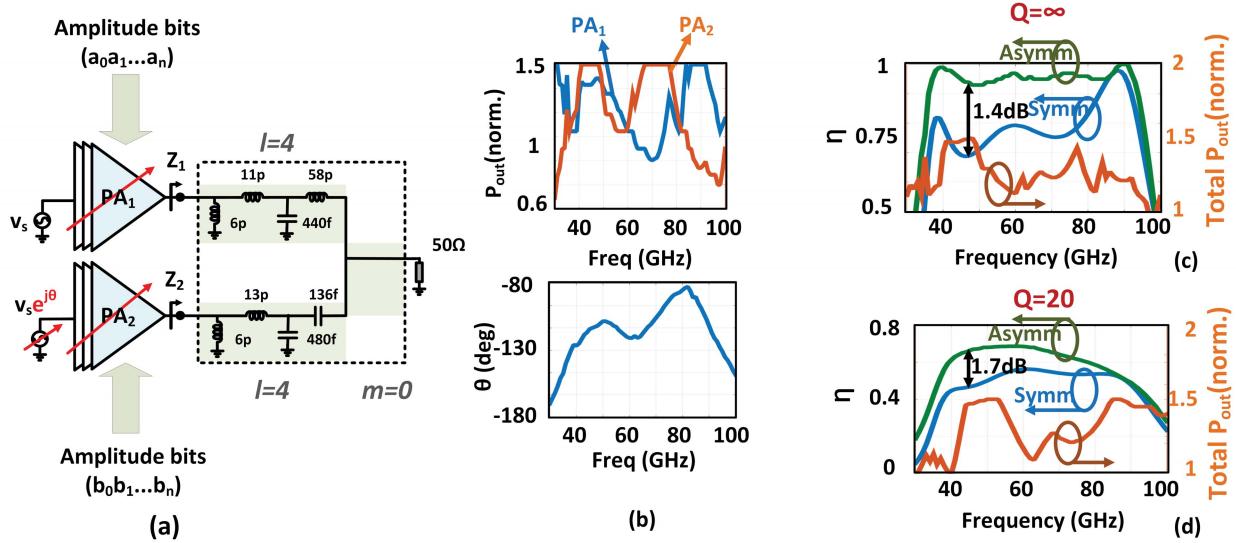


Fig. 9. (a) Example of a digital PA architecture where amplitude control is achieved through asymmetric switching of the PA cells. (b) Total output power from each cell across frequency normalized to that in a symmetrical combiner and phase control across the frequency of operation. (c) and (d) Comparison of efficiency of the A-combiner and S-combiner for ideal and lossy passives. The total output power of the A-combiner normalized to the S-combiner shows higher power delivery with higher efficiency across the frequency range with almost 50% improvement in efficiency at certain frequencies for lossy passives with 50% higher output power.

efficiency and total output power level over the reconfigurable frequency range. Functionally, this example is equivalent to multiple narrow-band switchable amplifiers, but this distributed approach eliminates the need for complex lossy mm-wave switching networks and encompasses the functionality in a monolithic network where reconfiguration can be achieved efficiently.

While the linearized model establishes the concept of active impedance synthesis, the constant output impedances of the unit cells in the model ( $Z_s = Z_{\text{opt}}^*$ ) at a given frequency independent of the driving conditions do not fully capture the voltage and current saturation effects for peak operation in a nonlinear PA. The amplitude variation in the driving conditions can be achieved digitally through a power-mixer/RF-DAC architecture by switching on- and off-cores, which simultaneously modulates the optimal load-pull impedance required for peak efficiency operation [51], [52]. Therefore, the network synthesis and the PA cell-operation need to be co-designed to ensure optimal efficiency throughout the operating range. Fig. 9 shows such a conceptual architecture and a design example, where frequency-dependent amplitude control is achieved digitally through switching the appropriate fraction of the cores in the combining cells and phase control is achieved in the LO path. Fig. 9(b) shows the phase control and simulated output power of each cell normalized to that in an S-combiner. Fig. 9(c) and (d) shows the achievable efficiency in an A-combiner against an S-combiner with ideal and lossy passives. The design example demonstrates higher power delivery with higher efficiency across the frequency range with nearly 50% improvement in efficiency and output power over certain frequency ranges for lossy passives. This distributed approach removes the complexity of broadband output combiners and implicitly encompasses this in the

active controls of the combining cells, suitable for silicon implementation.

#### IV. NETWORK SYNTHESIS AND DESIGN METHODOLOGY

Section III describes the active impedance synthesis properties of an asymmetrical architecture with design examples, and in this section, we will describe design methodologies for synthesizing such a network. As discussed before, the synthesis of an S-combiner is equivalent to that of a two-port combiner. An asymmetrical network synthesis is, however, a multi-port synthesis problem. While there are formal methods to construct the S-parameter description of such a network and synthesize it [53]–[59], in this section, we will provide an intuitive design methodology, which can be further improved with more sophisticated optimization procedures.

##### A. Condition 1: Power Transfer Efficiency

Let us consider the two-way A-combiner with lossless passive components [Fig. 10(a)] that achieves constant efficiency over a desired frequency range with both the PAs operating nearly at the peak of their output power levels. Therefore from (2) and (3), we desire a network, which satisfies  $\eta = |S_{31}|^2 + |S_{32}|^2 = 1$  (i.e.,  $|S_{33}|^2 = 0$ ) and also  $|p_1|^2 / |p_2|^2 \approx r$ , where “ $r$ ” is the ratio of sizes of the two PA cells implying  $|S_{31}| / |S_{32}| \approx (r)^{1/2}$ . It has to be remembered that the S-parameters are defined with respect to the complex impedances  $Z_{\text{ref}} = (Z_{s1}, Z_{s2}, Z_o)$ . Since the networks are lossless, the architecture can be simplified by encompassing NW<sub>3</sub> into one impedance  $Z_3$  as shown in Fig. 10(b). Therefore, the maximum achievable efficiency in power delivery is  $\eta = 1 - |S_{33}|^2$ , where  $S_{33}$  is given by

$$S_{33} = (Z_1 || Z_2 - Z_3^*) / (Z_1 | Z_2 + Z_3). \quad (6)$$

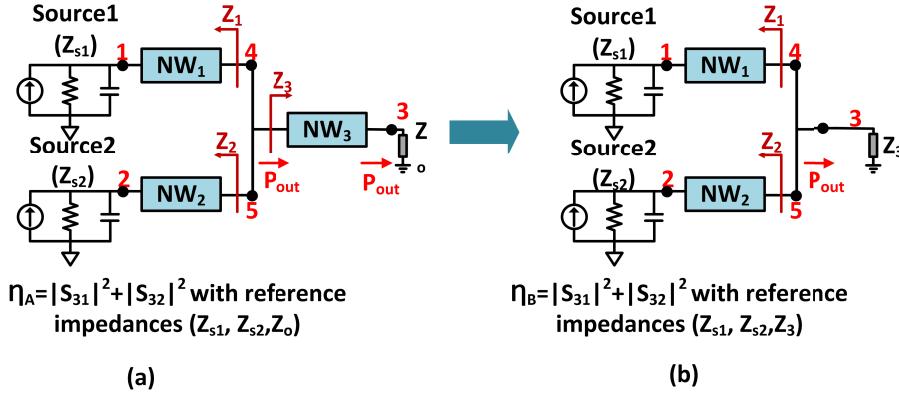


Fig. 10. (a) Synthesis of a two-way asymmetric combiner with ideal passives with each source being modeled by their complex output impedance  $Z_{s1,2} = Z_{\text{opt}1,2}^*$ . (b) Simplification of the three-port network by encompassing the network NW<sub>3</sub> into one impedance  $Z_3$  and the lossless nature of the passives ensures  $\eta_A = \eta_B$ . This decouples the three-port network problem into the synthesis of two two-port networks.

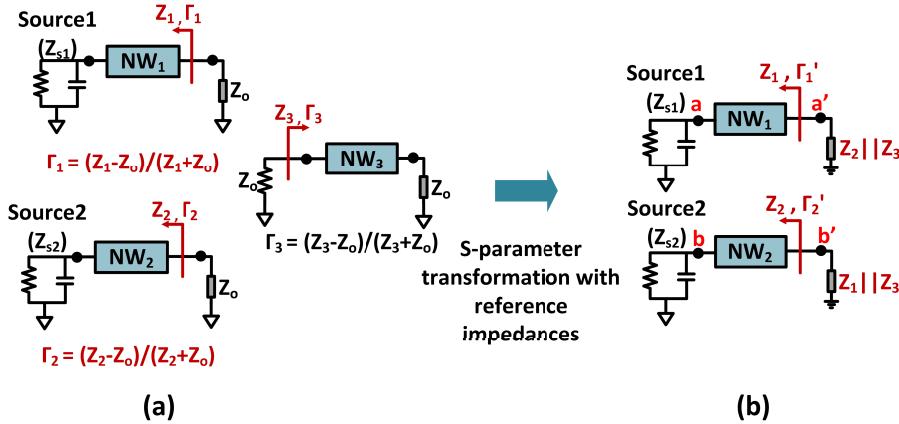


Fig. 11. (a) Representing the port impedances by their reflection coefficients with a reference load  $Z_0$ . (b) Transformation of the S-parameter with change in reference impedance.

Defining reflection coefficients as  $\Gamma_i = (Z_i - Z_o)/(Z_i + Z_o)$  as shown in Fig. 11(a), it can be shown that

$$S_{33} = \frac{\left[ \Gamma_1 \Gamma_2 - \frac{1-\Gamma_1}{2} \cdot \frac{1-\Gamma_2}{2} \right] - \Gamma_3^* \left[ 1 - \frac{1-\Gamma_1}{2} \cdot \frac{1-\Gamma_2}{2} \right]}{\left[ 1 - \frac{1-\Gamma_1}{2} \cdot \frac{1-\Gamma_2}{2} \right] - \Gamma_3 \left[ \Gamma_1 \Gamma_2 - \frac{1-\Gamma_1}{2} \cdot \frac{1-\Gamma_2}{2} \right]}. \quad (7)$$

In order to maximize efficiency,  $|S_{33}| \approx 0$ , and this implies

$$\left[ \Gamma_1 \Gamma_2 - \frac{1-\Gamma_1}{2} \cdot \frac{1-\Gamma_2}{2} \right] - \Gamma_3^* \left[ 1 - \frac{1-\Gamma_1}{2} \cdot \frac{1-\Gamma_2}{2} \right] = 0. \quad (8)$$

Considering a simplified network where the PAs combine directly at the load (i.e.,  $\Gamma_3 = 0$  or  $Z_3 = Z_o$ ), this simplifies to the following condition:

$$\Gamma_1 \Gamma_2 - \frac{1-\Gamma_1}{2} \cdot \frac{1-\Gamma_2}{2} = 0. \quad (9)$$

### B. Condition 2: Peak Operation of Both Cells

In order to ensure that both the PA cells operate at peak power over the range, the network as shown in Fig. 10(a) needs

to satisfy ( $|S_{31}|/|S_{32}| \approx (r)^{1/2}$ ). By dissociating the three-port network into two separate two-port networks, we perform an S-parameter transformation where terminating impedances are transformed from  $Z_{\text{ref}}(Z_{s1}, Z_{s2}, Z_o)$  to  $Z'_{\text{ref}1}(Z_{s1}, Z_2 || Z_3)$  and  $Z'_{\text{ref}2}(Z_{s2}, Z_1 || Z_3)$ , respectively, as shown in Fig. 11(b). Assuming as before, both PAs combining directly on the load, as shown in the Appendix, it can be proved that that the two-port network in Fig. 11(b) satisfies

$$|S_{aa'}|^2 = \frac{(1 - |\Gamma_1|^2) \cdot (1 + \text{Re}\{\Gamma_2\})}{2 \left| 1 - \frac{1-\Gamma_1}{2} \cdot \frac{1-\Gamma_2}{2} \right|^2}. \quad (10)$$

For lossless network,  $|S'_{aa}|^2 = 1 - |S_{aa}|^2 = 1 - |S_{11}|^2 = |S_{12}|^2 + |S_{13}|^2$ . This implies

$$|S_{12}|^2 + |S_{13}|^2 = \frac{(1 - |\Gamma_1|^2) \cdot (1 + \text{Re}\{\Gamma_2\})}{2 \left| 1 - \frac{1-\Gamma_1}{2} \cdot \frac{1-\Gamma_2}{2} \right|^2} \quad (11)$$

Similarly, for applying the same procedure to NW<sub>2</sub>, we obtain

$$|S_{12}|^2 + |S_{23}|^2 = \frac{(1 - |\Gamma_2|^2) \cdot (1 + \text{Re}\{\Gamma_1\})}{2 \left| 1 - \frac{1-\Gamma_1}{2} \cdot \frac{1-\Gamma_2}{2} \right|^2}. \quad (12)$$

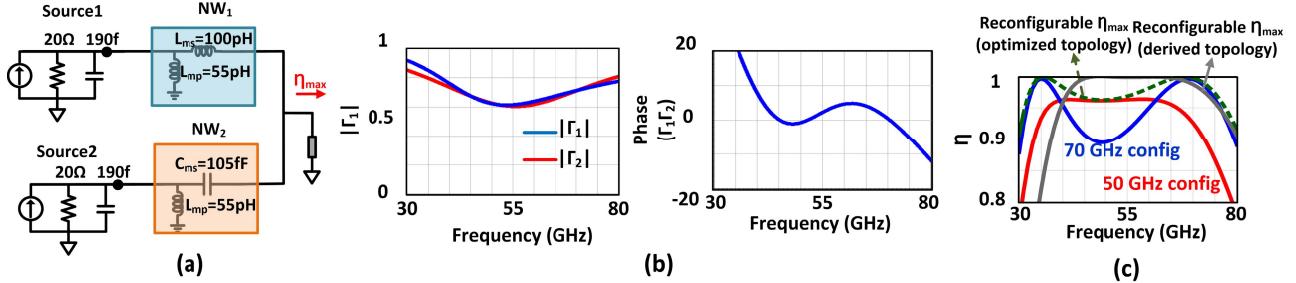


Fig. 12. (a) Synthesis and optimization of an asymmetric combiner. (b) Synthesized network establishes  $\Gamma_2 \approx \Gamma_1^*$  across the frequencies 40–70 GHz, which establishes optimal efficiency and peak operation of both the cells. (c) Power delivery efficiency of the synthesized network demonstrating reconfigurable  $\eta > 90\%$  across 40–80 GHz and can be optimized with slight tuning of the parameters covering 30–80 GHz. The figure also shows the efficiency variation when the PA is reconfigured for optimal operation at two frequencies, namely, 50 and 70 GHz.

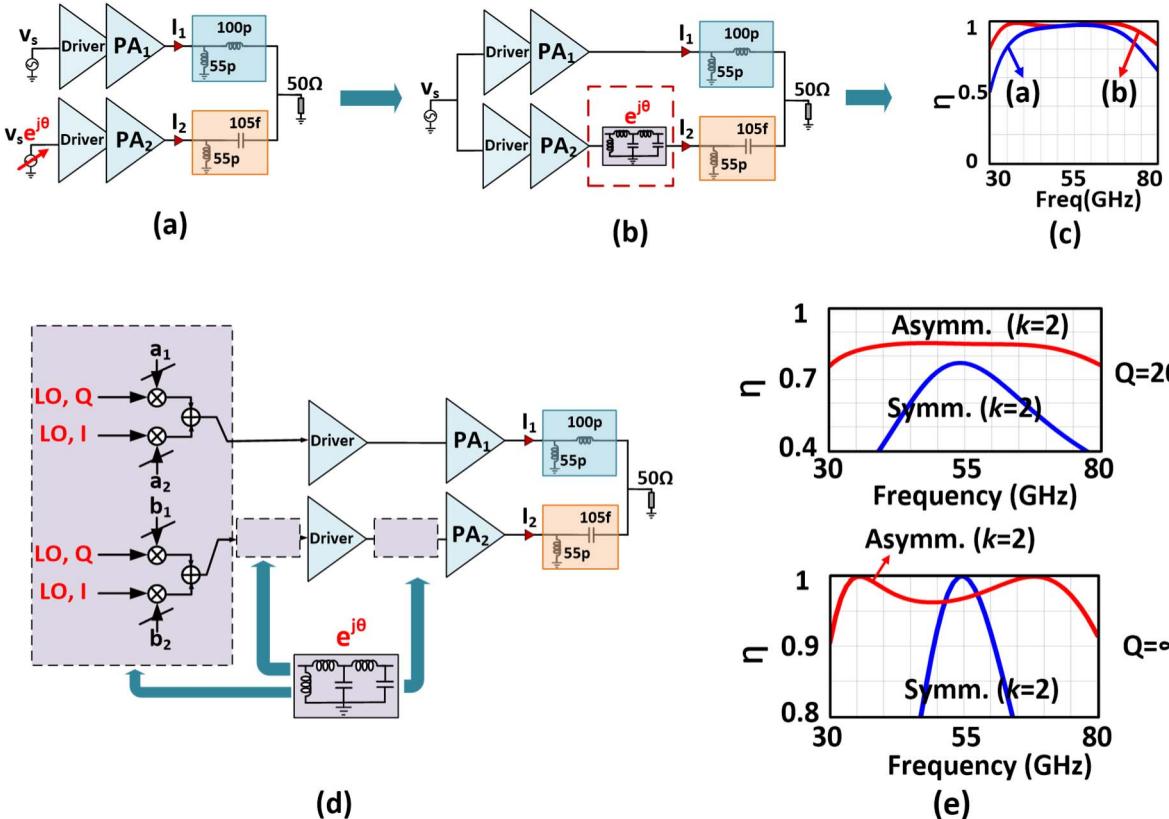


Fig. 13. (a) and (b) Intuitive understanding of the broadband nature of A-architecture by enabling the phase control with passive elements leading to an effective broadband higher order output combining network. (c) Comparison of the maximum efficiency of (a) and (b). (d) Dissociating the broadband higher order output network and encompassing the phase shifter either at baseband, or at the input or at the intermediate stage minimizing output combiner loss. (e) Comparison of the A-architecture versus optimized S-architecture for ideal and lossy passives.

Substituting  $|S_{31}|^2 = r|S_{32}|^2$  and performing (12)–(11) with  $|S_{31}|^2 + |S_{32}|^2 = 1$ , we get

$$\frac{1-r}{1+r} = \frac{1}{2} \cdot \frac{(1 - |\Gamma_2|^2) \cdot (1 + \text{Re}\{\Gamma_1\}) - (1 - |\Gamma_1|^2) \cdot (1 + \text{Re}\{\Gamma_2\})}{\left|1 - \frac{1-\Gamma_1}{2} \cdot \frac{1-\Gamma_2}{2}\right|^2}. \quad (13)$$

If we choose identical PA cells (Fig. 8), i.e.,  $r = 1$ , from (13), we get the second condition for peak operation

$$\frac{1 + \text{Re}\{\Gamma_1\}}{1 - |\Gamma_1|^2} = \frac{1 + \text{Re}\{\Gamma_2\}}{1 - |\Gamma_2|^2}. \quad (14)$$

In summary, (9) and (14) may have multiple solutions, and therefore, the network is not unique. As an example,  $\Gamma_2 = \Gamma_1$

satisfies (14) and leads to the symmetrical structure, while another solution leads to the desired asymmetrical combiner solution as follows

$$\Gamma_2 = \Gamma_1^*. \quad (15)$$

Substituting (15) in (9), we obtain a relationship on  $\Gamma_1$  as

$$|\Gamma_1| = \left| \frac{1 - \Gamma_1}{2} \right|. \quad (16)$$

### C. Design Example

In this example, we will demonstrate synthesis for an asymmetrical PA architecture operating between 30 and 80 GHz with the center frequency of 55 GHz based on the described methodology. Fig. 12 shows the unit PA cell (stacked topology

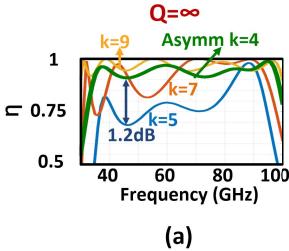


Fig. 14. Achievable reconfigurable efficiency for a two-way A-combiner with  $k = 4$  versus optimized S-combiners with  $k = 5, 7, 9$  for (a) ideal passives and (b) finite  $Q$  passives.

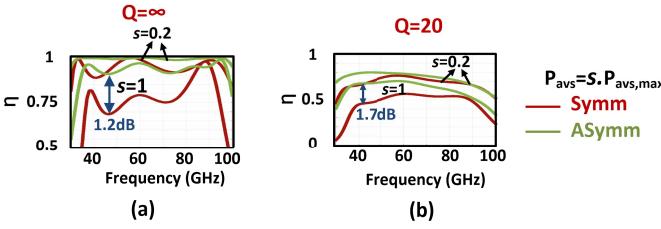


Fig. 15. Achievable reconfigurable efficiency for a two-way A-combiner with  $k = 4$  versus optimized S-combiner with  $k = 5$  for various power-scaling factors “ $s$ ” ( $= 0.2, 1$ ) for (a) ideal passives and (b) finite  $Q$  passives.

with  $96 \mu\text{m} \times 0.13 \mu\text{m}$  emitter size) with its output impedance ( $Z_s = Z_{\text{opt}}$ ) represented by the parallel network of  $R_s = 20 \Omega$ ,  $C_s = 190 \text{ fF}$ . First, an inductor ( $L_{\text{mp}} = 45 \text{ pH}$ ) is added in both branches to resonate out the source capacitance of  $190 \text{ fF}$  at the center frequency of  $55 \text{ GHz}$  and connect with the supply. With that established, the second condition  $\Gamma_2 = \Gamma_1^*$ , which satisfies (15), can be accomplished by adding inductor ( $L_{\text{ms}}$ ) in series in one branch and capacitor ( $C_{\text{ms}}$ ) in series in the other branch, such that  $j\omega_0 L_{\text{ms}} = -1/j\omega_0 C_{\text{ms}}$  at the center frequency  $\omega_0$ . The other condition expressed in (15), for efficiency enhancement, can be solved with  $\Gamma_1 = (R_s + j\omega_0 L_{\text{ms}} - Z_o)/(R_s + j\omega_0 L_{\text{ms}} + Z_o)$  at  $\omega_0$  leading to  $L_{\text{ms}} \approx 110 \text{ pH}$  and  $C_{\text{ms}} = 75 \text{ fF}$ . As shown in Fig. 12(b), the realized network maintains  $\Gamma_2 \approx \Gamma_1^*$  across the frequencies  $40\text{--}70 \text{ GHz}$  with reconfigurable  $\eta > 95\%$ , which can be improved to cover  $30\text{--}75 \text{ GHz}$  with slight tuning of the parameters [Fig. 12(a) and (c)]. Fig. 12(c) shows that even with a static configuration (at  $50 \text{ GHz}$ ), the A-combiner-based architecture shows an instantaneous broadband performance with a simple second-order network in each branch. Therefore, unlike a symmetrical architecture, the proposed network breaks a complex higher order network into simple lower order networks asymmetrically into several PA cells, and quasi-synthesizes a higher order network with the interaction of the combining cells. This will be addressed in more detail in Section V, which discusses the Bode–Fano bounds of such an asymmetrical combining network.

The broadband nature of the A-combiner is implicitly encompassed in the phase rotations at the input of the combining cells. An intuitive reasoning is shown in Fig. 13. Consider the phase rotations induced at the input of the source be transferred to the output and be realized with passive elements as shown in Fig. 13(a) and (b). This results in a

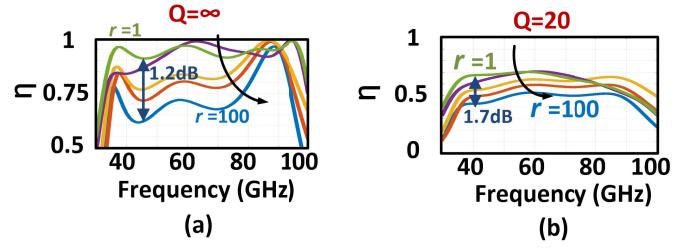


Fig. 16. Achievable reconfigurable efficiency for a two-way A-combiner with  $k = 4/5$  for various size ratios “ $r$ .” Here PA<sub>1</sub> is sized  $r$  times that of PA<sub>2</sub> for the same total PA size and output power.  $\eta$  for such two-way A-combiner with (a) ideal and (b) finite  $Q$  passives for different values of  $r$  varying from 1 to 100.

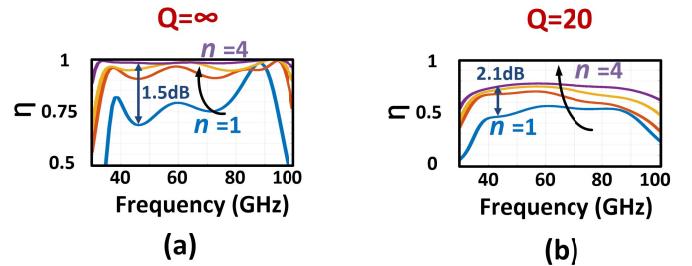


Fig. 17. Variation of reconfigurable efficiency for an  $N$ -way A-combiner with  $k < 5$  for various numbers of combining elements ( $N$ ) for constant output power for (a) ideal and (b) lossy passives.

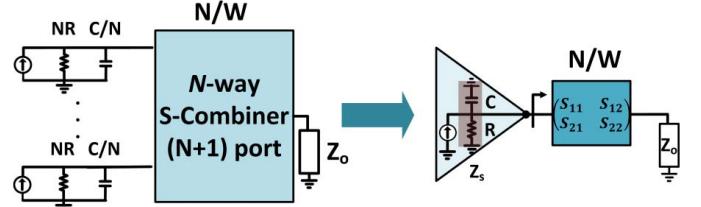


Fig. 18. Bandwidth bounds for an  $N$ -way symmetrical combiner is identical to that of a two-port network with scaled impedances.

characteristic broadband higher order combiner with a single source displaying efficiencies similar to that of the A-architecture [Fig. 13(c)], but with the additional losses and shortcomings of a complex output combiner as discussed before. The  $N$ -way asymmetrical architecture breaks this tradeoff between output power, efficiency, and frequency range by dissociating the complex higher order combiner network and distributing them into the various combining PAs and simple phase rotations. The phase rotations are realizable at any of the previous stages, either through variable delay lines or digitally through I,Q phase rotations, which allows its incurred losses not affect overall efficiency significantly. Fig. 13(d) shows the comparison between the second-order S and A-architectures with ideal and lossy passives.

## V. ASYMMETRICAL VERSUS SYMMETRICAL DESIGN TRADEOFFS

The ability to synthesize complex RF impedances actively creates very interesting design tradeoffs, and in this section,

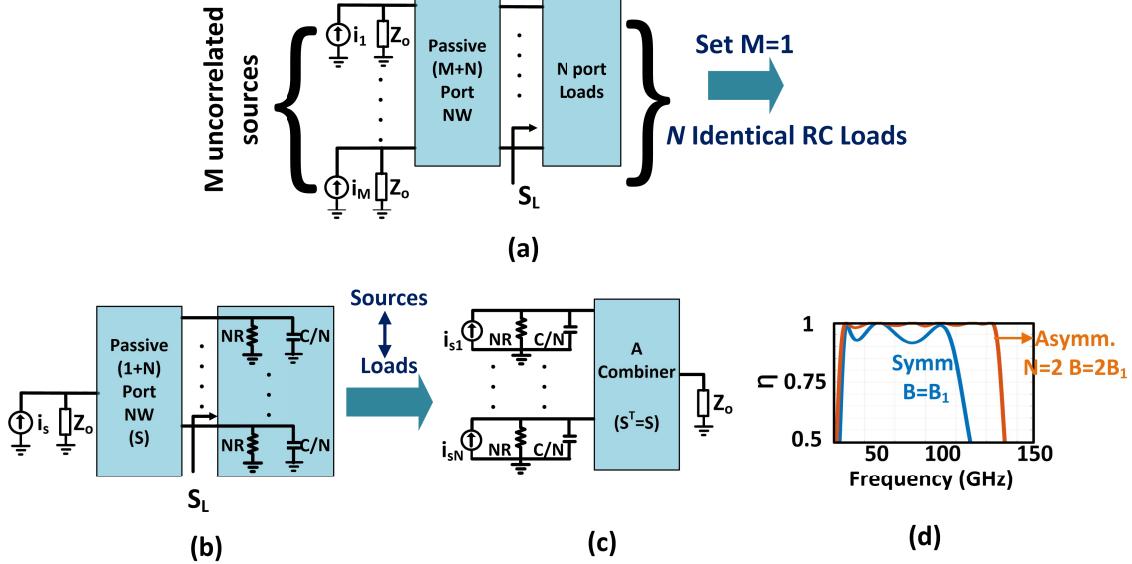


Fig. 19. (a) General  $(N + M)$  port passive network with  $M$  uncorrelated sources driving  $N$  loads defined by load  $S$  matrix ( $S_L$ ) whose bound scales as  $N/M$  [61]. (b) By setting  $M = 1$  and  $N$  identical  $RC$  loads in (a) to arrive at (b) which has  $N$  times higher bound than a single  $RC$  network [61]. (c) A-architecture with a combiner employing  $N$ -sources with scaled output impedances ( $NR, C/N$ ) driving a single load  $Z_o$  (obtained by interchanging the sources and loads) has  $N$  times bound compared with an S-architecture. (d) Simulation of the bound of a two-way A-combiner showing twice the bound of that of an S-combiner.

we provide qualitative and quantitative comparison of the frequency reconfiguration properties and its dependence on the design parameters, such as the order of the network, size and size ratio of the constituent amplifiers, and the number of combining stages.

#### A. Order of the Network $k$ ( $l + m$ )

Unlike a S-combiner, the network order of an A-combiner does not get reduced and equivalently, a quasi-higher order reconfigurable network can be synthesized with a lower number of matching elements. Fig. 14 shows this tradeoff comparing the reconfigurable peak efficiency of a two-way A-combiner with  $k = 4$  against optimized S-combiners with  $k = 5 - 9$  with ideal and lossy passives. The combined cell size is identical to the one described in Fig. 6. The reduction in the number of passive elements enables higher efficiencies achievable over the entire range with nearly 50% improvement over a range of frequencies for the design examples presented.

#### B. Scaling of Output Power

Expectedly, increasing the size of the constituent amplifiers to increase output power also simultaneously increases impedance transformation ratio, which typically reduces network efficiency due to higher losses. This makes it even more difficult to realize high power and efficient mm-wave PA capable of operating over a large frequency range of operation. Reducing the order of the network and synthesizing the desired complex RF impedances actively help to break this tradeoff. This is shown in Fig. 15, which compares the efficiency of the two architectures with  $k = 4$  and  $k = 5$ , respectively, for different power scaling ratios.

#### C. Sizing of the Combining Cells

The previous examples illustrate asymmetrical combining network with identical PA cells. Fig. 16 shows the variation of the performance as the splitting ratio is varied between the combining cells for a two-way combiner for constant output power. Intuitively, for a high value of  $r$  (say  $r = 100$ ), the architecture is equivalent to one cell and expectedly, the asymmetrical architecture is essentially equivalent to that of a symmetrical combiner. As shown in the example in Fig. 16, with increase in  $r$ , the A-combiner progresses toward an S-combiner with maximum efficiency improvement achieved near  $r = 1$ .

#### D. Number of Combining Stages

Intuitively, the asymmetrical architecture exploits the non-existence of symmetry in the combining networks to synthesize the variable complex RF impedance over the frequency range. Therefore, with a larger number of combining cells, the architecture can leverage more energy-storing elements to enable frequency reconfigurability over an even broader range of frequencies for the same output power. Unlike the symmetrical architecture, where the network order remains unchanged with the number of combining cells, the effective order of the network of an A-combiner increases with increase in ' $n$ ', enabling it to break the tradeoff between frequency range of operation and output power. This is shown in Fig. 17. The choice of the number of combining stages depends mainly on the required impedance transformation ratio, and the frequency range along with area overhead and layout constraints. As, for the example, shown in Fig. 17, if the range of frequencies is from 30 to 80 GHz, significant improvement could be seen

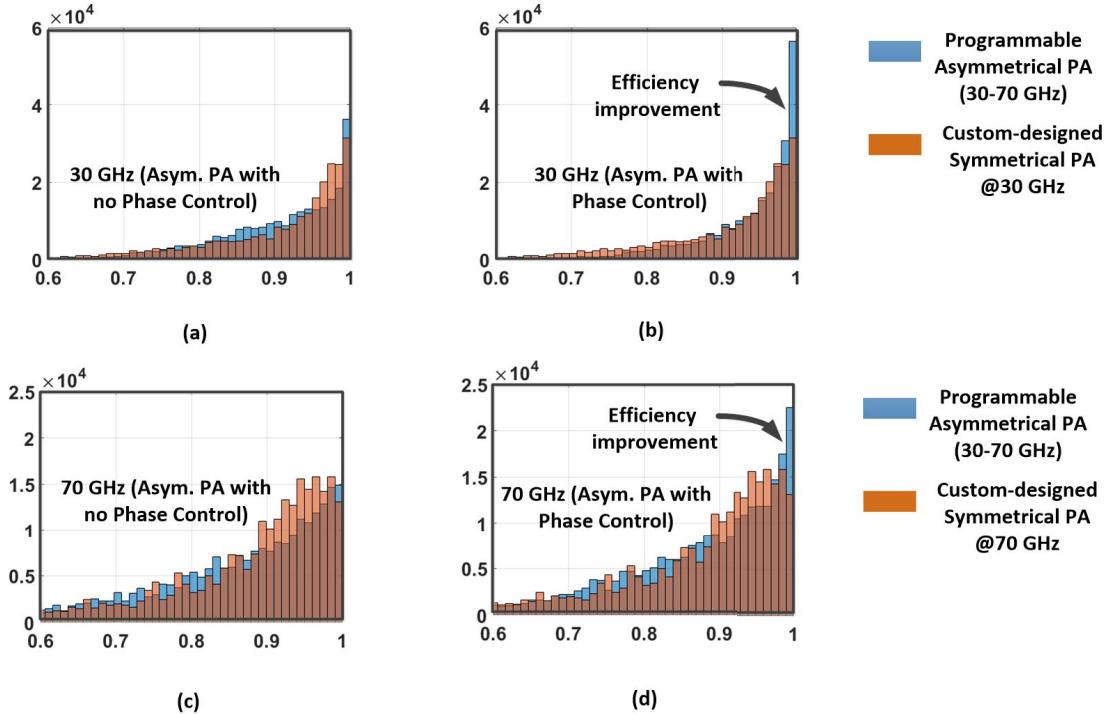


Fig. 20. Effect of process variations on the A-combiner against the S-combiner. (a) and (c) Monte Carlo simulations showing the spread of the efficiency with process variations at 30 and 70 GHz for a single programmable asymmetric architecture against separately designed symmetrical PAs at the two frequencies respectively. The efficiency degradation is similar in both cases. (b) and (d) Efficiency enhancement of the A-combiner with integrated phase control.

with  $n = 2$  (asymmetrical) over  $n = 1$  (symmetrical), while the improvement is not substantial from  $n = 2$  to  $n = 4$ . Therefore,  $n = 2$  may be an optimum choice over  $n = 4$  avoiding extra area overhead. For higher power generation with the same operating range, a higher number of combining stages will be required.

#### E. Bounds of Frequency Range of Operation Symmetrical Versus Asymmetrical

So far, we have understood intuitively that A-combiner performs more efficiently than the S-combiner due to the higher effective order of the combining network owing to the asymmetry. This can be quantitatively understood from the bound similar to the one developed by Bode–Fano that relates efficiency ( $\eta$ ) to the attainable bandwidth ( $B$ ) of a given network.

1) *S-Combiner*: The bandwidth bound that of an  $N$ -way S-combiner being mathematically identical to a two-port network due to operational symmetry (Fig. 18) is given by the Bode–Fano bound [47] as

$$\int_0^\infty \ln \left( \frac{1}{|r(f)|} \right) df = \int_0^\infty \ln \left( \frac{1}{\sqrt{1 - \eta(f)}} \right) df \leq \frac{1}{2RC} \quad (17)$$

where  $|r(f)|^2$  and  $\eta(f)$  represent the fraction of the reflected power and the transmitted efficiency of the network, respectively. The bound is independent of load and matching network and depends only on the time constant of source impedance ( $RC$ ) and shows clearly the tradeoff between  $\eta$  and  $BW$ .

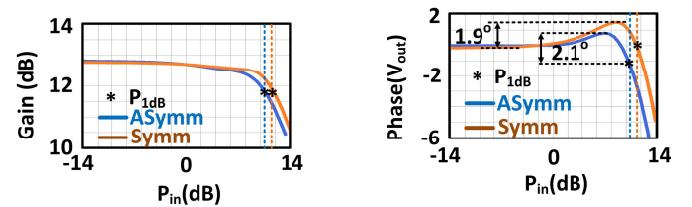


Fig. 21. Comparison of AM–AM and AM–PM distortion at 50 GHz.

2) *A-Combiner*: The bandwidth limitations of an A-combiner are related to the bound of a multi-port system and are more complex. It has recently been shown in [60] and [61] that the integral bound for a multi-port network with  $M$  uncorrelated sources driving  $N$  loads (defined by S-parameter  $S_L$ ), as shown in Fig. 19, is given by

$$\int_0^\infty \ln \left( \frac{1}{|r(f)|} \right) df \leq \frac{-1}{4M} \left( \sum_i p_{L,i} + \sum_i z_{L,i} \right) \quad (18)$$

where  $|r(f)|^2$  is the power reflection ratio [61] and  $p_{L,i}$  and  $z_{L,i}$ s are the poles and zeros of  $S_L$ . Therefore, for a single source with  $N$  identical  $RC$  loads [Fig. 19(b)], the bound is  $N$  times that of a two-port network and given by

$$\int_0^\infty \ln \left( \frac{1}{|r(f)|} \right) df \leq \frac{-1}{4} \left( \sum_i p_{L,i} + \sum_i z_{L,i} \right) = \frac{N}{2RC} \quad (19)$$

where the power reflection ratio is given by  $|r(f)|^2 = |S_{11}|^2 = 1 - \sum_{j=2}^{N+1} |S_{j,1}|^2$ . As shown in Fig. 19(c), if we now interchange the sources and loads resulting in the A-combiner

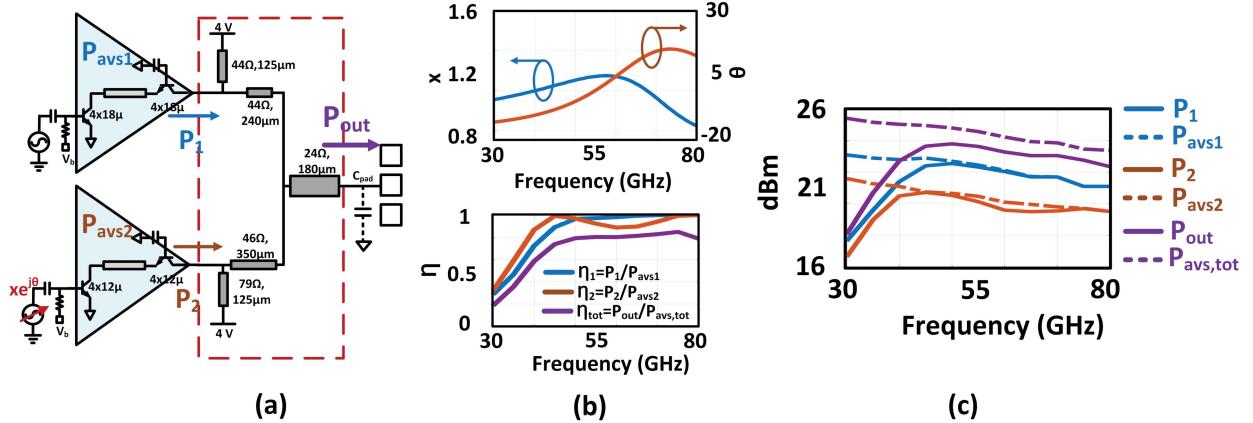


Fig. 22. (a) Output A-combiner with stacked PA unit cells with intra-stage t-line matching. The cells are sized at a ratio of 1.5:1. (b) Optimal driving conditions for amplitude and phase for frequency-reconfigurable operation. The bottom figure shows the power delivery efficiency of each PA cell ( $\eta_1, \eta_2$ ) and the total combining efficiency ( $\eta_{tot} = \frac{P_{out}}{P_{avs}}$ ).  $P_{avs}$  represents the maximum combined power that can be extracted from the PA cells with lossless networks designed optimally at each frequency. (c) Simulated output power from individual cells ( $P_1, P_2$ ) and the power delivered to the load ( $P_{out}$ ) against frequency, showing near optimal efficiency between 40 and 70 GHz.

with the load  $Z_o$  at port 1, the maximum efficiency of such an A-combiner from (2) due to the reciprocal nature of the passive network is given by  $\eta_{max} = \sum_{j \neq 1} |S_{1,j}|^2 = \sum_{j \neq 1} |S_{j,1}|^2 = 1 - |r(f)|^2$ , which results in the bound for maximum achievable efficiency for an  $N$ -way A-combiner as

$$\int_0^\infty \ln \left( \frac{1}{\sqrt{1 - \eta_{max}}} \right) df \leq \frac{N}{2RC}. \quad (20)$$

Hence, the bound for an  $N$ -way A-combiner is  $N$  times that of an  $N$ -way S-combiner. This is the essence behind the frequency-reconfiguration property of the proposed asymmetrical architecture. Fig. 19(d) shows this property and shows simulated bounds for two-way symmetrical and asymmetrical combining architectures with networks that reach close to the maximum achievable bounds.

#### F. Effect of Process Variations

It is interesting to observe the effects of process variations on efficiency degradation of an S-combiner and A-combiner as shown in Fig. 20(a) and (c). Fig. 20(a) and (c) shows Monte Carlo simulation of power-transfer efficiency due to process variations at 30 and 70 GHz, respectively, between separately custom-designed symmetrical architectures and programmable asymmetrical architecture operating between 30 and 70 GHz. As can be seen, with the nominal settings, the efficiency degradation is similar, but the phase control of the A-combiner allows strong enhancement of the performance post-fabrication.

#### G. Effect of AM-AM and AM-PM Distortion

Fig. 21 compares the AM-AM and AM-PM effects of two such architectures with similar output saturated power levels. As can be seen, the nonlinear effects are similar in both the cases, and therefore, no complex distortion compensation circuitry is required especially for the A-combiner architecture.

## VI. MM-WAVE PA DESIGN AND IMPLEMENTATION

A close co-design process between the constituent PA cells and the output combiner is followed for the co-optimization of peak power and efficiency across the frequency range.

### A. Choice of the Unit PA cell

A stacked topology for a PA cell was chosen for its higher gain, PAE, and higher optimum impedance by allowing larger voltage swings across the output [16], [19]. The optimum intra-stack matching is employed to maximize output power extracted from the common-emitter transistor to be pumped into the stacked transistor. For a wideband performance, the double-stack configuration with a transmission line for intra-stack matching is chosen in our design as shown in Fig. 22(a).

### B. Combiner Design

The combiner was designed following the methodology described in Section IV to ensure that the PAs operate close to peak efficiency and output power throughout the frequency range. Fig. 22(a) shows the details of the combiner. Given the range of amplitude and phase rotations, the two-way combiner was co-designed with the PA cells, which were sized at a near-optimal ratio of  $r = 1.5$ . It can be shown that given a constant available power, maximization of output power can be achieved by modifying (2) and optimizing the efficiency for peak operation of both PAs ( $\eta$ ) across the frequencies, where  $\eta$  is given by

$$\begin{aligned} \eta &= (|S_{31}p_1 + S_{32}p_2|^2)/(|p_1|^2 + |p_2|^2) \\ &\leq \frac{\left( |S_{31} \left( \frac{p_1}{p_2} \right)| + |S_{32}| \right)^2}{\left| \frac{p_1}{p_2} \right|^2 + 1} \\ &= (|S_{31}\sqrt{r}| + |S_{32}|)^2 / (r + 1) = \eta_{max} \end{aligned} \quad (21)$$

To ensure this efficient peak operation ( $\eta_{max}$ ) for the designed combiner with the ratioed PA cells, it can be shown

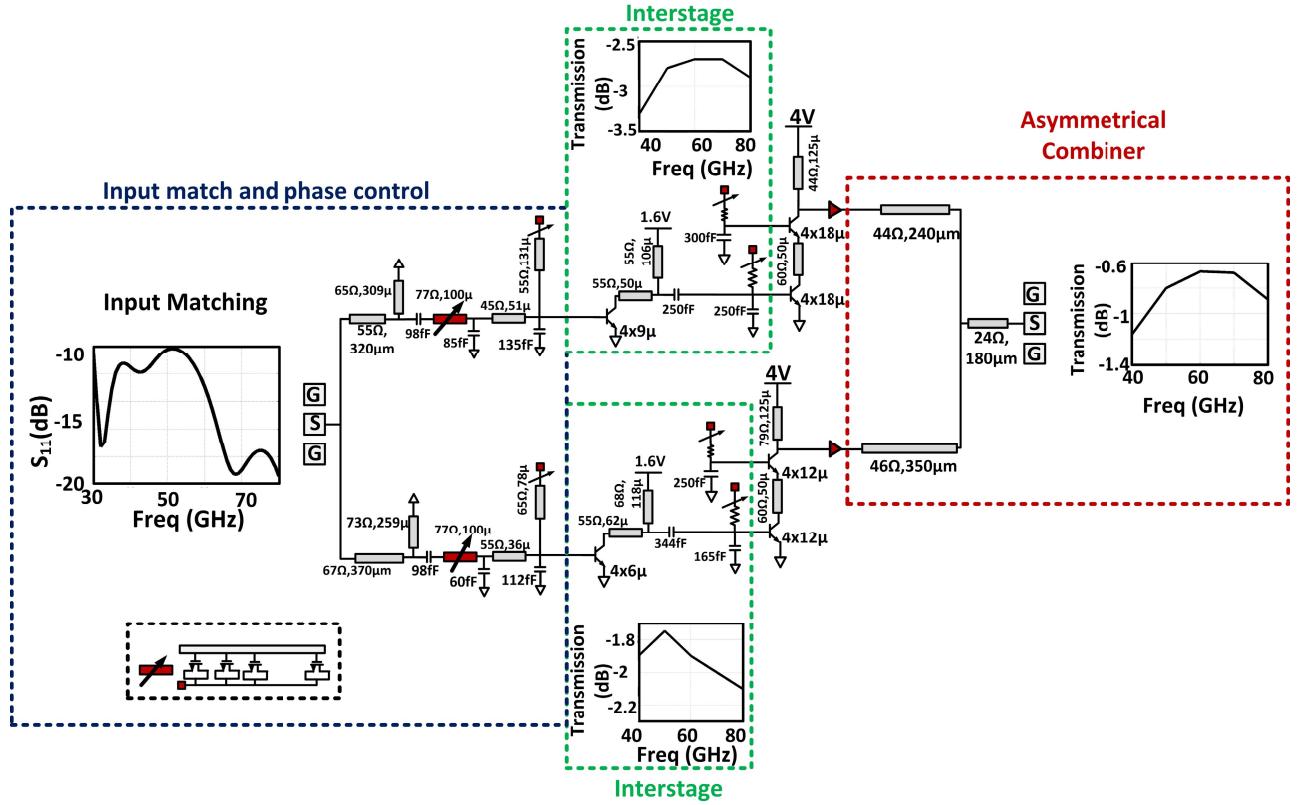


Fig. 23. PA schematic showing the PA and the driver cells, implemented matching networks, variable delay line for phase control and the simulated performance of the various matching stages.

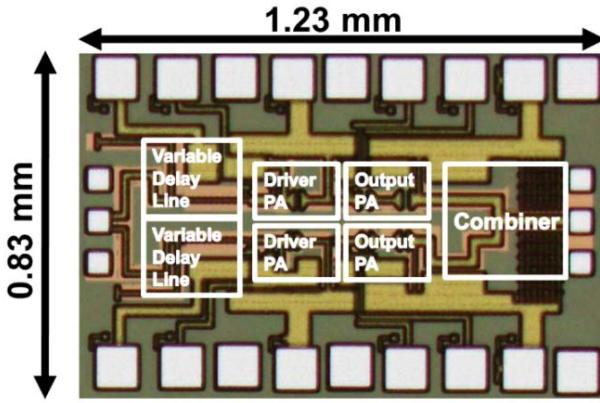


Fig. 24. Chip micrograph of the implemented PA.

that the optimal driving conditions should satisfy  $(p_2)/(p_1) = (xe^{j\theta})/(\sqrt{r})$  and  $|(p_2)/(p_1)| \approx (1)/(\sqrt{r})$ . As shown in Fig. 22(b), with the amplitude control ("x") between 1 and 1.2 and phase control within  $30^\circ$ ,  $\eta_{\max} > 70\%$  could be achieved across 45–80 GHz. The combiner is realized with micro-strip transmission lines and realized with the top Al metal layer of 4- $\mu\text{m}$  thickness. Fig. 22(c) shows the simulated performance of the output PA stage with the combiner. This shows the ability for  $P_{\text{out}}$  to follow closely  $P_{\text{avs}}$  across 40–80 GHz. Here,  $P_{\text{avs}}$  is defined as the maximum combined output power by both the PA cells when presented with optimal load-pull impedances across the frequency range.

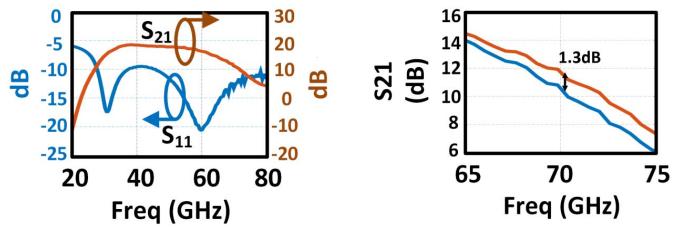


Fig. 25. Measured S-parameters for one configuration. Gain improvement of 1.3 dB is achieved through phase reconfiguration that enables re-alignment of optimal impedance for small-signal performance.

### C. Complete PA Architecture

The complete schematic of the proof-of-concept PA is shown in Fig. 23 [48]. The PA cells in the output stage are double-stacked with the transistors sized  $4 \times 18 \mu\text{m}$  and  $4 \times 12 \mu\text{m}$  in the upper and lower branches, respectively. Both these PA cells operate from 4-V supply. The capacitors used for intra-stack matching at the base of the stacked transistor are absorbed in the parasitics in both the branches. The driver amplifiers are common-emitter stages sized  $4 \times 9 \mu\text{m}$  and  $4 \times 6 \mu\text{m}$  in the upper and lower branches, respectively, and operate from a 1.6-V supply. Amplitude control is achieved by controlling the gain of the PA cells through bias control, while the differential phase tuning of up to  $40^\circ$  is achieved through a variable-delay transmission line realized with distributed varactors [48]–[51]. In order to minimize the effect of loss on the output power, the delay lines are integrated with the

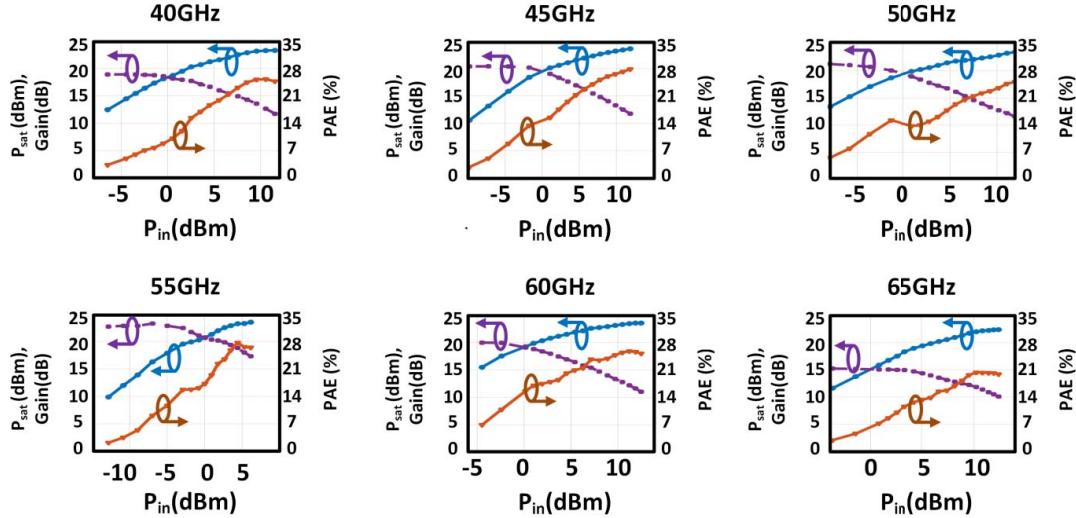


Fig. 26. Measured large-signal performance ( $P_{out}$ /PAE) when the PA is reconfigured across frequencies from 40 to 65 GHz.

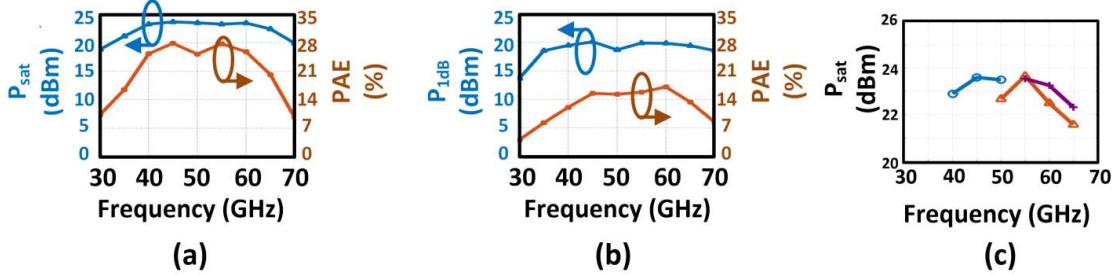


Fig. 27. Measured (a)  $P_{sat}$  and PAE<sub>peak</sub> and (b)  $P_{1dB}$  and PAE <sub>$P_{1dB}$</sub>  when the PA is reconfigured across frequencies from 40 to 65 GHz. The PA can be configured to maintain  $P_{sat} > 22$  dBm and  $P_{1dB}$  close to 20 dBm between 40 and 65 GHz with PAE<sub>peak</sub> > 25%. (c)  $P_{sat}$  variation for three sets of reconfigured conditions.

input matching. The simulated input matching is broadband with  $S_{11}$  below  $-10$  dB across 30–80 GHz. The inter-stages are designed to be broadband with losses below 3.2 and 2.1 dB for the upper and lower branches, respectively, for 40–80 GHz. The combiner loss is below 1.2 dB across 40–80 GHz. It can be noted that, in integration with the full transmitter system, the amplitude control could be achieved through a multibit DAC structure and the phase tuning could be achieved at the baseband itself. Enabling a wide phase synthesis can allow further optimization of a compact A-combiner architecture not constrained by the limited phase rotations of RF phase shifters.

## VII. MEASUREMENT RESULTS

The PA is implemented in 0.13- $\mu$ m SiGe BiCMOS process. The chip micrograph is shown in Fig. 24. The chip measures  $1.23 \times 0.83$  mm $^2$  with the active area measuring  $1.1 \times 0.32$  mm $^2$ . The main stage PA cells operate from 4-V supply, while the driver cells operate from 1.6-V supply.

### A. S-Parameter Measurement

The measured S-parameters for the chip for one configuration are shown in Fig. 25. The input matching is broadband with  $S_{11}$  below  $-9.5$  dB across 30–80 GHz. The small signal

gain for this given configuration peaks at 18 dB at 39 GHz. It can be noted that even though the PA architecture and output combining network is designed for maximizing output power across the frequency range, phase reconfiguration can be applied to reconfigure the output impedance and can enhance small-signal gain performance, as noted by a 1.3 dB increase in small-signal gain at 70 GHz shown in Fig. 25.

### B. Large-Signal Measurement

The PA was characterized for large signal measurement across 30–80 GHz where the PA is reconfigured at each frequency through bias and phase control. During reconfiguration, the bias voltages for the base of the common-source transistors and that of the stacked transistor are varied from 0.8 to 0.9 V and 2.6 to 2.9 V through resistive dividers, both of which enable gain control and amplitude control of the PA. The control voltage for the variable delay line between 0 and 1 V controls the relative phases between the two branches. The measured large-signal performance for the PA across 40–65 GHz is shown in Fig. 26. The measured  $P_{sat}$  and PAE<sub>peak</sub> for the frequencies 30–70 GHz are shown in Fig. 27(a). The peak  $P_{sat}$  is 23.6 dBm at a PAE<sub>peak</sub> of 27.7% at the center frequency of 55 GHz. The PA maintains a

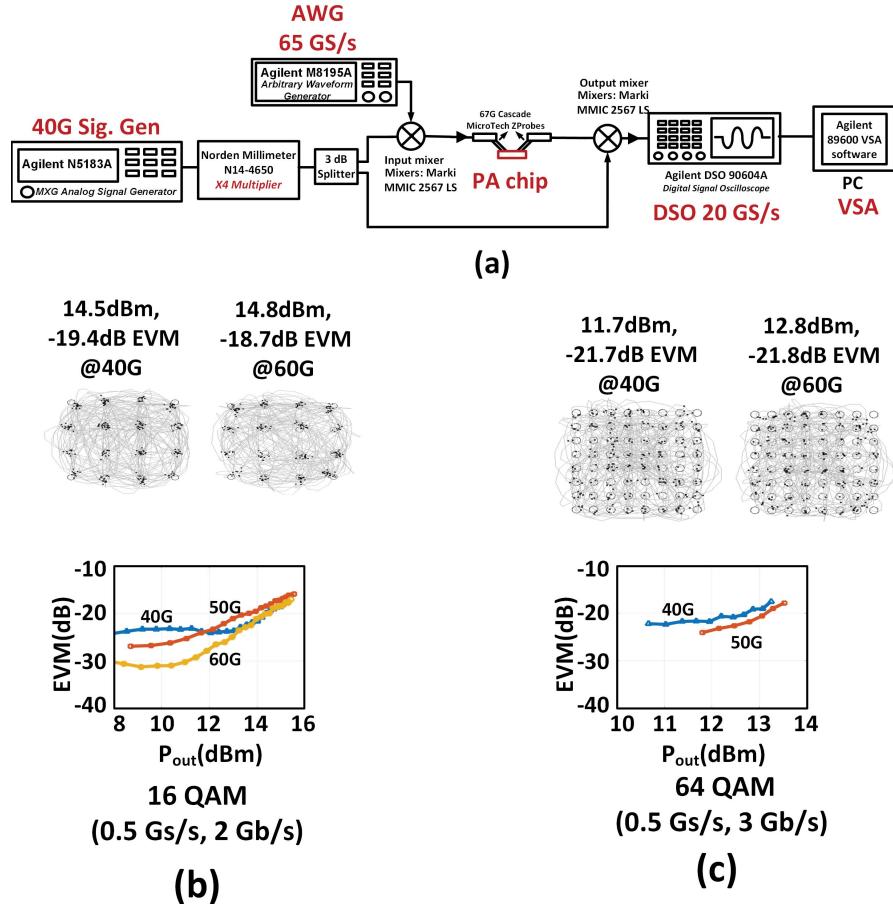


Fig. 28. (a) Measurement setup for non-constant envelope modulation. (b) Measured constellations and EVM variation against output power for (b) 16 QAM at data rate of 2 Gbps at 40 and 60 GHz and (c) 64 QAM at data rate of 3 Gbps at 40 and 60 GHz.

frequency reconfigurable  $P_{\text{sat}} > 22 \text{ dBm}$  with  $\text{PAE}_{\text{peak}} > 25\%$  between 40 and 60 GHz. The reconfigurable  $P_{\text{sat}}$  1-dB bandwidth spans 25 GHz between 40 and 65 GHz, while that of the  $\text{PAE}_{\text{peak}}$  spans between 40 and 60 GHz. The linearity of the PA and its ability to perform with high-efficiency at back-off is indicated by its 1-dB compression measurement. As shown in Fig. 27(b), reconfigurable  $P_{1\text{dB}}$  peaks at 19.9 dBm at a PAE of 15.7% at 55 GHz. The measured variations of  $P_{\text{sat}}$  against frequency for three different reconfiguration states at 45, 55, and 65 GHz are shown in Fig. 27(c).

### C. Measurement With Non-Constant Envelope Modulation

The measurement setup for measuring the PA performance with non-constant envelope modulations is shown in Fig. 28(a). The baseband data from Agilent M8195A arbitrary waveform generator with a sampling rate of 65 GS/s is up-converted through an external mixer as an input to the chip and is later down-converted through an identical mixer, then captured by a real-time oscilloscope with a sampling rate of 20 GS/s, and analyzed through the VSA software on PC. The measured constellations 16 QAM and 64 QAM across 40–60 GHz for data rates of 2 and 3 Gbps, respectively, along with EVM are shown in Fig. 28(b) and (c). EVM of below  $-18.5 \text{ dB}$  for  $P_{\text{avg}} < 14.5 \text{ dBm}$  for 16 QAM and an EVM

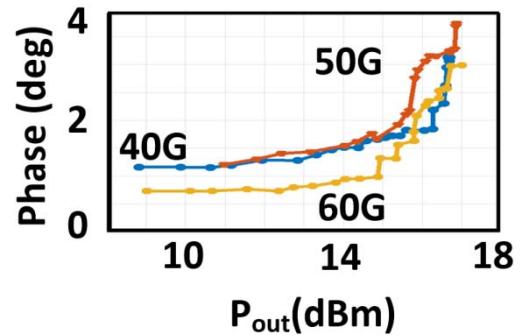


Fig. 29. Measured AM-PM distortion (limited by the nonlinearity of the transmitter mixer used for up-conversion).

of below  $-21 \text{ dB}$  for  $P_{\text{avg}} < 11.7 \text{ dBm}$  for 64 QAM is observed for 40–60 GHz. Currently, the linearity measurement is limited by the linearity of the input mixer, which results in these output power levels fall below the measured  $P_{1\text{dB}}$ . The measured AM-PM distortion between 40 and 60 GHz is shown in Fig. 29. It is measured as the rms phase error of the measured constellation of modulated-QPSK signals corresponding to different power levels. The phase distortion of below  $1.5^\circ$  is observed for output powers below 14 dBm for

TABLE I  
COMPARISON WITH STATE OF THE ART

	This Work	[6]	[11]	[15]	[16]	[17]	[18]	[38]
Frequency of Operation (GHz)	40-65	33-46	40-67	46	41	40-50	57-65	42-54
Technology	0.13μm SiGe	45nm CMOS SOI	28 nm LP CMOS	0.13μm SiGe	0.13μm SiGe	45nm CMOS SOI	65nm LP CMOS	45nm CMOS SOI
Architecture	Asymmetric Two way combiner	8 way combiner	Inductively coupled resonator/Norton transformation	8 way Dynamic Load Modulation	Double stack	2 bit Power DAC	8 way combiner	2 Triple Stacked PA
Peak $P_{\text{sat}}$ (dBm)	23.6 @55G	27.2	13.3	28.9	23.4	23.5-24.3	20.2	22.4@46G
Gain at $P_{\text{sat}}$	18.8 @55G	~12*	~10* @50G	13	14.5	18.3	20*	17.4
Peak PAE (%)	27.7 @55G	10.7	16	18.4	34.9	22-14.6	22.9	42.5
$P_{1\text{dB}}$ (dBm)	19.9 @55G	21	12	-	-	-	17.4	18.6
PAE @ $P_{1\text{dB}}$	15.7 @55G	~5*	14	-	-	-	~10 *	~18*
$P_{\text{sat}},1\text{dB}$ Bandwidth (GHz)	25 (40-65G)	>13(33-46G)	16 (46-62G)	-	>4 (39-43G)*	<10 (40-50G)*	~8 (57-65G)*	~7(42-49G)*
PAE,1dB Bandwidth (GHz)	20 (40-60G)	>13(33-46G)*	20(45-65G)*	-	>4 (39-43G)*	<10*	~5(57-62G)*	~5 (43-48G)*
Modulation/ Data Rate(Gbps)/ EVM (dB)	16QAM (2Gbps) EVM=-21dB @ 14.8dBm (60GHz) 64QAM(3Gbps) EVM=-25dB@ 12.8dBm (60 GHz)***	-	-	ASK (3Gbps) (Simulated)	-	ASK (2Gbps) BPSK (5Gbps)	-	-
Area (mm <sup>2</sup> )	1.02 (0.36**)	4.16	0.33	13.7	1.02	0.77	0.32**	0.28

\*Estimated from the plots.

\*\*Active chip Area.

\*\*\*Currently limited by measurement set-up

40–60 GHz and is also currently limited by the linearity of the input mixer in the measurement setup. Table I summarizes the measured performances of the chip and shows the comparison with the recent state-of-the-art mm-wave PAs in CMOS/SiGe processes.

### VIII. CONCLUSION

In this paper, we propose an active impedance synthesis methodology, which exploits interaction of multiple PA cells in an asymmetric combiner architecture to enable frequency-reconfigurable operation over a broad range of mm-wave frequencies. This paper presents the analysis and design methodologies of the proposed architecture along with detailed comparison with the classical symmetrical architecture. As a proof of concept, an integrated PA implemented in 0.13-μm SiGe BiCMOS process is demonstrated to achieve a peak  $P_{\text{sat}}$  of 23.6 dBm at a peak PAE of 27.7% with a frequency reconfigurable  $P_{\text{sat},-1\text{dB}}$  bandwidth of 25 GHz ranging from 40 to 65 GHz. The PA maintains  $P_{\text{sat}} > 22$  dBm at a PAE > 20% across the frequencies 40–65 GHz. Multi-Gbps data rates with non-constant envelope modulations of 16 QAM and 64 QAM at mm-wave frequencies are demonstrated.

### APPENDIX

Here, we derive some of the relations presented in Section IV describing network synthesis. Transformation of S

parameters between two set of terminating impedances  $Z_{\text{ref},i}$  to  $Z'_{\text{ref},i}$  ( $1 \leq i \leq N$ ) can be achieved as

$$S' = A^{-1} (S - R^H) (I - RS)^{-1} A^H \quad (22)$$

where  $R$  is a diagonal matrix with  $i^{\text{th}}$  diagonal element as  $r_i = (Z'_{\text{ref},i} - Z_{\text{ref},i})/(Z'_{\text{ref},i} + Z^*_{\text{ref},i})$  and  $A$  is a diagonal matrix with  $i^{\text{th}}$  diagonal element  $a_i = \sqrt{|1 - |r_i|^2|} \cdot (1 - r_i^*)/(|1 - r_i|)$  [62]. From Fig. 11,  $Z_{\text{ref},1} = Z'_{\text{ref},1} = Z_{s1}$ ,  $Z_{\text{ref},2} = Z_o$ ,  $Z'_{\text{ref},2} = Z_2||(Z_3 = Z_0)$ . This leads to

$$R = \begin{pmatrix} r_1 & 0 \\ 0 & r_2 \end{pmatrix} \quad (23)$$

where  $r_1 = \frac{(Z_{s1} - Z_{s1})}{(Z_{s1} + Z_{s1})} = 0$ ,  $r_2 = \frac{(Z_2||Z_o - Z_o)}{(Z_2||Z_o + Z_o)} = \frac{-1}{(1 + \frac{Z_2}{Z_o})}$  and

$$A = \begin{pmatrix} a_1 & 0 \\ 0 & a_2 \end{pmatrix} \quad (24)$$

where  $a_1 = 1$ ,  $a_2 = \sqrt{|1 - |r_2|^2|} \cdot (1 - r_2^*)/(|1 - r_2|)$ . This leads to

$$\begin{aligned} S' &= \begin{pmatrix} S_{aa} & S_{aa'} \\ S_{a'a} & S_{a'a'} \end{pmatrix} \\ &= \frac{1}{1 - r_2 s_{22}} \begin{pmatrix} s_{11}(1 - r_2 s_{22}) + s_{12}^2 r_2 & \frac{s_{12} a_2^*}{a_2} a_2^* \\ s_{12} a_2^* & a_2^* \end{pmatrix} \quad (25) \end{aligned}$$

where  $\begin{pmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{pmatrix}$  denotes the S-parameters of the upper two-port network in Fig. 11(a). From the figure, it can be seen that  $\Gamma_1 = s_{11}$  and  $\Gamma_2 = \frac{(Z_2 - Z_o)}{(Z_2 + Z_o)}$  implying  $r_2 = \frac{(\Gamma_2 - 1)}{(\Gamma_2 + 3)}$ . Applying these conditions, and simplifying, we obtain (11).

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**Chandrakanth R. Chappidi** (S'13) received the B.Tech. degree in electronics and electrical communication engineering from IIT Kharagpur, Kharagpur, India, in 2013.

He joined the Prof. Sengupta's Laboratory in 2014. His current research interests lie in exploring the novel reconfigurable techniques in RF and mm-Wave transmitters.

Mr. Chappidi was a recipient of the 2017 IEEE Microwave Theory and Techniques Graduate Fellowship and the 2017 Analog Devices Outstanding Student Designer Award.



**Kaushik Sengupta** (M'12) received the B.Tech. and M.Tech. degrees in electronics and electrical communication engineering from IIT Kharagpur, Kharagpur, India, in 2007, and the M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology (Caltech), Pasadena, CA, USA, in 2008 and 2012, respectively.

He performed research with the University of Southern California, Los Angeles, CA, USA, and the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2005 and 2006, respectively, where he was involved in nonlinear integrated systems for high-purity signal generation and low-power RF identification tags. He joined the Department of Electrical Engineering, Princeton University, Princeton, NJ, USA, as a Faculty Member, in 2013. His current research interests include high-frequency ICs, electromagnetics, and optics for various applications in sensing, imaging, and high-speed communication.

Dr. Sengupta received the Young Investigator Program Award from the Office of Naval Research in 2017. He was enlisted twice in the Princeton Engineering Commendation List, for Outstanding Teaching, in 2014 and 2017. He was a recipient of the Charles Wilts Prize in 2013 from the Department of Electrical Engineering, Caltech, for the best Ph.D. thesis, the Caltech Institute Fellowship, the Prime Minister Gold Medal Award of IIT Kharagpur in 2007, the IBM Ph.D. Fellowship from 2011 to 2012, the IEEE Solid State Circuits Society Predoctoral Achievement Award in 2012, the IEEE Microwave Theory and Techniques Graduate Fellowship in 2012, the Analog Devices Outstanding Student Designer Award in 2011, the Most Innovative Student Project Award of the Indian National Academy of Engineering in 2007, and the IEEE Microwave Theory and Techniques Undergraduate Fellowship in 2006. He was a co-recipient of the IEEE RFIC Symposium Best Student Paper Award in 2012 and the 2015 Microwave Prize from the IEEE Microwave Theory and Techniques Society. He serves on the Technical Program Committee of the IEEE Custom Integrated Circuits Conference and the European Solid-State Circuits Conference.