Bristol Ridge: A 28-nm x86 Performance-Enhanced Microprocessor Through System Power Management

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***Abstract*— Power management techniques can be effective at extracting more performance and energy efficiency out of mature systems on chip (SoCs). For instance, the peak performance of microprocessors is often limited by worst case technology (Vmax), infrastructure (thermal/electrical), and microprocessor usage assumptions. Performance/watt of microprocessors also typically suffers from guard bands associated with the test and binning processes as well as worst case aging/lifetime degradation. Similarly, on multicore processors, shared voltage rails tend to limit the peak performance achievable in low thread count workloads. In this paper, we describe five power management techniques that maximize the per-part performance under the before-mentioned constraints. Using these techniques, we demonstrate a net performance increase of up to 15% depending on the application and TDP of the SoC, implemented on "Bristol Ridge," a 28-nm CMOS, dual-core x86 accelerated processing unit.**

***Index Terms*— Accelerated processing unit (APU), system on chip (SoC), system power management, thermal design power, V_{max} reliability margin.**

I. Introduction

POWER and thermal management are at the forefront of concerns facing modern computing systems. Increasing circuit densities, limitations in technology scaling with respect to voltage and power reductions, dense system packaging, and increasing the cost of advanced cooling and packaging solutions have made power and thermal issues critical across all the classes of computing systems [1]. Bristol Ridge (BR) is Advanced Micro Devices (AMD's) next-generation mobile performance accelerated processing unit (APU). This design is a follow-on of Carrizo [2] and features four Excavator processor cores and eight Radeon TM Graphics Core Next cores. BR is implemented in a 28-nm HKMG planar dual-oxide final test (FT) technology featuring 3 Vts of thin-oxide devices and 12 Cu metal layers. By combining process enhancements with a myriad of system power optimization techniques, significant performance–power differentiation with respect to CZ is achieved [3]. In this paper, we describe these key system power management techniques used on BR, along with the details of the implementation and silicon results.

Manuscript received May 24, 2016; revised October 18, 2016; accepted October 19, 2016. Date of publication November 24, 2016; date of current version January 4, 2017. This paper was approved by Guest Editor Dejan Markovic.

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Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2016.2623637

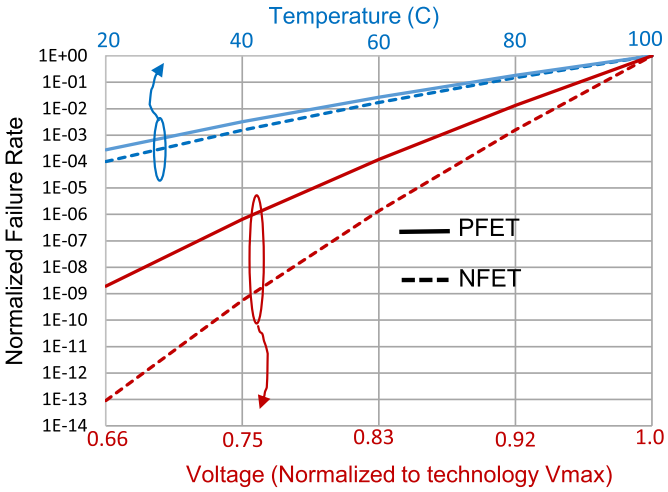

Fig. 1. TDDB failure rate versus temperature/voltage (28 nm).

II. Reliability Tracker

Microprocessors have fundamentally competing requirements between maximizing peak performance, and maintaining the long-term reliability of the silicon. To maximize peak performance, microprocessors want to operate at the highest frequency possible (F_{MAX}) in the boost processor state, which is typically set by the highest operating voltage (V_{MAX}). Nonperformance critical computation can be done in lower voltage and frequency processor states. In thermally limited systems, the maximum operating temperature (T_{MAX}) may become another limiter on F_{MAX}. To maximize product reliability, it is desirable to minimize V_{MAX} and T_{MAX}.

The critical limiters to long-term reliability in a high-performance microprocessor are time-dependent dielectric breakdown (TDDB) and electromigration (EM) [4]–[6]. The TDDB is strongly dependent on voltage and moderately dependent on temperature, as shown in Fig. 1, which shows the normalized TDDB failure rate of thin-oxide nFET and pFET devices in a 28-nm process technology. On the other hand, EM is enormously dependent on temperature and

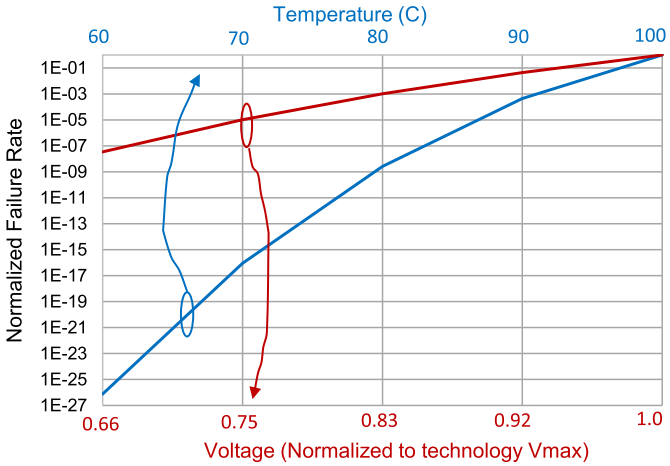

Fig. 2. EM failure rate versus temperature/voltage for copper interconnect (28 nm).

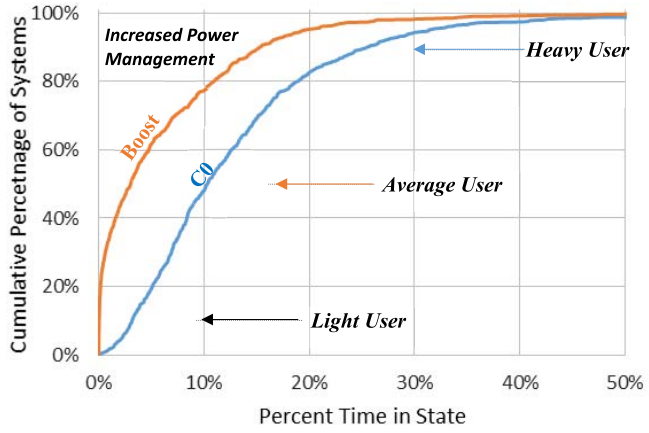

Fig. 3. C0, boost usage over a population of 810 systems.

strongly dependent on voltage, as shown in Fig. 2, which shows the normalized EM failure rate of copper interconnect. The failure rate can vary many orders of magnitude over the typical range of operating conditions found in microprocessors for desktop and laptop systems.

Standard microprocessor design assumes worst case conditions on voltage and temperature when designing for long-term reliability targets. That is, the microprocessor operates at V_{MAX} and T_{MAX} over the entire lifetime of the product. However, in modern microprocessors with sophisticated power management algorithms margining for the worst case V_{MAX} and T_{MAX} leaves an immense amount of performance unrealized, since the microprocessor only operates at maximum voltage and temperature a very small fraction of the product lifetime. Taking advantage of this can allow the same microprocessor silicon to deliver appreciably more performance.

A. Usage Model

For multiple generations of microprocessors, AMD has utilized a static usage model to eliminate ultraconservative constraints on their design. Based on internal field studies, microprocessor utilization models have been developed, which account for varying time spent in different processor states in terms of voltage and frequency, and more importantly, model the time a microprocessor is expected to be in a powered down state.

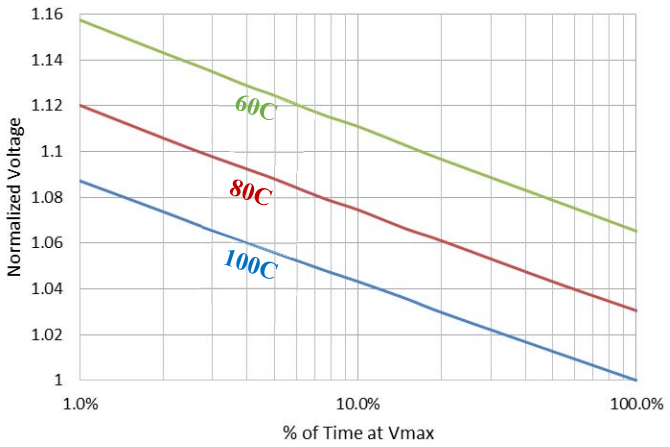

Fig. 4. Increase in normalized voltage versus percentage of lifetime spent at maximum voltage.

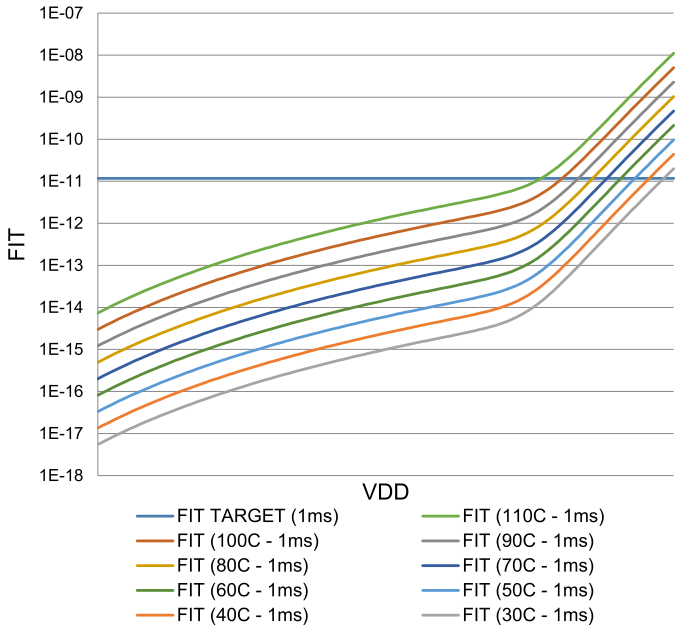

Fig. 5. FIT as a function of voltage and temperature and FIT target.

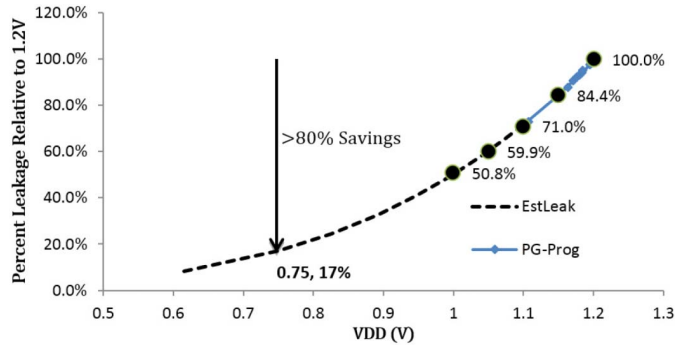

Fig. 6. Measured leakage power on 28-nm AMD x86-64 Core.

Since a static usage model is used to represent all users' behavior, the final operating margins must still be sufficiently conservative to prevent earlier failure, resulting in field failure rates beyond the target product specification. Fig. 3 shows the distribution of system C0 residency (CPU is active) measured from a population study of 810 client systems. Improving power management algorithms has the effect of shifting the

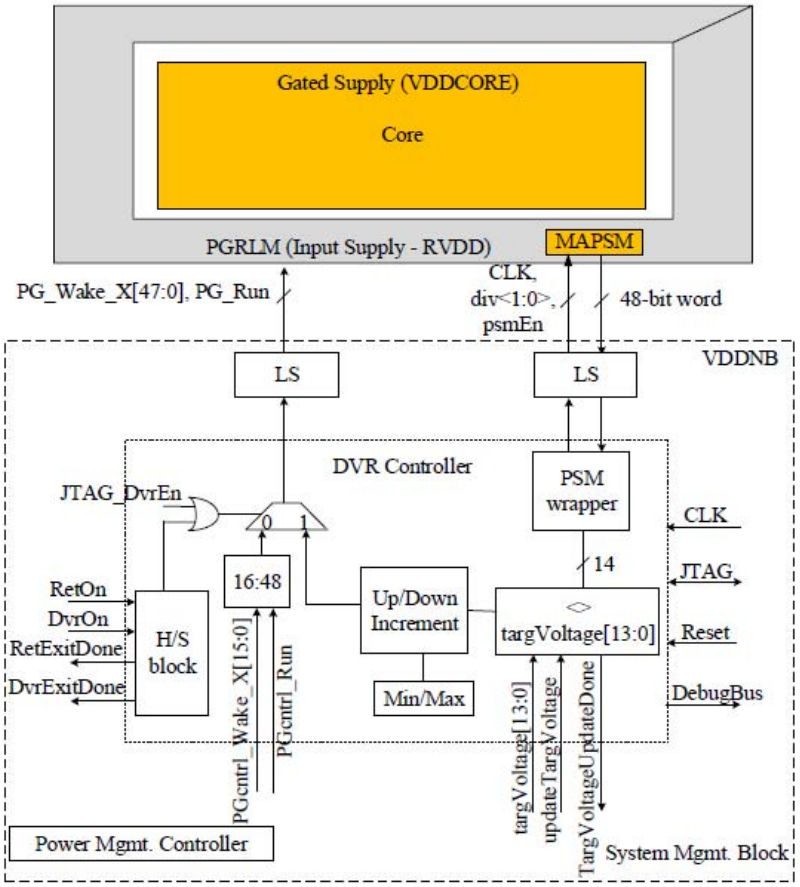

Fig. 7. LDO Controller.

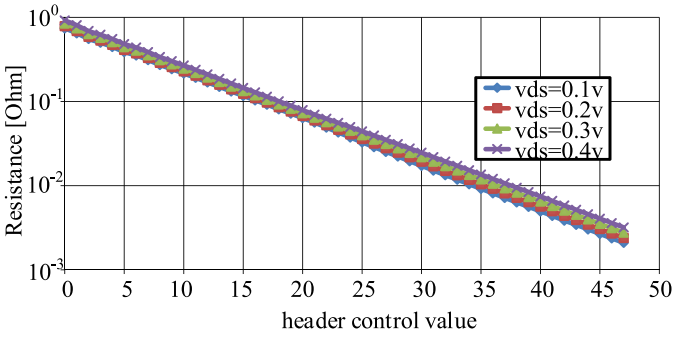

Fig. 8. PG header resistance across 48 WAKE states.

curves to the left. While the CPU is active, the fraction of time spent in boost is given in Fig. 3, and shows that the overwhelming majority of users utilize the microprocessor in its maximum boost state at V_{MAX} and F_{MAX} only a small portion of the time.

This fact can be used to raise the allowable V_{MAX}, as shown in Fig. 4, in the range of 4%–9% when the amount of time spent at V_{MAX} is in the range of 1%–10% (at constant temperature). This allows the microprocessor to deliver higher frequency in the top-most microprocessor boost state. In addition, roughly an extra 1.5% voltage increase can be achieved for every 10 °C of temperature headroom.

With the static usage model, worst case assumptions were made for temperature, adding unnecessary conservatism. The dynamic power management algorithms in modern microprocessors utilize on-die voltage and temperature sensors,

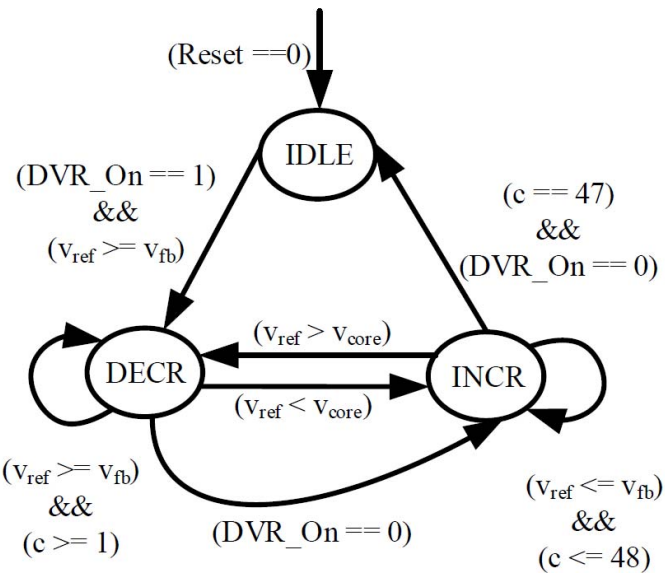

Fig. 9. DVR controller state machine.

which can be co-opted to monitor reliability wear-out in real-time.

B. Real-Time Reliability Monitoring

BR utilizes a reliability tracker to dynamically monitor the operating conditions for each compute unit, including the voltage (V_{DD}) and temperature (T), and estimates an aggregate

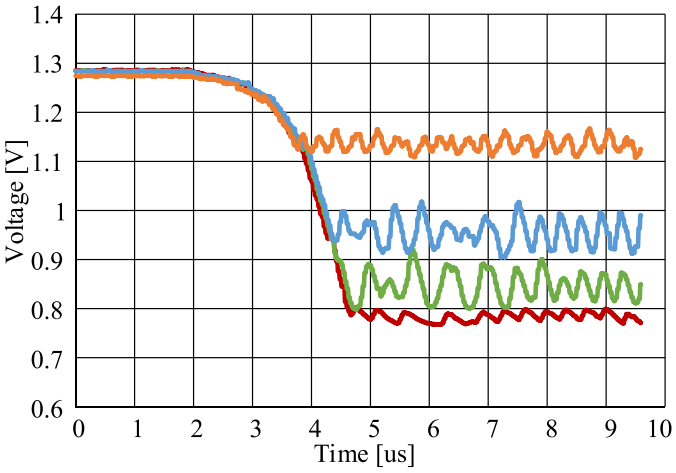

Fig. 10. Core measured on-die voltage, core frequency at 200 MHz.

failure, or FIT, rate for the TDDB and the EM in 1-ms increments, as shown in

$$\text{FIT} = k_{\text{TDDB}} \cdot e^{a_{\text{TDDB}} \cdot T} \cdot V_{\text{DD}}^{b_{\text{TDDB}}} + k_{\text{EM}} \cdot e^{a_{\text{EM}} \cdot T} \cdot V_{\text{DD}}^{b_{\text{EM}}} \tag{1}$$

where the subscripted variables are curve-fit from foundry process reliability models. The FIT rate is a function of voltage and temperature as shown in Fig. 5. In order to meet the long-term product reliability requirements, the incremental FIT must remain lower than the specified FIT target.

The FIT rate is calculated in 1-ms increments, faster than the frequency of P-State changes, so that only one V_{DD} and temperature measurement is required per interval. The results are then filtered to prevent fast P-State dithering

$$\text{FIT\_filtered}_N = \alpha \cdot \text{FIT} + (1 - \alpha) \cdot \text{FIT\_filtered}_{N-1}. \tag{2}$$

When the FIT_filtered_N is below the target threshold, then a higher-frequency P-State is made available, increasing F_{MAX}. When FIT_filtered_N is above the target threshold, this extra P-State is locked out, to prevent early microprocessor failure during the product lifetime.

Thus, by dynamically monitoring the processor cores voltage and temperature, the overwhelming majority of users can realize an extra 100 MHz increase in F_{MAX} while staying within long-term reliability targets, by allowing lower operating temperatures to enabled higher V_{MAX}. In addition, even heavy users can realize an extra frequency boost with customized product cooling solutions. This increase is on top of the 4%–9% improvement in V_{MAX} as afforded by the use of the static usage model.

III. Digital LDO

When a conventional CPU core is power gated, its voltage can fall as low as 0.1–0.2 V, depending on core and header design. Leakage power dissipation is thus virtually eliminated, leading to significant power savings. In a multicore processor that is power-limited, this scenario usually enables frequency boosting of one or more of the active cores, due to the additional available power coming from leakage savings.

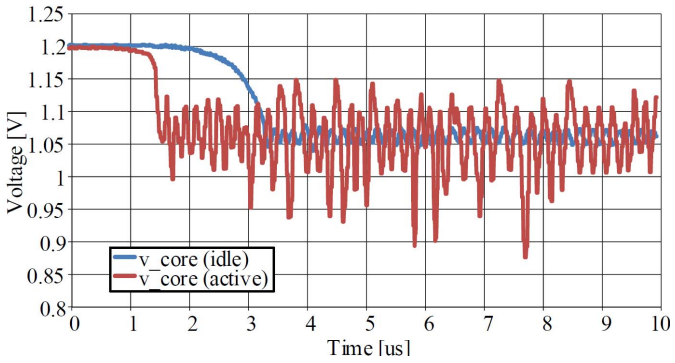

Fig. 11. Core active mode versus idle mode measured on-die voltage, core frequency at 800 MHz.

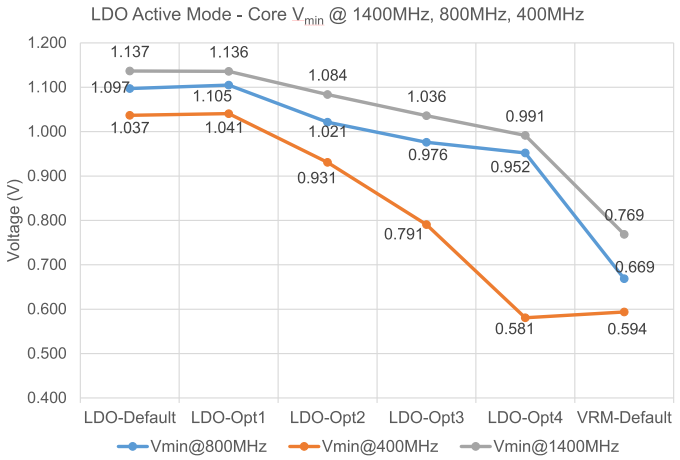

Fig. 12. LDO results.

Note that the state of sequential elements is lost at conventional power gating voltages. It is thus necessary to save and restore the state of the core (includes flushing of L1 and L2 cache memories) when entering/exiting power gating mode. This process causes significant entry and exit latencies, thus limiting the effectiveness of this technique for workloads with very frequent and short durations of idle state: for instance, if entering/exiting power gating implies an overhead of 100 μs, the system power management logic typically decides to go into this mode only if the core is in an idle state for longer than 1 ms. For shorter times, the power savings are not worth the latency. Therefore, in some relevant practical cases, full advantage of power gating is not realizable [7], [8].

For BR, we developed a fully digital voltage regulation system (DVR) that reuses conventional power gating header switches as digitally controlled resistors to drop the core voltage to the minimum voltage at which the sequential elements retain their state, V_{ret} (approximately 0.55 V in 28-nm technology). Fig. 6 indicates that significant amount of leakage power can still be saved without entering a true power gating state: for instance, greater than 80% of the leakage power can be saved at 0.7 V compared with 1.2 V. The DVR system enables fast voltage transitions ($>10\times$ improvement in latency), therefore offering an upside on performance and power efficiency for certain important processor use cases. Note that this technique can be applied to other building blocks of integrated circuits or systems on chip (SoCs).

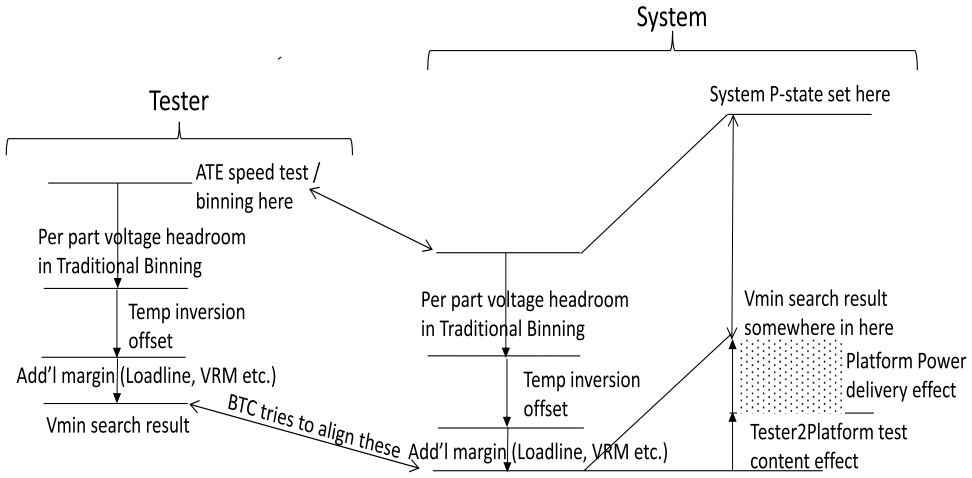

Fig. 13. Aligning test voltage to a real system.

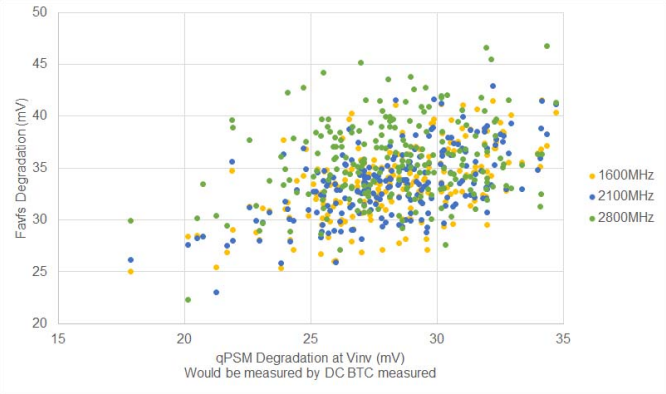

Fig. 14. BTC estimated aging from PSM counts (X) is highly correlated with actual paths aging (Y) across large operating range.

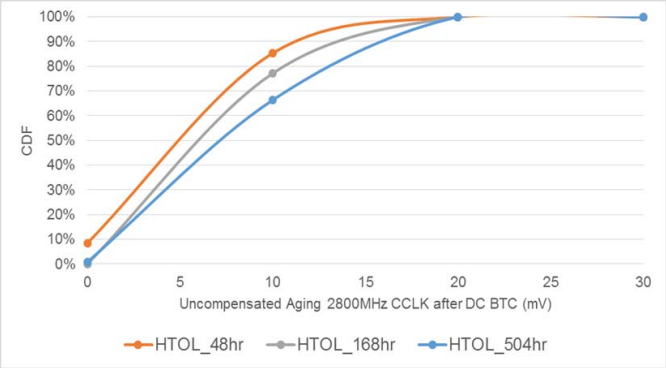

Fig. 15. PSM aging trend with time matches that of actual functional critical paths aging.

Fig. 7 shows the architecture of the fully digital on-die voltage regulation system (DVR). The DVR controller runs on a 100-MHz, fixed frequency clock. The system includes a time-to-digital converter that acts as a power supply monitor (PSM) to sample the core voltage; a 48-b thermometer code word that controls a set of pFET headers distributed along the edges of the core; and a digital controller that increments or decrements the 48-b control word to regulate the processor voltage to a target value. Fig. 8 shows the simulated total header resistance versus control word. This feedback system provides safe retention in the presence of input power supply and temperature changes. Entry and exit times of the "retention state" are in the 1–3 μs range, providing compelling advantage over full power-gating mode, where latencies are longer than 10 μs. The power headers that would be used for regular power gating are repurposed as a digitally controlled series resistance, in order to drop voltage from an input supply shared with another core in the chip. This approach results in virtually no overhead to the design. Area overhead of the controller is smaller than 4000 μm^2.

Fig. 9 shows the DVR controller state machine logic. During normal core operation, the controller is in IDLE state and all power gates are tuned ON. When the power management logic decides to enter regulation mode, the controller goes into DECR mode and begins increasing the resistance. The core voltage measured by the PSM (V_{fb}) is compared against a target value (V_{ref}), and the sign of the result causes the control word to be incremented/decremented to move to higher/lower resistance. Upon exit, the state machine enters INCR mode until all power gates are turned ON.

Fig. 10 shows measured on-die core voltage, for different target output voltages and $V_{\text{in}} = 1.275$ V. The core is running at low frequency (200 MHz) but remains active. Fig. 11 shows additional silicon results using the DVR system. In this case, the regulated core is kept in idle mode (blue curve), and running a worst case noise-inducing pattern at 800 MHz (red curve). The core is verified to be stable and completely functional both in active mode and idle mode. The key point is that on-die regulation is able to regulate effectively and maintain the low-frequency state operation without any voltage overhead. Any noise as observed on the regulated supply is compensated by the core's on-die adaptive clocking techniques.

The DVR system described in this paper allows us to operate one of the in *core idle/retention mode* and *core active mode*, in addition to traditional *power gating mode*, where the core is fully power gated (lowest power state). We can program the system to operate efficiently by leveraging each of these power states. Upon power and performance tradeoff analysis, *core active mode* was determined to give the best

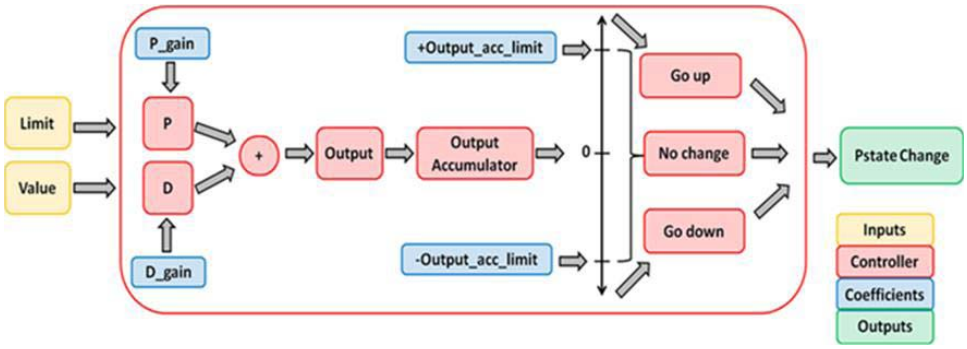

Fig. 16. STAPM controller.

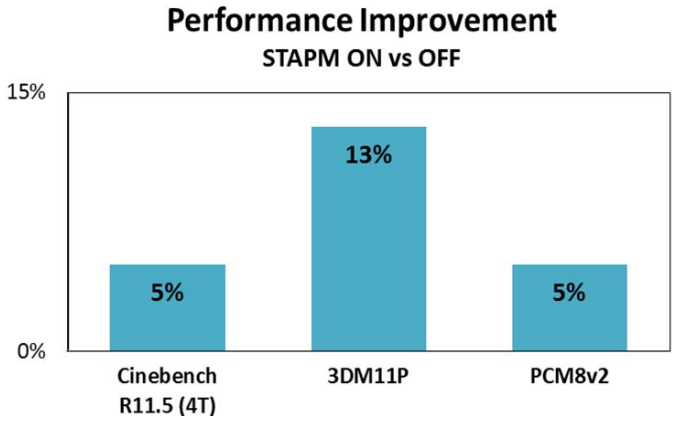

Fig. 17. STAPM performance improvement across various benchmarks.

uplift in performance. A new Pstate, $P_{\min}$, was defined in this mode, and made available to the system management control. Below table shows the effective frequency benefit we get in BR with lightly threaded applications using the new $P_{\min}$ state, with the other core in *C-state boost* mode. This feature is a mechanism, which allows active cores to exceed the normal P1 (configurable) P-State to a P0 boost P-State, if enough of the cores are in a low-power (e.g., CC6) state. *C-state boost* is a major performance contributor for lightly threaded workloads. An effective frequency increase of 6.2% is achieved in BR using the newly defined $P_{\min}$ state and *C-state boost*.

	C6 + CStateBoost	Pmin+CstateBoost
CState Boost Frequency	3.87 GHz	3.70 GHz
All State Boost Frequency	3.01 GHz	3.01 GHz
Effective Frequency	3.35 GHz	3.56 GHz (+6.2%)

It is worth noting that, as the controller runs on a relatively slow 100-MHz clock and there are no charge reserves on a low-impedance path to quickly source sudden current demand (no package capacitance was added to the regulated node), $P_{\min}$ includes deep architectural throttles to temper the di/dt droops. These techniques include "single issue operation," "disable branch prediction," and "nonspeculative operation." In $P_{\min}$, the core can safely operate at 800 MHz/0.95 V with a worst case current transient workload, as shown in Fig. 11. Fig. 12 shows the measured $V_{\min}$ for a worst case workload when operating the DVR system, with the different architectural throttles enabled. The default [voltage regulator module (VRM)] $V_{\min}$ voltage is also shown.

Summarizing, $P_{\min}$ can be used to provide similar power savings as conventional CC6 but faster exit latency and cache/core state retention, reducing idle transition latency by removing the need to flush the cache. The DVR system enables maximum residency in $P_{\min}$, raising the performance of lightly threaded workloads, since more time is spent in the *C-state boost* state, resulting in net performance gain of ∼6% in these scenarios.

IV. Boot-Time Calibration

Traditional binning includes fixed voltage margin to cover for VRM dc tolerance and package variations. However, most reference systems offer tighter voltage delivery than worst case specification. The voltage level is tracked in BR using on-die PSMs [9]. By comparing the PSM voltage in a quiescent condition during system "boot," with those on ATE, boot-time calibration (BTC) can accurately calibrate the dc component of the power supply difference. One difficulty with using the PSM count as reference is that the PSM count is dependent not only on voltage but also temperature. Also, there is no way to guarantee the system temperature at boot time will be same as the temperature at FT when the PSM voltage trends are fused into the part. In order to circumvent this issue and tune out the temperature dependence, BTC is carried out at the "temperature inversion" voltage (or $V_{\text{inversion}}$). This voltage represents the point at which transistor delay is virtually insensitive to temperature. To accomplish this, the voltage trends of the PSMs are characterized both at wafer sort, −5 °C, as well as FT, 100 °C. This allows the on-die system management unit to infer a unique per-part $V_{\text{inversion}}$ point at which PSM count can be compared with the reference FT count without any temperature related error. In this fashion, the BTC mechanism to accurately gauge the system dc loss.

The ac component of the voltage droop on a platform is quite different when compared with ATE due to power delivery and workload differences. For instance, ATE voltage droop at highest operating $F_{\max}$ is about 50 mV, while in systems, it is closer to 200 mV. BTC employs a smart platform-specific calibration of per-part ac voltage droop as a function of frequency, temperature and per-part leakage, switching capacitance, and droop measured on ATE. These dc and ac voltage droop components, as measured by BTC, allow the removal of worst case margins. Fig. 13 shows how

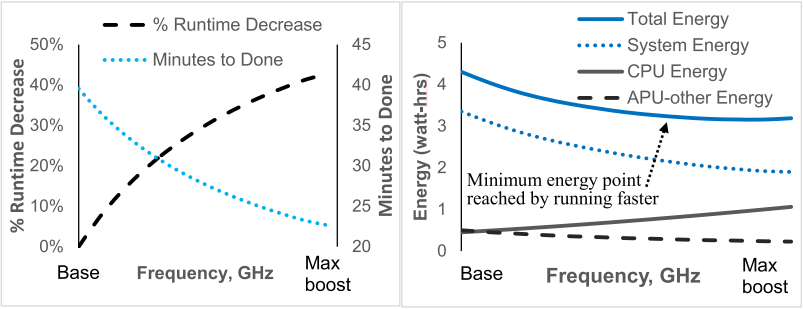

Fig. 18. STAPM achieves net system energy savings for running CPU "faster."

the voltages are aligned. The voltage savings from BTC on BR, on average, were measured to be ∼30 mV.

In addition, BTC allows for novel tracking of per-part aging behavior. Traditionally, binning would add a worst case margin to cover for aging (HCI/xBTI) effects over the target usage profile of the product. In contrast, since BTC now captures the PSM count of the part at each boot cycle and compares it to a fixed reference count measured originally on ATE, we theorize that the voltage margin added will increase naturally over time as the part (and hence PSM) ages. One key piece of data to enable this feature was to confirm that PSM aging trends in fact align with the functional critical paths on the design. In order to verify this, during high temperature operating life data collection, we collected both the PSM circuit aging and actual critical path aging on the chip. As shown in Fig. 14, the threshold voltage (V_t) degradation observed on the PSM matches well with the functional paths. In addition, we also prove that the aging trend with respect to time is also well matched between PSM and functional critical paths (Fig. 15). As a result, we can reduce the explicit aging guard band resulting in ∼20 mV of additional savings.

V. Shadow P-States

A critical path accumulator-based scheme to accurately assess true Si speed capability and address the problem of voltage margin reduction in traditional binning flows was briefly reported in [10]. While this original implementation was aimed at optimizing the per-part voltage required for target P-State frequency, in the BR implementation of AVFS, we use shadow Pstate to increase peak frequency on part-by-part basis directly when headroom is available. The peak $F_{\max}$ of the product is generally limited by technology ($V_{\max}$) or by infrastructure (EDC) limits. In traditional power binning flow, each part frequency capability in the system is not precisely known. As a result, the peak frequency is set conservatively to a worst case value that can be met by target distribution of parts. Instead AVFS allows us to exactly characterize the part-specific $F_{\max}$ capability, and BTC allows us to characterize the platform-specific power delivery margin. So instead of restricting to worst case power binned $F_{\max}$, at boot-time, we combine AVFS and BTC to build a frequency–voltage curve for a given part in a given platform. By solving along this curve, we can find the peak feasible frequency for this part under reliability $V_{\max}$ constraints. Similarly, by combining the per-part unique leakage and active power fuses with the frequency–voltage curve, we can determine the highest feasible frequency that meets the regulator supply current specifications. We refer to these peak boost frequencies that meet the infrastructure limits (electrical design current and process $V_{\max}$), as shadow P-States. In BR, shadow P-States enable peak boost frequencies, on average, to increase by 100 MHz over conservative traditional binning.

VI. STAPM

Skin temperature-aware power management (STAPM) improves performance by boosting APU CPU and/or GPU frequencies for as long as the estimated platform skin temperature remains below the specified limit. This can result in significant performance improvements for some benchmarks, enhanced user-experience, and even improved battery life for race-to-idle computations.

BR STAPM models the thermal capacitance of the platform using a simple alpha filter applied to the calculated APU power. This alpha-filtered APU power is proportional to skin temperature. Alpha-filter coefficients can be optimized by characterizing the chassis skin temperature response to APU power.

Fig. 16 shows the details of the controller. In mission-mode, skin temperature is controlled by controlling APU power with a proportional + derivative + accumulator algorithm in system management firmware. The inputs are an APU power limit that is proportional to the skin temperature limit and the alpha-filtered APU power. The output is a sequence of P-State assignments, whose residency profile results in an effective CPU or GPU frequency.

Fig. 17 shows how the benefits from STAPM varies across workloads. We included measured data from the CineBench, 3-DMark, and PCMark suites, and have demonstrated energy savings in the range of 5%–13% made possible by STAPM. Fig. 18 outlines the underlying principle of STAPM. Essentially, by allowing the core(s) to run at boost frequencies for short periods of time, we can reduce the "time to completion," The additional power from running the CPU faster is easily compensated, since it enables other system and SoC components to be put into low power sleep modes sooner. Thus, net platform energy savings are obtained overall from enabling STAPM.

VII. Conclusion

In this paper, we provided a detailed description of five power management techniques that provide a net performance

increase of up to 15% (depending on the application and TDP of the SoC), implemented on "BR," a 28-nm CMOS, dual-core x86 APU. Reliability tracker is a novel method of tracking and leveraging the fact that a microprocessor only operates at maximum voltage and temperature a very small fraction of the product lifetime. This allows the same microprocessor silicon to "reliably" deliver appreciably more performance with respect to the traditional approach to margin for the worst case assumption that the microprocessor operates at V_{MAX} and T_{MAX} over the entire lifetime of the product. Digital LDO is a fully digital voltage regulation system (DVR) that reuses conventional power gating header switches as digitally controlled resistors to drop the core voltage to the minimum voltage at which the sequential elements retain their state, V_{ret} (approximately 0.55 V in 28-nm technology). Given the $>10\times$ improvement in latency, the proposed active mode regulation offers up to 6% increase in performance and power efficiency for certain important processor use cases. BTC uses on-die PSMs to accurately calibrate the dc component of the VRM tolerance as well as aging margin required by part over time. This replaces the traditional beginning methodology, where the worst case margins are applied to the product for the entire lifetime, and measured savings on BR across multiple CPU Pstates upto 50 mV. Shadow P-States builds on the AVFS scheme from prior generation by maximizing the peak F_{max} on a per-part basis, under infrastructure (EDC) and process technology (V_{max}) constraints. This enabled upto 100-MHz improvement on average across large proportion of BR parts. Ultimately, STAPM uses a thermal capacitance model to estimate the platform skin temperature, and improves performance by boosting APU CPU and/or GPU frequencies for as long as the estimated platform skin temperature remains below the specified limit.

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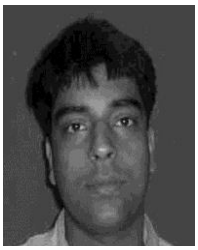

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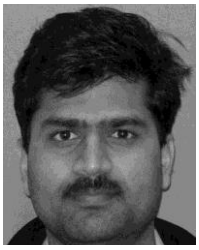

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