

Implicit Common-Mode Resonance in LC Oscillators

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Abstract—The performance of a differential *LC* oscillator can be enhanced by resonating the common mode of the circuit at twice the oscillation frequency. When this technique is correctly employed, *Q*-degradation due to the triode operation of the differential pair is eliminated and flicker noise is nulled. Until recently, one or more tail inductors have been used to achieve this common-mode resonance. In this paper, we demonstrate that additional inductors are not strictly necessary by showing that common-mode resonance can be obtained using a single tank. We present an NMOS architecture that uses a single differential inductor and a CMOS design that uses a single transformer. Prototypes are presented that achieve figure-of-merits of 192 and 195 dBc/Hz, respectively.

Index Terms—Oscillators, phase noise, voltage-controlled oscillators, dual resonance, common-mode resonance, LC.

I. INTRODUCTION

COMMON-MODE resonance is a powerful way of lowering the phase noise of an *LC* oscillator. The technique, introduced by Hegazi *et al.* [1], employs a tuned common-mode tank that resonates at twice the oscillation frequency and prevents the differential pair from loading the tank during triode operation [Fig. 1(a)]. Despite the work being published back in 2001, the reported figure of merit (*FOM*) remains state of the art. This enduring performance can be attributed to the fact that the quality factor (*Q*) of an inductor has not improved over the intervening years, and to the fact that the topology's noise factor and efficiency both approach theoretical limits.

A potential drawback of Hegazi *et al.*'s VCO is the requirement for an extra inductor and, in the case of a wideband design, the need to tune it along with the main tank. In addition, an overlooked aspect of the design is that the common-mode impedance of the main tank at $2f_{\text{LO}}$ can alter the oscillator's common-mode resonance point and can degrade the effectiveness of the tail inductor. Seeking to mitigate these issues, this paper analyzes a new oscillator topology that resonates the common mode of the circuit at $2f_{\text{LO}}$ without an additional inductor [2]. The new topology relies on a single tank that has two distinct modes: a differential mode that resonates at the desired oscillation frequency, and a common mode that resonates at twice the oscillation

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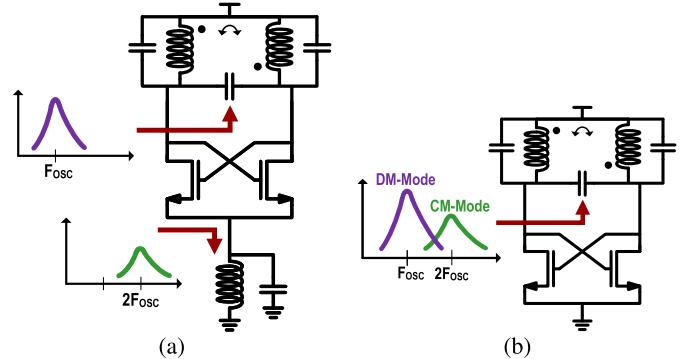


Fig. 1. Common-mode resonance topologies. (a) Original topology. (b) Proposed topology.

frequency [Fig. 1(b)]. A fully complementary version of the design is also discussed [3].

In Section II, we present a simplified discussion on the upper bound of *LC* oscillator performance. In Section III, we show how and why Hegazi *et al.*'s common-mode topology approaches this upper bound, and we introduce the proposed *implicit common-mode* topologies that match Hegazi *et al.*'s performance. We will also compare the proposed technique to other recently published designs that utilize a similar form of implicit common-mode resonance [4]–[7]. The importance of loop gain is discussed in Section IV. Measurement results from two different prototypes are presented in Section V, while Section VI discusses the practical limitations of the design. The conclusions are drawn in Section VII.

II. OPTIMUM CMOS *LC* OSCILLATOR PERFORMANCE

The oscillator *FOM* normalizes phase noise for oscillation frequency, carrier offset, and power [8]. Its definition is

$$FOM = \frac{\left(\frac{\omega_c}{\Delta\omega}\right)^2}{\mathcal{L}\{\Delta\omega\}P_{DC[mW]}}. \quad (1)$$

Fig. 2 shows the reported *FOM* for some of the most widely cited *LC* VCOs over the last 15 years. Remarkably, over this period, the *FOM* metric has not improved, and a clear upper limit of around 194–196 dBc/Hz is seen, which has been achieved by Hegazi *et al.*'s VCO, the Class-C VCO [9], and more recently by a CMOS design that also employs common-mode resonance [10].

To understand why *FOMs* have plateaued, it is instructive to rewrite the expression for *FOM* in terms of oscillator efficiency η and noise factor F [11]

$$FOM = \frac{2\eta Q^2}{kTF} 10^{-3} \quad (2)$$

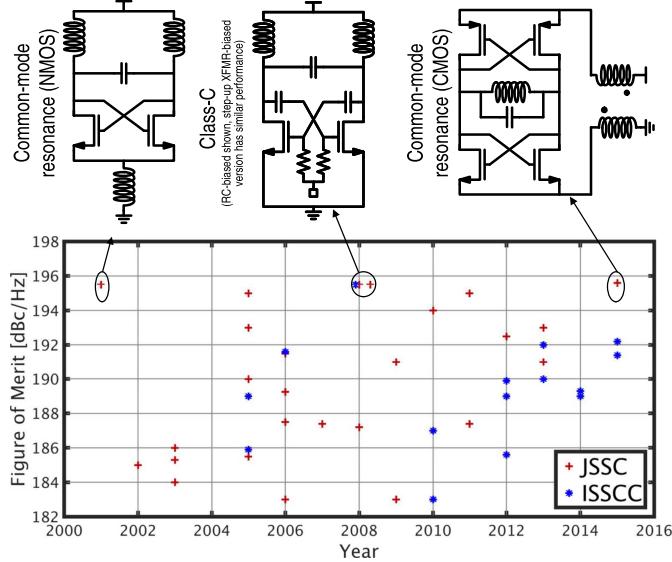


Fig. 2. Reported *FOMs* for the most cited LC VCOs. Among the best reported numbers are the NMOS [1] and CMOS [10] common-mode resonance topologies and the class-C VCO [9], [19].

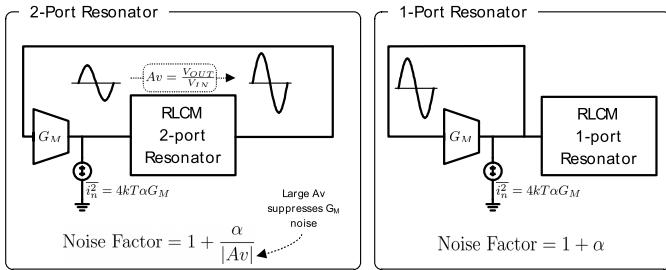


Fig. 3. Distinction between oscillators using two-port and one-port resonators.

where $\eta = P_{\text{TANK[mW]}}/P_{\text{DC[mW]}}$, the power dissipated in the tank is $P_{\text{TANK[mW]}} = A_c^2/(2R_p)$, the oscillation amplitude is A_c , and the equivalent tank loss is given by R_p . Now, as described by Mazzanti and Bevilacqua [12], if an oscillator is partitioned into a two-port reactive element and a memoryless conductance, as shown in Fig. 3, the noise figure is $F = 1 + \alpha/|A_v|$, where α is a constant that relates the noise current of the conductance with its instantaneous conductance, and A_v is the voltage gain across the two-port resonator. Accordingly, as $|A_v|$ becomes very large, conductance noise is suppressed, F approaches one, and the optimum *FOM*, in dBc/Hz, becomes

$$FOM_{\text{MAX}} = 176.8 + 20 \log_{10} Q \quad (3)$$

which is equal to the *FOM* of an 100%-efficient oscillator with a noiseless conductance quoted in [13].

While excellent results (particularily in terms of flicker noise suppression) have been achieved using this “step-up” technique [4]–[7], [9], making $|A_v| > 1$ can be problematic. First, in order to maximize oscillator efficiency, the swing at the output of the conductance should always be maximized, which in the case of a CMOS conductance means that the swing will be $V_{\text{DRAIN}} = V_{\text{DD}}$ or, in the case of an NMOS-only or PMOS-only conductance, will be $V_{\text{DRAIN}} = 2V_{\text{DD}}$.

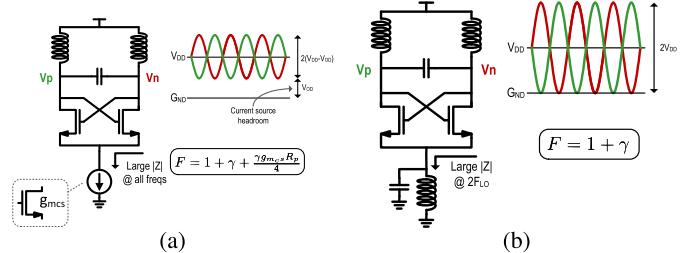


Fig. 4. Replacing the current source with a tuned tank enables rail-to-rail swing. (a) Class-B VCO. (b) Tail-tuning VCO.

Consequently, the swing at the input of the conductance will be $|A_v|V_{\text{DRAIN}}$, which can compromise reliability if a large A_v is employed. Second, the step-up transformer used in such a design should not result in an effective tank Q (i.e., the Q of the impedance parameter Z_{21} of the two-port tank [12]) that is degraded with respect to the Q of a tank that uses a single inductor occupying the same area. Although these issues can be managed, such designs do not currently outperform designs with $|A_v| = 1$, which corresponds to the one-port oscillator also shown in Fig. 3. In the case of this one-port design, the optimum *FOM* becomes

$$FOM_{\text{MAX(1PORT)}} = 176.8 + 20 \log_{10} Q + 10 \log 10(1 + \alpha). \quad (4)$$

When a single transistor or a differential pair is used as the negative conductance, the noise coefficient α is approximately equal to $\gamma = 2/3$ and, so, the one-port limit becomes $174.6 + 20 \log_{10} Q$, which is only 2.2 dB less than optimal.¹ As will be shown in Section III, the use of common-mode resonance results in a topology that gets within 1 dB of this one-port limit and 3 dB of the absolute limit.

III. COMMON-MODE RESONANCE

Consider the standard class-B oscillator shown in Fig. 4(a). Ignoring device capacitance and assuming current-limited operation, the noise factor of the circuit is [15]

$$F = 1 + \gamma + \frac{\gamma g_{m_{\text{CS}}} R_p}{4} \quad (5)$$

where the second term corresponds to the contribution of the differential pair, and the third term corresponds to the contribution of the current source. The third term can be minimized by reducing the transconductance of the current source device, $g_{m_{\text{CS}}}$, which, for a given current, corresponds to an increase in the overdrive voltage of the device. Increasing the overdrive voltage, however, results in an increase in the current source headroom requirement, which in turn limits oscillator efficiency. This tradeoff between efficiency and noise factor means that the achievable *FOM*, which occurs when the overdrive voltage of the current source is $\approx V_{\text{DD}}/2$, is approximately 10 dB less than optimal [13], [14].²

¹In [2], [3], [11], and [14], it was erroneously stated that optimal achievable value of η/F was $1/(1 + \gamma)$. The implicit assumption in that analysis is the constraint that $A_v \leq 1$. Given the analysis in [12], it is more correct to state that $\eta/F = 1/(1 + \gamma)$ is the limit for a one-port oscillator with a CMOS conductance.

²Reference [14] quotes a number of 7.5 dB because of a comparison with a one-port rather than a two-port oscillator.

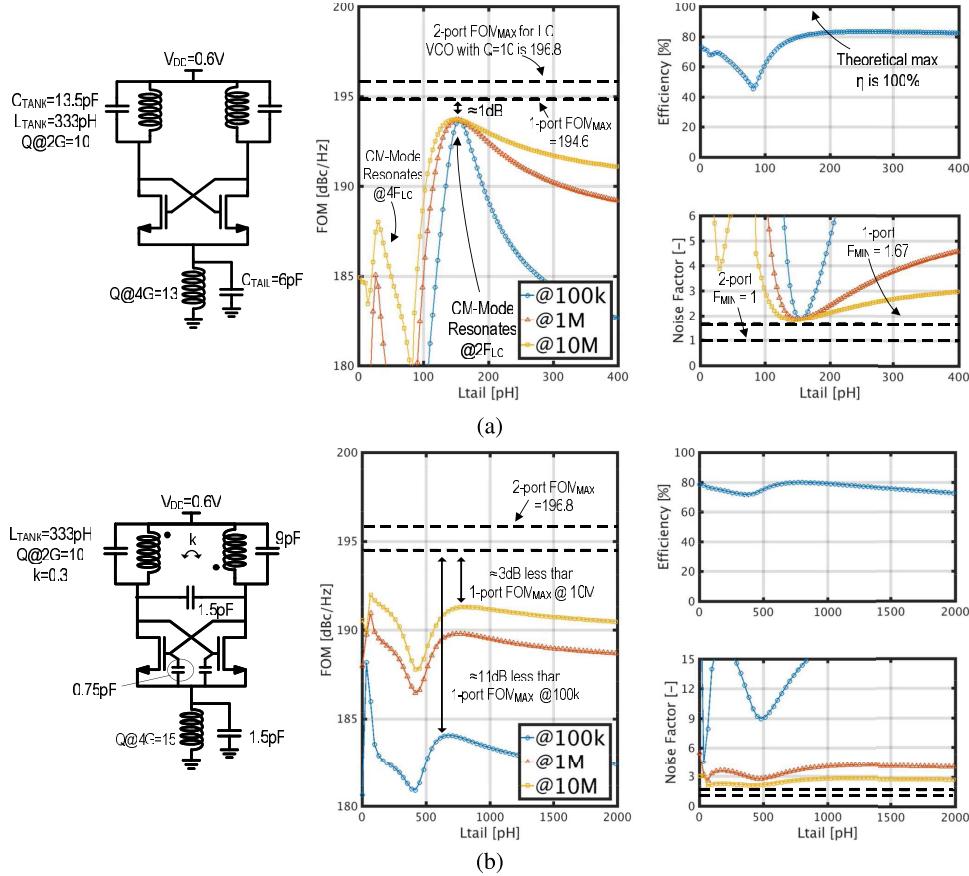


Fig. 5. Example of common-mode resonant designs. (a) Optimal common-mode resonant design. (b) Suboptimal common-mode resonant design.

Hegazi *et al.* break this inherent tradeoff by noting that the current source only needs to present a high impedance at $2f_{LO}$. Therefore, the current source can be removed and replaced with a $2f_{LO}$ resonant tank [Fig. 4(b)]. In this case, the noise factor drops to $1 + \gamma$ and the output swing becomes rail-to-rail, which allows the efficiency to approach 80% (in the presence of a tuned tail resonator, the current switched into the main tank is no longer square wave and, so, efficiency is not limited to $\eta = 2/\pi$). In other words, the topology gets within 3 dB of the theoretical maximum described in (3).³

A. Explicit Common-Mode Resonance

An always ignored feature of Hegazi *et al.*'s design is that the common mode of the main tank and device capacitance can play a large role in the effectiveness of $2f_{LO}$ resonance. First, consider the version of Hegazi *et al.*'s design with the values highlighted in Fig 5(a). Plotting FOM versus L_{TAIL} , a clear maximum is seen when L_{TAIL} resonates with C_{TAIL} . If F and η are plotted separately, we can see that each approaches their optimum values. Now consider the instructive (but contrived) case where C_{TAIL} is reduced such that it is comparable to the

device capacitance of the differential pair (including increased parasitic capacitance) as shown in Fig. 5(b). Furthermore, let us assume that the two tank inductors are coupled together with coefficient $k = 0.3$. Under this condition, when we sweep L_{TAIL} , we see the FOM never approaches the optimum, even for very large values of L_{TAIL} . The reason for the discrepancy in performance between the two VCO designs is that *the common-resonance technique mandates that the common mode of the entire circuit resonates*. In other words, we need to pay attention to the common-mode return path, which includes the main tank.

To gain some insight, consider Hegazi *et al.*'s design shown in Fig. 6(a) with the gate-source capacitance of the devices and the coupling coefficient of the main tank inductor explicitly drawn. As an exercise in circuit analysis, we can short power and ground (assuming large bypass capacitors), and we can move the reference potential to the source of the differential pair. The impedance loading the transistors is therefore the impedance, Z_{TANK} , shown in Fig. 6(b). It is this impedance that determines both the oscillation frequency and the common-mode resonant frequency [Fig. 6(c) and (d)]. From this ac perspective, a number of things become apparent. First, the common-mode resonant frequency can have a strong dependence on the components used in the main tank and, in certain cases, they can prevent or degrade common-mode resonance. Second, the common-mode impedance can be made to resonate at twice the resonate frequency of the differential

³The original design retained the current source, but its noise at $2f_{LO}$ was filtered by a shunt capacitor. Under this setup, provided AM-to-PM effects in the tank are small, the headroom of the device can be made arbitrarily small without degrading phase noise and its resultant FOM can, therefore, still get within 3 dB of FOM_{MAX} .

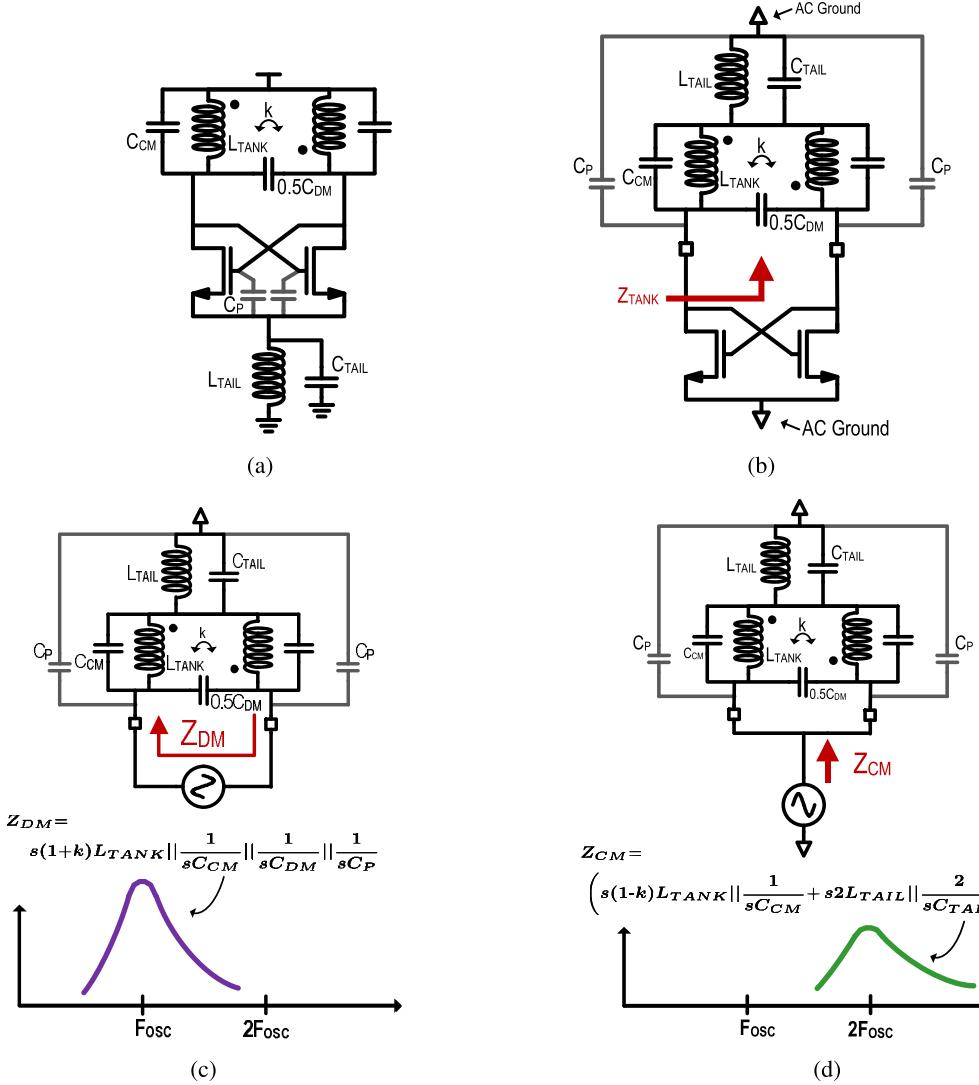


Fig. 6. Understanding the differential mode and common mode of Hegazi *et al.*'s VCO. (a) Topology. (b) AC-equivalent circuit. (c) Differential-mode tank impedance. (d) Common-mode tank impedance.

mode, even if the value of the tail inductor is zero. This latter point leads to the development of the implicit common-mode resonance topology documented in this paper.

B. Implicit Common-Mode Resonance

To resonate the common mode without an extra tail inductor, we null the L_{TAIL} terms shown in Fig. 6. This leads to the effective differential and common-mode impedances shown in Fig. 7. Now, we can tune the common-mode resonant frequency to twice the differential by appropriately choosing k , C_{CM} , and C_{DM} . It is straightforward to show that the common-mode resonates at twice the differential-mode resonate frequency when

$$\frac{C_{DM}}{C_{CM}} = \frac{3 - 5k}{1 + k} \quad (6)$$

where k is defined as per the dot convention shown in Fig. 7. To verify this topology, we conducted the idealized simulation shown in Fig. 8. The variable X sets the ratio of differential to single-ended capacitors. X was swept from 0 to 1, which moved all the capacitors from single-ended to differential,

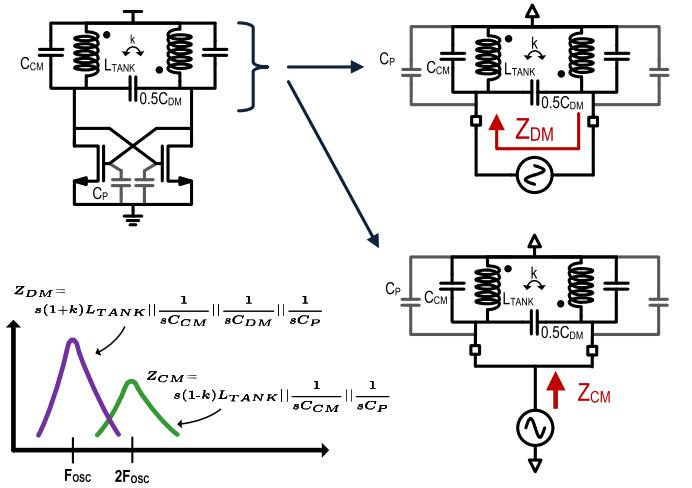


Fig. 7. Differential and common-mode impedances of the proposed topology.

and the resultant spot FOM , efficiency, and noise factor were plotted. We can see that the FOM reaches a maximum at $X = 0.65$, which corresponds to the common-mode reso-

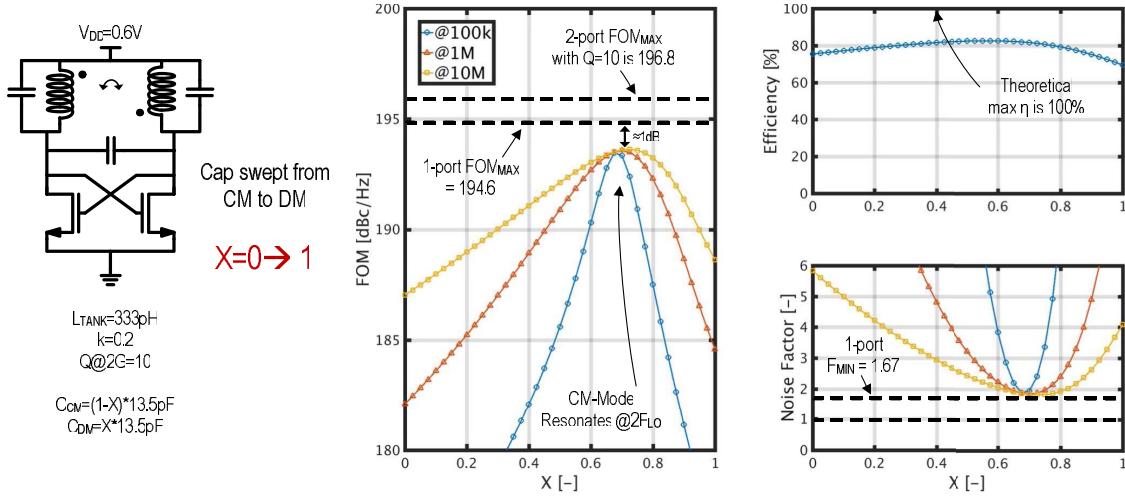


Fig. 8. Idealized simulation of the proposed topology.

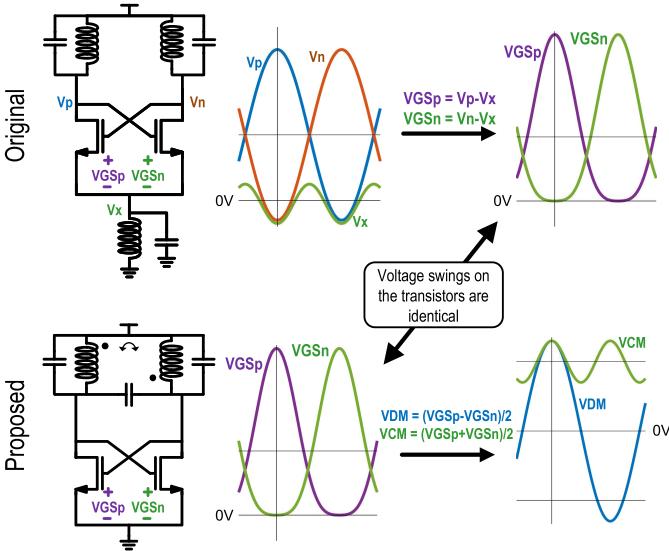


Fig. 9. Comparison of the time-domain waveforms of the original and the proposed common-mode resonant topologies.

nance point at $2f_{\text{LO}}$ for $k = 0.2$. As described by (3), the optimum FOM , assuming an inductor Q , of 10 is 196.8 and, so, the proposed oscillator (like Hegazi *et al.*'s design) gets within 3 dB of this theoretical limit. At the optimum point, efficiency reaches 80% while the noise factor hits $1 + \gamma$. Also, flicker noise is completely nulled at the optimum, as can be seen by the fact that the FOM at 100 kHz, 1 MHz, and 10 MHz all converge to the same value.

C. Comparison to Hegazi *et al.*'s Design and Other Notable Topologies

It is instructive to compare the time-domain waveforms of the proposed design with that of Hegazi *et al.*'s VCO (Fig. 9). Although the outputs of both VCOs are quite different, the gate-source voltages experienced by the transistors in each design are identical, because the $2f_{\text{LO}}$ tail oscillation in Hegazi *et al.*'s design appears as a common-mode oscillation in the proposed design. Put another way: from the transistor's perspective, there is no fundamental difference

between Hegazi *et al.*'s VCO and the proposed design and, therefore, we should not expect any difference in phase-noise performance. As they are theoretical equivalent, any theoretical analysis of Hegazi *et al.*'s design (such as [10] and [16]) is also applicable to the implicit common-mode design.

Although developed independently (and published simultaneously), the flicker noise reduction technique applied to the class-D topology presented in [6] and [7] is essentially the same as the proposed NMOS topology in this paper. Shahmohammadi *et al.* [6], [7] do not explicitly note the equivalence of the topology to Hegazi *et al.*'s work and instead arrived at their design by exploring technique to minimize flicker noise. Another relevant work is the class-F₂ topology [4], [5], which employs a resonator with multiple transformers and, which, among other interesting design features, appears to be the first example of common-mode resonance without an explicit tail network.

D. Fully Complementary Design

Fully complementary designs are often favored over NMOS designs in applications where the phase-noise specification is not challenging, but low-power consumption is important. This is because, for a given inductance, while an NMOS design is capable of lower phase-noise, the CMOS design reaches the same FOM with half the amplitude (and a quarter of the current). A secondary advantage of a CMOS design is that the output swing does not significantly exceed V_{DD} , which enables the use of thin-oxide minimum-length devices. Thin-oxide devices result in higher switched capacitor Q s and less capacitance for a given negative resistance. By contrast, an NMOS-only design generally requires thick-oxide devices in order to satisfy reliability guidelines.

For low-power applications, it is possible to extend the idea of implicit common-mode resonance to a fully complementary design. As shown in Fig. 10, we begin by designing separate NMOS and PMOS VCOs with identical tanks that have common modes that resonate at twice the differential-mode resonant frequency. Both VCOs should be biased across $V_{\text{DD}}/2$. Now, if both oscillators were fabricated on the same silicon,

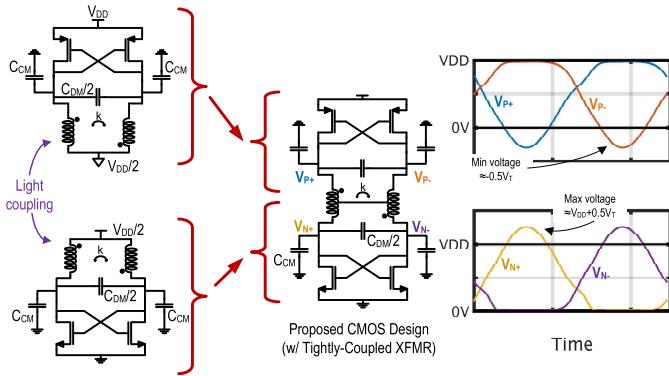


Fig. 10. Fully complementary topology with implicit common-mode resonance.

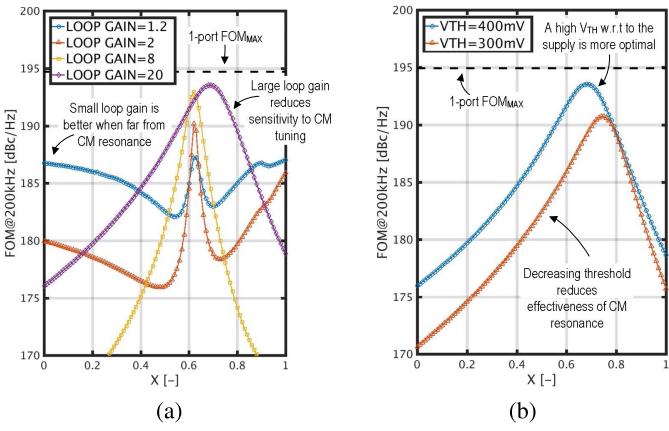


Fig. 11. Effect of differential pair on proposed oscillator. (a) Simulated effect of start-up loop gain on common-mode resonance effectiveness (W/L varied). (b) Simulated effect of threshold voltage on common-mode resonance effectiveness.

some light coupling between the two designs would cause frequency locking, and the phase-noise (of each individual VCO) would drop by 3 dB. A better approach is to short the center tap of both inductors and merge the two inductors into a tightly coupled transformer (also shown in Fig. 10), thereby reducing the current and area of the design. It can be shown that this topology also gets within 3 dB of FOM_{MAX} .

IV. NOTES ON START-UP LOOP GAIN

Assuming common-mode resonance is employed and enough loop gain exists to enable start-up and rail-to-rail swing, the FOM of the proposed oscillator should be independent of the size of the differential pair. That is, the oscillator's noise factor, $1 + \gamma$, does not include the device parameters of width and length. However, this first-order assessment assumes infinite common-mode rejection, which is never the case. In both Hegazi *et al.*'s design and the proposed design, the common mode will have a finite real impedance, and thus, the size of the differential pair can be important.

Fig. 11(a) repeats the simulation of Fig. 8, but with four different sizes of differential pair resulting in different start-up loop gains. For fair comparison, the fixed capacitance was changed to compensate for the varying device capacitance and to ensure all versions oscillated at 2 GHz. Two interesting

things can be noted. First, when the start-up loop gain is large, the sensitivity to common-mode tuning is reduced. Second, and this is important, if common-mode tuning is not employed the FOM collapses in the presence of large start-up loop gain, and a low loop-gain option is preferable (e.g., at $X = 0$, far away from the common-mode resonance point).

These observations suggest the following. In the absence of common-mode resonance, a large differential pair can severely degrade noise performance; however, the differential pair can be oversized if the common-mode impedance is guaranteed to be large or, more precisely, larger than the output resistance of the transistors when operating in deep triode.⁴ We offer a partial and a simplified analysis of this observation. Referring to Fig. 12, if the output resistance of the device in triode is small with respect the common mode of the main tank, its noise will be shunted to ground rather than flowing into the tank. The larger the device the more efficiently its noise (while in triode) will be shunted to ground.⁵

The threshold voltage of the devices relative to the supply is also important. Fig. 11(b) again repeats the simulation of Fig. 8, but with transistors whose threshold voltages have been artificially reduced to 300 mV from 400 mV by editing the model card. In each case, the transistors have been resized to provide the same amount of start-up loop gain (≈ 20) and the capacitance is altered to give the same oscillation frequency (≈ 2 GHz). The plot shows that reducing the threshold voltage has a negative effect on FOM . This can be explained as follows. As the difference between the supply voltage and the threshold of the transistors increases, the transistors spend a greater portion of the oscillation in the triode region and, therefore, given that common-resonance does *not* provide infinite common-mode rejection, the effect of tank loading becomes increasingly apparent. Fortunately, as technology scales, the delta between supply voltages and threshold voltages continues to drop. In addition, modern processes typically provide transistors with many different threshold options.⁶

To summarize: we have observed that an optimal situation in the proposed design, and indeed Hegazi *et al.*'s VCO, is when the thresholds of the differential pair devices are closer to V_{DD} (or the sum of NMOS and PMOS thresholds in case of a CMOS design), and the differential pair is oversized. If any of

⁴This analysis does *not* contradict the ideas behind the class-D VCO [17], [18]. In the single-tank version of that topology, good phase-noise performance was achieved by over sizing the differential pair, but without explicitly using common-mode resonance. However, the use of a single-turn inductor (with a large negative coupling coefficient) and a floating capacitance ensures that the common mode is still relatively large compared with the output resistance of the transistors when operating in deep triode. Therefore, some common-mode rejection is still achieved. Furthermore, that work even points out the existence of an optimal arrangement of single-ended to differential tank capacitance in which phase-noise is minimized in a class-D oscillator. We believe that this point (observed in simulation, but seemingly not measured) can be explained using common-mode resonance theory.

⁵Flicker noise suppression is more complicated. A good treatment of this topic is given in [7], while the presentation accompanying [2] also outlines the key mechanisms of suppression.

⁶One can view a class-C VCO as one in which the threshold is artificially increased such that the transistors spend less time in triode. Interestingly, as Fig. 8 suggests, class-C like operation and common-mode resonance are *not* mutually exclusive techniques and combining them may be beneficial in technologies with high supplies and low-threshold devices.

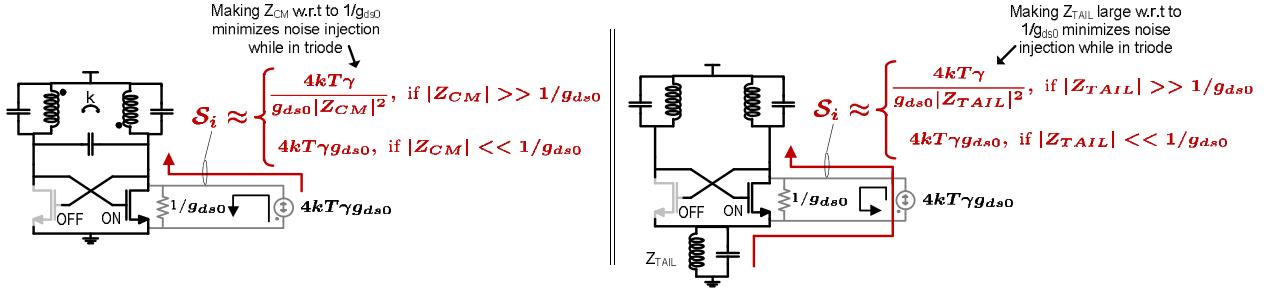


Fig. 12. Just like $|Z_{TAIL}|$ degenerates the noise of the devices in Hegazi *et al.*'s topology, $|Z_{CM}|$ effectively degenerates the devices in the proposed topology. If the common-impedance of the tank is large ($|Z_{CM}| \gg 1/g_{ds0}$), the differential pair should be maximized. If common-mode impedance is small ($|Z_{CM}| \ll 1/g_{ds0}$), the differential pair should be kept small.

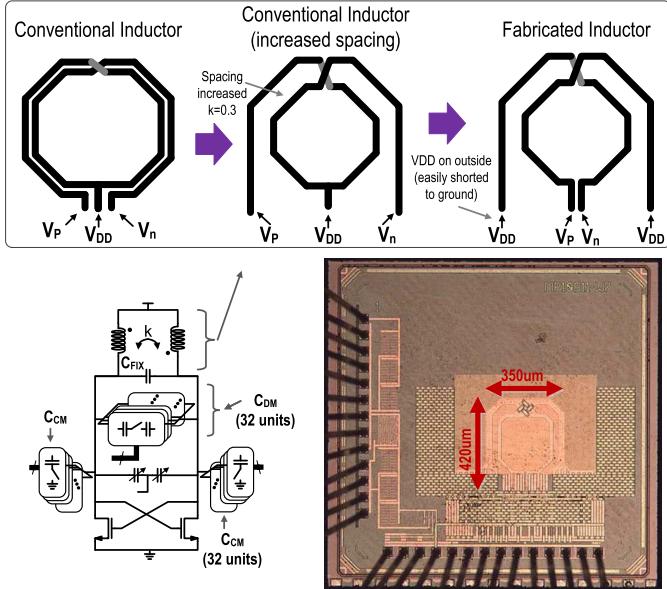


Fig. 13. Schematic and die micrograph of the fabricated NMOS design.

these three criteria are not achieved, common-mode resonance will be less effective.

V. MEASUREMENT RESULTS

To verify implicit common-mode resonance, an NMOS-only prototype [2] and CMOS prototype [3] were fabricated.

A. NMOS Prototype

Fig. 13 shows the schematic of the fabricated NMOS-only design. The chip was fabricated in 28 nm, but only thick-oxide (150 nm) devices were used in the oscillator core. As defined in (6), the arrangement of single-ended capacitance to differential capacitance is a function of the coupling coefficient, k , of the inductor. The common mode cannot resonate at $2f_{LO}$ unless k is less than 0.6. If k is very small or negative, then the value of C_{CM} , which includes parasitics, becomes impractically small. A larger value of k tends to reduce the area occupied by the inductor, but it comes at the cost of reduced common-mode impedance since

$$L_{CM} = L_{DM} \frac{1-k}{1+k}. \quad (7)$$

In the prototype, a value of $k = 0.3$ was chosen to maintain a large common-mode impedance and a relatively small area

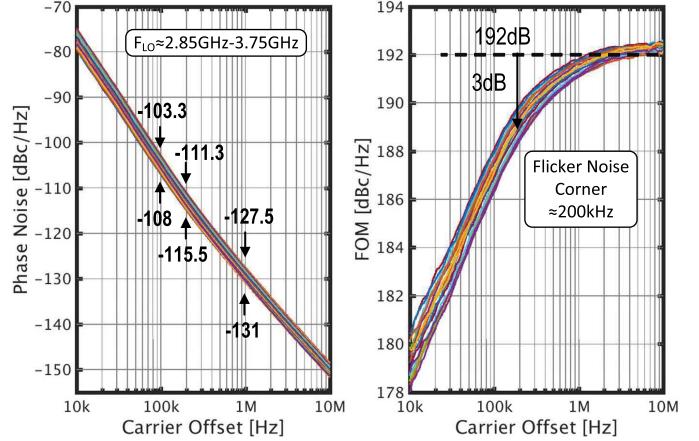


Fig. 14. Measured phase-noise and FOM of the NMOS VCO (composite plot of 22 points across frequency band).

overhead. As shown in Fig. 13, the 750 pH inductor is a two-turn inductor where the spacing between the turns was increased to attain the required k value (increasing the space between the windings does not affect Q , but it does affect area). Furthermore, the terminals were organized so that the V_{DD} terminals could be more easily shorted to the surrounding ground plane, thereby ensuring a good common mode Q .⁷

With a k equal to 0.3, the ratio of common mode to differential capacitance is one-to-one. Thirty-two differential and 32 common-mode unit cells are employed, which are switched in one at a time. It is important to note that when a differential unit capacitor bank is turned OFF, a large portion of its OFF capacitance appears as parasitic capacitance to ground (that is, common-mode capacitance). Therefore, a fixed differential capacitance is included in the design to ensure that the 1:1 ratio is maintained, even when all unit caps are OFF.⁸

The measured VCO was tunable from 2.85 to 3.75 GHz. Fig. 14 shows the phase-noise measured at 22 different points across the band. Plotting the resultant FOM , we note an

⁷This does have the potential to severely degrade the differential Q if good decoupling and low-loss routing between the separated V_{DD} ports does not exist (i.e., if the surrounding supply/ground plane is less than ideal). In retrospect, the conventional inductor with increased space between the windings, shown in Fig. 13, is likely a better option.

⁸This does limit the tuning range of the VCO. In addition, the presence of a single-ended capacitor bank (instead of only a differential capacitor bank) can lower the tank Q at higher oscillation frequencies. Hegazi *et al.*'s VCO does not have such problems due to the additional degree of freedom given by the tail inductor.

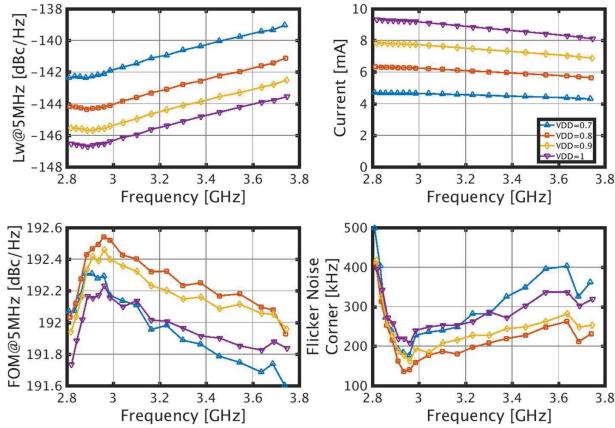
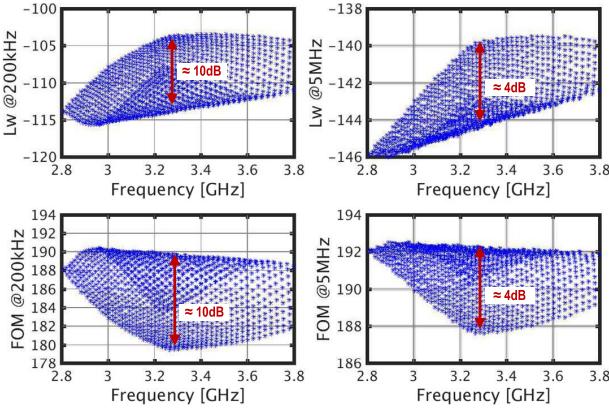


Fig. 15. Measured performance metrics of the NMOS VCO versus frequency.

Fig. 16. Measured phase-noise and *FOM* for all possible capacitor settings of the NMOS VCO.

FOM of 192 in the thermal noise region and a flicker noise corner of around 200 kHz. Fig. 15 shows the measured performance metrics for different supply voltages. When the supply is varied from 0.7 to 1 V, the phase-noise changes due to the changing current, but the *FOM* stays constant. A supply pushing number of between 6 and 30 MHz/V was recorded.

As the fabricated design has 32 common-mode and 32 differential-mode capacitors, there are over a thousand possible capacitor settings. Fig. 16 shows the measured spot *FOM* versus frequency for all possible settings at both 200 kHz and 5 MHz offsets, which includes configurations where the common mode correctly oscillates and many more configurations where the common mode is misaligned. Under normal operation, the differential and single-ended capacitors are switched in one at a time, which ensures correct common-mode resonance and results in the highest *FOM* and lowest phase-noise numbers at any given frequency. If the common-mode resonance is misaligned, we see performance degradations up to 4 dB at 5 MHz and 10 dB at 200 kHz. The increased sensitivity at 200 kHz is because of the presence of flicker noise. This figure, therefore, shows both the efficacy and the importance of accurate common-mode tuning.

B. CMOS Prototype

Fig. 17 shows the schematic of the CMOS prototype that was fabricated in 28 nm. Since the maximum voltage swing

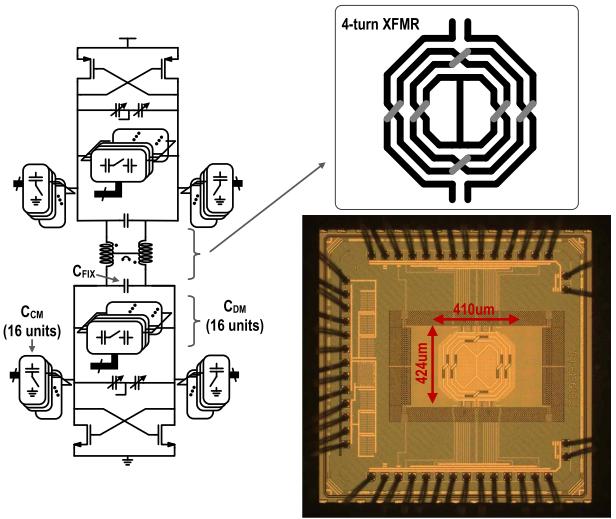


Fig. 17. Schematic and die micrograph of the fabricated CMOS design.

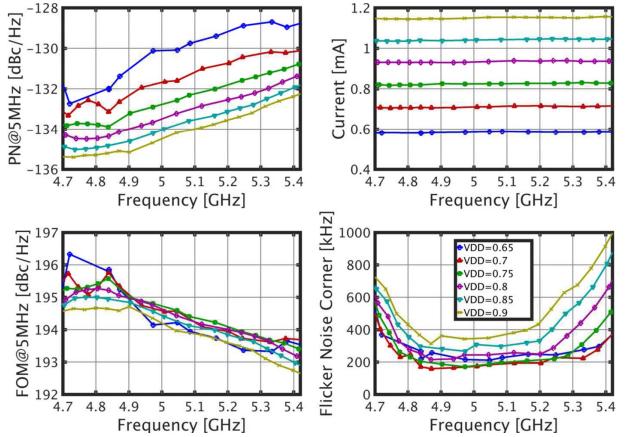


Fig. 18. Measured performance metrics of the CMOS VCO versus frequency.

in the core is around V_{DD} , minimum-length thin-oxide devices were used throughout the design. The transformer used four turns with the spacing between each turn sized to give a k around 0.37. The simulated inductance was approximately 1.7 nH, while the simulated Q was 18.

The measured VCO was tunable from 4.8 to 5.3 GHz. Fig. 18 shows the measured performance metrics for different supply voltages ranging from 0.65 to 0.9 V. For a supply of 0.7 V, the measured *FOM* is between 194 and 196 in the thermal noise region, and the flicker noise corner is measured at around 200 kHz. Again, when the supply is varied, the measured phase-noise changes due to the changing current, but the *FOM* stays reasonably consistent in the thermal noise region. The flicker noise corner does tend to increase with increasing supply, which can be explained by the fact that low-threshold devices were used in the differential pair to enable low voltage supply operation. As discussed in Section IV, when the difference between the supply voltage and the threshold of the transistors increases, the effectiveness of common-mode resonance degrades.

Fig. 19 shows the measured spot *FOM* versus frequency for all possible settings at both 200 kHz and 5 MHz offsets. Again, like the NMOS-only design, under normal operation,

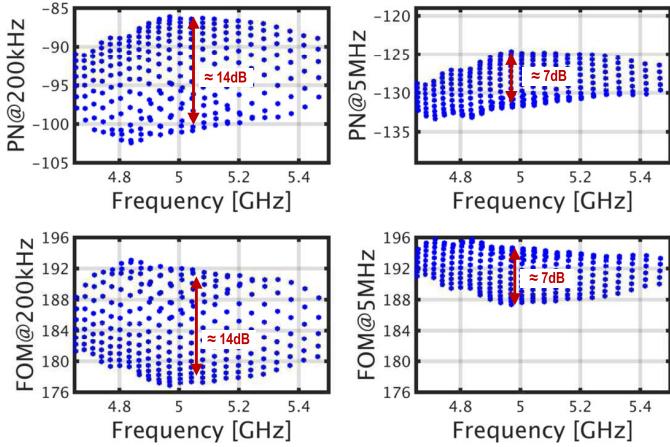


Fig. 19. Measured phase-noise and *FOM* for all possible capacitor settings of the proposed CMOS VCO.

TABLE I
COMPARISON TO OTHER COMMON-MODE RESONANCE TOPOLOGIES

	JSSC 2001 (Hegazi [1])	JSSC 2015 (Garampazzi [6])	This Work	
Topology	NMOS $2F_{LO}$ Tail Tuning	CMOS $2F_{LO}$ Tail Tuning	NMOS $2F_{LO}$ Implicit Resonance	CMOS $2F_{LO}$ Implicit Resonance
Technology	0.35 μ m	55nm	28nm	28nm
Supply Voltage	2.5	1.5	0.9	0.7
Frequency Range [GHz]	1.1-1.2 (18%)	7.4-8.4 (13%)	2.85-3.75 (27.2%)	4.7-5.4 (13.8%)
Phase Noise [dBc/Hz @ 3MHz]	-153.2	-133	-139.7	-126.9
Power [mW]	9.1	6.3	6.6	0.5
FOM [dB] (Thermal Region)	195	194.3-195.6	192-192.5	194-196
FOM [dB] (@100kHz)	185*	185*	186-188	188-191
Core Area [mm ²]	N/A	0.19	0.15	0.18
Passives	2	2	1	1

*Estimated from plots

the differential and single-ended capacitors are switched in one at a time, which ensures correct common-mode resonance and the highest possible *FOM* at a given frequency. If the common-mode resonant frequency is deliberately mistuned, we see performance degradations of 7 dB at 5 MHz and 14 dB at 200 kHz.

C. Table of Comparison

Table I compares both prototypes to NMOS and CMOS topologies employing explicit tail tuning, that is, Hegazi *et al.*'s [1] 2001 design and Garampazzi *et al.*'s [10] 2015 CMOS equivalent. Despite using one less passive component and, therefore, having one less degree of freedom, the measured *FOM* in the thermal noise region of the proposed NMOS design is within 3 dB of these gold standard designs, while the CMOS design achieves a similar *FOM* of around 195. If *FOM* is measured at 100 kHz, the prototypes

demonstrate superior performance, which suggests a lower flicker noise corner.

VI. PRACTICAL DESIGN NOTES

A. Limitations of Implicit Common-Mode Resonance

Unlike Hegazi *et al.*'s original design, implicit common-mode resonance requires the designer to control both the coupling coefficient of the inductor and the ratio of differential to single-ended capacitance. In certain cases, this requirement may compromise the differential quality factor of the tank. The amount of this degradation is completely dependent on the VCO specifications (i.e., tuning range and oscillator frequency), the passive size (i.e., number of inductor turns), and the technology used (i.e., programmable capacitor-*Q*s). Given that such specifications vary widely and the resultant design space is large, it is hard to provide a rigorous analysis of the relative performance of the two topologies. However, we can say that implicit common-mode topology is likely to lead to degraded performance (compared with Hegazi *et al.*'s design) in the following situations.

- 1) At frequencies and tuning ranges where the quality factor of programmable capacitors begin to dominate the resonator tank-*Q*. In such cases, the need for some fixed capacitance and/or the use of some single-ended programmable capacitors as opposed to only differential programmable capacitors (which have two times larger *Q*) will noticeably increase tank losses.
- 2) In high-power VCOs, where a single-turn inductor is required in order to get enough power into the oscillator. A small single-turn inductor typically exhibits a large negative *k*-factor that makes it difficult to resonate the common mode due to the requirement for minimum common-mode capacitance [see (6)].

Nevertheless, as demonstrated by the fabricated prototypes in this paper and the independent work documented in [6] and [7], implicit common-mode resonance is suitable for many common scenarios where *Q*-degradation due to capacitive elements is negligible, and where inductors of two or more turns are employed.

B. Area Savings

The potential for area savings is also highly dependant on a given design. If the "first-cut" primary inductor has a moderate *k*-factor of between 0.2 and 0.6, there is likely no need to adjust the space between the windings and, so, the area saving will equal the area occupied by the tail resonate tank (including any associated routing and programmable capacitor banks). If the spacing needs to be adjusted, more modest savings will be seen. This paper did not focus on optimizing the inductor area, but rather sought to demonstrate that common-mode resonance is possible without a tail network.

C. Tank Symmetry

For the best results, it is important to ensure that the *LC* tank of the implicit common-mode topology is balanced. Any deviation from symmetry will cause an increase in noise, especially close-in flicker noise. For this reason, it is important

to minimize systematic mismatch by maintaining symmetry in the design, the layout, and the immediate environment of the VCO. In the fabricated chips, we could individually control the “left-side” and “right-side” single-ended programmable capacitors banks. Therefore, we could deliberately induce systematic mismatch by turning on more right-hand-side capacitors than left-hand-side capacitors. When this was done common-mode resonance was still observed, but the flicker noise corner was higher. The optimum was always when the left-side and right-side capacitors settings were equal.

D. Amplitude Control

The differential amplitude of the proposed design is set by the supply at roughly $2V_{DD}$. If amplitude control is required, a current source can be included with a shunt capacitor to strip off its $2f_{LO}$ noise component, just like in Hegazi *et al.*’s [1] design. Provided the tank is perfectly linear and balanced, the low frequency noise competent of the current source will be up-converted as amplitude noise, not phase noise. (In practice, AM-to-PM conversion in the tank and other second-order effects can cause some of this noise to degrade the phase noise profile.) An alternative approach is to control the VCO supply through a dedicated low-noise LDO.

VII. CONCLUSION

Employing a tail inductor to resonate the common mode of an *LC* oscillator is a widely used technique that achieves state of the art performance. This paper shows that the same performance can be achieved without the need of a second passive component, provided the common mode of the primary tank resonates at twice the frequency of its differential mode. Fabricated NMOS-only and CMOS versions of the proposed topology achieved performance metrics comparable to the original tail-tuning designs.

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