A Precision Capacitance-to-Digital Converter With 16.7-bit ENOB and 7.5-ppm/°C Thermal Drift

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***Abstract*— This paper presents a high-precision capacitance-to-digital converter (CDC) for displacement measurement in advanced industrial applications, based on a charge-balancing third-order delta–sigma modulator. To achieve high precision, this CDC employs a precision external resistive reference and a quartz-oscillator-based time reference instead of a reference capacitor. To minimize the error contribution of the CDC circuitry, various precision circuit techniques, such as chopping and auto-zeroing, are applied at both system and circuit level. Measurement results of the prototype realized in 0.35-μm CMOS technology show that the CDC achieves an rms resolution of 42 aF across a capacitance range from 6 to 22 pF, corresponding to an effective number of bits (ENOB) of 16.7 bit. The conversion time for one measurement is 10.5 ms, during which the CDC consumes 230 μA from a 3.3-V single supply. The measured thermal stability is within ±7.5 ppm/°C across a temperature range from 20 °C to 70 °C, which represents a significant improvement compared to the state of the art. After a two-point calibration, all ten measured samples from one batch show absolute accuracy below ±25 fF across the entire capacitance measurement range.**

***Index Terms*— Capacitance-to-digital converter (CDC), capacitive sensor interface, delta–sigma modulator, displacement measurement, high precision, industrial applications.**

I. Introduction

IN HIGH-PRECISION mechatronic systems, such as lithography machines (Fig. 1), the position of critical elements has to be determined with sub-nanometer precision, while periodic recalibration is not feasible due to the harsh and/or inaccessible environment. In addition, the volume and the power budget for a position measurement system are limited in order to reduce the machine complexity and to prevent the generation of heat. In such applications, capacitive displacement sensors are attractive, since they are small and consume limited static power [1]. Due to the noisy industrial environment, the sensor interface electronics have to be integrated with the sensor head to provide a robust digital output.

To digitize the capacitance C_x of a precision displacement sensor, a precision reference is required, which can either be a physical reference capacitor C_{ref}, or a reference capacitance constructed using a combination of other references, such as resistors, inductors, time references, current references, and voltage references. The combination of these references then generates an equivalent reference capacitance.

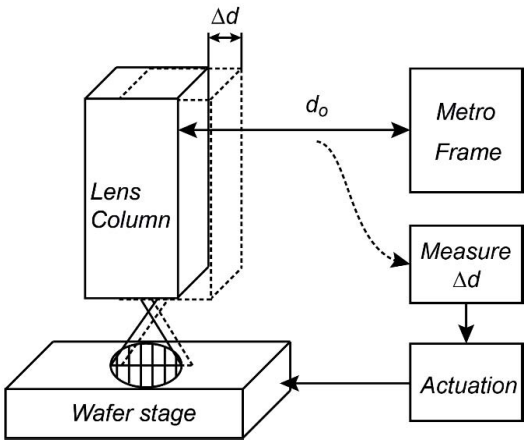

Fig. 1. Lithography machine in which the wafer stage is dynamically aligned with the lens columns by measuring its small displacement/vibration.

Most recently reported capacitance-to-digital converters (CDCs) employ a physical reference capacitor. Their operating principles include period modulation [2], [3], delta–sigma modulation [4]–[6], successive approximation [7], dual-slope conversion [8], and iterative delay-chain discharging [9]. When references other than capacitance are used, the CDCs are mainly oscillator-based circuits in which the sensor capacitance together with non-capacitive reference component (resistor, inductor) defines the oscillation frequency that is digitized by a time-to-digital converter [10]–[12].

While many of the CDCs with a capacitive reference demonstrate good resolution, measurement speed, and energy efficiency, their precision is ultimately limited by the quality of the capacitive references used. A survey of commercially available reference components [13] shows that most capacitive references, whether integrated or discrete, show thermal drifts above 30 ppm/°C, while their absolute inaccuracy without calibration can be more than 1%. Only dedicated capacitance standards achieve a temperature coefficient below 10 ppm/°C and small tolerances [14], but their cost and size are unattractive for sensor applications.

Oscillator-based CDCs ideally can employ more stable and accurate references, such as a resistive reference and a frequency reference. Both resistive references and frequency references are commercially available with sufficient accuracy and stability over temperature and time. In this work, the combination of a metal foil resistor [15] with a temperature coefficient of 2 ppm/°C ±2.5 ppm/°C across a wide temperature range and a quartz crystal oscillator with 0.2-ppm/°C

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thermal drift [16] is selected to generate an effective reference capacitance with better than 5-ppm/°C stability and high accuracy. This concept was proposed and evaluated by Yang and Nihtianov [13], [17], and Yang *et al.* [18]. This paper provides a comprehensive description of the design, details on the techniques used to mitigate the various error sources, and new results of the experimental evaluation of the prototype's resolution, transfer function, thermal stability, and long-term drift.

Furthermore, to achieve a performance level of the CDC defined mainly by the implemented references, care needs to be taken to reduce the effect of the interface electronics imperfections on the total error. This paper addresses this challenge by presenting an integrated precision CDC based on a charge-balancing incremental $\Delta\Sigma$ modulator that employs an active integrator as well as various precision circuit techniques to reduce the sensitivity to parasitic components.

This paper is organized as follows. Section II presents the operating principle of the proposed precision CDC. Section III analyzes its noise. Section IV details the circuit implementation, focusing on the precision circuit techniques applied. Experimental results of a prototype chip, which demonstrate superior precision while maintaining reasonable energy efficiency compared to the state of the art, are shown in Section V.

II. Operating Principle

For our target application, a CDC architecture needs to be selected that can be designed to introduce negligible errors, so that the precision is limited by the references, and that can provide a resolution in line with the precision. With the target capacitive sensor (10-μm nominal distance between the two sensor plates, each with a diameter of 20 mm), we aim for a measurement range of more than ± 5 μm around the nominal distance with sub-nanometer resolution. This translates to a capacitance range of above 15 pF and an attofarad range resolution, which corresponds to a effective number of bits (ENOB) of above 15 bits. Additionally, we aim for the CDC to be able to handle up to 10 pF of parasitic capacitance without sacrificing the performance, allowing it to interface with an off-chip sensor capacitance with associated parasitic capacitance. CDCs achieving this level of resolution have been reported that are based on delta–sigma modulators [5], [6], and on relaxation oscillators [2], [19]. The ratio-metric nature of these CDCs, typically implemented by means of charge balancing using an active integrator, in combination with the use of offset cancellation or auto-calibration techniques, gives these CDCs the potential to achieve high precision.

A block diagram of the charge-balancing incremental $\Delta\Sigma$ modulator proposed in this paper is shown in Fig. 2 along with typical waveforms. The reference resistance R_{ref} is converted into current $V_{\text{ref}}/R_{\text{ref}}$ by a resistance-to-current converter (RIC) using a reference voltage V_{ref}. After an initial reset, this current is continuously integrated by an active integrator. The sensor capacitor C_x is incorporated in a switched-capacitor circuit, which causes a charge $-C_x V_{\text{ref}}$ to be integrated if the modulator's bitstream output (bs) is one, in order to balance the charge contributed by the reference current. This charge-balancing operation is synchronized to the crystal clock. Every clock cycle, a clocked comparator detects the polarity of integrator's output and thus generates a bit of the output bitstream bs that determines whether $-C_x V_{\text{ref}}$ will be integrated in the next clock cycle. Due to this negative feedback, if the loop is operated for large number of clock cycles N, the accumulated charge in the integrator is approximately zero, meaning that on average, the reference current is balanced by the charge supplied by C_x

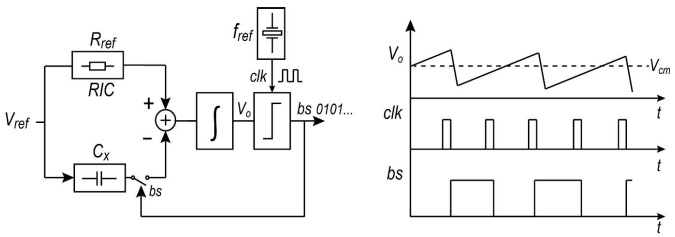

Fig. 2. Block diagram of the proposed precision CDC, based on a charge-balancing delta–sigma modulator with resistor/time reference, with typical waveforms at critical nodes.

$$N\frac{V_{\text{ref}}}{R_{\text{ref}}}t_{\text{ref}} = N_1 V_{\text{ref}} C_x \tag{1}$$

where t_{ref} is the duration of one period of the quartz crystal oscillator and N_1 is the number of clock cycles during which bs was one. The average value of the bitstream, determined using a decimation filter, can be written as

$$\mu = \frac{N_1}{N} = \frac{t_{\text{ref}}}{C_x R_{\text{ref}}}. \tag{2}$$

In this expression μ is inversely proportional to C_x, which is a result of the fact that C_x is placed in the feedback path of the $\Delta\Sigma$ modulator. However, this makes μ proportional to the measured displacement d (when $d \sim 1/C$ is the distance between the two parallel plates of the measured capacitor). Another advantage of this solution is the continuously running reference current, preventing clock jitter and the switching transients from limiting the resolution and precision. From this average, C_x can be easily calculated in the digital domain

$$C_x = \frac{t_{\text{ref}}}{\mu R_{\text{ref}}}. \tag{3}$$

This expression is independent of the exact value and the drift of V_{ref}, provided that V_{ref} drifts much slower than the conversion time. Ideally, if errors associated with the charge balancing are minimized, the precision of the measurement is purely determined by the resistive and time references used. In our design, we use a reference resistance of 400 kΩ and a reference measurement time period of 10 ms to enable capacitance measurement in the targeted range up to 22 pF. This measurement time corresponds to 2000 clock cycles of a 200-kHz reference clock.

III. Noise Analysis

The resolution of the CDC is limited by a combination of quantization noise and thermal noise, both of which decrease when the number of clock cycles per conversion N is increased. In an energy-efficient design, energy should primarily be spent on getting the thermal noise at the desired level, while the quantization noise level, which can

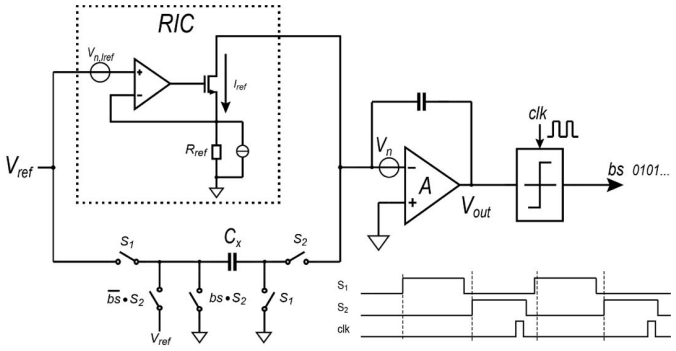

Fig. 3. Simplified circuit diagram of the front-end stage, including the main noise sources.

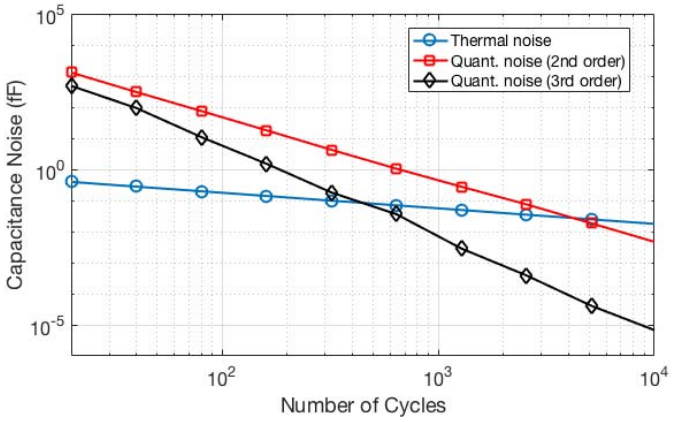

Fig. 4. Noise in the measured capacitance as a function of the number of operating cycles N, both due to thermal noise and due to the quantization noise of a second-order and a third-order modulators.

typically be reduced at a more modest cost in terms of energy consumption, should be designed to be below the thermal noise level [20], [21].

The main thermal-noise contributors are the RIC, the amplifier of the active integrator, and the switches associated with C_x, which contribute kTC noise (Fig. 3). Noise introduced by sources after the integrator is attenuated by the gain of the integrator when referred to the input, and is therefore negligible.

As shown in Fig. 3, an active RIC built around an operation transconductance amplifier (OTA) is used to generate the reference current $V_{\rm ref}/R_{\rm ref}$, rather than directly connecting $R_{\rm ref}$ to the virtual ground of the integrator, so as to prevent transients at the virtual ground of the integrator from affecting the reference current. This circuit is associated with two main noise sources: the thermal noise of the reference resistor $R_{\rm ref}$ and the equivalent input voltage noise $v_{n,\rm iref}$ of the OTA, which is approximately 16 kT/3g_m, assuming it is dominated by the OTA's input differential pair with transconductance g_m [22]. The resulting current noise density is

$$I_{n,eq}^2 = \frac{4kT}{R_{\rm ref}} + \frac{16kT}{3g_m R_{\rm ref}^2}. \tag{4}$$

The integration of this noise during a time period $t_{\rm ref}$ is equivalent to a sinc filter in the frequency domain with transfer function

$$H\,(f, t_{\rm ref}) = t_{\rm ref}\mathrm{sinc}\,(f t_{\rm ref}) = t_{\rm ref}\frac{\sin(\pi f t_{\rm ref})}{\pi f t_{\rm ref}}. \tag{5}$$

Therefore, the mean-squared noise charge due to the current noise can be calculated as

$$\overline{Q_{n1,\rm Iref}^2} = t_{\rm ref}^2 \int_0^\infty I_{n,eq}^2 \cdot H^2(f, t_{\rm ref}) df = \left(\frac{4kT}{R_{\rm ref}} + \frac{16kT}{3g_m R_{\rm ref}^2}\right) \times \frac{t_{\rm ref}}{2}. \tag{6}$$

The noise charge associated with the switched-capacitor operation can be estimated as [19]

$$\overline{Q_{n2,Cx}^2} = kTC_x\left(1 + \frac{x}{1+x} + \frac{4/3}{1+x}\right) \tag{7}$$

where $x = 2R_{\rm ON}g_m$ defines the relative noise contribution of the OTA compared to the ON-resistance $R_{\rm ON}$ (2 kΩ) of switches. The first term in (7) (kTC_x) represents the noise charge sampled when switches S_1 open. The second and third term represent the noise charge associated with the sampling of the noise of the switches and OTA, respectively, when switches S_2 open.

Assuming that these noise sources are uncorrelated, the mean-squared noise charge averaged over the N operating cycles of the modulator equals

$$\overline{Q_{n,\rm final}^2} = \frac{Q_{n1,\rm Iref}^2 + Q_{n2,Cx}^2}{N}. \tag{8}$$

The equivalent rms noise σ_{Cx} in the measured capacitance can then be found by comparing this to the signal charge $V_{\rm ref}C_x$

$$\sigma_{Cx} = \sqrt{\frac{Q_{n1,\rm Iref}^2 + Q_{n2,Cx}^2}{N \cdot V_{\rm ref}^2}}. \tag{9}$$

This is plotted as a function of N in Fig. 4, where $V_{\rm ref}$ is 1.65 V, C_x is 10 pF, $R_{\rm ref}$ is 400 kΩ, and g_m is 400 μS. To achieve a resolution of around 17 bits (42-aF rms with a 16-pF capacitance range), at least 2000 cycles are needed.

It is worth to mention that the impact of clock jitter of the frequency reference is negligible due to the following reasons.

1) The switched-capacitor network around C_x is designed to settle accurately, as a result of which jitter on the clock edges leads to negligible errors in the amount of charge transferred to the integrator.
2) The reference current is not switched, but integrated continuously throughout the entire measurement time (∼10.5 ms), as a result of which the effect of the clock jitter (in the range of picosecond) is readily negligible.

Fig. 4 also shows the quantization noise expressed in terms of an equivalent rms capacitance resolution, based on a behavior simulation of a second-order and a third-order modulator. At the mentioned number of 2000 cycles, the quantization noise of a second-order modulator is larger than the thermal noise, while that of a third-order modulator is well below the thermal noise. Therefore, the latter has been selected for the design. To reduce system complexity, a second-order modulator could be adopted, but this would have to be run

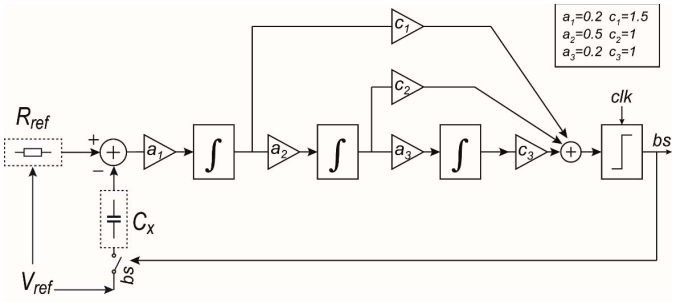

Fig. 5. Block diagram of the precision CDC based on a third-order delta–sigma modulator.

at a larger number of cycles to reach the targeted resolution, at the expense of higher energy consumption.

A block diagram of the modulator is shown in Fig. 5. A feed-forward loop filter is used to reduce the output swing of the integrators and thus improve the linearity of the system [21], [23]. A direct feed-forward path from the input to the quantizer is omitted, as it requires duplicating the sensor capacitor which significantly complicates the circuit without significantly reducing output swing [4], [23]. The values of the loop coefficients (shown in Fig. 5) are defined such that the zeros are all at dc.

With the selected loop coefficients, the CDC loop is stable within an input range from 0.2 to 0.75 of the full scale. To accommodate the desired capacitance range of the application (6 to 22 pF), the reference current is designed to be around 1.25 μA. A circuit level simulation shows that the output swing of the first integrator is within $\pm$450 mV, while the swing at the second and third integrators are within $\pm$300 mV and $\pm$250 m, respectively. Simulation also shows that the gain of the first integrator is above 120 dB within this output swing range, which guarantees the required linearity of the integrator.

IV. Precision Circuit Implementation

A simplified schematic of the proposed CDC is shown in Fig. 6, including the precision RIC, an auto-zeroed first integrator, a second and third integrator (details of which have been omitted for simplicity), and a clocked comparator. A timing diagram of the various signals involved is also shown in Fig. 6. Although the capacitor to be measured (C_x) is single ended, a pseudo-differential topology is used to minimize errors due to charge injection of the switches. To this end, a replica input network (shown in gray) is used, which, in contrast with Cx, is switched between ground and ground, rather than between ground and V_{ref}, to prevent it from contributing charge to the integrator. A replica of the output stage of the RIC balances the parasitic capacitance at the differential inputs without contributing current. A switched-capacitor (SC) network built around a capacitor C_{rep} that is nominally equal to C_x reduces differential charge-injection errors without contributing signal charge.

To reduce systematic errors due to the asymmetry of the circuit, such as offset and charge-injection mismatch, system-level chopping is implemented by reversing the polarity of the input signals (including both the SC network and the reference current) and of the bitstream bs. The system-level choppers are operated at a frequency f_{chop} that is a fraction of the frequency reference f_{ref}, such that two chopper periods fit within one conversion cycle, as shown in Fig. 6 [25]. An auto-zeroing (AZ) network at the input of first integrator reduces errors due to the overdrive voltage at the virtual ground associate with the integrator of I_{ref}. The motivation for applying AZ and details of the various building blocks will be discussed below.

A. Precision Resistance-to-Current Converter

A detailed circuit diagram of the precision RIC is shown in Fig. 7. To allow a reasonable resistance of R_{ref}, a scaled reference voltage V_{ref_I} (0.5 V) is used in the RIC, which is derived from V_{ref} (1.65 V) that is applied to the sensor capacitor. The scaling is done by a resistive divider consisting of two precision resistors. Due to the good matching of these resistors, this resistive divider has negligible impact on the precision of the CDC. The RIC uses feedback to realize a large output impedance, so as to minimize errors due to transients (V_{spike}) at the integrator's virtual ground associated with the switched-capacitor operation. To accurately copy the reference voltage V_{ref_I} to the reference resistor R_{ref}, a two-stage Miller-compensated amplifier (A_1 and A_2) with more than 120-dB dc gain is used. Its first stage A_1 is a standard folded-cascode amplifier with PMOS input pair and is chopped by a nested-chopper pair, operated at 50 and 1 kHz, respectively, to modulate offset and $1/f$ noise away from dc [26], where they are filtered out by the $\Delta\Sigma$ modulator and its decimation filter. The second stage A_2, which consists of an NMOS input pair with current-mirror load, converts the differential signal into a single-ended output to drive output transistor M_1. Its offset and noise are suppressed by the large gain of A_1 and are thus negligible.

Due to the finite output impedance of the RIC, transient signals at the virtual ground of the first integrator will cause voltage transients at the reference resistor. This will lead to variations in I_{ref}, which may be affected by changes in humidity, temperature, etc., due to the sensitivity of the parasitic capacitance C_p associated with the reference resistor to such environmental effects. To prevent this from limiting the CDC's stability, it is required that the RIC has enough loop gain to stabilize the voltage across R_{ref}, and enough output impedance, in the gigaohm range, to suppress the transient signals at the source of M_1 such that the error current has negligible effect on the accuracy. Moreover, to suppress errors due to transients at the virtual ground, a high dc gain is not sufficient. The frequency of these transients is determined by the 200-kHz clock of the modulator. As a consequence, it is required that the current source should have enough output impedance up to 200 kHz and its harmonics. In principle, this can be achieved by increasing the bandwidth of the two-stage amplifier. However, this is difficult due to the parasitic pole associated with the capacitance C_p. To nevertheless provide sufficient output impedance at high frequencies, a cascode transistor M_2 is added, which is regulated by a high-bandwidth amplifier A_3, which consists of a PMOS differential input pair with current-mirror load. Thus, transients at 200 kHz are

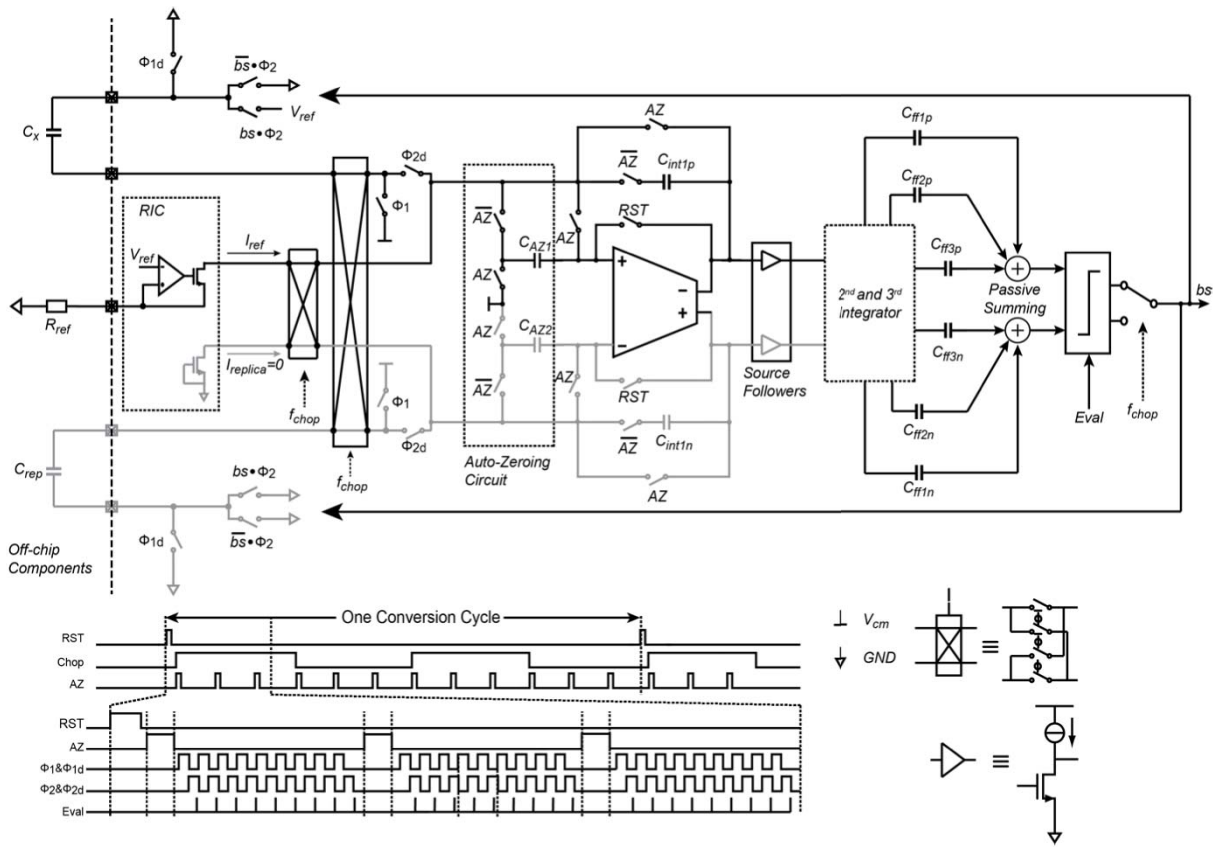

Fig. 6. Simplified circuit diagram of the proposed precision CDC including the associated timing diagram.

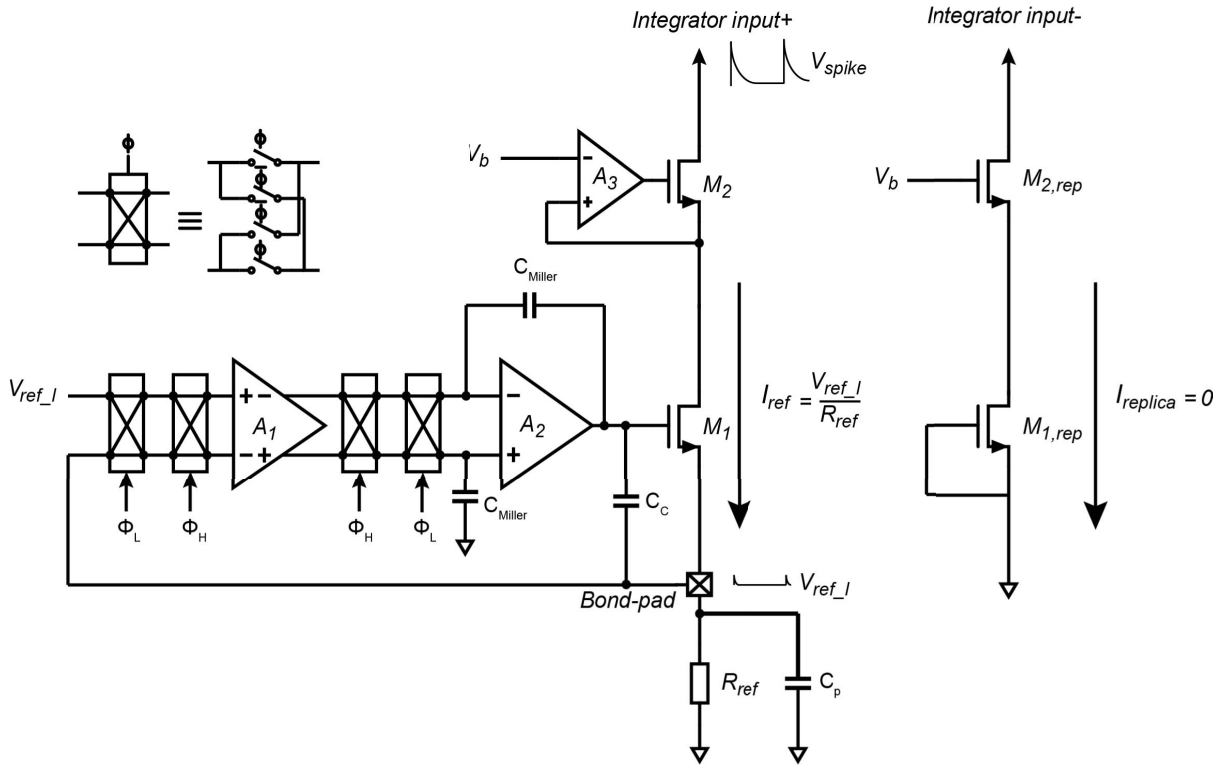

Fig. 7. Circuit diagram of the precision RIC.

suppressed by more than 40 dB. Simulation of the overall CDC shows that this suppression is enough for the required precision.

The RIC consumes 50-μA current from 3.3-V supply. Fig. 7 also shows the replica RIC required for the pseudo-differential implementation shown in Fig. 6. It employs the

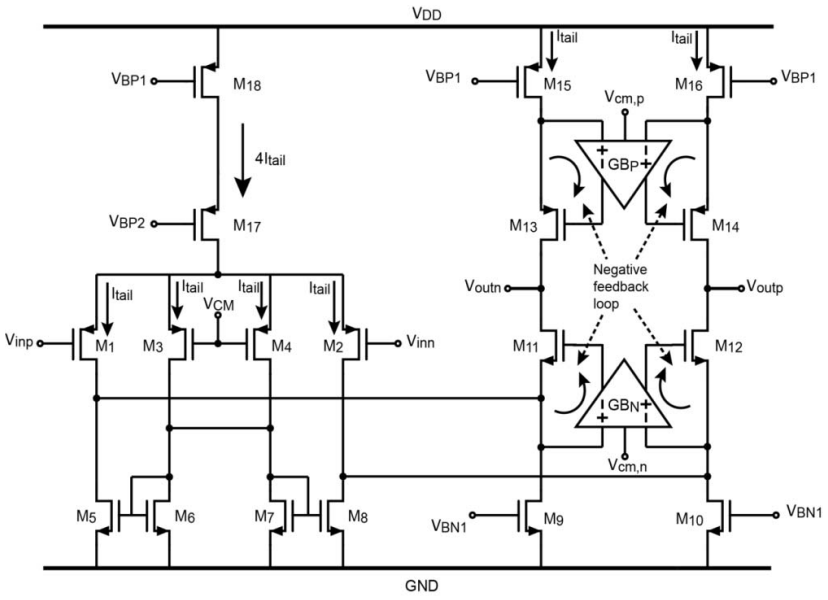

Fig. 8. Circuit diagram of the first integrator OTA with input CMFB and gain boosting.

same output structure as the main RIC. While this replica does not balance the impedance perfectly, since the replica is not biased, it provides matched parasitic capacitances at the inputs of the integrator.

B. First Integrator

The fully differential OTA used in the first integrator is shown in Fig. 8. It employs a folded-cascode topology with a PMOS input pair $M_{1,2}$. To ensure that the leakage of the integrator due to the OTA's finite gain is negligible and to provide enough suppression of the errors of later stages, gain boosting is used to achieve a dc gain of above 140 dB. For this purpose, two booster amplifiers GB_P and GB_N regulate the drain voltage of M_{15} and M_{16} to $V_{cm,p}$ and that of M_9 and M_{10} to $V_{cm,n}$ are added, ensuring a very high output impedance of the main amplifier [27], [28]. The CDC is designed to measure external capacitance; hence, it needs to handle a relatively large parasitic capacitance of up to 10 pF, due to the connection to off-chip components, including the wires and the parasitic capacitance of the external capacitor. To ensure sufficient settling accuracy [settling errors less than (1/2) LSB], the OTA is designed with a bandwidth above 7 MHz at 12-pF capacitive load at all corners, leading to a current consumption of 108 μA from the 3.3-V supply.

The use of the replica SC network, although it balances out errors due the charge injection of the switches, may introduce errors if the voltage across it is not held constant. The high gain and AZ of the first integrator's OTA (as will be discussed in the following) ensures that the overdrive voltage at its input will not lead to significant voltage variation across the replica network. Variation in the input common-mode voltage, however, also leads to errors, in particular to non-linearity, due to the pseudo-differential input configuration, in which C_x will vary for different displacement, while C_{rep} on the replica path is fixed. To minimize such errors, the input common-mode voltage is held constant by an input common-mode feedback (CMFB) circuit. This is realized by adding two extra transistors (M_3 and M_4) at the input, whose gates are connected to the desired common-mode level V_{cm}. These transistors regulate the input common-mode voltage by stealing tail current from the input pair. The current through these two transistors is copied to the output stage, which doubles the bandwidth of the CMFB loop [3]. The output common-mode voltage is defined during the reset phase, when the OTA is operated in a unity-gain configuration and hence the output common-mode voltage becomes V_{cm}.

C. Auto Zeroing

Given that the RIC is continuously connected, an overdrive voltage V_{od} appears at the virtual ground of the first integrator due to the limited transconductance G_m of the OTA (Fig. 9)

$$V_{\text{od}} = \frac{I_{\text{ref}}}{G_m}\left(1 + \frac{C_L}{C_{\text{int}}}\right) \tag{10}$$

where I_{ref} is the current provided by the RIC and the additional factor $I_{\text{ref}}/g_m C_L/C_{\text{int}}$ is due to the current I_L provided to the load capacitance C_L. Since this overdrive voltage is always present at the virtual ground of the integrator, it will be sampled by the SC feedback and thus lead to a charge error Q_e

$$Q_e = V_{\text{od}} C_x = \frac{I_{\text{ref}} C_x}{g_m}\left(1 + \frac{C_L}{C_{\text{int}}}\right). \tag{11}$$

Since the desired signal charge equals $V_{\text{ref}} C_x$, this error charge leads to a relative error in the measured capacitance of $V_{\text{od}}/V_{\text{ref}}$. This error is a function of the transconductance of the OTA. Hence, it is temperature dependent, leading to thermal drift.

A potential solution to reducing the overdrive voltage is to adopt a two-stage Miller-compensated amplifier instead of a single-stage OTA. Since the first stage of such an amplifier now drives the Miller capacitor instead of the integration capacitor, this reduces the input overdrive voltage by the ratio

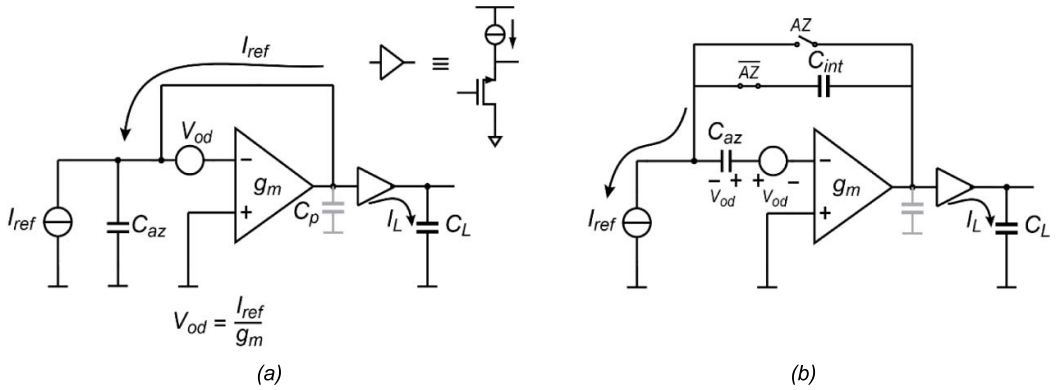

Fig. 9. Single-ended equivalent circuit of the auto-zeroed first integrator. (a) During AZ. (b) During integration.

of the integration capacitor and the Miller capacitor. This ratio would be limited to about 25-fold in our design and does not reduce the overdrive sufficiently.

Therefore, instead, the overdrive is reduced by periodically AZ the front-end integrator, as shown using an equivalent single-ended circuit in Fig. 9. During the AZ phase [Fig. 9(a)], the modulator is "frozen" (the state of the integrators is preserved) and $V_{\rm od}$ is stored on AZ capacitors $C_{\rm AZ1}$ and $C_{\rm AZ2}$. After the AZ, the modulator resumes its normal operation while $V_{\rm od}$ is compensated for by the voltage stored on the AZ capacitors [Fig. 9(b)]. To eliminate errors due to the load current I_L, which is not same during AZ and normal operation, source followers are added at the outputs of the integrator to provide the load current. Offset errors introduced by these source followers are negligible, as they are attenuated by the front-end integrator. Besides canceling $V_{\rm od}$, the AZ also reduces differential and common-mode input offset of the integrator.

In addition to reducing the overdrive voltage, the AZ also helps to reduce errors due the finite gain and offset of the input CMFB circuit. As mentioned, since C_x is a varying sensor capacitance while $C_{\rm rep}$ is fixed, any input common-mode variation will lead to errors. The AZ circuit samples and subtracts such variations and thus improves the linearity of the CDC.

Fig. 10 shows how this AZ operation is embedded in the overall timing of a conversion. During the AZ phase, all other switches are OFF, so as to freeze the states of the integrators. After the AZ phase, the CDC resumes its normal operation. The system-level chopping only happens at the rise edge of AZ signal, so that the overdrive voltage due to the continuous current source can be compensated by the following AZ operation.

The dimensioning of the AZ capacitor involves a trade-off between die size, measurement time, and noise contribution. A larger AZ capacitance occupies a larger die size and requires a longer settling time, thus increasing the overall measurement time and degrading the energy efficiency. Reducing the AZ capacitance, however, increases the kT/C noise associated with the AZ operation [13]. In our design, an AZ capacitance of 10 pF is selected, which results in a noise contribution comparable to that of the sensor capacitor, given by (7). Since the noise contribution of the RIC, given by (6), is dominant, the AZ operation has negligible impact on the resolution of the CDC.

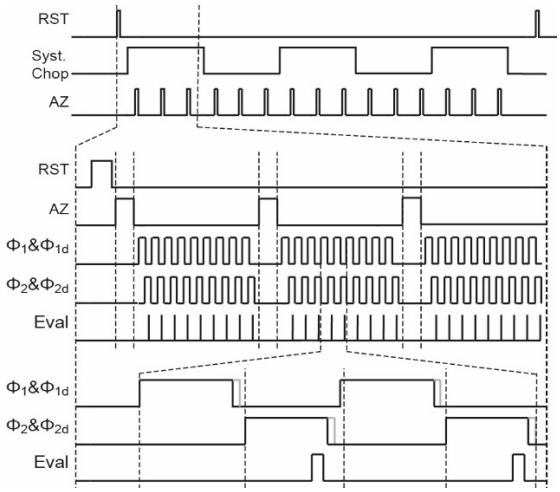

Fig. 10. Timing diagram of the proposed precision CDC with auto-zeroed front-end integrator and system-level chopping.

D. Other Building Blocks

Since the errors of the second and the third integrator are shaped by the first integrator, the requirements for these stages are relaxed. For this reason, their sampling capacitors are designed 4 times smaller than those of the first stage to reduce power consumption [4], [23], [29]. They employ fully differential folded-cascode OTAs (Fig. 11), with a CMFB loop that adjusts the input tail current to keep the output common-mode voltage, sensed using a switched-capacitor network [30], [31]. The integrators are designed to drive a 2.5-pF capacitive load with a unity-gain bandwidth of 5 MHz. Their dc gain is above 80 dB at all working conditions. They consume 20 μA each from a 3.3 V single supply.

The comparator consists of a pre-amplifier with 10$\times$ gain and an analog latch followed by a digital flip-flop. It guarantees a reaction time of less than 3 μs while consumes 10 μA from a 3.3-V single supply.

V. Experimental Results

The CDC was implemented in a 0.35-μm 4P3M CMOS process. It occupies an area of 6 mm^2; including the pad

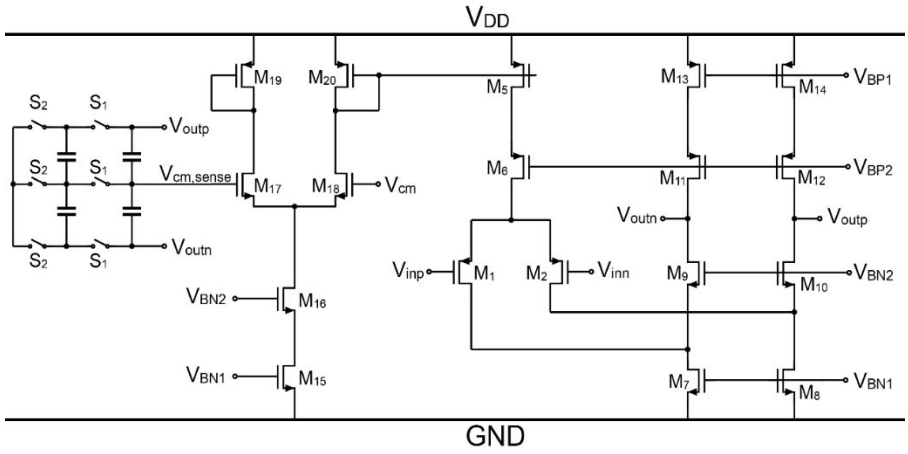

Fig. 11. Circuit diagram of the OTAs of the second and third integrators.

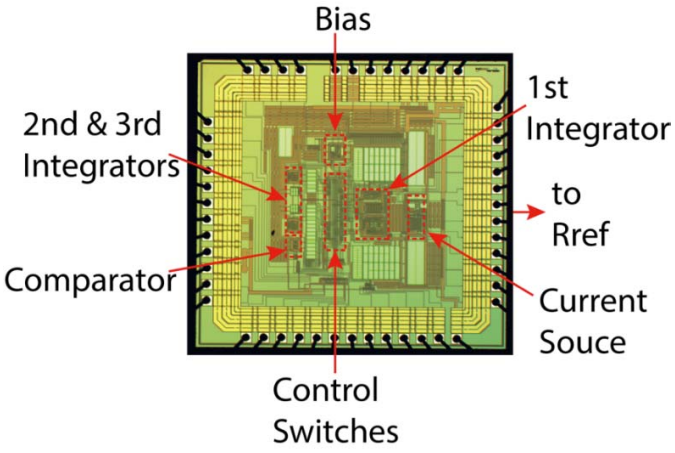

Fig. 12. Chip microphotograph of the precision CDC.

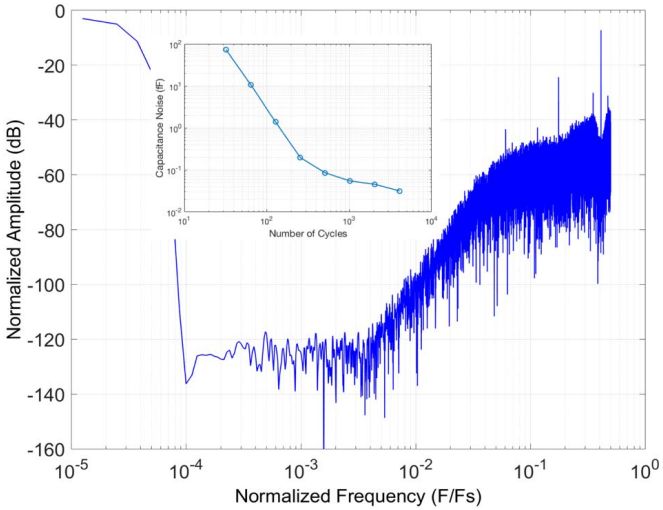

Fig. 13. Measured 65536-point FFT of the output digital bitstream with Kaiser window (frequency normalized to the average sampling frequency $f_s = 200$ kHz). The inset plot shows resolution of the CDC as a function of the number of cycles N that is used to obtain a single decimated output.

ring (Fig. 12). The overall size of the chip is limited by the pad ring, due to test features included on the chip. The size of the CDC circuit is less than 2 mm^2, which in the future can be substantially reduced by layout optimization and removal

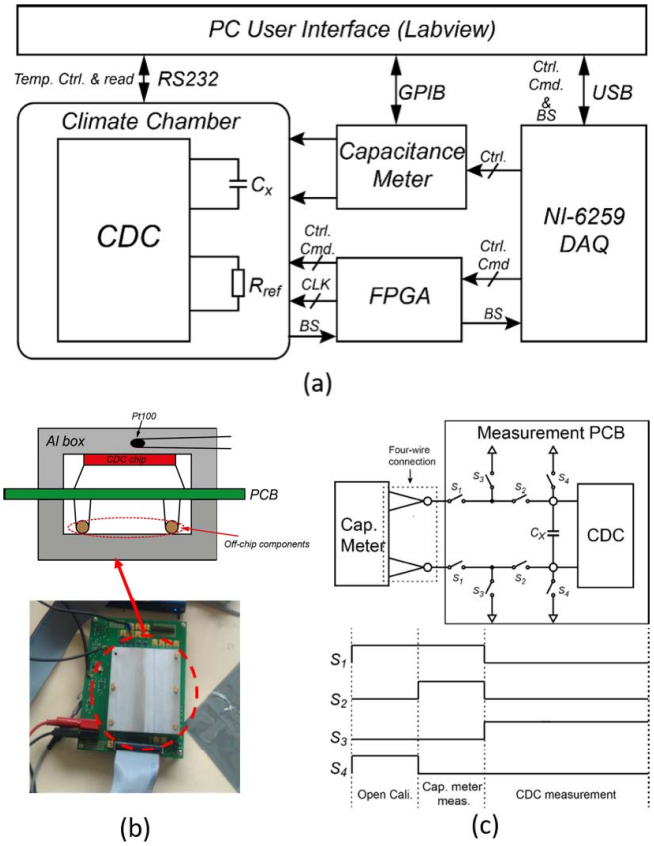

Fig. 14. Measurement setup for thermal stability. (a) Block diagram of the measurement setup. (b) Setup for stabilizing the temperature of the CDC. (c) Calibration scheme for compensating the cabling and parasitic effects of the external capacitance meter.

of test features, such as two 10-pF test capacitors. The chip consumes 230 μA from a 3.3-V supply. The first integrator draws the most current (108 μA) as it needs to handle large parasitic capacitance at the input and directly determines the overall precision performance. The RIC consumes 50 μA because it also directly affects the precision of the CDC. The second and third integrators consume 20 μA each, because they handle relatively small load (2.5 pF) and their error can be suppressed by the front-end stage(s).

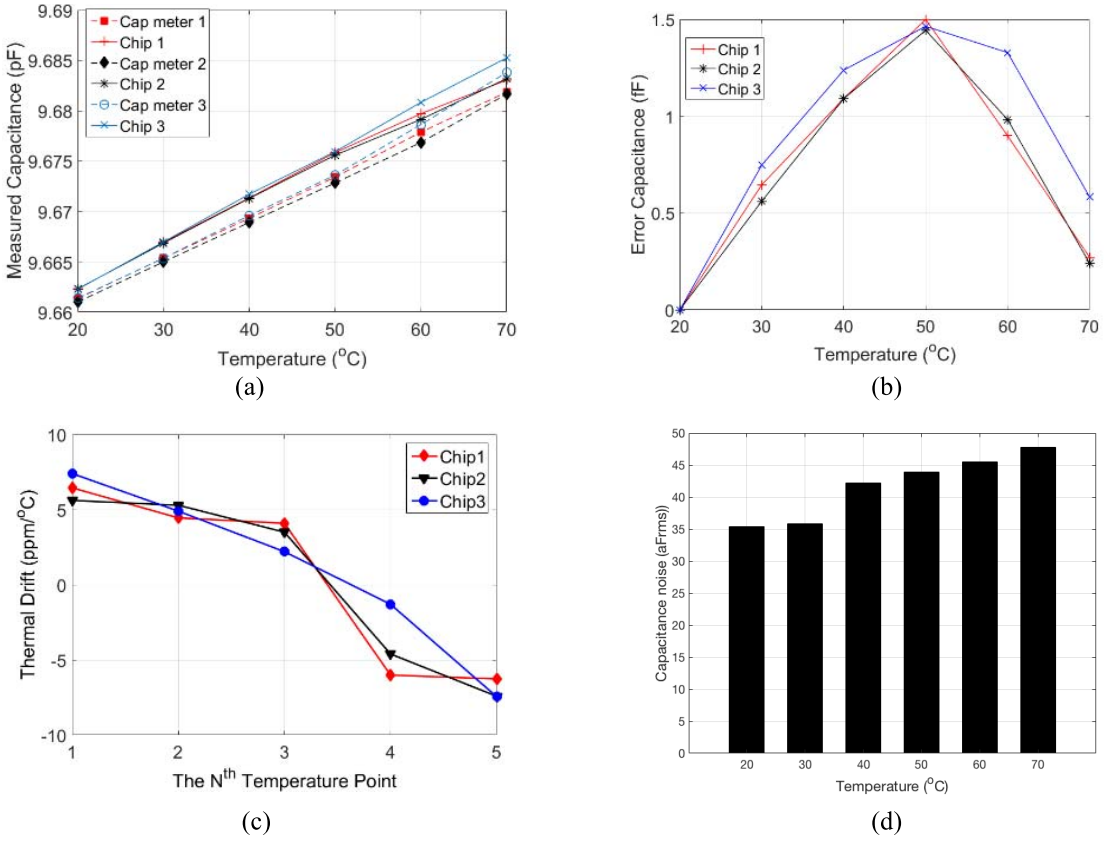

Fig. 15. (a) Measured thermal drift of the off-chip capacitor, using both the designed CDC chip and an external precision capacitance meter. (b) Measurement error with respect to the external capacitance meter. The slope is the thermal drift of the CDC chip. (c) Calculated thermal drift of the CDC chip per measurement temperature range. (x-axis shows the ranges: 1st range: 20 °C–30 °C, 2nd range: 30 °C–40 °C, 3rd range: 40 °C–50 °C, 4th range: 50 °C–60 °C, and 5th range: 60 °C–70 °C.) (d) Capacitance noise at different temperatures obtained by taking standard deviation of 50 successive measurements.

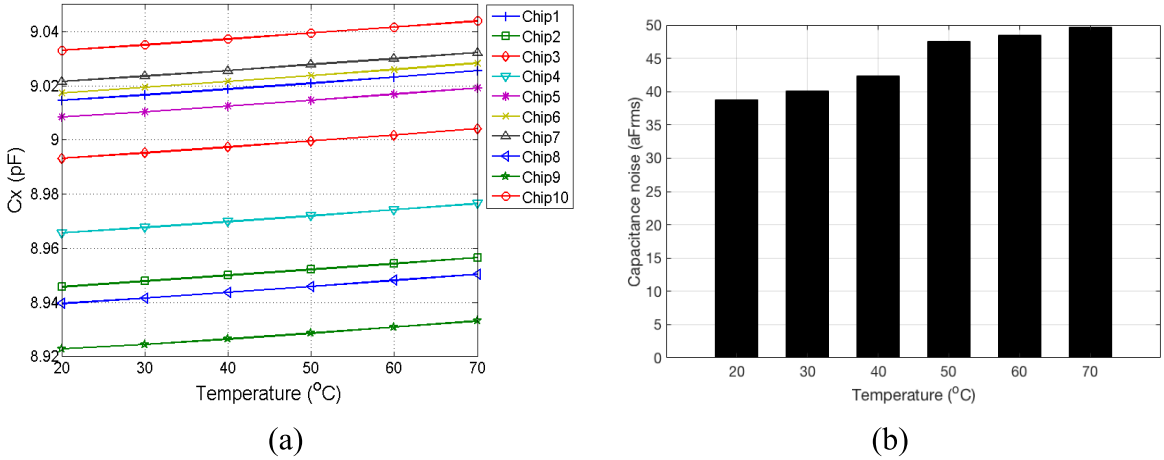

Fig. 16. (a) Measured thermal drift with on-chip PIP capacitor. (b) Capacitance noise at different temperatures obtained by taking standard deviation of 50 successive measurements.

Finally, the comparator draws 10 μA. The biasing circuit, source followers, and on-chip digital circuits consume an additional 22 μA. For flexibility, the Sinc4 decimation filter was implemented off-chip in a field programmable gate array (FPGA).

A. Resolution

Fig. 13 shows a 65536-point FFT of the modulator's output bitstream, demonstrating third-order noise shaping. To determine the resolution of the CDC, the standard deviation of the decimated output bitstream is measured and translated into an equivalent rms noise level on the measured capacitance. The inset of Fig. 13 shows a function of the number of cycles N used to obtain a single decimated output. For small N, the quantization noise dominates. With increasing N, the resolution improves by about 21 dB/octave. After about 500 cycles, thermal noise becomes dominant causing the slope to reduce to about 3 dB/octave. At $N = 2000$, corresponding

to a conversion time of 10.5 ms, an input-referred noise of 42 aF is reached, with corresponds to an ENOB of about 16.7 bits in input range of 16 pF (6 to 22 pF). With the target capacitive sensor (10-μm nominal distance between the two sensor plates, each with a diameter of 20 mm), this translates to a displacement measurement range of 4.5 to 16.5 μm with a displacement resolution of 42 pm.

B. Thermal Stability Measured With an Off-Chip Ceramic Capacitor

The thermal stability of the proposed CDC is determined by measuring an off-chip C0G ceramic capacitor with both the CDC and an external precision capacitance meter (Andeen-Hagerling A2700 [32]) at several temperature points. Thus, the thermal drift of the capacitor is calibrated using the precision capacitance meter, allowing the drift introduced by the CDC to be determined.

A block diagram of the measurement setup is shown in Fig. 14(a). The CDC, the precision references, and the measured capacitor are located in a climate chamber in which the temperature is swept from 20 °C to 70 °C in steps of 10 °C. The whole setup is in good thermal contact with an aluminum block, which minimizes temperature gradients in the setup [Fig. 14(b)]. The temperature of this block is monitored by a commercial Pt-100 temperature sensor, read out by a Keithley 2000 digital multimeter. Before the capacitance measurements are performed, sufficient time (>2 h due to the large thermal mass employed in the measurement setup) is allowed for thermal stabilization of the setup at each temperature step.

Parasitic capacitances due to the connection wires (e.g., the connection between the capacitance meter and the PCB/capacitor) contribute to temperature-dependent measurement errors. These parasitic capacitances are calibrated out using the scheme shown in Fig. 14(c). The precision capacitance meter is connected to the measurement PCB via a four-wire connection to eliminate errors due to the impedance of the connection wires. In addition, an open calibration is performed before each measurement with the help of a set of switches S_1 to S_4 to determine the parasitic capacitance on the PCB from the four-wire connections to the capacitor C_x, which is subtracted from the subsequent readings of the capacitance meter.

Fig. 15(a) shows both the CDC and the external capacitance meter measurement results at different temperatures for three samples of the chip. Taking the measurement results of the external capacitance meter as reference, Fig. 15(b) shows the calculated measurement error introduced by the CDC chip, the slope of which represents thermal drift. In Fig. 15(c), this slope is shown for the different temperature steps (1st: 20 °C to 30 °C, 2nd: 30 °C to 40 °C, etc.). All chips show similar drift within ±7.5 ppm/°C from 20 °C to 70 °C. Fig. 15(d) shows the noise (standard deviation of 50 successive measurements) in this measurement, which is in good agreement with the expected noise level. The non-linear behavior, corresponding to a positive drift at low temperatures and a negative drift at high temperatures, is unexpected. It does not comply with the thermal characteristic of the reference resistor. To explore this further, another stability measurement has been performed using an on-chip capacitor.

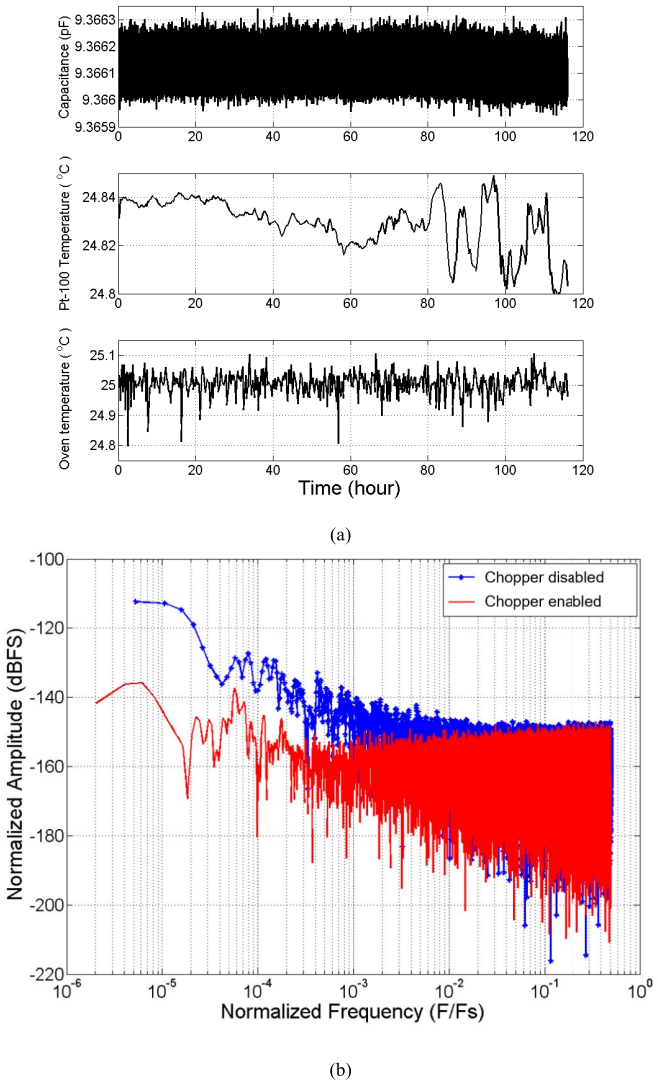

Fig. 17. (a) Measured long-term drift of the CDC under stable temperature and humidity environment. (b) Measured noise spectrum of the proposed CDC. (Results are decimated by Sinc4 filter.)

C. Thermal Stability Measured With an On-Chip Capacitor

The thermal stability is measured with an on-chip poly-insulator-poly (PIP) capacitor using a similar measurement setup. At each stabilized temperature, the on-chip capacitance is measured by the CDC. The results are shown in Fig. 16(a), along with the associated noise level in these measurements [Fig. 16(b)], for ten samples of the chip, all of which show a temperature drift around +24 ppm/°C. This includes the drift of the on-chip PIP capacitor, which cannot be separately measured in this experiment, but is specified to have a temperature coefficient of approximately +30 ppm/°C [33]. Therefore, the thermal drift contributed by the CDC is estimated to be around −6 ppm/°C across the entire temperature range.

This result differs from the drift measured using the external ceramic capacitor. Detailed simulations show that the difference can largely be explained by coupling of bit-

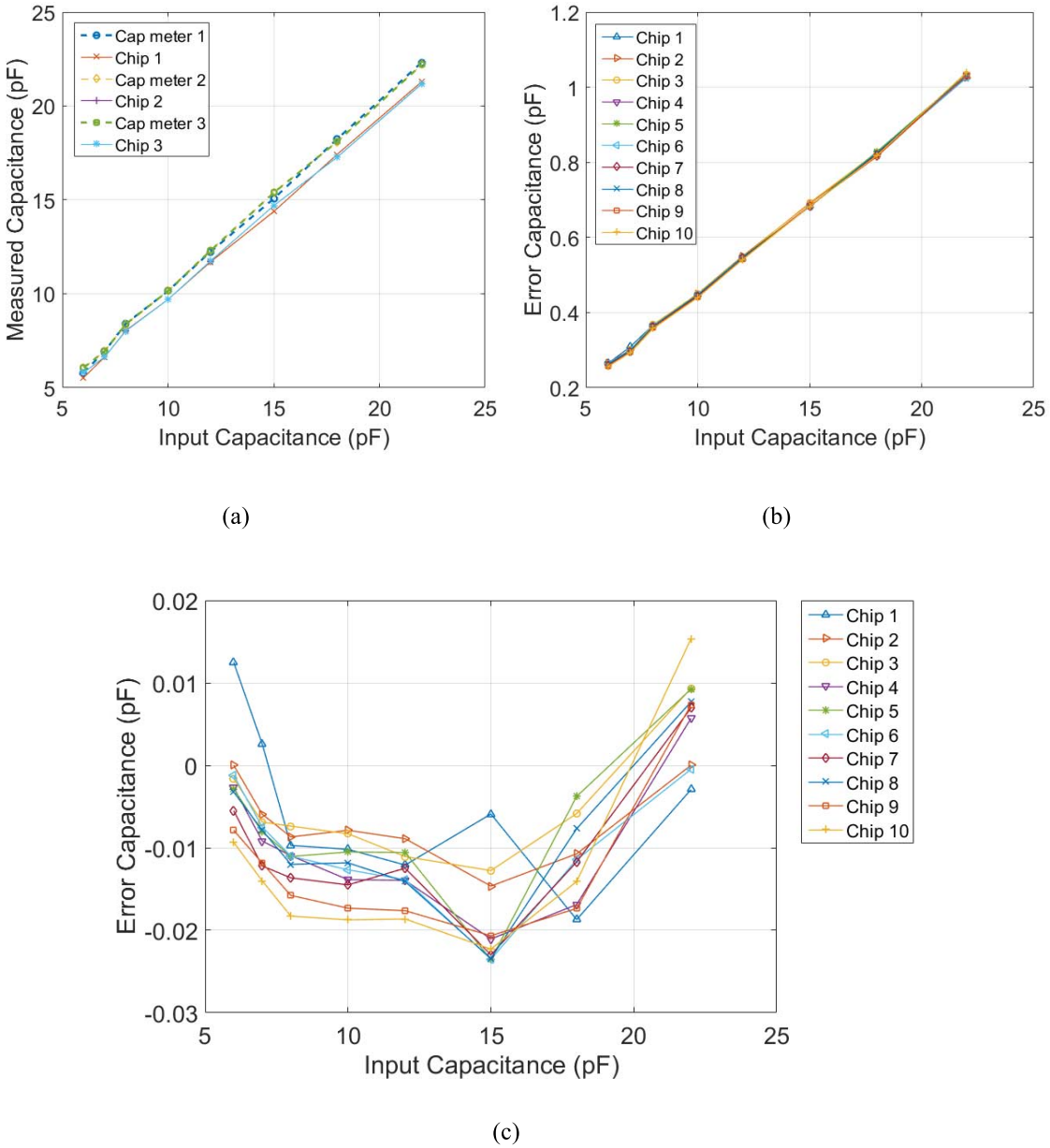

Fig. 18. (a) Measured transfer characteristics of the CDC and the capacitance meter. (Only three chips are shown for simplicity.) (b) Calculated measurement error of the CDC as a function of input capacitance. (c) Absolute error of the CDC measurement after batch calibration, i.e., calibrating one chip (Chip 2) at two points (6 and 22 pF) and applying the result to all other chips.

stream output to the input of the CDC via the electrostatic discharge (ESD) circuitry in the pad ring. This coupling is present when the CDC is configured to measure an off-chip capacitor, not when it measured the on-chip PIP capacitor, and introduces a signal-dependent error that can explain the non-linearity shown in Fig. 15(b). This coupling can be reduced by partitioning the pad ring so that the pads connected to the off-chip capacitor do not share the same ESD supply as the bitstream pad. Fortunately, even with the nonlinearity error, the CDC chip still demonstrates a thermal stability in line with our target.

D. Long-Term Stability

The CDC is designed for a high-precision industrial application that only allows recalibration of the system every few days. Hence, it is important that the CDC maintains the precision within the calibration intervals. A main source of the drift is the $1/f$ noise of the transistors. Therefore, to determine the long-term stability of the CDC, the on-chip PIP capacitor was measured for 116 h such that the drift of the CDC can be evaluated down to a frequency range of microhertz. During this measurement, temperature and humidity in the climate chamber were kept constant such that the measurement will show purely the effect of the $1/f$ noise. Since the temperature coefficient of the on-chip capacitor is in the order of 30 ppm/°C, the temperature variation of the measurement setup should be smaller than 30 mK, so that errors due to temperature variation are less than 1 ppm. To guarantee this, a big Aluminum block is used to stabilize the temperature of the setup. Its temperature is monitored

TABLE I

PERFORMANCE SUMMARY OF THE PROPOSED CDC IN COMPARISON WITH STATE-OF-THE-ART DESIGNS FOR WHICH THERMAL STABILITY IS REPORTED

	[3]	[4]	[5]	[6]	[34]	[35]	[36]	This work
Processor	0.16 µm	0.35 µm	0.35 µm	0.18 µm	0.35 µm	N/A	0.32 µm	0.35 µm
Reference(s)	Current and frequency	Current and frequency	Capacitive	Capacitive	Capacitive	Capacitive	Capacitive	Resistive and time
Sensor capacitance (pF)	0 to 8	0 to 6.8	8.4 to 11.6	0 to 24	0.8 to 1.2	13 to 21	0 to 0.256	6 to 22
Conversion time	0.21 ms	7.6 ms	20 ms	230 ms	50 µs	20 ms	0.38 ms	10.5 ms
ENOB (bit)	10.6	13.5	13.8	15.44	8.8	18.2	6.8	16.7
Temperature coefficient (ppm/°C)	N/A	N/A	N/A	N/A	300	26	300	7.5
Absolute inaccuracy	N/A	N/A	N/A	N/A	N/A	0.05 %[1]	N/A	< 0.2 %[2]
Power consumption	14 µW	211 µW	14.9 mW	33.7 µW	15.8 mW	1.9 mW	84 µW	760 µW
FoM (pJ/step)[3]	1.87	138.6	20.9	0.175	1765	125	283	74

[1] *The accuracy is achieved by individual factory calibration and the accuracy is validated at 25 °C across the capacitance range from 13 pF to 21 pF.*

[2] *The accuracy is achieved by a two-point batch calibration, i.e. by calibrating one chip and then applying the result to all other chips across the range of 6 pF to 22 pF. The performance is also validated at 25 °C. However, since the tolerance of the thermal drift of the CDC is within 10 ppm at all temperatures (20 °C to 70 °C) according to Fig. 6-18, it is expected that similar accuracy can be achieved at different temperatures without the need of extra calibration.*

[3] *The FoM is calculated based the well-accepted equation for Analog-to-Digital converters, as shown:* $FOM = \frac{Pt_{conv}}{2^{ENOB}}$, *where ENOB is defined as:* $\text{ENOB (bits)} = \left(20\log_{10}\frac{\Delta C_{max}}{2\sqrt{2}\sigma_{rms}} - 1.76\right)/6.02$.

during the whole measurement using the Pt100 thermometer. The relative humidity is kept at 50% ± 1%.

During the measurement, the bitstream of CDC was decimated by a Sinc4 filter and then stored. The result does not show any appreciable drift [Fig. 17(a)]. The frequency spectrum of these results, obtained using an FFT, is shown in Fig. 17(b). To verify the effectiveness of chopper, the same measurement was repeated without enabling the chopper. As can be seen from Fig. 17(b), the chopper effectively reduces the *1/f* noise corner without altering the thermal noise level. The measured the *1/f* noise corner with all the choppers enabled is below 200 μHz, corresponding to an hour-long time interval.

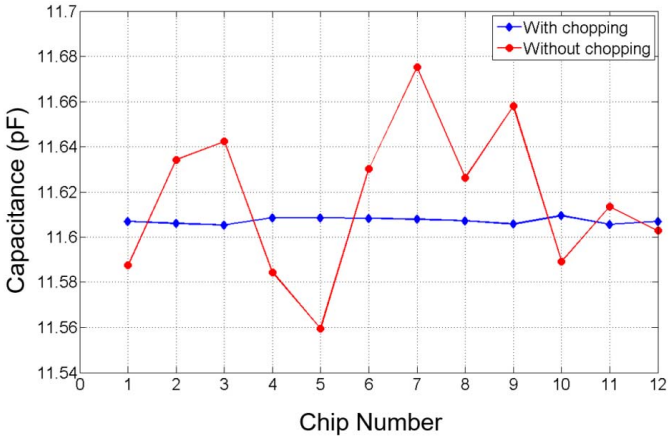

Fig. 19. Variation in the output of different chips measuring the same test capacitor with and without chopping.

E. Absolute Accuracy

The absolute accuracy of the CDC is measured by applying discrete input capacitors in the range from 6 to 22 pF to ten samples of the chip (from one wafer). For each measurement, the discrete capacitors were calibrated using a precision capacitance meter with <0.1% absolute inaccuracy [32]. For illustration, Fig. 18(a) only shows the measurement results of three chips (chip 1, 2, and 3), each with the corresponding calibration results (Cap meter 1, 2, and 3). Fig. 18(b) shows the measurement error of all the ten chips, calculated as the difference between the chip measurement results and calibration results. All chips exhibit a very similar systematic offset and gain error. To eliminate these, a two-point calibration is performed for only one chip and the result is applied to all other chips. As shown in Fig. 18(c), the inaccuracy after this batch calibration is within ±25 fF across the entire capacitance range (6 to 22 pF), which is less than ±0.2%. The residual errors could be related to signal-dependent charge injection, which is not completely compensated by the precision techniques applied and causes non-linearity. The sample-to-sample variation is within ±0.1%.

To quantify the effectiveness of the chopping techniques employed, one capacitor is measured using different chips both with and without enabling the choppers (including the choppers of the RIC and the system-level chopper). Fig. 19 shows the measurement results, from which the effectiveness of the choppers can be clearly seen. Without chopping, the chip-to-chip variation is around 1%. When chopping is applied, this reduces to below 0.1%.

A performance summary and comparison is provided in Table I. Compared to other CDCs for which thermal stability is reported, the proposed CDC represents a significant improvement in thermal stability and has comparable energy efficiency.

VI. Conclusion

A precision CDC has been designed and implemented in a 0.35-μm CMOS technology. The CDC is based on a charge-balancing $\Delta\Sigma$ modulator. To achieve high precision and thermal stability, the sensor capacitance is compared with external resistive and time references, as they are more precise and stable than capacitive references. To deal with various error sources that may degrade the precision, various circuit techniques, such as chopping and AZ, are employed at both system level and circuit level. Measurements of the prototype chip show that the entire system can measure capacitance with an rms resolution of 42 aF in a capacitance range of 6 to 22 pF, corresponding to an ENOB of 16.7 bit. Furthermore, the CDC demonstrates a thermal stability of better than $\pm$7.5 ppm/°C and an absolute inaccuracy (after a two-point batch calibration) within $\pm$25 fF across the entire measurement range. The CDC measures capacitance at a speed of 10.5 ms/sample, while consuming a total power of 760 μW from 3.3-V supply. Compared to the state of the art, this CDC represents a significant improvement in stability, making it a suitable candidate for applications such as precision displacement measurement.

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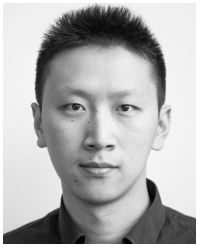

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