

# A 12-b ENOB 2.5-MHz BW VCO-Based 0-1 MASH ADC With Direct Digital Background Calibration

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**Abstract**—This paper presents a scaling friendly mostly digital voltage-controlled-oscillator (VCO)-based 0-1 multistage noise shaping (MASH) analog-to-digital converter. A novel background calibration technique corrects conversion errors due to VCO linear gain drift, residue generating digital-to-analog converter mismatches, and nonlinearity of the VCO voltage-to-frequency conversion. The proposed architecture minimally modifies the basic 0-1 MASH architecture and directly calibrates the main VCOs without relying on replica matching. A redundant first-stage coarse quantizer enables fast error estimation in the digital domain. A 12-b prototype implemented in 180-nm CMOS achieves 12-b ENOB over 2.5 MHz and consumes 4.8 mW from a 1.8 V supply.

**Index Terms**—0-1 multistage noise shaping (MASH), analog-to-digital converter (ADC), background calibration, boundary gap estimation, nonlinearity, VCO-based quantizer, voltage-controlled oscillator (VCO).

## I. INTRODUCTION

VOLTAGE-CONTROLLED oscillators (VCOs) are one of the few key building blocks that have been extensively used in both analog and digital systems. VCO input and output are both analog in nature; however, its output is often easily processed using digital circuits. In addition, a VCO can be used to implement an ideal integrator, an essential analog block in filters and noise-shaped analog-to-digital converters (ADCs). However, it was only recently that a VCO was used to implement ADCs [1]–[14] and analog filters [15]. Besides its inherent frequency to phase integration, passing VCO output through a transition detector directly quantizes its phase. A single-phase VCO-based quantizer is shown in Fig. 1(a) where the VCO transforms analog input to phase and a counter quantizes the accumulated phase each clock period  $T_s = 1/f_s$ , where  $f_s$  is the sampling rate. A multiphase VCO is often used to provide finer phase quantization. Besides providing multiphase outputs, small area and low voltage headroom have made ring VCOs ubiquitous in reported

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VCO-based ADCs [1]–[14]. Fig. 1(b) shows a ring VCO-based quantizer, where VCO phase is quantized by detecting the edge location of the sampled multiphase output using a digital encoder, which can also be viewed as a transition counter.

Fig. 1(c) shows an equivalent model for a continuous-time (CT) VCO-based modulator. Digital differentiator  $(1 - z^{-1})$  first-order shapes quantization noise. A discrete-time equivalent model is also shown in Fig. 1(d). High SQNR can be achieved by increasing the oversampling ratio ( $OSR$ ); however, voltage-to-frequency (V-to-F) nonlinearity introduces significant distortion that limits SNDR. Linearization of VCO-based quantizers has attracted a lot of attention from the research community during the last decade. Replica-based background calibration was proposed to correct VCO nonlinearity in open-loop VCO-based first-order  $\Sigma\Delta$  modulators [1]–[3]. Single stage architecture and mostly digital implementation make this approach very scaling friendly. However, high  $OSR$  and  $f_s$  significantly increase dynamic power. In addition, replica mismatches limit calibration accuracy. A VCO-based quantizer was used to replace the last stage integrator and quantizer of a high-order  $\Sigma\Delta$  modulator [4]–[7]. High-loop gain attenuates distortion components injected at the VCO output, and hence relaxes VCO linearity requirement. However, the mostly analog nature of this architecture negates the scaling benefit enabled by using a VCO.

Alternatively, linearity can be improved by reducing VCO input swing. This can be achieved by using the VCO as the second-stage quantizer in 0-1 MASH architecture [10]–[14]. In addition,  $OSR$  and  $f_s$  are reduced in proportion to the first-stage coarse quantizer resolution. However, this approach suffers from the well-known MASH problems. First, interstage gain has to be accurately defined. This is not easily achieved when using a VCO as its gain significantly drifts with voltage and temperature variations. Second, digital-to-analog converter (DAC) element mismatch error directly shows at output introducing additional distortion. In addition, despite that the motivation of using 0-1 MASH is to reduce VCO input using a medium resolution first stage and relies on the VCO noise shaping to improve SQNR; it is important to note that it is still desirable to have a large VCO full-scale frequency swing  $f_{swing}$  to increase the VCO-based modulator resolution. For a given SQNR specification, this relaxes the coarse quantizer resolution and reduces  $OSR$  and dynamic power. For instance, [13] uses only a 2-b coarse quantizer and relies on dither-based VCO linearization to enable high  $f_{swing}$  and SQNR.

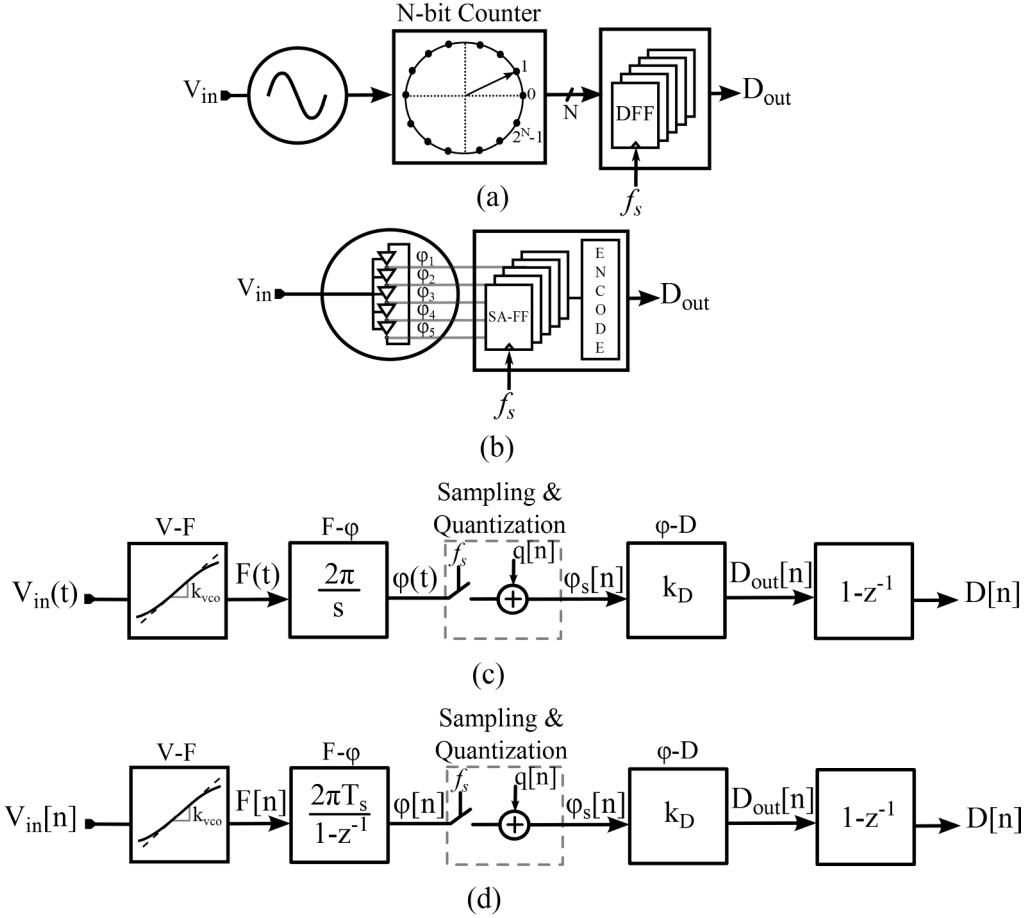


Fig. 1. VCO-based quantizer. (a) Single phase. (b) Multiphase. (c) Equivalent model in a CT  $\Sigma\Delta$  modulator. (d) Equivalent model in a DT  $\Sigma\Delta$  modulator.

Intuitively, relying more on the VCO and simplifying the first stage retains more of the VCO merits, such as small area and good scalability. Furthermore, reducing quantization error reduces background calibration loop convergence time as further explained in Section III.

The aforementioned 0-1 MASH nonidealities were circumvented by placing the MASH modulator inside a high-order  $\Sigma\Delta$  modulator, which relies on loop gain to suppress MASH errors and achieves high resolution using high-order noise shaping [6]. However, again the mostly analog nature of this approach negates the scaling benefit gained by using the VCO. Alternatively, a reduced VCO swing was adopted to eliminate VCO nonlinearity, and foreground calibration was used to correct other linear MASH errors [10], [11]. In [13], background VCO linear gain estimation, DEM, and a dither-based linearization were employed.

This paper presents a background calibration technique that simultaneously corrects for DAC mismatch error, VCO linear gain error, and nonlinearity [14]. In contrast to [13], the technique requires minimal modifications to the basic 0-1 MASH architecture and does not add analog dither to the input, which reduces input dynamic range. To the best of our knowledge, the proposed technique is the first to demonstrate direct background VCO nonlinearity calibration

with short convergence time. Measured start-up convergence time of only 64 ms is comparable to those of [1]–[3] where indirect calibration schemes were adopted. In those schemes, the absence of the input signal from the replica path enables short convergence time. However, this sacrifices calibration accuracy, as the schemes of [1]–[3] rely on accurate replica matching, which is hard to guarantee under process, voltage, and temperature (PVT) variations. A direct application of the technique in [1] to calibrate the main VCOs in the signal path suffers from very long convergence time, in the order of tens of seconds. Our proposed technique achieves fast convergence while directly calibrating the main VCOs. Fast convergence speed is achieved by reducing estimation error in the calibration loop. This is enabled by the use of narrow detection windows centered on the coarse quantizer decision boundaries. Only when the input falls inside these detection windows, the coarse quantizer is selectively dithered, and the corresponding ADC outputs, referred to as calibration samples, are processed by the calibration unit to estimate the correction parameters. This reduces calibration samples variance, which significantly shortens convergence time. Compared with the “split ADC” approach [16], selective dithering enables using a larger dither without sacrificing signal dynamic range. In addition, lower quantization error enabled by using the coarse quantizer reduces estimation error, further reducing convergence

TABLE I  
COMPARISON OF THE PROPOSED ARCHITECTURE TO EXISTING VCO-BASED  $\Sigma\Delta$  MODULATORS

	VCO Embedded in $\Sigma\Delta$ loop [4]–[8]	Open-Loop Single Stage [1]–[3]	Split ADC [16]	0-1 MASH Low VCO Swing [10]–[12]	0-1 MASH High VCO Swing [13]	This Work
Precision OTA-Based Analog Blocks	✓	✗	✗	✗	✗	✗
Adds Analog Dither to Input	✗	✗	✓	✗	✓	✗
Reduced VCO swing	✓ <sup>*</sup>	✗	✗	✓	✗	✗
V-to-F Nonlinearity Calibration	✗	Indirect Background	Direct Background	✗	Dither-Based Linearization	Direct Background
Replica VCO	✗	✓	✗	✗	✗	✗
Mostly Digital	✗	✓	✓	✓	✓	✓
Oversampling Ratio	Low	High	High	Low	Low	Low
Restrictions on Input Signal	✗	✗	✓	✗	✗	✓
VCO V-to-F Direct Background Calibration Time Constant	NA	$\sim 10^{10}$ samples <sup>**</sup>	$\sim 10^6$ samples	NA	NA	$\sim 10^5$ samples <sup>†</sup>

\* Some implementations reduce VCO swing to relax loop gain requirements.

\*\* Excludes [3] which can be applied only for indirect (replica-based) calibration. Value represents convergence time for [1] if the dither is added to the signal path to perform direct calibration of the main VCOs.

<sup>†</sup>In this work, overall calibration convergence time constant is set by the slower linear gain error and DAC mismatch errors calibration loop and is in the order of  $10^6$  samples. However, the V-to-F nonlinearity calibration time constant is much shorter in the order of  $10^5$  samples.

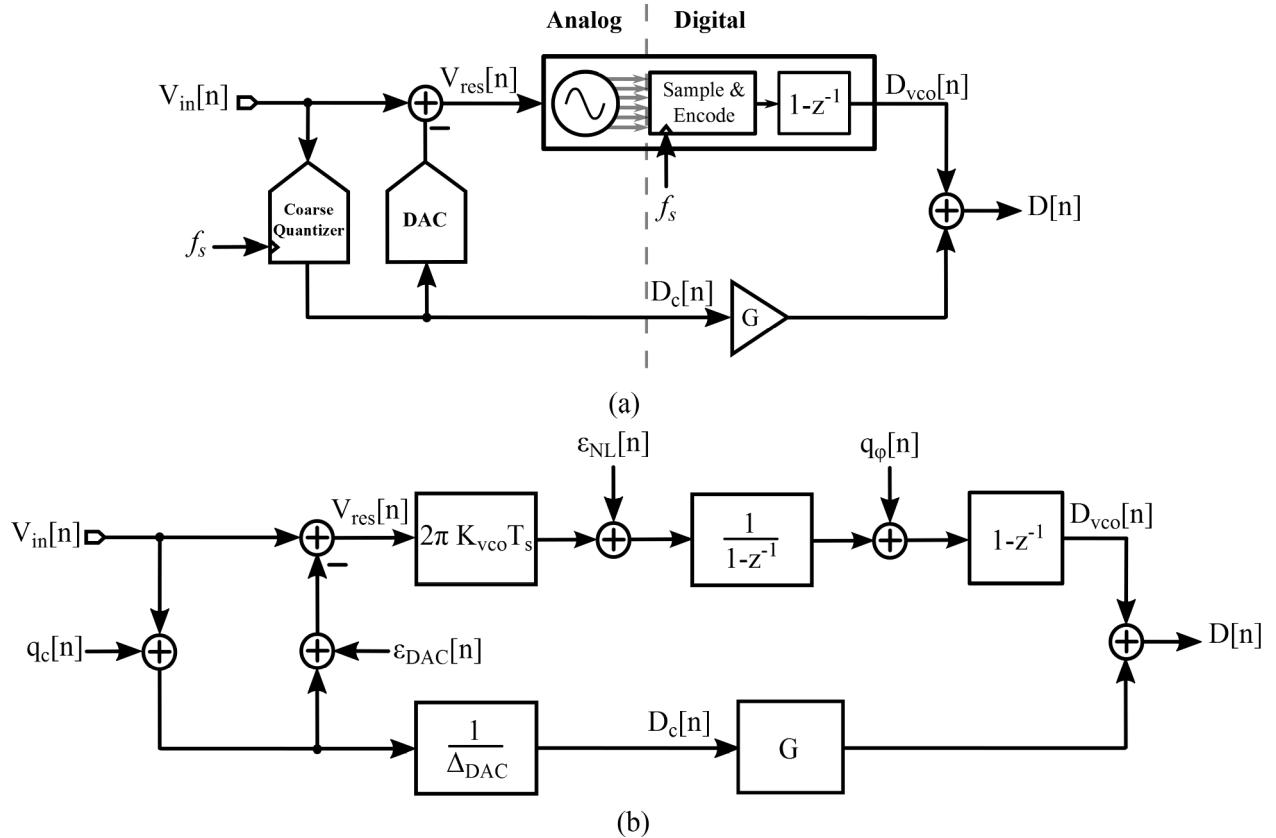


Fig. 2. (a) High level block diagram of a VCO-based 0-1 MASH and (b) its equivalent model.

time. Table I compares our work with prior approaches in VCO-based  $\Sigma\Delta$  modulators. The proposed design corrects MASH errors using direct background calibration and operates at a much lower *OSR* compared with [1]–[3], does not require precision analog blocks [4]–[7], does not require analog dither [13], and is mostly digital. However, similar to most direct background calibration techniques, it places restrictions on ADC input as further discussed in Section III.

This paper is organized as follows. Section II presents the VCO-based 0-1 MASH architecture and illustrates error

correction. Section III presents the proposed background calibration. Circuit implementation is described in Section IV. Section V reports the measured results. Finally, Section VI draws the conclusion.

## II. VCO-BASED 0-1 MASH ARCHITECTURE

### A. Basic Operation and Modeling

System level block diagram of a VCO-based 0-1 MASH is shown in Fig. 2(a). ADC operation is as follows. First,

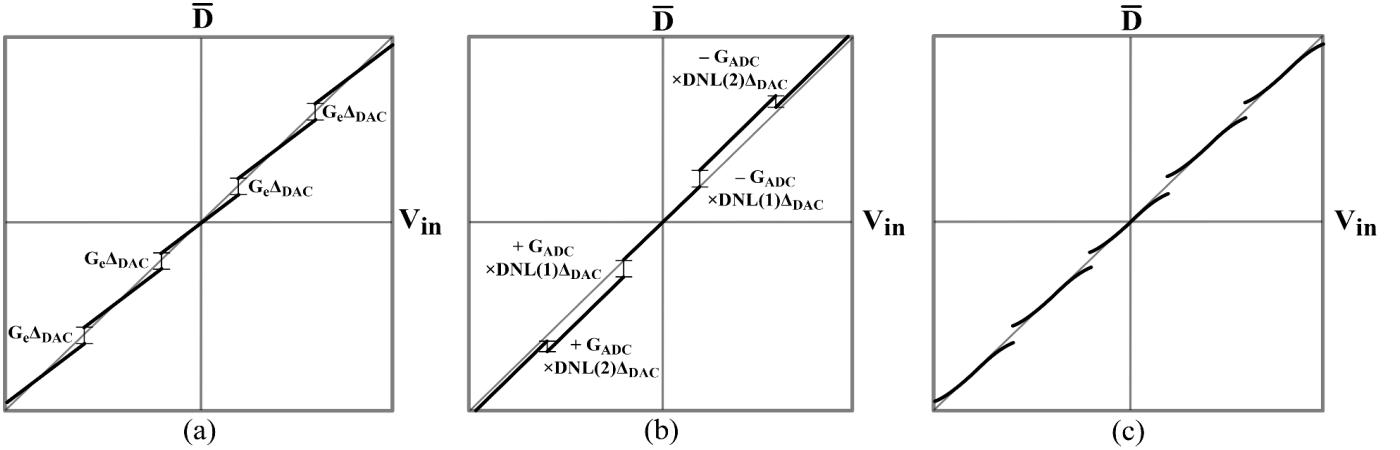


Fig. 3. ADC transfer function in the presence of only (a) gain error  $G_e$ , (b) DAC mismatch error, and (c) VCO tuning curve nonlinearity.

discrete-time input  $V_{in}[n]$  is coarse quantized. Second, residue  $V_{res}[n]$  is generated by subtracting coarse quantizer output  $D_c[n]$  from  $V_{in}[n]$ . Next,  $V_{res}[n]$  is applied to a VCO-based modulator. Finally,  $D_c[n]$  is scaled by  $G$  and added to the VCO-based modulator output  $D_{vco}[n]$  to obtain MASH output  $D[n]$ .

An equivalent model is shown in Fig. 2(b).<sup>1</sup> Phase-to-digital conversion gain  $k_D$  is assumed unity for simplicity of presentation.  $\varepsilon_{DAC}[n]$  is DAC mismatch error. Assuming a differential  $N$  trilevel element  $\{-\Delta_{DAC}, 0, +\Delta_{DAC}\}$  DAC, where  $\Delta_{DAC}$  is the DAC step size,  $\varepsilon_{DAC}[n]$  is given by

$$\varepsilon_{DAC}[n] = \begin{cases} \text{sgn}(D_c[n])\Delta_{DAC} \sum_{i=1}^{|D_c[n]|} \text{DNL}(i), & |D_c[n]| > 0 \\ 0, & |D_c[n]| = 0 \end{cases} \quad (1)$$

where  $\text{DNL}(i)$  is the DAC differential nonlinearity. Notice that  $\varepsilon_{DAC}$  has odd symmetry for complementary  $D_c$ . This property is a requirement for our proposed nonlinearity calibration technique.  $\varepsilon_{NL}[n]$  is VCO V-to-F nonlinearity error. For a pseudo-differential implementation,  $\varepsilon_{NL}[n]$  is third-order nonlinearity limited and is expressed as

$$\varepsilon_{NL}[n] \cong 2\pi T_s \gamma V_{res}^3[n] \quad (2)$$

where  $\gamma$  is the VCO V-to-F third-order nonlinearity coefficient. ADC output  $D[n]$  is given by

$$D[n] = G_{ADC}V_{in}[n] + G_e q_c[n] - (G_{ADC} - G_e)\varepsilon_{DAC}[n] + \varepsilon_{NL}[n] + (1-z^{-1})q_\phi[n] \quad (3)$$

where  $q_c[n]$  is first-stage quantization error,  $q_\phi[n]$  is phase quantization error, and  $G_{ADC} = G/\Delta_{DAC}$  is the ADC gain. Ideally,  $G$  is selected, such that gain error  $G_e = G_{ADC} - 2\pi k_{vco} T_s$  is nulled for the target  $f_s$  (note that this condition is only satisfied for a single  $f_s$ ). In the absence of gain error, DAC mismatches, and VCO nonlinearity,  $D$  is linearly proportional to  $V_{in}$  and  $q_c[n]$  is cancelled.

<sup>1</sup>The model assumes that both DAC and pseudo-differential VCO offsets are zero. The impact of offset will be discussed in Section IV.

Gain error due to PVT variations of  $k_{vco}$  leads to  $q_c[n]$  leakage to the output and introduces nonlinearity in the ADC transfer function. This is manifested as decision boundary gaps in the ADC transfer function, as shown in Fig. 3(a). The gaps are all equal to  $G_e \Delta_{DAC}$  independent of  $D_c$ . DAC mismatches introduce decision boundary gaps that are  $D_c$ -dependent, as shown in Fig. 3(b), and are equal to the corresponding DAC code DNL scaled by the VCO-based modulator gain (equal to ADC gain in the absence of gain error). The impact of VCO nonlinearity is shown in Fig. 3(c), assuming third-order nonlinearity. Notice that DAC mismatch decision boundary gaps are only  $D_c$ -dependent, whereas VCO nonlinearity error is only  $D_{vco}$ -dependent.

### B. Error Correction

ADC transfer function is linearized by correcting for VCO nonlinearity and subtracting decision boundary gaps due to VCO linear gain error and DAC mismatches, as shown in Fig. 4. Equation (3) can be expressed as

$$D[n] = (G_{ADC} - G_e)V_{in}[n] + \alpha[n] + \varepsilon_{NL}[n] + (1-z^{-1})q_\phi[n] \quad (4)$$

where  $\alpha[n]$  is given by

$$\alpha[n] = \begin{cases} \text{sgn}(D_c[n]) \sum_{i=1}^{|D_c[n]|} \beta_i, & |D_c[n]| > 0 \\ 0, & |D_c[n]| = 0 \end{cases} \quad (5)$$

where  $\beta_i$ ,  $i \in [1, N]$ , is the  $i^{\text{th}}$  decision boundary gap due to linear errors (VCO gain and DAC mismatch errors) [see Fig. 5(b)], and is given by

$$\beta_i = G_e \Delta_{DAC} - (G_{ADC} - G_e)\text{DNL}(i)\Delta_{DAC}, \quad i \in [1, N]. \quad (6)$$

Assuming that we devise a procedure to estimate  $\beta_i$  and a nonlinearity correction coefficient  $\eta = 2\pi T_s \gamma / (2\pi T_s k_{vco})^3$ , and let us denote the estimated values  $\hat{\beta}_i$  and  $\hat{\eta}$ , corrected ADC output  $D'[n]$  is given by

$$D'[n] = D[n] - \hat{\alpha}[n] - \hat{\eta} D_{vco}^3[n] \quad (7)$$

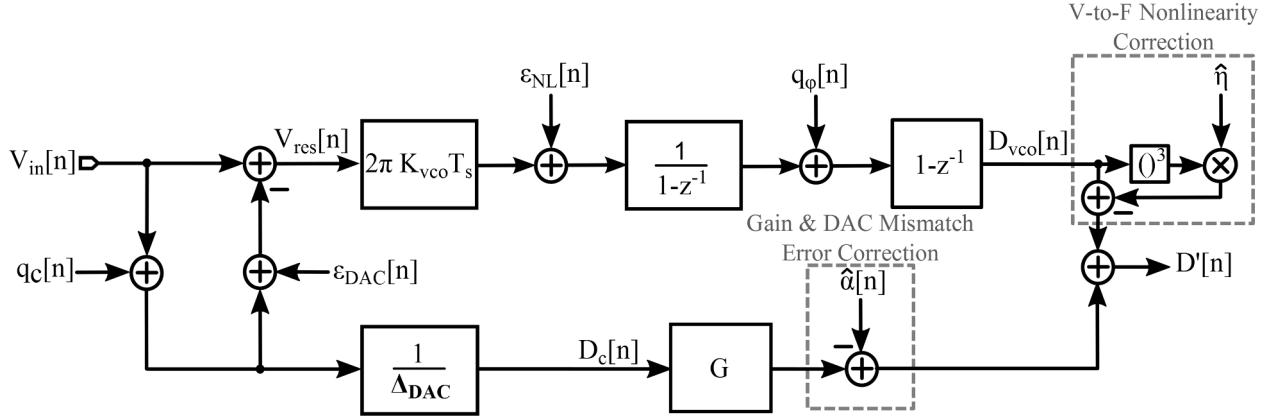


Fig. 4. Digital correction of VCO third-order nonlinearity and decision boundary gaps due to linear errors (VCO gain and DAC mismatch errors).

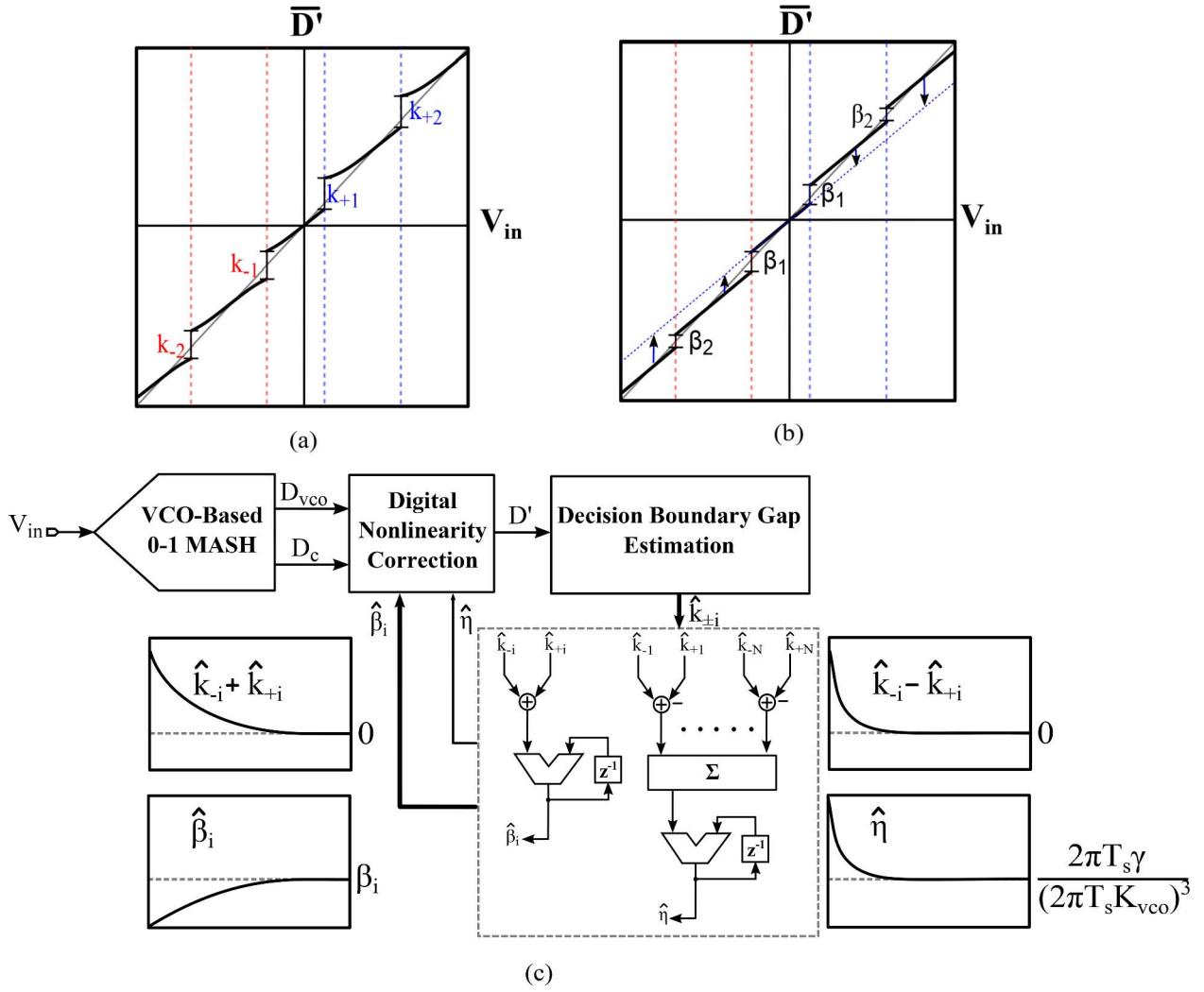


Fig. 5. Decision boundary gaps in the presence of (a) gain, DAC mismatch, and VCO nonlinearity errors and (b) gain and DAC mismatch errors only. (c) Zero-error forcing coefficient estimation LMS loops.

where  $\hat{\alpha}[n]$  is given by (5) after replacing  $\beta_i$  with  $\hat{\beta}_i$ . In the limit that  $\hat{\beta}_i = \beta_i$  and  $\hat{\eta} = 2\pi T_s \gamma / (2\pi T_s k_{vco})^3$ ,  $D'[n]$  is given by

$$D'[n] \cong (G_{ADC} - G_e)V_{in}[n] + (1-z^{-1})q_\phi[n] \quad (8)$$

$D'[n]$  is linearly proportional to  $V_{in}[n]$ . The ADC has gain error, which is acceptable in most applications, but its output

is free from distortion. The key to nonlinearity correction is decision boundary gaps  $k_{\pm i}$  estimation, which are shown in Fig. 5(a). Assuming VCO nonlinearity is cancelled, then  $k_{-i} = k_{+i} = \beta_i$  and ADC transfer function is linearized by shifting transfer function segments by  $\beta_i$ , as shown in Fig. 5(b). Placing the coarse quantizer positive and negative threshold levels asymmetrically as shown in Fig. 5(a)

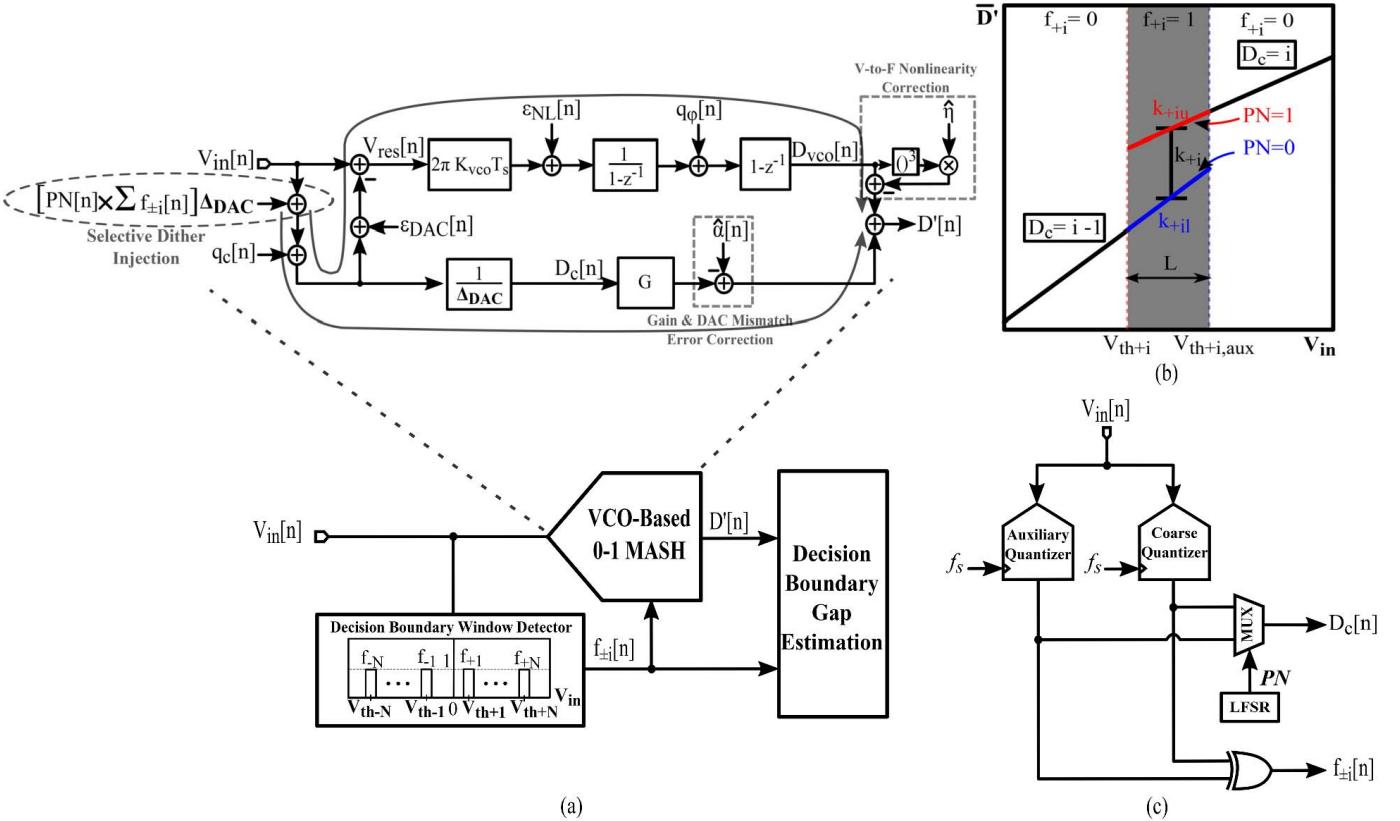


Fig. 6. (a) Conceptual block diagram of the proposed fast decision boundary gap estimation. (b) Selective dithering of coarse quantizer output at the decision boundary. (c) Circuit block diagram for realizing decision boundary window detection and selective dithering.

enables  $\hat{\eta}$  estimation using difference  $(k_{-i} - k_{+i})$ . Assuming negative  $\gamma$ , i.e., compressive tuning curve, then  $k_{+i} > k_{-i}$  and their difference is used in a zero-error forcing LMS loop to estimate  $\hat{\eta}$ , as shown in Fig. 5(c). For each calibration cycle  $m$ ,  $\hat{\beta}_i[m]$  and  $\hat{\eta}[m]$  are updated using  $\hat{k}_{\pm i}[m]$ , as given by

$$\hat{\beta}_i[m] = \hat{\beta}_i[m-1] + \mu_\beta (\hat{k}_{-i}[m] + \hat{k}_{+i}[m]) \quad (9)$$

and

$$\hat{\eta}[m] = \hat{\eta}[m-1] + \mu_\eta \sum_{i=1}^N (\hat{k}_{-i}[m] - \hat{k}_{+i}[m]). \quad (10)$$

The  $\hat{\eta}$ -estimation LMS loop forces  $k_{-i} = k_{+i}$ , which is only satisfied when the VCO is linearized. Simultaneously,  $\hat{\beta}_i$  LMS loops force  $k_{\pm i}$  to zero and  $\hat{\beta}_i$  converges to  $\beta_i$ . In Section III, we propose a fast decision boundary gap estimation technique, which is a key for error correction.

### III. FAST DECISION BOUNDARY GAP ESTIMATION

#### A. Basic Concept

Decision boundary gap estimation is a key to error correction in a multistage ADC architecture, e.g., pipeline ADCs [17]. Our proposed architecture employs a fast decision boundary gap estimation technique that relies on detecting whenever the ADC input is close to the decision boundary and selectively dithering the coarse quantizer output [18].

A conceptual block diagram is shown in Fig. 6(a). The decision boundary window detector vector output  $f_{\pm i}$ ,  $i \in [1, N]$  for a  $2N$  level coarse quantizer, is given by

$$f_{\pm i}[n] = \begin{cases} 1, & |v_{in}[n] - V_{th\pm i}| \leq L_{\pm i}/2 \\ 0, & |v_{in}[n] - V_{th\pm i}| > L_{\pm i}/2 \end{cases} \quad (11)$$

where  $V_{th\pm i}$  are the coarse quantizer thresholds and  $L_{\pm i}$  are the corresponding window detector width. Whenever  $f_{\pm i} = 1$ , two actions are taken. First, a random dither of amplitude  $\Delta_{DAC}$  is added to the coarse quantizer input, which effectively dithers coarse quantizer output  $D_c$  between  $D_c = i$  and  $D_c = i \mp 1$ , as shown in Fig. 6(b). Second,  $D'$  is captured by the decision boundary gap estimation logic. Decision boundary gap  $k_{\pm i}$  can be estimated as

$$\hat{k}_{\pm i} = \pm(\overline{D'}|_{f_{\pm i}=1, D_c=i} - \overline{D'}|_{f_{\pm i}=1, D_c=i\mp 1}) \quad (12)$$

which is equivalent to the correlation of the captured  $D'$  samples with the selectively added dither. Notice that the added dither simultaneously experiences the first-stage and second-stage transfer functions at the decision boundary and is cancelled at the output only when gains are equated. In addition, the dither does not reduce input dynamic range neither does it increase  $V_{res}$  swing as it is only selectively added and cancels at the output.

The window detection and selective dithering functions are implemented by replacing the coarse quantizer by the circuit shown in Fig. 6(c). An auxiliary quantizer is added

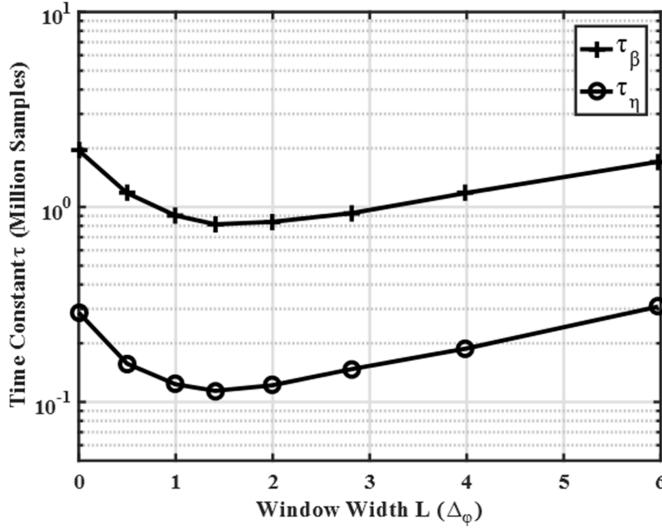


Fig. 7. Calibration loop time constants  $\tau_\beta$  and  $\tau_\eta$  as a function of window detection width  $L$ .

to implement the window detection function. The auxiliary quantizer is a replica of the coarse quantizer, i.e., for a given input, both quantizers have the same nominal output. However, due to random mismatches and noise, the two quantizers have different outputs whenever  $V_{in}$  is close to quantization thresholds. For instance, assuming  $V_{th+i,aux}$  is larger than  $V_{th+i}$ , as shown in Fig. 6(b), then  $D_c = i$  and  $D_c = i - 1$  for the coarse and auxiliary quantizers, respectively, whenever  $V_{th+i} < V_{in} < V_{th+i,aux}$ . Flags  $f_{\pm i}$  are generated by XORing the thermometer-coded coarse and auxiliary quantizer outputs. Window width  $L_i$  is set by  $V_{th+i,aux}$  and  $V_{th+i}$ , as shown in Fig. 6(b). Selective dithering is achieved by randomly selecting the main or the auxiliary quantizer output as the first-stage output, as shown in Fig. 6(c). This effectively dithers  $D_c$  only when  $f_{\pm i} = 1$ .

### B. Estimation Errors and Convergence Time

For simplicity of discussion, let us assume that all window detection widths are equal, i.e.,  $L_{\pm i} = L$ . For each calibration cycle, a finite number of samples  $M_{c,\pm i}$  are used to estimate the upper and lower boundaries of each boundary gap in (12). For instance, upper boundary  $\hat{k}_{+iu}$  is given by

$$\hat{k}_{+iu} = \frac{1}{M_{c,+i}} \sum_{j=1}^{M_{c,+i}} D_{cal,+iu}[j] \quad (13)$$

where  $D_{cal,+iu}$  values are the corresponding captured  $D'$  calibration samples and given by

$$D_{cal,+iu} = D'|_{f_{+i}=1, D_c=i}. \quad (14)$$

At steady state, i.e., after calibration loop convergence, and assuming  $G_{ADC}$  of unity,  $D_{cal,+iu}$  can be expressed as

$$\begin{aligned} D_{cal,+iu}[j] &\cong V_{in}[j] + v_{ns}[j] + v_{n\varphi}[j] + q_\varphi[j] - q_{\varphi d}[j] \\ &|V_{in}[j] + v_{n1}[j] - V_{thm,+i}| < \frac{L}{2} \end{aligned} \quad (15)$$

where  $V_{thm,+i}$  is the mean of  $V_{th+i}$  and  $V_{th+i,aux}$ ,  $v_{ns}$  is the input sampling kT/C noise,  $v_{n\varphi}$  is the input referred RMS VCO phase fluctuation over one conversion cycle,  $q_{\varphi d}[j]$  is the phase quantization error of the previous sample, and  $v_{n1}$  is the first-stage quantizer input referred RMS noise. Estimation error variance of  $\hat{k}_{+iu}$  is given by

$$\begin{aligned} \text{var}(\hat{k}_{+iu}) &= \frac{1}{M_{c,+i}} \left( \frac{L^2}{12} + \sigma_{ns}^2 + \sigma_{n\varphi}^2 + \frac{\Delta_\varphi^2}{6} \right) \\ &\cong \frac{1}{12M_{c,+i}} (L^2 + 2\Delta_\varphi^2) \end{aligned} \quad (16)$$

where  $\Delta_\varphi$  is the phase quantization step size.  $\sigma_{ns}$  and  $\sigma_{n\varphi}$  are typically smaller than quantization noise power, and hence have been ignored in (16). Substituting for  $M_{c,+i}$  in terms of the number of full rate ADC samples per calibration cycle ( $M$ ),  $\text{var}(\hat{\beta}_i)$  is given by<sup>2</sup>

$$\begin{aligned} \text{var}(\hat{\beta}_i) &\cong \mu_\beta \frac{\pi}{2} (\text{var}(\hat{k}_{+iu}) + \text{var}(\hat{k}_{+il}) + \text{var}(\hat{k}_{-iu}) + \text{var}(\hat{k}_{-il})) \\ &= \mu_\beta \frac{\pi}{12ML} (L^2 + 2\Delta_\varphi^2) \\ &\times \left( \frac{1}{f_{in}(V_{in} = V_{th+i})} + \frac{1}{f_{in}(V_{in} = V_{th-i})} \right) \end{aligned} \quad (17)$$

where  $f_{in}$  is the input signal probability density function (PDF). Assuming a uniform input distribution  $[-V_{ref}, +V_{ref}]$  and target  $\text{var}(\hat{\beta}_i) < \xi_\beta^2$  to meet THD specification,  $\beta_i$  calibration loop time constant  $\tau_\beta \equiv (M/\mu_\beta)$  should satisfy

$$\tau_\beta = \frac{M}{\mu_\beta} \geq \frac{\pi V_{ref}}{3\xi_\beta^2} \left( L + \frac{2\Delta_\varphi^2}{L} \right). \quad (18)$$

Notice that  $\tau_\beta$  is minimized for  $L = \sqrt{2}\Delta_\varphi$  and linearly increases with  $L$  for  $L \gg \Delta_\varphi$ . In addition,  $\tau_\beta$  minimum is linearly proportional to  $\Delta_\varphi$ . Doubling the VCO-based quantizer resolution reduces convergence time by a factor of 2. Similarly,  $\eta$  calibration loop time constant  $\tau_\eta$  should satisfy

$$\tau_\eta \geq \frac{1}{N} \frac{\pi V_{ref}}{3\xi_{\Delta k}^2} \left( L + \frac{2\Delta_\varphi^2}{L} \right) \quad (19)$$

where  $\xi_{\Delta k}^2$  is the upper limit for  $\text{var}(\Delta k)$  to meet THD specification, where  $\Delta k = k_{-i} - k_{+i}$  is the gap difference due to  $\eta$  estimation error.

Whereas  $\xi_\beta^2$  and  $\xi_{\Delta k}^2$  could be obtained numerically using behavioral simulations and used in (18) and (19) to obtain calibration loops time constants, the objective of (18) and (19) is to provide a guideline for selecting  $L$ . Behavioral simulations can be used to directly obtain the limits on calibration loop time constants to meet the target THD. MATLAB simulations are used to obtain  $\tau_\eta$  and  $\tau_\beta$  for  $\text{THD} < -80\text{dB}$  with a  $-1\text{-dBFs}$  sinusoidal input assuming a 14-level coarse quantizer,  $v_{n1} = 1.3$  mV,  $V_{ref}$  of 1.8 V, and  $\Delta_\varphi = 2^{-8}V_{ref}$ . Fig. 7 shows  $\tau_\eta$  and  $\tau_\beta$  as a function of  $L$ . Notice that  $\tau_\eta$  is almost an order of magnitude smaller than  $\tau_\beta$ . This is attributed to two

<sup>2</sup>This can be obtained by integrating the product of  $\text{var}(\hat{k}_{+iu})$  by the square of the transfer function  $H(z) = \hat{\beta}_i(z)/\hat{k}_{+iu}(z)$  which can be derived using the block diagrams in Fig. 4 and Fig. 5c.

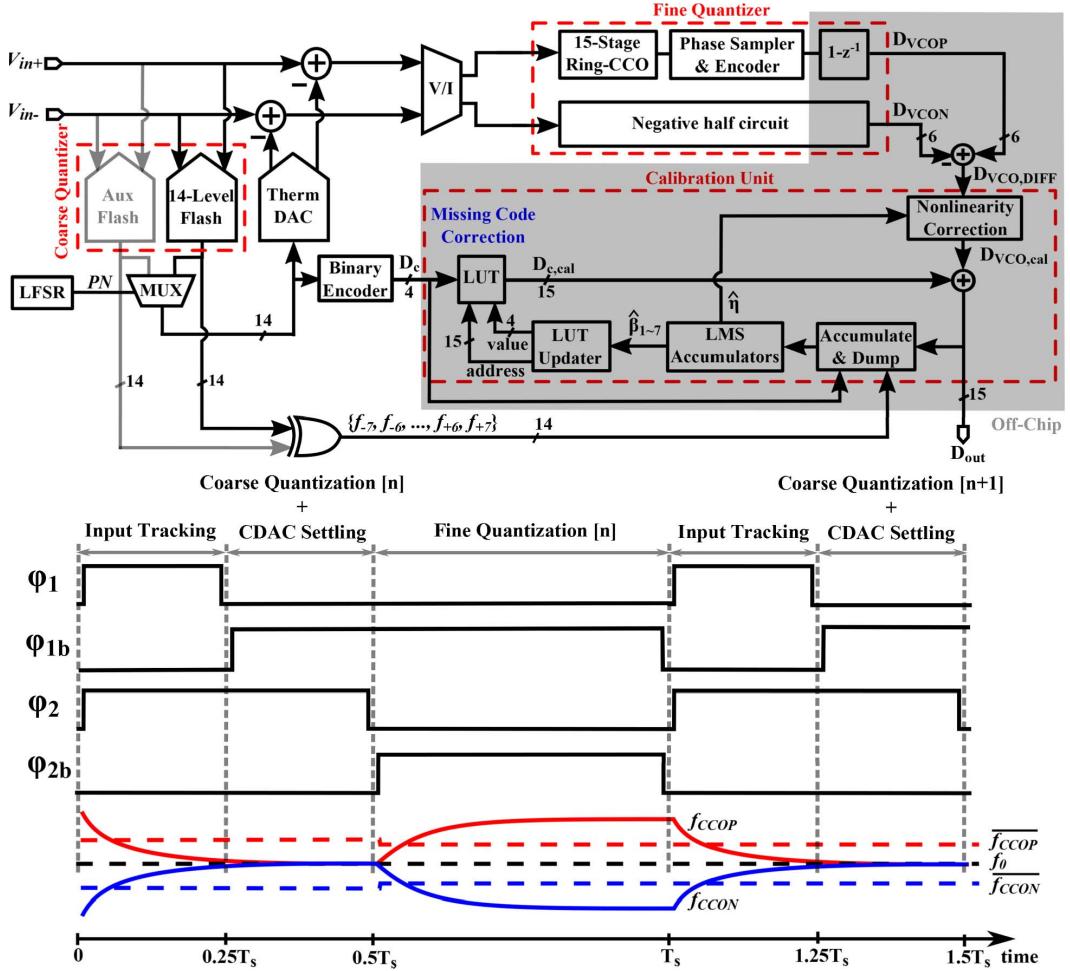


Fig. 8. High-level block diagram and timing of the implemented prototype ADC.

factors: first,  $\xi_{\Delta k}^2$  is typically larger than  $\xi_{\beta}^2$  for a given THD target. Intuitively, more  $\Delta k$  error due to VCO nonlinearity could be tolerated as it impacts ADC transfer function mostly at the decision boundaries, whereas a DAC mismatch error shifts the entire transfer function segment (see Fig. 3). Second, averaging of  $\Delta k_i$  estimation errors [see Fig. 5(c)] reduces estimation error variance, and hence  $\tau_{\eta}$ , by  $N$  (19). Setting  $L = \sqrt{2}\Delta_{\varphi}$  minimizes  $\tau_{\eta}$  and  $\tau_{\beta}$ .

Fig. 7 shows two important aspects of our proposed calibration. First, it still works even if  $L = 0$ , i.e., the corresponding main and auxiliary quantizers thresholds are equal. This is attributed to quantizers noise that widens the detection window. In the case of  $L = 0$ , a narrow detection window still exists whose effective width is proportional to the quantizers RMS noise  $\sigma_{n1}$ . The calibration loop converges around 2–3 times slower for  $L = 0$  compared with optimum  $L$ . Notice that this behavior is not captured in (18) and (19) as noise was ignored. Second, the technique can tolerate large  $L$  variations due to PVT. This allows relying completely on random offsets and noise of the quantizers to generate the detection window as implemented in this paper. In this case,  $L$  distribution is half Gaussian. As long as the largest  $L$ , under some yield assumption, is less than  $6\Delta_{\varphi}$  (see Fig. 7), the time constants are limited by  $L = 0$  values. Therefore,

the implementation in this paper offers a simple and robust solution at the cost of slight deviation from the optimum convergence time. It is worth noting that convergence time could be optimized via  $L$  post silicon calibration or using alternative techniques that offer better control on  $L$  at the cost of higher design complexity. For instance, [19] exploits comparator metastability to perform the window detection function in the time domain. This also reduces the area penalty by replacing the auxiliary comparator by few logic gates. In this paper, a replica quantizer was employed to reduce design complexity and enable a short design cycle. As a final note, our proposed technique relies on input samples in the vicinity of the first-stage quantizer decision boundaries. Therefore, input signal PDF should cover these regions [18].

#### IV. CIRCUIT IMPLEMENTATION

A block and timing diagram of the 12-b prototype ADC is shown in Fig. 8. The first stage operates on 25% duty cycle nonoverlapped clocks  $\{\varphi_1, \varphi_{1b}\}$  and the second stage operates on 50% duty cycle nonoverlapped clocks  $\{\varphi_2, \varphi_{2b}\}$ . These phases are generated on-chip using an off-chip  $2f_s$  clock. The first-stage quantizers are implemented as 14-level flash. During  $\varphi_1$ , flash comparators are reset and

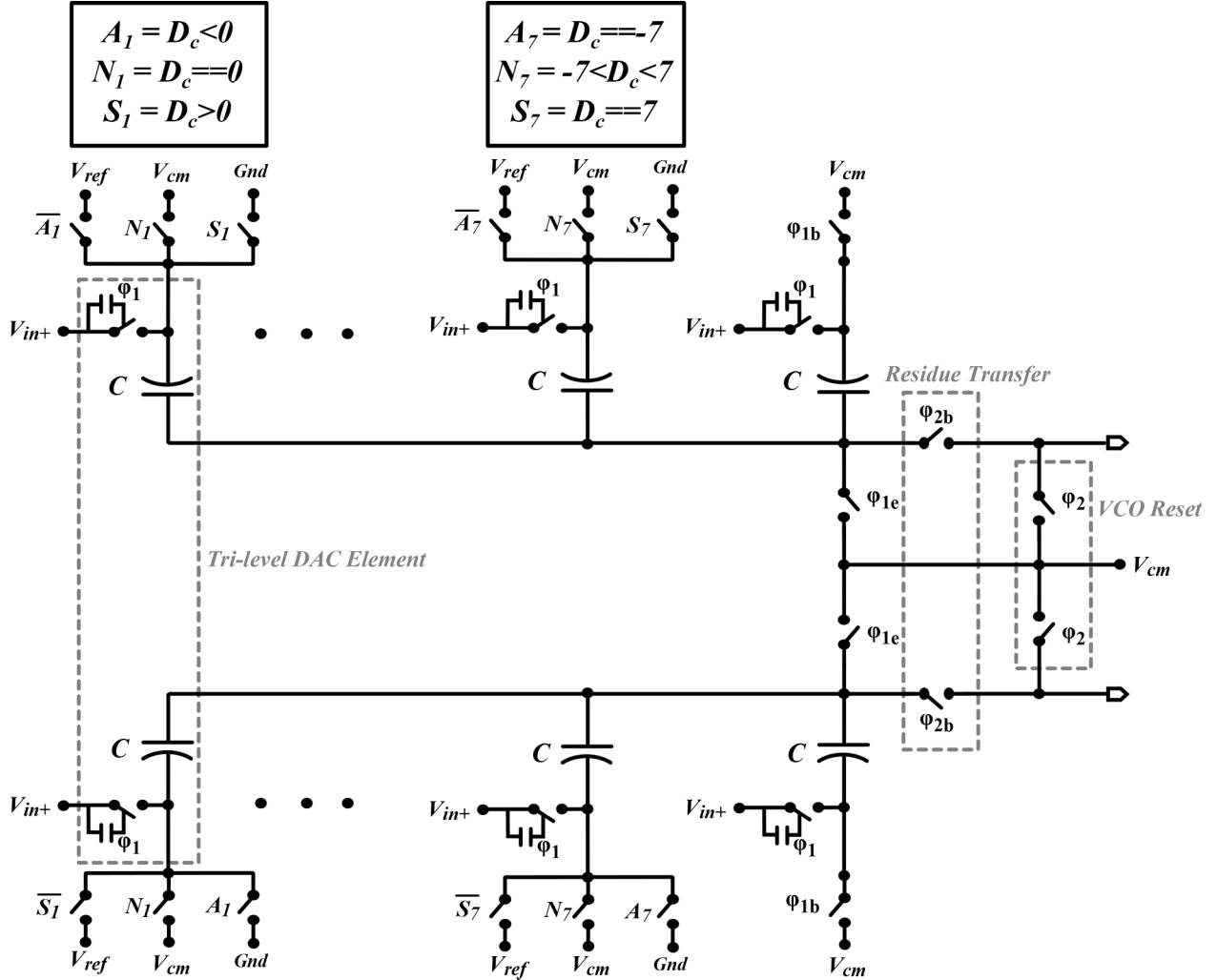


Fig. 9. Schematic of the differential CDAC, residue transfer switches, and VCO reset switches.

input is tracked. The differential input is bottom plate sampled on a thermometer capacitive DAC (CDAC) using early clock  $\varphi_{1e}$  falling edge. CDAC schematic is shown in Fig. 9. A 25-fF metal-insulator-metal (MIM) unit capacitor was used. CDAC is constructed using seven trilevel elements. The  $i^{\text{th}}$  CDAC trilevel element adds  $-V_{\text{ref}}/8$  if  $D_c \geq i$ ,  $+V_{\text{ref}}/8$  if  $D_c \leq -i$ , and zero if  $-i < D_c < i$ . This CDAC configuration ensures that CDAC mismatch error has odd symmetry for complementary codes, i.e.,  $k_{-i} = k_{+i} = \beta_i$  in the absence of VCO nonlinearity, and hence, any difference between  $k_{-i}$  and  $k_{+i}$  is attributed to VCO nonlinearity. On  $\varphi_{1b}$  rising edge, flash comparators are triggered, and the first-stage output is subtracted from the sampled input on CDAC. The generated residue is applied to the pseudodifferential VCO-based modulator on  $\varphi_{2b}$  rising edge. VCOs' frequencies change in proportion to the residue during  $\varphi_{2b}$  and are reset during  $\varphi_2$ . Each VCO phase is sampled on  $\varphi_2$  falling edge. Modulator outputs  $D_{\text{vco}}$  and  $D_{\text{vcon}}$  represent the quantized accumulated phase over one  $T_s$  and are proportional to the corresponding current-controlled oscillator (CCO) average frequency  $\bar{f}_{\text{CCOP}}$  and  $\bar{f}_{\text{CCON}}$  over one  $T_s$ . The combined modulator output  $D_{\text{vco,diff}}$  is proportional to the area enclosed between the VCO frequency red and blue waveforms in Fig. 8. Notice

that the accumulated phase is independent of VCO dynamics, e.g., step response time constant, as the accumulated phase during VCO reset compensates for the initial lag in phase accumulation during fine quantization due to finite VCO bandwidth. Therefore, to the first order, the total accumulated phase is independent of VCO dynamic response. In the presence of mismatch between the VCO step response time constant during fine quantization and reset phases, this introduces modulator gain error, if the time constant is independent of the applied residue, and weakly nonlinear error, if the time constant depends on the applied residue. As both VCO gain and dominant third-order nonlinearity are calibrated, the proposed architecture is not sensitive to VCO dynamic response.

#### A. First-Stage Coarse Quantizer

To enable VCO third-order nonlinear error estimation, flash threshold levels are placed asymmetrically. In contrast to [20], where performing dither correlation over the entire residue segment allows symmetric positive and negative thresholds, our proposed technique performs dither correlation only at the decision boundaries, which requires placing the coarse quantizer positive and negative threshold levels asymmetrically, as shown in Fig. 5(a), to enable  $\hat{\eta}$  estimation. Compared

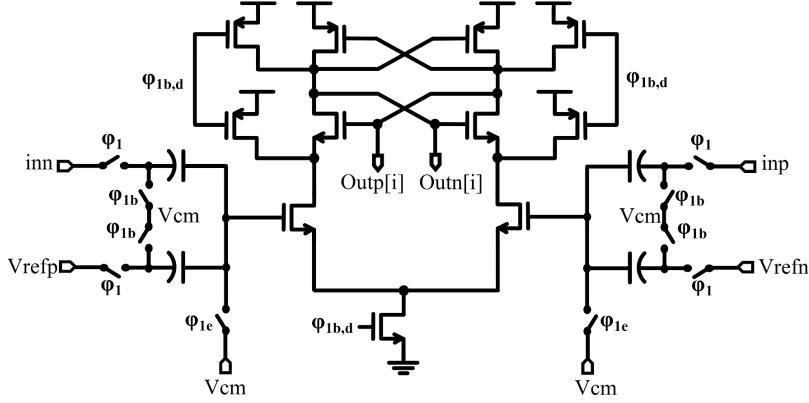


Fig. 10. Comparator schematic illustrating input and reference sampling.

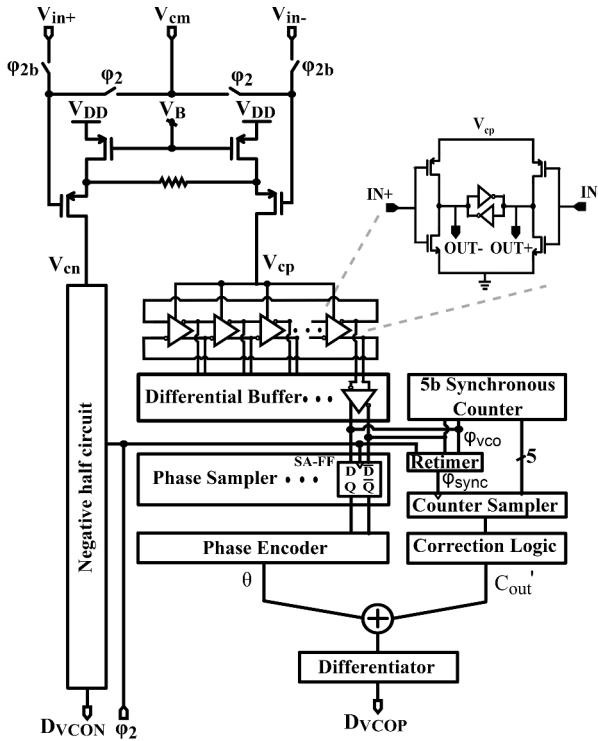


Fig. 11. Schematic of the VCO-based modulator.

with [20], performing the correlation over narrow input windows reduces estimation error, boosts convergence speed, and reduces the complexity and activity of the calibration unit, but places more requirements on the input signal statistics. The thresholds are initially placed at  $\{\pm 1, \pm 3, \pm 5, \pm 7, \pm 9, \pm 11, \pm 13\} V_{\text{ref}}/16$ . This provides redundancy to tolerate a maximum of  $V_{\text{ref}}/16$  variation for the coarse quantizer thresholds without overloading the second stage. In order to enable third-order nonlinearity error estimation, the positive thresholds are shifted to a lower level. Increasing the shift of the positive thresholds increases sensitivity to VCO nonlinearity, which reduces convergence time of the nonlinearity calibration loop; however, it reduces the threshold variation tolerance range. As a compromise, the positive thresholds are shifted by  $V_{\text{ref}}/32$  to  $\{1, 5, 9, 13, 17, 21, 25\} V_{\text{ref}}/32$ . Two  $24-k\Omega$  resistor ladders

generate the 14-level differential thresholds using an off-chip 1.8 V reference. Comparator schematic is shown in Fig. 10. The differential input and references are sampled on two custom 5-fF metal–oxide–metal (MOM) capacitors on  $\varphi_{1e}$  falling edge. Charges are redistributed on  $\varphi_{1b}$  rising edge, and next, the comparator is triggered on  $\varphi_{1b,d}$ , a delayed version of  $\varphi_{1b}$ . Comparators are sized, such that the window detection width  $L$  mean is approximately equal to  $\sqrt{2}\Delta_\theta$ . Comparator RMS input referred noise and offset are 1.3 and 7.5 mV, respectively. This corresponds to a window detection width mean and  $(3\sigma)$  maximum of 8.5 and 32 mV, respectively.

### B. VCO-Based Quantizer

Schematic of the VCO-based quantizer is shown in Fig. 11. A source degenerated PMOS pair converts the first-stage residue voltage to differential currents that control two 15-stage differential CCOs. Each CCO consumes  $145\ \mu\text{A}$ , and has a center frequency of 200 MHz and  $f_{\text{swing}}$  of 138 MHz corresponding to first-stage residue full swing of about  $190\ \text{mV}_{\text{pp}}$ . VCO phase noise is  $-108\ \text{dBc}/\sqrt{\text{Hz}}$  at 1-MHz offset, which translates to  $55\text{nV}/\sqrt{\text{Hz}}$  of input referred noise in addition to the  $40\text{-nV}/\sqrt{\text{Hz}}$  KT/C sampling noise. Thermal noise limited SNR is 81 dB over 2.5-MHz bandwidth.

Each of the CCO 15 phases is buffered differentially and sampled on a sense-amplifier-based flip-flop on  $\varphi_2$  falling edge. In addition, one of the CCO phases ( $\varphi_{\text{vco}}$ ) is fed to a JK-FF synchronous counter to keep track of CCOs phase overflow. This eliminates the need for center frequency calibration [1], [2] while enabling sample rate reconfiguration as in [1], [2], [10], and [13].  $D_{\text{vco}}$  is obtained by adding  $\theta$  and  $C'_{\text{out}}$ , where  $\theta$  is the VCO phase modulo  $2\pi$  and is captured using the VCO multiphase encoder [9], [10] (see Fig. 11), and  $C'_{\text{out}}$  is the number of whole  $2\pi$  cycles wrapped by the CCO and is captured by the synchronous counter. Schematic of the counter retiming and correction logic is shown in Fig. 12.  $\varphi_{\text{sync}}$  generator ensures that  $\varphi_{\text{sync}}$  rising edge arrives when counter output (*COUNT*) is valid. This is satisfied by generating  $\varphi_{\text{sync}}$  rising edge as a delayed version of the first  $\varphi_{\text{vco}}$  rising edge to arrive after  $\varphi_2$  goes low, as shown in Fig. 12. While this ensures proper timing, the captured *COUNT* ( $C_{\text{out}}$ ) would

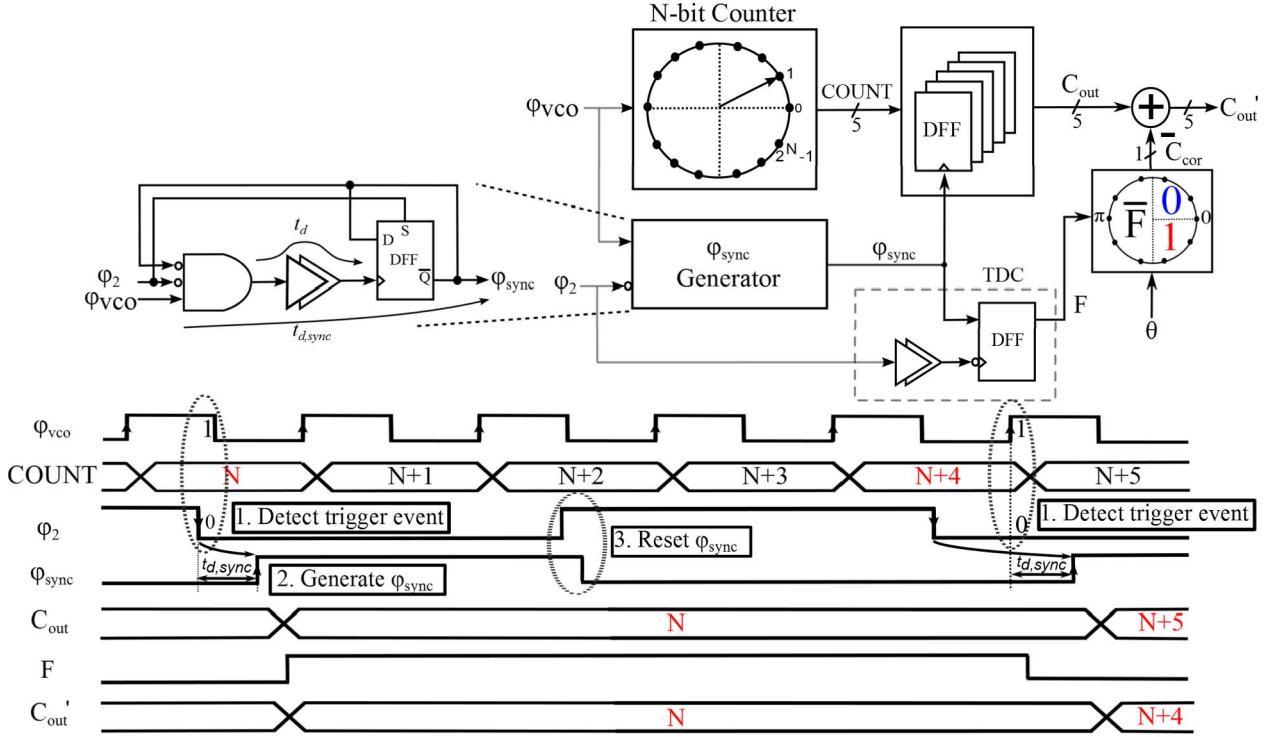


Fig. 12. Block diagram and timing of the synchronous counter illustrating retiming and correction logic.

be one more than the right count if  $\varphi_{vco}$  is low when  $\varphi_2$  rising edge arrives, i.e.,  $\pi < \theta < 2\pi$ . Therefore, a simple correction logic would be to subtract one from  $C_{out}$  whenever  $\pi < \theta < 2\pi$ . However, if  $\varphi_2$  rising edge arrives when  $\varphi_{vco}$  is close to  $\pi$ , there would be an ambiguity in  $C_{out}$ , e.g., due to clock skew. A flag  $F$  is generated to indicate the “extra count” event by checking  $\varphi_2$  to  $\varphi_{sync}$  delay. If an extra  $\varphi_{vco}$  edge is captured, this delay is greater than half nominal VCO period; otherwise, it is much smaller (equal to  $t_{d,sync}$ ), as shown in the timing diagram in Fig. 12. A 1-b time-to-digital converter is used to generate  $F$ . Whenever  $\theta$  is in the vicinity of  $\pi$ , i.e.,  $0.5\pi < \theta < 1.5\pi$ ,  $F$  is used for correction.

### C. Impact of VCO Mismatches

VCO mismatches have two main implications on the macrolevel. First, CCOs center frequencies are offset, which can be modeled by an input voltage offset, which if not excessively large would have no impact on calibration accuracy [3]. Second, the second-order nonlinearity coefficients do not cancel perfectly. In this section, we analyze the impact of these nonidealities.

First, let us assume that the two CCO tuning curves match perfectly except for an  $x$ -axis shift that represents an input referred offset  $V_{os}$ , e.g., due to  $V/I$  input pair threshold voltage mismatch. The differential output frequency  $\Delta f$  is given by

$$\Delta f(V_{in}) = f_p - f_n \cong f_{os} + k_{vco}V_{in} + 3\gamma V_{os}V_{in}^2 + \gamma V_{in}^3 \quad (20)$$

Notice that besides frequency offset  $f_{os}$ , the second-order nonlinearity term is generated through mixing of  $V_{in}$  and  $V_{os}$

via the third-order nonlinearity [21]. This term does not impact the stability of the nonlinearity calibration loop if it does not flip the error signal sign, i.e.,  $(k_{-i} - k_{+i})$ . This is guaranteed if  $V_{os}$  is smaller than  $V_{ref}/64$ , which is easily satisfied.<sup>3</sup> In addition, nonlinearity calibration accuracy is not impacted. Passing  $\Delta f$  through the digital nonlinearity correction block generates a second-order term, via mixing of  $f_{os}$  and the linear term  $2\pi k_{vco}V_{in}$ , that cancels the second-order term in (20). Intuitively, this term gets corrected along as it is also proportional to  $\gamma$ .

By contrast, second-order coefficient mismatches impact the accuracy of the nonlinearity calibration loop, and hence should be small by design. Let us assume that  $\Delta f$  is given by

$$\Delta f(V_{in}) = f_p - f_n \cong f_{os} + k_{vco}V_{in} + \alpha_{mis}V_{in}^2 + \gamma V_{in}^3 \quad (21)$$

where  $\alpha_{mis}$  is the second-order coefficient mismatch. It can be shown that the calibration loop converges to  $\hat{\eta}$  that satisfies<sup>4</sup>

$$\frac{3}{4}(\gamma - (2\pi k_{vco})^3 \hat{\eta}) \frac{V_{ref}}{16} = \alpha_{mis} \quad (22)$$

which can be reexpressed as

$$HD_{3,res} \left( \frac{V_{ref}}{16} \right) = \frac{2}{3} HD_2 \left( \frac{V_{ref}}{16} \right) \quad (23)$$

where  $HD_{3,res}$  is the residual VCO third-order harmonic distortion after calibration and  $HD_2$  is the second-order

<sup>3</sup>This can be derived by equating corresponding negative and positive decision boundary gaps and solving for the offset that causes their difference sign to flip.

<sup>4</sup>This condition can be obtained by solving for  $\hat{\eta}$  that equates the negative and positive decision boundary gaps.

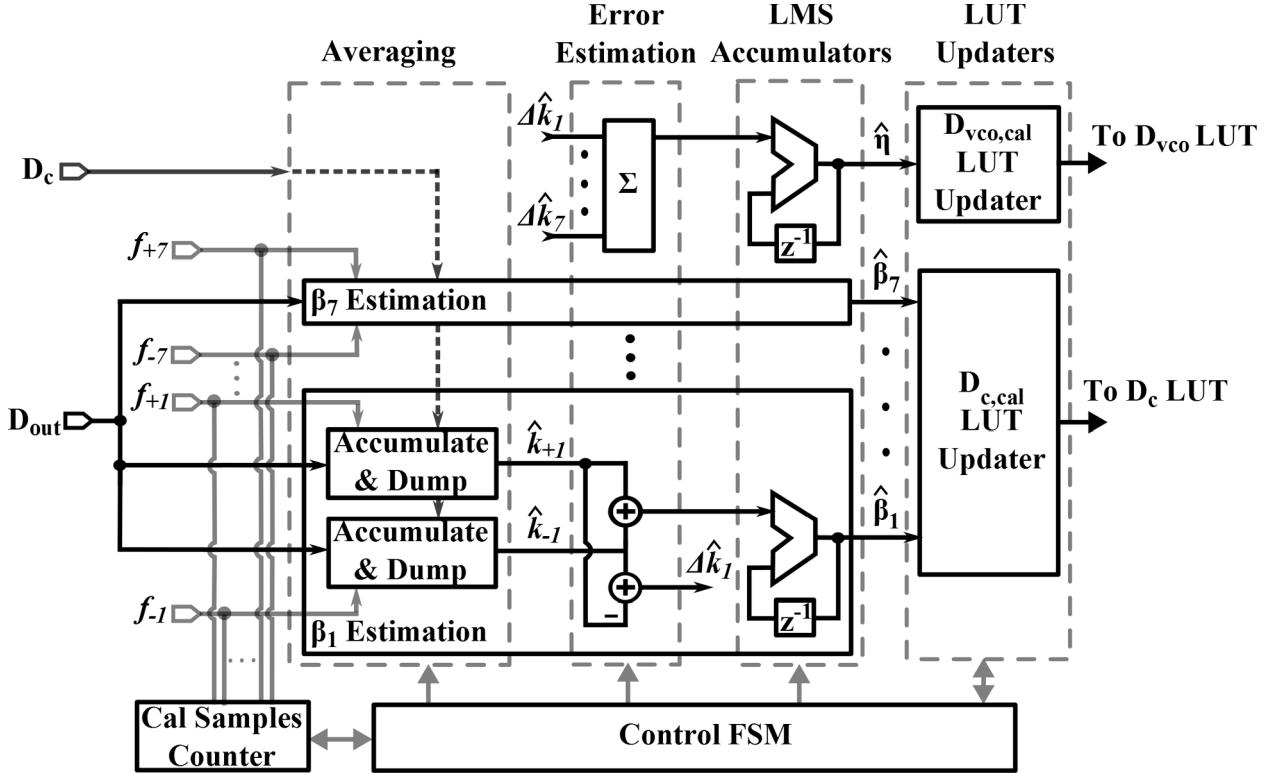


Fig. 13. Block diagram of the calibration unit.

harmonic distortion. Spectre Monte Carlo simulations (100 runs) show a worst case  $\text{HD}_2$  of  $-76$  dB. The corresponding ADC full swing THD and SFDR are better than  $-80$  and  $84$  dB, respectively, as obtained using MATLAB behavioral simulations. Our technique can be extended to calibrate the second-order nonlinearity by setting some of the positive flash thresholds to be larger in magnitude than the corresponding negative thresholds, e.g., placing positive thresholds at  $mV_{\text{ref}}/32$  and  $m \in \{1, 7, 9, 15, 17, 23, 25\}$ . This enables differentiating the second- and third-order nonlinearity errors in the background calibration loop.

#### D. Calibration Unit

A high-level diagram of the calibration unit is shown in Fig. 13. It consists of seven identical slices for  $\hat{\beta}_{1\sim 7}$  estimation and one slice for  $\hat{\eta}$ . For each calibration cycle, calibration samples are accumulated until a specified number, indicated by the Cal Samples counter, is collected. For each flag  $f_{\pm i}$ , calibration samples are sorted into two sets, based on  $D_c$ , corresponding to boundary gap upper and lower edges, and are used to estimate  $\hat{k}_{\pm i}$ . Error signals are then estimated using the sum and differences of  $\hat{k}_{\pm i}$  and used to update each of the LMS accumulators. Finally, the LUTs are updated using  $\hat{\beta}_{1\sim 7}$  and  $\hat{\eta}$ .

#### V. MEASUREMENT RESULTS

The prototype ADC was implemented in 180-nm CMOS and occupies an active area of  $0.22 \text{ mm}^2$  excluding the digital differentiator, output adder, and the calibration unit,

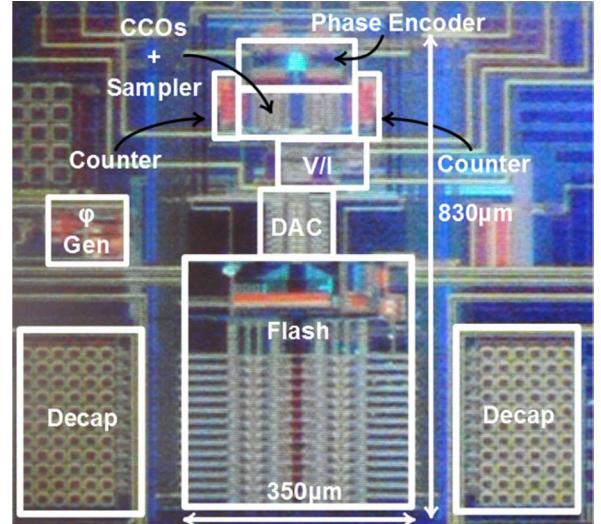


Fig. 14. Die photo.

which were implemented off-chip, as indicated in Fig. 8. ADC output is captured using a logic analyzer and transferred to MATLAB. Die photo is shown in Fig. 14. The ADC consumes  $4.8$  mW from  $1.8$  V supply while operating at  $51.2$  MS/s, out of which only  $24\%$  is analog. Power is divided into  $4$  mW for the on-chip ADC core and  $0.8$  mW for the off-chip digital backend (estimated using digital synthesis) that is consumed mainly by the LUTs, digital differentiator, and output adder. The calibration unit consumes negligible power given its low rate operation. Cal Samples was set

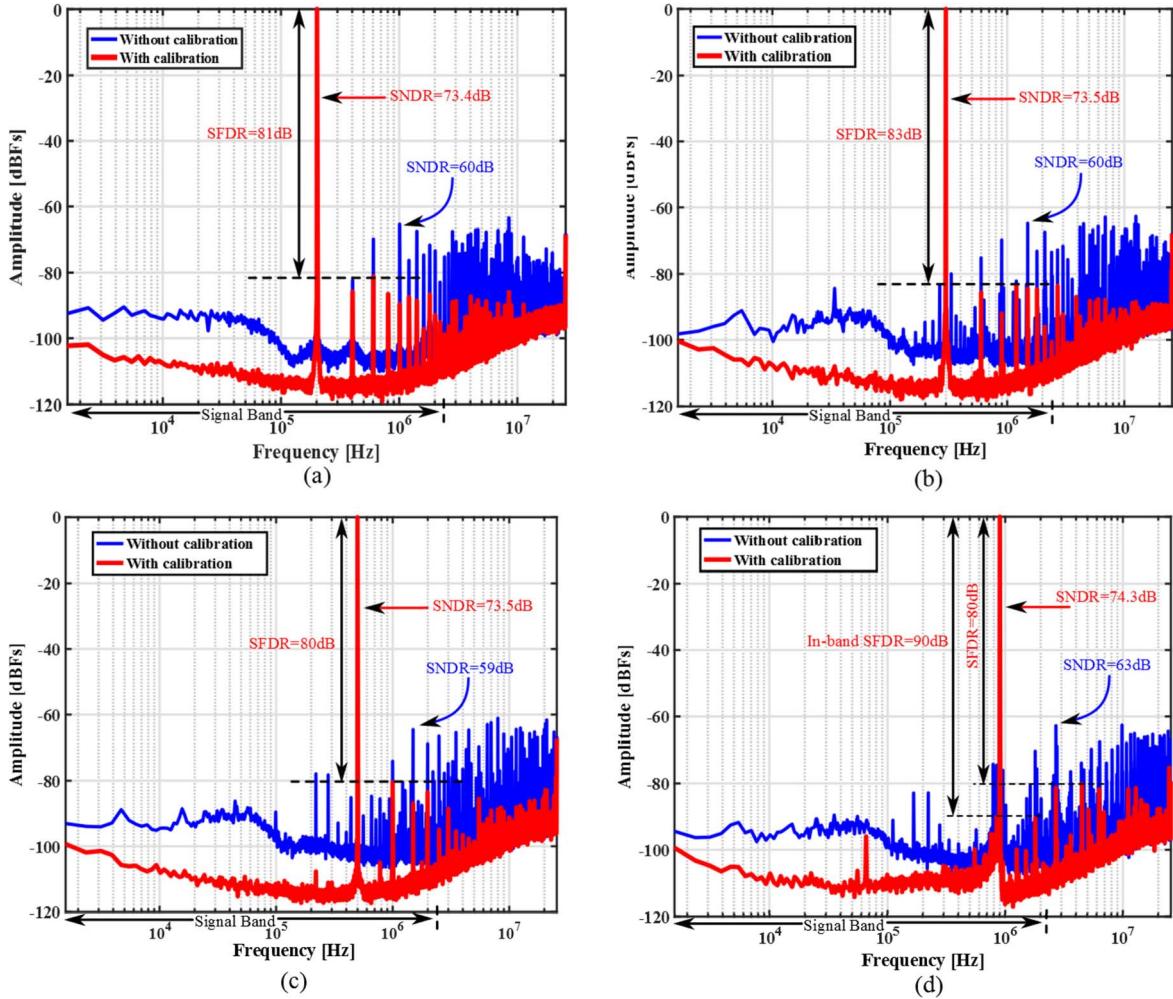


Fig. 15. Measured ADC output power spectral density for (a) 200 kHz, (b) 300-kHz input, (c) 500 kHz, and (d) 900-kHz sinusoidal input.

to 10k samples per calibration cycle. This corresponded to a short calibration cycle of 4 ms (200k full rate samples) for a sinusoidal input. This enables fast tracking response while maintaining a low activity factor for the low-rate LUT updaters. Fig. 15(a) shows output PSD for a 200-kHz 3.6 V<sub>pp</sub> input signal. Background calibration improves SNDR from 60 to 73.4 dB in 2.5-MHz signal band and SFDR from 66 to 81 dB.

The tone at  $f_s/2$  is attributed to coupling of an  $f_s/2$  data capture clock that is generated on-chip and sent along with the ADC output to the logic analyzer. As this tone is not intrinsic to the proposed architecture, is independent of the input signal, and is filtered by the decimation filter, it is not accounted for in SNDR/SFDR calculation. Output PSD for 300-kHz, 500-kHz, and 900-kHz input tones is shown in Fig. 15(b)–(d), respectively. The ADC maintains excellent linearity across the input band. For the 900-kHz input, the third harmonic lies out of band. Fig. 15(d) reports SFDR both in-band and up to  $f_s/2$ . After calibration, distortion tones are limited by residual errors due to higher order nonidealities that are not accounted for in the analyzed model, e.g., T/H nonlinearity, incomplete cancelation of VCO second-order nonlinearity due to mismatches, and higher order VCO nonlinearities.

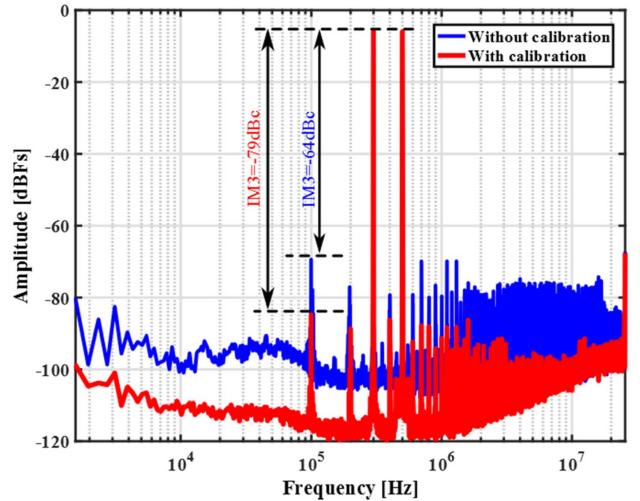


Fig. 16. Measured ADC output power spectral density with two tone input at 300 and 500 kHz.

Fig. 16 shows ADC output PSD with two tone input at 300 and 500 kHz. IM3 is reduced from  $-64$  to  $-79$  dBc after background calibration. Measured SNDR and SNR maintain linear increase with input amplitude up to full-scale swing,

TABLE II  
PERFORMANCE SUMMARY AND COMPARISON TO PRIOR VCO-BASED  $\Sigma\Delta$  MODULATORS

	[2]	[3]	[6]	[7]	[8]	[11]	[13]	This Work
Technology (nm)	65	90	90	65	65	40	65	<b>180</b>
$F_s$ (MHz)	2400	640	600	1200	1280	1600	1000	<b>51.2</b>
Bandwidth (MHz)	37.5	5	10	50	50	40	30	<b>2.5</b>
SNDR (dB)	70	73.9	78	71.5	64	59.5	65	<b>73.4</b>
Power (mW)	39	4.1	16	54	38	2.57	8.2	<b>4.8</b>
FoM1 <sup>*</sup> (fJ/conv-step)	196	101	120	176	294	42	94	<b>244</b>
FoM2 <sup>**</sup> (dB)	160	165	166	161	158	164	161	<b>161</b>
Area (mm <sup>2</sup> )	0.08	0.16	0.41	0.5	0.49	0.017	0.62	<b>0.22***</b>

\*  $FoM1 = \frac{Power}{2BW \times 2ENOB}$

\*\*  $FoM2 = SNDR + 10\log\left(\frac{BW}{Power}\right)$

\*\*\* Excludes area of the off-chip digital backend and calibration unit.

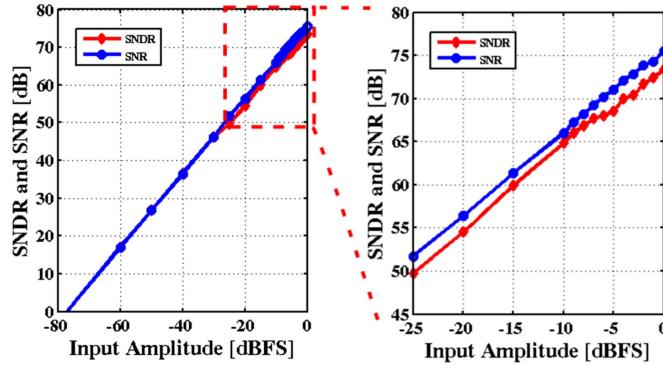


Fig. 17. Measured SNR and SNDR versus input amplitude.

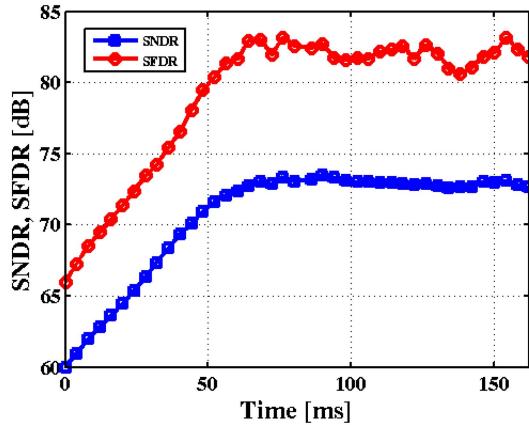


Fig. 18. Measured SNDR/SFDR learning curve.

as shown in Fig. 17. Fig. 18 shows the learning curve of ADC SNDR/SFDR. A tradeoff exists between convergence time and steady state SNDR/SFDR fluctuation. In this prototype, in order to reduce convergence time, the largest LMS  $\mu$  parameters that meet a target SFDR of 80 dB were selected. Startup convergence time is 64 ms corresponding to 16 calibration cycles. Measured learning curves for  $\hat{\beta}_i$  and  $\hat{\eta}$  are shown in Fig. 19.

Table II summarizes the prototype performance and compares it to state-of-the-art VCO-based  $\Sigma\Delta$  ADCs. The ADC achieves a figure-of-merit (FoM) that is in-line with the state-of-the-art despite the relatively old 180-nm process. As the proposed architecture is mostly digital and minimally modifies the 0-1 MASH architecture, which demonstrates good FoM in fine-line CMOS technologies [11], [13], its FoM and

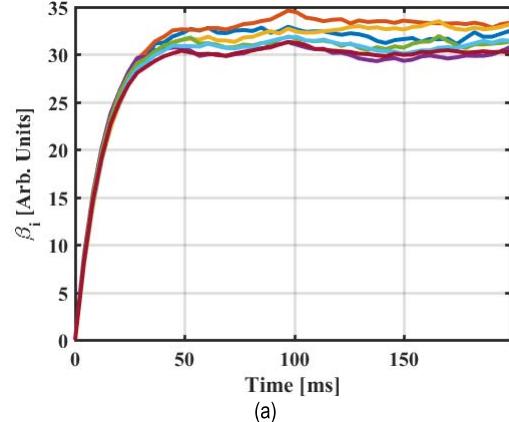


Fig. 19. Measured learning curve for (a)  $\hat{\beta}_i$  and (b)  $\hat{\eta}$ .

convergence time are expected to significantly improve if implemented in a more advanced technology node.

## VI. CONCLUSION

An LMS-based direct background calibration technique for correcting CDAC mismatches, VCO linear gain drift, and V-to-F nonlinearity in VCO-based 0-1 MASH  $\Sigma\Delta$  ADCs is proposed. Processing samples falling inside narrow detection windows at the coarse quantizer decision boundaries enables fast error estimation. The proposed architecture minimally modifies the basic VCO-based 0-1 MASH architecture by replicating the coarse quantizer. The reported prototype is first to demonstrate fast direct background VCO nonlinearity calibration.

## REFERENCES

- [1] G. Taylor and I. Galton, "A mostly-digital variable-rate continuous-time delta-sigma modulator ADC," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2634–2646, Dec. 2010.
- [2] G. Taylor and I. Galton, "A reconfigurable mostly-digital delta-sigma ADC with a worst-case FOM of 160 dB," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 983–995, Apr. 2013.
- [3] S. Rao, K. Reddy, B. Young, and P. K. Hanumolu, "A deterministic digital background calibration technique for VCO-Based ADCs," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 950–960, Apr. 2014.
- [4] M. Z. Straayer and M. H. Perrott, "A 12-bit, 10-MHz bandwidth, continuous-time  $\Sigma\Delta$  ADC with a 5-bit, 950-MS/s VCO-based quantizer," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 805–814, Apr. 2008.
- [5] M. Park and M. H. Perrott, "A 78 dB SNDR 87 mW 20 MHz bandwidth continuous-time  $\Delta\Sigma$  ADC with VCO-based integrator and quantizer implemented in 0.13  $\mu\text{m}$  CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3344–3358, Dec. 2009.
- [6] K. Reddy *et al.*, "A 16-mW 78-dB SNDR 10-MHz BW CT  $\Delta\Sigma$  ADC using residue-cancelling VCO-based quantizer," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2916–2927, Dec. 2012.
- [7] K. Reddy, S. Dey, S. Rao, B. Young, P. Prabha, and P. K. Hanumolu, "A 54mW 1.2GS/s 71.5dB SNDR 50MHz BW VCO-based CT  $\Delta\Sigma$  ADC using dual phase/frequency feedback in 65nm CMOS," in *IEEE Symp. VLSI Circuits Dig.*, Jun. 2015, pp. C256–C257.
- [8] B. Young, K. Reddy, S. Rao, A. Elshazly, T. Anand, and P. K. Hanumolu, "A 75dB DR 50MHz BW 3<sup>rd</sup> order CT- $\Delta\Sigma$  modulator using VCO-based integrators," in *IEEE Symp. VLSI Circuits Dig.*, Jun. 2014, pp. 1–2.
- [9] S. Rao, B. Young, A. Elshazly, W. Yin, N. Sasidhar, and P. K. Hanumolu, "A 71dB SFDR open loop VCO-based ADC using 2-level PWM modulation," in *IEEE Symp. VLSI Circuits Dig.*, Jun. 2011, pp. 270–271.
- [10] A. Sanyal, K. Ragab, L. Chen, T. R. Viswanathan, S. Yan, and N. Sun, "A hybrid SAR-VCO delta-sigma ADC with first-order noise shaping," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2014, pp. 1–4.
- [11] X. Xing and G. G. E. Gielen, "A 42 fJ/step-FoM two-step VCO-based delta-sigma ADC in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 714–723, Mar. 2015.
- [12] P. Zhu, X. Xing, and G. Gielen, "A 40MHz-BW 35fJ/step-FoM nonlinearity-cancelling two-step ADC with dual-input VCO-based quantizer," in *Proc. 40th Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2014, pp. 63–66.
- [13] A. Ghosh and S. Pamarti, "Linearization through dithering: A 50 MHz bandwidth, 10-b ENOB, 8.2 mW VCO-based ADC," *IEEE J. Solid-State Circuits*, vol. 50, no. 9, pp. 2012–2024, Sep. 2015.
- [14] K. Ragab and N. Sun, "A 12b ENOB, 2.5MHz-BW, 4.8mW VCO-based 0–1 MASH ADC with direct digital background nonlinearity calibration," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2015, pp. 1–4.
- [15] B. Drost, M. Talegaonkar, and P. K. Hanumolu, "Analog filter design using ring oscillator integrators," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3120–3129, Dec. 2012.
- [16] J. A. McNeill, R. Majidi, and J. Gong, "Split ADC' background linearization of VCO-based ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 1, pp. 49–58, Jan. 2015.
- [17] L. Brooks and H. S. Lee, "Background calibration of pipelined ADCs via decision boundary gap estimation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 10, pp. 2969–2979, Nov. 2008.
- [18] N. Sun, "Exploiting process variation and noise in comparators to calibrate interstage gain nonlinearity in pipelined ADC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 4, pp. 685–695, Apr. 2012.
- [19] K. Ragab, L. Chen, A. Sanyal, and N. Sun, "Digital background calibration for pipelined ADCs based on comparator decision time quantization," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 5, pp. 456–460, May 2015.
- [20] J. P. Keane, P. J. Hurst, and S. H. Lewis, "Background interstage gain calibration technique for pipelined ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 1, pp. 32–43, Jan. 2005.
- [21] A. A. Abidi, "General relations between IP2, IP3, and offsets in differential circuits and the effects of feedback," *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 5, pp. 1610–1612, May 2003.



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