A Class-G Voltage-Mode Doherty Power Amplifier

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***Abstract*— This paper presents the combination of two back-off efficiency enhancement techniques, the voltage-mode Doherty and the class-G switched-capacitor power amplifier (PA), to achieve efficiency peaking at both 6 and 12 dB back off without introducing the mode-switching glitches present in previous architectures. The proposed technique enables transmission of high peak-to-average-power ratio (PAPR) signals with high efficiency while maintaining excellent linearity. The PA is fabricated in 45-nm CMOS SOI with integrated balun for power combining and matching. At 3.5 GHz a saturated output power of 25.3 dBm is measured with 30.4%/25.3%/17.4% power added efficiency (PAE) at 0/6/12 dB back off. With memoryless, non-adaptive linearization, the PA achieves 19.2% PAE with −35.8 dB error vector magnitude (EVM) while transmitting a 40 MHz 256-QAM 10.1 dB PAPR 802.11ac modulation. Significant efficiency improvement compared to class-B and EVM better than −34 dB is maintained over more than 1 GHz bandwidth.**

***Index Terms*— Broadband, class-G (CG), CMOS integrated circuits, Doherty power amplifier (PA), linearity, polar modulation.**

I. Introduction

SINCE its invention in 1936, the Doherty power amplifier has seen widespread use to enhance efficiency in broadcast and communication systems transmitting signals with time-varying amplitude [1]. To achieve high spectral efficiency, many recent communications standards have adopted signals with high peak-to-average-power ratio (PAPR) modulation [2]. These high PAPR signals have again brought Doherty and other high back-off efficiency power amplifier (PA) architectures to the forefront [1]. At the same time, these modern digital modulation formats bring the additional demand of high linearity due to their tightly packed symbols. For example, an error vector magnitude (EVM) better than −35 dB is required for 1024-QAM OFDM modulation, a format that will be used in the upcoming 802.11ax standard.

A variety of techniques, such as Doherty [3], Outphasing [4], and Class-G [5], [6] (discrete supply switching), have been shown to greatly improve PA back-off efficiency to about 6 dB back off [Fig. 1(a)]. However, as PAPR continues to increase beyond 6 dB, this hard-earned efficiency enhancement gives only a minor improvement in average power added efficiency (PAE). To address this issue, a wide variety of extensions to the aforementioned techniques have been proposed, yet most suffer from a significant performance tradeoff. One such example, often referred to as extended Doherty [7], increases the impedance inverter characteristic impedance, as well as the size of the peaking amplifier, to realize an efficiency peak at deeper back off. Unfortunately the increased characteristic impedance leads to a higher impedance transformation ratio, increasing loss and limiting bandwidth. Extensions of other techniques [8], [9] giving efficiency peaks at 9–12 dB back off typically share similar tradeoffs between efficiency, bandwidth, linearity, and design complexity. Alternatively, combinations of different efficiency enhancement techniques can be applied to overcome the tradeoffs inherent to a single architecture at deep back off and achieve high efficiency, bandwidth, and linearity in a low-complexity design. In this paper, we combine the recently developed voltage-mode Doherty (VMD) [10] with the class-G switched-capacitor power amplifier (CG-SCPA) [6] for efficiency peaking at both 6 and 12 dB back off [Fig. 1(b)].

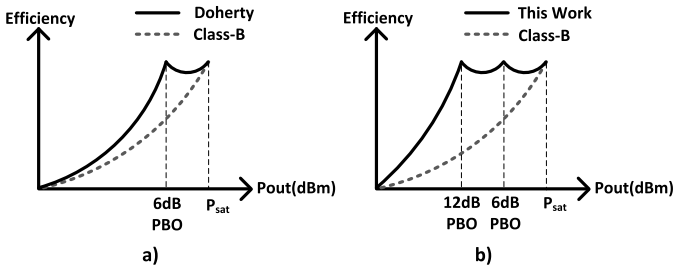

Fig. 1. Ideal efficiency of (a) conventional Doherty PA and (b) this work versus ouput power.

II. Previous Architectures

Combinations of efficiency enhancement techniques from Doherty with CG [11], Outphasing with multi-level CG [12], and Outphasing with power combined transformer [13], have been demonstrated to achieve efficiency enhancement beyond 6 dB back off. However, these techniques often suffer from a mode-switching glitch which can be characterized as a sudden change in system configuration such as power supply voltage, impedance level, or discontinuity of the input signal amplitude/phase at critical power levels, usually where efficiency peaks.

As a representative example of a combined architecture, the classical Doherty PA can be used with discrete power supply switching (CG) [11], as shown in Fig. 2. From 0 to 6 dB back off, the PA operates like the classical Doherty PA [3] providing efficiency peaking at 6 dB back off. To achieve additional efficiency peaking at 12 dB back off, mode switching is used. The power supply is switched from Vdd to Vdd/2, and the input drive is also changed such that both the main

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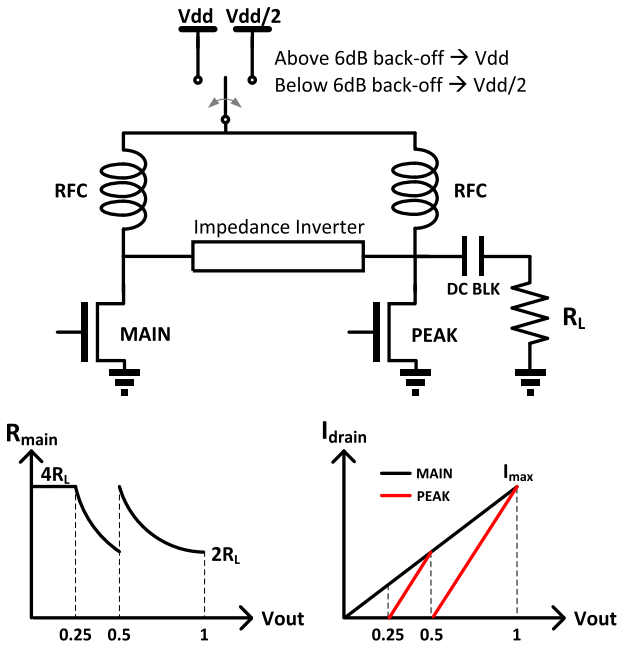

Fig. 2. Class-G (CG) conventional Doherty with a power switch added in the power supply path allowing switching between Vdd and Vdd/2 at 6 dB back off. A discontinuity in main PA impedance and peak PA current is seen at 6 dB back off.

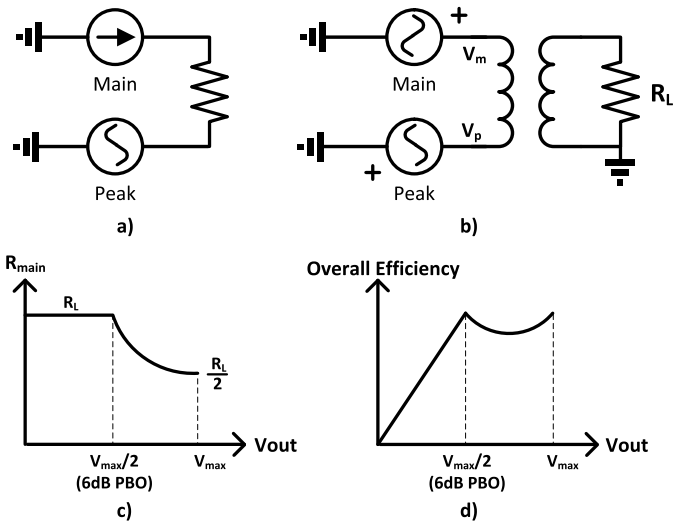

Fig. 3. (a) Current–voltage Doherty topology. (b) VMD. (c) Main PA impedance trajectory. (d) Overall efficiency of VMD.

and peaking PAs deliver the same power to the load. After the mode switch, the PA operate as classical Doherty PA but at half supply, resulting in a second efficiency peak at 12 dB back off, 6 dB from halving the supply, 6 dB from Doherty operation.

Though this technique achieves high efficiency at 12 dB back off, it has several drawbacks. First, the power supply switching at 6 dB back-off causes the glitch in the signal envelope [14] and significant power supply ringing [12] which distorts the PA output. Moreover, the step change in power supply also introduces a large jump in the AM–PM characteristics [11] due to non-linear drain capacitance. This effect is difficult to correct with pre-distortion as it significantly increases the bandwidth requirement of the pre-distorted signal. Second, the transistor used to implement the power supply switch must be very large in order to achieve the low on-resistance required to maintain high efficiency. This makes it difficult to precisely control the timing of power supply switching and usually limited its use to power control application [15]. In dynamic power supply modulation [11], the timing must be synchronized with the PA input signal. This restricts the maximum modulation bandwidth of the technique and significantly increases design complexity.

Several techniques have been proposed to mitigate the mode-switching glitch. One notable technique, as shown in [13], skips a transition to the low-power mode if two or more mode transitions would be required within a predefined time interval. It is shown in [13] that increasing the skipping time interval reduces distortion adjacent channel power ratio (ACPR) of the transmitted signal. Unfortunately, the loss of efficiency enhancement when more mode transitions are skipped leads to a reduced average efficiency. As the modulation bandwidth increases the number of skipped transitions required to maintain the same distortion level increases proportionally, severely limiting overall efficiency enhancement.

The described problems associated with mode-switching glitches makes it desirable to find techniques which leverage the efficiency benefit of multiple power supplies, yet do not require instantaneous reconfiguration of the entire PA. This would allow for improved efficiency beyond 6 dB back off without the large, sudden changes associated with mode switching.

III. Proposed Architecture

In this paper, the VMD and CG-SCPA architectures are combined for efficiency peaking at both 6 and 12 dB back off. The architecture is termed CG-VMD. First, the VMD and CG-SCPA architectures, each of which provides 6 dB efficiency peaking, will be discussed, and then the use of the two techniques in concert to form the CG-VMD will be introduced.

A. Voltage-Mode Doherty

VMD is a modification of the current–voltage Doherty [Fig. 3(a)] used by Doherty as a starting point for the derivation of the classic Doherty PA [3]. In the current–voltage Doherty architecture, the peaking PA (voltage source) modulates the load impedance of the main PA (current source) such that higher impedance is presented at lower power resulting in efficiency peaking at 6 dB back off. The advantage of this topology is that it does not require a narrowband impedance inverter [16] to achieve load modulation, enabling wide bandwidth. In VMD, the main PA is replaced with a voltage source, without changing the load modulation property of the main PA, and the floating load is replaced with a balun driving a single-ended load [Fig. 3(b)]. It can be shown that the impedance seen by the main PA is given by $R_m = R_L/(1+V_p/V_m)$, where V_m and V_p are the main and peaking amplifier voltages, respectively [10]. The operation from zero power to full power is as follows: the main PA turns on first and its voltage increases until the main PA saturates

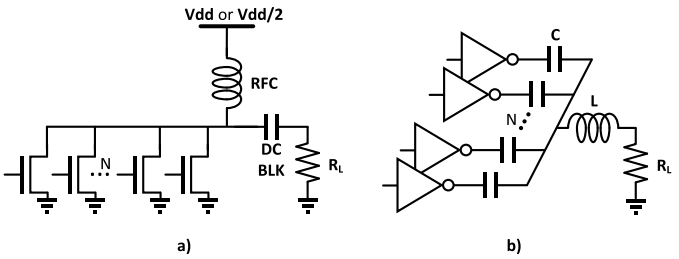

Fig. 4. (a) Conventional CG RF-DAC. (b) SCPA.

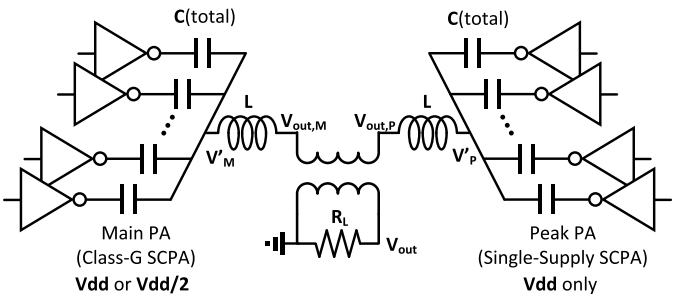

Fig. 5. CG-VMD. The unit cells in the main PA can independently operate at either full supply or half supply.

at 6 dB back off, then the peaking PA voltage increases until it also reaches saturation. This results in the main PA impedance profile of Fig. 3(c), and efficiency peaking at 6 dB back off [Fig. 3(d)]. Note that there is no additional switch [17] required to short the peaking PA at low power since it is a voltage source and thus itself provides a short when turned off. The high-efficiency voltage sources in the VMD are realized with switched-capacitor PAs [18] (SCPA) which provide high efficiency, linearity, and dynamic range, at gigahertz frequencies.

For wideband, high-efficiency operation, the VMD takes advantage of primary load modulation [10], [15] to completely utilize the transformer structure at all power levels. To implement the VMD alone with peaking at 12 dB back off, four transformers would need to be stacked and secondary load modulation must be used [19]. This results in low efficiency and narrow bandwidth when the PA operates at 12 dB back off.

B. Class-G Switched-Capacitor PA

Conventional CG PAs have the drawback of a mode-switching glitch [14]. This is because there is a single power supply for the entire PA [Fig. 4(a)]. At low power, the PA operates in half-supply mode, reaching saturation at about 6 dB back off. To further increase output power to the load, the power supply must be switched to full supply. Though the AM–AM distortion from supply switching can be corrected in steady state, this correction is sensitive to PVT variations. Additionally correcting the static AM–AM does not remove potential AM–PM discontinuities [11]. Even with a static correction, when the supply transitions, the voltage at the drain of the transistor cannot change instantaneously causing a brief AM–AM and AM–PM error which can be greater than an LSB, a so called "glitch." This glitch can be modeled as a short absence of signal which causes degradation in EVM, ACPR, and noise floor [14]. Since the frequency of supply transitions increase with modulation bandwidth, power supply switching glitches limit the usefulness of conventional CG techniques to narrowband modulation. By contrast, in an SCPA all unit cells are ac-coupled to the output [Fig. 4(b)], allowing individual unit cells to operate from different power supplies. This flexibility gives glitch-free CG operation [6]. At low power, all unit cells operate in half-supply mode until saturation is reached. To further increase the output power, unit cells operating at half supply can transition to full supply one-by-one without introducing a significant glitch in the PA output. The supply switching glitch in a CG-SCPA is that of a single unit cell; as the resolution of the CG-SCPA increases, the supply switching glitch becomes arbitrarily small.

To extend the CG-SCPA concept to 12 dB back off, unit cells would need to be capable of operating at full-, half-, and quarter-supply, significantly increasing unit cell design complexity and resulting in poor overall efficiency.

C. Class-G Voltage-Mode Doherty

The CG-VMD [20] is composed of a CG-SCPA used for the main PA and an SCPA for the peaking, operating across a transformer (Fig. 5). As shown in Fig. 6, at full power, the main and peaking PAs drive the transformer in anti-phase at full amplitude with a 25 Ω impedance seen by each PA. From full power to 6 dB back off, the peaking PA unit cells start to turn off, reducing the output amplitude, and increasing the impedance seen by the main PA until it reaches 50 Ω. At 6 dB back off the peaking PA is completely off and the main PA operates in saturation from full supply, providing efficiency peaking [10]. From 6 to 12 dB back off, the main PA unit cells transition one-by-one from full supply to half supply, gradually decreasing the main PA amplitude until all unit cells operate at half supply. With high-impedance (50 Ω) load and half supply for the main PA, efficiency peaking at 12 dB back off is achieved. The unit cell turn-on sequence for a CG-VMD with four unary-weighted unit cells in both the main and peaking amplifier is summarized in Fig. 7. As shown, only one unit cell changes state at a time, reducing jumps in power supply or impedance to a single unit cell step. Moreover, once the unit cell turn-on sequence is chosen, the operation of CG-VMD is as simple as that of a standard RF-DAC [21], with no additional synchronized mode-switching path needed [11], [17].

IV. Detailed Analysis

In as much as a variety of non-idealities will inevitably degrade back-off efficiency, the CG-VMD PA will be analyzed considering all relevant loss mechanisms. We will first assume ideal transistors and matching network to demonstrate the CG-VMD principle and its inherent capacitive divider losses. Then non-idealities of the totem-pole driver and output matching network will be included to show the design tradeoffs at gigahertz frequencies.

A. Class-G Voltage-Mode Doherty With Ideal Components

The loss of the CG-VMD comes primarily from the charging-and-discharging of the capacitive divider banks of

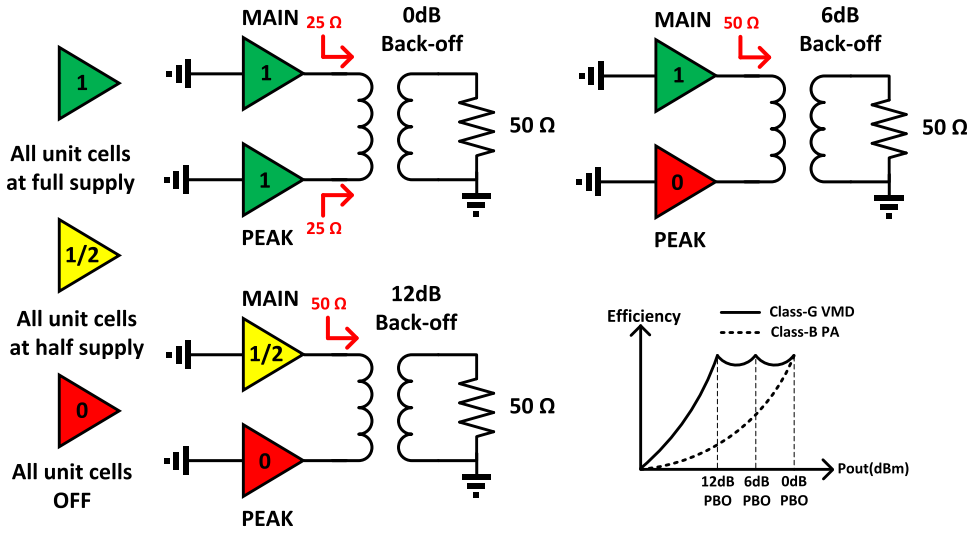

Fig. 6. CG-VMD operation at different efficiency peaking points. At 6 dB back off, VMD gives efficiency peaking. At 12 dB back off, a combination of VMD and CG-SCPA provide the peaking.

Vout	Back Off (dB)	CG-SCPA (Main)				SCPA (Peak)			
0	OFF	0	0	0	0	0	0	0	0
1/16	24	.5	0	0	0	0	0	0	0
2/16	18	.5	.5	0	0	0	0	0	0
3/16	15	.5	.5	.5	0	0	0	0	0
4/16	12	.5	.5	.5	.5	0	0	0	0
5/16	10	1	.5	.5	.5	0	0	0	0
6/16	9	1	1	.5	.5	0	0	0	0
7/16	7	1	1	1	.5	0	0	0	0
8/16	6	1	1	1	1	0	0	0	0
10/16	4.1	1	1	1	1	1	0	0	0
12/16	2.5	1	1	1	1	1	1	0	0
14/16	1.2	1	1	1	1	1	1	1	0
16/16	0	1	1	1	1	1	1	1	1

0 Off

0.5 Half Supply

1 Full Supply

Fig. 7. Unit cell turn-on sequence of CG-VMD.

the main and peaking PAs which occurs at the rising and falling edges of the RF input signal. We will first calculate the capacitive divider loss of the CG-SCPA and then generalize it to the CG-VMD.

1) Capacitive Divider Loss of CG-SCPA: Assuming fast rising/falling edges at the driver output, the inductors in the CG-SCPA matching network will act as open circuits at voltage transitions [18]. The equivalent circuit of the main PA (CG-SCPA) can be simplified, as shown in Fig. 8, where the unit cells are lumped into three groups: switching at full supply, switching at half supply, and off. If n_F and n_H are the fraction of unit cells operating at full- and half-supply, respectively, by the capacitive divider principle, the voltage swing at V' can be written as

$$V' = V_{\rm dd}n_F + 0.5V_{\rm dd}n_H = (n_F + 0.5n_H)V_{\rm dd}. \quad (1)$$

At the rising edge, the amount of charge taken from full- and half-supplies is

$$Q_F = n_F C(V_{\rm dd} - V') = n_F C V_{\rm dd}(1 - n_F - 0.5n_H) \quad (2)$$

$$Q_H = n_H C(0.5V_{\rm dd} - V') = n_H C V_{\rm dd}(0.5 - n_F - 0.5n_H) \quad (3)$$

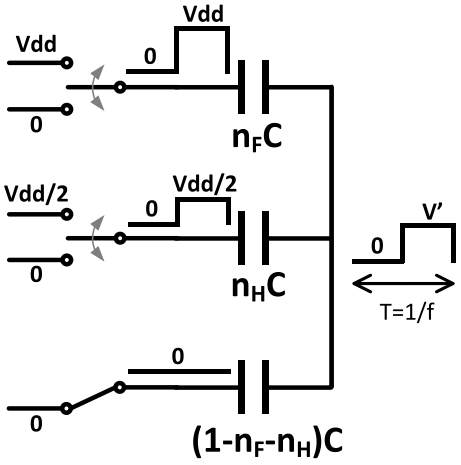

Fig. 8. CG-SCPA equivalent circuit for capacitive divider loss analysis.

and with RF carrier frequency f, the power dissipation due to the capacitive divider is

$$P_{\rm cd} = [n_F(1 - n_F) + 0.25n_H(1 - n_H) - n_F n_H]\, C V_{\rm dd}^2 f. \quad (4)$$

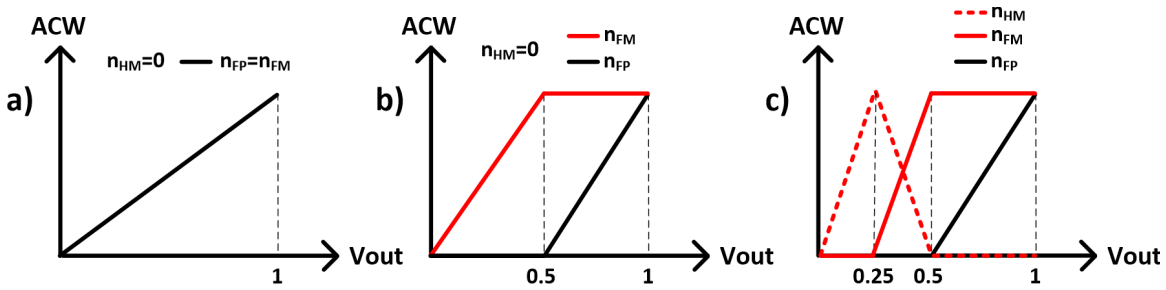

Fig. 9. ACW trajectory of (a) differential SCPA, (b) VMD, and (c) CG-VMD.

The waveform at node V' is filtered by the series LC resonator resulting in a sinusoidal waveform at the primary side of the transformer (Fig. 5) with amplitude

$$V_{\text{out},M} = \frac{2}{\pi}V' = \frac{2}{\pi}(n_F + 0.5n_H)V_{\text{dd}}. \tag{5}$$

2) Efficiency of CG-VMD: The efficiency of the CG-VMD for any choice of amplitude control word (ACW) is derived in this section. From Fig. 5, the capacitive divider loss and output voltage are

$$P_{\text{cd}} = P_{\text{cd},M} + P_{\text{cd},P} \tag{6}$$

and

$$V_{\text{out}} = V_{\text{out},M} + V_{\text{out},P} \tag{7}$$

which can be expanded to

$$P_{\text{cd}} = [n_{\text{FM}}(1-n_{\text{FM}}) + n_{\text{FP}}(1-n_{\text{FP}}) + 0.25n_{\text{HM}}(1-n_{\text{HM}}) - n_{\text{FM}}n_{\text{HM}}]\,CV_{\text{dd}}^2 f \tag{8}$$

$$V_{\text{out}} = \frac{2}{\pi}(n_{\text{FM}} + n_{\text{FP}} + 0.5n_{\text{HM}})V_{\text{dd}} \tag{9}$$

where the M and P subscripts denote main and peaking amplifier, respectively, ($n_{\text{HP}} = 0$). The output power and efficiency are then

$$P_{\text{out}}^0 = \frac{V_{\text{out}}^2}{2R_L} = \frac{2}{\pi^2 R_L}V_{\text{dd}}^2(n_{\text{FM}} + n_{\text{FP}} + 0.5n_{\text{HM}})^2 \tag{10}$$

$$\eta = \frac{P_{\text{out}}^0}{P_{\text{out}}^0 + P_{\text{cd}}} = \frac{1}{1 + \frac{P_{\text{cd}}}{P_{\text{out}}^0}} \tag{11}$$

$$\eta = \frac{1}{1 + \frac{\pi}{2Q_L}\frac{n_{\text{FM}}(1-n_{\text{FM}}) + n_{\text{FP}}(1-n_{\text{FP}}) + 0.25n_{\text{HM}}(1-n_{\text{HM}}) - n_{\text{FM}}n_{\text{HM}}}{(n_{\text{FM}} + n_{\text{FP}} + 0.5n_{\text{HM}})^2}} \tag{12}$$

with $Q_L = 1/(2\pi f R_L(C/2))$ being the loaded quality factor of the CG-VMD structure.

Though the capacitive divider loss of the PA is proportional to the carrier frequency as indicated by (8), it does not increase with frequency. This is because as frequency increases, the capacitor size decreases proportionally to maintain the same reactance. The efficiency of the PA depends on the loaded quality factor Q_L, with higher Q_L leading to lower capacitive divider switching loss and improved efficiency, but also reduced bandwidth, increased matching network insertion loss, and increased voltage stress on the capacitor bank. These issues limit practical implementations with on-chip matching networks to $Q_L \approx 2$ [10].

3) Efficiency Comparison: In this section, the ACW trajectories (n_{FM}, n_{HM}, n_{FP} versus V_{out}) for differential SCPA, VMD and CG-VMD will be described and the normalized loss and efficiency for these cases will be compared.

Fig. 9(a) shows differential SCPA operation, with the main and peaking PAs operating from full supply with equal magnitudes. Fig. 9(b) shows VMD operation, with both PAs operating at full supply. The main PA ACW increases until it saturates at 6 dB back off, and then the peaking PA increases to saturation. Fig. 9(c) shows the CG-VMD operation. The unit cells of the main PA operate at half supply until saturation at 12 dB back off. Then the unit cells of the main PA transition one-by-one to full supply thus n_{FM} increases as n_{HM} decreases. At 6 dB back off, the main PA saturates at full supply. The peaking PA ACW then increases in the fashion as VMD.

The normalized loss and efficiency for SCPA, VMD, and CG-VMD are plotted in Fig. 10. In VMD, the peak capacitive divider loss is half that of the SCPA, and there is also a loss null at 6 dB back off, resulting in the corresponding 6 dB efficiency peak. Beyond 6 dB back off, CG-VMD reduces the peak loss by another factor of 4 with an additional loss null at 12 dB back off, leading to 12 dB efficiency peaking.

B. Class-G Voltage-Mode Doherty With Non-Ideal Components

The SCPA/CG-SCPA can be modeled as a square wave voltage source with on-resistance R_{on}, as shown in Fig. 11 [10]. The power delivered by the PA to the output matching network is

$$P'_{\text{out}} = \frac{P_{\text{out}}^0}{\left(1 + \frac{2R_{\text{ON}}}{R_L}\right)^2} \tag{13}$$

and the conduction loss is

$$\frac{P_{\text{cond}}}{P'_{\text{out}}} = \frac{2R_{\text{ON}}}{R_L}. \tag{14}$$

Insertion loss attenuates the power delivered to the load by $P_{\text{out}} = \alpha P'_{\text{out}}$.

Switching losses come from the charge/discharge of parasitic capacitors and crowbar current in the SCPA/CG-SCPA drivers. This loss can be represented by an equivalent loss capacitance $C_{\text{sw}} \equiv P/(V_{\text{supply}}^2 f)$ where P is the power dissipated by the SCPA/CG-SCPA, including pre-drivers, when all cells are switching at frequency f, operating at V_{supply}, and drive no load. With this equivalent loss capacitance,

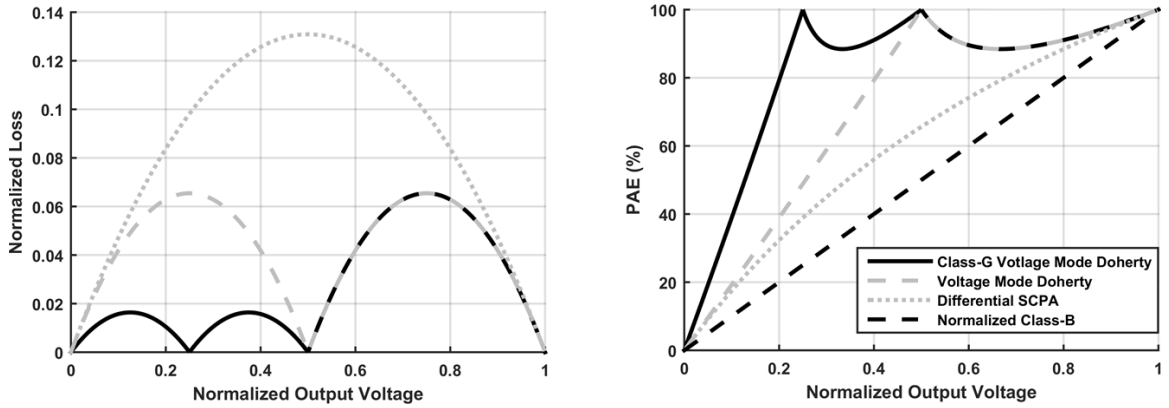

Fig. 10. Normalized loss and efficiency comparison of differential SCPA, VMD, and CG-VMD. ($Q_L = 1.5$ assumed).

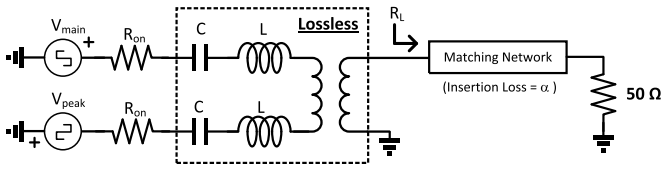

Fig. 11. Equivalent circuit for loss analysis. The loss of the capacitor banks, inductors, and transformer are lumped into matching network loss.

the switching loss is

$$P_{\rm sw} = n_{\rm FM} C_{\rm sw,FM} V_{\rm dd}^2 f + n_{\rm HM} C_{\rm sw,HM} (0.5 V_{\rm dd})^2 f + n_{\rm FP} C_{\rm sw,FP} V_{\rm dd}^2 f. \quad (15)$$

Conduction and switching losses can be traded through the sizing of the output stage transistors, with $R_{\rm ON} \propto 1/W$ and $C_{\rm sw} \propto W$. Therefore, the product $R_{\rm ON} C_{\rm sw}$ is constant and we can define the totem pole driver figure of merit $f_{\rm sw} = 1/(2\pi R_{\rm ON} C_{\rm sw})$ [10]. CMOS process scaling, anti-shoot-through current driver design, and a good layout practice can improve $f_{\rm sw}$. The switching loss relative to the power delivered to matching network is

$$\frac{P_{\rm sw}}{P'_{\rm out}} = \frac{\pi}{2} \frac{R_L}{2R_{\rm ON}} \left(1 + \frac{2R_{\rm ON}}{R_L}\right)^2 \frac{f}{f_{\rm sw}} \frac{n_{\rm FM} + 0.25k' n_{\rm HM} + n_{\rm FP}}{(n_{\rm FM} + 0.5 n_{\rm HM} + n_{\rm FP})^2} \quad (16)$$

where $f_{\rm sw}$ is defined for the CG-SCPA operating at full supply, and $k' = f_{{\rm sw},V{\rm dd}}/f_{{\rm sw},V{\rm dd}/2}$ is the ratio of CG-SCPA figures of merit when operating at full- and half-supply, respectively.

The overall output power and efficiency can now be written as

$$P_{\rm out} = \frac{\frac{2\alpha}{\pi^2} \frac{V_{\rm dd}^2}{R_L} (n_{\rm FM} + 0.5 n_{\rm HM} + n_{\rm FP})^2}{\left(1 + \frac{2R_{\rm ON}}{R_L}\right)^2} \quad (17)$$

and

$$\eta = \frac{\alpha}{1 + \frac{P_{\rm cond}}{P'_{\rm out}} + \frac{P_{\rm sw}}{P'_{\rm out}} + \frac{P_{\rm cd}}{P'_{\rm out}}}. \quad (18)$$

Fig. 12 shows the overall efficiency of the CG-VMD, using representative values of $\alpha, 2R_{\rm ON}/R_L$, $f_{\rm sw}$, k', and f, used in this paper. Note that when conduction and switching losses are added, the efficiencies 0, 6, and 12 dB back off are no longer 100%, and the efficiency peaking at deeper back off is lower.

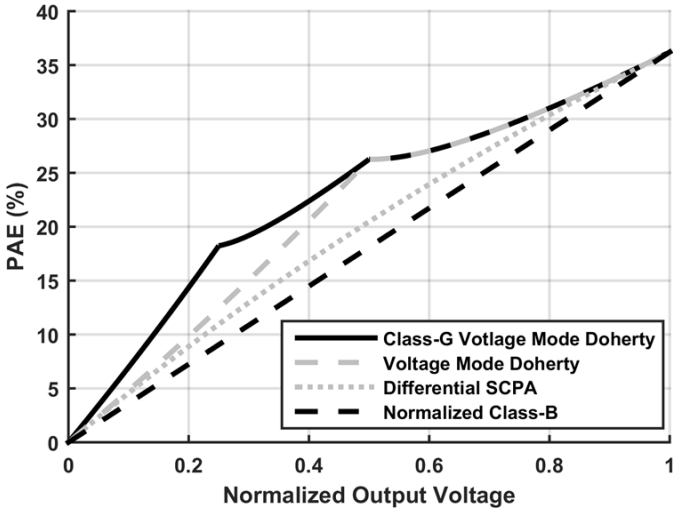

Fig. 12. Efficiency comparison of SCPA, VMD, and CG-SCPA with all relevant losses included. ($\alpha = 0.7$, $2R_{\rm ON}/R_L = 0.2$, $f_{\rm sw} = 27$ GHz, $f = 3.5$ GHz, and $k' = 1.8$).

At critical powers, the capacitive divider loss is zero and since the relative conduction loss $P_{\rm cond}/P'_{\rm out}$ is constant, the only factor reducing efficiency of the CG-VMD at deeper back off is increased relative conduction loss. Let $2A_0 = (\pi/2)(R_L/2R_{\rm ON})(1 + 2R_{\rm ON}/R_L)^2 (f/f_{\rm sw})$. Then by (16), the relative switching loss at 0/6/12 dB back off is

$$\frac{P_{\rm sw}}{P'_{\rm out}}(0\ {\rm dB}) = 2A_0 \frac{1+0+1}{(1+0+1)^2} = A_0 \quad (19)$$

$$\frac{P_{\rm sw}}{P'_{\rm out}}(6\ {\rm dB}) = 2A_0 \frac{1+0+0}{(1+0+0)^2} = 2A_0 \quad (20)$$

$$\frac{P_{\rm sw}}{P'_{\rm out}}(12\ {\rm dB}) = 2A_0 \frac{0+0.25k'+0}{(0+0.5+0)^2} = 2k'A_0 \sim 4A_0. \quad (21)$$

The increase in relative switching loss at 6 dB back off is due to the switching loss halving (only half of the unit cells are switching), while the output power is reduced by a factor of 4 [10]. The relative switching loss doubles again from 6 to 12 dB due to the decrease in $f_{\rm sw}$ of CG inverter when

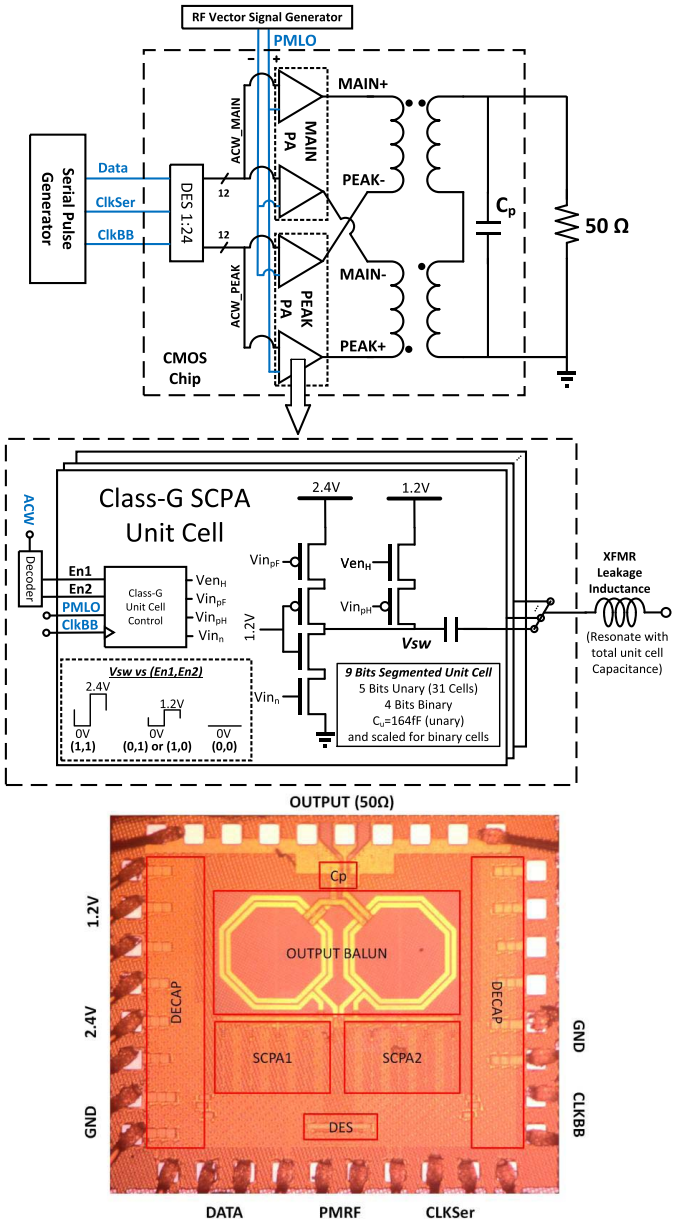

Fig. 13. CG VMD implementation and die micrograph.

operating at half supply. The doubling of relative switching loss in the CG-VMD for every 6 dB back off in power emphasizes the difficulty in achieving high back-off efficiency [13]. Similar efficiency degradation is also present in the conventional Doherty PA due to a sub-optimal load impedance in back off [22].

V. Implementation

The CG-VMD (Fig. 13) is implemented as a digital polar PA [21], in which an identical phase-modulated RF drives all unit cells, and the ACW determines whether each unit cell is OFF, ON at half supply, or ON at full supply. The main and peaking PAs are designed using a 5b unary, 4b binary, segmented DAC architecture such that the quantization noise will not limit the performance of the PA [24]. The PA is implemented in 45-nm CMOS SOI with integrated output transformer, and drives a 50 Ω load with no off-chip matching.

A. Output Transformer

The output transformer serves four purposes: differential to single-ended conversion, power combining, active-load modulation, and wideband matching. First, the differential to single-ended conversion of the transformer allows the PA to be pseudo differential, increasing output power by 6 dB and reducing sensitivity to supply/ground inductance [10]. Second, the voltages of the main and peaking PAs are combined in series, increasing the peak output power by another 6 dB. Third, the transformer provides the VMD load modulation, doubling the impedance seen by the main PA at back off, resulting in high efficiency. Moreover, primary load modulation fully utilizes the transformer structure at all power levels resulting in high back-off efficiency [15]. Last, the magnetizing and leakage inductances of the transformer are used as a wideband matching network such that no additional inductors are required.

The transformer can be modeled as coupled inductors with coupling factor k. At GHz frequencies, on-chip and low insertion loss transformers typically have $k \approx 0.7$, resulting in a leakage inductance comparable to the magnetizing inductance. Increasing transformer inductance lowers the quality factor of the parallel resonance $Q_p = R_L/\omega L$, but increases that of the series resonance $Q_s = \omega\,(1-k^2)L/(k^2 R_L)$ (Fig. 14). The overall bandwidth is determined by $\max(Q_s, Q_p)$. It can be shown that the minimum possible $\max(Q_s, Q_p)$ is $Q_{\min} = (1-k^2)^{1/2}/k$ which increases with decreasing coupling factor (Fig. 14). Therefore, the bandwidth of the CG-VMD is limited by the achievable coupling factor of the transformer. The matching network in Fig. 14 provides reactance compensation at offsets from the center frequency. Above/below the center frequency, the series resonance has positive/negative reactance which cancels the negative/positive reactance of the parallel resonance resulting in wider bandwidth.

The transformer in this paper is implemented as a figure-8 [23]. Electromagnetic simulations give $k = 0.6$ and $IL = 1.6$ dB for the balun. The load modulation of the CG-VMD output network operating at 0/6 dB and 12 dB back off is shown in Fig. 15.

B. Class-G SCPA Unit Cell Design

To minimize the delay mismatch between main and peaking PAs, the unit cells of both PAs are implemented with CG-SCPA unit cells (Fig. 13). The half-supply mode of the peaking PA is disabled and thus it functions as an SCPA. To equalize voltage steps between the main and peaking PAs, the LSB cell of the main PA is also disabled. Each unit cell is pseudo-differential to keep the fundamental virtual ground within the unit cell, reducing on-chip supply network loss and ripple [10]. The functionality of the CG-SCPA unit cell is explained in great detail in [6]; a brief explanation is provided here. In full-supply mode, $\mathrm{Vin_{pF}}$ and Vin_n switch, providing a 2.4 V pk–pk square wave, and $\mathrm{Ven_H}$ prevents current flow from the 2.4 to 1.2 V supply. In half-supply mode, $\mathrm{Vin_{pH}}$ and Vin_n switch, providing a 1.2 V pk–pk square wave. When the unit cell is off, $\mathrm{Vin}_n = 1.2$ V,

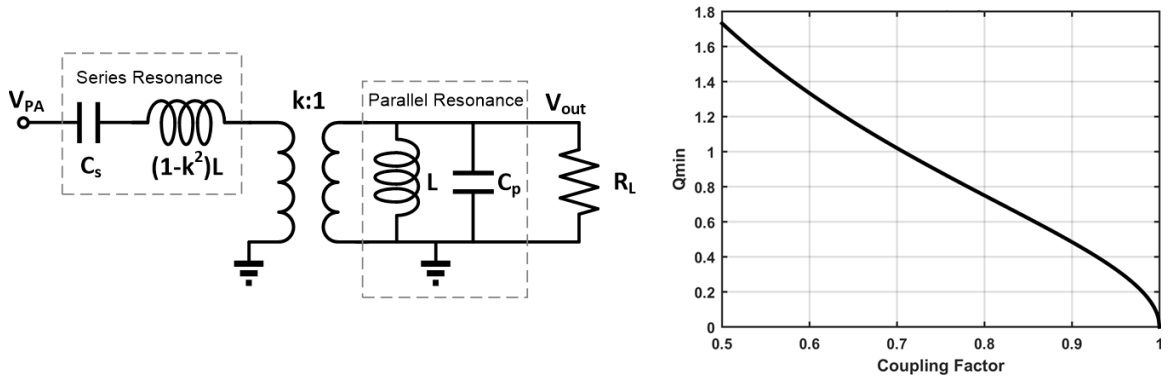

Fig. 14. Transformer as part of CG-VMD matching network. The series resonance is formed by leakage inductance and SCPA/CG-SCPA total unit cell capacitance, and the parallel resonance formed by magnetization inductance and a parallel matching capacitor. Q_{min} versus coupling factor shows the bandwidth limitation imposed by maximum achievable coupling factor of the transformer.

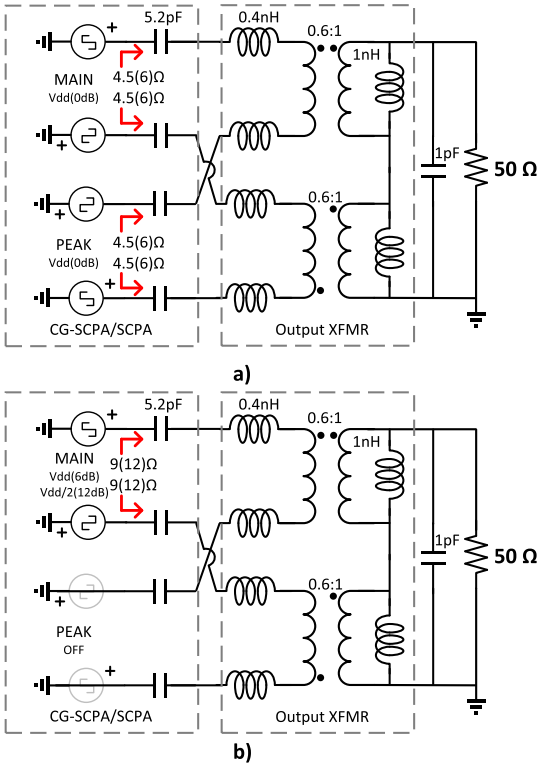

Fig. 15. Output transformer operation at (a) peak power (0 dB back off) and (b) 6 and 12 dB back off. The load impedance seen by the main PA is doubled at back off as expected. The impedance shown excludes transformer loss. When the loss is included, the impedance increases as shown in parentheses.

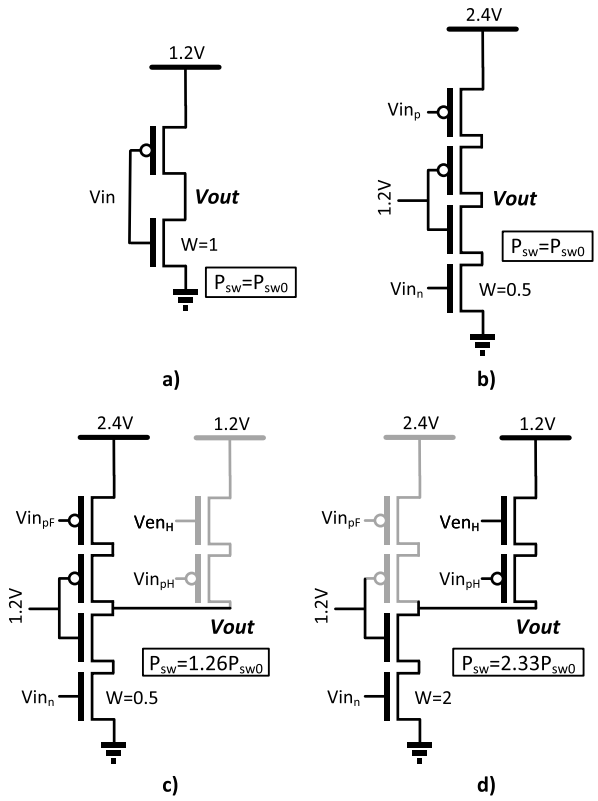

Fig. 16. Different totem pole driver designs. (a) Simple inverter. (b) Cascode inverter. (c) CG inverter operating at full supply. (d) CG inverter operating at half supply. The relative size of nMOS transistors is shown in this figure; the pMOS transistors are scaled to achieve the same drive strength.

$\text{Vin}_{\text{pF}} = 2.4$ V, and $\text{Vin}_{\text{pH}} = 1.2$ V, tying the unit cell capacitor to ground.

An important design metric of the unit cell is the totem pole driver figure of merit, f_{sw} discussed in Section IV, which affects overall efficiency of the PA. Different totem pole driver designs are shown in Fig. 16. To compare f_{sw} among these topologies, the final stage is sized to deliver the same power to the load with the same conduction loss R_{ON}/R_L, and the switching losses are compared. The simplest totem pole driver is a simple inverter, suitable for low-power PAs. The cascode inverter doubles voltage swing, thus the load impedance can be four times higher for the same output power, reducing the transistor size in half. Though the cascode inverter by itself has higher switching loss than a simple inverter, the power of the pre-driver is greatly reduced due to the smaller transistors, resulting in overall switching loss similar to that of a simple inverter. When operating at full supply, the CG inverter is simply a cascode inverter with parasitic half-supply branch increasing switching loss by about 26%. The half-supply branch of the CG inverter is stacked to withstand the full supply swing. This means, compared to a simple inverter, the transistors size must be doubled to maintain the

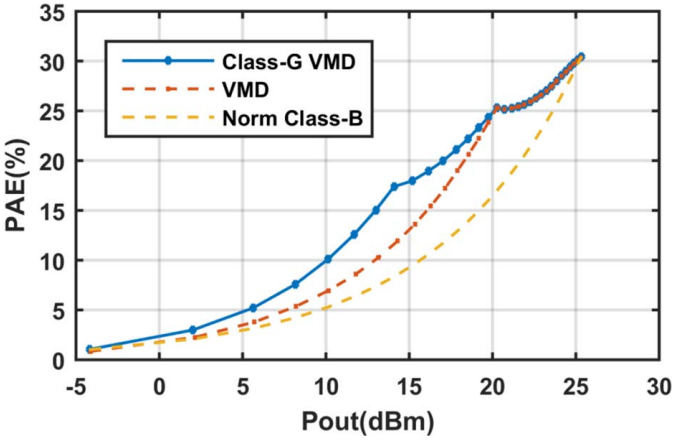

Fig. 17. Measured PAE versus Pout of CG-VMD at 3.5 GHz.

same conduction loss, resulting in twice the switching loss. Including the parasitic full-supply branch, the switching loss is increased by 133%. This means that the relative switching loss of a CG inverter when operating at half-supply compared to full supply is $k' = f_{\mathrm{sw},V\mathrm{dd}}/f_{\mathrm{sw},V\mathrm{dd}/2} = 1.8$ (Fig. 12).

VI. Measurement Setup and Result

The measurement setup is shown in Fig. 13. An RF vector signal generator (RF-VSG) is used to provide the phase-modulated LO (PM-LO), and a serial pulse pattern generator (PPG) is used to provide the ACW. The RF-VSG and PPG are synchronized with 10 MHz reference, and time alignment is performed at baseband. The output is probed with a 50 Ω GSG probe. The PAE accounts for all power consumed on the chip, including pre-drivers for all unit cells, LO distribution, and logic. The external PM-LO and serial ACW input signal powers are excluded, as most of the power is consumed in the termination resistors, while the power needed to drive a few minimum size inverters is all that would be required in an integrated implementation. Baseband signal generation, time alignment, and memoryless linearization are performed in MATLAB, with baseband sample frequency of 90 MHz, limited by the RF-VSG. Zero-order hold (ZOH) digital replicas appear at multiples of 90 MHz offset from the center frequency, and can be improved by the use of on-chip interpolation filter and wideband phase modulator [17].

The 45-nm CMOS SOI chips were fabricated on low resistivity and trap-rich high-resistivity substrates. Unless stated, results shown are from low-resistivity samples.

A. CW Measurement

For CW measurement, the ACW is swept and the output power and PAE are measured at different LO frequencies using a power meter. Fig. 17 shows the measured performance of CG-VMD at 3.5 GHz. The saturated power, peak PAE, 6 dB PAE, and 12 dB PAE are 25.3 dBm, 30.4%, 25.3%, and 17.4%, respectively. Compared to normalized Class-B, this gives a 1.6× and 2.3× improvement in PAE at 6 and 12 dB back off, respectively. For comparison, the performance of a VMD is also measured (Fig. 17) using ACW of Fig. 9(b). The CG-VMD improves efficiency beyond 6 dB back off

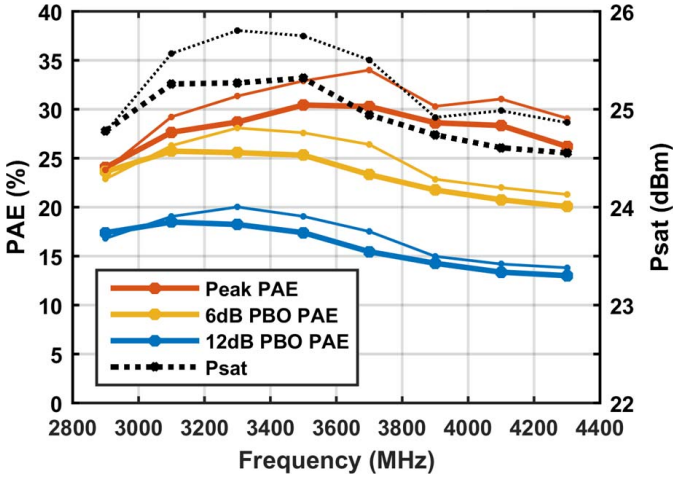

Fig. 18. Measured Psat and PAE at 0/6/12 dB back off across frequency. Results with low resistivity and trap-rich high-resistivity substrates are shown in thick and thin lines, respectively.

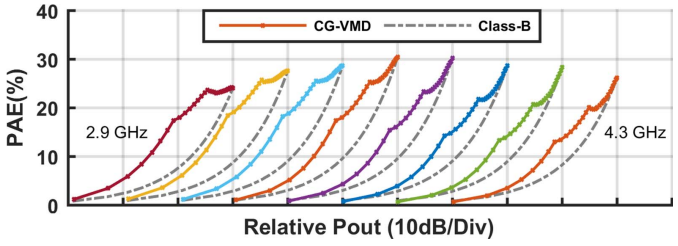

Fig. 19. Measured PAE back off characteristics from 2.9 to 4.3 GHz with 200 MHz step. Significant improvement over normalized class-B efficiency is observed over wide bandwidth.

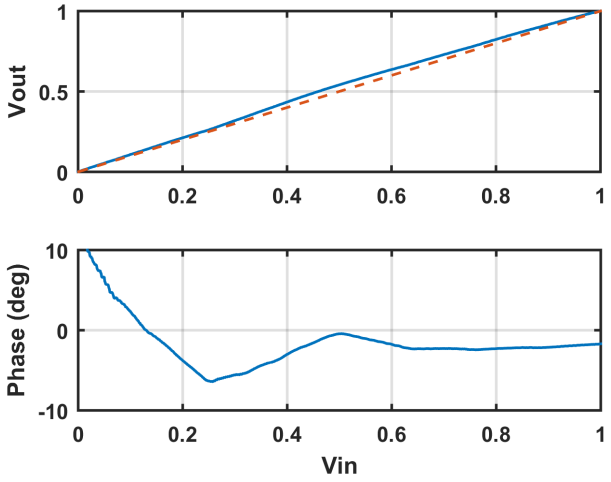

Fig. 20. Measured static AM–AM/–PM of the PA at 3.5 GHz. No discontinuity jump is observed at 6/12 dB back off.

as expected (VMD with cascode driver would have slightly higher peak and 6 dB back-off efficiency due to smaller driver switching loss as explained in Section V-B). The measured performance across frequency from 2.9 to 4.3 GHz is shown in Fig. 18, with 1 dB Psat fractional bandwidth of more than 38% and efficiency enhancement at both 6 and 12 dB back off maintained across the band, compared to a conventional Doherty PA which has narrow back-off efficiency bandwidth [16]. The trap-rich high-resistivity substrate variant

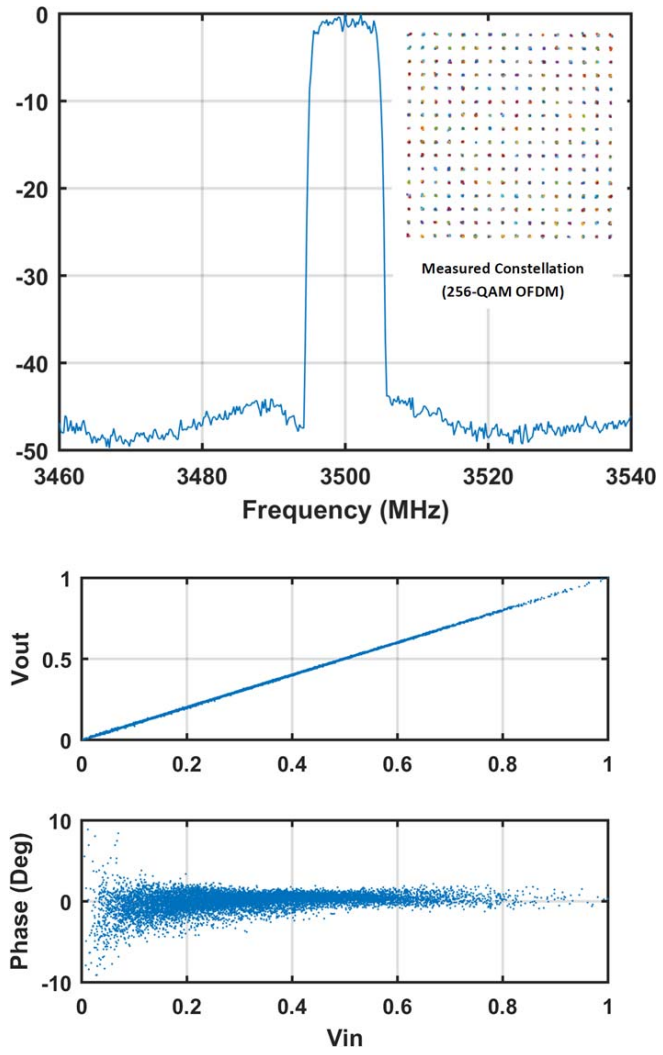

Fig. 21. Measured spectrum (500 kHz RBW), constellation, and dynamic AM–AM/–PM of 10 MHz 256-QAM OFDM with 8.2 dB PAPR. The dynamic AM–AM/–PM shows no glitch around 6/12 dB back off. The asymmetry in the spectrum is due to the measurement equipment reconstruction filter in the PM-LO path causing the distortion in polar architecture.

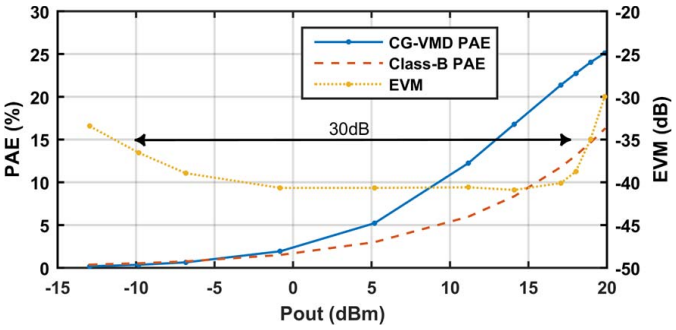

Fig. 22. Measured PAE and EVM of 10 MHz 256-QAM OFDM at various transmit power levels.

was also measured (Fig. 18) and shows higher PAE as expected due to lower substrate loss, in agreement with our analysis in Fig. 12.

The measured back-off PAE of the CG-VMD across frequency are plotted in Fig. 19 along with normalized

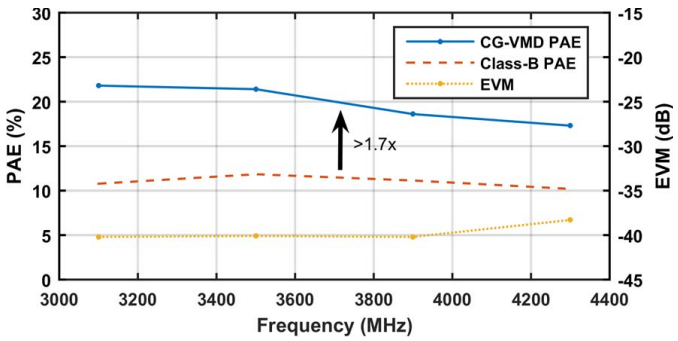

Fig. 23. Measured PAE and EVM of 10 MHz 256-QAM OFDM across frequency. Low EVM of better than −38 dB and efficiency enhancement of at least 1.7× is achieved over greater than 1 GHz bandwidth.

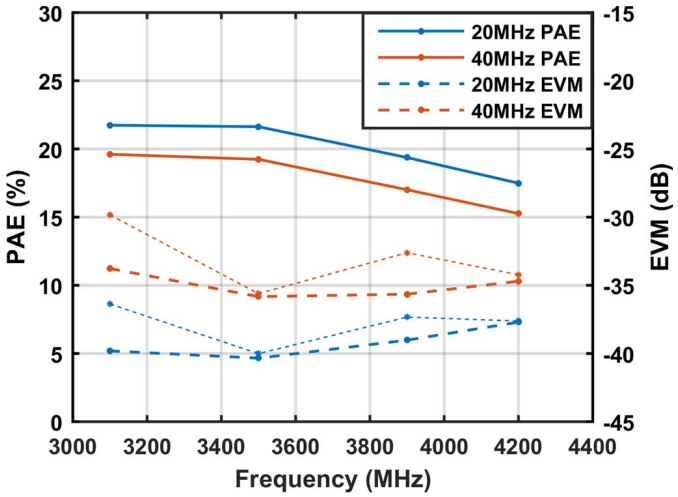

Fig. 24. PAE and EVM for 20 MHz / 40 MHz 256-QAM OFDM. For EVM, thick and thin lines indicate with and without receive amplitude equalization respectively.

class-B efficiency. The PA shows high-efficiency enhancement at both 6 and 12 dB back off over more than 1 GHz bandwidth.

B. Modulation Measurement

For measurement of modulated data, the PA is linearized with memoryless 1024 element AM–AM and AM–PM lookup tables (LUTs); the number of elements can be significantly reduced with interpolation techniques without affecting the performance. Fig. 20 shows the measured AM–AM/–PM characteristics of the PA, generated by applying a 30 kHz AM signal with 100% modulation index centered at 3.5 GHz. At each carrier frequency, the LUT used to linearize the PA is generated in a similar manner, without any additional adaptation. Prior to linearization, the AM–AM/–PM characteristics are free of any discontinuities present in conventional mode-switching efficiency-enhanced PAs. The AM–PM variation is due to a difference in the delay of unit cells when operating at full- and half-supply, respectively, and can be improved with delay compensation over process corners.

1) Narrowband Modulation: With 10 MHz 32-carrier 256-QAM OFDM with 8.2 dB PAPR, the PA achieves 17.1 dBm Pavg, −40.1 dB EVM, > 45 dBc ACPR, and 21.4%

TABLE I
COMPARISON WITH CMOS PA WITH GREATER THAN 6 dB BACK-OFF EFFICIENCY ENHANCEMENT

	This Work			[11]	[12]	[13]
Frequency (GHz)	3.5			3.7	2.4	2.4
1dB Psat Bandwidth(%)	38			48	-	43
Psat (dBm)	25.3			26.7	27.7	31.5
CMOS Node (nm)	45 SOI			65	65	45
Supply Voltage	1.2/2.4			1.65/3	2.5/1.8/1.35/0.85	2.4
Peak/6dB/12dB PAE (%)	30.4/25.3/17.4			40.2/37.0/26.2†	45.1/42/20***	27/20/13***
Topology	Class-G Voltage Mode Doherty			Class-G Conventional Doherty	Multi-Level Outphasing	Dynamic Power Control Outphasing
Glitch	No glitch††			Supply switching, and PA input discontinuities.	Supply switching, outphasing angle discontinuities.	Outphasing angle and impedance discontinuities.
Glitch Mitigation	Not needed			None	Supply damping network	Skipping window
Wideband back-off efficiency enhancement	>1.7x over 1 GHz		>1.6x over 1 GHz	2 discrete frequencies shown (3.7 GHz and 4.3 GHz)	N/A	N/A
Modulation	**10 MHz 32 Carriers 1024-QAM**	**10 MHz 32 Carriers 256-QAM**	**40 MHz 802.11ac 256-QAM**	1 MHz Single-Carrier 16-QAM	20 MHz 802.11g 64-QAM	20 MHz 64-QAM WiFi
Pavg (dBm)	**14.8**	**17.1**	**15.6****	20.8	20.2	24.8
Output PAPR(dB)*	**10.5**	**8.2**	**10.1**	5.9	7.5	6.7
EVM (dB)	**-40.3**	**-40.1**	**-35.8**	-24	-31.4	-25
Average PAE(%)	**18.0**	**21.4**	**19.2****	28.8†	27.6	16
Matching Network	On-Chip			On-Chip	On-Package	On-Chip

*Output PAPR = Psat(dBm)-Pavg(dBm)
**Trap-rich high resistivity substrate
***Estimated from figure
†Drain Efficiency, not PAE
††LSB step glitch, as large as conventional RFDAC

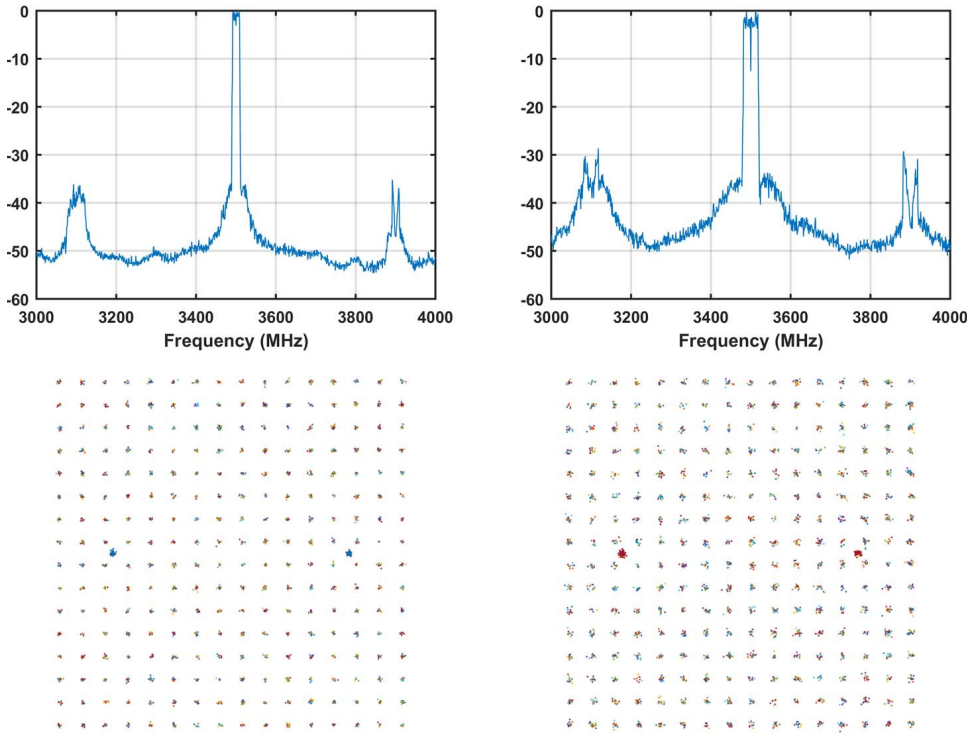

Fig. 25. Spectra (1 MHz RBW) and constellations for 256-QAM OFDM with 20 MHz (left) and 40 MHz (right) bandwidth.

PAE (Fig. 21), a more than a 1.8× improvement in efficiency compared to class-B back off. The dynamic AM–AM/–PM of the PA are glitch free at 6 and 12 dB back off as expected. Fig. 22 shows the tradeoff between EVM and PAE as the transmit power is varied. Measurement shows that the PAE can be improved by intentionally clipping the signal in exchange for degraded linearity. In particular, the CG-VMD achieves 19 dBm, 24% PAE while maintaining the required EVM to transmit 256-QAM OFDM. Excellent EVM is achieved over a wide dynamic range demonstrating the robustness of this PA with non-adaptive memoryless linearization (linearized PAs often require adaptive LUTs to operate over a wide dynamic range). At very low power, the efficiency is limited by the LO distribution power, and the EVM is limited by quantization

noise. Fig. 23 shows the efficiency and linearity of the PA when transmitting the 10 MHz 32-carrier 256-QAM OFDM signal at different frequencies. An efficiency enhancement of at least 1.7× is achieved while maintaining better than −38 dB EVM over 1 GHz bandwidth.

2) Wideband Modulation: For wideband modulation measurements, the RF-VSG is replaced by a 65 GSa/s arbitrary waveform generator (Keysight M8195A) which directly generates the wideband PM-RF signal. A baseband sampling frequency of 400 MHz is used. Although the M8195A is synchronized to the PPG with 10 MHz reference, a slow carrier phase drift is observed which is calibrated out in the reported results. With trap-rich high-resistivity substrate, the PA achieved −40.3/−35.8 dB EVM and 21.6%/19.2% PAE for 20/40 MHz 256-QAM OFDM modulation with 8.8/10.1 dB PAPR at 3.5 GHz (Fig. 24). The corresponding spectra and constellations are shown in Fig. 25, with measurement noise floor of better than −45 dBc. The far-out spectrum is limited by large ZOH replicas, making it difficult to conclusively demonstrate a glitch free far-out spectrum. An on-chip interpolation filter [17] would be required to move the replicas to a higher offset and demonstrate that far-out glitches do not exist. In the 40 MHz modulation measurement, the 802.11 mask is not quite met due to memory effects from the power supply decoupling network on the PCB. To support wider modulation bandwidth without significantly degrading modulation accuracy, the bypass capacitors would need to be moved closer to the chip and the supply/ground bondwires would need to be shorter.

Table I compares the performance of this PA to the current state-of-the art PAs with efficiency peaking beyond 6 dB back off. The removal of mode-switching glitches enabled by the CG-VMD architecture allows for significant efficiency enhancement while maintaining excellent EVM without any further glitch mitigation technique. The efficiency can be further improved by migration to a finer linewidth CMOS process (higher f_{sw}) and reduced transformer loss using on-package transformer.

VII. Conclusion

This paper demonstrates the combination of VMD and CG SCPA achieving efficiency peaking at 6 and 12 dB back off without introducing mode-switching glitches present in conventional architectures. The absence of the glitches and the narrowband impedance inverter allow this architecture to achieve high efficiency with excellent EVM while transmitting high PAPR modulation over wide bandwidth. As the need for higher spectral efficiency continues, modulation is expected to have ever higher PAPR and required EVM, and the techniques presented in this paper will help enable high-efficiency transmitters in the future standards.

Acknowledgment

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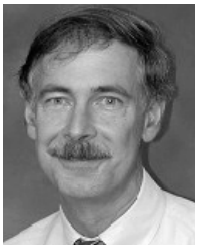

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