A 19 nV/$\sqrt{\text{Hz}}$ Noise 2-μV Offset 75-μA Capacitive-Gain Amplifier With Switched-Capacitor ADC Driving Capability

Hanqing Wang, Gerard Mora-Puchalt, Colin Lyden, Roberto Maurino, and Christian Birk

***Abstract*— This paper describes a capacitive-gain amplifier (CGA) with common-mode (CM) sampling (CMS) and switched-capacitor driving capability. The CMS CGA defines the amplifier CM voltage in a single auto-zero phase that significantly reduces the CM settling time. A pre-charge technique and dynamic filtering are used to allow the CGA to drive a switched-cap analog-to-digital converter (ADC) directly that relaxes the speed requirement on CGA and reduces folded noise aliases due to ADC sampling. As a result, it achieves 19-nV/$\sqrt{\text{Hz}}$ noise density while dissipating 75 μA. The 5 ppm/full-scale-range integral nonlinearity is achieved with programmable gain range from 1 to 128 with 2.7 to 3.6 V supply. It has 2 μV typical offset and 0.81 ppm/°C max gain error drift. The CGA was implemented in a 0.18-μm CMOS 1.8/3.3 V ultra low leakage technology and occupies only 0.53 mm^2 die area.**

***Index Terms*— Auto-zero (AZ), chopping, common mode (CM) sampling (CMS), gain boost, low drift, low offset, pre-charge, programmable gain amplifier (PGA), rail-to-rail, switch capacitor.**

I. Introduction

INSTRUMENTATION programmable gain amplifiers (PGAs) are essential components in precision signal conditioning [1]–[5]. Capacitive PGAs are popular for their low power, low noise, and high precision [6]–[9]. Compared to a resistive gain amplifier [10]–[14], the capacitive-gain network is highly linear, does not dissipate static power and can be noiseless. Additionally, capacitors have excellent matching and temperature drift which has a positive impact on offset/gain errors and their drift. They also offer a very high input impedance at low frequencies and rail-to-rail operation, which makes them very suited to interfacing with sensors such as thermocouples, resistance temperature detectors, or pressure sensors.

Capacitive PGAs, however, do not naturally define the amplifier inputs common-mode (CM) voltage present at the PGA summing node. In order to set this voltage, additional circuitry is necessary. This circuitry is designed not to interfere with the input signal amplification process and typically involves very large resistors at Giga–Ohm level and a corresponding slow CM settling [5]–[8]. Thus, these amplifiers cannot support fast multi-channel switching. In normal application, two extra unity gain buffers are added at PGA's output to drive analog-to-digital converter (ADC) that results in more power and area, because high closed-loop gain PGA is normally slow with weak driving ability. To suppress the amplifier's offset and large ripples at PGA output, dc servo loop, and ripples reduction loop are widely used [6], [7], [10], [13], [17] that make design complex and may introduce more error sources. Because the input signal is fully chopped in capacitive PGA, the settling is more challenging compared to resistor-based PGA.

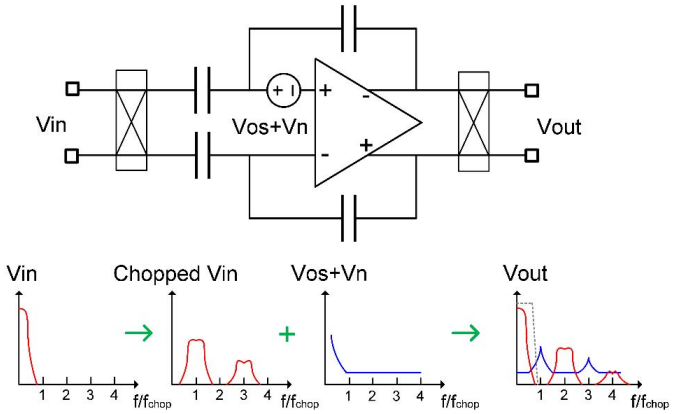

Fig. 1. Basic concept of CGA.

This paper presents a 19 nV/$\sqrt{\text{Hz}}$ noise, 2-μV offset, and 0.81 ppm/°C gain error drift PGA with switched-cap ADC driving capability [15]. In order to significantly reduce the CM settling time, the PGA employs a CM sampling (CMS) scheme which defines the amplifier CM voltage in a single auto-zero (AZ) phase. Additionally, a pre-charging technique and dynamic filtering (DF) are used to allow the PGA to efficiently drive the ADC switched-cap inputs directly while achieving a considerable noise reduction.

This paper is organized as follows. In Section II, it proposes a CMS scheme which defines the amplifier common voltage in each AZ phase and a fast two-stage amplifier without slew rate limitation. Section III describes how the PGA drives switched-cap ADC efficiently with the pre-charging technique and DF. The overall implementation is described in Section IV, and test results are given in Section V. The paper ends with conclusions in Section VI.

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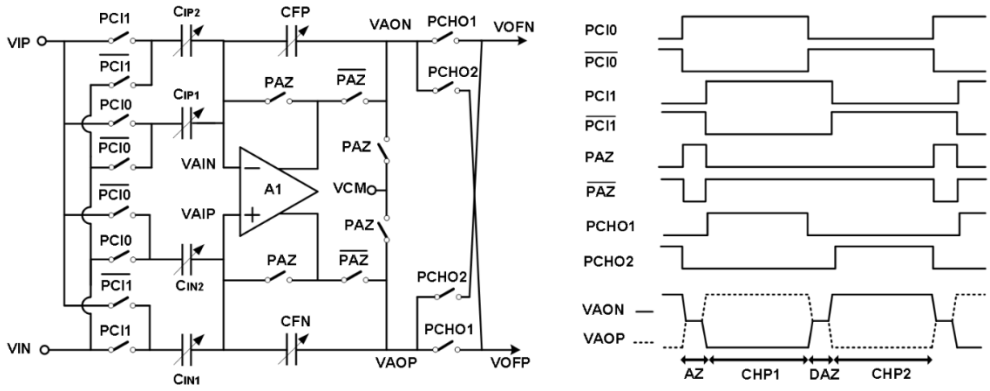

Fig. 2. Simplified proposed CMS capacitive PGA.

II. Common-Mode Sampled Gain Network

A. Conventional Capacitive-Gain Amplifier Topology

As shown in Fig. 1, the basic concept of capacitive-gain amplifier (CGA) is that the low-frequency input signal is fully chopped and amplified by the gain network, low-frequency amplifier error components such as offset and flicker noise remain at baseband as they are not affected by the input chopping and finally the signal is de-chopped back to baseband while the amplifier error components are chopped to higher frequencies, and filtered at a later stage.

Previously, large resistors which are typically implemented with transistors have been added to setup the common voltage at amplifier's summing nodes [5]–[8]. The main drawback is that the large resistor is intrinsically slow. Hence, the response to input common voltage changes is slow. Furthermore, the resistor itself may also introduce linearity error if it is not biased properly. In [9], a CM cancellation circuit is proposed to speed up the CM response. An extra amplifier is needed for this CM cancellation, requiring more power and increasing input-referred noise. To suppress the offset of the op-amp and ripples at the amplifier output, dc servo loops [6], [7], and ripple reduction loops were developed in [6], [7], [10], [13], and [17] that increase more power, area.

B. Common-Mode Sampled Scheme

Auto-zeroing plus chopping is widely used in precision designs [16]–[18]. In this design, the proposed PGA also employs these techniques to speed up CM response while cancelling the amplifier's offset. The simplified PGA with CMS [19] is shown in Fig. 2. Unlike the previously reported capacitive PGAs the input capacitors are split into two halves

$$C_{\mathrm{IP1}} = C_{\mathrm{IP2}} = \frac{C_{\mathrm{IP}}}{2}, C_{\mathrm{IN1}} = C_{\mathrm{IN2}} = \frac{C_{\mathrm{IN}}}{2}. \tag{1}$$

During the AZ phase [Fig. 3(A)], two input cap halves (C_{IP1} and C_{IN1}) are connected to the positive input and the other two halves (C_{IP2} and C_{IN2}) to the negative input so that, in charge average, the input CM voltage is applied to their left plates. Simultaneously, amplifier, A1 is in unity gain configuration so that its offset is sampled on nodes "VAIP", "VAIN."

During the amplifying period, the first chop phase [Fig. 3(B)] happens when C_{IP2} and C_{IN1} are reconnected to the opposite input voltage. Then, the differential signal is amplified by the gain network. We can analyze the charge at node "VAIP" as an example. In AZ zero phase the charge stored at node "VAIP" $Q_{\mathrm{VAIP\_AZ}}$ is

$$\begin{aligned} Q_{\mathrm{VAIP_{AZ}}} &= (V_{\mathrm{CMA}} + V_{\mathrm{OS}}/2 - \mathrm{VIP})C_{\mathrm{IP1}} + (V_{\mathrm{CMA}} + V_{\mathrm{OS}}/2 - \mathrm{VIN})C_{\mathrm{IP2}} \\ &\quad + (V_{\mathrm{CMA}} + V_{\mathrm{OS}}/2 - V_{\mathrm{CMO}})C_{\mathrm{FP}}. \end{aligned} \tag{2}$$

And in the CHP1 phase, the charge $Q_{\mathrm{VAIP_{CHP1}}}$ is

$$\begin{aligned} Q_{\mathrm{VAIP\_CHP1}} &= (V_{\mathrm{CMA}}{}' + V_{\mathrm{OS}}/2 - \mathrm{VIP})(C_{\mathrm{IP1}} + C_{\mathrm{IP2}}) \\ &\quad + (V_{\mathrm{CMA}}{}' + V_{\mathrm{OS}}/2 - \mathrm{VOFN})C_{\mathrm{FP}} \end{aligned} \tag{3}$$

where V_{CMA} is the actual output CM voltage of A1, which also sets the input CM of A1 during the AZ phase. V_{CM} is the desired output CM voltage of A1 and V_{OS} is A1 offset. For simplicity, let's assume $V_{\mathrm{CM}} = V_{\mathrm{CMA}}$. The charge at the summing node is unchanged between AZ and CHP1 phase. So we can get

$$\mathrm{VOFN} = V_{\mathrm{CMO}} + \frac{(\mathrm{VIN} - \mathrm{VIP})}{2}\frac{C_{\mathrm{IP}}}{C_{\mathrm{FP}}}. \tag{4}$$

Similarly for VOFP

$$\mathrm{VOFP} = V_{\mathrm{CMO}} + \frac{(\mathrm{VIP} - \mathrm{VIN})}{2}\frac{C_{\mathrm{IN}}}{C_{\mathrm{FN}}} \tag{5}$$

where $C_{\mathrm{IN}} = C_{\mathrm{IP}}$, $C_{\mathrm{FN}} = C_{\mathrm{FP}}$. The differential input voltage is amplified by the gain network and ideally the amplifier offset is cancelled so that neither dc servo loop nor ripple reduction loop is needed.

The third phase is dummy AZ (DAZ) phase [Fig. 3(C)] which is similar to AZ phase. The input cap connections to input signal are swapped compared to AZ phase. The differential input signal is zero so that the A1's output is at output CM voltage. Note that, there is no auto-zeroing in this phase. The AZ frequency is not higher than chop frequency, otherwise the auto-zeroing KT/C noise will fold back to baseband. During the second chop phase [Fig. 3(D)], all the input capacitors are switched to the opposite input voltage so the differential signal is amplified with the opposite polarity before it is de-chopped.

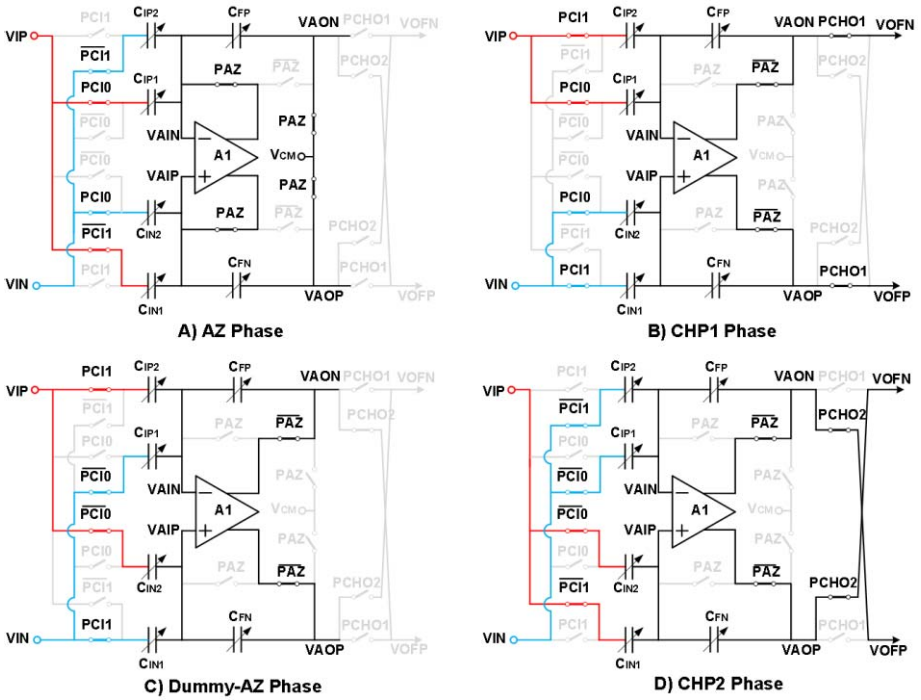

Fig. 3. CMS capacitive PGA operation.

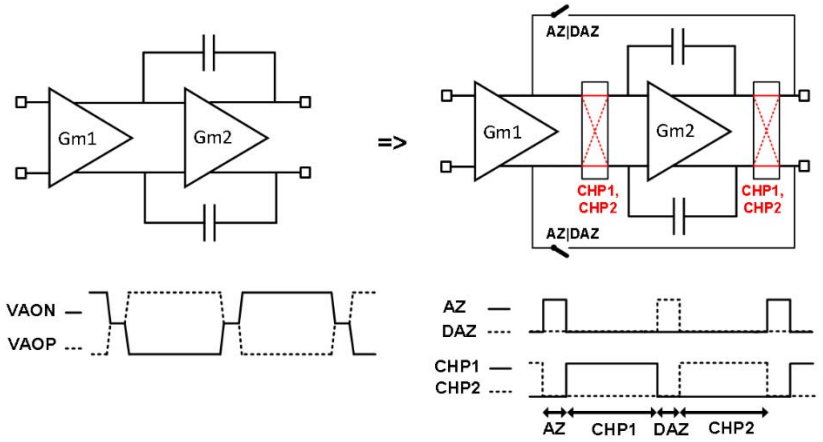

Fig. 4. Fast Miller-compensated amplifier with split Gm1 and Gm2.

The charge at A1 summing nodes is unchanged during the whole AZ cycle. The A1 offset and flicker noises are cancelled by the AZ and the sampled AZ noise at low frequencies is modulated up to the chopping frequency. In each AZ phase, the amplifier CM voltage is reset, yielding a fast response to input CM voltage variations. However, it requires CMFB and capability to drive and settle the input capacitors during AZ phase. It may result in more power and area that need to be optimized.

C. Fast Two-Stage Amplifier Without Slew Rate Limitation

The main amplifier A1 is a two-stage Miller-compensated amplifier for large output swing. Because of CM voltage sampling and chopping, the charge movement on Miller cap is large from phase-to-phase (Fig. 2). The worst case is when the input voltage is full scale, then the A1 output has to settle between zero and full scale in a short period and the speed is limited by slew rate. To solve the slew rate limitation, the Gm1 and Gm2 stages are separated during AZ phase and combined during amplify phase (see Fig. 4). In AZ (or DAZ) phase, Gm2 is disconnected from Gm1 and the slow input differential signal is kept on the Miller capacitors. The first stage Gm1 is used to define the CM voltage. Gm2 with Miller cap is chopped between CHP1 and CHP2 phase so that there is no large charge moving on Miller capacitors. When the AZ phase ends, Gm2 and Gm1 are combined, the right voltage is already on the Miller cap.

III. Switched-Cap ADC Driving Techniques

Normally, two extra ADC buffers or off-chip capacitors are required to drive the ADC switched-cap inputs, because the

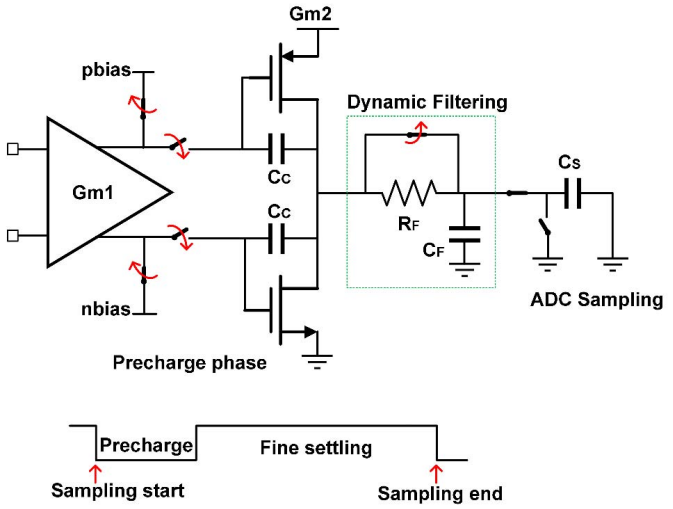

Fig. 5. ADC pre-charge buffer and DF.

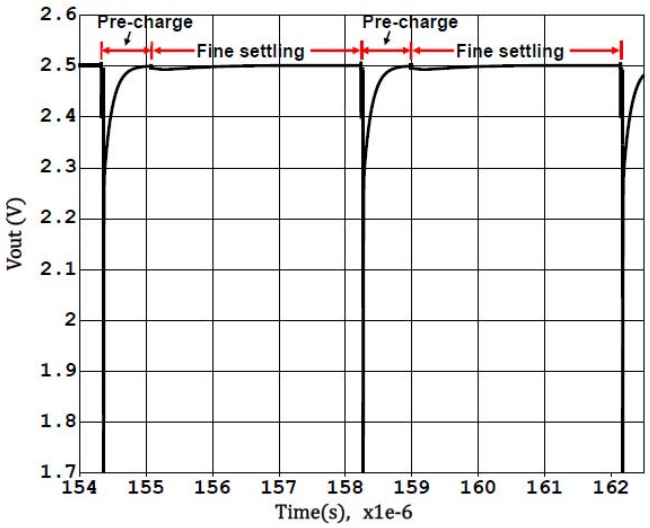

Fig. 6. Simulated PGA transient response with ADC pre-charge and DF while driving ADC.

high closed-loop gain PGA is normally low bandwidth so that it cannot drive the ADC [2]–[4]. In contrast, for ADC input buffers, to achieve accurate settling, wide bandwidth is required at the expense of higher noise aliases. Even the PGA was fast enough to drive ADC, the input-referred noise would be higher due to noise aliases and hence the overall power efficiency would be low. To overcome these challenges, a low power pre-charging scheme and DF are employed.

A. ADC Pre-Charging Buffer

As shown in Fig. 5, for a two-stage amplifier, if the Gm2 with Miller cap is disconnected from Gm1, the Gm2 stage will become a self-biased single-stage amplifier which is much faster than the high closed-loop gain PGA. With this feature, the output stage of two-stage Miller-compensated amplifier can be reused as an ADC pre-charge buffer. At the beginning of each ADC sampling phase, the Class-AB output stage together with Miller cap is disconnected from first stage so that the output stage holds a very close approximation of the desired output voltage. The outputs of the first stage are biased to the correct voltage, ready for reconnecting back to Gm2 (except the sampling period with AZ). Excluding Miller capacitor, the capacitance at first-stage output is small which is fast for mode switching. When the ADC is sampling, the kick back through the Miller cap will boost the output stage current strongly so that it pre-charges the ADC to the voltage very close to the desired final value. Less than 20% of sampling period is used for pre-charging. Then, in the fine settling phase, the output stage is reconnected back and the PGA only need to charge a very small residual error that is within several millivolt (Fig. 6). This scheme relaxes the speed requirement on PGA and there is no extra amplifier needed, nor extra power or area. Note that the large glitch in Fig. 6 is caused by ADC sampling.

To analyze how this pre-charge method improves settling, assuming a single pole system without slew rate limitation and the output voltage is full scale 2.5 V, the settling error is given by

$$V_{\mathrm{ERROR1}} = 2.5\ V \cdot \exp\left(-\frac{2\pi \cdot \mathrm{BW}}{256\ \mathrm{kHz}}\right) \tag{6}$$

$$V_{\mathrm{ERROR2}} = V_{\mathrm{residual}} \cdot \exp\left(-D \cdot \frac{2\pi \cdot \mathrm{BW}}{256\mathrm{kHz}}\right) \tag{7}$$

where the V_{ERROR1} is the settling error without pre-charging and V_{ERROR2} is settling error with pre-charging. D is duty cycle used for fine settling and V_{residual} is the residual error after pre-charging. BW is the bandwidth of the closed-loop gain PGA. The ADC samples at 256 kHz.

For pre-charge architecture, most sampling period is expected to be used for fine settling. The time used for pre-charging depends on the settling of the pre-charge buffer and delta-sigma ADC integrator 1. The pre-charge buffer and integrator 1 summing nodes settling error should be small enough that can relax the speed requirement for fine settling. The charge injection of the switches used to disconnect Gm2 will also introduce error. Here, 20% sampling period is used for pre-charging and the design target for residual error after pre-charging phase is no larger than 3 mV. The remaining 80% sampling period is used for fine settling. For 5-μV final settling error, the bandwidth requirement is 325 kHz. For normal PGA, to settle to the same accuracy with 100% sampling period for settling, the bandwidth requirement is 535 kHz. So for same settling accuracy, the speed requirement for this pre-charge architecture is lower. It can save more power with less noise folding.

B. Dynamic Filtering

Analysis above assumes the settling is ideally linear without slewing. However, to allow margin for non-ideal factors, a higher bandwidth of the PGA is chosen. The DF can be used to band limit the noise further. As shown in Fig. 5, in the pre-charge phase when the output stage is pre-charging ADC, the resistor is bypassed. Then, in the fine settling

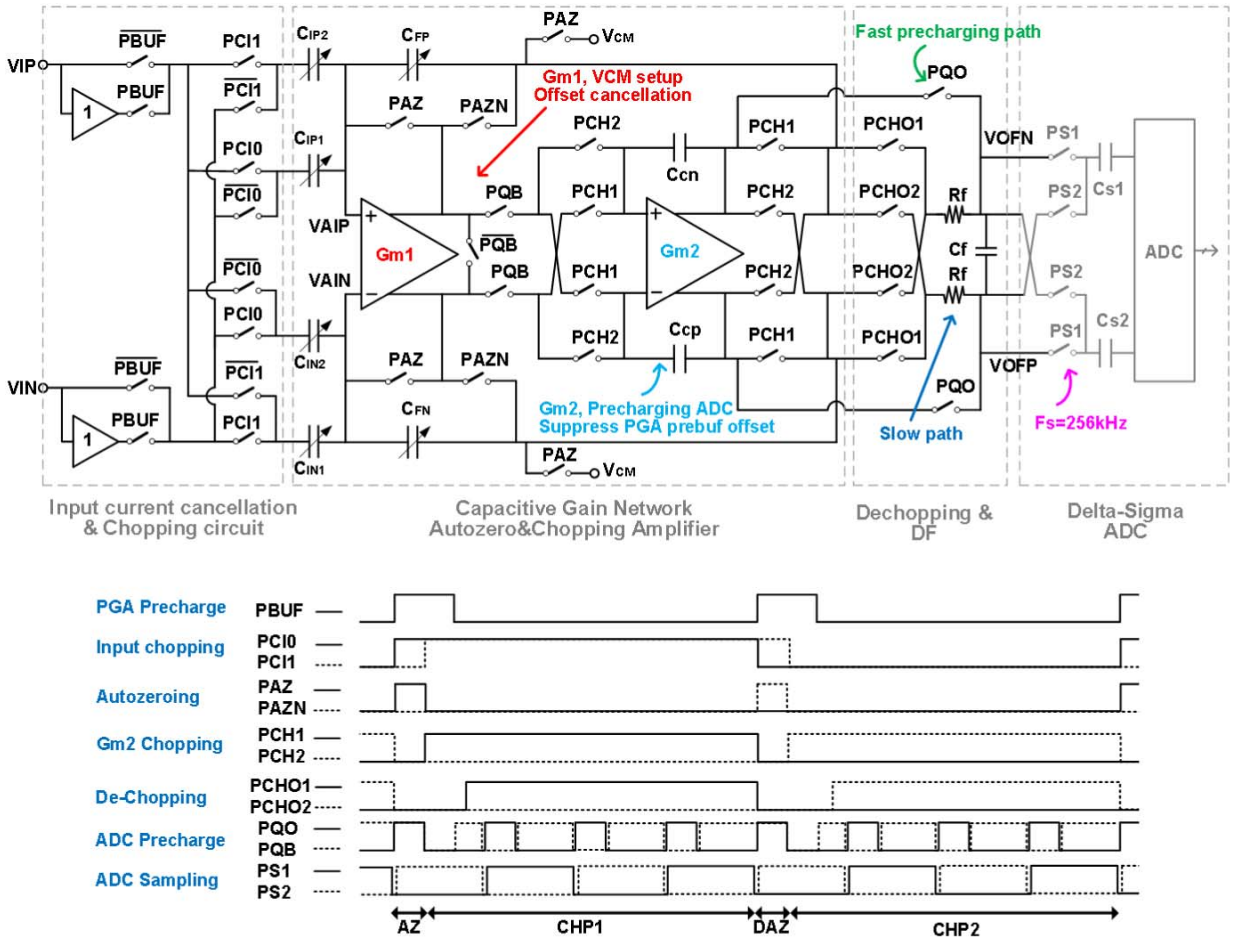

Fig. 7. Full circuit diagram of the fast settling CGA.

phase, the resistor with capacitor can band-limit the noise folding. The resistor and capacitor of dynamic filter are 20 kΩ and 15 pF, respectively. And the capacitance load from the ADC sampling capacitor is 2 pF. The dynamic filter is used to band limit the high-frequency thermal noise. The relative low-frequency chopping error is suppressed by the ADC digital filter with notch at chopping frequency. With pre-charging and DF, trading-off between settling and noise folding, the final input-referred noise is around 1.6× of the noise without noise aliases. Without dynamic filter, the noise is 25% higher because of more noise aliases.

IV. Overall Implementation

A. Top-Level Circuit Implementation

Fig. 7 shows the detailed PGA diagram including input pre-charge buffers, input chopper, capacitive gain network, de-chopper, and dynamic filter. The main amplifier is a two-stage (Gm1, Gm2) Miller-compensated amplifier. Two dynamically boosted buffers are used to pre-charge PGA input capacitors to reduce input current due to the chopping activity. Their average current is about 8% of total power.

During the PGA amplifying phase, at the beginning of each ADC sampling phase, Gm2 together with Miller caps Ccn and Ccp are disconnected from Gm1 (switch PQB). This output stage alone can pre-charge the ADC switched-cap input automatically (switch PQO). This structure acts as a class-AB single stage that is much faster than the full closed-loop PGA. DF is bypassed in pre-charge phase. After the pre-charge phase is complete, Gm2 is connected back to Gm1 for fine settling and DF is connected to band-limit noise.

One of the key design challenge is to achieve an accurate first ADC sample settling after the AZ phase and chopping. There are several actions that have to be done in a short period including AZ, chopping, and ADC sampling. In [8], a continuous time delta-sigma ADC is used to relax the speed requirement on input gain amplifier. However, it discards one sample data after chopping phase so that if the input is an ac signal, it may introduce large distortion. In this design, during the AZ phase, there is less time available for the PGA to drive the ADC and additionally, the amplified pre-charge buffers offset could saturate the PGA outputs at high PGA gains before they are bypassed. Two techniques are used to overcome these challenges.

First, during the AZ phase, Gm1 is configured as an unity gain amplifier to perform the AZ function on its own while Gm2 is disconnected from Gm1 to pre-charge the ADC inputs. Both actions happen simultaneously hence there is no settling penalty due to the AZ function. During the amplifying phase, Gm1 and Gm2 are coupled together and the offset of Gm2 is well suppressed by the Gm1 high open-loop gain.

TABLE I
PGA GAIN SETTINGS

Gain	1	2	4	8	16	32	64	128
Input Cap (pF)	4.48	8.96	17.92	17.92	17.92	17.92	17.92	17.92
Feedback Cap (pF)	4.48	4.48	4.48	2.24	1.12	0.56	0.28	0.14

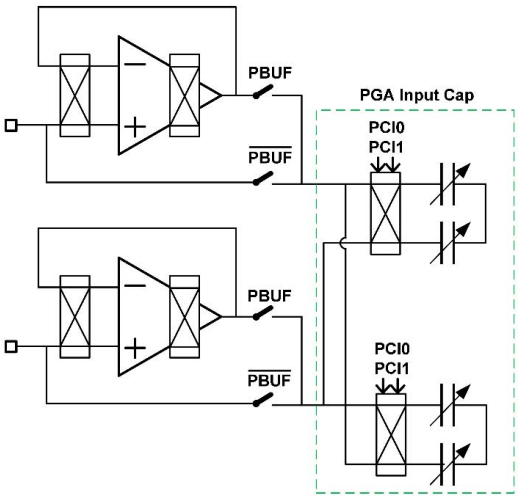

Fig. 8. PGA input pre-charge buffer.

Second, after the AZ phase and while the input pre-charge buffers are still enabled, the first chop phase takes place. Gm2 remains disconnected from Gm1 so C_{FP} and C_{FN} is also pre-charged by Gm2 and the input pre-charge buffers offset is not amplified by the gain network. After the input pre-charge buffers are bypassed, Gm1 and Gm2 are connected together for the final settling. In the second chop phase, Gm2 and the Miller caps are fully chopped.

By combining these two actions, the settling of the first ADC sample after the AZ and chopping event is not degraded. Therefore, the PGA AZ and chop activity becomes transparent to the ADC.

The PGA gain is implemented by the capacitor ratio of $(C_{IP1}+C_{IP2})/C_{FP}$, $(C_{IN1}+C_{IN2})/C_{FN}$. Both input and feedback capacitors are programmed as shown in Table I. The gain settings are 1, 2, 4, 8, 16, 32, 64, and 128 that is flexible for different applications.

B. Input Bias Current Cancellation Circuit

Due to chopping, the input impedance and input bias current are

$$R_{IN} = \frac{1}{2F_{CHOP}\cdot C_{IN}} \tag{8}$$

$$I_{IN} = 2V_{IN}\cdot F_{CHOP}\cdot C_{IN}. \tag{9}$$

For small gain of 1, the full-scale input voltage is 2.5 V. With 16-kHz chopping frequency and 4.48 pF (for Gain = 1) input capacitor, the input bias current is 360 nA that is too high for many sensor applications. To reduce input current, a positive feedback loop (PFL) was proposed in [6] to boost the input impedance. However, due to the uncertainty in parasitic

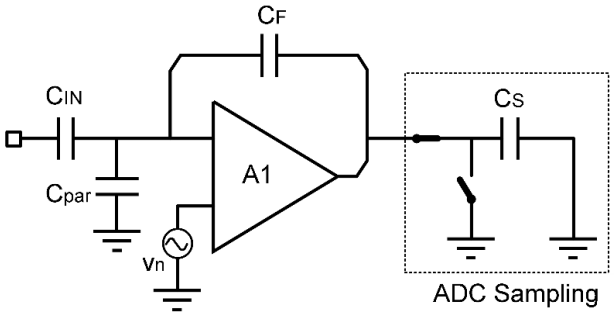

Fig. 9. Noise analysis with parasitic cap and ADC sampling.

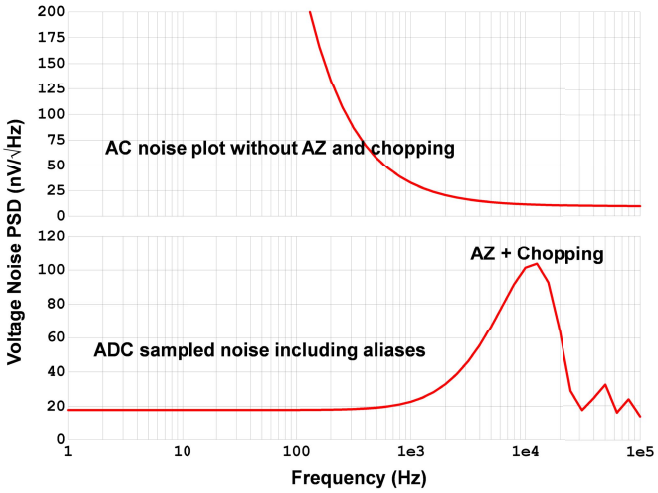

Fig. 10. Simulated input-referred noise result.

capacitance, the input impedance can only be boosted by 3×–10×. And the other issue arises in applications that require frequent channel switching, the input current in the first chop phase after channel switching is not fully cancelled by PFL, resulting in strong kick back to the input.

Two PGA pre-charge buffers are added at the PGA's input for input current cancellation. Each buffer is a rail-to-rail two-stage Class-AB amplifier [20]. The main residual error after pre-charging phase is the pre-charge buffer offset. The corresponding input bias current is

$$I_{IN} = 2V_{OS}\cdot F_{CHOP}\cdot C_{IN}. \tag{10}$$

To reduce the average input current caused by PGA pre-charge buffer offset, the PGA pre-charge buffer is chopped (Fig. 8). Though the average input current is improved, the input still needs to provide dynamic currents in each chopping phase due to PGA pre-charge buffer offset. The pre-charge buffer is only enabled when AZ and chopping actions happen, so its average power consumption is very low.

Though the input current introduced by offset of PGA pre-charge buffer has been cancelled by chopping, the offset can also slow down settling, especially for high gain mode. After AZ phase, the input pre-charge buffers are still enabled for a short while to drive the PGA input cap because of chopping event. While the pre-charge buffer offset will be

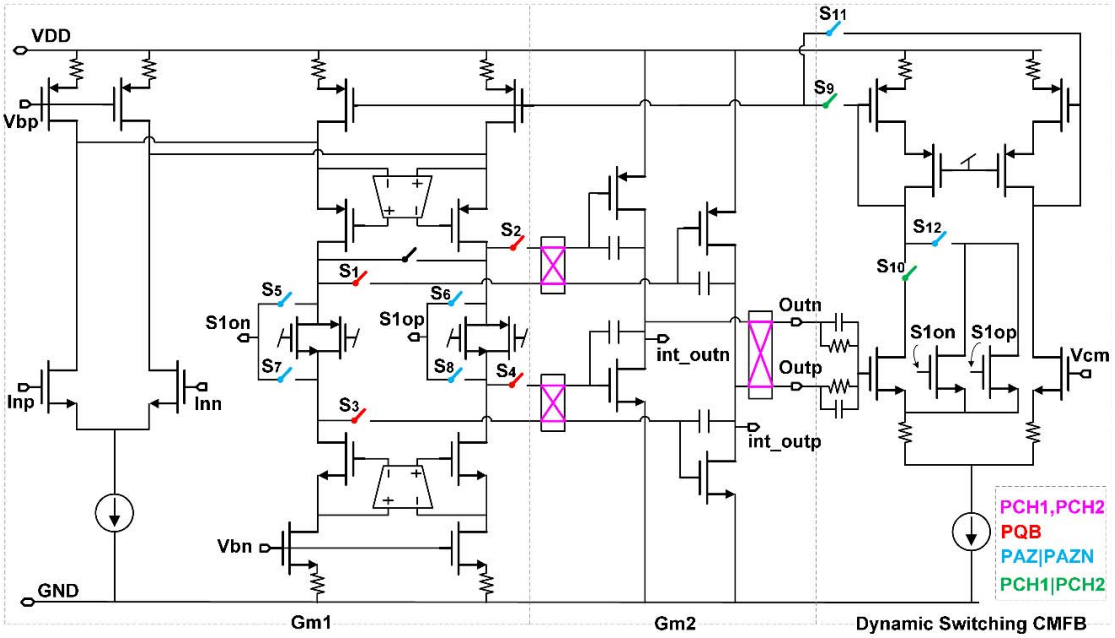

Fig. 11. Circuit diagram of Gm1, Gm2 with reconfigurable CMFB loop.

amplified by the gain network. The total offset for two pre-charge buffers could be 5 mV. For gain = 128, the voltage error at the PGA output is 5 mV*128 = 640 mV. For minimum 2.7-V supply and 2.5-V full-scale output, this error can saturate the amplifier, failing to settle to the accurate value within limited time. That is why after AZ phase and when the input pre-charge buffers are still enabled, Gm2 remains disconnected from Gm1 so C_{FP} and C_{FN} are also pre-charged by Gm2, meanwhile Gm1 output holds the right bias voltage. Gm2 couples back to Gm1 when the input pre-charge buffer is bypassed. So the input pre-charge buffers offset is not amplified by the gain network.

C. Noise Analysis and Design Optimization

Because the PGA input pre-charge buffer is only used when AZ and chopping happen, and ADC only samples data after bypassing input pre-charge buffer, it has no noise contribution. With a proper design, the input-referred noise power spectral density v_{n_RTI} at low frequency is down modulated thermal noise and dominated by the input differential pair of the main amplifier. Considering the ADC sampling effect, v_{n_RTI} is given by

$$v_{n\_\mathrm{RTI}} = \sqrt{\frac{\gamma\, 8\mathrm{KT}}{\mathrm{Gm1}}(1+\alpha)} \cdot \left(1 + \frac{1}{\mathrm{Gain}} + \frac{C_{\mathrm{par}}}{C_{\mathrm{IN}}}\right) \cdot N_{\mathrm{fold}} \quad (11)$$

where γ is a technology dependent coefficient, and α represents the noise contribution from load current sources relative to input pair. Gain is the CGA closed-loop gain ($C_{\mathrm{IN}}/C_{\mathrm{F}}$) and C_{par} is parasitic capacitance at the summing node (see Fig. 9). N_{fold} is the noise folding factor due to switched-cap ADC sampling.

According to this equation, the input-referred noise can be optimized by increasing Gm1, C_{IN} and reducing load current sources noise, parasitic capacitance, and noise aliases.

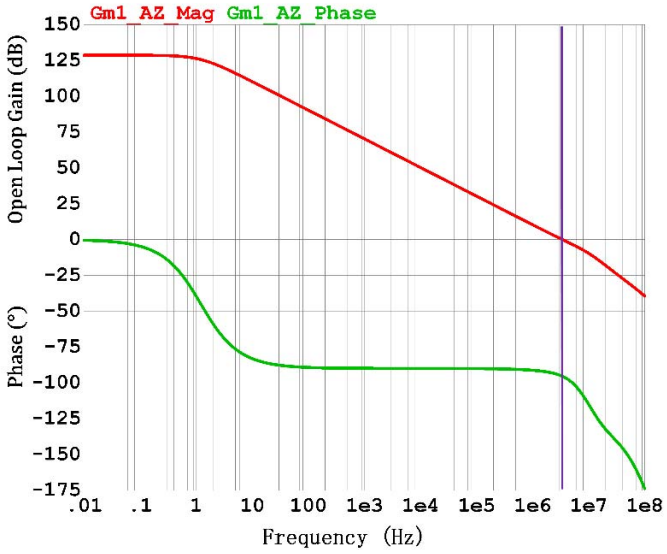

Fig. 12. Simulated ac open loop gain and phase margin of Gm1 in AZ phase.

The input pair consumes 29-μA current that gives transconductance Gm1 = 430 μS. Both NMOS and PMOS load current sources are source degenerated so α is minimized and the input pair is the main noise contributor. The input pair size should be large to reduce the $1/f$ noise. However, the large size also increases parasitic capacitance—$C_{\mathrm{par}}/C_{\mathrm{IN}}$ may become large. Meanwhile, large C_{IN} can suppress the parasitic cap impact on noise. Considering these factors, the parasitic capacitance from input pair in final implementation is 420 fF, with large input capacitor (for gain >= 2), $C_{\mathrm{par}}/C_{\mathrm{IN}}$ is just 1/40. The simulated input-referred noise density at chop frequency is 12 nV/$\sqrt{\mathrm{Hz}}$ (Fig. 10 ac noise plot without AZ and chopping).

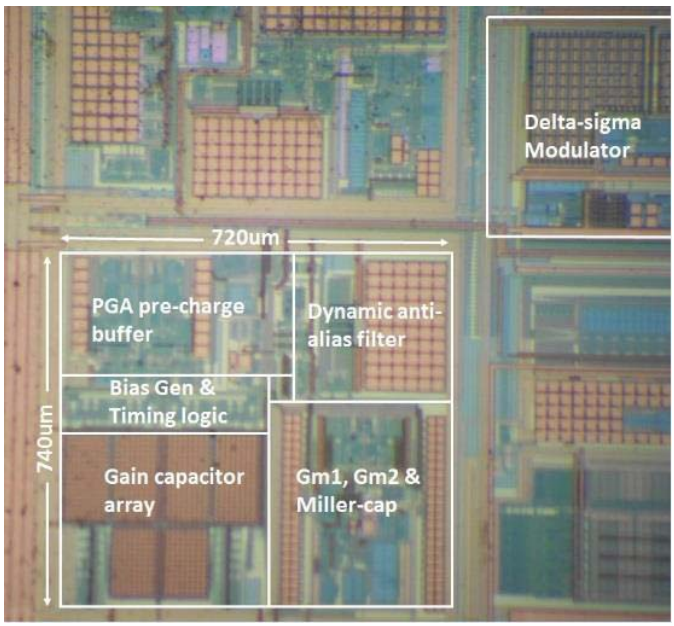

Fig. 13. Die micrograph.

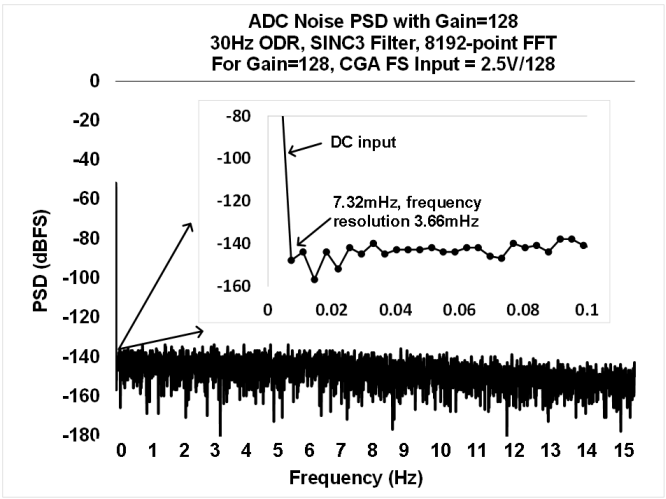

Fig. 14. Measured input-referred noise.

As discussed in Section III, when the CGA drives a switched-cap ADC, there is noise alias due to ADC sampling. ADC pre-charge buffer and DF are employed to improve settling and reduce the folded noise aliases so that N_{fold} of 1.6 is achieved. The input-referred sampled noise spectrum [21] is shown in Fig. 10 where the ADC sampling effect has been considered.

D. Fast Settling Main Amplifier

There is only one critical amplifier in this design that determines the key performance. It consumes 65 μA that is 87% of the total power. The Miller-compensated amplifier formed by Gm1 and Gm2 is shown in Fig. 11. The first stage is gain boosted to achieve high dc gain. Load transistors are source degenerated so the input pair is the main noise contributor. The 45% amplifier current is applied to the input stage

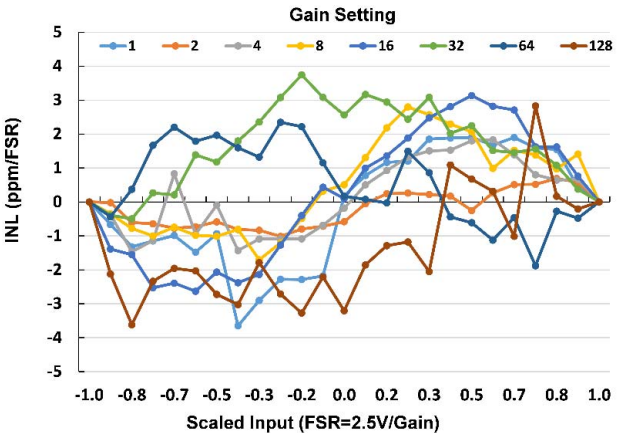

Fig. 15. Measured INL.

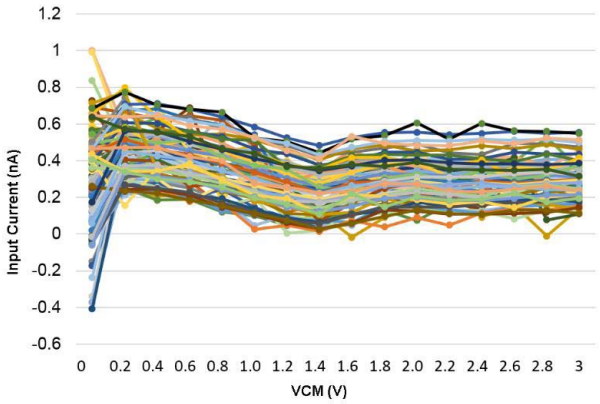

Fig. 16. Measured input bias current.

that gives 430-μS transconductance. The rail-to-rail Class-AB output stage Gm2 with Miller cap is chopped and used to pre-charge the ADC input caps by disconnecting S_{1-4}. The CM feedback (CMFB) circuit changes between the different phases. In amplifying phase, it works as the CMFB circuit of a regular two-stage amplifier (S_{9-10} are on, and S_{11-12} are off). In AZ phase, Gm2 is disconnected and self-biased so that no CMFB circuit is needed, and the CMFB amplifier controls the Gm1 CM voltage (S_{9-10} are off and S_{11-12} are on). Meanwhile, the floating biasing transistors are shorted by S_{5-8} so S1on and S1op become the outputs of Gm1, which is configured as an unity gain amplifier for auto-zeroing. The Gm1 is a single-stage op-amp in AZ phase that is very stable without compensation capacitor. The Gm2 errors like offset, noise is suppressed by high gain Gm1 (Fig. 12). And open-loop dc gain of the whole amplifier with Gm1 and Gm2 together is larger than 140 dB across process corner, voltage and temperature variation so that the linearity error and gain error due to dc gain are well suppressed. The unity gain bandwidth in high gain mode is 4 MHz.

V. Silicon Results

This design has been manufactured in a 0.18-μm CMOS process and occupies 0.53 mm^2 (Fig. 13). The PGA is part of a high precision ADC signal chain that samples the PGA

TABLE II
PERFORMANCE SUMMARY

	This Work	[7]Fan	[10]Wu	[11]Michel	[12]Akita	[14]Sebastiano
Year published	**2017**	2013	2011	2012	2013	2014
Technology (μm)	**0.18**	0.7	0.7	0.13	0.18	0.16
Supply (V)	**2.7-3.6**	20/5	5	1.2	1.5	1.8
Input offset (μV)	**<3.5**	<3	<3	<5	<3.5	<17
Input offset drift (nV/ ^{0}C)	**<70**	-	15	58	25	--
Gain error drift (ppm/ ^{0}C)	**<0.81**	-	<6	40	405	--
Input bias current (pA)	**400**	107	10000*	--	--	--
CMRR/PSRR (dB)	**>109/103**	148/120	127/130	116/108	102/101	99/102
INL (ppm /FSR)	**±5**	-	±4	--	--	--
Gain range	**1~128**	>20	>20	10~1000	>40	13
Quiescent current (μA)	**75**	8	290	31	194	320
Input noise density (nV/√Hz)	**19 (aliased)**	55	17	40	13.5	18.7
Die Area (mm^2)	**0.53**	1.35	5	0.465	0.06	0.07
FOM $e_n^2 \times I_q$ (nV^2/Hz · mA)	**27**	24.2	83.8	49.6	35.4	112

* calculate with 180M Ohm input impedance with 1.8V voltage

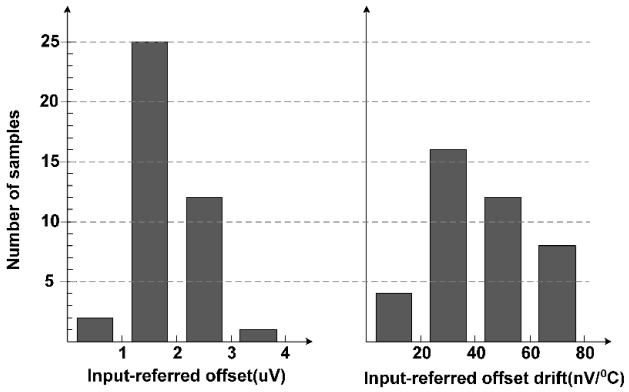

Fig. 17. Measured input-referred offset, offset drift.

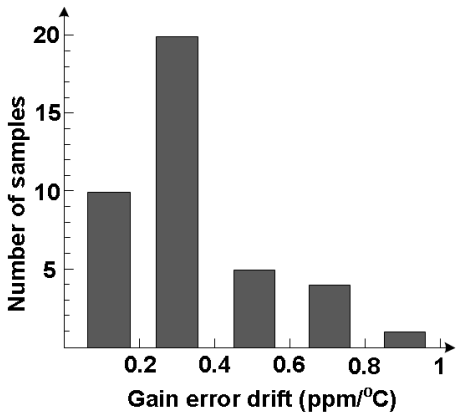

Fig. 18. Measured gain error drift.

output at 256-kHz frequency. The ADC is a 24-bit delta-sigma ADC with typical linearity of 2 ppm/ full-scale range (FSR). The ADC noise referred to PGA input is attenuated by PGA gain so that PGA noise was measured in high gain mode. The measured results show that the input-referred noise density is 19 nV/$\sqrt{}$Hz while drawing 75-μA supply current (see Fig. 14). The noise density is calculated by

$$\text{Noise(rms)} = \text{Noise}(nV/\sqrt{Hz}) \times \sqrt{\text{Unsettled ODR} \times 0.275} \tag{12}$$

where unsettled output data rate (ODR) is 30 Hz, input-referred root mean square (rms) noise is 55 nV, and 0.275 is gain factor of SINC3 filter. This noise density includes the noise folding caused by the ADC sampling inherent to any ADC system. It can be seen that the low frequency $1/f$ noise is well removed. Compared to other amplifier only designs [7], [10]–[12], [14] without noise aliases, this design still achieves an excellent figure-of-merit $27\text{nV}^2/\text{Hz} \cdot \text{mA}$.

The linearity was measured across all gain settings from 1 to 128 for a ±2.5 V/gain input range, and it gives an excellent linearity of 5 ppm/FSR (see Fig. 15). By using PGA input pre-charge buffer, the typical input bias current is reduced to 400 pA as shown in Fig. 16. The temperature range is from −40 °C to 105 °C. Among 40 samples tested, the offset and offset drift are 1.8 μV and 40 nV/°C (typical), and 3.5 μV and 70 nV/°C (worst case), respectively (see Fig. 17). The gain error is calibrated and gain error drift is 0.3 ppm/°C (typical), and 0.81 ppm/°C (max) (see Fig. 18). All the measured results are the signal chain performances that actually includes ADC error contribution. A summary of performance and the comparison with previous published gain amplifiers is presented in Table II.

VI. CONCLUSION

A precision CGA has been implemented in a 0.18-μm CMOS 1.8/3.3 V process. It has a die area of 0.53 mm^2 and consumes 75 μA from 2.7 to 3.6 V supply. It achieves an input-referred noise of 19 nV/$\sqrt{}$Hz, 2-μV offset and 0.81ppm/°C gain error drift. It also integrates the features of

fast CM response and switched-cap ADC driving capability. The fast CM response is obtained by using the CMS scheme. To speed up settling, the Miller-compensated amplifier two stages are split so that the output stage is reused as ADC precharge buffer in the AZ phase and amplify phase, and the input stage performs AZ function in the AZ phase. Dynamic filter is used to reduce the noise folding at the ADC input.

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