A 0.6-V, 0.015-mm^2, Time-Based ECG Readout for Ambulatory Applications in 40-nm CMOS

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***Abstract*— A scalable time-based analog front end in 40-nm CMOS is presented for ECG readout for ambulatory applications. The main challenge addressed is achieving a large dynamic range readout (necessary to handle large signals during motion) in a power and area-efficient manner at low voltage supplies while also tackling the challenges of increase in flicker noise and gate-leakage current. Demonstrated results show a significant improvement in ac-dynamic range without compromising on area (0.015 mm^2) and power consumption (3.3 μW). This paper will be relevant toward developing low-cost, low-power sensor system-on-chips required for wearable biomedical applications.**

***Index Terms*— Ambulatory, analog front end (AFE), biomedical, low area, low voltage, scaled technology, time-based, wearable.**

I. Introduction

SENSOR-SYSTEM-ON-CHIP (sensor SoC) technology is a great enabler for wearable biomedical readout systems that are used in personal healthcare solutions [1]–[4]. As shown in Fig. 1, a typical sensor SoC comprises of an analog-front end (AFE), which reads in multiple physiological signals and converts it into a digital signal. The on-chip DSP processes this signal, which is then transmitted off-chip wirelessly for further processing. Currently, existing research in this field focuses on increasing their functionality while lowering the power consumption and the cost.

For example, in order to reduce the power budget of the system—which is often dominated by the wireless link—data reduction methods like the on-node feature extraction have been proposed [5]. Furthermore, applications requiring advanced signal processing, such as machine learning for patient-specific feature extraction and compressive sampling, are also gaining popularity [6], [7].

Developing low-power, low-cost sensor SoCs is challenging, because at relatively larger technology nodes, such as the 180 nm, the functionality and the power consumption for such digitally intensive applications are limited by the on-chip DSP and the memory power consumption [1]. Although we can reduce the power and the area of the DSP by scaling down in technology and the supply voltage (VDD) [8], the AFE will face significant challenges in scaling down in area, which will lead to an increase in costs.

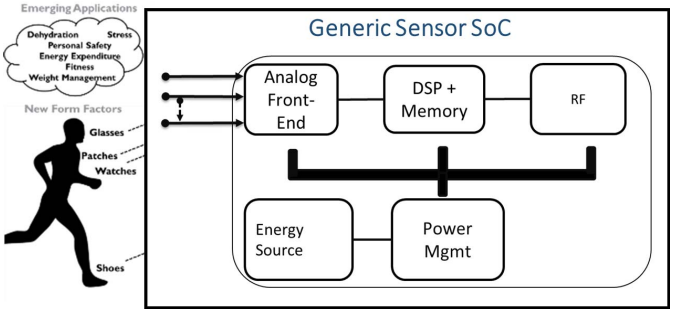

Fig. 1. Generic sensor readout architecture of physiological readout for wearable devices.

The main reason that the AFE does not scale well with technology is the need for large on-chip passives and large transistors. Large on-chip passives are needed to obtain a low kT/C noise and large on-chip time constants. Large transistors are needed to obtain a low flicker noise. The accompanied reduction of VDD further compounds the challenge of obtaining a low area. It will not only reduce the voltage swing, which is especially important for ambulatory applications to handle the large signals during motion [1], [9], but it will also require increasing the area so as to keep the dynamic range constant by lowering the noise floor. For biomedical applications, device noise (thermal noise and flicker noise) usually forms the fundamental limit to the achievable accuracy. Whereas, the maximum input signal is determined by the input signal amplitude and the dc-electrode (DEO) that can be accommodated by the AFE. Hence, in this paper, we refer to dynamic range synonymously with the ac-dynamic range and the DEO-handling capability of the system.

The tradeoff between voltage-supply, area, and dynamic range can be seen in the benchmarking table at the end of this paper. For example, a large dynamic range AFE was presented by [1] but it consumes a large silicon area (along with a 1-μF off-chip capacitor) and functions at a relatively high VDD (1.2 V). An AFE that functions at a low VDD of

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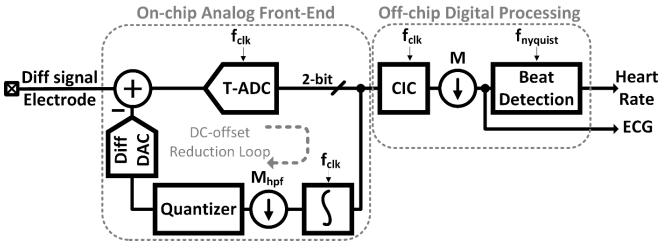

Fig. 2. Proposed time-based analog front-end (T-AFE) architecture.

0.45 V was presented by [10] but it consumes a large silicon area of 0.25 mm^2. An AFE that functions at low VDD (0.5 V) along with a low area consumption of 0.013 mm^2 was presented by [11] but at the cost of a limited input signal range capability (±50-mV DEO and <2-mV$_{pp}$ ac input). Apart from this tradeoff, design in small-scale technology, such as 40-nm CMOS, will introduce additional challenges of increased gate-leakage current and low intrinsic gain [12]. These, especially, will impact the design of instrumentation amplifiers (IAs), which require a high dc-gain and a high input impedance.

To overcome the above challenges, in this paper, we present time-based AFE in 40-nm CMOS for ECG readout, which operates at 0.6 V supply voltage. The readout can handle up to 40-mV$_{pp}$ ac-signal and up to 300-mV DEO offset while consuming 3.3-μW power and 0.015-mm^2 area. Thus, it can accommodate a larger ac-input and a three times larger DEO than the previous works with similar area, similar VDD, and noise performance [11].

Fig. 2 shows the block diagram of the proposed time-based AFE (T-AFE). The input voltage is converted into a 2-b differential digital output via a time-based converter analog-to-digital (ADC) (T-ADC) and then decimated by an off-chip cascaded-integrator-comb (CIC) filter to obtain the ECG signal and the heart-rate information. An on-chip digital dc-offset reduction loop also takes in 2-b digital output and feeds it back to the T-ADC input to reduce the input offset via a 7-b DAC. A key benefit of T-ADC is that its dynamic range is decoupled from VDD, unlike voltage-based ADCs, allowing it to handle larger amplitude signals at low VDD. Furthermore, direct interface of the T-ADC to the sensors enables us to avoid IAs and buffers that do not scale well with technology [12], whereas the mixed-signal feedback avoids large ac-coupling capacitors, saving area [11]. The proposed architecture will enable development of low-cost, low-power sensor SoCs for wearable and personal health applications.

This paper is organized as follows. Section II will present the background on time-based readout. It will then also present the conceptual and the corresponding small-signal analysis of the proposed time-based readout. The architecture of the T-AFE based on the concept and its circuit-level details will be discussed in Section III. Section IV will present the measurement results and the comparison with respect to the state-of-the art (SoA) designs. Finally, Section V will conclude this paper.

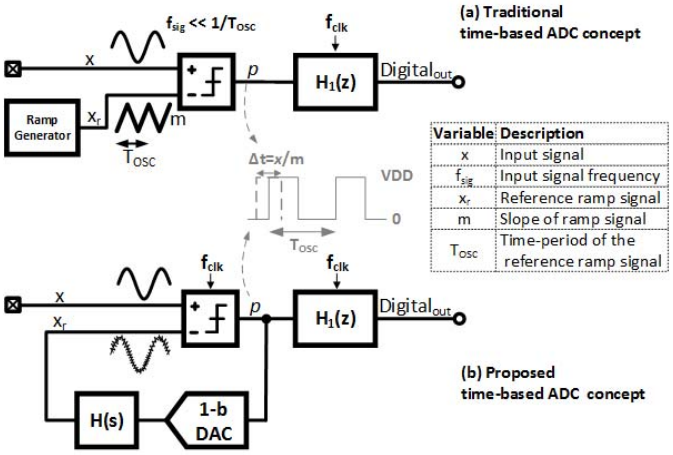

Fig. 3. Conceptual schematic of (a) traditional and (b) proposed time-based operation.

II. Time-Based Operation

A. Background

Time-based processing has emerged in other domains, such as ADCs [13]–[16], filters [17], [18], pixel-readouts [19] to decouple supply voltage and input dynamic range. More recently, time-based techniques have also been used for direct resistive/capacitive-to-digital sensor readouts [20]–[23]. Reference [24] discusses a neural readout using VCO-based readout. A significant challenge of applying existing time-based techniques to a biomedical readout is that the input signal is in voltage-domain and that the block which has to convert this into a time signal will face the same limitations of limited dynamic range as a voltage-based AFE. Hence, the implementation of these techniques is not suited for design in small-scale technology as they use large passives [24], and consume large power [13], [21]–[23] and high-gain blocks [23]. Thus, such architectures are able to demonstrate a low voltage or a large dynamic range operation but without significant improvement in both the area and the power consumption.

To understand this point further, Fig. 3 shows the conceptual diagram of a traditional [13] and the proposed T-ADC. In the traditional concept, the input signal, x, is converted into a time-domain pulse-width modulated (PWM) signal, p, by comparing it to a reference ramp signal denoted by x_r and then converted into a digital value by passing it through a simple digital low-pass filter. For proper operation, the frequency of x_r needs to be much higher than that of x and the comparator should have negligible delay. These requirements lead to a power consuming implementation, because both the comparator and the ramp generator have to handle a large dynamic range at relatively high frequencies (>1 MHz).

B. Proposed Concept

To overcome the above challenges, Fig. 3(b) shows the conceptual schematic of the proposed system. It comprises of a comparator and an integrator, H(s) in the feedback. This is a closed-loop implementation of the traditional time-based

approach and is actually an asynchronous delta modulator [25]. Since the loop is nonlinear, it oscillates at a certain frequency to generate its own reference ramp signal and the output of the comparator is a PWM signal as before. The feedback integrator not only serves to generate a reference signal, it also acts as a gain block for low frequency signals. Hence, at low frequencies, the DC-loop-gain of the feedback loop ensures a virtual ground at the comparator input. Thus, with this scheme, unlike [13], the comparator and the ramp integrator do not have to handle a large dynamic range. This allows us to utilize more power-efficient architectures, such as a dynamic comparator (sample frequency f_{clk}) to implement a low-power, high-speed comparator. The effect of noise folding can be reduced by adding a preamplifier. The output of the comparator is then converted into a digital value by passing it through a digital filter $H_1(z)$. In this paper, the CIC filter (in Fig. 2) implements $H_1(z)$.

The maximum x that can be handled by this loop will depend on two parameters—the voltage that can be accommodated by the integrator H(s) and by the maximum time deviation at the output, i.e., the PWM time period. In addition, the slew rate of the integrator should be larger than the slope of the input signal. The input-referred noise is determined by the noise floor, which comprises of quantization noise and the device noise of the comparator and H(s).

We will use this time-based loop to implement the T-ADC, as shown in Fig. 2. As is the case in all readout designs, the goal of the first stage is to provide a large gain, so that the noise of the following stages—the jitter on the CIC clock in the present architecture—does not affect the noise of the readout. In other words, we have to ensure that the conversion gain from input voltage to output PWM is large. To determine this, we first need to develop a small-signal model for the loop. This is done in Section II-C.

It is worth noting that this is not the only way to close the loop. For a more general analysis regarding the loop, the reader is referred to [14]. However, it is instructive to benchmark this with respect to the one of the other popular ways of doing so—the sigma-delta loop—wherein the integrator H(s) is in the feed-forward path [26]. Although this architecture has the benefit of quantization noise shaping, it places a strict requirement on the design of H(s). It needs a high dc-gain for sufficient suppression of low-frequency quantization noise, which will require large area and will be challenging to design in small-scale technology. However, in the present scenario, this is not the case and as will be seen in Section II-C, a simple charge-pump implementation is sufficient. The quantization noise can be reduced by increasing the clock frequency without any significant power penalty due to the small-scale technology and low voltage operation.

C. Small-Signal Analysis

Before we move on to the small-signal model, we need to define two parameters, the oscillation frequency of the loop and the slope of the ramp, as this will be used later. Furthermore, as will be seen in Section III, these parameters are important for determining the overall area consumption and the noise performance.

Oscillation frequency of the loop is the frequency at which the loop will oscillate when the input $x = 0$. This frequency is given by [14]

$$F_{\text{osc}} = \frac{1}{T_{\text{osc}}} = \frac{1}{4 \cdot t_d} \tag{1}$$

where t_d denotes the total time delay in the loop. Later on, this equation can also be heuristically seen in Fig. 4. The slope of the ramp will be determined by the load capacitance of the feedback integrator, C_p and its bias current, I

$$m = \frac{I}{C_p}. \tag{2}$$

A linear s-domain model for the integrator is well-known. To develop a small-signal model for the comparator, we will use the pseudocontinuous analysis used for linearizing PLL designs [27].

The required transfer function of the comparator can be written as follows:

$$K_T(f) = \frac{p(f)}{x_e(f)} \tag{3}$$

where $p(f)$ and $x_e(f)$ represent the small-signal of the output node and the error node (comparator input), respectively.

To calculate $p(f)$, Fig. 4(a) shows the representative timing waveform of the PWM output and the feedback integrator output for a zero input and a dc input. For a dc input, the PWM waveform will be shifted by Δt, which can be written as

$$\Delta t \approx \frac{x}{m}. \tag{4}$$

This will hold true if the input to the comparator is sufficiently small and that the integrator is ideal [22], [28], [29]. Since the information is in the timing deviation, we can remove the free-running signal information (analogous to the common-mode signal in the voltage-domain operation) for our analysis, as shown in Fig. 4(b). The pulses are Δt wide. To develop a small-signal model, it is important to make a few assumptions in order to linearize the operation. The loop can be linearized if we assume the following $\Delta t \ll (T_{\text{osc}}/2)$ and f.$\Delta t \ll 1$. Using the pseudocontinuous approximation, it can be shown that (Appendix A)

$$K_T(f) \sim \frac{4}{m \cdot T_{\text{osc}}} = \frac{1}{m \cdot t_d}. \tag{5}$$

Although we assumed an ideal integrator for the above analysis, this will never be the case in the real world. Hence, we assume an integrator pole $\omega_{\text{int}} = 1/(Z_{\text{int}}C_p)$, where Z_{int} is the output impedance of the integrator. We just have to ensure that $\omega_{\text{int}} \ll F_{\text{osc}}$, for (4) to be valid. For the purpose of simplicity, we will also assume that the impulse response of the digital filter, $H_1(z)$, is equal to that of the feedback integrator.

Fig. 5 shows the complete small-signal model of the loop. Considering (1)–(5), the transfer function of the gain at the comparator output, p, digital output, dig_{out}, and the

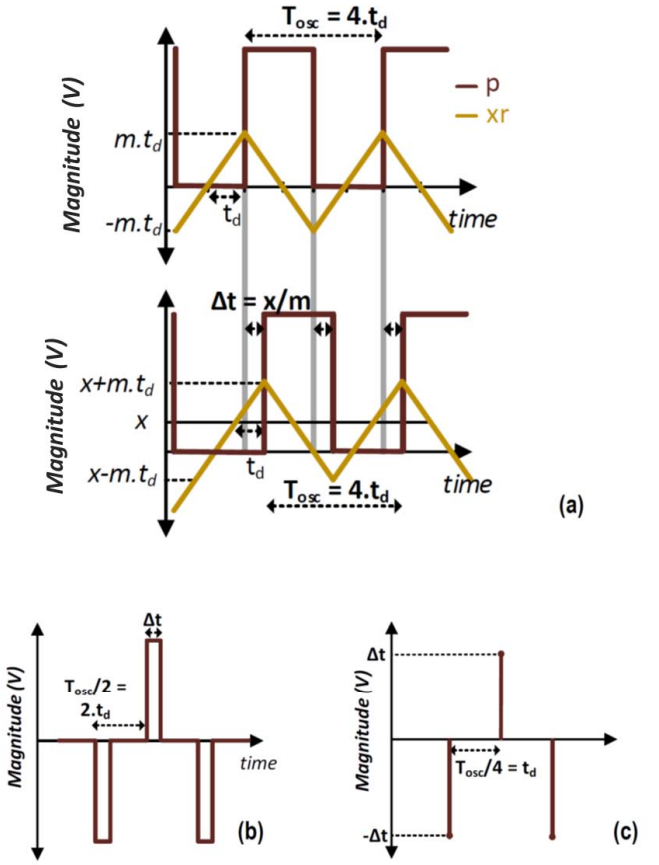

Fig. 4. (a) Representative time-domain signals (b) with common-mode information removed and (c) with the approximation $\Delta t \ll T_{\text{osc}}$.

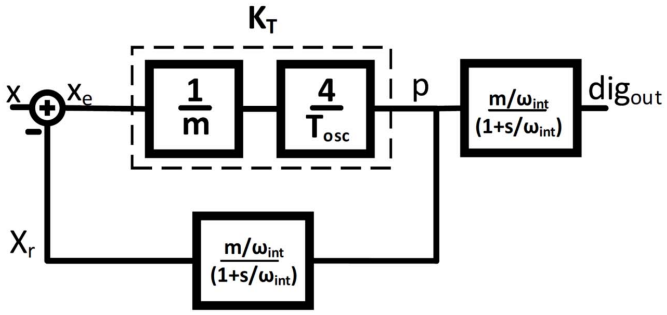

Fig. 5. Small-signal model of the time-based loop.

loop gain, LG, is given by

$$G(s) = \frac{p(s)}{x(s)} = \frac{\frac{4}{mT_{\text{osc}}}}{1 + \frac{4}{mT_{\text{osc}}} \cdot \frac{m/\omega_{\text{int}}}{1+s/\omega_{\text{int}}}} \approx \frac{\omega_{\text{int}}}{m}, \quad \text{for } s \ll \omega_{\text{int}} \tag{6}$$

$$\text{LG}(s) \approx \frac{4}{\omega_{\text{int}} \cdot T_{\text{osc}}}, \quad \text{for } s \ll \omega_{\text{int}} \tag{7}$$

$$D(s) = \frac{\text{dig}_{\text{out}}(s)}{x(s)} = \frac{\frac{4}{mT_{\text{osc}}}}{1+\frac{4}{mT_{\text{osc}}} \cdot \frac{m/\omega_{\text{int}}}{1+s/\omega_{\text{int}}}} \frac{m/\omega_{\text{int}}}{1+s/\omega_{\text{int}}} \approx 1, \quad s \ll \omega_{\text{int}}. \tag{8}$$

Since we do not want large on-chip time constants, we will design for $\omega_{\text{int}} \gg 100$ kHz, whereas the input frequency will be much lower. Hence, we have assumed $s \ll \omega_{\text{int}}$ in (6)–(8). To verify the validity of the models, Fig. 6 plots the simulated and the theoretical transfer function at the output and the loop gain.

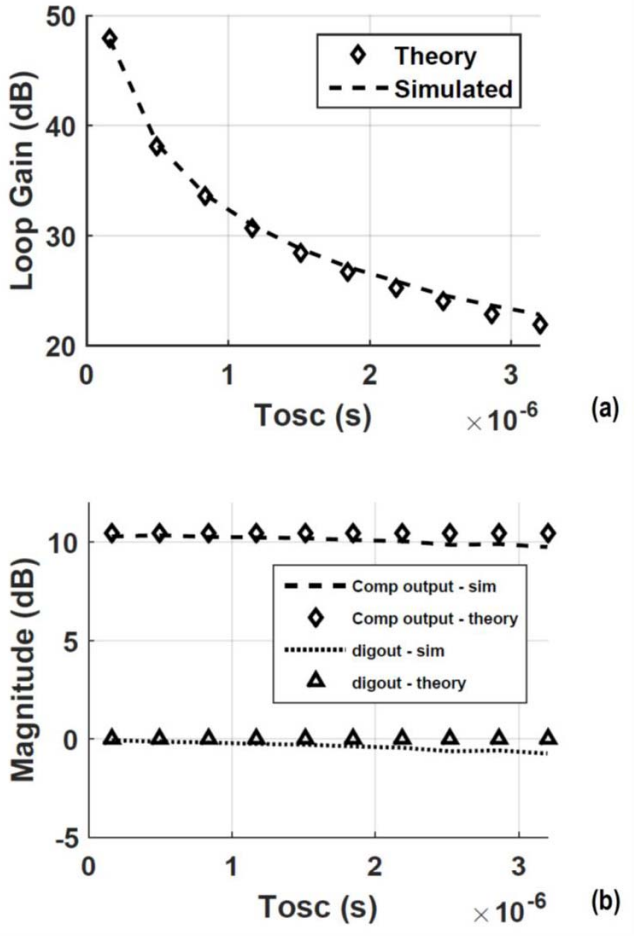

Fig. 6. Theoretical and simulated transfer function of (a) loop-gain versus T_{osc} and (b) gain-versus-T_{osc}.

To analyze the noise performance, Fig. 7 shows the small-signal loop with the major noise sources added—device noise from each of the blocks, $u_{n,\text{comp}}$ and $u_{n,\text{int}}$ (comparator and the integrator, respectively) and the quantization noise of the comparator, q. An inherent assumption in being able to depict the noise voltages as shown is that the noise should be of lower frequency than that of the ramp signal, F_{osc} [28], [30]. This is satisfied in our system due to the presence of the feedback integrator. The effect of clock jitter and noise fold over are not considered as their contribution can be minimized by the use of a differential architecture and an antialias filter, respectively. The total quantization noise will be $T_{\text{clk}}^2/12$, if we can assume a uniform probability density function for the quantization error. The corresponding total input-referred quantization noise will be

$$V q_{\text{in}}^2 = m^2 \cdot \frac{T_{\text{clk}}^2}{12}. \tag{9}$$

This also corresponds well to the quantization noise derived previously in [14]. However, this is the total quantization

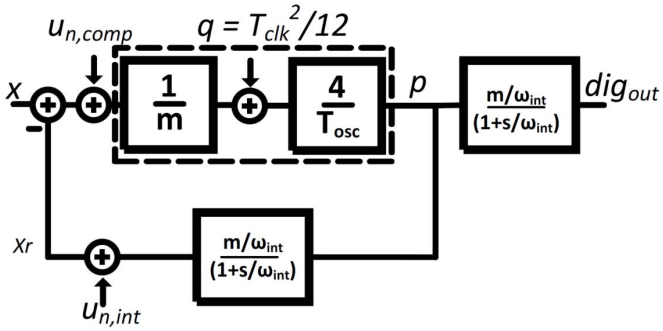

Fig. 7. Small-signal model with relevant noise sources.

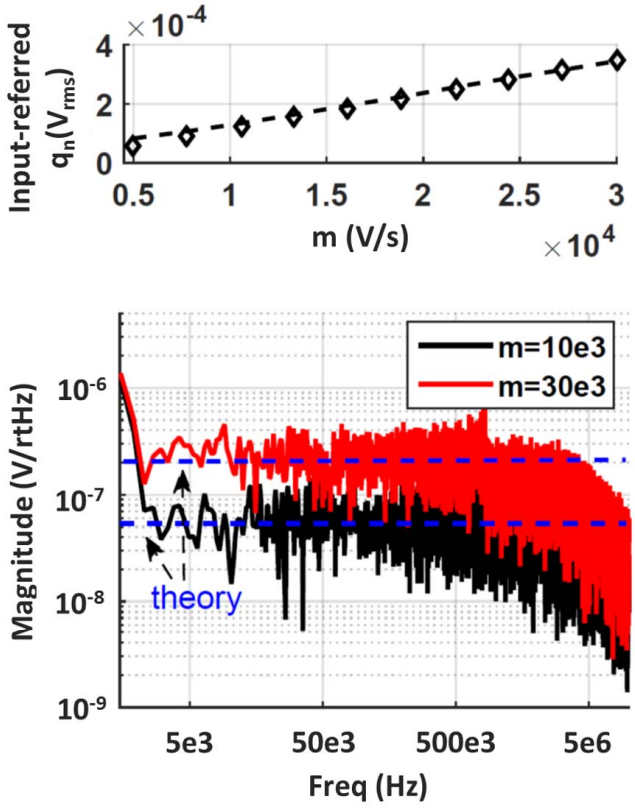

Fig. 8. Theoretical and simulated (a) input-referred total quantization noise and (b) noise-density floor.

noise in a bandwidth of $F_{\rm clk}/2$ bandwidth, whereas, we are generally interested in the total quantization noise for a much smaller bandwidth. To calculate this, we will first determine the quantization noise floor and then multiply it by the required signal bandwidth later on. This is given by (Appendix B)

$$S_{\rm qin}^2 = m^2 \cdot \frac{T_{\rm clk}^2}{12} \cdot \frac{1}{F_{\rm osc}}. \tag{10}$$

To validate the above equations, Fig. 8 plots the simulated and the theoretical values of $V_{\rm qin}$ and $S_{\rm qin}$.

As for the loop stability, since the integrator, H(s), is the only dominant low-frequency pole in the loop, the loop will be stable (as long as the linearizing assumptions in the previous analysis hold true).

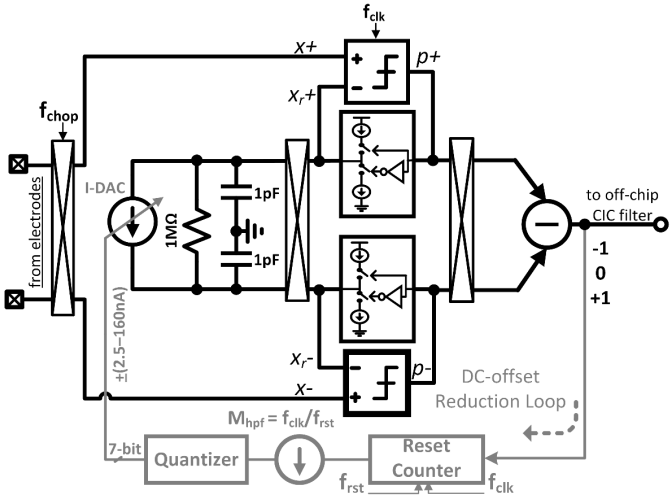

Fig. 9. Block-level architecture of the T-AFE.

III. Implementation of Time-Based AFE

A. Architecture

Fig. 9 shows the system-level view of the time-based AFE. It comprises of a pseudodifferential time-based ADC with a dc-offset reduction loop in feedback. Each pseudodifferential stage of the time-based ADC comprises the time-based loop presented earlier. The integrator H(s) is implemented by a simple charge-pump, with a current $I_{\rm cp}$ and capacitor C_p. The 1-b PWM comparator outputs are digitally subtracted and sent off-chip for further processing. A differential resistance of 1 MΩ is implemented in the feedback. The reasons for this are discussed later.

The 2-b digital output is also used to implement the digital dc-offset reduction loop to handle the DEC offset. This loop comprises of a digital integrator that acquires the dc-information (<1 Hz) from the 2-b output. The digital integrator is implemented as a reset integrator with reset frequency, $f_{\rm rst}$. This is then followed by a 1.5-b quantizer, which determines the sign of the DEO, which is then used to accordingly increment/decrement the estimated offset. This is done by a 7-b accumulator and a 7-b binary-weighted current DAC. Once, the estimated offset is within 1-LSB (or 2.5 mV) of the actual DEO, the feedback loop shuts off as the output of the 1.5-b quantizer will be 0. Although a higher resolution than 7-b can be designed, the area consumed by the DAC will also increase. Thanks to the time-domain operation, the T-AFE does not saturate in the presence of 2.5-mV offset.

Determining the value of slope of the ramp, m (2), is one of the key design decisions as it will determine the overall noise, area, and the power consumption of the system. Ideally, to have a low input-referred quantization noise (10), the value of m should be as small as possible (as long as it satisfies the slew-rate requirements of the input signal). However, that will also require large capacitors or small charge-pump currents—both of which are undesirable, because it will require large area and a small ac-dynamic range ($I_{\rm cp} \cdot R$), respectively. On the other hand, the value of m cannot be too large as a

high-frequency comparator clock will be required to keep the quantization noise low (10). Keeping these points in mind, we choose $m = 30 \times 10^3$ V/s, which is implemented with a charge-pump current $I_{\rm cp} = 30$ nA and $C_p = 1$ pF.

The chopping frequency, $f_{\rm chp}$, is 6 kHz and the clock frequency, $f_{\rm clk}$, is 25 MHz. The delay in loop, for this implementation, is ∼one clock-cycle delay, which gives $F_{\rm osc} = 6.25$ MHz. Given these values, the loop gain of each of the stages will be 12.5. Increasing the loop-gain further will require larger area, because the integrator time constant will need to be increased.

The differential resistance of 1 MΩ has been implemented to address two key design concerns of a pseudodifferential architecture: 1) the noise of the feedback stage $u_{n,\rm int}$ and 2) the common-mode swing at the output of the comparators. The noise of the feedback arises from the noise current of the charge pump and also the noise-current of the current DAC. We are interested in the voltage noise at the feedback node, which is given by $i_n^2 \cdot Z_{\rm int}^2$, where $Z_{\rm int}$ is the output impedance of the integrator. If the integrator is ideal, $Z_{\rm int} >$ inf, leading to a large $u_{n,\rm int}$. By implementing a resistance, the current-noise is shunted, leading to a lower $u_{n,\rm int}$. Although doing so will add an additional resistor noise, the overall architecture noise is not significantly increased, as will be seen later. For the common-mode signal that is input from the electrodes, each stage, due to negative feedback, will make a copy of the common-mode signal at their respective feedback nodes. Since the resistance is implemented differentially, it will act as an open for the common-mode signal. From (7), we can see that this will lead to a higher loop gain than for the differential signal, since now the time constant at the feedback node will be determined by the output impedance of the current sources of the charge-pump integrator, which will be ideally much higher than 1 MΩ. This will lead to common-mode swing suppression at the output.

The offset that arises due to the mismatch between the two pseudodifferential stages will be chopped out. It will not be reduced by the dc-reduction loop as the loop appears outside the chopper switches. This offset just has to be low enough not to saturate the charge-pump integrator. This is ensured by following symmetrical layout techniques both at the circuit- and the system-levels [31].

In Section III-B, we will discuss the transistor-level design of the comparator.

B. Block-Level Design Comparator

The key design specifications of the comparator are that it should have a high input impedance, high speed, low noise, and low-power consumption. Fig. 10 shows the transistor-level schematic of the implemented comparator to achieve this objective. It comprises a preamplifier followed by dynamic latch stages. The dc-gain of the preamplifier need not be high and should be just enough to suppress the nonidealities of the latches, such as charge injection, noise, and offset. For this purpose, a preamplifier gain of 20 will be sufficient. The preamplifier also acts as an inherent antialias filter to get rid of noise-folding effect. Since we want a high input impedance,

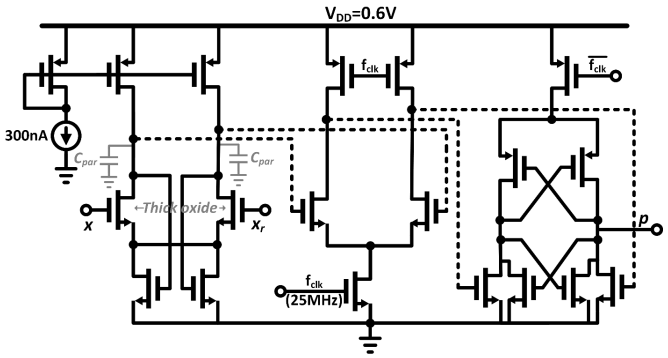

Fig. 10. Transistor-level schematic of the comparator.

the input transistors need to be small and have negligible gate-leakage current. Gate-leakage current can also be problematic in terms of noise as the corresponding current noise can flow into large electrode impedances to generate a large voltage noise. Thick-oxide transistors are used for the input transistors to eliminate the gate-leakage current. A drawback of using thick-oxide transistors is that their threshold voltage is high (0.55 V for this technology) and thereby reduces the maximum signal swing that can be handled by the input stage. Thanks to fact that we do not need a high dc-gain, a simple differential amplifier, which stacks just three transistors between the rails, can be used and hence, allowing the input stage to handle a large signal swing even at 0.6 V supply (170 $\rm mV_{pp}$; 150-$\rm mV_{pp}$ offset + 20-$\rm mV_{pp}$ input signal). A bias current of 300 nA is chosen to satisfy both the noise and the gain requirements of the preamplifier.

We implement a split tail-current source circuit for the common-mode feedback (CMFB), since they take lesser area compared with conventional structures like the resistive CMFB and the switched-capacitor CMFB. The tail current-source transistors have to be sized such that they remain in saturation for the required common-mode range.

C. System Noise Calculation of the T-AFE

The total input-referred noise density of the T-AFE can be written as

$$S_{n,\rm tot}^2 = 2\left(S_{n,\rm comp}^2 + S_{n,\rm int}^2 + S_{\rm qn}^2\right). \tag{11}$$

The noise of the comparator will be determined mainly by the thermal noise of the preamplifier, and the noise of the feedback will be determined by the resistor noise. Therefore, we can write

$$S_{n,\rm tot}^2 \approx 2\left(2\frac{4kT\gamma}{g_{m,\rm preamp}} + 4kTR/2 + m^2.\frac{T_{\rm clk}^2}{12}.\frac{1}{F_{\rm osc}}\right) \tag{12}$$

where k is Boltzmann's constant, γ is the noise coefficient, and $g_{m,\rm preamp}$ is the transconductance of the input-MOS pair of the preamplifier. In this technology, this is equal to 7.2 μs for a bias current of 300 nA. Assuming one clock-cycle delay, and substituting values from the previous analysis, $S_{n,\rm tot} \approx 300$ nV/rtHz.

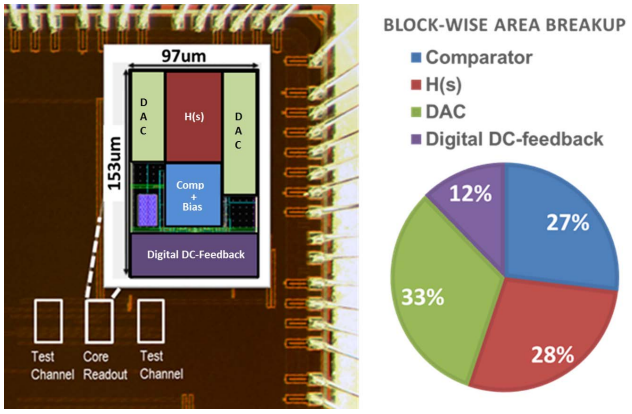

Fig. 11. Chip photograph with layout overlay and the corresponding blockwise area breakup.

The noise of the charge-pump integrator and the current-DAC will be much lower than the resistor noise and is hence ignored in the above calculation. At higher offsets, though, the noise of the current-DAC will increase and thereby determine the feedback noise. This will lead to a slight increase in the input-referred noise.

IV. Measurement

The prototype design is implemented in 40-nm TSMC GP (general purpose) process. Fig. 11 shows the chip photograph along with the layout overlay. The design utilizes an active chip area of 0.015 mm^2 (97 μm $\times$ 153 μm). This also includes the complete T-AFE along with the digital dc-reduction loop and the current-DAC. Fig. 11 also shows the blockwise breakup of the area utilization. It is divided roughly equally between the current-DAC, charge-pump integrator, and the comparator. From this, we can see that increasing either the DAC resolution, or the charge-pump capacitance, C_p, would have led to a lower DEO and input-referred quantization noise, respectively, and it would also increase the overall area.

The design consumes a power of 3.3 μW from a 0.6 V supply voltage. The comparators consume 1.6 μW of power, which is divided roughly equally between its static and the dynamic power components. Interestingly, the rest of the overall power consumption originates from the static gate-leakage current of the reset integrator in the digital dc-reduction loop.

Fig. 12 shows the input-referred noise spectrum of the T-AFE. As expected, the flicker noise is eliminated due to the use of chopper switches. The thermal noise floor is 0.6 μV_{rms}/rtHz, which translates to a total noise of 7.8 μV_{rms} in a bandwidth of 150 Hz. The discrepancy between the theoretically calculated value and the measured noise is because the capacitance at the comparator output is larger than the simulated value, leading to a higher delay than the expected ~one clock-cycle delay. At higher offsets, the noise will increase slightly due to increase in the current from the current-DAC. However, this value is still within the range required by the application [32]. The accuracy required for the digital CIC filter clock can be obtained by transforming this noise to the output. This will be <200 ps_{pp}, which is well within the range required by a standard digital circuit [33].

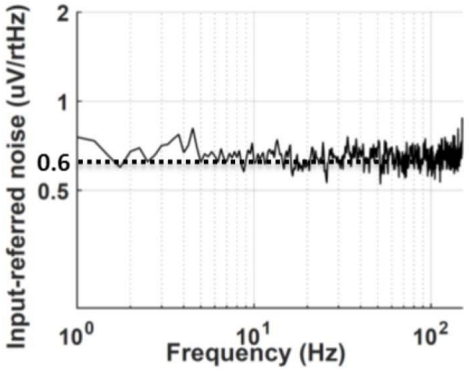

Fig. 12. Input-referred noise of the T-AFE.

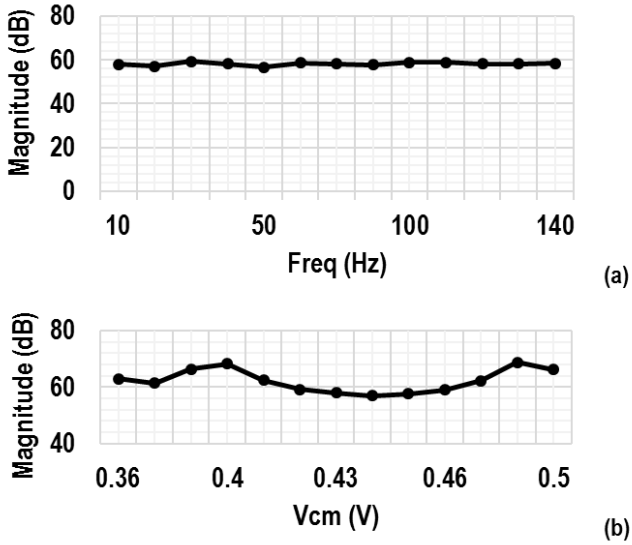

Fig. 13. Measured CMRR of the T-AFE. a) CMRR-vs-frequency b) CMRR-vs-V_{cm}.

Fig. 13(a) plots the CMRR-versus-frequency for the T-AFE. We achieve ~60-dB CMRR for the entire bandwidth. The CMRR increases to 70 dB by changing the common-mode voltage (V_{cm}), as shown in Fig. 13(b). The reason CMRR changes with respect to V_{cm} can be explained as follows. Change in the input common-mode voltage will lead to change in the impedances of the transistors of the comparator (input pair, current sources), transistors of the charge-pump integrator (current sources), and the current-DAC. This will affect the matching between the transistors and thus lead to slightly different loop characteristics for each pseudodifferential stage due to change in time delay, t_d, and the slope m and hence a change in the CMRR. Fig. 14 plots the transient response for a 5 mV_{pp} at 11-Hz input signal. This input signal is chosen, as generally, this is the maximum ECG signal that one can expect. As can be seen, we achieve an SFDR of 56 dB.

Fig. 15 shows a sample ECG recording obtained from the test chip with the subject at rest. To further verify the large-signal capability, the system is evaluated by acquiring an ECG signal from the noise-stress database [34]. The system does not saturate and maintains good beat detection capability even in the presence of motion.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH SoA

	[11] ISSCC '11	[1] ISSCC '14	[35] JSSC '11	[36] ISSCC '10	[10] ISSCC '13	This Work
Technology (nm)	65	180	65	130	180	40
Voltage Supply (V)	0.5	1.2	1	0.8-1	0.45	0.6
DEO (mV)	±50	±400	50	AC-Coupled	AC-Coupled	±150
ACInput signal	<1.7 mV_{pp} *	30 mV_{pp}	10 mV_{pp}	<8mV_{pp}	2.25mV_{pp} *	40 mV_{pp}
Area (mm^2)	0.013	>1.48 + 1µF off-chip	0.2	1.54	<0.25	0.015 + off-chip digital filter
Power (µW)	5	~50	2.1	<20	0.94	3.3
Input Impedance	(Pseudo-resistor)	> 500 MΩ	30 MΩ	(AC-coupled) <150MΩ	N/A	~50 MΩ
Integrated Noise (μV_{rms})	7.4 * (1Hz-150Hz)	0.612 (0.5Hz-150Hz)	10 * (1Hz-150Hz)	14 (100-6.3KHz)	3.2 (1-10kHz)	7.8 (offset < ±50mV) 20 (offset < ±150mV) @ (1Hz-150Hz)
Bandwidth (Hz)	300	150	500	6.3K	10K	150
CMRR (dB)	75	>110	134	59	73	60
THD	2% @ 0.6mV_{pp} input	0.6% @ 35mV_{pp} input	N/A	<0.4% @ 2mV_{pp}	N/A	1 %@ 40mV_{pp} input
Application	Neural (LFP)	ECG	Mainly WSN	EEG	EEG	ECG
Remarks	AFE	AFE	Only IA	AFE	AFE	AFE

*extrapolated

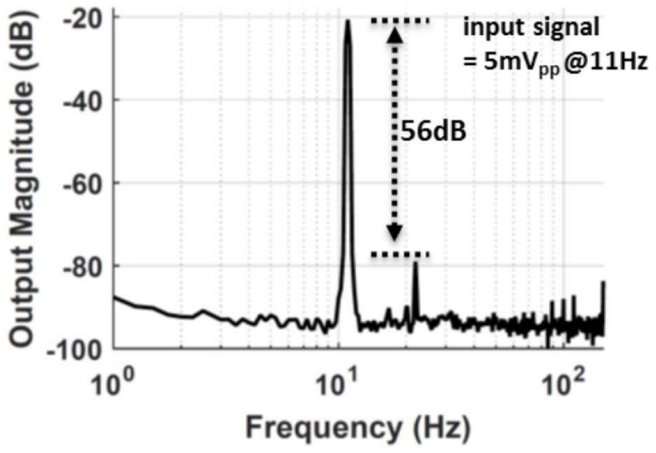

Fig. 14. FFT of the PWM comparator output.

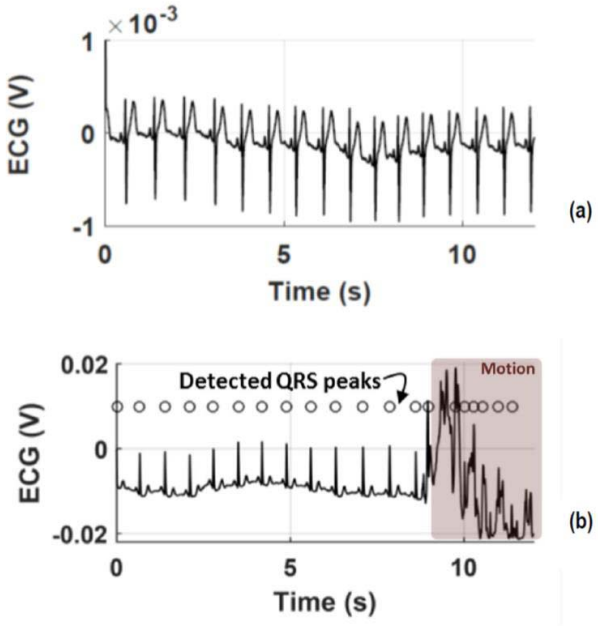

Fig. 15. ECG (a) with the subject at rest and (b) with motion-noise added [34].

Table I summarizes the performance of the T-AFE with respect to the SoA designs. The proposed AFE can handle an increase in ac dynamic range of input signals while keeping the VDD and the area very low. The area and the power consumption of the off-chip digital filter is not included, since the target applications for this AFE implementation require digitally intensive SoCs, we can assume that an on-chip DSP is available. Therefore, the off-chip digital filter

will not significantly add to the total system area and power consumption. The integrated noise of the proposed T-AFE is comparable with other low-area designs [11], [35]. Although the integrated noise increases with increase in the DEO, it is within acceptable biomedical signal acquisition limits. The power consumption, too, is comparable with SoA. The measured CMRR of the T-AFE is 60 dB and increases to 70 dB on changing the input common-mode voltage. The CMRR can be increased in future by improving the matching between the two pseudodifferential stages.

V. Conclusion

Emerging applications in wearable and personal healthcare applications require low-cost and low-power sensor SoCs, while also improving their functionality. This requires design of SoCs in small-scale technologies to take advantage of power-efficient computation. However, due to the accompanied VDD reduction and the need for large on-chip passives, the traditional voltage-based AFE architectures do not scale well with technology. This will, thereby, lead to a decrease in dynamic range and increase in costs. Other technological challenges, such as decrease in the intrinsic gain of the transistor and the increase in gate-leakage current, further compound this challenge.

We propose a time-based approach to overcome the challenge of maintaining a large dynamic range while operating with a low VDD. Utilizing a negative-feedback approach allowed us to implement scalable and power-efficient blocks, such as the dynamic comparator, while getting rid of the need for high-gain blocks. Furthermore, a digital dc-reduction loop was implemented to get rid of large on-chip passives.

In this paper, small-signal, linearized equations were first derived for the proposed T-AFE concept and then later used to optimize the design for a prototype ECG readout for an ambulatory application in 40-nm CMOS. The measured results show a significant improvement, in terms of area and power consumption while accommodating a large dynamic range, with respect to the SoA designs. The proposed architecture is not only promising for enabling low-power, low-cost sensor SoCs but it also opens further avenues for <40-nm AFE design.

Appendix A
Derivation of the Comparator Small-Signal Model

If we assume that $\Delta t \ll (T_{\text{osc}}/2)$, then the time period of pulse arrival is approximately $T_{\text{osc}}/2$. Using the pseudo-continuous approximation, as illustrated by [27], we can write

$$p(f) \approx \frac{1}{T_{\text{osc}}/2} \cdot \{2\Delta t(f)\text{sinc}(\pi f \Delta t(f))\}. \tag{A.1}$$

The "sinc" term denotes the Fourier transform of a pulse. Fig. 4(c) represents the waveform after this approximation.

The frequency transform p(f) is still nonlinear, and we have to make one more approximation to linearize it. We will assume that $f \cdot \Delta t \ll 1$. This is valid due to our assumptions that the ramp frequency, F_{osc}, has to be higher than the input frequency and that $\Delta t \ll (T_{\text{osc}}/2)$. Thus

$$p(f) \sim \frac{(2 \cdot \Delta t(f))}{T_{\text{osc}}/2}. \tag{A.2}$$

Substituting (A.2) and (4) in (3), we get the required linear model

$$K_T(f) \sim \frac{4}{m \cdot T_{\text{osc}}} = \frac{1}{m \cdot t_d}. \tag{A.3}$$

Appendix B
Quantization Noise Density Floor

To calculate the input-referred quantization-noise floor, we will observe the quantization-noise floor at the feedback node (or the integrator output node). For a properly designed loop with a large loop gain, the quantization noise at this node can be assumed to be equal to the input-referred quantization noise.

We also observe that since there is only one dominant pole in the loop (the integrator pole), we can assume that the quantization noise density should be flat at low frequencies (assuming a sufficiently busy signal) and roll-off at 20 dB/decade at $f = f_{\text{loopBW}}$, where f_{loopBW} is the loop bandwidth. Therefore, the quantization-noise floor, S_{qin}, can be written as

$$S_{\text{qin}}^2 \cdot \frac{\pi}{2} \cdot f_{\text{loopBW}} \approx m^2 \cdot \frac{T_{\text{clk}}^2}{12} \tag{B.1}$$

f_{loopBW} can be derived from (6) and is given by

$$f_{\text{loopBW}} = \frac{4 \cdot F_{\text{osc}}}{2\pi}. \tag{B.2}$$

Substituting (B.2) in (B.1), we get

$$S_{\text{qin}}^2 \approx m^2 \cdot \frac{T_{\text{clk}}^2}{12} \cdot \frac{1}{F_{\text{osc}}}. \tag{B.3}$$

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