

A 76- to 81-GHz Multi-Channel Radar Transceiver

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Abstract—This paper presents a packaged 76- to 81-GHz transceiver chip implemented in SiGe BiCMOS for both long-range and short-range automotive radars. The chip contains a two-channel transmitter (TX), a six-channel receiver (RX), a local-oscillator (LO) chain, and built-in self-test (BIST) circuitry. Each transmit channel includes multiple variable-gain amplifiers and a two-stage power amplifier. Measured on-die output power per channel is +18 dBm at 25 °C, decreasing to +16 dBm at 125 °C. Each receive channel includes a current-mode mixer, followed by intermediate-frequency buffers. At 25 °C, measured on-die noise figure is 10–11 dB, conversion gain is 14–15 dB, and input 1-dB compression point exceeds +1 dBm. An integrated LO chain drives the transmit and receive chains and includes an 18.5- to 20.6-GHz voltage-controlled oscillator connected to cascaded frequency doublers and a divide-by-four prescaler. At 25 °C, measured phase noise is -100 dBc/Hz at 1-MHz offset from a 77-GHz carrier. Integrated BIST circuits enable the measurement of signal power, RX gain, channel-to-channel phase, and internal temperature. The chip is flip-chip packaged into a ball-grid array and extracted interconnect loss for the package is 1.5 to 2 dB. Total power consumption for the chip is 1.8 W from 3.3 V for a single-TX, six-RX mode.

Index Terms—77 GHz, built-in self-test (BIST), radar, SiGe, transceiver, W-band.

I. INTRODUCTION

HIGH-PERFORMANCE, low-cost frequency-modulated continuous-wave (FMCW) radar sensors enable advanced driver-assistance systems in vehicles [1]. Multi-mode sensors which support both long-range radar (LRR) at 76 to 77 GHz and short-range radar (SRR) at 77 to 81 GHz can avoid the need to install separate radar solutions for each application [2]. These multi-mode radar sensors must achieve high saturated output power (P_{sat}) in the transmitter (TX) to enable long-range sensing, high dynamic range in the receiver (RX) to avoid linearity degradation due to near-in reflections, low phase noise in the voltage-controlled oscillator (VCO) to enable the detection of distant reflected signals, and wide tuning range in the VCO to enable

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high-resolution sensing at short range. Furthermore, multiple RX channels are needed to enable accurate angle-of-arrival measurements, whereas multiple TX channels can be used to support diverse transmit antennas. Radar performance metrics must be met across process, voltage, and temperature (PVT) and the packaging of the radar should have minimum degradation to the overall performance. Additional system-level analysis of 77-GHz automotive radar sensors can be found in [2].

The above requirements can be met by integrating multiple RX and TX elements into a single chip implemented in advanced silicon technology. Recently, both unpackaged and packaged radar transceiver chipsets have been published in SiGe and CMOS [3]–[13] which demonstrate high levels of RF performance. In many of these examples, the TX and RX were implemented as separate chips [3]–[8], simplifying thermal management, improving isolation, and allowing for system-level scaling to larger array sizes through incorporation of more chips at the board level. However, a fully integrated single-chip transceiver having higher element counts and reduced power consumption per element can simplify system design and reduce cost.

In this paper, we present a single-chip 76- to 81-GHz transceiver with a two-channel TX and a six-channel RX for automotive radar. The chip supports both LRR and SRR modes, through wideband optimization of both RX and TX and incorporation of a VCO which can support wide tuning for SRR and low phase noise for LRR. Furthermore, embedded built-in self-test (BIST) circuitry allows for functionality checks and calibration of the overall system. This paper is an extended version of our work presented in [14], and a second generation of the chipset is presented in [7], where our prior chipset had separate RX and TX chips, reduced RF performance, and fewer BIST capabilities. This paper is organized as follows. Section II describes the system architecture and the building block design for local-oscillator (LO), TX, and RX subsystems. Section III presents the evaluated chip-level performance of the transceiver, and Section IV presents the package design and measurement results.

II. TRANSCEIVER DESCRIPTION

A. Block Diagram

The radar system is partitioned into two main components—a millimeter-wave (mm-wave) transceiver chip and a separate CMOS signal-processing chip. A block diagram of the transceiver is shown in Fig. 1. This transceiver includes an LO chain, a two-element TX array, a six-element RX array, and BIST circuitry. The CMOS signal-processing chip is not discussed here, but would contain remaining portions of

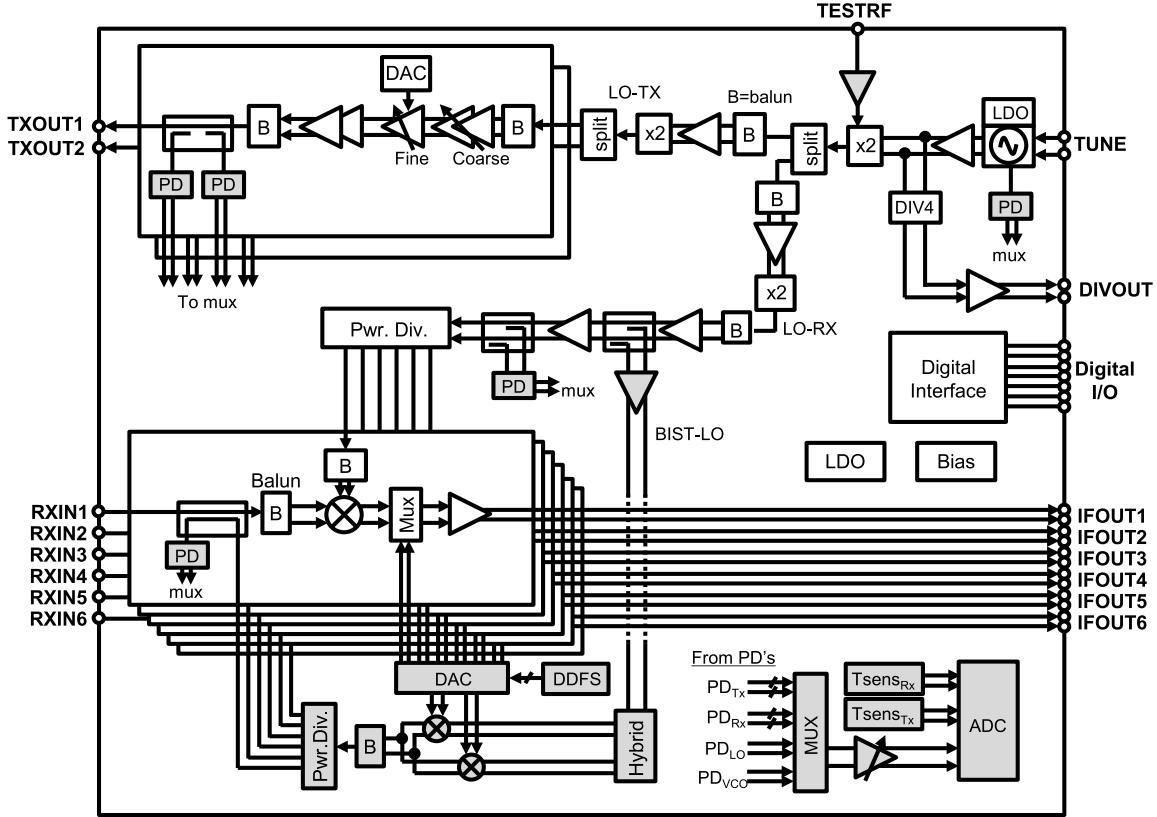


Fig. 1. Block diagram of the transceiver chip having two transmit channels, six receive channels, an LO network, and BIST (shaded in gray).

a frequency synthesizer for FMCW signal generation along with analog and digital baseband circuitry for the RX array. In this paper, we present the mm-wave transceiver, which has been implemented in a 130-nm SiGe BiCMOS 8HP technology from GlobalFoundries. The chip is designed for robust operation across PVT, namely, -40°C to $+125^{\circ}\text{C}$, 3 to 3.6V power supply variation, and all process corners.

B. LO Chain

The LO chain is built around a single 18.5- to 20.6-GHz VCO which covers the full SRR tuning range and targeting a phase noise lower than -112 dBc/Hz at 1-MHz offset for LRR operation (equivalent to -80 dBc/Hz at 100-kHz offset from a 77-GHz carrier). The VCO output is doubled to 40-GHz range¹ and then split to feed both the TX and RX arrays, where the LO signal is doubled once again to 80-GHz range. LO buffers are used at each step along the chain to guarantee sufficient power levels across PVT.

The VCO employs a differential Colpitts topology to achieve 18.5- to 20.6-GHz tuning range with low phase noise throughout the band. This corresponds to radar operation over 74 to 82.4 GHz, providing additional margin for the system. A simplified schematic of the VCO is shown in Fig. 2 [15]. A differential transformer-coupled tank is used to support wide

tuning range, reduce supply pushing in the VCO, and suppress noise conversion from amplitude domain to phase domain within the oscillator. The VCO has two modes, as follows: a narrowband LRR mode for coverage of 76 to 77 GHz in which smaller varactors (C5, C6) are used, and an ultra-wideband (UWB) SRR mode for coverage of 77 to 81 GHz in which additional varactors (C7, C8) are switched into the tank. In either mode, phase noise remains low at approximately -112 dBc/Hz at 1-MHz offset from the 18.5- to 20.6-GHz carrier. The VCO control voltages are provided from an off-chip synthesizer, with either single-ended or differential tuning possible. Biasing of the VCO is provided by an on-chip low-dropout (LDO) regulator to generate a 2.7-V low-noise supply for the VCO and a resistive digital-to-analog converter (RDAC) to set the VCO current. A power detector (PD) followed by an analog-to-digital converter (ADC) are attached to the VCO tank to allow measurement of swing and realization of automatic amplitude control (AAC).

Referring back to Fig. 1, the buffered VCO signal is provided to an on-chip divide-by-four prescaler. This $\sim 5\text{-GHz}$ divider signal is used to drive a separate FMCW synthesizer which generates the VCO control voltages. The prescaler is realized by two cascaded static divide-by-two stages implemented using current-mode logic. The divider output power can be selectable from -7 to 0 dBm by changing the current consumption of the final buffer stage.

The buffered VCO signal is further buffered and provided to a 20- to 40-GHz bypassable frequency doubler. Fig. 3 shows a simplified schematic [15]. The doubler is implemented as a

¹Note that frequencies are referred to as 20, 40, or 80 GHz for simplicity; however, these correspond to a minimum range of frequencies in support of LRR and SRR modes, namely, 19 to 20.25 GHz for the 20-GHz range, 38 to 40.5 GHz for the 40-GHz range, and 76 to 81 GHz for the 80-GHz range.

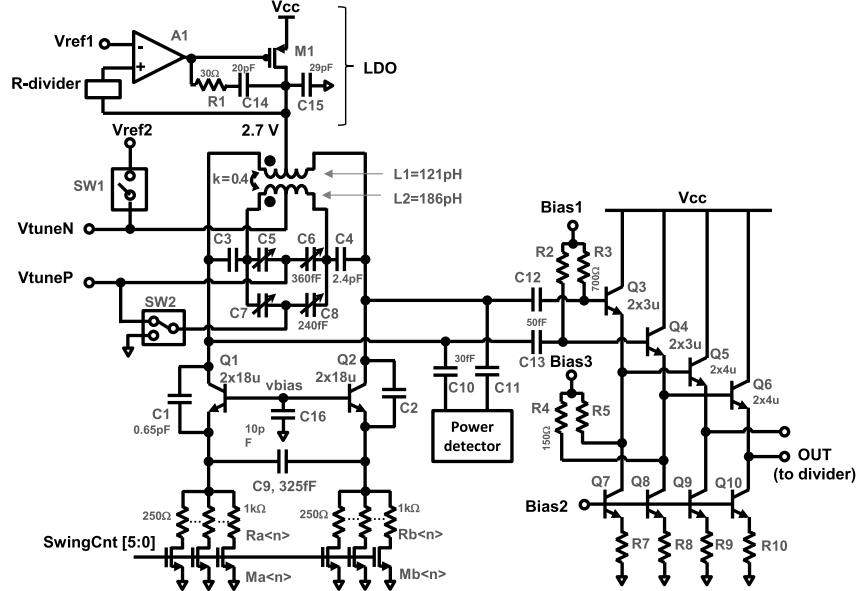


Fig. 2. Schematic of 18.5- to 20.6-GHz VCO with integrated low-dropout regulator and output buffer.

push-push topology (Q1, Q2) with a stacked cascode (Q3) to increase output impedance [16]. This doubling mode is enabled with Bias 1 (with Bias 3 grounded). In parallel to the doubler is a 40-GHz LO amplifier (Q4, Q5) which shares the same output matching network. This “bypass” path can be enabled using Bias 3 (with Bias 1 grounded) to allow injection of an external 40-GHz range LO source for testing purposes or for radar operation over a frequency range wider than that supported by the on-chip VCO. Switching of Bias 1 and Bias 3 (SW1, SW2) is realized using nMOS transmission gates to realize a multiplexing function. In general, for this doubler circuit as well as for most other schematics presented herein, all voltages labeled “BiasX” are derived from replica current mirrors. These are then bypassed using large double-gate nMOS capacitors and then provided to the circuit through low-impedance transmission lines.

Referring back to Fig. 1, after the 20- to 40-GHz doubler, the signal is split using a Wilkinson power splitter, and both outputs are then converted to differential using baluns and amplified with a differential buffer. Two separate 40- to 80-GHz doublers are then used, one for the TX array and one for the RX array. This 40- to 80-GHz doubling operation could be realized in a single circuit; however, having parallel doublers allows power-efficient local generation of the 80-GHz LO signals for the TX and RX arrays. In particular, the LO buffering necessary after the signal splitting is more power efficient at 40 GHz as compared to at 80 GHz. Furthermore, use of 40-GHz LO splitting is consistent with our prior chipset architecture, reducing risk. The 40- to 80-GHz doublers again use a push-push configuration, following the same topology as shown in Fig. 3, with the exception that the bypass LO path is removed and the output matching is updated for 80 GHz. In the TX, the 80-GHz doubled output (marked as LO-TX in Fig. 1) is split with a Wilkinson and then each is converted to differential using baluns. In the RX, the 80-GHz doubled output (marked as

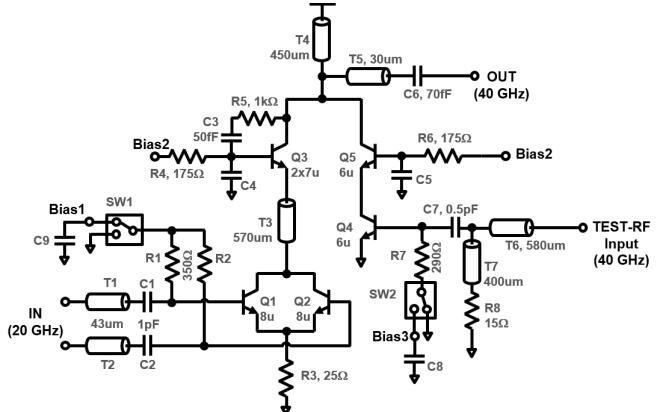


Fig. 3. Schematic of 20–40 GHz frequency doubler with selectable test RF amplifier path.

LO-RX in Fig. 1) is converted to differential using a balun. This then feeds an LO buffer chain within the RX.

C. Transmitter Array

The TX array includes two parallel channels, allowing for connection to diverse antennas having, for example, different antenna patterns. Each TX channel includes a two-stage coarse variable-gain amplifier (VGA) and single-stage fine VGA, all designed for 76- to 81-GHz operation. Together, these stages provide controllable gain of –20 to +30 dB in 0.5-dB steps. Finally, a two-stage balanced power amplifier (PA) followed by an output balun drives the external antenna, designed to provide +18 dBm into a 50- Ω output load for each TX chain.

Fig. 4(a) shows the circuit schematic for the first two VGAs. These provide a coarse gain-control function that can together reduce the final TX output power by 30 dB to as low as –10 dBm. The coarse VGA has two amplifier paths—an inner high-gain path and an outer low-gain path. In the

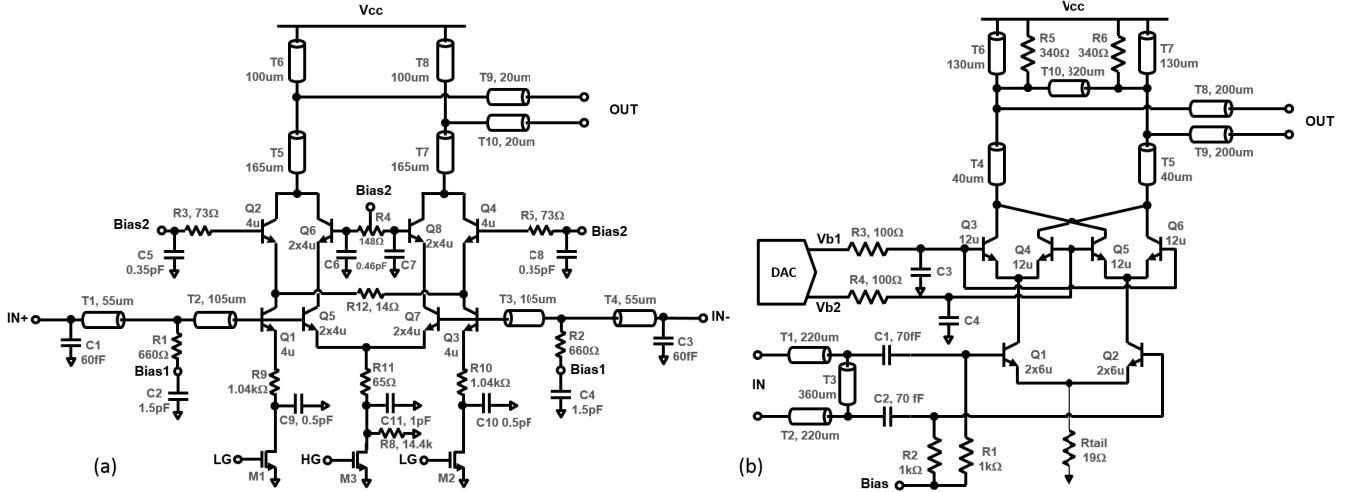


Fig. 4. Schematic of (a) coarse-control and (b) fine-control VGAs.

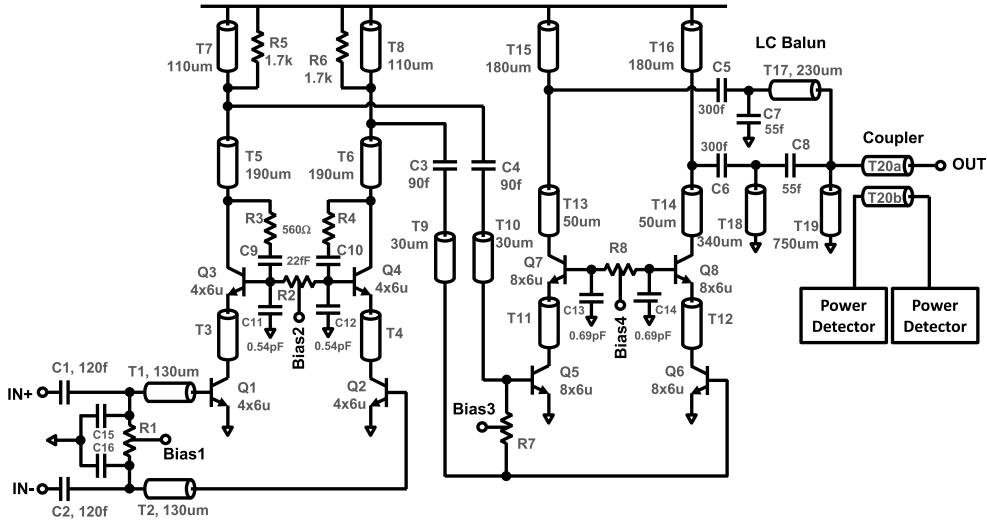


Fig. 5. Schematic of two-stage PA.

normal (high-gain) operating mode, the inner amplifier path is operational, the outer path is disabled, and the circuit behaves in a differential manner with no emitter degeneration. In the low-gain mode, the outer path is operational, the inner path is disabled, and the circuit behaves as a balanced class-AB amplifier. In this mode, degeneration in both lower (Q1, Q3) and upper (Q2, Q4) devices reduces power gain.

Fig. 4(b) shows a schematic for the fine VGA, which employs a cross-coupled Gilbert cell. This VGA topology was chosen to achieve low variation in output power across temperature. A transmission line (T10) connected between the positive and negative output nodes is used to suppress both common-mode signals and second-order differential-mode harmonics. VGA gain is set with a digital-to-analog converter (DAC) to provide the base voltages for the cross-coupling devices [17]. The fine VGA is designed to provide approximately 6-bit, 0.5-dB resolution, allowing the final TX output power to be set to a fixed value across PVT. Note that power consumption of the full TX chain is constant across VGA settings.

The PA shown in Fig. 5 is a two-stage class-AB balanced cascode amplifier [7], [18]. Custom low-inductance metal-oxide-metal capacitors (C11-14) designed using HFSS [19] are included for bypassing of the cascode base voltages, and the cascodes are designed for stability in both common and differential modes. Progressively larger transistor sizes are used within the pre-driver and the final driver stages to support higher current levels and thus higher power levels. Finally, an output inductor-capacitor (LC) balun allows single-ended drive of TX antennas. Shunt transmission line T19 at the output also simplifies the output electrostatic discharge (ESD), avoiding a need for an ESD diode [20]. The final driver is designed to generate +18-dBm P_{sat} at 25 °C and +16 dBm P_{sat} at 125 °C.

D. Receiver Array

The RX array includes six parallel channels to enable digital beamforming at baseband. Each input is single-ended to simplify the external interconnect and antenna design. Following an input LC balun, each RX chain includes a current-mode

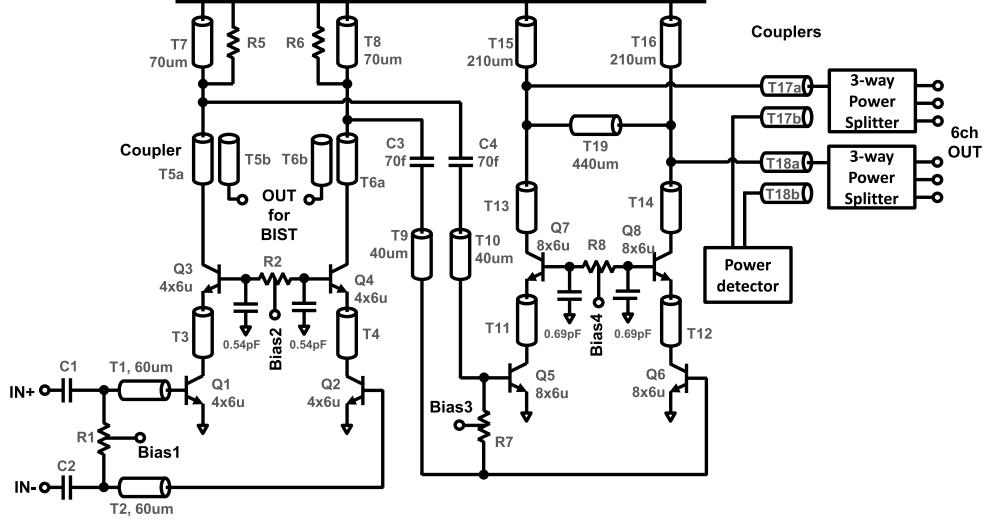


Fig. 6. Schematic of RX LO amplifier chain with six-way power split.

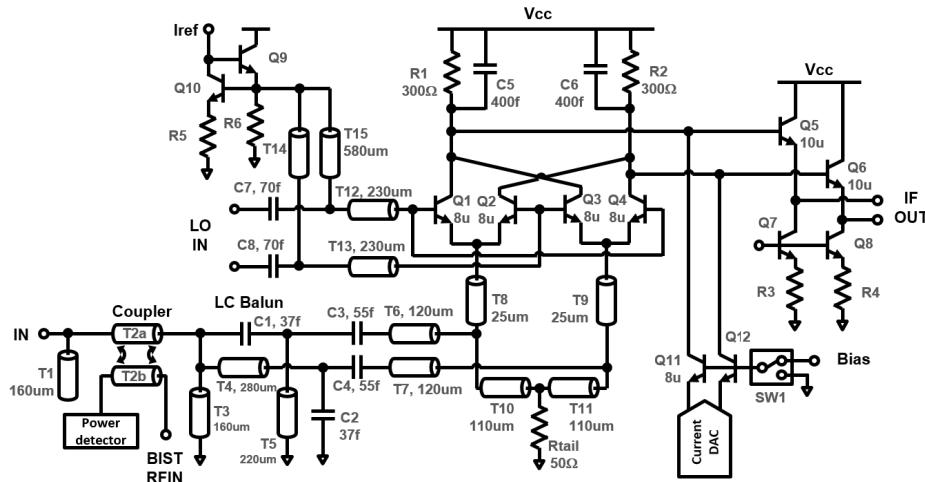


Fig. 7. Schematic of receive mixer with multiplexed loopback path and output buffer.

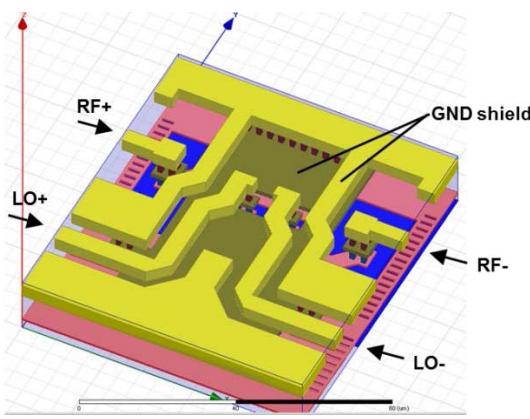


Fig. 8. Screenshot of 3-D modeled view (within HFSS) of mixer commutator metal layout.

downconversion mixer, a baseband multiplexer used to switch between the downconverted IF signal and an IF loopback test signal, and an IF buffer. The LO signal for the RX array is

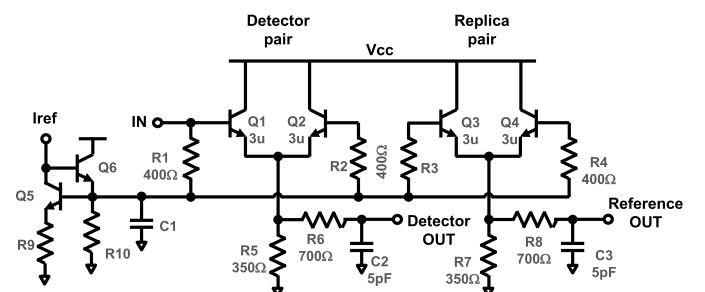


Fig. 9. Schematic of RF PD.

derived from the 80-GHz “LO-RX” signal, where the RX LO network includes two stages of amplification and two three-way passive power splitters. In the following section, we first describe the RX LO network and then the receive mixers.

The total LO network for the RX is designed to provide +5-dBm LO power to each of six mixers. A simplified schematic of the RX LO amplifier is shown in Fig. 6. Two stages of class-AB cascode amplifiers are used to

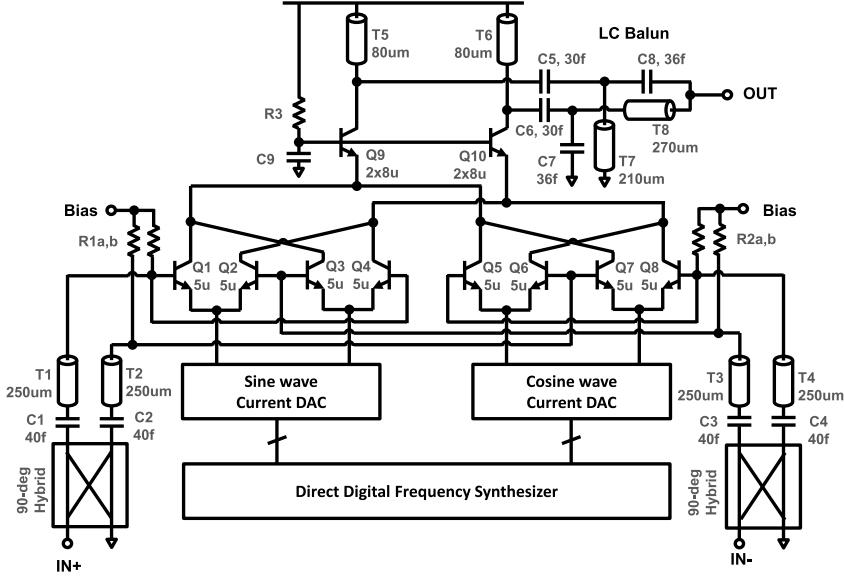


Fig. 10. Schematic of RF modulator for receive built-in-test.

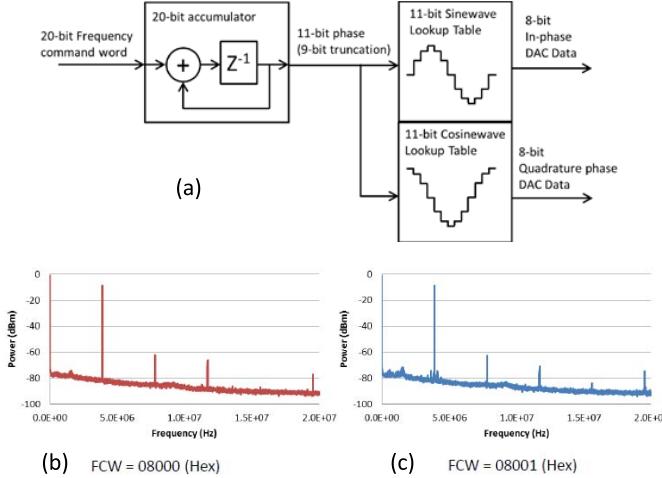
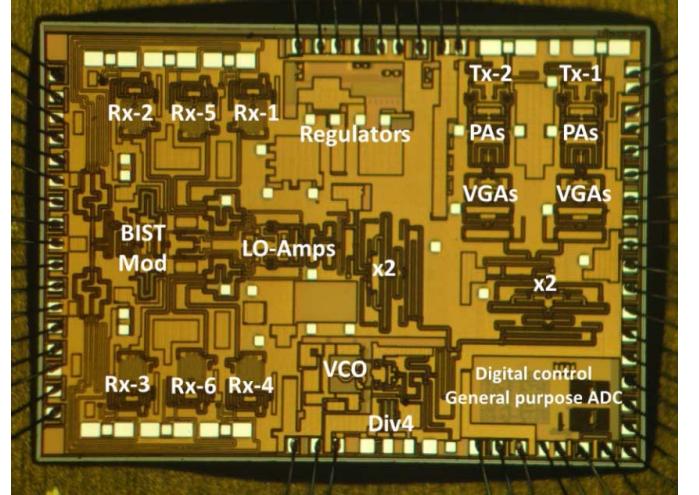


Fig. 11. (a) Block diagram of direct-digital frequency synthesizer and example measured spurious performance for (b) 3.90625- and (c) 3.90637-MHz outputs using 125-MHz clock.

provide approximately 28 dB of amplification. After the first stage, the 80-GHz LO signal is branched off using a hybrid coupler (not shown) to feed a built-in-test path discussed in the subsequent section. To generate six differential LO signals for the mixers, the differential LO signal is simply split using its positive and negative outputs and then each output is connected to a bank of three RXs via three-way passive power dividers [21]. This has lower loss and smaller area in comparison to a six-way differential power splitter or a combination of baluns and two-way power splitters. A shunt half-wavelength transmission line (T19) is connected between positive and negative outputs of the LO amplifier and is used to compensate for relative phase difference across frequency and thereby equalize for LO power discrepancy across the array. Note that the power delivered to the splitting network is monitored through a PD which is weakly coupled to the input to the splitter network via T17 and T18.

Fig. 12. Die photograph of transceiver chip (size is $4 \times 3 \text{ mm}^2$).

In our RX LO path, only passive components appear between the shared common LO amplifier and the array of six RX mixers. This provides an advantage in terms of relative LO phase variation across temperature or power supply condition between each RX channel. Because there are no active circuits, phase variation is minimized, simplifying any required channel-to-channel calibration across temperature.

The mixer schematic is shown in Fig. 7. A mixer-first topology with passive (transistor-free) transconductance allows for high input compression point with moderate noise figure [4], [22]. Also, not having a front-end low-noise amplifier avoids the introduction of temperature-dependent phase variation between channels. The mixer's input RF signal is first fed through a short ($27 \mu\text{m}$) input coupler (T2a, b) to allow monitoring of input power as well as low-level injection (-22 dB coupling) of a BIST signal, to be discussed in the following section. The input signal is converted to

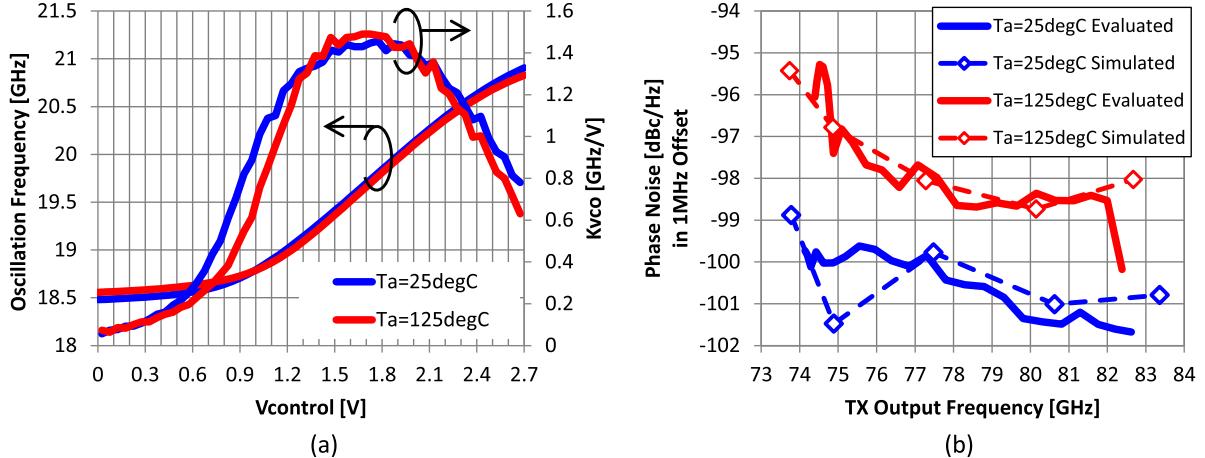


Fig. 13. (a) Measured VCO oscillation frequency and Kvco and (b) measured phase noise across band in 25/125 °C conditions, referenced to TX output.

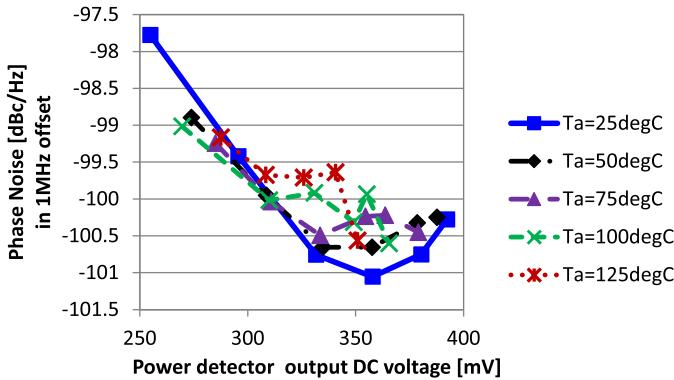


Fig. 14. Measured relationship between the phase noise (1-MHz offset from 80-GHz carrier) and VCO PD output dc voltage across temperature, obtained by sweeping the VCO RDAC value across possible values at multiple temperatures.

differential using an *LC* balun and then converted into current using an impedance matching network (T6–T9). In addition to having high linearity, the passive design minimizes phase variations across temperature between RX channels, since the only active devices are found within the commutator. To obtain low self-mixing and low dc offset, the LO signal is isolated from the RF signal within the commutator using symmetric layout and ground shielding, as depicted in Fig. 8.

The intermediate frequency (IF) output of the mixer drives an *RC* load and output emitter-follower buffer. The IF bandwidth is approximately 300 MHz. Additionally, a loopback path is included (Q11, Q12), allowing injection of modulated IF signals directly into the IF network. This can be used to measure the IF response of each RX chain with BIST.

E. Built-In Self-Test

BIST functionality is critical for low-cost mm-wave systems [23] and is included for our complete transceiver. All BIST circuitry is shaded in gray in Fig. 1 to illustrate these capabilities and how the inclusion of mm-wave BIST greatly impacts the overall system design and floorplan. For the LO network, BIST allows measurement of VCO power using

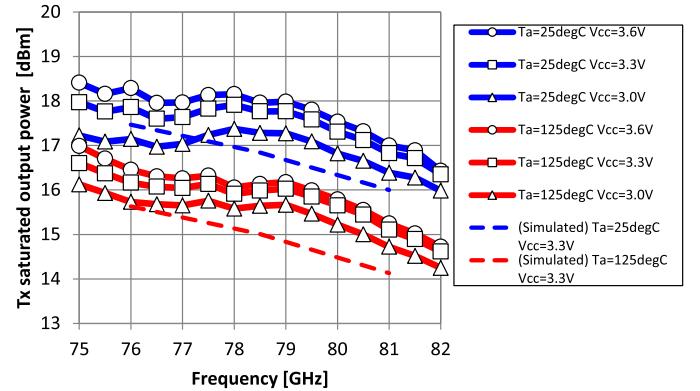


Fig. 15. Measured saturated output power of TX for $T = 25/125$ °C and across three power supply conditions.

a PD, enabling an AAC loop to be realized in mixed-signal domain. Specifically, the digitized measured power can be used to set the RDAC setting within the VCO to obtain a desired swing and thus a desired phase noise [24], [25]. An additional PD is used at the 80-GHz LO port of the RX array, prior to six-way splitting.

Fig. 9 shows the schematic of the PD which is used throughout the transceiver. An emitter-coupled differential pair creates a second-order response at the emitter, where the dc voltage corresponds to signal power [26]. A replica differential pair ensures a rejection of systematic dc offset across PVT variation by providing a PVT-dependent reference voltage. This transceiver chip has 12 PDs to check the functionality and RF signal power, as follows: one detector for each RX, two detectors for each TX, one detector for RX LO power, and one detector for VCO. Additionally, a temperature sensor is included. Each PD's output and temperature sensor's output are amplified by on-chip low-noise baseband amplifiers then detected by an on-chip 10-bit successive approximation ADC running at 10 MHz.

For the TX, BIST includes monitoring of power levels at the TX outputs. The TX output stage contains two PDs integrated on the forward and reverse coupled ports of a hybrid

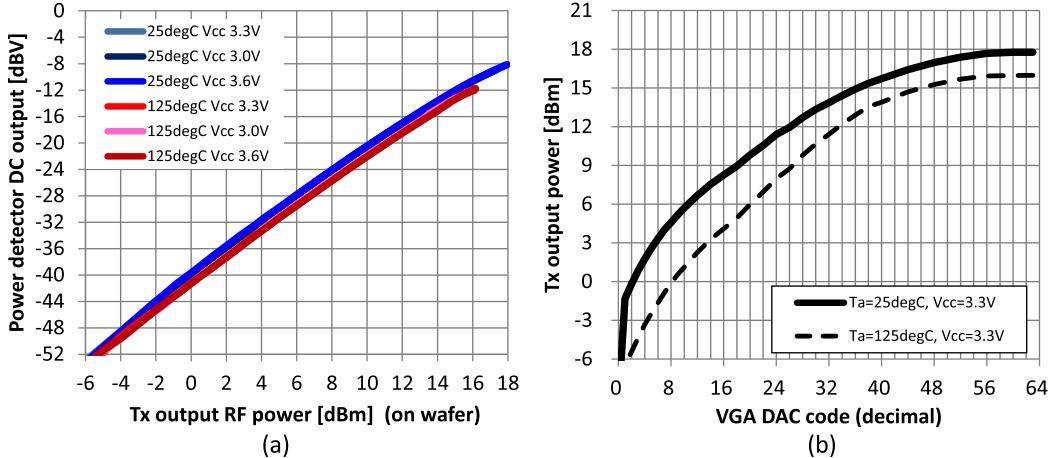


Fig. 16. (a) Measured relationship between TX output power and TX PD output and (b) measured TX output power versus control voltage of fine VGA.

coupler [13]. One PD is used to monitor the forward signal power delivered to the antenna to enable control of the output power using the VGA. Another PD is used to monitor reflected power caused by any impedance mismatch at the outside of chip. This function is useful to check for failures associated with package and/or board assembly. Either check can be run across frequency by simply sweeping the LO control and monitoring TX power.

Built-in-test of the RX is more extensive and allows measurement of amplitude and phase responses across frequency. To accomplish this, an FMCW-like signal is generated on chip and coupled into the input of each RX [5], [27]. The LO signal is first branched off from the RX LO path using a coupler and amplified. This signal is marked in Fig. 1 with ‘‘BIST-LO.’’ The 80-GHz LO signal is then fed into an integrated 80-GHz modulator, whose schematic is shown in Fig. 10. The input 80-GHz LO signals are first fed through a pair of quadrature hybrids to generate differential in-phase (I) and quadrature-phase (Q) LO signals. These couplers and the following matching network (C1–C4, T1–T4) are designed to achieve flat response across the full 76–81 GHz band. The quadrature LO is then provided to a pair of 80-GHz switching commutators (Q1–Q8). Baseband modulation is created using DACs controlled by an on-chip direct-digital frequency synthesizer (DDFS) [28]. The maximum clock frequency is 125 MHz and the maximum baseband modulation frequency is half of the clock frequency, or 62.5 MHz. After mixing, the modulated single-sideband 80-GHz signal is buffered with common-base amplifiers (Q9, Q10) and then impedance matched. An output *LC* balun converts to single-ended. These modulated test signals are then distributed through the 80-GHz RX array using symmetric transmission lines.

Fig. 11(a) shows a block diagram of DDFS circuit. The DDFS enables generation of digital sine and cosine waves whose frequency is controlled by a 20-bit frequency command word (FCW). The maximum frequency is limited by the Nyquist frequency of the operating clock. The generated digital IF sine and cosine signals are converted to analog current signals by two current DACs then injected into the IF ports of the 80-GHz IQ mixer. The generated IF signal is

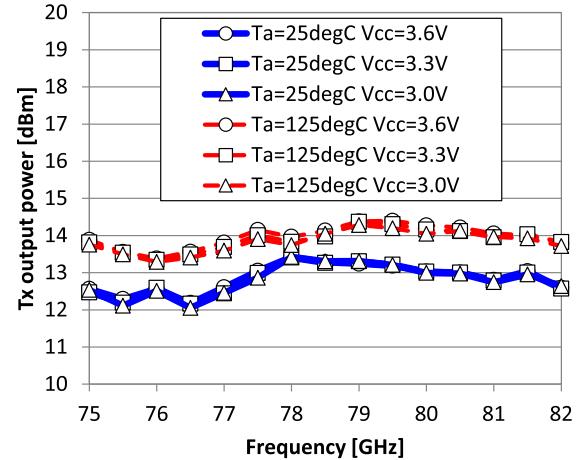


Fig. 17. Measured TX output power across power supply and temperature when power calibration is used to set power to 13 dBm.

up-converted by the IQ mixer then the generated RF signal becomes the single-tone signal, according to the following:

$$\begin{aligned} \sin(2\pi f_{\text{IF}}t) \cdot \cos(2\pi f_{\text{LO}}t) + \cos(2\pi f_{\text{IF}}t) \cdot \sin(2\pi f_{\text{LO}}t) \\ = \sin[2\pi(f_{\text{IF}} + f_{\text{LO}})t] \end{aligned} \quad (1)$$

where f_{IF} and f_{LO} represent the frequency of IF signal and mm-wave LO signal, respectively. Example measured spurious performances of the DDFS are shown in Fig. 11(b) for 3.90625-MHz output ($\text{FCW} = \#08000_{16}$) and Fig. 11(c) for 3.90637-MHz output ($\text{FCW} = \#08001_{16}$).

We now describe how the overall RX BIST operates. First, the input modulation is measured by enabling the baseband-only portion of the modulators (DDFS and DACs) and multiplexing these signals into the IF path of each receive mixer (i.e., Q11 and Q12 within Fig. 7, where the current DAC depicted there is the same current DAC used within the BIST network). In this loopback mode, we can measure the full IF response, including circuits on the transceiver and any circuits on the companion CMOS signal-processing chip. Second, the 80-GHz modulated BIST signals are created and distributed throughout the RX array. The power at each

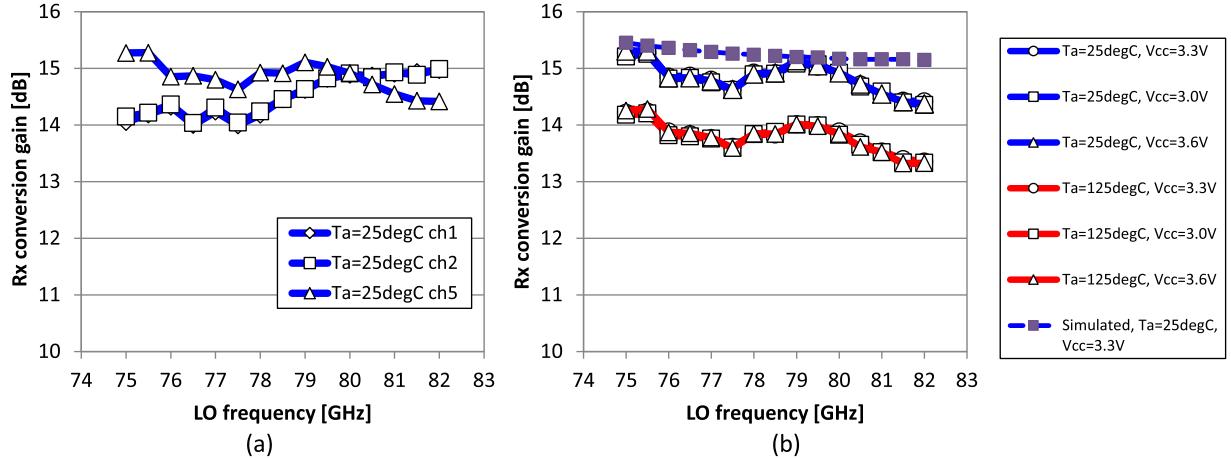


Fig. 18. Measured conversion gain with 2-MHz IF versus frequency for (a) RX chains 1, 2, and 5 at room temperature and (b) RX chain 5 across 25/125 °C and three supply voltages.

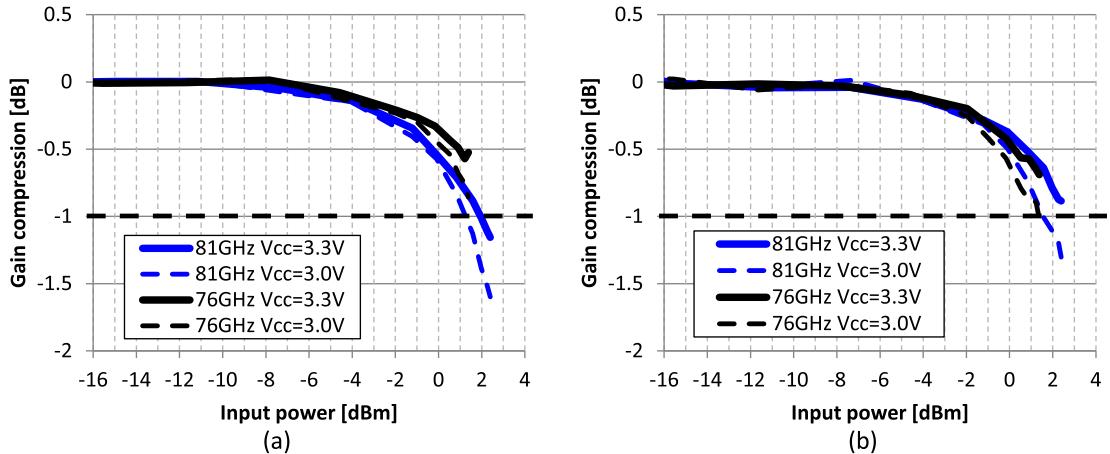


Fig. 19. Measured RX gain compression at 25 °C for (a) channel 2 and (b) channel 5.

RX input is then measured, using the PD which is coupled to the input of each mixer, as shown in Fig. 7. This allows us to measure the injected RF power to each input. Finally, the complete loop is operated, where the RF inputs for all mixers are provided through the BIST path and the LO inputs are provided as per normal operation. IF outputs are then measured. By comparing the detected RF power to the detected IF power, we can extract RX gain. Finally, by comparing the detected IF loopback phase to the detector BIST phase, we can extract phase response for each element as well as compare phase responses between elements.

III. CHIP-LEVEL MEASUREMENT RESULTS

The six-channel RX, two-channel TX, LO chain, and BIST circuitry have been integrated onto a single chip in SiGe BiCMOS 8HP technology from GlobalFoundries. Fig. 12 shows a die photograph of the chip. The chip dimension is 3 by 4 mm². A first set of measurements is completed using wafer-level probing for all RF and mm-wave signals. For these, the bare-die transceiver chip is mounted onto a printed circuit board (PCB), with all low-frequency signals directly wire-bonded to the board. Total power consumption is 1.8 W

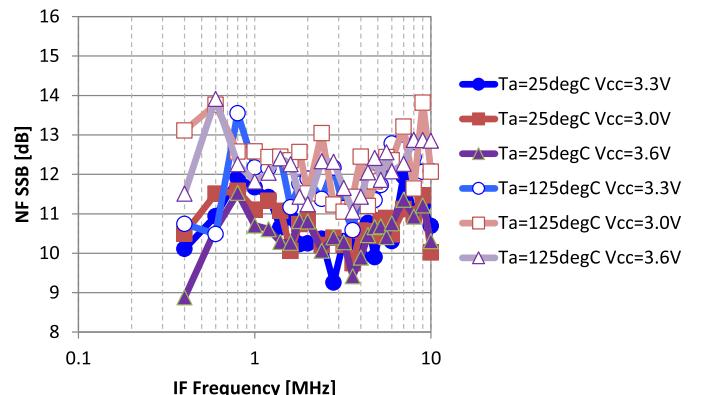


Fig. 20. Measured single-sideband noise figure for RX channel 5 at LO = 76 GHz.

from 3.3 V in a mode with one TX and six RX operational, and 1.6 W for one TX and four RX operational.

First, we summarize the LO chip-level measurements, focusing on phase noise and tuning range. For this measurement, we probe the prescaler output (~5 GHz) and then later validate this result through probed measurements of the

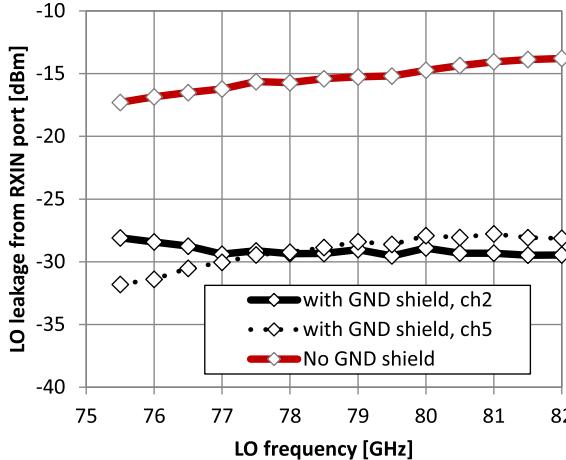


Fig. 21. Comparison between measured LO leakage with and without ground shield at 25 °C and typical supply condition. “No GND shield” corresponds to earlier version of chipset without ground shield within mixer commutator switch layout.

TX outputs. In UWB mode, the measured output frequency of the prescaler is 4.625 to 5.15 GHz, which corresponds to a range of 18.5 to 20.6 GHz for the VCO, and 74 to 82.4 GHz for the full radar. This is wide enough to cover both LRR and SRR modes. The measured tuning response and extracted VCO gain (K_{VCO}) are shown in Fig. 13(a), after converting the response to 20-GHz range for the VCO. Responses for both 25 °C and 125 °C are overlaid, indicating very little variation in the VCO response across temperature. The measured supply pushing of the VCO is less than 10 MHz/V for 20-GHz oscillation frequency, where the LDO as well as the transformer-coupled varactor structure both work to suppress supply pushing.

The measured and simulated phase noise across the band in UWB mode referred to an 80-GHz range output is shown in Fig. 13(b) for both 25 °C and 125 °C. Since the phase noise is measured at the divide-by-four output, 24 dB is added to the phase-noise measurement to account for the factor of 16 frequency difference. The phase noise at 1-MHz offset is below -100 dBc/Hz across most of the frequency range, with excellent correlation between measurements and simulations. Fig. 14 shows the measured relationship of phase noise and the power-detector output voltage across several temperature conditions. In this measurement, the VCO RDAC value is swept and then phase noise is recorded versus the PD output. The PD output is directly proportional to the RDAC setting. From this, we see that an appropriate optimization across PVT is approximately 350-mV output voltage, which can be used to set the AAC settings.

Next, we summarize TX chip-level measurements. Fig. 15 shows the measured and simulated TX saturated output power across temperature and supply voltage. The power variation across the frequency band is less than 1 dB and the variation across 3- to 3.6-V supply voltage is about 1 dB. The TX output power is approximately +18 dBm at 76–79 GHz for 25 °C and +16 dBm at 125 °C, both at $V_{CC} = 3.3$ V. Across all supply and temperature, output power remains above +15 dBm.

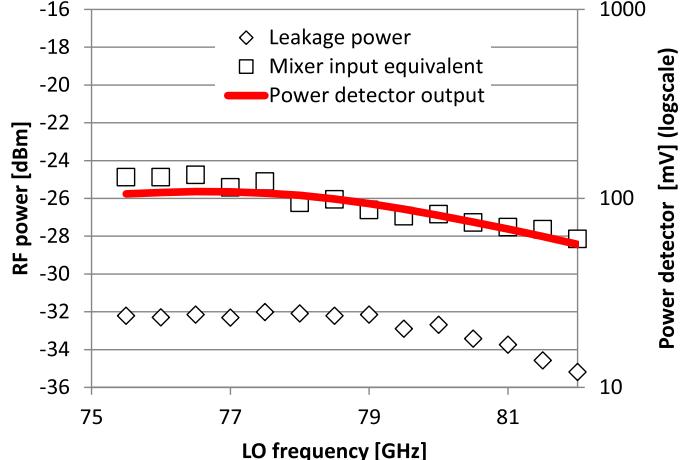


Fig. 22. Comparison of measured power at RX input using built-in PD to equivalent input power calculated based on measured IF power in BIST mode. This illustrates that RX BIST can extract IF conversion gain. Also included is measured leakage power at RF input, illustrating directivity of input coupler.

Fig. 16(a) shows the measured responsivity curve for the PD, relating the output RF power from the PA to the on-chip measured power from the PD. The relationship between the detected power and the output voltage is linear across a wide range. A slight temperature dependence exists, where the PD responsivity is about 1 dB less at 125 °C. This dependence could be calibrated by incorporating feedback from an on-chip temperature sensor. This temperature sensor is located directly between the PAs in the two TX chains, with a distance of 300 μ m to either PA.

Fig. 16(b) shows the measured response of the fine VGAs within the TX across DAC control settings and temperature. The gain step is roughly 0.5 dB in the linear region and total control range is wider than 15 dB in 25 °C condition. Though not graphed, the measured coarse-VGA gain step has been validated, showing approximately 25-dB gain drop in each stage and a total coarse gain reduction of 47 dB.

With both the PD and VGA validated, we can evaluate a power calibration routine for the TX chain where we attempt to equalize the output power to +13 dBm across all PVT conditions. As shown in Fig. 17, our results indicate that using the on-chip PD can allow leveled output power within ± 0.5 dB of target value across PVT.

Spurious content of the TX was evaluated through wafer probing at room temperature. The measured spurs at 20, 40, and 60 GHz were -57 , -47 , and -39 dBm, respectively. These spurs are caused by LO feedthrough in the frequency doublers as well as a mixing between 20- and 40-GHz signals in the second doubler.

We now summarize RX chip-level measurements. As will be discussed within the packaging section, the RX (and TX) channels have been co-designed to compensate for package-level parasitics. In the RX, channels 1–4 all have the same input matching network design, whereas channels 5–6 have a slightly different matching network design, as the package transitions of the middle channels are different. As a result, we report RX measurements for both types of channels.

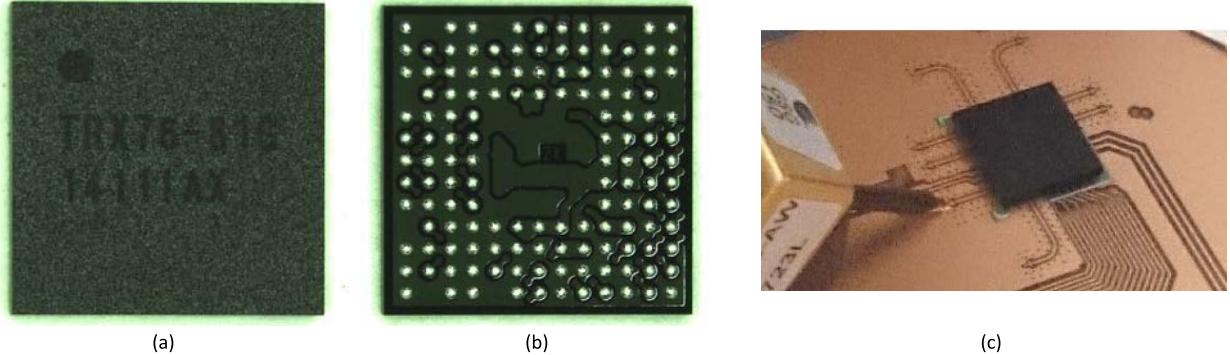


Fig. 23. Photographs of BGA package. (a) Top view. (b) Bottom view (size is 9.5 by 8 mm²). (c) Package-level measurement setup.

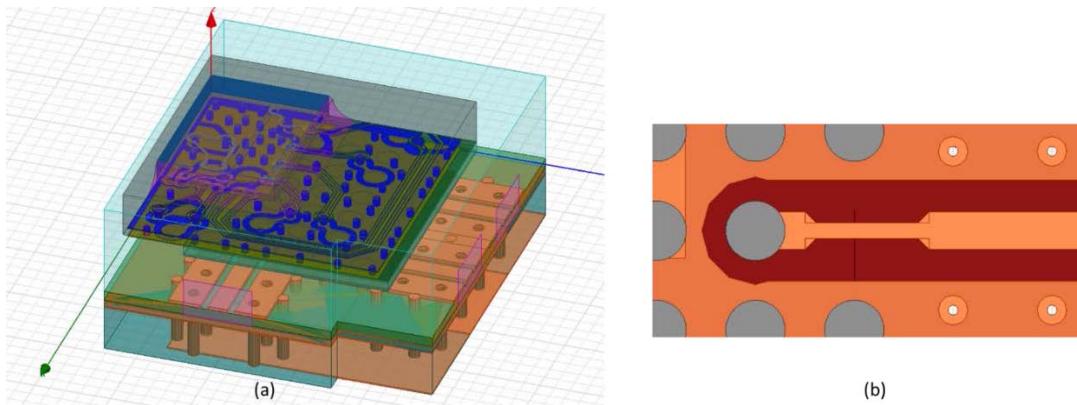


Fig. 24. (a) Screenshot of 3-D modeling by HFSS of the TX transition including chip, interposer, and PCB pattern. (b) Example PCB matching pattern.

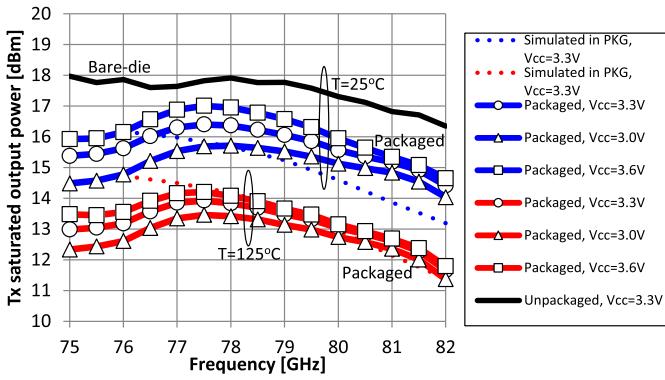


Fig. 25. Measured TX saturated output power across frequency, temperature, and supply voltage for packaged samples. Simulated chip-in-package and unpackaged conditions shown for comparison.

Fig. 18 shows the measured RX conversion gain across the LO frequency for 2-MHz IF output frequency. Fig. 18(a) shows only channels 1, 2, and 5, whereas channels 3, 4, and 6 have identical responses. RX channels 1 and 2 have identical conversion gain across the band, equal to 14 to 15 dB. RX channel 5 shows slightly higher and flatter conversion gain of 15 dB across the band, with gain for this channel across supply and temperature shown in Fig. 18(b). Simulated conversion gain is about 15.2 dB.

The measured gain compression curves for room temperature condition are shown in Fig. 19. The input

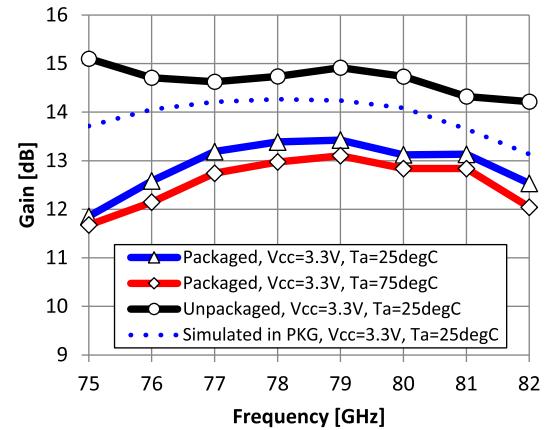


Fig. 26. Measured and simulated RX conversion gain for packaged and unpackaged samples.

1-dB compression point (iP_{1dB}) is higher than +1 dBm for 3-V supply condition and +2 dBm for 3.3 V. The measured single-sideband noise figure (NF_{SSB}) for LO frequency of 78.5 GHz is approximately 10.5 dB at 25 °C and 12 dB at 125 °C, as shown in Fig. 20, for IF varying from 0.4 to 10 MHz. The NF_{SSB} is measured using a double-sideband Y-factor measurement with W-band noise source at the input and Rohde and Schwarz signal source analyzer (FSUP 50) attached to the IF output. NF_{SSB} is obtained by adding 3 dB to the result.

Minimizing the LO leakage from the RX input port is

important for radar because the large leakage can reflect from an external impedance mismatching point causing self-mixing product and dc offset. Excessive dc offset takes up headroom and degrades the $iP_{1\text{dB}}$. Also large dc offset can increase the noise figure. Fig. 21 shows the measured results of LO leakage from RX input port and compares to our previous chipset [7] which had excessive leakage and offset, marked with the label “No GND shield.” As suggested earlier, the commutator layout with ground shield inserted between the RF and LO ports effectively reduces the LO leakage, with measurements indicating a 10-dB improvement. For this chip, the measured dc offset is 50 mV when the RF input port is left open, reducing to 20 mV when the input port is terminated with 50Ω .

We next validate the BIST measurement for RX gain extraction. Fig. 22 shows the RF power measured at the built-in PD (at the RX input) and also the leakage from RX input port. For this measurement, the RF input was terminated with 50Ω . Overlaid in Fig. 22 is the RX input equivalent power which is calculated from the IF output power and the measured conversion gain. Since equivalent input power agrees well with the detected RF power, we conclude that the BIST method for calculating RX conversion gain is accurate. To assess the quality of the on-chip modulator, we measured the spectrum of the 80-GHz signal at the RF input, where we observe that the opposite sideband is suppressed by over 20 dB. Finally, according to the measurement result, the directivity of the coupler is about 6 dB. Note that the RX BIST measurements could also be performed with the RF input left unterminated; however, this will result in reflections from the input network back into the mixer, where it can add constructively or destructively to the original coupled signal. Our measurements show this leads to a frequency-dependent input power injected into the mixer.

IV. PACKAGE DESIGN AND MEASURED RESULTS

Millimeter-wave packaging is an essential technology to reduce assembly cost for radar modules and achieve a more reliable RF transition at the RF ports. In this paper, we employ flip-chip connection to a ball-grid array (BGA) package, with package photographs shown in Fig. 23. The package size is 9.5 by 8 mm². In designing the package, 3-D electromagnetic simulations (HFSS [19]) were used to model the solder-ball and package transitions. Fig. 24(a) shows the 3-D modeling of TX interconnects. As mentioned earlier, the impedance of the RX and TX circuit is co-designed to match the impedance of package interposer. Also, there is an extra matching pattern on the PCB to provide additional adjustment for $50\text{-}\Omega$ load, as shown in Fig. 24(b). One disadvantage of flip-chip BGA packaging is the poor thermal dissipation, because the thermal connection between the silicon and package is mainly the connecting bump on the pads. To reduce the thermal resistance, this chip should have as many ground bumps in the neighborhood of thermal source, for example the TX chain. In our design, a total of 52 ground bumps are used, with many placed around the PA cores, the VCO, and the final LO buffers within the RX. The measured package thermal resistance is 21 K/W when the

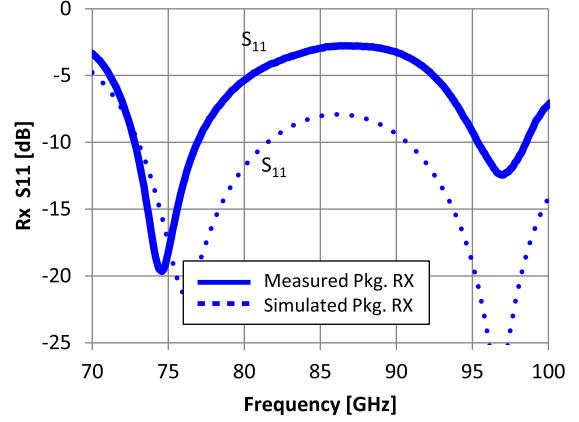


Fig. 27. Comparison between simulated and measured S_{11} for packaged RX.

package is stacked on a PCB evaluation board consisting of Rogers 3003 above FR4.

Fig. 25 shows the measured and simulated TX output power for a packaged sample. In this measurement, as shown in Fig. 23(c), a transmission line is probed on the PCB and the loss of this line is de-embedded up to the point of the connection to the package. The measured output power is +15 to +16.5 dBm in 25 °C condition. This indicates a 1.5- to 2-dB loss compared to the wafer-probed (unpackaged) measurement result, agreeing with our simulations. The measured return loss of the TX output port is above 10 dB across the entire frequency band.

Fig. 26 shows the measured and simulated RX conversion gain within the package. Once again, the insertion loss of package in RX path is 1.5 to 2 dB. Note that due to an operating temperature limitation of the off-chip synthesizer, we were unable to measure the RX above temperatures of 85 °C. Despite this limitation, the ratio of degradation level of conversion gain is the same as that of the wafer-probed measurement result. The measured return loss of the RX input port is above 10 dB from 73 to 77 GHz; however, increased mismatch is seen looking into the package, as shown in Fig. 27. This mismatch is attributed to modeling and manufacturing issues for the RX interconnect path.

Isolation between RX channels and between RX and TX channels is important. Measured RX-to-RX isolation is greater than 50-dB on-chip, degrading to >22 dB in package, as shown in Fig. 28(a). A stronger coupling between the adjacent RX solder-ball transitions degrades isolation, despite the presence of ground-ball connections in between. Measured RX-to-TX isolation is 55-dB on-chip, decreasing to 34 to 40 dB in package, as shown in Fig. 28(b). Improved RX-RX and RX-TX package-level isolation and improved RX package-level matching will be the subject of future work.

Smaller relative phase variation across temperature and supply voltage is important for radar systems. The radar module’s relative phase can first be tested before shipping to calibrate the phase relationship of each channel, enabling accurate angle detection. Once calibrated, any variation across temperature and supply can lead to errors. As a

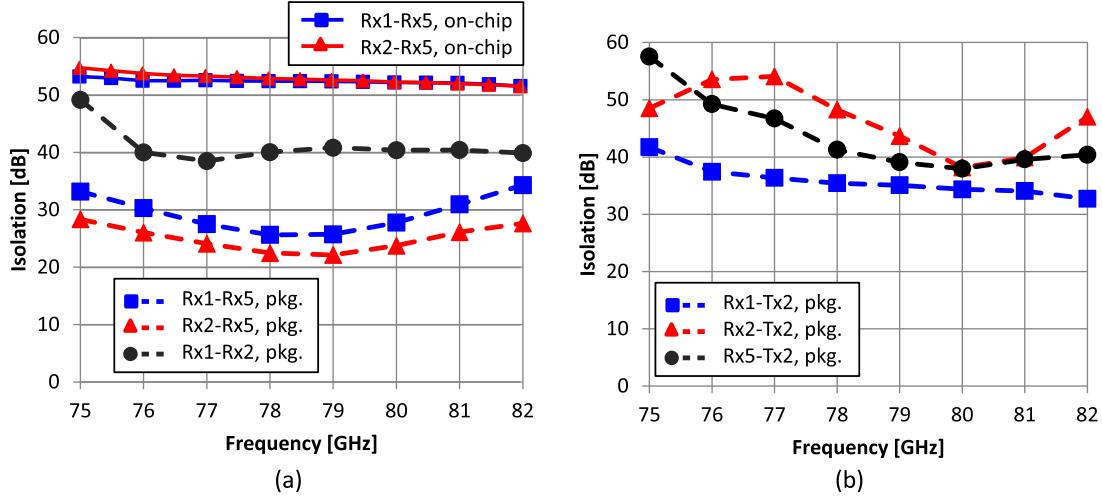


Fig. 28. Measured (a) RX-to-RX isolation on-chip and in-package and (b) RX-to-TX isolation in-package.

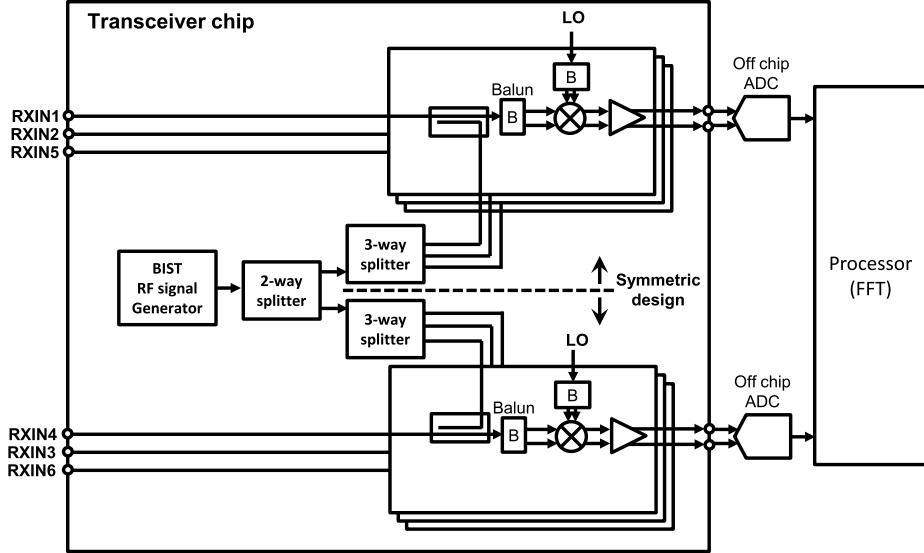


Fig. 29. Evaluation setup for channel-to-channel phase variation across temperature.

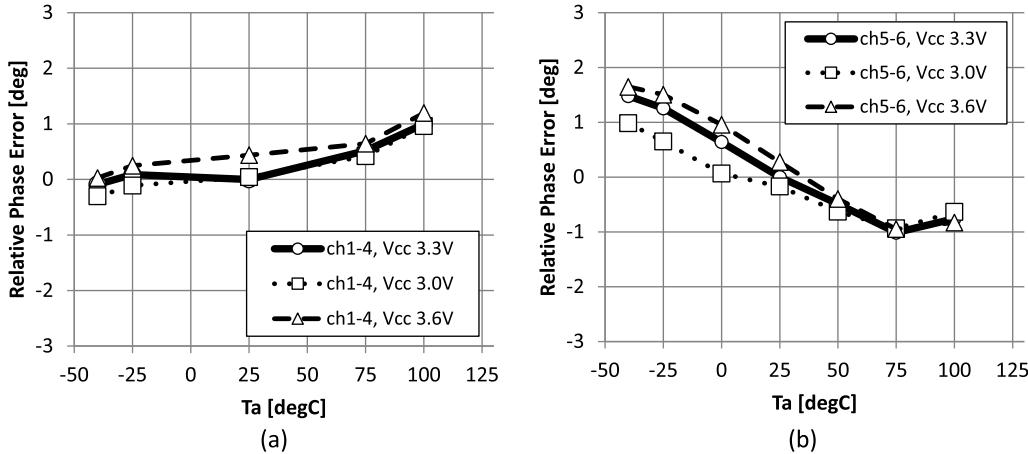


Fig. 30. Measured relative phase variation for (a) channels 1–4 and (b) channels 5 and 6, respectively.

result, very small variation is desired across temperature and supply.

Fig. 29 shows the evaluation setup used to measure the relative phase variation. To eliminate the effect of phase noise

and to realize the stable RF signal supply, the RX BIST is used to excite each RX signal chain. From a chip layout standpoint, the combinations of channels 1–4, channels 2 and 3, or channels 5 and 6 are symmetric. As a result, we can

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO OTHER WORK

Reference`	Wafer-Level Measurements				Package-Level Measurements			
	Lee [12]	Trotta [4]	Takeda [7]	This Work	Ku [9]	Trotta [4]	Wagner [5] Knapp [6]	This work
Technology	65nm CMOS	0.18um SiGe	0.13um SiGe	0.13um SiGe	0.13um SiGe	0.18um SiGe	0.18um SiGe	0.13um SiGe
Frequency [GHz]	75.6-76.3	76-81	76-81	76-81	76-84	76-81	76-81	76-81
Format	1 Chip	2 Chip	2 Chip	1 Chip	Flip chip-on-board	2 Pkg.	2 Pkg.	1 Pkg.
RX Gain [dB]	38.7	19	16	15	4	13	16.5	13
RX SSB NF [dB]	7.4 (LNA)	10 to 12	11 to 12	10 to 11	16	-	14 to 15	12
RX iP _{1dB} [dBm]	-22 (LNA)	> -5	> -2	> +1	-5.7	-	> -3	> +3
RX Phase Δ [deg.]	NA	< 4	+/- 0.6	< 2	<8 (rms)	-	-	-
TX P _{SAT} 25°C [dBm]	5.1	16	17	+17 to +18	6	+15	11.7	16
TX P _{SAT} 125°C [dBm]	-	14	15	+15 to +16	-	> 12	9.6	+13 to +14
TX Phase Noise, @1MHz [dBc/Hz]	-85.3	-97.5 to -95	-97 to -100	-99 to -100	NA	-97.5 to -95	-96	-99 to -100
VCO Range [%]	~1%	12%	11%	12%	NA	12%	9%	12%
Power Consumption [W]	0.24	0.79 (4RX) 1.75 (1TX)	0.79 (4RX) 1.16 (1TX)	1.8 (6RX+1TX)	2.54 (8RX+8TX)	0.79 (4RX) 1.75 (1TX)	0.85 (4RX) 2.3 (3TX)	1.8 (6RX+1TX)
Power for 1-Tx & 4-Rx [W]	NA	2.5	1.95	1.6	NA	2.5	≥1.6	1.6
Chip Size RX/TX [mm ²]	1.05	12.0 (4RX) 6.5 (1TX)	7.0 (4RX) 5.6 (1TX)	12.7 (6RX+2TX)	26.1 (8RX+8TX)	12.0 (4RX) 6.5 (1TX)	9.0 (4RX) 9.0 (3TX)	12.7 (6RX+2TX)

confidently measure phase offset between these channels (i.e., 1–4, 2–3, or 5–6) across temperature and ascribe this difference to the intrinsic circuit performance. Note that since channels 5 and 6 have different input matching compared to channels 1–4, the phase responses are different, which would be handled at factory calibration. The measured results of relative phase variation across the temperature and supply voltage are shown in Fig. 30, normalized to the 25 °C, 3.3-V supply condition. The phase variation is less than 2° for each condition.

V. CONCLUSION

This paper presents a single-chip packaged transceiver chip for 76- to 81-GHz automotive radar applications implemented in SiGe BiCMOS technology. Each TX achieves a saturated output power of +18 dBm at the chip output, while consuming 250 mA from 3.3 V. The VCO achieves a 77-GHz referred phase noise of −100 dBc/Hz at 1-MHz offset across the entire 76–81 GHz frequency band using a single VCO circuit. Each RX achieves input compression point greater than +1 dBm, noise figure of 10.5 dB, and conversion gain of 15 dB, while consuming 31 mA from 3.3 V. When inserted into a BGA package, TX output power and RX noise figure degrade

by 1.5 to 2 dB. The transceiver chip consumes 1.8 W in 1-TX and 6-RX mode, and 1.6 W in 1-TX and 4-RX mode. As summarized in Table I, compared to the results in [4]–[7], [9], and [11], this chip achieves the highest TX output power, the highest RX linearity, among the best noise figure, the lowest phase noise, and the best power efficiency.

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REFERENCES

- [1] M. Schneider, "Automotive radar-status and trends," in *Proc. German Microw. Conf.*, 2005, pp. 144–147.
- [2] J. Hatch, A. Topak, R. Schnabel, T. Zwick, R. Weigel, and C. Waldschmidt, "Millimeter-wave technology for automotive radar sensors in the 77 GHz frequency band," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 3, pp. 845–860, Mar. 2012.
- [3] N. Pohl, T. Klein, K. Aufinger, and H. M. Rein, "A low-power wideband transmitter front-end chip for 80 GHz FMCW radar systems with integrated 23 GHz downconverter VCO," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 1974–1980, Sep. 2012.
- [4] S. Trotta *et al.*, "An RCP packaged transceiver chipset for automotive LRR and SRR systems in SiGe BiCMOS technology," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 3, pp. 778–794, Mar. 2012.

- [5] C. Wagner *et al.*, "A 77 GHz automotive radar receiver in a wafer level package," in *IEEE RFIC Dig. Tech. Papers*, Jun. 2012, pp. 511–514.
- [6] H. Knapp *et al.*, "Three-channel 77 GHz automotive radar transmitter in plastic package," in *IEEE RFIC Dig. Tech. Papers*, Jun. 2012, pp. 119–122.
- [7] Y. Takeda, T. Fujibayashi, Y.-S. Yeh, W. Wang, and B. Floyd, "A 76- to 81-GHz transceiver chipset for long-range and short-range automotive radar," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2014, pp. 1–3.
- [8] B.-H. Ku *et al.*, "A 77–81-GHz 16-element phased-array receiver with $\pm 50^\circ$ beam scanning for advanced automotive radars," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 11, pp. 2823–2832, Nov. 2014.
- [9] B.-H. Ku, O. Inac, M. Chang, H.-H. Yang, and G. M. Rebeiz, "A high-linearity 76–85-GHz 16-element 8-transmit/8-receive phased-array chip with high isolation and flip-chip packaging," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 10, pp. 2337–2356, Oct. 2014.
- [10] C. Cui, S.-K. Kim, R. Song, J.-H. Song, S. Nam, and B.-S. Kim, "A 77-GHz FMCW radar system using on-chip waveguide feeders in 65-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 11, pp. 3736–3746, Nov. 2015.
- [11] C. Beck *et al.*, "Industrial mmWave radar sensor in embedded wafer-level BGA packaging technology," *IEEE Sensors J.*, vol. 16, no. 17, pp. 6566–6578, Sep. 2016.
- [12] J. Lee, Y.-A. Li, M.-H. Hung, and S.-J. Huang, "A fully-integrated 77-GHz FMCW radar transceiver in 65-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2746–2756, Dec. 2010.
- [13] T. Mitomo, N. Ono, H. Hoshino, Y. Yoshihara, O. Watanabe, and I. Seto, "A 77 GHz 90 nm CMOS transceiver for FMCW radar applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 928–937, Apr. 2010.
- [14] T. Fujibayashi *et al.*, "A 76- to 81-GHz packaged single-chip transceiver for automotive radar," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, Sep. 2016, pp. 166–169.
- [15] W. Wang, Y. Takeda, Y.-S. Yeh, and B. Floyd, "A 20 GHz VCO and frequency doubler for W-band FMCW radar applications," in *IEEE 14th Topical Meeting Silicon Monolithic Circuits RF Syst. Dig. Papers*, Jan. 2014, pp. 104–106.
- [16] C. Bredendiek, N. Pohl, K. Aufinger, and A. Bilgic, "An ultra-wideband D-band signal source chip using a fundamental VCO with frequency doubler in a SiGe bipolar technology," in *IEEE RFIC Dig. Tech. Papers*, Jun. 2012, pp. 83–86.
- [17] S. Otaka, G. Takemura, and H. Tanimoto, "A low-power low-noise accurate linear-in-dB variable-gain amplifier with 500-MHz bandwidth," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1942–1948, Dec. 2000.
- [18] U. R. Pfeiffer and D. Goren, "A 20 dBm fully-integrated 60 GHz SiGe power amplifier with automatic level control," *IEEE J. Solid-State Circuits*, vol. 42, no. 7, pp. 1455–1463, Jul. 2007.
- [19] Ansoft HFSS, 15th ed. Pittsburgh, PA, USA: Ansoft Corp., 2013.
- [20] S. Trotta *et al.*, "A multi-channel Rx for 76.5 GHz automotive radar applications with 55 dB IF channel-to-channel isolation," in *Proc. Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Rome, Italy, 2009, pp. 192–195.
- [21] E. J. Wilkinson, "An N-way hybrid power divider," *IEEE Trans. Microw. Theory Techn.*, vol. 8, no. 1, pp. 116–118, Jan. 1960.
- [22] D. Kissinger, B. Sewiolo, H.-P. Forstner, L. Maurer, and R. Weigel, "A fully differential low-power high-linearity 77-GHz SiGe receiver frontend for automotive radar systems," in *Proc. IEEE 10th Annu. Wireless Microw. Technol. Conf.*, Clearwater, FL, USA, Apr. 2009, pp. 1–4.
- [23] D. Kissinger, B. Laemmle, L. Maurer, and R. Weigel, "Integrated test for silicon front ends," *IEEE Microw. Mag.*, vol. 11, no. 3, pp. 87–94, May 2010.
- [24] J. W. M. Rogers, D. Rahn, and C. Plett, "A study of digital and analog automatic-amplitude control circuitry for voltage-controlled oscillators," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 352–356, Feb. 2003.
- [25] B. A. Floyd, "A 16–18.8-GHz sub-integer-N frequency synthesizer for 60-GHz transceivers," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1076–1086, May 2008.
- [26] S. Kulhalli, S. Seth, and S.-T. Fu, "An integrated linear RF power detector," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 1, May 2004, p. I-625–8.
- [27] D. Kissinger, R. Agethen, and R. Weigel, "A versatile built-in test architecture for integrated millimeter-wave radar receiver front-ends," in *Proc. IEEE Instrum. Meas. Tech. Conf.*, May 2012, pp. 254–258.
- [28] K. Gentile and R. Cushing, "A technical tutorial on digital signal synthesis," Analog Devices Inc. 1999, pp. 1–122. [Online]. Available: <http://www.analog.com/en/education/education-library/technical-tutorial-dds.html>



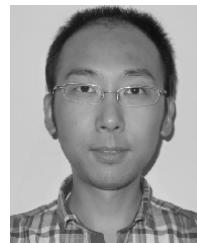
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