

Injection-Locked Wideband FM Demodulation at IF

Akshay Visweswaran, *Member, IEEE*, and John R. Long, *Fellow, IEEE*

Abstract—A low-power FM demodulator operating across a 2–10-GHz IF bandwidth for its application in wideband heterodyne receivers is presented. A four-stage ring oscillator locks to one-fourth of the input FM, thereby reducing the energy required for wideband demodulation. The measurements show that the oscillator is capable of locking to at least a modulating frequency of 400 MHz, and further testing is limited by the FM source. Linear demodulation of the quadrature-phased outputs is realized using a low-power folded CMOS mixer, even as the fractional bandwidth of the input FM approaches unity. The inductorless 65-nm CMOS prototype occupies 0.17 mm² and dissipates 3.2 mW from 1.2 V at the quiescent point. The measured SNR sensitivity is 8 dB and the demodulator bit-error rate is 0.1% at 10 Mb/s for a 45-mV_{pp} input signal at IF.

Index Terms—Class-AB, CMOS mixer, demodulator, differential amplifier, FM deviation, frequency divider, injection locking, intermediate frequency (IF), low power, ring oscillator, wideband.

I. INTRODUCTION

PORTABLE receivers for low-cost, high-speed wireless links should be compact, fully integrated, and consume minimal dc power. Co-optimization of systems and circuits is necessary to achieve energy-efficient low-power communication links [1]. Simple modulation schemes such as wideband frequency-shift keying (FSK) are currently of interest for wireless local- and personal-area communication, because they require low-complexity transceivers. However, power-efficient data transfers at rates up to 1 Gb/s are required for applications such as video streaming [2]. Demodulation at an intermediate frequency (IF) in a low-complexity heterodyne receiver [Fig. 1(a)] enables greater bandwidth handling and mitigates the impact of receiver flicker noise, limited port isolation, and signal interference often encountered in homodyne receivers. Circuit operation at a reduced fractional bandwidth¹ through an appropriate choice of IF can potentially simplify the implementation of a wideband receiver, thereby saving power and chip area.

Wideband receiver performance at rates approaching 1 Gb/s is limited by power consumption, which increases in proportion to the data rate. Demodulation of wideband signals is further restricted by the challenge and complexity of designing interface circuits and delay networks (at RF and IF),

Manuscript received December 6, 2015; revised April 5, 2016 and June 17, 2016; accepted August 22, 2016. Date of publication November 7, 2016; date of current version January 30, 2017. This paper was approved by Associate Editor Hossein Hashemi.

A. Visweswaran is with the Electronics Research Laboratory, Delft University of Technology, 2628CD Delft, The Netherlands (e-mail: a.visweswaran@tudelft.nl).

J. R. Long is with the Department of Electrical and Computer Engineering, University of Waterloo, Waterloo, ON N2L 3G1, Canada.

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2016.2605658

¹The ratio between the modulation frequency-span and the center-frequency is the fractional bandwidth.

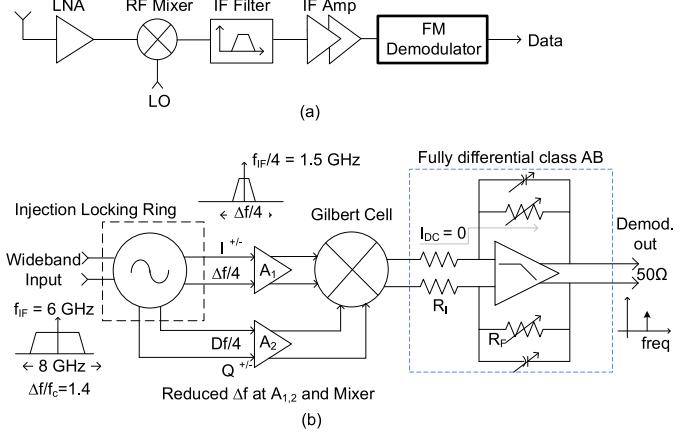


Fig. 1. Block diagrams of (a) heterodyne receiver with demodulation at IF and (b) injection-locked wideband IF demodulator developed in this paper.

despite the availability of submicrometer transistors having transit frequencies in excess of 250 GHz. While a tradeoff between bandwidth and power consumption is encountered in circuit design routinely, the phase linearity of conventional passive delays or phase-shift networks necessary for demodulation remains bandlimited. At present, there have been few demonstrations of integrated wideband circuits that verify the feasibility of energy-efficient communication links, e.g., the 3–5-GHz ultrawideband FM transceiver presented in [3]. This paper presents a wideband low-power demodulator based on quadrature-phased division of FM deviation. The demodulator operates across 2–10-GHz IF ($\Delta f/f_c = 1.4$), while consuming 0.32 nJ/b at a 10-Mb/s data rate [4]. The measurements verify that the oscillator is capable of locking to a modulating rate of at least 400 MHz. This 65-nm CMOS prototype optimized for a ~10-Mb/s data rate is the first demonstration of division of FM deviation and a fully-integrated multigigahertz low-power IF demodulator.

Section II describes division of the FM deviation and subsequent demodulation, with an emphasis on circuit design and operation. The fully differential Class-AB amplifier developed in [5] is presented in Section III. Extensive measurements characterizing the 65-nm CMOS prototype demodulator are detailed in Section IV, along with stand-alone characterization of the oscillator and its response to external noise and FM. Section V summarizes this paper.

II. LOCKED-IN DEVIATION DIVISION AND FM DEMODULATION

Injection-locked ring oscillators perform frequency division, and multiphase signal injection is known to widen the locking range of these dividers [6]. Four-stage oscillators requiring antiphase signals fit seamlessly into differential circuit chains, and inductorless implementations are widely used for

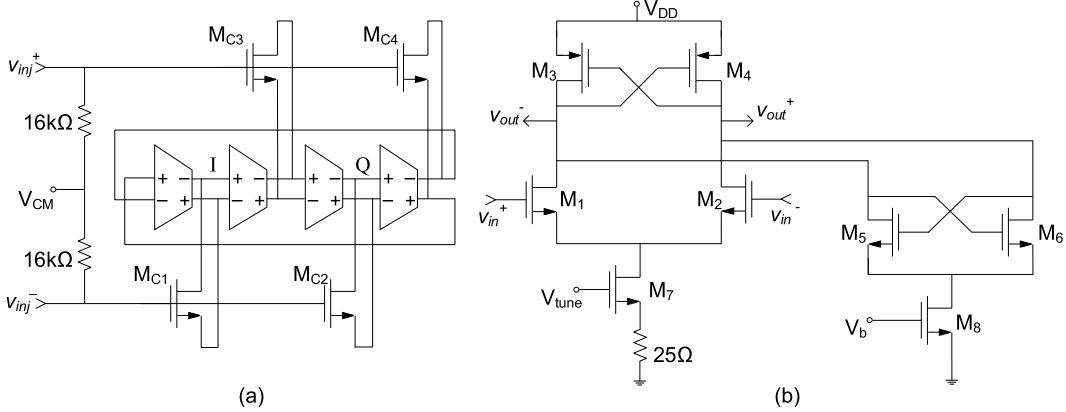


Fig. 2. (a) Injection-locked four-stage ring oscillator. (b) Implementation of each stage.

quadrature-phased frequency division of a local oscillator signal. These circuits are inherently compact in die area, require a lower input drive compared with dynamic CMOS frequency dividers (see [7]), and can operate across nearly two octaves in the low-gigahertz region [4], [8]. Since the output discharges entirely during each cycle, the free-running oscillator does not retain information from the previous cycle. This allows the oscillator to lock to a wide range of input frequencies (compared with tuned oscillators [9]) and track the modulation of a wideband FM signal with ease. The remarkable ability of these circuits to lock to FM signals and divide the frequency is the subject of this paper. It has remained an unexplored circuit technique for wideband demodulation.

It is important to note that while the locked-in oscillator reduces FM deviation by virtue of division, the modulation remains unaltered. This effect was observed by Beers [10], and is studied in detail in this section. The operating bandwidth is therefore reduced by the division factor (assumed to be four here), which eases the bandwidth/power consumption tradeoff in the stages that follow. Time instantaneous quadrature signals produced by the locked-in ring can be utilized for FM detection, thereby avoiding the need for wideband, true-time delays, and complex frequency plans for quadrature-phase generation. Other benefits of this approach to demodulation are: 1) data-rate-independent power consumption; 2) wideband operation; 3) insensitivity to noise and additive amplitude modulation (AM) of the input RF; 4) a requirement for low distortion is not imposed on the IF amplifier; and 5) the operation of the oscillator at one-fourth of the intermediate frequency enables a higher IF and a lower fractional bandwidth. The minimum signal amplitude required for injection locking and its susceptibility to in-band interferers are alleviated by applying the technique at IF rather than RF, because potential blockers can be filtered by the preceding stages. A wideband IF preamplifier is required in the chain [Fig. 1(a)], which is not implemented in the prototype demodulator developed in this paper.

Fig. 1(b) shows a block diagram of the proposed IF demodulator for the heterodyne receiver of Fig. 1(a). Quadrature outputs from the injection-locked input stage are interfaced through buffers $A_{1,2}$ to a Gilbert mixer. The power consumption of the interface buffers and the mixer are considerably reduced by the rail-to-rail output provided

by the ring oscillator and reduction of the signal bandwidth by FM division [illustrated in Fig. 1(b)]. The low-frequency demodulated output from the mixer is buffered for 50-Ω measurement using a differential Class-AB operational amplifier [5], which is configured in shunt feedback.

A. Oscillator Circuit Design and Operation

The four-stage ring oscillator shown in Fig. 2(a) constitutes the input stage. It is differentially injection locked to the wideband input signal through gain stages $M_{C1}-4$. Each stage consists of a differential pair loaded by a cross-coupled pMOS pair [shown in Fig. 2(b)], which provides local positive feedback to ensure that the outputs charge and discharge rapidly. Cross-coupled transistors $M_{5,6}$ (controlled by V_b) provide additional regenerative gain in the case of start-up failure. A frequency tuning range from 0.8 to 1.9 GHz is implemented via a variable resistor at the tail node, where M_7 is operated in triode and controlled by V_{tune} . The oscillator stages draw between 350 and 500 μ A, depending on V_{tune} . The dc voltage V_{CM} [Fig. 2(a)] ensures that transistors $M_{C1}-4$ operate in saturation and provide sufficient gain to prevent the oscillator from falling out of lock and distorting the demodulated waveform. Its optimal value cannot be determined *a priori* and is therefore obtained iteratively. All measurements have been performed with V_{CM} and V_b set to 0.6 and 0 V, respectively ($V_{DD} = 1.2$ V).

Fig. 3 shows the large-signal operation of one of the stages and the associated voltage and current waveforms. The triode resistance of transistor M_7 [see Fig. 2(b)] is represented by R_{ss} . Consider node ‘x’ and voltage v_x in Fig. 3(a). The impulse-like discharge current sunk by M_1 is sourced by transistor M_3 , after which it cuts off [annotated in Fig. 3(c) as ‘ i_{M3-1} ’]. The peak output swing appears across the drain-source of M_{C1} , which operates in saturation conducting a dc current (I_Q) sourced by M_4 and sunk by M_1 , noted as ‘ i_{M4} ’ in Fig. 3(a) and (c). Voltage V_{CM} biasing the gate of M_{C1} determines I_Q and the Q -point transconductance of M_{C1} . In the second half of the cycle, node ‘y’ is discharged via M_2 [‘ i_{M4-2} ’ in Fig. 3(c)], resulting in a swap of drain and source terminals for M_{C1} . Transistor M_{C1} conducts I_Q sourced by M_3 (now biased on) and sunk by M_2 —noted as ‘ i_{M3} ’ in Fig. 3(b) and (c). The drain–source overdrive (of M_{1-4}) required to conduct the steady-state value of I_Q

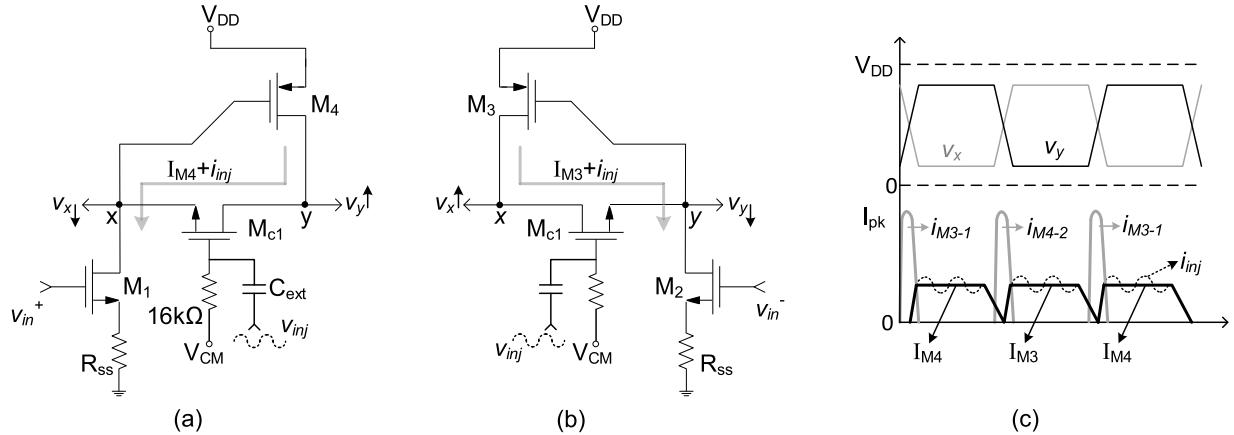


Fig. 3. Single stage circuit during large signal operation. (a) M_3 and M_2 are cut-off, and current flows from node y to node x , (b) M_1 and M_4 are cut-off and current flows from node x to node y . (c) An illustration showing current waveforms during large-signal operation.

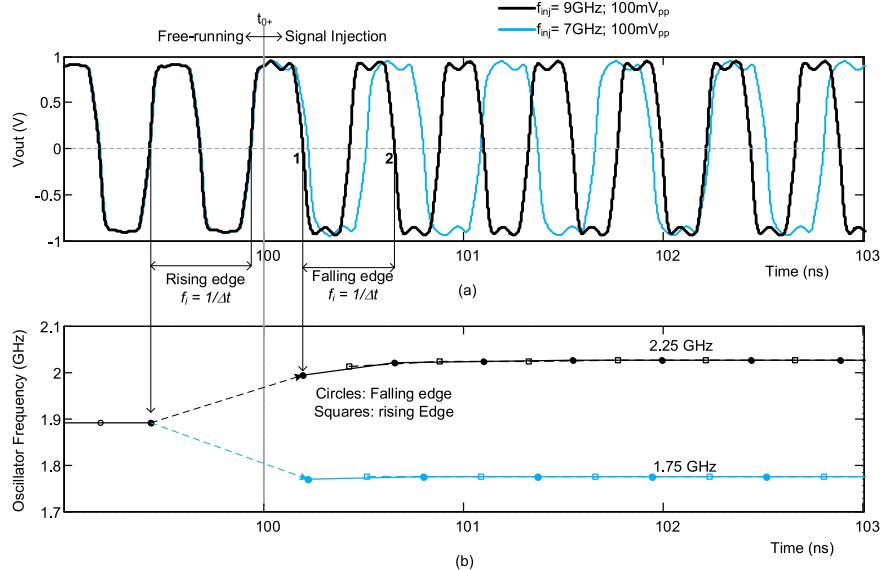


Fig. 4. Simulated locking responses for f_{inj} equal to 9 and 7 GHz are applied at 100 ns. (a) Time-domain simulation of the output voltage. (b) Instantaneous frequency versus time.

determines the peak-to-peak swing at nodes ‘ x ’ and ‘ y ’, i.e., v_x and v_y .

When an ac signal rides the bias voltage at the gate of the coupling transistors (e.g., M_{c1}), it drives a signal current into the oscillator loop, which drops across triode impedances loading its drain/source terminals (e.g., nodes ‘ x ’ and ‘ y ’). The resulting envelope (see Fig. 4) on the output triggers the charging and discharging of the subsequent stage and thereby draws the oscillator into lock. The envelope signal is eliminated by hard-limiting interface buffers. Fig. 4 shows the simulated time-domain response of the oscillator ($f_0 = 1.88\text{ GHz}$ and $V_{CM} = 0.6\text{ V}$) when 100-mV_{pp} locking signals with static frequencies of 7 and 9 GHz, respectively, are applied at a time of 100 ns. Due to the absence of memory in the loop, the oscillator locks to the frequency tones at wide offsets from its free-running frequency almost instantaneously (two cycles in this example), suggesting the ability to lock binary FSK at rates in the gigabit-per-second range. The binary FSK modulation rate is typically orders of magnitude below the carrier (f_c) and does not affect the tracking ability of the locked-in ring oscillator. Simulations suggest that the demodulator detects FM coherently when the carrier is typically one order of magnitude

higher in frequency than the modulating signal. This limits the maximum data rate to $\sim 400\text{ Mb/s}$ at the 2-GHz band edge and $\sim 2\text{ Gb/s}$ between 8 and 10 GHz.

B. Transformation of the FM Modulation Index

For a given FM modulation index, Bessel function coefficients (BFCs) fingerprint the signal spectrum at offsets from the carrier frequency [11]. These are evaluated via simulation of the locked-in oscillator to verify the FM transmission characteristics predicted by the analytical form of the expected output. A typical FM signal modulated by a single tone $\cos \omega_m t$ is:

$$v_{FM}(t) = X_o \cos \left[\omega_c t + \Delta \omega \int_0^t \cos(\omega_m t) dt \right] \\ = X_o \cos [\omega_c t + \beta \sin(\omega_m t)], \quad (1)$$

where X_o is the amplitude and ω_c and ω_m are the carrier and modulating angular frequencies, respectively. The FM deviation $\Delta \omega$ is a measure of the excursion that the instantaneous frequency takes about ω_c . The ratio $\Delta \omega / \omega_m$ [β in (1)] is defined as the modulation index. In addition, the ratio $\Delta \omega / \omega_c$ is defined as the deviation ratio $-D_r$ and twice its value is the

TABLE I
BFCs FOR DIFFERENT MODULATION INDICES

Theory	β	J_0	$J_1, J_0/J_1 $	$J_2, J_0/J_2 $	$J_3, J_0/J_3 $	$J_4, J_0/J_4 $	$J_5, J_0/J_5 $	$J_6, J_0/J_6 $	$J_7, J_0/J_7 $
0.25	0.9848	0.0077 18dB	0.0070 42.1dB						
1	0.765	0.44, 4.8dB	0.1149, 16.5dB	0.0195, 31.9dB					
4	-0.40	-0.066, 15.58dB	0.3641, 0.75dB	0.4301, -0.7dB	0.2811, 3dB	0.1320, 9.56dB	0.0345, 21.22dB	0.0151, 28.4dB	
Measurement									
	β	$ J_0/J_1 $	$ J_0/J_2 $	$ J_0/J_3 $	$ J_0/J_4 $	$ J_0/J_5 $	$ J_0/J_6 $	$ J_0/J_7 $	
Input (Fig. 19b)	4	15.32dB	0.72dB	-0.66dB	2.9dB	9.62dB	19.60dB	29.2dB	
Output (Fig. 19c)	1	4.82dB	16.82dB	31.64dB					
Input (Fig. 20a)	1	4.82dB	16.49dB	30.18dB					
Output (Fig. 20b)	0.25	18.58dB	42.12dB						
$J_n(\beta) = \frac{1}{2\pi} \int_{-\pi}^{\pi} e^{j(\beta \sin x - nx)} dx$									

signal's fractional bandwidth. The propagating phase $\phi(t)$ is the argument of the cosine function in (1). The instantaneous frequency equals the time derivative of phase:

$$\omega(t) = \frac{d\phi(t)}{dt} = [\omega_c + \Delta\omega \cdot \cos(\omega_m t)]. \quad (2)$$

When an FM signal is passed through a factor 'n' frequency divider, the resulting division of FM deviation and the carrier frequency is obtained by dividing $V_{FM}(t)$ from (1) by 'n':

$$v_o(t) = X_c \cos \left[\frac{\omega_c}{n} t + \frac{\beta}{n} \sin(\omega_m t) \right], \quad (3)$$

where X_c is the signal amplitude at the oscillator's output. A key observation from (3) is that the division of FM deviation is brought about by the transformation of the modulation index (now β/n) and the retention of the modulating signal. This is confirmed via SpectreRF simulation of the locked-in oscillator. Fig. 5 shows the spectrum of the divided FM deviation obtained at the output of the locked-in oscillator. The input FM signal has $f_c = 5$ GHz, $f_m = 100$ MHz, and $\beta = 4$. The BFCs for modulation indices of 1, 0.25, and 4 are listed in Table I [12], along with their ratio with the carrier-specific coefficient J_0 . It is seen that the offset tones normalized to the carrier tone in Fig. 5 agree well with the theoretical values listed in Table I. The harmonics seen in Fig. 5 are characteristic of FM distortion, where the deviation around harmonics of the carrier increases by a factor equal to the harmonic in question. The experimental results that validate the theory and simulation are presented in Section IV.

C. Quadrature Signals and FM Demodulation

In general, envelope detection of the derivative of an FM signal accomplishes FM demodulation [11]. Both filter-domain (see [2], [13]) and delay line implementations (see [14]–[16])

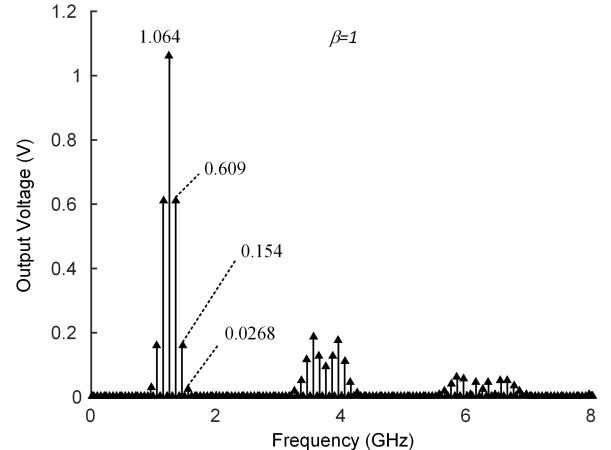


Fig. 5. Transformation of modulation index. Differential output of the locked-in oscillator showing division of FM deviation when locked to an 80-mV_{pp} input having $f_c = 5$ GHz and $f_m = 100$ MHz. The input modulation index of four is translated to one after division by four.

composed of differentiators are band limited to a narrow window in frequency where the phase gradient ($d\phi/df$) of the central passive network remains constant. For wideband operation, the realization of a controllable pure time delay entails complexity that often results in relatively high power consumption and large chip area [17]–[19]. It will be shown that the quadrature-phased outputs inherent in the locked-in ring oscillator simplify demodulation by circumventing the need for an auxiliary wideband true-time delay. In this section, a simple analytical prediction of the locked-in oscillator's quadrature-path delay is verified via simulation. It is then used to derive the demodulator's wideband characteristic. Under perfect lock, the Q and I signals [see Fig. 2(a)] are expected to be shifted in time by one-fourth of the instantaneous time period. For the FM input signal represented by (1) and the

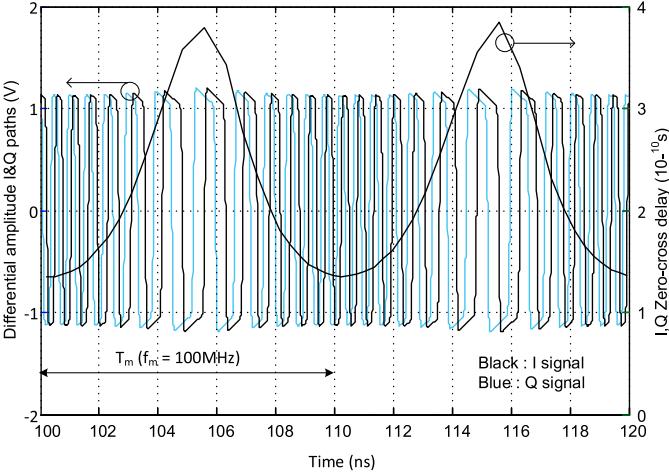


Fig. 6. Simulated transient I and Q signals and the delay between their zero crossings for $f_c = 5$ GHz, $f_m = 100$ MHz, and an FM deviation of 2.5 GHz ($\beta = 25$).

output of the locked-in oscillator represented by (3), the I and Q signals may be written as:

$$\begin{aligned} v_{\text{FM}_I}(t) &= X_c \cos \left[\frac{\omega_c}{n} t + \frac{\beta}{n} \sin(\omega_m t) \right] \\ &= X_c \cos [\omega'_c t + \beta' \sin(\omega_m t)], \end{aligned} \quad (4)$$

and

$$v_{\text{FM}_Q}(t) = X_c \cos [\omega'_c(t - \tau_d(t)) + \beta' \sin(\omega_m(t - \tau_d(t)))], \quad (5)$$

where ω'_c , and β' are the scaled-down carrier frequency and modulation index, respectively. The delay between the two branches τ_d determines the demodulator characteristic and is calculated using $\omega(t)$ defined by (2). It can be expressed as the sum of a fixed delay at f_c and a time-varying function of the modulating signal:

$$\begin{aligned} \tau_d(t) &= \frac{2\pi}{4\omega(t)} = \frac{1}{4} \left[\frac{1}{\{\beta' f_m \cos(\omega_m t) + f'_c\}} \right] \\ &= \frac{1}{4f'_c} \left[1 + \frac{-\cos(\omega_m t)}{\{\cos(\omega_m t) + 1/D_r\}} \right]. \end{aligned} \quad (6)$$

The ring oscillator's output interface consists of a series of hard-limiting inverters [Fig. 1(b)] switching between 0 and V_{DD} . In the midst of harmonics that comprise the square wave, the frequency modulation is ‘sampled’ at the zero crossings of the hard-limited FM signal. Fig. 6 shows a SpectreRF simulation of the voltages on the Q and I branches of the locked oscillator. The input signal has $f_c = 5$ GHz, $f_m = 100$ MHz, $\beta = 25$, $\Delta f = 2.5$ GHz, and the fractional bandwidth $\Delta f/f_c$ equal to 1. The delay between the zero crossings of the Q and I signals is also plotted in Fig. 6 against the right-hand Y -ordinate. The delay predicted by (6) compares well with the simulation, as seen from their comparison in Fig. 7(a). A superposition of the theoretical and simulated delays for a lower modulation index ($\beta = 4$) where $f_c = 8$ GHz, $f_m = 250$ MHz, and $\Delta f/f_c$ equal to 0.25 is shown in Fig. 7(b). A theoretical minimum ratio of ω_c/ω_m of

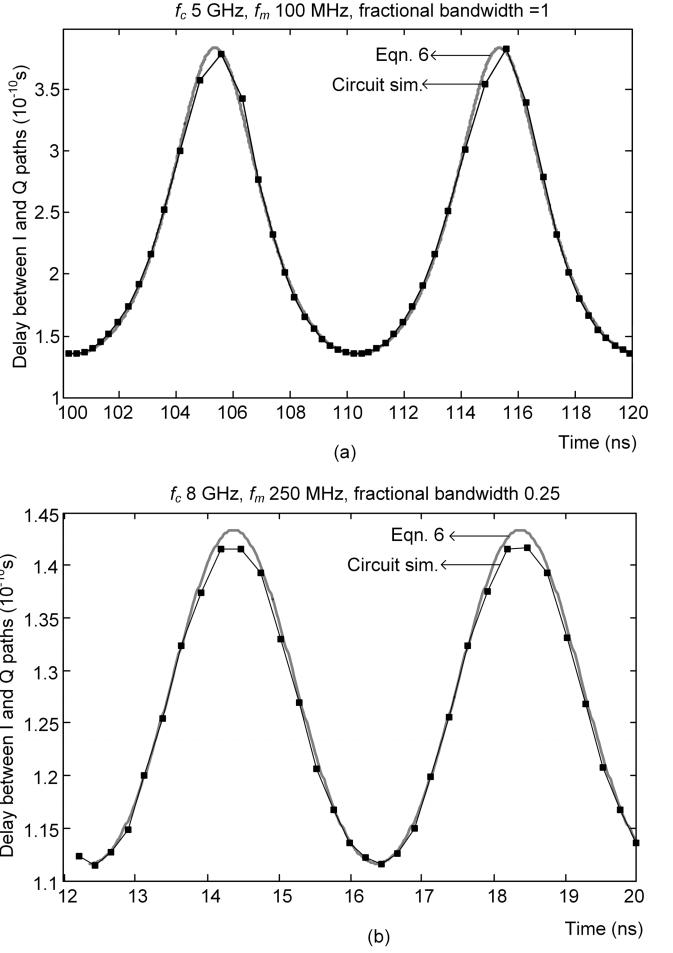


Fig. 7. Simulated delay between the Q and I signal paths recorded at zero crossings, compared with the delay predicted by (6) for (a) $f_c = 5$ GHz, $f_m = 100$ MHz, and an FM deviation of 2.5 GHz ($\beta = 25$) and (b) $f_c = 8$ GHz, $f_m = 250$ MHz, and an FM deviation of 1 GHz ($\beta = 4$).

eight is reached when applying Shannon's sampling limit to the scaling down of f_c by a factor of 4.

The Gilbert mixer driven by large signals at either port behaves like a phase detector. Its low-pass-filtered output current, describing the FM demodulator's characteristic, is proportional to the difference between the phases of (4) and (5) and may be expressed as [11], [20]:

$$i_O(t) \alpha [\omega'_c \tau_d(t) + \beta' \{\sin(\omega_m t) - \sin(\omega_m(t - \tau_d(t)))\}]. \quad (7)$$

Evaluating (7) for the limit $\tau_d \rightarrow 0$ (assuming $\omega_c \gg \omega_m$ and that τ_d equals $\pi/2\omega_c$) and using the simplification used in [31] for the evaluation of delay-line demodulators results in an approximation that sheds light on the recovery of the modulating signal:

$$\begin{aligned} \lim_{\tau_d \rightarrow 0} i_O(t) &= \beta' \tau_d \frac{[\sin(\omega_m t) - \sin(\omega_m(t - \tau_d))]}{\tau_d} \\ &= \beta' \tau_d \frac{d(\sin(\omega_m t))}{dt} = \frac{\pi}{2} D_r \cos(\omega_m t). \end{aligned} \quad (8)$$

Equation (8) predicts undistorted detection of the modulating signal. However, Fourier coefficients of (7) depend on ω_m and the deviation ratio D_r . The normalized form

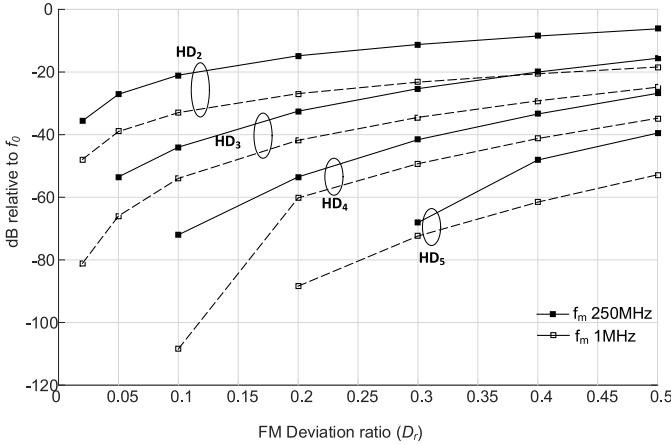


Fig. 8. Harmonic distortion of (7) versus deviation ratio for f_m equal to 1 and 250 MHz and f_c equal to 5 GHz.

of $i_0(t)$ from (7) is simulated using MATLAB to evaluate the output characteristic and baseband distortion assuming a constant of proportionality equal to one. The delay τ_d is described by (6). Harmonic distortion components (HD₂–HD₅) are plotted in Fig. 8 for a 5-GHz carrier modulated at 10 and 250 MHz. Baseband distortion increases with D_r , resulting in stringent filtering requirements. However, in the case of FSK demodulation, the data can be reconstructed easily via hard-limiting inverter stages. The demodulator's characteristic obtained from SpectreRF simulation of the entire circuit [i.e., components of Fig. 1(b)] is shown in Fig. 9. The normalized fundamental component of the mixer's output current is plotted against D_r and compared with the normalized theoretical prediction from (7). A good correlation is seen between the theory and simulation, while the demodulator's wideband capabilities are clearly visible, as the mixer's output current varies almost linearly even as the fractional bandwidth approaches unity. Characterization data for the demodulator prototyped in a 65-nm CMOS are presented in Section IV.

D. Folded Gilbert Mixer and Interface Buffers

The folded implementation of the four-quadrant Gilbert mixer is described in [4] and shown in Fig. 10(a). Complimentary transistors at its ports allow accurate bias regulation and common-mode rejection, while the fully-balanced implementation minimizes feedthrough. Current source I_2 biases transistors $M_{5,6}$, and the dc current difference between I_1 and I_2 is equally distributed between transistors M_{1-4} of the switching quad. This allows accurate bias control to tailor the current in the RF and quad transistors for large-signal drive at either port, where it operates as a phase detector [21]. Measurements are made with I_1 varied between 125 and 600 μ A, while maintaining 25 μ A in each of transistors M_{1-4} . The common-mode feedback amplifier is a folded cascode (FC) amplifier that consumes 30 μ A. The compensation capacitance C_c stabilizes the CMFB loop with a minimum current requirement of 25 μ A in each of transistors M_{1-4} .

Interface buffers $A_{1,2}$ [Fig. 1(b)] are shown in Fig. 10(b). They consist of a three-inverter cascade. Cross-coupling inverters between the paths preserve the desired 180° phase difference. The output dc is set to the midsupply using a

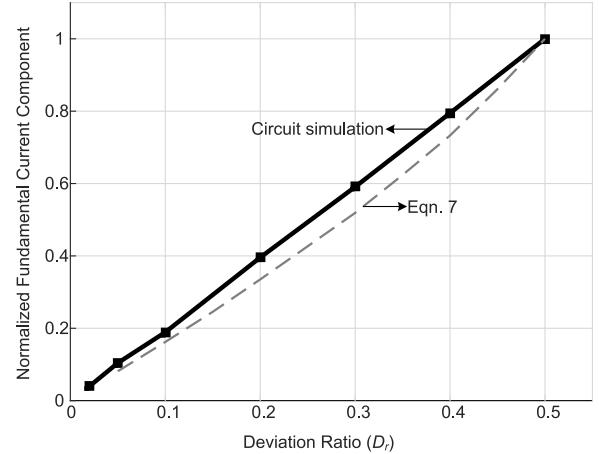


Fig. 9. Normalized plot of the mixer's fundamental output current component versus deviation ratio for f_c = 5 GHz and f_m = 10 MHz, compared with the characteristic predicted by (7).

resistive divider, and the interstage coupling network has a 40-MHz high-pass cutoff frequency that does not attenuate the propagating signal.

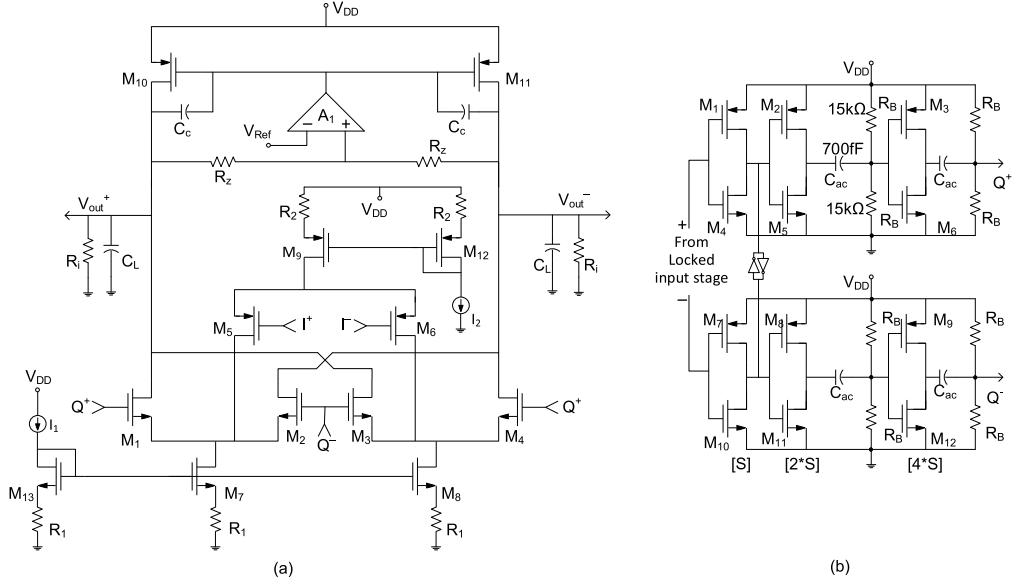
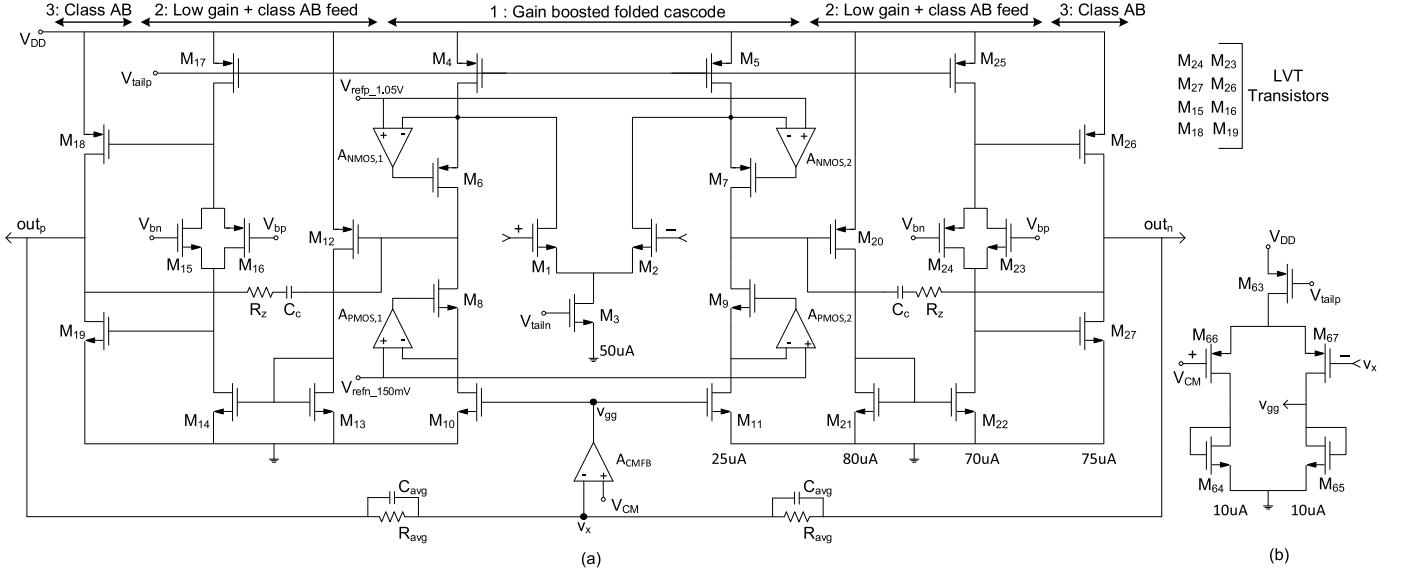
III. DIFFERENTIAL THREE-STAGE CLASS-AB AMPLIFIER: TOPOLOGY AND DESIGN

The fully-differential Class-AB amplifier developed for the prototype IF demodulator [5] is configured in shunt feedback. It interfaces the demodulated output to a 50- Ω environment. The amplifier is biased for low power consumption (800- μ A, 83-dB open-loop dc gain, and 70-MHz Unity-Gain Bandwidth), and it is compensated for a 60° phase margin when driving a 10-pF load. Differential operation maximizes the output swing from a given V_{DD} (1.8 V_{pp} from 1.2 V), suppresses even-order distortion, and rejects noise and interference arising from cointegration with other subcircuits.

The amplifier schematic, annotated with branch currents, is shown in Fig. 11, and schematics of the amplifier's subcells are shown in Fig. 12(a)–(c). The first stage is a fully-differential, gain-boosted FC amplifier. Looking at the second-stage half-circuit, low-gain inversions from M_{20} and M_{22} drive the Monticelli CMOS pair $M_{23,24}$ [22] that biases the third Class-AB stage. The diode-connected transistor M_{21} is a wideband load at the drain of M_{20} ; however, a significant second-stage pole is seen at the output of M_{22} . When the CMFB loop is operating, dc voltage at the first-stage output is determined by the V_{SG} requirement of M_{20} (and M_{12}) to conduct current sourced by M_{25} (and M_{17}), as determined by the mirror ratio between $M_{21,22}$ and $M_{13,14}$ [23], [24]. Trimming C_p controls the bandwidth of the gain boost loop and the doublet seen in the frequency response.

A. Small-Signal Analysis

The uncompensated amplifier has four important poles [5], which are evaluated in detail here. The dominant pole is located at the output of the first stage. Time constants of the third and second stages account for the second and third poles, respectively. The fourth pole is determined by the time

Fig. 10. (a) Folded CMOS Gilbert mixer.(b) Interface buffers A_{1,2}.Fig. 11. Circuit diagrams of (a) differential three-stage Class-AB amplifier and (b) A_{CMFB}.

constant associated with the source nodes of M_{6,7}. The doublet caused by gain boosting is placed between the unity gain frequency and the second pole of the amplifier [25]. A small-signal simulation of the amplifier's differential and common-mode responses for a 50- Ω ||10-pF load is shown in Fig. 13, for a total bias current of 800 μ A drawn from V_{DD}.

The poles of a Miller-compensated three-stage amplifier assuming one pole per stage are derived in [26] and shown in Fig. 14(a). Gain boosting increases the output impedance and therefore permits a lower C_c. Increasing g_{m3} increases gain and aids pole splitting (see 2 mA, for example, in Fig. 13). As a first-order approximation, the second stage's time constant is independent of networks loading other stages and the Miller capacitance. Placing the third pole P₃ outside the unity-gain bandwidth after pole splitting avoids the need for nested Miller compensation. The right half-plane zero due to C_c is transformed to a left half-plane zero using R_z. The pole

created by R_z and C₁ does not degrade the phase margin. The complimentary Monticelli bias cell transistors form a feedback loop indicated in Fig. 14(b). Signal paths G_f and H_r are the forward and reverse gains at dc, respectively. Solving for the input impedance [27] yields:

$$Z_{in} = \left[\frac{Z_{0_in}}{1 - G_f H_r} \right],$$

where

$$Z_{0_in} = \left[\frac{1}{g_{mn}} \| r_{ds1} \| r_{ds_n} \right], \quad (9)$$

$$G_f = \left[\left\{ \frac{\left(\frac{1}{g_{mp}} \| r_{ds2} \right)}{\left(\frac{1}{g_{mp}} \| r_{ds2} + r_{ds_np} \right)} \right\} + g_{mn} \left\{ \frac{1}{g_{mp}} \| r_{ds2} \| r_{ds_np} \right\} \right], \quad (10)$$

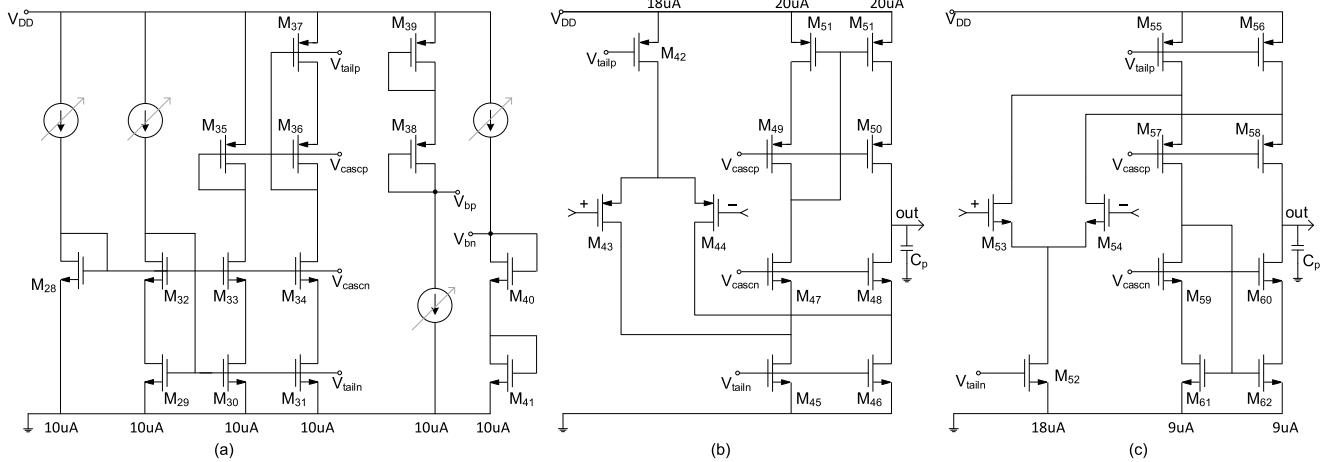


Fig. 12. Circuit diagrams of (a) bias block, and (b) A_p MOS, and (c) A_n MOS from Fig. 11.

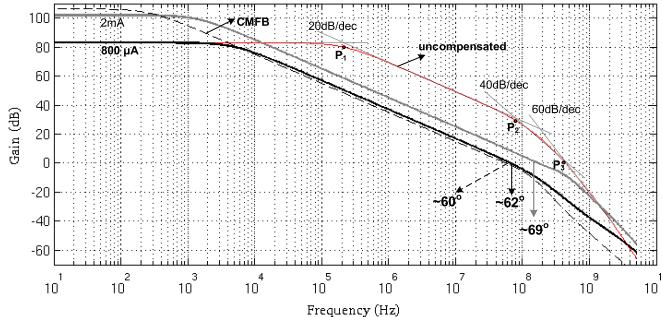


Fig. 13. Simulated differential and common-mode small-signal responses of the amplifier with phase margins annotated.

and

$$H_r = \left[\left\{ \frac{\left(\frac{1}{g_{mn}} \| r_{ds1} \right)}{\left(\frac{1}{g_{mn}} \| r_{ds1} + r_{ds_np} \right)} \right\} + g_{mp} \left\{ \frac{1}{g_{mn}} \| r_{ds1} \| r_{ds_np} \right\} \right]. \quad (11)$$

Z_{0_in} is the open-loop dc impedance loading node ‘a’ and g_{mn} , and g_{mp} are the transconductances of M_n and M_p , respectively. The output resistances (r_{out}) of M_1 and M_2 are r_{ds1} and r_{ds1} , respectively, and r_{ds_np} is the parallel combination of the r_{out} of M_n and M_p . Keeping $g_{mn} \approx g_{mp}$ in the presence of the passive transfer [first terms in (10) and (11)] ensures that the loop gain $G_f H_r$ is less than one to ensure stability. From Fig. 14(b), Z_{in} is 5.38 kΩ, the loop gain is 0.70, and the capacitance (C_L) loading node ‘a’ is ~ 90 fF. The second-stage pole ($Z_{in}C_L$) predicted at 354 MHz is in close proximity to P_3 at 385 MHz (see Fig. 13), validating the analysis. A measurement summary of the amplifier’s stand-alone performance [5] is given in Table II.

IV. MEASUREMENT RESULTS AND DISCUSSION

A micrograph of the $624 \times 277-\mu\text{m}^2$ demodulator prototype (core area) implemented in the 65-nm CMOS is shown in Fig. 15(a). The chip was mounted on a custom test board (PCB) for measurement. All bias nodes and the output are wire bonded to the PCB, while the RF input is

probed on-die. Fig. 15(b) shows a micrograph of the ring oscillator characterized stand-alone.

Measured spectra of the oscillator at band edges of 900 MHz (−13.4-dBm output) and 1.8 GHz (−14.8-dBm output) are shown in Fig. 16. The tuning range is 67% centered at 1.35 GHz.

The 2–10-GHz input bandwidth has been measured in subbands of 1 GHz [see setup in Fig. 17(a)]. National Instruments arbitrary waveform generator (AWG) cards synthesize linearly modulated analog FM signals of 1-GHz bandwidth that drive (off-chip) upconversion I/Q modulators to produce a wideband signal at the desired f_c . Programmable dc offset correction and I/Q phase correction minimize carrier feedthrough and power in the image band, respectively. The digital modulation frequency range of the AWG is 200 kb/s to 2 Mb/s.

The measurement setup shown in Fig. 17(b) combines noise and the input signal. Attenuators in both signal paths provide gain control, and a bandpass filter sets the noise bandwidth to 4.34–6.75 GHz (insertion loss <3 dB). Signal and noise power is measured at reference plane ‘Y’ (i.e., the probe head) using an HP-E4419A power meter and calibrated sensor head.

A 1-GHz bandwidth analog FM signal applied to the demodulator input is divided down by a factor of 4 to 250 MHz. For example, the 4–5-GHz bandwidth input signal of Fig. 18(a) is reduced to 1–1.25 GHz at the output of the locked-in oscillator [Fig. 18(b)]. Fig. 18(b) shows the spectrum over a frequency range wide enough to include FM harmonics. The suppression of harmonics is better than 20 dB, which indicates that the oscillator is operating within its locking range. As seen from the measured output in Fig. 18(b), the bandwidths of FM harmonics scale with the harmonic in question (as predicted in Fig. 5).

The measured division of FM deviation and translation of modulation index predicted by the theory and simulation are compared in Figs. 19 and 20. The FM input is generated by modulating a wideband voltage-controlled oscillator (VCO)—Hittite HMC586LC4B—using a laboratory signal source as shown in Fig. 17(b). The 4–8-GHz VCO has a near-constant sensitivity of ~ 0.4 GHz/V between 4.5 and 6 GHz.

TABLE II
MEASUREMENT SUMMARY OF THE FULLY-DIFFERENTIAL CLASS-AB AMPLIFIER [5]

65-nm CMOS Amp.	V _{DD} (V)	R _L / C _L (Ω/F)	R _Z , C _c (Ω, pF)	UGB (MHz)	Q _{point} I _{DC} (mA)	V _{out} (V _{pp})	S.R. (V/μs)	THD+N/freq (dB/kHz)	Overshoot, Damping fact.
High Power*	1.2	50–8/50p	850, 0.52	110	3.9	1.6	42	-82.6/150	1.1%, 0.82
Low Power*	1.2	50/10p	850, 0.52	75	0.8	1.6	42	-74/150	1.4%, 0.80

*The difference b/w the high and low power configurations is the current in the Class-AB arm, and load drive ability.

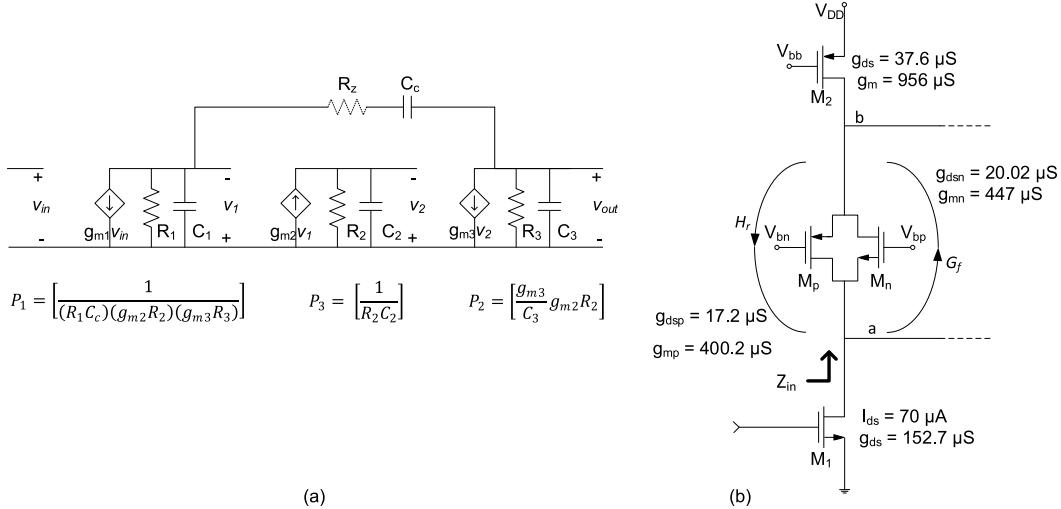


Fig. 14. (a) Simplified small-signal circuit used for analysis. (b) Transistor operating point parameters used to evaluate (9)–(11).

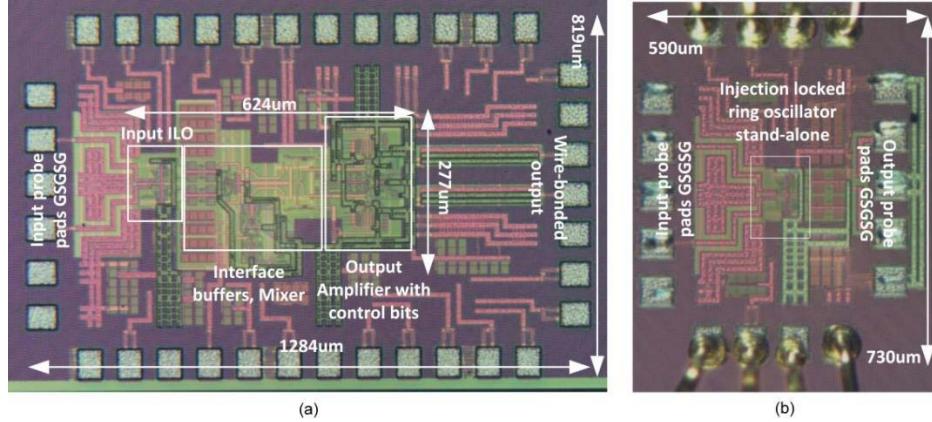


Fig. 15. 65-nm CMOS chip micrographs of (a) IF demodulator with $624 \times 277-\mu\text{m}^2$ core area and (b) stand-alone injection-locking oscillator.

Fig. 19(a) and (b) shows the simulated and measured input waveforms for a 5-GHz carrier modulated at 100 MHz with $\beta = 4$, respectively. Fig. 19(c) shows the spectrum of the fundamental FM output. The modulation index and bandwidth scale by a factor of four as predicted by theory. The experiment was repeated with a distorted input generated using overdriven back-to-back ZRON-8G amplifiers. The unaltered output confirms a low distortion requirement is not imposed on the IF amplifier. The verification at higher modulation rates is shown in Fig. 20, where a 7.5-GHz carrier is modulated at 400 MHz. The modulation index of 1 is scaled at the output to 0.25. The input impedance at the tuning port of the Hittite VCO limits β to <0.3 for modulating frequencies >450 MHz. BFC ratios obtained from the spectra in Figs. 19 and 20 are tabulated in Table I, showing a good comparison with the theory.

The oscillator's locking profile measured with V_{CM} [see Fig. 2(a)] set to 0.6 V is shown in Fig. 21, for free-running frequency (f_0) values of 1.25, 1.5, and 1.75 GHz [see the test setup in Fig. 17(b)]. For this measurement, the noise source is disconnected. The locking sensitivity is measured at each input frequency, with the oscillator first reset to f_0 . The signal path and source are calibrated for losses and errors, respectively. The locking sensitivity reduces as the offset from $4f_0$ increases. However, V_{CM} can be optimized for gain (i.e., increase current I_Q described in Section II-A). The locking range and sensitivity at a given frequency increase with V_{CM} as seen from the measurements in Fig. 21(b). The entire 2–10 GHz band can be covered without frequency tuning with V_{CM} set constant at 0.6 V at 400-mV_{pp} input swing.

The demodulated output for the test setup of Fig. 17(a) is shown in Fig. 22(a). The input RF band is 4–5 GHz, V_{CM}

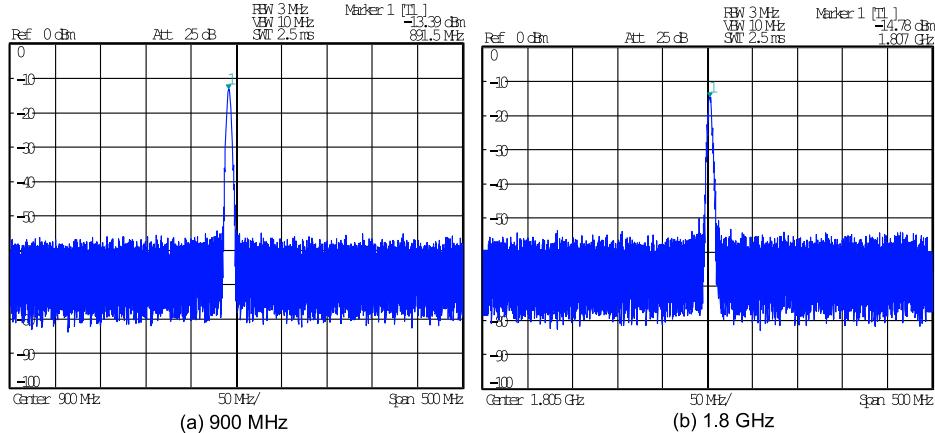


Fig. 16. Frequency spectra of the free-running oscillators at band edges of (a) 900 MHz and (b) 1.8 GHz. The tuning range is 900 MHz centered at 1.35 GHz (i.e., 66.7%).

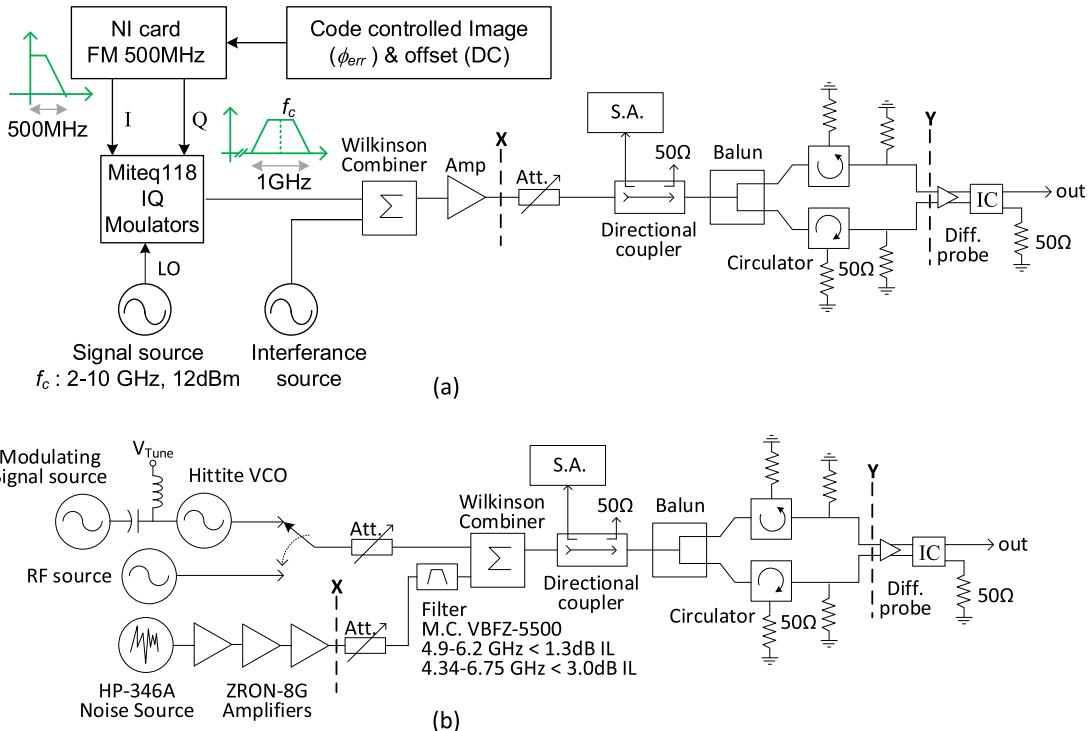


Fig. 17. Block diagrams of (a) wideband FM source setup and (b) setup for injection locking and noise analysis.

is 0.6 V, and f_0 is 1.5 GHz. The modulating signal is set to 2 MHz (limit of the wideband AWG) and a triangular waveshape is used to obtain a flat RF power spectrum. The demodulated output is a differential $1-V_{pp}$, 2-MHz triangular wave, with a second-harmonic suppression of ~ 24 dBc [see Fig. 22(a)]. The output spectrum for the low-band case of 2–3 GHz and $f_m = 1$ MHz is shown in Fig. 22(b). Note that the output power at frequencies lower than 10 MHz is attenuated by ac coupling at the spectrum analyzer input.

The bit-error rate (BER) of the demodulator is measured using 3.75–6.25 V pulses at a rate of 5 MHz from an HP-3762A data generator. The input stream (PRBS $2^{10} - 1$) consists of pseudorandom binary sequences of length equal to 1023 with one error bit per 1000 patterns. The data modulates a Hittite VCO (HMC586LC4B) to generate the

input FSK signal having a 1-GHz FM bandwidth around a 5-GHz carrier. Fig. 23(a) and (b) shows the BER versus the input voltage and input power (delivered to $1\text{ k}\Omega$), respectively, measured using an HP-3763A error detector. A back-to-back connection of the data generator and error detector yields a BER of 9.8×10^{-7} . During measurement, the oscillator's f_0 was maintained at 1.25 GHz and V_{CM} was kept equal to 0.62 V. The BER degrades rapidly with decreasing input power since the locking range of oscillator shrinks for diminishing inputs (Fig. 21). The BER measured for a 100-mV_{pp} input signal is 6.8×10^{-6} , and it drops to 1×10^{-3} for a 45-mV_{pp} input.

Fig. 24 shows the noise spectrum at plane 'X' on Fig. 17(b). The filtered noise is colored (not white or a flat spectral density). Similar to the measurements in Fig. 21, the curves marked 'free running' in Fig. 25 show the oscillator's locking profile when the noise source is disabled. Each point in Fig. 25

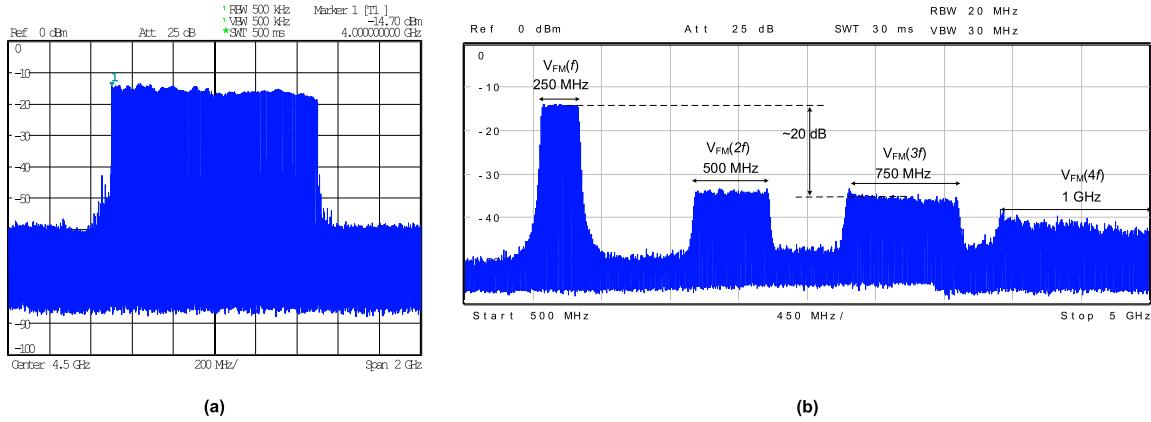


Fig. 18. Division of FM deviation. (a) 4–5-GHz bandwidth input FM. (b) Input bandwidth is divided down by a factor of 4 (1.00–1.25 GHz).

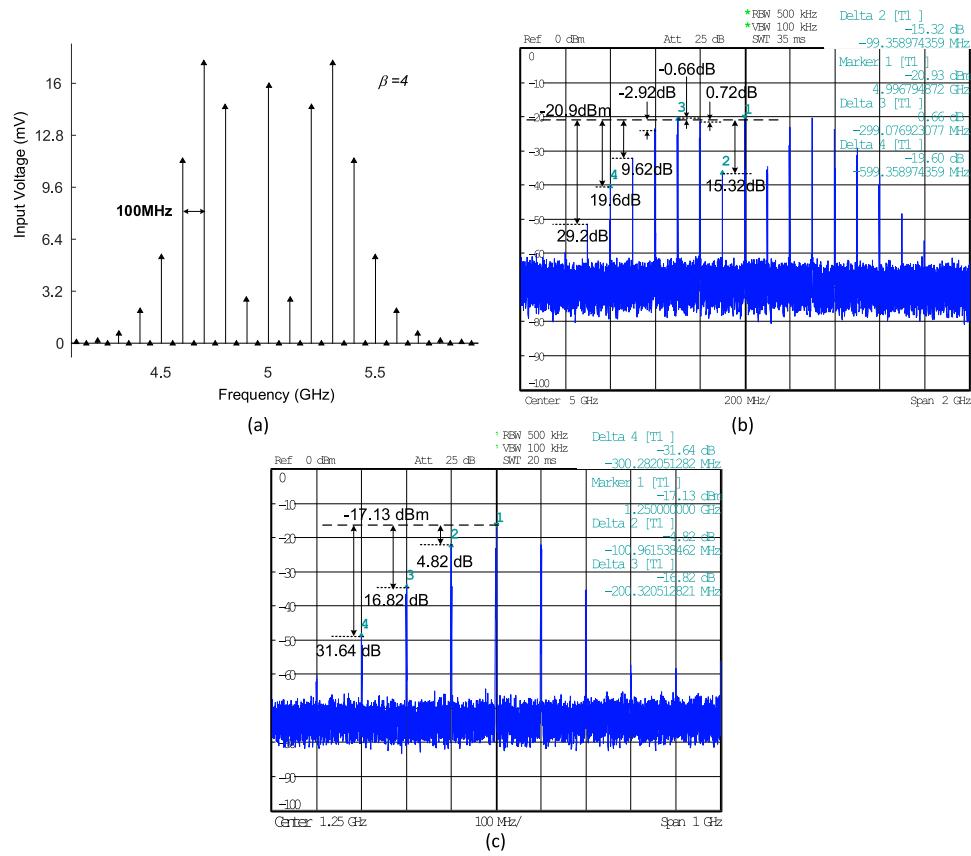


Fig. 19. Measured verification of theory and simulation predicting scaling of modulation index. Spectra of the (a) input signal used for simulation in Fig. 5, $f_c = 5$ GHz, $f_m = 100$ MHz, and $\beta = 4$, (b) FM signal of (a) generated and applied to the prototype oscillator, and (c) BFC scaling at the divided fundamental output having $\beta = 1$, which confirms the theory.

is an average of five readings. The three measurement sets show a maximum spread of ~ 7 mV (at 5.2 GHz) and an average spread of ~ 2.5 mV. Sensitivity of the demodulator is limited by the oscillator's locking behavior in the presence of noise, which is analyzed via measurement. Noise is typically a small-signal process compared with the signal for $\text{BER} < 10^{-3}$, and locking is a large-signal process. The evaluation of sensitivity limits requires comparable signal and noise levels (i.e., $\text{SNR} \approx 1$). Large-signal noise alters the properties of the free-running oscillator and its locking

sensitivity. Our experimental study of the oscillator's response to varying noise levels using the test setup of Fig. 17(b) (4 f_0 set midband to 5.5 GHz and $V_{CM} = 0.6$ V) reveals three distinct modes of operation.

In the first mode, the oscillator is driven by extremely low noise levels (i.e., high SNR). The interconnect losses are compensated using an ZRON-8G amplifier and trimmed to within 1 dB using attenuators. The integrated noise power (4.33–6.75 GHz) applied at the probe head is measured using the HP-E4419A power meter and is equal to -79.4 dBm.

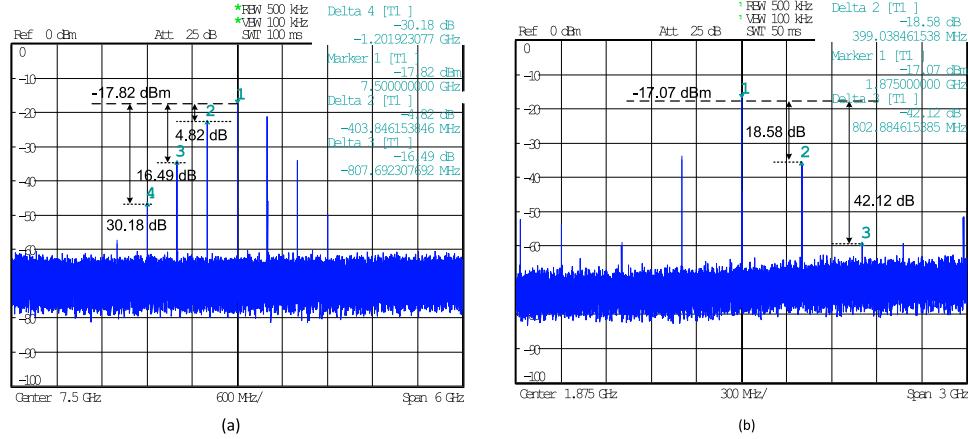


Fig. 20. Measured verification of division of modulation index for higher modulation rate. (a) Wideband FM input, $f_c = 5$ GHz, $f_m = 400$ MHz, and $\beta = 1$. (b) BFC scaling at the divided fundamental output having $\beta = 0.25$.

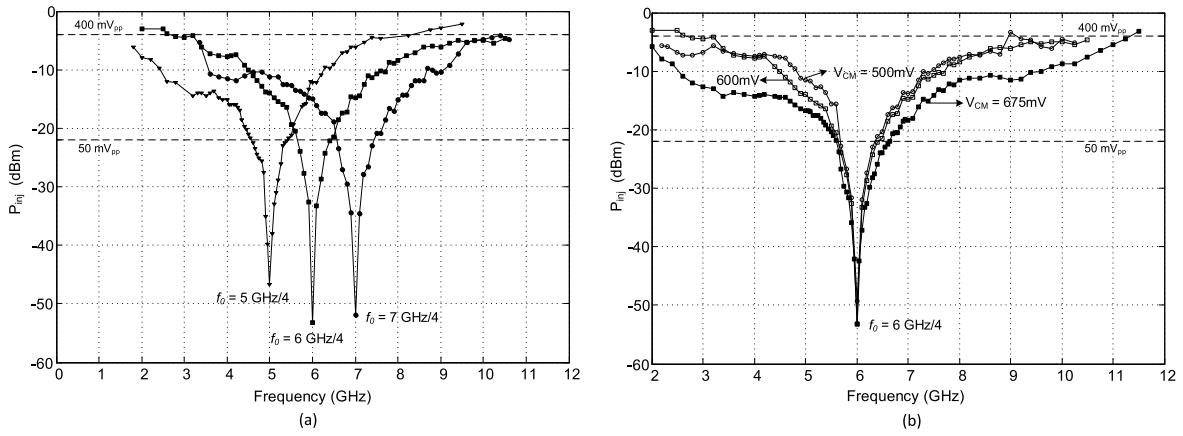


Fig. 21. (a) Free-running injection-locking profiles measured with the oscillator reset to f_0 each time. (b) Effect of V_{CM} on locking sensitivity and range.

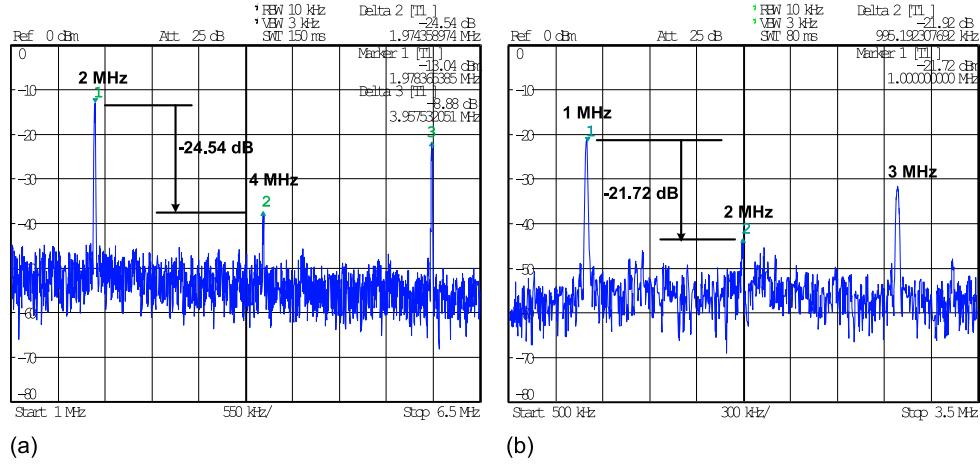


Fig. 22. Demodulated output spectra. (a) 4–5-GHz input modulated by a 2-MHz triangular signal. (b) 2–3-GHz input with 1-MHz modulation.

The noise induces a small shift in the frequency of oscillation (kilohertz range) along with a phase noise degradation of less than 0.6 dB. The observed frequency shift to a lower value agrees with theoretical predictions of an oscillator's response to white and colored noise [28]–[30]. In this mode, the locking sensitivity in the presence of noise does not vary discernibly in comparison with the free-running profile since the SNR

remains high. For -79.4 dBm noise, when the oscillator locks, the SNR is ~ 60 dB at the band edges and ~ 40 dB at $4f_0$ (see Fig. 25).

In the second mode, increased input noise continues to shift the oscillation frequency to a lower value. A measured example is shown in Fig. 25, where the black curve labeled 'a' represents the oscillator's locking profile in

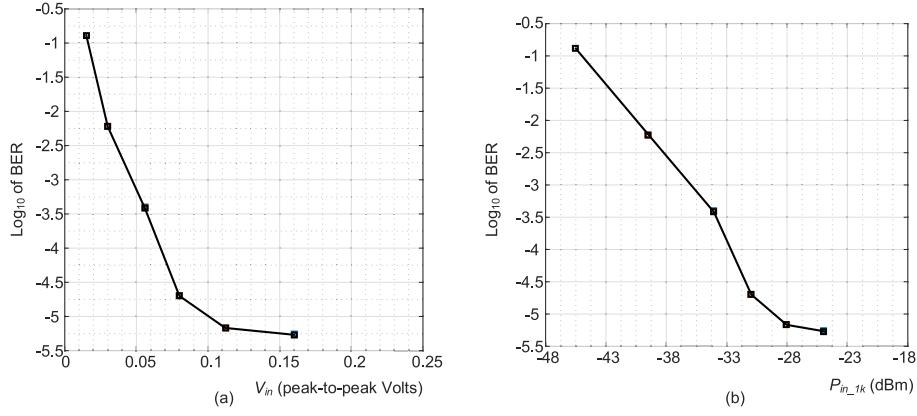


Fig. 23. Measured BER for the demodulator at a 10-Mb/s data rate versus (a) input amplitude and (b) power delivered to a 1-k Ω IF impedance.

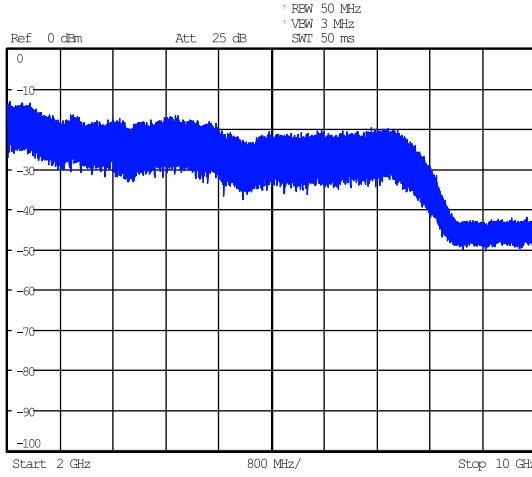


Fig. 24. Spectrum of the amplified noise-source captured with a 50-MHz resolution bandwidth at the reference plane ‘X’ in Fig. 17(b), showing the variation from an ideal white-noise source (noise coloring).

the presence of -40.3 dBm of integrated noise. A phase noise degradation of 9 dB and a noise-induced free-running frequency shift of ~ 6 MHz (24 MHz at $4f_0$) are observed at the output. As a result, the frequency for maximum sensitivity changes compared with the free-running case. The sensitivity change is more visible on the amplitude scale of the inset of Fig. 25. The measurements show that the oscillator is capable of locking to negative SNR values (between 5.49 and 5.56 GHz) in the vicinity of its newly established f_0 , as seen from Fig. 25. The ability to lock to negative SNR values over a narrow frequency range is characteristic of this mode.

In the third mode, the excess noise destabilizes the oscillator’s exciting chaotic behavior. The red curve labeled ‘c’ in Fig. 25 shows the locking profile in this mode when the noise power equals -23.57 dBm. The oscillator can still be locked to an input signal, although at an increased input drive (approximately -15 dBm). The absence of a stable oscillating frequency is reflected in the flat locking profile along with the inability to lock to negative SNR inputs compared with mode-2. A transitional state between modes-2 and 3 is captured by the blue curve labeled ‘b,’ when the oscillator is driven with -29.58 -dBm of integrated noise. The oscillator shows a weak preference for a single frequency compared with mode-1.

The free-running oscillator’s static locking profile (Fig. 21) does not accurately predict its response to a wideband signal. Fig. 26(a) shows the locking profile obtained from single-tone tests when the oscillator’s f_0 is 5.55 GHz/4. Appended to the static profile is the minimum detectable wideband signal level P_{mds} for which the oscillator locks to a 4.8–6.3-GHz wideband FM signal having $f_c = 5.55$ GHz, $f_m = 250$ MHz, and $\beta = 1$. The power of the wideband signal required for locking is less than what is predicted at the band edges of the free-running locking profile and similar for a 10- and 250-MHz modulation rate. The Bessel function transformation at the output characterizes FM-signal transmission through the locked-in ring, as shown in Section II-B. This is used to identify the minimum detectable signal, P_{mds} , which is measured at reference plane ‘Y’ on Fig. 17(b).

The input signal [P_{mds} at plane ‘Y’ in Fig. 17(b)] having $\beta = 1$ and $f_m = 250$ MHz is shown in Fig. 27(a). The integrated noise levels indicated in Fig. 26(b) are then applied to the input. The integrated noise of -23.57 dBm results in complete loss of lock and the output is shown in Fig. 27(b). The oscillator begins to partially lock to the input signal at 6-dB SNR for a -31.7 -dBm integrated noise input. This is evident from Fig. 27(c), where the sideband attenuation corresponds to a modulation index lower than the expected 0.25. A drop in power of the FM sideband spectral tones is indicative that the oscillator has not locked over the entire bandwidth. At an 8-dB SNR, the oscillator locks to the entire bandwidth, as seen from Fig. 27(d), with BFCs aligning with those for $\beta = 0.25$. Under the assumption that the oscillator tracks the same FM deviation at the same input drive levels, the SNR sensitivity for a 250-MHz signal can be expected to approximate that of a 500-Mb/s signal. With the knowledge that an 8-dB SNR input can be demodulated successfully and the locking amplitude is independent of the modulation rate for $f_c/f_m > 10$ [as seen from Fig. 26(a)], referencing P_{mds} of -25.75 dBm (32.62 mV_{pp}) against the FSK detection curve of Fig. 23(a) gives an approximate of BER of $10^{-2.25}$ (5.62×10^{-3}). Coherent detection of a binary FSK signal with $\beta = 1$ has a probability of error P_b , which is given by [31]:

$$P_b = \frac{1}{2} \operatorname{erfc} \left(\frac{\operatorname{SNR}}{2} \right)^{0.5} = 6 \times 10^{-3}. \quad (12)$$

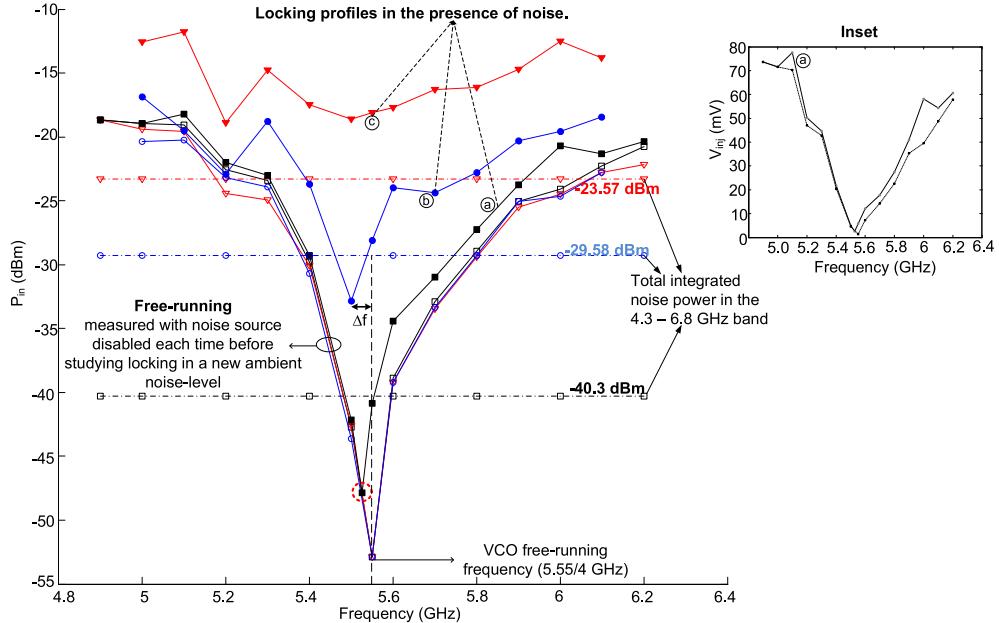


Fig. 25. Locking profile measured before and after applying different levels of integrated noise power to the locking signal. The oscillator's f_0 is tuned to the midband frequency of 5.55 GHz/4. Inset: the free-running profile and curve 'a' are shown in millivolt scale.

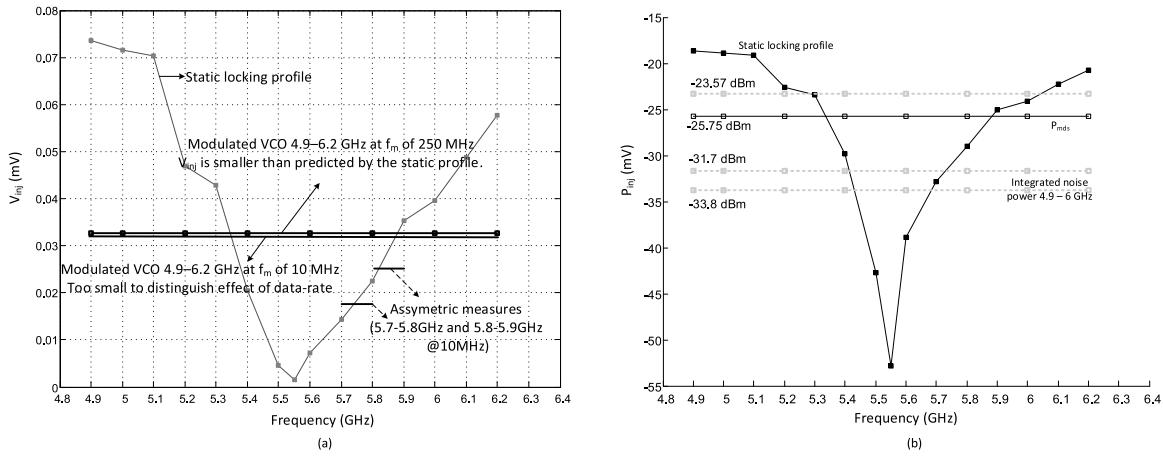


Fig. 26. (a) Locking sensitivity to modulated signals (horizontal lines) differs from the static locking profile. (b) Static locking profile and minimum input power level (P_{mds}) for locking to $f_c = 5.55$ GHz $f_m = 250$ MHz, and $\beta = 1$. The integrated noise levels applied for test are also shown.

For the same SNR, the estimate for BER of a high-data-rate binary FSK signal using the results in Figs. 23(a), 26(b), and 27(d) show less than 6.5% deviation from the theoretical estimate for a coherent FSK detector.

During the course of measurements shown in Figs. 25–27, it was observed that the oscillator consistently returns to its original free-running frequency and phase noise performance upon withdrawal of the external noise and signal stimuli.

Interference in millimeter-wave links is typically negligible. High antenna directivity enables line-of-sight wireless links, and attenuation due to path-loss reduces any potential interference. The response of the demodulator to in-band and out-of-band interferences is studied using the setup shown in Fig. 17(a). The oscillator is tuned to its lower band edge of 900 MHz. In the presence of a wideband input from 2 to 3 GHz, the power of the interference signal (out of band

at 1.95 GHz, i.e., 50-MHz spacing from the band edge and in band at $f_c = 2.5$ GHz) is ramped up and sequentially ramped down. Spectrum captures of the wideband input and interference tones [at reference plane 'X' in Fig. 17(a)] are shown in Fig. 28(a) and (b). As the power of the out-of-band interference surpasses the power of the FM spectral tones (by ~ 5.4 dB), it scrambles the demodulator output, which causes a rapid increase in harmonic content and beat notes. The observations from the experiment are illustrated in Fig. 28(c). During the ramp's descent, the interferer threshold for restoration of normal operation (noted as P_{th_d}) drops compared with the value in ascent (noted as P_{th_a}). Three important characteristics of the lock-in oscillator's response to interference are observed.

- 1) The time-based dependence of the response on its previous state reiterates the hysteresis accompanying injection locking that differentiates the oscillator's response to

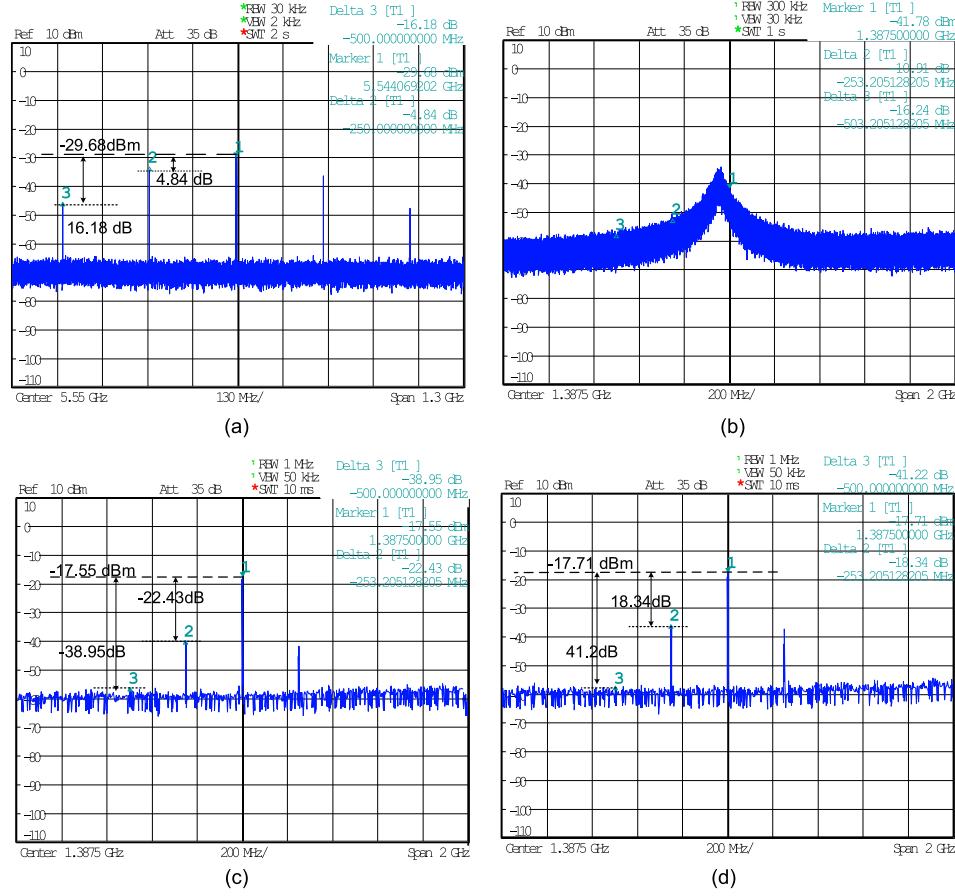


Fig. 27. Spectra of the locked-in oscillator for varying levels of SNR for a 5.55-GHz input ($f_{\text{osc}} = 1.3875$ GHz). (a) Input signal spectrum ($\beta = 1$ and $f_m = 250$ MHz). The output spectra for integrated noise levels of Fig. 26(b) at (b) SNR = -2.18 dB, (c) SNR = $+5.95$ dB, and (d) SNR = $+8.05$ dB.

TABLE III
PERFORMANCE SUMMARY OF RECENTLY PUBLISHED IF DEMODULATORS

[Ref.]	Tech.	V_{DD} (V)	Mod.	BW (Δf) (GHz)	$\Delta f/f_c$	Data Rate (Mb/s)	Q_{point} $P_{\text{diss.}}$ (mW)	Energy per bit (nJ)	P_{in} at 10^{-3} BER (dBm)	Output Power (dBm)
[15]	0.18um CMOS	1.8	GFSK	0.44-0.54	0.2	1	3.6*	3.6	n/a**	n/a
[32]	0.13um CMOS	1.2	FM/FSK	19.2-21.8	0.08	1500	7.2*	0.005	-16	+1
[33]	0.13um SiGe	2.7	FSK	8-10	0.22	2000	32.4 ^x	0.016	n/a	+1
[34]	0.18um CMOS	1.8	GFSK	.015-.025	0.50	1	12.6 ^x	12.6	n/a**	-13
This work	65nm CMOS	1.2	FM/FSK	2 – 10	1.34	10 800 ⁺	3.2	0.32	-36	+10 [•]

*Demod. core power (no IF or baseband amplifier)
**Rail-to-rail input drive
^xIncludes IF Limiter but not baseband amplifier
[•]Stand-alone oscillator characterization for high-data rate inputs
^{*} Q -point power dissipation does not include power for delivering 10dBm into the 50 Ohm load

static frequencies and modulation over the same frequency band [Fig. 26(a)].

- 2) A thresholding effect is observed. The performance of the demodulator degrades rapidly beyond a certain interference level.
- 3) A similar behavior is observed for in-band and out-of-band interferences. The difference observed in this experiment is a \sim 6-dB lower interference tolerance level

($P_{\text{th_}a}$) and a \sim 5-dB separation between $P_{\text{th_}a}$ and $P_{\text{th_}d}$ for the in-band interferer.

Table III summarizes the performance of IF demodulators based on delay lines [15], injection locking [32], and phase-shift networks [33], [34]. The IF demodulator developed in this paper achieves excellent low-power wideband performance. The quadrature VCO based design in [32] has a comparable data rate capability. However, the narrowband phase

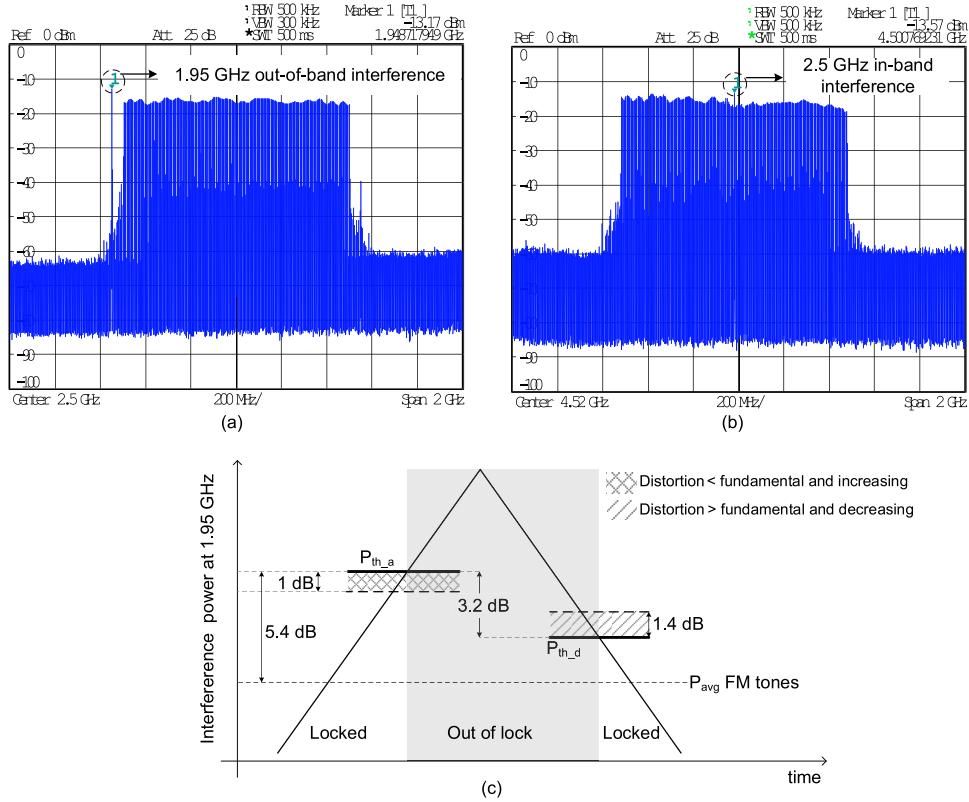


Fig. 28. Interference tests for a 2–3 GHz FM input having (a) out-of-band interference at 1.95 GHz and (b) in-band interference at 2.5 GHz. (c) Impact of interference levels on the demodulator and hysteresis.

linearity of the *LC* tank load and the limited locking range restrict its wideband performance ($\Delta f/f_c = 0.08$). The 7-mW power dissipation accounts only for the demodulator core. The $0.13\text{-}\mu\text{m}$ SiGe demodulator in [33] employs an *LC* phase-shift filter ($\Delta f/f_c = 0.22$), which limits wideband operation. In addition, as is the case with the *LC* delay in [15], the variation in magnitude response around the resonant frequency produces baseband distortion and limits sensitivity at wide offsets from the carrier. Large-signal drive and high mixer gain in [33] raises the power consumption to 34 mW. The active Bessel-filters-based quadrature discriminator in [34] shows wideband performance in the megahertz range ($\Delta f/f_c = 0.5$). However, the need for high-order filters increases power consumption (12.6 mW), while g_m/C bandwidth restricts efficient detection to lower data rates (~ 1 Mb/s). The quadrature-phased division of FM deviation demonstrated in this paper reinforces the factors that underpin efficient demodulation, namely, reduction of the signal bandwidth (via reformation of β), provision of wideband quadrature phases at no additional power expense, and large-signal drive delivered by the regenerative oscillator gain. When operating across 2–10 GHz ($\Delta f/f_c = 1.34$), the entire demodulator dissipates just 3.2 mW from 1.2 V. The IF preamplifier required to drive the demodulator can be optimized for nonlinear gain for a high-IF impedance using a ~ 17 -mW distributed amplifier (extrapolated for a 30-dB gain for $200\ \Omega$ from the results of the 90-nm prototype in [35]) or a ~ 12 -mW shunt-peaking driver [36] simulated in the 65-nm CMOS for a 35-dB gain from 2 to 10 GHz.

V. CONCLUSION

An FM demodulator is presented in which a four-stage ring oscillator locks to a wideband input and divides the FM deviation by four. Phase correlation of the locked-in oscillator's quadrature outputs allows simplified low-power demodulation, with a linear characteristic at baseband for a fractional bandwidth greater than one. Additional benefits of the injection locked demodulator are data-rate-independent power consumption, insensitivity to noise and AM interference, a requirement for low distortion is not imposed on the IF amplifier, and the operation of the oscillator at one-fourth of the intermediate frequency enables a higher IF and a lower fractional bandwidth.

The propagation of an FM signal through an injection-locked oscillator is analyzed in depth. The division of frequency deviation and scaling of BFCs derived analytically are verified via simulation and measured for a 65-nm prototype demodulator. Through simulation and analysis, low-power circuits developed in the work are evaluated, namely, a ring oscillator with wideband sensitivity, a folded CMOS mixer with *Q*-point control, and a three-stage differential Class-AB amplifier. The prototype IC is characterized extensively using a wide range of test-benches to study division of FM deviation, wideband demodulation, noise sensitivity, and BERs. Stand-alone characterization of the input oscillator showing its response to external noise and high modulation rate (up to 400 MHz) FM signals is presented, along with stand-alone characterization of the output Class-AB amplifier. The demodulator operation is measured over 2–10 GHz

$(\Delta f/f_c = 1.34)$. The energy consumption is just 0.32 nJ/b with an SNR sensitivity of 8 dB, and a 0.1% BER at 10 Mb/s observed for a 45-mV_{pp} input IF signal.

REFERENCES

- [1] E. McCune, "Foundations of Green communications," in *Proc. IEEE Commun. Workshop ICCW*, Jun. 2015, pp. 2744–2749.
- [2] A. Natarajan *et al.*, "A fully-integrated 16-element phased-array receiver in SiGe BiCMOS for 60-GHz communications," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 1059–1075, May 2011.
- [3] N. Saputra and J. R. Long, "A fully integrated wideband FM transceiver for low data rate autonomous systems," *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1165–1175, May 2015.
- [4] A. Visweswaran, J. R. Long, L. Galatro, M. Spirito, and R. B. Staszewski, "An FM demodulator operating across 2–10GHz IF," in *Proc. Radio Freq. Integr. Circuits Symp.*, Jun. 2013, pp. 213–216.
- [5] A. Visweswaran, J. R. Long, and R. B. Staszewski, "A 1.2V 110-MHz-UGB differential class-AB amplifier in 65nm CMOS," in *Proc. Custom Integr. Circuits Conf. (CICC)*, Sep. 2014, pp. 1–4.
- [6] A. Mirzaei, M. E. Heidari, R. Bagheri, and A. A. Abidi, "Multi-phase injection widens lock range of ring-oscillator-based frequency dividers," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 656–671, Mar. 2008.
- [7] A. Visweswaran, R. B. Staszewski, and J. R. Long, "A low phase noise oscillator principled on transformer-coupled hard limiting," *IEEE J. Solid-State Circuits*, vol. 49, no. 2, pp. 373–383, Feb. 2014.
- [8] S. D. Toso, A. Bevilacqua, M. Tiebout, N. D. Dalt, A. Gerosa, and A. Neviani, "A 0.06 mm² 11 mW local oscillator for the GSM standard in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 7, pp. 1295–1304, Jul. 2010.
- [9] A. Visweswaran, R. B. Staszewski, J. R. Long, and A. Akhnoukh, "Fine frequency tuning using injection-control in a 1.2V 65nm CMOS quadrature oscillator," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2012, pp. 293–296.
- [10] G. L. Beers, "A frequency-dividing locked-in oscillator frequency-modulation receiver," *Proc. IRE*, vol. 32, no. 12, pp. 730–737, Dec. 1944.
- [11] K. K. Clarke and D. T. Hess, *Communication Circuits: Analysis and Design (Chapters 11 and 12)*. Reading, MA, USA: Addison-Wesley, 1971.
- [12] E. Cambi, *Eleven and Fifteen-Place Tables of Bessel Functions of the First Kind, to All Significant Orders*. New York, NY, USA: Dover, 1948.
- [13] H. Darabi, S. Khoram, B. Ibrahim, M. Rofougaran, and A. Rofougaran, "An IF FSK demodulator for Bluetooth in 0.35 μm CMOS," in *Proc. Custom Integr. Circuits Conf. (CICC)*, May 2001, pp. 523–526.
- [14] H.-S. Kao, M.-J. Yang, and T.-C. Lee, "A delay-line-based GFSK demodulator for low-IF receivers," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2007, pp. 88–89.
- [15] J. Bae, K. Song, H. Lee, H. Cho, L. Yan, and H.-J. Yoo, "A 0.24 nJ/b wireless body-area-network transceiver with scalable double-FSK modulation," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2011, pp. 34–35.
- [16] D. E. Foster and S. W. Seeley, "Automatic tuning, simplified circuits, and design practice," *Proc. Inst. Radio Eng.*, vol. 25, no. 3, pp. 289–313, Mar. 1937.
- [17] N. Rajesh and S. Pavan, "Design of lumped-component programmable delay elements for ultra-wideband beamforming," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1800–1814, Aug. 2014.
- [18] S. Garakoui, E. A. M. Klumperink, B. Nauta, and F. F. E. Van Vliet, "A 1-to-2.5GHz phased-array IC based on gm-RC all-pass time-delay cells," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2012, pp. 80–82.
- [19] S. M. Kashmiri, S. A. P. Haddad, and W. A. Serdijn, "High-performance analog delays: Surpassing Bessel-Thomson by Padé-approximated Gaussians," in *Proc. Int. Symp. Circuits Syst.*, May 2006, pp. 2349–2352.
- [20] A. Bilotti, "Applications of a monolithic analog multiplier," *IEEE J. Solid-State Circuits*, vol. 3, no. 4, pp. 373–380, Dec. 1968.
- [21] B. Razavi, *RF Microelectronics*. Englewood Cliffs, NJ, USA: Prentice-Hall, 1998.
- [22] D. M. Monticelli, "A quad CMOS single-supply op amp with rail-to-rail output swing," *IEEE J. Solid-State Circuits*, vol. 21, no. 6, pp. 1026–1034, Dec. 1986.
- [23] V. Dhanasekaran, J. Silva-Martinez, and E. Sanchez-Sinencio, "Design of three-stage class-AB 16 Ω headphone driver capable of handling wide range of load capacitance," *IEEE J. Solid-State Circuits*, vol. 44, no. 6, pp. 1734–1744, Jun. 2009.
- [24] R. van Dongen and V. Rikkink, "A 1.5 V class AB CMOS buffer amplifier for driving low-resistance loads," *IEEE J. Solid-State Circuits*, vol. 30, no. 12, pp. 1333–1338, Dec. 1995.
- [25] K. Bult and G. J. G. M. Geelen, "A fast-settling CMOS op amp for SC circuits with 90-dB DC gain," *IEEE J. Solid-State Circuits*, vol. 25, no. 6, pp. 1379–1384, Dec. 1990.
- [26] M. Loikkanen and J. Kostamovaara, "Low voltage CMOS power amplifier with rail-to-rail input and output," *Anal. Integr. Circuits Signal Process.*, vol. 46, no. 3, pp. 183–192, Mar. 2006.
- [27] D. M. Pozar, *Microwave Engineering*, 2nd ed. New York, NY, USA: Wiley, 1998.
- [28] P. Maffezzoni, "Frequency-shift induced by colored noise in nonlinear oscillators," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 54, no. 10, pp. 887–891, Oct. 2007.
- [29] M. Bonnin and F. Corinto, "Phase noise and noise induced frequency shift in stochastic nonlinear oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 8, pp. 2104–2115, Aug. 2013.
- [30] R. F. Galán, "Analytical calculation of the frequency shift in phase oscillators driven by colored noise: Implications for electrical engineering and neuroscience," *Phys. Rev. E*, vol. 80, p. 036113, Sep. 2009.
- [31] J. F. M. Gerrits, M. H. L. Kouwenhoven, P. R. van der Meer, J. R. Farserotu, and J. R. Long, "Principles and limitations of ultra-wideband FM communications systems," *EURASIP J. Appl. Signal Process.*, vol. 3, pp. 382–396, Mar. 2005.
- [32] S.-H. Wen, C.-S. Wang, and C.-K. Wang, "A low power 20 GHz 1.5 Gb/s CMOS injection-pulling FSK modulator and frequency discriminator for 60GHz links," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2008, pp. 483–486.
- [33] A. Valdes-Garcia, S. Reynolds, and T. Beukema, "Multi-mode modulator and frequency demodulator circuits for Gb/s data rate 60 GHz wireless transceivers," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2007, pp. 639–642.
- [34] B. Chi, J. Yao, P. Chiang, and Z. Wang, "A 0.18-μm CMOS GFSK analog front end using a bessel-based quadrature discriminator with on-chip automatic tuning," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 11, pp. 2498–2510, Nov. 2009.
- [35] F. Zhang, A. Jha, R. Gharpurey, and P. Kinget, "An agile, ultra-wideband pulse radio transceiver with discrete-time wideband-IF," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1336–1351, May 2005.
- [36] J. Savoj and B. Razavi, "A 10-Gb/s CMOS clock and data recovery circuit with a half-rate binary phase/frequency detector," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 13–21, Jan. 2003.



Akshay Visweswaran (S'11–M'16) received the B.E. degree in electrical engineering from Sathyabama University, Chennai, India, in 2006, and the M.Sc. degree in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 2009, where he is currently pursuing the Ph.D. degree with the Electronics Research Laboratory. He was an Analog/RF designer at Conexant systems, Hyderabad, India, from 2006 to 2007, and with the IC-Laboratory at NXP Semiconductors, Eindhoven, The Netherlands, from 2009 to 2010.

He joined IMEC, Leuven, Belgium, as a Senior Researcher in 2015. His current research interests include RF/analog circuit design for integrated mm-wave wireless transceivers.



John R. Long (M'83–SM'14–F'15) received the B.Sc. degree in electrical engineering from the University of Calgary, Calgary, Alberta, in 1984, and the M.Eng. and Ph.D. degrees in electronics from Carleton University, Ottawa, ON, Canada, in 1992 and 1996, respectively.

He was with the Advanced Technology Laboratory at Bell-Northern Research, Ottawa, for 12 years, and began his Academic Career at the University of Toronto, Toronto, ON, from 1996 to 2002. From 2002 to 2014, he was the Chair of the Electronics Research Laboratory at the Delft University of Technology, Delft, The Netherlands, and joined the Faculty of Electrical and Computer Engineering, University of Waterloo, Waterloo, ON, in 2015. His current research interests include low-power and broadband circuits for highly-integrated wireless transceivers, energy-efficient wireless sensors, and mm-wave and high-speed data communication IC design.