A 28-GHz SiGe BiCMOS PA With 32% Efficiency and 23-dBm Output Power

Anirban Sarkar, *Member, IEEE*, Farshid Aryanfar, *Senior Member, IEEE*, and Brian A. Floyd, *Senior Member, IEEE*

***Abstract*— In this paper, we present a two-stage, four-way combined power amplifier (PA) operating in the 27–31-GHz frequency range in 180-nm SiGe BiCMOS technology. The output network of the PA employs spiral transformers and a microstrip T-combiner to realize low-loss two-way series, two-way parallel power combining. With the help of a lumped-element transformer model, we present a co-optimization technique for the transformer and the adjoining matching components to minimize the power loss of the full output network. The design methodology is applicable for realizing an arbitrary impedance at the device plane with a K-way series, M-way parallel combiner. The efficacy of this technique is demonstrated by the realization of a PA, which has 27.6-dB gain, 23.2-dBm, 1-dB compressed output power, 32.7% power-added efficiency (PAE) at 1-dB compression, and 15% PAE at 6-dB back off. Linearity measurements show less than 4° amplitude-modulation to phase-modulation distortion below 3-dB back off and less than −32-dBc intermodulation product at 6-dB back off.**

***Index Terms*— 28 GHz, fifth generation (5G), power amplifier (PA), power combining, SiGe, transformer.**

I. Introduction

THE fifth-generation (5G) cellular systems at millimeter-wave frequency bands can enable gigabit-per-second wireless links. Phased-array transmitters for the 5G mobile uplink need high output power and high-efficiency power amplifiers (PAs) to reduce size and power consumption. Based on the link budget presented in [1], we target an effective isotropic radiated power (EIRP) of 30 dBm. This EIRP can be achieved using a four-element array with 1-dBi unit antenna gain and 17-dBm output power per element. Assuming 6-dB output back off ($P_{-6\,dB}$) for an orthogonal frequency division multiplex scheme, we target a 1-dB compressed output power ($oP_{1\,dB}$) of 23 dBm and a power-added efficiency (PAE) of 15% at $P_{-6\,dB}$ to limit the power consumption of the four-element array to 1.35 W.

Single-transistor and cascode PAs in SiGe and CMOS technologies have demonstrated 15–18 dBm $oP_{1\,dB}$ with 30%–40% peak PAE at 28 GHz [2]–[4]. To increase output power, larger devices could be used, but the higher impedance transformation ratio and increased parasitics reduce both gain and bandwidth of the PA. Device stacking can be used to achieve a higher voltage swing and output power at the cost of reduced gain and linearity [5]. Alternatively, transformer-based series–parallel combined PAs can achieve higher output power while maintaining the same linearity as the unit PAs driving the transformer [5].

In this paper, we present a methodology to co-optimize an output transformer and adjoining matching elements to minimize the insertion loss of a two-way series, two-way parallel (S2P2) structure. This is in contrast to the existing design methodologies for series–parallel power combiners [5]–[8] where optimization of the transformer has been the focus. Inclusion of a matching network in this methodology also enables the possibility of realizing a broader range of impedance at the device plane compared with the existing work. The efficacy of this method is demonstrated through the realization of an S2P2 PA in SiGe with 23-dBm $oP_{1\,dB}$ and 32% PAE.

II. Output Combining and Matching Network Optimization

Prior work on transformer-based series–parallel power combined PAs [5]–[8] has emphasized the selection of optimum number of series and parallel stages and the selection of optimum transformer dimensions [5]. Chowdhury *et al.* [9] have demonstrated that the loss of the transformer could be minimized versus diameter for a fixed trace width; however, if we optimize the transformer with the sole objective of minimizing its power loss, the impedance presented by the combiner to the device may be suboptimal for PAE. In this case, the loss incurred due to additional matching elements between the combiner and the unit PAs could become significant. In this paper, we present a methodology to co-optimize the transformer with adjoining matching elements with the aid of a lumped-element transformer model in an S2P2 power combiner [Fig. 1(a)] to minimize the loss of the full network while providing the optimum impedance (Z_{opt}) to the devices for maximum PAE. Our goal is to express the loss of the full network, i.e., the transformer and matching elements, as a function of the transformer diameter.

To design and co-optimize the combiner and the matching network, we use the conceptual schematic shown in Fig. 1(b). The impedance transformation trajectory from R_{LT} to Z_{opt} is determined using Fig. 2, where $R_{LT} = R_L M/K$ is the

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A. Sarkar was with the Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC 27695 USA. He is now with Samsung Semiconductor, Inc., San Jose, CA 95134 USA.

F. Aryanfar was with Samsung Research America, Dallas, TX 75082 USA. He is now with Straight Path Communications, Inc., Dallas, TX 75075 USA.

B. A. Floyd is with the Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC 27695 USA.

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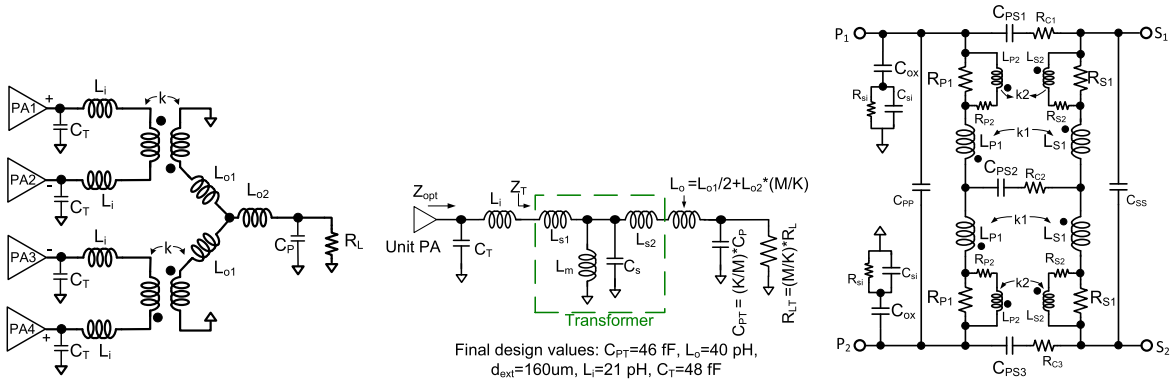
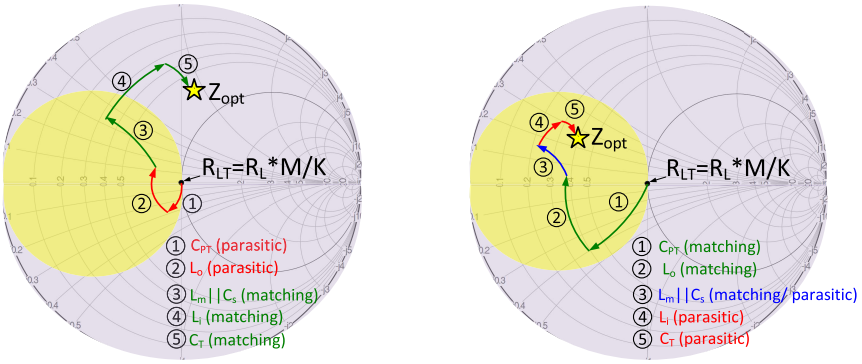


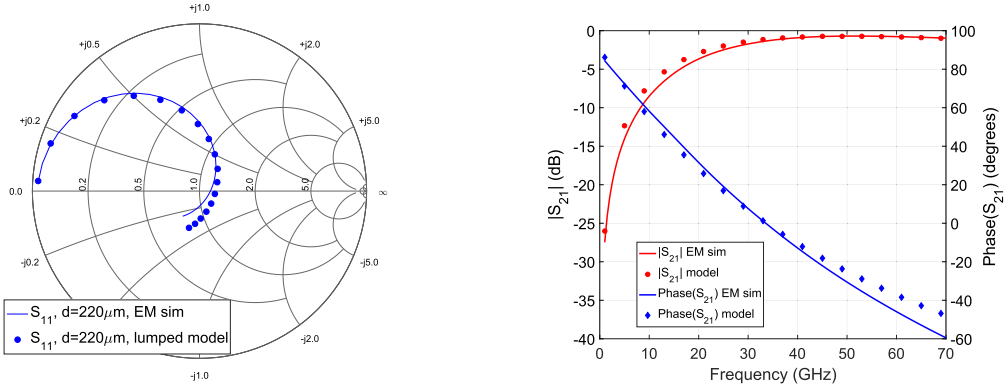
(a) (b) (c)

Fig. 1. (a) Lumped-element representation of output combiner, matching components, and parasitic components. (b) Equivalent network for a single PA. (c) Lumped-element model of transformer.



(a) (b)

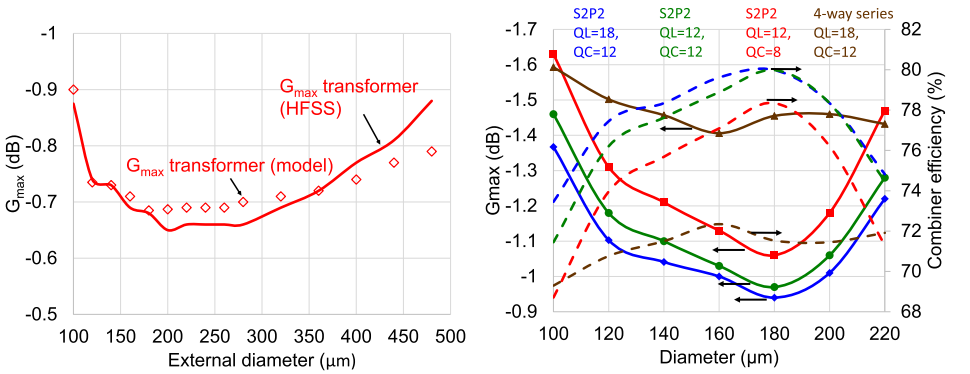
Fig. 2. Illustration of the impedance transformation network, matching, and parasitic elements based on the location of optimum impedance Z_{opt} for (a) Z_{opt} outside the conductance circle $G = 1/R_{\text{LT}}$ and (b) Z_{opt} inside the conductance circle $G = 1/R_{\text{LT}}$. Smith chart is normalized to R_{LT}.



(a) (b)

Fig. 3. Comparison of two-port S-parameters of transformers obtained using the lumped model and HFSS simulations. (a) S_{11} on smith chart. (b) S_{21} magnitude/phase.

transformed load resistance for a unit PA in a K-way series, M-way parallel combiner. For cases where Z_{opt} is outside the conductance circle $G = 1/R_{\text{LT}}$ [Fig. 2(a)], L_m, L_i, and C_T are used for impedance transformation, whereas the rest of the components are fixed. For cases where Z_{opt} is inside this circle [Fig. 2(b)], L_o, C_{PT}, and L_m are used for impedance transformation, and other components are fixed. To meet our $oP_{1\,\text{dB}}$ target of 23 dBm, we prefer a two-way series, two-way parallel ($K = 2$, $M = 2$) power combiner over a four-way series combiner ($K = 4$, $M = 1$), since it gives a higher transformed load resistance R_{LT}. As Fig. 2(a) indicates, higher R_{LT} decreases the impedance transformation ratio between R_{LT} and Z_{opt}, which further reduces the size and insertion loss of the matching network.



d_{ext} (um)	Z_T (Ω)	L_i (pH) (QL=18)	C_T (fF) (QC=12)
100	3.88+j*13.68	22.6	204.9
120	6.6+j*18	19.6	140.3
140	10.41+j*22.1	17.7	91.1
160	16.1+j*25.19	21.3	48.5
180	22.54+j*27.22	23	18.2
200*	27.42+j*24.64	41.8	0.5
220*	26.59+j*21.11	61.6	2.6

(a) (b) (c)

Fig. 4. (a) $G_{\max}$ of the transformer from the lumped model and EM simulations. (b) $G_{\max}$ of the full combiner network using lumped model for different Q-factors. (c) Value of matching elements L_i and C_T for different diameters calculated using (3)–(7).

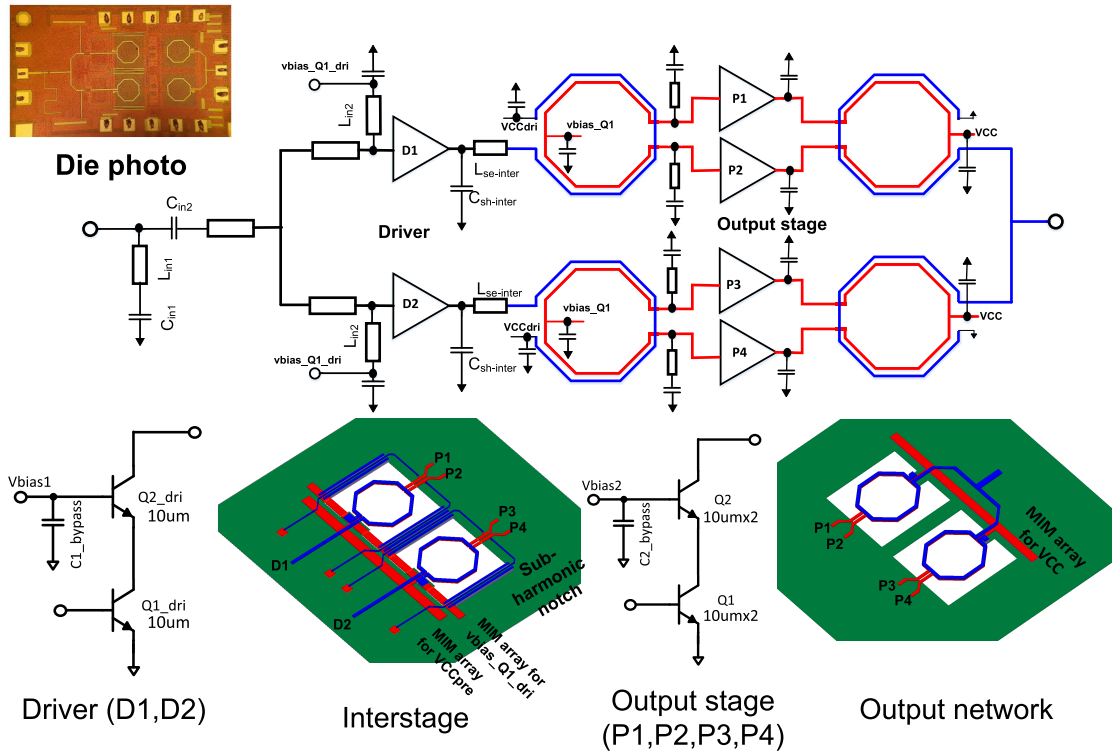
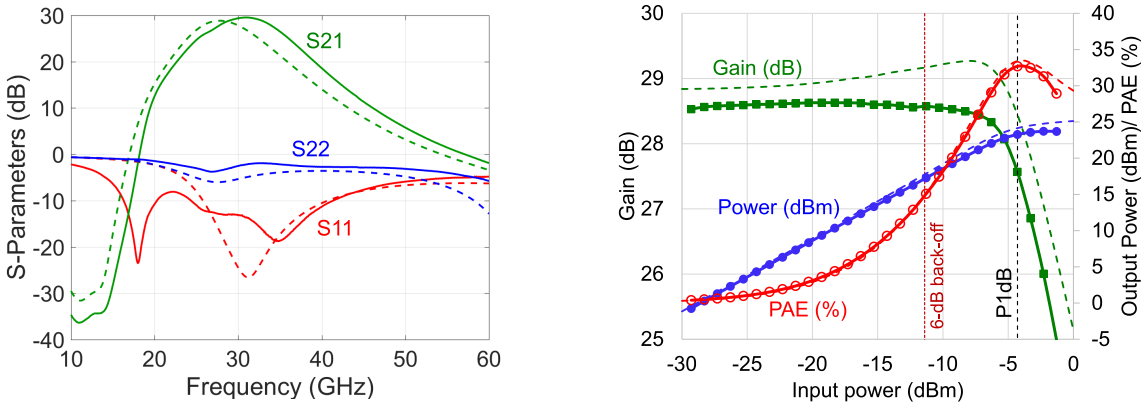


Fig. 5. Schematic and die photograph of two-stage 28-GHz PA.

To relate the matching network to the transformer geometry, we first assume that the impedance looking into the transformer (Z_T) can be expressed as a function of the transformer's external diameter (d_{ext}) for a fixed trace width of the transformer and for fixed parasitic components L_o and C_{PT}. For a desired Z_{opt}, using standard two-element matching theory, the matching components can be calculated as in (1) and (2), as shown at the bottom of next page for lossless passives, where $R_{\text{optP}}||X_{\text{optP}}$ is the parallel equivalent of Z_{opt}. Since the elements Z_T, C_T, and L_i are the functions of d_{ext}, the maximum gain $G_{\max}$ of the network in Fig. 1(b) can also be expressed as a function of d_{ext}. With finite Q, the matching values are modified as shown in the Appendix.

In this paper, Z_T and $G_{\max}$ of a two-way series, two-way parallel combiner have been calculated as a function of d_{ext} using a lumped-element model of the transformer, as shown in Fig. 1(c) and equations for lossy matching components L_i and C_T. The lumped model used for the transformer is based on the model presented in [9]. Most of the parameters of the model, including the primary inductors (L_{P1} and L_{S1}), the parasitic capacitors, and the resistors, have been calculated using analytical equations presented in [9] and [10]. The coupling coefficients ($k1$ and $k2$), the inductors representing frequency dependence of loss (L_{P2} and L_{S2}), and the substrate resistance R_{si} have been fit to electromagnetic (EM) simulations. A plot showing agreement between the lumped-element



(a) (b)

Fig. 6. (a) S-parameter measurements and (b) swept-power measurements at 28 GHz (simulation results shown with dotted lines).

model and the EM simulation across frequency for $d = 220$ μm is shown in Fig. 3. Additional plots showing agreement of the model with HFSS for other diameters can be found in [11].

Fig. 4(a) shows $G_{\max}$ of the transformer obtained from the lumped model as well as from 3-D EM simulation of the transformer using HFSS [12] for 28 GHz, illustrating an optimization, which focused only on transformer dimension. Fig. 4(b) then compares $G_{\max}$ and efficiency of the full combiner plus matching network for three sets of Q-factors with typical values of inductor and capacitor Q-factors in this technology being 18 and 12 at 28 GHz. We observe that the full network has about 0.2–0.5-dB extra insertion loss compared with the transformer alone. Furthermore, loss of the transformer is almost constant for d_{ext} ranging from 160 to 260 μm, whereas the loss of the combiner with adjoining matching networks quickly increases as we deviate from the optimum d_{ext} of 180 μm. The peak drain efficiency is impacted by 3%–4% points for d_{ext} ranging from 100 to 220 μm. For comparison, $G_{\max}$ of a four-way series combiner network computed using the same methodology has also been included in Fig. 4(b) for the case of inductor and capacitor Q-factors of 18 and 12, indicating that it has a higher loss compared with the S2P2 combiner as predicted earlier.

Top level metals M6 and M5 with the thicknesses of 2.81 and 1.59 μm are used for the transformer windings. To reduce power loss, the transformer is implemented over the substrate with no ground plane underneath; however, the transformer is surrounded by M2 ground planes to avoid unexpected coupling with adjacent structures and between the two transformer windings. For parallel combining, we prefer microstrip line rather than coplanar stripline due to well-controlled mode, and consequently the characteristic impedance of the microstrip line and ease of connecting to a single-ended ground-signal-ground output. Finally, to provide a good ac bypass at the center taps, an array of metal–insulator–metal (MIM) capacitors is used, as shown in Fig. 5.

TABLE I
PERFORMANCE OF THE 28-GHz PA ACROSS BAND

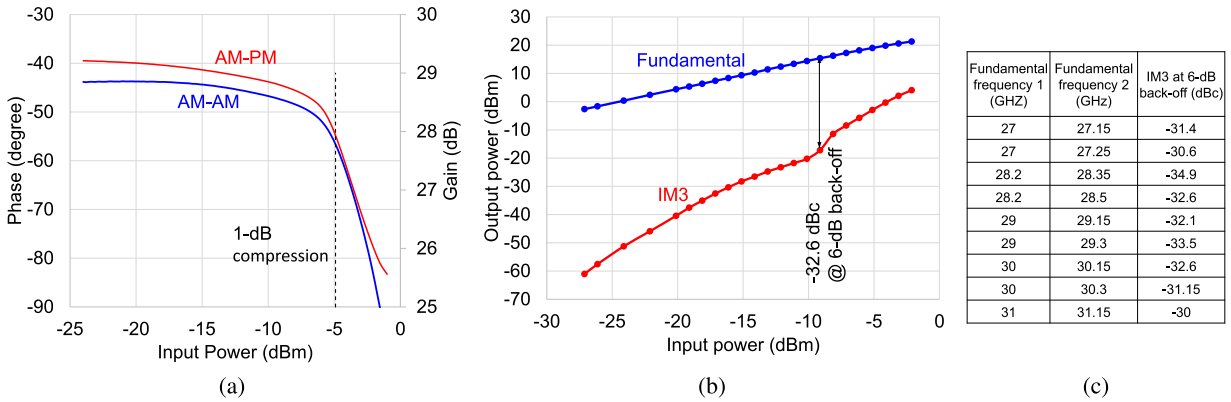
Frequency (GHz)	27	28	29	30	31
Gain (dB)	27.2	28.6	28.6	28.7	29.9
P_{sat} (dBm)	23.6	23.7	23.3	23.8	22.9
oP_{1dB} (dBm)	23.3	23.2	22.7	22.6	22.2
Peak PAE (%)	30.3	32.7	30.6	30.8	33
PAE 1-dB comp. (%)	29.9	32.7	29.8	29.5	32.4
PAE 6-dB-back-off (%)	13.7	15	13.8	13.4	13.8

III. PA DESIGN

The two-stage PA schematic is shown in Fig. 5. The PA is designed in TowerJazz 180-nm SiGe BiCMOS technology, which includes high-performance n-p-n transistors with an $f_T/f_{\max}$ of 200/260 GHz, a BV_{CEO} of 1.6 V, and a BV_{CBO} of 5.5 V. The output stage PAs are cascode amplifiers chosen because of the higher allowed voltage swing across the common base (CB) device, higher gain, and better reverse isolation. Both devices of the cascode amplifier use a dual-emitter, triple-base, and dual-collector structure for reduced base resistance and compact layout. The devices have 10-μm-long emitter with two fingers to deliver about 18-dBm $oP_{1\,\text{dB}}$ and are biased with a current density of 0.625 mA/μm. The adjacent deep trench regions of multiple

$$L_i = \frac{1}{\omega}\left(\sqrt{R_{\text{optP}}\,\mathbb{R}\text{e}[Z_T(d_{\text{ext}})] - (\mathbb{R}\text{e}[Z_T(d_{\text{ext}})])^2} - \mathbb{I}\text{m}[Z_T(d_{\text{ext}})]\right) \tag{1}$$

$$C_T = \frac{1}{\omega}\frac{\left(\sqrt{R_{\text{optP}}\,\mathbb{R}\text{e}[Z_T(d_{\text{ext}})] - (\mathbb{R}\text{e}[Z_T(d_{\text{ext}})])^2}\right) X_{\text{optP}} - \mathbb{R}\text{e}[Z_T(d_{\text{ext}})]R_{\text{optP}}}{\mathbb{R}\text{e}[Z_T(d_{\text{ext}})]R_{\text{optP}}X_{\text{optP}}} \tag{2}$$



Fundamental frequency 1 (GHZ)	Fundamental frequency 2 (GHz)	IM3 at 6-dB back-off (dBc)
27	27.15	-31.4
27	27.25	-30.6
28.2	28.35	-34.9
28.2	28.5	-32.6
29	29.15	-32.1
29	29.3	-33.5
30	30.15	-32.6
30	30.3	-31.15
31	31.15	-30

(a) (b) (c)

Fig. 7. Linearity measurements of the PA. (a) AM-PM distortion at 28 GHz. (b) IM3 with tones at 28.2 and 28.5 GHz. (c) IM3 product versus frequency.

TABLE II
PERFORMANCE COMPARISON WITH Ka AND Q-BAND PAs

Reference	Frequency (GHz)	Architecture	Gain (dB)	P_{sat} (dBm)	oP_{1dB} (dBm)	Peak PAE (%)	PAE at P_{1dB} (%)	PAE at 6-dB-back-off(%)	Technology
This work	28	Two stage, 4-way power combined	28.6	23.7	23.2	32.7	32.7	15	180-nm SiGe
[13] Helmi *et. el.*	28/46	Three/Two Triple-Stacked	17.3/17.4	24.6/22.4	23/19	15/42.5	12.5/22.5*	5/7.5*	45-nm SOI CMOS
[14] Welp *et. el.*	24	1-stage differential	18.5	24.7	23.7	31	27	7*	350-nm SiGe
[15] Mortazavi *et. el.*	28	Two stage, Class-F	21.2	17.1	15	42	38	18.5*	130-nm SiGe
[16] Jayamon *et. el.*	29	Multigate-cell	13	24.5	21	29	26	8*	45-nm SOI CMOS
[17] Shakib *et. el.*	30	Two-stage, transformer combined	15.7	14	13.2	35.3	34.3	16*	28-nm CMOS
[18] Essing *et. el.*	27	8-way parallel combined	20.7	31	N.A	13	N.A.	N.A.	250-nm SiGe
[19] Pei *et. el.*	30	2-stage Class-A	27	15	14*	8.5	N.A.	N.A.	250-nm SiGe
[20] Datta *et. el.*	39-47	Stacked Class-E	14	23.4	N.A	34.9	N.A.	N.A.	130-nm SiGe
[21] Park *et. el.*	28	1-stage, double stack class-AB	13.6	19.8	18.6	43.3	41.4	20*	28-nm CMOS
[22] Hu *et. el.*	28/37/39	2-stage Doherty	13	17.1	15.5	23	23	12*	130-nm SiGe

* Estimated from swept-power plots

fingers are merged to further reduce parasitic interconnects. The technology supports MIM capacitors at lower metal levels (M3 and M4), which enables us to realize a high quality bypass capacitor at the base terminal of the CB device. The common emitter and CB devices are biased using two separate but identical current mirrors. Load-pull simulations indicate that the cascode amplifier can achieve 18-dBm $oP_{1\,dB}$ with a 37% maximum peak PAE for $Z_{opt} = 28 + j32\ \Omega$ (excluding the device capacitance). A cascode driver stage is added to improve the gain of the PA. The device sizes, collector voltage, and bias current density are scaled down compared with the output stage to conserve dc power. A single-finger device with 10-μm-long emitter biased at a current density of 0.375 mA/μm and a collector voltage of 2.8 V is used for the driver stage to deliver 10-dBm $oP_{1\,dB}$ and 11-dB gain. To evaluate linearity of the PA chain versus driver stage current density, two-tone simulations were performed, indicating that the third-order intermodulation (IM3) distortion product does not degrade as long as the gain expansion of the chain is limited to 0.5 dB or the current density of the driver stage is above 0.3 mA/μm.

We design the interstage network to provide out-of-phase inputs to the balanced driver PA pair as well as to transform $Z_{in-driver}$ to $Z_{opt-pre}$. $Z_{in-driver}$ is the impedance looking into the driver stage and $Z_{opt-pre}$ is the optimum impedance at the pre-driver output for maximum PAE. The interstage matching network consists of a transformer balun, a series line $L_{se-inter}$, and a shunt MIM capacitor $C_{sh-inter}$, as shown in Fig. 5. Since $Z_{opt-pre}$ is outside the conductance circle G=Re$[1/Z_{in-driver}]$, the impedance transformation trajectory is similar to the one shown in Fig. 2(a), and the same optimization procedure presented in Section II is applied. Transient simulation of the PA revealed the generation of small subharmonic parametric oscillations at 3-dB back off and higher power levels. To suppress this oscillation, subharmonic notches are included in the interstage and input networks. The interstage notch is implemented with a series tank consisting of a 2.5-μm-thick, 480-μm-long line and a 196-fF MIM capacitor. To make the layout compact, the line is meandered around the transformer on both sides and over the ground planes, as shown in Fig. 5. The input network consists of a shunt microstrip line (L_{in2}) at the input of the driver amplifiers,

$$aX_{\mathrm{Li}}^2 + bX_{\mathrm{Li}} + c = 0 \tag{3}$$

$$X_{\mathrm{CT}} = \frac{\left(\left(\mathbb{R}\mathrm{e}[Z_T] + \frac{X_{\mathrm{Li}}}{Q_{\mathrm{Li}}}\right)^2 + (\mathbb{I}\mathrm{m}[Z_T] + X_{\mathrm{Li}})^2\right) X_{\mathrm{optP}}}{X_{\mathrm{optP}}\,(\mathbb{I}\mathrm{m}[Z_T] + X_{Li}) - \left(\left(\mathbb{R}\mathrm{e}[Z_T] + \frac{X_{\mathrm{Li}}}{Q_{\mathrm{Li}}}\right)^2 + (\mathbb{I}\mathrm{m}[Z_T] + X_{\mathrm{Li}})^2\right)} \tag{4}$$

$$a = \left(\frac{1}{Q_{\mathrm{Li}}^2} + 1\right)(Q_{\mathrm{CT}} X_{\mathrm{optP}} + R_{\mathrm{optP}}) \tag{5}$$

$$b = \left(\frac{2\,\mathbb{R}\mathrm{e}[Z_T]}{Q_{\mathrm{Li}}} + 2\,\mathbb{I}\mathrm{m}[Z_T]\right)(Q_{\mathrm{CT}} X_{\mathrm{optP}} + R_{\mathrm{optP}}) - X_{\mathrm{optP}} R_{\mathrm{optP}} \left(\frac{Q_{\mathrm{CT}}}{Q_{\mathrm{Li}}} + 1\right) \tag{6}$$

$$c = |Z_T|^2 (Q_{\mathrm{CT}} X_{\mathrm{optP}} + R_{\mathrm{optP}}) - X_{\mathrm{optP}} R_{\mathrm{optP}}\,(Q_{\mathrm{CT}}\,\mathbb{R}\mathrm{e}[Z_T] + \mathbb{I}\mathrm{m}[Z_T]) \tag{7}$$

a parallel combiner, a series MIM capacitor (C_{in2}), and a sub-harmonic notch filter (L_{in1} and C_{in1}).

IV. Measurement Results

A die photo of the fabricated chip is shown in Fig. 5, and the chip measures 1.15 mm × 0.62 mm, excluding pads. All measurements were performed with 2.8-V driver collector voltage, 7.5-mA driver quiescent DC current, 3.8-V output stage collector voltage, and 50-mA output stage quiescent DC current. S-parameter measurement and simulation results are shown in Fig. 6(a). The PA achieves 30-dB peak gain at 31 GHz, better than 12-dB input return loss, and less than 3-dB gain variation across the 27–31 GHz frequency range. Small-signal stability of the PA in the frequency range 100 MHz–67 GHz is verified by the μ-factor, and large signal stability is evaluated using a spectrum analyzer, revealing stable operation. Swept-power results at 28 GHz are shown in Fig. 6(b). At 28 GHz, the PA has 23.7-dBm $\mathrm{P_{sat}}$, 23.2-dBm $\mathrm{oP_{1\,dB}}$, 32.7% PAE at 1-dB compression, and 15% PAE at $\mathrm{P_{1\,dB}}$. Swept-power performance in the 27–31-GHz frequency range is presented in Table I, and shows that the PA has only 1.2-dB variation in $\mathrm{oP_{1\,dB}}$ across 27–31 GHz. Linearity of the PA is assessed with amplitude-modulation to phase-modulation (AM-PM) distortion and two-tone measurements shown in Fig. 7. AM-PM measurements of the PA indicate that the PA has less than 4° distortion at 3-dB back off and lower power levels. Two-tone measurements show that the PA has less than −32.6-dBc IM3 product compared with the fundamental tone at $\mathrm{P_{-6\,dB}}$.

V. Conclusion

In this paper, we demonstrate a co-optimization technique for the transformer and the matching network in a two-way series, two-way parallel combiner using a lumped-element model for the transformer. $G_{\max}$ of the network is calculated as a function of the transformer diameter using this lumped model and equations for matching components, which enables us to choose the optimum diameter. Consideration of matching components in the combiner also makes the method more generalized. Application of this technique results in 5-dB boost in $\mathrm{oP_{1\,dB}}$ with only 4%–5% point degradation in PAE compared with a unit PA. Performance comparison with the state-of-the art PAs is shown in Table II. Compared with other PAs with $\mathrm{oP_{1\,dB}}$>20 dBm, our PA achieves better PAE at 1-dB compression and back off.

Appendix

For finite quality factors, matching elements L_i and C_T can be calculated for a given Z_T and Z_{opt} with the following modified equations (3)–(7), as shown at the top of this page, where X_{Li}, Q_{Li}, X_{CT}, and Q_{CT} are reactances and quality factors of L_i and C_T. These equations have been derived using the standard two-element matching theory. Note that these assume an approximate value for the quality factor of the components *a priori*, and these equations can be used iteratively to obtain more precise values.

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References

[1] F. Khan, Z. Pi, and S. Rajagopal, "Millimeter-wave mobile broadband with large scale spatial processing for 5G mobile communication," in *Proc. 50th Annual Allerton Conf. Commun., Control, Comput. (Allerton)*, Oct. 2012, pp. 1517–1523.

[2] A. Sarkar and B. Floyd, "A 28-GHz class-J power amplifier with 18-dBm output power and 35% peak PAE in 120-nm SiGe BiCMOS," in *Proc. IEEE 14th Topical Meeting Silicon Monolithic Integr. Circuits RF Syst. (SiRF)*, Jan. 2014, pp. 71–73.

[3] A. Sarkar, K. Greene, and B. Floyd, "A power-efficient 4-element beam-former in 120-nm SiGe BiCMOS for 28-GHz cellular communications," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting (BCTM)*, Sep. 2014, pp. 68–71.

[4] S. Mortazavi and K.-J. Koh, "A 38 GHz inverse class-F power amplifier with 38.5% peak PAE, 16.5 dB gain, and 50 mW Psat in 0.13-μm SiGe BiCMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, May 2015, pp. 211–214.

[5] D. Zhao and P. Reynaert, "An E-band power amplifier with broadband parallel-series power combiner in 40-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 683–690, Feb. 2015.

[6] K. H. An *et al.*, "Power-combining transformer techniques for fully-integrated CMOS power amplifiers," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1064–1075, May 2008.

[7] Q. Gu, Z. Xu, and M.-C. Chang, "Two-way current-combining *W*-band power amplifier in 65-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 5, pp. 1365–1374, May 2012.

[8] J. Oh, B. Ku, and S. Hong, "A 77-GHz CMOS power amplifier with a parallel power combiner based on transmission-line transformer," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 7, pp. 2662–2669, Jul. 2013.

[9] D. Chowdhury, P. Reynaert, and A. M. Niknejad, "Design considerations for 60 GHz transformer-coupled CMOS power amplifiers," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2733–2744, Oct. 2009.

[10] S. Voinigescu, "High frequency devices," in *High-Frequency Integrated Circuits*, 1st ed. New York, NY, USA: Cambridge Univ. Press, 2013, ch. 4, pp. 10–15.
[11] A. Sarkar, "Efficient power amplifiers for millimeter-wave beamformers," Ph.D. dissertation, Dept. Elect. Comput. Eng., North Carolina State Univ., Raleigh, NC, USA, Dec. 2016.
[12] Ansys HFSS, Canonsburg, PA, USA. (2015). [Online]. Available: https://www.ansys.com
[13] S. R. Helmi, J. H. Chen, and S. Mohammadi, "High-efficiency microwave and mm-wave stacked cell CMOS SOI power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 7, pp. 2025–2038, Jul. 2016.
[14] B. Welp, K. Noujeim, and N. Pohl, "A wideband 20 to 28 GHz signal generator MMIC with 30.8 dBm output power based on a power amplifier cell with 31% PAE in SiGe," *IEEE J. Solid-State Circuits*, vol. 51, no. 9, pp. 1975–1984, Sep. 2016.
[15] S. Y. Mortazavi and K.-J. Koh, "A 28-GHz inverse class-F power amplifier with coupled-inductor based harmonic impedance modulator," in *Proc. Custom Integr. Circuits Conf. (CICC)*, Sep. 2015, pp. 1–4.
[16] J. A. Jayamon, J. F. Buckwalter, and P. M. Asbeck, "28 GHz >250 mW CMOS power amplifier using multigate-cell design," in *Proc. IEEE Compound Semicond. Integr. Circuit Symp. (CSICS)*, Oct. 2015, pp. 1–4.
[17] S. Shakib, H. C. Park, J. Dunworth, V. Aparin, and K. Entesari, "A 28GHz efficient linear power amplifier for 5G phased arrays in 28nm bulk CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Paper*, Jan. 2016, pp. 352–353.
[18] J. Essing, D. Leenaerts, and R. Mahmoudi, "A 27GHz, 31dBm power amplifier in a 0.25 μ SiGe:C BiCMOS technology," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting (BCTM)*, Sep. 2014, pp. 143–146.
[19] Y. Pei, Y. Chen, D. M. W. Leenaerts, and A. H. M. van Roermund, "A 30/35 GHz dual-band transmitter for phased arrays in communication/radar applications," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1629–1644, Jul. 2015.
[20] K. Datta, J. Roderick, and H. Hashemi, "Analysis, design and implementation of mm-Wave SiGe stacked Class-E power amplifiers," in *Proc. Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2013, pp. 275–278.
[21] B. Park *et al.*, "Highly linear mm-wave CMOS power amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4535–4544, Dec. 2016.
[22] S. Hu, F. Wang, and H. Wang, "A 28GHz/37GHz/39GHz multiband linear Doherty power amplifier for 5G massive MIMO applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Paper*, Feb. 2017, pp. 32–33.

Anirban Sarkar (S'10–M'17) received the B.E. degree in electrical engineering from the National Institute of Technology at Durgapur, Durgapur, India, in 2006, and the M.S. and Ph.D. degrees in electrical engineering from North Carolina State University, Raleigh, NC, USA, in 2011 and 2016, respectively.

He was an Intern with Samsung Research America, Dallas, TX, USA, in 2015. He is currently a Senior Engineer with the Modem RFIC Group, Samsung Semiconductor, Inc., San Jose, CA, USA. His current research interests include RF and millimeter-wave integrated circuits, especially linear and power-efficient transmitters and power amplifiers.

He has served as a Reviewer of the IEEE JOURNAL OF SOLID STATE CIRCUITS.

Farshid Aryanfar (S'01–M'05–SM'06) received the M.Sc. degree from the University of Tehran, Tehran, Iran, in 1998, and the Ph.D. degree from the University of Michigan, Ann Arbor, MI, USA, in 2004.

He was with Motorola, Schaumburg, IL, USA, and Rambus, Sunnyvale, CA, USA, and was a Senior Director and the Head of the RF and Analog Laboratory, Samsung Research America, Dallas, TX, USA, where he led the implementation of Samsung 5G mobiles and base station radios incorporating wideband phased array. He is currently the Vice President of Technology with Straight Path Communications, Inc., Dallas, TX, USA, developing 39-GHz radio for 5G fixed and mobile broadband. He has authored over 50 papers and holds over 40 patents (20 issued).

Brian A. Floyd (S'98–M'01–SM'10) received the B.S. (Hons.), M. Eng., and Ph.D. degrees in electrical and computer engineering from the University of Florida, Gainesville, FL, USA, in 1996, 1998, and 2001, respectively.

He held the Intersil/Semiconductor Research Corporation Graduate Fellowship and the Pittman Fellowship at the University of Florida, where he was involved in the CMOS RFIC design for on-chip wireless clock distribution. In 2001, he became a Research Staff Member with the IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA, where he was involved in the development of 3G WCDMA receivers in SiGe BiCMOS and CMOS technologies and then the investigation and demonstration of some of the first silicon-based millimeter-wave receivers, transmitters, and frequency synthesizers for applications at 60 GHz and above. In 2007, he became the Manager of the Wireless Circuits and Systems Group, IBM Thomas J. Watson Research Center, where he was involved in leading the development of 60-GHz phased-array transceiver, antenna, and package solutions under the IBM and MediaTek joint development program. In 2010, he joined the Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC, USA, as an Associate Professor. He has authored or co-authored over 88 technical papers and has 24 issued patents. His current research interests include RF and millimeter-wave circuits and systems for communications, radar, and imaging applications.

Dr. Floyd received the 2016 NC State Outstanding Teacher Award, the 2015 NC State Chancellor's Innovation Award, the 2014 IBM Faculty Award, the 2011 DARPA Young Faculty Award, the 2004 and 2006 IEEE Lewis Winner Awards for best paper at the International Solid-State Circuits Conference, and the 2006 and 2011 Pat Goldberg Memorial Awards for the best paper within IBM Research. From 2006 to 2009, he served on the technical advisory board to the Semiconductor Research Corporation (SRC) integrated circuits and systems science area. He currently serves as a Thrust Leader of the SRC's Texas Analog Center of Excellence. He has served as an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and on the technical program committee for the IEEE International Solid-State Circuits Conference. He currently serves on the steering committee for the IEEE RFIC Symposium and on the technical program committees for both the IEEE RFIC Symposium and the IEEE Bipolar/BiCMOS Circuits and Technology Meeting.