

All-Digital LTE SAW-Less Transmitter With DSP-Based Programming of RX-Band Noise

Enrico Roverato[✉], Member, IEEE, Marko Kosunen, Member, IEEE, Koen Cornelissens, Sofia Vatti, Member, IEEE, Paul Styren, Kaoutar Bertrand, Teuvo Korhonen, Member, IEEE, Hans Samsom, Patrick Vandenameele, Member, IEEE, and Jussi Rynänen, Senior Member, IEEE

Abstract—We present the first all-digital LTE transmitter (TX) using programmable digital attenuation of receive band (RX-band) noise. The system is architected to fully exploit the speed and low cost of DSP logic in deep-submicrometer CMOS processes, without increasing at all the design effort of the RF circuitry. To achieve operation without surface acoustic wave filter, the TX uses digital bandpass delta-sigma modulation and mismatch-shaping to attenuate the DAC noise at a programmable duplex distance. These functions can be implemented entirely within DSP, thus taking advantage of the standard digital design methodology. Furthermore, the fully digital RX-band noise shaping significantly relaxes the performance requirements on the RF front-end. Therefore, 10 bits of resolution for the D/A conversion are sufficient to achieve -160 dBc/Hz out-of-band (OOB) noise, without need for digital predistortion, calibration, or bulky analog filters. The TX was fabricated in 28-nm CMOS, and occupies only 0.82 mm^2 . Besides low OOB noise, our system also demonstrates state-of-art linearity performance, with measured CIM3/CIM5 below -67 dBc, and adjacent-channel leakage ratio of -61 dBc with LTE20 carrier. The circuit consumes 150 mW from 0.9-/1.5-V supplies at +3 dBm output power.

Index Terms—All-digital transmitter (TX), delta-sigma, LTE, mismatch-shaping, receive band (RX-band) noise, RF-DAC.

I. INTRODUCTION

THE crowded radio spectrum allocated for 3G/4G mobile communication, together with the growing demand for higher data-rates, has led to the situation where RF transmitters (TXs) and receivers (RXs) need to support multiple frequency bands. This is especially challenging in frequency-division duplexing (FDD), where limited duplexer isolation can result in RX sensitivity degradation if an excess of transmit power leaks to the receive band (RX-band). Because different FDD bands also have different TX–RX duplex spacings, boosting the isolation through multiple external surface acoustic wave (SAW) filters leads to unacceptable cost penalty, and is

Manuscript received April 21, 2017; revised August 7, 2017 and October 3, 2017; accepted October 3, 2017. Date of publication November 8, 2017; date of current version November 21, 2017. This paper was approved by Guest Editor Alyosha Molnar. (*Corresponding author: Enrico Roverato.*)

E. Roverato, M. Kosunen, and J. Rynänen are with the Department of Electronics and Nanoengineering, Aalto University School of Electrical Engineering, 02150 Espoo, Finland (e-mail: enrico.roverato@aalto.fi).

K. Cornelissens, S. Vatti, P. Styren, K. Bertrand, H. Samsom, and P. Vandenameele are with Huawei Technologies, 3001 Leuven, Belgium.

T. Korhonen is with Huawei Technologies, 00180 Helsinki, Finland.

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2017.2761781

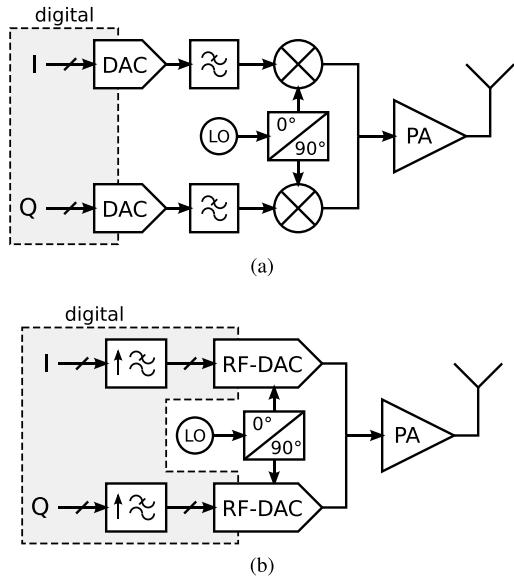


Fig. 1. Generic block diagram of (a) analog-intensive and (b) digital-intensive RF TX based on direct-conversion I/Q modulation.

usually avoided. Therefore, from the TX point of view, the only way to achieve SAW-less operation is to target strict out-of-band (OOB) emissions, typically around -160 dBc/Hz within the RX-band.

The advance of deep-submicrometer CMOS processes calls for digital-intensive TX architectures, in order to enable efficient integration with the application and digital baseband processors. However, low OOB noise is easier to achieve by utilizing extensive analog baseband filtering. For this reason, analog-intensive TX architectures [Fig. 1(a)] are still very popular and actively researched nowadays [1]–[6]. The main problem with these structures is that they do not significantly benefit from CMOS scaling, thus leading to large area consumption even in the most advanced process nodes. This becomes evident by analyzing the chip micrographs of the circuits published in [1] and [3]–[6], from where it can be noticed that the analog baseband section takes up to 50% of the total TX area.

On the other hand, digital-intensive TXs [Fig. 1(b)] do not use analog filtering after the D/A conversion, except for the weak attenuation provided by the RF matching network. Hence, two problems must be solved in order to enable low OOB emission levels. The first is the digital repetition

spectrum, attenuated only by the *sinc* response of the D/A converter's zero-order hold. This can be successfully handled by increasing the oversampling ratio (OSR) of the digital baseband signal, which is well supported by deep-submicrometer CMOS processes [7]–[15]. The second issue is the DAC quantization noise. Even with the increased OSR, quantization noise is a major obstacle for the successful implementation of all-digital SAW-less TXs. Therefore, recent research on the topic has focused extensively on this challenge, and several potential solutions have been proposed.

The most straightforward way to reduce the quantization noise is to increase the DAC resolution to 14 or 15 bits [9], [10]. However, the effective number of bits (ENOB) that can be achieved without digital predistortion (DPD) or calibration is typically around 10–12, which is not sufficient to meet the tight OOB emission requirements. Moreover, higher ENOB translates directly into increased DAC complexity, thus being controversial to the objectives of digital RF, i.e., simplification of the analog part and relaxation of its performance requirements. A more digital-like solution consists of connecting many DACs with different weights in a semi-digital finite impulse response (FIR) configuration, in order to reduce the quantization noise at a programmable offset from the TX band [11], [12]. This approach, which has been validated also for digital power amplifiers [13], [14], allows to relax the ENOB requirement for each converter. However, the design of this circuit is essentially analog and thus susceptible to device mismatches, even though the matching can be improved by using switched-capacitor converters [14]. Another recent innovation in the field of all-digital TXs is the resistive charge-based DAC [15]. The main idea is to use incremental signaling (rather than absolute) in order to provide intrinsic quantization noise attenuation. Even though the concept has shown the promise of low power consumption, the DAC still requires 12 bits for SAW-less operation. In the context of polar TXs, noise shaping has been explored in [16] to reduce the envelope quantization noise falling in the RX-band. However, the measured improvements are limited by other nonlinearities of the system, such as the asymmetry of rise/fall times in the Buck converter. More techniques to improve the amplitude resolution of all-digital polar TXs are presented in [17] and [18]. Although these methods try to exploit the benefits of nanoscale CMOS, they cannot be fully implemented within DSP, which would be attractive in terms of design portability and reusability.

In our recent work [19], we demonstrated for the first time that the RX-band noise of an all-digital TX based on direct-conversion I/Q modulation can be reduced by purely digital means. The proposed method exploits programmable bandpass $\Delta\Sigma$ modulation [20]–[25] and mismatch-shaping [26]–[35]. In addition to inheriting all the benefits of nanoscale CMOS, the purely digital implementation takes advantage of highly automated standard design methodologies, using hardware description languages (HDLs) that truly enable design reusability and portability to newer process technologies.

The first all-digital LTE TX implementing the aforementioned technique was presented in [36]. The circuit, fabricated in 28-nm CMOS with only 0.82-mm² active area, achieves

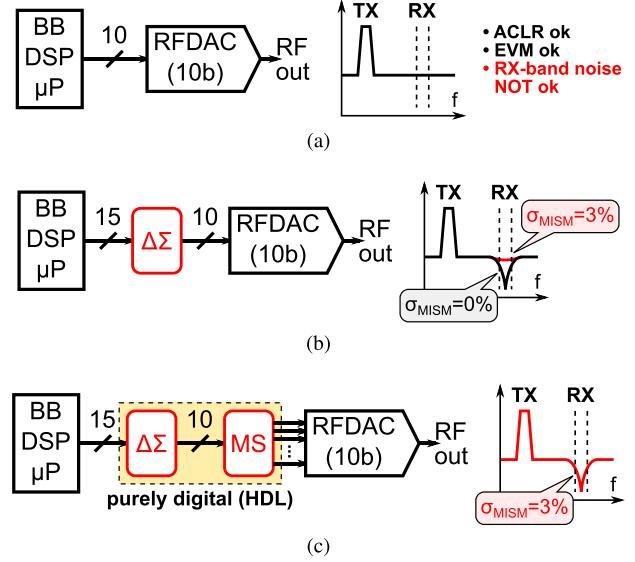


Fig. 2. Overview of the DSP-based technique used in this paper. (a) Linear quantization followed by a 10-bit RF-DAC. (b) Addition of a $\Delta\Sigma$ modulator to shape the quantization noise. (c) Addition of a mismatch-shaping encoder to shape the mismatch noise.

between -155 and -163 dBc/Hz noise at a programmable 30–400 MHz offset from the TX band, by using a conventional 10-bit current-steering DAC without DPD, calibration or analog filtering. The TX also shows excellent CIM3/CIM5 below -67 dBc, and adjacent-channel leakage ratio (ACLR) of -61 dBc with LTE20 carrier. This paper extends our previous publications [19], [36] by providing a more comprehensive description and analysis of the system, including the detailed implementation of the innovative DSP part of the TX, as well as new measured spectra for the OOB noise.

This paper is organized as follows. Section II introduces the DSP-based technique for RX-band noise attenuation used in the system. Section III discusses circuit-level design aspects, with special focus on the programmable bandpass $\Delta\Sigma$ modulator and mismatch-shaping encoder. Measurement results are presented and compared with system-level simulations in Section IV. Finally, Section V concludes this paper.

II. PROGRAMMABLE RX-BAND NOISE SHAPING

The DSP technique used in the system has been thoroughly discussed in [19]. This section only provides a qualitative overview. For further details, the reader is encouraged to consult [19], as well as the related literature on $\Delta\Sigma$ modulation [20]–[25] and mismatch-shaping [26]–[35].

Fig. 2(a) shows the simplified block diagram of an all-digital TX based on RF-DAC. Assuming a sufficiently large OSR (i.e., with sample rate in the order of hundreds of MHz), it turns out that 10 bits of resolution for the D/A conversion are more than adequate to meet the in-band and ACLR performance requirements for the user equipment of 3G/4G mobile radio standards (e.g., ACLR < -30 dBc, error-vector magnitude (EVM) $< 8\%$ for 64-QAM in LTE [37]), thus leaving a large margin for power amplifier nonlinearities. However, the TX fails at achieving low OOB emissions for

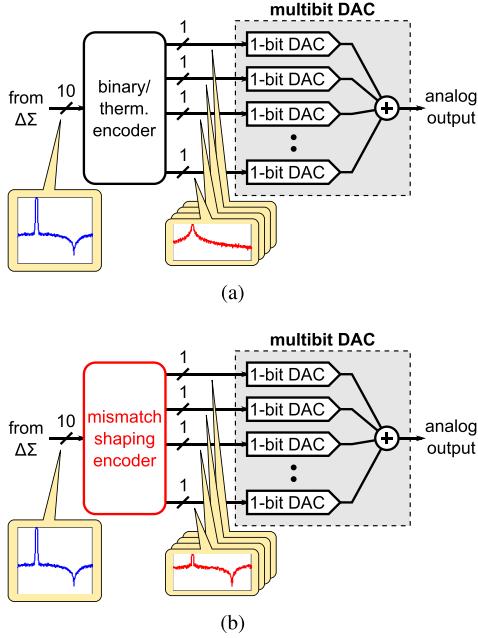


Fig. 3. Spectral densities of the input-output signals for (a) binary/thermometer encoder and (b) mismatch-shaping encoder.

SAW-less operation. As demonstrated in [7], ENOB up to 13 is needed to push the unfiltered quantization noise reaching the RF output below the typical limit of -160 dBc/Hz.

Because OOB emissions need to be particularly low only at duplex distance, the spectral density of the quantization noise can be shaped accordingly. This can be done by inserting a digital $\Delta\Sigma$ modulator [20]–[25] before the RF-DAC, as shown in Fig. 2(b). Since the RF-DAC resolution is still 10 bits, the noise transfer function (NTF) of the $\Delta\Sigma$ modulator can be properly designed as to provide a deep notch centered on the RX-band, while causing negligible noise amplification at other frequencies. Furthermore, by implementing a programmable NTF, the RX-band notch can be tuned to different TX–RX duplex spacings, thus enabling multiband support. The problem with this approach is that the performance of multibit $\Delta\Sigma$ modulation is limited by mismatch noise, caused by the inevitable static amplitude and timing mismatches between different conversion cells of the RF-DAC. This mismatch noise fills up the RX-band notch, and the practical performance that can be achieved is not sufficient for SAW-less operation.

Fortunately, mismatch noise can also be spectrally shaped in the digital domain, by employing a technique known as mismatch-shaping [26]–[35]. The operation principle can be intuitively explained as follows. In a typical binary/thermometer DAC segmentation, the 1-bit signals at the encoder output are strong nonlinear functions of the input, as shown in Fig. 3(a). In the presence of mismatches, these 1-bit signals leak to the analog output, thus causing the mismatch noise. Nevertheless, if the 1-bit signals could be shaped such that their spectral densities resemble that of the $\Delta\Sigma$ modulator output, then the mismatch noise would be also shaped, regardless of the mismatch statistics. This is possible by employing a mismatch-shaping encoder that implements

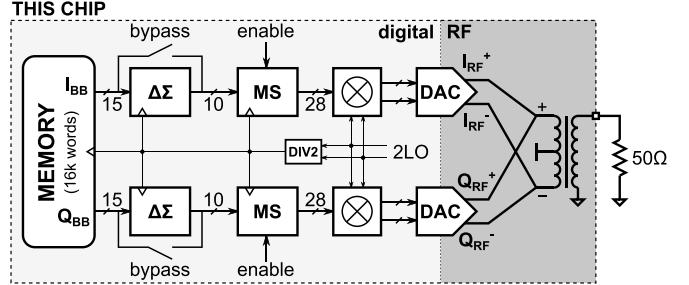


Fig. 4. System-level block diagram of the TX.

the same NTF used for the $\Delta\Sigma$ modulator, as shown in Fig. 3(b). Because the mismatch-shaping algorithm needs no knowledge of the actual mismatch profiles, which are random and unique for each chip sample, no DPD or calibration are required.

In conclusion, by combining the aforementioned techniques such as in Fig. 2(c), RX-band noise filtering can be accomplished in a fully digital fashion. The residual nonlinearity, caused by second-order effects, such as LO phase noise and memory in the RF-DAC, does not impair SAW-less operation. The added circuit blocks can be implemented in HDL and synthesized with a standard digital flow, thus taking advantage of nanoscale CMOS and maximizing design reusability. Even though both $\Delta\Sigma$ modulation and mismatch-shaping are well known and established techniques, the main novelty in this paper is to apply them to the RX-band, instead of the main signal band.

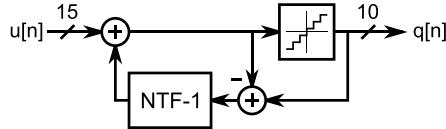
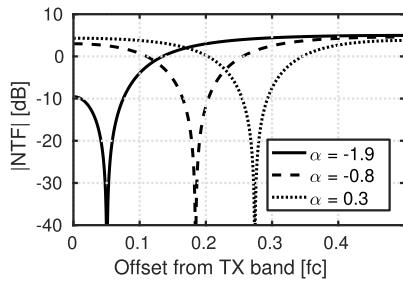
III. CIRCUIT IMPLEMENTATION

The system architecture of the implemented TX is shown in Fig. 4 [36]. The structure is based on direct-conversion I/Q modulation, but all signal processing is performed in the digital domain, preceding the DAC. All clocks in the system are derived from the 2LO signal, which is fed from an external source at twice the carrier frequency f_c . The sample rate for the digital baseband circuitry equals f_c , whereas the mixer also uses a clock at $2f_c$. The baseband I/Q data are generated offline and loaded into a 16k-word memory, from where they can be streamed to the rest of the TX chain. Even though ENOB of 13 is sufficient for OOB quantization noise below -160 dBc/Hz [7], the wordlength of I_{BB} and Q_{BB} at the memory output is 15 bits, in order to leave enough margin for roundoff errors in the DSP part. The outputs of I and Q paths are combined on-chip through an RF balun, designed to match 50Ω external load in the low-band (0.7–1.0 GHz) of the cellular radio spectrum.

In the remainder of this section, the circuit-level details of the key blocks are described.

A. Error-Feedback $\Delta\Sigma$ Modulator

As discussed in [19], one simple $\Delta\Sigma$ modulator architecture that suits the requirements of our system is the error-feedback (EF) structure of Fig. 5 [20]. This section will further show that a clever design of the loop filter in Fig. 5 achieves the

Fig. 5. EF $\Delta\Sigma$ modulator.Fig. 6. Programmable NTF realized by the $\Delta\Sigma$ and mismatch-shaping blocks. The magnitude responses are calculated from (2), with $r = 0.5$ and different values of α .

desired noise shaping performance with low implementation complexity.

1) Noise Transfer Function: For physical realizability, the NTF must be in the form

$$\text{NTF}(z) = \frac{1 + \sum_{i=1}^M b_i z^{-i}}{1 + \sum_{i=1}^M a_i z^{-i}} \quad (1)$$

where M is the modulator order and $\{b_i, a_i\}$ is the set of NTF coefficients [20]. Previous literature on bandpass $\Delta\Sigma$ modulation relies for example on coefficient precomputation [21], [22] or lowpass-to-bandpass transformation [23], [24] to implement a programmable NTF. In this paper, we use the more flexible method developed in [25], which is based on the direct placement of poles and zeros on the z -plane.

In our previous paper [19], a fourth-order NTF was used to create a wide notch in the RX-band. However, further analysis revealed that in practice a fourth-order NTF brings little to no performance improvement compared with a second-order NTF, while causing at least a twofold increase in the implementation cost. Therefore, it was eventually decided to realize second-order noise shaping for the TX of this paper.

The general expression of a second-order NTF from [25] is

$$\text{NTF}(z) = \frac{1 + \alpha z^{-1} + z^{-2}}{1 + r \alpha z^{-1} + r^2 z^{-2}} \quad (2)$$

where $\alpha \in (-2, 2)$ determines the notch frequency, and $r \in [0, 1]$ the maximum gain of the NTF. System-level simulations revealed that $r = 0.5$ is appropriate in our application. By choosing 8 bits of resolution for α , a tuning step smaller than 5 MHz at $f_c = 900$ MHz is achieved for offsets between 30 and 400 MHz. The frequency response of (2) is plotted in Fig. 6 for three different values of α . Furthermore, as will be shown next, the selected NTF leads to significant complexity reduction in the implementation of the loop filter.

2) Loop Filter Implementation: Even though the $\Delta\Sigma$ modulator itself only accounts for a small fraction of the overall system complexity, the EF $\Delta\Sigma$ loop is also the basic building block of the mismatch-shaping encoder, as Section III-B will show. Hence, an optimized implementation of the loop filter directly benefits the entire DSP system.

The design process starts from a conventional transposed-direct-form-II realization of the transfer function $\text{NTF}(z) - 1$ in the general case given by (1), with $M = 2$. Fig. 7(a) shows the resulting structure. Because all four coefficients $\{b_1, b_2, a_1, a_2\}$ should be programmable, four hardware multipliers are needed in the filter, leading to large implementation complexity.

A first major simplification is achieved by replacing the generic NTF coefficients with the corresponding expressions from (2), as shown in Fig. 7(b). The main advantage is that r does not need to be fully programmable because it only affects the maximum NTF gain. For example, in this paper a fixed $r = 0.5$ was chosen. Therefore, a hardware multiplier is not needed for r , and a much cheaper realization based on binary shifts and additions is possible.

The multiple feedback paths in the circuit lead to further simplifications. By examining Fig. 7(b) and denoting with y the upper register, it can be noticed that term $r a y[n]$ is both added and subtracted. This is also evident by writing the expression of the register input

$$y[n+1] = (1 - r)\alpha \cdot (q[n] - u[n] - y[n]) - r a y[n] \quad (3)$$

where $u[n]$ and $q[n]$ are the modulator input and output, respectively. A similar reasoning holds for term $r^2 y[n]$. These simplifications result in the structure of Fig. 7(c).

Last, we note that coefficients $1 - r$ and $1 - r^2$ in Fig. 7(c) are located between two additions. This breaks the datapath extraction during synthesis, preventing the inference of a multioperand adder with a single carry propagation stage [38], [39]. Hence, for better quality-of-results, it is convenient to move the two coefficients to the $u[n]$ and $q[n]$ inputs of the first adder.

The final circuit implemented in HDL is shown in Fig. 7(d). The optimized datapath cells extracted during synthesis are marked in yellow. The 15-to-10 quantizer is realized as a simple truncation (T) of the five LSBs, preceded by a constant addition for rounding purposes. The full internal wordlength for fixed-point implementation is 20 bits, since five additional LSBs are used in the feedback paths to achieve sufficient precision. As the EF loop only processes the quantization error, the wordlengths of most internal signals can in fact be reduced. For example, both registers in Fig. 7(d) are 12-bits wide.

B. Mismatch-Shaping Encoder

Several scrambling encoder topologies have been devised and implemented over the years, a selection of which can be found in [26]–[35]. As discussed in [19], the segmented tree-structure dynamic element matching encoder [34] used in mismatch-shaping configuration [29] is a good candidate for the needs of our system.

The architecture of the implemented tree encoder is shown in Fig. 8. The structure is tailored to a 10-bit DAC with

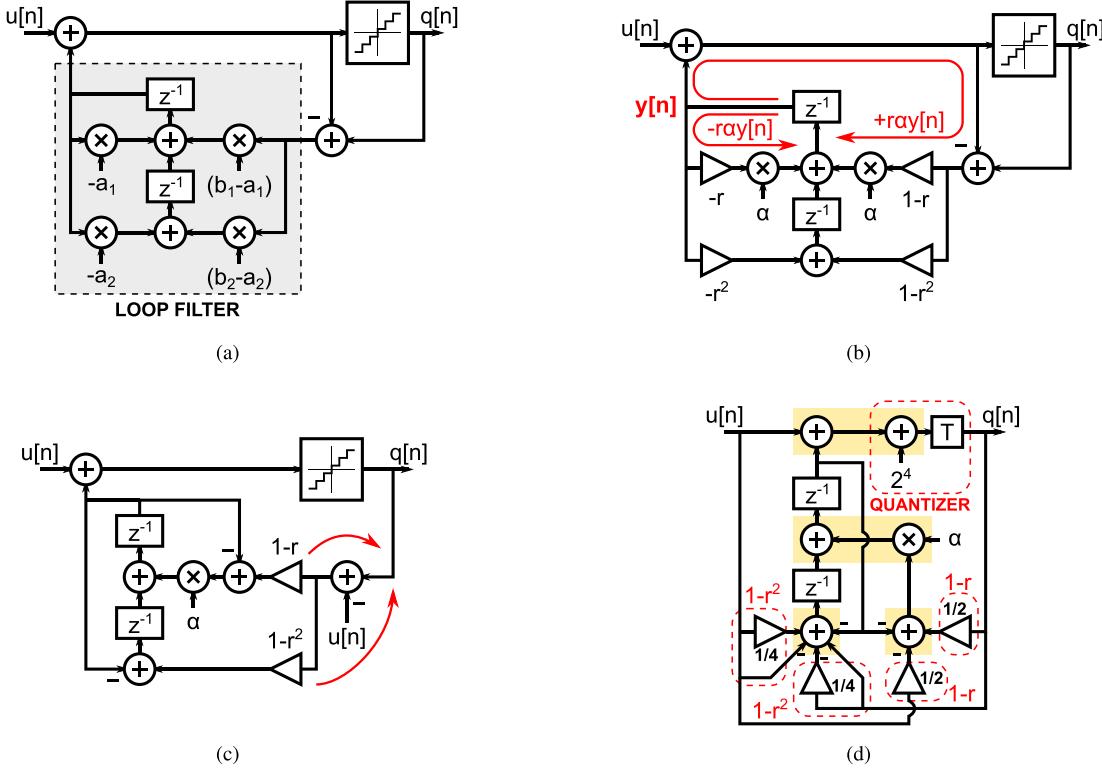


Fig. 7. Design process of the loop filter. (a) Conventional transposed-direct-form-II structure realizing a generic 2nd-order NTF from (1). (b) Applying the coefficients from (2). (c) Simplifying the terms which are both added and subtracted due to multiple feedback paths. (d) Final circuit implemented in HDL, where each yellow box is synthesized as an optimized datapath cell.

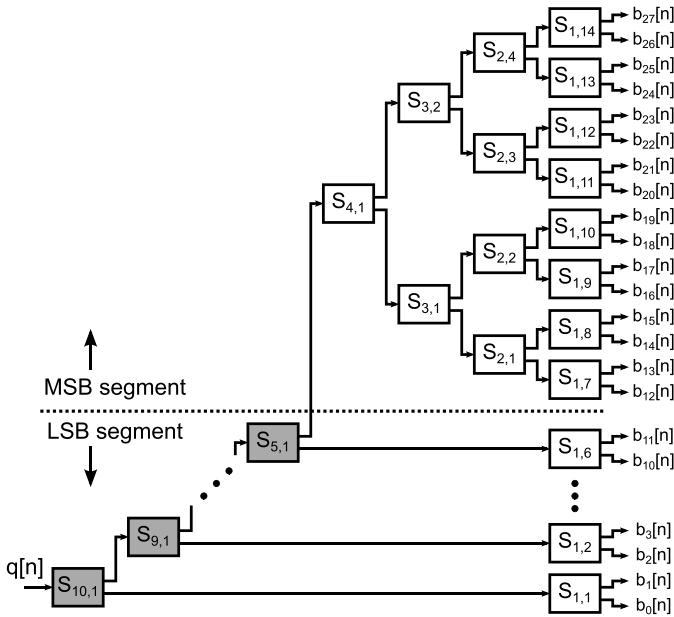


Fig. 8. Tree-structure mismatch-shaping encoder with 4 MSB + 6 LSB segmentation.

4 MSB + 6 LSB segmentation, where the MSB segment includes 16 unary weighted conversion cells with weight 64, and the LSB segment uses binary weights 32, 16, ..., 1. The binary cells are doubled to create the necessary redundancy for mismatch-shaping, resulting in a total of 28 conversion cells.

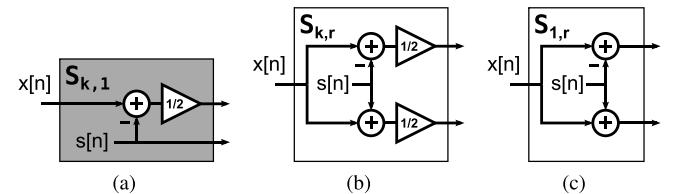


Fig. 9. Switching blocks for signed operation. (a) Segmenting. (b) Nonsegmenting, $k > 1$. (c) Nonsegmenting, $k = 1$.

The tree encoder consists of a cascade of segmenting and nonsegmenting switching blocks arranged into ten layers, with pipeline registers (not shown in Fig. 8) inserted between each layer. The function of each switching block is to split its input signal into two components, such that their weighted sum equals the input, while their individual spectral densities preserve the RX-band notch. By applying this principle iteratively throughout all layers, the operation of the whole encoder can be understood: the 1-bit outputs $b_i[n]$ are such that their weighted sum equals the encoder input $q[n]$, while their individual spectral densities still show the RX-band notch.

1) Switching Blocks: The original segmented tree encoder [34] assumes that all data propagating through the switching blocks be in unsigned integer format. In order to function correctly, this requires the addition of a constant offset to the encoder input. For example, in Fig. 8 the 10-bit signed encoder input $q[n] \in \{-512, \dots, +511\}$ would need to be mapped to the range $\{63, \dots, 1086\}$ for correct operation.

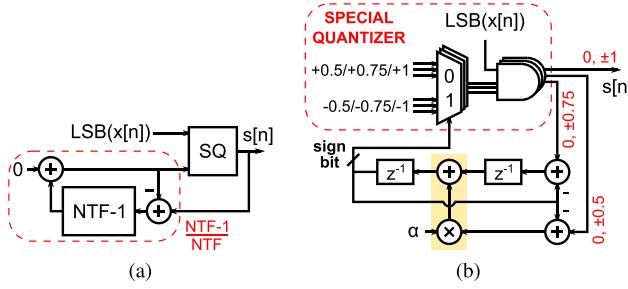


Fig. 10. Sequence generator internal to each switching block. (a) Conceptual block diagram, emphasizing the similarity with the EF $\Delta\Sigma$ modulator of Fig. 5. (b) Circuit implemented in HDL. For $S_{1,r}$, the $LSB(x[n])$ input is negated. The yellow box is synthesized as an optimized datapath cell.

In this paper, the internal structure of the switching blocks is modified to directly process signed data at no extra cost.

The modified structures are shown in Fig. 9. The main difference compared with [34] is that the switching blocks in the first layer ($k = 1$) do not need the $1/2$ gains factors. The $s[n]$ sequences are still generated internally within each block, and must satisfy

$$s[n] = \begin{cases} 0 & \text{if } x[n] \text{ is even} \\ \pm 1 & \text{if } x[n] \text{ is odd} \end{cases} \quad (4)$$

for layers $k > 1$, and

$$s[n] = \begin{cases} 0 & \text{if } x[n] \text{ is odd} \\ \pm 1 & \text{if } x[n] \text{ is even} \end{cases} \quad (5)$$

for the first layer $k = 1$. By analyzing the encoder structure under these constraints, it can be proven that for $q[n] \in \{-512, \dots, +511\}$, the $b_i[n]$ outputs take values only in $\{-1, +1\}$. Therefore, the sign bits of each $b_i[n]$ can be directly used to drive the corresponding conversion cells in the DAC.

2) *Sequence Generator:* The ternary sequences $s[n] \in \{-1, 0, +1\}$ must be generated within each switching block in a pseudorandom fashion, such that their spectral densities are shaped by the same NTF used for the $\Delta\Sigma$ modulator [29]. This can be done by utilizing an EF $\Delta\Sigma$ loop in the configuration of Fig. 10(a), with no signal input. The special quantizer (SQ) ensures that (4) and (5) are fulfilled, by forcing $s[n]$ to 0 or ± 1 depending on the sign of the loop filter output and the LSB of $x[n]$.

Because of the similarity between the circuits of Figs. 5 and 10(a), the loop filter optimization process described in Section III-A and shown in Fig. 7 can be applied in its entirety to the sequence generator as well. Furthermore, the new input-output constraints enable additional simplifications. Referring to Fig. 7(d) with $s[n]$ instead of $q[n]$, the three possible results of $(1 - r)s[n]$ and $(1 - r^2)s[n]$ for $s[n] \in \{-1, 0, +1\}$ can be precomputed and conditionally selected by the means of multiplexers and AND gates. The final circuit implemented in HDL is shown in Fig. 10(b). The full wordlength for the signals in the feedback loop is now 11 bits.

C. RF Front-End

Because OOB specifications place the tightest demands on all-digital TXs, the proposed DSP-based noise attenuation

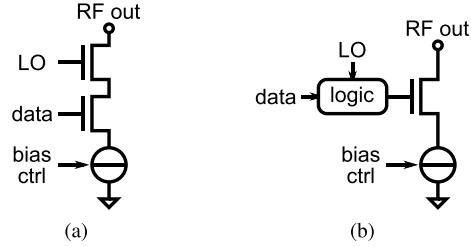


Fig. 11. Conceptual illustration of (a) “series mixing” and (b) “logic mixing” approaches, used to perform D/A upconversion of a single data bit in a current-steering RF-DAC.

method allows to significantly relax the performance requirements on the RF front-end. Therefore, no overdesigning or special circuit techniques are needed, and well-established RF-DAC architectures can be employed. In this paper, we opted for a cascaded current-steering structure because of its improved output impedance, as well as its high speed and large power control capabilities.

Most published current-steering RF-DAC structures can be broadly divided into two classes, depending on how the upconversion to RF is implemented. In the first class, upconversion is realized with the “series mixing” approach shown in Fig. 11(a): a separate switch driven by the LO signal is connected in series with the data switch and the current source (CS) [8], [9], [11], [40], [41]. The second class utilizes the “logic mixing” approach shown in Fig. 11(b): upconversion is performed before the actual D/A conversion by the means of simple logic gates, and a single switch is needed in series with the CS [12], [42]–[44]. Because in our system the voltage headroom is limited by the 1.5-V supply, using two series switches for LO and data is not feasible, and the “logic mixing” approach is chosen.

The detailed implementation of the RF front-end is shown in Fig. 12. The design is optimized for high linearity and low phase noise, with a moderate penalty in power consumption. The phase noise of the LO path is minimized by placing strong buffers on the longest wire segments. Each of the 28 mismatch-shaping encoder outputs is synchronized to the LO and separately upconverted through a logic circuit clocked at $2f_c$, which generates two pseudodifferential outputs c_P and c_N with 50% duty-cycle. In order to avoid cross-interaction between the I and Q paths, it is desirable to use 25% duty-cycling [11], [40], [42]. This can be achieved by performing a final AND with the 2LO signal before the conversion cell [42]. Such an arrangement has the additional advantage to hide the skews between different data bits [45], since the transitions of all c_P and c_N signals take place during the low phase of 2LO. The differential encoding ensures nearly constant current flow from the power supply, thus eliminating signal-dependent IR drop. The DAC array is segmented with the same 4 MSB + 6 LSB strategy used for the mismatch-shaping encoder, resulting in 16 unary cells with weight 64, and 6×2 binary cells with weights 32, 32, 16, 16, \dots , 1, 1. Cells with weight $K > 1$ are implemented by connecting in parallel K cells with weight 1. In the layout, decoupling capacitance is added wherever possible to stabilize all sensitive supply and bias nodes. However, no extra care is taken in the layout to

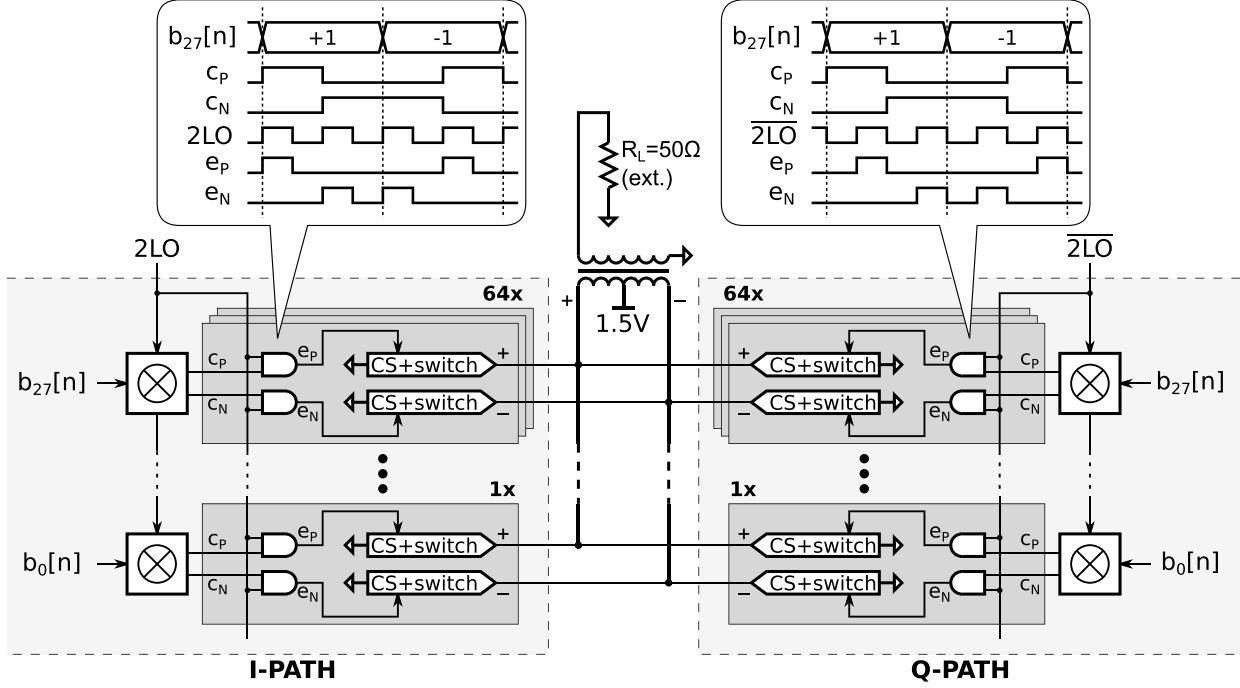


Fig. 12. RF front-end of the TX, including digital mixing, D/A conversion, and on-chip output balun.

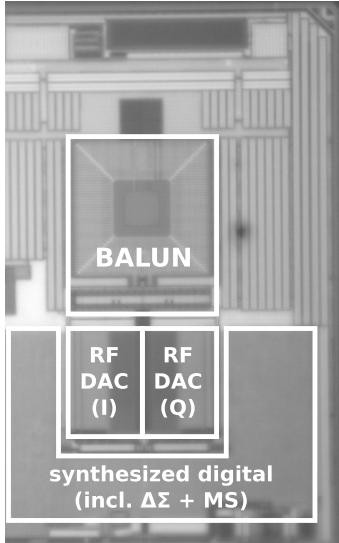


Fig. 13. Chip micrograph.

improve the matching. For example, the LO signal does not need a power-hungry tree distribution, since the nonlinearity caused by small timing imbalances is effectively shaped by the mismatch-shaping encoder.

IV. MEASUREMENT RESULTS

The complete system of Fig. 4 was integrated as the low-band TX path of a larger prototype 4G SoC. The chip was fabricated in a 28-nm CMOS process, and packaged with flip-chip technology. The die micrograph is shown in Fig. 13. The total active area of the highlighted blocks is 0.82 mm^2 , of which 0.47 mm^2 are occupied by the RF front-end. The

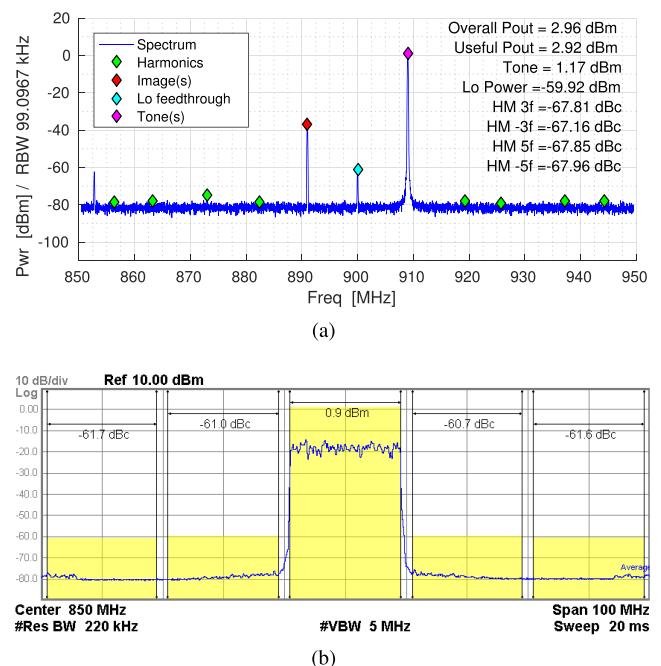


Fig. 14. Measured spectra for (a) 9-MHz CW tone at $f_c = 900 \text{ MHz}$ and (b) LTE20 signal at $f_c = 850 \text{ MHz}$ (Band 20).

circuit uses 1.5-V supply for the DACs, and two separate 0.9-V supply domains for the rest of the circuit: one for the synthesized digital part, and one for the LO path and digital mixers.

The measured output spectrum of a 9-MHz continuous-wave (CW) tone at 900-MHz carrier frequency is shown in Fig. 14(a). At +3 dBm output power, the image and LO feedthrough are at -36 and -61 dBc, respectively. The CIM3

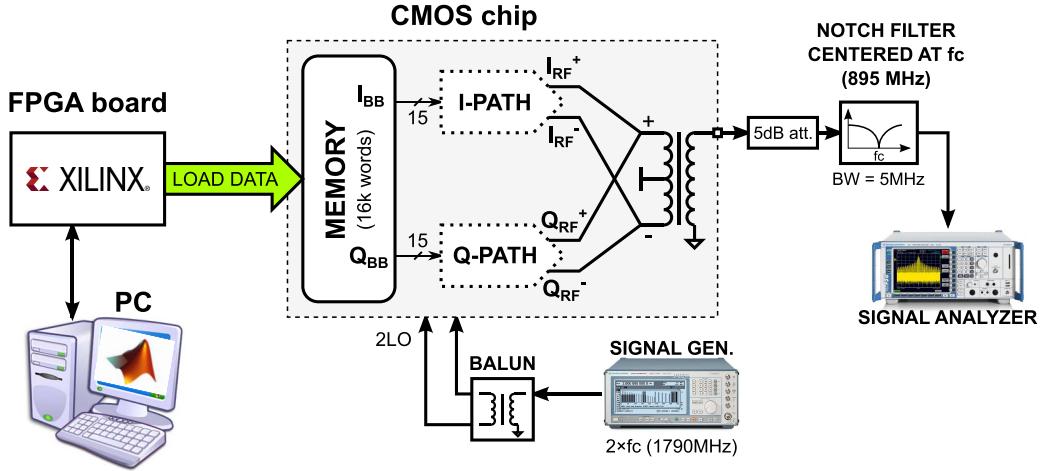


Fig. 15. Setup for OOB noise measurements.

and CIM5 are both below -67 dBc, barely visible above the noise floor. The overall power consumption of the TX is 150 mW, of which 75 mW are taken by the DACs, 22 mW by the LO path and digital mixers, and 53 mW by the $\Delta\Sigma$ modulators and mismatch-shaping encoders.

Fig. 14(b) plots the output spectrum with a $+0.9$ dBm LTE20 signal at 850 MHz (Band 20). Excellent E-UTRA ACLR performance of less than -60 dBc is achieved. Because of the limited on-chip memory size, the EVM cannot be measured. Nevertheless, the good overall linearity demonstrated with other performance metrics guarantees that the LTE EVM specifications would be met with wide margin. Both $\Delta\Sigma$ modulation and mismatch-shaping are active in the measurements of Fig. 14, but the notch is intentionally tuned out of the visible frequency span, in order to prove that the selected NTF does not degrade the signal quality in the passband.

Fig. 15 shows the setup used for OOB noise measurements. A notch filter centered at f_c is inserted at the TX output, in order not to saturate the spectrum analyzer while measuring very low noise levels. In addition, a 5-dB attenuator is needed to suppress the TX power that is reflected by the notch filter back to the chip. This arrangement enables to measure the OOB noise at an arbitrary offset from f_c , thus obviating the need for several duplexers. However, the notch filter has a fixed center frequency of 895 MHz with a stopband of 5 MHz. Hence, it is not possible to measure at different carrier frequencies or use modulated bandwidths larger than 5 MHz. All cable and filter losses are de-embedded from the results reported in this paper.

Fig. 16 plots the OOB spectra for a 1.709 -MHz CW tone at $+3$ dBm output power. The measurement is repeated in three different modes, corresponding to the configurations shown in Fig. 2(a)–(c). For the first mode, the baseband signal is linearly quantized directly to 10 bits and fed to the tree encoder with all sequence generator registers [Fig. 10(b)] in reset state, which turns the structure into a classical binary/thermometer encoder. For the second mode, the $\Delta\Sigma$ modulator is in use with the notch tuned to 95 -MHz offset, but mismatch-shaping is still disabled. For the last mode, both $\Delta\Sigma$ and mismatch-shaping

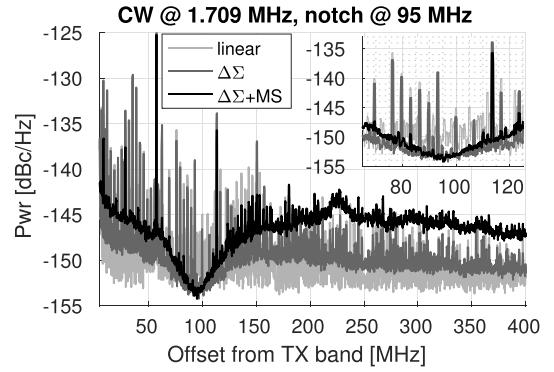


Fig. 16. OOB spectra for a $+3$ dBm CW tone, measured for different configuration modes [corresponding to Fig. 2(a)–(c)].

are enabled. The figure demonstrates the basic operation of mismatch-shaping, where the high-order nonlinearity arising from static mismatches (visible in the first two modes as a large amount of spurs) is converted to spectrally shaped noise. For example, mismatch-shaping improves the LO feedthrough and CIM3/CIM5 products by 10 and 7 dB, respectively. The measurement of Fig. 16 is limited by the noise figure of the signal analyzer, which is about 20 dB without using the internal pre-amplifier.

Fig. 17 combines the results of several RX-band noise measurements, performed with modulated LTE carriers at seven duplex distances selected from the LTE radio standard [37]. Each measurement is repeated in the same three modes as before [Fig. 2(a)–(c)]. The results show that OOB emissions are dominated by quantization noise in the first mode, and by mismatch noise in the second mode (especially at small duplex offsets). In the third mode, with both $\Delta\Sigma$ and mismatch-shaping enabled, the averaged RX-band noise is between -155 and -163 dBc/Hz at all measured offsets, which is sufficiently low for SAW-less operation. The notch center frequency is not restricted to the chosen duplex distances, but can be freely tuned within ± 447.5 MHz of the 895 -MHz carrier frequency, the only limit being the 8 -bit resolution of α in (2).

Fig. 17 also shows the expected performance from the system-level model developed in [19], using the mismatch statistics obtained from circuit-level simulations on the RF

TABLE I
PERFORMANCE COMPARISON

	ISSCC 2013 [3]	ISSCC 2015 [5]	ISSCC 2017 [6]	JSSC 2007 [8]	ISSCC 2011 [9]	ISSCC 2016 [15]	ISSCC 2017 [10]	This work
Architecture	Analog	Analog	Analog	DDRM	Polar	RQDAC	Polar	$\Delta\Sigma+MS$ DAC
DAC resolution [bits]	N/A	N/A	N/A	10	14	12	15	10
RF bandwidth [MHz]	20	10	20	20	5	20	40	20
Pout [dBm]	3.8	2	4.9 ²	2	6 ⁴	3.5	6	3
ACLR [dBc]	-41	-54	-42	-58	-50	-49	-45	-61
CIM3 [dBc]	< -60	< -70	-68	N/A	N/A	< -50	< -70	-67
RX-band noise [dBc/Hz]	-158.7 @ 30MHz	-157.9 @ -31MHz	-155 @ 30MHz	-144 @ 190MHz	-160 @ 45MHz	-159 @ 45MHz	-152 @ -31MHz	-158 @ 30MHz
Active area [mm²]	1.4	0.93	1.1	4 ³	2	0.22 ⁵	1.3	0.82
Supply [V]	1.1/2.5	1.8	1.0/1.8	1.2	2.5	0.9/1.1	1.0/1.1/1.3	0.9/1.5
Power consumption [mW]	159 ¹	216	120	157	119	11 ⁶	137	150
Technology [nm]	40	40	14	130	N/A	28	28	28

¹ data for Band 8² in 4G mode³ total chip area⁴ in 3G mode⁵ RF balun and DSP not implemented on-chip⁶ RF front-end at 7dB backoff, excluding off-chip DSP

front-end. The standard deviations of the random amplitude and LO timing mismatches are 3% of the LSB and 0.3 ps, respectively. Moreover, a systematic LO timing gradient of approximately 0.15 ps per conversion cell (increasing from LSB to MSB) is added to the random timing mismatch. Good agreement between predicted and measured values is observed for the modes without mismatch-shaping, thus confirming that quantization and mismatch noise are the performance limiting factors. For the mode with mismatch-shaping enabled, all simulated values (not shown in Fig. 17) are below -168 dBc/Hz. This is unrealistic, since the system-level model does not account for second-order effects, such as LO phase noise and memory in the RF-DAC. Nevertheless, the residual noise floor arising from these effects does not impair SAW-less operation.

Figs. 18 and 19 plot the OOB noise spectra for some of the measurements reported in Fig. 17(c). The zoomed-in-view insets in Fig. 18 are obtained by enabling the internal pre-amplifier of the signal analyzer, in order to measure the actual spectral densities in the RX-band without being limited by the instrument noise floor. Enabling $\Delta\Sigma$ modulation and mismatch-shaping yields up to 20-dB attenuation of the averaged RX-band noise compared with linear quantization, while causing just a moderate increase of the noise floor elsewhere. The small peak visible around $f_c/4$ (224 MHz) with the notch at 120 MHz is caused by nonlinear dynamics within the mismatch-shaping algorithm, which require further study. Nevertheless, even by accounting for power amplifier gain, the higher spectral density in the aforementioned cases is still well below the general spurious emission limits specified for LTE5, e.g., -86 dBm/Hz for frequencies above 40 MHz from the edge of the transmit band [37].

The spurs visible in Figs. 16, 18, and 19 around the multiples of 56-MHz offset are due to intermodulation with the $f_c/16$ clock of the on-chip memory. The large first harmonic (which is evident also in Fig. 14) increases the noise floor

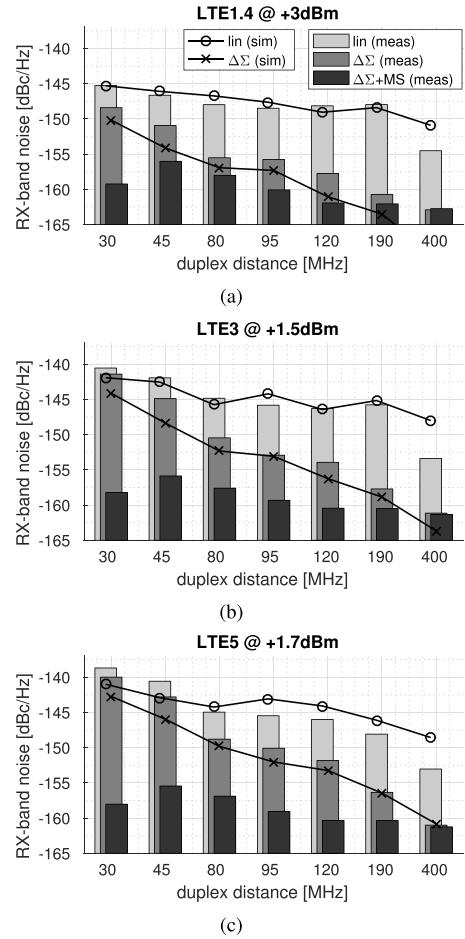


Fig. 17. Measurement of RX-band noise at various duplex distances, repeated for (a) LTE1.4, (b) LTE3, and (c) LTE5 signals, in the different configuration modes corresponding to Fig. 2(a)–(c). Simulation results for the cases with mismatch-shaping disabled are also shown.

in its vicinity, thus degrading the measured performance at 45-/80-MHz duplex distances (Fig. 17). Fortunately, these spurs are not a real issue in practice. First, the memory is only

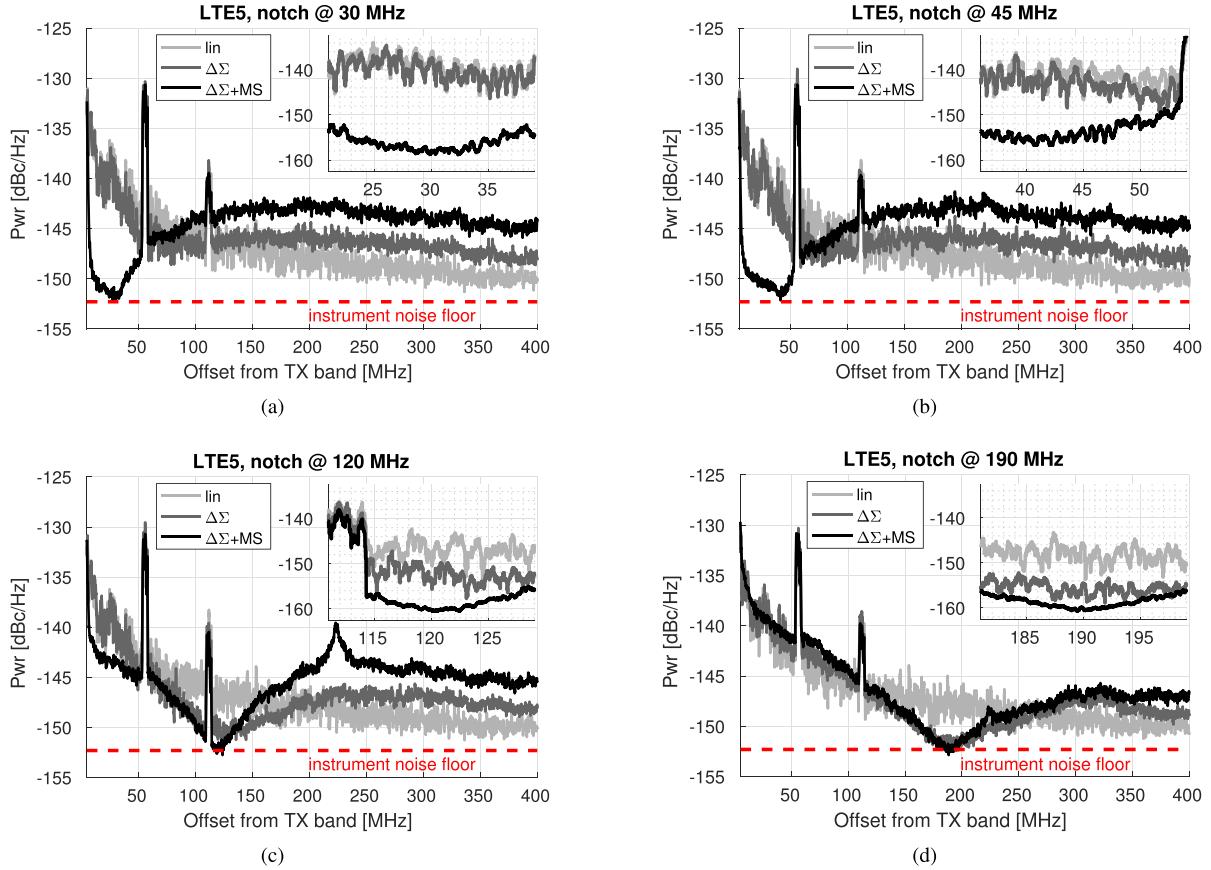


Fig. 18. OOB spectra for a selection of the measurements reported in Fig. 17(c), corresponding to the programmed duplex distances of (a) 30 MHz, (b) 45 MHz, (c) 120 MHz, and (d) 190 MHz. The zoomed-in-view RX-band insets are obtained by enabling the internal pre-amplifier of the signal analyzer, in order to overcome the instrument noise floor.

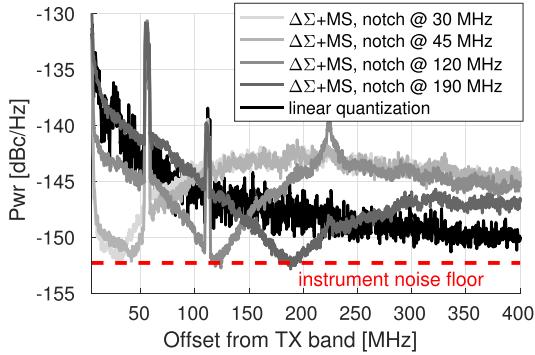


Fig. 19. Comparison between various OOB spectra from Fig. 18, showing the effect of tuning the notch to different offset frequencies.

implemented in this chip for prototyping purposes, whereas in a final implementation data would come from the baseband processor. Second, the presented TX is part of a larger SoC, which has digital circuits clocked at other frequencies, such as $f_c/2$, $f_c/4$, and a fixed 38.4-MHz reference. No important spurs from these clocks can be noticed in the measured spectra, indicating that also the isolation between memory and RF parts could be boosted through more careful design and layout.

Table I compares the TX with previous implementations. This paper stands out for its superior ACLR and compact die area, while exhibiting state-of-art overall performance.

Furthermore, our TX demonstrates for the first time the feasibility of all-digital RX-band noise filtering. As shown in Table I, this is the only published implementation achieving RX-band noise close to -160 dBc/Hz with a 10-bit DAC and no need for DPD, calibration or analog filtering.

V. CONCLUSION

We presented the first all-digital LTE SAW-less TX with programmable DSP-based attenuation of RX-band noise. The system, implemented in 28-nm CMOS with only 0.82-mm^2 active area, utilizes digital bandpass $\Delta\Sigma$ modulation and mismatch-shaping to push the DAC noise outside the RX-band. This solution enables between -155 and -163 dBc/Hz noise at a programmable 30–400 MHz duplex distance, by using a conventional current-steering DAC with only 10-bit resolution and no DPD, calibration nor analog filtering. Furthermore, the circuit achieves CIM3/CIM5 below -67 dBc, and ACLR of -61 dBc with LTE20 carrier. Even though the system was validated in an LTE environment, its operation with legacy standards, such as 2G and 3G is not precluded.

Unlike previous methods, our purely digital approach fully exploits the standard digital design methodology to enable design reusability and portability, while leveraging the fast and cheap DSP logic available in deep-submicrometer CMOS processes. Therefore, the presented TX inherits all the advantages of digital RF, making it a competitive low-cost solu-

tion for integration with the application and digital baseband processors into a single 4G SoC, with a minimal count of external components.

ACKNOWLEDGMENT

The authors are grateful to F. Steininger for his advice on DSP optimization and to K.-F. Bink for his help in building the measurement setup.

REFERENCES

- [1] O. Oliae *et al.*, “A multiband multimode transmitter without driver amplifier,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 164–165.
- [2] T. Kihara *et al.*, “A multiband LTE SAW-less CMOS transmitter with source-follower-driven passive mixers, envelope-tracked RF-PGAs, and Marchand baluns,” in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2012, pp. 399–402.
- [3] M. Ingels, Y. Furuta, X. Zhang, S. Cha, and J. Craninckx, “A multiband 40 nm CMOS LTE SAW-less modulator with -60 dBc C-IM3,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 338–339.
- [4] N. Codega, P. Rossi, A. Pirola, A. Liscidini, and R. Castello, “A current-mode, low out-of-band noise LTE transmitter with a class-A/B power mixer,” *IEEE J. Solid-State Circuits*, vol. 49, no. 7, pp. 1627–1638, Jul. 2014.
- [5] Y.-H. Chen, N. Fong, B. Xu, and C. Wang, “An LTE SAW-less transmitter using 33% duty-cycle LO signals for harmonic suppression,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 1–3.
- [6] V. Bhagavatula *et al.*, “A SAW-less reconfigurable multimode transmitter with a voltage-mode harmonic-reject mixer in 14 nm FinFET CMOS,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 220–221.
- [7] E. Roverato *et al.*, “A configurable sampling rate converter for all-digital 4G transmitters,” in *Proc. 21st Eur. Conf. Circuit Theory Design (ECCTD)*, Sep. 2013, pp. 1–4.
- [8] P. Eloranta, P. Seppinen, S. Kallioinen, T. Saarela, and A. Pärssinen, “A multimode transmitter in $0.13\text{ }\mu\text{m}$ CMOS using direct-digital RF modulator,” *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2774–2784, Dec. 2007.
- [9] Z. Boos *et al.*, “A fully digital multimode polar transmitter employing 17b RF DAC in 3G mode,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 376–378.
- [10] M. Fulde *et al.*, “A digital multimode polar transmitter supporting 40 MHz LTE carrier aggregation in 28 nm CMOS,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 218–219.
- [11] W. M. Gaber, P. Wambacq, J. Craninckx, and M. Ingels, “A CMOS IQ direct digital RF modulator with embedded RF FIR-based quantization noise filter,” in *Proc. ESSCIRC*, Sep. 2011, pp. 139–142.
- [12] S. Fukuda, S. Miya, M. Io, K. Hamashita, and B. Nauta, “Direct-digital modulation (DDIMO) transmitter with -156 dBc/Hz Rx-band noise using FIR structure,” in *Proc. ESSCIRC*, Sep. 2012, pp. 53–56.
- [13] R. Bhat and H. Krishnaswamy, “A watt-level 2.4 GHz RF I/Q power DAC transmitter with integrated mixed-domain FIR filtering of quantization noise in 65 nm CMOS,” in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2014, pp. 413–416.
- [14] R. Bhat, J. Zhou, and H. Krishnaswamy, “A >1 W 2.2 GHz switched-capacitor digital power amplifier with wideband mixed-domain multi-tap FIR filtering of OOB noise floor,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 234–235.
- [15] P. E. P. Filho, M. Ingels, P. Wambacq, and J. Craninckx, “A 0.22 mm^2 CMOS resistive charge-based direct-launch digital transmitter with -159 dBc/Hz out-of-band noise,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2016, pp. 250–252.
- [16] T. Nakatani, H. Gheidi, V. W. Leung, D. F. Kimball, and P. M. Asbeck, “Signal generation algorithm for digital polar transmitters with reduced receive band noise,” in *Proc. IEEE Top. Conf. Power Modeling Wireless Radio Appl. (PAWR)*, Jan. 2014, pp. 70–72.
- [17] J. Mehta *et al.*, “A 0.8 mm^2 all-digital SAW-less polar transmitter in 65 nm EDGE SoC,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 58–59.
- [18] M. Park, M. H. Perrott, and R. B. Staszewski, “An amplitude resolution improvement of an RF-DAC employing pulsedwidth modulation,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 11, pp. 2590–2603, Nov. 2011.
- [19] E. Roverato, M. Kosunen, J. Lemberg, K. Stadius, and J. Ryyynänen, “RX-band noise reduction in all-digital transmitters with configurable spectral shaping of quantization and mismatch errors,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 11, pp. 3256–3265, Nov. 2014.
- [20] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*. Hoboken, NJ, USA: Wiley, 2005.
- [21] K. Yamamoto, A. C. Carusone, and F. P. Dawson, “A delta-sigma modulator with a widely programmable center frequency and 82-dB peak SNDR,” *IEEE J. Solid-State Circuits*, vol. 43, no. 8, pp. 1772–1782, Aug. 2008.
- [22] S. Asghar, R. del Rio, and J. de la Rosa, “A 0.2-to-2 MHz BW, 50-to-86 dB SNDR, 16-to-22 mW flexible 4-order $\Sigma\Delta$ modulator with DC-to-44 MHz tunable center frequency in 1.2-V 90-nm CMOS,” in *Proc. IEEE/IFIP Int. Conf. VLSI-SoC*, Oct. 2012, pp. 47–52.
- [23] L. Cardelli, L. Fanucci, V. Kempe, F. Mannozzi, and D. Strle, “Tunable bandpass sigma delta modulator using one input parameter,” *Electron. Lett.*, vol. 39, no. 2, pp. 187–189, Jan. 2003.
- [24] J. Lindeberg, J. Vankka, J. Sommarek, and K. Halonen, “A 1.5-V direct digital synthesizer with tunable delta-sigma modulator in $0.13\text{-}\mu\text{m}$ CMOS,” *IEEE J. Solid-State Circuits*, vol. 40, no. 9, pp. 1978–1982, Sep. 2005.
- [25] E. Roverato, M. Kosunen, and J. Ryyynänen, “The synthesis of noise transfer functions for bandpass delta-sigma modulators with tunable center frequency,” in *Proc. 22nd Eur. Conf. Circuit Theory Design (ECCTD)*, Aug. 2015, pp. 1–4.
- [26] R. T. Baird and T. S. Fiez, “Linearity enhancement of multibit $\Delta\text{-}\Sigma$ A/D and D/A converters using data weighted averaging,” *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 42, no. 12, pp. 753–762, Dec. 1995.
- [27] R. Schreier and B. Zhang, “Noise-shaped multibit D/A converter employing unit elements,” *Electron. Lett.*, vol. 31, no. 20, pp. 1712–1713, Sep. 1995.
- [28] R. K. Henderson and O. J. A. P. Nys, “Dynamic element matching techniques with arbitrary noise shaping function,” in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 1996, pp. 293–296.
- [29] I. Galton, “Spectral shaping of circuit errors in digital-to-analog converters,” *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 44, no. 10, pp. 808–817, Oct. 1997.
- [30] R. Adams and K. Q. Nguyen, “A 113-dB SNR oversampling DAC with segmented noise-shaped scrambling,” *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1871–1878, Dec. 1998.
- [31] A. Yasuda, H. Tanimoto, and T. Iida, “A third-order $\Delta\text{-}\Sigma$ modulator using second-order noise-shaping dynamic element matching,” *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1879–1886, Dec. 1998.
- [32] T. Shui, R. Schreier, and F. Hudson, “Mismatch shaping for a current-mode multibit delta-sigma DAC,” *IEEE J. Solid-State Circuits*, vol. 34, no. 3, pp. 331–338, Mar. 1999.
- [33] T. S. Kaplan, J. F. Jensen, C. H. Fields, and M.-C. F. Chang, “A 2-GS/s 3-bit $\Delta\text{-}\Sigma$ -modulated DAC with tunable bandpass mismatch shaping,” *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 603–610, Mar. 2005.
- [34] K. L. Chan, J. Zhu, and I. Galton, “Dynamic element matching to prevent nonlinear distortion from pulse-shape mismatches in high-resolution DACs,” *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 2067–2078, Sep. 2008.
- [35] M. Neitola and T. Rahkonen, “A generalized data-weighted averaging algorithm,” *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 2, pp. 115–119, Feb. 2010.
- [36] E. Roverato *et al.*, “All-digital RF transmitter in 28 nm CMOS with programmable RX-band noise shaping,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 222–223.
- [37] *User Equipment (UE) Radio Transmission and Reception, Rev. 14.2.1*, Standard TS 36.101, 3GPP, Jan. 2017.
- [38] B. Parhami, *Computer Arithmetic: Algorithms and Hardware Design*, 2nd ed. London, U.K.: Oxford Univ. Press, 2010.
- [39] “Coding guidelines for datapath synthesis,” Synopsys, Mountain View, CA, USA, White Paper 015771, Sep. 2013.
- [40] M. S. Alavi, G. Voicu, R. B. Staszewski, L. C. N. de Vreede, and J. R. Long, “A 2×13 -bit all-digital I/Q RF-DAC in 65-nm CMOS,” in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2013, pp. 167–170.
- [41] E. Bechthum, G. I. Radulov, J. Briaire, G. J. G. M. Geelen, and A. H. M. van Roermund, “A wideband RF mixing-DAC achieving IMD <-82 dBc up to 1.9 GHz,” *IEEE J. Solid-State Circuits*, vol. 51, no. 6, pp. 1374–1384, Jun. 2016.
- [42] A. Pozsgay, T. Zounes, R. Hossain, M. Boulemnakher, V. Knopik, and S. Grange, “A fully digital 65 nm CMOS transmitter for the 2.4-to-2.7 GHz WiFi/WiMAX bands using 5.4 GHz $\Delta\text{-}\Sigma$ RF DACs,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 360–361.

- [43] C. Lu *et al.*, "A 24.7 dBm all-digital RF transmitter for multimode broadband applications in 40 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 332–333.
- [44] C. Erdmann *et al.*, "A 330 mW 14 b 6.8 GS/s dual-mode RF DAC in 16 nm FinFET achieving -70.8 dBc ACPR in a 20 MHz channel at 5.2 GHz," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 280–281.
- [45] H. Wang *et al.*, "A highly-efficient multi-band multi-mode all-digital quadrature transmitter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 5, pp. 1321–1330, May 2014.



Enrico Roverato (S'13–M'17) was born in Padua, Italy, in 1988. He received the B.Sc. degree in information engineering from the University of Padua, Padua, in 2010, and the M.Sc. and D.Sc. degrees in electrical engineering from Aalto University, Espoo, Finland, in 2012 and 2017, respectively.

Since 2012, he has been with the Department of Electronics and Nanoengineering, Aalto University, where he is currently a Post-Doctoral Researcher. His current research interests include all-digital RF transmitter circuits, with special focus on the implementation of high-speed DSP algorithms.

Marko Kosunen (S'97–M'07) received the M.Sc., L.Sc., and D.Sc. (Hons.) degrees from the Helsinki University of Technology, Espoo, Finland, in 1998, 2001, and 2006, respectively.

He is currently a Senior Researcher with the Department of Electronics and Nanoengineering, Aalto University, Espoo. His expertise is in implementation of the wireless transceiver DSP algorithms and communication circuits. He is currently involved in the implementations of cognitive radio spectrum sensors, digital-intensive transceiver circuits, and medical sensor electronics.

Koen Cornelissem received the M.Sc. degree in electrical engineering from KU Leuven, Leuven, Belgium, in 2004, and the Ph.D. degree from KU Leuven, in 2010, for his work entitled Delta-Sigma A/D Converter Design in Nanoscale CMOS.

He joined M4S as an Analog Design Engineer in 2010. In 2011, M4S was taken over by Huawei Technologies, Leuven, and converted into a Wireless Research and Development Center, where he is currently a Principal Analog Design Engineer on next generation cellular transceivers.

Sofia Vatti (S'06–M'14) was born in Athens, Greece, in 1980. She received the B.Sc. degree in electrical engineering from the University of Patras, Patras, Greece, in 2004, and the Ph.D. degree from Imperial College London, London, U.K., in 2008.

Since 2009, she has been with M4S-Huawei Technologies, Leuven, Belgium, as an RF IC Design Engineer, where she has been involved in the next generation cellular transceivers.

Paul Stynen was born in Antwerp, Belgium, in 1966. He received the master's degree in electronics from Katholieke Industriële Hogeschool Antwerpen, Hoboken, Belgium, in 1988.

He is currently with Huawei Technologies, Leuven, Belgium, as a Senior Digital Designer, specialized in very high speed (up to 10 GHz) digital RTL design and physical synthesis.



Teuvo Korhonen (M'15) was born in Sotkamo, Finland, in 1982. He received the M.Sc. degree in electrical engineering from the University of Oulu, Oulu, Finland, in 2010.

He is currently with Huawei Technologies, Helsinki, Finland, where he is currently involved in next generation terminal RFIC research and development.



Kaoutar Bertrand received the Master's degree from the Institut National des Postes et Telecommunications, Rabat, Morocco, in 2004.

After her graduation, she joined STMicroelectronics as a Physical Design Engineer, where she was involved in CMOS image sensors. Since then, she has been involved in the physical design of several blocks/SoC on several technologies and for several applications.



Hans Samsom received the Ph.D. degree from KU Leuven, Leuven, Belgium.

He has four years of research experience at IMEC, Leuven, researching the usage of memory optimization by transformational design. From 1995 to 2000, he was with Sitel Sierra Semiconductors, 's-Hertogenbosch, The Netherlands, and National Semiconductor, where he was involved in cordless phone solutions based on the DECT and PHS standard. In 2000, he joined the Belgian Research and Development Center, Resonext Communications. In this company and subsequently after the acquisition by RFMD, he developed 802.11a/b/g solutions, including the world's first PCI-Express-based WLAN SiP for the PC market and a low-power low-cost SDIO-based WLAN SoC solution for the mobile phone market. He was subsequently with Chipidea, Belgium, from 2005 to 2007, where he was involved in the product specification of RF transceivers for cellular and data networks. In 2007, he co-founded M4S, a fabless semiconductor startup in cellular radio market. In 2011, M4S was acquired by Huawei Technologies, Leuven, for which he is currently a Consultant with the Wireless Research and Development Center, HiSilicon, Leuven. His role included the definition and execution of successful semiconductor products, building teams, and managing engineering organizations. He has authored and presented 6+ papers at conferences and in journals, as well as 3+ patents issued or pending.

Patrick Vandenameele (S'96–M'00) was born Antwerp, Belgium, in 1973. He received the Ph.D. degree from KU Leuven, Leuven, Belgium, in 2000.

He was with IMEC on MIMO for WLAN applications in 2000. He joined Resonext Communications (acquired by Qorvo in 2003), developing fully integrated CMOS 802.11a/b/g solutions. He subsequently co-founded or consulted for several new wireless and/or semiconductor ventures, including Rivermark Technology Group, Sunnyvale, CA (providing soft WiFi IP for embedded systems), Essensium (indoor positioning technology), Future Waves (fabless semiconductor startup in mobile broadcasting market), and finally M4S (fabless semiconductor startup in cellular radio market acquired by Huawei Technologies in 2011). In each venture, his role included defining and executing semiconductor product roadmaps, raising funds, and building and managing engineering teams. Since 2017, he has been responsible for innovation management and venturing at IMEC. He has authored and presented 25+ papers at conferences and journals, as well as 21 patents issued or pending of which six licensed to third parties.



Jussi Rynnänen (S'99–M'04–SM'16) was born in Ilmajoki, Finland, in 1973. He received the M.Sc., Lic.Sc., and D.Sc. degrees in electrical engineering from the Helsinki University of Technology, Helsinki, Finland, in 1998, 2001, and 2004, respectively.

He is currently an Associate Professor with the Department of Electronics and Nanoengineering, Aalto University School of Electrical Engineering. He has authored or coauthored over 130 refereed journal and conference papers in the areas of analog and RF circuit design. He holds six patents on RF circuits. His current research interests include integrated transceiver circuits for wireless applications.

