

A 50 Gb/s 190 mW Asymmetric 3-Tap FFE VCSEL Driver

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Abstract—This paper describes the design of an energy-efficient vertical-cavity surface-emitting laser (VCSEL) driver circuit implemented in a 130 nm SiGe BiCMOS technology. The driver features a 3-tap feed-forward equalizer where positive and negative peaks are added to the main signal to compensate for the low-pass characteristic of VCSELs. The circuit is also able to generate asymmetric pre-emphasis to counteract the VCSEL nonlinearity. Bonded to an 18 GHz VCSEL, the driver can reach an error-free (bit error rate $< 10^{-12}$) optical data rate of 50 Gb/s with an horizontal eye opening better than 0.2 unit interval using a 22 GHz photoreceiver without equalization, retiming, and limiting amplifier at the receiver side. At 48 Gb/s, the horizontal eye opening is 0.5 unit interval. The circuit dissipates only 190 mW from a dual supply of 2.5 and 3.3 V, including the VCSEL power. To the best of the authors' knowledge, this is the fastest common-cathode VCSEL driver with lowest power consumption for data rates higher than 35 Gb/s. Thanks to the active delay line and the application of vertical inductor, the driver is very compact with an active area of only 0.036 mm² including the inductor.

Index Terms—Asymmetric, differentiator, driver, feed-forward equalizer (FFE), integrated circuit, laser, optical transmitter, SiGe BiCMOS, vertical-cavity surface-emitting laser (VCSEL).

I. INTRODUCTION

WITH the constant increase demands of Internet services, the heavy computation is moving into data centers. Nowadays, the majority of data centers use multimode optical fiber (MMF) and vertical-cavity surface-emitting laser (VCSEL) for short reach optical communications due to their low costs compared with the single mode (SM) counterpart [1]. Multimode (MM) VCSEL-based optical communication has several advantages compared with SM: 1) the alignment tolerance of MM optics is an order of magnitude larger compared with SM; 2) in MM VCSEL, optical insulator can be avoided; and 3) packaging costs for MM VCSEL are low and plastic coupling optics can be used [3]. Moreover, in [3], it is shown that in data centers manufactured between January 2012 and December 2015, over 90% of the links are shorter than 100 m. In 2017, switches and server interconnects are expected to adopt a new Ethernet standard consisting of 4 × 50 Gb/s as

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the evolution of the current 802.3bj 100 Gb/s standard that adopts 4 × 25 or 2 × 50 Gb/s.

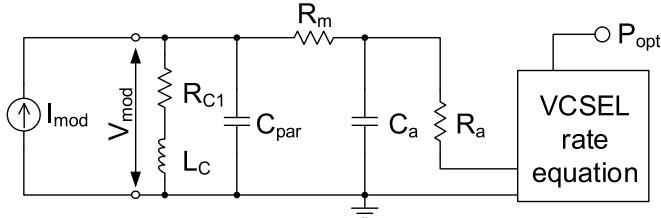
Even though 850 nm VCSEL diodes are continuously evolving reaching a bandwidth of 30 GHz [4], feed-forward equalizers (FFEs) are the main choice to increase the maximum data rate of short-range VCSEL-based optical transmitters [5]–[7]. The drawback of such equalizer is the high power dissipation for data rates higher than 40 Gb/s. A directly modulated cathode-driven VCSEL link with error-free operation [bit error rate (BER) $< 10^{-12}$] at 71 Gb/s is reported in [5] where a 2-tap equalizer is adopted allowing a data rate 2.7 times the VCSEL bandwidth. The drawback of this design is the high power consumption of 950 and 860 mW for the transmitter and the receiver, respectively.

In this paper, a 190 mW 3-tap equalizer capable of 50 Gb/s operation with an 18 GHz VCSEL [8] is presented. As explained in Section II, the main advantage of 3-tap equalizer over the 2-tap counterpart is the control over the jitter. Section III describes the equalizer design and implementation. The measurement setup and the electro-optical measurements are presented in Section IV. Finally, the results are compared with the state-of-the-art in Section V.

II. ASYMMETRIC 3-TAP EQUALIZER

The effectiveness of a 2-tap equalizer in VCSEL drivers is already proven in [6], [7], and [9] and used to reach the world record data rate of 71 Gb/s for a direct NRZ modulated VCSEL [5] when combined with equalization in the receiver. In [5]–[7], one main tap and a postcursor have been used. The equalization is created by subtracting the attenuated and delayed replica of the signal from its own, as in a digital finite impulse response (FIR) filter, while in [9], a peak is added to the signal using a differentiator [10].

Fig. 1 shows the simplified schematic used for the behavioral simulation of the equalizer and the relative parameters. The VCSEL parasitics and rate equations were modeled in [11]. The measurement and simulation of the VCSEL model show an electro-optical bandwidth of approximately 18 GHz. The electrical signal is provided with the modulation current I_{mod} and the relative voltage V_{mod} . Fig. 2 shows four different equalization scenarios for the modulation voltage V_{mod} and the corresponding output optical power P_{opt} . In Fig. 2(a) and (b), the VCSEL is modulated with an OOK signal and no equalization is applied. The optical eye amplitude is the worst of the four cases. The effect of a 2-tap equalizer is reported in Fig. 2(c) and (d) where the eye opening and also the jitter are increased. While the role of the second tap is to decrease



	description	value
I _{mod}	modulation current	4-11 mA
R _{C1}	driver output resistance	55 Ω
L _C	driver peaking inductor	320 pH
C _{par}	driver, VCSEL parasitic cap.	80 fF
R _m	VCSEL mirror resistance	35 Ω
R _a	VCSEL active area res.	50 Ω
C _a	VCSEL active area cap.	160 fF
P _{opt}	VCSEL optical output	2-5 mW

Fig. 1. Simplified schematic used for the behavioral model simulation including the output impedance of the driver, the electrical parasitic of the VCSEL, and the VCSEL rate equations. The dc bias current for the VCSEL is 8 mA.

the turn-ON/OFF time, the third tap decreases the overshoot and the jitter. This scenario can be seen in Fig. 2(e)–(h) where a substantial improvement in the output optical signal is achieved with the 3-tap equalizer.

One characteristic of VCSEL diodes is that the fall time is longer than the rise time [12], [13]. This phenomenon is mainly due to charge storage in the VCSEL and can be mitigated using an asymmetric pre-emphasis that accelerates the charge removal as reported in [12]. This characteristic is also visible in the optical eye diagrams in Fig. 2(f) and (h). Using an asymmetric equalization, the fall time of the VCSEL can be further reduced improving eye opening and jitter. This scenario is confirmed with the simulation. In fact, when the equalizer is asymmetric, the best eye opening and lowest jitter value is achieved as reported in Fig. 2(h).

Fig. 3 shows the comparison between the conventional 3-tap equalizer [Fig. 3(left)] that uses the structure of an FIR filter and the proposed architecture [Fig. 3(right)]. The output signal of a conventional FFE can be written as

$$V_{\text{out}}(n) = \sum_{k=-M}^N C_k V_{\text{in}}(n-k) \quad (1)$$

where M is the number of precursors, N is the number of postursors, C_k are the tap weight coefficients, and $V_{\text{in}}(n)$ is the input signal. In the example of Fig. 3(a), the tap coefficients are $C_0 = 4$, $C_1 = -2$, and $C_2 = 1$. In the proposed structure, as reported in Fig. 3(b), the peaks \tilde{V}_2 and \tilde{V}_3 are added to the signal to create an equalized signal.

One advantage of the proposed structure over the conventional equalizer is the use of only one delay cell instead of two. The delay cell is realized with a cascade of differential amplifiers and consumes 17.5 mW. Employing active delay line is preferable over passive delays because of the small

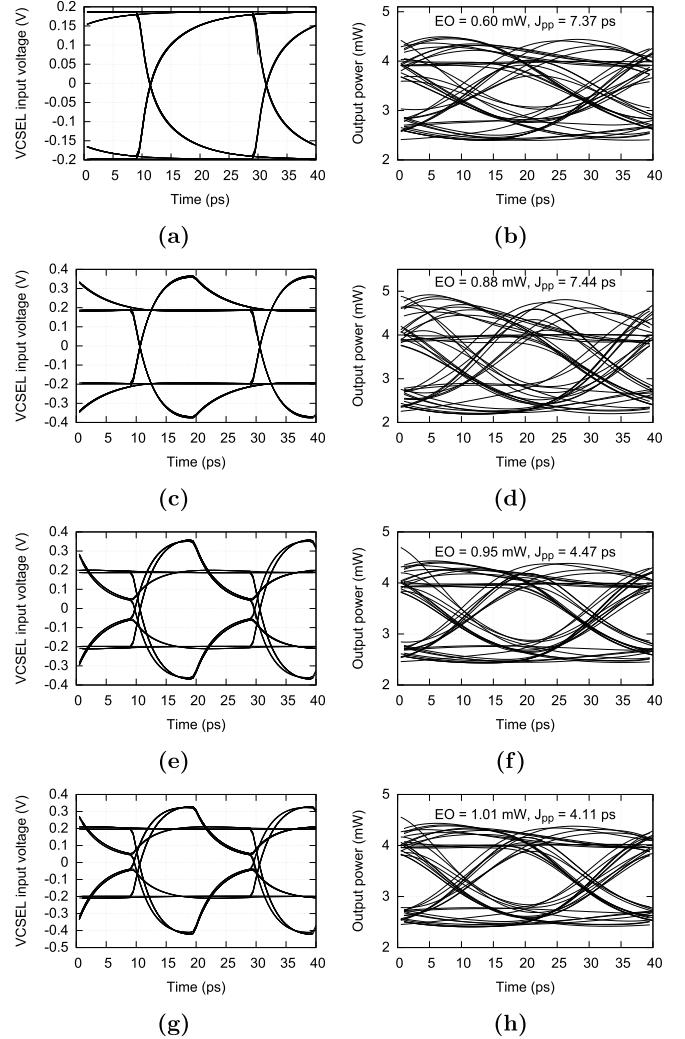


Fig. 2. Behavioral simulation showing the effect of different equalization schemes using an electro-optical VCSEL model. EO stands for eye opening and J_{pp} is the peak-to-peak jitter value. The data rate is 50 Gb/s. (a) VCSEL input voltage without equalization and (b) corresponding output optical power. (c) VCSEL input voltage with symmetric T/2-spaced 2-tap equalizer and (d) corresponding output optical power. (e) VCSEL input voltage with symmetric T/2-spaced 3-tap equalizer and (f) corresponding output optical power. (g) VCSEL input voltage with asymmetric T/2-spaced 3-tap equalizer and (h) corresponding output optical power.

footprint. Compared with the first and second taps, the third tap has a delay of approximately 15 ps.

III. CIRCUIT DESIGN

The block diagram and the power consumption breakdown of the implemented laser driver circuit are depicted in Fig. 4(a) and (b), respectively. The driver has a 100Ω differential input impedance and a single-ended output directly connected to the VCSEL. All the internal signals are differential to allow an easy realization of the peak generator and to increase the immunity to ground and supply nonideality. An input differential limiting amplifier is used to reshape the input signal. This amplifier has an output impedance of 70Ω , necessary because three differential amplifiers are connected to this block leading to 50 fF load capacitance. The asymmetric

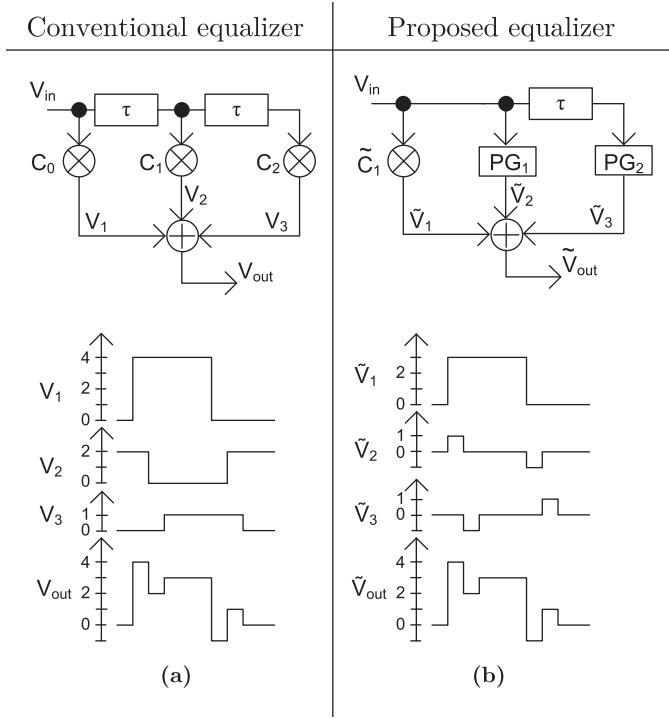


Fig. 3. Block diagram and waveform comparison between a conventional 3-tap equalizer (left) and the proposed structure (right). τ is the delay block and PG stands for peak generator.

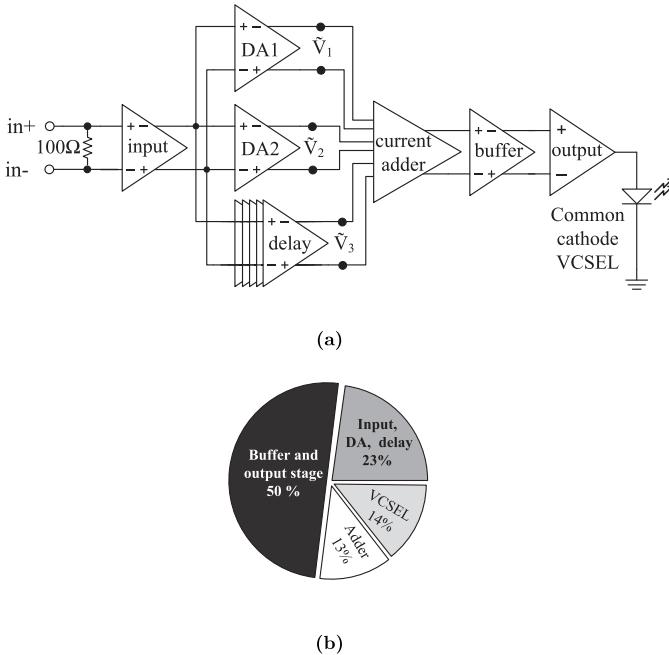


Fig. 4. (a) Block diagram of the proposed 3-tap equalizer circuit. (b) Power consumption breakdown chart. DA stands for differential amplifier.

equalizer is composed of the delay cells and the current adder circuit. A common emitter and an output stage are used to provide the equalized signal to the VCSEL that is connected in a common cathode fashion.

Another advantage of the proposed structure over a conventional equalizer is the asymmetric pre-emphasis generated with

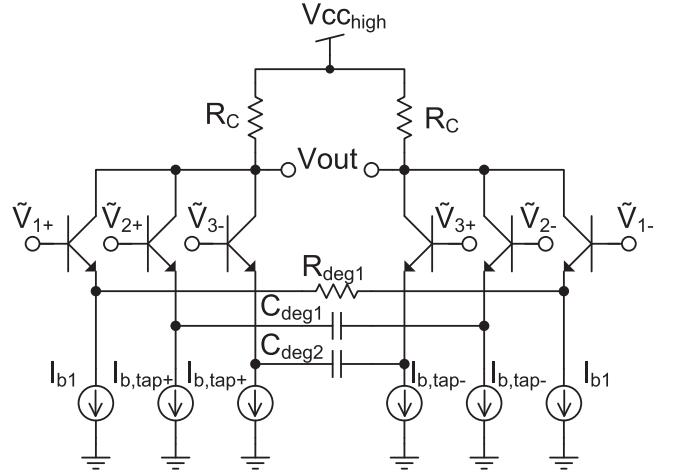


Fig. 5. Schematic of the current adder circuit where the peaks are generated using capacitive degeneration.

unbalanced differentiators. Fig. 5 shows the current adder used for the implementation of the asymmetric pre-emphasis. The adder is a parallel combination of one differential amplifier with resistive degeneration and two differential amplifiers with purely capacitive degeneration, also known as differentiators [10]. To achieve a symmetric eye opening, the differential amplifier with resistive degeneration is balanced. This means that the current I_{b1} in Fig. 5 is the same for the positive and negative sides of the differential pair. In addition, the asymmetric pre-emphasis is generated using independently controlled tail currents for the differentiators. The tail currents $I_{b,tap+}$ and $I_{b,tap-}$ can be set differently creating an asymmetric equalization as shown in Fig. 2(g); 40 % difference between $I_{b,tap+}$ and $I_{b,tap-}$ creates 35 mV dc offset at the output of the adder. The offset propagates to the output stage. The VCSEL, biased close to its power roll-off, is not sensitive to an output dc offset of approximately 50 mV that does not impact the overall performance. The offset can also be canceled out by tuning the bias current I_{out} of the output stage.

The schematics of the emitter follower and the output stage are shown in Fig. 6. The transistors in the output stage are the biggest transistors used in this chip. Together with the buffer, this stage consumes half of the total chip power as shown in the power breakdown in Fig. 4(b). The transistors in the output differential pair lead to 95 fF parasitic capacitance at the nodes X and X' . An emitter follower with transistor transconductance value of 70 mS is used between the peak generator and the output stage. Since the adder has an output impedance of 80 Ω, the low output impedance of the emitter follower shifts the pole at the nodes X and X' from 20 to approximately 100 GHz.

The output stage should have a bandwidth as high as possible to preserve the high-frequency component of the equalized signal. This, together with the fact that the output transistors should provide a peak-to-peak modulation current of 8.5 mA to the VCSEL, is the main challenge in a low-power driver design. Emitter degeneration and inductive peaking are used in the output stage to compensate for the parasitic capacitor

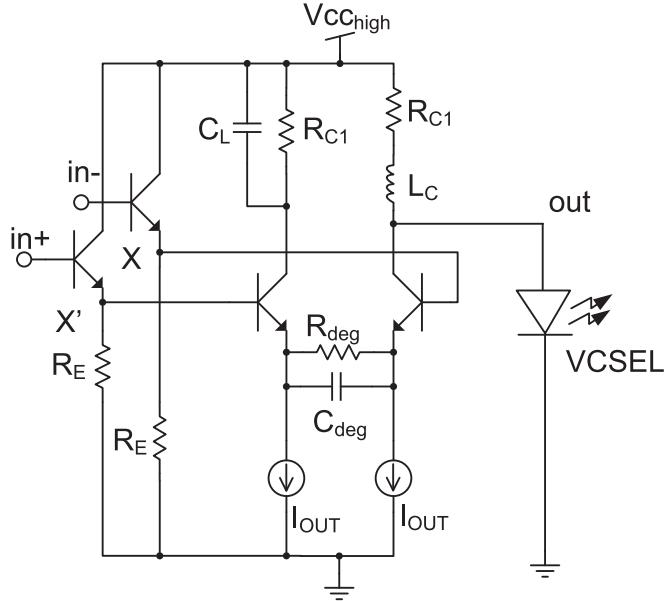


Fig. 6. Schematic of the linear buffer and output circuit.

of the output pad and the VCSEL chip. The resistor R_{deg} also reduces the gain of the output differential pair preventing clipping. Postlayout simulations have shown that the 320 pH vertical inductor L_C increases the bandwidth of the output stage from 44 to 56 GHz. Unlike conventional inductor in vertical inductors, the spiral is oriented perpendicularly to the substrate. Doing so, it is possible to save chip area and to place the active area of the driver as close as possible to the output pad avoiding additional parasitics in the output node. A p-well block is used under the inductor to increase the substrate resistivity and the self-resonance frequency of the inductor. Thanks to the high inductance per unit of area of the vertical inductor, a high self-resonance frequency of 66.5 GHz is achieved. A detailed description of vertical inductors can be found in [14] and [15].

IV. CIRCUIT IMPLEMENTATION AND MEASUREMENT

The circuit is manufactured in IHP 130 nm SiGe BiCMOS technology that offers bipolar n-p-n transistors with f_t/f_{max} of 300/500 GHz, respectively. Fig. 7 shows the chip micrograph and the microscope photograph of the active area. To save power, a 2.5 V supply is used for the input amplifier, delay line, and differential amplifiers DA1 and DA2, while the rest of the circuit is supplied from a 3.3 V source.

On-chip measurements of the eye diagram and BER are carried out using a wafer prober. A 67 GHz GSGSG RF probe is used to provide the differential input signal and the VCSEL light is coupled into a graded index optical fiber with a collimator. An optical attenuator with power meter is employed for the alignment of the collimator to the VCSEL. The optical to electrical conversion is done using a 22 GHz 1484-A-50 New Focus photoreceiver. The bandwidth limitation of the photoreceiver and the frequency-dependent loss of the RF cables are not deembedded and directly deteriorate the measurement results. The bit pattern

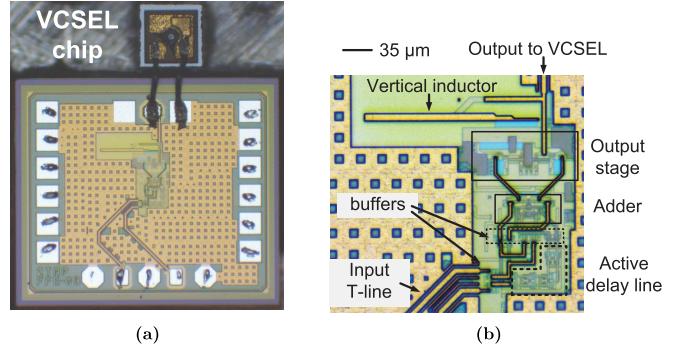


Fig. 7. Microscope photograph of the manufactured chip. (a) Micrograph of the chip wire bonded to the VCSEL. The pads' pitch is 100 μm . (b) Microscope photograph of the active area of the chip.

generator is an SHF12100B and the error analyzer is an SHF11100A. The maximum data rate at which the bit pattern generator and error analyzer are specified is 50 Gb/s, but one can run a back-to-back BER measurement up to 53 Gb/s. The eye diagrams are measured using a 70 GHz Agilent sampling oscilloscope.

A. Electrical Measurement

The electrical eye diagrams are measured on-chip using input and output 67 GHz RF probes. In Fig. 8, the electrical eye diagrams of the circuit in different operation modes are reported. Fig. 8(a)–(c) shows the electrical eye diagram at 20 Gb/s with one, two, and three taps. The equalizer taps can be switched OFF by tuning the bias currents of the differential amplifiers DA1 and DA2 and the delay line. The slight overshoot presented in Fig. 8(a) is due to the emitter degeneration and the vertical inductor used in the output stage. In Fig. 8(d)–(f), the effect of the asymmetric peaking can be seen. This asymmetric peak is obtained by tuning the currents $I_b, \text{tap}+$ and $I_b, \text{tap}-$ separately. With the reference current $I_b, 1$ of the adder circuit, the eye voltage swing can be changed. This scenario is depicted in Fig. 8(d) and (e). The circuit is faster than the measurement equipment and the electrical measurements at 50 Gb/s are reported in Fig. 8(g)–(i). In Fig. 8(g), the equalizer is switched OFF. The large voltage swing scenario with fully asymmetric 2-tap equalizer is shown in Fig. 8(h). Even when the equalizer is fully asymmetric, the performance of the driver does not deteriorate as proved by the open eye diagram in Fig. 8(h). At 50 Gb/s, the driver can still produce the asymmetric 3-tap equalization as shown in Fig. 8(i). It is important to notice that in the measurement of the electrical eye diagrams, the attenuation caused by the limited bandwidth of the RF probes, phase shifters, and the RF cables directly deteriorates the signal quality. Moreover, the impedance of the measurement equipment is 50 Ω while the VCSEL equivalent circuit, as reported for 8 mA bias in Fig. 1, is not 50 Ω .

B. Optical Measurement

The optical measurements are performed using a wafer prober and a collimator to couple the VCSEL light into

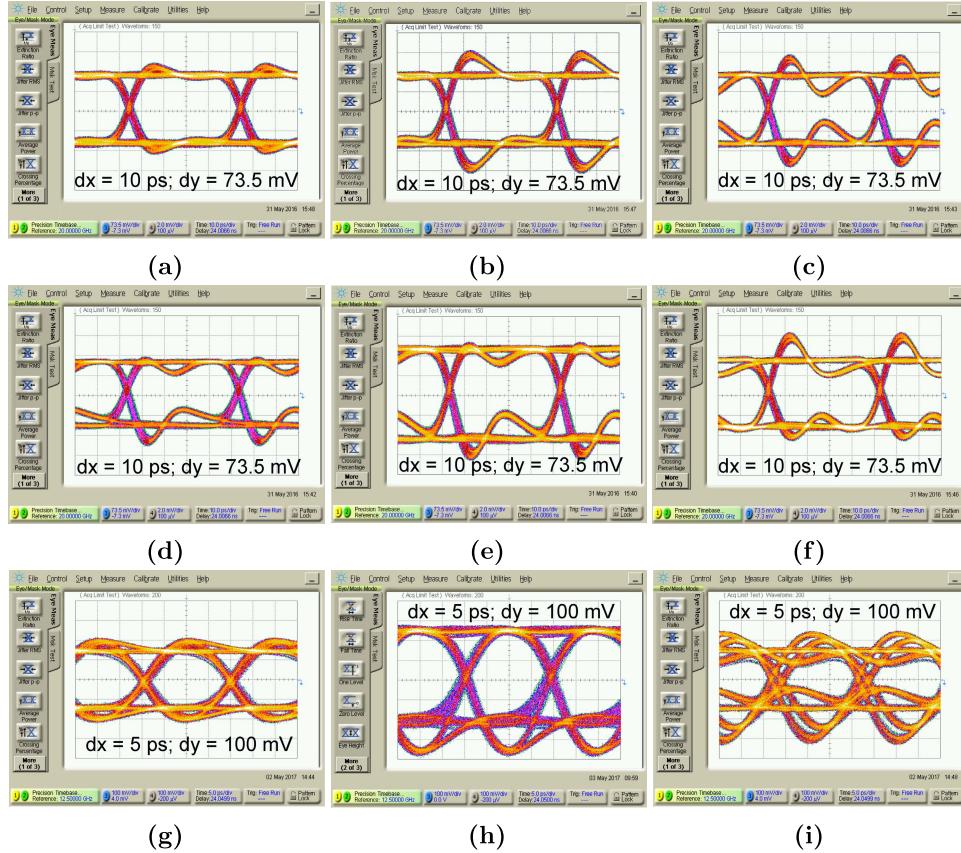


Fig. 8. Electrical eye diagrams. (a) 20 Gb/s, one-tap. (b) 20 Gb/s, 2-tap. (c) 20 Gb/s, 3-tap. (d) 20 Gb/s, 3-tap bottom asymmetric equalization. (e) 20 Gb/s, 3-tap bottom asymmetric equalization with large voltage swing. (f) 20 Gb/s, 3-tap top asymmetric equalization. (g) 50 Gb/s, one-tap. (h) 50 Gb/s, 2-tap bottom fully asymmetric equalization. (i) 50 Gb/s, bottom asymmetric 3-tap equalization.

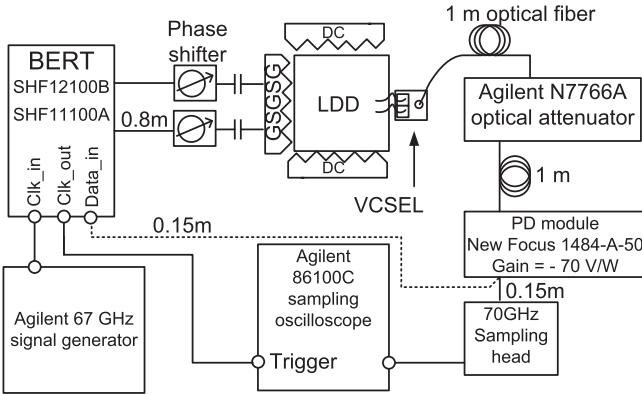


Fig. 9. Block diagram of the optical measurement setup. Please note the negative conversion gain of the photodetector that results in inverted optical eye diagrams.

a 2 m graded index MMF. All measurements are performed at room temperature. The block diagram of the electro-optical measurement setup is reported in Fig. 9. The dashed line is connected only for the BER measurement instead of the oscilloscope. It is important to note that the negative conversion gain of the photodiode module of -70 V/W leads to inverted optical eye diagrams. As in the simulation, for the electro-optical measurements, the VCSEL is biased at 8 mA, close

to its power roll-off. Biasing the VCSEL at higher currents would decrease the optical modulation amplitude (OMA) and lowering the bias current would make the VCSEL slower. At 50 Gb/s with the asymmetric equalization, the OMA is approximately 0.7 dBm.

The optical eye diagrams showing the effect of the equalization at 50 Gb/s are depicted in Fig. 10(b)–(i). The first eye diagram in Fig. 10(a) is obtained by driving the VCSEL directly with the pseudorandom bit sequence (PRBS) generator at 45 Gb/s without using the driver circuit. The VCSEL input electrical eye at 45 Gb/s is also shown in Fig. 10(a). When the equalization is turned off, the driver still provides a weak peak due to the inductance and emitter degeneration in the output stage. The effect of this peak can be seen in Fig. 10(b) where the eye opening improves compared with Fig. 10(a) at a cost of a slight jitter. A better eye opening is achieved using the 2-tap equalizer setting. In Fig. 10(c), the equalization is symmetric and produces high value of jitter and a large overshoot. The overshoot can be reduced using the asymmetric 2-tap equalizer as presented in Fig. 10(d). In Fig. 10(d), the smaller eye opening results from a longer turn-ON time of the VCSEL since the equalizer is fully asymmetric. In a 3-tap equalizer, the role of the third tap is to reduce the jitter and the overshoot. This is confirmed by the measurement reported in Fig. 10(e)–(i) where the quality of the optical eye diagram drastically improves with the addition of the

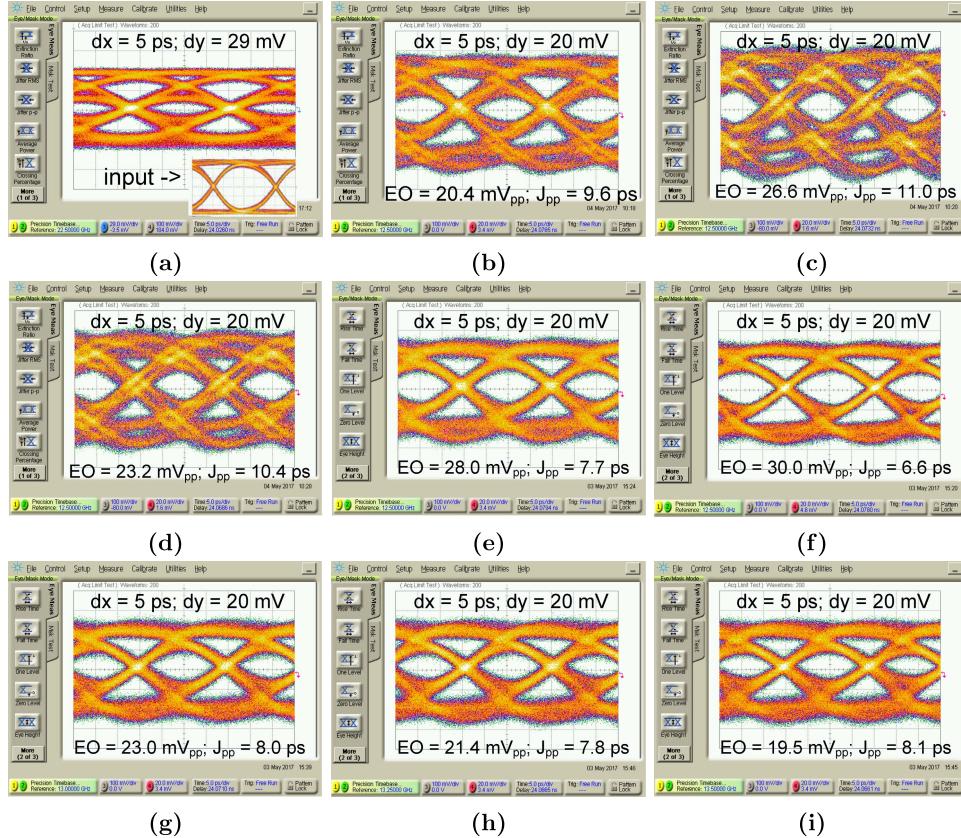


Fig. 10. Optical measurements showing the effect of the equalization. The eye diagrams are inverted because of the negative gain of the Newport 1484-A-50 photoreceiver. (a) Reference eye without equalization at 45 Gb/s obtained driving the VCSEL with the PRBS generator. (b) Weak 2-tap equalization at 50 Gb/s. (c) Strong symmetric 2-tap equalization at 50 Gb/s. (d) Strong fully asymmetric 2-tap equalization at 50 Gb/s. (e) Symmetric 3-tap equalization at 50 Gb/s. (f) Asymmetric 3-tap equalization at 50 Gb/s. (g) Asymmetric 3-tap equalization at 52 Gb/s. (h) Asymmetric 3-tap equalization at 53 Gb/s. (i) Asymmetric 3-tap equalization at 54 Gb/s. EO is the eye opening at the photodetector output and J_{pp} is the peak-to-peak jitter value.

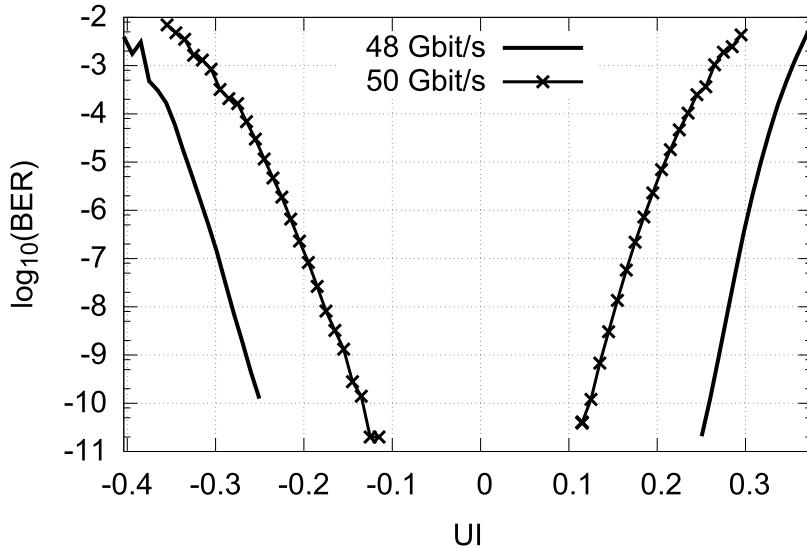


Fig. 11. BER test at 48 and 50 Gb/s with $2^7 - 1$ PRBS length. One UI represents the bit period for a given data rate.

third tap. The asymmetric equalizer also helps to improve eye opening and jitter compared with a symmetric equalization as shown in Fig. 10(e) and (f). These eyes are obtained with identical modulation and biasing parameters for the driver; the

only difference is that in Fig. 10(e) the currents $I_{b,tap+}$ and $I_{b,tap-}$ are equal (1 mA) while in Fig. 10(f) are different (0.8/1.2 mA). These results are in line with the simulation performed in Section II. The eye diagrams with

TABLE I
STATE-OF-THE-ART COMPARISON

Ref.	[16]	[17]	[18]	[19]	[9]†	this work	[5]
Technology	90 nm	65 nm	32 nm	130 nm	130 nm	130 nm	130 nm
	CMOS	CMOS	SOI	SiGe	SiGe	SiGe	SiGe
DR (Gbit/s)	25	26	35	40	48	50	71
FOM (mW/Gbit) s	2.4	1.8	1.3	7.8	3.9	3.8	13.4
Supply voltage (V)	1.2/2.65	1.0/3.0	1.1/3.09	2.5/3.3	2.5/3.4	2.5/3.3	4
OMA (dBm)	n.r.	0.82	1.5	2.3	2	0.7	n.r.*
VCSEL $f_{-3\text{dB}}$ (GHz)	11	16	16	16	20	18	26
Driver type	CC	CC	CA	CC	CC	CC	CA
Equalizer type	none	deg	none	GD eq	deg + ind	3-tap FFE	2-tap FFE

† = error free operation up to 46 Gbit/s, * = error-free eye opening OMA = 0.1 dBm, CA = common anode VCSEL driver, CC = common cathode, deg = emitter degeneration, GD eq = group delay equalization, ind = inductive peaking

asymmetric equalization at 52, 53, and 54 Gb/s are also shown in Fig. 10(g)–(i). The optical eye is still open at 54 Gb/s under the following conditions.

- 1) The measured VCSEL bandwidth is approximately 18 GHz.
- 2) The photodetector bandwidth is 22 GHz.
- 3) There is no reshaping or equalization present in the optical receiver. Furthermore, there are no limiting amplifiers, flip-flops, or data recovery present.
- 4) The PRBS generator and BER tester (BERT) are specified for 50 Gb/s and can work error free only until 53 Gb/s in back-to-back connection.

Another challenge is in the BER measurement. The BERT requires a minimum eye opening of 16 mV_{pp} at 50 Gb/s for a BER < 10⁻⁹. Due to the limited bandwidth of the photodetector and the absence of a limiting amplifier in the receiver, the electrical signals after the PD module are very close to the BERT input sensitivity limiting the maximum error-free (BER < 10⁻¹²) data rate to 50 Gb/s. At 50 Gb/s, a horizontal eye opening better than 0.2 unit interval (UI) was achieved using a 2⁷ – 1 bit stream. At higher data rates, it was not possible to synchronize the BERT with the PRBS generator. The bathtub tests at 48 and 50 Gb/s are shown in Fig. 11. The maximum error-free operation rate of the VCSEL directly driven by the PRBS generator (without using the driver chip and with the same receiver setup) was only up to 40 Gb/s.

V. CONCLUSION

In this paper, the design of a 190 mW VCSEL driver with 3-tap FFE is presented. The equalizer is implemented in a 130 nm SiGe BiCMOS technology. The driver features an asymmetric equalization to compensate for the different turn-on/off times of VCSELs. The effect of the equalization is shown to be beneficial by increasing the maximum error-free

data rate by 20%. An error-free 50 Gb/s optical transmission is achieved consuming only 190 mW of power including that of the VCSEL (\approx 20 mW). The estimated OMA at the receiver is 0.7 dBm. The equalizer extended the error-free operation from 40 to 50 Gb/s. At higher speed, the VCSEL and photodetector bandwidth as well as the BERT sensitivity limited the measurement of the maximum data rate.

Table I shows a comparison with state-of-the-art VCSEL drivers. To the best of the authors' knowledge, this work is the most energy-efficient VCSEL driver for data rates higher than 35 Gb/s. The results in [5] showed 71 Gb/s transmission using equalization in both the transmitter and the receiver. In this paper, no equalization was used at the receiver side and compared with [5] and the power consumption of the transmitter is 3.6 times smaller. Moreover, in [5], the VCSEL is cathode driven and has a bandwidth of 26 GHz, which is 44% higher than the VCSEL used in this paper.

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