

# A Subthreshold Voltage Reference With Scalable Output Voltage for Low-Power IoT Systems

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**Abstract**—This paper presents a subthreshold voltage reference in which the output voltage is scalable depending on the number of stacked PMOS transistors. A key advantage is that its output voltage can be higher than that obtained with conventional low-power subthreshold voltage references. The proposed reference uses native NMOS transistors as a current source and develops a reference voltage by stacking one or more PMOS transistors. The temperature coefficient of the reference voltage is compensated by setting the size ratio of the native NMOS and stacked PMOS transistors to cancel temperature dependence of transistor threshold voltage and thermal voltage. Also, the transistor size is determined considering the trade-off between diode current between n-well and p-sub and process variation. Prototype chips are fabricated in a 0.18- $\mu\text{m}$  CMOS process. Measurement results from three wafers show  $3\sigma$  inaccuracy of  $\pm 1.0\%$  from 0  $^{\circ}\text{C}$  to 100  $^{\circ}\text{C}$  after a single room-temperature trim. The proposed voltage reference achieves a line sensitivity of 0.31%/V and a power supply rejection of  $-41$  dB while consuming 35 pW from 1.4 V at room temperature.

**Index Terms**—Internet of things (IoT), low power, subthreshold, voltage reference.

## I. INTRODUCTION

A low-power Internet-of-things (IoT) system requires low-power building blocks to extend system lifetime or reduce battery size. A voltage reference is typically always turned on and contributes to standby power consumption. Thus, it should be designed within stringent standby power constraints to ensure a long system lifetime.

Bandgap voltage references [1]–[7] are the most common type of voltage reference, but they are not acceptable in ultra-low-power sensing systems (e.g., 8-nW standby power [8]) due to their high power consumption (3 nW [1], 29 nW [2], 32 nW [3]). In contrast, subthreshold voltage references [9]–[17] have lower power consumption (2.6 nW [9], 2.2 pW [17]). The picowatt power consumption [17] is achieved using the difference of two transistor threshold voltages ( $V_{th}$ ) [13]–[17]. However, their output voltages can be quite low (e.g.,  $\sim 0.2$  V [17]). If this low voltage sets the operating voltage of analog blocks, it can significantly limit their dynamic range compared with the supply voltage (e.g., 3.8 V for a lithium battery operating system). A higher reference voltage ( $V_{REF}$ ) can be obtained with an analog

voltage multiplier using an amplifier and resistors, but they can dwarf the power of the voltage reference itself. Thus, a new low-power voltage reference with a high  $V_{REF}$  is desirable for battery-operated systems.

This paper proposes a subthreshold voltage reference in which  $V_{REF}$  is similar to that of bandgap voltage references ( $\sim 1.2$  V). This higher  $V_{REF}$  than in conventional subthreshold voltage references is the result of stacking four PMOS transistors and can be raised further by increasing the number of stacked transistors. We discuss the proposed voltage reference [18] in detail in this paper, including measurement results obtained using a newly fabricated design across multiple wafers. The prototype voltage reference is implemented in a standard 0.18- $\mu\text{m}$  CMOS process, and measurement results show  $3\sigma$  inaccuracy of  $\pm 1.0\%$  from 0  $^{\circ}\text{C}$  to 100  $^{\circ}\text{C}$  after a single temperature trim while consuming 35 pW from a 1.4 V supply at room temperature. The proposed subthreshold voltage reference shows limited noise performance (24.4  $\mu\text{V}$  from 0.1 to 10 Hz) compared with conventional bandgap voltage references (6.1  $\mu\text{V}$  [4] and 9.1  $\mu\text{V}$  [7] from 0.1 to 10 Hz). Hence, such low-noise but high-power references might still be required to perform noise-critical operations. However, the proposed circuit can continually run and support other operations with less strict noise requirements without increasing the total system power significantly in low-power IoT systems.

This paper is organized as follows: Section II presents the proposed voltage reference, Section III discusses its circuit design, and Section IV reports the test chip measurement results. Finally, Section V concludes this paper.

## II. PROPOSED VOLTAGE REFERENCE

Fig. 1 shows the proposed circuit with four stacked PMOS transistors. It consists of top PMOS transistors ( $M_{CX}$ ) with high  $V_{th}$  ( $\sim 0.7$  V), zero- $V_{th}$  NMOS transistors ( $M_{NX}$ ), and stacked high- $V_{th}$  PMOS transistors at the bottom ( $M_{PX}$ ). The zero- $V_{th}$  NMOS transistors are native NMOS devices that are typically available in modern process technologies [19], [20]. Standard NMOS devices can be used, but the output voltage is reduced due to a lower  $V_{th}$  difference.  $M_{NX}$  serves as the current provider and transistors  $M_{CX}$  function as digital switches to control the amount of the current and trim the reference temperature coefficient (TC). In different branches, the size ratio between  $M_{CX}$  and  $M_{NX}$  is maintained to obtain the same leakage current through  $M_{CX}$  per unit transistor width of  $M_{NX}$ .

$M_{NX}$  and  $M_{PX}$  operate in the subthreshold region, and their drain current can be expressed as follows [21]:

$$I_d = \mu C_{OX} \frac{W}{L} (m-1) V_T^2 e^{\left(\frac{V_{gs}-V_{th}}{mV_T}\right)} \left(1 - e^{-\frac{V_{ds}}{V_T}}\right) \quad (1)$$

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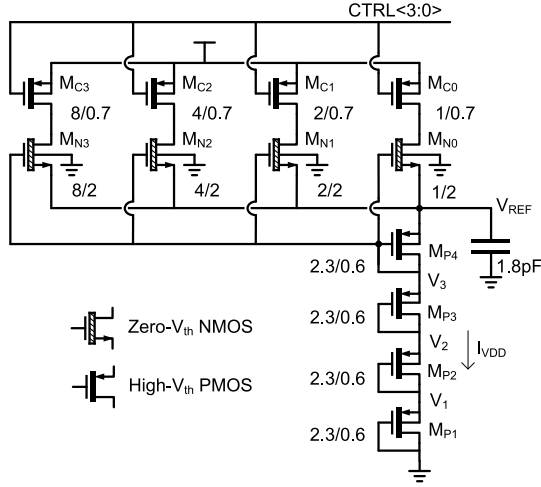
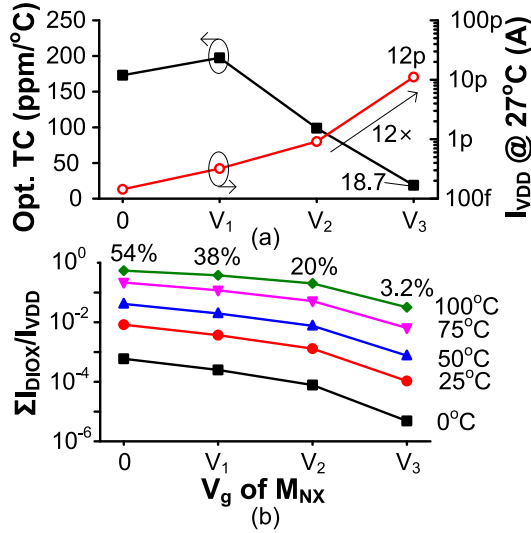


Fig. 1. Circuit diagram of the proposed voltage reference.

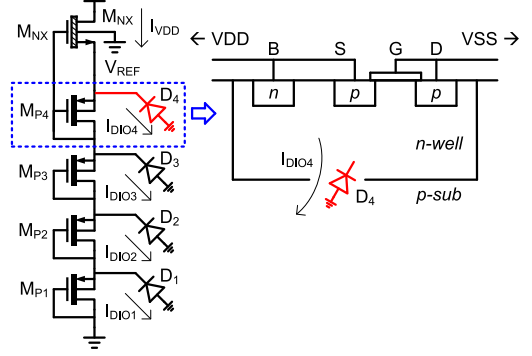
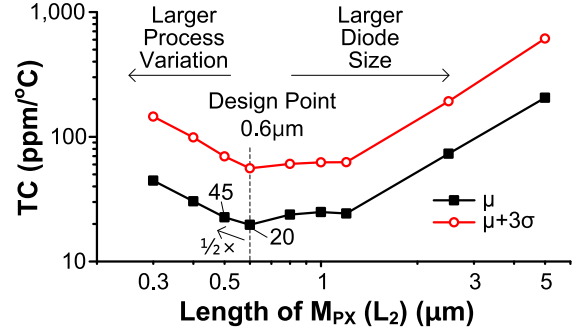
Fig. 2. Simulated TC,  $I_{VDD}$ , and  $\Sigma I_{DIOX}/I_{VDD}$  with different gate connection. (a) TC and  $I_{VDD}$ . (b)  $\Sigma I_{DIOX}/I_{VDD}$  with different temperatures.

where  $\mu$  is mobility,  $C_{ox}$  is oxide capacitance,  $W$  and  $L$  are transistor size,  $m$  is subthreshold slope factor, and  $V_T$  is the thermal voltage. Since the same current flows through turned-on  $M_{NX}$  and each  $M_{PX}$ , the following equation can be obtained assuming all of the  $M_{PX}$  transistors are identical:

$$I = \mu_1 C_{ox1} \frac{W_1}{L_1} (m_1 - 1) V_T^2 e^{\left(\frac{-V_{REF}/N - V_{th1}}{m_1 V_T}\right)} = \mu_2 C_{ox2} \frac{W_2}{L_2} (m_2 - 1) V_T^2 e^{\left(\frac{V_{REF}/N - |V_{th2}|}{m_2 V_T}\right)}. \quad (2)$$

Here  $N$  is the number of  $M_{PX}$ .  $W_1$  is the sum of the width of  $M_{NX}$  connected to supply voltage by  $M_{CX}$ .  $L_1$  is the length of  $M_{NX}$ .  $W_2$  and  $L_2$  are  $M_{PX}$  size. The factor "1-exp(- $V_{ds}/V_T$ )" in (1) can be ignored since the error is negligible for  $V_{ds} > 150$  mV (0.3% error). Since the body of  $M_{NX}$  is connected to ground and its drain is connected to  $V_{REF}$ , the body effect should be considered for  $V_{th1}$  as follows [21]:

$$V_{th1} = V_{th1.0} + \gamma \sqrt{2\phi_f + V_{REF}} - \gamma \sqrt{2\phi_f}. \quad (3)$$

Fig. 3. Diodes between  $n$ -well and  $p$ -sub in the proposed voltage reference.Fig. 4. TC across  $L_2$  from 1 k-sample MC simulations.

$V_{th1.0}$ ,  $\gamma$ , and  $\phi_f$  are the threshold voltage without the body effect, the body effect coefficient, and the difference between the Fermi potential and the intrinsic potential, respectively. The body effect shifts  $V_{REF}$  by 12% by changing  $V_{th1}$  by 8.8 mV in simulation.

From (2),  $V_{REF}$  can be obtained as follows:

$$V_{REF} = N \left\{ \left( \frac{m_1 |V_{th2}| - m_2 V_{th1}}{m_1 + m_2} \right) + \left( \frac{m_1 m_2 V_T}{m_1 + m_2} \right) \ln \left( \frac{\mu_1 C_{ox1} \frac{W_1}{L_1} (m_1 - 1)}{\mu_2 C_{ox2} \frac{W_2}{L_2} (m_2 - 1)} \right) \right\}. \quad (4)$$

To simplify the solution,  $V_{th1}$  is first calculated using the target value of  $V_{REF}$  for computing and including the body effect. A 100 mV estimation error of the body voltage results in only a 1% difference in  $V_{REF}$  by changing  $V_{th1}$  by 0.2 mV in simulation.

$V_{th}$  is complementary to absolute temperature [21]. However, the first term can be proportional or complementary depending on  $m_1$  and  $m_2$ . Also,  $V_T$  in the second term is proportional to temperature. However, the temperature coefficient of the second term can be also changed by transistor sizing of  $(W_1/L_1)$  and  $(W_2/L_2)$  in the log function. To achieve a low TC of  $V_{REF}$ , the temperature coefficient of the first term which is dictated by process technology can be cancelled by the second term through proper transistor sizing. By setting  $dV_{REF}/dT = 0$ , the optimal transistor size can be found to minimize TC.

$$\left( \frac{W_1/L_1}{W_2/L_2} \right)_{\text{optimal}} = \frac{\mu_2 C_{ox2} (m_2 - 1)}{\mu_1 C_{ox1} (m_1 - 1)} e^{\frac{q}{k} \left( \frac{1}{m_1} \cdot \frac{dV_{th1}}{dT} - \frac{1}{m_2} \cdot \frac{d|V_{th2}|}{dT} \right)} \quad (5)$$

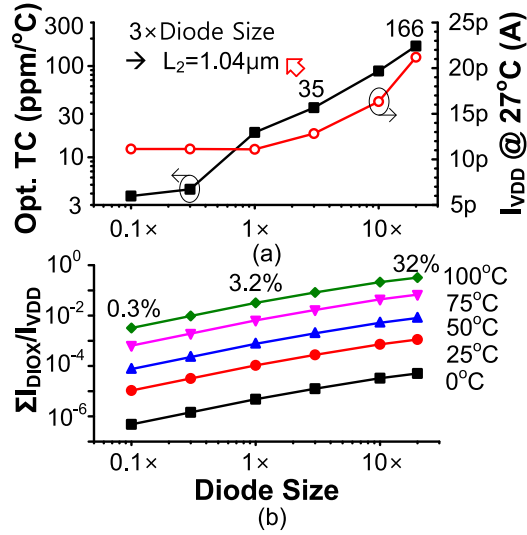


Fig. 5. Simulated  $\Sigma I_{DIOX}/I_{VDD}$  at different temperatures across diode sizes (1x is the design point).

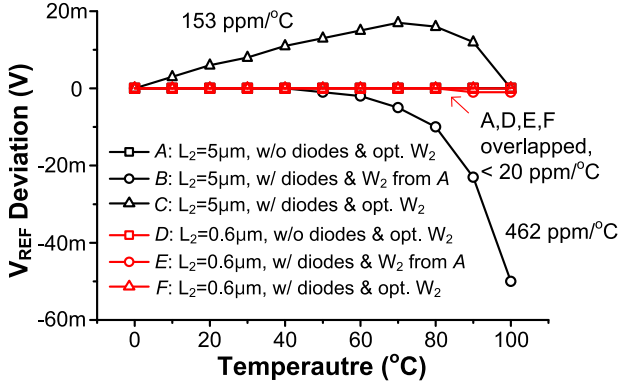


Fig. 6. Simulated impact of the diode current on TC.

where  $k$  is Boltzmann's constant and  $q$  is the elementary charge. The transistor size ratio is set to 0.52 based on calculation and simulation, considering the second-order temperature dependence of  $V_{th}$  and the temperature dependence of  $\mu$  and  $m$ . In measurement, the average TC of 22.5 ppm/°C from 0 °C to 100 °C is achieved, which is comparable with that of other state-of-the-art voltage references. In the voltage reference with TC of 22.2 ppm/°C, the second-order effect degrades the TC by 70.3% while deviation from the optimal transistor sizing due to process variation contributes to the TC with 29.7%.

### III. CIRCUIT DESIGN

In Fig. 1, the bias current of  $M_{PX}$  ( $I_{VDD}$ ) mainly depends on the gate voltage of  $M_{NX}$ . As shown in Fig. 2(a), when the gate of  $M_{NX}$  is connected to  $V_3$  we achieve an optimal TC which is lower than 50 ppm/°C (which is a competitive value with other state-of-the-art voltage references). It sets  $I_{VDD}$  to 12 pA in simulation with transistor size requirement for TC optimization. If the gate is connected to  $V_2$ ,  $V_1$ , or ground,  $I_{VDD}$  can be lowered, but it results in TC degradation. This is because the ratio of current through diodes between  $n$ -well

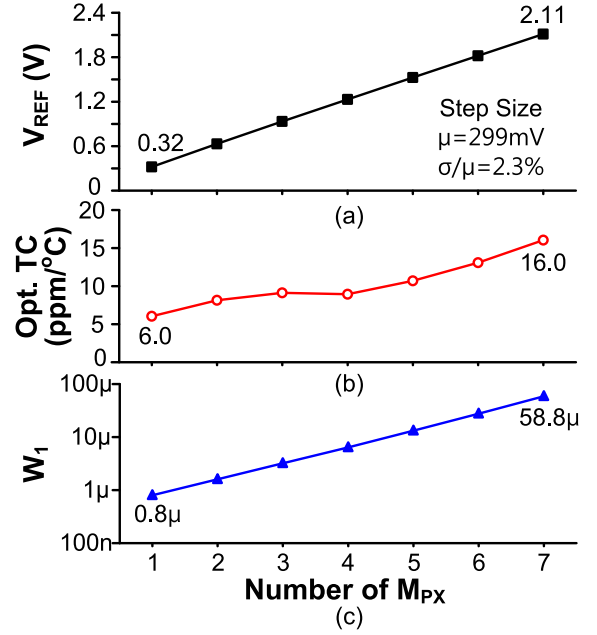


Fig. 7. Simulated  $V_{REF}$ , TC, and used  $W_1$  across the number of  $M_{PX}$ . (a)  $V_{REF}$ , (b) TC, (c)  $W_1$ .

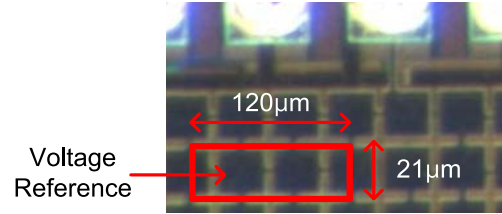


Fig. 8. Die photograph of the fabricated voltage reference.

and  $p$ -sub ( $I_{DIOX}$  in Fig. 3) to  $I_{VDD}$  becomes larger. As shown in Fig. 2(a), compared with the gate connected to the other nodes, the gate connected to  $V_3$  provides  $>12\times$  larger  $I_{VDD}$ . In Fig. 2(b), it keeps  $\Sigma I_{DIOX}/I_{VDD}$  less than 3.2% and helps achieve TC less than 50 ppm/°C. The constant 3.2% of  $\Sigma I_{DIOX}/I_{VDD}$  across temperatures results in TC of 1.2 ppm/°C in simulation. It shows that the exponential increase of  $\Sigma I_{DIOX}/I_{VDD}$  is the reason for the TC degradation.

$D_X$  (Fig. 3) pulls down relatively more current from the internal node at higher temperature and worsens the curvature of  $V_{REF}$ . The increased  $\Sigma I_{DIOX}/I_{VDD}$  can be explained with the diode current equation as follows [22]:

$$I_{DIO} = I_S \left( 1 - e^{-\frac{V_D}{V_T}} \right) \approx I_S = qA \left( \sqrt{\frac{D_P}{\tau_p}} \frac{n_i^2}{N_D} + \sqrt{\frac{D_N}{\tau_n}} \frac{n_i^2}{N_A} \right) \propto n_i^2. \quad (6)$$

$V_D$  is the voltage across the diode,  $A$  is the cross-sectional area,  $D_P$  is the diffusion coefficient of holes,  $D_N$  is the diffusion coefficient of electrons,  $N_D$  is the  $n$ -well donor concentrations,  $N_A$  is the  $p$ + acceptor concentrations,  $n_i$  is the intrinsic carrier concentration,  $\tau_p$  is the carrier lifetimes of holes, and  $\tau_n$  is the carrier lifetimes of electrons. Note that the diodes are reversely biased. In Fig. 3,  $V_D$  across  $D_1 - D_4$  is larger than 250 mV, and the factor “ $1 - \exp(-$

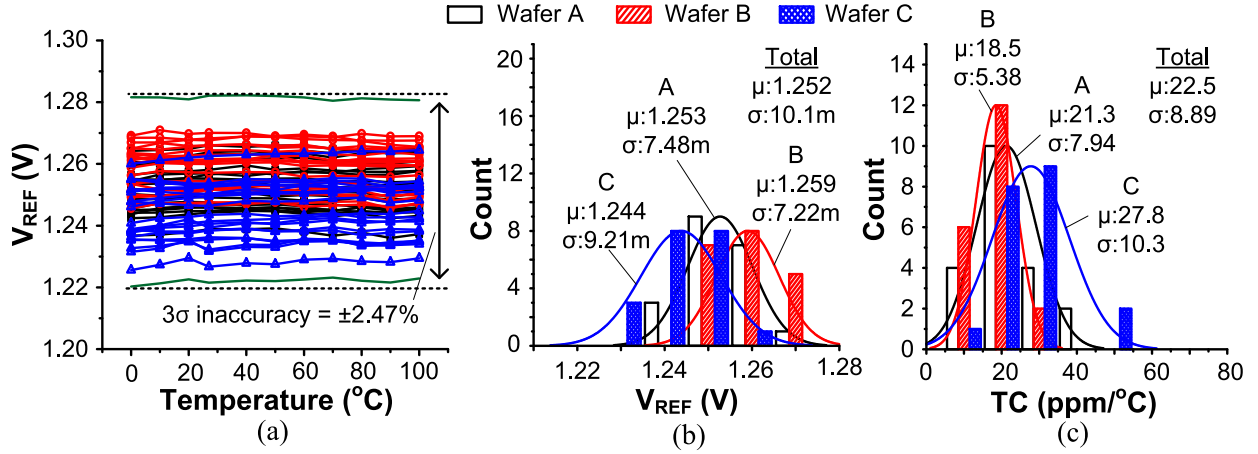


Fig. 9. Measured voltage reference without trimming. (a)  $V_{REF}$  across temperatures., (b) Distribution of  $V_{REF}$ , (c) Distribution of TC.

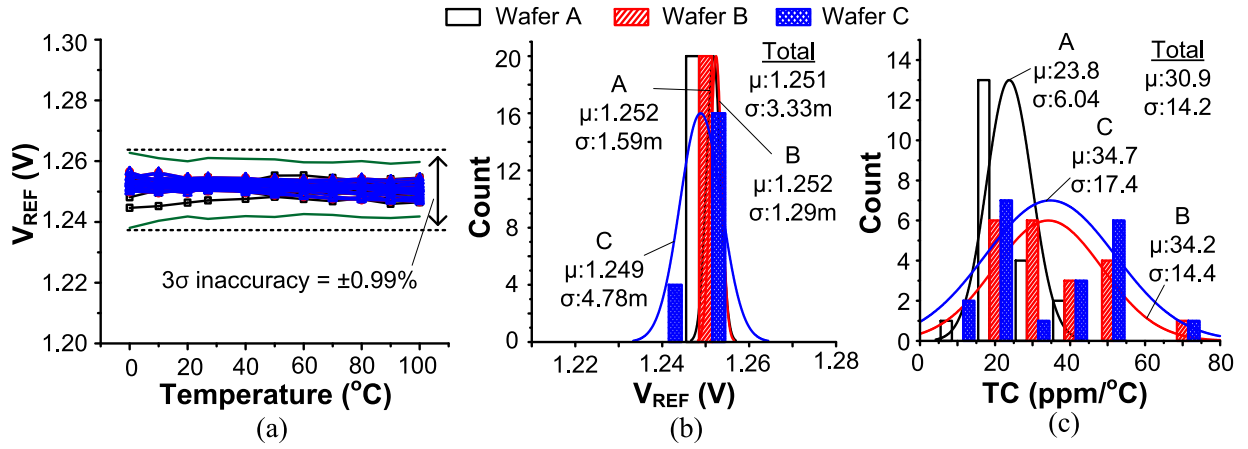


Fig. 10. Measured voltage reference after room-temperature trim. (a)  $V_{REF}$  across temperatures., (b) Distribution of  $V_{REF}$ , (c) Distribution of TC.

$V_D/V_T$  in (6) can be ignored since the error is negligible for  $V_D > 150$  mV (0.3% error). Thus,  $I_{DIO}$  is to the first order independent of  $V_D$  and  $I_{DIO} = I_{DIO4} = I_{DIO3} = I_{DIO2} = I_{DIO1}$ . The stronger temperature dependence of  $I_{DIO}$  than  $I_{VDD}$  comes from  $n_1^2$  proportional to  $\exp(-E_g/kT)$ .  $E_g$  is the silicon bandgap. In simulation,  $\Sigma I_{DIOX}$  is increased by 5–22 $\times$  more per 25  $^{\circ}$ C compared with  $I_{VDD}$  [the subthreshold current in (2)].

Four high- $V_{th}$  PMOS transistors are used to match the output voltage level to that of the bandgap voltage references ( $\sim 1.2$  V). Length of  $M_{PX}$  ( $L_2$ ) is set to 0.6  $\mu$ m considering a trade-off between process variation and the size of diodes shown in Fig. 4.  $W_2$  is changed according to  $L_2$  to maintain  $W_2/L_2$ . Variation on  $V_{th}$  of  $M_{PX}$  is inversely proportional to  $W_2 \times L_2$  [23]. This variation causes the transistor size to deviate from the optimal value. 2 $\times$  shorter  $L_2$  increases the average TC from 19.7 to 44.5 ppm/ $^{\circ}$ C. On the other hand, larger  $W_2$  and  $L_2$  increase the diode size of  $D_X$  (Fig. 3) and degrades TC. As shown in Fig. 5, larger diodes increase  $\Sigma I_{DIOX}/I_{VDD}$  and exacerbate TC. For TC less than 35 ppm/ $^{\circ}$ C,  $L_2$  needs to be smaller than 1.04  $\mu$ m.

As shown in Fig. 6, without considering  $I_{DIOX}$ ,  $L_2$  can be set to long value (e.g., 5  $\mu$ m) just for low-process variation,

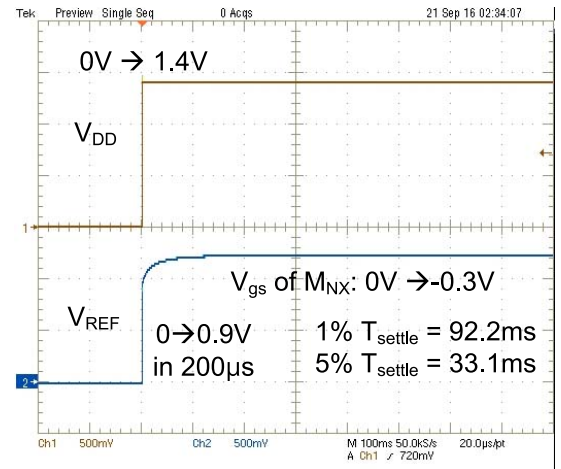


Fig. 11. Measured start-up waveform of  $V_{REF}$ .

and the reference achieves a TC of 2.0 ppm/ $^{\circ}$ C (simulation) with the optimal  $W_2$  (26.5  $\mu$ , curve A). However, considering  $I_{DIOX}$ ,  $V_{REF}$  is reduced at higher temperatures, increasing TC by 231 $\times$  (curve B). By reducing the  $W_2$  to 5.1  $\mu$ m,

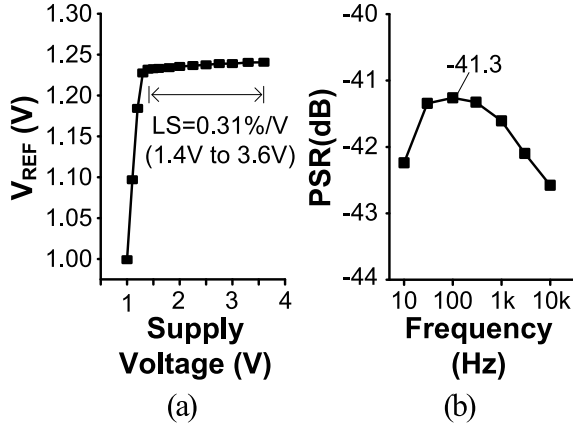


Fig. 12. Measured supply voltage dependence. (a) LS. (b) PSR.

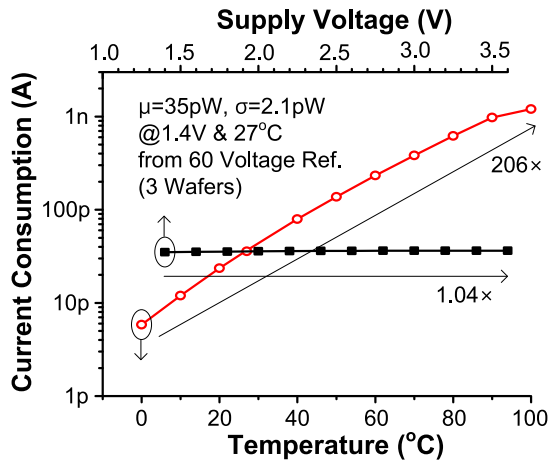


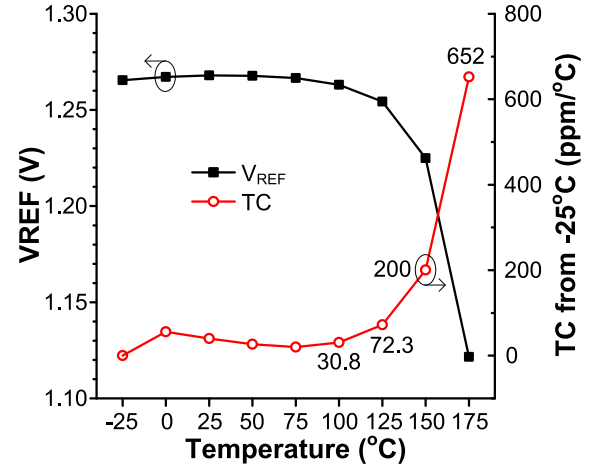
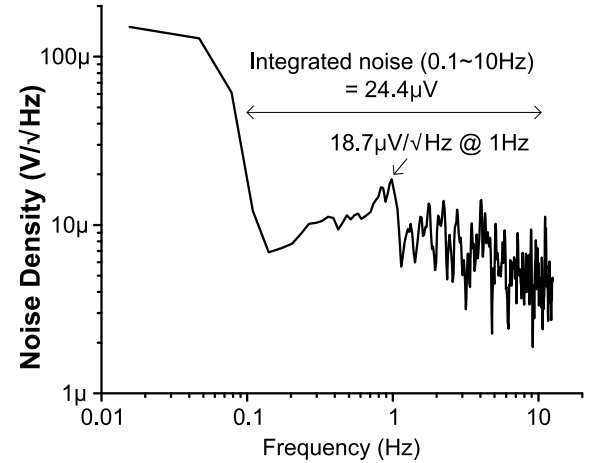
Fig. 13. Measured current consumption across supply voltages and temperatures.

TC can be lowered to 153 ppm/°C (curve C). Here, the diode size is equivalent to  $18.5\times$  the diode size in Fig. 5(a) and  $\Sigma I_{DIOX}/I_{VDD}$  is  $\sim 30\%$  at 100 °C. Although TC is improved by  $3\times$  with a narrower  $W_2$ , it is  $77\times$  worse than that achieved without considering  $I_{DIOX}$ . When  $0.6\ \mu\text{m}$  is selected for  $L_2$ , the difference in TCs is only  $2.2\times$ . The proposed circuit achieves TC of 18.7 ppm/°C in simulation with the optimal transistor length ( $L_2$ ) chosen by understanding the trade-off between process variation and TC.

Fig. 7 shows the scalable output voltage of the proposed circuit. In simulation,  $V_{REF}$  can be varied from 0.32 to 2.11 V by stacking different number of  $M_{PX}$  while maintaining TC  $< 20$  ppm/°C. Due to the body effect, higher  $V_{REF}$  requires wider  $W_1$  to maintain the supply current (13.6 – 22.0 pA). Within  $W_1$  of  $59\ \mu\text{m}$ , the circuit can provide seven different voltages up to half the level of thin-film Li battery voltage (3.6–4.2V), typically the most important reference voltage.  $V_{REF}$  is linearly increased with the number of  $M_{PX}$ . The voltage step size has a mean ( $\mu$ ) of 299 mV and sigma over mean ( $\sigma/\mu$ ) of 2.3%.

#### IV. MEASUREMENT RESULTS

The proposed voltage reference is fabricated in a 180-nm CMOS technology (Fig. 8). The area is  $120\ \mu\text{m} \times 21\ \mu\text{m}$

Fig. 14. Measured  $V_{REF}$  and TC from  $-25\ ^\circ\text{C}$  to  $175\ ^\circ\text{C}$ .Fig. 15. Measured noise spectrum of  $V_{REF}$ .

including a 1.8 pF decoupling capacitor. A total of 60 voltage references (three different wafers) are packaged in ceramic [24] and measured. Fig. 9 shows the measured  $V_{REF}$  and TC distribution without trimming. The voltage references achieve the average TC of 22.5 ppm/°C and  $3\sigma$  inaccuracy of  $\pm 2.47\%$  from 0 °C to 100 °C. Fig. 10 shows the results after room-temperature trimming to the average  $V_{REF}$  of uncompensated voltage references. The  $3\sigma$  inaccuracy from 0 °C to 100 °C is  $\pm 0.99\%$ , and average TC is 30.9 ppm/°C. Thus, inaccuracy is reduced by  $2.5\times$  at the expense of a 37% TC increase. To trim  $V_{REF}$  to a different voltage,  $W_1$  can be changed using transistors  $M_{CX}$  by sacrificing TC. In simulation,  $V_{REF}$  can be adjusted by 37 and 59 mV within TC of 50 and 100 ppm/°C, respectively.

Fig. 11 shows the measured start-up waveform of  $V_{REF}$  and 1% settling time of 92.2 ms. Time taken from 0 to 0.9 V is in 200  $\mu\text{s}$  since  $V_{gs}$  of  $M_{NX}$  (Fig. 1) is near to  $V_{th}$  initially. Fig. 12 shows line sensitivity (LS) of 0.31%/V across 1.4–3.6 V supplies and power supply rejection of  $\sim -40$  dB from 10 Hz to 10 kHz at room temperature.

The voltage reference dissipates 35.0 pW on average over 60 measured voltage reference from three wafers with a sigma

TABLE I  
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER WORKS.

Parameter	This Work	[1]	[2]	[3]	[4]	[5]	[6]	[9]	[10]	[11]	[12]	[17]
Technology ( $\mu\text{m}$ )	0.18	0.18	0.35	0.13	0.16	0.18	0.13	0.18	0.11	0.18	0.18	0.13
Type	CMOS	BJT	BJT	BJT	BJT	BJT	BJT	CMOS	CMOS	CMOS	CMOS	CMOS
Supply Voltage (V)	1.4–3.6	1.5–2.5	1.4–3.0	0.5–1.5	1.6–2.0	1.2–1.8	0.75–1.6	0.45–2.0	0.24–0.4	0.7–2.5	0.45–1.8	0.5–3.0
Average $V_{\text{REF}}$ (V)	1.25	1.19	1.18	0.50	1.09	1.09	0.26	0.26	0.20	0.44	0.12	0.18
Temp. Range ( $^{\circ}\text{C}$ )	0–100	–20–100	–10–110	0–80	–40–125	–40–120	–20–85	0–125	10–90	–25–85	–40–125	–20–80
$3\sigma$ Inaccuracy @ Entire Temp. Range (%)	4.9 <sup>†</sup> , 2.0 <sup>‡</sup>	N/A	N/A	N/A	1.5 <sup>†</sup> , 0.2 <sup>‡</sup>	N/A	N/A	N/A	N/A	N/A	N/A	N/A
$3\sigma$ Inaccuracy @ One Temp. (%)	2.4 <sup>†</sup> , 0.8 <sup>‡</sup>	0.4 <sup>‡</sup>	0.6 <sup>‡</sup>	2.0 <sup>†</sup>	N/A	2.2 <sup>†</sup>	6.0 <sup>†</sup> , 0.5 <sup>‡</sup>	10.8 <sup>†</sup>	N/A	N/A	11.6 <sup>†</sup> , 1.9 <sup>‡</sup>	2.6 <sup>†</sup>
TC (ppm/ $^{\circ}\text{C}$ )	8–53 ( $\mu\text{23}$ ) <sup>†</sup> , 11–73 ( $\mu\text{31}$ ) <sup>‡</sup>	$\mu\text{25}$ <sup>‡</sup>	13 <sup>‡</sup>	75–125 <sup>‡</sup>	5–12 <sup>‡</sup>	$\mu\text{147}$ <sup>†</sup>	$\mu\text{40}$ <sup>‡</sup>	39–357 ( $\mu\text{165}$ ) <sup>†</sup>	58–186 ( $\mu\text{134}$ ) <sup>†</sup>	$\mu\text{25}$ <sup>†</sup> , 22 <sup>‡</sup>	10–120 ( $\mu\text{32}$ ) <sup>†</sup> , 125–250 ( $\mu\text{64}$ ) <sup>‡</sup>	17–231 <sup>†</sup>
Current Consumption @ Room Temp. (A)	24p	2.0n	29n	64n	55 $\mu$	83 n	227 n	5.8n	21 $\mu$	27 n	32 n	4.4p
LS (%/V)	0.31	0.062	0.20	1.11	0.02	6.47	0.02	0.44	4.09	0.13	1.01	0.03
PSR (dB)	–41 @ 100Hz	–67 @ 100Hz	–53 @ DC	–52 @ DC	–74 @ DC	–62 @ 100Hz	–86 @ DC	–45 @ 30Hz	–42 @ DC	–65 @ DC	44 @ 100Hz	–53 @ 100Hz
Noise (0.1Hz–10Hz) ( $\mu\text{V}$ )	24.4	N/A	N/A	N/A	6.1	N/A	N/A	22.0	N/A	N/A	N/A	N/A
#Samples	60 (3 wafers)	10	10	6	61 (2 wafers)	9	90,000 (5 wafers)	40 (3 wafers)	10	40	55	49 (2 wafers)
Active Area ( $\text{mm}^2$ )	0.0025	0.098	0.48	0.026	0.12	0.029	0.070	0.043	0.070	0.041	0.012	0.0014

<sup>†</sup>: Untrimmed, <sup>‡</sup>: 1-point trimmed

of 2.1 pW at 1.4 V supply voltage and room temperature. As shown in Fig. 13, the circuit is not sensitive to the supply voltage since  $I_{\text{ds}}$  of  $M_{\text{NX}}$  is not sensitive to  $V_{\text{ds}}$ . However, the subthreshold current is sensitive to temperature, and power consumption increases by  $\sim 200\times$  from 0  $^{\circ}\text{C}$  to 100  $^{\circ}\text{C}$ . The operation of the proposed circuit is confirmed from –25  $^{\circ}\text{C}$  to 175  $^{\circ}\text{C}$  in measurement as shown in Fig. 14. To improve TC for a wide temperature range,  $I_{\text{VDD}}$  needs to be increased with larger  $W_1/L_1$  to reduce  $\Sigma I_{\text{DIOX}}/I_{\text{VDD}}$ . Fig. 15 shows the measured integrated noise of 24.4  $\mu\text{V}$  from 0.1 to 10 Hz, which is larger than that of conventional bandgap voltage references (6.1  $\mu\text{V}$  [4] and 9.1  $\mu\text{V}$  [7] from 0.1 to 10 Hz) mainly due to a trade-off between power consumption and noise performance. More on-chip decoupling capacitor can reduce noise, but it increases the initial settling time at startup and area [5].

Table I summarizes the performance of this voltage reference and compares it with previous low-power voltage references. Voltage references without a bipolar junction transistor (BJT) [9]–[12], [17] and two bandgap voltage references [3], [6] provide output voltages of less than 1 V. Compared with the bandgap voltage references in [1], [2], and [5], the proposed voltage reference achieves competitive performance in terms of  $3\sigma$  inaccuracy, TC, LS, and active area with  $>83\times$  lower current consumption. The bandgap voltage reference in [4] demonstrates superior performance in these parameters; however, the current consumption (55  $\mu\text{A}$ ) is similar to the active current consumption budget in microsystems and therefore it cannot be used for the targeted IoT systems.

## V. CONCLUSION

This paper proposes a subthreshold voltage reference with stacked pMOS transistors. The stacked transistors elevate the output voltage and help increase the dynamic range of analog circuits in battery-operated systems. The prototype voltage

reference with four stacked pMOS transistors is fabricated in a standard 0.18- $\mu\text{m}$  CMOS process. The measurement results from three different wafers show  $3\sigma$  inaccuracy of  $\pm 1.0\%$  from 0  $^{\circ}\text{C}$  to 100  $^{\circ}\text{C}$  with a single room-temperature trim with 35-pW power consumption at a 1.4 V supply and room temperature.

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