

A 28-GHz 32-Element TRX Phased-Array IC With Concurrent Dual-Polarized Operation and Orthogonal Phase and Gain Control for 5G Communications

Bodhisatwa Sadhu¹, Member, IEEE, Yahya Tousi, Joakim Hallin, Stefan Sahl, Scott K. Reynolds, Örjan Renström, Member, IEEE, Kristoffer Sjögren, Olov Haapalahti, Nadav Mazor, Bo Bokinge, Gustaf Weibull, Håkan Bengtsson, Anders Carlinger, Eric Westesson, Jan-Erik Thillberg, Leonard Rexberg, Mark Yeck, Xiaoxiong Gu, Senior Member, IEEE, Mark Ferriss, Duixian Liu, Fellow, IEEE, Daniel Friedman, and Alberto Valdes-Garcia, Senior Member, IEEE

Abstract—This paper presents the first reported 28-GHz phased-array IC for 5G communications. Implemented in 130-nm SiGe BiCMOS, the IC includes 32 TRX elements and features concurrent independent beams in two polarizations in either TX or RX operation. Circuit techniques to enable precise beam steering, orthogonal phase and amplitude control at each front end, and independent tapering and beam steering at the array level are presented. A TX/RX switch design is introduced which minimizes TX path loss resulting in 13.5 dBm/16 dBm Op1dB/Psat per front end with >20% peak power added efficiency of the power amplifier (including switch and off-mode LNA) while maintaining a 6 dB noise figure in the low noise amplifier (including switch and off-mode PA). Comprehensive on-wafer measurement results for the IC across multiple samples and temperature variation are presented. A package with four ICs and 64 dual-polarized antennas provides eight 16-element or two 64-element concurrent beams with 1.4°/step beam steering (<0.6° rms error) across a ±50° steering range without requiring calibration. A maximum saturated effective isotropic radiated power of 54 dBm is measured in the broadside direction for each polarization. Tapering control without requiring calibration achieves up to 20-dB sidelobe rejection without affecting the main lobe direction.

Index Terms—28 GHz, 5G, SiGe, antenna array, base station, beamforming, calibration, cellular, dual polarization, effective isotropic radiated power (EIRP), hardware, millimeter wave, mobile, multi-in multi-out, orthogonal phase and gain, phased array, picocell, sidelobe, silicon, switch, tapering, transceiver.

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B. Sadhu, Y. Tousi, S. K. Reynolds, M. Yeck, X. Gu, M. Ferriss, D. Liu, D. Friedman, and A. Valdes-Garcia are with the IBM T. J. Watson Research Center, Yorktown Heights, NY 10598 USA (e-mail: sadhu@us.ibm.com).

J. Hallin, K. Sjögren, and G. Weibull are with Ericsson, 417 56 Göteborg, Sweden.

S. Sahl, Ö. Renström, O. Haapalahti, B. Bokinge, H. Bengtsson, A. Carlinger, J.-E. Thillberg, and L. Rexberg are with Ericsson, 164 40 Stockholm, Sweden.

N. Mazor is with IBM Research, 3498825 Haifa, Israel.

E. Westesson is with Ericsson, 223 62 Lund, Sweden.

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I. INTRODUCTION

NEXT generation mobile technology (5G) is on its way to delivering mobile experience differentiation by providing higher data rates, lower latency, and improved link robustness [1]. The use of phased arrays at millimeter-wave frequencies offers a path to support multiple users with high data rates by establishing high-bandwidth directional links between the base station and mobile devices [2], [3]. Fig. 1 shows some potential use cases: millimeter-wave 5G phased-array picocells placed on buildings communicating with user handheld devices; 5G auto-cells in cars communicating with millimeter-wave 5G picocells or 5G basestations to provide high data rate, in-vehicle connectivity; and scaled up phased arrays used for millimeter-wave backhaul [1], [4]. Millimeter-wave phased arrays will create multiple simultaneous beams pointed to serve multiple users using spatial multiplexing, and each picocell will steer the beams electronically to serve users using time division multiplexing.

To realize these potential use cases, a 5G phased array base station must support a large number of precisely controlled beams, and to enable effective deployment, they must also be both compact and power efficient. These system goals have significant millimeter-wave radio interface implications, including scalability of the radio frequency integrated circuit-plus-antenna-array solution [4], increasing beam count by supporting dual polarization [5], precise beam steering while maintaining low sidelobes, and the requirement to achieve high effective isotropic radiated power (EIRP) without sacrificing TX mode power efficiency. Packaged Si-based phased arrays [6]–[15] with nonconcurrent dual-polarized TX and RX operation [7], [8], concurrent dual-polarized RX operation [8], and multi-IC scaling [8], [16] have been demonstrated. However, support for concurrent dual-polarized operation in both RX and TX remains unaddressed, and high output power comes at the cost of power consumption, cooling complexity, and increased size. Moreover, there is a need for architecture and circuit-level innovation that can simplify phased-array calibration.

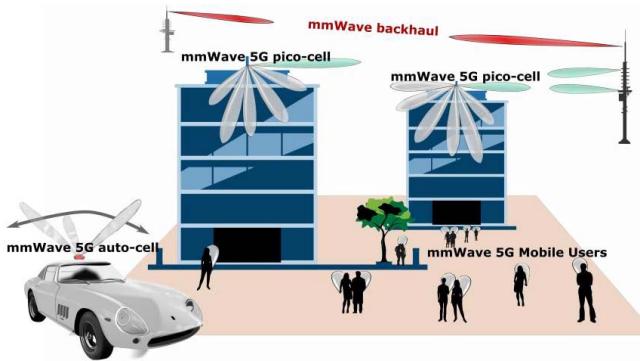


Fig. 1. Example use case scenarios for millimeter-wave 5G phased arrays.

The millimeter-wave IC reported in [17] and expanded here supports simultaneous dual-polarized operation in TX and RX modes, and the overall solution is compatible with a volume-efficient antenna-in-package solution. A new TX/RX switch at the shared antenna interface enables high EIRP without sacrificing TX efficiency, and a transmission line (t-line) based phase shifter achieves $<5^\circ$ phase steps with $<1^\circ$ rms error, which enables precise beam control. Furthermore, this paper introduces techniques to achieve orthogonal control of gain and phase which enables: 1) beam steering while maintaining side-lobe levels and 2) beam tapering with no calibration required while maintaining the main lobe direction. Minimizing calibration complexity is highly desirable in the context of the anticipated large-scale deployment of millimeter-wave phased arrays for 5G.

II. 5G PHASED-ARRAY CHALLENGES

Since the first publication of a Si-based phased-array IC in 2004 [18], and fully integrated millimeter-wave TX and RX ICs in 2006 [19], significant research in this area has resulted in improvements in frequency of operation, performance, and complexity. Among these, transceiver and phased-array designs operating in the 60-GHz frequency band targeting indoor networking applications have achieved a high level of integration and maturity [6], [7], [9]–[11], [15], [16], [20]–[23]. Millimeter-wave IC developments were accompanied by complete standards developments [24], [25] that consider beamforming and directional links. For these applications, the envisioned usage scenarios consider, in general, 2–3 users sharing a given space, peak data rates <7 Gb/s, and distances <20 m including reflections [26]. The expected deployment of millimeter-wave-based 5G base stations dynamically supporting a large number of users, however, demands a much greater level of performance from the beamforming solution than previously demonstrated. The following sections describe key system level challenges of designing a millimeter-wave phased array for a 5G base station. The effect of IC architecture and circuit-level tradeoffs are also discussed in the context of this challenge.

A. Support for Simultaneous Beams Using Spatial and Polarization Diversity

In traditional, quasi-omnidirectional cellular systems, the total data rate supported by a given base station is limited by

the available bandwidth. The ability to achieve beamforming provides a unique opportunity for spatial multiplexing, thereby re-using the same bandwidth in multiple spatially exclusive directions. Each beam can be formed using a unit phased array. Moreover, by using scalability techniques [4], [16], unit phased arrays can be combined to create larger apertures, resulting in narrower beams and higher directivity in TX and RX modes. In this context, a system level consideration relates to the optimal way to divide the total number of elements among multiple modular ICs. An approach using multiple small ICs with few elements per IC can be used to target a reduction in the interconnect length from the ICs to the antennas by enabling the small ICs to be placed close to the antennas.

However, from a system perspective, the small IC approach suffers from a few drawbacks.

- 1) System verification simulations are complicated and need to include many ICs and significant IC to IC connectivity on package.
- 2) Digital infrastructure needs to be per IC making digital control of the phased-array cumbersome, impacting both chip area and digital control speed.
- 3) Package assembly involving many small ICs is potentially significantly more complex, increasing the number of assembly steps and affecting assembly yield.

The tradeoffs between an approach using many small ICs and one using a few large ICs are listed in Table I. In this paper, we selected four ICs with 32 elements per IC to implement 128 element phased-array elements feeding 64 dual polarized in-package antennas. The IC scaling at the package level was implemented using a scaling approach introduced in [4] and [8].

An additional strategy to increase channel capacity by up to 2X is to use the two available orthogonal polarizations [5] to create simultaneous and independent beams. The support for multiple simultaneous beams not only increases the maximum number of simultaneous users that can be supported, but also opens a path to the implementation of self-backhauling [27] by using one polarization to establish a link between picocells.

B. Small Overall Solution Footprint

Given the advantages of supporting dual-polarization operation and multiple spatial beams, the next challenge is to realize such functionality in a small form factor. Unlike current macro-cell base stations, forthcoming 5G access points are expected to be deployed in multiple indoor and outdoor urban spaces, making a compact, Wi-Fi access point-like form factor desirable. At 28 GHz, the area occupied by the phased array is primarily determined by the area of the $\lambda/2$ spaced antenna array. As a result, sharing the antennas among multiple functions has a significant impact on the overall size of the solution. For example, to support half-duplex transmit and receive in both horizontal (H) and vertical (V) polarizations, the phased array needs to support four modes of operation: simultaneous TX-H and TX-V, and simultaneous RX-H and RX-V. As shown in the illustration and accompanying table in Fig. 2, this functionality can be implemented using different strategies with significantly different area implications.

	<u>Option 1</u>	<u>Option 2</u>	<u>Option 3</u>	<u>Option 4</u>
Aggregate array area	4X	2X	2X	1X
Aggregate # antennas	4N	2N	2N	N
Aggregate # frontends	4N	4N	2N	2N
Frontend type	TX or RX	TX or RX	TRX	TRX
IC complexity	Lowest	Low	High	Highest

Fig. 2. Different options for functional integration for 5G millimeter-wave phased arrays.

TABLE I
SUMMARY OF THE TRADEOFF BETWEEN DIFFERENT IC MODULARITY OPTIONS

Modular IC approach	Many small ICs with low integration	Few highly integrated large ICs
Interconnect length (IC FEs \leftrightarrow in-package antennas)	Small interconnect length when aggregate IC area is much lower than aggregate antenna area	Small interconnect length when aggregate IC area is similar to aggregate antenna area
mmWave performance verification of complete phased array	More challenging: Significant package routing and many ICs in phased array module make verification simulations challenging	Less challenging: Less package/board-level routing and fewer ICs makes phased array module verification easier
Digital control	Challenging: Digital infrastructure is repeated per IC, control is not centralized	Superior: Centralized digital control
Total IC area per complete phased array	Potentially larger aggregate IC area due to repeating digital infrastructure	Potentially smaller aggregate IC area due to fewer digital infrastructure instantiations
Package assembly	More challenging to assemble many small ICs, increasing number of assembly steps	Less challenging to assemble fewer ICs requiring fewer assembly steps
Overall yield	Trade-off: Higher yield for each individual IC with smaller area but lower assembly yield due to larger number of assembly steps	Trade-off: Lower yield for each individual IC with larger area but higher assembly yield due to smaller number of assembly steps

As compared to a single-polarized TX RX chipset implementation in Option 1, Option 4 achieves a $4\times$ reduction in area of the package. This makes Option 4 a compact, practical approach for a dual polarized millimeter-wave 5G phased-array solution.

This paper presents the first demonstration of a fully integrated dual polarized transceiver for millimeter-wave phased arrays, achieving the lowest footprint to achieve the required functionality (Option 4). Section III describes the design techniques that were used to tackle the design complexity challenge associated with such a high level of integration.

C. Low-Power Consumption to Ease the Thermal Solution

The choice of beamforming architecture can have a critical impact on the system power consumption. The tradeoffs

between hardware requirements and design complexity are described in [28] and [29]. In this paper, we have selected an RF-phase shifting architecture, which represents the lowest hardware and power consumption requirements at the cost of millimeter-wave design complexity.

Moreover, for a TRX solution, the TX/RX switch losses at the antenna can significantly impact TX efficiency, increasing the power consumption to achieve a desired output power. In this paper, we demonstrate a switch topology that minimizes TX switch losses to enable high TX efficiency (Section III-D.)

D. Accurate Beam and Sidelobe Control With Reduced Calibration Complexity

Finally, having outlined the challenges and tradeoffs associated with the overall array architecture, we turn to describing

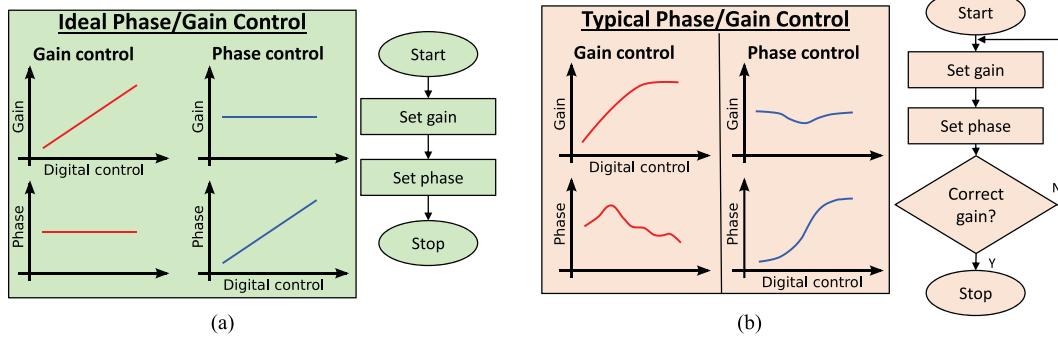


Fig. 3. (a) Ideal phase and gain control showing a simple beam control algorithm enabled by orthogonal phase and gain control. (b) Typical phase and gain control in state-of-the-art phased arrays showing a complex beam control algorithm due to non-orthogonal phase and gain control.

the phase shifting and beam steering requirements, and their associated calibration challenges. Among other requirements, a phased-array antenna has two important beamforming functions: beam steering and sidelobe suppression.

1) *Orthogonal Phase and Gain Control*: Beam steering and sidelobe suppression are directly determined by two actuators in each element: 1) the phase shifter which enables beam steering 2) and the variable gain amplifier (VGA), which achieves sidelobe suppression through tapering [30]. From a system perspective, it is imperative to achieve orthogonal beam steering and sidelobe suppression functions. In other words, sidelobe suppression should be maintained during beam steering, and beam pointing direction should be maintained while achieving sidelobe suppression. To achieve orthogonal sidelobe and beam steering control, the phase and amplitude control in each element must be orthogonal as well (either by design or after calibration), as shown in Fig. 3(a). However, in most current Si-based phased-array implementations, variable gain amplifiers show a significant phase variation over gain settings and millimeter-wave phase shifters typically show gain or loss variation of a few dB over phase settings, as shown in Fig. 3(b). The integration of memory units or beam tables at each front-end (FE) to store pre-calibrated phase and amplitude settings has been demonstrated previously [9]. Using these tables, it is, in principle, possible to store calibrated phase and amplitude control combinations that simulate orthogonality. However, to obtain such calibration tables for both beam steering and tapering across temperature, supply, and electromagnetic environment variations implies a complex and expensive calibration process. Such calibration not only requires large amounts of data storage and complex algorithms, but also relies on accurate phase measurements over the air. Ultimately the achievable effective phase and amplitude control resolution would be defined by the performance of such calibration. In this paper, the desired functional orthogonality has been directly mapped to the actuators by implementing inherently orthogonal phase and gain control functions. Circuit-level techniques that address this challenge are introduced in Section III and measurements demonstrating orthogonal sidelobe suppression and beam steering control are presented in Section IV.

2) *Phase Resolution*: A second key requirement is achieving phase resolution (or minimum phase shift step) and phase accuracy (often evaluated as the rms phase error compared

to intended steps). For phased arrays where a uniform phase gradient is applied, the phase resolution directly translates to beam steering resolution. For example, as shown in row 2 of the table in Fig. 4(a), when a uniform phase gradient is applied across the phased array, the beam steering resolution is 1.4° for a phase shifter resolution of 5° . In contrast, the beam steering resolution is only 6.5° for a phase shifter resolution 22.5° . However, for large arrays, it is possible to apply a non-uniform phase gradient and use an averaging effect to interpolate to a finer beam steering resolution, as shown in row 3 of the table in Fig. 4(a). This effect of beam interpolation using phase averaging is shown in the simulations results in Fig. 4(b)–(d) for an 8×8 square array with $\lambda/2$ element spacing. Fig. 4(b) shows a family of simulated beam patterns for attempted beam pointing at an arbitrary steering angle. Each beam pattern in Fig. 4(b) corresponds to a fixed phase shifter resolution; the phase shifter resolution is swept to create the family of beam patterns shown. As shown in Fig. 4, while fairly accurate beam pointing is achieved in an arbitrary direction even with low-resolution phase shifters (e.g., 22.5° resolution), the sidelobes are severely compromised when compared to beam patterns created using high-resolution phase shifters (e.g., 5° resolution). Fig. 4(c) and (d) shows the resultant sidelobe suppression as the beam is pointed across $\pm 45^\circ$. In general, as shown in Fig. 4(c) and (d), limited phase resolution produces a periodic degradation in the sidelobe suppression versus steering angle. While attempting ~ 20 -dB sidelobe suppression using a Taylor window tapering function, and with ideal phase resolution, a uniform sidelobe suppression of ~ 19.5 dB is obtained across $\pm 45^\circ$ scanning range. However, for a coarse phase resolution of 22.5° , the sidelobe suppression at some angles is degraded by as much as 5 dB. Moreover, a recent study has shown that a coarse (2 bit) resolution can also result in antenna-array gain reduction of up to 3 dB for non-boresight directions [31]. In this context, a phase resolution of 5° is an attractive target as it results in beam pointing with $<1^\circ$ beam steering resolution with sidelobe suppression levels within ~ 1 dB of an ideal phase shifter when attempting 20 dB sidelobe suppression.

III. CIRCUIT-LEVEL SOLUTIONS

In this section, we discuss the circuit architecture choices as well as circuit techniques and innovations that enable the design to overcome the challenges outlined in Section II.

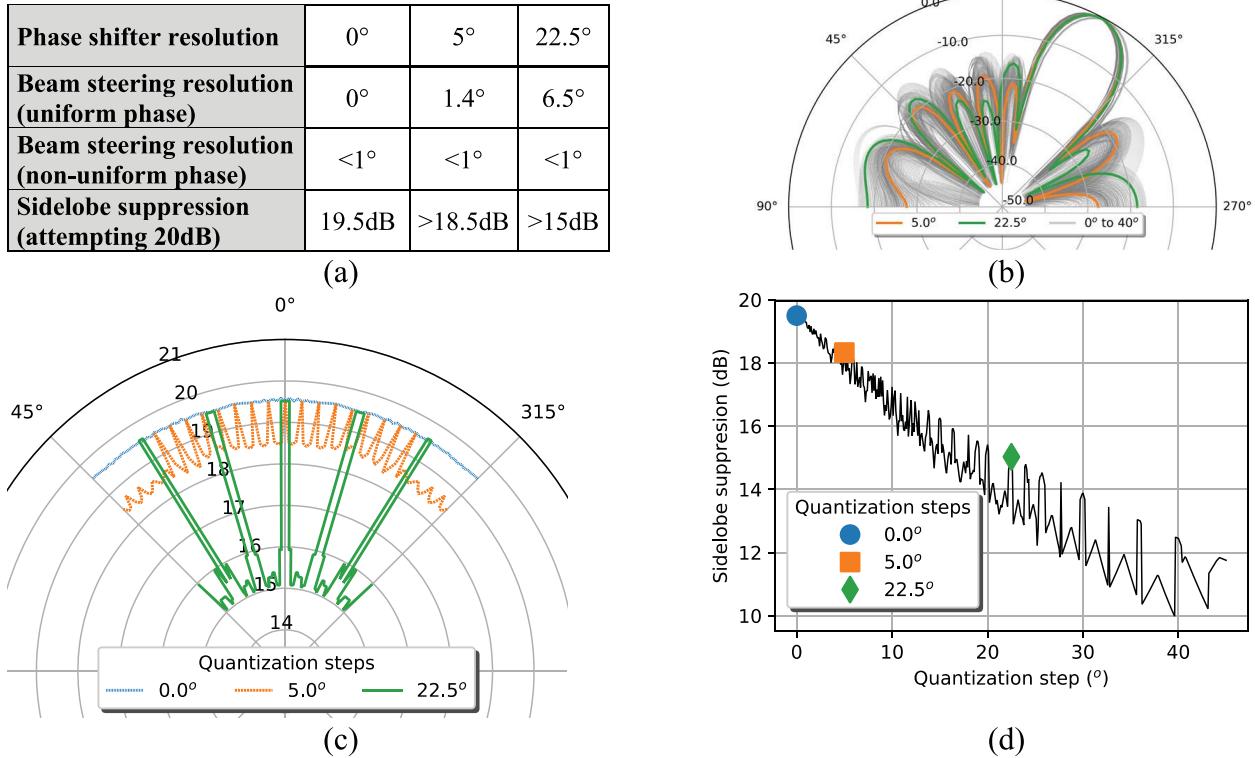


Fig. 4. (a) Simulation of the effect of phase shift quantization in an 8×8 phased array showing beam steering resolution for different phase shifter resolutions. (b) Beam pointing at an arbitrary direction (30°) for different phase shifter resolutions showing a large impact on sidelobe suppression. (c) Sidelobe suppression versus beam steering angle for three different phase shifter resolutions while attempting 20-dB Taylor window tapering. (d) Worst case sidelobe suppression versus quantization steps while attempting ~ 20 -dB Taylor window tapering.

The impact of the architectural choices and circuit-level performance parameters are summarized in Table II. Measured results for key circuit performance parameters are also summarized.

A. IC Architecture

The IC architecture is shown in Fig. 5. The IC includes two independent 16-element phased-array transceivers (TRX) enabling two simultaneous and independent 16-element beams in either TX or RX mode. The 32 separate single-ended TX/RX RF ports in the IC are designed to interface with 16 dual-polarized in-package antennas to support simultaneous beams in H and V polarizations. The IC uses an RF-phase shifting architecture that minimizes the total number of circuit components [28], [29]. Furthermore, each TRX FE shares an antenna, a passive, bidirectional RF phase shifter, and a passive, bidirectional combiner/splitter between the TX and RX in time division duplex operation. This sharing is achieved using TX/RX switches at each of these components, as shown in Fig. 5, and in the FE block diagram in the center of Fig. 6. The design uses $\lambda/4$ switches at the combiner/splitter and phase shifter, and uses a modified $\lambda/4$ switch at the antenna to enable a high transmit efficiency (Section III-D).

The IC uses a two-step sliding IF frequency conversion architecture with a 28-GHz RF, 7.34-GHz internal IF, and 3-GHz external IF. The two polarizations share an external 5.17-GHz local oscillator (LO) input that is quadrupled to 20.68 GHz to create the RF-LO. This 20.68-GHz RF-LO is

then divided to 10.34 GHz to create the IF-LO. The phased array combining/splitting is accomplished in two steps: first, two sets of eight signals are combined/split at RF using passive combiners/splitters; next, these two sets are further combined/split in the current domain at the 7.34-GHz internal IF. Note that the most hardware efficient 16×1 implementation presents a significant linearity challenge at the RF mixers which would need to handle 16 combined signals. In contrast, at the cost of an extra mixer per path, the implemented 8×2 architecture achieves higher linearity since the RF mixers must handle only eight combined signals. The TX IF mixer employs a Hartley image reject architecture followed by a low pass filter, while the TX RF mixer is followed by a high pass filter, which reduces the impact of image and LO spurs in the TX mode. In the RX mode, the combined and amplified signals at the output of the RF mixers are down converted using linear IF mixers followed by a linear 3-GHz VGA.

B. Front-End Architecture

Fig. 6 shows the architecture of each identical FE. Each 28-GHz FE comprises a shared $5^\circ/\text{step}$ loss-invariant phase shifter, a TX-RX switch, followed on the TX side by a phase-invariant VGA and phase inverter which interfaces with a single-ended power amplifier (PA) and antenna switch. On the RX side the antenna switch is followed by a single-ended LNA, an active balun and a phase-invariant VGA and phase inverter. Section III-D and III-E provides further details on some of the 28-GHz blocks in each FE.

TABLE II
CIRCUIT BLOCKS AND THEIR SYSTEM LEVEL IMPACT (QUALITATIVE)

	Sub-block performance parameter	Measurement	Phased array antenna module system impact
Architecture	RF phase shifting architecture	N/A	Minimizes area Minimizes power consumption
	Switched TX/RX architecture	N/A	2X reduction in area
	Simultaneous H/V polarization	N/A	2X reduction in area
Phase shifter	Phase control range	210° (+180° in phase inverter)	Enables beamforming
	Phase shift resolution	4.9°	Minimizes beam steering errors Improves side-lobe suppression
	Phase error	< ±1.5°	Minimizes beam steering errors Minimizes beam shape distortion Minimizes calibration complexity
	Gain variation during phase control	< ±0.7dB	Minimizes calibration complexity
	Phase switching speed	< 4ns	Beam switching speed < 4ns
VGA	Gain control range	8dB	Enables tapering up to 25dB side-lobe rejection
	Phase variation during gain control	±1.5°	Minimizes calibration complexity
Antenna switch	TX mode switch loss	~0dB	Improves TX efficiency achieving 23% power savings @Psat compared to traditional switch
	RX mode switch loss	~2.3dB	Trades off ~0.6dB RX sensitivity for 1.2dB TX efficiency improvement (see Fig. 6(b))
LNA	Noise figure	3.7dB	Improves RX sensitivity
	Gain	12dB	Improves RX sensitivity
PA	Op1dB	14dBm	Directly improves EIRP
	Gain	32dB	Improves linearity

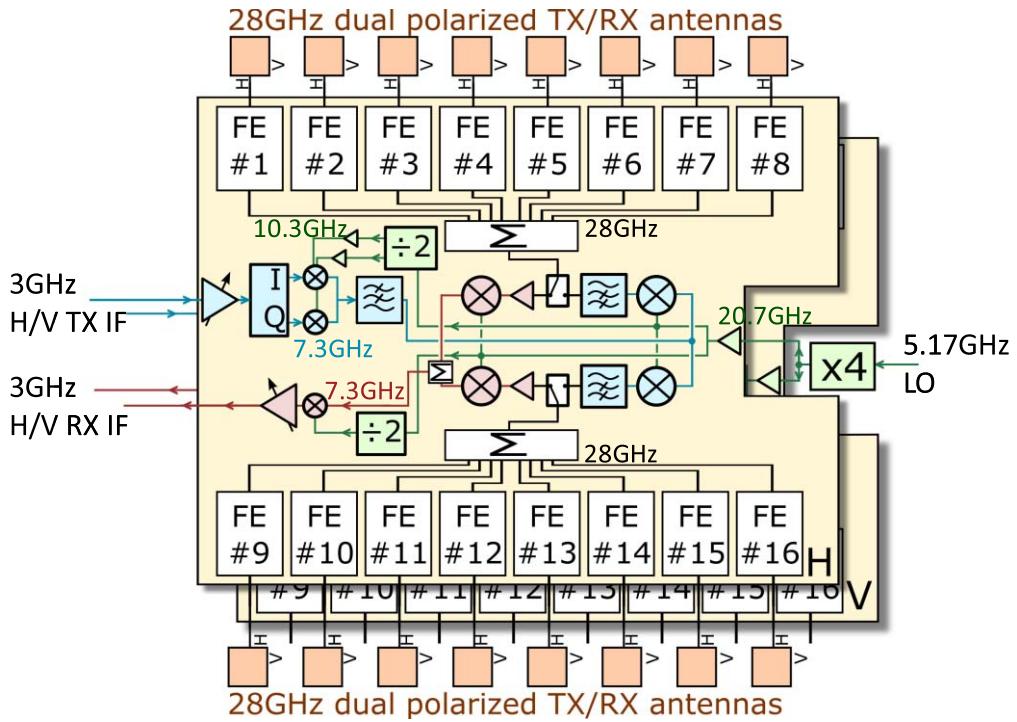


Fig. 5. IC architecture and block-level schematic.

C. Digital Control

The digital control infrastructure includes a centralized digital core and a distributed FE control module. The digital control bus is cascaded through each FE connecting to one

FE control module per FE. To save area, the FE control modules are incorporated underneath the splitter/combiner ground shield. The digital control interface of the IC is a serial peripheral interface running at 122 MHz. For a scaled solution

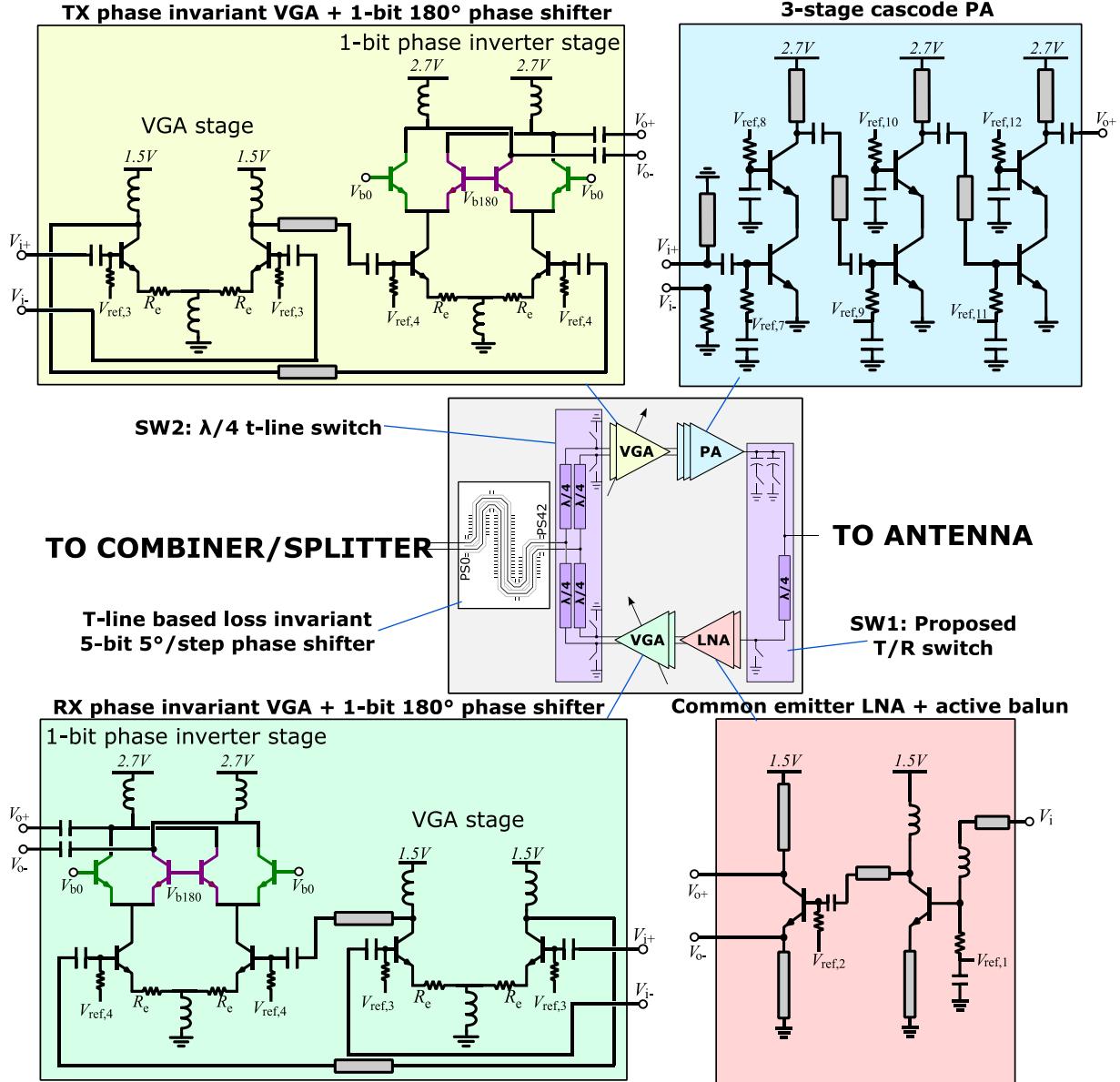


Fig. 6. Architectural block diagram of a single (H or V) front end with detailed schematics of front-end circuits.

with multiple ICs, each IC is uniquely addressable using IC address bits.

D. Front-End Transmit/Receive Switch

There are 16 FE blocks per polarization, making the FE power dissipation key to the overall power budget. As discussed in Section II, PA efficiency and T/R switch insertion loss are critical to the EIRP versus power dissipation tradeoff.

In this paper, a T/R switch that minimizes the insertion loss in the TX mode is introduced. In a traditional T/R switch implementation [32], $\lambda/4$ t-line-based switches are used at the PA and LNA. As a result, the signal flows through a $\lambda/4$ t-line in both TX and RX modes, resulting in approximately equal insertion losses in either mode. In the proposed design, the $\lambda/4$ t-line-based switch is omitted on the TX side, as shown

in Fig. 7(a). Thus, in TX mode, the PA is connected directly to the antenna, resulting in negligible TX insertion loss. In RX mode, it is desirable to create a high impedance at the TX input to ensure that most of the RX signal flows into the LNA. In the implemented design, when the PA is turned off, its output impedance is comprised of a low conductance real part in parallel with a high susceptance inductive load. As shown in Fig. 7(a), a bank of digitally controlled switched capacitors, in parallel with the output of the PA, create a suitable negative susceptance to resonate out the inductance. In RX mode, this strategy results in an effective high real impedance, reducing the impact of the TX input on the LNA noise figure (NF).

To demonstrate the resulting output power versus NF tradeoff, Fig. 7(b) compares the TX FE Op1dB and Psat, and RX LNA + switch NF of the proposed and traditional switch approaches. The removal of the PA $\lambda/4$ switch improves the

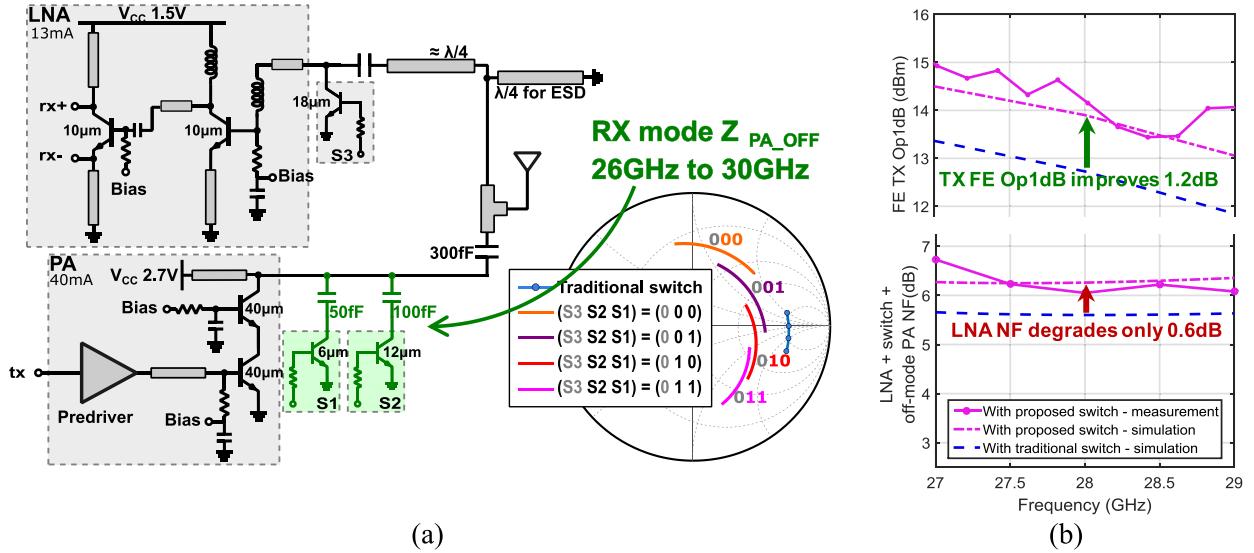


Fig. 7. (a) Detailed schematic of the implemented TX/RX switch. (b) Simulations and measurements showing performance (Op1dB of TX FE and NF of LNA + switch + PA) with the proposed TX/RX switch compared to simulations of the same performance parameters with a traditional TX/RX switch across frequency.

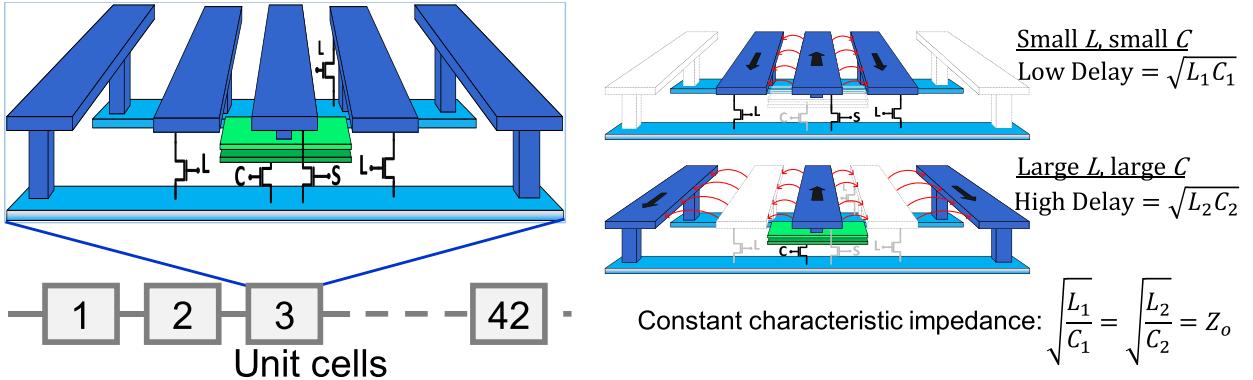


Fig. 8. Phase shifter using cascaded unit cells, showing 1 (rotated) unit cell in detail (left), and the mechanism for obtaining low delay and high delay modes in each unit cell (right).

Op1dB and Psat by 1.2 dB while incurring only a 0.6-dB penalty in RX NF. This results in Psat >16 dBm per signal path and PA + switch peak efficiency >20%, while still maintaining a 6-dB LNA + switch NF. Translating this to power savings, the additional 1.2-dB TX loss per path of the traditional approach would have consumed 2.35 W/pol. (or 23%) more power for the same Psat, compared to the chosen approach.

E. Phase Shifter

The phase shifter is arguably the most critical block in an RF-phase shifting phased array and determines phase control range, phase shift resolution, phase error, gain variation during phase control, and phase switching speed. The impact of these parameters on system level performance is tabulated in Table II. In order to simultaneously satisfy the requirements for all these parameters, a phase shifter concept based on tuning the line capacitance and line inductance of a t-line was first introduced in a 60-GHz CMOS design in [33]. This

paper utilizes the Ka-band implementation presented in [34] with a higher phase shift resolution compared to [33]. As shown in Fig. 8, the phase shifter consists of a series of unit cells that in aggregate construct the artificial t-line. Each unit cell includes side-shields and a MIMCA that can be switched in and out to alternate between a “high inductance + high capacitance” mode and a “low inductance + low capacitance” mode. Since the t-line delay relates to the inductance (L) and capacitance (C) as delay = \sqrt{LC} , these modes correspond to a high delay mode and a low delay mode. Moreover, in each of these modes, the ratio of inductance to capacitance is kept constant to maintain a constant characteristic impedance, $Z_0 = \sqrt{L/C}$.

A unit-cell t-line-based phase shifter offers several advantages. Compared to reflection type phase shifter (RTPS) designs [35], [36], the proposed approach enables high phase accuracy due to unit-cell matching. Moreover, unlike an RTPS which is limited by the C_{\max}/C_{\min} varactor ratio of a technology, the total phase range in a t-line phase shifter can be scaled easily by adding more unit cells, making it

possible to achieve $>180^\circ$ phase shift. Furthermore, the phase resolution can be improved simply by reducing the unit-cell size. Additionally, the t-line approximates a broadband true-time-delay and is not limited by the narrowband approximation of a phase shifter. Another significant advantage of the proposed approach is phase switching time. As shown in Fig. 8, phase switching is realized by switching MOS transistors attached to floating metals (with low capacitance) enabling switching speeds of a few nanoseconds. Loss invariance in the phase shifter is implemented using switched MOS resistors, shown as the “S” bit controlled MOSFETs in Fig. 8, that equalize the losses between the high delay and low delay modes. This technique enables $<\pm 0.5$ dB of loss variation across $>180^\circ$ of phase variation. The reader is referred to [34] for further circuit details, as well as detailed measurement results across process, temperature, and frequency.

F. Variable Gain Amplifier and Phase Inverter

Each FE incorporates a 28 GHz two-stage phase-invariant VGA in both TX and RX paths to enable beam tapering. As shown in Fig. 6, the resistively degenerated common emitter first stage realizes gain control by controlling the current bias through the bipolar junction transistor (BJT), while the second stage implements a phase inversion function using a switching cascode architecture. It was shown in [37] that for an optimized emitter degeneration resistance, the output phase is invariant to the bias current in the amplifier. Based on this principle, a 5-bit current digital to analog converter is employed to achieve phase invariant gain control in the FE VGA for both TX and RX paths to enable tapering while maintaining beam shape and direction. Moreover, since the value of the optimal emitter degeneration resistor is nominally independent of frequency, temperature and supply voltage, the achieved phase invariance property is robust and maintained across corners in the phased array [37]. The measured phase of the VGA S21 varies by $<\pm 2^\circ$ over 8 dB of gain range providing up to 25 dB of sidelobe suppression through beam tapering using a Taylor window function. This performance is maintained over 15 °C–110 °C (temperature measured on the probe chuck). The reader is referred to [37] for detailed block-level measurement results including phase invariance in the face of supply and temperature variation.

G. Power Amplifier

The PA comprises three cascode stages, as shown in Fig. 6, with each stage providing up to 15 dB of gain. To maximize gain, the input of each stage is directly matched to the output of the driving stage avoiding an intermediate $50\text{-}\Omega$ transition. Each PA stage comprises a common emitter cascode amplifier with an inductive load, implemented using t-lines. While coplanar waveguide t-lines offer a lower quality factor than do coil inductors, their magnetic field can be better controlled using side and bottom shields. This superior field control minimizes parasitic magnetic coupling that might otherwise destabilize the high gain PA circuit. Each stage of the amplifier is coupled through a capacitor to the next stage for independent biasing, and is used to simultaneously provide resonant

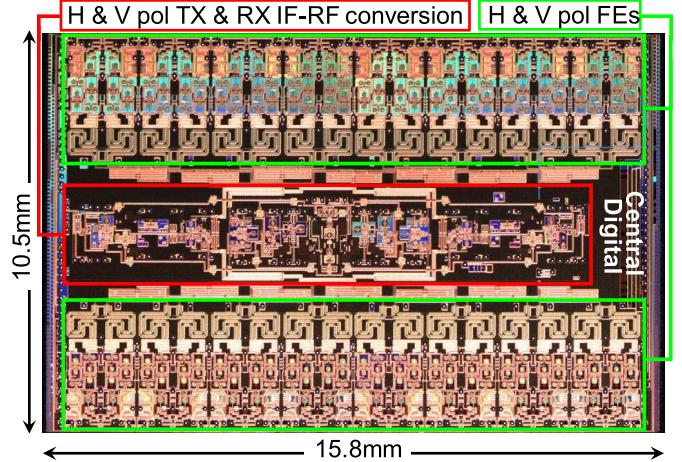


Fig. 9. Annotated die photograph of the IC implemented in 130-nm SiGe BiCMOS.

matching with the corresponding load inductor. The transistors and passive elements are sized to provide a maximum output 1-dB compression point for the lowest possible current consumption. This enables the PA to maintain linearity while achieving a small signal gain of up to 40 dB across the three stages. To minimize unwanted coupling between stages (thus assuring stability even at the highest gain settings), the layout of all BJTs in the PA are surrounded by substrate contacts to minimize substrate feedback, and low Q MOS capacitors are used extensively for supply and cascode bias decoupling.

H. Low-Noise Amplifier

The LNA consists of a single-ended inductively degenerated common emitter amplifier as the first stage, as shown in Fig. 6. This stage is followed by an active balun which uses the emitter and collector nodes of a bipolar transistor to produce a pseudo-differential signal. The high common mode rejection ratio of 37 dB (measured) in the following VGA stage shown in Fig. 6 produces well balanced differential signals. After the LNA first stage, the RX signal chain maintains differential signals.

IV. ARRAY LEVEL MEASUREMENT RESULTS

The 32TX 32RX IC is implemented in the Global Foundries 8HP 130-nm SiGe BiCMOS process (f_T/f_{MAX} of 200 GHz/280 GHz). The IC measures 15.8 mm by 10.5 mm, as shown in Fig. 9. The IC was characterized in three different scenarios as shown in Fig. 10:

- 1) on-wafer measurements using a probe card;
- 2) over the air measurements of the packaged IC in an antenna-in-package configuration;
- 3) measurements of the IC in a connectorized test package with a wired millimeter-wave interface.

A. Wafer Level IC Measurements

Wafer level measurements were performed on the antenna ports of three representative elements from nine different ICs on one wafer. As shown in Fig. 11, in TX mode the

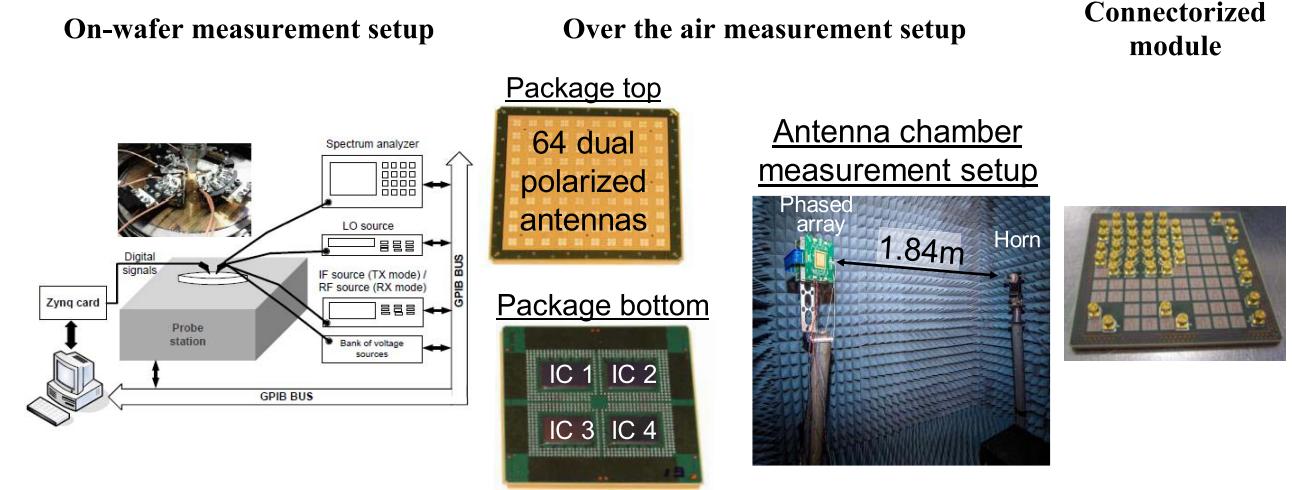


Fig. 10. Measurement setups for wafer probing measurement (left), over the air module measurement (center), and connectorized module (right).

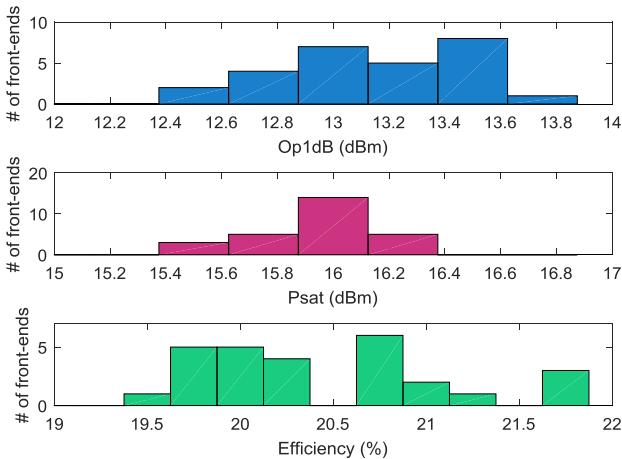


Fig. 11. Measured process variation of wafer level TX measurements across multiple ICs.

IC achieves a mean Op1dB of 13.5 dBm, a mean Psat of 16 dBm, and single-path mean gain of 32 dB, where measurements reflect chain performance from one IF input to one FE output. Each FE achieves ± 15 dB of gain control, including ± 4 dB of phase-invariant gain control. The measured peak PAE of the PA, including the switch and the LNA in its off state, is $> 20\%$, averaged across all 27 measured FEs. Fig. 12 shows the measured PAE of the PA, including the switch and LNA, across the 27 FEs at temperatures varying from 25 °C through 85 °C. The measured peak PAE peaks at 45 °C reaching 23% efficiency at Psat . In the RX mode, the IC achieves a mean gain of 32 dB, calculated as IF output / total input power at 16-LNA inputs. A phase invariant VGA provides ± 4 dB of phase-invariant gain control. These results are summarized in the left side of Table III.

A single representative IC was measured across temperature and supply variations. As shown in Table III, even though the full-chain gain in TX mode drops from 32 dB at 25 °C to 24 dB at 85 °C, TX linearity is maintained with no variation in either the Op1dB or Psat across this temperature range.

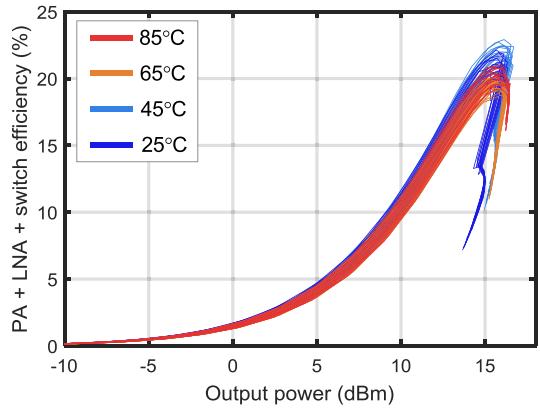


Fig. 12. Measured efficiency of the PA + switch + off-mode LNA at different output powers, measured across temperature.

The gain can be partially compensated using the TX IF-VGA which achieves 6 dB of gain control while maintaining linearity, as shown in Fig. 13(a). Moreover, as shown in Fig. 13(b), the PA bias can also be controlled to vary the measured TX gain while maintaining the TX linearity, further compensating for the loss of gain due to temperature increase.¹ In RX mode, the RX gain similarly drops from 34 to 28 dB across temperature, and can be compensated using either the IF-VGA or the RF phase invariant VGAs without affecting the NF or the linearity.

Fig. 14 shows the measured frequency response of the IC in TX mode showing single-path gain, Psat , and op1dB . As shown in Fig. 14, the IC achieves > 2 GHz bandwidth while maintaining linearity over a wide frequency range. Fig. 15 shows the measured PA efficiency, including the switch and off-mode LNA, with $> 20\%$ efficiency maintained over a > 2 GHz bandwidth. Fig. 16 shows the measured frequency response of the single-path gain in RX mode.

¹Note that changing the PA bias will change the phase shifts of the individual FEs. However, if the PA bias is simultaneously increased for all the identical FEs, the relative phase shifts among these matched FEs will be maintained, thereby retaining the beam-shape and pointing accuracy.

TABLE III
SUMMARY TABLE SHOWING THE PERFORMANCE OF THE IC AND SUB-BLOCKS (MEASURED ON WAFER)
AND ANTENNA MODULE WITH FOUR ICs (MEASURED OVER THE AIR)

On wafer					Antenna module w/ 4 ICs over the air	
Full IC performance						
	1 sample			27 samples μ / σ		
Temperature	25°C	65°C	85°C	25°C		
TX	Single-path gain ± Phase Invariant Gain Control (dB)	32 ±4.0	27 ±4.4	24 ±4.5	34 / 1.5 ± 4.0 / 0.2	Beam steering step (°) 1.4
	Single-path Op1dB (dBm)	14	14.1	13.9	13.5 / 0.4	Uncalibrated beam pointing RMS error with beam steering between ±30° (°) <1
	Single-path Psat (dBm)	16.4	16.6	16.2	16 / 0.2	Max. beam steering range ¹ (°) ±50
	PA+switch peak efficiency measured in full IC (%)	22.1	20.1	20.8	20.5 / 0.6	H to V isolation (dB) >30
	3dB BW (GHz)	2				TX linear power diss./IC/pol. (W) 4.6
	Op1dB/Psat variation across 360° phase control (dB)	<0.1	<0.2	<0.5		TX power diss. @Psat/IC/pol. (W) 5.1
	Op1dB/Psat variation across 8dB gain control (dB)	<0.1	<0.5	<2		RX power diss./IC/pol. (W) 3.3
RX	Single-path gain ± Phase Invariant Gain Control (dB)	34 ±4.0	31 ±4.4	28 ±4.5	35 / 0.6 ± 4.0 / 0.2	# of simultaneous beams per package 16-element 8
	3dB BW (GHz)	1.5				64-element 2
	Op1dB/Psat variation across 8dB gain control (dB)	<0.1	<0.5	<2		TX 64-element saturated EIRP /pol. (dBm) 54
	Op1dB/IC/pol. (dBm)					RX Op1dB/IC/pol. (dBm) 9.7
Sub-block performance						
LNA NF (dB)	3.7	4.1	4.3			
LNA + switch + off-mode PA NF (dB)	6.0	6.6	6.9			
TX/RX VGA gain control (dB)	8	8.8	9.1			
TX/RX VGA phase variation (°)	±1.5	±2	±1.5			
Phase shifter phase control (°)	210	210	210			
Phase shifter resolution (°)	4.9	4.9	4.9			
Phase shifter loss variation (dB)	±0.1	±0.2	±0.4			
RX front end Ip1dB (dBm)	-22.5	-21.5	-21.5			

¹ Sidelobe suppression >12dB w/ cal, w/o tapering

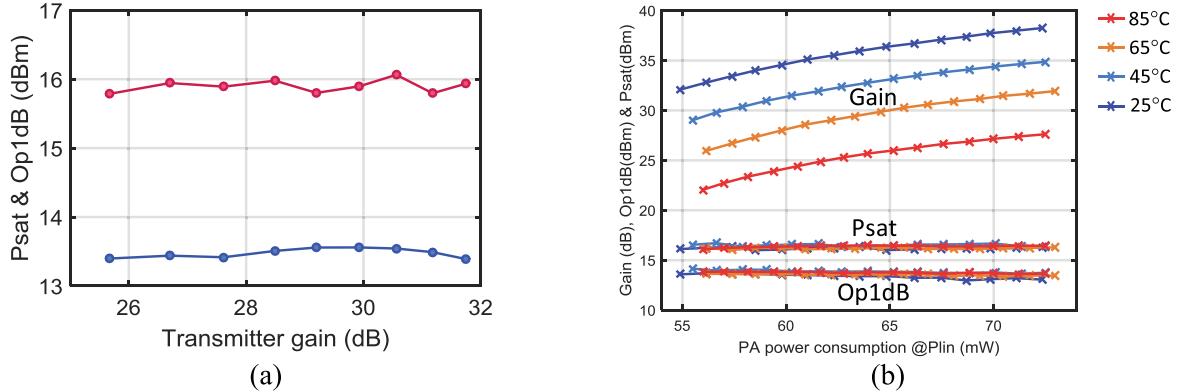


Fig. 13. (a) Measurement of Psat and Op1dB across gain control using the TX IF-VGA. (b) Measurement of Op1dB, Psat, and Gain versus PA power consumption in the linear operating region (Plin) for different PA last stage bias settings across 25 °C to 85 °C.

B. Over the Air Measurements of Antenna Module

Over the air measurements were performed using an antenna-in-package module incorporating four ICs and 64 dual polarized antennas [38], as shown in Fig. 10. The saturated

EIRP as the 64-elements are turned on is shown in Fig. 17. The turn-on characteristics closely match the expected theoretical EIRP of $20\log(\# \text{ of elements})$. With all 64-elements turned on, a saturated EIRP of 54 dBm is measured, representing

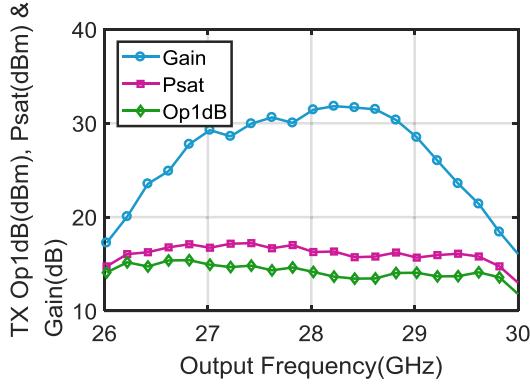


Fig. 14. Measured frequency response of the IC in TX mode showing single-path gain, saturated output power, and output 1-dB compression point.

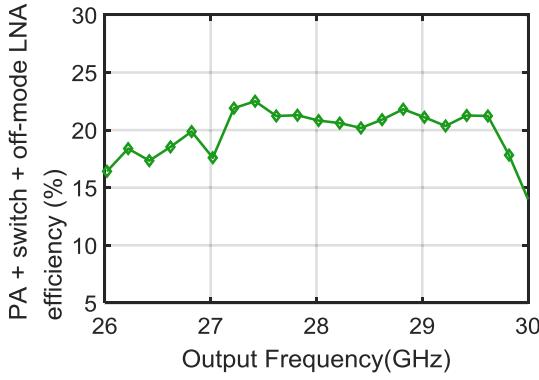


Fig. 15. Measured frequency response of the PA efficiency including the switch and off-mode LNA.

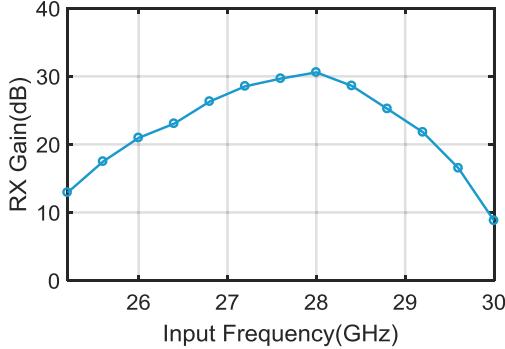


Fig. 16. Measured frequency response of the single-path gain in RX mode.

the highest saturated EIRP reported for a silicon-based packaged phased-array solution. A summary of the packaged IC measurements is tabulated in the right of Table III.

1) Gain Invariant Phase Control Measurements: The phase shifter was characterized after integration in the phased array by measuring the gain and phase shift of a single FE element over the air using a vector network analyzer (with a mixer for RF-IF conversion). The measured gain and phase shifts including the phase inversion from the 1-bit phase inverter are plotted in Fig. 18. For each phase inverter setting, the phase shifter provides 210° of phase control. The measured average phase step is 4.9° with rms phase error $<1.5^\circ$. The measured phase control in the FE is almost gain invariant (gain error ± 0.7 dB).

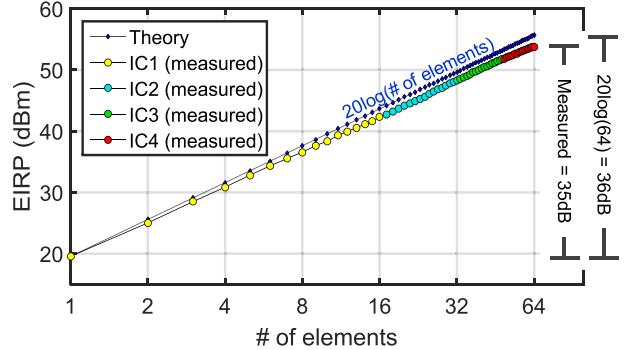


Fig. 17. Measured EIRP as a function of the number of elements turned on.

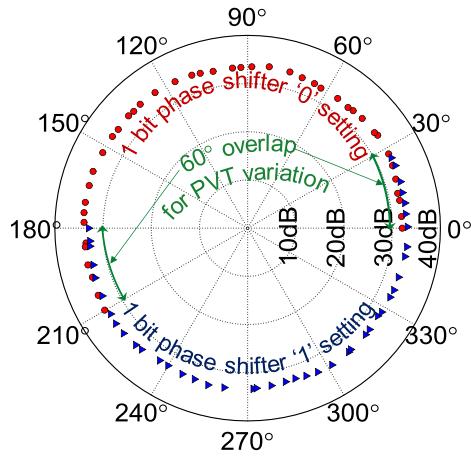


Fig. 18. Over the air measurement of gain invariant phase control demonstration for the full IC showing $<\pm 0.7$ -dB gain variation.

2) Phase-Invariant Gain Control Measurements: After integration into the phased array, the phase invariance of the VGA is measured using a two-element notch forming experiment. In Fig. 19, the measurement technique is illustrated and the measured results shown. The experiment consists of sweeping the phase of FE 2 while keeping FE 1 at a constant phase, measuring the resulting output power at multiple FE 2 VGA settings. With a constant loss phase shifter, a minimum is obtained at a relative phase of 180° (phase setting = 25 in this example), and the depth of the minimum varies depending on how close the relative amplitudes of FE 1 and FE 2 are. In this measurement, the setting for which the minimum is obtained is observed to remain unchanged, demonstrating the phase invariance of the VGA within half a phase shifter LSB step $\sim 2.5^\circ$.

3) Beamforming Measurements: Figs. 20–24 demonstrate the beamforming capabilities and performance of the packaged phased array. To demonstrate the accuracy of the phase and gain control, as well as the matching among elements, beamforming tests reported in this paper were made without gain or phase calibration, i.e., all FEs are assumed to have identical gain and phase settings for broadside beams; for beam steering, mathematically computed phase shifts for each FE were linearly translated to FE phase settings using the average phase shifter step of 4.9° . All beam measurements

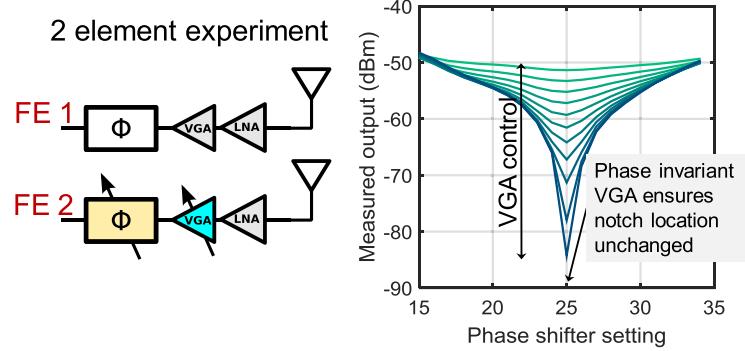


Fig. 19. Over the air measurement of phase-invariant gain control demonstration using two element notch forming with different VGA settings on the 2nd element. Varying notch depths at the same phase shifter setting proves VGA phase invariance.

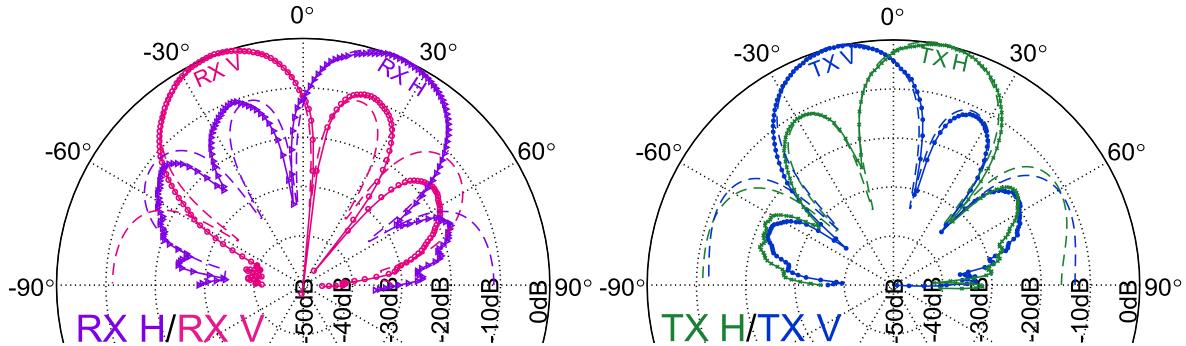


Fig. 20. Solid lines with markers showing different measured operating modes of the IC-package module with uncalibrated 16-element RX H/V beams pointed at $\pm 20^\circ$ respectively (left), and TX H/V beams pointed at $\pm 10^\circ$ respectively (right), using 1 IC. Superimposed dashed lines show the ideal mathematical patterns for comparison with the same angular resolution as the measurement setup. While the beams are shown to be symmetric in this example, they can be pointed independent of each other.

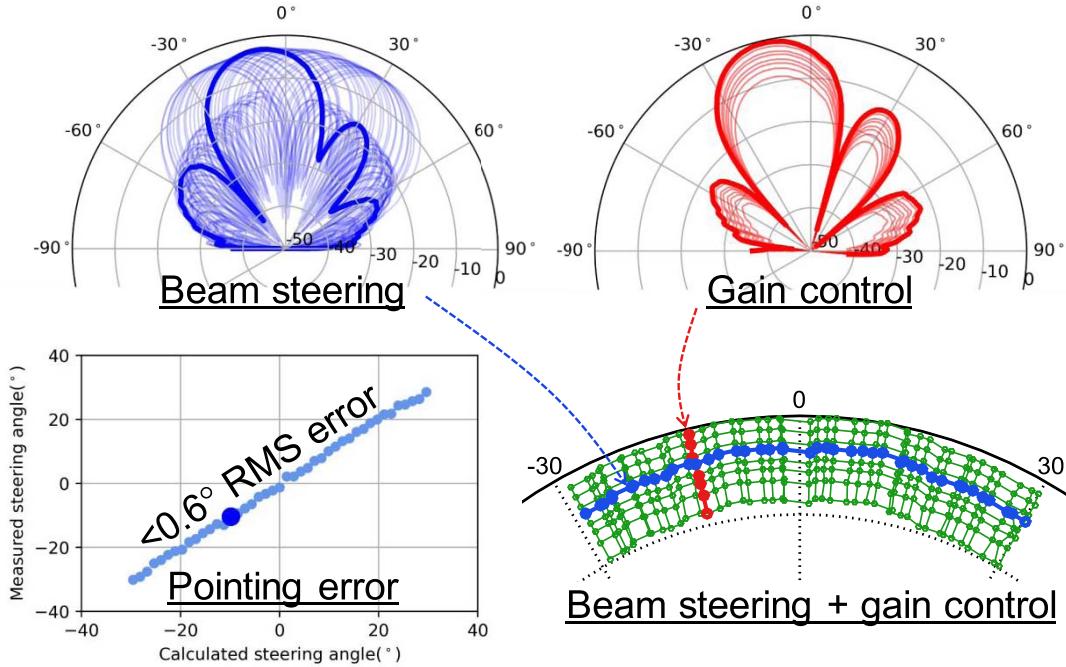


Fig. 21. Measured beam steering example at a fixed VGA setting (top left), and one gain control example at a fixed phase setting (top right). Uncalibrated steering angle versus calculation error (bottom left). Beam pointing directions for uncalibrated 16-element beam steering precision between $\pm 30^\circ$ with 8-dB VGA control (bottom right).

have an angular measurement resolution of 1° . Fig. 20 presents measured results showing different operating modes of the transceiver module. The IC can create two simultaneous

beams in both RX and TX modes. Fig. 20 shows four measured example beams: 16-element TX-H, 16-element TX-V, 16-element RX-H, and 16-element RX-V. Even without

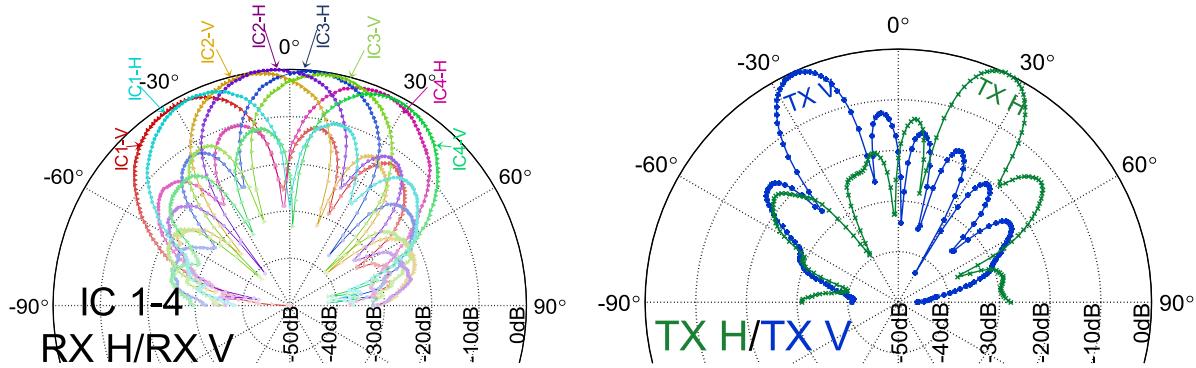


Fig. 22. Measured 8 simultaneous 16-element RX beams (left) and two simultaneous 64-element TX beams (right) using a 4-IC module, without requiring calibration.

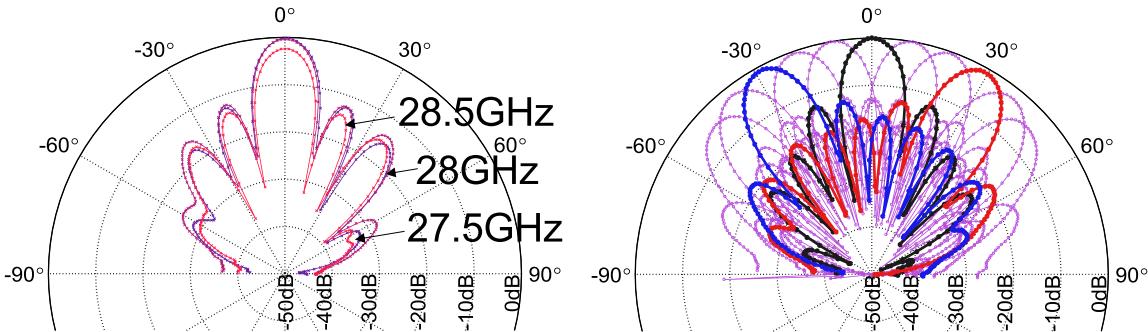


Fig. 23. Measured 64-element TX H beam pattern measurements across frequency at 27.5, 28, and 28.5 GHz (left) and 64-element TX V beam steering measurements from -50° to 50° in steps of 10° achieving at least 10-dB sidelobe suppression without applying any tapering.

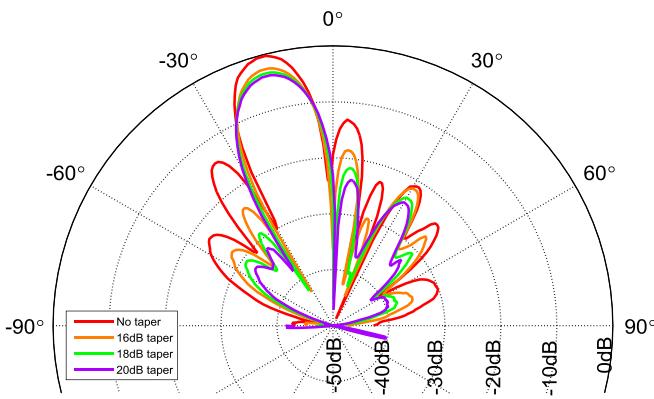


Fig. 24. Measured tapering of the 64-element phased array without requiring calibration.

calibration, up to 50-dB-deep notches are obtained with nearly ideal sidelobe levels, beam widths, and other beam characteristics. For comparison, ideal beams are shown with dashed lines in Fig. 20. To compare the expected notch depth with the measured notch depth, the same 1° angular resolution has been used for the ideal beams as is used for the beam measurements. As seen from Fig. 20, similar notch depths are obtained in measurement as is obtained with ideal beams in software with a 1° resolution demonstrating a near ideal IC and package solution, even without calibration. Beam steering over a range of $\pm 30^\circ$ is demonstrated in each of these modes, with $<1^\circ$ rms beam pointing error achieved.

Fig. 21 shows beam steering using uniform phase gradients in the phased array, demonstrating 1.4° beam steering resolution across a range of $\pm 30^\circ$, as expected from

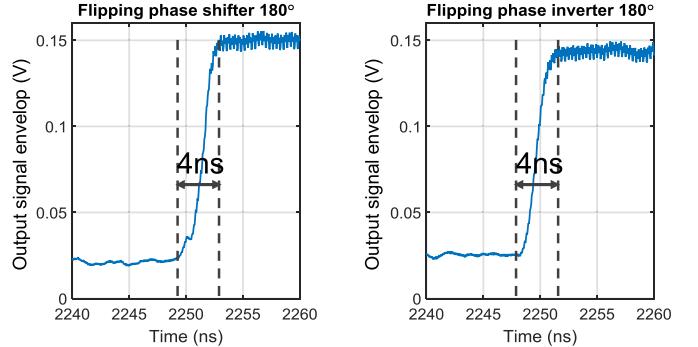


Fig. 25. Measured beam switching speed using either phase shifter and phase inverter.

theory [Fig. 4(a)]. As shown in the bottom right plot in Fig. 21, each data point along a given arc on the polar plot slice represents a beam pointing direction. Phase invariant FE gain control is used to change the beam gain over a 9-dB range, represented by the data points on the radial axis. The 43 different 16-element beams along one example arc are shown in the top left plot in Fig. 21. Gain control on one of these beams is shown in the top right plot in Fig. 21. Without any gain or phase calibration, the error across all directions and gain settings for this measurement is only 0.6° rms, as shown in the bottom left plot in Fig. 21.

Since each IC supports two simultaneous beams, each package housing four ICs can support eight simultaneous 16-element beams, as shown in Fig. 22 (left). Moreover, the ICs can be configured to form two simultaneous 64-element beams, as shown in Fig. 22 (right).

TABLE IV
SUMMARY OF INTEGRATED TRX PHASED ARRAYS FROM 28–100 GHz DEMONSTRATED WITH ON-CHIP OR IN-PACKAGE ANTENNAS

Reference	[11]		[6]	[4, 8]	[7]	[13]	[14]	[39]	[40]	[41]	This work
Frequency (GHz)	60		60	94	60	70–100	94	29	29	28	28
Elements per chip	8TX 32RX	32TX 4RX	32TRX	16TRX + 16RX	16TRX	16TX 4RX	4TX 4RX	4TRX	4TRX	8TRX	32TRX
Elements in package	8TX 32RX	32TX 4RX	32TRX	64TRX + 64RX	16TRX	16TX 4RX	4TX 4RX	32TRX	4TRX	8TRX	128TRX
Concurrent TX polarizations	1		1	1	1	1	1	1	1	1	2
Concurrent RX polarizations	1		1	2	1	1	1	1	1	1	2
Phase resolution (°)	—		90	11	5.6	22.5	9	5.6	5.6	45	5
RMS phase error (°)	—		6	3	—	—	—	6	6	7	0.8
TX P _{sat} (dBm) per element	—		3	2.5	8	8	6.4	<13*	—	10.5	16
TX Op1dB (dBm) per element	9		-3.5	-2	5.2	—	—	<11.7*	10.5	—	13.5
TX total power diss. / # of elements (mW)	112.5	56.9	37.5	168.8	74.4	343.8	105	200	200	85	143.8
RX total power diss. / # of elements (mW)	39.1	177.5	26.6	106.3	60	1125	90	130	105	50	103.1
Peak TX efficiency (total chip output power / dissipated power) (%)	—	—	5.3	0.9	<8.5	<1.8	4.1	7.4	5.6	13.2	13.8
TX EIRP per package per pol. @Psat (dBm)	—	28	32	—	27	34	22	41	—	31.5	54
Die area (mm ²)	77.1	72.64	29	44	26.3	24.5	7.4	11.7	11.7	7.3	166
Technology (nm)	65 CMOS		90nm CMOS	130nm SiGe	40nm CMOS	180nm SiGe	130nm SiGe	180nm SiGe	180nm SiGe	28nm CMOS	130nm SiGe
Integration level	Antenna in package		Antenna in package	Antenna in package	Package and MAC	Antenna on PCB	Antenna on PCB	Antenna on PCB	Antenna on PCB	Antenna in package	Antenna in package

* Measured on PA only

Beam measurements were taken across frequencies. As shown in Fig. 23 (left), the beam shape is maintained across frequencies. On the right of Fig. 23, beam steering across $\pm 50^\circ$ is shown with sidelobe suppression below 10 dB before applying tapering.

A Taylor window tapering function was applied by changing the gain of each FE’s VGA. As shown in Fig. 24, the phase invariance property of the VGA gain control enables sidelobe suppression up to 20 dB, without any significant change in the beam pointing direction. Again, no gain or phase calibration was applied during the tapering measurement.

C. Connectorized Package Measurements

Beam switching and RX \leftrightarrow TX switching measurements were performed using the connectorized test package

shown in Fig. 10. For the beam switching experiment, the FE phases are switched such that the combined output changes from a state of destructive interference to a state of constructive interference. The rise time of the combined output signal captures the beam switching speed of the phased array. As seen in Fig. 25, the measured beam switching speed is ~ 4 ns for both mechanisms of phase control—the t-line-based passive phase shifter and the active cascode-based phase inverter. TX \leftrightarrow RX switching speeds of < 100 ns were observed as shown in Fig. 26 for both switching events.

D. System Level Link Measurements

For initial system level measurements, two antenna modules were integrated with a baseband into a prototype picocell radio unit. This radio unit was then used to communicate with

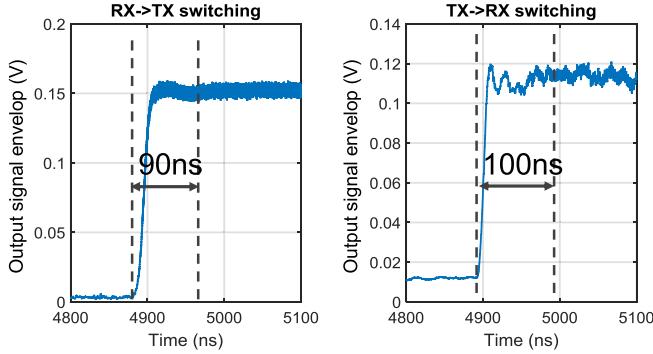


Fig. 26. RX \leftrightarrow TX switching speed measured using the connectorized module.

a prototype 28-GHz user equipment antenna at a distance of a few meters. Using four 64-element beams from the two antenna modules, and using eight 100-MHz channels with 256QAM modulation at 28 GHz, a data rate of 20.64 Gbps has been achieved providing 5.16 Gbps per beam.

V. CONCLUSION

Silicon-based millimeter-wave transceivers and phased arrays have matured, and telecom providers are considering utilizing millimeter-wave frequencies for mass deployment in cellular systems. This paper is the first demonstration of a 5G millimeter-wave phased-array module based on silicon ICs. Furthermore, for the first time, we have demonstrated simultaneous dual polarized beams in both TX and RX. Beam steering control with orthogonal phase and amplitude control has been developed and demonstrated. A circuit technique has been introduced to minimize the TX losses and improve TX mode efficiency. We have demonstrated an advancement in beam steering and tapering precision without the need for element to element calibration. Extensive measurements across process and temperature prove the suitability of this design for 5G cellular communications.

This phased-array performance has been compared with other millimeter-wave silicon-based packaged phased-array transceivers in Table IV. As seen in rows 4 and 5, this paper presents the first demonstration of a fully integrated dual polarized transceiver for millimeter-wave phased arrays. Moreover, this phased-array IC integrates the most number of elements per IC (32 TRX) and the most number of elements per package (128 TRX), and achieves the highest oP1dB per element, the highest saturated EIRP per package, the lowest phase resolution and rms phase error, and the highest peak TX efficiency. When compared to three other 28-GHz phased arrays [39]–[41] published since this work was first presented [17], this paper achieves $>4 \times$ # of elements, $<6 \times$ lower phase error, >13 dB higher saturated EIRP, >3 dB higher Psat and Op1dB, and achieves the highest TX efficiency. We expect that the demonstrated phased-array advancement will not only impact millimeter-wave mobile communication systems, but also open new opportunities for imaging applications, and for the development of complex and adaptive multi-function systems.

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REFERENCES

- [1] J. G. Andrews *et al.*, "What will 5G be?" *IEEE J. Sel. Areas Commun.*, vol. 32, no. 6, pp. 1065–1082, Jun. 2014.
- [2] W. Roh *et al.*, "Millimeter-wave beamforming as an enabling technology for 5G cellular communications: Theoretical feasibility and prototype results," *IEEE Commun. Mag.*, vol. 52, no. 2, pp. 106–113, Feb. 2014.
- [3] T. S. Rappaport *et al.*, "Millimeter wave mobile communications for 5G cellular: It will work!" *IEEE Access*, vol. 1, pp. 335–349, 2013.
- [4] X. Gu, A. Valdes-Garcia, A. Natarajan, B. Sadhu, D. Liu, and S. K. Reynolds, "W-band scalable phased arrays for imaging and communications," *IEEE Commun. Mag.*, vol. 53, no. 4, pp. 196–204, Apr. 2015.
- [5] C. Guo, F. Liu, S. Chen, C. Feng, and Z. Zeng, "Advances on exploiting polarization in wireless communications: Channels, technologies, and applications," *IEEE Commun. Surveys Tuts.*, vol. 19, no. 1, pp. 125–166, 1st Quart., 2017.
- [6] E. Cohen, M. Ruberto, M. Cohen, O. Degani, S. Ravid, and D. Ritter, "A CMOS bidirectional 32-element phased-array transceiver at 60 GHz with LTCC antenna," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 3, pp. 1359–1375, Mar. 2013.
- [7] M. Boers *et al.*, "A 16TX/16RX 60 GHz 802.11ad chipset with single coaxial interface and polarization diversity," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 3031–3045, Dec. 2014.
- [8] A. Valdes-Garcia *et al.*, "A fully-integrated dual-polarization 16-element W-band phased-array transceiver in SiGe BiCMOS," in *Proc. IEEE RFIC*, Jun. 2013, pp. 375–378.
- [9] A. Valdes-Garcia *et al.*, "A fully integrated 16-element phased-array transmitter in SiGe BiCMOS for 60-GHz communications," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2757–2773, Dec. 2010.
- [10] A. Natarajan *et al.*, "A fully-integrated 16-element phased-array receiver in SiGe BiCMOS for 60-GHz communications," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 1059–1075, May 2011.
- [11] S. Emami *et al.*, "A 60 GHz CMOS phased-array transceiver pair for multi-Gb/s wireless communications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2011, pp. 164–168.
- [12] B.-H. Ku, O. Inac, M. Chang, H.-H. Yang, and G. M. Rebeiz, "A high-linearity 76–85-GHz 16-element 8-transmit/8-receive phased-array chip with high isolation and flip-chip packaging," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 10, pp. 2337–2356, Oct. 2014.
- [13] S. Shahramian, M. J. Holyoak, and Y. Baeyens, "A 16-element W-band phased array transceiver chipset with flip-chip PCB integrated antennas for multi-gigabit data links," in *Proc. IEEE RFIC*, May 2015, pp. 27–30.
- [14] A. Townley *et al.*, "A 94 GHz 4TX-4RX phased-array for FMCW radar with integrated LO and flip-chip antenna package," in *Proc. IEEE RFIC*, May 2016, pp. 294–297.
- [15] V. Vidjakovic *et al.*, "A low-power radio chipset in 40 nm LP CMOS with beamforming for 60 GHz high-data-rate wireless communication," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 236–237.
- [16] S. Zahir, O. D. Gurbuz, A. Karroy, S. Raman, and G. M. Rebeiz, "A 60 GHz single-chip 256-element wafer-scale phased array with EIRP of 45 dBm using sub-reticle stitching," in *Proc. IEEE RFIC*, May 2015, pp. 23–26.
- [17] B. Sadhu *et al.*, "A 28 GHz 32-element phased-array transceiver IC with concurrent dual polarized beams and 1.4 degree beam-steering resolution for 5G communication," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2017, pp. 128–129.
- [18] H. Hashemi, X. Guan, and A. Hajimiri, "A fully integrated 24 GHz 8-path phased-array receiver in silicon," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2004, pp. 390–391.
- [19] B. Floyd, S. Reynolds, U. Pfeifer, T. Beukema, J. Grzyb, and C. Haymes, "A silicon 60 GHz receiver and transmitter chipset for broadband communications," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2006, pp. 649–658.

- [20] B. Sadhu *et al.*, "A 60 GHz packaged switched beam 32 nm CMOS TRX with broad spatial coverage, 17.1 dBm peak EIRP, 6.1 dB NF at < 250 mW," in *Proc. IEEE RFIC*, San Francisco, CA, USA, May 2016, pp. 342–343.
- [21] A. Tomkins *et al.*, "A 60 GHz, 802.11ad/WiGig-compliant transceiver for infrastructure and mobile applications in 130 nm SiGe BiCMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2239–2255, Oct. 2015.
- [22] N. Saito *et al.*, "A fully integrated 60-GHz CMOS transceiver chipset based on WiGig/IEEE 802.11ad with built-in self calibration for mobile usage," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3146–3159, Dec. 2015.
- [23] K. Okada *et al.*, "Full four-channel 6.3-Gb/s 60-GHz CMOS transceiver with low-power analog and digital baseband circuitry," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 46–65, Jan. 2013.
- [24] *IEEE Standard for Information Technology—Local and Metropolitan Area Networks—Specific Requirements—Part 15.3: Amendment 2: Millimeter-Wave-Based Alternative Physical Layer Extension*, IEEE Standard 802.15.3c-2009, 2009.
- [25] *IEEE Draft Standard for Information Technology—Telecommunications and Information Exchange Between Systems—Local and Metropolitan Area Networks—Specific Requirements—Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications*, IEEE Standard P802.11aq/013.0, Oct. 2017.
- [26] S.-K. Yong, P. Xia, and A. Valdes-Garcia, *60 GHz Technology for Gbps WLAN and WPAN: From Theory to Practice*. Hoboken, NJ, USA: Wiley, 2010.
- [27] R.-A. Pitaval, O. Tirkkonen, R. Wichman, K. Pajukoski, E. Lahetkangas, and E. Tirola, "Full-duplex self-backhauling for small-cell 5G networks," *IEEE Wireless Commun.*, vol. 22, no. 5, pp. 83–89, Oct. 2015.
- [28] A. Hajimiri, A. Komijani, A. Natarajan, R. Chunara, X. Guan, and H. Hashemi, "Phased array systems in silicon," *IEEE Commun. Mag.*, vol. 42, no. 8, pp. 122–130, Aug. 2004.
- [29] S. Kalia, S. A. Patnaik, B. Sadhu, M. Sturm, M. Elbadry, and R. Harjani, "Multi-beam spatio-spectral beamforming receiver for wideband phased arrays," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 8, pp. 2018–2029, Aug. 2013.
- [30] C. A. Balanis, *Antenna Theory: Analysis and Design*. Hoboken, NJ, USA: Wiley, Feb. 2016.
- [31] S. Chang, W. Hong, and J. Oh, "Quantization effects of phase shifters on 5G mmWave antenna arrays," in *Proc. IEEE Int. Symp. Antennas Propag. USNC/URSI Nat. Radio Sci. Meet.*, Vancouver, BC, Canada, Jul. 2015, pp. 2119–2120.
- [32] P. Song, R. L. Schmid, A. C. Ulusoy, and J. D. Cressler, "A high-power, low-loss W-band SPDT switch using SiGe PIN diodes," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Tampa, FL, USA, Jun. 2014, pp. 195–198.
- [33] W. H. Woods, A. Valdes-Garcia, H. Ding, and J. Rascoe, "CMOS millimeter wave phase shifter based on tunable transmission lines," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2013, pp. 1–4.
- [34] Y. Tousi and A. Valdes-Garcia, "A Ka-band digitally-controlled phase shifter with sub-degree phase precision," in *Proc. IEEE RFIC*, May 2016, pp. 356–359.
- [35] A. Natarajan, A. Valdes-Garcia, B. Sadhu, S. K. Reynolds, and B. D. Parker, "W-band dual-polarization phased-array transceiver frontend in SiGe BiCMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 6, pp. 1989–2002, Jun. 2015.
- [36] M.-D. Tsai and A. Natarajan, "60 GHz passive and active RF-path phase shifters in silicon," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Boston, MA, USA, Jun. 2009, pp. 223–226.
- [37] B. Sadhu, J. F. Bulzacchelli, and A. Valdes-Garcia, "A 28 GHz SiGe BiCMOS phase invariant VGA," in *Proc. IEEE RFIC*, May 2016, pp. 150–153.
- [38] X. Gu *et al.*, "A multilayer organic package with 64 dual-polarized antennas for 28 GHz 5G communication," in *Proc. IEEE IMS*, Jun. 2017, pp. 1899–1901.
- [39] K. Kibaroglu, M. Sayginer, and G. M. Rebeiz, "An ultra low-cost 32-element 28 GHz phased-array transceiver with 41 dBm EIRP and 1.0–1.6 Gbps 16-QAM link at 300 meters," in *Proc. IEEE RFIC*, Honolulu, HI, USA, Jun. 2017, pp. 73–76.
- [40] K. Kibaroglu, M. Sayginer, and G. M. Rebeiz, "A quad-core 28–32 GHz transmit/receive 5G phased-array IC with flip-chip packaging in SiGe BiCMOS," in *Proc. IEEE IMS*, Jun. 2017, pp. 1892–1894.
- [41] H.-T. Kim *et al.*, "A 28 GHz CMOS direct conversion transceiver with packaged antenna arrays for 5G cellular system," in *Proc. IEEE RFIC*, Honolulu, HI, USA, Jun. 2017, pp. 69–72.



Bodhisatwa Sadhu (S'08–M'12) received the B.E. degree in electrical and electronics engineering from the Birla Institute of Technology and Science (BITS), Pilani, India, in 2007, and the Ph.D. degree in electrical engineering from the University of Minnesota, Minneapolis, MN, USA, in 2012, focused on cognitive radio circuits.

Since 2012, he has been with IBM T. J. Watson Research involved in RF and millimeter-wave transceivers and frequency synthesizers, where he has led the design and demonstration of a self-healing 25-GHz low noise frequency synthesizer, a low-power switched beam 60-GHz CMOS transceiver IC for 802.11ad communications, and the first reported silicon-based 28-GHz phased array base-station IC for 5G communications. He is currently a Research Staff Member with the IBM T. J. Watson Research Center, RF Communication Systems Group, Yorktown Heights, NY, USA, and an Adjunct Assistant Professor with Columbia University, New York City, NY, USA. He has authored or co-authored 13 journal papers, 21 conference papers, the book *Cognitive Radio Receiver Front-Ends—RF/Analog Circuit Techniques* (Springer, 2014), several book chapters, and has 17 issued U.S. patents with 20+ pending.

Dr. Sadhu was a recipient of the BITS Pilani Silver Medal (university second rank across all disciplines) in 2007, the University of Minnesota Graduate School Fellowship in 2007, 3M Science and Technology Fellowship in 2009, the University of Minnesota Doctoral Dissertation Fellowship in 2011, five IBM Patent Plateau Awards, and the two IBM A-level Accomplishment Awards in 2016. He stood second in India in the Indian School Certificate examination (national high school examination) in 2003. He serves as a member of the Technical Program Committee of the IEEE Radio Frequency Integrated Circuits Symposium and Compound Semiconductor Integrated Circuit Symposium, and the Secretary of the IEEE NY EDS/SSCS chapter.



Yahya Tousi received the Ph.D. degree from the Department of Electrical and Computer Engineering, Cornell University, Ithaca, NY, USA, in 2012.

He was with SiTune Corporation, where he focused on wideband satellite receivers. In 2014, he joined the IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, to develop the next generation of millimeter-wave phased array transceivers for wireless communication systems. Since 2017, he has been a Member with the Faculty of Electrical and Computer Engineering, University of Minnesota, Minneapolis, MN, USA. His current research interests include high performance integrated circuits and novel architectures for millimeter-wave and terahertz systems with applications in communication, sensing, and healthcare.

Prof. Tousi was a recipient of the 2009 Cornell Jacob Fellowship, the 2011 IEEE Microwave Theory and Techniques Society Graduate Fellowship, and the 2011–2012 IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award.



Joakim Hallin received the M.Sc. degree in engineering physics and the Ph.D. degree in theoretical physics from the Chalmers University of Technology, Gothenburg, Sweden, in 1996 and 1991, respectively.

He completed Post-Doctoral Research with the University of British Columbia, Vancouver, BC, Canada. He was with Ericsson, where he involved in digital filter design and antenna research. He has been with Optillion focusing on > 100 Gb/s electro-optical communication systems, doing research with Chalmers University of Technology, microwave laboratory doing research on > 100Gb/s InP DHBT integrated circuit development publishing a number of papers, managing fingerprint sensor technology at Fingerprint Cards and doing microwave/millimeter wave RFIC design with Ericsson. He is currently an Experienced RFIC Designer with Ericsson, Sweden. He has authored a number of papers in quantum field theory.



Stefan Sahl received the M.S. degree in electrical engineering from KTH, Stockholm, Sweden, in 1993.

He was with Allgon and Ericsson, Kista, Sweden, involved in radio and analog design, from 1996 to 2000 and 1993 to 1996, respectively. He was with Infineon and Zarling Semiconductor, where he focused on RFIC design, from 2000 to 2003 and 2004 to 2007, respectively. He is currently a Senior Specialist RF ASIC Strategy with Ericsson.



Scott K. Reynolds received the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, USA, in 1988.

He joined IBM in 1988, where he involved in a wide variety of IBM products, including ICs for disk drive channels, electrical and optical I/O, and RF communication. In 2003, he was involved in the development of silicon millimeter-wave ICs and packaging for high-data-rate wireless links and other applications, including imaging. He was with IBM Research, where he went to manage the RF Circuits

and Systems Group from 2010 to 2013. In 2013, he left IBM to start his own business, Tavish Design, LLC. He continues to consult for IBM on millimeter-wave IC design and packaging. He has authored or co-authored many technical publications, including two papers on 60-GHz wireless transceiver circuits which won the Best Paper Awards at ISSCC in 2004 and 2006 and holds more than 30 U.S. patents.



Nadav Mazor received the B.Sc. degree in electrical and computer engineering from Ben Gurion University, BeerSheva, Israel, in 2010, and the M.Sc. degree from the Physical Electronics Department, Faculty of Engineering, Tel-Aviv University, Tel-Aviv, Israel, in 2013.

He has been with the IBM Haifa Research Labs, Millimeter-Wave Technology Group, Israel, where he was involved in designing of backhaul and 5G Cellular SiGe ICs, from 2012 to 2016. In 2016, he joined Vayyar Imaging Ltd., Yehud, Israel, where he

is a part of the RFIC Research and Development Team, designing imaging sensors with the millimeter waves for various applications such as breast cancer detection, stud finding, and many more. His current research interests include designing and modeling of wide band millimeter-wave IC frequency multipliers for communication and imaging applications.



Bo Bokinge received the M.S. degree in electrical engineering from the Institute of Technology, Linköping University, Linköping, Sweden, in 1978.

He was with Ericsson in 1978 and held numerous positions within analog and digital IC design units. Between 2002 and 2008, he was with Infineon. In 2008, he joined Ericsson where he, up to his retirement in 2017, involved in IC designs in the RF and microwave area.

Gustaf Weibull is currently an Engineer with the Ericsson, Göteborg, Sweden.

Håkan Bengtsson is currently an Engineer with the Ericsson, Sweden.



Anders Carlinger received the M.Sc. degree in electrical engineering from the KTH Royal Institute of Technology, Stockholm, Sweden, in 1989.

Since 1990, he has been with the Ericsson, Kista, Sweden, where he is currently an RF-IC Engineer. His current research interests include analog radio and RF-IC design for mobile communication systems, with a special interest in transmitter linearization.



Eric Westesson was born in Nässjö, Sweden, in 1973. He received the M.Sc. degree in electrical engineering from Lund University, Lund, Sweden, in 1998.

In 1998, he joined the Department of Applied Electronics, Lund University as a Ph.D. Student, where he was involved in the linearization of RF power amplifiers. In 2001, he joined the Ericsson Mobile Platforms (later ST-Ericsson and Ericsson Modems), where he was involved design for the cellular handset industry. Since 2014, he has been with the Ericsson Radio, Lund, where he is involved in RFIC design for millimeter-wave infrastructure.



Jan-Erik Thillberg received the M.Sc. degree in electrical engineering from the Royal Institute of Technology (KTH), Stockholm, Sweden, in 1987.

He was with the Ericsson Hardware Research Organization, where he was involved in the early 5G development. He has held various positions with the Ericsson within systems management and product management related to 1G, 2G, 3G, and 4G wireless systems development. He is currently a Technical Leader with the Ericsson Radio Product Development Organization, where he was involved in the commercial development of 5G products. His current research interests include radio architecture and radio technology.



Örjan Renström (M'99) received the M.S. degree in electrical engineering from the Royal Institute of Technology, Stockholm, Sweden, in 1992.

From 1987 to 2004, he was with the Ericsson, Stockholm. Between 2004 and 2013, he was with Kisel Microelectronics, Stockholm; SiRF Technology, Stockholm; and Huawei, Stockholm. Since 2013, he has been with the Ericsson. He is currently involved in RF-IC for mobile communication infrastructure applications.



Kristoffer Sjögren received the M.Sc. degree in physics with main field in wireless communication from the Chalmers University of Technology, Gothenburg, Sweden, in 2010.

After graduation, he was with Ericsson before he joined the Ericsson 5G development in 2014, where he was involved in high-frequency packaging techniques. From 2014 to 2017, he was involved in the evolution of Ericsson's 28 GHz 5G phased array wireless transceiver solution. He is currently with Sivers IMA, Kista, Sweden, developing a 57–71-GHz beam-steering all-integrated 802.11ad solution.



Olov Haapalahti received the M.Sc. degree in electrical engineering from the Luleå University of Technology, Luleå, Sweden, in 1999.

He was a Monolithic Microwave Integrated Circuit Design Engineer with the Ericsson Microwave Systems, from 1999 to 2002, and he was a Transceiver Board Radio Designer with Ericsson, Gothenburg, Sweden, from 2002 to 2006. He is currently an RF-ASIC Design Engineer with Ericsson, Kista, Sweden. His current research interests include analog radio and microwave ASIC design, covering Bi-CMOS, GaAs as well as GaN.



Leonard Rexberg received the M.Sc., M.Lic., and Ph.D. degrees from the Chalmers University of Technology, Göteborg, Sweden, in 1984, 1988, and 1991, respectively. His Ph.D. thesis was focused on radiation from planar antenna structures embedded in stratified dielectric layers.

Since 1995, he has been with the Ericsson AB Company, Stockholm, Sweden, where he is currently an Expert in radio algorithms. He has numerous patents in the area of antenna design and also in digital algorithms for signal correction such as DPD and CFR. He has a special interest in adaptive antenna and multi-in multi-out systems and has been involved in numerous research and development projects within this area from 1G analog telecommunication systems to the present digital 5G systems.



Mark Yeck received the B.S. degree in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, PA, USA.

He developed FPGA, DSP, and embedded systems in the fields of audio and motion control. He has been with IBM, where responsible for digital design and synthesis for monolithic phased arrays, FPGA design for RF transceiver control, digital test of SiGe and CMOS millimeter-wave transceivers, and FPGA design for high performance computing systems. He is currently with the IBM T.J. Watson Research Center, Yorktown Heights, NY, USA.



Xiaoxiong Gu (M'07–SM'12) received the Ph.D. degree in electrical engineering from the University of Washington, Seattle, WA, USA, in 2006.

He joined IBM Research as a Research Staff Member in 2007. His current research interests include 5G radio access technologies, optoelectronic and mm-wave packaging, electrical designs, modeling and characterization of communication, and computation systems. He was recently involved in antenna-in-package design and integration for mm-wave imaging and communication systems including *K*-band, V-band, and W-band phased-array modules. He has authored and co-authored over 70 technical papers and holds eight issued patents.

Dr. Gu received the Best Session Paper Award at IEEE ECTC in 2007, the IEC DesignCon Paper Awards in 2008 and 2010, the Best Interactive Session Paper Award from the IEEE DATE in 2008, the Best Conference Paper Award from the IEEE EPEPS in 2011, the IBM Plateau Invention Awards in 2012–2016, respectively, the IEEE EMC Symposium Best Paper Award in 2013, the SRC Mahboob Khan Outstanding Industry Liaison Awards in 2012 and 2014, and the IBM Outstanding Technical Achievement Award in 2016. He is the Co-Chair of the Professional Interest Community on Computer System Designs at IBM. He has been serving on the technical program committees for numerous IEEE conferences including IMS, EPEPS, ECTC, EDAPS, and DesignCon.



Mark Ferriss received the B.E. degree from the University College Cork, Cork, Ireland, in 1998 and the Ph.D. degree from the University of Michigan, Ann Arbor, MI, USA, in 2008.

From 1998 to 2002, he was with the Analog Devices, Ireland. Since 2009, he has been with IBM's T.J. Watson Research Center, Yorktown Heights, NY, USA.



Duixian Liu (F'10) is currently with the IBM T. J. Watson Research Center, Yorktown Heights, NY, USA.

He has designed antennas ranging from 3 to 240 GHz for the past 27 years, and concentrated on millimeter-wave antenna-in-package designs for phased array application for the past 14 years. He has edited or co-edited two books, written two book chapters, published more than 110 papers, and had 80 patents issued or pending.

Mr. Liu was a recipient of the three IBM's Outstanding Technical Achievement Awards, one Corporate Award, and the 2012 S. A. Schelkunoff Prize Paper Award of the AP Society. He was named as Master Inventor in 2007. He was an Associate Editor for the AP Transactions for 9 years, a Guest/Track Editor for three AP Transactions Special Issues, and.



Daniel Friedman received the Ph.D. degree from Harvard University, Cambridge, MA, USA, in 1992.

He subsequently completed Post-Doctoral research at Harvard and consulting work at MIT Lincoln Laboratory, Lexington, MA, USA, broadly in the area of image sensor design. In 1994, he joined IBM, where he initially developed field-powered RFID tags before turning to high data rate wireline and wireless communication. He is currently the Senior Manager of the Communication Circuits and Systems Department, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA. He has authored or co-authored more than 75 publications. He holds more than 50 patents. His current research interests include high-speed I/O design, PLL design, millimeter-wave circuits and systems, and circuit/system approaches to enabling new computing paradigms.

Dr. Friedman was a co-recipient of the Beatrice Winner Award for Editorial Excellence at the 2009 ISSCC and the 2009 JSSC Best Paper Award given in 2011. He was a member of the BCTM Technical Program Committee from 2003 to 2008 and the ISSCC International Technical Program Committee from ISSCC 2009 to ISSCC 2016; he served as the Wireline Sub-Committee Chair from ISSCC 2012 through ISSCC 2016 and has been serving as the Short Course Chair since ISSCC 2017.



Alberto Valdes-Garcia (S'00–M'06–SM'13) received the B.S. degree (Hons.) in electronic systems engineering from the Monterrey Institute of Technology, Monterrey, Mexico, in 1999, and the Ph.D. degree in electrical engineering from Texas A&M University, College Station, TX, USA, in 2006.

In 2000, he joined the Motorola Broadband Communications, as an RF Design Engineer. In 2006, he joined the IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, as a Research Staff Member, where he co-developed millimeter-wave power amplifiers, transmitters, phased arrays, self-healing circuits, and sub-system demonstrations with millimeter-wave modules. He was also involved in the development of carbon-based electronics and co-developed the world's first graphene integrated circuit (*Science*, 2011). In 2013, he joined IBM Research, as the Manager of the RF Circuits and Systems Group. In this capacity, he has co-led and made technical contributions to the development of a switched beam 60-GHz CMOS transceiver module for 802.11ad communications, the first reported Si-based 28-GHz phased array module for 5G communications (ISSCC 2017), and a 94-GHz polarimetric phased array RX and TX chipset. In 2013, he joined Columbia University, as an Adjunct Assistant Professor. Since 2016, he has been serving as a Principal Investigator of the Hyperimager Project with IBM's Research Frontiers Institute. He has 35 issued U.S. patents with 30+ pending. He has authored or co-authored more than 100 papers and received more than 3000+ independent citations. He is a Co-Editor of the book *60 GHz technology for Gbps WLAN and WPAN: From Theory to Practice* (Wiley, 2001).

Dr. Valdes-Garcia is the winner of the 2005 Best Doctoral Thesis Award presented by the IEEE Test Technology Technical Council. He was a recipient of the 2007 National Youth Award for Outstanding Academic Achievements, presented by the President of Mexico, and a co-recipient of the 2010 George Smith Award presented by the IEEE Electron Devices Society. Within IBM, he was a co-recipient of an Outstanding Innovation Award for "Demonstration of Wireless High Definition Video Links with 60 GHz SiGe Radios" in 2008, the 2009 Pat Goldberg Memorial Award to the best paper in computer science, electrical engineering, and mathematics published by IBM Research for the work Operation of Graphene Transistors at gigahertz frequencies (*Nano Letters*, 2009), and an Outstanding Technical Achievement Award for "High-speed Electronics Based on Graphene and 2-D Materials Beyond Graphene" (2017). He was inducted into the IBM Academy of Technology in 2015 and was recognized as an IBM Master Inventor in 2016. He has served for the IEEE 802.15.3c 60 GHz standardization Committee, from 2006 to 2009. Since 2009, he has been serving as a Technical Advisory Board Member with the Semiconductor Research Corporation, where he was a Chair of the Integrated Circuits and Systems Sciences Coordinating Committee, in 2011 and 2012, respectively. From 2010 to 2012, he was a Technical Program Committee Member with the IEEE Custom Integrated Circuits Conference and served as a Guest Editor for the IEEE Design and Test in 2012. Since 2016, he has been serving as a member for the IEEE MTT-S Microwave and Millimeter-wave Integrated Circuits Technical Committee. In 2013, he was selected by the National Academy of Engineering for its Frontiers of Engineering Symposium, and in 2015, for its German-American Frontiers of Engineering Symposium.