

Design-Oriented Analysis for Miller Compensation and Its Application to Multistage Amplifier Design

Wanyuan Qu, Shashank Singh, Yongjin Lee, Young-Suk Son, and Gyu-Hyeong Cho, *Fellow, IEEE*

Abstract—A design-oriented analysis (DOA) method is presented, which lends sufficient insights into various Miller compensation schemes. The method predicts the nondominant poles of the Miller-compensated amplifiers in an intuitive manner, and it serves as a good supplement to the conventional analysis. The usage of DOA is verified by the various design examples given in this paper. Guided by DOA, a multistage amplifier capable of driving a large-capacitive load (C_L) with low power consumption is presented. This amplifier employs an active zero to extend its Miller loop bandwidth, thereby pushing the amplifier's nondominant poles to high frequencies and achieving larger gain bandwidth (GBW). Fabricated in a 0.18- μm CMOS process, the amplifier achieves 1.18-MHz GBW and 59.6° phase margin when driving an 18-nF C_L , while consuming 69.6 μW from a 1.2-V supply. The design shows improved figures-of-merit compared with the prior state-of-the-art Miller-compensated multistage amplifiers.

Index Terms—Amplifier, frequency compensation, large-capacitive load (C_L), Miller compensation, multistage amplifier.

I. INTRODUCTION

SINCE the advances in CMOS process have led to a continuous degradation of amplifiers' intrinsic gain, multistage amplifiers are gaining popularity in the low-voltage and high-gain designs. Usually, the Miller compensation is employed for the frequency compensation because of its "pole-splitting" feature that can send the nondominant poles to high frequencies. In the past, although various Miller compensation schemes have been proposed to improve the gain bandwidth (GBW) of the circuit, complexity also increases and transfer functions become lengthy and elusive [1]–[20].

The conventional transfer function derivations usually render a complex relation among circuit parameters, impeding the intuitions from being obtained. On the other hand, [8] and [17] adopted a control-centric approach and improved the insights. For example, [8] claimed that the nondominant poles of a nested Miller compensation (NMC) amplifier is

the same as the poles of the unity feedback of NMC's inner Miller stage. Based on this knowledge, the design sequence is simplified, and design can start from the inner Miller stage, instead of from the overall amplifier as a whole. Similarly, [21] and [22] evaluate several advanced Miller strategies by comparing their respective inner Miller loops. Those prior works, although improving intuitions, did not explain the principle and the limits of the method. Besides, the method is still complex, since the complete transfer function of the inner Miller stage should be derived, which requires considerable computations.

In this paper, a control-centric design-oriented analysis (DOA) method is presented and thoroughly analyzed with both the advantages and the limits discussed. Besides, a simplification technique is presented, which helps identify the nondominant poles with significantly reduced computations. The insights are thus further enhanced. Besides, the efficacy of the method is verified in Section III with the examples of various Miller schemes (simple Miller, NMC, reversed Miller, and advanced Miller schemes), proving the DOA as a good supplement to the conventional transfer function analysis.

Guided by the DOA, a multistage amplifier capable of driving a large-capacitive load (C_L) with low power consumption is presented. The amplifier employs an active zero to extend its Miller loop's bandwidth and to push the nondominant poles to high frequencies. Therefore, the proposed design achieves improved figures-of-merit (FOM) compared with the prior arts. Finally, a brief discussion on the FOM is presented according to the equations of the DOA and the evolution and the applicability of different FOMs are discussed. This paper is organized as follows. Section II introduces the DOA, followed by the design examples using DOA in Section III. In Section IV, the proposed amplifier is described, including the discussions on the stability, circuit implementation, measurement results, and the FOM. The final conclusion is given in Section V.

II. DESIGN-ORIENTED ANALYSIS FOR MILLER COMPENSATION

Fig. 1 shows a two-stage Miller-compensated amplifier with four widely adopted Miller schemes classified by the substitution of compensation block (CB): simple Miller compensation (SMC) [Fig. 1(b)]; SMC with nulling resistor (SMCNR) [Fig. 1(c)]; SMC with voltage buffer (SMCVB) [Fig. 1(d)], and SMC with current buffer (SMCCB) [Fig. 1(e)]. In the Figs. 2–8, g_{mi} , R_{oi} , and c_{pi} are the i th stage transconductance, output resistance, and lumped node

Manuscript received May 29, 2016; revised July 25, 2016 and September 8, 2016; accepted October 17, 2016. Date of publication November 15, 2016; date of current version January 30, 2017. This paper was approved by Associate Editor Andrea Baschiroto.

W. Qu is with the Korea Advanced Institute of Science and Technology, Daejeon 34141, South Korea, and also with Silicon Works, Ltd., Daejeon 34027, South Korea (e-mail: wyqu@kaist.ac.kr).

S. Singh and Y. Lee are with Samsung Electronics, Hwaseong 18450, South Korea.

Y.-S. Son is with Silicon Works, Ltd., Daejeon 34027, South Korea.

G.-H. Cho is with the Korea Advanced Institute of Science and Technology, Daejeon 34141, South Korea.

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2016.2619677

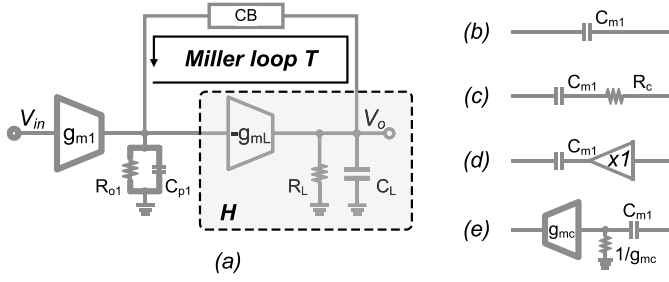


Fig. 1. (a) Two-stage Miller compensated amplifier with CB substituted as (b) SMC, (c) SMCNR, (d) SMCVB, and (e) SMCCB.

capacitance, respectively, and c_{mi} is the Miller capacitance. Unless otherwise noted, the following assumptions are made: $g_{mi}R_{oi} \gg 1$ and $C_{mi}, C_L \gg C_{pi}$.

A. Feedback Theory

Since Miller compensation generates a large capacitance using capacitive feedback, feedback theory is adopted for analysis. As shown in Fig. 1(a), a Miller-compensated amplifier equates a control system with a plant H and a feedback element CB . The transfer function from V_{in} to V_o , according to the closed-loop gain equation [25], is

$$\frac{V_o(s)}{V_{in}(s)} \approx A_\infty \frac{T}{1+T} + \frac{d}{1+T} \approx A_\infty \frac{T}{1+T} \quad (1)$$

where T is the Miller loop gain, A_∞ the ideal closed-loop gain when $T = \infty$, and d the direct feedforward when $T = 0$. DOA omits the second term, i.e., $d/(1+T)$, for simplicity. Both the use and the limit of DOA result from d omission. Since $A_\infty T/(1+T)$ reflects the effect of feedback, which determines the poles, and $d/(1+T)$ is the effect of feedforward, which affects the zeros, and the DOA predicts accurate poles while getting inaccurate zeros.

Two reasons justify this omission. First, it is always desirable to have an intuitive understanding on the poles. Since poles usually play an important role in determining the bandwidth, the DOA gives a quick understanding on the important bandwidth-limiting parameters. Second, even for designs, where the zeros are not negligible, combining the poles from the DOA with the zeros from the complete transfer function still gives accurate and insightful design equations.

B. High-Frequency Simplification

With d omitted, A_∞ and T , when applying the SMC of Fig. 1(a) and (b), are

$$A_\infty \approx -\frac{g_{m1}}{sC_{m1}} \quad (2)$$

$$T \approx -\frac{s \cdot g_{mL} R_L R_{o1} C_{m1}}{1 + s(R_{o1} C_{p1} + R_{o1} C_{m1} + R_L C_{m1} + R_L C_L) + s^2 R_L R_{o1} C_L C_{m1}} \quad (3)$$

where A_∞ indicates a single-pole behavior with $GBW = g_{m1}/C_{m1}$, while $T/(1+T)$, the unity feedback of T , generates the nondominant poles at and beyond T 's bandwidth.

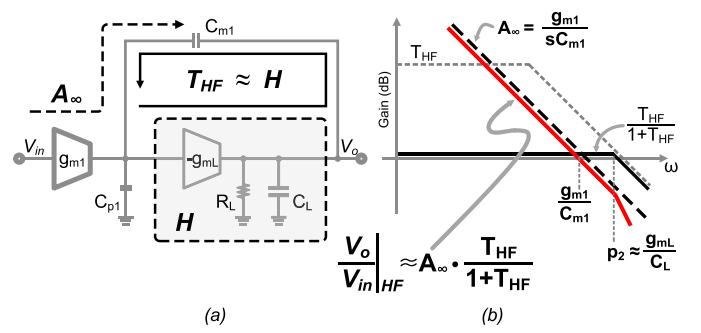


Fig. 2. Simplified analysis for SMC. (a) Simplified circuit. (b) Simplified Bode plot.

Instead of solving the complicated T directly, a simplification is presented to further simplify the T and reduce calculations. Since $T/(1+T)$ governs the high-frequency nondominant poles, only the high-frequency part of T needs to be considered. From (3), T has a zero at the origin and has two poles, when $C_L \gg C_{m1}$, at $1/R_{o1}C_{m1}$ and $1/R_L C_L$, respectively. As is shown, R_{o1} and C_{m1} contribute both the zero at the origin and the pole at $1/R_{o1}C_{m1}$. Since usually $GBW \gg 1/R_{o1}C_{m1}$, the high-frequency part of T effectively makes the zero and the pole cancel out, leaving a simplified Miller feedback path.

Based on the above-mentioned observation, this paper proposes to simplify the Miller loop T by assuming that the zero at the origin always cancels out the pole from R_{o1} . This simplification is achieved by ignoring R_{o1} in T analysis under the assumption that R_{o1} is infinitely large. This simplification, although originating from the SMC with $C_L \gg C_{m1}$, is found valid for all the commonly used schemes in Fig. 1 and for various C_L as long as $GBW \gg 1/R_{o1}C_{m1}$ (or $1/R_{o1}C_{p1}$ for SMCCB) and the Miller capacitor contributes the dominant term in open-circuit time constant. It is noted that, although $1/R_L C_L$ can be the first pole in the Miller loop, the assumed cancellation of R_{o1} -contributed pole with the zero improves insights and facilitates to obtain the nondominant poles as long as the above conditions are met. Since the conditions are typically satisfied, those assumptions are made for all the following designs.

III. DESIGN EXAMPLES USING DOA

A. Simple Miller Compensation

Fig. 2(a) shows the simplified Miller loop T_{HF} for SMC, assuming R_{o1} is infinitely large. Here, T_{HF} reduces to a first order with C_L in parallel with the series of C_{m1} and C_{p1} . $T_{HF}/(1+T_{HF})$ then imposes a nondominant pole p_2 at the bandwidth of T_{HF} , that is

$$p_2 \approx \frac{g_{mL}}{C_L + C_{m1}C_{p1}/(C_{m1} + C_{p1})} \approx \frac{g_{mL}}{C_L}. \quad (4)$$

Clearly, with little mathematics, the DOA predicts the exact p_2 well matched with the nondominant pole given by

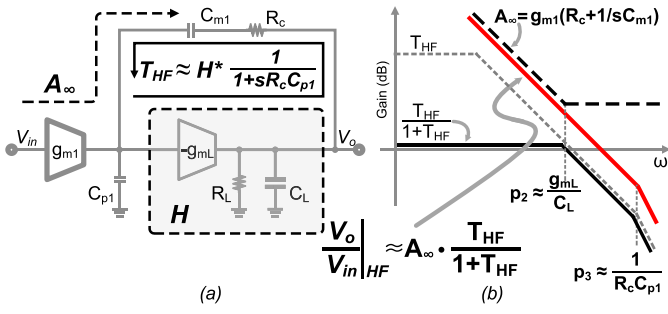


Fig. 3. Simplified analysis for SMCNR. (a) Simplified circuit. (b) Simplified Bode plot.

the complete transfer function

$$\frac{V_{in}}{V_o} \approx \frac{-g_{m1}g_{mL}R_{o1}R_L(1-sg_{mL}/C_{m1})}{1+sg_{mL}R_LR_{o1}C_{m1}+s^2R_{o1}R_L(C_{m1}C_{p1}+C_{m1}C_L+C_LC_{p1})}. \quad (5)$$

Since the DOA tells that the SMC has a GBW $\approx g_{m1}/C_{m1}$ and a nondominant pole p_2 , the phase margin ϕ' can be represented as

$$\phi' \approx 90^\circ - \tan^{-1}(\text{GBW}/p_2). \quad (6)$$

Now, given the desired GBW, ϕ' , and C_L , combining GBW = g_{m1}/C_{m1} and (6) gives the required g_{m1} , C_{m1} , and g_{mL} when setting any one of them. A typical design procedure sets g_{m1} first according to the noise requirement [7] and derives C_{m1} and g_{mL} . Finally, the zero is evaluated independently. Since (5) indicates a right-half-plane (RHP) zero at g_{mL}/C_{m1} , the phase margin ϕ , when considering the zero, is

$$\phi \approx \phi' + \tan^{-1} \frac{\text{GBW}}{\text{zero}} \approx \phi' - \tan^{-1} \frac{g_{m1}}{g_{mL}} \quad (7)$$

indicating that the zero is negligible when $g_{m1} \ll g_{mL}$. Here, the DOA gives a quick understanding on the nondominant poles and generates a simple design equation (6). Even for designs, where the zero is not negligible, combining the poles of the DOA with the zeros from transfer functions still generates a simple and accurate design equation (7).

B. Simple Miller Compensation With Nulling Resistor

Fig. 3(a) shows the simplified Miller loop T_{HF} of SMCNR, assuming R_{o1} is infinite. Here, T_{HF} is seen as H cascaded by a low-pass filter consisting of R_c , C_{m1} , and C_{p1} . Since $C_{m1} \gg C_{p1}$, C_{m1} can be ignored and $T_{HF} \approx H^*1/(1+sR_cC_{p1})$. By inspection, $T_{HF}/(1+T_{HF})$ then generates two poles at T_{HF} 's

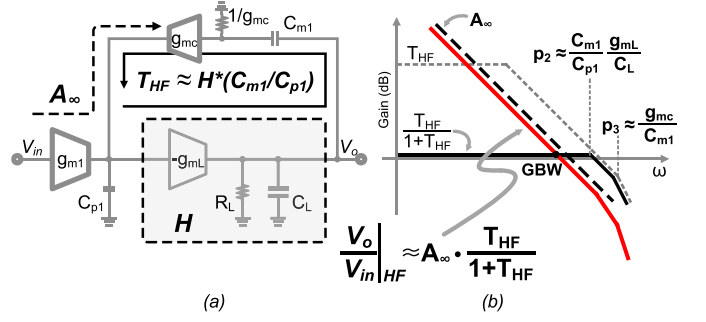


Fig. 4. Simplified analysis for SMCCB. (a) Simplified circuit. (b) Simplified Bode plot.

bandwidth and $1/R_cC_{p1}$, respectively

$$p_2 \approx \omega_{THF} \approx \frac{g_{mL}}{C_L + C_{m1}C_{p1}/(C_{m1} + C_{p1})} \approx \frac{g_{mL}}{C_L} \quad (8)$$

$$p_3 \approx \frac{1}{R_cC_{p1}}.$$

C_{m1} and C_{p1} in the denominator of p_2 represent their loading effect to H . On the other hand, the complete transfer function, when $R_c \ll R_{o1}$, which is typically the case, is given in (9), as shown at the bottom of this page. p_2 and p_3 match the nondominant poles in (9) with good accuracies

Besides, considering $A_\infty = g_{m1}^*(R_c + 1/sC_{m1})$, A_∞ predicts a zero at $1/R_cC_{m1}$, which is slightly different from the accurate zero at $1/(R_c - 1/g_{mL})C_{m1}$, as given by (9). The difference, as mentioned before, is because a feedforward d exists here.

A common design method for maximized GBW uses the zero of SMCNR to cancel p_2 , i.e., $1/(R_c - 1/g_{mL})C_{m1} = p_2$ and $\phi \approx 90^\circ - \tan^{-1}(\text{GBW}/p_3)$, where ϕ is the phase margin. Substituting the equations gives the optimized R_c as

$$R_c \approx \sqrt{C_L/(g_{mL}g_{m1}C_{p1} \tan \phi)} \quad (10)$$

which is the same as reported in [1] and [4] using the complete transfer equations.

C. Simple Miller Compensation With Current Buffer

Fig. 4(a) shows the simplified Miller loop of the SMCCB, assuming that R_{o1} is infinite. Here, H is cascaded by a common-gate amplifier consisting of C_{m1} , g_{mc} , $1/g_{mc}$, and C_{p1} , which contributes a gain of C_{m1}/C_{p1} and a pole at g_{mc}/C_{m1} . The $T_{HF}/(1+T_{HF})$ then predicts the nondominant poles at

$$p_2 \approx \omega_{\text{Miller}} \approx \frac{C_{m1}}{C_{p1}} \frac{g_{mL}}{C_L + C_{m1}} \approx \frac{C_{m1}}{C_{p1}} \frac{g_{mL}}{C_L} \quad (11)$$

$$p_3 \approx \frac{g_{mc}}{C_{m1}}.$$

$$\frac{V_{in}}{V_o} \approx \frac{-g_{m1}g_{mL}R_{o1}R_L[1-sC_{m1}(R_c-1/g_{mL})]}{1+sg_{mL}R_LR_{o1}C_{m1}+s^2R_LR_{o1}(C_{m1}C_L+C_{m1}C_{p1}+C_LC_{p1})+s^3R_{o1}R_LR_zC_{p1}C_{m1}C_L} \quad (9)$$

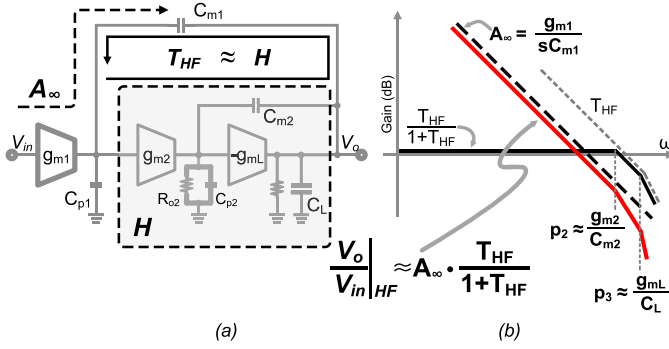


Fig. 5. Simplified analysis for NMC. (a) Simplified circuit. (b) Simplified Bode plot.

ω_{Miller} , the bandwidth of T_{HF} , is boosted by C_{m1}/C_{p1} times thanks to the common-gate amplifier and the C_{m1} in the denominator of p_2 represents the loading effect of C_{m1} to H . Besides, A_∞ indicates a left-half-plane (LHP) zero at g_{m1}/C_{m1} , because $A_\infty = g_{m1}^*(1/g_{m1} + 1/sC_{m1})$. Compared with the complete transfer function (12), as shown at the bottom of this page, the DOA predicts accurately both the nondominant poles and the zero. The reason for the correct zero is because there is no feedforward path d here for the SMCCB.

The design of the SMCCB can start from the inner Miller stage. Since the Miller loop T_{HF} has a bandwidth of ω_{Miller} and a pole at p_3 , the phase margin of the Miller loop can be represented as $\phi_{\text{Miller}} \approx 90^\circ - \tan^{-1}(\omega_{\text{Miller}}/p_3)$. In order to get a good tradeoff between the response time and the transient overshoot, ϕ_{Miller} of 60° – 70° is recommended. Substituting (11) into ϕ_{Miller} gives

$$C_{m1} \approx \sqrt{g_{m1}C_L C_{p1}/(g_{mL} \tan \phi_{\text{Miller}})} \quad (13)$$

which guides the optimum C_{m1} for maximum bandwidth and (13) is echoed by a similar result in [4]. Besides, ω_{Miller} is related to the overall GBW as (see the Appendix)

$$\omega_{\text{Miller}} \approx \chi \cdot \text{GBW} \quad (14)$$

where χ is the separation factor between ω_{Miller} and the GBW. Equation (A.5) in the Appendix tells that χ is a function of ϕ_{Miller} and the overall phase margin ϕ_{overall} . For example, $\chi \approx 2$ when $\phi_{\text{Miller}} \approx \phi_{\text{overall}} \approx 60^\circ$. Now, with the GBW, ϕ_{overall} , ϕ_{Miller} , and C_L specified, ω_{Miller} is derived, then g_{m1} , C_{m1} , g_{mL} , and g_{mc} can be calculated by setting any one of them.

D. Nested Miller Compensation

Fig. 5(a) is the simplified Miller loop of NMC, assuming that R_{o1} is infinite. Considering $C_{m1} \gg C_{p1}$, T_{HF} reduces to

unity feedback, i.e., $T_{\text{HF}} \approx H$, where H is the inner Miller stage, which is a two-stage SMC amplifier. The nondominant poles of the overall amplifier then result from $H/(1+H)$, the unity feedback of the inner Miller stage. This is the same conclusion as already proved in (8).

The design sequence of the NMC is the same as before. With the GBW, ϕ'_{overall} , ϕ_{Miller} , and C_L specified, where ϕ'_{overall} and ϕ_{Miller} are the phase margins of the overall amplifier and the inner Miller stage H , respectively, and ω_{Miller} can be derived first according to (A.5). Then, the inner Miller stage can be designed either according to (7), which includes the RHP zero's effect or according to (6), where the zero is negligible. It is noted here that the optimization in NMC may require iterations. The reason is because the separation factor χ given by (A.5) applies for the inner stage, which has two poles, but H here has two poles and an RHP zero. The transfer function of NMC is (15), as shown at the bottom of this page.

Finally, the zeros' effect is evaluated according to the complete transfer function (15). The overall phase margin ϕ_{overall} , when considering the zeros, is

$$\begin{aligned} \phi_{\text{overall}} &\approx \phi'_{\text{overall}} - \tan^{-1} \frac{g_{m2}/g_{mL}}{\chi + g_{m1}/g_{mL}} \\ &\approx \phi'_{\text{overall}} - \tan^{-1} \left(\frac{1}{\chi} \cdot \frac{g_{m2}}{g_{mL}} \right). \end{aligned} \quad (16)$$

From (16) and (7), a smaller g_{m2}/g_{mL} is beneficial to both the overall and the inner loops, indicating larger power requirements on g_{mL} , which is the most significant drawback of the NMC amplifier.

E. Reversed Nested Miller Compensation

Reversed NMC was proposed for circuits with inverting inner stage [24] and was extensively analyzed in [11]. Fig. 6 gives the simplified Miller loop T_{HF} of reversed nested Miller compensation (RNMC), assuming that R_{o1} is infinite. Besides, $C_L \gg C_{m1}$ is assumed to simplify explanations and C_{p1} is also ignored in Fig. 6(c) considering $C_{m1} \gg C_{p1}$.

Here, T_{HF} approximates to the product of G and H , both of which are first orders. G , shown in Fig. 6(c), is an inverting amplifier with a gain equals $-C_{m1}/C_{m2}$. Therefore, it is always advantageous to set $C_{m1} \gg C_{m2}$ and to boost the bandwidth of T_{HF} . Since G provides a gain to the inner Miller loop, the RNMC is always superior to its NMC counterparts from the GBW perspective. Besides, since $G \approx A_{G\infty}T_{\text{GHF}}/(1+T_{\text{GHF}})$, where $A_{G\infty} \approx -C_{m1}/C_{m2}$ and T_{GHF} is a local loop consisting of g_{m2} , C_{m2} , and C_{m1} , $T_{\text{GHF}}/(1+T_{\text{GHF}})$ then imposes a pole p_3 at the bandwidth of G . Now, with both G and H known, the nondominant poles

$$\frac{V_{\text{in}}}{V_o} \approx \frac{-g_{m1}g_{mL}R_{o1}R_L[1+sC_{m1}/g_{mc}]}{1+s g_{mL}R_L R_{o1}C_{m1}+s^2 R_L R_{o1}C_{p1}(C_L+C_{m1})+s^3 R_L R_{o1}C_{p1}C_L C_{m1}/g_{mc}} \quad (12)$$

$$\frac{V_{\text{in}}}{V_o} \approx \frac{-g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L[1-sC_{m2}/g_{mL}+s^2 C_{m1}C_{m2}/g_{m2}g_{mL}]}{(1+s g_{m2}R_{o2}g_{mL}R_L R_{o1}C_{m1})[1+s C_{m2}(1/g_{m2}-1/g_{mL})+s^2 C_{m2}C_L/g_{m2}g_{mL}]} \quad (15)$$

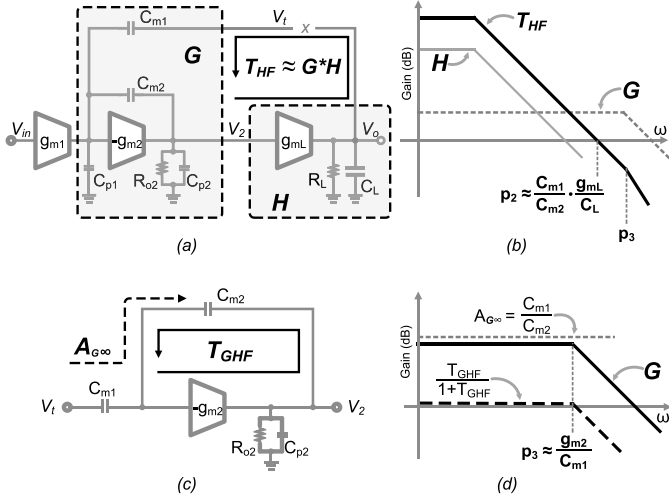


Fig. 6. Simplified analysis for RNMC. (a) Simplified circuit. (b) Simplified Bode plot of RNMC. (c) Simplified inner stage G . (d) Simplified Bode plot of G .

resulting from the $T_{HF}/(1 + T_{HF})$ are

$$p_2 \approx \omega_{\text{Miller}} \approx \frac{C_{m1}}{C_{m2}} \frac{g_{mL}}{C_L}$$

$$p_3 \approx \frac{g_{m2}}{C_{m1}C_{m2}/(C_{m1} + C_{m2})} \cdot \frac{C_{m2}}{C_{m1} + C_{m2}} \approx \frac{g_{m2}}{C_{m1}} \quad (17)$$

where C_{m1}/C_{m2} and g_{mL}/C_L in p_2 represent the gain of G and the bandwidth of H , respectively, and p_3 tells the bandwidth of G . Compared with the accurate nondominant poles given by transfer function (18), as shown at the bottom of this page, p_2 and p_3 show good accuracies.

Similarly, with the GBW, ϕ_{overall} , ϕ_{Miller} , and C_L specified, ω_{Miller} is derived first. Then, with ϕ_{Miller} and derived ω_{Miller} , p_3 can be calculated according to

$$\phi_{\text{Miller}} \approx 90^\circ - \tan^{-1}(\omega_{\text{Miller}}/p_3). \quad (19)$$

Finally, device parameters should be chosen according to (17) to satisfy the required ω_{Miller} and p_3 . The zeros, although exist in (18), do not have a significant effect in a well-guided design. As indicated by (18), RNMC has a lower RHP zero and a higher LHP zero. When the zeros are widely separated, the RHP zero occurs at g_{m2}/C_{m2} . Considering $C_{m1} \gg C_{m2}$ for maximum bandwidth boosting, RHP zero $\gg p_3 \gg \text{GBW}$. Therefore, the zeros can be properly ignored without losing accuracies.

F. Single Miller Capacitor Compensation

Ever since the first advanced Miller scheme (damping-factor-control frequency compensation (DFCFC) [6]), the

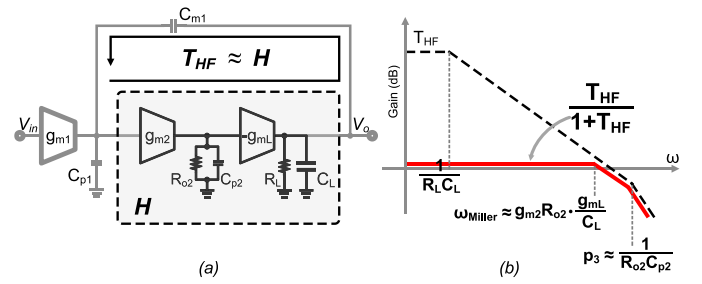


Fig. 7. Simplified analysis for SMCC. (a) Simplified circuit. (b) Simplified Bode plot.

FOM of the multistage amplifiers with large C_L has been enhanced significantly. From DOA's perspective, most previous studies before the DFCFC were focusing on the d design, i.e., modulating the feedforward zeros (such as exploiting large g_{mL} , feedforward path [3], [5], current/voltage buffers [9], [19], and nulling resistors [8]); while the advanced schemes focus on the T_{HF} design (by inserting gain stages into T_{HF}) and almost ignore d . The bandwidth of T_{HF} is thus significantly extended and the overall GBW greatly improved. The SMCC [14] is given as an example.

Fig. 7(a) is the simplified Miller loop of SMCC assuming that R_{o1} is infinite. Here, T_{HF} also reduces to a unity feedback with $T_{HF} \approx H$. H , as shown, is a two-stage amplifier with a dominant pole at $1/R_L C_L$ and a second pole at $1/R_{o2} C_{p2}$, respectively. The nondominant poles, as predicted by $H/(1 + H)$, are

$$p_2 \approx \omega_{\text{Miller}} \approx g_{m2} R_{o2} g_{mL} / C_L$$

$$p_3 \approx 1/R_{o2} C_{p2}. \quad (20)$$

$g_{m2} R_{o2}$ in p_2 represents the gain of g_{m2} stage, and g_{mL}/C_L is the bandwidth of the g_{mL} stage. As is shown, p_2 and p_3 matches well with the complete transfer function (21), as shown at the bottom of this page.

Besides, by inspection of Fig. 7(b), the Miller bandwidth ω_{Miller} cannot exceed its second pole at p_3 for a phase margin of at least 45° ; a design guideline can be given as

$$\text{GBW} \approx g_{m1}/C_{m1} < \omega_{\text{Miller}} < p_3 \quad (22)$$

which is also obtained in [14] by applying Routh's stability criterion. Clearly, the DOA gets this result much easier and provides more circuit explanations.

The design of the SMCC is the same as before. First, derive ω_{Miller} using the GBW, ϕ'_{overall} , and ϕ_{Miller} , then the inner Miller stage should be designed to satisfy the required ϕ_{Miller} ; finally, device parameters should be chosen according to (20) to satisfy the derived p_2 and p_3 . The zeros, as indicated by (21), are also negligible here. For example, the overall

$$\frac{V_{in}}{V_o} \approx \frac{-g_{m1} g_{m2} g_{mL} R_{o1} R_{o2} R_L [1 - s C_{m2}/g_{m2} - s^2 C_{m1} C_{m2}/g_{m2} g_{mL}]}{(1 + s g_{m2} R_{o2} g_{mL} R_L R_{o1} C_{m1})(1 + s C_{m2} C_L/g_{mL} C_{m1} + s^2 C_{m2} C_L/g_{m2} g_{mL})} \quad (18)$$

$$\frac{V_{in}}{V_o} \approx \frac{-g_{m1} g_{m2} g_{mL} R_{o1} R_{o2} R_L [1 - s C_{m1}/g_{m2} R_{o2} g_{mL} - s^2 C_{m1} C_{p2}/g_{m2} g_{mL}]}{(1 + s g_{m2} R_{o2} g_{mL} R_L R_{o1} C_{m1})(1 + s C_L/g_{m2} R_{o2} g_{mL} + s^2 C_L C_{p2}/g_{m2} g_{mL})} \quad (21)$$

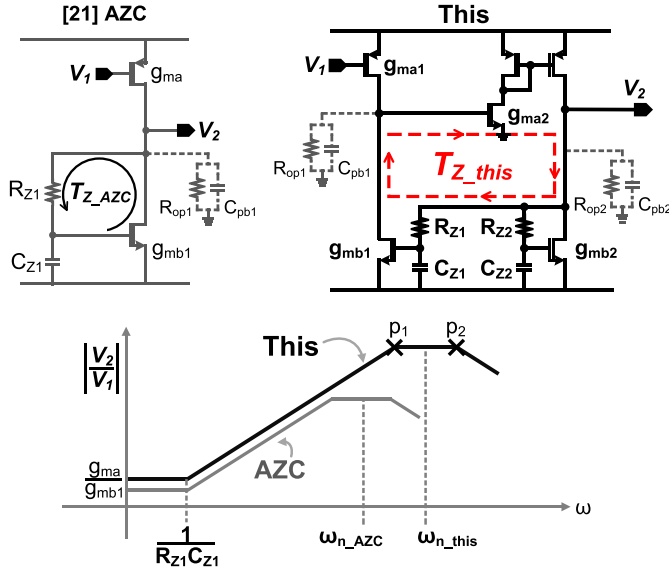


Fig. 8. Active zero circuits and gain plots of the prior and this paper.

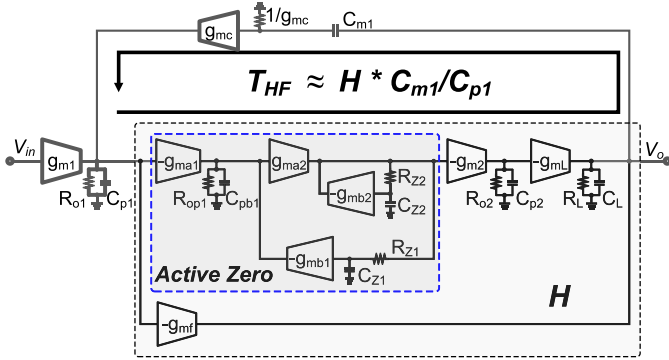


Fig. 9. Circuit block diagram of the proposed multistage amplifier.

phase margin when considering the RHP zero, ϕ_{overall} , is given as

$$\phi_{\text{overall}} \approx \phi'_{\text{overall}} - \tan^{-1}[g_{m1}/(g_{m2}R_{o2}g_{mL})]. \quad (23)$$

Since $g_{m2}R_{o2}$ provides significant amount of gain, the arctangent term in (23) is usually small, indicating almost negligible zero's effect. This explains the reason for the negligible RHP zeros in most advanced Miller schemes.

In summary, a rough performance comparison can be given, from GBW's perspective

$$\begin{aligned} \text{AdvancedMiller} &> \text{ReversedMiller} \\ &> \text{SimpleMiller} > \text{NestedMiller}. \end{aligned}$$

The advantages of the advanced and the reversed Miller schemes result from the fact that both the types insert gain stages into the Miller loop. This, however, is a tradeoff, because the added gain stage can cause instability to the inner Miller loop especially when C_L is small. Therefore, the advanced and reversed Miller schemes usually have a low boundary for C_L , which is governed by the inner Miller stage's stability.

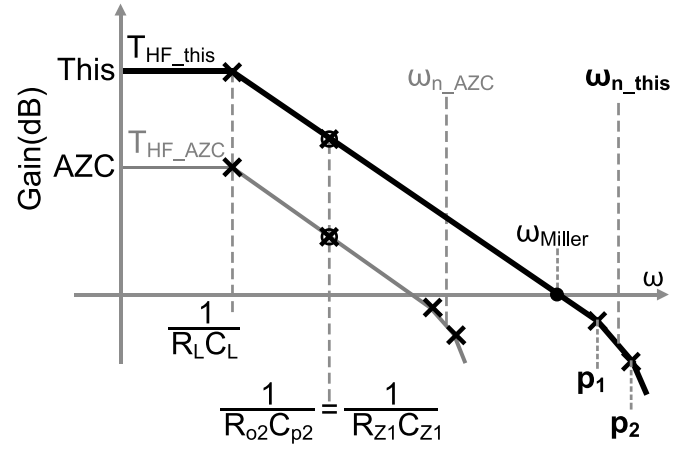


Fig. 10. Simplified Miller loop gain of the prior and this paper.

Last but not least, the above-mentioned examples show that the DOA simplifies the Miller loop and predicts the nondominant poles intuitively and accurately. It is found especially suitable for the advanced Miller schemes and for schemes with no feedforward d , such as SMCCB. For designs where the effect of zeros cannot be neglected, the DOA can still generate insightful equations when including the zeros from the complete transfer functions. Therefore, the DOA is a good supplement to transfer functions and help interpret the increasingly elusive transfer functions.

IV. PROPOSED SCHEME

A. Circuit Block Diagram

This paper proposes an advanced Miller scheme for multistage amplifiers driving a large C_L . The scheme adopts an active zero to extend the Miller bandwidth. Compared with other schemes, which also exploit an active zero [21], [22], the one proposed here has a larger bandwidth under the same power and C_L , thus the FOM is improved. The active zero circuit is described before delving into the overall circuit.

Fig. 8 shows the active zero circuits and the Bode plots of the prior [21] and this paper. Since [22] has a similar analytical form as [21], it is not discussed for simplicity. Here, an active zero is implemented using a local feedback. For example, in active zero compensation, local feedback T_{Z_AZC} is formed using R_{Z1} , C_{Z1} , and g_{mb1} . The feedback reduces the impedance at V_2 to $1/g_{mb1}$, and increases the impedance as feedback gain weakens at higher frequency. The gain from V_1 to V_2 , given by (24), increases when a zero occurs at $1/R_{Z1}C_{Z1}$ and flattens out when a pole is met at g_{mb1}/C_{Z1} , which equals the bandwidth of T_{Z_AZC}

$$\left. \frac{V_2}{V_1} \right|_{\text{AZC}} \approx \frac{g_{ma1}(1 + sR_{Z1}C_{Z1})}{g_{mb1} + sC_{Z1} + s^2R_{Z1}C_{Z1}C_{pb1}}. \quad (24)$$

Besides, (24) indicates another pole at $1/R_{Z1}C_{pb1}$. When extending the bandwidth of g_{mb1}/C_{Z1} by reducing C_{Z1} while keeping the zero at $1/R_{Z1}C_{Z1}$ fixed, the pole at $1/R_{Z1}C_{pb1}$ moves to lower frequency, and finally, generates a pair of complex poles at ω_{n_AZC} . From (25), given the specified zero frequency $1/R_{Z1}C_{Z1}$ and desired ω_{n_AZC} , the g_{mb1} value can be resolved first. Then, with the ω_{n_AZC} and estimated parasitic

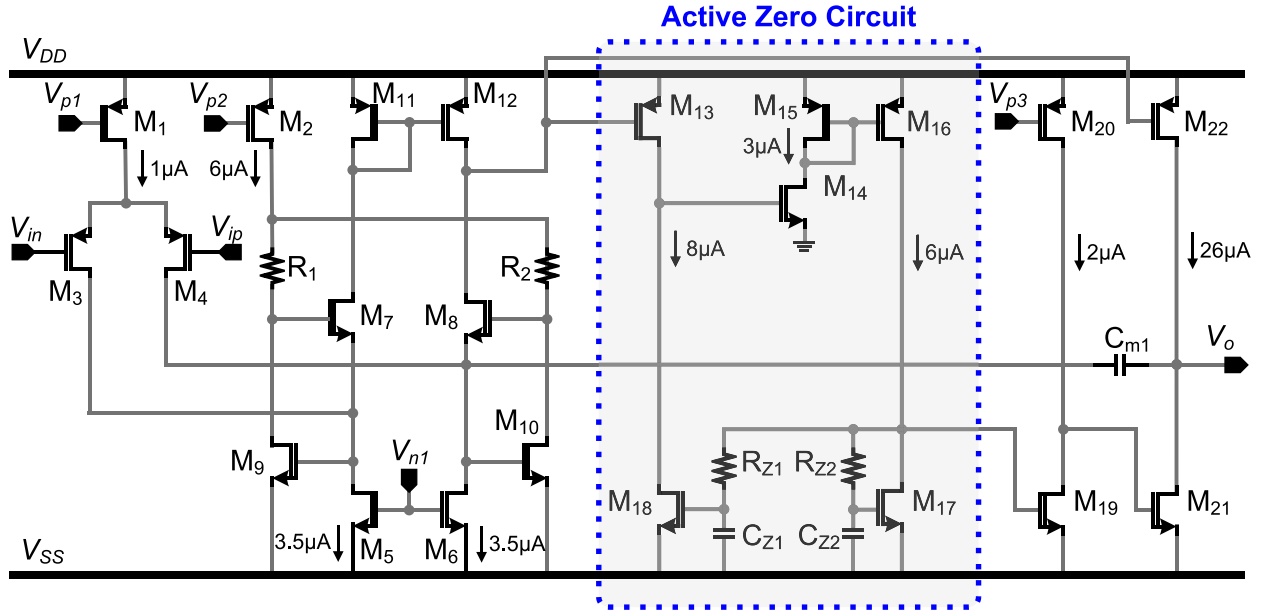


Fig. 11. Circuit schematic of the proposed amplifier.

C_{pb1} , the R_{z1} value can be derived. Equation (25) indicates that a smaller R_{z1} gives a larger damping factor ζ_{AZC}

$$\omega_{n_AZC} \approx \sqrt{g_{mb1}/(R_{z1}C_{z1}C_{pb1})} \quad \zeta_{AZC} \approx \frac{1}{2\omega_{n_AZC} R_{z1}C_{pb1}}. \quad (25)$$

This paper proposes to extend the bandwidth of the active zero's loop. Fig. 8 shows the proposed local loop T_{Z_this} comprising g_{ma2} , g_{mb1} , g_{mb2} , R_{z1} , R_{z2} , C_{z1} , and C_{z2} , where R_{z1} and C_{z1} generate the overall active zero at $1/R_{z1}C_{z1}$, and g_{mb2} , R_{z2} , and C_{z2} contribute a zero at $1/R_{z2}C_{z2}$. Compared with T_{Z_AZC} , which has two open-loop poles at $1/R_{z1}C_{z1}$ and $1/R_{pb1}C_{pb1}$, this work inserts a zero at $1/R_{z2}C_{z2}$ to further extend the bandwidth of T_{Z_this} . Besides, since the zero at $1/R_{z2}C_{z2}$ can be set much higher than $1/R_{z1}C_{z1}$, little extra current is required for g_{mb2} .

Specifically, the gain from V_1 to V_2 of the proposed circuit is (26) and (27), as shown at the bottom of this page, where p_0 – p_3 are the approximated parasitic poles. Here, p_0 cancels the zero at $1/R_{z2}C_{z2}$. p_3 is temporarily ignored for simplicity, because it is usually at very high frequency. The complex poles ω_{n_this} and the damping factor ζ , which results from p_1 and p_2 , are

$$\omega_{n_this} \approx \sqrt{g_{ma2}g_{mb1}R_{z2}/(R_{z1}C_{z1}C_{pb1})} \approx \sqrt{g_{ma2}R_{z2}\omega_{n_AZC}} \\ \zeta \approx \frac{\frac{g_{mb2}}{C_{z2}} + \frac{1}{R_{pb1}C_{pb1}}}{2\omega_{n_this}}. \quad (28)$$

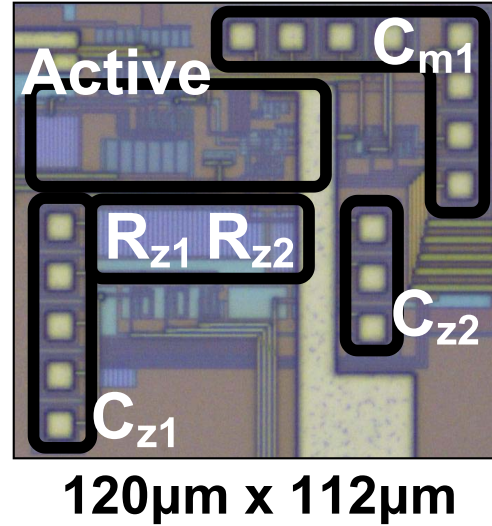


Fig. 12. Chip micrograph.

Similarly, given the specified zero at $1/R_{z1}C_{z1}$ and desired ω_{n_this} , the g_{ma2} , g_{mb1} , and R_{z2} can be set first; then the g_{mb2} and C_{z2} are determined to generate the desired damping factor. Equation (28) tells that a larger damping factor requires larger g_{mb2} or smaller C_{z2} . Compared with the previous work [21], [22], the bandwidth of the proposed active zero is

$$\frac{V_2}{V_1} \Big|_{this} \approx \frac{g_{ma1}g_{ma2}(1+sR_{z1}C_{z1})(1+sR_{z2}C_{z2})}{g_{ma2}g_{mb1}+s g_{ma2}g_{mb1}R_{z2}C_{z2}+s^2 R_{z1}C_{z1}(g_{mb2}C_{pb1}+C_{z2}/R_{op1})+s^3 R_{z1}C_{z1}C_{z2}C_{pb1}+s^4 R_{z1}R_{z2}C_{z1}C_{z2}C_{pb1}C_{pb2}} \quad (26)$$

$$p_0 \approx -\frac{1}{R_{z2}C_{z2}} \quad p_1 \approx -\frac{g_{ma2}g_{mb1}R_{z2}C_{z2}}{g_{mb2}C_{pb1}R_{z1}C_{z1}} \quad p_2 \approx -\frac{g_{mb2}}{C_{z2}} \quad p_3 \approx -\frac{1}{R_{z2}C_{pb2}} \quad (27)$$

TABLE I
DEVICE SIZES

Device	Size (μm)	Device	Size (μm)	Device	Size
M1	4/2	M15	0.4/0.4	R1-R2	34.9 kΩ
M2	12/1	M16	0.8/0.4	R _{Z1}	350 kΩ
M3-M4	16/1	M17	6/0.4	R _{Z2}	39.8 kΩ
M5-M6	16/3	M18	8/0.4	C _{Z1}	0.404 pF
M7-M10	16/0.4	M19	2/0.4	C _{Z2}	0.311 pF
M11-M12	8/1	M20	4/1	C _m	0.809 pF
M13	20/0.2	M21	20/0.2		
M14	2/0.2	M22	60/0.2		

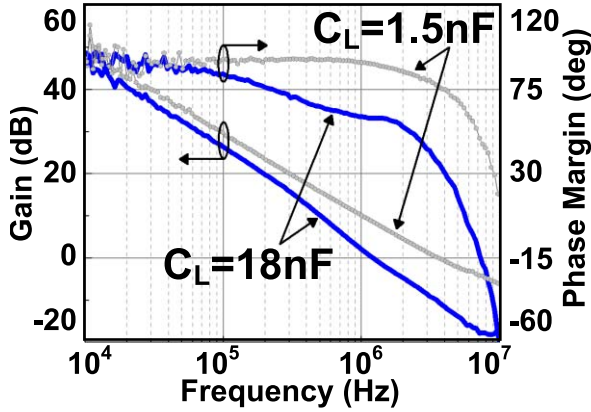


Fig. 13. Measured frequency responses for $C_L = 1.5$ and 18 nF.

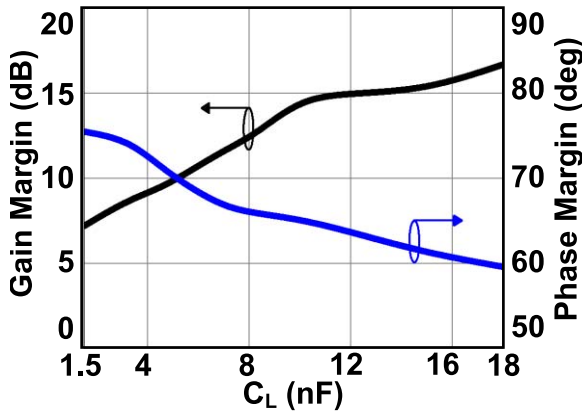


Fig. 14. Gain/phase margin versus C_L .

extended by $(g_{m2}R_{Z2})^{1/2}$ times. A proper R_{Z2} can efficiently extend ω_{n_this} while consuming limited current on g_{m2} . Considering that R_{Z2} and C_{pb2} constitute p_3 , and C_{pb2} is a small internal parasitic capacitance, a decent bandwidth extension is possible without reducing stability margins. In the proposed design, the $(g_{m2}R_{Z2})^{1/2}$ was set to ~ 2.3 times with p_3 (~ 400 MHz) significantly higher than the GBW (~ 1.18 MHz).

Fig. 9 shows the proposed multistage amplifier with large C_L . Here, a current-buffer Miller compensation is applied to an inner plant H consisting of the active zero, g_{m2} and g_{mL} stage. According to DOA and assuming that

the pole of the current buffer at g_{mc}/C_{m1} is sufficiently high, the simplified Miller loop is $T_{THF} \approx (C_{m1}/C_{p1}) \cdot H$. Now, H has a dominant pole at $1/R_L C_L$, a second pole at $1/R_{o2} C_{p2}$, and a zero at $1/R_{Z1} C_{Z1}$. From Fig. 10, T_{THF} equates a single pole system with a bandwidth of ω_{Miller} , given in (29), when the active zero cancels the second pole, i.e., $1/R_{Z1} C_{Z1} \approx 1/R_{o2} C_{p2}$

$$\omega_{Miller} \approx g_{m2} R_{o2} \frac{C_{m1}}{C_{p1}} \frac{g_{ma1}}{g_{mb1}} \frac{g_{mL}}{C_L}. \quad (29)$$

The (C_{m1}/C_{p1}) represents the current buffer gain, (g_{ma1}/g_{mb1}) and $g_{m2} R_{o2}$ are the dc gain of the active zero and the g_{m2} stage, respectively, and g_{mL}/C_L is the bandwidth of the g_{mL} stage. Since T_{THF} is limited by p_1 , which locates at high frequency, ω_{Miller} is extended and large GBW is achieved.

B. Design Procedure

The design starts from the inner Miller loop T_{THF} , and p_2 and p_3 are temporarily ignored to simplify analysis. Since T_{THF} shows a bandwidth of ω_{Miller} with a nondominant pole at p_1 , the phase margin of the Miller loop, ϕ_{Miller} , is

$$\phi_{Miller} \approx 90^\circ - \tan^{-1}(\omega_{Miller}/p_1). \quad (30)$$

Similarly, the Miller bandwidth ω_{Miller} is related to the overall GBW as

$$\omega_{Miller} \approx \chi \cdot \text{GBW}. \quad (31)$$

Now, with the GBW, $\phi_{overall}$, and ϕ_{Miller} specified, ω_{Miller} and p_1 are derived. Then, device parameters should be optimized according to (27) and (29). Besides, p_2 and p_3 , which were ignored at the beginning, should be extended sufficiently beyond p_1 .

C. Circuit Implementation

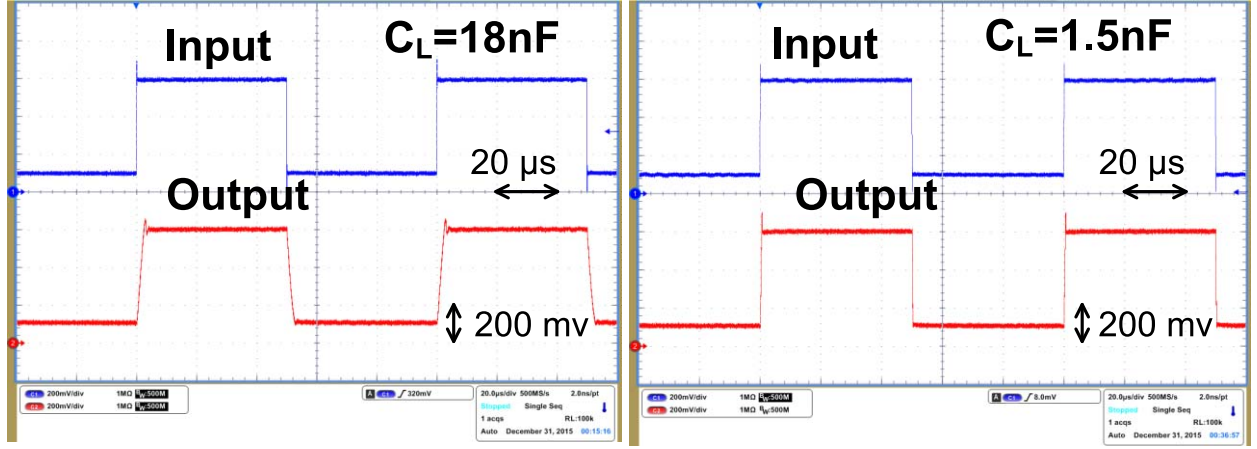
Fig. 11 shows the circuit implementation of the proposed amplifier. $M1-12$, R_1 , and R_2 form the input stage, and g_{m1} equals the transconductance of the input pair. The $M5-10$, R_1 , and R_2 boost the current buffer transconductance and extend the pole of the current buffer at g_{mc}/C_{m1} to high frequency. $M13-18$, R_{Z1} , R_{Z2} , C_{Z1} , and C_{Z2} compose the active zero circuit with the zero $1/R_{Z1} C_{Z1}$ at 1.1 MHz and $1/R_{Z2} C_{Z2}$ at 12 MHz, respectively. Finally, $M19-20$ and $M21-22$ constitute the second and final stages, respectively. $M22$ is a feedforward device, which forms a push-pull output stage with $M21$. As is seen from the circuit, the slew rate of the proposed amplifier is limited either by the input stage driving C_{m1} or limited by the output stage driving C_L . The linear settling time is mainly determined by the GBW and $\phi_{overall}$.

D. FOM Description

The most commonly adopted FOM are defined as follows:

$$\text{FOM}_S = \frac{\text{GBW} \cdot C_L}{\text{power}} \quad \text{FOM}_L = \frac{\text{SR} \cdot C_L}{\text{power}} \quad (32.1)$$

$$\text{IFOM}_S = \frac{\text{GBW} \cdot C_L}{\text{current}} \quad \text{IFOM}_L = \frac{\text{SR} \cdot C_L}{\text{current}} \quad (32.2)$$

Fig. 15. 500-mV step transient responses for $C_L = 1.5$ and 18 nF.

	[21] AZC JSSC 2013	[22] LEC ISSCC 2014	[23] LIA JSSC 2015	This	
Load C_L (pF)	15,000	500	560	1,500	18,000
GBW (MHz)	0.95	1.34	3.49	3.46	1.18
Phase margin (°)	52.3	52.7	53	75.5	59.6
Average SR (V/μs)	0.22	0.62	0.86	1.46	0.22
Average 1% T_S (μs)	4.49	0.62	0.9	0.57	4.1
DC Gain (dB)	>100	>100	>100	>100	
Power (μW@ V_{DD})	144 @ 2V	6.3 @ 0.9V	12.7 @ 1.2V	69.6 @ 1.2V	
C_{m1} Capacitance (pF)	1.42	0.63	0.24	0.81	
Chip Area (mm ²)	0.016	0.007	0.003	0.013	
CMOS Technology	0.35μm	0.18μm	0.13μm	0.18μm	
FOM _s (MHz·pF/mW)	98,958	106,349	153,890	74,569	305,172
FOM _L [(V/μs)·pF/mW]	22,917	49,206	37,921	31,466	56,897
IFOM _s (MHz·pF/mA)	197,917	95,714	184,668	89,483	366,207
IFOM _L [(V/μs)·pF/mA]	45,833	44,286	45,506	37,759	68,276
LC-FOM _s (MHz/mW)	69,689	122,240	641,207	92,174	377,222
LC-FOM _L [(V/μs)/mW]	16,138	56,559	158,005	38,894	70,329

Fig. 16. Performance summary.

which evaluate the small-signal and large-signal performance with normalized power or current. Equation (32) gives a fair comparison for the simple Miller and nested Miller schemes, because those schemes show an almost invariant $GBW \cdot C_L$ for a specific design. The advanced Miller, which inserts gain stages into the Miller loop, however, shows C_L dependence. For example, combining (11) and (13) for the SMCC gives

$$\omega_{\text{Miller}} \approx \sqrt{g_{m2}g_{mL}/(C_{p2}C_L \tan \phi_{\text{Miller}})}. \quad (33)$$

Since the GBW is proportional to ω_{Miller} , (33) indicates that $GBW \cdot C_L \propto \sqrt{C_L}$. Therefore, (32) gives an increasing FOM with an increasing C_L for the advanced Miller schemes. Reference [19] proposes a large-capacitive load FOM (LC-FOM), which suffers less C_L variations by normalizing the FOM of (32) with the compensation capacitance C_{m1} ,

which is also proportional to $\sqrt{C_L}$, as is given in

$$LC\text{-FOM}_S = \frac{GBW}{\text{power}} \cdot \frac{C_L}{C_{m1}} \quad LC\text{-FOM}_L = \frac{SR}{\text{power}} \cdot \frac{C_L}{C_{m1}}. \quad (34)$$

The LC-FOM, although provides good comparison for the advanced Miller schemes with a single C_L , does not serve as a good indicator for the advanced Miller schemes with wide C_L range, such as [21] and this paper. When C_L has a wide range, the nondominant poles are determined by the smallest capacitive load C_{L_small} , instead of the largest load C_{L_large} . When driving C_{L_large} , the Miller loop T_{HF} is overdamped and results in an almost constant $\omega_{\text{Miller}} \cdot C_{L_large}$. For this reason, this paper applies (32) for comparison.

E. Experimental Results

The proposed amplifier was fabricated in 0.18- μm CMOS process and measured in a unity-feedback configuration. Fig. 12 shows the die photograph with a size of 0.013 mm². The device sizes are given in Table I.

The amplifier was verified to be stable for C_L between 1.5 and 18 nF while consuming 69.6 μW power from a 1.2 V supply. Fig. 13 shows the measured frequency responses of the amplifier when C_L is 1.5 and 18 nF, respectively. The amplifier achieves a GBW of 3.46 and 1.18 MHz, and a phase margin of 75.5° and 59.6° for C_L at 1.5 and 18 nF, respectively. The gain/phase margins with different C_L are summarized in Fig. 14, which shows that larger C_L reduces ω_{Miller} and leads to low phase margin, whereas smaller C_L reduces the gain margin. Fig. 15 shows the step transient responses when the amplifier is in unity feedback. When a 500-mV step is applied, the proposed amplifier achieves the average 1% settling time of 0.57 and 4.1 μs for C_L at 1.5 and 18 nF, respectively.

Finally, the performance summary in Fig. 16 shows that the proposed amplifier improves FOM_s ($\times 1.98$), FOM_L ($\times 1.5$), IFOM_s ($\times 1.98$), and IFOM_L ($\times 1.5$) compared with the state-of-the-art Miller-compensated multistage amplifiers.

V. CONCLUSION

A DOA for Miller compensation is presented that provides intuitive understanding on the nondominant poles and improves intuitions. The applicability of the method is verified by the design examples using various different Miller schemes. Guided by the above-mentioned method, a multistage amplifier driving a large C_L is proposed. The proposed amplifier exploits an active zero to cancel the pole of an inner gain stage. Because the proposed active zero shows higher frequency parasitic poles than the previous work, the amplifier achieves better performance under the same power and C_L . The prototype shows FOM_s ($\times 1.98$), FOM_L ($\times 1.5$), IFOM_s ($\times 1.98$), and IFOM_L ($\times 1.5$) superior to the prior state-of-the-art work.

APPENDIX

A two-pole system $T(s)$ with widely separated poles p_1 and p_2 can be represented as

$$T(s) \approx \frac{T_{\text{DC}}}{(1 + s/p_1)(1 + s/p_2)} \quad (\text{A.1})$$

where T_{dc} is the dc gain. The unity feedback of $T(s)$ is then

$$\begin{aligned} \frac{T(s)}{1 + T(s)} &\approx \frac{1}{1 + \frac{s}{T_{\text{DC}} p_1} + \frac{s^2}{T_{\text{DC}} p_1 p_2}} \\ &\approx \frac{1}{1 + \frac{s}{\omega_{\text{Miller}}} + \frac{s^2}{\omega_{\text{Miller}}^2 \tan \phi_{\text{Miller}}}} \end{aligned} \quad (\text{A.2})$$

where ω_{Miller} and ϕ_{Miller} are the bandwidth and phase margin of $T(s)$, respectively. Here, $\omega_{\text{Miller}} \approx T_{\text{dc}} p_1$ and $\phi_{\text{Miller}} \approx \tan^{-1}(p_2/\omega_{\text{Miller}})$.

When $T(s)/(1 + T(s))$ generates the nondominant poles to an amplifier, which has a bandwidth of the GBW with the

dc gain of A_{dc} , the overall amplifier can be represented as

$$A(s) \approx \frac{A_{\text{DC}}}{(1 + \frac{s \cdot A_{\text{DC}}}{\text{GBW}})(1 + \frac{s}{\omega_{\text{Miller}}} + \frac{s^2}{\omega_{\text{Miller}}^2 \tan \phi_{\text{Miller}}})}. \quad (\text{A.3})$$

The phase margin of the overall amplifier, ϕ_{overall} , is

$$\phi_{\text{overall}} \approx 90^\circ - \tan^{-1} \frac{\text{GBW}/\omega_{\text{Miller}}}{1 - \text{GBW}^2/(\omega_{\text{Miller}}^2 \tan \phi_{\text{Miller}})}. \quad (\text{A.4})$$

Solving (A.4) gives the relationship between the GBW and ω_{Miller} as

$$\begin{aligned} \chi &\approx \frac{\omega_{\text{Miller}}}{\text{GBW}} \\ &\approx \frac{2}{\sqrt{\tan^2 \phi_{\text{overall}} \tan^2 \phi_{\text{Miller}} + 4 \tan \phi_{\text{Miller}} - \tan \phi_{\text{overall}} \tan \phi_{\text{Miller}}}} \end{aligned} \quad (\text{A.5})$$

where χ is the separation factor between ω_{Miller} and the GBW. Given the phase margin of the overall amplifier and $T(s)$, χ can be derived. For example, $\chi \approx 2$ when $\phi_{\text{overall}} \approx \phi_{\text{Miller}} \approx 60^\circ$.

REFERENCES

- [1] W. C. Black, D. J. Allstot, and R. A. Reed, "A high performance low power CMOS channel filter," *IEEE J. Solid-State Circuits*, vol. 15, no. 6, pp. 929–938, Dec. 1980.
- [2] B. K. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-18, no. 6, pp. 629–633, Dec. 1983.
- [3] R. G. H. Eschauzier, L. P. T. Kerklaan, and J. H. Huijsing, "A 100-MHz 100-dB operational amplifier with multipath nested Miller compensation structure," *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1709–1717, Dec. 1992.
- [4] G. Palmisano and G. Palumbo, "A compensation strategy for two-stage CMOS opamps based on current buffer," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 44, no. 3, pp. 257–262, Mar. 1997.
- [5] F. You, S. H. K. Embabi, and E. Sánchez-Sinencio, "Multistage amplifier topologies with nested G_m -C compensation," *IEEE J. Solid-State Circuits*, vol. 32, no. 2, pp. 2000–2011, Dec. 1997.
- [6] K. N. Leung, P. K. T. Mok, W.-H. Ki, and J. K. O. Sin, "Three-stage large capacitive load amplifier with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 35, no. 2, pp. 221–230, Feb. 2000.
- [7] G. Palmisano, G. Palumbo, and S. Pennisi, "Design procedure for two-stage CMOS transconductance operational amplifiers: A tutorial," *Analog Integr. Circuits Signal Process.*, vol. 27, no. 3, pp. 179–189, May 2001.
- [8] G. Palumbo and S. Pennisi, "Design methodology and advances in nested-Miller compensation," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 49, no. 7, pp. 893–903, Jul. 2002.
- [9] H. Lee and P. K. T. Mok, "Active-feedback frequency-compensation technique for low-power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 511–520, Mar. 2003.
- [10] H. Lee, K. N. Leung, and P. K. T. Mok, "A dual-path bandwidth extension amplifier topology with dual-loop parallel compensation," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1739–1744, Oct. 2003.
- [11] R. Mita, G. Palumbo, and S. Pennisi, "Design guidelines for reversed nested Miller compensation in three-stage amplifiers," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 50, no. 5, pp. 227–233, May 2003.
- [12] X. Peng and W. Sansen, "AC boosting compensation scheme for low-power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 2074–2079, Nov. 2004.
- [13] K. H. Lundberg, "Internal and external op-amp compensation: A control-centric tutorial," in *Proc. Amer. Control Conf.*, Jun./Jul. 2004, pp. 5197–5211.

- [14] X. Fan, C. Mishra, and E. Sánchez-Sinencio, "Single Miller capacitor frequency compensation technique for low-power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 584–592, Mar. 2005.
- [15] A. D. Grasso, G. Palumbo, and S. Pennisi, "Advances in reversed nested Miller compensation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 7, pp. 1459–1470, Jul. 2007.
- [16] A. D. Grasso, D. Marano, G. Palumbo, and S. Pennisi, "Improved reversed nested Miller frequency compensation technique with voltage buffer and resistor," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 54, no. 5, pp. 382–386, May 2007.
- [17] W. Aloisi, G. Palumbo, and S. Pennisi, "Design methodology of Miller frequency compensation with current buffer/amplifier," *IET Circuits, Devices Syst.*, vol. 2, no. 2, pp. 227–233, Apr. 2008.
- [18] X. Peng, W. Sansen, L. Hou, J. Wang, and W. Wu, "Impedance adapting compensation for low-power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 445–451, Feb. 2011.
- [19] S. Guo and H. Lee, "Dual active-capacitive-feedback compensation for low-power large-capacitive-load three-stage amplifiers," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 452–464, Feb. 2011.
- [20] S. S. Chong and P. K. Chan, "Cross feedforward cascode compensation for low-power three-stage amplifier with large capacitive load," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2227–2234, Sep. 2012.
- [21] Z. Yan, P.-I. Mak, M.-K. Law, and R. P. Martins, "A 0.016-mm² 144- μ W three-stage amplifier capable of driving 1-to-15 nF capacitive load with >0.95-MHz GBW," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 527–540, Feb. 2013.
- [22] W. Qu, J.-P. Im, H.-S. Kim, and G.-H. Cho, "A 0.9 V 6.3 μ W multistage amplifier driving 500pF capacitive load with 1.34 MHz GBW," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 290–291.
- [23] M. Tan and W.-H. Ki, "A cascode Miller-compensated three-stage amplifier with local impedance attenuation for optimized complex-pole control," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 440–449, Feb. 2015.
- [24] R. G. H. Eschauzier and J. H. Huijsing, *Frequency Compensation Techniques for Low-Power Operational Amplifiers*. Norwell, MA, USA: Kluwer, 1995.
- [25] K. Ogata, *Modern Control Engineering*, 4th ed. Upper Saddle River, NJ, USA: Prentice-Hall, 2002.



Wanyuan Qu received the B.S. degree in telecommunications engineering (Hons.) from the Beijing University of Posts and Telecommunications, Beijing, China, in 2006, and the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2008 and 2016, respectively.

Since 2008, he has been with Silicon Works Ltd., Daejeon, South Korea, where he is currently a Senior Analog Circuit Designer. He has successfully designed and mass-produced several ICs in the automotive, lighting, and mobile display applications. His current research interests include CMOS mixed-signal integrated circuit design, multistage amplifier, low-dropout regulator, automotive dc/dc converter, and LED lighting and LED backlight driver designs.



Shashank Singh (S'04) received the B.Tech. degree in electronics engineering from the Govind Ballabh Pant University of Agriculture and Technology, Pantnagar, India, in 2002, and the M.Tech. degree in electrical engineering from IIT Bombay, Bombay, India, in 2004.

Ever since 2013, he has joined Samsung Electronics, Inc., Hwasung, South Korea, where he was involved in the design of the power management circuits and analog front-ends, including signal conditioning. He was with Intel Corporation, Bangalore, India, during 2011–2013, with Freescale Semiconductor, Noida, India, during 2006–2011, and with Tata Consultancy Service Ltd., Bangalore, India, during 2004–2006. His current research interests include power management and low-noise and low-voltage analog design for the mobile and internet-of-things applications.



Yongjin Lee (S'15) received the B.S. degree from Sogang University, Seoul, South Korea, in 2013, and the M.S. degree from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2015.

In 2015, he joined Samsung Electronics, Inc., Hwasung, South Korea, where he was involved in the design of the digital low drop-out regulators. He is currently with the Mixed Signal Core Design Team. His current research interests include analog circuits about power management and thermal management in the mobile application processor.



Young-Suk Son was born in 1971. He received the B.S. degree from Kyung-Pook National University, Daegu, South Korea, in 1994, the M.S. degree in electrical engineering from Pohang University of Science and Technology, Pohang, South Korea, in 1996, and the Ph.D. degree in electrical engineering from Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2008.

From 1996 to 2001, he was with LG Semiconductor Company Ltd., Cheongju, South Korea. From 2002 to 2005, he was with the System LSI Business Division, Samsung Electronics Company Ltd., Yongin, South Korea, as a Senior Engineer, where he was involved in developing single-chip transceiver ICs for GSM/GPRS/EDGE. Since 2005, he has been with Silicon Works Company, Ltd., Daejeon, South Korea, as a Leader of the Analog Design Team, where he is involved in developing numerous state-of-the-art column driver ICs for active-matrix liquid crystal displays (AMLCDs) and active-matrix organic LED (AMOLED) displays. His current research interests include current-mode data driving technology for AMOLED applications and next generation column driver architectures for AMLCD applications, and extremely low power analog circuit designs, LED drivers, motor drivers, and dc/dc converters.



Gyu-Hyeong Cho (S'76–M'80–SM'11–F'16) received the B.S. degree from Hanyang University, Seoul, South Korea, in 1975, and the M.S. and Ph.D. degrees from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 1977, and 1981, respectively, all in electrical engineering.

During 1982–1983, he was with the Westinghouse Research and Development Center, Pittsburgh, PA, USA. In 1984, he joined the Department of Electrical Engineering, KAIST, where he has been a Full Professor since 1991. He has authored one book on advanced electronic circuits, and authored or co-authored over 200 technical papers. He holds 80 patents. His research interests included power electronics until the late 1990s, and he was involved in soft switching converters and high power converters. Later, he shifted to analog integrated circuit design, and his current research interests include power management ICs, Class-D amplifiers, and touch sensors and drivers for AMOLED and LCD flat panel displays and biosensors.

Dr. Cho served as a member of the ISSCC International Technical Program Committee. He received the Outstanding Teaching Award from KAIST. He was a Guest Editor in 2010. He is an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS.