Efficient Digital Quadrature Transmitter Based on IQ Cell Sharing

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***Abstract*— In this paper, we proposed and designed a digitally configured versatile RF quadrature transmitter. The transmitter efficiency was enhanced by IQ cell sharing and the deactivation of cells of opposite phases. In simulation, these techniques were able to increase the average efficiency of the transmitter from 46.3% to 70.7% for a 6.9-dB PAPR LTE signal. Moreover, the number of power amplifying cells was halved, improving the total efficiency of the transmitter. The proposed transmitter was implemented in a 6-b configuration at 0.8 GHz using a 28-nm CMOS process. Furthermore, the performance of the transmitter was verified. The dynamic range of the measured output power was in the range −20.2 to 13.9 dBm, and the measured average output power was 6.97 dBm for the 6.9-dB PAPR LTE signal. The measured power-added efficiencies of the transmitter at the peak power and average power were 40.43% and 29.1%, respectively.**

***Index Terms*— CMOS RF integrated circuits, digital-intensive transmitter, quadrature transmitter, RF DAC, software-defined radio (SDR) application, switched capacitor.**

I. Introduction

As THE volume of wireless data transfer increases, new complex communication standards have to be adopted continuously. Consequently, an interest in software-defined radio (SDR) transceivers is emerging, in order to support the multimode, multiband standards. A digital-intensive transmitter has many advantages for use in a flexible transceiver. Unlike analog transmitters, digital transmitters align with Moore′s law to a far better degree as the CMOS process scales down. On the other hand, the analog transmitter has a limit on CMOS scaling. Due to the nature of the digital circuit, it provides excellent programmability, making it suitable for SDR applications. Moreover, it is also easier to integrate the transmitter as a system-on-a-chip (SoC) with non-RF circuits, such as modems and various application processors, which are fully digital circuits.

The RF transmitter is classified as a quadrature transmitter and a polar transmitter as shown in Fig. 1(a) and (b). The polar transmitter is based on the polar coordinate signal consisting of the phase and amplitude information. The quadrature transmitter is based on the cartesian coordinate signal consisting of the in-phase (I) and quadrature phase (Q) information. The digital transmitter comprises many direct digital-to-RF conversion (DRFC) cells, which present the signal by thermometer codes or in an equivalent format. The polar transmitter transforms the I and Q signals into the amplitude and phase signals using a coordinate rotation digital computer (CORDIC). The phase information is upconverted to the RF carrier frequency, which becomes the input to the DRFC unit cells. Furthermore, the inverter in the DRFC unit amplifies the signal functioning as a power amplifier (PA). The amplitude signal is handled by the ON/OFF switching of the DRFC cells. The RF signal in the quadrature transmitter is obtained by summing the I and Q signals, which are expressed by the DRFC cells as shown in Fig. 1(a).

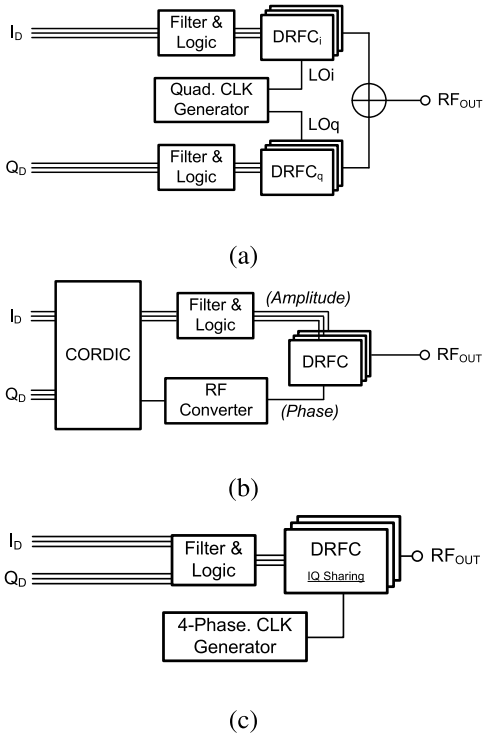

Fig. 1. Digital-intensive transmitter. (a) Quadrature architecture. (b) Polar architecture. (c) Proposed quadrature architecture.

The efficiency of the entire transmitter chain is strongly dependent on its PA efficiency. The polar architecture is advantageous for processing the nonconstant envelope signal, produced by QAM, OFDM, and QPSK, which have

Manuscript received November 26, 2015; revised April 22, 2016, July 14, 2016, September 13, 2016, and December 30, 2016; accepted January 13, 2017. Date of publication February 6, 2017; date of current version April 20, 2017. This paper was approved by Associate Editor Ali M. Niknejad.

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Digital Object Identifier 10.1109/JSSC.2017.2655058

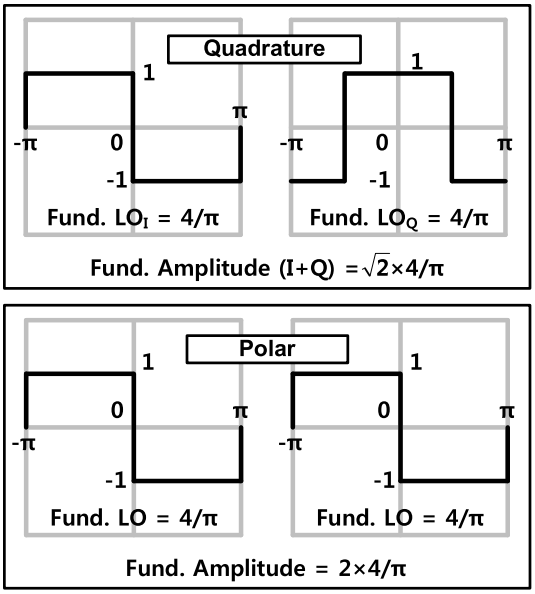


Fig. 2. LO shape in the transmitters and their fundamental components.

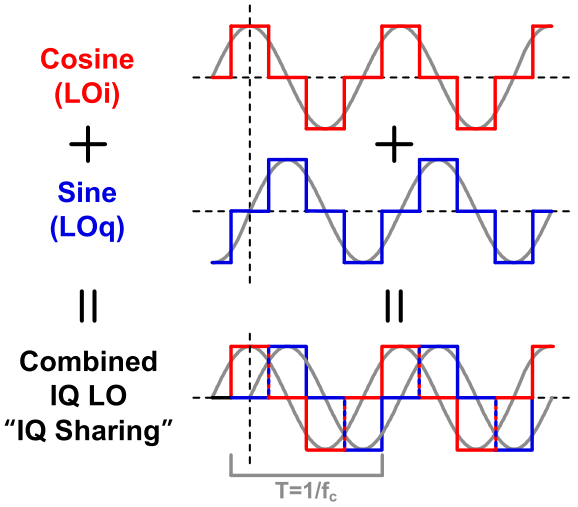


Fig. 3. Waveforms of three-level LO$_i$ and LO$_q$ and its combined IQ Sharing LO.

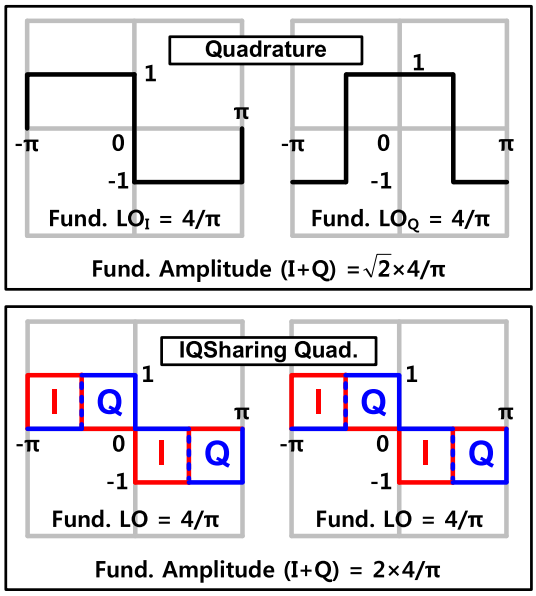


Fig. 4. LO waveform shapes and their fundamental components in conventional quadrature LO and IQ Sharing LO.

large spectrum. The polar transmitter has a high efficiency, because the amplitude information in polar form does not have any phase difference, contrasting the quadrature transmitter by 90° phase difference of I and Q signals. CMOS digital PAs, using the polar concept, have been extensively reported because of the advantage of the digital polar architecture [1]–[4]. However, converting the IQ to polar form, using CORDIC, is a severe burden as described in [8], due to: 1) the complex algorithm for realization; 2) the high-frequency operation for iteration; 3) CORDIC circuit nonlinearity (quantization noise and so on); 4) system complexity for meeting the stringent linearity; and 5) the large signal bandwidth of the phase path (about ten times), and the amplitude path (about two to three times) when compared with the signal bandwidth.

In contrast, the quadrature transmitter does not require the CORDIC, thus lowering the computing cost. This advantage can have a significant impact on a communication system with a large signal bandwidth. Due to these advantageous characteristics, the quadrature transmitters have been studied, in order to eliminate the cumbersome CORDIC [5]–[12].

Since the digital transmitters are configured using many cells, combining the cell outputs is a key design issue. A Gilbert mixer structure linearly combines the output currents. Due to the operation voltage being fixed, the output impedance of the Gilbert mixer is inversely proportional to the number of the on-cells. To overcome output impedance variation with the cell switching operation, the switched capacitors are used to linearly combine the outputs from each conversion cell. In the polar transmitter with the switched capacitor combiner [13], [14], the output impedance is constant as determined by the total sum of the combining capacitors regardless of the ON/OFF cell condition. Moreover, this architecture delivers much higher output power and efficiency than previously reported ones. In [12] and [15], the switched capacitor combiner is utilized in the quadrature transmitter to eliminate the issues of the polar architecture. However, due to the 90° phase difference of the conventional digital I and Q LOs, the output power of the conventional quadrature transmitter is lower than that of the polar transmitter by 3 dB when the magnitudes of I and Q are equal.

In the digital-intensive architectures with functional flexibility, the algorithms that can improve the performances can be easily implemented. In [16]–[18], a 2-D digital predistortion technique is applied to eliminate the nonlinearity of the digital PA in the digital quadrature transmitter. A transmitter based on the shared power amplifying cell structure is reported in [18] and [19]. This architecture allows a power amplifying cell to deliver both I and Q information simultaneously, thereby halving the required number of cells, as shown in Fig. 1(c). A dual-band digital transmitter is proposed in [18], combining the I and Q signals by an OR operation with complementary decoding scheme. Although [19] adopted the three-level LO

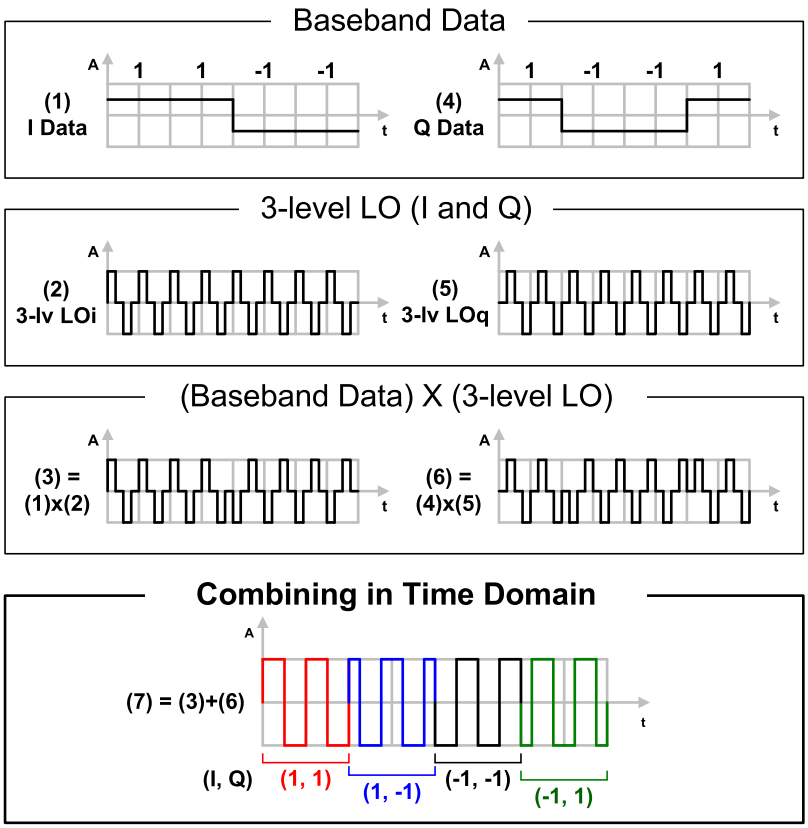


Fig. 5. Waveforms of I/Q data, three-level LOs, upconverted signals, and their combined signal.

concept, the upconverted signal at the power generation stage is processed at the two-level LO speed. The transmitter is further enhanced by using the switched capacitor combiner and digital processing techniques.

This paper introduces a detailed analysis of the transmitter with extensive measurement data. The efficiency enhancement technique based on IQ cell sharing and the deactivation of cells of the opposite phase is detailed in Section II. Section III explains the circuit implementation. The charging/discharging (C/D) loss analysis of the quadrature transmitter is described in Section IV. The experimental results are presented in Section V, and finally, the conclusions from this paper are presented in Section VI.

II. Digital Quadrature Transmitter Architecture

A. Conventional Digital Quadrature Transmitter

The output voltage of a general quadrature transmitter is given by

$$\text{Amplitude } (V) = \sqrt{I^2 + Q^2} \tag{1}$$

$$\text{Phase } (\Theta) = \tan^{-1}\frac{Q}{I}. \tag{2}$$

Because the transmitter uses the square type I and Q LOs with phase difference of 90° and 50% duty cycle for the Class-D type switching operation, the voltage amplitude can be determined from the Fourier series of the LO

$$\text{Amplitude } (V) = \frac{4}{\pi}\sqrt{I^2 + Q^2}. \tag{3}$$

Unlike the quadrature transmitter that requires I and Q signals for output generation, the polar transmitter represents the RF signal by the amplitude information and the phase-aligned LO information.

The I and Q LO waveforms of the quadrature and polar transmitters are shown in Fig. 2. The fundamental amplitude of the polar transmitter from the two cells is 2, because the two cells are operating in-phase. However, the fundamental amplitude in the quadrature case with the I and Q cells is $\sqrt{2}$-times smaller than in the polar case, because I and Q are 90° of phase difference. Therefore, when the same number of PA cells is used, the power of the quadrature transmitter is lower than that of the polar transmitter and the efficiency is also lower. This is the main disadvantage of the quadrature transmitter.

Despite this drawback, the quadrature transmitter is still a preferable architecture, as it does not require CORDIC, which expands the signal bandwidth by about ten times. Moreover, the drawback of the quadrature transmitter can be eliminated using signal mapping techniques that are introduced in Section II-B.

B. Techniques to Increase Efficiency

1) RF Waveform Shaping (IQ cell Sharing): To overcome the 3-dB power loss due to the quadrature LO shape, we propose a transmitter using three level I and Q LOs that enable time-division multiplexing as shown in Fig. 3. The LO waveforms have three levels (1, 0, and -1), and I and Q do

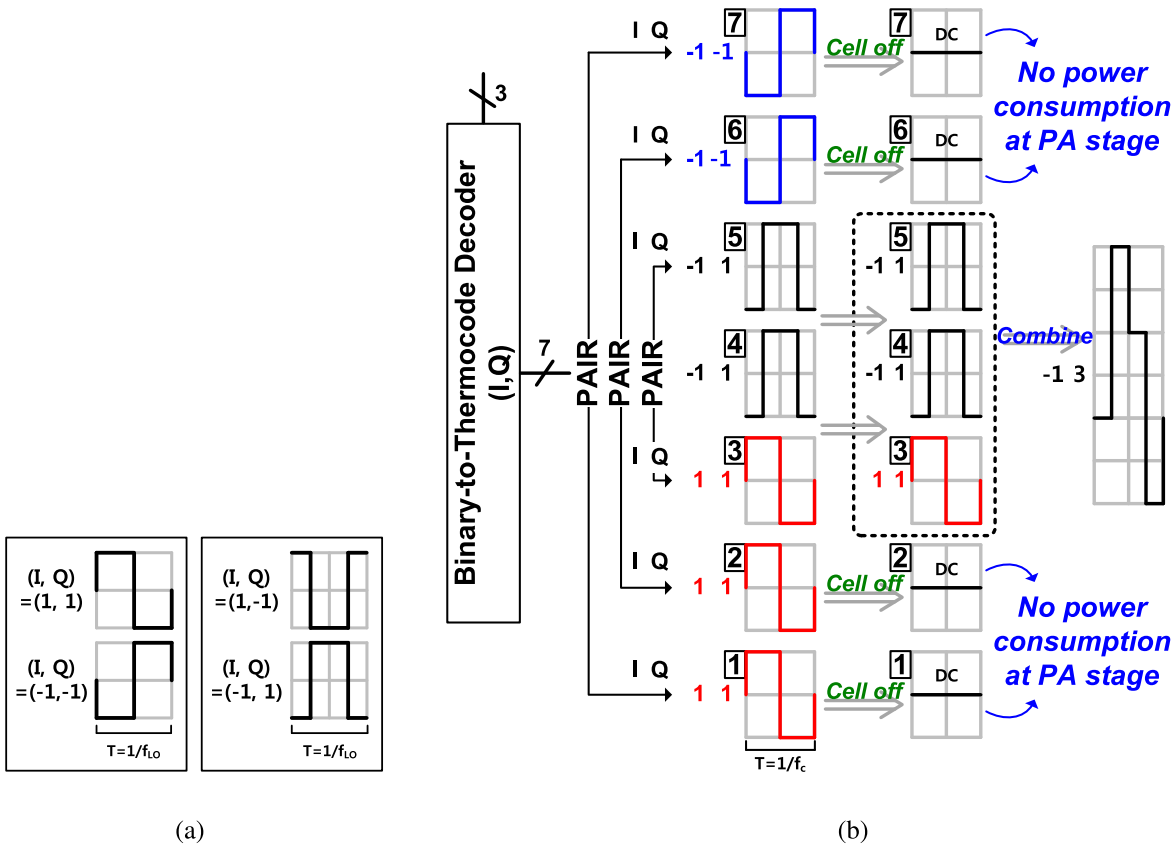


Fig. 6. (a) Opposite waveform pairs in the IQ Sharing operation. (b) DOC operation example of the transmitter having $(I,Q) = (-1,3)$.

not have the signal amplitudes of 1 or -1 at the same time. Therefore, the I and Q waveforms can be combined in the time domain, resulting in a two-level waveform, as shown in Fig. 3. With this architecture, the signal is processed using the three-level I and Q LOs. However, this transmitter operates as a two-level signal, at the power consuming amplifying chain, without increasing the switching frequency.

The waveforms of the proposed three-level LO and conventional LO with 50% duty cycle and 90° phase difference are shown in Fig. 4. The conventional LO has two cells (I and Q) with a fundamental amplitude of $4/\pi$, being 90° of phase difference. The sum of the fundamental amplitudes from the two cells is $\sqrt{2} \times 4/\pi$. The proposed three-level LO, which can express the I and Q bits simultaneously by time sharing, has two identical cells with the same amplitude of $4/\pi$. The amplitude from the two cells of the proposed LO is $2 \times 4/\pi$, indicating that the proposed LO generates a higher 3-dB power than the conventional LO, and the same amount of power as in the polar case is shown in Fig. 2. In short, the IQ Sharing technique can compensate for the 3-dB power loss of the quadrature transmitter. The two identical cells can be replaced by one double sized cell, reducing the number of power-generating cells. Thus, this technique enhances the efficiency of the transmitter, and the required number of power cells is halved, in comparison with the conventional quadrature with the same resolution.

Fig. 5 shows the signal processing steps of the proposed architecture. Fig. 5(1) and (4) represents the baseband

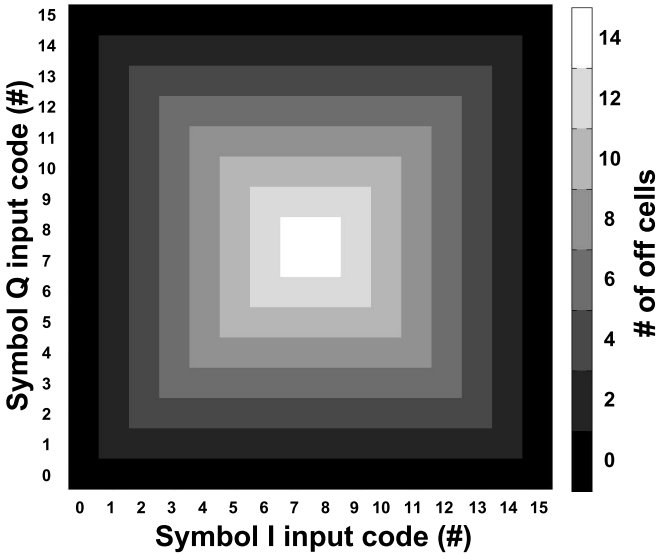


Fig. 7. Number of the deactivated cells on 4-b IQ plane of the IQ Sharing transmitter.

I and Q signals, respectively. Moreover, Fig. 5(2) and (5) represents the conceptual I and Q LO signals, respectively. After the I and Q signals are upconverted by the I and Q LO signals, the resulting waveforms are shown in Fig. 5(3) and (6). These upconverted I and Q signals can be combined in the time domain, to (7), a two-level waveform. Therefore, a pair of I and Q signals can be amplified by a single

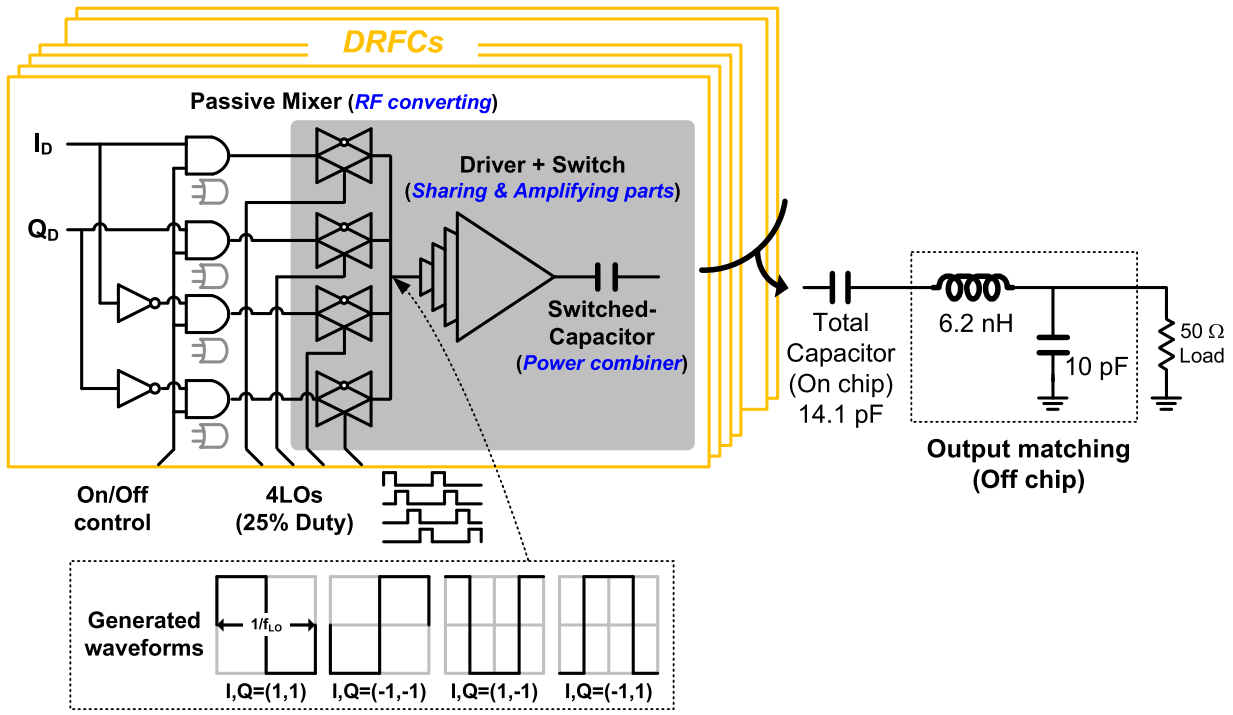


Fig. 8. Schematic of DRFC with the IQ Sharing waveforms and matching circuit.

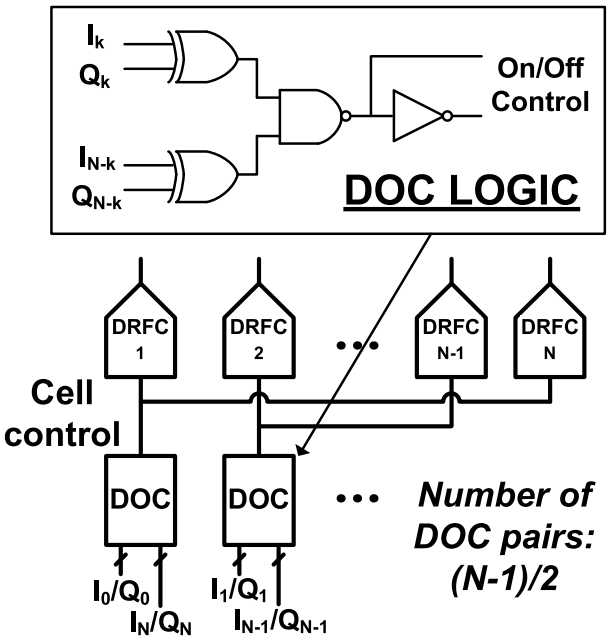


Fig. 9. Schematic of DOC logic.

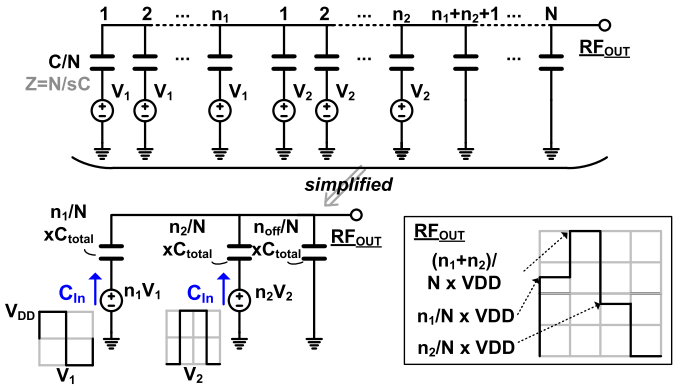


Fig. 10. Operation of switched capacitor to combine DRFC's output of the quadrature transmitter, its equivalent circuit, and output amplitude.

power-generating cell, using the two-level waveform, owing to the lack of overlap in the time domain. In this way, the number of power-generating cells is halved in comparison with the conventional quadrature case. The processed signals have an LO frequency that is identical to the conventional ones, except in the baseband signal transition region. However, the transition effect is negligible due to the low occurrence.

2) Data Processing (Deactivating Cells of the Opposite Phase): The digital transmitter consists of many DRFC cells for expressing the signal amplitude. By combining the outputs of the cells, an accurate digital RF output signal is generated. In the quadrature transmitter, the signal is represented by the cells with $+1$ or -1, which can be canceled each other out. The canceled operations do not produce any outputs, and the unnecessary operations should be deactivated in each DRFC to reduce the C/D loss of the switching stage. The cell pairs delivering 180° out-of-phase signals are deactivated at the digital logic stage with very little power consumption.

Unlike the conventional quadrature case in [15], the I and Q in the IQ Sharing cannot be canceled out independently, because the I and Q bit is converted to an RF signal by a single DRFC cell. Only the sharing cell pairs with the out-of-phase signals can be deactivated, as shown in Fig. 6(a). Fig. 6(b) shows an example of a 3-b IQ Sharing transmitter

with seven cells delivering the output $(I, Q) = (-1, 3)$. The upconverted baseband signal has one of four IQ Sharing waveforms as shown in Fig. 6(a). The LO waveforms of the IQ Sharing are represented by two levels: $+1$ (VDD) or -1 (GND), as shown in Fig. 4. The I/Q data in the example has two sets of $(-1, -1)$, two sets of $(-1, 1)$, and three sets of (1, 1). In this scenario, the cell pairs 1 and 7 and 2 and 6 have the out-of-phase output waveforms that can be turned OFF (deactivated) without affecting the combined output. We call this operation the deactivation of opposite cell (DOC) technique.

When the I and Q symbols in the total N cells have k or N-k values, where k is a positive integer from 0 to N/2, the total number of cells able to be deactivated is 2k. Fig. 7 shows the number of deactivated pairs in the 4-b IQ Sharing transmitter using the DOC technique in the IQ plane. The DOC appears frequently in the low-power region, and this technique boosts the efficiency more at lower powers where a large number of cell pairs can be deactivated. For the highly modulated signal with high Peak-to-Average Power Ratio (PAPR), the DOC technique is very effective.

III. Circuit Implementation

A. DRFC for IQ Sharing

Fig. 8 shows the block diagram of a unit DRFC cell in the IQ Sharing transmitter. The mixer structure is the same as the conventional passive mixer. The mixer consists of a transmission gate and a logic circuit, to multiply the data and carrier LO, for creating the one of four IQ Sharing waveforms. The mixer LO is a four phase signal with 25% duty cycle. To generate the IQ Sharing waveforms, the new mapping method is adopted. Consequently, a single power-generating cell can express one pair of I/Q data.

Due to degraded linearity caused by the LO duty cycle mismatch and phase mismatch, a symmetric LO routing and buffer design are essential. The four phase LOs are supplied to the DRFC cells by binary clock tree, which has gradually increasing sized inverter branches. To support the 25% duty cycle with high fidelity, we adopt a larger buffer (1.5 times greater) than the conventional transmitter using a 50% duty cycle LO. However, the power consumption of the larger buffer is insignificant, because the power portion of the clock buffer is under 5% of the total power consumption.

Moreover, the switch size on the DRFC′s power amplifying inverter design is important. A large sized switch can provide good linearity, because the ON-resistance is small and the switching capacitor can be driven quickly; however, the large switch consumes more driving power.

B. Logic Circuit for DOC

For the DOC operation, the phase relation of the thermocoded cell pairs with the same size is compared by the logic circuit in order to determine whether they will be OFF or not. In the previous example shown in Fig. 6, the DRFC cells transmit the four-type waveforms, and two pairs are transmitting the out-of-phase waveforms. When the two cells transmit signals with the out-of-phase waveforms, they are deactivated. This is performed by a DOC logic shown in Fig. 9, which consumes very little power. In the DOC operation, one cell is placed at VDD $(+1)$ and the other at GND (-1). Therefore, the two cells do not produce any output power and the cells are not switching at the carrier frequency.

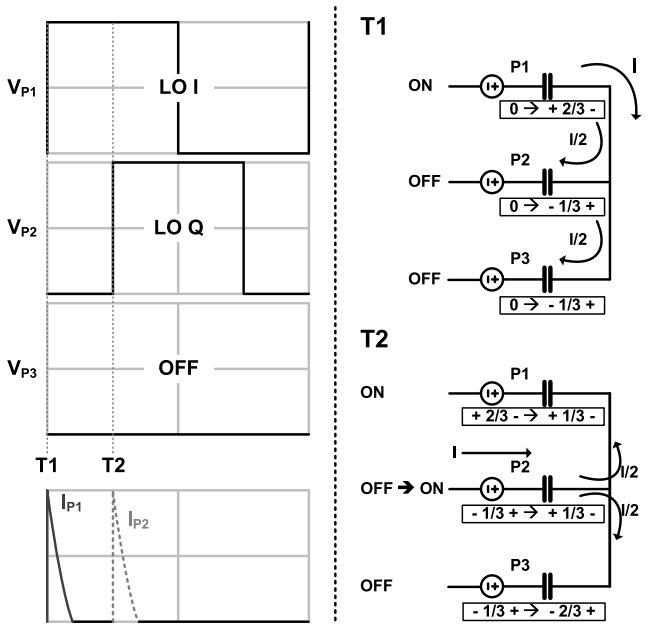


Fig. 11. Current flows in the switched capacitor voltage combiner. Three cells (P1, P2, and P3) are charged/discharged at different time slots of T1 and T2.

C. Switched Capacitor Power Combiner

The outputs from the DRFC cells should be combined accurately without generating any distortion. For this purpose, the outputs are combined using the switched capacitor [13]. Fig. 10 shows the switched capacitor voltage combiner with its Thevenin equivalent circuits, where the output voltage is exactly proportional to the number of the on-cells. For the VDD supply voltage, the fundamental component of LO, $V_{\rm lo}$, the output voltage $V_{\rm out}$, and the output power $P_{\rm out}$ are given by

$$V_{\rm lo} = \frac{2}{\pi} V_{\rm DD} \tag{4}$$

$$V_{\rm out} = C_{\rm total} \left(\frac{n_1 + n_2}{N} \right) V_{lo} \tag{5}$$

$$P_{\rm out} = \frac{1}{2} \frac{V_{\rm out}^2}{R_{\rm load}} \tag{6}$$

where $C_{\rm total}$ is the sum of the total series capacitors. n_1 and n_2 are the numbers of the on-cells for all phase states shown in Fig. 10, and N is the total number of capacitor cells. $R_{\rm load}$ is the load resistance at the carrier frequency after tuning out the capacitance $C_{\rm total}$. The output of the switched capacitor combiner is the amplified RF signal, and should be properly matched to get the power. When the total capacitance $C_{\rm total}$ is tuned out by a bandpass filter, the signal source drives the load resistance directly without any loss. Therefore, the output power of this transmitter is determined by the resistive load.

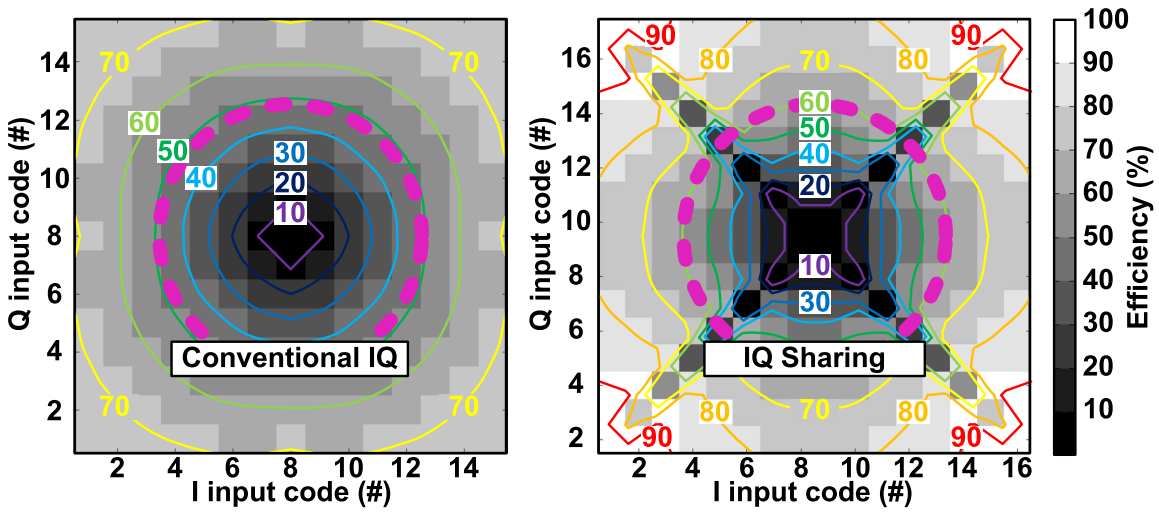


Fig. 12. Efficiency contours considering P_{out} and C/D loss only in the transmitters: conventional quadrature (left) and IQ Sharing (right). The dotted magenta circles are the average power region of the modulated signals (16 QAM LTE).

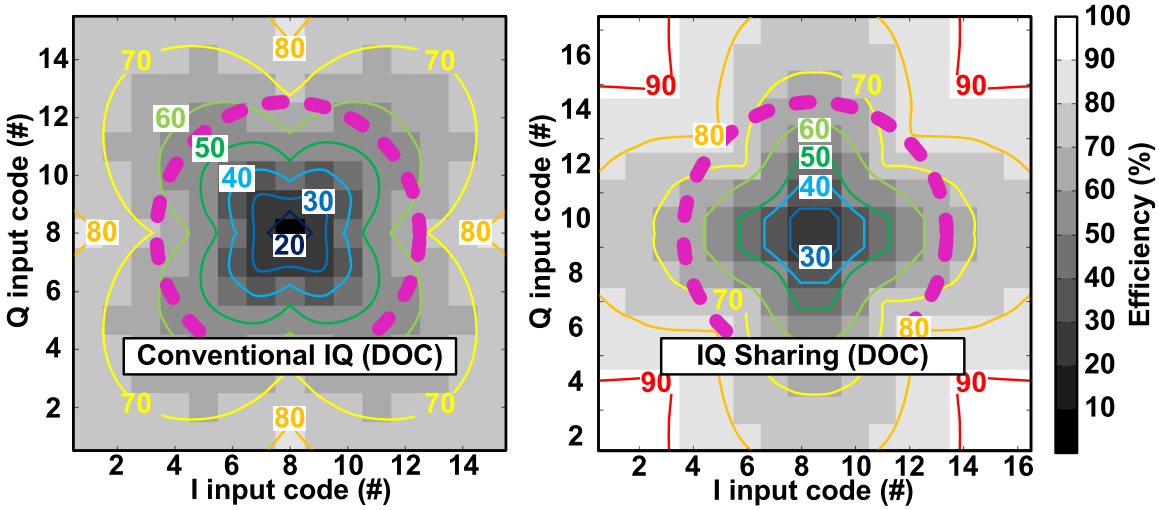


Fig. 13. Efficiency contours considering P_{out}, C/D loss, and DOC in the transmitters: conventional quadrature (left) and IQ Sharing (right). The dotted magenta circles are the average power region of the modulated signals (16 QAM LTE).

The switching operation of the power amplifying inverter stage consumes the majority of the power and determines the total efficiency. The losses of the amplifying cells are the ON-resistance loss of the transistor and the C/D loss of the combining capacitors. With this architecture, the signal fidelity is determined by the input code resolution and the sampling noise. Although the higher code resolution provides better adjacent channel leakage ratio (ACLR) in theory, the improvement is saturated at some point due to the circuit imperfection in the implementation process as shown in [8].

IV. C/D Loss Analysis of the Quadrature Transmitter

A. C/D Loss Analysis

The capacitor array is charged and discharged using the distributed Class-D type switches and the output of each cell is voltage combined, as shown in Fig. 10. The output voltage can be defined as in (5) being dependent on the drain voltage VDD of the switches, the number of the DRFC cells, turned-ON cells, and the LO waveform. The Fourier coefficient of the fundamental component varies according to the LO shape. As shown in the Thevenin model depicted in Fig. 10, there is no impedance variation related to cell switching. Here, we assume that the capacitance and ON-resistance of the switching device are small compared with the unit capacitance in the array and the load resistance. The main loss of the switched capacitor structure is the C/D loss of the capacitors, given that the voltage source directly drives the resistive load, under the condition that the capacitance is tuned. For the polar transmitter, all the cells are charging and discharging at the same time, and the C/D loss, P_{sc}, is determined by the number of the ON-state cells among N total cells as given by [13]

$$P_{\text{sc}} = C_{\text{in}} V^2 f \tag{7}$$

$$C_{\text{in}} = \frac{n(N-n)}{N^2} C_{\text{total}} \tag{8}$$

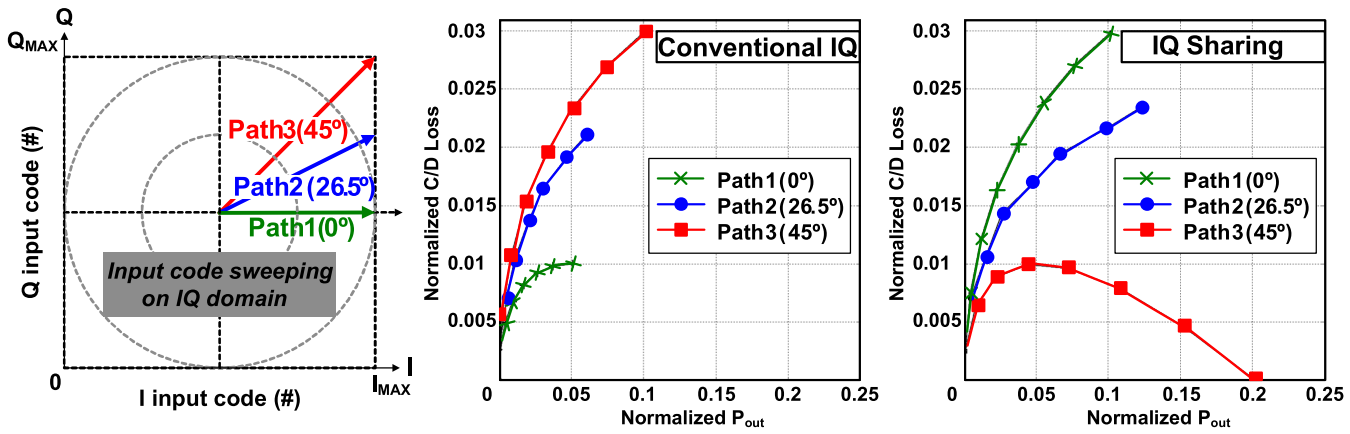


Fig. 14. Comparison of conventional quadrature IQ versus IQ Sharing along the three paths in I/Q plane. Their values are expressed relatively for comparison of the two transmitters. DOC technique is applied.

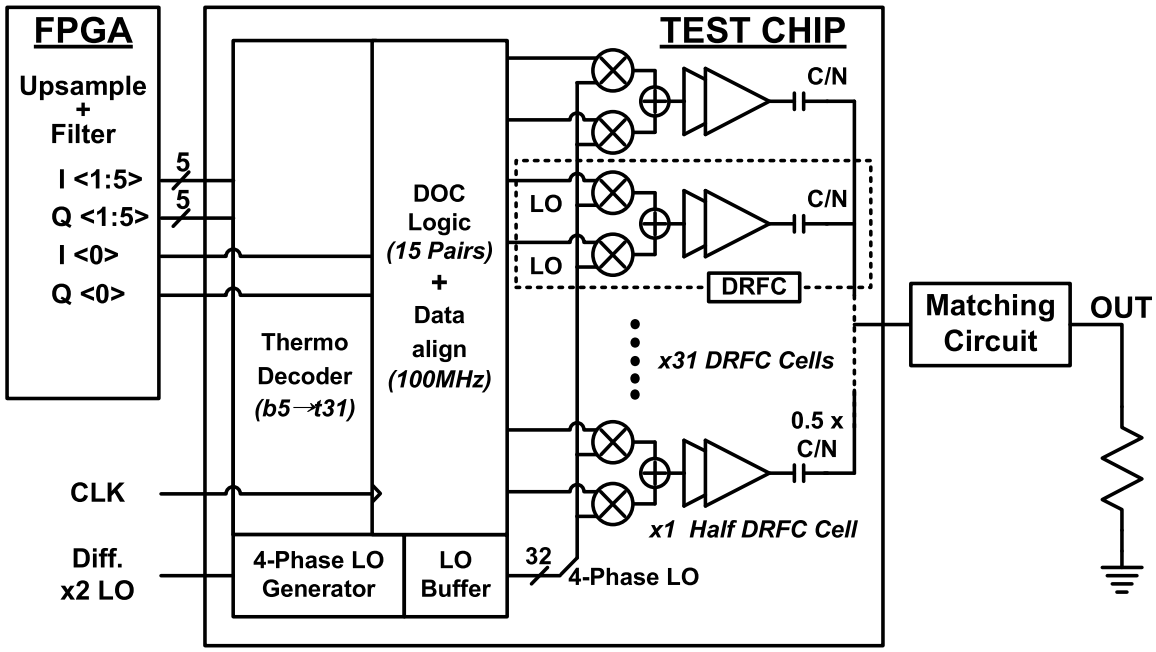


Fig. 15. Block diagram of the implemented 6-b IQ Sharing transmitter.

where C_{in} is the effective input capacitance varying with the number of the ON-state cells, C_{total} is the total capacitance, V is the voltage across the capacitor, which is VDD loaded by the switch, and f is the switching frequency (carrier frequency).

In a quadrature transmitter, the I and Q cells do not turn ON and OFF simultaneously and have three switching cases (I ON, Q ON, and OFF), as shown in Fig. 10. Thus, there are two charge steps for turning ON the I and Q cells, and the charging powers for the two cases (T1 and T2 cases) are evaluated in Fig. 11. The cells driven by the phase lead LO (LO I) are charged at T1. At this time, C_{in} and the C/D loss are similar to the polar transmitter. The C/D loss of the quadrature transmitter using the switched capacitor is

$$P_{\text{scT1}} = \frac{n_1(n_2 + n_{\text{OFF}})}{N^2} C_{\text{total}} V^2 f \tag{9}$$

$$P_{\text{scT2}} = \frac{n_2(n_1 + n_{\text{OFF}})}{N^2} C_{\text{total}} V^2 f. \tag{10}$$

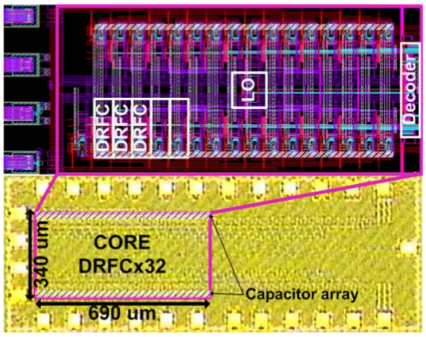


Fig. 16. Die micrograph and core layout.

In (9) and (10), n_1 is the number of the cells in the phase lead state, while n_2 is the number of the cells with the phase lag state. At T2, the cells driven by the phase lag (LO Q) are

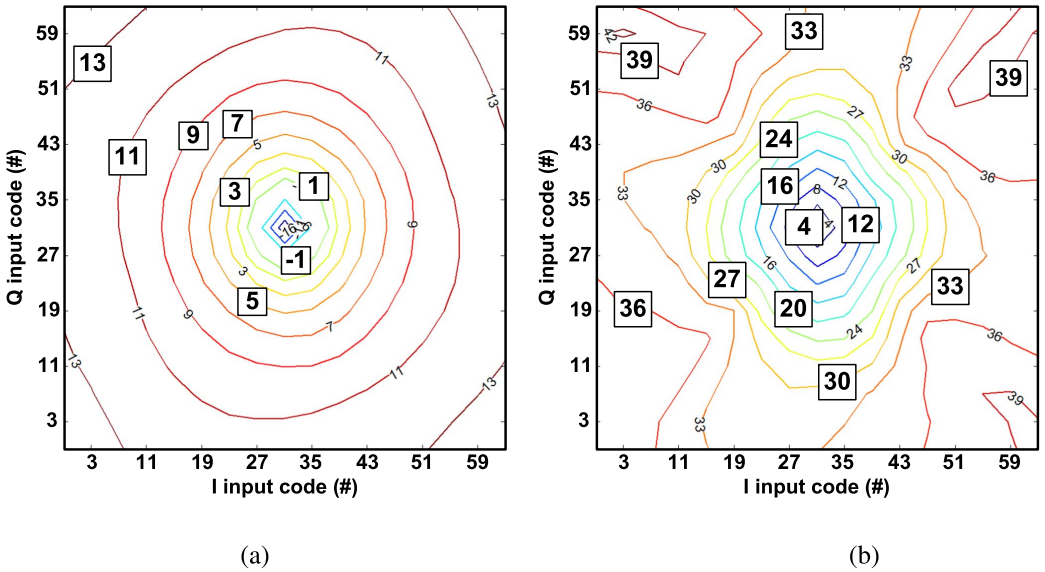


Fig. 17. CW measurement results of (a) output power (dBm) contours and (b) efficiency (%) contours.

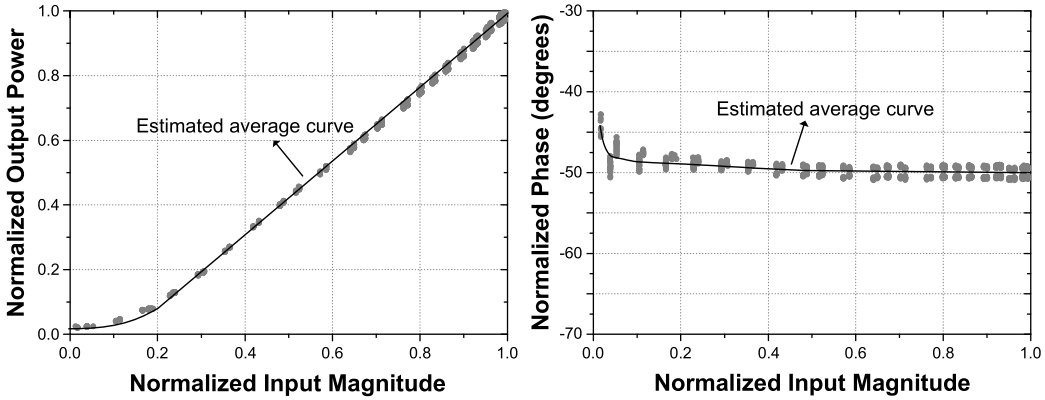


Fig. 18. Measured AM–AM and AM–PM results for a 2-MHz spacing two-tone signal.

turned ON. Owing to the voltage of the cells turned ON at $T1$ being constant at VDD, and additional Q cells being turned ON to VDD, the charging power is identical to (9) with n_2 being the number of Q cell. This calculation can be adopted for the IQ Sharing architecture, because there are two types of LO with 90° phase difference in the IQ Sharing transmitter operation shown in Fig. 6, the same as the operation of the conventional quadrature transmitter.

B. C/D Loss Versus Output Power

Based on the formulas (6), (9), and (10), the ideal efficiencies of the IQ Sharing transmitter and the conventional quadrature transmitter can be compared. In this paper, the ideal efficiency is determined by the C/D loss only. The 4-b transmitters are simulated under the conditions of the same output power with the same load resistance. Fig. 12 shows the efficiency contours of the two transmitters (conventional, IQ Sharing), without applying the cell deactivation technique. The center code has the minimum power for both the proposed and conventional quadrature structures, where the output power from all cells is near zero. The conventional quadrature and IQ Sharing transmitters have the highest efficiency points located on the lines at 45°, 135°, 225°, and 315°, because each point on the diagonal edges have maximum power. The IQ Sharing transmitter has a better efficiency than the conventional one.

Fig. 13 shows the efficiency contours when the DOC technique is applied. The enhanced performance is clearly evident. The DOC technique significantly improves the efficiencies in low-power regions from 10% to 30% points due to the large number of deactivated cells. The efficiency improvements along the diagonal lines are significant for the IQ Sharing transmitter, because the transmitter operates exactly like the polar transmitter along the diagonal line after applying the DOC. Except the diagonal line, the two transmitters have slightly lower efficiencies than the polar transmitter. Nevertheless, the efficiency is improved by the DOC technique. Due to the efficiencies being different for all the I and Q points, the average efficiency can be obtained based on the modulation code distribution on the IQ plane. The dotted magenta circle on the IQ plane represents the average power region with the highest distribution for

16 QAM LTE data codes. Fig. 13 clearly shows that the proposed transmitter has higher efficiency on the magenta circle than the conventional one.

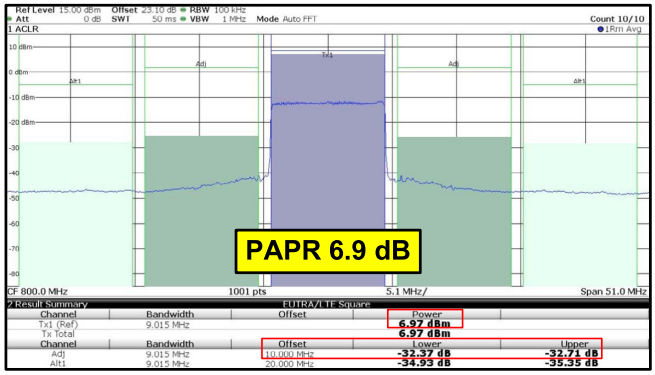
To clearly compare the IQ Sharing and conventional structures, the C/D losses along the three paths on the IQ plane are calculated with the same total number of cells under the DOC operation as shown in Fig. 14. The outputs and C/D losses of the IQ Sharing on path 1 (0°) and the conventional quadrature with path 3 (45°) are the same, because the cell turn-ON switching behaviors are identical in both the cases. The IQ Sharing structure has the highest efficiency along path 3 for 45°, 135°, 225°, and 315° lines, because all the cells have the same output waveform on these lines without having the out-of-phase cancellation. Similar to IQ Sharing, the conventional structure has the highest efficiency along the 0°, 90°, 180°, and 270° paths, because only the I or Q cells operate without I and Q cancellation. The IQ Sharing has a 3 dB-higher peak power than the conventional structure, and the conventional quadrature transmitter has a higher C/D loss at the high peak output powers. Consequently, the IQ Sharing transmitter has a considerably higher efficiency than the conventional quadrature transmitter.

V. Measurement Results

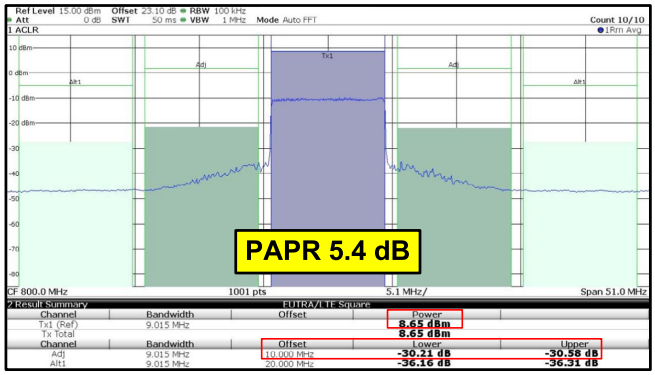
The proposed transmitter based on IQ Sharing with the DOC technique is implemented as shown in Fig. 15. The LO generator, for creating the IQ Sharing waveform, produces a four-phase differential signal with 25% duty cycle. The nonoverlapping four phase LO generator was designed using cross-coupled DFFs and additional nonoverlapping buffers to remove I–Q crosstalk [20]. The input signal is an LTE baseband digital signal upsampled from 61.44 to 100 MSPS with a 6-b resolution. The oversampling rate is limited by the data storage hardware specification, which is an FPGA board. The D flip-flops align the data to compensate for the code processing delay.

The proposed transmitter adopts a 6-b input. The higher 5 bits are decoded in a thermometer code, and the LSB is processed in binary. There are a total of 32 cells: 31 thermocode cells and one half size binary cell. Since the thermometer code provides good linearity and the binary code can reduce the number of cells, the transmitter is designed in a hybrid code composition in order to take advantage of both the code systems. The implemented transmitter has 15 pairs of the 30 thermocode cells for the DOC operation.

The proposed IQ Sharing transmitter is fabricated using a 28-nm CMOS RF process with eight-metal option. Fig. 16 is a die micrograph. The silicon die size is $660 \times 1660\ \mu\text{m}^2$ and the core area without the decaps and pad is $345 \times 690\ \mu\text{m}^2$. The 50-Ω load is transformed by the switched capacitor and LC circuits mounted on a PCB. The FPGA is the Vertex-4 ML402 evaluation board with a 100-MHz system clock. VDD of the power cell and logic is 1.1 V. All measured output powers include the matching loss, and the power-added efficiency (PAE) is calculated using the total power consumption at the switching stage, drive stage, all logics (DOC, Data alignment), and clock buffers.



(a)



(b)

Fig. 19. Measured output spectra with a modulated LTE signal (a) with 6.9-dB PAPR and (b) with 5.4-dB PAPR.

A. Static Measurement

The measurement is performed on 289 points formed by 17×17 points of the I and Q symbols at carrier frequency of 800 MHz. Fig. 17 shows the measured results of the efficiency and output power contours on the IQ plane. The power dynamic range is from −20.2 to 13.86 dBm, and the PAE at the peak power is 40.43%. At the peak output power, the second and third harmonics are measured as −37.5 and −43.2 dBm, respectively. The AM–AM and AM–PM distortions are shown in Fig. 18. A 2-MHz spacing two-tone signal at 800 MHz is used to measure the AM–AM and AM–PM characteristics, due to the memory limitations and saturated operation speed. The measurement results show a linear operation. The AM–AM distortion [13] in the switched capacitor structure is generated by the impedance variation of the switching cells, since the total source impedance is decided by the number of the on-cells. Moreover, nMOS and pMOS in the switch have different on-resistances. Consequently, the distortion occurs more severely at lower power than middle and higher output powers. The AM–PM distortions are generated by the time alignment mismatch between the transmitter input (FPGA) and signal analyzer, owing to synchronization mismatch between the external data storage and measurement setup.

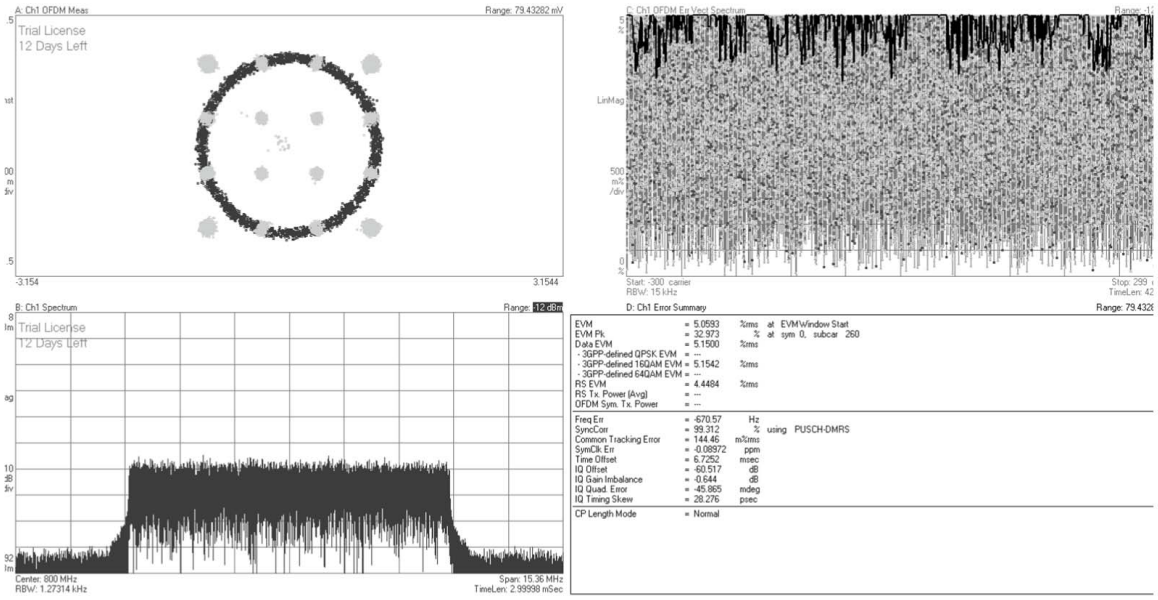
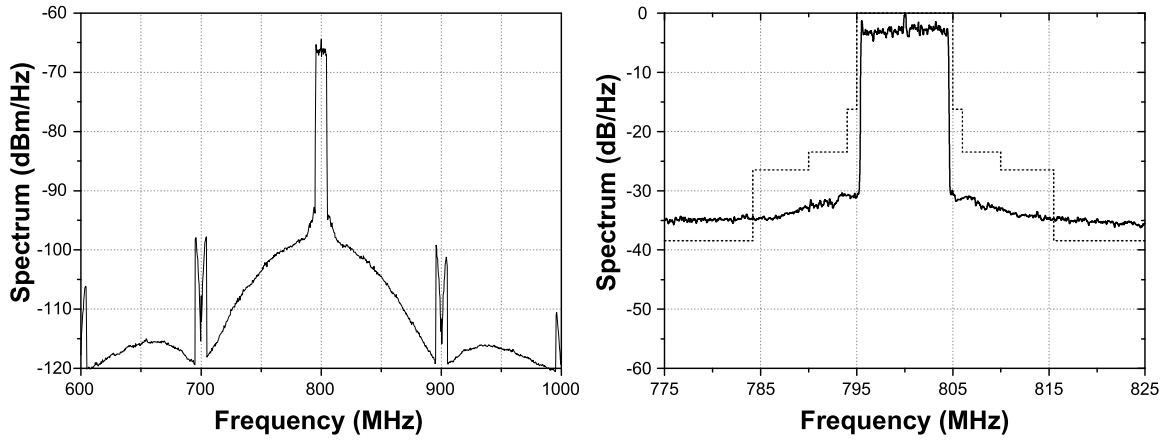


Fig. 20. EVM measurement results for LTE 16-QAM OFDM signal.



(a) (b)

Fig. 21. Measurement results (a) far-out and (b) close-in spectra for LTE 16-QAM

B. Dynamic Measurement

The implemented transmitter is measured using LTE signal with 16-QAM, 10-MHz bandwidth, 100 MSPS, and 6.9-dB PAPR. The PAE is 29.1% at an average output power of 6.97 dBm with the two-side ACLRs of −32.4 and −32.7 dBc, as shown in Fig. 19(a). With a simple crest factor reduction in the FPGA within the linear specification limit, the PAE is improved to 33.4% at an average output power 8.65 dBm with the ACLRs of −30.6 and −30.2 dBc, as shown in Fig. 19(b). The error vector magnitude (EVM) shown in Fig. 20 is measured using the LTE 16-QAM 10-MHz 8-ms 30.72 MSPS signal, where the predistortion technique is not applied. The measured EVM is 5%, but this value is higher than the real value due to the short time length (8 ms) of the input signal limited by the FPGA memory. Fig. 21 shows the far-out and close-in spectra of the transmitter. All the dynamic performances are measured at the average output power of 6.97 dBm, while spurs are repeated every 100 MHz as shown in Fig. 21(a). The close-in spectrum does not satisfy the 10-MHz LTE spectrum mask, as shown in Fig. 21(b). The measured transmitter may require an additional sharp filter to reduce the Rx band noise created by digital circuit. Moreover, a digital predistortion technique is also needed to improve the linearity [16], [17]. The symmetric layout and cell placement are helpful in reducing the ACLR by aligning the timing among the unit cells [12].

VI. Conclusion

An efficient and fully digital quadrature transmitter is developed. Due to the fully digitized architecture, the proposed transmitter has good programmability and can support a multimode operation. Unlike the polar architecture, there is no need for I/Q to polar conversion using a CORDIC, which produces a large bandwidth phase information signal, up to ten times larger than the original signal bandwidth. The conceptual three-level LO is employed in this paper.

TABLE I
COMPARISON OF THE DIGITAL-INTENSIVE TRANSMITTERS USING SWITCHED CAPACITOR

Reference	[9]	[12]	[14]	This work
Carrier frequency	2.2 GHz	2.2 GHz	800 MHz	800 MHz
Architecture	Polar (CORDIC power not included)	Polar (CORDIC power not included)	Quadrature	Quadrature
Supply voltage	1.2 V	1.5/3 V	1.25 V	1.1 V
Number of bit	9 bit	6 bit	8 bit	6 bit
Peak power	23.3 dBm	25.2 dBm	7.87 dBm	**13.9 dBm**
Peak PAE	38 %	45 %	10.8 %	**40.4 %**
Modulation signal	WLAN 802.11g 64-QAM	64-QAM OFDM WiFi	LTE 16-QAM 10 MHz 6.9 dB PAPR	LTE 16-QAM 10 MHz 6.9 dB PAPR
Average power	16.8 dBm	17.7 dBm	-0.11 dBm	6.97 dBm
Average PAE	21.8 %	27 %	6.3 %	29.1 %
E-UTRA ACLR	-	-	-30.5, -30.0 dBc	-32.4, -32.7 dBc
Die area	2.50×2.50 mm^2	1.43x0.73 mm^2	1.59x0.85 mm^2	1.66x0.66 mm^2
Matching network	On-chip	On-Chip	Off-chip	Off-chip
Technology	65 nm	90 nm	65 nm	28 nm

With this architecture, I and Q signals can be combined in the time domain and processed using the same power-generating cell with two-level possessing. Furthermore, by applying the DOC technique, the cells with the opposite phase are deactivated. Therefore, the efficiency of the IQ Sharing transmitter is increased by eliminating the power dissipation in the switch and driver operation of the DRFC cells. The DOC technique is particularly effective at low-power regions. The output of the DRFC cells is combined by the switched capacitor, which removes the output impedance dependence on the input signal, thereby providing good linearity. The C/D loss of the switched capacitor in the IQ Sharing structure has been analyzed on the IQ plane. Based on the loss analysis, the output power and efficiency of the proposed transmitter are evaluated. The proposed transmitter is implemented using a 28-nm CMOS process and evaluated. The transmitter with a switched capacitor is compared with the reported digital architecture shown in Table I. The polar transmitter [13] has a better performance compared with the proposed design. However, the proposed transmitter is based on quadrature processing with simple structure and low computing costs. Moreover, the polar transmitter does not include the CORDIC burden. The low power performance of the proposed transmitter can be enhanced by using a stacked structure with a high-drain-voltage device.

ACKNOWLEDGMENT

This research was supported by Samsung System LSI for chip fabrication. The authors would like to thank R. Schwarz for providing the spectrum analyzer used in this paper.

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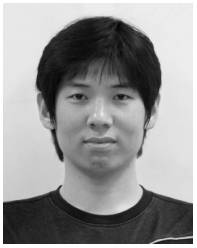

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