A 6.78-MHz Single-Stage Wireless Power Receiver Using a 3-Mode Reconfigurable Resonant Regulating Rectifier

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***Abstract*— A 6.78-MHz wireless power receiver using a 3-mode reconfigurable resonant regulating rectifier for resonant wireless power transfer is presented. The proposed receiver improves power conversion efficiency and reduces die area and off-chip components by achieving power conversion plus voltage regulation in one stage, using only four on-chip power transistors and one off-chip capacitor. Moreover, the proposed 3-mode operation reduces the output voltage ripples and accomplishes switching synchronization easily during mode switching. The proposed pulsewidth modulation controller using ramp-stacking technique and type-II compensation achieves tight voltage regulation in the full loading range with fast transient responses. An adaptive sizing method is also employed to further improve the light-load efficiency of the receiver. Fabricated in a standard 0.35-μm CMOS process using 5-V devices, the receiver regulates the output voltage at 5 V and delivers a maximum power of 6 W. The measured peak efficiency reaches 92.2% when delivering an output power of 3.5 W. For a load step between 0.5 and 5 W, the overshoot and undershoot are less than 300 mV and the settling times are less than 16 μs.**

***Index Terms*— Active rectifier, alliance for wireless power (A4WP), power conversion efficiency, reconfigurable resonant regulating (R^3) rectifier, resonant wireless power transfer (R-WPT), switching synchronization, 3-mode operation, type-II compensation, wireless charging.**

I. Introduction

PORTABLE electronic devices have perceived shorter battery cycle due to their ever-increasing functionalities. This creates a great demand for a more convenient and accessible way to charge batteries. To replace conventional wired charging, wireless charging is being developed into a standard feature for portable devices. Resonant wireless power transfer (R-WPT) using magnetic resonance emerges as a promising approach, as it provides spatial freedom and can charge multiple devices simultaneously [1]. Fig. 1 shows a typical power link of an R-WPT system that consists of a transmitter and a receiver. ISM band frequencies such as 6.78 or 13.56 MHz are commonly used as the resonance frequency of the *LC* tank. In the transmitter, the power amplifier drives the primary coil to generate magnetic fluxes that induce an AC voltage in the secondary coil. In the receiver, the coupled AC power is then rectified and regulated into a DC voltage to charge the battery. The power conversion efficiency of the receiver should be high to avoid heating up the device. It is also preferable to have a small die size and only a few off-chip components to reduce volume and cost. Many research efforts have been devoted to meet these challenges [2]–[9].

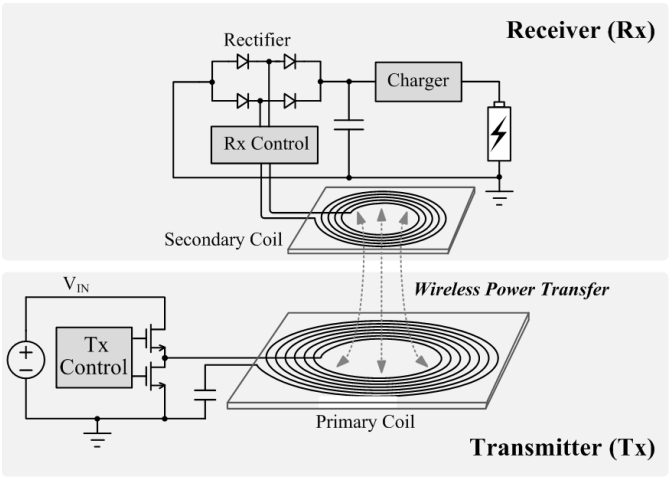

Fig. 1. Power link of an R-WPT system.

Conventional wireless power receivers adopt a two-stage topology. The first stage is a rectifier for AC–DC conversion, and the second stage is a low-dropout regulator (LDO) [2], [3] or a switching converter [4]–[7] for voltage regulation. Active rectifiers implemented by transistors and comparators with low forward voltage drops are commonly used to replace passive rectifiers to reduce the diode-drop loss, and various delay compensation schemes were proposed to compensate for the propagation delays for efficiency improvement [10]–[15]. For example, an adaptive ON/OFF delay-compensation technique that is insensitive to process, voltage and temperature (PVT) variations and mismatches was introduced in [15] recently. Rectifiers with reconfigurable output stages were also proposed to extend the range of power transmission [16]–[18]. However, in these cases, a voltage regulator such as an LDO is used as the second stage to produce a well-regulated output voltage, and this degrades the efficiency and increases the cost of the receiver. The efficiency of the LDO is limited by the ratio of the output voltage to the input voltage. For mobile charging applications of which the power level can be as high as several watts, the power loss of the LDO is significant and

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will cause heating problems. Efficiency improvement can be achieved by using a switching converter that can maintain high efficiency over a wide input and output range. However, a bulky inductor is needed and silicon cost is also significantly increased.

Efforts of implementing wireless power receivers with one-stage power conversion have been made in [8] and [9]. The resonant regulating rectifier (3R) proposed in [8] implements a passive rectifier followed by a step-down charge pump to produce a regulated output voltage. However, it needs five off-chip diodes and three off-chip capacitors; and the mode selection between heavy load and light load has to be done manually. The 1X/2X reconfigurable resonant regulating (R^3) rectifier proposed in [9] achieves one-stage power conversion plus voltage regulation using five on-chip power transistors and one off-chip capacitor. However, this 1X/2X R^3 rectifier regulates the output voltage based on the assumption that the induced AC voltage on the secondary coil in 2X mode is higher than that in 1X mode, which is only valid under a limited coupling and loading range [19]. Therefore, the target output power is in the mW range, and it is not suitable for high-power applications. The adaptive rectifier with a phase control mechanism [20] and the integrated 3R [21] are proposed to regulate the output voltage by modulating the conduction time of active diodes, and they also aim at low-power applications. On the other hand, voltage regulation can also be accomplished in the transmitter side [22], [23], but voltage accuracy and transient response of the receiver are compromised [8].

In this paper, we propose a new receiver topology that uses a 3-mode R^3 rectifier [24]. The proposed receiver realizes one-stage power conversion plus voltage regulation and complies with the specifications released by the alliance for wireless power (A4WP) [1]. It consists of only four on-chip power transistors and one off-chip capacitor, and can be implemented in a standard CMOS process using only 5-V transistors when the output voltage is regulated at 5 V. The proposed 3-mode operation reduces the output voltage ripples and accomplishes switching synchronization easily during mode switching. Moreover, a pulsewidth modulation (PWM) controller is proposed to regulate the output voltage in the full loading range and to achieve fast transient responses, and an adaptive sizing method is employed to further improve the light-load efficiency of the receiver.

The rest of this paper is organized as follows. In Section II, the characteristics of the series-resonant secondary tank are studied, and the concept of the proposed 3-mode R^3 rectifier is discussed. In Section III, the system architecture of the receiver and the implementation of the key circuit blocks are presented. Measurement results are provided in Section IV, and the research efforts are concluded in Section V.

II. 3-Mode Reconfigurable Resonant Regulating Rectifier

A. Characteristics of Series-Resonant Secondary Tank

For transmitting several watts using wireless power transfer, such as in mobile battery charging, the *LC* tank of the secondary coil is better to be series-tuned [15], [25], [26]. Fig. 2

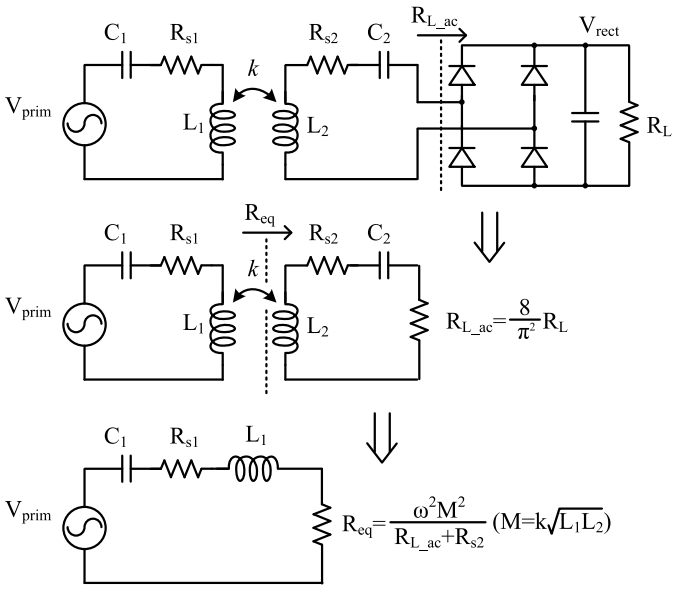


Fig. 2. Power link with a series-resonant secondary tank.

shows the circuit model of the power link with coupling coefficient k. The primary coil L_1 (with parasitic resistance R_{s1}) and the secondary coil L_2 (with parasitic resistance R_{s2}) are tuned by capacitors C_1 and C_2, respectively. Full-bridge rectifier is assumed for the following analysis. The input resistance of the rectifier R_{L_ac} and the reflected equivalent resistance of the secondary R_{eq} are given by [25], [26]

$$R_{L\_ac} = \frac{8}{\pi^2} R_L; \quad R_{eq} = \frac{\omega^2 M^2}{R_{L\_ac} + R_{s2}} \tag{1}$$

where ω ($=2\pi f_s$) is the resonance frequency of the *LC* tank in rad/s and f_s is chosen to be 6.78 MHz in this paper. M ($=k(L_1L_2)^{1/2}$) is the mutual inductance between the coils. The efficiencies of the primary stage and the secondary stage are, respectively, given by

$$\eta_{prim} = \frac{R_{eq}}{R_{eq} + R_{s1}}; \quad \eta_{sec} = \frac{R_{L\_ac}}{R_{L\_ac} + R_{s2}}. \tag{2}$$

The input power injected into the inductive link P_{in} and the output power P_{out} are, respectively, given by

$$P_{in} = \frac{V_{prim}^2}{2(R_{eq} + R_{s1})} \tag{3}$$

$$P_{out} = P_{in} \times \eta_{prim} \times \eta_{sec} \tag{4}$$

where V_{prim} is the magnitude of the AC source. Therefore, the rms current of the secondary tank I_{rms} and the output voltage of the rectifier V_{rect} are, respectively, computed as

$$I_{rms} = \sqrt{\frac{P_{out}}{R_{L\_ac}}} = \frac{\omega M}{\omega^2 M^2 + R_{s1}(R_{L\_ac} + R_{s2})} \frac{V_{prim}}{\sqrt{2}} \tag{5}$$

$$V_{rect} = \frac{2\sqrt{2}}{\pi} I_{rms} R_L. \tag{6}$$

Fig. 3 plots I_{rms} and V_{rect} versus R_L with different quality factors Q_1 of the primary coil (50, 100, and 200). It is noted that the series-resonant secondary tank behaves like

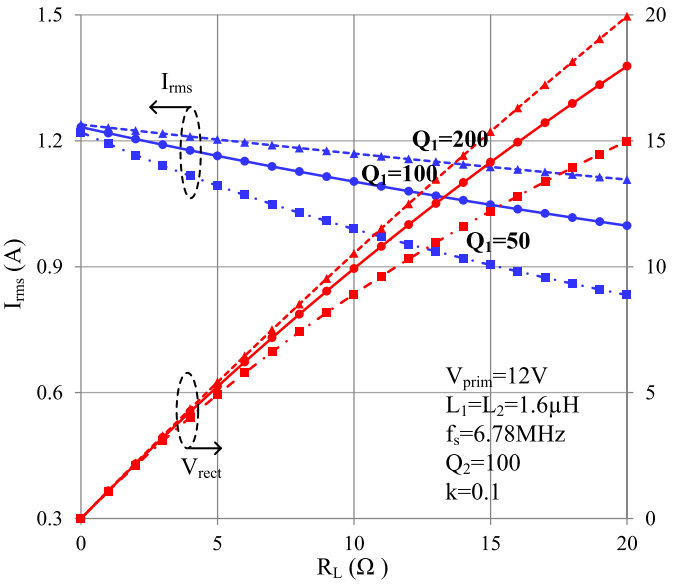


Fig. 3. I_{rms} and V_{rect} versus R_L with $Q1$ = 200/100/50.

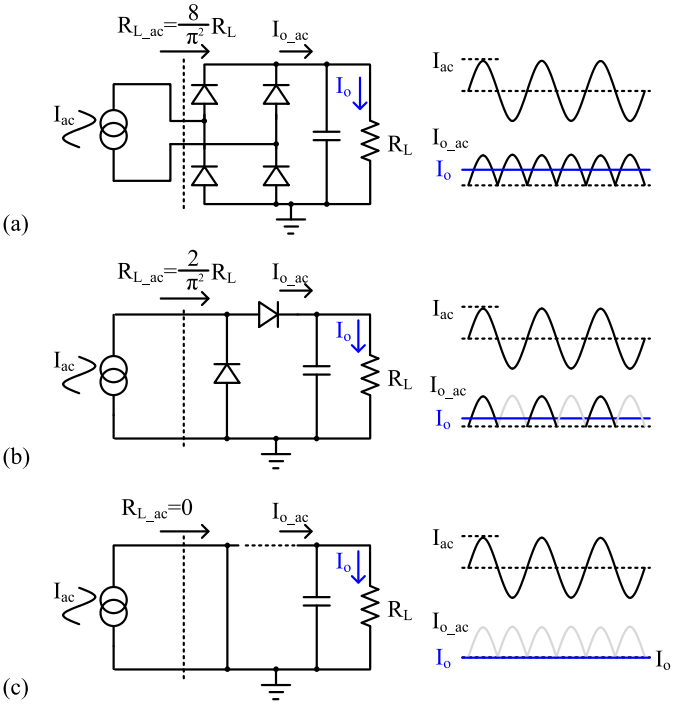


Fig. 4. (a) Full-bridge rectifier (1X mode). (b) Half-bridge rectifier (½X mode). (c) Freewheeling mode (0X mode).

a current source instead of a voltage source [26], [27]. We use this characteristic as the basis of our proposed reconfigurable rectifier design [24].

B. Concept of the 3-Mode R^3 Rectifier

As shown in Fig. 4, for a series-resonant secondary tank, either a full-bridge or a half-bridge rectifier can be used to convert AC power into DC power. Moreover, the secondary tank can also be shorted to work in the freewheeling mode. If the secondary tank is considered to be an AC current source,

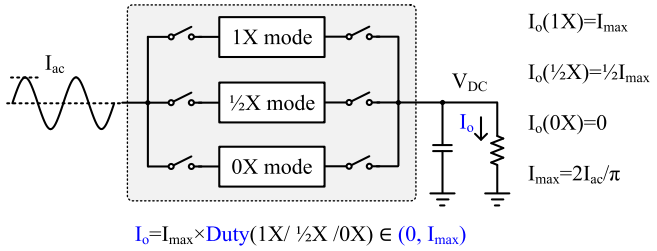


Fig. 5. Concept of the proposed receiver.

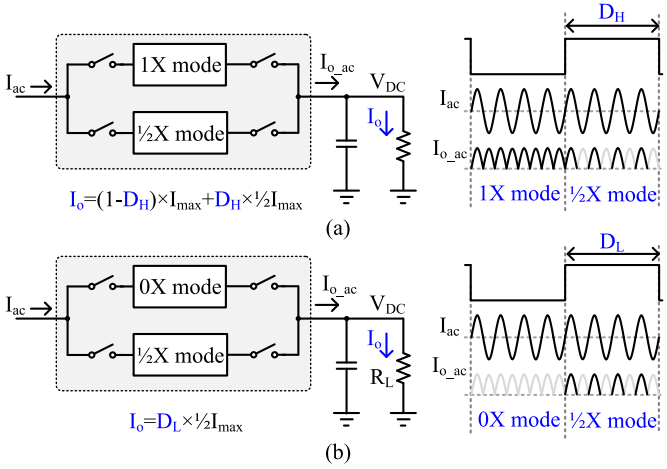
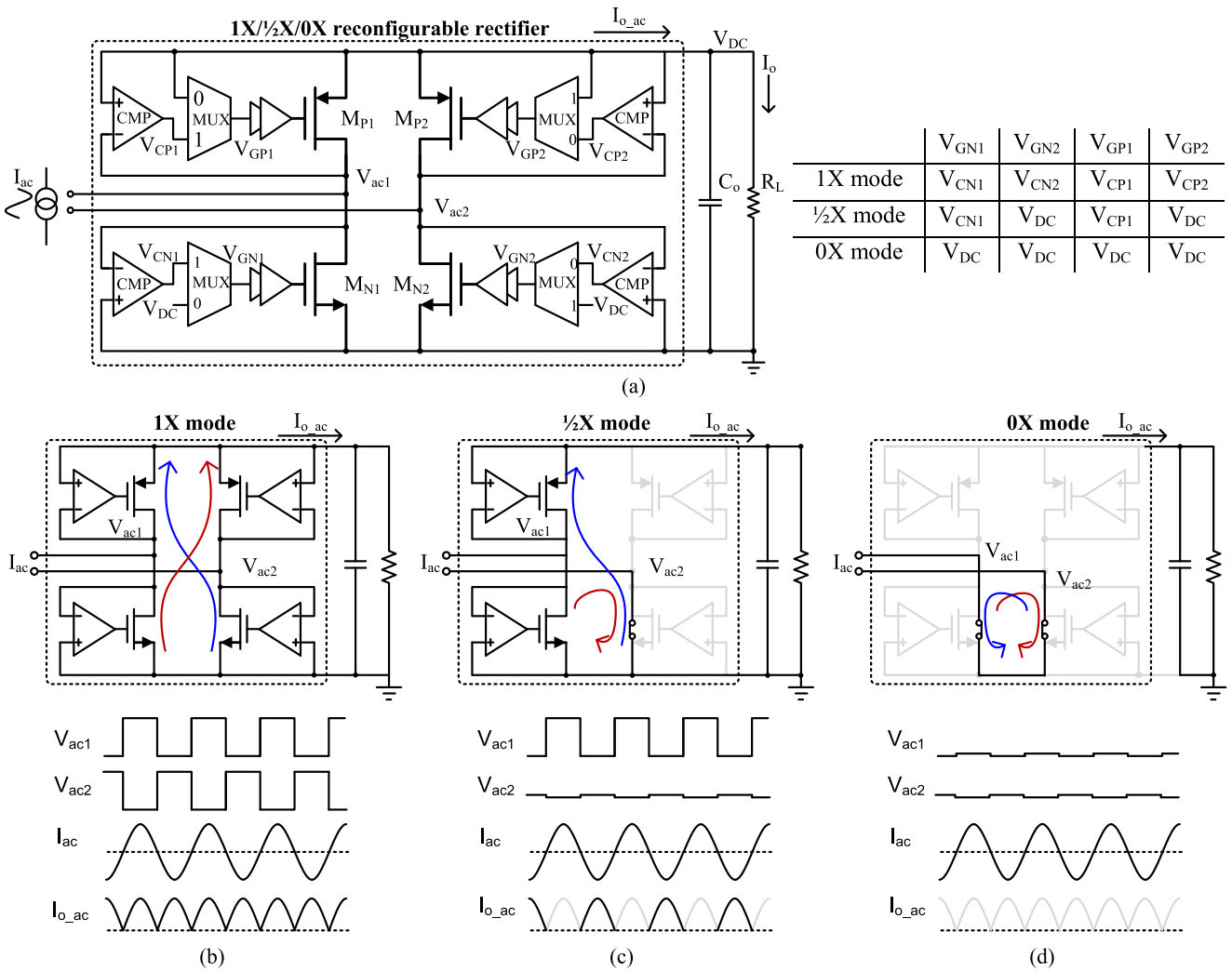


Fig. 6. Proposed 3-mode operation. (a) Heavy load. (b) Light load.

then obviously the output current of the full-bridge rectifier is twice of that of the half-bridge rectifier, and it is 0 in the freewheeling mode. We label the three modes as 1X mode, ½X mode, and 0X mode. Let the amplitude of the AC current be I_{ac}, then the 1X mode, ½X mode, and 0X mode will have different output currents I_{max}, ½I_{max}, and 0, respectively, where

$$I_{max} = \frac{2}{\pi} I_{ac}. \tag{7}$$

Fig. 5 shows the concept of the proposed receiver. If a reconfigurable rectifier is designed to switch periodically among the three modes, it can deliver any intermediate load current I_o between 0 and I_{max} depending on the duty ratio of each mode. It means that it is possible to regulate the output voltage through a PWM mechanism that modulates the input current. Therefore, we propose a new receiver topology, the 3-mode R^3 rectifier, in this paper. It consists of a 1X/½X/0X reconfigurable rectifier and a controller. As shown in Fig. 6, the R^3 rectifier is switched periodically between 1X mode and ½X mode in heavy load (when ½I_{max} < I_o < I_{max}); and between ½X mode and 0X mode in light load (when 0 < I_o < ½I_{max}), respectively. Fig. 7 shows the implementation of the 1X/½X/0X reconfigurable rectifier using active diodes. It consists of four on-chip power transistors ($M_{N1,2}$ and $M_{P1,2}$) and one off-chip capacitor (C_o) only. By controlling the gate-drive signals of the power transistors $M_{N1,2}$ and $M_{P1,2}$, the reconfigurable rectifier can be configured into 1X mode, ½X mode, and 0X mode, respectively.



	V_{GN1}	V_{GN2}	V_{GP1}	V_{GP2}
1X mode	V_{CN1}	V_{CN2}	V_{CP1}	V_{CP2}
½X mode	V_{CN1}	V_{DC}	V_{CP1}	V_{DC}
0X mode	V_{DC}	V_{DC}	V_{DC}	V_{DC}

Fig. 7. (a) 1X/½X/0X reconfigurable rectifier. (b) 1X mode. (c) ½X mode. (d) 0X mode.

The implementation of the controller will be discussed in the next section.

In principle, power regulation can be done by switching between 1X mode and 0X mode only. However, the proposed 3-mode operation results in more even distribution of power with reduced output voltage ripples by switching among 1X mode, ½X mode, and 0X mode. Fig. 8 shows the waveforms of the output voltage V_{DC} at different values of I_o with the two methods. The effect of ripple reduction of the 3-mode operation can best be illustrated by the case with $I_o = ½I_{max}$. If the R^3 rectifier only switches between 1X mode and 0X mode (labeled as 1X–0X operation), the output capacitor will be continuously charged for several resonant cycles and then discharged for the next several resonant cycles, resulting in large output ripple voltage ΔV_{DC}. With the 3-mode operation, the rectifier can work in a pure ½X mode instead of switching between 1X mode and 0X mode, and thus ΔV_{DC} is minimized. For the 1X–0X operation, ΔV_{DC} reaches the maximum value when $I_o = ½I_{max}$, and it increases with I_o when $0 < I_o < ½I_{max}$ and decreases with $I_o$when $½I_{max} < I_o < I_{max}$. For the 3-mode operation, ΔV_{DC} increases with I_o when $0 < I_o < ¼I_{max}$ and $½I_{max} < I_o < ¾I_{max}$, and decreases with I_o when $¼I_{max} < I_o < ½I_{max}$ and $¾I_{max} < I_o < I_{max}$, which is similar to the relationship between the output voltage ripple and the duty cycle of a three-level buck converter [28]. To make a comparison between the two methods, closed-loop transistor-level simulations were performed with two different PWM modulation periods T_{pwm} (1.2 and 1.8 μs) for different values of I_o. Normalized output voltage ripples of the two methods are plotted in Fig. 9, and ripple reduction using the 3-mode operation is obvious, especially when a larger T_{pwm} is used. In addition, the 3-mode operation also facilitates the receiver to achieve switching synchronization, as will be explained in Section III-B.

In a switching converter, increasing the switching frequency (f_{sw}) can reduce the size of the inductor and the output capacitor and thus can improve transient responses, but it also increases the switching loss and degrades the efficiency. f_{sw} should be properly selected to achieve a reasonable tradeoff between efficiency and transient responses [29]. While in the proposed receiver, the power transistors always switch

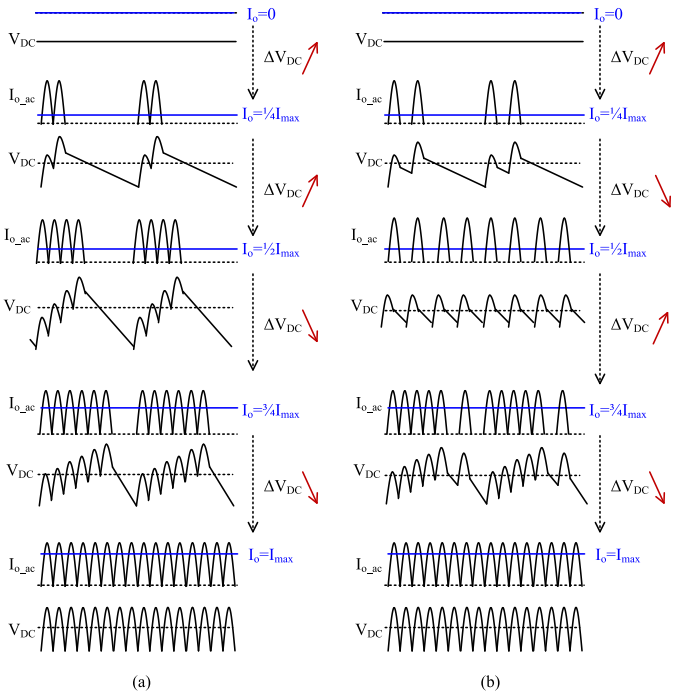


Fig. 8. Waveforms of V_{DC} at different values of I_o with (a) 1X–0X operation and (b) 3-mode operation.

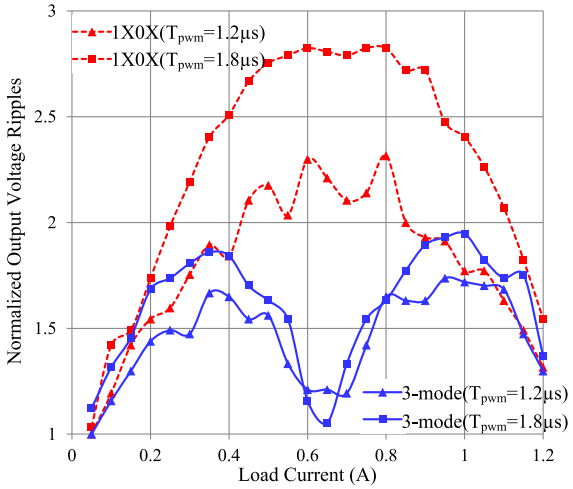


Fig. 9. Comparison of the normalized output voltage ripples between 1X–0X operation and 3-mode operation.

at the resonance frequency of the *LC* tank and their switching loss is not affected by the duration of T_{PWM}. As a result, intuitively, T_{PWM} should be as short as possible to reduce ΔV_{DC} and to improve transient responses. However, as one PWM modulation period has to be a multiple of the resonant cycles, the duty cycle of the PWM modulation can only be selected from discrete values. For example, if T_{pwm} is 1.2 μs that has eight resonant cycles, then the duty cycle can only be 0, 1/8, 2/8, . . . , 7/8, 1. The feedback loop will adjust the duty cycle period by period to achieve an averaged duty cycle needed at the price of increased ΔV_{DC}. Therefore, ΔV_{DC} consists of two parts: the ripple due to the PWM modulation and the fluctuation due to the limited resolution of

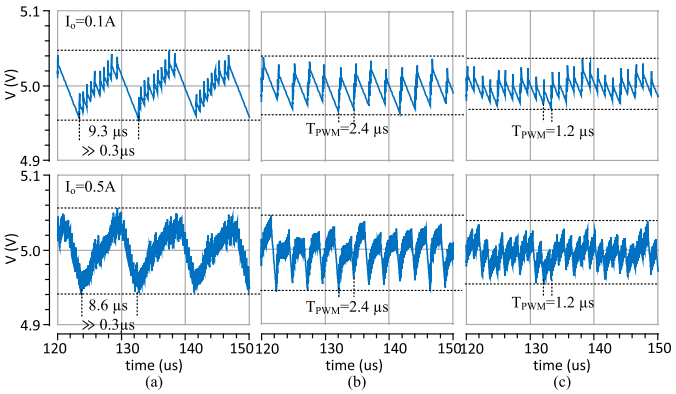


Fig. 10. Simulated waveforms of V_{DC} with different values of T_{PWM}. (a) $T_{PWM} = 0.3$ μs. (b) $T_{PWM} = 2.4$ μs. (c) $T_{PWM} = 1.2$ μs.

the duty cycle, which are both related to the duration of T_{PWM}. As shown in Fig. 10, if T_{PWM} is too short (e.g., 0.3 μs), the resolution of the duty cycle is too low and the receiver has to oscillate at a much longer period to regulate V_{DC} with a larger ΔV_{DC}. If T_{PWM} is too long (e.g., 2.4 μs), although the resolution of the duty cycle is increased, ΔV_{DC} is also increased. As a result, $T_{PWM} = 1.2$ μs is a good tradeoff for minimizing ΔV_{DC} and is thus selected as the modulation period of this paper.

Note that the three modes of the R^3 rectifier have different input resistances, as indicated in Fig. 4. With reference to Fig. 2, although R_L becomes larger in light load, the proposed R^3 rectifier will switch between ½X mode and 0X mode, and R_{L_ac} actually becomes smaller when compared to that in heavy load. Therefore, the power received at the secondary side is automatically reduced. At the same time, according to (1), R_{eq} is increased. Therefore, the loss on R_{s1} is reduced and the efficiency is improved. Moreover, the nodes $V_{ac1,2}$ are clamped to V_{DC} when $M_{P1,2}$ are ON and are around 0 V when $M_{N1,2}$ are ON. Therefore, the voltages of $V_{ac1,2}$ are well controlled in the proposed topology, and the voltage stress problem is thus relieved. For the other two-stage topologies, $V_{ac1,2}$ are not clamped between 0 V and V_{DC} and hence over-voltage protection circuits are needed [3], [5], [7], and high-voltage transistors that occupy large silicon area have to be used [7]. In addition, the secondary tank should be detuned in light load to reduce the received power to protect the receiver [3], [5], [7], and thus the system efficiency is degraded.

III. Implementation of 3-Mode R^3 Rectifier

Fig. 11 shows the block diagram of the proposed wireless power receiver using the 3-mode R^3 rectifier. It consists of a 1X/½X/0X reconfigurable rectifier as the power stage and a controller. The controller determines the loading conditions and switches among the operation modes of the reconfigurable rectifier for regulation. The receiver is implemented with an on-chip bandgap voltage reference.

A. PWM Controller

The schematic and the working principle of the proposed PWM controller are shown in Figs. 12 and 13, respectively. The PWM modulation frequency is chosen to be

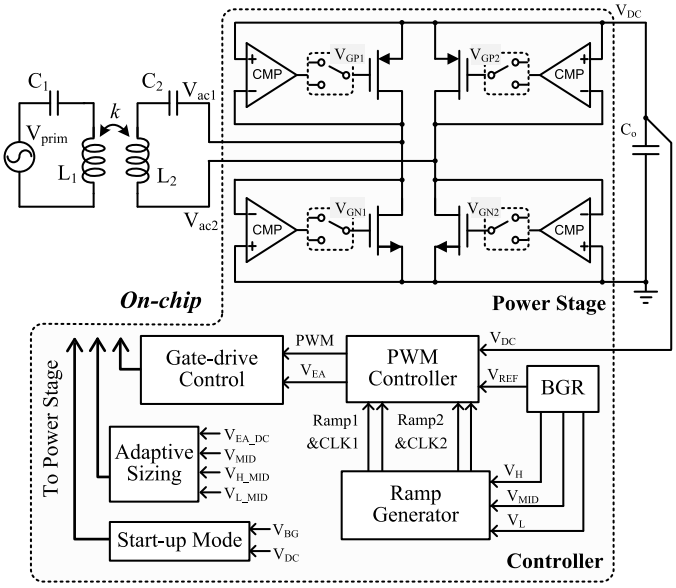


Fig. 11. Block diagram of the wireless power receiver with the 3-mode R^3 rectifier.

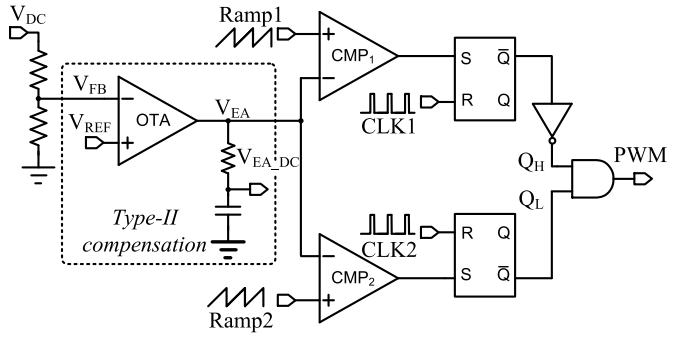


Fig. 12. Schematic of the PWM controller.

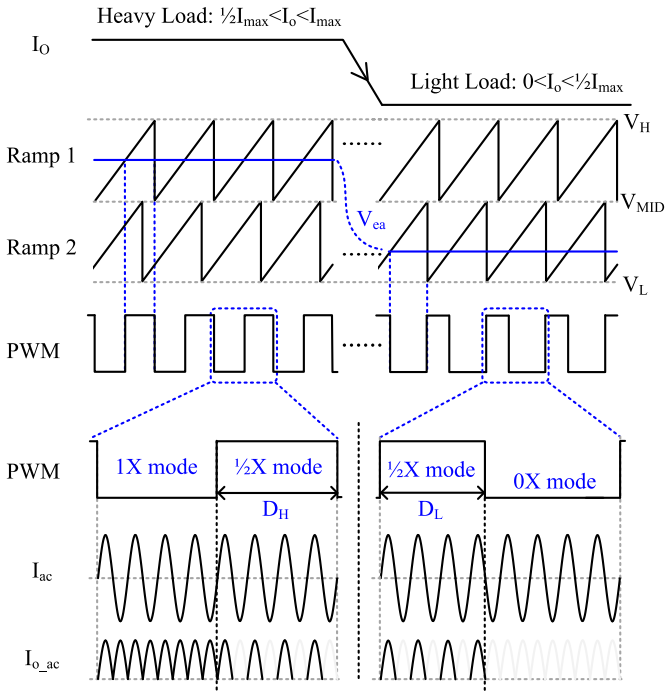


Fig. 13. Working principle of the PWM controller.

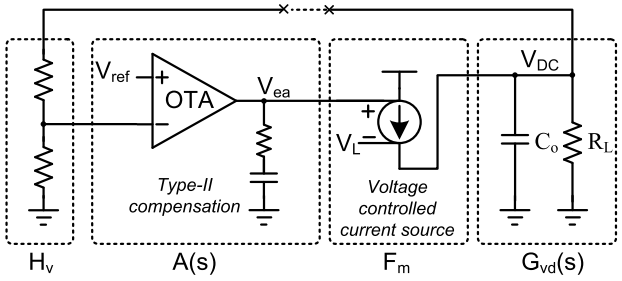


Fig. 14. Simplified small-signal model.

around 800 kHz ($T_{\text{pwm}} \approx 1.2\ \mu$s), which is about 1/8 of the resonance frequency. The PWM controller senses the output voltage V_{DC} and compares it with the reference voltage V_{REF}. Type-II compensation is adopted to stabilize the system and to achieve fast transient responses, as will be explained later. To implement the 3-mode operation with automatic transition between heavy load and light load, the output of the compensator V_{EA} is compared with two stacked ramp signals: Ramp 1 and Ramp 2. They have the same amplitude and frequency, but Ramp 2 ramps between V_L and V_{MID} and Ramp 1 ramps between V_{MID} and V_H. Accuracy in magnitude is guaranteed by using the delay-compensated ramp generator proposed in [29]. Note that the two ramp signals do not have to be synchronized. The working principle of the PWM controller is summarized as follows.

1) *Heavy Load ($\frac{1}{2}I_{max} < I_o < I_{max}$):* The feedback loop will drive V_{EA} into the range of Ramp 1, so Q_L keeps at "1" and the PWM signal is determined by Q_H. The R^3 rectifier switches between 1X mode and ½X mode. The duty cycle of ½X mode D_H is determined by comparing V_{EA} with Ramp 1, and a lower V_{EA} results in a larger D_H.
2) *Light Load ($0 < I_o < \frac{1}{2}I_{max}$):* The feedback loop will drive V_{EA} into the range of Ramp 2, so Q_H keeps at "1" and PWM signal is determined by Q_L. The R^3 rectifier switches between 0X mode and ½X mode. The duty cycle of ½X mode D_L is determined by comparing V_{EA} with Ramp 2, and a higher V_{EA} results in a larger D_L.
3) *Intermediate Load ($I_o = \frac{1}{2}I_{max}$) and $V_{EA} = V_{MID}$:* Depending on the mode the rectifier is working in (heavy load or light load), either D_H or D_L is equal to 1. Hence, smooth transition between heavy load and light load can be achieved. It is interesting to note that the duty cycle of a conventional switching converter working in continuous conduction mode is almost independent of the loading current; however, it is approximately proportional to the loading current in the proposed R^3 rectifier.

To determine the compensation network for the feedback loop, a simple but effective small-signal model is proposed, as shown in Fig. 14. By considering the series-resonant secondary

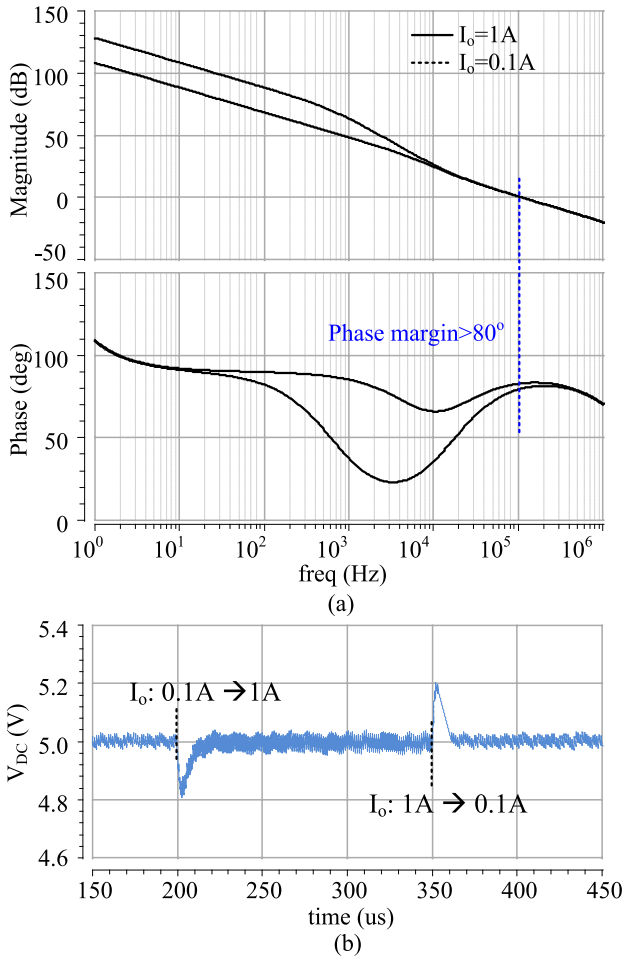


Fig. 15. (a) Bode plots of the loop transfer function of the system. (b) Simulated load transient responses.

as an AC current source, the power stage of the R^3 rectifier can be simplified as a first-order system with a pole p_d located at $-1/C_oR_L$. The loop-gain function is then given by

$$T_{\text{loop}}(s) = H_v A(s) F_m G_{vd}(s) \tag{8}$$

where H_v is the feedback ratio to set the desired output voltage and $A(s)$ is the transfer function of the compensator. Similar to a switching converter, F_m is the gain of the modulator [30], and is given by

$$F_m = \frac{1}{V_H - V_L}. \tag{9}$$

$G_{vd}(s)$ is the transfer function of the duty-cycle to the output voltage, and is given by

$$G_{vd}(s) = I_{\max} R_L \frac{1}{1 + \frac{s}{p_d}}. \tag{10}$$

This simple model serves well as a design guideline for loop compensation. Fig. 15(a) shows the Bode plots of (8) at different load currents (1 and 0.1 A) when the loop is well compensated, and the phase margins are good. The simulated transistor-level load transient responses shown in Fig. 15(b) verify that the receiver has good stability with small overshoot and undershoot. The loop bandwidth indicated in Fig. 15(a) is around 100 kHz, which is about 1/8 of the modulation frequency. This is similar to a switching converter that usually has a loop bandwidth of 1/10–1/5 of the switching frequency. Note that even if $I_{\max}$ is changed by ±20 dB due to the variation of the coupling coefficient, the receiver can still maintain a good stability with a phase margin of 50°. Moreover, there will be a communication channel between the transmitter and the receiver in a complete system, and $I_{\max}$ can be adjusted by the transmitter based on the coupling condition for more robust operation [1].

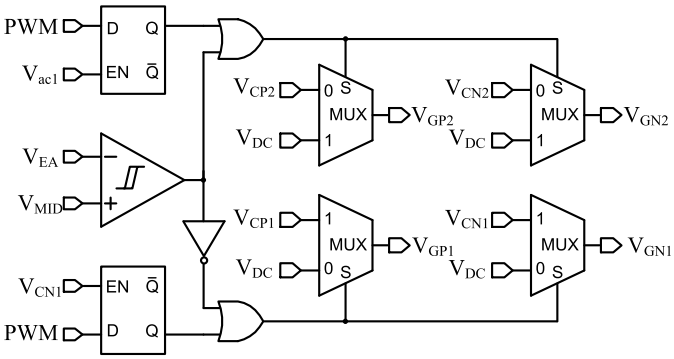


Fig. 16. Gate-drive control and switching synchronization circuits.

B. Gate-Drive and Switching Synchronization Circuits

Mode switching should be synchronized with the zero-crossing instants of I_{ac} to avoid switching noise and efficiency degradation, and it is done by off-chip tuning the delay cell in [8]. In the proposed 3-mode R^3 rectifier, switching synchronization can be easily accomplished. As shown in Fig. 7, it is noted that ½X mode shares the same half-cycle operation with both 1X mode (when V_{ac1} is "1") and 0X mode (when the output of the comparator V_{CN1} is "1"). If mode switching is only allowed to occur during the same half-cycle shared by both modes, switching synchronization is achieved automatically. This is done by adding only two D flip-flops into the gate-drive control circuit shown in Fig. 16. When driving heavy load, the R^3 rectifier switches between 1X mode and ½X mode, M_{N1} (M_{P1}) always works as an active diode, and its gate signal V_{GN1} (V_{GP1}) should always come from the output of the comparator V_{CN1} (V_{CP1}) and no change is needed during mode switching. When driving light load, V_{GN1} (V_{GP1}) should change between V_{CN1} (V_{CP1}) for ½X mode and V_{DC} (V_{DC}) for 0X mode, and it can only be changed when V_{CN1} is "1." Similarly, for M_{N2} (M_{P2}), the gate signal V_{GN2} (V_{GP2}) can only change between the output of the comparator V_{CN2} (V_{CP2}) for 1X mode and V_{DC} (V_{DC}) for ½X mode when V_{ac1} is "1" in heavy load, and is always connected to V_{DC} (V_{DC}) in light load. A hysteresis comparator compares V_{EA} and V_{MID} and determines the condition of the load. The gate signals of the power transistors in different modes are listed in Fig. 7.

C. Efficiency Analysis and Adaptive Sizing Method

Similar to a switching converter, the power loss of the power stage is a combination of conduction loss and switching loss of

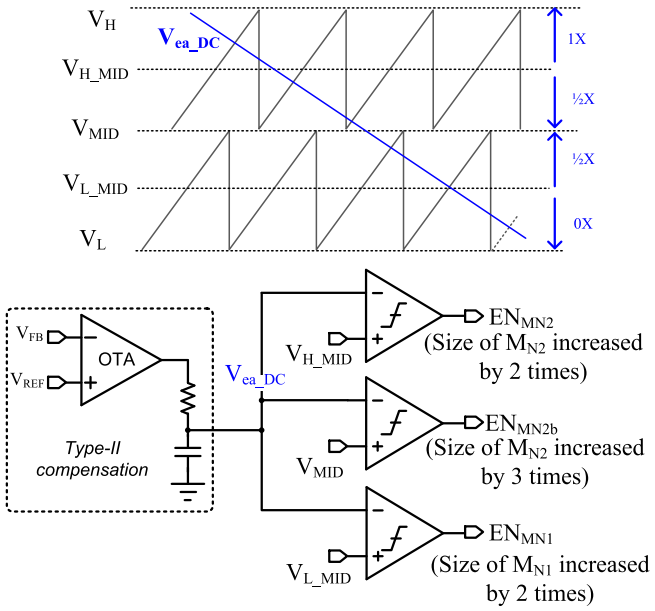


Fig. 17. Adaptive sizing method.

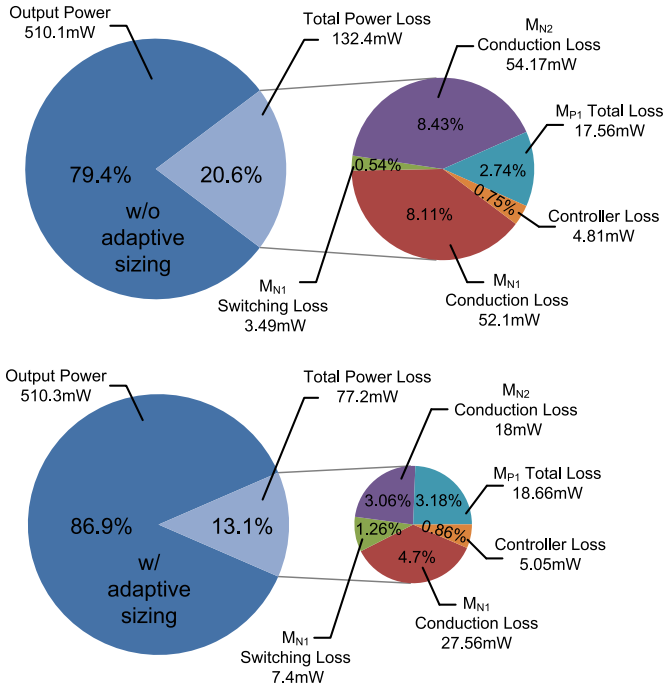


Fig. 18. Power distribution of the receiver with and without the adaptive sizing method when the output power is 0.5 W.

the power transistors. With reference to Fig. 7, the two pMOS power transistors M_{P1} and M_{P2} either work as active diodes or are always OFF. When working as diodes, M_{P1} and M_{P2} suffer from conduction loss and switching loss. When they are in the OFF state, there is no loss. Therefore, their sizes can be optimized by trading off between conduction loss and switching loss to minimize the total power loss. For the two nMOS power transistors M_{N1} and M_{N2}, they either work as active diodes or are always ON. When working as diodes, M_{N1} and M_{N2} suffer from conduction loss and switching loss. However, when they are in the ON state, there is conduction

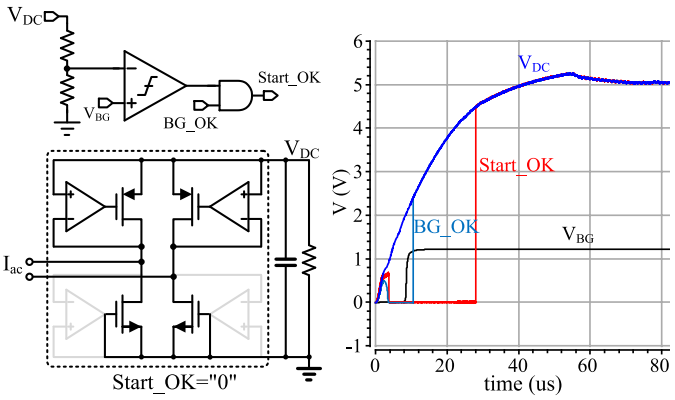


Fig. 19. Startup mode and the simulated startup waveforms.

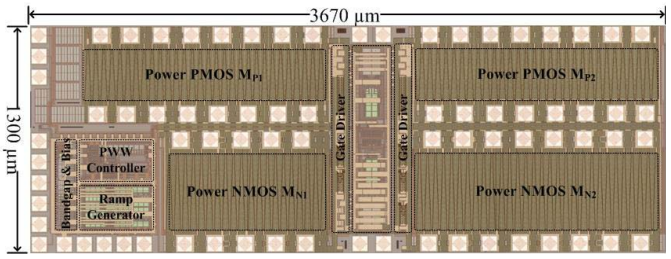


Fig. 20. Chip micrograph of the proposed R^3 rectifier.

loss only. It means that the conduction loss of M_{N1} and M_{N2} are more significant in ½X mode and 0X mode. Therefore, the sizes of M_{N1} and M_{N2} should be increased to reduce the conduction loss.

Based on the above analysis, an adaptive sizing method is proposed to further improve the light-load efficiency of the receiver. In the proposed PWM controller, the voltage level of V_{EA} indicates the mode status of the R^3 rectifier. For example, when $V_{MID} < V_{EA} < V_{H\_MID}$, the R^3 rectifier works longer in ½X mode than in 1X mode, so the size of M_{N2} should be increased to reduce the conduction loss. Fig. 17 shows the implementation of the proposed adaptive sizing method. V_{EA_DC} is actually used instead of V_{EA}, as it has the same DC value as V_{EA} but with much smaller ripples in the steady state and more stable transitions during transients. The sizes of M_{N1} and M_{N2} are first optimized assuming that they are working as diodes, and the sizes will be changed based on the mode status of the R^3 rectifier.

Fig. 18 shows the pie charts of the simulated power distribution of the receiver with and without the adaptive sizing method when the output power is 0.5 W. As the R^3 rectifier switches between ½X mode and 0X mode, M_{P2} has no loss and M_{N2} has only conduction loss. By employing the adaptive sizing method, the total loss is much reduced by reducing the conduction loss of M_{N1} and M_{N2}, and thus the efficiency is improved. It is interesting to note that, to improve the light-load efficiency, the sizes of power transistors are usually decreased to reduce the switching loss in a switching converter [31], while they are increased to reduce the conduction loss in the proposed 3-mode R^3 rectifier.

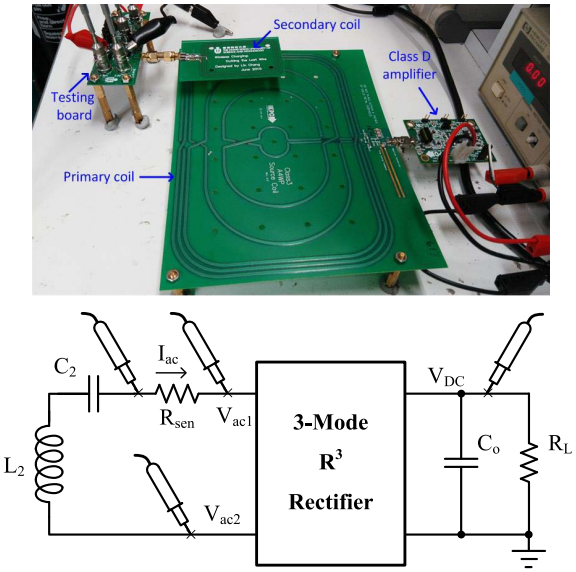


Fig. 21. Testing setup.

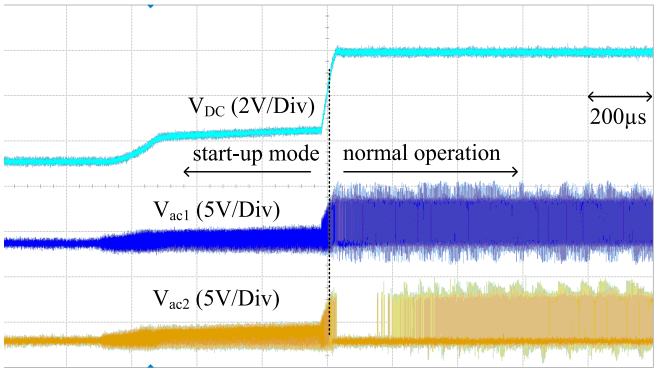


Fig. 22. Measured startup waveforms.

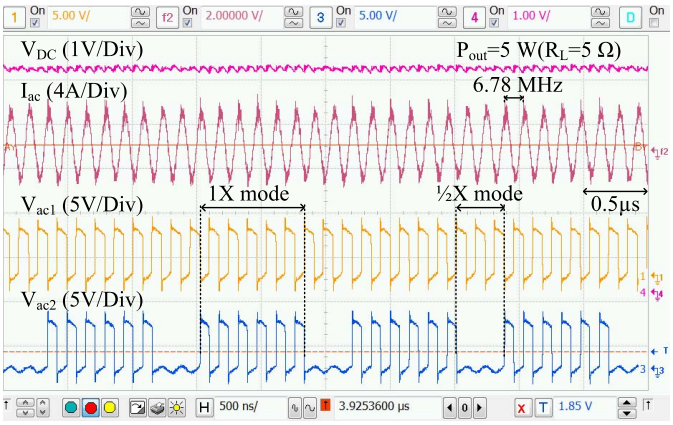
D. Startup Mode

In a wireless power receiver, the output voltage is also the power supply of the control circuit. Initially, the output voltage of the R^3 rectifier V_{DC} may start from 0 V, while the control circuit cannot function properly until V_{DC} reaches a certain level. It is possible that the R^3 rectifier gets stuck in 0X mode and the feedback loop fails. Therefore, a startup mode is needed and the design is shown in Fig. 19. During startup, Start_OK is "0," and the R^3 rectifier is forced to work as a full-bridge rectifier. The gates of M_{N1} and M_{N2} are connected to ground, and the transistors become passive diodes. When the bandgap reference ready signal BG_OK is "1" and V_{DC} is higher than 4.5 V, the startup mode ends and Start_OK becomes "1." The R^3 rectifier then enters into the normal operation mode. Fig. 19 also shows the simulated startup waveforms.

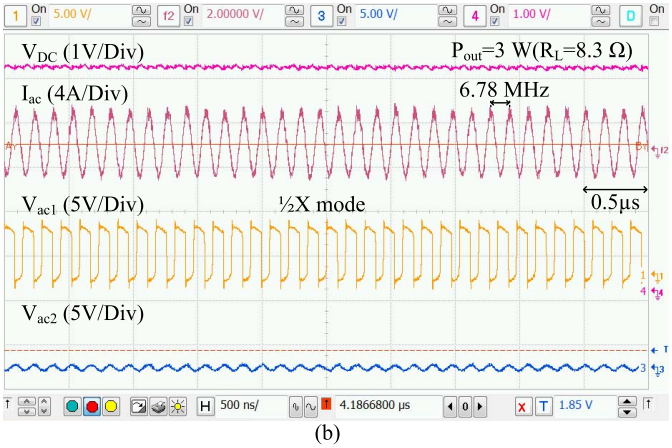
IV. Measurement Results

The proposed 3-mode R^3 rectifier was fabricated in a standard 0.35-μm CMOS process using 5-V devices. Fig. 20 shows the chip micrograph that measures 3670 μm $\times$ 1300 μm including the pads. A capacitor of 4.7 μF is used to filter the AC current, which is the only off-chip component needed for the receiver. Fig. 21 shows the testing setup. The transmitter and the primary coil are from a commercial demonstration kit which complies with the A4WP standard. A high-precision resistor is inserted into the input path to measure the input AC current. Initially, the power supply of the class-D amplifier is adjusted to the voltage level that the receiver delivers a maximum output power of 6 W with a maximum current of 1.2 A, and then it is fixed in the subsequent testing.

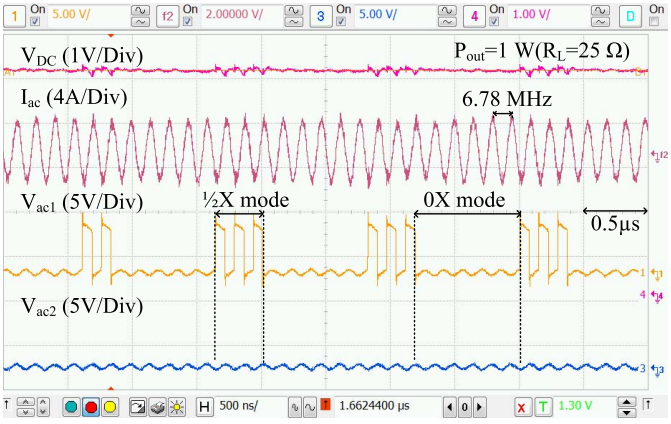
Fig. 22 shows the measured startup waveforms. The receiver achieves a smooth transition from the startup mode to the normal operation mode with a negligible overshoot at the output. Fig. 23 shows the measured AC input and DC output



(a)



(b)



(c)

Fig. 23. Measured steady-state waveforms when (a) $P_{out} = 5$ W, (b) $P_{out} = 3$ W, and (c) $P_{out} = 1$ W.

TABLE I
COMPARISON TO STATE-OF-THE-ART WIRELESS POWER RECEIVERS

	A-SSCC [4]	JSSC [8]	JSSC [3]	ISSCC [5]	TPE [7]	**This work**
Year	2012	2013	2015	2015	2016	**2016**
Technology	BCD 0.35 μm	BCD 0.35 μm	CMOS 0.35 μm	BCD 0.13 μm	BCD 0.18 μm	**CMOS 0.35 μm**
Receiver Structure	Rectifier +Buck	3R Rectifier	Rectifier +LDO	Rectifier +Buck	Rectifier +Buck	**3-Mode R^3 Rectifier**
Resonant Frequency	6.78 MHz	6.78 MHz	2 MHz	6.78 MHz	6.78 MHz	**6.78 MHz**
Output Voltage	5 V	5 V	3 V	5 V	5 V	**5 V**
Maximum Output Power	3 W	6 W	1.45 W	6 W	6 W	**6 W**
Peak Receiver Efficiency	68%	86%	75% (Rectifier only)	84.6%	80.86%	**92.2%**
Chip Area	18.3 mm^2	5.52 mm^2	4.8 mm^2	14.44 mm^2	12.25 mm^2	**4.77 mm^2**
Off-chip Components	1 inductor, 2 capacitors	5 diodes, 3 capacitors	3 capacitors	1 inductor, 2 capacitors	1 inductor, 2 capacitors	**1 capacitor**
Transient Responses	NA	>500μs (0.35W↔3.5W)	NA	NA	NA	**16μs (0.5W↔5W)**

Fig. 24. Measured load transient responses waveforms.

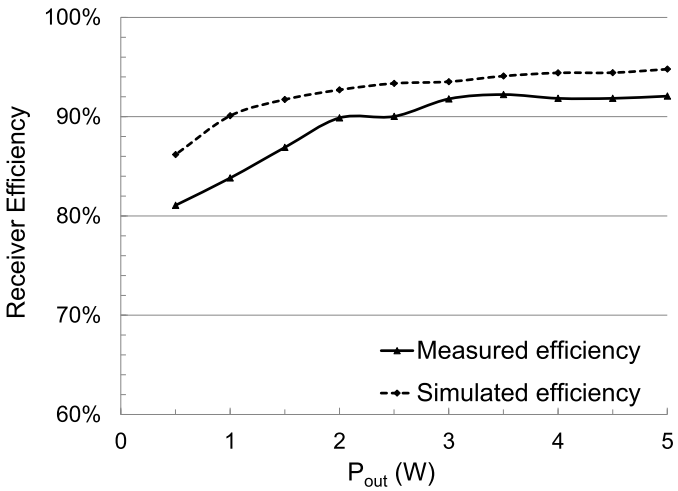


Fig. 25. Measured and simulated efficiency of the receiver.

waveforms when P_{out} is 5 W ($I_o = 1$ A), 3 W ($I_o = 0.6$ A), and 1 W ($I_o = 0.2$ A), respectively. Measurement results verify that the input current is approximately an AC current source and mode-switching is synchronized as designed. With reference to Fig. 7, the operation modes of the R^3 rectifier can be identified from the waveforms of $V_{\text{ac1,2}}$. It switches between 1X mode and ½X mode when $P_{\text{out}} = 5$ W; and between ½X mode and 0X mode when $P_{\text{out}} = 1$ W, as designed. The rectifier almost always stays in ½X mode when $P_{\text{out}} = 3$ W.

Fig. 24 shows the measured load transient responses. The proposed R^3 rectifier achieves a smooth and automatic transition between heavy load and light load with a tight regulation. When P_{out} changed between 0.5 and 5 W, the measured overshoot and undershoot were around 250 and 300 mV only, with a fast recovery time of 16 and 12 μs, respectively. The measured waveforms match with the simulation results shown in Fig. 15, which also verify the effectiveness of the proposed small-signal model.

Fig. 25 shows the measured power conversion efficiency of the receiver. The receiver efficiency is defined as the ratio of the output DC power to the input AC power, and the loss of the secondary coil is not included. Due to the irregular input waveforms and the switching noise, it is challenging to measure the efficiency accurately and hence the simulated efficiency is also included for reference. It is noted that by using the one-stage topology, the peak efficiency reaches 92.2% when $P_{\text{out}} = 3.5$ W. Moreover, the efficiency is higher than 81% when $P_{\text{out}} > 0.5$ W by employing the adaptive sizing method. The

discrepancy between the measured and simulated efficiency is mainly due to the loss on the metal routing and bondwires.

Table I summarizes and compares the performance of the proposed 3-mode R^3 rectifier with state-of-the-art integrated wireless power receivers. With the new topology introduced in this paper, the proposed receiver achieves the highest efficiency, the highest level of integration, the fastest transient responses, and the smallest chip area among all the designs summarized in the table.

V. Conclusion

This paper presents a wireless power receiver using a 3-mode R^3 rectifier for R-WPT. The proposed receiver improves power conversion efficiency and reduces die area and off-chip components by achieving power conversion and voltage regulation in one stage, using only four on-chip power transistors and one off-chip capacitor. With the proposed 3-mode operation, the output voltage ripples are reduced and switching synchronization can be easily accomplished. A PWM controller using two stacked ramp signals achieves voltage regulation in the full loading range with fast transient responses. An adaptive sizing method is also employed to further improve the light-load efficiency of the receiver. The proposed receiver is fabricated in a 0.35-μm standard CMOS process, and experimental results verify the effectiveness of the proposed topology. It achieves the highest efficiency, highest level of integration, fastest transient responses, and smallest chip area when compared with state-of-the-art designs, making it one of the most promising approaches in designing wireless power receivers.

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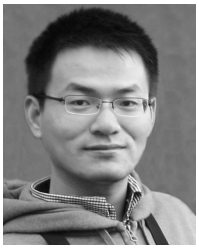

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