

A 200-mA Digital Low Drop-Out Regulator With Coarse-Fine Dual Loop in Mobile Application Processor

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Abstract—This paper proposes a coarse-fine dual-loop architecture for the digital low drop-out (LDO) regulators with fast transient response and more than 200-mA load capacity. In the proposed scheme, the output voltage is coregulated by two loops, namely, the coarse loop and the fine loop. The coarse loop adopts a fast current-mirror flash analog to digital converter and supplies high output current to enhance the transient performance, while the fine loop delivers low output current and helps reduce the voltage ripples and improve the regulation accuracies. Besides, a digital controller is implemented to prevent contentions between the two loops. Fabricated in a 28-nm Samsung CMOS process, the proposed digital LDO achieves maximum load up to 200 mA when the input and the output voltages are 1.1 and 0.9 V, respectively, with a chip area of 0.021 mm². The measured output voltage drop of around 120 mV is observed for a load step of 180 mA.

Index Terms—Coarse-fine control, current-mirror flash analog to digital converter (CMF ADC), digital low drop-out (LDO) regulator, dual loop, linear-regulator, shift register control, transient response.

I. INTRODUCTION

IN A mobile power system (MPS), the application processor (AP) requires a variety of power levels to supply the various internal intellectual properties (IPs), such as central processing unit, graphics processing unit, display controller, memory controller, and so on. Usually, a power management integrated circuit [1] on the same printed circuit board (PCB) supplies the multiple power levels to the AP. This conventional MPS, however, suffers severely from the parasitic effects of the PCB trace patterns. For example, the parasitic inductance due to the PCB routing pattern induces voltage spikes and ripples;

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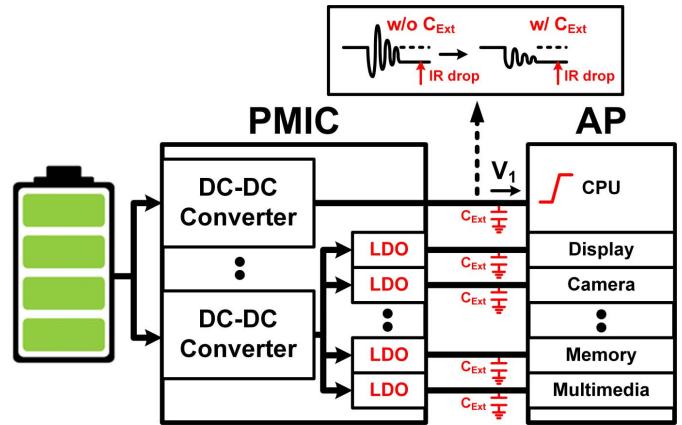


Fig. 1. Basic scheme of the MPS.

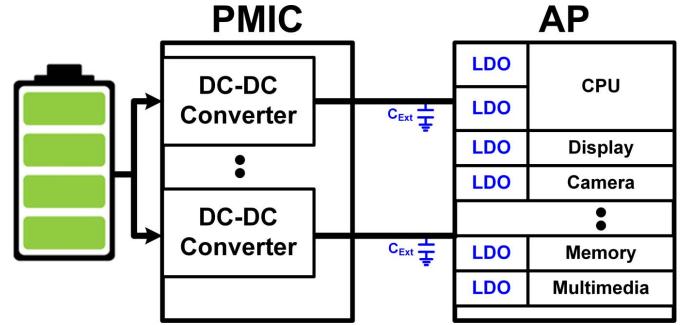


Fig. 2. New scheme of the MPS.

similarly, the parasitic resistance generates resistive drop on the voltages seen by the IPs. Fig. 1 shows an upgraded MPS, which alleviates the effect of the parasitic inductance by applying a filtering capacitor immediately close to the power pin of each IPs. The extra capacitors, however, significantly complicate the PCB design and increase cost. In addition, the shown scheme in Fig. 1 still suffers from the resistive voltage drops.

Fig. 2 shows the new MPS, which integrates the low drop-out (LDO) regulators inside the mobile AP. As is seen,

the extra device count is greatly reduced, leading to simplified PCB routing and lower cost. Besides, since the LDOs can be integrated close to the IPs, the parasitic effects of the PCB trace patterns are almost negligible. The integrated LDOs usually require large driving capacity and fast transient responses. For example, the digital controller IP which contains huge numbers of fast switching devices imposes a large and drastic load current change when the switching devices are dynamically ON and OFF. The maximum load current for such types of IPs can be as high as 200 mA. In addition, since a complicate mobile AP system requires numbers of LDOs to supply various IPs, the sizes of the LDOs should be kept small. In summary, for good integration with AP, the LDOs require high output current capacity, fast transient responses, and small chip area.

The structure of the LDOs is classified based on the way, the current of power transistor is controlled. An analog LDO controls the voltage from gate to source of the power transistor, whereas a digital LDO controls the number of the power transistor (ON or OFF control), as shown in Fig. 3. The analog LDO [2]–[10] usually consists of an error amplifier, a buffer driver, and a power transistor, whereas the digital LDO [11]–[18] consists of a digital controller and a switch array. Compared with the analog counterparts, the digital LDOs have three advantages, i.e., smaller power transistor area, less stability issue, and better process scalability. On the area aspect, the area of an LDO is usually dominated by that of its power transistors. Since the analog LDO should maintain minimum headroom voltage for each transistor to stay in saturation region, the operating range of the buffer driver is always limited, especially when low driver output impedance is required. On the other hand, the digital LDO fully turns on-and-off each power transistor. The gate-to-source voltage of digital LDO's power transistor is thus larger than that of the analog LDO, leading to significantly reduced chip area under the same supply voltage and load current requirements. In addition, from the frequency compensation aspect, the analog LDO is also more complex. For example, the load current variation induces a load-dependent pole at the output of the analog LDO, the frequency of which could range by decades. This wide variation of the pole location increases the design difficulties of LDOs. The digital LDOs, however, do not sense the small signal pole variation, because digital LDOs usually have comparator-based control, which acts only when the output voltage moves beyond the hysteresis window made by comparator delay [16]. Therefore, the digital LDOs have less load-dependent stability issues. Although the digital LDOs have three advantages over analog LDOs, they have two disadvantages also, i.e., more output voltage ripple and low power supply rejection ratio (PSRR). On the ripple aspect, since the digital LDOs are unable to match driving current with the load current because of their controlling mechanism involving a number of power transistors, the ripple exists in the output voltage. In addition, from PSRR aspect, the power transistors operate in deep triode region, and in this region, the device resistance from power to output is very small. This small resistance of the power transistors leads to low PSRR. So, the digital LDOs present a few problems when

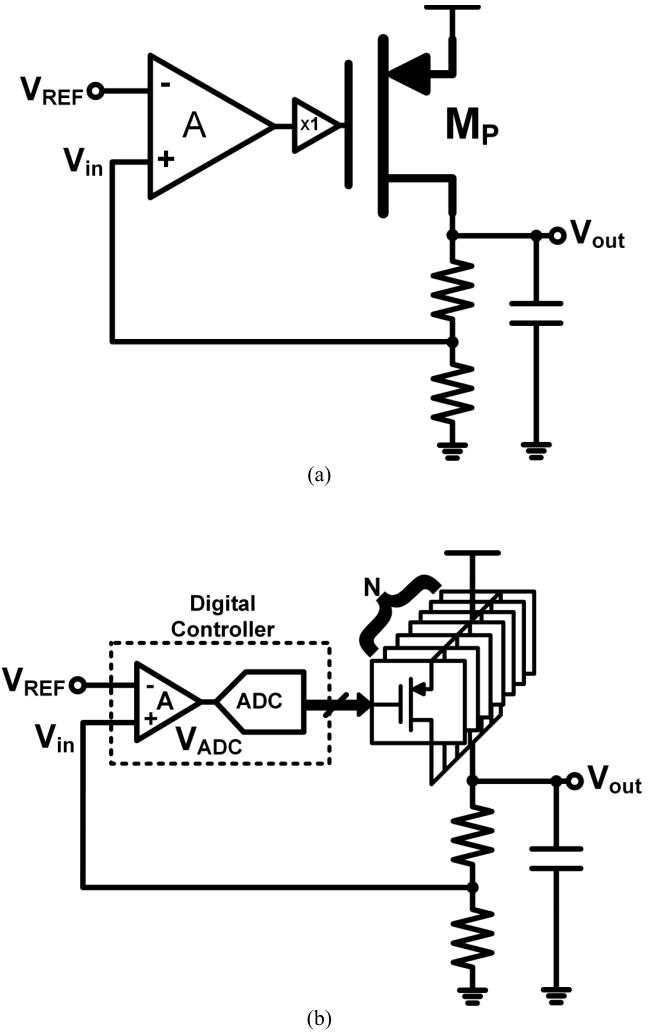


Fig. 3. Conventional structure of (a) analog LDO and (b) digital LDO.

driving sensitive circuits, i.e., power amplifier, analog to digital converter (ADC), phase locked loop, and so on. However, the mobile AP is less sensitive to power noise than core analog blocks, because the digital circuits in the mobile AP operate either “H” or “L.” In addition, the one thing of competitiveness in the mobile AP is small size. Therefore, the integrated LDOs should occupy small chip area. Finally, as the technology is shifting to lower nodes, the device process used in mobile AP is becoming progressively smaller. For these reasons, the digital LDOs have many advantages to be integrated within the mobile AP.

The reliability of the power transistor is a major concern, when an LDO is intended to drive large current or has large drop-out voltage [19]. The driving current of a power transistor unit cell needs to be set considering heating and ageing issues. In an analog LDO, all the power transistor units drive load current separately, hence, the analog LDO can operate well regardless of any reliability concern. However, in the case of a digital LDO, because the number of the power transistor unit decides driving current, and one power transistor unit always drives maximum current whenever it is ON, this can potentially lead to some reliability issues. But even in this case, if the drop-out voltage of an LDO is small, the maximum current of

TABLE I
COMPARISON TABLE TO ANALOG LDO AND DIGITAL LDO

Property \ Structure	Analog LDO	Digital LDO
Size of Power Transistor	Large	Small
Compensation	Load dependent	Less load dependent
Process Scale Down	Limitation	Development
Ripple @output voltage	No	Yes
Power Supply Rejection Ratio	Good	Bad
Reliability	Less concern	More concern

one power transistor unit will be limited and reliability will not be a concern. In the proposed design, the drop out voltage range is small, hence, reliability was not a major concern. Table I summarizes the specifications of the digital LDOs to the analog counterparts.

Although the digital LDOs seem like a prominent candidate for the integration with the mobile AP, the existing topologies are difficult to integrate [11]–[18]. The digital LDOs using shift registers [11]–[14] achieve high dc accuracy. However, this scheme is limited by the transient responses, because the output codes of the shift registers cannot change between the rising edges of the synchronization clock. Therefore, those LDOs adopt bulky external capacitors (100 nF [11]) and achieve only small output current capacity (4.6 mA [14]). The LDO using self-biased CMOS inverters [15] has fast transient response. But, because of the low loop gain, it shows poor output voltage dc accuracy ($\pm 10\%$). The distributed LDO [16], [17] achieves fast transient response with high dc accuracy at the cost of large amounts of current for controlling many blocks. The phase locked digital LDO [18], which consists of pure digital circuits, can be easily realized using logic blocks, however, it has a small driving capacity (~ 5 mA) and poor transient performance (~ 150 -mV output voltage undershoot with load transient from 0.4 to 1.2 mA).

This paper describes a new coarse-fine dual-loop digital LDO (CFL-DLDO) architecture, which achieves 200-mA current capacity with an area of only 0.021 mm^2 [20]. In addition, the maximum current efficiency is 99.94%. This paper is organized as follows. Section II reviews the architectures of the prior digital regulators and explains the need for the proposed coarse-fine dual loop architecture. Section III describes in detail the implementation of main building blocks and techniques used in the design. The experimental results and performance summary of the CFL-DLDO are provided in Section IV, and finally the conclusions are given in Section V.

II. CONTROL TECHNIQUES OF DIGITAL REGULATORS

A. Shift Register-Based Control

Fig. 4(a) shows the architecture of the digital LDOs using a clock-based comparator and a shift register to control the

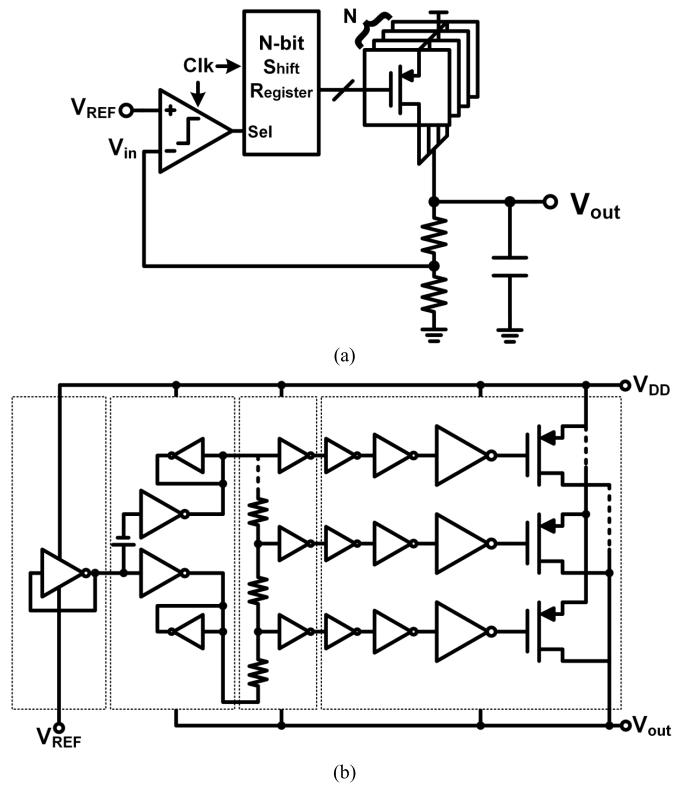


Fig. 4. Architectures of (a) shift register-based digital LDO and (b) self-biased inverter-based digital LDO.

power switch array [11]–[14]. In this control scheme, the comparator compares V_{REF} and V_{in} at every rising edge of the clock, and the comparator output determines the moving direction of the shift register. For example, when $V_{\text{in}} < V_{\text{REF}}$ and the comparator output become ‘H,’ the shift register shows a right shift operation with a turn-on signal pumped to the left-most register. Then, one more power transistor unit is turned on after the shift. When $V_{\text{in}} > V_{\text{REF}}$ and the comparator output gives ‘L,’ the shift register then gives a left shift operation with a turn-off signal pumped to the right-most register. Therefore, one power transistor unit is turned off

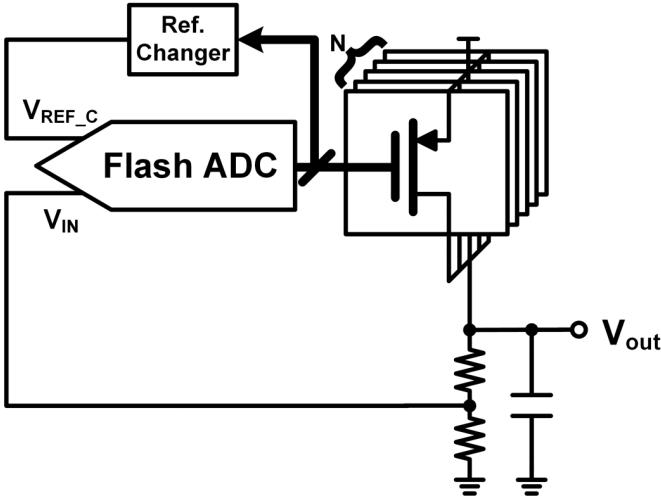


Fig. 5. Proposed architecture of the flash ADC-based digital LDO.

after the shift. The shift continues until $V_{\text{REF}} = V_{\text{in}}$. As can be seen from the operation, this control scheme converts the difference between V_{REF} and V_{in} into a time-dependent codes series, similar to a time to digital converter. Besides, since only one power transistor unit can be turned on or off during one period of clock, this topology is inherently slow in transient responses. Although some solutions are provided to turn on or off more transistor units for each clock cycle [12], [14], this topology still cannot respond immediately when the transition events occur between the rising edges of clock, leading to degraded transient response performance. On the other hand, this scheme shows good dc regulation performance, since it uses a high gain comparator, also the minimum supply voltage can be as low as 0.5–0.6 V [11], [13], [14].

B. Self-Biased Inverter-Based Control

One kind of digital regulators achieving fast transient response is the self-biased inverter-based control, as described in [15]. This regulator is made of half V_{DD} and composes of a push and a pull part. Fig. 4(b) shows the push part of this regulator. The first self-biased inverter connected to V_{REF} is the reference voltage generation block, the output of which is compared with the self-biased voltage related to V_{out} . The difference between V_{REF} and V_{out} is then digitized by an ADC in thermometer code. This scheme achieves response time as short as 288 ps. However, the dc error is as large as 118 mV when the load current varies from 0 to 1 A. Besides, the quiescent current varies considerably with temperature and process variations. Finally, because this scheme only generates half V_{DD} , it is not easily applicable to LDO regulators design.

C. Proposed Flash ADC-Based Control

Fig. 5 shows the proposed architecture of the flash ADC-based control scheme. Compared with the typical structure of digital LDOs given in Fig. 3(b), this scheme removes the error amplifier and inserts a code-dependent reference changer. As will be discussed, the removal of error amplifier

enhances the transient response performance and the reference changer compensates the output voltage error resulting from the low gain nature of the topology. From Fig. 3(b), the transient response time of a typical digital LDO is decided both by the delay of the error amplifier and by the conversion time of the ADC. The conversion time of ADC can be as low as 1 ns, as described in [21], while the delay of the error amplifier is determined by the amplifier's unity gain bandwidth. Given typical error amplifier's transconductance of about 100 μS for high dc regulation and parasitic capacitance of around 100 fF, the unity gain bandwidth of the error amplifier is

$$\text{UGBW} = \frac{1}{2\pi} \frac{g_m}{C_L} \approx 166 \text{ MHz} < 1 \text{ GHz}. \quad (1)$$

Obviously, the error amplifier limits the transient response more severely than the ADC does. The proposed flash ADC-based control scheme removes the error amplifier so the total delay in the control loop is only governed by that of the ADC's. Besides, since the flash ADC has the fastest speed among the various ADC architectures, this proposed scheme shows inherent fast transient response.

However, the speed improvement comes at the cost of reduced dc regulation accuracy. Because of the removal of the error amplifier, the total loop gain is significantly reduced, leading to large static error at the output voltage. For the typical structure shown in Fig. 3(b), the input of ADC, V_{ADC} , equals the difference between V_{REF} and V_{in} amplified by the error amplifier A, that is

$$V_{\text{ADC}} = A(V_{\text{REF}} - V_{\text{in}}). \quad (2)$$

The static error, which is the difference between V_{REF} and V_{in} , is obtained by

$$V_{\text{err}}(\text{max}) = V_{\text{REF}} - V_{\text{in}} = \frac{V_{\text{ADC}}(\text{max})}{A} \approx 0. \quad (3)$$

As is shown, the static error can be suppressed significantly by exploiting a large error amplifier gain A. The maximum error of the proposed flash ADC architecture, however, is defined by

$$V_{\text{ADC}} = V_{\text{REF}} - V_{\text{in}} \quad (4)$$

$$V_{\text{err}}(\text{max}) = V_{\text{REF}} - V_{\text{in}} = V_{\text{ADC}}(\text{max}) \neq 0. \quad (5)$$

Given the same dynamic range and resolution of the ADC, the static error of the proposed scheme is A times larger than that of the conventional structures. It can be seen that, since the proposed flash ADC scheme is essentially a proportional control scheme, each code change of ADC corresponds to an error voltage between V_{REF} and V_{in} . The larger the code change is required (such as the case when all the power switches turn on), the larger the error between V_{REF} and V_{in} is to be observed, as is shown in Fig. 6(a). In order to compensate this error, a code-dependent reference changer is implemented. Since the ADC code information is available and the ADC resolution is predefined, the difference between V_{REF} and V_{in} for a specific code can be exactly compensated by adjusting the reference voltage by the error amount. For a negative error, the reference voltage is boosted, and vice

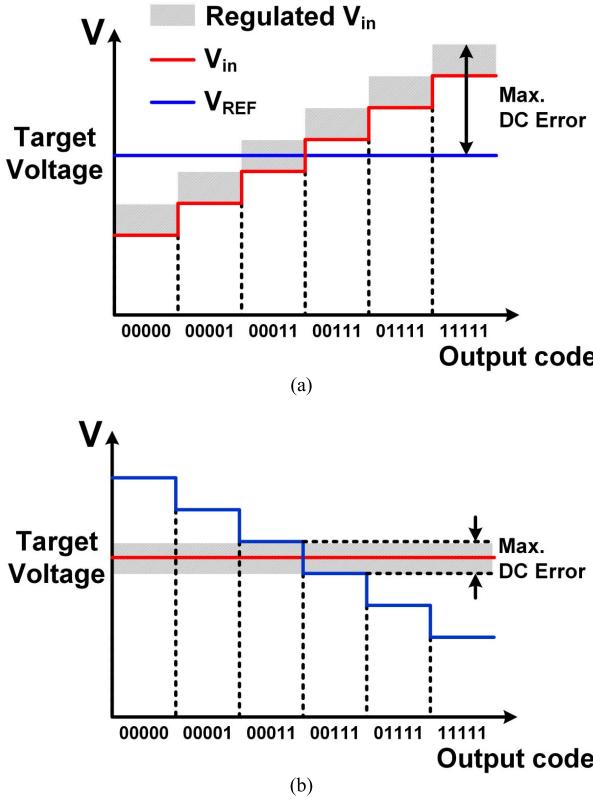


Fig. 6. DC error according to the output code. (a) Without reference changer. (b) With reference changer.

versa. Fig. 6(b) shows that, by applying the code-dependent reference changer, the error between V_{in} and the final target voltage can be reduced within one least-significant-bit (LSB) of ADC. In order to suppress the regulation error even further, the coarse-fine dual-loop architecture is proposed.

D. Proposed Coarse-Fine Dual-Loop-Based Control

As is discussed, the flash ADC-based control achieves fast transient responses and its regulation accuracy is one LSB of the flash ADC, which could still be large, given the high speed nature of the flash type ADC. Since the shift register-based control scheme obtains high regulation accuracy as mentioned before, this paper proposes to combine the flash ADC-based control with the shift register control scheme to achieve both fast transient response and high regulation accuracy.

Fig. 7 shows the proposed architecture of the CFL-DLDO. The proposed CFL-DLDO consists of a coarse loop, a fine loop, and a digital controller. The coarse loop adopts the flash ADC control scheme and the fine loop obeys the shift register-based control. The digital controller resolves the possible contentions between the coarse loop and the fine loop. Since the coarse loop is responsible for large load transition and the fine loop is responsible only for the fine tuning of the final voltage, the coarse loop is equipped with large current capacity and the fine loop with low current capacity. Each unit of the power switch array in the coarse loop is of the same size as that of the total sum of the power switches in the fine loop. In case of an abrupt load increase, the coarse loop immediately

turns on the required number of power transistors according to the code from the flash ADC, and then the fine loop turns on finer number of power transistors to improve regulation accuracy and to reduce the final output voltage ripple. Since the flash ADC senses the output voltage (V_{out}) continuously, instead of sensing by a synchronous clock, the CFL-DLDO can respond immediately to a load transition at any point of time and obtains fast transient performance. Moreover, the proposed scheme achieves large current driving capacity with low power consumption considering that only the flash ADC consumes static current. The detail operation of the CFL-DLDO is described in Section III.

III. DESIGN OF THE DIGITAL LOW DROP OUT REGULATOR WITH COARSE-FINE DUAL-LOOP

A. Operations of the Coarse-Fine Dual-Loop Digital LDO

In the prototype design, each unit of power switch in the coarse loop can supply 40-mA load current, and each unit of power switch in the fine loop drives 2 mA. Since there are 20 units of power switch in the fine loop, the total current capacity of the fine loop is 40 mA. The following describes the key algorithm for properly controlling both loops.

Fig. 8 shows the operation state diagrams. State-A is the steady state with the coarse loop code $C_{LPT}[4:0]$ unchanged and with the fine loop code $C_{SPT}[19:0]$ toggles one certain bit for each period of clock. For example, when the fine loop conducts an average current of 21 mA, the fine loops current changes repeatedly between 20 and 22 mA, with $C_{SPT}[10]$ toggling between "H" and "L." In case of an abrupt load current increase, the current mirror flash ADC (CMF ADC) immediately adjusts $C_{LPT}[4:0]$ and triggers state-B operation. In state-B, the fine loop is disabled with all the power switches in the fine loop turning off. Since only the coarse loop is active during the state-B, the loop eventually settles with only one certain bit of $C_{LPT}[4:0]$ repeatedly toggling. Once this toggling pattern is detected, the state moves from stage-B to state-C, in which a proper initial code for the fine loop $C_{SPT}[19:0]$ is estimated by the digital controller. $Init[2:0]$ controls the initial code for $C_{SPT}[19:0]$. After the fourth toggle of one certain bit of $C_{LPT}[4:0]$, with other bits of $C_{LPT}[4:0]$ unchanged, $Init[2:0]$ is determined and the operation enters stage-D. In state-D, the 20-b shift register of the fine loop is initialized according to $Init[2:0]$. The power switches of the fine loop, however, remain OFF during the state-D. On the eighth toggle of the certain bit of $C_{LPT}[4:0]$, the fine loop is enabled with an initial output current corresponding to $Init[2:0]$. Finally, the algorithm settles to state-A in steady state.

Figs. 9 and 10 show the timing diagram and the circuit operation of the CFL-DLDO, respectively, when load transition occurs from 20 to 200 mA. Before the transition occurs, the circuit stays in the steady state of state-A with load current (I_L) of 20 mA. Because I_L is smaller than 40 mA, the full current capacity of the fine loop, Fig. 10(a) indicates that the fine loop alone supports the entire load current. V_{out} is regulated by the comparator of the fine loop. When I_L changes abruptly from 20 to 200 mA, V_{out} starts to drop.

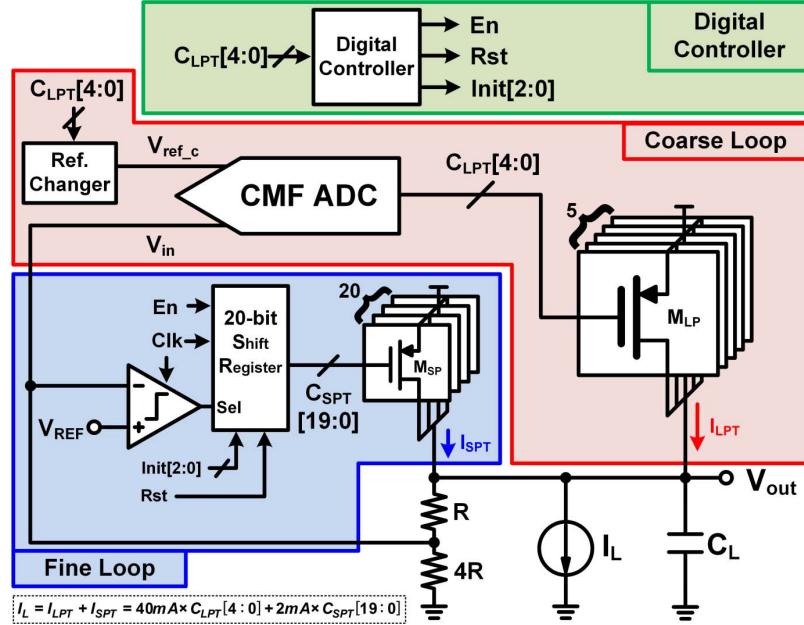


Fig. 7. Proposed architecture of the CFL-DLDO.

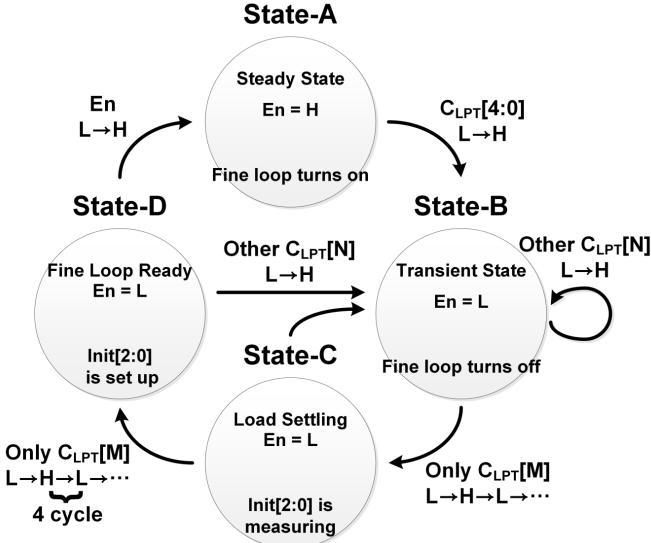


Fig. 8. State diagram of the CFL-DLDO.

The CMF ADC senses the V_{out} drop and instantly adjusts the coarse loop code and enters state-B, with circuit operation, as shown in Fig. 10(b). Now, the fine loop is disabled in order to avoid contentions and the coarse loop alone supports the load current. Apparently, the dropout voltage is reduced, because the coarse loop can supply large output current instantaneously. When the coarse loop settles, only one bit of $C_{LPT}[4:0]$ starts to toggle. In this specific case, $C_{LPT}[4]$ toggles between “H” and “L” with $C_{LPT}[3:0]$ being “0000.” In other words, the coarse loop supplies 160-mA constant current and 40-mA pulsating current. Once only one bit of $C_{LPT}[4:0]$ toggles, the circuit enters state-C, with circuit operation given in Fig. 10(c). After the fourth toggle of $C_{LPT}[4]$, the initial current estimation for the fine loop starts and state moves to

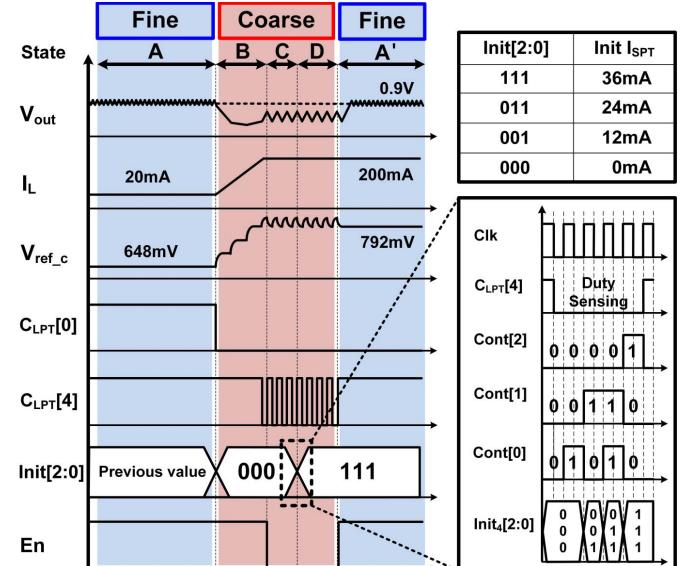


Fig. 9. Timing diagram of the CFL-DLDO when the load current changes from 20 to 200 mA.

state-D. In state-D, after the eighth toggle of $C_{LPT}[4]$, the digital controller enables the fine loop with the initial current determined in state-C. Without the initial current estimation, the V_{out} drop can be observed when the fine loop turns on. Finally, the circuit settles to state-A, as shown in Fig. 10(e). V_{out} is accurately regulated by the fine loop, with coarse loop and fine loop conducting 160 and 40 mA, respectively.

B. Current Mirror Flash ADC and Reference Changer

Fig. 11 shows the schematic of the CMF-ADC [22]. The CMF-ADC consists of a G_m cell and current-to-code converter. The G_m cell converts the difference between V_{in} and V_{refc} into an error current I_{err} . Here, with a tail current of $2I_B$

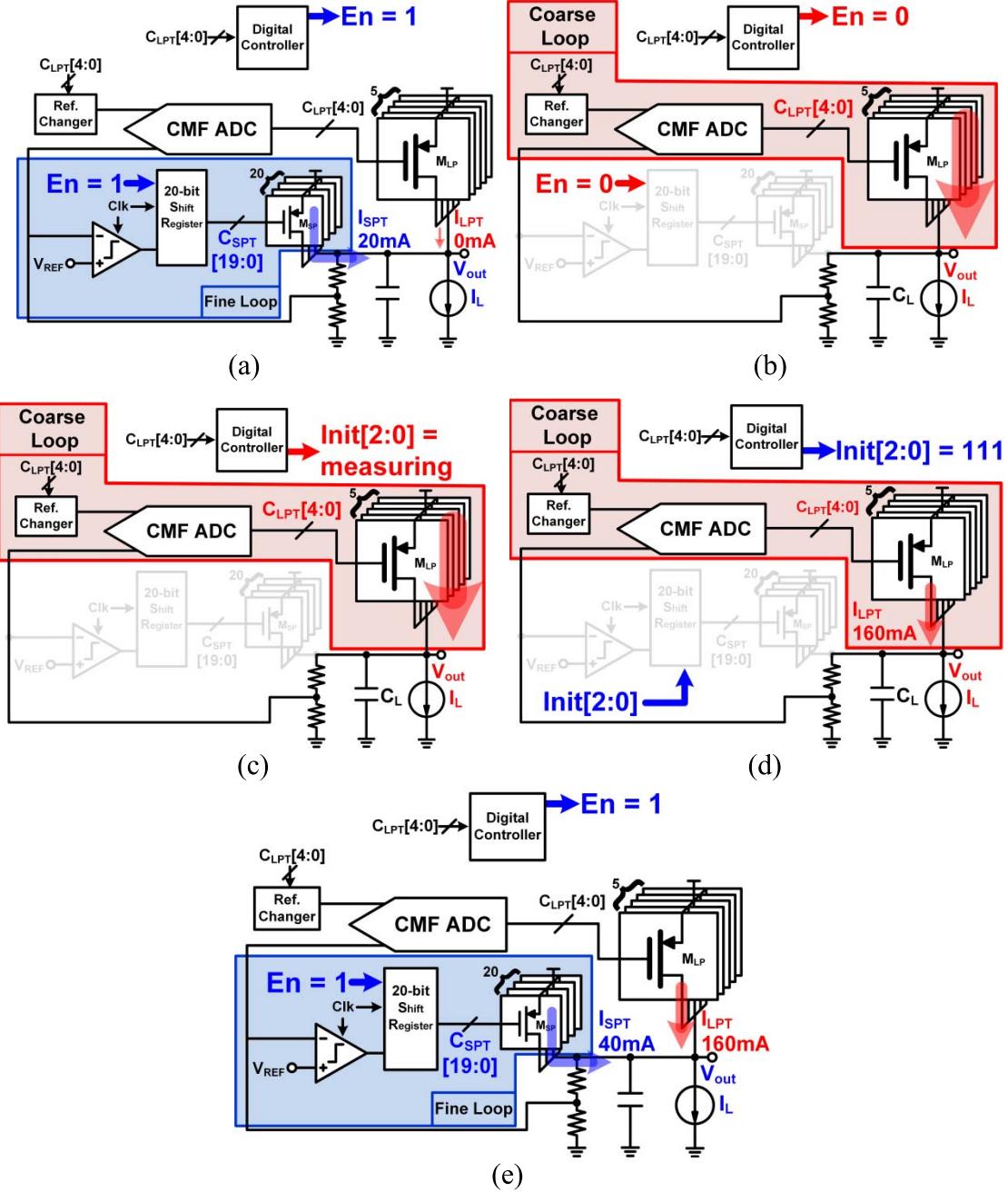


Fig. 10. Operation when the load current changes from 20 to 200 mA. (a) State A. (b) State B. (c) State C. (d) State D. (e) State A.

for the input differential pair, $I_1 = I_B - I_{\text{err}}$, $I_2 = I_B + I_{\text{err}}$, and I_3 replicates I_1 . By applying proper size ratios to the nMOS and pMOS current mirrors, the logic threshold voltage for a specific C_{LPT} code can be properly defined. For the size ratios given in Fig. 11, the logic “L” condition for each C_{LPT} code is given by

$$\begin{aligned} C_{LPT}[0] : I_{\text{err}} &< \frac{8}{20} I_B, \quad C_{LPT}[1] : I_{\text{err}} < \frac{4}{20} I_B \\ C_{LPT}[2] : I_{\text{err}} &< 0, \quad C_{LPT}[3] : I_{\text{err}} < \frac{4}{20} I_B \\ C_{LPT}[4] : I_{\text{err}} &< \frac{8}{20} I_B \end{aligned} \quad (6)$$

where I_{err} determines the $C_{LPT}[4:0]$ code. The larger the error current is, the larger the code change will be. Since I_{err} is related to the difference between V_{in} and V_{refc} , each nonzero code change translates into a nonzero offset to the final output voltage. As mentioned in Section II, the reference changer compensates this dc regulation error. Fig. 12 shows the reference changer, which consists of resistors, capacitors, switches, and a decoder. The coarse loop code, $C_{LPT}[4:0]$, selects the corresponding switch to change the reference voltage. The capacitors reduce the switching noise when the $C_{LPT}[4:0]$ code change occurs. Table II indicates that the voltage step between each two consequential reference voltages is 36 mV. Considering the resistive divider in the feedback path, the

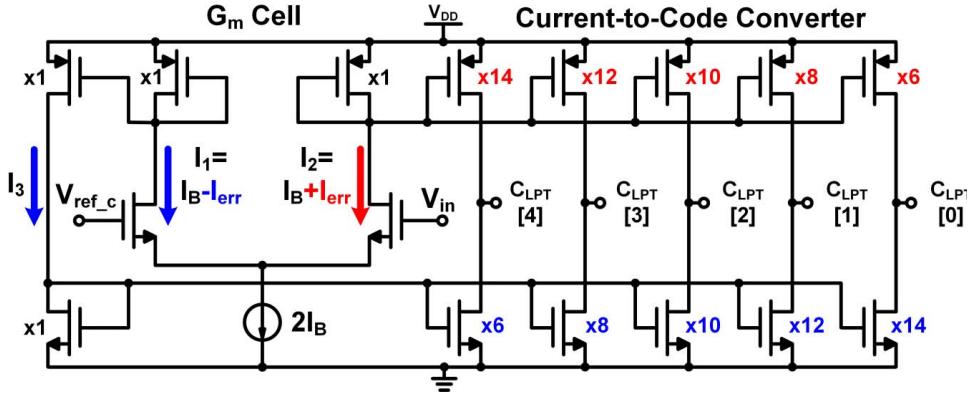


Fig. 11. Schematic of the CMF-ADC.

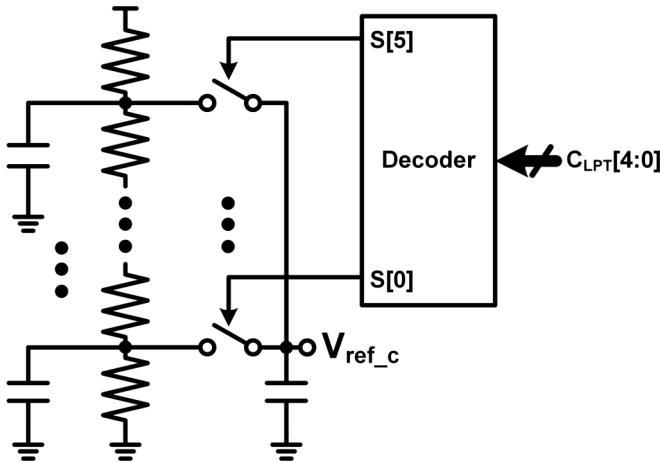


Fig. 12. Schematic of the reference changer.

TABLE II
TRUTH TABLE OF THE REFERENCE CHANGER

$C_{LPT}[4:0]$	$S[5:0]$	V_{ref_c}
11111	000001	648mV
11110	000010	684mV
11100	000100	720mV
11000	001000	756mV
10000	010000	792mV
00000	100000	828mV

final voltage step seen at V_{out} equals 45 mV. Applying the reference changer, the maximum regulation error reduces from 135 to 45 mV.

C. 20-b Shift Register

Fig. 13(a) shows the schematic of the 20-b shift register. This shift register consists of asynchronous set and reset

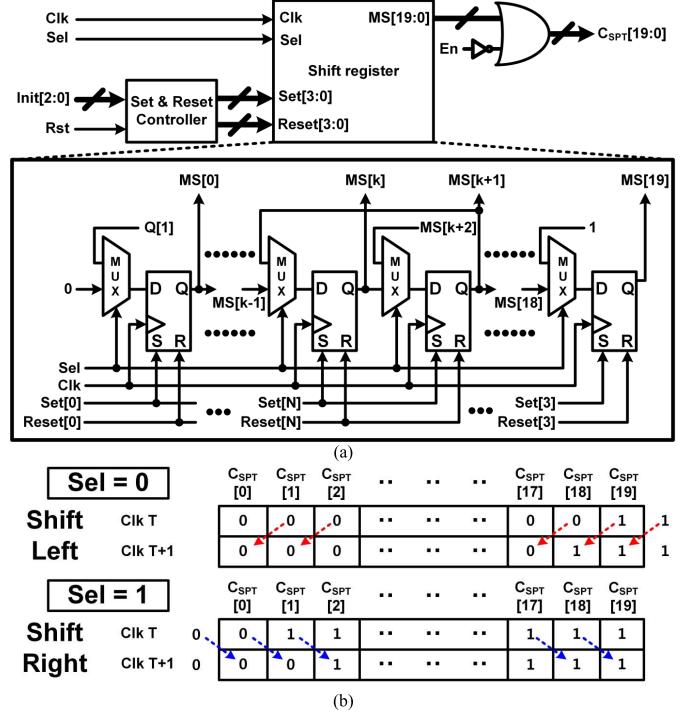


Fig. 13. (a) Schematic and (b) operation of the 20-b shift register.

D flip flops, multiplexers, and combinational logics. Here, the $MS[19:0]$ bits are the output of the shift registers and the $CSPT[19:0]$ bits are the final outputs, which control the power transistors. In normal operation, the shift register shifts to right when Sel is ‘L’ and shifts to left when Sel is ‘H,’ as shown in Fig. 13(b). During the shift right operation, one of $CSPT[19:0]$ changes from ‘H’ to ‘L,’ indicating one more power transistor to turn on. On the other hand, during the shift left operation, one of $CSPT[19:0]$ changes from ‘L’ to ‘H,’ indicating one power transistor turns off. Since the shift register operates at the rising edge of the clock, for each period of CLK, only one bit of $CSPT[19:0]$ changes. Compared with the shift registers in [11], this circuit incorporates asynchronous set and reset controllers. When Rst is ‘H,’ $Init[2:0]$ instantaneously forces each of the register output to ‘H’ or ‘L’ regardless of the clock. The final output, $CSPT[19:0]$, is valid only when En is ‘H.’

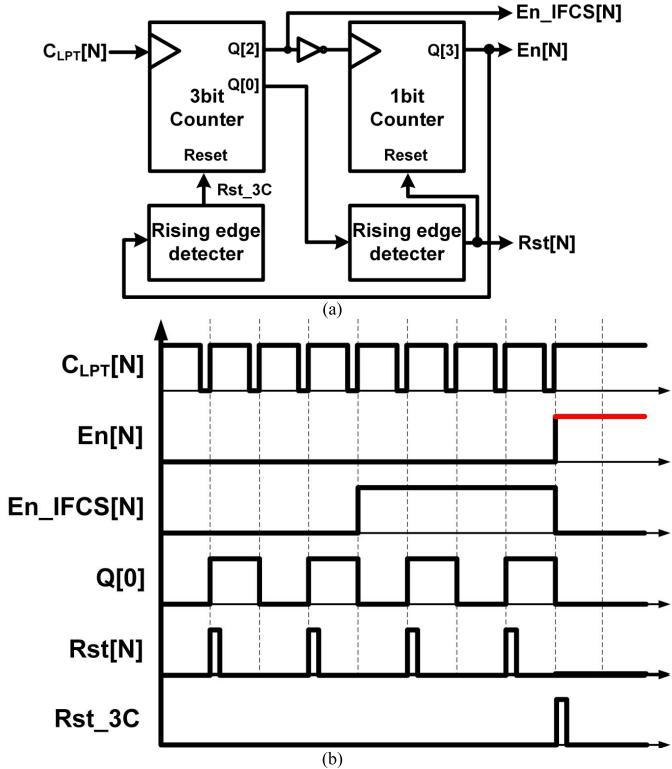


Fig. 14. (a) Schematic and (b) timing diagram of the EFLC.

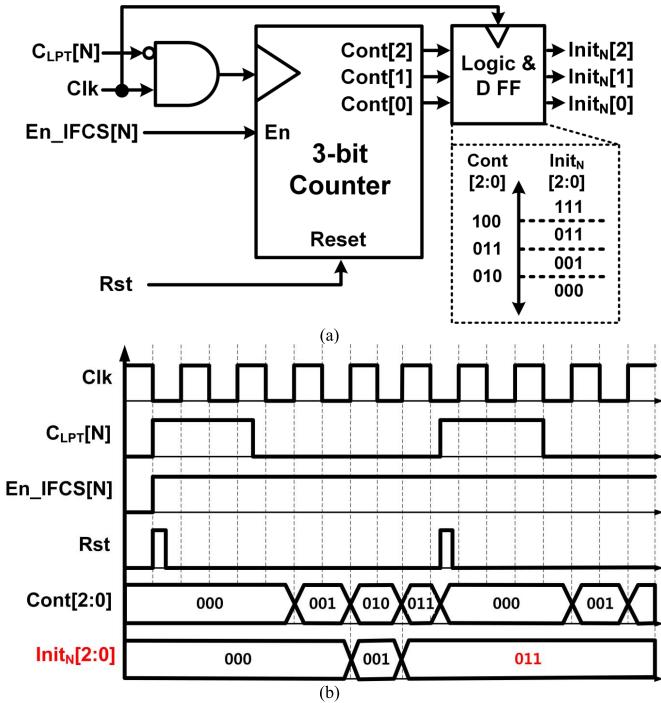


Fig. 15. (a) Schematic and (b) timing diagram of the IFCS.

D. Enable Fine Loop Controller

To control the fine loop, the enable fine loop controller (EFLC) is designed, as shown in Fig. 14(a). The EFLC is composed of five control units similar to the

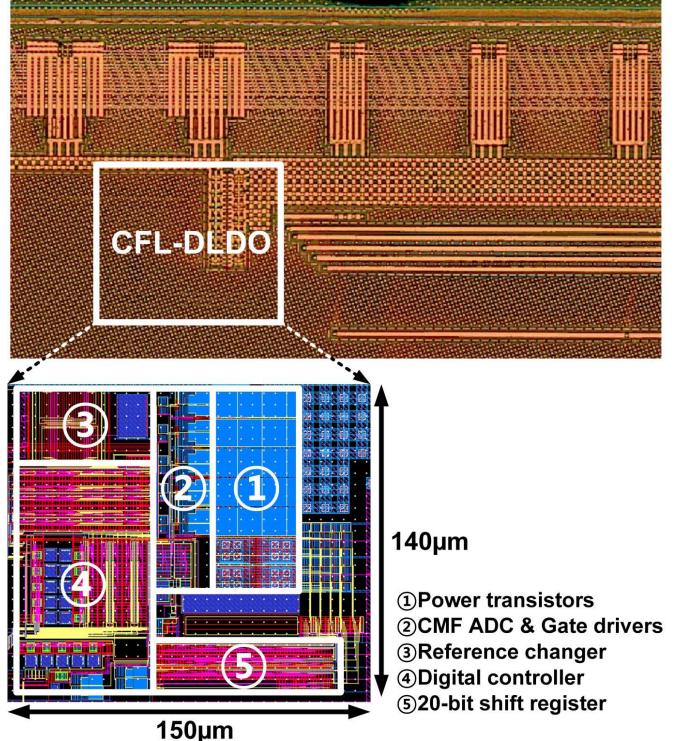


Fig. 16. Micrograph and layout of the CFL-DLDO.

number of the coarse loop codes. When the output load current changes largely, the CMF-ADC changes the coarse loop codes, $C_{LPT}[4:0]$, accordingly. In this situation, the EFLC keeps the fine loop in OFF mode. The clock of the 3-b counter in the control unit of the EFLC is $C_{LPT}[N]$, i.e., one unit out of $C_{LPT}[4:0]$. When $Q[0]$ changes from 'L' to 'H,' the rising edge detector generates Rst to be one pulse wave. Finally, the fine loop code, $C_{SPT}[19:0]$, changes to 'H' in order to turn off all the fine loop power transistor (M_{sp}) and the En changes from 'H' to 'L' to reset the 1-b counter. The operation of this controller is slightly different for cases when there is a decrease or increase in load current. The 3-b counter of the control unit in the EFLC operates at the rising edge of $C_{LPT}[N]$. As shown in Fig. 14(b), the output voltage rises when the output load current decreases, and then, $C_{LPT}[N]$ changes from 'L' to 'H.' Immediately, the EFLC starts operating because of the rising edge. Finally, the fine loop turns off by Rst . In this case, the peaking of the output voltage minimizes, because the fine loop turns off as soon as $C_{LPT}[N]$ changes. On the contrary, the output voltage drops when the output load current increases, and $C_{LPT}[N]$ changes from 'H' to 'L' by the CMF-ADC. In this case, the fine loop does not turn off instantly, because the rising edge does not occur. After the output voltage recovers to common level, $C_{LPT}[N]$ starts toggling. And then, the fine loop turns off because of the occurrence of rising edge. The fine loop not becoming reset instantly helps the output voltage droop. In both the cases, these controls help in fast transient response.

When the load current settles to some level, $C_{LPT}[N]$, one of the coarse loop codes, starts toggling. The 3-b counter output $Q[2:0]$ increases from '000' to '111.' When $Q[2:0]$

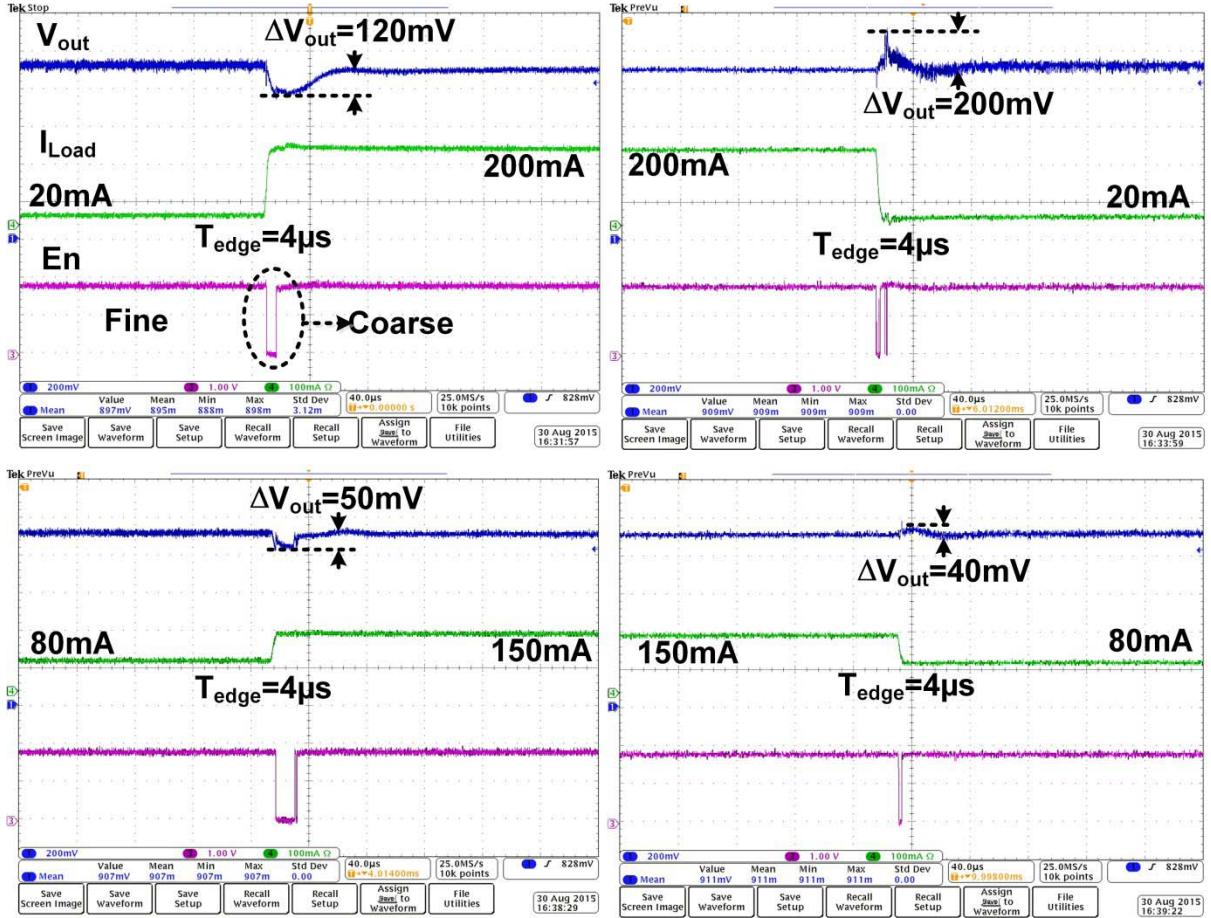


Fig. 17. Measured results for transient response of the CFL-DLDO.

TABLE III
PERFORMANCE TABLE

Paper	[11]	[13]	[14]	[15]	[16]	[18]	This work
Type	Digital	Digital	Digital	Digital	Digital	Digital	Digital
Process	65nm	40nm	130nm	90nm	45nm	32nm	28nm
$V_{in}[\text{V}]$	0.5	0.6	0.5-1.2	2.4	1.179-1.625	0.7-1.0	1.1
$V_{out}[\text{V}]$	0.45	0.4	0.45-1.14	1.2	0.9-1.1	0.5-0.9	0.9
$I_Q[\mu\text{A}]$	2.7	25.1	24-221	25700	12000*	92	110
Max. $I_{load}[\text{mA}]$	0.2	200	4.6	1000	42	5	200
Load capacitor[nF]	100	-	1	-	1.46	-	23.5
$\Delta V_{out}[\text{mV}] @ \Delta I_{load}$	40 @ 0.2mA	-	90 @ 1.4mA	116 @ 1A	7.6* @ 36mA	150 @ 0.8mA	120 @ 180mA
Max. Current Efficiency[%]	98.7	99.99	98.30	97.5	77.5*	97.8	99.94
Area[mm ²]	0.042	0.0375	0.355	0.03	0.075	0.0077	0.021
FOM**	270ns	-	940ps	-	62.4ps*	-	7.75ps

*Simulation result **FOM = $\frac{C_L \Delta V_{out}}{I_{max}} \times \frac{I_Q}{I_{max}}$

changes from 111 to 000, En becomes ‘H,’ because the rising edge occurs in $/Q[2:1]$, and the fine loop turns on. The final En is merged by 5 input OR gate, because the only one

unit operates. Afterward, the 3-b counter has to reset so that $Q[2:0]$ starts with ‘000’ code in the next transient situation. When $Q[2:0]$ is ‘100,’ the EFLC provides the initial fine

current selector (IFCS) with an enable signal. The IFCS will be discussed in the following paragraph.

E. Initial Fine Current Selector

Fig. 15(a) shows the structure of the IFCS that estimates the initial current for the fine loop before the fine loop turns on. The IFCS helps generate a smooth transition from state-D to state-A. Without IFCS, the transition from state-D to state-A would have to bear long settling time and larger output ripple, because the fine loop obeys the low-speed shift register-based control, and the maximum load current for the fine loop could be up to 40 mA. This low-speed shift register-based control and large output ripple can cause coarse loop to turn on and state change to state-B instead of state-A forming a continuous loop of state from state-B → state-C → state-D → state-B → state-C. This problem is solved by selecting the initial current for the fine loop in advance.

The IFCS consists of the five control units that are the same as the number of $C_{LPT}[4:0]$. The IFCS measures the duration for $C_{LPT}[N]$ being ‘L.’ Fig. 15(b) shows the timing diagram for the operation of IFCS. When $C_{LPT}[N]$ is ‘L,’ the 3-b counter counts the number of clock rising edges. When the counter output is smaller than ‘010,’ $Init_N[2:0]$ is set as ‘000,’ corresponding to an initial current of 0 mA. On the other hand, when the counter output is larger than ‘100,’ $Init_N[2:0]$ is set as ‘111,’ giving an initial current of 36 mA. En_1FCS is generated by the EFLC, as shown in Fig. 15. While $C_{LPT}[N]$ is toggling at fourth cycle, En_1FCS maintains ‘H,’ because En_1FCS is the same to $Q[2]$ in EFLC, as shown in Fig. 14. So, the duty for which $C_{LPT}[N]$ is at ‘L’ is measured for four consecutive times. Therefore, the IFCS can measure accurate duration for which $C_{LPT}[N]$ is ‘L.’ Finally, $Init[2:0]$ is merged by 5-input OR gate connected from $Init_0[2:0]$ to $Init_4[2:0]$.

IV. EXPERIMENTAL RESULTS

The CFL-DLDO was fabricated in a 28-nm Samsung CMOS technology. A micrograph and the layout of the CFL-DLDO are shown in Fig. 16. The total power transistors are sized to drive 200-mA load current and occupy only 0.007 mm^2 . The overall circuits of the CFL-DLDO occupy 0.021 mm^2 .

Fig. 17 shows the measured results for the transient responses. In steady state, the dc level of V_{out} is regulated to 0.9 V by the fine loop. When I_{Load} increases from 80 to 150 mA, En changes to ‘L’ and a V_{out} drop of about 50 mV is observed. On the contrary, when I_{Load} decreases from 150 to 80 mA, V_{out} shows an overshoot of about 40 mV. When I_{Load} changes from 20 to 200 mA with 4 μs of rising time, En changes to ‘L,’ the fine loop turns off and V_{out} gives a dropout voltage of 120 mV. When I_{Load} decreases from 200 to 20 mA, V_{out} reaches the supply voltage (1.1 V) with an overshoot of 200 mV. In this result, although the I_{Load} variation is large, V_{out} shows smaller drop voltage than other state-of-the-art digital regulators. The settling time is more than 10 μs , because the CFL-DLDO needs eight cycles for transforming the state. Fig. 18 shows dc load regulation about PVT variation. The dc load regulation is 0.035 V/A in the typical condition (1.1 V/Typ/25 °C). The dc level of the

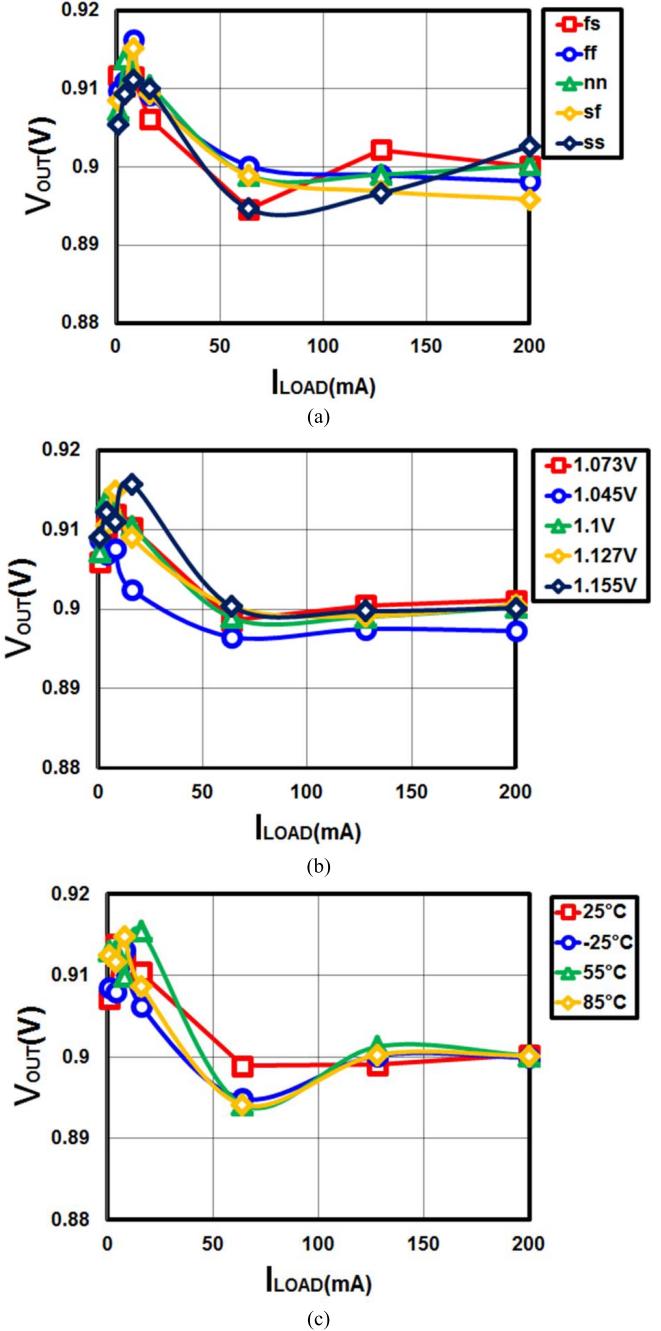


Fig. 18. Simulation results for dc load regulation about (a) process, (b) input voltage, and (c) temperature variation of the CFL-DLDO.

output voltage increases in the light load condition, because the driving current is larger than the load current. Fig. 19 shows the Monte Carlo simulation of the decision voltage difference in $C_{LPT}[4:0]$, a total of 200 Monte Carlo splits were covered. This result guarantees the monotonicity of the CMF-ADC. The performance of the CFL-DLDO is summarized and compared with other LDOs in Table III. The proposed CFL-DLDO generates a 0.9 V output from a 1.1 V supply voltage with a current driving capability of 200 mA, and the area is smallest among all. The figure of merit [it is defined in [8] as $C_L(V_{out}/I_{MAX})(I_Q/I_{MAX})$] of the proposed CFL-DLDO is 7.75 ps, the best performance achieved by

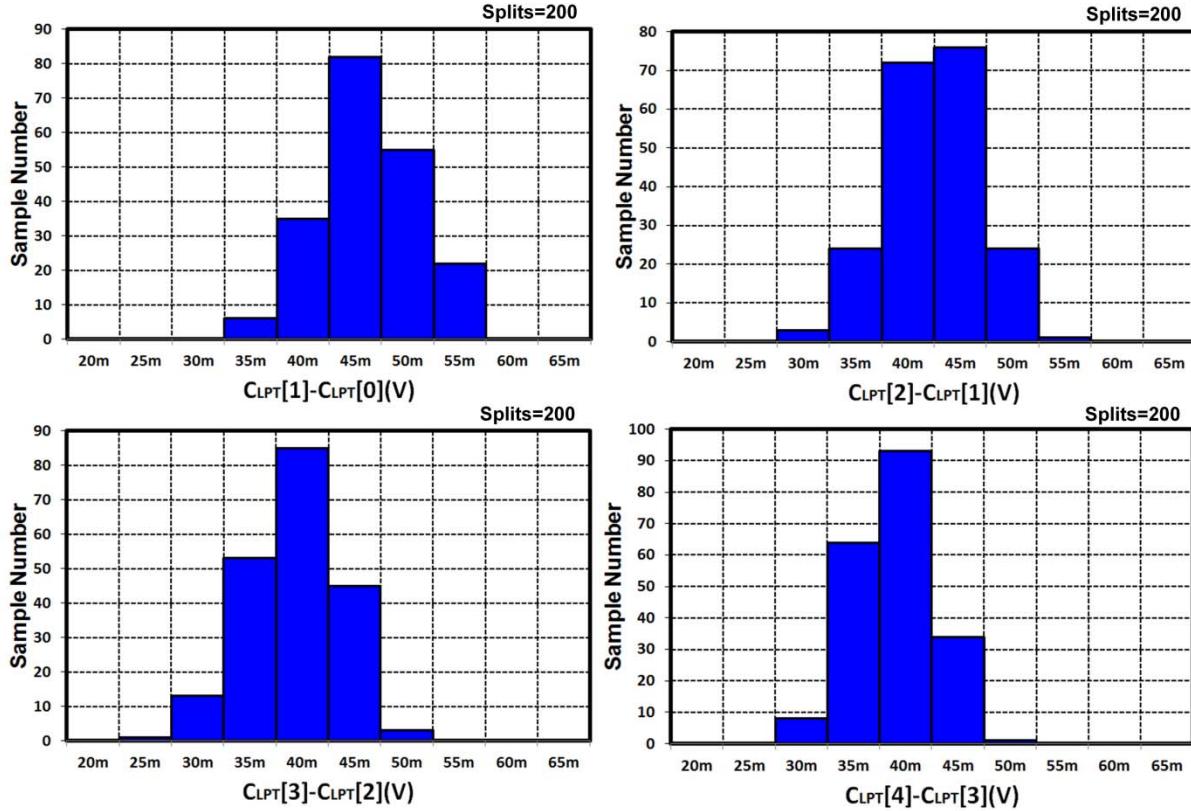


Fig. 19. Monte Carlo simulation results for decision voltage difference about $C_{LPT}[4:0]$.

digital LDOs. In addition, the maximum current efficiency is 99.94%.

V. CONCLUSION

This paper has presented a digital LDO regulator with coarse-fine dual-loop architecture capable of driving large load current (~ 200 mA). The coarse loop adopts flash ADC-based control and achieves fast transient response and LDO voltage (~ 120 mV in case of 180-mA load transition) The fine loop obeys shift register-based control and obtains high dc accuracy and low ripple. The digital controller controls the operation state and ensures system stability. The power consumption compared with other regulators is low for driving load current capability. The size of the proposed CFL-DLDO (0.021 mm^2) is the smallest among the digital regulators as a result of its simple control logic.

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