

256 Gb 3 b/Cell V-NAND Flash Memory With 48 Stacked WL Layers

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Abstract—A 48 WL stacked 256-Gb V-NAND flash memory with a 3 b MLC technology is presented. Several vertical scale-down effects such as deteriorated WL loading and variations are discussed. To enhance performance, reverse read scheme and variable-pulse scheme are presented to cope with nonuniform WL characteristics. For improved performance, dual state machine architecture is proposed to achieve optimal timing for BL and WL, respectively. Also, to maintain robust IO driver strength against PVT variations, an embedded ZQ calibration technique with temperature compensation is introduced. The chip, fabricated in a third generation of V-NAND technology, achieved a density of 2.6 Gb/mm² with 53.2 MB/s of program throughput.

Index Terms—3-D NAND, 3-D nonvolatile memory, 48 WL stack 3-D, flash memory, IO design, NAND flash, VNAND V-NAND, ZQ calibration.

I. INTRODUCTION

TODAY'S explosive demand for data transfer is accelerating the development of storage devices with even larger capacity and cheaper cost. Since the introduction of the 3-D technology in 2014 [1], V-NAND is believed to be a successful alternative to planar NAND and is quickly displacing planar NAND in the SSD market, due to its performance, reliability, and cost competitiveness. V-NAND has also eliminated the cell-to-cell interference problem by forming an atomic layer for charge trapping [2], which enables further technology scaling.

Fig. 1 shows the simplified cell architecture of VNAND. From GSL layer, main WLs and SSL layers are compiled in order. Then, channel hole for cell string is created by the etching process from the top of the SSL. Here, channel hole size ($=2r$) is important, because it affects both physical and electrical characteristics. The larger diameter promotes gas flow for the dry etch process, thereby making it easier to create channel hole. However, it is not desirable because the hole behaves as a physical barrier for current flow with increased WL resistance. Furthermore, channel hole critical

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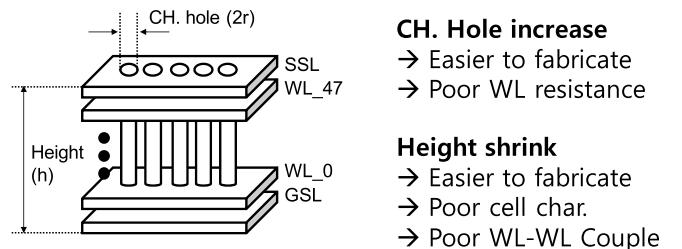


Fig. 1. VNAND scaling challenges.

dimension (CD) increase results in larger chip size. Mold height is another critical process parameter, because higher depth of a channel hole experiences larger amount of CD variation. Also, we may enlarge the hole CD to secure gas flow for the etching process. Therefore, the total mold height reduction is crucial for uniform performance and yield. But it brings several issues as follows: 1) when thickness of WL is reduced, the resistance for the WL is increasing, which leads to read and program performance degradation; 2) when spacer between WLs is reduced, we may need more time to apply a selected WL voltage because of coupling capacitance between WLs; 3) cell-to-cell interference is deteriorated due to the reduced distance between the adjacent cells; and 4) when WL thickness is scale-downed, cell's reliability is getting worse because of the short-channel effect for a cell transistor. For TLC devices, this reliability criterion is very important, because we have tight budget for cell V_t window.

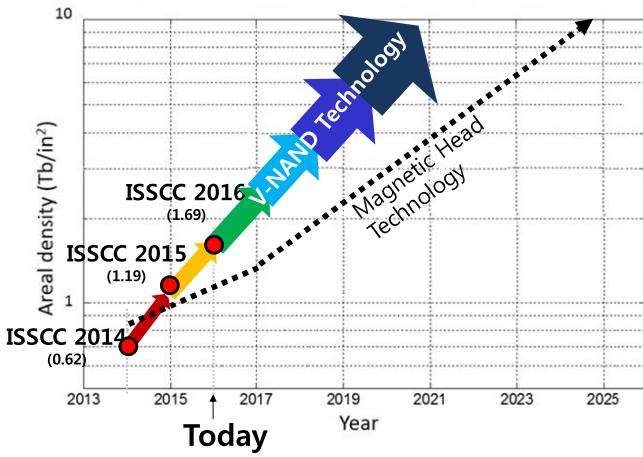
This paper presents a 256 Gb 3 b/cell flash memory with 48 stacked WLs featuring third generation V-NAND technology. In Section II, chip architecture with areal density comparison is discussed. Section III introduces schemes to enhance program and read performances along with the performance optimization technique with novel state machine architecture. Section IV will discuss program scheme for this paper. For reliable IO interfacing with minimal external component, on-chip-resistor-referenced (ZQ) calibration scheme is proposed in Section V. The conclusion is presented in Section VI.

II. CHIP ARCHITECTURE AND AERIAL EFFIEIENCY

When the storage capacity of a chip is doubled, storage cell efficiency in terms of chip size becomes better.



Fig. 2. Die photograph.

Fig. 3. VNAND versus magnetic hard drive technology comparison (IDEMA-ASTC Technology Roadmap <http://www.idema.org/>).

However, performance degradation for certain capacities of SSD is inevitable because interleaving efficiency decreases. To minimize the impact of capacity doubling, with respect to the previous work [3], a two-plane cell-array is implemented with 16 kB of page buffers for each plane with doubled storage capacity of 256 Gb when compared to [3]. The chip micrograph is shown in Fig. 2. A plane contains 1888 blocks, including spares for repair and file system management. The block size is 9 MB with 576 pages. One page unit corresponds to 16 kB.

Fig. 3 shows the VNAND technology trend when compared to magnetic hard disk. In 2014, the first V-NAND of 128 Gb MLC [1] was announced. With 129 mm² and 0.62 Tb/in², it was not up to par with magnetic hard drive in terms of areal density. The next generation came up in 2015 as TLC with the chip size of 68.9 mm² and the areal density of 1.19 Tb/in². The second generation was the first device that is outperforming the magnetic drive's areal density. Last, this paper even expands the gap by achieving 1.69 Tb/in².

III. PERFORMANCE ENHANCING SCHEME

Fig. 4 shows the cell block structure of this paper. There are four SSLs, which are controlled independently. The purpose of having independent SSL structure is to select only one SSL string among others. Similarly, there are four independent

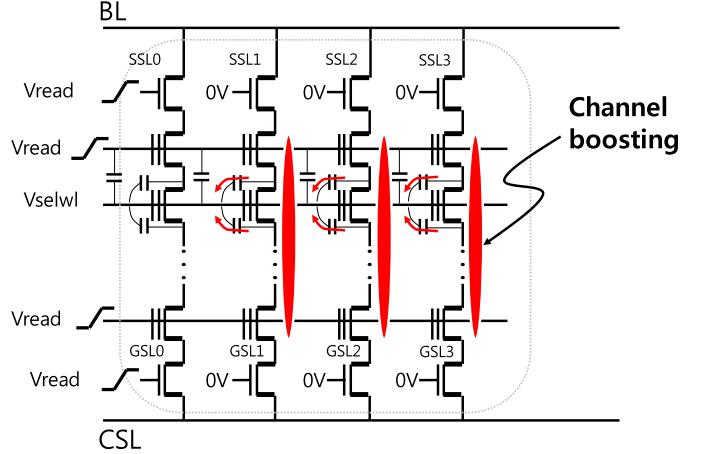


Fig. 4. WL couple issue for VNAND cell architecture.

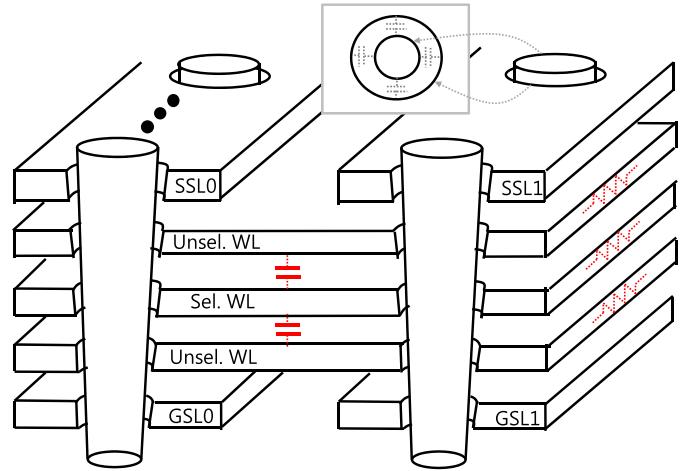


Fig. 5. WL couple issue explain in 3-D.

GSLs in a block to minimize read disturbance. If shared GSL structure is used, all channels from SSL0 to SSL3 will experience FN stress during the read operation, because all strings are connected to CSL. Therefore, it is essential to split all GSLs to prevent excessive read disturbance for VNAND. For instance, as shown in Fig. 4, when SSL0 (GSL0) string is selected and the rest of the SSL and GSL transistors are turned OFF. Then, Vread voltage is applied to unselected WLs and Vselwl is applied to a selected WL. During that time, channel potential for SSL1,2,3 is increasing, because the channels are effectively floated, which eventually lifts unselected WL's voltage. Consequently, this gives rise to selected WL voltage because of the capacitance between WLs. This seriously deteriorates performance, because more settling time is required to reach to the target voltage for the selected WL.

Fig. 5 shows various capacitive coupling elements for VNAND. WL-to-WL couple is significant for VNAND than planar NAND because of the relatively larger area between WLs. The amount of capacitance is directly proportional to the area. Another coupling capacitance exists between the channel hole and WLs. When a channel and a WL are fixed to some voltages, there exists electrical field between them. This small capacitance becomes substantial when we integrate more than 128k channels in a WL.

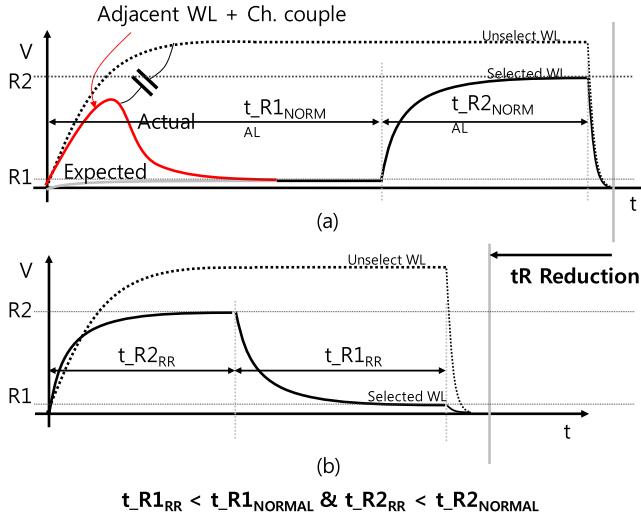


Fig. 6. Reverse read scheme.

For TLC NAND, two or three different levels are used for a read operation. As an example, Fig. 6(a) shows two-level read operation. The read operation at R1 is performed first and R2 read is performed later. However, during the R1 period, selected WL level of R1 is suffered voltage coupling due to voltage changes from adjacent WLs and channels of unselected SSLs. It is not until the adjacent WL's voltage saturates when the selected WL's level is reaching up to the target level. Eventually, we need to extend time period of t_{R1norm} to well execute R1 read operation. Besides, the second read operation is not affected at all, because there is no voltage change for adjacent WLs and channels for other SSL strings.

To resolve this undesirable situation, Fig. 6(b) is proposed. To prevent unwanted voltage disruption for selected WL, rather higher level read of R2 is performed first. Applying higher voltage during the first read phase is beneficial not only it is less affected from voltage disruption but also setup time for R2 is accelerated, because adjacent WL's rising voltage assists the R2 voltage setup at the selected WL. Despite increase in power dissipation due to relatively higher selected WL voltage during the first read operation, this scheme enhanced WL setup time.

As mentioned earlier, during the channel hole etching process, CD variation arises such that top hole CD is largest and WL0's CD is the smallest, as shown in Fig. 7. In other words, WL0's resistance is the smallest, while WL47's resistance is the largest. Similarly, WL0's WL to channel capacitance is the smallest because cross-sectional area between WL and channel hole is the minimum among all WLs. On the contrary, along with the largest resistance, WL47 has the largest capacitance because of the maximum capacitance between the WL and channel capacitance.

This WL loading variation becomes dominant when we perform program operation. For program operation, we apply more than 20 V for several microseconds on a selected WL. If the duration is not enough to reach to the target, we may waste the program pulse, because the voltage is not

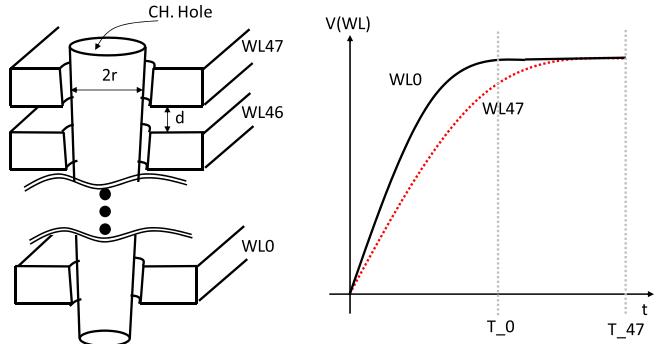


Fig. 7. WL loading variation due to channel hole CD variation.

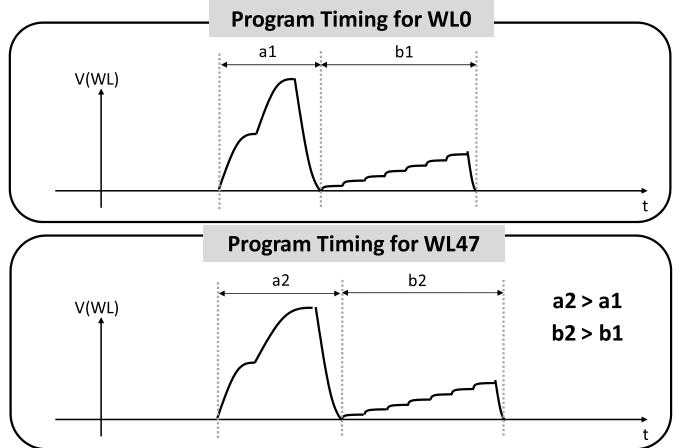


Fig. 8. Variable-pulse scheme to cope with WL loading variation.

enough to increase cell V_t as desired. In the worst case, the program operation will end up with program fail because of this problem. Also, program voltage generator's drivability is another factor because insufficient current supply creates extra delay for voltage setup in WL. However, increasing driver size is not appropriate, because it requires extra area. Furthermore, sufficient width for interconnect width should be reserved by sacrificing routing congestion.

Fig. 8 shows a scheme to resolve this program fail issue against WL loading variation. In the proposed scheme, WL0 is taking a short pulse for program, while WL47 is taking longer program pulse. Similarly, to adjust optimal timing for verify operation, verify timings are also tailored for each WL. In the example, program execution time $a1$ for WL0 is shorter than WL47's $a2$, while verify time $b1$ is shorter than $b2$.

To set customized durations for each WL, control logic needs to have the maximum flexibility for WL, BL, and page buffer time control. In Fig. 9(a), a control circuit can have flexible time delay of t_{12} (that initiates WL voltage change) after a series of page buffer operations. Here, t_{12} should be positive value, such that the next WL voltage is not initiated before the completion of the page buffer operations. With this specific limit in mind, it is impossible to initiate WL voltage earlier than t_1 even though the change is required for a better performance, as shown in Fig. 9(b).

Therefore, WL and BL control logics are separated to provide the maximum flexibility for optimization, as shown in Fig. 10. As shown in the figure, two distinctive WL and BL

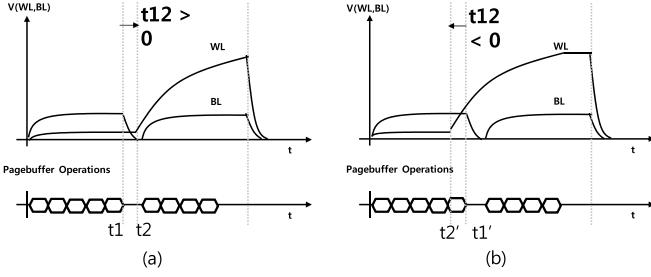


Fig. 9. Performance optimization example for VNAND.

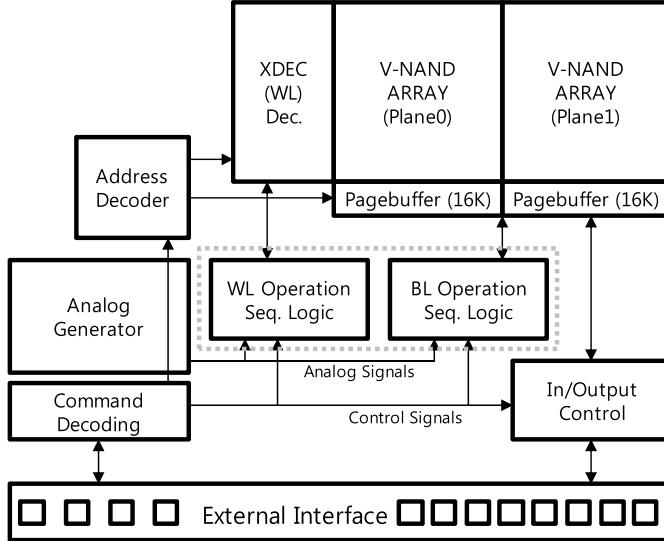


Fig. 10. Dual state machine to cope with dedicated BL and WL control logic.

control logic block independently adjust WL and BL voltages. As shown in Fig. 9(b), WL voltage can be changed before t_1 to maximize WL setup time. However, t_{12} should be carefully determined, such that earlier WL change does not introduce any logical operation error for page buffer. At the same time, page buffer control logics are finely tuned to maximize pagebuffer and BL operations that are independent from WL's characteristics. Consequently, it is possible to optimize their respective WL and BL timings for their respective WL's characteristics.

IV. CELL VT DISTRIBUTION

A planar TLC device necessitates complex reprogram scheme to compensate cell-to-cell interference [5]. Each WL needs to be programmed by applying three separate steps for program. Instead of floating gate for a planar device, VNAND employs atomic level of charge-trap layer, which exhibits negligible capacitance between the adjacent cells. Therefore, cell V_t distribution is well maintained even after the adjacent WLs are programmed.

Fig. 11 compares cell V_t distribution of planar device versus this paper. The planar TLC is using three-step program scheme to minimize V_t distribution, where this paper is using single-step program. As can be seen in the figure, V_t distribution of this paper exceeds planar TLC's raw BER performance. In general, cell V_t of erase state is vulnerable to FN stress

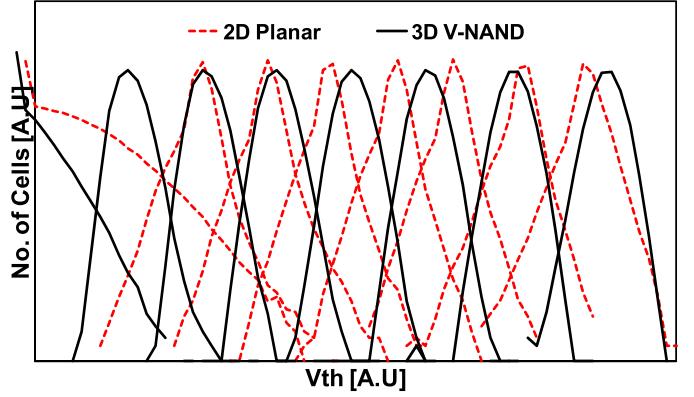
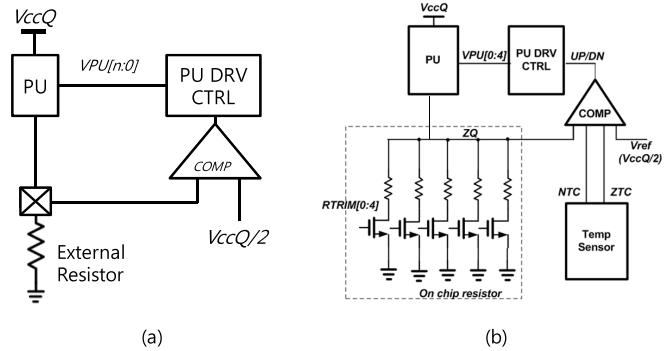
Fig. 11. Cell V_t measurement.

Fig. 12. (a) ZQ calibration concept. (b) On-chip ZA calibration circuit.

by program and read operations. However, in this paper, disturbance for the erase state is well suppressed, because cells struggle less number of program pulses than planar devices. Consequently, VNAND structure maximizes cell V_t window, thereby extending cell's reliability.

V. IO PERFORMANCE

It is critical to minimize the number of components and to maximize IO speed for mobile applications. IO speed requirement is very strict, because it is vital to have a good read and program throughput. To guarantee eye window at maximum frequency, each DQ driver needs to have uniform strength. Fig. 12(a) shows an example of DQ driver for pull-up. As shown in the figure, it is common to place an external resistor in PCB to adjust the strength in the actual environment to maximize frequency even though it is sacrificing area.

In this work, to minimize the number of external components, on-chip resistor is embedded to provide IO strength uniformity without any external component. In Fig. 12(b), when we set a certain value for V_{PUPU}, pull-up driver will supply current to ZQ node to generate a voltage that is proportional to RTRIM. When the voltage at ZQ and reference voltage comparison is completed, the result is reflected to driver controller by adjusting UP/DN signal. This procedure is continued until ZQ node voltage reaches to the V_{ref}.

Here, it is crucial to maintain a constant value for RTRIM and to keep comparator's characteristics across the operating temperature. However, it is impossible to have identical resistance for the resistor against temperature variation. Therefore, an additional temperature sensing circuit was designed to

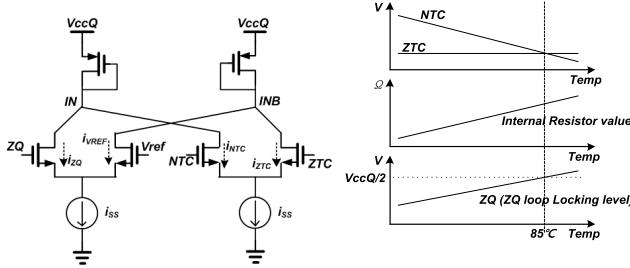


Fig. 13. Temperature compensation circuit for on-chip ZQ calibration.

TABLE I
COMPARISON WITH PREVIOUS WORK

	ISSCC 2015	ISSCC 2016
Bits per cell	3	3
Density	128Gb	256Gb
Chip Size	68.9mm ²	97.6mm ²
Technology	3D NAND 32 stacked WL	3D NAND 48 stacked WL
Organization	16 KB/Page 384 Pages/Block 2732 Blocks/Die	16 KB/Page 576 Pages/Block 3776 Blocks/Die
I/O Bandwidth	Max. 1Gb/s	Max. 1Gb/s
tBERS	3.5ms (Typ.)	3.5ms (Typ.)
tPROG	700us	660us
tR (4KB)	45us	45us

compensate temperature variation of the resistor, as shown in Fig 13. In the temperature sensor, an analog mixer with pMOS load is taking two identical tail currents for its differential pairs. The signal NTC is inversely proportional to the temperature, and ZTC is keeping identical value across the temperature. Once the on-chip resistance is finely tuned during the die sorting process, comparator's sensing level is adapted for resistance variation against temperature by regulating (ZTC-NTC) value as input offset for the comparator in Fig. 12(b).

VI. CONCLUSION

The 256 Gb TLC VNAND flash memory, which is fabricated using the 48 stacked WL process, is presented. In 97.6 mm² of the die size, bit density per area is maximized by doubling capacity, which results in more than 40% gain when compared to the previous work [3]. Write throughput is up to 53.3 MB/s and read throughput reaches up to 178 MB/s. To suppress WL-to-WL coupling due to height scale down, the reverse read scheme is proposed. A variable-pulse scheme is proposed to cope with WL loading variation. Also, to optimize the performance for each WL's characteristic, dual state machine is proposed to independently adjust WL and BL control. An on-chip ZQ calibration scheme is implemented to support high speed IO operation with minimal external component. Table I summarizes the key features of this paper.

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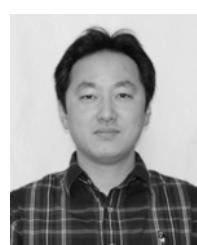
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Dr. Park received several achievement awards from Samsung for his outstanding work.



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He joined Samsung Electronics Company Ltd., Hwaseong, South Korea, in 1999, where he has been leading NAND flash memory design over 15 years. He had been a Team Leader of various world first commercialized NAND products, such as 0.12 μ m 1 Gb, 90 nm 2 Gb, 63 nm 8 G, 51 nm 16 G, 32 nm 32 G, 35 nm, and 41 nm 32 G and successfully commercialized the 2 bit and 3 bit NAND Flash Memory products. He has played an active role in advancing the design of 3-D NAND product using vertical channel structure and the core algorithm for next generation non-volatile memory device. He is currently a Master in Memory Division of Samsung. He holds over 40 papers and over 130 patents related to memory technology. He has served as a Memory Subcommittee Member of the International Solid-State Circuits Conference, and a Co-Operative Board Member of The Institute of Electronics and Information Engineers, South Korea.



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