A 5.6 ppm/°C Temperature Coefficient, 87-dB PSRR, Sub-1-V Voltage Reference in 65-nm CMOS Exploiting the Zero-Temperature-Coefficient Point

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***Abstract*— This paper describes an MOSFET-only voltage reference realized in 65-nm CMOS featuring a temperature coefficient (TC) of 5.6 ppm/°C from −40 °C to 125 °C, a power supply rejection ratio of 87 dB from dc up to 800 kHz (and 75 dB at 1 MHz), a minimum supply voltage of 0.8 V, and a power dissipation of 13 μW. These attributes are achieved by exploiting the zero-TC point of an MOSFET and combining it with a novel curvature-compensation technique, an active attenuator, and an impedance-adapting frequency compensation scheme.**

***Index Terms*— Curvature compensation, high-precision, MOSFET-only, sub-1-V, system-on-chip, voltage reference, wide-band high power supply rejection ratio (PSRR), zero-temperature-coefficient (ZTC) point.**

I. Introduction

IN COMPLEX systems-on-chip, temperature-stable and power-supply insensitive voltage references are required to cope with the presence of large thermal gradients [1], [2], as well as the noisy on-chip environment. Such voltage references must also operate at a low voltage (e.g., sub-1 V) to accommodate technology scaling which exacerbates the design challenges due to the inferior transistor characteristics in advanced CMOS technology nodes [3], [4].

Bandgap references [5]–[11], typically realized by the parasitic vertical p-n-p BJTs in CMOS, are presently the most ubiquitous voltage references, in part for their small output spread, V_{REF} spread, over PVT variations. The design art of bandgap references is mature, particularly in mature technology nodes where they in general require relatively high supply voltage (e.g., $V_{\mathrm{DD}} > 1$ V) due to the nonscalable BJT turn-on voltage. A recently reported bandgap reference achieves a sub-1-V operation by means of a locally boosted supply [12]. Also, in view of deteriorated BJT characteristics (e.g., reduced current gain and increased current gain spread) in advanced technology nodes, the said advantages of bandgap voltage references somewhat diminish with technology scaling [3], [7], [13].

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MOSFET-only voltage references [14]–[22] are an alternative, particularly in sub-1-V applications. Many MOSFET-only voltage references rely on the subthreshold MOSFET [14]–[20], which exhibits similar temperature behavior as the BJT, and feature ultra-low-power (e.g., nanowatt) operation. However, most nanowatt subthreshold voltage references only operate reliably over a limited temperature range. This is because the junction leakage current may severely affect the said subthreshold characteristics [23]. As a result, higher power dissipation is required to achieve wide temperature operation and low temperature coefficient (TC) [19], [20].

The zero-TC (ZTC) voltage reference [22] exploits the ZTC point of an MOSFET in the suprathreshold region. Hence, its characteristics are largely unaffected by junction leakage current. Consequently, the ZTC voltage reference is potentially advantageous over its subthreshold counterparts to achieve a wide temperature range and reliable/predictable performance. Nevertheless, the design art of the ZTC approach for MOSFET-only voltage references remains immature in the sense that their performance is largely inferior to the well-established bandgap and subthreshold approaches.

In this paper, we propose a sub-1-V ZTC voltage reference embodying a curvature compensation technique which achieves a low TC of 5.6 ppm/°C (3.2–9.8 ppm/°C, 50 samples) over a wide temperature range of −40 °C–125 °C. Furthermore, our proposed voltage reference exhibits a high power supply rejection ratio (PSRR) over a wide frequency range: 87 dB from dc to 800 kHz, and 75 dB at 1 MHz. We achieve these attributes by the following methods. First, the curvature compensation and its ensuing low TC are achieved from our investigation into a secondary mechanism of the ZTC point, and utilizing the drain-to-source voltage (V_{ds}) of the MOSFET—a previously unexploited parameter that can minimize the ZTC point temperature sensitivity. Second, the high PSRR is attributed to our active attenuator and impedance adapting compensation, which, respectively, improves the PSRR at low and high frequencies. The shortcomings of our design and mitigation means are also described.

This paper is organized as follows. Section II describes the fundamentals of the ZTC point, and our investigation into V_{ds} on the ZTC point accuracy. Section III describes the modus

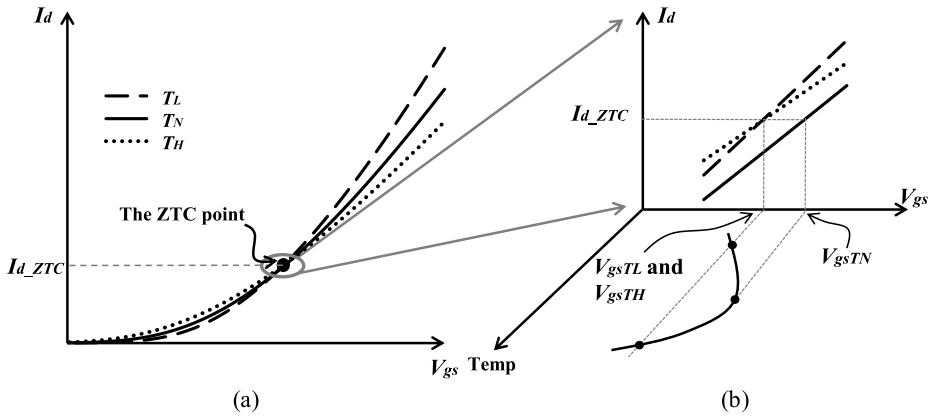

Fig. 1. (a) ZTC point of an nMOS. (b) Temperature sensitive ZTC point.

operandi of our voltage reference, including PSRR, noise and process variations. Section IV presents the measurements and benchmarking. Section V provides the conclusions.

II. Mechanisms of the ZTC Approach

In this section, we will investigate and derive the primary and secondary mechanisms of the ZTC point, and thereafter describe the pertinent parameters that can be effectively exploited to reduce the temperature sensitivity of the ZTC point.

The primary mechanism of the ZTC point [22] is the mutual compensation of temperature effects on threshold voltage, $V_{\rm th}$, and carrier mobility, μ. Fig. 1(a) shows the simulated drain-current (I_d) versus gate-to-source voltage ($V_{\rm gs}$) of an nMOS for three temperatures ($T_L < T_N < T_H$, where T_L, T_N, and T_H are low, nominal, and high temperature, respectively). Ideally, all three curves intersect at the same point, the ZTC point. However, as observed from Fig. 1(b), the three curves do not intersect at the same point in practice. For the sake of unambiguous definition, we define the ZTC point of the nMOS as a group of points with the same I_d but with different $V_{\rm gs}$ values at different temperatures; in Fig. 1(b), $V_{\rm gsTL}$, $V_{\rm gsTN}$, and $V_{\rm gsTH}$ are the corresponding $V_{\rm gs}$ at T_L, T_N, and T_H, respectively. Specifically, I_{d_ZTC} is the current at the intersection of the I_d–$V_{\rm gs}$ curves with T_L and T_H. Put simply, the ZTC point is temperature-sensitive, qualified by the temperature sensitivity of $V_{\rm gs}$. We will now show that the temperature-sensitive ZTC point ($V_{\rm gs\_ZTC}$) is largely due to the secondary effect of mismatch between the mobility temperature exponent and the velocity saturation index.

On the basis of the established α-power model [24], we derive $V_{\rm gs\_ZTC}$ (see the Appendix) and $dV_{\rm gs\_ZTC}/dT$

$$V_{\rm gs\_ZTC} = V_{\rm th0} - \eta T + \frac{\alpha\eta T_0}{\beta}\left(\frac{T}{T_0}\right)^{\frac{\beta}{\alpha}} \tag{1}$$

$$\frac{dV_{\rm gs\_ZTC}}{dT} = -\eta + \eta\left(\frac{T}{T_0}\right)^{\left(\frac{\beta}{\alpha}-1\right)} \tag{2}$$

where $V_{\rm th0}$ is $V_{\rm th}$ extrapolated at 0 K and is temperature independent; η ($\eta > 0$) is the TC of $V_{\rm th}$ [22]; α is the velocity saturation index [24], where on the basis of the α power model, $I_d \propto (V_{\rm gs} - V_{\rm th})^{\alpha}$; β is the temperature exponent of μ [22], where $\mu \propto T^{-\beta}$; and T_0 is the temperature where $dV_{\rm gs}/dT = 0$.

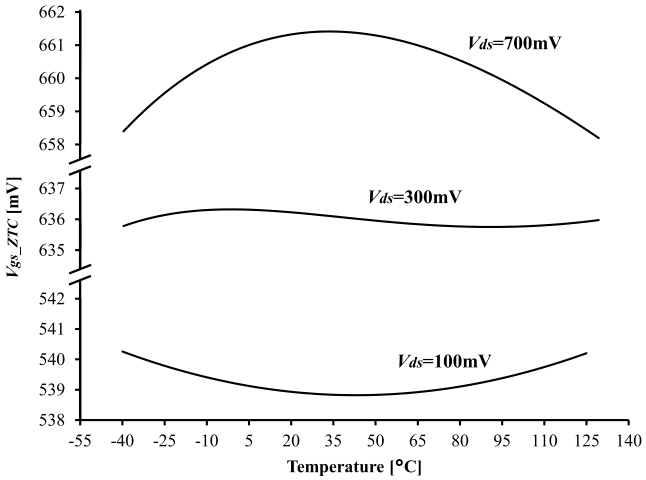

Fig. 2. Simulated $V_{\rm gs\_ZTC}$ when $V_{\rm ds} = 100$, 300, and 700 mV.

On the basis of (1) and (2), the ideal ZTC point ($dV_{\rm gs\_ZTC}/dT \equiv 0$) exists only if $\beta = \alpha$. However, $\beta \neq \alpha$ in practice because β is largely a constant equal to 1.5, whereas α is a variable whose value is between 1 and 2, depending on the operation region of the nMOS. Specifically, $\alpha \approx 1$ and $\alpha \approx 2$ when the nMOS is in the triode and saturation region, respectively. To depict the effect of the unequal β and α, we derive the second-order derivative of $V_{\rm gs\_ZTC}$ over T as

$$\frac{d^2V_{\rm gs}}{dT^2} = \left(\frac{\beta}{\alpha} - 1\right)\eta T_0^{\left(\frac{\beta}{\alpha}-1\right)} T^{\left(\frac{\beta}{\alpha}-2\right)}. \tag{3}$$

Equation (3) depicts that when $\alpha < \beta$, $d^2V_{\rm gs\_ZTC}/dT^2 > 0$, and that there is a local minimum. On the other hand, when $\alpha > \beta$, $d^2V_{\rm gs\_ZTC}/dT^2 < 0$, and there is a local maximum.

Fig. 2 shows the simulated $V_{\rm gs\_ZTC}$ against T for a low $V_{\rm ds}$ of 100 mV, a high $V_{\rm ds}$ of 700 mV, and a medium $V_{\rm ds}$ of 300 mV. For the low $V_{\rm ds}$ = 100 mV, where the nMOS is in triode region, we obtain $\alpha < \beta$ and as expected,

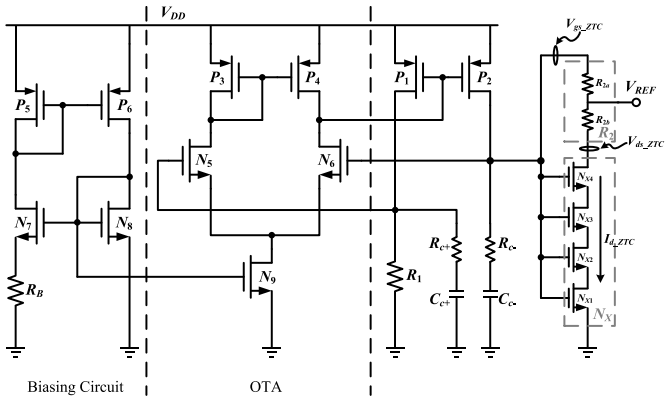

Fig. 3. Schematic of the proposed voltage reference.

$V_{\text{gs\_ZTC}}$ is a convex curve with a local minimum, where the TC is 20 ppm/°C. Conversely, for the high $V_{\text{ds}} = 700$ mV, where the nMOS is in saturation region, we obtain $\alpha > \beta$ and as expected, $V_{\text{gs\_ZTC}}$ is a concave curve with a local maximum, where the TC is 26 ppm/°C. It is interesting to note that when V_{ds} is the medium voltage of 300 mV, the $V_{\text{gs\_ZTC}}$ curve exhibits a concave–convex idiosyncrasy: concave at low T and convex at high T. This is not unexpected because at low T where V_{th} is high, $V_{\text{ds}} = 300$ mV is considered as a relatively high voltage ($V_{\text{ds}} > V_{\text{gs}} - V_{\text{th}}$) such that the nMOS is in the saturation region. Conversely, at high T, where V_{th} is low, $V_{\text{ds}} = 300$ mV is considered as a relatively low voltage ($V_{\text{ds}} < V_{\text{gs}} - V_{\text{th}}$) such that the nMOS is in the triode region. The characteristics of $V_{\text{gs\_ZTC}}$ are somewhat akin to V_{REF} in curvature compensation bandgap voltage references. On the basis of simulation results, when $V_{\text{ds}} = 300$ mV, the TC of the curvature-compensated $V_{\text{gs\_ZTC}}$ can be very low, e.g., ∼5 ppm/°C. This is approximately five times lower than when the nMOS is in the saturation region (e.g., $V_{\text{ds}} = 700$ mV) such as that employed in a reported ZTC voltage reference [22].

In summary, there exists an optimized V_{ds}, i.e., $V_{\text{ds\_ZTC}}$, where the ZTC point temperature sensitivity is minimized. At this optimized point, the nMOS is in the saturation region ($\alpha > \beta$) at low temperature and in the triode region ($\alpha < \beta$) at high temperature. In this fashion, the undesired mismatch between the mobility temperature exponent and the velocity saturation index is largely compensated over the entire temperature range, thereby minimizing the temperature sensitivity of the nMOS ZTC point. Put simply, by means of $V_{\text{ds\_ZTC}}$, a curvature-compensated $V_{\text{gs\_ZTC}}$ can be obtained.

III. Proposed ZTC Voltage Reference

In this section, we will first describe the realization of our proposed ZTC voltage reference embodying $V_{\text{ds\_ZTC}}$ and featuring a very low TC attribute. Subsequently, we will discuss our design considerations in terms of PSRR, noise, and process variations.

A. ZTC Voltage Reference Design

Fig. 3 shows the schematic of our proposed voltage reference, wherein an nMOS (N_X comprising the four stacked nMOS, N_{X1}–N_{X4}) is biased at its ZTC point ($V_{\text{gs\_ZTC}}$, I_{d_ZTC}, and $V_{\text{ds\_ZTC}}$). Table I provides the transistor sizes and resistor and capacitor values.

TABLE I

Transistor Sizes and Resistor and Capacitor Values of the Proposed Voltage Reference

Component	Parameter	Component	Parameter
N_{X1}∼N_{X4}	W=4μm, L=4μm	R_1	112kΩ
N_5, N_6	W=16μm, L=2μm	R_{2a}	37kΩ
N_7	W=4μm, L=4μm	R_{2b}	20kΩ
N_8	W=16μm, L=4μm	R_b	110kΩ
N_9	W=32μm, L=4μm	R_{C+}	30kΩ
P_1, P_2	W=16μm, L=2μm	R_{C-}	10kΩ
P_3, P_4	W=16μm, L=4μm	C_{C+}	2.4pF
P_5, P_6	W=2μm, L=1μm	C_{C-}	7.2pF

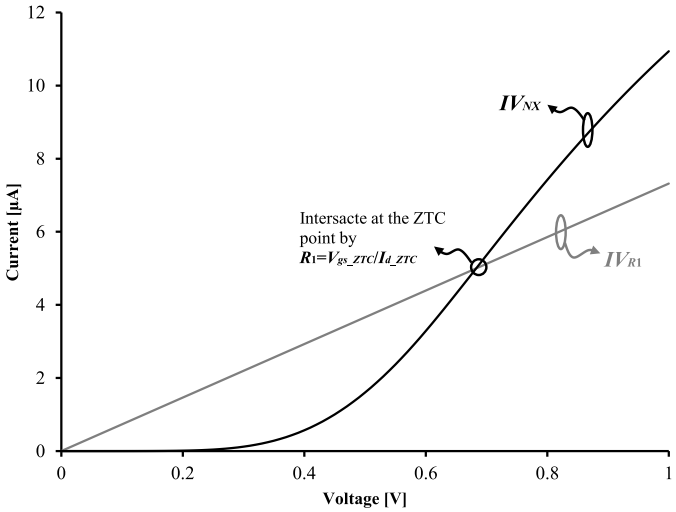

Fig. 4. Characteristic curves of R_1 and N_X.

The precise ZTC point is achieved by three means. First, N_X is biased at its ZTC point by appropriately designing R_1. Fig. 4 shows the characteristic curves of N_X and R_1, denoted as IV_{NX} and IV_{R1}, respectively. The intersection of these two curves is the designated bias point of R_1 and N_X, because R_1 and N_X are biased to the same operating point by the OTA ($N_4 - N_6$, P_3, and P_4) and the current mirror (P_1 and P_2). Hence, the ZTC point of N_X can be obtained by

$$R_1 = V_{\text{gs\_ZTC}}/I_{d\_\text{ZTC}}. \tag{4}$$

$V_{\text{gs\_ZTC}}$ and I_{d_ZTC} are precharacterized by simulations, and in practice, $V_{\text{gs\_ZTC}}$ and I_{d_ZTC} may deviate due to process variations. Nevertheless, the said deviation can be easily mitigated by trimming R_1 as part of a single element trimming for two (extreme) temperatures; see Section III-C.

Second, the ZTC point temperature sensitivity is further minimized by appropriately designing R_2. From Fig. 3, the ZTC point of N_X is optimized by

$$R_2 = (V_{\text{gs\_ZTC}} - V_{\text{ds\_ZTC}})/I_{d\_\text{ZTC}}. \tag{5}$$

As in the case of $V_{\text{gs\_ZTC}}$ and I_{d_ZTC}, $V_{\text{ds\_ZTC}}$ is precharacterized from simulations, and it is similarly somewhat sensitive

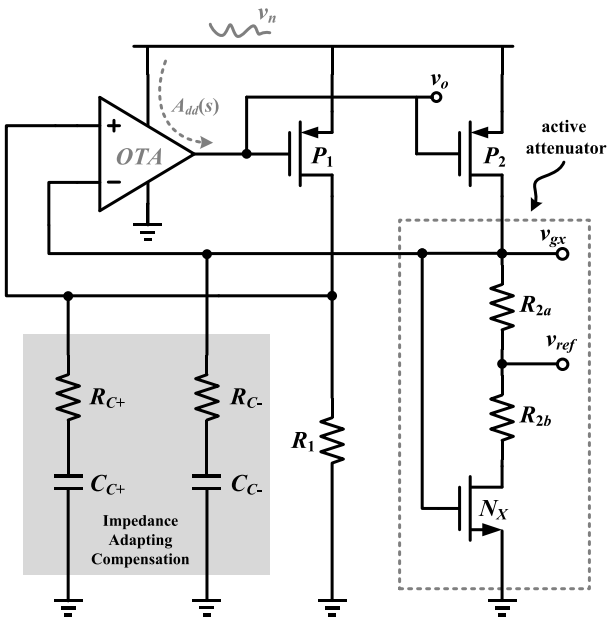

Fig. 5. Simplified schematic of the proposed voltage reference.

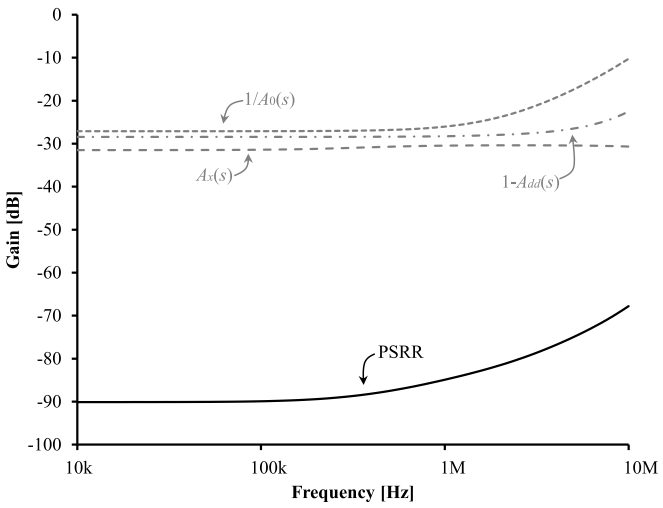

Fig. 6. Simulated PSRR and its components.

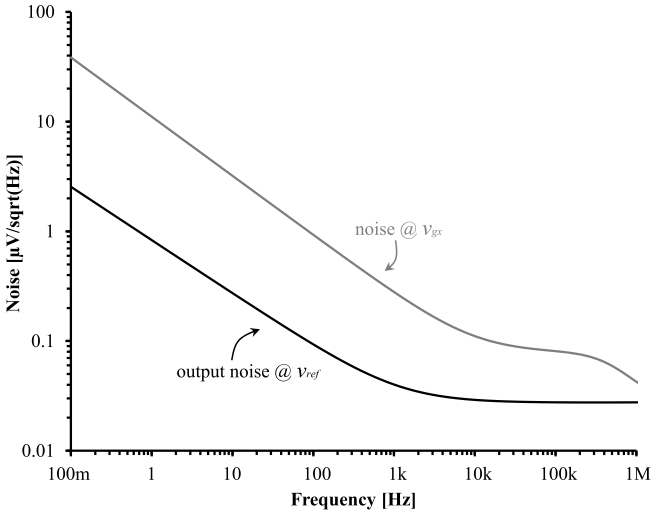

Fig. 7. Simulated noise at $v_{\rm ref}$ and $v_{\rm gx}$.

to process variations. We will show later that the process variation of $V_{\rm ds\_ZTC}$ can be easily mitigated by our proposed trimming circuit.

Third, the PSRR of $V_{\rm REF}$ is optimized by realizing R_2 by two serial resistors, $R_{2\rm a}$ and $R_{2\rm b}$, and by designing $R_{2\rm a} = 1/g_{m\_NX}$ (see later in Section B). On this basis, $V_{\rm REF}$ is expressed as a weighted ZTC voltage:

$$V_{\rm REF} = V_{\rm gs\_ZTC}(1 - R_{2a}/R_1). \tag{6}$$

In summary, our proposed voltage reference generates $V_{\rm REF}$ on the basis of exploiting the ZTC point of N_X, and the low TC attribute of $V_{\rm REF}$ is achieved by means of a previously "unused" $V_{\rm ds\_ZTC}$ which minimizes the temperature sensitivity of N_X ZTC point. In addition to the low TC, our proposed voltage reference also offers high PSRR at both low frequencies and high frequencies and low output noise. The design considerations leading to these two latter attributes will now be described.

B. PSRR and Output Noise

Fig. 5 shows the simplified schematic of our proposed voltage reference that embodies an active attenuator (enclosed within the dashed box), somewhat akin to the peaking current source [25].

The PSRR of $v_{\rm ref}$ can be obtained from the following two equations:

$$v_o = A_{dd}(s)v_n + A_0(s)g_{mp}(Z^+ - Z^-)(v_n - v_o) \tag{7}$$

$$v_{\rm ref} = A_x(s)g_{mp}Z^-(v_n - v_o). \tag{8}$$

Consequently, PSRR is expressed as

$$\text{PSRR} = \frac{v_{\rm ref}}{v_n} = \frac{Z^-}{Z^+ - Z^-} \times \frac{(1 - A_{dd}(s))A_x(s)}{A_0(s)} \tag{9}$$

where v_n is the supply noise; v_o is the small signal voltage at the output of the OTA; $A_{\rm dd}(s) = v_o/v_n$ is the gain from the power supply to the OTA output, and it is largely a constant over a wide frequency range [26]; $A_x(s) = v_{\rm ref}/v_{\rm gx}$ is the gain of the proposed active attenuator; $v_{gx}$is the small signal voltage at the gate of N_X; Z^+ and Z^- are impedance at the positive and negative inputs of the OTA, respectively; $A_0(s) = A_0/(1 + s/\omega_{p0})$ is the gain of the OTA; A_0 is the dc gain of the OTA; and ω_{p0} is the pole frequency of the OTA output.

In view of (9), the mechanisms affecting the PSRR of $v_{\rm ref}$ are $(1 - A_{\rm dd}(s))$, $A_x(s)$, and $1/A_0(s)$. Furthermore, as $(1 - A_{dd}(s))$ and $A_x(s)$ are largely a constant over a wide frequency range, the degradation of the PSRR at high frequencies is largely ascertained by ω_{p0}.

Fig. 6 shows the simulated PSRR, $(1 - A_{\rm dd}(s))$, $A_x(s)$, and $1/A_0(s)$. On the basis of the simulation results, our proposed active attenuator boosts the PSRR by ~30 dB. Note that as A_x(s) of the proposed active attenuator can be expressed as $(1 - g_{m\_\rm NX}R_{2a})$, the PSRR can be improved by setting $R_{2a} \approx 1/g_{m\_\rm NX}$, where $A_x(s) \approx 0$. The PSRR degrades beyond ~1 MHz, which is largely equivalent to the pole

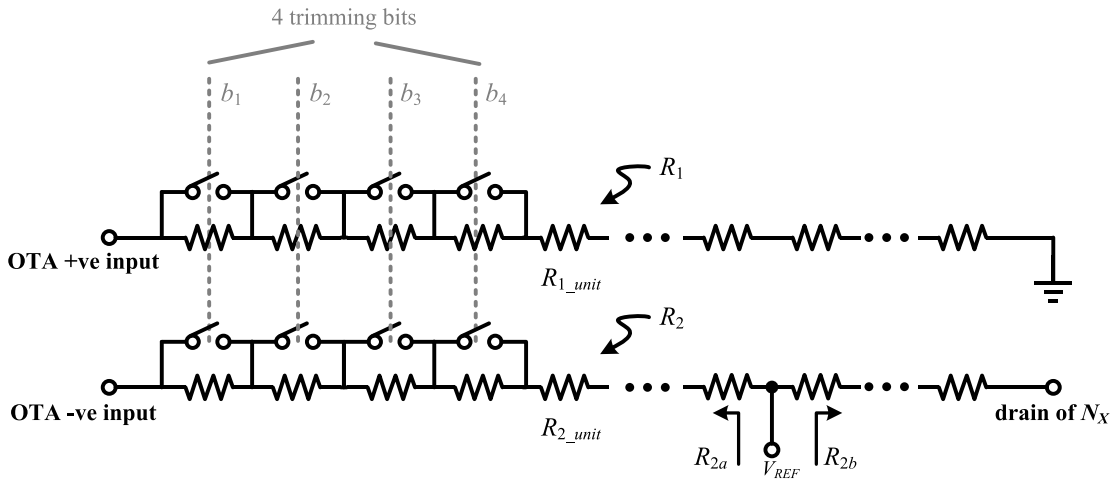

Fig. 8. Trimming circuit of the proposed voltage reference.

frequency of $A_0(s)$. Note that the pole frequency of $A_0(s)$ is ascertained by the frequency compensation employed to stabilize the circuit. We will now discuss the frequency compensation of our voltage reference.

The stability of our proposed voltage reference is achieved in two ways. First, in terms of feedback, our proposed voltage reference comprises two feedback loops—the negative feedback loop formed by the OTA, P_1, and R_1; and the positive feedback loop formed by the OTA, P_2, and N_X. Stability is ascertained by designing the negative feedback loop to be "stronger" than the positive feedback loop.

Second, there are two adjacent poles in each feedback loop. The poles at the output and input of the OTA (realized by $N_4 - N_6$, P_3, and P_4) are $\omega_{p0} = \sim$1 MHz and $\omega_{\rm p1} = \sim$8 MHz, respectively. To provide for stability, a frequency compensation circuit is required. Specifically, we adopt the impedance adapting compensation [27] (see Fig. 5) to introduce a left-hand-plane zero to neutralize the effect of ω_{p0}. The adopted compensation approach is advantageous over the conventional Miller compensation, because it does not shift ω_{p0} to an undesirably low frequency, thereby maintaining ω_{p0} at high ($\sim$1 MHz) frequency and achieving a high PSRR at high frequencies. Furthermore, it is worthwhile to note that the proposed active attenuator isolates $v_{\rm ref}$ node from the feedback loop. Consequently, the proposed voltage reference can accommodate a relatively large range of capacitive loading (up to 1 nF) without affecting stability. Note that the proposed voltage reference is unable to drive a resistive load, because the resistive load would affect the bias point of N_X.

In addition to boosting PSRR, the proposed active attenuator reduces the output noise. This is because noise transmitted from the gate of N_X ($v_{\rm gx}$) to the output ($v_{\rm ref}$) is significantly suppressed by the proposed active attenuator. Consequently, the output noise at $v_{\rm ref}$ is largely contributed by N_X and R_2.

Fig. 7 shows the simulated noise at $v_{\rm gx}$ and $v_{\rm ref}$, without a filtering capacitor. As expected, the output noise at $v_{\rm ref}$ is more than greater than ten times smaller than the noise at $v_{\rm gx}$. Specifically, the flicker noise corner is at $\sim$2 kHz and the thermal noise density at $v_{\rm ref}$ is 27 nV/Hz$^{1/2}$; this noise density is comparable to reported low-noise voltage references [5], [11]. Nevertheless, the flicker noise corner frequency is higher than the reported low-noise bandgap reference ($\sim$20 Hz) [11]. This is expected because the flicker noise of an MOSFET is much larger than a BJT with the same size and bias current [11].

In summary, our proposed voltage reference achieves wideband high-PSRR despite the challenges posed by technology scaling, including reduced transistor intrinsic gain and limited supply voltage. The high PSRR at low and high frequencies is achieved by the active attenuator and the impedance adapting compensation, respectively, largely without power dissipation penalty. Our proposed voltage reference also features relatively low thermal noise, and is attributed to the proposed active attenuator.

C. Process Variations

Like most MOSFET-only voltage references, the proposed voltage reference is sensitive to process variations, because the ZTC voltage of an MOSFET is fundamentally process-sensitive. Furthermore, the operating point of N_X may deviate from the desired ZTC point due to process variations. Consequently, process variations result in undesired $V_{\rm REF}$ spread, and a deteriorated TC and TC spread. To mitigate $V_{\rm th}$ spread (and other process variations), a large effective gate area of N_X was achieved by stacking four identical nMOS (N_{X1}–N_{X4} in Fig. 3) with the maximum L(4 μm) allowed in the process used. In addition, trimming of R_1 and R_2 was adopted to optimize TC and TC spread.

We will now show that trimming R_1 (Figs. 3 and 5) can adjust the bias point of N_X to the desired ZTC point (Fig. 4), and trimming R_2 provides a means to optimize $V_{\rm ds}$ of N_X to the desired $V_{\rm ds\_ZTC}$ [see (5)] to minimize the TC of the ZTC point. Fig. 8 shows the schematic of the trimming circuit, where R_1 and R_2 are realized by connecting the same number of unit resistors ($R_{1\_\rm unit}$ and $R_{2\_\rm unit}$, respectively) in series; and $R_{1\_\rm unit}$ and $R_{2\_\rm unit}$ are ratiometric, where $R_{2\_\rm unit} \approx 0.5R_{1\_\rm unit}$ in the proposed design. Consequent to (4) and (5), $R_2/R_1 = 1 - V_{\rm ds\_ZTC}/V_{\rm gs\_ZTC}$, and is largely a constant despite the

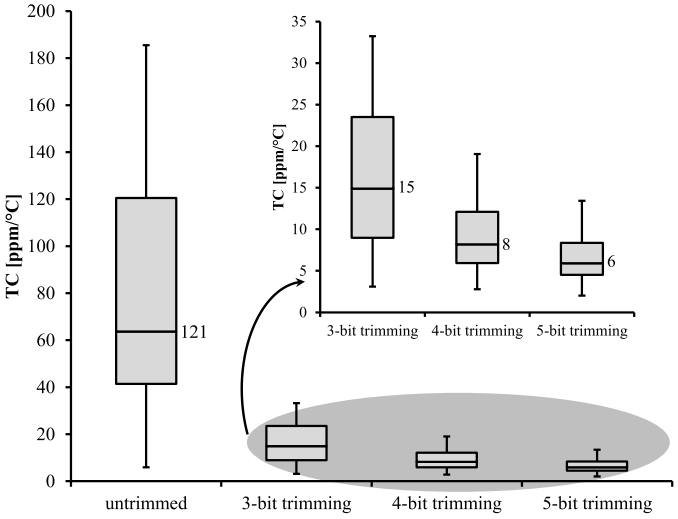

Fig. 9. Statistics of untrimmed TC and trimmed TC from a 200-run Monte-Carlo simulation.

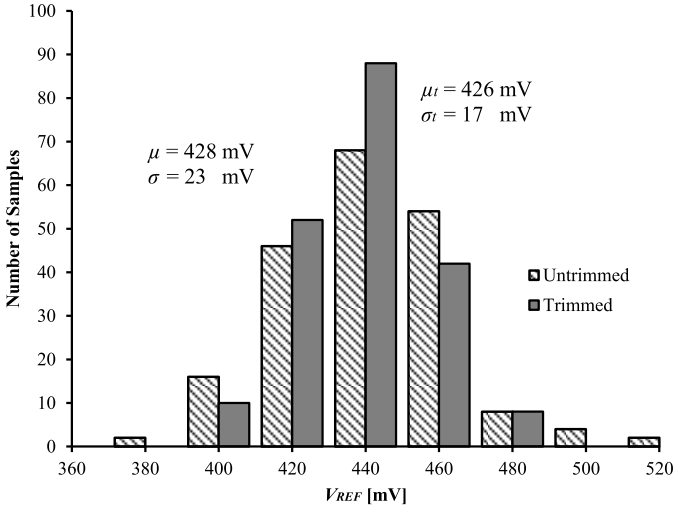

Fig. 11. Statistics of untrimmed and trimmed V_{REF} from a 200-run Monte-Carlo simulation.

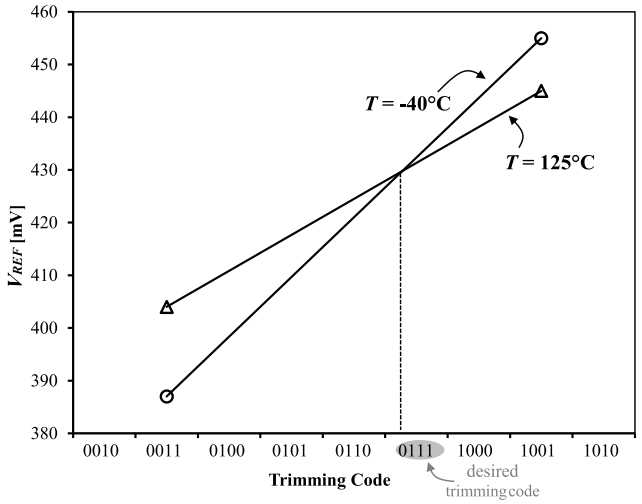

Fig. 10. Trimming process of the proposed voltage reference.

process variations. This is because both $V_{\mathrm{gs\_ZTC}}$ and $V_{\mathrm{ds\_ZTC}}$ vary monotonically with respect to V_{th} variations, the dominant process variation. By exploiting the constant R_2/R_1, we simplify the trimming process by concurrently trimming R_1 and R_2 with four trimming bits ($b_1 - b_4$), i.e., equivalent to one-element trimming.

From a 200-run Monte-Carlo simulation, Fig. 9 shows the box plot of the statistics of untrimmed TC and trimmed TC (including 3-b, 4-b, and 5-b trimmings). It can be seen that the proposed trimming can substantially reduce the TC and the TC spread, and they are reduced by increasing the number of trimming bits. We choose to adopt the 4-b trimming as it is a cogent tradeoff between trimming effectiveness and cost.

Fig. 10 shows the trimming process in the proposed voltage reference. In view of the process-sensitive ZTC voltage, the trimming needs to be performed at two temperatures (e.g., −40 °C and 125 °C) to ascertain the optimum trimming code. At each said temperature, we obtain the plot of V_{REF} versus code by sweeping the trimming code (typically, only two trimming codes are chosen for each temperature). The two plots intersect at a point, and the corresponding code at this intersection point is the desired trimming code ("0111" in Fig. 10), where the TC is minimized. The proposed two-point trimming can ensure a robust low TC by concurrently trimming R_1 and R_2. In the perspective of postmanufacturing calibration, trimming involving two temperatures (vis-à-vis one temperature or no trimming) is undesirable, as this is a cost penalty—a disadvantage of virtually all voltage references embodying curvature compensation (see Table II later).

Fig. 11 shows the statistics of the untrimmed and our trimmed V_{REF} obtained from the said 200-run Monte-Carlo simulation. The variation coefficient of untrimmed V_{REF} (σ/μ) and trimmed V_{REF} (σ_t/μ_t) is 5.5% ($\mu = 428$ mV and $\sigma = 23$ mV) and 4% ($\mu_t = 426$ mV and $\sigma_t = 17$ mV) respectively. The trimmed V_{REF} features smaller spread because the proposed trimming scheme can optimize N_X closer to the ZTC point, independent of geometry mismatch, e.g., mirror mismatch and opamp offset. On the basis of these simulations, we assert that the residual V_{REF} spread after trimming is mainly due to the spread of the ZTC voltage of N_X—this is congruous to the literature depicting the spread of the ZTC voltage in most MOSFET-only voltage references [14], [15], [18]. It is, nevertheless, worthwhile to note from (6) that the V_{REF} spread due to process variations can be further mitigated by an additional trimming of the ratio of R_1 and $R_{2\mathrm{a}}$. This is because V_{REF} is a weighted ZTC voltage. This additional trimming is not adopted in this design because of the associated trimming cost.

IV. Measurement Results

Fig. 12 shows the microphotograph of our proposed voltage reference whose active area is 80 μm × 130 μm realized in a commercial 65-nm bulk CMOS process. 50 samples of our proposed voltage reference are measured.

Fig. 13 shows the measured V_{REF} versus temperature of one of the samples. V_{REF} versus temperature curve depicts the desired curvature compensated characteristics—concave

TABLE II
PERFORMANCE BENCHMARK AGAINST BANDGAP VOLTAGE REFERENCES

		This work	[5]	[6]	[7]	[8]	[9]	[10]
Technology		65nm CMOS	0.6µm CMOS	0.35µm CMOS	0.16µm CMOS	0.35µm CMOS	0.5µm BiCMOS	90nm CMOS
V_{REF}[mV]		428	1142	858	1087	618	1285	720
Temperature Range [°C]		-40 to 125	0 to 100	-20 to 100	-40 to 125	-15 to 150	-40 to 100	0 to 100
Average TC [ppm/°C]		5.6	5.3[a]	12.4	5-12	4.9	7.2	32.6
Curvature Compensation		Yes	Yes	No	Yes	Yes	Yes	Yes
Coefficient of Variation		0.39% (50 samples)	N.A. (1 sample)	0.15% (11 samples)	0.05% (61 samples)	N.A. (5 Samples)	0.01% (5 Samples)	1.3% (5 Samples)
Trimming		2-Temp; 1-Element	2-Temp; 3-Element	1-Temp	1-Temp[b]	Mul Temp; 2-Element	4-Temp; 4-Element	No
PSRR [dB]	10Hz	87	47	68	74	N.A.	70	51
	1MHz	75	10	N.A.	N.A.	N.A.	10	N.A.
Minimum V_{DD}		0.8V	2V	1.4V	1.6V	2.5V	1.6V	1.15V
Power		13µW	46µW	162µW	88µW	95µW	40µW	0.58µW

a. Not average TC; TC obtained from one sample only
b. A chopper requiring an external clock is involved in the design

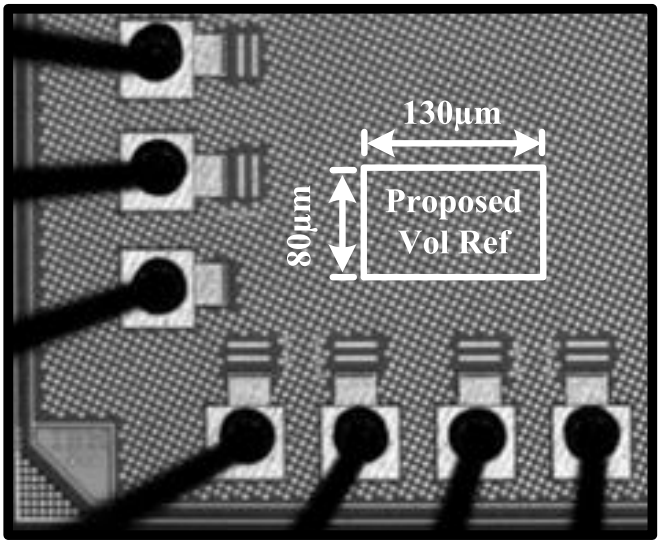

Fig. 12. Microphotograph of the proposed voltage reference.

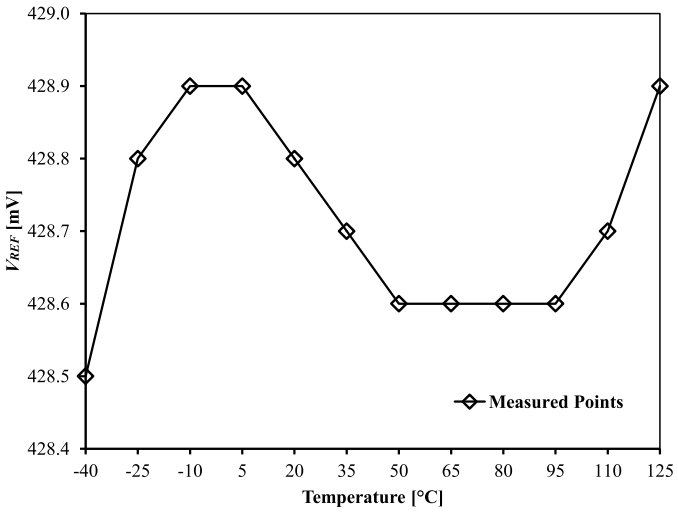

Fig. 13. Measured V_{REF} versus temperature of one sample (trimmed).

at low temperature (−40 °C–35 °C) and convex at high temperature (35 °C–125 °C). The average V_{REF} is 428.7 mV, and V_{REF} features a low TC of 5.6 ppm/°C over a wide temperature range from −40 °C–125 °C. As described in Section II (see Fig. 2), the curvature compensation and the ensuing low TC are attributed to our exploitation of $V_{\mathrm{ds\_ZTC}}$, which minimizes the temperature sensitivity of the ZTC point. The wide temperature range, on the other hand, is attributed to the characteristic of the ZTC point, which is unaffected by the junction leakage current effect.

Fig. 14 shows V_{REF} versus temperature of the 50 measured samples (trimmed) and the measured TC ranges from 3.2 ppm/°C to 9.8 ppm/°C with an average TC of 5.6 ppm/°C. Statistically, our voltage reference exhibits a relatively robust low TC (TC < 10 ppm/°C) after trimming, and all 50 samples depict the desired curvature-compensated attribute. This robustness is attributed to our proposed trimming circuit (see Fig. 8). For completeness, note that the TC of 50 samples ranges from 4.3 ppm/°C to 72.8 ppm/°C before trimming.

Fig. 15 shows the statistics of trimming codes. In the proposed voltage reference, we employ 4-b trimming (16 trimming codes) where 7 out of 16 trimming codes were needed to trim the 50 samples. This is expected because we designed the 4-b trimming based on Monte-Carlo simulations, which may overestimate the process variation of samples fabricated on the same wafer. In the case of samples from different wafers, we expect to use all 16 trimming codes.

TABLE III
PERFORMANCE BENCHMARK AGAINST SUBTHRESHOLD MOSFET-ONLY VOLTAGE REFERENCES

		This work	[14]	[15]	[16]	[17]		[18]
Technology		65nm CMOS	0.35μm CMOS	0.35μm CMOS	0.35μm CMOS	0.13μm CMOS	65nm CMOS	65nm CMOS
V_{REF}[mV]		428	670	858	263	176	328	474
Temperature Range [°C]		-40 to 125	0 to 80	-20 to 80	0 to 125	-20 to 80	-20 to 80	-40 to 90
Average TC [ppm/°C]		5.6	10	15	165	29	89 to 118	40
Curvature Compensation		Yes	No	No	No	No	No	No
Coefficient of Variation		0.39% (50 samples)	3.1% (20 samples)	0.94% (17 samples)	3.9% (40 samples)	0.18% (25 samples)	N.A. (17 samples)	3.4% (15 samples)
Trimming		2-Temp; 1-Element	N.A.	N.A.	N.A.	1-Temp	N.A.	2-Temp; 1-Element
PSRR [dB]	10Hz	87	47	45	45	51	40	40
	1MHz	75	40	N.A.	12	62	N.A.	20
Minimum V_{DD}		0.8V	0.9V	1.4V	0.45V	0.5V	0.5V	0.75V
Power		13μW	36nW	0.3μW	3nW	30pW	240pW	0.3μW

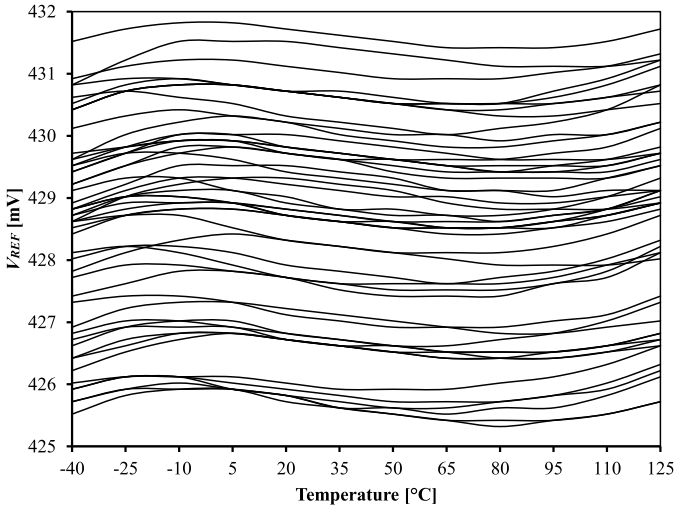

Fig. 14. V_{REF} versus temperature of 50 measured samples (trimmed).

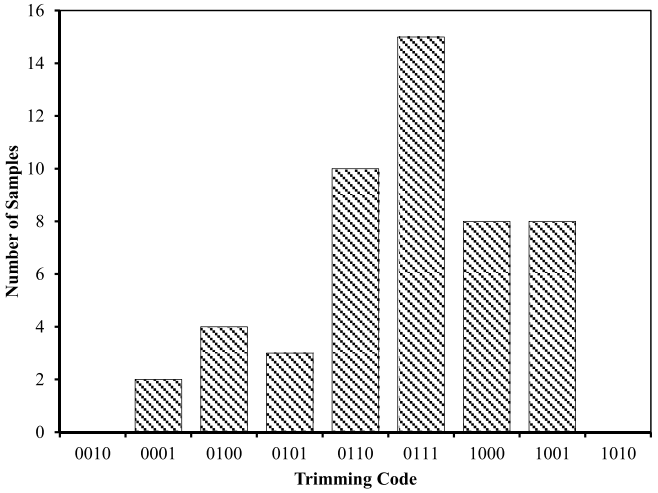

Fig. 15. Statistics of trimming codes.

Fig. 16 shows the statistical measurements (trimmed) of V_{REF} of the 50 samples. The mean (μ) V_{REF} is 428.5 mV, and its standard deviation (σ) is 1.67 mV, i.e., a coefficient of variation σ/μ of 0.4%. The measured σ/μ is substantially lesser than that estimated by Monte-Carlo simulations. This is, as discussed earlier, largely because all the 50 measured samples were fabricated on the same wafer.

Fig. 17 shows the measured PSRR of V_{REF}. Our proposed voltage reference exhibits a high PSRR of 87 dB at low frequency (<800 kHz), and the PSRR degrades beyond 800 kHz. As described earlier, the high PSRR at low frequencies and at relatively high frequencies is achieved, respectively, by means of the active attenuator and the impedance adapting compensation; both techniques do not incur excessive power dissipation penalty. It is worthwhile to note that compared with state-of-the-art CMOS voltage references, our design achieves the highest PSRR (see Tables II and III) at both low frequencies and relatively high frequencies. This is despite the reduced transistor intrinsic gain and the ensuing inadequate circuit loop gain of the 65-nm CMOS process (compared with more dated CMOS processes).

Fig. 18 shows the measured V_{REF} versus V_{DD} from 0.5 to 1.4 V (1.4 V is the maximum supply voltage in 65-nm CMOS process) for three temperatures, −40 °C, 27 °C, and 125 °C. It can be observed that the minimum V_{DD} for our design is ∼0.8 V for all three temperature conditions. This sub-1-V operation can be explained by noting that $V_{\mathrm{DD}} = V_{\mathrm{gs\_ZTC}} + V_{\mathrm{dsP1}}$ (see Fig. 3), where $V_{\mathrm{gs\_ZTC}} \sim 600$ mV (insensitive to temperature variations) and $V_{\mathrm{dsP1}} > 200$ mV for normal operation. Similar to the design mechanism for the realization of high PSRR at low frequencies, the supply insensitive attribute is achieved by the active attenuator.

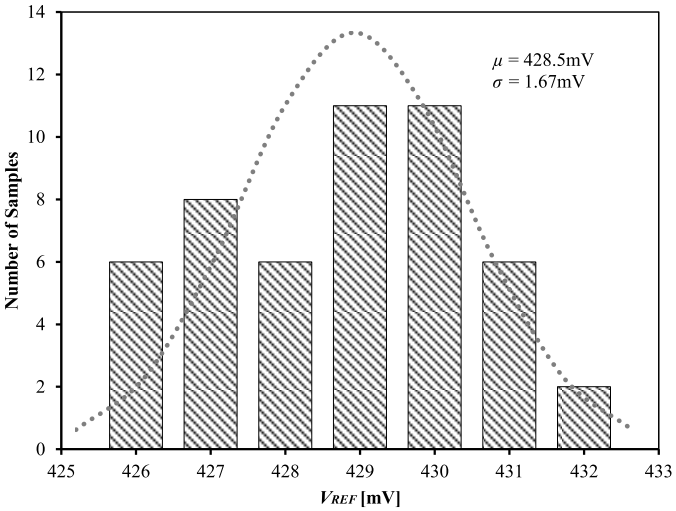

Fig. 16. Statistical measurement results of V_{REF} (trimmed).

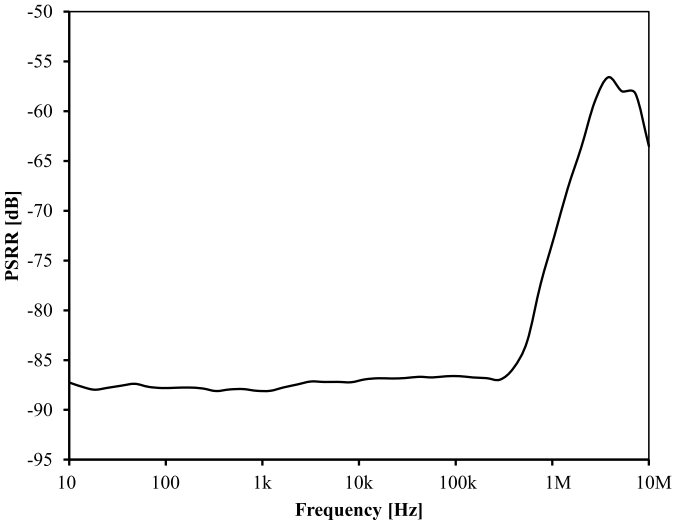

Fig. 17. Measured PSRR of the proposed voltage reference.

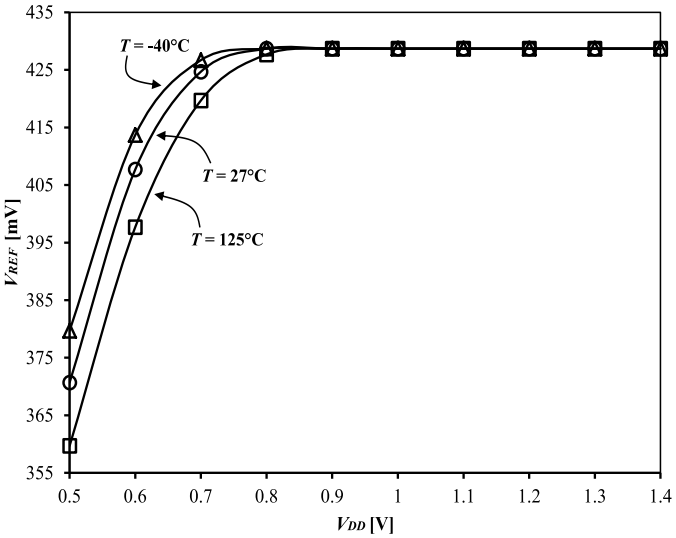

Fig. 18. Measured V_{REF} versus V_{DD}.

From the low frequency PSRR, we estimate that the line sensitivity (the parameter that quantifies V_{REF} sensitivity against supply variations), LS $\approx$ 0.1%/V; the limited resolution of our measurement equipment does not permit a direct LS measurement.

Tables II and III, respectively, benchmarks the performance of our proposed voltage reference against state-of-the-art bandgap references and subthreshold MOSFET-only voltage references. When benchmarked against reported bandgap voltage references (Table II), our proposed voltage reference is advantageous in the following three aspects. First, as expected, our voltage reference features the lowest minimum V_{DD}. Second, despite our proposed voltage reference being realized in the smallest feature-size CMOS process, its average TC (from 50 samples) is the second lowest; the TC [5] is not an average TC as it is based on one sample and the average TC [8] is obtained from only five samples. Third, our proposed design features the highest PSRR both at low and high frequencies. Of specific interest, the PSRR of our design at 10 Hz and 1 MHz is, respectively, a substantial 13 dB and very substantial 60 dB higher than designs that reported their PSRR. The shortcoming of our voltage reference is its relatively high coefficient of variation—the second highest amongst designs with reported coefficient of variation.

When benchmarked against subthreshold MOSFET-only voltage references (Table III), our design is advantageous in three aspects. First, our proposed design features the lowest TC: approximately two times lower than the next best design. Second, the stipulated temperature range of our design is the widest—yet featuring the lowest TC. Of specific interest, for the design with the next lowest TC [14], the stipulated temperature range of our design is a substantial two times wider, i.e., 165 °C vis-à-vis 80 °C. For completeness, it is pertinent to note that in general, the wider the temperature range, the larger is the expected TC—particularly at higher temperatures. As described earlier, this is largely because of the junction leakage current effect. It is worthwhile to note that the junction leakage current effect is not pertinent in our design for reasons already described. Third, our proposed design features the highest PSRR both at low and high frequencies. Of specific interest, the PSRR of our design at 10 Hz and 1 MHz is, respectively, a substantial 36 and 11 dB higher than the design with the next best PSRR. The V_{REF} spread of our design is the second smallest among the reported subthreshold voltage references. The shortcoming of our design over subthreshold designs is, as expected, the higher power dissipation. This is due to the fact that the critical transistors in our design are operated in the suprathreshold region.

V. Conclusion

We have described the design of a sub-1-V MOSFET-only ZTC voltage reference realized in 65-nm bulk-CMOS, featuring operation down to $V_{\mathrm{DD}} = 0.8$ V, $V_{\mathrm{REF}} = 428$ mV, low TC of 5.6 ppm/°C over a wide operating temperature range ranging from −40 °C–125 °C, high PSRR of 87 dB from dc to 800 kHz (75 dB at 1 MHz), a coefficient of variation of 0.39%, and relatively low power dissipation of 13 μW. Our proposed voltage reference achieved these attractive attributes by means of a novel curvature compensation technique and by means of an active attenuator and impedance adapting compensation.

APPENDIX

The derivation of $V_{\mathrm{gs\_ZTC}}(T)$ and $dV_{\mathrm{gs\_ZTC}}/dT$ [i.e., (1) and (2)] are delineated herein.

On the basis of the α-power law, I_d is expressed as

$$I_d = k\mu(T)(V_{\mathrm{gs}}(T) - V_{\mathrm{th}}(T))^{\alpha} \tag{a1}$$

where k is a constant.

As both μ (T) and $V_{\mathrm{th}}(T)$ are temperature dependent, they can, respectively, be expressed as

$$\mu(T) = k_{\mu}T^{-\beta} \tag{a2}$$

and (a2)

$$V_{\mathrm{th}}(T) = V_{\mathrm{th0}} - \eta T \tag{a3}$$

where k_{μ}, V_{th0}, and η are constant.

Hence, by substituting (a2) and (a3) into (a1), dI_d/dT is derived as

$$\begin{aligned}\frac{dI_d}{dT} &= k\left(\frac{d\mu(T)}{dT}\right)(V_{\mathrm{gs}}(T) - V_{\mathrm{th}}(T))^{\alpha} \\ &\quad + \alpha k\mu(T)(V_{\mathrm{gs}}(T) - V_{\mathrm{th}}(T))^{\alpha-1}\left(\frac{dV_{\mathrm{gs}}(T)}{dT} - \frac{dV_{\mathrm{th}}(T)}{dT}\right) \\ &= kk_{\mu}T^{-\beta-1}(V_{\mathrm{gs}}(T) - V_{\mathrm{th}}(T))^{\alpha-1} \\ &\quad \times\left(-\beta(V_{\mathrm{gs}}(T) - V_{\mathrm{th}}(T)) + \alpha T\left(\frac{dV_{\mathrm{gs}}(T)}{dT} + \eta\right)\right). \end{aligned} \tag{a4}$$

At the ZTC point where $I_d = I_{d\_\mathrm{ZTC}}$ is a temperature-independent current (i.e., $dI_{d\_\mathrm{ZTC}}/dT = 0$)

$$\beta(V_{\mathrm{gs\_ZTC}}(T) - V_{\mathrm{th}}(T)) = \alpha T\left(\frac{dV_{\mathrm{gs\_ZTC}}(T)}{dT} + \eta\right). \tag{a5}$$

As $V_{\mathrm{gsTL}} = V_{\mathrm{gsTH}}$, there exists a temperature where $dV_{\mathrm{gs\_ZTC}}(T)/dT = 0$. With a denotation that this temperature is T_0 $(T_L < T_0 < T_H)$

$$\left.\frac{dV_{\mathrm{gs\_ZTC}}(T)}{dT}\right|_{T=T_0} = 0. \tag{a6}$$

By substituting (a6) into (a5), we obtain

$$V_{\mathrm{gs\_ZTC}}(T_0) - V_{\mathrm{th}}(T_0) = \frac{\alpha\eta T_0}{\beta} \tag{a7}$$

and substituting (a7) into (a1), I_{d_ZTC} is expressed as

$$I_{d\_ZTC} = k\mu(T_0)\left(\frac{\alpha\eta T_0}{\beta}\right)^{\alpha} = kk_{\mu}T_0^{-\beta}\left(\frac{\alpha\eta T_0}{\beta}\right)^{\alpha}. \tag{a8}$$

On the basis of (a8), $V_{\mathrm{gs\_ZTC}}(T)$ is expressed as

$$\begin{aligned}V_{\mathrm{gs\_ZTC}}(T) &= V_{\mathrm{th}}(T) + \left(\frac{I_{d\_ZTC}}{kk_{\mu}T^{-\beta}}\right)^{\frac{1}{\alpha}} \\ &= V_{\mathrm{th0}} - \eta T + \frac{\alpha\eta T_0}{\beta}\left(\frac{T}{T_0}\right)^{\frac{\beta}{\alpha}}. \end{aligned} \tag{a9}$$

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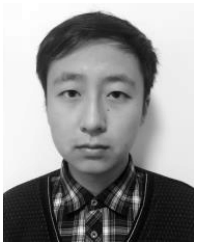

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