

# 8.3 M-Pixel 480-fps Global-Shutter CMOS Image Sensor with Gain-Adaptive Column ADCs and Chip-on-Chip Stacked Integration

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**Abstract**—This paper presents a 4K2K 480-fps global-shutter CMOS image sensor with a super 35-mm format for a highly realistic digital video system. The sensor employs newly developed gain-adaptive column analog-to-digital converters to obtain input-referred dark random noise of  $140 \mu\text{V}_{\text{rms}}$  for an input-referred full-scale readout of 923 mV. An on-chip online correction of the error between two switchable gains maintained the nonlinearity of the output image within 0.18%. A chip-on-chip integration process realized a front-illuminated image sensor stacked with two diced logic chips through 38-K microbump interconnections. The global-shutter pixel achieved a parasitic light sensitivity of  $-99.6 \text{ dB}$ . The 16-channel output interfaces with 4.752 Gbps/ch were implemented in the stacked logic chips.

**Index Terms**—Analog-to-digital converter (ADC), chip-on-chip stacked device, CMOS image sensor, global shutter, high frame rate, low noise.

## I. INTRODUCTION

THE demand for a highly realistic video system for 4 K digital imaging has been increasing. Low-noise and high-bit-resolution analog-to-digital converters (ADCs) are required to capture both highlights and detailed shadows. In addition to image quality, a higher frame rate is desired that can offer slow-motion movies for instant replays in sports broadcasting. High-speed image sensors with large optical formats [1]–[6] suppress the readout noise with a high analog gain; however, they cannot maintain the low noise while receiving the full scale of pixel output. Thus, gain-adaptive, multiple-slope, and multiple-sampling functions were proposed to improve the noise for shadows while capturing unsaturated highlights [7]–[14]. The gain-adaptive functions [7]–[9] employ column-parallel automatic gain control (AGC) preamplifiers to change the gain according to each pixel output. To implement a large number of column-parallel ADCs for the high frame rate at a high pixel resolution, the power consumption overhead and area penalty of column-parallel AGC preamplifiers are

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quite large. Furthermore, the column AGCs make the error correction of column gains complicated. The multiple-slope architecture [10], [11] switches offset slopes according to each pixel output to reduce the conversion time. The number of slopes increases in proportion to the reduction ratio of conversion time. Moreover, it is difficult to precisely calibrate offset errors among multiple slopes, because true correlated double sampling (CDS) cannot be performed for all slope references. The multiple-sampling functions [12]–[14] efficiently reduce the noise level for shadows; nevertheless, it is difficult to achieve the high frame rate because the multiple sampling increases the conversion time in proportion to the number of samplings.

To meet the demands of simultaneously supporting a high frame rate and high dynamic range, we proposed gain-adaptive column ADCs based on a single-slope ADC (SS-ADC) [15]. Instead of a programmable gain amplifier (PGA), we applied two slope references of different gains. The two slope references are switched by the pixel output level in each column. This approach contributes to no additional noise source on the readout chain and small overhead of area and power consumption. The proposed gain-adaptive column ADCs can suppress the sensor nonlinearity by on-chip online gain correction and realize small vertical fixed pattern noise (FPN) with no other calibration.

4 K digital imaging with slow-motion capture for professional applications, such as cinema production and broadcasting, also requires a global-shutter feature to avoid focal plane distortion. Standard CMOS image sensors employ a rolling-shutter exposure on account of the line-by-line readout. However, they cannot avoid the distortion inherent to rolling exposure regardless of the extent to which exposure speed is improved to capture a moving target. The global-shutter feature is strongly demanded, especially for movie cameras that cannot easily mount a mechanical shutter to avoid focal plane distortion.

Global-shutter pixels have been proposed by integrating an in-pixel analog memory. To maintain the compatibility of the image quality with that of standard rolling-shutter pixels, a low-leakage charge-domain analog memory is required [3], [16], [17]. In addition, the analog memory node should be carefully shielded from incident light to suppress parasitic light sensitivity (PLS). Thus, it is difficult to apply the pixel

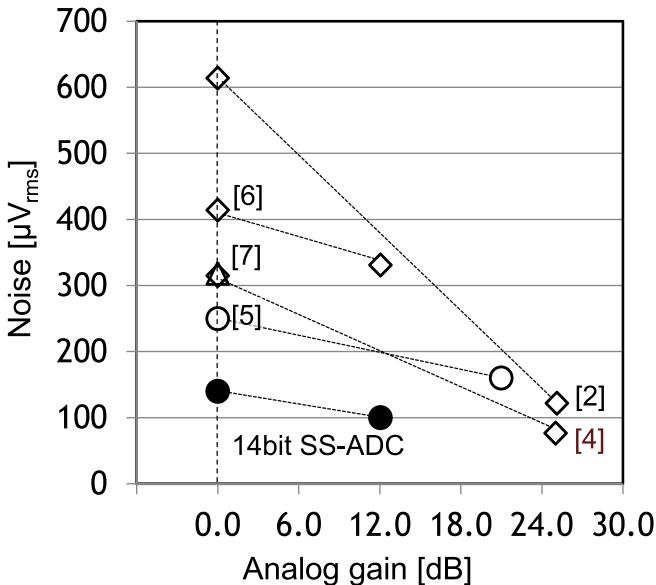


Fig. 1. Relation between analog gain and readout noise.

structure to a back-illuminated stacked device structure, such as in [18], because a light shield layer cannot efficiently cover the memory node. This is otherwise quite useful for achieving the high frame rate by highly parallel ADCs and high-speed clocking circuits. We consequently employed a global-shutter pixel with a charge-domain analog memory and a multiple chip-on-chip integration that realizes a front-illuminated image sensor stacked with two diced logic chips through microbump interconnections [15]. Microbump interconnections have been used to extend the data bandwidth with DRAM [19]. In the present image sensor, the microbump interconnections are used between analog and digital circuit parts of column ADCs to integrate highly parallel high-speed clocking ADCs and high-speed output interfaces with 4.752 Gbps/ch.

In this paper, we describe a CMOS image sensor using gain-adaptive column ADCs and multiple chip-on-chip integration. The gain-adaptive column ADCs efficiently achieve low-noise readout of full well capacity (FWC), even at the high frame operation. The circuit configuration minimizes the overhead of power consumption and the area penalty. The multiple chip-on-chip integration with the microbump interconnection enables a stacked and front-illuminated image sensor, which integrates a global-shutter pixel with low PLS and high-speed clocking circuits. We thus fabricated an 8.3 M-pixel 480-fps global-shutter CMOS image sensor with a super 35-mm optical format.

In the following section, we describe the sensor architecture and circuit configuration. In Section III, we present the device structure and our chip implementation. In Section IV, the performance and measurement results of the fabricated sensor are shown. Finally, conclusions are presented in Section V.

## II. CIRCUIT CONFIGURATION

### A. Concept of Gain-Adaptive Column ADC

To capture both highlights and detailed shadows, low-noise and high-bit resolution ADCs are required. Fig. 1 shows the relation between analog gain and readout noise among

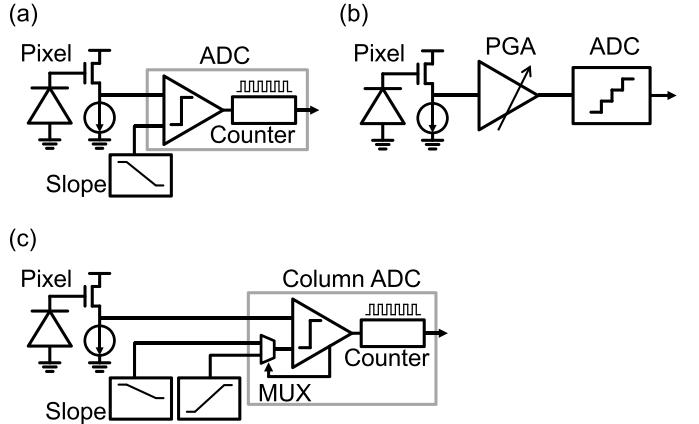


Fig. 2. Block diagram of column-parallel ADCs. (a) Single-slope ADC. (b) Column ADC with a PGA. (c) Proposed gain-adaptive column ADC.

high-speed image sensors with a high pixel resolution [2], [4]–[7]. Successive-approximation-register ADCs [2], [4] and pipeline-cyclic ADCs [6] employ column preamplifiers to suppress the noise of ADC. However, they cannot efficiently reduce the noise at an analog gain of 0 dB, where image sensors offer the maximum dynamic range to avoid clipping highlights. 12-bit SS-ADCs [5] attained better noise performance at the analog gain of 0 dB; moreover, 14-bit SS-ADCs can avoid clipping highlights while retaining detailed shadows. The characteristics of 14-bit SS-ADCs are also plotted in Fig. 1, where the noise level in a 14-bit operation mode with the same architecture of [5] is measured.

SS-ADCs promise the low-noise characteristics even at a gain of 0 dB in a 14-bit operation mode; however, the conversion time becomes longer than that of the 12-bit operation. The 12-bit and 14-bit operations of SS-ADC typically require  $2^{12}$  and  $2^{14}$  counting clocks, respectively. We therefore propose a pixelwise gain-adaptive architecture to reduce the conversion time of 14-bit SS-ADC. Fig. 2(a) depicts a concept diagram of standard SS-ADC. Adaptive gain-control methods using a PGA were presented [7]–[9] to reduce the conversion time of high-bit resolution A/D conversion, as shown in Fig. 2(b). In our proposal, we apply two slope references of different gains instead of the PGAs, as shown in Fig. 2(c). The two references are adaptively switched by the pixel output level in each column. This approach contributes to no additional noise source on the readout chain, while incurring small overhead of area and power consumption.

Two slope references of different gains—high-gain (HG) slope and low-gain (LG) slope—are used to obtain the dark pixel output with low noise and the bright pixel output without clipping, respectively. These slope references can be simply applied to single-slope A/D conversion, as shown in Fig. 3(a). The output image can be synthesized with two digital outputs converted by HG slope and LG slope. However, the conversion speed becomes longer; thus, the multiple sampling is not effective for high-frame-rate operation. In the proposed gain-adaptive operation shown in Fig. 3(b), each column ADC determines which slope reference will be used for conversion before the single-slope A/D operation. A pixel reset level is sequentially converted by the HG and LG slopes. We employ

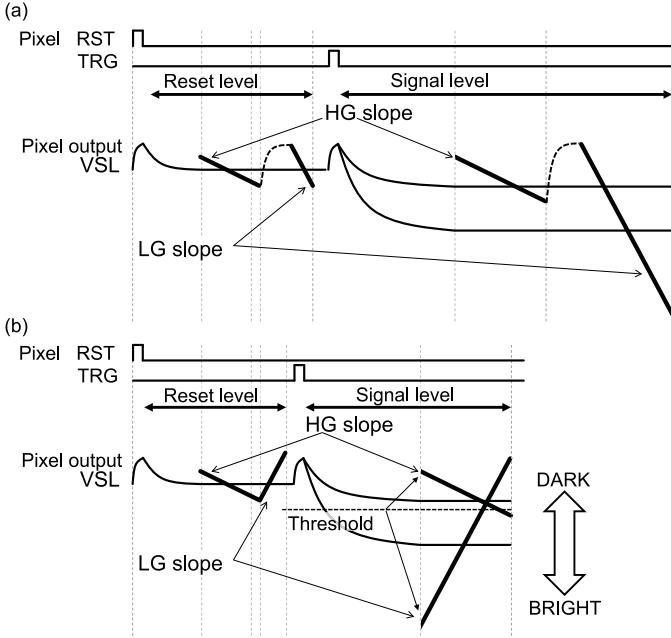


Fig. 3. Concept of A/D operation with two slope references. (a) Example of multiple-sampling single-slope A/D conversion. (b) Proposed gain-adaptive single-slope A/D conversion.

the positive LG slope against the negative HG slope to reduce the time overhead of switching from the HG slope to the LG slope. The HG and LG slopes in the opposite directions also contribute to reducing the power overhead of the slope generator, which is detailed in Section II-C. After the reset level is converted, the pixel signal level is compared with the threshold voltage; then, either the HG slope or LG slope is selected for conversion of the signal level. In the case of a darker pixel output than the determined threshold level, the HG slope is applied for low-noise conversion. Otherwise, in the case of a brighter pixel output than the threshold, the LG slope is applied for unclipped highlights. The threshold voltage is set to a higher level than the endpoint of the HG slope for the signal level. In our design, the gain ratio of HG and LG slopes is set to 12 dB. Accordingly, the 12-bit counting operation offers a 14-bit equivalent resolution for the dark pixel output. The gain-adaptive operation efficiently reduces the conversion time.

### B. Sensor Architecture

Fig. 4 presents a block diagram of the image sensor. It consists of a pixel array with an in-pixel memory for the global-shutter feature, row decoders and drivers, column-parallel ADCs with slope reference generators, control and data processing logics, and output interfaces. Each pixel has a photo diode, an overflow gate, a charge storage node, a charge transfer gate, a reset transistor, a source follower amplifier, and a pixel select transistor. The overflow gate is controlled by a signal of OFG and is used for the electrical shutter control at the beginning of the exposure period. All the photo diodes are simultaneously reset for the global shutter operation during the signal readout for the previous frame integration. Therefore, the exposure period of each frame can be continuous with no temporal dead time.

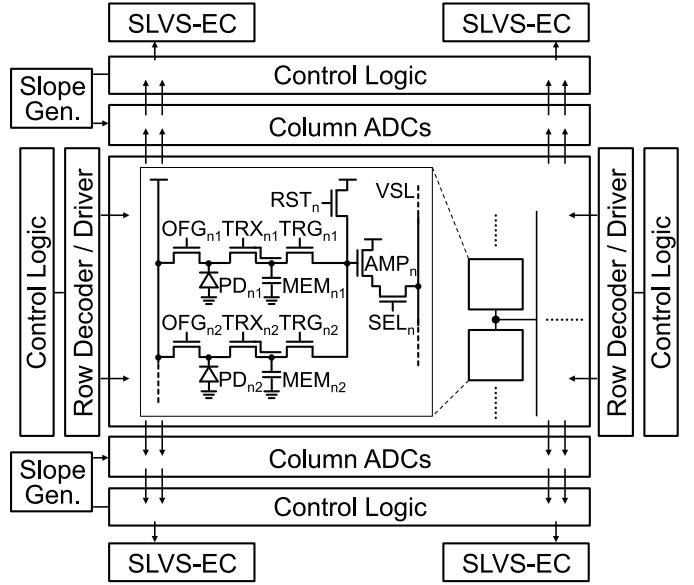


Fig. 4. Sensor block diagram with global-shutter pixels.

The charge storage node of MEM is placed under the first transfer gate controlled by a signal of TRX. At the end of the exposure period, photo electrons integrated on each photo diode are transferred to the memory node of MEM. During the exposure period for the next frame, the floating diffusion is reset by a signal of RST. Then, the signal electrons are output from the storage node to a floating diffusion at the source follower amplifier of AMP through the second transfer gate controlled by a signal of TRG. This signal readout operation from the storage node is performed line by line.

The reset transistor, source follower amplifier, and pixel select transistor are shared by two pixels. The pixel output is connected to column-parallel ADCs through a vertical signal line. The pixel outputs are digitized by the column-parallel ADC based on the SS-ADC architecture. The slope reference voltage is offered from the slope reference generator. The sensor has 16-channel output interfaces of a 4.752-Gbps/ch scalable low-voltage scaling interface with an embedded clock (SLVS-EC).

### C. Circuit Implementation

Fig. 5 presents a circuit diagram of gain-adaptive column ADCs. A slope generator distributes an HG slope and an LG slope to column ADCs. The two slopes are selected by  $D_{flag}$  in each column block. One is provided to a comparator; the other is connected to a capacitance of  $C_{dm}$ .  $C_{dm}$  is designed to have the same value as the comparator input capacitance to maintain the total load capacitance of each slope in a stable manner independently of  $D_{flag}$ . The output of the comparator,  $D_{CO}$ , inputs to the hybrid column counter presented in [5]. The hybrid column counter is composed of 5-bit memories for lower bits, 10-bit up/down ripple counter for upper bits, and a lower bit CDS unit. The hybrid column counter is extended with column buffers for digital CDS of gain-adaptive ADC. The digital codes can be buffered from the memories and counter. In addition, they are restored to the counters during a horizontal scanning period, as per  $D_{flag}$  from a comparator.

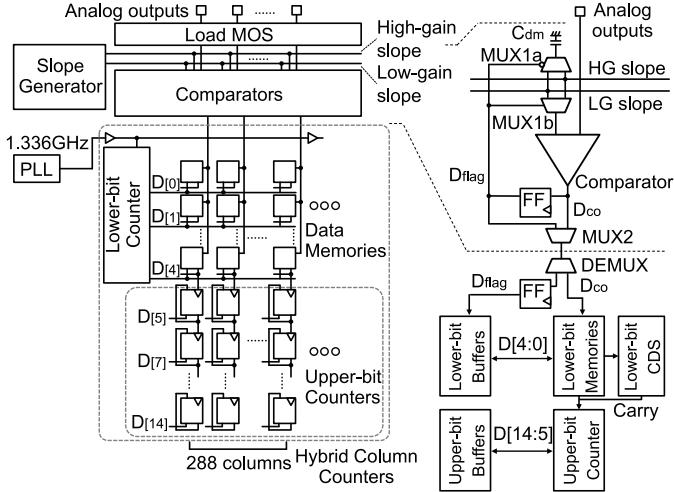


Fig. 5. Circuit diagram of pixelwise gain-adaptive column ADCs.

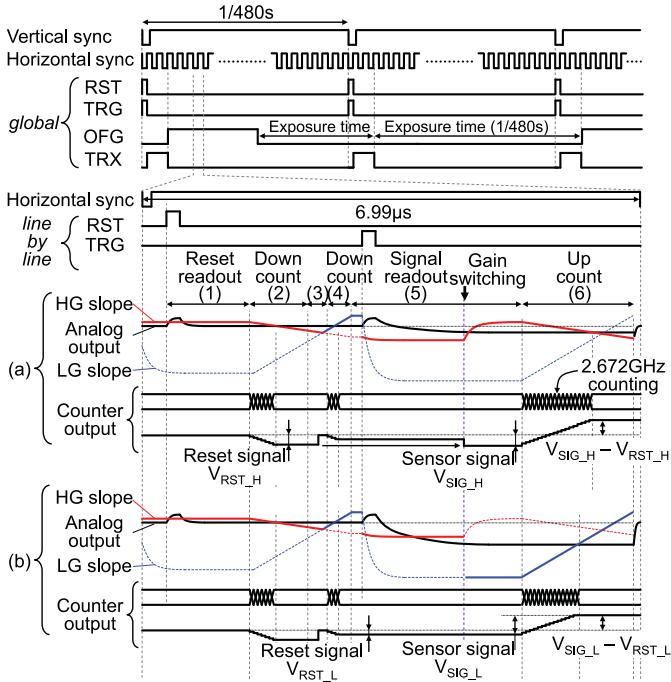


Fig. 6. Timing diagram. The operation is switched between (a) and (b) during the signal readout (5) according to each pixel output.

Fig. 6 shows a timing diagram of a vertical scanning period and a horizontal scanning period. At the beginning of the frame period, all in-pixel memories are globally reset by signals of RST and TRG. Then, the signal electrons in the photo diode are transferred to each in-pixel memory by the turning on of TRG. At the time that TRG turns off, the exposure time ends. If we require an exposure time that is shorter than the frame period of 1/480 s, OFG is activated at the time of TRG turning off, and the exposure period starts at the OFG turn-off point. In case the exposure time is the same as the frame period of 1/480 s for a dead-time free global-shutter operation, the OFG is inactivated. After the exposure time of the previous frame ends, the frame scan starts in a line-by-line fashion. The pixel reset level, settled in (1), is sampled for analog CDS at the comparator as the same technique presented in [5] and is

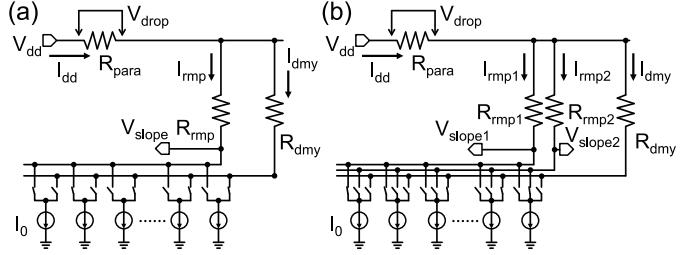


Fig. 7. Simplified circuit diagram of the slope reference generator. (a) Basic configuration. (b) Extended configuration for gain-adaptive ADC.

then converted into digital codes as  $V_{RST_H}$ . The HG slope is selected by resetting the  $D_{flag}$  in (2). Here, the LG slope is connected to the dummy capacitor of  $C_{dm}$ . The counter codes of  $V_{RST_H}$  are temporarily stored in the column buffers in (3). The pixel reset level is again converted into  $V_{RST_L}$  with the LG slope by setting  $D_{flag}$  in (4). During the operation period of (4), the HG slope is connected to the dummy capacitor of  $C_{dm}$ . Here, the gain of the LG slope is 12 dB lower than that of the HG slope. Furthermore, the operation procedure branches into (a) and (b), while an analog output of the pixel signal level is given in (5).

The HG slope is fixed to a threshold voltage. In terms of pixel settling, each comparator determines whether the pixel level reaches a higher or a lower level than the threshold level of the gain-switching point provided by the HG slope.  $D_{flag}$  is updated by each comparator output of  $D_{co}$ . Consequently, the HG and LG slopes are adaptively selected for darker and brighter pixels, respectively. The severe threshold accuracy is unnecessary for the adaptive-gain A/D conversion; therefore, the determination is made before the signal output has been completely settled. This “prediction” avoids the time overhead of the gain-adaptive operation compared with the original SS-ADC.

For the CDS operation in (6), the digital codes of  $V_{RST_H}$  are restored in the column counters in the case of (a), where the pixel output is darker than the threshold level. The HG slope is selected according to  $D_{flag}$ . The signal level is digitized as  $V_{SIG_H}$ , while the CDS is conducted as  $V_{SIG_H} - V_{RST_H}$ . Conversely, the digital codes of  $V_{RST_L}$  are still stored in the case of (b), where the pixel output is brighter than the threshold level. The LG slope is connected to a comparator, and the signal level is digitized as  $V_{SIG_L}$ . The CDS is performed in each column as well as in the case of (a). Finally, each column provides digital outputs of  $V_{SIG_H} - V_{RST_H}$  or  $V_{SIG_L} - V_{RST_L}$  with  $D_{flag}$ . The counter operates with a 1.336-GHz clock, which realizes 2.672-GHz counting. The pixel readout and A/D conversion is accomplished in 6.99  $\mu$ s.

Fig. 7 provides a simplified circuit diagram of the slope reference generator. The main overhead of power consumption of gain-adaptive column ADCs is the additional slope reference. In a basic configuration, as shown in Fig. 7(a), a slope reference voltage is generated by increasing a current of  $I_{rmp}$  to a load resistor of  $R_{rmp}$ . On the other hand, a dummy current of  $I_{dmy}$  follows the change of  $I_{rmp}$  during the A/D conversion because the total current of  $I_{dd}$  should be constant to avoid a voltage drop of  $V_{drop}$  caused by a parasitic load of  $R_{para}$ .

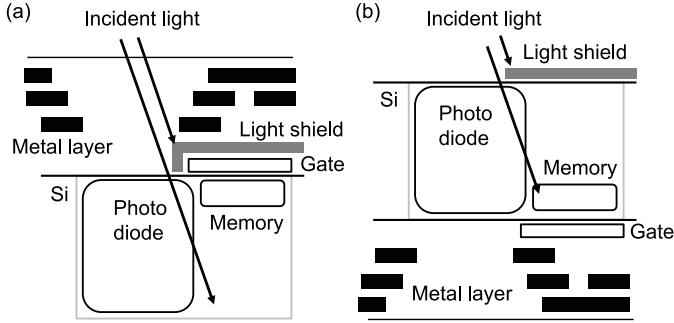


Fig. 8. Device structure of the global-shutter pixel with in-pixel memory. (a) Front-illuminated device structure. (b) Back-illuminated device structure.

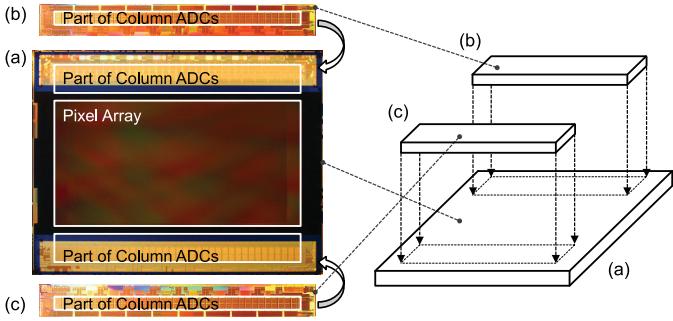


Fig. 9. Chip microphotograph and multiple chip-on-chip stacked structure with microbumps. (a) Sensor chip. (b) and (c) Logic chips.

For the gain-adaptive operation, the slope reference generator is extended, as shown in Fig. 7(b). The dummy current is split into an additional load resistor of  $R_{\text{rmp}2}$ . The split current of  $I_{\text{rmp}2}$  is controlled to generate an LG slope reference. The LG slope is opposite to the HG slope to keep the total current constant. The overhead of power consumption is thereby efficiently suppressed.

### III. DEVICE INTEGRATION

We employed a chip-on-chip stacked device structure to make available both a front-illuminated global-shutter pixel with low PLS and a process technology for stacked high-speed low-power circuits. As shown in the pixel structure of the front-illuminated global-shutter pixel in Fig. 8(a), the in-pixel memory is well protected from incident light by a special light shield layer. A potential barrier is formed beneath the in-pixel memory to block the photo-generated electrons under the memory region. On the other hand, it becomes difficult to completely cover the in-pixel memory by a light shield layer in the back-illuminated device structure shown in Fig. 8(b). The incident light generates photo electrons in the memory region so that the PLS degrades.

Fig. 9 shows the fabricated image sensor and device structure composed of a sensor chip and two diced logic chips with microbump interconnections. The base chip is a sensor fabricated with 90-nm 1-poly-Si 5-metal-layer image sensor process technology, which includes a pixel array and a portion of the column ADCs. The pixel array has  $4624 \times 2296$  global-shutter pixels. The number of effective pixels is  $3840 \times 2160$ . The pixel pitch is  $5.86 \mu\text{m}$ . The opening area of the light shield layer is approximately 30% of the pixel.

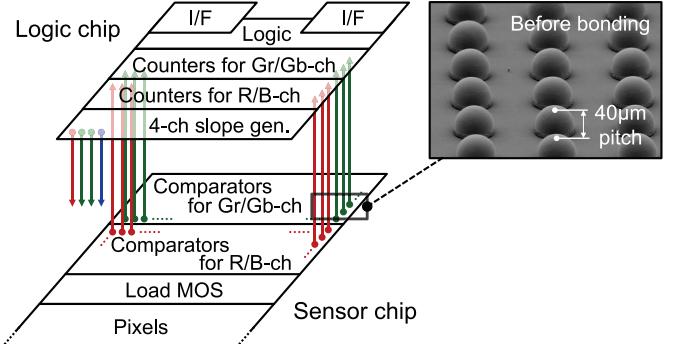


Fig. 10. Block diagram integrated on a sensor chip and logic chips through microbumps.

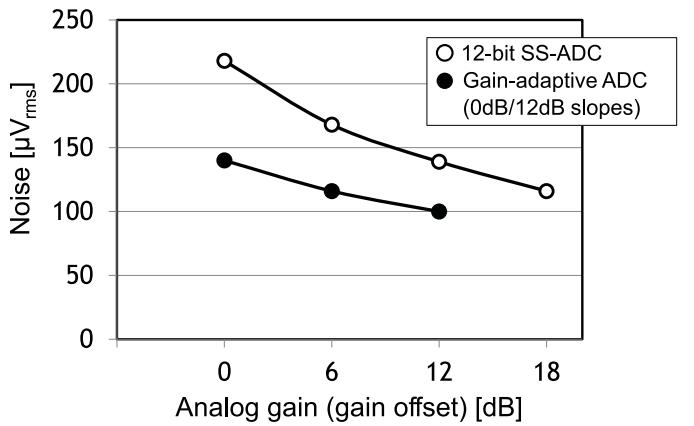


Fig. 11. Random noise versus analog gain offset.

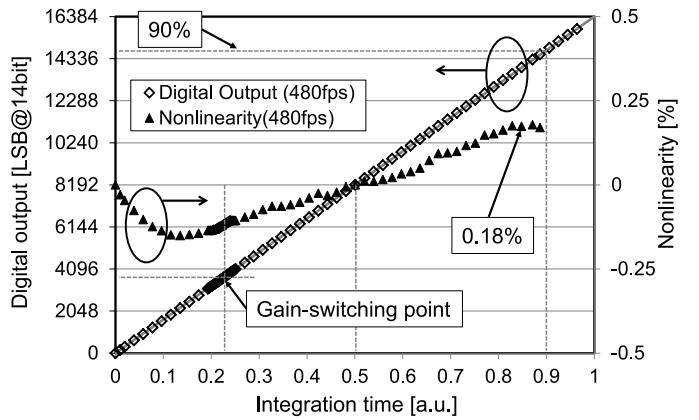


Fig. 12. Sensor linearity with on-chip gain calibration.

In the  $5.86-\mu\text{m}$  pixel pitch, four column ADCs are integrated on each side. The column ADCs are split into an analog part and a digital part on the sensor chip and the logic chips, respectively. The total microbumps are 38 K bumps for two diced logics. The logic chips are fabricated with 65-nm 1-poly-Si 9-metal-layer CMOS process technology. The chip-on-chip process can enable known-good-die testing before bonding so that the cost can be efficiently reduced, especially for a large optical format sensor and large-scaled logic circuits.

Fig. 10 depicts a magnified view of the stacked part of the block diagram. The  $40-\mu\text{m}$  pitch microbumps are arrayed on the comparator part and connect comparators to counter

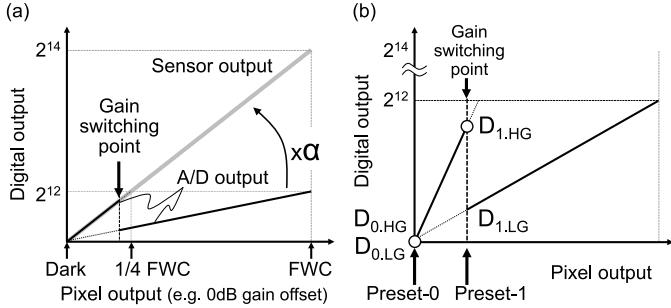


Fig. 13. On-chip gain calibration. (a) Digital output. (b) Preset levels for calibration.

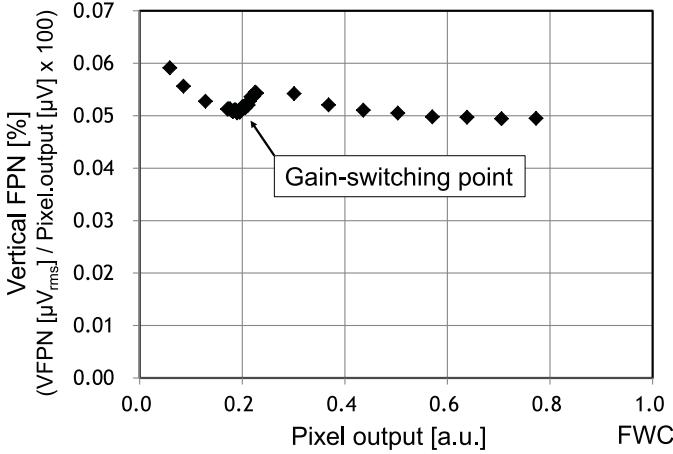


Fig. 14. Vertical FPN versus pixel output.

each column. The column ADCs are separated into two parts for the respective R/B and Gr/Gb channels. The counters are placed directly on the comparator part. Slope reference generators are integrated on the logic chip. Meanwhile, the slope signal is connected to the comparator through microbumps. We implemented the four-channel color-independent slope generators to control the white balance by analog gain offset. A total of 16-channel SLVS-EC interfaces of 4.752 Gbps/ch were integrated on the stacked logic chips.

#### IV. EXPERIMENTAL RESULTS

Fig. 11 shows the measured total random noise under a dark condition. Compared to the standard 12-bit single-slope operation, the gain-adaptive operation efficiently suppresses the input-referred random noise into  $140 \mu\text{V}_{\text{rms}}$  at an analog gain offset of 0 dB. The gain-adaptive operation uses 0 and 12 dB slopes for LG and HG slopes, respectively. The gain offset can be changed from 0 to 12 dB. For example, at an analog gain offset of 12 dB, the LG and HG slopes are set to 12 and 24 dB against the full scale of the pixel output. At the analog gain offset of 12 dB, the total input-referred random noise reaches  $100 \mu\text{V}_{\text{rms}}$ .

Fig. 12 shows the measured sensor linearity. The gain-adaptive column ADCs count 12-bit codes for the pixel signal level. The output codes obtained by the LG slope are multiplied by a gain ratio of  $\alpha$  of the HG slope to the LG slope at the on-chip digital block, as shown in Fig. 13(a), where the linear 14-bit outputs are reconstructed in nonlinearity within

TABLE I  
CHIP CHARACTERISTICS

Fabrication process	90nm 1P5M + Light Shield; 65nm 1P9M Logic
Supply voltage	3.3V / 3.0V / 1.25V / 1.2V
Num. of effective pixels	3840 (H) x 2160 (V)
Num. of total pixels	4624 (H) x 2296 (V)
Pixel size	5.86μm (H) x 5.86μm (V)
Output interface	16ch x 4.752Gbps/ch SLVS-EC
Max. frame rate	480fps
Power consumption	5.23W (480fps); 2.15W (60fps)
Saturation signal	30,450e-
Sensitivity	17,500e-/lx-s (green pixel, 3200K light with IR cut filter)
Parasitic light sensitivity	-99.6dB
Conversion gain	30.3μV/e-
Analog gain	Adaptive gain: 0dB / 12dB Gain offset: +0dB ~ +12dB (for each color independently)
RMS random noise	140μVrms (Gain offset 0dB); 100μVrms (Gain offset 12dB)
RMS vertical FPN	0.11e-rms at 480fps w/o additional correction circuit
Dynamic range	76.3dB

0.18% of the full scale without special trimming or tuning calibration parameters.

Our proposed gain-adaptive ADCs showed a strong advantage on negligible column variations of dark offset and gain on account of the complete CDS and common slope reference on the overall column ADCs. Therefore, we had to calibrate only the gain ratio of HG and LG slopes caused by the gain error on the slope generator. The proposed sensor has additional horizontal pixel lines with preset output levels, Preset-0 and Preset-1, on the dark level and the gain-switching level, as shown in Fig. 13(b). The preset voltages are offered from on-chip digital-to-analog converters. At the beginning of each frame scan, Preset-1 is tuned to the gain-switching point, and then both Preset-0 and Preset-1 are converted by HG and LG slopes to calculate the gain ratio of  $\alpha$  as  $(D_{1,HG} - D_{0,HG}) / (D_{1,LG} - D_{0,LG})$ . Preset-0 is set close to the pixel reset level as the dark level, where we do not need to precisely tune it because the analog CDS is carried out at the comparator of the column ADCs. Preset-1 is set to a predetermined voltage at first, where the difference between Preset-1 and Preset-0 corresponds to the gain-switching point controlled to 90% of HG-slope full scale on the slope generator. Here, the additional pixel line set to Preset-1 is converted in the adaptive-gain operation. The number of flag bits,  $D_{\text{flag}}$ , is counted. Then, Preset-1 is updated toward fifty-fifty “0” and “1” of the flag bits; i.e., the pixel output of Preset-1 becomes the threshold level of the gain-switching point. After Preset-1 is updated, the additional pixel line set to Preset-0 is converted by both HG and LG slopes to obtain  $D_{0,HG}$  and  $D_{0,LG}$ , where the column ADCs are forced to either an HG or LG operation. Next, that of updated Preset-1 is converted to obtain  $D_{1,HG}$  and  $D_{1,LG}$  in the same manner. The preset levels are turned over to the next frame as initial levels, and the calibration is carried out for each frame. The on-chip online digital calibration can follow a temperature drift, supply voltage conditions, and device variations. This helps make the connecting point invisible on a captured image, where the switching points are somewhat scattered by analog temporal noise and variations of pixel transistors.

TABLE II  
PERFORMANCE COMPARISON

		This Work	[7] 2016	[6] 2016	[1] 2015	[2] 2015	[3] 2013	[4] 2013	[5] 2011
Optical format		Super35	APS-H	N/A	Super35	Full35	2/3-inch	1-inch	Super35
Pixel pitch	μm	5.86	1.5	1.1	3.2	2.45	5	2.86	4.2
Global/Rolling shutter		<b>GS</b>	RS	RS	RS	RS	<b>GS</b>	RS	RS
Num of pixels (H)	pixels	3840	19568	7728	7680	15360	1920	4620	8192
Num of pixels (V)	pixels	2160	12588	4368	4320	8640	1080	3084	2160
Frame rate	fps	480	5	240	120	60	240	80	120
Power consumption	mW	5,230	1,970	3,000	3,200	11,050	1,100	1,100	3,000
Conversion gain	μV/e-	30.3	91.0	92.0	61.0	80.0	95.0	45.0	57.0
Analog gain (lowest)	times	1	1	1	3.5	1	2	1	1
Noise	μVRMS	<b>140</b>	319	414	317	614	380	315	250
	e-rms	4.6	3.5	4.5	5.2	7.7	4.0	7.0	4.4
Saturation	mV	<b>923</b>	687	524	933	800	1,425	720	1,197
	e-	30,450	7,550	5,700	15,300	10,005	15,000	16,000	21,000
Dynamic range	dB	76.3	66.7	62.1	69.7	62.3	71.5	67.2	74.4
FoM	e-.pJ/DRU	<b>0.92</b>	2.60	1.32	4.97	8.18	4.72	2.96	1.29

FoM = (power × noise) / (num. pixels × fps × DRU); DRU = {(saturation / gain) / noise}

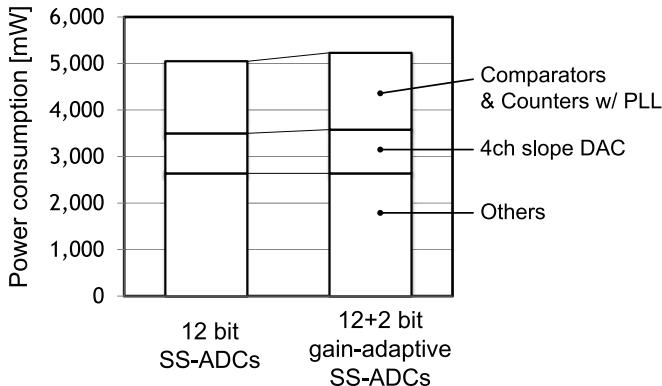


Fig. 15. Power consumption.

Fig. 14 shows the vertical FPN versus the pixel output from a dark condition to a bright condition close to the FWC. Owing to the complete CDS and gain calibration on the column-common slope references, the vertical FPN is at a very low level, less than 0.1%, which is negligible even on the gain-switching point. The vertical FPN under a dark condition is 0.11 e<sub>rms</sub> at 480 fps without additional correction.

Fig. 15 shows the measured power consumption at 480 fps with a standard 12-bit single-slope operation and the 12 + 2-bit gain-adaptive operation. The total power consumption is 5.23 W. The power consumption overhead is less than 4% compared to the standard 12-bit single slope operation of 5.05 W. The power consumption overhead comes from the column ADCs and the 4-ch slope DAC. The column ADCs including comparators and counters require an additional counting operation for a pixel reset level by the LG slope. The 4-ch slope DAC has an additional clamp control for the LG slope on the slope generators.

Fig. 16 shows a sample image captured at 480 fps with a gain-adaptive single-slope operation. The sensor offers good



Fig. 16. Sample image captured at 480 fps.

images without any loss of image quality in a 480-fps movie. Table I summarizes the chip characteristics. The saturation signal is 30,450 e- and the sensitivity is 17,500 e-/lx·s. The PLS of the global-shutter pixels achieves -99.6 dB. The PLS is defined as the sensitivity ratio of the in-pixel analog memory to the photo diode under a light condition of 5,100 K with an IR cut filter. The number is the worst case among the RGB color pixels. The intrascene dynamic range achieves 76.3 dB obtained by the input-referred random noise of 140 uVRMS and full-scale voltage of 923 mV at the gain offset of 0 dB. Table II shows the performance comparison of high-speed image sensors with similar optical formats [1]–[7]. The figure of merit is here defined as (noise × power)/(number of pixels × frame rate × dynamic range), which means the simultaneous capability of maintaining both highlights and detailed shadows with low noise readout.

## V. CONCLUSION

An 8.3M-pixel 480-fps global-shutter CMOS image sensor with a super 35-mm optical format was developed.

The proposed gain-adaptive column ADCs achieved 140- $\mu$ Vrms input-referred dark noise at 0 dB gain for the input-referred full-scale readout of 923 mV. The on-chip online correction of gain error efficiently suppressed the sensor nonlinearity within 0.18% and the vertical fixed-pattern noise was less than 0.1%. The front-illuminated stacked device structure with 38-K microbump interconnections realized the combination of a global-shutter pixel with -99.6-dB PLS and high-speed digital circuits for a 4.752-Gbps/ch interface. The proposed image sensor is expected to contribute to a highly realistic video system for 4 K digital imaging featuring slow-motion movies.

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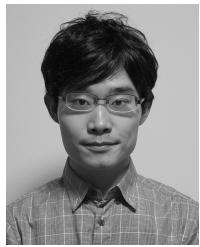
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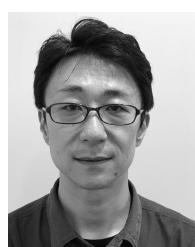
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