A 9-bit 215 MS/s Folding-Flash Time-to-Digital Converter Based on Redundant Remainder Number System in 45-nm CMOS

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***Abstract*— The first folding-flash time-to-digital converter (TDC) based on the remainder number system (RNS) is reported. In this paper, fine quantization of an input time interval is performed directly with dual free-running ring oscillators without additional circuitry to record the coarse bits. The RNS architecture reduces hardware complexity significantly without speed impairment relative to the full flash counterpart employing delay chains. As a proof-of-concept design, 490 quantization levels using only 84 delay stages achieve a sample rate of 215 MS/s and an LSB size of 9.4 ps. Without trimming or calibration, the measured differential nonlinearity and integral nonlinearity of the RNS TDC prototype are +0.53/−0.57 and +1.1/−1.1 LSBs, respectively.**

***Index Terms*— Folding-flash, remainder number redundancy (RNR), remainder number system (RNS), remainder redundancy (RR), time-to-digital converter (TDC).**

I. Introduction

TIME-TO-DIGITAL converters (TDCs) are widely used in many applications where precision time interval measurements are needed, e.g., in time-of-flight measurements. In TDC design, it is widely known that the flash architecture based on delay lines provides the highest conversion speed at the cost of circuit complexity [1], [2]. Fig. 1 shows the circuit diagram of a typical flash TDC. One problem associated with the flash architecture is complexity, which is exponentially dependent on the number of bits—for example, in a conventional n-bit delay-chain TDC 2^n-1 delay elements and 2^n-1 D-flip-flops (DFFs) are required, leading to high power and chip area consumptions. The LSB size of a delay-chain TDC is usually set by the propagation delay of a unit delay element (often one or two inverters), which is fundamentally limited by the process technology in which the TDC is implemented. Therefore, it is difficult to achieve high conversion linearity as it is hard to maintain good matching among many delay cells and DFFs. The Vernier TDC can achieve sub-inverter-delay LSB size [3]–[8]. The 2-D Vernier TDC further reduces the number of stages to be proportional to the square root of the conversion range [7]. However, they are at the cost of extra conversion time and latency that limits their utilization in higher conversion rate applications (e.g., >200 MS/s). The drawbacks of the flash architecture motivate the development of the pipelined TDCs [9], [10]. Although with pipeline, a small LSB size and hence a high resolution can be achieved; the necessity of time residue amplification dictates a higher architectural complexity, thus limiting the conversion throughput and efficiency.

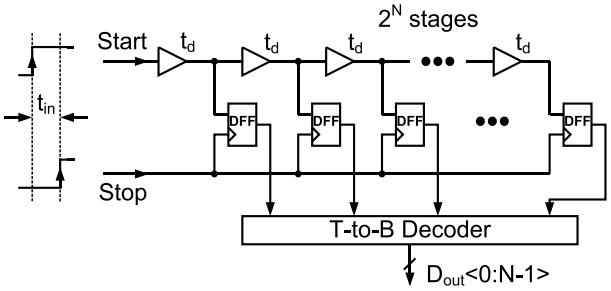

Fig. 1. Diagram of the conventional flash TDC.

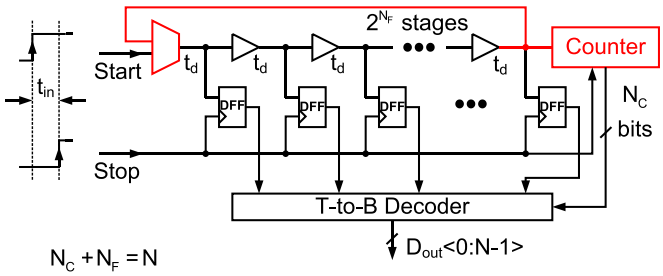

Fig. 2. Diagram of the folding TDC.

To reduce the number of delay elements of the flash architecture, ring oscillator (RO) plus counter [11] have been exploited as a folded delay chain for time quantization, which is similar to the folding operation in a folding analog-to-digital converter [12], but providing more linear characteristics. As shown in Fig. 2, delay cells are connected in a loop with an input multiplexer. This loop forms the fine quantizer, while a counter is employed as the coarse quantizer. The total conversion range is the summation of the fine and

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coarse resolutions. The resolution of the plain RO is normally limited by the propagation delay of delay cells, but can be increased by utilizing interpolation [13]–[16] or gated RO-based oversampling architecture with noise shaping [17], [18]. Albeit efficient, there are two problems encountered in a folding RO-based TDC. First, the input multiplexer and the counter load the loop at one node (but usually not at the same node), which leads to non-uniform stage delays within the loop (and thus nonlinearity), necessitating dummy-load insertion for all other RO stages. Second, the coarse counter and the fine quantizer may suffer from a synchronization issue, and additional bit alignment logic is needed to alleviate this problem as discussed in [19] and utilized in recent voltage-controlled oscillator-based converters [11], [20].

To eliminate the drawbacks above without degrading the performance, in this paper, a novel TDC architecture based on the remainder number system (RNS) is presented [21]. In RNS, a positive integer X is represented by its L remainders $\{r_1, r_2, \ldots, r_L\}$, obtained by dividing X by L positive integers $\{\Gamma_1, \Gamma_2, \ldots, \Gamma_L\}$, i.e., $\{r_i\} = X \bmod \{\Gamma_i\}$. When X is smaller than the least common multiple of $\{\Gamma_i\}$ and all the moduli $\{\Gamma_i\}$ are co-prime, such a representation is unique. In addition, compared with the binary arithmetic, the RNS arithmetic is carry free and can achieve very high processing speed for addition, subtraction, and multiplication operations. A direct benefit of the RNS conversion is the great reduction of the flash architectural complexity. For example, ideally, a converter based on the modulus set {5, 7, 9} can realize $5 \times 7 \times 9 = 315$ quantization levels, i.e., more than 8 bits, with only $5 + 7 + 9 = 21$ arbiters. Moreover, since no coarse counter is needed in an RNS TDC, the conversion speed is similar to that of the full flash type.

Last, while RNS has been used in numerous applications such as cryptography, channel coding, signal processing, and radar system, it is known to be sensitive to remainder errors [22]. To mitigate this problem, architectural redundancy will be introduced and realized in this prototype work.

This paper is organized as follows. First, an overview of RNS is given. Then the basic of RNS TDC is covered in Section II, followed by the introduction of the redundant RNS conversion architecture and design concerns on the analog impairments of RNS TDC in Section III. In Section IV, a prototype implemented in a 45-nm CMOS process, reporting an 8.94-bit 9.4-ps resolution and a 215 MS/s conversion speed, is presented. Last, the measurement results are summarized and the non-idealities are discussed in Section V, and a conclusion is drawn in Section VI.

II. RNS TDC Architecture

A. RNS Quantization Principle

The principle of RNS quantization is explained in Fig. 3. Suppose we have two integers, Γ_1 and Γ_2, that are co-prime and a floating-point input X. When X is divided by Γ_1 and Γ_2, it produces two quotients and two remainders, q_1, q_2, and r_1, r_2. In RNS, the quotients are discarded, whereas the integer parts of the remainders r_1 and r_2 are retained to represent the original input X. For a general L-remainder system,

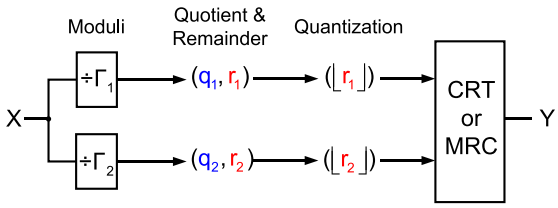

Fig. 3. Principle of the remainder number system.

we have

$$\begin{cases} Y = q_1\Gamma_1 + r_1 \\ Y = q_2\Gamma_2 + r_2 \\ \quad\vdots \\ Y = q_L\Gamma_L + r_L \end{cases} \tag{1}$$

where Y denotes the quantization outcome of X. To obtain a decimal representation of Y from the L remainders, two RNS decoding algorithms can be used: the Chinese remainder theorem (CRT) and the mixed radix conversion (MRC) [22]. In this paper, CRT is employed because its computation can be parallelized, while MRC is a sequential process [23]. For an L-remainder system, when CRT is employed as the RNS decoder, the final conversion outcome Y can be expressed as

$$Y = \sum_{i=1}^{L} \overline{\Gamma_i}\frac{\Gamma}{\Gamma_i} r_i + k \cdot \Gamma, \quad k \in \mathbb{Z}, \tag{2}$$

where the least common multiple $\Gamma = \Gamma_1\Gamma_2 \cdots \Gamma_L$, k represents one arbitrary element of the integer set $\mathbb{Z}$. As for the variable $\overline{\Gamma_i}$, if we substitute Y to (1), we can observe that for each divider Γ_i, the term $\overline{\Gamma_i}\Gamma r_i/\Gamma_i$ must contribute the remainder r_i, because other terms in (2) are all divisible by Γ_i. This actually indicates $(\overline{\Gamma_i}\Gamma r_i/\Gamma_i) \bmod \Gamma_i = r_i$, which can be obtained by solving

$$(\overline{\Gamma_i} \cdot \Gamma/\Gamma_i) \bmod \Gamma_i = 1. \tag{3}$$

In CRT, $\overline{\Gamma_i}$ is named the modular multiplicative inverse of Γ/Γ_i. For instance, let us choose two moduli $\Gamma_1 = 5$ and $\Gamma_2 = 7$, and an input X of 16.3; 16.3 divided by 5 produces a quotient 3 and a remainder 1.3. We retain the integer part of the remainder and record it as 1. In the same way, 16.3 divided by the second modulus 7 generates a remainder recorded as 2. Now the two remainders $r_1 = 1$ and $r_2 = 2$ jointly represent the quantization of the original input X. In this case, $\Gamma = 5 \times 7 = 35$, and the modular multiplicative inverses are given as

$$\begin{aligned} (\overline{\Gamma_1} \times 7) \bmod 5 &= 1, \\ (\overline{\Gamma_2} \times 5) \bmod 7 &= 1. \end{aligned} \tag{4}$$

So, we obtain $\overline{\Gamma_1} = 3$ and $\overline{\Gamma_2} = 3$ by inspection. Now substitute the results into (2) and the final result of Y is given by

$$\begin{aligned} Y &= 3 \times 7 \times r_1 + 3 \times 5 \times r_2 + 35k \\ &= 21r_1 + 15r_2 + 35k \\ &= 51 + 35k, \quad k \in \mathbb{Z}. \end{aligned} \tag{5}$$

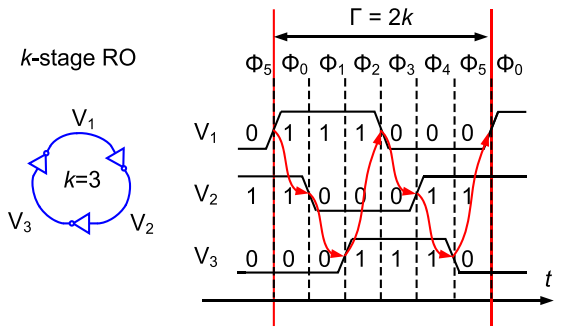

Fig. 4. Time-domain RO-based remainder generator.

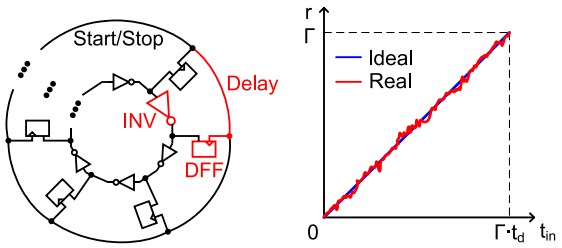

Fig. 5. Analog impairments in RO-based remainder generator.

It is noted that the full-scale input range for this modulus set is $5 \times 7 = 35$; so, $Y = 16$ is obtained for $k = -1$.

B. Time-Domain Remainder Generator

As analyzed before, an essential component of a TDC operating in the RNS domain is the remainder generator. Fortunately, RO is a natural remainder generator. In Fig. 4, a three-stage RO is given as an example. If we use the START and STOP signals to record the phase status within the RO, the remainder can be produced by simply differencing the recorded RO phases, i.e., $r = (\Phi_{\text{STOP}} - \Phi_{\text{START}}) \bmod 6$. The RO runs continuously for a continuous digitization of the incoming time intervals. The architecture, therefore, supports an equal run speed as the flash delay-chain structure, except the double sampling that results in 3 dB more quantization noise [19]. The RO internal phase cycles and one remainder production example are illustrated in Fig. 4. The cyclic thermometer codes represent the remainder of the input divided by 6 (i.e., the modulus of a k-stage RO is $2k$, essentially leading to 50% savings on hardware).

C. Analog Impairments

An inverter-based RO is chosen in this paper due to its simplicity. For a CMOS inverter, the timing error generated by device mismatch is much higher than that generated by thermal noise [24], so we focus on the analog impairments caused by the mismatch. There are mainly three types of mismatch errors in an RO-based TDC—the mismatch within the delay stages, the mismatch within the DFFs, and the propagation delay in the START/STOP distribution networks. Unfortunately, the plain RNS encoding is known to be vulnerable to the remainder errors, and thus to the mismatch errors identified above. The analog impairments will lead to

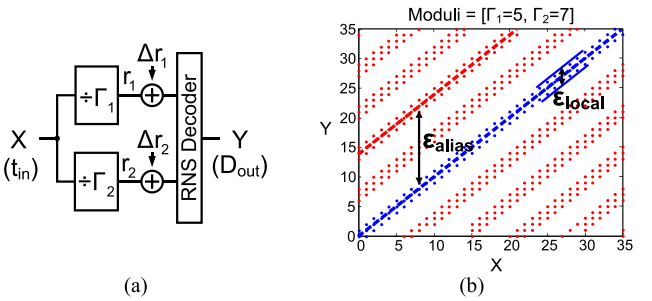

Fig. 6. (a) Non-ideal RNS system with remainder errors. (b) Reconstructed output versus input for $|\Delta r_i| \le 2$ LSBs.

conversion linearity errors as the red curve shown in Fig. 5. For example, if 1-LSB error is introduced to the remainders, $\Delta r_1 = 1$ and $\Delta r_2 = -1$, then (5) is revised to

$$\begin{aligned} Y &= 21(r_1 + \Delta r_1) + 15(r_2 + \Delta r_2) + 35k \\ &= 21r_1 + 15r_2 + 35k + 21\Delta r_1 + 15\Delta r_2 \\ &= 57 + 35k, \quad k \in \mathbb{Z}. \end{aligned} \tag{6}$$

The output Y is determined to be 22 for $k = -1$. In this case, the quantization error is 6 LSBs out of a full-scale range of 35 ($= 5 \times 7$) LSBs. This example reveals that the plain RNS architecture is sensitive to the remainder errors, and need to be remedied as errors are inevitable when signals are processed in analog forms.

To further explore the error sensitivity of the RNS architecture, behavioral simulation is conducted. Fig. 6(a) shows that a set of reminder errors $\{\Delta r_i\}$ is added to the reminders. In Fig. 6(b), the quantization output Y is plotted against the input X for a remainder error of $|\Delta r_i| \le 2$ LSBs. Results indicate that the errors can be large and are clustered in parallel bands separated vertically from each other. We categorize the RNS errors into two types: 1) the center distance from each error band to the primary band ($Y = X$). We term this the "alias" error or $\varepsilon_{\text{alias}}$ and 2) the local errors within each error band. We term this the "local" error or $\varepsilon_{\text{local}}$. The width of each error band is on the order of $\varepsilon_{\text{local}}$. The local errors are the typical integral nonlinearity (INL) and differential nonlinearity (DNL) errors we often encounter in data converters; whereas, the alias error is unique to the RNS architecture. Fig. 6 shows that for the same input X with varying magnitude of the remainder errors, the output Y can potentially deviate from its ideal value significantly, dependent on the exact magnitude of $\{\Delta r_i\}$. The alias error must be eliminated in a systematic way; otherwise, the RNS architecture is not practical.

III. Redundant RNS TDC Architecture

A. Redundant RNS Quantization Principle

Redundancy has been introduced to RNS to deal with remainder errors during digital transmission (or bit errors). The first method is called the remainder number redundancy (RNR) [25], as shown in Fig. 7(a), and the second is the remainder redundancy (RR) [26], as shown in Fig. 7(b). For RNR, an additional modulus is introduced. Since, the RNR

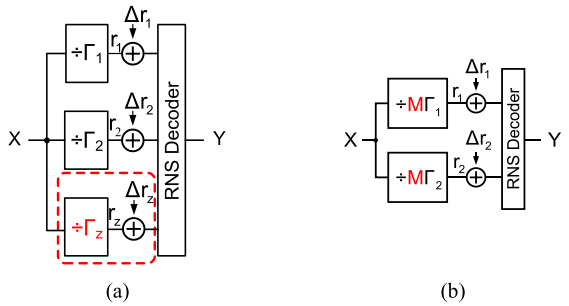

Fig. 7. Redundant RNS. (a) RNR: the moduli are $\{\Gamma_1, \Gamma_2, \Gamma_z\}$. (b) RR: the moduli are $\{M\Gamma_1, M\Gamma_2\}$.

method requires a part of the remainders to be completely error free, it is not suitable for an analog implementation, in which all remainders may contain errors. In contrast, the RR method introduces a common multiplier $M > 1$ to all moduli for error tolerance. [Here we recall that in the plain RNS encoding, the moduli are co-prime to each other and their greatest common divisor M is 1.] Therefore, in this paper, we chose the RR method. When RR is employed, we have

$$\begin{cases} Y = q_1\Gamma_1 M + \hat{r}_1 \\ Y = q_2\Gamma_2 M + \hat{r}_2 \\ \quad\vdots \\ Y = q_L\Gamma_L M + \hat{r}_L \end{cases} \tag{7}$$

where $1 \le i \le L$. Wang and Xia [26] have theoretically proved that when an adequate M is chosen, the solution of q_i is robust to remainder errors. The detailed algorithm proposed in [26] is summarized in the Appendix. The conclusion is quoted here—for RR RNS, if the first modulus is chosen as the reference,[1] q_1 can be recovered if and only if

$$\frac{M}{2} > |\Delta r_i - \Delta r_1|, \quad \text{for } 2 \le i \le L. \tag{8}$$

In practice, the worst case of (8) can be met by a more conservative criterion

$$\frac{M}{4} > \max|\Delta r_i|, \quad \text{for } 1 \le i \le L. \tag{9}$$

Then we can substitute the recovered (error-free) q_1 into (7), and the final residual error is from the remainder itself

$$|Y - X| \le \max|\Delta r_i|, \quad \text{for } 1 \le i \le L. \tag{10}$$

With RR, the RR-RNS converter provides similar speed performance as the flash converter. The characteristics of the plain and RR RNS are summarized in Table I. We note that in RR RNS, the full-scale input range is also enlarged by the same redundancy factor M. For example, (9) indicates that M needs to be larger than 8 for $|\Delta r_i| \le 2$LSBs. Fig. 8(a) and (b) show the simulation results for $M = 8$ and 10, respectively. In the latter case, $\varepsilon_{\text{alias}}$ disappears completely as expected.

[1]For an L-modulus system, we can obtain L different quotients, one for each remainder. Therefore, there are L ways to recover Y from the remainder set. Averaging can be performed over the set of recovered Y's for SNR improvement, assuming that the remainder errors are uncorrelated. This will be examined more in Section IV.

TABLE I
RNS METHOD COMPARISON

	Conventional RNS	RR RNS
Moduli	$\{\Gamma_1, \Gamma_2, \ldots \Gamma_L\}$	$\{M\Gamma_1, M\Gamma_2, \ldots M\Gamma_L\}$
Full-Scale Range	$FS = \prod_{i=1}^{L} \Gamma_i$	$FS = M\prod_{i=1}^{L} \Gamma_i$
Remainder Error Bound	$0 \le \Delta r_i < 1,\ 1 \le i \le L$	$\lvert\Delta r_i - \Delta r_1\rvert < M/2,\ 2 \le i \le L$
Reconstruction Method	$Y = q_i\Gamma_i + r_i + \Delta r_i,\ 1 \le i \le L$	$Y = Mq_i\Gamma_i + r_i + \Delta r_i,\ 1 \le i \le L$
Robustness	Not robust for $\lvert\Delta r_i\rvert \ge 1$	Robust $\lvert Y - X\rvert \le \max\lvert\Delta r_i\rvert, 1 \le i \le L$

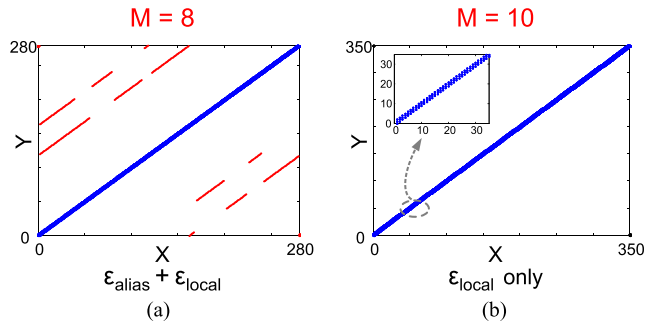

Fig. 8. Reconstructed output versus input of RR RNS for $|\Delta r_i| \le 2$ LSBs. (a) Moduli $= \{5M, 7M\} = \{40, 56\}$, $M = 8$. (b) Moduli $= \{5M, 7M\} = \{50, 70\}$, $M = 10$.

Now the redundant modulus set and the remainders become $\{M\Gamma_1 = 50,\ M\Gamma_2 = 70\}$ and $\{r_1 = 16,\ r_2 = 16\}$, respectively. If the same remainder errors are introduced, i.e., $\Delta r_1 = 1$ and $\Delta r_2 = -1$, we have $\{\hat{r}_1 = 17, \hat{r}_2 = 15\}$. For the dual moduli system, if the modulus 50 is chosen as the primary (i.e., to recover q_1 instead of q_2), according to the Appendix, we can obtain an output Y of 17; if the modulus 70 is chosen instead, Y is determined to be 15. So, in either case, the conversion error is 1 LSB out of a full range of 350 $(= 5 \times 7 \times 10)$ LSBs, i.e., significantly more accurate than the case without redundancy.

When the moduli are set, most of the parameters in the CRT algorithm can be calculated in advance to minimize the computational effort in decoding. It should be emphasized that the end results can be directly processed in RNS without going back and forth between the RNS and binary domains. Compared with the binary arithmetic, the major advantage of RNS is the absence of carry propagation for addition and multiplication [22], which are potentially suitable for high-speed applications. In this paper, we only use the CRT algorithm for performance evaluation of the RR-RNS converter.

B. Dual-RO RR-RNS TDC

To demonstrate the RNS TDC concept, the dual-RO RR-RNS TDC is proposed as shown in Fig. 9. Two remainders are directly obtained from two free-running ROs without any counter or other supporting circuitry. The stage numbers of the two ROs are chosen to be approximately the same to minimize the total number of RO stages.

For the dual-RO RR-RNS TDC, the analog impairments shown in Section III-C can be further modeled as a periodic

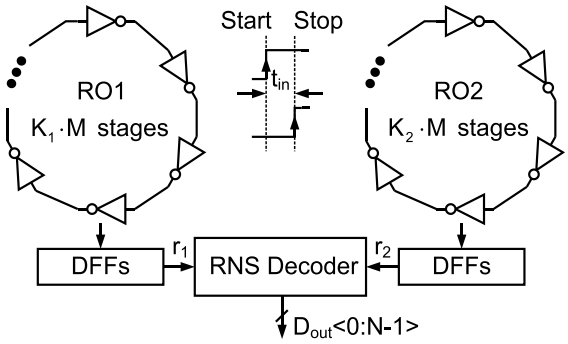

Fig. 9. Dual-RO RR-RNS TDC architecture.

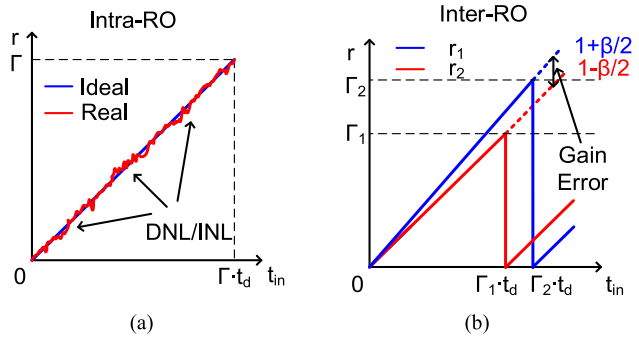

Fig. 10. (a) Intra-RO versus (b) inter-RO mismatch errors.

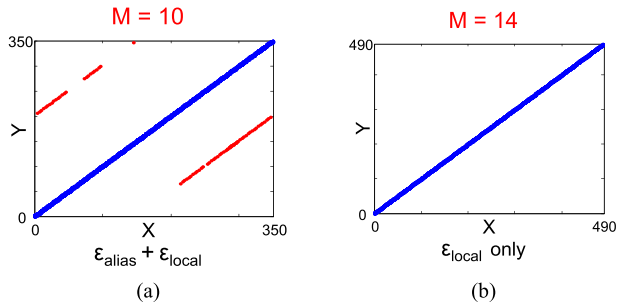

Fig. 11. Reconstructed output versus input of RR-RNS TDC for $|\Delta r_i| \leq 2$ LSBs. (a) Moduli = {50, 70}, $M = 10$ with $\beta = 0.6\%$. (b) Moduli = {70, 98}, $M = 14$ with $\beta = 0.6\%$.

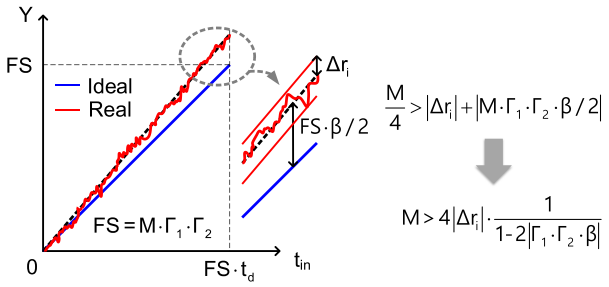

Fig. 12. Minimum requirement of M Factor with inter-RO gain mismatch β.

code-dependent offset—it is periodic because of the folding nature of the RO. As illustrated in Fig. 10(a), the code-dependent offsets within each RO lead to individual DNL and INL errors, called the "intra-RO" mismatch. Meanwhile, the mismatch of the average stage delay between the ROs will introduce systematic gain errors between the remainders, which is termed the "inter-RO" mismatch, as illustrated in Fig. 10(b). For example, in practice, the ideal RNS modulus set $\{\Gamma_1 = 5, \Gamma_2 = 7\}$ may become $\{\hat{\Gamma}_1 = 5.1, \hat{\Gamma}_2 = 7.2\}$. To model the inter-RO mismatch in this dual-RO architecture, we can introduce two variables α and β, defined as

$$\begin{cases} \hat{\Gamma}_1 = \alpha(1 + \beta/2)\Gamma_1 \\ \hat{\Gamma}_2 = \alpha(1 - \beta/2)\Gamma_2 \end{cases} \tag{11}$$

where α denotes the global gain error factor and β is the relative gain error factor. We note that the common factor α only introduces a small variation to the LSB size. Now substitute (11) into (7), the output Y is determined as

$$\begin{aligned} Y &= q_i(1 \pm \beta/2)\Gamma_i M + r_i + \Delta r_i \\ &= (q_i \Gamma_i M + r_i) + (\Delta r_i \pm \beta M q_i \Gamma_i/2). \end{aligned} \tag{12}$$

Equation (12) shows that the existence of the inter-RO mismatch exacerbates the total mismatch problem and dictates additional redundancy. For example, if β is non-zero, $\varepsilon_{\text{alias}}$ may reappear as the simulation result shown in Fig. 11(a). To mitigate this problem, the minimum value of the redundancy factor M should be increased when both intra-RO and inter-RO mismatches exist, that is

$$\frac{M}{4} > |\Delta r_i| + |\beta M q_i \Gamma_i/2|. \tag{13}$$

In this dual-RO topology, the term $Mq_i\Gamma_i$ should be smaller than the full-scale range $M\Gamma_1\Gamma_2$, as shown in Fig. 12. Then the conservative bound for M is revised to

$$\frac{M}{4} > |\Delta r_i| + |\beta M \Gamma_1 \Gamma_2/2|. \tag{14}$$

The extra term in (14) equals the product of the full-scale range and the gain error. This expression can be rewritten as

$$M > 4|\Delta r_i| \times \frac{1}{1 - 2|\Gamma_1\Gamma_2\beta|} \text{ for } 1 - 2|\Gamma_1\Gamma_2\beta| > 0. \tag{15}$$

If necessary, extra care such as phase locking can be applied to minimize the inter-RO mismatch [13]. As shown in (15), in this design, M is chosen to be 14 in order to cover a maximum of ± 2 LSB remainder error and an assumed gain error β of 0.6% based on the Monte Carlo simulation. These results are verified by behavioral simulation as shown in Fig. 11(b). It is notable that for an L-remainder RR RNS with a full-scale range FS, when an adequate M is chosen, the sum of the moduli is minimized when all the moduli are approximately equal to $(\text{FS}/M)^{1/L}$.

IV. Prototype Circuit Implementation

A. Overall Architecture

As analyzed previously, considering the intra- and inter-RO mismatches, the dual-RO RR-RNS TDC is proposed in this prototype work with $\{\Gamma_1 = 5, \Gamma_2 = 7\}$ and $M = 14$. So, its redundant modulus set is $\{M\Gamma_1 = 70, M\Gamma_2 = 98\}$. The values of Γ_1 and Γ_2 are chosen to be approximately equal to cover the full conversion range with minimum hardware. To achieve the RR, several techniques can be utilized, such as adding inverter stages, inserting local passive interpolation networks [14], [15]

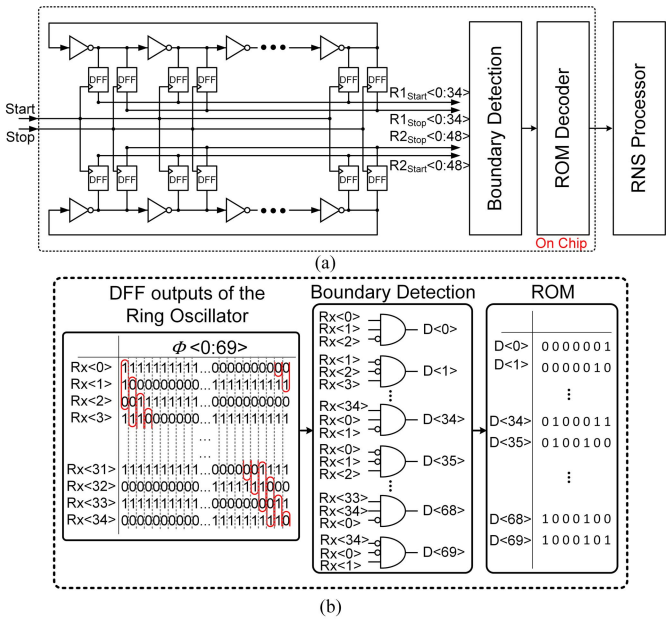

Fig. 13. (a) Architecture of the prototype dual-RO RR-RNS TDC. (b) On-chip readout functions.

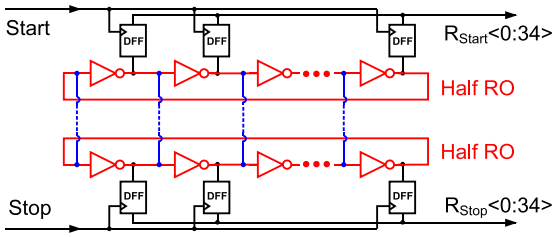

Fig. 14. Split-RO architecture.

or skewed set-reset latches [16], or employing time amplifiers [27]. In this proof-of-concept work, the redundant modulus set of {70, 98} is realized by a 35-stage RO and a 49-stage RO for simplicity. We note that the modulus of a k-stage RO is $2k$, which means an RO has a built-in redundancy factor of 2 compared to the delay-chain structure [21]. Therefore, 490 $(=5\times 7\times 14)$ quantization levels are achieved with only 84 $(=5\times 14/2+7\times 14/2)$ delay stages. The prototype RR-RNS TDC is shown in Fig. 13(a).

B. Dual-RO Remainder Generator

The TDC core consists of two RO-based remainder generators. Fig. 13(b) illustrates the detail of the RO consisting of 35 stages, in which Rx $\langle 0:34\rangle$ denotes the 35 outputs of the RO. A total of 70 cyclic thermometer codes are resolved, denoted as $\Phi\langle 0:69\rangle$. To avoid cluttering in the layout, each RO is split into two identical halves loaded by the START and STOP DFFs, respectively, as shown in Fig. 14. This arrangement also separates the START and the STOP signals physically to minimize crosstalk. The START and STOP signals are both distributed via an H-tree. To synchronize the two otherwise independent half ROs, their corresponding

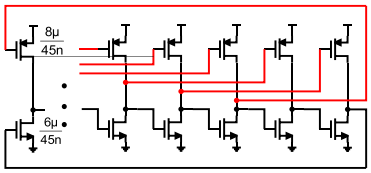

Fig. 15. Simplified schematic of the negatively skewed RO.

internal nodes are shorted through metal lines of minimum width, which helps cut down the parasitic capacitance of these connections while providing an equivalent resistance of ~200 Ω to limit any transient short circuit current between the two half inverters. To minimize the RO stage delay and to improve the TDC conversion speed, the RO topology incorporating a negatively skewed delay scheme [28] is adopted as shown in Fig. 15. The RO is based on a chain of inverters, with the NMOS and PMOS transistors in each stage driven by different nodes—the PMOS input is two stages leading that of the NMOS. Simulation results show that this scheme yields a smaller stage delay at the cost of double power consumption compared with the conventional inverter-based RO.

C. Readout Logics

The on-chip readout circuits are composed of the DFFs, boundary detectors, and ROM encoders. The DFF is realized by a symmetrical sense-amplifier-based arbiter [29]. The on-chip part also includes "01" boundary detectors and ROM encoders to help convert the cyclic thermometer codes from the DFFs, i.e., $R1_{\text{start}}\langle 0:34\rangle$, $R1_{\text{stop}}\langle 0:34\rangle$, $R2_{\text{start}}\langle 0:48\rangle$, and $R2_{\text{stop}}\langle 0:48\rangle$, to the binary format for data readout. The boundary detector is realized by a three-input AND gate to detect the "110" pattern for the even codes and "001" for the odd codes. The three-input AND gate helps reject bubble errors in the thermometer code, similar to that often deployed in voltage-domain flash converters. It is worth pointing out that among the aforementioned ±2 LSB remainder error, the worst case using a full-scale input shows that the cumulative RMS noise from the ROs is 0.13 LSBs in simulation, and the cumulative random mismatch from the delay cells plus arbiters is 0.08 LSBs. The remaining error budget is reserved for other non-idealities (e.g., gradient effect error, input clock jitter, and quantization noise), which will be discussed in Section V.

D. Split-TDC RNS Decoding

Since the dual ROs are free running, the recordings of the START and STOP events are asynchronous—the START and STOP events can begin at any RO stage and finish at another. Therefore, from sample to sample, an inherent DEM function is obtained, which helps improve the DNL performance of the TDC. However, the double sampling also doubles the quantization noise power, thus resulting in a 3-dB SNR penalty compared to the conventional flash TDC. We argued before that the dual-remainder structure can potentially gain 3 dB in SNR due to averaging. (A diagram of this is illustrated in Fig. 16.) As shown in the Appendix, for the dual-RO

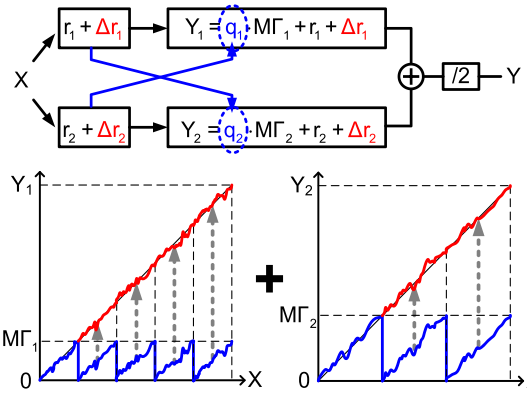

Fig. 16. 3-dB SNR improvement by averaging the conversion outcomes from the dual ROs.

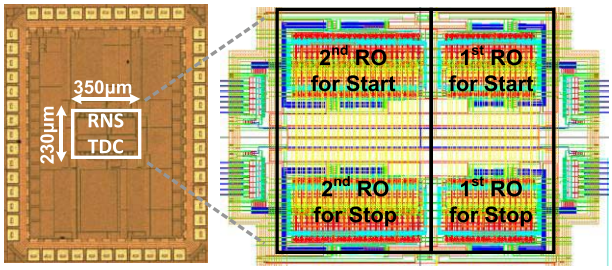

Fig. 17. Die photograph and layout screenshot of the prototype RNS TDC.

RR-RNS TDC, the quotients q_1 and q_2 can be recovered correctly in the presence of remainder errors. Since we have two remainders $\hat{r}_1$ and $\hat{r}_2$, two conversion outcomes can be obtained independently according to (7). If the residual errors are uncorrelated, averaging the two outcomes can provide further SNR improvement. This will be verified in Section V.

V. Measurement

The prototype RNS TDC chip was fabricated in a standard 45-nm CMOS process. A die photograph is shown in Fig. 17. The active area of the chip is 0.08 mm^2 (230 μm $\times$ 350 μm). The two ROs contain 49 stages and 35 stages, and the split-RO structures are clearly shown in the layout screenshot in Fig. 17. The power breakdown of the chip is shown in Fig. 18. The prototype consumes a total power of 24.2 mW from a 1-V supply. Out of this, the two ROs consume 21.2 mW (RO1 consumes 10.5 mW and RO2 consumes 10.7 mW), the DFFs consume 2 mW, and the remaining on-chip digital logics consume around 1 mW. Ideally, the two ROs should consume the same power since the RO power is proportional to the number of edge transmissions during a certain time and the two ROs are otherwise identical except the stage numbers. The difference in power consumption can be attributed to the mismatch. Lacking the matching data from the foundry, we oversized the ROs in this design—it can be further optimized in a future work.

To measure the DNL and INL, two synchronized synthesizers generate two clocks with a 100-Hz frequency offset to create a time ramp signal. A total of 4.5×10^5 samples are collected. As the LSB size is 9.4 ps with a 1-V supply,

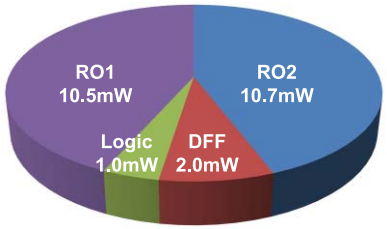

Fig. 18. Power breakdown (8.9-bit mode, $V_{DD} = 1$ V, $f_s = 215$ MS/s).

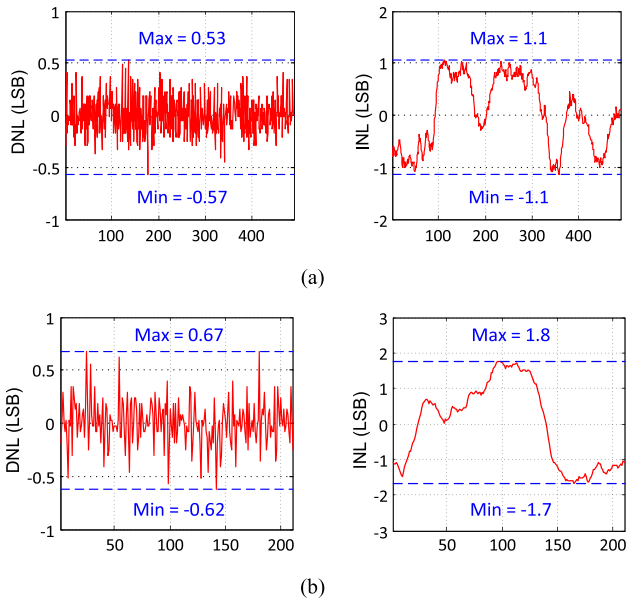

Fig. 19. Measured DNL and INL profiles for (a) and (b) $f_s = 215$ and 500 MHz.

the full input range is 9.4 ps $\times$ 490 = 4.6 ns for a 215-MHz sample rate. The TDC can also run beyond its full-range speed with a decimated conversion range due to its flash nature. As shown in Fig. 19, the DNL and INL at 215 MS/s (8.9-bit 9.4-ps resolution) and 500 MS/s (7.7-bit 9.4-ps resolution) are 0.57/1.1 and 0.67/1.8 LSBs, respectively. One expectation is that due to the random starting phase in this TDC, the non-linearity should show a flat characteristic from the histogram test. However, the measured INL curve exhibits a pattern. The cause of this pattern is analyzed as follows. Due to the large transient current of the readout circuit, large power bounce occurs due to the bond-wire inductance and insufficient on-chip bypass. This is verified by the measured supply voltage showing a 20-mV$_{PP}$ fluctuation in Fig. 20. In our layout, unfortunately, the ROs share the same power supply with the readout circuit and the supply bounce directly couples to the ROs and modulate their stage delays. When the supply voltage levels up, the stage delay of inverter decreases, so a larger code is recorded for the same input, resulting in a positive INL, and vice versa. Fig. 20 shows the power supply voltage and the INL curve together. We note that the shape of the INL is the same as that of the V_{DD}. The problem can be mitigated in a future design by separating the supply voltages for better isolation.

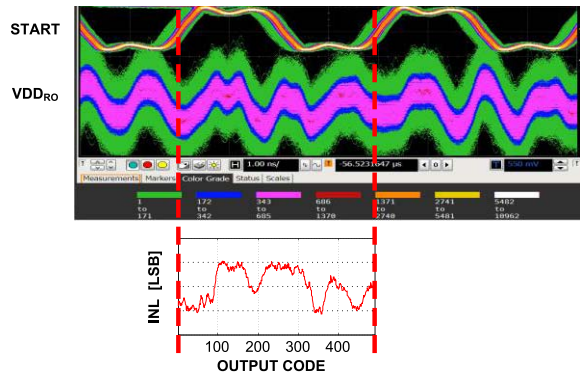

Fig. 20. Measured INL nonlinearity caused by the power supply noise.

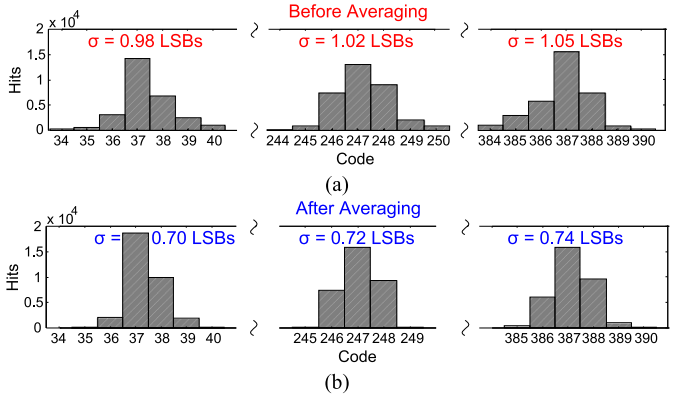

Fig. 21. Measured single-shot code histograms. (a) Before averaging. (b) After averaging.

Another major performance metric for TDC is the single-shot precision (SSP) [19]. To measure SSP, two input signals are routed to the chip from the same signal source with a certain difference of cable length. The measured SSP is shown in Fig. 21(a). As shown in Fig. 21(b), a 3-dB improvement in SNR due to averaging is observed in the SSP measurement as the measured noise standard deviation decreases from 1.05 to 0.74 LSBs, just as we expected. There are several noise sources in the proposed RNS TDC, i.e., the noise of the input signal, the quantization noise, the cumulative jitter in the ROs, the noise due to DEM averaging, and the noise in the DFFs and power supply. The measured SSP of the 35-stage RO is shown in Fig. 22(a). The RMS noise of the input signal is 1.9 ps or 0.20 Δ, and the quantization noise is

$$\sigma_q = \sqrt{\frac{\Delta^2}{12} \times 2} = 0.41\Delta. \tag{16}$$

The other error source σ_{DEM} unique in this design is due to the DEM averaging of the mismatch within the ROs. Assuming that the stage delay of the RO increases from minimum to maximum along a half ring and then decreases to minimum along the other half due to a gradient effect, the expected SSP versus the input is shown in Fig. 22(b). An intuitive observation is that when the input equals zero or any integer oscillation periods, the deviation of the measured code is zero. On the contrary, if the input equals a half period, the deviation will be the largest. This observation predicts the notches at the codes 0, 35, and 140 in the SSP curve in Fig. 22(a). At these

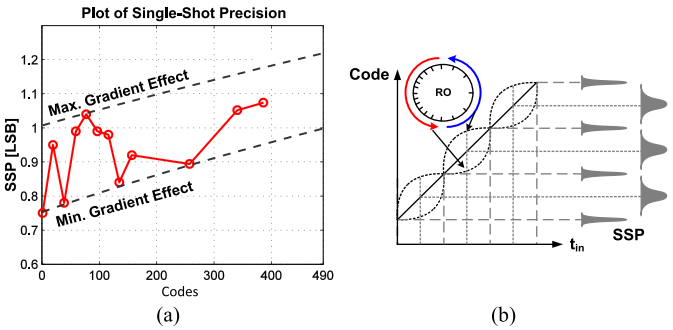

Fig. 22. (a) Measured SSP of the 35-stage RO. (b) SSP versus time input influenced by a gradient effect in the RO.

TABLE II
NOISE BREAKDOWN

Input clock noise, σ_{in}	0.20 Δ
Quantization noise, σ_q	0.41 Δ
Gradient effect error, σ_{DEM}	0 Δ ~ 0.66 Δ (code dependent)
Cumulative jitter, σ_j	0.25 Δ /cycle (code dependent)
Other, σ_{other}	0.60 Δ

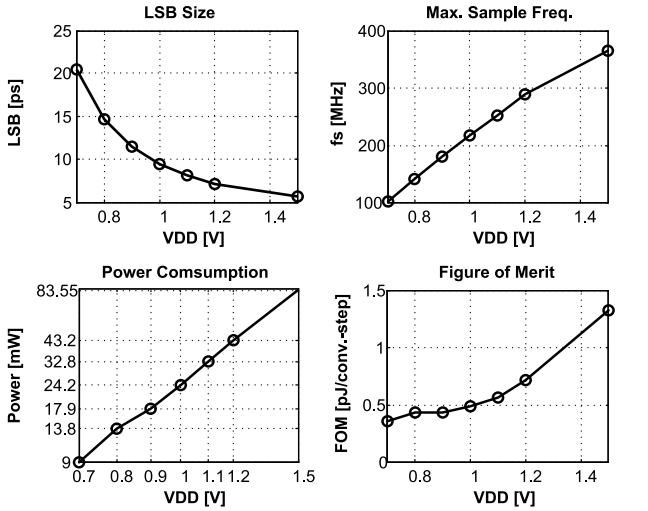

Fig. 23. Measurement results at different supply voltages.

codes, the mismatch averaging induced noise is zero. From the gap between the upper and lower bounds of the SSP curve, a peak value of $((1\Delta)^2-(0.75\Delta)^2)^{1/2} = 0.66\Delta$ is determined, which indicates that the mismatch standard deviation is ~10%. When the RO acts as a time quantizer, the k-cycle cumulative jitter is also of interest—it is proportional to the square root of the time interval between measurements or the input in this case [30]. By fitting the SSP curve to a parabolic function, the one-cycle jitter (at code 70) is determined to be 2.3 ps or 0.25 Δ. A detailed theoretical expression of the jitter and mismatch of the RO and arbiter is derived in [31]. The overall noise breakdown of the TDC is summarized in Table II.

Fig. 23 shows the LSB size, the maximum sampling frequency, the power consumption, and the corresponding

TABLE III
PERFORMANCE SUMMARY AND COMPARISON

	This work		JSSC '10 [7]	JSSC '14 [9]	JSSC '13 [10]	JSSC '13 [32]	ISSCC'15 [33]
Architecture	RNS		2D Vernier	Pipeline	Asyn. Pipeline	Two-Step	Flash
No. of bits	8.94	7.71	7	9	10	7	10
Resolution/ LSB size [ps]	9.4		4.8	1.12	1.76	3.75	1.17
Speed [MSPS]	215	500	50	250	300	200	100
DNL [LSB]	0.57	0.67	<1	0.6	0.6	0.9	0.8
INL [LSB]	1.1	1.8	3.3/1***	1.7	1.9	2.3	2.3
SSP [LSB]	0.74	0.84	N/A	0.69	0.7	N/A	N/A
N_{linear}*	7.86	6.23	4.90/6.00***	7.57	8.46	5.28	8.28
Power [mW]	24.2	27.3	1.7	15.4	115	3.6	0.78
FoM** [pJ/conv.-step]	0.48	0.73	1.14/0.53***	0.33	1.09	0.46	0.025
Area [mm^2]	0.08		0.02	0.14	0.88	0.02	0.036
Technology	45 nm		65 nm	65 nm	130 nm	65 nm	14 nm
Calibration	No		Background	No	Foreground	No	No

* N_{linear} = No. of bits - $\log_2$(INL+1)
** FOM = Power/($2^{Nlinear}fs$)
*** Based on the extrapolated TDC intrinsic INL

figure of merit of the prototype measured at various supply voltages. The measurement results are summarized in Table III and compared to several recent state-of-the-art TDC works operating at a similar speed.

VI. CONCLUSION

The concept, architecture, and experimental results of a 9-bit, 215 MS/s folding-flash RR-RNS TDC are reported. To the best knowledge of the authors, this paper constitutes the first TDC work based on RNS in monolithic forms. RR proves to be essential in realizing an alias-free converter in practice. The principle of RNS conversion is not limited to the time quantization, and has been successfully applied to voltage- and charge-domain data converters recently [16].

APPENDIX
CRT RR-RNS DECODING ALGORITHM

The RR-RNS algorithm proposed in [26] is briefly reviewed as follows. If the first modulus is chosen as the reference, we subtract the first equation from the remaining $L-1$ equations in (7) and obtain

$$\begin{cases} M(q_1\Gamma_1 - q_2\Gamma_2) = \hat{r}_{2,1} \\ M(q_1\Gamma_1 - q_3\Gamma_3) = \hat{r}_{3,1} \\ \quad\quad\vdots \\ M(q_1\Gamma_1 - q_L\Gamma_L) = \hat{r}_{L,1} \end{cases} \tag{17}$$

where $\hat{r}_{i,1} = \hat{r}_i - \hat{r}_1$ for $2 \le i \le L$. The following four steps can uniquely solve for Y.

1) Calculate $\hat{s}_{i,1} = [(\hat{r}_{i,1}/M)]$ from the obtained erroneous remainders for $2 \le i \le L$. The $[\cdot]$ represents the rounding operation.
2) Calculate the remainder

$$\hat{\xi}_{i,1} = \hat{s}_{i,1}\bar{\Gamma}_{i,1} \bmod \Gamma_i, \text{ for } 2 \le i \le L, \tag{18}$$

where $\bar{\Gamma}_{i,1}$ is the modular multiplicative inverse of Γ_1 modulo Γ_i ($\bar{\Gamma}_{i,1}\Gamma_1 \bmod \Gamma_i = 1$).

3) Substitute the remainder $\hat{\xi}_{i,1}$ and estimate q_1 by $\hat{q}_1$

$$\hat{q}_1 = \sum_{i=2}^{L} \hat{\xi}_{i,1} b_{i,1} \frac{\Gamma}{\Gamma_1\Gamma_i} \bmod \frac{\Gamma}{\Gamma_1}, \tag{19}$$

where $b_{i,1}$ is the modular multiplicative inverse of $(\Gamma/\Gamma_1\Gamma_i)$ modulo Γ_i.
4) Finally, obtain Y using

$$Y = \hat{q}_1\Gamma_1 M + \hat{r}_1. \tag{20}$$

Take the example in Section III-A, the redundant modulus set and the remainder set are $\{M\Gamma_1 = 50,\ M\Gamma_2 = 70\}$ and $\{r_1 = 16,\ r_2 = 16\}$, respectively. For an input $X = 16$, if remainder errors are introduced, i.e., $\Delta r_1 = 1$ and $\Delta r_2 = -1$, we have $\{\hat{r}_1 = 17, \hat{r}_2 = 15\}$. For the dual-moduli system, if the modulus 50 is chosen as the primary (i.e., to recover q_1 instead of q_2), according to (17), we have

$$10 \times (5q_1 - 7q_2) = -2. \tag{21}$$

The first step shows that $\hat{s}_{2,1} = [-2/10] = 0$, and $\bar{\Gamma}_{2,1} = 3$ according to $\bar{\Gamma}_{2,1} \times 5 \bmod 7{=}1$. Substitute these variables into (18), we have $\hat{\xi}_{2,1} = 0 \times 3 \bmod 7 = 0$ and $\hat{q}_1 = 0$. In this case, the final output Y is 17; alternatively, Y is 15 if the modulus 70 is chosen instead.

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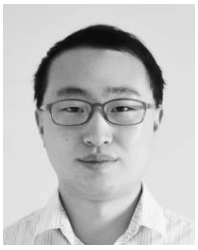
Dr. Wu was a recipient of the NXP Fellowship from TU Delft in 2007 and 2008, the Analog Devices Outstanding Student Designer Award in 2012, and the CICC Student Scholarship Award in 2014.



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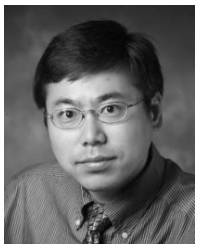
He is currently with Broadcom Ltd., Irvine, CA, USA. His current research interests include high-resolution ADCs and digital calibration techniques for data convertors.



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