

A Monolithically Integrated Large-Scale Optical Phased Array in Silicon-on-Insulator CMOS

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Abstract—A large-scale monolithic silicon nanophotonic phased array on a chip creates and dynamically steers a high-resolution optical beam in free space, enabling emerging applications in sensing, imaging, and communication. The scalable architecture leverages sub-array structure, mitigating the impact of process variation on the phased array performance. In addition, sharing control electronics among multiple optical modulators in the scalable architecture reduces the number of digital-to-analog converters (DAs) required for an N^2 array from $\mathcal{O}(N^2)$ to $\mathcal{O}(N)$, allowing a small silicon footprint. An optical phased array for 1550-nm wavelength with 1024 uniformly spaced optical grating antennas, 1192 optical variable phase shifters, and 168 optical variable attenuators is integrated into a 5.7 mm × 6.4 mm chip in a commercial 180-nm silicon-on-insulator RF CMOS technology. The control signals for the optical variable phase shifters and attenuators are provided by 136 DAs with 14-bit nonuniform resolution using 2.5-V input–output transistors. The implemented phased array can create 0.03° narrow optical beams that can be steered unambiguously within ±22.5°.

Index Terms—Lidar, nonlinear digital-to-analog converter (DAC), optical beam steering, optical beamforming, optical phased array, silicon photonics, silicon-on-insulator (SOI) CMOS, thermo-optic modulation.

I. INTRODUCTION

SHAPING and steering optical beams in a compact device with ultrahigh resolution and fast speed enable emerging applications in sensing, imaging, communication, and display. Conventional optical beam-steering solutions have been largely based on mechanical mechanisms. For instance, while a mechanically rotating mirror is used in 3-D ranging sensors, such as commercial lidars [1], an array of integrated micro-electromechanical system mirrors is used for projection displays [2]–[4]. Mechanical optical steering solutions are generally slow and susceptible to physical wear and tear as well as vibration. Depending on the realization, these mechanical

Manuscript received May 7, 2017; revised August 6, 2017; accepted September 11, 2017. Date of publication October 18, 2017; date of current version December 26, 2017. This paper was approved by Guest Editor Pui-In Mak. This work was supported in part by the Viterbi Postdoctoral Fellowship and in part by the MOSIS Service. (*Corresponding author:* SungWon Chung.)

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Digital Object Identifier 10.1109/JSSC.2017.2757009

beam-steering systems are bulky, consume significant energy, and have a limited steering capability. Furthermore, these mechanical approaches are only capable of steering a light beam, and are incapable of forming arbitrarily shaped light beams as needed for advanced communication and sensing applications. Non-mechanical optical beam steering is possible by modifying the effective refractive index of a transmissive (e.g., prism) or reflective (e.g., grating) structure. Liquid crystal spatial light modulators [5]–[7] and acousto-optic spatial light modulators [8] are the examples of such commercial systems (e.g., holographic displays).

Monolithic integration of nanophotonic devices and advanced electronic devices on a single chip is bringing up a new opportunity to realize an innovative electro-optic solution on optical beamforming. Electromagnetic wavefront can be arbitrarily formed by a phased array, which consists of spatially separated antennas each with an independent control of phase and amplitude of the signal. At radio frequencies, single-chip phased arrays, demonstrated first in 2004 [9], have now become mainstream with commercial products for automobile radars and wireless communications. At optical frequencies, electronically controlled solid-state optical phased arrays [10]–[21] have been demonstrated since 1990s with less than 128 array elements by either heterogeneous or monolithic integration.

A large-scale implementation of an optical phased array has seen strong demand in order to satisfy the need of high beam resolution and wide beam-steering range for emerging applications, such as self-driving cars and drones. As Section II will explain, shaping a narrow optical beam for high-resolution steering requires physically a large antenna array, while wide beam steering requires a narrow antenna pitch comparable with the short optical wavelength of electromagnetic radiation through the antenna array. As the number of array elements grows, electronic control signal routing for variable optical phase shifters occupies increasingly larger area. The monolithic integration platforms based on silicon on insulator (SOI) or bulk silicon substrate have a potential to economically realize a large-scale optical phase array in a compact form factor.

Device mismatch due to process non-uniformity [22]–[24] is a fundamental limiting factor preventing the realization of a monolithically integrated large-scale optical phased array with a conventional architecture. The need of electro-optical calibration circuitry [25], which mitigates such undesirable

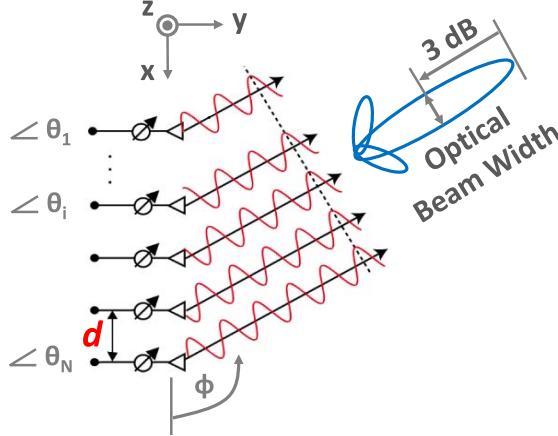


Fig. 1. 1-D uniform optical phased array with N elements.

impacts of mismatch, significantly increases the complexity of a large-scale optical phased array. A monolithically integrated very large-scale optical array with a small antenna pitch, therefore, does not exist. Previously reported large-scale optical phased arrays with 4096 antennas [13] and 1024 antennas [26] are static without ability to steer an optical beam to a desired location. The largest tunable optical phased array reported to date [21] has only 128 array elements.

This paper introduces a large-scale optical phased array architecture leveraging a hierarchical sub-array structure, and presents a monolithically integrated 1024-element optical phased array prototype in a commercial SOI CMOS process. The proposed architecture is independent of a specific monolithic integration platform and allows the sharing of control electronics among multiple variable optical phase shifters, so that compact silicon implementation is allowed with relatively simple metal interconnections for control electronics. The design parameters of the proposed architecture are determined based on the quantifiable impact of optical device nonidealities on the system-level performance of optical phased arrays.

The organization of this paper is as follows. Section II discusses the impact of process mismatch on the optical phased array performance, which limits the scalability of conventional optical phased array architecture. Section III introduces the proposed large-scale optical phased array architecture. Section IV presents the optical devices and electronic control circuits of a 1024-element 1-D optical phased array prototype chip. Test chip implementation and experimental characterization setup are described in Section V, presenting the measured results in Section VI. Conclusions are stated in Section VII.

II. DESIGN CONSIDERATIONS

The beam-steering range and the beamwidth of monolithically integrated large-scale optical phased arrays are limited by factors, including effective antenna aperture size, device mismatch, optical crosstalk, and noise.

To facilitate quantitative analysis on these optical phased array performance limitations, the beam-steering range and the beamwidth of a 1-D uniform array (Fig. 1) are formulated.

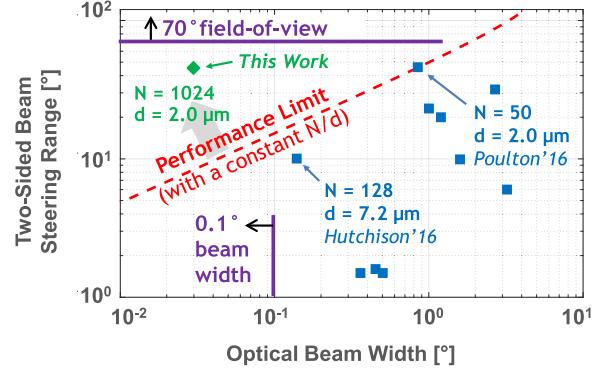


Fig. 2. Design tradeoff between beam-steering range and beamwidth for a constant N/d , where N is the number of antennas and d is the antenna pitch in a uniform optical phased array.

Suppose that the number of antennas in the array is N , and the distance between two adjacent antennas is a constant d . In a standard beamforming scheme, each antenna radiates the same power with a linear phase progression across the uniform array.

The unambiguous optical beam-steering range $\Delta\phi$ without grating lobes in the broadside radiation is given by

$$-\sin^{-1}\left(\frac{\lambda}{2d}\right) < \Delta\phi < \sin^{-1}\left(\frac{\lambda}{2d}\right). \quad (1)$$

A complete $\pm 90^\circ$ unambiguous beam-steering range is achieved with a half-wavelength ($\lambda/2$) antenna pitch. Given the short wavelength of optical frequencies, the antenna pitch must be extremely small to enable a meaningful steering range. For instance, if an unambiguous azimuthal steering angle of at least $\pm 35^\circ$ is necessary, the antenna pitch of an optical phased array operating at the 1550-nm wavelength should be less than 1350 nm.

The width of the main lobe at the half-power level of the array radiation intensity represents the optical beam resolution. The beamwidth of the uniform array is narrowest with the broadside radiation ($\phi = 90^\circ$) and broadens as the steering angle increases toward the endfire

$$\Delta\bar{\phi}_{3-\text{DB}} = \frac{c_1}{\sin\phi_0} \frac{\lambda}{Nd} \quad (2)$$

where the constant c_1 is the solution of $\sin(\pi x)/x = \pi/\sqrt{2}$, which is often approximated to 0.886, and ϕ_0 is the beam-steering angle. This expression shows that a relatively large effective array aperture size Nd , compared with the wavelength λ , is desirable in order to achieve a narrow beamwidth. High-resolution 3-D sensing requires a very fine spatial resolution. For instance, the resolution of a phased array lidar for automotive applications should be better than 0.1° for object identification at 200 m, which in turn requires more than 689 antennas with the 1350-nm pitch for $\pm 35^\circ$ beam steering. To meet this requirement, 0.08° beamwidth at the broadside is necessary, which achieves 0.1° beamwidth with $\pm 35^\circ$ steering angle.

Table I exemplifies the beam-steering range and the minimum 3-dB beamwidth of example uniform phase array

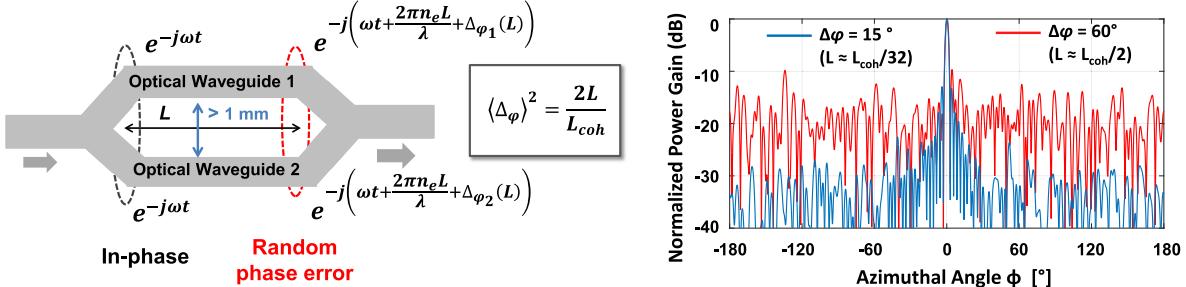


Fig. 3. Optical phase coherence length causing a relative random phase error on optical waveguide, which adversely affects the far-field noise floor of optical phased arrays with a long waveguide routing to the array antennas.

TABLE I
BEAM-STEERING RANGE AND MINIMUM BEAMWIDTH OF UNIFORM
OPTICAL PHASED ARRAYS WITH ISOTROPIC ANTENNAS

Number of Antennas	Antenna Spacing ¹	Steering Angle	Min. Beam Width
100	\$2\lambda\$	\$\pm 13.5^\circ\$	0.254°
100	\$\lambda\$	\$\pm 30.0^\circ\$	0.508°
100	\$\lambda/2\$	\$\pm 90.0^\circ\$	1.016°
1,000	\$2\lambda\$	\$\pm 13.5^\circ\$	0.025°
1,000	\$\lambda\$	\$\pm 22.5^\circ\$	0.051°
1,000	\$\lambda/2\$	\$\pm 90.0^\circ\$	0.102°

¹ \$\lambda\$ is the radiation wavelength from the optical phased array.

configurations with isotropic antennas with the 1550-nm wavelength.

A. Effective Antenna Aperture Size

The effective antenna aperture size \$Nd\$ not only determines the minimum chip size but also sets the beamwidth as in (2). A desirable design goal for a given effective antenna aperture size \$Nd\$ is, therefore, to maximize a quantity \$\kappa = 2|\Delta\phi|/\Delta\bar{\phi}_{3-\text{DB}}\$, intending to have a large unambiguous beam-steering range by having a small beamwidth. For an antenna pitch larger than \$\lambda/2\$, the quantity \$\kappa\$ can be approximated to \$N/d\$ by using a Taylor series expansion on (1) and taking the largest steering angle \$\psi_0 = |\Delta\phi|\$. This analysis agrees with intuitive expectation that a small antenna pitch \$d\$ is desirable for a given number of antennas \$N\$.

Fig. 2 visualizes the tradeoff between beam-steering range and beamwidth for the largest value of \$\kappa \simeq N/d\$ from [21], showing the best performance of monolithically integrated optical phased arrays is the orders of magnitude worse than what is needed for many emerging applications, such as automotive phased array lidars.

B. Mismatch

With micrometer-scale short wavelength in optical frequencies, mismatch leads to a random phase error in optical waveguides [24]. This random phase error does not average out but takes a random walk with its mean-square value increasing with a waveguide length [27]. When a coherent light with a wavelength \$\lambda\$ propagates in a waveguide of length \$L\$,

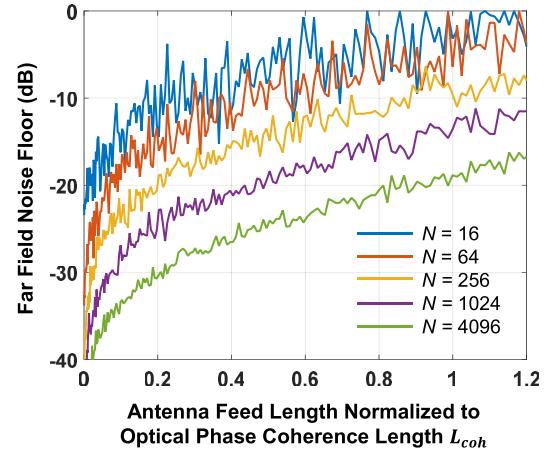


Fig. 4. Far-field noise floor variations in a uniform optical phased array with \$N\$ elements due to finite optical coherence length.

the random phase error is given by

$$\Delta\phi(L) = 2\pi \int_0^L \left(\frac{\lambda}{\Delta n_e(l)} \right)^{-1} dl = \frac{2\pi}{\lambda} \int_0^L \Delta n_e(l) dl \quad (3)$$

where \$\Delta n_e\$ is the deviation of an effective refractive index from its average value for an infinitesimal section of the waveguide at location \$x = l\$. Note that \$\lambda/\Delta n_e(l)\$ in the integral corresponds to the deviation of light travel distance within the infinitesimal section and is normalized to the wavelength of the light propagating within the waveguide core.

Optical phase coherence length is a parameter to quantify the random phase error in optical waveguides. The laser community defines the optical phase coherence length \$L_{coh}\$, such that the following relation on the expectation of the random phase error holds [28], [29]:

$$E \left[e^{i\Delta\phi(L)} \right] = \int_{-\infty}^{\infty} f_{\Delta\phi}(x) e^{ix} dx = e^{-L/L_{coh}} \quad (4)$$

where the probability density function \$f_{\Delta\phi}(x)\$ on the random phase error is a Gaussian distribution with zero mean and standard deviation \$\sigma\$. This definition indicates that, with a Mach-Zehnder interferometer (MZI) consisting of two identical waveguides with a length \$L = L_{coh}\$ as shown in Fig. 3, the average intensity at the MZI output is lower than the input light intensity by a factor of \$(1+e^{-1})/2 \simeq 0.6839\$. To suppress such random intensity decrease below 1 dB, the waveguide

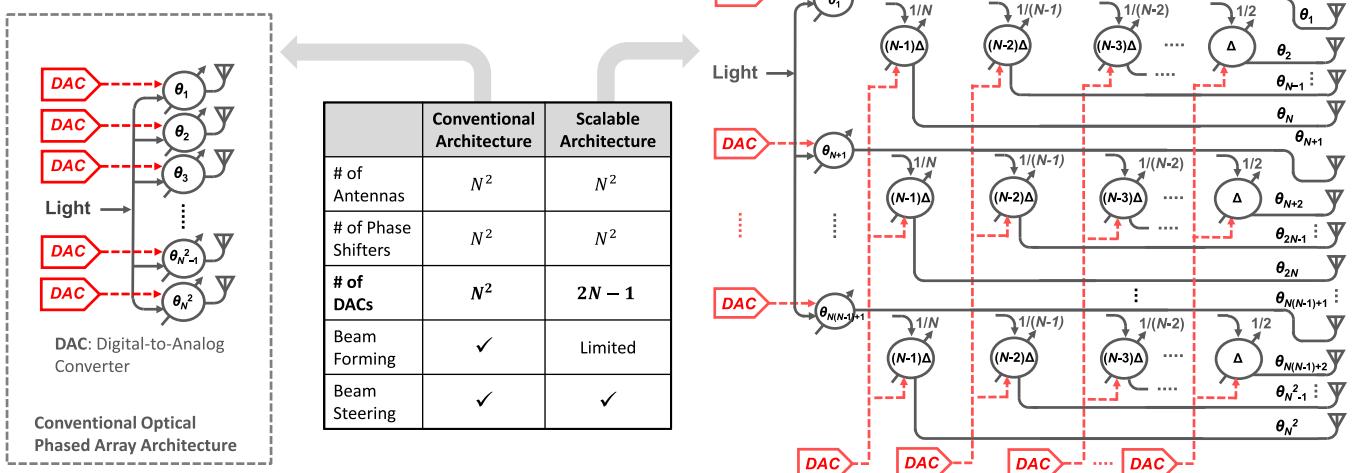


Fig. 5. Scalable optical phased array architecture, which reduces the silicon footprint of control electronics from $\mathcal{O}(N^2)$ to $\mathcal{O}(N)$ for a 1-D uniform array with N^2 elements, in an ideal monolithic integration technology with infinite optical phase coherence length.

length should be shorter than $L_{coh}/2$. This definition can be used to show that the root mean square of the random phase error $\Delta\phi(L)$ is given by $\sqrt{2L/L_{coh}}$ [27], which finds that an optical waveguide with $L = L_{coh}/2$ introduces approximately 60° root-mean-square phase error between the two waveguides of the MZI.

Characterization of optical phase coherence length in silicon photonics has shown several interesting observations [23], [24], [30]–[32]. First, the typical optical phase coherence length in modern silicon photonics technologies based on the SOI wafer is known as 4–5 mm [24]. This means that, in order to suppress the intensity variation of an MZI with two identical waveguides less than 3 dB, the waveguide length should be less than approximately 1.5 mm. Second, interestingly, optical phase coherence length is loosely related to the waveguide insertion loss [24], [30], which implies that the two waveguides with the same insertion loss can have a significantly large difference in optical phase coherence length. For instance, [24] observed that rib waveguides have a two to three times shorter optical phase coherence length compared with strip waveguides with a similar insertion loss. This indicates that the rib waveguides are more sensitive to process variations than the strip waveguides. Third, when optical waveguides are close to each other within 700–1000 μm distance [23], [24], [32], it is commonly observed from a wafer-level characterization of optical ring resonators and MZIs that the refractive index of the optical waveguide core material has statistically strong correlation. In other words, the accumulated random phase errors of geometrically close waveguides are negligible. Due to this spatial correlation, optical phase coherence is typically measured using an MZI whose two waveguide legs are separated by more than 1 mm. With the proposed large-scale optical phased array architecture, we take advantage of the spatial correlation by sharing control electronics for multiple optical modulators that are spatially close to each other.

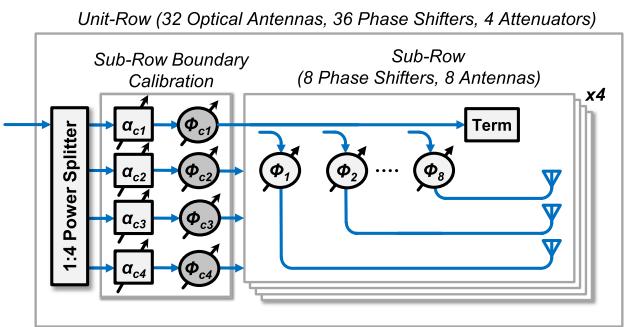


Fig. 6. 32-element example of sub-array architecture to overcome limitation from finite optical phase coherence length.

In a large-scale optical phased array, the antenna feed consists of a large number of long optical waveguides that run in parallel from variable optical phase shifters to antennas, and thus accumulated random phase error within the long waveguides should be considered. Fig. 3 shows the behavioral simulation results on the impact of random phase error on a 128-element uniform array with $\lambda/2$ antenna pitch. The simulation results show that 60° random phase error from an antenna feed with a length of $L_{coh}/2$ increases the far-field noise floor to -10 dB. Additional behavioral simulations show that the random phase error has little impact on beam steering and beamwidth. Simulation (Fig. 4) also shows that the number of array elements affects the impact of the random phase error on the far-field noise floor. To avoid the noise floor degradation, static phase calibration is necessary to each array element.

III. SCALABLE OPTICAL PHASED ARRAY ARCHITECTURE

A. Challenges in Conventional Architecture

A conventional optical phased array architecture (Fig. 1) has a limited scalability with monolithic integration primarily

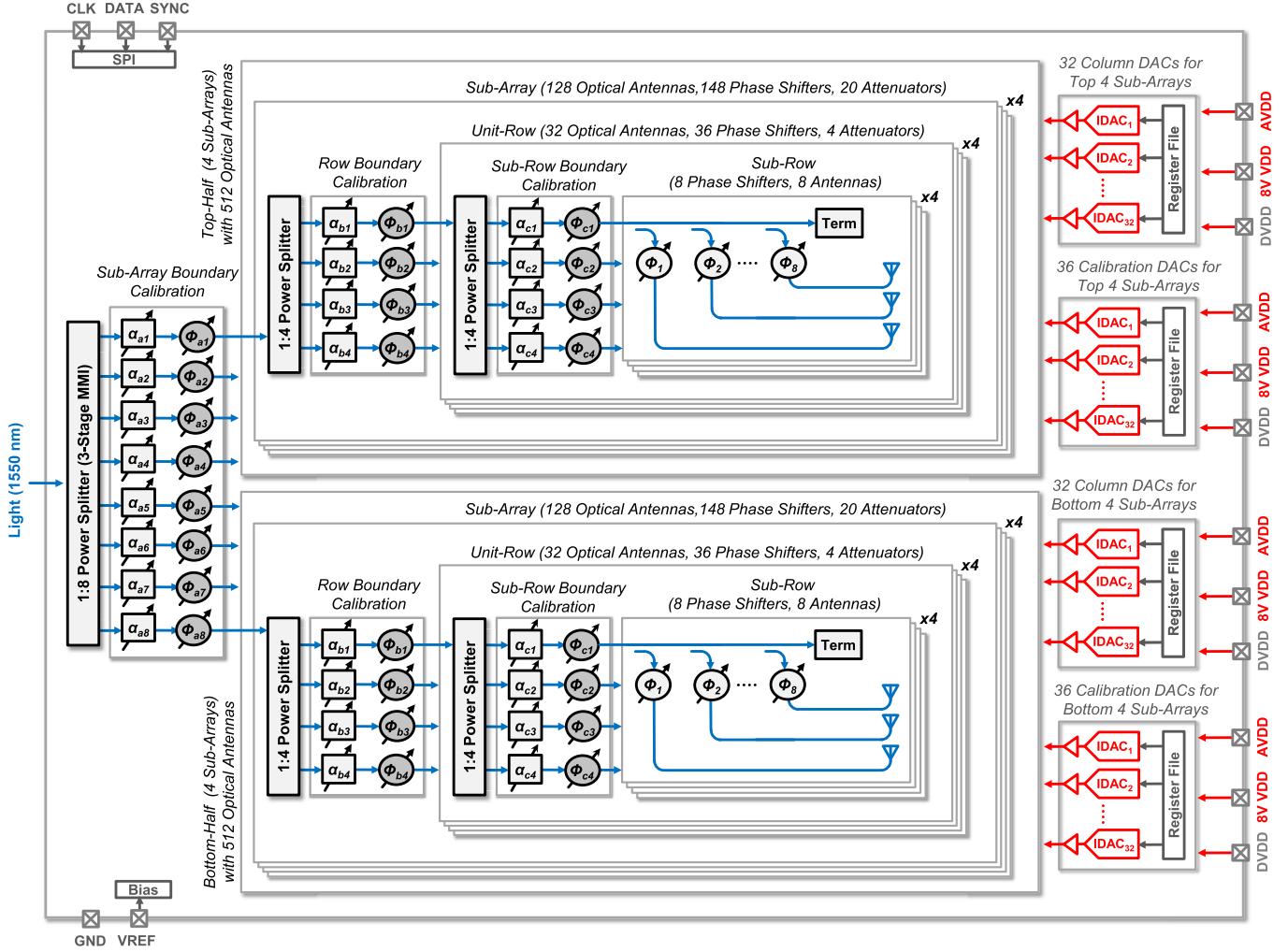


Fig. 7. Proposed scalable architecture with 1024 array elements, overcoming the array size limitation due to finite optical phase coherence length by exploiting a hierarchically nested sub-array structure.

due to control electronics and finite optical phase coherence length.

Optical phase coherence length sets the fundamental limit on the scalability of electronically tunable optical phased arrays in conventional architecture. The most compact realization of an array element (consisting of a 360° optical variable phase shifter, an optical variable attenuator, and an optical antenna) for a 2-D optical phased array in a monolithic integration platform is approximately $30 \mu\text{m} \times 30 \mu\text{m}$ [19]. If the technology provides an optical phase coherence length L_{coh} of 4 mm, 64 array elements with the $30\text{-}\mu\text{m}$ pitch need $1920\text{-}\mu\text{m}$ length waveguides for optical interconnects, corresponding to $0.48L_{\text{coh}}$. As discussed in Section II-B, this results in 57° root-mean-square random phase error accumulation, leading to a sidelobe level greater than -10 dB, as shown in Fig. 4. For a larger 128-element array with the same pitch, the sidelobe power level further grows to approximately -7 dB level, since the waveguide length doubles to $0.96L_{\text{coh}}$. This is a significant limitation in array size scalability with the conventional array architecture.

B. Proposed Scalable Architecture

This paper, for the first time, proposes a scalable optical phased array architecture for monolithic integration, where, for linear beam steering, N^2 optical variable phase shifters can be controlled by using $\mathcal{O}(N)$ digital-to-analog converters (DACs) in an N^2 -element optical phased array while overcoming array scalability limitation due to finite optical phase coherence length.

In the proposed architecture (Fig. 5), the N^2 variable phase shifters are placed in an $N \times N$ array. To briefly introduce the key idea, infinite optical phase coherence length is assumed for the proposed architecture exemplified in Fig. 5. The idea is to create a linear phase progression between adjacent columns, and also between the rows. The $N - 1$ variable phase shifters in each column are in-sync and driven by a single column-control current DAC. The relative phase shifts between the rows are set by N variable phase shifters at the beginning of each row. In each row, cascaded couplers with progressively increasing coupling ratio are used to equally distribute the optical signal to all the row variable phase shifters. The reduced number of

required DACs from $\mathcal{O}(N^2)$ to $\mathcal{O}(N)$ with N^2 array elements can increase the number of array elements in $36\text{ mm} \times 24\text{ mm}$ SOI CMOS chip from 360 to 1.3 million or reduce the chip area for 360 array elements from 864 mm^2 to 46 mm^2 . To further reduce the silicon area requirement for control electronics, the prototype chip uses nonlinear DACs presented in Section IV-F.

Fig. 6 shows an example of the proposed sub-array structure to overcome the array size limitation due to finite optical phase coherence length. Based on the measured optical phase coherence length of a similar SOI waveguide [24], the optical phase coherence length L_{coh} is estimated to around 4 mm. The sub-array consists of multiple optical variable phase shifters whose input is equally split from the common optical input port using cascaded optical directional power couplers. The waveguide length within the sub-row is $600\text{ }\mu\text{m}$, which is constant for all phase shifters. Since this is shorter than optical phase coherence length, as long as the sub-row boundary calibration is performed, the phase relation between the input signal and the multiple output signals of the sub-array is consistent with a bounded error.

Fig. 7 shows the proposed scalable optical phased array with 1024 elements for monolithic integration platforms with finite optical phase coherence length. In overall, three levels of nested sub-array structures are used to calibrate out both random phase error due to finite optical phase coherence length and static phase error due to systematic optical path difference. The 1024-element array is divided into eight top-level sub-arrays of 128 elements. Each top-level sub-array is divided into 4 unit rows (mid-level sub-arrays) of 32 elements, where each unit row is divided into 4 sub-rows (lower level sub-arrays) of 8 elements. In addition to the 1024 optical variable phase shifters connected to 1024 optical antennas, 168 optical variable phase shifters and 168 optical variable attenuators controlled by additional 72 DACs are used to manage process variation between sub-arrays, unit rows, and sub-rows as well as static optical path differences.

Each row (mid-level sub-array) has a common input and splits it into four sub-rows (i.e., lower level sub-array) as well as calibrates the phase offsets among the four sub-rows. Hence, the input-output (I/O) relation of the row is consistent regardless of the optical waveguides connecting the four sub-rows even beyond the optical phase coherence length.

In a similar way, each sub-array (top-level sub-array) has a common input and splits it into four rows (mid-level sub-array) as well as calibrates the phase offsets among the four rows. The proposed architecture takes the advantage of spatial correlation by closely placing multiple sub-arrays. Note that each row has 32 elements that are placed in a horizontal direction. The $134.5\text{-}\mu\text{m}$ vertical size of the row is significantly smaller than the horizontal size, so that the overall vertical size of the sub-array ($538\text{ }\mu\text{m}$) is still smaller than the horizontal size of a row as well as optical phase coherence length. Therefore, all four optical variable phase shifters in one of 32 columns in a sub-array can be driven by the same DAC.

The eight top-level sub-arrays are divided into two groups each with 512 elements, such that the vertical size of each group (four top-level sub-arrays), which is $1.61\text{ }\mu\text{m}$, is smaller

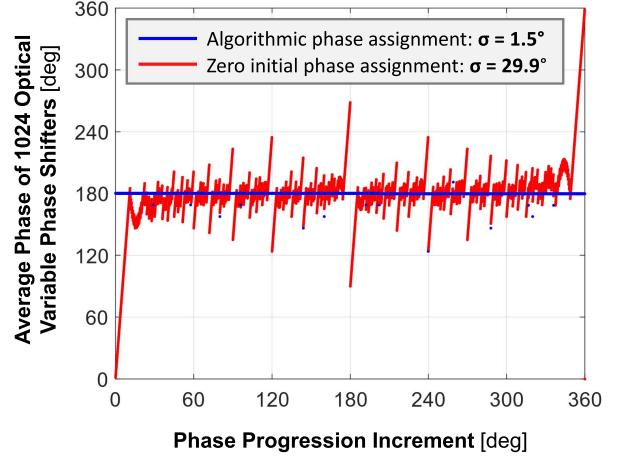


Fig. 8. Algorithmic phase assignment with the 1024-element optical phased array prototype for a varying phase progression among the adjacent phase shifters, which reduces the thermal gradient over the chip.

than the optical phase coherence length. If the vertical size of each group is less than 2.2 mm with $L_{coh} = 4\text{ mm}$ or equivalently less than 1.65 mm with $L_{coh} = 3\text{ mm}$, the root-mean-square random phase error at the antenna feed is less than 60° . Although this seems a fairly large error, the impact of this phase error on the beamwidth and the beam-steering accuracy is shown negligible by behavioral simulation as discussed in Section II-B owing to randomness of the error. The simulated far-field noise floor level is -18 dB below the main lobe.

The array calibration performed on optical variable phase shifters and optical variable attenuators at the sub-array boundary not only compensates the optical path length difference among the sub-arrays but also cancels out a random phased error accumulated in each sub-array. The calibration process also finds a static phase offset for each of the eight optical variable phase shifters in the low-level sub-arrays. A relevant phase offset compensates a deterministic phase shift introduced by each of the optical directional couplers in a low-level sub-array. Since each beam position results in a unique thermal gradient over the chip, for accurate beam control, the array calibration is necessary for each of all the possible beam-steering angles.

With the proposed large-scale optical phased array (Fig. 7), by adding another layer of sub-array structure, the accumulation of a random phase error can be bounded to a desirable limit without regardless of the physical size of the array. In other words, the array size is not limited by the random phase error accumulation. Instead, the optical power loss of long silicon waveguides becomes a limiting factor on the maximum physical size of an optical phased array with the proposed architecture.

C. Phase Allocation for Low Thermal Gradient

For a physically compact realization of optical phase modulation with a low insertion loss and a wide optical bandwidth, thermo-optic modulators are often used with monolithically integrated large-scale optical phased arrays [13]. With the

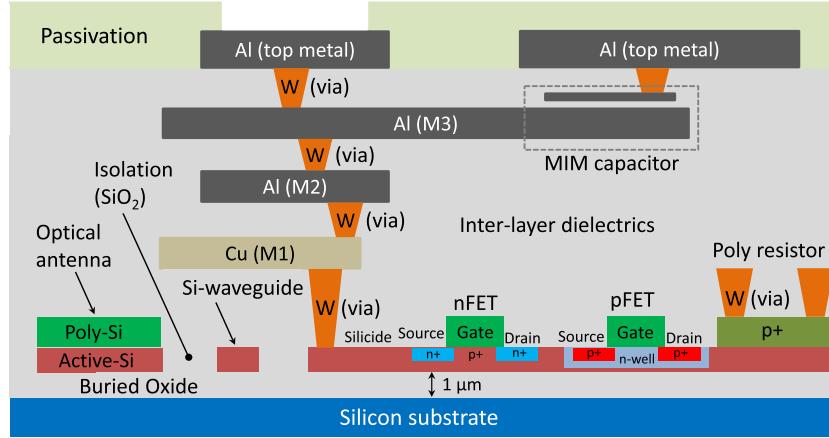


Fig. 9. Cross-sectional diagram of a 180-nm SOI CMOS technology, which can monolithically integrate nanophotonic devices and electrical devices for large-scale optical phased arrays.

proposed scalable array architecture, which does not have a complete degree of freedom to control all optical phase shifters in the array, it is imperative to have a low thermal gradient over the optical variable phase shifters that are driven by the same current DAC. The phase disturbance to each of these phase shifters due to the unwanted thermal gradient should be small compared with the random phase error accumulation due to finite optical coherence length.

An algorithm on phase allocation, which exploits a degree of freedom in assigning phase to each optical variable phase shifter, can significantly reduce the variation of the chip temperature regardless of beam-steering direction. For a linear phase progression in a uniform array, the phase of the first array element can be arbitrarily chosen without affecting the beam-steering direction. In N -element array with the proposed scalable architecture (Fig. 5), the phase of n th variable optical phase shifter output ($1 \leq n \leq N$) is given by

$$\theta_n = \theta_1 + (n - 1) \cdot \Delta\theta - 2\pi \left\lfloor \frac{\theta_0 + (n - 1) \cdot \Delta\theta}{2\pi} \right\rfloor + c_n \quad (5)$$

where $\Delta\theta$ is the phase progression and c_n is the necessary calibration for the n -phase shifter due to the static optical path difference associated with the phase shifter. The phase of the first variable optical phase shifter output θ_1 can be chosen by minimizing the average variance of the total phase sum of the first row for all possible values of $\Delta\theta$

$$\theta_1 = \arg \min_{\theta_1 \in [0, 2\pi]} \left[E \left(\text{Var} \left(\sum_{n=1}^R \theta_n(\Delta\theta) \mid \Delta\theta \right) \right) \right] \quad (6)$$

where R is the number of phase shifters in a row. Since the power consumption of thermo-optic phase modulators is a linear function of the modulated phase angle, minimizing the phase sum variance consequently minimizes the variation of the total power consumption of all optical variable phase shifters on a chip. Fig. 8 shows the reduction in the variation of the phase sum by using this algorithm for a 1024-element optical phase array. Compared with the conventional phase assignment method where the first phase is constant, the proposed technique reduces the variance of average phase shift

at each antenna from 29.9° to 1.5° . With the prototype optical phased array based on thermo-optic variable phase shifters, this result corresponds to the reduction of variation in the power consumption from 16.6% to 0.8%, which proportionally reduces the thermal gradient.

IV. BUILDING BLOCKS: NANOPHOTONIC DEVICES AND ELECTRONIC CIRCUITS

A. Optical Waveguide

The optical waveguide of the prototype optical phased array for 1550-nm wavelength is designed with 540-nm width and 145-nm thickness for single-mode operation in a monolithic integration platform whose cross section is shown in Fig. 9. The designed waveguide geometry allows a single TE-mode propagation only. In order to improve the mode confinement in the waveguide core such that the impact of sidewall roughness, which causes optical insertion loss, can be reduced, the waveguide width is chosen slightly larger than typical 450–500 nm width waveguides for the 1550-nm wavelength. Both straight and bend waveguides on the SOI CMOS technology are experimentally characterized using an MZI-based test structure [33], [34]. Measured results show that the straight waveguide with 540 nm × 145 nm cross section has 1.27-dB/mm optical loss, the 180° bend waveguide with 2-μm radius has 0.7 dB optical loss, and the 180° bend with 5-μm radius shows a lower optical loss of 0.2 dB.

B. Optical Directional Coupler

For large-scale optical phase arrays with dense optical waveguide routing, optical directional couplers split and combine optical power, allowing the most compact realization of sub-array structure among classical passive optics devices.

Fig. 10 shows the optical directional couplers designed to distribute optical signal to phase shifters in the prototype array. The coupling length L_c is the length of the region where the two waveguides are closest to each other, which determines how much optical power is transferred from one waveguide to the other. Up to the length L_π , at which complete power transfer

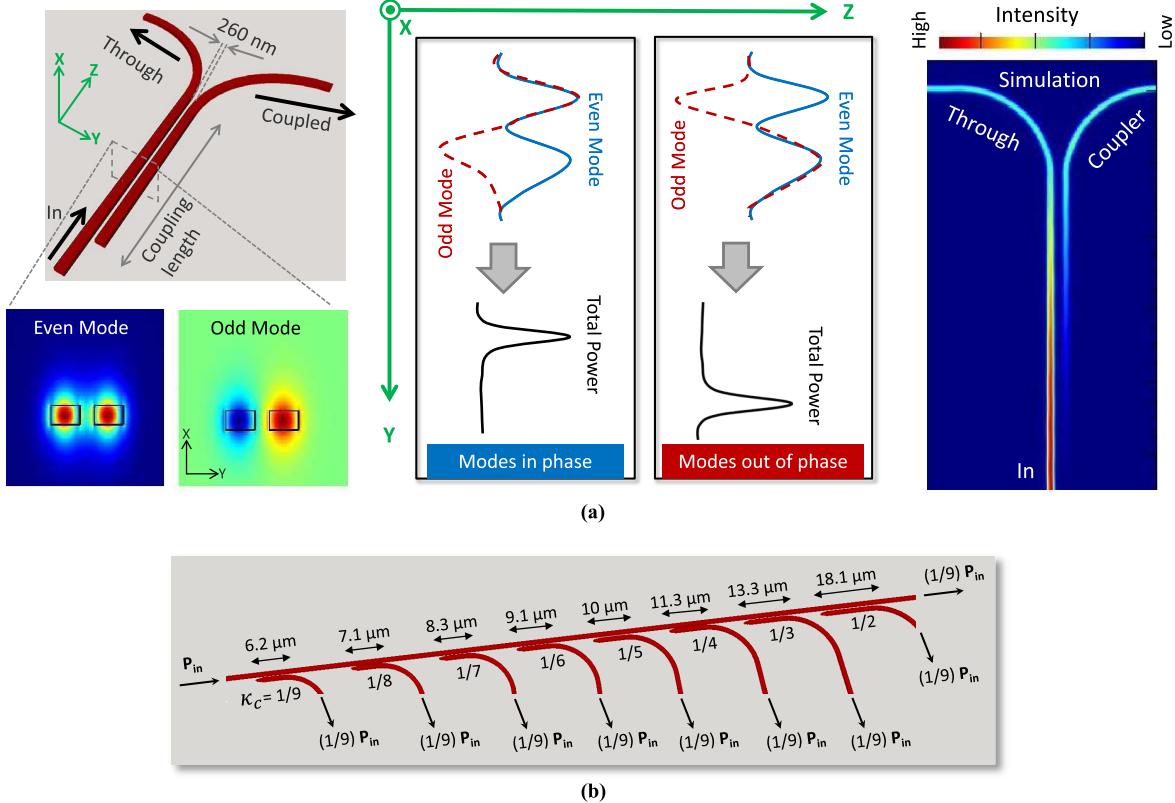


Fig. 10. Optical directional coupler in the monolithic integration platform. (a) 50:50 coupler design. (b) Designs with asymmetric coupling ratios for the sub-array optical signal distribution.

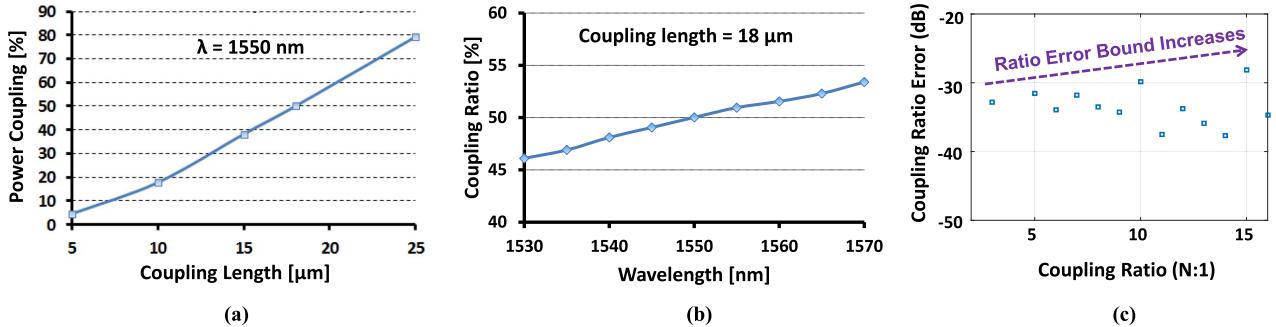


Fig. 11. Measured optical directional coupler characteristics. (a) Power coupling ratio depending on coupling length. (b) Power coupling ratio depending on wavelength. (c) Power coupling ratio error due to technology grid size.

occurs, the longer the coupling length, the more optical power is transferred to the output port. The optical power coupling ratio κ_c is obtained from coupled mode theory [35] as

$$\kappa_c = \sin^2 \left(\frac{\pi}{2} \frac{L}{L_\pi} \right) \quad (7)$$

and L_π is a function of the gap g between the two waveguides given by $L_\pi = c_1 e^{-c_2 g}$.

To distribute an optical input signal to multiple optical variable phase shifters in an array, multiple optical power couplers are cascaded in series [see Fig. 10(b)]. As the number of the phase shifters increases, the optical directional couplers need to tap relatively smaller amount of optical power, which in turn requires a shorter coupling length. As the coupling

length L_c gets smaller and approaches the technology grid size Δ_0 , which is 10 nm in the 180-nm SOI CMOS technology, the deviation of the power coupling ratio from a desired value increases due to the technology grid size limitation. Such a power coupling ratio error e_c is obtained as

$$e_c = \left| 1 - \left[\sin^2 \left(\frac{\pi \Delta_0 \lfloor L_c / \Delta_0 \rfloor}{2c_1 e^{-c_2 g}} \right) \right] \right| \quad (8)$$

where c_1 and c_2 are constants, which depend on the waveguide geometry and wavelength. Fig. 11(c) shows that the power coupling error e_c fluctuates and the peak error gradually increases as the coupling length L_c gets shorter. Since the compact realization of sub-array structure is important due to finite optical coherence length, the optical direction

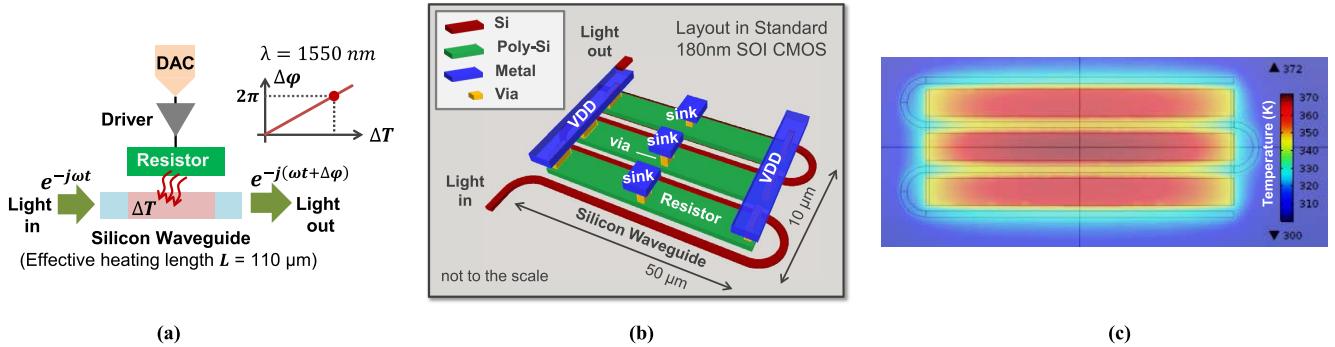


Fig. 12. Optical variable phase shifter designed in the monolithic integration platform. (a) Thermo-optic phase modulation mechanism. (b) Physical layout of the optical variable phase shifter. (c) Simulated temperature profile of the waveguide center-plane.

coupler is designed with $g = 260 \mu\text{m}$, the minimum gap allowed in the 180-nm SOI CMOS technology, and the number of cascaded directional couplers is limited to 8. Fig. 11(a) shows the measured power coupling ratio of the optical directional coupler. The 3-D finite-difference time-domain-based simulation predicted $L_\pi = 18 \mu\text{m}$, which is in good agreement with the measurement results. The directional couplers are fairly wideband, as shown in Fig. 11(b).

C. Optical Variable Phase Shifter

Optical variable phase shifters are based on thermo-optic modulation [see Fig. 12(a)]. The input light is delayed in proportion to the temperature rise ΔT of the waveguide¹ where the light is traveling. Flowing a current into a polysilicon strap near the waveguide realizes an electrically controlled heater to introduce the temperature rise. The phase shift $\Delta\phi$ added to the input light can be approximated [36] as

$$\Delta\phi \simeq \frac{2\pi L'}{\lambda} \frac{dn}{dT} \Delta T \quad (9)$$

where L is the length of the phase shifter, and the sensitivity of refractive index to temperature change dn/dT in silicon is approximately $1.84 \times 10^{-4} \text{ K}^{-1}$ for 1550-nm wavelength. Fig. 12(b) shows the optical variable phase shifter designed for the 1024-element array. Overall $110\text{-}\mu\text{m}$ long silicon waveguide is folded into four segments surrounding three polysilicon heaters. A standalone experimental test chip showed that the folded structure provides 1.8 times higher thermal efficiency compared with a straight structure, which consumes 85 mW for 360° phase shift in the same SOI CMOS technology. Although the lowest melting temperature of aluminum interconnection to the polysilicon heater is over 600°C , in order to limit the temperature of the monolithically integrated transistors, the polysilicon heaters are designed not to exceed 200°C . The maximum heater temperature is the key parameter that sets the silicon footprint of the optical variable phase shifter, which is $50 \mu\text{m} \times 10 \mu\text{m}$. To avoid the detrimental impact of metal contact silicidation on the silicon waveguide, the polysilicon heater is placed next to the silicon

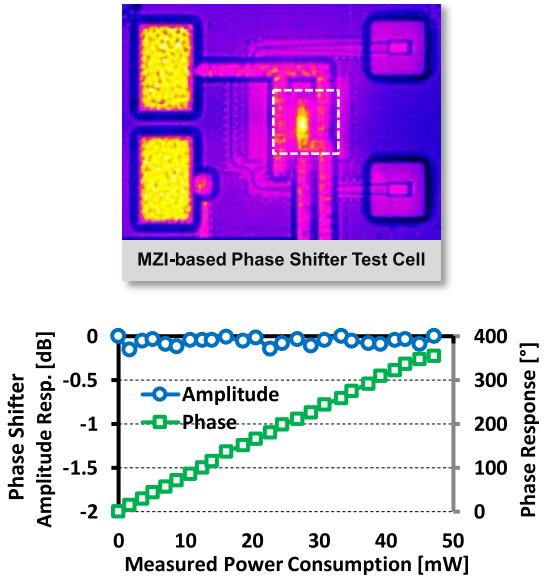


Fig. 13. Microphotograph and measured response of the optical variable phase shifter at the 1550-nm wavelength from an MZI-based standalone characterization structure.

waveguide rather than staying on top of the silicon waveguide. The edge-to-edge gap between the polysilicon heater and the silicon waveguide is set to 500 nm. The temperature profile of the phase shifter, obtained from the 3-D finite-element method (FEM) simulations [see Fig. 12(c)], shows heat delivery from the heater to the surrounding silicon waveguide. Fig. 13 shows the measured response of the optical variable phase shifter. An MZI-based test structure [33] characterizes the phase and the amplitude response. The optical variable phase shifter achieves 360° phase shift by consuming 48-mW power with the polysilicon heater. Obtaining the full coverage of 360° phase modulation range is critical to the optical beam-steering operation. Therefore, the integrated optical modulator driver (Section IV-F) is designed to provide up to 18-mA current, which allows the $330\text{-}\Omega$ polysilicon heater to dissipate up to 107 mW and the variable optical phase shifter to achieve up to 803° phase shift for providing necessary calibration offsets under a large process variation. For electro-migration reliability, the polysilicon heater is designed to allow up to 20-mA

¹The waveguide temperature rise ΔT is a deterministic value. The symbol Δ , in this paper, does not represent a statistical measure of standard deviation.

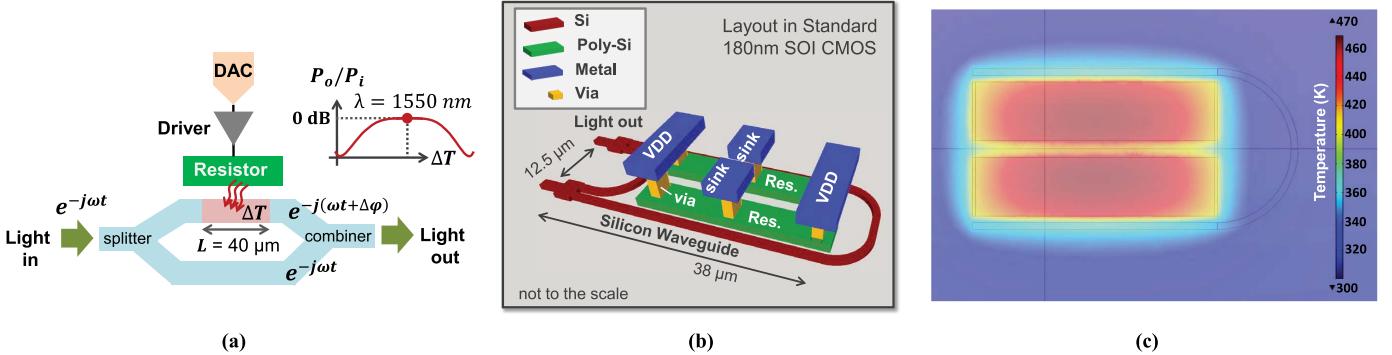


Fig. 14. Optical variable attenuator designed in the monolithic integration platform. (a) Thermo-optic intensity modulation mechanism. (b) Physical layout of the optical variable attenuator. (c) Simulated temperature profile of the waveguide center-plane.

current with 132-mW power dissipation. The measured optical insertion loss of the phase shifter is 2.3 dB, mostly contributed by the bend waveguide sections around the polysilicon heaters.

D. Optical Variable Attenuator

Fig. 14(a) shows the operating principle of the thermo-optic variable attenuator in the prototype chip, which performs array calibration and limited sub-array beamforming. After the input light is equally split into two branches, only one branch is selectively heated, and then, the two branches combine again. Depending on the phase shift introduced by the heated branch, the output light intensity P_o is modulated and can be approximated [34] as

$$P_o = P_i \cos^2 \left(\frac{\pi L}{\lambda} \frac{dn}{dT} \Delta T \right) \quad (10)$$

where L is the length of the heated waveguide section and ΔT is the temperature rise of the heated section. The output light intensity variation slope is higher for low temperature, and the slope gets smaller as the temperature goes higher. To have a large dynamic range control with relatively low power consumption, the variable attenuator is designed, such that the maximum attenuation can be obtained when the heater is OFF. This can be done by adjusting the length difference between the two branches. Fig. 14(b) shows the designed optical variable attenuator. For compact realization to be used in the 1024-element array prototype, the optical power splitter and the optical power combiner are implemented using a 1×2 multi-mode interferometer (MMI) whose silicon footprint is as small as $2.75 \mu\text{m} \times 2 \mu\text{m}$ and introduces 0.4-dB insertion loss. The $40-\mu\text{m}$ long region of the silicon waveguide between the two MMIs is heated by a $500\text{-}\Omega$ polysilicon heater consisting of two segments, making the overall silicon footprint of the optical variable attenuator as $38 \mu\text{m} \times 12.5 \mu\text{m}$. The temperature profile with 3-dB attenuation setting is obtained from 3-D FEM simulation [see Fig. 14(c)], showing heat delivery from the two-segment heater to the adjacent straight waveguides. Fig. 15 shows the measured response of the optical variable attenuator. An MMI-based test structure is also used to characterize the phase and the amplitude response of the variable optical attenuator, which achieves 15-dB amplitude control by consuming 70-mW power.

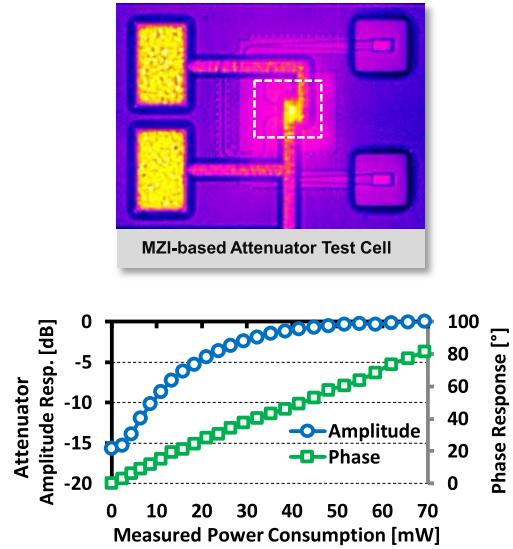


Fig. 15. Microphotograph and measured response of the optical variable attenuator at the 1550-nm wavelength from an MMI-based standalone characterization structure.

This is significant power consumption but in a typical range among compact thermo-optic modulators. The measured optical insertion loss of the optical variable attenuator is 1.2 dB contributed by the bend waveguides and the two MMIs.

E. Grating Coupler Optical Antenna

Grating couplers [13], [19] are used as an optical antenna in the prototype array chip in order to couple the light in and out of the chip. A typical grating coupler shown in Fig. 16(a) consists of the repeating grating teeth and the underlying waveguide. Following the fundamental Bragg reflection law, the grating period Λ determines the angle θ_c of the radiation direction as

$$n_c \sin \theta_c = n_e - \frac{\lambda}{\Lambda} \quad (11)$$

where n_c is the refractive index of the cladding material and n_e is the effective refractive index of the grating coupler determined by the geometry of the grating teeth and

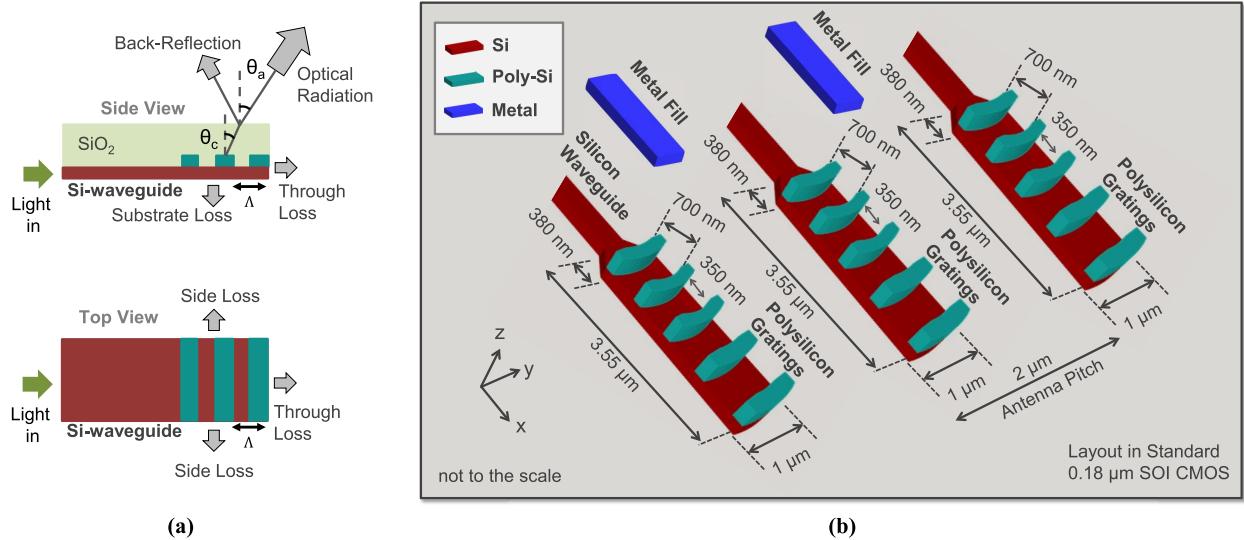


Fig. 16. Grating coupler optical antenna in the SOI CMOS monolithic integration platform. (a) Bragg reflection at the grating coupler. (b) Physical layout and a realization of a large-scale array, which requires systematic metal fill in-between antenna feed waveguides to satisfy manufacturing film density requirement.

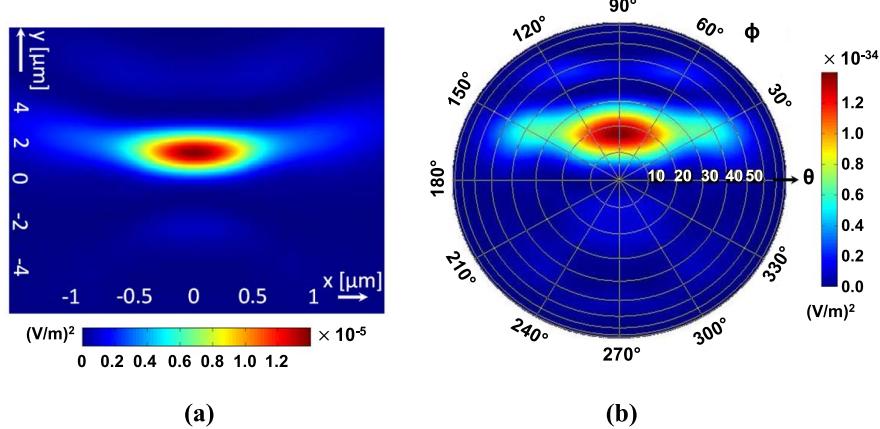


Fig. 17. Simulated near-field and far-field radiation of the focusing grating coupler optical antenna, showing 17° radiation angle to the normal of the chip surface. (a) Near-field optical emission. (b) Far-field optical radiation.

the waveguide. The radiation angle to the air θ_a is obtained with Snell's law as

$$\theta_a = \sin^{-1} \left(\frac{n_c \sin \theta_c}{n_a} \right). \quad (12)$$

Fig. 16(b) shows the designed grating coupler in an antenna array to couple out the light for beam steering in the air. The focusing grating coupler consists of 145-nm thickness silicon strip waveguide in the bottom and 165-nm thickness polysilicon grating teeth in the top [19]. Since the 1024-element prototype array has 2- μm antenna pitch, the strip waveguide of the grating coupler is designed to have 1- μm width, balancing radiation efficient and crosstalk between adjacent grating couplers. Fig. 17 shows the simulated near-field and far-field radiation pattern of the grating coupler optical antenna. Simulated coupling efficiency to the air is around 50% with the radiation angle θ_a of 17° to the normal of the chip surface.

F. Nonlinear Current DAC With High-Voltage Output Driver

DACs, which drive optical variable phase shifters (Fig. 13) in the prototype 1024-element array with 2- μm antenna pitch, are designed to provide 45° beam-steering range and 0.2° steering angle resolution for automotive lidar applications, which translates to 9.8-bit resolution, including an extra design margin of two bits for nonlinearity compensation. Transmitter optical beamwidth narrower than the steering resolution of 0.2° can improve the detector signal-to-noise ratio. Furthermore, the characteristics of the optical variable attenuator (Fig. 15) shows that a current DAC needs a nonlinear transfer characteristics in order to have a uniform resolution with linear digital control on the nonlinear optical modulation. For array calibration as well as optical output power control, the current DAC is designed to control the optical variable attenuator output power with a resolution of 0.1 dB. Considering sufficient oversampling and extensive characterization on the optical modulators, the current DAC is designed to operate up to 2 MS/s, which is

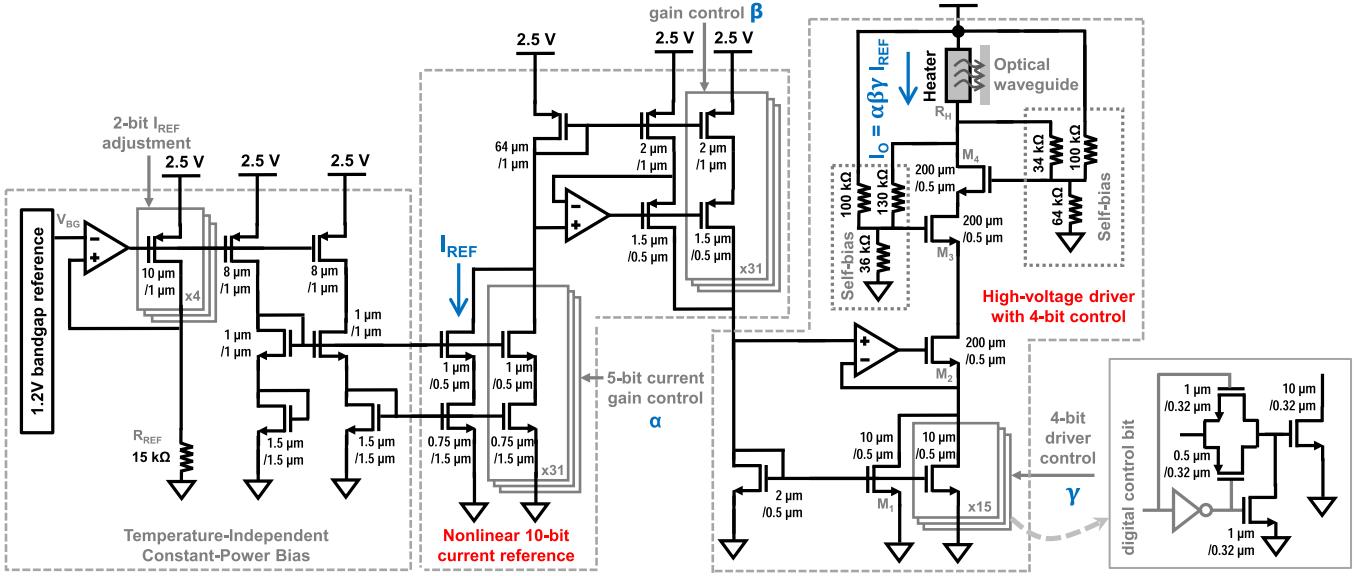


Fig. 18. Nonlinear current DAC consisting of a nonlinear 10-bit current reference and a high-voltage driver with 4-bit control. All transistors are 2.5-V I/O devices.

two orders of magnitude more than what is necessary for the less than 10-kHz optical modulation bandwidth of the thermo-optic modulators in the prototype chip.

Fig. 18 shows the circuit realization of a nonlinear current DAC consisting of two 5-bit tunable current references followed by a high-voltage driver with a 4-bit current scalar, providing overall 14-bit digital control. The architecture is based on cascaded current multipliers [37]. To increase the maximum power delivery to the optical modulator heaters and also to reduce the IR drop over the metal interconnection from the DAC to the optical modulator heaters, an 8-V supply voltage is used to drive the heaters of thermo-optic modulators on the prototype chip. The regulated current mirror at the high-voltage output driver is used to achieve a wide dynamic range of the DAC output current from 1 μ A to 18 mA. The current mirror regulation is implemented by using a two-stage operational amplifier with a DC gain of 50 dB. The 25-MHz unity-gain frequency of the operational amplifier at 125°C temperature achieves less than 82-ns settling time with 0.1% accuracy at the worst process corner simulation. To manage the 8-V supply, four 2.5-V I/O transistors are stacked using self-bias circuits. The resistive self-biasing network [38], [39] is designed, such that its settling time is similar to the operational amplifier so that the stacked transistors do not suffer excessive voltage stress during DAC output transitions. Fig. 19 shows the simulated step response of the DAC, which has 251-ns settling time with 0.1% accuracy to obtain the 9.8-bit beam-steering resolution at the 2-MS/s conversion rate. All bias voltages for the DAC are internally generated using a bandgap reference, such that the reference current I_{REF} , which is adjustable from 2.5 to 7.5 μ A, allows temperature-independent optical modulation with the nonlinear DAC. The resistance of the polysilicon heaters of the thermo-optic modulators in the prototype chip increases by approximately 10% when the temperature increases from 25 °C to 200 °C. For the

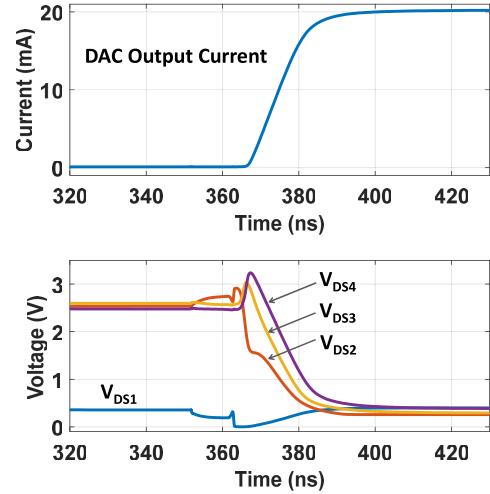


Fig. 19. Simulated settling behaviors of the nonlinear current DAC output and the stacked transistors in the high-voltage driver.

linear operation of thermo-optic modulators, it is necessary to dissipate a constant amount of power at the polysilicon heater for a given DAC input digital code. Therefore, as the temperature goes higher, in order to compensate for the increasing heater resistance, the bias current generation circuit should reduce the reference current rather than keeping it absolutely temperature-independent. The heater power consumption is given by $P_H = (kV_{BG}/R_{REF})^2 R_H$, where k is the current DAC gain, V_{BG} is the bandgap reference voltage, R_{REF} is the bias reference resistor, and R_H is the heater resistance, as seen in Fig. 18. Therefore, for the temperature-independent power consumption control of the polysilicon heaters, the bias reference resistor R_{REF} can be designed, such that the temperature sensitivity of the R_H/R_{REF}^2 term becomes minimum. This can be accomplished by connecting two resistors in series,

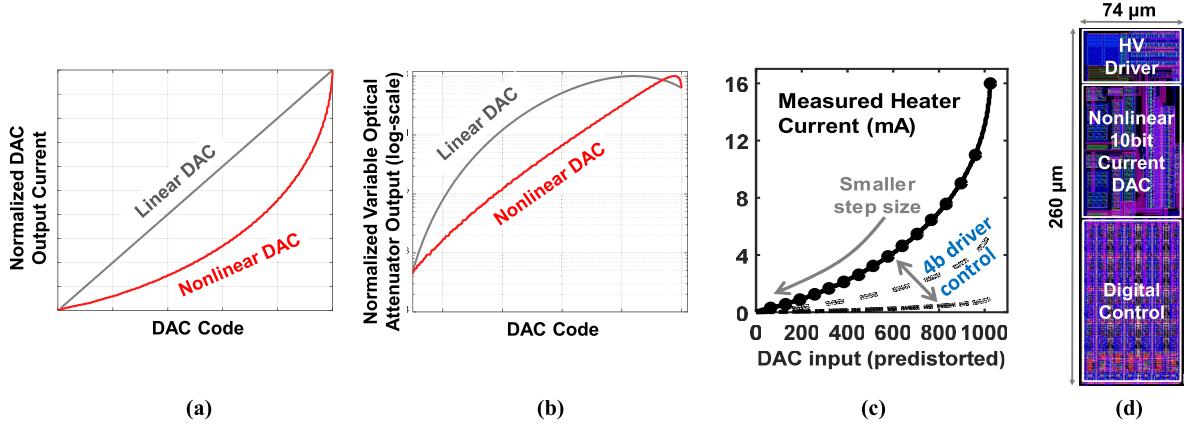


Fig. 20. (a) Simulated DAC output current. (b) Simulated output of an optical variable attenuator driven by the nonlinear DAC. (c) Measured DAC output current. (d) Silicon footprint of the nonlinear DAC.

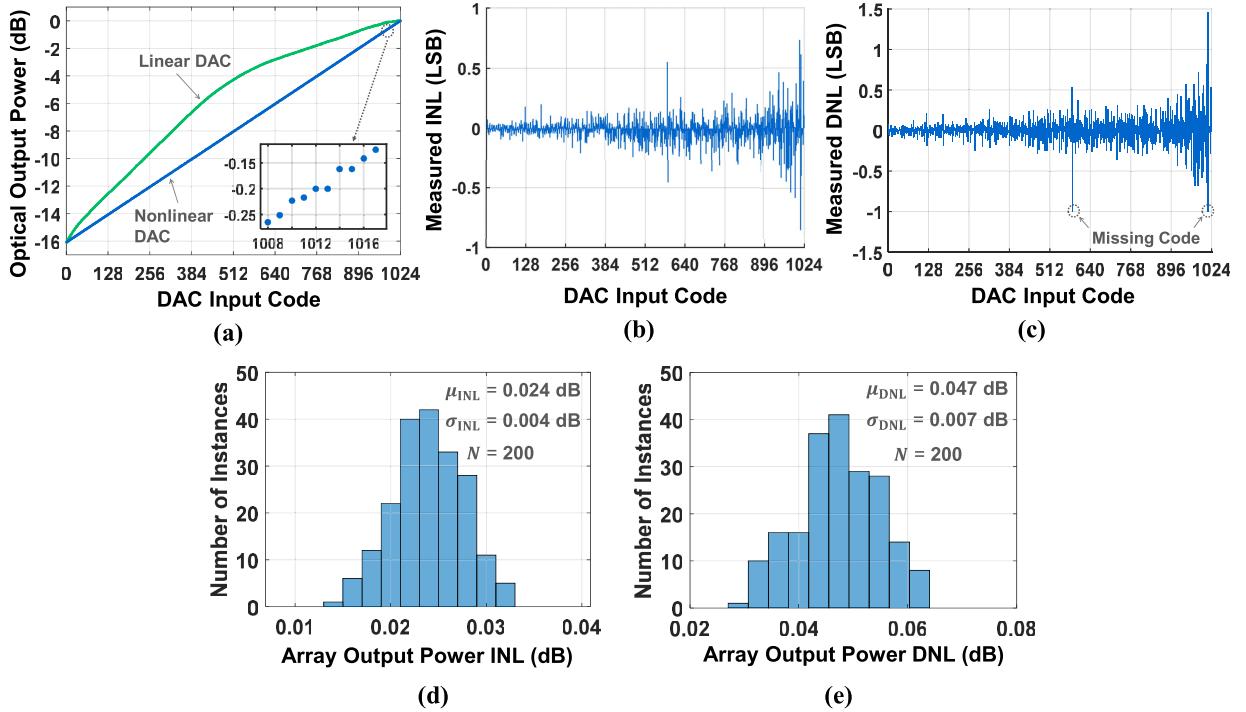


Fig. 21. DAC characterization with the optical variable attenuator in the prototype chip. (a) Measured output power of the optical variable attenuator. (b) and (c) Measured INL and DNL in the unit of the DAC LSB. (d) and (e) Simulated impact of process variations on the peak INL and the peak DNL of the optical phased array performance in output power control.

whose temperature coefficients have different signs to each other. The 15-kΩ bias reference resistor in the prototype chip is implemented as a polysilicon with the same temperature coefficient as the polysilicon heater of the optical modulators. Therefore, as the temperature goes higher, the heater power consumption slightly decreases. This is intended to prevent a thermal runaway.

Fig. 20 shows the transfer characteristics of the designed nonlinear DAC, which provides more uniform intensity control in decibel scale with the optical variable attenuator, compared with a conventional linear DAC. The nonlinear current DAC provides a smaller output step size with a lower output current

and a larger step size with a higher output current, so that the DAC characteristics can compensate the optical modulator nonlinearity. In order to improve the overall linearity, digital predistortion to the DAC input code is necessary. The measured nonlinear DAC characteristics up to 16-mA output is obtained with predistorted digital input codes and 6.7-μA reference current (I_{REF}). The reference current can be increased up to 7.5 μA to provide the maximum DAC output current of 18 mA. For the array column DACs driving up to eight optical phase shifters in the same column, the current mirror transistors in the high-voltage driver are correspondingly scaled up.

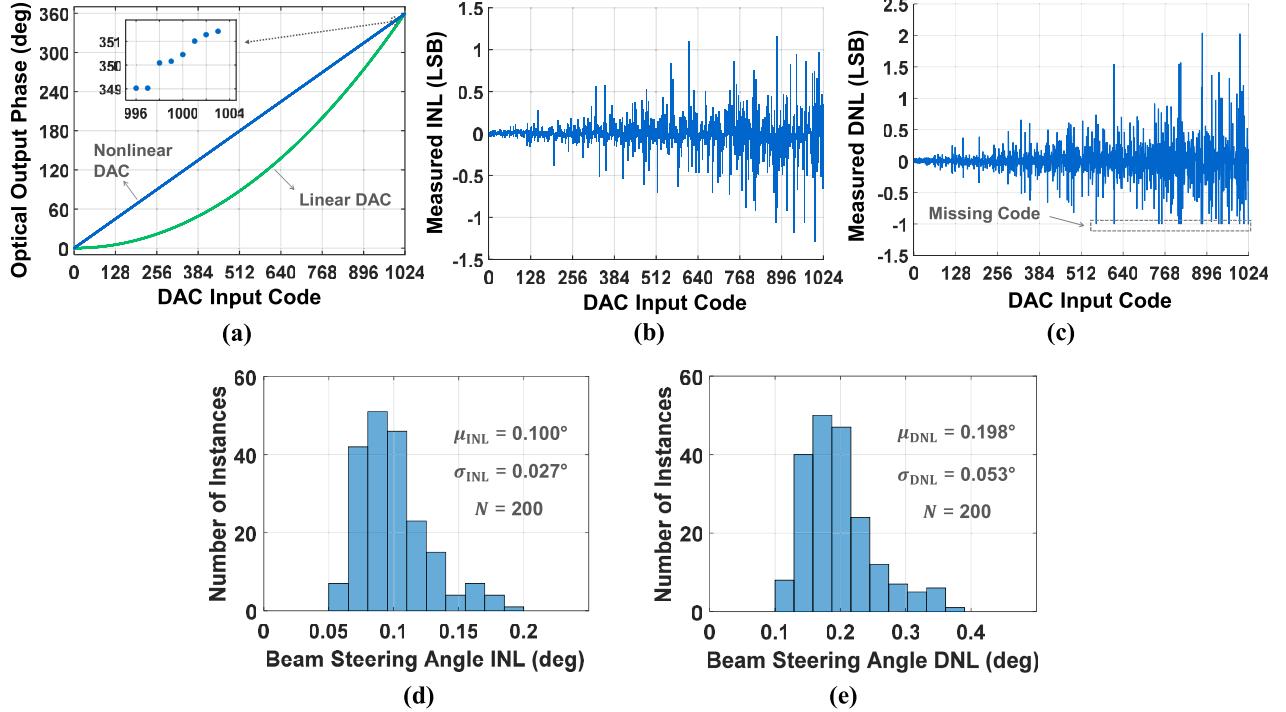


Fig. 22. DAC characterization with the optical variable phase shifter in the prototype chip. (a) Measured output phase response of the optical variable phase shifter. (b) and (c) Measured INL and DNL in the unit of the DAC LSB. (d) and (e) Simulated impact of process variations on the peak INL and the peak DNL of the optical phased array performance in the beam-steering accuracy.

Fig. 21(a) shows the measured optical output power of the optical variable attenuator driven by the nonlinear current DAC. The nonlinear DAC achieves up to 3.7 dB lower INL compared with an external linear DAC (Keysight E3631A). This linearity improvement in INL comes from the nonlinearity cancellation of the optical attenuator by the DAC as well as from the digital predistortion on the input codes. Fig. 21(b) and (c) shows the measured INL and DNL of the optical output power in the unit of the DAC least significant bit (LSB). Unit transistors in the two 5-bit tunable current mirrors of the DAC are sized, such that a standard deviation of drain current variation is 3%. The missing codes identified from the DNL measurement occur when the nonlinear DAC mismatch is large so that digital predistortion cannot provide a necessary correction. Statistical simulations on 200 samples are performed to observe how the impact of process variation on the nonlinear DAC affects the optical phased array system performance. A single LSB error in the DAC results in 0.016-dB deviation with the array output power control. Fig. 21(d) and (e) shows that both the peak INL (0.024 ± 0.004 dB) and the peak DNL (0.047 ± 0.007 dB) among the 200 samples are enough to provide array optical output power control with a resolution of 0.1 dB.

Fig. 22(a) shows the measured phase response of the optical variable phase shifter driven by the nonlinear DAC. The nonlinear DAC achieves up to 93° lower INL compared with the external linear DAC. Fig. 22(b) and (c) shows the measured INL and DNL of the phased response in the unit of the DAC LSB. The difference in the nonlinearity of the optical phase attenuator from the optical variable phase shifter results

in a different INL and DNL compared with those of the optical variable attenuator. There are more missing codes with the optical phase shifter, because the DAC nonlinearity cancels the nonlinearity of the attenuator better than the nonlinearity of the phase shifter. Additional 200 statistical simulations are performed to investigate the impact of the DAC mismatch on the beam-steering angle shift of the optical phased array. The single LSB error of the DAC results in 0.35° deviation with the optical variable phase shifter output, which consequently introduces 0.04° deviation in the beam-steering angle of the optical phased array. Fig. 22(d) and (e) shows that both the peak INL ($0.100^\circ \pm 0.027^\circ$) and the peak DNL ($0.198^\circ \pm 0.053^\circ$) among the 200 samples may provide the 0.25° resolution in the optical beam-steering angle control with a yield of 25% (50 samples achieve DNL less than the half of the 0.25° resolution).

V. IMPLEMENTATION

A. Monolithic Integration in SOI CMOS

Prototype optical phased arrays and test building blocks are monolithically integrated into Global Foundry 7RF SOI 180-nm SOI CMOS technology. All nanophotonic devices and electronic devices are fabricated on the same wafer with no modifications to the native SOI platform. The buried oxide layer with 1- μm thickness eliminates the need for any back-end post-processing steps.

In order to characterize the individual building blocks and the sub-systems of the 1024-element optical phased array, a 1.2 mm \times 6.4 mm test chip is implemented, which includes the building block test structures. Fig. 23 shows

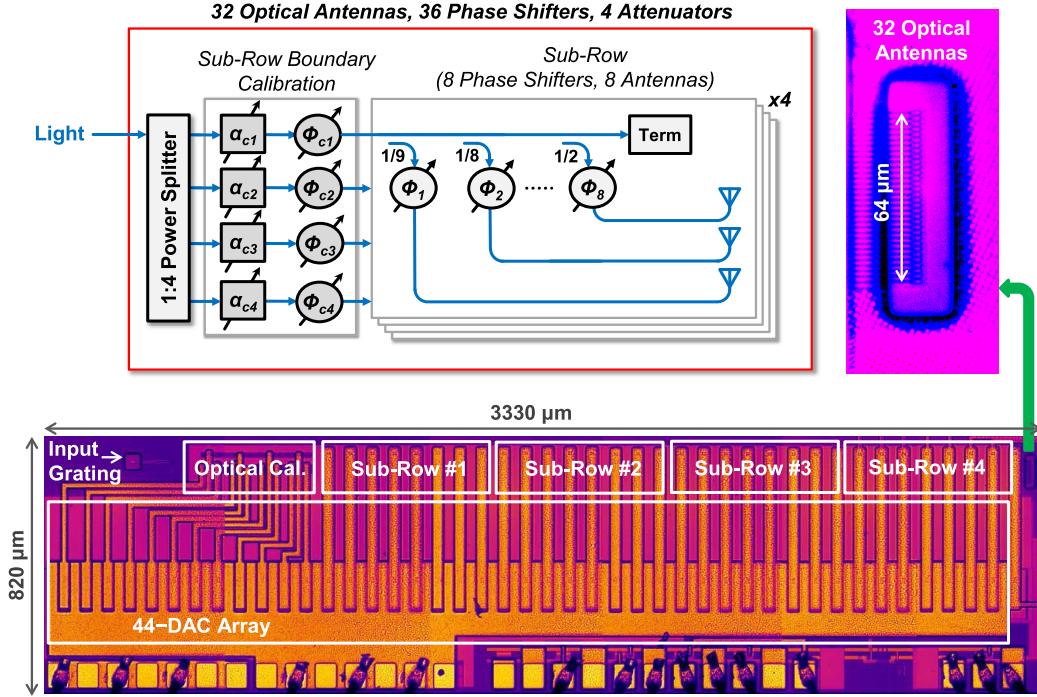


Fig. 23. 32-element optical phased array prototype and chip microphotograph.

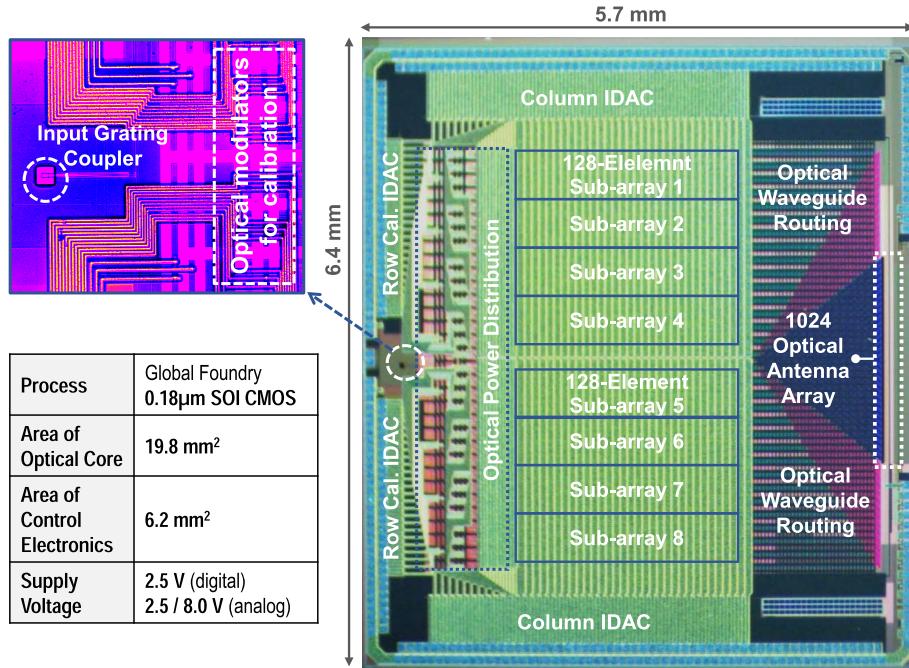


Fig. 24. 1024-element optical phased array chip microphotograph.

the chip microphotograph of the standalone sub-array with 32 elements, which is separately measured to characterize one unit row of the 1024-element optical phased array. The 32-element sub-array occupies 3.33 mm × 0.82 mm area, monolithically integrating 44 DACs, 32 optical variable phase shifters, 8 optical modulators for array calibration, and 4 dummy polysilicon heaters to keep a constant sub-array temperature.

An 1024-element optical phased array with the proposed scalable architecture, which consists of 8 sub-arrays and 136 DACs, is implemented in another chip with 5.7 mm × 6.4 mm size (Fig. 24). Optical components occupy approximately 54% of the 37.48 mm² area, while control electronics takes only 17% of the chip area. This is remarkable area saving considering that control electronics of an optical phased array with conventional architecture takes orders of magnitude larger

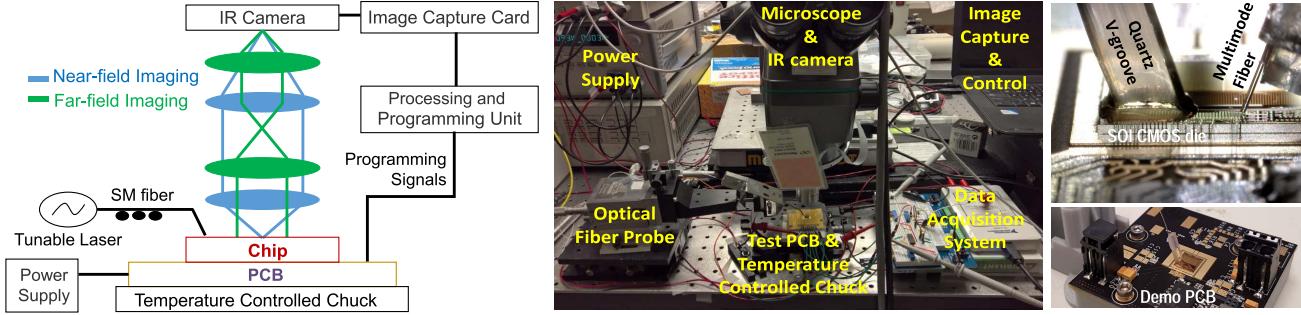


Fig. 25. Optical assembly and experimental test setup. For robust operation against vibration, the optical input fiber can be bonded to the SOI CMOS using a quartz V-groove.

area than all other optical components and thus difficult to be monolithically integrated in a large-scale array. Dummy metal patterns with 240-nm width are generated by a custom algorithm, such that the first metal dummy patterns are located between the optical waveguides [see Fig. 16(b)], providing 610-nm lateral spacing between the metal dummy patterns and the silicon waveguides to satisfy the film density requirement of the large-scale array chip.

B. Optical Assembly and Test Setup

Fig. 25 shows the optical assembly, which aligns a 9- μm -diameter single-mode fiber core with the on-chip input grating coupler. After the optical phased array chip is wire-bonded to a test printed circuit board (PCB), a quartz V-groove structure holding the fiber is bonded to the chip, such that the fiber angle to the normal of the grating coupler is in-between 18° and 20°. The optimum angle is found by adjustment before bonding the V-groove structure to the chip by monitoring optical output power from the array. To monitor the optical power, a multi-mode fiber with 100- μm diameter simultaneously captures the optical power from 32 to 50 grating coupler optical antennas.

In the experimental test setup for optical phase array characterization (Fig. 25), the optical phased array chip is wire-bonded into a PCB, which is in turn mounted on a temperature controlled chuck. The 1550-nm wavelength input light from a tunable laser source couples into the test chip through a single-mode fiber and a polarization controller. A high-resolution IR camera measures the output far-field radiation pattern.

VI. EXPERIMENTAL RESULTS

Fig. 26 shows the measured light intensity of 32-element array, demonstrating a 45° unambiguous optical beam-steering range. The normalized beam intensity in log-scale Cartesian coordinate shows that the largest sidelobe power level is 9 dB below the main lobe intensity, while the average sidelobe power level is 10.3 dB below the main lobe. The measured optical beamwidth of the 32-element sub-array is 1.2°, which is in good agreement with the theoretical analysis.

The measured far-field pattern in the leftmost infrared photograph in Fig. 27 is obtained before the array calibration, showing multiple horizontal sidelobe beam patterns

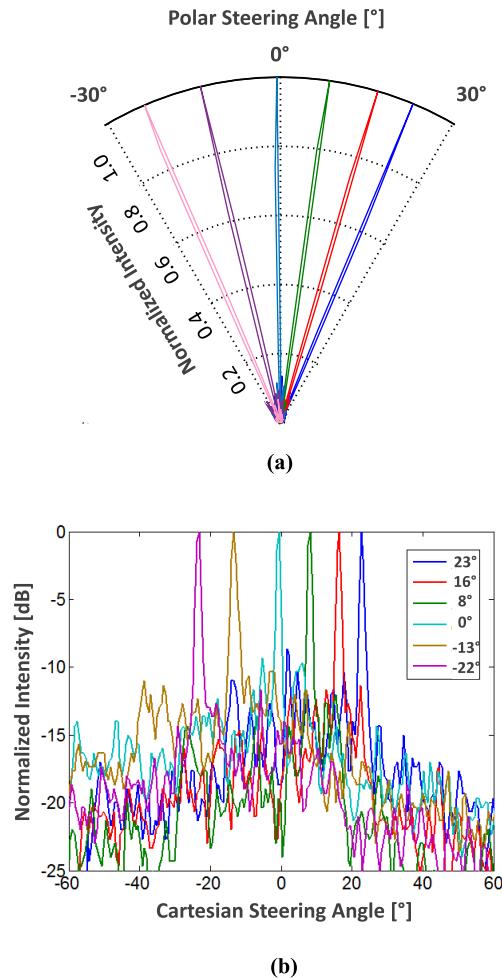


Fig. 26. Measured optical beam steering with the 32-element sub-array chip. (a) Normalized radiation intensity in linear polar coordinate. (b) Normalized radiation intensity in log-scale Cartesian coordinate.

that are perpendicular to the vertical beam-steering direction. In order to reduce the undesirable sidelobe power level and also to narrow the beamwidth, the array calibration is iteratively performed while observing the far-field radiation pattern, as discussed in Section III-B. After the array calibration, these sidelobe beam patterns are suppressed as shown in the second photograph in Fig. 27. The other far-field

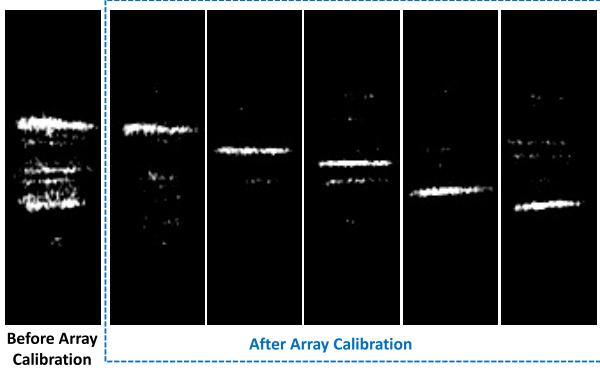


Fig. 27. Sidelobe suppression in the far-field radiation by array calibration (live demonstrated at the ISSCC 2017 Demonstration Session).

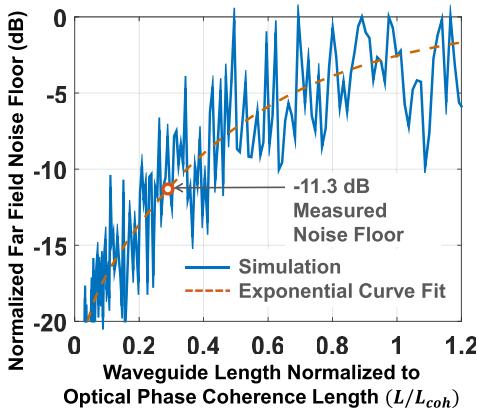


Fig. 28. Indirect measurement of optical phase coherence length from the measured far-field noise floor by using a curve fit to the 32-element array simulation data.

beam patterns in Fig. 27 show different beam-steering angles after separately performed array calibration for each steering angle.

As discussed in Section II-B, the optical phase coherence length can be found from the measured far-field radiation pattern of the 32-element sub-array. An exponential curve fit model (Fig. 28) is created from the array simulation data on the relation between the optical waveguide length and the far-field noise floor of the 32-element array. From the curve fit model, the waveguide length L corresponding to the -11.3 dB noise floor is found as 29% of the optical phase coherence length L_{coh} . Based on the discussion in Section II-B, the root-mean-square random phase error accumulation in a low-level sub-array can be obtained as $\sqrt{2L/L_{coh}} = 43.6^\circ$. The length of the optical waveguides from the beginning of the low-level sub-array, where a random phase error starts to accumulate, to the optical grating coupler antenna is $810 \mu\text{m}$. Therefore, the optical phase coherence length of the SOI CMOS technology is found as $810 \mu\text{m}/0.29 = 2.8 \text{ mm}$. The 4-mm optical phase coherence length reported in [24] is with a dedicated silicon photonics technology with a 220-nm thickness silicon layer with 0.48-dB/mm waveguide loss,

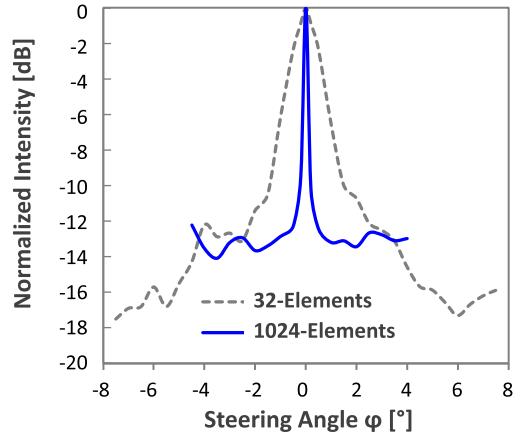


Fig. 29. Measured optical beamwidth of the 1024-element optical phased array.

while the 2.8-mm optical phase coherence length from the prototype chip is with a standard SOI CMOS technology with a 145-nm thickness silicon layer with 1.27-dB/mm waveguide loss. This clearly shows the correlation between waveguide loss and optical phase coherence length as studied in [30]. Note that this is a conservative calculation, because the far-field noise floor may be further reduced by more accurate array calibration.

Fig. 29 shows that the 1024-element array achieves 0.03° optical beamwidth, demonstrating significant reduction from the 1.2° beamwidth of the 32-element sub-array. The increased noise floor of the 1024-element array radiation pattern is due to additional optical insertion loss from: 1) the 1:8 optical distribution network to split the input optical power to the 8 sub-arrays each with 128 elements; 2) an additional optical variable phase shifter and an additional optical attenuator at the input of each sub-array for amplitude and phase calibration; and 3) added length in the optical waveguides for the antenna feed.

The maximum beam-steering speed of the prototype optical phased arrays is determined by the modulation bandwidth of the optical variable phase shifter. An experimental setup shown in Fig. 30 is used to characterize the phase modulation bandwidth of the optical variable phase shifter in the prototype array. The optical power gain of the MZI, whose one leg is an optical variable phase shifter, is measured, while an arbitrary waveform generator is continuously modulating the phase shifter with a square wave. The two voltage levels of the square wave are determined, such that the phase shifters can switch between 0° and 180° . The phase response then can be calculated from the measured amplitude response using the equations summarized in Fig. 30. The measured power gain response of the MZI and the corresponding phase response [see Fig. 31(a)] show that the phase modulation bandwidth of the optical variable phase shifter is 5 kHz. The step response of the MZI test structure [see Fig. 31(b)] shows that the $66\text{-}\mu\text{ms}$ rise time is faster than the $28\text{-}\mu\text{s}$ fall time due to longer heating time than cooling in the experimental setup. The step response of the optical variable attenuator for calibration and power control has a $40\text{-}\mu\text{ms}$ rise time. The required

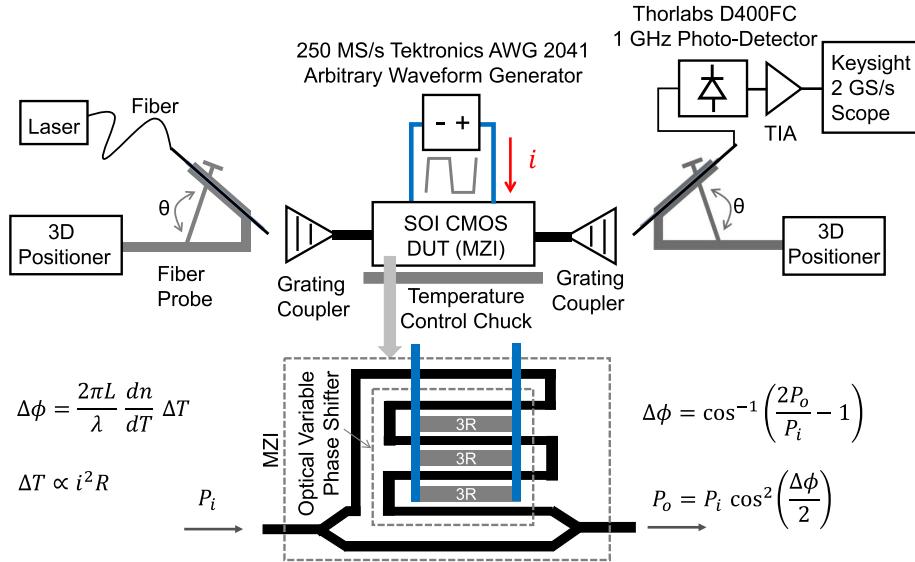


Fig. 30. Experimental setup to characterize the modulation bandwidth of the optical variable phase shifter in the prototype array, which determines the maximum optical beam-steering speed.

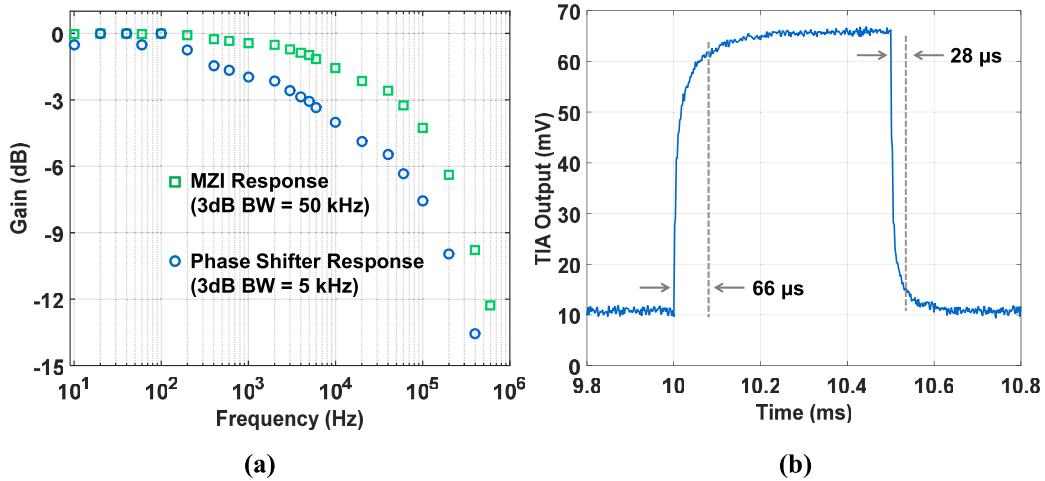


Fig. 31. Measured dynamic responses of the optical variable phase shifter. (a) Frequency response of the phase shifter. (b) Step response of the phase shifter.

beam scanning speed depends on the application. For instance, in a lidar used in automotive applications with a frame rate of 25 frames/s, a horizontal field of view of 60°, and a horizontal resolution of 0.2°, the time allocated for each scan angle is $1/[25 \times (60/0.3)] = 200 \mu\text{s}$. Assuming that the lidar requires 100 μs to stay at each angle to acquire the information with an acceptable signal-to-noise ratio, the setting time should be within 200–100 μs = 100 μs, which is within the capability of thermo-optic variable phase shifters.

The maximum optical power that can be steered by the 1024-element optical phase array prototype is limited by the fiber input grating coupler and the waveguide connected to the grating coupler. Once the fiber input power is split into multiple sub-arrays, the maximum optical power transmission limit can be scaled up by increasing the number of sub-arrays. To characterize the maximum optical radiation power, we measured silicon waveguides in an MZI test structure

TABLE II
MEASURED VARIABILITY OF BEAM-STEERING ACCURACY WITH THE PROTOTYPE OPTICAL PHASED ARRAY DEPENDING ON THE TEMPERATURE CHANGES OF THE CHIP SUBSTRATE

Temperature Change from 25°C	ΔT = 0°C	ΔT = 0.5°C	ΔT = 5°C
Steering Angle Deviation Δϕ	0°	0.20°	1.98°
Side-lobe Power Level	-10.54 dB	-10.53 dB	-10.47 dB
Beam Width in ϕ Direction	0.03°	0.03°	0.05°

whose both ends are connected by the same fiber grating couplers. A 1550-nm Amonics AEDFA-C-301 erbium-doped fiber amplifier injects a watt-level optical power into the grating coupler. The SOI chip with the MZI test structures

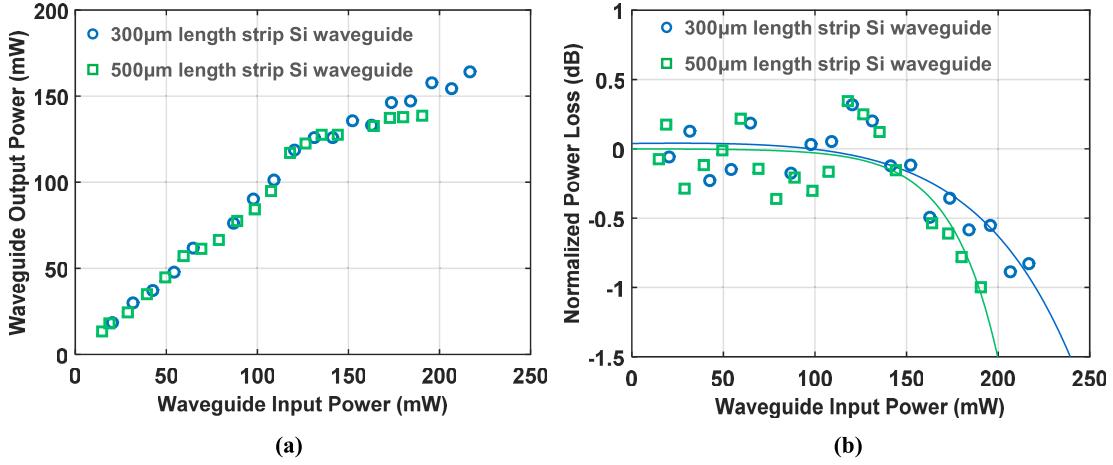


Fig. 32. Measured optical power handling capability of silicon waveguides with $540 \text{ nm} \times 145 \text{ nm}$ cross-sectional area, which determines the maximum optical power that the prototype phased array can radiate. (a) Optical input and output power. (b) Optical power loss (solid lines are fit to the measured data).

TABLE III
PERFORMANCE COMPARISON OF ELECTRONICALLY TUNABLE SOLID-STATE OPTICAL PHASED ARRAYS FOR SHORT-WAVE INFRARED LIGHT

	This Work	Hutchison Optica 2016[21]	Poulton Adv.Pho. 2016[42]	Abediasl Opt.Exp. 2015[19]	Hulme Opt.Exp. 2015[18]	Aflatouni Opt.Exp. 2015[17]	Kwong Opt.Lett. 2014[15]	Guo JSTQE 2013[14]	Sun Nature 2013[13]	Acoleyen Opt.Exp. 2009[11]
Number of Antennas	1024	128	50	8×8	32	16	16	8	8×8	16
Antenna Pitch	$2 \mu\text{m}$	$7.2 \mu\text{m}$	$2 \mu\text{m}$	$33 \mu\text{m}$	$4 \mu\text{m}$	$50 \mu\text{m}$	$4 \mu\text{m}$	$5.5 \mu\text{m}$	$9 \mu\text{m}$	$2 \mu\text{m}$
Max. Two-sided Steering Angle	45°	10°	46°	1.6°	23°	1.5°	20°	16°	9.9°	2.3°
Beam Width in ϕ Direction	0.03°	0.14°	0.85°	0.45°	1°	0.5°	1.2°	0.16°	1.1°	2.7°
Side-lobe Suppression	9 dB	9 dB	9 dB	12 dB	6 dB	6 dB	10 dB	10 dB	N/A	> 13 dB
Number of Control DACs	136 (on-chip)	128 (external)	50 (external)	128 (on-chip)	32 (external)	16 (external)	16 (external)	8 (external)	64 (external)	16 (external)
Power Consumption per Antenna	54 mW	80 mW	12 mW	21 mW	160 mW	N/A	20 mW	40 mW	9 mW	8 mW
Integrated Control (DAC + digital)	Yes	No	No	Yes	No	No	No	No	No	No
Optical Element Phase Control	Thermo-Optic	Thermo-Optic	Thermo-Optic	Thermo-Optic	Thermo-Optic	Charge-Injection	Thermo-Optic	Charge-Injection	Thermo-Optic	Thermo-Optic
Optical Element Intensity Control	No	No	No	Thermo-Optic	Optical Gain	No	No	Optical Gain	No	No
Architecture Scalability	Yes	No	No	No	No	No	No	No	No	No
Power Monitoring Photo Detector	No	No	No	No	Yes	No	No	Yes	No	No
Integrated Light Source	No	No	No	No	Ring Laser	No	No	DBR Laser	No	No
Optical Wavelength	1550nm	1310nm	1550nm	1550nm	1580nm	1550nm	1550nm	1550nm	1550nm	1550nm
Process Technology	SOI CMOS	Si-Photonics	Si-Photonics	SOI CMOS	Hybrid GaAs/Si	Si-Photonics	Si-Photonics	Pure III-V	Si-Photonics	Si-Photonics

are mounted on a temperature control chuck whose thermal time constant is less than $1 \text{ } ^\circ\text{C}/\text{s}$ when heated. In order to avoid the heating of the experimental setups, watt-level optical test signals are injected for 1 s with a repetition period of 100 s, allowing 99 s for cooling. It should be noted that this setup characterizes continuous-wave operation of the waveguides, because the 1 s excitation time is orders of magnitudes larger than the thermal time constant of the silicon waveguides. Fig. 32(a) shows the measured

input power versus output optical power of two waveguides with 300 and 500 μm length, respectively, demonstrating a linear relation between the input and the output power up to 150-mW input. Both waveguides have the same cross-sectional area ($540 \text{ nm} \times 145 \text{ nm}$). Fig. 32(b) shows the normalized optical power loss of the two waveguides. The low-power optical loss of 1.27 dB/mm is de-embedded in Fig. 32, and the plots show extra optical loss related to heating and two-photon absorption, which is a dominating physical loss

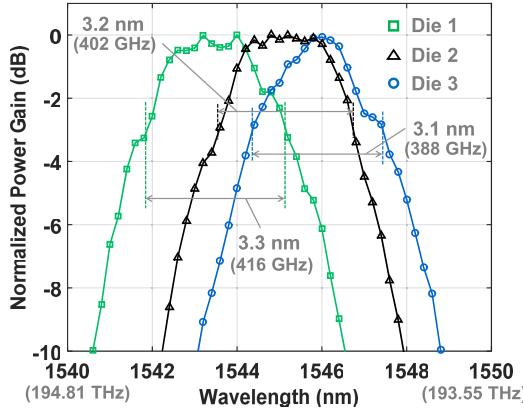


Fig. 33. Measured optical bandwidth of the 1024-element optical phased array, which determines the minimum pulsedwidth and the maximum data rate over the air.

mechanism for high optical power transmission. The 1-dB optical power loss occurs at 220 and 190 mW for the two waveguides with 300- and 500- μm length, respectively. These measurement results conclude, considering the 21.9-dB loss of the array excluding the input fiber grating coupler, that 160-mW optical power can be delivered into the chip and the 1024-element prototype array can radiate 0 dBm (1 mW) optical power. It should be noted that while impulse lidars for automotive applications [40], [41] require transmission of high-power (e.g., 50 W) short-duration (e.g., 5 ns) pulse trains (e.g., 50- μs period), the average transmitted power is quite low (e.g., $50 \text{ W} \times 5 \text{ ns}/50 \mu\text{s} = 5 \text{ mW}$). A coherent lidar that consumes the same average power while transmitting a frequency-modulated continuous signal would achieve the same performance. In other words, a monolithic silicon optical phased array is well capable of meeting the requirements of automotive lidars under a frequency modulated continuous wave coherent scheme.

The maximum modulation bandwidth is determined by the optical bandwidth of the phased array. Fig. 33 shows the variations in the optical bandwidth and the center wavelength of three sample dies, where the 1024-element optical phased array is fabricated. The optical bandwidth is larger than 388 GHz, allowing the transmission of optical pulses narrower than 3 ps, which is well beyond the required modulation bandwidth of lidars for automotive applications (typically less than a few gigahertz).

The effect of temperature change on the optical phased array chip, in terms of steering angle, sidelobe suppression, and beamwidth, is measured and summarized in Table II. To observe the impact of temperature variation, 25 °C calibration status is maintained for other temperatures. The prototype optical phased arrays with thermo-optic modulators were designed to operate with a temperature control subsystem that can regulate the chip temperature variation less than ± 0.5 °C, which introduces maximum $\pm 1.58^\circ$ phase disturbance among two adjacent optical phase shifters in a row of the prototype. Thermal gradient within the chip is regulated to the same extent by dummy heaters as well as by a phase

shifter control algorithm discussed in Section III-C. When the chip temperature changes by 1 °C, there are no visible changes in the steering accuracy in sidelobe suppression and beamwidth.

Table III summarizes the performance of the 1024-element array in comparison with the state-of-the-art solid-state optical phased array implementations that are electronically steerable. This paper is the first demonstration of a very large-scale optical phased array integrating both optical components and control electronics on a single chip.

VII. CONCLUSION

Optical phased arrays that can form narrow beams that can be steered unambiguously across a wide angular range enable interesting sensing, imaging, and communication applications. Realization of such optical phased arrays in a commercial silicon process enables the wide dissemination of this technology in consumer platforms. The main challenge is the realization of a large-scale optical phased array with small spacing between adjacent radiators (ideally half wavelength) with the ability to independently control the phase and amplitude of the optical signal into each antenna. Another practical challenge is due to the sensitivity of the optical phased array to process variations, mismatches, temperature gradients across the chip, and unwanted coupling of optical signal across closely spaced optical components. Naturally, loss, power handling, and power consumption are also very important in the realization of monolithic optical phased arrays.

This paper investigates an architecture-level solution to surmount some of the design challenges on realizing a very large-scale optical phased array. We proposed a scalable optical phased array based on the hierarchical sub-array structure, which extends the array size beyond the conventional limit constrained by a finite optical coherence length. The nested sub-array structure also allows multiple optical variable phase shifters to share the same control electronics for linear beam steering. Hence, a very large-scale optical phased array with integrated control electronics can be realized in orders of magnitude smaller silicon footprint compared with the size of conventional optical phased array realizations. A prototype optical phased array chip is realized to demonstrate the proposed scalable architecture rather than aiming for a particular application.

The proposed architecture is not specific to the aforementioned prototype and is applicable to other platforms. Silicon photonics is a suitable platform for the realization of complex monolithically integrated electro-optical systems in the short and mid-infrared wavelength range. Silicon processes that include thick silicon waveguides [43] may be used for low-loss realizations, while processes that offer silicon nitride waveguides [26] may be used to extend the wavelength range and power handling capability. Hybrid and heterogeneous integration approaches [44]–[46] may be used to add compound semiconductors, such as GaAs, InP, and GaN to the silicon photonics platforms for the realization of lasers and optical amplifiers in a large-scale optical phased array.

ACKNOWLEDGMENT

The authors would like to thank Nankyoung Suh Cockerham and Wes Hansford at The MOSIS Service for supporting the chip fabrication. They would also like to thank A. Willner and P. Liao at the University of Southern California for assistance with characterizing the nonlinearity and power handling capability of silicon photonic waveguides, and J. S. Orcutt at the IBM Thomas J. Watson Research Center for the technical discussions.

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