

A High-Frequency Three-Level Buck Converter With Real-Time Calibration and Wide Output Range for Fast-DVS

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Abstract—This paper presents a 50-MHz 5-V-input 3-W-output three-level buck converter. A real-time flying capacitor (C_F) calibration is proposed to ensure a constant voltage of $V_g/2$ across C_F , which is highly dependent on various practical conditions, such as parasitic capacitance, time mismatches, or any loading circuits from C_F . The calibration is essential to ensure the reliability and minimize the inductor current and output voltage ripple, thus maintaining the advantages of the three-level operation and further extending the system bandwidth without encountering sub-harmonic oscillation. The converter is fabricated in a UMC 65-nm process using standard 2.5-V I/O devices, and is able to handle a 5-V input voltage and provide a 0.6–4.2-V-wide output range. In the measurement, the voltage across C_F is always calibrated to $V_g/2$ under various conditions to release the voltage stress on the high- and low-side power transistors and C_F , and to ensure reliability with up to 69% output voltage ripple reduction. A 90% peak efficiency and a 23–29-ns/V reference-tracking response are also observed.

Index Terms—Adaptive level shifter (LS), buck converter, flying capacitor balance, flying capacitor voltage calibration, fully differential difference amplifier (DDA), real-time calibrations, three-level converter, time mismatch.

I. INTRODUCTION

THREE-LEVEL buck converters are attractive in high-voltage and reference-tracking applications, such as power amplifier (PA) supplies with RF envelope tracking (ET) [1]–[4] and efficient system-on-chip power supplies with dynamic voltage scaling (DVS) [5]. The challenges of the power supplies for these applications are high-speed and wide-voltage-range operations; for example, the PA supply in LTE applications requires an output voltage ranging from 0.5 to 4.5 V with 10–20-MHz ET bandwidth. To achieve such high performance, the dc–dc converter is required to have a wide bandwidth that determines its small-signal response, and

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small LC components that improve the large-signal response. High-frequency switching converters can meet both requirements; however, they have difficulty maintaining high efficiency with increased switching loss [6], especially with a high-voltage rating that usually requires lossy high-voltage devices. Implementation in advanced CMOS technologies with a smaller transistor size can reduce the switching loss, but the transistors can only stand low voltages. To provide a higher voltage than the nominal voltage of the standard transistors, for the converter, either thick-oxide I/O transistors can be used or multiple thin-oxide transistors can be stacked [7]. Thick-oxide I/O transistors can stand higher voltages, but they increase the switching loss due to the large parasitic gate capacitance and may even be unavailable for some process options. By stacking two thin-oxide transistors, on the other hand, the input and output voltages can be as high as twice the transistors' nominal voltage without breakdown issues. At the same time, the efficiency is improved with a smaller gate capacitance.

A three-level buck converter, as shown in Fig. 1(a), is an even better solution that has a potentially wider bandwidth and significantly reduced LC components [1]–[5]. It has an additional flying capacitor C_F , while inheriting the stacking benefits of the cascode two-level converter. Due to the flying capacitor and the time-interleaving switching behavior [8], the three-level buck converter has three voltage levels at the switching node V_X , and a doubled inductor current frequency, thus bringing many extra advantages. V_X is either $(V_g, V_g/2)$ or $(V_g/2, \text{zero})$ according to the duty cycle. Compared with a two-level buck converter with the same LC value and switching frequency, the three-level converter has only 1/4 of the peak inductor current ripple and 1/8 of the peak output voltage ripple [1], [5], [8] which means that the power inductor and output capacitor can be significantly reduced. Smaller output voltage ripple is very beneficial for applications such as high fidelity Class-D amplifiers [9]. With a smaller ripple, the bandwidth of the converter can be pushed to 1/5 of the switching frequency, which is the design limit in practice. Thus, the three-level converter can save costs, reduce the form factor, and boost the reference-tracking response.

All these advantages of the three-level converter, however, rely on the voltage of C_F being maintained at $V_g/2$. C_F works as another voltage source and a level shifter (LS), so the voltage difference across the power transistors can be well

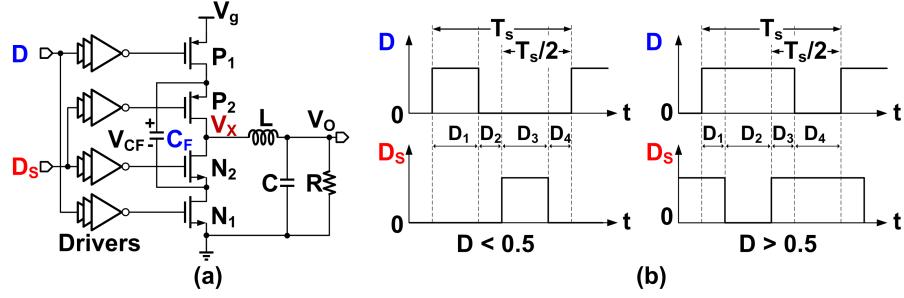


Fig. 1. (a) Three-level buck converter with (b) duty cycle signals.

defined and limited to $V_g/2$, and V_X can only be $V_g/2$, except for V_g and zero. However, in real silicon implementations, V_{CF} can easily deviate from $V_g/2$, and even go to 0 or V_g , due to imperfect conditions [10], [11], such as the parasitic capacitance of C_F , the time mismatches between the power transistors' driving signals, and the current-drawing circuits. V_{CF} not equaling $V_g/2$ will result in many serious problems, such as breakdown and reliability issues for the power transistors. V_X will have incorrect values, and as a result, the inductor current ripple and V_O ripple will increase significantly. The system stability may also be affected, with potential sub-harmonic oscillation occurring [12]. Therefore, the system bandwidth should be designed to be conservative due to the much larger noise. Thus, the calibration to keep V_{CF} always equal to $V_g/2$ is essential to ensure proper operation and maintain the advantages of three-level converters. However, this issue is not considered in most prior works, such as [1], [2], [5], and [13], and although a C_F balancing technique is proposed in [14], the V_{CF} regulation is only executed every 32 clock cycles, which is slow and may still bring voltage stress and reliability issues during any load/line transients. The regulation of V_{CF} also depends on loading conditions because of the limited resolution. Another C_F self-balancing technique is proposed in [15], but it needs a current sensor and cannot be applied in pulse width modulation control.

Motivated by the above concerns, a wide-output range, fast reference-tracking response, high-efficiency three-level buck converter with real-time calibration is presented [16]. The paper is organized as follows. Section II reviews the operation principle of the three-level buck converter. Section III discusses the importance of a calibrated V_{CF} and the non-idealities that bring V_{CF} variation. Section IV describes the proposed three-level buck converter in detail, including the proposed real-time calibration scheme with a differential difference amplifier (DDA) with common-mode feedback (CMFB) implementation, the type-III compensator, the drivers with an adaptive LS and dead-time control, and other building blocks. Measurement results are provided in Section V, followed by conclusions in Section VI.

II. OPERATION PRINCIPLE OF THREE-LEVEL BUCK CONVERTER

In the three-level topology, there are two pairs of complementary switches, P_1, N_1 and P_2, N_2 with the same duty

cycle signals of D and D_S , respectively, as shown in Fig. 1(a). Ideally, D and D_S have exactly the same duty cycle, but with a 180° phase shift. Every cycle can be divided into four parts, as shown in Fig. 1(b). The operating states and detailed timing diagrams of D , D_S , V_X , inductor current I_L , and V_{CF} are sketched in Fig. 2. When D is smaller than 0.5, for the first part, when $D = 1$ and $D_S = 0$, the converter works in State 1 (S_1). P_1, N_2 are turned on and P_2, N_1 are off, and V_X equals $V_g - V_{CF}$, which should be $V_g/2$ and larger than V_O . So, the inductor current goes up at the same time C_F is charging. For the second part, the converter works in State 2 (S_2), with V_X equaling 0. The inductor current goes down and V_{CF} stays the same. For the third part, the converter works in State 3 (S_3), with V_X equaling V_{CF} , which should be $V_g/2$. The inductor current goes up at the same time C_F is discharging. Finally, $D = 0$, $D_S = 0$, and the converter works in S_2 again. To conclude, V_X is either 0 or $V_g/2$, and the frequency of the inductor current is twice that of the duty cycle frequency. In every cycle, there is a charging and a discharging phase for C_F . When D is larger than 0.5, there is a new state, State 4 (S_4), in which the inductor current goes up and V_{CF} stays the same with V_X equaling V_g . The converter goes from $S_4 \rightarrow S_1 \rightarrow S_4 \rightarrow S_3$. In every cycle, V_X is either V_g or $V_g/2$ and C_F is charged and discharged.

III. DISCUSSION OF THE IMPERFECT V_{CF}

A. Importance of Calibrated V_{CF}

To ensure correct three-level operation, V_{CF} equal to $V_g/2$ is a prerequisite and must be guaranteed. Otherwise, the transistors will have overvoltage issues. Assume that V_g is 5 V and P_1, P_2, N_2 , and N_1 are 2.5-V devices, as shown in Fig. 3. If V_{CF} is 4 V instead of 2.5 V, then in S_1 and S_2 , V_{DS} of P_2 will be 4 V, much larger than the nominal 2.5 V. Due to the overvoltage stress, P_2 may breakdown and failures will appear. In other states, other transistors, such as N_2 , will also suffer from the same issue. Moreover, part of C_F is usually implemented with a MOS capacitor due to the high density, and a 4-V gate voltage can easily breakdown the 2.5-V MOS capacitor.

V_{CF} being unequal to $V_g/2$ also degrades the ripple reduction performance. The inductor current ripple and output voltage ripple of the same three-level converter with different V_{CF} values are simulated from 0 to 5 V, as shown in Fig. 4. As can be observed, the current ripple increases from around 25 to 250 mA, and the voltage ripple increases from around

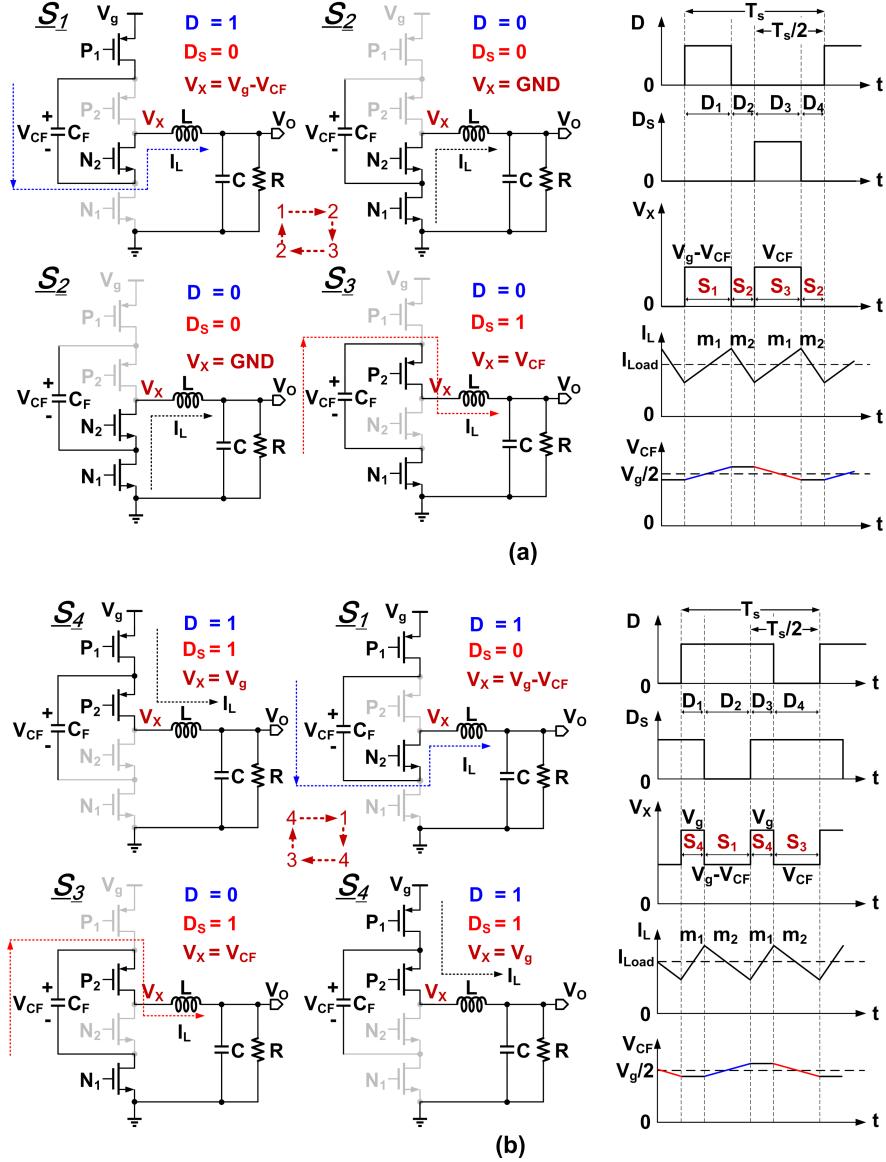


Fig. 2. Operating states and timing diagram of the three-level buck converter when (a) $D < 0.5$ and (b) $D > 0.5$.

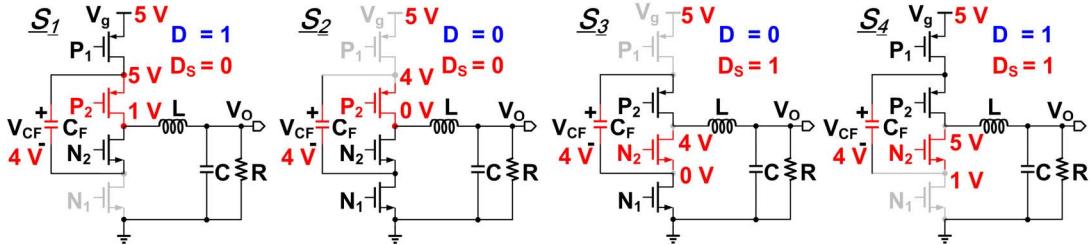


Fig. 3. Over-voltage problem caused by V_{CF} being unequal to $V_g/2$.

6 to 60 mV, an increment of around ten times. The much larger output voltage ripple will also result in extra voltage ripple of the output of the error amplifier (EA) in the controller. Thus, the system bandwidth should be designed to be lower to ensure stability, which limits the converter's transient response. When the current ripple is increased, higher conduction loss will result and unexpected reverse current conduction may occur.

To avoid all these problems, a calibration scheme which keeps V_{CF} to $V_g/2$ is essential for three-level buck converters.

B. V_{CF} 's Dependence on Different Non-Idealities

Ideally V_{CF} should always be $V_g/2$; however, in practical circuitry implementations, it depends on many imperfect conditions, such as the parasitic capacitance of C_F , the

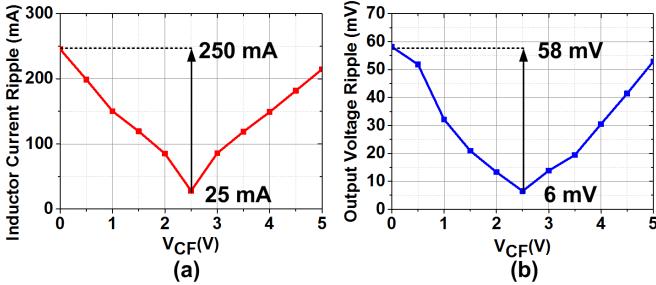


Fig. 4. (a) Inductor current ripple versus V_{CF} . (b) Output voltage ripple versus V_{CF} .

current-drawing circuits, and the time mismatch between the driving signals. The minimum flying capacitor value is determined by the loading conditions and the switching frequency [10]. In our design, a 5-nF flying capacitor is used, which occupies a large area. To increase the capacitor density in the CMOS process, C_F is implemented by stacking MIM, MOM, and MOS capacitors [17]. Though an N-cap, with the gate as the top plate and the N-well as the bottom plate, is chosen for smaller parasitics from the four kinds of available MOS capacitors [10], it still has comparatively large parasitic capacitance, around 1.36% of the total capacitance. Assume that the total parasitic capacitance of C_F is C_{FP} and it is from C_F 's bottom plate to ground, as shown in Fig. 5. When the three-level converter transits from S_2 to S_1 , or from S_3 to S_4 , C_{FP} will be immediately charged from 0 to $V_g/2$ by an additional current i_{charge} . This current will charge up C_F at the same time. Thus, V_{CF} increases during some state transitions.

V_{CF} also depends on other non-idealities, as shown in Fig. 6. For example, if C_F is used for powering the driver circuits, there will be current flowing out of C_F . Thus, V_{CF} decreases with the current drawing. As mentioned in Section II, there is a charging and discharging phase for C_F in every cycle, which should ideally be of equal lengths. However, time mismatch always exists in real-circuitry implementations. If D is larger than D_S , then the charging phase is longer than the discharging, and V_{CF} increases. Otherwise, if D is smaller than D_S , V_{CF} will decrease.

The simulated V_{CF} with different C_{FP} and a -1.5% time mismatch, and V_{CF} with different time mismatches and 200-pF C_{FP} under 3.4-V V_O are shown in Fig. 7. It can be seen that V_{CF} is very sensitive to the parasitics and time mismatch, and thus it is uncertain without regulation. Note that D and D_S are generated from the controller. Since they are controllable, D and D_S can be manually tuned to calibrate V_{CF} to the designated value $V_g/2$.

IV. PROPOSED THREE-LEVEL BUCK CONVERTER

A. Overall System Architecture

Fig. 8 shows the block diagram of the proposed three-level converter. In the controller, a type-III compensator is adopted for wide bandwidth. The ramp and clock generation block generates 180° shifted ramps and clocks, which generate the phase shifted D and D_S . Different from a conventional

three-level converter, C_F is not free switching, but real-time calibrated by the proposed V_{CF} calibration scheme to maintain $V_g/2$. The LS and drivers provide the driving signal in the appropriate voltage domain without shoot-through current.

B. Proposed V_{CF} Calibration Scheme

To calibrate V_{CF} , the two terminals of C_F , V_A and V_B , are sensed and compared with V_g and $V_g/2$. The difference between V_{CF} and $V_g/2$ results in V_{EA_CALI1} and V_{EA_CALI2} , and they are compared with Ramp and Ramp_S to generate D and D_S . D and D_S will be adjusted in accordance with V_{EA_CALII} and V_{EA_CALI2} . Thus, V_{CF} will increase or decrease accordingly until it reaches $V_g/2$.

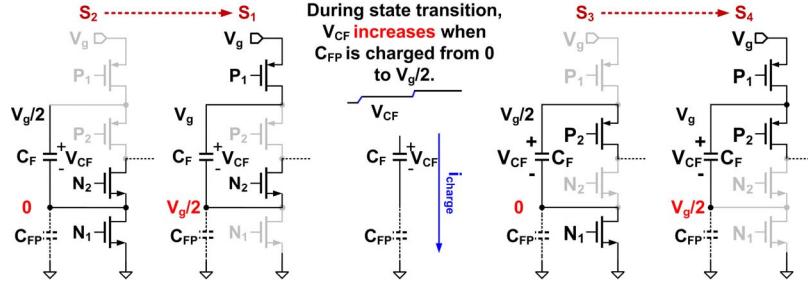
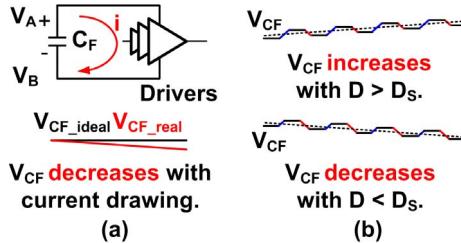
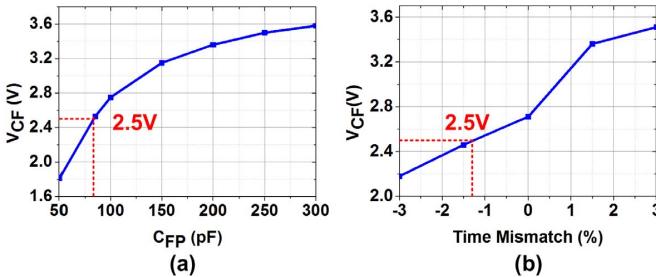
The timing diagram of the calibration process is sketched in Fig. 9. Conventionally, with no calibration, a single EA voltage is compared with the two ramps, generating almost the same D and D_S . Due to different non-idealities, V_{CF} is away from $V_g/2$, so V_X , which is either $V_g - V_{CF}$ in S_1 or V_{CF} in S_3 , is also away from $V_g/2$. We consider the case that V_{CF} is smaller than $V_g/2$ due to the non-idealities mentioned before, as an example. With the proposed calibration, V_{EA_CALII} and V_{EA_CALI2} are split from V_{EA} , and V_{EA_CALI2} will be smaller than V_{EA} , which is smaller than V_{EA_CALI1} . Thus, D increases and D_S decreases and C_F will have a longer charging than discharging time. V_{CF} increases as more charges are dumped to C_F . After several cycles, V_{CF} will return to $V_g/2$, and the difference between the two EA voltages will be small. The small time difference d between the two gate signals acts as the compensation for the non-idealities in the steady state. As a result, the overvoltage stress and reliability issues are relieved, and I_L and V_O ripple will be significantly reduced, with the possibility of higher system bandwidth.

C. Calibration Signals Generation, DDA, and CMFB Implementations

To fit into the inputs of the amplifier, the calibration signals V_{PP} , V_{PN} , V_{NP} , and V_{NN} are first generated from V_A , V_B , V_g , and $V_g/2$, as shown in Fig. 10(a). The fully DDA in Fig. 10(b) then amplifies the difference between V_{CF} and $V_g/2$ and results in the difference between V_{EA_CALI1} and V_{EA_CALI2} . Their common-mode voltages are regulated by the CMFB circuits in Fig. 10(b) based on V_{EA} . Through these mechanisms, V_{EA_CALI1} and V_{EA_CALI2} deviate from V_{EA} differentially. In normal operation, the two input pairs of the DDA follow [18]:

$$V_{PP} - V_{PN} = V_{NP} - V_{NN}. \quad (1)$$

If V_{CF} is smaller than $V_g/2$, which means $V_{PP} - V_{PN} < V_{NP} - V_{NN}$, then the sum of V_{PP} and V_{NN} is smaller than the sum of V_{NP} and V_{PN} , so the current in the left branch will be smaller than that in the right branch. As a result, $V_{EA_CALI1} > V_{EA_CALI2}$. Likewise, if $V_{CF} > V_g/2$, $V_{EA_CALI1} < V_{EA_CALI2}$, generating modulated D and D_S . The charging and discharging times for C_F are thus changed to ensure $V_{CF} = V_g/2$. In this way, the real-time calibration realizes always maintaining V_{CF} at $V_g/2$ under any conditions.

Fig. 5. V_{CF} 's dependence on the parasitic capacitance C_{FP} .Fig. 6. V_{CF} 's dependence on (a) supplied circuits and (b) time mismatches.Fig. 7. V_{CF} with (a) different C_{FP} when time mismatch is -1.5% and (b) different time mismatches when C_{FP} is 200 pF .

For each input pair, to ensure the DDA functions properly, the maximum differential input range should be smaller than

$$\Delta V_{in,max} = \pm \sqrt{\frac{2I_{SS}}{\mu_N C_{ox} \frac{W}{L}}} \quad (2)$$

where I_{SS} is the tail current of the differential pair and W/L is the aspect ratio of the input transistors [19]. Otherwise, the transistor with the smaller input voltage will be off. A large input difference requires a large I_{SS} and increases the power consumption.

Thus, in this design, the signal generation block in Fig. 10(a) aims to reduce the input difference to zero. First, $V_{NP} - V_{NN}$, which are generated from V_g and $V_g/2$, are set to zero. V_g and $V_g/2$ are scaled to 0.4 and 0.2 V, respectively, with same-ratio voltage dividers. Then they are both shifted up to 0.8 V by a source follower to fit into the input common-mode voltage range of the DDA with minimal difference. To make them both shifted up to 0.8 V, the current of the V_{NN} branch is 12 times that of V_{NP} .

Second, $V_{PP} - V_{PN}$, which are generated from V_A and V_B , are set to zero. V_A and V_B are toggling between $(V_g, V_g/2)$ and $(V_g/2, 0)$, respectively, and V_{PP} and V_{PN} can be generated to the same level from V_A and V_B by intentionally using different bias currents in the LS, which is similar to the way V_g

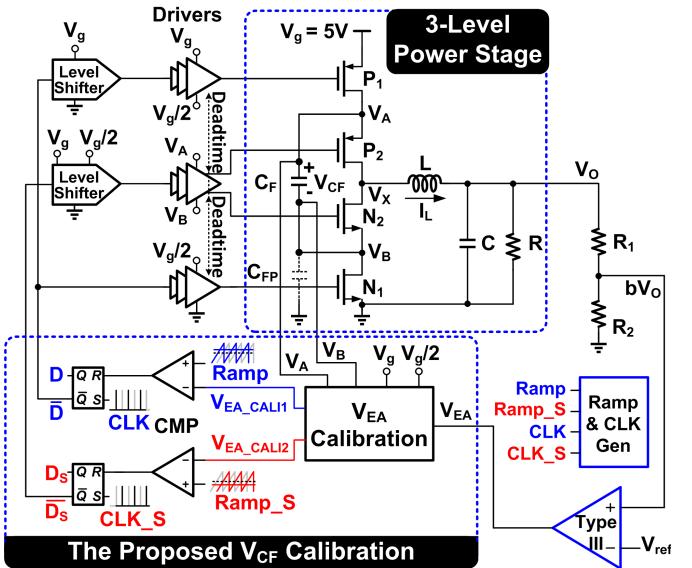


Fig. 8. Block diagram of the proposed three-level buck converter.

and $V_g/2$ are dealt with. With the same kinds of resistors and transistors and good matching of layout, the mismatch between the voltage dividers and LSs can be kept to the minimum.

For V_A and V_B , two branches of source followers are used to guarantee that the final values of V_{PP} and V_{PN} are always 0.8 V. By increasing the bias currents, which is done by increasing the current mirror size from 1 to 12 and 38, source followers 1, 2, and 3 can shift up 0.4, 0.6, and 0.8 V, respectively. V_{PP1}, V_{PN1} are either 0.6 or 0.8 V, and V_{PP2}, V_{PN2} are either 0.8 or 1 V, depending on whether V_B is 0 or $V_g/2$ as indicated in the table in Fig. 10(a). If one of the combinations of V_{PP1}, V_{PN1} and V_{PP2}, V_{PN2} is selected as the DDA's input, there will be a problem. As shown in Fig. 11(a), when the common-mode voltage of one pair of the DDA's inputs is toggling, it will bring large noise at the outputs of the DDA. Under this condition, the EA voltages have around 128-mV ripple while the ramps' amplitude is only 400 mV. As a result, the converter has sub-harmonic oscillation, with V_O ripple increased to 41 mV.

In order to fix the input voltages, V_{PP1}, V_{PN1} are selected as the inputs when they are 0.8 V and V_B is $V_g/2$; and V_{PP2}, V_{PN2} are selected when they are also 0.8 V and V_B is 0. Thus, the four inputs of the DDA are always around 0.8 V. However, since V_B is not an ideal sharp square pulse and the transmission gates' real control signals have some delays,

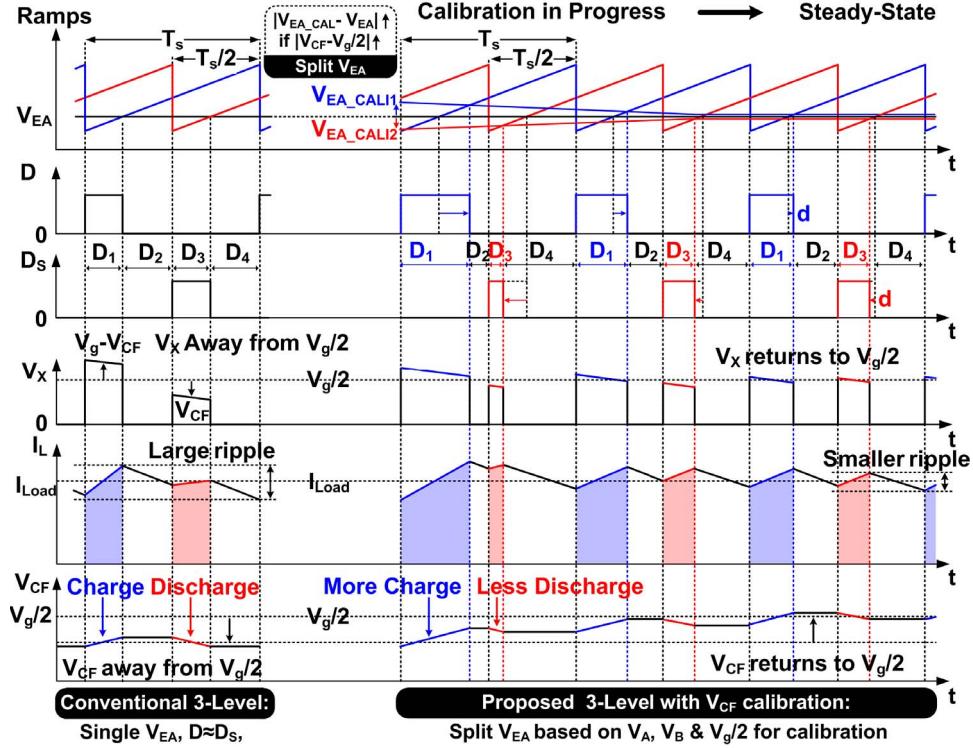


Fig. 9. Timing diagram of the calibration process.

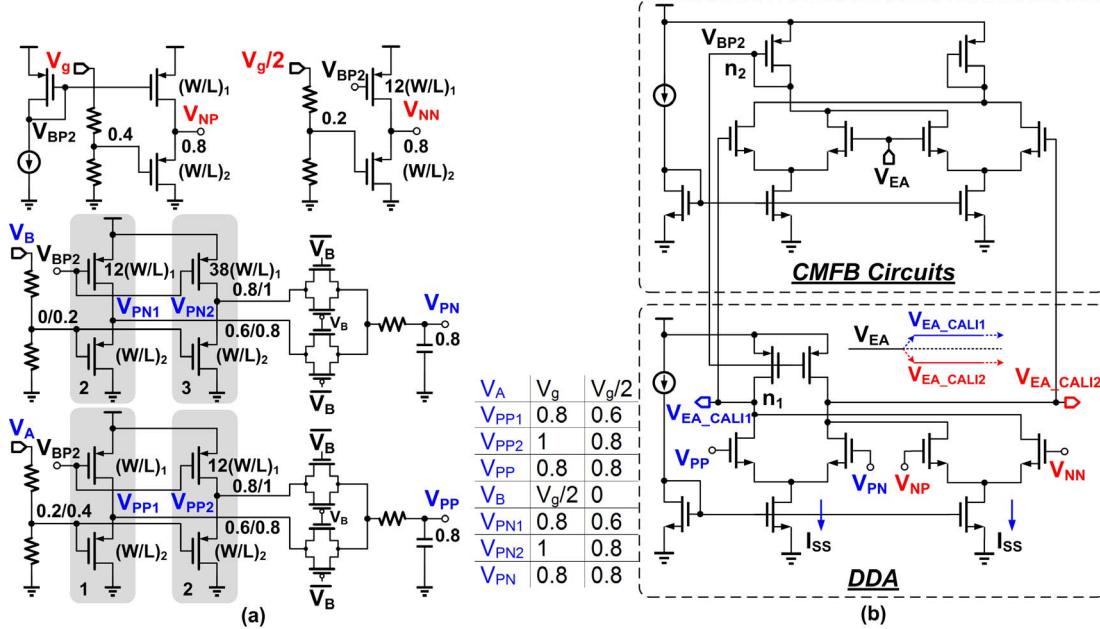


Fig. 10. Circuitry implementation of the (a) signal generation block. (b) DDA and CMFB circuits.

the selected signals (V_{PP1} and V_{PP2}) have some large peaks, as shown in Fig. 11(b). The EA voltages have around 61-mV ripple and V_O has 11-mV ripple. Though no sub-harmonic oscillation occurs in the simulation, the large EA voltage ripple is still dangerous and there is a high possibility that in the real-circuitry operation instability may happen with switching noise. Thus, an RC filter is added after the transmission gate. V_{PP} signal is flatten with this filter, as shown

in Fig. 11(c). As a result, the EA voltages' ripple is reduced to 23 mV, an acceptable and safe value, and the V_O ripple is reduced to 9 mV.

The common-mode voltages of V_{EA_CAL1} and V_{EA_CAL2} are regulated by an amplifier with a diode-connected load. The CMFB loop has two poles at node n_1 and n_2 , respectively. n_1 is a high-impedance node, so it is set as the dominant pole. To keep the loop's stability, the pole at n_2 should be pushed

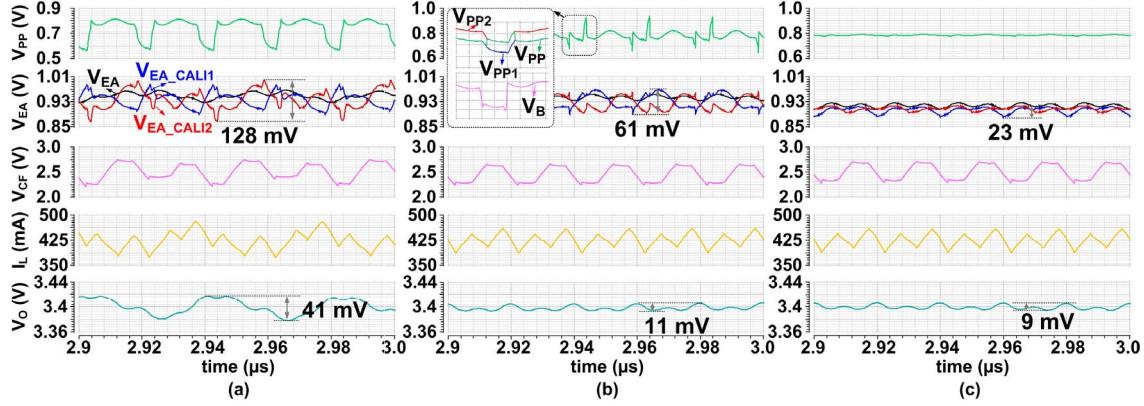


Fig. 11. V_{PP} , the three EA voltages, V_{CF} , I_L , and V_O waveforms when (a) only V_{PP1} is chosen as the input of the DDA. (b) V_{PP1} and V_{PP2} are chosen according to V_B . (c) Noise filter is added after V_{PP1} and V_{PP2} are chosen.

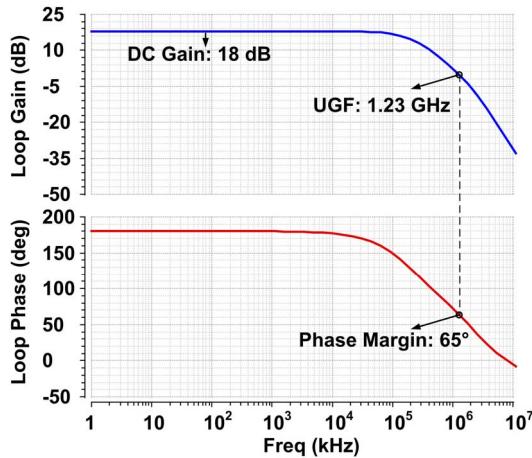


Fig. 12. Bode plots of the CMFB circuits.

to at least 1.7 times the bandwidth. This is made possible with the low-impedance diode-connected load. Bode plots of the CMFB loop are shown in Fig. 12. It has 18-dB dc gain and a 1.23-GHz unity gain frequency (UGF) with a 65° phase margin.

D. Calibration Loop's Transfer Function Analysis

To ensure the calibration loop's stability, its loop-gain function is analyzed. Assume that the charging duty cycle for C_F is D_{CH} , and the discharging duty cycle is D_{DIS} . As shown in Fig. 2, the average inductor current in the charging and discharging phase is approximately I_{LOAD} . Since the inductor current has small ripple with the three-level operation, equations for the C_F charging and discharging can be written as follows. During D_{CH}

$$\frac{dV_{CF}}{dt} = \frac{I_{LOAD}}{C_F}. \quad (3)$$

And during D_{DIS}

$$\frac{dV_{CF}}{dt} = -\frac{I_{LOAD}}{C_F}. \quad (4)$$

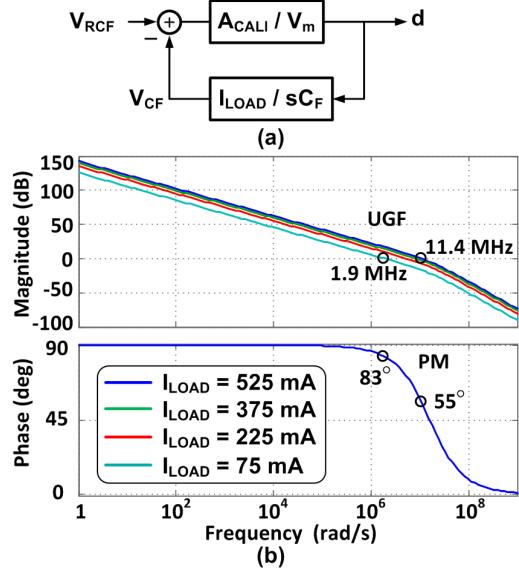


Fig. 13. (a) Small-signal model. (b) Bode plots of the calibration loop.

Thus, in one period

$$\frac{dV_{CF}}{dt} = \frac{I_{LOAD}}{C_F}(D_{CH} - D_{DIS}) + M \quad (5)$$

in which, M is the lumped change to V_{CF} from all the other parasitics. To facilitate the discussion, derivative values are represented by above-dotted letters, e.g., \dot{V}_{CF} , and perturbed quantities by hatted letters, e.g., \hat{V}_{CF} . So, in this steady state

$$\dot{V}_{CF0} = \frac{I_{LOAD}}{C_F}d_0 + M \quad (6)$$

where d_0 is the difference between D_{CH} and D_{DIS} . \dot{V}_{CF0} should be zero, and thus d_0 compensates M . To perturb the system, perturbed components are added to all steady-state quantities as follows:

$$\dot{V}_{CF0} + \hat{\dot{V}}_{CF} = \frac{I_{LOAD}}{C_F}(d_0 + \hat{d}) + M. \quad (7)$$

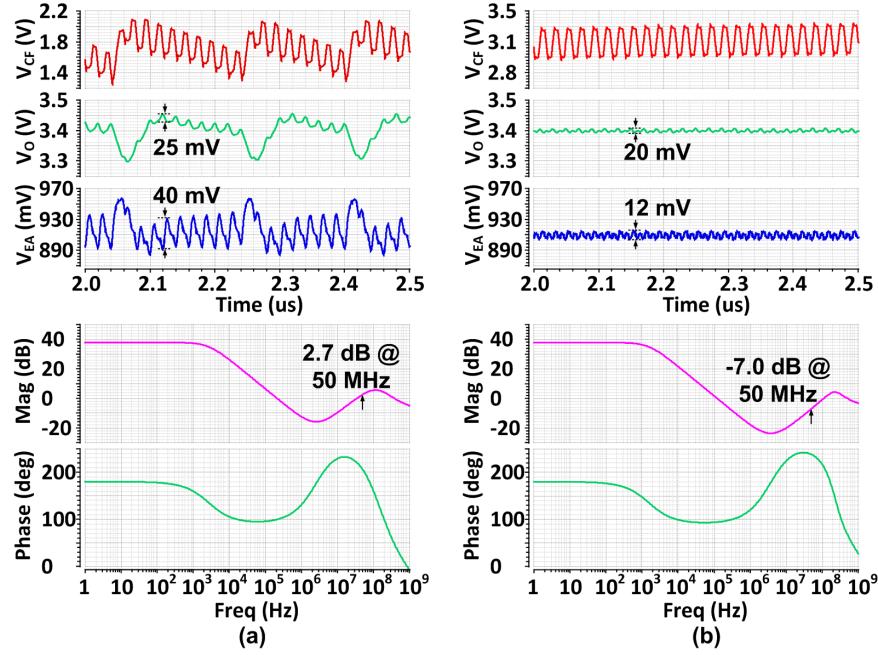


Fig. 14. Waveforms of V_{CF} , V_O , and V_{EA} , and Bode plots of the type-III compensator when (a) 10- and (b) 5-MHz bandwidth is designed without the proposed calibration.

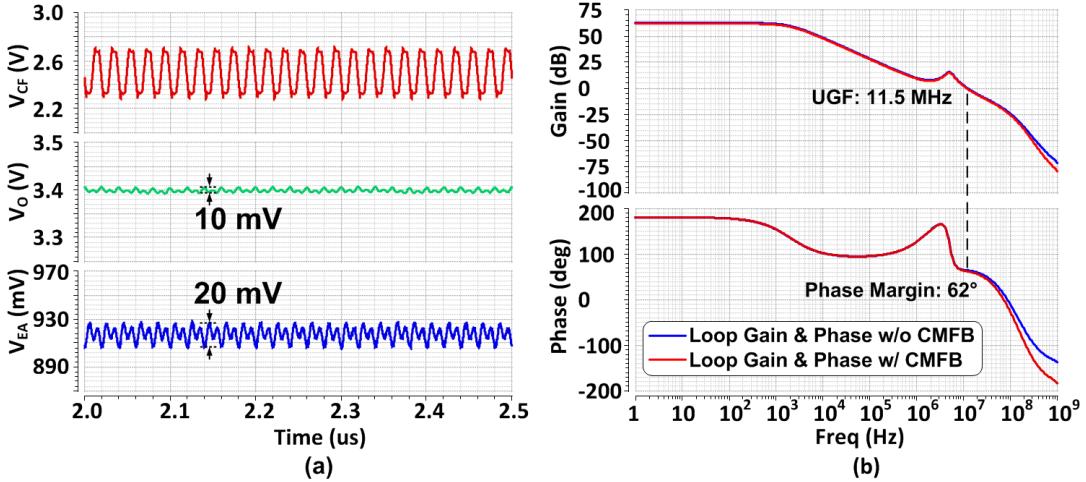


Fig. 15. (a) Waveforms of V_{CF} , V_O , and V_{EA} . (b) Bode plots of the loop with and without CMFB.

So, the perturbed relationship can be obtained as

$$\widehat{V_{CF}} = \frac{I_{LOAD}}{C_F} \hat{d}. \quad (8)$$

Taking the Laplace transform of the time-domain equations

$$\widehat{sV_{CF}} = \frac{I_{LOAD}}{C_F} \hat{d} \quad (9)$$

where \hat{d} is determined by the comparison result of V_{EA_CALI1} and V_{EA_CALI2} with the ramp signals, so

$$\hat{d} = \frac{A_{CALI}}{V_m} \widehat{V_{CF}} \quad (10)$$

in which A_{CALI} is the transfer function of the DDA and V_m is the amplitude of the ramps.

According to (9) and (10), the small-signal model of the calibration loop is sketched in Fig. 13(a), and the loop's transfer functions can be derived as

$$T_{CALI}(s) = -A_{CALI}(s) \frac{I_{LOAD}}{s C_F V_m} \quad (11)$$

in which the pole from the RC filter in the signal generation block is counted as part of $A_{CALI}(s)$. Bode plots of the calibration loop under different loading currents are shown in Fig. 13(b). By designing the gain of the DDA, the UGF of the calibration loop can be determined. Note that the RC filter discussed in this section forms the second pole and should be placed in higher frequency. The maximum UGF under 525 mA is 11.4 MHz with 55° phase margin in this design and the wide bandwidth guarantees the fast response of the calibration block.

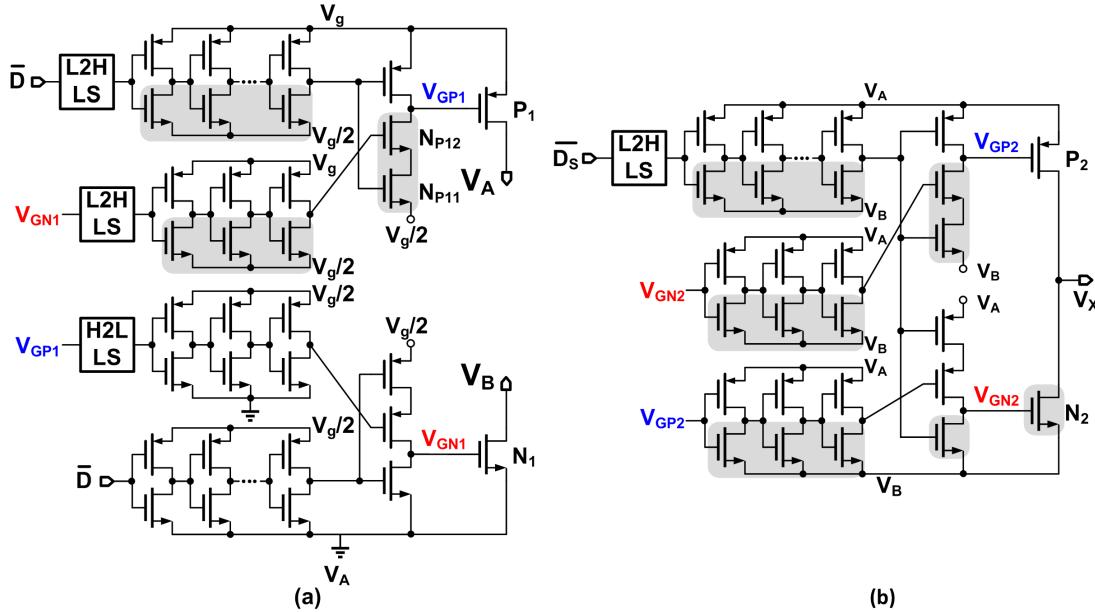
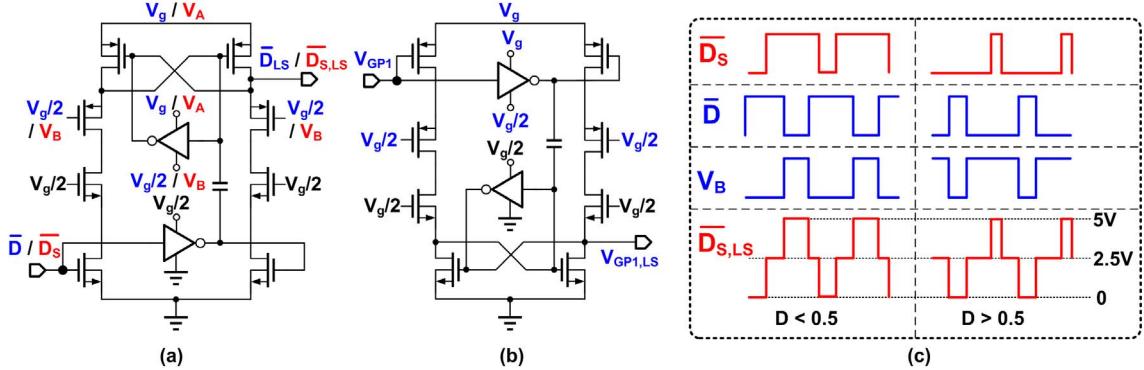
Fig. 16. Drivers for (a) P_1 , N_1 and (b) P_2 and N_2 .

Fig. 17. (a) L2H and (b) H2L LSs. (c) Original and shifted gate driving signals.

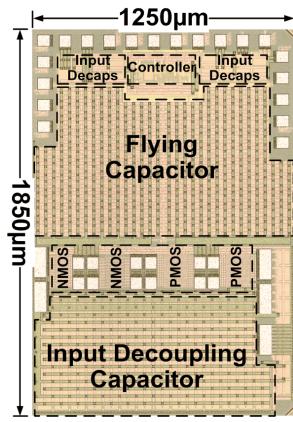


Fig. 18. Chip micrograph.

E. Type-III Compensator Design and Loop Stability

Based on the tradeoff between high efficiency and fast tracking response, the switching frequency of the three-level buck converter is designed at 50 MHz. The proposed three-level converter has a 100-nF inductor, a 10-nF output capacitor, and a 5-nF flying capacitor. The time difference d between the two gate driving signals is surely smaller than $(C_F/C)^{1/2}$,

so the three-level converter has the same transfer function as the two-level buck converter with the same LC components [10]. A type-III compensator is adopted for wide bandwidth. Without the proposed calibration, the output voltage ripple can be much larger than expected, as shown in Fig. 4(b), and thus only limited system bandwidth can be designed. If a 10-MHz bandwidth with around 60° phase margin is designed for the 50-MHz non-calibrated three-level converter, the simulated waveforms of V_{CF} , V_O , and V_{EA} are shown in Fig. 14(a), where sub-harmonic oscillation is observed. However, with a more conservative designed 5-MHz bandwidth with around 60° phase margin, the converter can work in the stable states, as shown in Fig. 14(b). Even with enough phase margin, the converter instability may still occur due to the limited noise attenuation of the compensator at the switching frequency.

The Bode plots of the compensators for the 10- and 5-MHz bandwidths are also shown in Fig. 14 and they have 2.7 and -7 dB gain at the switching frequency, respectively. This means that the switching noise from V_O will be amplified or attenuated accordingly, which can be verified by the waveforms of V_O and V_{EA} at the top. If the EA's output voltage has large noise and ripple, the comparator may be

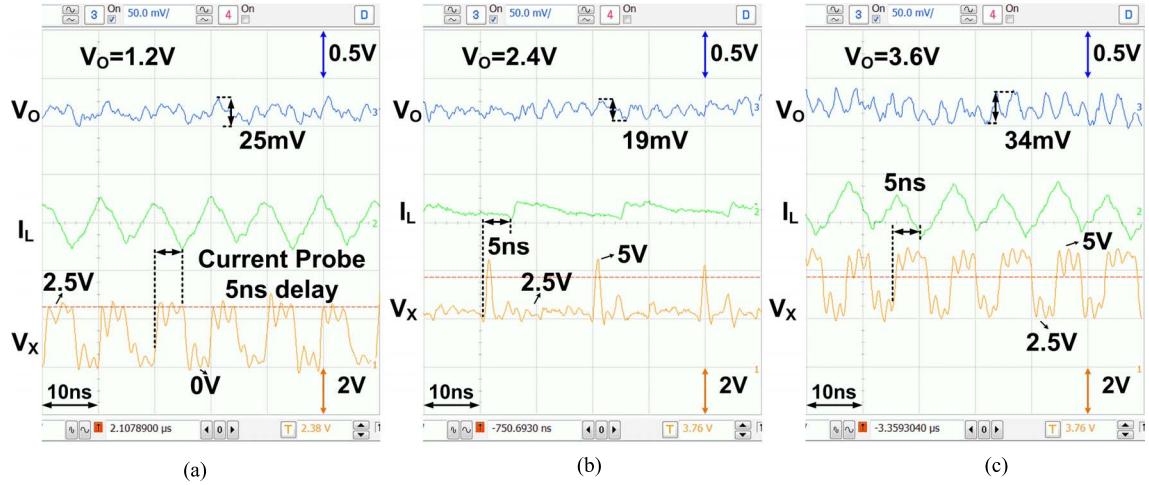


Fig. 19. Measured steady-state waveforms of V_O , I_L , and V_X when V_O is (a) 1.2, (b) 2.4, and (c) 3.6 V.

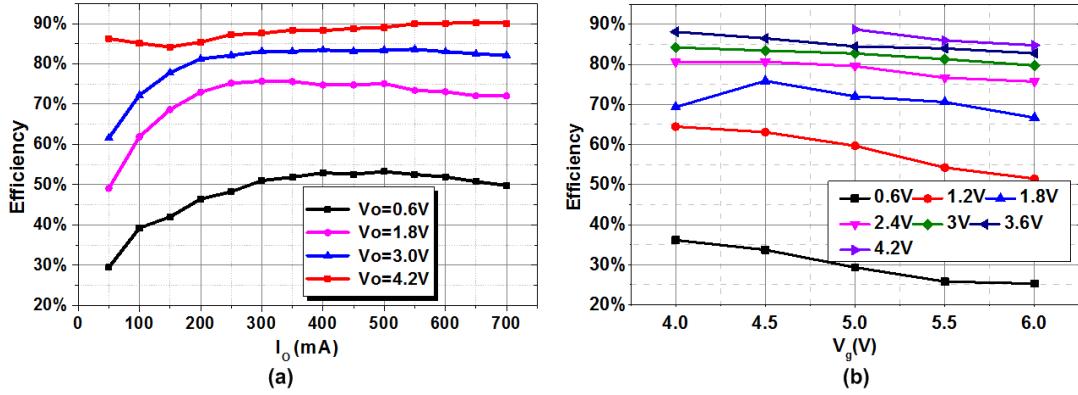


Fig. 20. Measured efficiency with different V_O under (a) different I_O when $V_g = 5$ V, and (b) different V_g .

falsely triggered so that sub-harmonic oscillation may appear. With the proposed calibration, the ripple of V_O is kept to the minimal value, so that even if the V_O ripple is amplified at the EA output with the same 10-MHz bandwidth compensator, the converter can still be stable, with the simulated waveforms shown in Fig. 15(a). The Bode plots of the loop's transfer function are shown in Fig. 15(b). It is shown that the three-level buck converter achieves 11.5-MHz UGF with 62° phase margin. The CMFB block in the proposed calibration is an additional block adding poles to the main loop, so it affects the loop's transfer function at high frequency. To reduce its influence, the UGF of the CMFB should be designed to be as high as possible. In this design, the CMFB with 1.23-GHz UGF has negligible influence on the system's UGF and phase margin.

F. Drivers and Level Shifters

In the three-level power stage, as shown in Fig. 16, the driver for N_1 is powered by $V_g/2$. For P_1 , the duty cycle signal is shifted up to the $(V_g, V_g/2)$ domain and the driver is powered by V_g and $V_g/2$. The dead-time between P_1 and N_1 is generated by a local feedback loop [20]. P_1 is turned on when V_{GP1} is low, and V_{GP1} is pulled down when N_{P11} and N_{P12} are turned on. N_{P12} is only turned on when V_{GN1} is zero,

which means N_1 is off. Thus the dead-time between P_1 and N_1 is guaranteed. Since V_{GP1} and V_{GN1} are in different voltage domains, high-to-low (H2L) and low-to-high (L2H) LSs are needed. As for P_2 and N_2 , since the source of N_2 is always connected to V_B , the gate driving signal for N_2 should in the $(V_B + V_g/2, V_B)$ domain. V_{CF} is calibrated to $V_g/2$, so N_2 's driving signal is actually in the (V_A, V_B) domain. The source of P_2 is connected to V_A , so it has the same voltage domain as N_2 and can share the same driver with N_2 . Therefore, the gate driving signal \bar{D}_S should be shifted to (V_A, V_B) domain and then fed into the driver powered by C_F [21]. The dead time is also generated by the same method without LSs. The N-transistors in shade are all deep N-well devices to have the body connected to $V_g/2$ or V_B .

To shift a signal from low voltage to high voltage, a high-speed LS is used [22], as shown in Fig. 17(a). For \bar{D} , the gates of the middle four transistors are biased to $V_g/2$ and they work as the isolation between the top high-voltage region and the bottom low-voltage region. The voltage across the capacitor is $V_g/2$, so it can shift the signal up with a very fast speed. For \bar{D}_S , the high-voltage region is biased with V_A and V_B and the isolation P-transistors are gate-biased with V_B . So \bar{D}_S can be adaptively shifted according to V_B . The H2L LS with the same working principle is also shown in Fig. 17(b), and

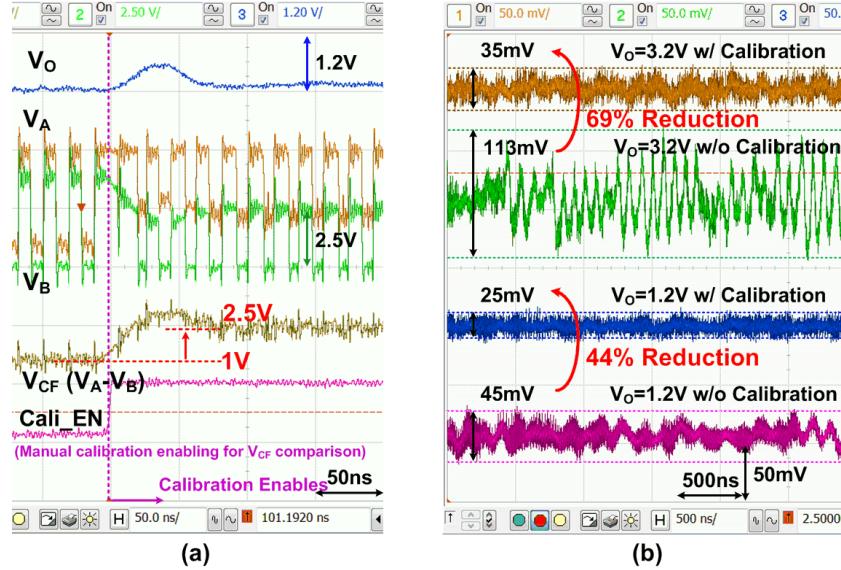


Fig. 21. Measured waveforms of (a) calibration process and (b) V_O ripple voltage with and without calibration.

the original and shifted time-domain waveforms of the gate driving signals are sketched in Fig. 17(c).

V. MEASUREMENT RESULTS

The proposed three-level buck converter occupies $1875 \mu\text{m} \times 1250 \mu\text{m}$ in a UMC 65-nm CMOS process as shown in the chip micrograph in Fig. 18. The power transistors (P_{1-2} and N_{1-2}) are implemented by standard 2.5-V I/O devices to achieve a 0.6-~4.2-V output V_O from a 5-V input V_g for high-voltage applications, such as RF PA supply or battery/USB powered devices. A 5-nF C_F is implemented on-chip by stacking MIM, MOM, and MOS capacitors. With a bond-wire package, 50-MHz switching converters require large input decoupling capacitors to reduce the ripple at V_g [23]. To increase the capacitance density, a 2.5-nF input decoupling capacitor is implemented by stacking MIM, MOM, and MOS capacitors. In this process, 5-V devices are not available. To cope with 5-V V_g , two 2.5-V N-caps are connected in series. A 100-nH air core inductor is used with 12.3-mΩ DC resistance, 100 quality factor, and 1.2-GHz self-running frequency.

The steady-state waveforms are shown in Fig. 19. V_X switches at 100 MHz, and it is either 0, 2.5 V when $V_O = 1.2$ V ($D < 0.5$) or 2.5, 5 V when $V_O = 3.6$ V ($D > 0.5$). A high-frequency current probe (Tektronics CT6) is used to measure the inductor current. It can only measure the ac current and has 5-ns delay as can be noticed from the delay between V_X and I_L . In Fig. 19(b), the duty cycle is very close to and slightly larger than 50%. When the duty cycle is 50%, ideally, V_X should be alternating between $V_g - V_{CF}$ and V_{CF} . When the duty cycle is slightly larger than 50%, with the proposed calibration, D is slightly larger than D_S , so V_X is $V_g - V_{CF}$, a short pulse of V_g and then V_{CF} . Fig. 20(a) shows the measured efficiency versus I_O under different V_O when $V_g = 5$ V. Over 90% peak efficiency is achieved when V_O is 4.2 V with a load current of 650 mA. Fig. 20(b) shows

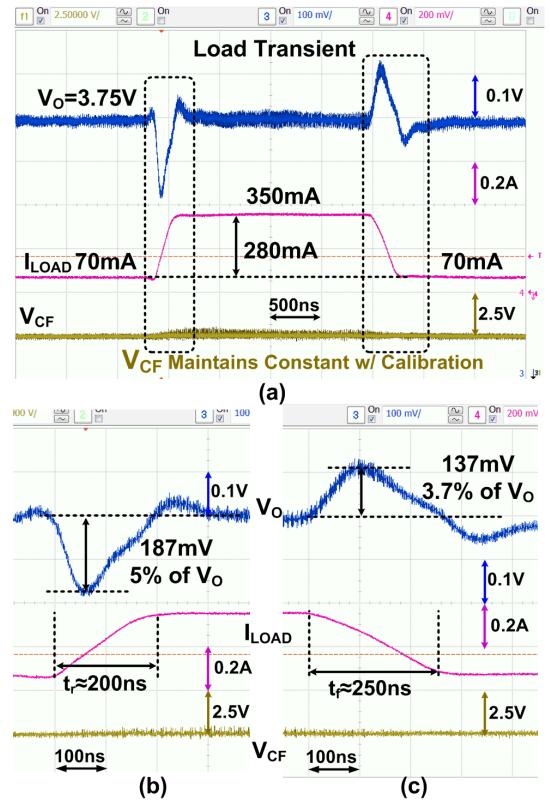


Fig. 22. Measured waveforms of (a) load transient response. Zoomed-in sections of the (b) load-increasing transient and (c) load-decreasing transient responses.

the measured efficiency versus V_g under different V_O when the load is an 8-Ω resistor. For most cases, the efficiency increases with lower V_g due to the less switching loss. The measured calibration performances are shown in Fig. 21. As shown in Fig. 21(a), before calibration is enabled, V_{CF} is about 1 V, which is far from $V_g/2 = 2.5$ V. After the calibration is enabled, V_{CF} returns to $V_g/2$ within 50 ns. As a result, up to

TABLE I
COMPARISON WITH PRIOR ARTS

Works	[5] JSSC'12	[13] PESC'08	[14] CICC'15	[19] JSSC'14	[24] JSSC'13	This Work
CMOS Tech.	130 nm	250 nm	22 nm High-Density MIM	130 nm	40 nm	65 nm (I/O Devices)
Topology	3-Level buck	3-Level buck	3-Level buck	2-Level buck	2-Level buck w/ DLDO	3-Level buck
Max. P_{OUT}	1 W	0.1 W	0.25 W	3.6 W	1.2 W	3 W
Frequency	50–200 MHz	37.5 MHz	250 MHz	30 MHz	N/A	50 MHz
C_{FLY}	18 nF	5.07 nF	5 nF	N/A	N/A	5 nF
C_{OUT}	10 nF	25.09 nF	5 nF	1 μF	100 nF	10 nF
L	$1 \text{nH} \times 4$	26.7 nH	1.5 nH	330 nH	1 μF	100 nH
V_g	2.4 V	3.6 V	1.5 V	3.3 V	2.2–3.6 V	5 V
V_o	0.4–1.4 V	1 V	0.4–1.2 V	0.45–2.4 V	0.8–3 V	0.6–4.2 V
V_o -Range/ V_g	42%	28%	53%	59%	N/A	72%
Max. Efficiency	77%	69.7%	72%	86.6%	94%	90%
Up-tracking	Open-loop	N/A	286 ns/V	670 ns/V	133 ns/V	29 ns/V
Down-tracking					(only 0.18 V step measured)	23 ns/V
V_{CF} Calibration	No	No	Once 32 cycles	N/A	N/A	Real-Time

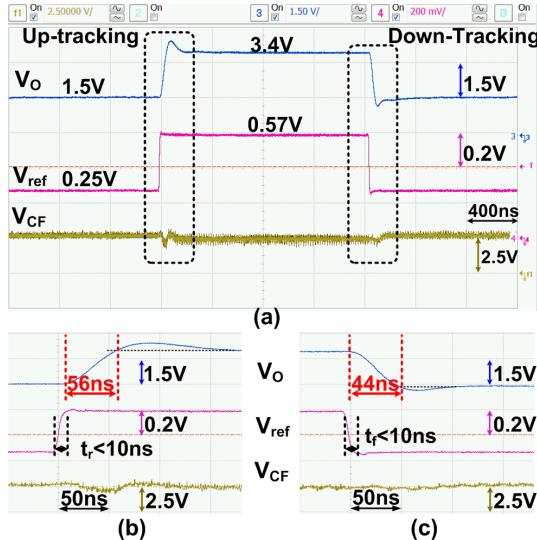


Fig. 23. Measured waveforms of (a) reference-tracking response. Zoomed-in sections of the (b) up-tracking and (c) down-tracking responses.

69% V_o ripple reduction from the V_{CF} calibration is observed in Fig. 21(b).

Fig. 22 shows the measured transient response at $V_o = 3.75$ V with a load step from 70 to 350 mA. Fig. 22(b) and (c) shows the zoomed-in sections of the load-increasing and load-decreasing transient responses. The converter has unobservable load regulation, and only has 3%–5% overshoot or undershoot during the above 1.12-A/ μs transient. Fig. 23 shows the measured reference-tracking response with an 8- Ω resistive load. Fig. 23(b) and (c) shows the zoomed-in sections of the up-tracking and down-tracking responses. With the reduced LC values and the well-optimized type-III compensator, the up/down reference-tracking-times are only 56 and 44 ns, respectively, between 1.5 and 3.4 V. This is much faster than the buck converter with a similar switching frequency designed for DVS [19] and a digital-low

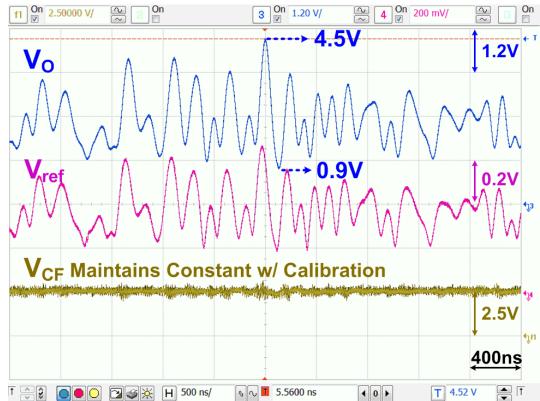


Fig. 24. Measured ET response with 10-MHz LTE envelope.

dropout regulator (LDO)-assisted buck converter [24]. Due to the real-time calibration, V_{CF} is always constant during the transients, as shown in Figs. 22 and 23. To further measure the functionality of the three-level converter, the ET performance is shown in Fig. 24. It is measured with an 8- Ω resistive load and real 10-MHz LTE envelope. Without the help of a linear amplifier, the converter can track the envelope ranging from 0.9 to 4.5 V within a 10-ns delay with 82% efficiency at 28-dBm output power. Thus, it is a good PA power supply candidate, both for average power tracking mode and ET mode for 10-MHz LTE applications.

A comparison with prior arts is shown in Table I. The efficiency of the proposed converter is higher than those of the first four works. Although it is lower than that of [24], it operates at a higher voltage rating of 5 V compared with 3.6 V, delivers a larger power of 3 W instead of 1.2 W, and is implemented with a less advanced technology of 65 nm versus 40 nm. Moreover, the design complexity is significantly increased in [24] with a digital-LDO to assist the transient response. Our work also achieves a wider

output voltage range and much faster reference-tracking speed than all prior arts, including the one with five times faster switching frequency of 250 MHz implemented with 22-nm core devices [14] and the one with a digital-LDO [24]. Among the integrated three-level converters, it is the only one with real-time V_{CF} calibration in the tens of megahertz range.

VI. CONCLUSION

In this paper, a high-frequency three-level buck converter is presented for high-voltage and reference-tracking applications. A real-time V_{CF} calibration scheme is proposed to continuously regulate V_{CF} to $V_g/2$. Thus, it avoids breakdown issues, ensures ripple reduction performance and extends the converter's bandwidth to a higher frequency. The proposed three-level buck converter is fabricated in a standard 65-nm CMOS process, operating at 50 MHz with a 100-MHz equivalent switching frequency, and 5-V supply voltage. Experimental results show that it achieves a 0.6–4.2-V wide output range, 69% ripple reduction, 90% efficiency, and a well-optimized fast reference-tracking speed of 23–29 ns/V, which prove it to be a good candidate in fast reference-tracking applications for SoCs. The proposed converter also shows the ability to track a 10-MHz LTE envelope ranging from 0.9 to 4.5 V within a 10-ns delay without using any of the hybrid fast-converters required in previous works, which proves it to be a good candidate for PA supply applications.

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