1.23-pJ/bit 25-Gb/s Inductor-Less Optical Receiver With Low-Voltage Silicon Photodetector

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***Abstract*— This paper presents the design and measurement results of an inductor-less and power-efficient 25-Gb/s optical receiver in 65-nm TSMC technology. Furthermore, the design and characteristics of a novel 850-nm low-voltage silicon-on-insulator-based all-silicon photodetector (Si-PD) are demonstrated. The proposed receiver front end consists of an inverter-based feedback transimpedance amplifier and three stages of inverter-based Cherry–Hooper post-amplifier. To this structure, local positive feedback and third-order interleaved active feedback are added to increase the bandwidth of the front end. Measurement results show that the receiver front end has a transimpedance gain of 69.4 dBΩ, a bandwidth of 13.6 GHz, and an input-referred current noise of 3.28 μA_{rms}. It occupies only 0.0056 mm^2 and consumes 30.8 mW at 1.1-V supply voltage. The proposed Si-PD has a responsivity of 0.05 A/W (at 850 nm), a dark current of 0.02 nA, and a bandwidth of 12.6 GHz at 0-V bias voltage. For a bit error rate of 10^{-12}, the optical receiver with a wire-bonded Si-PD has a sensitivity of 46 and 54 μA_{p-p} at data rates of 20 and 25 Gb/s, respectively, at a reverse-bias voltage of 0.41 V. The energy efficiency of the all-silicon 850-nm optical receiver is 1.23 pJ/bit at 25-Gb/s data rate. The receiver front end was also measured with an electrical input signal with supply voltages lower than 1.1 V. For an input sensitivity of 5 mV_{p-p}, the receiver front end has energy efficiencies of 0.425 and 0.8 pJ/bit at data rates of 20 and 25 Gb/s, for supply voltages of 0.85 and 1 V, respectively.**

***Index Terms*— Energy efficient, interleaved active feedback (IAFB), optical interconnects, optical receiver, positive feedback (PFB), silicon photodetector (Si-PD), transimpedance amplifier (TIA).**

I. Introduction

In RECENT years, the ever-growing bandwidth demand in data centers and supercomputers has pushed the need for high-speed optical interconnects for board-to-board and chip-to-chip connections. Directly modulated vertical-cavity surface-emitting lasers (VCSELs) are cost-effective and energy-efficient transmitter solutions predominantly used in such applications [1]–[3]. In this context, using a mature and reliable complementary metal–oxide–semiconductor (CMOS) technology provides a cost-effective solution for optical transceivers. However, the design of a power-efficient optical receiver with a high gain-bandwidth product is more challenging in CMOS technology compared with SiGe, GaAs, and InP technologies, due to the lower transition frequency (f_T) of CMOS.

When the technology is not fast enough to design a receiver with a high gain-bandwidth product, bandwidth extension techniques are employed. Inductive peaking is a common bandwidth enhancement technique for an efficient optical receiver at the cost of chip area [4]–[10]. However, in high bandwidth density multi-channel applications, area-efficient transceivers are desirable [11]. Compact bandwidth extension techniques include active inductors [12], third-order interleaved active feedback (IAFB) [13], multi-peaking bandwidth extension [14], and local positive feedback (PFB) [11], [15]. In a single-ended dc-coupled multistage amplifier, optimizing the active inductors increases the design complexity of the biasing for each stage [16]. The third-order IAFB and multi-peaking bandwidth extension techniques enhance the bandwidth of uniform multistage amplifiers by separating the poles. They have been implemented using cascaded first-order differential or single-ended common-source (CS) amplifiers. In this paper, the IAFB enhances the bandwidth of a cascade of second-order Cherry–Hooper (CH) post-amplifiers. Local PFB is also employed.

The proposed receiver front end consists of an inverter-based feedback transimpedance amplifier (TIA) and a post-amplifier chain based on three stages of an inverter-based CH amplifier. The bandwidth of the receiver is increased by using IAFB and local PFB. This paper demonstrates the design and experimental results of the proposed receiver front-end fabricated in TSMC 65-nm technology. Furthermore, measurement results are obtained for a low-voltage all-silicon photodetector (Si-PD) fabricated in a silicon-on-insulator (SOI) technology [17]. The proposed optical receiver is an area- and power-efficient design suitable for multi-channel applications. Furthermore, it can be implemented in an SOI CMOS platform for monolithic integration with the proposed Si-PD to reduce packaging complexities.

The rest of this paper is organized into five sections. Section II discusses the bandwidth extension of the cascaded CH amplifiers with third-order IAFB. Also, it presents the design of the proposed receiver front end. The measurement results of the fabricated chip with an electrical input signal are

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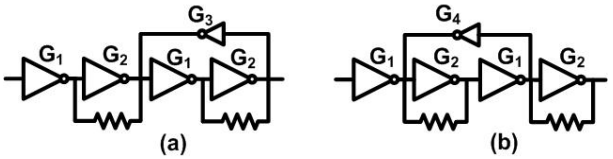

Fig. 1. Block diagram of two cascaded CH amplifiers with AFB. (a) Feedback signal is added to the input of the first section of a CH. (b) Feedback signal is added to the input of the second section of a CH.

presented in Section III. Section IV demonstrates the design of the new grating-assisted Si-PD, and the measurement results of the optical front end with wire-bonded Si-PD. Finally, the conclusion is given in Section V.

II. Receiver Design

In this section, the bandwidth enhancement of the cascaded second-order inverter-based CH amplifier with third-order IAFB is discussed. Also, the design of the proposed optical receiver and the tradeoff among bandwidth, power dissipation, group-delay variation, and noise is presented.

An inverter-based CH amplifier is a low-power design with a reasonable gain-bandwidth product, especially in low-voltage technologies [18]. It consists of two inverters with resistive feedback (R_f) around the second inverter. Based on our simulation results, for the same gain and power dissipation, an inverter-based CH amplifier can provide a larger bandwidth than two cascaded CS amplifiers.

A. Bandwidth Extension of Cascaded CH Amplifiers With Active Feedback

Two forms of third-order active feedback (AFB) are considered in a chain of CH amplifiers. Fig. 1(a) shows the cascade of two CH amplifiers when the AFB connects to the input of the first section of the second CH (G_3). Fig. 1(b) shows the feedback signal added to the input of the second section of the first CH (G_4).

First, the transfer function of two cascaded CH amplifiers with AFBs G_3 and G_4 are calculated. For simplicity, it was assumed that the sizes of G_3 and G_4 are small and their loading on G_1 and G_2 are negligible. In practice, the size of the feedback inverter is lower than 0.1 times that of the CH's inverters. Also, all stages have the same capacitive load C_L (mainly caused by the gate–source capacitor of the following stage). The transfer function of each stage is calculated by

$$G_1(s) = \frac{-g_{m1}}{Y_{L1}},\quad Y_{L1} = g_{ds1} + sC_L + \frac{g_{m2} + g_{ds2} + sC_L}{1 + g_{ds2}R_f + sC_LR_f} \tag{1}$$

$$G_2(s) = \frac{1 - g_{m2}R_f}{1 + g_{ds2}R_f + sC_LR_f},\quad G_4(s) = \frac{-g_{m4}}{Y_{L1}} \tag{2}$$

$$G_3(s) = \frac{-g_{m3}}{Y_{L2}},\quad Y_{L2} = g_{ds2} + sC_L + \frac{g_{m2} + g_{ds1} + sC_L}{1 + g_{ds1}R_f + sC_LR_f} \tag{3}$$

where R_f is the feedback resistor, g_{mi} is the sum of the transconductances of the PMOS and the NMOS transistors in the inverter, and g_{dsi} is the sum of the output conductance of PMOS and NMOS transistors in the inverter. Note that G_2 (s) is the voltage-to-voltage gain of the stage consisting of the inverter G_2 and the feedback resistor. Assuming $g_m \gg g_{ds}$ and $1 \gg g_{ds2}R_f$, the transfer functions are simplified as follows:

$$G_1(s) = \frac{-g_{m1}(1 + sC_LR_f)}{g_{m2} + 2sC_L + s^2C_L^2R_f},\quad A_1 = g_{m1}/g_{m2} \tag{4}$$

$$G_2(s) = \frac{1 - g_{m2}R_f}{1 + sC_LR_f},\quad A_2 = g_{m2}R_f - 1 \tag{5}$$

$$G_3(s) = \frac{-g_{m3}(1 + sC_LR_f)}{g_{m2} + 2sC_L + s^2C_L^2R_f},\quad \beta_a = g_{m3}/g_{m2} \tag{6}$$

$$G_4(s) = \frac{-g_{m4}(1 + sC_LR_f)}{g_{m2} + 2sC_L + s^2C_L^2R_f},\quad \beta_b = g_{m4}/g_{m2}. \tag{7}$$

The transfer function of a CH amplifier is calculated by

$$H_{CH}(s) = G_1(s)G_2(s) = \frac{A_1A_2}{1 + \frac{2s}{\omega_g} + \frac{s^2}{\omega_r\omega_g}} = \frac{A_{CH}}{D(s)} \overset{g_{m2}R_f \gg 1}{\longrightarrow} \omega_{p1,2} = \omega_r\left(-1 \pm j\sqrt{|A_2|}\right) \tag{8}$$

where $\omega_r = 1/C_LR_f$ and $\omega_g = g_{m2}/C_L$. The transfer function of the two cascaded CH amplifiers with AFB G_3 or G_4 is given by

$$H_{AFB}(s) = \frac{G_1^2G_2^2}{1 - G_1G_2G_j} \quad \text{where } j = 3,\ 4. \tag{9}$$

By substituting the $G_i, i = 1, 2, 3,$ and 4

$$H_{AFB-a}(s) = \frac{A_{CH}^2}{D^2(s) + A_{CH}\beta_a(1 + s/\omega_r)} \tag{10}$$

$$H_{AFB\text{-}b}(s) = \frac{A_{CH}^2}{D^2(s) + A_{CH}\beta_b(1 + s/\omega_r)} \tag{11}$$

where H_{AFB-a} is the transfer function of the circuit in Fig. 1(a) and H_{AFB-b} is the transfer function of the circuit in Fig. 1(b). Using the same size feedback inverters G_3 and G_4 results in equal feedback gain ($\beta_a = \beta_b = \beta$). Therefore, $G_3 = G_4 = G_f$ and as a result, the transfer functions H_{AFB-a} and H_{AFB-b} are equal. The effect of the AFB on the CH structure is presented through numerical simulations. The gain of the CH stage is set to 2.3, $\omega_r = 80$ rad/ns and $\omega_g = 150$ rad/ns.

Fig. 2 shows the variation of the gain, gain peaking, and normalized bandwidth of two cascaded CH amplifiers with respect to various feedback gains (β). The normalized bandwidth is calculated by dividing the bandwidth of the amplifier

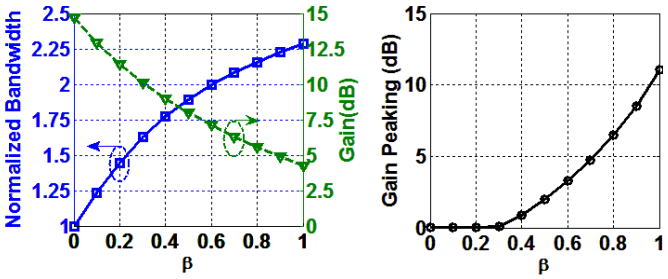

Fig. 2. (a) Variation of the bandwidth and gain of two cascaded CH amplifiers for various feedback gains (β). (b) Associated gain peaking.

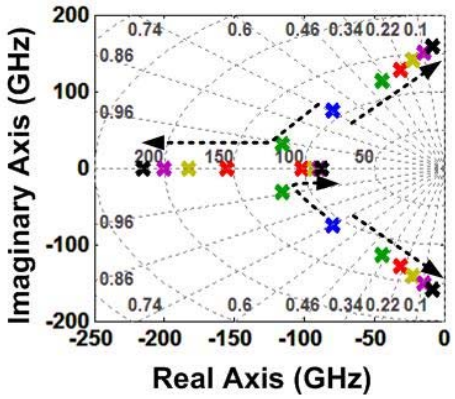

Fig. 3. Poles plot of two cascaded CH amplifiers for different gains of AFB.

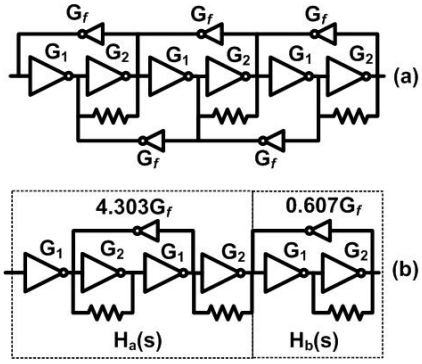

Fig. 4. (a) Block diagram of three cascaded CH amplifiers with uniform IAFB. (b) Its equivalent circuit with two non-uniform non-IAFBs.

with AFB to the bandwidth of the amplifier without AFB. Increasing the feedback gain reduces the gain of the amplifier and increases its bandwidth, and generates gain peaking for a feedback gain larger than 0.3.

Fig. 3 shows the pole locations for two cascade CH amplifiers for variation of the feedback gain β from 0 to 1. The arrows in Fig. 3 show the trend as the feedback gain increases. Without feedback, the system has two repeated pairs of complex conjugate poles (blue crosses in Fig. 3). The AFB pushes one pole to high frequency, leaving one real pole and a pair of complex conjugate poles to shape the frequency response. Increasing the feedback gain moves the two dominant poles to lower damping factor which generates peaking in the magnitude frequency response. Next, the AFBs are combined to improve the bandwidth of a multistage CH amplifier.

Fig. 4(a) shows the block diagram of three cascaded CH amplifiers with uniform IAFB. The transfer function of the circuit is obtained by

$$H_{\mathrm{IAFB}}(s) = \frac{G_1^3 G_2^3}{1 - 5G_1G_2G_f + 3G_1^2G_2^2G_f^2} = \frac{G_1^2G_2^2}{1 - 4.303G_1G_2G_f} \cdot \frac{G_1G_2}{1 - 0.607G_1G_2G_f}. \quad (12)$$

By substituting the expressions for G_1, G_2, and G_f in (12), the transfer function of the three cascaded CH amplifiers with

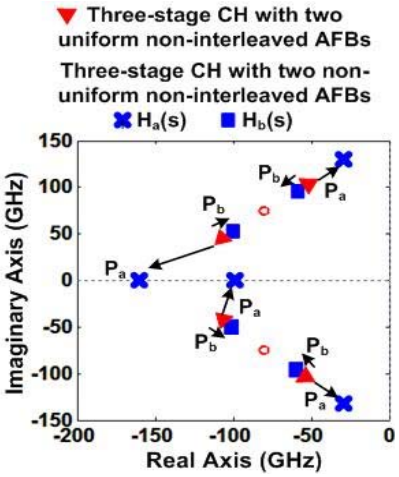

Fig. 5. Pole splitting behavior of three cascaded CH amplifiers with uniform IAFB for feedback gain of $\beta = 0.08$.

uniform IAFB is calculated by

$$H_{\mathrm{IAFB}}(s) = H_a(s) \cdot H_b(s) = \frac{A_{\mathrm{CH}}^2}{D^2(s) + 4.303A_{\mathrm{CH}}\beta(1 + \frac{s}{\omega_r})} \cdot \frac{A_{\mathrm{CH}}D(s)}{D^2(s) + 0.607A_{\mathrm{CH}}\beta(1 + \frac{s}{\omega_r})}. \quad (13)$$

The first term in (13) has the same denominator as the transfer functions in (10) and (11) but with a feedback gain of $P_a \times \beta$, where $P_a = 4.303$. Also, the second term has the same denominator as the two cascaded CH amplifiers with a feedback gain of $P_b \times \beta (P_b = 0.607)$. Therefore, the three cascaded CH amplifiers with uniform IAFB with the feedback gain of β have the same transfer function as the three cascaded CH amplifiers with two non-uniform non-IAFBs. This observation is similar to that of [13]. Fig. 4(b) shows the block diagram of the equivalent circuit with two non-uniform non-IAFBs.

Replacing the two weighted feedbacks in Fig. 4(b) with two uniform non-interleaved feedbacks with a gain of β, which means $P_a = P_b = 1$, results in a transfer function with eight complex poles, occurring as two sets of repeated poles (red triangles in Fig. 5). By giving the amplifier non-uniform non-interleaved feedback, (i.e., $P_a = 4.303$ and $P_b = 0.607$) poles no longer occur in repeated pairs (shown in blue). The arrows in Fig. 5 show the effect of coefficients P_a and P_b on the poles' movement in comparison with two uniform non-interleaved feedbacks. Note that both transfer functions also have a pair of conjugated zeros.

Fig. 6 compares the frequency response of three cascaded CH amplifies with two non-uniform non-IAFBs and with two uniform non-IAFBs for $\beta = 0.08$. In comparison with an amplifier with two uniform non-IAFBs, using uniform IAFB increases the bandwidth by 32% at the cost of 3.7-dB gain reduction.

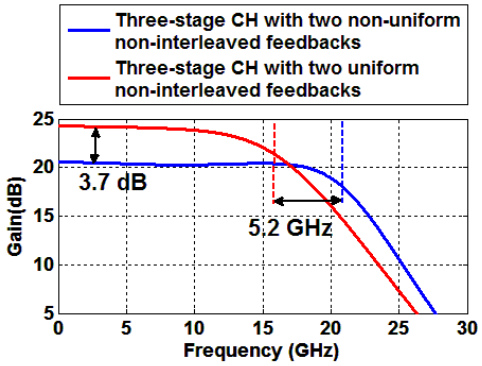

Fig. 6. Simulated frequency response for three cascaded CH amplifiers with two non-uniform non-IAFBs (or uniform IAFB) and with two uniform AFBs.

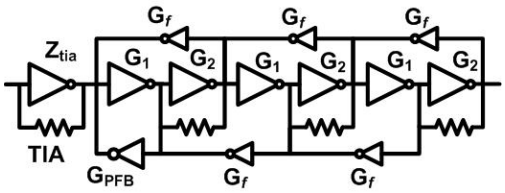

Fig. 7. Block diagram of the proposed receiver front end.

B. Proposed Optical Receiver

Fig. 7 shows the block diagram of the proposed receiver front end. The post-amplifier chain is connected to the output of an inverter-based feedback TIA. A small PFB is added in the first section of the first CH amplifier to extend the bandwidth of the TIA by creating a negative resistance at the output of the TIA [15]. The transfer function of the proposed receiver front end including the TIA and PFB is presented in Appendix A. Also, Appendix B indicates a discussion about the effect of feedback inverters on the low-frequency input-referred current noise of the receiver front end.

In designing the receiver, the CH inverters are assumed to be the same size as the TIA inverter. In an inverter, selecting an equal size for the PMOS and NMOS transistors maximizes the total transconductance for a given input capacitance, which increases its gain-bandwidth product [19]. Also, the equal bias voltage of the inverters leads to the same current density in the TIA, CH amplifier, and feedback inverters. The width of the transistors in the TIA is swept to find an optimum gain-bandwidth product. Also, the size of the IAFB inverters and PFB inverter are swept for maximum bandwidth with a flat response. In simulations, capacitance was added to each transistor to model additional metal coupling capacitance not part of the intrinsic transistor model. The gate–source, gate–drain, and drain–source capacitors of $0.11 \times W$ fF/μm, $0.1 \times W$ fF/μm, and $0.08 \times W$ fF/μm obtained from layout extraction were added, where W is the width of the transistor in μm. Table I compares simulation results of the proposed optical receiver to an optical receiver consisting of an inverter-based TIA and CH amplifiers without IAFB and PFB. In this simulation, the load capacitor of the receiver front end is chosen based on the anticipated capacitive load of the following

TABLE I

COMPARISON OF THE SIMULATION PARAMETERS AND RESULTS FOR A THREE-STAGE CH

	TIA and three-stage CH (reference)	TIA and three-stage CH with IAFB and PFB
TIA feedback resistor	300 Ω	300 Ω
CH feedback resistor	150 Ω	215.5 Ω
MOS width (CH, TIA)	25 µm	25 µm
PFB ratio	—	0.16
IAFB ratio	—	0.064
Input Cap. (pads+PD)	100 *f*F	100 *f*F
Load Cap.	100 *f*F	100 *f*F
Supply voltage	1.2 V	1.2 V
Bias current	22.7 mA	24.1 mA
Transimpedance gain	76.6 dBΩ	76.6 dBΩ
Bit rate	30 Gb/s	30 Gb/s
3 dB bandwidth	12.34 GHz	16.65 GHz
Total output noise	8.65 mV_{rms}	11.76 mV_{rms}
Group delay variation	±2.1 ps	±3.4 ps
Maximum eye opening for 30 $\mu A_{p\text{-}p}$ input	135 $mV_{p\text{-}p}$	181.8 $mV_{p\text{-}p}$
Power dissipation	27.3 mW	29 mW

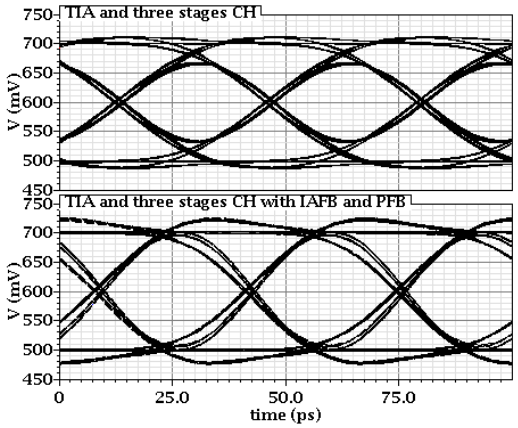

Fig. 8. Eye diagrams of the reference receiver front end and the proposed receiver front end for 30 Gb/s random data with 30-μA_{p-p} input.

circuits such as the integrated decision circuit and an output buffer.

With the same transimpedance gain, the proposed receiver front end has a 35% larger bandwidth, while the power consumption increases only by 6.2%. The proposed design also has a ±1.3 ps larger group-delay variation in comparison with the reference design. The group-delay variation of the proposed receiver is ±0.07 ps larger than ±10% of the 30-Gb/s bit unit interval (UI), $\pm 0.1 \times$ UI is ±3.33 ps, which is the typical limit for group-delay variation [20]. Fig. 8 compares the output eye diagram of the reference receiver front end (top) and the proposed receiver front end (bottom) for 30-Gb/s 30-μA_{p-p} random data.

The maximum eye opening of the proposed front end is 46 mV larger than the maximum eye opening of the reference design. It has slightly larger pattern-dependent jitter resulting from a slight increase in the group-delay variation. Although

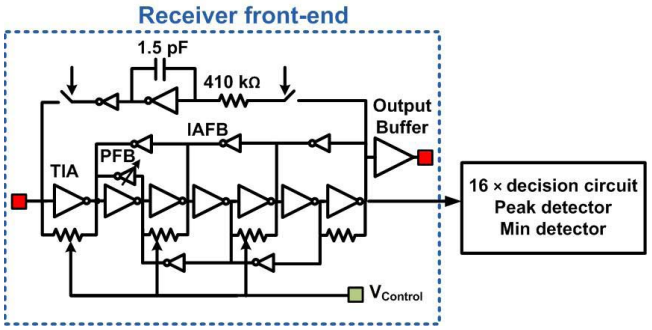

Fig. 9. Block diagram of the proposed optical receiver.

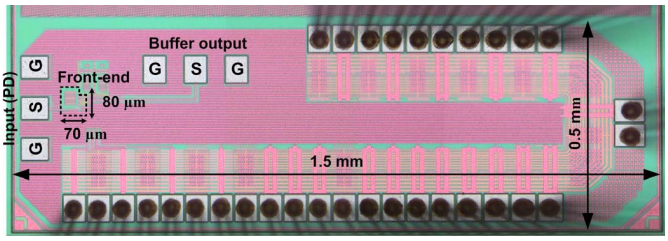

Fig. 10. Micrograph of the proposed optical receiver.

the proposed receiver has a signal-to-noise ratio (SNR) slightly less than the SNR of the reference design, the larger peak-to-peak eye of the proposed front end provides a better performance by relaxing the design requirement of the following circuits after the receiver front end such as integrated decision circuits.

The performance of the proposed receiver was studied for various MOSFET fabrication process corners in combination with ±10% resistance variation, ±10% supply variation, and temperature variation. Based on the simulation results, the proposed receiver is stable across process, voltage and temperature (PVT) variation. For the slow–slow corners, the proposed receiver exhibits a peaking of at most 0.5 dB in the magnitude of the frequency response, and a group-delay variation between ±4.5 and ±8.7 ps. It shows a flat frequency response with group-delay variation lower than ±2.2 ps for the fast–fast corners. The proposed receiver shows 15-dB gain variation and 6-GHz (36%) bandwidth variation across PVT while the reference design shows 27-dB gain variation and 4.7-GHz (37.8%) bandwidth variation across PVT. A regulator should be used to combat gain and bandwidth variation due to the supply voltage changes. Also, the gain variations can be partially reduced by use of automatic gain control circuitry.

The design parameters of the fabricated optical receiver are modified based on post-layout simulation results for optimum performance for a targeted data rate of 25–30 Gb/s. The required transimpedance gain is determined based on the input-referred noise of the optical receiver, and the required peak-to-peak amplitude of the integrated decision circuits.

The block diagram of the fabricated optical receiver is shown in Fig. 9. It consists of an analog front end with a variable gain control (VGC) circuit and an offset cancellation feedback which, based on the simulation result, generates a 2.8-MHz low-frequency cutoff. An output buffer, 16 decision circuits, a minimum detector, and a peak detector are loading the front end. However, this paper focuses on the front end of the optical receiver and presents its experimental results.

The PMOS and NMOS transistors in the inverter-based feedback TIA and three CH amplifiers have a width of 25 μm and use the minimum length of 60 nm. The feedback resistors in the TIA and CH amplifier are 300 and 200 Ω, respectively. The PMOS and NMOS transistors in the inverter-based IAFB are 2.25 μm wide and 60 nm in length. The first stage of the CH amplifier has a fixed inverter-based PFB with PMOS and NMOS transistors 4 μm wide and a 3-bit variable PFB with PMOS and NMOS transistors 0.5, 1, and 2 μm wide. The effective width of the PFB transistors can be adjusted from 4 μm for control bits of 000 to 7.5 μm for control bits of 111. There is also a variable resistor in the TIA and in the two stages of post-amplifier that controls the gain and bandwidth of the front end by applying a voltage through the V_{Control} pin in Fig. 9. A 7-μm-wide NMOS transistor in parallel with the fixed feedback resistor implements the variable resistor. Based on the simulation result, the minimum resistance of the NMOS variable resistor is approximately 60 Ω for V_{Control} of 1.2 V. The output buffer is a PMOS CS amplifier with a width of 25 μm and a length of 60 nm and it has an on-chip 100-Ω load resistance. There are on-chip shift registers that enable/disable switches in the optical receiver for various receiver configurations to provide an optimized performance.

III. Receiver Front-End Characterization

This section presents a complete characterization of the receiver front end with an electrical input signal. Fig. 10 shows the micrograph of the optical receiver fabricated in TSMC 65-nm CMOS technology. The total size of the chip is 1.5 mm × 0.5 mm, while the receiver front end including the offset compensation loop occupies only 0.0056 mm^2 (70 μm × 80 μm) of the area. The fabricated chip is packaged in a ceramic quad flat package CQFP80 and is partially wire bonded. The cavity size of the package is 7.6 mm × 7.6 mm. The input and output pads of the front end (shown with red squares in Fig. 9) interface to two 40-GHz ground–signal–ground probes in the electrical measurement and later the input pad is wire-bonded to a fabricated SOI-based all-Si-PD. Due to the large cavity size of the CQFP80, relatively long wire bonds for the supply voltage affect the receiver performance as discussed later in this section. An ATmega328 microcontroller is programmed to generate the required bit stream for loading the on-chip shift registers that control the switches in the optical receiver.

The receiver front end without the output buffer (4.4 mW) consumes 26.4 mW at 1.1-V supply voltage. Next, the experimental results of the frequency response and the transient response of the proposed receiver front end are discussed.

A. Frequency-Response Measurement

The frequency response of the receiver front end is measured using a 50-GHz microwave network analyzer

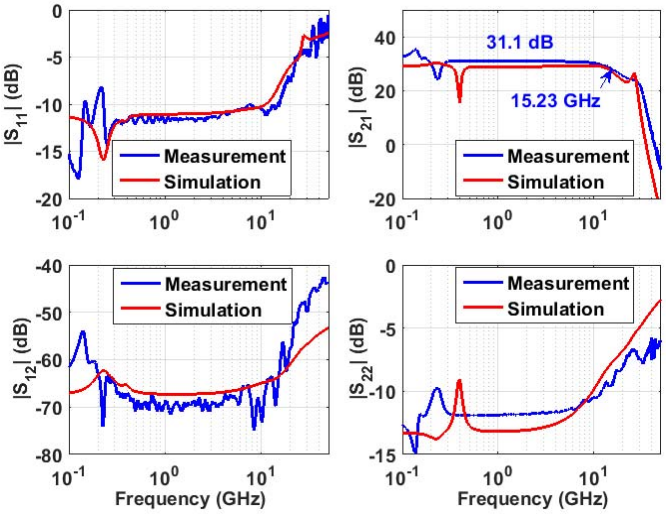

Fig. 11. Measured S-parameter in comparison with the simulated S-parameter.

(Agilent PNA-X N5245A). Fig. 11 compares the measured S-parameters of the receiver with the post-layout simulation results. In this measurement, the offset cancellation feedback is enabled, while the 3-bit PFB is set to 000, and the VGC is disabled by applying 0 V to the V_{Control}, which results in the maximum gain for the front end. The effect of a long wire-bond for the supply voltage is modeled as a 4-nH inductor. As expected from the simulation, there is a low-frequency resonance due to the inductance of the supply voltage's long wire-bond and the on-chip decoupling capacitors. Note that a single-ended structure is more sensitive to the power supply noise, substrate noise, and package resonances. However, in comparison with a differential topology, it consumes less power, which is favorable for a low-power design. Using an on-chip regulated power supply can reduce the supply noise in the single-ended topologies [21]. The magnitude of the measured S_{21} is approximately 2 dB larger than the simulation, while its bandwidth is about 1.4 GHz smaller. The S_{21} obtained in simulation also shows a low-frequency cutoff of 1.9 MHz which is smaller than the low-frequency cutoff 2.8 MHz in the transimpedance simulation. For frequencies greater than 10 GHz, the large difference between the measured and simulation S_{12} resulted from a signal coupling between the input and output pads.

The transimpedance gain (Z_T) of the front end is extracted from the measured S-parameters by

$$Z_T = Z_0 \frac{S_{21}}{1 - S_{11}} \tag{14}$$

where Z_0 is the characteristic impedance of 50 Ω. The simulated and measured transimpedance gain is compared in Fig. 12. The transimpedance gain is approximately 68.1 dBΩ (or 2541 Ω), which is 2.2 dB larger than the simulation result. It shows a 3-dB bandwidth of 13.2 GHz, which is 1.8 GHz smaller than the simulation result.

The increase in the transimpedance gain and the reduction in the bandwidth of the fabricated chip may be due to larger

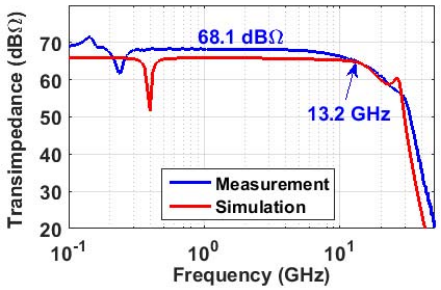

Fig. 12. Extracted transimpedance gain from measured S-parameter in comparison with the simulated transimpedance gain.

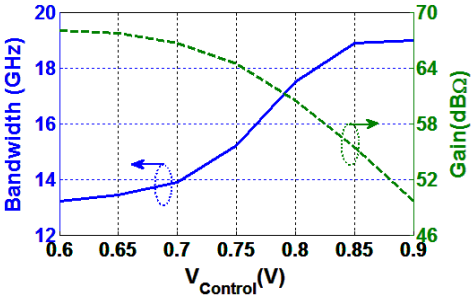

Fig. 13. Measured bandwidth and gain of the receiver front end for various V_{Control}.

feedback resistors in the TIA and post-amplifier relative to the designed values due to process variation. The higher resistance value in the offset cancellation loop also reduces the low-frequency cutoff of the receiver. Based on the simulation result, the transimpedance gain of the front end before the output buffer is 7.8 dB larger than after the output buffer, and it has a slightly larger bandwidth.

By setting the 3-bit PFB to 111 (3-bit PFB = 111), the measured transimpedance gain increases by 1.3 dB–69.4 dBΩ, while the bandwidth increases by 0.4 GHz (13.6 GHz). Applying a voltage larger than 0.6 V to the V_{Control} reduces the voltage gain and enhances the bandwidth of the front end, as shown in Fig. 13. The receiver shows a maximum gain-bandwidth product of 33.16 THz·Ω for a V_{Control} of 0.6 V for a bandwidth of 13.2 GHz and gain of 2512 Ω. Furthermore, a minimum gain-bandwidth product of 5.74 THz·Ω is obtained for a V_{Control} of 0.9 V for a bandwidth of 19 GHz and gain of 302 Ω.

B. Noise Measurement

The noise standard deviation is measured at the front end output without applying any input signal to the receiver. The total standard deviation (σ_{Total}) is 4.11 mV_{rms}. The receiver noise is calculated from $\sigma_{\text{RX}}^2 = \sigma_{\text{Total}}^2 - \sigma_{\text{Scope}}^2$, where the noise standard deviation (σ_{Scope}) of a disconnected 30-GHz scope is measured to be 0.47 mV_{rms}. The noise standard deviation of the front end (σ_{RX}) is 4.08 mV_{rms} when the offset cancellation feedback is enabled, the 3-bit PFB is set to 000, and 0 V is applied to the V_{Control}. By enabling all PFB for control bits of 111 (3-bit PFB = 111), the noise standard deviation of the receiver increases to 4.87 mV_{rms}. Applying 0.9 V to the

TABLE II
FRONT-END PERFORMANCE FOR VARIOUS RECEIVER CONFIGURATIONS

	3bit PFB =000 $V_{Control}$ = 0 V	3bit PFB =111 $V_{Control}$ = 0 V	3bit PFB =000 $V_{Control}$ = 0.9 V
Transimpedance gain	68.1 dBΩ	69.4 dBΩ	49.6 dBΩ
Bandwidth	13.2 GHz	13.6 GHz	19 GHz
Output noise (σ_{RX})	4.08 mV_{rms}	4.87 mV_{rms}	10.7 mV_{rms}

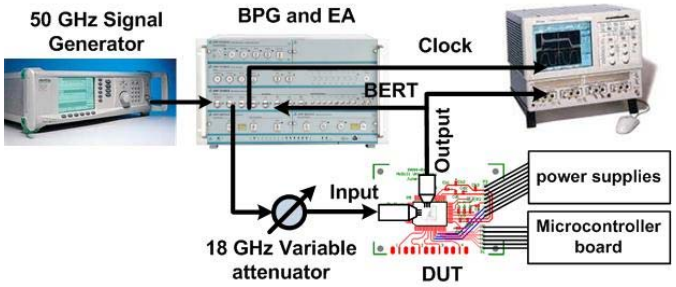

Fig. 14. Test setup for transient measurement with an electrical input signal.

V_{Control} increases the noise standard deviation of the receiver to 10.7 mV_{rms}. Table II summarized the performance of the receiver front end for various receiver configurations.

C. Transient Measurement

For the transient measurements presented in this section, the offset cancellation feedback is enabled, the 3-bit PFB is set to 000, and the VGC is disabled by applying 0 V to the V_{Control}.

The test setup used for the bit error rate (BER) and eye diagram measurements is shown in Fig. 14. A 400 mV_{p-p} output of a bit pattern generator (BPG) is attenuated with an 18-GHz variable attenuator to reduce the amplitude of the input signal. The attenuator changes from 0 to 69 dB with 1-dB steps. Then, the signal is applied to the input pad of the receiver front end. The amplified output is detected by an error analyzer (EA) for BER measurement and by a 30-GHz scope for eye diagram measurement. The loss of the cables and connectors is ignored in the measurement results.

The BER measurement for nonreturn to zero (NRZ)-OOK pseudorandom binary sequence (PRBS) $2^7 - 1$ data for different bit rates is shown in Fig. 15(a). Fig. 15(b) shows the sensitivity of the receiver front end for BER lower than 10^{-12} and different PRBS patterns.

The sensitivity of the front end at a bit rate of 30 Gb/s increases from 7 mV_{p-p} for PRBS 2^7-1 data to 11.25 mV_{p-p} for PRBS $2^{31} - 1$ data, which corresponds to a 2-dB power penalty; for the other measured bit rates, the power penalty is 1 dB. The power penalty for a longer length of PRBS data results from larger jitter and baseline wander due to the low cutoff frequency of the receiver front end [20]. To decrease the baseline wander effect on the long PRBS pattern, the low-frequency cutoff of the receiver should be in the range of a few hundred kilohertz. This can be achieved by increasing the resistance and capacitance of the offset cancellation feedback by a factor of three to four.

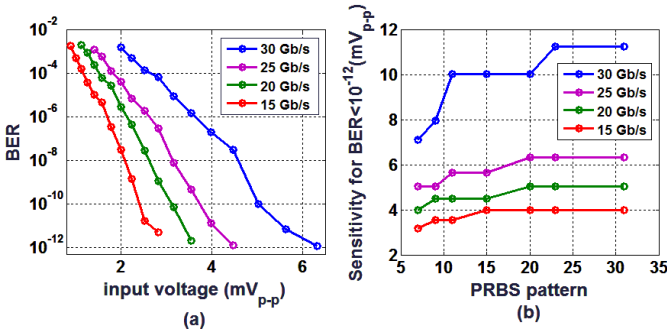

Fig. 15. (a) BER measurement for various bit rates with respect to the received peak-to-peak input voltage. (b) Input sensitivity for BER lower than 10^{-12} with respect to different lengths of PRBS data.

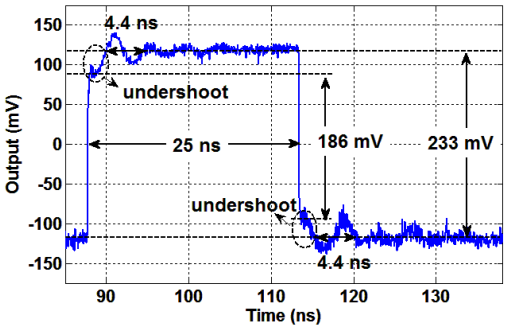

Fig. 16. Step response of the receiver front end.

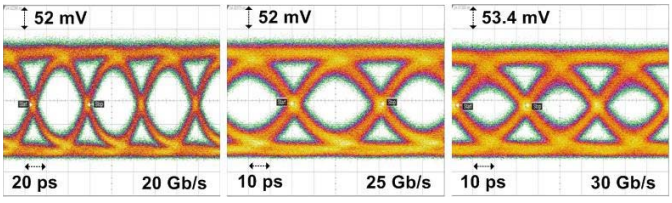

Fig. 17. Eye diagrams for 20, 25, and 30 Gb/s PRBS $2^{31} - 1$ NRZ-OOK data for 8-mV_{p-p} input signal.

The step response of the receiver front end is measured to study the effect of the low-frequency notch on the time domain operation. Fig. 16 shows the response of the receiver front end for a 20-MHz square-wave input. The step response shows undershoot and ringing with an approximate period of 4.4 ns or a frequency of 227 MHz, which is the frequency of the notch in the measured S_{21}. As shown in Fig. 16, the undershoot degrades the average peak-to-peak amplitude by 20% that results in 0.98-dB power penalty [20].

Fig. 17 shows the output eye diagram of the front end for various bit rates of NRZ-OOK PRBS $2^{31}-1$ data for an 8-mV peak-to-peak input signal. The larger intersymbol interference at 30 Gb/s reduces the maximum eye opening by 55% in comparison with the maximum eye opening at 20 Gb/s.

The energy efficiency of the receiver was explored by measuring the BER across supply voltage at various data rates of PRBS $2^7 - 1$ data pattern. Fig. 18(a) shows the receiver sensitivity for BER lower than 10^{-12} for different power dissipations, while the related supply voltage is shown. At each

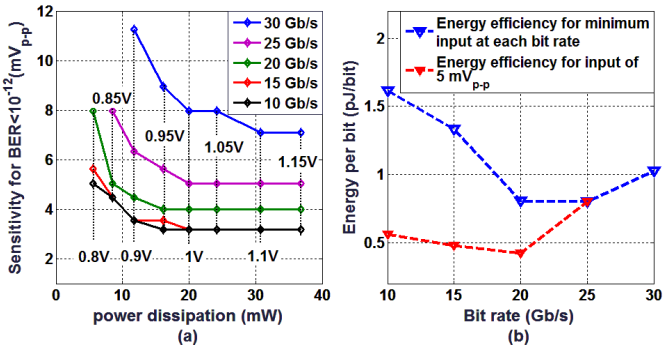

Fig. 18. (a) Input sensitivity of the front end for BER less than 10^{-12} for various power dissipations. (b) Energy efficiency for different bit rates.

data rate, the sensitivity improves before becoming constant as the supply voltage and hence power dissipation is increased.

Fig. 18(b) indicates the energy per bit with respect to the bit rate. The blue dashed line is calculated based on the lowest power dissipation that provides the minimum peak-to-peak input sensitivity for each bit rate, while the red dashed line is calculated based on the lowest power dissipation for input signal sensitivity of 5 mV_{p-p} at bit rates of 25 Gb/s and lower.

The proposed receiver front end has an energy efficiency of 1.03 pJ/bit at 30-Gb/s bit rate for an input sensitivity of 7 mV_{p-p} and supply voltage of 1.1 V. The receiver operates at minimum sensitivity with an energy efficiency of 0.8 pJ/bit for bit rates of 25 and 20 Gb/s, respectively. For the input sensitivity of 5 mV_{p-p}, the front end shows an energy efficiency of 0.425 pJ/bit at 20 Gb/s at a supply voltage of 0.85 V.

IV. Receiver Measurements With Wire-Bonded Si-PD

The proposed receiver front end is packaged with a novel all-Si-PD, as reported in [17]. This section summarizes the design and characterization of the Si-PD. Then, the measurement results of the optical front end with wire-bonded Si-PD are discussed.

A. Proposed Grating-Assisted All-Silicon Photodetector

Silicon with high absorption coefficient at short wavelengths enables monolithic integration of an optical receiver with a photodetector. This integration reduces the cost and complexity of the packaging and provides a more reliable optical system [22], [23]. However, the bandwidth of a Si-PD fabricated in a bulk technology is limited to sub-GHz due to the slow diffusion current of carriers generated by absorbed photons outside the depletion region of the photodetector [24]. Several techniques have been demonstrated to reduce the slow diffusion of carriers in Si-PDs at the cost of responsivity degradation [22]–[25]. For increasing the responsivity, most of the modified Si-PDs are designed for avalanche performance (avalanche photodetector) with high reverse-bias voltage. Furthermore, their optical receiver requires power-hungry equalization techniques for high-speed operation.

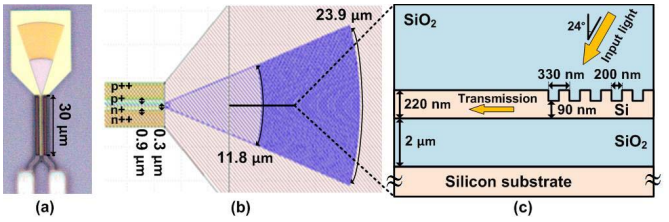

Fig. 19. (a) Micrograph of the all-Si-PD. (b) Top view of the novel Si-PD with focusing GC. (c) Side view of the GC.

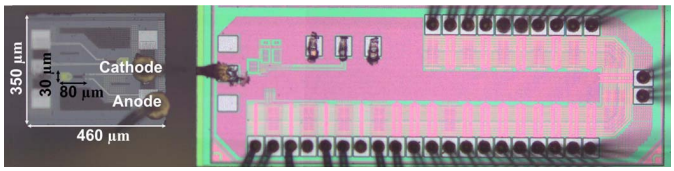

Fig. 20. Micrograph of the proposed optical receiver with the wire-bonded all-Si-PD.

The bandwidth of the Si-PD can be improved by fabricating the photodetector on an SOI platform. The insulator between the active area of the Si-PD and the substrate enhances the bandwidth of the PD without any equalization techniques [26]. However, the responsivity of this type of PD is limited by the thickness of the silicon layer on the insulator. In [27], we proposed a novel SOI-based Si-PD in which the incident light is directed horizontally using a grating coupler (GC), significantly increasing optical absorption in the depletion area, thereby increasing the PD's responsivity. We demonstrated an optimized design of the grating-assisted Si-PD along with its performance at 14-V reverse-bias voltage in [17], while in this paper the Si-PD operates at a reverse-bias voltage lower than 0.5 V. Fig. 19 shows the micrograph of the photodetector along with its design parameters. It is fabricated in an SOI technology with 220-nm silicon thickness at the Institute of Microelectronics IME-A∗ Star. The parasitic capacitance and resistance of this Si-PD are estimated to be 2.3 fF and 57 Ω, respectively. The parasitic capacitance of the 65 μm × 65 μm bond pad is estimated with ANSYS high frequency structure simulator software to be approximately 15 fF.

The Si-PD has a responsivity of 0.05 A/W, a dark current of 20 pA, and a broad bandwidth of 12.6 GHz at 0-V reverse-bias voltage. For a reverse-bias voltage greater than 10 V, the responsivity rapidly increases. The Si-PD has a responsivity of 0.3 A/W, a dark current of 2 μA, and a bandwidth of 16.4 GHz at 14-V reverse-bias voltage.

High bandwidth at low reverse-bias voltage makes this photodetector a perfect candidate for low-voltage applications. Furthermore, it eliminates the equalization techniques required to compensate the low bandwidth of other types of Si-PD fabricated in a bulk CMOS technology. In addition, the photodetector potentially can be implemented in an SOI-based CMOS technology for monolithic integration with an optical receiver.

B. Optical Measurement

Fig. 20 shows the micrograph of the proposed optical receiver with the wire-bonded Si-PD. The total size of the

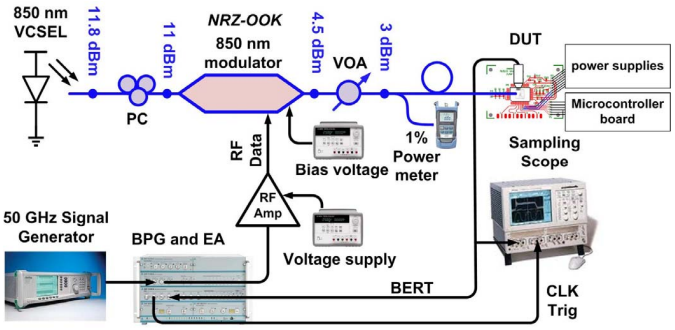

Fig. 21. Test setup for transient measurement with an optical input signal.

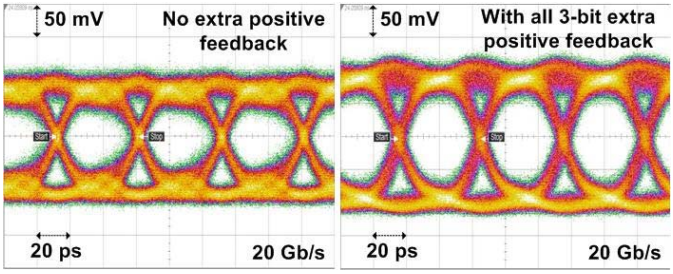

Fig. 22. Eye diagram for 20-Gb/s PRBS $2^{31}-1$ NRZ-OOK data for 0-dBm average optical power.

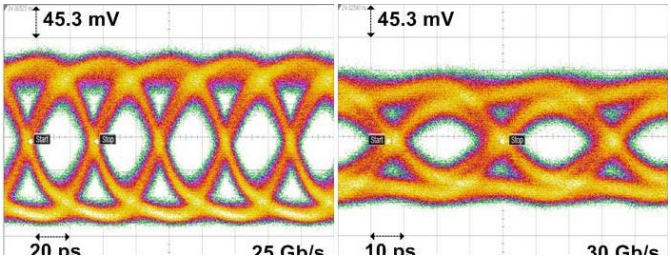

Fig. 23. Eye diagrams for 25- and 30-Gb/s PRBS $2^{31}-1$ NRZ-OOK data for 0-dBm average optical power.

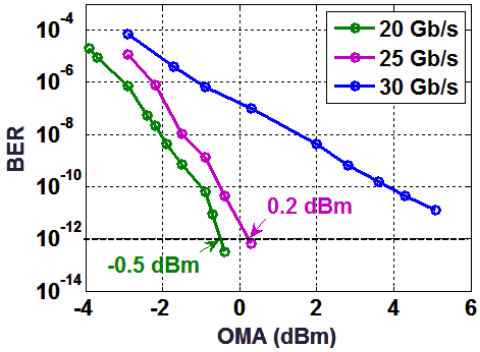

Fig. 24. BER measurement for NRZ-OOK PRBS 2^7-1 data.

photodetector chip is 350 μm $\times$ 460 μm, while the Si-PD occupies only 30 μm $\times$ 80 μm of the area.

Fig. 21 shows the test setup used for the eye diagram and BER measurements. A continuous wave generated by a VCSEL source from Thorlabs with 11.8-dBm optical power at 848.2 nm is injected through a polarization controller (PC) with 0.5-dB insertion loss. A 40-GHz Mach–Zehnder modulator with an extinction ratio of 14 dB and an insertion loss of 6.5 dB at 850 nm is driven by a baseband signal from the output of the BPG. For reducing the SNR in BER measurement, the modulated data are injected into a variable optical attenuator. A 99%–1% directional coupler is used to monitor the average received optical power. Because the input GC is polarization sensitive, the modulated data are then injected into another PC. The maximum optical power on the GC of the Si-PD is 2.5 dBm. The modulated optical signal is launched to the Si-PD and converted to a photocurrent. The optical front end converts the photocurrent into a voltage and amplifies it. The cathode of the Si-PD is wire-bonded to the input pad of the optical front end, which has a dc voltage of 0.41 V. To reduce the length of the wire bond of the photodetector, the anode of the Si-PD is wire-bonded to the bottom metal plate of the CQFP80 cavity, which is grounded. The optical front end has a 1.1-V supply voltage, and 0 V is applied to the V_{Control} for maximum receiver gain while the 3-bit PFB is swept from 000 to 111 to find an optimum performance at each bit rate.

Fig. 22 shows the output eye diagram for 20-Gb/s NRZ-OOK PRBS $2^{31}-1$ data for an average optical power of 0 dBm. Eye diagrams are compared when the 3-bit PFB is set to 000 and 111. As expected, the front end has a larger gain that increases the peak-to-peak output voltage. Furthermore, the quality of the eye diagram is improved due to the increased bandwidth.

Fig. 23 shows the output eye diagram of the front end for 25- and 30-Gb/s bit rates NRZ-OOK PRBS $2^{31}-1$ data for an average optical power of 0 dBm. At 25-Gb/s bit rate, the 3-bit PFB is set to 111. At 30-Gb/s bit rate, the 3-bit PFB is set to 000 since the quality of the eye diagram is slightly better than for control bits of 111.

Next, the BER is measured for the NRZ-OOK PRBS 2^7-1 data at different bit rates. Fig. 24 shows the BER measurement with respect to the optical modulation amplitude (OMA). For bit rates of 20 and 25 Gb/s, the 3-bit PFB is set to 111, while at 30 Gb/s, it is set to 000. The optical front end has input sensitivities of -0.5 and 0.2 dBm for BER of 10^{-12} at bit rates of 20 and 25 Gb/s, respectively. The highest data rate of the receiver is limited by the low bandwidth (12.6 GHz) of the photodiode at a low reverse-bias voltage and the large group-delay variation caused by the inductance of the Si-PD's wire bonds. Furthermore, the BER is measured for the NRZ-OOK PRBS $2^{31}-1$ data. The sensitivity of the optical receiver degrades by 0.3 and 4 dB for bit rates of 20 and 25 Gb/s, respectively.

The peak-to-peak current sensitivity is calculated from the OMA sensitivity and responsivity of the Si-PD. The input current sensitivity of the proposed optical front end is 46 μA_{p-p} at 20 Gb/s, which results in an input-referred current noise of 3.28 μA_{rms} [28].

Table III summarizes the performance of the proposed optical receiver with wire-bonded Si-PD and compares it with previously published high-speed optical front ends for

TABLE III
PERFORMANCE SUMMARY OF THE PROPOSED OPTICAL FRONT END COMPARED WITH RECENTLY PUBLISHED WORK IN A SIMILAR PROCESS TECHNOLOGY AND AT A SIMILAR DATA RATE

	JSSC'14 [5]	JSSC'15 [7]	JSSC'15[8]	JSSC'16 [29]	JSTQE'16 [23]	CICC'17 [30]	This work
Technology	CMOS 65 nm	CMOS 65 nm	CMOS 65 nm	CMOS 65 nm	CMOS 65 nm	CMOS 28 nm	CMOS 65 nm
Front end topology	TIA+LA+EQ	TIA+LA	TIA+LA+CDR	TIA+IIR-DFE	TIA+LA+CTLE +On-chip Si-PD	TIA+ID	TIA+PA
Peaking inductor	Yes	Yes	Yes	No	Yes	No	No
Wavelength	850 nm	850 nm	N.A.	850 nm	850 nm	850 nm	850 nm
PD responsivity	0.53 A/W	0.47 A/W	N.A.	0.5 A/W	0.272 A/W @ 12.3 V	0.5 A/W	0.051 A/W @ 0.41 V
Data rate (Gb/s)	25-28 Gb/s	25 Gb/s	25-26.5 Gb/s	20 Gb/s	18 Gb/s	20 Gb/s	25 Gb/s
Gain	76.8 dBΩ	72.5 dBΩ	71 dBΩ	---	102 dBΩ	---	69.4 dBΩ
Data pattern	PRBS 2^9-1	PRBS 2^7-1	PRBS 2^7-1	PRBS 2^7-1	PRBS 2^{15}-1	PRBS 2^7-1	PRBS 2^7-1
Sensitivity@ 10^{-12} current	98 $\mu A_{p\text{-}p}$	98 $\mu A_{p\text{-}p}$	106-184 $\mu A_{p\text{-}p}$	88.9 $\mu A_{p\text{-}p}$	88 $\mu A_{p\text{-}p}$	69 $\mu A_{p\text{-}p}$	54 $\mu A_{p\text{-}p}$
Sensitivity@ 10^{-12} (OMA)	-7.3 dBm	-6.8 dBm	N.A.	-7.5 dBm	-4.9 dBm	-8.6 dBm	0.2 dBm
Power efficiency	4.9 pJ/bit	2.72 pJ/bit	1.35 pJ/bit (front end)	0.75 pJ/bit	2.7 pJ/bit	0.7 pJ/bit	1.23 pJ/bit
Total area	0.32 mm^2	1.0725 mm^2 *	0.32 mm^2 **	0.027 mm^2	0.23 mm^2	0.005 mm^2	0.0056 mm^2

LA: *Limiting amplifier,* ***EQ:*** *Equalizer,* ***CDR:*** *Clock-data recovery,* ***IIR-DFE:*** Infinite impulse response-decision feedback equalizer, ***PA:*** *Post-amplifier,* ***CTLE:*** *Continues-time linear equalizers,* ***ID:*** *Integrate-and Dump (ID) circuit,*
* There are 4 receivers in that area.
** Total area of the optical receiver with CDR.

850-nm applications. Overall, the proposed optical front end occupies only 21% of the next smallest front-end fabricated in 65-nm CMOS. It also shows the lowest peak-to-peak current sensitivity of 54 μA_{p-p} at 25-Gb/s data rate while providing a reasonable energy efficiency of 1.23 pJ/bit. However, the low responsivity of 0.051 A/W at 0.4-V reverse-bias voltage of the Si-PD leads to a larger optical sensitivity in comparison with other optical front ends. Note that the responsivity of the proposed Si-PD increases by a factor of 6 to 0.3 A/W for 14-V reverse-bias voltage, which would improve the optical sensitivity to −7.45 dBm. However, the packaging arrangement in this paper prevented us from measuring the performance of the receiver with a large reverse-bias voltage. The integrated avalanche Si-PD in [23] has a responsivity of 0.273 A/W and 3-dB bandwidth of 1.1 GHz at 12.3-V reverse-bias voltage. However, the proposed Si-PD has a large bandwidth of 12.6 GHz at 0 V and can support high-speed operation without requiring any equalization techniques. Furthermore, operating at low bias voltage reduces the complexity of the bias circuits.

V. CONCLUSION

This paper presents the design and experimental results of a low-power and compact 25-Gb/s optical receiver in 65-nm TSMC technology. It was prototyped with a novel low-voltage SOI-based all-Si-PD. The receiver front end consists of an inverter-based feedback TIA and three cascaded inverter-based CH amplifiers. To this structure, variable PFB and third-order IAFB are added to increase the total bandwidth of the optical front end. The proposed optical receiver has a transimpedance gain of 69.4 dBΩ, a bandwidth of 13.6 GHz, and an input-referred noise of 3.28 μA_{rms}. It occupies only 0.0056 mm^2 and consumes 30.8 mW at 1.1-V supply voltage. The photodetector used in this demonstration has a responsivity of 0.05 A/W, a dark current of 0.02 nA, and bandwidth of 12.6 GHz at 0-V bias voltage. The optical receiver with wire-bonded Si-PD has input sensitivities of −0.5 and 0.2 dBm, for BER of 10^{-12} at data rates of 20 and 25 Gb/s, respectively, while the Si-PD has a reverse-bias voltage of 0.41 V. The energy efficiency of the optical front end is 1.23 pJ/bit at 25-Gb/s data rate. Additional electrical measurement results show that the receiver front end has input sensitivities of 3.6, 4.5, and 6.4 mV_{p-p} for BER of 10^{-12} at data rates of 20, 25, and 30 Gb/s, respectively. Furthermore, the electrical measurement with supply voltage lower than 1.1 V shows that, for input sensitivity of 5 mV_{p-p}, it has energy efficiencies from 0.425 to 0.8 pJ/bit for data rates between 10 and 25 Gb/s and supply voltages from 0.8 to 1 V.

APPENDIX A

The transimpedance of an inverter-based feedback TIA with effective transconductances of g_{mt}, feedback resistor of R_t, and input capacitance of C_{in}, is given by

$$Z_{tia}(s) = \frac{1 - g_{mt}R_t}{g_{mt} + s(C_L + C_{in}) + s^2 C_L C_{in} R_t}$$
$$A_{tia} = (g_{mt}R_t - 1)/g_{mt}. \quad (15)$$

Also, the transfer function of the PFB with effective transconductances of g_{m5} is given by

$$G_{PFB}(s) = \frac{-g_{m5}(1 + sC_{in}R_t)}{g_{mt} + s(C_L + C_{in}) + s^2 C_L C_{in} R_t}$$
$$\alpha = g_{m5}/g_{mt} \quad (16)$$

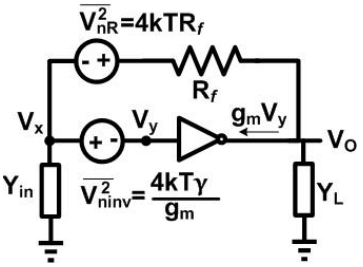

Fig. 25. Block diagram for calculating the output noise of a transimpedance stage.

dc gain of the receiver is given by

$$R_T = \frac{A_{\text{tia}} A_1^3 A_2^3}{1 + 5\beta A_1 A_2 - A_1\alpha + 3A_1^2 A_2^2 \beta^2 - 3A_1^2 A_2 \alpha\beta}. \quad (17)$$

As it is expected, the AFB reduces the dc gain and the PFB increases the dc gain.

APPENDIX B

This section presents the calculation of the low-frequency input-referred current noise of the proposed receiver (Fig. 7). First, we calculate the output noise of our proposed receiver coming from the TIA and three cascaded CH amplifiers. Then, the output noise caused by the IAFB and PFB is calculated. A CH amplifier consists of a transconductance stage (G_1) and a transimpedance stage (G_2), which has a similar structure as the input TIA stage. For a transimpedance stage, its output noise is caused by the thermal noise of the feedback resistor (V_{nR}^2) and the thermal noise of the PMOS and NMOS transistors in the inverter (V_{ninv}^2). We used the model illustrated in Fig. 25 to calculate the output noise of the transimpedance stage due to the feedback resistor and the inverter.

In Fig. 25, Y_L is the output admittance of the transimpedance stage given by $Y_L = g_{\text{ds}} + sC_L$. Y_{in} is the input admittance of the transimpedance stage. For the input TIA, $Y_{\text{in}} = sC_{\text{in}}$, where C_{in} represents the input capacitor of the TIA. For the transimpedance stage in the CH amplifier, $Y_{\text{in}} = Y_L$, if all inverters have the same load capacitance and output conductance. The relation between the output noise of the transimpedance stage and the thermal noise of the feedback resistor along with the thermal noise of the inverter is calculated by

$$V_{\text{no}} = V_{nR}\frac{g_m + Y_{in}}{g_m + Y_{\text{in}} + Y_L + Y_L Y_{\text{in}} R_f} + V_{\text{ninv}}\frac{g_m(1 + R_f Y_{\text{in}})}{g_m + Y_{\text{in}} + Y_L + Y_L Y_{\text{in}} R_f}. \quad (18)$$

Assuming that $g_m \gg g_{\text{ds}}$ and $g_m \gg g_{\text{ds}} g_{\text{ds}} R_f$, the low-frequency noise at the output of the transimpedance stage is obtained by

$$\overline{V_{\text{no}}^2} = \overline{V_{nR}^2} + \overline{V_{\text{ninv}}^2} = \overline{V_{nR}^2} + \frac{\overline{I_{\text{ninv}}^2}}{g_m^2} \quad \text{where } \overline{I_{\text{ninv}}^2} = 4\ \text{kT}\gamma\, g_m. \quad (19)$$

Note that at low frequency, the feedback resistors in the TIA and the transimpedance stage in the CH amplifier reduce both input and output resistances of the TIA to approximately $1/g_m$. Therefore, the output noise of the transconductance stage G_1 is given by

$$\overline{V_{no-G1}^2} = \frac{\overline{I_{\text{ninv1}}^2}}{g_{m2}^2}. \quad (20)$$

The total output noise due to the TIA and three cascaded CH amplifiers in the proposed design shown in Fig. 7 is obtained by

$$\overline{V_{n-\text{out(TIA+CH)}}^2} = \left(\frac{1}{1 + 5\beta A_1 A_2 - A_1\alpha + 3A_1^2 A_2^2 \beta^2 - 3A_1^2 A_2 \alpha\beta}\right)^2 \left(\left(\overline{V_{nRt}^2} + \frac{\overline{I_{\text{ninv}}^2}}{g_{\text{mt}}^2}\right) A_1^6 A_2^6 + \frac{\overline{I_{\text{ninv1}}^2}}{g_{m1}^2}\left(A_1^4 A_2^6 + A_1^2 A_2^4 + A_2^2\right) + \left(\overline{V_{nR}^2} + \frac{\overline{I_{\text{ninv2}}^2}}{g_{m2}^2}\right)\left(A_1^4 A_2^4 + A_1^2 A_2^2 + 1\right)\right). \quad (21)$$

The low-frequency input-referred current noise of the proposed receiver due to the TIA and three cascaded CH amplifiers is calculated by

$$\overline{I_{n-\text{in(TIA+CH)}}^2} = \frac{\overline{V_{n-\text{out(TIA+CH)}}^2}}{R_T^2}. \quad (22)$$

Assuming that $g_{\text{mt}} = g_{m2} = g_{m1} = g_m$, which results in $A_1 = g_{m1}/g_{m2} = 1$, the input-referred current noise caused by the TIA and CH amplifier is given by

$$\overline{I_{n-in(\text{TIA+CH})}^2} = \frac{\overline{V_{nRt}^2}}{A_{\text{tia}}^2} + \frac{\overline{V_{nR}^2}}{A_{\text{tia}}^2}\left(\frac{1}{A_2^2} + \frac{1}{A_2^4} + \frac{1}{A_2^6}\right) + \frac{\overline{I_{\text{ninv}}^2}}{A_{\text{tia}}^2 g_m^2}\left(2 + \frac{2}{A_2^2} + \frac{2}{A_2^4} + \frac{1}{A_2^6}\right). \quad (23)$$

From (23), we see that the feedback inverters (G_f, G_{PFB}) do not affect the low-frequency input-referred noise caused by the TIA and CH amplifiers. More precisely, the low-frequency noise contribution of the TIA and CH stages to the input-referred noise of the receiver with IAFB and PFB is the same as the receiver without IAFB and PFB.

If $g_{\text{mt}} R_t \gg 1$, the TIA gain $A_{\text{tia}} \approx R_t$, also if $A_2 \gg 1$ (in our design $A_2 \approx 3$) the equation can be simplified to

$$\overline{I_{n-in(\text{TIA+CH})}^2} = \frac{4\ \text{kT}}{R_t} + \frac{8\ \text{kT}\gamma}{R_t^2 g_m}. \quad (24)$$

The first term in the above question is the current noise of the TIA's feedback resistor, which directly appears in the input-referred current noise and has the dominant effect. The second dominant part is related to the thermal noise of the inverters in the TIA and the transconductance stage of the first CH amplifier.

Next, the noise contribution of several feedbacks to the input-referred current noise is calculated. The thermal noise

current injected into the outputs of the IAFB and the PFB are given by

$$\overline{I_{n-\mathrm{IAFB}}^2} = 4\ \mathrm{kT}\gamma\, g_{mf}, \quad \overline{I_{n-\mathrm{PFB}}^2} = 4\ \mathrm{kT}\gamma\, g_{m5}. \tag{25}$$

Note that at low frequency, the feedback resistors in the TIA and the TIA portions of the CH amplifiers reduce both input and output resistances of the TIA to approximately $1/g_m$. Therefore, the output noise of the of feedback inverters G_f and the G_{PFB} inverter are given by

$$\overline{V_{\mathrm{no}-Gf}^2} = \frac{\overline{I_{n-\mathrm{IAFB}}^2}}{g_{m2}^2}, \quad \overline{V_{\mathrm{no-GPFB}}^2} = \frac{\overline{I_{n-\mathrm{PFB}}^2}}{g_{\mathrm{mt}}^2}. \tag{26}$$

The low-frequency output noise of the receiver due to the IAFB and the PFB is obtained by

$$\begin{aligned}\overline{V_{n-\mathrm{out}(I\mathrm{AFB+PFB})}^2} &= \left(\frac{1}{1+5\beta A_1A_2 - A_1\alpha + 3A_1^2A_2^2\beta^2 - 3A_1^2A_2\alpha\beta}\right)^2 \\ &\left(\left(\frac{\overline{I_{n-\mathrm{PFB}}^2}}{g_{\mathrm{mt}}^2} + \frac{\overline{I_{n-\mathrm{IAFB}}^2}}{g_{\mathrm{mt}}^2}\right)A_1^6A_2^6 \right. \\ &\left. + \frac{\overline{I_{n-\mathrm{IAFB}}^2}}{g_{m2}^2}\left(A_1^4A_2^6 + A_1^4A_2^4 + A_1^2A_2^4 + A_1^2A_2^2\right)\right).\end{aligned} \tag{27}$$

The input-referred current noise PSD is calculated by dividing the output noise PSD by the square of the transimpedance gain. Assuming that $g_{\mathrm{mt}} = g_{m2} = g_{m1} = g_m$, then $A_1 = g_{m1}/g_{m2} = 1$. The input-referred current noise caused by the IAFB and PFB is calculated by

$$\begin{aligned}\overline{I_{n-\mathrm{in}(\mathrm{IAFB+PFB})}^2} = \frac{\overline{I_{n-\mathrm{PFB}}^2}}{A_{\mathrm{tia}}^2 g_m^2 A_2^6}A_2^6 + \frac{\overline{I_{n-\mathrm{IAFB}}^2}}{A_{\mathrm{tia}}^2 g_m^2 A_2^6} \\ \times\left(A_2^6 + A_2^6 + A_2^4 + A_2^4 + A_2^2\right).\end{aligned} \tag{28}$$

The three first terms in (28), which are related to PFB and the two leftmost IAFB have the largest contribution to the input-referred noise of the receiver. By substituting $\beta = g_{\mathrm{mf}}/g_m$ and $\alpha = g_{m5}/g_m$, the equation can be simplified to

$$\overline{I_{n-\mathrm{in}(\mathrm{IAFB+PFB})}^2} = \frac{4\ \mathrm{kT}\gamma}{A_{\mathrm{tia}}^2 g_m}\left(\alpha + \beta\left(2 + \frac{2}{A_2^2} + \frac{1}{A_2^4}\right)\right). \tag{29}$$

Assuming that $\gamma = 1$, the ratio of the input referred-noise due to the IAFB and PFB over the input referred-noise due to the TIA and CH amplifiers is obtained by

$$\begin{aligned}\frac{\overline{I_{n-\mathrm{in}(\mathrm{IAFB+PFB})}^2}}{\overline{I_{n-\mathrm{in}(\mathrm{TIA+CH})}^2}} \\ = \frac{\frac{1}{g_m}\left(\alpha + \beta\left(2 + \frac{2}{A_2^2} + \frac{1}{A_2^4}\right)\right)}{R_t + R_f\left(\frac{1}{A_2^2} + \frac{1}{A_2^4} + \frac{1}{A_2^6}\right) + \frac{1}{g_m}\left(2 + \frac{2}{A_2^2} + \frac{2}{A_2^4} + \frac{1}{A_2^6}\right)}.\end{aligned} \tag{30}$$

In our design $\alpha = 0.064$, $\beta = 0.16$, $g_m \approx 40$ m, $R_t = 300\ \Omega$, $R_f = 215.5\ \Omega$, and $A_2 \approx 3$, which results in a ratio of 0.0197. Assuming that $A_2 \gg 1$, the ratio is simplified to

$$\frac{\overline{I_{n-\mathrm{in}(\mathrm{IAFB+PFB})}^2}}{\overline{I_{n-\mathrm{in}(\mathrm{TIA+CH})}^2}} = \frac{\alpha + 2\beta}{g_m R_t + 2}. \tag{31}$$

Equations (30) and (31) show that the low-frequency noise density of the receiver is only slightly increased using the proposed combination of AFB.

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