A 48-V Wide-V_{in} 9–25-MHz Resonant DC–DC Converter

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***Abstract*— This paper presents a wide-V_{in} step-down parallel-resonant converter (PRC), comprising an integrated 5-bit capacitor array and a 300-nH resonant coil, placed in parallel to a conventional buck converter. Soft-switching resonant converters are beneficial for high-V_{in} multi-MHz converters to reduce dominant switching losses, enabling higher switching frequencies. The output filter inductor is optimized based on an empirical study of available inductors. The study shows that faster switching significantly reduces not only the inductor value but also volume, price, and even the inductor losses. In addition, unlike conventional resonant concepts, soft-switching control as part of the proposed PRC eliminates input voltage-dependent losses over a wide operating range, resulting in 76.3% peak efficiency. At $V_{in} = 48$ V, a loss reduction of 35% is achieved compared with the conventional buck converter. Adjusting an integrated capacitor array, and selecting the number of oscillation periods, keeps the switching frequency within a narrow range. This ensures high efficiency across a wide range of $V_{in} = 12$–48 V, 100–500-mA load, and 5-V output at up to 25-MHz switching frequency. Thanks to the low output current ripple, the output capacitor can be as small as 50 nF.**

***Index Terms*— Buck converter, inductors, multi-MHz switching, resonant dc–dc converter, soft-switching.**

I. Introduction

In TODAY'S electronics systems, several dc–dc converters are required to generate various voltage rails at the point of load. Multi-MHz dc–dc converters with frequencies in the order of 100 MHz, achieving tiny size at low cost, have been published for low input voltages in the range of 1–5 V [1], [2]. In contrast, several applications in growth areas like automotive, industrial, and IT servers require much larger input voltages in the range of 12–50 V. Converters for such high input voltages, which are switching in the multi-MHz range to achieve high integration, are rarely published. The motivation for this paper is supported by general system-level considerations for highly integrated high-V_{in} converters, outlined in Section II, including inductor sizing and design limitations of conventional resonant concepts. The resulting higher conversion ratios require larger filter inductors. A significant reduction of the inductor size is possible by increasing the switching frequency, and by properly choosing the current ripple and thus the inductor value of the converter. To optimize the main inductor of the proposed converter, the benefit of a smaller inductor size and lower inductor losses is explored in an empirical study of available inductors in Section II-A. The main challenge for multi-MHz operation at high input voltages is excessive switching losses, which scale up linearly with the switching frequency. The main part of the switching losses increases even quadratically to the input voltage, due to charging of the switching node capacitance.

Soft-switching or zero-voltage switching (ZVS) are well-known techniques to reduce switching losses [5]. It can be utilized in a resonant converter or a quasi-resonant converter (QRC) [3], [6]. In resonant converters, the frequency of a resonant circuit determines the overall switching period of the converter, while in QRCs, oscillation of a resonant circuit only occurs during the OFF-time of the converter.

Thus, high efficiency is only achieved in a very narrow operating range [5]. A wide range of load and input voltages would require to vary the converter's switching frequency over a wide range. Section II-B reveals the associated design limitations for a conventional QRC, as shown in Fig. 1(a). This includes very small switch ON-time pulses and high losses in some of the operating points.

This paper presents a soft-switching buck converter for 12–48-V input and 5-V output at switching frequencies up to 25 MHz, which overcomes these limitations. It introduces a parallel-resonant converter (PRC), as shown in Fig. 1(b). Section III describes the implementation and the different operation modes of the PRC. A dedicated soft-switching control eliminates input voltage-dependent charging and switching losses across a wide range of input voltage and load current [4]. The PRC consists of a resonant circuit attached to a regular buck converter. The resonant frequency is tunable by an on-chip capacitor array. Allowing different numbers of oscillations of the resonant circuit, a wide range of operating points can be achieved, while the resulting switching frequency can be limited to a very narrow range, compared with conventional resonant concepts. Fast switching and resonant operation ensure small current and output voltage ripple, resulting in small passives. Particularly, L_0 and C_0 can be significantly reduced. Experimental results and a comparison to the state-of-the-art converters are presented in Section IV.

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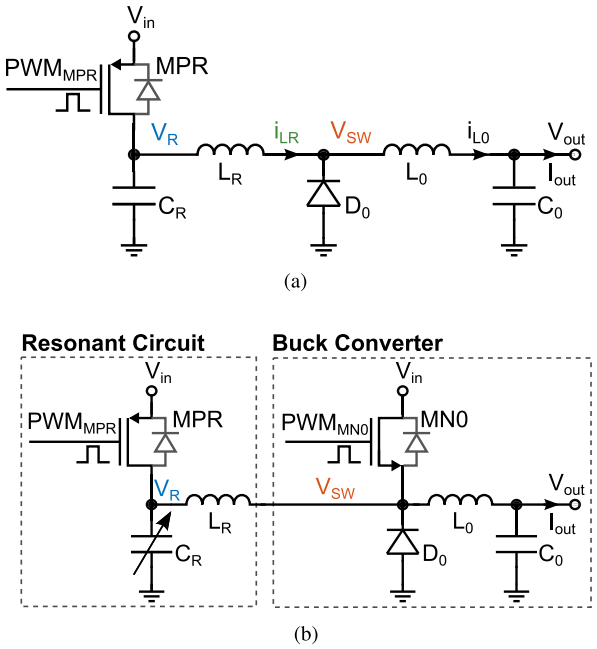

Fig. 1. (a) Conventional QRC [3]. (b) Proposed PRC [4].

II. Converter System Considerations

A. Inductor Scaling

The increase of the switching frequency is motivated by enabling smaller passive filter components. In this section, the scaling of inductor losses, including ac losses (core losses, skin effect, and proximity effect) and dc losses (wiring resistance), and the inductor volume toward higher switching frequencies is explored by comparison of inductors available on the market. For this reason, inductors from a large inductor supplier are analyzed in terms of volume (and thus power density) and losses (with loss models provided by the supplier). The converter was assumed to operate at 48-V input, 5-V output, and 0.5-A load current. First, the current ripple was chosen to be fixed at a typical value of $\Delta I_{L0} = 0.2$ A ($\Delta I_{L0}/I_{\text{out}} = 40\%$), and the inductors were designed for different switching frequencies.

The required inductor value for each switching frequency was calculated. For each of the resulting inductor values, all suitable inductors, offered by the vendor, were analyzed by comparing inductor losses, inductor volume, and price. At each frequency, the inductor with the smallest available inductor volume is selected. Fig. 2(a) shows the inductor losses, the inductor volume (marker size), and the price (color scale) of the selected inductors. It can be observed that a frequency increase allows to scale down the inductor volume, and at the same time, it exhibits significantly lower inductor losses, as the dc resistance is reduced due to the reduction of the required inductor value. Only at frequencies above 30 MHz and at high current ripple, ac losses become dominant and thus make air-core inductors the favorable choice. This is in accordance with a theoretical study of the inductor scaling in [7]. Moreover, the price of the inductors reduces toward smaller inductor volumes. At $f_{\text{sw}} = 1$ MHz, the most expensive inductor is

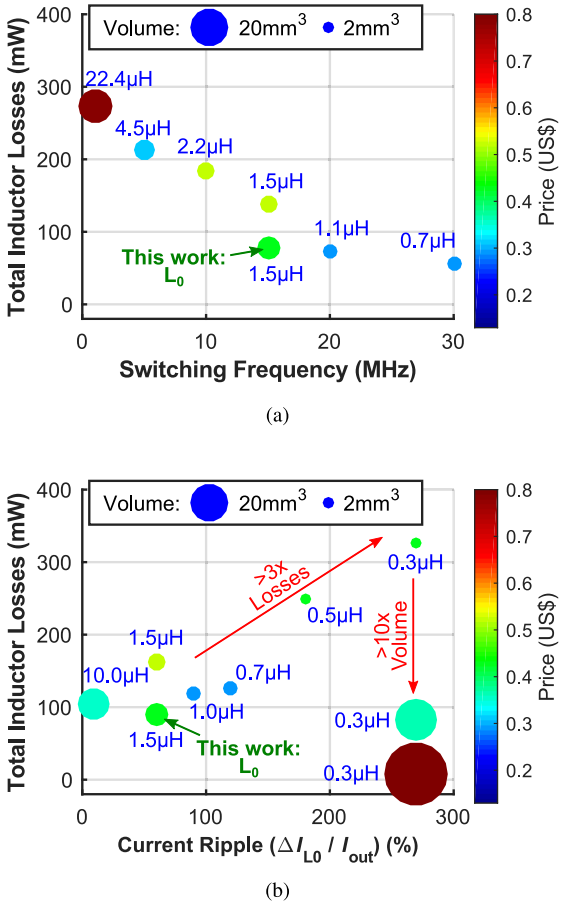

Fig. 2. Scaling of the inductor for a buck converter operated at different switching frequencies and current ripple ($V_{\text{in}} = 48$ V, $V_{\text{out}} = 5$ V, and $I_{\text{out}} = 0.5$ A). (a) Scaling of inductor losses, inductor volume, and price at different switching frequencies, with a fixed current ripple of 40%. (b) Scaling of inductor losses, inductor volume, and price at different current ripples, with a fixed switching frequency of 10 MHz.

required, with a ferrite core of $L_0 = 22.4$ μH, a volume of 17 mm^3, and a price of U.S. \$0.78. Increasing the frequency, for example up to $f_{\text{sw}} = 20$ MHz, the inductor value can be reduced to $L_0 = 1.1$ μH with a six times smaller volume of only 3 mm^3. This inductor is available at a price of only U.S. \$0.30, even using a more expensive compound core material. Other operating conditions show a similar trend. Higher switching frequencies up to the range of 20–30 MHz are thus highly beneficial for smaller inductor volumes, lower price, and less heat dissipation.

Second, a similar inductor analysis is done, while the switching frequency is kept constant at $f_{\text{sw}} = 10$ MHz and the inductors values are selected to achieve different inductor current ripples. Again, the inductors with the smallest available inductor volume are shown in Fig. 2(b) for different current ripples. The inductor losses increase by more than three times, if the current ripple is increased from below 100% toward 300% (at 0.5-A load) and the inductor volume remains equal. The inductor losses can only be decreased by significantly increasing the inductor volume, which is demonstrated in Fig. 2(b) with two additional inductors of 0.3 μH. These inductors, which operate at a current ripple

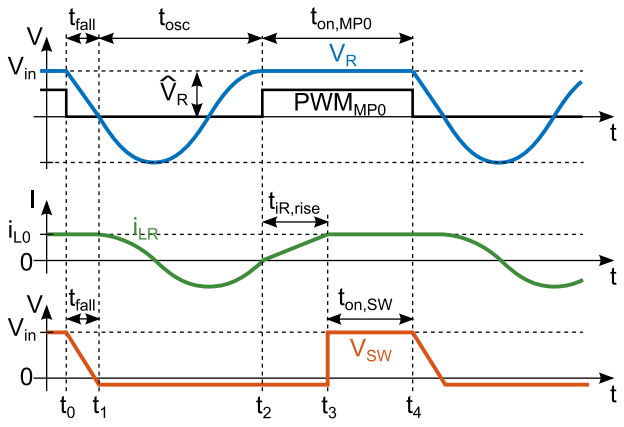

Fig. 3. Signals of the conventional QRC.

of 270%, are chosen such that they have inductor losses comparable to a 1.5-μH inductor operating at 60% current ripple. Even at a five times smaller inductor value, the inductor volume is at least three times larger.

The converter presented in this paper is suitable to operate at switching frequencies of 8–25 MHz [see Section IV]. The output filter inductor (L_0) is chosen as an inductor with a ferrite core with a value of 1.5 μH, as this results in a current ripple range of approximately 80–380 mA (15–75% at $I_{\text{out}} = 0.5$ A). The inductor used for this paper is added to Fig. 2. According to the analysis of Fig. 2(b), the current ripple allows to determine the best tradeoff between inductor losses and inductor volume. By further increasing the current ripple with a slightly smaller inductor value (e.g., $L_0 = 1$ μH), the inductor volume could be further reduced, with the drawback of higher inductor losses.

The optimization of the inductor losses allows to at least partially compensate the higher switching losses toward higher switching frequencies.

B. Frequency Variation in Resonant Converters

The lowest switching frequency across the operating range determines the size of the passive filter components, if a specific limitation of the output voltage ripple needs to be fulfilled. Operating points requiring higher switching frequencies lead to additional switching losses, without further benefit in terms of converter volume. As a consequence, it is desirable to limit the switching frequency range in resonant converters. The following analysis of a conventional QRC [3] demonstrates that boundaries of the frequency range strongly limit the operating range (V_{in}, I_{out}). A wider operating range would only be possible at slower switching by using a significantly larger resonant circuit, which limits integration.

A conventional QRC according to Fig. 1(a) is typically used in discrete power electronics [5]. An IC-level design was presented in [3]. ZVS can be achieved by adding a resonant circuit L_R and C_R to a regular buck converter. The converter is controlled only with one switch, which is beneficial for lower switching losses in multi-MHz operation.

The operating principle is demonstrated by means of the converter's main waveforms in Fig. 3. This also helps to understand the proposed PRC later on. When the switch MPR is turned on, the current i_{LR} increases through the resonant inductor L_R until it carries the output current I_{out}. The switching node V_{SW} rises as long as it is equal to the input voltage V_{in}. The diode D_0 is blocking, and the current in L_R stays constant as $V_{\text{SW}} = V_R$. When the switch MPR is turned off, V_R and V_{SW} decrease to a negative forward voltage $-V_F$ of D_0, and the diode D_0 turns on. V_R begins to oscillate around $-V_F$. Once V_R reaches V_{in}, the switch MPR can be switched ON with ZVS, i.e., zero drain–source voltage.

As shown in Fig. 3, the switching frequency f_{sw} results from the overall switching period $T = 1/f_{\text{sw}}$, which can be split into four different periods

$$T = t_{\text{fall}} + t_{\text{osc}} + t_{\text{IR,rise}} + t_{\text{on,SW}}. \tag{1}$$

When the power switch MPR is turned on at t_0, V_{SW} and V_R are both discharged approximately in the same time t_{fall} by the inductor currents i_{LR} and i_{L0} to the value of the negative forward voltage $-V_F$ of D_0. t_{fall} scales linear with V_{in} and with $1/I_{\text{out}}$ [see Fig. 3]. Thus, it significantly impacts the period and the switching frequency at varying operating points.

At time t_1, V_{SW} is held constant to $-V_F$ by the conducting diode D_0. As MPR is still OFF, V_R experiences an oscillation around a mean value of $-V_F$. The amplitude $\hat{V}_R$ of the oscillation calculates to

$$\hat{V}_R = \sqrt{L_R/C_R} \cdot I_{\text{out}}. \tag{2}$$

For $\hat{V}_R < V_{\text{in}}$, MPR can be turned on with soft-switching at the maximum of the oscillation of V_R, which occurs at 2/3 of the oscillation period. In this case, t_{osc} is independent of V_{in} and I_{out}. The quality of soft-switching is related to the voltage difference across MPR when it turns on. The voltage difference depends on the amplitude $\hat{V}_R$. For $\hat{V}_R > V_{\text{in}}$, MPR turns on (or the body diode of MPR becomes conducting), as soon as the oscillation of V_R reaches V_{in}. In this case, the turn-on event happens before 2/3 of the oscillation period (before the oscillation would reach its maximum), and thus, t_{osc} becomes dependent of V_{in} and also of I_{out}, as it changes $\hat{V}_R$ [see (2)]. At time t_2, the inductor current i_{LR} is zero. During $t_{\text{iLR,rise}}$, i_{LR} increases until it reaches the current in the inductor L_0. At t_3, it exceeds i_{L0}, and V_{SW} is pulled up. The high-phase and thus the effective ON-time $t_{\text{on,SW}}$ of the QRC ends at t_4, when MPR is turned off again. $t_{\text{on,SW}}$ depends on V_{in}, as it defines the duty cycle of the converter.

The impact of the operating points on all the converter phases results in a wide variation of both the switching frequency as well as the effective ON-time $t_{\text{on,SW}}$ of the converter. In Fig. 4, the frequency variation of the conventional QRC is plotted over a wide input voltage and load current range, while the resonant components are $L_R = 300$ nH and $C_R = 30$ pF, which are in the range to be potentially fully integrated. A variation of V_{in} from 10 to 50 V and of the load from 0.1 to 0.5 A result in a five times frequency variation.

One limitation of the QRC is that V_R swings negative during t_{osc} to $-\hat{V}_R$. The drain–source voltage of MPR thus reaches a maximum of $V_{\text{in}} + \hat{V}_R$. To achieve ZVS, requiring $\hat{V}_R > V_{\text{in}}$, the maximum ratings of MPR need to be $> 2V_{\text{in}}$. Assuming

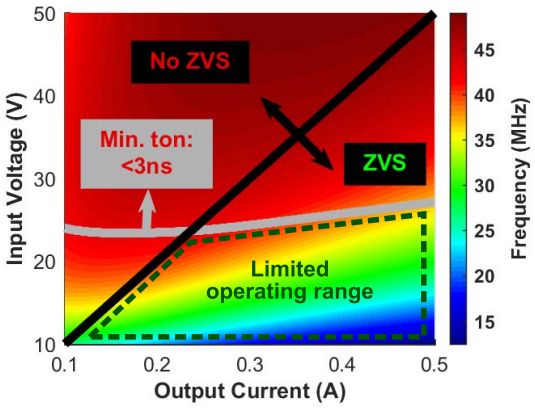

Fig. 4. Frequency variation in a frequency-controlled QRC for a wide load and input voltage range.

that a realistic design for a 50-V input will use a technology rated to 100 V, the maximum amplitude has to be limited to $\hat{V}_R = 50$ V. This corresponds to the maximum load current of $I_{out} = 0.5$ A for the design in Fig. 4. The maximum $\hat{V}_R$ value decreases toward smaller loads, and ZVS is achieved only for a combination of small input voltage and large output load. This is indicated in Fig. 4 (diagonal line).

A second limitation is related to the fact that the required duty cycle gets very small at high V_{in}. Since high V_{in} requires high switching frequencies at the same time, the resulting effective ON-time $t_{on,SW}$ is reduced to the sub-nanosecond range. The operating range in which the ON-time reduces to below 3 ns is indicated in Fig. 4. In high-voltage technologies, which are typically not optimized for speed, the generation of ON-time pulses <3 ns is usually very challenging. Together with the ZVS limitation, the QRC can only support a significantly reduced operating range, which is indicated in Fig. 4. The PRC proposed in this paper overcomes these limitations.

III. Parallel-Resonant Converter

The proposed PRC consists of a conventional buck converter with MN0, an external diode D_0, and an output filter L_0 and C_0, controlled by PWM_{MN0}. D_0 is implemented as a Schottky diode to avoid reverse recovery losses and to reduce forward conduction losses. The output voltage is controlled by the ON-time of MN0, identical to a conventional buck converter. Thus, the output voltage regulation is state of the art. Resonant operation is achieved by placing a resonant circuit L_R and C_R and a second switch MPR in parallel to a buck converter [see Fig. 1(b)]. A pMOS switch is used as the resonant node reaches negative voltage levels of $V_R = -V_{in}$, which is not supported by nMOS devices in various technologies. The resonant switch MPR controls the energy in the resonant circuit. Fig. 5 (Mode 1) shows the signals of the switching node V_{SW} of the buck converter stage and V_R of the resonant circuit. MPR is turned on at t_0. As V_{SW} is still low, the current in the inductor L_R increases until it exceeds the current through L_0 and starts to charge up V_{SW} toward t_2 with nearly no losses.

MN0 is turned on when V_{SW} reaches V_{in} with ZVS, and the turn-on losses of MN0 are significantly reduced. The maximum voltage of V_{SW}, and thus the minimum voltage $V_{DS,MN0}$ at turn on of MN0, is determined by the ON-time of MPR; thus, the ON-time of MPR controls ZVS of MN0. After MPR is turned off (t_1), V_R resonates and swings back toward V_{in} after one or multiple oscillation periods n, which allows to also turn on MPR with soft-switching at t_4. The amplitude of the resonant circuit depends on V_{in}, I_{out}, and C_R. To achieve soft-switching at MPR over a wide operating range (V_{out} and I_{out}), C_R is adjustable, implemented as an integrated 5-bit capacitor array.

Smaller C_R values lead to higher amplitudes, required for increasing V_{in}, which results in a higher resonant frequency. At the same time, higher V_{in} requires smaller duty cycles, which is limited by the resonant charging of V_{SW}. To overcome this limitation, the converter operates with different numbers of oscillation periods n of V_R, depending on the value of I_{out} and V_{in} (and thus C_R). Three different operation modes can be distinguished in the PRC, which depending on the turn-on conditions of MPR and the number of oscillation periods n of V_R. The signals of the different operation modes are shown in Fig. 5.

Mode 1: The turn on of MPR occurs after a single oscillation of V_R ($n = 1$). C_R adjusts the maximum of V_R to reach V_{in} at the turn on of MPR. V_{in} is limited to <24 V, as the ON-time of MN0 becomes small (<3 ns). ZVS brings good efficiency, despite the high frequency with considerable gate charge losses.

Mode 2: C_R is set to its maximum value to achieve a lower oscillation frequency of V_R, resulting in reduced switching losses. The turn on of MPR happens after two oscillation periods of V_R ($n = 2$). The entire first period occurs while MN0 is ON. Consequently, V_R is oscillating around V_{in}, and the positive half-wave (after $n = 1$) is clamped by the body diode of MPR. As V_{SW} is low, the resonance inductor L_R experiences a significant current increase during body diode conduction and the resulting high-phase of V_R. I_R is high enough to again pull up V_{SW}. This intermediate swing up of V_{SW} again transfers energy to the output without turning on MN0, which reduces the overall voltage ripple at the output. A conventional buck converter requires to switch up to 40% faster to achieve the same output voltage ripple at $n = 2$. V_R swings up close to V_{in}, and soft-switching of MPR is achieved.

Mode 3: The value of C_R is set low enough (higher frequency) such that V_R reaches V_{in} at $n = 1$ and $n = 2$. With higher switching frequency and lower intermediate V_{SW} pull-up, the output voltage ripple is similar to Mode 2. A frequency variation of $\pm 20\%$ changes the ripple by only $\pm 8\%$. $V_{in} = 48$ V can be handled for $n = 3$ at reduced frequency and losses.

Table I summarizes the operation modes, including the selection of n, the related V_{in} range for each of the modes, and the switching frequency range.

Fig. 6 shows the implemented soft-switching control for MPR and MN0. When the falling edge of V_R crosses zero, a zero-cross detection circuit sets ZCD_{VR} high. In each switch control block [Fig. 6 (bottom)], the positive edge of ZCD_{VR} is passed through two variable 8-bit delay chains with 250-ps resolution (LSB), which results in a maximum

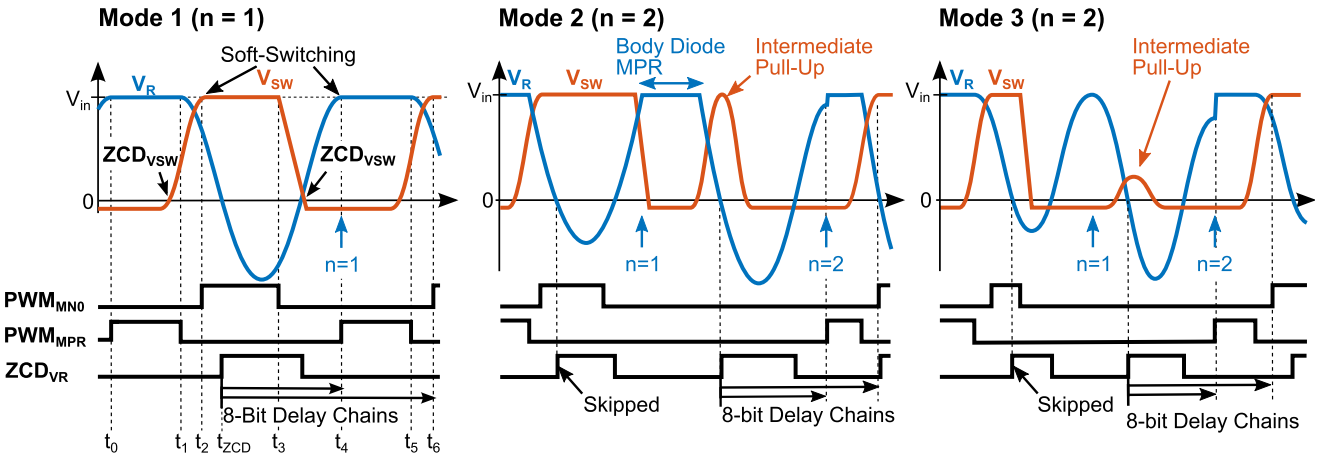

Fig. 5. Signals and switching principle of the proposed PRC in its different operation modes 1–3.

TABLE I
OPERATION MODES OF THE PRC

	Oscillation cycles n	V_{in} (typ.)	Switching frequency (typ.)
Mode 1	1	<24 V	15 - 30 MHz
Mode 2	2	<25 V	9 - 15 MHz
Mode 3	2	25 - 36 V	11 - 14 MHz
	≥3	>36 V	9 - 10 MHz

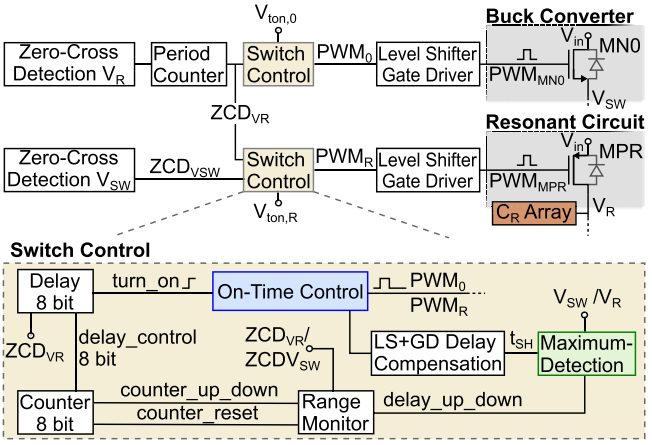

Fig. 6. Block diagram of the proposed PRC.

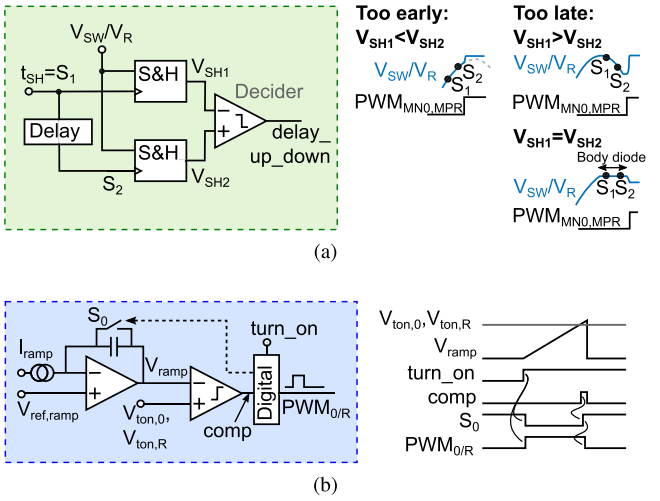

Fig. 7. Implementation of the proposed PRC. (a) Maximum detection circuit and principle. (b) ON-time control of PWM_0 and PWM_R, circuit, and signals.

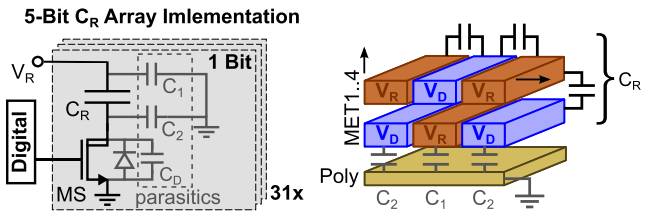

Fig. 8. Implementation of the 5-bit C_R array.

possible delay of 64 ns. The delayed signal (turn_on) initiates PWM_0 or PWM_R to be set high. The delay is adjusted cycle-by-cycle by an up-down counter, such that both MN0 and MPR turn on with minimum voltage across (soft-switching or ZVS).

To evaluate if soft-switching is achieved, V_{SW} and V_R are each sampled twice, with a delay of about 500 ps, by the maximum detection block [see Fig. 7(a)], shortly before the corresponding switches are turned on. If the first sampled voltage S_1 is smaller than the second sampled voltage S_2, MN0 or MPR has been turned on too early at the rising edge of V_{SW} or V_R before the maximum voltage is achieved. Consequently, the up-down counter, controlling the 8-bit delay, is increased for the next period. If $S_1 > S_2$, MN0 and MPR have been turned on too late, and after the maximum of V_{SW} or V_R, the counter is decreased. The counter is also decreased if $S_1 \approx S_2$. This case indicates that either the body diode is conducting (turn on too late) or the corresponding switch is turned on at the optimum soft-switching point, which is the maximum of V_R or V_{SW}. Consequently, the 8-bit delay value is toggled between the optimum turn-on point and one LSB time step after the optimum turn-on point. A logic-based range monitor observes ZCD_{VSW} and ZCD_{VR} to ensure that the turn on only occurs if V_{SW} and V_R are positive.

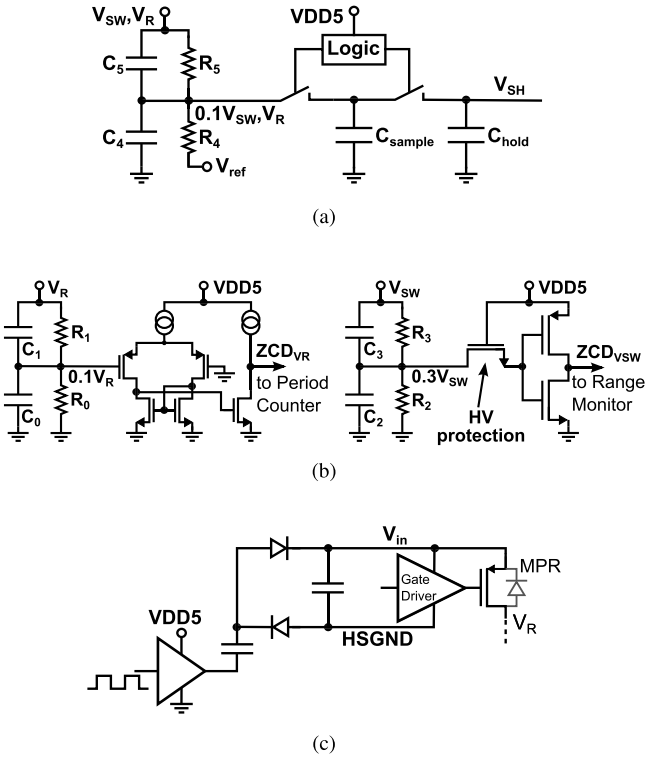

Fig. 9. Sub-circuits of the converter. (a) S&H. (b) Zero-cross detection circuits for V_R (left) and V_{SW} (right). (c) Gate driver supply with charge pump.

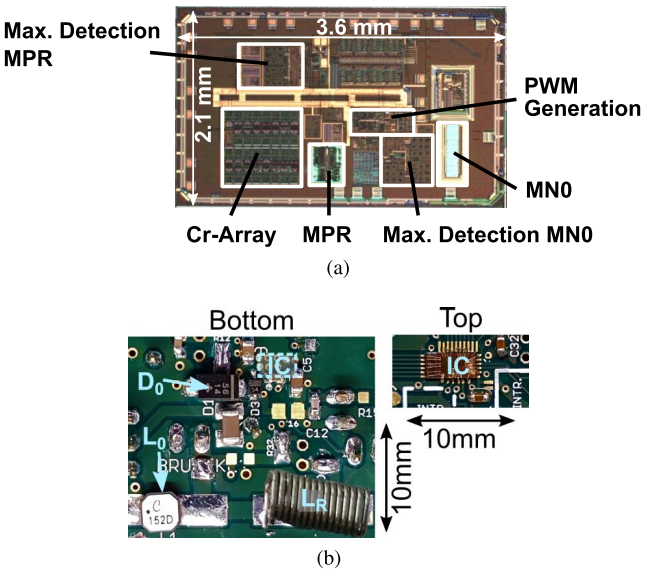

Fig. 10. Photograph of (a) test chip implemented in a 180-nm BCD technology and (b) board of the converter with the IC directly bonded to the PCB.

The ON-time control [see Fig. 7(b)] operates similar to a conventional pulsewidth modulator. The signal turn_on initiates an integrator ramp. The ON-time of MN0 or MPR is controlled by comparing the ramp to the reference voltages $V_{\text{ton},0}$ or $V_{\text{ton,R}}$. $V_{\text{ton},0}$ controls the output voltage, while $V_{\text{ton,R}}$ is adjusted such that MP0 is turned on with ZVS.

The integrated 5-bit capacitor array, which covers a range of 50–150 pF, is shown in Fig. 8. Its LSB element utilizes

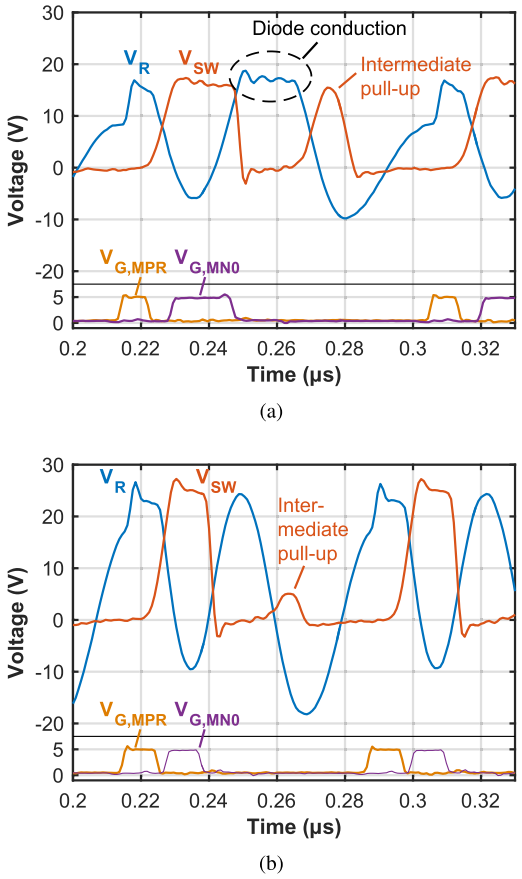

Fig. 11. Transient measurements of the proposed PRC. (a) $V_{\text{in}} = 16$ V and $I_{\text{out}} = 300$ mA in Mode 2 with $n = 2$. (b) $V_{\text{in}} = 24$ mA and $I_{\text{out}} = 300$ mA in Mode 3 with $n = 2$.

interleaved finger capacitors with a poly-Si plate against substrate coupling and associated losses. If the high-voltage switch MS is turned on, the capacitor cell is enabled and increases the total C_R value, resulting in lower switching frequency and higher amplitudes of V_R, adjusting the soft-switching condition. Parasitic capacitors determine the minimum value of C_R (if all switches MS are deselected).

The sample and hold (S&H) circuit of the maximum detection blocks is shown in Fig. 9(a). A frequency compensated voltage divider with a high time accuracy in the picosecond range is connected to V_{SW} or V_R, respectively. A two-stage sampling allows the sampled signal V_{SH} to be available at the output (C_{hold}) for the whole switching period, while the sampling capacitance C_{sample} is connected back to the divided input. Thus, V_{SH} can be evaluated with a high-accurate low-speed comparator during the entire switching cycle. Each switch of the S&H is implemented in complementary with an nMOS transistor and a pMOS transistor in parallel. This allows to compensate the gate charge coupling into the sampled signal, as the gate of the pMOS turns high, while the gate of the nMOS turns low. A positive voltage at V_{ref} shifts the divided voltage up to avoid the divided voltage from becoming negative for negative V_R or V_{SW}, which would open the switches and interfere the sample signals.

Each zero-cross detection circuit [see Fig. 9(b)] comprises an additional frequency compensated voltage divider.

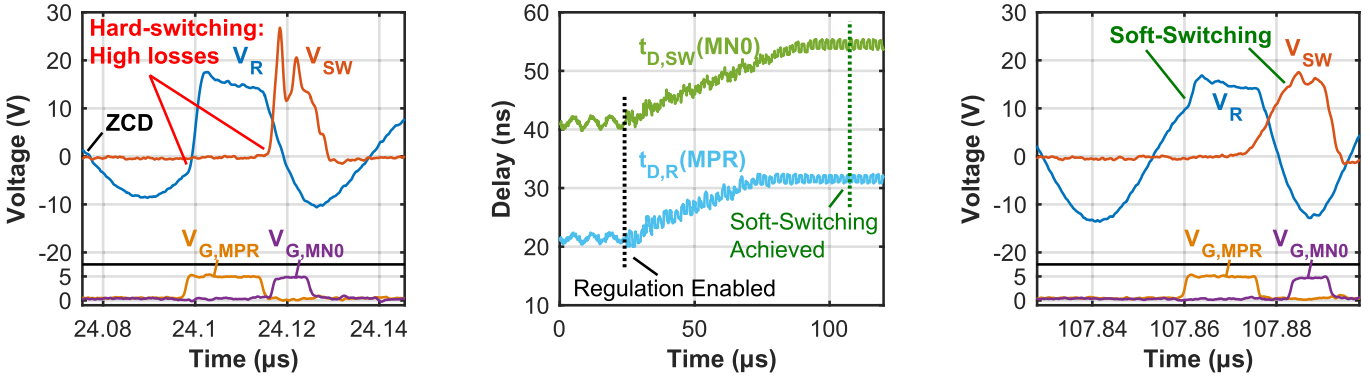

Fig. 12. Transient measurement results of the turn-on regulation and waveforms. (a) Transient measurement with soft-switching control disabled: high switching losses. (b) Settling of turn-on delay control for MPR and MN0. (c) Transient measurement with settled soft-switching control at both MPR and MN0.

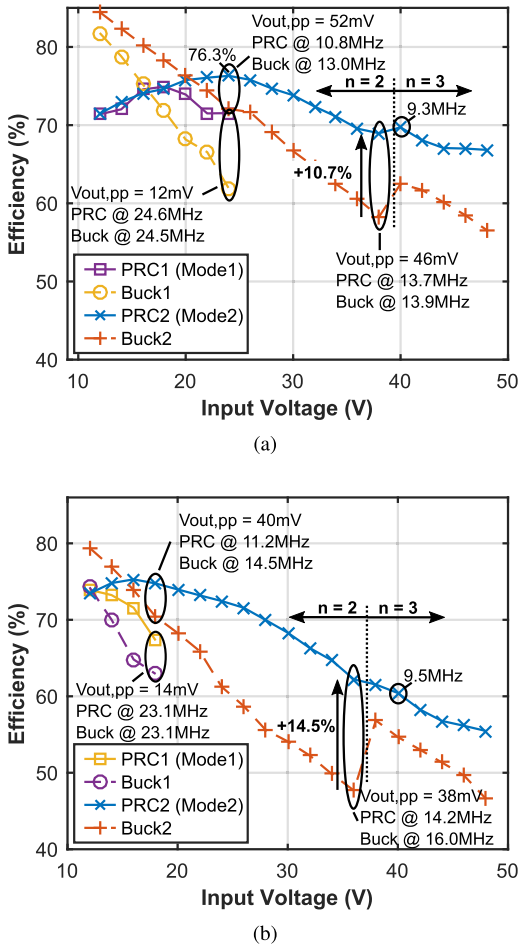

Fig. 13. Measured efficiency of the proposed PRC versus input voltage at (a) $I_{\text{out}} = 500$ mA and (b) $I_{\text{out}} = 300$ mA.

V_R requires a more accurate zero-cross detection for the period counter, while V_{SW} uses a simple inverter with clamped input for high-voltage protection, which connects to the range monitor. Fig. 9(c) shows the charge pump supply for the MPR gate driver. It uses off-chip components, but full integration would be feasible. The gate driver for MN0 is supplied with a conventional bootstrap circuit.

IV. Experimental Results and Discussion

The proposed PRC has been implemented in a 180-nm BCD technology [see Fig. 10(a)]. Fig. 10(b) shows the PCB of the converter used for the experiments.

Fig. 11(a) shows the measured transient signals at $V_{\text{in}} = 16$ V in Mode 2 ($n = 2$, see Fig. 5) with the body diode conducting at the first maximum of the oscillation of V_R and the resulting high intermediate pull-up close to V_{in} reducing the output voltage ripple. In Fig. 11(b), the converter operates at $V_{\text{in}} = 24$ V in Mode 3 ($n = 2$), without body diode conduction at a higher overall switching frequency and a reduced intermediate pull-up.

For disabled soft-switching control, Fig. 12(a) confirms inefficient hard-switching of both devices at the switching node V_{SW} and the resonant node V_R. Fig. 12(b) shows the measured settling of the turn-on delay for MN0 and MPR, respectively, after the soft-switching control is enabled. Both delays increase and reach their optimum values (soft-switching) at 87 μs ($t_{D,\text{SW}}$) and 73 μs ($t_{D,R}$). The according signals V_{SW} and V_R in soft-switching condition are shown in Fig. 12(c) for $V_{\text{in}} = 15$ V, 300 mA, and $n = 2$ oscillations.

Fig. 13 shows the measured efficiency versus V_{in}. At $I_{\text{out}} = 500$ mA [see Fig. 13(a)], the peak efficiency of the PRC is 76.3% at $V_{\text{in}} = 24$ V in Mode 2 at a switching frequency of 10.8 MHz and 71.5% in Mode 1 at switching frequency of at close to 25 MHz. Thus, Mode 1 is slightly less efficient but allows up to a 2.5 times increase of the switching frequency, resulting in a significantly smaller output filter. However, Mode 1 is limited to a maximum input voltage of 24 V at $I_{\text{out}} = 500$ mA and 18 V at $I_{\text{out}} = 300$ mA [see Fig. 13(b)]. Input voltages up to 48 V are reached for $n = 3$ cycles at $V_{\text{out}} = 5$ V in Mode 3 (in accordance to Table I). At this large conversion ratio of nearly 10:1, the converter still achieves efficiencies above 67%. For $V_{\text{in}} > 20$ V, the PRC is superior in efficiency by up to 10.7% compared with the conventional buck converter at a switching frequency that results in the same output voltage ripple. At $I_{\text{out}} = 300$ mA [see Fig. 13b)], the maximum efficiency gain is 14.5% at $V_{\text{in}} = 36$ V. The two plots in Fig. 13 reveal that the switching frequency increases toward higher V_{in} up to 40 V to about 14 MHz for $n = 2$.

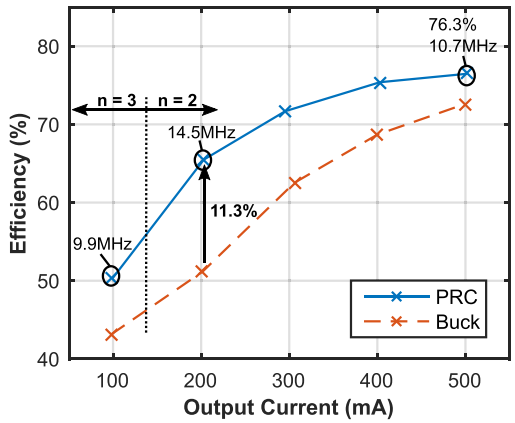

Fig. 14. Measured efficiency of the proposed PRC versus load current at $V_{\text{in}} = 24$ V.

TABLE II
LOSS COMPARISON OF A BUCK CONVERTER AND THE PRC AT $I_{\text{out}} = 0.5$ A

	$V_{in} = 24$ V	$V_{in} = 48$ V
Losses in buck converter	**969 mW**	**1918 mW**
− Loss reduction by soft-switching of MN0	−586 mW	−1540 mW
+ Losses of resonant circuit	+392 mW	+862 mW
Losses of PRC	**776 mW**	**1240 mW**
Δ Losses PRC vs. buck converter	−193 mW −20 %	−678 mW −35 %

As soon as the number of oscillation periods of V_R is increased to $n = 3$ at $V_{\text{in}} = 40$ V and above, the switching frequency is reduced to below 10 MHz, similar to switching frequencies required at low V_{in}. This way, the overall switching frequency stays in a range of 9–15 MHz, which is significantly lower than the frequency range of a conventional QRC, as indicated in Fig. 4.

Fig. 14 shows the efficiency versus output current. At $V_{\text{in}} = 24$ V, the proposed PRC shows up to 11.3% higher efficiency than a hard-switching buck converter, corresponding to a 21.3% loss reduction. The switching frequency increases toward lower currents for $n = 2$ to nearly 15 MHz. If the number of oscillation periods is changed to $n = 3$ at $I_{\text{out}} < 200$ mA, the switching frequency is again reduced to about 10 MHz, which limits the switching losses at light load.

Table II shows the improvement of the losses in the PRC compared with the buck converter. It opposes the losses, which are reduced by achieving soft-switching in the buck converter stage, and the additional losses dissipated in the required PRC resonant circuit. Soft-switching nearly eliminates transition losses and charging losses of the parasitic capacitances at the switching node V_{SW}. The added losses caused by the resonant circuit are mainly due to the resonant switch. Negative voltages at V_R require the implementation of MPR as a pMOS device in this technology, with large parasitics (gate charge, and so on) and ON-state resistance. With an nMOS switch (e.g., with SOI), calculations indicate that the PRC has the potential to achieve peak efficiencies of $> 85\%$. The loss contribution of the integrated capacitor is negligible (typically $\leq 1\%$ efficiency) due to the low-resistive implementation [see Fig. 8]. The prototype for the experimental measurements uses an air-core inductor L_R in the resonant circuit, with inductor losses at a non-significant level. A typical resonant frequency of L_R above 20 MHz brings L_R to the border, at which air-core inductors become favorable, as shown in Section II-A and [7]. Further volume reduction or even on-chip integration is expected to be possible with a custom inductor design and, in general, with the ongoing progress regarding RF inductor technology and core materials. A further loss optimization is possible by replacing the external Schottky diode by an integrated low-side switch. The resulting synchronous output stage is expected to be more efficient only with an accurate dead time control [8], which makes the overall control of the converter complex.

TABLE III
COMPARISON WITH PRIOR ART

	[9]	[8]	[3]	[10]	**This Work**
Technology	0.5 µm 120V CMOS	0.18 µm HV BCD	0.18 µm HV BCD	not reported	**0.18 µm HV BCD**
f_{sw}	2 MHz	10 MHz	8 MHz	5 MHz	**9-15 MHz**
V_{in}	12-100 V	12-18 V	20 V	8-14 V	**12-48 V**
I_{out}	0.5 A	0.5 A	0.2 A	10 A	**0.5 A**
V_{out}	10 V	1.8 V/5 V	5 V	1.2 V	**5 V**
L_0	1.5 µH	10 µH	2.2 µH	2x100 nH	**1.5 µH**
C_0	4.7 µF	10 µF	30 µF	91 nF	**50 nF**
Add. passives	C=1 µF	-	L=1.2 µH	C=1 µF	**L_R=300 nH**
Peak Eff.	90 %	81 %	72.3 %	82.5 %	**76.3 %**

Table III shows the comparison with prior art. Reference [3] comprises a quasi-resonant concept, but soft-switching is achieved only at a fixed conversion ratio. Reference [9] can handle 100 V, but it runs at higher output voltage and a much lower frequency, whereby the current ripple in the inductor increases up to 2 A. To achieve similar inductor losses, this results in a multiple times larger inductor volume compared with this paper [as demonstrated in Fig. 2(b)], even at the same inductor value ($L_0 = 1.5$ μH).

Moreover, a larger output capacitor C_0 is required ($C_0 = 4.7$ μF). Thanks to the resonant operation at high switching frequency with significantly lower current ripple, the converter in this paper allows to reduce C_0 to extremely small values ($C_0 = 50$ nF), which could be easily integrated on-chip with a suitable technology, e.g., deep trench capacitors [11].

This paper supports a wide input range of 12–48 V and 100–500-mA output current range at switching frequencies up to 15 MHz. At input voltages below 24 V, even switching frequencies up to 25 MHz with only slightly lower efficiencies are possible by changing the operation mode.

V. CONCLUSION

An increase of the switching frequency leads to a significant reduction of not only the values of the passives in the

converter but also the size, price, and even the inductor losses. In contrast, the expected efficiency in a converter scales down drastically by increasing the operating points toward high input voltages and multi-MHz switching, as well as by decreasing the output voltage or current. A PRC is introduced, which overcomes the efficiency decrease by soft-switching of the power switches, achieved by a mixed-signal soft-switching control. Implemented in a 180-nm high-voltage BCD technology, the PRC achieves soft-switching over a wide input voltage range of 12–48 V and over an output current range of 100–500 mA. This is also supported by a fully integrated adjustable 8-bit capacitor array and by turning on the resonant power switch not every oscillation period, but after multiple resonant cycles n. Also the resonant power switch operates in soft-switching mode, ensuring minimum losses. The PRC achieves peak efficiencies up to 76.3% at 10.8-MHz switching. Switching frequencies up to even 25 MHz are supported below the input voltage of 24 V. The PRC is able to reduce the required switching frequency range to 9–15 MHz. A conventional QRC would require a frequency range of about 10–50 MHz for the same range of operating points. The proposed converter enables highly compact power management solutions for various applications. It can be designed for even higher switching frequencies and input voltages, suitable for future high-efficient power electronics applications using GaN devices.

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