A Bypass-Switching SAR ADC With a Dynamic Proximity Comparator for Biomedical Applications

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***Abstract*— A bypass-switching successive approximation (BSSA) register analog-to-digital converter (ADC) employing a newly proposed dynamic proximity comparator is presented in this paper. By exploiting the current characteristics of a current correlator, the proposed comparator generates the bypass signal directly along with the polarity comparison result. The bypass window size can be adjusted to optimize the power reduction for different sensing applications with low-voltage sensitivity. A BSSA logic circuit is adopted with reduced number of logic gates as well as switching power. A prototyped chip including a proposed ADC has been designed and fabricated in a 0.18-μm CMOS process occupying an area of 0.041 mm^2. With a supply voltage of 0.6 V and at a sampling rate of 50 kS/s, the measured signal-to-noise-distortion ratio (SNDR) and spurious free dynamic range (SFDR) are 56.9 and 68.7 dB, respectively, achieving an effective number of bits (ENoB) of 9.16. The ADC consumes power of 114 nW while digitizing sinusoidal inputs. With a bypass window size of ±32 LSBs, the designed ADC consumes only 76 nW when quantizing full-scale electrocardiography signals that are generated from a certified commercial simulator, exhibiting a figure-of-merit (FoM) of 2.66 fJ/conversion-step. Besides ECG signals, the ADC is also demonstrated by digitizing electromyography and electrooculography signals from human bodies.**

***Index Terms*— Biomedical circuit, bypass switching, current correlator, dynamic comparator, electrocardiography (ECG), low power, proximity comparator, successive approximation register analog-to-digital converter (SAR ADC).**

I. Introduction

As A variety of wearable and implanted biomedical devices have emerged rapidly and have significantly improved our daily lives, the demands of low-power circuits for physiological signal acquisition have been unprecedentedly high. To facilitate long-term monitoring without frequent battery recharge or replacement, power-efficient analog sensing front-end circuits [1]–[4] for sensor and biomedical applications have recently been developed with fully differential topologies for high common-mode and supply rejection ratios. As shown in Fig. 1(a), a differential analog-to-digital converter (ADC) with high conversion efficiency is a critical and indispensable block in the developed sensing platform to digitize received physiological signals for subsequent signal processing. In targeted biomedical applications, since frequencies of interest are relatively low and the required resolution is moderate, the architecture of successive approximation register (SAR) ADC is adopted in our developed analog-front-end (AFE) because of its high power efficiency [5]–[11].

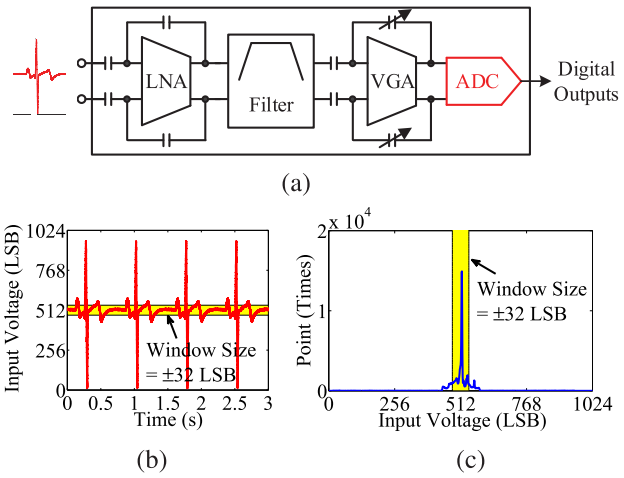

Fig. 1. (a) Developed analog sensing front-end requires a differential ADC with high power efficiency. (b) Waveform of a simulated ECG signal in a full-scale of 10-bit quantization. (c) Amplitude distribution of the sampled ECG signals shows that 72% of data points are within common-mode level ±32 LSBs.

To improve SAR ADC power efficiency and resolution, the structure of capacitors [12] as well as switching methods [7], [10], [13]–[17] and comparator architectures [18]–[20] have been widely studied. Some ADCs can be reconfigured to optimize the performance according to the sensing applications [6], [21]. Recently, the properties of biopotential signals can be exploited to further reduce the power consumption [5], [7], [9], [17]. Typically, biopotential signal waveforms, such as electrocardiography (ECG), electromyography (EMG), electrooculography (EOG), electroencephalography (EEG), and neural signals, exhibit spike-like characteristics. A physiological signal usually stays at its rest potential most of the time if not excited. Once the signal is triggered, the amplitude rises abruptly in the depolarization phase and falls rapidly in the following repolarization phase. After a short period

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of hyperpolarization phase, the physiological signal returns to the rest potential. An ECG waveform generated from a certified commercial simulator is shown in Fig. 1(b) as an example with a full-scale of 10-bit quantization levels. The corresponding distribution of signal magnitudes is plotted in Fig. 1(c). Apparently, most of the sampled ECG signals fall within the proximity of the common-mode level. If the developed SAR ADC can detect whether the sampled signal is in the proximity of the common-mode level and can skip the conversion-steps of the first few most significant bits (MSBs) accordingly, substantial amounts of switching energy can be saved in digitizing such biopotential signals.

Such bypass-switching SAR ADC is first proposed in [5], where two additional comparators and an external reference voltage are employed for bypass detection. The reference voltage that defines the bypass window size affects the circuit resolution and the amount of power saving dramatically. If the window size exceeds the designed range, the linearity degrades significantly owing to the incorrect bypass decision along with the mistakenly skipped conversion-steps. Although the reference voltage variation that results in window size smaller than the desired range only causes modest impact on power saving, the required precision for the reference voltage needs to be within one least significant bit (LSB) to achieve maximum power saving. Besides, although overall ADC power consumption is reduced substantially, bypass detection using two comparators is not straightforward, resulting in circuit complexity and extra power consumption in bypass detection logics. Almost at the same time, Guerber *et al.* [22] proposed a ternary SAR ADC using time quantizer for bypass window implementation to reduce the switching power. The bypass window size is determined by a current-starved delayed unit and varies in different stages, resulting in complicated circuits and more power consumption. Recently, a common-mode voltage ($V_{\rm cm}$)-based, switching SAR ADC with MSB bypass scheme is proposed [23]. However, the generation circuit for $V_{\rm cm}$ is not trivial and consumes additional power. This paper presents a bypass-switching SAR ADC that employs a newly proposed dynamic proximity comparator that can generate the bypass signal directly along with the regular polarity outputs in the same conversion-step. Besides the benefits of power and silicon area reduction, thanks to the current mode operation, the sensitivity of the bypass window size to reference voltages can also be greatly relaxed.

This paper is organized as follows. In Section II, the circuit implementation and design principles of the proposed dynamic proximity comparator along with detailed analysis on sensitivity, speed, and bypass window size are presented. Section II also sheds light on the logics for BSSA and for code recovery. The comparison of power saving with respect to the bypass-switching architecture using three comparators is illustrated in Section III. Besides, the power saving in ECG recording applications with different bypass window sizes is also analyzed in Section III. The test bench and biological measurement results from a prototyped chip are shown in Section IV along with the calibration procedure for bypass window size. Finally, the conclusion is drawn in Section V.

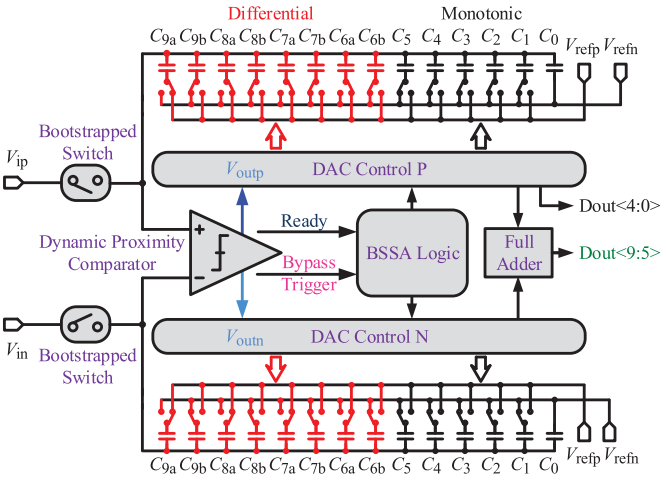


Fig. 2. Block diagram of the proposed bypass-switching SAR ADC that employs a dynamic proximity comparator and corresponding BSSA logic.

II. Circuit Implementation and Design Principles

As shown in Fig. 2, the proposed SAR ADC is composed of a pair of bootstrapped track-and-hold (T/H) switches, one dynamic proximity comparator, one BSSA logic block, and two sets of feedback DAC capacitor arrays with corresponding control and driving circuits. The first four capacitors, from C_9 to C_6, for the first four MSBs are split into half equally and are connected to $V_{\rm refp}$ and $V_{\rm refn}$, respectively, as shown in Fig. 2, rendering $V_{\rm ref}/4$ coupling with less capacitor areas and switching power consumption [25]. To avoid ADC linearity degradation due to the comparator dynamic offset, these capacitors are switched differentially in their conversion-steps to keep the input common-mode voltage at the same level. The rest of the capacitors, from C_5 to C_0, can be switched monotonically because the common-mode voltage only drops by 31 LSBs and the non-linearity induced by such small common-mode variation is negligible. The unit capacitor in the employed capacitor arrays adopts the 3-D-layer structure illustrated in [26] with a capacitance value of 1 fF.

A. Dynamic Proximity Comparator

The proposed dynamic proximity comparator employed in the presented bypass-switching SAR ADC adopts a current correlator [24] in the conventional dynamic two-stage comparator architecture so that it generates not only regular polarity outputs but also bypass trigger signals directly in the same conversion-step. The schematic of a conventional dynamic two-stage comparator [13] is shown in Fig. 3(a). The first stage senses the input signals and charges up the nodes of v_p and v_n accordingly. The following latch circuit as the second stage generates rail-to-rail digital outputs. A current correlator, as shown in Fig. 3(b), is composed of a pseudo differential pair and a bump cell, of which simulated transfer characteristics are shown in Fig. 3(c). The distinction between the current from the pseudo differential pair, $I_{\rm diff}$, and the current from the bump cell, $I_{\rm bump}$, varies with the absolute value of the input differential voltage. By exploiting such transfer characteristics, the information of proximity can be

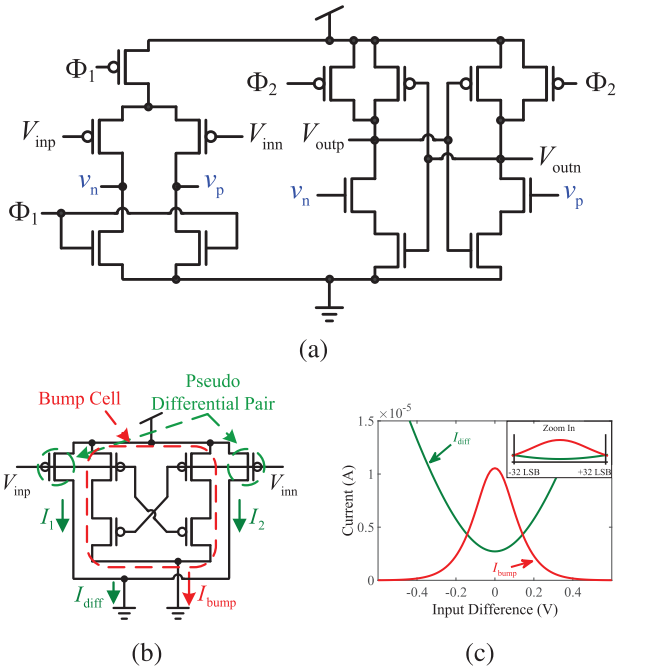


Fig. 3. (a) Schematic of a conventional two-stage dynamic comparator [13]. (b) Schematic of a current correlator [24] that consists of a pseudo differential pair and a bump cell. (c) Transfer characteristics of currents from the pseudo differential pair and from the bump cell in a current correlator for proximity detection.

transformed into currents that can be utilized to tell whether the input signals are within the designed bypass window.

The complete comparator schematic is shown in Fig. 4 with a table of all transistor dimensions. In the reset phase, M_{29} is off and the first stage output levels of v_p, v_n, v_{diff}, and v_{bump} are forced low through M_{7-10}. The output levels of the second stages, including, V_{BTn}, V_{BTp}, V_{outn}, and V_{outp}, are forced high through M_{11}, M_{14}, M_{21}, and M_{24}, respectively. There is no static power consumption in the reset phase. When clock signals, Φ_1 and Φ_2, toggle, the first stage outputs are charged up toward V_{DD} at different speeds and the latches with positive feedback at the second stages separate their corresponding output signals into opposite digital levels.

As shown in Fig. 4, the inputs of the polarity comparison latch, v_n and v_p, come from the internal nodes of the current correlator, namely, the drain nodes of the transistors M_3 and M_4. In the beginning of the charging phase, since M_5 and M_6 are in the cutoff state, M_3 and M_4 operate as a pseudo differential pair and generate polarity comparison results. The proximity detection latch receives signals from current correlator output nodes of v_{bump} and v_{diff}, which depend on the magnitudes of charging currents, I_{bump} and I_{diff}, as well as the capacitance values of corresponding MOS capacitors, M_{17} and M_{18}. When the sampled input voltage amplitude is small, v_{bump} will be charged up in a speed faster than v_{diff}. Consequently, the bypass latch output voltage V_{BTp} remains high and the output voltage V_{BTn} goes low, indicating a triggered bypass signal. The size of the bypass window can be adjusted easily through the reference voltages at the MOS capacitors, $V_{\text{ref,bump}}$ and $V_{\text{ref,diff}}$.

The timing diagrams of signals from the dynamic proximity comparator are shown in Fig. 5. In phase 1, nodes of v_p and v_n are charged from the reset level, 0 V, toward V_{DD} individually with speeds depending on sampled input signals. At the starting edge of phase 2, the polarity comparison latch is activated by the accumulated voltages at these charging nodes, which are above the threshold voltage of nMOS transistors M_{25} and M_{26}. Therefore, the positive feedback of the latch would stretch the output voltages V_{outp} and V_{outn} to be opposite digital levels by the end of phase 2. Nearly concurrently at the starting edge of phase 2, transistors M_5 and M_6 enter the saturation region, and the bump cell starts to operate. Therefore, the node of v_{bump} is charged up subsequently. In the example shown in Fig. 5, the bump current is large enough for v_{bump} to overtake the other charging node of v_{diff} before reaching the threshold point of the latch. Consequently, the output voltage of V_{BTp} goes high in phase 3 and the ADC enters the bypass mode. After locking the output results by the D-flip-flops (DFFs) in the following logic circuits, the comparator will be reset during phase 4.

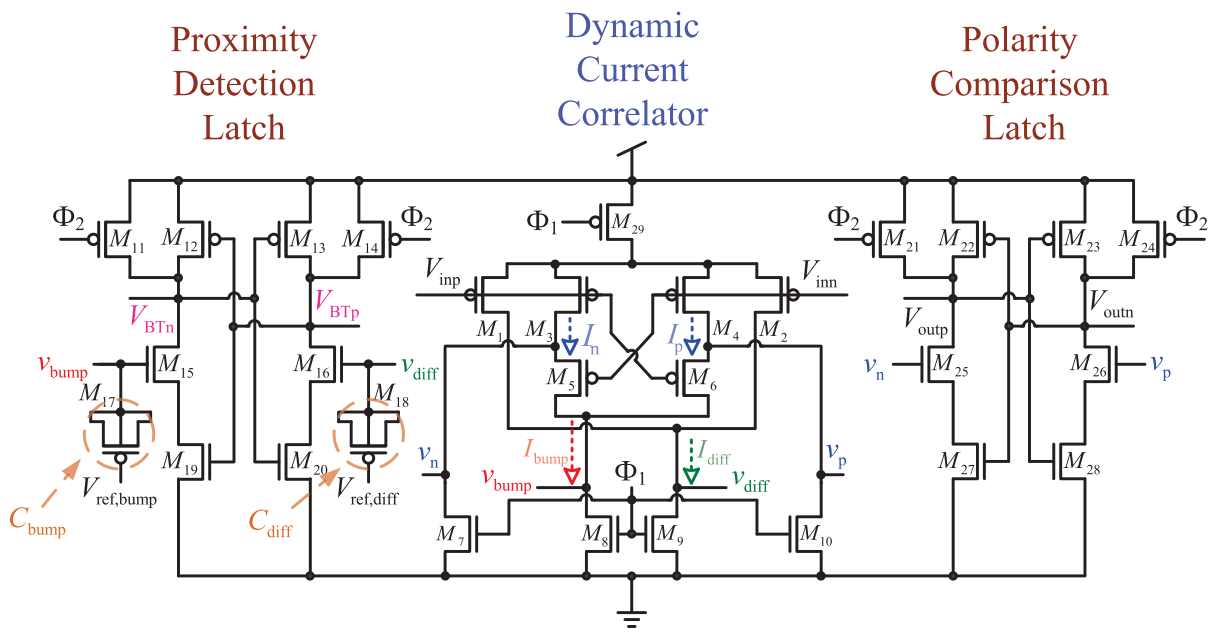
B. Bypass Window Size Tuning Range and Sensitivity

In the proposed dynamic proximity comparator, the bypass window size depends on the charging speeds at the nodes of v_{bump} and v_{diff}. Two pMOS transistors, M_{17} and M_{18}, are adopted as MOS capacitors, C_{bump} and C_{diff}, to adjust the charging speed of these nodes and to compensate for the effects of component mismatch, process variation, and parasitics along the charging paths. By modifying the reference voltages of $V_{\text{ref,bump}}$ and $V_{\text{ref,diff}}$, the capacitance values can be tuned accordingly, leading to adjustable bypass window size with low sensitivity to the reference voltages. Moreover, the transistors in the pseudo differential pair and in the bump cell should be sized large enough with careful layout to avoid noticeable horizontal offset.

To characterize the bypass window tuning range and sensitivity, rise times of v_{bump} and v_{diff} versus input difference are simulated under different biasing conditions of $V_{\text{ref,bump}}$ and $V_{\text{ref,diff}}$ with the results plotted in Fig. 6. The intersection points represent attainable bypass window sizes with corresponding biasing voltages. The minimum bypass window size is realized under the condition of $V_{\text{ref,bump}} = V_{\text{DD}}$ and $V_{\text{ref,diff}} = 0$, resulting in the maximum C_{bump} and the minimum C_{diff}. Through decreasing $V_{\text{ref,bump}}$ and increasing $V_{\text{ref,diff}}$, the window size can be adjusted in continuum toward the maximum value. Within the available voltage range, which is limited by the supply voltage of 0.6 V, the tuning range of the bypass window size in the designed ADC is 17 LSBs as shown in Fig. 6. The average sensitivity of the bypass window size to the bias voltages is less than 14.17 LSB/V, which has been reduced by 120 times when compared with the voltage sensitivity in [5].

C. Analysis on Bypass Window Size

To provide guidelines in designing the proposed dynamic proximity comparator, it is critical to analyze the bypass window size. As shown in Fig. 3(c), although both I_{diff} and I_{bump}



Unit	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	M_9	M_{10}	M_{11}	M_{12}	M_{13}	M_{14}
$\mu m/\mu m$	1/0.25	1/0.25	8/0.25	8/0.25	8/0.25	8/0.25	0.25/0.18	0.25/0.18	0.25/0.18	0.25/0.18	1/0.18	1/0.18	1/0.18	1/0.18

M_{15}	M_{16}	M_{17}	M_{18}	M_{19}	M_{20}	M_{21}	M_{22}	M_{23}	M_{24}	M_{25}	M_{26}	M_{27}	M_{28}	M_{29}
2/0.18	2/0.18	1/1	1/1	1/0.18	1/0.18	1/0.18	1/0.18	1/0.18	1/0.18	2/0.18	2/0.18	1/0.18	1/0.18	2/0.5

Fig. 4. Schematic of the proposed dynamic proximity comparator, which is composed of a dynamic current correlator as the first stage and two latches as the second stage.

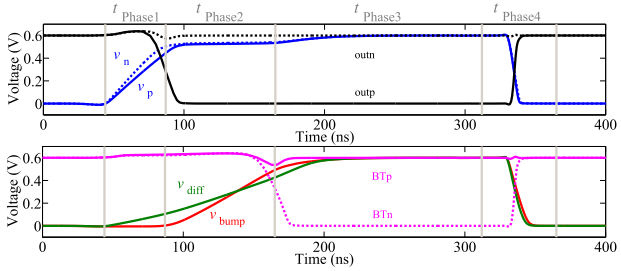


Fig. 5. Timing diagrams of signals from the proposed dynamic proximity comparator.

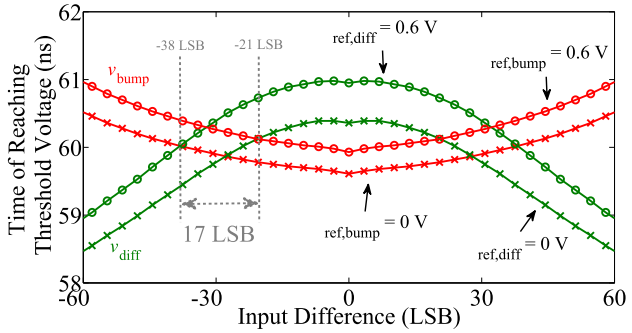


Fig. 6. Simulated periods of time for the nodes of v_p and v_n in the comparator reaching the latch threshold voltage in various reference voltage settings.

vary with input differential voltage ΔV, I_{diff} is relatively constant when the input differential voltage is within the bypass window. Therefore, small-signal approximation can be applied to simplify the analysis of the bypass window size, which is less than ±19 mV. The bypass window size analysis, starting from the timing constraints of the comparator and following the speed analysis, are detailed in Appendix A. The final expression of the bypass window size can be derived as

$$V_{\text{BW}} = \frac{I_{\text{cm}}}{g_m} \cdot \sqrt{1 - \frac{2}{S} \cdot \frac{C_{\text{bump}}}{C_{\text{diff}}}} \tag{1}$$

where g_m is transistor transconductance in the pseudo differential pair, I_{cm} is the common-mode current component, and S is the ratio of the aspect ratio of transistors in the bump cell to that in the pseudo differential pair.

From (1), the bypass window size can be designed through parameters of S and C_{bump} to C_{diff} ratio. The simulated values are compared with the theoretical curve predicted by (1) in Fig. 7. The discrepancy between the theoretical curve and S-sweeping simulation results is due to the non-negligible t_{phase1} in Fig. 5 when S is too small. In this paper, the size of transistors in the bump cell is designed to be eight times larger than that in the pseudo differential pair so that the charging current is large enough with a negligible period of t_{phase1}. With $S = 8$, the simulation results of $C_{\text{diff}}/C_{\text{bump}}$ sweeping fit the theoretical curve very well because the values of C_{diff} and C_{bump} are independent of the charging speed at v_p and v_n as well as t_{phase1}.

D. Bypass-Switching Successive Approximation

An example of the conversion process of the proposed 10-bit bypass-switching SAR ADC is illustrated in Fig. 8, where a bypass window is defined around the input common-mode level, V_{cm}, with the size of ±32 LSBs. During the

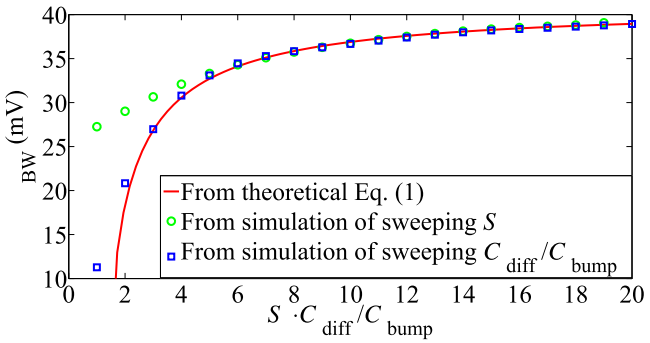


Fig. 7. Bypass window size comparisons between results from simulation and from the theoretical equation.

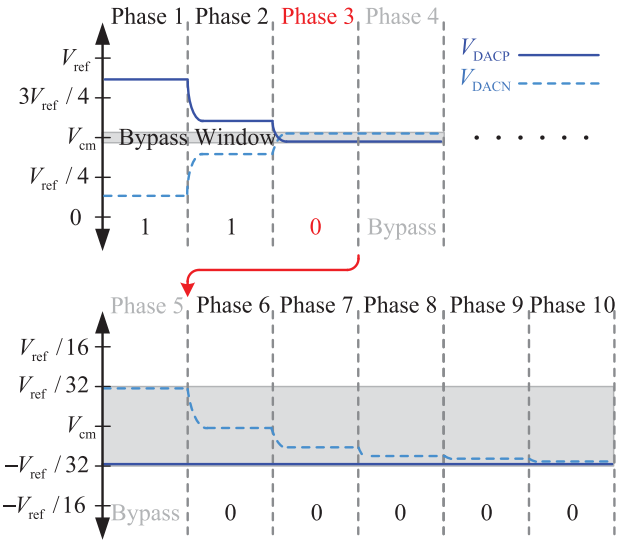


Fig. 8. Example of the switching procedure of the proposed bypass-switching SAR ADC. Since the input amplitude falls within the bypass window and triggers the bypass mechanism in phase 3, the conversion jumps to phase 6 directly and skips the switching phases 4 and 5.

first four conversion phases, as long as the comparator input voltages fall inside the bypass window, the conversion process jumps to phase 6 directly and skips the phases in between. As a result, the switching energies of DAC capacitors and the comparator for corresponding bit conversions in the skipped phases can be saved. Maximum power reduction is achieved when the sampled input signal magnitude is within the bypass window. The input voltage level demonstrated in Fig. 8 triggers the bypass signal at phase 3, where the comparator input voltages shift into the bypass window, and the switching power for the fourth and fifth MSBs is saved. Because the proximity detection in our implementation requires a constant input common-mode voltage, the conventional differential switching method is utilized for the first four MSB conversion-steps. The remaining bits are converted using the monotonic switching technique to realize cost savings with respect to logic gates and DAC switching power [14].

The proposed logic circuits for BSSA logic as well as for feedback DAC controls are shown in Fig. 9. To ensure the BSSA logic receiving valid comparator outputs of $V_{\mathrm{BT(p,n)}}$ and $V_{\mathrm{out(p,n)}}$, the dynamic proximity comparator is followed by a "Ready Control" block, within which an once-triggered DFF is employed to lock the bypass trigger signal while making bypass decisions [5]. Once the DFF is asserted, the result will be kept until next code conversion.

The BSSA logic adopts an asynchronous structure implemented by serially connected DFFs with a few simple logic gates for the bypass function, which is realized in the first four MSB stages (from P_9 to P_6), as shown in Fig. 9. The conversion would jump to phase 6 once the bypass signal, BT, is triggered to the high logic level. The output of the fifth stage, P_5, will then be triggered for the following monotonic DAC switching. At the same time, the comparator outputs $V_{\mathrm{out(p,n)}}$ in the bypass-triggered phase will be captured and locked at the digital output of B_5 for code recovery operation.

Following the BSSA logic circuit, the DAC control block generates control signals to switch the DAC capacitors, rendering the successive approximation voltages at the comparator input nodes. Two sets of output signals, from $C_{9\mathrm{a}}$ to $C_{6\mathrm{a}}$ and from $C_{9\mathrm{b}}$ to $C_{6\mathrm{b}}$, switch the first four MSB feedback capacitors differentially. Only one set of output signals, from C_5 to C_0, switch the rest of feedback capacitors monotonically. The digital outputs of $B_{\mathrm{p9-6}}$ and $B_{\mathrm{n9-6}}$ are generated from DFFs with the input data coming from the comparator outputs directly. The DFFs are triggered by corresponding BSSA logic signals of P_{9-6} and are reset by the sampling clock so that these output signals remain at zero if the corresponding phases are bypassed. These signals will be summed up through a four-bit full adder for code recovery.

When the bypass signal is triggered, at least one of the first four MSB conversion-steps is skipped. To obtain the correct binary code, four full adders are utilized to recover the final output bits of the first five MSBs, from D_9 to D_5, as shown in Fig. 10. Considering the previous example in Fig. 8 with the input magnitude of code 864, the MSB (B_9) and MSB-1 (B_8) outputs are generated from the comparator directly. The corresponding digital outputs in the bypassed phases, B_7 and B_6, are kept at the reset level, which is 0 V. The output of MSB-4 (B_5) is the polarity comparison result obtained in the phase 3. By summing these digital outputs directly, the rectified output code of 1101100000 is recovered as expected.

It is worth noting that the logic gates of NANDs, ANDs, and NOR along the bypass signal paths merely toggle when the bypass signal, BT, is low. Once the BT signal is triggered to high, logic circuits in the first four stages before P_5 are deactivated from toggling. The DAC control outputs between the bypass phase and P_5 will be kept low without any power dissipation. Compared with the SA logic implemented in [5], more switching power in logic circuits can be saved because of the direct generation of the bypass signal. Besides, the maximum number of bypassed phases in this implementation can be as many as four, which is one phase more than the implementation in [5].

III. Power Saving Comparison and Analysis

A. Power Saving Comparison

To fairly compare the power saving of the proposed bypass-switching ADC circuit, denoted as $\mathrm{ADC_{DPComp,BSSA}}$,

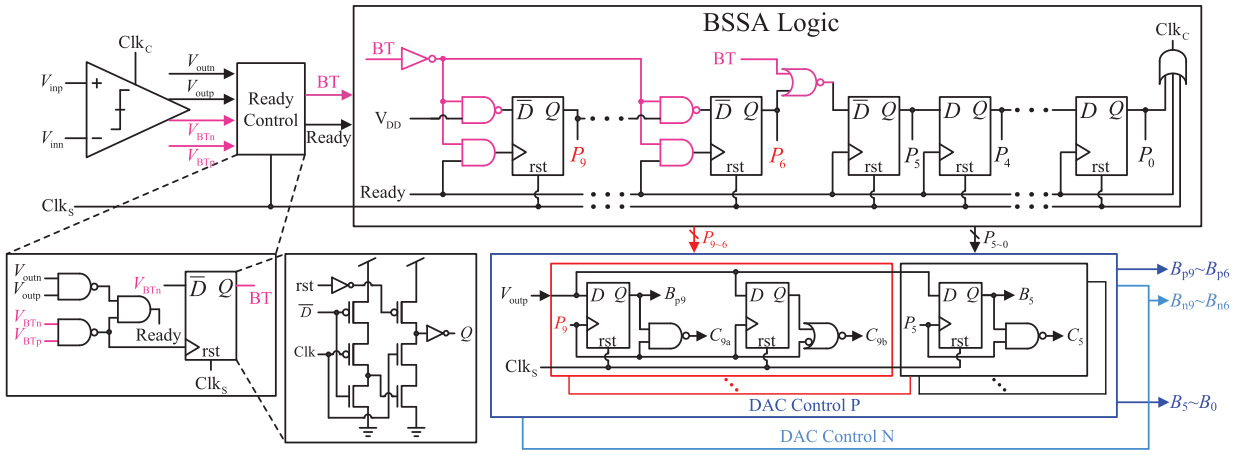


Fig. 9. Digital circuits for "Ready Control" block, for BSSA, and for DAC control.

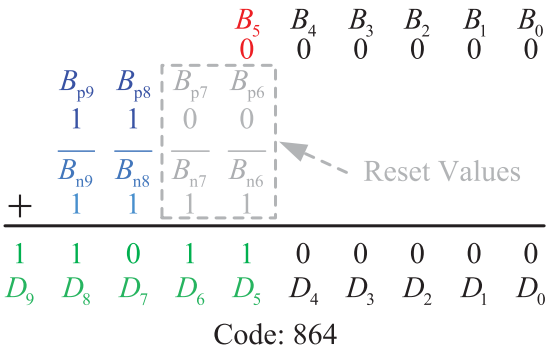


Fig. 10. Example of the code recovery operation with an input magnitude of code 864. The ADC enters the bypass mode in phase 3, leaving B_7 and B_6, at reset values. The correct code can be recovered by using four full adders.

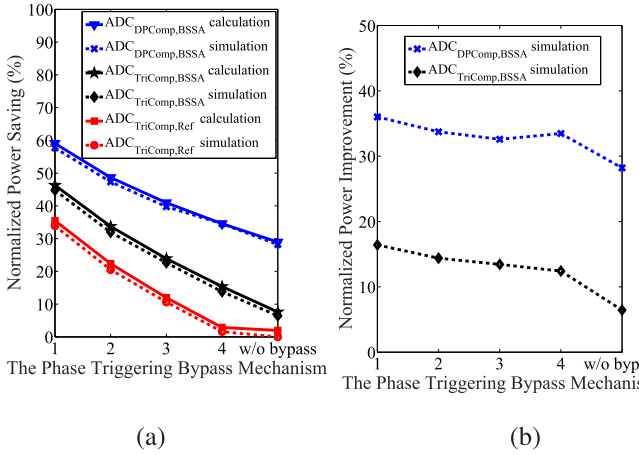


Fig. 11. (a) Comparison of normalized power saving among different designs. The power is normalized with respect to the simulated power consumption of $ADC_{TriComp,Ref}$ when it does not trigger bypass mechanism. (b) Power saving improvements with respect to $ADC_{TriComp,Ref}$ with different bypass-entering phases.

with that of the architecture proposed in [5], schematics of two other bypass-switching SAR ADC circuits, denoted as $ADC_{TriComp,Ref}$ and $ADC_{TriComp,BSSA}$, are built and simulated. Both of these two ADC circuits employ three conventional two-stage dynamic comparators, as shown in Fig. 3(a), along with the same unit capacitor of 1 fF as in $ADC_{DPComp,BSSA}$. The first ADC, $ADC_{TriComp,Ref}$, follows the SA logic implementation in [5] and is used as the baseline reference. The second ADC, $ADC_{TriComp,BSSA}$, employs the BSSA logic as presented in Section II and is used to evaluate the power efficiency improvements caused by the proposed dynamic proximity comparator and the BSSA logic, respectively. The normalized power saving percentages from these three bypass-switching ADCs with the same bypass window size of ±32 LSBs and with different bypass-entering phases are calculated, simulated, and plotted in Fig. 11(a). The calculation of the power saving from each ADC is based on the simulated power consumption when the bypass mechanism is not triggered along with the numbers of toggles from the logic gates and comparators in different bypass-entering phases. The equations for power estimation for the proposed ADC, $ADC_{DPComp,BSSA}$, are presented in Appendix B. Similar methodology is also applied to estimating the power for $ADC_{TriComp,Ref}$ and $ADC_{TriComp,BSSA}$. The calculated values match the simulation results pretty well. As in Fig. 11(b), the proposed BSSA logic provides the power saving improvements by more than 10% and the proposed dynamic proximity comparator further improves the power saving by another 20%. By combining the proposed dynamic proximity comparator with the BSSA logic, the power can be further reduced by more than 30% in each bypass-entering phases when compared with the architecture proposed in [5].

B. Power Saving in Digitizing ECG Signals

In an ECG recording application, the signal amplitudes are small in most of a single period of heartbeats, where only R- and S-peaks exhibit high amplitude. The artificial ECG signals shown in Fig. 12 are generated from a certified commercial ECG simulator with a high probability of 72% that the signal amplitudes are within the bypass window and trigger the bypass signal in the first conversion phase. Besides, the probabilities that the bypass mechanism will be activated in the second, third, and fourth phases are 1%, 2%, or 25%, respectively. The distribution of ±32-LSB segments that activate the bypass mechanism in different switching phases is

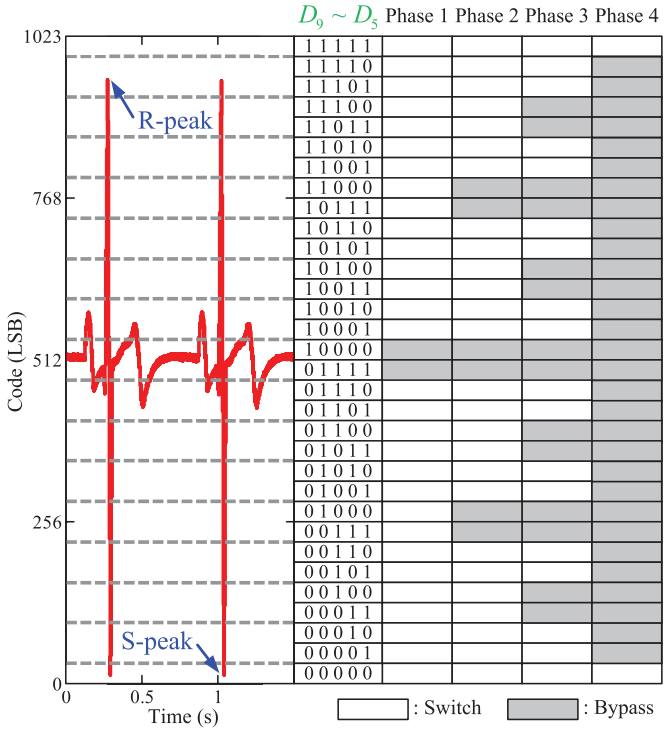


Fig. 12. Distribution of the predicted bypass-triggered phases while digitizing certified artificial ECG signals with the bypass window size of ±32 LSBs.

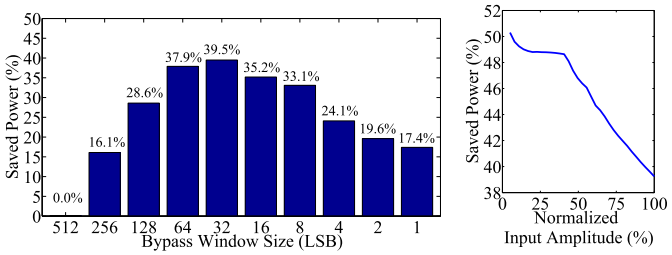


Fig. 13. (a) Simulated percentages of saved power by using the proposed bypass-switching SAR ADC with different bypass window sizes in the ECG recoding application. (b) Amounts of saved power versus normalized input amplitudes with the bypass window size of ±32 LSBs. The power reduction is more conspicuous at smaller input amplitudes.

displayed in Fig. 12. Only the segments at the top and at the bottom do not trigger the bypass signal with very low probabilities.

The total power reduction can be estimated from the product of the probability and the power saving in each phase [5]. Given the simulated ECG signals shown in Fig. 12 with the beat rate of 80 beats per minute (b/m), the amounts of power reduction with different bypass window sizes can be simulated and are plotted in Fig. 13(a). The ADC with a bypass window size of ±32 LSBs achieves the most power saving. Compared with $\text{ADC}_{\text{TriComp,Ref}}$ that adopts the architecture proposed in [5], the proposed ADC can further save more than 35% of power in digitizing the ECG signals shown in Fig. 12.

In reality, to prevent noise or motion artifact from saturating the circuit, it is unlikely that the peak-to-peak amplitude of received physiological signals occupies the full input range

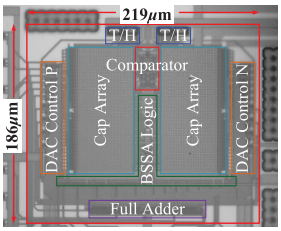


Fig. 14. Micrograph of a prototyped chip containing a proposed bypass-switching SAR ADC occupying an area of 0.041 mm^2.

of the ADC. The amount of power saving increases with the attenuation of the input amplitude. As shown in Fig. 13(b), with a bypass window size of ±32 LSBs, 39.5% of power can be saved in the worst case. If the input amplitude is attenuated to 6.3% of the full-scale so that the signal in the whole period is within the bypass window, the maximum power saving of 50.6% can be achieved. Besides, the amount of power saving also increases with the decrease of the heart beat rate.

IV. Measurement Results

A prototype chip including a proposed bypass-switching SAR ADC has been designed and fabricated in a 0.18- μm CMOS process with one-poly-six-metal (1P6M) layers. The micrograph of the circuit is shown in Fig. 14 with an occupied area of 0.041 mm^2. The designed ADC is supplied by a 0.6 − V voltage source with a maximum input swing range of 70.4% of the supply rails. With $V_{\text{ref,diff}}$ connected to the ground, an external voltage source is applied to $V_{\text{ref,bump}}$ to adjust the bypass window size. To maximize the power saving for ECG recording applications, the bypass window size is tuned to ±32 LSBs. The measured tolerance voltage of $V_{\text{ref,bump}}$ for the same window size is ±24 mV.

A. Bypass Window Size Calibration

The bypass window sizes with the same bias voltage from eight different chips are measured with the histogram plotted in Fig. 15(a). To calibrate the bypass window size, a concept proving test bench, which includes an FPGA, a discrete DAC chip, and a computer running the calibration procedure in a script language, is set up to emulate an IC test equipment that can provide precise reference voltages with fast switching for one-time calibration. The input voltages of the ADC are set at $V_{\text{cm}} \pm 33$ LSBs and an external 4-bit digital-to-analog converter (DAC) is applied to $V_{\text{ref,bump}}$. By monitoring the number of conversion-steps through the "Ready" signal in Fig. 9, the calibration DAC can be set through a binary search algorithm starting from 1000. If the observed number of pulses from the "Ready" signal is six, according to Fig. 12, the realized bypass window is too large. To reduce the bypass window size, based on Fig. 6, the DAC code should be increased further. Therefore, the MSB of the calibration DAC remains at 1. Otherwise, the observed number of pulses is nine and the corresponding bit should be toggled back to 0. The calibration proceeds with the next bit toggled to 1. It can be estimated that by using an IC test equipment, the whole

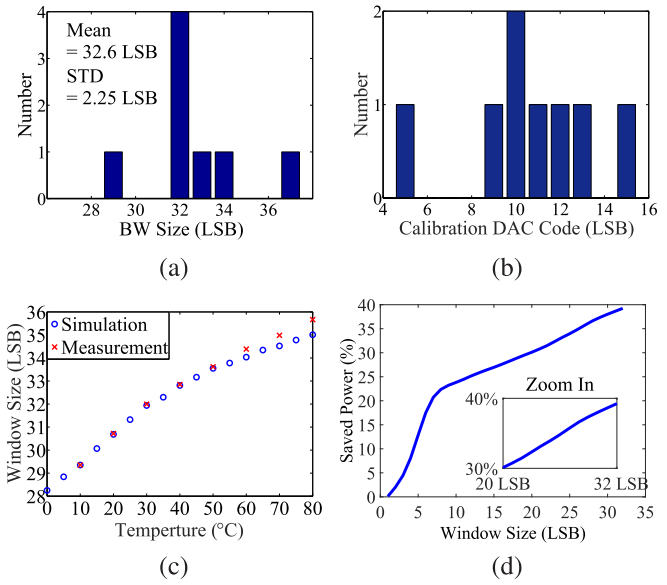


Fig. 15. (a) Variation of measured bypass window sizes from eight different chips with the bias voltage of $V_{\mathrm{ref,bump}}$ is at 400 mV. (b) Histogram of codes from a 4-bit DAC that calibrates the bypass window size to ± 32 LSBs. (c) Measurement and simulation results of the bypass window size from one prototyped ADC over the temperature range from 0°C to 80°C after one-time calibration. (d) Amount of power saving reduces gradually with the reduced calibrated bypass window size while quantizing a full-scale ECG signal.

calibration procedure can take only four sampling cycles, which is 80 μs when the sampling rate is at 50 k samples per second (kS/s).

The calibrated bypass window size increases with the temperature. The measured and simulated sensitivity is around 0.12 LSB/°C, as shown in Fig. 15(c). Since the proposed ADC circuit is for biomedical applications, the operating temperature is assumed not to change too much so that the proposed one-time foreground calibration is adequate to deal with the process variation. Besides, the calibrated bypass window size can be backed off by several bits with the cost of gradual reduction in power saving, as shown in Fig. 15(d), to prevent the window size from exceeding ± 32 LSBs at the high temperature operation. Compared with [5], the highly accurate reference voltage is only used in one-time calibration and is no longer required in normal operation.

B. Test Bench Measurements

A sinusoidal signal at 24.85 kHz is digitized by the designed SAR ADC at a sampling rate of 50 kS/s and the measured spectrum is shown in Fig. 16. The measured SNDR is 56.9 dB, and the measured SFDR is 68.7 dB with 16384 recorded points, achieving an ENoB of 9.16 with the input frequency close to the Nyquist frequency. The measured differential non-linearity (DNL) error and integral non-linearity error (INL) are plotted in Fig. 17. The peaks of the measured DNL and INL are $-0.77/0.65$ and $-0.67/0.89$ LSB, respectively.

To verify the robustness of the designed SAR ADC, the measured values of SNDR and SFDR are plotted versus different input frequencies with the same sampling rate,

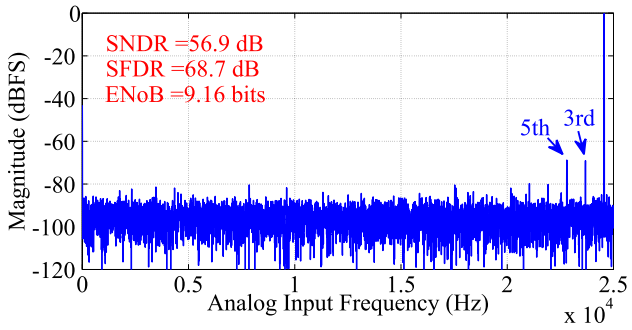


Fig. 16. Measured output spectrum from the designed SAR ADC at a sampling rate of 50 kS/s with the input frequency of 24.85 kHz.

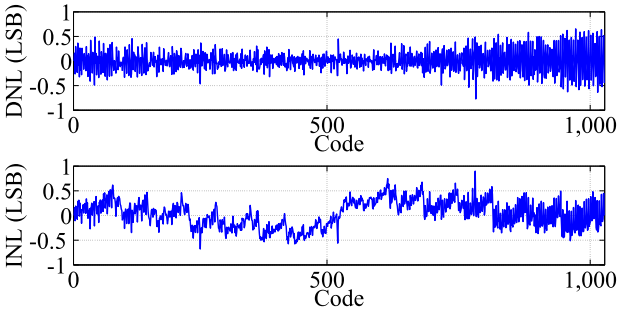


Fig. 17. Measurement results of DNL and INL.

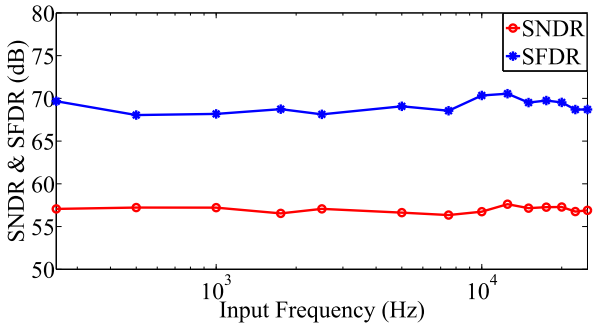


Fig. 18. Measured SNDR and SFDR results with different input frequencies at a fixed sampling rate of 50 kS/s.

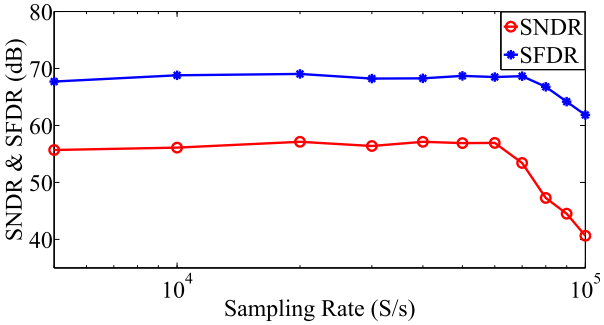


Fig. 19. Measured SNDR and SFDR values with an input frequency of 2 kHz at different sampling rates.

as shown in Fig. 18. At low frequencies, the measured SNDR and SFDR are 57.1 and 69.66 dB, respectively. The effective resolution bandwidth (ERBW) is above 25 kHz. With a fixed

TABLE I
PERFORMANCE SUMMARY FROM MEASUREMENTS

Parameter	Measured Value
Process (μm)	0.18
Unit Capacitance (fF)	1
Supply Voltage (V)	0.6
Resolution (bits)	10
Input Common-mode Voltage (V)	0.3
Input Swing Range (mV)	845
Sampling Rate (kS/s)	50
Input Frequency (kHz)	24.9
THD/SFDR (dB)	61.9/68.7
SNR/SNDR (dB)	58.4/56.9
ENoB (bits)	9.16
Power (nW)	114 (sin.) / 76.1 (ECG)
FoM (fJ/Conversion-step)	3.99 (sin.) / 2.66 (ECG)
DNL Peaks (LSB)	−0.77/0.65
INL Peaks (LSB)	−0.67/0.89
Core Area (mm^2)	0.041

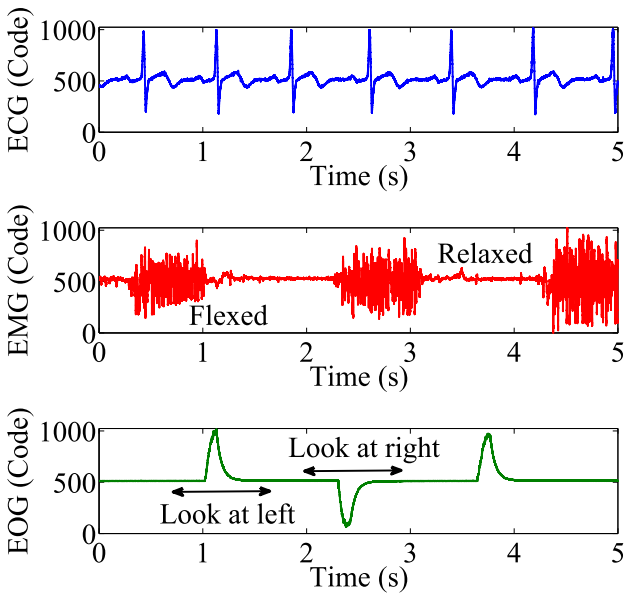


Fig. 20. Digitized electrophysiological signals that are taken from human bodies by using the designed SAR ADC. The signals displayed from the top to the bottom are ECG, EMG, and EOG, respectively.

2 − kHz sinusoidal input signal, the SNDR and SFDR measurements are performed at different sampling rates. As shown in Fig. 19, the measured values of SNDR and SFDR are 56.94 and 68.49 dB, respectively, when the sampling rate is increased to 60 kS/s.

With a full-scale 24.9 − kHz sinusoidal input signal, the measured total power consumption of the designed bypass-switching SAR ADC is 114 nW at a sampling rate of 50 kS/s. The portions from the bootstrapped T/H, the dynamic proximity comparator, BSSA logic, DAC control, and DAC switches are 0.9%, 17.9%, 48.1%, 18.4%, and 14.7%, respectively. Although the Walden FoM [27] that takes the sampling frequency into account was first proposed to compare ADC performance and have been widely adopted in many studies, it does not reflect the SNDR degradation at frequencies close to the Nyquist frequency. Therefore, another widely used FoM shown in (2) that include the term of ERBW is employed in this paper to quantify the conversion efficiency [28]

$$\text{FoM} = \frac{\text{Power}}{2^{\text{ENoB}} \times \min\{2 \times \text{ERBW}, F_s\}} \tag{2}$$

where F_s is the sampling frequency. The measured FoM number of the designed ADC with a bypass window size of ±32 LSBs in sinusoidal conversion is 3.99 fJ/conversion-step. When the ADC digitizes an artificial ECG signals at the rate of 80 b/m with the amplitude of 845 mV_{pp}, the measured power consumption drops to 76.1 nW, resulting in an FoM value of 2.66 fJ/conversion-step. The performance of the designed ADC from test bench measurements is summarized in Table I.

The measured performance is compared with recent state-of-arts in Table II. Although the ADCs in [7] and [17] can also save significant power when the input amplitude is small, they rely on the small increment in adjacent samples. Therefore, when the input signal amplitude is large, the suitable input frequencies for such ADCs need to be much lower than the Nyquist frequency, resulting in larger values for FoM. The ADCs in [5], [22], and [23] as well as this paper exploit bypass windows to save power when the input signal is small. The bypass window created in [5] relies on accurate reference voltage and two extra comparators. The bypass window size in [22] is determined by a current-starved delay unit and a charge pump circuit with background calibration. Although the approach in [22] is able to bypass more conversion-steps than the proposed approach, the time quantizer and digital logic are more complicated and consume more power. The ADCs in [10] and [23] achieve better FoM because of the V_{cm} switching scheme. However, the generation circuit for V_{cm} is not trivial and its power consumption is not counted in the FoM. Besides, the ADCs in [23] and [29] are fabricated in more advanced processes with smaller parasitic capacitances and less digital switching power.

C. Biological Measurement Results

Besides quantizing signals generated from equipments, the designed ADC is also demonstrated by digitizing physiological signals taken from human bodies through commercial Ag/AgCl skin electrodes. The captured signals are amplified by a low-noise amplifier with a gain of 40 dB. The digitized output waveforms are shown in Fig. 20. The power dissipation while recording the ECG from two arms is 74.6 nW. Besides the ECG signals, the flexed and relaxed muscle EMG signals from the right forearm are digitized, as shown in the second plot, with an average power of 86.7 nW. Finally, the digitized EOG signals taken during the eye movements with an amplifier gain of 54 dB is shown in the third plot. The average power during EOG measurement is 89.1 nW. Furthermore, when the

TABLE II
SUMMARY OF PERFORMANCE COMPARISON

	[5] 2012	[22] 2012	[7] 2014	[30] 2014	[8] 2014	[10] 2015	[31] 2015	[29] 2016	[32] 2016	[17] 2016	[23] 2016	This work 2017
Technology (nm)	180	130	180	180	180	180	110	65	180	180	90	180
Supply voltage (V)	0.6	0.8	0.5	0.6	0.9	0.6	1	0.4	0.8	0.6	0.4	0.6
Input Swing Range (V)	1.13	1.6	N/A	1.2	1.8	N/A	2	N/A	N/A	1.2	N/A	0.845
Sampling Rate (kS/s)	200	8000	4	100	100	20	20	1	200	200	750	50
Input Frequency (kHz)	90	4000	1.3	47	47	10	10	0.5	8.05	10	375	24.9
Resolution (bits)	10	12	10	10	9	10	10	8	10	10	10	10
SNDR (dB)	57.46	61.18	59.3	56.5	50.1	58.3	56.5	48.78	59.2	57.86	56.3	56.9
ENoB (bits)	9.25	9.87	9.55	9.09	8.03	9.39	9.09	7.81	9.54	9.32	9.07	9.16
Power (W)	sin./BW 1.04μ/493n	75μ	8.7n	0.39μ	1.33μ	38n	0.1μ	0.72n	0.2μ	2.01μ	780n	sin./ECG 114n/76.1n
FoM (fJ/Conv.-step)	9.48*/4.49*	10.0	4.46†	7.16	50.88	2.83	9.16	3.20	16.67†	157†	1.94	3.99/2.66
Active Area (mm^2)	0.082	0.056	0.12	0.103	0.033	0.163	0.033	0.013	0.105	0.154	0.038	0.041

* The numbers are different from those listed in [5], which are obtained from 200 kS/s with the SNDR of 57.98 dB measured with 2 kHz input signal.
† The numbers are different from those listed in [7], [17], [32], which are based on the Walden figure-of-merit adopting the sampling frequency.

inputs are steady in the rest period, the power consumption from the designed ADC is only 70.5 nW.

V. CONCLUSION

A bypass-switching SAR ADC with a newly proposed dynamic proximity comparator is presented in this paper. By employing a current correlator, the proposed dynamic proximity comparator generates the bypass signal directly along with the polarity comparison results. The size of the bypass window can be adjusted with low-voltage sensitivity to optimize power reduction for different sensing applications. The proposed comparator speed and bypass window size are analyzed in detail as well as power saving in the ECG recording application. The BSSA logic is simplified, resulting in the less switching power consumption. A prototype chip of the proposed ADC with a bypass window size of ±32 LSBs has been designed and fabricated in a 0.18- μm CMOS process and operates with a 0.6- Vsupply. The measured ENoB is 9.16 at a sampling rate of 50 kS/s with the power consumption of 114 nW when testing with a sinusoidal input signal close to the Nyquist frequency. The power consumption reduces to 76.1 nW with an FoM number of 2.66 fJ/conversion-step when the designed ADC digitizes a simulated ECG signal. The ADC is also demonstrated with several physiological signals taken from human bodies. In summary, the proposed bypass-switching SAR ADC exhibits low-power consumption, small silicon area, and low-voltage sensitivity.

APPENDIX

A. Bypass Windows Analysis

Given a small amplitude of ΔV, small-signal approximation can be applied to simplify the analysis. The charging currents from the current correlator shown in Fig. 4 can be modeled as

$$I_1 = I_{\text{cm}} + (g_m \cdot \Delta V) \tag{3}$$

$$I_2 = I_{\text{cm}} - (g_m \cdot \Delta V) \tag{4}$$

$$I_{\text{diff}} = I_1 + I_2 \tag{5}$$

$$I_{\text{bump}} = 2S \cdot \frac{I_1 I_2}{I_1 + I_2} \tag{6}$$

where I_1 and I_2 are the currents flowing through transistors M_1 and M_2 in the pseudo differential pair, respectively, g_m is transistor transconductance in the pseudo differential pair, I_{cm} is the common-mode current component, and S is the ratio of the aspect ratio of transistors in the bump cell to that in the pseudo differential pair.

Two necessary conditions to activate the proximity detection latch can be formulated as

$$\max\left(\frac{I_{\text{bump}}}{C_{\text{bump}}} \cdot t_{\text{LT}}, \quad \frac{I_{\text{diff}}}{C_{\text{diff}}} \cdot (t_{\text{phase1}} + t_{\text{LT}})\right) \geq V_{\text{LT}} \tag{7}$$

and

$$\left|\frac{I_{\text{bump}}}{C_{\text{bump}}} \cdot t_{\text{LR}} - \frac{I_{\text{diff}}}{C_{\text{diff}}} \cdot (t_{\text{phase1}} + t_{\text{LR}})\right| \geq V_{\text{LR}} \tag{8}$$

where C_{bump} and C_{diff} are the capacitances at υ_{bump} and υ_{diff} nodes, respectively, V_{LT} is the latch threshold voltage, V_{LR} is the latch resolution voltage, t_{phase1} is the period of time for voltages υ_p and υ_n being charged up so that the bump cell can be functional normally, and t_{LT} and t_{LR} are the required periods of time to meet threshold and resolution conditions.

Nevertheless, the period of t_{phase1} decreases with the increment in input amplitude. Therefore, the terms of t_{phase1} in (7) and (8) are negligible when estimating the worst case of the required period of time for t_{phase2}, in which case the input amplitude is equal to the bypass window size and the nodes of υ_{diff} and υ_{bump} are assumed to be charged up at the same speed.

The expressions of (7) and (8) can then be simplified as

$$\left(\frac{I_{\text{bump}}}{C_{\text{bump}}}\cdot\frac{B+1}{2}-\frac{I_{\text{diff}}}{C_{\text{diff}}}\cdot\frac{B-1}{2}\right)\cdot t_{\text{LT}}=V_{\text{LT}} \quad (9)$$

$$\left(\frac{I_{\text{bump}}}{C_{\text{bump}}}-\frac{I_{\text{diff}}}{C_{\text{diff}}}\right)\cdot B\cdot t_{\text{LR}}=V_{\text{LR}} \quad (10)$$

where

$$B=\begin{cases}1, & \text{if } \Delta V\le V_{\text{BW}}\\ -1, & \text{if } \Delta V> V_{\text{BW}}\end{cases} \quad (11)$$

and V_{BW} is the bypass window size. After rearranging and collecting terms in (9) and (10), the required periods of time, t_{LT} and t_{LR}, can be expressed as

$$t_{\text{LT}}=V_{\text{LT}}\cdot\frac{B+1}{2}\left\{\frac{S[I_{\text{cm}}^2-(g_m\Delta V)^2]}{I_{\text{cm}}\cdot C_{\text{bump}}}\right\}^{-1}-V_{\text{LT}}\cdot\frac{B-1}{2}\left\{\frac{2I_{\text{cm}}}{C_{\text{diff}}}\right\}^{-1} \quad (12)$$

and

$$t_{\text{LR}}=V_{\text{LR}}\cdot B\left\{\frac{S[I_{\text{cm}}^2-(g_m\Delta V)^2]}{I_{\text{cm}}\cdot C_{\text{bump}}}-\frac{2I_{\text{cm}}}{C_{\text{diff}}}\right\}^{-1}. \quad (13)$$

The maximum period of time for the proposed comparator to make proximity decision, t_{phase2}, can be expressed as

$$t_{\text{phase2}}=\max\left(t_{\text{LT}},t_{\text{LR}}\right). \quad (14)$$

The bypass window size can be estimated from (13) by assuming the $t_{\text{LR}}=\infty$ when $\Delta V=V_{\text{BW}}$s. Therefore

$$\frac{S[I_{\text{cm}}^2-(g_m\cdot V_{\text{BW}})^2]}{I_{\text{cm}}\cdot C_{\text{bump}}}-\frac{2I_{\text{cm}}}{C_{\text{diff}}}=0 \quad (15)$$

and

$$V_{\text{BW}}=\frac{I_{\text{cm}}}{g_m}\cdot\sqrt{1-\frac{2}{S}\cdot\frac{C_{\text{bump}}}{C_{\text{diff}}}}. \quad (16)$$

The bypass mechanism is activated when $\Delta V<V_{\text{BW}}$.

B. Power Saving Estimation

The power consumption of the proposed bypass-switching ADC can be estimated from the product of the probability that the bypass mechanism will be triggered and the power consumption of the corresponding phase, which can be expressed as the following equations

$$P_{(C)}=\frac{P_{(C),\max}}{10}\cdot\sum_{i=1}^{10-M}(M+i)\cdot f(i) \quad (17)$$

$$P_{(L)}=\frac{P_{(L),\max}}{319-4M}\cdot\sum_{i=1}^{10-M}(28M+32i-1)\cdot f(i) \quad (18)$$

$$P_{(D)}=\frac{P_{(D),\max}}{19-M}\cdot\sum_{i=1}^{10-M}(M+2i-1)\cdot f(i) \quad (19)$$

$$P_{(S)}=\frac{P_{(S),\max}}{2^9-1}\cdot\sum_{i=1}^{10-M}\left(\sum_{k=0}^{M+i-2}2^k\right)\cdot f(i) \quad (20)$$

$$P_{(T)}=P_{(C)}+P_{(L)}+P_{(D)}+P_{(S)}+P_{(R)} \quad (21)$$

where $P_{(C)}$, $P_{(L)}$, $P_{(D)}$, $P_{(S)}$, $P_{(R)}$, and $P_{(T)}$ denote the amount of power consumption related to the comparator (C), the BSSA logic (L), the DAC controls (D), the buffers for switching DAC capacitors (S), the remaining circuit blocks that are not related to the bypass mechanism (R) such as the sampling switch and the code recovery circuit, and the total power consumption (T), respectively. Besides, the window size is represented by 2^M LSBs, and $f(i)$ is the probability that the bypass mechanism will be triggered in the ith phase. The symbols of $P_{(X),\max}$ represent the power consumption of sub-blocks without triggering bypass mechanism. The corresponding values of $P_{(X),\max}$ and $P_{(R)}$ are obtained from simulation.

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