Analysis and Design of a 30- to 220-GHz Balanced Cascaded Single-Stage Distributed Amplifier in 130-nm SiGe BiCMOS

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***Abstract*— This paper describes a novel distributed amplifier (DA) architecture for ultra-wide band of operation at millimeter-wave frequency. The DA consists of two cascaded single-stage DAs (CSSDAs) embedded in a balanced architecture. The implemented design retains the benefits of CSSDAs in terms of high maximum frequency, broad band of operation, and compact area, while significantly improving the amplifier input and output matching and its linearity with the balanced architecture, which are the major issues of this class of circuits. The small-signal analysis is provided in detail and explains the nature of the poor output matching typical of this class of DAs. Furthermore, the CSSDA gain is calculated as function of frequency and circuit parameters, extending available literature results, and providing direct design guidelines with a compact formula. Experimental validation is demonstrated with the fabrication of a circuit prototype in a 130-nm SiGe BiCMOS process. The circuit is able to provide an average of 16-dB gain over the frequency band 30–220 GHz, with input- and output-return losses above 10 dB, and a maximum measured output-referred 1-dB compression point of 4.5 dBm. To the best knowledge of the authors, the measured matching and linearity are the best reported for CSSDAs.**

***Index Terms*— BICMOS integrated circuits, distributed amplifier (DA), distributed parameter circuits, millimetre-wave integrated circuits, ultra-wideband technology.**

I. Introduction

AS FORMALIZED in the Shannon-Hartley theorem, one fundamental approach to increase the data rate of communication lies in increasing the bandwidth of the radio channel in use. Unallocated ultra-wide bands of operation can be found for frequencies in the millimeter-wave range, from 30 to 300 GHz. For these reasons, a keen research interest is devoted to millimeter-wave and ultra-wideband electronics. Since one fundamental block of transceiver and imaging systems is the amplifiers, useful gain over frequency bands of hundreds of gigahertz are required. Introduced by Percival [1] in 1936, distributed amplifiers (DAs) are widely used to achieve such wide bands of operation, in conjunction with high gain and good matching. The most common DA is the Travelling-Wave Amplifier (TWA), which consists of several active elements—or gain-cells—embedded between two transmission lines used to guide input and output signals. The use of several cells is the main drawback of TWAs which require larger area and dissipate more dc power compared to tuned amplifiers.

At their core, distributed amplification techniques rely on synthetic transmission lines realized embedding the gain-cell capacitances into transmission lines. In practical cases, the main limitation to high-frequency operation is the resistive losses at the input of the cells [2], which increase with the square of the operation frequency. Different design solutions have been reported with strategies for minimizing or compensating the gain-cell losses [2], [3]; however, the most straightforward design approach is the reduction of the number of employed gain cells. The single-stage configuration is the fastest distributed architecture, but also the one with lowest gain. Cascading several single-stage DAs [5], [6] achieve gain levels comparable to TWAs, while still reaching the highest possible cutoff frequency. Amplifiers with such structure are referred to as cascaded single-stage DAs (CSSDAs) [7]. Moreover, CSSDAs require less power and chip-area than TWAs for comparable gain since the input signal distribution is different [8], [9]: while all the cells of TWAs receive the same input signal with different phase delays, in CSSDAs, the output of each cell is used as input of the following one. A comparison between the CSSDA and TWA responses for the same set of design parameters was previously presented in [11] and [12], reaching the same conclusion. For the same reason, CSSDAs are less linear than TWAs, resulting in lower input and output power levels at the 1-dB compression point [11]. Although linearity limitations can be solved with higher dc power levels, a second and more serious drawback of CSSDAs is the poor output matching: this results from features inherent to the circuit topology, which renders the conventional configuration of CSSDA unmatchable at the upper edge of its operation band [11]–[13]. While several implementation of CSSDAs has been demonstrated [12]–[19], all of them present poor output-matching characteristics at the highest end of the band of operation, ranging from $|S_{22}| = -5$ dB below 100 GHz [14]–[16], to $|S_{22}| = 0$ dB for designs operating above 200 GHz [12], [13]. This effect appears to be associated with the circuit topology, as it is independent from the fabrication technology. Although the basic principle of

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operation is well understood, a compact and general expression for the frequency response of the circuit has not been reported so far; in particular, no expression of the output impedance suitable to describe the unmatched behavior is available.

This paper presents the first complete analysis of the CSSDAs behavior as function of all key parameters and can serve as specific design guideline. In particular, the circuit analysis explains quantitatively the typical limitations of the output matching behavior. As the analysis shows how the problem has no solution within the circuit topology itself, this paper proposes the balanced architecture to retain the frequency response advantages of the CSSDA and yet match the amplifier over the full band of interest. A circuit sample fabricated in a 130-nm SiGe BiCMOS process with maximum frequency of oscillation of 370 GHz validates the concept experimentally. The description of the fabrication process is in Section II, while the general analysis for CSSDA is in Section III. The analysis and the design of the proposed balanced solution are given in Section IV. Section V presents the measurement results used to validate the proposed analysis, while Section VI summarizes the work with a comparison against the state of the art.

II. Technology

The circuit subject of this paper is fabricated in a 130-nm SiGe BiCMOS process. At the time of writing, this process is the fastest SiGe BiCMOS commercially available [20], and it is offered by IHP as SG13G2. Under optimal bias conditions, the nominal power-gain cutoff frequency ($f_{\max}$) is 450 GHz, which is reduced to 370 GHz for the actual fabrication run of the presented design. The transistors are well suited for millimeter-wave applications; this feature is further supported by the process back end, which enables the fabrication of high-quality inductors and transmission lines through the availability of two thick top metal layers on top of five lower layers for dense interconnections. Among them, the lowest metal has the smallest thickness to enable fine lithography used for the contact with the silicon devices, while the top metals are thicker in order to sustain higher current densities and to reduce their sheet resistance. Altogether the seven metal layers enable the design of coplanar, microstrip, and stripline waveguides with a high degree of freedom for the dielectric thickness. This process offers also passive components such as polysilicon resistors and metal-insulator-metal capacitors with high-quality factors and high resonance frequencies.

III. CSSDA Analysis

In this section, the circuit analysis of CSSDAs is provided with the aim of quantifying its operation mechanisms and intrinsic limits. The section is divided into two parts: the first one recalls the fundamental concept of distributed amplification, while the second presents the general circuit analysis for CSSDAs.

A. Distributed Amplification

In any of their possible implementations, the operation of DAs rely on synthetic transmission lines, which consists of

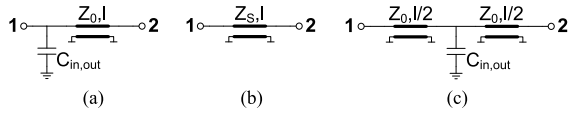

Fig. 1. (a) Two-ports formed by the capacitor $C_{\text{in,out}}$ and the transmission line of impedance Z_0 and length ℓ. (b) Equivalent synthetic transmission line obtained with (1). (c) Two-ports formed by $C_{\text{in,out}}$ interposed between two lines of impedance Z_0 and length $\ell/2$.

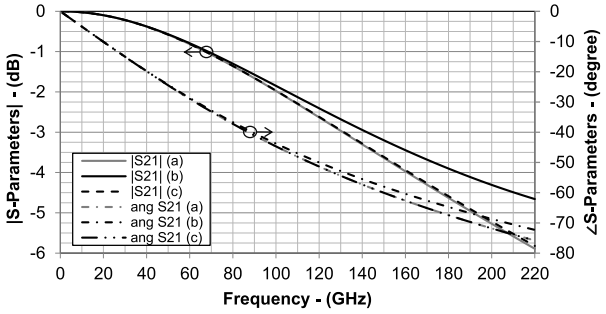

Fig. 2. Comparison of the transmission parameters for the circuit of Fig. 1(a)–(c).

TABLE I
Transmission Line Parameters

ℓ_1 [μm]	ℓ_2 [μm]	L [μH/m]	C [pF/m]	Z_0 [Ohm]
50	50	0.42	92.5	65

sections of physical transmission lines loaded by the input and output capacities of the amplifier gain-cells $C_{\text{in,out}}$. The general assumptions for the modeling of DAs are thus recalled here to set aside the preliminary equivalences that will be used in Section III-B to perform the circuit analysis of CSSDAs.

As their physical counterparts, the synthetic transmission lines are characterized by characteristic-impedance Z_S and propagation constant β_s [21]

$$Z_S = \sqrt{\frac{L'}{C' + \frac{C_{\text{in,out}}}{\ell}}} \quad \beta_s = \omega\sqrt{L'\left(C' + \frac{C_{\text{in,out}}}{\ell}\right)} \tag{1}$$

where ω is the signal angular frequency, L' and C' are the inductance and capacitance per unit length of the physical lines, and ℓ the distance between the gain cells. The fundamental assumption in distributed amplification techniques is thus the equivalence between a transmission line loaded by a capacitor, and the synthetic transmission line obtained with (1). The networks are shown in Fig. 1. This equivalence allows embedding the cell capacitances in the transmission lines structure, and inherently results are a flat and wideband frequency response. The simulated behaviors of the networks of are compared in Fig. 2. For the sake of this example and the practical relevance within this paper, the line-properties and attached capacitance are chosen in the same order of those of the presented design: $C_{\text{in,out}}$ is 50 fF, ℓ 25 μm, and L' and C' are summarized in Table I within Section III-B. The frequency band of interest is from 1 to 220 GHz. In this band, the models in Fig. 1 have negligible difference in the response: for the insertion-phase below 1° at 100 GHz, and

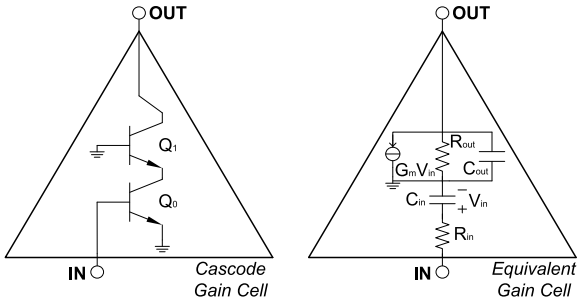

Fig. 3. Cascode gain cell and equivalent small-signal circuit.

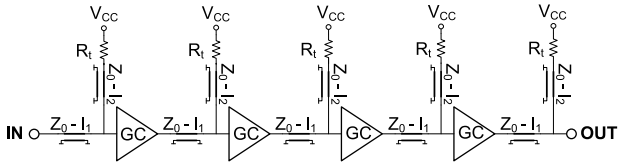

Fig. 4. CSSDA circuit schematic. The gain cells are labelled with GC.

below 6° at 220 GHz; while for the insertion-loss below 0.2 dB at 100 GHz, and 1 dB at 220 GHz. The synthetic-line model is thus an approximation of the circuits of Fig. 1(a) and (c), which provides compact description for the line-capacitor circuit. In subsection III-B, the presented model will be used for the analysis of the CSSDA response.

B. CSSDA Circuit Analysis

As mentioned above, the analysis of DAs is based on embedding the cell capacitances into the transmission lines to create synthetic transmission lines. A compact equivalent description of the gain elements is required for the calculation of the properties of these synthetic lines. If cascode amplifiers are in use, as in this paper, high isolation is achieved between input and output of the cells, and an unilateral model can be applied [4]. The equivalent small-signal model of the cascode cells is shown in Fig. 3: the device is modeled at the input with a resistance R_{in} and a capacitance C_{in}. The output consists of a transconductance G_m, in parallel with output capacitance C_{out} and resistance R_{out}. R_{out} can be neglected because of the high output-resistance typical of cascode amplifiers [4].

The circuit schematic of CSSDAs is illustrated in Fig. 4. This DA consists of a cascade of single-stages where the parasitic capacitances of the cell are embedded into transmission line as in the configuration of Fig. 1(c). Fig. 5 shows the equivalent circuit of CSSDAs obtained with the representation of the cell in Fig. 3, and used for the *circuit analysis*. The input signal propagates into the synthetic-line formed by ℓ_1, ℓ_2 and C_{in} as in Fig. 1(c). ℓ_1 and ℓ_2 are thus assumed to be equal. The impedance of this synthetic line is Z_S, calculated as in (1) with $\ell = \ell_1 + \ell_2$. Finally, the line is terminated with the resistor R_T, of the same value as Z_S. This ensures matching condition between the synthetic line and the termination resistor; hence only forward-propagating waves are present into this CSSDA section. The CSSDA input-impedance Z_{IN} is thus Z_S, and it is assumed equal to the generator impedance. The input-voltage V_{IN} thus propagates till Section A accumulating a phase delay of $\beta_S \ell/2$. The voltage across the input capacitance of the first

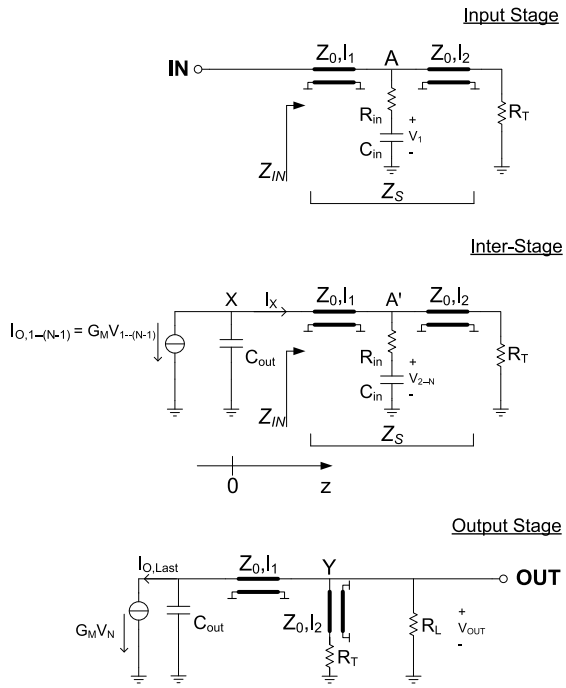

Fig. 5. Equivalent small-signal circuit of the CSSDAs in Fig. 4.

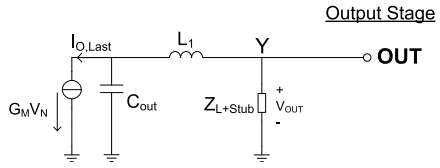

Fig. 6. Equivalent small-signal circuit of the last CSSDAs stage. The line ℓ_2 and the resistors $R_T - R_L$ have been replaced with the impedance $Z_{L+\text{Stub}}$, while the line ℓ_1 has been approximated with a lumped inductance L_1.

gain-cell V_1 and the resulting output current of the first gain cell I_{O1} are then [21]

$$V_1 = \frac{V_{\text{IN}}}{1 + j\omega R_{\text{in}} C_{\text{in}}} \cdot e^{-j\beta_S \ell/2} \quad I_{O1} = G_m V_1. \tag{2}$$

With reference to Fig. 5, I_{O1} is the input source of the first inter-stage and is filtered by the output-cell capacitance C_{out} placed between node X and ground. The actual input-current and input-voltage of the second stage are I_X and V_X, which can be expressed as

$$I_X = \frac{-G_m V_1}{1 + j\omega Z_S C_{\text{out}}} \quad V_X = I_X \cdot Z_S \tag{3}$$

where I_X travels thus in the second stage along the loop consisting of Z_S and R_T. At section A', it accumulates a phase delay of $\beta_S \ell/2$, as in the first section. Combining (3) with these considerations, the relation between the voltage across the C_{in} of the $(N-1)$th stage, and that across the C_{in} of the (N)th stage can be expressed as

$$V_N = \frac{Z_S G_m V_{N-1} (-1)^{N-1}}{(1 + j\omega Z_S C_{\text{out}}) \cdot (1 + j\omega R_{\text{in}} C_{\text{in}})} \cdot e^{-j\beta_S \ell/2}. \tag{4}$$

The relation between the output current of the last cell $I_{O,\text{Last}}$ and the output voltage V_{OUT} can be calculated with the equivalent circuit of Fig. 6: the impedance $Z_{L+\text{Stub}}$ represents the network consisting of R_L, R_T and the T-line of

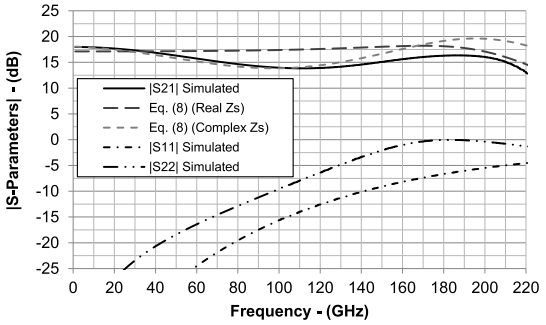

Fig. 7. Comparison between the circuit simulation of Fig. 5 and the gain formula in (8).

TABLE II
SMALL-SIGNAL PARAMETERS OF THE GAIN CELL

C_{in} [fF]	C_{out} [fF]	R_{in} [Ohm]	R_{out} [Ohm]	G_m [mS]
61.5	23	6.7	500	80

length ℓ_2; while the $\ell_{1,2}$ have been replaced with a lumped inductance $L_{1,2}$ of value $L' \cdot \ell_{1,2}$, under the assumption that these two lines are small compared to the wave length. As a result, $V_{\rm OUT}$ is expressed as

$$V_{\rm OUT} = -I_{O,\rm Last}\frac{A}{B} \tag{5}$$

where A and B are defined as follows:

$$A = R_L(R_T + j\omega L_2) \tag{6}$$

$$B = R_L + R_T - \omega^2(L_1 C_{\rm out}(R_L + R_T) + R_L L_2 C_{\rm out}) + j\omega(L_2 + C_{\rm out}(R_L R_T - \omega^2 L_1 L_2)). \tag{7}$$

The combination of (2)–(7) leads to *the analytic expression of the frequency response of a N-stages CSSDA*

$$\frac{V_{\rm OUT}}{V_{\rm IN}} = \frac{Z_S^{N-1}(-G_m)^N e^{-j\beta_S \ell N/2}}{(1 + j\omega R_{\rm in} C_{\rm in})^N \cdot (1 + j\omega Z_S C_{\rm out})^{N-1}} \cdot A/B. \tag{8}$$

This expression of the gain is compared in Fig. 7 against the circuit simulation of the model in Fig. 5, for the values of the line parameters in Table I, the gain cell in Table II, R_T and Z_S of 25 Ω, and the same generator, load, and CSSDA input and output impedances. Equation (8) predicts the gain with good accuracy in the lower and higher part of the spectrum of amplification, while deviates in the intermediate region. At low frequency, in fact, the synthetic-line model fits with negligible error the line-capacitor circuit (Fig. 1), and it starts to deviate from it for increasing frequency, as shown at 100 GHz in the simulation of Fig. 7. On the other hand, the error between the circuit simulation and (8) reduces toward 200 GHz. The same frequency trend can be appreciated in Fig. 8 where it is illustrated the comparison between the phase of the CSSDA gain, simulated with the circuit of Fig. 5 and with the gain formula in (8). The real and imaginary parts of the CSSDA input-impedance $Z_{\rm IN}$ are shown in Fig. 9. As described before, if Z_S is equal to R_T, $Z_{\rm IN}$ should real and equal to them. On the other hand, as it can be seen from Fig. 9, the synthetic-model loses accuracy at higher frequency in predicting the

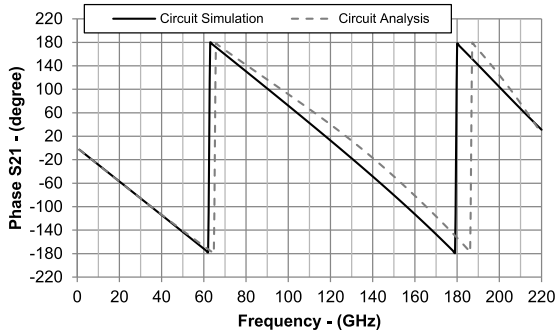

Fig. 8. Comparison between the CSSDA insertion-phase simulated with the circuit of Fig. 5 and formula of the gain in (8) evaluated with real Z_S.

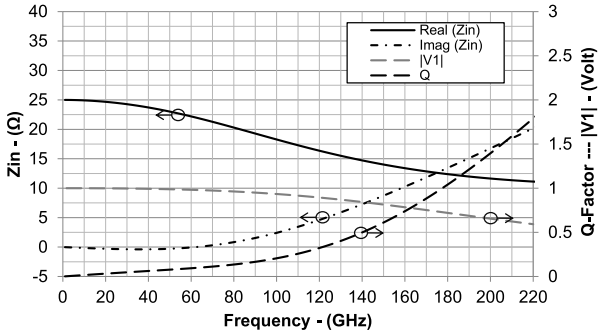

Fig. 9. Comparison between the CSSDA input-impedance, the voltage V_1 for the input circuit of Fig. 5 and Q-factor of this network.

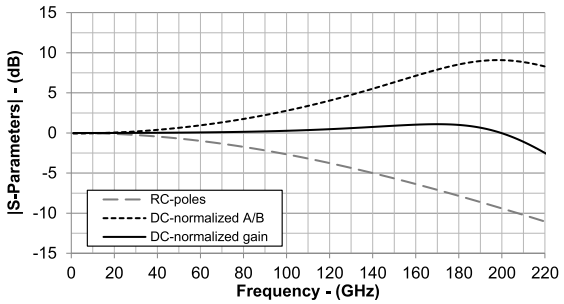

Fig. 10. Contributions of the terms in (8) to the frequency trend of CSSDA gain.

response of the line-capacitor circuit, and $Z_{\rm IN}$ decreases in the real part and increases in the imaginary one. Due to the periodic structure of the amplifier, $Z_{\rm IN}$ is also equal to the input impedance of the intermediate stages (Fig. 5). This impedance is labeled Z_S in (3), and it is used to calculate the gain in (8). Fig. 7 shows then the gain re-calculated with (8) and taking in consideration the frequency variations and the imaginary part of Z_S. Equation (8) now predicts with better accuracy the circuit simulation, and it deviates only in the upper part of the band due to the approximation of the output transmission lines $\ell_{1,2}$ with lumped inductance $L_{1,2}$.

With its close approximation of the complete circuit, (8) is a powerful tool for important *considerations on the amplifier frequency response*. Fig. 10 shows the frequency trend of the terms in (8). The limiting factors at high frequencies are the frequency poles associated with the input and output networks, originating from $R_{\rm in}C_{\rm in}$ and $Z_S C_{\rm out}$, respectively. The gain roll

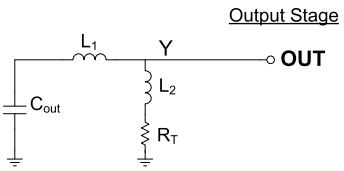

Fig. 11. Equivalent circuit for the calculation of the CSSDA output impedance. The lines ℓ_1 and ℓ_2 have been replaced with equivalent inductors L_1 and L_2.

off for increasing frequency is compensated by the term A/B introduced by the output network with the inductance L_2: at low frequency of operation it can be approximated as a short dividing the current $I_{O,\text{Last}}$ between R_T and the load, while at higher frequency this inductor offers a larger impedance, which directs more and more current to the load rather than in R_T. As it is shown in Fig. 10, the CSSDA gain is constant up to the resonance frequency of the term A/B representing the output network, and it drops past that. This resonance frequency $f_{R\text{-OUT}}$ can be expressed as

$$f_{R\text{-OUT}} = \frac{1}{2\pi}\sqrt{\frac{1}{C_{\text{out}}\left(L_1 + L_2\frac{R_L}{R_L+R_T}\right)}}. \tag{9}$$

For the presented simulation $f_{R\text{-OUT}}$ occurs at 190 GHz, and it can be used for approximate the 3-dB upper corner frequency of the amplifier, as well its bandwidth. The CSSDA gain-bandwidth product (GBP) can be thus expresses as

$$\text{GBP}_{\text{CSSDA}} = \left(\frac{P_{\text{DC}}}{NV_tV_{\text{cc}}}\right)^{2N}\cdot\left(\frac{Z_S^N R_L}{Z_S+R_L}\right)^2\cdot f_{R\text{-OUT}} \tag{10}$$

which is obtained assuming $Z_S = R_T$, and substituting G_m with $(P_{\text{DC}}/(NV_tV_{\text{cc}}))$, where P_{DC} is the dissipated power, V_{cc} the voltage supply, and V_t the thermal voltage. Equation (10) shows that the GBP grows with P_{DC}^{2N} with N the number of cells. This is a key advantage with respect to the TWAs, where the GBP is proportional to $(P_{\text{DC}})^2$ [23].

The equivalent CSSDA circuit presented in Fig. 5 can be used also for *considerations on the amplifier matching*. If on one hand, the output network enhances the gain compensating the system poles, on the other deteriorates the output matching of the amplifier. The output impedance of the CSSDA consists of two admittances connected in parallel: Y'_T from the series $\ell_2{-}R_T$, and Y'_{CO} from the series $\ell_1{-}C_{\text{out}}$. The circuit can be simplified again replacing the lines $\ell_1{-}\ell_2$ with the equivalent lumped inductors L_1 and L_2. The equivalent circuit of the output stage is thus illustrated in Fig. 11. As a result, the output admittance of the circuit can be expressed as

$$Y_{\text{OUT}} = \frac{1-\omega^2C_{\text{out}}(L_1+L_2)+j\omega C_{\text{out}}R_T}{(R_T+j\omega L_2)(1-\omega^2C_{\text{out}}L_1)}. \tag{11}$$

Conjugate matching, $Y_{\text{OUT}} = 1/R_L$, can be achieved only for low frequencies, where the lines can be approximated as a short and C_{out} as an open, and for the special case or $R_T = R_L$. For increasing frequency of operation the line inductance and the C_{out} capacitance gradually deteriorate the matching at the output. Finally, at $f_{R\text{-OUT}}$ an LC resonance occurs and the output is severely un-matched, as it can be seen from Fig. 7 around 200 GHz. This behavior is an open problem of the CSSDAs state of the art [11]–[13], which can be addressed with the balanced architecture, as it will be shown in Section IV. It can be further noted in Fig. 7 that also $|S_{11}|$ degrades toward high frequency. As explained above, this is due to the input synthetic line deviates from the values of impedance predicted in (1) for frequencies of operation approaching the LC resonance of synthetic-line itself [4]

$$f_{\text{LC\_Synthetic\_Input}} = \frac{1}{\pi\sqrt{L_{\text{line}}C_{\text{in}}}} \tag{12}$$

where L_{line} is the line inductance $L'\cdot(\ell_1+\ell_2)$, and the line capacitance has been neglected with respect to the cell-input capacitance. For the simulation of Fig. 7 this occurs at 219 GHz.

Finally, an *alternative explanation of the broad band behavior of the CSSDA as a low-Q amplifier* achieved through resistive elements can be provided with the simulation in Fig. 9, where the Q-factor of the input network is compared against the voltage V_1 and the amplifier input impedance. As it can be appreciated for increasing frequency of operation where the synthetic-model loses validity, V_1 drops as well. From Fig. 9 is thus possible to associate the frequency band of amplification with the one where the Q-factor of the network is the lower. The analytically expression of the Q-factor of the input line is in (13), as shown at the bottom of this page.

IV. Balanced CSSDA: Analysis and Design

This section gathers the design and the circuit analysis of the balanced CSSDA subject of this paper. The section is divided into four parts: the first one illustrates the general architecture of the circuit; the second lists the benefits of the balanced architecture and shows the designed Lange coupler; the third specializes the presented CSSDA analysis to the balanced case where gain-peaking techniques are employed to extend the amplifier frequency band of operation; and the fourth describes the employed gain cells.

A. Architecture

The circuit schematic of the presented amplifier is shown in Fig. 12. It consists of input and output on-chip Lange couplers, which enclose two CSSDA modules in a balanced configuration. Each of the enclosed DAs consists of four gain cells, connected via custom transmission lines. These integrated lines are compliant with the metal density rules of the process, and the resulting structure is a hybrid between coplanar and microstrip [3]. The characteristic impedance of

$$Q = \left|\frac{\omega L_1[(\omega C_{\text{in}}(R_T+R_{\text{in}}))^2+(1-\omega^2L_1C_{\text{in}})^2+1-\omega^2L_1C_{\text{in}}]-\omega^2C_{\text{in}}\left(R_T^2-\omega^2L_1C_{\text{in}}R_{\text{in}}^2\right)}{R_T+R_{\text{in}}(\omega^2L_1C_{\text{in}})^2+R_TR_{\text{in}}(R_T+R_{\text{in}})(\omega C_{\text{in}})^2}\right| \tag{13}$$

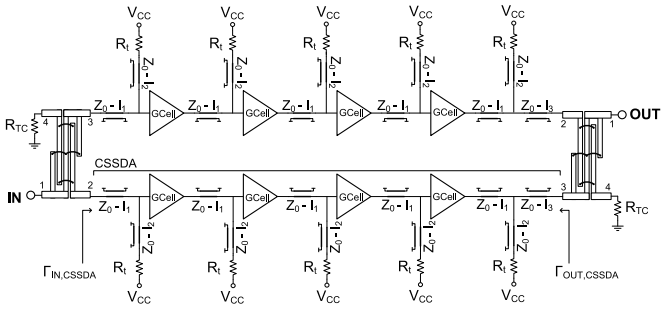

Fig. 12. Circuit schematic of the presented Balanced CSSDA.

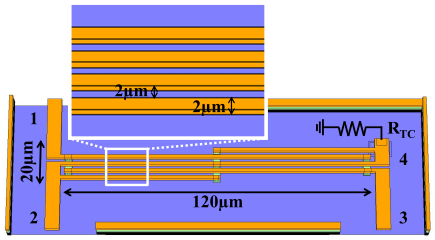

Fig. 13. 3-D view of the Lange coupler with the four terminals marked, and the physical dimensions annotated. The blue layer is the ground metal-plate underneath realized with the lowest metal of the stack, while the signal conductors, drawn in orange, are realized with the highest metal of the stack.

the lines is $Z_0 = 65\ \Omega$, which reduces to a lower synthetic-line impedance after the insertion of the cells, as predicted in (1).

B. Balanced Design

Good input and output matching are required to maximize power gain and mitigate stability issues. Especially at high frequencies, the optimization of $|S_{11}|$ and $|S_{22}|$ is complicated by the model inaccuracies of the employed devices and the process variations [22]. Moreover, as discussed above, CSSDAs suffer of poor output matching at the higher end of their band. The balanced architecture, achieved with integrated Lange couplers plus two identical CSSDA modules driven in quadrature, it overcomes these limitations and offers a robust matching to the load and the generator impedance at the cost of higher power consumption and silicon footprint.

The designed coupler is a microstrip Lange-coupler with a ground metal beneath. The component is shown in Fig. 13: it splits the power fed at port 1 to ports 2 and 3, inserting a relative phase shift between them of 90°, while port 4 is isolated and terminated with a matched resistance R_{TC} of 50 Ω. Fig. 14 shows the simulated S-Parameters of the coupler with the port definition of Fig. 13. $|S_{31}|$ and $|S_{21}|$ are -3.8 dB at 200 GHz: for this frequency the couplers divide the power at port 1 in half while inserting 0.8 dB of path losses. To ease the description of the coupler behavior, Fig. 15 shows the difference between the path responses in terms of phase delay and insertion losses.

The two orthogonal input signals are applied to the CSSDAs (Fig. 12), whose input and output impedances are represented with the reflection coefficients $\Gamma_{\mathrm{IN,CSSDA}}$ and $\Gamma_{\mathrm{OUT,CSSDA}}$. The waves reflected at their inputs are combined by the coupler

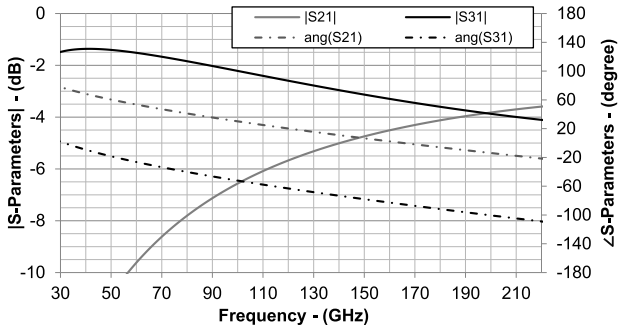

Fig. 14. Simulated S-Parameters of the designed Lange couplers.

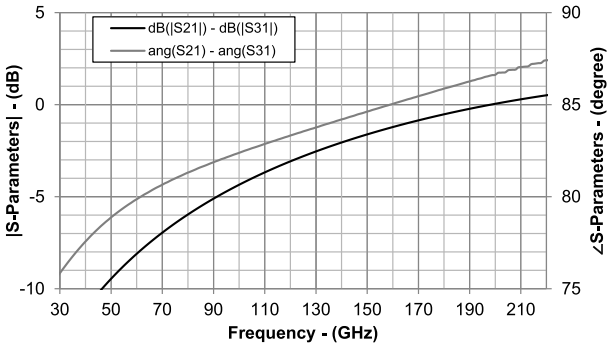

Fig. 15. Simulated phase and amplitude imbalance for the designed coupler.

and the total phase shift between the two waves accounts now to 2 times 90°, hence 180°. This results in a destructive interference which always matches the input port to the generator impedance. The same mechanism is also exploited at the amplifier output. This, as validated by the measurement results in Section V translates in wideband input and output matching covering the frequency region where the phase and amplitude balance of the two combiner paths is the highest. For this design, this frequency region is around 200 GHz, exactly where two CSSDA modules suffer of poor matching. It is important to notice that toward dc the couplers show large amplitude imbalance (Fig. 15), and the balanced architecture is not able anymore to improve the matching. In this condition, the matching of the system is dominated by the matching of each of the individual CSSDAs. This, as shown in Fig. 7, is satisfactory: below -10 dB for frequencies below 100 GHz. Above 100 GHz, the output matching of the CSSDA modules deteriorates gradually toward high frequency, but at the same time the amplitude imbalance between the combining path gradually decreases, improving the output matching of the balanced CSSDA. This effect results in an $|S_{22}|$ constant over frequency and is achieved tailoring the coupler response to the output matching degradation of the CSSDAs. The balanced architecture is, therefore, exploited to improve the matching of the CSSDAs only toward the higher frequencies of operation. This approach breaks the tradeoff between gain and output matching originating from the peaking output network of the amplifier.

Another important feature of balanced amplifiers is the improved linearity. In balanced amplifiers, in fact, the input

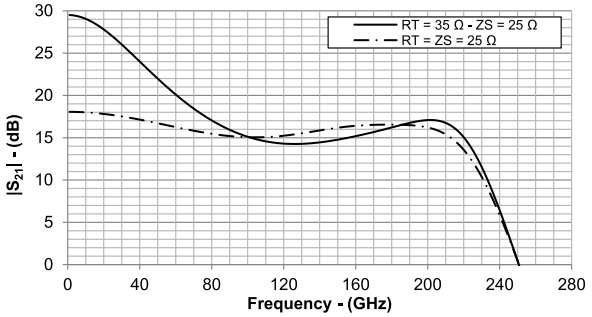

Fig. 16. Circuit simulation of the CSSDA response for equal and different values of the synthetic impedances and termination resistance. A gain-peaking toward low frequency has been achieved using R_T higher than Z_S.

signal is divided between two identical amplifiers (the CSSDA modules in this paper) improving by a factor 2 the input linearity. In similar way, the two amplified signals are combined at the output increasing as well by a factor 2 the output linearity. Depending on the actual design, the stand-alone CSSDAs will compress first at the input or at the output, but the balanced architecture is beneficial in either case, resulting in an improvement by a factor of 2 for the overall amplifier linearity. Once again this comes at the cost of higher power consumption.

In Fig. 14, it can be appreciated that toward low frequencies the path from ports 1 to 2 suffers from increasing insertion losses. For frequencies around 30 GHz then the input-signal propagates mostly from ports 1 to 3 of the input coupler (Fig. 12), while being highly attenuated at port 3. At the output, since the coupler is now rotated by 180°, the attenuation is on the previous un-attenuated input signal. The couplers are then a limiting factor for widebands operation, considering the CSSDAs capability of amplification from dc to hundreds of gigahertz [12], [13]. As it will be shown in Section IV-C, to compensate this effect and extend the bandwidth of the whole amplifier, the CSSDA have been optimized with a peaking of the gain toward low frequency.

C. CSSDA Modules: Analysis and Design

The two CSSDAs, which form the presented balanced amplifier is an evolution from the conventional CSSDA architecture presented in Section III. For these circuits, in fact, two gain-peaking techniques are introduced in the low and high part of the amplifying spectrum.

1) Peaking of the Gain Toward Low Frequency: The peaking of the gain toward dc is used to fit at best the balanced architecture, compensating the increasing insertion losses of the couplers (Fig. 14). To achieve the gain peaking toward low frequency, the synthetic-line impedance Z_S is designed lower than R_T, as well ℓ_1 is shorter than ℓ_2. The peaking of the gain with these design choices is illustrated in Fig. 16 against the conventional CSSDA. To analytically quantify this effect, the intermediate Nth section of the CSSDA for this case is provided in Fig. 17. The length of ℓ_2 is divided into ℓ'_2, equals to ℓ_1, and ℓ''_2. This extra transmission line length is in series with the termination resistor R_T, and the

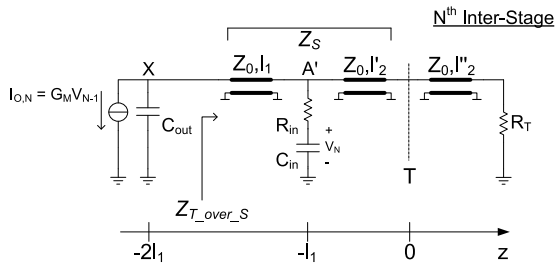

Fig. 17. Equivalent small-signal circuit of the generic Nth stage of a CSSDAs with ℓ_2 longer than ℓ_1. ℓ_2 has been divided into ℓ'_2, which is equal to ℓ_1, and ℓ''_2 which is the remaining part.

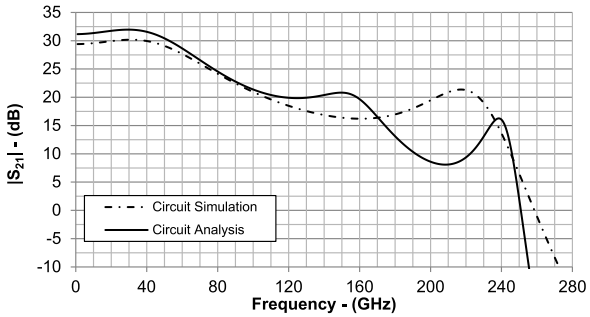

Fig. 18. Comparison between simulation and circuit analysis in (15) of the CSSDA gain with peaking toward low frequency.

two form together the termination-impedance Z_T. Since Z_T is different from Z_S, the forward-propagating wave will be partially reflected at the interface T, and a reflection coefficient Γ_T is defined. The voltage at section A' in Fig. 17 will be thus the sum of the waves propagating forward and backward

$$V'_A = V_X \cdot D, \quad D = \frac{1+\Gamma_T e^{-j\beta_S 2\ell_1}}{1+\Gamma_T e^{-j\beta_S 4\ell_1}} e^{-j\beta_S \ell_1}. \tag{14}$$

With V_X as in (3) but with Z_S replaced by the impedance seen at section X toward the load (Fig. 17). This impedance is indicated with $Z_{T\_over\_S}$, and it is equal to the transformation of Z_T over ℓ_1 plus ℓ'_2, which account to two times ℓ_1. Using (14), to modify the circuit analysis presented in Section III, the gain can be formulated for the general case of $Z_T \neq Z_S$, and $\ell_1 \neq \ell_2$

$$\left|\frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}}\right| = \left|\frac{(Z_{T\_over\_S})^{N-1}(-G_m \cdot D)^N}{(1+j\omega R_{\mathrm{in}} C_{\mathrm{in}})^N \cdot (1+j\omega Z_{T\_over\_S} C_{\mathrm{out}})^{N-1}} \cdot \frac{A}{B}\right|. \tag{15}$$

With A and B as in (6) and (7) but with Z_T in place of R_T, and Z_S replaced by $Z_{T\_over\_S}$. The comparison between circuit simulation and (15) is shown in Fig. 18 for the actual design values of $\ell_1 = 50$ μm, $\ell_2 = 170$ μm and R_T 35 Ω. The proposed analysis fits in the low part of the spectrum of amplification, while deviates for increasing frequency of operation where the synthetic-line model predicts with decreasing accuracy the behavior of the line-capacitor circuit. In particular, the gain of the CSSDA is in this case is more dependent upon Z_S than respect the case $Z_T = Z_S$ (8). In fact, this is formalized in (15) by the term D, which is

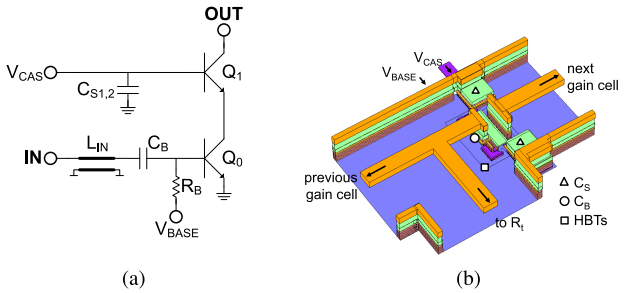

Fig. 19. (a) Schematic and (b) 3-D view of the designed gain cells.

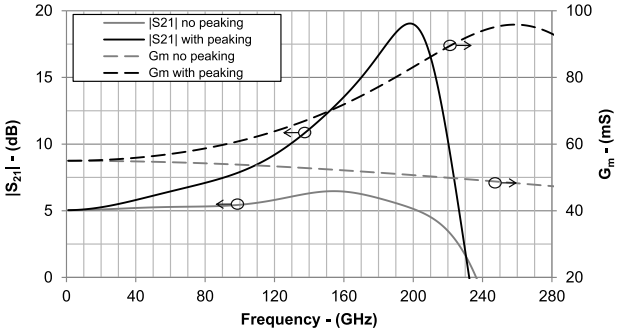

Fig. 20. Circuit simulation of the CSSDA gain peaking established with $\ell_{\rm IN}$ (Fig. 19). The result is compared against the case of no peaking for equal design parameters. The equivalent gain-cell transconductances G_m are also illustrated for both cases. G_m is calculated as the ration between the output short current of the cell divided the input voltage.

dependent on Z_S and elevated to the power of N. This terms reduces to 1 if $Z_T = Z_S$.

2) Peaking of the Gain Toward High Frequency: The gain of the CSSDA modules has been also peaked toward high frequency around 200 GHz. The aim is to further extend the bandwidth of operation of the system compensating the frequency-dependent synthetic-line losses. The peaking of the gain has been achieved with the line-segment $\ell_{\rm IN}$ placed at the input of the cell, as shown in Fig. 19. The length of this line is 15 μm, which is short compared to the signal wavelength, and can be replaced with an equivalent inductor of 6.3 pH. This value is calculated as the product between the line length and its inductance per unit-of-length. $\ell_{\rm IN}$ boosts the equivalent gain-cell transconductances G_m for increasing frequency, which results in peaking of the amplifier gain. In particular, the increase of cell transconductance with frequency has been designed to match the drop of the amplifier gain toward high frequency due to the losses. For the presented design, the required frequency slope was achieved peaking the transconductance of the gain element at 260 GHz. This technique was first introduced in [3] for a different gain-cell topology. The resulting peaking effect is shown in Fig. 20 against the case of no peaking, and also the G_m are reported for the two cases.

D. Design of Gain Cell

The design of the cell targeted a minimization of the input pole caused by $R_{\rm in}C_{\rm in}$ to pursue the highest frequency of operation. The schematic of the cell is in Fig. 19(a). The main contribution to $R_{\rm in}$ is the contact resistance between the

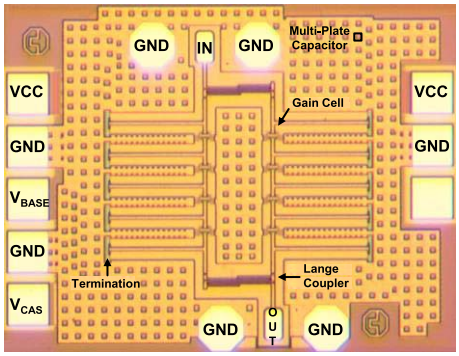

Fig. 21. Micro-photograph of the balanced CSSDA. The die area is 0.38 mm^2.

base terminal of the transistors and the transmission lines. To reduce it, the widest available HBTs from the model library have been used. The emitter area of the transistor Q_0 has been set to $10 \times 0.9 \times 0.07$ μm^2. This produced a minimal $R_{\rm in}$ of 6.7 Ω. In turn, the use of large emitter-area resulted in a large input capacity. $C_{\rm in}$ has been thus lowered by the capacitor C_b of 120 fF, as in [2]. Further minimization of $C_{\rm in}$ has been accomplished through the cascode topology of the cell, where the Miller effect over Q_0 is reduced respect than other configuration such as common emitter. As mentioned in Section IV-C.2, a line segment $\ell_{\rm IN}$ has been used to boost the cell equivalent transconductance by a $C_{\rm in}$ peaking. $\ell_{\rm IN}$ is 15 μm, and with the same line impedance Z_0 of the other lines used in the circuit. It boosted the cell-G_m from 55 mS at 1 GHz up to 95 mS at 260 GHz.

The dc paths between the cell are decoupled by C_b, while R_b of 25 kΩ biases the base current of Q_0. As shown in [2] and [3], C_b is embedded into the synthetic transmission lines and does not limit the operation of the amplifier toward lower frequencies, down to hundreds of megahertz for this technology and for this set of design values. However, for lower frequencies, it limits the cell transconductance and prevents any dc gain [3]. The bases of the transistor Q_1 are ac-grounded through capacitors $C_{S-1,2}$ of 150 fF. The 3-D view of the complete gain element is in Fig. 19(b). Full electromagnetic simulations have been performed to predict the parasitic affecting the performance of the final circuit layout, and, in particular, avoid positive feedback to ensure the amplifier stability. In addition, standard tests to investigate the system stability were performed, such as the impulse response, and the K-factor.

V. Measurement Results

The presented novel architecture has been tested with a circuit prototype fabricated in a 130-nm SiGe BiCMOS process with nominal $f_{\rm max}$ of 450 GHz, which is reduced to 370 GHz in the tolerance corner of the actual fabrication run. A picture of the fabricated hardware, with a total area of 0.38 mm^2, is shown in Fig. 21. All the measurements are acquired on-chip with bias $I_{\rm CC} = 121$ mA and $V_{\rm CC} = 3$ V. The parasitics associated to the pads have been taken in account and compensated in the design through electromagnetic simulations; it is thus not necessary to de-embedded them from the measurement results. A vector analyzer with converter

TABLE III
DESIGN PARAMETERS OF THE FABRICATED CIRCUIT

ℓ_1 [μm]	ℓ_2 [μm]	L [μH/m]	C [pF/m]	Z_0 [Ohm]
50	170	0.42	92.5	65
ℓ_{IN} [μm]	C_{in} [fF]	C_{out} [fF]	R_{in} [Ohm]	G_m [mS]
15	50	23	6.7	55

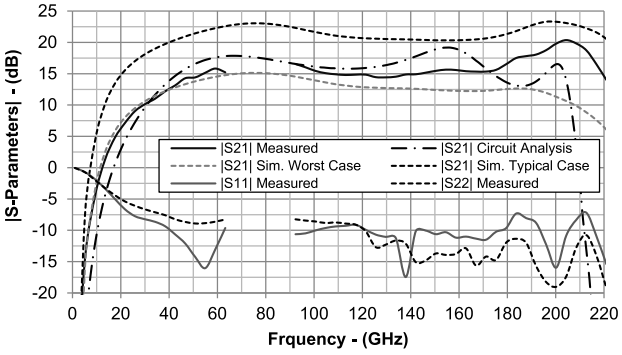

Fig. 22. Measured S-parameters and simulated $|S_{21}|$ for worst and typical process corner, and calculated as in (15).

modules is used to perform the S-parameter characterization of the ultra-wide spectrum of amplification in the following ranges: from 200 MHz to 67 GHz, from 90 to 140 GHz, and from 140 to 220 GHz. The gap in the experimental results between 67 and 90 GHz is due to the lack of available instrumentation for this band.

Fig. 22 shows the *S-parameter measurements*, and the simulated $|S_{21}|$ for the nominal $f_{\max}$ (450 GHz) and for the worst-case process corner (340 GHz). The gain is predicted well at low frequency by the worst-case process-corner model, while in proximity of 200 GHz the amplifier behaves within the gain region defined by the two models. The amplifier provides an average of 16-dB gain, with a peak value of 20 dB, while the frequencies where the gain drops by -3 dB from the average value are 45 and 220 GHz, which is the highest observable frequency with the available measurement equipment. Fig. 22 also shows the gain calculated using (15) with the design values provided Section IV-C, which are gathered in Table III, in conjunction with the simulated response of the couplers. The predicted absolute value and frequency behavior of the gain expressed as in (15) match the measurement results, validating the presented circuit analysis. Fig. 23 shows also the agreement between measured and simulated $|S_{11}|$ and $|S_{22}|$.

The *large-signal measurements* are presented in Figs. 24 and 25 as function of frequency in the range from 30 to 60 GHz and from 90 to 140 GHz. The measured input-referred 1-dB compression point (iP1dB) at 50 GHz is -16 dB, corresponding to an output-referred 1-dB compression point power (oP1dB) of -0.5 dBm. The measured iP1dB at 130 GHz is -10.5 dBm, corresponding to an output-referred 1-dB compression point power (oP1dB) of 4.5 dBm. The measured gain-compression curves for 180, 200, and 220 GHz are shown in Fig. 26. For these frequencies, the iP1dB cannot be reached due to the limited output power of the available equipment. Nevertheless, it is possible to appreciate a linear behavior of the device for up to an input

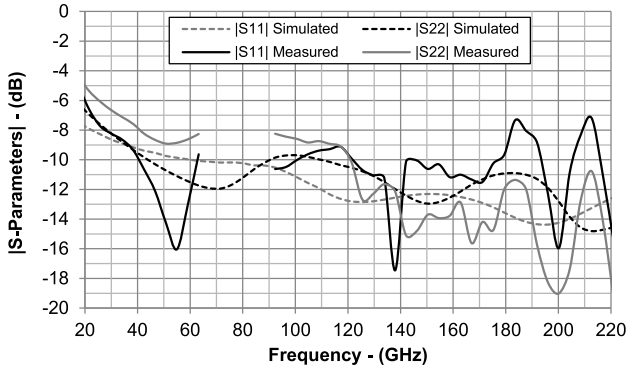

Fig. 23. Measured and simulated $|S_{11}|$ and $|S_{22}|$.

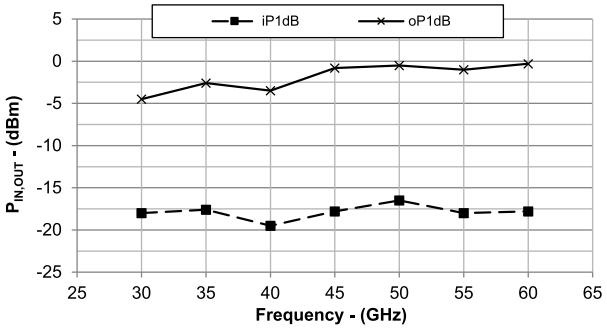

Fig. 24. Measured input and output power at 1-dB compression of the gain, for the frequency range 30–60 GHz.

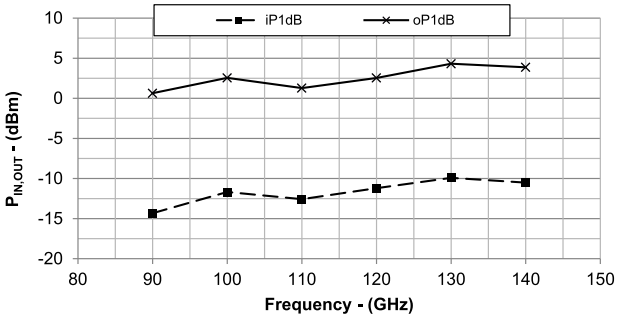

Fig. 25. Measured input and output power at 1-dB compression of the gain, for the frequency range 90–140 GHz.

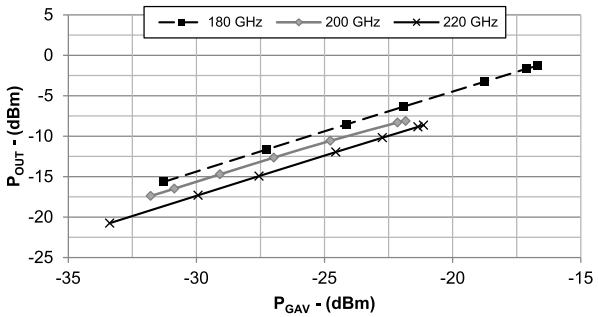

Fig. 26. Measured compression curves for 180, 200, and 220 GHz. P_{GAV} are the available power of the generator.

power of -16.5 dBm, corresponding to an output power of -1.28 dBm. The presented characterization of the amplifier linearity highlights how for increasing frequency of operation the oP1dB increases. This is due to the couplers, which for

TABLE IV
STATE OF THE ART OF CSSDAS

Ref.	GBP [GHz]	f_{LOW} [GHz]	f_{HIGH} [GHz]	BW [GHz]	Gain [dB]	Peaking [dB]	f_{max} [GHz]	oP1dB [mW]	P_{DC} [mW]	$\|S_{11}\|$, $\|S_{22}\|$ [dB]*	Area [mm^2]	Δtp/BW [ps/GHz]	NF [dB]	Technology
[16]	199	dc	25	25	9	6	n.a.	n.a.	60	-5, -5	0.36	50/30	n.a.	65 nm Si CMOS
[14]	260	25	65	65	16.5	3	n.a.	n.a.	333	-5, -5	1.31	n.a.	n.a.	150 nm GaAs pHEMT
[18]	312	dc	70	70	13	4	200	1	85	0, -2	0.78	75/70	n.a.	90 nm Si CMOS
[19]	900	dc	90	90	20	5	n.a.	1	90	-5, -5	0.31	80/100	n.a.	40 nm Si
[13]	759	80	250	170	13	0	450	n.a.	74	-4, 0	0.22	10/110	n.a.	130 nm SiGe
[12]	1514	2	240	240	16	2	650	n.a.	117	-5, 0	0.41	24/200	10†	250 nm InP
This Work	1102	45	220**	175**	16	4	370	4.5	360	-7.5, -11	0.38	20/200	9.5†	130 nm SiGe

*: Measured in the higher part of the spectrum of amplification, **: Limited by the available equipment, †: Minimum value.

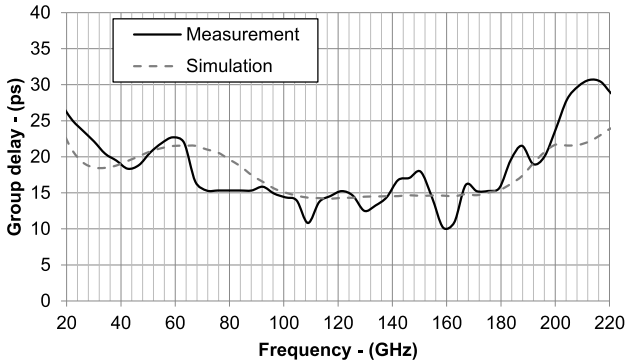

Fig. 27. Measured and simulated group delay over the frequency range from 20 to 220 GHz.

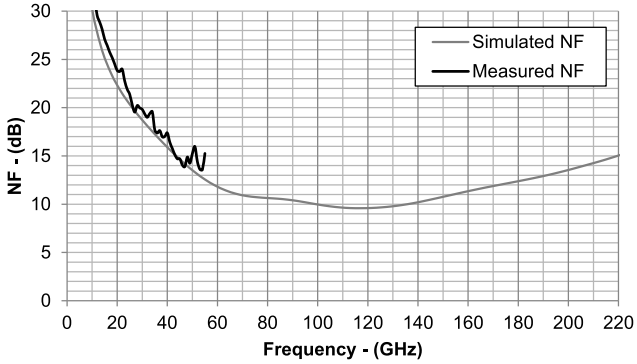

Fig. 28. Measured and simulated NF from 10 to 220 GHz.

raising frequencies feed more uniformly the input signal to the CSSDA modules making both of them contribute to the output power, as the amplitude balance shows in Fig. 15.

The *group-delays measurements* and simulations are presented in Fig. 27. The simulated group delay variation is below 10 ps in the frequency range from 20 to 220 GHz, while the measured group delay variation is below 20 ps in the same range.

The *noise figure (NF) measurements* and simulations are presented in Fig. 28. The available equipment allows characterization up 55 GHz. At this frequency, the NF is 14 dB in agreement with simulation. The simulated NF reaches the minimum value of 9.5 dB at 110 GHz.

VI. CONCLUSION

A novel amplifier topology is proposed to address shortcomings of CSSDAs with the use of two Lange couplers in balanced configuration. Experimentally demonstrated in a 130-nm SiGe BiCMOS process, the presented solution addresses the two main issues of CSSDA, i.e., poor output matching in the upper part of the frequency spectrum of amplification [11]–[13], and reduced input and output power at 1-dB compression. The claim is supported by extended circuit analysis and a detailed description of which inherent features of the circuit network cause the difficulties in the output matching design. Furthermore, the first compact and general analytic expression has been presented for the prediction of CSSDA gain versus the frequency of operation.

The prototype gain peaks at 20 dB, and its average in-band value is 16 dB. The frequencies where the gain drops by -3 dB from the average value are 45 (f_{LOW}) and 220 GHz (f_{HIGH}), which is the highest observable frequency with the available measurement equipment. Compared against the state-of-art gathered in Table IV, the circuit shows one of the largest reported gain-bandwidth product (GBP, where the bandwidth of the other devices is measured in the same manner for a fair comparison), the highest output-power in 1-dB compression, while still being functional above 200 GHz, and despite the lower f_{max} with respect to the fastest reported designs. The demonstrated group delay variations over frequency (Δtp/BW) is also one of the best reported so far for DAs, thus validating the usefulness of the peaking and balanced techniques for broad band applications requiring low phase dispersion. The balanced configuration enabled also the best input and output matching at f_{HIGH}, solving issue of poor matching at the highest end of the band typical in CSSDAs.

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