A Chopping Switched-Capacitor RF Receiver With Integrated Blocker Detection

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***Abstract*— A 0.1–0.6 GHz chopping switched-capacitor (SC) RF receiver (RX) with an integrated blocker detector features a tunable center frequency, a programmable filter order, and a high out-of-band (OB) linearity. RF impedance matching, high-order OB interferer filtering, and flicker-noise chopping are achieved with passive SC circuits only. The 34–80 mW 65-nm RX achieves 35-dB gain, +31 dBm OB-third-order input intercept point, +15 dBm B1dB, and 4.6–9 dB NF. The 0.2-mW integrated blocker detector detects large OB blockers with only 1-μs response time. The filter order can be adapted to blocker power with the blocker detector.**

***Index Terms*— Blocker detector, chopping, CMOS, cognitive radio, discrete time (DT), high linearity, IIR filter, *N*-path filter (NPF), software-defined radio, switched capacitor (SC), wideband receiver (RX).**

I. Introduction

OUT-OF-BAND (OB) linearity is a key challenge in the design of tunable RF receivers (RXs) for software-defined radios and cognitive radios. For RXs operating at a fixed RF frequency, OB interference can be attenuated with a high-Q passive filter, which relaxes the linearity requirement. Unfortunately, however, because most tunable RXs do not have wide-tuning high-Q pre-select filters, the impact of large close-by blockers saturates the RF front end and desensitizes the RX. Even if the interferer power is not high enough to block the desired signal, the intermodulation and cross modulation caused by the OB interferers can degrade the signal-to-noise ratio in frequency division duplexing or co-existence scenarios.

A number of techniques have been proposed to reduce OB linearity in RF RXs. For example, N-path filters (NPFs) [1], [2] and mixer-first RXs [3]–[6] achieve high continuous wave (CW) blocker tolerance, but offer only low-order filtering before the active baseband or RF circuits resulting in limited OB linearity for a close-by blocker. In [7], a passive switched-capacitor (SC) circuit is used for impedance matching and phase shifting in a beamforming RX, but it only provides first-order filtering similar to other mixer-first designs.

Manuscript received July 17, 2017; revised October 29, 2017; accepted February 11, 2018. Date of publication April 11, 2018; date of current version May 24, 2018. This paper was approved by Associate Editor Kenichi Okada. This work was supported in part by the Wei Family Foundation and in part by the DARPA CLASIC Program. *(Corresponding author: Yang Xu.)*

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Digital Object Identifier 10.1109/JSSC.2018.2808423

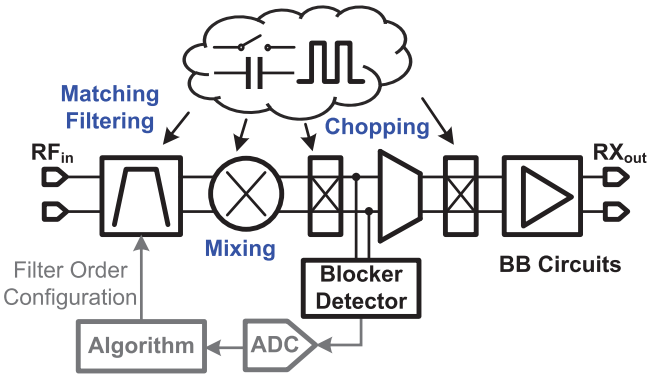

Fig. 1. Proposed chopping SC RF RX with blocker detection.

Self-Interference (SI) cancellation [8] reduces close-by transmitter SI for high cross-modulation linearity in co-existence applications, but the canceller limits power handling and has a limited bandwidth. An SCRX [9] uses SC circuits to realize high-order and high-linearity filtering to reduce the OB blockers. Unlike conventional discrete-time (DT) RXs [10]–[13] that filter out the blocker after the LNA and a mixer, an SC RX filters out the blocker before the active circuits resulting in high OB linearity even for a close-by blocker. The drawback of the SC RX is its relatively high noise figure (NF) and need for large-area baseband transconductors (Gms) to reduce RX in-channel flicker noise.

The proposed chopping SCRX with integrated blocker detector (see Fig. 1) achieves input impedance matching, programmable high-order filtering, and mixing similar to [9]. By placing linear, high-order SC filtering before the analog circuits, the RX demonstrates a high OB linearity. The RF SC front end has been modified to improve the noise performance. A chopping technique is merged into the SC circuits to reduce the Gm's size and flicker noise. We use inverter-based Gm cells to reduce the supply voltage and minimum-channel-length transistors to reduce Gm size. A blocker detector is integrated with the SCRX to detect the OB RF blocker envelope with a short response time before the blocker is propagated to the Gm cells. The filter order can be increased with a feedback loop when a large blocker is detected to make the filter order adapt to the blocker power.

The chopping SC RF RX is described in Section II. Section III describes the blocker detection. The front-end architecture and the circuit implementation are presented in Section IV. Measurement results are provided in Section V, and Section VI presents our conclusions.

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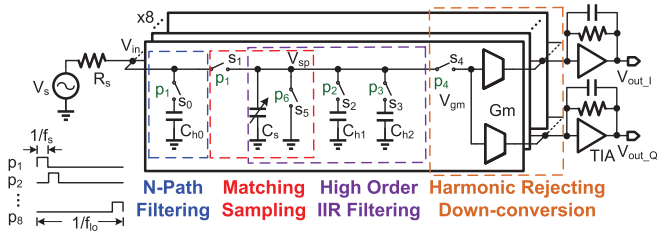


Fig. 2. Simplified architecture of the SCRX in [9].

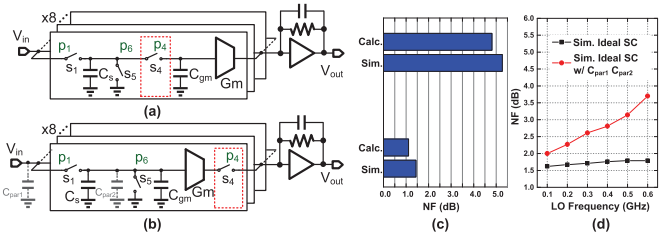


Fig. 3. (a) SC RF RX without filtering [9]. (b) Proposed approach to improve the NF by relocating output switch s_4 after the baseband Gm. (c) Calculated and behavioral-level simulated NF of both architectures. Gm noise is ignored. (d) Simulated NF versus LO frequency.

II. Chopping Switched-Capacitor RF Receiver Design

The linear, passive SC RF circuit located in front of the RX active baseband circuits provides high OB blocker tolerance, but the RX noise performance is limited by the switches. In this paper, we developed a modified SC RF RX to improve the noise performance. We incorporated the chopping technique into the modified SCRX to solve the flicker noise problem [14].

A. Conventional Switched-Capacitor Receiver

Fig. 2 shows the simplified architecture of a conventional SC RF RX with eight time-interleaved SC banks [9]. At the RF input, the NPF creates a bandpass input impedance to reduce the OB blocker, and the RF signal is sampled on C_s by s_1 with a sampling frequency of f_s. The input impedance matching is achieved by discharging the sampling capacitor C_s through switch s_5. C_s is tuned for different local oscillator (LO) frequencies to maintain the impedance matching [9]. The high-order passive DT IIR filter [15] further attenuates the OB blocker before it propagates to the baseband Gm input. Since the blocker tolerance for the SCRX is only limited by the supply voltage and higher order SC filtering provides large attenuation, rail-to-rail blocker tolerance can be achieved with an SCRX [9]. Each SC branch (e.g., C_{h1} with s_2) provides an additional order of filtering. Filter order programmability is realized by enabling and disabling the switches attached to the history capacitors C_{hi}. The Gm cells amplify the baseband signal, and their transconductances are scaled in different banks to achieve harmonic rejecting down-conversion as in a harmonic rejection mixer [16]. The desired signal is located at the RX LO frequency $f_{\text{LO}} = f_s/8$. The analysis of the SCRX is described in [9].

B. Improving Noise Performance of the Passive Switched-Capacitor RF Front End

Fig. 3(a) shows an SC RF RX without filtering. To achieve RF input impedance matching to an RF source with impedance R_s at a sampling frequency f_s, the capacitance of C_s needs to be $C_s \approx 0.63/f_s R_s$. The noise factor F of the passive SC RF circuit is then

$$F = 1 + \frac{R_{\text{ON},1}}{R_s} + \frac{1}{2R_s|G(f_s/8)|^2}\left[\frac{e^{-1/f_s R_s C_s}}{f_s C_s} + \frac{1}{\alpha_{\text{gm}} f_s C_s}\right] \tag{1}$$

where $R_{\text{ON},1}$ is the ON-resistance of switch s_1, $\alpha_{\text{gm}} = C_{\text{gm}}/(C_{\text{gm}} + C_s)$, and C_{gm} is the Gm input parasitic capacitance [9]; $G(f)$ is the equivalent continuous-time (CT) transfer function before the CT signal is sampled by the sampler (C_s with s_1 and s_5)

$$G(f) = \frac{1}{1 + jf/f_{rc}} \cdot [1 - e^{-2\pi(f_{rc}+jf)/f_s}] \tag{2}$$

with $f_{rc} = 1/(2\pi R_s C_s)$ [9]. Using the RF input matching condition, the noise factor can be simplified to $F = 1 + R_{\text{ON},1}/R_s + 0.27 + 1.23/\alpha_{\text{gm}}$. The second, third, and fourth terms in the noise factor formula are caused by switches s_1, s_5, and s_4, respectively. The noise from s_1 can be reduced using switches with smaller R_{ON}; the noise from s_5 is partially dumped by R_s when s_1 is turned ON; the noise from the IIR filter can be ignored [9], [15]; and the noise from Gm and other baseband circuits can be suppressed by using large transconductances. Noise from s_4 is much higher than s_1. For the noise from s_1, the high-frequency noise folding is reduced by the intrinsic low-pass transfer function of the SCRX [9]; however, for s_4, all the high-frequency noise components are folded into desired signal band due to the large equivalent low-pass filtering bandwidth ($1/R_{\text{ON}}C_s$) when sampling the s_4 noise. Output switch s_4 is the dominant noise source that limits the noise performance and should be removed to improve the noise factor.

Moving switch s_4 to the Gm output [see Fig. 3(b)] improves the SC RX's noise performance. The noise from s_4 is suppressed by the Gm as in a conventional passive mixer [17]. Ignoring the Gm noise, the noise factor of the modified SC RX is $F = 1 + R_{\text{ON},1}/R_s + 0.27$. Fig. 3(c) shows the calculated and behavioral-level simulated NF of the conventional and modified SC RXs for a 1-Ω switch R_{ON}. The Gm noise is ignored. By relocating s_4, the NF is improved by 3.8 dB with the theoretical lower limit of the NF at 1 dB. In real circuits, the NF will be higher than the lower limit due to non-idealities, such as the non-zero switch R_{ON}, clock non-ideality, and the parasitic capacitor especially at high LO frequency. Fig. 3(d) shows the simulated behavioral-level NF versus LO frequency with realistic circuit parameters. For a 10-Ω switch R_{ON}, the NF is 1.6 dB at low frequencies and increases slightly at high frequencies due to the finite slope of the non-overlapping clock. Adding the parasitic

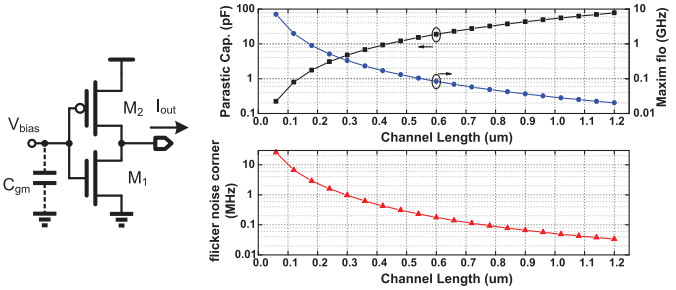


Fig. 4. Simulated Gm parasitic capacitance, flicker-noise corner, and maximum f_{LO} of the SCRX versus transistor length for a 100-mS inverter-based Gm in 65-nm CMOS.

capacitors at the RF input ($C_{par1} = 2$ pF[1]) and the sampling node ($C_{par2} = 3$ pF) to the model [see Fig. 3(a)], the NF is higher and increases even more at higher LO frequencies. Capacitor C_{par1} directly reduces the RF signal at high frequencies resulting in an increase in NF.

Taking into account the parasitic capacitance C_{par2} and C_{gm} [see Fig. 3(b)], the RX input impedance without an NPF at an LO frequency f_{LO} is $0.63/[(C_s + C_{par2} + C_{gm})f_{LO}]/8$. The presence of C_{par2} and C_{gm} results in a maximum LO frequency $F_{lo,max}$ when C_s is set to 0. If the LO frequency is higher than $F_{lo,max}$, the RX input resistance decreases, which reduces the RF signal and increases the NF. Reducing the parasitic capacitance C_{par2} improves the noise performance.

A drawback of the modified SCRX is that the Gm parasitic capacitor (C_{gm}) limits the frequency range even if other non-idealities are ignored. For the inverter-based Gm cell shown in Fig. 4, the transconductance gm is proportional to W/L, and C_{gm} is proportional to WL for a given process and bias condition [18]. Using transistors with smaller length in the Gm cell reduces C_{gm} while not changing gm. However, small-size Gm cells increase the flicker-noise corner of the RX, since flicker noise corner frequency f_c is proportional to gm/WL [18]. Fig. 4 shows the simulated Gm parasitic capacitance, the flicker-noise corner, and calculated maximum f_{LO} versus the transistor length, assuming the total Gm transconductance in one SC bank in the modified SCRX is 100 mS for both I and Q paths. We observe a tradeoff between maximum f_{LO} and flicker noise corner. To achieve 0.6-GHz maximum f_{LO}, the flicker noise corner is around 2 MHz, a value too high for a signal bandwidth of several MHz. It is therefore necessary to lower flicker noise while achieving high maximum f_{LO}.

C. Chopping Switched-Capacitor RF Receiver Architecture

To break the tradeoff between maximum f_{LO} and flicker-noise corner in the modified SCRX, we present an SC RF RX with chopping to remove the Gm flicker noise. Minimum-length transistors are used in the Gm cells to maximize the receive frequency range and reduce the Gm area.

The operation of our modified SCRX is shown in Fig. 5(a). The sampling rate of the eight time-interleaved SC banks

[1]RF input traces need to connect to 32 switches on the positive and negative sides, which results large parasitic capacitors.

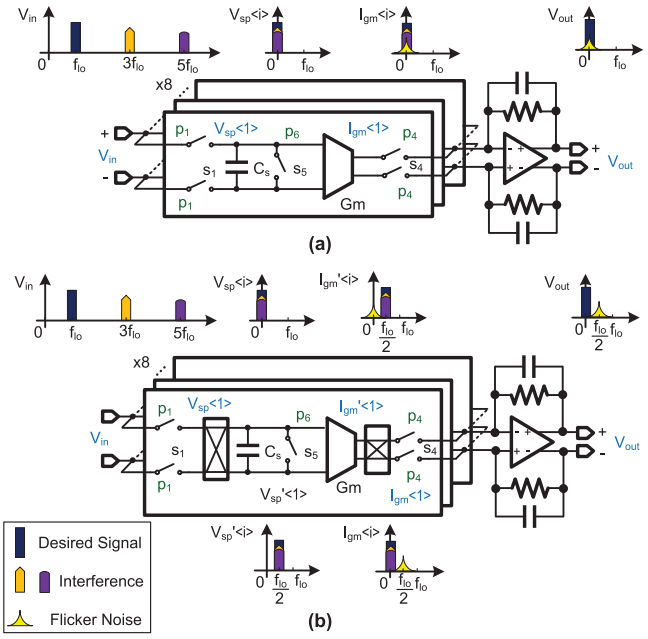


Fig. 5. (a) Modified differential SCRX with improved noise performance. (b) Proposed modified SCRX including chopping.

is f_s resulting in f_{LO} of $f_s/8$. For SC band #i, both the desired signal at f_{LO} and the interference at the LO harmonics (e.g., third and fifth LO harmonics) are down-converted to node $V_{sp}\langle i\rangle$. The Gm flicker noise is then added to the desired signal. The Gm output currents $I_{gm}\langle i\rangle$s for all SC banks are combined before being amplified by the transimpedance amplifier (TIA) with phase shift $i\pi/4$. Since the Gm cells are scaled as a sine wave as in a harmonic rejection mixer [16], the down-conversion from third- and fifth-order harmonics is rejected, and the flicker noise remains in the desired signal band.

By adding choppers before C_s and after Gm [see Fig. 5(b)], the desired signal is up-converted to the chopping frequency $f_{chop} = f_{LO}/2$, before it reaches the Gm input. The desired signal is down-converted back to baseband before all Gm currents are combined, while the Gm flicker noise is up-converted to the chopping frequency. In a classic chopping system, the chopper is typically placed before the Gm cells. In this design, the chopper is moved before C_s, since it can then be merged with the sampling switches to reduce the number of switches. Since C_s is symmetric and it is reset before the input voltage is sampled, moving the chopper before C_s does not have an impact to the whole RX system. The chopping is chosen to be $f_{LO}/2$ so that the chopper can be merged into the sampler easily. Also, this chopping frequency choice helps to reduce the spurious response due to chopping. Fig. 6(a) shows the chopping SC RF RX with high-order filtering. All switches are driven by eight-phase non-overlapping clock signals p'_1–p'_8. Choppers in series with the switches attached to C_{hi} are used to ensure that the IIR filter transfer function is maintained while chopping. The chopper and the SC circuits can be merged while replacing the clock signals

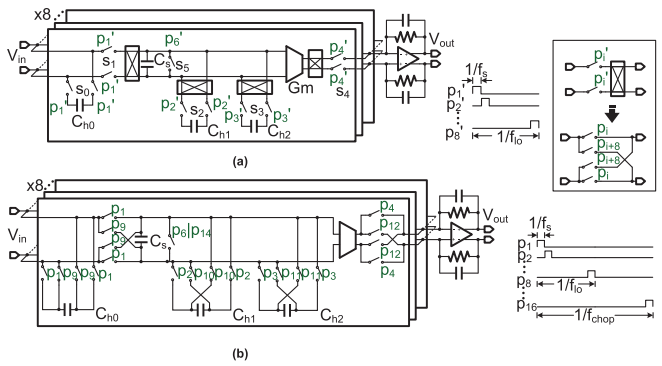


Fig. 6. (a) Architecture of the proposed chopping SC RF RX with high-order filtering. (b) Implementation with the chopper merged into the SC circuits.

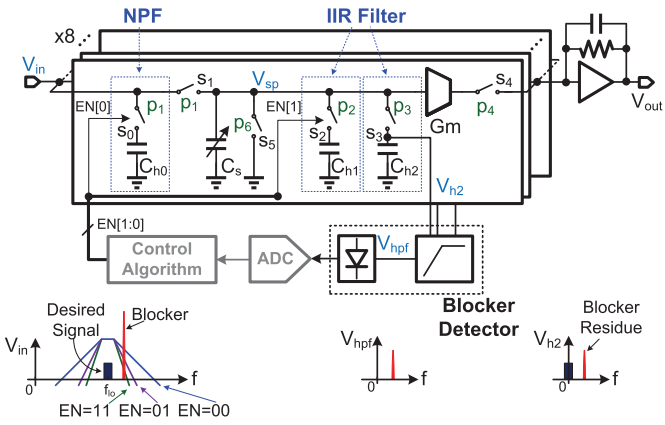


Fig. 7. Block diagram of the SC RF RX with an RF blocker power detector.

to a 16-phase non-overlapping clock p_1–p_{16} [see Fig. 6(b)]. Switches driven by p_i' and the attached chopper are replaced by two cross-coupled switch pairs driven by p_i and p_{i+8} so that $f_{\text{chop}} = f_s/16$. The 16 time intervals can be equally divided into two groups. The sampling polarity is changed every eight time interval. At the end of each eight time interval, C_s is reset, so the circuits between different choppers have no memory effect, resulting in a transfer function for the chopping RX that is identical to the transfer function of an RX without chopping. In addition, the noise source of each switch in our chopping RX is independent, with one switch pair turned ON in the chopper at each time interval. The noise performance from the SC RX's thermal noise with chopping and without chopping should be the same.

III. Programmable Blocker Filtering and Blocker Detection

The SCRX with programmable blocker filtering and blocker detection (see Fig. 7) is shown for simplification with the singled-ended SC RX driven eight-phase clock without chopping. The programmable filter is used to improve OB linearity. The SC circuits placed before the Gm cells have very high linearity with blocker tolerance limited only by supply voltage and transistor threshold voltage to achieve the rail-to-rail blocker tolerance [9]. However, for the SCRX without filtering [see Fig. 3(b)], OB linearity is limited by active Gm cells. By introducing high-order filtering into the SCRX, the OB blocker can be attenuated before it is amplified by the Gm. High-order filtering is achieved by the NPF (C_{h0} with s_0) at the RF input and the second-order IIR filter (C_{h1} with s_2 and C_{h2} with s_3) after sampling, with filtering occurring sequentially. For SC bank #1, the filter attenuates the OB interferer in p_1–p_3. Since the signal is propagated only to the TIA in p_4, during this time interval, OB blocker amplitude at Gm input is already attenuated to reduce the distortion generated by the analog circuits. While higher order filtering before Gm cells provides larger OB attenuation and better OB linearity, the high-order filter needs more clock power consumption to drive the SC filters. This power dissipation is unnecessary when OB interference does not exist or has lower power. The filter thus needs to be programmed to a lower order filtering mode with a lower OB interference level.

We incorporate an integrated blocker detection before the non-linear Gm cells so that the filter order can be tuned when a large blocker is detected. Since the blocker residue is available on the history capacitor C_{h2}, simple detector implementation can be achieved. In the SCRX (see Fig. 7), the last IIR filter is always turned ON as a default configuration. After s_3 is turned ON, C_s and C_{h2} have the same voltage, and C_s holds this voltage when s_4 is turned ON. V_{h2} is thus a replica of the voltage amplified by the Gm and holds the blocker residue after filtering. In the blocker detector, the high-pass filter attenuates the in-band signal, and the envelope detector detects the blocker residue to configure the filter order. Because C_{h2} is tens of pF, detecting the blocker at V_{h2} results in very low circuit overhead and performance penalty, so detector input capacitance can be ignored and does not affect the transfer function. If we try to detect the blocker directly at the Gm input node, the minimum capacitance at V_{sp} node will increase and limit the maximum f_{LO} as discussed in Section II. In addition, switches need to be added after the detector to ensure that only the voltage is amplified when s_4 is turned ON. If we detect the blocker at Gm output, a large ac coupling capacitor must be used, since the detector requires low input impedance due to the low TIA input impedance. This detector can detect blockers very quickly, but cannot tell if the blockers have disappeared. For the system design, the filter order should be increased when the detector output is high, but not decreased when the detector output is low. The filter order can be reset when the system is not receiving data.

IV. RF Receiver Circuit Implementation

A. RF Receiver Circuit Architecture

The architecture of the chopping SCRX prototype IC (see Fig. 8) consists of four SC banks, common-mode feedback (CMFB) circuits, a blocker detector, and a clock generator. Off-chip TIAs convert Gm output currents to voltages in I and Q paths. In each SC bank, the C_s pairs with sampling phases p_i and p_{i+4} share the same C_hs capacitance in the NPF and the IIR filters to reduce the dc and even-order LO harmonic response. The switches are implemented with CMOS transmission gates. The nMOS and pMOS in the switch have

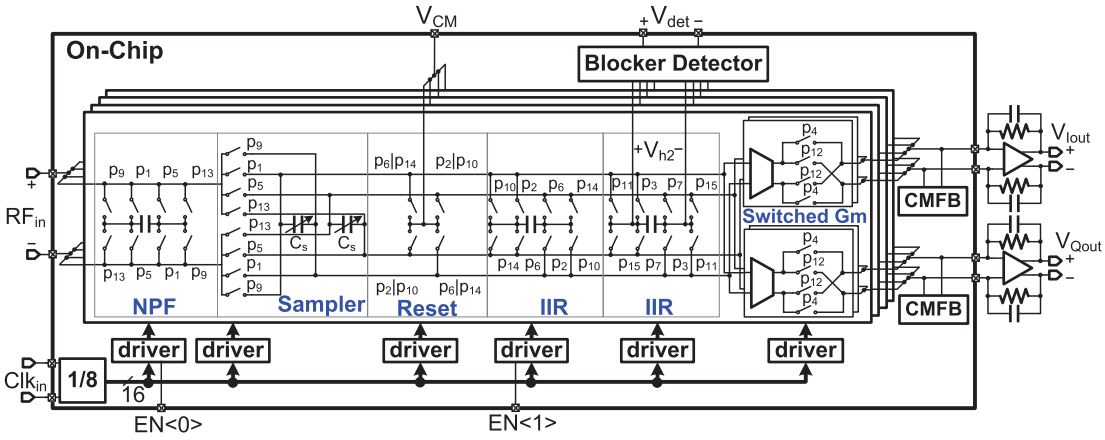


Fig. 8. Schematic of the chopping SC RF RX.

the same size $W/L = 100\ \mu$m/60 nm. The Gm cells generate I and Q baseband currents. The Gms push current only to the TIAs when the output switches are turned ON, which means that the Gms need to be activated only in 1/8 duty cycle in one period $16T_s$. The Gms are therefore powered down in inactive time intervals to save power, achieved by the switched Gm. The on-chip LO divider generates the 16-phase non-overlapping clock signals, with filter order configured by the clock drivers as in [9].

Harmonic rejection is implemented by scaling the Gms in I and Q paths as cosine and sine waves. The two main Gm factors used in the I and Q paths are $\text{gm}\cdot\cos(i\pi/4)$ and $\text{gm}\cdot\sin(i\pi/4)$ (factor #1) and $\text{gm}\cdot\cos(i\pi/4+\pi/8)$ and $\text{gm}\cdot\sin(i\pi/4+\pi/8)$ (factor #2) [19], where gm is the effective transconductance in the DT mixing [9] and i is the SC bank index. Total Gm transconductance in these two cases is 4.8gm and 5.2gm. Since the dc current is proportional to the transconductance, using factor #1 can save power consumption. However, because the switched Gm is used, total dc currents in the I and Q paths are not the same at different time intervals generating a ripple on the supply. Because of this effect, we use factor #2 with a 5:12 size ratio to approximate the $\sin(\pi/8):\sin(3\pi/8)$ ratio resulting in an effective gm of 114 mS. The harmonic rejection ratio (HRR) depends on the gain and phase mismatches [20] and can be improved using calibration [9], [21].

The gain of the RX can be derived as in [9]. The samplers are modeled as a CT transfer function G(f) and ideal samplers with choppers, and the switched Gm cells are modeled as DT mixers with chopping followed by reconstruction circuits to convert the DT signals back to the CT domain. The conversion gain is

$$\begin{aligned} CG(f_{\text{in}}) &= \frac{V_{\text{out}}(f_{\text{in}}-f_s/8)}{V_s(f_{\text{in}})} \\ &= G(f_{\text{in}})\cdot\frac{1}{T_s}\cdot\frac{1}{2}\text{gm}\cdot T_s\text{sinc}\left(\pi\frac{f_{\text{in}}-f_s/8}{f_s}\right) \\ &\quad\cdot R \approx \frac{1}{2}G(f_{\text{in}})\text{gm}R \end{aligned} \tag{3}$$

where f_{in} is the input RF frequency close to an LO frequency of $f_s/8$, gm is the equivalent Gm transconductance for DT mixing, and R is the feedback resistor in the TIA. The sinc function approximates to 1 for f_{in} close to $f_s/8$. The noise factor of the RX is

$$\begin{aligned} F &= 1+\frac{R_{\text{ON},1}}{R_s}+\frac{1}{|G(f_s/8)|^2} \\ &\quad\cdot\left\{\frac{e^{-1/f_sR_sC_s}}{2f_sR_sC_s}+\frac{1}{\text{gm}R_s}\left[\gamma\left[\sin(\pi/8)+\sin(3\pi/8)\right]\right.\right. \\ &\quad\left.\left.+\frac{2\gamma\,\text{gm}_{\text{CMFB}}}{\text{gm}}+\frac{2}{\text{gm}R}+\frac{\overline{V_{n,op}^2}(1+R/R_{o,\text{gm}})^2}{2kT\text{gm}R^2}\right]\right\} \end{aligned} \tag{4}$$

where G(f) is the sampler gain shown in (2), gm_{CMFB} is the transconductance of the CMFB circuit, $\overline{V_{n,op}^2}$ is the input-referred voltage noise source of the op-amp in the TIA, and $R_{o,\text{gm}}$ is the Gm output resistance. In a transistor-level circuit, the parasitic capacitance at the RF input (C_{par1} in Fig. 3) decreases the imaginary part of the input admittance and reduces the sampler gain at high frequencies. The parasitic capacitance in parallel with C_s (C_{par2} in Fig. 3) decreases the real part of the input admittance for high LO frequencies and reduces the signal gain. In addition, the non-ideal non-overlapping clock with finite rise and fall time reduces the switch turn-on time in the sampling phase at higher LO frequency, which also reduces the sampler gain. NF thus increases with LO frequency in a transistor-level circuit due to reduction in $G(f)$ in (4). Using a more scaled process with lower parasitic capacitance and a better clock generator improves the NF at high LO frequencies. When the NPF is enabled, the NF will be higher due to NPF loss. The Gm-TIA circuit is also a significant noise source in the chopping SCRX. The NF can be improved with larger gm value in (4). The finite gm output resistance increases the noise contribution of the TIA op-amp. To reduce the parasitic capacitance, the transistor channel length is minimized as described in Section II-B. The output resistance of a 100-mS Gm with a minimum-channel-length transistor is only several hundred ohms. To improve this value, we use a negative Gm at the Gm output (described in Section IV-B). The option of increasing the channel length to improve the Gm output resistance would result in such a

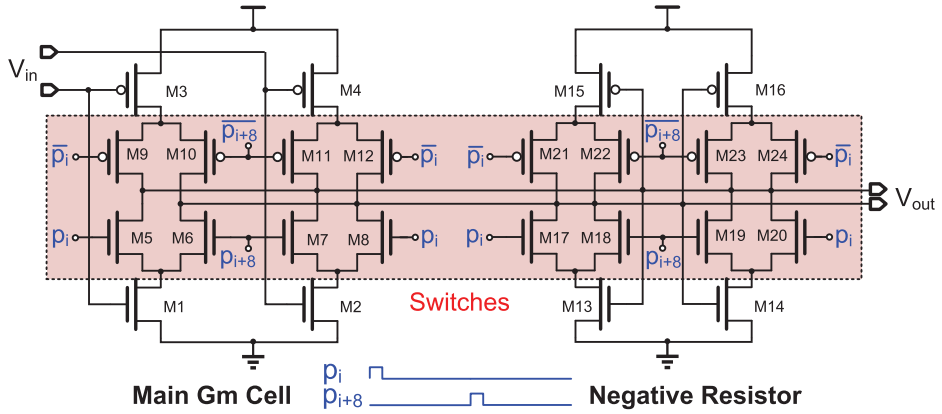


Fig. 9. Schematic of the baseband switched Gm cell.

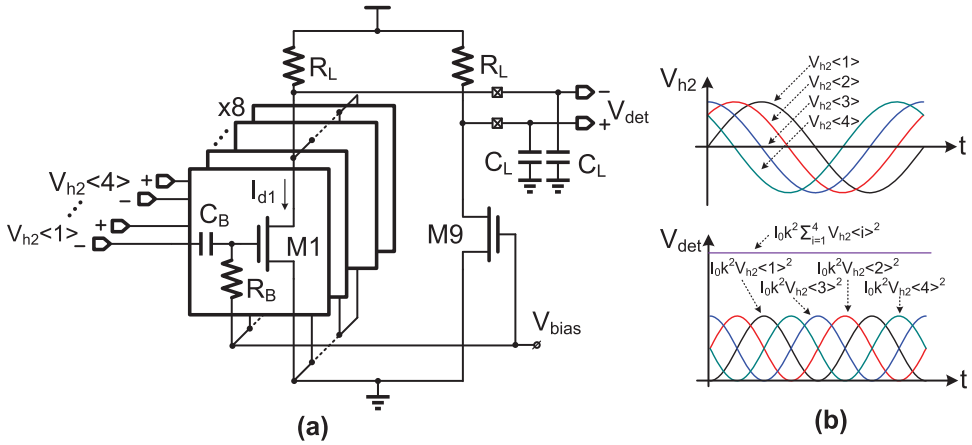


Fig. 10. (a) Schematic of the blocker detector. (b) Input and output waveforms of the blocker detector.

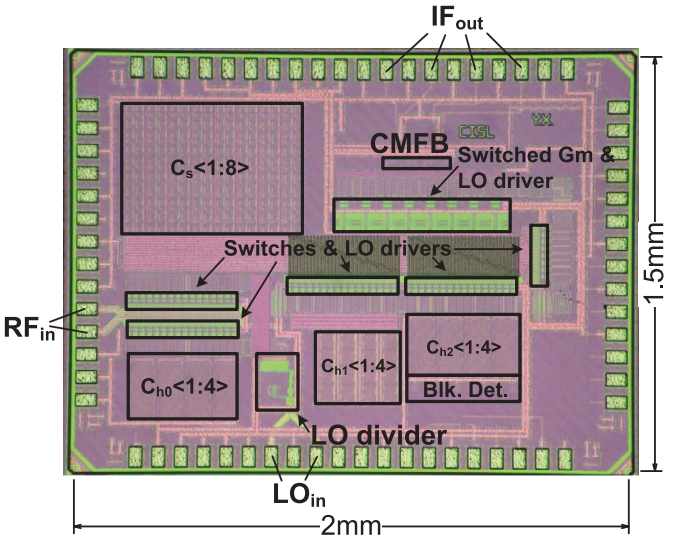


Fig. 11. Chip photograph.

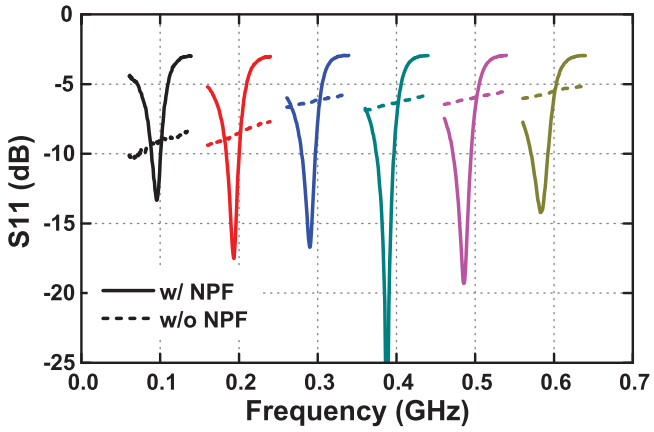
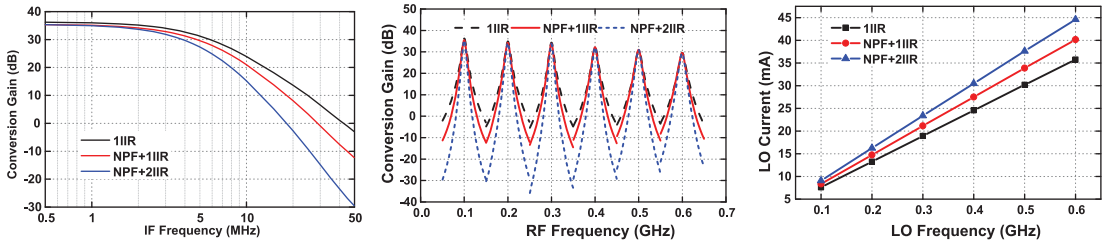


Fig. 12. Measured differential-mode S_{11} for LO frequencies ranging from 0.1 to 0.6 GHz with a 0.1 G-Hz step with and without the NPF.

large increase in the parasitic input capacitance that it would have a worse effect on the noise performance.

B. Baseband Circuit

Circuit implementation of the switched Gm (see Fig. 9) consists of a main Gm cell and a negative resistor. The input common-mode voltage is set to V_{CM} in reset phase (see Fig. 8), and the output common-mode voltage is set by the CMFB circuit as in [22]. Inverter-based design [23] is adopted to improve power efficiency. In the main Gm cell, transistors M1–M4 provide transconductance, and the nMOS and pMOS are sized to achieve the same transconductance. Transistors M5–M12 are the switches that propagate the Gm output current to the TIA and achieve the chopping. For the



(a) (b) (c)

Fig. 13. (a) Measured conversion gain $V_{I\text{out}}/V_{\text{RF}}$ versus IF frequency for a 0.1-GHz LO. Measured (b) conversion gain and (c) LO current versus RF frequency for LO frequencies ranging from 0.1 to 0.6 GHz with a 0.1-GHz step and for different filter configurations.

size-5 Gm cell, M1 and M2 are 40 μm/60 nm; M3 and M4 are 96 μm/60 nm; and M5–M12 are 32 μm/60 nm. The dc current of the Gm is cut down when the switches are OFF to save power [24]. The minimum-length transistors with low output impedance used in the main Gm cell increase the noise contribution of the TIA op-amp. A negative resistor [6] is adopted at the Gm output node to increase output impedance. Transistors M13–M16 generate negative resistance, and M17–M24 cut off the dc current as in the main Gm cell. For the size-5 Gm cell, M13 and M14 are 2.5 μm/120 nm; M15 and M16 are 6 μm/120 nm; and M17–M24 are 8 μm/60 nm. All transistors in the switched Gm use minimum length thanks to the chopping technique. In the same way as we saw with the switches, the Gm area is scaled with the CMOS process. Compared with switch-Gm in [24], transistors M1–M4 and M13–M16 work in saturation region when the switches are ON, and work in inversion mode when the switches are OFF to avoid build-up time of the inversion layer while the switches are turned ON as well as to avoid the parametric loss at Gm input [25]. If M1–M4 work in depletion mode when the switches are turned OFF, a parametric loss of $(C_s + C_{\text{gm,dep}})/(C_s + C_{\text{gm,sat}})$ is generated when the switches are turned ON, where $C_{\text{gm,dep}}$ is the Gm input capacitance in depletion mode and $C_{\text{gm,sat}}$ is the Gm input capacitance in saturation region, $C_{\text{gm,dep}} < C_{\text{gm,sat}}$.

The transistor-level simulated conversion gain of the SCRX without the NPF is 36.3 dB, which matches the calculated 37.4-dB conversion gain. The simulated NF of the behavioral-level RX with only SC noise without the NPF is 1.6 dB with 10-Ω switches R_{ON}, which does not change with LO frequency [see Fig. 14(b)]. With parasitic capacitance at RF input and clock non-idealities, NF increases with LO frequency. The simulated NF of the transistor-level RX with parasitics and clock non-idealities is 3.9 dB for a 0.1-GHz LO with an increase to 8.5 dB when LO is 0.6 GHz. Compared with the NF with and without noise from the Gm-TIA circuit, we find Gm-TIA to be the main noise source.

C. Blocker Detection Circuit

The blocker detector [see Fig. 10(a)] consists of eight ac-coupled common-source transistors with resistor and off-chip capacitor loads and a replica. The 55-Ω R_B and 1.3-pF C_B compose a high-pass filter to attenuate the in-band signal. All the transistors work in weak inversion mode. The output current of each transistor is $I_d = I_0 \cdot \exp(kV_{\text{gs}})$ [26]. For history capacitor voltage $V_{h2}\langle i\rangle$, output current is $I_0[\exp(kV_{h2}\langle i\rangle) + \exp(-kV_{h2}\langle i\rangle)] \approx 2I_0 + I_0k^2V_{h2}\langle i\rangle^2$. Since each $V_{h2}\langle i\rangle$ has a phase shift of $i\pi/4$ and the output current of the replica is $8I_0$, the detector output voltage is

$$V_{\text{det}} = I_0k^2\sum_{i=1}^{4}\left[V_{h2,pk}\cos(\omega_{\text{IF}}t + i\pi/4)\right]^2 = 2I_0k^2V_{h2,pk}^2 \quad (5)$$

[see Fig. 10(b)] with the blocker detector detecting the envelope of the intermediate frequency (IF) blocker signal. The load resistor R_L is 15 kΩ, and the load capacitor C_L is 10 pF to achieve a small settling time.

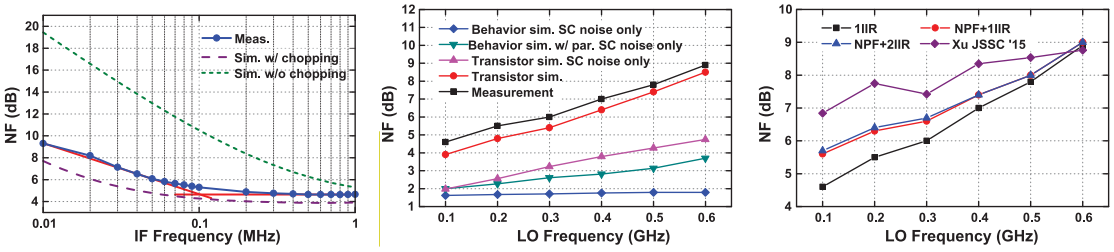
V. Measurement Results

Our chip prototype was fabricated in a 65-nm CMOS process with an active area of 1.63 mm^2 (see Fig. 11). The supply voltage of the baseband circuit is 1.1 and 1.25 V for the LO circuits.

Fig. 12 shows measured differential input reflection coefficient s_{11}. The RX achieves a wideband impedance matching without the NPF as in [9]. Without the NPF, the input impedance matching is mainly limited by the parasitic capacitance. The parasitic capacitor at the RF input decreases the imaginary part of Y_{in}. Also, the parasitic capacitor in parallel with C_s decreases the real part of Y_{in} at high LO frequencies. With the NPF, the OB S_{11} is higher due to low NPF OB impedance, and the deviation of S_{11} center frequency and LO frequency is caused by RF input parasitic capacitance [2]. For the remainder of the measurements, an off-chip 180° hybrid drives the differential RF input, and the loss of the hybrid is calibrated out. The measured LO leakage to the RF input is less than -58 dBm across LO frequencies when all the filters are enabled.

The conversion gain $V_{I\text{out}}/(V_s/2)$ with different filter configurations is measured for an LO frequency of 0.1 GHz in Fig. 13(a). Fig. 13(b) and (c) shows the measured conversion gain and LO current for LO frequencies from 0.1 to 0.6 GHz for different filter orders. The conversion gain is lower for higher LO frequencies due to the parasitic capacitance and clock non-idealities. The OB attenuation and LO current increase with higher filter order.

The measured and simulated NF versus IF frequencies with 0.1-GHz LO and the first-order IIR filter are shown in Fig. 14(a). The measured flicker noise corner is 100 kHz



(a) (b) (c)

Fig. 14. (a) Measured and simulated NF versus IF frequency for an LO frequency of 0.1 GHz with the first-order IIR filtering. (b) Measured and simulated NF versus LO frequency for the RX with the first-order IIR filter. (c) Measured NF across LO frequency compared with the earlier SCRX.

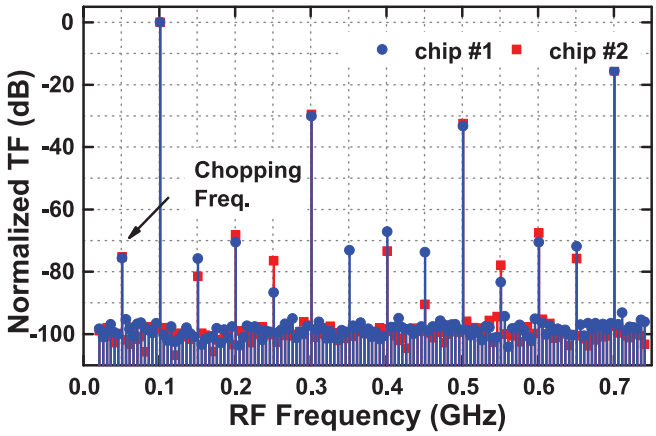


Fig. 15. Measured wideband transfer function for an LO frequency of 0.1 GHz.

with chopping, while the simulated flicker noise corner without chopping is significantly higher. The simulated and measured NF versus LO frequency is shown in Fig. 14(b) and (c). The noise degradation compared with the ideal circuit is discussed in Section IV-B. The NF for a 0.1-GHz LO with the first-order IIR filter is 4.6 dB, which is 2.2 dB better compared with the earlier SCRX [9]. With the NPF, the NF is higher due to NPF loss. The NF increases with LO frequency due to RF input parasitic capacitance and clock non-idealities.

The measured wideband transfer function for a 0.1-GHz LO is shown in Fig. 15. The HRR for the third-order LO harmonics is 30 dB and for the fifth-order LO harmonics is 33 dB with one-stage harmonic rejection. If better HRR is needed, the calibration method of [9] and [21] can be applied. The HRR for the seventh-order LO harmonics is 15.5 dB similar to other eight-phase harmonic rejection RXs [20]. The chopping frequency for a 0.1-GHz RX is 50 MHz. The spurious responses due to chopping are lower than -70 dB and are not higher than the responses from LO even-order harmonics. Thus, the noise impact due to chopping can be ignored.

Fig. 16(a) shows the measured blocker 1-dB compression point (B1dB) versus blocker frequency for a 0.2-GHz LO. As expected, the B1dB for a close-by blocker increases with filter order. When all filters are enabled, the B1dB for a 30-MHz blocker offset is 13 dBm, and the maximum B1dB is larger than 15 dBm (3.6 V_{pp} if referred to a 50-Ω resistor).[2] The OB-third-order input intercept point (IIP3) [see Fig. 16(b)] is measured with a two-tone signal at 0.231 and 0.261 GHz for a 0.2-GHz LO. When all filters are turned ON, the OB-IIP3 is 31 dBm. The triple beat (TB) [see Fig. 16(c)] for a 0.2-GHz LO versus SI peak power is measured with a -30 dBm adjacent-channel jammer and two-tone SI signals with a frequency offset as small as -30 MHz and a 5-MHz frequency spacing. The TB for a -4 dBm SI peak power is 62.5 dB with the highest order filtering, and the RX can handle larger than 10-dBm SI peak power. The high-order filtering improves B1dB, OB-IIP3, and TB compared with the first-order IIR filter. With the NPF and the second-order IIR filters, B1dB for a 30-MHz blocker offset is improved by 12.8 dB, OB-IIP3 is improved by 13 dB, and TB for a -4 dBm SI peak power is improved by 26.5 dB. Fig. 16(d) shows the measured B1dB, OB-IIP3, and OB-IIP2 (two tone: $f_1 = f_{LO} + 60$ MHz and $f_2 = f_{LO} + 61$ MHz) for LO frequencies stepped between 0.1 and 0.6 GHz. In an frequency- division duplex (FDD) or co-existence application, the filter order can be tuned with SI power level information available in the same device.

We measured the blocker NF for 0.1-GHz LO frequency and a blocker at 30-MHz frequency offset with the NPF and the second-order IIR filter (see Fig. 17). The NF matches the simulation result with an LO phase noise of -150 dBc/Hz at 30-MHz offset for a 1/16-duty-cycle LO. The simulated blocker NF without LO phase noise does not change with blocker power, since the CMOS switch R_{ON} almost does not change when the blocker swing increases [9]. We find that reciprocal mixing mainly increases the blocker NF. In the future work, this can be further improved using a better clock generator. Compared with other blocker-tolerant RXs, our RX achieves a better blocker NF for a large blocker (5 dBm) thanks to its low gain compression.

For an unknown CW OB blocker, the blocker detector can be used to adapt the filter order to the blocker power between two communication packets. Fig. 18 shows the filter adaptation using the integrated blocker detector. The Gm input-referred blocker power [see Fig. 18(a)] is the blocker power level at the input of the (non-linear) Gm and is calculated by subtracting the normalized measured RF filtering

[2] B1dB saturates to 15 dBm due to finite supply voltage [9].

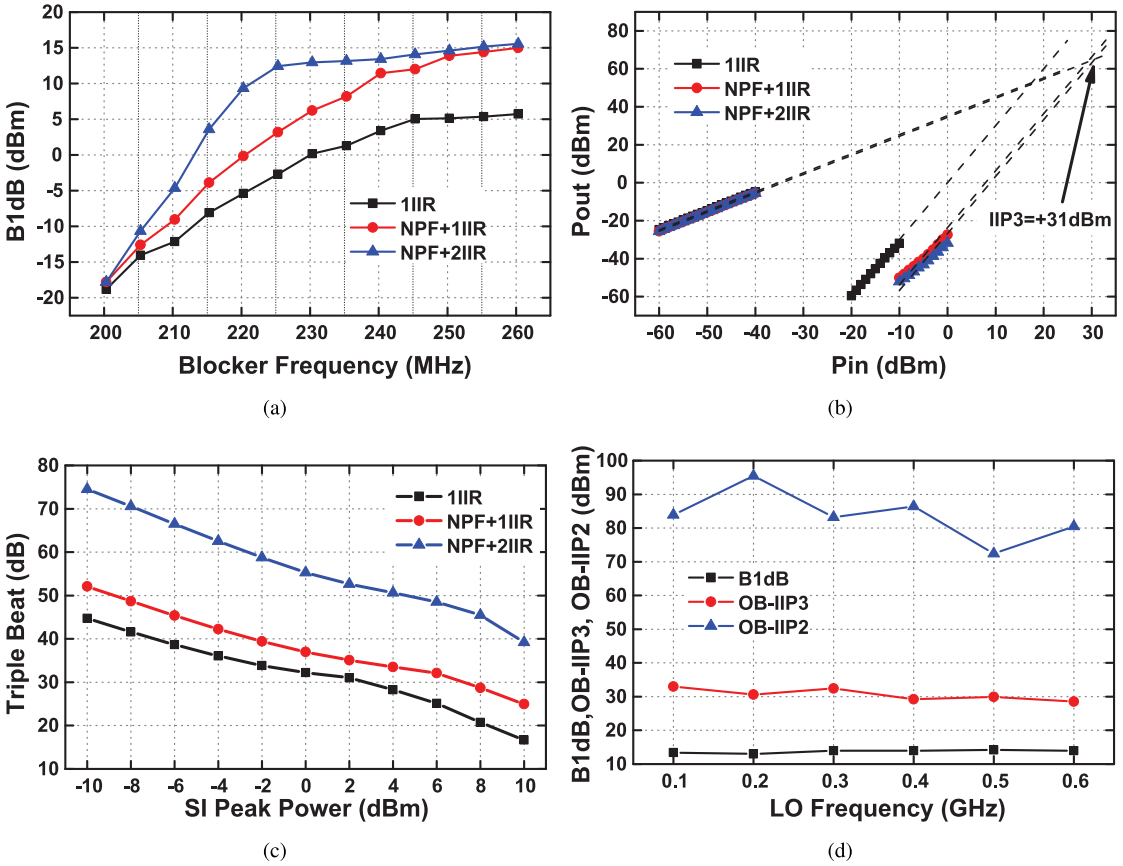


Fig. 16. Measured (a) blocker 1-dB compression point versus blocker frequency, (b) OB IIP3, and (c) TB versus two-tone SI peak power for an LO frequency of 0.2 GHz with different filter configurations. (d) Measured B1dB, OB-IIP3, and OB-IIP2 for LO frequencies stepped between 0.1 and 0.6 GHz.

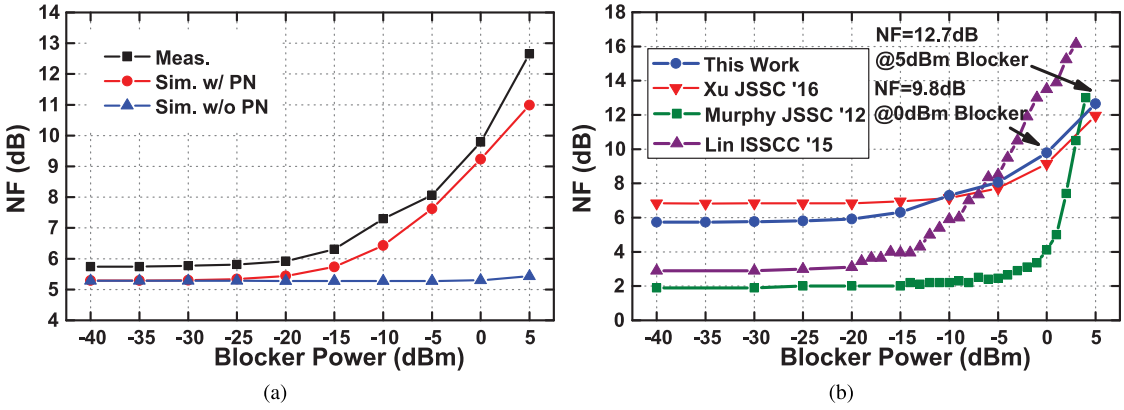


Fig. 17. (a) Measured and simulated blocker noise with blocker at 30 MHz for a 0.1-GHz LO. (b) Measured blocker NF compared with other blocker-tolerant RXs.

transfer function from the applied blocker input power. The detector output voltage is a linear function of the Gm input-referred blocker power. Fig. 18 shows the measured conversion versus blocker power with adaptive filter order for a 0.2-GHz LO and 30-MHz blocker offset. The detector output voltage increases with blocker power; when the voltage is higher than a threshold (50 mV), the filter order is increased and improves gain compression. The blocker detector transient response [see Fig. 18(c)] settles at less than 1 μs; after increasing the filter order, V_{det} stabilizes again in 1 μs. The detector consumes only 0.2 mW (including 0.1 mW from bias circuits).

When compared with the state of the art (see Table I), our RX achieves the highest OB spurious-free dynamic range [27]. The NF and the power consumption are better than in [9], and our RX supports fast blocker detection. For FDD and the coexistence application, compared with an SI cancellation method, our RX provides similar TB performance

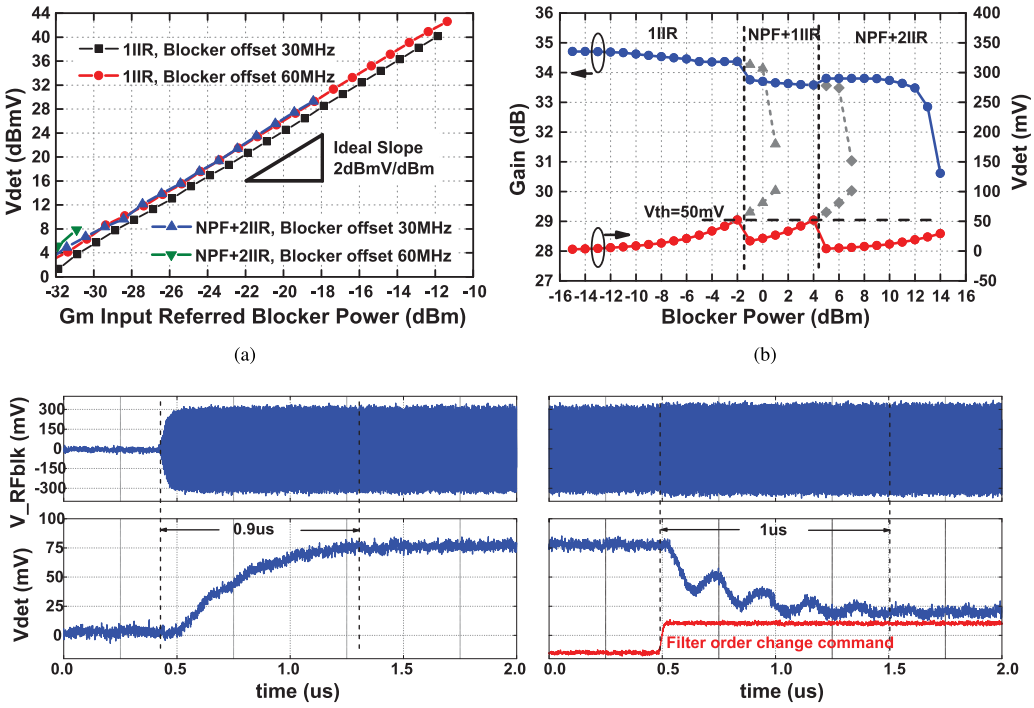


Fig. 18. (a) Measured blocker-detector output voltage versus Gm input-referred blocker power for different filter orders and blocker offset frequencies. (b) Measured conversion gain versus blocker power with adaptive filter order for a 0.2-GHz LO and a 30-MHz blocker offset. (c) Blocker-detector transient response.

TABLE I

COMPARISON WITH THE STATE OF THE ART

	This work	Xu JSSC '16	Murphy JSSC '12	Zhou ISSCC '15	Darvishi JSSC '13	Lin ISSCC '15
Technology	65nm	40nm	40nm	65nm	65nm	
Architecture	Chop. SC	SC	FTNC	SI Canc.	NPF	Mixer-first
Blocker detector	Yes	No	No	No	No	No
RF freq. (GHz)	0.1-0.6	0.1-0.7	0.08-2.7	0.8-1.4	0.1-1.2	0.1-1.5
NF (dB)	4.6-9	6.8-9.7	1.5-2.4[a] 3.5-5	4.8, 5.3[b]	2.8	1.5-2.9
OB-IIP3 (dBm)	**31**	24	13[a], 17	17	26	13
B1dB (dBm)	**15**	15	<0[a], <5	4	7	13.5
TB_{-4dBm}[c](dB)	**63**	NR	NR	48, 64[b]	NR	NR
Max Handled Peak SI Power (dBm)	**>10**	NR	NR	NR, -4[b]	NR	NR
OB-SFDR[d] (dB)	**92.9**	87.5	83.7[a], 85	84.1	91.5	83.7
Power (mW)	Ana: 24 LO: 9.5-55.8 Detector: 0.2	Ana: 52 LO: 7-53	35-78	63-69, 107-160[b]	18-57.4	11

NR = not reported; a: with noise cancellation b: with self interference cancellation, calibration is required c: Triple beat at a -4dBm SI peak power d: OB-SFDR = 2/3(OB_IIP3-(-174dBm/Hz)-10log (1MHz)-NF)

and has larger power handling. The NF increases at higher LO frequencies, which is limited by parasitic capacitance. This limitation can be improved with process scaling.

VI. CONCLUSION

We propose a chopping SC RF RX with high OB linearity to improve OB interference tolerance. We show that a highly linear passive SC RF circuit placed before non-linear baseband Gm cells provides high-order filtering and improves OB linearity. By using the chopping, a key noise source in the earlier SC RF RX is eliminated, and the NF is improved. Our blocker detector detects blocker residue on the history capacitor before the Gm cells and does not affect the RX performance and makes it possible for the filter order to adapt quickly to blocker power. These techniques provide a more efficient way to make tunable RXs survive the serious limiting effects of OB interference.

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