

100 Gb/s Differential Linear TIAs With Less Than 10 pA/ $\sqrt{\text{Hz}}$ in 130-nm SiGe:C BiCMOS

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Abstract—The design methodology and circuit implementation of a transimpedance (TI) amplifier (TIA) featuring low averaged input-referred current noise density without compromising the TIA bandwidth (BW) are presented. The technology role in the key performance metrics is also discussed and verified by means of two analogous TIA designs implemented in two different 130-nm SiGe:C BiCMOS processes from IHP, SG13S with $f_T/f_{\max} = 250/340$ GHz and SG13G2 with $f_T/f_{\max} = 300/500$ GHz. Both TIAs adopt a fully differential linear architecture with three stages: an input shunt-feedback TI stage followed by a variable gain amplifier which provides post-amplification with 15-dB gain control range and an output $50\text{-}\Omega$ buffer. The TIA in SG13S features 68.5 dBΩ differential TI gain, 42-GHz 3-dB BW, and 8 pA/ $\sqrt{\text{Hz}}$ averaged input-referred current noise density while the second TIA in SG13G2 provides 65 dBΩ differential TI gain, 66-GHz 3-dB BW, and 7.6 pA/ $\sqrt{\text{Hz}}$. Measured total harmonic distortion in both TIAs in the maximum gain condition is better than 5% for ~ 800 mVppd output swing and input currents of ~ 300 μA pp. Both circuits dissipate 150 mW of power and are shown to operate at up to 100 Gb/s data rate with clean PRBS31 non-return to zero and PAM-4 eye diagrams. To the author's best knowledge, the reported TIAs exhibit the lowest averaged input-referred current noise density shown to date at a BW sufficient to support 100 Gb/s net data rate, surpassing other silicon-based and InP implementations toward the next-generation 400 Gb/s optical links.

Index Terms—100 Gb/s, 400 Gb/s, BiCMOS, low noise, optical receiver, PAM-4, SiGe:C HBT, TIA.

I. INTRODUCTION

DIVEN by bandwidth (BW)-hungry applications such as high-definition TV, internet video, and cloud-enabled services, data-center communication is an unfolding market. With global IP traffic forecast to grow at a compounded rate of 23% per month, reaching the 2-ZB threshold by 2019 [1], an ever-larger underlying transport capacity will be needed,

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rapidly surpassing the current 100 Gb/s standard, only in commercial deployment since 2009 with the standardization of 400 Gb/s and 1 Tb/s systems already underway [2]–[5]. Such increase in capacity cannot be sustainably accommodated by successively multiplexing lower speed carriers on different wavelengths (i.e., four lanes \times 25 Gb/s) limited by power dissipation, form factor, and system complexity. The 400 Gb/s links will require a minimum speed of 100 Gb/s/lane to convey economically feasible products. Next-generation transceivers must, therefore, resort to alternative dimensions to increase data throughput, namely, the use of high-order modulation formats and/or the increase in the baud rate. High-order modulation formats provide higher spectral efficiency, but are more susceptible to noise and non-linearities, featuring low optical signal-to-noise ratio (OSNR) tolerance. On the other hand, higher baud rates relax the degradation in OSNR, but must resort to innovative circuit-level techniques and further advancements in high-speed electronics in order to increase the analog BW. Both directions bring new design challenges to the receiver front end, urging the development of new architectures featuring millimeter-wave BWs, high linearity, and low noise.

While communication inside data-center resorts mainly to intensity-modulation direct-detection formats due to their relative system-level simplicity [4]–[6], in longer distance links such as communication between data centers or long haul, coherent detection techniques are preferred for overcoming the imperfections of the optical fiber [7]. A generic block diagram of a single branch of such a coherent receiver is shown in Fig. 1. It makes use of two balanced photodetectors (PDs), which perform the optical to electrical transformation, after which a fully differential linear transimpedance (TI) amplifier (TIA) amplifies the weak current produced by the PDs and converts it to the voltage domain. The TIA is usually followed by a variable gain amplifier (VGA), as a part of an automatic gain control loop, which further amplifies the signal to ensure reliable operation of the clock and data recovery (CDR) circuits. After the CDR, a demultiplexer generates the low-speed data streams for the digital logic. The TIA, as the front-end device, is a critical building block in the receiver, typically limiting the overall system performance. In particular, the sensitivity of the TIA will determine the power level at which the channel needs to operate (i.e., the tolerable channel loss), and thus, the development of a high-sensitivity TIA is the key to creating a low-power optical link, already from the transmitter side. This paper presents the design methodology and circuit implementation in a 130-nm SiGe:C BiCMOS technology of

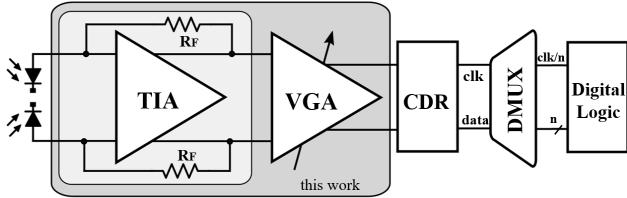


Fig. 1. Block diagram representation of one branch of a coherent receiver.

a differential linear TIA optimized for low averaged input-referred noise current density while preserving large BW for high-speed, high-sensitivity optical receivers.

Simultaneous sensitivity and BW optimization is still a fundamental challenge in TIA design. TIA topologies such as common-gate or regulated cascode [8] that aim at relaxing the effect of the input capacitance for enhancing the BW, incur in high current noise contribution, degrading the sensitivity. Shunt-feedback TIAs are known for their low-noise characteristics; however, simultaneous high-frequency operation requirement limits the maximum value of the feedback resistor [9] and therefore, the maximal sensitivity. To alleviate this issue, different techniques such as π -network matching at the input or between stages [10] use inductors to tune out the parasitic capacitances, effectively extending the BW without integrating the noise at higher frequencies, but with still moderate effect: $22.42 \text{ pA}/\sqrt{\text{Hz}}$ for 50-GHz BW in 65-nm CMOS [11]. A more effective approach based on post-amplifier equalization has been introduced in [12], and exploited in 65-nm CMOS for the first time in [13] and [14], for improving sensitivity without sacrificing BW, achieving $15.3 \text{ pA}/\sqrt{\text{Hz}}$ for 18-GHz BW in [13] and $17.8 \text{ pA}/\sqrt{\text{Hz}}$ with 21.4-GHz BW in [14].

The TIA topology presented in this paper makes use of a low-BW shunt-feedback input TI stage which integrates substantially less noise together with multi-stage equalization and input series peaking, which recover the target BW. The noise-BW tradeoff is shown to be surpassed, with designs that feature less than $10 \text{ pA}/\sqrt{\text{Hz}}$ averaged input-referred current noise density while operating at 100 Gb/s data rate. Analogous TIA designs are implemented in two different 130-nm SiGe:C BiCMOS processes from IHP, SG13S with $f_T/f_{\max} = 250/340 \text{ GHz}$ (referred as 13S-TIA, in the following) and SG13G2 with $f_T/f_{\max} = 300/500 \text{ GHz}$ (referred as G2-TIA), in order to evaluate the technology role and limitations in the circuit performance. Both TIA designs are well matched at the input and output to 50Ω by means of reactive structures and can also be seen as general-purpose low-noise cascadable gain blocks for conditioning signals between blocks in different applications [15]. The low-noise design methodology together with the characteristics of the SiGe:C BiCMOS technology used, bring the presented prototypes ahead of the state of the art, featuring, to the author's best knowledge, the best noise performance at such data rate compared to other silicon-based and InP solutions.

The remainder of this paper is organized as follows. Section II reviews the fundamentals of the design methodology that allows for an effective noise-BW decoupling in a bipolar

front end. Section III describes briefly the technology characteristics. Section IV presents the circuit design details. Section V shows the measurement results from both technologies and compares the performance of both TIAs with an extensive review of the state of the art. Section VI provides the conclusion.

II. DESIGN METHODOLOGY

This section begins with an analysis of the noise and BW relationship for the case of a classical shunt-feedback topology in a bipolar front end. The design constraints of this implementation are discussed and shed light into the extent up to which an equalization method as the one used here transcends the aforementioned noise-BW compromise.

In Fig. 2, a shunt-feedback TIA with post-amplification is presented, and the main noise sources are annotated as corresponding to a bipolar implementation. For the general case of a second-order system comprising a core amplifier with gain A , and cutoff frequency f_0 , the TI limit (1) as derived in [16], describes the maximum TI gain that a TIA can attain for a given BW and technology (f_T)

$$\begin{aligned} R_F &\leq A \cdot f_0 / (2\pi \cdot C_T \cdot \text{BW}^2) \\ R_F &\sim f_T / (2\pi \cdot C_T \cdot \text{BW}^2) \end{aligned} \quad (1)$$

where C_T is the total input capacitance obtained as the sum of the parallel input capacitance of the amplifier (C_I) and the capacitance of the photodiode (C_{PD}). Inequality (1) reveals that the TI degrades quadratically with the BW, and not linearly, if the input capacitance is constant. The TI limit produces a rapid degradation of the sensitivity in high BW applications, since for a desired BW it sets an upper bound to R_F which, as will be shown in the following, is one of the dominant noise sources. The contributions to the input-referred noise in Fig. 2 are as follows: $I_{n,R_F}^2 = 4kT/R_F$ is the feedback resistor thermal noise and contributes directly to the input. From the amplifier, there is the shot noise generated by the base current which is given by $I_{n,B}^2 = 2qI_C/\beta$ and adds directly to the input; the shot noise generated by the collector current, given by $I_{n,C}^2 = 2qI_C$ and the thermal noise generated by the intrinsic base resistance, given by $I_{n,R_b}^2 = 4kT/R_b$, and both must be referred to the input [9]. Finally, the noise of the post-amplifier stage is modeled with voltage source $V_{n,\text{post}}^2$, and must be divided by the TIA TI transfer function $|Z_T(s)|$ to find its contribution in the input noise. It is also assumed that the gain of the core amplifier is $A \gg 1$, so that the noise contributions of the amplifier load can be neglected and $|Z_T(s)|$ equals R_F at low frequency [9]. The total input-referred noise spectrum for the case of shunt-feedback TIA with post-amplification ($I_{n,\text{in,TOT}}^2$), is given by

$$I_{n,\text{in,TOT}}^2 = I_{n,R_F}^2 + I_{n,\text{amp}}^2 + I_{n,\text{post}}^2 \quad (2)$$

where [9]

$$\begin{aligned} I_{n,\text{amp}}^2(f) &= \frac{2qI_C}{\beta} + 4kTR_b \left(\frac{1}{R_F^2} + (2\pi f C_{PD})^2 \right) \\ &+ \frac{2qI_C}{g_m^2} \left(\frac{1}{R_F^2} + (2\pi f C_T)^2 \right). \end{aligned} \quad (3)$$

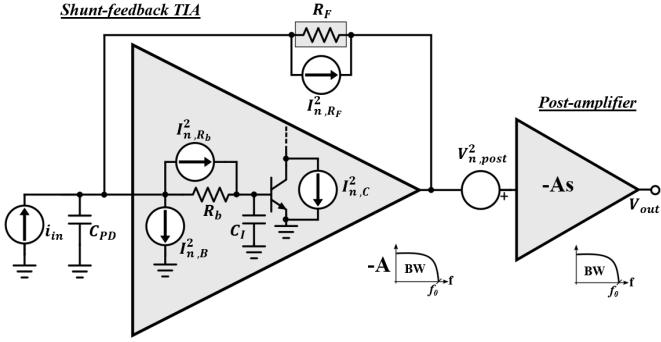


Fig. 2. Front end of optical receiver in classical cascaded approach comprising bipolar shunt-feedback TIA stage and post-amplifier.

Neglecting base shot noise it results

$$I_{n,amp}^2(f) = \frac{4kT R_b}{R_F^2} + \frac{2q I_C}{g_m^2 R_F^2} + \frac{2q I_C (2\pi C_T)^2}{g_m^2} f^2 + 4kT R_b (2\pi C_{PD})^2 f^2. \quad (4)$$

For calculating the contribution from the post-amplifier, \$Z_T(s)\$ must be obtained. Considering the typical case of a shunt-feedback TIA with a Butterworth response for maximally flat gain, the TIA frequency response is given by [9]

$$|Z_T(s)|^2 \approx R_F^2 / \left| 1 + \frac{s}{2\pi \text{BW}} \right|^4 \quad (5)$$

and then, the post-amplifier contribution to the input noise will be given by

$$I_{n,post}^2(f) = \frac{V_{n,post}^2}{R_F^2} \left(1 + \left(\frac{f}{\text{BW}} \right)^4 \right) \quad (6)$$

and therefore, the total noise

$$I_{n,in,TOT}^2 = \frac{4kT}{R_F} + \frac{4kT R_b}{R_F^2} + \frac{2q I_C}{g_m^2 R_F^2} + \frac{2q I_C (2\pi C_T)^2}{g_m^2} f^2 + 4kT R_b (2\pi C_{PD})^2 f^2 + \frac{V_{n,post}^2}{R_F^2} + \frac{V_{n,post}^2}{R_F^2} \left(\frac{f}{\text{BW}} \right)^4 \quad (7)$$

where the most dominant components correspond to the white thermal noise contribution of the feedback resistor and the \$f^2\$ term of the base resistance. From (1) and (7), the trade-off between BW and noise in this implementation becomes evident, and standalone minimization of the dominant noise contributors in (7) would directly degrade the BW: increasing \$R_F\$ reduces its thermal noise but reduces the BW quadratically; reducing the base resistance (\$R_b\$) of the input transistors by augmenting their size increases the input capacitance and deviates the biasing condition from the peak \$f_T\$, both effects reducing BW, and for the same \$I_C\$ increases the collector noise.

It is here that the benefit of post-amplifier equalization strikes in by effectively decoupling these two entities. Instead of having both stages with the same BW (\$\text{BW}/n\$), the input stage is designed with a lower BW (\$\text{BW}/n\$), and the post-amplifier provides peaking at the higher frequencies, equalizing the

gain such that the total bandwidth is restored to BW. In this case, from (1) the feedback resistor in the TIA must increase proportionally to \$n^2\$ in order to keep the same TI gain – BW product. Replacing in (7) the term \$R_F\$ with \$n^2 R_F\$ and BW with \$(\text{BW}/n)\$ then

$$\begin{aligned} I_{n,in,TOT}^2 &= \frac{4kT}{n^2 R_F} + \frac{4kT R_b}{n^4 R_F^2} + \frac{2q I_C}{g_m^2 n^4 R_F^2} + \frac{2q I_C (2\pi C_T)^2}{g_m^2} f^2 \\ &+ 4kT R_b (2\pi C_{PD})^2 f^2 + \frac{V_{n,post}^2}{n^4 R_F^2} + \frac{V_{n,post}^2}{n^4 R_F^2} \left(\frac{f}{\text{BW}/n} \right)^4 \\ &= \frac{4kT}{n^2 R_F} + \frac{4kT R_b}{n^4 R_F^2} + \frac{2q I_C}{g_m^2 n^4 R_F^2} + \frac{2q I_C (2\pi C_T)^2}{g_m^2} f^2 \\ &+ 4kT R_b (2\pi C_{PD})^2 f^2 + \frac{V_{n,post}^2}{n^4 R_F^2} + \frac{V_{n,post}^2}{R_F^2} \left(\frac{f}{\text{BW}} \right)^4. \end{aligned} \quad (8)$$

It can be seen how the frequency-dependent terms (\$f^2\$ and \$f^4\$) from (8) are the same as in (7), but the thermal noise from the feedback resistor has been reduced by a factor of \$n^2\$ and the other dc noise components from the amplifier and post-amplifier noise have been reduced by a factor of \$n^4\$, which even for low values of \$n\$, essentially eliminates them. Therefore, although the post-amplifier contributes now with in-band input-referred noise starting the ramp-up at \$f = \text{BW}/n\$, having reduced its dc noise magnitude by an \$n^4\$ factor, its contribution to the input-referred noise amounts, on the whole, to a lower value.

This approach will be useful as far as the post-amplifier is able to restore the BW; if too aggressive peaking is used, it might be difficult to preserve gain and group delay flatness over frequency, inducing data-dependent jitter which compromises signal integrity and pulse fidelity. This effectively limits the extent of BW reduction of the first stage. Following this approach, the TIAs presented in this paper target to achieve a low-noise level at the input while still maintaining a BW above \$\sim\$45 GHz. The block diagram of the TIAs is depicted in Fig. 3, and it comprises five blocks: input matching structures, input TIA stage, VGA, 50-\$\Omega\$ buffer, and output matching structures. The amplification is divided in three stages: the input TIA stage amplifies the low-frequency part and will feature a BW that is less than 2 times the value of the total BW finally achieved. The second stage, a VGA with capacitive degeneration, has a bandpass-like characteristic providing peaking in the middle frequency range. Finally, shunt peaking is used in the output buffer and series peaking is used at the input of the TIA, in order to raise the TI gain at the higher frequencies. The input inductor has the additional benefit of improving the high-frequency matching, since 50-\$\Omega\$ interface is targeted. Section IV provides the specific details on the circuit design.

III. TECHNOLOGY

Both TIA designs are implemented in the SiGe:C BiCMOS technology platform of IHP, in two different processes: the first TIA is implemented in the SG13S qualified process [17] which

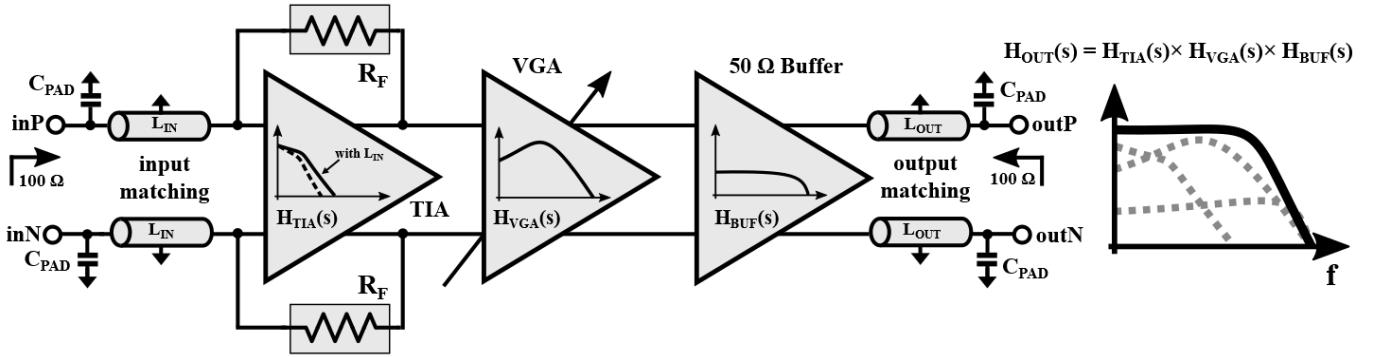


Fig. 3. Block diagram of the TIAs.

provides $f_T/f_{\max}/\beta = 250/340 \text{ GHz}/900$ and the second TIA is fabricated in the SG13G2 process [18], which is not yet qualified, and is therefore susceptible to experiencing larger deviations from the model predictions, and features $f_T/f_{\max}/\beta = 300/500 \text{ GHz}/650$. Both processes have an available back end of line stack of seven metal layers with two thick layers of 2- and 3- μm thickness, suitable for RF passive components design. The noise performance of HBTs, expressed in terms of the minimum noise figure (NF_{\min}) is strongly dependent upon both the dc current gain (β) and the f_T/f_{\max} figures, as given by (9) from [19] where n is the collector current quality factor and R_e is the emitter resistance

$$\text{NF}_{\min} = 1 + \frac{n}{\beta} + \frac{f}{f_T} \sqrt{\frac{2qI_C(R_e + R_b)}{kT}} \left(1 + \frac{f_T^2}{\beta f^2} \right) + \frac{n^2 f_T^2}{\beta f^2}. \quad (9)$$

Since the SG13G2 technology features lower β , the noise performance at the lower frequencies will be limited. On the other hand, due to the higher f_T and lower R_b (from the higher f_{\max} [19]) than the SG13S process, the NF_{\min} with increasing frequency will be lower. This has been graphically represented in [20] for both processes at 25 GHz, and it can be seen that for collector current densities above 5 mA/ μm^2 , the NF_{\min} from the SG13G2 technology is ~ 1 dB lower than for the SG13S. Below that biasing condition, however, the lowest NF_{\min} is achieved, with both technologies performing similarly in terms of noise.

IV. CIRCUIT IMPLEMENTATION

The complete schematic of the RF path of the implemented TIAs is presented in Fig. 4. It follows a fully differential linear architecture suitable for a coherent receiver implementation. Differential signaling serves also to mitigate the common-mode noise from power supply and silicon substrate, as well as the effects of supply and ground inductance that appear in single-ended excitation. Vulnerability to common-mode noises would be particularly severe in applications involving multi-channel parallel optical receivers for above 100 Gb/s and therefore, fully differential signaling is required already at the input stage of the receiver [21].

As described in Section II, a common-emitter shunt feedback topology with constant TI gain was selected for the

input TIA stage, with transistors (Q_1-Q_2). Emitter followers (Q_3-Q_4) precede the feedback resistors and the second stage, for level shifting and buffering. This input stage is biased with a tail current that might be adjusted with the pin BiasI which controls as well the bias of the second stage. The current mirrors have been implemented as indicated in the biasing circuit depicted in Fig. 4. Large resistors have been added to the bases of transistors in order to improve the mirroring matching and to mitigate possible signal leakage or disturbances thanks to the low-pass filtering effect created with these resistors and the capacitors placed at the base connection. A typical current mirror implementation with emitter degeneration resistors would be more effective [22], but was not feasible due to the lack of headroom in the VGA. The biasing of the input stage is set to $\sim 5 \text{ mA}/\mu\text{m}^2$ collector current density, which according to [20] falls in the region of lowest NF_{\min} . Following the TIA, a VGA is used to maintain linearity, reducing jitter, and pulsedwidth distortion for high input currents. The VGA provides a 15-dB gain-controlled range, while maintaining constant BW during gain tuning. A current steering topology has been used to meet these requirements, where the gain is controlled with the $V_c - V_{cb}$ difference. This voltage difference is generated with the circuit presented in Fig. 5, which by using a bandgap reference requires only one external control voltage (GC) for the gain tuning. Resistive degeneration was used with resistors $R_{E1} \sim 40 \Omega$ to improve the linearity of this stage. A degeneration capacitor is included in parallel with resistors R_{E1} to introduce a high-frequency zero at $1/\pi R_{E1} C_{\text{deg}}$ responsible for the gain peaking in the mid-band frequency range. C_{deg} is implemented as a varactor which allows for a $\pm 35\%$ tuning range to accommodate possible process variations. The typical value is set in both cases to 220 fF. In the maximum gain setting, the VGAs provide 9-dB dc gain. Emitter followers ($Q_{11}-Q_{12}$) are used for level shifting and to drive the large transistors of the output buffer.

The output buffer is a common-emitter differential pair with 50- Ω loads which provides broadband matching at the output and delivers an output voltage of $\sim 1 \text{ V}_{\text{ppd}}$ to the 25- Ω equivalent load. This headroom is responsible for the large power dissipated in the buffer alone, which amounts to 40% of the total. Degeneration resistors were used to improve the linearity. The buffer provides 0-dB gain; shunt peaking was used at the supply to boost the gain at the higher frequencies in

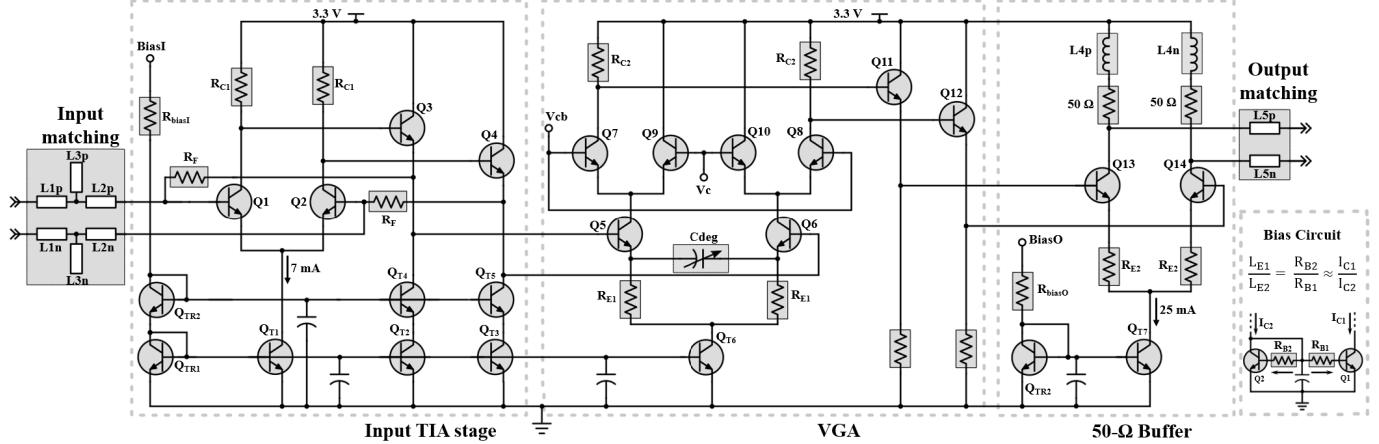


Fig. 4. Schematic of the TIAs.

order to equalize the VGA roll-off. At the output, inductors L_5 where inserted in series and are used to improve the matching at the high frequencies, compensating the degradation caused by the capacitance of the output transistors (Q_{13} - Q_{14}) and the effect of the pad capacitances (25 fF).

The inductors at the input (L_1 - L_3) are used to extend the BW by compensating the dominant pole produced by the input impedance of the first stage and the pad capacitance. The value of these inductors was chosen so as to guarantee broadband 50- Ω matching mainly to allow characterization of the ICs in a conventional measurement environment. If used more aggressively, higher BW extension ratio could be achieved, but the S_{11} would be deteriorated [23]. In the 13S-TIA only one inductor was used ($L_2 = L_3 = 0$), while in the G2-TIA, which features a larger BW, a broader frequency range was covered using a single-stub network. The peaking produced by all the reactive components was carefully controlled. Since the TIAs must be able to process broadband random data, peaking would translate into ringing in the eye diagram, largely deteriorating the performance, especially in the case of multilevel signals. In the presence of an external PD, the value of these inductors should be tuned to absorb the added parasitic capacitances of the PD and the pad. Moreover, all the inductors in the circuit have been designed as microstrip transmission lines with ground shield. The shield was implemented in the bottom-most metal layer so as to minimize the capacitance added to the signal trace. This reduces significantly the Q -factor, and hence the magnitude of the peaking, and moreover improves the modeling accuracy against variations in the characteristics of the substrate. It also provides layout flexibility in placing components next to each other since the coupling is reduced, and allows for an uninterrupted ground mesh covering the entire chip. The effect of the inductors at the input and output in the S_{11} and S_{22} of the G2-TIA can be seen in Fig. 6(a).

The noise-BW optimization was an iterative process. The averaged input-referred current noise density, BW, input/output matching, gain ripple, and group delay variation were monitored while minimizing the dominant noise contributors. The target low average input-referred current noise density was obtained, when the contributions from

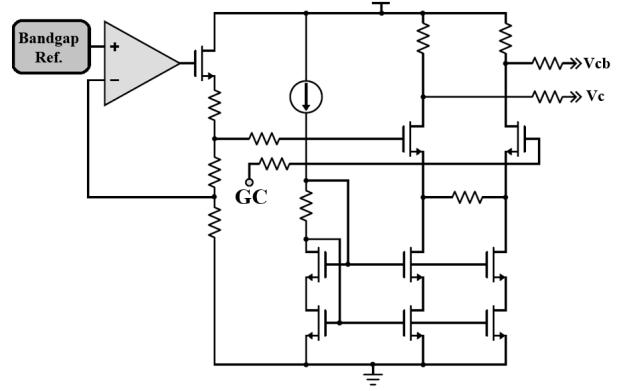


Fig. 5. Gain control circuitry.

collector noise and thermal noise from the base resistance of the input transistors and the thermal noise from the feedback resistor become comparable and together amount to $\sim 45\%$ of the total noise. The contribution of each stage to the total BW equalization can be observed in Fig. 6(b) for the G2-TIA example. The input stage has a BW that is 2.2 times less than the total BW finally achieved, which is recovered by the VGA in the mid-band and by the peaking effect of the input reactive structures and the output buffer in the high-frequency range. In Fig. 6(c), the group delay variation corresponding to a different number of components added to the RF path is depicted; it can be seen that the most critical variation arises from the peaking capacitor in the VGA; the designed inductors add a constant delay at all frequencies, without inducing delay variation. Fig. 7 depicts the distribution of the top contributors in the integrated input-referred noise. The number of noise contributors considered accounts for $\sim 90\%$ of the total integrated input-referred noise. As mentioned in Section II, it can be seen how the input stage clearly dominates the total noise, despite the large peaking used in the VGA for equalization. The contribution from R_F becomes now comparable to the second-order terms from (8). The slice labeled as “TIA stage: other contributors” in the pie chart represents the noise from other sources not modeled in (8), such as the base resistances of Q_3 - Q_4 , or the emitter-resistance noise from Q_1 - Q_2 , for example, each with very small contribution

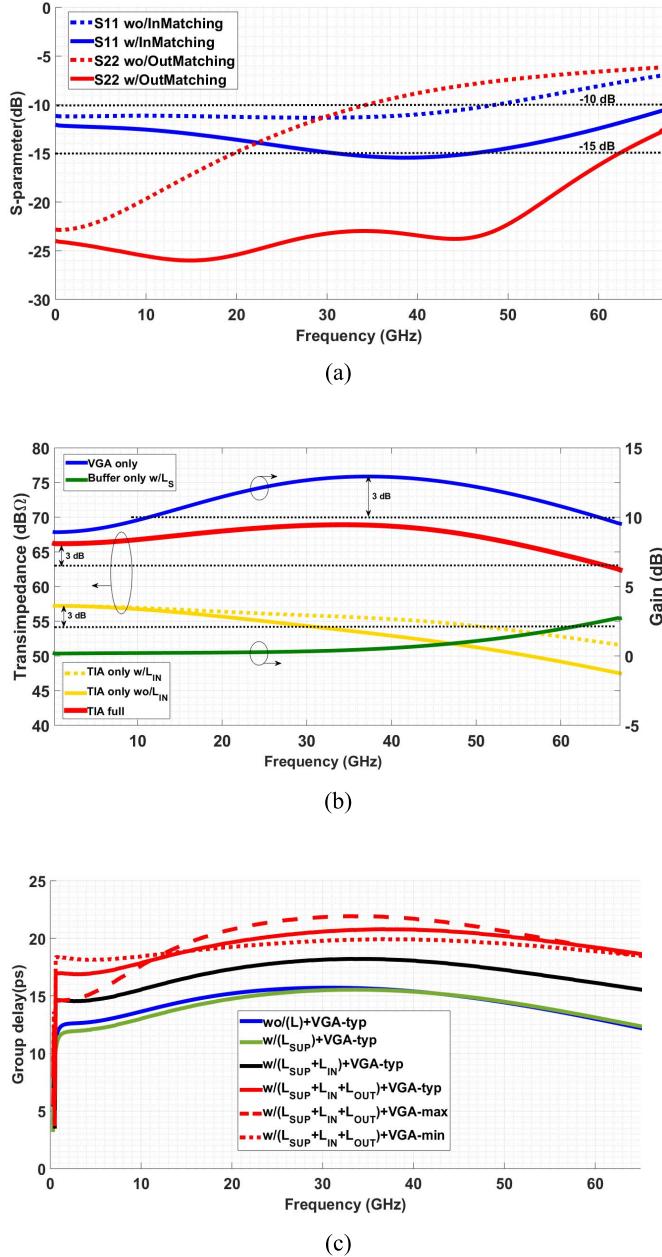


Fig. 6. Post-layout simulation results from G2-TIA. (a) Effect of input and output matching structures. (b) Gain over frequency for different stages. (c) Group delay with different reactive components added to the RF path.

in the total noise, and that now, due to the reduction in the previously much larger sources, become more visible.

All relevant component parameters from the SG13S and SG13G2 designs are presented in Tables I and II, respectively. Both ICs dissipate 150-mW power from a 3.3-V supply. In Fig. 8, the chip microphotographs of the 13S and G2 TIAs are presented, where all the described reactive structures can be clearly distinguished. Both chips have identical pad-frame and occupy 0.42-mm² area.

V. EXPERIMENTAL VERIFICATION

The TIAs were fully characterized in the electrical domain via on-wafer probing. S-parameters, eye diagram, total

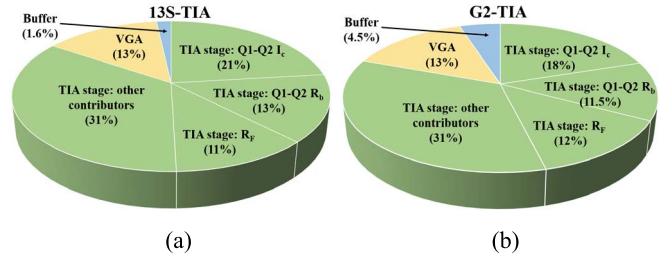


Fig. 7. Distribution of the different noise contributions in the integrated input-referred noise for the (a) 13S-TIA and (b) G2-TIA.

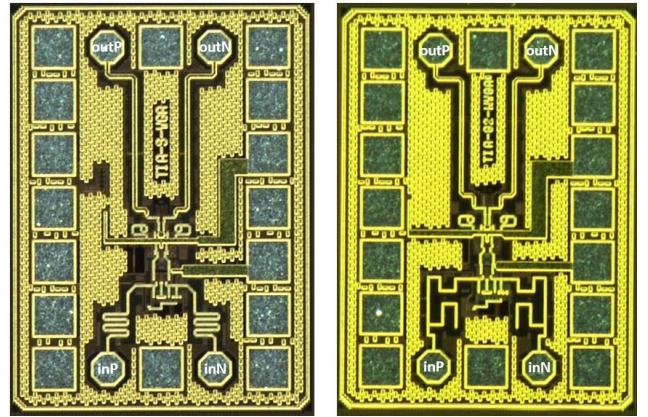


Fig. 8. Chip microphotographs of 13S-TIA (left) and G2-TIA (right).

TABLE I
13S-TIA DESIGN PARAMETERS' SUMMARY

Parameter	Value	Parameter	Value
L1	2 μm×370 μm	R _{E1}	40 Ω
L2	0	R _{E2}	17 Ω
L3	0	Q1-Q2	8×120×840 nm ²
L4	2 μm×120 μm	Q3-Q4	4×120×840 nm ²
L5	6 μm×350 μm	Q5-Q10	4×120×840 nm ²
R _F	550 Ω	Q11-Q12	2×120×840 nm ²
R _{C1}	130 Ω	Q13-Q14	8×120×840 nm ²
R _{C2}	150 Ω	C _{deg}	10×974×800 nm ²

harmonic distortion (THD), and noise measurements were carried out, as described in the following.

A. S-Parameters

In the frequency domain, four-port, true-differential, S-parameters measurements up to 67 GHz were performed using a Rhode & Schwarz ZVA67 vector network analyzer with -40 dBm of input power. The results are presented in Fig. 9(a) and (b) for the 13S and G2 TIAs, respectively. The 13S-TIA results are in excellent agreement with the simulation, and both input and output return loss are better than 13 dB up to 45 GHz. The G2-TIA S-parameters measurements are also in good agreement with the simulation, with a slight gain deviation of 1.2 dB already from dc due to process variations. |S₁₁| and |S₂₂| are better than 10 dB in the whole measurement span. The ripple observed in the measured results is due to the very small input powers used to avoid the saturation of the amplifiers. The open-load TI gain has been extracted from

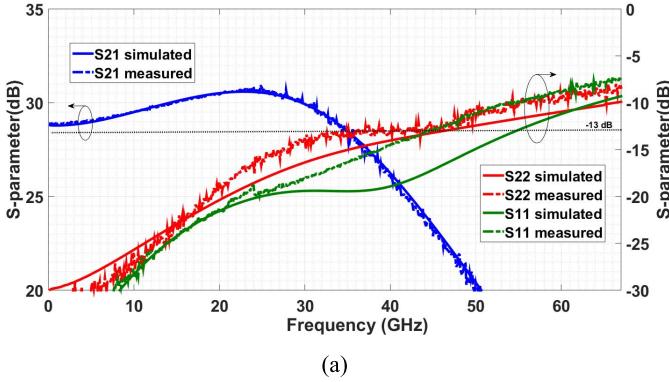


Fig. 9. Measured versus simulated S-parameters. (a) 13S-TIA. (b) G2-TIA.

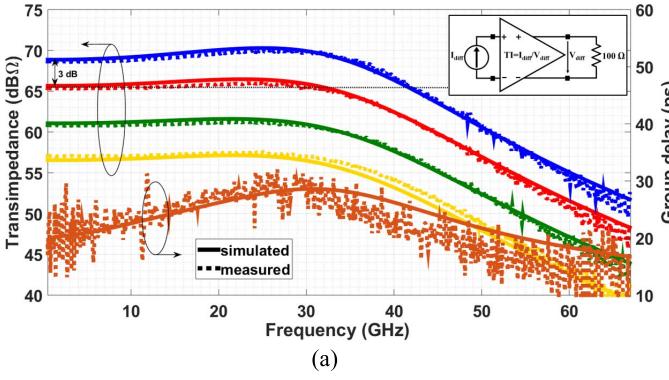


Fig. 10. Measured versus simulated TI with gain control and group delay. (a) 13S-TIA. (b) G2-TIA.

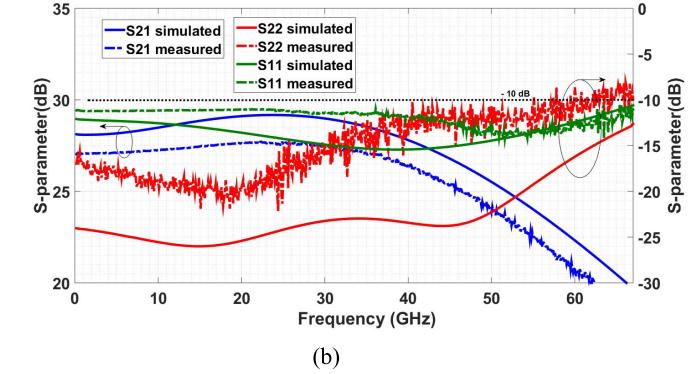
TABLE II
G2-TIA DESIGN PARAMETERS' SUMMARY

Parameter	Value	Parameter	Value
L1	$2 \mu\text{m} \times 60 \mu\text{m}$	RE1	40Ω
L2	$2 \mu\text{m} \times 240 \mu\text{m}$	RE2	18Ω
L3	$2 \mu\text{m} \times 140 \mu\text{m}$	Q1-Q2	$10 \times 70 \times 900 \text{ nm}^2$
L4	$2 \mu\text{m} \times 130 \mu\text{m}$	Q3-Q4	$5 \times 70 \times 900 \text{ nm}^2$
L5	$5 \mu\text{m} \times 330 \mu\text{m}$	Q5-Q10	$6 \times 70 \times 900 \text{ nm}^2$
RF	480Ω	Q11-Q12	$5 \times 70 \times 900 \text{ nm}^2$
RC1	160Ω	Q13-Q14	$10 \times 70 \times 900 \text{ nm}^2$
RC2	150Ω	C _{deg}	$10 \times 974 \times 800 \text{ nm}^2$

the S-parameters as $\text{TI} = V_{\text{diff}}/I_{\text{diff}}$, as illustrated in the inset of Fig. 10(a) and the results from both TIAs are depicted in Fig. 10(a) and (b), compared to the simulation results. The 13S-TIA showed $68.5 \text{ dB}\Omega$ of differential TI, with 42-GHz BW, while the G2-TIA features a smaller TI gain of $65 \text{ dB}\Omega$ but 36% higher BW, reaching the 3-dB point only at 66 GHz. The corresponding group delay from each TIA is presented in Fig. 10(a) and (b), derived from the phase of the S_{21} forward transmission coefficient, with an aperture value of 5. It can be seen that in both cases, measurements and simulation are in very good agreement, and both TIAs feature a low group delay variation of $\pm 5 \text{ ps}$ within the respective BWs.

B. Noise

To characterize the noise of the IC, two sets of measurements were performed. With the input of the TIA left



$$I_{n,\text{in}} = \frac{2\sqrt{(2.3 \text{ mV})^2 - (0.7 \text{ mV})^2}}{68.5 \text{ dB}\Omega} = 1.64 \mu\text{A}_{\text{rms}} \quad (10)$$

$$I_{n,\text{in,avg}} = \frac{I_{n,\text{in}}}{\sqrt{42 \text{ GHz}}} = 8 \text{ pA}/\sqrt{\text{Hz}}. \quad (11)$$

The measured integrated output noise of the 13S-TIA was $2.3 \text{ mV}_{\text{rms}}$, which after subtraction of the noise of the oscilloscope module itself ($0.7 \text{ mV}_{\text{rms}}$) translates into a differential integrated input-referred current noise of $1.64 \mu\text{A}_{\text{rms}}$ and average input-referred current noise density of $8 \text{ pA}/\sqrt{\text{Hz}}$. With similar procedure, the G2-TIA featured a slightly lower averaged input-referred current noise density value of $7.6 \text{ pA}/\sqrt{\text{Hz}}$. In addition, the equivalent output-referred noise voltage spectral density up to 30 GHz was also measured as reported in Fig. 11 compared to the simulation results. These values were obtained with a Rhode & Schwarz FSV30 spectrum analyzer after performing a noise calibration, with the receiver in open input. Simulation and measurement are in good agreement; the slight deviation between both curves is partially

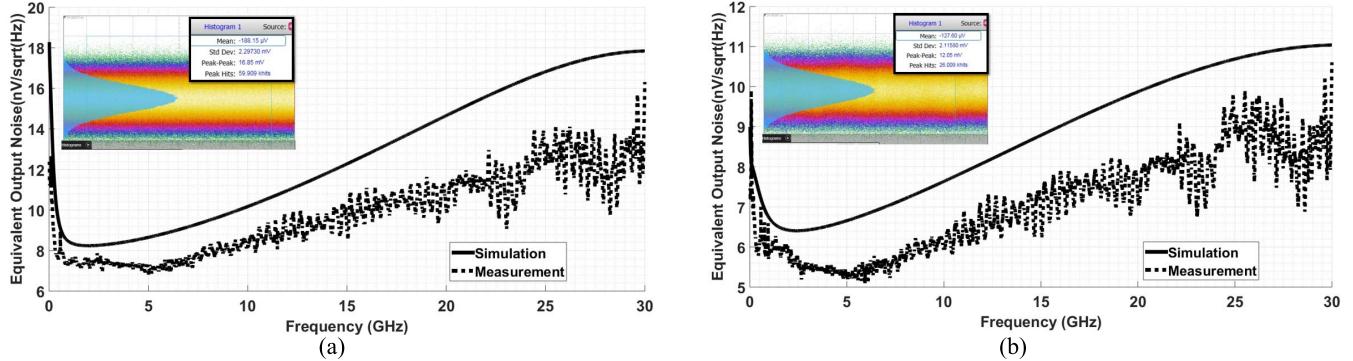


Fig. 11. Measured versus simulated output-referred noise voltage spectral density. (a) 13S-TIA. (b) G2-TIA. Inset: Integrated output noise from the histogram function of the oscilloscope.

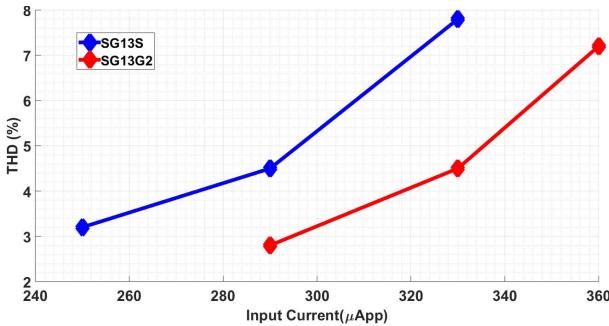


Fig. 12. Measured THD at 1 GHz for different input currents in the maximum gain condition.

attributed to built-in error in the loss de-embedding procedure, from differences in the actual insertion loss of the components present in the setup and the values reported in the datasheets. The larger deviation in the G2-TIA is attributed to the observed process variations. The measured results are also in line with the output-referred noise spectral density obtained from the oscilloscope measurements, i.e., $11 \text{ nV}/\sqrt{\text{Hz}}$ for the 13S-TIA and $7 \text{ nV}/\sqrt{\text{Hz}}$ for the G2-TIA.

C. Linearity

The linearity of the TIA was characterized by measuring THD at 1 GHz, considering ten harmonics. For this setup, at the input, a Rhode & Schwarz SMR60 signal generator was used and the signal was split and converted to differential using a Marki broadband balun up to 67 GHz. At the output, a similar balun combines the signal which is applied to a 50-GHz Agilent E4448A spectrum analyzer. After de-embedding the losses at input and output, the THD values were obtained for different input currents as presented in Fig. 12. The TIAs remain linear with THD below 5% in the maximum gain condition for input currents in the range of $300 \mu\text{App}$ and 800 mVppd output voltage. Due to the lower TI gain, the G2-TIA shows a larger linear range.

D. Eye Diagram

In the time domain, an SHF 12105A bit pattern generator (BPG) together with an SHF 603A multiplexer (MUX) were used to produce the input signals that were applied to the TIAs, as seen in the setup photograph depicted in Fig. 13. The

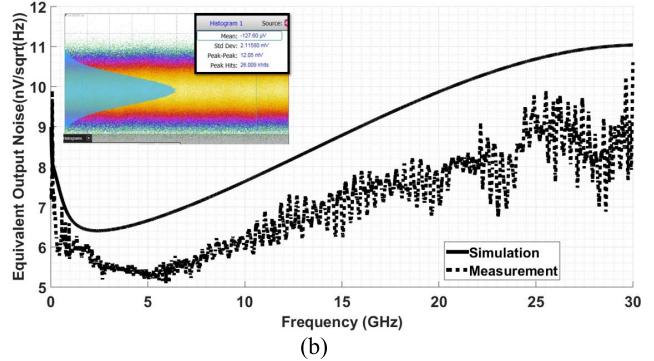


Fig. 13. Time-domain measurement setup using 67-GHz components (adaptors, cables, dc-blocks, and attenuators).

MUX doubles the ON-OFF-keying data rate from two channels of the BPG. At the input, after the MUX output, a set of attenuators and a pair of dc blocks were used, after which two phase-matched 0.5-m RF cables guide the differential signal to the input probe. At the output, two similar cables are used between the output and the oscilloscope sampling heads. DC blocks are also inserted at the output. All these cascaded components at input and output, with 67-GHz BW each, significantly deteriorate the eye diagrams, since no pre-emphasis techniques were used to compensate for the setup losses. Despite these limitations, wide open single-ended eye diagrams measured with $2^{31}-1$ PRBS and input signals as low as $100 \mu\text{App}$ are presented in Fig. 14, up to 90 and 100 Gb/s data rate, for the 13S and G2 TIAs, respectively, in agreement with the small-signal BWs. Wide open eyes at these data-rates with such a small amplitude are also a sign of the good sensitivity of the TIAs. PAM-4 measurements were as well conducted. Using the same setup described before, the MUX was replaced with a 6-bit digital to analog converter (DAC) SHF 614B, using six channels of the BPG. The single-ended output eye diagrams with PAM-4 modulation are shown in Fig. 15, for input currents such that the TIAs deliver $\sim 800 \text{ mVppd}$ at the output. It can be seen how open eye diagrams with equally spaced levels were obtained, at 45 and 50 GBd for the 13S and G2 TIAs, respectively. The input eye diagrams, with $310 \mu\text{App}$ for the 13S-TIA and $420 \mu\text{App}$ for the G2-TIA, are shown in the insets of Fig. 15 for comparison. Both TIAs have clear capability of delivering above 100 Gb/s data rate in PAM-4 multi-level format.

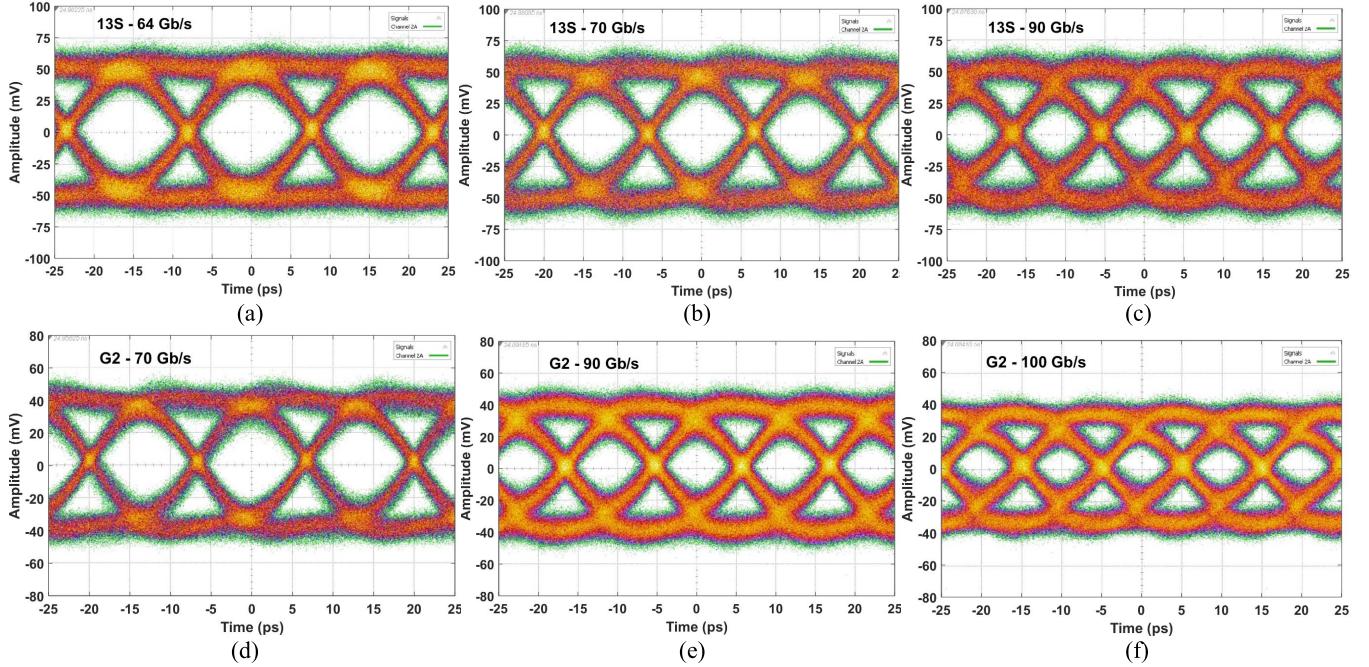


Fig. 14. Time-domain single-ended measurement results at $100 \mu\text{App}$ NRZ PRBS31 for 13S-TIA at (a) 64, (b) 70 and (c) 90 Gb/s, and for G2-TIA at (d) 70, (e) 90 and (f) 100 Gb/s.

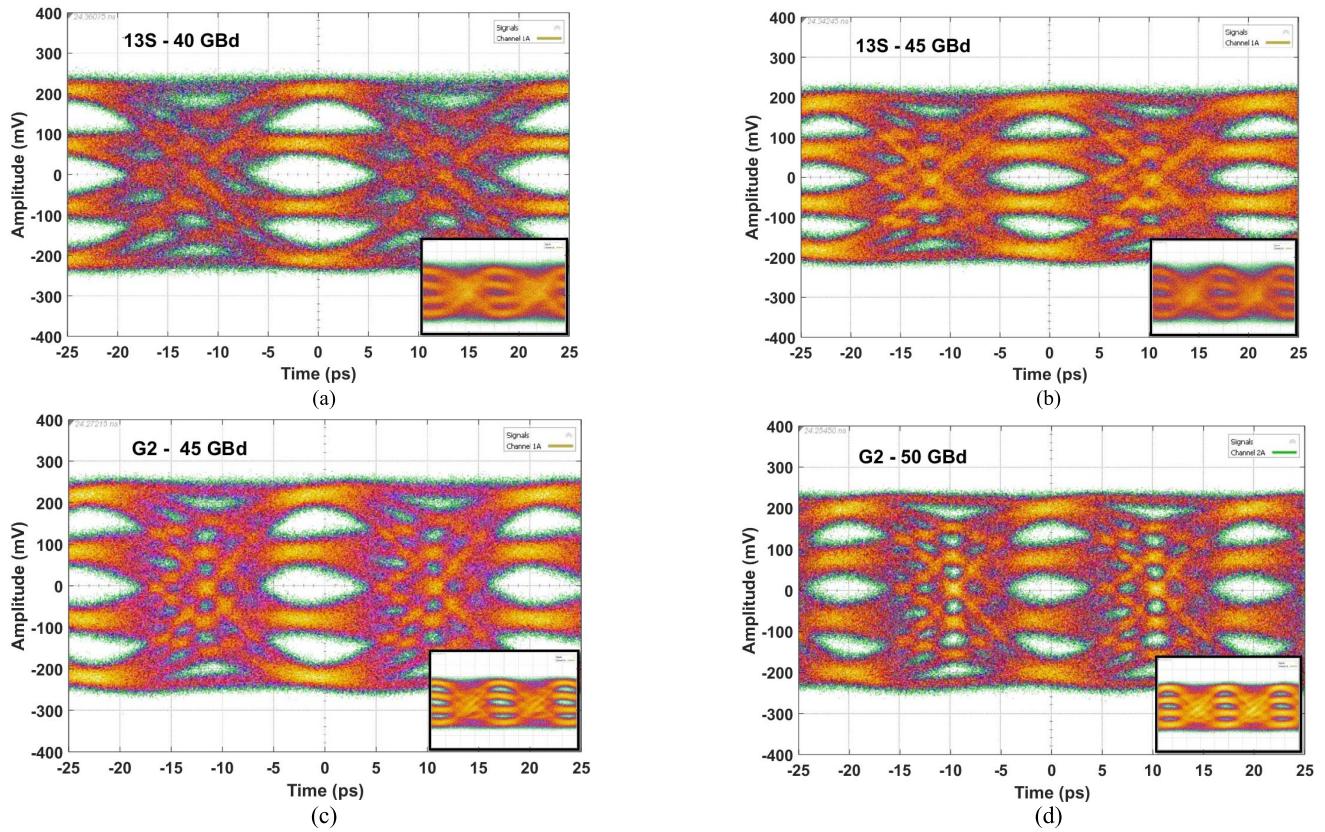


Fig. 15. Time-domain single-ended measurement results of PAM-4 PRBS31 for 13S-TIA at (a) 40 and (b) 45 GBd, and for G2-TIA at (c) 45 and (d) 50 GBd.

E. Technology Comparison: SG13S Versus SG13G2

From (1), in a shunt-feedback TIA implementation, an increase of $\sim 30\%$ in the $\text{TI} \cdot \text{BW}^2$ product, $\text{TI} \cdot \text{BW}^2$, is expected in the G2-TIA from the f_T technology

improvement considering also a 15% reduction in the input capacitance owing to the smaller G2 transistors. Such an improvement has indeed been observed in the fabricated chips, with the $\text{TI} \cdot \text{BW}^2$ product experiencing a slightly higher 40% enhancement in the G2-TIA, due to the increased optimization

TABLE III
MEASURED PERFORMANCE COMPARED WITH PRIOR PUBLISHED WORK

Ref.	Year	Technology	f_t (GHz)	SE/S2D ¹ /Diff.	Linear/ Limit.	PD (fF)	TI (dBΩ)	Bandwidth (GHz)	Noise (pA/ $\sqrt{\text{Hz}}$)	Power (mW)
[11]	2014	65 nm CMOS	-	Diff.	Limit.	50	52	50	22.42	49.2
[13]	2014	65 nm CMOS	-	S2D	Limit.	160	83	18	15.3	93
[14]	2014	65nm CMOS	-	SE	Limit.	N/A	76.8	21.4	17.8	137.5
[23]	2017	130 nm BiCMOS	300	Diff.	Linear	N/A	62	60	5.5	85
[24]	2016	250 nm CBiCMOS	110 /95	Diff.	Linear	N/A	52.5	32	13.1	70
[25]	2013	130 nm BiCMOS	-	Diff.	Limit.	65	76.5	23	15.8	68
[26]	2014	65 nm CMOS	-	SE	Limit.	N/A	42	24	16	3
[27]	2015	55 nm BiCMOS	330	SE	Linear	N/A	-	92	17.7 ²	48
[28]	2016	130 nm BiCMOS	-	Diff.	Linear	N/A	77	34	20	285
[29]	2016	130 nm BiCMOS	-	S2D	Limit.	N/A	72	38.4	14.8	261
[30]	2014	130 nm BiCMOS	200	SE	Limit.	N/A	55	86	20.4	89
[31]	2010	250 nm BiCMOS	180	S2D	Limit.	>100	75.5	37.6	20	150
[32]	2012	250 nm BiCMOS	180	S2D	Limit.	100	70.8	20.5	18	57
[33]	2015	130 nm BiCMOS	300	SE	Limit.	N/A	65	53.8	12.34 ³	21.2
[34]	2004	InGaAs-InP	160	Diff.	Limit.	N/A	56	47	35	484
[35]	2013	InP	300	Diff.	Linear	N/A	55	107	44 ³	360
This – 13S	2017	130 nm BiCMOS	250	Diff.	Linear	N/A	68.5	42	8	150
This – G2	2017	130 nm BiCMOS	300	Diff.	Linear	N/A	65	66	7.6	150

¹S2D stands for single-ended to differential. ²Calculated from reported integrated input referred current noise of 5.6 μA_{rms} in 100 GHz. ³simulated.

flexibility that the design methodology offers, despite the lower TI gain.

The averaged input-referred current noise density is, however, very similar in both TIAs. This comparable performance in terms of noise is attributed to the design methodology. Both TIAs have been designed with a factor $n \sim 2$ from (8). The feedback resistor (R_F) is also similar in both TIAs, and the input stage has been biased with low collector current density, rendering a similar noise contribution from the transistors in the low-frequency range as well. However, the higher f_T/f_{\max} reduces the contributions of the f^2 and f^4 components in (8) in the SG13G2 implementation, which translates into a slightly lower input-referred noise current noise density when averaged over the BW. The similar noise at the low frequencies can be seen from Fig. 11(a) and (b), where the difference in the output-referred voltage noise at 30 GHz corresponds to the lower 3.5 dBΩ TI gain in the G2-TIA, rendering similar input-referred noise values.

F. State-of-the-Art Comparison

Table III shows a comparison of the designed amplifiers with state-of-the-art TIAs in different technologies. The proposed designs feature the lowest average input-referred current noise density, with similar TI gain and without significantly deteriorating BW or power dissipation characteristics compared to other CMOS and InP solutions. This evidences the strength of the design methodology in surpassing the noise-BW tradeoff. Reference [23], which exhibits a lower input-referred current noise density of 5.5 pA/ $\sqrt{\text{Hz}}$, follows the same design technique here described. To achieve such a

low value, the VGA was removed and strong input series peaking was utilized at the expense of deteriorating the input 50-Ω matching, making it only suitable for a high-impedance optical interface. It is also worth noting that the performance of TIAs described herein terms of BW and sensitivity can only be maintained in a real application if the PD is closely integrated with the TIA and assumes a similar capacitance as the pads currently present in the layout (~ 25 fF). This would be feasible, for example, with Ge PDs, which show BWs above 70 GHz with capacitances lower than 15 fF, much smaller than III-V discrete photodiodes at similar data rates [36].

VI. CONCLUSION

The design methodology and circuit implementation of a TIA featuring low averaged input-referred current noise density without compromising the TIA BW have been presented. Two analogous TIA designs implemented in two different 130-nm SiGe:C BiCMOS processes from IHP, SG13S with $f_T/f_{\max} = 250/340$ GHz and SG13G2 with $f_T/f_{\max} = 300/500$ GHz, have been described, and illustrate the technology role in the key performance metrics of the amplifiers. The 13S-TIA features 68.5 dBΩ differential TI gain, 42-GHz 3-dB BW, and 8 pA/ $\sqrt{\text{Hz}}$ averaged input-referred current noise density; while, the G2-TIA provides 65 dBΩ differential TI gain, 66-GHz 3-dB BW, and 7.6 pA/ $\sqrt{\text{Hz}}$. Measured THD in both TIAs in maximum gain condition is better than 5% for 800 mVppd output swing and input currents in the order of 300 μA_{pp} . Both circuits dissipate 150 mW of power and are shown to operate at up to 100 Gb/s data rate with clean

PRBS31 non-return to zero (NRZ) and PAM-4 eye diagrams. The reported TIAs exhibit the lowest averaged input-referred current noise density shown to date at a BW capable of supporting 100 Gb/s net data rate, surpassing other silicon-based and InP implementations. Such performance has been enabled both by the low-noise technology and by the adopted design methodology, which allows to effectively overcome the classical noise-BW tradeoff.

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