A High-Fractional-Bandwidth, Millimeter-Wave Bidirectional Image-Selection Architecture With Narrowband LO Tuning Requirements

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***Abstract*— An image-selection, two-element transceiver is presented that operates over a large fractional bandwidth (FBW) covering both 71–76 and 81–86 GHz while requiring only 3 GHz of local oscillator (LO) tuning range at the RF mixer. A bidirectional sliding-intermediate frequency (IF) Weaver architecture allows operation in either transmit (TX) or receive (RX) modes. The sliding IF and narrow LO tuning range allow wideband image rejection using only a single-stage polyphase filter. The circuit is implemented in a 90-nm SiGe BiCMOS process and the RF and LO circuitry consume at most 150 and 250 mW, respectively. Measurements show less than ±0.75-dB gain variation over 10 GHz in the TX mode and less than ±1-dB variation over 10-GHz bandwidth in the RX mode. With 16- and 64-quadrature-amplitude modulation (QAM), the error vector magnitude is below −22 and −28.5 dB at the data rates of 12 and 9 Gb/s, respectively.**

***Index Terms*— Bidirectional transceivers, *E*-band, error vector magnitude (EVM), 5G, high data rate, image-selection transceiver, millimeter wave (MMW), SiGe.**

I. Introduction

MILLIMETER-WAVE (MMW) bands offer a large bandwidth for next-generation backhaul communication links [1]–[14]. In particular, *E*-band (71–76 and 81–86 GHz) provides a total of 10-GHz bandwidth with 2-GHz channels and is an excellent candidate for data rates exceeding 10 Gb/s over distances greater than 1 km due to the low atmospheric loss compared with 60 GHz. While traditionally GaAs or InP monolithic microwave integrated circuit (MMIC) processes were required for operation at the *E*-band, a recent work on the *E*-band [5]–[14] has demonstrated silicon-based monolithic solutions that allow substantial receive (RX) and transmit (TX) system integration.

The wide channel bandwidth (2 GHz) and large fractional bandwidth (FBW) (20%) impose substantial circuit design challenges to enable low error vector magnitude (EVM) with high-order quadrature-amplitude modulation (QAM) waveforms. Fig. 1 shows an example of conventional frequency planning for a 71–86-GHz transceiver system [5]–[10]. To cover both the 71–76-and 81–86-GHz bands, a local oscillator (LO) tuning range should be 15 GHz, which significantly complicates an MMW oscillator design, increases phase noise (PN) penalties, as well as image-rejection ratio (IRR) and conversion gain variation across the bandwidth.

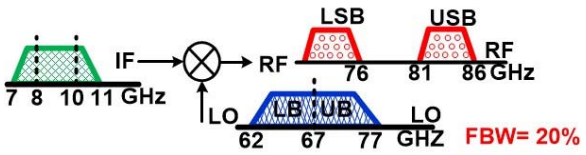

Fig. 1. Conventional single-sideband frequency planning of the *E*-band system requiring more than 20% FBW for LO.

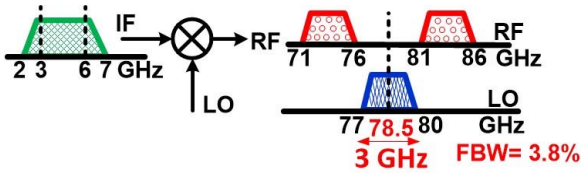

Fig. 2. Proposed frequency planning for ISA requiring less than 4% FBW for LO.

Generating quadrature LOs over the large FBW produces phase and amplitude mismatches that degrade the EVM. Earlier schemes have produced quadrature signals at MMW bands using quadrature VCO (QVCO) [15], multi-stage polyphase filter (PPF) [16]–[18], or coupled line coupler [19]. The QVCO LO requires tuning and locking range over the wideband LO range, increasing the PN and power consumption. A wideband multi-stage PPF is lossy and requires a wideband calibration circuit [6], [8]. For example, [8] proposed a compact layout for the two-stage PPF to reduce the mismatch arised from the device sizing and the MMW interconnect. However, it requires calibration circuitry with a switched varactor and an inductor with switchable lines operating within the wideband range. In [7], a load-intensive approach is proposed using a broadband oscillator with 45° power splitter to achieve lower amplitude and phase imbalance; however, this scheme only improves the data rate to 0.04 Gb/s. Therefore, a complex and wideband calibration circuit and buffer amplifiers are required to compensate the I/Q imbalance and the

Manuscript received October 2, 2017; revised February 28, 2018; accepted April 4, 2018. Date of publication May 15, 2018; date of current version July 20, 2018. This paper was approved by Associate Editor Waleed Khalil. *(Corresponding author: Najme Ebrahimi.)*

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Digital Object Identifier 10.1109/JSSC.2018.2828855

loss for the wideband multi-stage PPF or the other quadrature generation circuitry operating in a wide bandwidth.

In the proposed architecture, the LO is placed between the upper (81–86 GHz) and lower band (71–76 GHz) of the E-band shown in Fig. 2. Since 77 GHz is commonly used for automotive radar, this frequency band is not used in the communication system. The feature of the image-selection architecture (ISA) is that lower sideband (LSB) and upper sideband (USB) are images of each other, and selection between bands doubles the bandwidth and requires a smaller LO tuning range. Therefore, the ISA is a modification of a traditional image-rejection architecture [20]–[24], where a single phase inversion selects either the upper or lower band. This frequency plan reduces the tuning range to less than 3 GHz for E-band applications and results in more uniform circuit performance in terms of conversion gain and IRR. The IRR is also subject to a smaller tuning range and therefore is not prone to bandwidth-induced amplitude and phase mismatch, which relaxes the PPF requirements, its calibration circuitry, and therefore the EVM. This paper expands on earlier work from [25] that proposed the ISA to reduce the LO tuning range and details the tradeoff between FBW and PN, gain variation, and I/Q imbalance that increases EVM. In addition, this paper explains the bidirectional operation of the ISA for both TX and RX modes. In Sections II and III, the ISA is described with the analytical expression of the principle operation of the architecture. The circuit implementation of a two-channel bidirectional up-converter/down-converter is presented in Section IV. Section V presents the TX and RX measurement results and the improvement in the generated waveform.

II. EVM Degradation in Wideband MMW Transceivers

Lower EVM is a requirement for spectrally efficient M-QAM waveforms. For M-QAM communication circuits, the signal-to-noise ratio (SNR) is expressed as an EVM that can be related to the bit-error rate (BER) [26]

$$\mathrm{BER} = 1 - \left(1 - 4 \times Q\left(\sqrt{\frac{3}{(M-1)\mathrm{EVM}^2}}\right)\right)^2 \qquad (1)$$

where $Q(x)$ is the Gaussian complementary error function. For a fixed probability of bit error, the EVM must be reduced as the QAM complexity increases, i.e., $(M-1)\mathrm{EVM}^2$ is constant. For example, the EVM should drop by roughly a factor of 2 to increase the QAM constellation from $M = 16$ to $M = 64$ symbols.

EVM is degraded by numerous circuit nonidealities, including LO PN, I/Q mismatch, leakage, dc offsets, conversion gain flatness, frequency dependence, and amplitude non-linearity. The power amplifier (PA) and modulator non-linearity are improved with digital pre-distortion. LO leakage and dc offsets are common issues with the homodyne-based architecture. Heterodyne-based schemes are typically less sensitive to these problems but suffer from low IRR and high LO PN. Amplitude and phase mismatch of the quadrature LO (or RF) paths prevent perfect elimination of the unwanted image band as well as frequency-independent mixer conversion gain over high bandwidth. In other words, the amplitude and phase mismatch both degrade the IRR and cause conversion gain variation within the modulated signal bandwidth. Furthermore, the LO PN generates a phase error. For wideband MMW communication systems, I/Q mismatch and LO PN are the most significant EVM degradation factors excluding PA compression effects [27]. Assuming independence between the IRR and PN, the EVM is

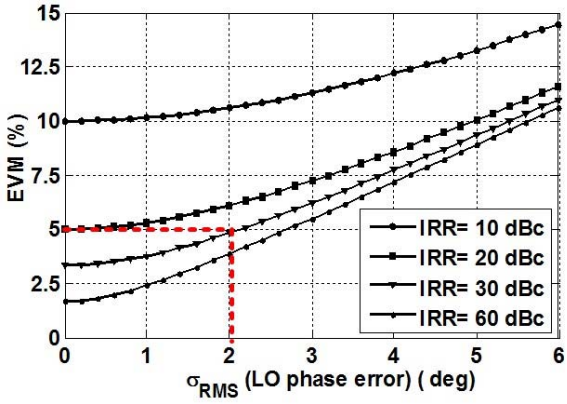


Fig. 3. EVM dependence to rms value of LO PN for various IRRs.

$$\mathrm{EVM} \approx \sqrt{\mathrm{EVM}_{\mathrm{IRR}}^2 + \mathrm{EVM}_{\mathrm{PN}}^2} = \sqrt{\frac{1}{\mathrm{IRR}^2} + \sigma_\phi^2} \qquad (2)$$

where σ_ϕ^2 is the root-mean-square (rms) phase error due to LO PN. Sections II-A and II-B explore how these factors are influenced by a high FBW.

A. Phase Noise

The rms LO phase error is estimated from the PN spectrum. While the oscillator has $1/f^3$ noise at low frequency, the oscillator tracks the PN of the reference within the loop bandwidth of the PLL giving rise to a white PN spectrum at low frequency with magnitude $L(f) = PN_0$ [28]. In the $1/f^2$ region, the PN of the oscillator is not filtered by the PLL. The $1/f^2$ PN of the oscillator depends on the tuning range, specified as an FBW, and characterized by $L(f_m) \propto ((1/Q_L)(f_0/f_m))^2 = \rho((\mathrm{FBW}/f_m))^2$, where f_m is the frequency offset from the carrier frequency f_o, Q_L is the loaded resonator quality factor, and a constant ρ is a proportionality factor in the $1/f^2$ region. To find the rms phase jitter that results from the PLL, the PN is integrated

$$\sigma_\phi^2 = 2\int_0^\infty L(f_m)df_m = 2\mathrm{FBW}\sqrt{\rho PN_0}. \qquad (3)$$

Consequently, we expect the rms phase jitter to be directly proportional to the FBW of the oscillator. For high-FBW applications, e.g., E-band, the large LO tuning range requirement increases the rms phase error. Fig. 3 shows the EVM versus rms PN for different IRR ratios. For 30-dB IRR, the rms phase error should be less than 2° to achieve the required 5% (−26 dB) EVM for 64-QAM and corresponds to an average −124 dBc/Hz at 1-MHz offset according to (3). This places stringent requirements on the oscillator design in order to meet the PN requirement. The earlier work by authors proposed

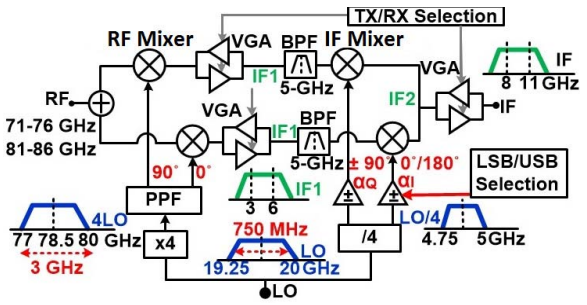


Fig. 4. Proposed bidirectional 71–86-GHz image-selection transceiver uses the sliding-IF Weaver architecture with phase selector in $f_{LO}/4$-path to select the USB and LSB signals.

injection-locked techniques to achieve the tuning range and low PN criteria for 6-Gb/s operation [29].

B. Image-Rejection Ratio

The IRR is related to the amplitude mismatch ΔA and phase mismatch $\Delta\theta$ between the I and Q signal paths [30], [31]

$$\text{IRR} = \frac{1 + 2(1+\Delta A)\cos(\Delta\theta) + (1+\Delta A)^2}{1 - 2(1+\Delta A)\cos(\Delta\theta) + (1+\Delta A)^2}. \tag{4}$$

To achieve an IRR of 30 dB, the phase mismatch must be lower than 1.75° and 3°, respectively, for amplitude mismatch of ±0.5 and ±0.25 dB. Given that $\tau = RC$ defines the time constant of a PPF, the EVM is approximated as

$$\text{EVM} \approx \frac{1}{\text{IRR}(\omega)} = \left|\frac{1-\tau\omega}{1+\tau\omega}\right| \tag{5}$$

where $2(\tau\omega - 1)$ can be approximated as an FBW under negligible PN error. As the FBW increases from 5% to 20%, the EVM increases by a factor of 4 from 1.3% (−37.7 dB) to 5.3% (−25.5 dB). If we account for a 10% RC variation, the EVM increases to roughly 10% (−20 dB) and 4% (−28 dB) for 20% and 5% FBW, respectively. Clearly, large FBW directly translates into large EVM particularly when accounting for process variation.

III. Image-Selection Architecture for High-Fractional Bandwidth

The key insight for the ISA is to use the two RF bands, 71–76 and 81–86 GHz, as images of one another. Two well-known and traditional image-rejection architectures are Hartley and Weaver [31]. The Hartley architecture requires a 90° phase shifter such as RC PPF at the intermediate frequency (IF) signal path and is therefore sensitive to the mismatches and gain flatness over the signal bandwidth. The Weaver architecture removes the Hilbert transform from the RF/IF signal path by adding a second quadrature mixer step. This relaxes the IRR challenges as the quadrature generation is shifted to the LO path and does not affect the direct IF/RF signal path.

Fig. 4 shows the proposed ISA for bidirectional operation. A sliding IF Weaver architecture uses a multiply-by-four to drive the RF mixer and divide-by-four to drive the IF mixer. By changing the quadrature LO phases of either RF mixer, $4f_{LO}$-derived mixer, or IF mixer, $f_{LO}/4$-derived mixer, the LSB or USB are selected. Since the $f_{LO}/4$ mixer operates at much lower frequency, implementing phase inverter in this path shown as α_I and α_Q in Fig. 4 saves overall dc power consumption. The sliding-IF Weaver architecture relaxes the required LO tuning range of the LO centered at 19.625 GHz to be less than 1 GHz, while $4f_{LO}$ covers 77–80 GHz. The first RF mixer in the RX mode moves the RF frequency band to 4.5 GHz over 3-GHz bandwidth, IF1. The second down-converter in the RX mode, IF mixer, mixes the first IF, IF1, with $f_{LO}/4$, and moves the signal to the second IF, IF2, at $f_{IF1} + f_{LO}/4$, to around 10 GHz which is filtered out by another bandpass variable-gain amplifier (VGA) centered at the second IF. The bandpass filter (BPF) is required between the IF mixer and the RF mixer to reject the unwanted mixing product such as the 15-GHz mixing product from the IF mixer in the TX mode.

To analyze the RX mode, the input signal $x_{RF}(t)$ is represented as

$$x_{RF}(t) = A_U\cos(\omega_U t) + A_L\cos(\omega_L t), \tag{6}$$

where A_U, ω_U, A_L, and ω_L, are the amplitude and angular frequency of the USB and LSB components of the input signal, respectively. Multiplying $x_{RF}(t)$ by the multiply-by-four quadrature LO phases, ω_{LO1}, and filtering the high-frequency components through the BPF, the signals are again multiplied by divide-by-four LO quadrature phases at ω_{LO2}, and the IF signals are filtered and summed with weights α_I and α_Q from phase inverter conversion. The inverting I/Q phases of the $f_{LO}/4$ LO path, α_I and α_Q, change between +1 and −1. Based on the phase inverter signs, the USB or LSB is selected as

$$x_{IF}(t) = \begin{cases} \dfrac{A_U}{2}\cos((\omega_U - \omega_{LO1} + \omega_{LO2})t) & \alpha_I = \alpha_Q \\ -\dfrac{A_L}{2}\cos((\omega_L - \omega_{LO1} - \omega_{LO2})t) & \alpha_I = -\alpha_Q \end{cases} \tag{7}$$

where ω_{IF2} centered around 10 GHz is at $\omega_{IF2} = \omega_U - \omega_{LO1} + \omega_{LO2} = \omega_{LO1} + \omega_{LO2} - \omega_L$. A challenge for the Weaver architecture is the secondary image problem, originating when an interferer is located at $2\omega_{LO2} - \omega_{RF} + 2\omega_{LO1}$. This signal will down-convert to $2\omega_{LO2} - \omega_{RF} + \omega_{LO1}$ after the first RF down-conversion in the RX mode, while the in-band input signal will down-convert to $\omega_{RF} - \omega_{LO1}$. As a result, these two signals are images of one another with respect to the LO signal of the IF mixer, ω_{LO2}. This secondary image and the main signal will down-convert to the same IF2 frequency, $\omega_{LO2} - \omega_{RF} + \omega_{LO1}$, after the second down-conversion in the RX mode. Using the BPF centered at 5 GHz between the two mixers mitigates the second image.

For the TX mode, a similar result can be reached and the IF signal will move to the USB or LSB according to

$$x_{RF}(t) = \begin{cases} \dfrac{A_{IF}}{2}\cos((\omega_{IF2} - \omega_{LO2} + \omega_{LO1})t) & \alpha_I = \alpha_Q \\ -\dfrac{A_{IF}}{2}\cos((\omega_{IF2} - \omega_{LO2} - \omega_{LO1})t) & \alpha_I = -\alpha_Q. \end{cases} \tag{8}$$

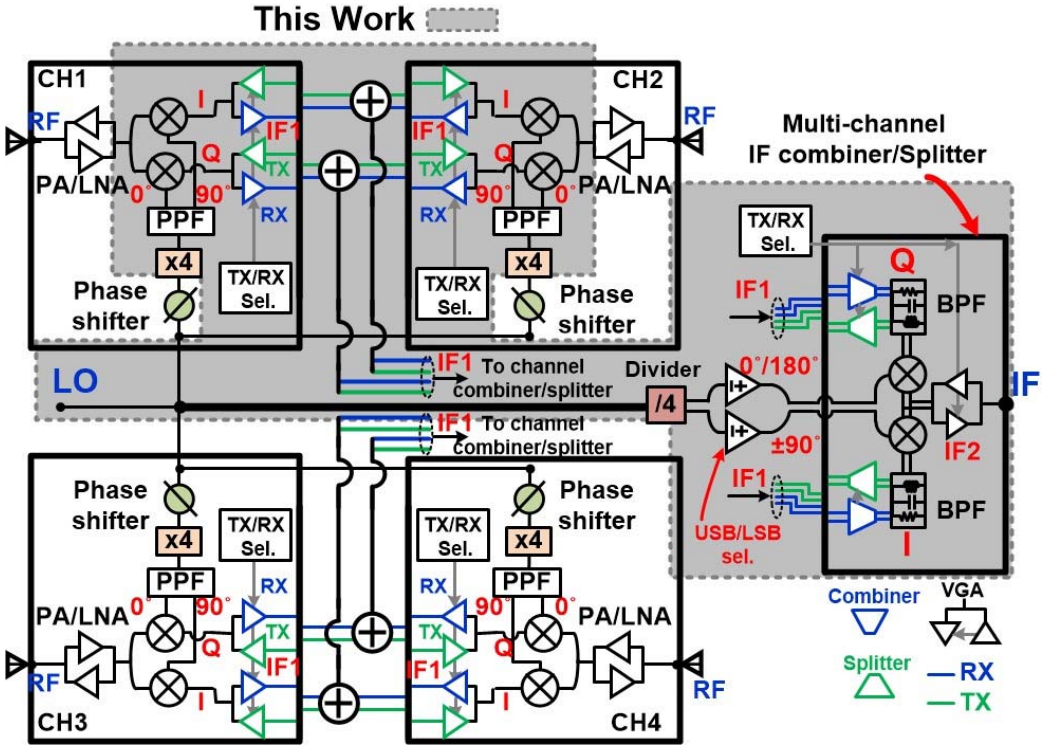


Fig. 5. Proposed block diagram of a scalable phased-array system employing the proposed ISA while sharing the quadrature IF mixer between channels. The implemented block diagram of this paper is composed of two channels without PA/LNA and phase shifters, shown inside the gray box.

In both RX and TX modes, the image selection depends on the gain and phase imbalance in the I and Q paths from (4) and

$$\text{IRR} = \left|\frac{\Delta\alpha + \alpha_I + \alpha_Q}{\Delta\alpha + \alpha_I - \alpha_Q}\right| \approx \left|\frac{2\alpha}{\Delta\alpha}\right| \tag{9}$$

where $\Delta\alpha$ is the gain imbalance between I and Q path and α is the common-mode gain of I and Q path, where $\alpha = (\alpha_I + \alpha_Q/2)$. The IRR in (9) is shown to be improved with gain compensation in the I and Q signal paths, $\Delta\alpha = 0$.

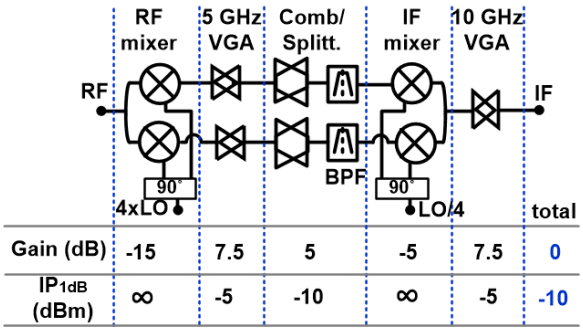
IV. Circuit Implementation

The proposed ISA shown in Fig. 4 is extended to combine signals from two elements, e.g., for multiple input multiple output (MIMO) or phased-array systems. Fig. 5 shows the block diagram for a four-channel system realized here that can employ either IF or LO-path phase shifting technique. Since the required IF and LO bandwidth of the proposed sliding-IF Weaver architecture is narrow, e.g., IF $\sim$ 8–11 GHz and LO $\sim$ 19–20 GHz, the design of the phase shifter either in the IF path or LO path is more power efficient. Specifically, the injection-locked coupled oscillator-based phase shifter implemented in [10] requires a locking range of less than 1 GHz. To verify the proposed image-selection bidirectional scheme, this paper demonstrates two channels as shown in Fig. 5 (gray box). Furthermore, this prototype investigates only the operation of the modulator (up-converter) and demodulator (down-converter) to characterize the ISA, and this paper does not have a PA, LNA, or phase shifter. Earlier work has described the implementation of these blocks [10].

Using two lossy passive mixers in Weaver configuration shown in Fig. 4 in each element requires more power consumption to achieve the desired conversion gain. Therefore, the proposed multi-element ISA shown in Fig. 5 shares the IF up-/down-conversion mixer between each elements. Each element contains a passive RF quadrature mixing block with the variable VGAs centered around 5 GHz, IF1. The generated differential I/Q signals from each element are routed through the chip to the shared multi-channel IF combiner block, where the IF quadrature mixing circuitry and the 5-GHz BPF are located. The I/Q combiner and splitter in the shared multi-channel block interface between the BPF matching network and each element's I/Q VGAs. The second bandpass amplifier at IF2, 8–11 GHz, in the shared multi-channel block provides additional conversion gain to the system while providing matching to the IF port of the chip. Fig. 6 shows the equivalent block diagram and linearity budget of the channel from the RF port to the IF port. For a 10-dBm saturated output power with an average 20-dB gain for the PA or LNA [32]–[38], approximately 0-dB conversion gain is desired for the modulator (up-converter) and demodulator (down-converter), while the circuits compress at -10 dBm. The desired gain and linearity, input $P_{1-\text{dB}}$, of each block are shown in Fig. 6. The IF1 (5 GHz) and IF2 (10 GHz) VGAs have the most stringent linearity requirement which is around -5-dBm input $P_{1-\text{dB}}$. Sections IV-A–IV-D describe each of the building block of the proposed two-element system.

A. Passive RF Mixer and VGA

Fig. 7 shows the RF front end for the E-band. The balun converts the signal to balanced ports at the two ring mixers.



Gain (dB)	-15	7.5	5	-5	7.5	0
IP_{1dB} (dBm)	∞	-5	-10	∞	-5	-10

Fig. 6. Equivalent block diagram of each channel from RF port to main IF port considering the desired gain and linearity requirement of each block.

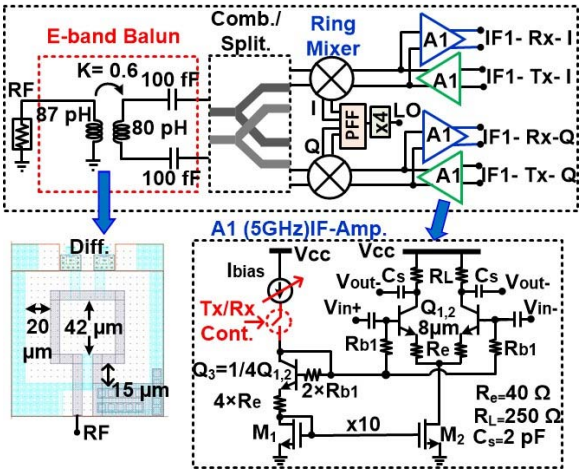


Fig. 7. Block diagram of the *E*-band front end (RF mixer and VGAs) and inset schematic for the 5-GHz IF VGA.

The I/Q ring mixer has two double-balanced passive FET mixers for low RF to LO leakage and even-order harmonic distortion. The passive mixers are inherently bidirectional and drive or are driven by IF VGAs.

The schematic of the IF bidirectional VGA is also shown in Fig. 7 with 3-bit current mirror control, I_{bias}. The amplifier is using heterojunction bipolar transistors (HBTs), $Q_{1,2}$, with emitter degeneration for better linearity. Transistors $Q_{1,2}$ have the emitter length of 100 nm and the width of 8μm. A series TX/RX switch selects the mode of operation for the transceiver [39]. The TX amplifier output is connected to the input of RX amplifier. While the desired amplifier is ON, the complementary amplifier is OFF. For example, the input impedance for the RX mode is shunted by the load amplifier of TX amplifier. When disabled, each amplifier provides high impedance at the common interface node [39]. This amplifier also compensates the I/Q amplitude mismatch caused by quadrature mixer. The 3-bit switchable current mirror, I_{bias}, of current source provides the minimum gain resolution of 0.2–0.5 dB to compensate $\Delta\alpha$ variation shown in (9).

Two quadrature mixers are connected at the RF with a simple *T*-junction layout connected to the balun. The balun uses two top metal layers with 7 μm width, 4 μm thickness, and 42 μm inner dimension. Electromagnetic (EM) simulation

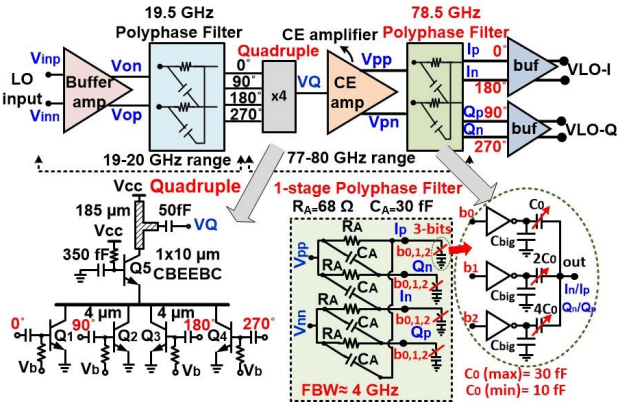


Fig. 8. Multiply-by-four LO generation circuit block diagram with the quadrupler and one-stage PPF schematics.

indicates the overall RF balun loss below 1 dB with the gain imbalance of 0.65 dB and the phase imbalance of 5.4° at 78.5 GHz. The balun size is designed to match the input impedance at the IF port to a 50-Ω impedance at the RF port. The RF port return loss, S_{11}, is be better than 15 dB over 10-GHz bandwidth of the *E*-band. This bidirectional matching also provides a 50-Ω impedance match at the IF port with return loss better than 10 dB at frequencies below 22 GHz. Large-signal simulation predicts 12.5-dB conversion loss and input $P_{1\text{dB}}$ larger than 0 dBm for the front end from the IF1 I or Q ports to the single-ended RF port.

B. Multiply-by-Four Quadrature Frequency Generation

The multiply-by-four LO generation circuit block diagram is shown in Fig. 8. A one-stage PPF centered at 19.5 GHz generates four LO phases to drive the quadrupler. An *LC* tuned load amplifier centered at 19.5 GHz compensates the simulated 9-dB loss of this *RC* PPF. To increase the power gain and provide a differential signal, an additional common-emitter (CE) amplifier using a single-ended to differential balun as a load is used. The differential end of the balun is loaded by the *R* and *C* components of the PPF centered at $4 \times f_{\text{LO}}$, 78.5 GHz. This CE buffer with the associated loss of the balun provides 8-dB gain at 78.5 GHz.

The second PPF is also a single stage that generates quadrature phases at $4 \times f_{\text{LO}}$ from 77 and 80 GHz. To further minimize the I/Q imbalance due to the layout variations, ΔR, and ΔC, each resistor is constructed from three parallel resistors and each capacitor is constructed by two series capacitors [40]. The *RC* extraction of the 78.5-GHz PPF and EM simulations for the routing between the elements indicate a ±5° phase imbalance and ±1.5-dB amplitude imbalance at 78.5 GHz corresponding to an IRR below 20 dB. To improve the IRR to 30 dB, e.g., for 64 QAM, a 3-bit switchable nMOS (n-cap) varactor shown in Fig. 8 is added at each of the positive and negative I and Q outputs of the PPF for amplitude and phase calibration of ±4° phase resolution with ±25° phase tuning with less than 0.25–0.5-dB amplitude mismatch. The differential output signal of PPF is amplified by a 15-dB two-stage amplifier to increase the power gain and the conversion gain of the mixer.

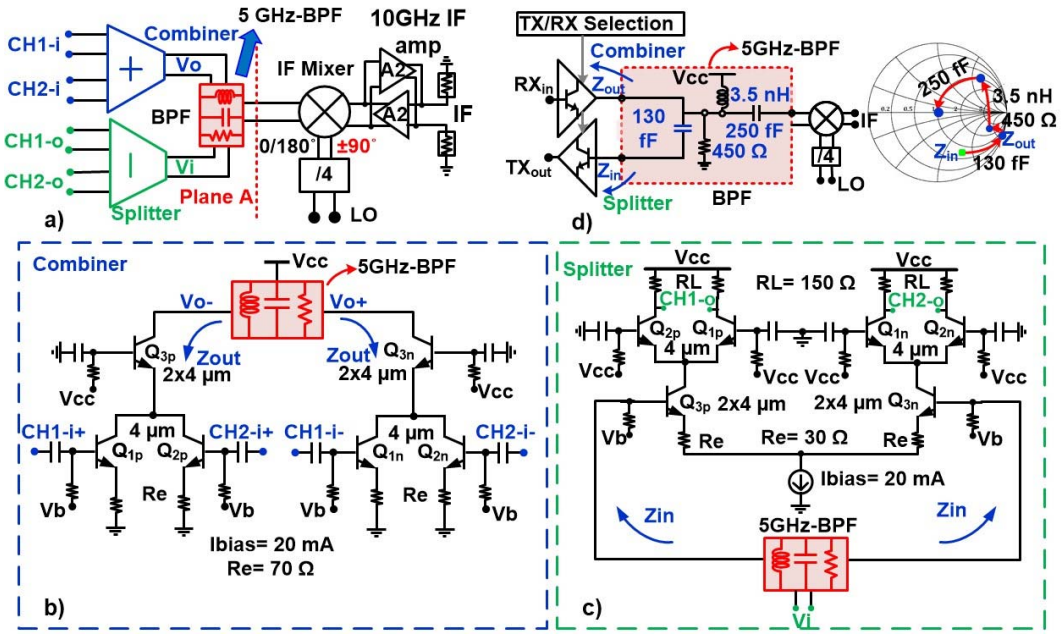


Fig. 9. Quadrature IF mixer with multi-channel IF combiner/splitter. (a) Conceptual block diagram of sharing the quadrature IF mixer between channels. (b) Channel IF-combiner circuitry for RX mode. (c) Channel IF-splitter circuitry for TX mode. (d) Bidirectional and shared BPF design components.

C. Multi-Channel IF Combiner/Splitter

The proposed ISA can share the IF up-/down-conversion quadrature mixer between multiple RF elements in MIMO or phased-array systems. Each element has a $4f_{LO}$-derived quadrature mixer, RF mixer, generating the IF1 signals, and the I and Q signals of IF1 of each elements are combined in the RX mode or split in the TX mode to share the IF conversion and BPF in the image-selection block, as shown in Fig 9(a). The *RLC* BPF is bidirectional and shared between the combiner/splitter to filter unwanted mixing spurs and provide matching between the combiner/splitter and the $f_{LO}/4$-derived quadrature mixer, IF mixer. In the RX mode, the BPF loads the combiner, while for the TX mode, it creates an input matching network for the splitter. In each mode of operation, the complementary circuit is switched OFF and provide high impedance at the interface node. Simulation results predict that 100-Ω differential matching at the interface node, plane A, will result in an optimum condition for conversion gain-linearity tradeoff. Fig. 9(b) and (c) shows the active combiner and splitter circuit schematics, respectively. The combiner uses emitter-degeneration amplifiers, Q_{1-2}, to combine the quadrature IF1 signals from each elements. The output of these amplifiers is summed and buffered to a common-base amplifier, Q_3, which drives the BPF as the load. The splitter schematic is composed of the differential emitter-degeneration amplifier, Q_3, which converts the voltage to current flowing to two cascode CB amplifiers, Q_{1-2}. These cascode CB amplifiers split the current to each elements. The normalized input impedance of the splitter for the TX mode and output impedance of the combiner for the RX mode are shown in Fig. 9(d). A series capacitance of 130 fF will move the splitter normalized impedance to the combiner's output impedance. Consequently, the remaining elements of a BPF can be shared for each mode of operation, TX/RX. The resultant and shared BPF components values, R, L, and C are shown in Fig. 9(d). S-parameter simulations show better than 10-dB return loss at interface node, plane A, over the 3-GHz IF1 bandwidth. The large-signal simulation of multi-channel combiner/splitter indicates around 3.5-dB gain for splitter with -6.5-dB input $P_{1-\mathrm{dB}}$ and 7.2-dB gain for combiner which will be compressed at -5.5-dBm input power.

The IF mixer is also an nMOS ring mixer with an average loss of 5 dB over the IF_1 bandwidth. The 10-GHz bandpass amplifier, A2, is applied after this mixer to further compensate the loss and filter the unwanted image and mixing spurs. Moreover, this amplifier provides matching at the IF port of the chip. Fig. 10 shows the bidirectional operation of this bandpass active filter with each amplifier's schematic. The circuit employs Miller feedback to improve the linearity of circuit and provide resistive matching at another port of mixer. For example, for the TX mode, a 50-Ω input impedance at the IF port is realized with a 150-Ω feedback resistance for the TX mode. The input return loss is better than 10 dB within 3–22-GHz bandwidth. The large-signal simulations for each mode of operation shows an average gain of 6 dB with input $P_{1-\mathrm{dB}}$ of -8.5 dBm.

Large-signal simulation for one channel from IF port to RF port is shown in Fig. 11 at 73.5 GHz. The VGAs are tuned to the maximum gain-state providing the maximum P_{sat} for both TX or RX modes. The maximum simulated conversion gain of the TX mode and RX mode is around 4 and 2.5 dB, respectively. This corresponds to -12-dBm input $P_{1-\mathrm{dB}}$ for the TX mode and around -10-dBm input $P_{1-\mathrm{dB}}$ for the RX mode which is around the desired calculated input $P_{1-\mathrm{dB}}$ shown in Fig. 6. By changing the VGA current states from the low to high, the simulated system provides the minimum and maximum gain of -1.6–4 dB for the TX mode and the

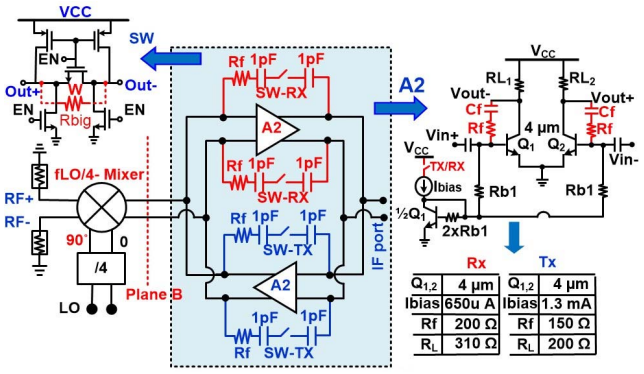


Fig. 10. Bidirectional TX and RX configuration of the second IF bandpass active filter with its amplifier's schematic.

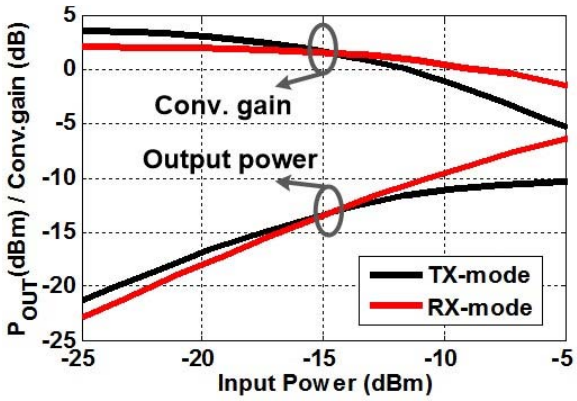


Fig. 11. Large-signal simulation of one channel for TX and RX modes while setting the VGAs for maximum gain state for both modes and only changing the enabling TX/RX switch.

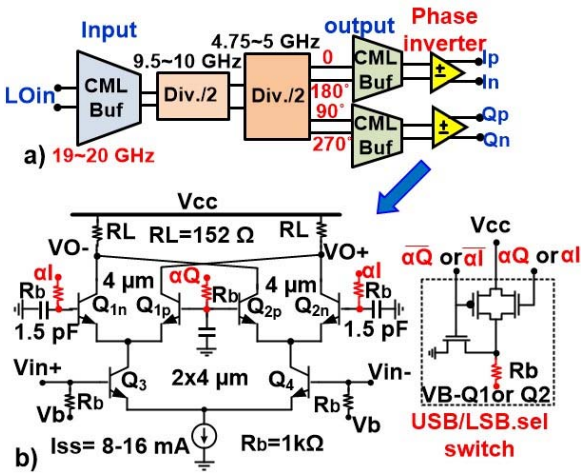


Fig. 12. LO generation circuitry of IF mixer. (a) Block diagram of D/4 quadrature frequency generation path. (b) USB/LSB selection, phase inverter multiplexer, schematic.

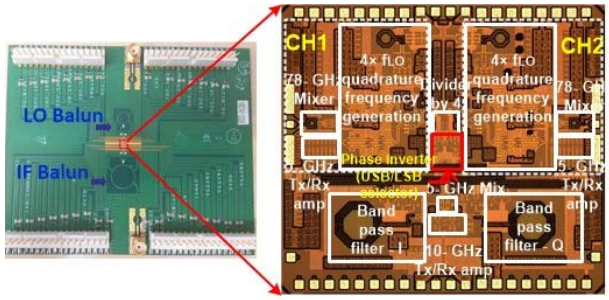


Fig. 13. Chip micrograph and board level assembly.

maximum and minimum gain of −3–2.5 dB for the RX-mode. The simulated conversion gain variation over bandwidth is less than ±0.4 dB in each VGA state. The simulated IRR is also around 29 dB corresponding to 2° phase imbalance and 0.25-dB amplitude imbalance at $4f_{LO}$ quadrature mixer LO path.

D. IF Mixer LO Generation and USB/LSB Selection

Fig. 12(a) shows the block diagram of the quadrature LO frequency generation for the IF mixer. The LO generation block for the IF mixer consists of divider-by-four (D/4) block and phase inverter to select the upper or lower band. The D/4 is composed of two cascaded D-latch current-mode logic (CML) blocks with two input and output buffers operating at 19.5 and 4.875 GHz, respectively. The phase inverter illustrated in Fig. 12(b) is a phase multiplexer composed of cascode amplifiers with CE transistor. The USB/LSB mode is selected by switching the base voltage of four common-gate amplifiers to the ground or V_{cc}. The phase inverter provides a variable gain of 17–23 dB based on the dc current flowing through the current mirror to compensate the I/Q amplitude mismatch and reduce the third-harmonic tone, $3f_{LO}/4$, generated from a D/4 path. The third-harmonic tone produces undesirable spurs that fall into the IF2 band. For example, an 85-GHz input RF frequency, using 20-GHz LO frequency ($4f_{LO} = 80$ GHz, $f_{LO}/4 = 5$ GHz, and $3f_{LO}/4 = 15$ GHz) will move the mixing spurs products generated from $f_{LO}/4$ and $3f_{LO}/4$ to the same IF_2 frequency as $f_{RF} - 4f_{LO} + f_{LO}/4$ and $f_{RF} - 4f_{LO} - 3f_{LO}/4$ which is 10 GHz. To reduce the third-harmonic tone effect, the phase inverter is operated in a linear region at the expense of overall conversion gain. Large-signal simulations of the output power and the third-harmonic tone illustrate that biasing the transistor with lower current reduces the gain from 23 to 17 dB but improves the third-harmonic suppression by 15 dB.

V. Measurement Results

The chip micrograph mounted on a PCB board is shown in Fig. 13. The system includes two channels implemented in a 90-nm SiGe BiCMOS process using 2-V power supply. Each channel contains a separate 71–86-GHz I/Q RF mixer, 4 × LO quadrature generation chain, and 5-GHz bidirectional VGAs. The 5-GHz I/Q IF signals of each channel are combined and connected to the 5-GHz BPF and 5-GHz I/Q IF mixer. The chip occupies 2.1×1.9 mm^2 including pads and ESD. The dc pads, LO, and IF pads are wire-bonded to the PCB, while the first layer of PCB uses 10-mil thickness Rogers 5880 material for the high-frequency signal routing, i.e., IF (8–11 GHz) and LO (19–20 GHz). As the IF and LO ports of the chip

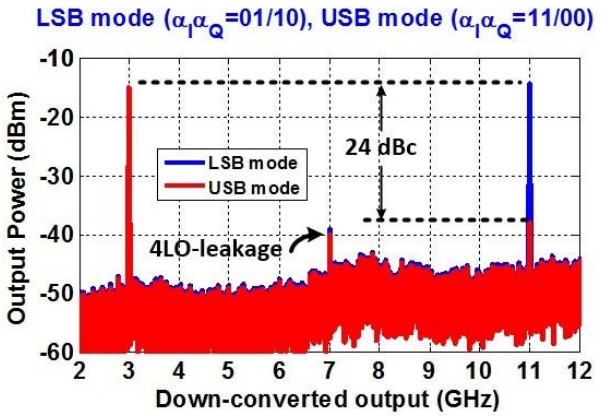


Fig. 14. Image-selection performance—the de-embedded output spectrum in the TX mode for USB mode setting ($\alpha_I\alpha_Q = 00/11$) and LSB mode setting ($\alpha_I\alpha_Q = 01/10$) with $f_{\rm IF} = 9$ GHz and $f_{\rm LO} = 20$ GHz correspondent to $f_{\rm RF\text{-}USB} = 84$ GHz, $f_{\rm RF\text{-}LSB} = 76$ GHz, $4f_{\rm LO} = 80$ GHz, and 87-GHz LO frequency of down-converted external mixer.

are differential, hybrid baluns centered at 8.5 GHz for IF and 19.5 GHz for LO are designed on the board with less than 3-dB loss and under 1-dB amplitude imbalance and 8° phase imbalance within 3-GHz bandwidth. All IF, LO, and RF ports of the chip are matched to 50 Ω. The RF signal chain consumes between 120 and 150 mW, where 78 mW is consumed by the VGAs and around 72 mW is consumed by combiner/splitter. The 4 × LO and LO/4 circuitry consumes 182 and 68 mW, respectively.

A. TX Measurements

To demonstrate image selection, the chip is configured for either USB ($\alpha_I\alpha_Q = 00/11$) or LSB ($\alpha_I\alpha_Q = 01/10$) modes. The TX spectrum is shown in Fig. 14 for USB and LSB modes with phase inversion in the image-selection circuit. The IF and LO signals of chip are located at 9 and 20 GHz, respectively, equivalent to 84 GHz at USB and 76 GHz at LSB and $4f_{\rm LO}$ leakage signal at 80 GHz. Using the 87-GHz LO of the down-converted external mixer in the measurement setup will move the USB, LSB, and $4f_{\rm LO}$ leakage signals to 3, 11, and 7 GHz, respectively. The LO leakage and IRR ratio in Fig. 14 are around 23 and 24 dB, respectively.

The output power and conversion gain as the input power is swept for LSB and USB modes in the TX mode were previously reported in [25]. For an approximate 2.5-dB conversion gain for both LSB and USB modes, the transmitter compresses at an input power level around −15 dBm. For this equal conversion gain state, the measurements shows the IRR is 25 dB for the LSB mode and 23 for the USB mode without optimizing the calibration conditions (VGA/PPF). The performance for minimum and maximum VGA gain is presented in Fig. 15. The conversion gain are shown in Fig. 15(a) and compared with simulations. The simulated conversion gain for minimum and maximum VGAs setting are −1.6–4 dB, respectively, with less than ±0.4-dB variation across the two bands. For the measurement results, the gain variation in the LSB mode is less than ±0.4 dB at the minimum and maximum

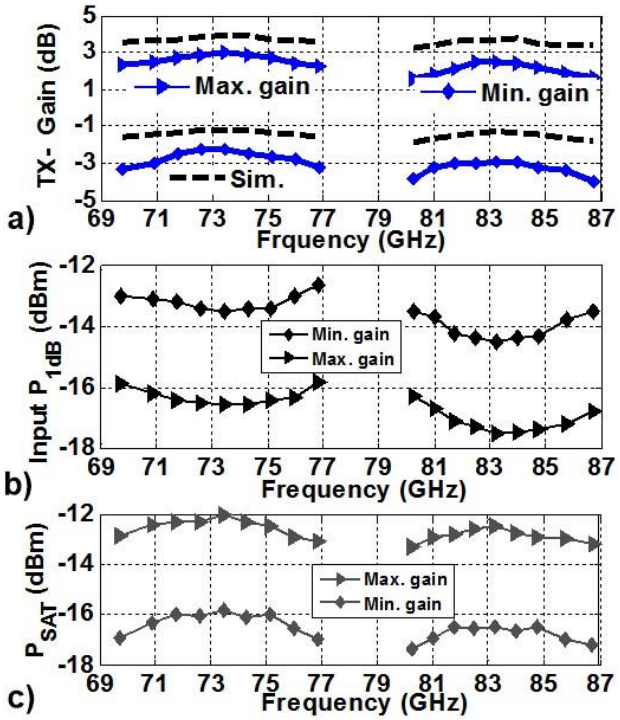


Fig. 15. Transmitter measured performance versus frequency for the maximum and minimum states of VGA settings. (a) Conversion gain. (b) Input $P_{1-\rm dB}$. (c) Saturated output power.

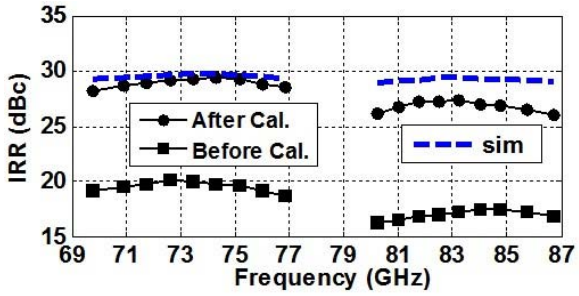


Fig. 16. Before and after calibration performance (3-bit VGAs and 3-bit varactors) for IIR versus frequency.

VGA power levels, while the gain variation is ±0.5 dB in the USB. Fig. 15(b) shows the input $P_{1-\rm dB}$ variation over frequencies for the USB and LSB of the two VGA states. The $P_{1-\rm dB}$ values over the entire USB and LSB band vary less than ±0.75 dB for the maximum VGA state and less than ±1 dB for the minimum VGA state. The saturated output power of the TX front end varies from the minimum of −17 dBm to the maximum of −12 dBm in Fig. 15(c). $P_{\rm sat}$ varies by less than ±0.6 dB for both VGA states. Note that this paper does not have any PA, and therefore, $P_{\rm sat}$ can be amplified by 20 dB using an E-band PA [32]–[35]. It should also be noted that the E-band/W-band PA in [32]–[35] or LNA [36]–[38] has less than ±1.5-dB gain variation, $P_{1-\rm dB}$, and $P_{\rm sat}$ over the 3-dB bandwidth.

The IRR for both USB and LSB modes is plotted over the frequency band in Fig. 16 before and after calibration. The one-stage PPF provides around 20-dB IRR which results

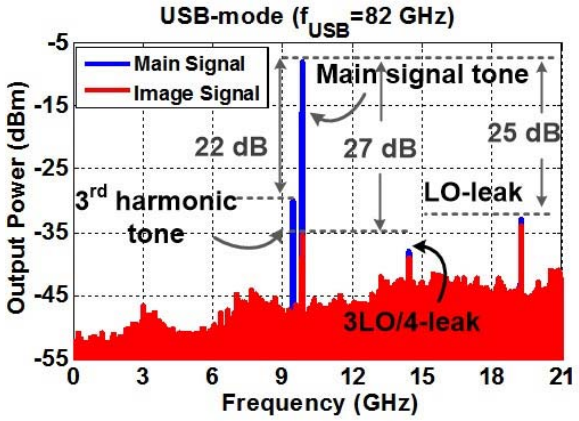


Fig. 17. Output spectrum of the receiver for USB mode with f_{USB} at 82 GHz and f_{LSB} at 72 GHz using $f_{\mathrm{LO}} = 19.25$ GHz.

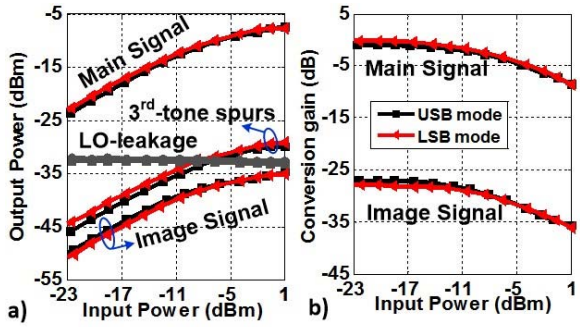


Fig. 18. Large-signal measurement result for receiver for 73 GHz as LSB and 83 GHz as USB. (a) Main signal, third-harmonic tone, image signal output power, and $4f_{\mathrm{LO}}$ LO-leakage power versus input power. (b) Main signal and image signal conversion gain versus input power.

in below 7.5% (−22.5 dB) EVM under 2° LO phase error without calibration. The amplitude and phase mismatch are compensated using the 3-bit variable caps and VGAs and the IRR at 73 GHz increases from 19 to 29 dB. At 83 GHz, the IRR increases from 17 to 27 dB, as shown in Fig. 16. The IRR measurements shows that these results provide reasonable agreement with simulation in the LSB mode under the assumption of 2°/0.25-dB phase and amplitude imbalance. The LO leakage of the transmitter that arises from the multiplication by four path, $4f_{\mathrm{LO}}$, for before and after calibration are also measured. The LO leakage at 73 GHz improves from 14 dBc before calibration to 25 dBc after calibration, while at 83 GHz it improves from 12 to 24 dBc.

B. RX Measurement

The measured output spectrum of the receiver is shown in Fig. 17 in the USB mode for RF input at 82 GHz and LO signal at 19.25 GHz. Therefore, the first IF (IF1) signal will be located at 5 GHz and will mix with $f_{\mathrm{LO}}/4$ at 4.8 GHz and $3f_{\mathrm{LO}}/4$ harmonic tone at 14.4 GHz to generate the second IF (IF2) at 9.8 GHz and the third-harmonic mixing tone at 9.43 GHz. With USB/LSB selection, the desired RF channel will move to $f_{\mathrm{IF1}} + f_{\mathrm{LO}}/4$, while the image band is at $f_{\mathrm{IF1}} - f_{\mathrm{LO}}/4$ as described in Section III. A bandpass amplifier

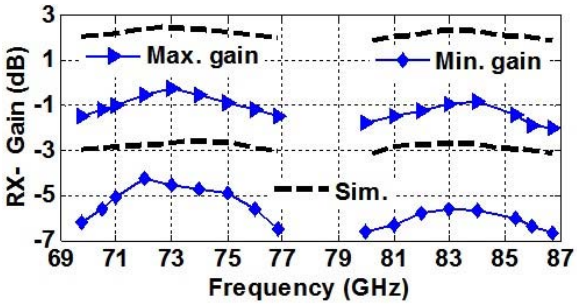


Fig. 19. Measured receiver conversion gain performance versus frequency for the maximum and minimum states of VGA settings.

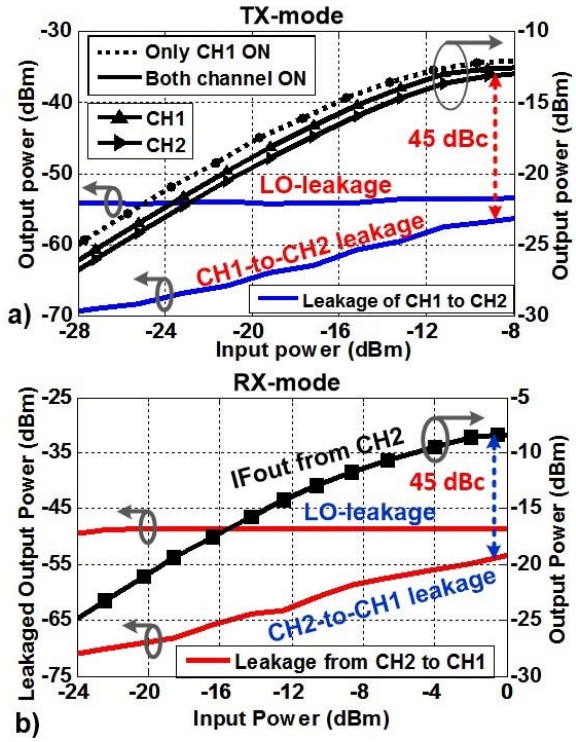


Fig. 20. Measurement results for channel-to-channel isolation performance for (a) TX mode while CH1 is ON and the leakage tones to CH2 are considered and (b) RX mode while CH2 is ON and the leakage tones to CH1 RF port are considered.

after the second down-conversion, A2, operating at center frequency of 10 GHz, filters out the second conversion term, $f_{\mathrm{IF1}} - f_{\mathrm{LO}}/4$. Therefore, to measure the IRR performance of the RX mode, the image band is provided to the front end while setting to the complementary state. For example, a signal in the LSB band located at 72 GHz is measured, while the front end is set to the USB mode and the LSB tone at 72 GHz as an image will move to $(f_{\mathrm{IF1}} + f_{\mathrm{LO}}/4)$ which will not be filtered out by the bandpass amplifier, A2. Fig. 17 indicates this as the red plot, where the RF input at 72 GHz will down-convert at 9.8 GHz with 27-dB filtering effect arised from the calibration circuit in the RX mode. The RX system also provides better than −25-dBc LO leakage. However, the mixing spurs at $3f_{\mathrm{LO}}/4$ are rejected by only 22 dBc, which can be suppressed more than 22 dB at the expense of system overall conversion gain.

The receiver large-signal performance for the USB signal at 83 GHz and LSB signal at 73 GHz is shown in Fig. 18 versus input power. The maximum output power at the IF port of both USB and LSB modes is around −7.7 dBm, as shown in Fig. 18(a). The LO leakage, D/4 third-harmonic tone mixing spur, and IRR are around 25 dBc, 22 dBc, and 27 dB, respectively. The conversion gain of the main and image signal is shown in Fig. 18(b). The conversion gain performance over the frequency for the maximum and minimum states is shown in Fig. 19 and compared with the simulation. The simulated conversion gain for the two VGA states is −3 dB for the minimum state and 2.5 dB for the maximum state. The conversion gain measurement indicates an averaged value of −5.5 dB for the minimum state and the −1 dB value for the maximum state. The measured gain variation is less ±0.75 at the minimum and maximum VGA power levels in the LSB band, while the gain variation is ±0.8 dB in the USB band. The conversion gain variation over the entire the 71–86-GHz band is around ±1 dB for the RX mode. The measurement result for the maximum output power of the IF port shows an average power value of −12.5 dB of IF Psat for the minimum state and an average power level of −8 dBm for the maximum state. The amount of power variation is less than ±0.5 dB for each band and ±1 dB for entire band. In addition, measurement result shows that the input $P_{1-\mathrm{dB}}$ of the receiver has the average magnitude of −10.5 dBm for the maximum gain state, which improves to the averaged value of −8 dBm for the minimum gain state. The input $P_{1-\mathrm{dB}}$ variation over entire band is less than ±0.75 dB. The noise figure (NF) is also measured for both states, which changes from $NF_{\min}$ of 14 dB for the minimum gain state to $NF_{\min}$ of 20 dB for the maximum gain state. The third-order intermodulation (IM) characteristic was also measured with a two-tone test and the IIP3 is approximately 0 dBm at 73.5 GHz.

C. Channel-to-Channel Isolation

Fig. 20(a) and (b) shows the channel-to-channel isolation for the TX and RX modes, respectively. For the TX mode, the CH2 was probed and its output power was measured, while it was ON and OFF. When both channels are ON, the maximum output power is reduced by 1 dB, as shown in Fig. 20(a). When one channel is OFF and the other is ON, the output RF signal and the $4f_{\mathrm{LO}}$-leaked signals at the RF port of the ON channel leak to the other channel's RF port. Fig. 20(a) also shows the leaked power of CH1 as ON channel to CH2 as OFF channel in the TX mode versus input power. The isolation is around 40 dBc for $4f_{\mathrm{LO}}$ leakage and 45 dBc for main signal leakage. Fig. 20(b) shows the output power variation of CH2 versus input power as the ON channel in the RX mode when CH1 is OFF. The amount of leaked power, RF and $4f_{\mathrm{LO}}$ signals, to the OFF channel's RF port, CH1 is also shown in Fig. 20(b). The RF port leakage to the OFF channel is around 45-dBc rejection.

D. QAM Modulation Measurements

The EVM measurement setup is shown in Fig. 21. Modulated signals are generated with a 65-GS/s arbitrary waveform generator, Keysight M8195, and applied to the IF port of the chip. The down-converted RF output signal is captured using 6-GHz real-time oscilloscope, DSO80604b. The output data were analyzed using the 89600 VSA software to characterize the waveform. Fig. 22(a) shows the output measurement spectrum for the modulated signal at f_{IF} of 7.875 GHz with the symbol rate of 1.25 GHz (7.5 Gb/s) for 64 QAM for two USB and LSB modes changed by only 1 bit of α_I, α_Q in the phase inverter block. The prototype IC exhibits a flat and constant power over the 1.25 GHz bandwidth for both modes. $f_{\mathrm{LO}} = 19.5$ GHz converts the IF signals to the RF frequency of 75 GHz in LSB and 81 GHz for USB by changing the phase selection. Using a 79-GHz external down-converter mixer moves the USB and LSB to 2 and 4 GHz, respectively. Without calibration, the EVM is 4.65% (−26.6 dB) for the USB and 4.32% (−27.3 dB) for the LSB with an averaged IRR of 20 dB and LO leakage of 15 dBc. Fig. 22 (b) shows that the calibration circuitry, including the 3-bit VGAs and 3-bit varactors in PPF, can improve the LO leakage and image rejection by 10 dB over the 1.25-GHz bandwidth in the LSB mode. With calibration, the IRR is improved to an average of 30 dB and the LO leakage to 25 dBc. The EVM improves from 4.32% (−27.3 dB) for 7.5 Gb/s in the LSB mode to 3.1% (−30.2 dB).

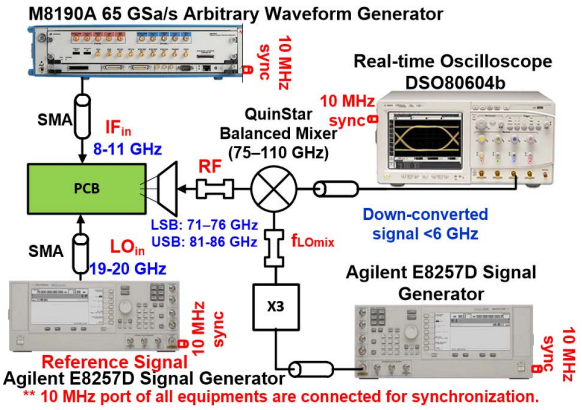


Fig. 21. Transmitter QAM modulation setup.

The output EVM for 16 QAM and 64 QAM with 1-GHz symbol rate was measured by changing the IF from 8 to 11 GHz and LO signal from 19 to 20 GHz for both LSB and USB. The variation on EVM across frequency is shown in Fig. 23 and indicates less than ±0.5 dB either the LSB or USB and less than ±1 dB EVM variation over entire band. The maximum achievable symbol rate for 16 QAM was 3 GHz and for 64 QAM was 2 GHz. Fig. 24(a) and (b) shows the result for the output EVM versus data rate for two conditions of IRR and $4f_{\mathrm{LO}}$ leakage. For the un-calibrated IRR of 20 dB and $4f_{\mathrm{LO}} = 15$ dBc, the maximum data rate for 16 QAM is 12 Gb/s with the EVM of 11% (−19.2 dB). If restricted to EVM below 5% (−26 dB), the maximum data rate cannot exceed 6 Gb/s for 16 QAM. For 64 QAM, the maximum data rate is 9 Gb/s for EVM below 4% (−28 dB). Optimizing the calibration condition for IRR

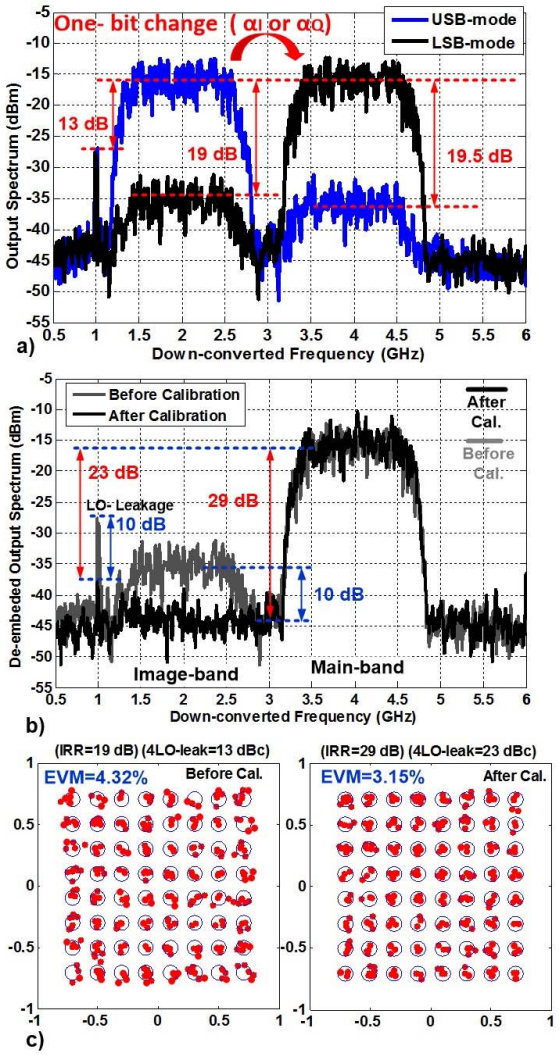


Fig. 22. TX modulation with the symbol rate of 1.25 GHz at 64 QAM (7.5 Gb/s) for $f_{IF} = 7.875$ GHz and $f_{LO} = 19.5$ GHz ($4f_{LO} = 78$ GHz) corresponding to $f_{LSB} = 75$ GHz and $f_{USB} = 81$ GHz with the setup down-converter mixer LO of 79 GHz. (a) Modulated output spectrum for USB and LSB modes by only 1-bit change of phase inverter, α_I, α_Q. (b) Calibration effect on TX modulated signal in the LSB mode. (c) EVM enhancement after optimized calibration.

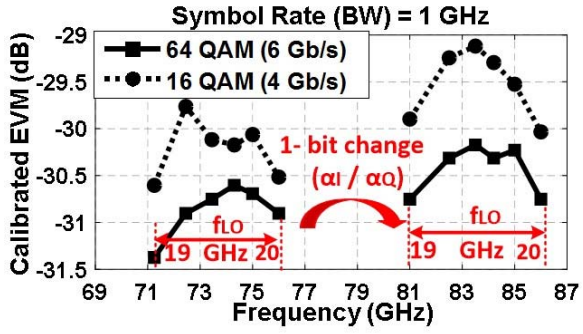


Fig. 23. Calibrated EVM effect for 16 QAM and 64 QAM versus frequency, which is tuned with $f_{LO} = 19$ to 20 GHz ($f_{IF} = 8$–10 GHz) and 1-bit phase inverter change for USB and LSB selection with the modulated bandwidth of 1 GHz.

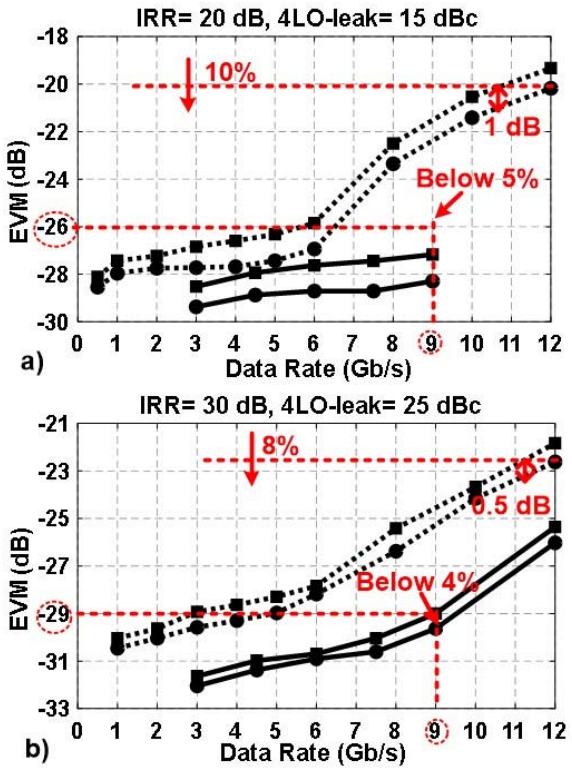


Fig. 24. EVM versus data rate for two sets of IRR and LO leakage. (a) Un-calibrated condition of IRR = 20 dB and 4LO-leakage 15 dBc. (b) Optimized calibration condition of IRR = 30 dB and 4LO-leakage 25 dBc.

of 30 dBc and $4f_{LO} = 25$ dBc improves the EVM of the highest data rate. For 16 QAM, the maximum data rate is 12 Gb/s with 8% (−22 dB) EVM, while 64 QAM reaches 12 Gb/s with 5.5 % (−25.2 dB) EVM.

E. Performance Summary and Comparison

A comparison of this paper with the other recent quadrature *E*-band or *W*-band modulators is shown in Table I. This paper reports the up-converter/down-converter independent of the RF front-end LNA and PA. The measurements indicate that this paper requires the lowest LO tuning range to cover the 10-GHz RF band at 71–76 and 81–86 GHz; when normalized to the RF band, the LO tuning range is 30%. Furthermore, the reduced tuning range demonstrates the circuit's capability to achieve the lowest EVM for both 16 QAM and 64 QAM as well as the highest data rate, 12 and 9 Gb/s, respectively compared with earlier work. It also demonstrates the advantage of low conversion gain variation over the RF bandwidth.

Wideband quadrature LO frequency generation blocks for the I/Q up-converter/down-converter tend to dominate amplitude and phase imbalances that result in conversion gain variation. The E-band/W-band PA in [32]–[35] or LNA [36]–[38] has less than ±1.5-dB gain variation, OP_{1-dB}, NF, and P_{sat} over the 3-dB bandwidth. Consequently, the larger gain variation for the systems in [6], [9], and [10] results from the wideband LO generation circuitry, and this paper indicates that better EVM results from architectures that alleviate the FBW requirements of the LO.

TABLE I
COMPARISON SUMMARY WITH OTHER *W*-BAND AND *E*-BAND TRANSCEIVER

	[6]	[8]	[10]	[7]	[9]	[5]	This Work
Frequency (GHz)	70-90	71-86	71-76 81-86	64-84	70-100 #(75-95)	71-76 81-86	71-76 81-86
Function	RX	TX	TX/RX	TX	TX/RX	TX/RX	TX/RX
Architecture	Heterodyne	Direct Conversion	Heterodyne	Sub-harmonic	Direct Conversion	Sliding-IF Heterodyn	Sliding-IF Weaver
LO-tuning range (GHz)/Normalized to RF Band (%)	>25 125%	>15 >100%	>10 >100%	>20 >100%	>20 > 100%	>14 >140%	**3** **30%**
Conversion Gain per element (dB)	**>19	**<11	**>20	0	**>25	**>36	TX:-2.5 to+3 RX: -4 to 0
Gain Variation (dB)	0*8	0*4	0*>10	±1	0*>10	N/A	**TX:±0.75 RX: ±1**
IRR (dB)	N/A	36-40	N/A	40	N/A	N/A	30
Constellation (Data rate/EVM) (Gb/s/dB)	N/A	64 QAM (4.5 /-24) 16 QAM (14/-18)	256 QAM (6 /-30.5)	256 QAM (0.04 /-34)	1*16 QAM (10 /-22) 32 QAM (8.75/-24)	128 QAM (0.7 /-30.5)	**64 QAM (9 /-28.3) 16 QAM (12/-22)**
DC Power (mW) per channel	2*760	3*102	RX: 286 TX: 386	3*40.8	500	RX: 600 TX: 1800	4*400
LO block **Mixer & IF amp** **RF block (PA or LNA)**	5*611 82.5 66	N/A N/A N/A	89 75 PA: 225 LNA: 125	N/A 40.8 N/A	N/A N/A N/A	262 >220 PA: 800 LNA: 114	6*250 7*150 N/A
Technology	0.35 µm SiGe	40 nm GP CMOS	90 nm SiGe	65 nm CMOS	0.18 µm SiGe	0.13 µm SiGe	90 nm SiGe

** containing PA for TX or LNA for RX transceiver. # 3-dB bandwidth is 75-95 GHz. 0* The maximum PA or LNA gain variation is ±1.5dB within 3dB-bandwidth. 1* whole wireless link. 2* with VCO and prescalor. 3* w/o LO frequency generation block. 4* 250 mW for LO-path. 5*: quadrature VCO: 462 mW, frequency prescalar: ~150 mW. 6* Multiplier x4 : 182 mW, Div/4: 68mW. 7* Combiner/splitter: 72 mW, modulator and VGAs: 78 mW.

VI. CONCLUSION

This paper presents a high-FBW, *E*-band transceiver architecture that requires only 3-GHz LO tuning range at the mixer to cover MMW bands between 71–76 and 81–86 GHz. The architecture employs a sliding-IF Weaver scheme, which to the best of our knowledge, has not been demonstrated at MMW frequency bands. Reduced LO tuning range relaxes the constraints on quadrature frequency generation and mitigates the amplitude/phase imbalance originated from the circuits, such as a PPF. The modulator (up-converter) and demodulator (down-converter) exhibit a relatively flat conversion gain, output power, and input/output $P_{1-\mathrm{dB}}$ over entire wideband operation, 71–86 GHz. A data rate of 12 and 9 Gb/s is achieved with 64-QAM, while the EVM is only 5.5% (−25.2 dB) and 4% (−28.3 dB), respectively. The architecture can be applied to MIMO and phased-array systems.

ACKNOWLEDGMENT

The authors would like to thank Nokia for the support of this research and, in particular, T. Kovarik for the support. They would also like to thank N. Rostamyan for his help in quadrature-amplitude modulation measurements.

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