Design of 1.8-mW PLL-Free 2.4-GHz Receiver Utilizing Temperature-Compensated FBAR Resonator

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***Abstract*— This paper presents a 1.8-mW 2.4-GHz channelized receiver for ISM-band applications. Unlike traditional ISM-band radios which typically require a phase-locked loop (PLL) for channelization, we propose a modified sliding-IF receiver architecture with a suitable local oscillator (LO) frequency plan utilizing a temperature-compensated thin film bulk acoustic-wave resonator (FBAR). This strategy completely eliminates the need for a PLL by directly dividing down the fixed FBAR oscillator frequency. An inductor-less current-reuse balun LNA is proposed allowing a low-power wideband matching as well as noise cancelling. The frequency conversion is achieved by a hybrid mixer, which stacks a switching mixer on a switched-g_m mixer for current reuse. It also features good voltage headroom and common-mode noise rejection. The FBAR-based Colpitts oscillator achieves the phase noise of −144 dBc/Hz at 3.5-MHz offset. The measured RX gain, noise figure, and in-band IIP_3 are 57.8 dB, 15.7 dB, and −18.5 dBm, respectively, without external crystal and on-chip inductors, which allows us to reduce the size and weight of the receiver system. It dissipates 0.86 mW (RX) and 0.92 mW (LO) from a single 1-V supply.**

***Index Terms*— 2.4 GHz, balun LNA, channelization, Colpitts oscillator, current reuse, image rejection, low power, mixer, noise cancelling, phase-locked loop (PLL) free, resonator, sliding IF, temperature compensated, thin film bulk acoustic-wave resonator (FBAR), wideband.**

I. Introduction

RECENTLY, low power, short-range ISM-band transceivers have become extremely important in enabling new applications and have become highly successful commercially. The new Internet of Things (IoT) wireless connectivity IC market is expected to increase 54% by 2020, which is mostly shared by a number of technologies including the IEEE 802.15.4, ZigBee and Bluetooth low energy [1]. The main challenge is that the battery life is limited due to the power-hungry RF transceiver which consumes almost 90% of the total battery energy. For instance, a typical always-on ZigBee radio can only operate less than an hour on an energizer 337 coin–cell battery [2]. Beside the severe power budget, many design tradeoffs are involved for RF transceiver such as input matching, noise figure (NF), linearity, area as well as the number and cost of external components.

Generally, traditional short-range ISM-band radios require a phase-locked loop (PLL)-based frequency synthesizer for channelization across the band of interest [3]–[6]. Those radios show excellent in-band phase noise with the cost of large amount of power consumption due to the unavoidable RF feedback loop. Also, the external quartz is necessary as the reference of the PLL, incurring additional area and cost. A bulk acoustic-wave (BAW)-based 2.4-GHz ZigBee receiver saves power and area by eliminating the off-chip quartz with super-high IF architecture [7]. However, owing to the limited turning range of BAW oscillator, an 8.2-mW low-frequency *LC*-PLL is necessary for channel select tuning. To remove the power-hungry PLL, Heragu *et al*. [8] adopt a BAW-based digital-controlled oscillator and a BAW-based RF filter with small frequency offset to achieve an 80-MHz turning range. Several BAW resonators are nevertheless necessary to span the bandwidth increment, and several constrains limit its power consumption: 1) the power consumption of the receiver should benefit by eliminating the PLLs, but the super-high-frequency RF and IF operation increases the overall power consumption again and 2) owing to the intrinsically high-Q of the BAW resonators, the channel selective filter shows a "round" bandpass shape, which will increase the in-band ripple for wideband applications such as ZigBee.

Another technique for saving power is the circuit-reuse among several devices and sub-blocks. The LNA-mixer-voltage-controlled oscillator (VCO) cell [9], [10] has been proposed to save power by sharing the current between the RF blocks, as shown in Fig. 1(a). However, the I/Q generation is embedded in the RF by using capacitive degeneration. The I/Q accuracy is quite sensitive to process variation. Lin *et al*. [11] proposed an RF-to-baseband current-reuse structure by merging the baseband filters into the current-reuse path for saving power, as shown in Fig. 1(b). It also benefits from better linearity due to the low-voltage swing at the internal node. However, it relies on stacked devices which result in limited

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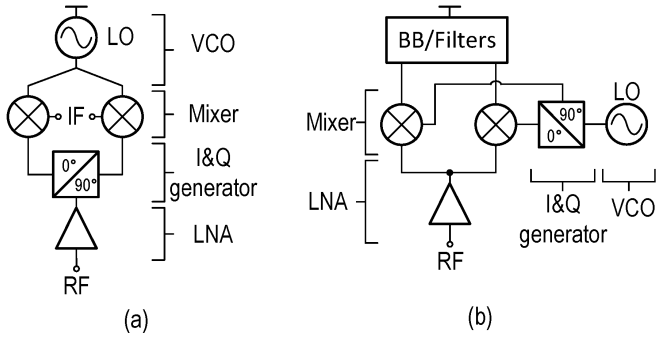


Fig. 1. (a) LMV cell. (b) RF-to-baseband current-reuse receiver.

voltage headroom for each device. Also, like most of low-IF receivers, high-frequency quadrature local oscillator (LO) generation increases the total power consumption.

The 2.4-GHz receiver in [12] validates the minimum supply voltage down to 0.18 V. It can tolerate 50% variation of its energy-harvesting supply up to 0.3 V. However, like most ultralow-voltage receivers, a micropower manager is required to provide multiply internal voltages. Startup time ($>200\ \mu$S) may be an problem while launching connections for low-duty-cycle IoT devices. At the same time, channelization circuit which may eventually increase the total power consumption was not mentioned in the literature. A blocker-tolerant ADPLL-based RX with hybrid loop is proposed in [13], which achieves over 20 dB 2nd/3rd ACR without any external RF filters. However, the analog RX chain still consumes a total power of 5.5 mW. The sub-sampling technique in [14] saves a lot of power and chip areas because of the digital IF processing. This technique is also compatible with technology scaling. Heragu *et al.* [8] demonstrate a film bulk acoustic-wave resonator (FBAR) and sub-sampling co-design technique. Integer-N dividers are used to generate the channel selection LO (approximately 80-MHz tuning range), and the receiver consumes a total power of 10.69 mW.

Here, we demonstrate the details of a channelized 2.4-GHz receiver utilizing a fixed-LO temperature-compensated FBAR resonator [15]. First, we propose a modified sliding-IF receiver architecture utilizing a temperature-compensated thin FBAR. A channelized frequency plan allowing a fixed-frequency LO to overcome the tuning range limitations of the FBAR oscillator is demonstrated. This strategy completely eliminates the need for a PLL by directly dividing down the fixed FBAR oscillator frequency. Second, we propose a current-reuse balun LNA allowing a low-power wideband match without using inductors. Third, frequency conversion is achieved by a hybrid mixer, which stacks a switching mixer on a switched-g_m mixer for current reuse.

Section II presents the ZigBee receiver architecture and frequency plan for our PLL-free receiver. Section III describes the implementation of key building blocks in detail. Measurement results and performance comparisons are summarized in Section IV, and conclusions are made in Section V.

II. Proposed Sliding-IF Receiver Architecture

The sliding-IF architecture has proved to be one of most energy-efficient architectures for 2.4-GHz ISM-band receivers.

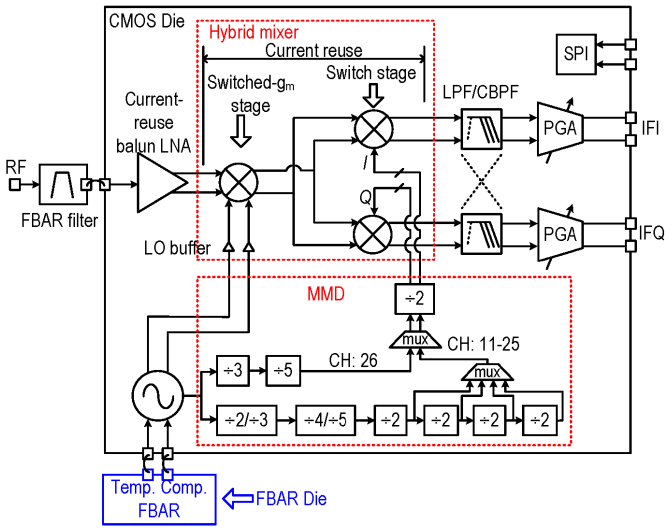


Fig. 2. Block diagram of the channelized ZigBee receiver utilizing fixed-LO temperature-compensated FBAR resonator.

To further reduce the power consumption and simplify the system architecture, we propose a modified sliding-IF architecture that only requires a fixed-frequency LO reference, facilitating the use of our FBAR OSC frequency reference.

A. Proposed Radio Architecture

Fig. 2 shows the block diagram of the proposed ZigBee receiver. The RF signal is prefiltered by a low-loss FBAR filter to ensure a more than 21.8-dB image-rejection ratio. The balun-LNA amplifies the RF signal and provides a differential output to the hybrid mixer which down-converts the RF signal to a configurable IF. The hybrid mixer inherently shares the current between the 1st and 2nd down-conversion to provide a low-power solution. The sliding-IF receiver architecture avoids a high-frequency quadrature LO generator, thus reducing dc power. Unlike previous designs, we use a fixed-frequency LO as a reference which is produced by a temperature-compensated FBAR oscillator. The FBAR oscillator has extremely good spectral purity owing to the intrinsic high-quality factor of the FBAR resonator and lack of PLL spurs. An integer type multimode divider (MMD) creates a 25% duty-cycle four phase 2nd LO signal for channel selection. In order to convert all 16 ZigBee channels to baseband, we implemented a configurable filter which can be programmed to low-pass filter (LPF) and complex bandpass filter (CBPF). The bandwidth of the filter can be varied by adjusting its transconductance cells and capacitors. Each channel of the ZigBee standard can be converted to the baseband with different combinations of the MMD division ratios and IF modes. The total RX gain can be controlled to accommodate a wide input range by using programmable gain amplifiers (PGAs).

B. Frequency Planning

To better understand the working principles of the proposed receiver architecture, a conceptual diagram of the frequency

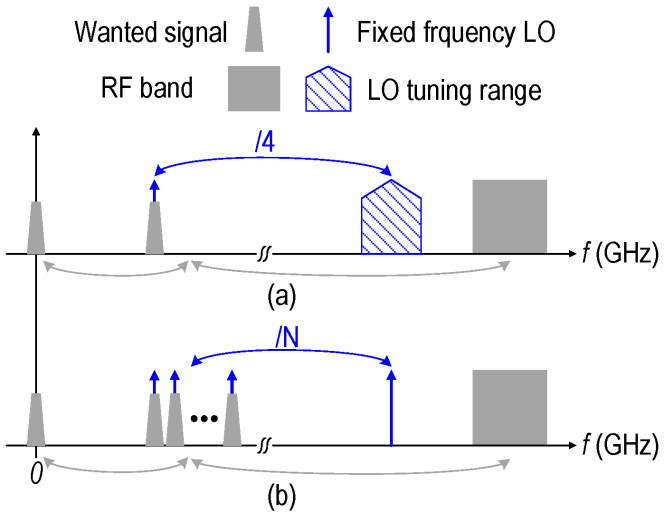
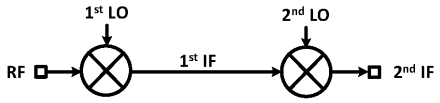


Fig. 3. Conceptual diagram of the proposed frequency conversion mechanism. (a) Traditional sliding-IF [10]. (b) Proposed sliding-IF.



CH	RF (MHz)	1st LO (MHz)	1st IF (MHz)	1st Image-rejection	2nd LO (MHz)	2nd IF (MHz)	2nd Image-rejection	MMD division radio (1st LO/2nd LO)
11	2405	2400	5	FBAR filter	5	0	N/A	480
12	2410	2400	10		10	0		240
13	2415	2400	15		15	0		160
14	2420	2400	20		20	0		120
15	2425	2400	25		25	0		96
16	2430	2400	30		30	0		80
17	2435	2400	35		30	5	CBPF	80
18	2440	2400	40		40	0	N/A	60
19	2445	2400	45		40	5	CBPF	60
20	2450	2400	50		50	0	N/A	48
21	2455	2400	55		50	5	CBPF	48
22	2460	2400	60		60	0	N/A	40
23	2465	2400	65		60	5	CBPF	40
24	2470	2400	70		75	5	CBPF	32
25	2475	2400	75		75	0	N/A	32
26	2480	2400	80		80	0	N/A	30

Fig. 4. Frequency planning for each channel.

conversion mechanism is shown in Fig. 3. To translate the input frequency to the 2nd IF of zero, the LO frequencies (f_{LO1} and f_{LO2}) of the traditional sliding-IF receiver [Fig. 3(a)] are defined as

$$f_{LO1} = \frac{2^n}{2^n + 1} \times f_{RF}, \quad n = 1, 2, 3 \ldots \tag{1}$$

$$f_{LO2} = \frac{1}{2^n} \times f_{LO1}, \quad n = 1, 2, 3 \ldots \tag{2}$$

The requirement for the LO tuning range is no less than $2 \times BW_{RF}/3$, which is around 54 MHz. Thus, a PLL is traditionally necessary for frequency tuning. MEMS resonators are known to provide high-quality factor around the gigahertz range [16]. FBAR oscillators exhibit a power/phase noise tradeoff 30 dB better than *LC* oscillators. To overcome the tuning range limitations, we have designed a simple frequency plan allowing a fixed-frequency 1st LO which is shown in Fig. 3(b). During the 1st frequency conversion, the entire RF band (2405–2480 MHz) is converted to a wideband 1st IF (5–80 MHz) by a fixed 2.4-GHz LO, while channelization is achieved in a 2nd frequency conversion. The 2nd LO frequency is generated by the programmable MMD. We employ two different IF modes (zero-IF and low-IF) to ensure that the integer-N-type MMD can cover all 16 ZigBee channels.

The proposed sliding-IF architecture is a unique solution that allows a fixed-frequency LO to overcome the tuning range limitations of FBAR oscillators. Compared to other *LC*-VCO solutions, the FBAR oscillator enables ultralow-power oscillation due to the high-Q resonators ($Q > 2000$). Meanwhile, the channelization scheme with a div-by-two chain is a simper solution than any other Integer-N or Frac-N solution in traditional PLL designs.

Generally, the choice of division ratio in the sliding-IF receiver is governed by the tradeoff between the quadrature accuracy and image rejection [17]. In our proposed receiver, it is also determined by the 1st LO frequency as well as the center frequency of each RF channel. We therefore chose the frequency plan for each channel as shown in Fig. 4. There are 16 different channels for ZigBee (indexed from 11 to 26). We fixed the 1st LO frequency to be 2.4 GHz. The key technique to improve the quadrature accuracy is to lower the 1st IF frequency, which is also desirable for minimizing power consumption. Moreover, it is important to make sure that the 2nd LO can be generated by dividing down from fixed 2.4 GHz 1st LO frequency with integer-N dividers. Therefore, we chose the 1st IF frequency from 5 to 80 MHz, which is very close to the baseband. We also program the 2nd LO frequency as shown in Fig. 4. Based on this frequency plan, all 16 channels can be translated to the baseband, either zero-IF (0 MHz) or low-IF (5 MHz).

To better understand how to translate the wanted RF signal to different IF modes for each channel, the frequency translation mechanism is illustrated with the channel indexed 21 and 22, as shown in Fig. 5. The input signal is filtered by a sub-mm^3 FBAR prefilter and the RF-image rejection solely depends on the filter characteristic of the FBAR filter (steps A and D). Thanks to the FBAR filter, the stopband rejection from 2.320 to 2.395 GHz (which corresponds to the RF-image band) is better than 21.8 dB. For the channel 21, the 2.455-GHz RF signal is first down-converted to the 1st IF at 55 MHz, and the 2nd LO is then generated by a divide-by-48 from the 1st LO at 2.4 GHz (step B). Here, we chose the low-IF mode for the second down-conversion, and the CBPF is selected to filter the IF-image during the second down-conversion (step C). A similar concept is used during the first down-conversion for channel 22 (step D). As we know, the 1st IF and 2nd LO signals occupy the same center frequency at 60 MHz. Thus, for channel 22, we chose the zero-IF mode for the second down-conversion. In addition, an LPF is used here to filter the out-of-channel interferes. Note that the I/Q sequences of 2nd LO will be swapped for channel 24 to avoid incorrect IF-image band filtering. Using this method, the wanted channel is filtered, down-converted, and then selected to the baseband in quadrature by using the fixed-frequency LO reference and integer-N dividers.

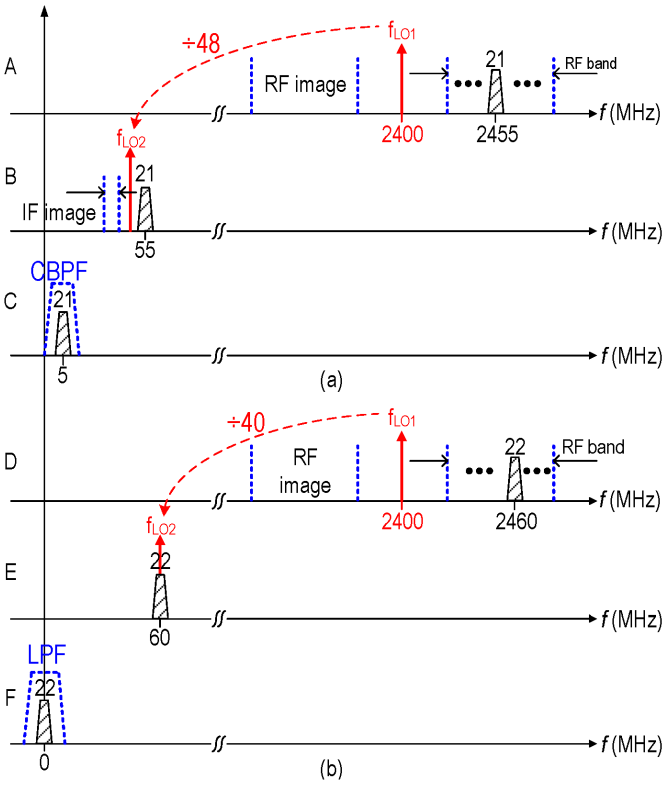


Fig. 5. Frequency translation mechanism of (a) low-IF (channel 21) mode and (b) zero-IF mode (channel 22).

C. Discussion

The spurious response will affect the first two channels (11 and 12), the 2nd LO harmonics will fall into the passband of FBAR filters. This will deteriorate the noise performance and potentially down-convert the unwanted signals by LO harmonics. The spurious response problem can be solved by using harmonic-rejection mixers (HRM) techniques as shown in [18]; however, this will also increase the complexity of the oscillator design and consume more power. The HRM will need multiple phase LOs to generate the staircase wave to reject the LO harmonics. Though it is not implemented in this design, the proposed MMD can be easily modified to generate eight-phase LOs as shown in Fig. 6. For channels 11–25, two of the divide-by-two components can be merged together as a divide-by-four. For channel 26, a quadrature generator such as polyphase filter which is followed by an additional Q path will be added to the original MMD. This solution will not increase the power consumption for each channel except for channel 26.

The modified sliding-IF architecture can be used in transmitter design, but in the reversed direction. As a result, the MMD can be used to generate the first-LO (same as the second LO in the RX) for up-conversion. Then, 2.4-GHz FBAR oscillator will convert the IF signal to the RF. To minimize spurious emissions, a set of HRMs are necessary in the frequency translation from baseband to RF. Due to the FBAR filters, unwanted image sidebands generated in the up-conversion due to single-phase LO are suppressed. Moreover, FBAR resonators can be integrated with the power amplifier (PA)

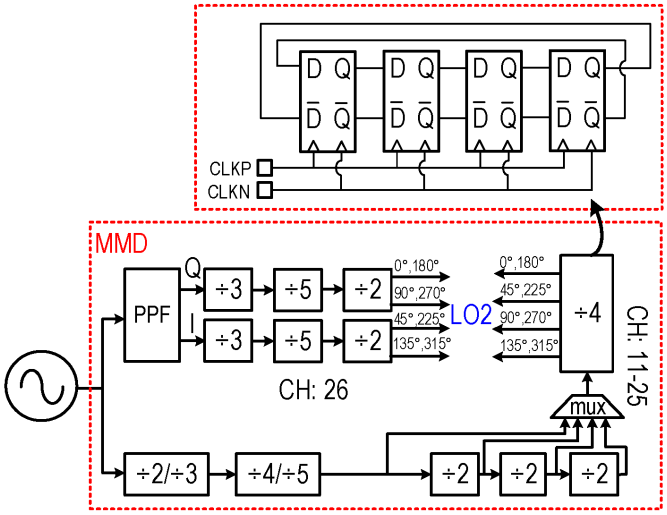


Fig. 6. Modified MMD for HRM.

by system in package or even system-on-chip (SoC) technique. Therefore, the PA output matching network can be replaced by the FBAR filter, leading to the decrease of circuit complexity and the enhancement of overall efficiency.

FBARs and CMOS chips are typically placed side-by-side interconnected at the package level, via wire or chip–chip flip–chip bonding. The key advantages are their modularity, high flexibility, and reasonably low fabrication complexity. Moreover, there is a strong trend to produce devices with ever diminishing size and weight for IoT application, especially for implantable biomedical applications. The development of stable and CMOS-compatible wafer-level packaging techniques will enable flexible and cost-effective SoC solutions in the near future.

III. Circuit Implementation

A. Current-Reuse LNA

A common-gate (CG) and common-source (CS) LNA [19] has been used to avoid the off-chip balun and to achieve a low NF by noise cancelling. However, it relies on asymmetric CG-CS transconductances and loads to achieve noise cancellation of CG transistors which is not compatible with frequency and process variations. Other work has also addressed this issue [20]. By introducing an ac-coupled CS branch and a differential current balancer (DCB), the same load is allowed for both CS and CG branches for wideband output balancing. We transfer this technique to our LNA design, but only introduce a single transistor to avoid the high-voltage supply.

Fig. 7 shows the proposed current-reuse balun LNA. Unlike active gain boost CG-CS LNA structures, we stacked the pFETs (M_5–M_8) above the nFETs (M_1–M_4) to further increase the current efficiency (g_m/I_d). Because, there are four transistors stacked from the supply to the ground, low V_{TH} (LVT) transistors are used. The V_{TH} of an LVT-nFET device is around 300 mV, which is suitable for the 1-V supply. Due to the severe headroom limitation, we bias the low V_{th} devices (M_1–M_8) in moderate inversion to optimize the tradeoff between their g_m/I_d and f_T. We feedback the RF signal to M_3 and M_5 by using two inverter-based

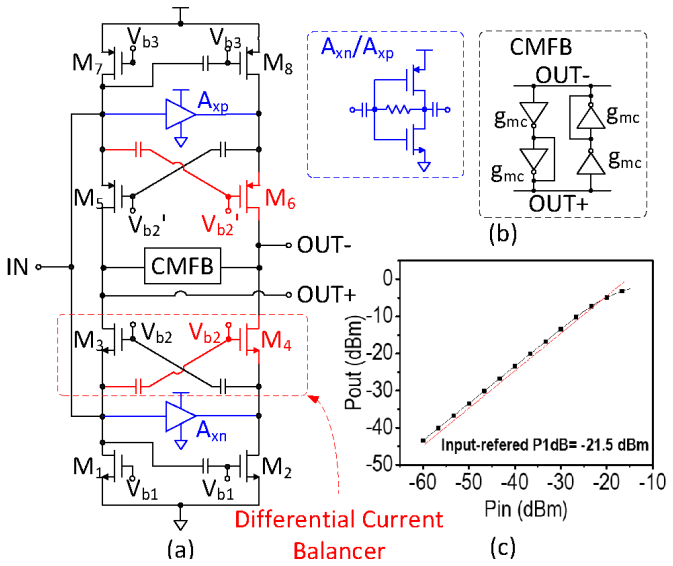


Fig. 7. (a) Schematic of current-reuse balun LNA. (b) Schematics of ac-coupled inverter amplifier and CMFB. (c) Simulated P1 dB.

amplifiers (A_{xp} and A_{xn}) to reduce the input impedance (R_{in}) and to improve NF while keeping the two branch currents small and equal. We also feed forward the RF signal into M_4 and M_6 to reduce the differential signal imbalance. We employ a self-biased common-mode feedback (CMFB) to stabilize the dc level [21] as shown in Fig. 7(b). Ideally, it generates finite common-mode resistance ($1/2 \times g_{mc}$) and infinite differential resistance [$1/(g_{mc} - g_{mc})$] at the output nodes. The RF signals are ac-coupled between CG and CS devices. Thus, each device is biased directly from a separate voltage reference. The minimum bias voltage for V_{b1} and V_{b2} are $V_{ov} + V_{th}$ and $2V_{ov} + V_{th}$, respectively. It is, therefore, possible to power the stacked LNA from a lower voltage supply. However, because of four stacked devices, the average overdriven voltage is limited to 250 mV under a 1-V supply. The simulated input-referred 1-dB compression point of proposed LNA is −21.5 dBm, as shown in Fig. 7(c).

DCB is commonly used to achieve wideband output balancing and improve reverse isolation and linearity [19]. In principle, a cascode amplifier with cross-coupled capacitors could realize the DCB. However, the overhead of the DCB consumes more voltage headroom than a typical cascade stage. To overcome this issue, a higher voltage supply or dual-voltage supply is necessary. In view of the tradeoff in the output balancing and voltage headroom, we propose a current-reuse balun-LNA that utilizing the CG stage as one of the cross-coupled transistors of the DCB structure. As illustrated in Fig. 8(b)–(c), the proposed embedded DCB benefits the balun-LNA twofold: 1) the DCB acts as a differential current-controlled current source with unity gain, forcing the $i_{sig} = i_{sig+} = i_{sig-}$, while keeping the voltage headroom the same as a conventional CG-CS LNA and 2) compared to the conventional CG-CS balun-LNA, the minimum dc current for input impedance matching is reduced. The input small signal ac current (i_{in}) can be written as

$$i_{in} = i_{sig+} = -i_{sig-} = (g_{mx} + g_{m2})v_{in}. \tag{3}$$

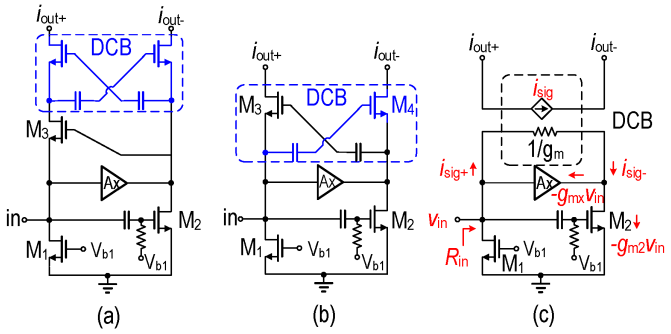


Fig. 8. (a) Schematic of balun-LNA using cascoding DCB [14]. (b) Proposed balun-LNA with embedded DCB. (c) Equivalent circuit of the proposed balun-LNA.

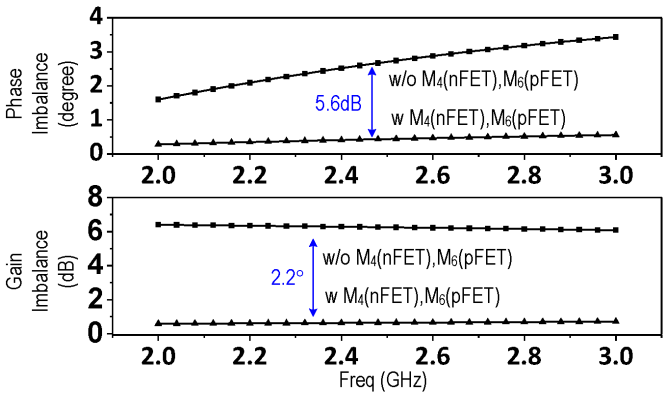


Fig. 9. Simulated gain and phase imbalance performance.

Thus, the RF input impedance is given by

$$R_{in} = \frac{1}{g_{m2} \times \left(1 + \frac{g_{mx}}{g_{m2}}\right)}. \tag{4}$$

Note that, for 50-Ω matching, the intrinsic transconductance is $(1 + g_{mx}/g_{m2})$ times less than that of the conventional CG-CS balun LNA, which reduces the power consumption by the same factor. While taking the stacked pFETs into account, the intrinsic transconductance is further reduced. Corresponding to a $|S_{11}|$ value of < -10 dB, the tolerable R_{in} for $R_S = 50\ \Omega$ ranges from 26 to 97 Ω. In this paper, R_{in} is set to 70 Ω ($g_{m2} = 1.4$ mS and $g_{mx}/g_{m2} = 4$) to reduce total power consumption, while yielding $|S_{11}| < -15$ dB. The tradeoff is that the impedance matching BW is slightly worse compared to strict 50-Ω matching.

The simulated gain and phase imbalance performance are shown in Fig. 9. Compared with the CG-CS structure, the gain and phase imbalance of the proposed structure are improved by 5.6 dB and 2.2°, respectively. From 2 to 3 GHz, the gain and phase mismatch are <0.5 dB and <1.2°, respectively.

The CG-CS balun LNA is also known as a noise-cancelling LNA. The noise-cancelling principle has been discussed in [11]. To simplify the study, we assume that the g_m of the NMOS devices is the same as the PMOS counterpart. In order to completely eliminate the noise generated by the CG devices M_1/M_7, the equation of $R_{in} \times g_{m,CS} = 1$ should be

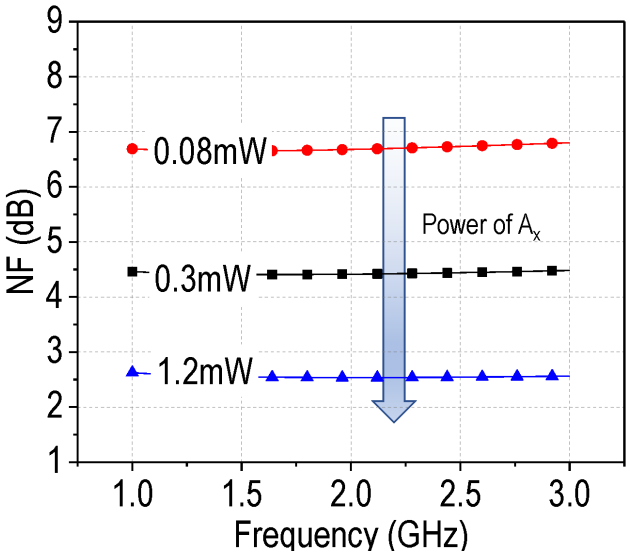


Fig. 10. Simulated NF versus the total power of A_x ($A_{xp} + A_{xn}$).

satisfied, where $g_{m,CS} = 2(g_{mx}+g_{m2})$. The ideal g_{mx} for noise cancelling should be 5.7 mS, which is approximately the same as we used ($g_{mx} = 5.6$ mS) in our design. However, device sizing for full-noise cancellation of the M_1/M_7 does not result in the lowest total NF. While the LNA burns a total power of 0.5 mW, the auxiliary amplifiers A_x (A_{xp} and A_{xn}) and CS devices (M_2 and M_8) become the dominant noise contributor. Fig. 10 shows the simulated NF versus power of the auxiliary amplifiers A_x. We optimized the A_x power to be 0.3 mW for a tradeoff between NF and power performance. The NF performance can be improved (NF $<$ 2.6 dB) by increasing the total power of the A_x stage ($>$1.2 mW) with a partial noise-cancelling condition.

B. Temperature-Compensated FBAR Oscillator

The first LO is a fixed-frequency oscillator utilizing a 0.1 mm^2 temperature-compensated FBAR. Fig. 11(a) shows the schematic of differential Colpitts oscillator, the cross section of the FBAR and its mBVD model. The center frequency of FBAR oscillator is determined by

$$\omega_o = \sqrt{\frac{(g_m L_x + R_L(C_1 + C_2))}{L_x R_L C_1 C_2}} \tag{5}$$

where L_x represents the motional inductance of the FBAR. Low V_t and triple-well NMOS transistors are used for M_1 and M_2 to maximize the transconductance and also to decrease the dc power. Compared to a traditional FBAR, a compensation layer is added to compensate the negative temperature coefficient of AlN FBAR. Based-on the mBVD model, the Q of the resonator is more than 1000 which is high enough to allow extremely low phase noise application.

Fig. 11(b) shows the measured FBAR temperature coefficient. In a six-inch wafer, the median temperature coefficient is 0.89 ppm/°C. The FBAR oscillator is temperature stable within +/−50 ppm (200 kHz) over 0 °C to 100 °C, which is sufficient for the ZigBee application. However, it may not be adequate as a system clock for low-duty-cycle IoT applications that mostly involve a long sleep time. To further improve FBAR stability, an electronic temperature compensation scheme [22] can be used to decrease intrinsic +/−50 ppm stability of the FBAR oscillator down to +/−3 ppm.

The sensitivity of the oscillation frequency to capacitive variation is about −10 MHz/pF or over 5000 ppm/pF, as shown in Fig. 12, where the x is normalized resonator area, and n is capacitor array size. There, the oscillation frequency can be tuned with relatively small tunable or switchable capacitors (C_1, C_2), overcoming fabrication and temperature related process variations. This method has been utilized in precision crystal oscillator [23]. Please note that increasing the tuning range would load the resonator and result in increased power consumption.

C. Hybrid Mixer

Like other dual-conversion RF front ends, it is desirable for sliding-IF receiver has two cascaded mixers for low-voltage application, where voltage headroom is scarce. The tradeoffs among gain, noise, linearity, and power consumption make the RF down-conversion mixer the most challenging block in the sliding-IF receiver.

Active Gilbert-cell mixers are widely used due to their high gain and moderate linearity. However, its use in a dual-conversion application is limited. It requires two voltage-mode active mixers cascaded, resulting in a high-power consumption and low linearity. Passive mixers consume negligible dc current, and usually exhibit superior linearity when LO drive at the gate is large. However, the input impedance is generally low (on the order of 200–500 Ω), severely loading down the previous stage and thus degrading the front-end RF gain.

In view of the tradeoffs existing in the common active and passive mixer topologies, we propose a hybrid mixer topology, where it behaves like a Gilbert mixer with its "g_m cell" switched by the LO signals, as illustrated in Fig. 13. Similar to a Gilbert mixer, the second *LO* feeds into the gate and the small signal into the source of the switching stage. The difference lies in the g_m stage: the first *LO* feeds into the source of the g_m cell, it behaves like a switched-g_m active mixer [24]. Compared to its Gilbert-type counterpart, we propose the hybrid mixer for two reasons: first, we stacked the second conversion mixer (switch stage) at the top of switch-g_m mixer for current reuse, it reduces the requirement of V_{dd} and the amplitude of LO. Second, I and Q signals in second conversion share the same switched-g_m cell. The 25% duty-cycle four phase second LO signal avoids the impedance loading between I and Q branches. The first *LO* signal induces only common-mode noise at the outputs that can be rejected differentially.

D. Analog Baseband

The baseband filter can be configured either as a complex BPF or a LPF. The complex BPF is a frequency-shifted version of the LPF. To convert an arbitrary LPF to a complex BPF centered at $\omega_{BP} = 5$ MHz, every frequency-dependent element in the LPF should be altered to be a function of $s - j\omega_{BP}$

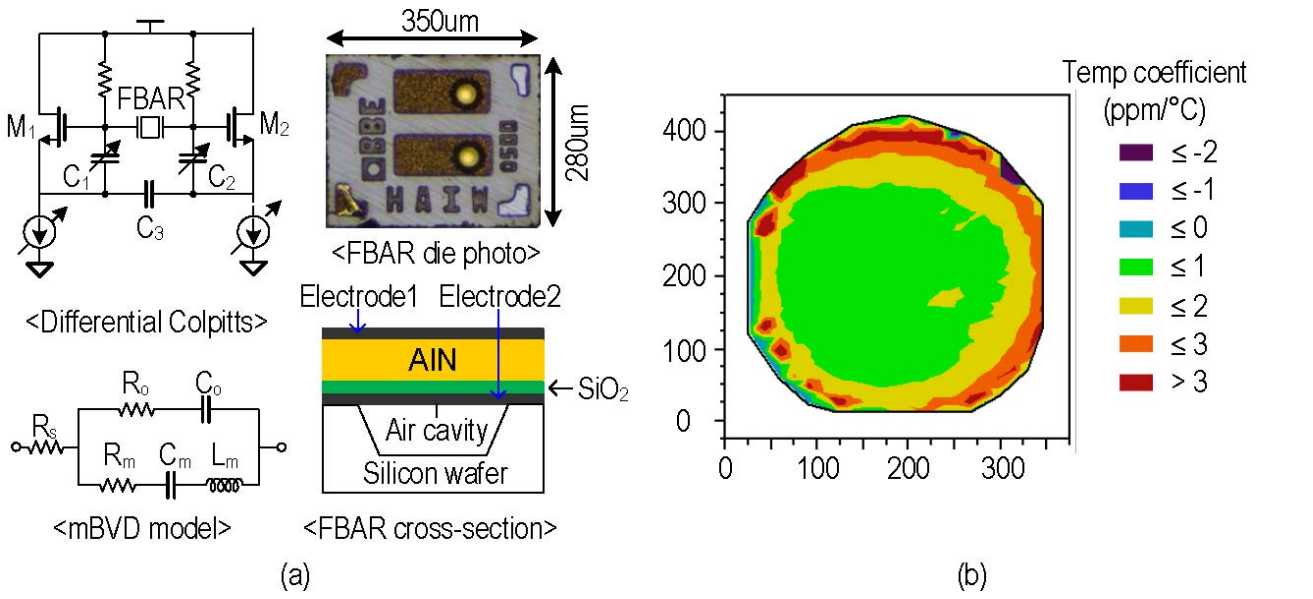


Fig. 11. (a) Schematic of differential Colpitts oscillator, the cross section of the FBAR and its mBVD model. (b) Measured FBAR temperature coefficient.

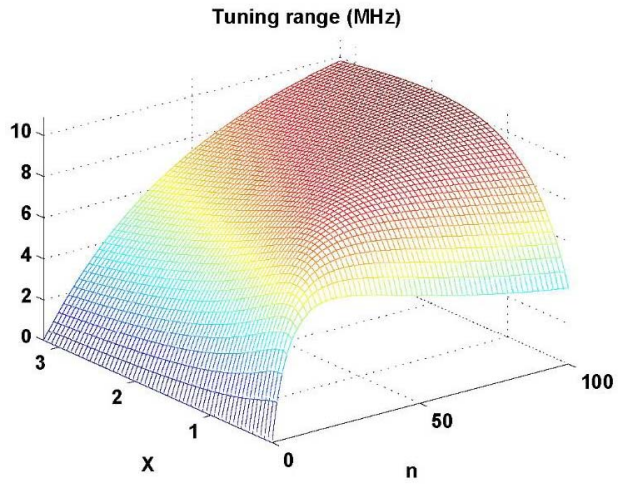


Fig. 12. Sensitivity of the oscillation frequency to capacitive variation.

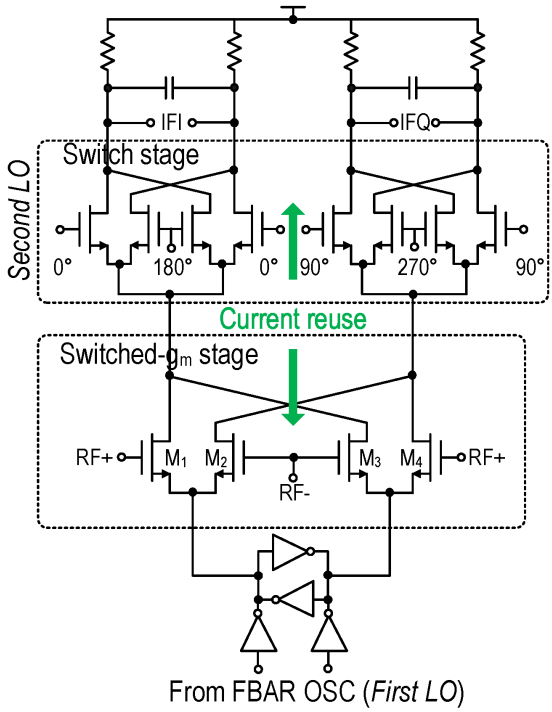


Fig. 13. Schematic of hybrid mixer.

instead of s. Fig. 14 shows the block diagram of the entire baseband configurable filter. The basic frequency-dependent element in a filter is the integrator. In the zero-IF mode, the dc current of the transconductance (G_{m4}) can be switched off and the filter works as an LPF with its corner frequency at 1 MHz. The baseband filter is discretely tuned using a combination of binary weighted switched capacitors and OTAs (G_{m1}–G_{m4}). We chose a 4-bit capacitor bank with minimum 1-pF step which can achieve a total of 15 different tuning steps. Simulation result shows that the bandwidth of the filter (LPF mode) is tunable from 200 kHz to 8 MHz which is sufficient to cover the PVT variations. The maximum peak current is around 110 μA under BPF mode.

In order to increase the current efficiency and reduce input-referred noise, the least number of transistors is used in the OTA, as shown in Fig. 14. The OTA is based on the inverter which is similar to the G_m shown in [21]. This OTA is preferred over prior work for two reasons. First, the OTA in [21] is directly tuned through its supply voltage. Additional circuitry may need to achieve multiply voltages from a single 1-V supply, and therefore may consume more power. Second, the OTA in [21] is more susceptible to supply noise and requires a clean supply during operation. Herein, we use fully differential structure with a binary weighted tail current source to improve the PSRR performance. Due to severe headroom limitations, we forward bias the bulk–source junction of the device by 250 mV to reduce their V_{TH} by around 35 mV (10%).

Fig. 15 shows the schematic of the PGA. Compared to a conventional operational amplifier stage, we use the following techniques to save the dc power.

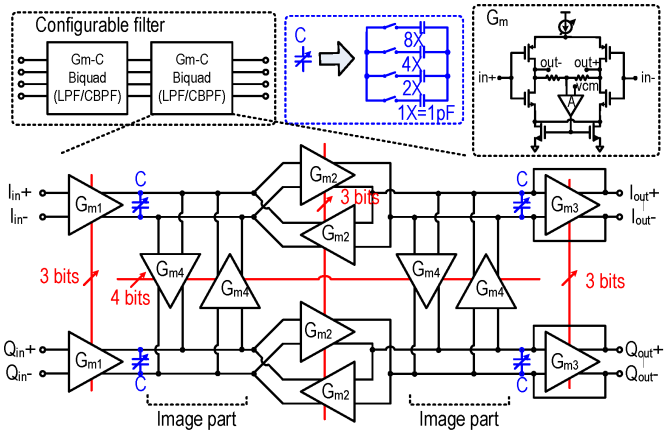


Fig. 14. Block diagram of the baseband configurable filter.

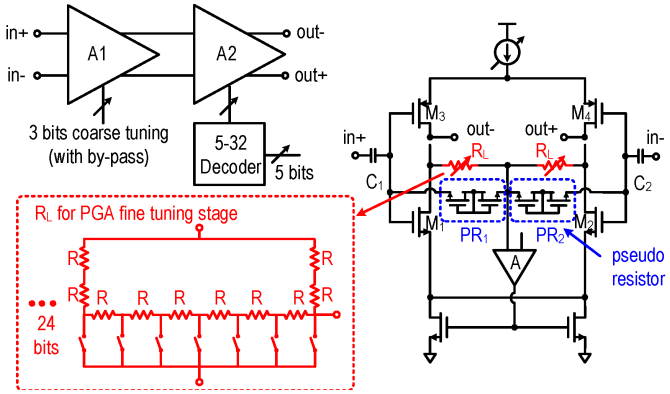


Fig. 15. Schematic of the PGA.

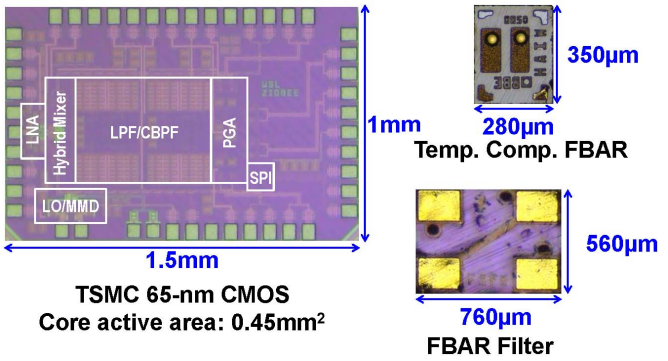


Fig. 16. Die micrographs of CMOS chip in 65-nm CMOS, temperature-compensated FBAR resonator, and FBAR filter.

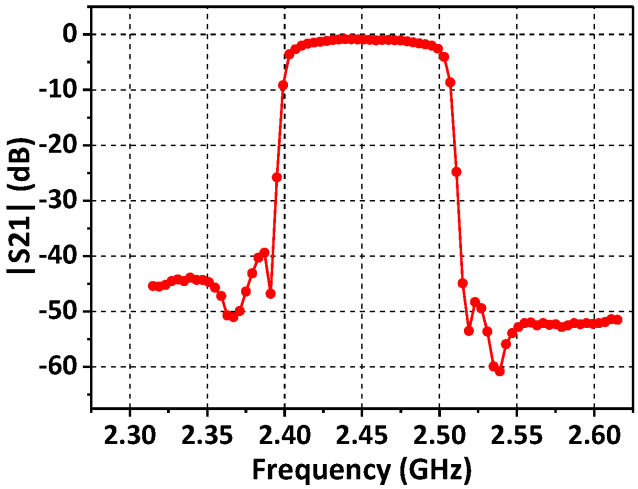


Fig. 17. Measured frequency response of FBAR filter.

1) The dc current of the first stage (A1) can be switched off in the low-gain mode.
2) The inverter-based amplifier reuses the binary weighted current to boost the g_m.
3) The differential input is ac coupled by using pseudo resistors without consuming extra dc power.

The high-pass filter corner is set to ≈100 kHz by C_1 (5 pF) and PR_1 after Miller-gain reduction. The pFET and nFET are sized to 8 μm/80 nm and 20 μm/80 nm to source enough current (10 μA/branch) to provide sufficient bandwidth (≈10 MHz). To save the area, the programmable R–$2R$ resistor ladder is also used as averaging resistors of common-mode feedback loop.

IV. Experimental Results

The chip was fabricated in a 65-nm CMOS process. Fig. 16 shows the die micrographs of CMOS chip in 65-nm CMOS, temperature-compensated FBAR resonator, and the FBAR filter. The CMOS chip occupies a core area of 0.45 mm^2 without using any inductors. A 2.4-GHz temperature-compensated FBAR resonator was mounted near the chip.

Fig. 17 shows the measured $|S_{21}|$ of the FBAR pre-filters. The insertion loss is 0.8–3.4 dB in the frequency range of 2.404–2.481 GHz. For the ZigBee channel 11, the distance between passband and stopband is only 8 MHz. It achieves a 21.8-dB out-of-band image rejection from 2.396 to 2.404 GHz. For other channels, it achieves >37-dB out-of-band image rejection.

We used a vector network analyzer and a NF analyzer to measure the S-parameter and gain/NF, respectively. Because of the CG amplifier, the input matching is rather wideband as shown in Fig. 18(a). The $|S_{11}|$ bandwidth (<-10 dB) is ≈0.7 GHz from 2.1 to 2.8 GHz looking directly into the chip. The wideband low-Q matching eases the coverage of bondwire inductance and input capacitance variations. At the PGA output, we measure an overall maximum gain of 57.8 dB, and the voltage gain is also tunable over more than 50 dB. We measured a NF (excluding FBAR prefilter) of 9.8 to 11.5 dB at the low-IF mode and 13.6 to 15.7 dB at the zero-IF mode, respectively. We observe that the NF of the zero-IF mode is ≈4 dB higher than the low-IF mode. Because the hybrid mixer is the combination of two active mixers (Switched-g_m and Gilbert), we expect significant flicker noise at 3 MHz or below. Fig. 18(c) shows the measured linearity of the RF front end. We achieve an IIP_3 of -18.5 dBm at a moderate gain of 25 dB. The configurable filter response shows 41 dB (44 dB) rejection at the adjacent (alternate) channel. It also provides 37-dB image rejection at the second down-conversion [Fig. 18(d)].

Fig. 19 shows measurement results of NF, in-band and out-of-band IIP3s versus receiver gain. The measured in-band

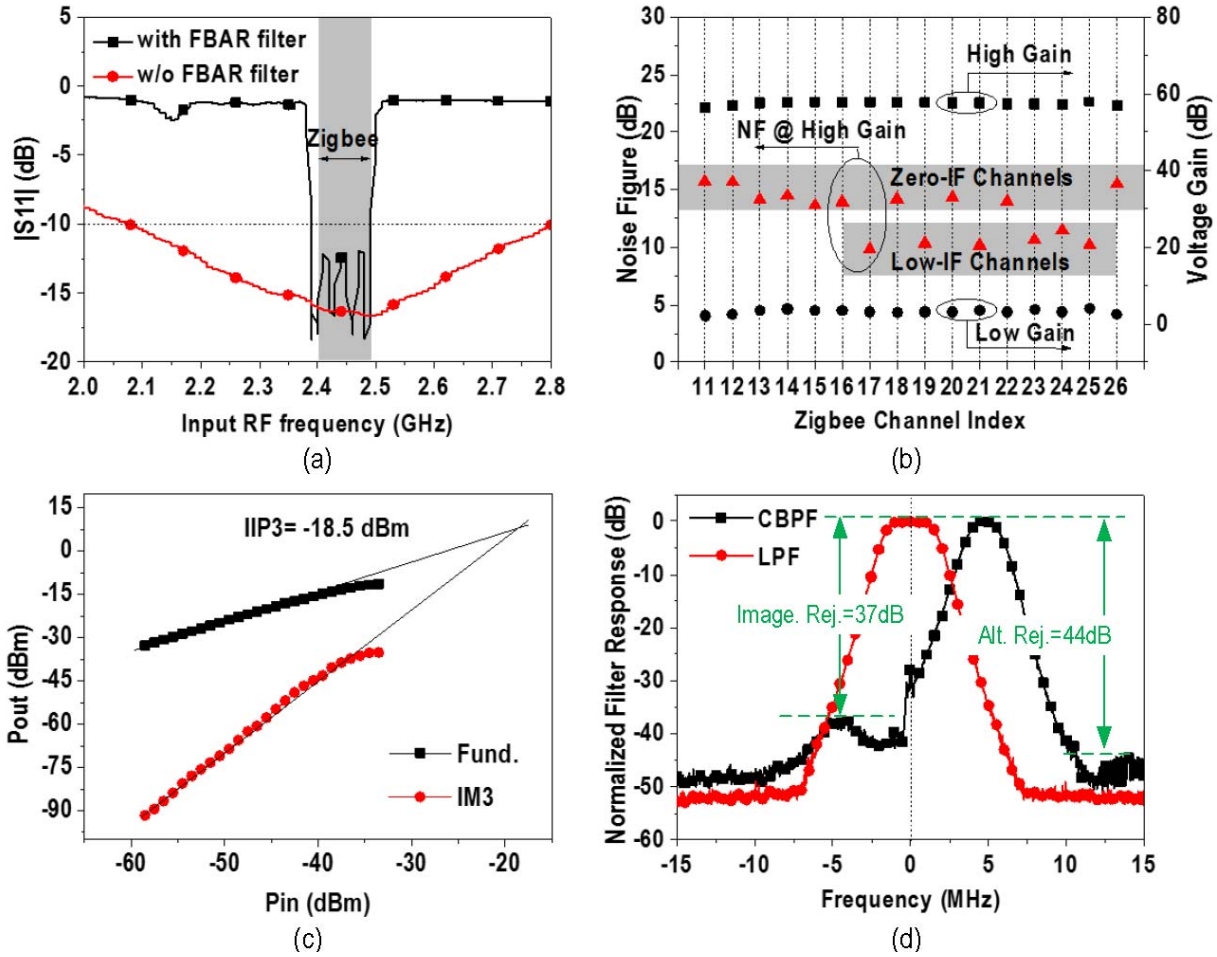


Fig. 18. (a) $|S_{11}|$, (b) voltage gain and NF, (c) in-band IIP_3, and (d) filter response.

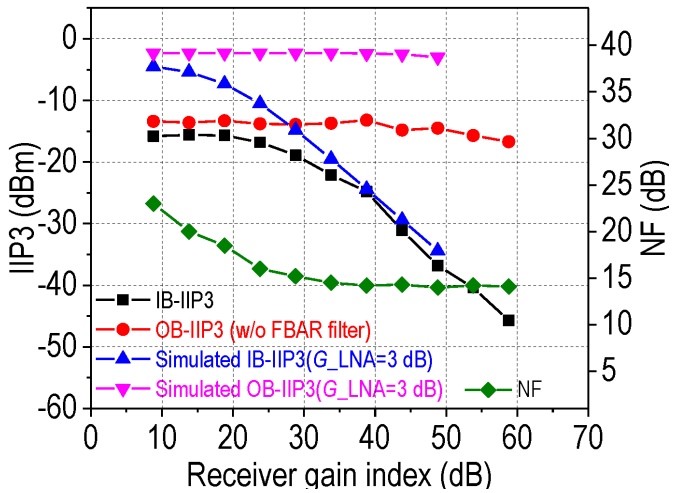


Fig. 19. Measurement results of NF, in-band, and out-of-band IIP3s versus receiver gain.

IIP3s are −15.8 and −45.7 dBm at the gain of 57.8 and 7.8 dB, respectively. Meanwhile, by applying two tones at (LO + 10 MHz, LO + 20 MHz) mentioned in the test profile of [11], we achieved out-of-band IIP3s of −16.7 to −13.4 dB with the gain of 7.8 to 57.8 dB, respectively. The measured NF at low-gain mode is about 23 dB. The overall P1 dB at low-gain mode is −25.8 dBm (approximately 10 dB lower than measured in-band IIP3 shown in Fig. 19). Although the gain-compression performance does not meet the ZigBee (802.15.4) specification that the maximum input signal level is −20 dBm, it can be easily fixed by providing more gain settings in the LNA. Fig. 19 also shows the simulated IIP3 performance with the gain of LNA about 3 dB, as a result, the receiver achieves an in-band IIP3 of −4.5 dB. For those out-of-band far-out blockers, they can be filtered simultaneously by the FBAR prefilter and the baseband filter (approximately >74-dB blocker rejection), before entering main amplification stage of the PGA.

The measured phase noise (Fig. 20) at 3.5-MHz offset frequency is −144 dBc/Hz with an amplitude of 250 mV (peak-to-peak) that has significant margin to the ZigBee specifications [25]. The total power consumption used in the oscillator is 660 μW. The FBAR OSC worked well even when we reduced the supply voltage to 500 mV. The measured phase noise is lower than −135 dBc/Hz at 1-MHz offset.

Based on the SNR requirement of the ZigBee standard (7-dB SNR at the demodulator for a 2-MHz channel bandwidth), this receiver achieves a −88 dBm sensitivity [17]

$$P_{\text{sen}} = -174\text{dBm/Hz} + \text{NF} + 10\log B + \text{SNR}_{\text{min}}. \quad (6)$$

TABLE I
CHIP SUMMARY AND COMPARISON WITH THE STATE OF THE ART

Performance Comparison									
	This work	ISSCC'13 [3]	JSSC '13 [7]	ISSCC'08 [9]	ISSCC'15 [10]	ISSCC'13 [11]	ISSCC'17 [26]	ISSCC'17 [12]	ISSCC'16 [13]
Standard	ZigBee	ZigBee/BLE/ MBAN	NA	ZigBee	BLE	ZigBee	IEEE802.1 5.4/BLE[a]	BLE	BLE
Architecture	Sliding-IF RX+LO	Sliding-IF RX+TX+PLL	Sliding-IF RX+PLL	Low-IF LMV	Low-IF LMV	Low-IF RX	Zero-IF	Low-IF	Hybrid Loop
XTAL	No	Yes	No	N/A	N/A	N/A	Yes	Yes	Yes
On-chip Inductors	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Supply [V]	1	1.2	1.8	1.2	0.6	1.2	0.85	0.18	0.6/1.1
RX Power [mW]	0.86	>1.6	2.4	3.6[b]	0.6[b]	1.7	0.87	0.382	6
PLL/LO Power [mW]	0.92	1.8	15.4			N/A	0.68		
Gain [dB]	57.8	NA	44.2	75	55.6	57	N/A	34.5	72
NF [dB]	15.7[d]	6	14.8	12	15.8	8.5	6	11.3	N/A
IIP_3 [dBm]	-18.5	-19	-28	-12.5[c]	-16.8[c]	-6[c]	N/A	-12.5[c]	N/A
Image Rej. [dB]	1^{st} = 40dB 2^{nd} = 37dB	35	N/A	35	30.5	36	No image	26.2	N/A
PN@3.5M [dBc/Hz]	-144	N/A	N/A	-107	N/A	N/A	N/A	-113	N/A
Technology	65-nm	90-nm	180-nm	90-nm	130-nm	65-nm	40-nm	28-nm	65-nm
Core Area [mm^2]	0.45	2	N/A	0.35	N/A	0.22	0.3	1.65	9

Power Breakdown [mW]						
LNA	Mixer	Filters	PGA	FBAR OSC	Dividers	Total
0.51	0.20	0.11	0.04	0.66	0.26	1.78

Simulated gain Distribution [dB]					
FBAR filter (Measured)	LNA	Mixer	Filters	PGA	Total
-3.4 ~ -0.8	16.6	5.3	-0.5	-10 ~ 37.8	8 ~ 58.3

a) FSK-type modulation; (b) LMV only, no channelization; (c) Out-of-band IIP_3; (d) excluding FBAR pre-filters

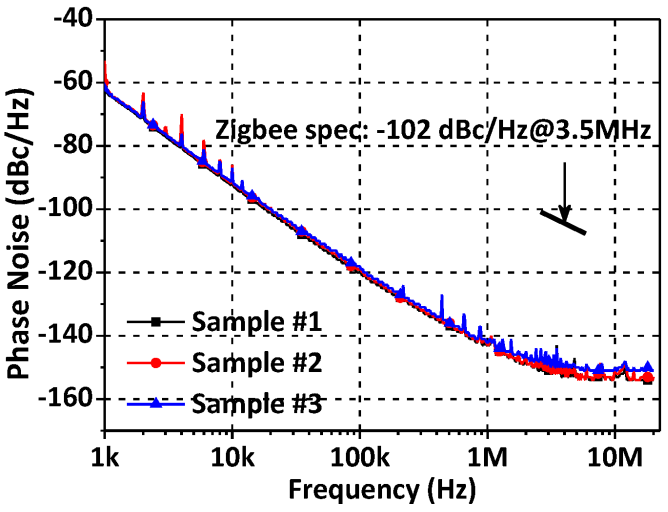


Fig. 20. Measure phase noise of FBAR oscillator.

A performance comparison with the relevant recently published state of the arts is shown in Table I, where [3] is a traditional PLL-based transceiver architecture, [7] is a BAW-based 2.4-GHz receiver, [9]–[11] are classical current-reuse between RF and baseband blocks, [26] is a phase-tracking architecture suitable for constant-envelope frequency-shift keying-type modulation scheme. Though the RF performances (NF and power) reported in [26] are better than our receiver. The significance of our work is that we successfully removed the off-chip crystals and on-chip inductors by using FBAR resonators. In addition, the PLL-free architecture with simple divider chains allows us to fasten the startup time, which is significant and competitive with most of the recent published IoT receivers.

V. CONCLUSION

In this paper, we present a 2.4-GHz PLL-free receiver for low cost low power ISM-band applications that is designed without external quartz or PLLs. We demonstrated a modified sliding-IF architecture scheme with a suitable LO frequency plan. It eliminates the need for a PLL by directly dividing down the fixed FBAR oscillator frequency. The temperature-compensated FBAR oscillator is temperature stable within $+/-50$ ppm over 0 °C to 100 °C. Moreover, we presented a current-reuse balun LNA allowing a low-power wideband match without using inductors. A hybrid mixer combines the switching mixer and switched-g_m mixer together for power saving. For the baseband filter, inverter-based OTAs were exploited to boost the current efficiency. As a result, the proposed receiver achieves -88 dBm sensitivity with a total power consumption of 1.8 mW.

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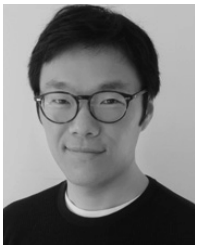

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