A Low-Jitter and Low-Reference-Spur Ring-VCO-Based Switched-Loop Filter PLL Using a Fast Phase-Error Correction Technique

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***Abstract*— A low-jitter and low-reference-spur ring-type voltage-controlled oscillator (VCO)-based switched-loop filter (SLF) phase-locked loop (PLL) is presented. To enhance the capability of suppressing jitter of a VCO, we propose a fast phase-error correction (FPEC) technique that emulates the phase-realignment mechanism of an injection-locked clock multiplier. By the proposed FPEC technique, accumulated jitter of a VCO can be removed intensively in a short interval, thereby suppressing jitter dramatically. Based on a PLL topology having an intrinsic integrator in a VCO, the proposed architecture can also achieve a low reference spur despite a high multiplication factor (i.e., 64). This paper also presents the selective frequency-tuning technique used in the VCO that helps the proposed architecture further suppress the level of reference spur. The proposed PLL was fabricated in a 65-nm CMOS process. The measured rms jitter integrated from 1 kHz to 80 MHz and the reference spur of the output signal with a 3.008-GHz frequency were 357 fs and −71 dBc, respectively. The total active area was 0.047 mm^2, and the power consumption was 4.6 mW.**

***Index Terms*— Jitter, multiplication factor, phase-error correction, phase-locked loop (PLL), phase noise, reference spur, ring voltage-controlled oscillator (VCO), switched-loop filter (SLF).**

I. Introduction

VOLTAGE-CONTROLLED oscillators (VCOs), which are core circuits of clock generators, are classified into two categories, i.e., ring VCOs and *LC* VCOs, according to their frequency-generation mechanisms. Ring VCOs have clear advantages over their counterpart: a much higher integration efficiency and a wider frequency-tuning range without the need of large passive components. Also, they naturally can generate multiple phases of the output signal and be more robust to the effect of frequency pulling. On the other hand, ring VCOs have higher jitter because the frequencies of their outputs are defined by the amount of the total delay from the multiple delay stages, which involves increases in thermal noise. This poor performance of jitter has been the major bottleneck, and it has limited the use of ring VCOs in the design of low-jitter clock generators. Thus, so far, almost all clock generators targeted for generating low-jitter signals have used *LC* VCOs, which can achieve much lower jitter (or phase noise) due to their sharp frequency selection by an *LC* tank having a high Q-factor.

In order to take advantage of the aforementioned merits of ring VCOs, many studies have been conducted on ring-VCO-based clock generators that can suppress the VCO's jitter effectively [1]–[25], thereby achieving an overall performance of jitter that is comparable to that of *LC*-VCO-based architectures. Recently, injection-locked clock multipliers (ILCMs) have attracted a lot of attention [1]–[19]. In ILCMs, the clean reference clock produces narrow, intensively strong pulses that are injected to the VCO, which causes a momentary realignment of the phase of VCO's output signal. Due to this phase-realignment mechanism, the phase error of the VCO is removed instantaneously, and ILCMs can have very low jitter, even when using a ring VCO. However, a critical problem of ILCMs is that this low jitter is valid only when the free-running frequency of the VCO (f_{VCO}) is sufficiently close to the target frequency [26]. Thus, when the difference between f_{VCO} and the target frequency increases due to frequency drifts caused by process, voltage, and temperature (PVT) variations, the noise performance easily can be degraded. The drifts of f_{VCO} cause a more severe problem, i.e., a significant increase in reference spur. Since the phase-realignment mechanism of ILCMs does not involve an integrator, it cannot correct drifts of f_{VCO}. Thus, when f_{VCO} deviates from the target frequency, periodic phase shifts occur, resulting in large levels of reference spur. The effect of deviations in the frequency on the level of reference spur can be very severe, e.g., only a 1% deviation in the frequency can cause reference spur of as much as −20 dBc, when the multiplication factor (N) is 10 [27]. The vulnerability of ILCMs to deviations in f_{VCO} in the absence of an integrator also prevents the ILCMs from having a large N.

On the other hand, phase-locked loops (PLLs) that have the integrator in their transfer functions can produce much higher stability despite the drifts of f_{VCO} caused by PVT variations. However, a ring VCO cannot be incorporated in conventional PLLs that use a continuous-time loop filter, if the aim is to achieve a performance of ultralow jitter. This is because these PLLs also incur increases in reference spur,

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when the noise-reduction bandwidth of the VCO is extended. In type-I PLLs that use an XOR-type phase detector (PD), the control voltage of the VCO fluctuates more as the noise-reduction bandwidth of the VCO increases, resulting in a large reference spur [22]. Also, in type-II PLLs, the bandwidth should be limited to suppress the magnitude of ripples in the control voltage, which are caused by the leakage of the loop filter or mismatches in the up and down currents of the charge pump (CP) [28]. Switched-loop-filter (SLF)-based PLLs also are considered to be another promising solution [20]–[25]. By isolating the moments, at which phase errors are detected and delivered to the VCO, SLF PLLs can remove the tradeoff associated with the noise-reduction bandwidth of the VCO. Thus, the bandwidth can be increased to suppress the jitter of the VCO considerably, without any significant increase in the reference spur. Although SLF PLLs can achieve fair performance of jitter without the problem of reference spur, the performance of jitter itself is still inferior to that of ILCMs. The jitter is different for the two architectures because of the differences in their phase-error-correction mechanisms. A detailed discussion of the differences between the two mechanisms is presented in Section II.

In this paper, we propose a new ring-VCO-based SLF PLL that can generate concurrently an output signal with low jitter and low reference spur. By using the fast phase-error correction (FPEC) technique [29] that emulates the phase-realignment mechanism of an ILCM, which momentarily removes the phase error of the VCO, the proposed SLF PLL can achieve very low jitter. Also, because the proposed architecture is based on the PLL topology, it includes the intrinsic integrator of the VCO; thus, low reference spur and high stability can be maintained even when the multiplication factor increases. The selective frequency-tuning (SFT) technique proposed for the VCO also helps the PLL further reduce the level of reference spur.

This paper is organized as follows. Section II presents the comparison between the error-correction mechanisms of conventional SLF PLLs and ILCMs and introduces the concept of the proposed FPEC technique. The implementation and the operation of the SLF PLL with the FPEC technique are described in Section III. Section IV presents the analysis of the FPEC technique and design considerations. Experimental results are presented in Section V, and conclusions are drawn in Section VI.

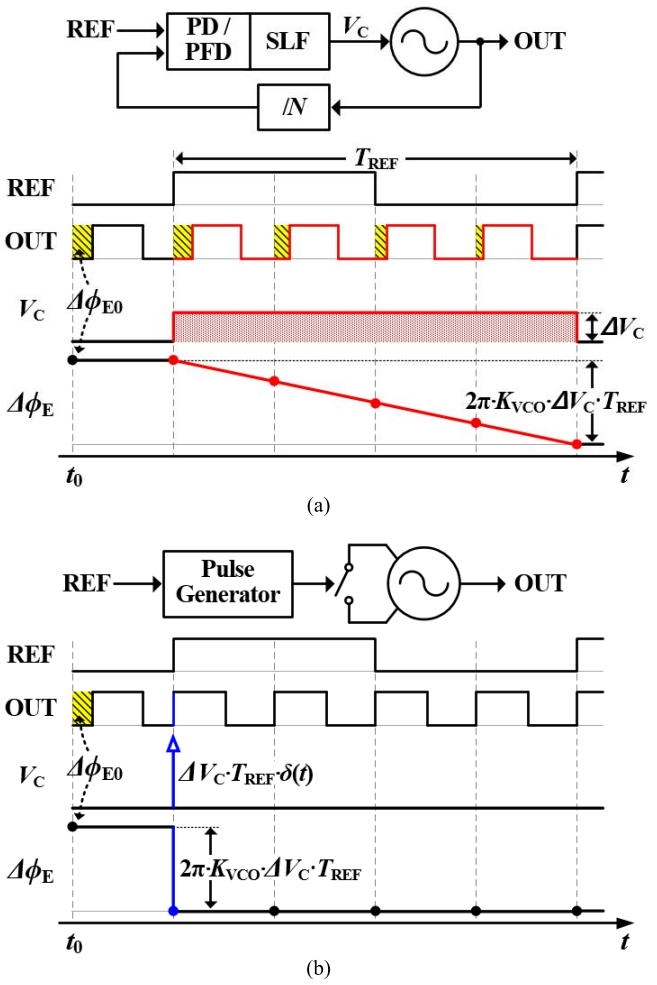


Fig. 1. Representation of phase-error correction mechanism. (a) Conventional SLF PLL. (b) ILCM.

II. Concept of the Proposed Fast Phase-Error Correction

A. Comparison of Phase-Error Corrections of ILCMs and SLF PLLs

To understand the difference in the suppression of jitter in the VCOs of conventional SLF PLLs and ILCMs, the mechanisms of phase-error correction of the two architectures must be compared. Fig. 1(a) and (b) shows how the phase error $\Delta\phi_E$ decreases in an SLF PLL and an ILCM, respectively. To focus on the process in which the initial phase error $\Delta\phi_{E0}$ is removed over a reference period T_{REF}, we assume the following conditions. First, both architectures are in steady state, and the frequency deviation of f_{VCO} from the target frequency is zero. Second, no additional phase error except $\Delta\phi_{E0}$ is added from either the VCO or the reference clock during the current period. Third, $\Delta\phi_{E0}$ is completely removed during this T_{REF}, i.e., the phase-correcting factor β [2] is exactly one. In the case of a typical SLF PLL, as shown in Fig. 1(a), $\Delta\phi_{E0}$ detected by the PD causes a finite change in the control voltage (V_C) of the VCO, i.e., ΔV_C, and it also causes a corresponding change in f_{VCO}, and these changes are maintained constantly during theT_{REF}. Then, due to the effect of the integrator of the VCO, the changed f_{VCO} removes $\Delta\phi_{E0}$ gradually over the T_{REF}. When the phase-error correction in this T_{REF} is completed, the amount of the total phase corrected during the period is $2\pi \cdot K_{\mathrm{VCO}} \cdot \Delta V_C \cdot T_{\mathrm{REF}}$, and this value should be equal to $\Delta\phi_{E0}$ since β is assumed to be one. However, as shown in Fig. 1(b), an ILCM corrects the phase of the VCO itself without the use of the integrator of the VCO. Thus, $\Delta\phi_{E0}$ can be removed momentarily at the beginning of the T_{REF}. Since the phase-realignment mechanism of an ILCM directly corrects the phase of the VCO, there must be no change in f_{VCO} during the process. Also, since the phase correction of ILCMs does not use any external loops, physically, there is no V_C. However, to compare in parallel the

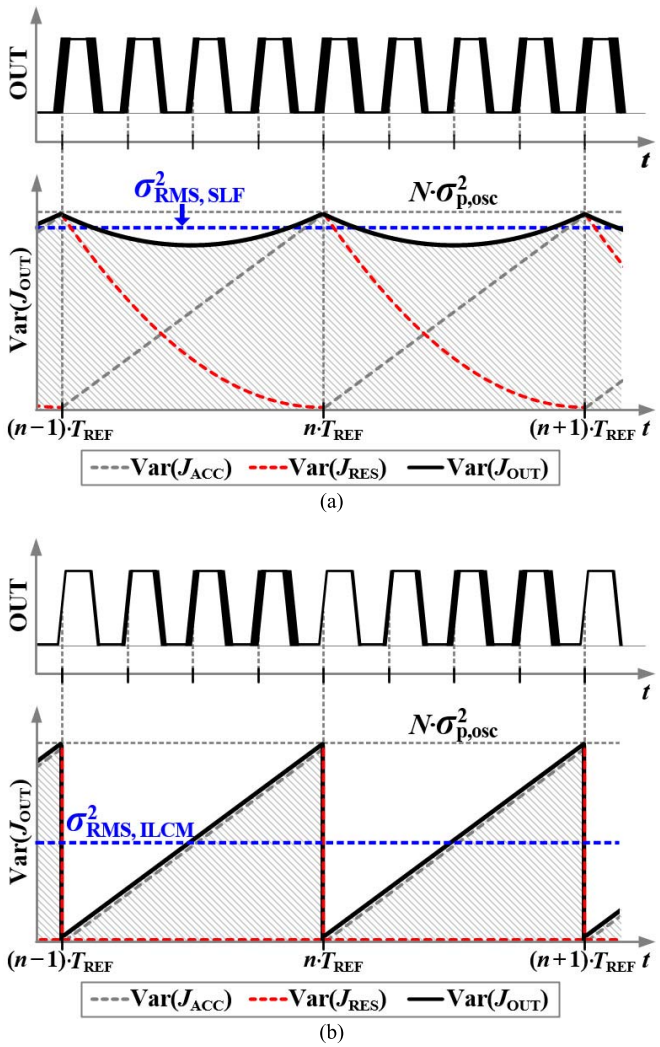


Fig. 2. Conceptual illustration of how rms jitter is determined differently according to phase-error correction mechanisms. (a) In conventional SLF-PLLs. (b) In ILCMs.

phase-realignment mechanism of an ILCM and that of an SLF PLL, we can represent the increase in V_C conceptually using a Dirac-delta function $\delta(t)$, as shown in Fig. 1(b). In doing so, the phase correction of an ILCM can be represented as if it included an integrator. Since β is 1, the total amount of the phase corrected over the T_{REF} also must be identical to $2\pi \cdot K_{\mathrm{VCO}} \cdot \Delta V_C \cdot T_{\mathrm{REF}}$.

Based on the analyses of the phase-error corrections, as shown in Fig. 1(a) and (b), the rms jitter of each architecture can be estimated theoretically. Since the purpose of this theoretical analysis is to compare the capabilities of suppressing the jitter of the VCO in the two architectures, it is adequate to consider only the thermal noise of the VCO rather than including the flicker noise. Similarly, noise from the reference clock or from other building blocks is not considered. To obtain a fair comparison, the same VCO is assumed in both architectures. Fig. 2(a) and (b) shows how differently the rms jitter σ_{rms} is determined in an SLF PLL and an ILCM, respectively. In Fig. 2(a) and (b), the black solid line represents the variance of the total output jitter J_{OUT}, which is obtained by superimposing the variances of the two jitter components assuming steady state. The first component (red dashed line) is the residual jitter of the VCO J_{RES}, which is accumulated in the previous T_{REF} and removed during the current T_{REF}, according to the corresponding phase-error-correction mechanism in Fig. 1(a) or (b). The second component is the jitter that is newly accumulated by the VCO during the current T_{REF} (gray dashed lines), J_{ACC}. Since the same VCO is assumed, the variance of J_{ACC} should be the same for both cases. As shown in Fig. 2(a) and (b), the variance of J_{ACC} increases linearly and reaches $N \cdot \sigma^2_{p,\mathrm{osc}}$ at the end of the current T_{REF} [30], [31], where N is the multiplication factor, and $\sigma_{p,\mathrm{osc}}$ is the standard deviation of the period jitter of the free-running VCO. (Note that the variances of J_{OUT}, J_{RES}, and J_{ACC} are time-varying values, while $\sigma_{p,\mathrm{osc}}$ is a constant value.) As a result, the difference in J_{OUT} of the two architectures should come from J_{RES} (red dashed line). As shown in Fig. 1(a), in an SLF PLL, $\Delta\phi_E$ is reduced linearly over time. Thus, in Fig. 2(a), the variance of J_{RES} of an SLF PLL at the nth reference period, i.e., $n \cdot T_{\mathrm{REF}} \leq t < (n+1) \cdot T_{\mathrm{REF}}$, can be represented as $N \cdot \sigma^2_{p,\mathrm{osc}} \cdot (1 - t - n \cdot T_{\mathrm{REF}})/T_{\mathrm{REF}})^2$. On the other hand, as shown in Fig. 1(b), an ILCM is able to eliminate $\Delta\phi_E$ momentarily at the beginning of a T_{REF}; thus, no J_{RES} must be remained in the current T_{REF}, as shown in Fig. 2(b). Due to the difference of J_{RES}s stemming from the difference of the phase-error-correction mechanisms, the total sum of the variances of the two jitter components (or the area under the black line) is much smaller in ILCMs. Consequently, ILCMs can achieve a much lower value of rms jitter than conventional SLF PLLs.

B. Concept of the Proposed Fast Phase-Error Correction Technique

The preceding analysis shows that FPEC by the phase-realignment mechanism of an ILCM is the reason for its low jitter. From this observation, we developed the FPEC technique that emulates the phase-realignment mechanism of an ILCM. In the proposed FPEC technique, the process of correcting the phase error can be expedited by boosting the magnitude of ΔV_C during a short interval, as in the case of the ILCM in Fig. 1(b). Fig. 3 shows a conceptual timing diagram of the FPEC technique, which includes two different phase-correction periods: 1) the proportional period T_{PROP} and 2) the integral period T_{INT}. Even though T_{PROP} is short, the loop gain is set to very high so that V_C changes significantly like an impulse and $\Delta\phi_{E0}$ is removed rapidly. However, if the duration of the proportional period of T_{PROP} with a high loop gain is excessively extended, $\Delta\phi_{E0}$ could be overcorrected, and its magnitude could even increase, which would cause the loop to become unstable and degrade the performance of jitter. To avoid these problems, the loop gain is reduced during the long period of T_{INT} following T_{PROP} so that the remaining $\Delta\phi_{E0}$ can be removed slowly while maintaining a stable condition. As a result, by using the proposed FPEC technique, SLF PLLs can achieve ultralow jitter without concerns about stability. The phase-error correction of a conventional CP PLL with a continuous-time loop filter also is similar to the shape

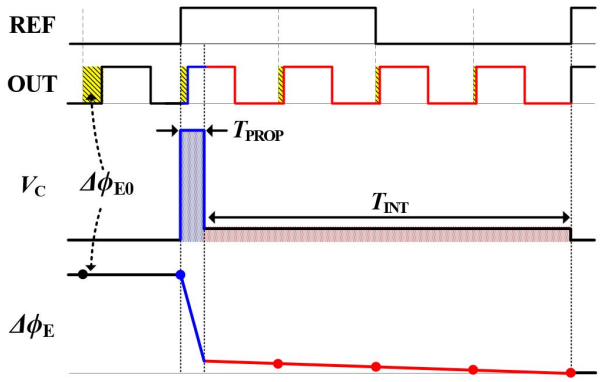


Fig. 3. Conceptual timing diagram of the proposed FPEC technique.

in Fig. 3, but it cannot suppress the jitter of the VCO as much as the FPEC technique because it has a tight tradeoff between jitter and the reference spur associated with the noise-reduction bandwidth of the loop [32].

Although the FPEC technique is based on a concept similar to the phase-realignment mechanism of ILCMs, it does not have the reference spur problem. As mentioned earlier, ILCMs cannot correct drifts of f_{VCO} due to the absence of the integrator of the VCO, which results in a large reference spur. Different from ILCMs, the transfer function of the proposed SLF PLL with the FPEC has the integrator of the VCO, so it can continue to correct any drifts of f_{VCO} in the locked state. Since the increase in phase error due to drifts of f_{VCO} remains at zero for N cycles of the VCO signal, the proposed SLF PLL also can achieve a low reference spur, despite a large value of N.

III. Implementation of the SLF PLL Using the FPEC Technique

A. Switched-Loop Filter Embodying the FPEC Technique

Fig. 4(a) and (b) shows the schematics and the timing diagram, respectively, of the proposed SLF embodying the FPEC. The main building components of the FPEC-SLF are three capacitors (C_P, C_I, and C_C) and three switches (SW_R, SW_P, and SW_I). The capacitances of C_P and C_I are the same, while that of C_C is much smaller than the other two capacitors, and these three capacitors are connected with or disconnected from each other selectively, based on the configurations of the switches. All three switches are open at the beginning of a new period, so, when the PD detects $\Delta\phi_{E0}$, C_P is charged with the corresponding amount of charges. Since the gain of the PD, K_{PD}, is very high, even a small phase error results in a large increase in V_P. Then, during T_{PROP} when SW_P is on and SW_I is off, V_P is connected to V_C. Since C_C is much smaller than C_P, V_C momentarily increases almost up to the value of V_P, quickly decreasing $\Delta\phi_{E0}$. The increase of V_C in T_{PROP}, i.e., $\Delta V_{C,P}$, can be represented as

$$\Delta V_{C,P} = \Delta\phi_{E0} \cdot K_{\mathrm{PD}} \cdot \frac{C_P}{C_P + C_C}. \tag{1}$$

When SW_P is turned off and SW_I is turned on during T_{INT}, the connection of V_C is switched to V_I. Then, the frequency

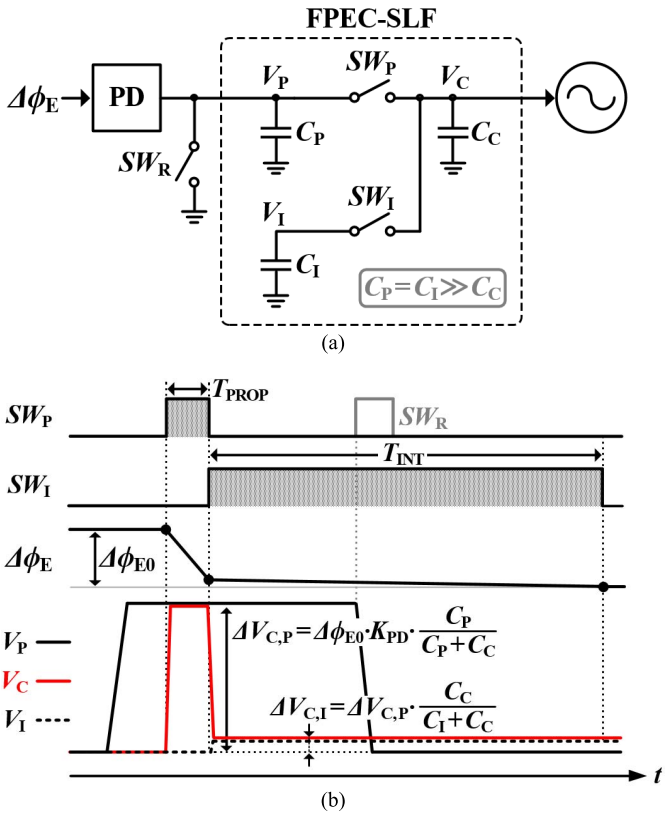


Fig. 4. (a) Schematics of the proposed SLF embodying the FPEC. (b) Operation of the FPEC-SLF.

information of the VCO in C_I is updated by the new information in C_C. Since C_I is much larger than C_C, the loop gain during T_{INT} becomes very small, and the stability of the loop can be maintained. As the charge on C_C moves into C_I, $\Delta V_{C,P}$ decreases as a factor of $C_C/(C_I + C_C)$, and the net change of V_C in T_{INT} with respect to its initial value, $\Delta V_{C,I}$, can be represented as

$$\Delta V_{C,I} = \Delta V_{C,P} \cdot \frac{C_C}{C_I + C_C}. \tag{2}$$

In the middle of T_{INT}, when SW_R is turned on, V_P is initialized to prepare the next phase-error-correction cycle. By using (1) and (2), the amount of the phase-error correction $\Delta\phi_{\mathrm{CORR}}$ can be represented as

$$\begin{aligned}\Delta\phi_{\mathrm{CORR}} &= 2\pi \cdot K_{\mathrm{VCO}} \cdot \int_0^{T_{\mathrm{REF}}} \Delta V_C(t) \cdot dt \\ &= 2\pi \cdot K_{\mathrm{VCO}} \cdot (\Delta V_{\mathrm{C,P}} \cdot T_{\mathrm{PROP}} + \Delta V_{\mathrm{C,I}} \cdot T_{\mathrm{INT}}).\end{aligned} \tag{3}$$

Then, β can be represented as

$$\begin{aligned}\beta = \frac{\Delta\phi_{\mathrm{CORR}}}{\Delta\phi_{\mathrm{E0}}} &= 2\pi \cdot K_{\mathrm{VCO}} \cdot K_{\mathrm{PD}} \cdot \frac{C_{\mathrm{P}}}{C_{\mathrm{P}} + C_{\mathrm{C}}} \cdot T_{\mathrm{PROP}} \\ &\quad \cdot \left(1 + \frac{C_{\mathrm{C}}}{C_{\mathrm{I}} + C_{\mathrm{C}}} \cdot \frac{T_{\mathrm{INT}}}{T_{\mathrm{PROP}}}\right)\end{aligned} \tag{4}$$

where the units of K_{VCO} and K_{PD} are [Hz/V] and [V/rad], respectively. Here, one radian corresponds to $T_{\mathrm{VCO}}/2\pi$, where T_{VCO} is the period of the VCO. To minimize rms jitter, β must be close to one. Then, the detected phase error is completely

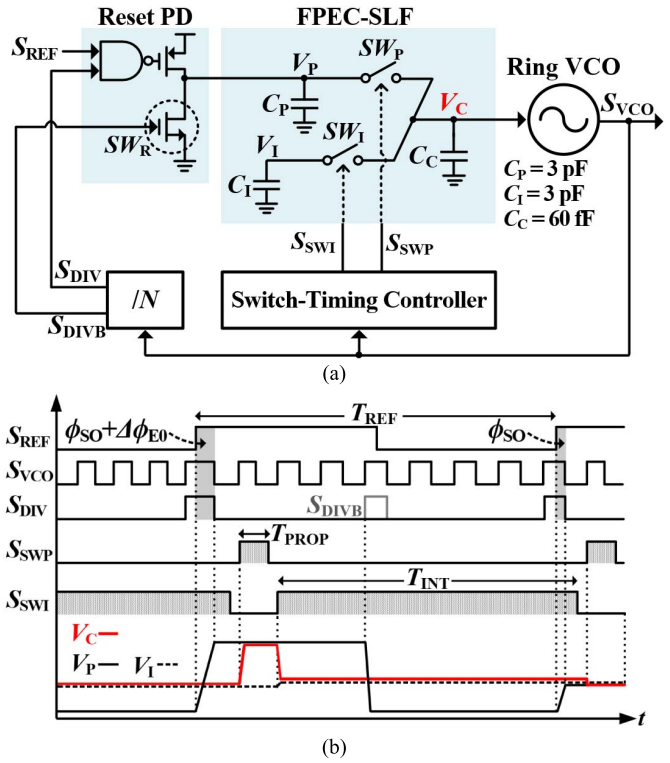


Fig. 5. Proposed SLF PLL with an FPEC technique. (a) Overall architecture. (b) Timing diagram.

corrected during the current T_{REF} and not transferred to the next T_{REF}. How the loop parameters were designed is explained in Section III-B.

B. Overall Architecture and Operation of the SLF PLL With the FPEC Technique

Fig. 5(a) shows the overall architecture of the proposed SLF PLL with the FPEC technique. It consists of the reset PD, the FPEC-SLF, the switch-timing controller, a ring-VCO, and a frequency divider. In the design of the FPEC-SLF, the capacitances of the three capacitors were selected as optimal values, i.e., C_P and C_I were 3 pF, and C_C was 60 fF. The rationale for selecting these values is explained in Section IV. Based on the timing of the output of the ring VCO, the control signals, S_{SWP} and S_{SWI}, for the switches of SW_P and SW_I, respectively, were generated by the switch-timing controller to reconfigure the SLF dynamically. To minimize gate-leakage current, SW_P and SW_I are designed using thick-oxide transistors (thick-oxide NMOSs). In this paper, the switch to initialize charges in C_P, i.e., SW_R in Fig. 4(a), was implemented using an NMOS switch of the reset PD, and it was controlled by S_{DIVB}. The proposed PLL was designed to generate an output frequency of approximately 3 GHz, and the multiplication factor of N was fixed at 64.

Fig. 5(b) shows the timing diagram of the proposed SLF PLL in steady state. As shown in Fig. 5(b), when S_{REF} and S_{DIV} are delivered, the reset PD detects the phase error, $\phi_{SO} + \Delta\phi_{E0}$, where ϕ_{SO} is the static offset of the loop, and $\Delta\phi_{E0}$ is the initial phase error to be corrected. Since this paper is based on a Type-I PLL, a finite ϕ_{SO} is assumed to exist even in steady state. When S_{SWP} changes from low to high during T_{PROP}, V_C increases momentarily, reducing $\Delta\phi_{E0}$ rapidly in a short time. When S_{SWI} changes to high following S_{SWP}, then C_C and C_I start to share charges. During this long T_{INT}, the remainder of $\Delta\phi_{E0}$ is removed slowly, while the frequency of the VCO is adjusted. Theoretically, as the ratio of T_{PROP} to T_{REF} approaches zero, the operation of the proposed SLF PLL becomes closer to that of an ILCM, and lower rms jitter can be achieved. To estimate rms jitter with respect to T_{PROP}/T_{REF}, we performed behavior simulations using Simulink. In each simulation, we assumed that the phase error was corrected only during T_{PROP} and β was maintained to be one. As shown in Fig. 6, the normalized rms jitter, i.e., $\sigma_{rms}/(\sqrt{N}\sigma_{p,osc})$, decreases almost linearly as T_{PROP}/T_{REF} is reduced. However, in practice if T_{PROP}/T_{REF} is too small, the gain of the PD should increase excessively to make β close to one; then, the capture range of the proposed PLL would be reduced significantly, since the PD must operate like a bang-bang PD. Considering this issue, we designed the apparatus such that T_{PROP}/T_{REF} was 1/8. In this paper, K_{VCO} and K_{PD} were designed to be approximately 150 MHz/V and 0.4 V/rad (or 7.6 GV/s) to make β close to one.

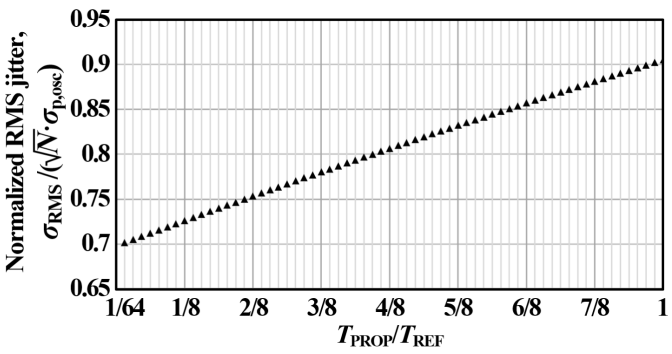


Fig. 6. Normalized rms jitter with respect to T_{PROP}/T_{VCO} when β is maintained to be one.

In the proposed FPEC-SLF, clock feedthroughs occur when S_{SWP} or S_{SWI} is toggled, and they could perturb the V_C of the VCO. If all stages were connected to V_C as in the case of a typical ring VCO, as shown in Fig. 7(a), the moment at which the perturbation of V_C occurred would coincide with at least one signal transition at the outputs of multiple stages, which would cause a huge fluctuation of f_{VCO}, and, as a result, a large reference spur. [In the case of Fig. 7(a), the falling edges of S_{D1} and S_{D3} were affected by S_{SWP} and S_{SWI}, respectively.] To address this problem, in this paper, we presented an SFT-ring VCO, as shown in Fig. 7(b). The proposed VCO is composed of five stages of an inverter-based delay cell, D_0–D_4. Different from conventional ring-VCO topologies, only the delay of D_4 is controlled by V_C through an NMOS pull-down transistor, M_C. Thus, the transitions at the outputs of the other delay cells can be excluded from the effect of the fluctuation of V_C. In addition, M_C is connected to S_{D4} through two cascaded NMOS switches, M_1 and M_0, which are enabled or disabled by S_{D1} and S_{D3}, respectively. According to the phases of S_{D1} and S_{D3}, M_C is connected to the VCO, only when S_{D4} changes from high to low in every period of the VCO; thus, V_C selectively controls only the

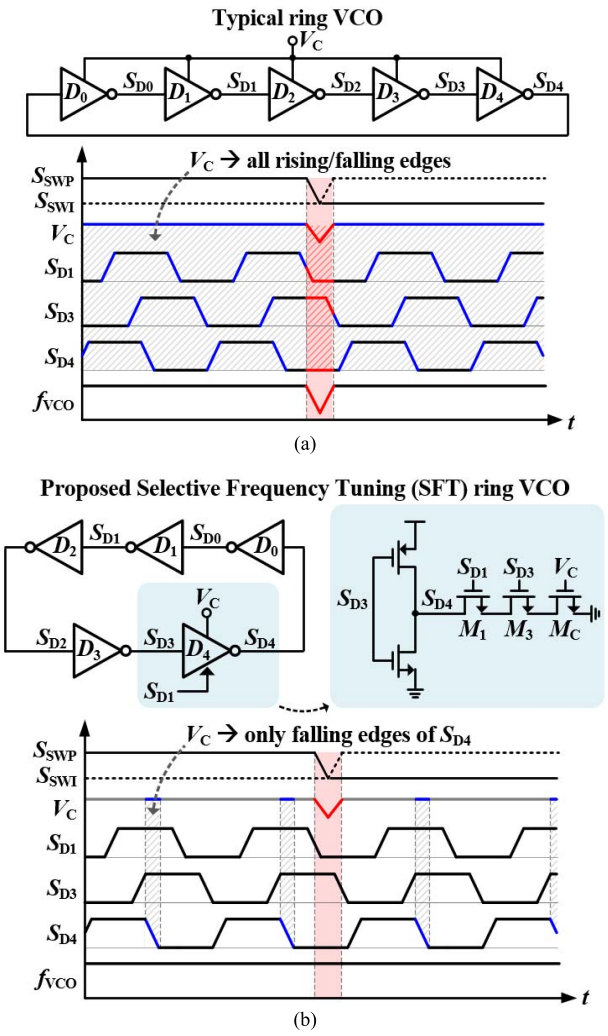


Fig. 7. (a) Typical ring-VCO with V_C connected to all stages. (b) Proposed SFT-ring VCO with V_C connected to only one stage.

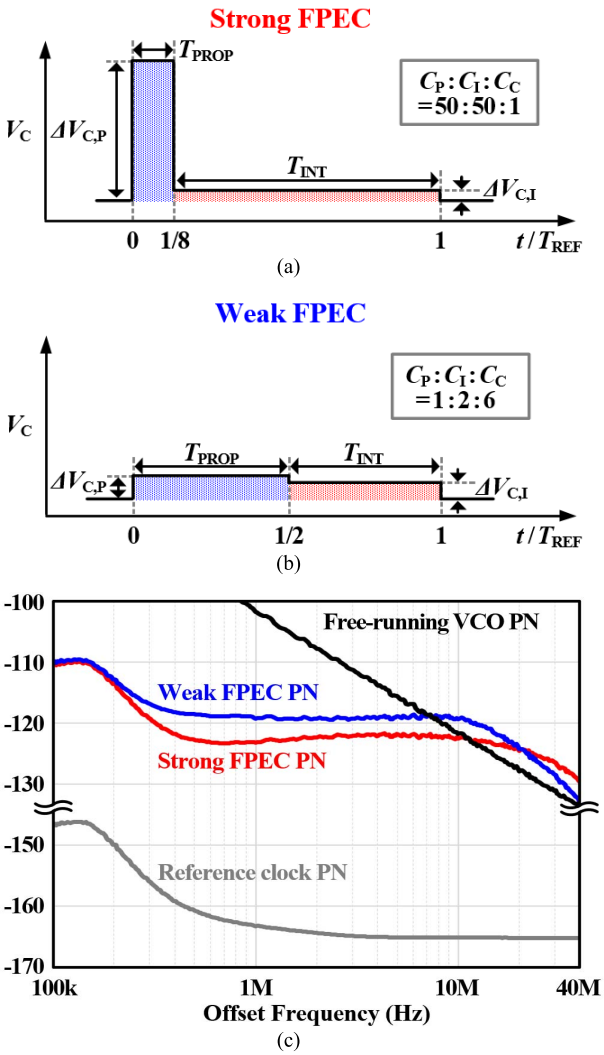


Fig. 8. (a) Case of the strong FPEC we designed. (b) Case of a relatively weaker FPEC. (c) Phase noise simulation with different strengths of the FPEC.

transition time of the falling edges of S_{D4}. Since these falling edges of S_{D4} should never be aligned with the moment of the fluctuation of V_C, S_{D4} is not affected by the fluctuation. Since the transition time of every falling edge of S_{D4} is adjusted by the same amount in steady state, the SFT technique of the proposed VCO does not cause any additional spurs. Despite a potential reduction of K_{VCO}, which was 150 MHz/V in this paper, the SFT technique was useful for minimizing the level of reference spur. According to post-layout simulation, the variation of K_{VCO} across V_C was approximately $\pm 30\%$ from the targeted value, i.e., 150 MHz/V. This variation would result in the deviation of the β of the loop from one, thereby increasing rms jitter. In this paper, we have initially calibrated β by controlling K_{PD}. (The PD was designed to have six-bit switchable PMOSs to change K_{PD}.) For a more complete design, a background gain calibrator [33] can be implemented to maintain β close to one regardless of the variation of K_{VCO}.

IV. Analysis on the Proposed FPEC Technique

A. Effect of Noise Reduction According to FPEC Strength and Design Considerations

To verify the effectiveness of the proposed FPEC technique, the amounts of the reduction of the VCO noise according to different strengths of the FPEC were compared through simulations. Fig. 8(a) shows the case of the FPEC that we designed. With the ratio of C_P to C_I to C_C as 50 to 50 to 1, the ratios of the durations and gains of T_{PROP} to T_{INT} became 1 to 7 and 51 to 1, respectively. Fig. 8(b) shows the case of an FPEC with significantly reduced strength; with the ratio of C_P to C_I to C_C as 1 to 2 to 6, the ratios of the durations and gains of T_{PROP} to T_{INT} change to 1 to 1 and 4 to 3, respectively. In the second case, since the gains of the two periods are similar, this SLF PLL with weak FPEC can be regarded to be very close to a conventional SLF PLL, where the loop gain is constant throughout a reference period. Since the capability of the phase-error correction was assumed to be the same in the two cases, i.e., β in each case was equal to 1, the sums of the two areas of T_{PROP} and T_{INT} also should be the same. To compare the reductions in the jitter of the VCO according to the different strengths of the FPEC technique, we performed simulations of phase noise for the cases shown in Fig. 8(a) and (b). The noise data of the free-running VCO was obtained from post-layout simulation, while that of the reference clock was measured. Fig. 8(c) shows the phase noises of SLF PLLs

with strong and weak FPEC in Fig. 8(a) and (b), respectively. As shown in Fig. 8(c), the PLL with a strong FPEC achieved lower in-band phase noise than the PLL with a weak FPEC by more than 3 dB at offset frequencies less than 20 MHz. This is because the stronger FPEC can remove the jitter of the VCO much faster, just as the phase-realignment mechanism of an ILCM can do. The two graphs of phase noise were similar at frequencies below 200 kHz, since the overall phase noise was dominated by the phase noise of the reference clock. At the out-band frequencies above approximately 8 MHz, it was observed that the phase noises of the FPEC PLLs were 3 dB higher than that of the free-running VCO. This is because the abrupt change in J_{OUT} by the FPEC operation is supposed to increase the levels of high-frequency components in the power spectral density of J_{OUT} [34]. Since this effect becomes more significant as the strength of the FPEC increases, the strong FPEC PLL has higher phase noise around 40 MHz than the weak FPEC PLL. However, since the phase noise at these high offsets provides less contribution, the strong FPEC PLL can achieve still much lower rms jitter.

While the ratio between the three capacitors determines the strength of the FPEC, their capacitances affect the amount of noise contributed to the overall in-band noise by the FPEC-SLF and the PD. Thus, we decided the values of C_P, C_I, and C_C carefully using the following design considerations. First, to strengthen the magnitude of the FPEC, C_C should be far smaller than C_P and C_I. However, since the kT/C noise from the thermal noise of SW_P and SW_I must increase as C_C decreases, the value of C_C should not be reduced too much. Thus, to prevent the degradation of in-band phase noise, C_C was designed to have a capacitance of 60 fF. Second, when deciding the value of C_P, we considered the noise contribution of the reset PD. When the reset PD charges C_P, its thermal noise is supposed to be delivered to V_P. However, this effect can be minimized by increasing the value of C_P. Since a large capacitance of C_P is also good at increasing the strength of the FPEC, it is better to increase its value as far as its area occupancy is allowed. Considering this tradeoff, C_P was designed to have a capacitance of 3 pF. When the noise data from the post-layout simulations were used, the levels of the in-band phase noise of the FPEC-SLF and the reset PD were calculated to be less than -140 dBc/Hz and -152 dBc/Hz, respectively, which were negligible compared to the overall phase noise. To minimize the effect of clock feedthrough or charge injection in the FPEC SLF, C_I was designed to be identical to C_P, just as SW_I was to SW_P. As a result, the ratio of the capacitances of C_P to C_I to C_C became 50 to 50 to 1, which ensured that the FPEC technique had sufficient strength, as shown in Fig. 8(c).

B. Transient Behavior of the FPEC-SLF PLL for Frequency Acquisition

Fig. 9 shows the transient behavior, when the proposed FPEC-SLF PLL obtained the frequency acquisition. In Fig. 9, we assumed that f_{VCO} was smaller than the target frequency and that $\Delta\phi_E$ has $\Delta\phi_{E0}$ and ϕ_{SO} at the beginning. Due to the large initial difference between f_{VCO} and the target

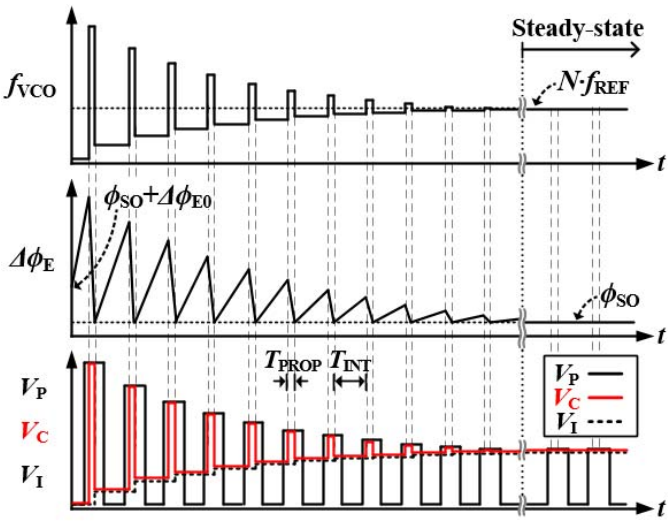


Fig. 9. Transient behavior of the proposed SLF PLL with the FPEC technique when f_{VCO} was smaller than the target frequency. ($\Delta\phi_E$ consists of $\Delta\phi_{E0}$ and ϕ_{SO}).

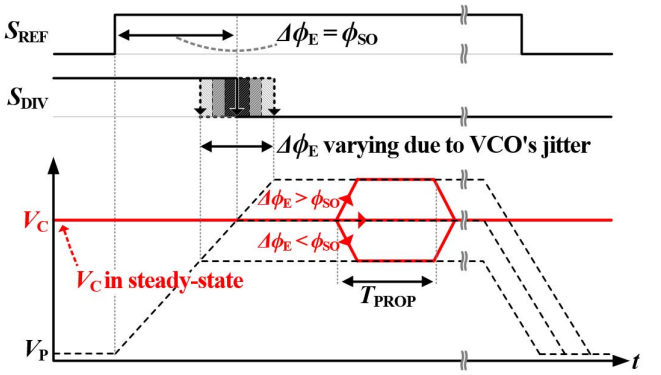
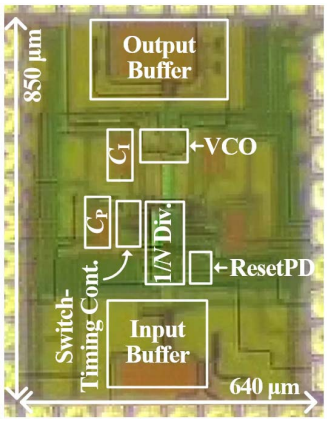


Fig. 10. Illustration of how V_P and V_C change to correct $\Delta\phi_E$ in steady state.

frequency, $\Delta\phi_E$ accumulates over time after the operation starts. During the following T_{PROP}, $\Delta\phi_E$ is decreased sharply by the FPEC operation, where the loop has a high gain, resulting in significant increases in V_C. When the operation of the loop enters T_{INT}, V_C decreases and V_I increases as C_C and C_I share charges. Since f_{VCO} is still smaller than the target frequency, $\Delta\phi_E$ should increase again, as it did in the beginning. However, since the difference in the frequencies has affected the values of V_C and V_I, their values are greater than their initial values, and f_{VCO} is higher than the initial frequency. As this process is iterated, f_{VCO} approaches the target frequency, and the increase of $\Delta\phi_E$ in T_{INT} becomes smaller. When f_{VCO} finally reaches the target frequency, the PLL acquires the lock, all node voltages are settled, and $\Delta\phi_E$ in average becomes equal to ϕ_{SO}. Due to the high gain of the PD of this paper, ϕ_{SO} was less than 100 ps. Since ϕ_{SO} is small, the proposed architecture could look like a Type-II PLL, and, actually, the proposed SLF PLL using the FPEC technique also can be designed as a Type-II architecture. Even in steady state $\Delta\phi_E$, i.e., the distance between the rising edge of S_{REF} and the falling edge of S_{DIV}, varies instantaneously due to the jitter of the VCO. Fig. 10 presents how V_P and V_C



(a)

Power Consumption (mW)	
VCO	4.12
1/*N* Divider	0.24
Reset PD	0.14
Switch-Timing Controller	0.08
Total	4.58

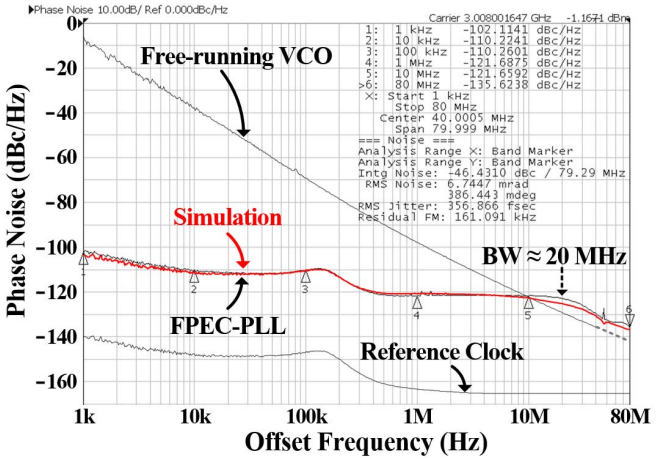
(b)

Fig. 11. (a) Die photograph. (b) Power-breakdown table.

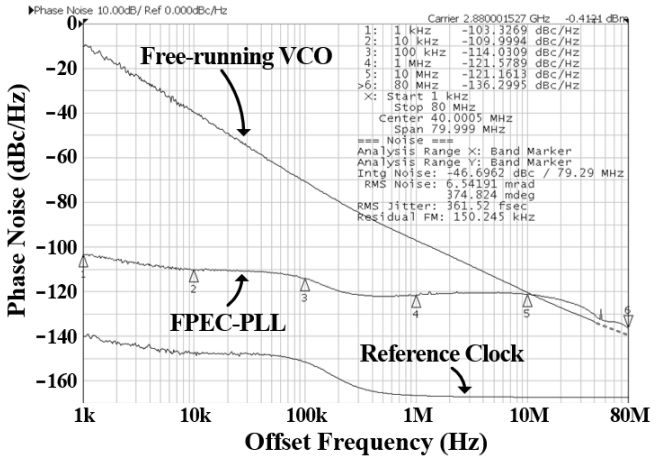
in the propose PLL change to correct the variation in $\Delta\phi_E$. When $\Delta\phi_E$ increases over ϕ_{SO}, V_P increases over the steady-state value of V_C, thereby increasing V_C momentarily during T_{PROP} to promptly correct $\Delta\phi_E$. When $\Delta\phi_E$ decreases, since the increase in V_P is less than the steady-state value of V_C, V_C is momentarily decreased to correct $\Delta\phi_E$.

V. Experimental Results

The proposed PLL was fabricated in a 65-nm CMOS technology, and the active area was 0.047 mm^2, as shown in Fig. 11(a). The supply voltage was 1.2 V, but the circuits driving SW$_P$ and SW$_I$ (thick-oxide NMOSs) used a 2.2-V supply. The total power consumption was approximately 4.6 mW; the VCO consumed 4.12 mW and other circuits of the loop, such as the reset PD, the switch-timing controller, and the divider, consumed 0.46 mW, as shown in Fig. 11(b). Fig. 12(a) shows the measured phase noise of the output signal with a frequency of 3.008 GHz, when a reference clock with a frequency of 47 MHz was used. A signal source analyzer, Agilent E5052B, was used to measure phase noise. As shown in Fig. 12(a), the proposed PLL achieved a very wide bandwidth more than 20 MHz (almost a half the frequency of the reference clock), which dramatically suppressed the jitter of the ring VCO. When the loop was turned off, the spot noise of the free-running VCO at the 1-MHz offset was −98.2 dBc/Hz. However, when the loop having the FPEC technique operated, the spot noise at the same offset was reduced to −121.6 dBc/Hz. As explained in Section IV, the phase noise of the FPEC PLL at out-band frequencies above 10 MHz is higher than that of the free-running VCO, because of the operation of the FPEC, emulating the phase-realignment mechanism of an ILCM. The difference between the two phase-noise curves around 20 MHz is slightly more than 3 dB. This is because the noise of the reference clock also was added to that of the output signal of the PLL. Since N was as large as 64, the elevation of the noise of the reference clock by 20log N was not negligible. The rms jitter integrated from 1 kHz to 80 MHz was only 357 fs. In Fig. 12(b), when the output frequency was 2.880 GHz from a 45-MHz reference clock, the phase noise at the 1-MHz offset and the RMS jitter were



(a)



(b)

Fig. 12. Measured phase noise of the output signals with a frequency of (a) 3.008 and (b) 2.880 GHz.

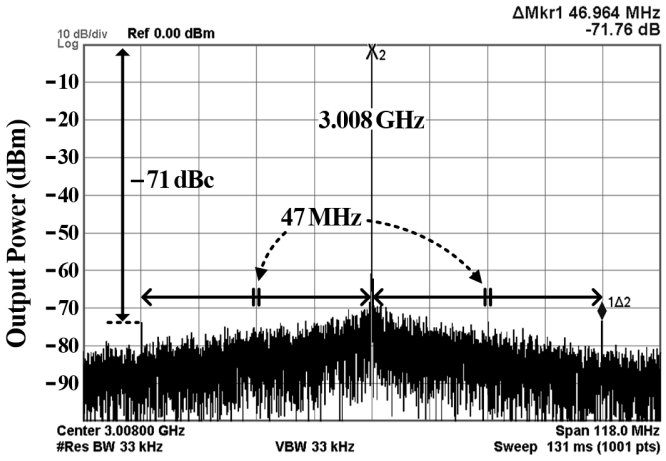


Fig. 13. Measured spectrum of the output signal with a frequency of 3.008 GHz.

−121.5 dBc/Hz and 362 fs, respectively. To move the free-running frequency of the VCO near 2.880 GHz, the supply voltage of the VCO was slightly lowered by 50 mV from 1.2 V, since K_{VCO} was relatively small for the VCO of the prototype PLL in this paper. For a complete design, a coarse frequency-tuning circuit can be added. Fig. 13 shows the output spectrum, measured by a spectrum analyzer, Agilent N9030A. As shown

TABLE I
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART RING-VCO-BASED CLOCK GENERATORS

	This work	JSSC'16 [17] S. Choi	ISSCC'17 [18] D. Coombs	ISSSC'16 [15] H. Kim	JSSC'16 [22] L. Kong	ISSCC'16 [21] K-Y. J. Shen
Process (CMOS)	65 nm	65 nm	65 nm	65 nm	65 nm	14 nm
Architecture	SLF-PLL w/ FPEC	ILCM	ILCM	MDLL	SLF-PLL	SLF-PLL
Out. freq., f_O (GHz)	3.008	1.2	5.0 (2.5 – 5.75)	2.4	2.4 (2.0 – 3.0)	4.0 (0.4 – 5.0)
Ref. freq. (MHz)	47	120	125	75	22.6	100
Mult. Factor (N)	64	10	40 (20 – 46)	32	106 (88 – 133)	40 (4 – 125)
1MHz PN (dBc/Hz) @ f_O (GHz)	−121.6 @ 3.008	–134.4 @ 1.2	–116.0 @ 5.0	–115.0 @ 2.4	–113.8 @ 2.4	–112.0 @ 4.0
Integ. jitter,σ_t (fs) (Integ. range)	357 (1k − 80MHz)	185 (10k − 40MHz)	340 (1k − 40MHz)	699 (10k − 40MHz)	970 (10k − 200MHz)	1264 (100k – 1GHz)
Ref. spur (dBc)	–71	–53	–45	–51	–65	N/A
Power, P_{DC} (mW)	4.6	9.5	5.3	1.51	4.0	2.6
Active area (mm^2)	0.047	0.06	0.09	0.024	0.015	0.021
*FOM_{JIT} (dB)	–242.3	–244.9	-242.4	–241.3	–234.1	–233.9

*FOM_{JIT}: $10\log_{10}(\sigma_t^2 \cdot P_{DC}(\text{mW}))$ (dB)

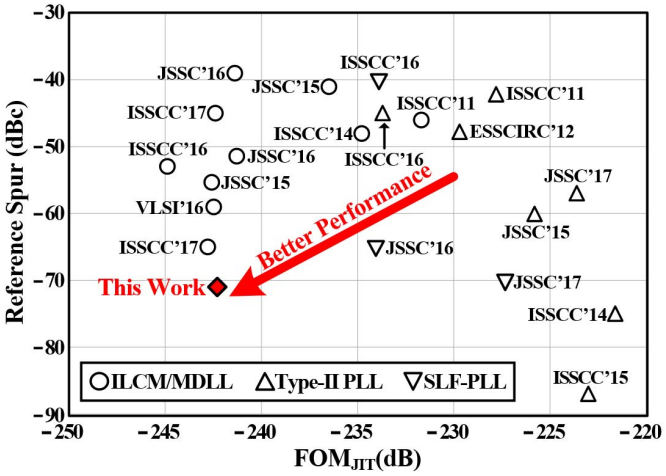


Fig. 14. Performance comparison with state-of-the-art ring-VCO-based clock generators where N is four or more.

in Fig. 13, when the output frequency was 3.008 GHz, the level of reference spur at the 47-MHz offset was −71 dBc.

Table I compares the performance of the proposed architecture with that of state-of-the-art ring-VCO-based clock generators. According to Table I, this paper achieved excellent performances of rms jitter and the figure-of-merit of jitter (FOM_{JIT}), which were almost comparable to those of ILCMs [17], [18] and a multiplying delay-locked loop (MDLL) [15], while it had a far lower reference spur and a larger N. Compared to conventional SLF PLLs [21], [22], this paper had lower rms jitter, thereby achieving much better FOM_{JIT}.

Fig. 14 compares the performances of the proposed FPEC-SLF PLL, in terms of FOM_{JIT} and the level of a reference spur, with those of the state-of-the-art ring-VCO-based clock generators based on ILCMs, MDLLs, type-II PLLs, and SLF PLLs, where N was four or more. Fig. 14 clearly shows that the proposed FPEC-PLL achieved the outstanding performances of jitter and reference spur, concurrently.

VI. CONCLUSION

In this paper, we presented a low-jitter and low-reference-spur ring-VCO-based SLF PLL, using the FPEC technique. By emulating the phase-realignment mechanism of an ILCM, the proposed PLL with the FPEC technique was capable of removing the accumulated jitter of a VCO intensively in a short interval. Therefore, while it used a ring VCO, the proposed PLL was able to generate output signals with an ultralow jitter performance like an ILCM. Since the transfer function of the proposed architecture included the integrator of the VCO, it could also achieve a low reference spur, despite having a large multiplication factor of N. This paper also presented the SFT technique for the design of a ring VCO to remove the effect of the clock feedthrough, caused when the switches in the FPEC-SLF were toggled. Consequently, the proposed SLF PLL with the FPEC technique was able to achieve ultralow jitter, low reference spur, and large N at the same time.

REFERENCES

[1] S. Ye, L. Jansson, and I. Galton, "A multiple-crystal interface PLL with VCO realignment to reduce phase noise," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2002, pp. 447–478.
[2] S. Ye, L. Jansson, and I. Galton, "A multiple-crystal interface PLL with VCO realignment to reduce phase noise," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1795–1803, Dec. 2002.

[3] B. Mesgarzadeh and A. Alvandpour, "First-harmonic injection-locked ring oscillators," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2006, pp. 733–736.

[4] P. Park, J. Park, H. Park, and S. Cho, "An all-digital clock generator using a fractionally injection-locked oscillator in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2012, pp. 336–337.

[5] S. Lee, S. Ikeda, H. Ito, S. Tanoi, N. Ishihara, and K. Masu, "An inductorless injection-locked PLL with 1/2- and 1/4-integral subharmonic locking in 90 nm CMOS," in *IEEE Radio Freq. Integr. Circuits Symp. (RFIC) Dig.*, Jun. 2012, pp. 189–192.

[6] W. Deng, A. Musa, T. Siriburanon, M. Miyahara, K. Okada, and A. Matsuzawa, "A 0.022 mm^2 970μW dual-loop injection-locked PLL with −243 dB FOM using synthesizable all-digital PVT calibration circuits," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 248–249.

[7] A. Musa, W. Deng, T. Siriburanon, M. Miyahara, K. Okada, and A. Matsuzawa, "A compact, low-power and low-jitter dual-loop injection locked PLL using all-digital PVT calibration," *IEEE J. Solid-State Circuits*, vol. 49, no. 1, pp. 50–60, Jan. 2014.

[8] W. Deng *et al.*, "A 0.0066 mm^2 780μW fully synthesizable PLL with a current-output DAC and an interpolative phase-coupled oscillator using edge-injection technique," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 266–267.

[9] W. Deng *et al.*, "A fully synthesizable all-digital PLL with interpolative phase coupled oscillator, current-output DAC, and fine-resolution digital varactor using gated edge injection technique," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 68–80, Jan. 2015.

[10] Y. Lee, M. Kim, T. Seong, and J. Choi, "A low phase noise injection-locked programmable reference clock multiplier with a two-phase PVT-calibrator for $\Delta\Sigma$ PLLs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 3, pp. 635–644, Mar. 2015.

[11] M. Kim, S. Choi, and J. Choi, "A 450-fs jitter PVT-robust fractional-resolution injection-locked clock multiplier using a DLL-based calibrator with replica-delay-cells," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2015, pp. C142–C143.

[12] M. Kim, S. Choi, T. Seong, and J. Choi, "A low-jitter and fractional-Resolution injection-locked clock multiplier using a DLL-based real-time PVT calibrator with replica-delay cells," *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 401–411, Feb. 2016.

[13] Z. Huang, B. Jiang, L. Li, and H. C. Luong, "A 4.2μs-settling-time 3rd-order 2.1 GHz phase-noise-rejection PLL using a cascaded time-amplified clock-skew sub-sampling DLL," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan./Feb. 2016, pp. 40–41.

[14] S. Choi, S. Yoo, and J. Choi, "A 185 fsRMS-integrated-jitter and −245 dB FOM PVT-robust ring-VCO-based injection-locked clock multiplier with a continuous frequency-tracking loop using a replica-delay cell and a dual-edge phase detector," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 194–195.

[15] H. Kim, Y. Kim, T. Kim, H. Park, and S. Cho, "A 2.4 GHz 1.5 mW digital MDLL using pulse-width comparator and double injection technique in 28 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. (ISSCC) Tech. Papers*, Jan./Feb. 2016, pp. 328–329.

[16] Y. Lee, H. Yoon, M. Kim, and J. Choi, "A PVT-robust −59-dBc reference spur and 450-fsRMS jitter injection-locked clock multiplier using a voltage-domain period-calibrating loop," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2016, pp. C238–C239.

[17] S. Choi, S. Yoo, Y. Lim, and J. Choi, "A PVT-robust and low-jitter ring-VCO-based injection-locked clock multiplier with a continuous frequency-tracking loop using a replica-delay cell and a dual-edge phase detector," *IEEE J. Solid-State Circuits*, vol. 51, no. 8, pp. 1878–1889, Aug. 2016.

[18] D. Coombs, A. Elkholy, R. K. Nandwana, A. Elmallah, and P. K. Hanumolu, "A 2.5-to-5.75 GHz 5 mW 0.3 psrms-jitter cascaded ring-based digital injection-locked clock multiplier in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 152–153.

[19] S. Kim *et al.*, "A 2.5 GHz injection-locked ADPLL with 197 fsRMS integrated jitter and −65 dBc reference spur using time-division dual calibration," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 494–495.

[20] L. Kong and B. Razavi, "A 2.4 GHz 4 mW inductorless RF synthesizer," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

[21] K.-Y. J. Shen *et al.*, "A 0.17-to-3.5 mW 0.15-to-5 GHz SoC PLL with 15 dB built-in supply noise rejection and self-bandwidth control in 14 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 330–331.

[22] L. Kong and B. Razavi, "A 2.4 GHz 4 mW integer-N inductorless RF synthesizer," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 626–635, Mar. 2016.

[23] L. Kong and B. Razavi, "A 2.4-GHz 6.4-mW fractional-N inductorless RF synthesizer," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2016, pp. C236–C237.

[24] L. Kong and B. Razavi, "A 2.4 GHz RF fractional-N synthesizer with 0.25 fREF BW," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 330–331.

[25] L. Kong and B. Razavi, "A 2.4-GHz 6.4-mW fractional-N inductorless RF synthesizer," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 2117–2127, Aug. 2017.

[26] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, Sep. 2004.

[27] B. M. Helal, C. M. Hsu, K. Johnson, and M. H. Perrott, "A low jitter programmable clock multiplier based on a pulse injection-locked oscillator with a highly-digital tuning loop," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1391–1400, May 2009.

[28] B. Razavi, *RF Microelectronics*. Upper Saddle River, NJ, USA: Prentice-Hall, 2011.

[29] T. Seong, Y. Lee, S. Yoo, and J. Choi, "A −242-dB FOM and −71-dBc reference spur ring-VCO-based ultra-low-jitter switched-loop-filter PLL using a fast phase-error correction technique," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2017, pp. C186–C187.

[30] R. Navid, T. H. Lee, and R. W. Dutton, "Minimum achievable phase noise of RC oscillators," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 630–637, Mar. 2005.

[31] A. A. Abidi, "Phase noise and jitter in CMOS ring oscillators," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1803–1816, Aug. 2006.

[32] A. Homayoun and B. Razavi, "On the stability of charge-pump phase-locked loops," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 6, pp. 741–750, Jun. 2016.

[33] T.-K. Kuan and S.-I. Liu, "A loop gain optimization technique for integer-*N* TDC-based phase-locked loops," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 7, pp. 1873–1882, Jul. 2015.

[34] N. Da Dalt, "An analysis of phase noise in realigned VCOs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 3, pp. 143–147, Mar. 2014.

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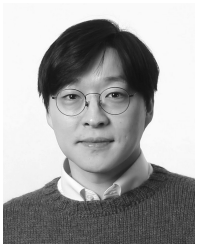

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