A 2.4-GHz, Sub-1-V, 2.8-dB NF, 475-μW Dual-Path Noise and Nonlinearity Cancelling LNA for Ultra-Low-Power Radios

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Abstract—A 0.7-V, 2.4-GHz low-power LNA combines a 1:3 front-end balun with dual-path noise and nonlinearity cancellation for the improved noise performance at low powers. In traditional noise cancellation techniques, only the noise of the main path is cancelled, while the noise of the auxiliary path is reduced by using higher power. In the proposed design, the noise and nonlinearity of both the main and the auxiliary paths are mutually cancelled allowing for low-power operation. The 2.8-dB noise figure, $-10.7~{\rm dBm}$ third-order input intercept point LNA in a Taiwan Semiconductor Manufacturing Company (TSMC)'s 65-nm GP process consumes 475 $\mu{\rm W}$ of power resulting in an figure of merit of 28.8 dB, which is 8.2 dB better than the state of the art.

Index Terms—802.15.6, low power, noise cancellation, receiver, RF, ultra-low-power radio, ultra-low power receiver, wireless body area network (WBAN).

I. INTRODUCTION

THERE is an increasing demand for low-power radios with the proliferation of the Internet of Things (IoT), wireless body area networks (WBANs), and next generation 5G [1]–[4]. A WBAN is a network of medical sensors or actuators on, in, or around the human body using wireless connectivity. WBAN is capable of revolutionizing future health care. A typical WBAN scenario includes a network of medical sensors for monitoring vital statistics, such as temperature, blood sugar, and heart rate, and actuators, such as insulin pumps, cardiac pacemakers, and so on. By connecting these devices with a local base unit, e.g., a cell phone, WBAN will enable remote patient monitoring by providing doctors with real-time vital data. This will result in reduced health care costs and early detection and prevention of diseases. Remote patient monitoring will significantly benefit the aging population in regions where there is a scarcity of clinics and clinicians. Furthermore, the wireless connectivity can facilitate untethered patient monitoring without limiting patient movement. However, all these devices require radios, which can transmit

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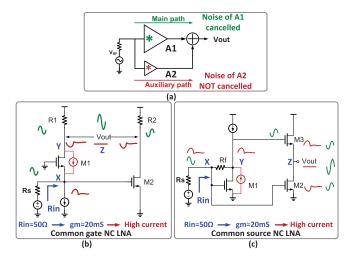


Fig. 1. Traditional NC LNA and their shortcomings. (a) Traditional NC LNA mechanism. (b) Traditional common gate NC LNA. (c) Traditional common source NC LNA.

and receive signals in order to maintain wireless connectivity. As most of these devices are likely to be powered by small batteries, their radios have to be extremely power efficient. The IEEE 802.15.6 standard provides the necessary specifications for such low-power radios [5].

With the proliferation of wireless technology in the last two decades, a plethora of "things" have Internet connectivity. This has led to the so-called IoT, which is a network of objects, animals, and people, provided with an IP address and the ability to transfer data without human-to-human or human-to-computer interaction. Cisco has predicted that 50 billion items will be connected to the Internet by 2020 [6]. However, in order to minimize the impact of such devices on the environment and on energy consumption, the power consumption of these IoT radios should be extremely low when deployed for Internet connectivity. In addition, many of these nodes will not have continuous access to power and are likely to use small batteries further increasing the need for low-power radios.

The rapid scaling of the power supply $(V_{\rm dd})$ with technology reduces power consumption in digital circuits where the power consumed can be expressed as $\approx CV_{\rm dd}^2f$. This facilitates the power reduction in modern radios that have large digital blocks. Therefore, it is preferable to use sub-1-V circuits in order to reduce power and accommodate technology scaling. However, low $V_{\rm dd}$ degrades the SNR of the RF front end, which can be partially restored by using noise cancelling (NC) techniques. Unfortunately, traditional NC

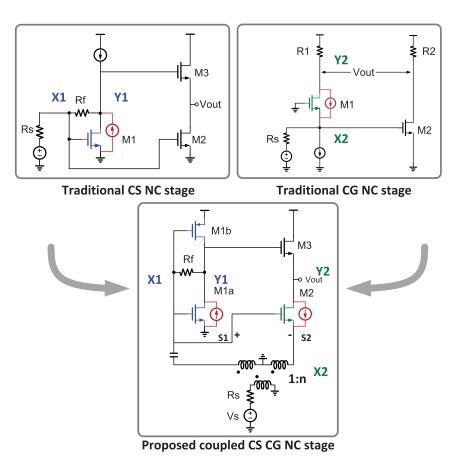


Fig. 2. Combining traditional CS and CG NC LNA stages to form a coupled CS-CG NC LNA.

LNAs are power hungry and are not well suited for low-power operation [7]–[10].

Traditional NC techniques are based on the availability of two suitable nodes X and Y in the circuit where the signals are in phase but the noise of the main path is out of phase at these nodes, as shown in Fig. 1(a). NC LNAs have been realized as either common source (CS) [8] or as common gate (CG) [7] amplifiers. For both these designs, the input impedance is provided by an input transistor M1 as $Z_{in} = 1/g_{m_1}$ (i.e., CG or high gain with resistive feedback). For $Z_{\rm in} = 50 \ \Omega$, the required g_m is 20 mS, which necessitates that the power is greater than 1.5 mA even for low $(V_{\rm GS} - V_{\rm TH}) = 150$ mV. Larger $(V_{\rm GS} - V_{\rm TH})$ is required for higher linearity but results in increased power. Furthermore, the noise of the auxiliary path (M2) does not get cancelled; and therefore, to improve the overall noise figure (NF), g_{m_2} is increased at the cost of higher current [Fig. 1(b) and (c)]. Mutual noise cancellation has been reported in a nonlinearity mixer-based RF front ends [11], [12] where the noise of both the main and auxiliary paths are cancelled by virtue of the mutual inductance of a differential inductor, but the technique cannot be easily ported to other designs. This paper focuses on mutual noise cancellation in the LNA itself making it more versatile. The LNA design in this paper encompasses the frequency bands for the IEEE 802.15.6 narrowband standard, the industrial-scientific-medical band, the U.S. medical body area network (MBAN), and the European MBAN bands spanning 2.3-2.5 GHz.

A subset of this paper has been presented at [13]. Here, we have expanded the work [11] with additional analysis and new simulation results, including the impact of process variation and mismatch using Monte Carlo simulations and additional test setup details. Section II provides the circuit diagram for the LNA and explains the CS and CG noise cancellation mechanisms and matching requirement as well as simulations. Section III provides an analysis of the signal addition, noise cancellation, and nonlinearity cancellation mechanisms. Section IV describes the impact of process variation and mismatch. Section V provides simulation and measurement results. Finally, Section VI concludes this paper.

II. CIRCUIT DESIGN

We propose a dual-path NC LNA, which is a hybrid of the CS and the CG NC LNAs coupled together using the two secondary turns of a step-up balun, as shown in Fig. 2. The CG stage acts as the auxiliary path for the CS stage and vice versa. As a result, the noise of both stages gets cancelled. The input stage consists of a 1:3 balun. The secondary S1 of the balun is connected to a class AB inverter stage consisting of transistors M1a and M1b acting as a CS amplifier (A1). The secondary S2 of the balun is connected to a CG stage formed by M2 (A2). Here, A1 (CS amplifier) and A2 (CG amplifier) form the two parallel amplifiers that provide gain. If a differential output is required then an active or a passive balun could be used at the output node.

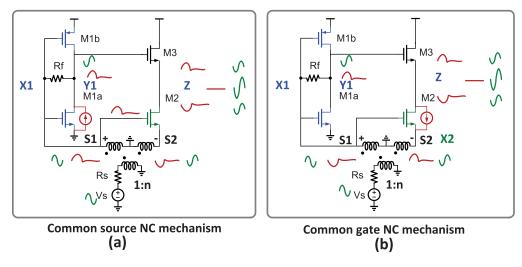


Fig. 3. Noise cancellation mechanism in the proposed LNA. (a) CS NC mechanism. (b) CG NC mechanism.

A. CS Noise Cancellation

As shown in Fig. 3(a), for the noise cancellation of the CS amplifier, M1a/M1b forms the main path and M2 forms the auxiliary path. The noise current of M1a and M1b flows through R_f and R_{s1} , where R_{s1} is the impedance-transformed input source resistance at S1. This results in two in-phase instantaneous noise voltages at Y1 and X1. The noise voltage at X1 is inverted at Z by M2. Note that M2 is a g_m -boosted stage, as the two secondary terminals of the balun, i.e., S1 and S2, provide opposite signal phases. The noise voltage at Y1 appears in phase at Z due to the source follower formed by M3. Since the noise voltages from the main and auxiliary paths are out of phase, they get cancelled at the output Z [Fig. 3(a)].

B. CG Noise Cancellation

For the noise cancellation of the CG amplifier [Fig. 3(b)], M2 forms the main path and M1a/M1b forms the auxiliary path. The noise current of M2 flows through R_{s2} , which is the impedance-transformed input source resistance seen at S2. This current is also drawn through M3. As a result, the noise voltages at nodes X2 and Z are inversely correlated. The noise voltage at the input X2 undergoes phase inversion at node X1, because S1 and S2 form an inverting transformer. This noise at X1 is inverted by M1a/M1b and propagated by the source follower (M3) to cancel the primary path noise. On the other hand, the signal voltages from the two paths are in phase at the output Z and get added. The signal voltage is inverted at Z after passing through the path formed by S1, the inverter, and the source follower. The signal voltage is also inverted at Z after passing through the path formed by S2 and the CG stage. The mutual coupling between the two stages using the mutual inductance of S1 and S2 of the balun facilitates dual-path noise cancellation. In addition to noise, the nonlinearity of the input transistors M1a/M1b and M2 is also cancelled. This is because, similar to noise, the nonlinearity in the drain current due to g_m/g_{ds} can be modeled as dependent current sources between the drain and the source [7].

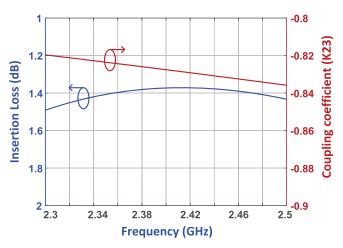


Fig. 4. IL and coupling between secondaries of the balun.

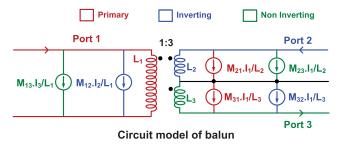


Fig. 5. Circuit model for the balun.

$C. Z_{in}$

The 1:3 balun transforms the $R_s = 50-\Omega$ source resistance to a 450- Ω differential resistance reducing the required g_m for impedance matching by nine times. As shown in Fig. 4, at 2.4 GHz, the simulated insertion loss (IL) of the balun is 1.4 dB, and the coupling coefficient (k) between the two secondaries is -0.83. An equivalent circuit model for the balun [14], [15] is shown in Fig. 5. Here, port 1 is the primary, port 2 is the inverting secondary, and port 3 is the noninverting secondary. Mxy are the mutual inductances and Lx are the self-inductances, where "x" and "y" are the various ports.

The CS stage is a current-reuse class AB amplifier, which achieves two times the g_m value on the same current. The two secondary terminals S1 and S2 that are connected to the gate and the source of M2 act as an inverting transformer and boost the g_m value by two times for the same current. Therefore, the effective g_m requirement for M2 is reduced by nine times. The secondary impedances seen by the left-hand side (S1) and the right-hand side (S2) of the balun are made equal in the balanced condition, i.e., $2 \cdot g_{m_2} = g_{m_1} = g_{m_{1a}} + g_{m_{1b}}$ such that $Z_{\text{in}} = 2/(9g_{m_1})$.

III. SIGNAL, NOISE, AND NONLINEARITY ANALYSIS

Next, we provide some theoretical analysis for signal addition and noise cancellation. This analysis is performed at RF under the assumption that the inductances associated with the balun terminals have been resonated out with appropriate capacitances, i.e., we only consider the real parts of circuits.

A. Signal Analysis

The signals through both feedforward paths are in phase, get added to each other, and can be expressed as follows, where n is the passive voltage gain of the balun:

$$A_{v} = A_{v1} + A_{v2}$$

$$A_{v1} = \frac{2n(1 - g_{m_1}R_f)(g_{m_3} + sC_{gs3})}{(2 + s(2C_{gd1} + 2C_{db1} + C_{gs3})(g_{m_3} + s(C_{gs3} + C_L))}$$
(2)

$$A_{v2} = \frac{-2ng_{m_2}g_{m_3}}{g_{m_3} + sC_L}. (3)$$

B. Noise Analysis

The circuit has been designed to completely cancel the noise of M1a and M1b. Under this condition, the gain required [8] of the auxiliary path formed by M2 is as follows, where R_{s1} is the impedance-transformed input source resistance at S1 and $g_{m_1} = g_{m_{1a}} + g_{m_{1b}}$:

$$A_{v2} = n(1 + R_f/R_{s1}). (4)$$

Let us now focus on the noise cancellation mechanism of M2 as shown in Fig. 6. The residual noise voltage V_{no} of M2 at the output after cancellation can be expressed as follows, where $V_{n\text{main}}$ is the path noise of M2 appearing at the output and $V_{n\text{aux}}$ is the path noise at the output due to M1a and M1b:

$$V_{no} = V_{n\text{main}} + V_{n\text{aux}} \tag{5}$$

$$V_{n\text{main}} = (3I_n/4)(1/(g_{m_3} + sC_L)) \tag{6}$$

$$V_{\text{naux}} = -(I_n R_{s1}/4)(A_{p1}/n). \tag{7}$$

Furthermore, the requirement on g_{m_1} and g_{m_2} for matching can be expressed as follows, where the factor 2 accounts for the g_m -boosting of M2:

$$g_{m_1} = 1/R_{s1} (8)$$

$$g_{m_2} = 1/(2R_{s2}). (9)$$

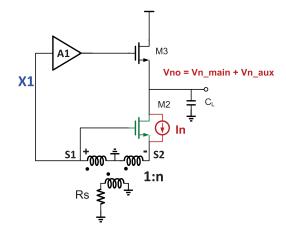


Fig. 6. Simplified model for noise cancellation of M2.

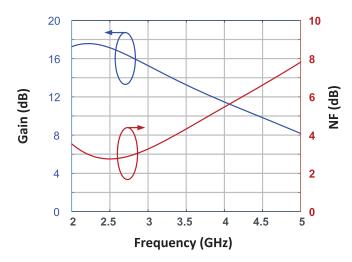


Fig. 7. Wideband simulation results for NF and gain.

Using (3), (4), (8), and (9) and eliminating g_{m_1} , g_{m_2} , and A_{v_2} , we can express g_{m_3} as follows:

$$g_{m_3} = 1/(R_f + R_{s1}) - sC_L. \tag{10}$$

Using (2), (5), (6), (7), and (10), the residual noise (V_{no}^2) of M2 at the output can be expressed as $(1/4)V_n^2$ by excluding frequency-domain effects. Therefore, if the circuit is designed for the complete noise cancellation of A1 (M1a and M1b) then under these conditions, only 75% of the noise from A2 (M2) can be cancelled. The simulated noise figure and gain are shown over a wide frequency range of 2–5 GHz in Fig. 7 to demonstrate frequency effects. We note that the best noise cancellation occurs around the designed frequency of 2.4 GHz.

C. Nonlinearity Analysis

The nonlinearity of both the CS and CG transistors due to nonlinear input conductance and output conductance can be modeled as a dependent current source between the drain and the source, as shown in Fig. 8 [7]. These current sources are a function of both v_{gs} and v_{ds} and therefore include g_m nonlinearity, gds nonlinearity, and secondary effects, such as drain-induced barrier lowering. Mathematically, we can

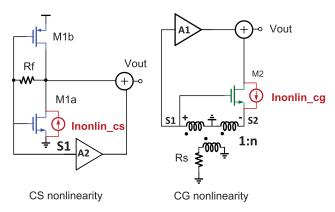


Fig. 8. Modeling nonlinearity for both the CS and the CG paths.

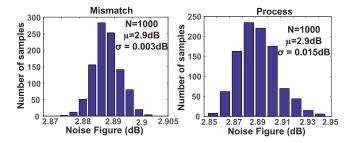


Fig. 9. Monte Carlo simulation results for noise figure.

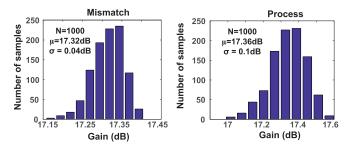


Fig. 10. Monte Carlo simulation results for gain.

express the drain current as a function of v_{gs} using the Taylor expansion shown in (11). The nonlinearity terms can be summed together as shown in (12)

$$I_{ds}(v_{gs}) = g_{m_1}V_{gs} + g_{m_2}v_{gs}^2 + g_{m_3}v_{gs}^3 + \dots$$
 (11)

$$I_{ds}(v_{gs}) = g_{m_1} V_{gs} + I_{\text{nonlin}}. \tag{12}$$

We can similarly model nonlinearity in terms of v_{ds} . The nonlinear component of drain current undergoes the same phase reversal mechanism as noise and gets cancelled in our proposed circuit. Since nonlinearity can be modeled as a current source similar to noise, we can achieve complete cancellation of nonlinearity of the CS device. Similarly, we can achieve 75% cancellation of the nonlinear terms for the CG device following the methodology used for noise cancellation derived in Section III.

IV. IMPACT OF PROCESS VARIATION AND MISMATCH

Monte Carlo simulations were performed using available models from the foundry to quantify the effect of process variation and device mismatch on the noise figure and the gain of the LNA. As shown in Fig. 9, the standard deviation

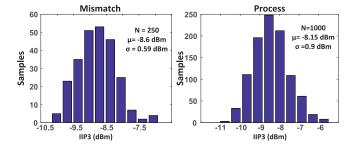


Fig. 11. Monte Carlo simulation results for IIP3.

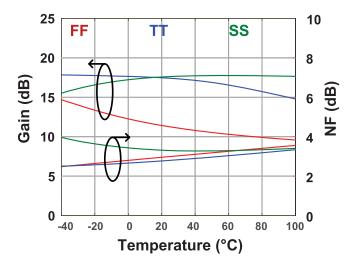


Fig. 12. Process corner simulation results for gain and noise figure versus temperature.

of the noise figure at 2.4 GHz is 0.015 dB due to process variation and 0.003 dB due to device mismatch. As shown in Fig. 10, the standard deviation of the gain at 2.4 GHz is 0.1 dB due to process variation and is 0.04 dB due to device mismatch. As shown in Fig. 11, the standard deviation of the third-order input intercept point (IIP3) is 0.9 dB due to process variation and is 0.59 dB due to device mismatch. Mismatch of Ls1 and Ls2 will lead to a mismatch in the noise transfer functions. However, with proper layout, the mismatch between inductances can be minimized. Mismatch between Lp and Ls1+Ls2 will lead to a drift in the value of n, which will lead to gain variation. Fig. 12 shows simulated gain and NF versus temperature for TT, SS, and FF corners. Across temperature range of -40 °C-100 °C, the gain variation is 2 dB at SS corner, 3 dB at TT corner, and 5.1 dB at FF corner, and the NF variation is 0.6 dB at SS corner, 0.8 dB at TT corner, and 1 dB at FF corner. Across 10% VDD variation, the gain variation is 0.75 dB and the NF variation is 0.5 dB, as shown in Fig. 13. The measured NF and IIP3 of the LNA over five samples are shown in Fig. 14. The measured P1dB of the LNA over five samples is shown in Fig. 15.

Next, we provide measurements results from the prototype design.

V. SIMULATION AND MEASUREMENT RESULTS

The prototype was implemented in Taiwan Semiconductor Manufacturing Company (TSMC)'s 65-nm CMOS

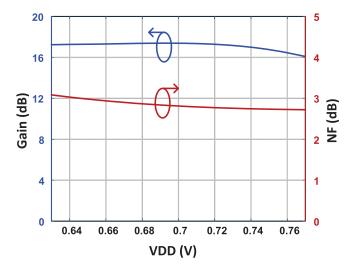


Fig. 13. Variation of gain and NF with V_{DD} .

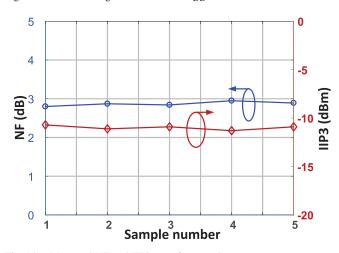


Fig. 14. Measured NF and IIP3 over five samples.

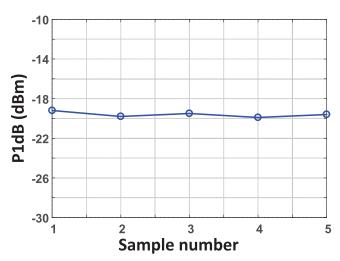


Fig. 15. Measured P1dB over five samples.

GP technology and occupies an area of 0.42 mm². The die-micrograph is shown in Fig. 16, and the test setup is shown in Fig. 17. The chip was tested by probing the die using the RF probes. The noise figure measurements were done using an Agilent 346A noise source and an R&S FSW43 spectrum analyzer with a noise figure measurement

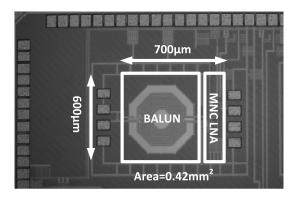


Fig. 16. Die-micrograph of the LNA.

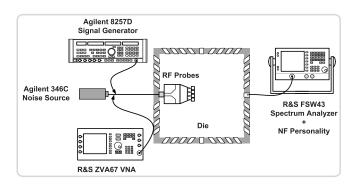


Fig. 17. Test setup for LNA measurement.

software. Linearity measurements were done using two-tone tests where the tones were generated using an Agilent's 8257D signal generator. The S11 measurements were done using an R&S ZVA67 vector network analyzer. All losses have been de-embedded in the measurements provided here.

For an ideal apples-to-apples comparison, we would have preferred to have two designs, one with noise cancellation and one without. However, it was not possible to have "no noise cancellation" without changing the topology. Therefore, the only fair comparison is to use the figure of merit (FOM) for LNAs. However, as a compromise, we implemented a separate design in silicon where we grounded the source of M2 (in A2) and kept the secondary of the balun open, such that the dual-path noise cancellation mechanism was partially suppressed and only the CS cancellation mechanism was active. Fig. 18 shows the measured and simulated NF with noise cancellation and with partial noise cancellation. The measured results match quite well with simulations in both cases. The full cancellation technique improves the partial cancellation design by reducing the NF by 2 dB. The measured NF at 2.3 GHz is 2.8 dB. The residual NF is mainly due to the IL of the balun, the residual noise of M2 (25%), and the uncancelled noise of R_f and M3. The noise contribution of balun, R_f , and M3 is, respectively, 29%, 6%, and 38% in simulation.

The measured gain at 2.3 GHz is 17.4 dB, and S11 is better than -13.5 dB throughout the frequency range as shown in Fig. 19. Fig. 20 shows the measured two-tone test output with cancellation and with partial cancellation.

		PERFORMANCE COMPARISON						
Reference	Freq.	NF	NC	Gain	-			
Number	[GHz]	[dB]	[Y/N]	[dB]				

Reference	Freq.	NF	NC	Gain	IIP3	Power	FOM
Number	[GHz]	[dB]	[Y/N]	[dB]	[dBm]	[mW]	[dB]
[8]	2	2.4	Y	13.7	0	35	14
[7]	5.2	3.5	Y	15.6	0	14	17.8
[18]	3	2.3	N	9.8	-7	12.6	13
[17]	2.46	4.7	N	20.2	-20	0.93	20.7
[19]	5	14.0	N	3.2	-8.0	0.8	9.6
[16]	2.4	11.8	N	12.7	-6.0	0.380	20.8
[20]	5	19	N	27	-3.0	1.0	18
[21]	2.4	18.3	N	15.7	-9.0	0.5	13.1
CS degenerated LNA	2.4	7.1	N	10.2	-8	0.49	22.2
Ours	2.4	2.8	Y	17.4	-10.7	0.475	28.8

TABLE I

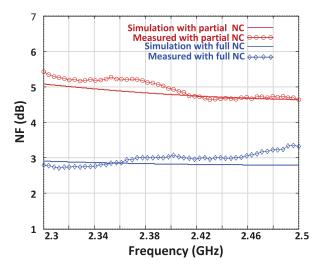


Fig. 18. Measured and simulated NFs with full and partial NC.

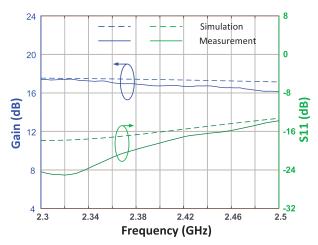


Fig. 19. Measured and simulated gain and S11 of the LNA.

In comparison to partial cancellation, the full cancellation technique improves the IIP3 of the LNA by 3.4 dB. The performance of the LNA is summarized and compared with state-of-the-art designs in Table I. The proposed design has the lowest power of 475 μ W and the highest FOM [16] of 28.8 dB, which is 8.2 dB higher than the state of the art for noise cancellation. For a fair comparison, the FOM is the

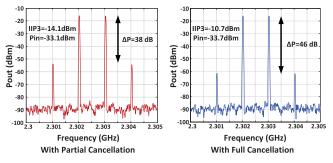


Fig. 20. Two-tone output spectrum with full and partial cancellation.

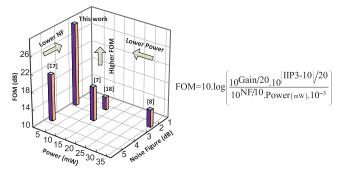


Fig. 21. FOM, power, and noise figure comparison.

best parameter, and an improvement in the FOM by 8.2 dB is very significant. This design has nearly 2 dB better NF and 10 dB better IIP3 than [17] while consuming half the power by virtue of the mutual noise and nonlinearity cancellation. It has similar NF and 3.7 dB lower IIP3 but 26.5 times lower power than [10]. The simulated IIP3 of the LNA is -8.6 dBm. The measured and simulated IIP2 is 7.2 and 9.78 dBm, respectively. Table I also shows the simulated performance of a standard CS inductively degenerated LNA in the same TSMC 65-nm process with 0.7-V supply and $700-\mu A$ bias current. The CS LNA has a noise figure of 7.1 dB, an IIP3 of -8 dBm, a gain of 10.2 dB, and an FOM of 22.2 dB, which is 6.6 dB worse than our design. Fig. 21 shows a 3-D bar chart of the various designs displaying the FOM, the power, and noise figures. It is clearly visible that the proposed design improves the FOM in terms of the linearity, noise figure, and power.

VI. CONCLUSION

We have proposed a dual-path mutual noise cancellation technique that improves the NF, nonlinearity, and power consumption of fully integrated LNAs with on-chip matching suitable for sub-1-V operation. In traditional noise cancellation techniques, the noise of the auxiliary path is suppressed by burning significant power. In contrast, we have proposed a dual-path NC technique, which mutually cancels the noise and nonlinearity of both the main (A1) and auxiliary paths (A2). This is achieved by using a balun whose secondary acts as an inverting transformer and passively couples noise from both paths by virtue of its reciprocity. The step-up balun provides voltage gain and relaxes the g_m requirement for matching of the input transistors, thereby reducing power. The loss in IIP3 due to passive voltage gain from the balun is compensated by nonlinearity cancellation inherent to these techniques. The circuit exploits current reuse and g_m -boosting for low power. This design shows that low-power noise cancellation techniques are feasible.

REFERENCES

- [1] M. Rahman, M. Elbadry, and R. Harjani, "A 2.5 nJ/bit multiband (MBAN & ISM) transmitter for IEEE 802.15.6 based on a hybrid polyphase-MUX/ILO based modulator," in *Proc. IEEE RFIC*, Jun. 2014, pp. 17–20.
- [2] S. Pellerano, A. Mirzaei, C. M. Hung, J. Craninckx, K. Okada, and V. Vidojkovic, "Radio architectures and circuits towards 5G," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 498–501.
- [3] M. Rahman, M. Elbadry, and R. Harjani, "An IEEE 802.15.6 standard compliant 2.5 nJ/bit multiband WBAN transmitter using phase multiplexing and injection locking," *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1126–1136, May 2015.
- [4] M. Rahman and R. Harjani, "CMOS energy efficient integrated radios for emerging low power standards," in *Proc. Int. SoC Design Conf. (ISOCC)*, Oct. 2016, pp. 151–152.
- [5] IEEE Standard for Local and Metropolitan Area Networks—Part 15.6: Wireless Body Area Networks, IEEE Standard 802.15.6-2012, Feb. 2012.
- [6] Cisco. (2011). Cisco Internet Business Solutions Group White Paper, The Internet of Things. [Online]. Available: https://www.cisco.com
- [7] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1341–1350, Jun. 2008.
- [8] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 275–282, Feb. 2004.
- [9] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "The Blixer, a wideband balun-LNA-I/Q-mixer topology," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2706–2715, Dec. 2008.
- [10] D. Murphy et al., "A blocker-tolerant wideband noise-cancelling receiver with a 2dB noise figure," in *IEEE Int. Solid-State Circuits Conf. (ISSCC)* Dig. Tech. Papers, Feb. 2012, pp. 74–76.
- [11] M. Rahman and R. Harjani, "A 0.7V 194μW 31dB FOM 2.3-2.5 GHz RF frontend for WBAN with mutual noise cancellation using passive coupling," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, May 2015, pp. 175–178.
- [12] M. Rahman and R. Harjani, "A sub-1V 194μW 31-dB FOM 2.3-2.5 GHz mixer-first receiver frontend for WBAN with mutual noise cancellation," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 4, pp. 1102–1109, Apr. 2016.
- [13] M. Rahman and R. Harjani, "A sub-1 V, 2.8db NF, 475μw coupled LNA for Internet of Things employing dual-path noise and nonlinearity cancellation," in *Proc. IEEE RFIC*, Jun. 2017, pp. 236–239.
- [14] J. R. Long, "Monolithic transformers for silicon RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1368–1382, Sep. 2000.
- [15] J. R. Long and M. A. Copeland, "The modeling, characterization, and design of monolithic inductors for silicon RF IC's," *IEEE J. Solid-State Circuits*, vol. 32, no. 3, pp. 357–369, Mar. 1997.

- [16] J. Deguchi, D. Miyashita, and M. Hamada, "A 0.6V 380μW -14 dBm LO-Input 2.4 GHz double-balanced current-reusing single-gate CMOS mixer with cyclic passive combiner," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2009, pp. 224–225.
- [17] F. Zhang, K. Wang, J. Koo, Y. Miyahara, and B. Otis, "A 1.6 mW 300 mV-supply 2.4 GHz receiver with -94 dBm sensitivity for energy-harvesting applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 456–457.
- [18] C.-W. Kim, M.-S. Kang, P.-T. Anh, H.-T. Kim, and S.-G. Lee, "An ultrawideband CMOS low noise amplifier for 3-5-GHz UWB system," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 544–547, Feb. 2005.
- [19] H. H. Hsieh and L. H. Lu, "Design of ultra-low-voltage RF frontends with complementary current-reused architectures," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 7, pp. 1445–1458, Jul. 2007.
- [20] M. A. Abdelghany, R. K. Pokharel, H. Kanaya, and K. Yoshida, "Low-voltage low-power combined LNA-single gate mixer for 5 GHz wireless systems," in *Proc. IEEE RFIC*, Jun. 2011, pp. 1–4.
- [21] H. Lee and S. Mohammadi, "A 500 μW 2.4 GHz CMOS subthreshold mixer for ultra low power applications," in *Proc. IEEE RFIC*, Jun. 2007, pp. 325–328.



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