

An Ultra-High Input Impedance Analog Front End Using Self-Calibrated Positive Feedback

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Abstract—This paper presents circuit techniques for ultra-high input impedance analog front end (AFE). In order to boost input impedance, various on- and off-chip parasitic capacitances are cancelled using an active shield and negative capacitance technique. To maximize the cancellation, a self-calibration scheme with active shield replica is proposed for positive feedback-based negative capacitance, which settles at the boundary between stable and unstable states in calibration mode. A prototype IC fabricated in 0.18- μm CMOS achieves an input impedance of 50 G Ω at 50 Hz, equivalent to 60-fF capacitance, while consuming 289 nW from 0.8-V supply. The proposed AFE is applied to heart-rate monitoring using 1-cm² dry electrodes over clothes without any straps.

Index Terms—Analog front end (AFE), electrocardiography (ECG), non-contact, positive feedback, self-calibration, ultra-high input impedance.

I. INTRODUCTION

WITH the growing interest in wearable health monitoring, bio-signal acquisition integrated circuits (ICs) for ExG have garnered much interest over the past decade [1]–[4]. For wearable ExG sensors, achieving high input impedance is of great importance, as it offers several advantages, such as high common-mode rejection ratio (CMRR), robustness to interference, and resiliency to contact variation. Hence, many prior works have focused on improving the input impedance of the analog front end (AFE) to more than several G Ω s by using techniques, such as active shielding and positive feedback. Unfortunately, these techniques are ultimately limited by on-chip parasitics that cannot be removed due to stability issue. While trimming can be used to maximally cancel the parasitic capacitance, it is undesired in practice due to increased manufacturing cost.

In this paper, we propose an ultra-high input impedance AFE whose parasitic capacitance is cancelled both inside

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and outside the chip [13]. The result is an AFE that has 50-G Ω input impedance at 50 Hz, equivalent to 60-fF input capacitance, while consuming 289 nW when implemented in 0.18- μm CMOS.

The basic methods that we use are active shield [5]–[7] and negative capacitance [10]–[12] by using self-calibration. However, to overcome the limitations of these techniques, we propose a self-calibrated positive feedback (SCPF) that employs active shield replica and stability boundary detection. Although the implementation of the main idea was shown in [13], this paper adds further knowledge and valuable insights in circuits and system design, such as a detailed analysis of the self-calibration scheme and theoretical background on why it is necessary to find stability boundary during calibration. A robust method of correctly determining the stability in the presence of circuit non-ideality is also described. At the circuit level, guidelines on how one should design amplifiers and signal source for the proposed self-calibration are given. Finally, we demonstrate a non-contact electrocardiography (ECG) sensor that uses 1-cm² electrodes over clothes without any chest straps.

This paper is organized as follows. In Section II, impedance boosting techniques and overall system architecture are described. Next, self-calibration scheme of positive feedback is presented in Section III, followed by the detailed implementation of the proposed system in Section IV. Measurement results of the prototype IC, including demonstration of non-contact ECG sensors, are shown in Section V, and conclusions are drawn in Section VI.

II. HIGH INPUT IMPEDANCE ANALOG FRONT END

The input capacitance (C_{IN}) of the AFE can be divided into two components: off-chip external (C_{EXT}) and on-chip internal (C_{INT}) capacitance. To minimize these capacitances, active shield and negative capacitance technique can be used.

A. Active Shield to Remove External Capacitance

The external parasitic capacitance originates from the signal trace outside the chip, from the pin-out of the chip to the electrode. The capacitance depends on how long the trace is and what it is coupled to, and its value typically ranges from few hundreds of fFs to few tens of pFs. As the trace is external, a shield structure can be placed along the printed circuit board (PCB) trace or the cable wire so that the parasitic capacitance is formed between these lines. Since both nodes of this capacitor are accessible, it is possible to use active shield

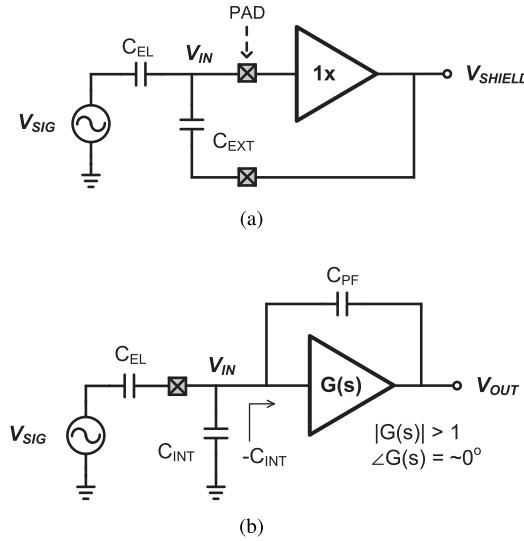


Fig. 1. (a) Active shield to remove external capacitance. (b) Negative capacitance using positive feedback to remove internal capacitance.

technique shown in Fig. 1(a), where a unity gain buffer keeps a constant voltage across the external capacitor [6]–[9]. As the unity gain buffer is not ideal, the capacitance seen from the input node at the pad does not become zero, but becomes $C_{EXT}/(1 + A_{OTA}(s))$, where $A_{OTA}(s)$ is the open-loop gain of the operational transconductance amplifier (OTA) inside the buffer. For example, C_{EXT} of 10 pF is reduced down to 100 fF if A_{OTA} is 40 dB.

Although the active shield technique is effective in reducing the external capacitance, it unfortunately adds parasitic at the input node, since OTA itself has its own input capacitance. As these parasitics cannot be removed by the active shield, it ultimately limits the minimum achievable capacitance. In Section III, we will describe how this capacitance can be removed as well.

Note that the active shield technique can also be applied to reduce some of the on-chip parasitic capacitance [6]. The shield structure can be implemented on-chip using lower metal layers to remove parasitic from the input trace to the substrate or neighboring interconnects. However, it is not possible to remove parasitic capacitance that stems from diode junction or MOSFET gate input, which inevitably exist due to electrostatic-discharge (ESD) and amplifier. Thus, efficacy of the active shield technique in removing internal capacitance is quite limited.

B. Negative Capacitance to Remove Internal Capacitance

Internal parasitic capacitance exists between the input node and other nodes within the IC. It generally consists of parasitic capacitances from ESD, pad, and amplifier input. Note that only one node (the input node) is accessible for these capacitors, since the other node is usually a substrate or a ground. Thus, applying the active shield technique is not possible. Instead, a negative capacitance technique using positive feedback loop can be employed to cancel the capacitance, as shown in Fig. 1(b) [10]–[12]. The amount of negative

capacitance seen at the input of the amplifier is given as $-C_{PF}(G(s) - 1)$, where $G(s)$ is the gain of the amplifier that can be implemented using a feedback amplifier for an accurate gain [10]. Note that $G(s)$ should have a constant magnitude response within the signal bandwidth for a frequency-independent capacitance cancellation. If $G(s)$ has peaking in its magnitude response at a certain frequency, the negative capacitance will be larger at this frequency and may cause system instability. Therefore, $G(s)$ should have a constant magnitude response, i.e., $G(s) = G_0$. Hence, the transfer function from the signal source (V_{SIG}) to the amplifier input (V_{IN}) can be expressed as the following equation:

$$\frac{V_{IN}}{V_{SIG}} = \frac{C_{EL}}{C_{EL} + C_{INT} - C_{PF}(G_0 - 1)} \quad (1)$$

where C_{EL} is the source impedance (or coupling capacitor). Since the goal is to maximize the input impedance, negative capacitance should fully cancel C_{INT} , and thus

$$C_{INT} = (G_0 - 1)C_{PF}. \quad (2)$$

Note that the magnitude of (1) can be larger than 1 by having larger negative capacitance. In such a case, however, gain is unpredictable, as C_{EL} is unknown and can vary. More importantly, it may cause instability when C_{EL} is small as described in the Appendix. Thus, the negative capacitance technique used in previous works [11], [12] was far from satisfying (2). In this paper, a self-calibration technique is proposed in order to satisfy (2). Once proper C_{PF} is found through calibration, a high input impedance AFE can be obtained. It should be noted that the proposed calibration scheme is not affected by changes in external or electrode capacitance, as can be seen in (2), where C_{EXT} or C_{EL} is not the part of the equation.

C. Proposed Self-Calibrated Analog Front End

The overall architecture of the proposed ultra-high input impedance AFE is shown in Fig. 2. It consists of four blocks: active shield, two stages of amplification, SCPF, and 11-bit successive approximation analog-to-digital converter (SAR ADC). The SCPF consists of a calibration signal generator, active shield replica, calibration logic, and programmable positive feedback capacitor bank (C_{PF}).

The AFE has two modes of operation: signal acquisition mode and calibration mode. In the signal acquisition mode, CAL_{EN} is low, and the calibration signal generator and calibration logic are turned off. The input first goes through an active shield that reduces external capacitance. Next, it is passed on to a fixed gain amplifier (FGA) and a programmable gain amplifier (PGA). The FGA has a positive feedback capacitor (C_{PF}) that is programmed during calibration mode to cancel the internal parasitic capacitance. The output of the PGA is then quantized by the SAR ADC.

During the calibration mode, CAL_{EN} is high, and the calibration signal generator and logic are turned on. Calibration signal is applied to an FGA through ac-coupling capacitor C_3 , and the FGA is disconnected from the active shield and the PGA. Instead, it is connected to an active shield replica for an

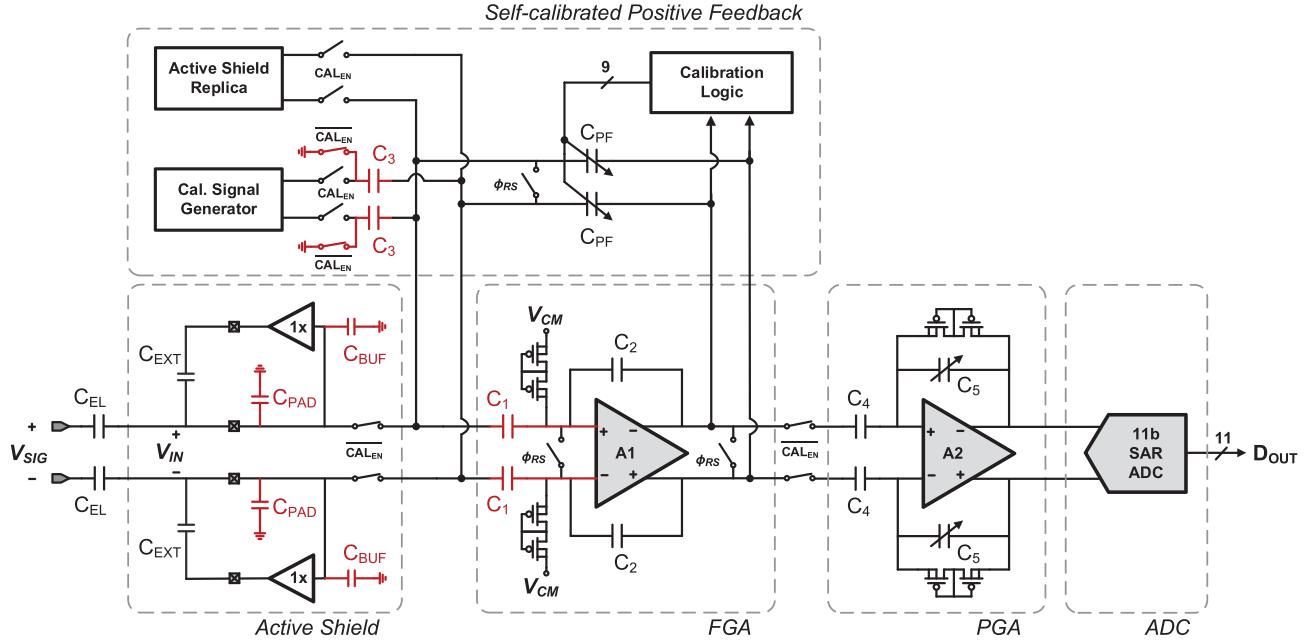


Fig. 2. Overall system architecture of the proposed ultra-high input impedance AFE.

accurate modeling of the internal parasitics during acquisition mode, as will be described in detail in Section III. Note that C_3 is grounded during the acquisition mode, since C_3 should be considered as part of the internal capacitance.

D. Noise Analysis

For the noise analysis of the proposed AFE, an equivalent noise model is established, as shown in Fig. 3. Note that the noise from the PGA is negligible, as the FGA provides enough gain. The input referred noise of the AFE $\overline{V_{ni,AFE}^2}$ can be represented as a sum of the noise from the FGA $\overline{V_{ni,FGA}^2}$ and active shield $\overline{V_{ni,BUF}^2}$, respectively

$$\overline{V_{ni,AFE}^2} = \overline{V_{ni,FGA}^2} \left(1 + \frac{C_{PF}}{C_{EL}} + \frac{C_{INT}}{C_{EL}} + \frac{C_{EXT}}{C_{EL}} \right)^2 + \overline{V_{ni,BUF}^2} \left(\frac{C_{EXT}}{C_{EL}} \right)^2. \quad (3)$$

Noise in the FGA is from V_{CM} generator for input common-mode voltage ($\overline{V_{n,CM}^2}$), pseudo-resistor for input bias ($\overline{V_{n,RCM}^2}$), and input referred noise from A1 ($\overline{V_{ni,A1}^2}$). The detailed expression of input referred noise of the FGA can be expressed as

$$\overline{V_{ni,FGA}^2} = \overline{V_{ni,A1}^2} \left(1 + \frac{C_2}{C_1} \right)^2 + \left(\overline{V_{n,RCM}^2} + \overline{V_{n,CM}^2} \right) \left(\frac{1}{sR_{CM}C_1} \right)^2. \quad (4)$$

From (3), it can be seen that the overall noise of AFE highly depends on the coupling capacitor from electrode (C_{EL}). When using a non-contact electrode, C_{EL} is very small (e.g., 1 pF), and integrated noise becomes large. Hence, acquired

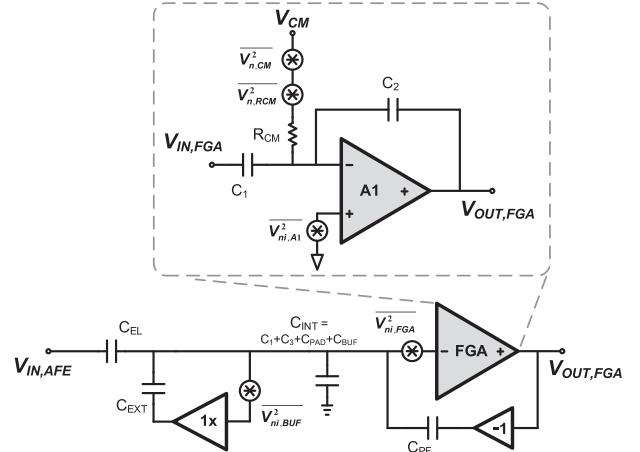


Fig. 3. Equivalent noise model of the proposed AFE.

signal quality is expected to be poorer than that using wet electrode or dry electrode with firm contact.

It should also be noted that the input referred noise is increased by about the ratio of the overall input capacitance (C_{IN}) to coupling capacitor (C_{EL}), which is the reciprocal value of attenuation factor when all the techniques are not used. This implies that signal-to-noise ratio is not improved by the proposed technique.

III. POSITIVE FEEDBACK CALIBRATION

A. Calibration Mode Architecture

The detailed schematic of the AFE in self-calibration mode is shown in Fig. 4. The active shield replica consists of dummy pads and dummy shield buffers. The calibration signal generator provides a differential test signal (V_{CAL}) via coupling capacitor C_3 . The calibration logic monitors the output

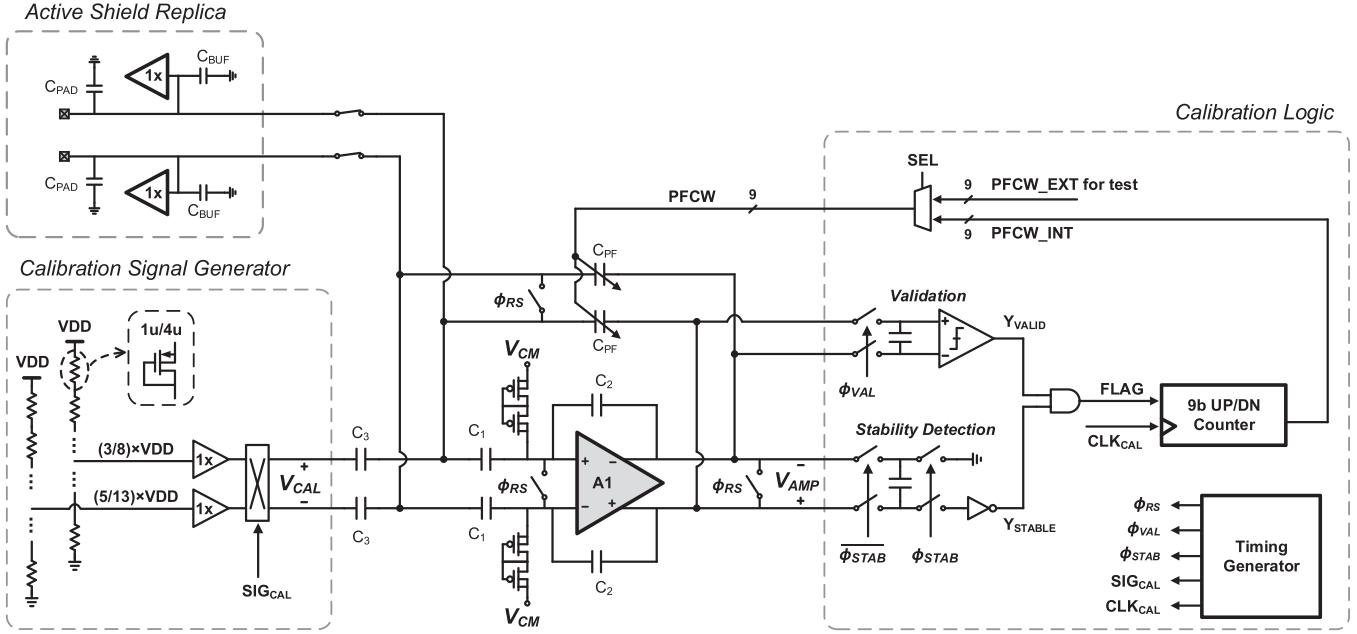


Fig. 4. Schematic of the core circuits during self-calibration.

of the FGA and updates the positive feedback control word (PFCW) so that the internal parasitic capacitance is maximally cancelled.

B. Cancelling the Internal Capacitance by Finding Stability Boundary

First, it should be noted that impedance must be maximized for signal acquisition mode, not for calibration mode. The transfer function of Fig. 2 (acquisition mode) can be written as (1), where $C_{INT} = C_{PAD} + C_{BUF} + C_1 + C_3$. One end of C_3 is grounded during acquisition mode. By including C_3 , internal capacitance in acquisition and calibration is the same. As was described in (2), C_{PF} must have the following value to cancel C_{INT} :

$$C_{PF} = C_{INT}/(G_0 - 1). \quad (5)$$

To see how this condition translates to in calibration mode, the transfer function during calibration mode shown in Fig. 4 can be expressed as follows:

$$\frac{V_{AMP}}{V_{CAL}} = \frac{G_0 \cdot C_3}{C_{PAD} + C_{BUF} + C_1 + C_3 - (G_0 - 1)C_{PF}} = \frac{G_0 \cdot C_3}{C_{INT} - (G_0 - 1)C_{PF}}. \quad (6)$$

It can be seen that (5) results in a denominator of zero in (6), an unstable state where poles are located on the imaginary axis. Therefore, in order to fully cancel the internal capacitance in acquisition mode, we must find the stability boundary in calibration mode, at which it becomes unstable. It should be noted that the system will be stable in acquisition mode even if the system is unstable during calibration mode, as their system transfer functions are different.

Note that in prior works, it is difficult to satisfy (5). In [11], [12], and [18], C_{PF} is set equal to C_2 so that only C_1 is

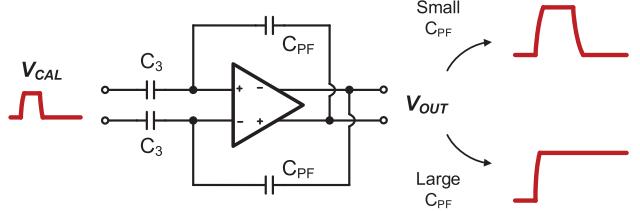


Fig. 5. Transient response for pulse input during calibration mode.

cancelled. In [10], C_{PF} is made programmable but must be trimmed manually. Such is not only cumbersome, but it is also difficult to satisfy (5) from external measurements.

To find the stability boundary in calibration mode, we observe how the AFE behaves to a small-signal pulse input (V_{CAL}) for different C_{PF} values, as shown in Fig. 5. When C_{PF} is small, there is a weak positive feedback, and thus, the AFE is stable. It operates as an amplifier with a gain given by (6). On the other hand, when C_{PF} is too large, the AFE behaves as a latch due to the strong regeneration from the positive feedback, as shown in Fig. 5. Therefore, stability can be determined by looking at the output at the end of an input pulse.

A detailed timing diagram of the AFE during calibration mode is shown in Fig. 6. When the reset clock ϕ_{RS} is low, V_{CAL} is applied to the amplifier, which goes up by 7 mV and down by 7 mV. The output is sampled just before ϕ_{RS} goes high and fed to the comparator to determine the stability. Although there are two states in theory (stable and unstable), the amplifier behaves a bit differently within each state depending on the strength of positive feedback. When C_{PF} is small such that the system is far from stability boundary, the amplifier has a small gain, and we refer to this state as "strictly stable." When C_{PF} is increased so that the system is closer to the boundary but still maintains stability, the amplifier

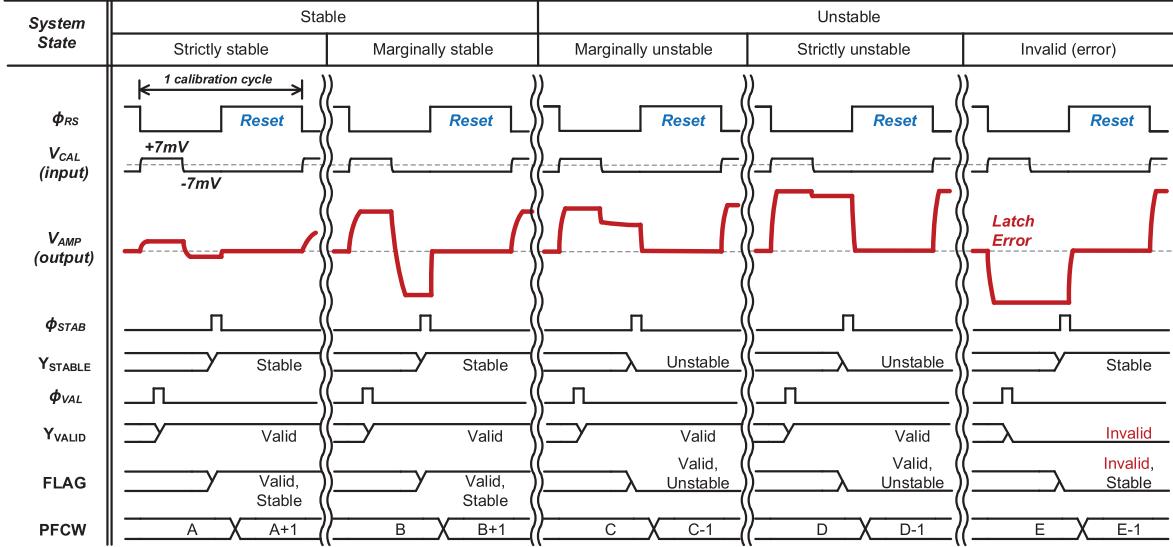


Fig. 6. Timing diagram of the calibration mode. There are five possible responses depending on the positive feedback strength.

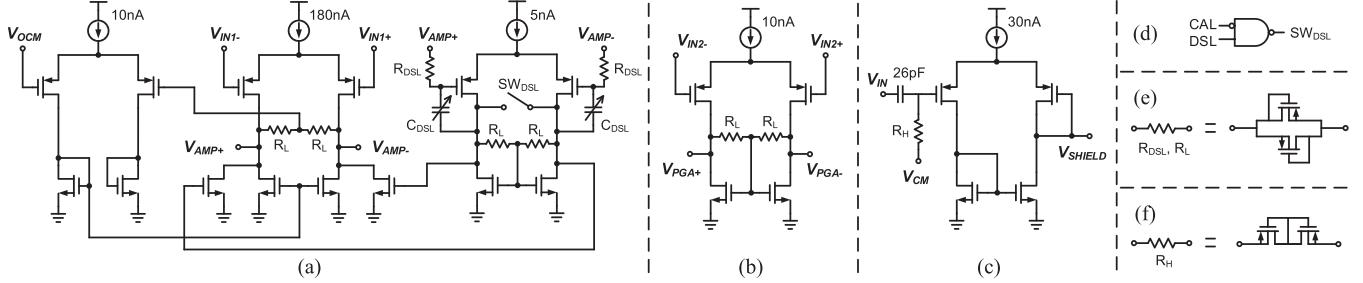


Fig. 7. Schematic of (a) OTA of FGA (A1), (b) OTA of PGA (A2), (c) active shield buffer, (d) control switch in DSL, (e) low-resistive pseudo-resistor, and (f) high-resistive pseudo-resistor.

gain becomes larger and exhibits rail-to-rail swing. We refer to this state as “marginally stable.”

In a similar manner, unstable state can also be classified into two sub-states. A “strictly unstable” state is when the positive feedback is too strong, and thus, the system behaves as a strong latch. A “marginally unstable” state is when the positive feedback is close to the stability boundary and the system works as a latch but in a weak manner. Within this weak latch region, the amplifier output does not reach the supply voltage and comes down slightly when the input signal goes low.

In our proposed AFE, an inverter-based comparator is used to check the system stability, as shown in Fig. 4. The differential output of the amplifier is converted to a single-ended signal by a switched capacitor and then fed to an inverter, which uses its own threshold to make the decision. A low output means that the system is stable and a high means unstable.

To guarantee that the proposed stability check is correct, there is one more validation that must be performed. As ϕ_{RS} goes low, the amplifier output may immediately start to move to the negative rail regardless of stability due to an ill-defined input or offset. Although such output will not cause error when the amplifier is in a stable state, it will lead to an error in an unstable state, as shown in Fig. 6. To avoid such an

error, the invalid decision is corrected by a validator circuit that samples the output just after V_{CAL} is applied and detects its sign. When the voltage sampled by the validator is low, the system is determined as unstable regardless of the stability detector output.

Based on the detected system state, a 9-bit PFCW is changed so that positive feedback becomes stronger when the system is stable and weaker when it is unstable. Hence, the system settles at the boundary between stable and unstable states, where the condition given in (2) is satisfied. The calibration process runs for 512 cycles so that all possible codes of the capacitor bank can be covered. When the calibration is finished, the PFCW is adjusted by 5 LSBs toward more stable state to have some margin, so that the system is stable under supply or temperature variations.

IV. IMPLEMENTATION

A. Amplifiers

The amplification stage is composed of two capacitive feedback amplifiers, FGA and PGA, as shown in Fig. 2. The FGA has a fixed gain of 20 set by $C_1/C_2 = 3.4 \text{ pF}/170 \text{ fF}$. The gain of the PGA is controlled externally and can be set to 1, 3, 6, or 20 by changing the negative feedback capacitance C_5 . The transistor-level schematics of OTAs used in FGA and PGA are shown in Fig. 7(a) and (b), respectively.

The OTA of FGA (A1) is composed of three parts: core amplifier, common-mode feedback (CMFB), and dc servo-loop (DSL). For the core amplifier, a simple single-stage amplifier is employed instead of a two-stage amplifier. As discussed in Section II-B, the amplifier should have constant magnitude. As it is easier and more power efficient to obtain constant magnitude response from a single-stage amplifier than a two-stage amplifier, A1 is implemented using a single-stage architecture.

DSL is employed to additionally attenuate the output offset caused by mismatch in input transistors and resistors. R_{DSL} is implemented using a pseudo-resistor, which has about 125 G Ω . C_{DSL} is a programmable capacitor bank whose value can be selected among 650 fF, 1.3 pF, 2.6 pF, and 5.3 pF, where the default value is 2.6 pF.

The DSL is turned off during calibration. This is to avoid conflict, since when the AFE is unstable, DSL will try to bias the amplifier to come out of the unstable state. Thus, FGA will be incorrectly biased in the stable state. The DSL is turned off by simply shorting its outputs as shown in Fig. 7(a) and (d), so that the common-mode output is fed to the core amplifier.

The OTA of the PGA (A2) is shown in Fig. 7(b). It maximizes the output swing for the subsequent ADC. CMFB is provided by resistors. The input common mode is the same as the output due to the feedback resistors, as shown in Fig. 2. All resistors for OTA output common-mode sensing are implemented using symmetric pseudo-resistor pair as shown in Fig. 7(e) so that they have the same resistance from either side.

Note that the proposed work does not have chopper stabilization and is susceptible to $1/f$ noise [14]–[16]. However, it is important to discern R peaks and R-R interval rather than distinguishing the whole PQRST waveform for wearable heart-rate monitoring. Moreover, it is mostly the large common-mode signals that are more problematic than the $1/f$ noise in practical scenarios.

Active shield buffer employs single-stage OTA structure, and its schematic is shown in Fig 7(c). Input of active shield is ac-coupled by a capacitor and a pseudo-resistor to make its dc bias at 300 mV. Note that shield buffer is a single-pole system (basic single-stage differential amplifier), and it is stable regardless of C_{EL} or C_{EXT} .

B. Self-Calibrated Positive Feedback

The SCPF is composed of calibration signal generator, active shield replica, positive feedback capacitor bank, and calibration logic, as shown in Fig. 4. The calibration signal generator produces V_{CAL} by alternating two dc voltage levels that are close together. The amplitude of V_{CAL} is determined by considering noise, offset, and amplifier gain. The minimum amplitude should be larger than the thermal noise and offset voltage. Given an input referred noise of about 10 μ V and a comparator offset of about 10 mV, which are extracted from simulation and a minimum gain of 3 by setting $C_3 = 1.7$ pF, $C_{INT} = 5$ pF, and $G_0 = 20$ in (6), at least 4 mV is required for a reliable comparator decision. In the proposed design, the pulse amplitude is set to about 7 mV.

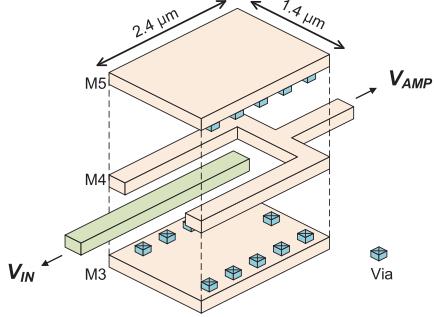


Fig. 8. Layout of the unit capacitor of C_{PPF} .

An obvious way to implement dc levels of small difference is to use a series of many resistors. For example, in order to generate 7-mV difference from 0.8-V supply, 110 resistors can be used. Unfortunately, such implementation requires large area especially when the resistor is a power saving pseudo-resistor that has its own separate n-well. To reduce the area, we propose using two small resistor ladders where the number of resistors in each ladder is different and relatively coprime, such as 13 and 8. By taking the fifth and third points of the respective ladder, the voltage difference becomes 7 mV (i.e., $5/13 - 3/8 = 1/104$). This voltage difference is turned into a differential pulse signal (V_{CAL}) by using buffers and switches and applied to the AFE through ac-coupling capacitor C_3 .

C_{PPF} is composed of a fixed capacitor of 170 fF and a 9-bit capacitor bank of 256 fF. The fixed capacitance compensates for the capacitance (C_1) looking into FGA, and the programmable capacitor bank compensates for the remaining internal capacitance, such as C_{PAD} , C_{BUF} , and C_3 . C_{PPF} is laid out to minimize the parasitic capacitance as shown in Fig. 8, where it can be seen that V_{IN} is surrounded by V_{AMP} like a coaxial cable [17]. Thus, there is little parasitic between V_{IN} and other nodes. The unit capacitor is designed to have a small capacitance of 0.5 fF, since it is multiplied by the closed-loop gain G_0 . G_0 is set to 20 in this design, and thus, the negative capacitance by the unit capacitor is about -10 fF. This makes it possible to cover internal parasitic from 0 to 5.12 pF using the capacitor bank.

C. SAR ADC

The ADC is an 11-bit synchronous SAR ADC with a sampling frequency of 1 kHz. Unit capacitor of the DAC is 2 fF, and the total capacitance is 4 pF. Comparator is composed of a pre-amplifier and a latch. The pre-amplifier is biased to draw 30 nA from 0.8-V supply.

V. MEASUREMENT RESULTS

The proposed AFE is implemented in 0.18- μ m CMOS, and its die size is 1200 μ m \times 1600 μ m, as shown in Fig. 9. The AFE draws 320 nA from 0.8 V, and the detailed breakdown of power consumption is shown in Fig. 10. Note that the power consumed by the calibration block is 68 nW, but it is turned off during acquisition mode and thus not included in Fig. 10.

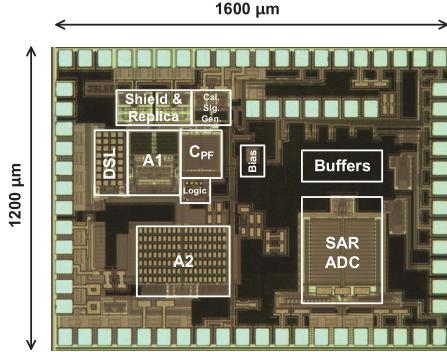


Fig. 9. Die photograph.

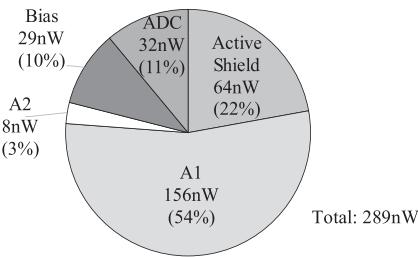


Fig. 10. Measured AFE power breakdown.

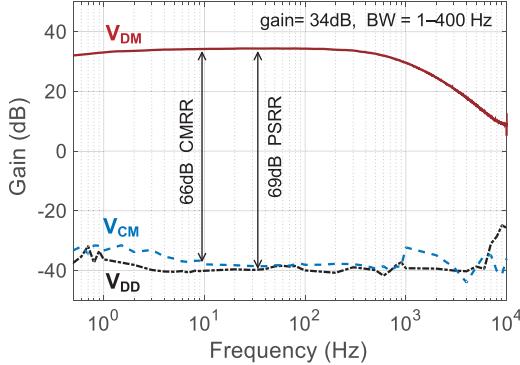


Fig. 11. Measured magnitude response of the AFE.

A. General AFE Characteristic

The magnitude response of the AFE is shown in Fig. 11. The measured differential gain is 34 dB where the gain of FGA and PGA is 26 and 8 dB, respectively. Signal bandwidth is measured as 400 Hz. CMRR and PSRR are measured as 66 and 69 dB, respectively, which is comparable to those of recent state-of-the-art sub- μ W low-power biosignal AFEs [11], [18]. Input referred noise power spectral density for firm contact ($C_{EL} = 1 \mu\text{F}$) and non-contact ($C_{EL} = 1 \text{ pF}$) is shown in Fig. 12. The integrated noise over the signal bandwidth is $8.26 \mu\text{V}_{\text{rms}}$ and $118.42 \mu\text{V}_{\text{rms}}$, respectively. The thermal noise floor above 100 Hz is $140 \text{ nV}/\text{Hz}^{1/2}$, resulting in a noise efficiency factor of 8.43. The measured performance of SAR ADC is shown in Fig. 13, which has 10 effective number of bits (ENOB) at Nyquist input.

In Fig. 12, $1/f^2$ noise is clearly seen, which is expected from (4). This $1/f^2$ noise is dominated by the pseudo-resistor,

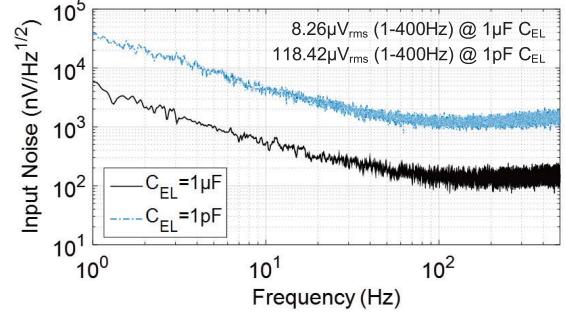


Fig. 12. Measured input referred noise power spectral density.

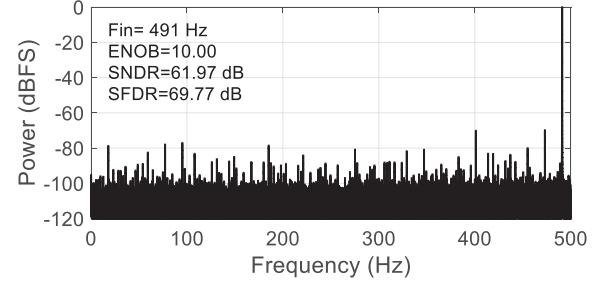
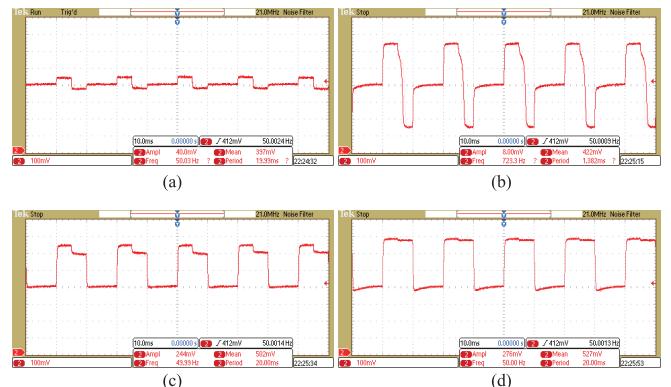
Fig. 13. Measured 2^{16} -point FFT of SAR ADC output.

Fig. 14. Measured FGA output during the calibration mode for four different cases. (a) Strictly stable. (b) Marginally stable. (c) Marginally unstable. (d) Strictly unstable.

since noise from V_{CM} generator is negligible due to the large decoupling capacitor. Although the AFE has relatively high integrated noise, this can be improved by enlarging the capacitor C_1 , so $1/f^2$ noise is further suppressed. Moreover, instrumentation amplifier topology or non-inverting active electrodes can be employed for FGA, as it removes C_1 from the input node and reduces the internal capacitance.

B. Input Impedance

The transient response of the AFE in calibration mode is shown in Figs. 14 and 15. First, PFCW was controlled externally to observe the four different responses explained earlier: 1) strictly stable; 2) marginally stable; 3) marginally unstable; and 4) strictly unstable. The measured results match our expected behavior, as shown in Fig. 14; the AFE acts as an amplifier in stable region shown in Fig. 14(a) and (b) and

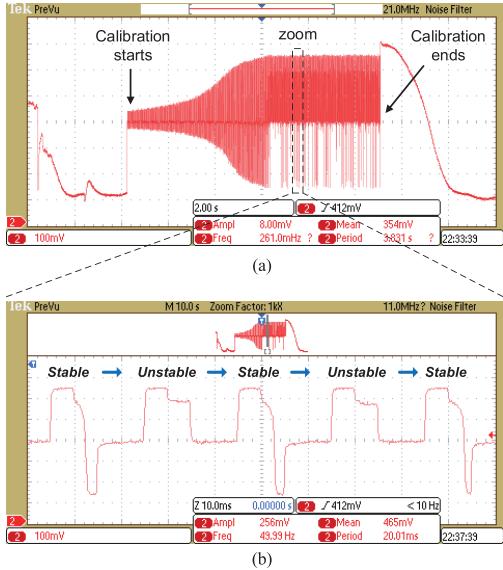


Fig. 15. Measured FGA output during the calibration mode. (a) Entire self-calibration process. (b) Zoomed transient response when the self-calibration is settled.

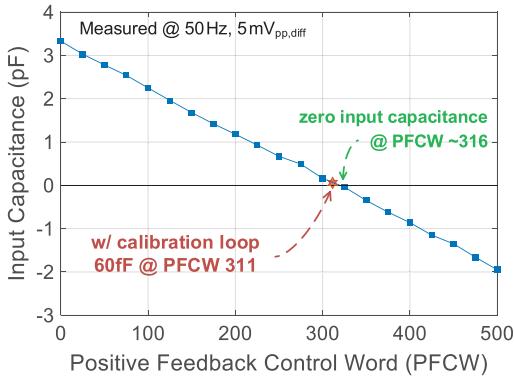


Fig. 16. Measured input capacitance against PFCW.

as a latch in unstable region shown in Fig. 14(c) and (d). Next, PFCW was controlled automatically using self-calibration, and the output is shown in Fig. 15(a). The amplitude gradually increases as the PFCW is updated. A magnified transient response during settling is also shown in Fig. 15(b), where it can be seen that the PFCW alternates between stable and unstable state, which is when the input impedance is maximized.

The measured input capacitance versus PFCW is shown in Fig. 16 when $5 \text{ mV}_{\text{pp,diff}}$, 50-Hz input signal is applied. When PFCW is zero, which is equivalent to the conventional technique of having $C_{\text{PF}} = C_2$ [11], [12], [18], the input capacitance is measured to be about 3.3 pF. The input capacitance decreases as PFCW increases and is almost removed when PFCW is 316. In the proposed scheme, the PFCW backs up by five codes and thus is set to 311, and the proposed AFE achieves 60 fF of input capacitance. The measured input impedance compared with the conventional technique is shown in Fig. 17. Without any technique, the input impedance was measured as $0.5 \text{ G}\Omega$ at 50 Hz. With the conventional positive feedback technique ($C_{\text{PF}} = C_2$), the impedance is increased to $1 \text{ G}\Omega$. The proposed AFE achieves 50 times higher impedance

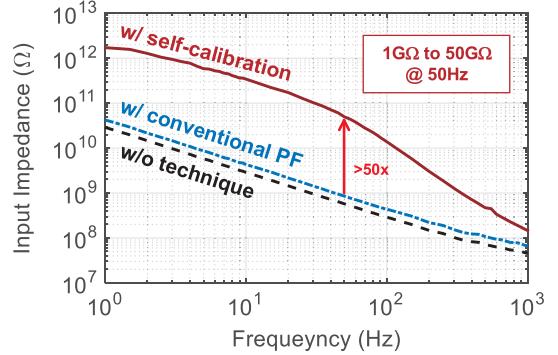


Fig. 17. Measured input impedance over frequency.

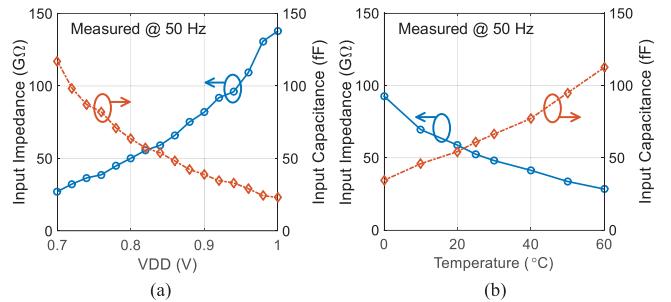


Fig. 18. Input impedance and input capacitance variation under supply and temperature variation.

of $50 \text{ G}\Omega$ compared with the conventional technique. This is because the self-calibration cancels all the internal parasitics while the conventional technique cancels only C_1 . It can also be seen that impedance boosting rolls off near 1 and 100 Hz. This frequency range is considered as an effective impedance boosting range, and the closed-loop gain of FGA is almost constant over this frequency.

Since foreground calibration technique can be susceptible to variation in the surrounding environment, the robustness of the proposed AFE is checked against supply and temperature variations, as shown in Fig. 18. The application of the proposed AFE is a wearable sensor, and thus, the temperature range of $0\text{--}50^\circ\text{C}$ is applied. Calibration is first done at 0.8-V supply and room temperature condition, and then, environmental change is applied. As can be seen, even against $0.7\text{--}1.0\text{-V}$ supply and $0\text{--}50^\circ\text{C}$ temperature change, input capacitance changes only about -30 to $+50 \text{ fF}$ ($+90$ to $-20 \text{ G}\Omega$) and $+40$ to -20 fF (-20 to $+30 \text{ G}\Omega$), respectively, and the proposed AFE is stable and achieves high input impedance. The change in input impedance is due to the change in open-loop gain of the active shield and FGA, as they affect the input impedance as explained in Sections II and IV.

The performance of the proposed AFE is summarized and compared with other high input impedance AFEs in Table II. It can be seen that most of the previous works are focused on canceling just one of the external or internal parasitics. It is important to note that none of the previous works can remove all the internal parasitic capacitances from pad, ESD, and amplifier inputs. Although [6] achieves similar capacitance as ours, its capacitance will be higher in practical IC design where a large ESD capacitance is unavoidable.

TABLE I
PERFORMANCE COMPARISON

	[6] JETCAS 11	[9] VLSI 16	[10] TBIOSAS 11	[12] ISSCC 16	[11] ISSCC 15	[13] JSSC 15	This Work
Process	0.5μm	0.18μm	0.18μm	40nm	65nm	65nm	0.18μm
VDD	3.3V	1.8V	1.2V	1.2V	0.6V	0.6V	0.8V
Current/Ch	4.8 μA ^a	60 μA ^a	11 μA ^a	1.67 μA ^a	5 nA	31 nA	361 nA
CMRR	N/A	108 dB	82 dB	N/A	60 dB	55 dB	66 dB
PSRR	N/A	N/A	N/A	N/A	63 dB	67 dB	69 dB
Input-Referred Noise	200nV/√Hz @1Hz 45nV/√Hz @1kHz	0.67 μV _{rms} (0.5-100Hz)	0.8 μV _{rms} (0.5-100Hz)	2 μV _{rms} (0.5-200Hz)	26 μV _{rms} (1.5-370Hz)	6.52 μV _{rms} (0.1-250Hz)	8.26 μV_{rms} (1-400Hz)
NEF	N/A	28.2 ^b	12.3	7	2.1 ^c	2.64 ^c	8.43^c
Input Impedance	~250GΩ @ 1Hz ~50GΩ @ 60Hz	~18GΩ @ 1Hz 6.7GΩ @ 50Hz	~2GΩ @ 1Hz ~150MΩ @ 50Hz	~300MΩ @ 0.1Hz ~200MΩ @ 10Hz	>2GΩ	>110MΩ	200GΩ @ 1Hz 50GΩ @ 50Hz
Equivalent Input Capacitance	0.06 pF	0.47 pF	21 pF	80 pF	~1.6 pF ^d	~28.9 pF ^d	0.06 pF
Impedance Boosting Techniques	Active shield	Active shield	Manually trimmed negative cap.	Pre-charging, Fixed negative cap. ($C_{PF} = C_2$)	Fixed negative cap. ($C_{PF} = C_2$)	Fixed negative cap. ($C_{PF} = C_2$)	Active shield, Self-calibrated negative cap.

^a 2 channels are required for signal recording

^b calculated from reported information

^c considered power consumption of core circuit, excluded bias circuit and ADC

^d calculated from $1/(2\pi f_m \cdot Z_m)$, where f_m is 50Hz if f_m is not specified

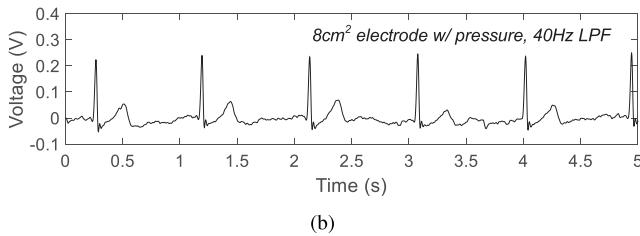
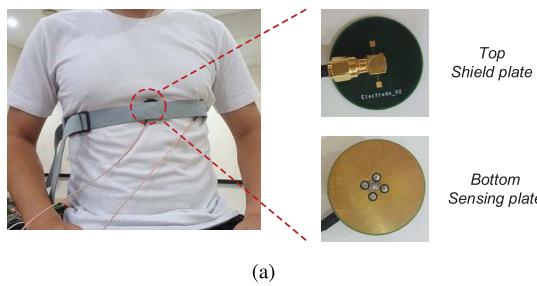


Fig. 19. ECG measurement with custom non-contact electrodes and the AFE.
(a) Measurement setup (b) Measured ECG.

C. Demonstration of Non-Contact ECG Sensor

To test the proposed AFE in a practical setting, we employed the AFE in a non-contact ECG recording. The ECG was recorded using two custom electrodes shown in Fig. 19(a). Two circular electrodes having 8 cm^2 of area were put on a T-shirt above the chest and were pressed with a strap to increase the electrode coupling capacitance (C_{EL}). The recorded ECG is shown in Fig. 19(b), where the output of the AFE was low-pass filtered with 40-Hz cutoff frequency.

To see whether the proposed AFE could be adopted to a miniaturized non-contact ECG sensor, two 1-cm^2 electrodes were implemented on a flexible PCB, as shown in Fig. 20(a). The strap used in Fig. 19(a) is removed, and vest used in

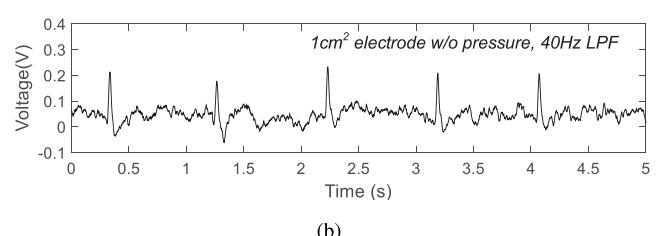
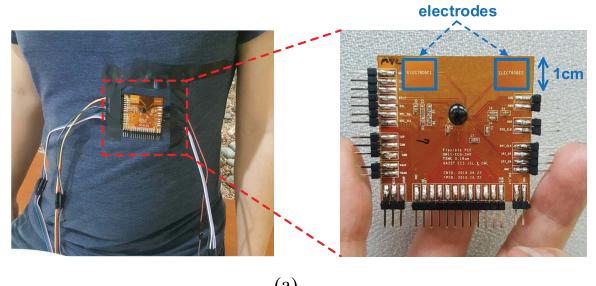


Fig. 20. ECG measurement with a miniaturized non-contact complete system.
(a) Measurement setup (b) Measured ECG after ADC.

prior works [5], [19] is not used. Such results in a larger gap between the body and the electrode and decreases C_{EL} , which increases signal attenuation and the noise as seen in (3). Thus, the ECG quality in Fig. 20(b) is worse than that in Fig. 19(b). Yet, it can be seen from Fig. 20(b) that the ECG can be recorded, despite the small electrode area and relatively large separation between the skin, clothes, and electrodes. It should be noted that in real ECG measurement, the two coupling capacitors (C_{EL}) cannot be equal and have inevitable mismatch. Even with mismatch in C_{EL} , we were able to obtain ECG, as shown in Figs. 19 and 20.

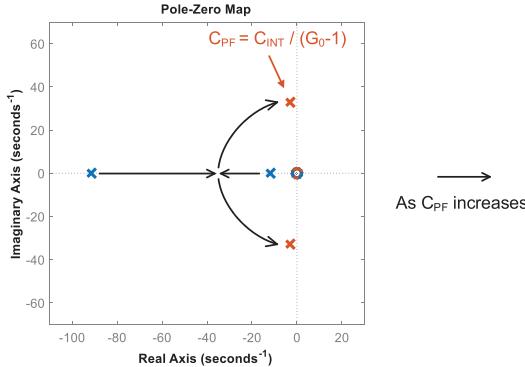


Fig. 21. Simulated pole-zero plot for the system during acquisition mode when $C_{EL} = 10 \text{ fF}$, $C_{INT} = 5 \text{ pF}$, and $G_0 = 20$.

VI. CONCLUSION AND FUTURE WORK

We have presented an ultra-high input impedance AFE using positive feedback self-calibration. By finding the stability boundary in calibration mode, parasitic capacitance during signal acquisition could be fully cancelled. The proposed AFE with SCPF and active shield achieves 50 GΩ of input impedance below 50 Hz, which is equivalent to an input capacitance of 60 fF.

While the proposed technique achieves ultra-high input impedance, there is a room for improvement. First, changing the calibration scheme from foreground to background will give higher impedance against supply and temperature variations. It will also provide better stability against environmental change. Second, changing differential topology to active electrodes will provide better performance and is more suitable for the proposed technique.

APPENDIX

The transfer function of the first-stage amplifier $G(s)$ has a bandpass response that can be expressed as follows:

$$G(s) = G_0 \cdot \frac{2\zeta_0\omega_n s}{s^2 + 2\zeta_0\omega_n s + \omega_n^2} \quad (7)$$

where ω_n is the natural frequency, ζ_0 is the damping ratio, and G_0 is the midband gain of the amplifier. Then, the transfer function during signal acquisition mode shown in Fig. 1(b) becomes

$$\begin{aligned} \frac{V_{OUT}(s)}{V_{SIG}(s)} &= \frac{C_{EL}}{C_{EL} + C_{INT} - C_{PF}(G(s) - 1)} G(s) \\ &= \frac{G_0 \cdot C_{EL}}{C_{EL} + C_{INT} + C_{PF}} \\ &\cdot \frac{2\zeta_0\omega_n s}{s^2 + \frac{C_{EL} + C_{INT} - (G_0 - 1)C_{PF}}{C_{EL} + C_{INT} + C_{PF}} 2\zeta_0\omega_n s + \omega_n^2} \\ &= A' \cdot \frac{2\zeta_0\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2}. \end{aligned} \quad (8)$$

Hence, the system is stable if the following condition is met:

$$C_{EL} + C_{INT} > (G_0 - 1)C_{PF}. \quad (9)$$

TABLE II
PFCW ADJUSTMENT

Adjustment after self-calibration	ζ when $C_{EL}=1 \text{ pF}$	ζ when $C_{EL}=250 \text{ fF}$
0 LSB	1.99	0.39
2 LSB	2.12	0.44
5 LSB	2.13	0.50
10 LSB	2.32	0.60

Note that the calibration scheme ensures $C_{INT} = (G_0 - 1) \cdot C_{PF}$, and therefore, this stability condition is always satisfied after calibration. It should be noted that although the proposed AFE is always stable, its damping ratio (ζ) is affected by C_{EL} . That is, as C_{EL} becomes smaller, ζ gets smaller. To see the damping ratio that is affected by C_{EL} , we considered an extreme case where C_{EL} is very small ($C_{EL} = 10 \text{ fF}$).

A simulated pole-zero plot of the above-mentioned system is shown in Fig. 21, where $C_{EL} = 10 \text{ fF}$, $C_{INT} = 5 \text{ pF}$, and $G_0 = 20$. Two poles of the system are on the real axis when C_{PF} is zero, and gradually move toward imaginary axis as C_{PF} increases. When the optimal condition given in (2) is met, two poles are close to the imaginary axis. However, they are still on the left-half-plane, and the system is stable.

In the proposed calibration scheme, PFCW is adjusted by 5 LSBs as explained in Section III. The PFCW adjustment after calibration helps to provide larger ζ when C_{EL} is small as shown in Table II.

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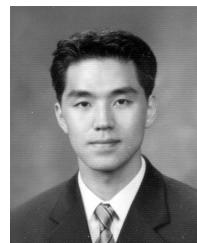
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