

# A Hysteretic Buck Converter With 92.1% Maximum Efficiency Designed for Ultra-Low Power and Fast Wake-Up SoC Applications

Francesco Santoro<sup>ID</sup>, Member, IEEE, Rüdiger Kuhn, Neil Gibson, Nicola Rasera, Thomas Tost, Helmut Graeb, Fellow, IEEE, Bernhard Wicht, Senior Member, IEEE, and Ralf Brederlow, Senior Member, IEEE

**Abstract**—This paper presents a dc–dc converter for integration in the power management unit of an ultra-low power microcontroller. The converter is designed to significantly reduce the wake-up energy and startup delay of the supplied core. The use of a minimized output capacitor is the key factor to save the wake-up energy. The converter is buffered with only 56 nF and guarantees a stable output of 1.2 V with a voltage ripple smaller than 30 mV. The controller of the proposed dc–dc converter is based on a predictive peak current control that allows the system to control the energy transfer at extremely low power consumption. The proposed circuit is implemented in 130-nm CMOS technology with an area of only 0.14 mm<sup>2</sup>. It achieves a high conversion efficiency of 92.1% and a small quiescent current of 440 nA. It operates from 1.8 to 3.3 V with a maximum load of 2.65 mA.

**Index Terms**—Buck, dc–dc, fast wake-up, low energy, low power, minimized capacitor, wake-up energy.

## I. INTRODUCTION

**S**MART devices are widely present in our daily life, e.g., healthcare, safety, entertainment, home automation, and so on [1]. The smarter these devices grow the more power they require. Nevertheless, many of them have to be portable devices not connected to the powerline (e.g., smoke detectors and alarms). They fall in the *ultra-low power* (ULP) category and are supplied by a limited energy source (e.g., battery, super capacitors, harvesters, and so on). Fig. 1 shows a simplified block diagram of a generic smart device. Even rather simple

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F. Santoro was with the Department of Electronics, Technical University of Munich, 80333 Munich, Germany, and also with Texas Instruments Deutschland GmbH, 85356 Freising, Germany. He is now with Infineon Technologies Austria AG, Villach 9500, Austria (e-mail: francesco.santoro@tum.de).

R. Kuhn, N. Gibson, N. Rasera, T. Tost, and R. Brederlow are with Texas Instruments Deutschland GmbH, 85356 Freising, Germany (e-mail: r.kuhn@ti.com; neil@ti.com; nicolarasera@gmail.com; t-tost@ti.com; r-brederlow@ti.com).

H. Graeb is with the Department of Electronic Design Automation, Technical University of Munich, 80333 Munich, Germany (e-mail: graeb@tum.de).

B. Wicht is with the Leibniz Universität Hannover, 30167 Hannover, Germany, and also with the Robert Bosch Center for Power Electronics, Reutlingen University, 72762 Reutlingen, Germany (e-mail: bernhard.wicht@ims.uni-hannover.de).

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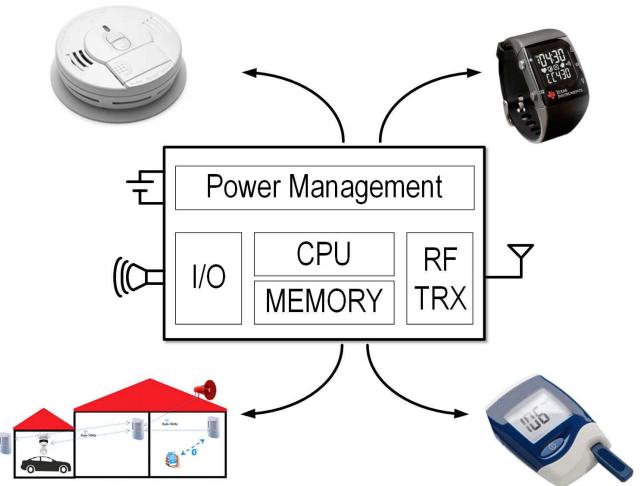


Fig. 1. Simplified block diagram and examples of an ULP application.

smart devices very often embed power-hungry electronic subsystems [2], e.g., sensors, actuators, wireless communication systems, and micro controller units (MCUs) [3], [4]. The energy consumption of MCUs is very often dominant in the energy budget of the overall system. Efficient MCUs are therefore key to make the aforementioned smart devices convenient and profitable. Embedded *power management units* (PMUs) are responsible to manage the energy transfer in an MCU from the external source to the internal circuitry. They play a fundamental role to reduce the energy consumption of the MCU in all operational modes, and as a result prolong the battery lifetime. In general, every *ultra-low energy* (ULE) MCU operates in the two main modes, i.e., active mode and sleep mode (see Fig. 2). The contribution of each mode and of switching transitions between the modes to the total energy budget is shown as follows:

$$\begin{aligned} E_{\text{TOT}} = & P_{\text{ACTIVE}} \cdot t_{\text{ACTIVE}} \\ & + P_{\text{SLEEP}} \cdot (t_{\text{CYCLE}} - t_{\text{ACTIVE}}) \\ & + E_{\text{MODE\_TRANSITION}}. \end{aligned} \quad (1)$$

In order to increase the energy efficiency at global level, the PMU should not only optimize the energy consumption in all modes of operation, but also during mode transitions [5], [6]. The voltage converters, that are the core of PMUs, are usually optimized to be efficient in either mode. Linear regulators offer a good solution to the

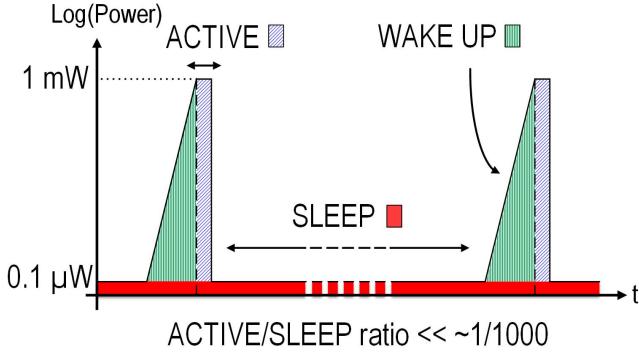


Fig. 2. Qualitative power profile of an ULE MCU.

optimization problem, but their efficiency drops dramatically as the difference between the input and the output voltage increases. Switched-capacitor regulators [7] are flexible because they can be fully integrated and are very efficient for low power loads, but they become less effective when there is a variable ratio between the input and the output voltages (e.g., battery-powered applications). Moreover, they need a larger capacitance as compared with linear regulators that increases the required energy for modes transition. Inductor-based dc–dc converters need more external components than both linear and switched-capacitor regulators, but they overcome the limitations of the aforementioned converters families. In this paper, a dc–dc converter designed to be integrated in a PMU of an ULE MCU and to improve the overall energy efficiency at the system level is presented.

This paper is organized as follows. Section II introduces the concepts behind system-oriented optimization. Section III shows our topology in detail. Section IV presents the circuit block implementation. Section V reports the experimental results of the fabricated converter. Finally, the conclusions are presented in Section VI.

## II. SYSTEM-ORIENTED OPTIMIZATION FOR ULTRA-LOW ENERGY PMU

State-of-the-art PMUs are mostly designed to maximize their active power efficiency when they supply their maximum loads. However, at system level, the active power optimization alone might not be enough to reach the optimum, i.e., the minimum energy consumption per active cycle. The assumption that the active power optimization leads to the minimum of the system energy, for a full cycle is valid, when the active phase is dominant in the total energy budget. For ULE application, the active phase is seldom dominant and the balance between active mode, sleep mode and mode transition, or wake-up (see Fig. 2) is key to reach the energy minimization.

Fig. 2 shows the three main phases of a full cycle of an ULE application: active mode, sleep mode, and wake-up. During the active mode, the system is fully operational and the circuits (e.g., MCU, peripherals, and so on) are executing the tasks they are designed for. The energy consumed in this phase is described by the first term of (1), i.e.,  $P_{ACTIVE} \cdot t_{ACTIVE}$ .  $P_{ACTIVE}$  is the average power consumption during active mode and  $t_{ACTIVE}$  is the amount of time in an active cycle that the system spends in active mode. The sleep mode is when the

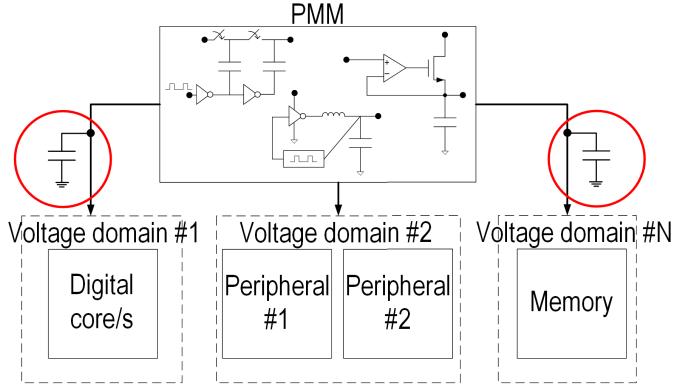


Fig. 3. Block diagram of an MCU.

system is idling or partially turned off waiting for the next active phase. In this phase, the energy goes to circuits that are always on to keep the application alive and reactive (e.g., digital power control circuits and retention flops storing the configuration of digital circuits only active in the active phase), while the leakage is minimized by powering down or reducing the supply voltage in digital domains (e.g., CPUs and digital logic). The energy consumed in this phase is described by the second term of (1), i.e.,  $P_{SLEEP} \cdot (t_{CYCLE} - t_{ACTIVE})$ .  $P_{SLEEP}$  is the average power consumption during sleep mode and  $t_{CYCLE} - t_{ACTIVE}$  is the amount of time in an active cycle that the system spends in the sleep mode.

Since most of the ULE applications spend a negligible time in active mode as compared with sleep mode [8], [9], similar focus has to be given to the optimization of the energy during sleep mode and wake-up [5], [8]. Both sleep mode and active mode contributions to the energy budget strongly depend on the specific application with only a small fraction attributed to the PMU, while the wake-up energy contribution is primarily determined by the PMU design and concept. Waking up the system means to power up all the voltage domains that have been shut down or reduced in sleep mode. Let us first consider the case where all voltage domains except the control power domain are completely powered down: the shorter the wake-up phase the less energy is required to get the system fully operational again. The power domains are usually connected to the output capacitor of the converters integrated in the PMUs that are regulating such voltages (see Fig. 3). Therefore, the time and energy needed to power up the power domains depend on the size of the output capacitors that need to be charged back from 0 V to the active voltage  $V_{ACTIVE}$ .

Equation (2) shows the total energy budget for the wake-up phase. The wake-up energy corresponds to  $E_{MODE\_TRANSITION}$ , the third element in (1), when only one active mode and one sleep mode are present in the system

$$E_{WU} \propto C_{OUT} \cdot (V_{ACTIVE} - V_{SLEEP})^2 + V_{DD} \cdot I_{BIAS} \cdot t_{WAKE-UP}(C_{OUT}). \quad (2)$$

The first term of (2), i.e.,  $C_{OUT} \cdot (V_{ACTIVE} - V_{SLEEP})^2$  represents the amount of energy needed to recharge the output capacitor itself to the target voltage  $V_{ACTIVE}$  required for the active mode, while the second term, i.e.,  $V_{DD} \cdot I_{BIAS} \cdot$

$t_{\text{WU}}(C_{\text{OUT}})$  represents the amount of energy wasted by the analog circuits while they wait for the wake-up time to refill the output capacitor.

Equation (2) shows that the smaller the output capacitor the lower is the energy budget required for the wake-up phase. In fact, a smaller capacitor requires less energy and time to be charged to a target voltage. A shorter wake-up time is dually beneficial because: 1) it allows the system to be fully operational sooner and 2) at the same time it reduces the energy overhead consumed by the circuits during the wake-up phase [see (2)]. In the second case of lowering the supply voltage in digital voltage domain (to reduce leakage current), the same consideration for saving wake-up energy holds (reduced by the difference between active and sleep supply voltages). For ULE applications, a minimized output capacitor in the PMU is therefore favorable and necessary to reach the minimal energy consumption. The reduction of the wake-up energy is limited by the digital circuit design tradeoff that the system on chip (SoC) is willing to take. In fact, a minimized capacitor might influence the accuracy of the regulated voltage—here as detailed, e.g., in [8] a 20-mV maximum ripple is accepted. Section III describes a dc–dc converter design meant to be integrated in a PMU for ULE MCUs that has been optimized to maximize the efficiency at system level.

### III. CONCEPT OF THE PROPOSED DC–DC CONVERTER

The design of the proposed buck converter is presented starting from the architecture-level to the analog implementation of the fundamental blocks.

Standard dc–dc converters usually rely on large output capacitor to achieve high power efficiency, stability, and good regulation [10], [11]. A minimized output capacitor allows the system to be energy efficient, but it worsens the regulation accuracy and could make it harder to achieve the stabilization of the converter. In ULE applications, the available power budget for the control loop of the converter (i.e., controller, driver, and power stage) is greatly reduced as compared with the standard applications. For example, the targeted application, i.e., an ULE MCU, presents a load range that spans from 2.65-mA down to 100 nA. Often a few  $\mu\text{W}$  are needed to operate [9], [12] resulting in a maximum controller power budget in the order of hundreds of nW to guarantee a good efficiency. The primary design challenge for the proposed converter is to guarantee good regulation capability and power efficiency with a very small output capacitor and a strictly limited power budget [13]. The minimization of the capacitor leads to a first tradeoff with the inductor size. For a given output power budget, the ripple voltage on the output capacitor is proportional to the equation as follows:

$$V_{\text{RIPPLE}} \propto \frac{T_{\text{ON}}}{L \cdot C_{\text{OUT}}} \quad (3)$$

Considering (3), either reducing  $T_{\text{ON}}$  or increasing  $L$  are the only two options to keep the output ripple constant and within specifications. Reducing  $T_{\text{ON}}$  leads to an increase of the switching frequency and, consequently, to an increase of losses that worsen the power efficiency; however, increasing

$L$  requires the use of a larger inductor. A reduction in (3) must be compensated by improving the remaining variables. To avoid an excessive increase of the inductance value,  $T_{\text{ON}}$  has to also decrease. As a consequence, the switching frequency that is inversely proportional to  $T_{\text{ON}}$  increases and is higher as compared with the standard dc–dc converters. A choice of 18  $\mu\text{H}$  for a 56-nF output capacitor is a good tradeoff to achieve a good conversion efficiency for 2.65-mA maximum load at small wake-up energy. Despite the large value of inductance, the required inductor form factor is small due to the low current rating. In this design, an SMD inductor (Coilcraft XPL2010) that occupies 4  $\text{mm}^2$  is used. This is still small as compared with the standard MCU package, the inductor is attached to. The controller must react quickly to changes in the output voltage. Consequently, the inductor current must be rapidly steered around the dc current value of the load because the exceeding inductor current is integrated in the output capacitor. The smaller the output capacitor the larger is the output voltage variation, when the exceeding inductor current is integrated. Therefore, a slow and complex control loop might easily drive the output ripple out of specification when a minimized capacitor is used. A standard voltage mode or current mode control based on PID or PI compensator requires an  $RC$  compensation network together with an operational amplifier. The operational amplifier poses a significant limitation in terms of either bandwidth or power consumption for the regulation loop. Due to the limited power budget available for the regulation loop, the operational amplifier could only guarantee a minimal bandwidth that might not be sufficient to properly regulate the voltage over a minimized output capacitor.

In contrast, hysteretic control is, in general, faster than voltage and current modes. Specifically, the *single-bound hysteresis control* (SBHC) differs from the traditional hysteretic operation wherein  $V_{\text{OUT}}$  is maintained between two voltages levels. SBHC is more commonly used in switched-capacitor converter design [14], [15] and the earliest implementation has been introduced in [14]. In this control technique,  $V_{\text{OUT}}$  is regulated around a single-bound reference voltage. As a result, the delay introduced by the comparator hysteresis is eliminated, thereby enhancing the closed-loop response considerably. The main drawback of this approach is the limited accuracy in the regulation of the output voltage. Moreover, the loop speed mainly depends on the propagation delay of the comparator that is process, voltage and temperature (PVT) dependent. A non-hysteretic control mode can definitely improve the regulation accuracy but it would make the response time of the loop slower. The high speed of the loop is key to minimize the output capacitor therefore the SBHC is a suitable choice for the implemented buck converter. The proposed controller, in Fig. 4, consists of a comparator, a pulse generator, a driver, and a power stage. The comparator *COMP* compares the voltage at the capacitor  $C_{\text{OUT}}$  to a reference voltage  $V_{\text{REF}}$  and provides ON- and OFF-signals to the *pulse generator*. The pulse generator provides the driver with the  $T_{\text{ON}}$  and  $T_{\text{OFF}}$  pulses for the P and nMOS devices of the power stage.

Restricting this regulation to *discontinuous conduction mode* (DCM) shown in Fig. 5, the system is asymptotically

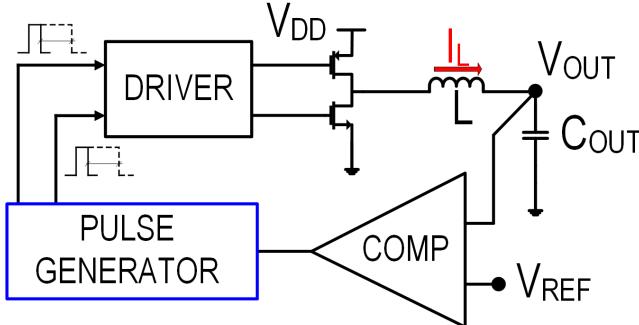


Fig. 4. Proposed dc-dc architecture.

stable [16]. Furthermore, DCM allows the system to optimize the amount of energy delivered to the output in an active cycle. In fact, when the inductor is completely discharged at the end of every active cycle, i.e., DCM, the energy delivered to the output (both output capacitor and load) can be exactly estimated as follows:

$$E_{\text{IN} \rightarrow \text{OUT}} = \frac{V_{\text{OUT}} \cdot I_{\text{PEAK}} \cdot (T_{\text{ON}} + T_{\text{OFF}})}{2} \Big|_{T_{\text{IDLE}}=0}. \quad (4)$$

$I_{\text{PEAK}}$  is the peak value of the inductor current reached at the end of  $T_{\text{ON}}$  (see Fig. 5). The  $T_{\text{IDLE}}$  phase has no influence on the output energy budget because in this phase the inductor is completely discharged and the output capacitor sources the load. The amount of energy delivered to the output can then be optimized for a given load and a minimized output capacitor by choosing and keeping under control the optimal  $I_{\text{PEAK}}$ . The repetition frequency of the “single packet of energy” per active cycle ( $T_{\text{ON}} + T_{\text{OFF}}$ ), which is represented by the current triangle in Fig. 5 is self-defined by the load current. In fact, the higher the load current, the faster the output capacitor discharges and vice-versa at lower load currents. The discharging rate of the output capacitor defines  $T_{\text{IDLE}}$  (see Fig. 5) and in turns the pulse repetition frequency.

For this design (56 nF, 18  $\mu$ H), typical  $T_{\text{ON}}$  and  $T_{\text{OFF}}$  times correspond to a switching frequency between 3 and 5.5 MHz at maximum load. The estimated power budget breakdown at the two frequency limits is shown in Fig. 6.

This approach makes the system capable of reacting fast to abrupt changes in the load magnitude that is a typical situation for digital loads and inherently limits the maximum load current. In fact, when the load current exceeds the maximum value,  $T_{\text{IDLE}}$  approaches 0 s and the controller generates active pulses continuously (Fig. 5). Therefore, no more power can be delivered to the output. Beyond this point, a further increase of the load current leads to a drop of the output voltage and has to be avoided in the application (e.g., by a clock frequency limit for all applications running simultaneously). Our approach minimizes also overshoots and undershoots during load transients. In fact, unlike *continuous conduction mode*, the inductor is discharged after every active cycle and in the worst case scenario the output capacitor should only store the controlled energy of a “single packet,” i.e., a single current pulse. DCM also allows its own regulator power consumption to scale rather well with the load current of an

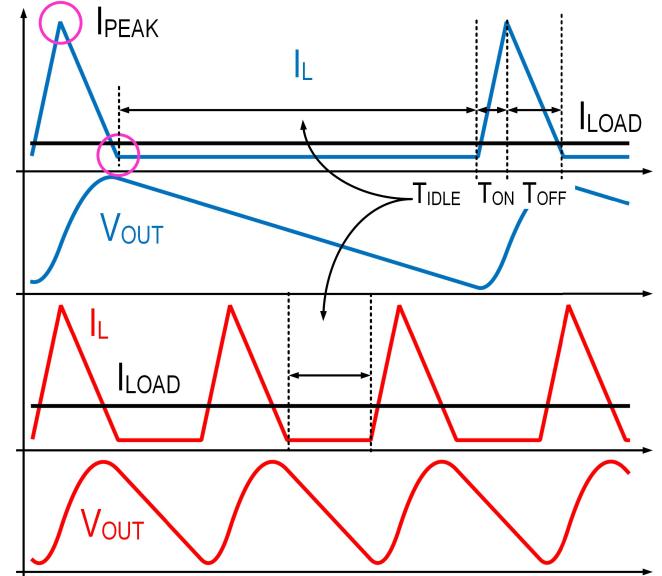


Fig. 5. Time diagram of inductor current and output voltage in DCM at different current loads.

MCU [16]. In fact, a significant part of the current needs of the controller is dynamic with the update rate, and therefore scales with lower update rates. This means that also in the light load condition the system efficiency stays high. For all the aforementioned reasons, DCM is the best choice for our implementation. The inductor current must then be regulated to achieve the optimal performance for the controller.

Common peak current control in DCM relies on the detection of two boundary conditions (pink circles in the time diagram in Fig. 5): the optimum  $I_{\text{PEAK}}$  determines the length of the  $T_{\text{ON}}$  pulse and the zero current crossing determines the length of the  $T_{\text{OFF}}$  pulse. A critical boundary condition for good efficiency is the detection of the zero current crossing. Usually, very fast and precise detectors and sensors are designed to perform this task. To overcome speed-related constraints and to save power, an innovative predictive peak current control scheme is proposed. Both pulses are determined by integrating the inductor equation [16]

$$V_L = L \cdot \frac{\partial I_L}{\partial t} \quad (5a)$$

$$\int \partial t = \frac{L}{V_L} \int \partial I_L \rightarrow \begin{cases} T_{\text{ON}} = \frac{I_{\text{PEAK}} \cdot L}{V_{\text{DD}} - V_{\text{OUT}}} \\ T_{\text{OFF}} = \frac{I_{\text{PEAK}} \cdot L}{V_{\text{OUT}}} \end{cases} \quad (5b)$$

For a given optimal peak current  $I_{\text{PEAK}}$  and inductor size  $L$ , the width of the pulse  $T_{\text{ON}}$ , which drives the high-side switch, is inversely proportional to the difference between  $V_{\text{DD}}$  and  $V_{\text{OUT}}$ . The related circuits will be described in Section IV-D. The width of the pulse  $T_{\text{OFF}}$  driving the low side switch is inversely proportional to  $V_{\text{OUT}}$  [see (5)]. Consequently, the controller dynamically adapts the widths of both  $T_{\text{ON}}$  and  $T_{\text{OFF}}$  pulses with respect to  $V_{\text{DD}}$  and  $V_{\text{OUT}}$  changes [see (5)]. With such a control scheme, the system keeps  $I_{\text{PEAK}}$  close to its optimum value and predicts the zero-crossing point at almost no power consumption. The optimum value of  $I_{\text{PEAK}}$

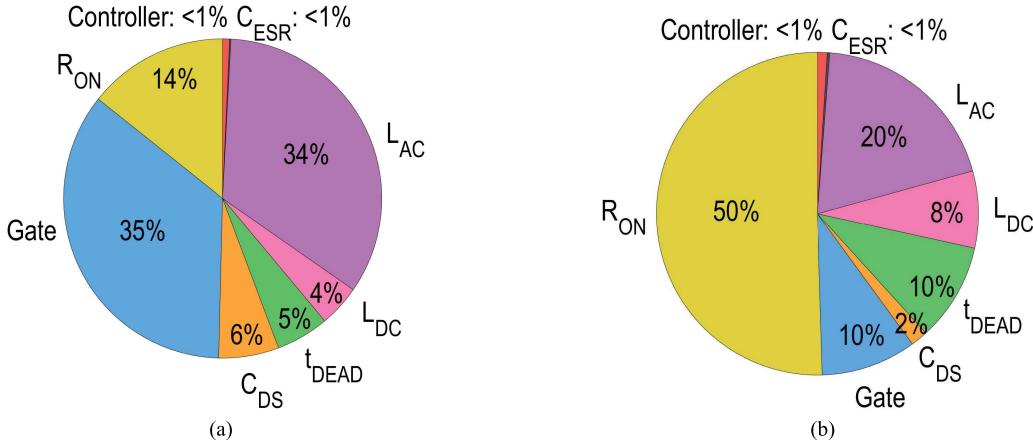


Fig. 6. Estimated power budget breakdown at the two frequency limits at (a) 5.5 MHz and (b).

has been chosen by means of computer simulations. A script has been implemented to model and optimize the overall losses for a given minimized capacitor. This script takes as inputs the value of the desired minimized capacitor, technology parameters, input and output range, maximum output voltage ripple and maximum load of the dc-dc converter, and key parameters of the reactive components (e.g., ESR, DCR, and so on) and provides as output the high-side and low-side switch size, inductor size, and the optimum value of  $I_{PEAK}$ . A similar approach has been presented in [10] and [17]. The main differences with the proposed control scheme are the following.

- 1) The  $T_{ON}$  generation, in this paper, is based on the direct sensing of  $V_{OUT}$ . Therefore, the regulation can be achieved for a wider range of  $V_{OUT}$  values, enabling the voltage scaling of the regulated voltage.
- 2) The  $T_{OFF}$  generation in [10] is based on the use of a detector. In the presented design,  $T_{OFF}$  generation is based on a predictive approach.
- 3) The FSM of this paper allows the system to regulate a voltage close the reference (e.g., absolute maximum current load) and beyond with an output voltage drift toward 0 V. This approach limits the maximum current (overload protection) and allows the system to recover from the temporary overload conditions as well.

The proposed control technique is valid for a known inductance value of the inductor. In fact, both pulses are proportional to a constant  $I_{PEAK} \cdot L$  that is the product between the optimal inductor peak current and the inductance value of the inductor  $L$ . While  $I_{PEAK}$  is a design parameter, the inductance value is influenced by external parameters (e.g., manufacturing tolerances, temperature, and so on). Therefore, the system is designed to use the nominal value of the inductance at the startup and to withstand inductor tolerances up to 30%. It can start without the exact knowledge of the inductor value at reduced efficiency. From here, the effect of manufacturing tolerances is fixed by a one-time adjustment to achieve optimal efficiency, i.e., the constant  $I_{PEAK} \cdot L$  of (5) is adjusted to compensate the variation of  $L$  from its nominal value. Such trimming procedure is a standard process for power regulation

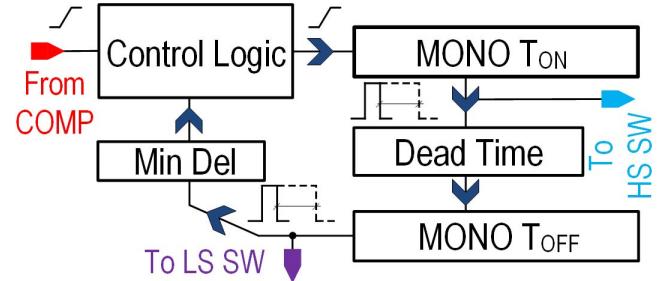


Fig. 7. Block diagram of the proposed pulse generator.

circuits integrated into an MCU [12]. As an example, the one-time adjustment can be done by measuring the difference in the expected voltage slope and the actual slope of the voltage on the high-side switch when it is biased with a specific supply voltage and turned on. Such slope depends on the actual inductor value [18]. Section IV presents the detailed implementation of the main blocks of the controller.

#### IV. CIRCUIT BLOCK IMPLEMENTATION

##### A. Pulse Generator

The pulse generator, shown in Fig. 7, is the core of the whole controller. The system has two stable states as expected from a hysteretic controller [16]: an ACTIVE state and an IDLE state. In the IDLE state, the pulse generator is frozen and  $V_{OUT}$  is equal to or greater than  $V_{REF}$ . The ACTIVE state represents the regulation phase wherein  $V_{OUT}$  is smaller than  $V_{REF}$ . In this phase, the pulse generator generates the  $T_{ON}$  and  $T_{OFF}$  pulses according to the predictive function described in Section III. The minimized capacitor  $C_{OUT}$  is then recharged via the power MOSFETs. The operation of the pulse generator is described herein detail: first, the control logic monitors the comparator output to detect an activation signal (i.e.,  $V_{OUT} < V_{REF}$ ). When an activation signal is asserted, a new active cycle starts: the control logic triggers the  $T_{ON}$  monostable and blanks the comparator's output until the end of the current active cycle. This second function guarantees both the DCM condition and the stability of the pulse generation phase. The  $T_{ON}$  mono-stable generates a variable on-pulse for

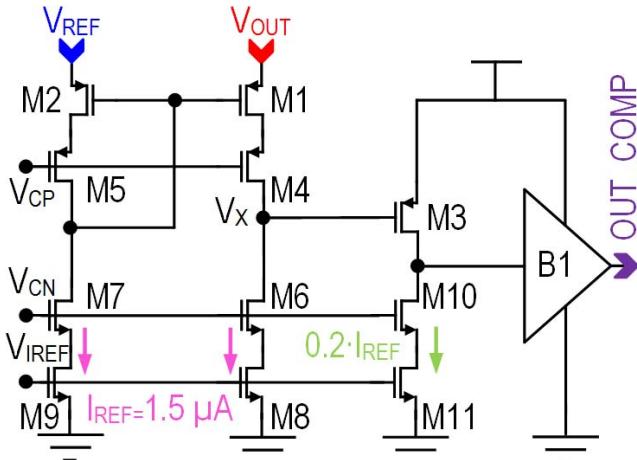


Fig. 8. Schematic of the output comparator.

the high-side switch. To avoid both switches to be open at the same time, a dead-time delay circuit is triggered next. Then, the  $T_{OFF}$  mono-stable generates the pulse for the low side switch. A delay (MIN-DEL) is finally added to the active cycle to dump any residual energy in the inductor. It also provides a known initial condition for the next active cycle (i.e.,  $I_L = 0$ ). The MIN-DEL delay increases directly proportional to the parasitic capacitance at the switching node and inversely proportional to the core losses of the inductor. After the MIN-DEL, the delayed edge of the  $T_{OFF}$  pulse clears the control logic. Then, the control logic starts again to monitor the comparator activity to determine the beginning of the next active cycle.

#### B. Comparator

The output comparator COMP is directly connected to the main control variable: the output voltage  $V_{OUT}$ . It is responsible to provide the ON-OFF signal to the pulse generator. Although, the output voltage dynamics can partially be foreseen [8], an accurate and continuous monitoring is necessary to guarantee a good regulation. For the aforementioned reason, a continuous-time topology is preferred to a clocked one. The input pair is based on a pMOS common-gate topology because the supply voltage is in the range of the dc-dc output voltage that is compared at the input of the comparator. With this topology, it is possible to avoid the resistive division of the input signal. In this way, there is no attenuation of the input signal variations and the area for the resistive divider might be saved or used for other devices. The proposed topology shows also some drawbacks: e.g., the reference is loaded with the bias current  $I_{REF}$ . This poses a limit to maximum reference current and in turn to the maximum gain of the comparator. A schematic of the output comparator is shown in Fig. 8. The source of M1 is directly connected to the monitored output  $V_{OUT}$ , while the source of M2 is connected to the reference voltage  $V_{REF}$ . M2 generates the proper bias voltage proportional to the reference voltage for M1. M1 varies its current depending on the dynamics of  $V_{OUT}$ . As a consequence, the node  $V_x$  is charged as  $V_{OUT}$  increases or discharged as

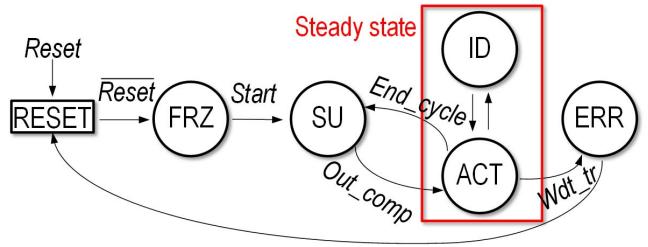


Fig. 9. Bubble diagram of the FSM.

$V_{OUT}$  decreases. A voltage at node  $V_x$  larger than  $V_{OUT}$  leads to conduction through the body diode of M1. Such harmful condition should be avoided. As long as  $V_{OUT}$  is greater than GND and its dynamics are slower than the one of  $V_x$ , the body diode of M1 is never forward biased.  $V_x$  voltage level is then the comparison result between  $V_{REF}$  and  $V_{OUT}$ . The analog comparison result is then amplified by the pMOS common source stage composed by M3. The buffer B1 finally amplifies toward the rail the comparison result. M4–M5–M6–M7–M10 are the cascodes of the input pair and the current sources composed by M8–M9–M11.

#### C. Control Logic

The control logic is an asynchronous *finite-state machine* (FSM) that supervises and manages the regulator in all its functional states (e.g., startup, regulation, and so on). Fig. 9 shows a bubble diagram of the FSM. Each bubble represents a state in which the proposed converter can operate. The five states are *frozen* (FRZ), *startup* (SU), *idle* (ID), *active* (ACT), and *error* (ERR). The input signals are five: reset, start, out\_comp, end\_cycle, and wdt\_tr, while the output signals are ton\_gen toff\_gen err\_flag. First, the controller enters FRZ after the reset signal is deasserted. In this state, the controller is insensitive to all signals but start. The signal start determines the beginning of startup phase of the converter, i.e.,  $C_{OUT}$  is completely discharged and  $V_{OUT}$  is equal to 0 V. When start is asserted the controller enters SU. This state is very similar to ID described in Section IV-A; the main difference between these two states are the variables (voltage levels) fed to the two mono-stables that embodies the predictive current control described in Section III and shown in Fig. 7. An analog multiplexer feeds either  $V_{REF}$  in SU or  $V_{OUT}$  in ID to the mono-stables to always ensure the correct calculation of  $T_{ON}$  and  $T_{OFF}$ . Especially, the calculation of  $T_{OFF}$  is critical during the startup phase; in fact,  $V_{OUT}$  in (5) is at the denominator of the  $T_{OFF}$  expression and must always be different from 0 V to guarantee the stability of the system. The FSM toggles between SU and ACT depending on the value of out\_comp and end\_cycle to refill the output capacitor and reach the reference voltage. If the reference voltage is never reached, i.e., SU fails, the proposed FSM cannot recover from this condition on its own. The detection of SU failure is skipped in this FSM because the target application of the proposed buck converter is the integration in a PMU of an MCU. In standard PMUs, there are also one or more supervisor FSMs that keep track of the external and internal

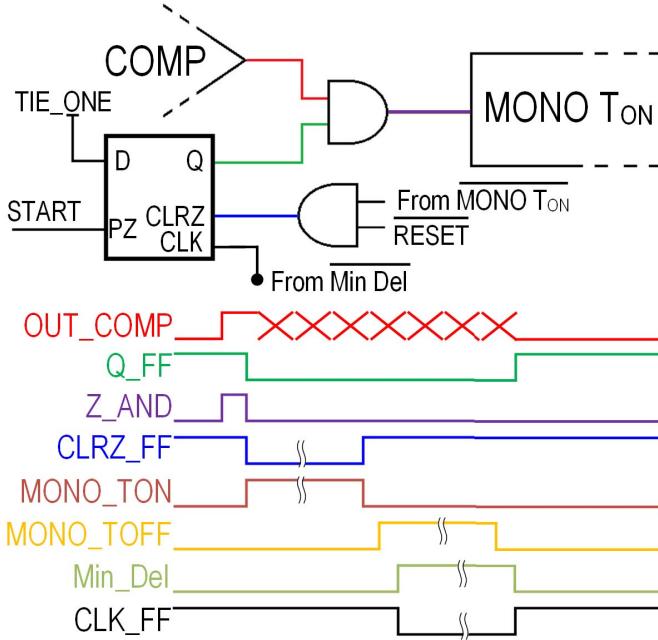


Fig. 10. Block diagram of the implementation of the four main states of the FSM.

generated voltages. These FSMs take care of generating reset signals and/or to manage the startup sequence of the core converters. If an SU failure is detected, the supervisor FSM in the PMU could potentially increase the  $T_{ON}$  length to solve the issue. The controller switches between SU and ID after the first assertion of out\_comp, i.e., when the comparator indicates that the steady-state voltage equal or greater than  $V_{REF}$  has been reached for the first time. After this transition from SU to ID the analog multiplexer permanently feeds the mono-stable with  $V_{OUT}$ . From here, the controller toggles between ID and ACT to regulate the output voltage: this phase represents the steady-state condition for hysteretic controllers [Fig. 9 (red square)]. Fig. 10 shows the implementation of the four main states of the FSM. In ACT, the mono-stables generate  $T_{ON}$  and  $T_{OFF}$  according to (5) and the following algorithm: in Fig. 10, when an active cycle starts the inverted output of  $T_{ON}$  generated by the  $T_{ON}$  mono-stable forces a 0 on the CLRZ of the D-FF.  $Q$  is therefore forced to 0 and gates the output of COMP through the AND gate. During a regulation cycle the output of the comparator is ignored by the system. At the end of the regulation cycle, the rising edge of the inverted and delayed  $T_{OFF}$  pulse triggers the CLK input of the D-FF. The D input is tied to 1 therefore  $Q$  becomes 1. This last step represents the generation of the end\_cycle that asserts the end of the generation of one active cycle in the FSM, shown in Fig. 9, and allows the system to go back to ID and monitor out\_comp again. If, after the previous regulation cycle, the output voltage ended up close to the reference voltage generating chattering in the comparator the system triggers an active cycle at the first 0 → 1 edge of the out\_comp and blinds the comparator again until the end of the current regulation cycle. In this way, the DCM is guaranteed in every condition as well as the stability of

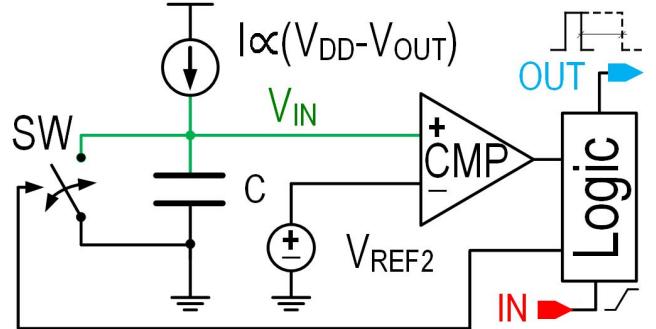


Fig. 11. Block diagram of the  $T_{ON}$  mono-stable.

the predictive current mode. The last state ERR does not influence the regulation capability of the converter. It has been included for safety reasons only; the  $T_{ON}$  duration is monitored by an analog watchdog to avoid an over current condition on the inductor and consequently an over voltage condition at the output. If, for any reason, the  $T_{ON}$  generation fails and lasts too long the watchdog asserts wdt\_tr and the FSM enters the ERR state. In this state, the pulse generation is stopped, the power stage is set to high impedance,  $C_{OUT}$  is discharged, and the error signal err\_flag is asserted. The controller cannot escape the ERR state until the FSM is reset. This state is optional and can be excluded from the FSM by disabling the watchdog.

#### D. Mono-Stables

The  $T_{ON}$  and  $T_{OFF}$  mono-stables embody the predictive current control generating the  $T_{ON}$  and  $T_{OFF}$  pulses according to (5) [17]. The duration of the pulse  $T_{ON}$  is described by the following:

$$T_{ON} = \frac{I_{PEAK} \cdot L}{V_{DD} - V_{OUT}}. \quad (6)$$

Equation (6) is implemented exploiting the relationship between the time constant of a capacitor charged by a current and the induced voltage drop. The time  $T_{CH}$  to charge a capacitor  $C$  with a current  $I_X$  to a target voltage  $V_{TG}$  can be expressed as follows:

$$T_{CH} = C \cdot \frac{V_{TG}}{I_X}. \quad (7)$$

Fig. 11 shows a block diagram of the implemented mono-stable. The variable pulse generation is triggered by a positive edge on the mono-stable input (pin "IN" in Fig. 11). This signal opens the reset switch SW parallel to the capacitor  $C$ . Such reset switch is mandatory to ensure a known initial condition for the charging phase of the capacitor during the pulse generation, i.e.,  $V_C$  equal to 0 V. A current proportional to the voltage difference  $V_{DD} - V_{OUT}$  flows into the capacitor  $C$  until the voltage at node  $V_{IN}$  reaches the target voltage  $V_{REF2}$  (see Fig. 11). When  $V_{IN}$  is equal or greater than  $V_{REF2}$ , the comparator CMP toggles and the LOGIC stops the pulse generation. The block LOGIC controls both the pulse generation and the reset phase of the mono-stable. The time diagram of the pulse generation phase is shown in Fig. 12.

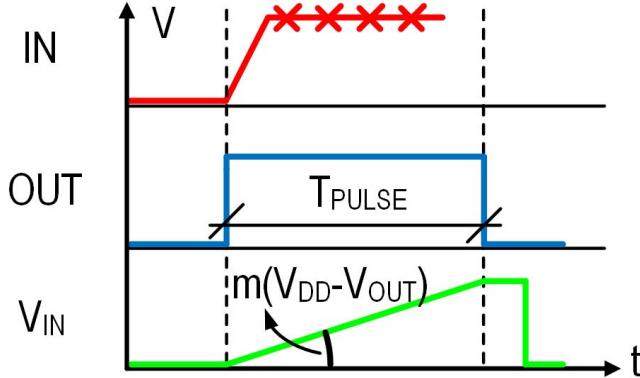


Fig. 12. Time diagram of the pulse generator.

The resulting pulselength  $T_{\text{PULSE}}$  on the OUT pin, shown in Fig. 12, can be described by (7)

$$T_{\text{PULSE}} = C \cdot \frac{V_{\text{REF2}}}{gm \cdot (V_{\text{DD}} - V_{\text{OUT}})}. \quad (8)$$

The capacitor  $C$  is charged to  $V_{\text{REF2}}$  that represents the target voltage  $V_{\text{TG}}$  in (7) and the current  $I_X$  in the mono-stable is the current proportional to the voltage difference  $V_{\text{DD}} - V_{\text{OUT}}$ . To better show the dependence of the current from the variable  $V_{\text{DD}} - V_{\text{OUT}}$ , it can be rewritten as  $gm \cdot (V_{\text{DD}} - V_{\text{OUT}})$ . It is then possible to generate the proper  $T_{\text{ON}}$  pulse by matching the value of the variables in (6) to the ones in (8)

$$C \cdot \frac{V_{\text{REF2}}}{gm} = I_{\text{PEAK}} \cdot L \implies T_{\text{PULSE}} = T_{\text{ON}}. \quad (9)$$

The predictive pulse generation can be tuned on the actual value of the inductor. The tuning is also beneficial to compensate variation in  $C$ ,  $V_{\text{REF2}}$ , and  $gm$ , but it does not correct temperature-dependent effects. To tune the mono-stables in Fig. 11, there are three possibilities: either the  $gm$  of the current generator or the capacitor size or the  $V_{\text{REF2}}$  value can be adjusted. If the current source in Fig. 11 generates a current proportional to  $V_{\text{OUT}}$  only, the denominator in (8) becomes  $gm \cdot V_{\text{OUT}}$ . Matching the variable shown in (9) allows the mono-stable to generate the proper  $T_{\text{OFF}}$  pulse. The main analog blocks of the  $T_{\text{ON}}$  mono-stable are the voltage-dependent current source  $I_{\text{VDD-VOUT}}$  and the comparator CMP. Their schematics are shown in Figs. 13 and 14, respectively. In the voltage-dependent current source, two voltage buffers set a voltage difference across the resistance  $R$ . The first buffer is a pMOS super source follower composed by M2 and M3. This buffer sets  $V_Y$  to  $V_{\text{IN}2} + V_{\text{SG}2}$ . The transistors M1, M4, and M5 form a pMOS flipped super source follower that sets  $V_X$  to  $V_{\text{IN}1} + V_{\text{SG}1}$ . M6 mirrors the output current flowing into M5. With proper matching of M1 and M2 the current flowing in M5 is then equal to  $(V_{\text{IN}1} - V_{\text{IN}2})/R$ . When  $V_{\text{IN}1}$  and  $V_{\text{IN}2}$  are proportional, respectively, to  $V_{\text{DD}}$  and  $V_{\text{OUT}}$  the current generator provides the proper current for the  $T_{\text{ON}}$  pulse generation [19]. CMP is a time-continuous dual stage comparator. The first stage [Fig. 14 (red circle)] composed by M1, M2, and M3 is a differential pMOS input pair loaded by  $R$ . After this first stage with a moderate gain, there is a complementary self-biased differential amplifier [20]. This

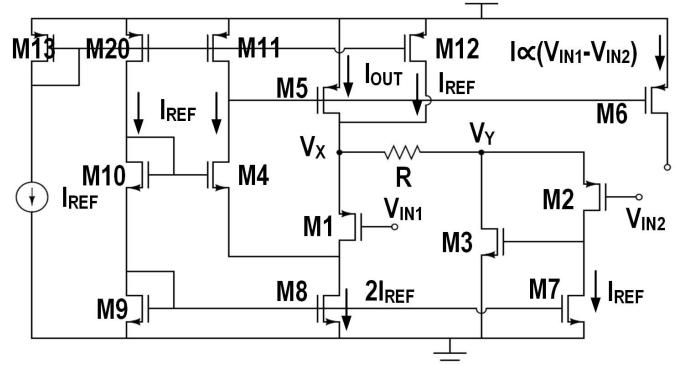
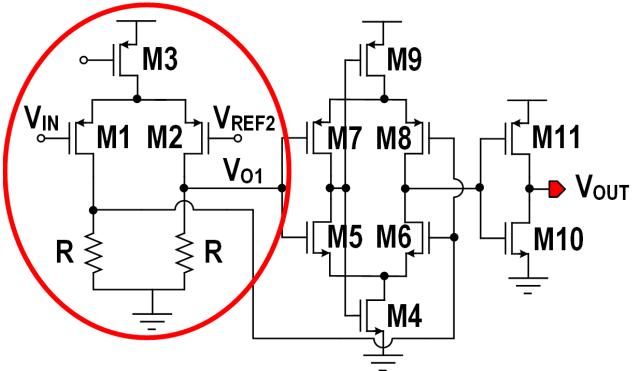
Fig. 13. Schematic of the  $I \sim (V_{\text{DD}} - V_{\text{OUT}})$  current generator.

Fig. 14. Schematic of the comparator CMP.

stage has a higher gain and a minimized power consumption. In fact, this topology consumes power only during transitions. M4 and M9 supply the amplification stage M5, M6, M7, and M8 only when both transistors conduct ( $V_{\text{O}1}$  nearly equal  $V_{\text{DD}}/2$ ). M10 and M11 are the final inverter that strongly amplifies the output signal of the second stage. In active mode, the main branches of these circuits are fully biased while in low power mode (LPM) the bias is reduced or, for some branches, even shut down. The generation of  $T_{\text{OFF}}$  is based on the same topology shown in Fig. 11. In (5), the denominator of  $T_{\text{OFF}}$  only depends on  $V_{\text{OUT}}$ . Therefore, the main difference with the  $T_{\text{ON}}$  generation comes from the voltage-dependent current source  $I$  in Fig. 11 that provides a  $V_{\text{OUT}}$ -dependent current. This current source is implemented with a standard operational transconductance amplifier (OTA).

### E. Operating Modes

Regulators for ULE MCUs have to supply a wide range of load currents. Often the output power range spans over the orders of magnitude. The controller should therefore be able to fulfill the requirements in terms of bandwidth for the maximum load current, but at the same time the available power budget for regulation drops to nW for good efficiency when sub- $\mu$ A current is supplied. DCM helps to scale the power consumption of the controller with the load current but it is limited by the fixed power consumption that derives from circuits: specifically, the power for the bias of analog

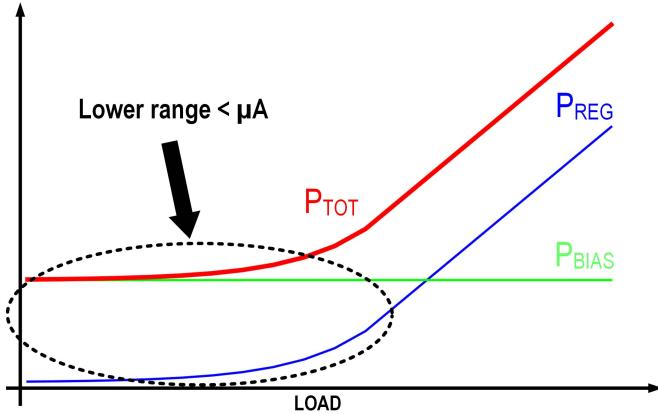


Fig. 15. Qualitative power profile of a DCM buck converter.

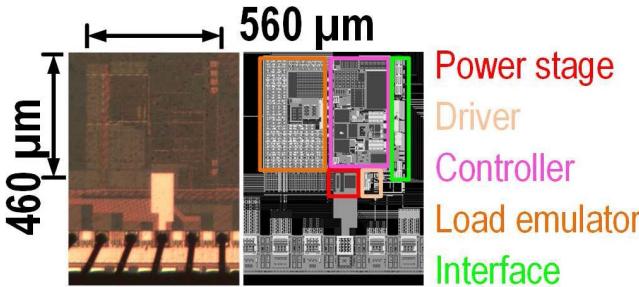


Fig. 16. Die photograph and layout.

circuits and/or the leakage of digital circuits. Fig. 15 shows the high-level profile of the power consumption against the load current for a DCM controller.

$P_{REG}$  is the power component that derives from the activity of the circuits during regulation. It is proportional to the switching frequency and in turn to the load. In the lower range of the supplied load, it becomes negligible and  $P_{BIAS}$  is dominant. This component is independent of the load and it is only defined by the specification of the circuits. The DCM alone cannot optimize the power consumption in the lower range of the load. The bias power should be scaled down depending on the load level. However, sudden changes in the MCU load current—worst cases are load jumps from circa 100 nA to a couple of mA happens depending on the switching activity of the MCU. A fully analog regulation can hardly react to such sudden changes in the load, especially when the bias power is minimized to improve the efficiency at the cost of a lower controller bandwidth. For an integrated regulator supplying an MCU system, the load magnitude can be estimated in advance as it strongly depends on the clock speed of the system and the power mode of the MCU itself [8]. If the load current need is changing, the system will indicate a power-clock mode change a few clock cycles ahead of the expected load current change. The dc–dc will be ready to take this current at the time when it occurs. For the sake of simplicity and demonstration, the presented converter has only two operating modes: active mode and low power mode. In active mode, the circuits of the controller operate at full power and speed. The resulting power losses inherently scale

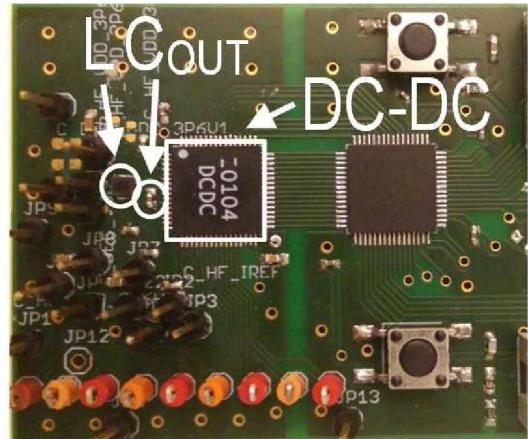


Fig. 17. PCB and scheme of measurements setup.

with the load current due to the DCM operation. In low power mode, the bias power of the circuits is scaled in relation to the information received by the MCU about its own activity. For this purpose, a bias control system is integrated into the controller. The bias control system is controlled by the MCU. In LPM, when the BCS imposes the highest bias reduction, the analog circuits either operate in deep subthreshold or they are completely shut down. Therefore, the bandwidth of the analog loop is greatly reduced. This loss in bandwidth for the analog part of the system can be compensated by the information about the clock activity that the system receives from the MCU [8], [12]. Reference [21] is an example of how the reduced bandwidth and driving capability at lower power can be realized for such systems. Depending on practical load current range needs, several modes can be added. In the presented system, active mode shows the best performances between 2.65 mA and 3  $\mu$ A, and low power mode from 3  $\mu$ A to 100 nA load current.

## V. EXPERIMENTAL RESULTS

The proposed dc–dc converter is implemented in a 130-nm CMOS technology and occupies 0.14 mm<sup>2</sup>. Fig. 16 shows both die photograph and layout. The silicon is packaged in a VQFN 64 pins (9 mm  $\times$  9 mm) using standard bonding. This

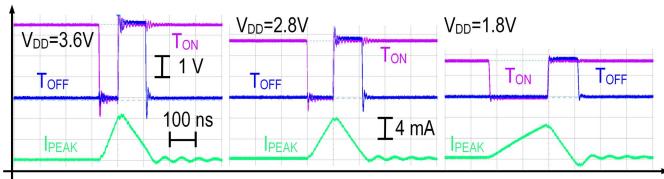


Fig. 18. Behavior of the predictive peak current control.

package is commonly used for ULP MCUs and includes the typical parasitic structure that might load the converter in a practical use case.

Measurements are performed with an external inductor (18  $\mu$ H) from Coilcraft (XPL2010) and capacitor (56 nF) from Murata (GRM series). Despite the large value of the inductance, the form factor of the inductor is quite small (4 mm<sup>2</sup>) as compared with a typical MCU package. References, always available in a systemlike [12] are off-chip. Fig. 17 shows the PCB and the diagram of the measurement setup. The three main elements of the system are highlighted, i.e., the IC that contains the controller and the power stage of the converter, the 18- $\mu$ H inductor and the output capacitor. The inductor occupies  $\sim 5\%$  of the surface taken by the IC. In Fig. 18, the experimental behavior of the converter loop is shown at different input voltages. As expected, the  $T_{ON}$  pulse varies with  $V_{DD}$  and  $T_{OFF}$  does not change keeping the  $I_{PEAK}$  constant. At the lowest input voltage level (1.8 V), a small reduction of the peak current occurs. This is caused by the combination of two effects: 1) the increase of  $R_{ON}$  of the high-side switch due to the low voltage level generates a higher voltage drop and 2) this drop has a stronger influence on the inductor voltage that is at its minimum ( $V_{DD\_MIN} - V_{OUT}$ ).  $T_{ON}$  and  $T_{OFF}$  pulses have been measured over temperature in order to verify the stability of the controller. The width of both pulses does not vary more than 10%. In Section II, the advantages of using a minimized output capacitor were discussed. Both the wake-up energy and the startup delay are reduced. In this context, the startup delay is the amount of time that the converter needs to recharge the output capacitor from 0 V to the target value  $V_{REF}$ . Fig. 19 and Table I show the best and worst cases over temperature. Even the worst case startup delay is considerably smaller as compared with the state-of-the-art dc–dc converter [22] which show startup times in the order of hundreds of  $\mu$ s. The effect of the temperature on this parameter is significant (Table I) because the converter has not been specifically optimized for this purpose.

The converter is designed for an MCU digital core as load. The supplied voltage must remain within a tolerance of  $+30/-70$  mV to guarantee a fault-free operation [8]. As already mentioned in Section IV-E, the worst case load condition for such system is represented by a current step from sleep mode to active mode (see Section IV-E, MCU running at maximum clock speed). In Fig. 20, the system reaction for such a step current change in both directions is shown. The MCU load is emulated by on-chip current sources. The converter can properly regulate this worst case load change with a ripple lower than 30 mV. The transition times in Fig. 20 are less than 200 ns for all load transitions.

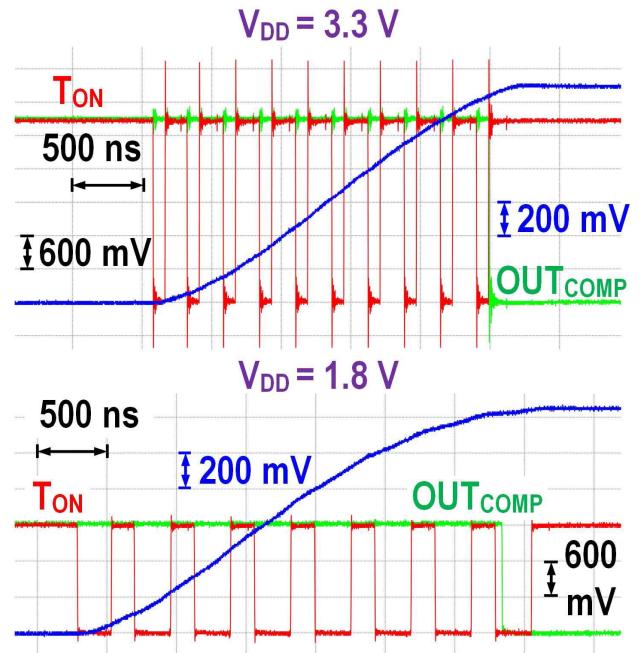


Fig. 19. Best and worst case for the startup delay.

TABLE I  
STARTUP DELAY ( $\mu$ s)

$V_{DD}$	Temp	-40	27	95
3.3 V		2.11	2.40	3.14
3.0 V		2.21	2.49	3.16
2.7 V		2.32	2.59	3.27
2.4 V		2.47	2.69	3.39
2.1 V		2.44	2.80	3.68
1.8 V		2.55	3.04	4.16

The effect of the offset in the comparator can be observed in Fig. 20. At 2.65 mA, the regulator is close to its absolute maximum load. In this condition, the regulated voltage at the end of an active cycle is close to the reference voltage. When the difference between the regulated and reference voltages is in the offset range (a few mV), the comparator might keep its high state. When the FSM senses a high state in the comparator output right after a regulation cycle, it immediately triggers the next one. This effect is visible in the waveform at 2.65-mA load. The small peak represents the regulation cycle in which the comparator stays high and the high peak is the second cycle issued by the FSM to recover the overload condition. The final voltage at max to min load step represents the absolute worst case: a load step at the beginning of a regulation cycle. In this situation, almost all the charge in the inductor is integrated in the capacitor and the ripple is maximum.

Tables II and III show the line and load regulation performance in active mode. The characterization of these two parameters is done in active mode only because in this load range the MCU works up to its maximum performance (highest

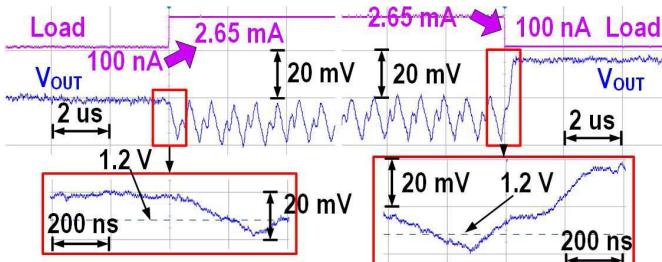


Fig. 20. Dynamic behavior of the output voltage at worst case load jumps.

TABLE II  
LINE REGULATION (%)

Temp	-40	27	95
Load			
2.65 mA	0.055	0.046	0.157
10 $\mu$ A	0.074	0.078	0.226

TABLE III  
LOAD REGULATION (%)

Temp	-40	27	95
V <sub>DD</sub>			
3.3 V	1.104	0.548	0.841
1.8 V	1.066	0.844	0.990

frequencies and switching activity), therefore, a more precise regulation is needed. These two parameters are not as critical as the ripple voltage but they are fundamental to characterize the regulation capability of the dc–dc. In low power mode, the regulated voltage only needs to guarantee data retention and minimum performances of the MCU. A higher efficiency in LPM is obtained at a cost of a poorer static accuracy and a reduced bandwidth.

Fig. 21 shows the output ripple voltage of the system versus load range at different input voltages. The ripple stays always within specification in active mode (smaller than 30 mV) and increases in low power mode since here the digital circuits can accept more supply voltage tolerance due to their low clock speed.

Fig. 23 shows the measured efficiency of the fabricated converter over the load range at different input voltages and room temperature. Fig. 22 shows the same kind of data for a low temperature ( $-40^{\circ}$ ) and Fig. 24 for a high temperature ( $+95^{\circ}$ ). The peak efficiency is 92.15% at 2.65-mA output current, room temperature, and 1.8-V supply voltage. The impact of the low power mode described in Section IV-E on the efficiency at light load can be observed. The solid lines show the efficiency when the system is in active mode only while the dashed line show the efficiency when low power mode is used for load currents smaller than 10  $\mu$ A.

The enhancement of the efficiency in low power mode is limited to moderate temperature. At high temperature, where leakage currents are maximal, the effect of the low power

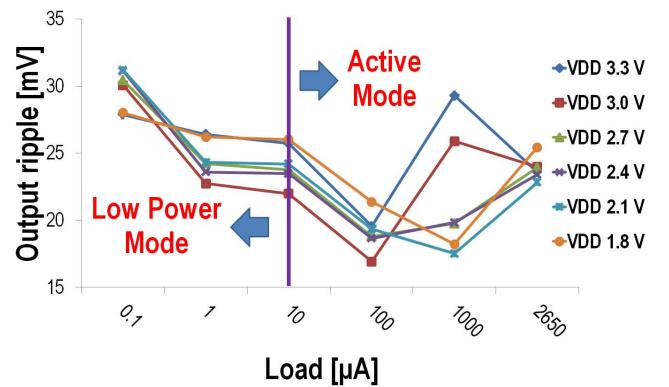
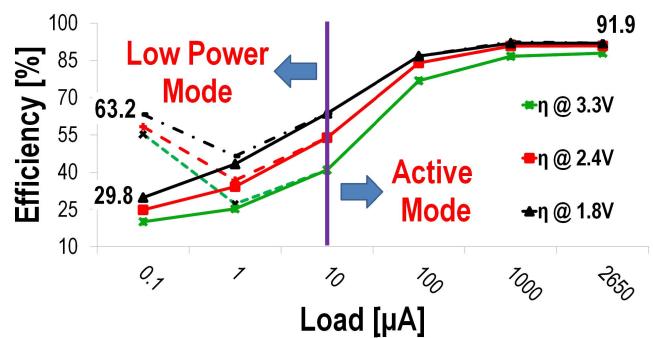
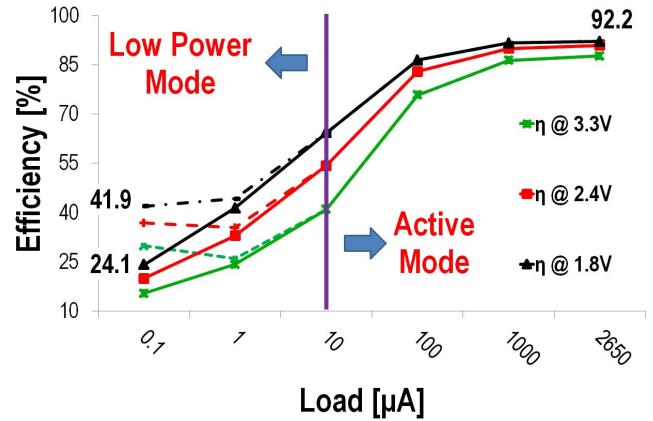


Fig. 21. Output ripple of the proposed converter.

Fig. 22. Efficiency of the proposed converter at the temperature of  $-40^{\circ}$ .Fig. 23. Efficiency of the proposed converter at the temperature of  $+27^{\circ}$ .

mode is negligible. The improvement is up to 17.8% at in the lowest range of the load at room temperature. In this test-chip, low power mode control is done via an external FSM that emulates the PMU of the MCU.

The key performance metrics of the proposed buck converter are compared with recent state-of the-art low power buck converters in Table IV.

For the benchmarking of our design, a *figure of merit* (FOM) =  $(C_{\text{OUT}} \cdot V_{\text{RIPPLE}})/I_{\text{LOAD}}$  is used. This FOM is characterized by the minimum capacitor  $C_{\text{OUT}}$  that is needed to minimize the wake-up energy, per maximum load current  $I_{\text{LOAD}}$  at a constant ripple voltage  $V_{\text{RIPPLE}}$  (fundamental for good regulation). The FOM is also an indirect measure for

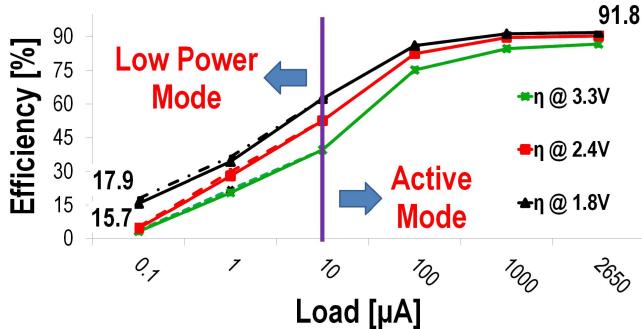
Fig. 24. Efficiency of the proposed converter at the temperature of  $+95^{\circ}\text{C}$ .

TABLE IV  
COMPARISON TO OTHER STATE-OF-THE-ART POWER CONVERTERS

	<b>DC-DC</b>				
	[23]	[10]	[22]	[24]	This work
Topology	Buck	Buck	Buck	Buck	Buck
Process geometry [nm]	40	500	n.a.	180	130
Area [ $\text{mm}^2$ ]	0.084	n.a.	n.a.	0.71	0.14
Wake-up energy [nJ] <sup>a</sup>	302.5	5000	250000	2250	80.64
Quiescent current [ $\mu\text{A}$ ] <sup>b</sup>	n.a.	n.a.	0.18 <sup>c</sup> -425	n.a.	0.44-12.32
Efficiency @ max load [%] <sup>d</sup>	(10mA) 86	(50mA) 76	(50mA) 91	(20mA) 88	(2.65mA) 92.15
Efficiency @ 200 $\mu\text{A}$ [%] <sup>d</sup>	80	n.a.	$\leq 89$	89	87.7
Voltage ripple [mV]	11	27	40	100	29
Output range [V]	0.3-0.55	0.5	0.8-5	1.5-1.6	1.2
Output cap. [nF]	1000	20000	10000	1000	56
Inductor [ $\mu\text{H}$ ]	220	1	2.2	4.7	18
FOM [ns]	1100	10800	8000	8000	613
	<b>LDO</b>				
	[25]	[26]	[27]	This work	
Topology	LDO	LDO	LDO	Buck	
Process geometry [nm]	65	28	350	130	
Area [ $\text{mm}^2$ ]	0.029	0.021	0.053	0.14	
Quiescent current [ $\mu\text{A}$ ]	12.5-216	110	4.04-164	0.44-12.32	
Max. $I_{\text{LOAD}}$ [ $\text{mA}$ ]	3.511	200	50	2.65	
Voltage ripple [mV]	40	120	6.6	29	
Output range [V]	0.45-0.95	0.9	0.9	1.2	
Output cap. [nF]	0.4	23.5	1000	56	
FOM <sup>2</sup> [pF]	1.1	1.72	0.59	0.23	

<sup>a</sup>only the recharge of  $C_{\text{OUT}}$  was taken into account ||| w/o cap re-charging current due to leakage.

<sup>b</sup>due to the large  $C_{\text{OUT}}$  the system can be switched off for long periods.

<sup>c</sup>FOM2 from [25] =  $(I_0/I_{\text{LOAD}})(V_{\text{RIPPLE}}/V_{\text{OUT}})C_{\text{OUT}}$ ; for both FOMs smaller value is better.

the wake-up time of the regulator. Our design achieved an FOM 1.8X better than prior art. As compared to the best counterpart [22], the quiescent current is only slightly higher. This is due to the higher regulation speed needed to react for current changes which in the proposed design are not compensated by a  $\sim 200$ X larger output capacitor. For the same reason [22] also has a  $\sim 200$  higher wake-up energy. The energy consumption of our proposed solution is clearly superior at system level. Table IV compares the performance of the proposed converter with recent state-of-the-art LDOs. LDOs are wake-up energy efficient, however, using a performance metric for low power LDOs (FOM from [25]), the presented dc-dc converter performs well. Note that as compared with LDOs, the proposed converter guarantees also better conversion efficiency in active mode even at the highest  $V_{\text{DD}}$ .

## VI. CONCLUSION

An integrated dc-dc converter for ULP and IoT applications has been presented. The proposed design is optimized for lowest energy at system level. In the context of ULP applications, the proposed design overcomes the limitations of standard dc-dc converters: it simultaneously meets the performance of well-known startup energy efficient converters, such as LDOs, in terms of wake-up energy savings and

it also presents the advantages of the switching converters over the linear regulators (e.g., high conversion efficiency even at large  $V_{\text{DD}}-V_{\text{OUT}}$ ). The proposed converter enables an unprecedented reduction in wake-up energy and startup delay without sacrificing best-in class efficiencies in active and standby mode. The peak conversion efficiency is 92.15% at 1.8 V  $V_{\text{DD}}$  with a load current of 2.65 mA.

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## REFERENCES

- G. Kortuem, F. Kawsar, V. Sundramoorthy, and D. Fitton, "Smart objects as building blocks for the Internet of Things," *IEEE Internet Comput.*, vol. 14, no. 1, pp. 44-51, Jan. 2010.
- MultiParameter BioSignal Monitor Design Guider*, document TIDU875, Texas Instruments, Jun. 2015.
- S. Paul *et al.*, "A sub- $\text{cm}^3$  energy-harvesting stacked wireless sensor node featuring a near-threshold voltage IA-32 microcontroller in 14-nm tri-gate CMOS for always-ON always-sensing applications," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 961-971, Apr. 2017.
- T. Fukuda *et al.*, "A 7ns-access-time 25  $\mu\text{W}/\text{MHz}$  128 kb SRAM for low-power fast wake-up MCU in 65 nm CMOS with 27 fA/b retention current," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 236-237.
- S. Hanson *et al.*, "Ultralow-voltage, minimum-energy CMOS," *IBM J. Res. Develop.*, vol. 50, nos. 4-5, pp. 469-490, 2006.
- R. G. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester, and T. Mudge, "Near-threshold computing: Reclaiming Moore's law through energy efficient integrated circuits," *Proc. IEEE*, vol. 98, no. 2, pp. 253-266, Feb. 2010.
- M. Steyaert, A. Sarafianos, N. Butzen, and E. D. Pelecijn, "Fully integrated power management: The missing link?" in *Proc. Eur. Conf. Circuit Theory Design (ECCTD)*, Sep. 2017, pp. 1-4.
- M. Lueders *et al.*, "Architectural and circuit design techniques for power management of ultra-low-power MCU systems," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 11, pp. 2287-2296, Nov. 2014.
- Implementing A Smoke Detector With The MSP430F2012*, document SLAA335, Texas Instruments, Oct. 2006.
- B. Sahai and G. A. Rincon-Mora, "An accurate, low-voltage, CMOS switching power supply with adaptive on-time pulse-frequency modulation (PFM) control," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 2, pp. 312-321, Feb. 2007.
- S.-H. Lee *et al.*, "A 0.518  $\text{mm}^2$  quasi-current-mode hysteretic buck DC-DC converter with 3  $\mu\text{s}$  load transient response in 0.35  $\mu\text{m}$  BCDMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 1-3.
- A. Baumann *et al.*, "A MCU platform with embedded FRAM achieving 350 nA current consumption in real-time clock mode with full state retention and 6.5  $\mu\text{s}$  system wakeup time," in *Proc. Symp. VLSI Circuits*, Jun. 2013, pp. C202-C203.
- F. Santoro *et al.*, "A 92.1% efficient DC-DC converter for ultra-low power microcontrollers with fast wake-up," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2017, pp. 1-4.
- T. M. Van Breussegem and M. S. J. Steyaert, "Monolithic capacitive DC-DC converter with single boundary-multiphase control and voltage domain stacking in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1715-1727, Jul. 2011.
- J. Jiang, W. H. Ki, and Y. Lu, "Digital 2-/3-phase switched-capacitor converter with ripple reduction and efficiency improvement," *IEEE J. Solid-State Circuits*, vol. 52, no. 7, pp. 1836-1848, Jul. 2017.
- R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. New York, NY, USA: Springer, 2001.
- F. Santoro, D. Schmitt-Landsiedel, N. Gibson, R. Kuhn, T. Tost, and R. Brederlow, "An ultra-low power, 2 mA Iout buck converter optimized for <50 mV ripple at a load cap of only 27 nF," in *Proc. 11th Conf. Ph.D. Res. Microelectron. Electron. (PRIME)*, Jun. 2015, pp. 208-211.
- F. Santoro, R. Brederlow, N. Gibson, and R. Kuhn, "Power transfer estimation," U.S. Patent 14,543,565, Jan. 10, 2017.
- V. Ivanov and I. Filanovsky, *Operational Amplifier Speed and Accuracy Improvement*. Dordrecht, The Netherlands: Springer, 2004.

- [20] M. Bazes, "Two novel fully complementary self-biased CMOS differential amplifiers," *IEEE J. Solid-State Circuits*, vol. 26, no. 2, pp. 165–168, Feb. 1991.
- [21] V. Ivanov, R. Brederlow, and J. Gerber, "An ultra low power bandgap operational at supply from 0.75 V," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1515–1523, Jul. 2012.
- [22] 50 mA/500 mA, High Efficiency, Ultralow Power Step-Down Regulator, document ADP5301, Analog Devices, Aug. 2015.
- [23] X. Zhang *et al.*, "A 0.6 V input CCM/DCM operating digital buck converter in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2377–2386, Nov. 2014.
- [24] C.-S. Wu, M. Takamiya, and T. Sakurai, "Buck converter with higher than 87% efficiency over 500 nA to 20 mA load current range for IoT sensor nodes by clocked hysteresis control," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2017, pp. 1–4.
- [25] D. Kim and M. Seok, "Fully integrated low-drop-out regulator based on event-driven pi control," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan. 2016, pp. 148–149.
- [26] Y.-J. Lee *et al.*, "A 200 mA digital low-drop-out regulator with coarse-fine dual loop in mobile application processors," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan. 2016, pp. 150–151.
- [27] Y.-H. Lam and W.-H. Ki, "A 0.9V 0.35  $\mu$ m adaptively biased CMOS LDO regulator with fast transient response," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2008, pp. 442–462.



**Francesco Santoro** (M'15) received the M.Sc. degree in electronic engineering from the Politecnico di Torino, Turin, Italy, in 2012. He is currently pursuing the Ph.D. degree with the Technical University of Munich, Munich, Germany.

His research focused on power management for ultra-low power systems and he worked in cooperation with Texas Instruments Deutschland GmbH, Freising, Germany. In 2016, he joined Infineon Technologies Austria AG, Villach, Austria, as an Analog-Mixed-Signal Designer. His current research interests include power management design for low power systems, for automotive products and data converters.



**Rüdiger Kuhn** received the Dipl.-Ing. degree in electrical engineering from the Technische Universität Chemnitz, Germany, in 1996.

He joined the Interuniversity Microelectronics Center (IMEC), Leuven, Belgium, in 1996, where he worked on BiCMOS technology development and device optimization. Since 2000, he has been with Texas Instruments Deutschland GmbH, Freising, Germany, as an Analog Design Engineer. His current research interests include the development of analog IP for microcontrollers, covering power management, clocking solutions, and data converters.



**Neil Gibson** received the B.Sc. degree (Hons.) in electronics from the University of Dundee, Dundee, U.K., in 1982.

Since 1982, he has held a variety of positions in research and development organizations. He is currently with Texas Instruments Deutschland GmbH, Freising, Germany. He holds over 20 patents in the area of power conversion and op-amp design.



**Nicola Rasera** received the B.Sc. degree in information engineering and the M.Sc. degree in electronic engineering from the University of Padua, Padua, Italy, in 2012 and 2014, respectively.

He was with Texas Instruments Deutschland GmbH, Freising, Germany, from November 2013 to May 2014, where he worked on his master's thesis, developing an ultra-low power predictive  $T_{ON}$  and  $T_{OFF}$  circuit for the control of an innovative Buck converter. He was with Texas Instruments Deutschland GmbH from 2014 to 2017, developing low

power inverting buck-boost converters for the biasing of LCD and OLED displays.



**Thomas Tost** was an Associate Engineer at Siemens Technik Akademie, Munich, Germany, in 2001. Since 2001, he has been a Layout Engineer with Texas Instruments Deutschland GmbH, Freising, Germany, developing analog IP layouts and custom mixed-signal full chip layouts for a microcontroller family. Since 2014, he also attends an extra-occupational course of studies in electrical engineering at FOM Hochschule Hochschulzentrum München, in addition to his profession.



**Helmut Graeb** (M'02–SM'03–F'14) received the Dipl.-Ing., Dr.-Ing., and Habilitation degrees in electrical engineering from the Technical University of Munich (TUM), Munich, Germany, in 1986, 1993, and 2008, respectively.

Since 1987, he has been with the Institute for Electronic Design Automation, TUM, where he has been the Head of a research group since 1993. His current research interests include design automation for analog and mixed-signal.

Dr. Graeb is a co-founder of MunEDA GmbH, Munich.



**Bernhard Wicht** (M'01–SM'14) received the Dipl.-Ing. degree in electrical engineering from the Technische Universität Dresden, Germany, in 1996, and the Ph.D. degree from the Technical University of Munich, Germany, in 2002.

From 2003 to 2010, he was with the Mixed-Signal Automotive Business Unit, Texas Instruments Deutschland GmbH, Freising, Germany, responsible for the design of automotive power management ICs. In 2010, he became a Full Professor for integrated circuit design and a member of the Robert Bosch Center for Power Electronics at Reutlingen University, Reutlingen, Germany. Since 2017, he has been heading the Chair of Mixed-Signal IC Design at Leibniz Universität Hannover, Germany.



**Ralf Brederlow** started his career at the Corporate Research of Infineon Technologies Austria AG, as a Designer and later Technical Project Manager in 1999, working on CMOS process related design for manufacturing, security aspects of MCUs, and sensor systems applications. In 2006, he joined Texas Instruments (TI) Deutschland GmbH, Freising, Germany, responsible for the development of analog, digital, and memory peripherals for TI's ultra-low-power microcontroller product family and for the definition and development of the technology

and circuits for TI's ultra-low-power microcontrollers. In 2015, he joined Kilby Labs to start a branch of TI's research division at the Freising site. He holds 32 patents and has published 64 papers.

Dr. Brederlow was the General Chair of the IEEE International Electron Devices Meeting (IEDM) in 2008, and from 2013 to 2014 the Chair of the European Solid-State Device Research Conference/European Solid-State Circuits Conference (ESSDERC/ESSCIRC) Steering Committee.