A 1.08-nW/kHz 13.2-ppm/°C Self-Biased Timer Using Temperature-Insensitive Resistive Current

Jaehong Jung, *Member, IEEE*, Ik-Hwan Kim, *Member, IEEE*, Seong-Jin Kim, *Member, IEEE*, Yoonmyung Lee, *Member, IEEE*, and Jung-Hoon Chun, *Member, IEEE*

***Abstract*— This paper proposes a 32.7 kHz self-biased wake-up timer using temperature-insensitive resistive current. A dual-loop structure with supply-regulation loop and frequency-locked loop determines the regulated voltages at both ends of a temperature-compensated resistor and cancels out the amplifier offset voltages, thus generating temperature-insensitive resistive current for the switched capacitor. Moreover, a self-biasing scheme in low-power design reduces the power variation across the temperature range and eliminates the necessity of a sub-μA reference current generator. The proposed timer with its start-up circuit generates <12 ms lock time, which is 20 times less than what obtained without a start-up circuit, and exhibits a long-term frequency stability of 10 ppm and a temperature coefficient of 13.2 ppm/°C with an energy efficiency of 1.08 nW/kHz.**

***Index Terms*— Allan deviation, low power, oscillators, RC-time constant, temperature sensitivity, wake-up timer.**

I. Introduction

TO MINIMIZE the power consumption during the sleep mode in the sensing platforms of the wireless sensor network (WSN) applications and guarantee reliable cross-communication, fully-integrated wake-up timers are required with extremely low power consumption and excellent long-term frequency stability against the temperature and supply variation. Compared with other on-chip oscillators, an RC-time constant-based relaxation oscillator (RCxO) has been generally used as an on-chip wake-up timer for its superior frequency stability and compact size. The frequency-locked loop (FLL)-based RCxO, as described in [1], significantly decreases the power consumption by replacing a power-hungry continuous comparator in the comparator-based RCxOs [2], [3] with a low-power amplifier. Although the comparator is dynamically controlled by the sub-duty-cycle technique in [4], variations of the comparator and buffer delays still degrade the frequency stability against the process, voltage, and temperature (PVT) variation. In the current-reusing scheme of [5], power efficiency is further improved by placing a switched resistor and a switched capacitor. However, since the switched resistor is directly connected to supply voltage, it is susceptible to the supply noise. Furthermore, the switched capacitor-based replica bias generator that replaces the large sub-μA reference current generator still requires an additional area for the replica switched capacitor circuit.

To address these challenges, a 32.7 kHz self-biased wake-up timer with a supply-regulation loop (SRL) and an FLL is proposed in this paper. A dual-loop structure internally generates the temperature-insensitive resistive current. The proposed timer consumes only 35.4 nW at 32.7 kHz with a 13.2 ppm/°C temperature coefficient (TC) and a 0.44 %/V stability, and exhibits long-term stability of <10 ppm. The remainder of this paper is organized as follows. Section II describes the architecture of the proposed timer and its operation. Section III presents the detailed circuit diagram and overall transient characteristics. Next, Section IV discusses the measurement results for the multiple samples, and finally this paper is concluded in Section V.

II. Overall Architecture

Fig. 1 exhibits the architecture of the proposed self-biased timer with a SRL and an FLL. The timer consists of a tunable resistor (R_{TC}), a tunable switched capacitor (C_{SW}), a self-biasing circuit with its start-up circuit, a voltage-controlled oscillator (VCO), a reference generator, and two amplifiers. A temperature-compensated resistor (R_{TC}), which consists of a 4-bit tunable p-type non-silicided poly resistor and a 4-bit tunable n-type silicided poly resistor for TC trimming, and a switched capacitor (C_{SW}) are connected in series to minimize the power consumption and avoid current mismatch without an additional current-chopping technique in parallel structure [1], [2]. V_{D1} and V_{D2} at both ends of R_{TC} are regulated to V_{R1} and V_{R2} by the SRL and FLL, respectively. The mutual interference of the two loops is negligible as the bandwidth of the SRL is 8 times higher than that of the FLL. Moreover, as the SRL shields V_{D1} and V_{D2} from the supply noise, it significantly improves noise immunity and frequency stability of the timer. The current (I_R) to charge C_{SW} is then

Manuscript received November 24, 2017; revised February 7, 2018; accepted March 28, 2018. Date of publication May 28, 2018; date of current version July 20, 2018. This paper was approved by Associate Editor Azita Emami. This work was supported in part by the Basic Science Research Program through the National Research Foundation of Korea under Grant 2016R1D1A1B04933413 and in part by the Ministry of Trade, Industry, and Energy under Project 10008040. *(Corresponding author: Jung-Hoon Chun.)*

J. Jung and I.-H. Kim were with the College of Information and Communication Engineering, Sungkyunkwan University, Suwon 16419, South Korea. They are now with Samsung Electronics, Hwaseong 18448, South Korea (e-mail: jungjae00@skku.edu).

S.-J. Kim is with the Department of Electrical and Computer Engineering, Ulsan National Institute of Science and Technology (UNIST), Ulsan 44610, South Korea.

Y. Lee and J.-H. Chun are with the College of Information and Communication Engineering, Sungkyunkwan University, Suwon 16419, South Korea (e-mail: jhchun@skku.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2018.2824307

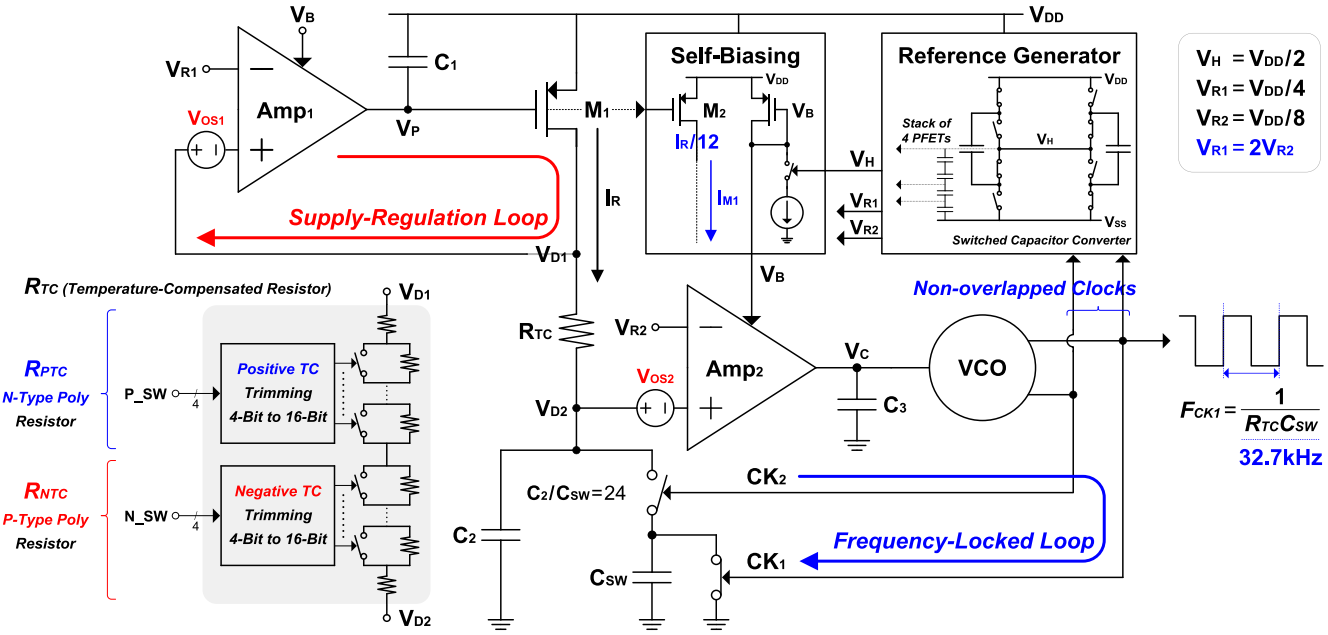


Fig. 1. Architecture of the proposed 32.7 kHz self-biased timer using temperature-insensitive resistive current (I_R) with a SRL and an FLL.

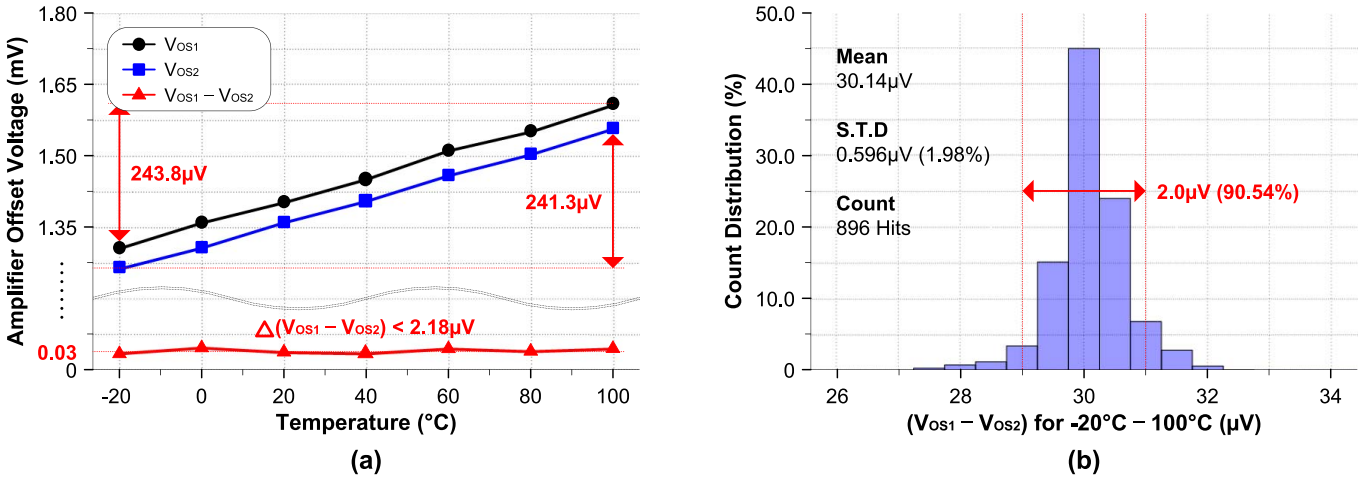


Fig. 2. Monte-Carlo simulation results for (a) amplifier offset voltage variations versus temperature and (b) histogram about ($V_{OS1} - V_{OS2}$).

derived as

$$I_R = \frac{(V_{R1} + V_{OS1}) - (V_{R2} + V_{OS2})}{R_{TC}} \quad (1)$$

where V_{OS1} and V_{OS2} are the amplifier offset voltages of Amp_1 and Amp_2, respectively. The Monte-Carlo simulation results in Fig. 2(a) exhibit that the temperature variations of the amplifier offset voltages are mostly cancelled out by using the identically sized amplifiers operating at similar input bias voltages. In this Monte-Carlo simulation, the total number of counts is 896 hits, and the number of counts at each temperature is 128 hits. Each data point in Fig. 2(a) exhibits the average result at each temperature. It is clearly shown that ($V_{OS1} - V_{OS2}$) is almost independent of the temperature. Using the same simulation results, we also plotted a histogram about ($V_{OS1} - V_{OS2}$), as shown in Fig. 2(b). The drift of ($V_{OS1} - V_{OS2}$) across the temperature range from −20 to 100 °C is only less than 2.18 μV, verifying an effective offset cancellation. Furthermore, as ($V_{OS1} - V_{OS2}$) is only less than 0.02 % of ($V_{R1} - V_{R2}$), the current (I_R) can be briefly expressed as follows:

$$I_R = \frac{(V_{R1} - V_{R2}) + (V_{OS1} - V_{OS2})}{R_{TC}} = \frac{V_{R1} - V_{R2}}{R_{TC}} \quad (2)$$

That is, the amplifier offset voltage, V_{OS1} and V_{OS2}, and their temperature dependencies have minimal impacts on the generation of resistive current. Thus, the optimized TC of the resistor (R_{TC}) and amplifier offset cancellation significantly reduce the temperature sensitivity of the resistive current, I_R.

Because the periodic switching operation of C_{SW} is governed by I_R, the output frequency (F_{CK1}) of the timer is derived as

$$I_R \frac{1}{F_{CK1}} = C_{SW}(V_{R2} + V_{OS2}) = C_{SW} V_{R2} \quad (3)$$

$$F_{CK1} = \frac{I_R}{C_{SW} V_{R2}} = \frac{(V_{R1} - V_{R2})}{V_{R2} R_{TC} C_{SW}} = \frac{1}{R_{TC} C_{SW}} \quad (4)$$

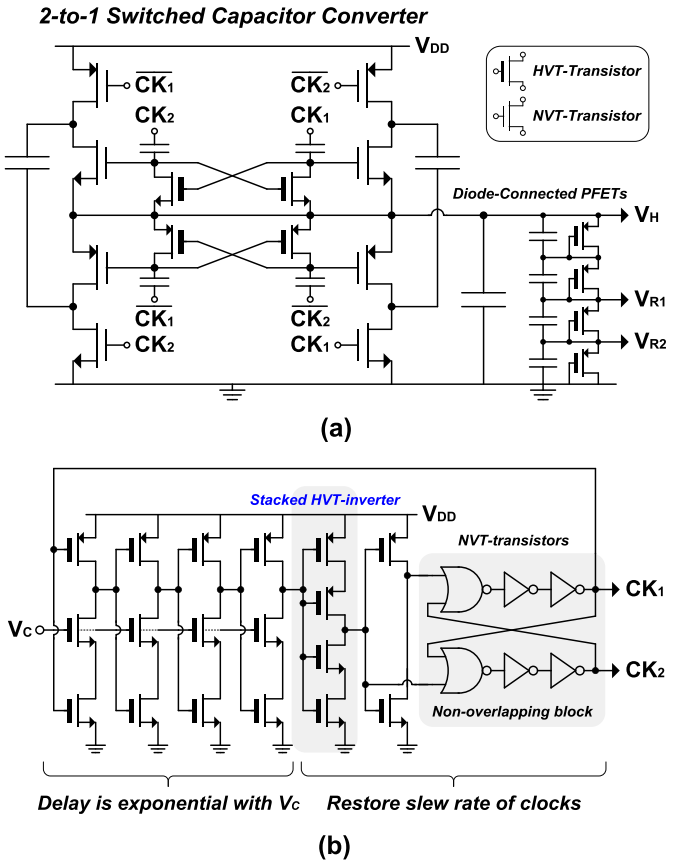


Fig. 3. Circuit diagrams of (a) reference generator and (b) VCO.

The reference voltages, V_{R1} and V_{R2}, of the SRL and FLL are generated by dividing the supply voltage (V_{DD}) in the reference generator, and V_{R1} is $2V_{R2}$. Because we use the nominal supply voltage (V_{DD}) of 1.2 V, the reference voltages, V_{R1} and V_{R2}, are determined as 300 and 150 mV, respectively. In (3), the offset voltage of Amp_2 can be ignored as it is considerably smaller than the reference voltage of Amp_2 ($V_{OS2} < 0.01V_{R2}$). Actually, since V_{OS2} varies linearly across the temperature range from −20 to 100 °C, as shown in Fig. 2(a), it can be easily compensated by trimming the TC of R_{TC}, as in [1]. Combining (2) and (3), and using $V_{R1} = 2V_{R2}$, we can derive the simplified expression for the output clock frequency, F_{CK1}, as in (4), which has only R_{TC} and C_{SW}.

III. Circuit Details and Transient Characteristics

In design of RCxOs, there is a key trade-off between power consumption and area. That is, as the resistor's size determining the RC-time constant is increased, the power consumption can be reduced. However, with the excessively large resistor's size, the junction and sub-threshold leakage current of the transistors can be compatible with the resistive current, especially at high temperature; thus, the temperature characteristics are seriously degraded. Considering these trade-offs, the resistive current (I_R) and the temperature-compensated resistor (R_{TC}) are determined as 19.2 nA and 7.8 MΩ, respectively. The capacitor (C_{SW}) is set to 3.9 pF to achieve the target frequency of 32.7 kHz.

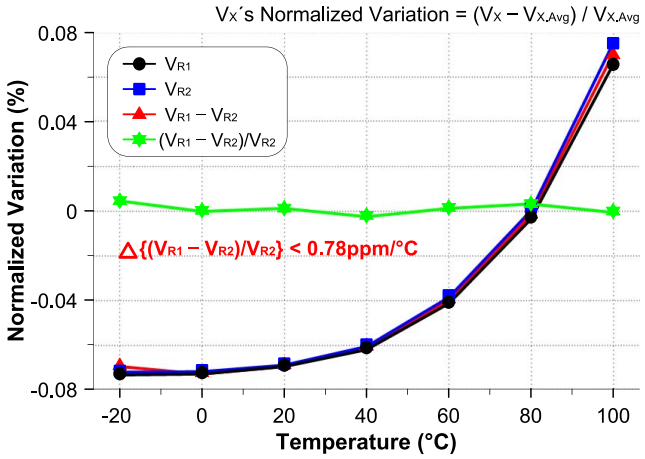


Fig. 4. Simulation results for variation of the reference voltages.

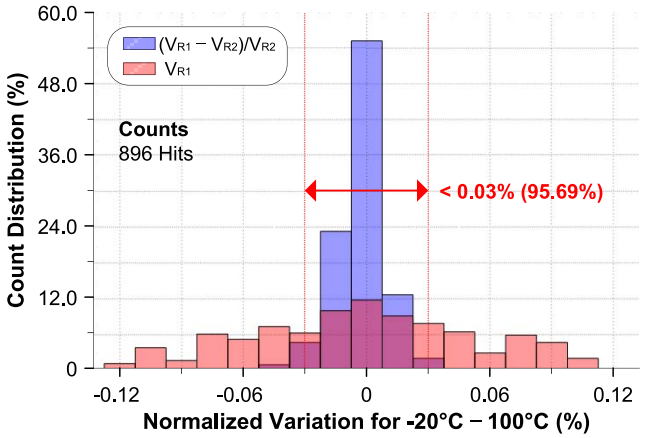


Fig. 5. Monte-Carlo simulation results about $(V_{R1} - V_{R2})/V_{R2}$ and V_{R1}.

A. Reference Generator

The reference generator in Fig. 3(a) is composed of a 2-to-1 switched capacitor converter [6] and a stack of diode-connected PFETs. To minimize the switching overhead in the VCO, the 2-to-1 switched capacitor converter is used only in the first stage and it generates $V_H (= V_{DD}/2)$ with steps aligned with the output clocks of the VCO. Next, V_{R1} and V_{R2} are generated by dividing V_H with the stack. As shown in Fig. 4, a ratio of $(V_{R1} - V_{R2})$ and V_{R2} in (4) varies with the TC less than 0.78 ppm/°C across the temperature range due to the equivalent temperature dependencies of V_{R1} and V_{R2}. We also ran Monte Carlo simulation for seven discrete temperature numbers from −20 to 100 °C. The number of counts at each temperature is 128 hits, and the total number of counts is 896 hits. The Monte-Carlo simulation results in Fig. 5 show that the ratio metric design, $(V_{R1} - V_{R2})/V_{R2}$, can significantly reduce the impacts of random mismatches in the reference generator. Therefore, the proposed timer can achieve the excellent temperature sensitivity. Moreover, the ratio metric design inherently suppresses V_{DD}-dependence; thus, improving the line sensitivity.

B. Voltage-Controlled Oscillator (VCO)

Fig. 3(b) shows the VCO with the non-overlapping block. The control voltage, V_C, determines the output frequency

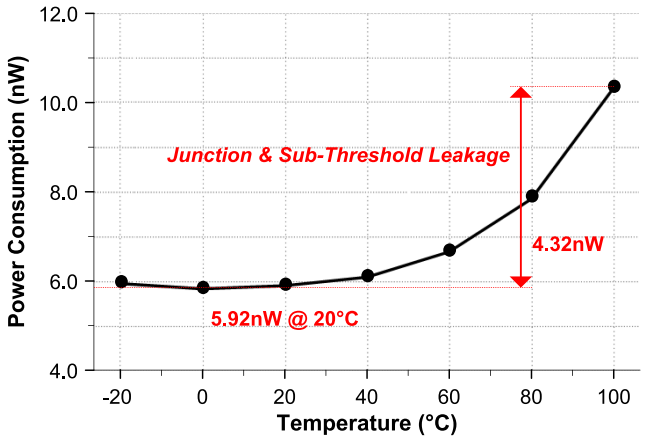


Fig. 6. Simulation results for the power consumption of the VCO.

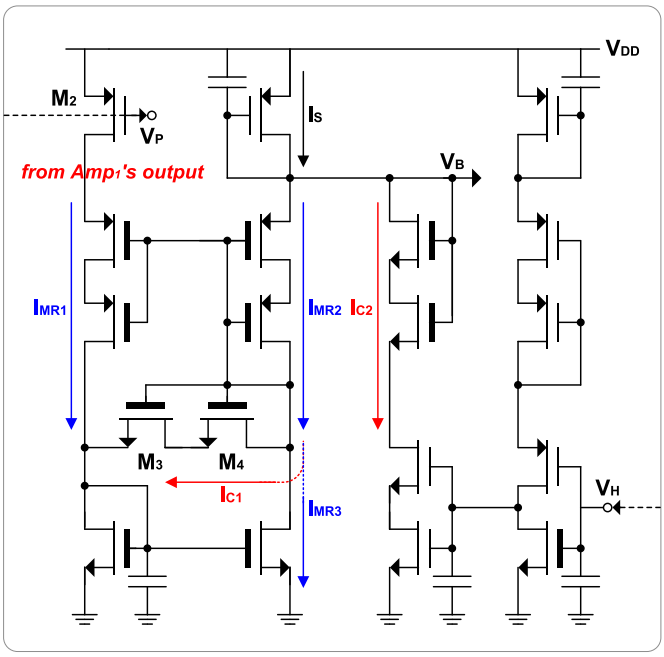


Fig. 7. Circuit diagram of a self-biasing scheme with its start-up.

through the first four stages. Furthermore, as the delays in these stages are exponential with V_C, the VCO generates wide frequency ranges from kHz to MHz with a VCO gain of 0.82 MHz/V. A high-V_T stacked inverter is then used to reduce the short-circuit current, as in [1]. Finally, the nominal-V_T NOR-based non-overlapping block gradually restores slew-rate of the clocks and generates the non-overlapped differential clocks, CK_1 and CK_2. The simulation results in Fig. 6 show that the power consumption of the VCO only varies by about 4.32 nW across the temperature range from −20 to 100 °C. However, this is only less than 16 % of the overall power consumption of the proposed timer.

C. Self-Biasing Scheme with a Start-Up Circuit

Fig. 7 shows the self-biasing scheme with its start-up circuit to minimize the area, power, and design complexity. The self-biasing scheme in this design aims to mirror the temperature-insensitive resistive current (I_R) to produce the bias current (I_S) for the amplifiers (Amp_1 and Amp_2). Each

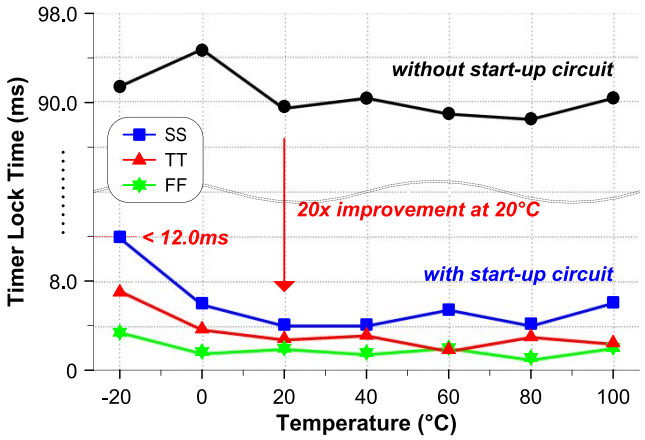


Fig. 8. Simulation results for the lock time of the proposed timer.

mirroring current in Fig. 7 is expressed as follows:

$$I_{MR2} = I_{MR3} + I_{C1},\ I_{MR3} = I_{MR1} + I_{C1}. \tag{5}$$

If there is no start-up circuit in the initial operation, I_R and I_S are very small due to the absence of V_{R1} and V_{R2} in (2). In such a case, the bandwidth of the amplifiers in the SRL and FLL is significantly limited, causing the excessively long lock time of the timer (Fig. 8).

To address these issues, the self-biasing output voltage (V_B), which is directly connected to the gates of the mirroring PFETs inside the amplifiers, is pulled down by a start-up circuit. As V_H from the 2-to-1 switched capacitor converter is initially held to the ground potential (V_{SS}), the activated start-up circuit generates the temporary and deterministic bias current, I_S, regardless of I_{MR1}. As the amplifiers are properly biased, and the control voltage (V_C) increases high enough to activate the VCO, the 2-to-1 switched capacitor converter gradually elevates V_H to half of the supply voltage (V_{DD}), and this high V_H ends the start-up circuit, thus, resulting in the transition from the start-up mode to the self-biasing mode.

During this transition, the M_3 and M_4 NFETs provide a current path to compensate the current mismatch between I_{MR1} and I_{MR2}. Here, I_{MR2} is not completely governed by I_{MR1} and is distributed to I_{MR3} and I_{C1}. However, as the SRL and FLL steadily approach the locking condition, I_{MR1} increases and I_{C1} decreases accordingly. The self-biasing circuit eventually enters a steady state. Therefore, I_{C1} and I_{C2} are less than 8 pA, and $I_{MR1} = I_{MR2}$, completing the self-biasing operation in the proposed timer, as described in the following equation:

$$I_R/12 = I_{MR1} = I_{MR2} = I_S. \tag{6}$$

Note that the self-biasing scheme using I_R reduces the power variation across the wide temperature range. Furthermore, the start-up circuit ensures a reliable initial operation of the timer and yields a 20-fold improvement of the lock time at the room temperature, as shown in Fig. 8.

D. Transient Characteristics

The transient characteristics of the proposed timer are shown in Fig. 9. First, the VCO is activated by the start-up operation, then, the reference voltages, V_{R1} and V_{R2}, of the SRL and FLL are generated with the steps aligned with the output clock

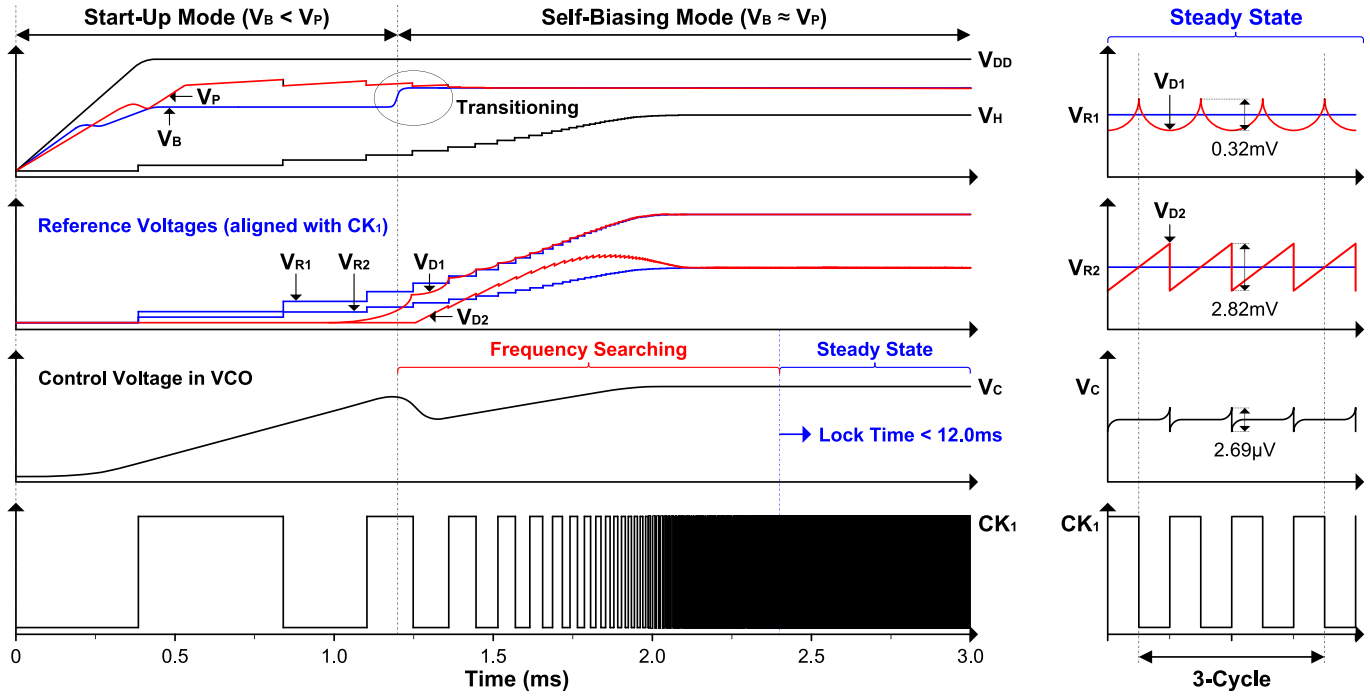


Fig. 9. Transient characteristics according to the start-up and the self-biasing modes, and details of a steady-state operation.

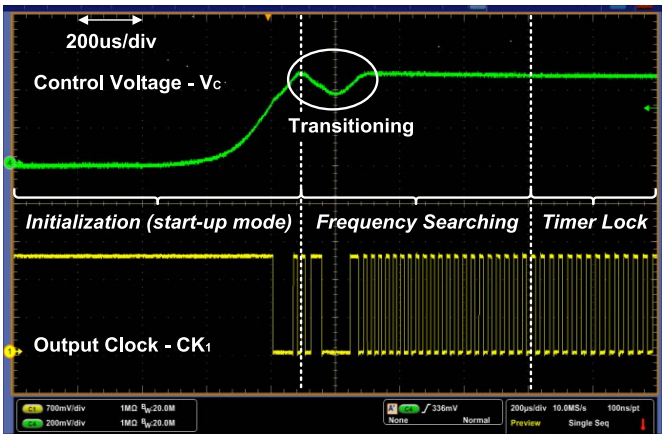


Fig. 10. Measurement results for the transient characteristics.

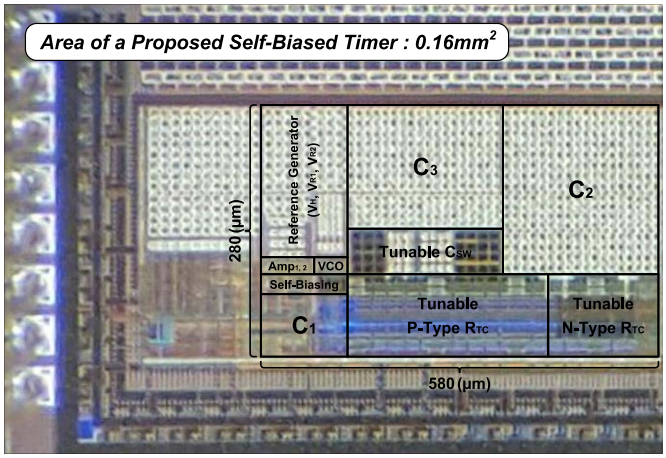


Fig. 11. Die micrograph.

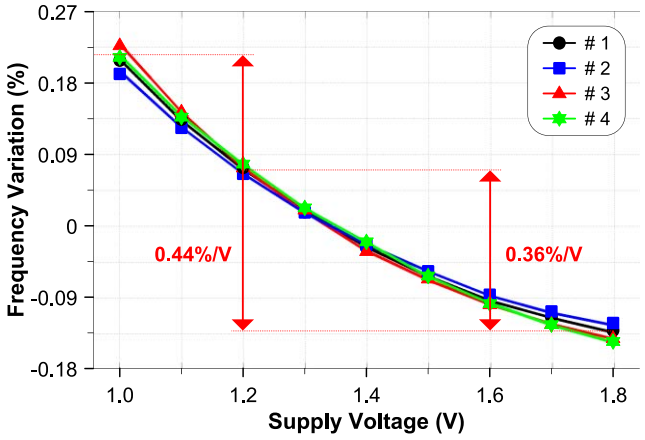


Fig. 12. Measurement results for line sensitivity.

of the VCO (CK_1). As the elevated V_H causes the transition, V_B first increases with a distinct step and then slowly converges to the final value, V_P. In the steady state, V_C and the frequency of CK_1 are settled. The measured transient responses in Fig. 10 exhibit that the proposed timer is settled within 2 ms (48 cycles) at room temperature. Furthermore, the waveform of V_C shows an over-damped behavior and verifies the loop stability of the SRL and FLL.

As shown in Fig. 9, the switching nature of the timer causes the periodic ripples on V_{D1} and V_{D2}. However, these are effectively suppressed by the low-pass filters on V_C and V_P, which are composed of C_1, C_3, and the high output impedances of the amplifiers in Fig. 1. Comparing with the ripples of the control voltage (80 μV) in [5], the ripples on V_C are nearly negligible; thus, the long-term frequency stability of the proposed timer is significantly improved.

IV. Measurement Results

In this paper, a 32.7 kHz ultra-low-power self-biased timer is proposed and fabricated using a 180 nm CMOS

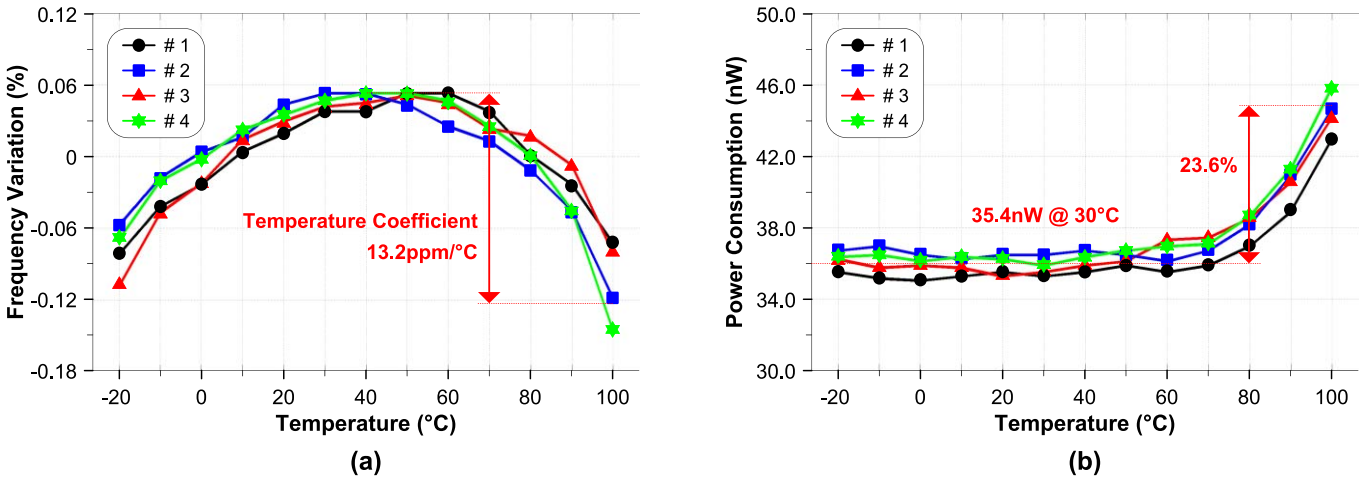


Fig. 13. Measurement results for (a) temperature sensitivity and (b) power consumption across the temperature range from −20 to 100 °C.

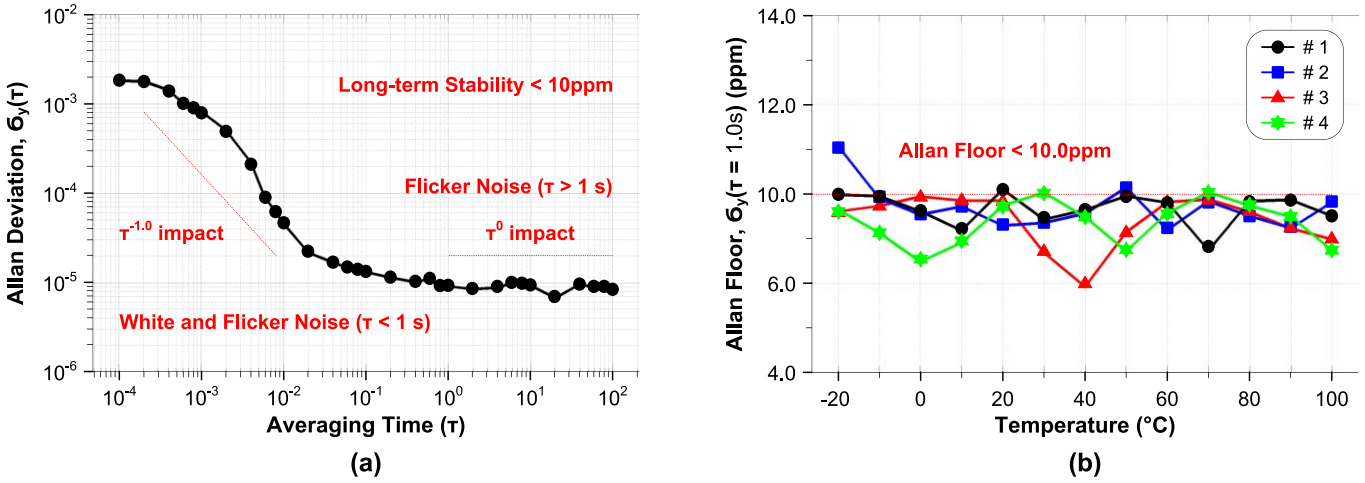


Fig. 14. Measurement results for (a) long-term Allan deviation and (b) Allan floor at $\tau = 1$ s across the temperature range from −20 to 100 °C.

process technology with an active area of 0.16 mm^2. A die micrograph is shown in Fig. 11. The output frequency and TC of the timer are controlled by the following procedure.

1) First, the nominal frequency of the proposed timer is coarsely controlled by trimming only the switched capacitor, C_{SW}.
2) Next, we trim the n-type poly resistor, R_{PTC}, to finely adjust the output clock frequency close to 32.7 kHz.
3) Finally, by trimming the p-type poly resistor, R_{NTC}, the TC of the proposed timer can be optimized through the two-point (20 and 60 °C) calibration procedure. The output clock frequency of the proposed timer is tunable from 23.1 to 54.2 kHz, which is achieved by only trimming C_{SW}.

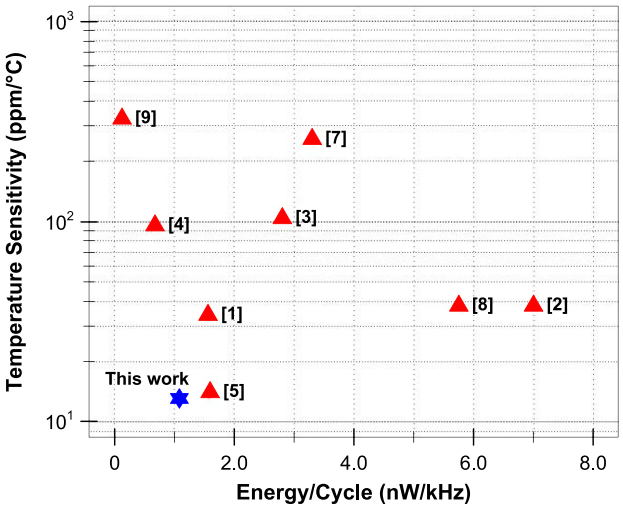
As shown in Fig. 12, the measured line sensitivity is 0.44 %/V for the wide supply voltages from 1 to 1.8 V for four sample-chips. The temperature sensitivity and the power consumption of the timer are measured from −20 to 100 °C under the nominal supply voltage of 1.2 V. We achieve the best and worst TCs of 11.2 and 16.4 ppm/°C in chips 1 and 4, respectively (Fig. 13(a)), and the average is 13.2 ppm/°C. At room temperature (30 °C), the power consumption of the proposed timer is only 35.4 nW at 32.7 kHz, translated to an excellent energy efficiency of 1.08 nW/kHz. Furthermore, the power consumption across the wide temperature range in Fig. 13(b) varies only by <23.6 % owing to the self-biasing scheme.

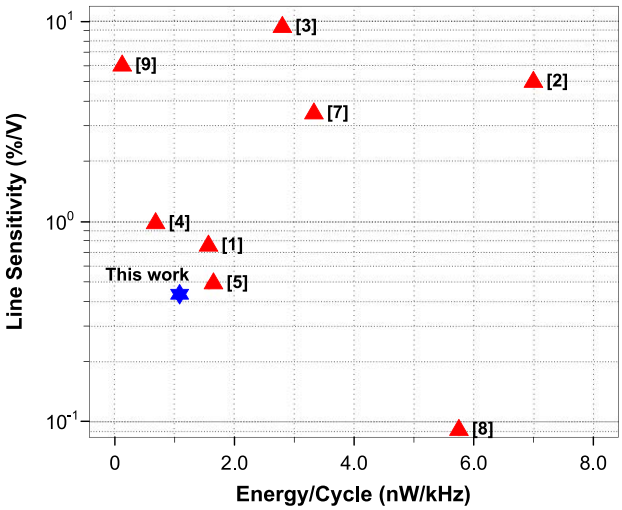
The long-term Allan deviation for chip 1 is shown in Fig. 14(a). Allan deviation is the indicator for the noise immunity and the long-term frequency stability of the proposed timer. For the short averaging time ($\tau < 1$ s), the white noise and flicker noise processes (τ^{-1}) determine the Allan deviation, as described in [2]. If the averaging time is longer than 1 s ($\tau > 1$ s), the Allan deviation is limited by the flicker noise process (τ^0). The measured Allan floor shows that the long-term frequency stability is only less than 10 ppm. Moreover, the Allan deviation at $\tau = 1$ s in Fig. 14(b) also exhibits that the Allan floors across the temperature range from −20 to 100 °C are less than 10 ppm. Fig. 15 shows the overall power breakdown of the proposed timer at the room temperature (30 °C).

Table I compares the proposed wake-up timer with the state-of-the-art ultra-low-power timers in the kHz range. This paper accomplishes the lowest temperature sensitivity, 13.2 ppm/°C,

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART TIMERS





	This work	[1]	[2]	[3]	[4]	[5]	[7]	[8]	[9]
Process (nm)	180	180	65	90	65	180	350	65	180
Frequency (kHz)	32.7	70.4	18.5	100	1350	3	3.3	33	122
Power (nW)	35.4	110	130	280	920	4.7	11	190	14.4
Line Sensitivity (%/V)	0.44	0.75	< 5	9.4	0.98	0.48	3.5	0.09	6
TC[1] (ppm/°C)	13.2	34.3	38.5	104.6	96.0	13.8	260	38.2	327
Temperature Range (°C)	-20 - 100	-40 - 80	-40 - 90	-40 - 90	0 - 145	-25 - 85	-20 - 80	-20 - 90	-20 - 100
Long-term Stability (ppm)	< 10	< 7	< 20	< 10	-	< 63	-	< 4	< 40
Area (mm^2)	0.16	0.26	0.032	0.12	0.005	0.5	0.1	0.015	0.03
Energy/Cycle (nW/kHz)	1.08	1.56	7.0	2.8	0.68	1.56	3.33	5.76	0.12

[1]Temperature Coefficient (TC) = $(Freq._{Max} - Freq._{Min})/\{Freq._{Avg} \times (Temp._{Max} - Temp._{Min})\} \times 10^6$

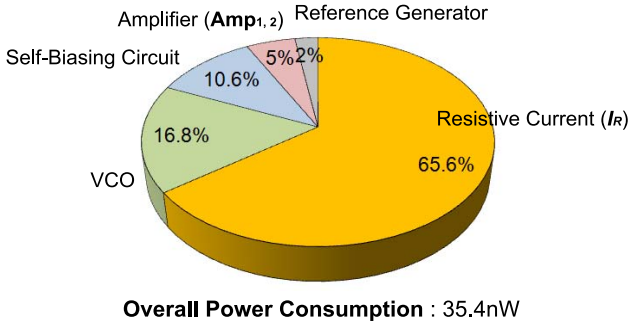


Fig. 15. Power breakdown of the proposed timer at room temperature.

among the previous works. Furthermore, in terms of a trade-off between the temperature sensitivity and energy efficiency, the proposed timer exhibits the best reported performance. The line sensitivity and long-term stability are also excellent.

V. CONCLUSION

A 32.7 kHz ultra-low-power self-biased timer is proposed to provide an accurate wake-up signal and minimize the power of the sleep mode in the sensing platforms. The proposed timer in this paper internally generates temperature-insensitive resistive current through the dual-loop structure and achieves frequency stability of 13.2 ppm/°C and 0.44 %/V with a superior energy efficiency of 1.08 nW/kHz. Moreover, the self-biasing scheme, which is only composed of the transistors, minimizes the power variation across the temperature range and reduces an overhead in the low-power design process. Finally, the timer utilizing its start-up circuit improves the lock time by 20-fold with a reliable initial operation.

REFERENCES

[1] M. Choi, T. Jang, S. Bang, Y. Shi, D. Blaauw, and D. Sylvester, "A 110 nW resistive frequency locked on-chip oscillator with 34.3 ppm/°C temperature stability for system-on-chip designs," *IEEE J. Solid-State Circuits*, vol. 51, no. 9, pp. 2106–2118, Sep. 2016.

[2] A. Paidimarri, D. Griffith, A. Wang, G. Burra, and A. P. Chandrakasan, "An RC oscillator with comparator offset cancellation," *IEEE J. Solid-State Circuits*, vol. 51, no. 8, pp. 1866–1877, Aug. 2016.

[3] K.-J. Hsiao, "A 32.4 ppm/°C 3.2-1.6V self-chopped relaxation oscillator with adaptive supply generation," in *Proc. Symp. VLSI Circuits (VLSIC)*, Jun. 2012, pp. 14–15.

[4] A. Savanth, J. Myers, A. Weddell, D. Flynn, and B. Al-Hashimi, "A 0.68 nW/kHz supply-independent relaxation oscillator with ±0.49%/V and 96 ppm/°C stability," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 96–97.

[5] T. Jang, M. Choi, S. Jeong, S. Bang, D. Sylvester, and D. Blaauw, "A 4.7 nW 13.8 ppm/°C self-biased wakeup timer using a switched-resistor scheme," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 102–103.

[6] S. Bang, A. Wang, B. Giridhar, D. Blaauw, and D. Sylvester, "A fully integrated successive-approximation switched-capacitor DC-DC converter with 31 mV output voltage resolution," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 370–371.
[7] U. Denier, "Analysis and design of an ultralow-power CMOS relaxation oscillator," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 1973–1982, Aug. 2010.
[8] D. Griffith, P. T. Røine, J. Murdock, R. Smith, "A 190 nW 33 kHz RC oscillator with ±0.21% temperature stability and 4ppm long-term stability," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 300–301.
[9] S. Dai and J. K. Rosenstein, "A 14.4 nW 122 KHz dual-phase current-mode relaxation oscillator for near-zero-power sensors," in *Proc. IEEE Custom Integr. Circuits (CICC)*, Sep. 2015, pp. 1–4.
[10] K. Choe, O. D. Bernal, D. Nuttman, and M. Je, "A precision relaxation oscillator with a self-clocked offset-cancellation scheme for implantable biomedical SoCs," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2009, pp. 402–403.
[11] K. Tsubaki, T. Hirose, N. Kuroki, and M. Numa, "A 32.55-kHz, 472-nW, 120 ppm/°C, fully on-chip, variation tolerant CMOS relaxation oscillator for a real-time clock application," in *Proc. IEEE Eur. Solid-State Circuit Conf. (ESSCIRC)*, Sep. 2013, pp. 315–318.
[12] T. Tokairin *et al.*, "A 280 nW, 100kHz, 1-cycle start-up time, on-chip CMOS relaxation oscillator employing a feedforward period control scheme," in *Proc. IEEE Symp. VLSI Circuits (VLSIC)*, Jun. 2012, pp. 16–17.
[13] A. Shrivastava, D. A. Kamakshi, and B. H. Calhoun, "A 1.5 nW 32.768 kHz XTAL oscillator operational from a 0.3 V supply," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 686–696, Mar. 2016.
[14] Y. Lee, B. Giridhar, Z. Foo, D. Sylvester, and D. Blaauw, "A 660 pW multi-stage temperature-compensated timer for ultra-low-power wireless sensor node synchronization," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2011, pp. 46–48.
[15] J. Lee and S. Cho, "A 10 MHz 80 μW 67 ppm/°C CMOS reference clock oscillator with a temperature compensated feedback loop in 0.18 μm CMOS," in *Proc. IEEE Symp. VLSI Circuits (VLSIC)*, Jun. 2009, pp. 226–227.
[16] A. Shrivastava and B. H. Calhoun, "A 150 nW, 5 ppm/°C, 100 kHz on-chip clock source for ultra low power SoCs," in *Proc. IEEE Custom Integr. Circuits (CICC)*, Sep. 2012, pp. 1–4.
[17] Y. Lu, G. Yuan, L. Der, W.-H. Ki, and C. P. Yue, "A ±0.5% precision on-chip frequency reference with programmable switch array for crystal-less applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 10, pp. 642–646, Oct. 2013.
[18] Y. Tokunaga, S. Sakiyama, A. Matsumoto, and S. Dosho, "An on-chip CMOS relaxation oscillator with voltage averaging feedback," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1150–1158, Jun. 2010.
[19] M. Choi, I. Lee, T.-K. Jang, D. Blaauw, and D. Sylvester, "A 23 pW, 780 ppm/°C resistor-less current reference using subthreshold MOSFETs," in *Proc. IEEE Eur. Solid-State Circuit Conf. (ESSCIRC)*, Sep. 2014, pp. 119–122.
[20] *53230A 350 MHz Universal Frequency Counter/Timer, 12 Digits/s, 20 ps*, Keysight Technol., Santa Rosa, CA, USA, 2015.

Jaehong Jung (S'16–M'17) received the B.S. and M.S. degrees in semiconductor systems engineering from Sungkyunkwan University, Suwon, South Korea, in 2015 and 2017, respectively.

He joined an Internship Program at Samsung Electronics, Hwaseong, South Korea, in 2014, where he has been with the Infrastructure Design and Technology Team since 2017. His current research interests include high-speed serial links, phase-locked loops (PLLs), data converters, and clock generation circuit designs.

Ik-Hwan Kim (S'16–M'17) received the B.S. and M.S. degrees in semiconductor systems engineering from Sungkyunkwan University, Suwon, South Korea, in 2015 and 2017, respectively.

He joined an Internship Program at Samsung Electronics, Hwaseong, South Korea, in 2014, where he has been with the Infrastructure Design and Technology Team since 2017. His current research interests include high-speed serial links, power management ICs, and DC–DC converter designs.

Seong-Jin Kim (S'04–M'10) received the B.S. degree in electrical engineering from the Pohang University of Science and Technology, Pohang, South Korea, in 2001, and the M.S. and Ph.D. degrees in electrical engineering from KAIST, Daejeon, South Korea, in 2003 and 2008, respectively.

From 2008 to 2012, he was a Research Staff Member at the Samsung Advanced Institute of Technology, Yongin, South Korea, where he was involved in the development of CMOS imager for real-time acquisition of 3-D imagers. From 2012 to 2015, he was with the Institute of Microelectronics, A*STAR, Singapore, where he was involved in the design of analog-mixed signal circuits for various sensing systems. In 2015, he joined the School of Electrical and Computer Engineering, Ulsan National Institute of Science and Technology, Ulsan, South Korea, as an Associate Professor. His current research interests include high-performance imaging devices, and biomedical interface circuits and systems.

Yoonmyung Lee (S'08–M'12) received the B.S. degree in electronic and electrical engineering from the Pohang University of Science and Technology, Pohang, South Korea, in 2004, and the M.S. and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2008 and 2012, respectively.

From 2012 to 2015, he was with the University of Michigan as a Research Faculty. In 2015, he joined Sungkyunkwan University, Suwon, South Korea, as an Assistant Professor. His current research interests include energy-efficient integrated circuit design for low-power high-performance very large scale integration systems and millimeter-scale wireless sensor systems.

Dr. Lee was a recipient of the Samsung Scholarship and Intel Ph.D. Fellowship.

Jung-Hoon Chun (S'01–M'06) received the B.S. and M.S. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 1998 and 2000, respectively, and the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, USA, in 2006.

From 2000 to 2001, he was with Samsung Electronics, Hwaseong, South Korea, where he developed BiCMOS RF front-end IC for wireless communication. From 2006 to 2008, he was with Rambus Inc., Los Altos, CA, USA, where he worked on high-speed serial interfaces such as FlexIO, XDR, and XDR2. He is currently an Associate Professor with Sungkyunkwan University, Suwon, South Korea. He also consults for the several IC design and foundry companies in South Korea and Silicon Valley. His current research interests include high-speed serial links, image sensors, new memory devices, power management ICs, on-chip electrostatic discharge protection, and I/O design.

Dr. Chun was a recipient of the IEEE SOI Conference Best Paper Award in 2010, the IEEE CICC Best Paper Award in 2008, the Benhamou SGF Fellowship from 2003 to 2005, and the Gold Medal at the Humantech Thesis Competition in 1998. He served on the Technical Program Committee of the IEEE A-SSCC from 2009 to 2011 and from 2014 to 2017.