

# A 12-Gb/s –16.8-dBm OMA Sensitivity 23-mW Optical Receiver in 65-nm CMOS

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**Abstract**—Optical interconnects are being increasingly deployed in data centers to meet growing bandwidth requirements under tight power constraints. Therefore, there has been renewed focus on increasing data rates and improving power efficiency of optical links. Among all the link components, laser diodes typically consume the most power. Their power dissipation is dictated by the amount of signal power that needs to be transmitted to meet the bit error rate requirements under given channel loss and receiver sensitivity conditions. Consequently, improving receiver sensitivity directly helps lowering laser diode power consumption. In this paper, we present design techniques to implement such high sensitivity optical receivers. To this end, we identify noise-bandwidth tradeoffs of a shunt feedback transimpedance amplifier (SF-TIA) and elucidate how they limit the maximum achievable sensitivity at a given data rate and process technology. We then propose to combine a low-bandwidth SF-TIA with a four-tap decision feedback equalizer to overcome this noise-bandwidth tradeoff. The proposed SF-TIA uses high-gain multistage amplifier and large feedback resistance and achieves greatly improved noise performance. Fabricated in a 65-nm CMOS technology and heterogeneously integrated with a photonic IC, the proposed optical receiver achieves optical modulation amplitude sensitivity of  $-16.8$  dBm with 1.9-pJ/bit efficiency at 12 Gb/s.

**Index Terms**—Decision feedback equalizer (DFE), high sensitivity, multi-stage shunt feedback transimpedance amplifier (TIA), optical links, optical receiver, silicon photonics, TIA.

## I. INTRODUCTION

MODERN data centers contain thousands of interconnected servers and managing their power dissipation is one of the most challenging issues [1]. According to [1], interconnection network consumes around 23% of the total data center power consumption. As a result, there is a need for communication links that provide high bandwidth while consuming low power. Because of its low loss, optical fiber has become the de-facto medium of communication in data

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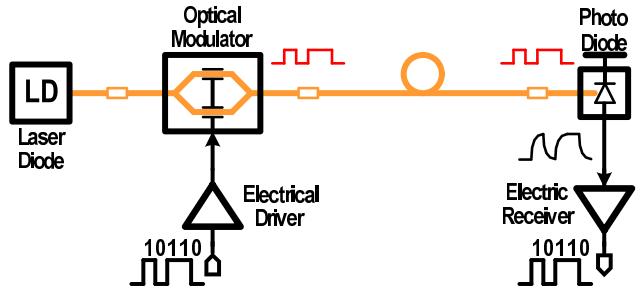


Fig. 1. Typical optical communication link.

centers [2]. Such optical fiber links are also better suited for increasing communication distance without significantly increasing power consumption. As shown in Fig. 1, a typical optical link consists of a transmitter (Tx) that converts electrical data into optical domain, an optical fiber, and a receiver (Rx) that converts the received optical signals back into electrical domain. While loss in the fiber is itself negligible, imperfect optical/electrical coupling at the Tx and Rx along with the Tx modulation loss causes frequency-independent signal attenuation. Consequently, minimum laser diode optical power is determined by the aforementioned losses and Rx optical sensitivity. Therefore, high-sensitivity optical receivers help reduce laser diode optical power, the major source of power dissipation in optical links, thus enabling low-power optical links. The design of such optical receivers is the main focus of this paper.

A typical optical receiver front-end is composed of a photo diode (PD) followed by a transimpedance amplifier (TIA) and a cascade of main amplifiers (MAs). PD outputs a current proportional to the power of the received optical signal. TIA converts PD current to voltage and the MAs amplify TIA output voltage to the desired signal level and drive the following decision circuitry. Both the receiver bandwidth and sensitivity are governed by the front-end TIA. While there are numerous TIA circuit topologies available in the literature [3]–[19], shunt feedback TIA (SF-TIA) offers superior gain-noise performance, and therefore is most commonly used [3]–[6], [8]–[12]. However, its performance degrades, especially at high data rates, due to the inevitable tradeoff between gain, bandwidth, and noise. This tradeoff arises from the fact that TIA gain scales proportionally with its feedback resistor, while both TIA bandwidth and noise scale inversely with the resistor value.

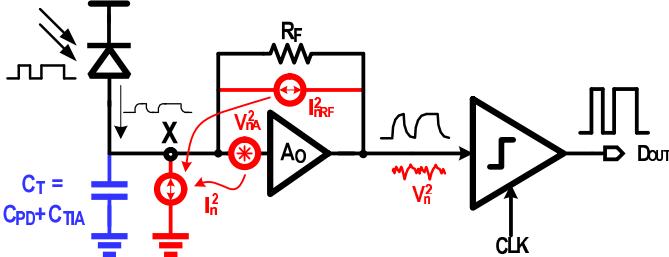


Fig. 2. Illustration of noise contributors in SF-TIA.

Conceptually, this tradeoff can be resolved by using a cascade of a low-bandwidth TIA + equalizer combination [4]–[10], [13]–[15], wherein noise is reduced by using a large feedback resistor at the expense of reduced TIA BW and the inter symbol interference (ISI) resulting from reduced TIA bandwidth is suppressed by the equalizer. In [4]–[6], a low-bandwidth TIA is followed by continuous-time linear equalizer (CTLE). However, CTLE amplifies high-frequency noise of the TIA and limits receiver sensitivity improvement. In [7], a decision feedback equalizer (DFE) is used to mitigate ISI without enhancing noise. However, utilizing a simple passive resistor to convert PD current to voltage severely limits the bandwidth, gain, and noise performance. More importantly, because TIA is embedded in the IIR-DFE critical path, it increases DFE loop latency, which results in incomplete cancellation of ISI.

In view of these drawbacks, this paper presents a high-sensitivity optical receiver that uses a high-gain low-bandwidth multistage SF-TIA cascaded with a four-tap FIR DFE. Fabricated in 65-nm CMOS process, the proposed receiver achieves an optical modulation amplitude (OMA) sensitivity of  $-16.8$  dBm at 12 Gb/s with a bit error rate (BER) of  $10^{-12}$ . The rest of this paper is organized as follows. After a brief overview on the design tradeoffs of the SF-TIA in Section II, the proposed optical receiver architecture is presented in Section III. Circuit implementation details of critical building blocks are provided in Section IV. Experimental results of the test chip are shown in Section V. Key contributions of this paper are summarized in Section VI.

## II. DESIGN TRADEOFFS IN SHUNT FEEDBACK TRANSIMPEDANCE AMPLIFIERS

A simplified schematic of SF-TIA is shown in Fig. 2. It consists of a feed-forward voltage amplifier and a feedback resistor,  $R_F$ , that converts input PD current into output voltage. TIA bandwidth is dictated by the pole at node X due to capacitance,  $C_T$ , and TIA input resistance.  $C_T$  is made up of two types of capacitances: 1) the PD, pad, and routing capacitance ( $C_{PD}$ ) and 2) TIA input capacitance ( $C_{TIA}$ ). Under the simplifying assumption that feed-forward amplifier has infinite bandwidth and a gain of  $A_O$ , SF-TIA transimpedances at dc ( $R_T$ ) and  $-3$  dB bandwidth are equal to  $(R_F A_O / 1 + A_O)$  and  $(A_O + 1/2\pi R_F C_T)$ , respectively. These expressions are accurate only as long as the TIA bandwidth is much lower than that of the feed-forward amplifier bandwidth. At high data rates, feed-forward amplifier bandwidth becomes comparable with the TIA bandwidth and its impact on the TIA performance cannot be ignored. In such cases, impact of finite bandwidth of

feed-forward amplifier can be accounted for by representing it as a single pole ( $\omega_A$ ) system with a transfer function of  $A(s) = A_O / (1 + (s/\omega_A))$ . This makes TIA transimpedance  $Z_T(s)$  to have second-order response given by [20]

$$Z_T(s) = \frac{R_F A_O}{1 + A_O} \times \frac{1}{1 + s/(\omega_o Q) + s^2/\omega_o^2} \quad (1a)$$

$$\omega_o = \sqrt{\frac{(1 + A_O)\omega_A}{R_F C_T}} \quad (1b)$$

$$Q = \frac{\sqrt{(1 + A_O)\omega_A R_F C_T}}{1 + R_F C_T \omega_A}. \quad (1c)$$

For maximally flat TIA magnitude (Butterworth) response,  $Q = 1/\sqrt{2}$  and the TIA bandwidth ( $BW_{3dB}$ ) can be expressed using (1b) and (1c) as

$$BW_{3dB} = \frac{\sqrt{2} A_O (A_O + 1)}{2\pi R_F C_T} \approx \frac{\sqrt{2} A_O}{2\pi R_F C_T}. \quad (2)$$

Equation (2) illustrates that the second-order SF-TIA  $3$ -dB bandwidth is increased by  $\sqrt{2}$  compared with the case when feed-forward amplifier had infinite bandwidth (first order) [20]. Also, feedback resistance,  $R_F$ , needed to achieve Butterworth SF-TIA response can be calculated using (1b) as

$$R_F = \frac{(A_O + 1)\omega_A}{C_T BW_{3dB}^2} \approx \frac{GBW_A}{2\pi C_T BW_{3dB}^2} \quad (3)$$

where  $GBW_A$  is the gain-bandwidth product of the feed-forward amplifier. Equation (3) shows that  $R_F$  decreases quadratically with  $BW_{3dB}$ , whereas it increases linearly with  $GBW_A$ . Thus, at high data rates, feedback resistance must be reduced to increase SF-TIA bandwidth at the expense of reduced transimpedance and increased  $R_F$  current noise.

### A. Noise Analysis

The main noise contributors of SF-TIA are the feedback resistor and feed-forward amplifier (see Fig. 2). When referred to the TIA input, noise from the feedback resistor appears as white noise while the feed-forward amplifier voltage noise has both  $f^2$  and white noise, as shown in Fig. 3(a). The input referred current noise power spectral density [ $\bar{i}_n^2(f)$ ] can be expressed as [20]

$$\begin{aligned} \bar{i}_n^2(f) &= \frac{4kT}{R_F} + \frac{4kT\gamma}{g_m R_F^2} + 4kT\gamma \times \frac{(2\pi C_T)^2}{g_m} \times f^2 \\ &\approx \frac{4kT}{R_F} + 4kT\gamma \times \frac{(2\pi C_T)^2}{g_m} \times f^2 \end{aligned} \quad (4)$$

where  $g_m$  is the transconductance of MOS input devices of the feed-forward amplifier. The output voltage noise power spectral density of the TIA can be calculated by multiplying the input referred current noise power spectral density by the squared magnitude of TIA transfer function [Fig. 3(c)]. The total input referred current noise power ( $\bar{i}_n^2$ ) can be calculated using Personick integrals [20] and expressed using two Personick integral numbers ( $I_1$  and  $I_2$ ) as shown in the following:

$$\bar{i}_n^2 = \beta_1 \times I_1 BW_{3dB} + \beta_2 \times \frac{I_2^3}{3} BW_{3dB}^3 \quad (5)$$

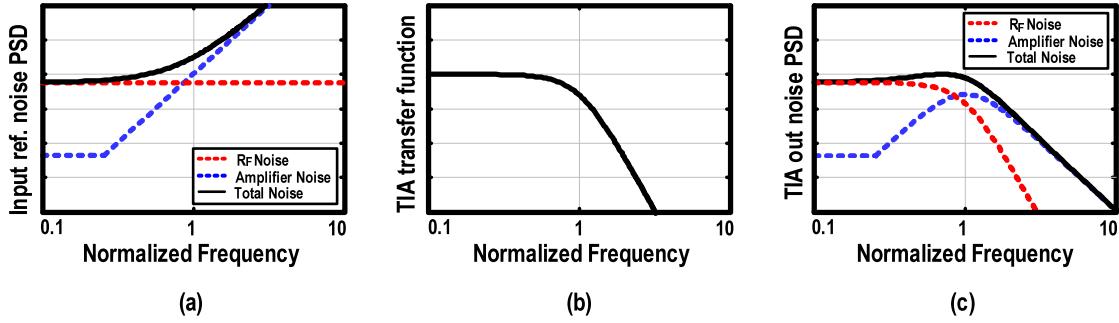


Fig. 3. (a) SF-TIA input referred current noise PSD. (b) SF-TIA magnitude response. (c) SF-TIA output voltage noise PSD.

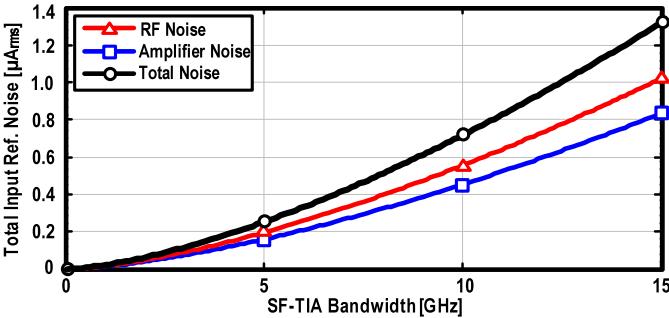


Fig. 4. Total input referred current noise of SF-TIA versus its 3-dB bandwidth ( $C_T = 100 \text{ fF}$ ,  $f_T = 150 \text{ GHz}$ , and  $\text{GBW}_A = 0.5 f_T$ ).

where  $\beta_1$  is the white noise coefficient ( $R_F$  noise) and  $\beta_2$  is  $f^2$  noise coefficient (feed-forward amplifier noise). Therefore, the total input referred current noise power ( $\bar{i}_n^2$ ) is given by

$$\bar{i}_n^2 = \frac{4kT}{R_F} \times I_1 \text{BW}_{3\text{dB}} + 4kT\gamma \times \frac{(2\pi C_T)^2}{g_m} \times \frac{I_2^3}{3} \text{BW}_{3\text{dB}}^3 \quad (6)$$

where  $I_1 = 1.11$  and  $I_2 = 1.49$  for Butterworth response [20]. The first term in (6) is due to  $R_F$  and the second term is due to feed-forward amplifier, which is minimized when  $C_{\text{PD}} = C_{\text{TIA}}$  [20]. Denoting input device  $g_m$  by

$$g_m = 2\pi f_T \times C_{\text{TIA}} = 2\pi f_T \times \frac{1}{2} C_T \quad (7)$$

and substituting (3) and (7) into (6),  $\bar{i}_n^2$  can be expressed in terms of  $C_T$ ,  $f_T$ , and TIA BW<sub>3dB</sub> as

$$\begin{aligned} \bar{i}_n^2 &= 4kT \frac{2\pi C_T}{\text{GBW}_A} \times I_1 \text{BW}_{3\text{dB}}^3 + 4kT\gamma \frac{4\pi C_T}{f_T} \times \frac{I_2^3}{3} \text{BW}_{3\text{dB}}^3 \\ &= 4kT \frac{2\pi C_T}{f_T} \text{BW}_{3\text{dB}}^3 \times \left( I_1 \times \frac{f_T}{\text{GBW}_A} + \frac{I_2^3}{3} \times 2\gamma \right). \end{aligned} \quad (8)$$

Equation (8) shows that both the noise quantities are proportional to  $\text{BW}_{3\text{dB}}^3$  and  $C_T/f_T$ , and therefore reducing TIA bandwidth is very beneficial in decreasing receiver input referred noise and improving receiver sensitivity. Fig. 4 shows input referred root-mean-square (rms) current noise ( $\bar{i}_n^2$ )<sup>1/2</sup> of a Butterworth SF-TIA versus its bandwidth, obtained using (8), for  $C_T = 100 \text{ fF}$  and  $f_T = 150 \text{ GHz}$  with  $\text{GBW}_A = 0.5 f_T$ . It shows that  $(\bar{i}_n^2)^{1/2}$  increases from 0.25 to 0.7  $\mu\text{A}_{\text{rms}}$

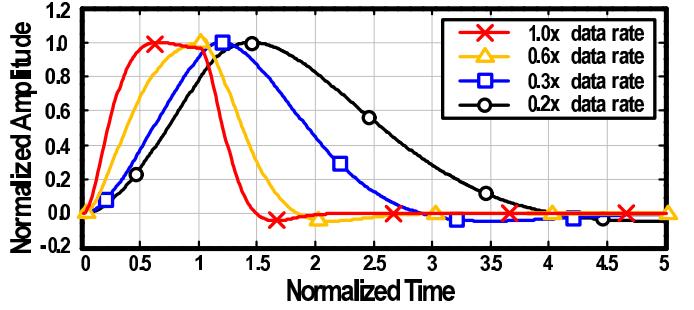


Fig. 5. SF-TIA pulse responses for different bandwidth–data rate ratios.

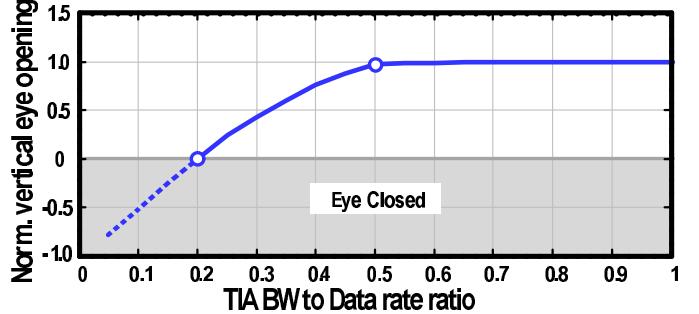


Fig. 6. Normalized vertical eye opening at the SF-TIA output versus its 3-dB bandwidth–data rate ratio.

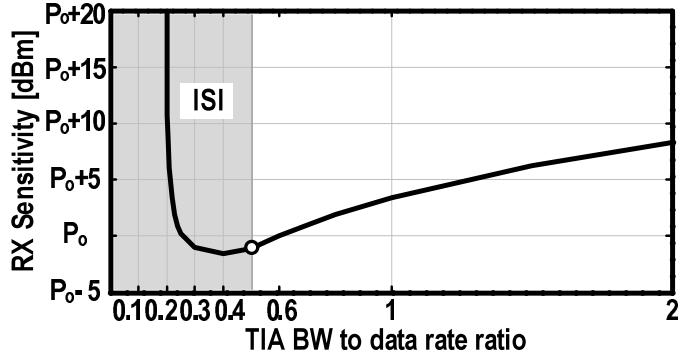


Fig. 7. SF-TIA receiver sensitivity at different TIA bandwidth–data rate ratios.

when the TIA bandwidth is increased from 5 to 10 GHz. Therefore, it is desirable to reduce TIA bandwidth for lower noise and improve receiver sensitivity. However, reducing TIA bandwidth increases the amount of ISI, which reduces voltage margin at the input of the decision circuit.

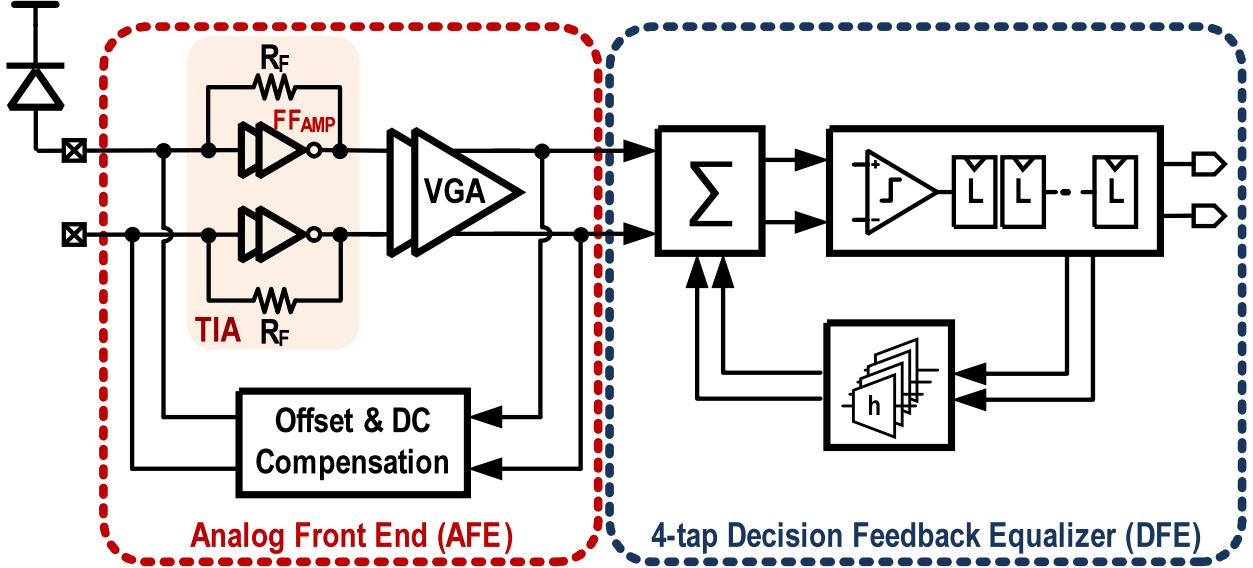


Fig. 8. Block diagram of the proposed optical receiver architecture.

### B. Impact of Inter Symbol Interference Introduced by SF-TIA

The impact of ISI can be evaluated using peak distortion analysis [21]. Using pulse response,  $y(t)$ , of a Butterworth SF-TIA shown in Fig. 5, minimum vertical eye opening ( $V_{\min}$ ) can be calculated as

$$V_{\min} = y[M] - \sum_{n=0}^{M-1} |y[n]| - \sum_{n=M+1}^{\infty} |y[n]| \quad (9)$$

where  $M$  is the main cursor index, while indices from 0 to  $M-1$  are for precursors and from  $M+1$  to  $\infty$  for post cursors. The normalized minimum vertical eye opening versus SF-TIA bandwidth-to-data rate ratio plotted in Fig. 6 illustrates that significant ISI is introduced for ratios less than 0.5 leading to complete eye closure when the ratio reaches 0.2.

BER of a receiver using a band-limited TIA can be determined by evaluating the combined impact of noise and ISI. In the noise-limited case (ISI is negligible), BER is governed by the signal-to-noise ratio (SNR) of the received signal and is equal to  $10^{-12}$  when SNR is equal to 7 (16.9 dB). In the ISI-limited case, the SNR lower bound can be estimated as the ratio between signal power calculated at the minimum vertical eye opening point of the received signal (calculated using peak distortion analysis) to total noise power. Receiver optical OMA sensitivity ( $P_{\text{sens}}|_{\text{OMA}}$ ) for a given BER can be calculated by incorporating TIA noise ( $i_n^2$ ) and the normalized minimum vertical eye opening ( $V_{\min}$ ) using the following equation:

$$P_{\text{sens}}|_{\text{OMA}} = 10 \log \left( R \times \sqrt{i_n^2} \times \frac{\sqrt{2} \operatorname{erfc}^{-1}(2 \times \text{BER})}{V_{\min}} \right) \quad (10)$$

where  $R$  is the PD responsivity. For 20-Gb/s data rate, BER of  $10^{-12}$ , and TIA with  $C_T = 100 \text{ fF}$ ,  $f_T = 150 \text{ GHz}$ , and  $\text{GBW}_A = 0.5f_T$ , receiver optical OMA sensitivity is plotted in Fig. 7 at different TIA bandwidths normalized to the data rate. This plot shows that receiver sensitivity is limited by

TIA noise for bandwidths larger than  $0.5x$  data rate and by ISI for smaller bandwidths, thus illustrating the fundamental tradeoff between noise and ISI. We seek to overcome this tradeoff by augmenting low bandwidth TIA with an equalizer as described next.

### III. PROPOSED OPTICAL RECEIVER

The block diagram of the proposed optical receiver is shown in Fig. 8. It is composed of analog front-end (AFE) consisting of a low-bandwidth multistage SF-TIA, variable gain amplifiers (VGAs), a dc offset correction loop, and a four-tap DFE back-end. Multistage SF-TIA uses large feedback resistor and three-stage feed-forward amplifier ( $FF_{\text{amp}}$ ) to achieve low noise and high gain, respectively. The four-tap DFE uses half-rate architecture and is optimized for minimum first-tap loop delay. Compared with a CTLE [4], FIR DFE offers ISI cancellation without enhancing noise, and compared with IIR-DFE [7], [8], it offers better ISI cancellation flexibility particularly at higher data rates where SF-TIA exhibits higher order response. These statements are further quantified next.

Increasing  $R_F$  by  $\alpha_{RF} > 1$  reduces SF-TIA bandwidth by the same factor to  $\text{BW}_{3\text{dB}}/\alpha_{RF}$ . The resulting ISI from reduced BW can be suppressed either using a CTLE [4]–[6] or a DFE [7], [8], [10]. Using a CTLE has two major drawbacks. First, high-frequency peaking needed to restore TIA bandwidth enhances noise and degrades sensitivity. Following analysis like the one used to derive (8), input referred noise ( $i_n^2|_{\text{CTLE}}$ ) of the optimal CTLE-equalized SF-TIA with its bandwidth perfectly restored can be calculated as:

$$\overline{i_n^2}|_{\text{CTLE}} = 4kT \frac{2\pi C_T}{f_T} \text{BW}_{3\text{dB}}^3 \times \left( \frac{I_1}{\alpha_{RF}} \times \frac{f_T}{\text{GBW}_A} + \frac{I_2^3}{3} \times 2\gamma \right). \quad (11)$$

Equation (11) shows that CTLE helps in reducing  $R_F$  noise contribution by  $\alpha_{RF}$  but does not affect the feed-forward

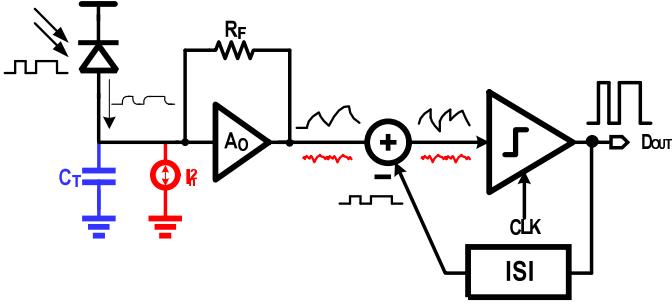


Fig. 9. Block diagram of DFE equalized TIA.

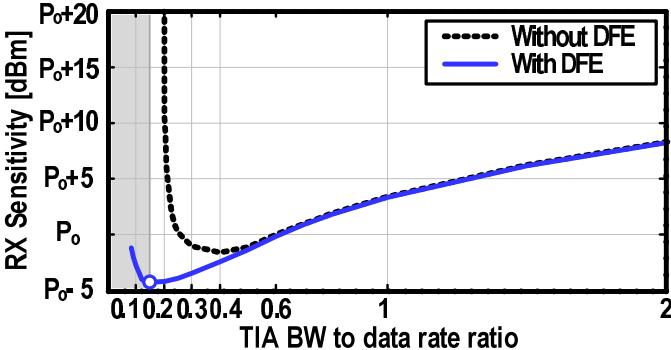


Fig. 10. DFE equalized TIA sensitivity (blue curve) at different TIA bandwidth–data rate ratios.

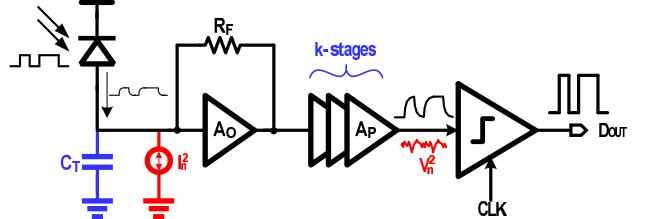
amplifier noise, which is the same conclusion reached by [4]. Second, CTLE with its first-order peaking response (one zero and two poles) cannot adequately compensate loss introduced by second-order TIA loss profile without introducing in-band peaking. Any such peaking, however, results in TIA noise enhancement and degrades receiver sensitivity.

Alternatively, DFE aims to mitigate ISI by directly subtracting the right amount ISI from the TIA output using the sampler output as shown in Fig. 9. DFE does neither add noise nor alter noise transfer function. However, DFE can only compensate ISI introduced by post cursors and cannot cancel any pre cursor ISI caused by second-order transfer function of the TIA. Consequently, the minimum vertical eye opening after DFE,  $V_{\min}$ , equals

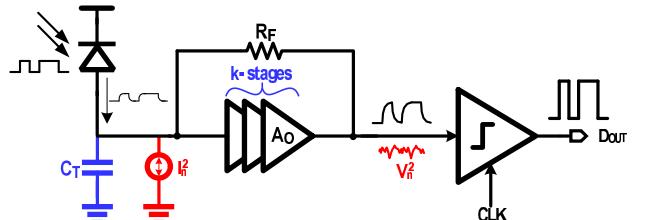
$$V_{\min} = y[M] - \sum_{n=0}^{M-1} |y[n]|. \quad (12)$$

Sensitivity of a DFE-equalized TIA calculated using minimum eye opening obtained from (12) and the TIA noise calculated in Section II-A is plotted in Fig. 10 for various TIA bandwidth–data rate ratios. This plot shows about 4-dB sensitivity improvement when TIA bandwidth is 0.15x the data rate compared with the conventional TIA that has a bandwidth–data rate ratio of 0.5x, which is the same conclusion arrived in [8] when using second-order TIA with DFE.

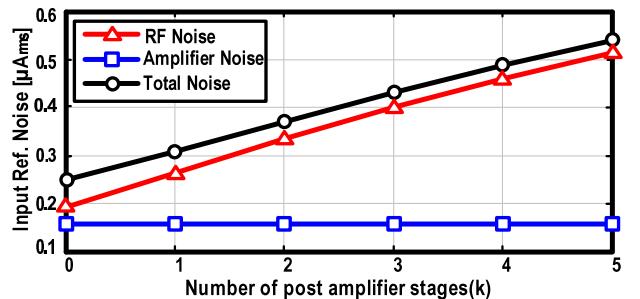
While DFE relaxes TIA bandwidth requirement, large front-end gain is still required to ensure adequate signal amplitude at the input of the decision circuitry. High front-end gain can be achieved either by additional voltage gain stages at the output of the TIA [5], [11] [Fig. 11(a)], or by using a high-gain multistage SF-TIA feed-forward amplifier [12], [22] [Fig. 11(b)]. Both architectures utilize additional voltage gain



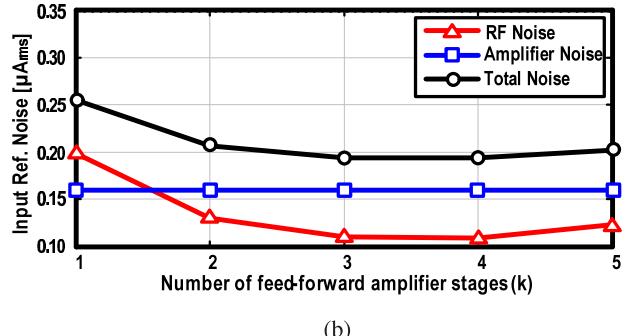
(a)



(b)

Fig. 11. (a) Block diagram of single-stage SF-TIA followed by  $k$  stages of post amplifiers. (b) Block diagram of SF-TIA with  $k$  stage feed-forward amplifier.

(a)



(b)

Fig. 12. (a) Input referred current noise of (a) SF-TIA followed by  $k$  stages of post amplifiers and (b) SF-TIA with  $k$  stage feed-forward amplifier ( $C_T = 100$  fF,  $f_T = 150$  GHz, 3-dB bandwidth of 5 GHz, and  $\text{GBW}_A = 0.5 f_T$ ).

stages but differ in where they are placed. In one case, they are placed outside the SF-TIA loop and in the other inside it. Consequently, they offer different noise, stability, gain, and bandwidth tradeoffs as described next.

Amplifying stages when added after the SF-TIA as shown in Fig. 11(a) (topology-1) end up degrading front-end bandwidth. Alleviating this bandwidth degradation requires lowering  $R_F$  with the exact amount of reduction ( $\Gamma_{PA}[k]$ ) dictated

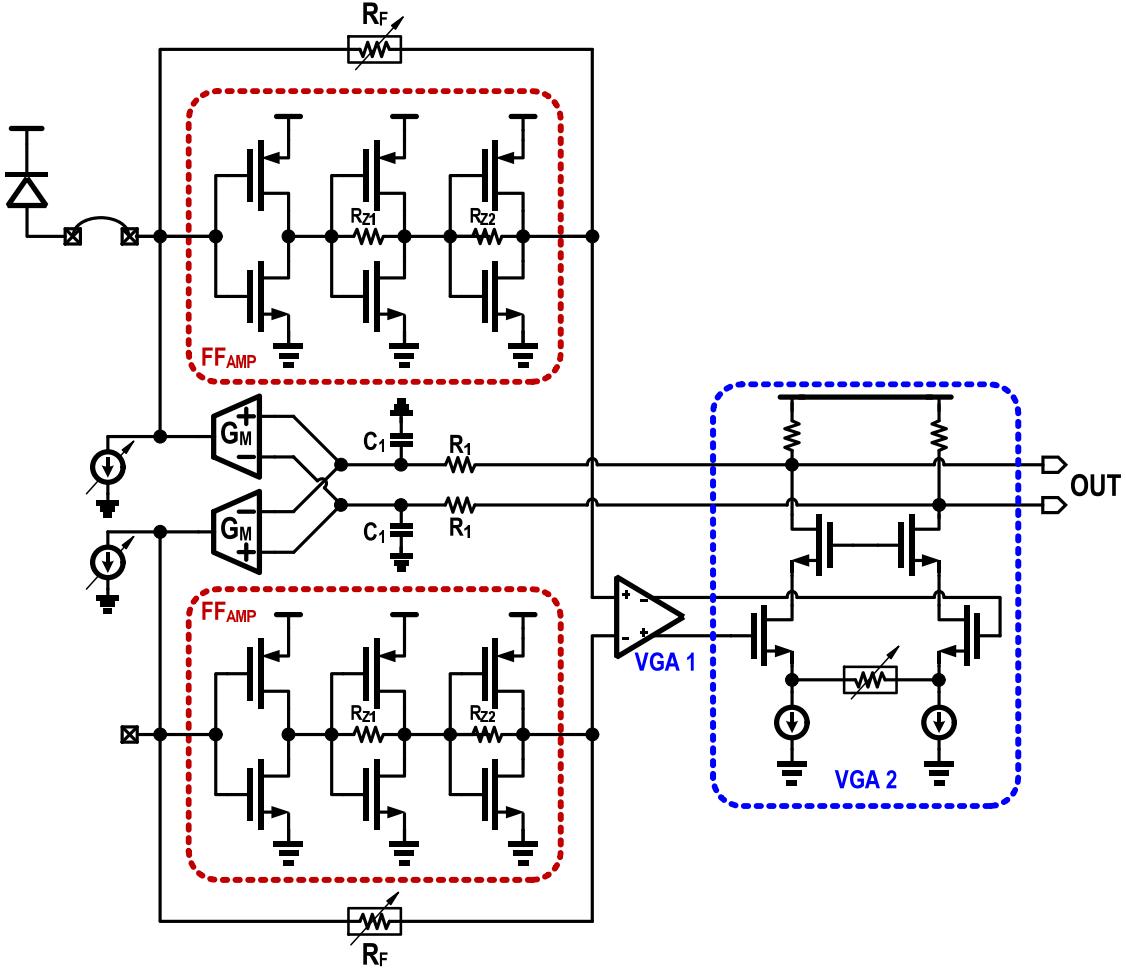


Fig. 13. Schematic of the proposed AFE.

by the number of amplifying stages ( $k$ ) (see Appendix A for an expression for  $\Gamma_{PA}[k]$ ). On the other hand, using  $k$  stages of feed-forward amplifier inside the SF-TIA as shown in Fig. 11(b) (topology 2) increases SF-TIA feed-forward gain and permits increasing the feedback resistor value without altering the SF-TIA 3-dB bandwidth. The amount by which the feedback resistor can be increased ( $\Gamma_{FF}[k]$ ) is derived in Appendix B. Using analysis similar to that described in Section II-A, an expression for  $i_n^2$  of the two new topologies can be derived as

$$\bar{i_n^2} = 4kT \frac{2\pi C_T}{f_T} \text{BW}_{3 \text{ dB}}^3 \times \left( \frac{I_1}{\Gamma[k]} \times \frac{f_T}{\text{GBW}_A} + \frac{I_2^3}{3} \times 2\gamma \right) \quad (13)$$

where  $\Gamma[k]$  equals  $\Gamma_{PA}[k]$  in the case of adding  $k$  amplifying stages after SF-TIA, and  $\Gamma_{FF}[k]$  when the  $k$  stages are added inside the SF-TIA. Equation (13) shows that only the feedback resistor noise contribution is affected in both options while the feed-forward amplifier noise remains unaltered. Input referred rms current noise ( $i_n^2$ ) $^{1/2}$  plotted versus the number of added amplifying stages ( $k$ ) in Fig. 12 for a front-end BW<sub>3 dB</sub> of 5 GHz shows that ( $i_n^2$ ) $^{1/2}$ , as expected, increases with  $k$  for topology-1 and decreases with  $k$  for topology-2. For example, ( $i_n^2$ ) $^{1/2}$  is 0.2  $\mu\text{A}_{\text{rms}}$  when a three-stage feed-forward amplifier

is used in the SF-TIA, which is two times lower compared with the case of a single-stage SF-TIA followed by three post amplifier stages (0.4  $\mu\text{A}_{\text{rms}}$ ). Based on this analysis, SF-TIA using multistage feed-forward amplifier is employed in our design.

#### IV. BUILDING BLOCKS

The proposed optical receiver consists of an AFE followed by the DFE (see Fig. 8). The AFE consists of a multistage SF-TIA, a two-stage VGA, and a dc offset correction loop. Multistage SF-TIA uses large feedback resistor and three-stage feed-forward amplifier to achieve high gain and low noise. The VGA, designed using CML stages, provides a gain of 10 dB and shields the TIA from DFE loading. The mixed-signal dc/offset correction circuitry compensates for PD dc current and receiver offset. Four-tap DFE uses half-rate architecture and is optimized for minimum first tap loop delay. The receiver is intended to be connected to a Silicon Photonics PD that has 50-fF junction capacitance. In the following sections, detailed implementation of the receiver building blocks is discussed.

##### A. Transimpedance Amplifier and VGA

Schematic of SF-TIA along with the VGA is shown in Fig. 13. The feed-forward amplifier is implemented using

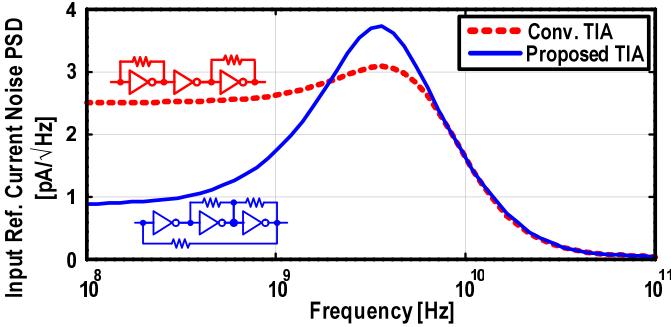


Fig. 14. Input referred current noise PSD of conventional SF-TIA with multistage post amplifier (red curve) and the proposed multistage SF-TIA (blue curve).

a cascade of three CMOS inverter stages to achieve high gain-bandwidth product even when operating with a low supply voltage. Large gain provided by the three stages helps in increasing feedback resistor value and consequently reduces its noise contribution. The simulated feed-forward amplifier dc gain and bandwidth are 30 dB and 7 GHz, respectively. A 20-k Ω feedback resistor is used, which results in a TIA bandwidth of 3.5 GHz with total capacitance at the input of the TIA of 120 fF, which is composed of 50-fF PD capacitance, 50-fF pad and routing parasitic capacitance, and 20-fF TIA input capacitance. Even though feed-forward amplifier noise is minimized when  $C_{PD} = C_{TIA}$  [20], the utilized  $C_{TIA}$  is only 20% of the  $C_{PD}$  to reduce the TIA power consumption at the expense of increasing TIA noise by 7% (0.3-dB sensitivity degradation).

Local feedback resistors,  $R_{Z1}$  and  $R_{Z2}$ , are added in the second and third stages to reduce intrinsic gain and improve phase margin to about 65° in the prototype. Feedback resistor is made programmable to control the TIA bandwidth and tradeoff noise with ISI. The simulated input referred current noise PSD of the proposed and conventional multistage post amplifier SF-TIA [5] is plotted in Fig. 14. Both TIAs have the same bandwidth, size, and power consumption. Simulation results show that the input referred noise of the proposed and conventional SF-TIAs is 0.3 and 0.5 μA<sub>rms</sub>, respectively, which illustrates that the proposed SF-TIA offers better noise performance while providing the same bandwidth and consuming the same power as that of a conventional SF-TIA.

A dummy TIA is used to generate reference voltage to the VGA that converts single-ended TIA output to a differential signal. Even though dummy TIA doubles noise power and degrades sensitivity by about 3 dB, it is necessary to improve supply noise immunity and ensure robust operation of the single-ended inverter-based TIA. However, a large capacitor can be added at the output of the dummy TIA to filter its noise, but is not used in our design because it severely degrades high-frequency power supply noise rejection. Two CML VGA stages (VGA1 and VGA2) are used to amplify the TIA output to about 400 mV<sub>pp</sub>. The second stage is designed to drive large input capacitance of the DFE summing amplifiers. VGA1 and VGA2 have a gain of 3.6 and 2 dB, respectively. Each of the VGAs has a 3-dB bandwidth of 8.5 GHz, which reduces AFE overall bandwidth to 3 GHz. Unlike limiting amplifiers used

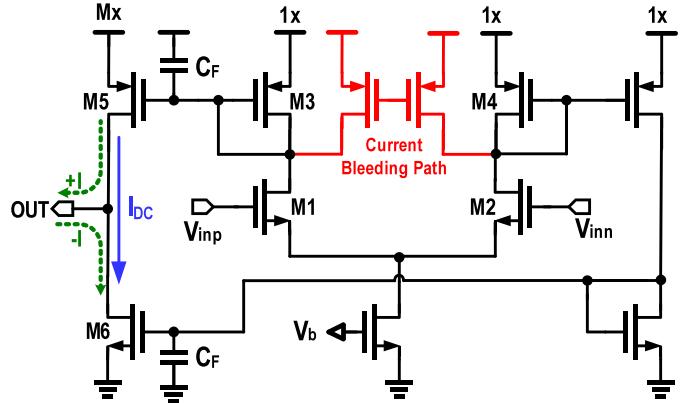


Fig. 15. Schematic of transconductance (GM) cell used in the analog offset cancellation loop.

in conventional receivers, the linearity of post amplifiers is important as they drive the DFE. So, both stages are source degenerated to improve linearity. Thanks to the large gain provided by the TIA, post amplifiers are designed with low GBW product and consume 1.5-mW power.

### B. DC Offset Cancellation

The average PD current and input referred offset due to random mismatches degrade receiver sensitivity. To mitigate this, a dc offset cancellation loop that uses coarse digital trimming along with fine analog cancellation is employed (see Fig. 13). This mixed digital/analog approach is necessary to cover wide range of PD dc currents and offset voltages with fine accuracy. Digital trimming is performed through two 5-bit DACs (LSB = 0.5 μA) that draw current from the main and dummy TIA inputs. With AFE dc transimpedance of 20 kΩ, digital trimming provides a cancellation range of 310 mV with a resolution of 10 mV (0.5 μA × 20 kΩ), when referred to the output of VGA. Analog cancellation path consisting of low cutoff RC section ( $R_1, C_1$ ) followed by two transconductors (GM) cells is connected between the second VGA output and TIA input as shown in Fig. 13. Closed-loop transfer function of the AFE ( $H_{AFE}(s)$ ) is given by

$$H_{AFE}(s) = \frac{Z_T(s)}{1 + Z_T(s) \times G_m \times H_{RC}(s)} \approx \frac{R_T}{1 + R_T \times G_m \times H_{RC}(s)} \approx \frac{R_T}{1 + R_T \times G_m + s R_1 C_1} \quad (14)$$

where  $H_{RC}(s)$  is the transfer function of the low-pass filter section formed by ( $R_1, C_1$ ) and  $G_m$  is transconductance of the GM cells. The cutoff frequency ( $f_C$ ) of the AFE can be calculated from (14) as

$$f_C = \frac{1 + R_T \times G_m}{2\pi \times R_1 \times C_1}. \quad (15)$$

Cutoff frequency ( $f_C$ ) must be much smaller than the received signal data rate to avoid baseline wander or data-dependent jitter, especially in the presence of long sequence of consecutive identical digits. The implemented AFE has

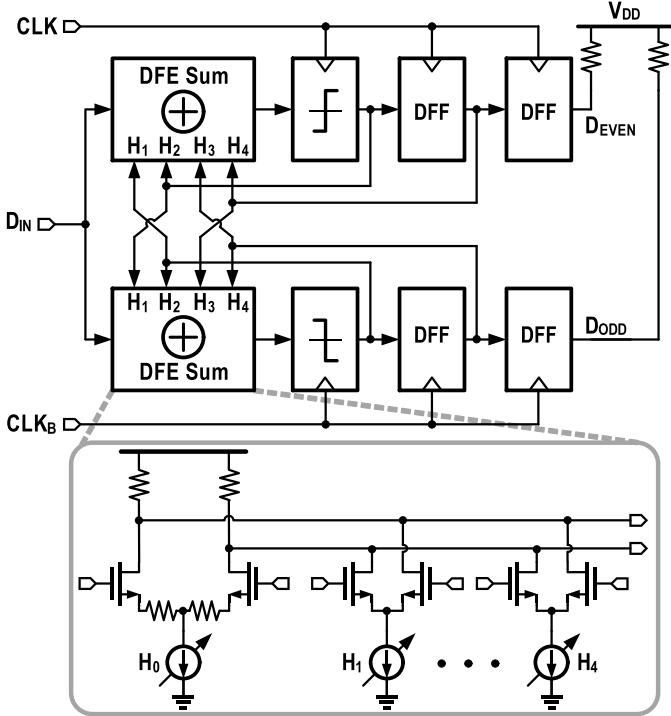


Fig. 16. Block diagram of four-tap half-rate DFE.

a cutoff frequency of 20 kHz. Analog cancellation path further reduces the residual offset left after coarse digital correction by the amount of AFE dc open loop gain ( $R_T \times G_m$ ). Therefore, AFE must have a dc gain of about 20 to reduce residual offset from 10 to 0.5 mV. In other words, achieving 0.5-mV output offset accuracy requires GM cells to have a transconductance of 1 mS (20/20 k $\Omega$ ). The GM cells implemented using current mirror OTAs shown in Fig. 15 can provide both positive and negative compensating currents. The output noise of the GM cell greatly affects overall receiver noise performance because the compensating current (GM output current) is applied directly to the TIA input. Output current noise [ $\overline{i_n^2}_{\text{OUT}}(f)$ ] of the GM cell can be expressed as

$$\begin{aligned} & \overline{i_n^2}_{\text{OUT}}(f) \\ & \approx \overline{i_n^2}_{(M5+M6)}(f) + M \times \overline{i_n^2}_{(M1+M2+M3+M4)}(f) \cdot |H(s)|^2 \\ & = \overline{i_n^2}_{(M5+M6)}(f) + M \times \overline{i_n^2}_{(M1+M2+M3+M4)}(f) \\ & \quad \frac{1}{1 + \left(\omega \frac{C_F}{g_m M_5}\right)^2} \end{aligned} \quad (16)$$

where  $H(s)$  is the transfer function of the low-pass filter formed by diode connected device M3 and  $C_F$ . The second term in (16) can be suppressed using large  $C_F$ , which modifies (16) to

$$\overline{i_n^2}_{\text{OUT}}(f) \approx \overline{i_n^2}_{(M5+M6)}(f) = 4kT\gamma(g_m M_5 + g_m M_6). \quad (17)$$

Equation (17) shows that the GM cell output noise is minimized by reducing  $g_m$  of M5 and M6 transistors, which can be done by reducing dc current in the output stage ( $I_{dc}$ ). To this end, current bleeding branches are added in the first stage of the GM cell (see Fig. 15) to reduce the output stage dc current without reducing  $g_m$  of input devices, M1/M2.

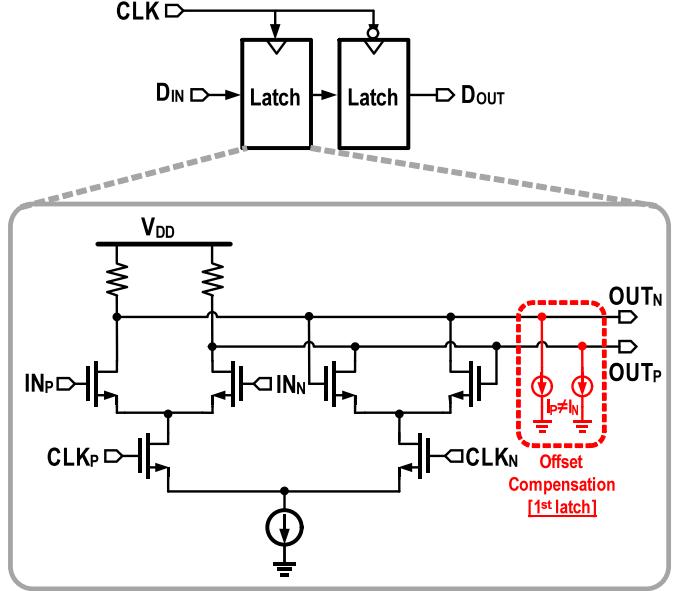


Fig. 17. Schematic of DFE comparator and latch.

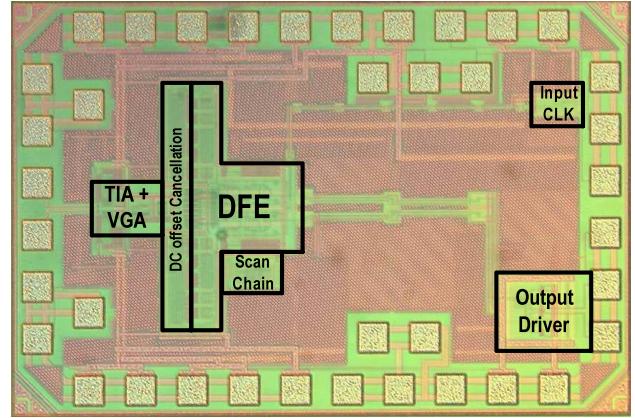


Fig. 18. Die micrograph of the proposed optical receiver.

It is important to note that the offset compensation current generated by the analog loop is applied to both the main and dummy TIAs. This improves low-frequency power supply noise rejection and also helps in achieving lower residual offset compared with a single-ended topology. The implemented offset cancellation range can be extended by increasing the range of offset trimming DAC. Because DAC output current is proportional to input signal at a high extension ratio, its noise contribution is large only when the modulated input signal is large. As a result, increasing DAC range does not degrade sensitivity.

### C. Half-Rate DFE

Block diagram of the four-tap half-rate DFE is shown in Fig. 16. Simulations show that four taps are sufficient to cancel the ISI when TIA bandwidth is 15% of the input data rate (Section III). The taps' weights are programmable to cover both small and large amounts of ISI at low and high data rates, respectively. The comparators are built using two CML latches as shown in Fig. 17. Offset of the first

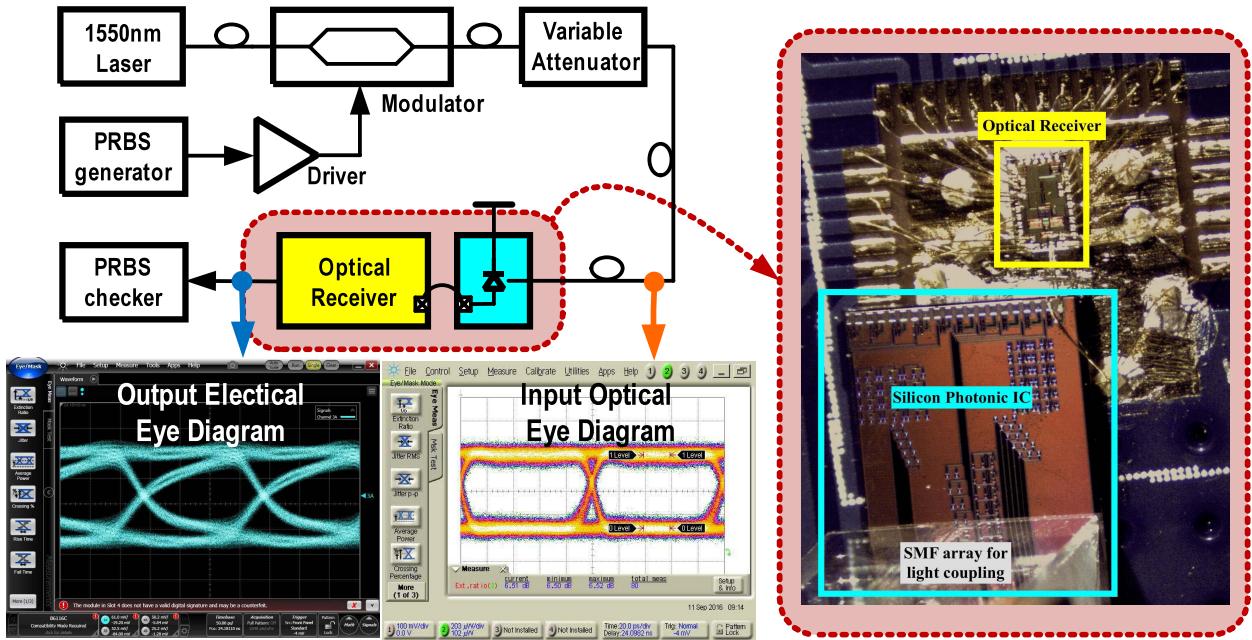


Fig. 19. Optical test setup and micrograph of the receiver bonded to the PD in the Silicon Photonics IC.

latch is canceled at its output by adding unbalanced currents. D-flip flops are used to generate the delayed versions of the sampled clock and they are implemented with master–slave CML latches. The DFE summing amplifiers are implemented by CML circuits with resistively degenerated input differential pair for better linearity, and current DACs are used to set the DFE weights. DFE latches are driven by an external 6-GHz sampling clock. Total power consumption of four-tap DFE is 17 mW at 12 Gb/s. A 50- $\Omega$  CML output driver is used to drive half-rate data off chip.

## V. EXPERIMENTAL RESULTS

A prototype receiver is fabricated in a 65-nm CMOS technology and tested with a Silicon Photonic waveguide Ge PD. Photonic integrated circuit with the PD is wire-bonded to the TIA input. The receiver occupies an active area of 0.12 mm<sup>2</sup> and its micrograph is shown in Fig. 18. The PD has a junction capacitance of 50 fF and responsivity of 0.75 A/W. The optical test setup is shown in Fig. 19. The laser output is modulated by a LiNb modulator with  $(2^{31} - 1)$  PRBS pattern generator and coupled to the PD via a single-mode fiber. A variable attenuator is used to set the optical signal power to the desired level at PD input for sensitivity measurements. The full-rate optical signal received by the PD is ISI free with an extinction ratio of 6.5 dB as shown in Fig. 19.

Fig. 20 shows the receiver BER versus input OMA at 5, 10, and 12 Gb/s. When the DFE coefficients are optimally set, the receiver achieves sensitivities of –19.2, –17.4, and –16.8 dBm for 5, 10, and 12 Gb/s, respectively, at  $10^{-12}$  BER. At 5 Gb/s, the receiver performance is independent of whether the DFE is enabled or not because the receiver bandwidth of 3.5 GHz is sufficiently wide to not introduce ISI. However, large amount of DFE equalization is needed at 12 Gb/s to achieve error-free operation ( $\text{BER} < 10^{-12}$ ) at –16.8-dBm

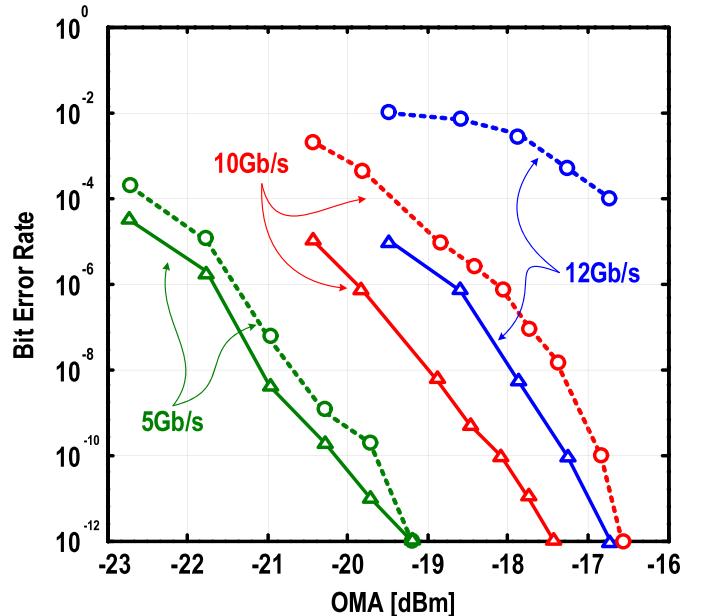


Fig. 20. Measured BER versus OMA at 5, 10, and 12 Gb/s for PRBS31 input pattern when DFE is enabled (solid) and disabled (dotted).

OMA, which is the highest sensitivity reported at 12 Gb/s in 65-nm CMOS technology.

Bathtub curves are measured for 10 and 12 Gb/s at input OMA of –12 dBm and shown in Fig. 21. At 10 Gb/s, DFE increases eye opening from 0.1 to 0.3UI at  $10^{-9}$  BER. At 12 Gb/s, the eye is totally closed when the DFE is disabled and an eye opening of 0.3UI is achieved with DFE. The input full-rate optical eye and the output half-rate electric eye are shown in Fig. 19. The total receiver power consumption at 12 Gb/s is 23 mW, which translates to a power efficiency of 1.9 pJ/bit. Of the 23 mW, TIAs consume 4.5 mW,

TABLE I  
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART OPTICAL RECEIVERS

Reference	F. Liu JSSC'12 [3]	Dan Li JSSC'14 [4]	M. Raj JSSC'16 [15]	A. Sharif JSSC'16 [8]	Proesel ISSCC'13 [7]	Cevrero ISSCC'17[9]	Palermo ISSCC'07 [19]	This Work
Technology	40nm CMOS	65nm CMOS	28nm CMOS	65nm CMOS	90nm CMOS	14nm FinFET bulk	90nm CMOS	65nm CMOS
Architecture	TIA Half-rate	TIA + CTLE	RC BW-limited Double-Sampler	TIA + IIR-DFE Half-rate	DFE-IIR Full-Rate	TIA + 1-tap DFE Half-Rate	Integrating Double-Sampler	High FB Res. TIA + 4-tap DFE Half-Rate
Data Rate [Gb/s]	10	25	32	20	8   9	32   64	10   16	10   12
PD Responsitivity	0.8	0.91	0.9	0.5	0.55	0.52	0.5	0.75
Rx Cin [fF]	--	160	120fF	200	140	69	440	100
Area [mm <sup>2</sup> ]	0.007	0.42†	0.018**	0.027	0.0045	0.028	0.105	0.12
Power [mW]	4	93	3.26	14.1	8.4	91++	23	23
Sensitivity OMA [dBm]	(-12)*	-11.9	-8.8	-5.8	-7   -5	-13   -5.5	(-6.6)*   (-2.4)*	-17.6   -16.8

\* Calculated from reported avg. sensitivity

\*\*4 channel

† including pads

++ Meas. at 64 Gb/s

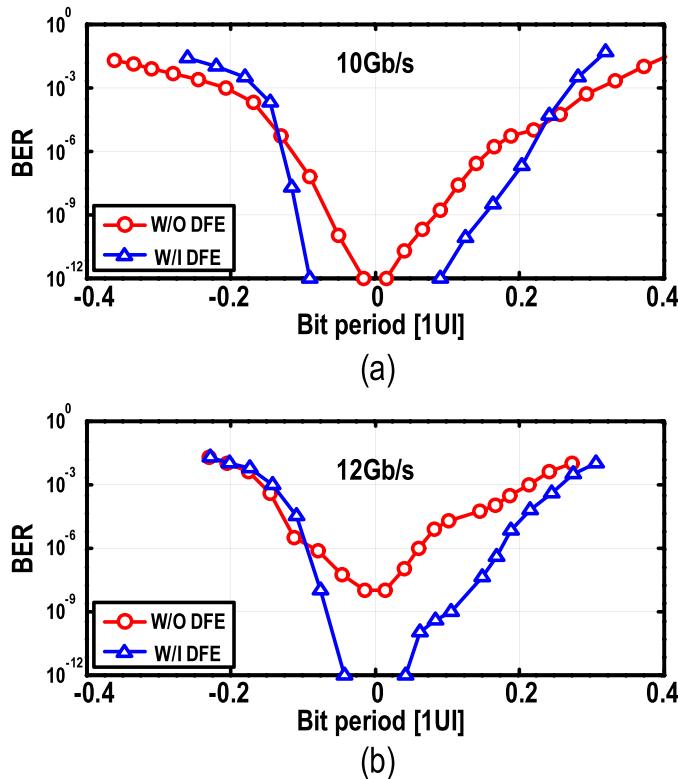


Fig. 21. Bathtub curves with and without the DFE. (a) 10 Gb/s. (b) 12 Gb/s.

VGAs consume 1.5 mW, and the DFE consumes 17 mW including the clock buffers. The performance summary and comparison with the state-of-art clocked optical receivers are shown in Table I. Thanks to the combination of the low-noise multistage SF-TIA with DFE, the proposed receiver achieves the highest sensitivity in 65-nm CMOS technology at 12 Gb/s. The proposed equalization technique can be extended to higher data rates similar to [9] in which 64 Gb/s is achieved. The achieved performance reduces the sensitivity gap between the state-of-art BiCMOS and CMOS optical receivers.

## VI. CONCLUSION

We presented design techniques to implement high-sensitivity optical receivers. Low-bandwidth multistage SF-TIA cascaded with a four-tap DFE was proposed to overcome SF-TIA noise–bandwidth tradeoff. Sensitivity analysis showed that low-bandwidth SF-TIA with DFE improves the receiver sensitivity by 4 dB. The proposed multistage SF-TIA uses three-stage feed-forward amplifier and a 20-k $\Omega$  feedback resistor and greatly improves noise performance. A prototype of the proposed receiver was fabricated in 65-nm CMOS. The receiver was wire-bonded with silicon photonic wave guide PD. The measured OMA sensitivities at 10 and 12 Gb/s were  $-17.4$  and  $-16.8$  dBm, respectively, which is the highest reported sensitivity in 65-nm CMOS technology at 12 Gb/s. The receiver power dissipation is 23 mW (1.9 pJ/bit).

## APPENDIX A SF-TIA FOLLOWED BY MULTISTAGE POST AMPLIFIER

Block diagram of single-stage SF-TIA followed by multistage post amplifier is shown in Fig. 11(a). SF-TIA is assumed to have Butterworth response with a bandwidth of  $BW_{TIA}$ . The post amplifiers are realized with a cascade of  $k$  identical stages that have a gain of  $A_P$  and bandwidth of  $BW_P$ . For simplicity, we assume that  $BW_P$  and  $BW_{TIA}$  are both equal to  $BW_S$ . The magnitude of transimpedance, ( $|Z_{T2}(f)|$ ), can be expressed as

$$|Z_{T2}(f)| = A_P^k \frac{R_F A_O}{1 + A_O} \times \left( \frac{1}{\sqrt{1 + f^4/BW_S^4}} \right) \times \left( \frac{1}{\sqrt{1 + f^2/BW_S^2}} \right)^k. \quad (18)$$

As expected, dc transimpedance ( $R_T$ ) is equal to  $A_P^k (R_F A_O / 1 + A_O)$ , which is higher than single SF-TIA by  $A_P^k$  while  $BW_{3dB}$  is lower than the SF-TIA bandwidth ( $BW_S$ ). The bandwidth degradation factor ( $\alpha_k = BW_{3dB}/BW_S$ ), numerically calculated and plotted

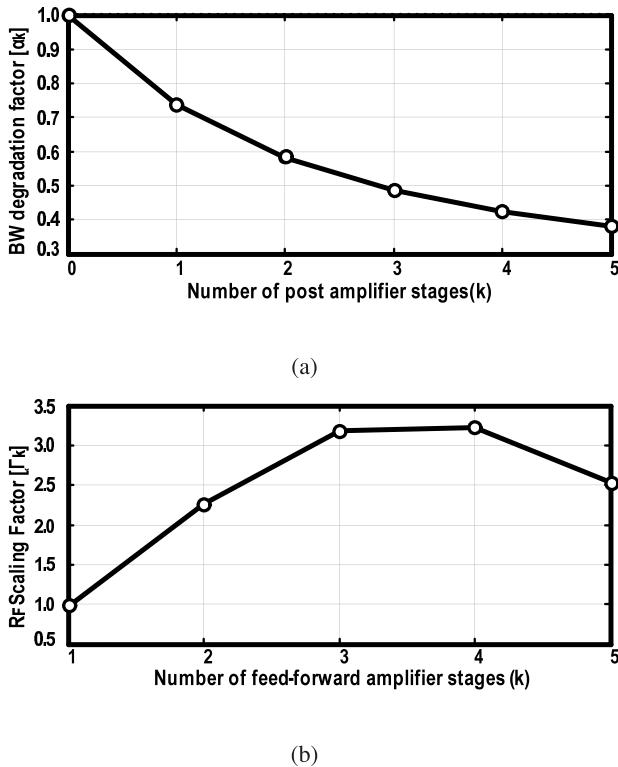


Fig. 22. (a) SF-TIA bandwidth degradation factor ( $\alpha_k$ ) versus number of post amplifier stages. (b) Feedback resistor scaling factor ( $\Gamma_k$ ) versus feed-forward amplifier stages ( $\phi_m = 64^\circ$ ).

versus the number of post amplifier stages ( $k$ ) in Fig. 22(a), shows that adding post amplifiers significantly degrades  $BW_{3\text{dB}}$ . For example, bandwidth is reduced by a factor of two when three post amplifier stages are added. Using (3), SF-TIA feedback resistor ( $R_F$ ) can be expressed as

$$R_F = \frac{GBW_A}{2\pi C_T BW_s^2} = \frac{GBW_A}{2\pi C_T BW_{3\text{dB}}^2} \times \alpha_k^2 \\ = \frac{GBW_A}{2\pi C_T BW_{3\text{dB}}^2} \times \Gamma_{PA}[k] \quad (19)$$

where  $\Gamma_{PA}[k]$  is the reduction amount in  $R_F$  while utilizing  $k$  stages of post amplifiers in order to obtain the required receiver front-end 3-dB bandwidth.

## APPENDIX B

### SF-TIA WITH MULTISTAGE FEED-FORWARD AMPLIFIER

Block diagram of SF-TIA implemented using a multistage feed-forward amplifier is shown in Fig. 11(b).  $k$  identical gain stages each of which having a gain of  $A_O$  and one pole at  $BW_O$  are used to implement the feed-forward amplifier. Assuming  $(R_F, C_T)$  is the dominant pole, loop gain unity gain frequency and phase margin can be estimated as

$$FUGF = A_O^k / (2\pi R_F C_T) \quad (20)$$

$$\phi_m = 90 - k \times \tan^{-1} \left( \frac{A_O^k}{2\pi R_F C_T \times BW_O} \right). \quad (21)$$

A phase margin of  $64^\circ$  is required to achieve a response similar to the Butterworth response of single-stage SF-TIA.

$BW_{3\text{dB}}$  of multistage SF-TIA can be calculated from (2) by substituting  $A_O$  by  $A_O^k$  and is equal to

$$BW_{3\text{dB}} \approx \frac{\sqrt{2} A_O^k}{2\pi R_F C_T}. \quad (22)$$

Using (21) and (22), multistage SF-TIA  $BW_{3\text{dB}}$  is expressed as

$$BW_{3\text{dB}} = \sqrt{2} \tan \left( \frac{90 - \phi_m}{k} \right) \times BW_O. \quad (23)$$

$R_F$  of multistage SF-TIA can be expressed in terms of  $BW_{3\text{dB}}$  using (22) and (23) as

$$R_F = \frac{GBW_O}{2\pi C_T BW_{3\text{dB}}^2} \times \Gamma_{FF}[k] \quad (24a)$$

$$\Gamma_{FF}[k] = \frac{\sqrt{2} GBW_O^{k-1}}{BW_{3\text{dB}}^{k-1}} \times \left( \sqrt{2} \tan \left( \frac{90 - \phi_m}{k} \right) \right)^k \quad (24b)$$

where  $\Gamma_{FF}[k]$  represents  $R_F$  scaling factor in multistage SF-TIA compared with the single-stage SF-TIA case. For  $k = 1$  and  $\phi_m = 64^\circ$ ,  $\Gamma_{FF}[k]$  equals to unity, irrespective of the TIA  $BW_{3\text{dB}}$  because this condition is equivalent to the single-stage SF-TIA case.  $\Gamma_{FF}[k]$  is plotted versus the number of stages in Fig. 22(b) with SF-TIA  $BW_{3\text{dB}}$  equal to 5 GHz. It shows that  $R_F$  is increased by 3x while utilizing three-stage TIA feed-forward amplifier. However,  $\Gamma_{FF}[k]$  decreases for larger number of stages to ensure the desired phase margin requirement. Therefore, there exists an optimum for the number of stages to achieve the highest enhancement in  $R_F$ .

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