A $1.8e^-_{rms}$ Temporal Noise Over 110-dB-Dynamic Range 3.4 μm Pixel Pitch Global-Shutter CMOS Image Sensor With Dual-Gain Amplifiers SS-ADC, Light Guide Structure, and Multiple-Accumulation Shutter

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***Abstract*— A $1.8e^-_{rms}$ temporal noise over 110 dB dynamic range 3.4 μm pixel pitch global shutter (GS) CMOS image sensor (CIS) single-slope analog digital converters (ADCs) with dual-gain amplifier (SSDG-ADC), light guide (LG) structure, and multiple-accumulation shutter has been developed for various accuracy required applications. The newly developed CIS pixel achieves low noise, high saturation, high sensitivity, and high frame rate with seamless GS function. Low noise, high saturation, and high frame rate are realized by small photodiode, large charge-domain memory, and seamless multiple-accumulation readout procedure with SSDG-ADC. Furthermore, high sensitivity is realized by the optimized shape LG structure. The GS CIS is fabricated in a 130 nm 1Poly-Si 4Metal with light shield CMOS process. This image sensor achieves $1.8e^-_{rms}$ temporal noise, 16 200e^- full-well capacity with 60 fps multiple-accumulation and 28 000e^-/lx·s sensitivity. This image sensor also realizes high-dynamic range readout procedure and in-pixel coded exposure for deblurred images. We also describe the examination results about the relationship of the sensitivity, parasitic light sensitivity, and LG structure.**

***Index Terms*— Adaptive signal detection, CMOS image sensors, CMOS integrated circuits, image enhancement, image quality, image restoration, linearization techniques, optical design.**

I. Introduction

CMOS image sensors (CISs) with global shutter (GS) function are required in a variety of areas, including broadcasting, automobile, drones, and surveillance applications. For these applications, image accuracy (e.g., simultaneity, synchronization) is strongly demanded, and GS CISs are needed to avoid rolling shutter (RS) distortion and flash band effect (Fig. 1). These applications also benefit from the high image quality (e.g., 80-dB dynamic range) and high frame rates (e.g., 60 fps) of GS CISs [1]–[4]. To realize a GS CIS, a memory structure (MEM), additional MOS transistors [overflow gate (OG), GS], and additional drive lines (OG, GS, and overflow drain) are necessary in each pixel (Fig. 2). Due to this increase in the number of components, photodiode (PD) area and aperture are restricted. Therefore, sensor performance (e.g., noise, sensitivity, and saturation) of GS CISs has generally remained inferior to that of RS sensors. To break down this constraint, we introduce a multiple-accumulation shutter technique for GS CISs [5], [6] and the optimized shape light guide (LG) structure [6], [7]. Furthermore, we combine the column single-slope analog digital converters (ADCs) with dual-gain amplifiers (SSDG-ADCs) [6], [8] to implement this shutter technique effectively, while also achieving low-power consumption less than 500 mW, a 60 fps frame rate with multiple-accumulation and a seamless exposure. Seamless exposure means that exposure period is approximately equal to a frame period, and does not have an intermission between frame and frame (Fig. 3). In Fig. 3, "n" means the number of multiple-accumulation times.

In this paper, we describe the sensor architecture in Section II, the details on the key technologies in Sections III and IV, the measurement results in Section V, the applications in Section VI and the summary in Section VII, respectively.

II. Sensor Architecture

Fig. 4 shows a block diagram of the GS sensor. The chip comprises a PD array, row and column decoders, pixel circuit drivers and multiple-accumulation shutter drivers, column 10 b SS-ADCs with dual-gain column amplifiers (12 b equivalent SSDG-ADC), column memories, signal processors, and a 1.2 V sub-low voltage differential signaling interface. The pixel array consists of 2676(H) × 2200(V) pixels. Fig. 4 also shows a schematic of the pixel. A pixel pitch is 3.4 μm and a unit pixel consists of a two-floating-diffusion (FD) shared pixel structure with charge-domain memories (MEM), OG, GS transfer gates and column output line (CL). To shorten readout period, two CLs are located in each column.

Fig. 5(a) shows a SSDG-ADC block and schematic and Fig. 5(b) shows a SSDG-ADC timing diagram.

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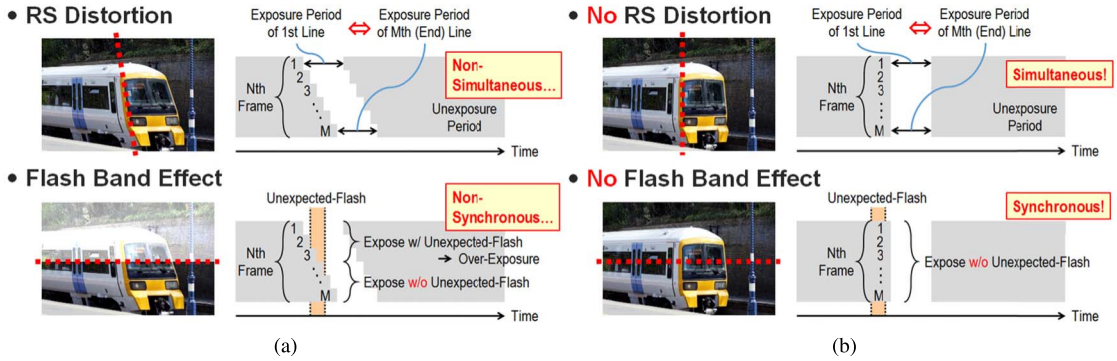

Fig. 1. RS problems. (a) RS CIS. (b) GS CIS.

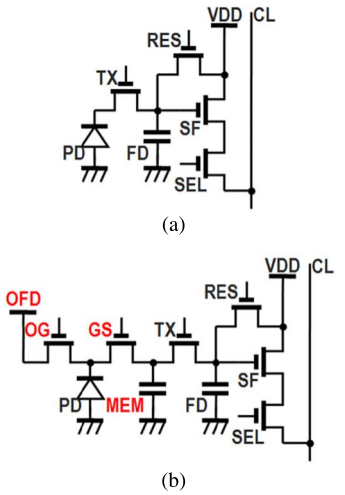

Fig. 2. Pixel schematic. (a) RS CIS. (b) GS CIS.

The column SSDG-ADC comprises a ramp generator, a dual-gain (unity or 4×) column pre-amplifier, a limit circuit, a comparator, and column memories. To reduce the power consumption, a common counter outputs multiple count signals with gray code to the column memories on each side with 972 MHz count frequency. For correlated double sampling (CDS), readout circuits operate noise readout period and signal readout period (S-AD) in each frame. In S-AD period, this architecture operates as follows: in low-brightness case (the column pre-amplifier output Vampo below the threshold level Lth), the column pre-amplifier gain Gamp is 4×, the comparator compares the output signal with the 10 b count, and the column memories store 10 b data. On the other hand, in high-brightness case (Vampo above the Lth), the limit circuit judge that Gamp changes from 4× to unity gain, and Vampo is suppressed. As a result, the comparator is able to compare the output signal with only 10 b count in both cases. Therefore, we are able to realize 12 b equivalent AD conversion with 10 b comparator, and the S-AD period is able to shorten 1/4 of the 12 b SS-ADC [Fig. 5(b)]. The limit circuit compares Vampo with Lth (equal to Vjdg + Vgs_M2) and clips Vampo in order to avoid pre-amplifier saturation. The Lth is 1000 LSB equivalency. The power increase of additional limit circuit is negligible, because most of the current consumed by the limit circuit is provided from the constant current source transistor M1 [Fig. 5(a)].

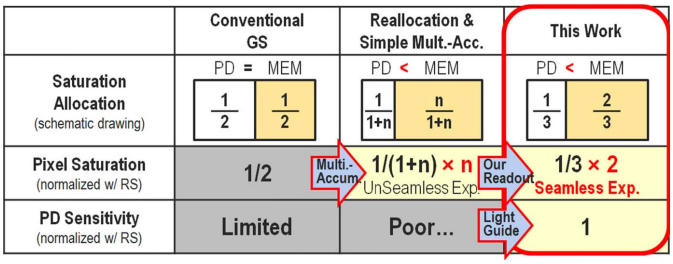

Fig. 3. Concept of this paper.

Fig. 6(a) shows a SSDG-ADC post processing block diagram in a signal processor. The signal processor does the following operations: gray-coded data decoding, digital CDS, and linearity compensation for dual-gain stitching. The output code is gained with a digital domain based on a judge result. Fig. 6(b) shows output characteristics without and with the linearity compensation. The linearity compensation to stitch the joint point is necessary, because the judge threshold level and ramp signal vary with various factors (e.g., temperature, process). The gap of the joint point deteriorates one of the ADC evaluation indexes differential non-linearity (DNL). The compensation parameters are slope (α) and offset (β). In high-brightness region, although the output code of SSDG-ADC shows four LSB discrete value by amplified (bit shift) according to column amplifiers' gain setting, the influence on image quality is slight, because photon shot noise is at least more than 30 LSB in this region.

III. Multiple-Accumulation Technology

Fig. 7(a) shows a timing diagram of conventional signal readout procedure, equivalent to a 60 fps drive for this sensor. During the S-AD from MEM to FD ($T_{READOUT}$), the PD accumulates the next frame charge. In this readout procedure, the period for retaining the signal in the MEM (T_{RETAIN}) is as long as the $T_{READOUT}$, and the signal charge is retained in either line(s). Therefore, the signal charge transfer from PD to MEM is once in a frame, and the signal saturation of the PD is as much as that of the MEM. Fig. 7(b) shows a timing diagram of a multiple-accumulation shutter readout procedure. In this procedure, the readout period is cut in half for seamless exposure, but the saturation of the pixel about

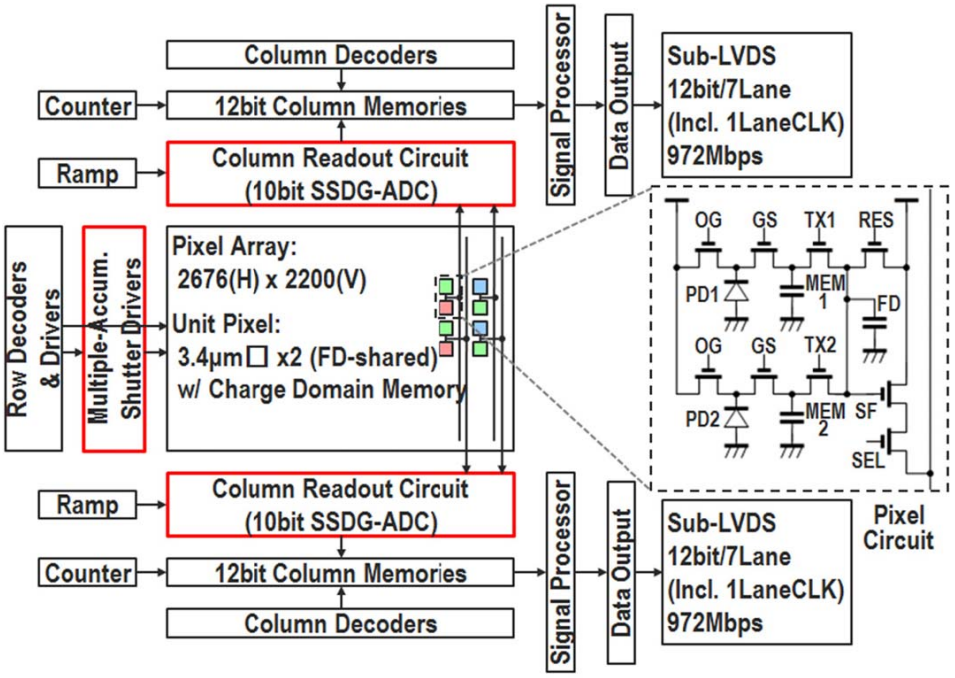

Fig. 4. CIS block diagram.

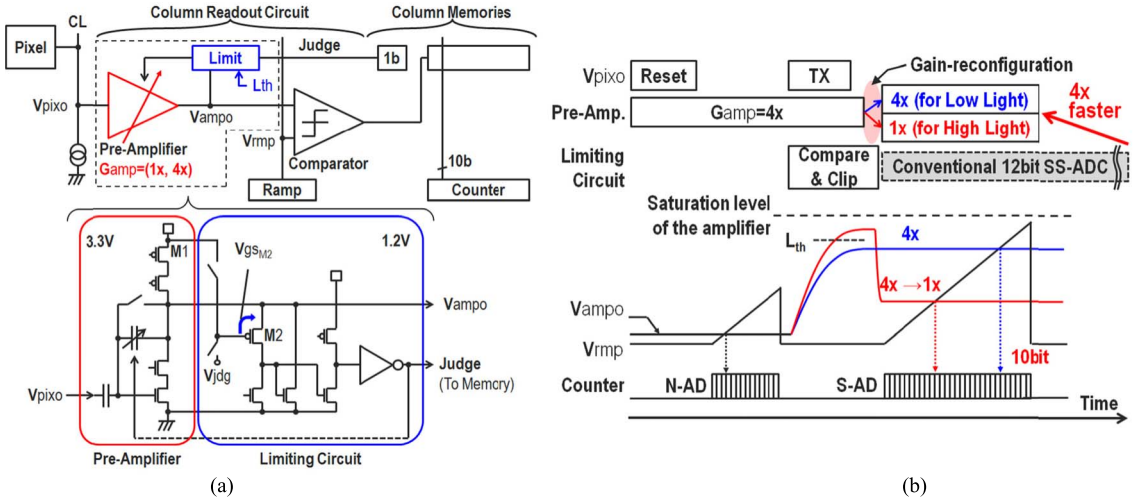

Fig. 5. SSDG-ADC diagrams. (a) Block and circuit diagram. (b) SSDG-ADC timing diagram.

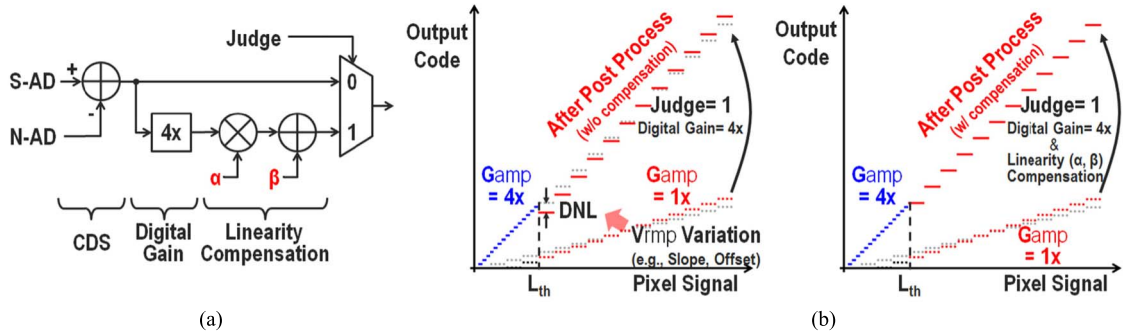

Fig. 6. SSDG-ADC post process in signal processor. (a) Block diagram. (b) Output characteristics (with out and with compensation).

twice as large as the saturation level of PD by the adoption of the SSDG-ADC. Specifically, the frame rate is 60 fps, and the ratio of $T_{RETAIN}/T_{READOUT}$ is about 2. Since the MEM is empty after $T_{READOUT}$, the MEM can retain the signal charge of the "next" frame seamlessly. Hence, the number of transfers from PD to MEM can be multiplied. In Fig. 7(b), the number of GS pulses is doubled for equal transfer intervals.

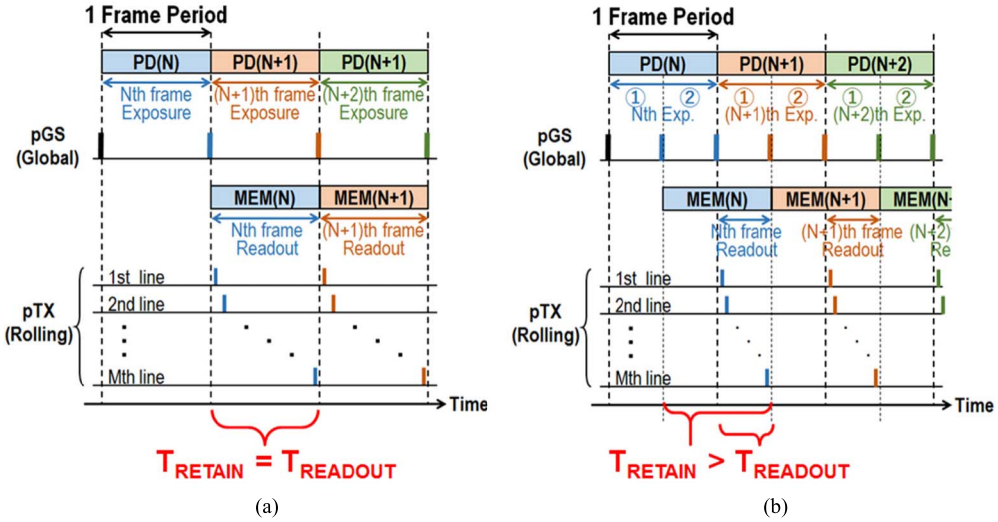

Fig. 7. Signal readout procedure. (a) Conventional signal readout. (b) Multiple-accumulation signal readout.

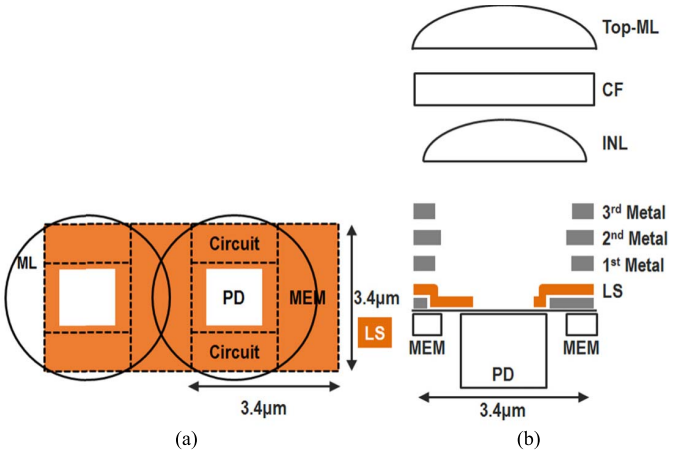

Fig. 8. Pixel structure diagrams without LG structure. (a) Top-view diagram. (b) Cross-section diagram.

IV. Light Guide Structure Design

Fig. 8(a) and (b) shows the top-view and the cross-section diagram of the pixel. The pixel pitch is 3.4 μm and the PD area is only about 25% of the pixel. Generally, in the GS pixel, there is a LS structure to avoid parasitic light for memory. The PD aperture size is limited by LS placement. To guide the incident light for the PD, we examined to adopt a high refractive index material based LG structure.

Fig. 9 shows three types of a LG structure: a medium top (2.2 μm) and wide bottom (1 μm) with steep slope [Fig. 9(a)], a narrow top (2 μm) and narrow bottom (0.8 μm) with steep slope [Fig. 9(b)], and a wide top (2.4 μm) and narrow bottom (0.8 μm) with gentle slope [Fig. 9(c)]. Furthermore, the LS aperture width is 1.3, 1.1, and 1.1 μm, respectively. In addition, the structure of the top lens, the inner lens, the PD, and the wiring layers assumed the same design in all types.

Fig. 10(a) and (b) shows the simulated results of incident light angle dependence of sensitivity and parasitic light sensitivity (PLS), respectively. The simulation was carried out with single wavelength of 550 nm (green) based on the 3 D finite-difference time-domain method. The structure (a) is advantageous in sensitivity, however, the PLS performance is remarkably inferior to the structure (c). Moreover, the structure (b) is inferior in both sensitivity and PLS performance to the structure (c). Therefore, the wide LG structure in both top side and bottom side is important for the sensitivity improvement. On the other hand, the narrow LG structure in bottom side and MEM covering width with LS are important for the PLS improvement. We adopted the well-balanced structure (c) in this case.

V. Pixel Performance

The measured photoelectric conversion characteristics of the fabricated GS sensor are shown in Fig. 11(a), (b), (c), and (d). For 120 (single-accumulation shutter) and 60 fps (multiple-accumulation shutter), the saturation signal is 8100e^- and 16 200e^- (twice), respectively. In 120 fps output result, we are able to confirm the 12 b equivalency signal output (about 4000 LSB). In addition, the sensitivity, the dark temporal noise, and the (PLS) are 28 000e^-/lx $\cdot$ s in green pixel, 1.8e^-_{rms}, and -89 dB, respectively, with no difference between the two procedures. We used a International Commission on Illumination light source A (2856 K) for the measurement. The DNL at joint point (Lth), column fixed pattern noise and row temporal noise are -1.3 LSB/+1 LSB, 0.05 LSB and 0.07 LSB with SSDG-ADC and linearity compensation, respectively. Furthermore, in case of short exposure period, of course we are able to achieve the high saturation without frame rate lowering by using multiple-accumulation. For example, in case of 1/120 s accumulation period, we are able to achieve both the 16 200e^- saturation signal and 120 fps frame rate with 2$\times$ accumulation shutter.

Fig. 12 shows the simulated light intensity profiles of 15° incident light angle with and without LG structures. The 15° incident light angle is approximately equivalent to f-number less than 1.8. The incident light angle dependence

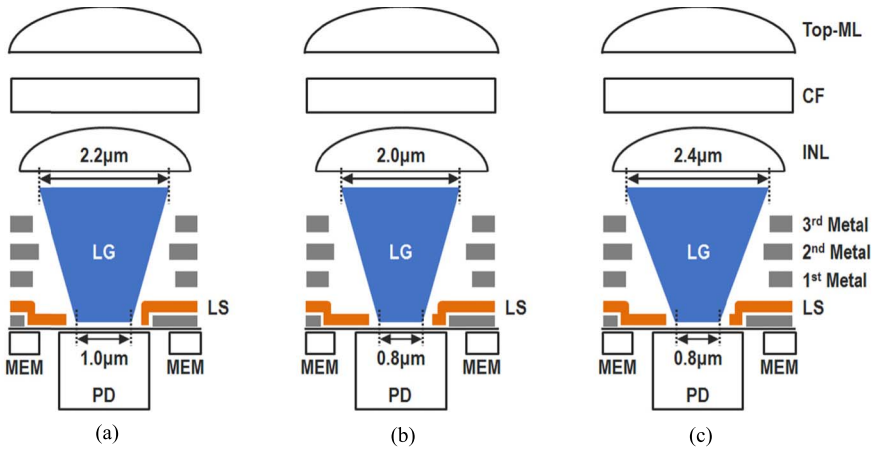

Fig. 9. Three types of candidate pixel structure with LG structure. (a) Top/Bottom: 2.2/1 μm, steep slope. (b) Top/Bottom: 2/0.8 μm, steep slope. (c) Top/Bottom: 2.4/0.8 μm, gentle slope.

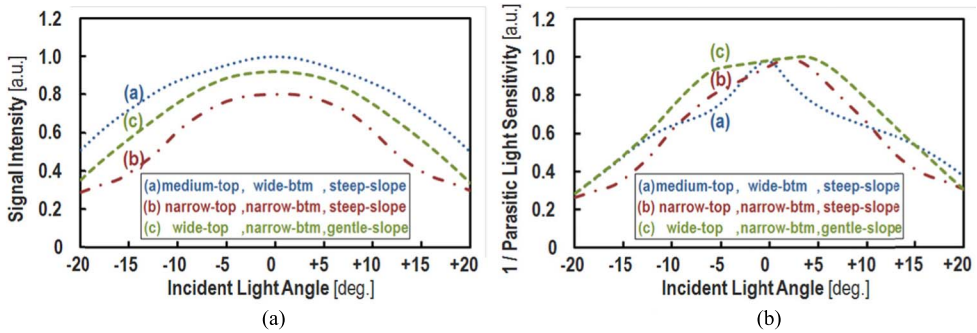

Fig. 10. Simulated sensitivity and PLS results of incident light angle dependence. (a) Sensitivity simulation results. (b) PLS simulation results.

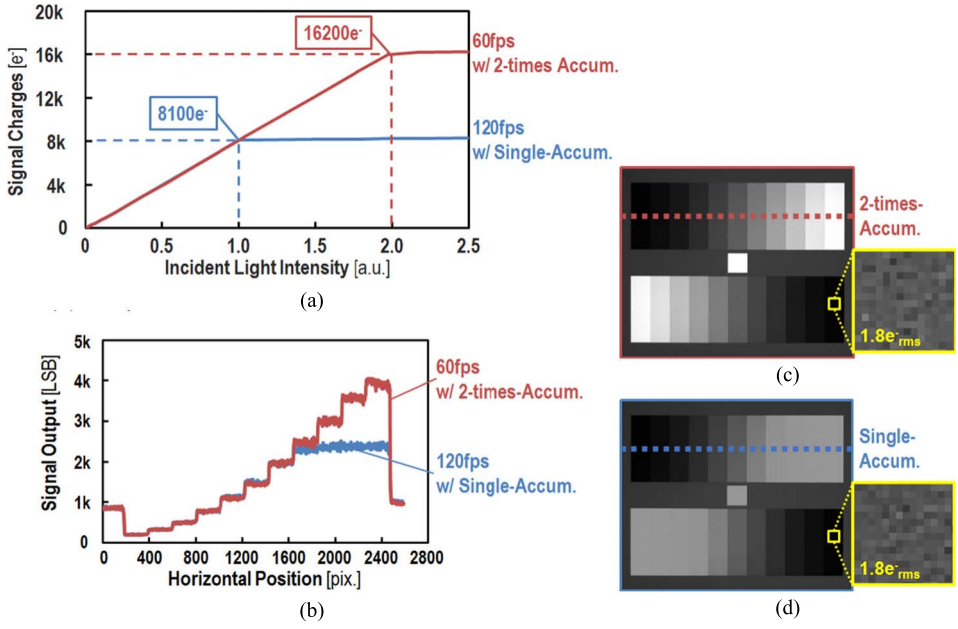

Fig. 11. Photoelectric conversion characteristics and dark temporal noise measurement results. (a) Photoelectric conversion characteristics. (b) Gray-scale chart measurement results. (c) 2× multiple accumulation image. (d) Single-accumulation image.

is one of the important indexes for surveillance cameras with wide-angle lens. As evident from Fig. 12, the LG structure is very effective for the PD sensitivity.

Fig. 13(a) and (b) shows the measured and the simulated results of incident light angle dependence with and without LG structures about sensitivity and PLS, respectively.

TABLE I
FABRICATED CIS PERFORMANCE

Process Tech.	**130**nm CMOS **1P4M** + **LS**	
Optical Format	**2/3** inch	
Pixel Pitch	**3.4** μm	
Num. of Eff. Pixels	**2592** (H) x **2054** (V)	
Power Supply	**3.3** V (analog), **1.2** V (digital)	
Max. Frame Rate	**120** fps w/o mult.-accum.	**60** fps w/ mult.-accum.
Power Consumption	**450** mW w/ full pixel readout	
Full Well Capacity (per unit area)	**8100** e^- (**700** $e^-/\mu m^2$)	**16200** e^- (**1400** $e^-/\mu m^2$)
Sensitivity (per unit area)	**28000** $e^-/lx \cdot s$ (**2420** $e^-/lx \cdot s \cdot \mu m^2$)	
Temporal Noise	**1.8** e^-_{rms} w/ SSDG-ADC	
Dynamic Range (High-DR mode)	**73.1** dB w/o mult.-accum.	**79.0** dB (**111** dB) w/ mult.-accum.
Parasitic Light Sensitivity	**-89** dB	

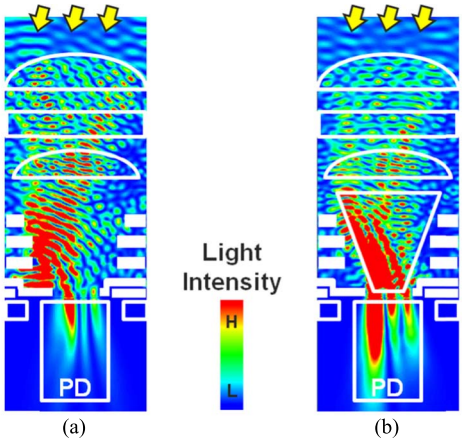

Fig. 12. Simulated light intensity profile (Incident light condition is 15°). (a) Without LG structure. (b) With LG structure.

As the effect of the LG structure, the normalized sensitivity ratio of 15° incident light to the perpendicular light is improved from 21% (simulation without LG) to 62% (measured with LG) [Fig. 13(a)]. The measured results agreed very well with the simulation results. Furthermore, the normalized PLS ratio is improved from 6.9% (simulation without LG) to 36% (measured with LG) [Fig. 13(b)]. There is a discrepancy between the measured results and the simulation results. This discrepancy is thought to be the influence of the incident light except "green" wavelength. In addition, the PLS characteristics are not symmetric. This asymmetry depends on the presence of the GS transfer gate.

Table I lists the fabricated CIS performance.

VI. SENSOR APPLICATIONS

Fig. 14(a) shows a timing diagram and Fig. 14(b) shows a captured high-dynamic-range (HDR) image using short (84 μs) exposure with the multiple(2×)-accumulation shutter and long (8.3 ms) exposure with a single-accumulation readout procedure. By using the multiple-accumulation shutter, we are able to use full-well capacity effectively. Although, the exposure period is not seamless and blur may occur to fast-moving objects in this case, this procedure is a useful and simple HDR method for static and slow moving objects. According to the calculation from the ratio of accumulation period (about 100×), the dynamic range improvement is about 40 dB. On the other hand, we allocated about 8 dB overlap for the stitching point to be hardly noticeable. As a result, the dynamic range increases from about 79 dB in 60 fps with the multiple-accumulation procedure to 111 dB in 60 fps for the HDR procedure. In this case, the SNR drop at the stitching point is about 12 dB and malfunction such as unexpected coloring and stitching gap did not occur. In the synthesized HDR image, we are able to recognize the LED light source shape and white shell design in a bright area (close-up A), and the flower vase texture and turtle shell design in a dark area (close-up B).

Fig. 15(a) shows a timing diagram and Fig. 15(b) shows a captured in-pixel coded exposure [9] image with the multiple-accumulation shutter. The coded exposure is one of the deblurred technologies and uses to remove "blur" in Fourier space division (deconvolution). In this case, the train runs toward the left side from the right side, its moving speed is equivalent to 60 km/h, and the exposure period is not seamless. The multiple-accumulation and in-pixel MEM are suitable for the in-pixel coded exposure. We prepared 16× shutter operation for various applications and, in this case, used 13× multiple-accumulation and 52 b coded exposure [9]. The single-accumulation has 100-ms accumulation period and the coded exposure has a total of 50-ms accumulation period. The deblur processing was carried out with external system. Without in-pixel coded exposure, the deblurred image quality deteriorates by the deconvolution noise (zero data in Fourier space). On the other hand, we are able to recognize the numbering of the moving train in the deblurred image with in-pixel coded exposure. Peak signal-to-noise ratio in zoomed-up images is 16 and 24.6 dB, respectively. This shows the in-pixel coded exposure method works well. This procedure is suitable for the surveillance applications.

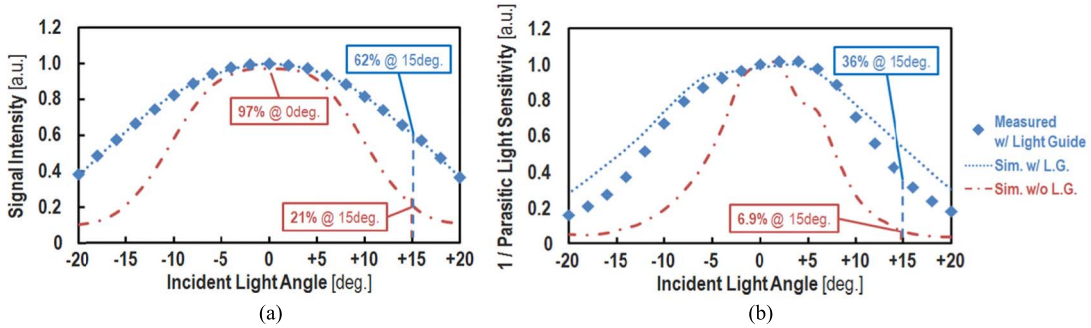

Fig. 13. Measured and the simulated sensitivity results of incident light angle dependence. (a) Sensitivity results. (b) PLS results.

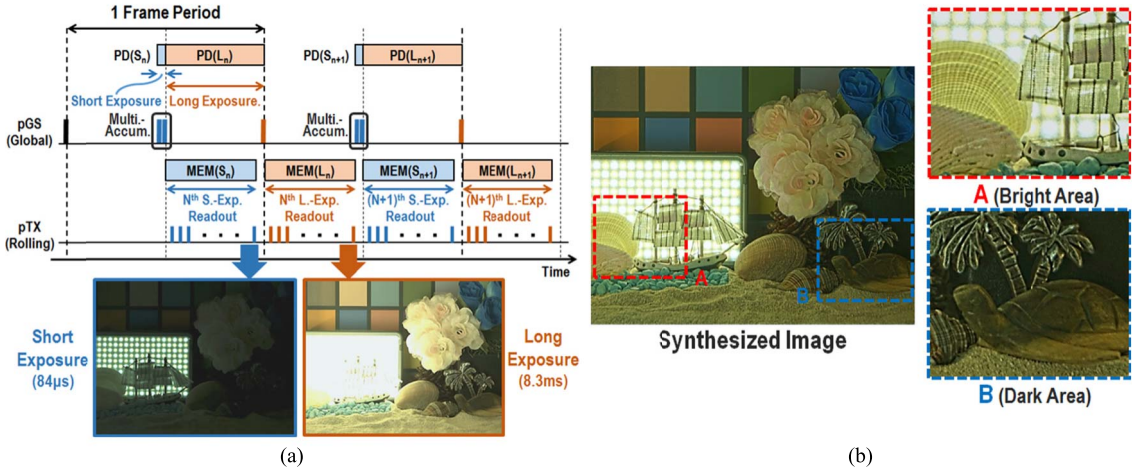

Fig. 14. High-dynamic range application. (a) HDR readout timing diagram. (b) 110 dB over dynamic range synthesized image.

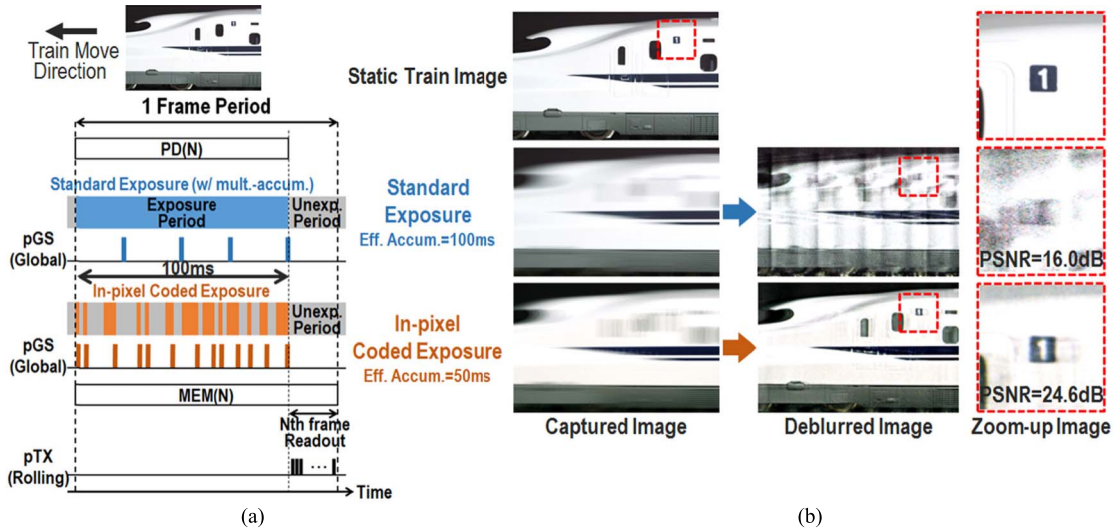

Fig. 15. In-pixel coded exposure application. (a) In-pixel coded exposure-timing diagram. (b) Captured and deblurred images.

VII. Summary and Conclusion

Table II lists the performance comparison of recently published CISs [1], [3]–[5], [10]. The measured chip power consumption is 450 mW at a frame rate of standard 120 fps mode and 60 fps with the multiple-accumulation shutter. In each mode, FOM1 of 1.27e$^-$ and 2.54e$^-$ · nJ are achieved, respectively, when FOM1 is defined as (power × noise × 10^9)/(number of effective pixels × fps). Furthermore, FOM2 of 0.28e$^-$ and 0.29e$^-$·pJ are achieved, respectively, when FOM2 is defined as (power × noise × 10^{12})/(number of effective pixels × fps)/(full-well capacity/noise). Based on the recent results in Table II, the FOMs of the fabricated image

TABLE II
PERFORMANCE COMPARISON OF RECENTLY PUBLISHED CISs

	unit	This work		[5] IEDM 2016 K. Kawabata, et al.		[4] VLSI 2016 Y. Oike, et al.	[3] IISW 2013 P. Centen, et al.	[1] ISSCC 2012 M. Sakakibara, et al.	[10] ISSCC 2016 T. Arai, et al.
Shutter Function	-	GS		GS		GS	GS	GS	RS
Pixel Pitch	μm	3.4		6.4		5.86	5	6.4	1.1
Num. of Eff. Pixels	-	2592 x 2054		3960 x 2400		3840 x 2160	1920 x 1080	3840 x 2160	7728 x 4368
Max. Frame Rate	fps	120	60	120	30	480	240	60	240
Full Well Capacity (per pixel area)	e^- ($e/\mu m^2$)	8100 (700)	16200 (1400)	19000 (460)	70000 (1700)	30450 (890)	15000 (600)	32200 (790)	5700 (4710)
Sensitivity (per pixel area)	$e^-/lx \cdot s$ ($e/lx \cdot s \cdot \mu m^2$)	28000 (2420)		80000 (1950)		17500 (510)	54250 (2170)	78000 (1900)	6000 (4960)
Temporal Noise	e^-_{rms}	1.8		1.8		4.6	4	4.8	3.6
Dynamic Range (HDR mode)	dB	73.1 -	79.0 (111)	80.4 -	91.7 -	76.3 -	71.5 -	76.5 (83.0)	64 -
Power Consumption	W	0.45		1.5		5.23	1.1	2.0	3.0
Figure of Merit 1	$e^- \cdot nJ$	1.27	2.54	2.37	9.47	6.04	8.84	19.29	1.33
Figure of Merit 2	$e^- \cdot pJ$	0.28	0.29	0.22	0.24	0.92	2.36	2.88	0.84

FoM1= Power[W] x DRN[e^-] x 10^9 / (FPS[s^{-1}] x Num. of Eff. Pixels)
FoM2= Power[W] x DRN[e^-] x 10^{12} / (FPS[s^{-1}] x Num. of Eff. Pixels x DRU); DRU=FWC[e^-] / DRN[e^-]

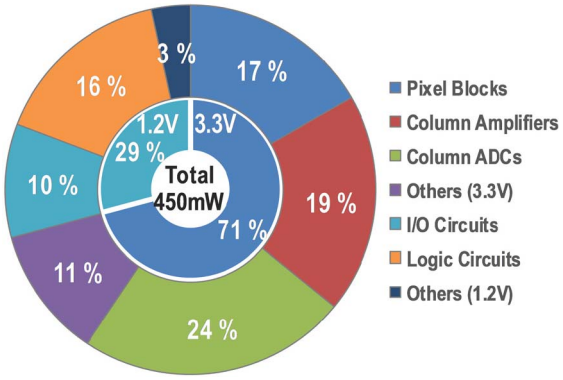

Fig. 16. Power consumption breakdown.

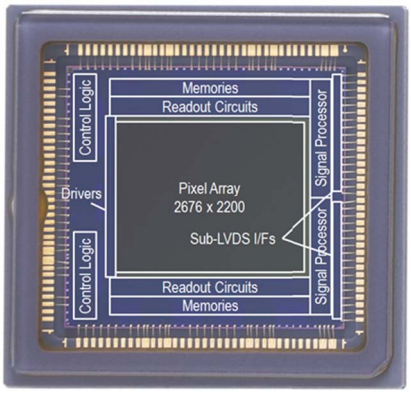

Fig. 17. Chip-package photomicrograph.

sensor are comparable or better than those of others, in spite of the addition of the GS function and the pixel size shrinkage.

Fig. 16 shows a power consumption breakdown. The column ADCs, pre-amplifiers, pixel blocks, and logic circuits account for 24%, 19%, 17%, and 16% of total power consumption, respectively. By the adoption of the common gray-code counter, we realized approximately 40% of power saving as ADC blocks. A chip-package photomicrograph is shown in Fig. 17.

We realized both the GS function and the high sensor performance. Specifically, we achieved high saturation, high sensitivity, and low temporal noise. Furthermore, we demonstrated useful application, high-dynamic range operation and in-pixel coded exposure.

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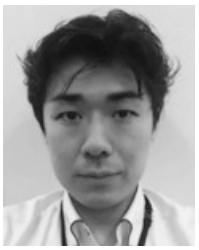

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