A Wirelessly Powered UWB RFID Sensor Tag With Time-Domain Analog-to-Information Interface

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***Abstract*— This paper presents a wirelessly powered radio frequency identification sensor tag with an analog-to-information interface. A time-domain interface, incorporating an ultra-low-power impulse radio ultra-wideband (IR-UWB) transmitter (TX), is employed. The analog signal from the sensor is compared with a triangular waveform, resulting in a pulse-position modulation signal to trigger UWB pulses. Thanks to the high time-resolution IR-UWB radio, time intervals of the impulses can be used to represent the original input value, which is measured remotely on the reader side by a time-of-arrival estimator. This approach not only eliminates the analog-to-digital converter (ADC) but also significantly reduces the number of bits to be transmitted for power saving. The proposed tag is fabricated in a 0.18-μm CMOS process with an active area of 2.5 mm^2. The measurement results demonstrate that a 300-kS/s sampling rate with a 6.7-bit effective number of bits (ENOB) is obtained via a UWB receiver with a sensitivity of −93 dBm and an integration window of 10 ns. The ENOB is improved to 7.3 bits when the integration window is reduced to 2 ns. The tag can be powered up by a −18-dBm UHF input signal. The power consumption of the proposed tag is 41.5 μW yielding a 1.3-pJ/conv.step figure of merit, offering 9× and 67× improvements compared with the state of the art based on an ADC and a backscattering TX, and the tag based on an ADC and a narrowband TX, respectively.**

***Index Terms*— Energy harvesting (EH), pulse position modulator, Radio Frequency IDentification (RFID), time domain, ultra-wideband (UWB), UWB transmitter (TX), wireless sensing.**

I. Introduction

WIRELESS sensing and Radio Frequency IDentification (RFID) are the key technological enablers in realizing the vision of the Internet of Things (IoT) [1]. Tiny RFID tags with sensors will be embedded into our daily objects or even be implanted into human bodies, monitoring health and the surrounding environment [2], [3]. Although they show a great potential, sensor tags have many design challenges, which impede their widespread adoption. One of the most critical issues is to implement an energy-efficient tag with medium resolution and a high data rate. For example, a 256-channel electrocorticogram recording device with a 500-Hz bandwidth for each channel, an 8-bit resolution, a sampling rate of 256 kS/s, and a corresponding data rate of 2 Mb/s is required. Therefore, the goal of this paper is to demonstrate a sensor tag, which can provide an 8-bit resolution with a sampling rate exceeding 256 kS/s, while the power consumption is under 100 μW. The effective data rate is higher than 2 Mb/s.

To eliminate the battery requirement, tags should be in an energy-autonomous manner with a microwatt-level power budget, for example, harvesting energy from an ambient environment, such as thermal gradients or mechanical vibrations [4], [5]. Meanwhile a traditional wireless sensing device usually consists of a Nyquist-rate analog-to-digital converter (ADC)-based signal recording block, a digital signal processing (DSP) block, and an RF transmitter (TX). Typically, these functions consume 16%, 10%, and 74%, respectively, of the total power [6]. Such an architecture is more complex than an RFID tag, while its power consumption is far beyond the energy budget for energy-autonomous devices. Moreover, Nyquist-sampling ADC produces a huge amount of raw data, which need to be further transmitted, dramatically increasing the burden of wireless communication and resulting in the TX's power dominance. Even with the most energy-efficient TX [except ultra-wideband (UWB), which provides pJ/bit energy efficiency] [7], the energy consumption per bit is still in the range of several hundred pJ/bit during ON-state mode [8], which is orders of magnitude higher than other parts. Therefore: 1) reducing the amount of data sent and 2) the extremely low-power TX design are the most effective methods in realizing the energy autonomous wireless sensing applications.

A substantial amount of research work has focused on energy-efficient sensor interfaces and TXs as individual blocks [9], [10]. Conventional RFID-like RF-powered devices employ ADCs and backscatter techniques, as shown in Fig. 1(a) [11]. However, radio signals are transmitted for each data bit, which is limited in low-power applications with high sampling rate requirements. Sensor nodes equipped

Manuscript received July 10, 2017; revised November 27, 2017 and February 20, 2018; accepted March 28, 2018. Date of publication May 7, 2018; date of current version July 20, 2018. This paper was approved by Associate Editor Azita Emami. This work was supported in part by the NSFC under Grant 61571137, in part by the Shanghai Pujiang Program under Grant 17PJ1400800, in part by the Key Project of Shanghai Science and Technology Innovation Plan under Grant 15JC1400101, and in part by the JSSF Project under Grant 20150164. *(Corresponding author: Zhuo Zou.)*

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Digital Object Identifier 10.1109/JSSC.2018.2825455

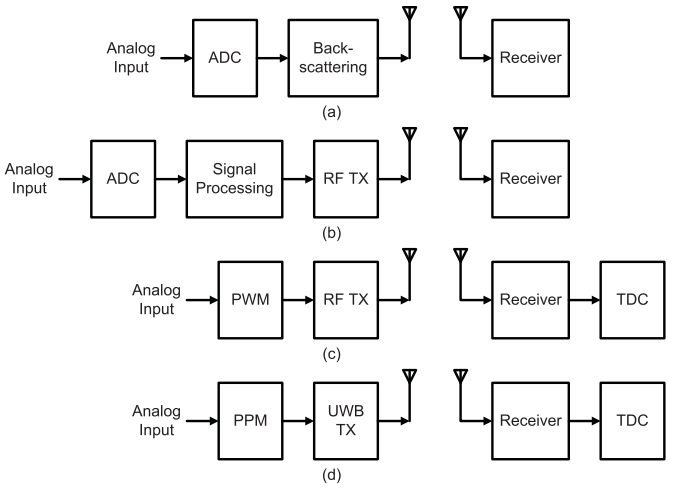


Fig. 1. Wireless sensing systems based on (a) ADC and backscattering, (b) ADC, on-node processing, and RF TX, (c) PWM and FSK TX, and (d) proposed PPM and UWB TX.

with an RF TX are presented in [12] with a higher data rate, at the cost of high power consumption. More recently, sophisticated functions, such as data compression and feature extraction, have been demonstrated to reduce the amount of data transmitted as shown in Fig. 1(b) [13], [14]. However, this incurs information loss and requires extra hardware on the tag. In [15], a clockless system converts the sensed data into pulsewidth modulation (PWM) signals and transmits them by frequency-shift keying (FSK) carrier as illustrated in Fig. 1(c). Hence, the time-to-digital converter (TDC) is moved to the receiver side resulting in power saving for the sensor tag. Nevertheless, the narrowband FSK TX is still complex and power-hungry. An RC-based time-domain sensing interface was presented [16]. It employs an RC time constant interface to convert the sensor information into time intervals by measuring the discharging time of the RC circuits. However, a local reference clock is still needed for the discrete-time comparator which limits the sampling rate and the system resolution.

In this paper, we present a wirelessly powered UWB sensor tag with an analog-to-time interface, as shown in Fig. 1(d). Pulse-position modulation (PPM) is employed to convert the analog signal into a pulsing signal with various pulse positions, which is then transmitted by an ultra-low-power impulse radio ultra-wideband (IR-UWB) TX. The proposed system reduces the number of pulses to be sent from N (the ADC's resolution in bits) to 2, without scarifying the system resolution thanks to the high time-resolution UWB pulses. Moreover, the TDC is moved to the reader side, which further degrades the tag's power consumption [17]. The quantization is performed by the reader using a time-of-arrival (ToA) estimator as a TDC. To verify the system concept, the tag is implemented in a 0.18-μm CMOS process. A 300-kS/s sampling rate with 6.7-bit effective number of bits (ENOB) is achieved by using a software-defined radio (SDR) UWB receiver with -93-dBm received power and a 10-ns ToA integration window, while the power-up sensitivity is measured as -18 dBm. The effective data rate is 2 Mb/s. The total power consumption is 41.5 μW, yielding a 1.3-pJ/conv.step figure-of-merit (FOM). The ENOB can be elevated to 7.3 bits by reducing the integration window to 2 ns, resulting in an FOM of 0.9 pJ/conv.step.

The remainder of this paper is organized as follows. The proposed PPM-UWB approach is discussed in Section II. This is followed by a circuit description in Section III. The measurement results are elaborated in Section IV, with conclusions given in Section V.

II. System Description

A. Architecture of PPM-UWB Wireless Sensing System

Fig. 2(a) shows the system concept of the PPM-UWB sensing system. By comparing the analog signal with a tunable triangular waveform (TW), the sensor information is represented by a time-domain signal with variable pulse positions. A pulser generates narrow pulses with different time intervals at each rising edge of the TW signal or per falling edge of the PPM signal. The pulser's output is then fed to a simple UWB TX as a drive signal. The short duration of UWB pulses enables accurate ToA estimations [18]. Thus, on the reader side, the intervals of received pulses are measured by means of ToA estimation as a TDC. Such a design basically makes use of the voltage-to-time conversion part of a traditional single-slope ADC, yet moves the power-hungry TDC to the reader side. For the conventional single-slope ADC, the design is usually aimed at a precise clock and a TW with high linearity, thus a high-speed reference clock is normally used [19]. In the presented design aiming for extremely low cost and low power, a triangular wave generator (TWG) based on the relaxation oscillator architecture is employed, because it provides a relatively high-accuracy clock compared with a free-running ring oscillator but consumes far less power consumption compared with a phase-locked loop (PLL). The TWG used in this paper also eliminates the high gain–bandwidth-product feedback amplifiers (used in [20]) to simplify the circuit at the expense of non-linearity issues. The dual-slope architecture [21] can also be considered in such a system. It is more tolerant to RC variations, yet it needs two steps for each conversion and requires three pulses per sample compared with two in the single-slope architecture used in this paper.

The proposed architecture offers the following advantages over the conventional methods: 1) an IR-UWB TX featuring much lower power consumption compared with a narrowband TX is used to emit pulses, leading to significant power reduction; 2) as the high time-domain resolution UWB pulses facilitate accurate ToA estimations, thus only two pulses are sent for each sampling, reducing the number of pulses transmitted; 3) the burden of the TDC is moved to the reader side to minimize the power of the tag; and 4) the TWG circuit can be greatly relaxed, because it can be calibrated wirelessly on the reader side to improve linearity. Moreover, no local oscillator is required.

B. PPM-UWB Tag Operation

Fig. 2(b) demonstrates the operation principle of the PPM-UWB tag: 1) the system sampling rate is the frequency

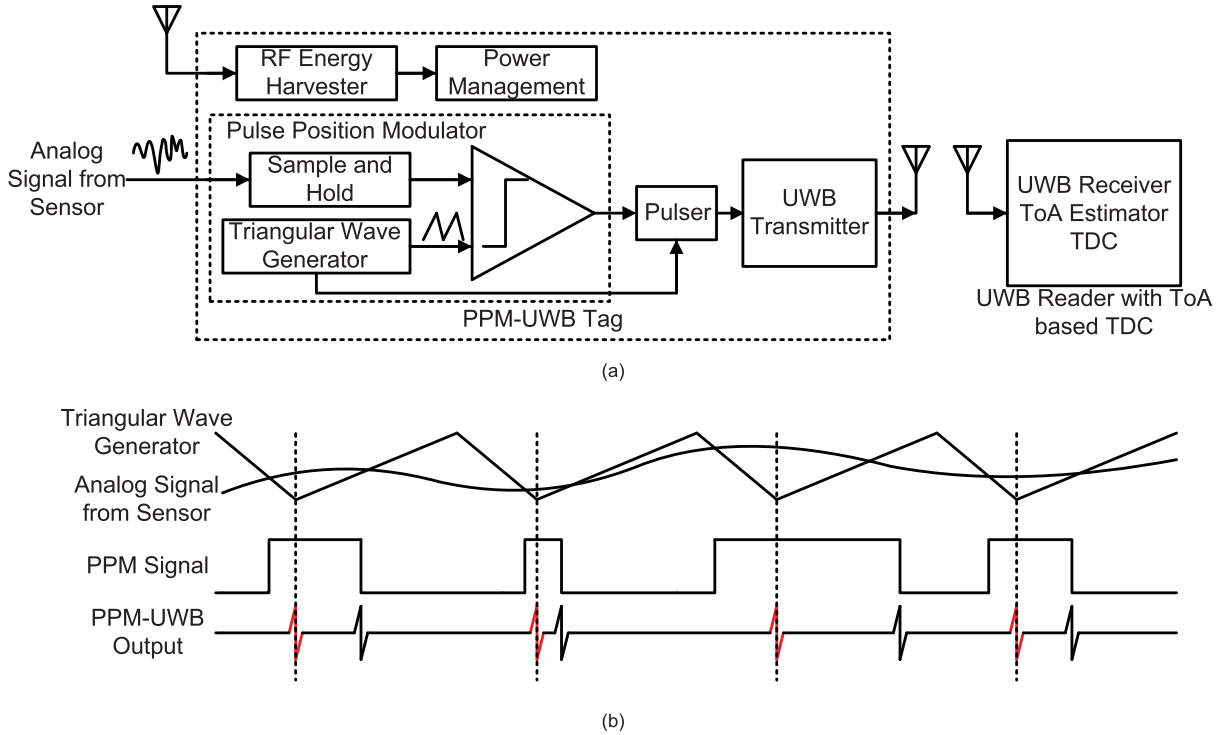


Fig. 2. (a) System architecture of the proposed PPM-UWB system. (b) Signaling of the reader and tag.

of the TWG that can be specified by the reader; 2) the pulses that are triggered by the rising edge of the TW and the falling edge of the PPM signal and their position represent the sensor signal; 3) the first pulse is a reference pulse indicating the beginning of the TW, which is used for reader-tag synchronization (see the red ones). Therefore, only two pulses are sent for each sample. When transmitting N-bit data (where N is the ADC's resolution in bits), the transmitting power is reduced by $N/2$ times compared with conventional digital encoding schemes.

C. Performance Analysis

In a wirelessly powered tag system, the operating distance is mainly determined by the tag's sensitivity toward powering up, the pulse swing transmitted by the tag, and the reader's sensitivity (minimal input power to detect pulses and estimate to ToA). In the downlink, aiming at a 2-m operating distance for readers with 20-dBm effective isotropic radiated power (EIRP) in the 915-MHz frequency band, a power-up threshold of approximately -18 dBm of the tag should be guaranteed. In the uplink, assuming that the peak power spectrum density is -60.4 dBm/MHz and the -10-dB bandwidth is 3.4 GHz at a pulse rate of 10 MHz [22], the transmitted power approximates to -60.4 dBm/MHz $+10\log_{10}$ (3400) MHz $= -25.1$ dBm, then -40.3 dBm of power will be emitted at a pulse rate of 300 kHz. The receiver sensitivity of the reader should be better than -92 dBm with 4.5-GHz radio center frequency when aiming at an operating distance longer than 2 m.

In the proposed time-domain system, the time quantization of PPM-UWB pulses on the receiver side is implemented by ToA estimation. The ToA estimation error depends on: 1) the time quantization intervals of the ToA estimator in the TDC and 2) the signal-to-noise ratio (SNR) degradation of the RF signal due to the wireless propagation.

We first analyze the case that the ToA estimation in the noise-free environment. This design is similar to a single-slope ADC [23]. The basic idea is to generate a TW, which is then compared against the analog input by a comparator. The upper and lower limits of the TW are tunable, based on the swing range of incoming signals, in order to maximize the dynamic range [20]. If non-ideal factors are ignored and the TW range is slightly larger than the dynamic range of the input signal, the resolution can be calculated by

$$n = \log_2\left(\frac{T_r}{T_s} \times \frac{T_s}{T_q}\right) = \log_2\left(\frac{T_r}{T_q}\right) \tag{1}$$

where T_r is the rising part of the TW, which is used for input signal quantization in this system, T_s is the sampling period, and n is the system resolution in bits. The time-domain ADC only occupies a certain part of the full-scale time range T_s. T_q is the quantization clock that is realized by the reader. The resulting resolution is shown in Fig. 3. For instance, to meet a 7-bit resolution requirement with a 200-kS/s sampling rate for the PPM-UWB tag, T_q needs to be less than 25 ns. If the sampling rate of the system increases to 500 kS/s, T_q of 10 ns is then necessary to guarantee 7-bit resolution. The tradeoff between the sampling rate and the resolution is illustrated in Fig. 3. However, the real time-domain systems suffer from noise and distortion. In a conventional ADC, the effective number ENOB is usually employed to evaluate the dynamic range. Similarly, the time SNR (TSNR) and the ENOB of time-domain systems are given in the following to measure the corresponding performances.

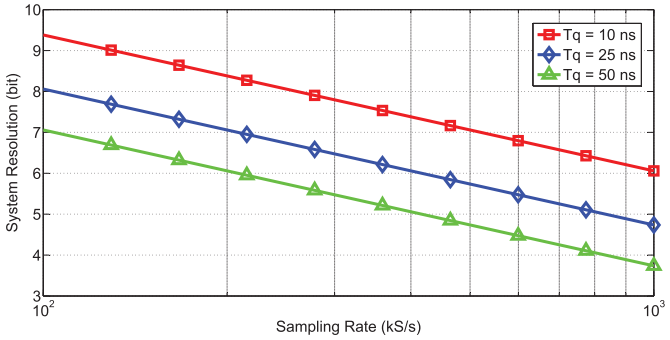


Fig. 3. System resolution versus sampling rate and ToA integration window for PPM-UWB approach where $T_r/T_s = 2/3$.

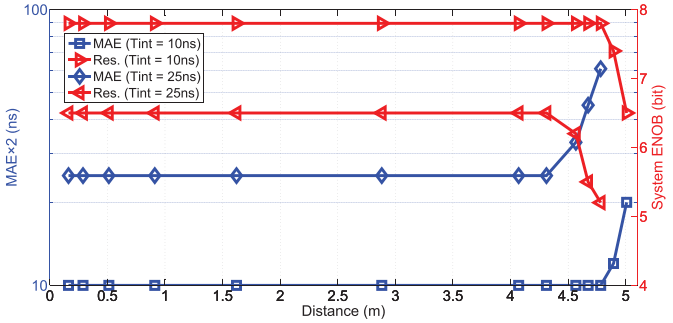


Fig. 4. MATLAB simulations of system ENOB and MAE versus distance and T_{int} for $fs = 300$ kS/s and $T_r/T_s = 2/3$ using MES ToA estimation.

The quantization error can be introduced from both the initial and the final time of an event taking place. In the proposed system, as the initial time is given with a precise value by high-accuracy synchronization, thus only the errors of the final time need to be considered. Assuming that the time full-scale range is T_{FSR} and the input time-domain signal is uniform distribution between 0 to T_{FSR}, while the quantization error T_e is assumed to be uniform distribution between 0 and T_q, then the ideal mean absolute error (MAE) of time-domain quantization $T_{e,\text{MAE}}$, and TSNR can be expressed as:

$$\text{TSNR} = 20\log_{10}\left(\frac{T_{\text{in,MAE}}}{T_{e,\text{MAE}}}\right) = 20\log_{10}\left(\frac{\frac{T_{\text{FSR}}}{2}}{\frac{T_q}{2}}\right)$$
$$= 20\log_{10}\left(\frac{T_{\text{FSR}}}{T_q}\right) \approx 6.02 \times n \ dB \quad (2)$$

where n is the number of bits of system resolution. The TSNR is similar to the SNR in a traditional ADC [24]. According to (2), a larger time range T_{FSR} or a smaller quantization time T_q is preferred in order to obtain a higher TSNR.

Similar to the definition of ENOB for ADCs [25], the ENOB of the time-domain system can be obtained by the following expression, where the measured MAE value of time-domain quantization is used:

$$\text{ENOB} = \log_2\left(\frac{T_{\text{FSR}}}{\text{measured\_}T_{e,\text{MAE}} \times 2}\right). \quad (3)$$

In this paper, the ToA estimation is implemented by energy detection (ED) receivers. The maximum energy selection (MES) method is employed because of its simple implementation. By integrating the received signal in small time windows over a symbol period and then selecting the integrator which gives the maximum value, a ToA estimate can be produced [26]. The ToA error is dependent on the integration intervals, such that the integration window T_{int} is equivalent to the quantization clock T_q. According to (1) and (2), the MAE and the resolution of time-domain systems, which use an MES-based ToA estimator, can be expressed as in the following:

$$T_{e,\text{MAE}} = \frac{1}{T_{\text{int}}}\int_0^{T_{\text{int}}} x\,dx = \frac{T_{\text{int}}}{2} \quad (4)$$

$$n = \log_2\left(\frac{T_r}{T_s} \times \frac{T_s}{T_{\text{int}}}\right) = \log_2\left(\frac{T_r}{T_{\text{int}}}\right). \quad (5)$$

When the system operates wirelessly, the pulses propagate over the wireless channel with additive white noise and path loss (the multipath effect is ignored here). The degraded SNR will further decrease the system performance. The simulation of the ToA error and the system ENOB with respect to different SNRs and T_{int} values has been performed and plotted in Fig. 4. A model is developed to simulate the time-domain characteristics of UWB receptions. The additive white Gaussian noise channel is employed, while the free-space path loss can be obtained by $L = 20\log_{10}(4\pi d f_c/c)$. Furthermore, a reasonable estimation can be given as follows: the UWB TX of the tag emits -40.3 dBm of power at a pulse rate of 300 kHz [22]. Meanwhile, the center frequency of UWB pulses is assumed to be 4.5 GHz, and the bandwidth is estimated to be 5 GHz (3–8 GHz). The antennas' gain of both the tag and the receiver are chosen as 0 dB. In addition, the MES ToA estimation is employed, and the integration window T_{int} is selected to be 10 and 25 ns.

As shown in Fig. 4, a 5-ns MAE with an SNR of -8 dB (corresponding to 0.9 m in distance) can be achieved using ED receivers with a 10-ns T_{int}. The corresponding ENOB is 7.8 bits at a 300-kS/s sampling rate, while the ENOB decreases to 6.5 bits for $T_{\text{int}} = 25$ ns with an MAE of 12.5 ns. In low SNR conditions, the overall performance of both estimators degrades and the $T_{\text{int}} = 10$-ns ED estimator achieves an ENOB of 6.5 bits when distance $= 5$ m, while the $T_{\text{int}} = 25$-ns ED estimator achieves 5.5 bits at 4.7 m. The ENOB can be enhanced by improving the ToA accuracy at the reader side. This can be achieved by smaller integration windows or more complex ToA estimators such as coherent receivers.

In summary, the time-domain resolution is determined by both the reader and the tag. The reader's timing resolution depends on the ToA error, which is constrained by the integration window T_{int}. While at the tag side, the major timing noise (jitter) is caused by the noise of the TWG.

D. Offline-Online Calibration

The proposed PPM-UWB system with the single-slope architecture permits ultra-low-power operation, yet suffers from PVT variations and the nonlinearity issue of the simple TWG circuit. Therefore, an offline-online digital calibration scheme is employed in this paper. The offline calibration is performed only once for each die during the post-fabrication stage (e.g., during chip testing) for process variations and to

reduce the effect owing to the nonlinearity of the TWG's slope. During the calibration, the dc references are applied as the inputs, and their ToA results are stored in a lookup table (LUT) as the corresponding values in the reader. In this paper, a 256-byte LUT is used aiming for 8-bit resolution.

The two-point calibration method [27] is utilized for online calibration during the operation phase, to compensate temperature and voltage variations in different environments. It is performed for every read when the tag is powered up, and only two clock cycles are needed. Before converting the analog input of sensor values, two reference voltages V_{REF1} and V_{REF2} ($V_{\mathrm{REF2}} > V_{\mathrm{REF1}}$) of the tag are converted into two reference codes D_{VREF1} and D_{VREF2} by the ToA estimator at the reader. Then, the sensor input voltage V_{IN} are turned into D_{VIN}. Hence, these digital codes can be expressed as

$$D_{\mathrm{VREF1}} = \mathrm{ToA}(A_S \times V_{\mathrm{REF1}} + D_{\mathrm{offset}}) \tag{6}$$

$$D_{\mathrm{VREF2}} = \mathrm{ToA}(A_S \times V_{\mathrm{REF2}} + D_{\mathrm{offset}}) \tag{7}$$

$$D_{\mathrm{VIN}} = \mathrm{ToA}(A_S \times V_{\mathrm{IN}} + D_{\mathrm{offset}}) \tag{8}$$

where A_S and D_{offset} are the actual slope and the transfer curve offset of the PPM modulator that are sensitive to the temperature and voltage variations. To compensate these effects, the calibrated code D'_{VIN} can be calculated from D_{VREF1}, D_{VREF2}, and D_{VIN} as

$$\begin{aligned} D'_{\mathrm{VIN}} &= \frac{D_{\mathrm{VIN}} - D_{\mathrm{VREF1}}}{D_{\mathrm{VREF2}} - D_{\mathrm{VREF1}}} \\ &= \frac{(A_S \times V_{\mathrm{IN}} + D_{\mathrm{offset}}) - (A_S \times V_{\mathrm{REF1}} + D_{\mathrm{offset}})}{(A_S \times V_{\mathrm{REF2}} + D_{\mathrm{offset}}) - (A_S \times V_{\mathrm{REF1}} + D_{\mathrm{offset}})} \\ &= \frac{1}{V_{\mathrm{REF2}} - V_{\mathrm{REF1}}} \times V_{\mathrm{IN}} - \frac{V_{\mathrm{REF1}}}{V_{\mathrm{REF2}} - V_{\mathrm{REF1}}}. \end{aligned} \tag{9}$$

In (9), the subtractions eliminate D_{offset}, and the slope A_S is compensated by the division, because the same voltage-to-time circuit is used. Thus, D'_{VIN} is calibrated at the reader side. Finally, D'_{VIN} addresses its corresponding dc value stored in the LUT, which has been obtained through the offline calibration as the output result.

The proposed calibration scheme has been validated by simulations and measurements, which will be discussed in Section IV-B.

III. Tag Design and Circuit Implementation

In order to demonstrate the proposed system concept, the tag has been implemented using a 0.18-μm CMOS technology. Fig. 5 presents a block diagram of the tag, which consists of five building blocks: a power-management unit (PMU) with energy harvesting (EH), an RF demodulator, an IR-UWB TX, a pulse-position modulator, and a digital baseband. The PMU rectifies the RF wave to the dc voltage as a power supply to the whole tag. The RF demodulator receives the RF signal and demodulates it into a clock and data. The extracted clock is utilized for the baseband control. The digital baseband decodes these data to identify and execute the commands from the reader and then trigger the tag's finite-state machine. A PPM modulator is employed as a sensor interface to quantize the output of the sensor. The pulser generates narrow pulses at each rising edge of the TW signal or per falling edge of the PPM signal, which provides a drive signal for the UWB TX. An IR-UWB TX, in the band of 3–8 GHz, is utilized to wirelessly transmit the PPM signal. Two low-dropout regulators (LDOs) are introduced to provide regulated voltage to the circuits. LDO1 provides a 1.8-V supply to the comparator of the pulse position modulator, which reduces delay variation, and to the IR-UWB TX, which improves the pulse amplitude. LDO2 generates a 1.2-V supply for the TWG and the RF demodulator in order to reduce power consumption.

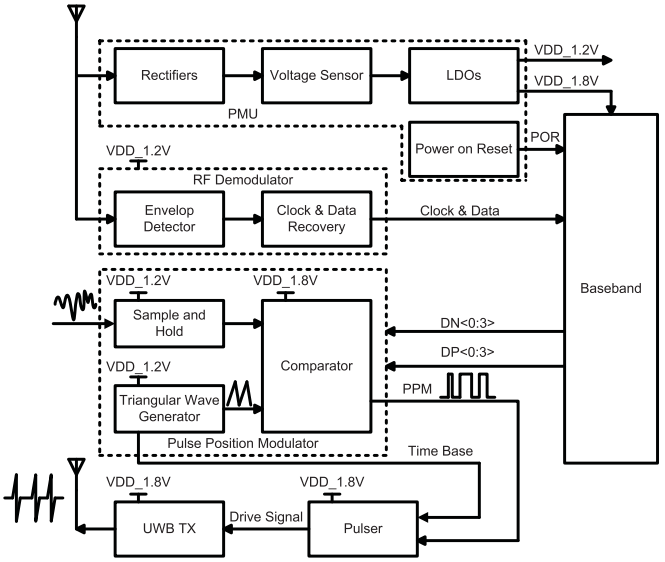
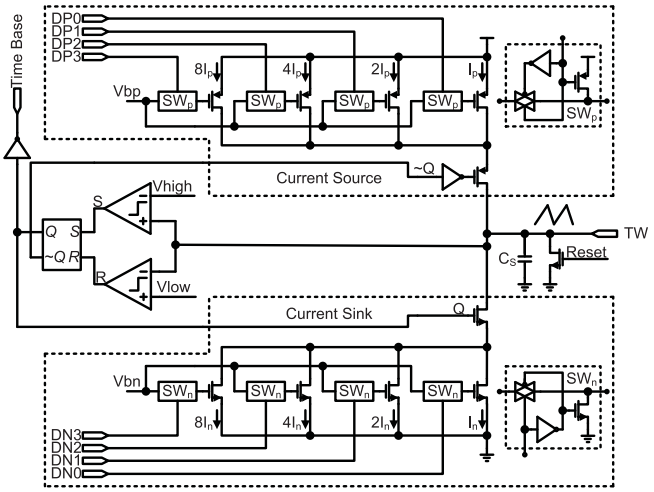


Fig. 5. Schematic of main building blocks.

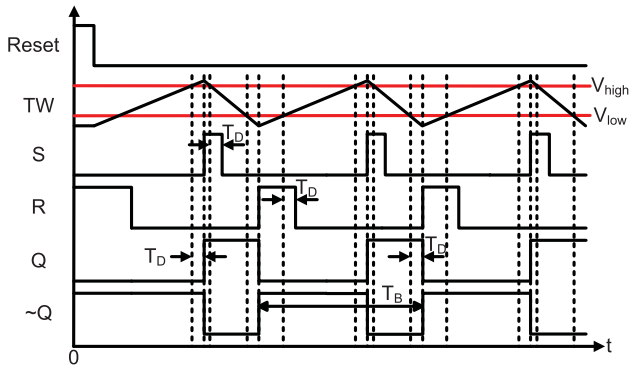
A. Pulse-Position Modulator

The pulse-position modulator, shown in Fig. 2, consists of a sample-and-hold (S/H) circuit, a flexible TWG, and a continuous comparator. The proposed TWG employs a very simple approach that a pair of complementary binary-scaled current source and sink linearly charge and discharge a capacitor C_s to generate a TW. Therefore, the power consumption is reduced significantly. However, the nonlinearity of the TWG's slope limits the resolution of the ADC. This nonlinearity can be effectively suppressed by background calibration on the reader side where power constraint is far more relaxed. In addition, no oscillator or PLL is required in the modulator. Therefore, superior low-power performance is achieved compared with [28] at the cost of increased timing noise. Other methods such as the injection-locking method [29] to extract RF carrier as the reference and the voltage-averaging feedback technique [30] can be applied to improve the timing accuracy but also to bring power and area overhead.

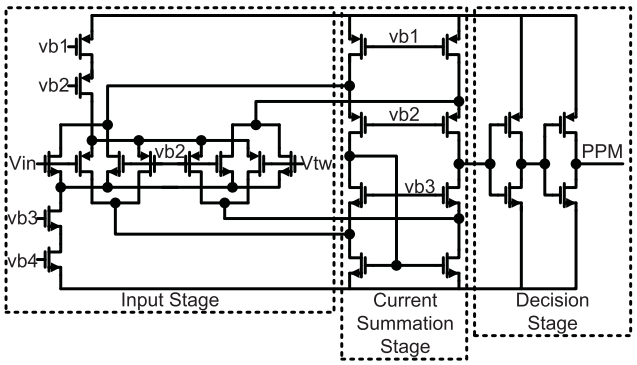
As shown in Fig. 6(a), two comparators are employed in the TWG to compare the voltage across the capacitor with the threshold voltages V_{high} and V_{low}. The outputs of the two comparators are applied to an S-R latch to drive the transmission gates. The operating frequency of the TWG is equivalent to the tag's sampling rate. As shown in Fig. 6(b), T_B is the period of time base signal, which is equal to the tag's sampling period. The circuits' delay T_D leads to unused parts



(a)



(b)



(c)

Fig. 6. (a) Schematic of the TWG. (b) TWG operation waveforms. (c) Schematic of the continuous-time comparator.

of T_r in (1). T_D can be reduced by increasing the operating current but at the cost of higher power consumption.

The continuous-time comparator includes three stages: input stage, current summation stage, and decision stage. The fully differential input stage has a rail-to-rail operating range and provides isolation between the input signal and the current summation circuit. A comparator with a constant propagation

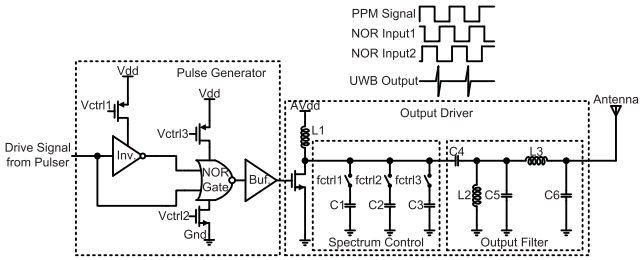


Fig. 7. Schematic of the UWB TX.

delay is critical to minimizing time-quantization distortion. This is achieved by utilizing extra differential pairs operating in the midvoltage region as shown in Fig. 6(c). When the input pair cuts off, the tail current is diverted to the dummy pair. Furthermore, an S/H circuit is used to sample the analog input and ensure stable data during comparison. Therefore, the slew rate is dominated by the bias current, and the propagation delay variation remains lower than the time-domain least significant bit. The operating frequency of the continuous-time comparator in the proposed tag is twice as high as the tag's sampling rate, including an output transition from low to high or from high to low for each sampling. This has obvious advantages over a discrete-time comparator-based approach, whose operating speed is at least 2^N (N is the ADC's resolution in bits) times faster than the sampling rate [16].

B. UWB Transmitter

In this paper, a low-power IR-UWB TX is implemented. A carrierless IR-UWB without up-conversion is employed in order to reduce the power consumption. The shape and spectrum of the output impulses are both adjustable. The TX consists of two blocks, a pulse generator and an output driver with a pulse-shaping filter, as shown in Fig. 7. A short pulse with a duration of hundreds of picoseconds is generated by the pulse generator, after which a driver is used to upconvert the signal. The pulse-shaping filter regulates the spectrum of the output impulses to meet the Federal Communications Commission (FCC) spectral mask.

As shown in Fig. 7, the drive signal from the pulser propagates through a tunable delay cell to generate an inverted signal. An NOR-gate combines the edges of the drive signal and its inverted replica to form a pulse whose duration is in the order of hundreds of picoseconds. A current-starved inverter is employed to implement the tuning delay cell. The tunable pulsewidth is realized by controlling the charge current through Vctr1. The UWB impulses are only triggered on the signal edges of the NOR-gate's output. Meanwhile, the flat part of the output pulse has no effect on the UWB pulse generation, but unnecessary power is also consumed in the driver. To obtain high power efficiency, a TW-like pulse is produced by the starved NOR-gate. Vctr2 and Vctr3 adjust the charge and discharge delay of the NOR-gate to eliminate the flat part of the generated pulse. A class-C output driver with a common source structure is employed, which shifts signals toward the UWB frequency range and improves the UWB

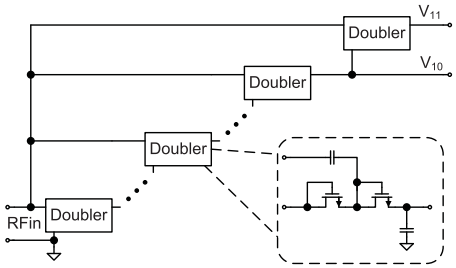


Fig. 8. Schematic of the rectifier.

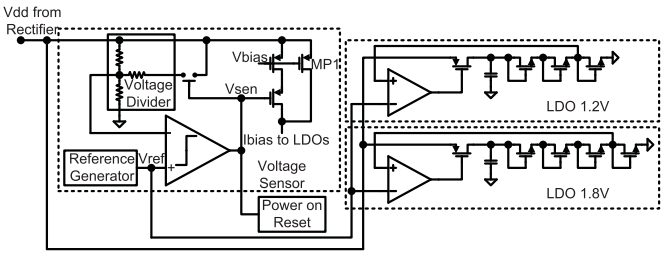


Fig. 9. Schematic of the voltage sensor and LDOs.

pulse swing. The output transistor is wide enough in order to create a high current for the short conduction time. A buffer is inserted before the driver to improve the driving capability. Acting as a bandpass filter, a third-order Bessel filter is used to regulate the transmitted pulse spectrum under the spectral constraint of the FCC mask [7]. The center frequency tuning is realized by fctr1–3 to compensate the PVT variations. The tuning range of the center frequency is from 3.5 to 4.7 GHz, which can cover the three channels (3.5, 4.0, and 4.5 GHz) in the low band of the IEEE 802.15.6 standard [31].

C. Power-Management Unit

The PMU supplies power to the chip from the incoming electromagnetic wave. It consists of a rectifier, a voltage sensor, two voltage regulators, and a power-on-reset (PoR) circuit. The rectifier, which is composed of 11-stage CMOS voltage multipliers, captures the incoming 915-MHz RF signal into a dc voltage for EH, as shown in Fig. 8. The incoming power is accumulated on a storage capacitor. A 4-nF on-chip capacitor is employed by using an nMOS cap, which provides a high-capacity density. The power consumption of the tag is too high to be scavenged from harvested power. Thus, a voltage-sensor consuming a 1.4-μA current is employed to enable the tag's operation when the voltage in the storage capacitor reaches 2.8 V. When the capacitor voltage is less than 2 V, the operation stops and the tag is recharged again. Two LDOs provide regulated voltages of 1.8 and 1.2 V for the tag. The PoR is adopted to generate a reset signal when the tag begins operating. The total current of the PMU during charging is 1.6 μA, thus the rectifier needs to deliver at least 4.5 μW.

Conventional rectifiers are based on the Dickson voltage multiplier [32], where diode-connected MOS transistors are used. In this design, zero-threshold-voltage transistors are utilized to increase the efficiency [33]. Meanwhile, the voltage sensor consists of a reference voltage generator, a voltage divider, and a Schmitt trigger as shown in Fig. 9. A CMOS

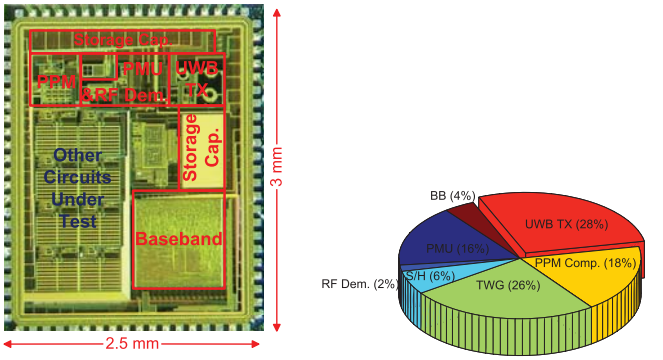


Fig. 10. Die microphotograph and power consumption breakdown of the chip with total power of 41.5 μW.

transistor-based reference generator is used to provide reference voltage. The voltage divider distributes the voltage from the storage capacitor among the diode-connected MOS transistors. The comparator compares the output voltage with the reference voltage. When the storage voltage reaches 2.8 V, the $V_{\rm sen}$ becomes low. The positive feedback changes the divider fraction. In turn, the threshold of the Schmitt trigger will convert to 2 V during discharging. Therefore, a 0.8-V voltage range provides the current needed for the chip operation.

Two LDOs are employed to generate 1.8 and 1.2 V, instead of a power-hungry switched-mode power supply. The same reference voltage, Vref, emanating from the voltage sensor is employed. The output voltage is scaled and then compared with the reference. The negative feedback amplifier controls the voltage drop of the pass pMOS to maintain a constant output voltage with the required value. The PMU can be enabled with a minimized input power if the voltage sensor is the only part of the chip operating in the charging phase. However, the transient response of the LDOs will be long. In the proposed PMU, a small bias current is provided for the LDOs during the charging phase. The small current reduces the transient response of the LDOs significantly while the rectifier performance is only slightly decreased. When the rectifier's output voltage reaches 2.8 V and $V_{\rm sen}$ becomes low, the transistor MP1 turns ON and delivers enough current for the LDOs and the tag's operation.

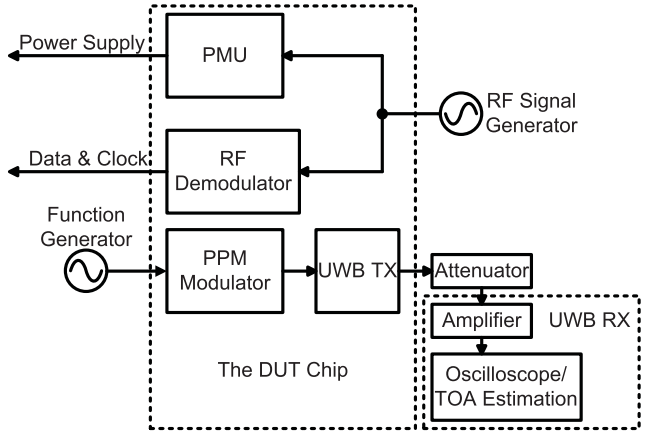
IV. Experimental Results and Discussion

A. Chip Measurement

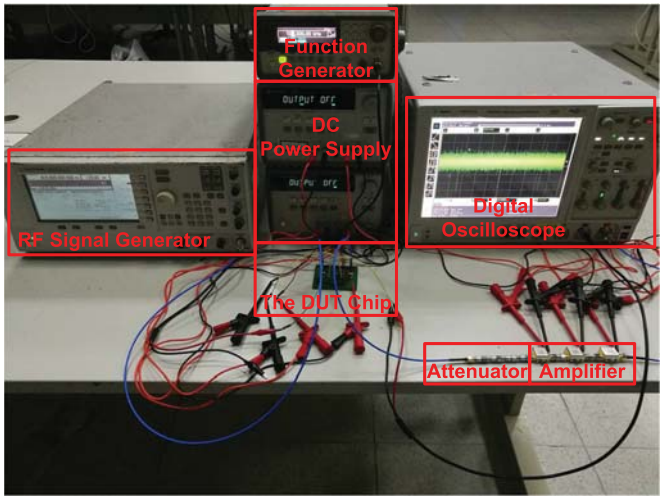
The proposed PPM-UWB tag has been fabricated using a 180-nm CMOS technology. The microphotograph of the die is shown in Fig. 10, while the chip summary is given in Table I. The active area of the tag is 2.5 mm^2. The power consumption is 41.5 μW at a sampling rate of 300 kS/s during conversion and transmission. Fig. 10 also presents the power breakdown of the proposed tag. The pulse-position modulator, which consists of an S/H circuit, TWG, and PPM comparator, accounts for 50% of total power, while the TX only accounts for 28% of total power consumption, which is significantly reduced compared with 74% in [6]. The main part of the pulse position modulator's power is caused by the static current that

TABLE I
CHIP SUMMARY

Technology	0.18 μm CMOS
Active Area	2.5 (mm^2)[1]
Downlink	915 MHz
Sensitivity	-18 dBm
Uplink	UWB 3–8 GHz
UWB Pulse Amplitude	350 mV_{pp}
Power Consumption	41.5 μW@300 kS/s



(a)



(b)

Fig. 11. Measurement setup. (a) Instrument connections. (b) Test environment.

is nearly fixed in this design. While the proposed UWB TX is fully power-scalable with different pulse rates, as no dc power is consumed in the recommended IR-UWB TX. The TWG consumes less than 11 μW, which is due to the simplified circuit and the elimination of reference clock.

The measurement setup is shown in Fig. 11. In the downlink, a 915-MHz modulated RF wave is used to power up the tag and send the clock and commands. The wave is produced

[1]The baseband shares control logic for other testing circuits on the same die, which brings about 0.5 mm^2 extra area.

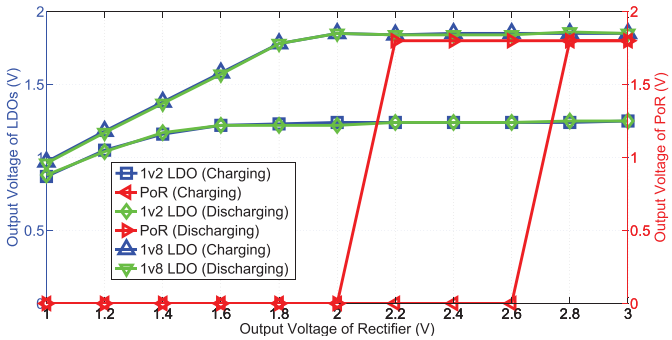


Fig. 12. Measured PMU performance.

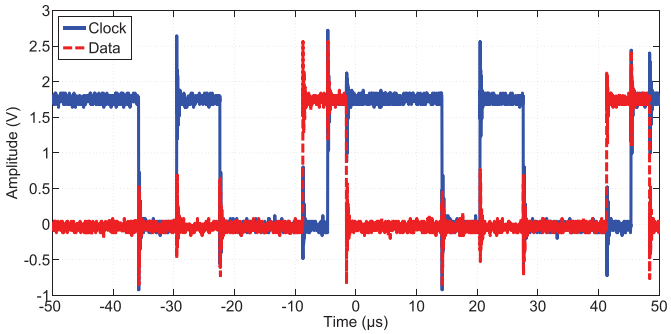


Fig. 13. Clock and data recovery.

by an RF signal generator to model the RFID reader. The sensitivity of the PMU is tested to be -18 dBm, corresponding to an operating range of 2 m when the reader broadcasts an EIRP of 20 dBm. As shown in Fig. 12, the upper and lower limits at which the voltage sensor switches the tag ON or OFF are 2.8 and 2 V, respectively. The 1.8-V and 1.2 V-LDOs fully work when the output of the rectifier reaches 2 and 1.6 V, respectively, while the two LDOs also work when the PoR signal is disabled, because a small bias current is employed. With a -18-dBm power up signal, the discharging time is approximately 95 μs when using a 4-nF on-chip storage capacitor. During discharging, more than 56 PPM-UWB pulses, which is equivalent to 28 samples in the proposed tag, will be transmitted at the 300-kS/s sampling rate. The number of pulses can be increased to at least 1790 when an off-chip storage capacitor of 100 nF is added. Depending on different sensing requirements, different capacitance values and duty-cycling schemes can be chosen. For example, on-chip capacitance may be sufficient for applications where continuous measurement is not needed, whereas a bigger off-chip capacitor needs to be considered for more continuous samples.

An amplitude-shift keying-modulated RF signal with a 100% modulation depth has been used to measure the data and clock recovery performance as shown in Fig. 13. The data are encoded using PWM of the carrier wave, as in the case of conventional class-1 RFIDs [34]. PWM of the 915-MHz carrier transforms data "1" or "0" into an envelope with a low-level duration of 18.75 or 6.25 μs, respectively. A 40-kHz clock and 40-kb/s data rate are demonstrated by the RF demodulator in this figure.

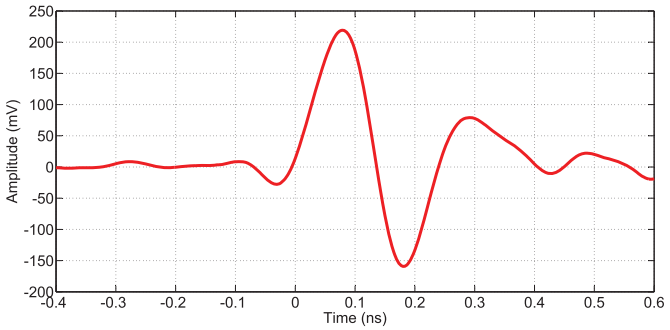


Fig. 14. Directly measured pulse at the UWB TX output through lossy PCB.

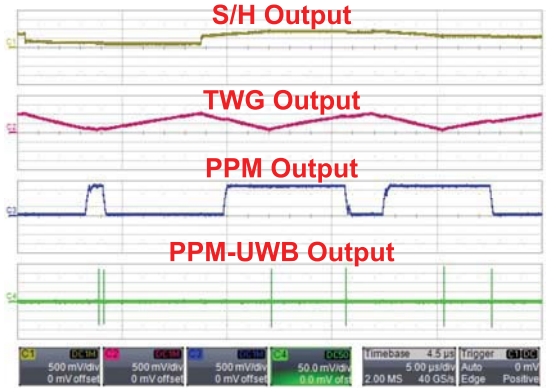
In the uplink, the center frequency of the UWB TX is chosen to be 4.5 GHz with an off-chip matching network for maximized $V_{\mathrm{p-p}}$. The peak-to-peak amplitude of measured pulse is higher than 350 mVpp with a 1.8-V clock source providing drive signal, as illustrated in Fig. 14. The pulse duration is approximately 0.7 ns, while the maximum −10-dB bandwidth ranges from 3 to 6 GHz, which is FCC compliant.

For the TWG, the sampling frequency could be adjusted in 225 steps using $DP_{0\sim3}$ and $DN_{0\sim3}$ digital inputs and the maximum TW swing range is 1 V_{p-p}. The function generator is employed to model analog signals from a sensor.

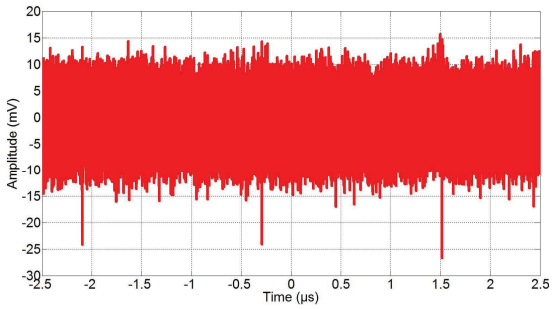
B. System Evaluation and Discussion

The functionality of the entire system is tested by giving 1-$V_{\mathrm{p-p}}$ sine waves at 40 kHz. This signal is followed by an on-chip S/H circuit. The TWG is set to a swing range of 1.1/0.1 V and an oscillation frequency of 120 kHz. Fig. 15(a) shows the transient measurement result of the proposed sensor tag. In this tag, a pulse-position modulator and a UWB TX are utilized to extract and transmit the input voltage in the time domain. Only two pulses are transmitted for each sample. The loss of impulse amplitude compared with Fig. 14 is due to the nonideal edge of the drive signal.

To measure the PPM-UWB modulation performance, an SDR UWB receiver has been implemented using a high-speed digital oscilloscope (Agilent DSO91204A) and off-the-shelf components as shown in Fig. 11. This oscilloscope has a 12-GHz analog bandwidth and a 40-GS/s sampling rate for high-speed analog-to-digital conversion [35], as well as memory for each channel, which enables back-end processing. A broadband amplifier is added at the front end of the oscilloscope to enhance the sensitivity of receiver. To verify the coverage range, the tag and the receiver are connected by an attenuator, ranging from 30 to 50 dB, and two coaxial cables, corresponding to a distance of 0.17–1.68 m in a free-space environment. This design is aimed at short-range contactless RFID sensing, and therefore, the non-line-of-sight and multipath effects are not considered. An SDR ToA estimator is implemented via MATLAB. It converts the received PPM-UWB pulses into digitized codes, which is equivalent to time-to-digital conversion. In this paper, an MES-based ToA estimator is adopted [26]. Then, a time-to-digital conversion is executed in which the proposed offline calibration algorithm



(a)



(b)

Fig. 15. (a) Transient measurement result of the proposed UWB sensor tag. (b) PPM-UWB signal achieved by receiver with 48-dB attenuation and a broadband amplifier, which corresponds to 1.3 m in free space and indicates that the system is capable of operation beyond 1 m.

TABLE II
MEASURED ENOB WITH OFFLINE CALIBRATION

Int. Window	Ideal Imple.	After Calibration				
		0.5 m	0.8 m	1.2 m	1.3 m	1.5 m
10 ns	7.8 bits	6.7 bits	6.7 bits	6.7 bits	6.7 bits	5.9 bits
25 ns	6.5 bits	5.8 bits	5.8 bits	5.8 bits	4.8 bits	
50 ns	5.5 bits	4.9 bits	4.9 bits	4.2 bits		

is also employed to compensate the non-linearity of the PPM modulator.

Fig. 15(b) shows the received PPM-UWB signal with an attenuation of 48 dB, and a broadband amplifier, which corresponds to 1.3 m in free space, implies that he system is capable of operating remotely beyond 1 m. To calculate the ENOB, 100 test points are selected and a 3–8 GHz filter is implemented in software to reject out-of-band noise, so that the MAE and the ENOB can be achieved. The integration window for ToA estimation T_{int} is set to be 10, 25, and 50 ns, while a sampling rate of 300 kS/s at 27 °C is applied. The measured ENOB of the PPM-UWB-based ADC is shown in Table II. The ideal implementation bases on the simulated results as shown in Fig. 4.

The nonlinearity of the TW's slope is a factor that affects the resolution. A significant performance degradation can be observed without calibration, i.e., the ENOB drops to 5.6 bits and less than 5 bits in the simulated and measured result, respectively, with a 10-ns integration window and a sampling

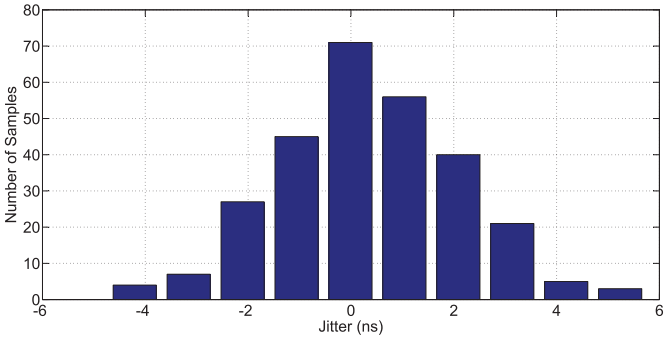


Fig. 16. Simulated histogram of the TWG's jitter at 27 °C.

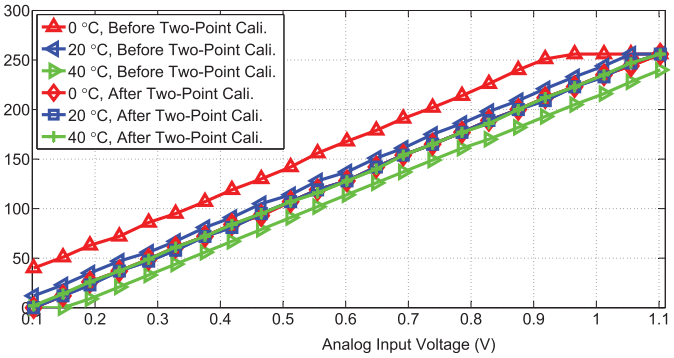


Fig. 17. Simulated sensing transfer characteristic for 0 °C, 20 °C, and 40 °C.

rate of 300 kS/s. This is mainly owing to the nonlinearity of the TWG, which is not optimized with high efforts considering the power and the area of wirelessly powered applications. When the offline calibration process abovementioned is performed, the ENOB can reach 6.7 bits in the measurement as shown in Fig. 19(a). The effective data rate is 2 Mb/s. It implies that the nonlinearity issue is effectively mitigated through the offline calibration. As shown in Table II, the 1.1-bit loss compared with the ideal implementation is essentially caused by the timing noise. It is mainly from the jitter of the TWG, which is up to 10.5 ns (peak-to-peak) in the simulation as shown in Fig. 16 when a bias current and a supply voltage from the PMU are used. This is far larger than other timing noises, for example, 0.02 ns from the UWB TX and 1.03 ns from the comparator. The peak-to-peak jitter of the TWG was measured to be 10.2 ns, resulting in about 1-bit loss compared with the ideal implementation. When $T_{\text{int}} = 25$ ns or $T_{\text{int}} = 50$ ns, the resolution loss is less obvious, because the integration window at this point dominates the ENOB. When the attenuation increases to 48 dB (corresponding to a distance of 1.3 m) or 49 dB (corresponding to a distance of 1.5 m), the SNR decreases, causing the ToA error under a 50- or 25-ns integration window to increase dramatically. As discussed before, the integration window determines the ToA error in the high SNR region, which thus affects the resolution. Therefore, the ENOB can be improved by reducing the ToA integration window at the reader side. When the integration window is set to be 2 ns, an ENOB of 7.3 bits is achieved with a sensitivity of −95 dBm.

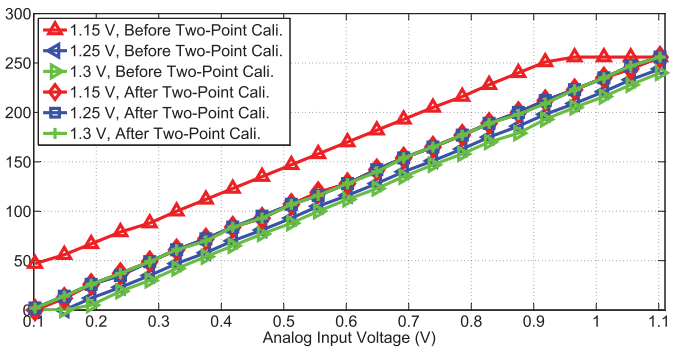


Fig. 18. Simulated sensing transfer characteristic for 1.15, 1.25, and 1.3 V.

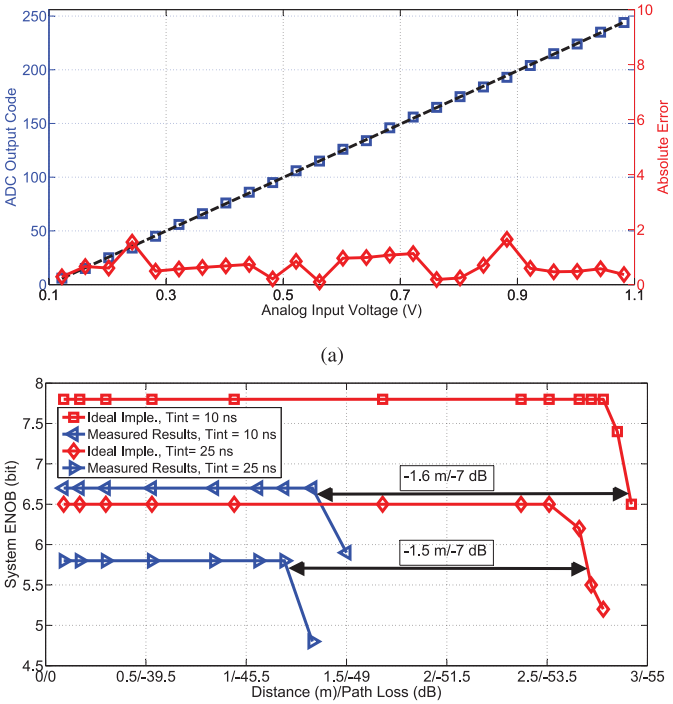


Fig. 19. (a) Measured sensing transfer characteristic and absolute error after calibration with 40-dB attenuation. (b) System ENOB versus distance (path loss) where the ideal implementation is similar to the system simulation in Fig. 4.

The output codes of the PPM-UWB tag are affected by PVT variations. The two-point calibration mentioned before is used to overcome this problem. The reference voltages, V_{REF1} and V_{REF2}, are set to be 0.3 and 0.9 V, respectively. Fig. 17 shows the simulated digital code as a function of the input voltage at 0 °C, 20 °C, and 40 °C. The slope and offset of the transfer curve are drifted with the temperature before calibration. Similarly, the simulated sensing transfer characteristics at 1.15, 1.25, and 1.3 V are shown in Fig. 18. As can be seen, the variations of the output codes are mitigated after the two-point calibration so that the system becomes more tolerant to the voltage and temperature changes. The simulated and measured ENOB are reported in Table III using the proposed offline–online calibration scheme. Only a

TABLE III
SIMULATED AND MEASURED ENOB WITH ONLINE CALIBRATION UNDER DIFFERENT VOLTAGES AND TEMPERATURES

T_{int} / Temp.	10 ns (1.2 V, Simu.)	2 ns (1.2 V, Simu.)	10/2 ns (1.15 V, Simu.)	10/2 ns (1.25 V, Simu.)	10/2 ns (1.3 V, Simu.)	10 ns (Meas.)	2 ns (Meas.)
0 °C	6.8 bits	7.4 bits	/	/	/	6.7 bits	7.4 bits
10 °C	6.7 bits	7.4 bits	/	/	/	6.7 bits	7.3 bits
20 °C	6.7 bits	7.4 bits	/	/	/	6.7 bits	7.3 bits
30 °C	6.7 bits	7.4 bits	6.8/7.4 bits	6.7/7.3 bits	6.7/7.3 bits	6.7 bits	7.3 bits
40 °C	6.7 bits	7.3 bits	/	/	/	6.6 bits	7.3 bits

TABLE IV
PROPOSED SENSING SYSTEM COMPARISON WITH THE STATE OF THE ART

Reference	**TBCAS 2017 [28]**	**TBCAS 2016 [36]**	**TCAS II 2016 [37]**	**JSEN 2016 [15]**	**TCAS II 2016 [16]**	**JSSC 2015 [11]**	**JSSC 2013 [38]**	**This Work**
Technology	350 nm	130 nm	130 nm	350 nm	180 nm	65 nm	130 nm	180 nm
Area	4.07 mm^2	11.75 mm^2	25 mm^2	12.5 mm^2	1.8 mm^2	5.76 mm^2	8.25 mm^2	2.5 $(mm^2)^g$
EH Band	10 MHz	/	/	13.56 MHz	/	300 MHz	/	915 MHz
EH Sensitivity	20.3 dBm	/	/	17.1 dBm	/	-6.5 dBm	-10 dBm	-18 dBm
TX Band	0.2-0.8 GHz	30-120 MHz	fc = 8 GHz BW=1.1 GHz	915 MHz	3-5 GHz	300 MHz	402/433 MHz	3-8 GHz
Sensing Technology	Time Domain	Analog to Digital	Analog to Digital	Time Domain	Time Domain	Analog to Digital	Analog to Digital	Time Domain
Sampling Rate	20 MS/s	1 kS/s	31.25 kS/s[a]	21.48 kS/s[a]	6.7 kS/s	1 kS/s[a]	25 kS/s[d]	300 kS/s
ENOB	5.1 bits	8.4 bits	8.45 bits	8.02 bits	7.7 bits	8.3 bits[c]	7.5 bits[e]	6.7[h]/7.3[i] bits
Radio Technology	UWB	Body Chan. Commu.	UWB	Narrow Band	UWB	Backscattering	Narrow Band	UWB
Total Power	52.8 mW	259.6 µW	15 µW	6.4 mW	3.9 µW[b]	3.5 µW	397 µW[f]	41.5 µW
FOM (pJ/conv.step)	77	768.5	1.4	1147.8	2.8	11.1	87.7	1.3[h]/0.9[i]

a. Sampling rate of one channel. b. Excluding reference clock. c. ENOB is approximately calculated using SFDR for a 1.0 mV input. d. Sampling rate is estimated to be 25 kS/s at 200 kb/s data rate using 8-bit ADC. e. ENOB is assumed to have 0.5-bit loss compared with the target resolution. f. Raw data mode. g. Active area. h. 10-ns integration window. i. 2-ns integration window.

variation of 0.1 bit is found when it is simulated under the tt corner for voltage supply changes from 1.15 to 1.3 V and temperature changes from 0 °C to 40 °C, respectively. We also measured the sensor tag when the temperature ranges from 0 °C to 40 °C using a temperature chamber (Binder MKF240). The bias current and the power supply come from the PMU powered by the 915-MHz UHF incoming signal, thus the non-ideal issues of the power supply have been included. The measurement results demonstrate that the ENOB is guaranteed after calibration under different voltages and temperatures.

The measured ENOB of the entire system versus distance (attenuation) is shown in Fig. 19(b). In order to compare this with the simulation result of the ideal system implementation, similar to that shown in Fig. 4, a 300-kS/s sampling rate is applied and a 10/25-ns integration window is used in the SDR receiver. While the radiated energy of the TX in simulation is replaced with the measured value of our chip, with other parameters remaining the same compared with Fig. 4. As can be seen, if $T_{\text{int}} = 10$ ns, the proposed system has a 6.7-bit ENOB in a 1.3-m range. The 7-dB loss in terms of the reading distance, compared with the ideal implementation, is caused by the noise figure of the amplifier at the UWB receiver (4.5 dB), the insertion loss of the coaxial cables (1 dB), and other non-ideal issues, such as the noise of the oscilloscope and the insertion loss of the attenuators. Moreover, when the integration window increases to 25 ns, the ENOB decreases to 5.8 bits at 1.2 m.

C. Performance Comparisons

A performance comparison is shown in Table IV, where

$$\text{FOM} = \frac{\text{Power}}{\text{Sampling\_rate} \times 2^{\text{ENOB}}}. \tag{10}$$

For fair comparison, we assume that a 25-kS/s sampling rate can be achieved at a 200-kb/s data rate using the 8-bit ADC in [38]. The ENOB is estimated to have a 0.5-bit loss compared with the target resolution (i.e., a 7.5-bit ENOB for an 8-bit resolution ADC, which is consistent with a state-of-the-art ADC [39]). The power consumption of the proposed chip is only 41.5 μW at the sampling rate of 300 kS/s. The ENOB is 6.7 bits with an integration window of 10 ns, resulting in a 1.3-pJ/conv.step FOM. 9× and 67× FOM improvements are achieved, compared with the state-of-the-art tag based on an ADC and a backscattering TX [11], and the tag based on an ADC and a narrowband RF TX [38], respectively. The ENOB increases to 7.3 bits when a 2-ns integration window is chosen. The corresponding FOM is improved to 0.9 pJ/conv.step. The state-of-the-art tag based on

an successive approximation register (SAR) ADC and a UWB TX exhibits low-power consumption [37]. However, the SAR ADC has a large area overhead, which is limited in large-scale recording.

V. Conclusion

A PPM-UWB-based sensor tag with an analog-to-time sensor interface in a 180-nm CMOS is proposed for wirelessly powered IoT applications. As a result of the pulse-position modulator and an ultra-low-power IR-UWB TX, the analog information can be directly converted and transmitted in the time domain. The number of bits to be sent is reduced thanks to the high time-resolution UWB pulses. The SDR receiver extracts the PPM-UWB signals, makes the time-to-digital conversion, and calibrates the outputs. Thus, the original input signals can be recovered. The measurement results demonstrate that a 6.7-bit ENOB at a 300-kS/s sampling rate is achieved at an integration window of 10 ns and a distance of 1.3 m, corresponding to an effective data rate of 2 Mb/s. The total power consumption of the sensor tag is 41.5 μW at a 1.3-pJ/conv.step FOM. The presented chip obtains 9$\times$ and 67$\times$ FOM improvements, compared with the state-of-the-art ADC- and backscattering-based tag, and the ADC- and narrowband RF TX-based tag, respectively. When the integration window decreases to 2 ns, the ENOB and the FOM are improved to 7.3 bits and 0.9 pJ/conv.step, respectively. The operating range of the downlink is up to 2 m with an EH sensitivity of -18- and 20-dBm broadcasted power.

Acknowledgment

The authors would like to thank Q. Wang from Synopsys and X. Zhang from Cypress for their help with the design of the sensor tag.

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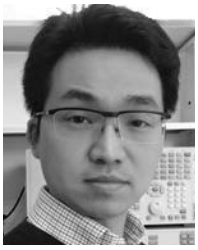

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