A Fully Decoupled *LC* Tank VCO Topology for Amplitude Boosted Low Phase Noise Operation

Bodhisatwa Sadhu, *Member, IEEE*, Tejasvi Anand, *Member, IEEE*, and Scott K. Reynolds

***Abstract*— This paper describes a general technique for reducing oscillator phase noise in *LC* voltage-controlled oscillators (VCOs). Phase noise is reduced using a circuit topology that decouples the *LC* tank from the active devices using capacitive transformers, thereby achieving a higher amplitude of oscillation not limited by the transistor breakdown voltage. Moreover, the proposed VCO topology reduces active device noise injection into the tank by further improving phase noise. As proof of concept, two VCOs operating at 16–19 GHz and 31.8–39.6 GHz, respectively, are implemented in the Global Foundries (GF) 130-nm SiGe BiCMOS 8HP technology (f_T/f_{MAX} of 200/280 GHz). The lower frequency VCO achieves a phase noise of −110 dBc/Hz at a 1-MHz offset from a 17-GHz carrier while the higher frequency VCO achieves a phase noise of −103.2 dBc/Hz at a 1-MHz offset from a 36-GHz carrier. The higher frequency VCO was also implemented in a second, more advanced GF 130-nm SiGe BiCMOS 8XP technology (f_T/f_{MAX} of 260/320 GHz), yielding a further average phase noise improvement of 1.9 dB over the 8HP version.**

***Index Terms*— Decoupled tank, linearization, local oscillators (LOs), mm-wave, oscillation amplitude, phase noise, phase-locked loop, tuning range, voltage-controlled oscillators.**

I. Introduction

SYNTHESIZER phase noise directly impacts link error vector magnitude and data rate [1]–[3], and is therefore one of the most important performance parameters in transmitter and receiver design. The phase noise of *LC* oscillators is primarily limited by: 1) the inherent device noise of voltage-controlled oscillator (VCO) components and 2) the signal power in the tank. For example, in Leeson's phase noise model [4], the phase noise $L(\Delta\omega)$ at an offset of $\Delta\omega$ from the oscillation frequency, ω_0 is given as

$$L(\Delta\omega) = \frac{2FkT}{P_{\text{sig}}} \cdot \left(1 + \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right). \tag{1}$$

Here, the inherent device noise is represented by the excess noise from the active devices, F, and the tank quality factor, Q, while P_{sig} represents the signal power in the tank. While parameters Q and F are typically set by the process technology and VCO topology, respectively, phase noise can be improved by increasing the tank signal power.

Unfortunately, the tank amplitude is typically limited in VCOs, first by active device non-linearity and second by active device breakdown limits. In spite of this amplitude limit, it is still possible to increase tank signal power by adjusting tank current and equivalent tank parallel resistance. In particular, observe that while the amplitude of oscillation is given by $A_{\text{tank}} = I_{\text{tank}} \cdot R_{\text{tank}}$, where I_{tank} is the tank current and R_{tank} is the equivalent parallel tank resistance, the tank signal power is given by $P_{\text{sig}} = I_{\text{tank}}^2 \cdot R_{\text{tank}}$. As a result, R_{tank} can be reduced and I_{tank} increased to maintain a given tank amplitude, A_{tank}, while increasing the signal power, P_{sig}, thereby improving phase noise. One method to reduce tank resistance, R_{tank}, is by reducing the tank inductance and increasing the tank capacitance at a given oscillation frequency, as proposed in [5] and [6].

However, this strategy has practical limits. When the physical size of the capacitor becomes comparable to that of the inductor (see die photo in [7, Fig. 5] for example), the parasitic inductance of the interconnect connecting the capacitor to the rest of the VCO circuit results in the creation of a higher order tank that can support spurious parasitic oscillations. The problem is exacerbated at higher frequencies where capacitors dominate the quality factor, and physically large capacitors are often required to achieve a high quality factor. As a result, for a given amplitude limit, the tank signal power in a cross-coupled VCO (CC-VCO) is practically limited.[1]

Let us now review the underlying cause for the amplitude limit in VCOs and explore strategies to increase this limit. The amplitude limit is typically imposed by MOSFETs entering triode operation in MOS-based VCOs or bipolar junction transistors (BJTs) entering saturation in BJT-based VCOs. In order to extend the voltage limit to reduce phase noise, transistor linearization has been used in BJT VCOs using independent bias control [10]–[12], and more recently, in FET VCOs by minimizing triode operation [13]–[16]. The linearization pushes the transistor compression to higher amplitudes, thereby increasing the amplitude of oscillation, and hence

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[1]Note that another strategy to increase tank signal power is to connect multiple VCOs in parallel [8], [9] thereby adding their signal power coherently while averaging their noise power. This strategy directly trades off both area and power for phase noise, and can be used in conjuction with any VCO topology if the trade-off is deemed worthwhile.

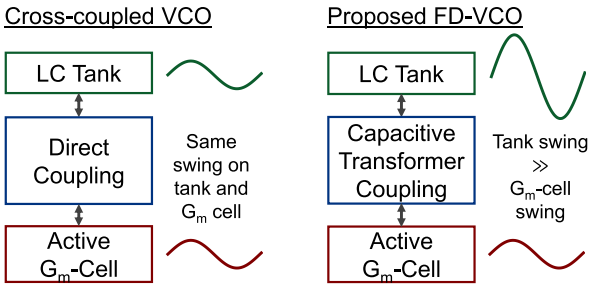


Fig. 1. Conceptual understanding of a fully decoupled VCO achieving large tank amplitudes while maintaining low active device amplitudes.

improving the phase noise. While this approach addresses the non-linearity imposed amplitude limit, the achievable amplitude now becomes limited by the active device breakdown voltage.

This paper, an expansion of [17], proposes a generalized circuit topology which allows the *LC* tank to be fully decoupled from the active devices using capacitive transformers, as shown conceptually in Fig. 1. The capacitive transformers are designed such that the transistor terminals see only a fraction of the tank amplitude. As a result of the lower amplitude at the transistor terminals, larger tank amplitudes can be attained before the devices saturate or reach breakdown voltage limits. Since the tank amplitude determines the phase noise in the VCO, this decoupling approach leads to VCO phase noise reduction without sacrificing transistor breakdown reliability. The fully decoupled tank VCO (FD-VCO) topology also reduces active noise injection into the tank, thereby further improving oscillator phase noise.

The paper is organized as follows. Section II describes the concept and evolution of the fully decoupled *LC* tank VCO and compares its amplitude limit with that of CC-VCO and partially decoupled VCO. Section III presents the phase noise and tuning range analysis of the fully decoupled topology. Section IV presents the implementation details of two VCO prototypes at 17 and 36 GHz. Section V presents the measurement results from the two VCO prototypes, and finally Section VI provides concluding remarks on this paper.

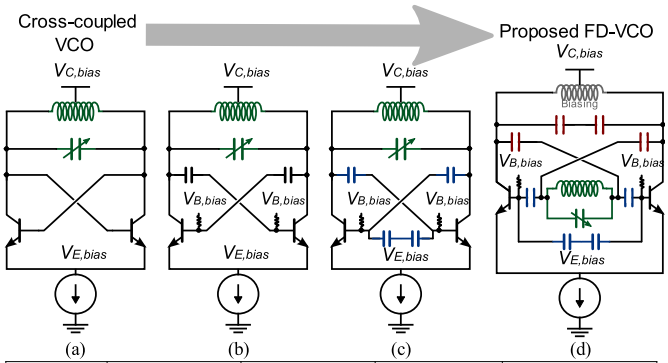
II. Decoupled Tank VCO Concept and Evolution

This section introduces the fully decoupled VCO topology, and explains its higher signal amplitude from: 1) a voltage limit perspective and 2) a large signal transconductance perspective.

A. Voltage Limit Perspective

The voltage swing in a CC-VCO needs to conform to constraints such as maintaining the transistor region of operation and staying clear of transistor junction breakdown limits. Typically, bipolar CC-VCOs are constrained by $V_{\mathrm{BC,sat}}$ (preventing the BJT from entering saturation) and $V_{\mathrm{CE,breakdown}}$ (collector emitter avalanche breakdown voltage). Capacitive or inductive decoupling can be used to separate and control the voltage swings at different nodes so as to increase the tank swing while keeping it within the saturation and breakdown constraints.

To understand how decoupling can be employed for increasing the voltage swing, and thereby reducing phase noise, let



Topology	(a) Cross-coupled (CC-VCO)	(b) Bias-decoupled (BD-VCO)	(c) Partially-decoupled tank (PD-VCO)	(d) Proposed fully-decoupled tank (FD-VCO)
Max. tank amplitude*	0.25 V	0.75 V	0.8 V	Not limited
Limiting constraint	BJT saturation	BJT saturation	V_{CE} Breakdown	None

*Using reasonable estimates for BJT breakdown and saturation voltages in GF 130nm SiGe 8HP

Fig. 2. Evolution (and comparison) from the vanilla CC-VCOs to the fully decoupled tank CC-VCO. (a) CC-VCO. (b) Bias-decoupled CC-VCO. (c) Partially decoupled tank CC-VCO. (d) FD-VCO.

us consider the four VCOs shown in Fig. 2 for comparison. While these examples use capacitive decoupling, the analyses can be extended to inductive decoupling as well.

Moreover, in order to get a quantitative estimate for comparison, let us use the following reasonable values for the Global Foundries (GF) 130-nm BiCMOS 8HP technology: $V_{\mathrm{BC,sat}} = 0.7$ V, $V_{\mathrm{CE,breakdown}} = 3.5$ V for a 1-kΩ base biasing resistor, and 2.5 V for a 10-kΩ base biasing resistor. In order to keep some margin, let us set $V_{\mathrm{BC,lim}} = 0.5$ V and $V_{\mathrm{CE,lim}} = 2.5$ V. Let the regulated voltage supply be at 2.3 V, and the single-ended amplitude of oscillation at the tank, collector, and base can be given by A_T, A_C, and A_B, respectively.

The amplitude of oscillation is constrained by $V_{\mathrm{BC,lim}}$ and $V_{\mathrm{CE,lim}}$ in the following way:

Saturation constraint

$$(V_{B,\mathrm{bias}} + A_B) - (V_{C,\mathrm{bias}} - A_C) \leq V_{\mathrm{BC,lim}}.$$

Breakdown constraint

$$(V_{C,\mathrm{bias}} + A_C - V_{E,\mathrm{bias}}) \leq V_{\mathrm{CE,lim}}.$$

1) Cross-Coupled VCO: Fig. 2(a) shows a conventional CC-VCO, similar to that described in [5]. In this case, the collector bias and base bias are both assumed to be at the regulated supply of 2.3 V ($V_{B,\mathrm{bias}} = V_{C,\mathrm{bias}} = 2.3$ V), while the emitter bias is assumed to be approximately $V_{E,\mathrm{bias}} = V_{B,\mathrm{bias}} - V_{\mathrm{BE,on}} (\approx 0.7\mathrm{V}) \approx 1.6$ V. In this case

$$A_C = A_B = A_T.$$

$$\text{Saturation constraint: } A_T \leq \frac{V_{\mathrm{BC,lim}}}{2} = 0.25 \text{ V}.$$

$$\text{Breakdown constraint: } A_T \leq V_{\mathrm{CE,lim}} - V_{\mathrm{CE,bias}} = 1.8 \text{ V}$$

$$\therefore A_{T,\mathrm{CC}} \leq 0.25 \text{ V}.$$

As a result, the VCO is limited by the saturation constraint to a very low amplitude swing of 0.25 V that severely impacts the achievable phase noise.

2) Bias-Decoupled Cross-Coupled VCO (BD-VCO): In order to improve the voltage swing, the base and collector bias voltages can be decoupled as shown in Fig. 2(b) [10]–[12]. In this case, let $V_{C,\text{bias}} = 2.3$ V (regulated supply), $V_{E,\text{bias}} = 0.6$ V (to accommodate a current source), and $V_{B,\text{bias}} = V_{E,\text{bias}} + V_{\text{BE,on}} = 1.3$ V. The resulting amplitude limit can be derived as shown in the following:

$$A_C = A_B = A_T.$$

Saturation constraint

$$A_T \leq \frac{(V_{\text{BC,lim}} + V_{C,\text{bias}} - V_{B,\text{bias}})}{2} = 0.75 \text{ V}. \quad (2)$$

Breakdown constraint

$$A_T \leq V_{\text{CE,lim}} - V_{\text{CE, bias}} = 0.8 \text{ V}$$

$$\therefore A_{T,\text{BD}} \leq 0.75 \text{ V}. \quad (3)$$

It can be observed from (3) that in the BD-VCO configuration, the VCO is limited by the saturation constraint [similar to CC-VCO], but achieves a much higher amplitude of oscillation of 0.75 V compared to the conventional CC-VCO. Here, it is assumed that the bias current will be increased in order to achieve the higher oscillation amplitude. For simplicity, parasitic capacitances have been ignored in this analysis.

3) Partially Decoupled Tank Cross-Coupled VCO: To further increase the oscillation amplitude (at the cost of higher power consumption), a capacitive transformer can be used to partially decouple the tank from the BJT base node, as shown in Fig. 2(c). This topology retains the bias decoupling of the bias-decoupled VCO while reducing the base swing by a factor of k_B (let us say) in order to extend the VCO voltage limit. The capacitive transformer allows signal amplitude control at the various nodes and enables transconductance linearization to achieve higher oscillation amplitudes. For this analysis, let us assume the same bias voltages as the bias-decoupled VCO

$$A_T = A_C = k_B \cdot A_B.$$

Breakdown constraint

$$A_T \leq V_{\text{CE,lim}} - V_{CE,\text{bias}} = 0.8 \text{ V}.$$

Saturation constraint A_T

$$\leq \frac{(V_{\text{BC,lim}} + V_{C,\text{bias}} - V_{B,\text{bias}})}{\left(1 + \frac{1}{k_B}\right)} = \frac{1.5 \text{ V}}{\left(1 + \frac{1}{k_B}\right)}$$

$$\therefore A_{T,\text{PD}} \leq 0.8 \text{ V}. \quad (4)$$

In this case, we can choose a value of k_B so as to overcome the saturation constraint and be limited by the breakdown constraint. By solving 4, we arrive at $k_B = 1.15$. Despite this, the tank amplitude is limited to only 0.8 V.

4) FD-VCO: In order to allow the tank amplitude to increase further (at the cost of higher power consumption) without violating the saturation or breakdown constraints, we can completely decouple the tank from both the collector and base nodes using two capacitive transformers, as shown in Fig. 2(d). Again, we assume the same bias voltages as the bias-decoupled VCO

$$A_T = k_C \cdot A_C = k_B \cdot A_B.$$

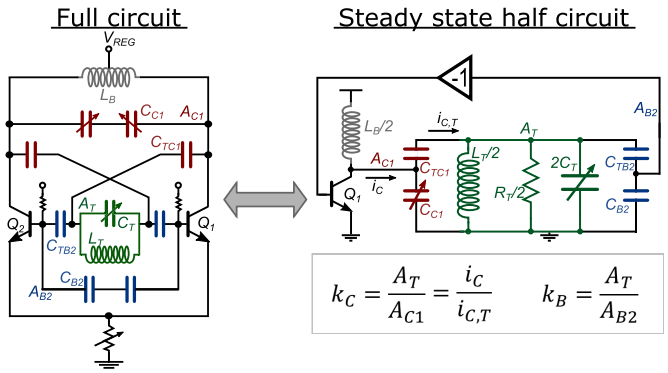


Fig. 3. Fully decoupled VCO full-circuit and half-circuit equivalent models.

Breakdown constraint

$$A_T \leq k_C \cdot (V_{\text{CE,lim}} - V_{\text{CE,bias}}) = k_C \cdot 0.8 \text{ V}.$$

Saturation constraint

$$A_T \leq \frac{(V_{\text{BC,lim}} + V_{C,\text{bias}} - V_{B,\text{bias}})}{\left(\frac{1}{k_C} + \frac{1}{k_B}\right)} = \frac{1.5 \text{ V}}{\left(\frac{1}{k_C} + \frac{1}{k_B}\right)}$$

$$\therefore A_{T,\text{FD}} \text{ can be increased beyond either constraint.} \quad (5)$$

Using the degree of freedom afforded by k_B and k_C, we see that arbitrarily large values of tank amplitude, A_T, can be obtained.[2] A detailed full-circuit schematic and a corresponding steady-state half-circuit model of the proposed 17-GHz FD-VCO is shown in Fig. 3. As shown in Fig. 3, the collector and base swings are a fraction $(1/k_C)$ and $(1/k_B)$ of the tank swing, respectively. Also, due to the capacitive transformers, only a fraction, $(1/k_C)$, of the collector current flows into the tank. Similarly, only a fraction of the base current, $(1/k_B)$, flows into the tank. The definitions of some of these variables are also shown in Fig. 3.

B. Transconductance Perspective

We can also consider the decoupling of the tank as a means to linearize the transconductance cell in the VCO resulting in an increase in the amplitude of oscillation. The linearization in the BJT can be visualized using a transconductance compression plot. Fig. 4 plots the G_m of one transistor in the G_m cell versus the oscillation amplitude. Trace I in Fig. 4(a) shows an example G_m of a BJT in a BD-VCO, as shown in Fig. 2(b) and used in [12]. For small oscillation amplitudes, a large transconductance is obtained (= small signal g_m), and the transconductance compresses with increasing amplitude, as expected. In the case of a CC-VCO, the steady state average G_m is given by $G_m = (2/R_T)$, where R_T is the full circuit effective parallel tank resistance as shown in Fig. 3. Plotting this in Fig. 4(a), the resulting oscillation amplitude, $A_{T,\text{BD}}$, can be obtained. The startup margin for this VCO is represented by the ratio of the small signal g_m and the effective parallel tank conductance, $2/R_T$: startup margin $= [(g_m \cdot R_T)/2]$.

Now, let us assume that G_m cell in this oscillator is fully decoupled from the tank. The oscillation steady-state condition

[2]In practical FD-VCOs, the achievable tank amplitude will be limited by startup considerations, as discussed in Section II-B.

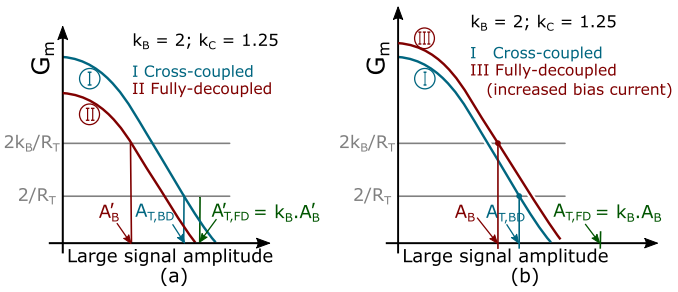


Fig. 4. Transconductance linearization in a fully decoupled tank VCO compared to a bias-decoupled VCO (a) for the same current and (b) with higher current consumption in the fully decoupled tank VCO.

can be derived from the half circuit in Fig. 3

$$\frac{Gm \cdot A_B}{k_C} \cdot \frac{R_T}{2} = A_T \implies \frac{Gm \cdot A_T}{k_C \cdot k_B} \cdot \frac{R_T}{2} = A_T \implies \frac{G_m}{k_C} = \frac{2k_B}{R_T}. \tag{6}$$

Trace II in Fig. 4 shows an example device transconductance curve for $k_C = 1.25$ and $k_B = 2$. As shown in the figure, Trace II is similar to Trace I, but shifted down by the current division factor, $(1/k_C)$, as given in (6). Solving (6) in the context of Fig. 4(a), the steady-state oscillation amplitude at the base, A'_B, can be derived. As can be seen, the base voltage swing has been reduced: $A'_B < A_{T,\mathrm{BD}}$. However, since the tank amplitude is a factor of k_B larger than the base amplitude, the resulting voltage swing on the tank increases to $A'_{T,\mathrm{FD}} = k_B$. A'_B, which, as shown in Fig. 4, can be larger than the tank swing of a BD-VCO, $A_{T,\mathrm{BD}}$.

Moreover, due to the voltage swing reduction at the BJT nodes, the FD-VCO in Trace II now operates in the current limited regime as compared to the voltage limited regime operation of the BD-VCO in Trace I. In order to minimize phase noise, the VCO bias current can now be increased to push the VCO back to the edge of the voltage limited regime operation [5]. Assuming that the FD-VCO is constrained by the saturation constraint, using (2) and (5) it can be shown that the base swing can now be increased to $A_B = A_{T,\mathrm{BD}} \cdot (2\,k_C/k_B + k_C)$, as shown using Trace III in Fig. 4(b), while maintaining the saturation constraint. The bias-decoupled VCO G_m curve is replotted from Fig. 4(a) for comparison. As shown in the figure, the resultant tank swing in the FD-VCO is now even larger than $A'_{T,\mathrm{FD}}$, given by: $A_{T,\mathrm{FD}} = k_B \cdot A_B = (k_B k_C/(k_B + k_C)) \cdot A_{T,\mathrm{BD}}$.

The reduction in effective transconductance seen by the tank initially reduces the VCO startup margin to $[(g_m \cdot R_T)/(2k_B \cdot k_C)]$. However, the startup margin is then partially restored as a by-product of increasing the bias current to enable even higher oscillation amplitudes as discussed in the following. Specifically, the increase in the bias current in Trace III restores the reduction in the startup margin from $((g_m \cdot R_T)/(2k_B \cdot k_C))$ to $(g_{m,\mathrm{high}} R_T/(2 \cdot k_B \cdot k_C))$, where $g_{m,\mathrm{high}}$ is the new transconductance with higher bias current. The change in startup margin can be visualized in Fig. 4(b). The overall direction and amount of impact of the FD-VCO on startup margin depends on the specific non-linearity of the active devices. Moreover, due to the highly non-linear transconductance in BJTs, BJT-based CC-VCOs start with a large startup margin, and this tradeoff is typically acceptable.

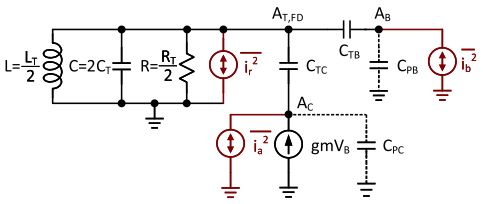


Fig. 5. Small-signal model of the proposed FD-VCO for phase noise analysis.

III. Phase Noise and Tuning Range Analysis

This section presents an analysis of the improvement in the phase noise and FoM of the proposed FD-VCO. Tuning range improvement in the proposed FD-VCO is also discussed.

A. Phase Noise Analysis

The phase noise of the proposed FD-VCO is analyzed and compared with that of a bias-decoupled oscillator. Fig. 5 shows a small signal half-circuit model of the proposed FD-VCO highlighting the dominant noise sources. Using a KCL analysis, it can be shown that the voltage noise introduced into the tank at an offset frequency $\Delta\omega$ is given as

$$\left|V_{Tn}^2\right| = \frac{i_a^2 R^2}{k_C^2 \left(2Q\frac{\Delta\omega}{\omega}\right)^2} + \frac{i_b^2 R^2}{k_B^2 \left(2Q\frac{\Delta\omega}{\omega}\right)^2} + \frac{i_r^2 R^2}{\left(2Q\frac{\Delta\omega}{\omega}\right)^2} \tag{7}$$

where i_a^2 is the BJT collector shot noise power, i_b^2 is the BJT base noise power, and i_r^2 is the noise power due to losses in the tank. In a high Q tank, the BJT collector shot noise and BJT base noise dominates the tank noise contribution. Assuming that the collector shot noise is the dominant phase noise contributor, the phase noise in the proposed FD-VCO can be written as

$$L(\Delta\omega) = 10\log\left(\frac{i_a^2 R^2}{2A_{T-\mathrm{FD}}^2 . k_C^2 \left(2Q\frac{\Delta\omega}{\omega}\right)^2}\right). \tag{8}$$

Let us assume that both the bias-decoupled VCO and FD-VCO are limited by the saturation constraint. From (2) and (5), the resulting tank voltage of the FD-VCO, $A_{T,\mathrm{FD}}$ is expressed as

$$A_{T,\mathrm{FD}} = 2A_{T,\mathrm{BD}}\left(\frac{k_B k_C}{k_B + k_C}\right) \tag{9}$$

where $A_{T,\mathrm{BD}}$ is the tank amplitude of the CC-VCO.

In order to achieve this higher amplitude of oscillation, the bias current of the FD-VCO has to be increased by a factor of k_C, which increases the power consumption and shot noise proportionally. Using (8) and (9), and incorporating a factor of k_C in the numerator to capture the increased shot noise, the phase noise of the FD-VCO can be expressed as

$$L(\Delta\omega) = 10\log\left(\frac{i_a^2 R^2}{8A_{T,\mathrm{BD}}^2 \left(2Q\frac{\Delta\omega}{\omega}\right)^2} \frac{(k_B + k_C)^2}{k_B^2 k_C^3}\right). \tag{10}$$

Note that the phase noise of a BD-VCO or a CC-VCO can be arrived at by setting $k_B = 1$ and $k_C = 1$ in (10) with the appropriate value of the tank amplitude. Moreover, the linearization techniques implemented in [13] and [10] are specific cases of the analysis in this section, and can be obtained by substituting $k_B = 1$ and $k_C > 1$ for [10] and $k_B > 1$ and $k_C = 1$ for [13].

At this point, it is instructive to compare the figure of merit (FoM) of the proposed FD-VCO with that of the BD-VCO. Using (10), the FoM of the proposed FD-VCO can be written as

$$\mathrm{FoM_{FD}} = -10\log\left(\frac{i_a^2R^2}{8A_{T,\mathrm{BD}}^2\left(2Q\frac{\Delta\omega}{\omega}\right)^2}\frac{(k_B+k_C)^2}{k_B^2k_C^3}\right) + 10\log\left(\frac{\omega}{\Delta\omega}\right)^2 - 10\log\left(\frac{P_{\mathrm{FD}}}{1\ \mathrm{mW}}\right) \quad (11)$$

where P_{FD} is the power consumption of the proposed FD-VCO. Similarly, the FoM of the BD-VCO can be written as

$$\mathrm{FoM_{BD}} = -10\log\left(\frac{i_a^2R^2}{2A_{T,\mathrm{BD}}^2\left(2Q\frac{\Delta\omega}{\omega}\right)^2}\left(\frac{\Delta\omega}{\omega}\right)^2\frac{P_{\mathrm{BD}}}{1\ \mathrm{mW}}\right) \quad (12)$$

where P_{BD} is the power consumption of the proposed BD-VCO.[3] Since the bias current of the FD-VCO has to be increased by a factor of k_C, the relationship between the power consumption of the FD-VCO and the BD-VCO can be written as

$$P_{\mathrm{FD}} = k_C \times P_{\mathrm{BD}}. \quad (13)$$

Using (13), (11) can be rewritten as

$$\mathrm{FoM_{FD}} = -10\log\left(\frac{i_a^2R^2}{8A_{T,\mathrm{BD}}^2\left(2Q\frac{\Delta\omega}{\omega}\right)^2}\frac{(k_B+k_C)^2}{k_B^2k_C^3}\right) + 10\log\left(\frac{\omega}{\Delta\omega}\right)^2 - 10\log\left(\frac{k_CP_{\mathrm{BD}}}{1\ \mathrm{mW}}\right). \quad (14)$$

Using (12) and (14), the difference in the FoM of the proposed FD-VCO compared to the BD-VCO can be shown to be

$$\mathrm{FoM_{FD}} - \mathrm{FoM_{BD}} = 10\log\left(4\left(\frac{k_Bk_C}{k_B+k_C}\right)^2\right). \quad (15)$$

This result demonstrates that for all $k_B > 1$ and/or $k_C > 1$, the FD-VCO achieves a higher (better) FoM compared to the BD-VCO. Note that in the above-mentioned FoM analysis, we have assumed BJT shot noise as the only source of noise, which increases as the bias current (power consumption) of the oscillator increases. However, in practice, the collector shot noise is only a fraction of the total noise contribution in the tank. Since the other noise sources do not increase with increasing collector bias current, the FoM difference derived in (15) is pessimistic, and the improvement in FoM of the proposed FD-VCO is expected to be higher than that derived in (15).

[3]Note that (12) can also be obtained by setting $k_B = 1$ and $k_C = 1$ in (11).

B. Tuning Range Analysis

The fully decoupled tank utilizes capacitive transformers that load the tank directly. In this section, we analyze the effect of these capacitive transformers on the tuning range of the VCO. For this, we consider capacitively tuned CC-VCO and FD-VCO with no added fixed capacitance. In both VCOs, the minimum oscillation frequency is determined primarily by the maximum variable capacitance, $C_{\mathrm{var,max}}$, since $C_{\mathrm{var,max}} \gg C_{\mathrm{par}}$. Therefore, to compare the tuning range, we can compare only the maximum oscillation frequency of the CC-VCO and FD-VCO for a given tank inductor and some variable tank capacitance. We use half-circuit representations for simplified analysis. Moreover, for this analysis, we ignore the relatively minor impact of the biasing inductor on the tuning range.

The maximum oscillation frequency, $f_{\mathrm{max,CC}}$, of the CC-VCO is given as

$$f_{\mathrm{max,CC}} = \frac{1}{2\pi\sqrt{\frac{L_T}{2}\cdot(2\cdot C_{\mathrm{var,min}} + C_{\mathrm{PB}} + C_{\mathrm{PC}})}} \quad (16)$$

where L_T is the tank inductance, $C_{\mathrm{var,min}}$ is the minimum capacitance of the variable capacitor, and C_{PB} and C_{PC} are the effective base-ground and collector-ground parasitic capacitances of the BJT, as shown in Fig. 5. Similarly, for the FD-VCO half-circuit shown in Fig. 3, the maximum oscillation frequency, $f_{\mathrm{max,\,FD}}$, is given as

$$f_{\mathrm{max,\,FD}} = \frac{1}{2\pi\sqrt{\frac{L_T}{2}\cdot C_{\mathrm{min}}}}$$

where

$$C_{\mathrm{min}} = \left(2C_{\mathrm{var,min}} + \frac{C_{\mathrm{PB}}+C_{B2}}{k_B} + \frac{C_{\mathrm{PC}}+C_{C1}}{k_C}\right). \quad (17)$$

Note that, in principle, C_{B2} and C_{C1} in Fig. 3 can be eliminated and C_{TB2} and C_{TC1} correspondingly reduced to maintain k_B and k_C, without any change in the fully decoupled functionality. In that case, (17) reduces to

$$f_{\mathrm{max,\,FD}} = \frac{1}{2\pi\sqrt{\frac{L_T}{2}\cdot\left(2C_{\mathrm{var,min}} + \frac{C_{\mathrm{PB}}}{k_B} + \frac{C_{\mathrm{PC}}}{k_C}\right)}}. \quad (18)$$

This expression shows that the maximum achievable frequency is effectively increased in the FD-VCO as compared to that of the CC-VCO topology, yielding an *increase* in the achievable tuning range.

As suggested in Section II-B, the bias current can be increased to restore the base-collector swing of the BJT both to minimize phase noise and to partially restore the startup margin. In order to implement this bias current increase, the BJT size might need to be increased. For a BJT size scaling of n_W, (18) is modified as shown in (19), reflecting a reduction in maximum frequency, and hence a reduction in the tuning range benefit

$$f_{\mathrm{max,\,FD}} = \frac{1}{2\pi\sqrt{\frac{L_T}{2}\cdot C_{\mathrm{min}}}}$$

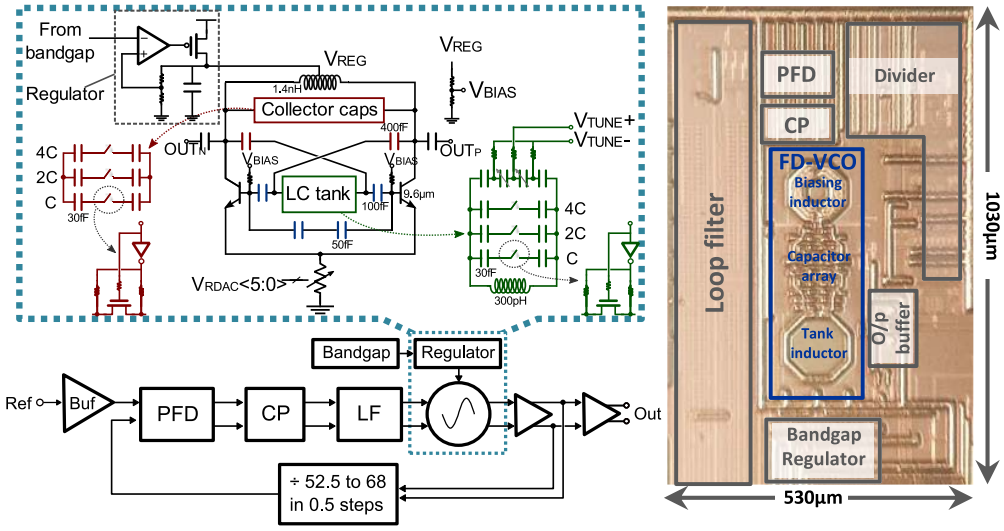


Fig. 6. PLL block diagram with details of the decoupled VCO circuit topology, and die micrograph of the PLL implemented in GF 130-nm SiGe BiCMOS 8-HP technology occupying 0.55 mm^2 with the VCO occupying 0.1 mm^2.

where

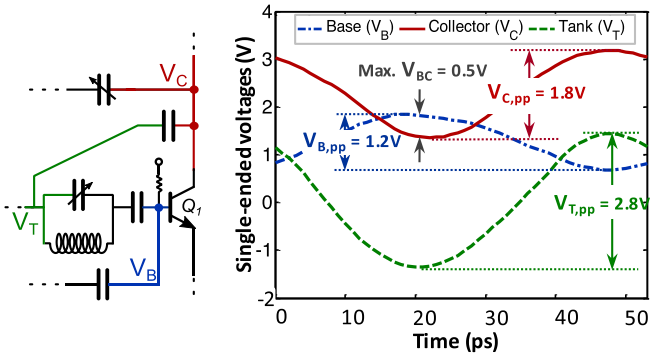
$$C_{\min} = \left(2C_{\text{var,min}} + \frac{n_W \cdot C_{\text{PB}}}{k_B} + \frac{n_W \cdot C_{\text{PC}}}{k_C}\right). \quad (19)$$

Moreover, to control the voltage and current division ratios independently, additional capacitors, $C_{B1,2}$, and $C_{C1,2}$ can be added, as shown in Fig. 3. These added capacitors allow better control of the coupling factors and the maximum frequency of oscillation in the face of process, voltage, and temperature (PVT) variation. These benefits, however, come at the expense of tuning range, as suggested in (17). For example, in our implementation, we use the $C_{B1,2}$ capacitors in the 17-GHz VCO, achieving a 17% tuning range, but eliminate them in the 36-GHz VCO, improving the tuning range to 22% despite the increase in center frequency. We also use a variable $C_{C1,2}$ in order to achieve fine tuning in the tank [the effect of $C_{C1,2}$ variation on the output frequency is reduced by a factor of k_C, as suggested by (17)].

IV. Proof of Concept Implementations

Fig. 6 shows both a block diagram of the implemented 17-GHz phase-locked loop (PLL) that includes the VCO, and a detailed circuit diagram of the decoupled tank VCO itself. The outputs of the PLL are probed via a 50-Ω push–pull totem-pole output buffer. The sub-integer-N PLL is intended to cover a frequency range of 16.66–18.51 GHz. When followed by a frequency tripler, this synthesizer provides a local oscillator (LO) function at 50–55.5 GHz appropriate for 60-GHz radios using the sliding IF architecture described in [12] and [18].

The simulated voltage waveforms appearing at key circuit nodes are shown in Fig. 7. The single-ended voltage swing on the tank is 2.8 V_{pp}, but the swing on the collector (1.8 V_{pp}) is only a fraction $[(1/k_C), k_C = 1.5]$ of the tank swing. Moreover, the base divider ensures that the base swing is limited to only 1.2 V_{pp}, a fraction $[(1/k_B), k_B = 2.4]$ of the tank swing. As discussed in Section III-A, the capacitive decoupling



Max. voltage in VCO		Technology limits		
$V_{CE,max}$ (R_B= 4.5kΩ)	2.3V	V_{CE} breakdown	R_B= 1kΩ	3.5V
			R_B= 10kΩ	2.5V
$V_{CB,max}$	2.5V	V_{CB} breakdown		5.9V
$V_{BC,max}$	0.5V	V_{BC} forward bias		0.7V

Fig. 7. Simulated voltage waveforms on the tank, collector, and base nodes in the VCO, and the corresponding foundry-provided breakdown voltages.

offers a further benefit in that it allows the base and collector to be biased independently. The biasing and the swing are designed such that the maximum V_{BC} voltage (=0.5 V) does not forward bias the junction, keeping the BJT away from saturation. For this design, which uses a 4.3-kΩ base biasing resistance, the maximum V_{CE} voltage is 2.3 V, safely below the foundry provided 2.5-V V_{CE} breakdown limit for a 10-kΩ base biasing resistance, thereby ensuring operation well away from avalanche breakdown. For comparison, to obtain the same tank swing in a bias-decoupled VCO, the maximum V_{CE} voltage would have been 2.8 V, pushing the device into the breakdown regime. Moreover, V_{BC} would have been 1.1 V, driving the BJT deep into saturation.

As shown in Fig. 6, VCO current bias control is achieved using a variable 6-bit switched resistor tail. Frequency tuning

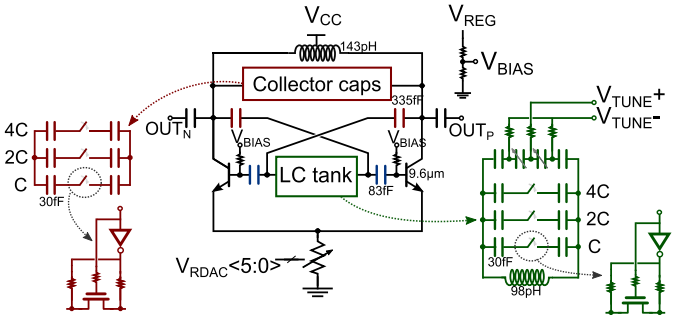


Fig. 8. VCO topology for the 36-GHz design in 8HP and 8XP technologies.

is achieved using 3-bit binary weighted switched capacitors on the tank for coarse tuning, 3-bit binary weighted switched capacitors on the collector for fine tuning, and a differentially controlled, fully decoupled varactor in the tank for analog control. Due to the capacitive feedback, the oscillator frequency is less sensitive to the capacitance variation in the collector. This allows larger switched capacitors to be used on the collector as compared to the tank for a given frequency step, thereby reducing the process sensitivity and relative parasitic capacitance of the fine tuning mechanism. Note that the fine tuning capacitors alter the collector voltage division factor, $1.35 > k_C > 1.6$. However, beyond $k_C = 1.3$, this variation does not violate the breakdown limit or affect the non-linearity or noise significantly, and the phase noise remains relatively constant with fine tuning.

As shown in Fig. 7, a large voltage swing is created on the VCO tank. To ensure that the switches in the switched capacitors maintain their state (ON/OFF) throughout the waveform time period, the switches are biased as shown in Fig. 6. The biasing scheme ensures the following V_{GS} voltages ensuring the switch state is maintained throughout the oscillation period
Switch off
$V_{GS} \leq V_{DD} - V_{T,p}$ ($V_{GS} \approx -400$ mV from simulation).
Switch on
$V_{GS} \approx V_{DD} - V_{sw,p}$ ($V_{GS} \approx$1200 mV from simulation)
where $V_{T,p}$ is the single-ended amplitude of oscillation in the tank, and $V_{sw,p} \ll V_{T,p}$ is the single-ended amplitude of oscillation on the drain–source of the switch when it is turned on. To extend the amplitude of oscillation to even higher voltages, a stacked switch topology can be used [13].

In order to validate the VCO design methodology and topology at mm-wave frequencies, a 36-GHz FD-VCO prototype was also implemented. The topology of the 36-GHz VCO, shown in Fig. 8, is modified compared to the 17-GHz VCO topology shown in Fig. 3 by removing the explicit base capacitor; here the parasitic base capacitor in the BJT is utilized to realize the required voltage division. As in the 17-GHz VCO, a variable 6-bit switched resistor is used for current bias control, switched capacitors are used in the tank for 3-bit coarse tuning, and in the collector for 3-bit fine tuning. The switches in the switched capacitor array are biased similar to those in the 17-GHz VCO to ensure that the switch state is maintained throughout the oscillation period. A differentially controlled varactor is implemented in the tank for analog control and a 50-Ω push–pull totem-pole output buffer is used for measurements.

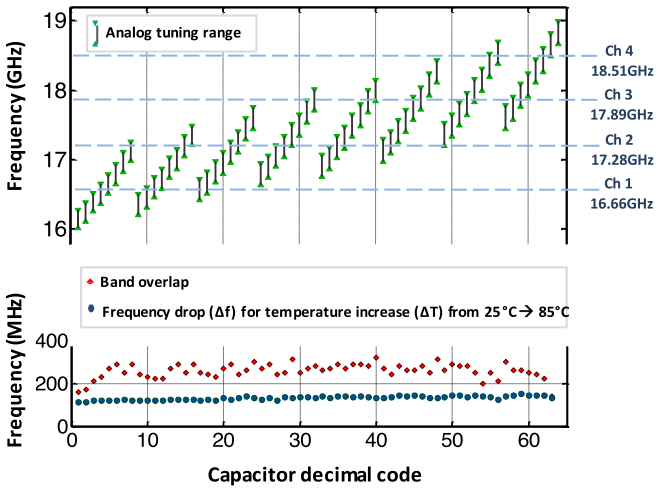


Fig. 9. Measured coarse, fine, and analog tuning of the 17-GHz VCO, band-to-band overlap, and frequency change from 25 °C to 85 °C temperature.

Note that the fully decoupled tank design technique is expected to be even more valuable for the future technology nodes that improve device speed at the cost of reliability (lower breakdown voltages). To benchmark the VCO performance in one such advanced node, the 36-GHz VCO was also fabricated in the GF advanced 130-nm SiGe BiCMOS 8XP technology [19], featuring high-performance NPN BJTs with peak f_T/f_{MAX} of 260/320 GHz. This is an improvement over the GF 130-nm SiGe BiCMOS 8HP technology [20] featuring NPN BJTs with peak f_T/f_{MAX} of 200/280 GHz. The new technology also reduces the base resistance, thereby reducing the base noise from the NPN BJTs. This enhanced device performance comes at the cost of a 100-mV reduction in the V_{CE} breakdown voltage as compared to [20]. The VCO implementation is identical in the two technology nodes, providing an apples-to-apples comparison of the performance between these two technologies.

Moreover, a version of a FD-VCO-based frequency synthesizer in the GF 130-nm SiGe BiCMOS 8XP technology is integrated in a 94-GHz transmitter and receiver chipset [21]–[23] demonstrating low phase noise performance in the context of mm-wave transceivers.

V. Measurement Results

The die micrograph of the PLL incorporating the proposed FD-VCO in GF 130-nm SiGe BiCMOS 8HP process is shown in Fig. 6. Measurement results from the 17-GHz PLL in GF 130-nm SiGe BiCMOS 8HP and from the 36-GHz VCO in GF 130-nm SiGe BiCMOS 8HP and GF advanced 130-nm SiGe BiCMOS 8XP technology are discussed as follows. Spectrum and phase noise measurements were taken using the R&S FSU-67 spectrum analyzer.

A. Measurement of 17-GHz VCO and PLL

The tuning characteristics of the 17-GHz PLL, showing the achievement of a 16–19 GHz (17%) tuning range, are plotted in Fig. 9. The PLL center frequencies for the four

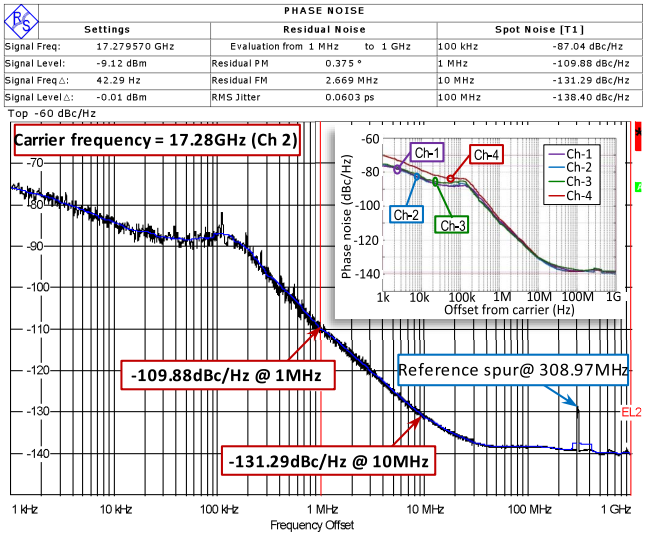


Fig. 10. Measured phase noise versus offset frequencies at 17.28 GHz (channel 2) and an inset of the phase noise in all four channels.

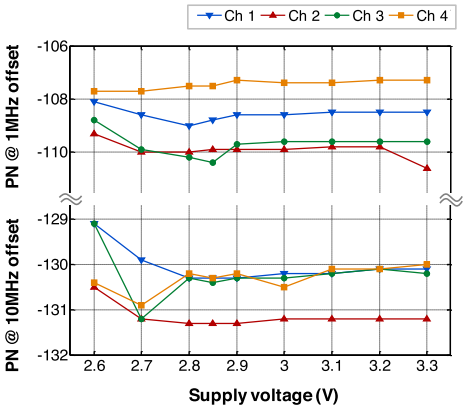


Fig. 11. Measured phase noise of the 17-GHz VCO with supply pushing between 2.6 and 3.3 V across all four channels.

60-GHz channels are annotated. As seen from the plot, the collector fine tuning enables significant band-to-band overlap to account for PVT variations. The lower half of the figure shows the band-to-band overlap is consistently around 300 MHz, while the frequency change over a temperature range of 25 °C to 85 °C is significantly lower (100 MHz) across the tuning range.

Fig. 10 shows a phase noise plot versus offset frequencies. The PLL is configured to have a low bandwidth of ≈100 kHz so that the VCO phase noise dominates at 1 and 10 MHz offsets. The phase noise at 1 MHz is −109.9 dBc/Hz and at 10 MHz is −131.3 dBc/Hz from a 17.28-GHz carrier. The measured PLL phase noise for use in the four 60-GHz channels (inset of Fig. 10) shows that the low noise performance is maintained throughout the frequency range.

Fig. 11 plots the effect of supply pushing on the VCO phase noise across the four channels. The low noise linear voltage regulator depicted in Fig. 6 regulates the 2.85-V supply to $V_{REG} = 2.3$ V for the VCO and ensures less than 1 dB

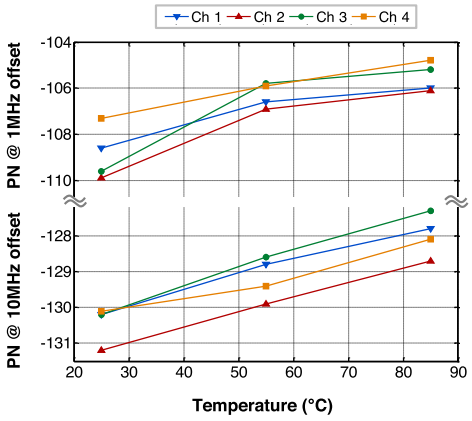


Fig. 12. Measured phase noise of the 17-GHz VCO with temperature variation for 25 °C, 55 °C, and 85 °C across all four channels.

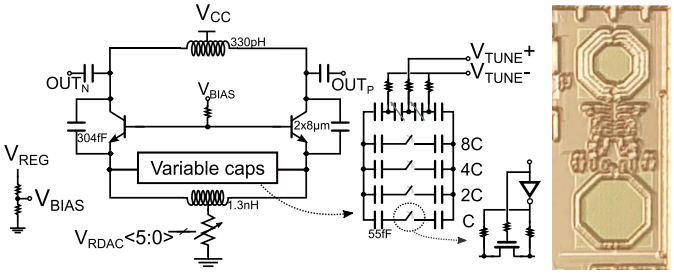


Fig. 13. Schematic and die photo of a 16.5–19.8-GHz modified Colpitts VCO implemented for comparison with the FD-VCO-based PLL.

measured phase noise variation across the four channels for supply pushing from 2.7 to 3.3 V. Fig. 12 plots the effect of temperature on the VCO phase noise across the four channels. As shown in the figure, the phase noise degrades by about 3 dB with a temperature increase from 25 °C to 85 °C. The die micrograph of the PLL is shown in Fig. 6. The PLL occupies 0.55 mm^2 while the VCO occupies 0.1 mm^2.

Phase noise performance of VCOs is highly dependent on the process technology and the associated circuitry with the VCO (e.g., other PLL sub-blocks and regulator). In order to perform an apples to apples comparison of the FD-VCO with other VCO topologies, the phase noise performance of the FD-VCO was compared to two other VCOs: the bias-decoupled VCO published in [12], and a 16.5–19.8 GHz modified Colpitts VCO shown in Fig. 13. All three VCOs are designed in the same GF 130-nm SiGe BiCMOS 8HP design process, instantiated within near-identical integer-N PLLs, and measured in the same setup. Fig. 14 plots the phase noise of the three VCOs at 1 and 10 MHz offsets across the four carrier frequency channels. As shown in Fig. 14, the FD-VCO performs 7–8 dB better than either the BD-VCO or the modified Colpitts across all channels.

The FD-VCO consumes slightly higher power than its counterparts in order to sustain the higher voltage swing. Including this effect, we see that the FoM, plotted in Fig. 15 shows at least 6-dB higher performance in the FD-VCO compared to either the BD-VCO or the modified Colpitts across all

TABLE I
COMPARISON OF THE 17-GHz FD-VCO WITH STATE-OF-THE-ART VCOs IN THE 15–25-GHz FREQUENCY RANGE

Reference	JSSC'08 [12]	JSSC'13 [13]	ISSCC'11 [24]	JSSC'11 [25]	ESS-CIRC'09 [26]	JSSC'04 [27]	TCASI'15 [28]	RFIC'15 [29]	**This work (17 GHz)**
Center freq. (f_{osc}) (GHz)	17.4	24.7	24.8	15	20.8	20	20	17.25	**17.5**
Freq. range (GHz)	16.0 - 18.8	21.8 - 27.5	21.7 - 27.9	10.0 - 20.0	17.9-21.3	18.0 - 23.0	18.7-21.2	10.5 - 24.0	**16.0 - 19.0**
Tuning range (%)	16.1	23	25	66.7	16	25	12.5	78.3	**17.1**
PN @ 1-MHz from f_{osc} (dBc/Hz)	-100.5	-101	-101	-90	-110.3	-99*	-115	-105*	**-110.6**
PN @ 1-MHz from 17.5 GHz (dBc/Hz)*	-100.5	-104	-97	-88.7	-111.8	-100.4	-116	-104.9	**-110.6**
Power consumption (mW)	22†	24	40	7.1**	7.5	9	23	20	**27.5**
Area (mm^2)	–	–	–	0.0029	0.172	–	0.048	0.02	**0.1**
FoM @ 1-MHz offset (dBc/Hz)	172.1	175.2	172.8	167.5	187.6	172.7#	187	176.7	**181.3**
FoM_T @ 1-MHz offset (dBc/Hz)	176.2	188.6	180.8	184	192	180.65	189	194.6	**186**
VCO topology / technique	Bias-decoupled	Partially-decoupled with linearized g_m	Bias-decoupled	Variable inductor	Dual-transformer	Cross-coupled	Trans-former coupled varactor	Capacitance-boosted	**Fully-decoupled tank**
Technology (nm)	130 BiCMOS	32 SOI	45 CMOS	90 CMOS	180 BiCMOS	250 BiCMOS	SiGe HBT	32 SOI	**130 BiCMOS**

*Calculated using a 20 dB/dec. degradation with offset and/or carrier frequency
Measured at 2MHz offset
** Measured at 20GHz
† Measured at IBM Research (not reported in [12])

$$FoM = -L(\Delta f) + 20\log\left(\frac{f}{\Delta f}\right) - 10\log\left(\frac{P_{DC}}{1mW}\right)$$

$$FoM_T = FoM + 20\log\left(\frac{Frequency\ Tuning\ Range\ [\%]}{10\%}\right)$$

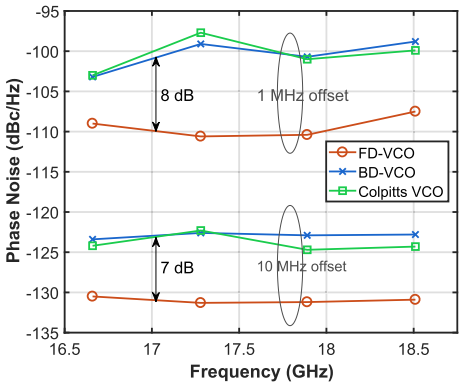


Fig. 14. Measured phase noise comparison of the FD-VCO with the BD-VCO in [12] and a modified Colpitts VCO implemented in the same technology and measured at the same operating frequencies with near-identical PLL settings.

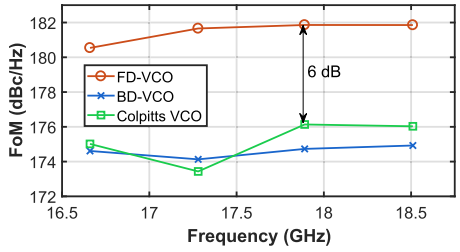


Fig. 15. Measured FoM comparison of the FD-VCO with the BD-VCO in [12] and a modified Colpitts VCO.

channels. The performance of the proposed 17-GHz VCO compared to other state-of-the-art VCOs in a similar frequency range is summarized in Table I.

B. Measurement of 36-GHz VCO

As mentioned in Section IV, the 36-GHz VCO was implemented in two technologies: GF 130-nm SiGe BiCMOS 8HP [20] and GF advanced 130-nm SiGe BiCMOS 8XP technology [19]. Fig. 16 shows a die micrograph of the VCO in the GF 8HP and GF 8XP technologies. The VCO occupies 0.06 mm^2 in both technologies.

The 36-GHz VCO achieves a tuning range of 31.8–39.6 GHz (22%). The tuning characteristics measured for the GF 8HP implementation of the VCO is shown in Fig. 17. The tuning range in the GF 8XP version is almost identical to that of the GF 8HP version. As in the case of the 17 GHz PLL, the collector fine tuning enables significant band-to-band overlap to account for PVT variations.

Fig. 18 plots the phase noise profiles measured in both technologies at the VCO center frequency. The current consumption for both VCOs is 13 mA from a 2.3-V supply.

TABLE II
COMPARISON OF THE 36-GHz FD-VCO WITH STATE-OF-THE-ART VCOs IN THE 30–40-GHz FREQUENCY RANGE

Reference	JSSC'07 [30]	RFIC'10 [31]	ISSCC'13 [32]	ISSCC'13 [33]	**This work (36 GHz) 8HP**	**This work (36 GHz) 8XP**
Center freq. (f_{osc}) (GHz)	40	39.9	32.9	40	**35.7**	**35.6**
Freq. range (GHz)	34.4 - 41.9	34.29 - 39.88	28 - 37.8	33.6 - 46.2	**31.8-39.6**	**31.8-39.6**
Tuning range (%)	18.8	14	29.8	31.5	**21.8**	**21.9**
PN @ 1-MHz from f_{osc} (dBc/Hz)	-100.2	-98.1	-103.6	-97*	**-103.2**	**-103.9**
PN @ 1-MHz from 35.7 GHz (dBc/Hz)*	-101.2	-99.06	-102.9	-97.7	**-103.2**	**-103.9**
Power consumption (mW)	27	14.4	10	9.8	**30**	**30**
Area (mm^2)	0.625	0.15	0.03	0.0084	**0.06**	**0.06**
FoM @ 1-MHz offset (dBc/Hz)	177.9	178.53	183.94	176.5#	**179.48**	**180.15**
FoM_T @ 1-MHz offset (dBc/Hz)	183.36	181.45	193.42	186.46#	**186.3**	**187**
VCO topology / technique	Standing Wave	Cross-coupled	Bias-decoupled BJT + cross-coupled MOS	Cross-coupled	**Fully-decoupled tank**	**Fully-decoupled tank**
Technology (nm)	180 CMOS	65 CMOS	130 SiGe	32 CMOS	**130 BiCMOS**	**130 BiCMOS**

*Calculated using a 20 dB/dec. degradation with offset and/or carrier frequency
Measured at 10 MHz offset frequency

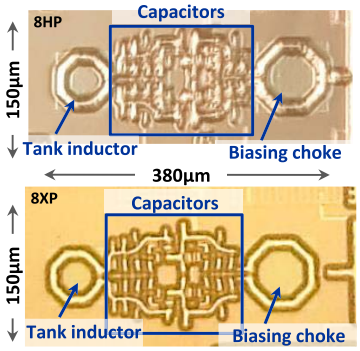


Fig. 16. Die photo of the 36-GHz VCO in the GF 130-nm SiGe BiCMOS 8HP technology (top) and GF advanced 130-nm SiGe BiCMOS 8XP technology (bottom).

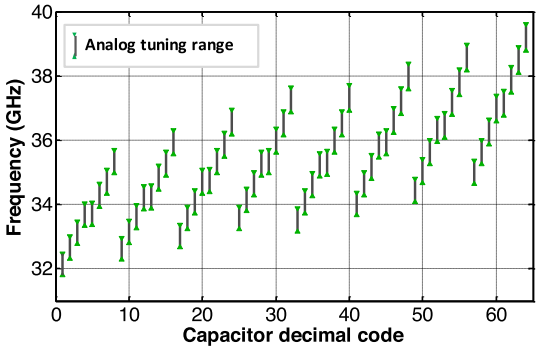


Fig. 17. Frequency tuning for the 36-GHz VCO in GF 8HP technology.

As shown in the figure, the GF 8XP implementation achieves a phase noise of −103.9 dBc/Hz at a 1-MHz offset and −113.4 dBc/Hz at a 3-MHz offset from a 35.6-GHz carrier achieving a 1.9-dB average improvement (35% lower noise power) over its GF 8HP counterpart.

The resulting FoMs achieved at 1-MHz offset are 180.1 dBc/Hz for the GF advanced 130-nm SiGe BiCMOS 8XP design and 179.5 dBc/Hz for the GF 130-nm SiGe BiCMOS 8HP design. The corresponding FoM_T values

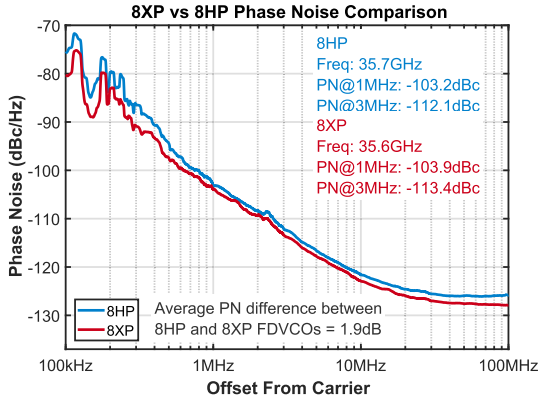


Fig. 18. Phase noise comparison of the FD-VCO between two SiGe 130-nm BiCMOS technology nodes—8HP [13] and 8XP [14].

achieved are 187.1 dBc/Hz and 185.8 dBc/Hz, respectively. The performance of the proposed 36-GHz VCOs compared to other state-of-the-art VCOs in a similar frequency range is summarized in Table II.

VI. CONCLUSION

This paper describes an *LC* VCO design technique that uses a fully decoupled *LC* tank to achieve tank voltage swings in excess of active device breakdown limits. Under the proposed approach, the transistor terminals see a fraction of the tank amplitude and the tank sees a fraction of the transistor transconductance and noise. Two VCO designs, centered at 17 and 36 GHz, respectively, are implemented and measured to demonstrate the benefits of the new approach. The 17-GHz synthesizer featuring the fully decoupled tank VCO exhibits at least 7-dB phase noise improvement and 6-dB FoM improvement over similar PLLs incorporating cross-coupled [12] and modified Colpitts *LC* VCOs implemented in the same technology (130-nm SiGe BiCMOS) and measured in the same setup. Compared to many state-of-the-art VCOs at comparable frequencies, it achieves lower phase noise and better FoM. The 36-GHz VCO is demonstrated in two

technology nodes: GF 130-nm SiGe BiCMOS 8HP and GF 130-nm SiGe BiCMOS 8XP and shows a 1.9-dB average improvement in the advanced technology despite its lower active breakdown voltage. This improvement demonstrates the potential of this technique to leverage technology advancement to a higher technology f_{MAX} achieved at the cost of lower breakdown voltages.

The principles of the demonstrated technique can also be applied in other design contexts. First, note that while in this paper, the fully decoupled tank VCO uses capacitive dividers for both linearization and decoupling; it is also possible to achieve the desired tank isolation by means other than capacitive dividers. An alternate approach, for example, is transformer-based decoupling, which has the advantage of biasing the circuit using a low impedance voltage source reducing noise injection from the voltage source, as well as increasing the V_{CE} breakdown voltage (the breakdown voltage is a function of the base impedance). This benefit comes at the cost of area and design complexity of realizing transformers in Si technology. In addition, although described here in detail for BJTs, the technique is equally applicable to MOSFETs and other active devices.

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