IEEE JOURNAL OF

SOLID-STATE CIRCUITS

A PUBLICATION OF THE IEEE SOLID-STATE CIRCUITS SOCIETY



APRIL 2018 VOLUME 53 NUMBER 4 IJSCBC (ISSN 0018-9200)

SPECIAL ISSUE ON THE 2017 SYMPOSIUM ON VLSI CIRCUITS

STECKE ISSUE ON THE 2017 STAN OSICAL ON VEST CIRCUITS	
EDITORIAL	
New Associate Editors	963
Introduction to the Special Issue on the 2017 Symposium on VLSI Circuits	965
SPECIAL ISSUE PAPERS	
A High Energy Efficient Reconfigurable Hybrid Neural Network Processor for Deep Learning Applications	
S. Yin, P. Ouyang, S. Tang, F. Tu, X. Li, S. Zheng, T. Lu, J. Gu, L. Liu, and S. Wei	968
BRein Memory: A Single-Chip Binary/Ternary Reconfigurable in-Memory Deep Neural Network Accelerator	
Achieving 1.4 TOPS at 0.6 W	
H. Yonekawa, S. Sato, H. Nakahara, S. Takamaeda-Yamazaki, M. Ikebe, T. Asai, T. Kuroda, and M. Motomura	983
Recryptor: A Reconfigurable Cryptographic Cortex-M0 Processor With In-Memory and Near-Memory Computing for	
IoT Security	995
A 4 + 2T SRAM for Searching and In-Memory Computing With 0.3-V $V_{\rm DDmin}$	
S. Jeloka, M. Saligane, Y. Kim, M. Kawaminami, A. Harada, S. Miyoshi, M. Yasuda, D. Blaauw, and D. Sylvester	1006
Exploiting Approximate Feature Extraction via Genetic Programming for Hardware Acceleration in a Heterogeneous	
Microprocessor	1016
An Adaptive-Clocking-Control Circuit With 7.5% Frequency Gain for SPARC Processors	
Y. Kakimura, K. Tajiri, S. Shirota, R. Nishiyama, H. Sakurai, H. Okano, Y. Tomita, S. Satoh, and H. Yamashita	1028
A Digitally Controlled Fully Integrated Voltage Regulator With 3-D-TSV-Based On-Die Solenoid Inductor With a	
Planar Magnetic Core for 3-D-Stacked Die Applications in 14-nm Tri-Gate CMOS	
H. K. Krishnamurthy, S. Weng, G. E. Mathew, N. Desai, R. Saraswat, K. Ravichandran, J. W. Tschanz, and V. De	1038
Double Pile-Up Resonance Energy Harvesting Circuit for Piezoelectric and Thermoelectric Materials	
KS. Yoon, SW. Hong, and GH. Cho	1049
A Stacked CMOS Image Sensor With Array-Parallel ADC Architecture	
T. Takahashi, Y. Kaji, Y. Tsukuda, S. Futami, K. Hanzawa, T. Yamauchi,	
P. W. Wong, F. T. Brady, P. Holden, T. Ayers, K. Mizuta, S. Ohki, K. Tatani, H. Wakabayashi, and Y. Nitta	1061
320×240 Back-Illuminated 10 - μ m CAPD Pixels for High-Speed Modulation Time-of-Flight CMOS Image	
Sensor Y. Kato, T. Sano, Y. Moriyama, S. Maeda, T. Yamazaki,	
A. Nose, K. Shiina, Y. Yasu, W. van der Tempel, A. Ercan, Y. Ebiko, D. Van Nieuwenhove, and S. Sukegawa	1071

(Contents Continued on Back Cover)



A 10.1" 183-μW/electrode, 0.73-mm²/sensor High-SNR 3-D Hover Sensor Based on Enhanced Signal Refining and Fine Error Calibrating Techniques	
	1079
A Miniaturized Single-Transducer Implantable Pressure Sensor With Time-Multiplexed Ultrasonic Data and Power	
Links	1089
Sparsity of Neural Signals	1102
A Capacitively Degenerated 100-dB Linear 20–150 MS/s Dynamic Amplifier	
	1115
A 65-nm CMOS I/Q RF Power DAC With 24- to 42-dB Third-Harmonic Cancellation and Up to 18-dB Mixed-Signal Filtering	1127
A 4.2-mW 10-MHz BW 74.4-dB SNDR Continuous-Time Delta-Sigma Modulator With SAR-Assisted Digital-Domain	
Noise Coupling	4400
IH. Jang, MJ. Seo, SH. Cho, JK. Lee, SY. Baek, S. Kwon, M. Choi, HJ. Ko, and ST. Ryu	1139
A 16-bit 16-MS/s SAR ADC With On-Chip Calibration in 55-nm CMOS	1140
A. Shikata, L. D. Fernando, N. Guthrie, B. Chen, M. Maddox, N. Mascarenhas, R. Kapusta, and M. C. W. Coln A 69-dB SNDR 300-MS/s Two-Time Interleaved Pipelined SAR ADC in 16-nm CMOS FinFET With Capacitive	1149
Reference Stabilization E. Martens, B. Hershberg, and J. Craninckx	1161
A 2-GS/s 8-bit Non-Interleaved Time-Domain Flash ADC Based on Remainder Number System in 65-nm CMOS	1101
	1172
A 3.2 ppm/°C Second-Order Temperature Compensated CMOS On-Chip Oscillator Using Voltage Ratio Adjusting	11/2
Technique	1184
A Low-Jitter and Low-Reference-Spur Ring-VCO-Based Switched-Loop Filter PLL Using a Fast Phase-Error	110.
Correction Technique	1192
A 65-nm 10-Gb/s 10-mm On-Chip Serial Link Featuring a Digital-Intensive Time-Based Decision Feedback	
Equalizer	1203
A 32 Gb/s, 4.7 pJ/bit Optical Link With -11.7 dBm Sensitivity in 14-nm FinFET CMOS	
I. Ozkaya, S. Kim, D. M. Kuchta, S. Lee, S. V. Rylov, H. Ainspan, T. O. Dickson, J. F. Bulzacchelli, and M. Meghelli	1214
A 60-Gb/s 1.9-pJ/bit NRZ Optical Receiver With Low-Latency Digital CDR in 14-nm CMOS FinFET	
	1007
L. Kull, C. W. Baks, J. E. Proesel, M. Kossel, D. Luu, B. G. Lee, F. E. Doany, M. Meghelli, Y. Leblebici, and T. Toifl	1227