# E-Band Multi-Phase *LC* Oscillators With Rotated-Phase-Tuning Using Implicit Phase Shifters

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***Abstract*— A rotated-phase-tuning (RPT) technique is proposed for millimeter-wave (mmW) *LC*-based oscillators. Without using varactors, the oscillation frequency is tuned by phase interpolation to vary the phase of the current flowing into the *LC* tank. Interestingly, the intrinsic delay of transistors is leveraged to rotate the phases for interpolation and thus to optimize the oscillator's performance in terms of frequency tuning range and phase noise. Two E-band RPT oscillator prototypes are designed and implemented in a 65-nm CMOS process. The first one with four-phase output measures oscillation frequency from 67.8 to 81.4 GHz and phase noise of −108 to −113 dBc/Hz at 10-MHz offset, while consuming 13 to 25 mW from a 1-V supply. With similar power consumption, the second prototype featuring eight-phase output operates from 74.8 to 79 GHz and achieves phase noise of −116 to −118 dBc/Hz at 10-MHz offset. The four-phase and eight-phase oscillators occupy small core areas of 0.02 and 0.06 mm$^2$, respectively.**

***Index Terms*— CMOS, frequency tuning, intrinsic delay, millimeter-wave (mmW), multiphase, oscillator, phase noise, rotated-phase-tuning (RPT), tuning range, varactor-less.**

## I. Introduction

THE ever-increasing demands for high-data-rate wireless communication, radar sensing, and imaging continue to motivate the research and development of millimeter-wave (mmW) transceiver systems using mainstream CMOS technologies [1]–[4]. In these systems, a local oscillator (LO) signal is indispensable for performing frequency conversion between the RF and the baseband. Generally, the LO frequency is required to be tunable to accommodate various operating channels and the phase noise should be sufficiently low to negligibly deteriorate the signal-to-noise ratio (SNR). In addition, multiple phases are highly desired to support direct-conversion architectures which are advantageous in terms of simplicity, image free, and low consuming power [5], [6] and to enable phased-arrays that have been widely employed for link budget improvement and beam steering at mmW [7], [8]. To address these performance requirements, various topologies and techniques have been developed for mmW LO generation. In particular, directly synthesizing the LO based on a voltage-controlled oscillator (VCO) oscillating at the desired frequency is recognized as one of the optimal choices due to its large output swing, continuous frequency coverage, and the simplicity for system integration [6], [9], [10]. However, the circuit design and implementation in CMOS remains a major challenge, especially considering that a wide frequency range is typically required to tolerate process, voltage, and temperature (PVT) variations. Foremost, the quality factor of tuning varactors is predominantly low at mmW, which directly results in phase noise degradation [11], [12]. Enlarging the transistors and burning more power could increase the oscillation amplitude and thus improve the phase noise, but the more parasitic capacitance induced would in turn narrow down the tunable frequency range. In case multiple-phase output is required, the situation would get even worse due to the additional loading from the coupling devices.

Recently, several novel frequency tuning techniques for mmW VCOs have been reported. In fact, most of them are based on switched inductors or transformers to vary the effective inductance in the *LC* tank and thus to achieve wide frequency tuning range [13]–[18]. For instance, by using transformer-based magnetic tuning, the VCO in [19] has successfully realized a tuning range of 41%. However, low-Q varactors are still required to continuously fine-tune the frequency. More importantly, the phase noise at certain frequency range is poor, limiting the achievable figure of merit (FoM). For multi-phase *LC* oscillators, these techniques would inevitably experience performance degradation due to the more parasitics presented. In [20], a varactor-less interpolative-phase tuning is proposed for multi-phase oscillators, demonstrating state-of-the-art phase noise. However, multiple dedicated phase shifters are required, resulting in large chip area and high-power consumption.

In this paper, a simple but effective varactor-less rotated-phase-tuning (RPT) technique suitable for multiphase mmW *LC* oscillators is proposed. Unlike conventional phase tuning,

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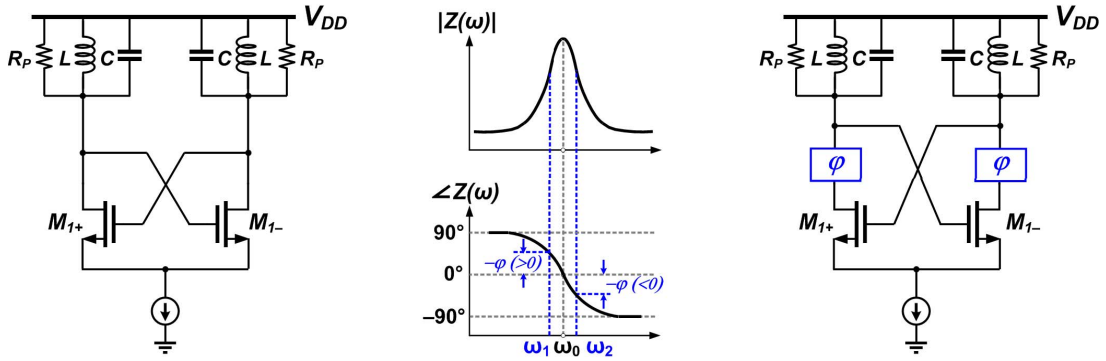



Fig. 1. (a) Conventional *LC* oscillator. (b) Impedance of the *LC* tank. (c) With phase shift inserted to change the oscillation frequency.

the intrinsic delay of the transistors is leveraged to rotate the phases and thus to improve the oscillator performance. To validate the proposed RPT technique, two E-band oscillators are designed and implemented. The one with four-phase output achieves a wide tuning range of 18% from 67.8 to 81.4 GHz, while the other with eight-phase output measures low phase noise of −116 to −118 dBc/Hz at 10-MHz offset around 77 GHz. They only occupy small core areas due to the implicit phase shifters.

This paper is organized as follows. In Section II, the proposed RPT technique for mmW oscillators is described and the design of variable phase shift is discussed. Section III analyzes the properties of RPT oscillators and presents the circuit implementation of four-phase and eight-phase RPT oscillator prototypes. Section IV shows the measurement results, and finally conclusion is given in Section V.

## II. Proposed Rotated-Phase-Tuning Technique

### A. Tuning Method and Working Principle

For the conventional differential *LC* oscillator depicted in Fig. 1(a), it is well known that stable oscillation requires the negative transconductance of the cross-coupled transistor pair to be sufficient to compensate the tank loss represented by $R_P$. In fact, this is merely the gain condition and an underlying phase condition is automatically satisfied when the oscillation frequency is derived. By treating the differential oscillator as a feedback loop composed of two single-ended inverting buffers, the phase condition that the total phase shift along the loop should be 360° becomes more obvious. Since each of the two transistors already has 180° phase difference between its output current and input voltage, the *LC* tank is required to contribute 0° phase shift, resulting in oscillation at the resonance frequency, i.e., $\omega_0 = 1/\sqrt{LC}$, as illustrated by the impedance plots in Fig. 1(b). Therefore, tuning of the oscillation frequency can be simply implemented by varying either $L$ or $C$ to shift the tank's resonance frequency, which has been commonly employed but inevitably suffers from several drawbacks for mmW VCOs as mentioned earlier. More importantly, the analysis also indicates that the oscillation frequency changes along with the phase shift in the loop. As shown in Fig. 1(c), if a phase shift ($\varphi$) is inserted in series with the *LC* tank, then the tank would have to provide a phase of $-\varphi$ to compensate $\varphi$ and thus the circuit will be oscillating at a new frequency rather than $\omega_0$ as long as the gain condition can be still fulfilled [21]. One step further, continuous frequency coverage can be obtained by properly tuning the phase shift $\varphi$ somehow. Intuitively, its range would be proportional to the span of the variable phase shift.

Before considering the detailed circuit implementation, it is worthwhile investigating the requirement on the variable phase shifts. From Fig. 1(b), it can be observed that the impedance magnitude of the *LC* tank decreases as the oscillation frequency gradually deviates from the resonance frequency $\omega_0$. In particular, the equivalent quality factor of the *LC* tank can be approximated as [22]

$$Q \approx Q_0 \cdot \cos\varphi \tag{1}$$

where $Q_0$ denotes the intrinsic quality factor at $\omega_0$. Apparently, as $|\varphi|$ increases and gets too close to 90°, both the output amplitude and the phase noise of the oscillator will be severely degraded if the oscillation still sustains. Therefore, depending on the tolerable performance degradation, an upper limit is imposed on the variable phase range $|\varphi|$, yielding finite frequency tuning range. In other words, when designing the variable phase shift, there is performance tradeoff between the phase noise and the frequency tuning range.

To facilitate circuit implementation, phase interpolation [23] can be employed to vary the phase shift. The idea is to superpose two existing vectors with different phases ($\Delta\theta \leq 90°$) and control their amplitude ratio such that the resulted vector can have a tunable phase. Since the cross-coupled pair ($M_{1\pm}$) in the conventional oscillator topology already contributes one differential current branch, a differential pair of transistors ($M_{2\pm}$) is added in parallel with it to generate the other, as shown in Fig. 2(a). These two currents are then superposed and injected into the *LC* tank. With the tail currents $I_{b1}$ and $I_{b2}$ tuned to vary the transconductance of $M_{1\pm}$ and $M_{2\pm}$, respectively, amplitude-ratio control and thus phase interpolation can be realized. Now, the problem is how to supply the differential pair with a voltage signal which has exactly the same frequency but a different phase compared to the output voltage. Fortunately, this can be

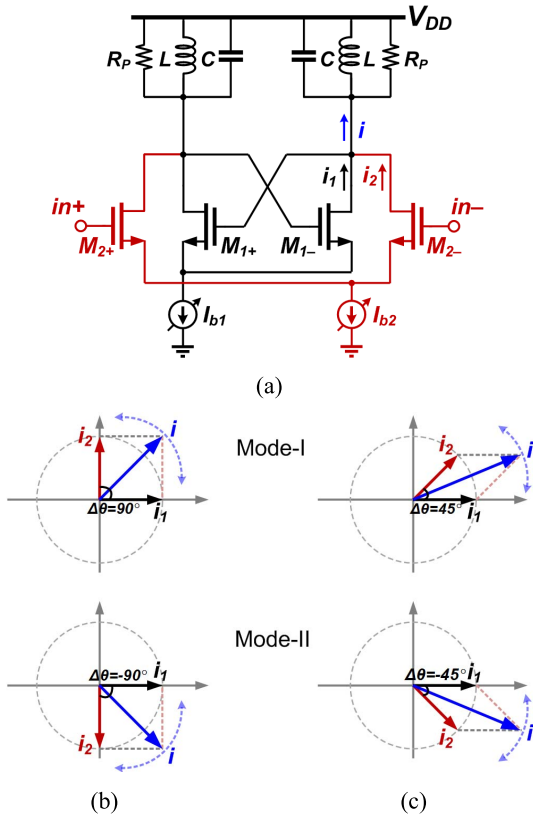



Fig. 2. Phase interpolation for phase tuning. (a) Schematic of the oscillator cell. (b) Phasor diagrams when the phase difference $\Delta\theta$ is $\pm 90°$. (c) Phasor diagrams when the phase difference $\Delta\theta$ is $\pm 45°$.

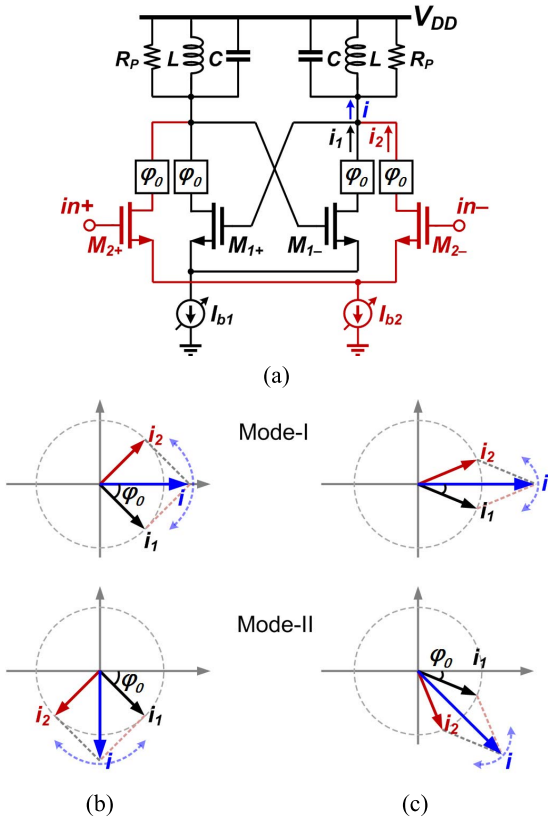



Fig. 3. Inserting negative phase shift $\varphi_0$ to the phase interpolation for the proposed RPT. (a) Schematic of the oscillator cell. (b) Phasor diagrams when the phase difference $\Delta\theta$ is $\pm 90°$ and $\varphi_0 = -45°$. (c) Phasor diagrams when the phase difference $\Delta\theta$ is $\pm 45°$ and $\varphi_0 = -22.5°$.

addressed by connecting multiple oscillator cells together to form an $N$-stage $LC$-based ring oscillator. Benefited from the multiple-phase output, phase difference exists between the input voltage to the differential pair and the output voltage in each stage. To be more specific, the phase difference $\Delta\theta$ is either $180°/N$ or $-180°/N$, corresponding to two oscillation modes, defined as Mode-I and Mode-II, respectively [20]. For $N = 2$ and $N = 4$, their phasor diagrams in current domain are illustrated in Fig. 2(b) and (c), respectively. As such, with the aforementioned phase tuning approach based on phase interpolation, the oscillation frequency can be varied. However, as the magnitude of the interpolated current is the same for the two modes and ideally the $LC$ tank is symmetrical in terms of amplitude and phase response, it is not able to predict which mode the oscillator will operate at and thus phase ambiguity issue exists [24], [25]. In addition, the single polarity of the phase shift due to mono-mode operation confines the oscillation frequency within either the lower or the higher side near the peak frequency $\omega_0$. Furthermore, the frequency tuning range is limited in both two modes. On one hand, the variable phase range is bounded by the degradation of output amplitude and phase noise, as pointed out earlier. On the other hand, the maximum achievable phase shift cannot exceed the phase difference $\Delta\theta$ due to the phase interpolation approach used.

In order to optimize the frequency tuning range and to mitigate the performance tradeoff, both of the above two limiting factors should be tackled appropriately. At first, the phase difference $\Delta\theta$ needs to be reasonably large and not a bottleneck for the variable phase range. This can be easily achieved by optimizing the number of stages in the oscillator. In conjunction with other considerations including layout symmetry and routing complexity for practical implementation, the optimal stage number ($N$) is either 2 or 4, yielding $|\Delta\theta|$ equal to 90° and 45°, and output phases of 4 and 8, respectively. Afterward, the variable phase shift range should be maximized to widen the frequency tuning range while the negative effect on the phase noise is minimized. As the polarity of the phase shift does not affect the equivalent quality factor, it is desired to be both positive and negative to better utilize the available phase difference for a larger variable range without any performance penalty. To implement this, a negative phase shift of $\varphi_0$ is inserted to each of the two current branches and it is designed to be around half of the phase difference, i.e., $\varphi_0 \approx -|\Delta\theta|/2$. By doing so, all the current vectors are rotated clockwise, resulting in variable phase shift approximately evenly distributed around the impedance peak of the $LC$ tank for Mode-I operation. Fig. 3 illustrates the schematic and the corresponding phasor diagrams. Interestingly, Mode-II operation is discriminated because the $LC$ tank would have to contribute a larger phase which corresponds to a much lower impedance compared with Mode-I. As such, the phase ambiguity issue is resolved. In Section II-B, the implementation of the negative phase shift $\varphi_0$ will be discussed.

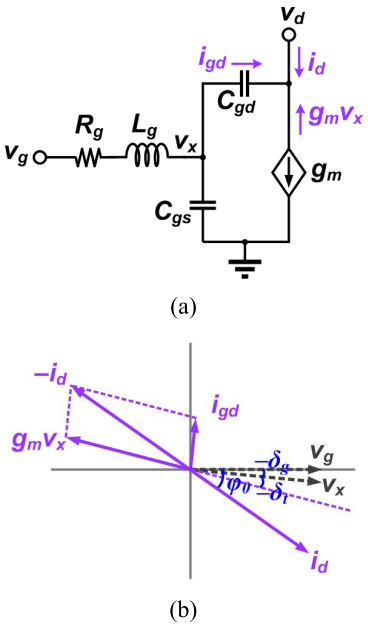



Fig. 4. (a) Small-signal model of an NMOS transistor. (b) Phasor diagram showing the phase delay $\varphi_0$ between the input gate voltage and the output drain current [27].

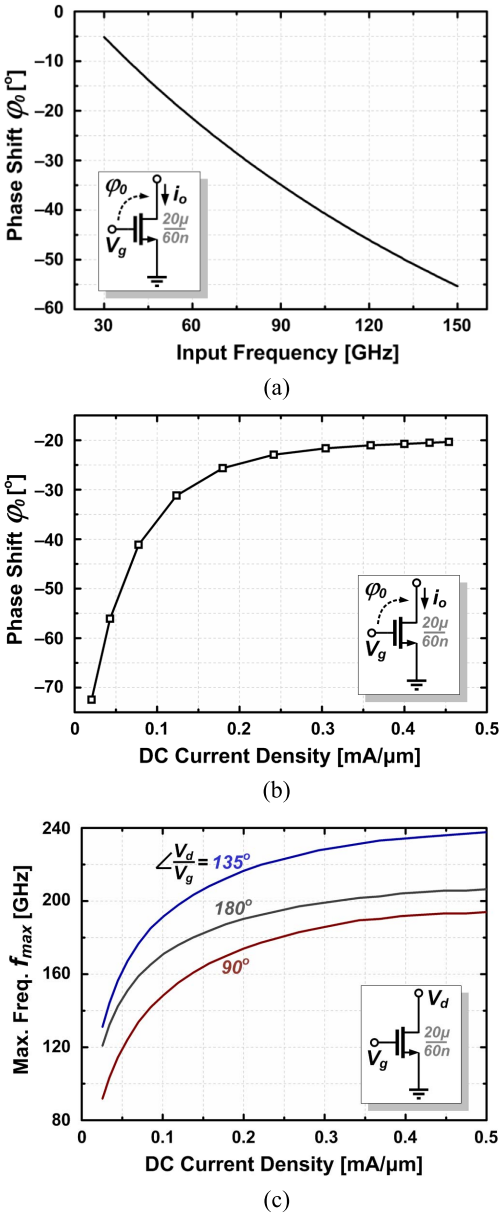



Fig. 5. (a) Simulated phase shift versus input frequency when the current density is fixed at 0.15 mA/$\mu$m. (b) Simulated phase shift at 77 GHz. (c) Simulated maximum frequency of oscillation versus dc current density at different phase shifts between the gate and the drain voltage [28].

### *B. Implicit Phase Shifters*

Considering that the phase shift $\varphi_0$ required for rotating the phase tuning is negative, it is possible to utilize the MOSFETs' delay which is notably large at mmW for implementation [26]. To analyze the delay of an NMOS transistor, its small-signal model is shown in Fig. 4(a) [27]. First, a delay exists at the gate due to the parasitic resistance, inductance, and capacitance (denoted by $-\delta_g$). Second, when the V-to-I conversion is performed by the transconductance $g_m$ in the main path, the nonzero transit time of the carriers [25] causes another delay of $-\delta_t$ between the output drain current ($g_m v_x$) and the inner gate voltage $v_x$. Third, the feedforward current $i_{gd}$ through the gate-to-drain capacitance $C_{gd}$ also contributes some phase shift. Overall, the output current from the drain ($i_d$) is the summation of $i_{gd}$ and $g_m v_x$, as depicted by the phasor diagram in Fig. 4(b). Fig. 5(a) plots the total phase delay obtained from SpectreRF simulations. Approximately, it increases proportionally with the operating frequency. From Fig. 4(b), it can be observed that the ratio between $i_{gd}$ and $g_m v_x$ varies for different $g_m$ if a constant gate voltage $v_x$ is assumed. In consequence, the delay is a function of the current density. As verified by the simulation results plotted in Fig. 5(b), a lower current density corresponds to a larger phase delay. In addition, the device size also affects the delay owing to the difference in the layout and thus the parasitics. Therefore, by optimizing the current density as well as the device size, it would be possible to obtain the required negative phase shift $\varphi_0$.

Since the oscillator cell shown in Fig. 3 consists of a differential pair and a cross-coupled pair, the delay of their NMOS transistors can be leveraged as the negative phase shift, which is ~22.5° and ~45° for the eight-phase and the four-phase oscillators, respectively. With such implicit phase shifters, no dedicate phase shifter is needed and thus both the chip area and the power consumption can be saved. Moreover, considering the much more complicated routings required and the potential instability problem attributed to multiple possible oscillation modes [20], employing explicit phase shifters would not be preferred here. However, depending on the current density required for the desired phase shift, the devices' actual $f_{\max}$ would be typically lower than the optimum. In addition, in the presence of voltage phase difference between the gate and the drain nodes $\angle(V_d/V_g)$ when the devices are deployed in a circuit topology, the achievable $f_{\max}$ would be quite different from their own theoretical $f_{\max}$ [28]. For the two-stage and four-stage *LC*-based ring oscillator

whose phasor diagrams are shown in Fig. 3, the voltage phase difference $\angle(V_d/V_g)$ is 90° and 135° for the differential pair ($M_{2\pm}$), respectively, and 180° for the cross-coupled pair ($M_{1\pm}$). Accordingly, Fig. 5(c) plots the simulated $f_{\max}$ versus dc current density at three different voltage phase shifts, 90°, 135°, and 180° [28]. Apparently, the $f_{\max}$ degrades much in some cases and the devices would then become less efficient in compensating the tank loss for sustaining oscillation. To ensure proper operation, the two transistor pairs $M_{1\pm}$ and $M_{2\pm}$ in Fig. 3(a) should not approach the region with limited $f_{\max}$ simultaneously. Therefore, in tuning the interpolated phase shifts, each the two currents ($i_1$ and $i_2$) is varied one at a time while the other is kept constant such that at least a pair of transistors can feature $f_{\max}$ far beyond the operating frequency and remain efficient. In the following discussions, the proposed frequency tuning technique will be referred as RPT to differentiate from conventional solutions.

## III. Design and Analysis of RPT Oscillators

In order to validate the proposed RPT technique, two E-band oscillators are designed: one with four-phase output and the other with eight-phase output. As shown in Fig. 6, the four-phase oscillator consists of two stages cascaded as a ring while the eight-phase one is composed of four stages. In each stage, the cross-coupled pair $M_{1\pm}$ provides the negative resistance and the differential pair $M_{2\pm}$ realizes the coupling to its proceeding stage. At the same time, their intrinsic delay is optimized to achieve the desired phase shift $\varphi_0$. No varactor is used at the $LC$ load and the frequency tuning is purely relying on RPT, which is performed by varying the tail currents $I_{b1}$ and $I_{b2}$ to adjust the interpolated phase. More specifically, all the gates of $I_{b1}$ and $I_{b2}$ are tied together and connected to two independently controlled current sources ($I_{b01}$ and $I_{b02}$) using a current-mirror configuration, respectively. In this section, the properties of the proposed RPT oscillators will be analyzed in detail.

### A. Oscillation Conditions

In the vicinity of the resonance frequency $\omega_0$, the impedance of the $LC$ tank in each oscillator stage can be approximated as

$$Z(\omega) \approx \frac{R_P}{1 + j2Q_0(\omega - \omega_0)/\omega_0} \tag{2}$$

where $R_P$ represents the equivalent parallel resistance and $Q_0$ is the quality factor. Therefore, the phase shift of the tank can be derived as

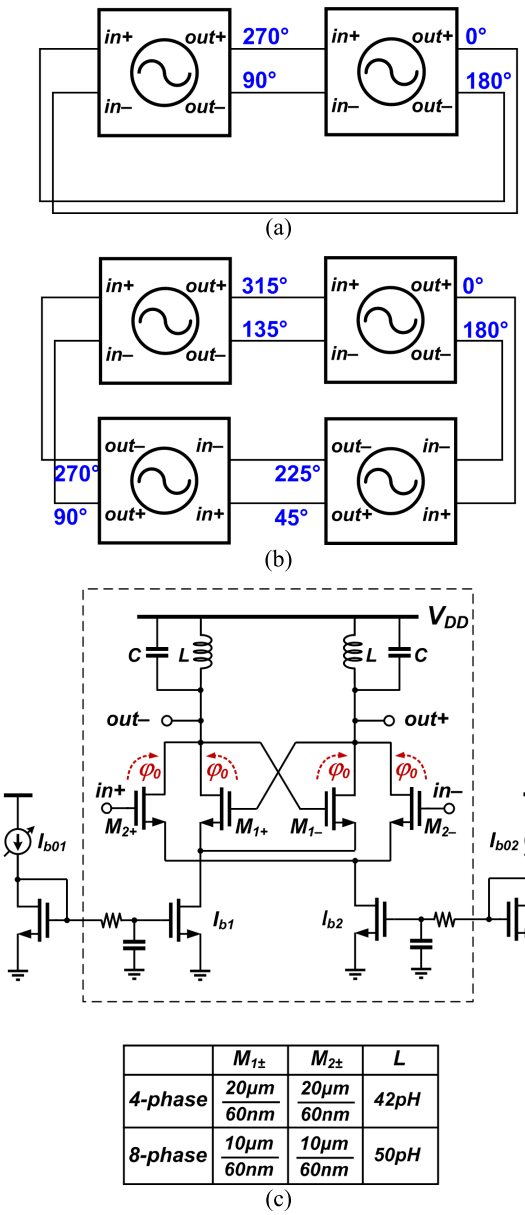
$$\angle Z(\omega) \approx -\arctan \frac{2Q_0(\omega - \omega_0)}{\omega_0}. \tag{3}$$

On the other hand, the total current injected to the $LC$ tank at the frequency $\omega$ can be derived as

$$i_t = (|i_1|\cos\varphi_1 + |i_2|\cos\varphi_2) + j(|i_1|\sin\varphi_1 + |i_2|\sin\varphi_2) \tag{4}$$

where $\varphi_1$ and $\varphi_2$ denote the phase of the currents $i_1$ and $i_2$ that are generated by $M_{1\pm}$ and $M_{2\pm}$, respectively. As such, the interpolated phase $\varphi$ can be expressed as

$$\varphi = \arctan\left(\frac{|i_1|\sin\varphi_1 + |i_2|\sin\varphi_2}{|i_1|\cos\varphi_1 + |i_2|\cos\varphi_2}\right). \tag{5}$$




| | $M_{1\pm}$ | $M_{2\pm}$ | $L$ |
|---|---|---|---|
| 4-phase | 20μm / 60nm | 20μm / 60nm | 42pH |
| 8-phase | 10μm / 60nm | 10μm / 60nm | 50pH |

(c)

Fig. 6. (a) Block diagram of the four-phase RPT oscillator. (b) Block diagram of the eight-phase RPT oscillator. (c) Schematic of the oscillator cell in each stage.

To sustain stable oscillation, the two multi-phase oscillators must fulfill both the gain and the phase conditions simultaneously. The phase condition requires that the total phase shift along the loop to be 0

$$\angle Z(\omega) + \varphi = 0. \tag{6}$$

By substituting the two terms in (6) with (3) and (5), the oscillation frequency can be derived as [26]

$$\omega \approx \omega_0 \cdot \left(1 + \frac{|i_1|\sin\varphi_1 + |i_2|\sin\varphi_2}{|i_1|\cos\varphi_1 + |i_2|\cos\varphi_2} \cdot \frac{1}{2Q_0}\right). \tag{7}$$

For the gain condition, it indicates that the voltage gain of each oscillator stage should be at least unity. Thus, by using (2), (4), and (6), it can be derived that

$$(g_{m1}\cos\varphi_1 + g_{m2}\cos\varphi_2) \cdot R_P \geq 1 \tag{8}$$

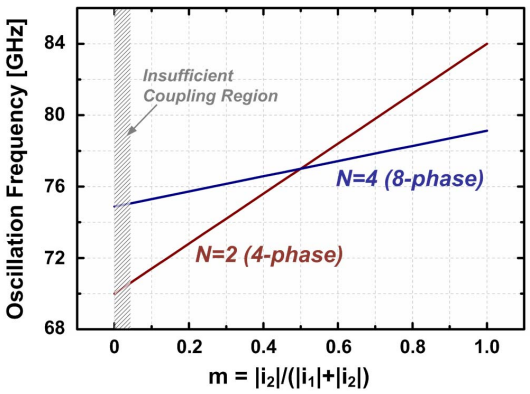



Fig. 7. Calculated oscillation frequency for the four-phase and the eight-phase RPT oscillators versus $m$.

where $g_{m1}$ and $g_{m2}$ are the transconductance of $M_{1\pm}$ and $M_{2\pm}$, respectively.

In addition to (7) and (8), it is also worthwhile to mention that sufficiently strong coupling between neighboring stages is required for the multi-phase oscillators. Otherwise, the output phases may not be accurate and the oscillator cells may even work independently at different frequencies. Therefore, the amplitude ratio $|i_2|/|i_1|$ cannot be too small.

### *B. Frequency Tuning*

By defining $m$ to be $|i_2|/(|i_1| + |i_2|)$, the oscillation frequency expressed in (7) can be rewritten as

$$\omega \approx \omega_0 \cdot \left[1 + \frac{(1-m)\sin\varphi_1 + m\sin\varphi_2}{(1-m)\cos\varphi_1 + m\cos\varphi_2} \cdot \frac{1}{2Q_0}\right]. \quad (9)$$

From (9), it can be observed that the oscillation frequency can be tuned by varying $m$. In fact, the oscillation frequency varies monotonically with $m$. Fig. 7(a) plots the frequency versus $m$ which is obtained from calculation using (9) for the four-phase and the eight-phase oscillators, in which $\varphi_1 = -\varphi_2$ is assumed to be 45° and 22.5° and $Q_0$ is assumed to be 5.5 and 7.5, respectively. Different quality factors are mainly attributed to specific design considerations, as discussed later in Section III-E. Again, to ensure sufficient coupling for oscillating as a ring, the oscillators should not be operated in the region where $m$ is too small, as shown in Fig. 7(a). Moreover, similar to conventional multi-phase oscillators consisting of multiple identical oscillation cells, the phase accuracy depends on their coupling strength. Therefore, the minimum $m$ would need to be increased according to the device mismatches and the required phase accuracy.

If hard switching is assumed for the transistor pairs $M_{1\pm}$ and $M_{2\pm}$ such that their output currents are square waves, then $i_1 = 2I_{b1}/\pi$ and $i_2 = 2I_{b2}/\pi$, resulting in $m = I_{b2}/(I_{b1}+I_{b2})$. Consequently, frequency tuning can be achieved by adjusting the tail current ratio. An effective approach is to vary each of the two bias currents ($I_{b1}$ and $I_{b2}$) one at a time while the other is kept unchanged, as mentioned in Section II-B. Apparently, since $m$ is inversely proportional to $I_{b1}$ and proportional to $I_{b2}$, the oscillation frequency decreases with $I_{b1}$ but increases with $I_{b2}$. The oscillation frequency curves obtained from calculation using (7) and from SpectreRF simulations for the two RPT oscillators are plotted in Fig. 8(a) and (b), respectively. As analyzed in Section II-B, the phase shift contributed by a transistor varies for different current densities. Therefore, assuming constant values for $\varphi_1$ and $\varphi_2$ in calculation using (7) is not strictly correct. A more accurate estimation of the oscillation frequency can be made by simulating and incorporating the phase shift variations into (7) and (9).

By assuming $m$ to be continuously variable from 0 to 1 which corresponds to tuning $I_{b2}$ from 0 to $I_{b1}$ and then tuning $I_{b1}$ from $I_{b2}$ to 0 for simplicity, the maximum tuning range of RPT oscillators can be approximated as

$$\begin{aligned} \mathrm{TR}_{\max} &\le \frac{\omega_{\max} - \omega_{\min}}{\omega_0} \approx (\tan\varphi_{02} - \tan\varphi_{01}) \cdot \frac{1}{2Q_0} \\ &= \left[\tan\varphi_{02} - \tan\left(\varphi_{02} - \frac{180^\circ}{N}\right)\right] \cdot \frac{1}{2Q_0} \end{aligned} \quad (10)$$

where $\varphi_{01}$ and $\varphi_{02}$ represent the values of $\varphi_1$ and $\varphi_2$ when $M_{1\pm}$ and $M_{2\pm}$ are biased with the default fixed current, i.e., 1 mA in Fig. 7(b), respectively. Apparently, the varying of $\varphi_1$ and $\varphi_2$ due to the current tuning does not affect the maximum achievable tuning range.

As indicated by (10), the tuning range is inversely proportional to the quality factor. In addition, it reduces with increasing of the number of stages in an RPT oscillator, assuming that the gain condition expressed by (8) is satisfied. Interestingly, by equating $\partial TR_{\max}/\partial\varphi_{02}$ to 0, it turns out that $\varphi_{02} = 90^\circ/N$ corresponds to a minimum value of $\mathrm{TR}_{\max}$. Therefore, in the presence of some phase errors which inevitably exist in real implementation, the tuning range could be larger, but the gain condition might become a concern if $\varphi_{02}$ deviates from $90^\circ/N$ too much.

The proposed oscillators in Fig. 6 feature frequency tuning in current domain and their output frequencies are very sensitive to the current control signals. To operate them within a conventional phase-locked loop (PLL), several improvements can be applied. First, each of the two current tails in the oscillation cells can be decomposed into an array of current sources which are binarily weighted and controlled digitally. By doing so, the high tuning sensitivity can be greatly reduced. Second, since there are two signals to be controlled for frequency tuning as indicated by Fig. 7(b), a switching circuity is required to switch in the control signal to be connected with the charge pump's output. Third, considering that the tuning slopes are negative and positive when varying $I_{b1}$ and $I_{b2}$, respectively, the two inputs of the phase frequency detector (PFD) in PLL would need to be swapped depending on which bias current is tuned. Fourth, V-to-I conversion circuitry can be integrated such that the voltage control signal from the charge pump can be directly used for fine-tuning the frequency continuously.

### *C. Oscillation Amplitude*

By multiplying (2) with (4) and then using (6), the oscillation amplitude can be derived as

$$|v_{\text{out}}| = |i_t||Z(\omega)| = (|i_1|\cos\varphi_1 + |i_2|\cos\varphi_2)R_P. \quad (11)$$

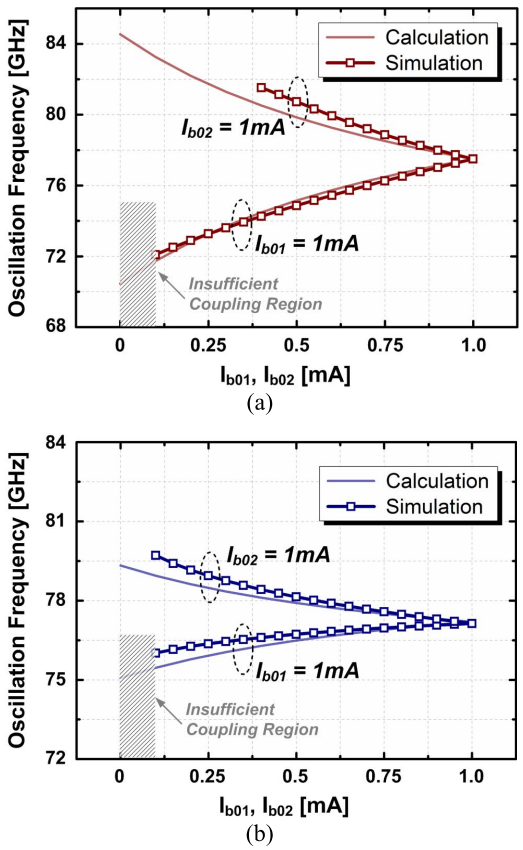



Fig. 8. Calculated and simulated oscillation frequency versus the tuning currents ($I_{b01}$ fixed at 1 mA while $I_{b02}$ varied from 0 to 1 mA, and vice versa). (a) Four-phase RPT oscillator. (b) Eight-phase RPT oscillator.

To verify (11), following the frequency tuning method in Section III-B, the calculated and simulated oscillation amplitude for the eight-phase RPT oscillator are plotted in Fig. 9. A little discrepancy is expected mainly due to the hard-switching approximation of the transistors in calculation. From (11), it can be observed that the output amplitude would vary much if one of the currents, $|i_1|$ and $|i_2|$, is adjusted while the other is kept unchanged for frequency tuning. Quantitatively, assuming the first and the second current contribution terms in (11) are equal for simplicity, the ratio of the minimum to the maximum output amplitude can be quickly estimated as 1/2. Simulations in SpectreRF verify that the output amplitude variations of the two oscillators in Fig. 6 are both around ±3 dB. Fortunately, as oscillators are generally followed by buffers to increase the driving capability and to ensure sufficient isolation from subsequent building blocks in a system, the undesired amplitude variations will be greatly suppressed. For instance, if buffers with classical differential topology which typically consists of a differential input

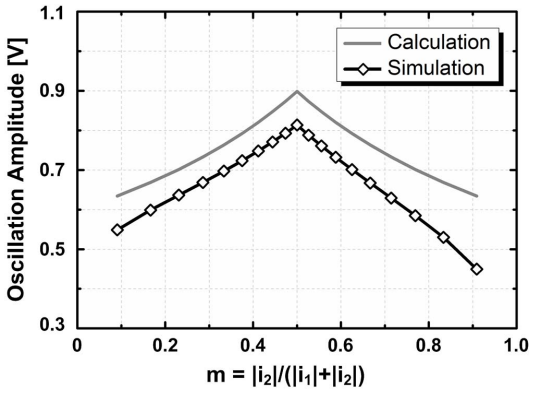



Fig. 9. Calculated and simulated oscillation amplitude versus $m$ for the eight-phase RPT oscillator.

transistor pair, a tail current and an $LC$ load are employed, a ±3-dB amplitude variation at the input will only induce ±0.5-dB difference at the output, as indicated by SpectreRF simulation. On the other hand, if relatively constant amplitude is required directly at the oscillator's output, then $|I_{b1}|$ and $|I_{b2}|$ can be tuned in a differential way such that the current ratio $m$ is varied but their magnitude sum ($|I_{b1}|+|I_{b2}|$) is kept constant. As such, ($|i_1|+|i_2|$) remains the same and the total magnitude variation of the two current terms in (11) would get greatly reduced.

### D. Phase Noise

Owing to the multiple oscillator stages used in an $N$-stage oscillator, the number of noise sources is $N$ times as that in a single-stage oscillator, resulting in an increase of the total noise power by $N$. On the other hand, the presence of $N$ $LC$ tanks attenuates the noise by a factor of $N^2$. As a consequence, compared with a single-stage oscillator, an $N$-stage $LC$ oscillator features overall phase noise improvement of $10\log_{10} N$ dB theoretically [29]. However, two important effects should be also taken into account in practice. At first, as the $LC$ tank has to provide a phase shift of $\varphi$, the quality factor will be lower than the intrinsic $Q_0$ at the resonance frequency. From (1) and (5), the effective $Q$ can be written as

$$Q \approx \frac{Q_0(|i_1|\cos\varphi_1 + |i_2|\cos\varphi_2)}{\sqrt{(|i_1|\sin\varphi_1 + |i_2|\sin\varphi_2)^2 + (|i_1|\cos\varphi_1 + |i_2|\cos\varphi_2)^2}}. \tag{12}$$

The second effect is the degradation of oscillation amplitude due to RPT. As indicated by (11), the output amplitude is smaller than $|i_1|+|i_2|$ in the presence of phase shift $\varphi_1$ and $\varphi_2$.

$$\mathcal{L}(\Delta\omega) \approx 10\log_{10}\left[\frac{kT}{N}\cdot\frac{1}{Q^2}\cdot\frac{\pi^2}{4}\cdot\frac{1}{(|i_1|\cos\varphi_1 + |i_2|\cos\varphi_2)^2 R_P}\cdot\left(\frac{\omega}{\Delta\omega}\right)^2\cdot(1+F)\right] \tag{13}$$

$$\mathcal{L}(\Delta\omega) \approx 10\log_{10}\left[\frac{kT}{N}\cdot\frac{1}{Q^2}\cdot\frac{\pi^2}{4}\cdot\frac{1}{(|i_1|+|i_2|)^2\cos^2\frac{90^\circ}{N}R_P}\cdot\left(\frac{\omega}{\Delta\omega}\right)^2\cdot(1+F)\right] \tag{14}$$

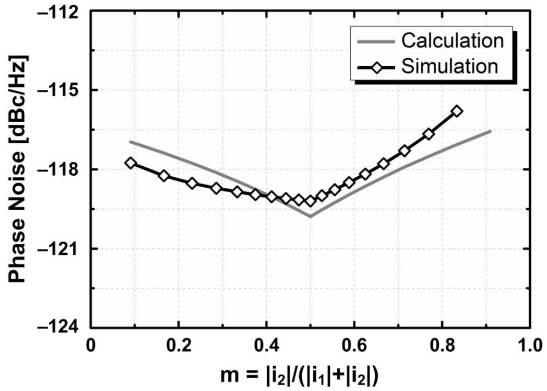



Fig. 10. Calculated and simulated phase noise at 10-MHz offset versus $m$ for the eight-phase RPT oscillator.

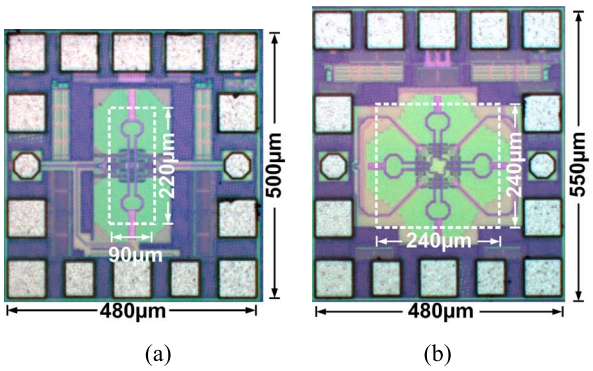



Fig. 11. Chip micrographs of (a) four-phase RPT oscillator and (b) eight-phase RPT oscillator.

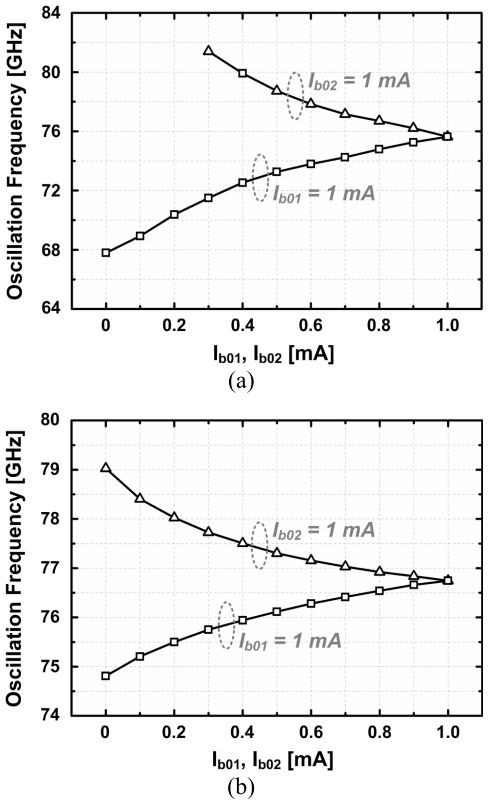



Fig. 12. Measured frequency tuning curves. (a) Four-phase RPT oscillator. (b) Eight-phase RPT oscillator.

By utilizing Leeson's equation [30], the phase noise of an $N$-stage RPT oscillator can be derived as (13) shown at the bottom of the previous page. In (13), $k$ is Boltzmann's constant and $F$ is the excess noise factor to account for the noise contributed by other devices besides the *LC* tanks [20]. Again, if both $\varphi_1$ and $\varphi_2$ are set to $90°/N$ such that the RPT is optimal, (13) can be simplified as (14). Equation (14), shown at the bottom of the previous page, indicates that a high quality factor of the *LC* tanks directly helps lower the phase noise, which is similar to other *LC*-based oscillators. In addition, more stages in an RPT oscillator are also beneficial to its phase noise at the expense of higher power consumption.

Similar to other multi-phase oscillators which are composed of multiple oscillation stages coupled together in a ring [10], [24], the excess noise factor $F$ in (12) mostly originates from the thermal noise contributions from both the cross-coupled pair $M_{1\pm}$ and the differential pair $M_{2\pm}$. Using the approximation for $F$ in [31], the phase noise contributed by the thermal noise of $R_P$ and the transistors $M_{1\pm}$ and $M_{2\pm}$ is calculated for the eight-phase RPT oscillator. The calculated and simulation results are plotted in Fig. 10, which indicates good agreement and in turn verifies (14). However, since the relative magnitude of the two current branches inside each oscillation cells directly affects the interpolated phase and hence the oscillation frequency, AM-to-PM conversion would be more dominant than that in conventional *LC* oscillators. Furthermore, as the thermal noise is proportional to the transconductance which is a function of the bias current, it can be derived that the phase noise contributed by $M_{1\pm}$ and $M_{2\pm}$ increases with $I_{b1}$ and $I_{b2}$, respectively. Similarly, the theoretically strong AM-to-PM conversion will also cause significant $1/f$ upcoversion. As a result, the phase noise would be degraded in both the $1/f^2$ and the $1/f^3$ regions.

Overall, the phase noise improvement is still notably large because of the higher effective quality factor and the multi-stage *LC* filtering in the proposed RPT oscillators. Simulations indicate that the $1/f$ corner frequency is lower than 400 kHz. If necessary, the phase noise in the $1/f^3$ region can be greatly attenuated first by properly designing the PLL's bandwidth in the frequency synthesizer and then compensated with the help of a digital carrier tracking loop in the baseband when an entire RF system is integrated [32], [33].

Finally, it is noteworthy mentioning that in the presence of PVT variations or modeling inaccuracy which would inevitably cause $\varphi_1$ and $\varphi_2$ deviated from optimum, the interpolated current vector will become unevenly distributed around the tank's resonance peak such that the worst phase noise will be degraded.

### *E. Design Considerations*

From the above analysis, it can be expected that the four-phase RPT oscillator would have wider tuning range while the eight-phase one could exhibit better phase noise

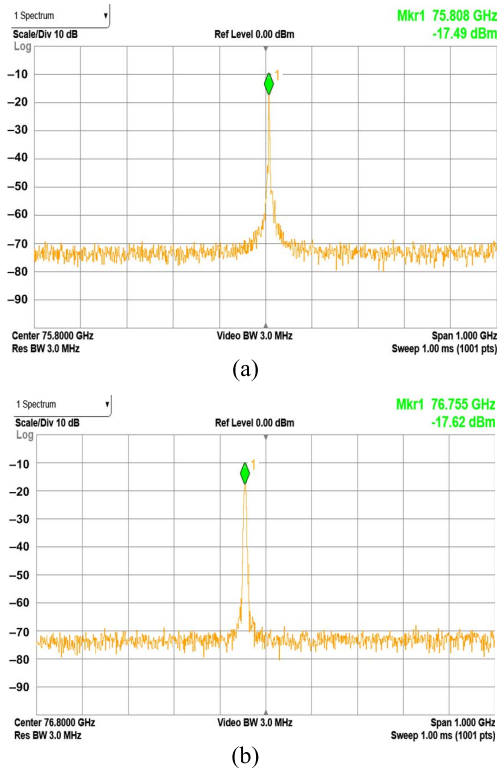



Fig. 13. Measured output spectrum. (a) Four-phase RPT oscillator. (b) Eight-phase RPT oscillator.

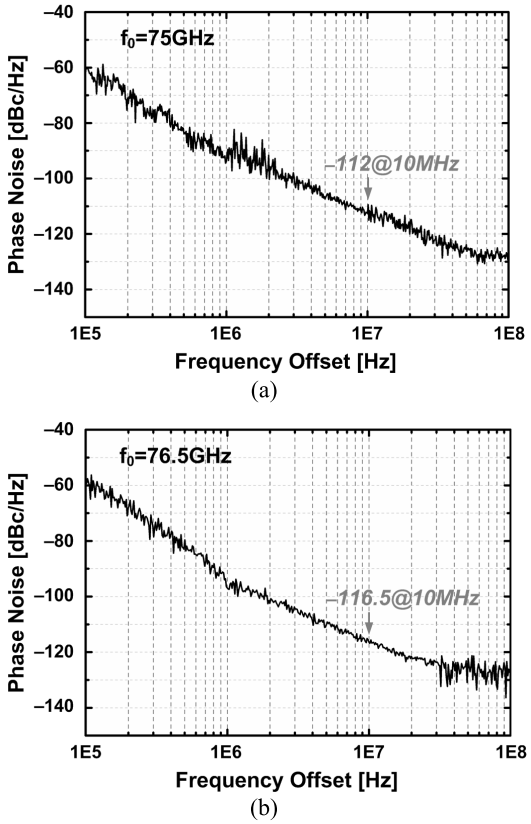



Fig. 14. Measured phase noise. (a) Four-phase RPT oscillator. (b) Eight-phase RPT oscillator.

performance. To facilitate amplitude control for phase interpolation, the transistor pairs $M_{1\pm}$ and $M_{2\pm}$ are designed to be of the same size in each of the two RPT oscillators. Then, their detailed dimensions are determined based on the gain condition, with enough margins included to ensure proper startup of the oscillation. As such, the aspect ratio of the transistors in the four-phase oscillator is larger than that in the eight-phase oscillator, as listed in Fig. 6(c). Afterward, the current density of the transistors is optimized. Differential microstrip lines are employed for making connections between neighboring stages and they are carefully modeled by using full-wave electromagnetic (EM) simulator. Eventually, the negative phase shifts corresponding to the optimal RPT ($\sim$45° for the four-phase oscillator and $\sim$22.5° for the eight-phase oscillator) are achieved approximately in post-layout simulations.

The differential inductor in each oscillator stage is implemented by a single differential coil with a center tap to save area and to improve quality factor. Mainly attributed to the difference in transistor size and thus the parasitics, the quality factor of the *LC* tank is not the same for the two oscillators. With the transistor model provided by the foundry and the inductor model obtained from EM simulations, it turns out that the tank $Q$ is $\sim$5.5 and $\sim$7.5 for the four-phase and the eight-phase RPT oscillators. Consequently, the former can achieve a tuning range of $\sim$3 times wider than the latter. On the other hand, both the higher tank $Q$ and the larger number of *LC* tanks used help improve the phase noise of the eight-phase RPT oscillator.

## IV. Experimental Results

The two proposed RPT oscillators shown in Fig. 6 were fabricated in a 65-nm CMOS process. The top thick metal is chosen for the inductor windings to minimize its resistive loss and thus to improve the quality factor. Highly symmetrical floorplan is realized by placing the oscillator stages properly. Fig. 11(a) and (b) shows the chip photographs, which occupy core areas of $0.09 \times 0.22$ mm$^2$ and $0.24 \times 0.24$ mm$^2$ excluding pads for the four-phase and the eight-phase RPT oscillators, respectively. For testing purpose, open-drain buffers are included to route the mmW signals out and to drive the input impedance of the equipment. In addition, down-conversion mixers are also integrated to down-convert the high-frequency signals to characterize the phase errors. All measurements were performed in chip-on-board assemblies, with the mmW outputs observed by on-wafer probing while the dc and low-frequency pads directly wire-bonded to the printed circuit board (PCB).

For spectrum measurement, the high-frequency signals from the oscillators are down-converted by an external harmonic mixer (Keysight M1970W) and then measured with a signal analyzer (Keysight PXA N9030B). The oscillation frequency is tuned by varying each of the two bias currents, i.e., $I_{b01}$ and $I_{b02}$, one at a time while the other remains unchanged. Fig. 12(a) and (b) plots the measured frequency tuning curves. The four-phase RPT oscillator measures tuning ranges from 67.8 to 75.6 GHz and from 75.6 to 81.4 GHz, with $I_{b02}$ and $I_{b01}$ tuned, respectively. For the eight-phase

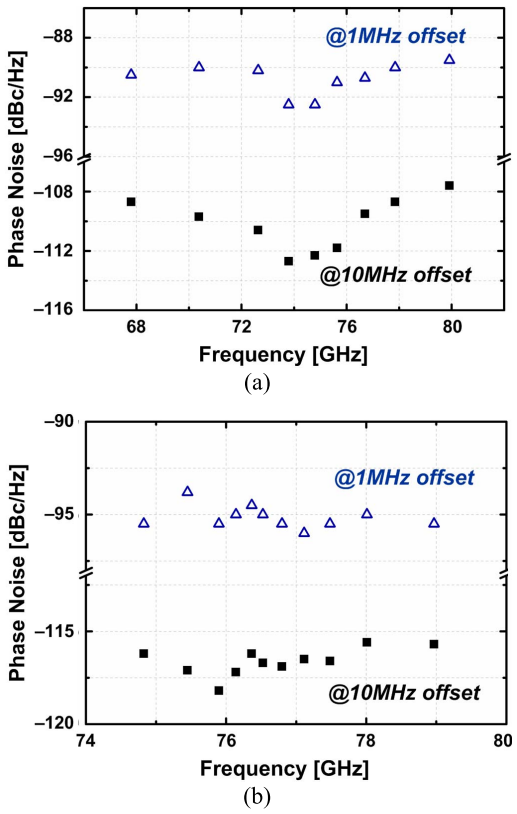



Fig. 15. Measured phase noise at 1- and 10-MHz offsets versus oscillation frequency. (a) Four-phase RPT oscillator. (b) Eight-phase RPT oscillator.

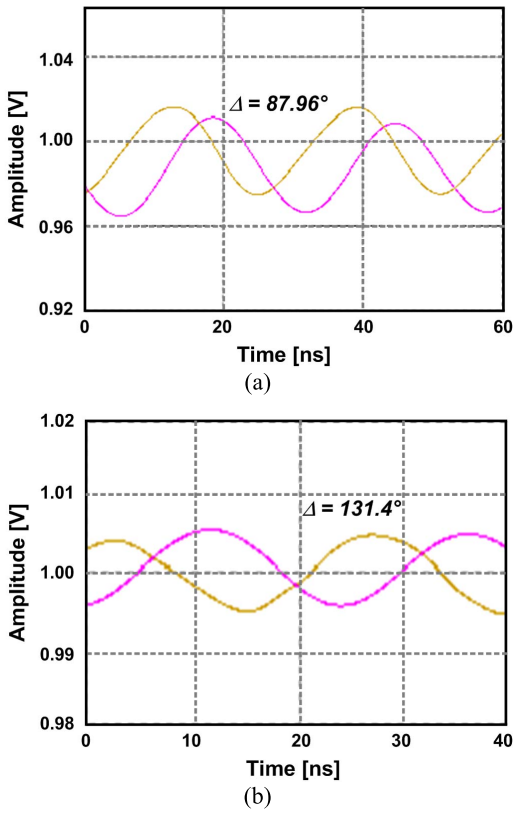



Fig. 16. Measured transient waveforms of the down-converted signals. (a) Four-phase RPT oscillator. (b) Eight-phase RPT oscillator.

oscillator, its output frequency can be tuned from 74.8 to 79 GHz in total. When the bias current $I_{b02}$ is 0, there is still some current flowing through the tail current $I_{b2}$ due to the non-negligible leakage in nanoscale transistors. As long as the coupling strength is sufficient and thus the oscillator stages are able to injection lock each other to output a single frequency tone, $I_{b02} = 0$ is allowed. On the other hand, the upper limit on the current ratio is determined by whether the gain condition can be satisfied. Due to this reason, $I_{b01}$ cannot be arbitrarily small for the four-phase RPT oscillator such that the maximum current ratio $m$ cannot exceed 0.8. Fig. 13(a) and (b) shows the measured output spectrum when the two oscillators are oscillating at around 76 GHz. The measured power variations are ∼6.5 and ∼5.5 dB for the four-phase and eight-phase RTP oscillators within their output frequency ranges, respectively. Fig. 14(a) and (b) shows the measured phase noise plot at 75 and 76.5 GHz for the four-phase and the eight-phase RPT oscillators, respectively. Within the entire tunable frequency ranges, their phase noise at 10-MHz offset frequency measures from −108 to −113 dBc/Hz and from −116 to −118 dBc/Hz, as plotted in Fig. 15(a) and (b), respectively. The two oscillators both consume similar dc power of 13 to 25 mW from 1-V supply.

With the LO port fed by an external signal generator, the on-chip mixers down-convert the mmW outputs to around several tens of megahertz. Fig. 16 shows the transient waveforms obtained using an oscilloscope for each of the two RPT oscillators. The measured phase errors are within 4.2° and 3.6° for the four-phase and the eight-phase oscillators, respectively, and their amplitude mismatches are within 1.5 dB.

Table I summarizes the measured performance of the two proposed RPT oscillators and compares to recently published state-of-the-art E-band multi-phase frequency generation circuits. The FoM characterizes the overall performance in terms of oscillation frequency, phase noise, and power consumption, while the FoM$_T$ and FoM$_A$ additionally takes the tuning range and the chip area into account, respectively, as shown in the following [11], [34]:

$$\text{FoM} = 10\log_{10}\left[\left(\frac{f_0}{\Delta f}\right)^2 \frac{1}{\mathcal{L}(\Delta f)\cdot P_{\text{diss}}|_{\text{mW}}}\right] \quad (15)$$

$$\text{FoM}_T = \text{FoM} + 20\log_{10}\left(\frac{\text{TR}|_{\%}}{10}\right) \quad (16)$$

$$\text{FoM}_A = \text{FoM} - 10\log_{10}\left(A|_{\text{mm}^2}\right) \quad (17)$$

where $f_0$ is the oscillation frequency, $\mathcal{L}(\Delta f)$ is the phase noise at frequency offset of $\Delta f$, $P_{\text{diss}}|_{\text{mW}}$ is the dissipated power in mW, $TR|_{\%}$ is the tuning range in percentage, and $A|_{\text{mm}^2}$ is the occupied core area in mm$^2$. With the proposed RPT technique, the four-phase oscillator achieves the widest frequency tuning range of 18.2% and the highest average FoM$_T$ of 180.5 dB compared to existing E-band fundamental quadrature oscillators, while both FoM and FoM$_A$ are among the highest. In addition, the eight-phase oscillator demonstrates the highest average FoM of 181.5 dB.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH E-BAND MULTI-PHASE FREQUENCY GENERATION CIRCUITS

| References | This Work | | [6] TMTT '16 | [35] ESSCIRC '14 | [36] ASSCC '16 | [37] TMTT '13 | [38] ISSCC '15 |
|---|---|---|---|---|---|---|---|
| Topology | Fund. Osc. | Fund. Osc. | Fund. Osc. | Fund. Osc. | Fund. Osc. | Fund. Osc. + PPF | Fund. Osc.+ Tripler |
| $f_{min}$ [GHz] | 67.8 | 74.8 | 71.4 | 83.7 | 89.4 | 70 | 70.5 |
| $f_{max}$ [GHz] | 81.4 | 79.0 | 76.1 | 88.7 | 100.9 | 89 | 85.5 |
| TR [GHz / %] | 13.6 / 18.2 | 4.2 / 5.5 | 4.7 / 6.4 | 5 / 5.8 | 11.5 / 12.1 | 19 / 23.9 | 15 / 19.2 |
| Tuning Tech. | Rotated-phase-tuning | | Varactor | Varactor | Magnetic | Varactor | Varactor |
| Output Phases | 4 | 8 | 4 | 4 | 4 | 4 | 4 |
| Phase Noise [dBc/Hz] | –108 / –113 @10MHz | –116 / –118 @10MHz | –114 / –117 @10MHz | –109 / –119 @10MHz | –99 / –107 @10MHz | –87 / –94 @1MHz | –88 / –92 @1MHz |
| Supply [V] | 1 | 1 | 0.7 | 0.7 | 0.7 | 3.3 | 1.2 |
| Power [mW] | 13 to 25 | 13 to 25 | 35.6 | 28.4 | 7.6 | 310.2 | 47.3 |
| Core Area [$mm^2$] | 0.02 | 0.06 | 0.03 | 0.03 | 0.02 | 0.11 | 0.29 |
| FoM [dB] | 173 / 178 | 180 / 183 | 176 / 179 | 173 / 183 | 170 / 177 | 159 / 168 | 170 / 172 |
| $FoM_T$ [dB] | 178 / 183 | 175 / 178 | 172 / 175 | 169 / 179 | 172 / 179 | 165 / 176 | 176 / 178 |
| $FoM_A$ [dB] | 190 / 195 | 193 / 196 | 191 / 194 | 188 / 198 | 187 / 194 | 169 / 178 | 175 / 177 |
| Technology | 65nm CMOS | 65nm CMOS | 28nm CMOS | 40nm CMOS | 65nm CMOS | 0.35μm SiGe | 65nm CMOS |

## V. CONCLUSION

An RPT technique was proposed to tune the oscillation frequency of multi-phase mmW oscillators without using varactors. The negative phase shift required for RPT was implemented by reusing the transistors that are essential for sustaining oscillation as implicit phase shifters. Fabricated in the 65-nm CMOS technology, a four-phase oscillator featuring the widest tuning range of 18% from 67.8 to 81.4 GHz and the highest average $FoM_T$, and an eight-phase oscillator operating from 74.8 to 79 GHz with the highest average FoM have been demonstrated.

## REFERENCES


[1] K. Okada *et al.*, "Full four-channel 6.3-Gb/s 60-GHz CMOS transceiver with low-power analog and digital baseband circuitry," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 46–65, Jan. 2013.

[2] P.-J. Peng, P.-N. Chen, C. Kao, Y.-L. Chen, and J. Lee, "A 94 GHz 3D image radar engine with 4TX/4RX beamforming scan technique in 65 nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 656–668, Mar. 2015.

[3] Y. Chao, L. Li, and H. C. Luong, "An 86-to-94.3 GHz transmitter with 15.3 dBm output power and 9.6% efficiency in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan./Feb. 2016, pp. 345–346.

[4] D. Guermandi *et al.*, "A 79 GHz binary phase-modulated continuous-wave radar transceiver with TX-to-RX spillover cancellation in 28 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 354–355.

[5] H. Wu, N.-Y. Wang, Y. Du, and M.-C. F. Chang, "A blocker-tolerant current mode 60-GHz receiver with 7.5-GHz bandwidth and 3.8-dB minimum NF in 65-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 3, pp. 1053–1062, Mar. 2015.

[6] M. Vigilante and P. Reynaert, "Analysis and design of an E-band transformer-coupled low-noise quadrature VCO in 28-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 4, pp. 1122–1132, Apr. 2016.

[7] M. Tabesh *et al.*, "A 65 nm CMOS 4-element sub-34 mW/element 60 GHz phased-array transceiver," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 3018–3032, Dec. 2011.

[8] A. Natarajan, A. Komijani, X. Guan, A. Babakhani, and A. Hajimiri, "A 77-GHz phased-array transceiver with on-chip antennas in silicon: Transmitter and local lo-path phase shifting," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2807–2819, Dec. 2006.

[9] U. Decanis, A. Ghilioni, E. Monaco, A. Mazzanti, and F. Svelto, "A low-noise quadrature VCO based on magnetically coupled resonators and a wideband frequency divider at millimeter waves," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2943–2955, Dec. 2011.

[10] L. Wu and H. C. Luong, "A 49-to-62 GHz quadrature VCO with bimodal enhanced-magnetic-tuning technique," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 10, pp. 3025–3033, Oct. 2014.

[11] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.

[12] J. J. Rael and A. A. Abidi, "Physical processes of phase noise in differential LC oscillators," in *Proc. IEEE Custom Integr. Circuits Conf.*, May 2000, pp. 569–572.

[13] T.-Y. Lu, C.-Y. Yu, W.-Z. Chen, and C.-Y. Wu, "Wide tunning range 60 GHz VCO and 40 GHz DCO using single variable inductor," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 2, pp. 257–267, Feb. 2013.

[14] S. Elabd, S. Balasubramanian, Q. Wu, T. Quach, A. Mattamana, and W. Khalil, "Analytical and experimental study of wide tuning range mm-Wave CMOS LC-VCOs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 5, pp. 1343–1354, May 2014.

[15] J. Zhang, N. Sharma, W. Choi, D. Shim, Q. Zhong, and K. K. O, "85-to-127 GHz CMOS signal generation using a quadrature VCO with passive coupling and broadband harmonic combining for rotational spectroscopy," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1361–1371, Jun. 2015.

[16] Y. Chao and H. C. Luong, "Analysis and design of wide-band millimeter-wave transformer-based VCO and ILFDs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 9, pp. 1416–1425, Sep. 2016.

[17] W. Fei, H. Yu, H. Fu, J. Ren, and K. S. Yeo, "Design and analysis of wide frequency-tuning-range CMOS 60 GHz VCO by switching inductor loaded transformer," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 3, pp. 699–711, Mar. 2014.

[18] E. Mammei, E. Monaco, A. Mazzanti, and F. Svelto, "A 33.6-to-46.2 GHz 32 nm CMOS VCO with 177.5 dBc/Hz minimum noise FOM using inductor splitting for tuning extension," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 350–351.

[19] J. Yin and H. C. Luong, "A 57.5-90.1-GHz magnetically tuned multimode CMOS VCO," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1851–1861, Aug. 2013.

[20] S. Rong and H. C. Luong, "Design and analysis of varactor-less interpolative-phase-tuning millimeter-wave LC oscillators with multiphase outputs," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1810–1819, Aug. 2011.
[21] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, Sep. 2004.
[22] J. V. D. Tang, P. V. D. Ven, D. Kasperkovitz, and A. V. Roermund, "Analysis and design of an optimally coupled 5-GHz quadrature LC oscillator," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 657–661, May 2002.
[23] H. Wang and A. Hajimiri, "A wideband CMOS linear digital phase rotator," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2007, pp. 671–674.
[24] A. Mirzaei, M. E. Heidari, R. Bagheri, S. Chehrazi, and A. A. Abidi, "The quadrature LC oscillator: A complete portrait based on injection locking," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1916–1932, Sep. 2007.
[25] P. Andreani, A. Bonfanti, L. Romano, and C. Samori, "Analysis and design of a 1.8-GHz CMOS LC quadrature VCO," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1737–1747, Dec. 2002.
[26] L. Wu, S. Liao, and Q. Xue, "A 312-GHz CMOS injection-locked radiator with chip-and-package distributed antenna," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 2920–2933, Nov. 2017.
[27] R. Han and E. Afshari, "A CMOS high-power broadband 260-GHz radiator array for spectroscopy," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3090–3104, Dec. 2013.
[28] O. Momeni and E. Afshari, "High power terahertz and millimeter-wave oscillator design: A systematic approach," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 583–597, Mar. 2011.
[29] P. Andreani and X. Wang, "On the phase-noise and phase-error performances of multiphase LC CMOS VCOs," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1883–1893, Nov. 2004.
[30] D. B. Leeson, "A simple model of feedback oscillator noise spectrum," *Proc. IEEE*, vol. 54, no. 2, pp. 329–330, Feb. 1966.
[31] L. Romano, S. Levantino, C. Samori, and A. L. Lacaita, "Multiphase LC oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 7, pp. 1579–1588, Jul. 2006.
[32] T. Siriburanon *et al.*, "A low-power low-noise mm-wave subsampling PLL using dual-step-mixing ILFD and tail-coupling quadrature injection-locked oscillator for IEEE 802.11ad," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1246–1260, May 2016.
[33] J. R. Pelliccio *et al.*, "Phase noise effects on OFDM wireless LAN performance," *Appl. Microw. Wireless*, vol. 13, no. 7, pp. 68–78, 2011.
[34] B. Soltanian, H. Ainspan, W. Rhee, D. Friedman, and P. R. Kinget, "An ultra-compact differentially tuned 6-GHz CMOS LC-VCO with dynamic common-mode feedback," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1635–1641, Aug. 2007.
[35] M. Vigilante and P. Reynaert, "An E-band low-noise transformer-coupled quadrature VCO in 40 nm CMOS," in *Proc. Eur. Solid-State Circuits Conf.*, 2014, pp. 423–426.
[36] X. Liu, C. Chen, J. Ren, and H. C. Luong, "Transformer-based varactor-less 96 GHz–110 GHz VCO and 89 GHz–101 GHz QVCO in 65 nm CMOS," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2016, pp. 357–360.
[37] I. Nasr, B. Laemmle, K. Aufinger, G. Fischer, R. Weigel, and D. Kissinger, "A 70–90-GHz high-linearity multi-band quadrature receiver in 0.35-$\mu$m SiGe technology," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4600–4612, Dec. 2013.
[38] Z. Huang, H. C. Luong, B. Chi, Z. Wang, and H. Jia, "A 70.5-to-85.5 GHz 65 nm phase-locked loop with passive scaling of loop filter," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 448–450.

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