A 10-bit 2.6-GS/s Time-Interleaved SAR ADC With a Digital-Mixing Timing-Skew Calibration Technique

Chin-Yu Lin, Yen-Hsin Wei, and Tai-Cheng Lee, *Senior Member, IEEE*

***Abstract*— A 16-channel time-interleaved 10-bit SAR analog-to-digital converter (ADC), employing the proposed delta-sampling auxiliary SAR ADCs and a digital-mixing calibration technique to compensate timing-skew error, achieves a 2.6-GS/s sampling rate. The ADC has been fabricated in a 40-nm CMOS technology and achieves a 50.6-dB signal-to-noise-and-distortion ratio at Nyquist rate while dissipating 18.4 mW from a 1.1-V power supply. The digital calibration improves interleaving spurious tones from −33.6 to −63.2 dB in the best case.**

***Index Terms*— Delta-sampling auxiliary SAR analog-to-digital converter (ADC), digital-mixing calibration, figure of merit (FoM), interleaving spurious tone, time-interleaved SAR ADC, timing skew.**

I. Introduction

RECENTLY, radio architectures, such as 802.11ad (WiGig) and the next-generation mobile communication system (5G), require analog-to-digital converters (ADCs) with bandwidth beyond a gigahertz and effect number of bit of 6–8 bits while remaining excellent power efficiency for longer battery life. This implies that the conversion rate of multi-GS/s of the ADC is highly demanded for such applications. To achieve the GS/s sampling rate, pipelined ADCs are typically preferable for their superior throughput. However, several high-gain and wide-bandwidth op-amps are needed to maintain the accuracy and linearity, leading to power-hungry design. Besides, the low supply voltages and the reduced intrinsic gain in advanced technologies are not favorable for op-amp-based ADC designs. In another way, time interleaving is proposed to increase the overall speed of ADC. Also, time interleaving can relax the speed and power tradeoff and lower the limited conversion rate of a single-channel ADC in an energy efficient way. Furthermore, SAR ADC has recently become one of the attractive choices used for interleaved system for its simple structure, and good power efficiency in the advanced technology. The sweet spot of the SAR ADC is found to locate around 10-bit and 200–300 MS/s designs [1], [2], which is suitable to be a unit cell in the time-interleaved ADC. However, the mismatches between each channel such as offset mismatch, gain mismatch, and timing mismatch still degrade the overall performance of the system and thus call for calibration techniques, and there would be overhead for interleaved ADCs. The correction of offset and gain mismatch is very straightforward and can be compensated in the digital domain. In contrast, timing-skew mismatch is more difficult to be corrected because the skew-induced error is dependent on signal content. Exploring timing-skew calibration technique is one of the major topics of this paper.

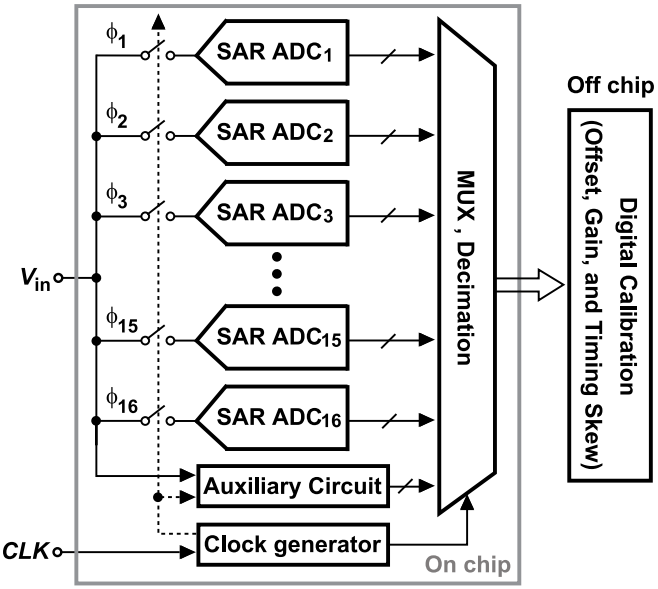

Fig. 1. System block diagram of the proposed ADC.

To minimize the front-end sample-and-hold (S/H) design effort, many time-interleaved ADCs are developed in the distributed sampling scheme, leaving the timing-skew problem resolved by calibration. Few timing-skew calibration algorithms have been reported for interleaved ADCs to correct timing error in the analog domain [3]–[6] or in the digital domain [7]. The drawback of the analog correction includes the feedback-induced stability hazard, jitter introduced by the controlled delay line and long convergence time. The digital-domain correction takes advantage from technology scaling but the complex digital slope-extraction filter for error acquisition limits the signal bandwidth. The proposed ADC [8] demonstrates a digital timing-skew correction algorithm

Manuscript received May 6, 2017; revised August 19, 2017 and October 17, 2017; accepted January 3, 2018. Date of publication January 30, 2018; date of current version April 23, 2018. This paper was approved by Associate Editor Andrea Baschirotto. This work was supported in part by Mediatek Inc. and in part by the Ministry of Science and Technology both under Contract 103-2622-E-002-034. (*Corresponding author*: *Tai-Cheng Lee.)*

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Digital Object Identifier 10.1109/JSSC.2018.2793535

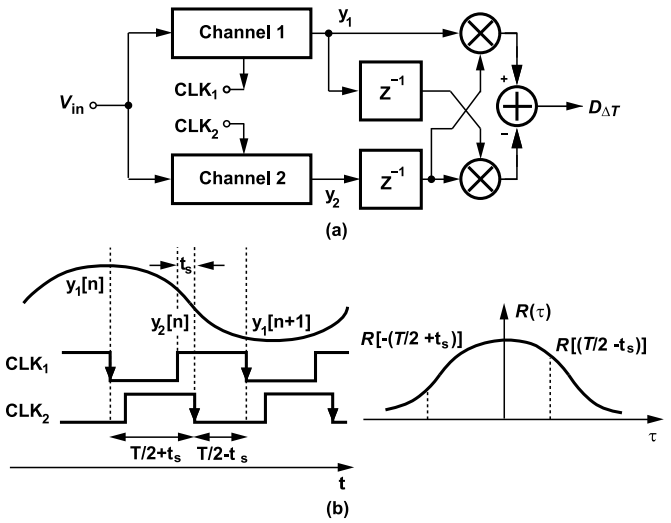

Fig. 2. (a) Two-channel TI ADC with the digital-mixing method. (b) Principle of digital mixing.

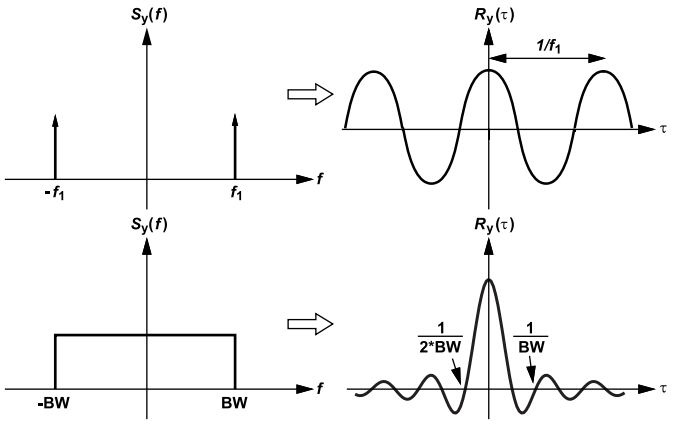

Fig. 3. Autocorrelation functions of a sinusoidal wave and a band-limited signal.

incorporating with a delta-sampling technique for mixed-signal skew detection, achieving a wide signal bandwidth. As shown in Fig. 1, a 10-bit 2.6-GS/s ADC is implemented by interleaving 16 SAR ADCs whose sampling rate is 162.5 MS/s. The analog auxiliary circuit including eight auxiliary delta-sampling ADCs collaborates with digital circuits to estimate the skew error in the digital domain. After that, the ADC outputs are corrected digitally without any feedback. In addition to skew error, the gain and offset compensations are included in the calibration engine. The digital parts of calibration circuits are implemented by software for proof of the concept in this prototype.

This paper is organized as follows. In Section II, the concept of the proposed timing-skew calibration is introduced. Section III describes the proposed delta-sampling ADC architecture for signal difference extraction which minimizes the overhead of analog auxiliary circuitry. A detailed time-interleaved system implementation of the prototype and the mismatch analysis between main and auxiliary ADCs are included in Section IV. Finally, Sections V and VI outline the experimental results and the conclusion, respectively.

II. Proposed Timing-Skew Calibration

This section describes the proposed timing calibration scheme. First, a digital-mixing method [5] for timing-skew estimation will be introduced. Then the proposed timing-skew correction is elaborated with its basic principle, architecture, and calibration algorithm. Last, the design consideration and signal difference extractions which reduce the analog design effort for the proposed calibration are discussed.

A. Digital-Mixing Skew Detection

The timing skew can be detected via digital-mixing method which calculates two autocorrelation function values in the digital domain and takes their difference as the timing-skew estimation, as shown in Fig. 2(a) by using a dual-channel time-interleaved ADC as an example. The two clocks are out of phase if there is no timing skew and their clock period is $1/f_s$. As shown in Fig. 2(b), with the order of channel 1, channel 2, and then channel 1, let the three consecutive samples denoted as $y[-(T/2+t_s)+nT]$, $y[0+nT]$, and $y[(T/2-t_s)+nT]$, respectively, where the three arguments stand for the three consecutive sampling time instants, T is the sampling period of each channel, t_s is the timing skew, and n is the discrete time index. Also, their corresponding outputs are represented as $y_1[n]$, $y_2[n]$, and $y_1[n+1]$, respectively. By manipulating the outputs of the dual-channel ADC, digital mixing calculates both of the autocorrelation functions $R(\tau)$, one from samples of $y[-(T/2+t_s)+nT]$ to $y[0+nT]$ and the other from those of $y[0+nT]$ to $y[(T/2-t_s)+nT]$, as shown in the following:

$$R[-(T/2+t_s)] = \sum y_1[n]y_2[n] \tag{1}$$

$$R[T/2-t_s] = \sum y_2[n]y_1[n+1]. \tag{2}$$

Therefore, for small value of t_s, the difference between (1) and (2) is derived as follows:

$$\begin{aligned} E_t &= R[-(T/2+t_s)] - R(T/2-t_s) \\ &= R(T/2+t_s) - R(T/2-t_s) \\ &= 2t_s[R(T/2+t_s) - R(T/2-t_s)]/(2t_s) \\ &\sim 2t_s \frac{dR(\tau)}{d\tau}\bigg|_{\tau=T/2}. \end{aligned} \tag{3}$$

The estimated timing-skew information is proportional to the skew t_s with a proportional factor that depends on the signal statistics, i.e., the first derivative of its autocorrelation function. In addition, the skew detection ability for different kinds of signals is discussed. Fig. 3 shows the autocorrelation functions of a sinusoidal wave and a stationary signal having a uniform spectrum across a limited bandwidth. For a sinusoidal wave with frequency f_1, the autocorrelation is a *cosine* wave. For a band-limited signal with uniform spectrum in that bandwidth, the autocorrelation is a *sinc* function. In general, it can be shown that for modulated and non-modulated signals, skew information can be derived from the derivative of their autocorrelation function around τ. With this information, the sampling instant of the channel 2 ADC could be adjusted earlier or later

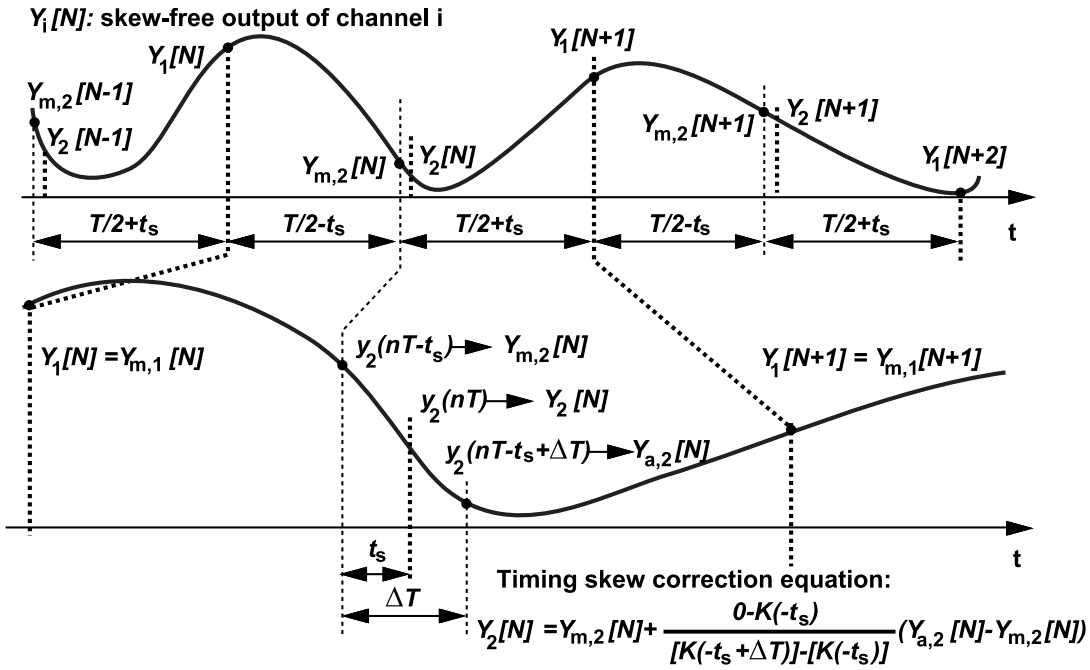

Fig. 4. Skew calibration algorithm for a two-channel ADC.

in an analog manner depending on the polarity of E_t. Rather than tuning the sampling instant, in this paper, a digital feedforward correction is proposed with the digital-mixing skew detection to reduce analog circuit complexity.

B. Proposed Digital Timing-Skew Correction

The timing skew in each channel can cause phase modulation in an interleaved system. Specifically, the amplitude difference between the actual sampled value and the ideal sampled value without timing skew is called the skew-induced sampling error here. Unlike offset and gain errors in the interleaved ADC, the sampling error is in essence a function of the input signal frequency. Thus, without the knowledge of the input frequency beforehand, manipulating the estimated timing skew cannot directly correct the error since it is a function of the input frequency. Instead, it would call for some feedback iteration between estimation and correction to minimize the error until convergence done. An all-digital feedforward skew calibration is reported in [7]. Without loss of generality, the timing skew is assumed to be much smaller than the period of the high-frequency signal. Then, for input signal $x(t)$, the sampled values with timing skew of t_s from the ideal sampling instance of t_i in a certain channel i can be modeled by the first-order Taylor series approximation

$$x(t_i + t_s) \approx x(t_i) + t_s \cdot \frac{dx}{dt}(t_i). \tag{4}$$

The first term on the right-hand side of (4) is the ideal sampled value, and the second one is the sampling error term modeled by the multiplication of the skew t_s and the first-order derivative of the input signal. Alternatively, the other Taylor series approximation can be expressed as

$$x(t_i) = x(t_i + t_s - t_s) \approx x(t_i + t_s) + (-t_s)\frac{dx(t_i + t_s)}{dt}. \tag{5}$$

Equation (5) can be seen as the correction equation where the first term on the right-hand side is the skewed sampled value, and the second one is the correction term. Therefore, what we need to know to operate the sampling error correction is the first-order derivative of the signal, or the slope and the timing skew. However, most of the timing-skew estimation methods [5], [6] only determine the relative timing skew rather than the absolute value because they just need a rough estimation or the polarity of the specific timing skew for analog skew calibration. Also, the estimation amount may differ from different input statistics even for the same timing skew. Therefore, (5) could not be evaluated directly as in [7] if digital mixing is employed for skew detection. Rather than calculating the signal derivative and the exact timing skew, the proposed method estimates the error by interpolating or extrapolating between the sampled point and an auxiliary point. If an auxiliary point $x(t_i + t_s + \Delta T)$ is available around the sampled point $_x(t_i + t_s)$, (5) can be rewritten as

$$\begin{aligned} x(t_i) &= x(t_i + t_s - t_s) \\ &\approx x(t_i + t_s) - K \cdot t_s \cdot \frac{x(t_i + t_s + \Delta T) - x(t_i + t_s)}{K \cdot (t_s + \Delta T) - K \cdot t_s} \end{aligned} \tag{6}$$

where K is a constant and $\Delta T \ll 1$. Fortunately, this result has both the estimated skew terms in the numerator and the denominator if all the estimate skew values are first-order proportional to the input signal statistics. These statistics-dependent factors can be cancelled without defecting the estimated sampling error as the input statistics varies. With the input-statistics-independent sampling error estimated in hand, the sampling error can be directly corrected without any feedback or iteration between estimation and correction to minimize the error.

The detail operation of the proposed timing skew calibration is illustrated in Fig. 4, where a dual-channel ADC is shown for simplicity. As shown in Fig. 4, the skew-free quantized

sequence of channel i is denoted as $Y_i[N]$ and T is the sampling period of each single channel. First, channel 1 can be treated as the reference, and the sampling instant of the channel 2 is skewed by $-t_s$ due to the non-ideality of the sampling circuits. The sampling instant of the auxiliary channel 2 ADC for slope estimation is intentionally skewed by ΔT from the actual sampling instant of the channel 2. Therefore, channel 2 samples the input with value $y(nT-t_s)$ and its corresponding quantized output is denoted as $Y_{m,2}[N]$. The auxiliary channel 2 samples the input with value $y(nT-t_s+\Delta T)$ and the quantized one is denoted as $Y_{a,2}[N]$. The two quantity $-t_s$ and $-t_s+\Delta T$ which are skew time index of the channel 2 and the auxiliary one, respectively, can be estimated by the digital-mixing method, as illustrated in Fig. 4. Using the outputs of ADCs, digital mixing calculates the difference of the autocorrelation functions R from channel 1 to channel 2 and from channel 2 to its succeeding channel 1, both for the nominal and auxiliary outputs in channel 2. They are derived as (7) and (8), respectively

$$R[-(T/2-t_s)]-R(T/2+t_s) = \sum_n [Y_{m,1}(n)Y_{m,2}(n)] - \sum_n [Y_{m,1}(n+1)Y_{m,2}(n)] \quad (7)$$

$$R[-(T/2-t_s+\Delta T)]-R(T/2+t_s-\Delta T) = \sum_n [Y_{m,1}(n)Y_{a,2}(n)] - \sum_n [Y_{m,1}(n+1)Y_{a,2}(n)]. \quad (8)$$

It can be proven that the values calculated in (7) and (8) are proportional to the timing skew of main and auxiliary outputs. Thus, the timing-skew information of both outputs can be estimated as two digital quantities denoted as $K\times(-t_s)$ and $K\times(-t_s+\Delta T)$, where K is a proportional factor that depends on the signal statistics and has been proven as the first-order derivative of the autocorrelation in Section II-A.

Since the main and auxiliary signal paths samples the same input signal with slightly delay ΔT compared to the total accumulation period, multiple of T, so that the sampled input signal statistics can be the same for both paths. Therefore, it is reasonable to assume that K remains the same for both of main and auxiliary signal paths. However, the sampling clock jitter may disturb the measurement of the timing skew. In this design, 16 384 samples are accumulated to suppress the deviation of the estimated timing skew for each calibration cycle. Because the three sampled values of $Y_{m,2}[N]$, $Y_{a,2}[N]$, and the $Y_2[N]$ corresponding to the main channel 2, the auxiliary channel 2, and the ideal channel 2, respectively, are close in time, the three sampling points can be approximately connected by a straight line for signal up to Nyquist frequency with the proper choice of ΔT. The following equation shows the linear approximation of the three outputs:

$$\frac{Y_2(N)-Y_{m,2}(N)}{0-K\cdot(-t_s)} = \frac{y_{a,2}(N)-y_{m,2}(N)}{K\cdot(-t_s+\Delta T)-K\cdot(-t_s)}. \quad (9)$$

With (9), the correction equation is derived as

$$Y_2(N) = Y_{m,2}(N) + \frac{0-K\cdot(-t_s)}{K\cdot(-t_s+\Delta T)-K\cdot(-t_s)}(Y_{a,2}(N)-Y_{m,2}(N)). \quad (10)$$

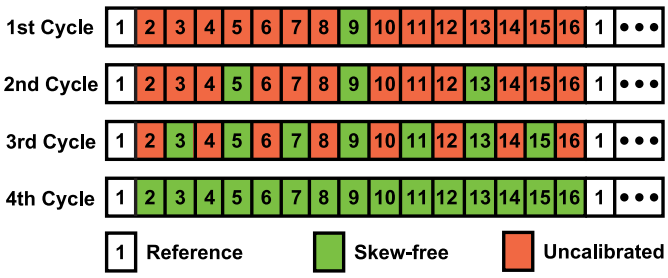

Fig. 5. Calibration sequences for a 16-channel interleaved ADC.

Although the statistics-dependent factor K, t_s, and ΔT appear in the equation, none of them needs to be known in advance. Once the autocorrelation of the main channels and the auxiliary channels is estimated, $K\times(-t_s)$ and $K\times(-t_s+\Delta T)$, as shown in (10), are available for the correction. Furthermore, rather than adjusting the analog variable-delay line, the realization of (10) can be implemented fully in the digital domain. Specifically, timing-skew correction equation (10) has the same form as Taylor series approximation in (6). However, one should notice that the noise in auxiliary ADC would be injected to the output and degrade the SNR of 3 dB for the worst case.

Fig. 5 shows the timing-skew calibration sequence for a 16-channel interleaved ADC. First, make channel 1 as the reference channel, estimate and correct the skew of channel 9. After channel 9 is calibrated, channel 1 and channel 9 could be employed as the reference channels for the skew correction of channels 5 and 13. According to system simulations, 16 384 sampling points are required in every calibration cycle to achieve a 10-bit accuracy. The process continues and the number of the calibrated channels grows exponentially until all the outputs are corrected. It takes four calibration cycles for the 16-channel time-interleaved ADC to be compensated. The algorithm can be implemented both in foreground or background, depending on the application scenario. The skew detection can perform one time at startup. However, if the user would like to track the skew continuously, the detection can be activated without interrupting the normal operation.

C. Design Consideration

The design consideration for the proposed correction scheme is mainly focused on how to choose the intentional delay ΔT between main and auxiliary ADCs. If the added skew is too large to maintain the linear approximation, the residue interleaving spurs would remain at certain level and corrupt the signal-to-noise-and-distortion ratio (SNDR) even the skew correction has been performed. The following equation describes the situation that the linear approximation causes the approximation error as large as 0.5 LSB for a 10-bit resolution:

$$2\pi f_{\mathrm{Nyq}}(-t_s+\Delta T)-\sin[2\pi f_{\mathrm{Nyq}}(-t_s+\Delta T)] = 1/1024 \quad (11)$$

where f_{Nyq} is the Nyquist frequency. The value of $(-t_s+\Delta T)$ is around 22 ps for an ADC running at 2.6 GS/s with a 1.3-GHz Nyquist input. Here, the intentional skew ΔT

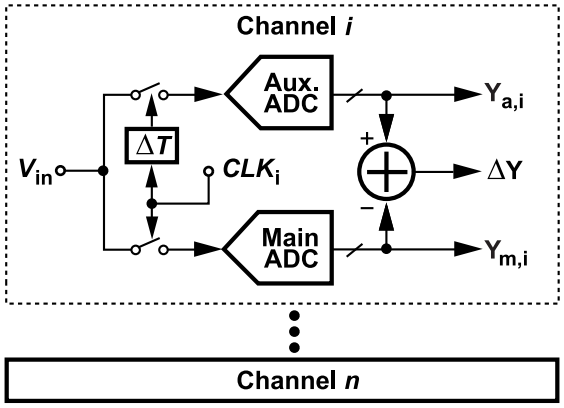

Fig. 6. Dual ADCs for skew calibration.

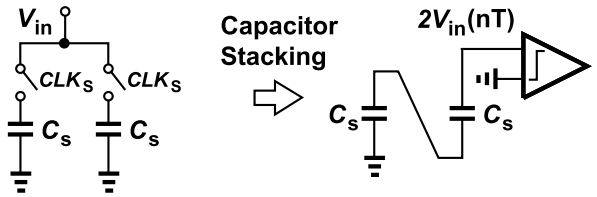

Fig. 7. Conventional capacitive charge pump.

is designed to be 10 ps. Assume that the timing skew is controlled within 10 ps, the ratio $t_s/\Delta T$ will not exceed 1 which guarantees the SNDR degradation is less than 6 dB at Nyquist rate.

D. Signal Difference Extraction

According to the previous introduction, the calibration is accomplished by evaluating the signal derivative with the help of the auxiliary outputs. From the correction equation, what we need is the signal difference between the actual and the auxiliary sampling points. The intuitive implementation is employing an identical ADC beside the original ADC with a sampling clock delayed by ΔT, as shown in Fig. 6. But this implementation results in twice power and area consumptions. Owing to the extraction of the signal difference rather than the entire signal range, employing a full-range auxiliary ADC is not a proper solution. Assume that the extra delay is 10 ps and input frequency of 1.3 GHz, the maximum ΔY is about 42 LSBs which is less than 6-bit dynamic range. If the difference can be obtained in the analog domain before A/D conversion, more power and area could be reduced. Therefore, a delta-sampling operation is proposed to perform difference extraction before ADC and the difference is then digitized for the proposed timing-skew calibration.

III. Proposed Delta-Sampling SAR ADC

The advantage of extracting signal difference before A/D conversion for timing-skew calibration can reduce hardware significantly. Therefore, the implementation of the analog difference extraction and its succeeding digitized operation will be explored in this section.

A. Delta-Sampling Operation

The operation is based on capacitor stacking to perform addition of input signals, as shown in Fig. 7. In [9], a simple charge pump combined with a source follower is proposed to achieve 2× stage gain in the pipelined stages. An 11-bit SAR ADC with embedded passive gain is also reported in [10]. The sampling capacitors serve for charge pump after sampling phase and provide a signal gain of 2× prior to the comparator without much power penalty to relax the comparator noise requirement. Inspired by the 1.5-bit differential capacitive charge pump multiplying DAC converter shown in Fig. 8 which involves both signal polarities in the single-ended implementation for better common-mode rejection, the possibility of performing delta-sampling operation by capacitive charge pump with differential signaling is investigated.

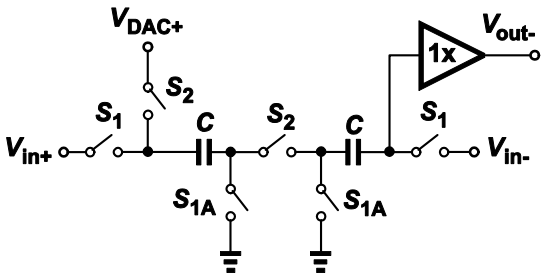

Fig. 8. 1.5-bit differential capacitive charge pump MDAC.

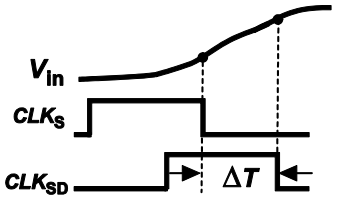

Fig. 9. Concept of delta-sampling operation.

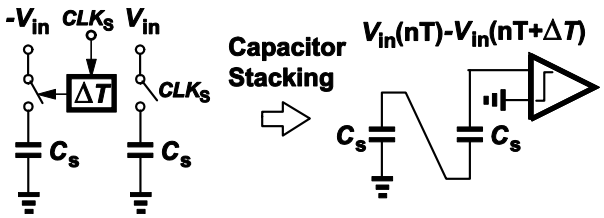

Fig. 10. Concept of delta-sampling operation.

The delta-sampling scheme captures the signal difference between two adjacent timing instants which forms a window ΔT, as shown in Fig. 9. Basically, it does the subtraction on the two sampled values which are sampled at two different timing instants. Recall the operation of the conventional capacitive charge pump. After sampling, it does the summation on the two fixed values which are sampled at the same instant. If the sign of one of the input signals is inverted and one of the sampling clocks is delayed, the delta sampling is completed within the specific timing slot, as shown in Fig. 10.

B. Circuit Implementation

Through the delta-sampling operation, the required analog information is stored in the sampling capacitors. However, the digital representation of the signal difference is nec-

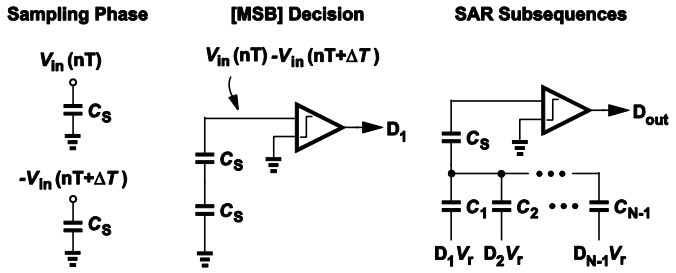

Fig. 11. *N*-bit delta-sampling SAR ADC.

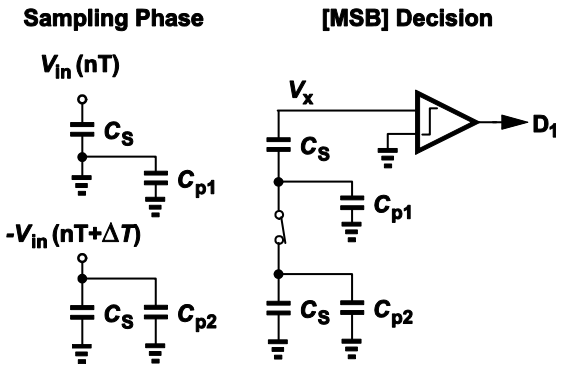

Fig. 12. Delta-sampling equivalent circuits with parasitic capacitors.

essary rather than the analog one in the proposed timing-skew calibration. Thus, quantization has to be proceeded after delta sampling. The SAR architecture combines the S/H circuit and the digital-to-analog converter (DAC) in a single capacitor array which makes it suitable for digitizing signal difference after delta sampling in a compact and low-power manner. For simplicity, Fig. 11 shows a single-ended implementation for an *N*-bit delta-sampling SAR ADC. After sampling, the capacitor stacking evaluates the signal difference at the input of the comparator. Afterward, the $(N-1)$-bit DAC which is decomposed from the lower C_s generates the corresponding analog values according to the comparison results in sequence for SAR A/D conversion.

However, if the dominant parasitic capacitor between the sampling capacitors is included in the [MSB] decision phase, the gains of the top-plate sampled value to the delta-sampling output for the two sampling capacitors are different. In that case, a full-scale fluctuation appears at the output which occupies the dynamic range of the delta-sampling ADC and saturates the output. This phenomenon will be discussed analytically by the effective circuit model, as shown in Fig. 12. If the parasitic capacitors C_{p1} and C_{p2} are considered, we can defined $\alpha = C_{p1}/(C_s + C_{p2})$. Then, the voltage at node x is given by

$$V_x = V_{\text{in}}(nT) - \frac{1}{1+\alpha}V_{\text{in}}(nT+\Delta T) = \frac{V_{\text{in}}(nT) - V_{\text{in}}(nT+\Delta T)}{1+\alpha} + \frac{\alpha}{1+\alpha}V_{\text{in}}(nT). \quad (12)$$

As one can see, in addition to signal difference with gain of $1/(1+\alpha)$, a full-scale signal feeds through to the output with $\alpha/(1+\alpha)$ gain. Take the maximum digital representation of a 10-bit full-scale signal to be 1023. Assume that $\alpha = 0.1$,

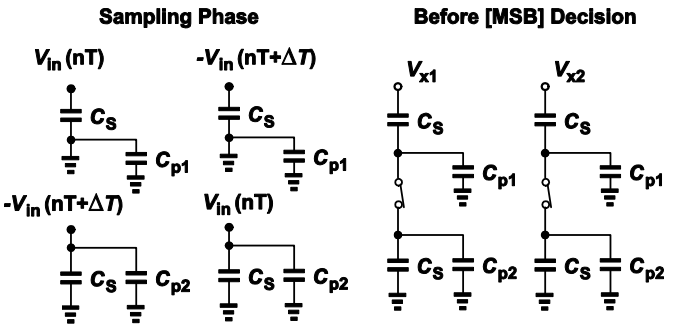

Fig. 13. Dual-path delta-sampling ADC.

the feed through part would be about 102 which are much larger than the maximum signal difference. Thus, the output is dominated by the signal feed through rather than the desired result.

To resolve this issue, a dual-path charge pump circuit shown in Fig. 13 is employed to neutralize the feed through. An identical circuit is applied along with the original path but all the inputs and the sampling clocks are reversed. The voltages at x_1 and x_2 are given by

$$V_{x1} = \frac{V_{\text{in}}(nT) - V_{\text{in}}(nT+\Delta T)}{1+\alpha} + \frac{\alpha}{1+\alpha}V_{\text{in}}(nT)$$
$$V_{x2} = \frac{V_{\text{in}}(nT) - V_{\text{in}}(nT+\Delta T)}{1+\alpha} - \frac{\alpha}{1+\alpha}V_{\text{in}}(nT+\Delta T). \quad (13)$$

After the charge redistribution, the output would be

$$V_{\text{out}} = \frac{1+0.5\alpha}{1+\alpha}[V_{\text{in}}(nT) - V_{\text{in}}(nT+\Delta T)]. \quad (14)$$

Therefore, the fluctuation is cancelled and only the signal difference is available at the output with the gain slightly less than 1. As mentioned before, the dynamic range of the delta-sampling ADC is less than 6 bits when operating at Nyquist rate. To place a few design margins, a 7-bit delta-sampling SAR ADC is implemented in the prototype. Fig. 14 shows the circuit implementation and the corresponding timing diagram for better understanding of the operation. Note that only the single-ended schematic is shown for simplicity.

IV. Implementation of 16-Times Interleaved ADC

A. Interleaved Architecture

Fig. 15 examines the collaboration between main and auxiliary ADCs in detail. In addition to the main 16-channel ADC, eight delta-sampling ADCs are employed to extract the signal difference for skew calibration. Because the delta-sampling ADCs deal with less signal range, they can operate twice faster than the main ADCs. Therefore, one more interleaving hierarchy is created between main and auxiliary ADCs. Two main ADCs share a single delta-sampling ADC which further reduces the number of auxiliary ADCs. Take channels 1 and 9 for example, ADC_{a1} interleaves between ADC_{m1} and ADC_{m9}. When ADC_{m1} samples the input, ADC_{a1} samples the signal difference within ΔT. And ADC_{a1} does exactly the same task in the sampling phase of ADC_{m9}. The simulated power

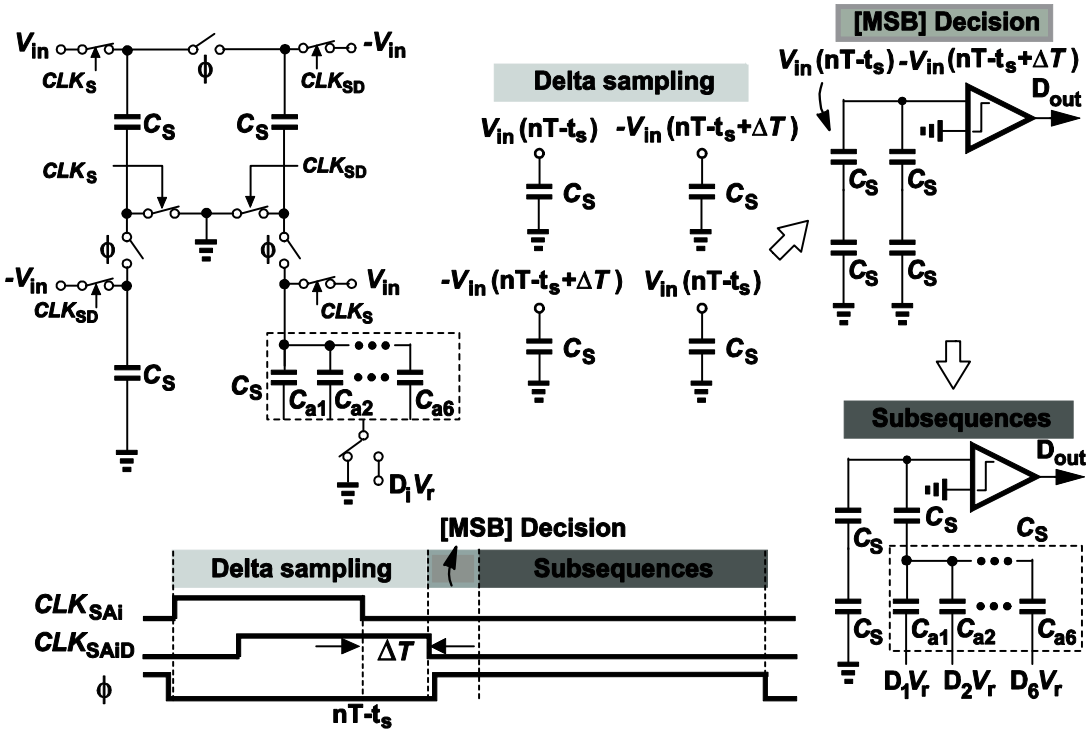

Fig. 14. Detailed circuit implementation and timing diagram.

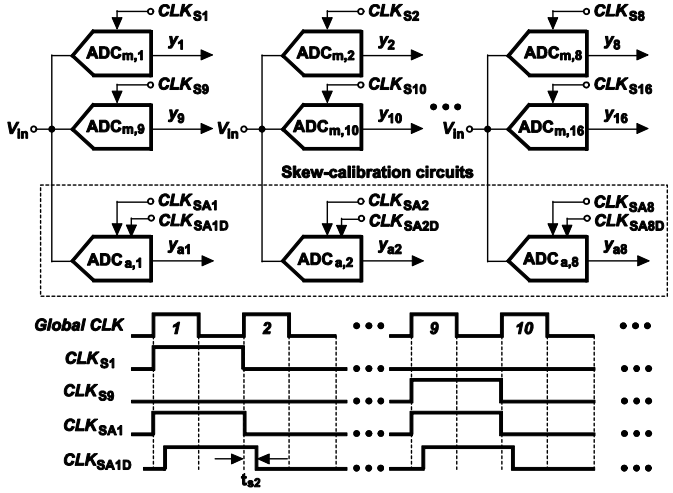

Fig. 15. Block and clock diagrams of the proposed ADC.

consumption of the auxiliary ADC is about 82% of the main ADC. Considering the number of the auxiliary ADCs is half of that of the main ADCs, the power overhead is 41%. Compared with the design which employs an identical ADC as an auxiliary ADC, the delta-sampling technique saves 59% of power consumption. Besides, the loading increases about 40%. Each 10-bit SAR ADC employs top-plate sampling to acquire the analog input signal with a 1.4-$V_{pp,diff}$ swing. The differential DAC with the split capacitor switching scheme [11] is used to maintain the common-mode voltage and the LSB capacitor with set-and-down switching is used to save the total capacitor by half. Besides, the direct switching technique [12] is applied to speed up the conversion rate. A unit capacitor of 1.2 fF is

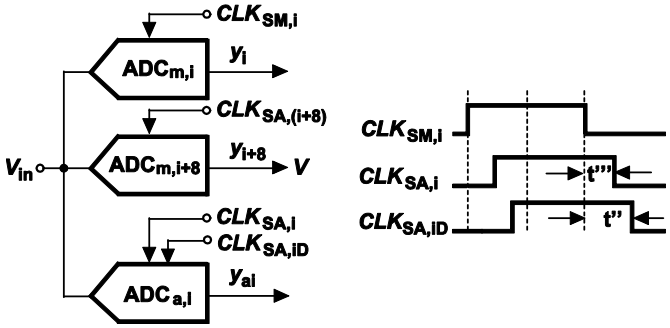

Fig. 16. Mismatches between main and auxiliary ADCs.

chosen and the common centroid arrangement in the DAC is employed to reduce mismatch effect.

B. Mismatches Between Main and Auxiliary ADCs

In addition to mismatches among all the main ADCs, employing auxiliary ADCs also introduces mismatches between main and auxiliary ADCs, as shown in Fig. 16. Similarly, they gain mismatch, offset mismatch, and timing skew. These mismatches might degrade the interleaving spurs. The offset of the auxiliary ADCs is also calibrated along with the main channel offset calibration, leaving the gain and timing-skew mismatches to be carefully analyzed.

First, how the gain error between main and auxiliary ADCs affects the acquisition of skew error is discussed. Fig. 17 describes the linear approximation model which is adopted in the proposed timing-skew calibration. Assume that the sampling instant is skewed from 0 to t' and the added

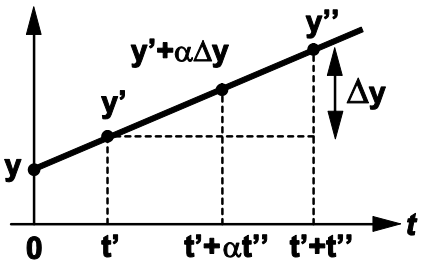

Fig. 17. Linear approximation model with auxiliary ADC gain error.

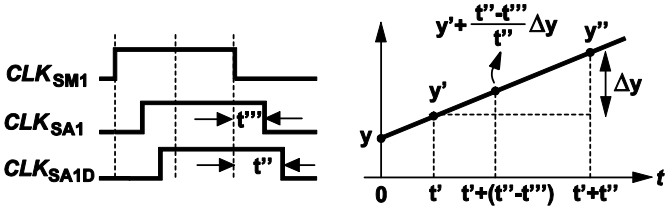

Fig. 18. Linear approximation model with timing skew.

delay is t'', the corresponding sampled values are y, y', and y''. And the ideal signal difference is defined as Δy. If the relative gain error of auxiliary ADC is α, the output becomes $\alpha\Delta y$. Therefore, the digital mixing results in Kt' and $K\alpha t'$, respectively. Take these parameters into the correction equation; the corrected result is given by

$$y = y' - \frac{Kt'}{K\alpha t''}(\alpha\Delta y) = y' - \frac{t'}{t''}(\Delta y). \tag{15}$$

As one can see, $\alpha$is cancelled and calibrated output remains unchanged even in the presence of gain error. The behavioral simulation shows that ± 40 % variation of α results in spurious tones less than 65 dB. If α is too large, the approximation error becomes large; whereas small α makes the signal difference too small to be detectable. To guarantee the accuracy of the correction, the presence of the non-linear parasitics which might invalidate the linear approximation should also be addressed. In this paper, because the delta-sampling ADC operates under a relatively low signal level, the non-linear behavior can be greatly reduced. In addition, both the main and the auxiliary ADCs are designed to have the linearity better than 10 bits which makes the linear model still hold within a 10-bit level.

Then the timing skew between main and auxiliary ADCs is discussed. Fig. 18 shows clocking diagram and the linear approximation model in the presence of timing skew. Because the sampling clocks of the main and auxiliary ADCs are generated by different buffers, there is skew t'' between $\mathrm{CLK_{SM1}}$ and $\mathrm{CLK_{SA1}}$. Under linear approximation, the ideal signal difference Δy is scaled by $(t'' - t''')/t''$. And the equivalent added delay becomes $t'' - t'''$. Take these parameters into the correction equation; the corrected output is given by

$$y = y' - \frac{Kt'}{K(t'' - t''')}\left(\frac{t'' - t'''}{t''}\Delta y\right) = y' - \frac{t'}{t''}(\Delta y). \tag{16}$$

Obviously, the corrected value remains the same. Therefore, the timing skew between the main and auxiliary ADCs is tolerable as long as the linear approximation is guarantee. That is, the total skew should be less than 22 ps as mentioned before. One more issue is the sampling imbalance between the main and the auxiliary ADCs that could be lumped as bandwidth mismatch. The bandwidth mismatch can be decomposed to gain and phase (timing skew) mismatches which are tolerable according to the analysis above. The delta-sampling ADC only captures the voltage difference rather than the absolute voltage around the sampling instant and this explains the tolerance of bandwidth mismatch intuitively.

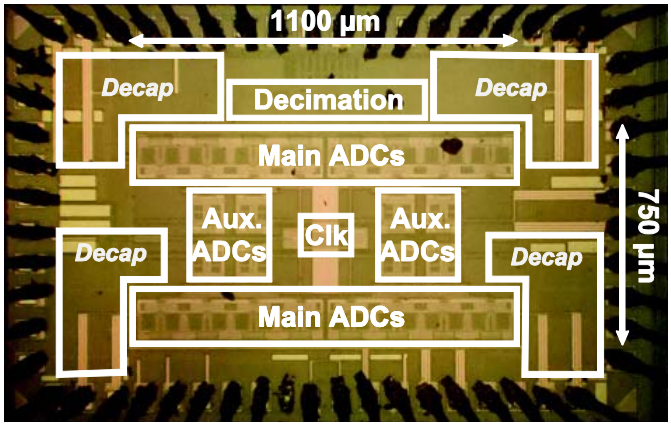

Fig. 19. Chip micrograph.

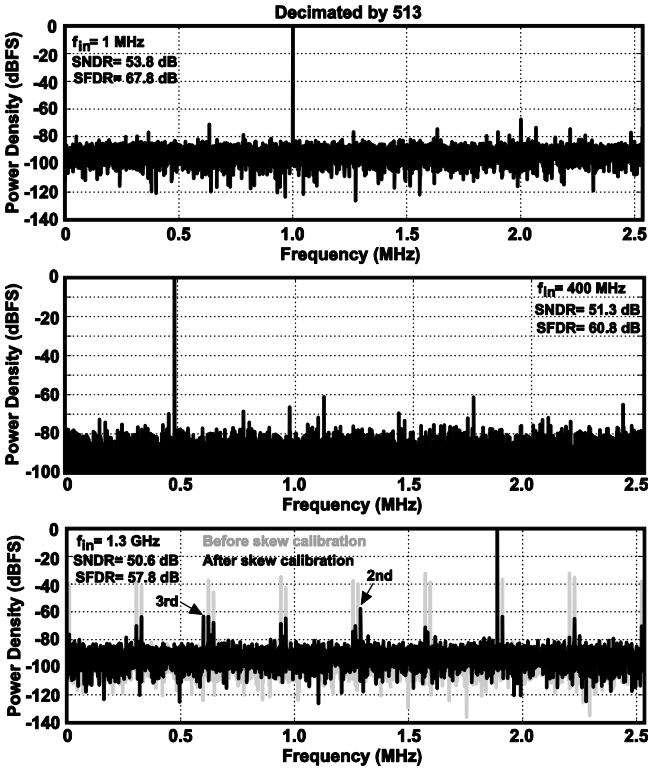

Fig. 20. Measured output spectrums with sampling rate of 2.6 GS/s.

V. Experimental Results

A 10-bit 2.6-GS/s 16-times interleaved SAR ADC is fabricated in a 40-nm CMOS technology to verify the proposed timing-skew calibration. Fig. 19 shows the micrograph of

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART ADCS

	ISSCC 14 [3]	ISSCC 15 [4]	ISSCC 14 [7]	ISSCC15[13]	JSSC 13 [6]	This Work	
Technology	65 nm	45 nm	40 nm	45 nm	65 nm	40 nm	
Resolution [bit]	10	10	9	10	11	10	
Supply [V]	1.0	1.1	1.1	1.2	1.2	1.1	
Speed [GS/s]	1.0	1.6	1.62	1.7	2.8	2.6	
Mismatch tones[dBFS]	60	N/A	70	N/A	60	63.2	
Skew Estimation	Digital	Analog	Digital	—	A&D	A&D	
Skew Correction	Analog	Analog	Digital	—	Analog	Digital	
SNDR@Peak[dBFS]	53.3	57.2	50.0	55.3	50.9	54.2	
SNDR@Nyquist[dBFS]	51.4	56.1	48.0	51.2	50.0	50.6	
Power [mW]	18.9	17.3	93 (1)	15.4	44.6	18.4	39.2(2)
FoM@ Low f_{in}[fJ/c.-s.]	50.0	21.0	222.2 (1)	19.0	56	16.8	35.8(2)
FoM@ Nyq. [fJ/c.-s.]	62.3	21.0	279.7 (1)	30.4	78	25.6	54.5(2)
Area [mm^2]	0.78	0.364	0.83 (1)	0.057	0.63	0.825	0.92(2)

(1) With references and input buffer
(2) With estimated calibration power and area

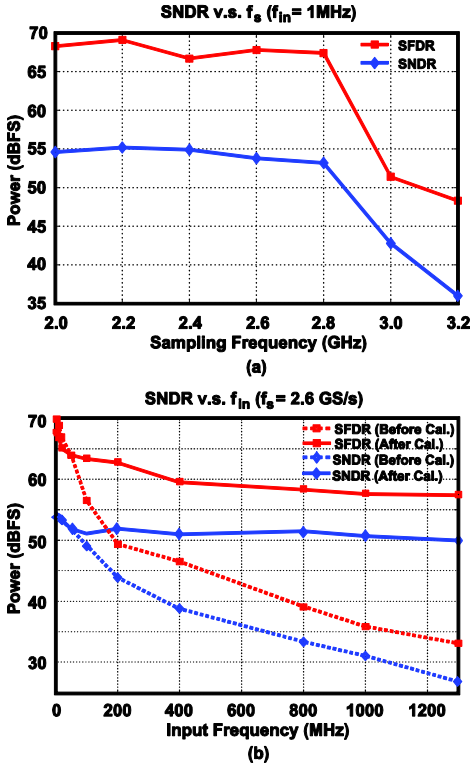

Fig. 21. Measured dynamic performance versus (a) sampling rate and (b) input frequency.

the chip. The active area is 1100 μm $\times$ 750 μm, excluding the decimation circuit, output buffers, and the reference decoupling capacitors. The output digital codes are decimated by 513 and captured by a logic analyzer. The ADC was measured with on-chip reference decoupling capacitors and the total capacitance is about 500 pF for all the 16 main ADCs and eight delta-sampling ADCs as well as a 1-V external reference voltage while running from a 1.1-V power supply. The power consumption of the core circuit is 18.4 mW, excluding the reference generation. The gate assumption for the digital calibration is about 130 K which results in estimated power consumption of 20.8 mW and area of 0.1 mm^2 in a 40-nm CMOS technology. Except for the skew calibration, the total estimated power includes the gain and offset calibration which also contributes considerable consumption. The dominant parts are the gain and skew correction logics which contain multipliers running at 162.5 MHz. Fig. 20 shows the measured output spectrums when the ADC is operating at 2.6 GS/s. The measured result gives an SNDR of 53.8 dB and an spurious-free dynamic range (SFDR) of 67.8 dB achieved with a 1-MHz input signal. With a Nyquist-rate input, the performance is dominated by timing-skew error before skew calibration as shown in the gray line. After skew calibration, the SNDR is 50.6 dB and SFDR is 57.8 dB which is mainly contributed by the 2nd order harmonic. All the interleaving tones are below -63.2 dB. The spectrum at the mid-band input frequency of 400 MHz is also shown to include the high-frequency spurs and harmonics in band. The residual interleaving tones come from the larger-than-expected summation of the intrinsic and the added skew. Fig. 21(a) shows the dynamic performance versus sampling rate with a 1-MHz input signal. The SNDR decreases rapidly as the sampling rate increases above 2.8 GS/s. Fig. 21(b) shows the

dynamic performance versus input frequencies before and after calibration. The effective bandwidth is about 1 GHz with a 3-dB SNDR drop. The total power consumption with digital calibration logic included (implemented in software during testing) is 39.2 mW. The proposed time-interleaved SAR ADC with timing-skew calibration achieves a Walden figure of merit (FoM) of 54.5 fJ/conversion step and a Schreier FoM of 154.6 dB under a 1-GHz effective resolution bandwidth. Table I shows the performance summary of this ADC and the comparison with the other state-of-the-art high-speed ADCs. This paper employs mixed-signal skew estimation and digital correction to minimize the convergence time.

VI. Conclusion

A 10-bit 2.6-GS/s 16-time interleaved SAR ADC with timing-skew calibration is presented in this paper. This ADC employs mixed-signal error estimation and digital error correction techniques to perform an efficient interleaving skew calibration. A delta-sampling SAR ADC is also presented to serve as auxiliary ADC for signal difference extraction, reducing the power and area consumption. The proposed architecture, fabricated in 40-nm general purpose CMOS technology, consumes 39.2 mW estimated power while operating at 2.6 GS/s, and achieves Walden FoMs of 35.8 and 54.5 fJ/conversion step at 1-MHz input and Nyquist rate.

Acknowledgment

The authors would like to thank the TSMC University Shuttle Program for chip fabrication.

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