A 0.18-V 382-μW Bluetooth Low-Energy Receiver Front-End With 1.33-nW Sleep Power for Energy-Harvesting Applications in 28-nm CMOS

Haidong Yi, *Student Member, IEEE*, Wei-Han Yu, *Student Member, IEEE*, Pui-In Mak, *Senior Member, IEEE*, Jun Yin, *Member, IEEE*, and Rui P. Martins, *Fellow, IEEE*

***Abstract*— This paper describes an ultra-low-voltage Bluetooth low-energy (BLE) receiver (RX) front end with an on-chip micropower manager (μPM) to customize the internal voltage domains. It aims at direct powering by the sub-0.5-V energy-harvesting sources like the on-body thermoelectric, eliminating the loss and cost of the interim dc–dc converters. Specifically, the RX incorporates: 1) a two-stage power-gating low-noise amplifier with fully on-chip input-impedance matching and passive gain boosting reducing both the active and sleep power; 2) a class-D voltage-controlled oscillator (VCO) in parallel with a class-C starter to secure a fast startup; and 3) a μPM using ring-VCO-locked charge pumps and bandgap references to withstand the supply-voltage variation (0.18–0.3 V). Fabricated in 28-nm CMOS, the RX operates down to a 0.18-V supply, while exhibiting 11.3-dB NF and −12.5-dBm out-of-band IIP3. The VCO shows < −113 dBc/Hz phase noise at 2.5-MHz offset. The active and sleep power are 382 μW and 1.33 nW, respectively.**

***Index Terms*— Bandgap reference (BGR), Bluetooth low energy (BLE), charge pump (CP), class-D voltage-controlled oscillator (VCO), CMOS, energy harvesting, low-noise amplifier (LNA), micropower manager (μPM), power-gating, receiver (RX), ultra-low power (ULP), ultra-low voltage (ULV).**

I. Introduction

FOR true mobility of Internet-of-Things (IoT) products, the relaxed specifications of Bluetooth low energy (BLE) [1] are in favor of direct powering by ambient energies, freeing the cost of routine battery replacement. Energy sources like the on-body thermoelectric [2] are promising, providing a power-generation density of ∼50 μW/cm^2, and a relatively stable output power comparing to other types of energy harvesters such as vibration. The key challenge hindering its utility is the deeply low and inconstant output voltage (50–300 mV) [3]. The energy harvester is typically followed by one or more dc–dc converter(s) for maximum power extraction and regulation as depicted in Fig. 1(a) [3]. Yet, the conversion efficiency (η) of most dc–dc converters is limited to 40%–75% [4], while entailing external bulky inductors and capacitors. Another issue is related to the voltage-boosting factor that has to sacrifice the output current, as shown in Fig. 1(a), where $I_{\mathrm{SOURCE}} = I_{\mathrm{LOAD}} \times$ voltage-boosting factor $\times 1/\eta$. If the voltage-boosting factor is 5 (0.2 V → 1 V) and $\eta = 75\%$ for the dc–dc converter, only 15% of I_{SOURCE} finally goes as I_{LOAD}.

Current-reuse receivers (RXs) are getting popular for ultra-low-power (ULP) radios. Transistor stacking in sub-1-V CMOS technologies, regrettably, reduces both the voltage headroom and block-to-block isolation. In [5], merging the voltage-controlled oscillator (VCO) with the low-noise amplifier (LNA) and mixers allows significant power savings, but the VCO may be pulled by the RF blockers, and the noises of the RX path and LO path (VCO) will cross-affect each other. Although the VCO pulling and noise crosstalk can be prevented by separately powering the current-reuse RX path and LO path [6], the cost and power loss of the extra dc-dc converter are unneglectable.

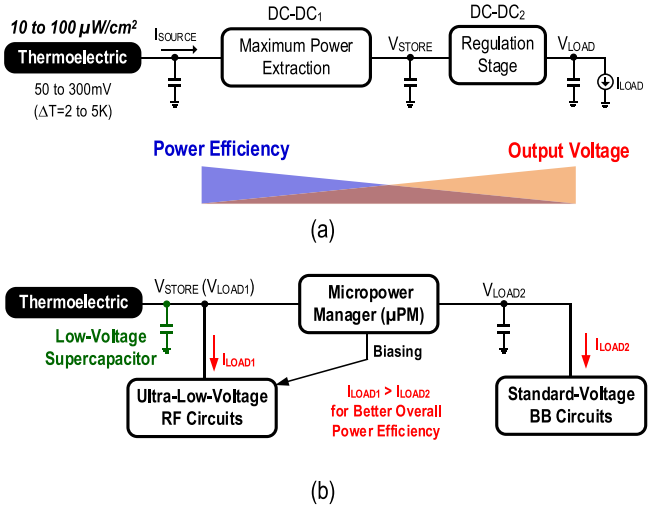

Fig. 1. (a) Conventional energy-harvesting topology. (b) Codesign between our proposed energy-harvesting topology and ULV RF circuits, where a μPM can provide the critical biases and support the standard voltage BB circuits.

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H. Yi, W.-H. Yu, P.-I. Mak, and J. Yin are with the State-Key Laboratory of Analog and Mixed-Signal VLSI and the Faculty of Science and Technology, Department of Electrical and Computer Engineering, University of Macau, Macau 999078, China (e-mail: pimak@umac.mo).

R. P. Martins is with the State-Key Laboratory of Analog and Mixed-Signal VLSI and the Faculty of Science and Technology, Department of Electrical and Computer Engineering, University of Macau, Macau 999078, China, on leave from the Instituto Superior Técnico/Universidade de Lisboa, 1049-001 Lisbon, Portugal (e-mail: rmartins@umac.mo).

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Alternatively, the sub-0.5-V energy-harvesting sources favor the use of an ultra-low-voltage (ULV) supply to build an ULP radio. In [7], the supply voltage (V_{DD}) is minimized to 0.3 V by extensively applying inductor-based RF circuits to maximize the voltage headroom, and forward-body-biasing to reduce the transistor's threshold voltage (V_{TH}) while raising their instrinic f_T. Yet, the tradeoff is a substantial increase of the transistor's leakage current (e.g., Fig. 2(b) [7]), that is unbearable for low-duty-cycle IoT applications [8] since the BLE RX stays mostly (∼99%) in the sleep mode.

The presented RX [9] innovates an on-chip micropower manager (μPM) to enable ULV and ULP operations [Fig. 1(b)]. The RF circuits (LNA and VCO) are ULV-enabled to directly draw dc current (I_{LOAD1}) from the energy-harvesting source (V_{LOAD1}), avoiding any interim power converters. V_{LOAD1} can be stabilized by a thin-film low-voltage supercapacitor [10], which also serves as the energy reservoir. Its capacitance is subject to the required duty-cycle ratio. Only the ULP baseband (BB) circuits entail a higher standard voltage (V_{LOAD2}) that can be customized via the μPM-RX codesign. Keeping I_{LOAD2} in the level of hundreds of μA benefits the design of the μPM, as it can be built by fully on-chip switched-capacitor charge pumps (CPs) for voltage boosting (i.e., no external bulky inductors or capacitors). Also, since most RF performances such as noise figure (NF), small-signal gain, and input-impedance matching are related to the supply current rather than the supply voltage, ULP Bandgap references (BGRs) can be incorporated in the μPM to bias the RF circuits against process-voltage-temperature (PVT) variations. The tolerability of RF blockers can be addressed via properly designing the LNA with gain control according the sensitivity target. Other key features of the μPM are capable of self-startup down to 0.15 V, and regulated output voltages against supply-voltage variation to reduce the excessive power.

This paper is organized as follows. Section II overviews the RX system architecture. The μPM is detailed in Section III, followed by the designs of the VCO and RX-path building blocks in Sections IV and V, respectively. Section VI summarizes and discusses the measurement results, and finally the conclusions are drawn in Section VII.

II. System Overview

The presented ULV RX front-end (Fig. 2) is headed by a single-ended LNA with on-chip input-impedance matching. It is followed by a passive *RC–CR* network for I/Q generation (V_{rfI}, V_{rfQ}), and four passive mixers for frequency down-conversion and single-to-differential conversion. The local oscillator (LO) signals are the differential outputs ($V_{osc\pm}$) of a switching-type Class-D VCO [11] that features output-swing enhancement to improve the mixer's NF and conversion gain, while preventing the need of power-hungry LO buffers. The obtained four-phase BB signals (I/Q and differential) are then amplified by four BB transimpedance amplifiers (TIAs), and finally buffered off-chip for 50-Ω measurements ($V_{out,I\pm}$, $V_{out,Q\pm}$). The noncascode inductor-based LNA and VCO are ULV-enabled to operate against an uncertain energy-harvesting voltage ($V_{DD,EH} \approx$ 0.15–0.30 V). The critical biases of the

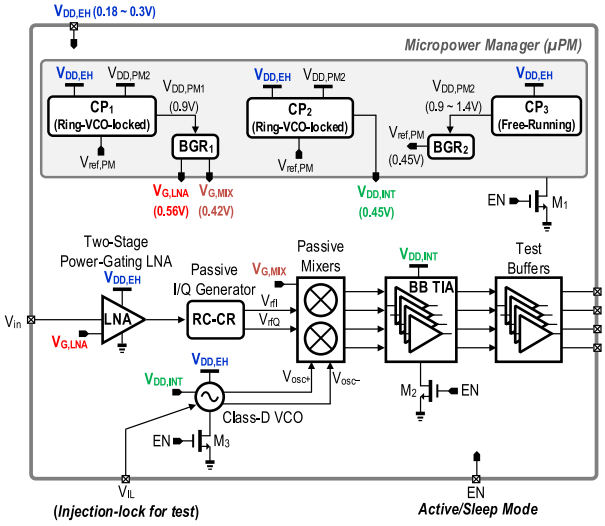

Fig. 2. System overview of the proposed ULV RX front end with an on-chip μPM to customize the internal supply and biases. The power-hungry LNA and VCO are ULV design to directly draw current from $V_{DD,EH}$. V_{IL} is for injection locking the VCO during the RX measurements as there is no PLL.

LNA ($V_{G,LNA}$) and mixers ($V_{G,MIX}$), as well as the internal supply ($V_{DD,INT}$) of the BB TIAs, are generated by the μPM. Inside the μPM, there are three CPs ($CP_{1,2,3}$) and two BGRs that will be detailed in Section III. CP_1 is designed to offer a ∼0.9-V supply, with a small current budget, for BGR_1 that generates $V_{G,LNA}$ and $V_{G,MIX}$, securing the robustness of the LNA and mixers against PVT variations. BGR_1 inherently rejects the output ripple of CP_1. For CP_2, it is designed to generate a ∼450-mV $V_{DD,INT}$, with a relatively higher current budget (∼100 μA), to power up the four BB TIAs, and bias the Class-C starter of the VCO to be detailed in Section IV. CP_2 features a set of interleaved clocks for output-ripple reduction, minimizing such ripple noise from corrupting the BB TIAs. CP_3 is a free-running design to secure a fast self-startup. It activates BGR_2 to generate an essential reference voltage ($V_{ref,PM}$) for the feedback control of $CP_{1,2}$; both feature a ring-VCO-locked loop to regulate their outputs ($V_{DD,PM1}$ and $V_{DD,INT}$) against $V_{DD,EH}$ variation.

In the sleep mode, high-V_{TH} (HVT) power-gating NMOS transistors (M_{1-3}) are incorporated for sleep-current suppression of the μPM, BB TIAs, and VCO. The LNA features a self-shutdown mechanism to avoid NF and linearity penalties due to the extra power-gating switches, to be detailed in Section V.

III. Micropower Manager (μPM)

The μPM aims to withstand a $V_{DD,EH}$ range from 0.15 to 0.3 V. The total power budget is ∼100 μW, and the design details of CP_{1-3} are presented next.

A. CP_{1-3} Driven by Bootstrapped Ring-VCO (BTRO)

The aimed $V_{DD,EH}$ is as low as 0.15 V, while the standard analog blocks like the BGRs should operate at a voltage of ∼0.9 V. Thus, CP_1 is designed with a 10× conversion

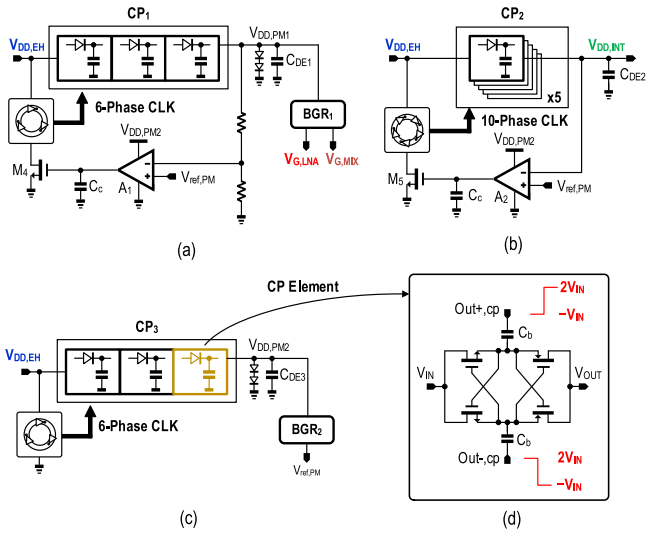

Fig. 3. (a) Ring-VCO-locked CP1. (b) Ring-VCO-locked CP2. (c) Free-running CP3 for self-startup. (d) Schematic of each CP element. The sketched swing of Out±,cp is in the ideal case.

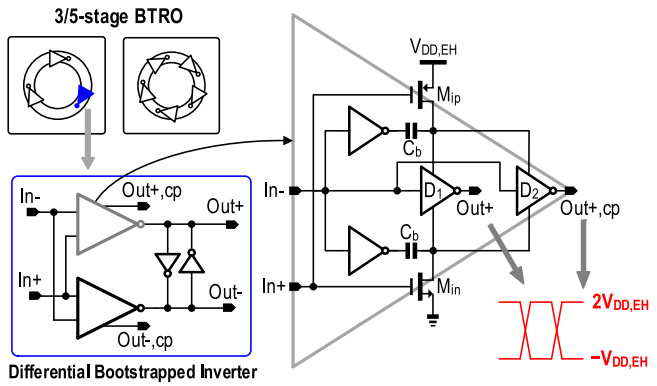

Fig. 4. 3/5-stage BTRO. The ideal output swing is 3 $\times V_{DD,EH}$. Out± is for driving the next inverter using D1, and Out±,cp is for driving the CP elements using D2.

ratio using three sub-cells in series [Fig. 3(a)]. The six-phase clocks are generated by a three-stage differential bootstrapped ring-VCO (BTRO). Ideally, CP_1 delivers $V_{DD,PM1} = V_{DD,EH}+3V_{DD,EH}+3V_{DD,EH}+3V_{DD,EH} = 10V_{DD,EH}$, that is 1.5 V at $V_{DD,EH} = 0.15$ V. $V_{DD,PM1}$ from CP_1 powers up BGR_1 that offers the gate biases of the LNA ($V_{G,LNA}$) and mixers ($V_{G,MIX}$).

Since the BB TIAs require a minimum 0.45-V $V_{DD,INT}$ with a 100-μA current budget, CP_2 is designed with a 4× conversion ratio: $V_{DD,INT} = V_{DD,EH}+3V_{DD,EH} = 4V_{DD,EH}$. There are five sub-cells in parallel to enhance the output current, as shown in Fig. 3(b). The 10-phase clocks are the intrinsic outputs of a five-stage differential BTRO without extra buffering. $V_{DD,PM2}$ from CP_3 [Fig. 3(c)] powers up both BGR_2 to generate $V_{ref,PM}$, and the error amplifiers ($A_{1,2}$) used for the feedback control, as shown in Fig. 3(a) and (b). CP_3 utilizes a free-running ring-VCO for self-startup. The cascode diodes at $V_{DD,PM1}$ and $V_{DD,PM2}$ are used to limit the maximum voltage below 1.4 V for overvoltage protection, and the BGRs use the 1.8-V-thick-oxide transistors to ensure the device reliability for the input supply range. The smoothing capacitors (C_{DE1-3}) aid output-ripple reduction.

The CP elements of CP_{1-3} are the same as that shown in Fig. 3(d), using a cross-coupled structure to boost the input voltage ($V_{DD,EH}$) targeting a value as low as 0.15 V, with the device size computationally optimized for a maximum power conversion efficiency (PCE). The three- and five-stage differential BTROs are detailed in Fig. 4. The single-ended BTRO has been reported in [12], whereas the employed BTRO is based on differential bootstrapped inverters [13] that can ideally offer a clock swing up to 3 × $V_{DD,EH}$ to drive up the CP elements. In practice, due to the conduction loss of the transistors and voltage drop on the boosting capacitors (C_b) caused by the loading current, the clock swing is only ~2.3 × $V_{DD,EH} = 0.35$ V_{pp}(simulation) in the employed 28-nm CMOS process, but is still adequate to operate the CP elements in the range of tens of MHz (~20 MHz at 0.15-V $V_{DD,EH}$). Also, unlike the single-ended BTRO counterpart, M_{ip} and M_{in} here can be driven more synchronically by In+, instead of Out+, to reduce the power loss due to reverse current. The BTRO's outputs can also be separately out via the inverters D_1 and D_2, to reduce the dependence of the oscillation frequency on the load drivability. The BTRO is designed with low-threshold-voltage ($V_{TH} \approx 260$ mV) transistors. During the startup, the inverters inside each BTRO work in the sub-threshold region, but could ensure a loop gain of ~12 dB at 0° phase shift to ensure oscillation. The signal swing, when entering the steady state, will be boosted to 3 × $V_{DD,EH}$(−$V_{DD,EH}$ to 2 $V_{DD,EH}$), and the transistors will be driven into the triode region with the boosted swing to reduce the conduction loss.

The optimization of CP_{1-3} is based on simple resistive loads (R_L) in simulation. $CP_{1,2,3}$ are optimized at $V_{DD,EH} = 0.15$ V.CP_1 has the same circuit parameters as CP_3 excluding the feedback loop. R_L of CP_1 is 500 kΩ to model the power consumption of BGR_1 and resistors in the voltage divider. R_L of CP_2 is 4.5 kΩ to model the power consumption of the BB TIAs (~45 μW). With a 2.5-pF MOM capacitor C_b, a 41% PCE is obtained for $CP_{1,3}$, and $V_{DD,PM1,2}$ is 1.11 V. For CP_2, $C_b = 15$ pF and $V_{DD,INT} = 0.48$ V lead to a 49% PCE, with the power consumption of the feedback circuits of $CP_{1,2}$ excluded from the PCE calculation. Although the PCE of $CP_{1,3}$ is lower than that of CP_2, the power consumption of $CP_{1,3}$ is only ~5.93 μW, that is much smaller than that of CP_2(~96 μW). Hence, the PCE of the whole μPM is dominated by CP_2.

B. Ring-VCO-Locked Loop for Voltage Regulation

To tolerate an uncertain $V_{DD,EH}$, $CP_{1,2}$ are rounded by a ring-VCO-locked loop to regulate $V_{DD,PM1}$ and $V_{DD,INT}$, and reduce the excessive power when $V_{DD,EH}$ goes unnecessarily high. Especially for the BB TIAs (inverter-like amplifiers), their dc currents will raise nonlinearly with $V_{DD,INT}$. To surmount it, A_1 (A_2) are added to sense $V_{DD,PM1}$ ($V_{DD,INT}$) and return the control signal via the current source M_4 (M_5) for voltage regulation, as shown in Fig. 3(a) and (b). From PVT simulations, the feedback loop continues functioning when

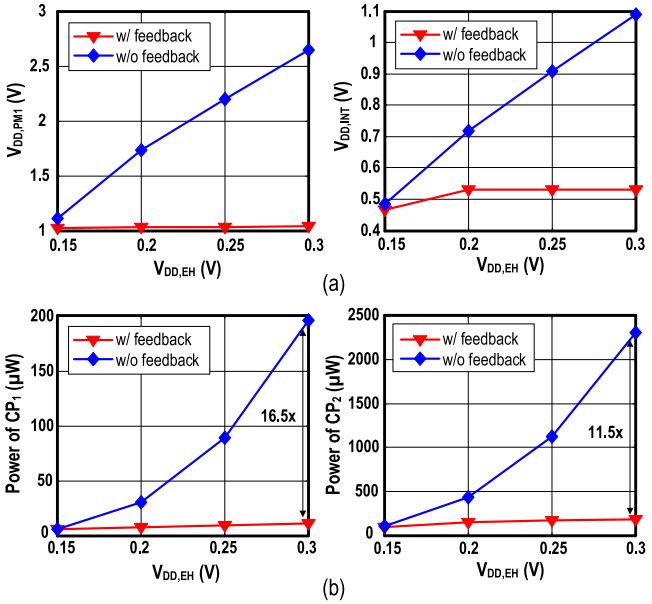

Fig. 5. Performances of CP1 (left) and CP2 (right) versus $V_{DD,EH}$ with and without feedback control. (a) Output voltage. (b) Power consumption.

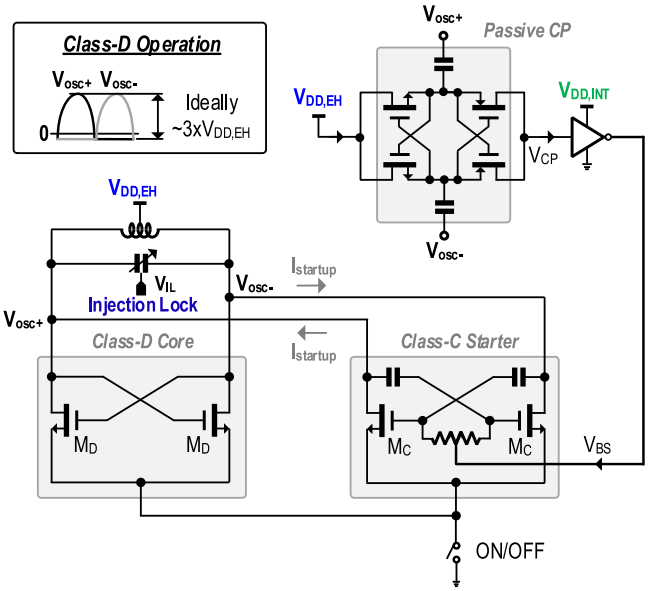

Fig. 6. ULV class-D VCO with a class-C starter to assist a fast startup. The passive CP senses the swing buildup at $V_{osc\pm}$ to activate/deactivate the class-C starter before/after startup. The steady-state oscillation is governed by the class-D VCO.

$V_{DD,EH}$ is down to 0.15 V. Considering the tradeoff between the stability and settling time of the two feedback loops, the compensation capacitors C_c in Fig. 3(a) and (b) are set at 3 pF. $A_{1,2}$ have a simulated open loop gain of 35 dB, while consuming 0.27 μW.

The simulated output voltage and power consumption of $CP_{1,\ 2}$ versus $V_{DD,EH}$ with and without the feedback control are compared in Fig. 5(a) and (b), respectively. The variation of output voltage against $V_{DD,EH}$ is $\Delta V_{DD,PM1}(\Delta V_{DD,INT})/\Delta V_{DD,EH}$. With the feedback control, $V_{DD,PM1}$ is clipped to ~1.03 V for $V_{DD,EH}$ = 0.15–0.3 V, corresponding to a sensitivity of 0.11 V/V. $V_{DD,INT}$ is bounded to ~0.53 V, but with a higher sensitivity of 0.45 V/V (due to the low output voltage at 0.15 V). Both results are considerable improved when comparing with no feedback, i.e., 10.2 V/V for $V_{DD,PM1}$ and 4.06 V/V for $V_{DD,INT}$. Similarly, with feedback control, the power consumption of CP_1 (CP_2) only mildly increases from 5.93 to 11.2 μW (96–184 μW) with the rising of $V_{DD,EH}$. Otherwise, it will jump to 196 μW for CP_1 and 2.3 mW for CP_2. From Fig. 5(b), we can derive that the total power consumption of CP_1 and CP_2 is controlled to be 195 μW at $V_{DD,EH}$ = 0.3 V, saving the excessive power by ~11.8× against no feedback.

C. Output-Ripple Reduction of CP_1 and CP_2

With C_{DE1} = 6 pF for CP_1, the simulated maximum output ripple of $V_{DD,PM1}$ versus $V_{DD,EH}$ is reduced to 3.44 mV when $V_{DD,EH}$ increases. The ripple frequency is 2× of the BTRO's frequency (~40 MHz) at $V_{DD,EH}$ = 0.15 V. The simulated supply rejection of the $BGR_{1,2}$ is 35 dB at dc, and 9.5 dB at 40 MHz. Thus, the maximum ripple of $V_{G,LNA}$ and $V_{G,MIX}$ can be reduced to 1.13 mV.

In order to reduce the ripple of $V_{DD,INT}$ while not using a large C_{DE2}, CP_2 can benefit from interleaved clocks. With 10-phase clocks equally distributed to the five sub-cells of CP_2, the output ripple is ideally reduced by 5× against two-phase clocks [14]–[16]. Thus, the interleaved clocks benefit the die area. The simulated maximum ripple of $V_{DD,INT}$ is <0.77 mV_{pp} at an affordable C_{DE2} of 18.9 pF, which contributes to the overall NF degradation by <1 dB at the RX's differential BB outputs.

IV. ULV Class-D VCO With a Class-C Starter

To maximize the power efficiency it is preferable that the VCO works directly at $V_{DD,EH}$. Since the outputs of the VCO will directly drive the mixers without any additional buffers, a large VCO output swing is favored to improve the RX NF and conversion gain. Here, a switching-type class-D topology (Fig. 6) is chosen since it ideally can generate an output swing close to ~3 ×$V_{DD,EH}$ by enlarging the cross-coupled transistors, and removing the current-biased circuitry of the conventional class-B VCO, which renders it suitable for ULV operation [11]. On the other hand, the oscillation frequency of the class-D VCO is sensitive to the supply pushing at an ULV $V_{DD,EH}$. Since the speed of supply variation caused by the enviroment change is quite slow when powered by an energy-harvesting source, a phase-locked loop (PLL) with a typical loop bandwidth of several hundreds of kHz should be fast enough to stabilize the VCO frequency when receiving the data.

Yet, the cross-coupled transistors may not offer adequate negative transconductance at ULV $V_{DD,EH}$ in the presence of PVT variations, which would cause the VCO to fail to startup. Even using a large-size (400 μm/28 nm) low-V_T device for M_D, the simulated small-signal g_m is below the startup criteria when T < −10 °C at slow corner and $V_{DD,EH}$ = 0.18 V [Fig. 7(a)]. To surmount this issue, a class-C starter (Fig. 6)

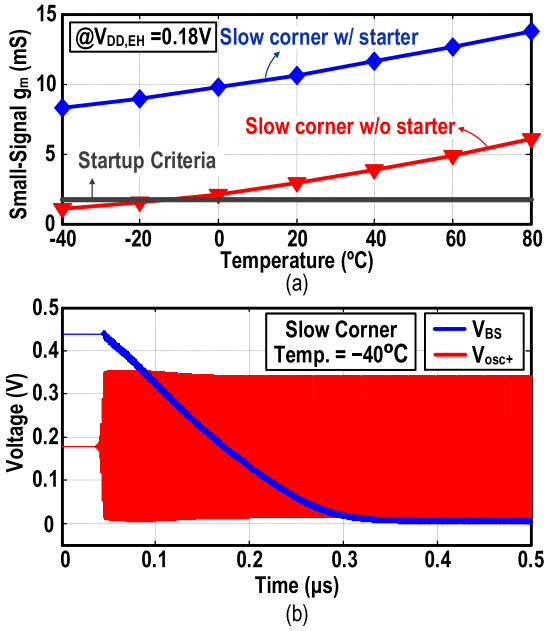

Fig. 7. Simulated (a) small-signal gm of MD versus temperature at the slow corner and (b) voltage waveforms during startup under the slow corner and temperature of -40 ° C. ($V_{DD,EH} = 0.18$ V).

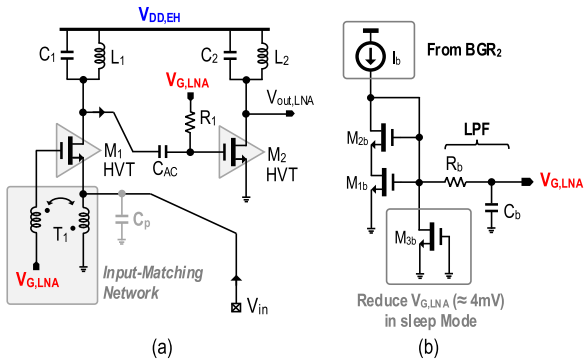

Fig. 8. (a) ULV two-stage power-gating LNA with on-chip input-impedance matching. (b) Its self-shutdown bias circuit in the sleep mode.

is added in parallel with the class-D core. A dynamic bias voltage V_{BS} ensures a robust startup. V_{BS} is generated by inverting V_{CP} which is the output of a passive CP continuously sensing the VCO outputs: $V_{osc\pm}$. When the VCO is starting up, $V_{CP} \approx 0$ V, and V_{BS} is pulled to $V_{DD,INT}$ provided by CP_2. During the startup, the class-C starter is biased at a voltage of ~0.45 V higher than the V_{TH} of M_D. Thus, it can deliver a large negative transconductance in presence of PVT variations using M_C with a smaller transistor size: $(W/L)_{M_C} = (W/L)_{M_D}/25$. When oscillation has been built up, the large-signal transconductance of the class-D core is sufficient to sustain the oscillation, so that the class-C starter can be turned off to reduce the power consumption and prevent the phase noise degradation. This is done automatically since the passive CP would charge $V_{CP}$to $V_{DD,EH} + V_{osc,pp}$, which pulls V_{BS} to ground. As shown in Fig. 7(b), at T = −40 °C and slow corner, the VCO starts up within 45 ns and the average g_m (~4.5 mS) of M_D during stable oscillation well exceeds the startup criteria. The output swing slightly decreases by 19 mV after the class-C starter is completely turned off. At T = 27 °C and typical corner, the simulated startup time VCO is 25 ns. After the class-C starter is completely turned off, the VCO power is significantly reduced by 2.3× from 330 to 145 μW while the phase noise at 2.5-MHz offset is improved by 3.3 dB. The simulated output swing is 0.35 to 0.63 V_{pp} for $V_{DD,EH} = 0.18$–0.3 V, which is lower than 3 × $V_{DD,EH}$ since the additional losses introduced by the switches become large when $V_{DD,EH}$ is lower than the threshold voltage of M_D (~0.3 V).

To achieve low-power consumption, a large inductance value is preferable. Here a three-turn inductor has been chosen to realize an inductance of 4.49 nH while still keeping a high Q of ~20. Besides, for explicit power down and sleep-current control, a tail switch is added for power gating. The control voltage of the switched-capacitor array for frequency tuning is provided by $V_{DD,INT}$ from CP_2 drawing a neglectable dc current. The injection-lock port (V_{IL}) is for RX testing, similar to [7].

V. ULV Receiver (RX) Path

The RX path mainly consists of an LNA, a passive I/Q generator, four passive mixers and four BB TIAs as detailed next.

A. ULV Two-Stage Power-Gating LNA

As shown in Fig. 8(a), the single-ended single-transistor (M_1) LNA features an on-chip transformer (T_1) for input-impedance matching and passive gain boosting between M_1's source and gate terminals [17]. Both the primary and secondary coils of T_1 have an inductance of ~5.4 nH, and a low Q factor of ~5.6. They are reversely-coupled with a coupling factor of 0.86. From simulations at $V_{DD,EH} = 0.18$ V, the dc current of the LNA's first stage can be reduced from 2.1 mA (without T_1) to 612 μA (with T_1) for a similar voltage gain and input-matching quality. ULV operation mainly challenges the large-signal linearity of the LNA. To balance the NF and linearity performances, the LNA's first stage is loaded with a low-Q LC tank (L_1C_1) to provide a just-reasonable gain of ~14 dB. The LNA's second stage is designed to drive a capacitive load of 723 fF from the I/Q generator + passive mixers, and thus it only provides a 2-dB gain with a current consumption of 510 μA. Both $M_{1,2}$ are sized with a long-channel length (180 nm), and biased with an adequate overdrive ($V_{GS} - V_{TH} \approx 110$ mV) to balance the linearity, gain and sleep current of the LNA [18]. The simulated IIP3 and NF of the overall LNA is −17.4 dBm, and 9.84 dB, respectively, before considering the noise injected by the μPM. Moreover, $M_{1,2}$ are HVT devices to suppress their sleep currents that simulate 0.55 nA in the sleep mode, against 0.23 μA in low-V_T devices. The LNA's blocker tolerability is limited at the output node of its second stage, which can be improved by introducing gain control while not affecting the input-impedance matching. It is preferred for BLE since the reference signal level is relaxed to −67 dBm under blocker performance measurement [19].

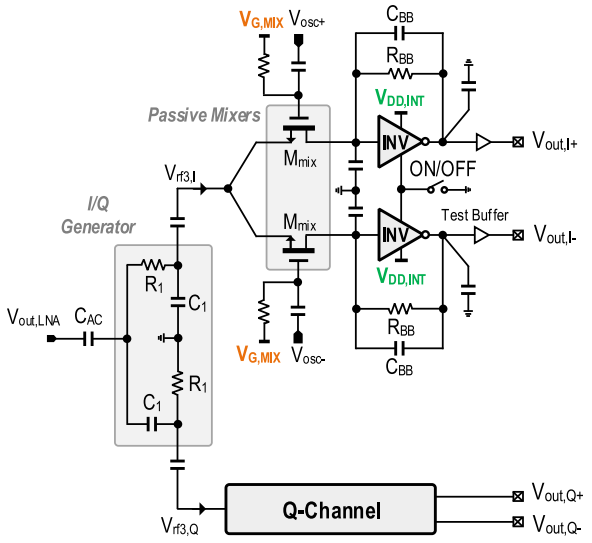

Fig. 9. RF path, passive I/Q generator, passive mixers, and BB TIAs.

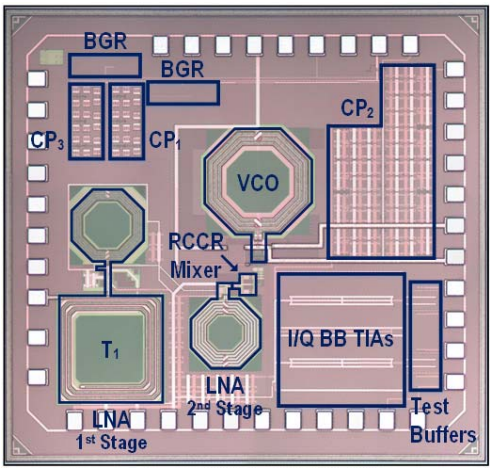

Fig. 10. Chip photograph of the ULV RX fabricated in 28-nm CMOS.

The current reference (I_b) of the bias circuit is shown in Fig. 8(b). The current mirror has a supply voltage ($V_{DD,PM1}$) of ~0.9 V generated by CP_1, thus it can provide a ~580-mV bias voltage ($V_{G,LNA}$) for the HVT devices, while ensuring an adequate overdrive voltage. A low-pass filter, R_b (1 MΩ) and C_b (40 pF), is added to prevent the μPM from injecting noise into the LNA. $M_{1b,2b}$ are series connected to reduce the required I_b to 700 nA. To assess the robustness, we carried out 100-run Monte Carlo simulations on process variations. The dc current of the LNA varies <3%.

The bias circuit of the LNA has a self-shutdown mechanism. A 160/60 nm device, M_{3b}, is added with its gate tied to the ground as a ~60-MΩ MOS resistor. The resistance of M_{3b} is large compared to the diode-connected M_{1b} and M_{2b} at a high voltage, thus not affecting the generated $V_{G,LNA}$ in the active mode. In the sleep mode, when the μPM is switched off, the impedance of the diode-connected M_{1b-2b} and BGR is large, thus the impedance of M_{3b} becomes relatively low pulling $V_{G,LNA}$ to ground. From simulations, $V_{G,LNA}$ is reduced from 160.6 to 3.3 mV via M_{3b}, reducing the leakage current from 9.13 to 0.55 nA at $V_{DD,EH} = 0.18$ V.

B. Passive I/Q Generator, Passive Mixers, and BB TIAs

The I/Q generator is an *RC–CR* network and the mixers are NMOS switches (Fig. 9). The I/Q generator realized in the RF path maximizes the LO swing at M_{mix} given by the VCO ($V_{osc\pm} \approx 0.35 V_{pp}$). With $R_1 = 256\ \Omega$ and $C_1 = 260$ fF, the simulated insertion loss is < 7 dB. R_1 is implemented as two parallel-connected resistors to enhance the I/Q accuracy against process mismatches. We carried 100-run Monte Carlo simulations on process variations, showing a worst image-rejection ratio (IRR) of 25 dB, which is adequate for either zero-IF or low-IF reception for the BLE standard.

The passive mixers are biased at 450 mV via BGR_2 balancing the RX NF and conversion gain. The four passive mixers convert the I/Q RF signals into four BB I/Q differential signals for the BB TIAs.

Each BB TIA is an inverter-like amplifier with *RC* feedback (R: 23 kΩ; C: 1.37 pF), consuming a simulated current of 25 μA at a 0.46-V $V_{DD,INT}$. The TIA's transistors are relatively large (NMOS: 375/10 μm and PMOS: 1020/10 μm) to suppress their flicker noise for 0.5 MHz-IF downconversion. The TIA exhibits a simulated gain of 22.6 dB and bandwidth of 0.5 MHz. It shows a 22.5-dB rejection at 5-MHz offset for channel selection. The simulated input 1-dB gain compression of the TIA at 2-MHz offset is −7.8 dBm. Two capacitors have been added at the input (4 pF) and output (20 pF) of the TIA to add two more real poles. They effectively suppress the 2×LO feedthrough component while aiding partially the channel selection. The common-mode noise injected by CP_2 is further suppressed at the BB TIA's differential outputs. To meet the BLE channel-selection specification, sub-0.5-mW BB filters similar to [5] or [22] should be added; the supply voltage can be provided by a CP similar to the architecture as shown in Fig. 3. With it, a low-power low-dynamic-range ADC is also expected for digitization.

VI. Measurement Results

The ULV RX prototyped in 28-nm CMOS (Fig. 10) occupies an active area of 1.65 mm^2. The strict density rules are fulfilled. The measurements were conducted in a three-step approach: from the stand-alone μPM and VCO to the complete RX. The latter is aided by an external signal source to injection-lock the VCO, similar to [7], as there is no PLL in this prototype. We measured the startup characteristic of the μPM with the Tektronix MDO3024 Oscilloscope terminated with a 10-MΩ probe. The VCO and complete RX are measured with the Keysight 9030A PXA Signal Analyzer. The I/Q differential BB outputs are converted to single-ended via off-chip transformers crucial here to reject the common-mode noises. $V_{DD,EH}$ is given by a typical power supply sweeping from 0.18 to 0.3 V to balance the overall performances.

A. Stand-Alone μPM

Fig. 11(a) plots the outputs of the μPM at $V_{DD,EH} =$ 0.18 V with an external enable signal (EN, in Fig. 2). The startup time is ~200 μs that can be overlapped with the fast startup time (~50–400 μs) of the state-of-the-art BLE crystal

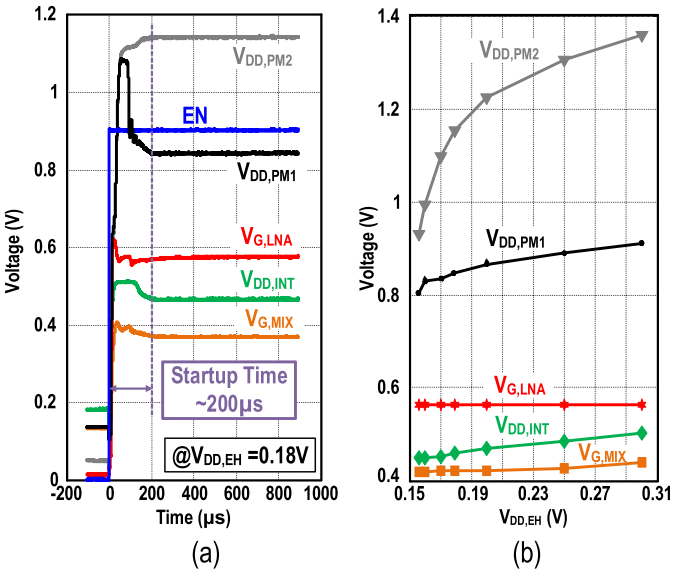

Fig. 11. Measured (a) startup transients of the μPM and (b) outputs against $V_{DD,EH}$ variation.

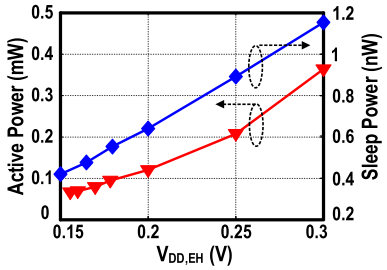

Fig. 12. Measured power consumption and sleep power of the μPM against $V_{DD,EH}$ variation.

oscillator [20], [21]. Thus, the agility of the RX in launching a connection should not be affected. The voltages ramp up rapidly in $\sim$50 μs while they take $\sim$150 μs to stabilize. Thus, the startup time is dominated by the feedback control loop in $CP_{1,2}$. Fig. 11(b) shows the voltage variation over $V_{DD,EH}$ from 0.156 to 0.3 V. The variations of $V_{G.LNA}$ and $V_{DD,INT}$ are controlled to be 0.18% and 12%, respectively, saving the excessive power. $V_{DD,PM1}$ and $V_{DD,INT}$ increase with $V_{ref,PM}$ mainly due to the increased voltage drop on the tail switch M_1 (see Fig. 2) at a high $V_{DD,EH}$.

Fig. 12 shows the power consumption and leakage power of the μPM. Comparing Fig. 12 with Fig. 5(b), the power consumption goes up along with $V_{DD,EH}$ which is mainly due to the free-running CP_3. The power of BTRO in CP_3 also raises significantly with $V_{DD,EH}$, while the leakage power is nearly proportional to $V_{DD,EH}$.

B. Stand-Alone VCO

Fig. 13(a)–(c) summarizes the phase noises of the free-running VCO at 2.3 and 2.6 GHz under different $V_{DD,EH}$. The worst phase noise is -113 dBc/Hz at 2.5-MHz offset at the 2.3 GHz [Fig. 13(c)], still fulfilling the BLE standard. The VCO output power, including the loss of the test buffer [Fig. 13(d)] increases from -19 to -13 dBm when $V_{DD,EH}$ goes up from 0.18 to 0.3 V. The frequency tuning range is

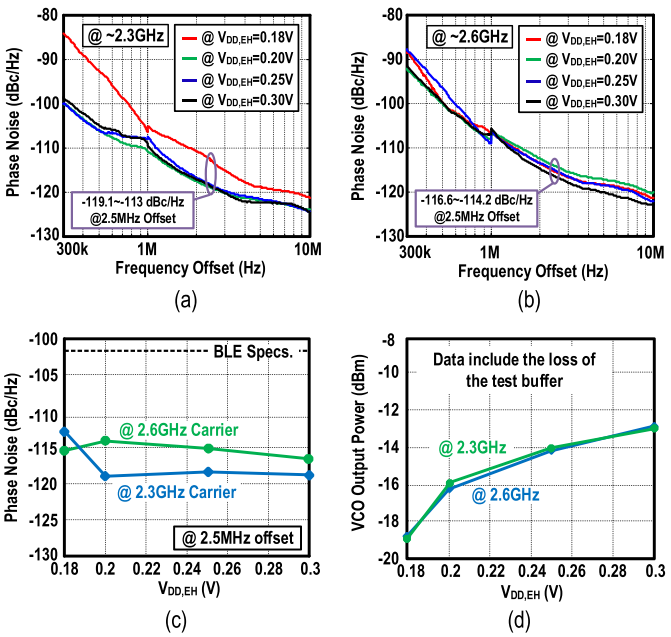

Fig. 13. Measured performances of the class-D VCO. (a) and (b) Phase noises at $\sim$2.3 GHz and $\sim$2.6 GHz. (c) Phase noise and (d) output power against $V_{DD,EH}$ variation.

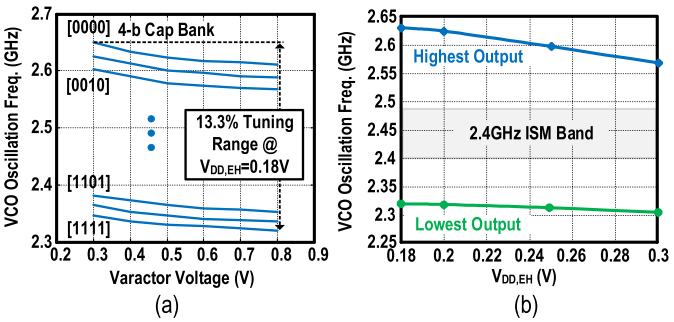

Fig. 14. Measured (a) frequency tuning range of the class-D VCO and (b) frequency pulling against $V_{DD,EH}$ variation.

13.3% [Fig. 14(a)], and Fig. 14(b) plots the supply pulling versus $V_{DD,EH}$. On the other hand, Fig. 15 exhibits the active and sleep powers versus $V_{DD,EH}$. The lowest active power is 153 μW and the leakage power is 0.45 nW, at $V_{DD,EH} = 0.18$ V.

C. Complete RX

The VCO is injection locked to an external RF source for a stable RX NF measurement [7]. It is achieved by injecting a 2$\times$LO frequency signal at the common-mode node V_{IL}. The input-impedance matching of the LNA [Fig. 16(a)] shows a 100-MHz matching bandwidth with small variation as $V_{DD,EH}$ changes. Yet, the matching bandwidth is upshifted by $\sim$50 MHz from the 2.4-GHz ISM band, which is likely due to the inaccuracy of the transformer modeling. The RF-to-BB quadrature gain is 34.5 dB at 0.18 V, and up to 41.3 dB at 0.3 V [Fig. 16(b)]. The RF-to-BB gain increases mainly due to the enlarged $V_{DD,INT}$ of the BB TIAs from CP_2, since the TIAs are self-biased.

Fig. 16(c) illustrates the double sideband (DSB) NF and out-of-band IIP3. A DSB NF of 11.3 dB is achieved at 1 MHz IF at $V_{DD,EH}$ =0.18 V. It is improved to 8.8 dB when

TABLE I
COMPARISON WITH THE STATE-OF-THE-ART ULP RXS (PLL IS NOT INCLUDED)

	This Work		JSSC'15 [5] [A. Selvakumar, et al.]	JSSC'13 [7] [F. Zhang, et al.]	JSSC'14 [6] [Z. Lin, et al.]
Applications	2.4GHz BLE		2.4GHz BLE	2.4GHz Non-Standard	2.4GHz ZigBee
Key Architecture & Circuit Techniques	**Power-Gating LNA + ULV Class-D VCO + Passive I/Q Gen. + Micro-Power Manager**		Current-Reuse Quadrature-LNA-Mixer-VCO Cell	Transformer-Coupling LNA and VCO + IF N-Path Filter	Current Reuse RF-to-BB Cell + VCO & DIV-by-4
External Matching	**Zero**		1 inductor + 1 cap.	1 inductor + 2 caps.	zero
Supply Voltage (V)	**0.18**	**0.3**	0.8	0.3	0.6 & 1.2
Active Power (μW)	**382**	**1305**	600 [1]	1600	2700 [1]
Sleep Power (nW)	**1.33**	**3.32**	N/A	N/A	N/A
NF (dB)	**11.3**	**8.8**	15.1 to 15.8	6.1	9
VCO Phase Noise (dBc/Hz) @ Offset	**-113 to -115.5 @ 2.5 MHz**	**-116.6 to -118.9 @ 2.5 MHz**	-109 @ 2.5 MHz	-112.8 @ 1 MHz	N/A
	[BLE spec: -102 @ 2.5 MHz] [2]				
Out-of-Band IIP3 (dBm)	-12.5	+4.8	-15.8 to -16.8	-21.5	-6
	[BLE Spec: -30] [2]				
IRR (dB)	26.2	25.1	30.5 to 37.3	N/A (no I/Q)	28
	[BLE Spec: 21] [2]				
Voltage Gain (dB)	34.5	41.3	55.5 to 56.1	83	55
BB Style	With I/Q		With I/Q	Without I/Q	With I/Q
BB Filtering	3 real poles [3]		2 complex poles	2 N-path filters	3 complex poles
Active Area (mm^2)	1.65		0.25	~1.7	0.26
Technology	28nm CMOS		130nm CMOS	65nm CMOS	65nm CMOS

[1] [5]-[6] have not included the loss, power and area of the power-management units if using a sub-0.5V energy-harvesting source.
[2] BLE specifications from [5]. [3] Partial channel-selection filtering.

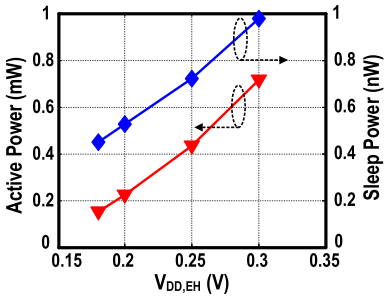

Fig. 15. Measured power consumption and sleep power of the class-D VCO against VDD,EH variation.

$V_{DD,EH} = 0.3$ V. Limited by the bandwidth of the BB TIAs, the DSB NF at 1-MHz IF is higher than that at 0.4 MHz. An IF of 0.5 MHz is expected to achieve low NF and avoid signal distortion. Without differential combining, the ripple injection from CP_2 can degrade the DSB NF by 5–6 dB at 0.1–0.8-MHz IF. With a two-tone test at 3- and 5-MHz offsets from the LO frequency, the RX shows a reasonable IIP3 of −12.5 dBm [Fig. 16(d)] even at $V_{DD,EH} = 0.18$ V, due to the adequate and stable bias voltages generated by the μPM. The measured 5-MHz in-band $P_{1\ dB}$ blocker power of the LNA is −27.5 dBm [Fig. 16(e)]. The NF against the in-band (2.5 GHz + 3 MHz) and out-of-band (1.9 GHz) blocker power is shown in Fig. 16(f). The NF is degraded to 20 dB at −26 dBm (2 dBm) for the in-band (out-of-band) blocker. The IRR of the RX is >25.1 dB.

D. Power Breakdown in the Active/Sleep Mode

Fig. 17 outlines the total active and sleep power at different $V_{DD,EH}$. The total power consumption at $V_{DD,EH} = 0.18$ V is 382 μW, where 75% of current is drawn directly from $V_{DD,EH}$ and only 25% of the current passing through the μPM. At $V_{DD,EH} = 0.3$ V, the power consumption goes up to 1.3 mW, with main contribution from the Class-D VCO since its gate bias is tied directly to $V_{DD,EH}$. At $V_{DD,EH} = 0.18$ V, the leakage power is as low as 1.33 nW, thanks to the ULV operation and the use of long-channel HVT devices for the LNA and other power-gating switches.

E. Performance Benchmark

Comparing with the state-of-the-art ULP RXs in Table I [5]–[7], this paper, aided by a μPM, succeeds in operating against a deeply low and uncertain supply voltage, while consuming low active and sleep power. No external components are entailed. These are all crucial parameters for low-cost energy-harvesting IoT applications. Note that [5]–[6] have not included the loss, power and area of their power-management units if using a sub-0.5-V energy-harvesting source. The power consumption here is optimized at 0.18 V, but is sub-optimized at 0.3 V due to the excessive VCO power. I/Q demodulation is supported for the BLE, while [7] does not. The main expense of this ULV ULP RX is the active area (1.65 mm^2), which is dominated by the utilization of three coils in the LNA and the fully integrated μPM.

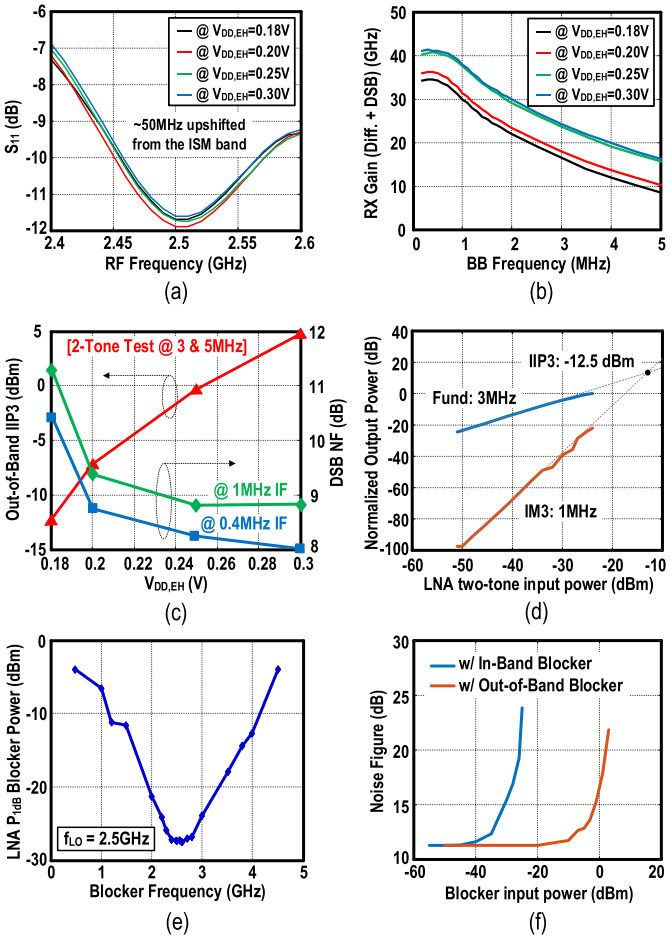

Fig. 16. Measured RX (a) $S11$, (b) RF-to-BB gain against VDD,EH, (c) NF and out-of-band IIP3 against $V_{DD,EH}$, (d) in-band IIP3 profile at $V_{DD,EH} = 0.18$ V, (e) blocker P1dB against blocker frequency, and (f) NF against blocker power at VDD,EH $= 0.18$ V.

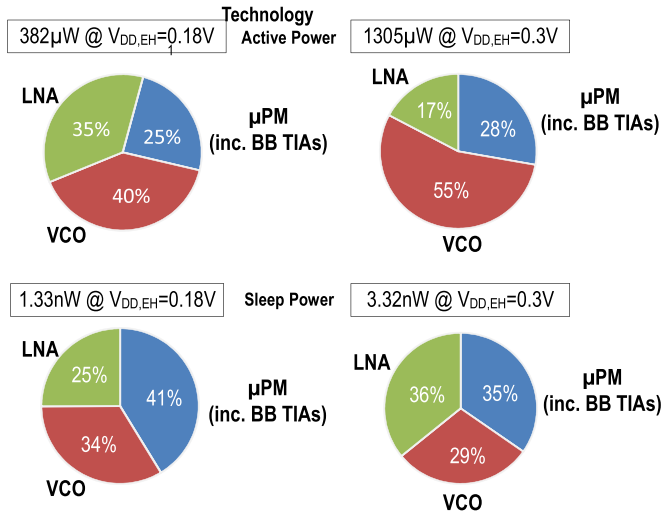

Fig. 17. Breakdown of active and sleep power at $V_{DD,EH} = 0.18$ and 0.3 V.

Note that the PLL is not included in [5]–[7] and this paper. A 0.2-V analog type-I PLL with VCO for BLE has been recently demonstrated in [23], with a total power consumption of ~0.7 mW. We also acknowledge that although this paper has managed to lower the power consumption, it has a higher NF than the recent BLE RXs [24], [25].

VII. Conclusion

An ULV RX front-end-aided by an on-chip μPM has been presented. It aims at direct powering by a sub-0.5-V energy-harvesting source without further power regulation. The circuit techniques are: 1) an μPM to deliver the internal supply voltages and biases unlimited by the energy-harvesting voltage; 2) an ULV 3-coil two-stage LNA with an on-chip input transformer to enhance the NF and gain, and power-gating to suppress the sleep power; and 3) an ULV Class-D VCO assisted by a Class-C starter to ensure robust and fast startup. Fabricated in 28-nm CMOS, the RX prototype achieves low active power (382 μW) and sleep power (1.33 nW) down to 0.18 V, while being compliant with the BLE standard.

References

[1] Bluetooth. (2013). *Bluetooth Specification Version 4.1*. [Online]. Available: http://www.bluetooth.com

[2] T. Torfs *et al.*, "Wearable autonomous wireless electro-encephalography system fully powered by human body heat," in *Proc. IEEE Sensors*, Oct. 2008, pp. 1269–1272.

[3] S. Bandyopadhyay and A. P. Chandrakasan, "Platform architecture for solar, thermal, and vibration energy combining with MPPT and single inductor," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2199–2215, Sep. 2012.

[4] J. Kim, P. K. T. Mok, and C. Kim, "A 0.15 V input energy harvesting charge pump with dynamic body biasing and adaptive dead-time for efficiency improvement," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 414–425, Feb. 2015.

[5] A. Selvakumar, M. Zargham, and A. Liscidini, "Sub-mW current reuse receiver front-end for wireless sensor network applications," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2965–2974, Dec. 2015.

[6] Z. Lin, P.-I. Mak, and R. P. Martins, "A 2.4 GHz ZigBee receiver exploiting an RF-to-BB-current-reuse Blixer + hybrid filter topology in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 6, pp. 1333–1344, Jun. 2014.

[7] F. Zhang, Y. Miyahara, and B. P. Otis, "Design of a 300-mV 2.4-GHz receiver using transformer-coupled techniques," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3190–3205, Dec. 2013.

[8] A. Paidimarri, N. Ickes, and A. P. Chandrakasan, "A +10 dBm BLE transmitter with sub-400 pW leakage for ultra-low duty cycles," *IEEE J. Solid-State Circuits*, vol. 51, no. 6, pp. 1331–1346, Jun. 2016.

[9] W.-H. Yu, H. Yi, P.-I. Mak, J. Yin, and R. P. Martins, "A 0.18 V 382 μW Bluetooth low-energy (BLE) receiver with 1.33 nW sleep power for energy-harvesting applications in 28 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 414–415.

[10] Q. Lv *et al.*, "Solid-state thin-film supercapacitors with ultrafast charge/discharge based on *N*-doped-carbon-tubes/au-nanoparticles-doped-MnO_2 nanocomposites," *ACS Nano Lett.*, vol. 16, no. 1, pp. 40–47, Nov. 2015.

[11] L. Fanori and P. Andreani, "Class-D CMOS Oscillators," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3105–3119, Dec. 2013.

[12] Y. Ho, Y.-S. Yang, C. Chang, and C. Su, "A near-threshold 480 MHz 78 μW all-digital PLL with a bootstrapped DCO," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2805–2814, Nov. 2013.

[13] H. Yi, J. Yin, P.-I. Mak, and R. P. Martins, "A 0.032-mm^2 0.15-V three-stage charge-pump scheme using a differential bootstrapped ring-VCO for energy-harvesting applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 2, pp. 146–150, Feb. 2018.

[14] H.-P. Le, S. R. Sanders, and E. Alon, "Design techniques for fully integrated switched-capacitor DC–DC converters," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 2120–2131, Sep. 2011.

[15] T. Van Breussegem and M. Steyaert, "A 82% efficiency 0.5% ripple 16-phase fully integrated capacitive voltage doubler," in *IEEE Symp. VLSI Circuits Dig.*, Jun. 2009, pp. 198–199.

[16] D. Ma and F. Luo, "Robust multiple-phase switched-capacitor DC–DC power converter with digital interleaving regulation," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 16, no. 6, pp. 611–619, Jun. 2008.

[17] X. Li, S. Shekhar, and D. J. Allstot, "G_m-boosted common-gate LNA and differential Colpitts VCO/QVCO in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2609–2619, Dec. 2005.

[18] T. Soorapanth and T. H. Lee, "RF linearity of short-channel MOSFETs," in *Proc. Int. Workshop Design Mixed-Mode Integr. Circuits Appl.*, Jul. 1997, pp. 81–84.
[19] J. Prummel *et al.*, "A 10 mW Bluetooth low-energy transceiver with on-chip matching," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3077–3088, Dec. 2015.
[20] D. Griffith, J. Murdock, and P. T. Røine, "A 24 MHz crystal oscillator with robust fast start-up using dithered injection," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan./Feb. 2016, pp. 104–105.
[21] Y. I. Kwon, S.-G. Park, T.-J. Park, K.-S. Cho, and H.-Y. Lee, "An ultra low-power CMOS transceiver using various low-power techniques for LR-WPAN applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 2, pp. 324–336, Feb. 2012.
[22] Y.-H. Liu *et al.*, "A 3.7 mW-RX 4.4 mW-TX fully integrated Bluetooth Low-Energy/IEEE802.15.4/proprietary SoC with an ADPLL-based fast frequency offset compensation in 40 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 236–237.
[23] J. Yin, S. Yang, H. Yi, W.-H. Yu, P.-I. Mak, and R. P. Martins, "A 0.2 V energy-harvesting BLE transmitter with a micropower manager achieving 25% system efficiency at 0dBm output and 5.2 nW sleep power in 28 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 450–451.
[24] T. Sano *et al.*, "A 6.3 mW BLE transceiver embedded RX image-rejection filter and TX harmonic-suppression filter reusing on-chip matching network," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 240–241.
[25] K. W. Kuo *et al.*, "A Bluetooth low-energy transceiver with 3.7-mW all-digital transmitter, 2.75-mW High-IF discrete-time receiver, and TX/RX switchable on-chip matching network," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1144–1162, Apr. 2017.

Haidong Yi (S'16) received the B.Sc. degree in electronic science and technology from Henan University, Kaifeng, China, and the M.Eng. degree in microelectronics from Fudan University, Shanghai, China, in 2012 and 2015, respectively. He is currently pursuing the Ph.D. degree in electronic and computer engineering with the University of Macau, Macao, China, with focusing on the ultra-low-voltage low-power analog and RF circuit techniques.

Wei-Han Yu (S'09) received the B.Sc. and M.Sc. degrees in electrical and electronics engineering from the University of Macau (UM), Macao, China, in 2010 and 2012, respectively, and the Ph.D. degree from the State-Key Laboratory of Analog and Mixed-Signal VLSI and Faculty of Science and Technology, Department of Electronic and Computer Engineering, UM, in 2018.

He is currently a Post-Doctoral Researcher at UM. His current research interests include RF and mm-wave transmitter, power amplifier, digital predistortion, and EM modeling for next-generation mobile communications.

Dr. Yu was a recipient the IEEE ISSCC STGA Award and the FDCT S&T Postgraduate Student Award in 2016, and the IEEE SSCS Predoctoral Achievement Award in 2018.

Pui-In Mak (S'00–M'08–SM'11) received the Ph.D. degree from the University of Macau (UM), Macao, China, in 2006.

He is currently a Full Professor with the Faculty of Science and Technology, Department of Electronic and Computer Engineering, UM, and an Associate Director (Research) with the State Key Laboratory of Analog and Mixed-Signal VLSI, UM. His current research interests include analog and radio-frequency (RF) circuits and systems for wireless and multidisciplinary innovations.

Prof. Mak co-received the DAC/ISSCC Student Paper Award 2005, the CASS Outstanding Young Author Award 2010, the National Scientific and Technological Progress Award 2011, the Best Associate Editor of IEEE Transactions on Circuits and Systems II 2012 and 2013, the A-SSCC Distinguished Design Award 2015, and the ISSCC Silkroad Award 2016. In 2005, he was decorated with the Honorary Title of Value for scientific merits by the Macau Government. He was an Editorial Board Member of IEEE Press from 2014 to 2016, a member of the Board-of-Governors of IEEE Circuits and Systems Society from 2009 to 2011, a Senior Editor of the IEEE Journal on Emerging and Selected Topics in Circuits and Systems from 2014 to 2015, and an Associate Editor of the IEEE Transactions on Circuits and Systems I from 2010 to 2011 and 2014 to 2015 and II 2010 to 2013. He has been an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and the IEEE Solid-State Circuits Letters since 2017. He was the TPC Vice Co-Chair of ASP-DAC in 2016, a TPC Member of A-SSCC from 2013 to 2016, ESSCIRC from 2016 to 2017. He has been a TPC Member of ISSCC since 2016. He was a Distinguished Lecturer of the IEEE Circuits and Systems Society from 2014 to 2015 and is currently the IEEE Solid-State Circuits Society. He is currently the Chair of the Distinguished Lecturer Program of IEEE Circuits and Systems Society.

Jun Yin (M'14) received the B.Sc. and M.Sc. degrees in microelectronics from Peking University, Beijing, China, in 2004 and 2007, respectively, and the Ph.D. degree in electronic and computer engineering the from the Hong Kong University of Science and Technology, Hong Kong, in 2013.

He is currently an Assistant Professor with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China. His current research interests include CMOS RF integrated circuits for wireless communication and wireless sensing systems, specializing in the frequency generation and synthesis circuits including oscillators and phase-locked loops.

Rui P. Martins (M'88–SM'99–F'08) was born in 1957. He received the bachelor's, master's, and Ph.D. degrees, as well as the Habilitation for Full-Professor in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), TU of Lisbon, Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively.

He has been with the Department of Electrical and Computer Engineering, IST, since 1980. Since 2013, he has been with the Faculty of Science and Technology (FST), Department of Electrical and Computer Engineering, University of Macau (UM), Macao, China, as a Chair-Professor. In FST, he was the Dean of the Faculty from 1994 to 1997. He has been a Vice-Rector of the UM since 1997. From 2008, after the reform of the UM Charter, he was nominated after open international recruitment, and reappointed in 2013, as a Vice-Rector (Research) until 2018. Within the scope of his teaching and research activities, he has taught 21 bachelor and master courses, and in UM, has supervised (or co-supervised) 19 Ph.D. theses and 21 Master theses. He was a Co-Founder of Chipidea Microelectronics (Macao) (now Synopsys) from 2001 to 2002, and the Founding Director of the Analog and Mixed-Signal VLSI Research Laboratory of UM, and the State Key Laboratory of China (the first in Engineering in Macao). He has co-authored six books and nine book chapters, and 111 papers in scientific journals and 266 papers in conference proceedings, as well as other 60 academic works. He holds 16 US Patents and 2 Taiwan Patents.

Dr. Martins was a Nominations Committee Member of the IEEE CASS in 2016 and is currently the Chair of the IEEE Fellow Evaluation Committee of IEEE CASS, class of 2018. He was a member of the IEEE CASS Fellow Evaluation Committee from 2013 to 2014, and CAS Society representative in the Nominating Committee, for the election in 2014, of the Division I (CASS/EDS/SSCS)—Director of the IEEE. He was a recipient of the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999, and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001. He was the Founding Chairman of the IEEE Macau Section from 2003 to 2005 and the IEEE Macau Joint-Chapter on Circuits and Systems (CAS)/Communications from 2005 to 2008 [2009 World Chapter of the Year of the IEEE CAS Society (CASS)]. He was the General Chair of the 2008 IEEE Asia-Pacific Conference on CAS—APCCAS'2008, and the Vice-President for Region 10 (Asia, Australia, and the Pacific) of the IEEE CASS from 2009 to 2011. Since then, he was the Vice-President (World) Regional Activities and Membership of the IEEE CASS from 2012 to 2013, and an Associate Editor of the IEEE TRANSACTIONS ON CAS II: EXPRESS BRIEFS from 2010 to 2013, nominated the Best Associate Editor of T-CAS II from 2012 to 2013. He was the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference—ASP-DAC'2016. In 2010, he was elected, unanimously, as a Corresponding Member of the Portuguese Academy of Sciences, Lisbon, being the only Portuguese Academician living in Asia.