A 3.2 ppm/°C Second-Order Temperature Compensated CMOS On-Chip Oscillator Using Voltage Ratio Adjusting Technique

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***Abstract*— A CMOS on-chip oscillator for the local interconnection network bus is presented. The temperature dependence of the output frequency is compensated by the voltage ratio adjusting technique. The frequency variation with supply voltage is reduced by a voltage regulator with a wide input range of 1.8–5 V. The frequency shift caused by package stress is minimized by resistor placement. Over a temperature range of −40 °C to 150 °C, the measured temperature coefficients of the output frequency are 3.2 ppm/°C without the effect of the package stress and 14.2 ppm/°C with the effect of the package stress, respectively. The measured frequency variation with supply voltage is within ±0.015%.**

***Index Terms*— Frequency shift, frequency variation, on-chip oscillator (OCO), package stress, temperature compensation.**

I. Introduction

In RECENT years, the demand for CMOS on-chip oscillators (OCOs) has increased rapidly because they are more robust against mechanical shock than crystal oscillators and provide lower bill of materials cost. One of their potential applications is the local interconnection network (LIN) bus. As shown in Fig. 1, the LIN bus is used in sub-control systems such as door-mirror adjustment and widow lift control system in automobiles to allow the intercommunication of microcontrollers. Up to now, the clock used in the LIN bus is provided by crystal oscillators. It is because no CMOS OCO can meet all the following requirements: 1) the clock frequency is tens of megahertz (24 MHz in general), which guarantees the operation of the microcontrollers and 2) the frequency variation with temperature and supply voltage is within ±0.5% [1], which guarantees the synchronization for data transmission through the LIN bus. The CMOS OCOs in [2]–[4] have a frequency variation within ±0.5% but their frequencies are lower than 24 MHz. In [5] and [6], the frequencies of the CMOS OCOs are enough but their frequency variations are over ±0.5%. Moreover, to the best of the author's knowledge, the frequency shift caused by package stress has never been considered in the past CMOS OCOs.

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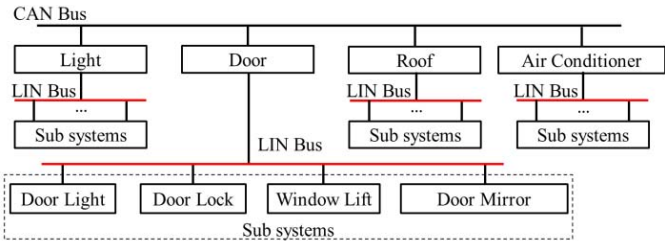


Fig. 1. Example of the application of the LIN bus.

This paper discusses a 3.2 ppm/°C CMOS OCO to meet the requirements of the clock used in the LIN bus. In [7], the following three issues have been described briefly.

1) In order to meet the frequency requirement, a resistor and capacitor (*RC*) network is combined with a voltage-controlled oscillator (VCO).
2) The voltage ratio adjusting (VRA) technique is developed to realize the second-order temperature compensation over a temperature range of −40 °C to 150 °C.
3) The frequency shift caused by package stress is minimized by resistor placement based on the simulation of package stress.

In this paper, we discuss these three issues in more detail, which includes the improvement of the loop bandwidth of the OCO at high output frequencies and the solution of the stability problem caused by the fine trimming resolution. In addition, we discuss how to use interpolation to reduce the number of trim codes which is required in trimming.

II. Architecture of the Proposed On-Chip Oscillator

Fig. 2 illustrates the architecture of the proposed OCO, which is similar to the OCO in [3]. Relaxation oscillators [2], [4]–[6] cannot generate a frequency which is higher than the operation frequencies of their *RC* networks. In contrast, this OCO can generate that frequency by adjusting a divide-by-N divider. This allows us to expand the output frequency to 80 MHz for motor control. A voltage regulator (REG) is used to reduce the frequency variation with supply voltage (1.8–5 V). A frequency-locked loop (FLL) is comprised of a *RC* network, an integrator, a VCO, and a divide-by-N divider. Due to the FLL, the current I_R is equal to the average current for charging the capacitors C_1 and C_2 ($C_1 = C_2 = C =$ 250 fF), which means $I_R = 2V_bCf_o/N$. Therefore, the output

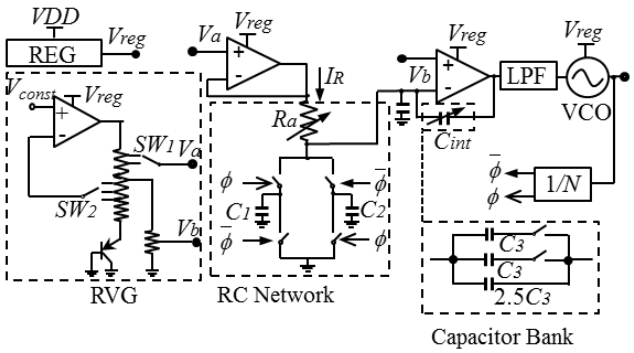


Fig. 2. Architecture of the proposed OCO.

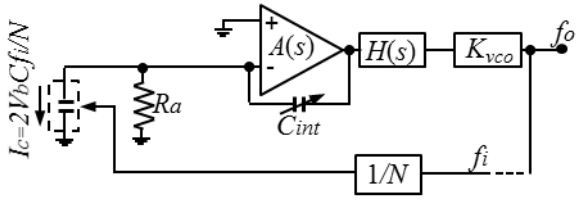


Fig. 3. Small signal equivalent architecture of the proposed OCO.

frequency f_o becomes

$$f_o = N\frac{1}{2\mathrm{CR}_a}\frac{V_a - V_b}{V_b} \tag{1}$$

where V_a and V_b are the two reference voltages provided by a reference voltage generator (RVG), R_a (150 kΩ) is the resistor used in the *RC* network, and N is the division ratio. According to (1), the output frequency can be increased by increasing N.

In our design, the operation frequency of the *RC* network is set to 24 MHz and a wide adjustable range of N from 1 to 10/3 is used to generate the desired frequency range from 24 to 80 MHz. A low-pass filter is used before the VCO to reduce the jitter caused by the fractional-N divider. A large N results in a high output frequency, but causes a long startup time because it decreases the bandwidth of the OCO. Since a startup time of shorter than 2 μs is demanded in typical condition in our application, we need to alleviate the reduction of the bandwidth.

The small signal equivalent circuit of the OCO is shown in Fig. 3. The open loop gain is

$$\frac{f_o}{f_i} \approx -\frac{2V_b A_0 R_a C K_{\mathrm{vco}}}{N(1 + s/2\pi f_{\mathrm{lpf}})(1 + sA_0 R_a C_{\mathrm{int}})} \tag{2}$$

where A_0 is the dc gain of the operation amplifier (OP-AMP) and f_{lpf} is the bandwidth of the LPF. Then, the close loop bandwidth of the OCO can be written as

$$f_{u\_\mathrm{oco}} \approx \frac{V_b C K_{\mathrm{vco}}}{\pi N C_{\mathrm{int}}} \tag{3}$$

which shows that f_{u_oco} is inversely proportional to N. Therefore, when $N = 10/3$, the bandwidth of the OCO is much narrower than that when $N = 1$.

In order to solve that problem, C_{int} is changed with respect to N, which reduces the change of the bandwidth. A capacitor bank is used in C_{int} as shown in Fig. 2, where the identical capacitance C_3 is 1 pF. Fig. 4 shows the change of the bandwidth of the OCO with respect to N. Without the capacitor bank, the bandwidth reduces by a third when $N = 10/3$. With the capacitor bank, the bandwidth only reduces by a twice. It demonstrates that the reduction of the bandwidth caused by increasing N is alleviated by the capacitor bank.

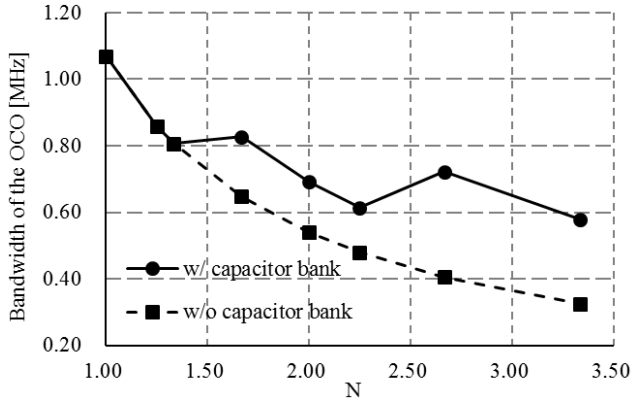


Fig. 4. Change of the bandwidth of the OCO with respect to N.

III. Voltage Ratio Adjusting Technique

A. Theory of the Voltage Ratio Adjusting Technique

Although the first-order temperature coefficients (TC1s) of the resistors have been compensated in the CMOS OCOs [2]–[6], frequency variations are deteriorated by their second-order temperature coefficients (TC2s). Several second-order temperature compensations have been used in band gap references [8]. However, these compensations are fundamentally different from what is required in this paper, because not voltage but the voltage ratio should be used to compensate the TC2 of R_a.

The key point of the VRA is that the TC1 and TC2 of the voltage ratio can be controlled by only adjusting the TC1 of V_a and that of V_b. Assuming that all the higher order (≥3) TCs are zero, we have

$$f_o = f_{o0}(1 + \lambda_f \Delta T + \xi_f \Delta T^2) \tag{4}$$

where f_{o0} is f_o at room temperature, and λ_f and ξ_f are the TC1 and the TC2 of f_o, respectively. According to (1), we also have

$$f_o = \frac{N}{2C}\frac{1}{R_a(1 + \lambda_R \Delta T + \xi_R \Delta T^2)} \times \frac{V_{a0}(1+\lambda_a \Delta T+\xi_a \Delta T^2) - V_{b0}(1+\lambda_b \Delta T+\xi_b \Delta T^2)}{V_{b0}(1 + \lambda_b \Delta T + \xi_b \Delta T^2)} \tag{5}$$

where R_{a0}, V_{a0}, and V_{b0} are the parameters in (1) at room temperature and other parameters are defined in Table I. Because (4) must be equivalent to (5), ignoring the higher order terms (≥3), we can get

$$\lambda_f = \frac{V_{a0}}{V_{a0} - V_{b0}}(\lambda_a - \lambda_b) - \lambda_R \tag{6}$$

$$\xi_f = \frac{V_{a0}}{V_{a0} - V_{b0}}(\xi_a - \xi_b) - \xi_R - \lambda_R \lambda_b - (\lambda_R + \lambda_b)\lambda_f. \tag{7}$$

TABLE I
PARAMETERS DEFINITION

λ_a	TC1 of V_a	ξ_a	TC2 of V_a
λ_b	TC1 of V_b	ξ_b	TC2 of V_b
λ_R	TC1 of R_a	ξ_R	TC2 of R_a
λ_{be}	TC1 of V_{be}	ξ_{be}	TC2 of V_{be}
ΔT	Temperature deviation from room temperature		
V_{const}	Input voltage of the RVG		
V_{be0}	Base-emit voltage of the bipolar transistor at room temperature		
β, θ, γ, m	Resistance ratios as shown in Fig. 4		

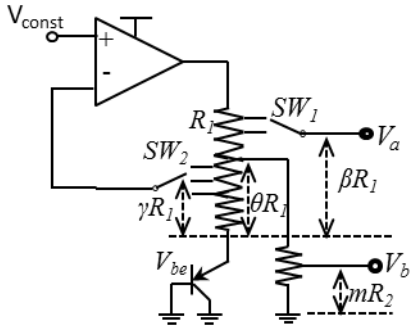


Fig. 5. Proposed RVG circuit.

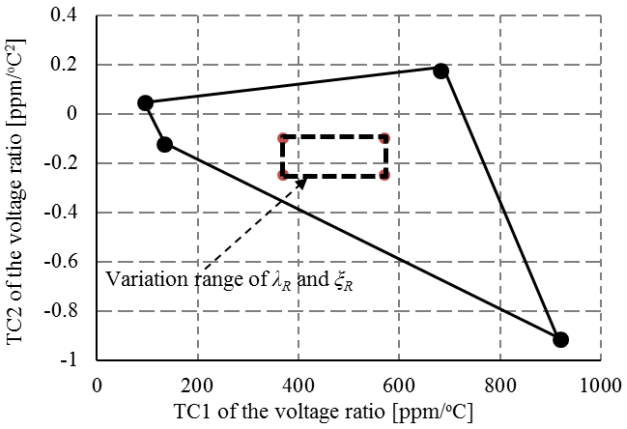


Fig. 6. Adjustable range of the TC1 and TC2 of the voltage ratio.

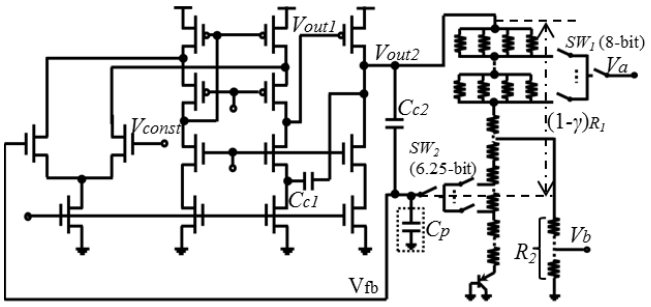


Fig. 7. Detail circuit of the RVG.

When we get $\lambda_f = 0$ by adjusting $\lambda_a - \lambda_b$, (7) becomes

$$\xi_f = \frac{V_{a0}}{V_{a0} - V_{b0}}(\xi_a - \xi_b) - \xi_R - \lambda_R \lambda_b. \tag{8}$$

According to (8), $\xi_f = 0$ can be obtained by adjusting λ_b. It indicates that the first- and second-order temperature compensation can be realized by only adjusting λ_a and λ_b.

In order to explain that the proposed RVG can be used for the VRA technique, the RVG circuit is redrawn in Fig. 5. The adjustment of λ_a and λ_b is realized by changing the switches SW_1 and SW_2. According to the architecture of the RVG, (6) and (8) can be rewritten as (9) and (10), as shown at the bottom of this page, respectively.

All parameters in (9) and (10), as (11) and (12) shown at the bottom of the next page, are also shown in Table I. When the second-order temperature independence of f_o is completely compensated, we must have $\lambda_f = \xi_f = 0$. Then according to (9) and (10), the required β and γ for temperature compensation can be solved as

Since a unique β and γ can be calculated when $\lambda_f = \xi_f = 0$, the RVG can provide the required reference voltages to realize the VRA technique.

B. Stability Problem Caused by the Wide Adjustable Range and Fine Resolution

In order to guarantee successful temperature compensation against process and voltage variation, a wide adjustable range of TC1 and TC2 of the voltage ratio is employed. Fig. 6 shows that the adjustable range of TC1 of the voltage ratio is set to approximately three times the variation range of λ_R, and the adjustable range of TC2 of the voltage ratio is set to approximately two times the variation range of ξ_R. In order to get an enough accuracy of temperature compensation, an 8-bit control word SW_1 and a 6.25-bit control word SW_2 are used. Therefore, the resolution of TC1 and that of TC2 are approximately 2.14 and 0.0075 ppm/°C^2, respectively.

As shown in Fig. 7, a thermometer code is used to avoid the effect of the on-resistance of the switches, which then results in a smaller resistance mismatch than a binary code.

$$\lambda_f = -\lambda_{\text{be}} \frac{V_{\text{be0}} V_{\text{const}} \frac{\beta-\theta}{\gamma}}{V_{\text{const}} \left\{ \frac{\theta}{\gamma} \left[1 + \frac{(\beta-\theta)R_1}{R_2} - m \right] + \frac{\beta-\theta}{\gamma} \right\} - V_{\text{be0}} \left\{ \frac{\theta-\gamma}{\gamma} \left[1 + \frac{(\beta-\theta)R_1}{R_2} - m \right] + \frac{\beta-\theta}{\gamma} \right\} V_{\text{const}} \frac{\theta}{\gamma} - V_{\text{be0}} \frac{\theta}{\gamma}} \tag{9}$$

$$\xi_f = \frac{V_{\text{be0}} \lambda_R \lambda_{\text{be}} (\theta - \gamma)}{V_{\text{const}} \theta - V_{\text{be0}} (\theta - \gamma)} + \frac{\xi_{\text{be}}}{\lambda_{\text{be}}} \lambda_R - \xi_R \tag{10}$$

However, it causes a stability problem of the OP-AMP because the large parasitic capacitance generates an additional pole. In Fig. 7, it is shown that the OP-AMP is a second-stage folded cascode amplifier [9]. In general, the first pole is at the node V_{out1} and the second pole is at the node V_{out2}. The capacitor C_{c1} (300 fF) is employed to split these two poles to guarantee the stability. However, a large parasitic capacitance C_p of over 600 fF is generated by over 300 switches and 1000 identical resistors in R_1(200 kΩ). This parasitic capacitance causes an additional pole at the node V_{fb}. When R_2 (500 kΩ) is ignored, the frequency of this pole is

$$f_{Rp} = \frac{1}{2\pi\gamma(1-\gamma)R_1C_p}. \tag{13}$$

Since $\gamma\ (1-\gamma)R_1$ is approximately 40 kΩ in our design, we can calculate the pole frequency $f_{Rp} \approx 6.6$ MHz by (13). Because this frequency is lower than the frequency of the pole at the node V_{out2}, the additional pole becomes the second pole of the OP-AMP, which then deteriorates the phase margin.

We can increase the capacitance C_{c1} to improve the phase margin but it causes a low bandwidth and a low slew rate. Therefore, a compensation capacitor C_{c2} (800 fF) is added to create a high frequency signal path as shown in Fig. 7. With this capacitor, the transfer function from V_{out2} to the node V_{fb} becomes

$$\frac{V_{\text{fb}}}{V_{\text{out2}}} = \gamma\,\frac{1+s(1-\gamma)R_1C_{c2}}{1+s\gamma(1-\gamma)R_1(C_{c2}+C_p)}. \tag{14}$$

According to (14), a zero is generated by $(1-\gamma)\ R_1$ and C_{c2}. When $C_{c2} = C_p/(1-\gamma)$, the additional pole can be removed by the zero. In Fig. 8, it is shown that the phase margin is only 50° without C_{c2} in typical condition, which cannot guarantee the stability against process–voltage–temperature variation. When C_{c2} is added, the phase margin is increased by 46°. It means that although a large parasitic capacitance is caused by over 300 switches and 1000 identical resistors, the stability of the OP-AMP can be guaranteed.

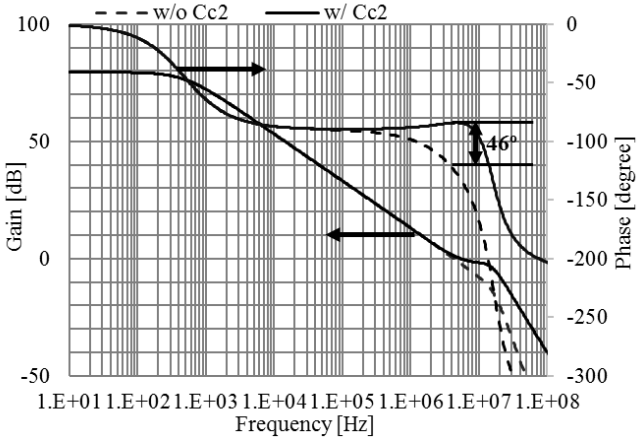


Fig. 8. Bode plot of the RVG without C_{c2} and with C_{c2}.

Fig. 9. Deformation of the package with temperature.

IV. Reduction of Frequency Shift

Silicon dies are subject to large stress after packaging because the thermal-expansion coefficients of plastic packages are several times larger than these of silicon dies [10]. Fig. 9 shows the deformation of plastic packages with temperature. In general, plastic packages are molded at a high temperature. In this condition, plastic packages and silicon dies are flat and no stress occurs. At low temperatures, plastic packages shrink at a higher rate than silicon dies and become curved, which then results in compressive stress to silicon dies. When resistors are compressed by the stress, the resistance shifts because of the piezo-resistive effect, which then causes a frequency shift. A post-package trim can eliminate the frequency shift. However, a wafer-level trim is more general in industry than a post-package trim because of the low cost. The reason of the low cost is that all the chips in one wafer can be heated or cooled together. Therefore, the frequency shift caused by package stress must be minimized.

In order to minimize the frequency shift, the following two methods are used in our design.

1) A titanium nitride (TiN) resistor (R_a) is employed because it has a smaller piezoresistance coefficient than a polysilicon resistor. We have proved that the change of the resistance of a TiN resistor is approximately 1/3 of that of a poly silicon resistor under the same stress from our previous experimental results. In addition, no additional mask is needed when we use a TiN resistor because TiN is used as the dielectric material of the metal–insulator–metal capacitors in our process.
2) The TiN resistor R_a is placed at a low-stress area which is selected by simulating the stress distribution. The

$$\beta^* = \frac{\lambda_{\text{be}}V_{\text{be0}}V_{\text{const}}\gamma^*\theta + \lambda_R[V_{\text{const}}\theta - V_{\text{be0}}(\theta-\gamma^*)]\left\{V_{\text{const}}\left(\frac{\theta^2R_1}{R_2}+m\theta\right) - V_{\text{be0}}\left[\frac{(\theta-\gamma^*)\theta R_1}{R_2}+m\theta+\gamma^*(1-m)\right]\right\}}{\lambda_{\text{be}}V_{\text{be0}}V_{\text{const}}\gamma^* + \lambda_R[V_{\text{const}}\theta - V_{\text{be0}}(\theta-\gamma^*)]\left\{V_{\text{const}}\left(\frac{\theta R_1}{R_2}+1\right) - V_{\text{be0}}\left[\frac{(\theta-\gamma^*)R_1}{R_2}+1\right]\right\}} \tag{11}$$

$$\gamma^* = \theta - \frac{V_{\text{const}}\theta\left(\frac{\zeta_{\text{be}}}{\lambda_{\text{be}}} - \frac{\zeta_R}{\lambda_R}\right)}{V_{\text{be0}}\left[\left(\frac{\zeta_{\text{be}}}{\lambda_{\text{be}}} - \frac{\zeta_R}{\lambda_R}\right) - \lambda_{\text{be}}\right]} \tag{12}$$

TABLE II
REQUIRED INFORMATION FOR STRESS SIMULATION

Width and length of the plastic package
Width, length and thickness of the silicon die
Diameter and thickness of the die pad
Thickness of the mold resin under and over the die pad
Thermal-expansion coefficient of the mold resin, the lead frame and the die pad

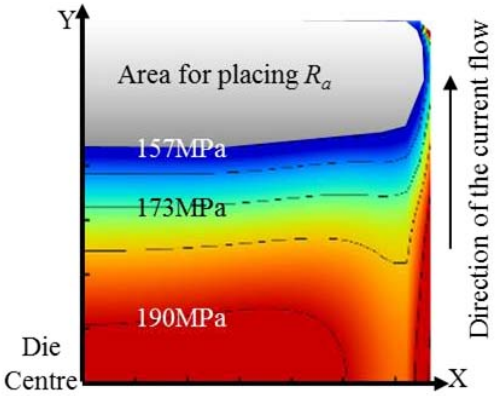


Fig. 10. Simulation result of the package stress distribution.

required information for simulating package stress distribution is shown in Table II. Inputting the information into the simulator called Ansys Mechanism, we can simulate the stress distribution as shown in Fig. 10. Only 1/4 of the die is shown due to the symmetry. It should be noted that we have proved that the resistance shift is dominated by the stress along the direction of the current flow by our experiment. Therefore, only the stress along the y-axis is shown. Because the stress is low in the area near the upper edge, this area is selected for placing R_a.

V. TRIMMING METHOD

Trimming is needed for OCOs because process variations lead to spreads in the temperature coefficient of the output frequency. The trimming of the proposed OCO differs from that of conventional OCOs in the following two respects.

1) The number of combinations of the trim code (yield up to 20 480) is much larger than that of the conventional OCOs using a first-order temperature compensation.

2) The frequency must be measured at three temperature points because we need the second-order temperature characteristic of the frequency.

These two different points cause a higher testing cost since the trimming time is increased. Therefore, it is important to develop a trimming method which uses few trim codes but can achieve an acceptable trimming accuracy.

We use interpolation to reduce the required number of trim codes in trimming. The trimming of the OCO is carried out in two stages, measurement and calculation.

In the first stage, instead of measuring the frequencies at all trim codes, we choose the trim codes by linear step and

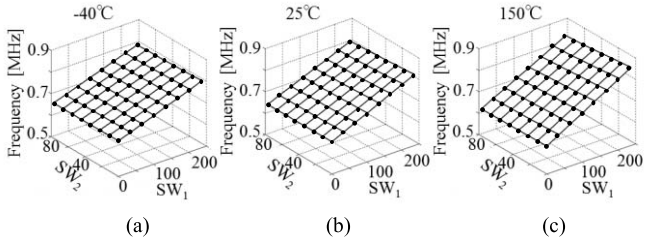


Fig. 11. Measured frequency at the selected trim codes at (a) −40 °C, (b) 25 °C, and (c) 150 °C.

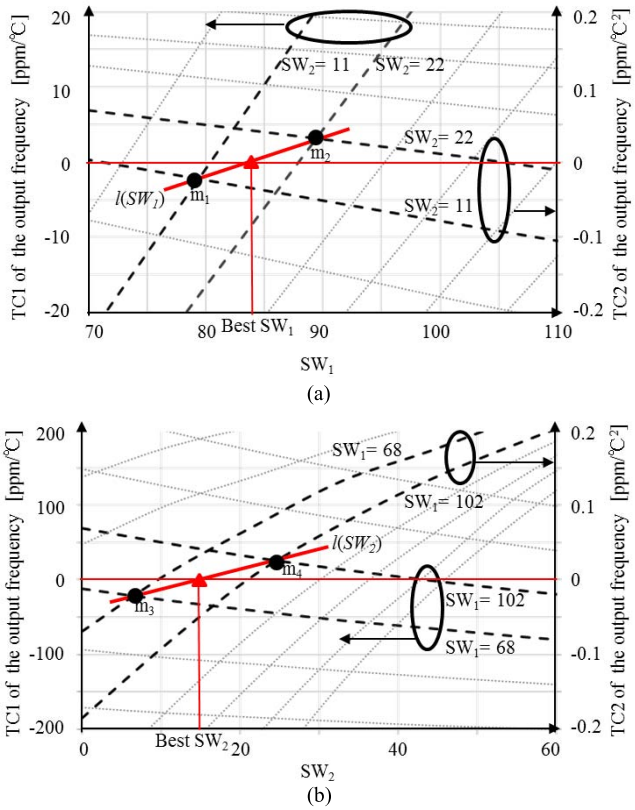


Fig. 12. Change of the TC1 and TC2 of the frequency (a) with respect to the trim code of SW_1 and (b) with respect to the trim code of SW_2.

measure the frequencies at three temperature points (−40 °C, 25 °C, and 150 °C). The steps for SW_1 and SW_2 are 34 and 11, respectively. Fig. 11(a)–(c) shows the measured frequencies at −40 °C, 25 °C, and 150 °C, respectively. It should be noted that the output frequency of the OCO shown in Fig. 11 is divided by 32, because the maximum operation frequency of the output interface of the chip is 1 MHz.

In the second stage, the target is to calculate the best trim code of SW_1 and that of SW_2 to make TC1 = TC2 = 0. From the measured frequencies shown in Fig. 11, we calculate the TC1 and TC2 of the frequencies. Fig. 12(a) shows the calculated TC1 and TC2 when fixing the trim code of SW_2. The lateral axis is the trim code of SW_1. The left vertical axis is the TC1 of the frequency, and the right vertical axis is the TC2 of the frequency. The black cross-points represent TC1 = TC2 at these trim codes. We choose the two cross-points (m_1 and m_2) which are closest to zero and connect

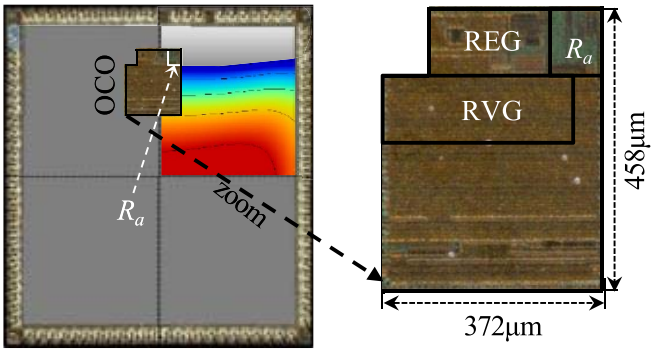


Fig. 13. Die Photographs.

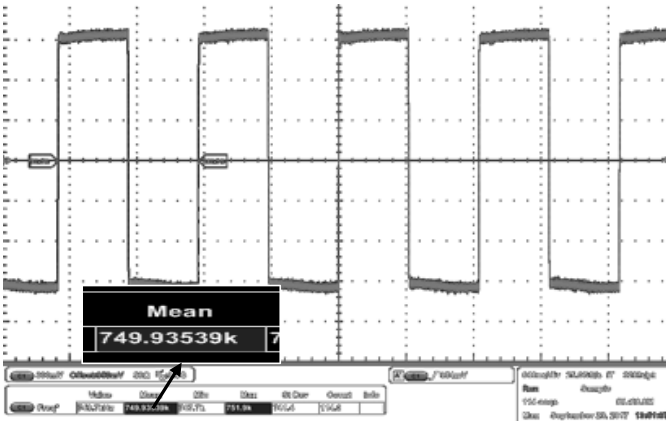
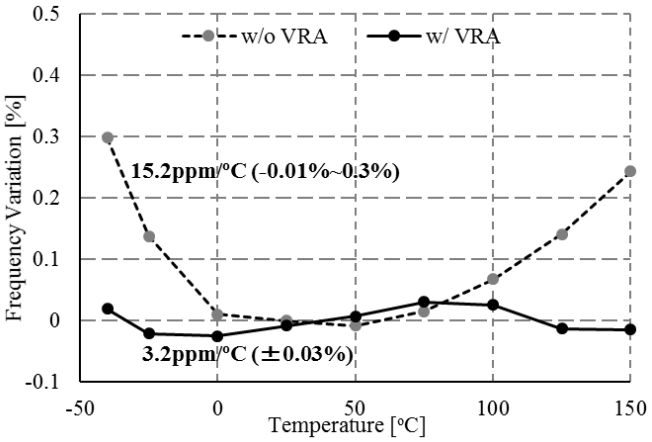
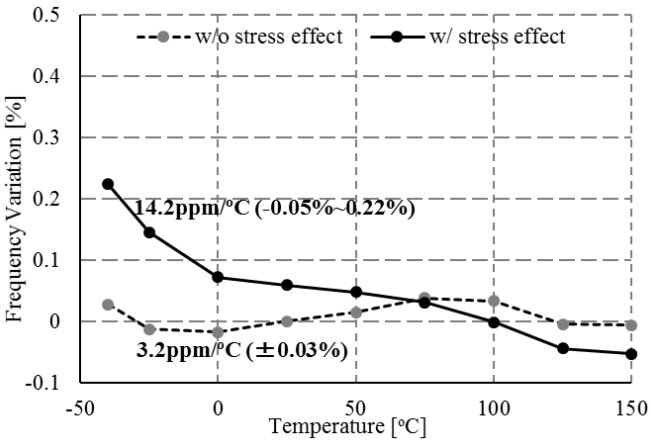


Fig. 14. Measured waveform of the proposed OCO. (The output frequency is divided by 32).



(a)



(b)

Fig. 15. Measured frequency variation with temperature (a) excluding the effect of package stress and (b) including the effect of package stress.

them to make a straight line $l(\mathrm{SW}_1)$. Then, the best trim code of SW_1 is the trim code of SW_1 when $l(\mathrm{SW}_1) = 0$, because at that trim code we have $\mathrm{TC1} = \mathrm{TC2} = 0$. Fig. 12(b) shows the calculated TC1 and TC2 when fixing the trim code of SW_1. We choose the two cross-points (m_3 and m_4) and connect them to make a straight line $l(\mathrm{SW}_2)$, which is the same as what we do in Fig. 12(a). Then, the best trim code of SW_2 is calculated by making $l(\mathrm{SW}_2) = 0$.

Using the proposed trimming method, we only have measured the frequencies at 64 trim codes, which is the same as the trimming of our previous OCO using a first-order temperature compensation. Therefore, the trimming cost is not much higher than that of our previous OCO. The trimming accuracy is also acceptable because the output frequency has a small temperature variation shown in Section VI.

VI. Experimental Results

A test chip is fabricated in 0.18-μm CMOS process. Fig. 13 shows that R_a is placed in the low-stress area, and the area of the OCO is 372×458 $\mu\mathrm{m}^2$. The chip is trimmed to oscillate at 24 MHz and measured at a temperature range of -40 °C to 150 °C and a supply voltage range of 1.8–5 V. Fig. 14 is the measured waveform of the proposed OCO. Fig. 15(a) shows that the temperature coefficient of the output frequency is 3.2 ppm/°C without the effect of the package stress. Fig. 15(b) depicts that including the effect of the package stress, the temperature coefficient of the output frequency becomes 14.2 ppm/°C, which is still better than the OCOs in [2]–[6]. The frequency variation with supply voltage is measured to be within ±0.015% as shown in Fig. 16. We also have measured over 200 chips in wafer level. The average temperature coefficient of the output frequency is

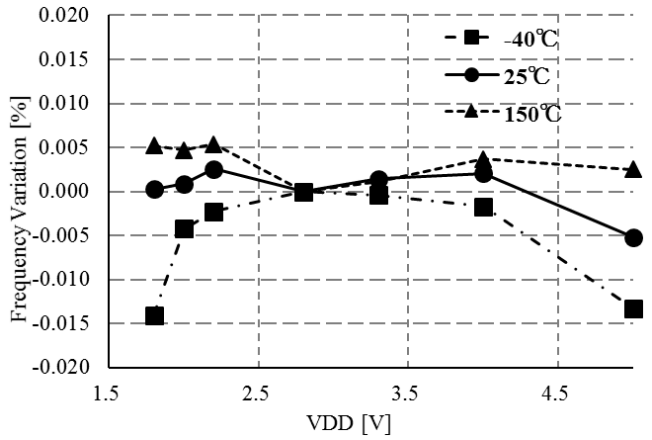


Fig. 16. Measured frequency variation with supply voltage.

TABLE III
PERFORMANCE COMPARISON

	[2]	[3]	[4]	[5]	[6]	This work
Process [CMOS]	65nm	180nm	180nm	180nm	90nm	180nm
Freq. [MHz]	6	10	14	32.8	51.3	24 to 80
Temp. Range [ºC]	-40 to125	-20 to 100	-40 to 125	-40 to 85	-20 to 100	-40 to 150
VDD Range [V]	1.15 to 1.35	1.2 to 3.0V	1.7 to 1.9V	1.5 to 3.6V	0.8 to 1.2V	1.8 to 5.0V
Freq. Variation with VDD [%]	±0.26	±0.05	±0.16	±0.13	±0.53	±0.015
Temp. Coefficient of f_o w/o Stress Effect [ppm/ºC]	24.2	66.7	23	134	21.8	3.2@ 24MHz 7.4@ 80MHz
Temp. Coefficient of f_o w/ Stress Effect [ppm/ºC]	N/A	N/A	N/A	N/A	N/A	27.4@ 24MHz
Current Efficiency [μA/MHz]	13.3	6.7	1.8	0.35	0.4	8.3@ 24MHz 5.0@80MHz
Area [mm^2]	0.02	0.22	0.04	0.013	0.027	0.17

3.3 ppm/°C and the σ is 2.45 ppm/°C. We have measured 12 chips after package. The minimum and maximum temperature coefficients of the output frequency are 11.75 and 27.65 ppm/°C, respectively. In typical condition, the measured 1 σ long-term jitter is 39 ns in a 1-ms time window and the measured startup time of the OCO is shorter than 2 μs. The performance of the OCO is summarized and compared with other state-of-the-art designs in Table III. It is shown that our proposed OCO can operate at the widest temperature range over −40 °C to 150 °C and achieves the best temperature coefficient of the output frequency.

VII. CONCLUSION

This paper discusses a CMOS OCO for the LIN bus application. Three key points are presented to improve the performance of the OCO. The first one is that a VCO and a divider are used to increase the output frequency. The second one is the VRA technique is developed to realize the second-order temperature compensation. The third one is that the frequency shift is minimized by placing the resistor in a low-stress area. The proposed OCO achieves a frequency range from 24 to 80 MHz, a temperature coefficient of 3.2 ppm/°C in wafer level, and a temperature coefficient of 14.2 ppm/°C after package, which demonstrates that it can be used in high-speed and high-accuracy applications including the LIN bus. Our next objective is to improve the power consumption to expand the application of the OCO.

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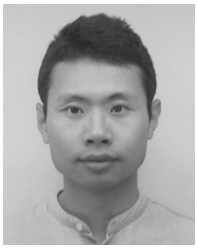

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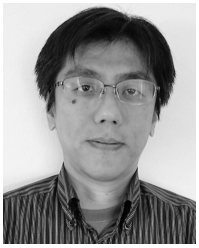

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