A 93.3% Peak-Efficiency Self-Resonant Hybrid-Switched-Capacitor LED Driver in 0.18-μm CMOS Technology

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***Abstract*— This paper presents an integrated light-emitting diode (LED) driver based on a self-resonant hybrid-switched-capacitor converter (H-SCC) operating in the megahertz range. An integrated zero-current detection (ZCD) circuit is designed to enable self-resonant operation and zero-current switching. A self-resonant timer is proposed to set the switching frequency to resonance automatically, accommodating for variations in the LED voltage, output current, inductor value, and/or parasitic components, and improving the converter efficiency at light loads without the need for an accurate clock with variable frequency. A ZCD threshold control is also proposed to enable continuous conduction mode and improve efficiency at large currents. The design of high-speed integrated current sensors to measure the inductor current in the H-SCC is also presented. Capacitors, power switches, ZCD, current monitors, and the control circuitry of the LED driver are integrated on-chip in a low-cost, 5-V, 0.18-μm bulk CMOS technology. The proposed driver was measured using inductor values between 36 and 470 nH. It achieves a peak efficiency of 93.3% and an efficiency of 83.1% at the nominal current. The LED driver is able to control a 700-mA LED down to less than 10% of its nominal current. The effective chip area is 7.5 mm^2, and the maximum power density is 373 mW/mm^2. To our knowledge, this LED driver can achieve efficiencies comparable to prior art LED drivers using a 6.6× smaller inductor.**

***Index Terms*— CMOS integrated circuit, light-emitting diode (LED) drivers, power integrated circuits, switching converters, zero-current switching (ZCD).**

I. Introduction

LIGHTING accounts for a significant percentage of global electricity usage and battery consumption in portable devices [1]. Solid-state light-emitting diode (LED) lighting has emerged as a solution offering high-efficiency and long operating lifetime. Moreover, LED technology enables novel form factors, miniaturization of light sources, color mixing flexibility, and novel smart lighting applications, based on internet of things (IoT) concepts [2]. LEDs are current controlled; thus, specialized devices, the LED drivers, are needed to regulate their current, bridging the difference between supply voltage and LED voltage with minimum losses. LED drivers should offer current control capability, high-power efficiency, high power density, and reliability in a compact form factor.

IC integration of LED drivers makes it possible to achieve compact form factors and smart functionalities such as dimming, communication, and integration with environmental sensors at low cost [3], [4]. However, it is a challenge to preserve high efficiency and current dimming capabilities when the driver is scaled to IC dimensions. Two main types of converters have been used in LED drivers: linear and switched-inductor converters. Linear converters are the most suitable candidates for IC integration, but they suffer from poor efficiency at large conversion ratios. Inductive converters [5]–[12] achieve high efficiency (ideally 100%), but they demand large inductors, which are difficult to integrate on-chip/in-package with low dc resistance. Inductive converters offer a continuous conversion ratio, which is suitable to dim the current of LEDs. Switched-capacitor converters (SCCs) have enabled fully integrated voltage converters on-chip. However, SCCs suffer from charge-transfer losses which jeopardize the converter efficiency [13]. Also, they are limited to discrete conversion ratios and suffer from poor efficiency when the conversion ratio is different from the nominal one [14]. Taking into consideration the large variation of the LED forward voltage in manufacturing and the need for dimming, SCCs are not suitable for LED drivers. Some LED drivers use an SCC followed by a linear regulator to control the LED current [15]; however, the dissipative nature of the linear stage increases the total power losses.

Recent research in integrated voltage regulators has demonstrated on-chip dc–dc converters with reasonable power efficiency using hybrid SCCs (H-SCCs) [16]–[25]. A first H-SCC approach merges SCC and inductive converter in one single topology [16]. The SCC is used to step-down the input voltage using slow high-voltage devices, while the inductive converter is used to regulate the output voltage using fast low-voltage devices. In this way, the size of the inductor is reduced. However, this solution still demands a large number of discrete passive components, which increases cost and size. Other resonant approaches have used small inductor values connected to SCCs [17]–[22]. They are able to eliminate the charge-transfer losses, as well as decrease switching losses performing soft-switching at the resonant frequency. Indeed, the switching frequency is chosen equal to the resonant

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frequency between the flying capacitors of an SCC and a small inductor.

Comparison studies among optimized on-chip power converters constrained to the same area have shown that resonant H-SCCs converters using miniature inductors have better efficiencies than switched-inductor counterparts like buck converters [26]. This is due to the higher switching frequencies required in switched-inductor converters to achieve current ripples comparable to the one observed in resonant H-SCCs. Moreover, if the converters are operated at the same frequency, same chip area, and with inductances up to hundreds of nanohenrys, H-SCCs are more efficient than buck converters due to their smaller rms-to-dc inductor current ratio, which leads to smaller conduction losses. The LED driver which is the focus of this paper aims at a strong reduction in the inductor size compared to classical switched-inductor LED drivers (which typically require inductors of several microhenry), while keeping high-power efficiency. For this reason, a resonant H-SCC architecture is selected, because of its promising efficiency with minute inductors. Small external surface mounting device (SMD) or PCB inductors with large tolerances are typically used in resonant H-SCC. Some of these converters embed flying capacitors on-chip obtaining moderate efficiencies [17], [18], [21], [22]; others use several external capacitors of large values to improve power efficiency [19], [20], [23], [24]. External components, however, increase the form factor and result in resonant frequency variations according to the tolerances of the components and the interconnections. Hence, they demand a precise clock with variable frequency to accomplish resonant operation and achieve the best efficiency.

The design of previous H-SCC topologies normally aims at voltage-to-voltage conversion, where the output voltage is kept regulated. Expanding the report in [27], this paper proposes the first CMOS integrated LED driver exploiting a self-resonant H-SCC. This driver is capable to dim a white 700-mA LED load using on-chip 5-V switches, in 0.18-μm CMOS technology, an on-chip capacitor, and a compact inductor from 36 to 470 nH, at a switching frequency in megahertz range. A self-resonant feature is also proposed in this paper, which waives the need of an accurate clock reference: the switching frequency is indeed automatically adjusted to the resonant frequency of the actual inductor and capacitors, including parasitics. An integrated zero-current detection (ZCD) circuit enables the self-resonant operation and zero-current switching (ZCS). The integrated current control loop, exploiting an on-chip current sensor adapted to the H-SCC, keeps the output current at its desired value. Section II introduces the resonant H-SCC operation. Section III presents the system architecture and describes the power train, ZCD circuitry, self-resonant operation, the current sensor, and the current loop control. Section IV shows the experimental results, and conclusions are drawn in Section V.

II. Resonant Hybrid-Switched Capacitor Converter (H-SCC) Operation

A conceptual schematic of the proposed resonant H-SCC LED driver is shown in Fig. 1. The power train is composed

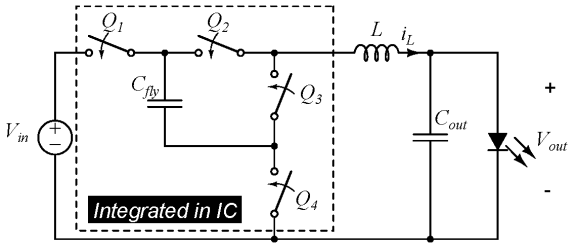

Fig. 1. Simplified schematic of integrated resonant H-SCC LED driver.

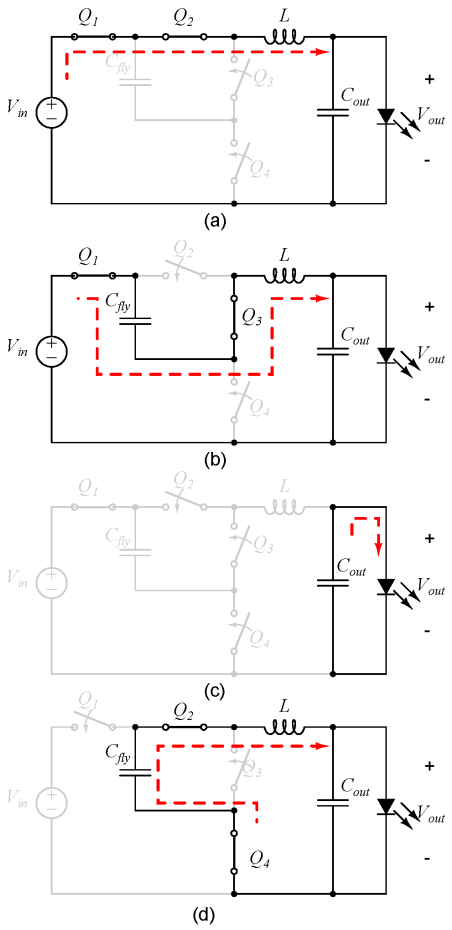

Fig. 2. Equivalent circuits of the H-SCC converter. (a) State 1. (b) State 2. (c) State 3. (d) State 4.

of four on-chip 5-V nMOS switches (Q_{1-4}), one on-chip flying capacitor (C_{fly}), one SMD (or PCB printed) air-core inductor (L), and an SMD output capacitor (C_{out}). The use of the inductor in series with the load turns the converter into a suitable current source for LEDs, such as the 186-lm/700-mA LED LX18-P150-3 [28], which is used for most experimental characterizations. The operational states of the converter are described in Fig. 2.

The H-SCC operation is based on quasi-resonance between C_{fly} and L, i.e., state 2 [S2—Fig. 2(b)] and state 4 [S4—Fig. 2(d)]. Each of these states ends when the inductor current is zero, enabling a simple implementation of ZCS. ZCS is useful to decrease the switching losses. In pure resonant

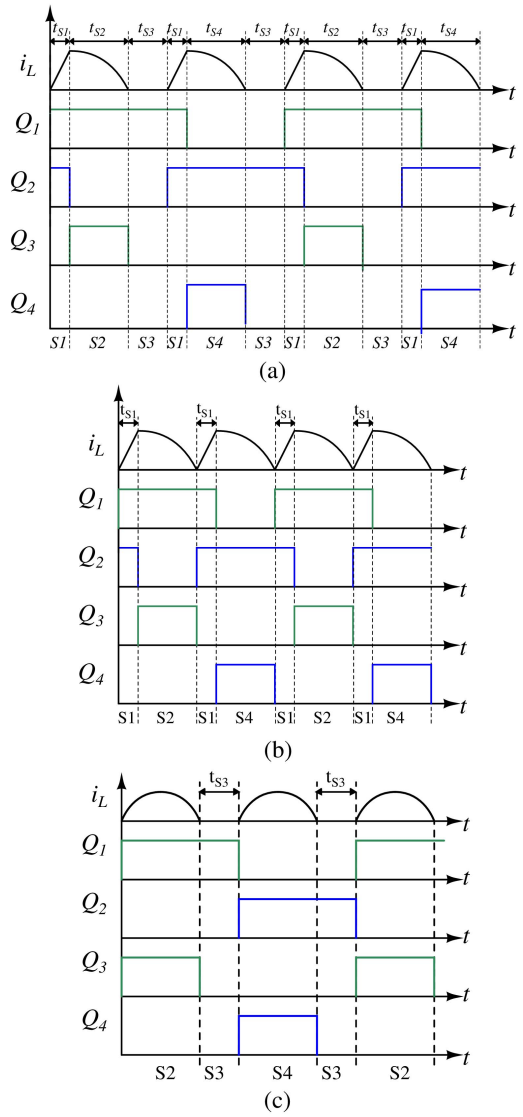

Fig. 3. Inductor current waveform and gate control signals. (a) Full-state sequence: S1→S2→S3→S1→S4→S3. (b) Sequence for an output voltage above $V_{\text{in}}/2$: S1→S2→S1→S4. (c) Sequence for an output voltage below $V_{\text{in}}/2$: S2→S3→S4→S3.

operation (state sequence S2→S4→S2→S4), the nominal conversion ratio is 2:1, i.e., $V_{\text{out}} = V_{\text{in}}/2$.

To control the LED current and to cope with variable LED forward voltages, the converter has to enable V_{out} higher and lower than $V_{\text{in}}/2$. Thus, two additional states were added to increase or decrease the output voltage and LED current, state 1 [S1—Fig. 2(a)] and state 3 [S3—Fig. 2(c)], respectively. The resonant H-SCC can operate using the full-state sequence: S1→S2→S3→S1→S4→S3.

The inductor current i_L and the gate control waveforms for the switches can be observed in Fig. 3(a). In S1, LED and inductor are charged directly from the power supply using the switches Q_1 and Q_2, thus, the current in the inductor increases almost linearly in time

$$I_L(t) = \frac{(V_{\text{in}} - V_{\text{out}})}{L} t \tag{1}$$

where V_{in} is the input voltage and V_{out} is the output voltage of the converter, as well as, the forward voltage of the LED. Thus, a larger average output current can be achieved by increasing the duration of S1 (t_{S1}). The charge in the flying capacitor is kept unchanged.

In S2, the flying capacitor is charged through the inductor and the load from V_{in}: this reduces the charge sharing losses typical of SC converters [13]. The current in the inductor is described by

$$I_L(t) = i_0 e^{-\alpha t}\cos(\omega_d t) + \frac{2(V_{\text{in}} - V_{\text{out}} - Vc_1) - i_0 R_{\text{ESR}}}{2Z} e^{-\alpha t}\sin(\omega_d t) \tag{2}$$

where i_0 and Vc_1 are the inductor current and voltage across the capacitor (C_{fly}) at the end of S1; ω_d is the resonant frequency, given by $\omega_d = (\omega_0^2 - \alpha^2)^{1/2}$, $\omega_0 = 1/(\text{LC}_{\text{fly}})^{1/2}$, $\alpha = (R_{\text{ESR}}/2L)$, and Z is the impedance given by: $Z = (L/C_{\text{fly}} - (R_{\text{ESR}}/2)^2)^{1/2}$. R_{ESR} represents the series resistance in the path of the inductor current, i.e., on-resistance of the switches, inductor resistance, and capacitor ESR. As shown in Fig. 3(a), the current i_L decreases in this state: when it returns to 0, Q_3 is switched OFF at zero current and S2 ends. The duration of S2 (t_{S2}) depends on t_{S1}, L, C_{fly}, R_{ESR}, V_{in}, and V_{out}; i.e., the time that ZCS is achieved varies with the desired output current (controlled by t_{S1}), parasitic elements present in the packaging and assembly, inductor tolerances, input supply changes, and changes in LED's forward voltage. Therefore, integrated monitors are needed to detect the zero-current event.

In S3, the inductor has zero current, the charge in the flying capacitor does not change and the LED current is supplied by the output capacitor (C_{out}). The time in S3 (t_{S3}) can be used to decrease the average LED current.

In S4, the converter completes the quasi-resonant cycle, started at S2: C_{fly} is discharged through the inductor to the load. The current in the inductor during S4 is described by

$$I_L(t) = i_0 e^{-\alpha t}\cos(\omega_d t) + \frac{2(Vc_2 - V_{\text{out}}) - i_0 R_{\text{ESR}}}{2Z} e^{-\alpha t}\sin(\omega_d t) \tag{3}$$

where Vc_2 is capacitor (C_{fly}) voltage at the end of S2. Again, as shown in Fig. 3(a), i_L decreases during this state: when it returns to 0, Q_4 is switched OFF at zero current and S4 ends. As in S2, the duration of S4 (t_{S4}) varies according to the desired output current, parasitic elements present in the packaging and assembly, inductor tolerances, changes in the input supply (embedded in Vc_2), and LED's forward voltage. Therefore, integrated monitors are used to detect the zero-current event also in this state.

So far, in the full-state sequence, S1 increases the output current, while S3 decreases the output current. Thus, using both states in the same operating sequence would be suboptimal, because it would cause a larger rms inductor current and jeopardizing power efficiency. To achieve better efficiencies, the H-SCC should operate in two different state sequences.

On the one hand, to accomplish output voltages above $V_{\text{in}}/2$, S3 should not be used. In this case, to increase the LED

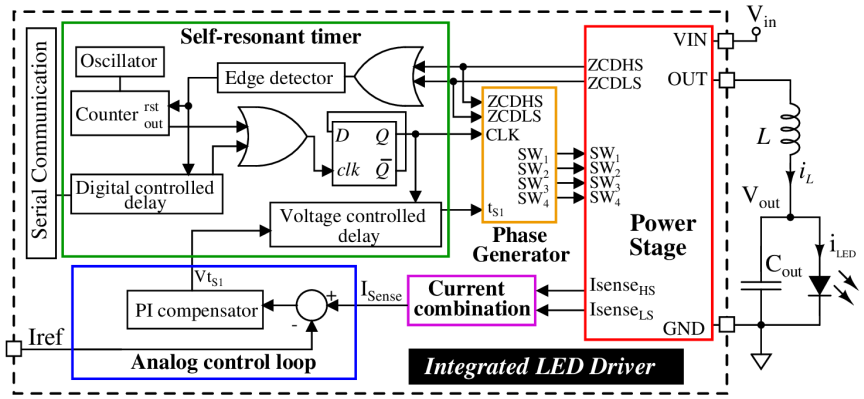

Fig. 4. Self-resonant H-SCC LED driver—system architecture. Inside the stippled box are shown all integrated components.

current, the sequence S1→S2→S1→S4 [Fig. 3(b)] is indeed preferred to the full-state sequence [Fig. 3(a)].

On the other hand, to accomplish output voltages below $V_{\text{in}}/2$, it is preferred the state sequence S2→S3→S4→S3 [Fig. 3(c)] where S1 is not used. This technique is called dynamic OFF-time modulation (DOTM) [17], [25]. It provides a good light-load efficiency as the switching frequency decreases with the addition of t_{S3} between the resonant semi-cycles.

In any of the two state sequences mentioned earlier, there is a need to know the duration of S2 and S4 to achieve ZCS. However, as aforementioned, the precise duration of S2 and S4 ($t_{\text{S2/S4}}$) is difficult to compute and varies according to the desired output current and implementation variables. For this reason, the driver uses ZCD monitors to switch to the next converter state. This technique is called self-resonant timing and will be described in Section III.

III. System Architecture

The system architecture of the complete integrated LED driver is shown in Fig. 4. It is composed of power stage, current sensor, current control loop, self-resonant timer, and phase generation block. The power stage delivers energy to the LED using the aforementioned state sequence and embeds the ZCDs. The current through the power switches is measured in each state using internal current sensing ($I\,\text{sense}_{\text{HS/LS}}$), and is suitably combined to reconstruct a scaled version of the inductor current (current combination). This information is used to control the LED current in an analog control loop, which sets the duration of S1 (t_{s1}) to accomplish the desired output current according to a reference I_{ref}, so that $I_{\text{LED}} = 512 I_{\text{ref}}$. Analog dimming can be performed by changing the current I_{ref} supplied to an external pin, to control the desired light output. The phase generator creates the logic signals that control the switches Q_{1-4} (SW_{1-4}) in the power train through different states of the converter. It uses as input t_{s1}, the output of the ZCDs, and a time reference. This time reference is generated by the self-resonant timer. These circuits are described in detail in the following.

A. Power Stage

A more detailed view of the integrated power stage is given in Fig. 5, where the power train is shown together with a self-biasing gate driver network and the ZCD.

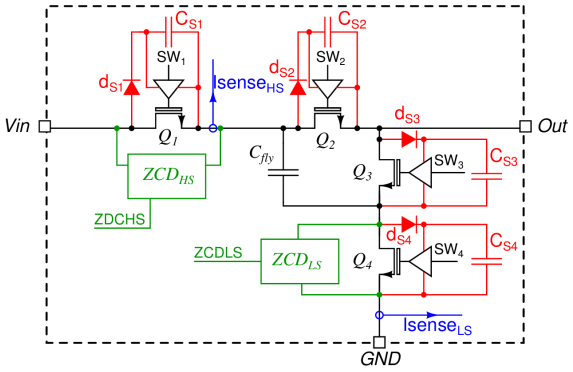

Fig. 5. Proposed resonant H-SCC power stage with ZCD and self-biasing network (d_{S1}–d_{S4} and C_{S1}–C_{S4}). All elements in this figure are integrated on-chip.

To achieve best efficiency and power density, an optimization procedure is used to set the size of the power switches and the size of the flying capacitor (C_{fly}). Here, the parameters of the 0.18-μm CMOS technology were used to compute the losses and total area of the H-SCC. C_{fly} is implemented atop the switches using double metal–insulator–metal (MIM) capacitors. This optimization is run at $V_{\text{in}} = 5$ V using different commercial inductors and considers the additional area of other passives on-chip ($C_{\text{S1}} - C_{\text{S4}}$). The optimization is also constrained to accomplish reasonable area and cost. Thus, it is performed for $I_{\text{LED}} = 0.15$ A, instead of the maximum output current $I_{\text{LEDmax}} = 0.7$ A. This results in a predicted efficiency loss at I_{LEDmax} of 4.6%, and in a 26% decrease in chip area. The optimization results are shown in Fig. 6. The efficiency increases with larger inductance values, but the positive impact becomes smaller for inductors above 150 nH. The total area of the IC does not change with the inductor value and it is dominated by the capacitor size. The results of the optimization show a tradeoff between efficiency and IC area, according to the value of C_{fly}. Therefore, the designer should make a choice between area and efficiency. In this design, C_{fly} is set to 16 nF; correspondingly, the power switches have $W = 60$ μm, $m = 512$, and use the minimum length available for 5-V transistors ($L_{\text{min}} = 0.7$ μm).

1) Self-Biasing Network: The power switches are implemented using nMOS devices that offer better on-resistance per

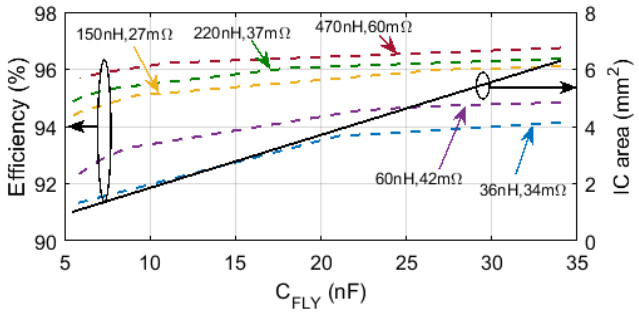

Fig. 6. Efficiency and area optimization summary for several inductors; using 0.18-μm technology parameters: $V_{\text{in}} = 5$ V and $I_{\text{LED}} = 0.15$ A. Interconnect resistance (e.g., bond wires) is not considered in this optimization.

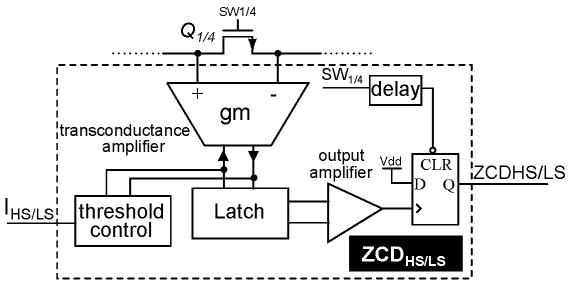

Fig. 7. Integrated ZCD block diagram.

unit area compared to pMOS. Thus, bootstrap circuits must be used to properly turn-on the nMOS devices. An on-chip self-biasing network provides the supply voltage for the gate drivers and it is composed of one nMOS transistor in diode configuration (d_{SX}) and one capacitor (C_{SX}) in parallel to each power switch. The gate drivers (tapered buffers) are supplied by the auxiliary capacitors C_{SX} ($x = 1$–4). The charging of C_{SX} depends on the voltage of the flying capacitor ($V_{C_{\text{fly}}}$). In S2, the switches Q_1 and Q_3 are turned-on charging C_{S2} to $V_{C_{\text{fly}}}$ and C_{S4} to $V_{\text{in}} - V_{C_{\text{fly}}}$. In S3, the auxiliary capacitors are not charged. In S4, Q_2 and Q_4 are turned-on charging C_{S1} to $V_{\text{in}} - V_{C_{\text{fly}}}$ and C_{S3} to $V_{C_{\text{fly}}}$. Additional charge is transferred in S1 to C_{S3} and C_{S4}, which will recover voltages below $V_{\text{in}}/2$. C_{SX} of 520 pF are embedded on-chip using MIM capacitors. This value is enough to drive the power switches, which have 69-pF input capacitance. Control signals (SW) are suitably shifted to match the voltage domain of each tapered buffer.

2) Threshold-Controlled Zero-Current Detector: The ZCD block detects when the inductor current crosses zero. This zero-current event happens exclusively at the end of S2 and S4. Therefore, ZCD is performed in S2 and S4, while the output of the ZCD is deactivated in the other states. ZCD is made using two on-chip voltage monitors, which observe the V_{ds} of the switches Q_1 (high-side ZCD_{HS}) and Q_4 (low-side ZCD_{LS}), as shown in Fig. 5. Q_3 can also be chosen instead of Q_1, as well as Q_2 instead Q_4; however, the design is relaxed when one of the terminals of the switch is fixed.

V_{ds} is transformed in a differential current by the transconductor g_m (Fig. 7), a suitable threshold current ($I_{\text{HS/LS}}$) is added/subtracted, and the difference is fed to a latch. The latch output is further amplified to full swing and sets a flip-flop when the polarity of V_{ds} changes. The flip-flop is reset at the beginning of the next state S1.

Fig. 8 shows the transistor-level implementation of the ZCD_{HS}. The transconductance amplifier is composed of 5-V transistors M_1–M_{14}. The differential pair M_1 and M_2 is properly biased to handle input voltages close to the supply voltage (V_{in}). A bias current (I_b) of 100 μA is used to bias the differential pair. The output currents of the differential pair are mirrored with a factor of 3 by M_3–M_6 and M_{11}–M_{14} to a low-voltage domain (VDD). This decreases the power consumption and allows using low-voltage devices to increase the speed of the latch. Low-voltage transistors M_{15}–M_{18} compose the latch, which is designed to provide a small hysteresis of 8 mV at the input to avoid unnecessary activity when the inductor current is close to zero.

The input imbalance at which the ZCD is triggered can be increased using the transistors M_{19}–M_{23} to inject the external current I_{HS}. The latch current I_r is increased, while I_{l} is reduced; i.e., a larger current from M_{14} is demanded to change the state of the latch. Thus, a larger V_{ds} (or I_{ds}) over the power transistor triggers the ZCD (Fig. 9). An output amplifier is implemented by M_{24}–M_{30} using a complementary self-biased differential topology [29]. This stage provides small delay and it can easily interface with digital gates thanks to its large output swing. Finally, the output of the comparator is latched to avoid oscillations at the output due to current ringing around zero. The ZCD is shut-ON/OFF using the control signal of Q_3 (SW_3). A common level shifter is used to translate the control signal to 5-V domain ($\text{SW}_{3\text{Vin}}$). After SW_3 is enabled, a digital-controlled delay (DCD) provides a blanking time that delays the activation of the output. This prevents false detections at the beginning of the S2 or S4 phase due to the power switching from S1 and the turn-on settling time. The implementation of the ZCD_{LS} is similar, but the input of the transconductance amplifier is p-type to be able to sense the low-side power switch.

The threshold control feature enables the correction of delays between the zero-current event and the effective switch-OFF of Q_3 and Q_4. Controlling I_{HS} and I_{LS}, the detection of zero can be anticipated to mitigate such delays (Fig. 9). Also, the threshold current level of the ZCD can be set to trigger the circuit when the current in the inductor is still flowing, and thus can be used to change the converter operation to continuous conduction mode (CCM), reducing the rms value and conduction losses at large output currents.

B. Current Sensor and Current Control Loop

The senseFET-based [30] current sensor is made up of three components: a high-side current sensor (CS_{HS}), a low-side current sensor (CS_{LS}), and a current combination block. The current-sensing scheme is drawn in Fig. 10. CS_{HS} observes Q_1, while CS_{LS} is connected to Q_4. The currents in Q_1 and Q_4 provide the full information of the inductor current waveform, when they are combined in a single current, I_{sense} with the right polarity and sequence using current mirrors and transmission gates (current combination block). The low-side current ($I\text{sense}_{\text{LS}}$) is flipped to match the direction of the

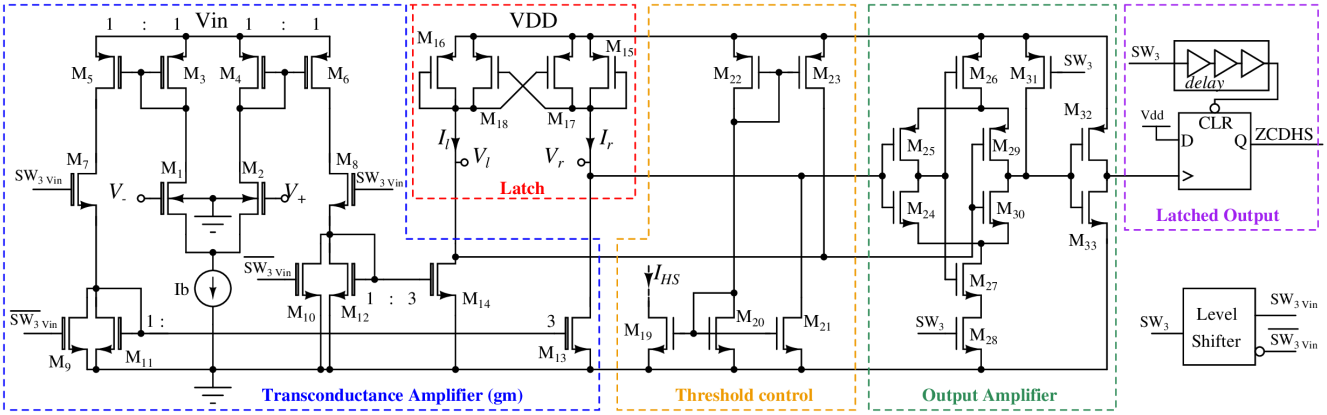

Fig. 8. Integrated ZCD—high-side circuit.

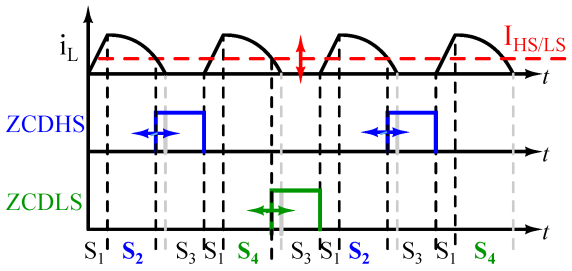

Fig. 9. Variable detection level in the ZCD.

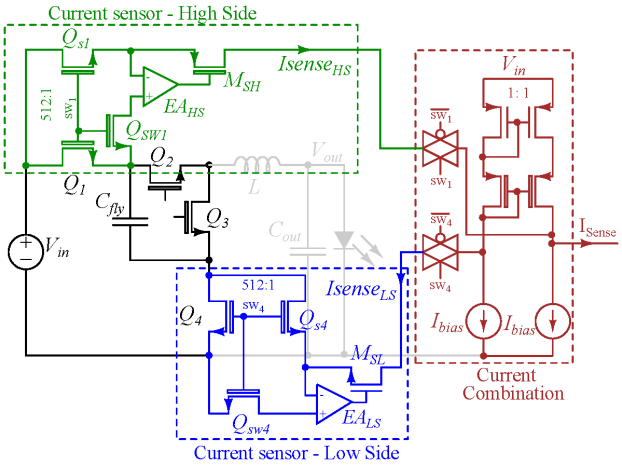

Fig. 10. Current sensing in the resonant H-SCC.

high-side current ($I\text{sense}_{\text{HS}}$) using a cascode mirror. A bias current of 100 μA is added to $I\text{sense}_{\text{LS}}$ and extracted at the output to ensure that the current mirror is always biased. CS_{HS} and CS_{LS} use a sense transistor Qs, which is matched to the power transistor, but 512 times narrower. The drain–source voltage of Q_{S1} and Q_{S4} are kept equal to the respective power transistors by an error amplifier (EA). Q_{SW} disconnects the EA from the power transistor when this is OFF, avoiding undesired switching-ON of Q_{S} [8]. The EA design, based on [8], achieves large loop-gain and GBW to guarantee high accuracy and fast response at low power consumption.

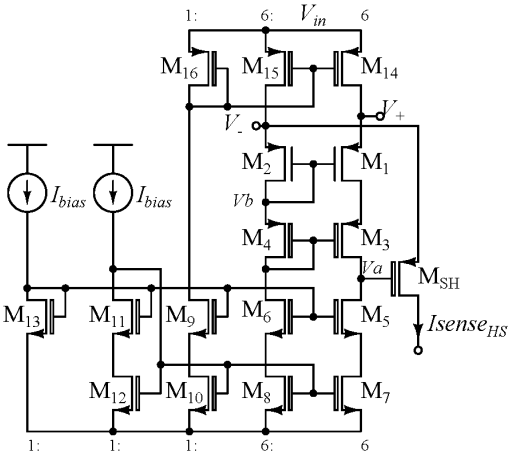

Fig. 11. EA of current sensing—high-side circuit.

The 5-V common-gate EA high-side circuit is shown in Fig. 11. The voltages V_- and V_+ are kept equal using the voltage mirror formed by M_2–M_1. The negative feedback formed by the gate-controlled transistor M_{SH} and M_1–M_4 controls the output current $I\text{sense}_{\text{HS}}$. To improve accuracy, the cascode transistors M_3–M_4 and the low-voltage cascode current mirror M_5–M_{13} increase the gain of the EA. Stability is improved using LV transistors for the input pair (M_1–M_2), moving the non-dominant pole (node Vb) to higher frequencies. To avoid slow starting of the sensor, the EA is always biased. The current mirror M_{14}–M_{16} provides bias current to the EA when the power transistor is OFF. The bias current (I_{bias}) is 5 μA.

The low-side current sensing (Fig. 12) is based on the previous common-gate EA. However, it is designed in the 1.8-V domain, which provides larger GBW and lower power consumption. To improve the headroom of the EA, a low-voltage cascode mirror is used in the voltage mirror M_1–M_4.

Fig. 13 shows the simulated waveforms of the current sensor in the LED driver. The output currents of the high- and low-side sensors, $I\text{sense}_{\text{HS}}$ and $I\text{sense}_{\text{LS}}$, are shown using the S1→S2→S1→S4 sequence. Both signals are combined in $I\text{sense}$, which is compared to the inductor current waveform.

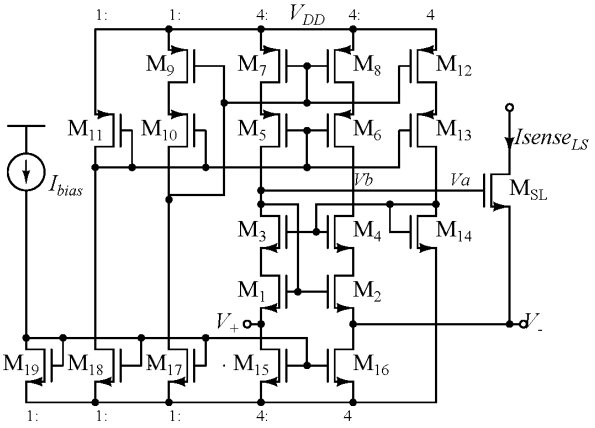

Fig. 12. EA of current sensing—low-side circuit.

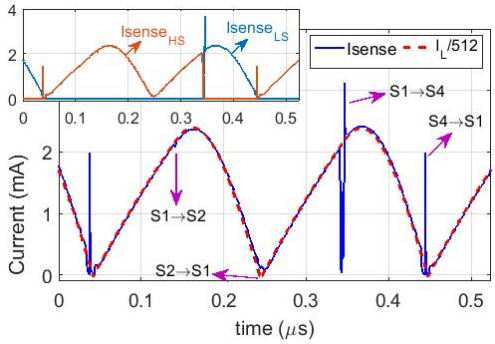

Fig. 13. Current sensor simulation waveforms in H-SCC LED driver.

The ratio between the sense current and the inductor current is 512. Glitches are expected for the transitions between S1 and S4, where the low-side sensor takes over from the high-side. The duration of the glitches depends on the (intentional) dead time between SW_1 and SW_4. Transitions between S1 and S2 do not have glitches as they are performed by the same sensor.

The control block of the H-SCC is shown in Fig. 4; it uses an external reference current I_{ref} and the average value of the sensed current I_{sense} to control the LED current changing the duration of S1 (t_{S1}). A standard PI compensator is used to guarantee steady-state accuracy. A voltage-controlled delay (VCD), formed by current-starved delay gates, translates the output voltage Vt_{S1} of the compensator to the delay t_{S1} used by the phase generators, as shown in Fig. 14.

C. Self-Resonant Timer

A time reference is needed to switch the power train, which has to be adapted according to the actual values of the inductance, capacitance, additional parasitic components, and LED forward voltage. Also, the clock frequency has to be modified to achieve ZCS when the duration of S1 (t_{S1}) is changed. This paper implements a self-resonant scheme without reference clock, which sets automatically the right S2 and S4 durations ($t_{\text{S2/S4}}$) to achieve ZCS in different conditions of operation.

The self-resonant timer is shown in Fig. 14. It uses as input the ZCD signals, which indicate that the converter has to move to the next state. An edge detector creates a pulse indicating the existence of a zero-current event. The pulse passes through a DCD (set via a serial interface), to create a controlled t_{S3}. Then, the pulse reaches the timer output D flip-flop and toggles it, initiating a new S1 state. The self-resonance not only needs to be initialized, but it can stop too due to changes in input voltages or transitory currents when the LED current is dimmed. To avoid this, a watchdog circuit is added to ensure switching in any condition: the ZCD pulse is used to reset a slow counter at 250 kHz, triggered by a fixed ring oscillator. If a zero-current event is not detected anymore, the overflow of this counter will toggle the output flip-flop, initiating a new S1 and (re)activating the current circulation in the power train. The time diagram of the self-resonant timer using the watchdog is shown in Fig. 15.

The phase generator (Fig. 14) is triggered by the timer signal, and its delayed version containing the information of t_{S1} determined by the control loop. It is composed of two non-overlapping clocks (NCLK), which guarantee a dead time between SW_1–SW_4 and SW_2–SW_3. To avoid a negative current in S3, SW_3 and SW_4 are turned off when the zero-current crossing is detected.

The start-up behavior is simulated for $L = 150$ nH, $C_{\text{out}} = 10$ μF, and $V_{\text{in}} = 5$ V, setting the target output to 0.7 A. Fig. 16 shows the output current (I_{LED}), the inductor current (I_{L}), and the self-resonant timer (timer) waveforms. One should notice that the start-up peak in the inductor is close to the operational value of the peak inductor current. This soft-start is observed because of the large on-resistance of the switches caused by the initial weak biasing of the power train. The self-biasing network requires indeed some cycles to charge its capacitors. Moreover, the converter is automatically started under no load, as the LED current remains zero until the output voltages reach the nominal forward voltage (2.8 V). Finally, the self-resonant timer starts-up thanks to its integrated watchdog. This keeps a low switching frequency until the converter reaches the steady-state condition.

IV. Experimental Results

The die photograph of the self-resonant H-SCC LED driver is shown in Fig. 17. It is fabricated using a 0.18-μm CMOS technology and directly bonded to the PCB to minimize interconnect losses. The MIM capacitors that compose C_{fly} and the self-biasing capacitors (C_{S1}–C_{S4}) are placed above the 5-V nMOS switches that compose the power train to save area. Gate drivers and analog (ZCD and current sensing) and digital circuitry are also highlighted. The value of C_{fly} is 16 nF and the effective area of the driver is 7.5 mm^2. The driver is nominally operated at $V_{\text{in}} = 5$ V with an external inductor of 150 nH (PFL2510) and an output capacitor (C_{out}) of 10 μF.

The self-resonant operation waveforms of the LED driver using a full sequence S1→S2→S3→S1→S4→S3 are shown in Fig. 18. The gate signals of the power switches can be observed as well as the current measured with the integrated current sensor (I_{sense}). The inductor current i_L measured by

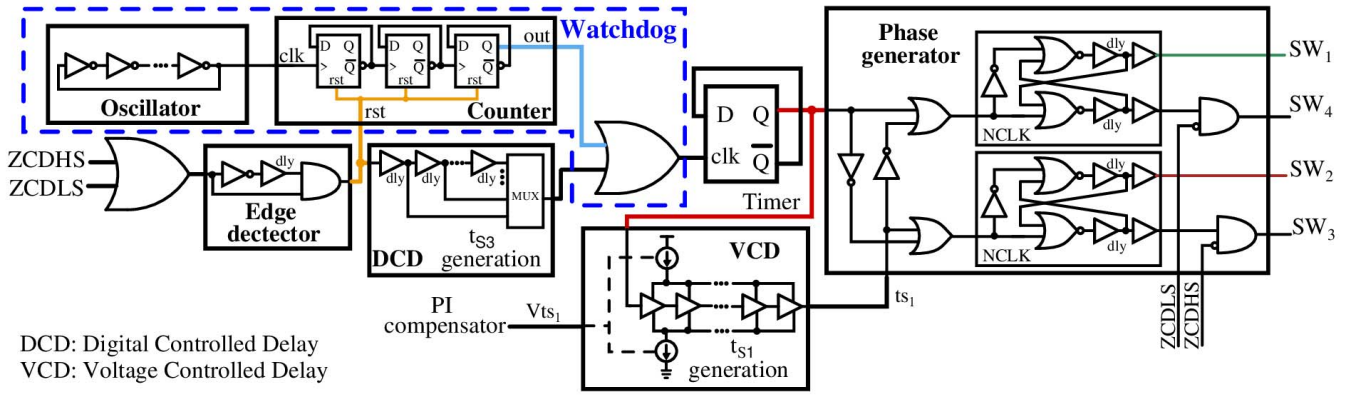

Fig. 14. Self-resonant timer with watchdog and phase generator circuits.

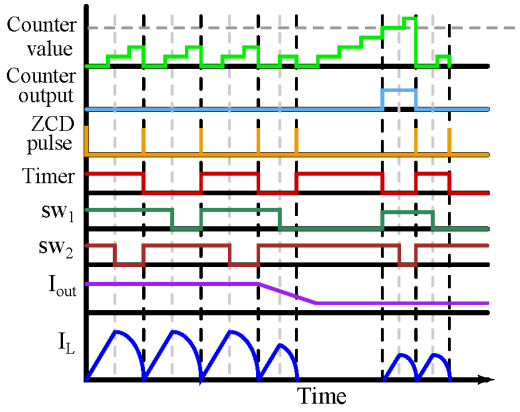

Fig. 15. Self-resonant and watchdog function based on ZCD.

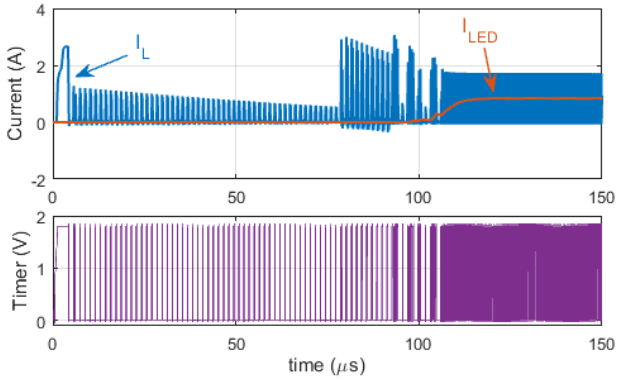

Fig. 16. Inductor current (I_L), output current (I_{LED}), and self-resonant timer (timer) simulation waveforms for a start-up event using $L = 150$ nH, $C_{\text{out}} = 10$ μF, and $V_{\text{in}} = 5$ V.

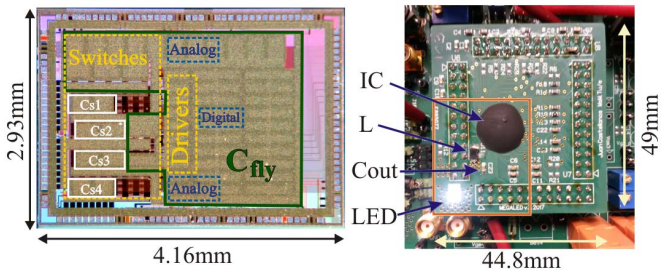

Fig. 17. Die and PCB of the self-resonant H-SCC LED driver chip.

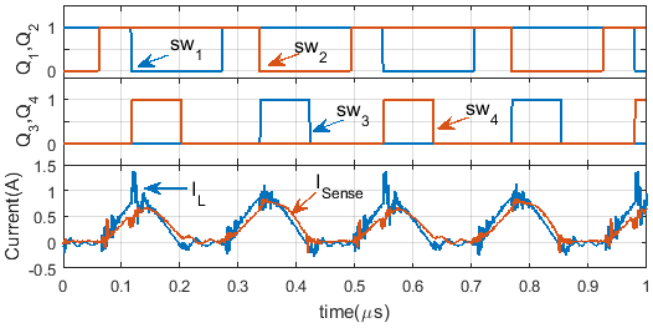

Fig. 18. Power switches' gate signals, current sensing (I_{sense}) scaled 512 times, and inductor current (I_L) experimental waveforms in self-resonant operation.

an external sensor is also added in Fig. 18. The I_{sense} shows a glitch in the transition S1→S4 when the transition between $I\text{sense}_{\text{HS}}$ and $I\text{sense}_{\text{LS}}$ is made. Also, the sensed current suffers from slope errors because of mismatch between the power MOS and the sense-FETs in the high- and low-side current sensors. The maximum measured error for the average output current after calibration is 6%. In this photograph, the full-state sequence is used for the purpose of demonstration. As the minimum forward voltage of the LEDs used in this prototype is larger than $V_{\text{in}}/2 = 2.5$ V, the optimal operational sequence for V_{out} above $V_{\text{in}}/2$ [Fig. 3(b)] is used in all other measurements.

The adaptability of the driver to operate with different inductor values thanks to the self-resonant timer is observed in Fig. 19. Here, t_{S2} and t_{S4} are automatically adjusted by the circuit changing the switching frequency; values between 2 and 6 MHz are measured for inductors between 36–470 nH.

In the inset of Fig. 19, the inductor waveforms exhibit undesired negative currents; however, this can be avoided using the threshold-controlled ZCD. Fig. 20 shows the control of the ZCD detection threshold using the bias currents I_{HS} and I_{LS}. This allows to adjust the minimum value of i_L, from an undesired negative current up to zero (for ZCS) and more, achieving continuous conduction mode. The last operation

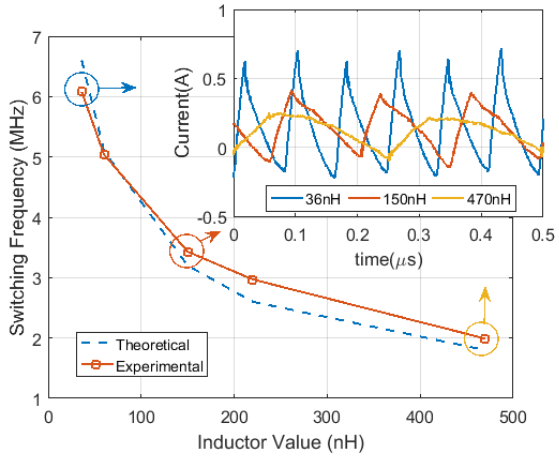

Fig. 19. Experimental switching frequency versus inductor value using self-resonant operation and inductor current (I_L) waveforms using five different inductors (PFL1050-36, PFL1050-60, PFL2510-151, PFL2510-221, and PFL2010-471) at $I_{\text{LED}} = 150$ mA and $I_{\text{HS/LS}} = 0$ μA.

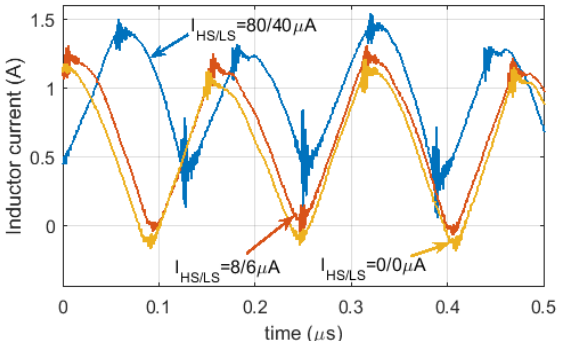

Fig. 20. Measurement of the inductor current for ZCD threshold adjustment. At $L = 150$ nH, $V_{\text{in}} = 5$ V for $I_{\text{HS/LS}} = 0$ μA: undesired negative current; $I_{\text{HS/LS}} = 8/6$ μA: ZCS and $I_{\text{HS/LS}} = 80/40$ μA: CCM.

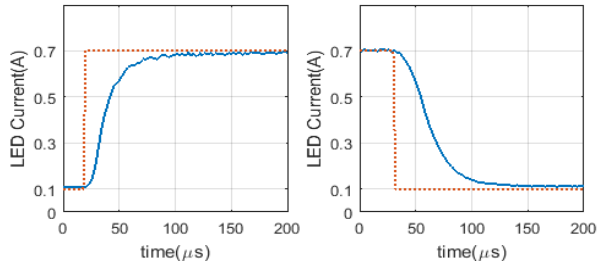

Fig. 21. Step response of the H-SCC. LED current at rise and fall transitions.

mode can be used to improve efficiency at high output current. When the LED current varies for a given $I_{\text{HS}}/I_{\text{LS}}$, ZCS is not guaranteed, as dI_L/dt is changed. Therefore, the value of $I_{\text{HS}}/I_{\text{LS}}$ needs to be tuned to the actual value of inductance and load current. This adjustment could be performed autonomously on-chip based on the measured inductor current, using e.g., a suitable lookup table (LUT) and DACs for the generation of the threshold currents.

In Fig. 21, the response of the driver to a sudden change in I_{ref} was measured, showing a 38-μs rise time and 46-μs fall time and validating the stability of the integrated control loop.

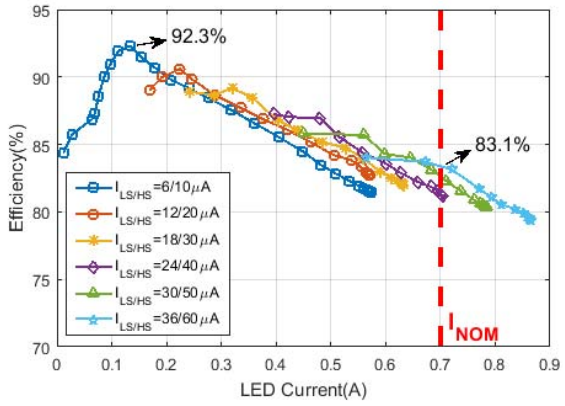

Fig. 22. Experimental efficiency versus LED current at several ZCD thresholds for $V_{\text{in}} = 5$ V and $L = 150$ nH.

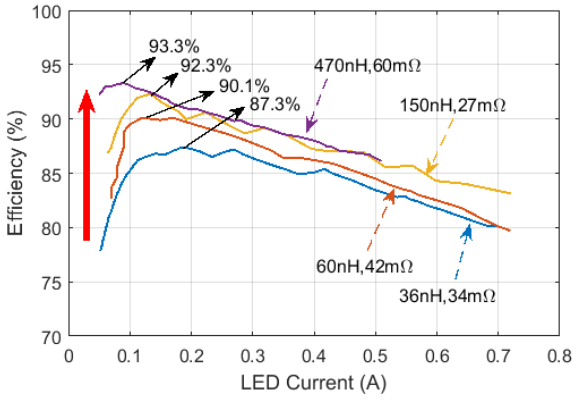

Fig. 23. Experimental efficiency versus LED current at several inductor values for $V_{\text{in}} = 5$ V, $I_{\text{LS}} = 6$–36 μA, and $I_{\text{HS}} = 10$–60 μA.

The estimated power consumption of the control circuitry is 13.1 mW, which represents almost the totality of the LED driver quiescent power losses.

The efficiency of the self-resonant H-SCC is measured using a 150-nH inductor at $V_{\text{in}} = 5$ V in the LED current range with several ZCD thresholds (Fig. 22). A peak efficiency of 92.3% is measured at $I_{\text{LS/HS}} = 6/10$ μA, where the ZCS is achieved. This efficiency gradually decreases when the output current is increased. This is due to the larger conduction losses ($I^2_{\text{Lrms}} R_{\text{ESR}}$) associated with the total series resistance in the current path R_{ESR}. This resistance is due to the on-resistance of the power switches, to the parasitic resistance of the interconnections (which is as large as 100 mΩ in our converter due to the use of conventional wire bonding) and to the resistance of the inductor. As shown in Fig. 22, at heavy loads, higher ZCD thresholds can enable a better tradeoff between switching losses and conduction losses: increasing the threshold, ZCS does not happen anymore, but the rms of the current waveform is reduced achieving CCM and higher switching frequency. Therefore, an efficiency improvement at large current is observed: the measured efficiency at the nominal current can be increased up to 83.1%. The driver is able to dim the LED below 10% of its nominal current. In Fig. 23, the efficiency is measured at different inductor values using

TABLE I
PERFORMANCE COMPARISON AMONG LED DRIVERS

	High-voltage LED drivers				***Commercial Low-voltage LED drivers***		***Low-voltage LED drivers***					
	JSSC 2015 [8]	***ISSCC 2015 [9]***	***ISSCC 2016 [10]***	***JSSC 2016 [11]***	***LM 2758 [15]***	***TPS 61054 [12]***	***JSSC 2011 [5]***	***A-SSCC 2013 [6]***	***TPEL 2014 [7]***	***This work***		
Technology	0.35µm HV	0.18µm HV	0.5µm HV	0.5µm HV	-	-	0.5µm	0.25µm HV	0.18µm	0.18µm		
Topology	Induc.	Induc.	Induc.	Induc.	SCC + Linear	Induc.	Induc.	Induc. (ext. diode)	Induc.	H-SCC		
V_{in} (V)	5-45	12-24	16-24	5-115	5.5	5	3-5.5	5	2.7-5.5	4.5-5.5		
L (µH)	8.2-39	33-68	22	10-39	-	2.2[d]	2.2	10	1	0.036	0.15	0.47
η_{Peak} (%)	97.2	96	96	94.4	90	96	90.7	92.1	91	87.3	92.3	93.3
η_{Inom} (%)	78[a,b]	72[a]	-	84[a,b]	65	70	86	84.8	86[a]	80	83.1	-
Fsw (MHz)	≤4	0.5	1.2	1.6, 2.2	1.5	2	1-2	0.52-0.58	2.5	6	3.4	2
I_{nom} (A)	0.7	1	1	0.35	0.7	0.7	1.2	0.3	2	0.7		
IC Size (mm^2)	6.6	11.2	15	9.4	3.1[c]	9[c]	5	1.014	4.1	7.5		
C_{fly} (µF)	-	-	-	-	2[d]	-	-	-	-	0.016[c]		

[a] Estimated values, [b] estimated using a single LED, [c] size of the IC package, [d] recommended values, [e] On-chip capacitor.

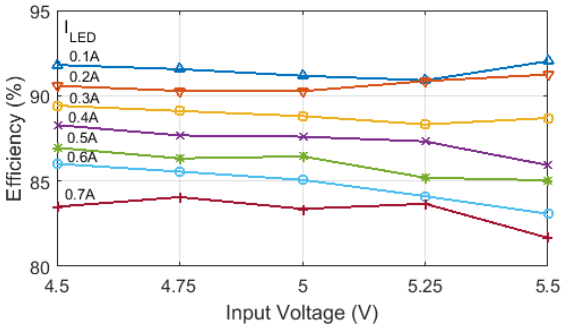

Fig. 24. Experimental efficiency versus input voltage at several LED current values using 150-nH inductor.

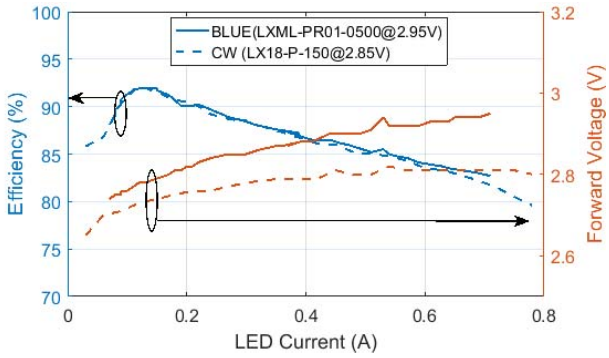

Fig. 25. Experimental efficiency and LED forward voltage versus LED current using two different LEDs and a 150-nH inductor at $V_{in} = 5$ V.

the previous methodology to tune the threshold control of the ZCD; the inductors were chosen to have similar dc resistance to make the comparison easier. A peak efficiency of 93.3% is achieved using 470 nH. One can observe that the maximum output current for this inductor is limited at about 0.5 A, due to the limited amount of delay that can be generated by the VCD. Efficiencies at low currents are improved when larger inductor values are used: this is because of the lower switching frequency, as observed previously in Fig. 19. At large currents, the larger rms values and switching frequency result in lower efficiency for small inductor values.

Fig. 24 shows the efficiency of the LED driver using input voltages from 4.5 to 5.5 V for different LED current levels. The efficiency is not jeopardized by the variation of the input supply. Also, Fig. 25 shows the efficiency of the driver and the LED forward voltage using a blue LED and a cool white (CW) LED. Here, the LED driver can supply current to LEDs with different forward voltages; while the efficiency remains the same. This also demonstrates that the driver can address LED forward voltage variations due to manufacturing or thermal drift.

The measured performance of this H-SCC LED driver is compared with prior integrated dc/dc LED drivers in Table I. When using a 150-nH inductor, this paper can achieve peak and nominal efficiencies comparable to the state-of-the-art LED drivers [5]–[7]. This represents at least a 6.6× reduction in inductor size compared to prior art. Moreover, no external flying capacitors are used. The maximum power density for this LED driver is 373 mW/mm^2. A comparison with other

works using power density as figure of merit is difficult, as most literature in Table I does not provide details on the size of the inductor used. The driver is capable to automatically adapt to different inductor values/tolerances and to variations in the LED characteristics.

V. Conclusion

This paper discusses the design and implementation of the first H-SCC integrated LED driver using self-resonant operation. By using ZCD, zero-current switching and self-resonance are achieved. In self-resonant mode, the switching frequency is automatically adapted to variations due to parasitic, tolerance of the components, inductor values, and forward voltage variation from the LED load. This eliminates the need of an accurate and variable clock reference. Also, by using a variable threshold level in ZCD, switching losses can be traded-off for lower conduction losses and efficiency can be improved at heavy loads. The LED driver controls the output current, sensing the inductor waveform with integrated current monitors. It is capable to control the current in a 700-mA LED and dim it down to 10% with efficiencies always above 80%. The peak power efficiency is 93.3%, while the efficiency at nominal current is 83.1%. Compared to prior art, this paper uses the smallest inductor values, i.e., 36 nH and achieves a maximum power density of 373 mW/mm^2.

References

[1] U.S. Department of Energy. (Dec. 7, 2015). *Rise and Shine: Lighting the World With 10 Billion LED Bulbs*. Accessed: Sep. 6, 2017. [Online]. Available: https://energy.gov/articles/rise-and-shine-lighting-world-10-billion-led-bulbs

[2] S. Li, S.-C. Tan, C. K. Lee, E. Waffenschmidt, S. Y. Hui, and C. K. Tse, "A survey, classification, and critical review of light-emitting diode drivers," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1503–1516, Feb. 2016.

[3] F. Che, L. Wu, B. Hussain, X. Li, and C. P. Yue, "A fully integrated IEEE 802.15.7 visible light communication transmitter with on-chip 8-W 85% efficiency boost LED driver," *J. Lightw. Technol.*, vol. 34, no. 10, pp. 2419–2430, May 15, 2016.

[4] *High-Efficiency White LED Driver With Programmable Ambient Light Sensing Capability and I2C-Compatible Interface*, LM3532 datasheet, Texas Instruments, Jul. 2011.

[5] S. Rao *et al.*, "A 1.2-A buck-boost LED driver with on-chip error averaged SenseFET-based current sensing technique," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2772–2783, Dec. 2011.

[6] J.-S. Guo, S.-M. Lin, and C.-H. Tsai, "A hysteretic boost regulator with emulated-ramp feedback (ERF) current-sensing technique for LED driving applications," in *Proc. ASSCC*, Singapore, Nov. 2013, pp. 61–64.

[7] P. Malcovati, M. Belloni, F. Gozzini, C. Bazzani, and A. Baschirotto, "A 0.18-μm CMOS, 91%-efficiency, 2-A scalable buck-boost DC-DC converter for LED drivers," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5392–5398, Oct. 2014.

[8] Z. Liu and H. Lee, "A 26 W 97%-efficiency fast-settling dimmable LED driver with dual-nMOS-sensing based glitch-tolerant synchronous current control for high-brightness solid-state lighting applications," *IEEE J. Solid-State Circuits*, vol. 50, no. 9, pp. 2174–2187, Sep. 2015.

[9] S. Dietrich *et al.*, "A 7.5 W-output-power 96%-efficiency capacitor-free single-inductor 4-channel all-digital integrated DC-DC LED driver in a 0.18 μm technology," in *Proc. ISSCC*, Feb. 2015, pp. 1–3.

[10] H.-A. Yang *et al.*, "A 96%-efficiency and 0.5%-current-cross-regulation single-inductor multiple floating-output LED driver with 24b color resolution," in *Proc. ISSCC*, Jan./Feb. 2016, pp. 230–231.

[11] Z. Liu and H. Lee, "A wide-input-range efficiency-enhanced synchronous integrated LED driver with adaptive resonant timing control," *IEEE J. Solid-State Circuits*, vol. 51, no. 8, pp. 1810–1825, Aug. 2016.

[12] *TPS6105x High-Power White LED Driver*, TPS61054 datasheet, Texas Instruments, Sep. 2004.

[13] M. D. Seeman, "A design methodology for switched-capacitor DC-DC converters," Ph.D. dissertation, Dept. EECS, Univ. California, Berkeley, CA, USA, 2009.

[14] M. S. Makowski and D. Maksimovic, "Performance limits of switched-capacitor DC-DC converters," in *Proc. PESC Rec.*, Atlanta, GA, USA, Jun. 1995, pp. 1215–1221.

[15] *Switched Capacitor Flash LED Driver in DSBGA Package*, LM2758 datasheet, Texas Instruments, Apr. 2008.

[16] R. C. N. Pilawa-Podgurski and D. J. Perreault, "Merged two-stage power converter with soft charging switched-capacitor stage in 180 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1557–1567, Jul. 2012.

[17] K. Kesarwani, R. Sangwan, and J. T. Stauth, "Resonant-switched capacitor converters for chip-scale power delivery: Design and implementation," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6966–6977, Dec. 2015.

[18] C. Schaef and J. T. Stauth, "A 3-phase resonant switched capacitor converter delivering 7.7 W at 85% efficiency using 1.1 nH PCB trace inductors," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2861–2869, Dec. 2015.

[19] C. Schaef, E. Din, and J. T. Stauth, "A digitally controlled 94.8%-peak-efficiency hybrid switched-capacitor converter for bidirectional balancing and impedance-based diagnostics of lithium-ion battery arrays," in *Proc. ISSCC*, Feb. 2017, pp. 180–181.

[20] W.-C. Liu, P. Assem, Y. Lei, P. K. Hanumolu, and R. Pilawa-Podgurski, "A 94.2%-peak-efficiency 1.53 A direct-battery-hook-up hybrid Dickson switched-capacitor DC-DC converter with wide continuous conversion ratio in 65 nm CMOS," in *Proc. ISSCC*, Feb. 2017, pp. 182–183.

[21] W. Kim, D. Brooks, and G.-Y. Wei, "A fully-integrated 3-level DC-DC converter for nanosecond-scale DVFS," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 206–219, Jan. 2012.

[22] L. G. Salem and P. P. Mercier, "A single-inductor 7+7 ratio reconfigurable resonant switched-capacitor DC-DC converter with 0.1-to-1.5V output voltage range," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, San Jose, CA, USA, Sep. 2015, pp. 1–4.

[23] Y. M. Ju *et al.*, "A hybrid inductor-based flying-capacitor-assisted step-up/step-down DC-DC converter with 96.56% efficiency," in *Proc. ISSCC*, Feb. 2017, pp. 184–185.

[24] L.-C. Chu *et al.*, "A three-level single-inductor triple-output converter with an adjustable flying-capacitor technique for low output ripple and fast transient response," in *Proc. ISSCC*, Feb. 2017, pp. 186–187.

[25] C. Schaef, J. S. Rentmeister, and J. Stauth, "Multimode operation of resonant and hybrid switched-capacitor topologies," *IEEE Trans. Power Electron.*, Feb. 2018. [Online]. Available: https://ieeexplore.ieee.org/document/8293858/

[26] Y. Pascal and G. Pillonnet, "Efficiency comparison of inductor-, capacitor-, and resonant-based converters fully integrated in CMOS technology," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 5, no. 3, pp. 421–429, Sep. 2015.

[27] J. C. C. Rodriguez, M. Turhan, M. A. M. Hendrix, A. H. M. van Roermund, and E. Cantatore, "A 92.2% peak-efficiency self-resonant hybrid switched-capacitor LED driver in 0.18 μm CMOS," in *Proc. ESSCIRC*, Leuven, Belgium, 2017, pp. 344–347.

[28] *DS107 LUXEON Rebel PLUS Product Datasheet*, LX18-P150-x datasheet, Lumileds, 2017.

[29] M. Bazes, "Two novel fully complementary self-biased CMOS differential amplifiers," *IEEE J. Solid-State Circuits*, vol. 26, no. 2, pp. 165–168, Feb. 1991.

[30] S. Yuvarajan and L. Wang, "Power conversion and control using a current sensing power MOSFET," in *Proc. 34th Midwest Symp. Circuits Syst.*, vol. 1. Monterey, CA, USA, May 1991, pp. 166–169.

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