0.04-mm^2 103-dB-A Dynamic Range Second-Order VCO-Based Audio $\Sigma\Delta$ ADC in 0.13-μm CMOS

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***Abstract*— This paper presents a compact-area, low-power, highly digital analog-to-digital converter (ADC) for audio applications. The proposed converter is implemented using only oscillators and digital circuitry, without operational amplifiers nor other highly linear circuits. The ADC consists of two twin second-order $\Sigma\Delta$ modulators, which can work both individually or in a pseudodifferential configuration. The proposed system has been implemented in a 0.13-μm standard CMOS technology. The single-ended configuration occupies an active area of 0.02 mm^2, is powered at 1.8 V with a current consumption of 155 μA, and achieves an A-weighted dynamic range (DR) of 98 dB-A. The pseudodifferential configuration achieves 103 dB-A of A-weighted DR at the expense of doubling the area and power consumption.**

***Index Terms*— Analog-to-digital converter (ADC), audio, highly digital, microphones, phase-referenced integration, sigma–delta modulation, time encoding, voltage-controlled oscillator (VCO)-ADC.**

I. Introduction

THE evolution of mobile devices and the Internet of Things (IoT) during the last years has increased the interest on the development of new low-cost integrated microphones. Voice recognition has become very popular nowadays, and the trend is toward devices continuously listening and waiting for user commands. Moreover, techniques, such as background noise cancellation, require more than one microphone per device, which increases even more the demand of low-power low-cost MEMS microphones.

This kind of microphones consists of a sensing element, which is typically a variable capacitance and a readout circuit. The readout circuit measures the change in the capacitance and generates an output signal proportional to the sound pressure. The output signal can be either analog or digital. Analog microphones have been very popular during the last years because of their lower price and versatility. However, digital microphones have some advantages over analog microphones (e.g., better power supply rejection), and the trend indicates that they may gain popularity in the near future [1].

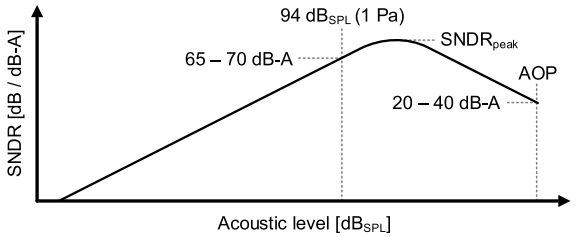

Fig. 1. Example of the SNDR for different input acoustic levels of a MEMS microphone.

The competitiveness of a microphone is given by its silicon area, power consumption, MEMS complexity (e.g., single-ended or differential), dynamic range (DR) which is typically required to be above 100 dB, and the acoustic overload point (AOP) which in most cases has to be higher than 120 dB$_{SPL}$. The signal-to-noise and distortion ratio (SNDR) of this kind of systems is typically measured using an input tone of 1 kHz and A-weighting. For very large acoustic signals, the SNDR of MEMS microphones is typically limited by distortion [2]. As shown in Fig. 1, the AOP is the maximum input level to which the distortion is acceptable, which is typically in the range between 20 and 40 dB-A (in this paper, we use 40 dB-A of signal-to-distortion ratio as the limit). Another common specification is the SNDR for an input signal of 1 Pa (94 dB$_{SPL}$), which is usually targeted above 65–70 dB-A [3].

A digital microphone typically consists of an analog microphone connected to a compact low-power analog-to-digital converter (ADC). The low bandwidth of the audible sound (20 kHz) promotes the use of oversampled converters, such as sigma–delta ($\Sigma\Delta$) modulators [4], [5]. However, the wide variety of audio codecs available in the industry hinders the standardization of the communication protocols and data rates. A typical sampling frequency for this kind of converters is between several hundreds of kilohertz and a few megahertz, which forces the $\Sigma\Delta$ to be third order or higher [6], [7] if the quantizer is single bit. Nowadays, new protocols, such as MIPI SoundWire, proposes the use of higher data rates up to a few tens of megahertz, which may enable the use of low-order $\Sigma\Delta$ converters [8].

Despite its higher power consumption, switched-capacitor (SC) $\Sigma\Delta$ values are sometimes preferred instead of continuous-time (CT) $\Sigma\Delta$ values, which are less tolerant to

Manuscript received June 22, 2017; revised September 20, 2017, November 29, 2017, and January 19, 2018; accepted January 19, 2018. Date of publication February 16, 2018; date of current version May 24, 2018. This paper was approved by Associate Editor Pietro Andreani. This work was supported in part by the European Union under Project 610484 FP7-IAPP and in part by CICYT, Spain, under Project TEC2014-56879-R. *(Corresponding author: Fernando Cardes.)*

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Digital Object Identifier 10.1109/JSSC.2018.2799938

some circuit impairments such as clock jitter [9]. However, implementing any of these topologies in modern deep submicrometer technologies is becoming challenging because of various reasons. For example, the trend to reduce the power supply voltage reduces the voltage headroom available for stacking transistors, which complicates the design of analog circuitry. Moreover, CMOS technology scaling also adversely affects the gain of the transistors. In contrast, digital circuitry benefits from transistor size and voltage supply reduction, which improves its speed and power consumption.

Time encoding is an emerging alternative to the classical voltage (or current) encoding. A time-encoding system typically uses the input signal to modulate a timing characteristic of a carrier signal (for example, its frequency, phase, period, duty cycle, delay, and so on). One of the most used building blocks is the voltage-controlled oscillator (VCO), which combined with digital circuitry can operate as a time-domain integrator. For example, a VCO can work as the quantizer of a traditional converter [10]–[12]. A VCO can also be used as the first stage of an ADC of different orders of noise shaping [13]–[20]. Finally, various VCOs can be connected together to create more complex converters with higher order noise shaping [21], [22]. In [22], a third-order $\Sigma\Delta$ modulator is built combining two oscillators with an analog integrator, a quantizer, and various feedback DACs. In [21], in contrast, the possibility of implementing an ADC based on VCOs only is proposed. Subsequent publications [23], [24] have built up theoretical background around this idea. Later, [25] proposed a generic approach to VCO-based analog filters, including CT-$\Sigma\Delta$ filter loops. Last, in [26], these architectures have been implemented with a wide bandwidth and medium DR target. One of the main drawbacks of VCO-based converters is the distortion injected by VCOs for very large input signals, which frequently implies the need for nonlinearity correction techniques [26]–[29].

In this paper, we demonstrate the application of VCO-ADCs to low-power sensor applications, such as MEMS microphones. We propose a compact VCO-based second-order $\Sigma\Delta$ modulator implemented without operational amplifiers. The converter consists of two single-ended branches which can be combined in a pseudodifferential architecture, making it compatible with both single-ended and differential MEMS microphones. In both configurations, the levels of distortion achieved are within the range commonly accepted in audio applications without the need for any linearity correction. The converter has been implemented in the 0.13-μm CMOS, with an active area of 0.04 mm^2 and a current consumption of 300 μA at 1.8 V. Measurements show (after A-weighting) that the DR obtained is 103 dB, and the AOP is above 125 dB$_{\mathrm{SPL}}$.

This paper is organized as follows. Section II describes how VCOs and digital counters can be used to replace analog integrators, and proposes the architecture of a second-order $\Sigma\Delta$ modulator based on oscillators. Section III gives the details about the implementation of the system at the transistor level, and Section IV shows the measurements obtained from the experimental integrated circuit. Finally, Section V concludes this paper.

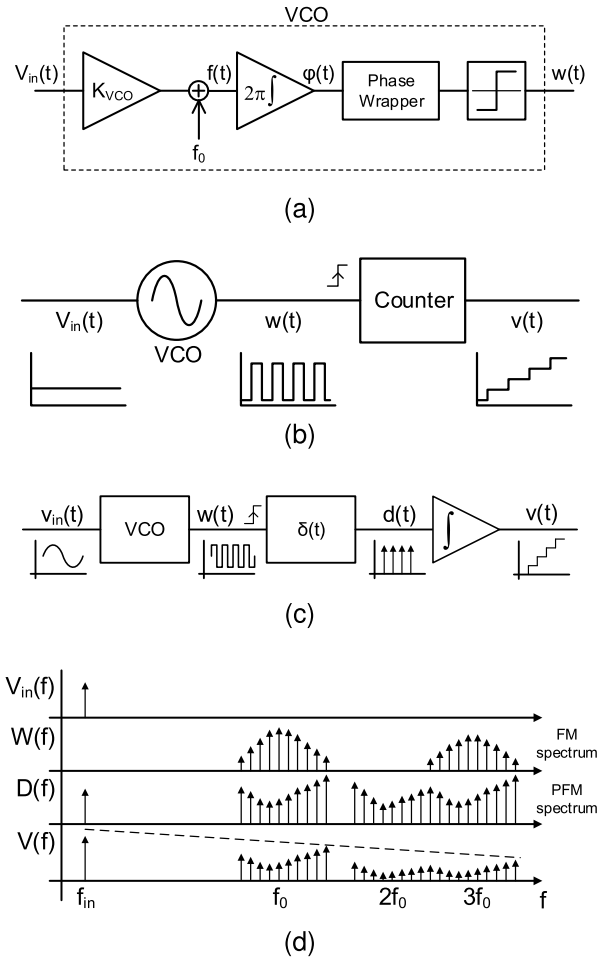

Fig. 2. (a) Classical model of a VCO as a phase integrator. (b) VCO and counter working as an integrator. (c) PFM-based model of a VCO and a counter operating as an integrator. (d) Spectra of the state variables of (c).

II. Proposed Architecture

A. Phase-Referenced Integration

Fig. 2(a) shows the typical way to model a VCO as a phase integrator [30], where V_{in} is the input of the VCO, K_{VCO} is the VCO gain, f_0 is the central oscillation frequency, $f(t)$ is the instantaneous oscillation frequency, $\varphi(t)$ is the phase of the oscillator, which is the result of integrating $f(t)$, and $w(t)$ is the square output signal, which is the result of wrapping the phase and passing it through a comparator. A counter can be used to perform the unwrapping and obtain $v(t)$, which is the integral of the input signal $V_{\mathrm{in}}(t)$ approximated as a staircase, as shown in Fig. 2(b).

An equivalent way to model a VCO followed by a counter is depicted in Fig. 2(c). In this equivalence, the counter is modeled as an edge detector ($\delta(t)$) followed by an integrator. Fig. 2(d) shows the spectra of the state variables of this model. The input signal $V_{\mathrm{in}}(f)$ is a Dirac delta at frequency f_{in}, assuming a sinusoidal input. The oscillation $W(f)$ is a square signal, which shows frequency modulation (FM). The output of the edge-detector is an impulse train which shows pulse FM (PFM), as described in [25], [31], and [32]. Finally, the output of the integrator is the same staircase as the

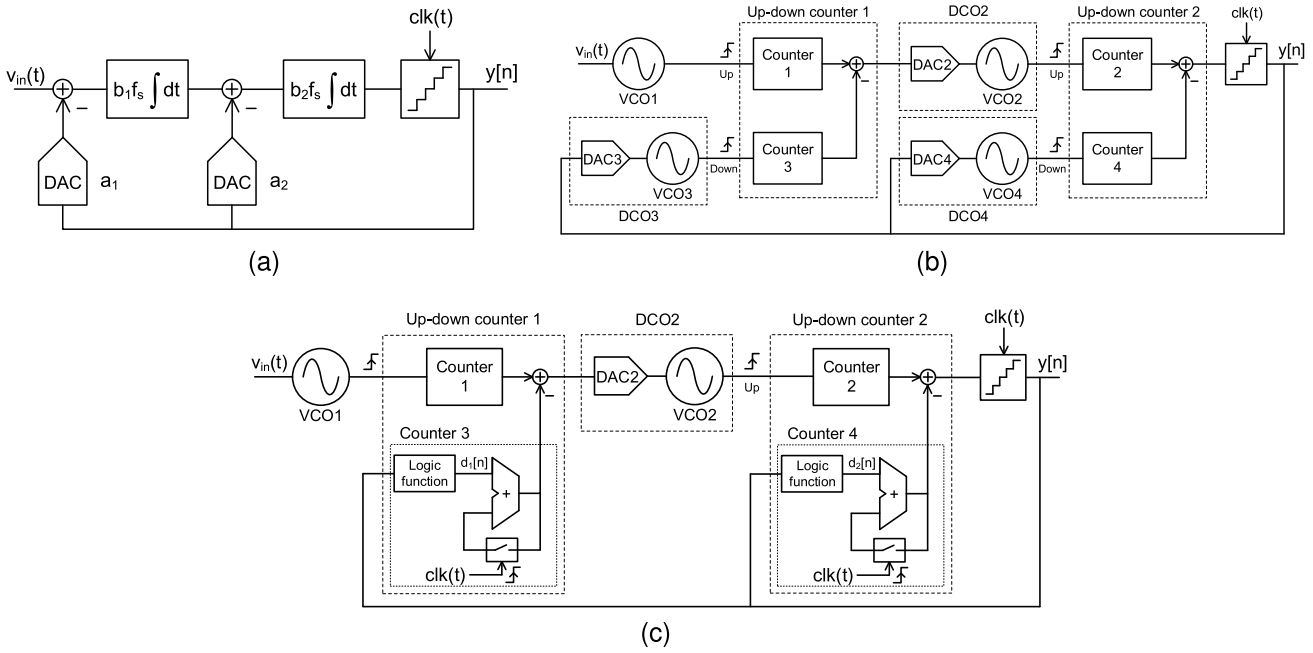

Fig. 3. (a) Classical second-order $\Sigma\Delta$ modulator. (b) Implementation of the same system using oscillators and counters. (c) Simplification of the system using discrete-time feedback integrators.

one obtained in Fig. 2(b), whose spectrum $V(f)$ contains the input signal and the harmonics of the PFM attenuated by the integration. We name "phase-referenced integrator" (PRI), the counter that performs the edge detection and the integration.

We can use this equivalence to transform integrator-based systems into oscillator-based systems. For example, the second-order $\Sigma\Delta$ modulator depicted in Fig. 3(a) can be built using only oscillators and digital circuitry, as shown in Fig. 3(b).

In this example, the first integrator is performed by VCO1-Counter 1, which integrates the input signal, and DCO3-Counter 3 [digitally controlled oscillator (DCO)], which integrates the feedback signal. Note that Counters 1 and 3 (and similarly Counters 2 and 4) can be combined within an up–down counter whose value is increased and decreased, respectively, by VCO1 and DCO3. Similarly, the second integration is performed by DCO2-Counter 2 and DCO4-Counter 4. In order to obtain equivalent systems, the sensitivity of these oscillators must be chosen not to alter the gain of any branch of the system

$$K_{\mathrm{VCO1}} \cdot K_{\mathrm{DCO2}} = b_1 \cdot b_2 \cdot f_s^2 \tag{1}$$

$$K_{\mathrm{DCO3}} \cdot K_{\mathrm{DCO2}} = a_1 \cdot b_1 \cdot b_2 \cdot f_s^2 \tag{2}$$

$$K_{\mathrm{DCO4}} = a_2 \cdot b_2 \cdot f_s. \tag{3}$$

The main difference between the original system depicted in Fig. 3(a) and the VCO-based equivalent of Fig. 3(b) relies on the presence of the PFM harmonics described before, which may degrade the performance of the converter. In general, increasing the oscillation frequency is an effective way to reduce the power of the harmonics.

The number of oscillators used in Fig. 3(b) can be reduced modifying the system, as shown in Fig. 3(c). In this variant, oscillators 3 and 4 are removed, and counters 3 and 4 are transformed into digital discrete-time integrators. Therefore, the value of each "up–down counter" is increased by one on each oscillation rising edge, and on each sampling instant is decreased by a value that depends on the feedback. Note that this causes that the decrements produced in the outputs of the counters are independent of the duration of the sampling period. Therefore, this topology presents better tolerance to clock jitter. The relationship between the modulator output and the value subtracted to each up–down counter is determined by two logic functions, which generate signals $d_1[n]$ and $d_2[n]$ according to the following equations:

$$d_1[n] = d_{1_{\mathrm{Offset}}} + y[n] \cdot g_{d1}, \quad g_{d1} = \frac{K_{\mathrm{DCO3}}}{f_s} \tag{4}$$

$$d_2[n] = d_{2_{\mathrm{Offset}}} + y[n] \cdot g_{d2}, \quad g_{d2} = \frac{K_{\mathrm{DCO4}}}{f_s} \tag{5}$$

where K_{DCO3} and K_{DCO4} are calculated according to (1)–(3). Note that the offset components ($d_{1_{\mathrm{Offset}}}$ and $d_{2_{\mathrm{Offset}}}$) affect the dc values of different signals of the system, but they do not modify the position of the poles or the zeros of the modulator.

B. VCO-Based Second-Order $\Sigma\Delta$ Modulator

Fig. 4 depicts a VCO-based second-order $\Sigma\Delta$ modulator based on the equivalence explained in Section II-A, specifically in the architecture shown in Fig. 3(c). The system proposed consists of two twin modulators which can work both independently or in a pseudodifferential configuration. In this design, we have decided to use a single-bit quantizer to comply with the standard digital interfaces of digital MEMS microphones. The interconnection between the integrator stages of the $\Sigma\Delta$ modulator could be multi-bit as in [26]. A multi-bit interstage connection helps in wide bandwidth applications,

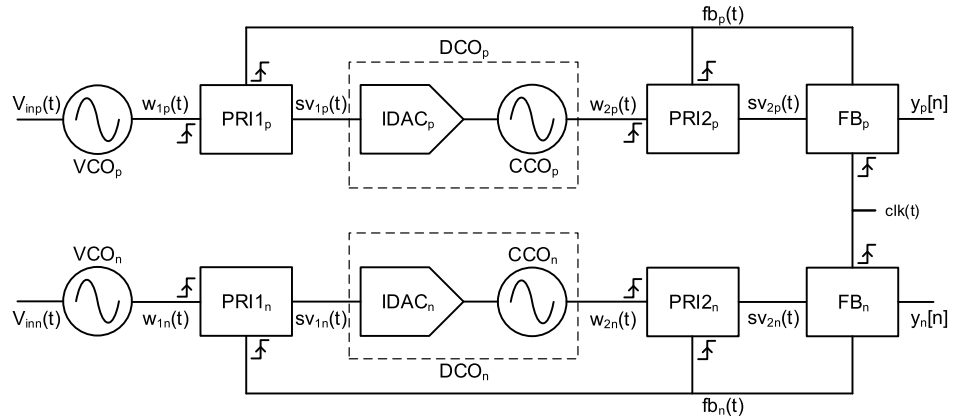

Fig. 4. Proposed pseudodifferential second-order VCO-based $\Sigma\Delta$ modulator.

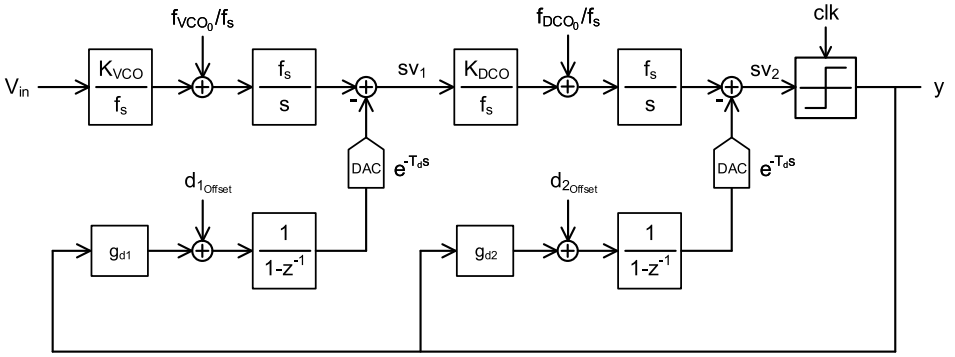

Fig. 5. Model of the proposed VCO-ADC with a linearized loop filter.

where the speed of the DACs is a limiting factor due to the high sampling rates. However, such multi-bit implementation would not be as efficient in power and area as a single-bit interstage connection, which reduces the complexity of the DACs and the counters of Fig. 3(c). The sampling rate chosen in this chip is 20 MHz, which is sufficiently low to ensure proper operation with a single-bit interconnection and enables this solution to be competitive against SC $\Sigma\Delta$ modulators. However, this decision reduces the range of oscillation frequencies suitable to build the modulator. In the following paragraphs, we describe one of the single-ended modulators.

The input voltage controls the oscillation frequency of the VCO, whose output is the FM signal $w_1(t)$. The center oscillation frequency is $f_0 = 4.8$ MHz, and the oscillator gain is $K_{\text{VCO}} = 7.2$ MHz/V (the relative frequency deviation is $k_d = K_{\text{VCO}}/f_0 = 1.5\ \text{V}^{-1}$). Assuming a maximum input swing of ± 320 mV (for 125 dB_{SPL}), the oscillation frequency falls, then, within the range of 2.5 MHz–7.1 MHz. PRI1 is a 1-bit up–down counter, whose value is increased on each rising edge of $w_1(t)$ and decreased on each rising edge of the feedback, fb(t). The output of this PRI is fed into the second stage, which consists of a DCO and a second PRI. The DCO consists of a current DAC (IDAC) followed by a current-controlled oscillator (CCO). The CCO can oscillate at only two different frequencies: $f_{\text{low}} = 2.5$ MHz when PRI1 is "0" and $f_{\text{high}} = 9.5$ MHz when PRI1 is "1." Therefore, we can define the sensitivity of the DCO as $K_{\text{DCO}} = 7$ MHz/code. Finally, the output of PRI2 is sampled by the subcircuit FB, which also generates the feedback pulse fb(t).

This set of parameters has been chosen with two goals. On one hand, these parameters must be chosen to place the poles and the zeros in the correct position to achieve the target noise transfer function and signal transfer function. Fig. 5 describes a simplified model of the VCO-ADC shown in Fig. 3(c) based on the equivalence presented in Fig. 2. A delay (T_d) has been introduced to model the time that the counter requires to update its value after the clock edge. This diagram also illustrates the correspondence between the parameters of the VCO-based system and the coefficients of the classical $\Sigma\Delta$ modulator of Fig. 3(a). On the other hand, the appropriate selection of frequencies is required to avoid the saturation of the 1-bit PRIs. The oscillation frequencies of both oscillators must be lower than the sampling frequency in order to avoid that two rising edges of the same oscillator are produced before a feedback pulse is generated to reset the PRIs. In addition, given that a rising edge of the DCO is required to generate the feedback pulse, f_{high} must be kept above the maximum oscillation frequency of the VCO.

Fig. 6 illustrates the behavior of one of the channels of this VCO-ADC with the set of parameters proposed, assuming $T_d = 0$. At instant t_1, the rising edge in $w_1(t)$ sets the output of the PRI1 ($\text{sv}_1(t)$) to "1." When this happens, the frequency of the DCO changes from f_{low} to f_{high}, so its phase ($\varphi_{\text{DCO}}(t)$) climbs at higher rate. At t_2, this phase reaches 2π, which

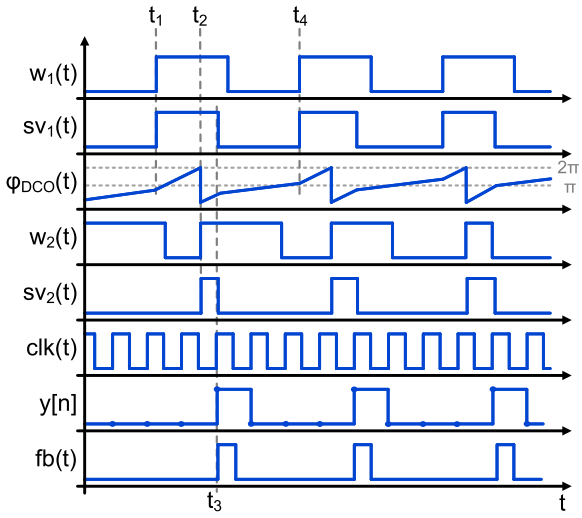

Fig. 6. State variables of one of the branches of Fig. 4.

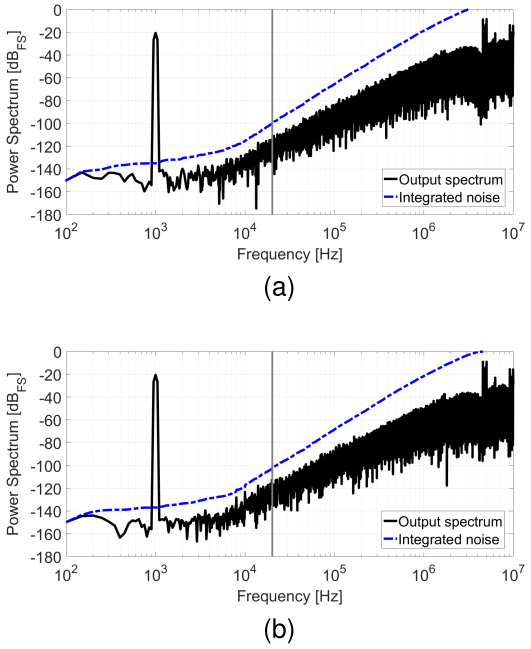

Fig. 7. Simulated spectra for an input signal of -20 dB$_{\mathrm{FS}}$ at 1 kHz. (a) Single-ended converter. (b) Pseudodifferential converter.

generates a rising edge on $w_2(t)$, and therefore, $\mathrm{sv}_2(t)$ is set to "1." At t_3, the rising edge of the clock clk samples for first time when $\mathrm{sv}_2(t) = 1$, generating a short pulse in $\mathrm{fb}(t)$ which clears both PRIs. This sets the oscillation frequency of the DCO back to f_{low} until t_4, the next rising edge of $w_1(t)$.

Figs. 7 and 8 show the result of behavioral simulations of the proposed system implemented with ideal oscillators for two different input signals. The second-order noise shaping is clearly visible in both single-ended and pseudodifferential configurations. Simulations shown in Fig. 7 have been computed applying a -20 dB$_{\mathrm{FS}}$ input tone at 1 kHz. The SNDR obtained in the single-ended converter [see Fig. 7(a)] in 20 kHz (audio bandwidth) is 81.4 dB, which increases up to 88 dB-A using A-weighting. In the case of the pseudodifferential converter

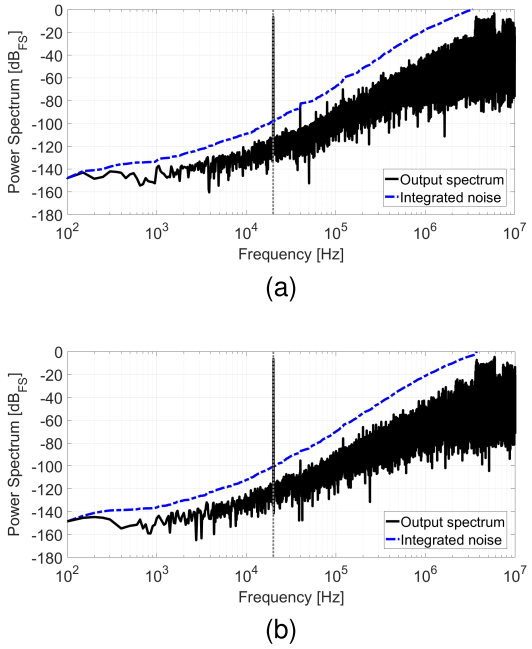

Fig. 8. Simulated spectra for an input signal of -6 dB$_{\mathrm{FS}}$ at 20 kHz. (a) Single-ended converter. (b) Pseudodifferential converter.

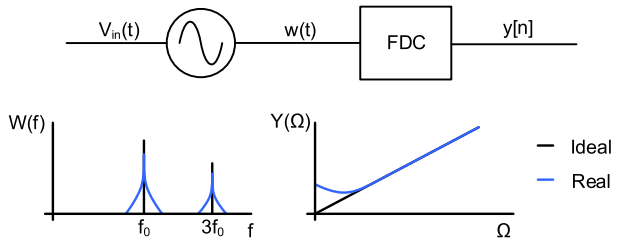

Fig. 9. Effect of phase noise in the output spectrum of a VCO-ADC.

[see Fig. 7(b)], the SNDR is 83.8 dB (90.4 dB-A). Fig. 8 shows the simulated spectra of both configurations for a -6 dB$_{\mathrm{FS}}$ and 20-kHz input tone. The SNR obtained from these simulations is, respectively, 93.3 and 95.9 dB.

C. Influence of Nonidealities

The VCO of the first stage performs the voltage-to-frequency conversion, which is the ultimate limit of the resolution of the ADC. The oscillation frequency of an ideal VCO would have a linear and deterministic relationship with the input voltage. However, any VCO implementation suffers from two important nonidealities: phase noise and distortion. Phase noise is the result of the modulation of the electrical noise generated by the components that make up the circuit. This noise is modulated by the oscillation, and appears in the spectrum of $w(t)$ around the oscillation frequency and its harmonics [33]. In a VCO-based ADC, this noise is down-converted by the frequency-to-digital converter, and it is visible at the output of the modulator $y[n]$, as shown in Fig. 9. This limits the resolution of the converter, especially at low input levels [34]–[36].

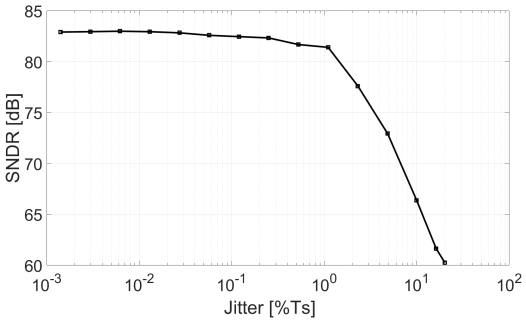

Fig. 10. Simulated SNDR at -20 dB_{FS} for different values of clock jitter standard deviation referred to the ideal sampling period.

Phase noise is very dependent on the topology of oscillator, and it has been shown that an *LC* oscillator typically exhibits much lower phase noise than other CMOS oscillators [37]. However, given that an integrated coil requires too much area in modern technologies, other alternatives, such as ring oscillators, are frequently preferred. Furthermore, the phase noise of a ring oscillator depends on many factors, such as the oscillation amplitude, the current consumption, the number of stages, the area of the transistors, or the symmetry between rising and falling edges [38]–[40]. It should not be forgotten that the maximum SNR of a VCO also depends on the sensitivity of the oscillator. A high sensitivity, however, may worsen the linearity of the VCO for large input signals, and the distortion caused by the nonlinear relationship between the oscillation frequency and the input voltage may become the limiting factor. An important advantage of the pseudodifferential configuration compared with the single-ended configuration is the cancellation of the even harmonics of the distortion. The second oscillator also exhibits phase noise, although its impact on the performance of the system is negligible because of two reasons. On one hand, the frequency variation of the DCO is much larger than in the case of the VCO. Therefore, small frequency variations caused by noise are in comparison smaller. Furthermore, the DCO is in the middle of the filter loop, and errors injected at this point are high-pass filtered by the loop.

Another important nonideality that must be considered is the jitter of the sampling clock, which is the random variation of the sampling period. Jitter is another manifestation of the same phenomenon as phase noise, but it is measured referring the standard deviation of the period to its average duration. The influence of jitter in the performance of CT $\Sigma\Delta$ converters has been extensively studied in the literature [41], [42]. As explained earlier, in this VCO-based $\Sigma\Delta$ modulator, the integration of the feedback is done in discrete time, which shows better tolerance to clock jitter than classical CT $\Sigma\Delta$ with CT feedback integration. Fig. 10 shows the SNDR of the proposed system at -20 dB_{FS} for different values of clock jitter. It can be observed that the SNDR is almost constant up to a jitter standard deviation of 1% of the ideal sampling period (*Ts*).

Finally, metastability may be a problem in the digital circuitry. On one hand, both PRIs have two inputs: the feedback pulse which is synchronized with the sampling clock and the oscillation which is asynchronous. The potential conflict arises when a rising edge happens in both inputs almost simultaneously. The PRI must be capable of handling this situation (at least in the wide majority of the cases), so both edges are properly taken into account. On the other hand, the feedback generator also has two inputs: the sampling clock and the output of the PRI2 whose rising edges are asynchronous, while the falling edges are synchronized with the feedback pulse and, therefore, with the sampling clock.

III. Circuit Design

A. Voltage-Controlled Oscillator

As stated before, the VCO of the first stage deserves special attention, because it performs the critical voltage-to-frequency conversion of the input signal, which sets the limit in the maximum achievable resolution of the ADC. Fig. 11 shows the proposed VCO, which is composed of a three-stage single-ended voltage-controlled ring oscillator followed by a buffer and a level shifter. The biasing circuitry required to interface the MEMS and drive the VCO has not been included in this test chip, and the voltage produced by the MEMS has been emulated externally using a signal generator, as explained in Section IV. Ring oscillators are widely used in VCO-ADCs [12], [16], [26] due to their sensitivity and low phase noise. Another advantage of these oscillators is that they can be used in multi-bit configurations using the multiple phases of the ring. However, given that our priority is simplifying the digital circuit that follows the oscillator, we only use one of the outputs of the ring oscillator. The VCO has been designed using periodic-steady-state simulations and *pnoise* analysis to estimate the oscillation frequency, sensitivity, phase noise, and distortion. These simulations have been combined with an optimization algorithm to find a suitable VCO in terms of SNDR, area, and power consumption. The PMOS transistors of the ring oscillator (M_1–M_3) are W/L $=$ 72 μm/8 μm, whereas the NMOS (M_4–M_6) are W/L $=$ 48 μm/8 μm. With these dimensions, the target oscillation frequency and gain ($f_0 = 4.8$ MHz and $K_{VCO} = 7.2$ MHz/V) are reached when the dc input voltage is 1.1 V for nominal conditions. However, temperature and process variations alter the oscillation frequency for a given dc input voltage. Monte Carlo simulations show that the standard deviation of the oscillation frequency at 1.1 V is approximately 250 kHz. Very high oscillation frequencies may result in the saturation of PRI1 for high input levels. In contrast, lower oscillation frequencies imply lower VCO sensitivity, which attenuates the input signal (see Fig. 5). Moreover, lowering the VCO frequency increases the power of PFM harmonics, which may degrade the performance of the modulator. System-level simulations have been used to check that the converter tolerates a variation of ± 1 MHz (4σ) without significant loss of performance.

One of the phases of the ring oscillator (ϕ_1) is taken as the main output, and it is connected to a chain of inverters to square the oscillation. The amplitude of this oscillation depends on the supply of the inverters, so a level shifter is required to obtain an oscillation level compatible with the digital circuitry whose supply voltage is 1.8 V. The other two

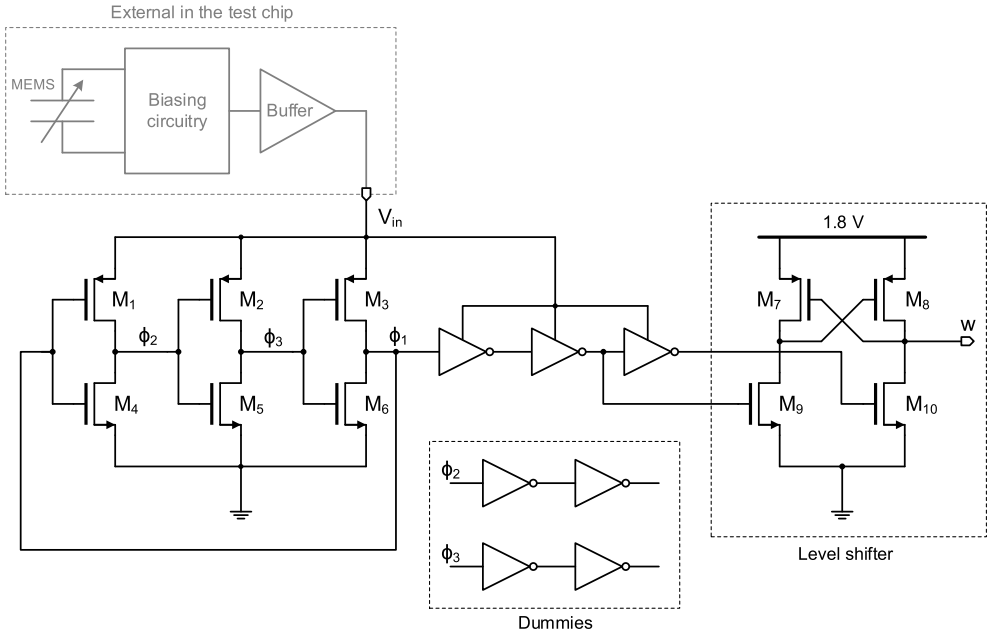

Fig. 11. Proposed three-stage single-ended voltage-controlled ring oscillator.

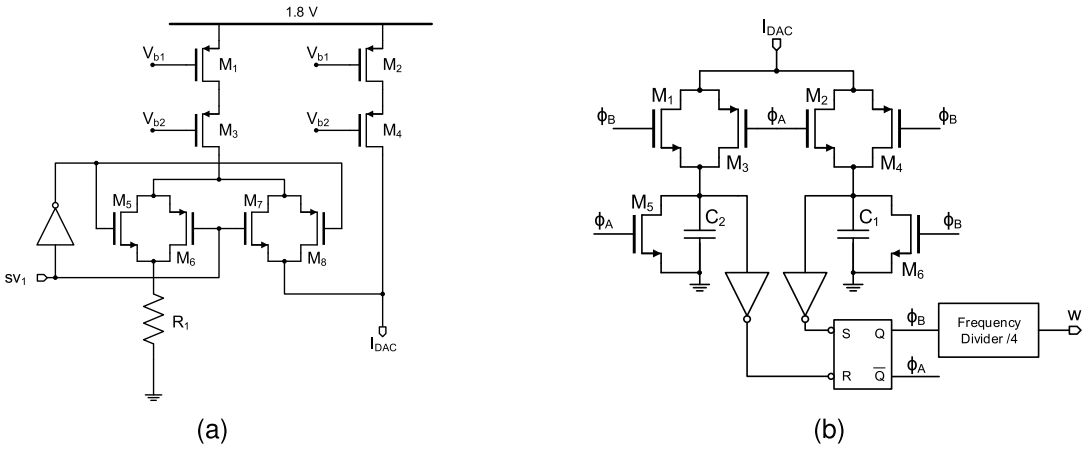

Fig. 12. Proposed DCO. (a) 1-bit IDAC. (b) CCO.

outputs of the ring oscillator, ϕ_2 and ϕ_3, are connected to dummy inverters in order to maintain the symmetry of the oscillator. The current consumption of the VCO (including inverters and level shifter) is 75 μA at the center frequency.

B. Digitally Controlled Oscillator

The DCO of the second stage can oscillate only at $f_{\text{low}} \approx 2.5$ MHz or $f_{\text{high}} \approx 9.5$ MHz, which has two interesting features: first, the oscillator is intrinsically linear, because it can only oscillate at two different frequencies and secondly, given that these two frequencies are very different, the error introduced by random phase fluctuations (including power supply noise and the intrinsic phase noise of the oscillator) is in comparison small, and has less impact on the resolution of the ADC. Moreover, errors introduced after the first integrator (VCO1) are high-pass filtered due to the system loop. However, given that the output of the first PRI consists of pulses which can be very short, the voltage-to-frequency response of the DCO must be fast enough to properly respond to these pulses, as shown in Fig. 6. Among others possibilities, one solution is the combination of a 1-bit IDAC followed by the CCO shown in Fig. 12. This oscillator topology can respond to very short input pulses and, in contrast to a ring oscillator, it generates a rail-to-rail output without the need for a level shifter.

The IDAC of Fig. 12(a) has a current source (M_2 and M_4), which drives 5 μA into the output. In addition, another current source (M_1 and M_3) generates 15 μA, which is routed through an analog multiplexer (M_5–M_8). When the control signal sv_1 is low, this current is thrown away through the resistor R_1 to maintain the current source properly biased. When sv_1 is high, the current is added to the output, so the total output current is 20 μA.

The CCO, shown in Fig. 12(b), is a relaxation oscillator in which two capacitors are alternately charged and discharged.

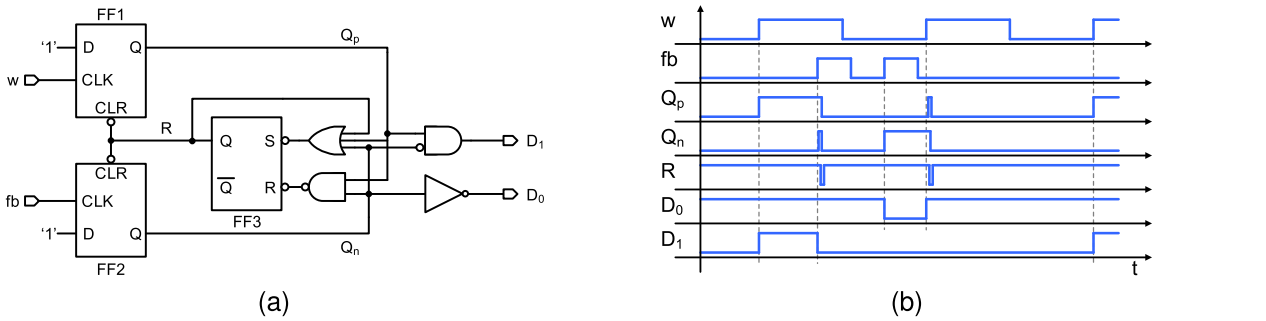

Fig. 13. Proposed 1-bit PRI. (a) PRI diagram. (b) PRI behavior.

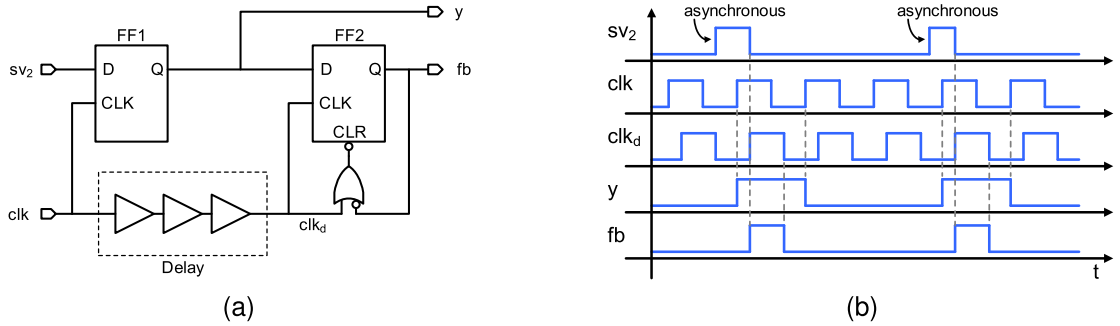

Fig. 14. Proposed feedback generator. (a) Feedback generator schematic. (b) Feedback generator behavior.

When $\phi_A = \overline{\phi_B} = 1$, the current provided by the IDAC is used to charge the capacitor C_1 through M_2 and M_4, while C_2 is cleared by M_5. When the voltage of C_1 reaches the threshold voltage of the inverter to which it is connected (approximately 0.9 V), the set-reset flip-flop is toggled, and capacitors C_1 and C_2 exchange roles. Using the capacitors of 250 fF, the oscillation frequencies obtained are $f_{\text{low}} \approx 10$ MHz and $f_{\text{high}} \approx 38$ MHz, which have been divided by four with a frequency divider composed of two T-type flip-flops in cascade to obtain the target values. The total current consumed by the DCO, taking into account the biasing circuit and the digital circuitry, is 55 μA.

C. Digital Circuitry

Apart from the two oscillators described in Sections III-A and III-B, each single-ended branch requires two PRIs and a feedback generator. The schematic of the PRIs is shown in Fig. 13(a).

It can be observed that it is, in essence, similar to the phase and frequency comparator that can be found in phase-locked loops. Two D-type flip-flops FF1 and FF2 are set to "1" by rising edges on inputs w and fb, respectively. When both flip-flops are "1," FF3 resets the flip-flops, as shown in Fig. 13(b). This circuit behaves as a two-bit up/down counter whose output is a thermometric code. As stated in Section II, with the set of frequencies chosen, the counter only needs 1 bit, and therefore, output "D_0" has not been used. System-level simulations have been run to check that neither of the PRIs gets saturated for any input level in the range of interest. This is similar to the simulations that are run in classical CT-$\Sigma\Delta$ modulator to estimate the size of the state variables. A potential source of errors is related to the pulse generated by FF3 to reset the other two flip-flops.

While this signal is active (low), neither FF1 nor FF2 can react to rising edges on their respective clock input ports. The duration of this pulse is set by the logic circuit that accompanies FF3, which ensures that the pulse is long enough to reset both FF1 and FF2. Circuit-level simulations show that the duration of this pulse is between 600 ps and 1.4 ns, depending on temperature and process variations. System-level simulations show that the errors caused by receiving a rising edge while flip-flops are being reset is not a significant noise source compared to other dominant noise sources, such as the phase noise of the first oscillator.

The feedback generator is depicted in Fig. 14(a). The first flip-flop (FF1) samples the output of the PRI2 (sv_2) and generates the output bitstream (y). The second flip-flop (FF2) samples the output with the clock delayed about 2 ns (clk_d), and sends a pulse through fb every time it samples "1." Note that this delay of 2 ns corresponds to the parameter T_d of Fig. 5. Fig. 14(b) describes the behavior of this circuit. In this case, FF1 may be sensitive to metastability, because sv_2 and clk are not synchronized. However, the delay between clk and clk_d ensures that signal y is stable before it is sampled by FF2, so metastability errors are improbable. This has been checked by extensive circuit-level simulation.

IV. Experimental Results

The proposed second-order VCO-based $\Sigma\Delta$ modulator has been fabricated in the 130-nm standard CMOS, resulting in the integrated circuit shown in Fig. 15. Each single-channel

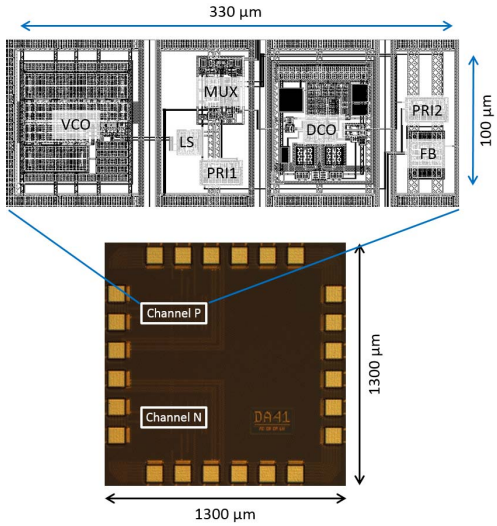

Fig. 15. Die micrograph with dimensions.

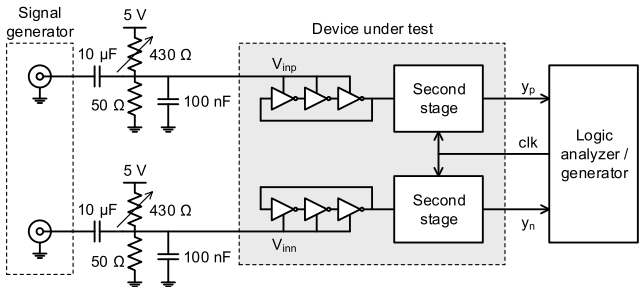

Fig. 16. Test fixture used for all the measurements.

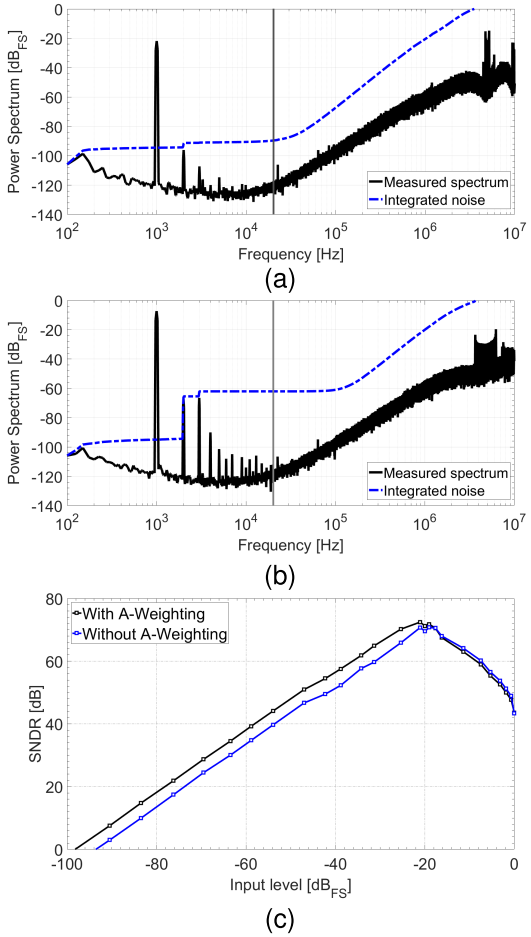

Fig. 17. Measurements of the single-ended configuration. (a) Measured spectrum at -20 dB$_{FS}$. (b) Measured spectrum at -5.5 dB$_{FS}$. (c) Measured SNDR for different input levels.

modulator is laid out over the white rectangles marked in the die photograph, which have a size of 330 μm $\times$ 100 μm. This area includes supplementary circuitry for testing purposes, but the active area of the chip occupies 0.02 mm^2 for each single-channel modulator and 0.04 mm^2 for the pseudodifferential converter. Each channel has a pad for the input voltage, another for the output data bitstream, and two multiplexed digital test pads to monitor internal signals, such as the outputs of the oscillators and the PRIs.

The measured oscillation frequency for a 1.1 V of input dc voltage was slightly below the values obtained by simulation, and we had to increase the dc level to 1.16 V in order to reach the nominal center oscillation frequency and oscillator gain (4.8 MHz and 7.2 MHz/V, respectively). The digital test pads allow to measure the oscillation frequencies of the DCO, which are $f_{\text{low}} \approx 2.5$ MHz or $f_{\text{high}} \approx 9.5$ MHz.

The performance of the ADC has been measured by adding a 1-kHz tone through a coupling capacitor to the required 1.16-V dc level generated using potentiometers at the input of the converter, as depicted in Fig. 16.

Fig. 17 shows the measured performance of the proposed ADC in the single-ended configuration. The spectrum of Fig. 17(a) has been measured applying an input signal of 32 mV$_{\text{peak}}$ (-20 dB$_{\text{FS}}$). The SNDR obtained is 69.6 dB and 71.2 dB-A when A-weighting is applied. Fig. 17(b) shows the measured spectrum for an input signal of -5.5 dB$_{\text{FS}}$, on which the VCO nonlinearity limits the SNDR to 56.6 dB (55.4 dB-A). In Fig. 17(c), we can observe the SNDR measured for different input levels, referred to the input full scale (320 mV$_{\text{peak}}$). The DR obtained without and with A-weighting is 93.5 dB and 98 dB-A, respectively. The current consumption of this converter is 155 μA powered at 1.8 V.

At the cost of doubling the power and the area, the pseudodifferential configuration has a superior performance, as shown in Fig. 18. The SNDR at -20 dB$_{\text{FS}}$ (64 mV$_{\text{peak}}$) calculated from the spectrum of Fig. 18(a) is 76.7 dB (78.9 dB-A). Fig. 18(b) depicts the measured spectrum at -5.5 dB$_{\text{FS}}$, on which the SNDR obtained is 59.2dB (58 dB-A). The DR is also extended to 98.5 dB (103 dB-A), as can be observed in Fig. 18(c). As expected, the even harmonics produced by the nonlinearities of the input VCO are canceled because of the differential operation. However, the SNDR for large input signals is still limited by the distortion of the VCOs. Nevertheless, the linearity achieved in both configurations is above 40 dB-A of SNDR for the maximum input level, making them suitable for low-cost microphones [1], [2] without the need for linearity compensation circuits.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR ART

Parameter	This work		[4]	[6]	[5]	[43]	[8]	[44]	[45]
Tech. [nm]	**130**		180	160	180	40	28	160	180
Supply Voltage [V]	**1.8**		1.8	1.6	1.8	2.5/1.2	3.3/1	1.8	5/1.8
BW [kHz]	**20**		20	20	24	24	24	20	20
F_S [MHz]	**20**		2.4	3	6.144	6.5	24	11.29	2.56
$SNDR_{peak}$ [dB]	**69.6**	**76.6**	80	91.3	98.2	90	98.5	103	99.3
DR [dB]	**93.5**	**98.5**	96	103.1	103	102	100.6	109	101.3
$DR_{A\text{-}weighted}$ [dB]	**98**	**103**	-	106	-	-	-	-	-
Power [mW]	**0.28**	**0.56**	0.73	0.39	0.28	0.5	1.13	1.12	1.1
FoM_S [dB]	**172**	**174**	170.4	180	182.3	179	173.8	181.5	173.9
Area [mm^2]	**0.02**	**0.04**	0.4	0.21	1.25	0.05	0.022	0.16	0.38

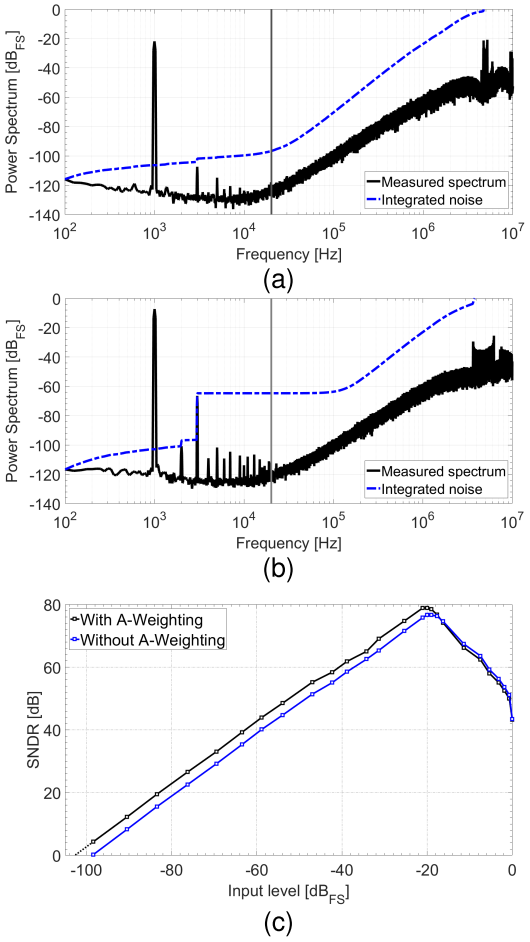

Fig. 18. Measurements of the pseudodifferential configuration. (a) Measured spectrum at -20 dB_{FS}. (b) Measured spectrum at -5.5 dB_{FS}. (c) Measured SNDR for different input levels.

It can be observed that, in addition to the even harmonics compensation, the differential configuration also reduces the low frequency noise that is visible in Fig. 17(a) below 1 kHz. This noise comes from the coupling of power supply noise to the input of both VCOs through the off-chip common-mode generator that produces 1.16 V. As this noise is added directly to both inputs, the single-ended configuration is very sensitive to power supply noise, whereas in the differential configuration, it is attenuated by the common-mode rejection

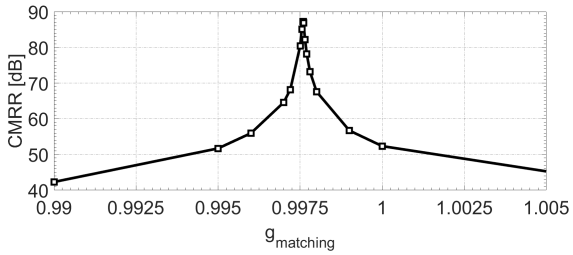

Fig. 19. CMRR for different mismatch gain correction factors.

ratio (CMRR). We have measured this ratio by connecting the input of both channels to a 100-mV_{pp} sine wave at 1 kHz and quantifying the attenuation observed at the differential output. The resulting CMRR is 52.3 dB, which can be improved by enhancing the matching between both VCOs, as shown in Fig. 19. In this graph, we display the CMRR obtained for different values of the correction factor g_{matching}, which has be used to calculate the output sequence as follows: $y_{\text{diff}}[n] = y_p[n] \cdot g_{\text{matching}} - y_n[n]$. It can be observed that the CMRR can reach above 87 dB with the appropriate matching between the two VCOs.

The achieved Schreier figure-of-merit (FoM), which is defined as $\text{FoM}_S = \text{DR} + 10\log_{10}(\text{BW}/P)$ [46], is 172 dB for the single-ended modulator and 174 dB for the pseudodifferential converter. Note that these calculations consider the current consumption of all the oscillators. Table I shows a summary of the key parameters obtained in this paper in comparison with the result of other audio converters reported in the last years. While the measured DR and FoM values are in par with other works, the area occupied by our design is significantly smaller than most of them. The only papers in this selection with similar areas are [8] and [43], which were implemented in much modern technologies (40 and 28 nm, respectively).

V. CONCLUSION

This paper presents a second-order VCO-based $\Sigma\Delta$ modulator for audio applications. The ADC is aimed for low-cost application, on which silicon area reduction is priority. The converter proposed consists of oscillators and digital circuitry, without the need of any operational amplifier nor highly linear circuits. It can work both as a single-channel converter and in a pseudodifferential configuration, occupying, respectively,

0.02 and 0.04 mm^2 in the 0.13-μm CMOS technology. The single-channel system reaches 71.2 dB-A of peak SNDR, 98 dB-A of DR, and 155 μA of current consumption. The pseudodifferential system has 78.9 dB-A of peak SNDR and 103 dB-A of DR, and it consumes 310 μA.

ACKNOWLEDGMENT

The authors would like to thank C. Perez from the Carlos III University of Madrid and B. Kuttin from Infineon Technologies Austria AG for their help.

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