

An EEG-NIRS Multimodal SoC for Accurate Anesthesia Depth Monitoring

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Abstract—In surgical operation environments, anesthesia enables doctors to safe and accurate medical process with minimized movement and pain of patients. In general anesthesia, non-invasive and reliable monitoring of anesthesia depth is required because it is directly related to patient's life. However, the current anesthesia depth monitoring approach, bispectral index (BIS), uses only electroencephalography (EEG) from the frontal lobe, and it shows critical limitations in the monitoring of anesthesia depth such as signal distortion due to electrocautery, electromyography (EMG) and dried gel, and false response to the special types of anesthetic drugs. In this paper, a multimodal head-patch system that simultaneously measures EEG and near-infrared spectroscopy (NIRS) on the frontal lobe is proposed. For EEG monitoring, mixed-mode dc-servo loop is proposed to cancel out the $\pm 300\text{-mV}$ electrode-dc offset for dried gel condition with 3.59 noise-efficiency factor. To compensate the electromagnetic noises (EMG and electrocautery) in the system level, NIRS signal is measured. Logarithmic transimpedance amplifier (TIA) and closed-loop controlled (CLC) NIRS current driver are proposed. Logarithmic TIA can reject ambient light up to 10 nA to achieve a 60-dB dynamic range. According to the comparator output, CLC NIRS driver duty cycle can be adjusted from 0.625 ms to 50 ms adaptively. The 16-mm² system-on-chip is fabricated in 65-nm CMOS. It dissipates 25.2-mW peak power. With the combined signals, it can show the clinically important transition from the awake to deep state, but BIS cannot detect the transition in a clinical trial.

Index Terms—Anesthesia depth monitoring, electroencephalography (EEG) instrumentation amplifier (IA), multimodal system-on-chip (SoC), near-infrared spectroscopy (NIRS) transimpedance amplifier (TIA).

I. INTRODUCTION

A NESTHESIA is an irreplaceable part of surgery. In surgical operation environments, anesthesia enables doctors to safe and accurate medical process with minimized movement and pain of patients. In general anesthesia, the anesthesia depth is directly related to patient's health. Therefore, it is important

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to maintain a proper depth. Too light anesthesia (underdosage) can cause awareness during anesthesia, allowing the patient to recall the surgical procedure. Patients who have experienced awareness suffer from post-traumatic stress disorder, depression, sleep disorder, and anxiety. Awareness occurs about 1–2 times per 1000 patients, which means 20 000–40 000 cases per year [1]. Furthermore, it shows much higher incidence (0.2%–1.2%) for children [2]. On the other hand, too deep anesthesia (overdosage) can lead to complications such as liver damage, sleep apnea, stroke, lung infections, and even death [3]. It is especially dangerous for high risk patients because of hemodynamic disturbances. To prevent these accidents, anesthesiologists monitor anesthesia depth of patients based on physiological changes.

There are two conventional methods to assess anesthesia depth. The first method is based on observation. Pulmonary measures, cardiovascular, and clinical signs (respiratory rate, mean arterial pressure, heart rate, blood pressure, blood oxygen, shedding of tears, perspiration, and limb movement) are not reliable methods to evaluate the brain status of patients because of its person-to-person dependence. The second method, current anesthesia depth monitoring product bispectral index (BIS) [1], [4] and entropy [5], uses only electroencephalography (EEG) from the frontal lobe and it identifies changes in brain activity based on quantitative analysis during general anesthesia. Most commonly used device, BIS, uses algorithms to provide a numeric value between 0 (patient does not have brain activity) and 100 (patient is fully awake). The value is correlated to the depth of anesthesia and a value of 40–60 is regarded as a proper depth. In the medical market, the BIS monitor is the most popular monitor. However, there are critical limitations in BIS. First, wire-line communication gives inconvenience to surgeons. Second, in the case of long-term sedation [6], contact gel is dried resulting in increased electrode-dc offset (EDO) and contact impedance. Third, EEG signal is easily distorted by electrical interferences such as electromyography (EMG) signals due to patient's nociceptive response and electrocautery for cutting and hemostasis. Fourth, as shown in Table I, EEG signal shows the false response to the anesthesia caused by special types of anesthetic drugs [7] and fails to monitor the anesthesia depth level. This is because N-methyl-D-aspartate (NMDA) receptor does not give notable changes to EEG signal [8]. To assess NMDA receptor antagonist such as ketamine, additional signal should be achieved. According to reference [8],

TABLE I
RECEPTORS AND ANESTHETIC AGENTS

Receptor	Agent	Signal	
		EEG	CBF ³
GABA ¹	Propofol	Sensitive	Delayed
NMDA ²	Ketamine	Insensitive	Sensitive

¹GABA : Gamma-Aminobutyric Acid

²NMDA : N-Methyl-D-Aspartate

³CBF : Cerebral Blood Flow

NMDA receptor changes cerebral blood flow (CBF). If it is possible to achieve additional CBF signal in a compact system form, improved anesthesia depth monitoring system could be implemented. Near-infrared spectroscopy (NIRS) hemodynamic signals, which measure the change of CBF optically, are complementary to the electrical monitoring system based on EEG signal [9], and can not only compensate for the distorted depth level due to electromagnetic interference but also can be implemented in small form. In spite of its importance, a unified anesthesia depth monitoring system combining EEG together with NIRS has not been reported because NIRS signal has widely different dynamic ranges (10 p–10 nA), and also the signal level variations from person to person and environment are not manageable.

In this paper, we present a multimodal anesthesia depth monitoring system-on-chip (SoC) for compact and accurate head-patch system [10]. The proposed SoC communicates with external device through Bluetooth communication. To reject EDO up to ± 300 mV with low noise even in dry condition, mixed-mode dc-servo loop is proposed. Measured NIRS signal is used to compensate electromagnetic interference. Multimodal approach for anesthesia depth monitoring enables users to assess various anesthetic agents. Logarithmic transimpedance amplifier (TIA) provides a 60-dB dynamic range with ambient light rejection. The proposed head patch is fully implemented and verified by clinical trials.

The rest of this paper is organized as follows. Section II describes the overview of the proposed multimodal anesthesia depth monitoring system architecture and its operation. Section III discusses the key building block of the proposed SoC and algorithm including: 1) mixed-mode dc-servo loop; 2) logarithmic TIA with ambient light rejection; 3) closed-loop controlled (CLC) settling monitor; and 4) features and algorithms. Section IV shows the implementation and measurement results including clinical trials. Finally, the conclusion will be made in Section V.

II. OVERVIEW OF HEAD-PATCH ARCHITECTURE AND OPERATION

Fig. 1 illustrates the anesthesia depth monitoring system. On the bottom side of the head-patch, two-channel EEG/EMG electrodes (each 3.14 cm^2) and a one-channel NIRS module composed of a red ($\lambda = 650 \text{ nm}$) and infrared (IR)

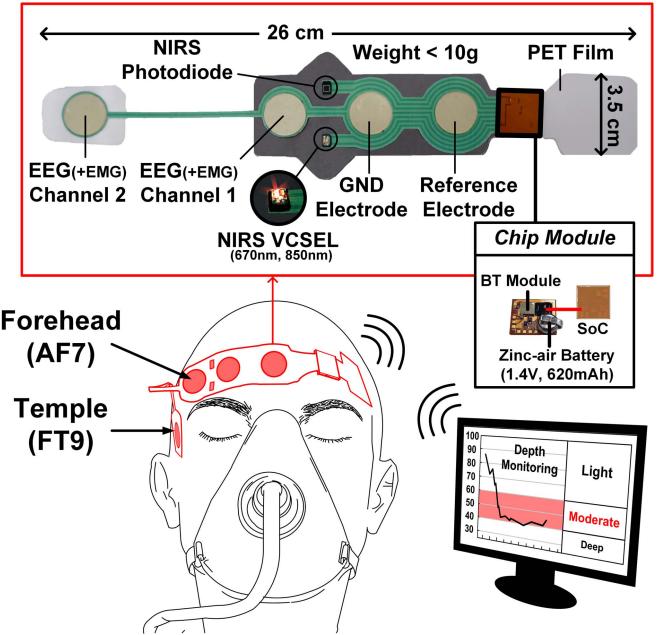


Fig. 1. Proposed multimodal anesthesia depth monitoring system.

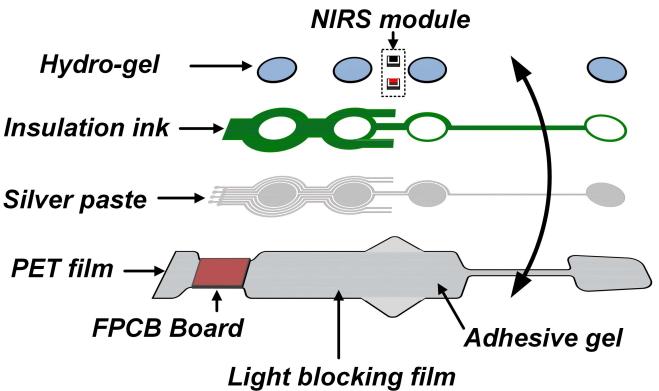


Fig. 2. Proposed system details.

($\lambda = 850 \text{ nm}$) vertical-cavity surface-emitting laser (VCSEL) and a photodiode (PD) on a silicon holder are integrated on the polyethylene terephthalate (PET) film. To reduce ambient light in a system level, winged-shaped blocking film is covering the NIRS module. The proposed SoC, Bluetooth module, and zinc-air battery (620 mAh) are assembled on the flexible printed circuit board. Compact ($26 \times 3.5 \text{ cm}^2$) and lightweight ($< 10 \text{ g}$) system enables the practitioner to measure signals with high convenience. The system is applied directly on the patient's forehead (AF7 site) and temple (FT9 site). Because the muscle of AF7 is sensitive to pain, EEG signal on AF7 is used to monitor EMG activity. All the acquired signals are pre-processed (hemoglobin concentration, band power, phase calculation, multimodal coupling, etc.) in the SoC. Then, these are sent to an external device through Bluetooth interface. The device can display the anesthesia depth level with the help of deep neural network (DNN) to help the anesthesiologist adjust the drug dosages for the safe anesthesia.

Fig. 2 shows the proposed system details. It consists of hydro-gel, reusable NIRS module, insulation ink, silver paste,

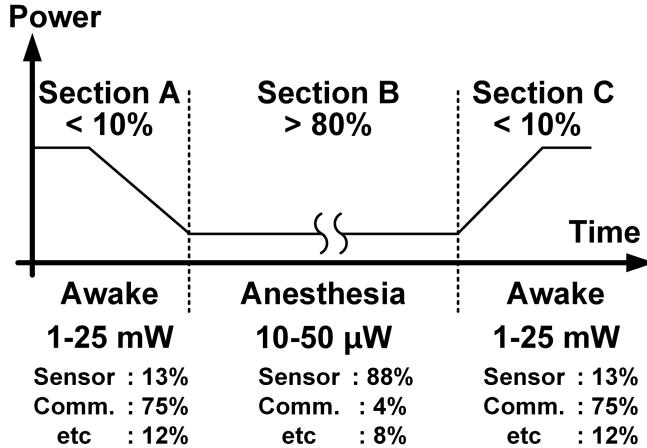


Fig. 3. System operation scenario.

and PET film. Adhesive gel is covered on the PET film so it is easily attached on the patient's forehead. Light blocking film can reject external light over 100 dB and it can help to reduce ambient light component of NIRS. Module hole can hold reusable NIRS module to guarantee good signal quality and avoid direct contact with patient's skin.

Fig. 3 shows the system operation scenario details. In order to guarantee more than 20 h of operation in a small form and wireless system, its power consumption should be optimized. Transition sections from awake to anesthesia (Section A), and from anesthesia to awake (Section C) are more important intervals than those of the steady state phase (Section B), so it is required to have more dense data in Sections A and C. Feature window and window overlap sizes are adjusted depending on which section the patient is in. System power consumption has a range of 1–25 mW (Sections A and C) and 10–50 μ W (Section B). Fortunately, Section B accounts for more than 80% for the total procedure, so overall power consumption can be reduced to 0.2–7 mW. Therefore, it is important to reduce sensor power in Section B for low-power operation.

III. MULTIMODAL ANESTHESIA DEPTH MONITORING SOC AND ALGORITHM

Fig. 4 shows the overall block diagram of the proposed SoC. It consists of: 1) two-channel EEG/EMG readout for large EDO tolerance and low noise; 2) one-channel NIRS readout for large dynamic range; 3) red/IR VCSEL driver for closed-loop duty control; 4) 12-bit successive approximation (SAR) analog-to-digital converter (ADC); and 5) digital module for pre-processing and communication through Bluetooth module. Concurrently achieved bio-signals are converted to digital bits. After pre-processing, these codes are sent to the external devices such as standardized medical instrument and smart device.

A. Mixed-Mode DC-Servo Loop

In surgery environments, the most critical issue is dried interface of wet electrodes, especially for EEG signal sensing in long-term surgery. The increased differential-mode EDO can saturate amplifier outputs. In general, the worst-case

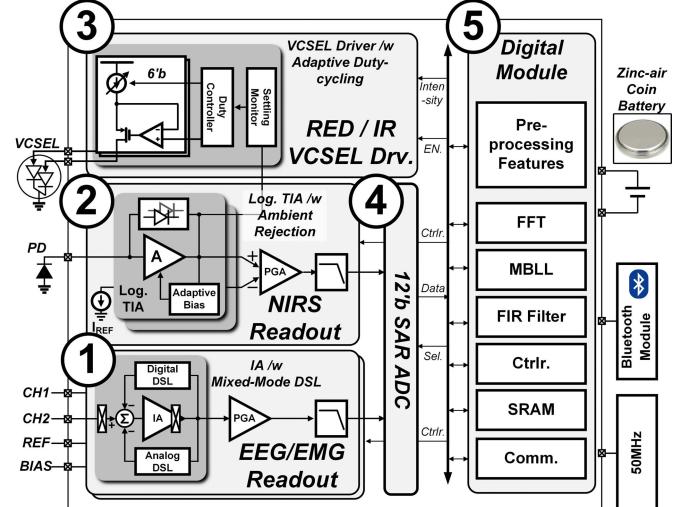


Fig. 4. Overall block diagram of the proposed SoC.

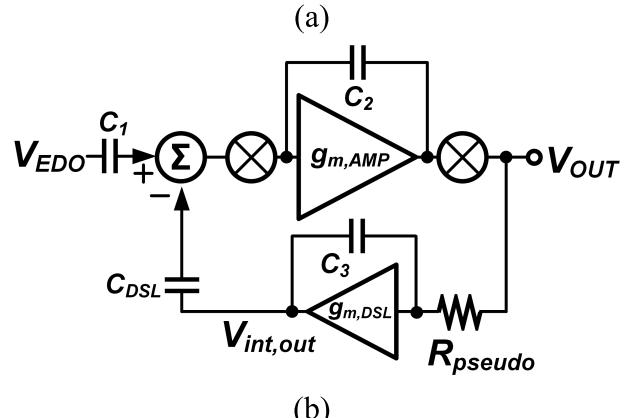
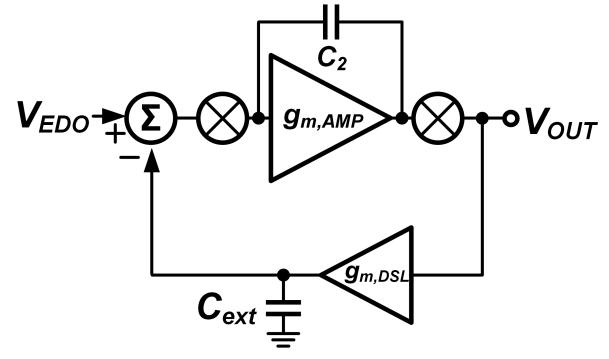


Fig. 5. Conventional dc-servo loop architectures. a) Conventional architecture using external capacitor in DSL. b) Conventional architecture using pseudo-resistor.

specification is tolerable as high as ± 300 mV EDO for dry electrodes. Since it is slowly changed over time, it lies out-of-band of the EEG and EMG signals. But, the EEG amplifier must provide high-pass characteristics to ensure amplifier output not to be saturated. An advanced solution for the problem is using a dc-servo loop (DSL) extracting the dc offset at the output of the amplifier and feeds back at the input of the amplifier to avoid amplifier saturation. It costs additional power and noise.

There are several DSL architectures [9], [11]–[15]. In Fig. 5(a), a simple architecture of read-out circuit in [13]

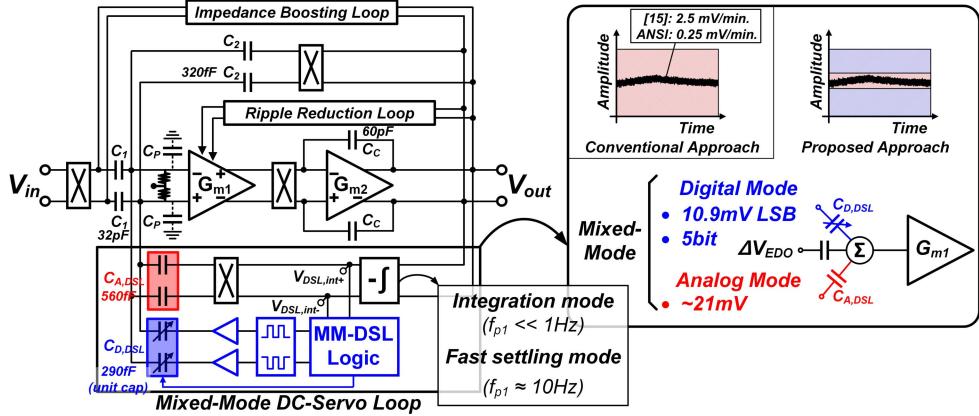


Fig. 6. EEG IA with mixed-mode dc-servo loop.

is illustrated. In this architecture, to achieve large RC time constant with g_m - C filter, an external capacitor ($1 \mu\text{F}$) is used. Its noise contribution is closely related to EDO cancellation range. In Fig. 5(a), its noise contribution is in the following equation:

$$V_{n,DSL}^2 = \frac{V^2 n, g_m, \text{DSL} \cdot g_m, \text{DSL}^2}{s^2 C_{ext}^2} \quad (1)$$

where $V_{n,DSL}^2$ represents the noise contribution component for the overall instrumentation amplifier (IA), $V_{n,gm,DSL}^2$ is the noise of g_m, DSL , g_m, AMP is the transconductance of main amplifier, and C_{ext} is an external capacitor. As $g_m, \text{AMP}/sC_{ext}$ decreases, its noise contribution can also be decreased. However, its limitation comes from cancellation range and it will be as follows:

$$V_{DSL} = V_{OUT} \cdot \frac{g_m, \text{AMP}}{sC_{ext}} \quad (2)$$

where V_{OUT} is the final output of IA, and V_{DSL} is DSL output. The EDO cancellation range is proportion to $g_m, \text{AMP}/sC_{ext}$.

In Fig. 5(b), another DSL architecture [9], [12] is shown. In this architecture, to achieve large RC time constant, pseudo-resistors ($<100 \text{ G}\Omega$) are used. Its noise contribution is

$$\overline{V_{n,DSL}^2} = \left(\frac{C_1 + C_2 + C_P + C_{DSL}}{C_1} \right)^2 \cdot \overline{V_{n,int,out}^2} \cdot \left(\frac{C_{DSL}}{C_1} \right)^2 \quad (3)$$

where C_P represents the parasitic capacitance of g_m, AMP gate and $V_{n,int,out}$ represents output noise of the integrator. Also, in this case, it is proportion to C_{DSL}/C_1 . Its EDO cancellation range is $V_{DSL} = V_{OUT} C_{DSL}/C_1$ and it is also increasing as C_{DSL}/C_1 increases.

For these DSL architectures, there is a tradeoff between noise contribution and EDO cancellation range. In dry electrode condition, EDO range can be up to 300 mV and it causes large power consumption for low $V_{n,int,out}^2$. There have been many IA architectures for EEG monitoring, but their noise-efficiency factor (NEF) cannot be smaller than 4.0 with a 300-mV EDO cancellation range [11]–[15] because

of the tradeoff. In this paper, with the proposed mixed-mode DSL (MM-DSL), 3.59 NEF IA at 300-mV EDO is achieved.

The proposed IA with MM-DSL architecture is shown in Fig. 6. Capacitive-coupled IA [9] is chosen for core amplifier architecture. The impedance boosting loop [9], [12] is designed to have maximum impedance in 50–60 Hz. Adding the positive feedback loop, over $1\text{-G}\Omega$ impedance can be achieved at 50–60 Hz. To alleviate the risk of oscillation, there is enough margin for the boosting capacitance. Moreover, the reconfigurable capacitive digital-to-analog converter (CDAC) is connected in parallel so that it can be trimmed for the proper capacitance size. Ripple reduction loop [9], [12] can be used to reject ripple components caused by chopper modulated 1/f noise and offset. To improve the EDO tolerance with low noise, it needs to be removed in a different way than before. The MM-DSL is composed of digital DSL ($C_{D,DSL}$) for wide range ($\pm 350 \text{ mV}$) and low noise ($0.44 \mu\text{Vrms}$), and analog DSL ($C_{A,DSL}$) for fine resolution. Along with the charge provided by the conventional analog DSL, the digital DSL charge output ($C_{D,DSL} \times V_{DD}$) which is driven by square wave can cancel out the EDO charge ($C_1 \times V_{in,EDO}$). The detailed operation of the proposed MM-DSL is described in the flow chart of Fig. 7. Initially, with the help of SAR algorithm, digital DSL cancels EDO coarsely with 5-bit CDAC of the 10.9-mV LSB. And then, analog DSL is activated to decrease the remaining EDO finely down within 21 mV. There is a tradeoff between amplifier noise performance and the digital bit transition incidence. The smaller analog DSL cancellation range is, the better noise performance is, but the more frequently bit transition occurs. The ratio of digital DSL LSB to analog DSL range should be 1 to even number because after bit transition, it is ideal for EDO to be positioned at the center of the LSB. For the absolute value, in this chip, the analog DSL cancellation range is designed to provide 4 times bit transition/hour [16], which is 0.02% data missing due to settling time. $C_{D,DSL}$ is updated continuously according to $V_{DSL,int}$ to remove the temporal EDO drift. Right after the DSL starts and whenever the value of C_{DSL} changes, digital DSL incurs large settling time over 60 s. The first pole of IA f_{p1} is increased to over 10 Hz (fast settling mode) to reduce the settling time to 30–50 ms. To alleviate stability problem, the pole in the low-noise

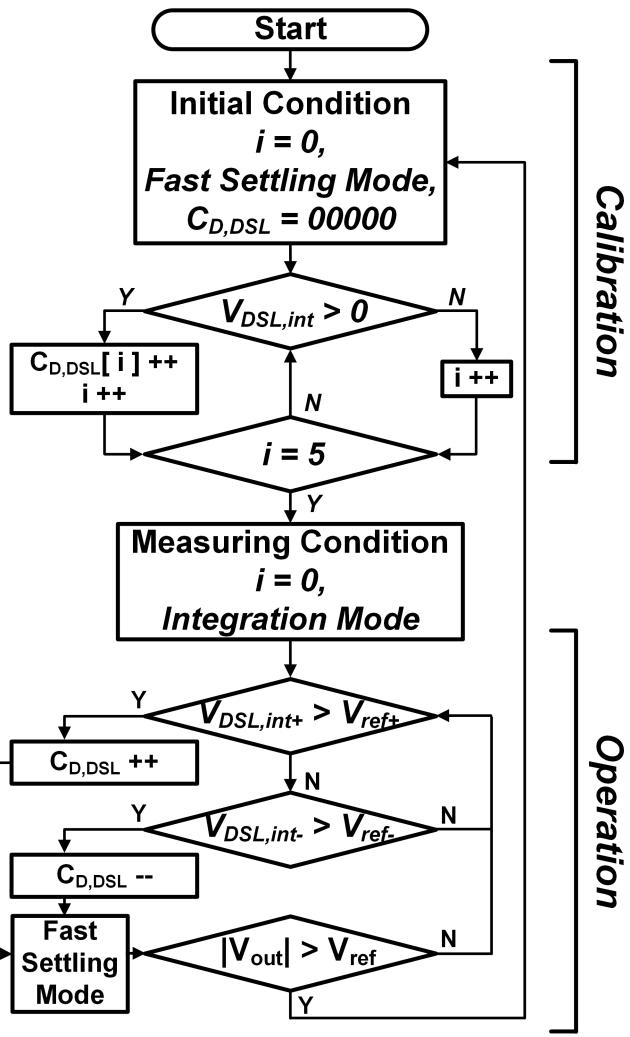


Fig. 7. Mixed-mode DSL flow chart.

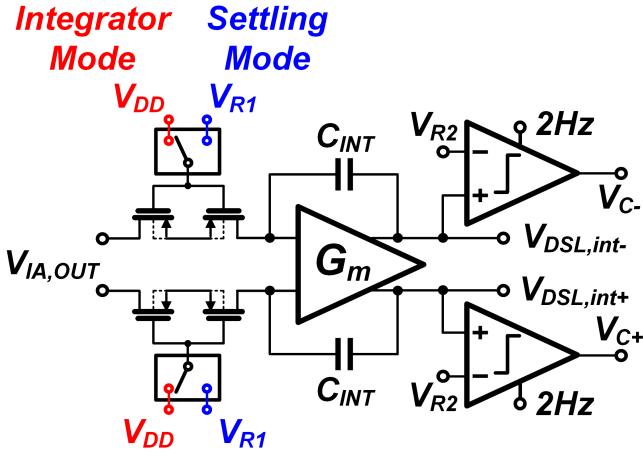
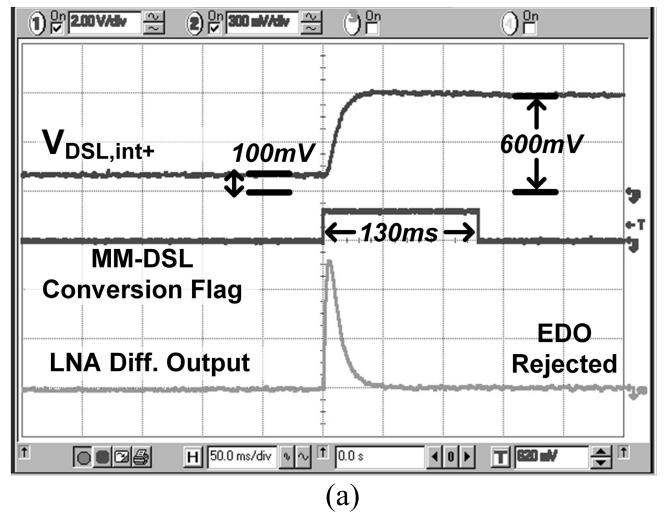


Fig. 8. Mixed-mode DSL integrator.

amplifier (LNA) is moved to 2 kHz with capacitor switching. In this paper, 130-ms window is assigned for the enough margin.

Analog integrator of MM-DSL is shown in Fig. 8. To realize very large RC value, pseudo-resistor is used, but its gate voltage is adjusted to change f_{p1} . In the Integration Mode, when the gate voltage is connected to V_{DD} , this circuit works



(a)

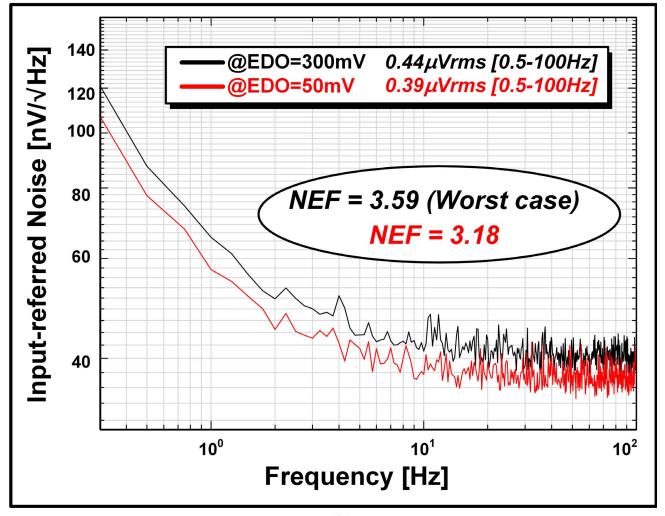


Fig. 9. Measurement results of EEG IA. a) Operation flow time-domain measurement. b) Noise measurement.

as an integrator with $f_{p1} = 0.5$ Hz, and in the fast settling mode, when the gate voltage is connected to reference voltage V_{R1} , f_{p1} increases to >10 Hz. The EDO cancellation range is determined by an output range of the integrator, $V_{DSL,int}$. To monitor the analog DSL cancellation range margin, analog DSL outputs are connected to comparators. Comparator negative inputs are set to V_{R2} (150 mV). If the analog DSL margin is about to be insufficient, that is, when the one of the comparator is inverted, a flag signal is generated to add or subtract the digital DSL LSB. There is an additional power consumption due to digital DSL (capacitance charging <1 nW at maximum capacitance, comparator <10 nW at the 2-Hz sampling rate), but the amount is much smaller than the total IA current consumption (4.5 μ A).

Fig. 9 shows the measurement results. During the bit conversion, IA differential outputs, $V_{DSL,int+}$ node and conversion flag signal are represented in Fig. 9(a). With the EDO drift, $V_{DSL,int+}$ meaning cancellation capacity keeps decreasing until threshold voltage (100 mV) with integration mode. For 130 ms, conversion flag (fast settling mode) is on and $V_{DSL,int+}$ is reset to maximum margin of 600 mV. The IA

TABLE II
COMPARISON TABLE FOR EEG IA

	R. Yazicioglu JSSC'08	J. Yoo JSSC'13	J. Xu JSSC'15	R. Muller JSSC'15	M. Altaf JSSC'15	This Work
V _{DD} (V)	3.0	1.8	1.8	0.5	1.8	1.2
Current(A)	2.3μ	1.4μ	12.9μ ^a	4.6μ ^c	1.8μ ^b	4.5μ (4.9μ^a)
CMRR(dB)	120	>100	102	88	97	>110
Z _{in} (Ω)	1G	>500M	1G@1Hz	28M	>500M	1G
Noise RTI	0.59μVrms [0.5-100Hz]	0.91μVrms [0.5-100Hz]	0.65μVrms ^a [0.5-100Hz]	0.58μVrms [0.5-100Hz]	0.90μVrms [0.5-100Hz]	0.44μVrms (0.48μVrms^a) [0.5-100Hz]
NEF	4.1	5.1	6.80 ^a	4.76 ^c	4.64 ^b	3.59 (4.09^a)
PEF	19.8	46.8	83.2 ^a	11.33 ^c	38.8 ^b	15.5 (20.1^a)
Max. EDO(mV)	45	200	350	50	240	300

^aPGA (power, noise) is considered.

^bThis work uses NEF/ch metric in the paper. It is modified in this table. (×2 for Current)

^cEntire Front-end and ADC power dissipations are considered.

differential outputs are close to zero at the first time because of rejected EDO, but during the fast settling mode, its value is changed because of the changed $C_{D,DSL}$. After that, input EDO is canceled with the changed $C_{D,DSL}$. Because EDO drift is extremely slow [16], bit transition case happened under 3 times for 1-h operation time during surgery. Noise measurement result is shown in Fig. 9(b). At the 300-mV EDO condition, its integrated noise is 0.44 μVrms for 0.5–100 Hz. These results are explained as follows:

$$\overline{V_{n,DSL}^2} = \left(\frac{C_1 + C_2 + C_P + C_{A,DSL} + C_{D,DSL}}{C_1} \right)^2 \cdot \overline{V_{n,int,out}^2} \cdot \left(\frac{C_{A,DSL}}{C_1} \right)^2 \quad (4)$$

$$V_{Range} = V_{int,OUT} \cdot \left(\frac{C_{A,DSL}}{C_1} \right) + V_{DD} \cdot \left(\frac{C_{D,DSL}}{C_1} \right) \quad (5)$$

where $C_{A,DSL}$ represents the analog DSL capacitance, $C_{D,DSL}$ represents the digital DSL capacitance, V_{Range} represents the dc-servo loop cancellation range, and $V_{int,OUT}$ represents the analog DSL output. Due to the decreased $C_{A,DSL}$, the input-referred noise value goes down, but V_{Range} degradation is prevented thanks to $C_{D,DSL}$. Noise value change due to $C_{D,DSL}$ shows minor degeneration because C_1 (32 pF) is much larger than $C_{D,DSL}$ (maximally 9.3 pF). With the help of settling scheme and $C_{D,DSL}$, this architecture can overcome the tradeoff.

Table II shows the comparison result for on-chip DSL IAs. With the help of the MM-DSL, the IA shows the state-of-the-art NEF of 3.59 at the 300-mV EDO input. For IA alone, it dissipates only 4.5 μA including DSL peripheral blocks. Even though PGA is considered, its NEF shows the state of the art with a 300-mV EDO cancellation range.

B. Logarithmic Transimpedance Amplifier With Ambient Light Rejection

There are several requirements of NIRS TIA: 1) large dynamic range of 60-dB NIRS input current because of

person-to-person variation; 2) contrast-sensitive characteristics [17]; and 3) ~10 nA ambient light for the system. With the conventional TIA of resistive feedback, it is impossible to cover 60-dB input dynamic range with fixed feedback resistor. To cover the 60-dB dynamic range, reconfigurable resistive feedback can be used, but its real-time gain adjustments and thermal noise can distort input NIRS current. Moreover, its contrast-sensitive characteristics makes difficult to use linear gain TIA. Ambient light rejection is also necessary to reject light from the intense lamp of operating room. With the system form, ambient light can be reduced by 100 dB at least, so the SoC should reject ambient light current up to 10 nA.

In this paper, to satisfy the overall requirements for NIRS sensing in the operating room, logarithmic TIA with ambient light rejection is proposed. Fig. 10 shows the schematic of the logarithmic TIA. The logarithmic conversion is obtained from the subthreshold exponential current relationship between the current through $M_{3,4}$ and gate-source voltage of $M_{3,4}$. The logarithmic equation and small signal gain are as follows:

$$V_{OUT} = V_t \cdot \log \left(\frac{I_{in}}{I_P} \right) + \kappa V_g + (1 - \kappa) V_{DD} \quad (6)$$

$$v_{OUT} = V_t \cdot \frac{i_{in}}{I_{in}} \quad (7)$$

where V_{out} is the TIA output, I_P is the pre-exponential factor, i_{in} is TIA input current, V_t is the thermal voltage, V_g is the gate voltage of the $M_{3,4}$, κ is the inverse of the subthreshold slope factor, v_{out} is output small signal, and i_{in} is $M_{3,4}$ small signal current. As shown in this analysis, its output characteristics are sensitive to signal contrast. To reject ambient light, duty-cycled VCSEL current driver and first replica part are used. VCSEL driver turns on and off alternatively. When it is OFF-state, SW_{EN} is OFF and only the ambient light component is flow through the first replica part. At this moment, $I_{total} = I_{amb}$ and bias voltage for I_{amb} is stored on the C_1 capacitor. In the ON-state, SW₁ is OFF and $I_{total} = I_{sig} + I_{amb}$. Output signal $V_{out,TIA}$ is determined by only I_{sig} component. It can reject ambient light current up to 10 nA.

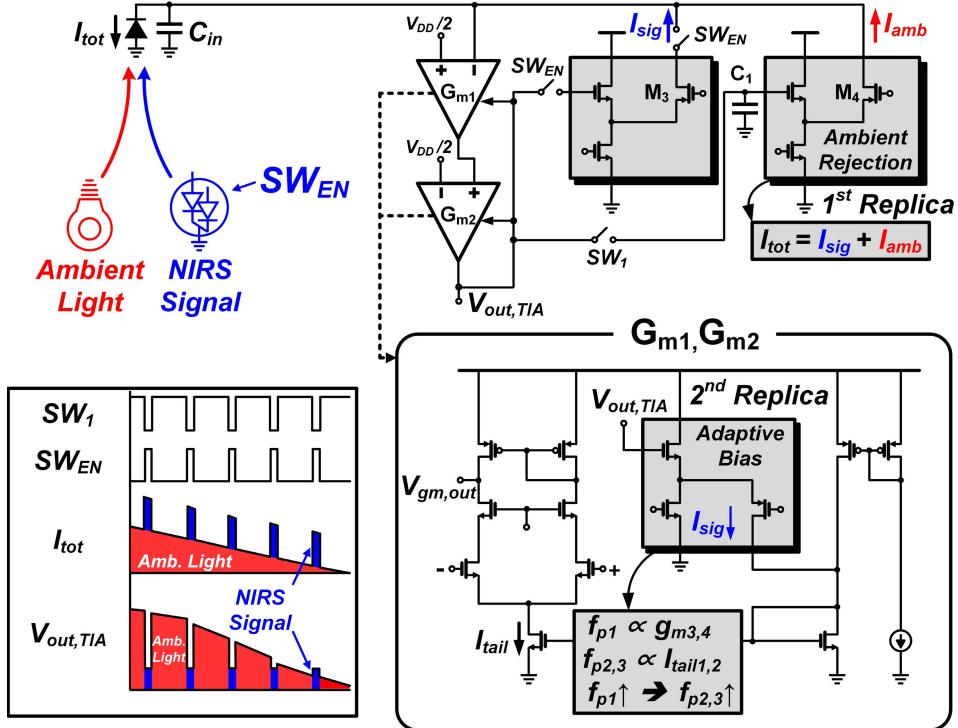


Fig. 10. Logarithmic TIA with ambient light rejection.

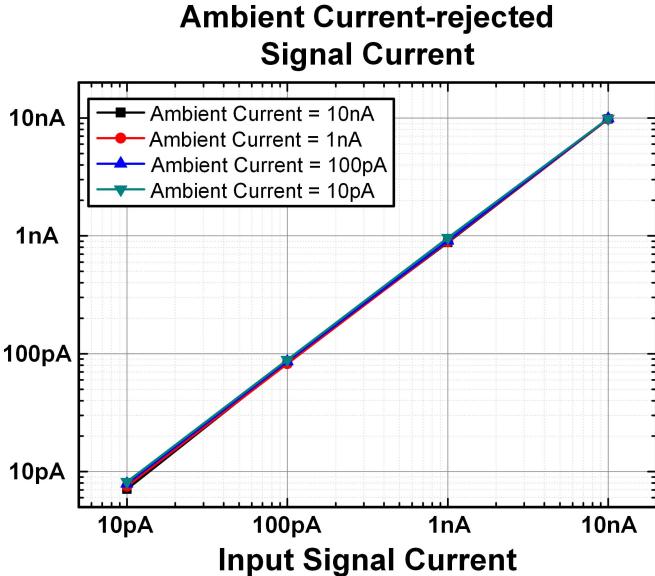


Fig. 11. Ambient current rejection test result.

The resulting problem from the logarithmic TIA is the moving pole depending on input current. The first pole f_{p1} is proportional to $g_{m3,4}$, which is a function of input current. The second and third pole $f_{p2,3}$ are proportional to the bias current of G_{m1} and G_{m2} . When input current increases, it can degrade phase margin and cause stability problem because of the moving first pole. For this reason, adaptive bias circuit with second replica in $G_{m1,2}$ is used. In $G_{m1,2}$, $V_{out,TIA}$ is directly connected to the second replica circuit and it injects current to the conventional bias current. If input current

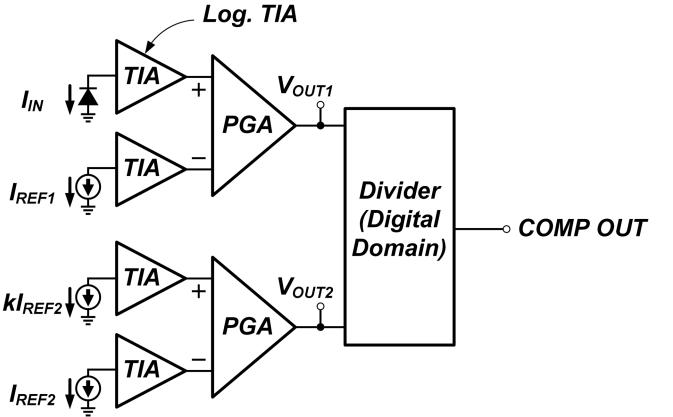


Fig. 12. Temperature compensation circuit in logarithmic TIA.

increases, unlike transconductance in saturation mode, $g_{m3,4}$ is proportional to current in subthreshold mode as I_d/nV_t . It increases second pole according to the first pole changes with I_{tail} current. With the second replica circuit, f_{p1} and $f_{p2,3}$ have linear relationship.

To verify the ambient light rejection scheme, the TIA test was performed with built-in test circuits. The signal and ambient current components are injected by trimmed precise current source. Because the signal current is synchronized with SW_{EN} , it acts like a PD current. Four points (10 pA, 100 pA, 1 nA, and 10 nA) for signal and ambient current components are tested and it is shown in Fig. 11. It shows high accuracy (>95%) in a small ambient light environment, but for large ambient light, low accuracy (<85%) is acquired. The main reason for the inaccuracy is clock-feedthrough. SW_1 control signal can change the stored voltage of C_1 and it can

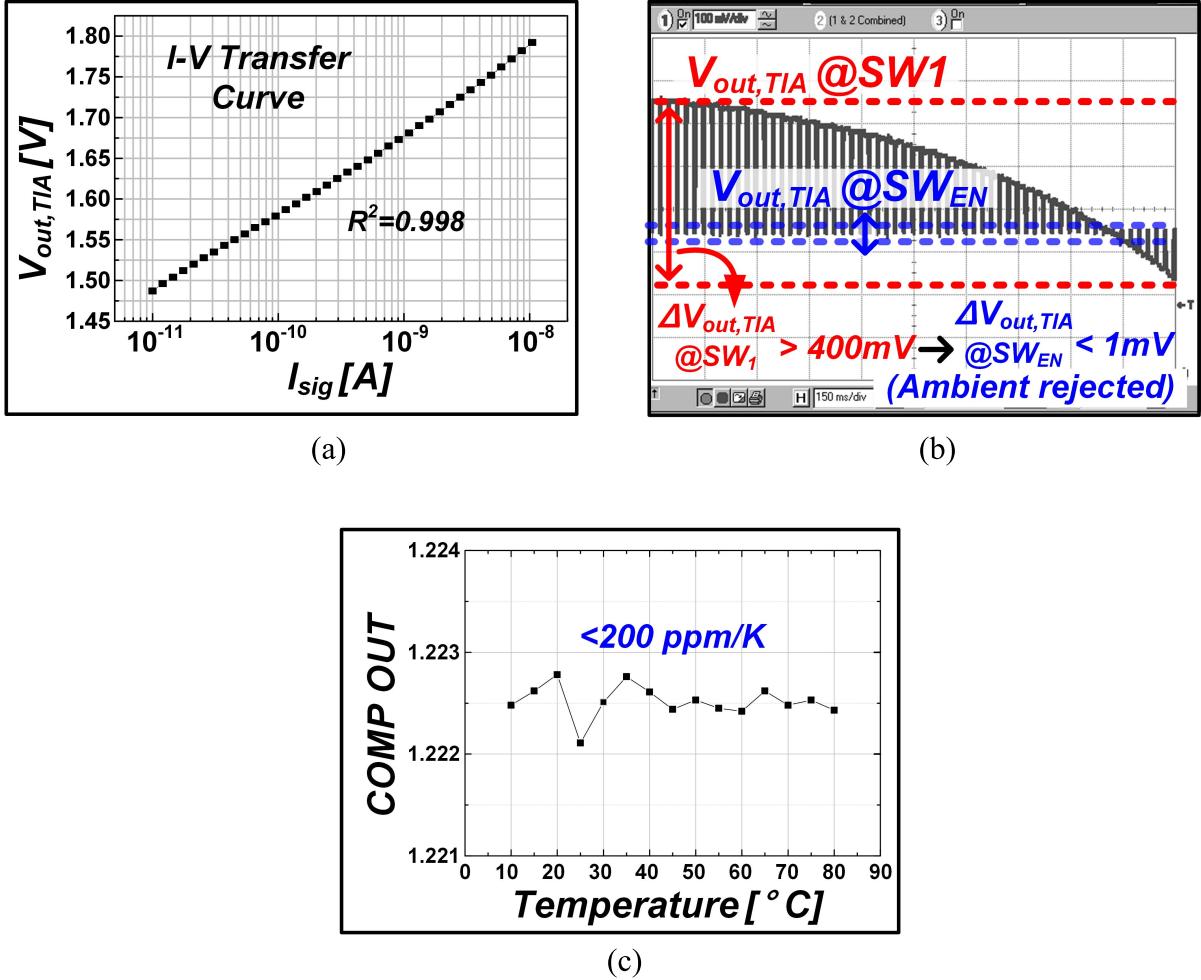


Fig. 13. Measurement results of logarithmic TIA. a) Linearity of TIA. b) Ambient rejection measurement in time domain. c) Temperature compensated output.

change the M_4 source voltage. In rare cases, large ambient current and small signal current can be the input for the TIA, and the clock-feedthrough is fatal for this case. To improve the accuracy, capacitance C_1 should be increased, but there is a limit due to stability.

Because of its temperature dependence in (6) and (7), TIA output can be varied as temperature changes. Its temperature compensation circuit is shown in Fig. 12. With the current references as input sources, dummy TIA circuits [18] are used

$$\begin{aligned} \Delta V_{\text{OUT1}} &= V_t \cdot \log \left(\frac{I_{\text{in}}}{I_P} \right) - V_t \cdot \log \left(\frac{I_{\text{REF1}}}{I_P} \right) \\ &= V_t \cdot \log \left(\frac{I_{\text{in}}}{I_{\text{REF1}}} \right) \end{aligned} \quad (8)$$

$$\begin{aligned} \Delta V_{\text{OUT2}} &= V_t \cdot \log \left(\frac{k I_{\text{REF2}}}{I_P} \right) - V_t \cdot \log \left(\frac{I_{\text{REF2}}}{I_P} \right) \\ &= V_t \cdot \log(k) \end{aligned} \quad (9)$$

$$\begin{aligned} V_{\text{COMP,OUT}} &= \frac{\Delta V_{\text{OUT1}}}{\Delta V_{\text{OUT2}}} = \frac{V_t \cdot \log \left(\frac{I_{\text{in}}}{I_{\text{REF1}}} \right)}{V_t \cdot \log(k)} \\ &= \frac{\log \left(\frac{I_{\text{in}}}{I_{\text{REF1}}} \right)}{\log(k)}. \end{aligned} \quad (10)$$

The temperature dependence can be minimized by subtraction and dividing functions. Parameter k is 10 and I_{REF1} is 100 pA.

Fig. 13 shows the measurement results of logarithmic TIA. As shown in Fig. 13(a), its R-squared value of TIA transfer function is 0.998 which shows the good logarithmic correlation. The main reason of nonlinearity is related to operation region of $M_{3,4}$. However, in this paper, the 60-dB input dynamic range is enough for linear log functions. To show the ambient light rejection function, in Fig. 13(b), ambient light is fluctuated with the steady VCSEL input condition. $V_{\text{out},\text{TIA}}$ at SW_{EN} on shows voltage variation under 1-mV despite 400-mV ambient light variation. Temperature compensated output shows steady output for the temperature variation condition is shown in Fig. 13(c). For 10 $^{\circ}\text{C}$ –80 $^{\circ}\text{C}$ variation, the ratio between $V_{\text{out}1}$ and $V_{\text{out}2}$ shows less than 200 ppm/K.

C. Closed-Loop Controlled Settling Monitor

As the C_{in} capacitance (<100 pF) and input current values have a large dynamic range (10 p–10 nA) due to person-to-person differences, it results in variable settling time of TIA. To save the power consumption and monitor the settling state of TIA, the turn-on time of VCSEL should be adaptively

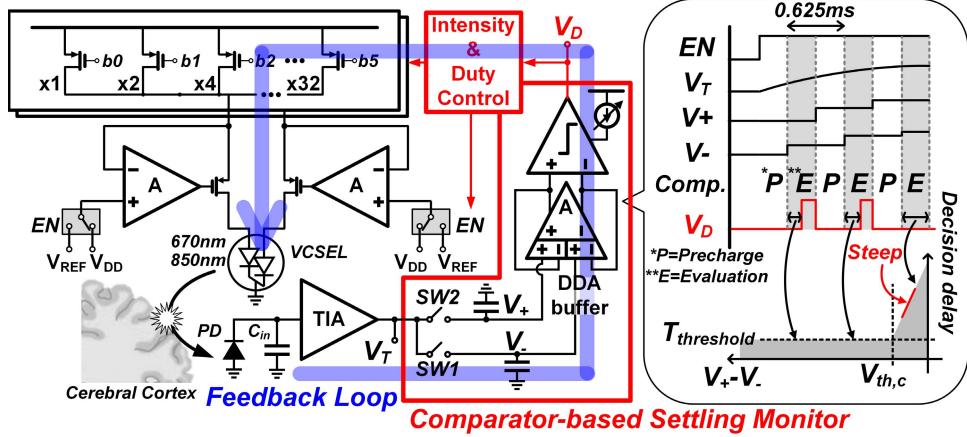


Fig. 14. CLC NIRS current driver.

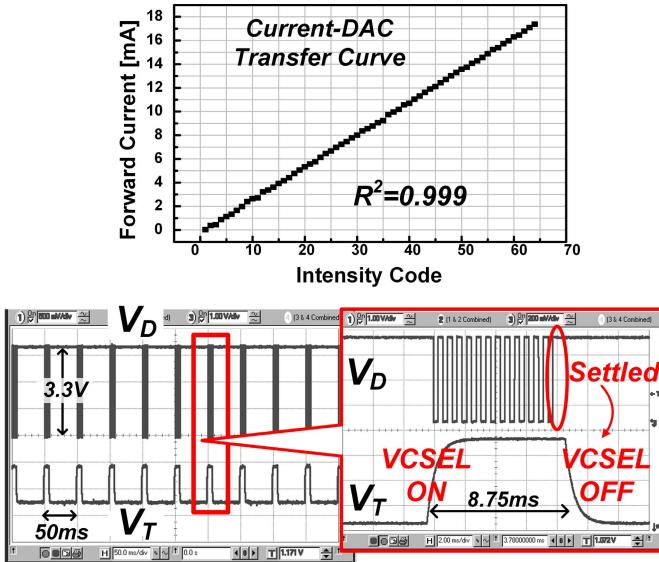


Fig. 15. Measurement results of current driver.

controlled. To satisfy the requirements, CLC NIRS current driver using comparator is proposed. Fig. 14 shows the schematic of the CLC NIRS current driver. The settling monitor circuit is composed of switch and capacitor for alternate sampling of TIA output, a differential difference amplifier buffer for a fixed common-mode voltage, and a comparator for difference monitor. At the P (precharge) period with SW_2 ON, TIA output (V_T) is sampled on V_+ node and at E (evaluation) period with SW_1 ON, V_T is sampled on V_- node. The comparator delay time is evaluated based on their voltage difference. When the voltage difference is larger than threshold value ($V_{th,c}$), the comparator delay time is almost constant $T_{threshold}$, but when the input voltage difference is less than $V_{th,c}$, the comparator delay time increases drastically. If comparator delay is longer than the E period or comparator input difference becomes temporally constant, TIA output is stabilized and VCSEL can be turned off to save power.

Fig. 15 shows the measurement results of the current driver. With the comparator-based settling monitor, settling state is constantly monitored. V_D represents the comparator output and V_T means TIA output. As shown in the V_D result, it does

not show any changes because of settled V_T value. VCSEL turns on during 8.75 ms at the moment. Its driving current from 0 to 17.2 mA can be controlled linearly by 6-bit intensity codes

D. Features and Algorithms

Figs. 16 and 17 show algorithm flow and actual measurement. In EEG [19], three domains (frequency, phase, and time) are used to extract features. These features are the similar with those of the BIS monitor. In frequency domain, beta ratio and EMG signals are used. The more deeply anesthetized the patient is, the smaller the frequency component of the EEG signals becomes. The power ratio between 30–47 Hz and 11–20 Hz represents an obvious change for the states of patient. EMG magnitude reflects the muscle activity or artifact. Large magnitude of EMG gives more weight to the NIRS rather than EEG for final output. SynchFastSlow is a feature that can be extracted from the phase domain. Bispectrum operation is applied to the 0.5–47-Hz and 40–47-Hz bands and the ratio of the two results is used. This feature is used to digitize the phase nonlinear interaction in the brain. In time domain, burst suppression ratio and quazi features are used. When the patient is in a very deep anesthetic state, EEG repeats burst and suppression. Burst suppression ratio and quazi features are a kind of markers representing the deep anesthetic state.

NIRS provides a concentration of oxygenated (oxy-Hb, HbO_2) and deoxygenated (deoxy-Hb, Hb) hemoglobin that are in direct relation with hemodynamic changes in the brain. For the feature, absolute (oxy-Hb, deoxy-Hb) and relative values ($rHbO_2 = HbO_2/HbO_2 + Hb$, $rHb = Hb/HbO_2 + Hb$) of concentration are used. Agents affect the brain cortex activation and its effect is shown as blood flow change. Especially, the pre-frontal cortex represents the patient's consciousness, it is the best position to record NIRS signal for anesthesia application. These features provide a better understanding of relationship between hemodynamic changes and the anesthetic state in special drugs use and electromagnetic noise environment.

Temporal kernel canonical correlation analysis is used to calculate neurovascular coupling [20]. The algorithm is

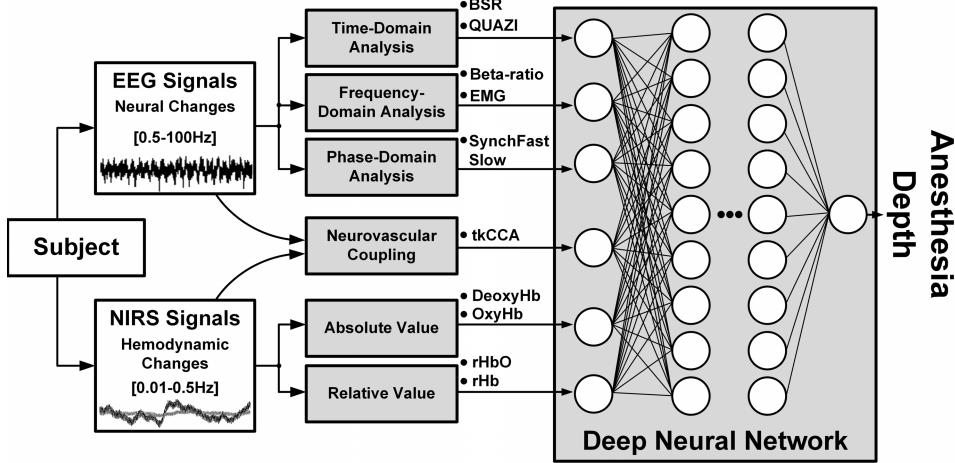


Fig. 16. Depth index algorithm flow.

Features from measured results

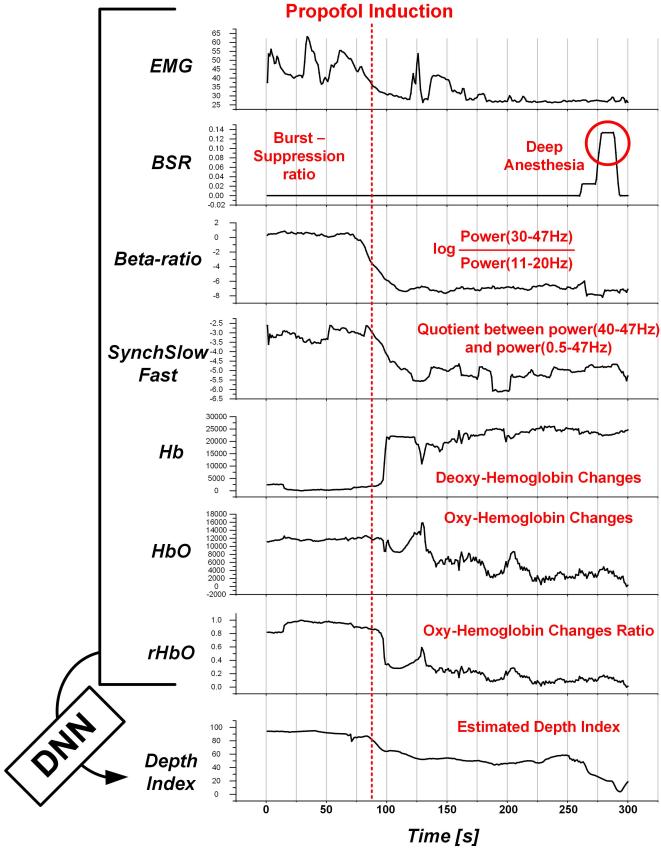


Fig. 17. Actual measurement and extracted features.

used for maximum correlation between different modalities. According to the anesthetic depth of patient, its correlation pattern shows different patterns. In this paper, to combine EEG and NIRS signals and to find the coupling coefficient, temporal kernel canonical correlation analysis is adopted. This coefficient can be an additional feature for depth monitoring. Especially, this feature shows better results for some anesthetic agents which does not give changes to BIS monitoring.

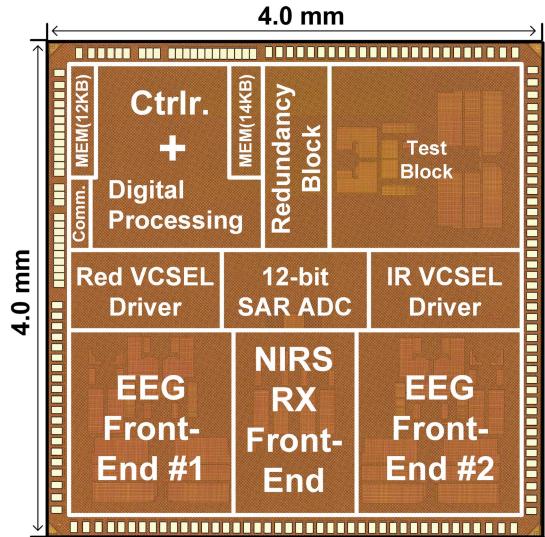


Fig. 18. Chip micrograph.

For data combining, DNN technique is used. The proposed DNN combines 10 features for the anesthesia depth estimation. Back propagation ANN is used with a sigmoid activation function and the Levenberg–Marquardt algorithm. The number of nodes in the hidden layer is 5. The system calculated the final output based on running average of the 60 epochs of data (each epoch is 0.5 s). The number of the total samples is 1210 h from 380 patients. By referring to anesthetic agent concentration and patient's response to external stimulation, skilled anesthetist's comment was used as a ground truth for training.

IV. MEASUREMENT AND IMPLEMENTATION RESULTS

A. Chip Implementation Results

Fig. 18 and Table III show the chip micrograph and a performance summary. The $4 \times 4 \text{ mm}^2$ chip is fabricated in 65-nm CMOS process. It dissipates 25.2-mW peak power with the maximum red/IR VCSEL driving current of 5.4 mA/7.3 mA.

TABLE III
CHIP PERFORMANCE SUMMARY

Process		65nm CMOS	
Die Size		4.0 x 4.0 mm ² (including pads)	
Supply Voltage		1.2 V / 3.3 V	
Max. Power Consumption		25.2mW	
EEG Readout	LNA	Gain	100V/V
		Bandwidth	0.5-250Hz
		Input-Referred Noise	0.44μV _{rms}
		EDO-tolerance	350mV
		Current	4.5μA
		Input Impedance	1GΩ @60Hz
	PGA	NEF	3.59
		Gain	20-54dB
		Bandwidth	250Hz
		Current	2.0μA
	Bit / Sampling Rate		12b / 2kHz
NIRS	Read-out	Gain	155-235dB
		Bandwidth	1k-100kHz
		Input Dynamic Range	10p-10nA
		Ambient-tolerance	10p-10nA
		Current	1μ-30μA
		Bit / Sampling Rate	12b / 20-80Hz
	Driver	Bit	6bit
		Current Range	0 - 17.2mA
	Digital Block		Operating Freq.
	On-chip SRAM		50 MHz
	On-chip SRAM		26 KB

With the help of MM-DSL, the IA shows the state-of-the-art NEF of 3.59 at the 300-mV EDO input. Logarithmic TIA can reject ambient light of 10 p–10 nA to maximize the dynamic range up to 60 dB. According to the comparator-based settling monitor output, NIRS driver duty cycle can be adjusted from 0.625 m to 50 ms adaptively.

B. System Implementation Results

Fig. 19 shows the clinical trials environment. In the operating room, the external device is used to monitor and record EEG and NIRS signals in real-time through Bluetooth communication.

Index algorithm of previous work is focused on unimodal features. In this paper, coupling between EEG and NIRS is considered for additional feature. Table IV shows the EEG-NIRS coupling coefficient feature result for eight patients. Among several features, coupling between EEG beta

TABLE IV
EEG-NIRS COUPLING COEFFICIENT RESULTS

EEG(Beta)-NIRS(HbO₂) Coupling Coefficient

	Awake	Anesthesia
#1	0.654	0.052
#2	0.597	0.120
#3	0.701	0.075
#4	0.407	0.021
#5	0.486	0.088
#6	0.698	0.102
#7	0.566	0.054
#8	0.751	0.105
Avg.	0.608	0.077

TABLE V
SYSTEM COMPARISON TABLE

	BIS™	This Work
System		
Electrode Dimension	28cm x 2.8cm	26cm x 3.5cm
Components	Monitor + Converter + Electrode	Electrode + External Device
Communication	Wireline	Wireless
Signal	EEG	NIRS, EEG
Ketamine Monitoring	X	O
Electrical Interference Compensation	X	O

band power and HbO₂ concentration show obvious changes. On average, the coupling coefficient is 7.9 times larger when awake state compared to sleeping state.

Fig. 20 shows the clinical results for propofol-induced general anesthesia and ketamine-induced general anesthesia, respectively. First, the estimated anesthesia depth values of the proposed system are compared with reference values, in this case BIS [4] output, during the same surgical operation. The proposed depth index trends such as sudden drop after the propofol sedation and steady increase after the reduction of inhalational anesthetic are almost the same as the index of reference. During intubation, which causes intense EMG, and electrocautery step, sudden BIS index rising (10–15) is observed but the proposed system generates stable results.

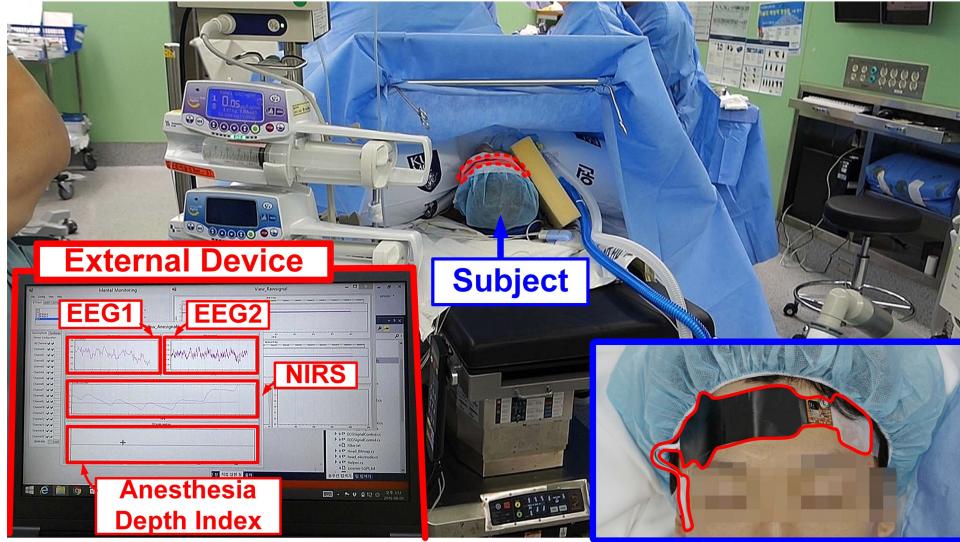


Fig. 19. Clinical trials environment.

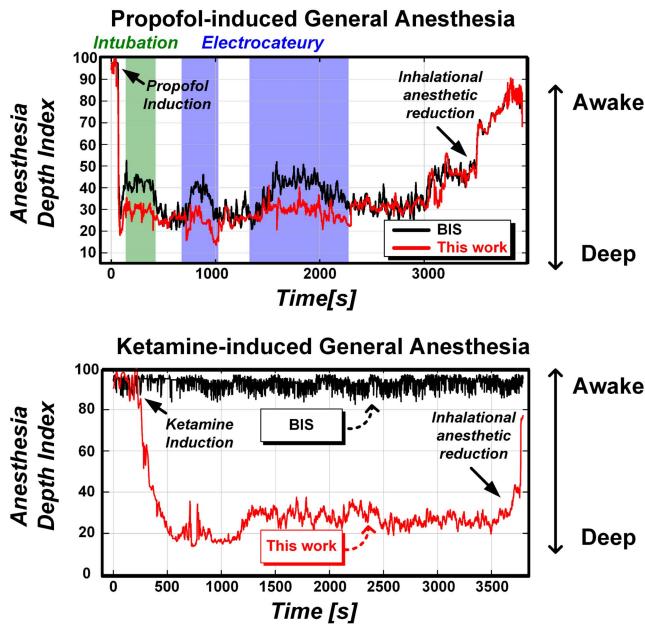


Fig. 20. Clinical results for propofol-induced general anesthesia and ketamine-induced general anesthesia.

Second, ketamine, which BIS gives false result, is used to test the operation of the proposed system. Its output clearly shows the clinically important transition from the awake to deep state but BIS cannot detect the transition.

Table V shows system comparison with BIS. The proposed system is implemented in PET film. The SoC can communicate with external device through wireless communication. Thanks to the multimodal measurement, it guarantees wide assessability for various anesthetic agents and robustness to electrical interference. As a result, the proposed anesthesia monitoring system achieves accuracy and compactness at once.

V. CONCLUSION

A multimodal SoC is designed for an accurate and compact anesthesia depth monitoring. The proposed SoC provides a wireless communication interface for convenient operating room environments. The proposed EEG IA measures EEG signal from frontal and temple head. To reject EDO with low-noise characteristic, the mixed-mode DSL which adopts analog and digital DSL concurrently is used. By adding NIRS measurements, the system robust to electromagnetic noise (EMG, electrocautery) is realized. The logarithmic TIA measures NIRS signal to achieve hemodynamic information from forehead. It covers 10 p–10 nA input current range without discrete gain change. Ambient light can be reduced by >100 dB in the system and <10 nA in the circuit. For efficient power consumption in the current driver and accurate signal measurement in the TIA, CLC current driver is proposed. With a simple comparator, its settling status can be monitored. The proposed SoC occupies 4 mm × 4 mm including pads in a 65-nm CMOS technology, and it is incorporated into a 3.5 cm × 26 cm head patch. With the multimodal signal achievement, it assesses both γ -Aminobutyric acid (GABA) and NMDA receptor-based anesthetic agents. As a result, the compact anesthesia depth monitoring head patch enables more accurate anesthesia depth monitoring even under special drugs which the BIS cannot detect the anesthesia for safe surgery in the operating room.

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