

An FFE Transmitter Which Automatically and Adaptively Relaxes Impedance Matching

Minsoo Choi^{ID}, Sooeun Lee^{ID}, Myungguk Lee^{ID}, Ji-Hoon Lee^{ID}, Jae-Yoon Sim^{ID}, *Senior Member, IEEE*, Hong-June Park^{ID}, *Senior Member, IEEE*, and Byungsub Kim^{ID}, *Senior Member, IEEE*

Abstract—This paper proposes the first feed-forward equalizing transmitter (Tx) which adaptively relaxes impedance matching. Using an on-chip time-domain reflectometer monitor, the Tx accurately detects the impedances of the channel and the receiver (Rx), and then automatically configures its termination impedance to maximize the received signal by optimally relaxing the constraint of impedance matching at the cost of a negligible penalty in signal integrity. The Tx is universally compatible with arbitrary impedances of channels and Rx, and achieves better performance and power efficiency than the conventional Tx with impedance matching. The proposed Tx was fabricated in 65-nm CMOS technology. The Tx successfully adapted to any combination of a channel impedance of 35–75 Ω and a receiver impedance of 30–200 Ω. When the impedance matching of the Tx is adaptively and optimally relaxed, the eye size and the power efficiency are improved by up to 3.8 times and 2 times, respectively, compared with the conventional Tx. These results verify that the proposed Tx can adapt to various impedances of the channel and the receiver while achieving better performance and power efficiency than the conventional Tx with impedance matching.

Index Terms—Compatibility of impedance standards, feed-forward equalization, high-speed interconnect, impedance adaptation, impedance matching, relaxed impedance matching.

I. INTRODUCTION

IN MODERN high-speed interconnects, diverse impedance standards are being used. In backplane applications, the differential characteristic impedance is typically 100 Ω [1]–[4], but also any value between 80 and 130 Ω is allowed according to IEEE 802.3ba [5] or optical interconnect forum (OIF) [6]. Standards of double data rate version 4 (DDR4) and graphics double data rate version 5 (GDDR5) specify that two different characteristic impedances (40 and 50 Ω) can be used for channels and any resistances between 25 and 60 Ω can be used for termination [7]–[9]. In cable applications, both 75-Ω coaxial [10] and 50-Ω twinax cables [11] are widely used.

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The authors are with the Department of Electrical Engineering, Pohang University of Science and Technology, Pohang 790-784, South Korea (e-mail: byungsub@postech.ac.kr).

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Diversity of impedance standards is the source of huge user inconvenience due to incompatibility. Since electronic devices can be only connected to cables and ports exploiting the identical impedance standard, users must check compatibility of products regarding the impedance standard. Otherwise, users suffer from signal integrity problems. For example, if a 50-Ω transmitter (Tx) is used with a 100-Ω receiver (Rx) and a 75-Ω channel, impedance mismatch causes reflection which severely raises the bit-error rate. However, of course, many regular users are not aware of the impedance standards, and impedance-standard compatibility among devices is too confusing for them, becoming the source of big inconvenience.

In addition, many researchers reported that the 50-Ω standard is not optimal for power [12] and performance [13] since it causes unnecessarily large power consumption and also limits the Tx output swing [12]–[14]. These can be improved if a link is optimally customized for a specific application without restriction of an impedance standard [10]. However, customized links could not be widely used due to problem in compatibility with the existing 50-Ω infrastructures. For this reason, a fixed impedance standard obstructs the advancement of technology.

Furthermore, the impedance matching is an over-constraint, which can be relaxed for better performance and power efficiency without sacrificing signal integrity [15].

In this paper, we propose the first high-speed feed-forward equalizing (FFE) Tx which automatically adapts to various channel and Rx impedances. The impedances of the channel and the Rx are detected by an on-chip time-domain reflectometer (TDR) monitor to optimally configure Tx impedance. The optimal Tx impedance that maximizes the received signal at a cost of negligible reflection is theoretically derived for the first time from a new impedance matching constraint dubbed “relaxed impedance matching” which is also suggested for the first time. The proposed FFE Tx was fabricated in 65-nm CMOS technology. In the experiment, the Tx successfully adapted to any combination of a channel impedance between 35 and 75 Ω and an Rx impedance between 30 and 200 Ω while achieving better performance and power efficiency than the conventional Tx. In a blind compatibility test, the proposed Tx improved the eye size by up to 3.8 times compared with the conventional Tx. Power efficiency is improved by up to twice.

The rest of this paper is organized as follows. Section II theoretically explains relaxed impedance matching. Sections III and IV, respectively, describe the circuit

design and the adaptation algorithm of the proposed FFE Tx. Section V shows the experimental results. Section VI provides the conclusion.

II. RELAXED IMPEDANCE MATCHING

We propose a new impedance matching constraint dubbed “relaxed impedance matching” for the first time. This constraint provides theoretical guidance in maximizing the received signal by violating impedance matching at the cost of a penalty in signal integrity below a design target. This section will explain how relaxed impedance matching constraint can be theoretically derived and how it can be applied to Tx design.

A. Transfer Function Model

For later derivation, this section reviews a transfer function model of a high-speed link [16]. An interconnect with a current-mode-logic (CML) Tx and an Rx can be modeled as Fig. 1. The Tx is modeled with a current source $I_{Tx}(f)$ and a termination impedance $Z_{Tx}(f)$. The Rx is modeled with a termination impedance $Z_{Rx}(f)$. $V(l, f)$ is the received voltage at the Rx. The interconnect is modeled as an $RLGC$ transmission line with length l where R , L , G , and C are the line resistance, inductance, conductance, and capacitance per unit length, respectively. This transmission line can be characterized by a characteristic impedance $Z_C(f)$ and a propagation constant $\gamma(f)$

$$Z_C(f) = \sqrt{(R + j2\pi fL) / (G + j2\pi fC)} \quad (1)$$

$$\gamma(f) = \sqrt{(R + j2\pi fL)(G + j2\pi fC)} = \alpha(f) + j\beta(f). \quad (2)$$

In (2), $\alpha(f)$ and $\beta(f)$ are the attenuation constant and the phase constant, respectively. The transfer function $V(l, f)/I_{Tx}(f)$ of the interconnect in Fig. 1 can be rigorously derived as

$$\frac{V(l, f)}{I_{Tx}(f)} = \left\{ \frac{Z_{Tx}(f)Z_C(f)}{Z_{Tx}(f) + Z_C(f)} \right\} 2e^{-l\gamma(f)} \left\{ \frac{Z_{Rx}(f)}{Z_C(f) + Z_{Rx}(f)} \right\} \times \left\{ \frac{1}{1 - \Gamma_{Tx}(f)\Gamma_{Rx}(f)e^{-2l\gamma(f)}} \right\} \quad (3)$$

where $\Gamma_{Tx}(f) = (Z_{Tx}(f) - Z_C(f))/(Z_{Tx}(f) + Z_C(f))$ and $\Gamma_{Rx}(f) = (Z_{Rx}(f) - Z_C(f))/(Z_{Rx}(f) + Z_C(f))$ are the reflection coefficients at the Tx and the Rx, respectively [16]. If the interconnect satisfies the validity condition

$$|\eta(f)| = |\Gamma_{Tx}(f)\Gamma_{Rx}(f)e^{-2l\gamma(f)}| \ll 1 \quad (4)$$

$V(l, f)/I_{Tx}(f)$ can be approximated as

$$\frac{V(l, f)}{I_{Tx}(f)} \approx \left\{ \frac{Z_{Tx}(f)Z_C(f)}{Z_{Tx}(f) + Z_C(f)} \right\} 2e^{-l\gamma(f)} \left\{ \frac{Z_{Rx}(f)}{Z_C(f) + Z_{Rx}(f)} \right\}. \quad (5)$$

Equation (5) accurately describes the transfer function as long as (4) is satisfied [16]. The relative error of (5) with respect to (3) is identical to the validity parameter $|\eta(f)|$ of (4) [16].

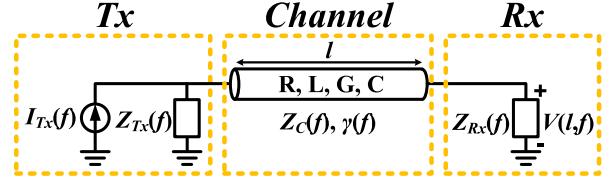


Fig. 1. Model of an interconnect with a CML Tx and an Rx.

B. Relaxed Impedance Matching

Relaxed impedance matching is a loose design constraint on termination impedances in order to bound deviation of the spectral shape of the transfer function due to impedance mismatch below a desired level. Whereas the conventional impedance matching guarantees zero reflection, relaxed impedance matching guarantees that reflection negligibly affects the spectral shape of the transfer function.

Theoretically, a transfer function of a well-matched interconnect is proportional to $e^{-l\gamma(f)} = e^{-l\{\alpha(f)+j\beta(f)\}}$. In typical interconnects (Fig. 1), $Z_C(f)$, $Z_{Tx}(f)$, and $Z_{Rx}(f)$ are usually resistive [$Z_C(f) = Z_0$, $Z_{Tx}(f) = R_{Tx}$, and $Z_{Rx}(f) = R_{Rx}$], and thus the rigorous transfer function (3) can be expressed as

$$\frac{V(l, f)}{I_{Tx}(f)} = \left(\frac{R_{Tx}Z_0}{R_{Tx} + Z_0} \right) 2e^{-l\gamma(f)} \left(\frac{R_{Rx}}{Z_0 + R_{Rx}} \right) \times \left\{ \frac{1}{1 - \Gamma_{Tx}\Gamma_{Rx}e^{-2l\gamma(f)}} \right\}. \quad (6)$$

If the termination impedances are matched ($R_{Tx} = R_{Rx} = Z_0$), the rigorous transfer function can be derived from (6) as

$$\frac{V(l, f)}{I_{Tx}(f)} = \left(\frac{Z_0}{2} \right) e^{-l\gamma(f)} = \left(\frac{Z_0}{2} \right) e^{-\alpha(f)l} e^{-j\beta(f)l}. \quad (7)$$

Because $e^{-l\gamma(f)}$ is the only frequency-dependent term in (7), the spectral shape of the transfer function with impedance matching (7) is solely determined by $e^{-l\gamma(f)} = e^{-l\{\alpha(f)+j\beta(f)\}}$.

Even though the termination impedances are not matched, the spectral shape of the transfer function can be preserved as long as the validity condition (4) is satisfied. Although $R_{Tx} \neq Z_0$ and $R_{Rx} \neq Z_0$, the transfer function can be approximated as (8) from (6) if (4) is satisfied; i.e., $|\eta(f)|$ is small

$$\frac{V(l, f)}{I_{Tx}(f)} \approx \left(\frac{R_{Tx}Z_0}{R_{Tx} + Z_0} \right) 2e^{-l\gamma(f)} \left(\frac{R_{Rx}}{Z_0 + R_{Rx}} \right). \quad (8)$$

Even in this case, the spectral shape of the transfer function is almost indistinguishable from the one with impedance matching (7) because $e^{-l\gamma(f)} = e^{-l\{\alpha(f)+j\beta(f)\}}$ is the only frequency-dependent term in both (7) and (8). In addition, the deviation of the spectral shape between (7) and (8) is bounded by a small number $|\eta(f)|$ of (4) if (4) is satisfied because the relative approximation error of (8) with respect to (6) is $|\eta(f)|$ [16]. This implies that the penalty of violating impedance matching is negligible in terms of signal integrity and is bounded by (4). In this sense, the condition (4) will be referred as a relaxed impedance matching constraint in the rest part of this paper.

Relaxed impedance matching constraint provides design guidance in tradeoff between signal integrity and other metrics such as signal amplitude. For instance, clever selection of R_{Tx} and R_{Rx} satisfying (4) can increase the amplitude of the received signal with a negligible penalty in signal integrity. Within the range satisfying (4), we can intentionally select R_{Tx} and R_{Rx} to increase $(R_{Tx}Z_0/(R_{Tx} + Z_0))(2R_{Rx}/(Z_0 + R_{Rx}))$ term of (8) larger than the corresponding term $Z_0/2$ of (7). This selection increases the magnitude of the transfer function for all frequencies, yet the penalty in signal integrity is bounded by a small number $|\eta(f)|$. As a result, the received signal is larger than the one of impedance matching, and has a negligible penalty in signal integrity.

Simulation verifies the concept of relaxed impedance matching. Fig. 2 shows the magnitude and phase of the transfer function ($|V(l, f)/I_{Tx}(f)|$ and $\angle(V(l, f)/I_{Tx}(f))$) and the magnitude of the validity parameter ($|\eta(f)|$) of example interconnects with $Z_0 \approx 50 \Omega$ and various values of R_{Tx} and R_{Rx} . The spectral shapes of $|V(l, f)/I_{Tx}(f)|$ and $\angle V(l, f)/I_{Tx}(f)$ with $R_{Tx} = 65 \Omega$ and $R_{Rx} = 80 \Omega$ are almost identical to the ones with $R_{Tx} = R_{Rx} = 50 \Omega$ [Fig. 2(a) and (b)] because (4) is satisfied ($|\eta(f)| < 0.03$) for all frequencies [Fig. 2(c)]. Also, Fig. 2(a) shows that $|V(l, f)/I_{Tx}(f)|$ is about 1.4 times (3 dB) larger with $R_{Tx} = 65 \Omega$ and $R_{Rx} = 80 \Omega$ than with 50Ω matching. However, with $R_{Tx} = 150 \Omega$ and $R_{Rx} = 80 \Omega$, the spectral shape of $|V(l, f)/I_{Tx}(f)|$ significantly differs from the example with $R_{Tx} = R_{Rx} = 50 \Omega$ for $f < 4$ GHz because (4) is not satisfied for $f < 4$ GHz: $|\eta(f)| > 0.03$ for $f < 4$ GHz [Fig. 2(c)]. With $R_{Tx} = 150 \Omega$ and $R_{Rx} = 80 \Omega$, the large ripple of $|V(l, f)/I_{Tx}(f)|$ [Fig. 2(a)] for $f < 4$ GHz is caused by the large term $1/[1 - \Gamma_{Tx}(f)\Gamma_{Rx}(f)e^{-2l\gamma(f)}]$ in (3) due to large $\eta(f)$ in this frequency range. These results verify that the signal amplitude can be increased without a significant penalty in signal integrity by relaxing the constraint of impedance matching while complying with (4).

The principle of relaxed impedance matching holds even though parasitic capacitors of interconnects are considered. Fig. 3 shows an example of a typical interconnect ($Z_C(f) = Z_0$, $Z_{Tx}(f) = R_{Tx}$, and $Z_{Rx}(f) = R_{Rx}$) with parasitic capacitors C_{par} at the Tx output and the Rx input. If the interconnect is terminated with $R_{Tx} = R_{Rx} = Z_0$ and satisfies (4), the transfer function can be approximated from (3) as

$$\frac{V(l, f)}{I_{Tx}(f)} \approx \left(\frac{Z_0}{2}\right) \left\{ \frac{1}{1 + j2\pi f C_{par} \left(\frac{Z_0}{2}\right)} \right\}^2 e^{-l\gamma(f)}. \quad (9)$$

Although $R_{Tx} \neq Z_0$ and $R_{Rx} \neq Z_0$, if (4) is satisfied, the transfer function can be approximated from (3) as

$$\begin{aligned} \frac{V(l, f)}{I_{Tx}(f)} &\approx \left(\frac{R_{Tx}Z_0}{R_{Tx} + Z_0}\right) \left\{ \frac{1}{1 + j2\pi f C_{par} \left(\frac{R_{Tx}Z_0}{R_{Tx} + Z_0}\right)} \right\} 2e^{-l\gamma(f)} \\ &\times \left\{ \frac{1}{1 + j2\pi f C_{par} \left(\frac{R_{Rx}Z_0}{R_{Rx} + Z_0}\right)} \right\} \left(\frac{R_{Rx}}{Z_0 + R_{Rx}}\right). \quad (10) \end{aligned}$$

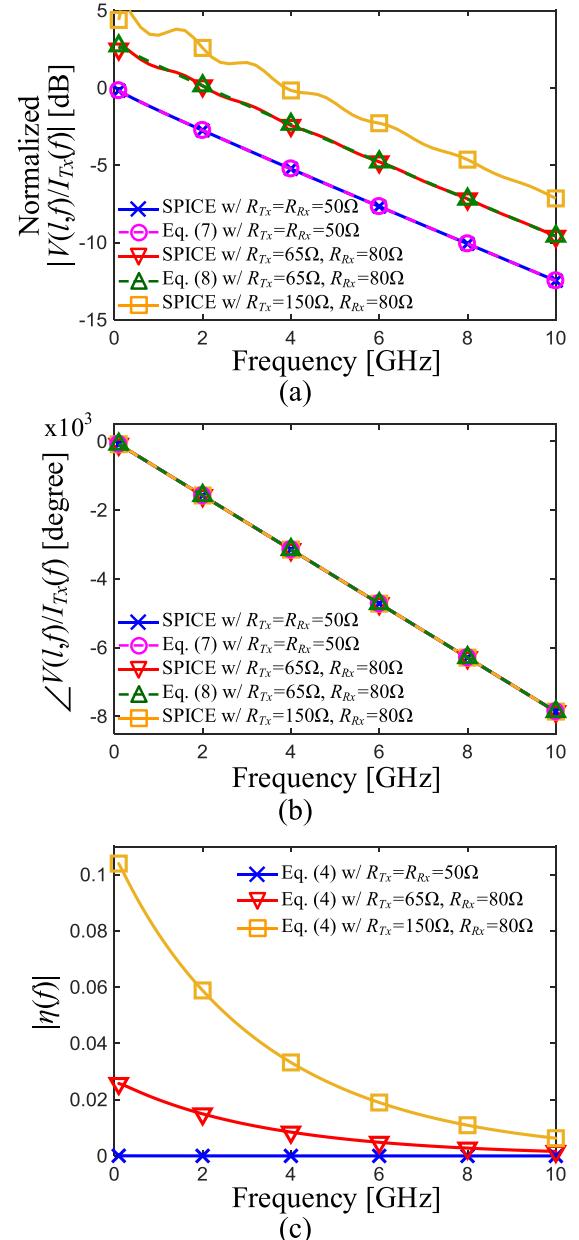


Fig. 2. (a) $|V(l, f)/I_{Tx}(f)|$, (b) $\angle V(l, f)/I_{Tx}(f)$, and (c) $|\eta(f)|$ of example interconnects (Fig. 1) with various R_{Tx} and R_{Rx} configurations. A 35-cm PCB trace with $Z_0 \approx 50 \Omega$ was commonly used. The RLGC parameters used in this interconnect are $R_o = 0.5 \Omega/m$, $R_s = 3.97 \times 10^{-4} \Omega/(m \cdot Hz)^{1/2}$, $L = 3.14 \times 10^{-7} \text{ H/m}$, $G_o = 0 \text{ S/m}$, $G_d = 1.48 \times 10^{-11} \text{ S/(m \cdot Hz)}$, and $C = 1.24 \times 10^{-10} \text{ F/m}$, respectively. $|V(l, f)/I_{Tx}(f)|$ were calculated and simulated by using (7), (8), and SPICE. $|\eta(f)|$ was calculated by using (4).

Because (4) is satisfied ($|\eta(f)|$ is small) in both examples, $1/[1 - \Gamma_{Tx}(f)\Gamma_{Rx}(f)e^{-2l\gamma(f)}]$ term in (3) causes negligible ripples in their frequency responses and thus can be ignored in (9) and (10). The spectral shapes of the transfer functions (9) and (10) are determined by $[1/[1 + j2\pi f C_{par}(Z_0/2)]]^2$ term and $[1/[1 + j2\pi f C_{par}(R_{Tx}Z_0/(R_{Tx} + Z_0))]] \times [1/[1 + j2\pi f C_{par}(R_{Rx}Z_0/(R_{Rx} + Z_0))]]$ term, respectively, together with $e^{-l\gamma(f)} = e^{-l[\alpha(f) + j\beta(f)]}$ term. Since $e^{-l\gamma(f)}$ term is common in both (9) and (10), the deviation of the spectral

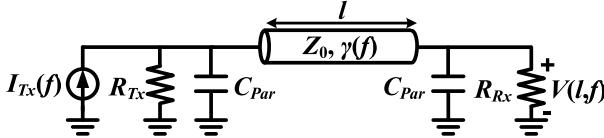


Fig. 3. Example of a typical interconnect ($Z_C(f) = Z_0$, $Z_{Tx}(f) = R_{Tx}$, and $Z_{Rx}(f) = R_{Rx}$) with parasitic capacitors C_{par} at the Tx output and the Rx input.

shape between (9) and (10) is solely determined by the other two terms. Because C_{par} is smaller than 500 fF in typical high-speed interconnects, the poles of $[1/\{1 + j2\pi f C_{par}(Z_0/2)\}]^2$ and $[1/\{1 + j2\pi f C_{par}(R_{Tx}Z_0/(R_{Tx} + Z_0))\}] \times [1/\{1 + j2\pi f C_{par}(R_{Rx}Z_0/(R_{Rx} + Z_0))\}]$ are significantly higher than the Nyquist frequency of our application. Therefore, the spectral shape of (10) is still almost identical to the one of (9) within the interesting frequency range. If the poles added by C_{par} are close enough to the Nyquist frequency so that $[1/\{1 + j2\pi f C_{par}(Z_0/2)\}]^2$ term of (9) and $[1/\{1 + j2\pi f C_{par}(R_{Tx}Z_0/(R_{Tx} + Z_0))\}] \times [1/\{1 + j2\pi f C_{par}(R_{Rx}Z_0/(R_{Rx} + Z_0))\}]$ term of (10) significantly differ within the interesting frequency range, then the relaxed impedance matching causes the additional channel roll-off penalty of $|1 + j2\pi f C_{par}(Z_0/2)|^2 [1/\{1 + j2\pi f C_{par}(R_{Tx}Z_0/(R_{Tx} + Z_0))\}] [1/\{1 + j2\pi f C_{par}(R_{Rx}Z_0/(R_{Rx} + Z_0))\}]$ for the additional dc gain of $(2R_{Tx}Z_0R_{Rx}/(R_{Tx} + Z_0)(Z_0 + R_{Rx}))$ in the frequency response (10). The additional channel roll-off is typically not large compared with the intrinsic channel roll-off by the attenuation ($|e^{-2ly(f)}| = |e^{-2\alpha(f)l}|$) along the interconnect and thus can be easily compensated by FFE. Therefore, a designer can improve the dc gain by the relaxed impedance matching at the small cost of additional channel roll-off which can be compensated by FFE if the parasitic capacitor C_{par} is not negligible within the interesting frequency range.

The simulation also verifies our theoretical analysis on the relaxed impedance matching with the parasitic capacitors. Fig. 4 shows $|V(l, f)/I_{Tx}(f)|$ and $\angle V(l, f)/I_{Tx}(f)$ of example interconnects in Fig. 3 with impedance matching ($R_{Tx} = R_{Rx} = 50 \Omega$) and relaxed impedance matching ($R_{Tx} = 65 \Omega$ and $R_{Rx} = 80 \Omega$). For both interconnects, $C_{par} = 500$ fF and $Z_0 = 50 \Omega$ are used. Because $|\eta(f)|$ is small (Fig. 5), both examples satisfy (4). As a result, the ripples in their frequency responses $|V(l, f)/I_{Tx}(f)|$ are negligible [Fig. 4(a)]. Due to C_{par} , the transfer function of the example interconnect with $R_{Tx} = R_{Rx} = 50 \Omega$ has two identical poles at about 12.7 GHz while the one with $R_{Tx} = 65 \Omega$ and $R_{Rx} = 80 \Omega$ has two poles at about 10.3 and 11.3 GHz. Although the poles (10.3 and 11.3 GHz) with $R_{Tx} = 65 \Omega$ and $R_{Rx} = 80 \Omega$ locate at lower frequencies than the one (12.7 GHz) with $R_{Tx} = R_{Rx} = 50 \Omega$, their frequencies are still much higher than the Nyquist frequency of our application (6 GHz). Therefore, the spectral shapes of $|V(l, f)/I_{Tx}(f)|$ and $\angle V(l, f)/I_{Tx}(f)$ with relaxed impedance matching ($R_{Tx} = 65 \Omega$ and $R_{Rx} = 80 \Omega$) are still similar to the ones with impedance matching ($R_{Tx} = R_{Rx} = 50 \Omega$) [Fig. 4(a) and (b)]. The additional channel roll-off penalty

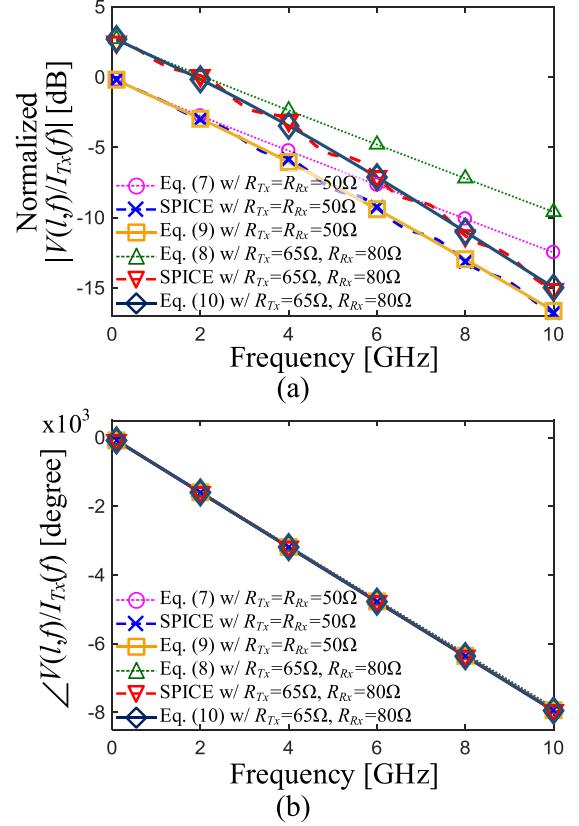


Fig. 4. (a) $|V(l, f)/I_{Tx}(f)|$ and (b) $\angle V(l, f)/I_{Tx}(f)$ of example interconnects (Fig. 3) with various R_{Tx} and R_{Rx} configurations. A 35-cm PCB trace with $Z_0 \approx 50 \Omega$ was commonly used. C_{par} were 500 fF. $|V(l, f)/I_{Tx}(f)|$ were calculated and simulated by using (9), (10), and SPICE. For comparison, $|V(l, f)/I_{Tx}(f)|$ and $\angle V(l, f)/I_{Tx}(f)$ of the previous examples (without C_{par}) shown in Fig. 2 are also plotted.

by the relaxed impedance matching is calculated from the frequency responses normalized with respect to their dc gains. The simulated channel roll-off penalty is only about 0.61 dB at the Nyquist frequency (6 GHz) while $|V(l, f)/I_{Tx}(f)|$ is about 1.3 times (2.28 dB) larger at 6 GHz with $R_{Tx} = 65 \Omega$ and $R_{Rx} = 80 \Omega$ than with 50Ω -matching [Fig. 4(a)]. This result verifies that the signal amplitude can be increased by relaxing the constraint of impedance matching while complying with (4) even with the parasitic capacitors.

Fig. 5 shows why signal integrity is preserved by relaxed impedance matching even though parasitic capacitors cause large reflection at high frequency. Fig. 5 shows $|\eta(f)|$, $|\Gamma_{Tx}(f)|$, $|\Gamma_{Rx}(f)|$, and $|e^{-2ly(f)}| = |e^{-2\alpha(f)l}|$ of the example interconnects in Fig. 3 with impedance matching ($R_{Tx} = R_{Rx} = 50 \Omega$) and with relaxed impedance matching ($R_{Tx} = 65 \Omega$, $R_{Rx} = 80 \Omega$), both of which are used in Fig. 4. The parasitic capacitors at both terminals ($C_{par} = 500$ fF) are included in the calculation. Due to the impedance mismatch caused by C_{par} , $|\Gamma_{Tx}(f)|$ and $|\Gamma_{Rx}(f)|$ increase as the frequency increases. At the Nyquist frequency (6 GHz), the interconnect with relaxed impedance matching ($R_{Tx} = 65 \Omega$ and $R_{Rx} = 80 \Omega$) has large $|\Gamma_{Tx}(f)|$ of 0.49 and $|\Gamma_{Rx}(f)|$ of 0.55 (Fig. 5), and they are even larger at higher frequency. Even with $R_{Tx} = R_{Rx} = 50 \Omega$, the reflection coefficients are large ($|\Gamma_{Tx}(f)| = |\Gamma_{Rx}(f)| = 0.43$ at 6 GHz),

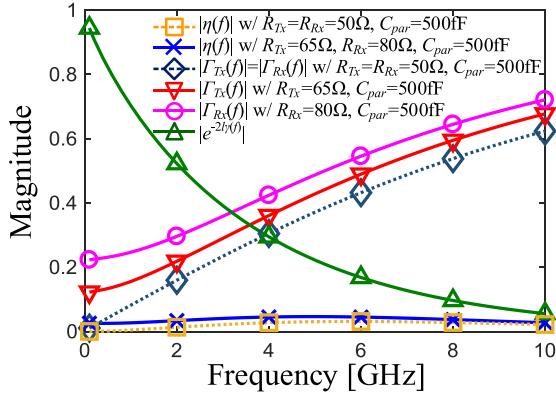


Fig. 5. $|\eta(f)|$, $|\Gamma_{Tx}(f)|$, $|\Gamma_{Rx}(f)|$, and $|e^{-2l\gamma(f)}| = |e^{-2\alpha(f)l}|$ of example interconnects (Fig. 3) with a 35-cm 50- Ω PCB trace, $C_{par} = 500\text{ fF}$, and various R_{Tx} and R_{Rx} configurations: 1) $R_{Tx} = R_{Rx} = 50\Omega$ and 2) $R_{Tx} = 65\Omega$ and $R_{Rx} = 80\Omega$.

showing that the conventional impedance matching cannot reduce large reflection due to the impedance discontinuity by the parasitic capacitors at high frequency. The fact that such large reflection coefficients in Fig. 5 do not cause serious signal integrity problems in Fig. 4 might be counter-intuitive according to the conventional impedance matching theory. These large reflections must be reduced to prevent a serious signal integrity problem in the conventional impedance matching approach. However, the principle of relaxed impedance matching is not violated in Fig. 5 because $|e^{-2l\gamma(f)}| (= |e^{-2\alpha(f)l}|)$, which is small in the frequency region where the reflection coefficients $|\Gamma_{Tx}(f)|$ and $|\Gamma_{Rx}(f)|$ are large, makes $|\eta(f)| (= |\Gamma_{Tx}(f)| \times |\Gamma_{Rx}(f)| \times |e^{-2l\gamma(f)}|)$ small in all frequency regions of interest (Fig. 5). At low frequency, $|\eta(f)|$ is small even though $|e^{-2l\gamma(f)}| (= |e^{-2\alpha(f)l}|)$ is large because $|\Gamma_{Tx}(f)|$ and $|\Gamma_{Rx}(f)|$ are small due to the small admittances of the parasitic capacitors. At high frequency, $|\eta(f)|$ is small, although $|\Gamma_{Tx}(f)|$ and $|\Gamma_{Rx}(f)|$ are large because $|e^{-2l\gamma(f)}| (= |e^{-2\alpha(f)l}|)$ is small. Because $|\eta(f)|$ is small in all frequency regions, the signal integrity is preserved even with large reflection by the parasitic capacitors at high frequency. It is noticeable that the conventional impedance matching which has large reflection coefficients also implicitly relies on the principle of relaxed impedance matching (Figs. 4 and 5).

C. Range of the Transmitter Impedance Complying With Relaxed Impedance Matching

The range of R_{Tx} complying with relaxed impedance matching (4) is derived for a given arbitrary R_{Rx} , channel parameters ($l, \gamma(f) = \alpha(f) + j\beta(f)$, and Z_0), and a target upper bound K of the penalty $|\eta(f)|$ in signal integrity. If $|\eta(f)|$ is bounded by a given positive number K

$$|\eta(f)| = |\Gamma_{Tx}(f)\Gamma_{Rx}(f)e^{-2l\gamma(f)}| \leq K. \quad (11)$$

Because R_{Tx} , Z_0 , and R_{Rx} are positive real numbers, we can easily solve (11) for R_{Tx} as

$$\begin{cases} Z_0 \left(\frac{A - K}{A + K} \right) \leq R_{Tx} \leq Z_0 \left(\frac{A + K}{A - K} \right), & \text{if } 0 \leq K < A \\ 0 \leq R_{Tx} \leq \infty, & \text{if } A \leq K \end{cases} \quad (12)$$

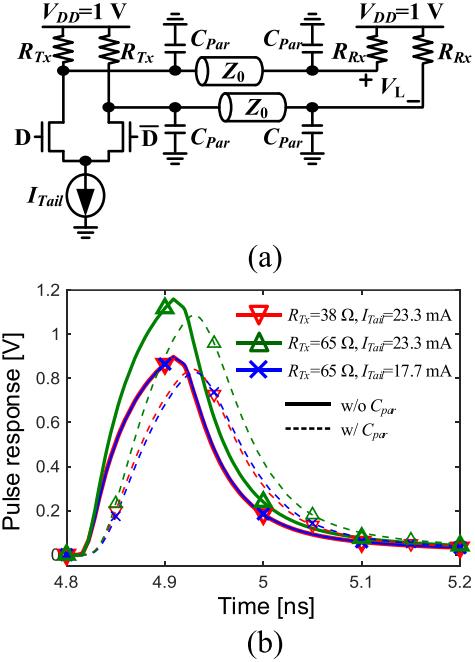


Fig. 6. (a) Example interconnect with a CML Tx, a 35-cm 50- Ω PCB trace, and an 80- Ω Rx. (b) Simulated received signals of (a) with $R_{Tx} = 38\Omega$ and $R_{Tx} = 65\Omega$ when a 100-ps-wide pulse is transmitted. The wire attenuation at the Nyquist frequency ($f = 5\text{ GHz}$) is 6.5 dB. The pulse responses are obtained by SPICE simulation. Voltage levels of the received pulses in Fig. 6(b) are adjusted for easy comparison.

where $A = |\Gamma_{Rx}e^{-2l\gamma(f)}|$. As explained earlier, the R_{Tx} value within the range (12) makes the deviation of the spectral shape with respect to the one with impedance matching bounded by K . It is also noticeable that any R_{Tx} value would tightly bound $|\eta(f)|$ if the Rx is matched ($|\Gamma_{Rx}| = 0$) or the channel attenuation is large ($|e^{-2l\gamma(f)}| = |e^{-2\alpha(f)l}|$ is small).

D. Impedance Relaxation for CML Transmitters

For a CML Tx, the largest R_{Tx} that complies with relaxed impedance matching is preferable because it maximizes the signal amplitude with a negligible penalty in signal integrity.

Fig. 6(a) shows an example link with a CML Tx, a 35-cm 50- Ω printed-circuit-board (PCB) trace, and an 80- Ω Rx. For a target upper bound K of 0.03, the R_{Tx} range that makes $|\eta(f)| \leq K = 0.03$ for all frequencies is calculated from (12). R_{Tx} must satisfy (12) in a broad frequency band because a broadband signaling such as non-return-to-zero (NRZ) is typically used for high-speed links. For this reason, $|e^{-2l\gamma(f)}| = |e^{-2\alpha(f)l}| = 1$ is used to calculate R_{Tx} range with (12) because the tightest bound of (12) is set by the largest value of $|e^{-2l\gamma(f)}| (= 1)$ which occurs at dc; $|e^{-2l\gamma(f)}| = 1$ when $f = 0$. The calculated R_{Tx} range is $38\Omega \leq R_{Tx} \leq 65\Omega$. Fig. 6(b) compares simulated received signals of Fig. 6(a) with and without C_{par} when a 100-ps-wide pulse is transmitted. To show the benefit of the relaxed impedance matching, the received signals were simulated for both the maximum and the minimum R_{Tx} values satisfying the relaxed impedance constraint: 38 and 65 Ω . Regardless of C_{par} , with the same Tx's tail current of $I_{Tail} = 23.3\text{ mA}$,

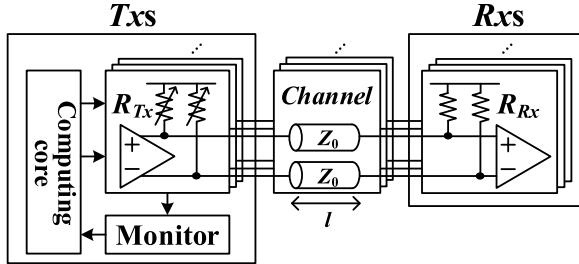


Fig. 7. Link overview.

the amplitude is about 1.3 times larger with $R_{Tx} = 65 \Omega$ than with $R_{Tx} = 38 \Omega$. When I_{Tail} of the $R_{Tx} = 65 \Omega$ example is reduced to 17.7 mA, the received signals of the two examples become almost identical [Fig. 6(b)], proving that the relaxed impedance matching constraint preserves the spectral shape of the transfer function. It also implies that the interconnect with $R_{Tx} = 65 \Omega$ consumes only 76% power of the one with $R_{Tx} = 35 \Omega$ for the same amplitude.

The simulation results can be also theoretically interpreted by (8). $|V(l, f)/I_{Tx}(f)|$ in (8) is proportional to $R_{Tx}Z_0/(R_{Tx} + Z_0)$. Because $R_{Tx}Z_0/(R_{Tx} + Z_0)$ is 1.31 times larger with $R_{Tx} = 65 \Omega$ than with $R_{Tx} = 38 \Omega$, the simulated pulse response is 1.31 times larger with $R_{Tx} = 65 \Omega$ than with $R_{Tx} = 38 \Omega$ for the same I_{Tail} . Similarly, we can explain why $R_{Tx} = 65 \Omega$ requires less I_{Tail} than $R_{Tx} = 38 \Omega$ for the same amplitude.

III. CIRCUIT DESIGN

In this section, we describe the design of the proposed FFE Tx which adapts to arbitrary impedances of channels and Rxs by automatically configuring R_{Tx} . Fig. 7 illustrates an overview of a link exploiting the proposed Txs that are connected to arbitrary channels and Rxs. For R_{Tx} configuration, first, Z_0 and R_{Rx} are detected by an on-chip TDR monitor, and then used to calculate the optimal R_{Tx} that complies with relaxed impedance matching for an upper bound $K = 0.03$ in (12). Last, R_{Tx} is automatically configured to the optimal value. After R_{Tx} configuration, the monitor is totally shut down to save power.

The proposed method is implemented with a four-tap FFE Tx and an on-chip TDR monitor (Fig. 8). The Tx was designed in typical half-rate architecture consisting of two ways of half-rate latches, multiplexers (MUXs), and a CML driver. The TDR monitor consists of a slicer, a 96-bit snapshot, and a finite-state machine (FSM). The monitor can be shared by many Txs to amortize the hardware cost.

In normal operation, the configuration MUXs (C-MUXs) select the data from the serializing MUXs (S-MUXs), and the Tx operates as a typical four-tap FFE. In this mode, the monitor is in idle state to save power. During adaptation, the C-MUXs override the data from S-MUXs with control bits required by the detection algorithm which will be explained in Section IV. In this mode, the Tx output voltage is observed by the monitor and the result is fed to the FSM to detect R_{Rx} and Z_0 . Based on the detected R_{Rx} and Z_0 , the FSM automatically configures R_{Tx} to the optimal value.

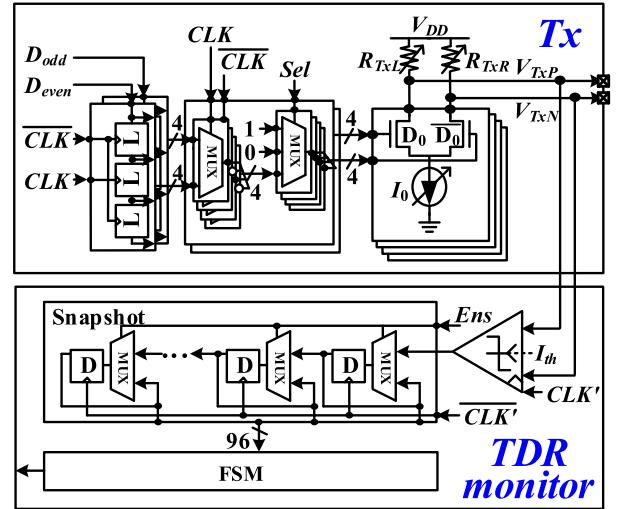


Fig. 8. Simplified schematics of the proposed Tx and the TDR monitor.

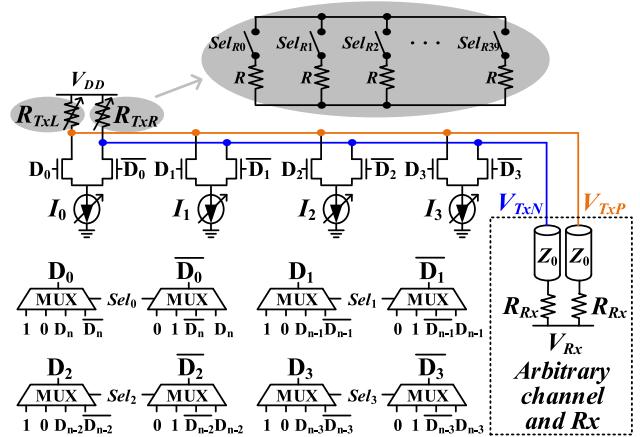


Fig. 9. Detailed schematic of the driver and C-MUXs in Fig. 8.

Fig. 9 shows the detailed schematic of the CML driver and the C-MUXs. The termination resistance can be configured between 30 and 200 Ω . This range does not require extra hardware cost because process variation also requires a similar configuration range of R_{Tx} . Inputs to the C-MUXs are "1," "0," and the both conjugate data from the S-MUXs (D_i and \bar{D}_i). C-MUXs can flip the tap polarities and also turn them off by appropriate selection of inputs. Although a typical CML driver is exploited in this paper, other types of drivers such as a source-series termination driver [17] would be also used in a similar fashion to implement the proposed method.

The front end of the TDR monitor is a slicer consisting of a pre-amplifier with a tunable threshold and a sense amplifier followed by a dynamic-balanced S-R latch (Fig. 10). The input of the slicer is the Tx output voltage, and the slicer output is fed to the following 96-bit snapshot [18]–[20], which has fast enabling and disabling the ability (Fig. 8). When the snapshot is disabled, 96 consecutive sliced bits are held, and the FSM can read these bits reliably at low speed (Fig. 8).

Fig. 11 describes a timing-control circuit for the snapshot and the timing diagrams of the control signals. The snapshot is

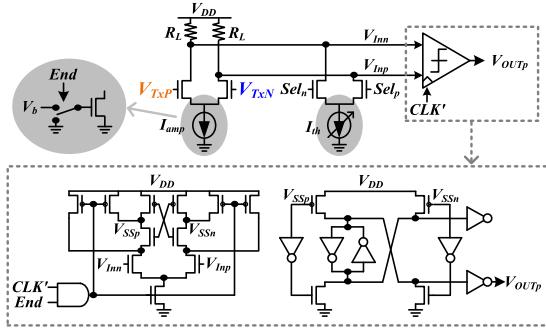


Fig. 10. Detailed schematic of the slicer in the TDR monitor.

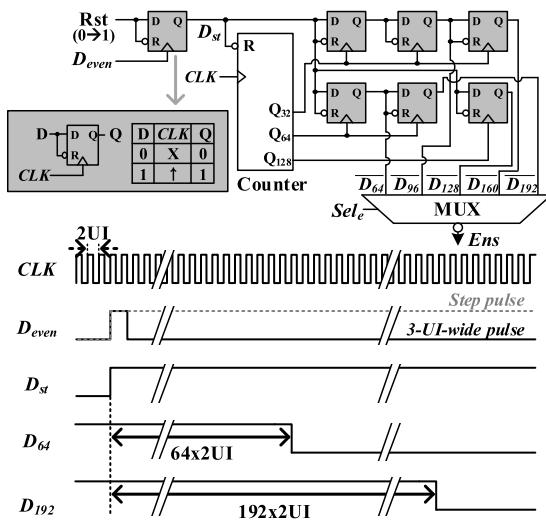


Fig. 11. Timing-control circuit for the snapshot and the timing diagrams of the control signals.

enabled by the first transition of the transmitted data D_{even} and then disabled after 64–192 clock cycles, which corresponds to 128–384 unit interval (UI). The wide programmable range of the delay of the disabling signal increases the range of applicable channel length of the proposed method, which will be explained in Section IV. The impedance adaptation and relaxation relies on the monitoring of the reflected signal that is originally transmitted by the Tx, and reflected at the Rx and travels back toward the Tx, and observed at the Tx. By appropriately delaying the disabling signal for the snapshot, the observable timing window (192 UI) of the monitor can be adjusted for the arrival time of the reflected signal depending on the channel length.

IV. ADAPTATION ALGORITHM

Fig. 12 shows a flowchart of the R_{Tx} adaptation algorithm. In step 1, the Rx's termination impedance R_{Rx} and voltage V_{Rx} are detected. In step 2, the flight time t_f is detected by observing the Tx output voltage after transmitting a 3-UI-wide square pulse. If t_f is detected, then the TDR monitor detects the channel's characteristic impedance Z_0 by observing the Tx output voltage after transmitting a step pulse in step 3. If t_f is not detected, R_{Tx} is automatically configured to its maximum

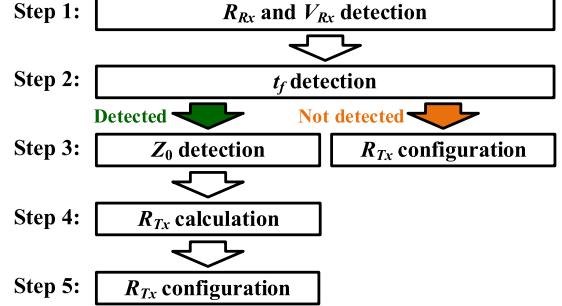


Fig. 12. Flowchart of the R_{Tx} adaptation algorithm.

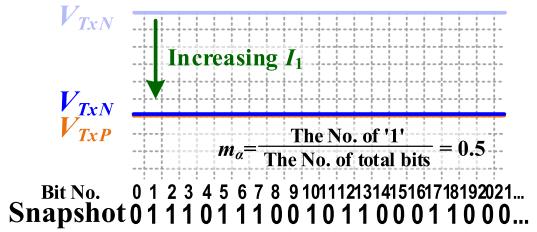


Fig. 13. Example illustration of R_{Rx} and V_{Rx} detection procedure. The bit sequence of the monitor output is also illustrated.

value and the adaptation algorithm finishes. In step 4, from the detected R_{Rx} and Z_0 , the optimal R_{Tx} value is calculated by using (12). Finally, the R_{Tx} is automatically configured to the optimal value. The details of detection algorithm are described in the following sections.

A. Rx's Termination Impedance and Voltage Detection

R_{Rx} and V_{Rx} are detected by observing the Tx output voltage at dc with various R_{Tx} and tap current settings.

For this detection, the first and the second taps (I_0 and I_1) are, respectively, configured to set the dc voltage levels of V_{TxP} and V_{TxN} by setting $D_0 = 1$ and $D_1 = 0$ whereas other taps (I_2 and I_3) are turned off (Fig. 9). Also, R_{TxL} and R_{TxR} are set to two different resistance values ($R_{TxL} = R_{TxLa}$ and $R_{TxR} = R_{TxRa}$) and I_0 is set to an arbitrary value ($I_0 = I_{0a}$). If we know the I_1 value ($I_1 = I_{1a}$) that makes $V_{TxP} = V_{TxN}$ with this configuration, then we can acquire the following equation for R_{Rx} and V_{Rx} as:

$$\begin{aligned} & \left(\frac{1}{R_{TxLa} + R_{Rx}} \right) (R_{Rx} V_{DD} + R_{TxLa} V_{Rx} - R_{TxLa} R_{Rx} I_{0a}) \\ &= \left(\frac{1}{R_{TxRa} + R_{Rx}} \right) (R_{Rx} V_{DD} + R_{TxRa} V_{Rx} - R_{TxRa} R_{Rx} I_{1a}). \end{aligned} \quad (13)$$

I_{1a} can be found by examining bit average m_a (defined in Fig. 13) of the monitor output while sweeping I_1 as illustrated in Fig. 13. When $V_{TxP} = V_{TxN}$, the bit stream of the slicer output contains almost equal numbers of “1” and “0” resulting in $m_a \approx 0.5$.

Similarly, by finding another I_1 value ($I_1 = I_{1b}$) that makes $V_{TxP} = V_{TxN}$ with a different configuration ($R_{TxL} = R_{TxLb}$, $R_{TxR} = R_{TxRb}$, $I_0 = I_{0b}$), another equation

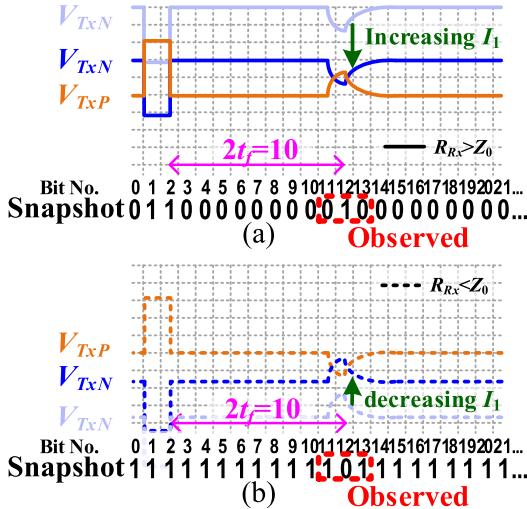


Fig. 14. Example illustrations of t_f detection procedures when (a) $R_{Rx} > Z_0$ and (b) $R_{Rx} < Z_0$. The bit sequence of the monitor output is also illustrated.

for R_{Rx} and V_{Rx} can be obtained as follows:

$$\begin{aligned} & \left(\frac{1}{R_{TxLb} + R_{Rx}} \right) (R_{Rx} V_{DD} + R_{TxLb} V_{Rx} - R_{TxLb} R_{Rx} I_{0b}) \\ &= \left(\frac{1}{R_{TxRb} + R_{Rx}} \right) (R_{Rx} V_{DD} + R_{TxRb} V_{Rx} - R_{TxRb} R_{Rx} I_{1b}). \end{aligned} \quad (14)$$

From (13) and (14), formulas of R_{Rx} and V_{Rx} can be acquired as

$$R_{Rx} = \frac{-R_{TxLa} R_{TxRa} \Delta I_a \Delta_{RTxb} + R_{TxLb} R_{TxRb} \Delta I_b \Delta_{RTxa}}{\Delta V_a \Delta_{RTxb} - \Delta V_b \Delta_{RTxa}} \quad (15)$$

$$V_{Rx} = V_{DD} - \frac{R_{TxLa} R_{TxRa} \Delta I_a \Delta V_b - R_{TxLb} R_{TxRb} \Delta I_b \Delta V_a}{\Delta V_a \Delta_{RTxb} - \Delta V_b \Delta_{RTxa}} \quad (16)$$

where $\Delta I_a = I_{0a} - I_{1a}$, $\Delta I_b = I_{0b} - I_{1b}$, $\Delta_{RTxa} = R_{TxLa} - R_{TxRa}$, $\Delta_{RTxb} = R_{TxLb} - R_{TxRb}$, $\Delta V_a = I_{0a} R_{TxLa} - I_{1a} R_{TxRa}$, and $\Delta V_b = I_{0b} R_{TxLb} - I_{1b} R_{TxRb}$.

B. Flight Time Detection

t_f is detected by observing reflection of a transmitted square pulse.

For t_f detection, R_{TxL} and R_{TxR} are set to the same resistance value ($R_{TxL} = R_{TxR}$) in Fig. 9. A 3-UI-wide square pulse is transmitted with the first tap I_0 by feeding $D_0 = \dots 111000111\dots$ while the initial differential voltage level of the transmitted pulse is adjusted by the second tap I_1 with $D_1 = 0$. Other taps (I_2 and I_3) are turned off. The transmitted pulse propagates along the channel, and reflected at the Rx. The reflected voltage returns to the Tx again at $2t_f$ after the original transmission of the pulse. By detecting the arrival time of the reflected signal, we can acquire t_f . Since t_f is not sensitive to the pulse width and the required accuracy is not high, the pulse width of 3 UI is chosen to relieve the timing requirement for the monitor.

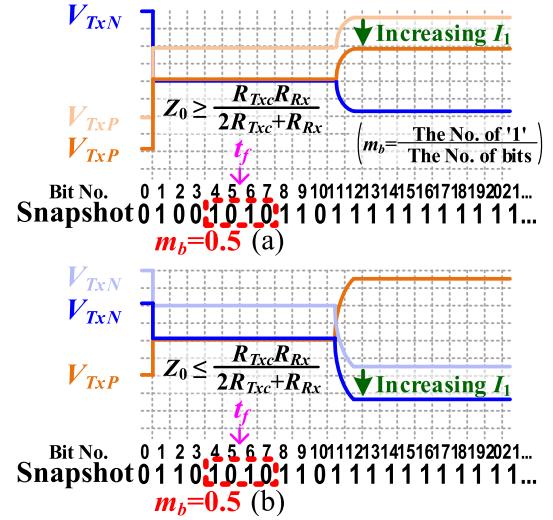


Fig. 15. Example illustrations of Z_0 detection procedures when (a) $Z_0 \geq R_{Txc} R_{Rx} / (2R_{Txc} + R_{Rx})$ and (b) $Z_0 \leq R_{Txc} R_{Rx} / (2R_{Txc} + R_{Rx})$.

The arrival time of the reflected signal can be easily detected by searching for the position of a “010” or “101” bit pattern in the 96 bits of the monitor output while sweeping I_1 . Fig. 14 illustrates two examples of this procedure. First, the monitor searches for the “010” bit pattern by increasing I_1 from its minimum value [Fig. 14(a)]. If $R_{Rx} > Z_0$, the reflected signal is a positive pulse and the “010” pattern can be found. Otherwise ($R_{Rx} < Z_0$), the reflected signal is a negative pulse, and thus the “010” pattern cannot be found. In this case, the monitor searches for “101” bit pattern by decreasing I_1 from its maximum value [Fig. 14(b)]. Once “010” or “101” bit pattern is found, its position corresponds to $2t_f$ (Fig. 14). If neither “010” nor “101” bit pattern is found because the reflected signal is too small, the adaptation algorithm finishes and R_{Tx} is automatically set to its maximum value; relaxed impedance matching (4) is already satisfied regardless of R_{Tx} .

C. Detection of the Characteristic Impedance of the Channel

For Z_0 detection, R_{TxL} and R_{TxR} are set to the same resistance value ($R_{TxL} = R_{TxR} = R_{Txc}$) and I_0 is set to an arbitrary value $I_0 = I_{0c}$ in Fig. 9. A step pulse is transmitted with the first tap by feeding $D_0 = \dots 111000\dots$ while the step height is determined by I_{0c} and the initial differential voltage level is adjusted by I_1 and D_1 configuration (Fig. 15). I_2 and I_3 are turned off.

Z_0 is detected by observing the Tx output voltage at around t_f after transmitting a step pulse. Before the reflected signal arrives to the Tx at around $2t_f$, the channel behaves like a resistor with resistance of Z_0 . Therefore, the differential Tx output voltage (V_{diff1}) at around t_f can be expressed as $V_{diff1} = 2I_{0c}(R_{Txc}Z_0/(R_{Txc} + Z_0))$ (Fig. 15). By using this, we can acquire Z_0 by detecting V_{diff1} .

V_{diff1} can be detected by searching for the I_1 value ($I_1 = I_{1c}$) that makes $V_{TxP} = V_{TxN}$ at around t_f . Fig. 15 illustrates examples of this procedure. First, the monitor searches

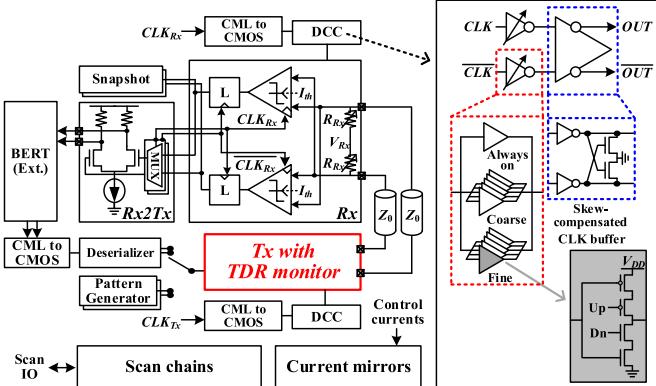


Fig. 16. Test-support blocks and the test setup.

for I_{1c} by increasing I_1 with $D_1 = 1$ [Fig. 15(a)]. If $Z_0 \leq R_{Txc}R_{Rx}/(2R_{Txc} + R_{Rx})$, I_{1c} may not be found in this search. If so, the monitor searches for I_{1c} by increasing I_1 with $D_1 = 0$ [Fig. 15(b)]. Theoretically, I_{1c} can be always found by one of the two searches. Similar to R_{Rx} and V_{Rx} detection, $V_{TxP} = V_{TxN}$ at $\sim t_f$ can be easily examined by the bit average m_b (defined in Fig. 15) of the monitor output at $\sim t_f$: $m_b \approx 0.5$ if $V_{TxP} = V_{TxN}$. Once I_{1c} is found, V_{diff1} can be calculated as

$$V_{diff1} = \begin{cases} (I_{0c} + I_{1c}) \left(\frac{R_{Txc}R_{Rx}}{R_{Txc} + R_{Rx}} \right), & \text{if } Z_0 \geq \frac{R_{Txc}R_{Rx}}{2R_{Txc} + R_{Rx}} \\ (I_{0c} - I_{1c}) \left(\frac{R_{Txc}R_{Rx}}{R_{Txc} + R_{Rx}} \right), & \text{if } Z_0 \leq \frac{R_{Txc}R_{Rx}}{2R_{Txc} + R_{Rx}}. \end{cases} \quad (17)$$

In (17), R_{Txc} and I_{0c} are known values, and R_{Rx} is already detected in the first step. By substituting (17) with $V_{diff1} = 2I_{0c}(R_{Txc}Z_0/(R_{Txc} + Z_0))$ and solving it for Z_0 , we can obtain Z_0 as

$$Z_0 = \begin{cases} \frac{R_{Txc}R_{Rx}(I_{0c} + I_{1c})}{2I_{0c}R_{Txc} + (I_{0c} - I_{1c})R_{Rx}}, & \text{if } Z_0 \geq \frac{R_{Txc}R_{Rx}}{2R_{Txc} + R_{Rx}} \\ \frac{R_{Txc}R_{Rx}(I_{0c} - I_{1c})}{2I_{0c}R_{Txc} + (I_{0c} + I_{1c})R_{Rx}}, & \text{if } Z_0 \leq \frac{R_{Txc}R_{Rx}}{2R_{Txc} + R_{Rx}}. \end{cases} \quad (18)$$

V. EXPERIMENT

To verify the impedance adaptation and relaxation scheme, we fabricated the proposed Tx (Fig. 8) and test-support blocks (Fig. 16) in 65-nm bulk CMOS technology. Fig. 17 shows its die micrograph. The Tx core and the monitor occupy $91 \times 81 \mu\text{m}^2$ and $198 \times 72 \mu\text{m}^2$, respectively. The test chip was packaged using a chip-on-a-board (COB) assembly [Fig. 18(a)] on three different 35-cm PCB traces with $Z_0 = 35, 50$, and 75Ω . Fig. 18(b) shows the *in-situ* measured frequency responses of the PCB traces with bond wires and PADs. The frequency responses have a notch at around 5.5 GHz caused by the bond wires and PADs. This shows that the channels used in the experiment have impedance discontinuity and mismatch. Fig. 16 shows the test setup with the test-support blocks. For various tests with various R_{Rx} values, an Rx with tunable threshold voltage and termination resistors

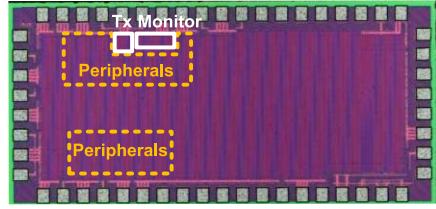
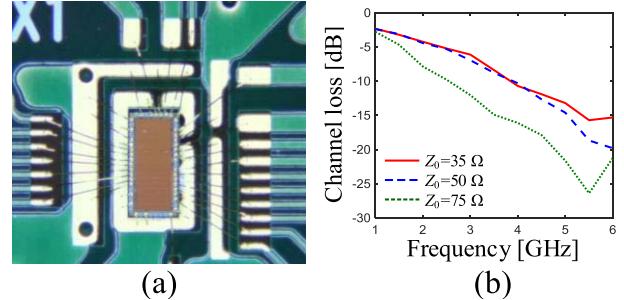
Fig. 17. Die micrograph ($1 \times 2 \text{ mm}^2$).

Fig. 18. (a) COB micrograph used in the experiment and (b) *in-situ* measured frequency responses of the 35-cm PCB traces ($Z_0 = 35, 50$, and 75Ω) with bond wires and PADs. The frequency responses in Fig. 18(b) were measured when $R_{Tx} = R_{Rx} = Z_0$. Then, the dc losses caused by terminations were adjusted.

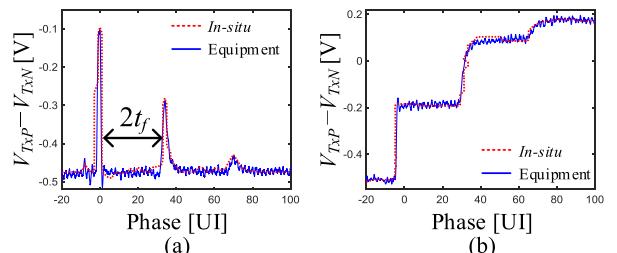


Fig. 19. Tx output voltages measured by the TDR monitor and by an equipment at 8 Gb/s while transmitting (a) square pulse and (b) step with $Z_0 = 35 \Omega$ and $R_{Rx} = 200 \Omega$ (sample 1 in Fig. 20).

whose resistance can be configured between 30 and 200Ω were implemented. The data were sourced from either an internal pattern generator or an external bit-error rate tester (BERT). The Rx retransmits the recovered data to the BERT using a simple CML Tx (Rx2Tx in Fig. 16) for bit-error rate testing. The Tx and Rx clocks were provided by clock generators which are synchronized with the BERT. Duty-cycle correctors (DCCs), each of which adjusts rising/falling delays, were utilized for both Tx and Rx clocks. All digital-control bits were interfaced by scan chains via slow I/Os while reference currents were externally provided.

With various configurations, the Tx was tested with 1-V supply, and the results are shown in Figs. 19–25 and Table I.

Fig. 19 shows the Tx output voltage measured using the TDR monitor and the corresponding voltage measured at the near end of the channel using an equipment while transmitting square and step pulses. The same impedance configuration of sample 1 in Fig. 20 were used: $Z_0 = 35 \Omega$ and $R_{Rx} = 200 \Omega$. Fig. 19(a) clearly shows the reflected pulse at ~ 34 UI, which

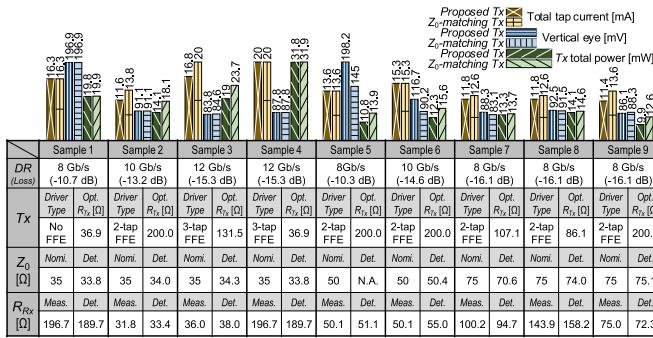


Fig. 20. Summary of the proposed Tx's adaption ability test. DR : data rate. $Opt.$: optimal values of the Tx impedance configured by impedance adaptation. *Nomi.*: the nominal designed values that may differ from the real quantities. *Det.*: values detected by the TDR monitor. *Meas.*: values measured with multi-meters.

causes the second step at ~ 34 UI in Fig. 19(b). The detected t_f is 17 UI. This measurement justifies that the detection algorithm is suitable to the shape of the reflected signal.

The detectable range of the channel is limited by the shape and position of the reflection signal. If the channel is too short and thus the reflected pulse returns to the Tx too soon, then it may overlap with the original transmitted pulse. Also, if the channel is too long, and thus the reflected pulse returns to the Tx too late, the reflected pulse may not be recorded in the snapshot sequence of the monitor. In both cases, the Tx will fail to detect t_f , and thus it cannot be applied to such channels. In this design, a 3-UI-wide square pulse is transmitted with a half-rate clock of 6 GHz (1 UI = 83.33 ps), and the detectable t_f range is $1.5 \text{ UI} \leq t_f \leq 192 \text{ UI}$, which corresponds to $0.125 \text{ ns} \leq t_f \leq 16 \text{ ns}$. The corresponding detectable range of the channel length is between 2.02 and 258.46 cm. Since the detectable t_f range scales with the clock period, the minimum (maximum) detectable channel length can be easily reduced (increased) shorter (longer) than 2.02 cm (258.46 cm) by increasing (decreasing) the clock frequency if necessary. The minimum detectable channel length can be further reduced by using a square pulse narrower than 3 UI to reduce the minimum detectable t_f below 1.5 UI.

The adaptation ability of the Tx is tested with nine different combinations (samples) of Z_0 ($35\text{--}75 \Omega$) and R_{Rx} ($30\text{--}200 \Omega$). The results are summarized in Fig. 20. In all tests, Z_0 and R_{Rx} were accurately detected by the monitor within 10% error, compared with both their nominal (*Nomi.*) and measured (*Meas.*) values; *Nomi.* and *Meas.* are explained in Fig. 20. When R_{Tx} is automatically set to the optimal value calculated from the detected Z_0 and R_{Rx} , large eye diagrams were measured *in-situ* (Fig. 21). These results verify that the Tx can successfully adapt to various channels and Rxs.

For the same nine configurations, we also compared the proposed Tx and the conventional Z_0 -matching Tx ($R_{Tx} = Z_0$). Eye diagrams and total tap currents of both Txs are measured at the highest achieved data rate of 12 Gb/s and compared in Fig. 22; this result corresponds to the sample 3 in Fig. 20. For the similar eye sizes, our Tx requires only 84% total tap current of the Z_0 -matching Tx. Comparison

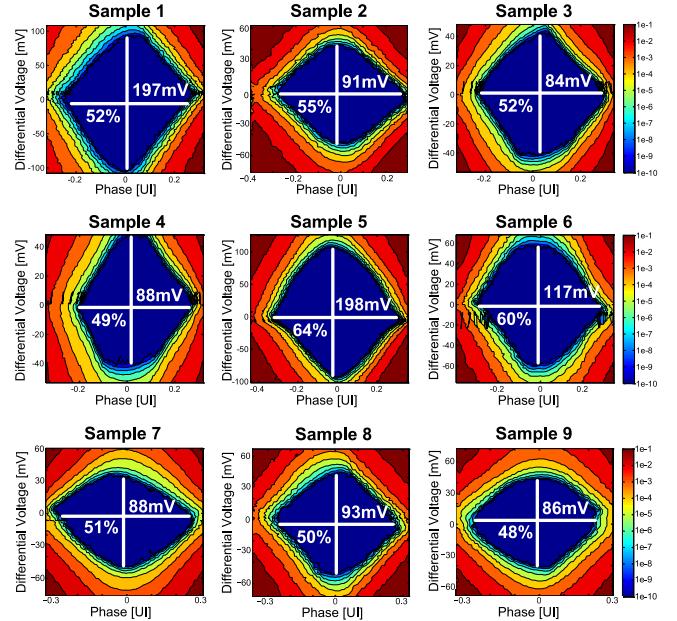


Fig. 21. Eye diagrams measured *in-situ* at the Rx when the Tx is transmitting data. These results correspond to the nine samples in Fig. 20.

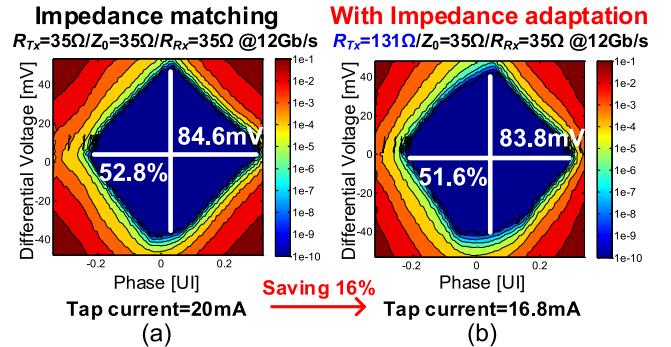


Fig. 22. Eye diagrams measured *in-situ* at the Rx when (a) Z_0 -matching Tx and (b) proposed Tx are used. Eye diagrams were measured *in-situ* at 12 Gb/s with 35Ω Rx and a 35Ω channel. This configuration is the same as in the sample 3 in Fig. 20. The channel loss of 15.3 dB was measured at 6 GHz. The Z_0 -matching Tx was manually terminated by $R_{Tx} = 35 \Omega$ while the proposed Tx automatically configured R_{Tx} to 131Ω .

results for eight other configurations are also summarized in Fig. 20. In all tests, the proposed Tx consumed the same or less total tap currents than Z_0 -matching Tx even though the former obtained the same or larger vertical eye sizes. In addition, our Tx achieved the same or better power efficiency compared with Z_0 -matching Tx. These results verify that the proposed Tx can adapt to various impedances of the channels and Rxs while achieving the same or better eye size and power efficiency compared with the Z_0 -matching Tx.

The proposed Tx's adaptation ability to arbitrary channels and Rxs was compared with standard Txs at 8 Gb/s. When 50- and 75- Ω standard Txs are blindly connected to a 35Ω channel and a 200Ω Rx, the impedance mismatch of the Txs reduces vertical eye sizes from 197 mV (Z_0 -matching that corresponds to sample 1 in Fig. 20) to 130 mV [Fig. 23(b)] and to 52 mV [Fig. 23(a)], respectively. If the Tx attempts

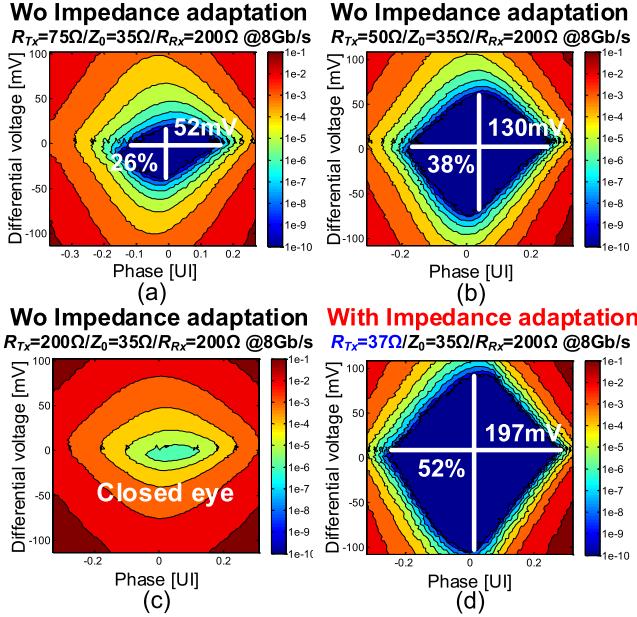


Fig. 23. Eye diagrams measured *in-situ* at the Rx when (a) 75- Ω standard Tx, (b) 50- Ω standard Tx, (c) Tx with $R_{Tx} = R_{Rx}$, (d) proposed Tx are used. In this experiment, the Txs transmit PRBS-31 data at 8 Gb/s to a 200- Ω R_{Rx} through a 35- Ω channel. The channel loss measured at the Nyquist frequency ($f = 4$ GHz) was 10.7 dB. All the Txs used 16.3-mA tap current.

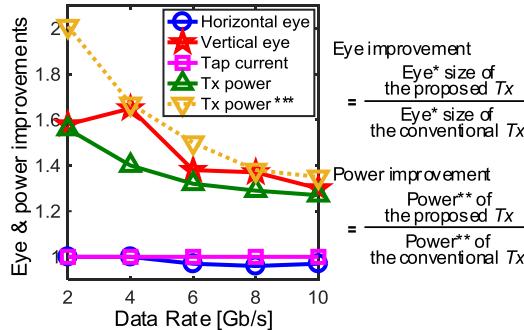


Fig. 24. Eye and power improvements of the proposed Tx in a 50- Ω standard link: $Z_0 = R_{Rx} = 50 \Omega$ at 2–10 Gb/s. The conventional Tx was matched using $R_{Tx} = 50 \Omega$ while the proposed Tx automatically configured R_{Tx} to 200 Ω . In this figure, eye* includes horizontal and vertical eyes. Power** includes Tx power and total tap current. The Tx power*** is the Tx's power improvement when both Txs achieve almost identical eye opening.

to set $R_{Tx} = Z_0$ by measuring dc current at the Tx output, $R_{Rx} = 200 \Omega$ would be falsely detected as Z_0 . Thus, the Tx falsely configures $R_{Tx} = 200 \Omega$. It completely closes the eye [Fig. 23(c)]. When the proposed Tx is used, R_{Tx} is automatically set to 37 Ω (almost the same as Z_0), achieving vertical eye of 197 mV [Fig. 23(d)] which is almost the same as the Z_0 -matching Tx. In summary, the proposed Tx improves the vertical eye sizes by 1.5x and 3.8x, compared with the 50- and 75- Ω standard Txs, respectively.

The proposed method also improves poor power efficiency at low data rate. For backward compatibility, Txs are required to operate at broad ranges of data rates; for instance, for 2–10 Gb/s. However, the power efficiency of the 50- Ω standard link ($Z_0 = R_{Tx} = R_{Rx} = 50 \Omega$) drastically decreases at low data rate because the power consumption by the tap current of

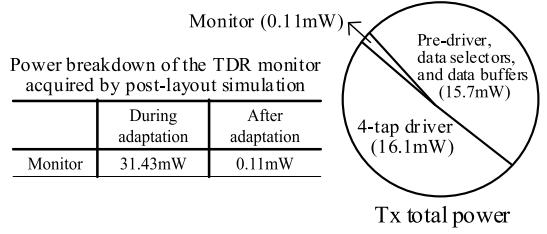


Fig. 25. Power breakdown of the proposed Tx at 12 Gb/s (sample 4 in Fig. 20).

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	Conventional Tx	This work
Technology	65-nm CMOS	65-nm CMOS
Architecture	4-tap FFE TX	4-tap FFE TX
Adaptation to Channel	X	O (Demonstrated for $Z_0=35 \Omega$ –75 Ω)
Adaptation to R_{Rx} impedance	X	O (Demonstrated for $R_{Rx}=30 \Omega$ –200 Ω)
PRBS-23, Data rate=12 Gb/s, loss=−15.3 dB, $Z_0=35 \Omega$, $R_{Rx}=35 \Omega$	<p>Tx termination 35 Ω</p> <p>Tap current 20.0 mA</p> <p><i>Tx</i> power 23.7 mW</p> <p>Vertical eye 84.6 mV</p> <p>Horizontal eye 52.8 %</p>	<p>Tx termination 131 Ω (Automatically adapted)</p> <p>Tap current 16.8 mA</p> <p><i>Tx</i> power 19 mW</p> <p>Vertical eye 83.8 mV</p> <p>Horizontal eye 51.6 %</p>
PRBS-31, Data rate=8 Gb/s, loss=−10.7 dB, $Z_0=35 \Omega$, $R_{Rx}=200 \Omega$	<p>Tx termination 75 Ω</p> <p>Tap current 16.3 mA</p> <p><i>Tx</i> power 18.0 mA</p> <p>Vertical eye 52 mV</p> <p>Horizontal eye 26 %</p>	<p>Tx termination 37 Ω (Automatically adapted)</p> <p>Tap current 16.3 mA</p> <p><i>Tx</i> power 19.8 mW</p> <p>Vertical eye 197 mV (3.8x)</p> <p>Horizontal eye 52 % (2x)</p>
PRBS-31, Data rate=2 Gb/s, loss=−4.3 dB, $Z_0=50 \Omega$, $R_{Rx}=50 \Omega$	<p>Tx termination 50 Ω</p> <p>Tap current 9.6 mA</p> <p><i>Tx</i> power 8.1 mW</p> <p>Vertical eye 274 mV</p> <p>Horizontal eye 80 %</p>	<p>Tx termination 200 Ω (Automatically adapted)</p> <p>Tap current 5.7 mA</p> <p><i>Tx</i> power 4.0 mW (2x)</p> <p>Vertical eye 274 mV</p> <p>Horizontal eye 80 %</p>

the Tx does not scale with the reduced data rate; the tap current and the corresponding power consumption is relatively large at low data rate due to the small termination impedance of 50 Ω . When our Tx is used in the 50- Ω standard link, $R_{Tx} = 200 \Omega$ is automatically configured. As a result, the vertical eye size is improved by about 1.6–1.3x at 2–10 Gb/s compared with the 50- Ω Tx for the same tap current (Fig. 24). When the total tap currents are scaled for the same eye size, our Tx can reduce the Tx power by up to 2x at 2 Gb/s (Fig. 24).

Fig. 25 summarizes the power consumption of the proposed Tx and the TDR monitor measured at 12 Gb/s when connected to a 35- Ω channel and a 200- Ω R_{Rx} (sample 4 in Fig. 20). During R_{Tx} adaptation, the monitor consumed about 31.4 mW. However, after the adaption, the monitor was turned off and consumed only 0.1 mW, which is only about 3% of the total power consumption of the Tx (31.9 mW). This result shows that the power overhead of the monitor is negligible.

The performance of the proposed Tx and comparison with the conventional Txs are summarized in Table I.

VI. CONCLUSION

We propose an FFE Tx, which automatically adapts to arbitrary impedances of the channel and the Rx. An on-chip

TDR monitor attached at the Tx output accurately detects channel and Rx impedances, and then the impedance matching of the Tx is automatically and adaptively violated (relaxed) to maximize the signal amplitude at the cost of a negligible penalty in signal integrity. The optimal configuration of the Tx impedance is theoretically derived from a relaxed impedance matching constraint which is suggested for the first time in this paper. Theoretically, we proved that the relaxed impedance matching constraint bounds the penalty in signal integrity caused by impedance mismatch below a desired level.

The proposed FFE Tx was implemented in 65-nm CMOS technology and tested. In the experiment, the Tx successfully adapted to any combination of channel impedances of 35–75 Ω and Rx impedances of 30–200 Ω while achieving the same or better eye size and power efficiency compared with the conventional Z_0 -matching Tx. When blindly connected to an arbitrary channel and an arbitrary Rx, the Tx improved the eye size by 3.8x. In addition, the Tx improved poor power efficiency of a conventional 50- Ω link by up to 2x.

All these results show that the proposed Tx can provide seamless and automatic universal compatibility with diverse impedance standards while achieving better performance and power efficiency than the one with the conventional impedance matching. In addition, these features allow optimal link design beyond the restriction of the impedance standard, and thus enable evolution of technology without the problem of backward compatibility.

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REFERENCES

- [1] X. Gu, K. J. Han, M. Cracraft, R. R. Donadio, and Y. Kwark, “Efficient parametric modeling and analysis for backplane channel characterization,” in *Proc. Electron. Compon. Technol. Conf.*, May 2012, pp. 1880–1885.
- [2] V. Ricchiuti, “Design tips: Checking high speed digital backplanes,” *IEEE Electromagn. Compat. Mag.*, vol. 1, no. 2, pp. 90–93, 2nd Quart., 2012.
- [3] S. Han, S. Lee, M. Choi, J.-Y. Sim, H.-J. Park, and B. Kim, “A coefficient-error-robust FFE TX with 230% eye-variation improvement without calibration in 65 nm CMOS technology,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 50–51.
- [4] S. Han, S. Lee, M. Choi, J.-Y. Sim, H.-J. Park, and B. Kim, “A coefficient-error-robust feed-forward equalizing transmitter for eye-variation and power improvement,” *IEEE J. Solid-State Circuits*, vol. 51, no. 8, pp. 1902–1914, Aug. 2016.
- [5] *IEEE 802.3 Ethernet Working Group*. Accessed: Jun. 17, 2010. [Online]. Available: <http://www.ieee802.org/3/ba>
- [6] *Optical Interconnect Forum (OIF)*. Accessed: Jul. 19, 2010. [Online]. Available: <http://www.oiforum.com/public/currentprojects.html>
- [7] *JDEC DDR3 & DDR4 Standard*. Accessed: Sep. 25, 2012. [Online]. Available: <https://www.jedec.org/category/technology-focus-area/main-memory-ddr3-ddr4-sdram>
- [8] K. Kaviani *et al.*, “A tri-modal 20-Gbps/link differential/DDR3/GDDR5 memory interface,” *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 926–937, Apr. 2012.
- [9] S.-M. Lee *et al.*, “An 80 mV-swing single-ended duobinary transceiver with a TIA RX termination for the point-to-point DRAM interface,” *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2618–2630, Nov. 2014.
- [10] R. A. Aroca and S. P. Voynigescu, “A large swing, 40-Gb/s SiGe BiCMOS driver with adjustable pre-emphasis for data transmission over 75 Ω coaxial cable,” *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2177–2186, Oct. 2008.
- [11] J. Han, Y. Lu, N. Sutardja, and E. Alon, “A 60 Gb/s 288 mW NRZ transceiver with adaptive equalization and baud-rate clock and data recovery in 65 nm CMOS technology,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 112–113.
- [12] H. Hatamkhani and C.-K. K. Yang, “Power analysis for high-speed I/O transmitters,” in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2004, pp. 142–145.
- [13] B. Kim, Y. Liu, T. O. Dickson, J. F. Bulzacchelli, and D. J. Friedman, “A 10-Gb/s compact low-power serial I/O with DFE-IIR equalization in 65-nm CMOS,” *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3526–3538, Dec. 2009.
- [14] M. Bassi, F. Radice, M. Brucolieri, S. Erba, and A. Mazzanti, “A 45 Gb/s PAM-4 transmitter delivering 1.3 Vppd output swing with 1V supply in 28 nm CMOS FDSOI,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 66–67.
- [15] M. Choi *et al.*, “An FFE TX with 3.8x eye improvement by automatic impedance adaptation for universal compatibility with arbitrary channel and RX impedances,” in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2017, pp. 58–59.
- [16] M. Choi, J.-Y. Sim, H.-J. Park, and B. Kim, “An approximate closed-form channel model for diverse interconnect applications,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 10, pp. 3034–3043, Oct. 2014.
- [17] C. Menolfi *et al.*, “A 28 Gb/s source-series terminated TX in 32 nm CMOS SOI,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2012, pp. 334–335.
- [18] B. Kim and V. Stojanović, “A 4 Gb/s/ch 356 fJ/b 10 mm equalized on-chip interconnect with nonlinear charge-injecting transmit filter and transimpedance receiver in 90 nm CMOS,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2009, pp. 66–67.
- [19] B. Kim and V. Stojanović, “An energy-efficient equalized transceiver for RC-dominant channels,” *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1186–1197, Jun. 2010.
- [20] M. Lee, S. Han, J.-Y. Sim, H.-J. Park, and B. Kim, “A 10-GHz multi-purpose reconfigurable built-in self-test circuit for high-speed links,” in *IEEE Asian Solid-State Circuits Dig. Tech. Papers*, Nov. 2017, pp. 73–76.



Minsoo Choi received the B.S. degree in electronic engineering from Soong-Sil University, Seoul, South Korea, in 2012, and the M.S. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, South Korea, in 2014, where he is currently pursuing the Ph.D. degree.

His current research interests include high-speed links, signal/power integrity, and interconnect modeling.



Sooeun Lee was born in Su-Won, South Korea, in 1990. She received the B.S. and M.S. degrees in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, South Korea, in 2013 and 2015, respectively, where she is currently pursuing the Ph.D. degree with the Department of Electronic and Electrical Engineering.

Her current research interests include high-speed serial/parallel links, signal integrity, and biosensor driving circuits.

Ms. Lee was a co-recipient of the Gold Award of the 15th Korean Solid-State Circuits Design Contest.



Myungguk Lee received the B.S. degree in electronic engineering from the Kumoh National Institute of Technology, Gumi, South Korea, in 2015, and the M.S. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, South Korea, in 2017, where he is currently pursuing the Ph.D. degree.

His current research interests include high-speed I/O circuit design.



Ji-Hoon Lee received the B.Eng. (First Class Hons.) degree in electrical and electronic engineering from the Imperial College of Science, Technology and Medicine, London, U.K., in 2015, and the M.S. degree from the Pohang University of Science and Technology (POSTECH), Pohang, South Korea, in 2017.

He was a Research Scientist at the Center for Biomicro-System, Brain Science, Institute of Korea Institute Science and Technology, Seoul, South Korea, from 2017 to 2018. His current research interests include advanced nanotechnology and materials science for biological/biomedical research.



Jae-Yoon Sim (M'02–SM'13) received the B.S., M.S., and Ph.D. degrees in electronic and electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, South Korea, in 1993, 1995, and 1999, respectively.

From 1999 to 2005, he was a Senior Engineer with Samsung Electronics, Hwasung, South Korea. From 2003 to 2005, he was a Post-Doctoral Researcher with the University of Southern California, Los Angeles, CA, USA. In 2005, he joined POSTECH, where he is currently an Associate Professor.

Prof. Sim has served on the Technical Program Committees of the IEEE International Solid-State Circuits Conference, Symposium on Very Large Scale Integration Circuits, and the Asian Solid-State Circuits Conference. He was a recipient of the Author Recognition Award at ISSCC 2013 and was a co-recipient of the Takuo Sugano Award at ISSCC 2001.



Hong-June Park (M'88–SM'13) received the B.S. degree from Seoul National University, Seoul, South Korea, in 1979, the M.S. degree from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 1981, and the Ph.D. degree from the University of California at Berkeley, Berkeley, CA, USA, in 1989.

He was a CAD Engineer with ETRI, Daejeon, from 1981 to 1984, and a Senior Engineer with the TCAD Department, Intel, Santa Clara, CA, USA, from 1989 to 1991. In 1991, he joined the Faculty of Electronic and Electrical Engineering, Pohang University of Science and Technology (POSTECH), Pohang, South Korea, where he is currently a Professor. He developed the public-domain window program SIGMA-SPICE, which solved the dc convergence problem with GUI based on the Berkeley SPICE3. He has authored four books on analog and digital CMOS circuits in Korean. He has authored or co-authored over 240 research papers including 80 international journal papers and holds 24 international patents and 42 Korean patents. His current research interests include CMOS analog circuit design such as high-speed interface circuits, ROIC of touch sensors, and analog/digital beamformer circuits for ultrasound medical imaging.

Prof. Park is a member of IEEK. He served as the Editor-in-Chief for the *Journal of Semiconductor Technology and Science* from 2009 to 2012, the Vice President for the IEEK in 2012, and a Technical Program Committee Member for ISSCC, SOVC, and A-SSCC for several years. He was a recipient of the Haedong Academics Award from IEEK in 2012.



Byungsuk Kim (M'11–SM'16) received the B.S. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, South Korea, in 2000, and the M.S. and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 2004 and 2010, respectively.

He was an Analog Design Engineer with Intel Corporation, Hillsboro, OR, USA, from 2010 to 2011. In 2012, he joined the Faculty of Department of Electrical Engineering, POSTECH, where he is currently an Associate Professor.

Dr. Kim received several honorable awards. He was a recipient of the IEEE JOURNAL OF SOLID-STATE CIRCUITS Best Paper Award in 2009, and the Analog Device Inc., Outstanding Student Designer Award from MIT in 2009. He was a co-recipient of the Beatrice Winner Award for Editorial Excellence at the 2009 IEEE Internal Solid-State Circuits Conference. He has been serving as a Technical Program Committee Member of the IEEE Asian Solid-State Circuits Conference since 2012.