

# A 1.8-V 6.9-mW 120-fps 50-Channel Capacitive Touch Readout With Current Conveyor AFE and Current-Driven $\Delta\Sigma$ ADC

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**Abstract**—This paper presents an area- and energy-efficient readout for capacitive touch sensors. An analog front end (AFE) with current conveyor mitigates the requirements of front-end opamp and provides a differential current from adjacent channels, removing sensor's baseline and interferences. The sensing current from the AFE is directly digitized by a current-driven 2nd-order  $\Delta\Sigma$  analog-to-digital converter and its direct interfacing with the current signal achieves high signal-to-noise ratio (SNR) without suffering voltage saturation in the AFE, and provides reconfigurable SNRs and frame rates with respect to oversampling ratio. An area-efficient sinc<sup>2</sup> filter, whose filter coefficients are commonly provided, enables full parallel implementation of  $\Delta\Sigma$  ADCs. A 50-channel prototype IC is fabricated in a 0.18- $\mu\text{m}$  CMOS process, occupying only 1.96 mm<sup>2</sup>. Using a 10.1-in 28 × 50 touch screen panel and a 3.3-V transmitter, this work achieves SNRs of 53.3 and 41.7 dB with finger and 1-mm- $\phi$  stylus, respectively, while drawing only 6.9 mW from 1.8-V supply at 120 fps. This results in the state-of-the-art figure-of-merit of 0.11 and 0.41 nJ/step for finger and 1-mm- $\phi$  stylus, respectively. Moreover, 500-dpi on-glass fingerprint sensor is verified with the same prototype IC and 15-V transmitter, and 70 × 50 fingerprint image is successfully captured with 150- $\mu\text{m}$  cover glass.

**Index Terms**—Area-efficient decimation filter, capacitance-to-digital conversion, capacitive touch sensor, current conveyor analog front end (AFE), current-driven delta-sigma analog-to-digital converter (ADC), energy-efficient, incremental delta-sigma ADC, on-glass fingerprint sensor.

## I. INTRODUCTION

CAPACITIVE touch sensors are essential for user interfaces of mobile devices, such as smart phones and tablets. The energy efficiency of capacitive touch sensors should be optimized due to their battery-powered operation. For high-quality touch features, the number of sensing channel

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has been increased in touch screen panels (TSPs). This, in turn, requires fine-pitch arrangements of sensing channels, getting a reduction of sensing capacitors. Furthermore, as the size of the TSP increases, the sensing condition is aggravated, resulting in an increase of power. Nevertheless, high signal-to-noise ratio (SNR) with fast scan rate is required for seamless interaction even under the condition of reduced sensing capacitors.

In order to mitigate the SNR degradation, several types of readout architectures have been investigated [1]–[12]. At the driving (TX) side, a sinusoidal or square pulse signal is applied to the TSP and its voltage or frequency can be increased to improve the SNR by applying more energy to the TSP [1], [2]. A higher TX voltage, increasing the signal energy directly, requires more settling time to achieve sufficient accuracy, and the voltage level is often limited to avoid saturation in an analog front end (AFE). The maximum TX frequency is also limited by the *RC* delay of the TSP and its variations. A parallel driving scheme, which drives multiple TX channels with a coded sequence, provides an improved SNR by a factor of  $\sqrt{N}$ , where  $N$  is the number of channels driven simultaneously [3]–[8]. This scheme suffers from severe saturation in the AFE, especially when multiple touches happen in the same receiver (RX) channel as addressed in [1] and [2]. At the RX side, assuming thermal noise limited readouts, multiple sampling and averaging of the AFE output also improve SNR by a factor of  $\sqrt{M}$ , where  $M$  is the number of oversampling, without implementing a gain stage as in [9]–[11]. Since a gain amplifier is not incorporated in the readout chain, the improvement of dynamic range (DR) can be achieved as well. The factor  $M$  should be determined by the number of channel, frame rate, and target resolution. In practice, however, the AFE architecture often limits  $M$  due to its voltage saturation. The RX readout with incremental delta-sigma ( $\Delta\Sigma$ ) analog-to-digital converters (ADCs) provides a good tradeoff between frame rate and resolution [5], [12].

The energy-efficiency figure of merit (FoM) of capacitive touch sensors, motivated by the FoM of ADCs, can be defined as unit step energy per sensing node. Fig. 1 shows the FoM comparison of the state-of-the-art works and most of them are located at an area higher than the FoM of 1 nJ/step. The charge demodulating integrator architecture achieves excellent energy efficiency (0.71 nJ/step) and high SNR of 49 dB [1]. This paper utilizes the parallel-TX scheme with eight-channel TX and imposes the handling capability of high TX voltage up to 12-V. The best energy efficiency (0.33 nJ/step) has

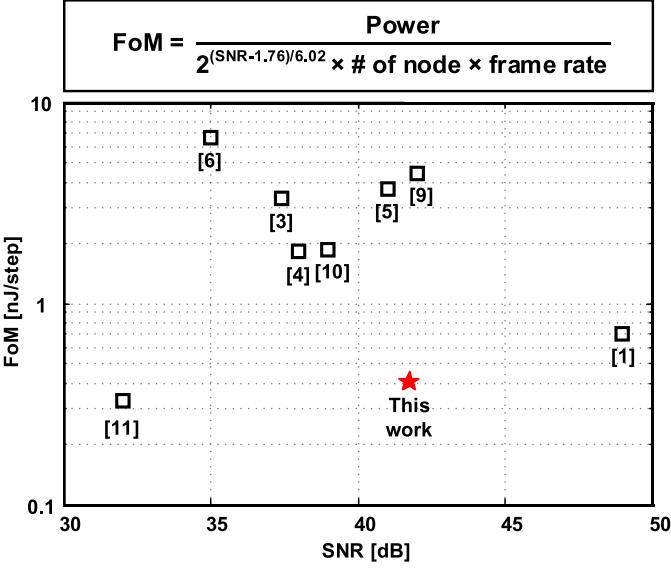
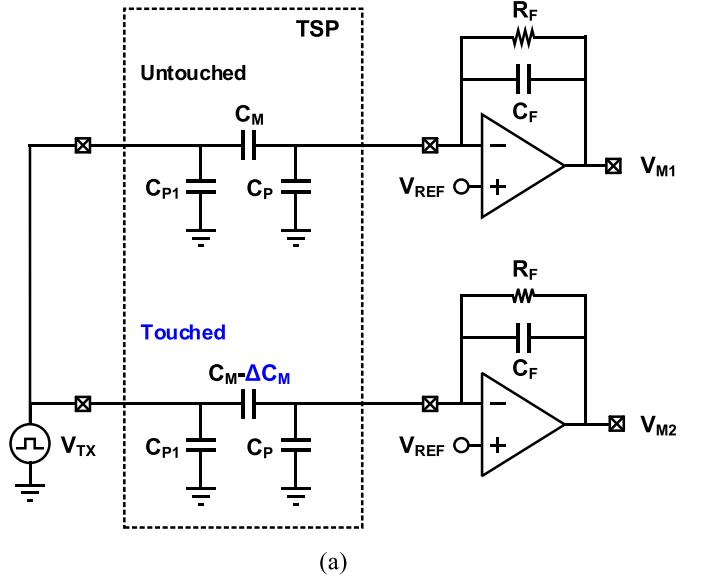


Fig. 1. FoM comparison for 1-mm- $\phi$  stylus with the other state-of-the-art works.

been achieved using a two-step architecture [11], wherein the coarse touch area first measured using self-capacitor readout is digitized by using fine mutual-capacitor readout. This two-step architecture can be more energy efficient, since touch sensors typically include small number of touched points among entire sensing nodes. However, with parallel-TX scheme or two-step architecture, it might suffer from some errors in touch coordination for fast moving objects on the TSP.

This paper presents the design of an energy-efficient readout interface for capacitive touch sensors [13]. It employs an energy-efficient current-driven  $\Delta\Sigma$  ADC architecture, wherein a current conveyor is used as the AFE directly interfacing with the  $\Delta\Sigma$  ADC. The current conveyor AFE relaxes the requirements of the front-end opamp by isolating a large parasitic capacitor on TSPs, and provides a differential current from adjacent channels, that removes the baseline of the sensor and interferences before its voltage conversion. The charge balancing between the sensing current from the AFE and a reference charge is implemented using the 2nd-order  $\Delta\Sigma$  ADC, which should process small sensing currents, resulting in a large power saving. This direct interfacing with the sensing current provides an improved DR without suffering any voltage saturation. An area-efficient sinc<sup>2</sup> filter, whose filter coefficients are commonly provided, enables the full parallel implementation of  $\Delta\Sigma$  ADCs. The prototype 50-channel readout IC is implemented in a 0.18- $\mu\text{m}$  CMOS process. It occupies an area of 1.96 mm<sup>2</sup>, requiring approximately four times less area per column compared to previous state of the art. This work is verified with a 10.1-in 28  $\times$  50 channel TSP and a 3.3-V TX driver. It achieves SNRs of 53.3 and 41.7 dB with finger and 1-mm- $\phi$  stylus, respectively, at 120 fps while consuming only 6.9 mW from a 1.8-V supply. This corresponds to a FoM of 0.11 and 0.41 nJ/step for finger and 1-mm- $\phi$  stylus, respectively, which shows an improvement of more than four times that of previous state-of-the-art works [1]–[12]. This work is further verified using 500-dpi transparent on-glass



(a)

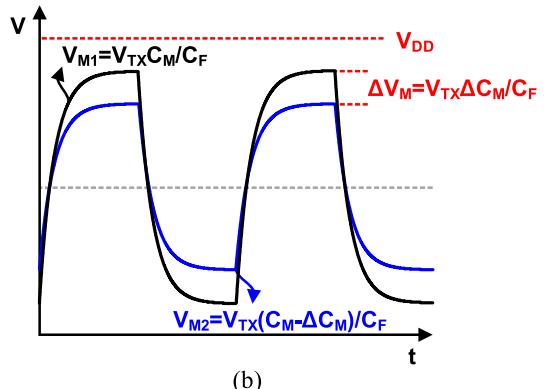


Fig. 2. (a) Schematic of the conventional AFE and its (b) voltage outputs.

fingerprint sensor and a 15-V TX driver. The sensor of 70  $\times$  50 array is implemented with a pitch of 50  $\mu\text{m}$ . This work achieves a capacitor resolution of 34 aF, and a fingerprint image is successfully captured at the rate of 19 fps with SNR of 10.3 dB with the 150- $\mu\text{m}$  thickness cover glass.

This paper is organized as follows. Section II describes the AFE architectures and provides their comparison and Section III presents the architecture of the proposed readout interface. Section IV discusses the implementation details and Section V presents the measurement results. Finally, the conclusions are drawn in Section VI.

## II. ANALOG FRONT-END ARCHITECTURE

For touch sensor application, there are two different AFE architectures to sense the charge signal from the TSP. One is a capacitive charge amplifier [1]–[12], which converts the input charge to a voltage signal, and the other is a current conveyor [13]–[15], which converts the input charge to a current signal. In this section, we will introduce the operation principles of two architectures and compare their energy-efficiency.

### A. Capacitive Charge Amplifier AFE

The working principle of the capacitive charge amplifier with the TSP is illustrated in Fig. 2(a). Here, an electrical

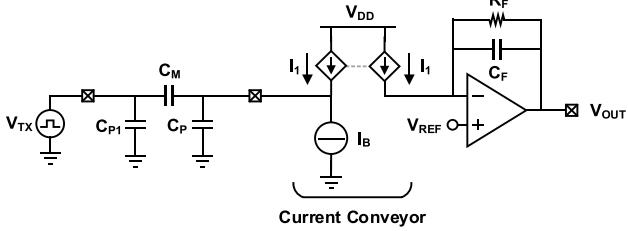


Fig. 3. Schematic of the proposed current conveyor AFE.

model with a mutual capacitor  $C_M$  and two parasitic capacitors ( $C_P$  and  $C_{P1}$ ) is used for the TSP. When the TX signal  $V_{TX}$  is applied to the TX electrode, the charge amplifier converts the charge signal  $Q = V_{TX}C_M$  from the mutual capacitance  $C_M$  into the voltage output  $V_{M1} = V_{TX}C_M/C_F$ . When the sensing channel of the TSP is touched, the value of  $C_M$  is decreased ( $\Delta C_M$ ) and it provides the voltage output  $V_{P2} = V_{TX}(C_M - \Delta C_M)/C_F = V_{M1} - \Delta V_M$ , as shown in Fig. 2(b).

A critical issue associated with the charge amplifier AFE is that the value of  $\Delta C_M$  ( $< 100$  fF) is much smaller than the baseline capacitor  $C_M$  ( $\sim 1\text{pF}$ ). The voltage ratio  $\Delta V_M/V_{M1}$  is less than 1/10, which indicates that the charge amplifier suffers a large signal swing to process mostly unnecessary signals. This enforces the use of either a high supply voltage  $V_{DD}$  or large feedback capacitor  $C_F$  to avoid the output voltage saturation of the charge amplifier. In a fine-pitch TSP, this problem is aggravated because the higher  $V_{TX}$  is used for a smaller  $\Delta C_M$  to maintain the signal charge  $\Delta Q = V_{TX}\Delta C_M$ , forcing the use of much larger  $C_F$ . In conjunction with a large  $C_P$ ,  $C_F$  affects as a load capacitance of the charge amplifier, resulting in an increase of power.

In order to remove the baseline signal from  $C_M$  and convert only the signal charge from  $\Delta C_M$ , many touch sensor AFEs employ the differential sensing of two adjacent channels using a gain amplifier, integrator, or analog filter [1], [2], [5]–[7], [10]–[12]. The differential voltage, however, is often engaged at the outputs of charge amplifiers. Therefore, the power penalty of the charge amplifier still remains and the following stage introduces additional power consumption. In order to eliminate  $C_M$  without additional stages, a fully differential charge amplifier has been used [3], [4], [8], [9]. Since only  $\Delta V_M$  appears at the output of the fully differential charge amplifier, it enables the increase of the signal gain, which improves a sensing resolution. A drawback of this architecture is that the frame-rate loss by a factor of 2 due to the two-phase (or even-odd) channel switching to get differential signals among adjacent channels.

### B. Current Conveyor AFE

The proposed AFE, as shown in Fig. 3, employs a current conveyor followed by a charge amplifier. If an input current from the TSP is forced through the input, a related current  $I_1$  will flow through the sensing branch. The same current  $I_1$  is conveyed into the charge amplifier and converted to the output voltage of the charge amplifier. There would be slight differences in the  $I_1$  due to the finite output impedance of the current

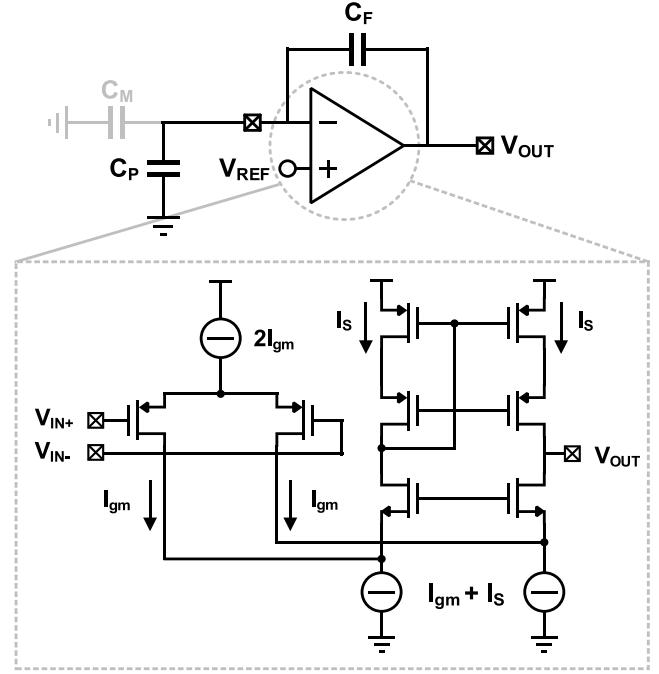


Fig. 4. Simplified schematic of the conventional AFE with a folded-cascode OTA.

conveyor, but the difference is mitigated by setting the output voltage of the current conveyor to the virtual ground voltage  $V_{REF}$  of the charge amplifier. Complementary currents can be provided further with additional outputs by a repetition of the current conveyor. Since the current conveyor isolates a large parasitic capacitor  $C_P$  on the TSP from the charge amplifier, the load capacitance of the charge amplifier can be reduced. Therefore, the power consumption of the charge amplifier is much smaller than that of the conventional AFE. It also enables current signaling before its voltage conversion, such as signal amplification, baseline removal, signal demodulation, and charge balancing, which will be described in Section III.

### C. Settling Time Comparison

For capacitive touch sensors, the maximum bandwidth  $\omega_m$  is determined by the  $RC$  time constant of the TSPs. The bandwidth  $\omega_0$  of the AFE should be matched with the  $\omega_m$  to achieve the maximum efficiency. The charge amplifier AFE can be simplified with  $C_P$  and  $C_F$ , as shown in Fig. 4, since  $C_P$  is much larger than  $C_M$ . Assuming one pole system, the time constant  $\tau$  of the charge amplifier can be defined by  $C_L/(\beta \times g_m)$ , where  $C_L$  is the load capacitance of the charge amplifier,  $C_F \times C_P/(C_F + C_P)$ ,  $\beta$  is the feedback factor and  $g_m$  is the transconductance of the amplifier. Since  $\beta$  is  $C_F/(C_F + C_P)$ ,  $\omega_0$  which is  $1/\tau$ , is determined by  $g_m/C_P$ . In addition to  $g_m$ , the slew condition also determines  $\omega_0$ , since the TX driving generates a large signal requiring a high slew-rate. The slew-rate is also limited by the internal current and parasitic capacitance, and the bandwidth estimation of the charge amplifier AFE is dependent on the amplifier structure.

On the other hand, in the current conveyor AFE, the  $\omega_0$  is directly determined by  $g_m/C_P$ , where  $1/g_m$  is the input

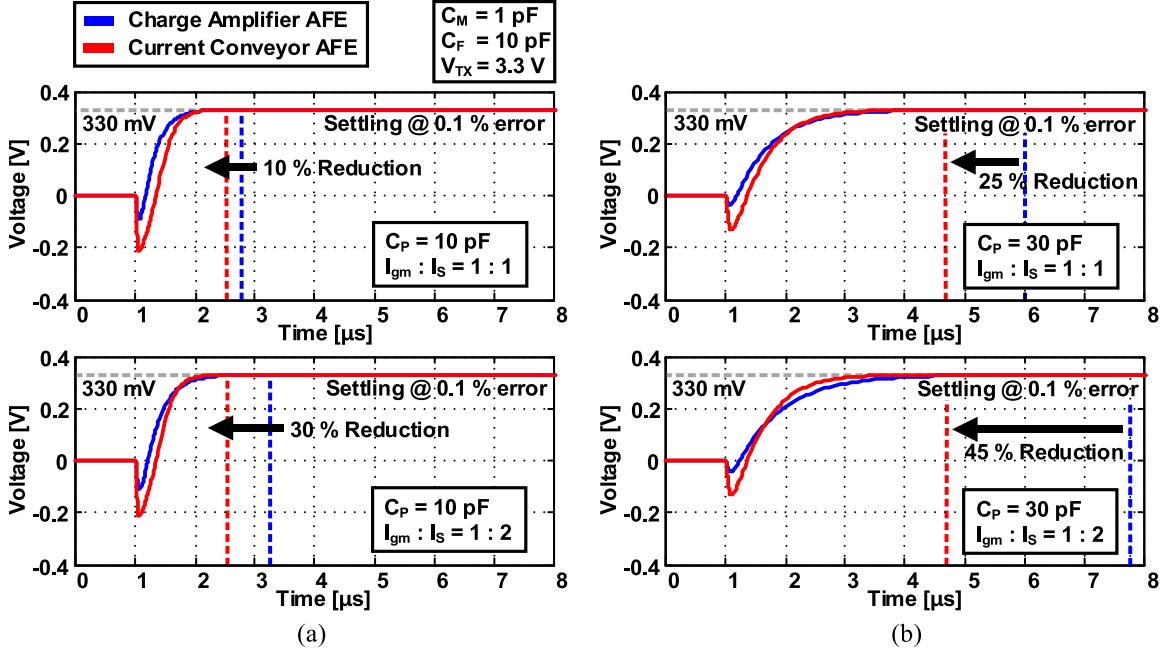


Fig. 5. Settling time comparison with charge amplifier and current conveyor AFE on  $I_{gm}:I_S$  of 1:1 (top) and 1:2 (bottom) with  $C_P$  of (a) 10 and (b) 30 pF.

impedance of the current conveyor, since there is no feedback in the current conveyor. Furthermore, the bias current,  $I_B$  for  $g_m$  is also used for current slewing because the current conveyor has single branch. Due to the small load capacitance by  $C_P$  isolation, small amount of current is required for the following charge amplifier. Therefore, the current conveyor consumes most of the power in the current conveyor AFE.

For a settling time comparison, both AFEs employ a folded-cascode operational transconductance amplifier (OTA), which is commonly used in many AFEs [9]. As shown in Fig. 4, the conventional AFE with folded-cascode OTA requires a bias current  $I_S$  for the current buffer along with the drain current  $I_{gm}$  of the input. Although the current influence is divided to  $g_m$  and slew-rate in this topology, the current conveyor provides both  $g_m$  and slew-rate simultaneously by single bias current. Therefore, both  $g_m$  and slew-rate can be maximized in the case of same current amount. Fig. 5 shows the simulated settling time with the same current consumption of  $20 \mu\text{A}$  for both AFEs. For the AFE of charge amplifier, the current ratio between  $I_{gm}$  and  $I_S$  is chosen to be 1:1 (top) and 1:2 (bottom) as examples for typical case and higher slew-rate one, respectively. Meanwhile, the current ratio between current conveyor and charge amplifier is taken to be 8:2 for the proposed AFE, because the following charge amplifier needs smaller current than current conveyor that is caused by the isolation of  $C_P$ . The settling time is measured from the input transition to the time when the AFE output enters an error of 0.1%. When  $C_P$  is 10 pF, as shown in Fig. 5(a), the settling time of the current conveyor AFE is reduced by 10% and 30% for the charge amplifier AFE with 1:1 and 1:2 current ratios, respectively. When  $C_P$  increases to 30 pF, as shown in Fig. 5(b), the settling time reduction is further enhanced to 25% and 45%, respectively. Therefore, the current conveyor AFE can provide wider bandwidth and better energy-efficiency compared to the charge amplifier AFE.

### III. PROPOSED READOUT INTERFACE

#### A. Overall Architecture

Fig. 6 shows the overall block diagram of the proposed readout interface. The interface consists of dual-output current conveyors (DOCCs), current-driven  $\Delta\Sigma$  ADCs, SRAM buffer memory, and scanning circuits. A full parallel implementation is used for the readout circuits, which maximizes an energy-efficiency. DOCCs sense the input current  $I_M$  from the TSP, which enables the required current signaling such as signal amplification, baseline removal, and signal demodulation. The signal current  $I_{SIG}$  is fed to the current-driven  $\Delta\Sigma$  modulators, providing direct digital conversion of the  $I_{SIG}$  without voltage conversion. A compact sinc<sup>2</sup> filter is used for the decimation filter, which produces a 14-bit digital value  $D_{OUT}$  representing a TSP output from modulator's bit stream  $bs$ . After the ADC of each TX, the digital output is transferred to SRAM buffer memory. During the conversion of next TX, the output values are taken out through the sense amplifiers. Fig. 7 shows the timing diagram of two TX conversions. Each TX is driven by square pulse sequentially at TX driving frequency of 200 kHz, and the signal demodulation is performed at the same frequency  $f_{DRV}$ . Since the charge signal is generated for every edge of the TX pulse, quantizing decision can be made for each charge signal, resulting  $f_S = 2f_{DRV} = 400$  kHz. The  $\Delta\Sigma$  ADCs are reset and operate for 120 cycles generating an output code  $D_{OUT}$  for each RX, and the conversion time for single TX is  $300 \mu\text{s}$ , which corresponds to the frame rate of 120 fps for a  $28 \times 50$  channel TSP.

#### B. Dual-Output Current Conveyor AFE

Fig. 8 describes the operating principle of the DOCC AFE. In order to eliminate the baseline current  $I_M$  from  $C_M$ , the single-ended current conveyor is elaborated into a DOCC, generating two output currents from a sensing branch, and the

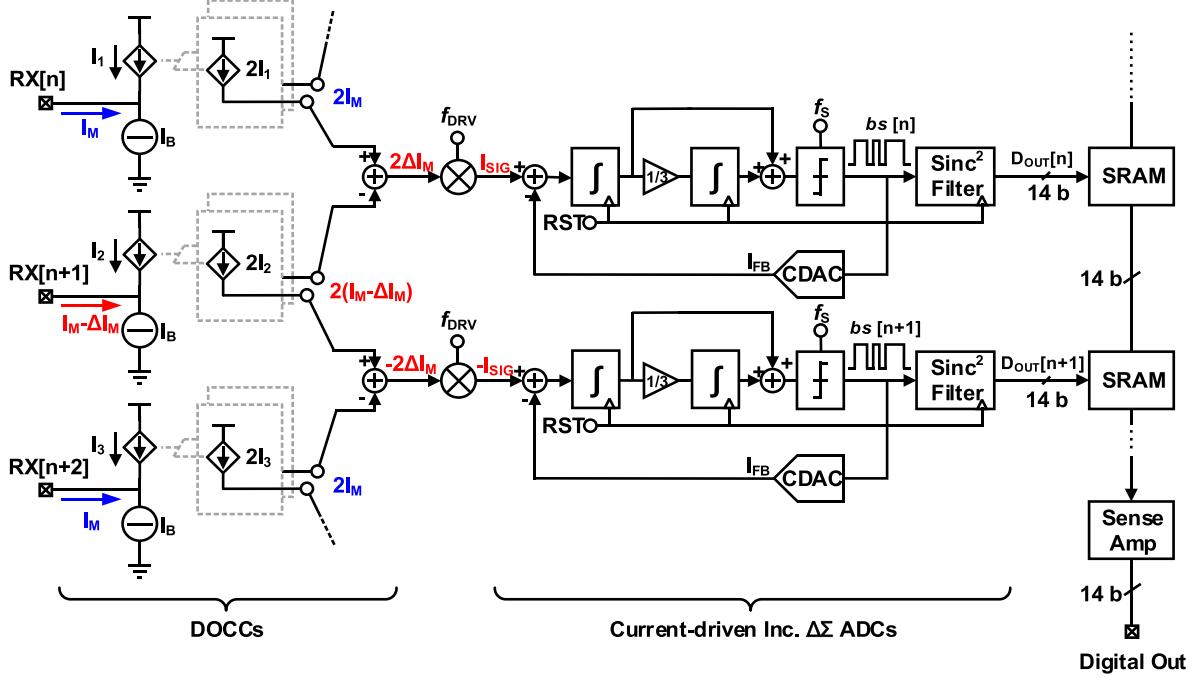


Fig. 6. Overall block diagram.

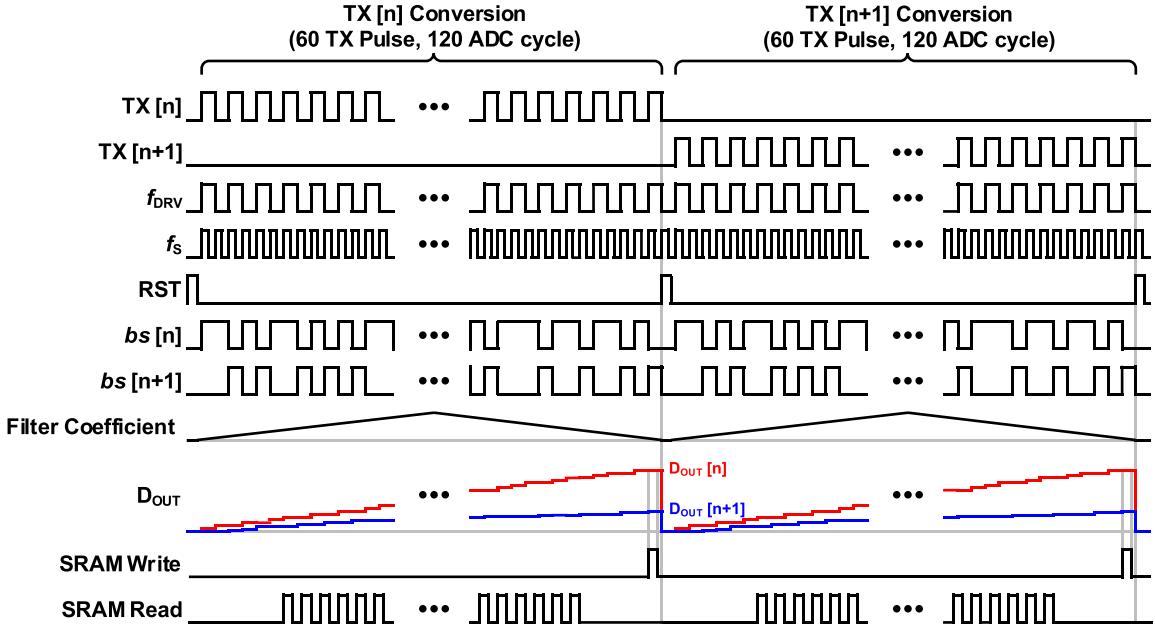


Fig. 7. Operation timing chart.

current signal is subtracted with their adjacent channels, providing differential currents ( $\pm\Delta I_M = I_1 - I_2$  or  $I_2 - I_1$ ). The DOCC prevents the frame-rate loss, which has been caused by even-odd channel switching in conventional fully differential AFEs [3], [4], [8], [9]. It should be noted that the baseline  $I_M$  elimination is implemented before its voltage conversion. Since the following charge amplifier only deals with  $\Delta I_M$ , this enables the use of a small integration capacitor  $C_F$  and low supply voltage, resulting in reduction of area and power. This current subtraction provides noise immunity against com-

mon noise such as display noise, whose feature is determined by the common-mode rejection ratio (CMRR) of the DOCC, which will be described in Section IV. Since the current copies with scaling factors simply follow the size ratio between input and output of the current conveyor, the DOCC provides a current gain of 2 for signal amplification, thus transferring  $2\Delta I_M$  into the charge amplifier. The output current might vary with changes in output voltage of the DOCC due to the finite output impedance, but the output voltage is set by  $V_{REF}$  of the following charge amplifier and the current

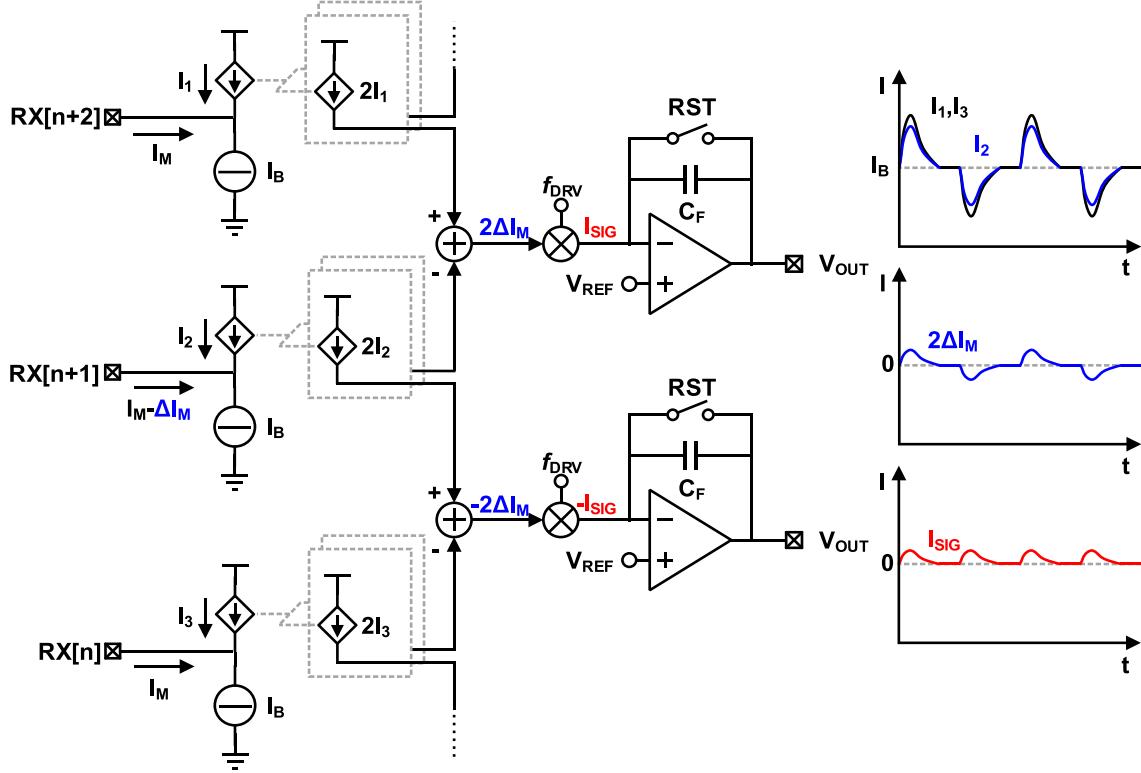


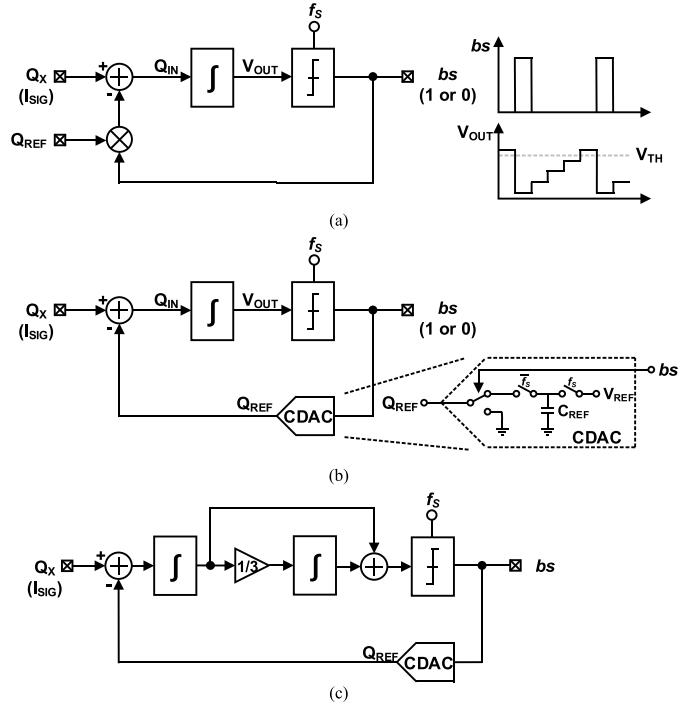
Fig. 8. Operating principle of the DOCC AFE.

error can be well mitigated. The channel mismatch of the DOCC output results in an offset current causing the voltage saturation of the charge amplifier, but this offset current can be eliminated with a demodulation chopper at the output of the DOCC. A demodulation chopper, which operates at the same frequency  $f_{DRV}$  of the TX driver for signal demodulation to the baseband, not only rectifies  $2\Delta I_M$  but also reduces the offset current and low-frequency  $1/f$  noise of the DOCC. Since the chopper switches are placed at the virtual ground of the charge amplifier, the signal-dependent chopper artifacts are also mitigated. Finally, two differential currents  $\pm I_{SIG}$  are integrated in the charge amplifiers.

### C. Current-Driven $\Delta\Sigma$ Modulator

The input current  $I_{SIG}$  can be digitized with a current-driven  $\Delta\Sigma$  ADC by comparing the  $I_{SIG}$  to known reference charge  $Q_{REF}$ . Fig. 9(a) shows the conceptual diagram of the  $\Delta\Sigma$  modulator and the 1st-order loop filter is employed for its simplicity. At the beginning, the integrator and the comparator output are reset. During its conversion, whenever the output of integrator exceeds the comparator's threshold  $V_{TH}$ ,  $bs$  becomes high and  $Q_{REF}$  is subtracted from the input of the integrator. This negative feedback provides the repeated but regulated outputs to the integrator, and it makes zero average charge into the integrator. A bit stream density  $\mu$  can be defined as the ratio between the number of high  $bs$  and the total number of bit stream. As a result of zero average input charge  $Q_{IN}$ , the bit-stream density  $\mu$  can be calculated as follows:

$$\mu (Q_X - Q_{REF}) + (1 - \mu)Q_X = Q_{IN} = 0. \quad (1)$$

Fig. 9. (a) Charge balancing with the 1st-order  $\Delta\Sigma$  modulator. (b) 1st-order  $\Delta\Sigma$  modulator with CDAC. (c) Implemented 2nd-order  $\Delta\Sigma$  modulator with CDAC.

The equation provides  $\mu$  as follows:

$$\mu = Q_X / Q_{REF} \propto I_{SIG} / Q_{REF}. \quad (2)$$

As shown in Fig. 9(b),  $Q_{REF}$  can be generated from a capacitive digital-to-analog converter (CDAC), which utilizes

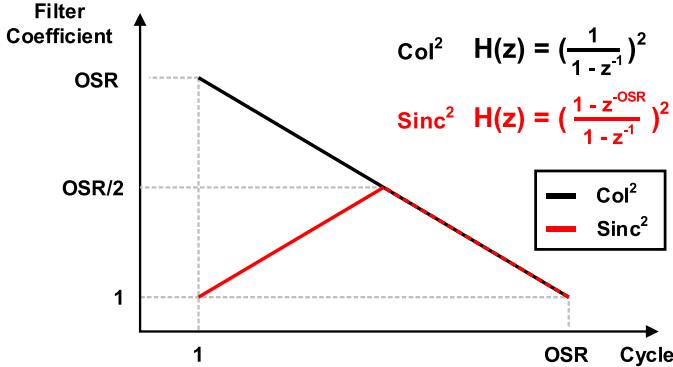


Fig. 10. Filter coefficient and transfer function of the  $\text{Col}^2$  and  $\text{sinc}^2$  filters.

a reference capacitor  $C_{\text{REF}}$  and a voltage  $V_{\text{REF}}$ . Since  $Q_X = 2V_{\text{TX}}\Delta C_M$ , the  $\mu$  can be obtained as follows:

$$\mu = Q_X/Q_{\text{REF}} = 2V_{\text{TX}}\Delta C_M/V_{\text{REF}}C_{\text{REF}} \quad (3)$$

where the factor of 2 comes from the current gain of the DOCC. Therefore, the digital representation for  $\Delta C_M$  can be obtained. The value of  $C_{\text{REF}}$  is chosen as 0.2 pF for a  $V_{\text{TX}}$  of 3.3 V, considering the stability of the modulator, and designed to be tunable in the range of 0.1–0.3 pF to cover various  $V_{\text{TX}}$ . Since the signal swing in the loop filter is maintained regardless of the number of TX driving, voltage  $V_{\text{TX}}$ , and capacitor  $C_M$ , it can provide sufficient SNRs under various touch environments.

To implement an energy-efficient  $\Delta\Sigma$  modulator, the over-sampling ratio (OSR), which is the number of cycles to produce a digital output, should be minimized. A minimum OSR can be calculated to bring the kTC noise ( $C_M \sim 1$  pF) to the target resolution ( $\sim 0.2$  fF) and the quantization noise also should be matched to the same noise level with similar OSR. Otherwise, the  $\Delta\Sigma$  modulator becomes a quantization-noise-limited design, requiring unnecessarily high number of cycles. Therefore, the order of modulator has been increased to the 2nd-order to achieve the sensing resolution of 0.18 fF with the OSR of 120, while the use of the 3rd-order modulator would not provide a reduction of OSR in this paper. Fig. 9(c) shows a block diagram of the implemented 2nd-order  $\Delta\Sigma$  modulator. The input signal is the rectified current  $I_{\text{SIG}}$ , and the CDAC is used for the charge balancing. A feed forward architecture is employed without direct path from  $Q_X$  to the input of the quantizer, providing the signal transfer function of a low-pass filter. The designed coefficient provides a usable input range of  $\pm 0.9 \times C_{\text{REF}}$ , and the output swing of the 1st integrator is maintained within a range of 30% of the supply voltage.

#### D. Decimation Filter

A digital decimation filter produces a multi-bit digital code from the bit stream of the  $\Delta\Sigma$  modulator for each readout channel. In order to achieve sufficient quantization-noise filtering, the order of the decimation filter should be matched to that of the modulator. For the 2nd-order incremental  $\Delta\Sigma$  modulator, both 2nd-order cascade-of-integrators ( $\text{Col}^2$ ) and  $\text{sinc}^2$  filters can be considered as a candidate, whose filter

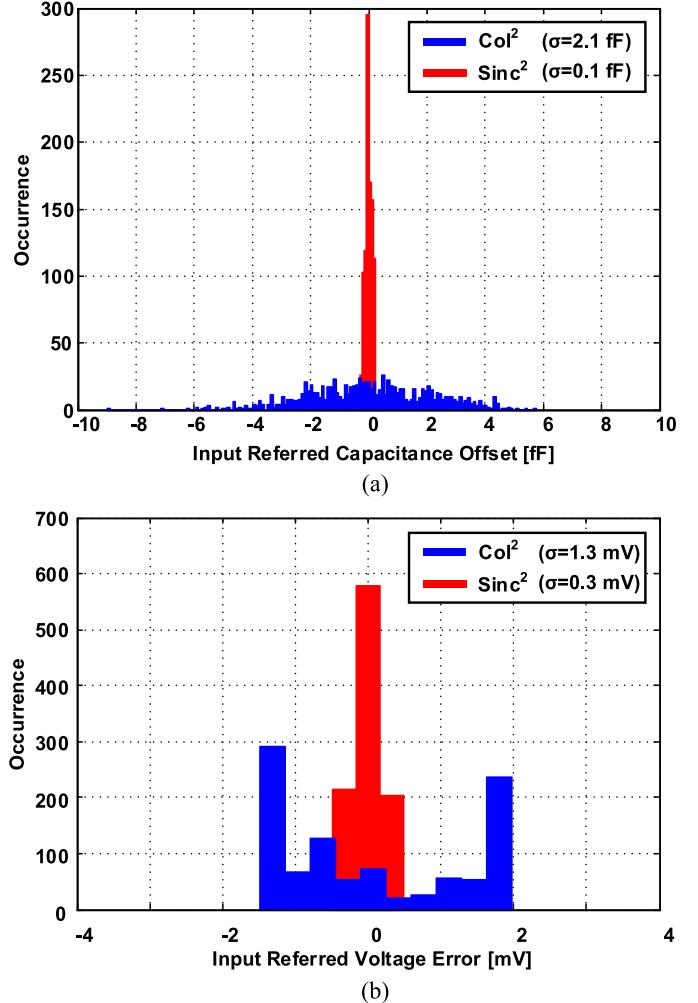


Fig. 11. Input-referred (a) capacitance offset by initial offset and (b) voltage error by high-frequency noise of the  $\text{Col}^2$  and  $\text{sinc}^2$  filters (total 1000 samples).

coefficient and transfer function are shown in Fig. 10 [17]. Although the decimation efficiencies of two filters are well recognized in [5], [12], [17], and [18], a survey of the literature suggests that the practical aspects, such as initialization and interference, are rarely described and thus we will evaluate them in this paper.

At the start of the conversion, both the modulator and decimation filer are reset, which brings the modulator in a well-known state. In practice, the integrator imposes an initial offset and its offset variations mainly caused by the reset switches, and the asymmetric coefficient of the  $\text{Col}^2$  filter gives large weights (as large as OSR) to the initial bit streams, thus resulting in offset errors. Therefore, the offset errors can be significant, making severe channel variations for multi-channel readouts. In contrast, a  $\text{sinc}^2$  filter, which has the symmetric filter coefficient, is less sensitive to the initial offset variations, because the filter's weights are small values for initial bit streams. Fig. 11(a) shows the input-referred capacitance offset comparison for the  $\text{Col}^2$  and  $\text{sinc}^2$  filters, when the same  $\Delta\Sigma$  modulator is used and an initial random offset (max 10% of  $V_{\text{DD}}$ ) is added at the integrator's output. The standard deviations of the capacitance offset for

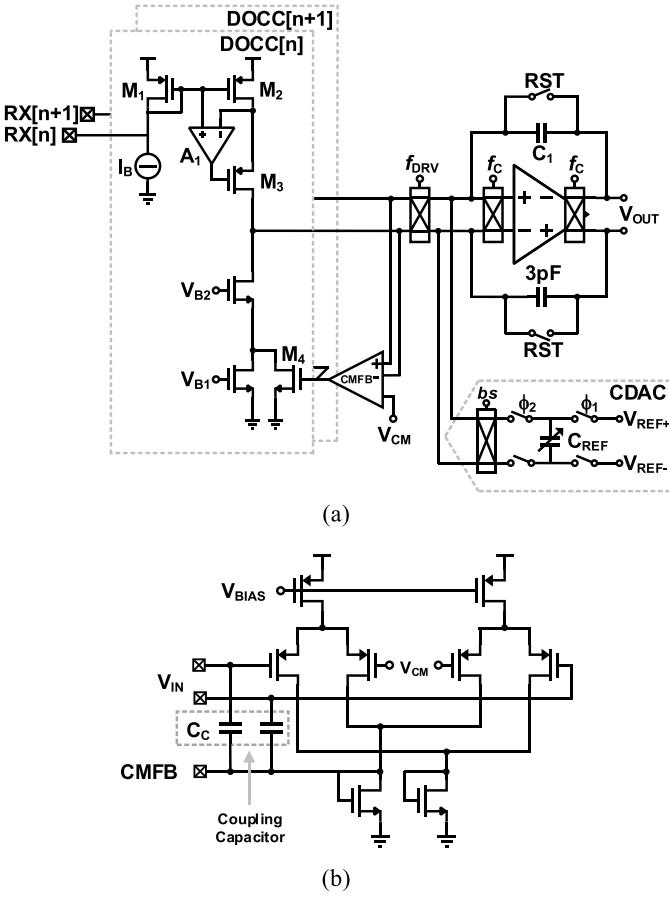


Fig. 12. Schematic of (a) DOCC with the 1st integrator and (b) CMFB.

the  $\text{CoI}^2$  and  $\text{sinc}^2$  filters are 2.1 and 0.1 fF, respectively. It means that the  $\text{CoI}^2$  filter is 21 times more sensitive to initial offset variation than the  $\text{sinc}^2$  filter. Another disadvantage of the  $\text{CoI}^2$  filter is that it does not have notches of the  $\text{sinc}^2$  filter, which appears at selective frequency and its harmonic owing to symmetry of filter coefficient. Since the readout suffers from high-frequency noise in the touch sensor applications, these notches are used for filtering out of high-frequency noises from the sensor. Fig. 11(b) shows the input-referred voltage error comparison for the  $\text{CoI}^2$  and  $\text{sinc}^2$  filters, when the interference noise (20% amplitude of  $V_{DD}$ ) uniformly distributed from 100 to 200 kHz is applied at the input. The voltage error of the  $\text{CoI}^2$  filter is almost four times larger than that of the  $\text{sinc}^2$  filter. Therefore, the  $\text{sinc}^2$  filter provides better noise immunity against large external noise such as display noise. Considering these benefits, the  $\text{sinc}^2$  filter is used in this paper. Although the  $\text{sinc}^2$  filter is rather complex to implement, but area- and power-efficient implementation of the  $\text{sinc}^2$  filter is proposed, which will be described in Section IV.

#### IV. IMPLEMENTATION DETAILS

##### A. Dual-Output Current Conveyor AFE

Fig. 12(a) shows the schematic of the proposed DOCC AFE, which also acts as the first integrator of the current-driven  $\Delta\Sigma$  modulator. The input current from the TSP is injected into the sensing branch and subsequently, it is mirrored in the

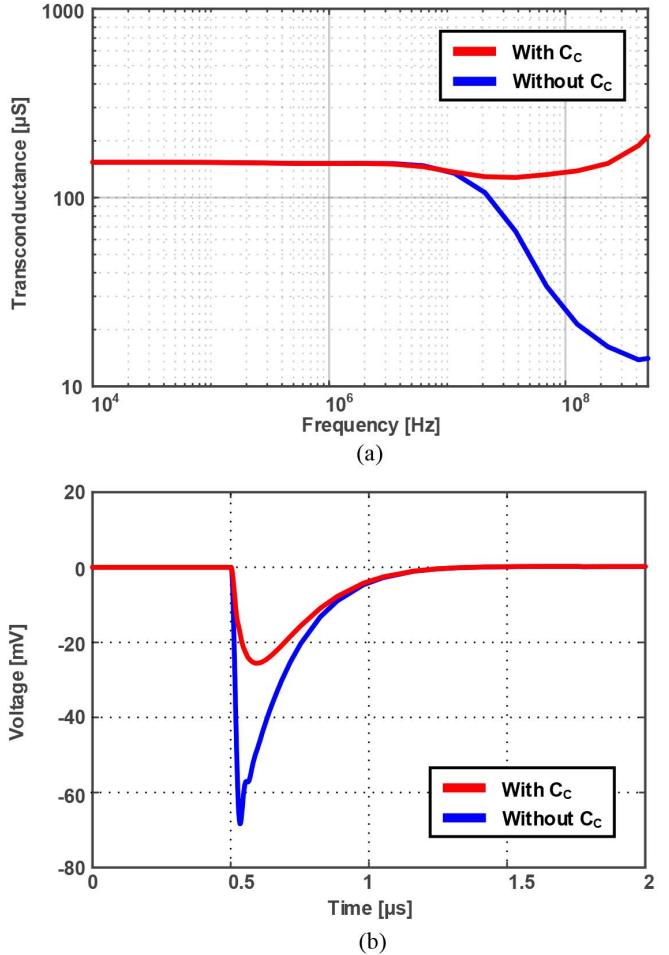
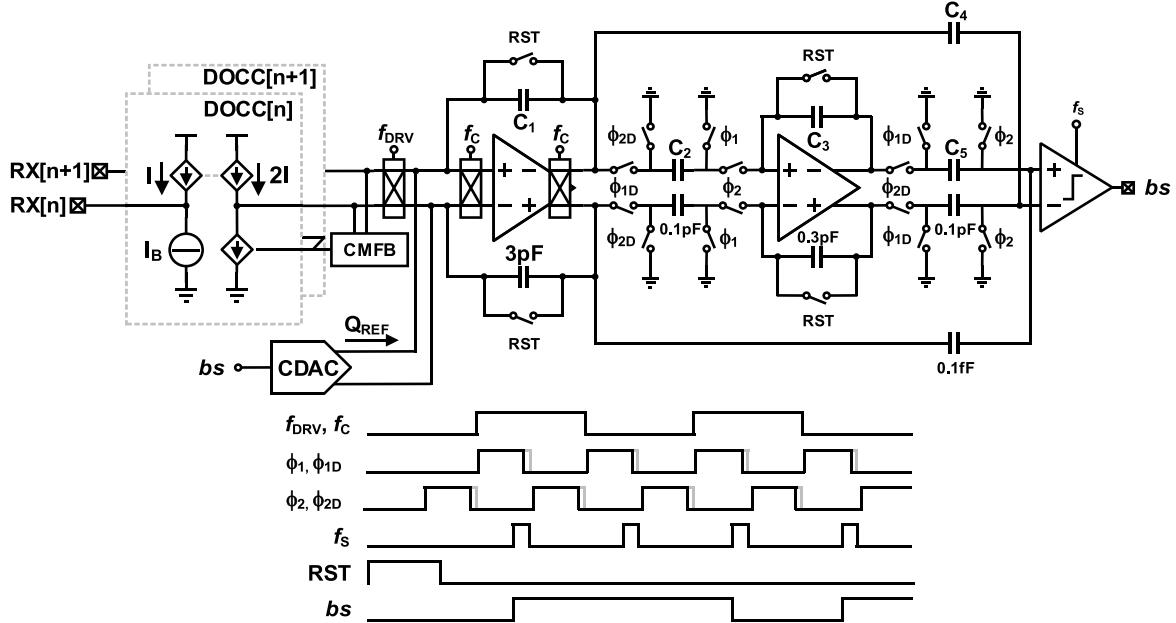
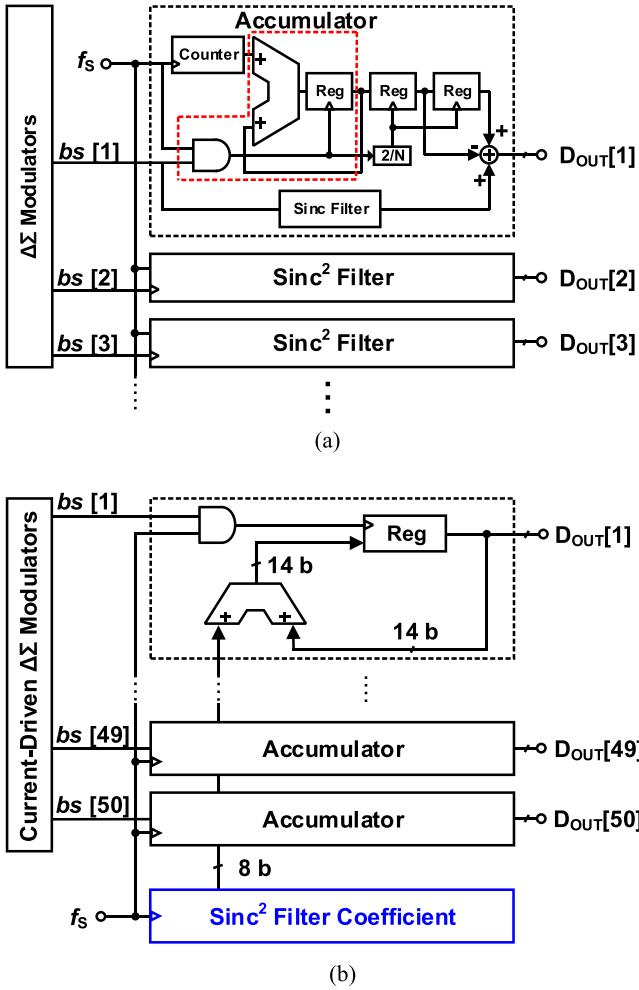


Fig. 13. (a) Frequency response of CMFB. (b) Transient response of 1st integrator's common-mode output by current pulse input.

reference current  $I_B$  by a gain of 2, realized by the transistors size ratio of  $M_1$  ( $W/L = 11/0.5 \mu\text{m}$ ) and  $M_2$  ( $22/0.5 \mu\text{m}$ ). The reference current  $I_B$  is determined by two design parameters, the target input impedance and the maximum input charge. The input impedance of the sensing branch should be sufficiently small for an operating frequency of TX. Furthermore,  $I_B$  should be sufficiently large to accommodate the external noise to avoid signal clipping due to saturation. In this paper,  $I_B$  of 10  $\mu\text{A}$  is selected to achieve sufficient  $g_m$  (130  $\mu\text{S}$ ). Moreover, it provides an acceptable charge of 25 pC at a TX frequency of 200 kHz. Considering  $C_M$  of 1 pF and TX voltage of 3.3-V, an extra charge of 20 pC remains for external noise, such as display and charger noise. For instance, this provides an ability to handle interference from a coupling capacitor of 1 pF with a charger noise of 20-V [2], [5] or a coupling capacitor of 20 pF with a display noise of 1 V [3]. The accuracy of the current conveyor can be improved with the aid of the auxiliary amplifier  $A_1$  with the cascode transistor  $M_3$  that forces the gate and drain of  $M_2$  to have the same voltage. As a result, the current conveyor achieves 1% gain error over the entire input current range. The common noise from the two adjacent TSP channels and the baseline current from  $C_M$  are removed by a common-mode feedback (CMFB) circuit at the

Fig. 14. Proposed current-driven  $\Delta\Sigma$  modulator and timing diagram.Fig. 15. Block diagram of (a) conventional and (b) proposed sinc<sup>2</sup> filters.

output of the DOCCs, as shown in Fig. 12(b). To improve the high frequency CMRR, coupling capacitors  $C_C$  (200 fF each) are employed. During the current transfer, the gate of the  $M_4$  is

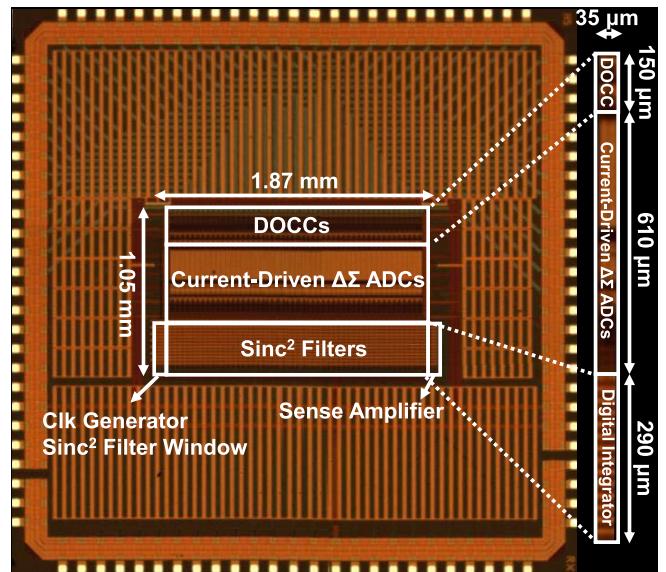


Fig. 16. Chip micrograph.

traced to the DOCC outputs, which improves response speed. Fig. 13(a) shows the frequency response of transconductance  $I_{CM}/V_{IN}$ , where  $I_{CM}$  is common-mode current output of transistor  $M_4$  and  $V_{IN}$  is voltage input of CMFB. Owing to  $C_C$ , the transconductance of high frequency region is enhanced. Fig. 13(b) shows the common-mode voltage output of 1st integrator when common input current pulse of 5  $\mu$ A is injected. Due to the enhancement of high frequency response with  $C_C$ , the common-mode voltage output shows faster response than that without  $C_C$ . The CMFB achieves a CMRR of 49 dB at  $f_{DRV}$  of 200 kHz. The current signal from the DOCC is demodulated to the baseband using the demodulation chopper before the first integrator and the dc offset and  $1/f$  of the DOCC are modulated and removed in the first integrator.

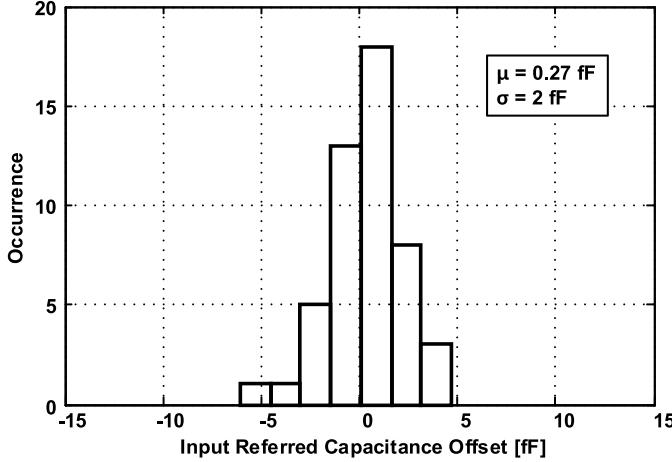
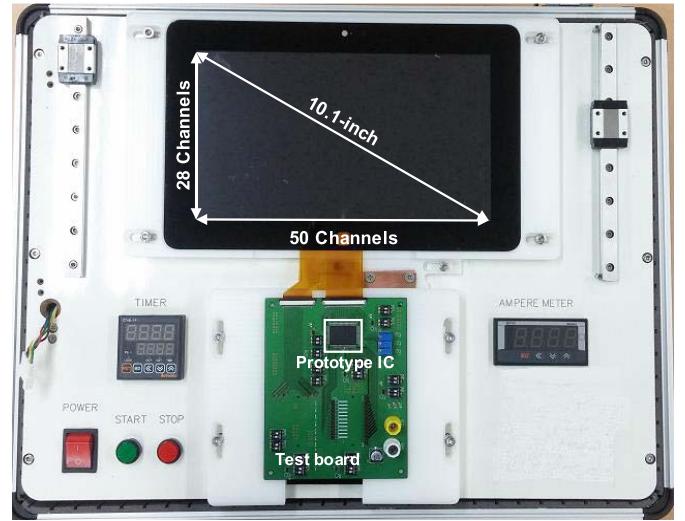
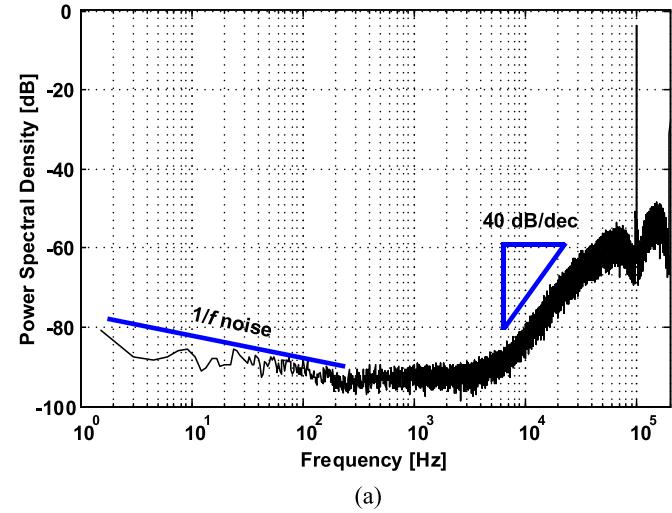
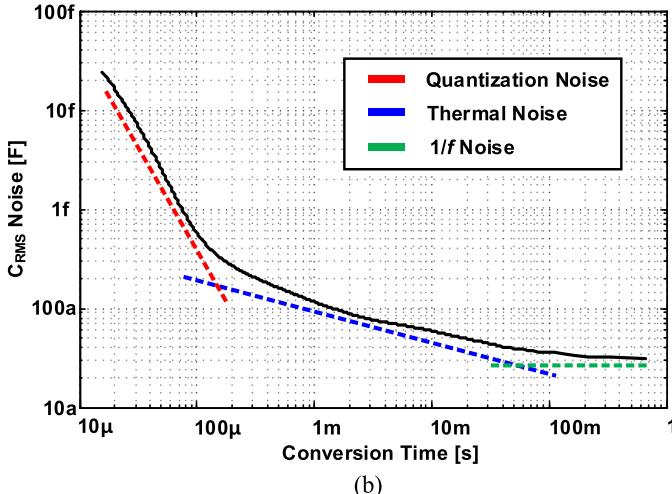


Fig. 17. Measured input-referred capacitance offset variation of 50 channels.

Fig. 19. Measurement setup for 10.1-in 28  $\times$  50 channels TSP.

(a)

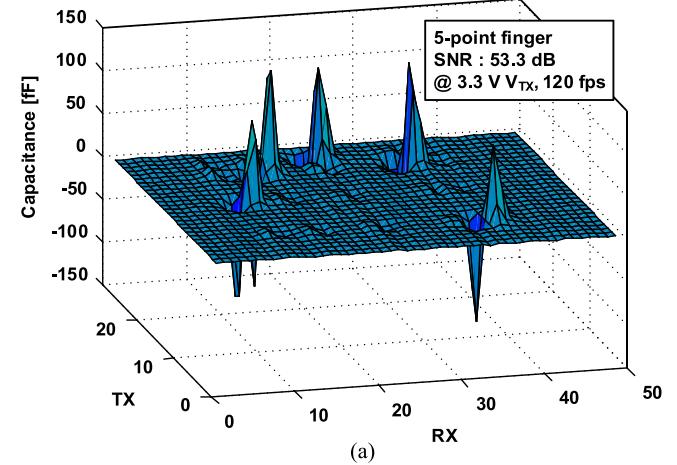


(b)

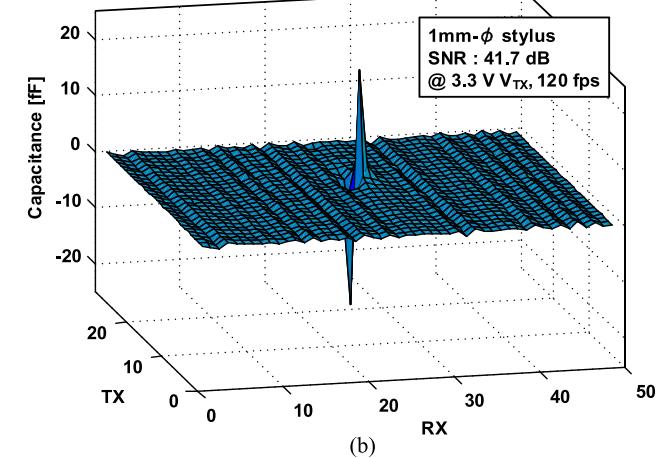
Fig. 18. Measured (a) PSD of the 2nd-order  $\Delta\Sigma$  modulator. (b) Capacitance RMS noise.

### B. Current-Driven $\Delta\Sigma$ Modulator

Fig. 14 shows the schematic of the proposed current-driven  $\Delta\Sigma$  modulator. The  $Q_{\text{REF}}$  from CDAC, which is determined by the sampled charge from  $C_{\text{REF}}$  and  $V_{\text{REF}}$ , is integrated



(a)



(b)

Fig. 20. Measured images for (a) five-point finger and (b) 1-mm- $\phi$  stylus.

with the DOCC output current at the first integrator and  $C_{\text{REF}}$  is implemented to be adjustable to control the feedback gain. The first integrator is designed using a folded-cascode OTA with a chopper for reducing offset and  $1/f$  noise. The chopping frequency,  $f_C$ , is selected as half of the sampling

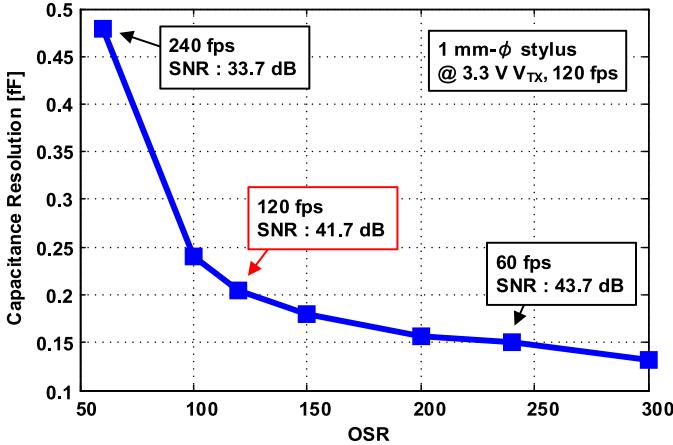


Fig. 21. Measured capacitance resolution versus OSR.

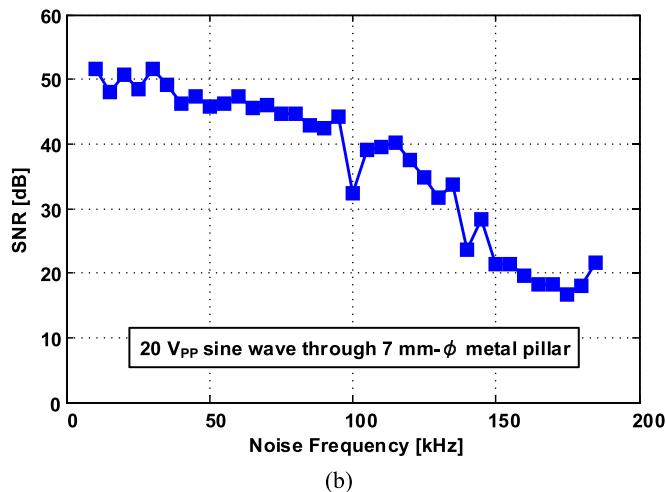
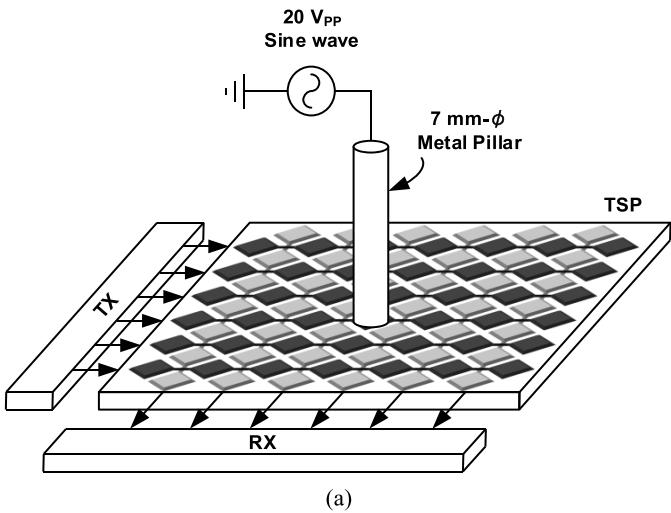


Fig. 22. (a) Measurement setup for in-band noise immunity. (b) Measured SNR versus in-band noise frequency.

frequency ( $f_S/2$ ) to prevent aliasing of high frequency quantization noise. The value of  $g_m$  (33  $\mu$ S) of this OTA can be small since it drives a small load capacitance. Because the charge balancing maintains the output of the first integrator at

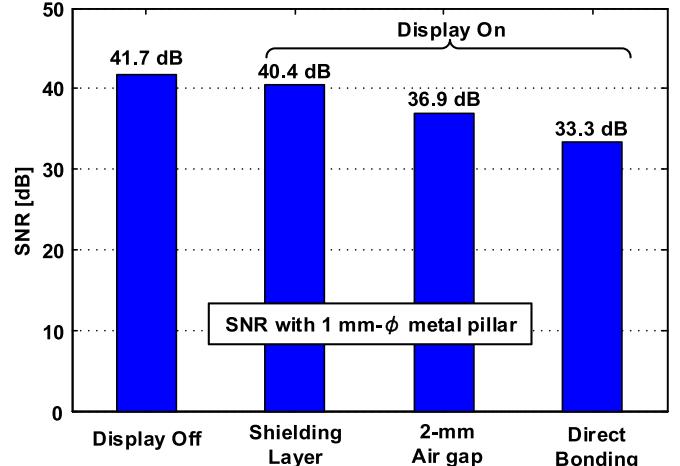


Fig. 23. SNR with display noise according to panel bonding condition.

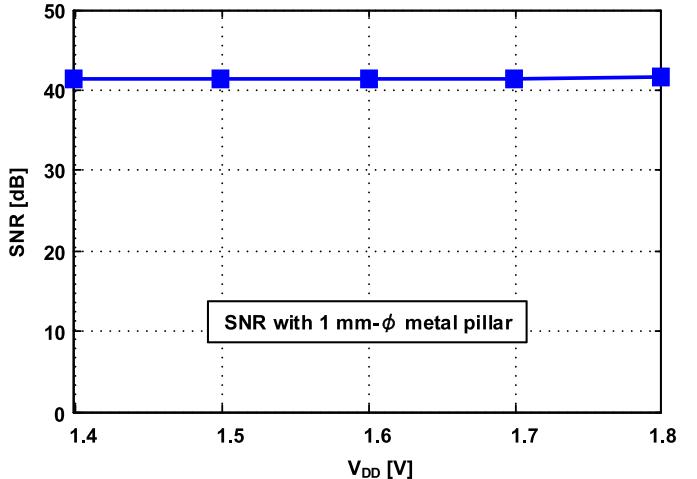


Fig. 24. SNR variation according to supply voltage.

certain range, the feedback capacitor  $C_F$  can be small (3 pF) even with a 1.8-V supply. Due to the small  $C_F$ , the output might be saturated by large external noise. However, the charge balancing forces the output to be settled at the desired level after a few sampling cycles. Therefore, the oversampling of the  $\Delta\Sigma$  modulator reduces the effect of the signal saturation and limits the effects of SNR degradation. Before the ADC cycle, two integrators are reset and then the  $\Delta\Sigma$  modulator starts the conversion. The modulator uses a non-overlapping clock with a delayed falling edge to mitigate signal-dependent charge injection. The sampling capacitor of the second stage is reduced to 0.1 pF and a passive adder is used at the input of the quantizer. A 1-bit comparator is implemented with a dynamic comparator.

### C. Sinc<sup>2</sup> Decimation Filter

The sinc<sup>2</sup> filter is used for providing the digital output  $D_{OUT}$  from the  $bs$  of each  $\Delta\Sigma$  modulator. The conventional sinc<sup>2</sup> filter has been implemented using an accumulator, sinc filter, counter, and register, as shown in Fig. 15(a). However, this filter has significant area and power overhead for 50-channel

implementation. Therefore, we propose a novel  $\text{sinc}^2$  filter that shares a filter coefficient implemented using an 8-bit up/down counter at the chip level. The counter output is uploaded to each digital integrator. Its accumulator designed using a 14-bit digital integrator is implemented in each channel, and determines the integration of the filter coefficient according to  $bs$ , as shown in Fig. 15(b). The filter coefficient obtained from the coefficient generator changes at every cycle, but the accumulator does not work at low  $bs$ . Since the up/down counter consumes ten times more power than the accumulator, this work achieves a significant power savings. Moreover, the proposed  $\text{sinc}^2$  filter also doubles the area efficiency in a  $0.18\text{-}\mu\text{m}$  CMOS technology. It should be noted that the proposed structure can be applied for various decimation filters by simply changing the filter coefficient.

## V. MEASUREMENT RESULTS

A  $1.96\text{-mm}^2$ , 50-channel prototype IC has been fabricated in a  $0.18\text{-}\mu\text{m}$  CMOS process, as shown in Fig. 16. The single channel occupies only  $0.037\text{ mm}^2$ , including the DOCC, 2nd-order  $\Delta\Sigma$  modulator, and  $\text{sinc}^2$  filter. The total power consumption is  $6.85\text{ mW}$  at the supply voltage of  $1.8\text{-V}$ . Fig. 17 shows the input-referred capacitance offset of  $0.27\text{ fF}$  with a standard deviation of  $2\text{ fF}$  over 50 channels. The noise power spectral density (PSD) of a single channel represents a 2nd-order noise shaping with noise floor of  $-90\text{ dB}$ , suppressing  $1/f$  noise by chopping, as shown in Fig. 18(a). The capacitance noise in RMS over the conversion time is shown in Fig. 18(b). As the conversion time increases, the dominant noise source changes from quantization noise to thermal noise, and the  $1/f$  noise limits the noise enhancement by integration.

### A. Touch Sensor Measurement

The  $28 \times 50$  channel 10.1-in glass-film-film structure TSP is attached to  $1366 \times 768$  LCD display, and it is connected to the fabricated IC, as shown in Fig. 19. A TX driver, providing sequential pulse of  $3.3\text{-V}$  and consuming  $0.05\text{ mW}$ , is used for the TSP measurement. It consists of a voltage buffer and a 1-to-28 multiplexer. The SNR for touch sensors can be calculated as follows [3]:

$$\text{SNR (dB)} = 20 \log \frac{S_{\text{Touch}}}{N_{\text{Touch}} \text{RMS}_{100}} \quad (4)$$

where  $S_{\text{Touch}}$  is averaged touch data over 100 sample and  $N_{\text{Touch}} \text{RMS}_{100}$  is the standard deviation of 100 samples, which can be also defined as the capacitance resolution. As shown in Fig. 20, the touched signals obtained by a five-point finger and  $1\text{-mm-}\phi$  metal pillar are measured under the driving voltage of  $3.3\text{ V}$  and frame rate of  $120\text{ Hz}$ . The measured SNR for fingers and  $1\text{-mm-}\phi$  stylus are  $53.3$  and  $41.7\text{ dB}$ , respectively. The capacitance resolution exhibits a tradeoff relationship with the frame rate, as shown in Fig. 21. It should be noted that OSR of  $120$  is optimum since the quantization noise and thermal noise are well matched. Below this point, although the frame rate can be enhanced, the capacitance resolution worsens rapidly due to quantization noise. On the other hand, above the

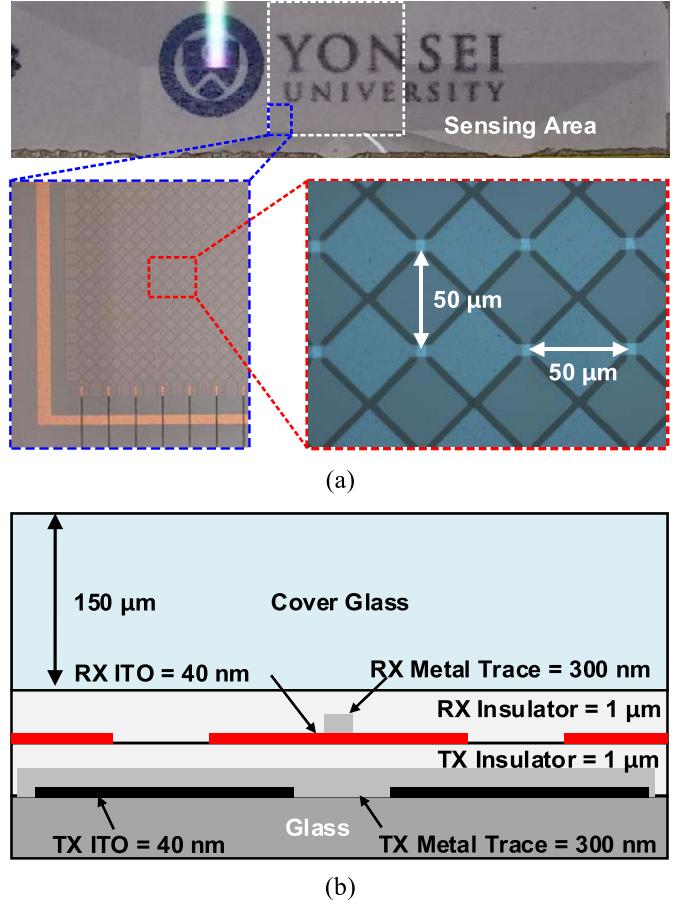


Fig. 25. (a) Micrograph of the fingerprint sensor and (b) its vertical structure.

optimal point, the capacitance resolution is slowly enhanced by the averaging of thermal noise. A capacitance resolution of  $0.19\text{ fF}$  is achieved at  $120\text{ fps}$  and can be enhanced to  $0.13\text{ fF}$  for an OSR of  $300$ .

The noise performance is measured when the in-band frequency of  $20\text{-}V_{\text{pp}}$  sinusoidal signal is injected through a  $7\text{-mm-}\phi$  metal pillar, as shown in Fig. 22(a). As shown in Fig. 22(b), the measured SNR is more than  $40\text{ dB}$  at a  $95\text{ kHz}$  noise frequency and the overall SNR remains above  $17\text{ dB}$ . Moreover, the degradation of SNR due to display noise is measured with several stack-up structures, as shown in Fig. 23. A shielding layer,  $2\text{-mm}$  air gap and direct bonding structures achieve the SNR of  $40.8$ ,  $36.6$ , and  $31.2\text{ dB}$ , respectively. We also investigate SNR measurements at lower supply voltage. As can be seen from Fig. 24, the proposed structure shows consistent performance for  $V_{\text{DD}}$  higher than  $1.4\text{-V}$ .

Table I shows the performance summary and comparison with previous published works. It is noted that the proposed touch sensor uses a supply voltage of  $1.8\text{-V}$  owing to differential current signaling and charge balancing, resulting in a reduction of power consumption. Moreover, the area-efficient structure achieves an area of  $0.04\text{ mm}^2$  per single channel, which is an improvement of more than four times on the previous state-of-the-art works. This work achieves a FoM of  $0.41\text{ nJ/step}$  for  $1\text{-mm-}\phi$  stylus, which

TABLE I  
PERFORMANCE SUMMARY AND COMPARISON WITH THE OTHER STATE-OF-THE-ART WORKS

|                            |        | This work                               | [1]   | [3]                                    | [4]                                    | [5]   | [6]  | [9]  | [11] |
|----------------------------|--------|---|-------|--|--|-------|------|------|------|
| Technology [nm]            | 180    | 180                                     | 180   | 85                                     | 180                                    | 180   | 90   | 350  |      |
| Supply [V]                 | RX     | 1.8                                     | -     | 3.3 <sup>†</sup> /<br>1.8 <sup>‡</sup> | 3.3 <sup>†</sup> /<br>1.2 <sup>‡</sup> | 3.3   | 3.3  | -    | 3.3  |
|                            | TX     | 3.3                                     | 12    | 3.3                                    | 3.3                                    | 3.3   | 3.3  | -    | -    |
| Channel                    | RX     | 50                                      | 32    | 138                                    | 57                                     | 64    | 24   | 16   | 80   |
|                            | TX     | 28                                      | 48    | 78                                     | 35                                     | 36    | 30   | 28   | 80   |
| Frame Rate [Hz]            | 120    | 120                                     | 240   | 240                                    | 120                                    | 240   | 120  | 322  |      |
| Power [mW]                 | 6.9    | 30                                      | 559.9 | 56                                     | 94.5                                   | 52.8  | 24.6 | 21.8 |      |
| Area [mm <sup>2</sup> ]    | 1.96   | 14.7                                    | 71.2  | 12.5                                   | 36                                     | 14.86 | 15.9 | 13.7 |      |
| Power/RX [mW]              | 0.14   | 0.94                                    | 4.05  | 0.98                                   | 1.48                                   | 2.2   | 1.54 | 0.27 |      |
| Area/RX [mm <sup>2</sup> ] | 0.04   | 0.46                                    | 0.52  | 0.22                                   | 0.56                                   | 0.62  | 1    | 0.17 |      |
| SNR [dB]                   | Finger | 53.3                                    | 62    | 56.6                                   | -                                      | 54    | 55   | 60   | 41   |
|                            | 1 mm-Φ | 41.7 <sup>*</sup><br>40.4 <sup>**</sup> | 49    | 37.4                                   | 38                                     | 41    | 35   | 42   | 32   |
| FoM<br>[nJ/step]           | Finger | 0.11                                    | 0.16  | 0.39                                   | -                                      | 0.83  | 0.67 | 0.56 | 0.11 |
|                            | 1 mm-Φ | 0.41 <sup>*</sup><br>0.48 <sup>**</sup> | 0.71  | 3.58                                   | 1.8                                    | 3.73  | 6.65 | 4.45 | 0.33 |

$$\text{FoM} = \text{Power} / (2^{(\text{SNR}-1.76)/6.02} \times \# \text{ of node} \times \text{frame rate})$$

<sup>†</sup> For analog, <sup>‡</sup> For digital.

\* Display off, \*\* Display on

TABLE II  
PERFORMANCE SUMMARY AND COMPARISON WITH THE OTHER FINGERPRINT SENSORS

|                        | This work     |     | [19]                 | [20]                 | [21]                 | [22]             |       |
|------------------------|---------------|-----|----------------------|----------------------|----------------------|------------------|-------|
| Method                 | Capacitive    |     | Capacitive           | Capacitive           | Capacitive           | Ultrasonic       |       |
| Resolution [dpi]       | 500           |     | 508                  | 423                  | 500                  | 591 × 438        |       |
| Sensor pitch [μm]      | 50            |     | 50                   | 58                   | 50                   | 43 × 58          |       |
| Channels               | 70 × 50       |     | 224 × 256            | 160 × 192            | 256 × 224            | 110 × 56         |       |
| Transparency           | ○ (85%)       |     | ×                    | ×                    | ×                    | ×                |       |
| Sensor-IC Connection   | FPCB          |     | On-Chip (Integrated) | On-Chip (Integrated) | On-Chip (Integrated) | Vertical Bonding |       |
| Sensing Capacitor [fF] | With Glass    | 0.1 | 65                   | 43                   | -                    | -                |       |
|                        | Without Glass | 0.5 |                      |                      |                      |                  |       |
| Frame rate [Hz]        | 19            |     | 0.3–50               | 6.67                 | 3.3                  | Fast             | 380   |
|                        |               |     |                      |                      |                      | Slow             | 4     |
| Power [mW]             | 7.1           |     | 25                   | 35                   | -                    | Fast             | 106.4 |
|                        |               |     |                      |                      |                      | Slow             | 0.01  |

is four-time improvements compared to the state-of-the-art works.

### B. Fingerprint Sensor Measurement

A 500-dpi transparent on-glass fingerprint sensor is fabricated [25], and it is also measured using the same readout IC. The proposed sensor is designed to have a 50-μm pitch with

diamond patterns, as shown in Fig. 25(a) to recognize the small distance between ridges and valleys in the fingers. In order to ensure transparency, a 40-nm-thick TX and RX indium tin oxide electrode is connected to a metal trace with a 1-μm-thick insulator on the glass substrate, as shown in Fig. 25(b). The high TX voltage of is required with the OSR of 300 for small capacitor sensing, because the electrode layer is covered with 150-μm-thick glass, which results in a sensing

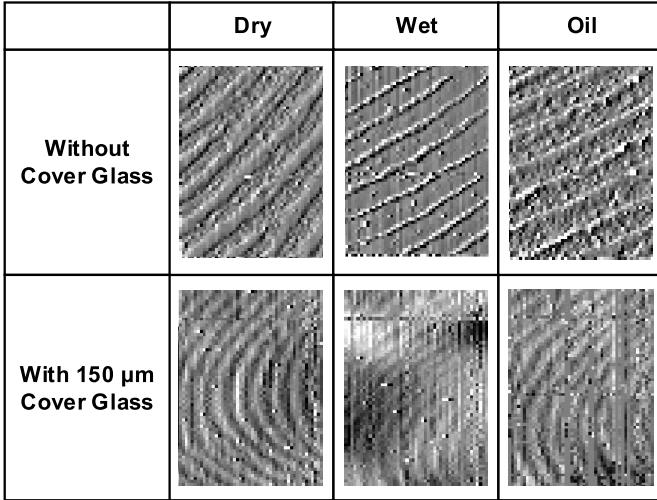


Fig. 26. Measurement results of a fingerprint with and without the cover glass.

capacitance less than 1 fF. A driver of 15-V consists of a 3.3-V TX driver and a voltage level shifter. Fig. 26 shows the successful measurement of  $70 \times 50$  sample images of a fingerprint assuming practical operating environment. The normal condition is denoted as “Dry.” Perspiration and some oil drops are labeled as “Wet” and “Oil,” respectively. In the SNR, although the capacitance resolution ( $NTouch_{RMS100}$ ) is defined in the same way as described in Section V-A, the signal ( $STouch$ ) should be defined as the capacitance difference of the fingerprint’s ridge and valley. The measured capacitance resolution is 34 aF at 19 fps, and the SNR of 10.3 and 23.5 dB are measured for each fingerprint with or without cover glass, respectively. Table II shows the performance comparison with the previous fingerprint sensors. This paper achieves sufficient performances compared to the conventional non-transparent fingerprint sensors.

## VI. CONCLUSION

An area- and energy-efficient capacitive touch readout is proposed using current conveyor AFE and current-driven  $\Delta\Sigma$  ADC. The current conveyor AFE enables baseline signal reduction and parasitic capacitor isolation from the amplifier, thus saving significant power consumption. The current-driven  $\Delta\Sigma$  ADC provides a direct digital conversion of the current signal to achieve high SNR. The prototype 50-channel IC is fabricated in a  $0.18\text{-}\mu\text{m}$  CMOS process, occupying only  $1.96\text{ mm}^2$ . It consumes only 6.9 mW at a supply voltage of 1.8-V. In combined with 10.1-in TSP and 3.3-V TX, this work achieves 53.3 and 41.7 dB SNR for fingers and 1-mm- $\phi$  stylus, respectively. This corresponds to the state-of-the-art FoMs of 0.11 and 0.41 nJ/step, respectively, which is four times less energy than the state-of-the-art. The capacitance resolution is further improved with increased TX voltage and OSR. Using a 500-dpi on-glass fingerprint sensor and 15-V TX, this work achieves the capacitor resolution of 34 aF and the fingerprint image is successfully measured at 19 fps with a cover glass of  $150\text{-}\mu\text{m}$  thickness.

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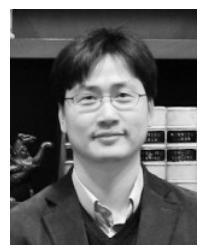
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