

A 1.24 μA Quiescent Current NMOS Low Dropout Regulator With Integrated Low-Power Oscillator-Driven Charge-Pump and Switched-Capacitor Pole Tracking Compensation

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Abstract—Supply regulation using low quiescent current linear regulators helps in extending the battery life of power aware applications with very long standby time. A 1.24 μA quiescent current NMOS low dropout (LDO) that uses a hybrid bias current generator (HBCG) which boosts the bias current dynamically and adaptively to improve the transient response is presented in this paper. A bias-current scalable error amplifier with an on-demand pull-up/pull-down buffer drives the NMOS pass device. The error amplifier is powered with an integrated dynamic frequency charge pump to ensure low dropout voltage. A low-power relaxation oscillator (LPRO) generates the charge pump clocks. A novel switched-capacitor pole tracking (SCPT) compensation scheme is proposed to ensure stability up to maximum load current of 150 mA with a low-ESR 1 μF output capacitor. Designed in a 0.25 μm CMOS process, the LDO has an output voltage range of 1–3 V, a dropout voltage of 240 mV, and a core area of 0.11 mm^2 .

Index Terms—Adaptive biasing, dynamic biasing, hybrid biasing, low I_Q low dropout (LDO), NMOS LDO, on-demand buffer, relaxation oscillator, switched-capacitor tracking compensation.

I. INTRODUCTION

PORTABLE devices, low-power micro-controller unit system-on-chip (SoC) ICs, always-on Internet-of-things (IoT) sensor systems, and biomedical devices rely on various power saving schemes to increase their battery life. Sleep/standby mode operation, dynamic supply voltage scaling, and on/off supply schemes have been presented in [1] and [2] for low-power operation where event-driven, on-demand, fast wake-up schemes are used to ensure fast response time. Due to these schemes, the standby power consumption of such systems is dominated by their supply regulators. Such supply regulators need to have two critical features: very low-power consumption during standby mode and fast response to transient load currents during fast wake-up. Thus, output

capacitor stabilized low dropout (LDO) regulators powering such applications must have low-power dissipation for better efficiency during light load current (I_{LOAD}) condition while maintaining good transient response to switching load current with minimum variation in their output voltage (V_{OUT}). The undershoot/overshoot voltage (ΔV_O) of an LDO with output capacitor (C_{LOAD}) is given by [3] as follows:

$$\Delta V_O \approx \frac{\Delta I_{\text{LOAD}}}{C_{\text{LOAD}}} t_R = \frac{\Delta I_{\text{LOAD}}}{C_{\text{LOAD}}} (t_{\text{BW}} + t_{\text{SR}}) \quad (1)$$

where Δt_R is the recovery time to load current transients. This recovery time is governed by the small-signal propagation delay associated with the LDO loop bandwidth (t_{BW}) and the large signal delay associated with the limited slew rate at the parasitic gate capacitance of pass device (t_{SR}). Both t_{BW} and t_{SR} can only be reduced at the expense of increased power consumption.

In order to ensure low no-load quiescent current (I_Q) while achieving fast transient response, various current scaling schemes have been presented. Adaptive biasing schemes scale the bias current proportional to I_{LOAD} as presented in [4] and [5]. This approach gives the benefit of better slew rate and better loop bandwidth at higher I_{LOAD} . However, due to low bias current at light load conditions, the recovery time and undershoot for zero to full-load transition of low- I_Q LDOs, cannot be minimized with this scheme as the loop response is slow to begin with. Dynamic slew rate enhancement schemes are presented in [6]–[11] where the slew rate at the gate of the pass device is scaled only during the load transient event, thereby reducing undershoot voltage. This technique alone is very effective in output capacitor-less LDOs where the parasitic gate capacitance tends to decide the dominant pole as well as the required slew rate. In general, low I_Q output capacitor-less LDOs offer limited maximum load current capability and suffer from large undershoot voltage during zero to full-load current step. Lu *et al.* [12] present a fully integrated NMOS LDO which generates a low-ripple regulated output voltage by efficiently managing the available supply voltage for the error amplifier and the switched-capacitor dc–dc converter output as the supply for pass device. However, due to unavailability of a good output storage capacitance in this fully integrated scheme, it suffers from large undershoot voltage for a relatively small load

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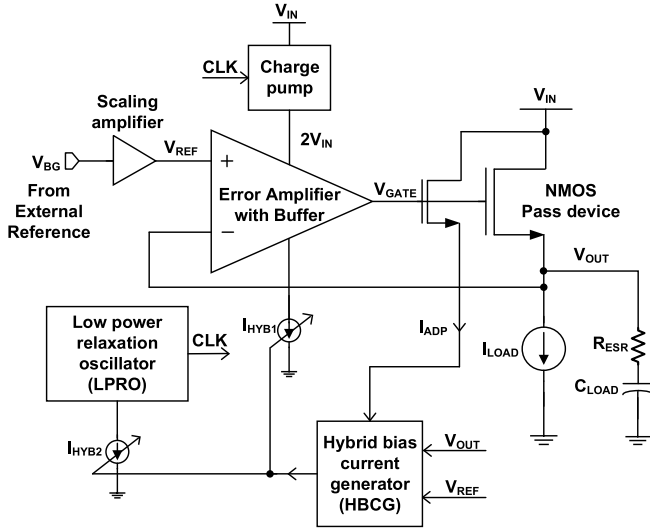
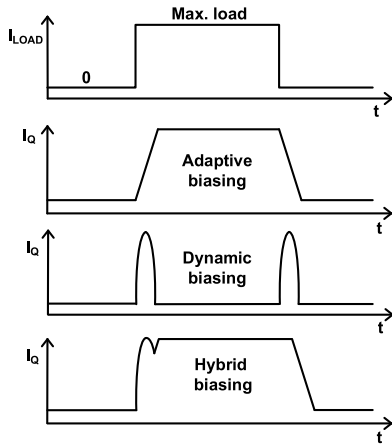


Fig. 1. Block diagram of the proposed NMOS LDO.

Fig. 2. Comparison of the proposed hybrid biasing scheme with previously presented I_Q scaling schemes.

current transient. Recently, LDOs which employ dynamic slew enhancement along with adaptive biasing have been reported in [13]–[16]. Although increased slew rate helps in reducing t_{SR} as shown in (1), high t_{BW} due to limited loop bandwidth at light load currents can still limit the total recovery time Δt_R for zero to full-load current transients, especially in output capacitor stabilized LDOs.

This paper presents an NMOS pass-device LDO with a low I_Q of 1.24 μ A. The block diagram of this LDO is shown in Fig. 1. Superior transient response, low output impedance even at light load currents and lower gate parasitic capacitance due to smaller physical size are the three distinct advantages which make NMOS a favorable choice for pass device in comparison to PMOS. A bias-current scalable, two-stage error amplifier with an on-demand pull-up (PU)/pull-down (PD) buffer drives the pass device. A hybrid bias-current generator (HBCG) that scales the bias current dynamically during load transients and adaptively with I_{LOAD} is proposed for improved transient response. This HBCG scheme allows faster I_Q scaling which improves both loop bandwidth and slew rate of the error amplifier even at light I_{LOAD} . Fig. 2 shows a comparison of the bias-current profile of the HBCG scheme

with earlier presented current scaling techniques. Low dropout voltage for this NMOS LDO is ensured by powering the error amplifier with a charge-pump voltage doubler. Native NMOS which offers negative or close to zero threshold voltage may seem like a better pass device alternative to using a charge-pump along with regular NMOS pass device. However, additional mask cost, larger area due to higher minimum length, and higher levels of drain to source leakage current are major limitations of native NMOS which make the charge-pump and regular NMOS a preferable choice especially in such low- I_Q LDOs. A dynamic frequency charge-pump is employed for powering the hybrid-mode biased error amplifier, which acts as a variable load. A very low-power relaxation oscillator (LPRO) is proposed to generate the charge pump clocks with clock frequency proportional to I_{LOAD} . Switched-capacitor pole tracking (SCPT) compensation scheme is proposed for loop stability across load conditions. This LDO provides a maximum I_{LOAD} of 150 mA while using a low-ESR 1 μ F load capacitor (C_{LOAD}). A low-power scaling amplifier shifts the external reference voltage of 0.8 V to an internal reference (V_{REF}) equal to the required output voltage (V_{OUT}) and the error amplifier is operated in unity gain configuration.

The rest of this paper is organized as follows. Analysis and design details of the proposed HBCG circuit are presented in Section II. Section III covers the design details of the bias-current scalable error amplifier with buffer while Section IV presents the design of the proposed low-power LPRO circuit. Stability analysis and SCPT compensation scheme are presented in Section V. Section VI presents the measurement results and Section VII draws the conclusion.

II. HYBRID BIAS-CURRENT GENERATOR (HBCG)

Fig. 3 shows the design details of HBCG circuit. As noted earlier, this circuit is responsible for both adaptive current scaling and dynamic current scaling. Load-dependent adaptive current is obtained by MN1, which mirrors a fraction (1:4000) of the pass device (MNP) current. In order to ensure accurate mirroring, the source voltage of MN1 needs to be equal to V_{OUT} . This is achieved using the current mirrors MN2 and MN3 along with MP1 and MP2. As I_{LOAD} increases, drain-source current in MN1 also increases and current mirror pair MN2 and MN3 ensures equal current flow in both branches, forcing MP1 and MP2 to have the same V_{GS} . As the gate terminal is common to both MP1 and MP2, the source voltage of MP2 which is V_{OUT} is copied onto the source terminals of MP1 and MN1. MN4 mirrors the final adaptive current (I_{ADP}). At zero I_{LOAD} , MN1 is in deep subthreshold region and does not conduct any current. Effectively, the entire adaptive scaling implementation has no contribution in the overall I_Q of the LDO and serves as a major advantage in such low I_Q LDOs. At startup, the gate voltage of MN2 and MN3 is pulled down to ground by the diode connected MN2. However, the common-gate voltage of both MP1 and MP2 is indeterministic at startup and if it is close to V_{DD} , the entire adaptive scaling circuit may fail to turn on even when I_{LOAD} increases as MP1 and MP2 will remain in OFF state. In order to avoid this faulty case, their gate node is discharged to ground by MN5 using a short pulse V_{STUP} at startup.

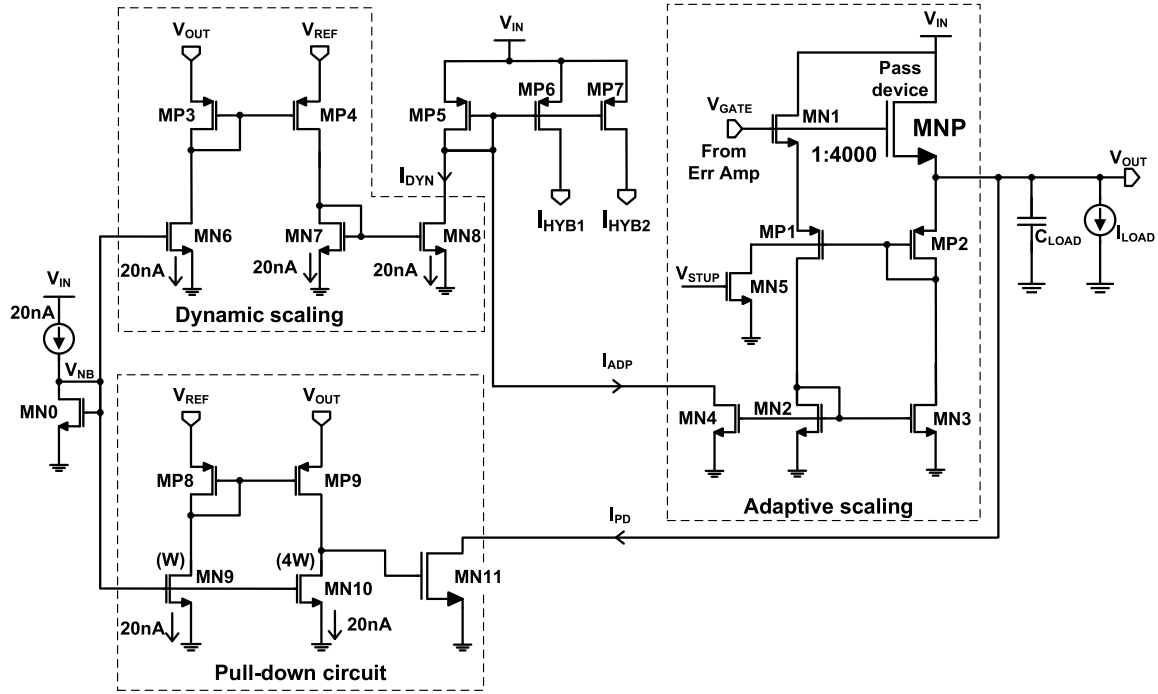


Fig. 3. HBCG with on-demand output capacitor pull-down circuit.

Fast dynamic current scaling is based on virtual ground error voltage ($\Delta V = V_{OUT} - V_{REF}$) which is obtained by monitoring the input voltages of the error amplifier. Fast detection is achieved by utilizing PMOS common-gate differential pair with source terminals as inputs. As shown in the dynamic scaling segment of Fig. 3, the input pair consists of highly matched MP3 and MP4 transistors operating in subthreshold region. When the LDO is in steady state, the error voltage $\Delta V \approx 0$ and the 20 nA bias current is mirrored to generate $I_{DYN} = 20$ nA through MP3 and MP4 and MN7 and MN8 current mirrors. However, during an output undershoot event ($\Delta V < 0$) caused due sudden step-up of I_{LOAD} , the undershoot in V_{OUT} produces an increased gate drive (ΔV_{SG}) for MP4 through diode connected MP3. Effectively, current through MP4 which is biased in subthreshold region increases exponentially and is mirrored by MN7 and MN8 resulting in an exponential increase in I_{DYN} . Due to the absence of high-impedance paths, this scheme provides instantaneous current scaling during load transients.

The adaptive current (I_{ADP}) is added to dynamic current (I_{DYN}) and then mirrored by MP5–MP6, MP7 to generate the bias currents of the error amplifier (I_{HYB1}) and oscillator (I_{HYB2}). In addition, a current-comparator-based, on-demand pull-down circuit (PD) circuit is added to discharge the load capacitor (C_{LOAD}) during an overshoot event ($\Delta V > 0$) caused due to sudden step-down of I_{LOAD} . A subthreshold biased PMOS pair MP8 and MP9, similar to that of dynamic scaling circuit with reversed input voltage terminals is used as shown in the pull-down circuit segment of Fig. 3. In comparison with MN9, a 4 times stronger current source MN10 is used to hold the gate of pull-down circuit device MN11 to less than 15 mV which is much lower than the NMOS threshold voltage of 550 mV. Such low gate voltage ensures that there is

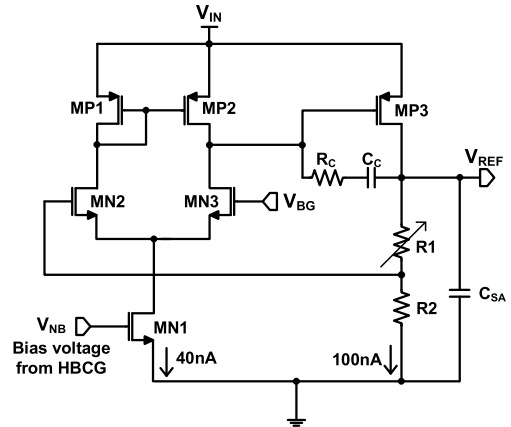


Fig. 4. Scaling amplifier with programmable resistor divider feedback.

no unexpected leakage current through MN11 during steady-state operation of the LDO. However, during V_{OUT} overshoot, higher gate drive (ΔV_{SG}) increases the current through MP9. This current overpowers the current source MN10 and pulls the gate of MN11 high, thereby discharging C_{LOAD} . This pull-down circuit is triggered only when the ΔV exceeds ~ 35 mV.

Fig. 4 shows the scaling amplifier which generates the scaled reference voltage V_{REF} from the external reference V_{BG} . It consists of simple two-stage design with a differential amplifier as its first stage and a PMOS common source amplifier as its second stage driving a 2 pF output capacitance (C_{SA}). To keep the current branches to minimum, the bias voltage (V_{NB}) for the tail current source (MN1) is derived from MN0 of the HBCG circuit in Fig. 3 and both devices are closely matched in layout to minimize mismatch. The scaling amplifier is stabilized using Miller capacitance C_C

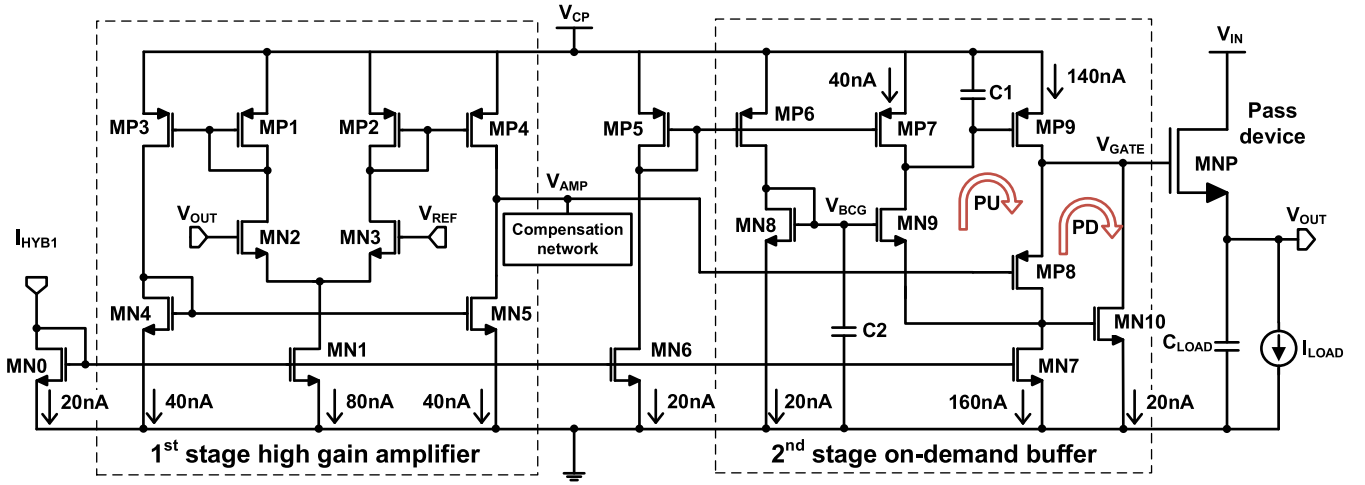


Fig. 5. Two-stage error amplifier with on-demand PU/PD buffer.

and resistor R_C is used to cancel the right half-plane zero associated with Miller compensation. Digitally programmable resistor divider with fixed R_2 and variable R_1 is used to generate V_{REF} corresponding to the LDO output voltage range of 1–3 V.

III. ERROR AMPLIFIER WITH ON-DEMAND PULL-UP/PULL-DOWN BUFFER

The regulation feedback loop consists of a two-stage error amplifier which is shown in Fig. 5. The charge-pump voltage doubler provides the supply voltage to this bias-current scalable error amplifier. Due to this $2 \times V_{IN}$ voltage supply which can go as high as 6 V when $V_{IN} = 3.3$ V, the error amplifier uses 7 V devices instead of 3.3 V devices. The pass device also is a 7 V regular NMOS. The bias current (I_{HYB1}) of the error amplifier is generated by the HBCG circuit. The first stage of the amplifier consists of a symmetrical operational transconductance amplifier (OTA). Small-signal analysis of this amplifier shows that the gain of the amplifier (G_{AMP}) and its 3 dB pole location (P_{AMP}) are given by

$$G_{AMP} \cong g_{m_{MN2}} * (r_{ds,MP4} || r_{ds,MN5}) \quad (2)$$

$$P_{AMP} \cong \frac{1}{2\pi(r_{ds,MP4} || r_{ds,MN5})C_{AMP}} \quad (3)$$

where C_{AMP} is the effective load capacitance at the output of the first stage. With increase in I_{HYB1} , although output impedance ($r_{ds,MP4} || r_{ds,MN5}$) drops, increase in $g_{m_{MN2}}$ compensates for this drop, thereby maintaining a dc gain higher than 50 dB for all possible I_{HYB1} values. However, its 3 dB bandwidth increases proportionally with I_{HYB1} as P_{AMP} moves to a higher frequency due to the reduction in output impedance.

A second-stage bias-current scalable dual-loop CMOS voltage buffer is placed in between the first stage and the pass device in order to increase the slew rate at the gate of the pass device and improve the load transient response. Unlike, the voltage buffer with only on-demand PU capability as shown in [3] and super-source follower buffer with only on-demand PD presented in [4], the proposed buffer achieves

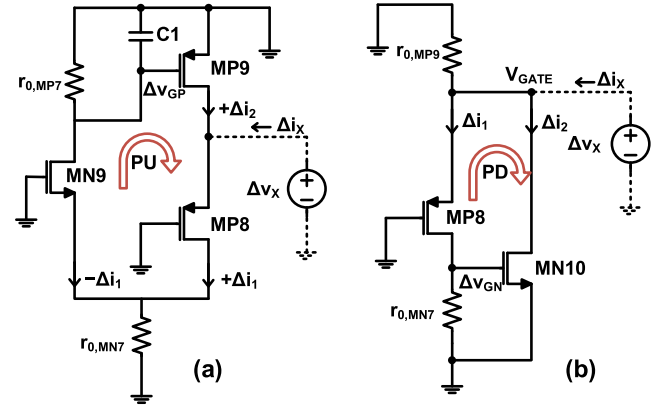


Fig. 6. Small-signal equivalent circuits for determining output impedance for active (a) PU loop and (b) PD loop of the proposed buffer.

on-demand fast PU as well as fast PD capability improving the transient response to I_{LOAD} step-up and step-down, respectively.

At the core, the buffer consists of a PMOS source follower (MP8). For simplicity, the PU and PD loops are analyzed separately. Instead of a regular source follower biased with a fixed current source, dynamic fast PU is achieved through a negative feedback loop realized using common-gate stage (MN9 and MP7) and common source stage (MP9) which constitute a cascoded flipped-voltage follower. This feedback loop not only provides the required on-demand sourcing current to charge the gate of pass device during a load step-up but also reduces the small-signal output impedance of the buffer. The effective output impedance can be calculated using the small-signal equivalent diagram, as shown in Fig. 6(a) for the PU loop. Small-signal test voltage Δv_x is applied at the output of the buffer with input v_{in} shorted to ground. The effective output impedance is given by

$$r_{0,PU} = \frac{\Delta v_x}{\Delta i_x} = \frac{\Delta v_x}{\Delta i_1 - \Delta i_2}. \quad (4)$$

The small-signal current $+\Delta i_1$ is translated to $-\Delta i_1$ onto the CG stage MN9, drops across the equivalent impedance

of $(r_{ds,MP7}||r_{ds,MN9})$ and is converted to voltage Δv_{GP} . This Δv_{GP} is converted to Δi_2 using MP9 and is given by

$$\Delta i_2 = g_{m_{MP9}} * \Delta v_{GP} \cong g_{m_{MP9}} * -\Delta i_1 * (r_{ds,MP7}||). \quad (5)$$

Using (4) and (5), we get

$$r_{0,PU} \cong \frac{\Delta v_x}{[1 + g_{m_{MP9}}(r_{ds,MP7}||r_{ds,MN9})]\Delta i_1}. \quad (6)$$

Substituting $\Delta i_1 = g_{m_{MP8}} * \Delta v_x$, we get

$$r_{0,PU} \cong \frac{1}{g_{m_{MP8}} * g_{m_{MP9}} * (r_{ds,MP7}||r_{ds,MN9})}. \quad (7)$$

Thus, the effective output impedance is reduced by a factor of loop gain given by $A_{PU} = g_{m_{MP9}} * (r_{ds,MP7}||r_{ds,MN9})$ in comparison to a simple source follower in which case it would have been just $(1/g_{m_{MP8}})$, thereby pushing the parasitic pole at the gate of pass device (P_{GATE}) to higher frequency. Similar analysis can be done for the fast PD loop which is a super-source follower formed by MP8, MN7, and MN10 as shown in Fig. 6(b) where the effective output impedance is given by

$$r_{0,PD} = \frac{\Delta v_x}{\Delta i_x} = \frac{\Delta v_x}{\Delta i_1 + \Delta i_2}. \quad (8)$$

The small-signal current Δi_1 drops across the effective impedance $(r_{ds,MP8}||r_{ds,MN7})$ producing voltage Δv_{GN} which is translated to Δi_2 given by

$$\Delta i_2 = g_{m_{MN10}} * \Delta v_{GN} \cong g_{m_{MN10}} * \Delta i_1 * (r_{ds,MP8}||r_{ds,MN7}). \quad (9)$$

Using (8) and (9) and substituting $\Delta i_1 = g_{m_{MP8}} * \Delta v_x$, we get

$$r_{0,PD} \cong \frac{1}{g_{m_{MP8}} * g_{m_{MN10}} * (r_{ds,MP8}||r_{ds,MN7})} \quad (10)$$

reducing the effective output impedance by a factor of loop gain given by $A_{PD} = g_{m_{MN10}} * (r_{ds,MP8}||r_{ds,MN7})$. At steady state, gate voltage of MN10 is held at a threshold voltage lower than V_{BCG} and it conducts approximately 20 nA of drain-source current as shown in Fig. 5.

The PU loop consists of three different poles

$$\begin{aligned} \text{MN9 drain pole: } P_{PU1} &\cong \frac{1}{(r_{ds,MP7}||r_{ds,MN9}) * C_1} \\ \text{MNP gate pole: } P_{GATE} \text{ or } P_{PU2} &\cong \frac{1}{(r_{0,PU}) * C_{G,MNP}} \\ \text{MP8 drain pole: } P_{PU3} &\cong \frac{1}{(r_{ds,MP8}||r_{ds,MN7}||1/g_{m_{MN9}}) * C_{par}} \end{aligned}$$

Since $r_{0,PU}$ is reduced by using the cascoded flipped-voltage follower approach, P_{PU2} is pushed to a higher frequency even at light bias-current conditions. The effective impedance looking-in at the drain of MP8 is reduced due to the low impedance of MN9 ($1/g_{m_{MN9}}$). This accompanied with the low equivalent parasitic capacitance (C_{par}) at this node, ensure that P_{PU3} is at a much higher frequency. Therefore, the entire PU loop is stabilized using C_1 ($=1$ pF), which is connected to the gate of MP9 making P_{PU1} the dominant pole. P_{PU2} and

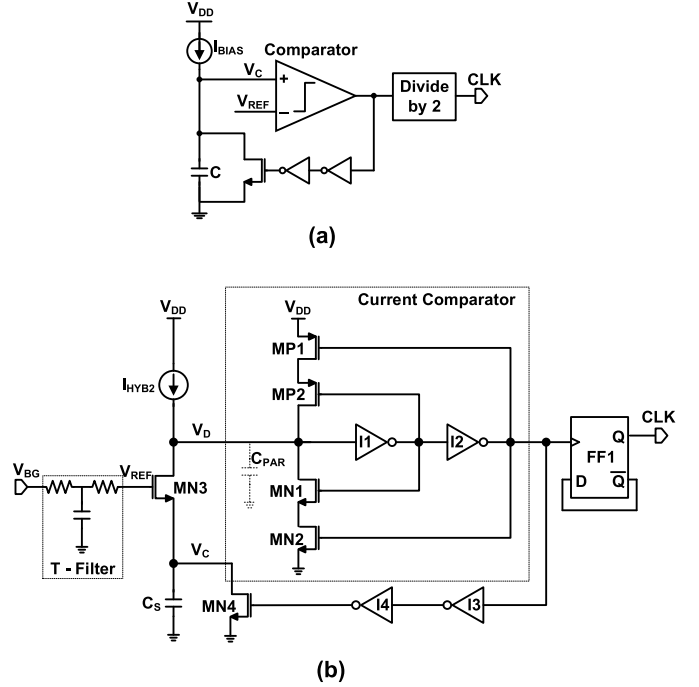


Fig. 7. (a) Block diagram of typical relaxation oscillator. (b) Proposed LPRO with current comparator and NMOS switch.

P_{PU3} remain beyond the PU loop unity-gain bandwidth (UGB) even at light bias-current condition providing a minimum phase margin of 45° across all load conditions. C_2 ($=1$ pF) acts as a glitch filter capacitor to keep the gate voltage of MN9 constant during large signal variations at its drain and source nodes. The PD loop gain is weak compared to PU loop in normal operation and is dominant only during I_{LOAD} step-down. It is naturally stabilized with the gate capacitance of MNP. As the variable biasing current I_{HYB1} increases with I_{LOAD} , the output impedance of the buffer is reduced further and pushes P_{GATE} to higher frequency.

The entire two-stage error amplifier is powered by a cross-coupled voltage doubler charge-pump in order to maintain a low dropout voltage for the LDO. However, variable I_{HYB1} which biases the error amplifier, modulates the current drawn from the charge pump with I_{LOAD} and ultimately, changing its $2 \times$ output voltage. In order to maintain a constant output voltage of $\approx 2V_{IN}$, the charge pump clock frequency (F_{CLK}) is modulated to counteract its load current variations. A current tunable LPRO is proposed to generate the charge pump control clocks.

IV. LOW-POWER RELAXATION OSCILLATOR (LPRO)

A typical relaxation oscillator architecture is shown in Fig. 7(a). A bias current (I_{BIAS}) charges the capacitor (C) until its voltage (V_C) exceeds a reference voltage (V_{REF}) at which the comparator momentarily changes its output state to logic high to discharge the capacitor. As soon as the capacitor is discharged, the comparator outputs a logic low and the same sequence repeats periodically to produce an output clock. The approximate output clock frequency (F_{CLK}) of this oscillator

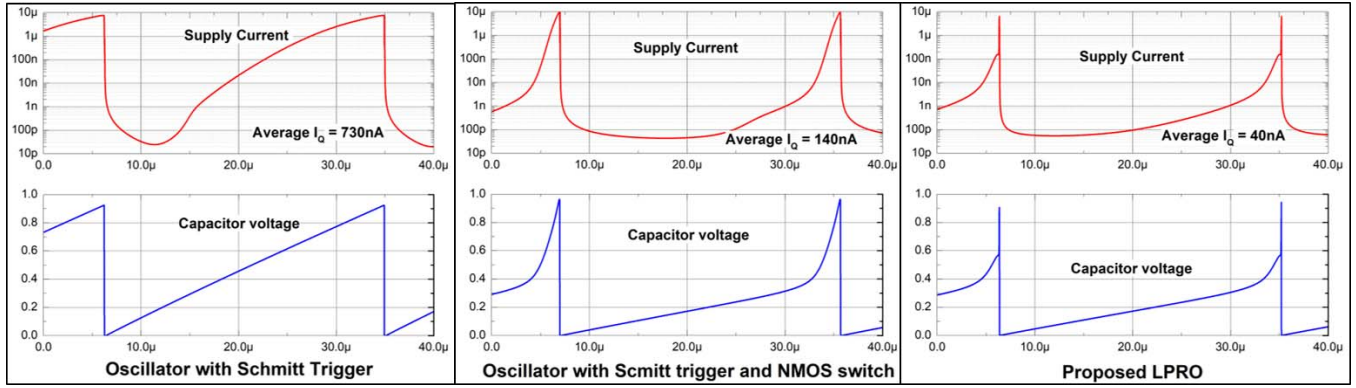


Fig. 8. Comparison of the transient profile of supply current and capacitor voltage for the proposed LPRO with other architectures.

is given by

$$F_{\text{CLK}} \cong \frac{I_{\text{BIAS}}}{2C * V_{\text{REF}}} \quad (11)$$

revealing that it is directly proportional to bias current. Although a preferred option for low-power clock generation, the major limitation for nanopower operation of this circuit comes from the power consumption in comparator. This comparator typically consists of just a Schmitt trigger or an OTA followed by a Schmitt trigger. The long charging time of the capacitor due to small I_{BIAS} results in higher switching losses and the OTA if used, consumes steady dc power. Denier [17] presents the use of current comparator instead of OTA. The oscillator uses equal bias currents for generation of reference voltage and for capacitor charging and claims lower power consumption due to reduced number of current-conducting branches. In this paper, a nanopower relaxation oscillator that does not use an OTA or an additional reference generator is proposed for charge-pump clock generation. Instead it uses the available external reference voltage and a fully digital current comparator for ultralow-power operation. The response time of this current comparator is proportional to the input current [18] which directly benefits the frequency scalability of the oscillator with its bias current.

Fig. 7(b) shows the overall schematic of the proposed LPRO circuit. The second output from HBCG circuit (I_{HYB2}) acts as the charging current. An NMOS switch MN3 is placed in between current source I_{HYB2} and the capacitor (C_S) with its gate controlled by V_{REF} . A T-filter is placed in between the external reference voltage (V_{BG}) and V_{REF} to avoid switching noise coupling onto V_{BG} . Initially, the capacitor voltage V_C and therefore the drain voltage of MN3 (V_D) are at zero after the previous discharge cycle. At this state, output of inverter I1 in the current comparator is at logic high while the output of I2 is at logic low due to which transistor MP1 and MN1 are on and MP2 and MN2 are off. As I_{HYB2} charges C_S , V_C increases linearly. This pushes MN3 into subthreshold region where its drain-source current is given by

$$I_{\text{DS,MN3}} \propto e^{\left(\frac{V_{\text{GS}}}{\eta V_t}\right)} \left(1 - e^{-\left(\frac{V_{\text{DS}}}{V_t}\right)}\right) \quad (12)$$

where $V_t = (kT/q) \approx 26 \text{ mV}$ at $T = 27^\circ\text{C}$ and η is a process constant. As V_C increases

further, both V_{GS} and V_{DS} of MN3 reduces ensuring $e^{(V_{\text{GS}}/\eta V_t)} \rightarrow 0$ and $(1 - e^{-(V_{\text{DS}}/V_t)}) \rightarrow 0$, thereby exponentially reducing $I_{\text{DS,MN3}}$. The difference current ($I_{\text{HYB2}} - I_{\text{DS,MN3}}$) increases exponentially and charges the small parasitic input capacitance C_{PAR} . Therefore, V_D increases exponentially from zero and output of I1 changes to logic low turning on MP2. However, I2 is designed to be weak so that its output transition to logic high happens after a small delay. During this momentary period, both MP1 and MP2 are on and quickly charge C_{PAR} such that V_D shoots up instantaneously and speed-up the switching activity even for very low values of I_{HYB2} . I3 and I4 buffer the output of I2 to discharge C_S through switch MN4. As V_C drops, MN3 turns on. MN3 and MN4 along with the regenerative feedback of MN1 and MN2 discharges C_{PAR} and V_D is pulled down to zero. This cycle repeats to produce a periodic clock whose output duty cycle error is corrected by using a clock divider FF1 to obtain the output clock. Instead of current mode, the entire comparator can be analyzed in voltage mode similar to a Schmitt trigger circuit and can be considered a voltage mode comparator with threshold voltage determined by the device sizing. The effective clock frequency of the output clock is given by

$$F_{\text{CLK}} \cong \frac{I_{\text{HYB2}}}{2C_S * (V_{\text{BG}} - V_{\text{THN}})}. \quad (13)$$

Since I_{HYB2} changes with I_{LOAD} , the clock frequency also changes proportionally to generate a load current dependent frequency as required by the dynamic frequency charge pump.

Fig. 8 shows a comparison between the simulated transient capacitor voltage and supply current profiles for different types of oscillator. Even in case of an oscillator with Schmitt trigger, the effective area under the supply current curve is reduced when a switch is introduced in between the capacitor and bias current. This is reduced further by introduction of the fast switching current comparator as in the case of LPRO. The average I_Q of the proposed LPRO is only 40 nA for an output frequency of 22 kHz which translates to an oscillator figure of merit (FOM) of only 2.7 nW/kHz for a supply voltage case of 1.5 V. Monte Carlo simulation results with $N = 100$ samples for the output frequency and average I_Q of the LPRO are captured in Fig. 9 at $I_{\text{LOAD}} = 0$. A 3σ variation of $\pm 10 \text{ nA}$

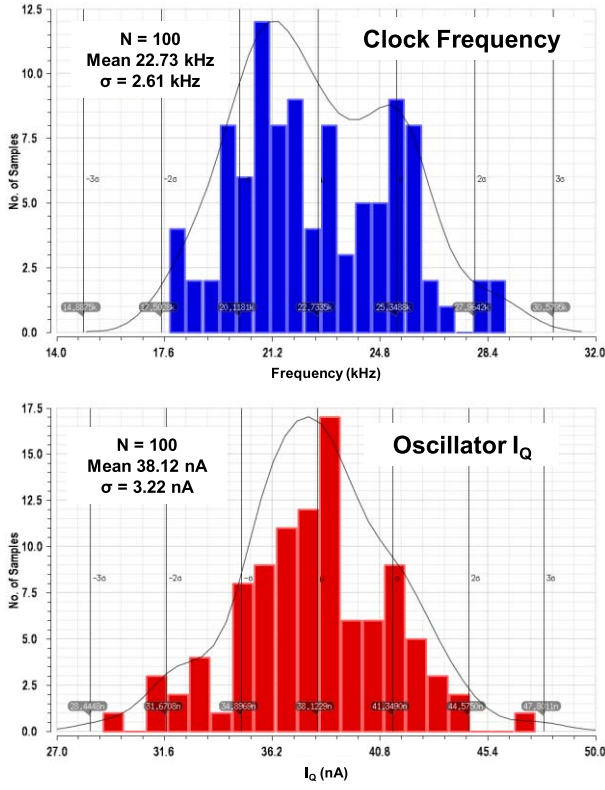


Fig. 9. Histogram of clock frequency and average I_Q of the proposed LPRO for Monte Carlo simulation ($N = 100$).

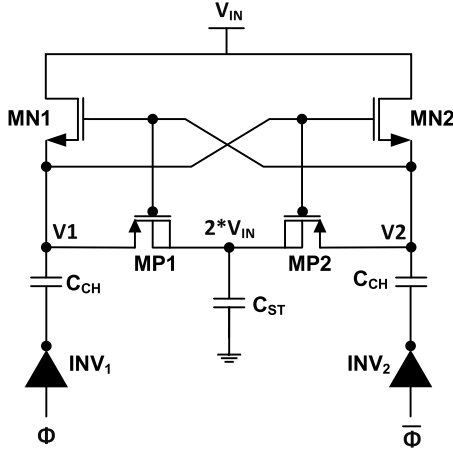


Fig. 10. Clock frequency modulated charge-pump voltage doubler.

is a negligible variation when compared to the overall I_Q of the LDO.

Fig. 10 shows the employed cross-coupled voltage doubler charge-pump [19]. It uses non-overlapping clock phases and two inverters (INV₁ and INV₂) to drive two charging capacitors (C_{CH}). Due to the combined effect of NMOS switches MN₁ and MN₂ along with the inverters, the node voltages V₁ and V₂ swing between V_{IN} and 2 × V_{IN}. This charge is then transferred onto storage capacitance C_{ST} in every clock phase and maintains the output voltage of the charge-pump close to 2 × V_{IN}. In order to ensure that output voltage ripple

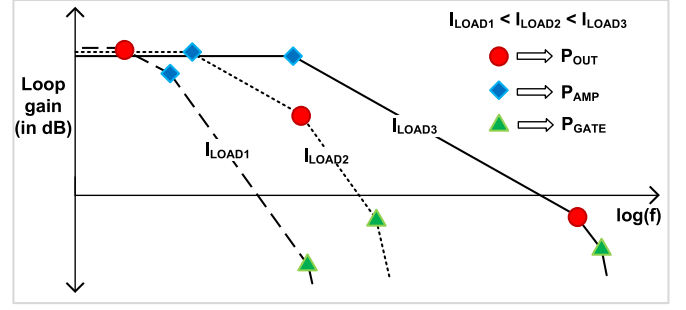


Fig. 11. LDO pole locations and their movement with increasing load current.

is kept low for the entire 3 σ frequency variation range of around ± 8 kHz as shown in Fig. 9, both C_{CH} and C_{ST} are sized slightly higher to be 8 pF each.

V. STABILITY ANALYSIS AND COMPENSATION

The stability of this LDO is determined by the location of three distinctive poles: the LDO output pole P_{OUT} , amplifier output pole P_{AMP} , and the pass device gate pole P_{GATE} . Since the NMOS pass device acts like a source follower, the output impedance of the LDO is given by

$$R_{OUT} \cong \frac{1}{g_{m,MNP}} || R_{LOAD} \quad (14)$$

where R_{LOAD} is the load current equivalent resistance connected at the output of the LDO. Thus, P_{OUT} is given by

$$P_{OUT} \cong \frac{1}{2\pi \left(\frac{1}{g_{m,MNP}} || R_{LOAD} \right) C_{LOAD}} \quad (15)$$

P_{AMP} is given in (3) and P_{GATE} is obtained by using (7) and parasitic pass device gate capacitance C_{GATE} as

$$P_{GATE} \cong \frac{1}{2\pi (g_{m,MP8} * g_{m,MP9})(r_{ds,MP7} || r_{ds,MN9})C_{GATE}} \quad (16)$$

P_{OUT} changes with I_{LOAD} and due to adaptive biasing, P_{AMP} , P_{GATE} , and the loop UGB also change with I_{LOAD} . Fig. 11 shows the typical movement of these poles with I_{LOAD} . The proposed buffer design makes sure that P_{GATE} is always beyond the loop UGB and hence does not influence the overall loop stability. At zero to light load currents (I_{LOAD1}), P_{OUT} is at a very low frequency (~ 1 Hz) and is very close to P_{AMP} (~ 10 Hz). As I_{LOAD} increases to about 1 mA (I_{LOAD2}), P_{OUT} drastically shifts to higher frequency, however, due to very minor increment in bias current, P_{AMP} moves slightly. Hereafter, as the I_{LOAD} increases, P_{OUT} shifts to higher frequency eventually moving outside the UGB for close to maximum I_{LOAD} conditions (I_{LOAD3}). P_{AMP} also shifts to higher frequency due to proportional increase in bias current thereby increasing the loop UGB. Closely spaced low-frequency poles at light I_{LOAD} and constantly frequency shifting poles with increase in I_{LOAD} result in challenging considerations for the compensation scheme. Current buffer compensation as presented in [4] is very effective in pole splitting but in this case, since the two poles of interest are at very low frequency, the required Miller capacitance for

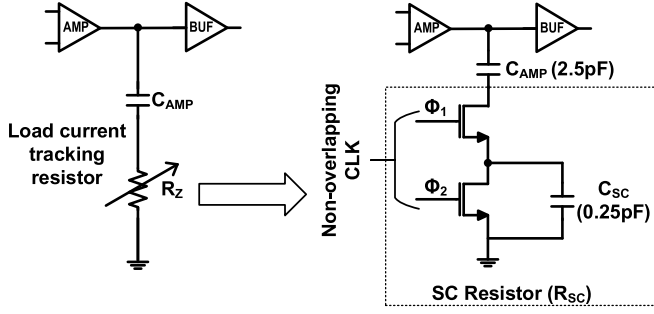


Fig. 12. Proposed SCPT compensation scheme.

pole splitting results in huge area penalty for integration. Tan *et al.* [20] present a weighted current feedback technique along with Miller compensation but is suitable for load capacitance up to 10 nF. Pole tracking compensation is presented in [21] and [22] where the movement of P_{OUT} is tracked and used for compensation. However, the load current of [21] is limited to 100 μ A on the lower side instead of zero and the zero implemented using MOS resistor in [22] can vary significantly due to process variations.

In this paper, a P_{OUT} tracking zero is introduced to provide a phase boost and ensure stability. A zero can be introduced in the loop by using a resistor R_Z as shown in Fig. 12. However, with $C_{AMP} = 2.5$ pF, in order to introduce a zero at around UGB for no-load, the required resistance can be as high as 100 M Ω which results in large area penalty. Moreover, R_Z needs to track P_{OUT} and hence needs to be variable resistor. This is achieved using a novel SCPT compensation scheme where a switched-capacitor resistor (R_{SC}) is placed instead of R_Z to introduce a zero (Z_{SC}). The same oscillator clock is used to control R_{SC} with its effective value given by

$$R_{SC} = \frac{1}{F_{CLK} * C_{SC}} \quad (17)$$

where C_{SC} is the capacitance used to implement R_{SC} and the SCPT zero Z_{SC} is given by

$$Z_{SC} = \frac{F_{CLK} * C_{SC}}{2\pi C_{AMP}}. \quad (18)$$

However, from (13), we know that $F_{CLK} \propto I_{HYB1}$ and due to adaptive biasing we have $I_{HYB1} \propto I_{LOAD}$. Therefore, from (18), we have

$$Z_{SC} \propto I_{LOAD}. \quad (19)$$

Thus, Z_{SC} tracks P_{OUT} which is proportional to I_{LOAD} and provides a phase boost for the entire range of load currents. A small capacitance $C_{SC} = 0.25$ pF is used to implement R_{SC} , providing an area-efficient solution. Non-overlapping clocks control the switches used in this switched-capacitor resistor. Fig. 13 shows the simulated gain and phase response of the LDO loop obtained using periodic steady state (PSS) followed by periodic ac (PAC) simulation for different load current values for a load capacitance of 1 μ F. The impact of hybrid biasing can be seen as the UGB shifts with load current. The phase margin is always above 30° and demonstrates the effectiveness of the SCPT compensation. The 3 σ variation of

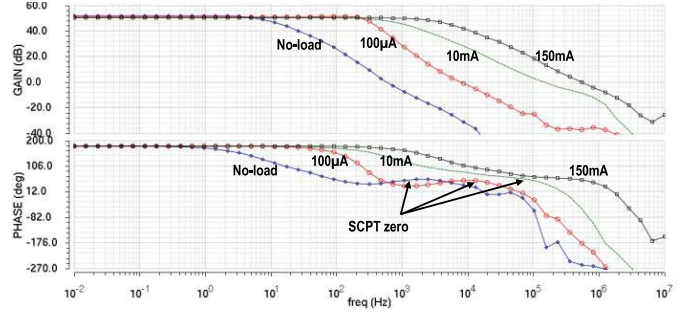


Fig. 13. LDO loop gain and phase response with the pole tracking SCPT zero highlighted.

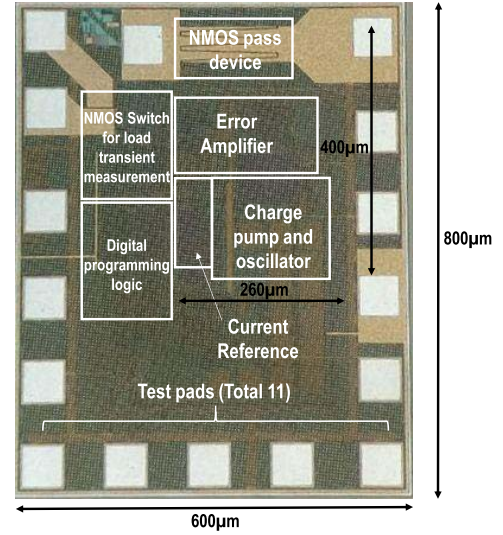


Fig. 14. Die micrograph.

± 8 kHz in oscillator frequency might cause a minor change in the actual value of the phase margin but does not affect the stability. This scheme ensures that the LDO is stable even for increments in load capacitance up to 47 μ F. The zero introduced by SCPT compensation also increases the UGB of the loop thereby improving its transient response. It is to be noted that in this compensation scheme, the clock frequency is always at least 50 times the loop UGB ($F_{CLK} \geq 50 * UGB$) for all load current conditions. Therefore, any pole (P_{par}) formed due to R_{SC} and net parasitic capacitance (C_{par}) attached to it, given by

$$P_{par} = \frac{1}{R_z * C_{par}} = \frac{F_{CLK} * C_{SC}}{C_{par}} \quad (20)$$

will always be much beyond the loop UGB and does not affect the stability of the LDO.

VI. SIMULATION AND MEASUREMENT RESULTS

This LDO is fabricated in a 0.25 μ m single-poly four-metal CMOS process. Fig. 14 shows the die micrograph. The core area is 400 μ m \times 260 μ m excluding the test pads and the additional circuitry used for programming and testing. This LDO uses an external voltage reference. Although bandgap reference is not integrated within the LDO, sample-and-hold

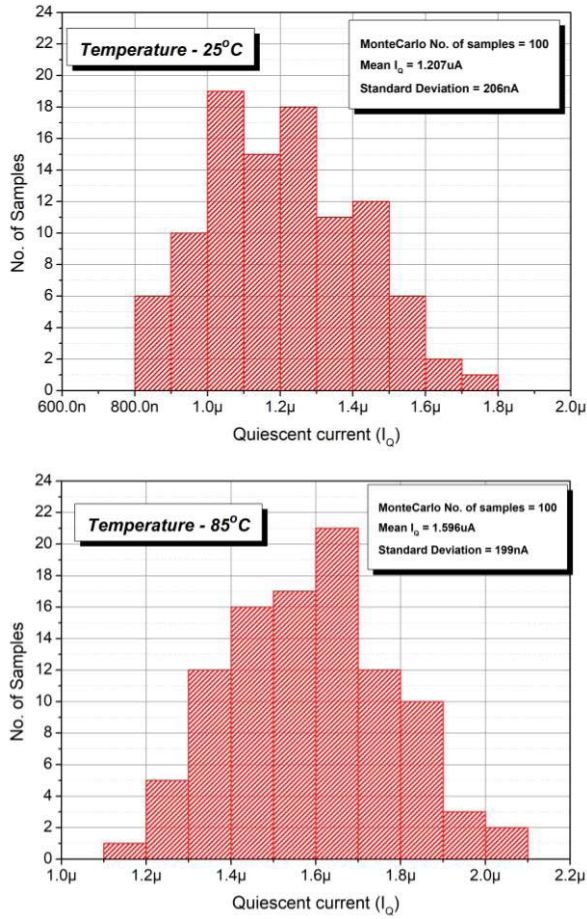


Fig. 15. Simulated no-load I_Q using Monte Carlo 100 samples at 25 °C and 85 °C.

approaches presented in [23] can be used to reduce its current consumption to few nano-Amperes and therefore its contribution to the overall I_Q of the LDO can be made negligible. The LDO has a digitally programmable output voltage range of 1–3 V and a maximum output current capability of 150 mA at a dropout voltage of 240 mV. The load capacitance range is from 1 to 47 μ F. A single bond wire is used to bond the output of the LDO to the package pin and impacts the dc load regulation which is 25 mV as I_{LOAD} increases from 0 to 150 mA.

Table I shows the simulated block level no-load I_Q consumption breakdown of the LDO. The major contribution to the overall I_Q is from the error amplifier and associated charge-pump in order to ensure good transient response. The programmable resistor divider which is critical for output voltage programmability consumes 100 nA while the internal constant-gm current reference branches takes 40 nA. Fig. 15 shows Monte Carlo simulation results for the overall I_Q of the LDO for 25 °C and 85 °C with process variation and device mismatch. Fig. 16 captures the I_Q of the LDO and its current efficiency versus I_{LOAD} . The no-load I_Q of the proposed LDO is only 1.24 μ A. It stays below 2 μ A for $I_{LOAD} < 200 \mu$ A and is only about 5 μ A even when I_{LOAD} goes up to 1 mA thereby consuming very low supply current even at light load conditions. The

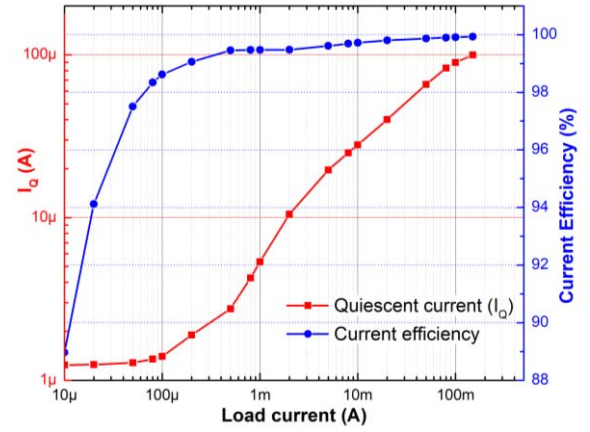


Fig. 16. Quiescent current and current efficiency of the LDO versus load current.

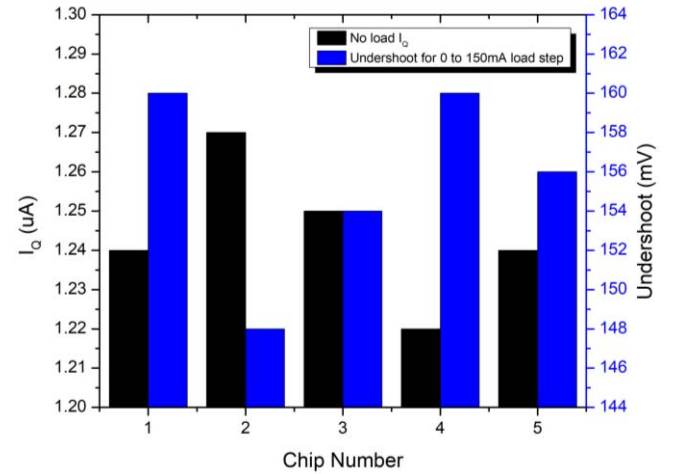


Fig. 17. Measured no-load I_Q for five different chips along with the undershoot voltage for a load transient of 0–150 mA.

TABLE I
SIMULATED BLOCK LEVEL NO-LOAD I_Q BREAKDOWN

Block	I_Q (nA)
Error amplifier with buffer	400
Hybrid bias-current generator (HBCG)	100
Low power relaxation oscillator (LPRO)	40
Reference scaling amplifier	40
Programmable resistor divider	100
Charge-pump	480
Constant-gm current reference	40
Total	1200

current efficiency is above 95% even for I_{LOAD} as low as 50 μ A and is above 99% for 200 μ A and above. The measured I_Q of 1.24 μ A shows that the design is centered across the the mean value as shown in the Monte Carlo simulation

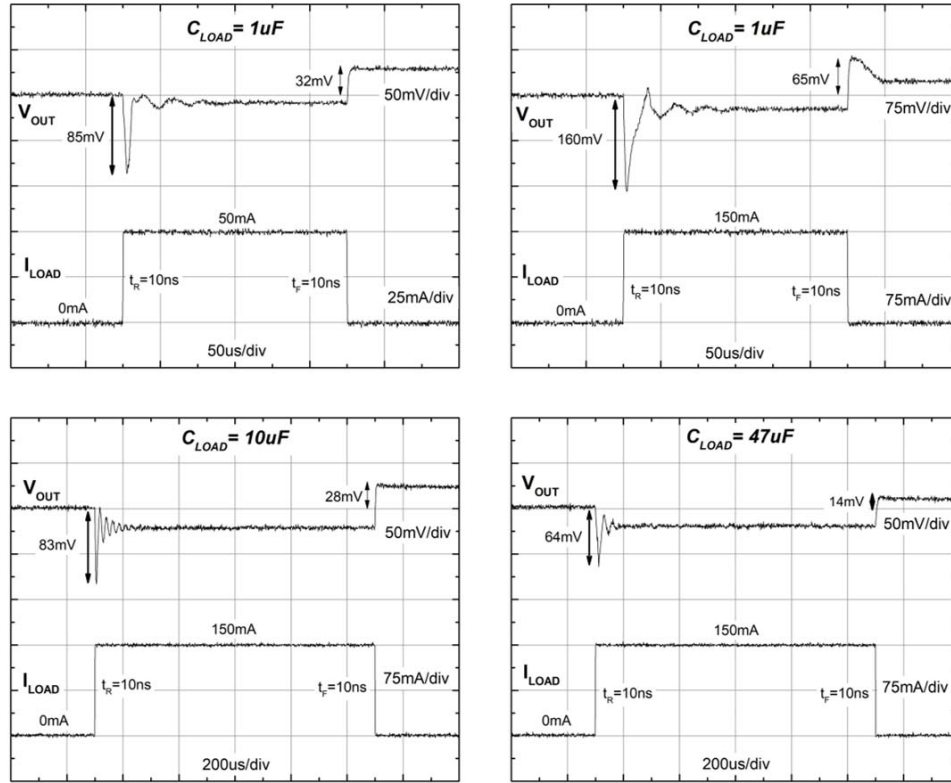


Fig. 18. Measured load transient response of the proposed LDO for different load steps and output capacitor values.

results in Fig. 15 and achieves a high current efficiency. Fig. 17 shows the measured I_Q of five different test chips along with their output undershoot voltage for a 0 to 150 mA load current step. The results show consistency in the both I_Q and undershoot voltage with less than 3% variation. The measured load transient response for different load steps and output capacitor combinations is shown in Fig. 18. For $C_{LOAD} = 1 \mu F$, the undershoot and overshoot voltage for load step of 0–50 mA and vice-versa are 76 and 32 mV, respectively, and are 135 and 65 mV, respectively, for a load step of 0–150 mA. The output recovers to tolerable error limit of $\pm 1\%$ within $10 \mu s$. Reduction in both undershoot and overshoot voltages is observed when $C_{LOAD} = 10 \mu F$ and $C_{LOAD} = 47 \mu F$ which also confirms the stability of the LDO at these load capacitance levels. Besides using an NMOS pass device, low overshoot/undershoot, and fast recovery performance of this low I_Q LDO is only possible due to the hybrid biasing working alongside the on-demand PU/PD buffer and SCPT compensation. Although choice of NMOS pass device results in additional requirement of charge-pump and associated oscillator for ensuring LDO voltage, improved transient response, and effective usage of the oscillator for SCPT compensation scheme overpowers this limitation. The impact of output capacitor PD circuit can be seen in the case of 0–150 mA transition with $C_{LOAD} = 1 \mu F$ as the high output overshoot of 65 mV is quickly discharged and brought down to a tolerable error voltage. In all other cases when the output voltage overshoot is less than 35 mV, the pull-down circuit does not kick-in for capacitor discharge. However,

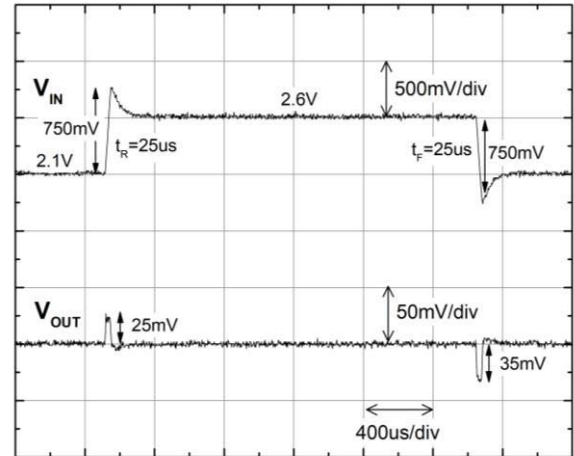


Fig. 19. Measured line transient response of the LDO at full-load current.

the worst case voltage error is less than 3% in such cases and is negligible.

Fig. 19 shows the line transient response of the LDO at maximum load condition ($I_{LOAD} = 150$ mA) for output voltage of 1.8 V. The initial step-up and step-down in the supply voltage is 0.75 V and results in an undershoot of 35 mV and overshoot of 25 mV. This constitutes less than 2% error for an output voltage of 1.8 V. The power supply rejection (PSR) of the LDO is shown in Fig. 20 at $I_{LOAD} = 150$ mA. The UGB improvement achieved due to hybrid biasing enables higher than 20 dB rejection for frequencies up to 20 kHz.

TABLE II
PERFORMANCE COMPARISON OF THE PROPOSED LDO WITH PREVIOUSLY PUBLISHED OUTPUT CAPACITOR STABILIZED LDOs

Parameter	[4] 2007	[24] 2008	[25] 2009	[9] 2010	[26] 2010	[27] 2016	[16] 2017	This work
Technology (μm)	0.35	0.35	0.35	0.35	0.09	0.18	0.18	0.25
Area (mm^2)	0.264	0.409	0.188	0.225	0.00274	0.0245	0.028	0.108
Input voltage V_{IN} (V)	2.0	2.0	2.1 – 5.0	2.0	1.0	1.2 – 1.8	1.4	1.5 – 3.3
Output voltage V_{OUT} (V)	1.8	1.8	2.0	1.8	0.9	1.0	1.2	1.0 – 3.0
Max. load current (mA)	200	150	100	100	50	100	50	150
Dropout voltage (mV)	200	200	60	200	100	200	200	240
C_{LOAD} (μF)	1.0	1.0	4.7 – 10	1.0 – 10	1.0	1.0	1.0	1.0 – 47
ESR zero requirement	No	No	0.3 Ω – 0.5 Ω	0.1 Ω – 0.4 Ω	0.35 Ω	0.35 Ω	No	No
I_Q (μA)	20 – 340	27	40	4	9.3	135.1	1.6 – 200	1.24 – 100
Current efficiency @ max. load	99.5	N.A.	N.A.	99.996	N.A.	99.86	99.6	99.93
PSR (dB)	>45dB (0 – 20kHz)	>40dB (0 – 20kHz)	N.A.	N.A.	>54dB (0 – 100kHz)	>35dB (0 – 100kHz)	>30dB @10MHz	>22dB (0 – 20kHz)
Undershoot (mV)	54	65 [#]	40 [#]	55	6	25	24	135
Overshoot (mV)	15	70 [#]	54 [#]	25	8	~0	5	65
T_R (μs)	0.27	0.43 [*]	12	0.55 [*]	0.16 [*]	0.25 [*]	0.48	0.9
FOM (ps)	27	78 [*]	4800	22 [*]	74.4 [*]	338 [*]	18.5	7.4

^{*} Calculated from the results shown by the paper

[#] Measured for load transient from non-zero minimum value to maximum load current

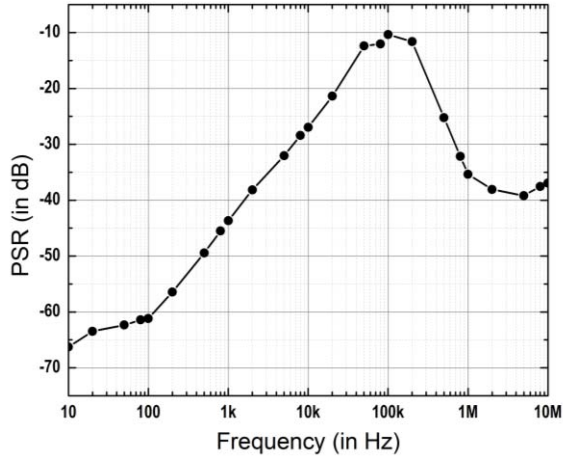


Fig. 20. Measured PSR of the LDO at full-load current.

Table II provides a comprehensive comparison of the proposed LDO with previously published work highlighting its major advantages. In comparison, this LDO has the lowest I_Q which is critical for low power consumption during standby and light load conditions. The SCPT compensation not only ensures stability of the LDO from zero to entire range of load current, but also for a capacitance range of 1–47 μF without depending on an external ESR zero thereby providing the widest output capacitor range. The FOM defined as $\text{FOM} = T_R * (I_Q / I_{\text{LOAD,MAX}})$ is incorporated from [4] for a proper baseline comparison where T_R is the recovery time given by $T_R = (C_{\text{LOAD}} * \Delta V / I_{\text{LOAD,MAX}})$, where ΔV is the undershoot voltage. A lower FOM suggests an overall better performing LDO. The proposed LDO achieves at least 66% reduction in FOM when compared to LDOs with maximum load current capability of 100 mA or above. Although [16] has

a comparable no-load I_Q , its maximum load current is limited to 50 mA and it has a 2.5 times higher FOM.

VII. CONCLUSION

This paper presents an NMOS LDO with a very low I_Q of 1.24 μA . Hybrid bias-current scaling scheme is presented to improve the bandwidth and slew rate of the LDO for fast response to load current transients. A charge-pump powered, bias-current scalable two-stage error amplifier is implemented for LDO regulation. The proposed on-demand PU/PD buffer ensures high slew rate at the gate of the pass device. An LPRO with load current controlled clock frequency is proposed to generate the control clocks for the charge pump. This oscillator consumes only 40 nA of I_Q at light load currents. A novel SCPT compensation scheme is employed for LDO stability. This technique uses the already available variable clock frequency to achieve stability for a load capacitance range of 1–47 μF without the requirement of an ESR zero. Measurement results show that the LDO has a recovery time of less than 10 μs for zero to full-load current step-up and achieves higher than 95% current efficiency even for small load current of 50 μA . The competitive transient FOM makes this LDO highly favorable for supply regulation of battery powered, long standby time, and short wake-up time applications.

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