A Regulation-Free Sub-0.5-V 16-/24-MHz Crystal Oscillator With 14.2-nJ Startup Energy and 31.8-μW Steady-State Power

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***Abstract*— This paper reports a regulation-free sub-0.5-V crystal oscillator (XO). The XO specifically designed for Bluetooth low-energy (BLE) radios aims for direct-powering by the harvested energy. To secure its performance against process, voltage, and temperature (PVT) variations, while reducing its startup time and energy, we propose a dual-mode g_m scheme and a scalable self-reference chirp injection (SSCI) technique. The former employs an inductive multistage g_m to mitigate the crystal's stray capacitance during the startup, but a single-stage g_m in the steady state to preserve the phase noise (PN). For the latter (SSCI), we generate a scalable chirping sequence to kick-start the XO, avoiding trimming of the auxiliary oscillator. The XO fabricated in 65-nm CMOS is measured with two common crystals (16/24 MHz) over a 0.3-to-0.5-V supply. At 24 MHz and 0.35 V, the startup time and energy of the XO are 400 μs and 14.2 nJ, respectively, while showing a steady-state power of 31.8 μW and a PN of −134 dBc/Hz at 1-kHz offset. The frequency stability is 14.1 ppm against temperature (−40 °C–90 °C) and 17.9 ppm against voltage (0.3–0.5 V), both conform to the BLE standard (±50 ppm) with adequate margin.**

***Index Terms*— Bluetooth low-energy (BLE), chirping, CMOS, crystal oscillator (XO), duty-cycling, energy harvesting (EH), fast startup, Internet-of-Things (IoT), ultralow power (ULP), ultralow voltage (ULV).**

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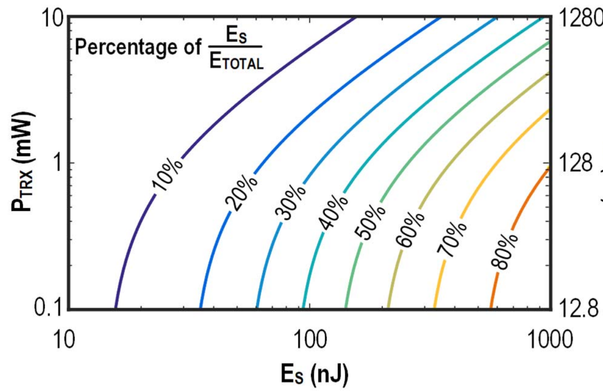

Fig. 1. Percentage of energy consumed during the startup of the XO over the total energy $E_{\text{TOTAL}} = P_{\text{TRX}} \times T_{\text{ON}} + P_{\text{SLEEP}} \times T_{\text{OFF}} + E_S$. P_{SLEEP} (assumed 1 μW here, as approximated from [7]) is the sleep power, T_{ON} (128 μs) and T_{OFF} (128 ms) are the assumed active time and sleep time of the TRX, respectively.

I. Introduction

Ultralow-power (ULP) wireless radios are the cornerstone of a wide variety of Internet-of-Things (IoT) applications. In particular, for the environmental monitoring, the ULP radios should operate under intermittent operation [1] to further reduce the data handling while prolonging the battery lifetime. Each ULP radio requires a stable reference for frequency synthesis at RF. The crystal oscillator (XO) is a reliable solution, but without the startup aid, it can take a few milliseconds for the XO to settle into the steady state [2]–[5] due to the high quality factor of the crystal ($\sim 10^5$). Its startup time (t_s) dominates the "ON" latency of the radio, and its startup energy (E_S) can significantly degrade the effectiveness of duty cycling. As depicted in Fig. 1, if the active energy (E_{TRX}) of a transceiver (TRX) is 1280 nJ (ON-time of 128 μs [6] and active power of 10 mW [7]), the percentage of energy spent for starting the XO in every working cycle is ∼42% for E_S of 1000 nJ for conventional XO and a duty cycle of 0.1%. Such a percentage is going up since recent TRXs have managed to lower their active power (P_{TRX}) by proper circuit techniques [8]–[10]. In this regard, it is essential to reduce E_S for the ULP radios to save energy by duty cycling. Recent efforts in both academia

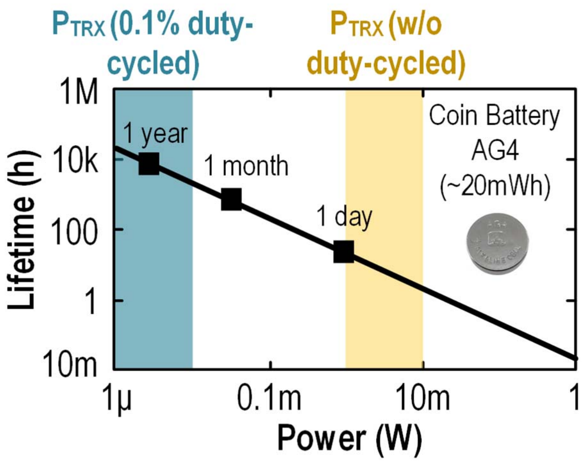

Fig. 2. Estimated lifetime of a commercial coin battery AG4 versus P_{TRX}, which can be expressed as: battery capacity/($P_{\mathrm{TRX}} \times$ active duty cycle).

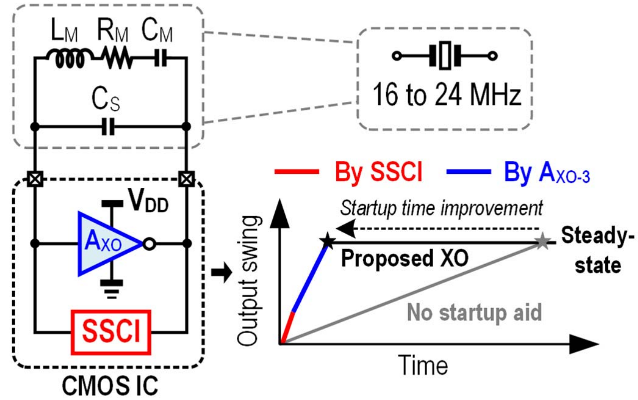

Fig. 3. Overview of the proposed XO and illustration of t_S improvement by two techniques: SSCI and inductive three-stage g_m. L_M, C_M, and R_M are the modeled inductance, capacitance, and resistance of the crystal, respectively, whereas C_S is the crystal's stray capacitance.

and industry succeeded in shortening t_s and E_S of the XO [6], [7], [11]–[16].

On the other hand, long-term sustainability of wireless sensor nodes is another critical perspective of IoT deployment. For battery-powered ULP radios, the effort of battery replacement is largely labor-intensive. Even with a 0.1% active cycle, and a P_{TRX} of 2.3 mW, the lifetime of a ULP radio can hardly exceed a year under a coin-size battery (Fig. 2). For the prospect of one trillion IoT devices in the years to come, it implies 2.7 billion of batteries replacement daily, being a tremendous effort and unsustainable to the environment. To this end, energy harvesting (EH) offers the outlook for perpetual operation [17]–[19] of the ULP radios, while eliminating the cost and volume limit of the battery. Thermoelectric (10–1000 μW/cm^2) and photovoltaic (indoor: 10–100 μW/cm^2) are promising ambient sources, but their sub-0.5-V outputs [17] are too low for typical circuit solutions, and can vary (although slowly) with the environmental factors (e.g., temperature or light intensity). These facts motivate a new paradigm of analog and RF circuits that can survive against an inconstant sub-0.5-V supply voltage (V_{DD}), eliminating the cost and loss of interim dc–dc converters and regulators.

This paper reports a regulation-free sub-0.5-V XO according to the system aspect of the EH Bluetooth low-energy (BLE) radios described in [20]–[23]. Unlike the existing fast-startup XOs that are based on standard or I/O voltages to power-up their inverter-like or active-load amplifiers [6], [11]–[14], our proposed XO is ultralow-voltage (ULV)-enabled by using single-/multistage resistive-load amplifiers. This circumvents from the ineluctable voltage headroom limit, rendering it compatible with the ULV application. Specifically, we propose a dual-mode g_m scheme and a scalable self-reference chirp injection (SSCI) technique for the XO to surmount the operating challenges in both startup and steady state (Fig. 3). The reported XO includes load capacitors of 6 pF and suits common commercially available crystals. Yet the technique can also be applied to crystals with different load capacitances. This paper is expanded from [24], with additional details and measurement results.

After the introduction, Section II details the proposed dual-mode g_m scheme and SSCI. Section III presents the transistor-level design of the sub-0.5-V XO. Section IV summarizes the experimental results, and finally, Section V draws conclusions.

II. Fast-Startup XO Using Dual-Mode G_m Scheme and SSCI

For a crystal's resonant frequency (f_m) at tens of megahertz, its t_s (milliseconds) dominates the "ON" latency of a duty-cycled radio, raising the average power consumption. As well, for energy-limited EH sources, the startup energy (E_S) of the XO is crucial as it may demand a large instant current from the EH source or reservoir. Recent XOs [6], [11]–[15] have succeeded in reducing both t_s and E_S. Herein, we propose two techniques: dual-mode g_m and SSCI, for balancing the XO performances in both startup (i.e., t_s and E_S) and steady state [i.e., power consumption and phase noise (PN)]. The envelope of the XO during the startup at time t is

$$A_{\mathrm{env}}(t) = A_i \cdot e^{\frac{R_N - R_M}{2L_M}t} \tag{1}$$

where A_i is the initial amplitude and R_N is the negative resistance of the overall impedance viewed from the crystal core (details in Section II-B). L_M and R_M are the motional inductance and resistance of the crystal, respectively. The aim of SSCI is to increase A_i instantly after enabling the XO, while the dual-mode g_m allows a boosted R_N afterward. They together bring down t_S without momentarily raising the startup power, culminating in a lower E_S and a relaxed power-source design, with details presented in the following.

A. Scalable Self-Reference Chirp Injection

Signal injection to the XO can bring down t_s if the injection frequency is close to f_m of the crystal [12]. Instead of waiting for the XO to build up its oscillation amplitude, an auxiliary oscillator (AO) can be used to excite the crystal. Yet, due to the high-Q nature of the crystal, such signal injection is only

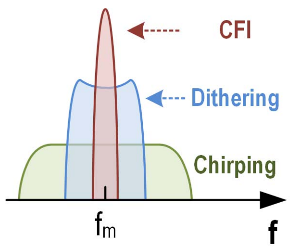

Fig. 4. General illustration of different signal-injection techniques in the frequency domain. Assuming the total power of each injection signal is similar, the crystal absorbs more power from CFI than CI since the CI spectrum spreads over a broader band.

TABLE I

OVERVIEW OF DIFFERENT SIGNAL-INJECTION TECHNIQUES TO KICK-START THE XO

	Characteristics of the injecting signal		
	Constant frequency	Dithering	**Chirping**
t_S & E_S reduction	✓✓✓	✓✓	✓
Trimming on AO	Required	Required	**Not required**
Precision of AO	Very critical	Critical	**Relaxed**
Literature	[14, 15]	[6]	[12] and this work

effective if its frequency does not deviate by >0.5% from f_m [6]. Several signal-injection techniques for kick-starting the XO have been reported. They can be categorized into three groups: constant frequency injection (CFI) [11], [14], [15], dithering injection [6], and chirp injection (CI) [12].

CFI injects a clock signal into the crystal with a constant frequency close to f_m, as illustrated in the frequency domain (Fig. 4). With a constant frequency and narrow bandwidth (e.g., full-width at half-maximum of the 7.7-μs pulse in [14]: 156 kHz), a clock frequency precisely matching f_m is essential to excite the crystal. This involves calibration as well as a delicate design for the AO which will be challenging in a sub-0.5-V design. As an example, the XO in [14] achieves t_s values of 58/10/2 μs from 1.84/10/50 MHz crystals. Yet it has a supply voltage of 1 V. Also, the ring oscillator entails frequency calibration after fabrication.

Dithering injection toggles the AO frequencies between two values by compensating the frequency deviation of the injection signal caused by temperature and voltage variations. As such, the injection signal can cover a wider frequency range than that of CFI. Still, trimming is necessary to compensate the process variation on the AO. Compared with CFI, its effect on shortening t_s is lower, since the signal power is spread to a wider spectrum. As a result, there is smaller power to be absorbed by the crystal at f_m. For instance, the XO in [6] exhibits a slashed t_S of <400 μs by using dithered-signal injection (dithered step size: 2%), but it still demands trimming to manage the process variations on the injection oscillator.

Here, we consider CI to be more robust and inexpensive, as it relies on a frequency-rich signal to excite the crystal and avoids frequency calibration. The principle is alike dithering but covers a wider frequency range. It gradually sweeps the oscillating frequency and progressively decreases/increases the frequency. As such, this chirping sequence can generate a spectrum between the highest frequency f_H and the lowest frequency f_L, as evinced by its Fourier transform [25]. If $f_L < f_m < f_H$ regardless of process, voltage, and temperature (PVT) variations, the power will be delivered to the crystal persistently. Despite its weaker effectiveness on t_S reduction since the power spreads to a wider band, CI has the benefit of no trimming on the AO. It is especially suitable for low-cost and ULV radios, where the frequency variation of the AO against voltage and temperature can be more exacerbated.

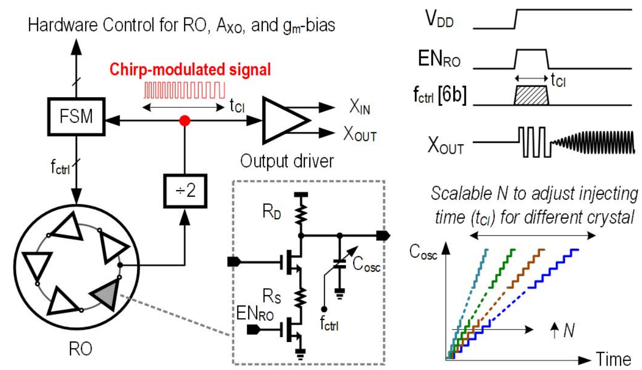

Fig. 5. Proposed SSCI. It generates a chirping signal to kick-start the XO using an untrimmed RO with relaxed precision. The FSM provides feasibility to scale t_{CI}, accommodating different crystal packages (i.e., L_M and C_S).

In [12], CI was applied together with the R_N-boosting technique, showing a t_S of 158 μs without trimming or calibration on the AO. Still, the related RC-sweeping unit for modulating the frequency of the AO is area hungry (estimated ~90% of the chip area) due to its large time constant (at the order of 10 μs) for generating the chirping sequence. Table I summarizes the key features of the three signal-injection techniques.

To avoid the pitfalls of [12], we introduce the SSCI (Fig. 5) that only entails an untrimmed oscillator with relaxed precision. Its frequency range can easily cover f_m variation against PVT. Unlike the RC-based chirping [12], here we incorporate a five-stage RO with a finite state machine (FSM) to control the oscillating frequency of the RO via a cap-bank. Hence, the chirping sequence can be generated by referencing its own signal and requiring no area-hungry RC-units to modulate the oscillating frequency. The FSM counts the number of pulses and sequentially raises C_{OSC} by sending the control signal f_{ctrl} to the RO. In addition, compared to the analog sweeping technique in [12], the FSM can digitally scale the total injection time (t_{CI}), decided by the number of exciting cycles at each cap-bank value C_{OSC}

$$t_{\mathrm{CI}} = N \times \sum_i t_i \tag{2}$$

where N is the number of cycles to repeat at each C_{OSC}, and t_i is the period of a single cycle at ith C_{OSC}. The average amplitude of oscillation on the crystal after the chirping sequence is proportional to $\sqrt{t_{\mathrm{CI}}}$, as suggested from the Fourier transform of the chirping sequence [25] and also the time-domain

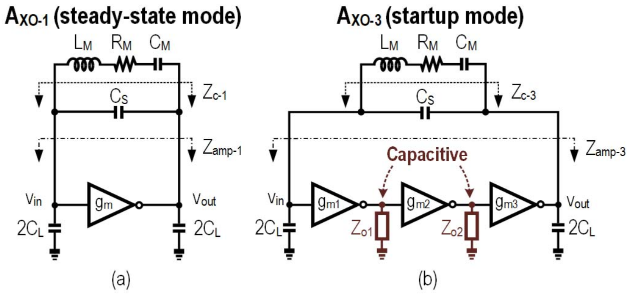

Fig. 6. XO using (a) one-single g_m ($A_{\mathrm{XO}-1}$) for the steady-state and (b) three-stage g_m ($A_{\mathrm{XO}-3}$) for the startup.

analysis in [12]. Thus, N can be programmed to adjust t_{CI}, rendering the XO easily compatible with different crystal parameters, i.e., an optimum t_{CI} depends on L_M, R_M and R_N (C_S) [12]. This digital-intensive architecture is more area efficient. The oscillation signal at the RO has varying duty-cycle with VT-variation. To maximize the injection energy (i.e., 50% duty cycle), the chirp-modulated signal is a div-by-2 output of the RO. This output serves as both the exciting signal for the crystal via the output driver, and the trigger signal for the FSM. The RO is powered down by the FSM automatically after the injection.

B. Dual-Mode g_m Scheme

The XO using a one-stage g_m ($A_{\mathrm{XO}-1}$), especially for the Pierce oscillator, is popular as it can optimize the steady-state PN [6], [12]–[14], [26]. The g_m offers a negative resistance compensating the equivalent resistance of the crystal. Its value also determines the growth of the oscillation amplitude before the XO reaches the steady state. As shown in Fig. 6(a), by omitting the resistive loss induced by $A_{\mathrm{XO}-1}$, the impedance between the I/O ($Z_{\mathrm{amp}-1}$) becomes

$$Z_{\mathrm{amp}-1} = -\frac{g_m}{4\omega_0^2 C_L^2} + \frac{1}{j\omega_0 C_L} \tag{3}$$

where C_L is the designated crystal's load capacitance and ω_0 is the angular oscillating frequency $2\pi f_0$. Since Z_{amp} is shunted by the crystal's stray capacitance (C_S), the negative resistance (R_N) of the overall impedance looking from the crystal core (Z_C) is affected

$$R_N \equiv -\mathrm{Re}(Z_c) = \frac{-\mathrm{Re}(Z_{\mathrm{amp}})}{[\omega_0 C_s \mathrm{Re}(Z_{\mathrm{amp}})]^2 + [1-\omega_0 C_s \mathrm{Im}(Z_{\mathrm{amp}})]^2}. \tag{4}$$

If $\omega_0 C_S |Z_{\mathrm{amp}}| \ll 1$, we can have $R_N \approx -\mathrm{Re}(Z_{\mathrm{amp}})$ that matches the expression in [6] for $A_{\mathrm{XO}-1}$. A large R_N favors more t_S reduction according to (1). Yet, for $|Z_{\mathrm{amp}}|$ to be comparable with $1/\omega_0 C_S$ [i.e., a higher g_m and thus $|\mathrm{Re}(Z_{\mathrm{amp}})|$ to speed up the startup], we have to cogitate the effect from C_S. Thus, we can deduce the specific R_N of $A_{\mathrm{XO}-1}$ (i.e., $R_{N,1}$) from (4) as given by

$$R_{N,1} = \frac{4 g_m C_L^2}{(g_m C_s)^2 + 16 C_L^2 \omega_0^2 (C_L + C_S)^2}. \tag{5}$$

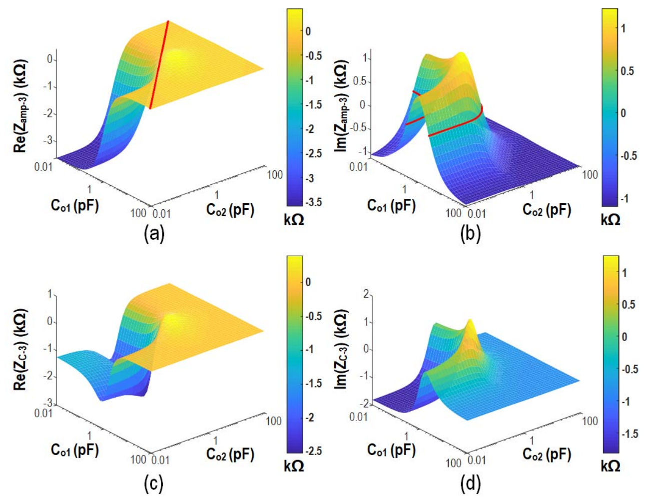

Fig. 7. Plot of the impedances as function of C_{o1} and C_{o2}. (a) $\mathrm{Re}(Z_{\mathrm{amp}-3})$. (b) $\mathrm{Im}(Z_{\mathrm{amp}-3})$. (c) $\mathrm{Re}(Z_{C-3})$. (d) $\mathrm{Im}(Z_{C-3})$. For (a) and (b), the contours where $\mathrm{Re}(Z_{\mathrm{amp}-3}) = 0$ kΩ and $\mathrm{Im}(Z_{\mathrm{amp}-3}) = 0$ kΩ are depicted with red lines.

Taking the derivative of (5), we can obtain the maximum value of $R_{N,1}$ with respect to g_m at a fixed C_L

$$R_{N,1,\max} = \frac{C_L}{2\omega_0 C_s (C_L + C_s)} \tag{6}$$

where we apply $g_m = 4\omega_0 C_L (1 + C_L/C_s)$. Obviously, $\mathrm{Im}(Z_{\mathrm{amp}-1})$ can only be negative (capacitive) for $A_{\mathrm{XO}-1}$, and $R_{N,1}$ has an upper limit if only g_m is the sizing parameter [12], [13]. For instance, $R_{N,1}$ is limited to 1.2 kΩ with $C_S = 2$ pF, $f_0 = 24$ MHz, and $C_L = 6$ pF, even if we apply an oversized $g_m = 14.5$ mS. There were efforts to raise $R_{N,1}$ by increasing g_m or tuning C_L temporarily during the startup [13], [26], [27]. Yet, increasing g_m incurs in larger power consumption and is unfavorable toward reduction of E_S. Furthermore, $R_{N,1}$ is bound by (6), and is maximally $1/2\omega_0 C_S$ (i.e., 1.66 kΩ in the above example when $C_L \gg C_S$ and $g_m \approx 4\omega_0 C_L^2/C_s$).

Inspecting (4), if a positive $\mathrm{Im}(Z_{\mathrm{amp}})$ is possible to counteract the effect of C_S, R_N can be boosted to surmount the aforesaid R_N-limit. Our idea is to mimic a microhenry-range inductor on chip for this purpose. Interestingly, it is found that a three-stage g_m ($A_{\mathrm{XO}-3}$) with designated capacitive loads (Z_{o1-2}) can effectively mimic an inductive effect during the startup [Fig. 6(b)]. Although a multistage g_m has been applied in [28] to save the XO's steady-state power, this paper explores first its inductive feature for t_S reduction. For $A_{\mathrm{XO}-3}$, we define its Z_{amp} as $Z_{\mathrm{amp}-3}$ as given by

$$\begin{aligned} Z_{\mathrm{amp}-3} &= \frac{-G_{m,\mathrm{eff}}}{4\omega_0^2 C_L^2 (1 + j\omega_0 r_{o1} C_{o1})(1 + j\omega_0 r_{o2} C_{o2})} + \frac{1}{j\omega_0 C_L} \\ &= -\frac{G_{m,\mathrm{eff}}(1 - \omega_0^2 r_{o1} C_{o1} r_{o2} C_{o2})}{4\omega_0^2 C_L^2 [1 + (\omega_0 r_{o1} C_{o1})^2][1 + (\omega_0 r_{o2} C_{o2})^2]} \\ &\quad + \frac{1}{j\omega_0 C_L} \left\{ 1 - \frac{G_{m,\mathrm{eff}} (r_{o1} C_{o1} + r_{o2} C_{o2})}{4 C_L [1 + (\omega_0 r_{o1} C_{o1})^2][1 + (\omega_0 r_{o2} C_{o2})^2]} \right\} \end{aligned} \tag{7}$$

where $G_{m,\mathrm{eff}} = g_{m1} \cdot r_{o1} \cdot g_{m2} \cdot r_{o2} \cdot g_{m3}$ and $Z_{o1/2}$ is represented as a parallel load of $r_{o1/2}$ and $C_{o1/2}$. Since at 24 MHz the impedance of $2C_L$ at the output (553 Ω) is usually much smaller than the resistive load of the third stage, its resistive part is neglected. Manifested from (7), both the real and imaginary parts of $Z_{\mathrm{amp}-3}$ are unbounded between positive and negative. For a positive $\mathrm{Im}(Z_{\mathrm{amp}-3})$, (8) has to be satisfied

$$\frac{G_{m,\mathrm{eff}}(r_{o1}C_{o1} + r_{o2}C_{o2})}{[1 + (\omega_0 r_{o1}C_{o1})^2][1 + (\omega_0 r_{o2}C_{o2})^2]} > 4C_L. \tag{8}$$

Alternatively, for a negative $\mathrm{Re}(Z_{\mathrm{amp}-3})$, we set $1/(r_{o1,2}C_{o1,2}) > \omega_0$. In a practical design, the complete independent variables are only $C_{o1,2}$ and $g_{m1,2,3}$ as $r_{o1,2}$ are correlated with $g_{m1,2}$, especially when the voltage headroom is restrained. Fig. 7(a) and (b) plots $\mathrm{Re}(Z_{\mathrm{amp}-3})$ and $\mathrm{Im}(Z_{\mathrm{amp}-3})$, as a function of $C_{o1,2}$, respectively, where we set $g_{m1,2} = 0.4$ mS, $g_{m,3} = 1.5$ mS, $r_{o1,2} = 7$ kΩ, $C_L = 6$ pF, and $\omega_0 = 2\pi \times 24$ MHz. At small $C_{o1,2}$, we have $\mathrm{Re}(Z_{\mathrm{amp}-3}) = -G_{m,\mathrm{eff}}/4\omega_0^2 C_L^2$. $\mathrm{Re}(Z_{\mathrm{amp}-3})$ increases to 0 kΩ when we enlarge $C_{o1.2}$, and turn to positive if $C_{o1}C_{o2} > 1/\omega_0^2 r_{o1} r_{o2}$ [red line in Fig. 7(a)].

For $\mathrm{Im}(Z_{\mathrm{amp}-3})$, it is negative (capacitive) for sufficient small or large $C_{o1,2}$, but can be turned to positive (inductive) within a specific range, defined by the quadratic equation in (8) and shown in Fig. 7(b). By solving (8), the desired inductive effect can be achieved. For example, for $C_{o1} = C_{o2} = 0.5$ pF, the desirable inductive impedance $Z_{\mathrm{amp}-3} = -1.6 + 1.2\mathrm{j}$ kΩ can be achieved.

Fig. 7(c) and (d) shows the changes of $\mathrm{Re}(Z_{C-3})$ and $\mathrm{Im}(Z_{C-3})$ after paralleling $A_{\mathrm{XO}-3}$, respectively, with $C_S = 2$ pF. When C_{o1} and C_{o2} are small, the value of $\mathrm{Re}(Z_{C-3})$ (i.e., $-R_{N,3}$) is alike to that of $A_{\mathrm{XO}-1}$ and is bounded by (5), in which g_m is replaced by $G_{m,\mathrm{eff}}$ that is ~ -1.2 kΩ. Such limitation can be surpassed here with an inductive $Z_{\mathrm{amp}-3}$ as derived in Fig. 7(b). For instance, for $C_{o1} = C_{o2} = 0.5$ pF, we can have $\mathrm{Re}(Z_{C-3}) = -2.4$ kΩ due to the inductive $A_{\mathrm{XO}-3}$. Thus, a higher R_N can be achieved even with similar power consumption when compared to the $A_{\mathrm{XO}-1}$, enabling an energy-efficient startup. Due to the intricate expression of $R_{N,3}$, its optimization is done numerically, as shown in Fig. 7(c), before proceeding to transistor- level implementation. Besides, our technique is also applicable to different f_0. Using a similar mathematical model derived by (4) and (7) and changing the total g_m and $C_{o1,2}$ correspondingly, we have simulated to boost the R_N by 6.1× at $f_0 = 10$ MHz and 7.4× at $f_0 = 50$ MHz with the $A_{\mathrm{XO}-3}$ compared to $A_{\mathrm{XO}-1}$. Since reference clock at 16/24 MHz is common for BLE as [6] and [13] reported, thus in this paper, we only focus on $f_0 = 16$ and 24 MHz.

Apparently, for the same power budget, $A_{\mathrm{XO}-3}$ is inferior to $A_{\mathrm{XO}-1}$ in terms of the steady-state PN, as each stage shares a smaller bias current and the noises accumulate. Also, for $\mathrm{Im}(Z_{C-3})$ that determines the exact oscillating frequency of the XO, it deviates from the designated value due to the presence of C_{o1} and C_{o2} [Fig. 7(d)]. This affects the accuracy of f_0. Thus, it is desirable to implement a dual-mode g_m scheme that can balance the startup and steady-state performances. During the startup where the PN and accuracy of f_0 are irrelevant, $A_{\mathrm{XO}-3}$ is enabled and connected to the crystal to attain a larger R_N for fast startup. When the crystal has gained sufficient energy for oscillation, $A_{\mathrm{XO}-3}$ is OFF and disconnected from the crystal while $A_{\mathrm{XO}-1}$ takes over to sustain the oscillation. As a result, the XO can benefit from both $A_{\mathrm{XO}-3}$ (fast startup) and $A_{\mathrm{XO}-1}$ (low PN and accurate f_0).

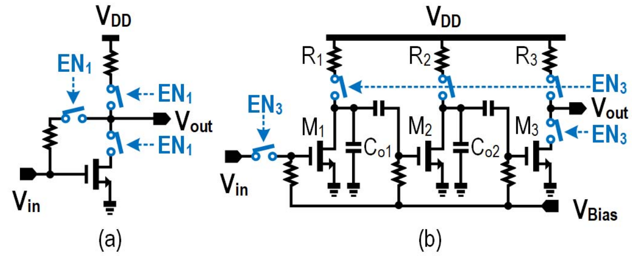

Fig. 8. Circuit implementation of (a) $A_{\mathrm{XO}-1}$ and (b) $A_{\mathrm{XO}-3}$.

III. Transistor-Level Implementation

The core elements of the XO (e.g., $A_{\mathrm{XO}-1}$, $A_{\mathrm{XO}-3}$, and RO) are designed to operate below a 0.5-V V_{DD}. Only the static and dc circuits (digital logic and constant-g_m bias circuit) operate at 0.7 V to facilitate the design. These circuits together consume <5 μA and are mostly powered-off during the steady state. Thus, the 0.7-V supply can be easily generated by an on-chip switched-capacitor charge pump and shared with other blocks at the system level as described in [22].

Both $A_{\mathrm{XO}-1}$ and $A_{\mathrm{XO}-3}$ are based on subthreshold common-source (CS) amplifiers with resistive loads [Fig. 8(a) and (b)]. Unlike other solutions that use current-source loads [6], [13], [14], the resistive load aids to preserve a moderate g_m even with $V_{\mathrm{DD}} < 0.35$ V, for a small bias current (simulated at $I_{\mathrm{dc}} = 100$ μA). For instance, the simulated g_m of $A_{\mathrm{XO}-1}$ is 1.3 mS at $V_{\mathrm{DD}} = 0.3$ V and −40 °C, being 4× higher than that of the current-source load (assuming an identical g_m with $V_{\mathrm{DD}} = 0.35$ V at 20 °C). Furthermore, at high temperature, the intrinsic output resistance of the transistor decreases rapidly. This affects the stability of R_N and causes variation on t_s, especially for $A_{\mathrm{XO}-3}$. The $A_{\mathrm{XO}-1}$ with resistive load has a tradeoff of lower immunity to power supply noise (noise power from V_{DD} modulated to the output of XO with a resistive load that is 3 dB larger than its current-source-load counterpart at 1-kHz offset). Also, it has a large f_0 variation since the g_m of $A_{\mathrm{XO}-1}$ is not fixed. Still, this is manageable for the BLE standard (<±50 ppm [29]), as well as other IoT protocols (e.g., ZigBee: ±40 ppm). A small nominal I_{dc} of 100 μA is adequate for the expected PN.

$A_{\mathrm{XO}-1}$ is self-biased by a feedback resistor R_F, whereas $A_{\mathrm{XO}-3}$ is an ac-coupled three-stage CS amplifier aided by a constant-g_m bias circuit. As revealed by (7), the g_m of the $A_{\mathrm{XO}-3}$ has a considerable impact on $R_{N,3}$. Thus, the constant-g_m bias circuit secures $A_{\mathrm{XO}-3}$ to be inductive, and a stable $R_{N,3}$ for robust-and-fast startup against PVT. The channel lengths of the transistors are chosen such that their output resistances are ∼10× larger than the resistors R_{1-3}.

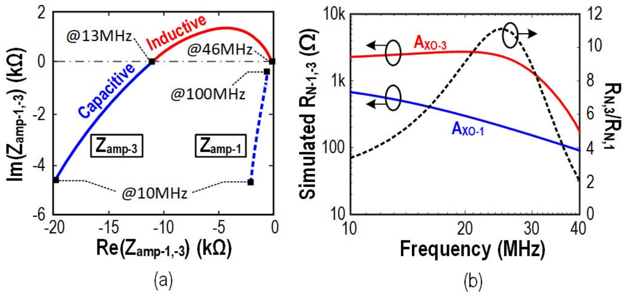

Fig. 9. (a) Locus plot of the $Z_{\text{amp}-1,-3}$ against frequency. (b) Simulated $R_{N,1}$ and $R_{N,3}$ with a fixed total g_m budget of 2.3 mS, and the boosting ratio against frequency.

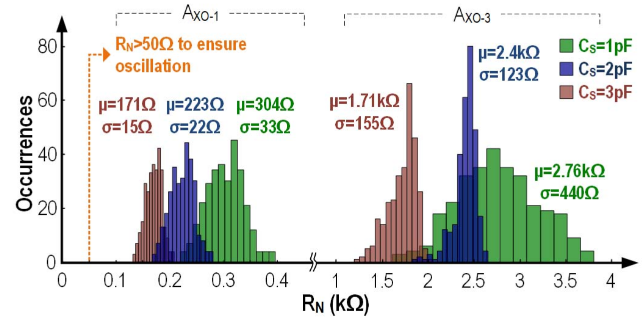

Fig. 10. Monte-Carlo-simulated R_N ($f_0 = 24$ MHz, $N = 300$, $V_{\text{DD}} = 0.35$ V).

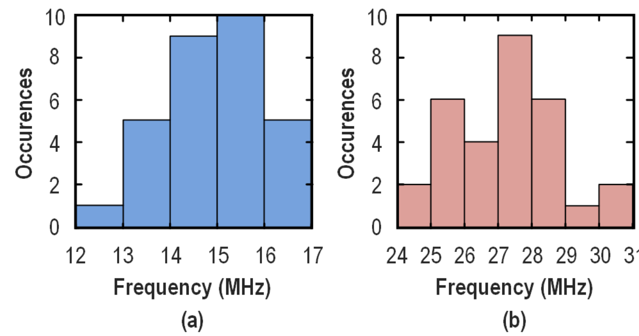

Fig. 11. (a) Monte-Carlo-simulated f_L with $V_{\text{DD}} = 0.4$ V and $T = 90$ °C. (b) Monte-Carlo-simulated f_H with $V_{\text{DD}} = 0.3$ V and $T = -40$ °C. $N = 30$ for both cases.

This soothes temperature dependence of $R_{N,3}$ as r_{o1-3} are then dominated by R_{1-3}. On the other hand, the widths of the transistors are deterministic of the parasitic capacitances. Especially for C_{GS} of the transistor, it not only is sensitive to the operating conditions and affects $C_{o1,2}$ but also forms a capacitive divider with the ac-coupling network and degrades the gain; the gain attenuation should be controlled within 5% to depress their overall impacts. $A_{\text{XO}-3}$ is designed to have similar power consumption (~100 μA) as $A_{\text{XO}-1}$. As such, the power consumption does not vary instantaneously, easing the design and layout of the power supply. CMOS switches are inserted to each current branch such that $A_{\text{XO}-1}$ or $A_{\text{XO}-3}$ can be isolated from the crystal while lowering their leakage power (simulated <14 nW at 0.35 V and 20 °C) when disabled. They have minimal channel lengths and adequate widths such that their ON-resistances are negligible when compared with R_{1-3}.

Both the parasitic capacitances of the transistors and the finite I/O resistance of $A_{\text{XO}-3}$ will affect the accuracy of the derivation from (7). Thus, $R_{N,3}$ should be further optimized via simulation. The total g_m budget is 2.3 mS (total bias current: 100 μA, assuming a $g_m/I_D = 23\ \text{V}^{-1}$), and r_{o1-3} are set according to the g_m of each gain stage. Fig. 9(a) shows the locus plots of $Z_{\text{amp}-1}$ and $Z_{\text{amp}-3}$ implemented with practical transistors and integrated passives. $Z_{\text{amp}-1}$ is capacitive over all frequencies, while $Z_{\text{amp}-3}$ is inductive over the 13-to-46-MHz range, rendering its compatible with different f_0. Optimized at the most popular XO frequency of 24 MHz, the optimum $R_{N,3}$ is 2.4 kΩ after paralleling it with a C_S of 2 pF. This result is ~9× higher than $R_{N,1}$ under the same g_m budget and surpasses $R_{N,1,\max}$ [Fig. 9(b)]. The boosting effect is insensitive to the frequency between 15 and 34 MHz, under $R_{N,3}/R_{N,1} > 6$.

The Monte-Carlo-simulated $R_{N,3}$ (mean) is >9.1× higher than $R_{N,1}$, and the boosting factor is immune to $C_s = 1$–3 pF, as specified from the crystal manufacturer (Fig. 10). We design $R_{N,1}$ to be >50 Ω against PVT to compensate the resistive loss of the crystal (measured R_M of the crystal: 19 Ω), and safeguard the oscillation as well as PN of the XO.

Ideally, $A_{\text{XO}-3}$ should be enabled for the entire startup phase. Yet the g_m values of M_{1-3} deviate from their small-signal values when the oscillation amplitude is growing. This results in an aggravated $R_{N,3}$. Thus, the optimum active time of $A_{\text{XO}-3}t_{\text{sw}}$ is the time when $R_{N,3} \approx R_{N,1}$, which means $A_{\text{XO}-3}$ no longer helps t_s reduction. The optimal t_{sw} can be found via simulations with measured crystal parameters to avoid any extra detection and control mechanism.

To realize the SSCI, a five-stage RO is constituted by CS-amplifiers with source degeneration. Compared with the RO with inverters or relaxation oscillator, an RO with CS-amplifiers balances between the frequency stability and compatibility with the sub-0.5-V V_{DD}. The source resistor (R_S in Fig. 5) also reduces the variation of oscillating frequency against V_{DD}. From the simulation, the frequency variation of RO is reduced by ~20% over a 0.3-to-0.5 V V_{DD}. R_D is set to 36 kΩ. The current consumption of the RO is 20 μA. We implemented the div-by-2 unit and FSM with a standard logic.

We designed the f_H and f_L of the SSCI module as 36 and 12 MHz, respectively, which are chosen such that $f_L < f_m < f_H$ is satisfied even with PVT variation (Fig. 11). The total size of the C_{OSC} is simulated to be 135 fF to output an f_L of 12 MHz (after div-by-2). Then, the resolution of the cap-bank should be determined. This is decided by the minimum duration of t_{CI}; since for a complete chirping sequence all of the states need to be swept at least once, the minimum t_{CI} (i.e., $N = 1$) is set by the resolution (number of pulses), as depicted in (2). The optimum t_{CI}, according to [12] and the measured crystal parameter, is derived as 4.6 μs. Thus, we set C_{OSC} as a binary-coded 6-bit cap-bank (unit cap: 2.14 fF), corresponding to a minimum t_{CI} of 4 μs with the designate

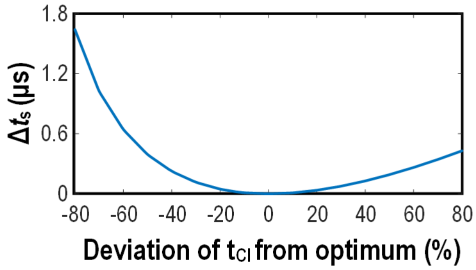

Fig. 12. Increase in t_s caused by the deviation of t_{CI} from the optimum duration.

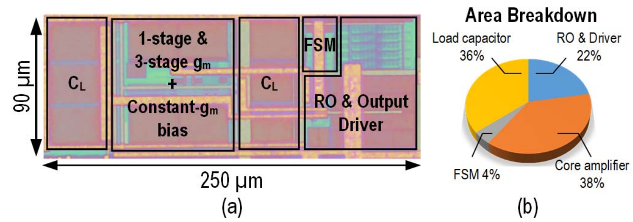

Fig. 13. (a) Chip micrograph. (b) Area breakdown of the XO.

f_H and f_L. Even though there is a discrepancy between the applied and optimum t_{CI}, the t_s is almost unaffected as the t_{CI} is only present for a short period when compared with t_s. As manifested in Section II-A, the amplitude of oscillation after the CI is proportional to $\sqrt{t_{\mathrm{CI}}}$. Thus, even the applied t_{CI} is 13% shorter than the optimum in our case, the amplitude is only 7% smaller. Thanks to the high growth of the oscillation amplitude of the $A_{\mathrm{XO}-3}$ [time constant in (1): 9.33 μs], the discrepancy between the applied and optimum t_{CI} can be compensated by the $A_{\mathrm{XO}-3}$ quickly, e.g., the 0.6 μs discrepancy is countervailed by the growth of oscillation amplitude in that 0.6 μs ($\sim$1.07×). No significant difference on t_s will emerge, even with PVT variation on the t_{CI} (Fig. 12).

The RO generates an oscillating signal at $2f_H$ with $C_{\mathrm{OSC}} =$ 0 fF (with oscillating frequency governed by the parasitic capacitances), and C_{OSC} is progressively increased by the FSM bit-by-bit according to N to $C_{\mathrm{OSC}} = 135$ fF whereas the RO oscillates at $2f_L$. In this paper, the variable N is digitally configurable among 1, 2, 4, and 8.

IV. Experimental Results

The XO was fabricated in 65-nm CMOS with fixed on-chip C_L of 6 pF. Extra cap-bank can be added to the XO for finer control of C_L if necessary. The active area is 0.023 mm^2 [Fig. 13(a)], of which 36% corresponds to the load capacitors [Fig. 13(b)]. The target f_0 can be flexible between 16 and 24 MHz. The FSM (i.e., t_{CI}) as well as the enabling of the V_{DD} are governed by a field-programmable-gate-array (Fig. 14). We first verify the SSCI functionality. Fig. 15(a) shows the measurement of the oscillating frequency of the RO (after div-by-2) against C_{OSC}, which is consistent with the post-layout simulation. The frequency range of the chirping sequence can safely cover the designated f_m against voltage and temperature variations. The average f_L and f_H across five dies at room temperature are 10.93 (σ: 0.32 MHz) and 35.96 MHz (σ: 1.21 MHz), respectively. Fig. 15(b) confirms the chirping sequence with $N = 1$ and Fig. 15(c) shows the duration of t_{CI} against N. This implies that the SSCI can generate a chirping sequence with variable t_{CI} (4–32 μs in this paper) to accommodate different crystal parameters without resorting from area-hungry RC-units.

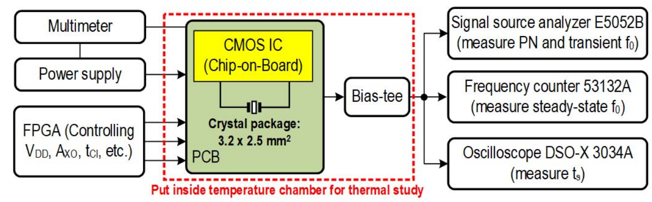

Fig. 14. Measurement setup of the XO.

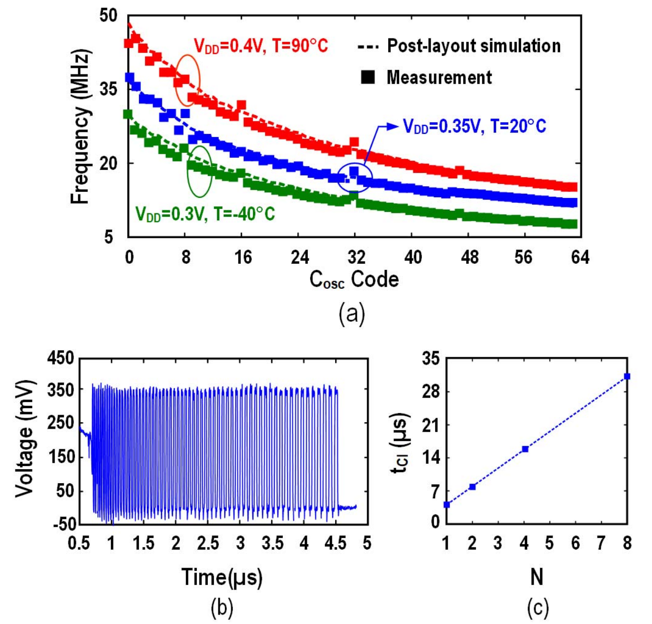

Fig. 15. (a) Measured and simulated oscillating frequencies of the RO versus C_{OSC} at different conditions, robust to cover f_0 of the crystal even with V_{DD} and temperature variations. (b) Measured chirping sequence ($N = 1$). (c) Injection duration t_{CI} against N. For the latter two figures, $V_{\mathrm{DD}} = 0.35$ V, $T = 20$ °C.

The XO was then tested with a 24-MHz crystal (package: 3.2 × 2.5 mm^2) without any startup aid at room temperature (20 °C) and $V_{\mathrm{DD}} = 0.35$ V. The measured crystal parameters L_M, R_M, C_M, and C_S are 11.1 mH, 19 Ω, 3.95 fF, and 1.3 pF, respectively. Under these conditions, we have $t_s = 1.3$ ms [Fig. 16(a)]. t_s is shortened to 530 μs when $A_{\mathrm{XO}-3}$ is enabled during the startup.

Since directly measuring R_N by inserting a resistance in series with the crystal is not viable (R_N is the real part of the impedance seen by the crystal core, which cannot be separated from the C_S), we have to estimate $R_{N,1}$ and $R_{N,3}$ from the growth of the oscillation amplitude according to (1), which can be rewritten as

$$\ln\left(\frac{A_{\mathrm{env}}(t_0+\Delta t)}{A_{\mathrm{env}}(t_0)}\right) = \frac{R_N - R_M}{2L_M}\cdot\Delta t \tag{9}$$

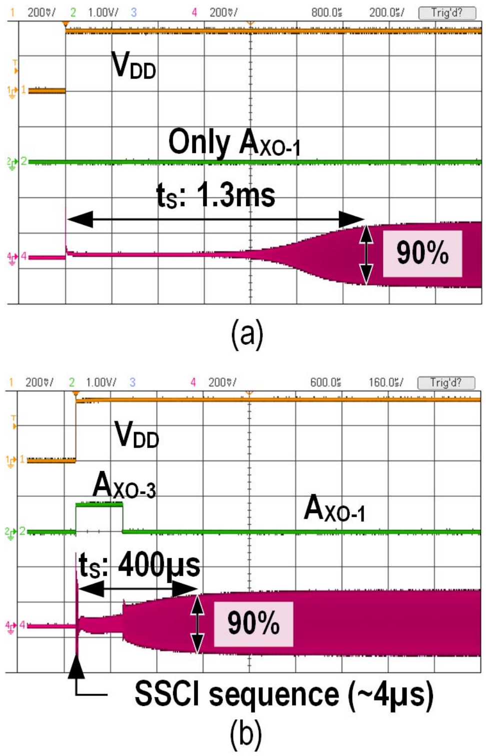

Fig. 16. Measured startup waveform (a) without startup aid and (b) with SSCI and $A_{\mathrm{XO}-3}$ enabled.

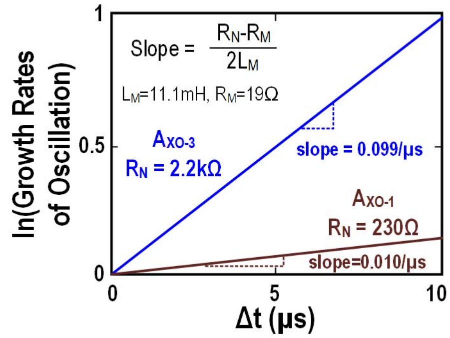

Fig. 17. Estimated R_N from the exponential growth of X_{OUT}'s amplitude (before the transistors enter triode/cutoff region).

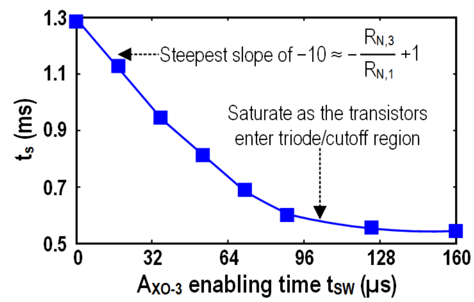

Fig. 18. Total t_s versus t_{sw}, the enabling time of $A_{\mathrm{XO}-3}$ (without SSCI).

where t_0 is the starting time and Δt is the elapsed time. Hence, by measuring the growth of the oscillation amplitude within a specific time interval, the R_N of the XO can be estimated. For $A_{\mathrm{XO}-1}$, the growth of oscillation is $1.01\times/\mu$s, and therefore $R_{N,1}$ is calculated as 230 Ω (Fig. 17), which is close to the prediction as described in Section III. Similarly, $R_{N,3} \approx 2.2$ kΩ is found. The achieved R_N-boosting factor is 9.6×, coinciding with the simulation and evincing the functionality of $A_{\mathrm{XO}-3}$.

Owing to two reasons, the reduction of t_s is not commensurate with the R_N-boosting ratio between $A_{\mathrm{XO}-3}$ and $A_{\mathrm{XO}-1}$. First, as described in Section III, M_{1-3} will deviate from their nominal operating points and deteriorate $R_{N,3}$. This can be revealed by measuring t_s against t_{sw} (Fig. 18). When t_{sw} is short (<60 μs) where M_{1-3} are in the subthreshold region, the small-signal model is still valid to estimate t_s against t_{sw} [i.e., slope of the curve (~ -10) closely matches with $-R_{N,3}/R_{N,1} + 1$]. As t_{sw} further increases, the oscillation drives M_{1-3} away from its original operating point and worsens $R_{\mathrm{N},3}$. Hence, the slope of the curve declines and eventually reaches zero whereas the $A_{\mathrm{XO}-3}$ no longer aids t_s-reduction. Second, the XO entails an overhead time to enter the steady state after switching to $A_{\mathrm{XO}-1}$. After switching to $A_{\mathrm{XO}-1}$, the XO still takes $\sim$380 μs to enter the steady state. The improvement on t_s here is limited by the nonideality of the ULV $A_{\mathrm{XO}-3}$. In fact, for the amplifiers with standard I/O voltage and higher output swing, the reduction of t_s should be more profound and better matched with the R_N-boosting ratio.

With both $A_{\mathrm{XO}-3}$ and SSCI enabled, t_S is further shortened to 400 μs (3.3× reduction) and the corresponding E_S is 14.2 nJ (2.8× reduction) [Fig. 16(b)]. When switching from $A_{\mathrm{XO}-3}$ to $A_{\mathrm{XO}-1}$ that have different output impedances and thus operating frequency, there is an instantaneous change of the output swing, since the magnitude of current passing through the crystal does not change abruptly. The percentage of energy consumed in the startup phase by the SSCI, $A_{\mathrm{XO}-3}$, and $A_{\mathrm{XO}-1}$ is 7%, 39%, and 53%, respectively. It has been verified that t_{sw} can tolerate ±50% uncertainty for $<10\%$ t_S variation, implying that an adequate t_s can be obtained even with non-optimal t_{sw} (e.g., variation on PVT and crystal's parameters). This also justifies that the existed RO will be good enough to control t_{sw}, avoiding any external detection and control mechanism.

For the transient frequency of the XO, it takes $\sim$300 μs to settle for a ±20 ppm f_0 accuracy (i.e., 50 kHz drifting from the center frequency of 2.44 GHz in a packet, as defined in [29]). This result is 3.5× faster than the case without startup aid (Fig. 19). Fig. 20 plots the summary of the reduction in t_S and E_S with different startup aids. The steady-state power is 31.8 μW at 0.35 V, and the PN is -134 dBc/Hz at 1-kHz offset [Fig. 21(a)], being adequate for most IoT applications and comparable to other state-of-the-art XOs with a standard voltage (e.g., [4], it reports a PN of -136 dBc/Hz at 1 kHz and at $f_0 = 26$ MHz). As illustrated in Fig. 21(a), the PN of the $A_{\mathrm{XO}-1}$ is 15 dB better than that of $A_{\mathrm{XO}-3}$, confirming the poorer PN performance of the $A_{\mathrm{XO}-3}$.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH RECENT ART

	This work		JSSC'16 [12]	ISSCC'16 [6]		ISSCC'17 [13]	JSSC'18 [14]¶	
Applications	BLE		Bluetooth	BLE		BLE	N/A	
Fast-startup techniques	ULV inductive 3-stage g_m + SSCI		Chirp injection + g_m-boosting	Dithered injection		Dynamic load + g_m-boosting	Precisely-timed CFI	
Steady-state techniques	ULV 1-stage g_m + resistive load		1-stage inverter	1-stage g_m + current-source load				
CMOS process (nm)	65		180	65		90	65	
Active area (mm^2)	**0.023**		0.12	0.08		0.072	0.09 (per XO)	
Supply voltage, V_{DD} (V)	**0.35***		1.5	1.68		1.0	1.0	
Temperature, T_{Range} (°C)	−40 to 90		−30 to 125	−40 to 90		−40 to 90	−40 to 85	
C_L (pF)	6		8 (off-chip)	6	9	10	9	8
Frequency, f_0 (MHz)	**16**	**24**	39.25	24	24	24	50	10
Startup energy, E_S (nJ)	**15.8**	**14.2**	349	--	--	36.7	13.3	12
Startup time, t_S (μs)	460	400	158	64	435	200†	2.2	10
$\Delta t_S/t_S$ over T_{range}	9.8%	7.5%	7%	±35%	±20%	26.6%	7%	3%
$\Delta f_0/f_0$ (ppm) versus T_{Range}	21.9 ◊	14.1 ◊	±5.5	N/A		N/A	N/A	
$\Delta f_0/f_0$ (ppm) versus V_{DD}	13.4 §	17.9 §	±0.6 (1.2 to 1.8 V)	N/A		N/A	N/A	
Steady-state power (μW)	**31.6**	**31.8**	181	393	693	95	195	45.5

* Digital & constant-g_m bias circuits are at 0.7 V (current budget: 5 μA) to be generated by an on-chip charge pump as [22].
† Amplitude >90% and $\Delta f_0/f_0$ <±20 ppm. ◊ @ 0.35 V. § Across 0.3 to 0.5 V @ 20 °C.
¶ Only results from similar crystal packages were compared.

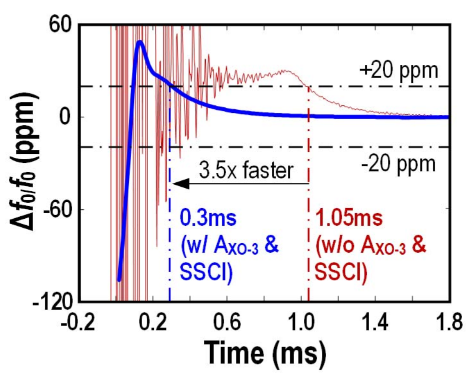

Fig. 19. Transient f_0 profiles of the XO ($V_{DD} = 0.35$ V, $T = 20$ °C).

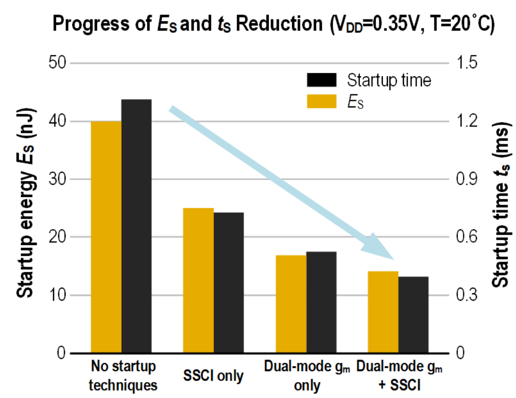

Fig. 20. Progress of E_S and t_s reduction of the XO ($f_0 = 24$ MHz) with different startup aids.

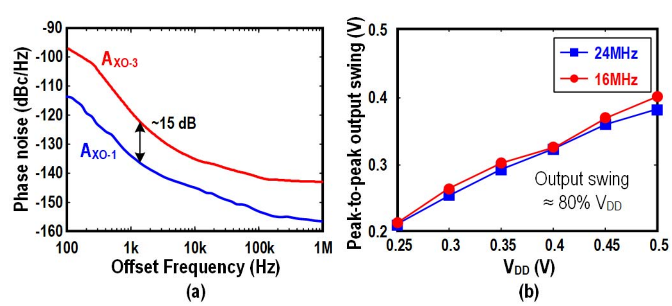

Fig. 21. (a) PN of the XO with A_{XO-1} and A_{XO-3} as core versus offset frequency ($f_0 = 24$ MHz). (b) Output voltage swing of the XO against V_{DD}.

In terms of robustness, we confirm that the XO can uphold a steady-state output swing >80% of V_{DD} for $V_{DD} = 0.3$–0.5 V [Fig. 21(b)]. For the variation of t_s against V_{DD}, it is measured <25% from its mean (400 μs) for $V_{DD} = 0.3$–0.5 V [Fig. 22(a)]. Only the RO of the SSCI fails to start if V_{DD} drops down to 0.25 V, but A_{XO-3} is still in place to aid t_S reduction. The frequency deviation ($\Delta f_0/f_0$) is 19.7 ppm (17.9 ppm) across 0.25 (0.3 V) to 0.5 V [Fig. 22(b)]. Over −40 °C–90 °C, t_S variation is <7.5% [Fig. 22(c)], and the $\Delta f_0/f_0$ is 14.1 ppm [Fig. 22(d)]. Similar results were obtained for a 16-MHz crystal [i.e., $\Delta f_0/f_0 = 13.4$ ppm over 0.3–0.5 V, $\Delta f_0/f_0 = 21.9$ ppm over −40 °C–90 °C, and t_S variation: 9.8%].

In another test, the XO was powered by a small commercial solar cell (1 × 3.8 cm^2) in an indoor environment. Its nominal output voltage is close to 0.35 V at a solar irradiance of 0.4 mW/cm^2. Then, the output voltage of the solar cell is swept by altering the light reaching the solar cell.

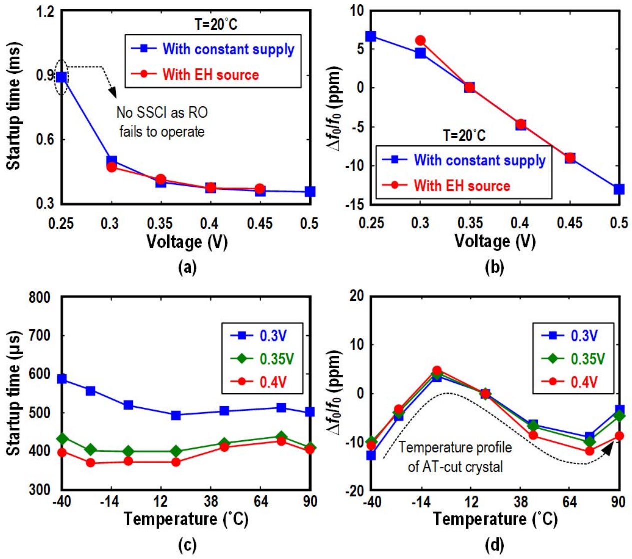

Fig. 22. Measured XO (f_0 = 24 MHz) performances. (a) Startup time against V_{DD}. (b) Frequency stability against V_{DD}. (c) Startup time against temperature. (d) Frequency stability against temperature.

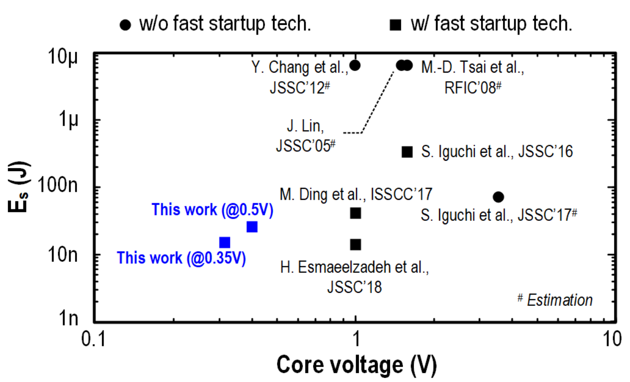

Fig. 23. Startup energy of XOs from the literature versus their core V_{DD}. Some of their E_S values (marked with #) were not reported, thus they are estimated through the multiplication of their startup times by the steady-state powers.

The measured metrics of the XO powered by the solar cell are comparable to those using a typical power supply [Fig. 22(a) and (b)].

Table II and Fig. 23 benchmark the performance of the XO with the prior art. In terms of E_s, this paper is $>2.6\times$ better than [13] and slightly higher than [14]. Furthermore, the proposed circuit can be considered in the vanguard, since it proves the feasibility of regulation-free operation under a wide range of sub-0.5-V V_{DD}, while conforming to the frequency-stability specification of the BLE standard.

V. Conclusion

A regulation-free sub-0.5-V XO for energy-harvesting BLE radios has been reported. Two circuit techniques, dual-mode g_m and SSCI, are introduced to reduce the startup time t_s and energy E_s. The dual-mode g_m exploits the inductive feature of a three-stage g_m (A_{XO-3}) to counteract C_S of the crystal during the startup, and the low-noise feature of a one-stage g_m (A_{XO-1}) to preserve the PN in the steady state. Both A_{XO-1} and A_{XO-3} are ULV-enabled using resistive-load CS amplifiers. For the SSCI, a scalable chirping sequence effectively raises the initial oscillation amplitude of the crystal under different conditions, avoiding the need of a precisely trimmed AO. The XO prototyped in 65-nm CMOS has a compact area (0.023 mm^2) that is $>3.1\times$ smaller than the prior art. The measured t_s and E_s of the XO, with a 24-MHz crystal, are 400 μs and 14.2 nJ, respectively. The frequency stability against voltage (0.3–0.5 V) is 17.9 ppm and temperature (−40 °C–90 °C) is 14.1 ppm; both conform to the BLE standard.

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