

# A Four-Phase Buck Converter With Capacitor-Current-Sensor Calibration for Load-Transient-Response Optimization That Reduces Undershoot/Overshoot and Shortens Settling Time to Near Their Theoretical Limits

Yi-Wei Huang<sup>✉</sup>, Student Member, IEEE, Tai-Haur Kuo, Senior Member, IEEE,  
Szu-Yu Huang, Student Member, IEEE, and Kuan-Yu Fang

**Abstract**—This paper presents a four-phase buck converter with capacitor-current-sensor (CCS) calibration for load-transient-response optimization that targets the theoretically minimal output-voltage undershoot  $\Delta V_{US}$ , overshoot  $\Delta V_{OS}$ , and settling time  $t_S$  when large and rapid load-current transients  $\Delta I_{load}$  occur. The proposed CCS calibration calibrates the CCS' equivalent impedance to emulate a scaled replica of the output capacitor's impedance  $Z_{Co}$ . Thus, the CCS can accurately sense the output-capacitor current  $I_{Co}$  despite  $Z_{Co}$  variations due to different output voltages, fabrication variations, and printed-circuit-board parasitics. Moreover, a load-transient optimizer is proposed to utilize the accurately sensed  $I_{Co}$  to instantly detect the large and rapid  $\Delta I_{load}$ , and synchronously control the charging and discharging durations of the output inductors in all four phases, resulting in small  $\Delta V_{US}/\Delta V_{OS}$  and short  $t_S$ . The converter is implemented in a 0.18- $\mu m$  CMOS process with 1.93-mm<sup>2</sup> chip area. For a 1.8-A/5-ns step-up (step-down)  $\Delta I_{load}$ , the measured  $\Delta V_{US}$  ( $\Delta V_{OS}$ ) and  $t_S$  are 92 mV (75 mV) and 133 ns (110 ns), respectively. Compared with other state-of-the-arts, both the measured  $\Delta V_{US}$  ( $\Delta V_{OS}$ ) and  $t_S$  in this paper are the closest to their respective theoretical limits, i.e., the fastest load-transient response with the smallest  $\Delta V_{US}$  ( $\Delta V_{OS}$ ) and the shortest  $t_S$  under the same input voltage, output voltage, output inductance, and output capacitance.

**Index Terms**—Active phase count (APC), calibration, capacitor-current sensor (CCS), dc-dc converter, fast transient, load-transient-response optimization, multiphase dc-dc converter, phase shedding.

## I. INTRODUCTION

IN MEETING the demands for increasing functionality while saving power in electronic devices, such as those with application processors, switching dc-dc converters [1]

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The authors are with the Department of Electrical Engineering, National Cheng Kung University, Tainan 70101, Taiwan (e-mail: ywhuang\_msic@ee.ncku.edu.tw; thkuo@ee.ncku.edu.tw).

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can encounter large and rapid load-current transients  $\Delta I_{load}$ , leading to large undershoots  $\Delta V_{US}$  and overshoots  $\Delta V_{OS}$ , as well as long settling times  $t_S$  in the output voltage  $V_O$ . Moreover, large  $\Delta V_{US}$  can cause function failures, large  $\Delta V_{OS}$  can reduce reliability, and long  $t_S$  can degrade performance. For example, a longer  $t_S$  due to a step-up  $\Delta I_{load}$  leads to a longer duration of  $V_O$  below its nominal value, and thus a longer duration for processors employing the adaptive clocking scheme [2] to run at lower clock frequencies. A viable solution is to implement converters with a fast load-transient response to reduce  $\Delta V_{US}$ ,  $\Delta V_{OS}$ , and  $t_S$ .

The load-transient response of a buck converter can be optimized for the fastest  $V_O$  settling with the theoretically minimal  $\Delta V_{US}$  ( $\Delta V_{OS}$ ) and  $t_S$  due to a step-up (step-down)  $\Delta I_{load}$  [1], especially when the change rate of the load current is much larger than the slope of the inductor current. If lower theoretically minimal  $\Delta V_{US}$ ,  $\Delta V_{OS}$ , and  $t_S$  with a larger effective slope of the inductor current are needed, multiphase converters are beneficial compared with single-phase ones [3]. The theoretical limits of  $\Delta V_{US}$ ,  $\Delta V_{OS}$ , and  $t_S$  are for standard dc-dc buck converters, which can be connected in parallel with low-dropout regulators [4] to further reduce  $\Delta V_{US}$  and shorten  $t_S$ ; nevertheless, this can cause degraded efficiency if large and rapid  $\Delta I_{load}$  occurs frequently.

Fig. 1 shows a diagram of an  $N$ -phase buck converter, including  $N$  power stages  $\Phi_{1-N}$ ,  $N$  output inductors  $L_{O1-N}$ , an output capacitor, and a controller. Previous works [5]–[8] have reported controllers for multiphase buck converters to provide fast load-transient response. However, the controllers in [5]–[7] cannot instantly detect large and rapid  $\Delta I_{load}$  due to the inherent delays of the pulse width modulation (PWM) trigger [5], [6] or hysteresis controller [7]. Moreover, the controllers in [6] and [7] cannot instantly enable all phases to handle large and rapid light-to-heavy  $\Delta I_{load}$  due to the employed slow-response active phase count (APC) technique, which disables some phases at light loads to maintain high efficiency over a wide load range. Furthermore, the controllers in [5]–[8] are not able to accurately control the charging  $T_{ch}$  and discharging  $T_{dch}$  durations of the output inductors during

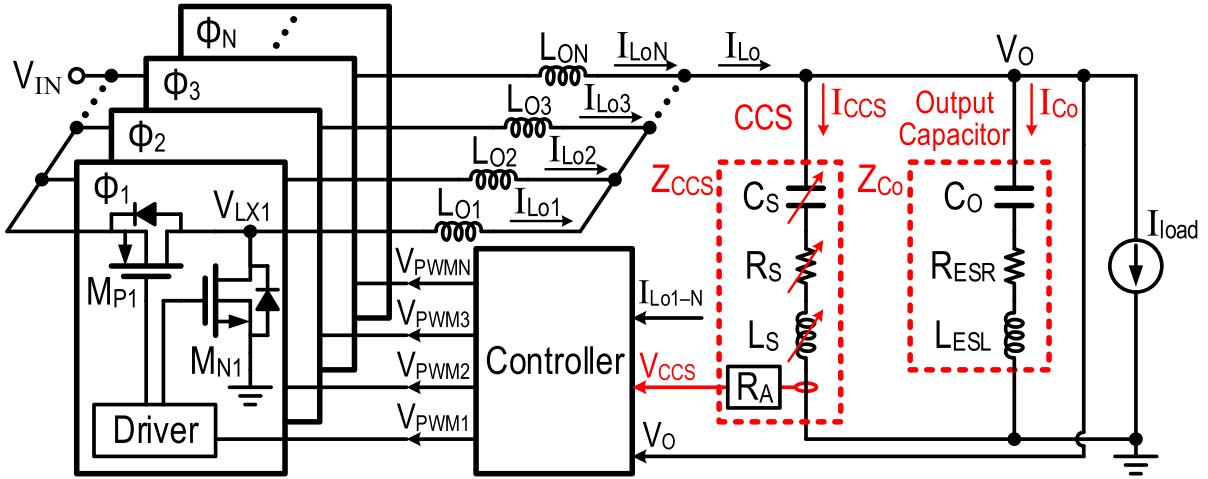


Fig. 1. Diagram of an N-phase buck converter.

load transients; as such, their load-transient responses cannot be optimized.

The load-transient response can be optimized by utilizing the output-capacitor current  $I_{Co}$  [1], which can be sensed by an invasive or non-invasive capacitor-current sensor (CCS) [1]. An invasive CCS senses  $I_{Co}$  via a resistor in series with the output capacitor, causing both  $\Delta V_{US}$  and  $\Delta V_{OS}$  to increase. A non-invasive CCS, as shown in Fig. 1, senses  $I_{Co}$  via a network in parallel with the output capacitor, where the equivalent impedance  $Z_{CCS}$  of the non-invasive CCS emulates a scaled replica of the output capacitor's impedance  $Z_{Co}$ . Because the current flowing into the non-invasive CCS is negligible, its effects on  $\Delta V_{US}$  and  $\Delta V_{OS}$  are negligible. Nevertheless, the  $I_{Co}$  sensing accuracy of a non-invasive CCS is degraded if  $Z_{Co}$  varies due to different  $V_O$ , fabrication variations, and printed-circuit-board (PCB) parasitics. Although the previous work [1] has reported non-invasive CCS implementation, the  $Z_{CCS}$  cannot be adaptively adjusted with  $Z_{Co}$  variations, and so the load-transient response can be optimized only under well-controlled circuit parameters, including  $Z_{Co}$ .

In response, this paper presents a four-phase buck converter with the proposed CCS calibration and load-transient optimizer (LTO) techniques. The CCS calibration calibrates  $Z_{CCS}$  to emulate a scaled replica of  $Z_{Co}$ , which enables the CCS to accurately sense  $I_{Co}$  despite the  $Z_{Co}$  variations. The LTO in the controller utilizes the accurately sensed  $I_{Co}$  to instantly detect large and rapid step-up (step-down)  $\Delta I_{load}$ , immediately forces the APC to enable all phases, synchronously pulls the switching nodes  $V_{LX1-4}$  in Fig. 1 high (low), and accurately control the charging  $T_{ch}$  and discharging  $T_{dch}$  durations of  $L_{O1-4}$ . In this manner, this paper achieves optimization of the load-transient response, which reduces  $\Delta V_{US}$  ( $\Delta V_{OS}$ ) and shortens  $t_S$  in  $V_O$  to near their respective theoretical limits, when large and rapid step-up (step-down)  $\Delta I_{load}$  occur.

The remainder of this paper is organized as follows. Sections II and III illustrate the CCS calibration and LTO, respectively. Section IV presents the architecture of the four-phase buck converter. Section V addresses the circuit

implementations, while Section VI provides the measured results. Finally, Section VII offers the conclusions.

## II. CAPACITOR-CURRENT-SENSOR CALIBRATION

The output-capacitor's impedance  $Z_{Co}$ , as shown in Fig. 1, comprises the capacitance  $C_O$ , equivalent series resistance  $R_{ESR}$ , and equivalent series inductance  $L_{ESL}$ . The non-invasive CCS senses output-capacitor current  $I_{Co}$  to generate a scaled sensed current  $I_{CCS}$ , i.e.,  $I_{CCS} = I_{Co}/K$ , which is then converted into  $V_{CCS}$  with a scaling factor  $R_A$ . The CCS' impedance  $Z_{CCS}$  is modeled with an equivalent series capacitance  $C_S$ , resistance  $R_S$ , and inductance  $L_S$ , and can be expressed as

$$Z_{CCS}(s) = V_O(s)/I_{CCS}(s) = 1/(s \cdot C_S) + R_S + s \cdot L_S. \quad (1)$$

The goal of CCS calibration is to adjust the impedances of  $C_S$ ,  $R_S$ , and  $L_S$  to be proportional to their respective  $C_O$ ,  $R_{ESR}$ , and  $L_{ESL}$  counterparts with the same ratio  $K$  (i.e.,  $C_S = C_O/K$ ,  $R_S = R_{ESR} \cdot K$ , and  $L_S = L_{ESL} \cdot K$ ); accordingly, the resultant  $Z_{CCS} = K \cdot Z_{Co}$ . This means that  $I_{CCS}$  is a scaled replica of  $I_{Co}$ , and so the CCS is able to accurately sense  $I_{Co}$ .

During the proposed CCS calibration, the converter operates with only  $\Phi_1$  enabled under a stable load current  $I_{load}$ ; hence, as shown in Fig. 1, assuming that the current flowing into the CCS is negligible due to the large  $K$  used in this paper; the  $\Phi_1$  inductor current  $I_{Lo1} = I_{Co} + I_{load}$ . Consequently,  $\Delta I_{Lo1} = \Delta I_{Co}$ , where  $\Delta I_{Lo1}$  and  $\Delta I_{Co}$  are  $I_{Lo1}$  and  $I_{Co}$ 's ripples, respectively. Thus,  $\Delta I_{Lo1}$  can act as the reference signal for calibrating the CCS by comparing  $\Delta I_{Lo1}$  and  $K \cdot \Delta I_{CCS}$ , where  $\Delta I_{CCS}$  is  $I_{CCS}$ 's ripple. Fig. 2 shows the operation principle of the proposed CCS calibration. Because  $Z_{Co}$  is dependent on the frequency, as the frequency increases,  $Z_{Co}$  is initially dominated by  $C_O$ , then by  $R_{ESR}$ , and finally by  $L_{ESL}$ . Hence, as shown in Fig. 2, as the frequency increases,  $Z_{Co}$  initially decreases, reaches a low point, and then finally increases. Accordingly, the calibration process is divided into three steps for calibrating  $L_S$ ,  $C_S$ , and  $R_S$ . Fig. 2 (bottom) shows a timing diagram of the

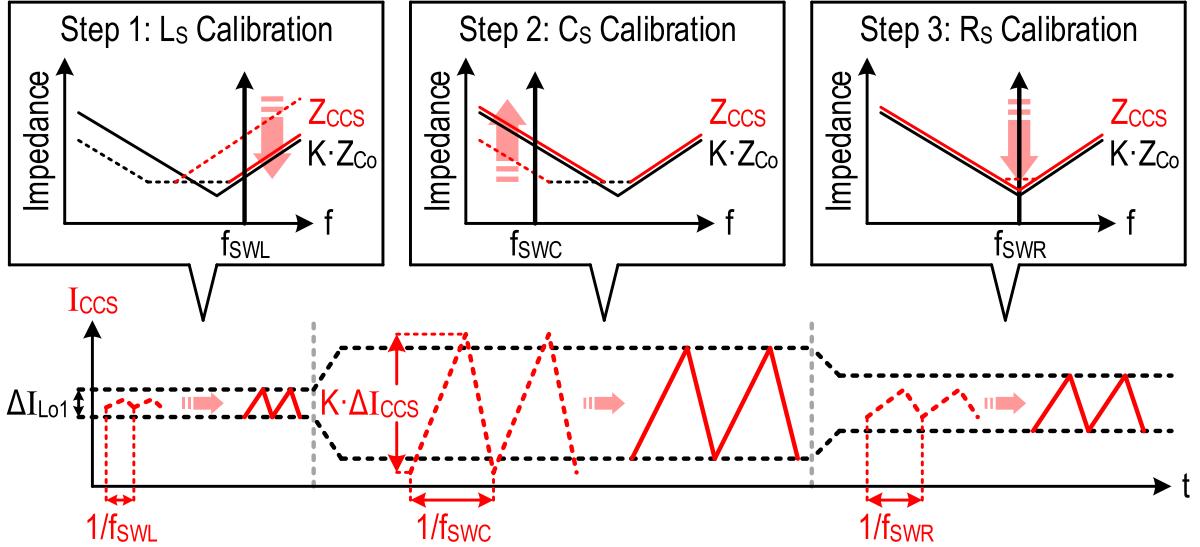


Fig. 2. Operation principle of the proposed CCS calibration with a  $Z_{CCS}$  example featuring initial  $L_S$ ,  $C_S$ , and  $R_S$  greater than their respective calibrated values.

calibration operations. During  $L_S$  calibration, the converter changes its PWM switching frequency  $f_{sw}$  to  $f_{SWL}$ , which ensures that  $Z_{Co}$  is dominated by  $L_{ESL}$  and  $Z_{CCS}$  by  $L_S$ . The variation in  $L_{ESL}$  can be identified by comparing  $\Delta I_{Lo1}$  with  $K \cdot \Delta I_{CCS}$ , and calibrated by adjusting  $L_S$  until  $K \cdot \Delta I_{CCS} = \Delta I_{Lo1}$ . During  $C_S$  calibration, the converter changes  $f_{sw}$  to  $f_{SWC}$ , which enables  $Z_{Co}$  to be dominated by  $C_O$  and  $Z_{CCS}$  by  $C_S$ . As with the variation in  $L_{ESL}$ , the variation in  $C_O$  can be similarly identified and calibrated by adjusting  $C_S$ . During  $R_S$  calibration, the converter changes  $f_{sw}$  to  $f_{SWR}$ , which makes  $R_{ESR}$  and  $R_S$ , respectively, dominate  $Z_{Co}$  and  $Z_{CCS}$ . Likewise, the variation in  $R_{ESR}$  can be identified and calibrated by adjusting  $R_S$ . Fig. 2 also shows a  $Z_{CCS}$  example, in which prior to CCS calibration, the  $Z_{CCS}$  comprises  $L_S > L_{ESL} \cdot K$ ,  $C_S > C_O/K$ , and  $R_S > R_{ESR} \cdot K$ . Accordingly, at the onset of the  $L_S$ ,  $C_S$ , and  $R_S$  calibrations,  $K \cdot \Delta I_{CCS} < \Delta I_{Lo1}$ ,  $K \cdot \Delta I_{CCS} > \Delta I_{Lo1}$ , and  $K \cdot \Delta I_{CCS} < \Delta I_{Lo1}$ , respectively. At the end of the  $L_S$ ,  $C_S$ , and  $R_S$  calibrations, the resultant  $K \cdot \Delta I_{CCS}$  values equal their corresponding  $\Delta I_{Lo1}$ .

Fig. 3 shows the simplified architecture of the proposed buck converter for CCS calibration. The CCS including  $R_A$ , CCS calibration circuit, and the power stages are integrated on chip except for the  $L_{O1-4}$  and output capacitor. Because the on-chip inductor  $L_S$  shown in Fig. 1 cannot be easily realized, a transimpedance amplifier (TIA) is used to emulate  $L_S$  [9]. As shown in Fig. 3, the TIA comprises a transconductance  $g_m$ , output capacitance  $C_{co}$ , and a feedback resistance  $R_A$ . In addition, since the TIA's output resistance is much greater than both  $R_A$  and  $R_1$ , it is ignored in this paper. The  $V_O/V_{CCS}$  in Fig. 1 can be expressed as

$$\begin{aligned} V_O(s)/V_{CCS}(s) \\ = [s^2 \cdot (L_S \cdot C_S) + s \cdot (R_S \cdot C_S) + 1]/(s \cdot C_S \cdot R_A) \quad (2) \end{aligned}$$

where  $V_{CCS}$  is converted from  $I_{CCS}$  via the TIA.

On the other hand, the  $V_O/V_{CCS}$  in Fig. 3 can be expressed as

$$\frac{V_O(s)}{V_{CCS}(s)} = \frac{s^2 \cdot \frac{C_{co}}{g_m} \cdot (R_1 + R_A) \cdot C_S + s \cdot \left( \frac{C_S + C_{co}}{g_m} + C_S \cdot R_1 \right) + 1}{s \cdot \frac{C_S}{g_m} \cdot (g_m \cdot R_A - 1)}. \quad (3)$$

By designing  $g_m \cdot R_A \gg 1$  and  $R_A \gg R_1$ , the  $R_S$  and  $L_S$  in Fig. 1 can be expressed as

$$R_S \approx R_1 + (1/g_m) \cdot (1 + C_{co}/C_S) \quad \text{and} \quad L_S \approx R_A \cdot (C_{co}/g_m). \quad (4)$$

Hence, the  $R_S$  ( $L_S$ ) in Fig. 1 can be calibrated by adjusting the  $R_1$  and  $C_{co}$  ( $C_{co}$ ) in Fig. 3. As shown in Fig. 3, the CCS calibration circuit includes a PWM generator, an amplitude comparator, and a logic circuit.  $EN_{Cal}$  is the calibration enabled signal and is generated off-chip. CCS calibration starts when  $EN_{Cal}$  is pulled high; then, the converter enables  $\Phi_1$  only and operates under open-loop control. The PWM generator generates  $D_{Cal}$  with a duty ratio of  $V_{REF}/V_{IN}$  so that  $V_O$  is regulated to its targeted value. The frequency of  $D_{Cal}$  is then changed to  $f_{SWL}$ ,  $f_{SWC}$ , and  $f_{SWR}$  for calibrating  $L_S$ ,  $C_S$ , and  $R_S$ , respectively. Both  $f_{SWL}$  and  $f_{SWC}$  are selected based on their dominant frequencies.  $f_{SWR}$ , in theory equal to  $1/(2\pi(L_{ESL} \cdot C_O)^{1/2})$  at the  $Z_{Co}$  impedance valley, is generated according to both the calibrated  $L_S$  and  $C_S$ , which are sent from the logic circuit via  $S_f$  upon completion of the  $L_S$  and  $C_S$  calibrations. Hence,  $R_S$  (and thus  $R_1$ ) is the last to be calibrated. The calibration ranges of  $C_O$ ,  $L_{ESL}$ , and  $R_{ESR}$  are analyzed in Section V-A. To ensure that the calibration range can encompass the  $Z_{Co}$  range, and that  $f_{SWL}$  and  $f_{SWC}$  are properly selected, we refer to the output capacitor's specifications, including characteristic data provided by the

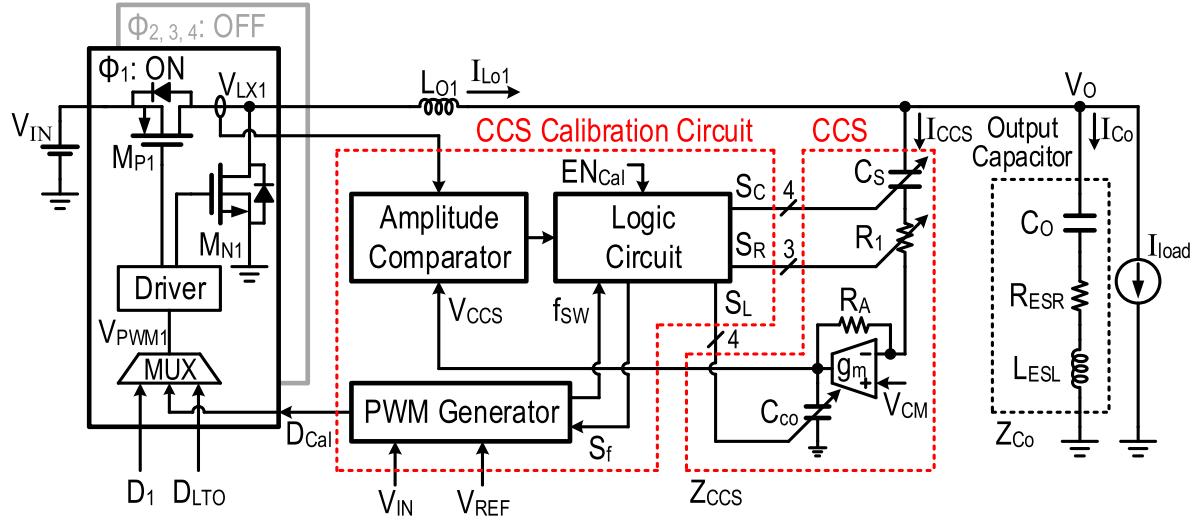
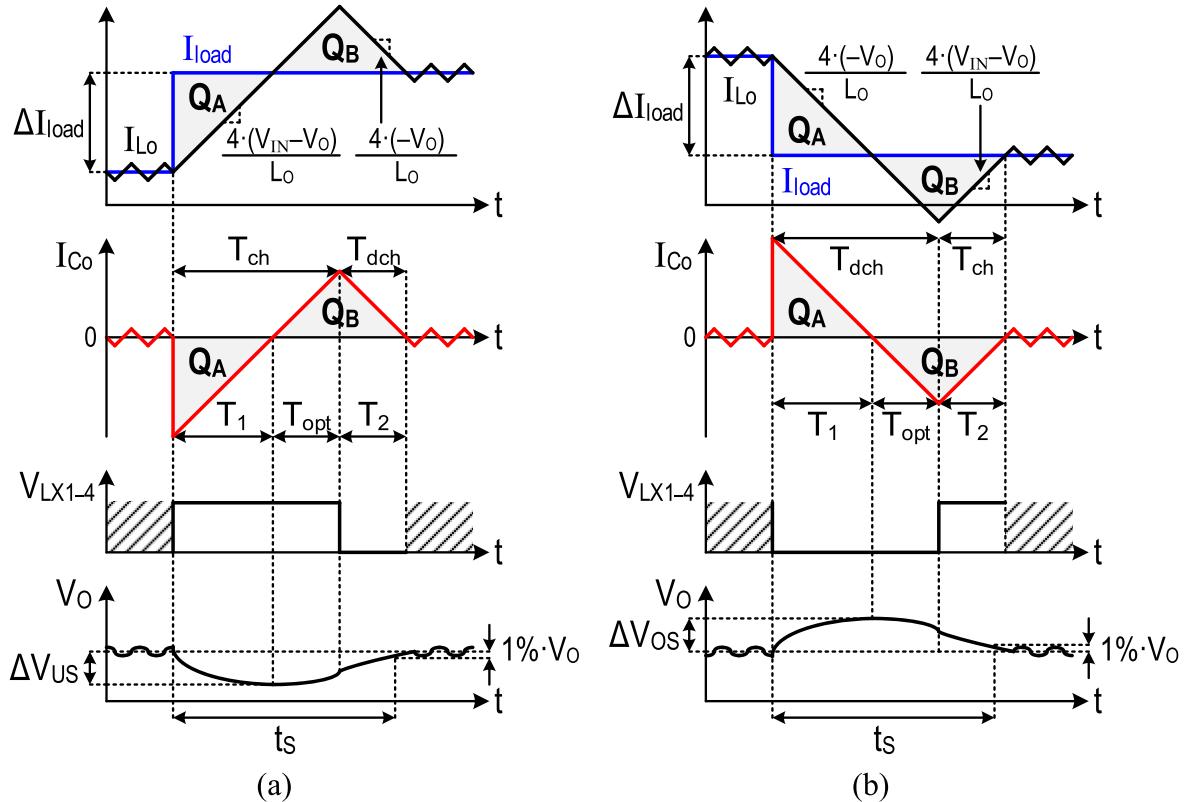


Fig. 3. Simplified architecture of the proposed buck converter during CCS calibration.

Fig. 4. Waveforms of optimized load-transient responses for large and rapid (a) step-up  $\Delta I_{load}$  and (b) step-down  $\Delta I_{load}$ , where the regions with slashes indicate that  $V_{LX1-4}$  are interleaved instead of synchronized PWM signals.

manufacturer, with margins left for the parasitics from the PCB layout. In this paper,  $f_{sw}$  is 30 MHz, while  $f_{swL}$  and  $f_{swC}$  are, respectively, selected as 17 and 4 MHz. If the  $Z_{Co}$  variations are larger,  $f_{swL}$  should be increased to cause  $Z_{Co}$  and  $Z_{CCS}$  to be more dominated by their respective  $L_{ESL}$  and  $L_S$ , while  $f_{swC}$  should be decreased to cause  $Z_{Co}$  and  $Z_{CCS}$  to be more dominated by their respective  $C_O$  and  $C_S$ . Both  $C_{co}$  and  $C_S$  are implemented as 4-bit adjustable capacitor arrays, while  $R_1$  is implemented as a

3-bit adjustable resistor array.  $I_{CCS}$  is converted into  $V_{CCS}$  via the TIA, while  $I_{Lo1}$  is obtained from the current through the high-side power switch  $M_{P1}$  and converted into  $V_{ILo1}$  via an inductor-current sensor (LCS). The amplitude comparator first obtains and compares  $V_{CCS}$ 's ripple  $\Delta V_{CCS}$  and  $V_{ILo1}$ 's ripple  $\Delta V_{ILo1}$ , after which the logic circuit adjusts  $C_{co}$ ,  $C_S$ , and  $R_1$  by the 4-bit  $S_L$ , 4-bit  $S_C$ , and 3-bit  $S_R$ , respectively. The CCS calibration ends with the completion of  $R_S$  calibration, at which point the converter returns to closed-loop control

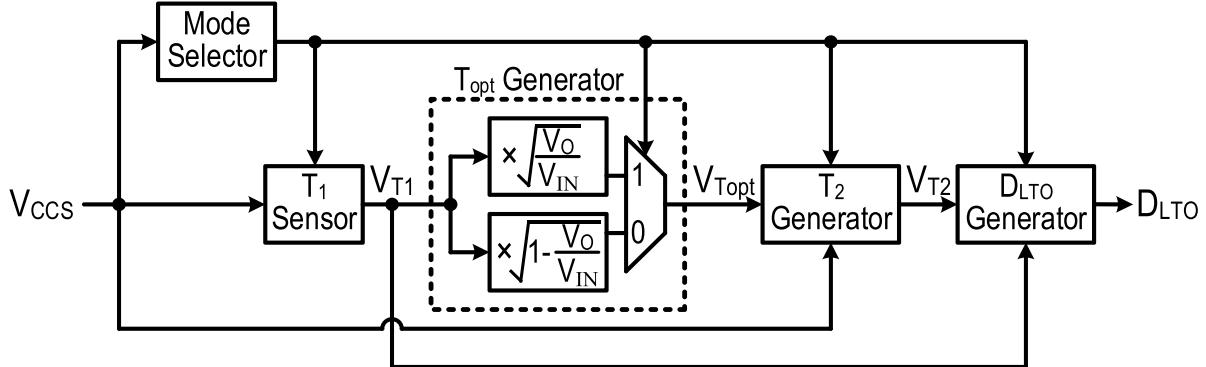


Fig. 5. Block diagram of the LTO in the proposed buck converter.

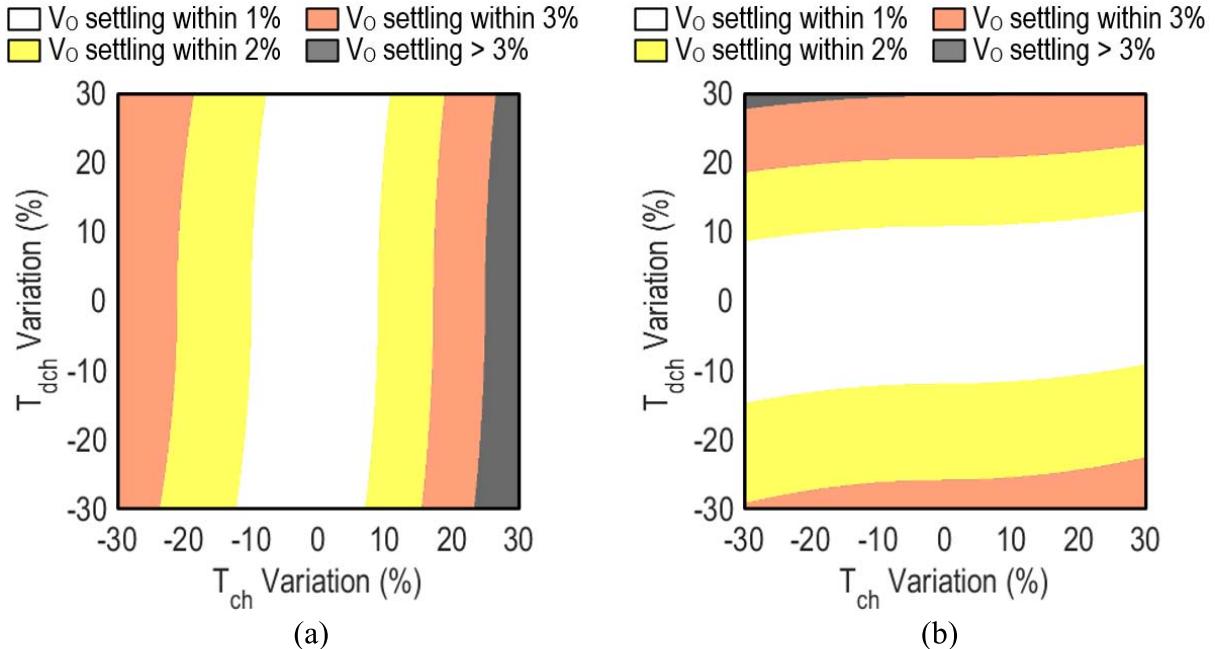


Fig. 6. Required accuracy of  $T_{ch}$  and  $T_{dch}$  for  $V_O$  settling within 1%–3% of its nominal value at the end of LTO operation against a (a) step-up  $\Delta I_{load}$  and (b) step-down  $\Delta I_{load}$ .

with the PWM switching frequency changed from  $f_{SWR}$  to  $f_{sw}$  and  $V_{PWM1}$  governed by  $D_1$  from the  $V_O$  regulation loop, as described in detail in Section IV.

The accuracy of CCS calibration can be observed by the differences in the amplitudes of  $I_{Co}$  in voltage and  $V_{CCS}$  on the same scale. For example, the converter operates with only  $\Phi_1$  enabled with  $C_O = 620$  nH,  $R_{ESR} = 20$  mΩ, and  $L_{ESL} = 0.6$  nH. The 1/2-LSB errors of  $C_S$ ,  $R_1$ , and  $C_{co}$  cause amplitude differences of about 0.2, 0.5, and 3.5 mV, respectively. The amplitude difference is dominated by the 1/2-LSB error in  $C_{co}$  since both  $Z_{Co}$  and  $Z_{CCS}$  are dominated by their respective  $L_{ESL}$  and  $L_S$  at  $f_{sw}$ . Meanwhile, the resolutions of  $C_S$ ,  $R_1$ , and  $C_{co}$  are limited by the on-chip circuit noise and component mismatch, with which achieving 4-bit accuracy is not difficult in general 0.18- $\mu$ m CMOS processes.

### III. LOAD-TRANSIENT OPTIMIZER

This section elaborates the proposed LTO technique, and then introduces the block diagram of the LTO in the proposed

buck converter. The LTO implements time-optimal control based on  $I_{Co}$  [1], which can be accurately sensed via the proposed CCS calibration. Fig. 4(a) shows the waveforms of the optimized load-transient response for large and rapid step-up  $\Delta I_{load}$ , where the change rate of  $I_{load}$  is much faster than that of the effective slope of the inductor current  $I_{Lo}$  (i.e.,  $\Delta I_{load}/\Delta t_{load} \gg \Delta I_{Lo}/\Delta t$ ), and the  $\Delta V_{US}$  is assumed to be much smaller than the targeted  $V_O$  level. According to the timing diagrams in Fig. 4(a), the occurrence of a large and rapid step-up  $\Delta I_{load}$  is instantly reflected by a step-down  $I_{Co}$ . The LTO instantly detects the  $I_{Co}$  step-down, enables all four phases  $\Phi_{1-4}$ , and pulls  $V_{LX1-4}$  high to ensure  $I_{Lo}$  rises by its steepest slope  $4 \cdot (V_{IN} - V_O)/L_O$  until  $I_{Lo}$  equals  $I_{load}$  (i.e.,  $I_{Co}$  equals zero), thereby minimizing  $Q_A$  in Fig. 4(a) and realizing the theoretically minimal  $\Delta V_{US}$ . Then, the LTO calculates the optimal time interval  $T_{opt}$ , during which  $V_{LX1-4}$  remain high. At the end of  $T_{opt}$ , the LTO turns  $V_{LX1-4}$  low to ensure  $I_{Lo}$  falls by its steepest slope  $4 \cdot (-V_O)/L_O$  until  $I_{Lo}$  equals  $I_{load}$  (i.e.,  $I_{Co}$  equals zero) again, thereby regulating  $Q_B$  to equal  $Q_A$  and realizing the theoretically minimal  $t_S$ , where

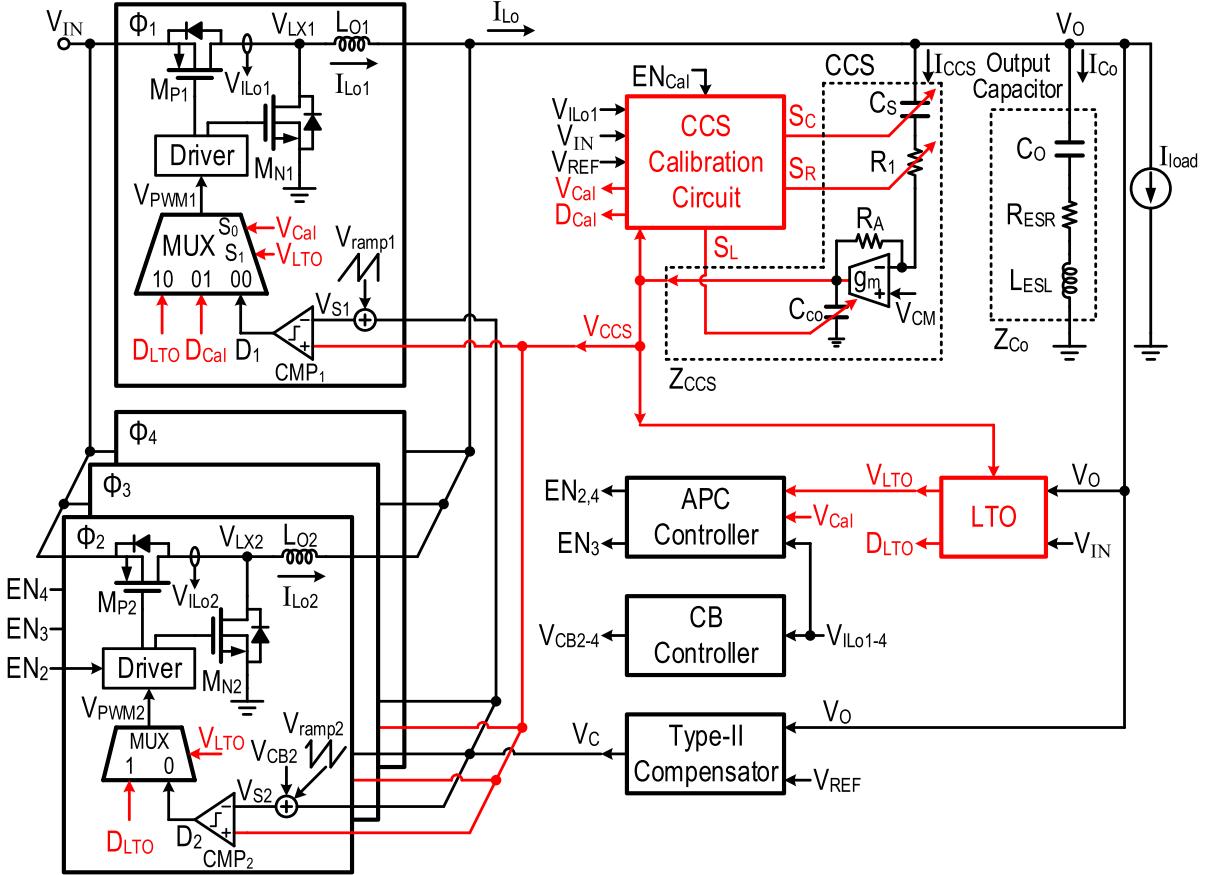


Fig. 7. Architecture of the four-phase buck converter with the proposed techniques.

$t_S$  starts from the instant of  $\Delta I_{\text{load}}$  and ends at the settling of  $V_O$  within 1% of its nominal value. In Fig. 4(a),  $T_{\text{ch}}$  can be divided into  $T_1$  and  $T_{\text{opt}}$ , while  $T_{\text{dch}}$  equals  $T_2$ , where  $T_1$  and  $T_2$  are the respective time intervals from the load transient to the first  $I_{\text{Co}}$  zero-crossing (i.e., the start of  $T_{\text{opt}}$ ) and from the end of  $T_{\text{opt}}$  to the second  $I_{\text{Co}}$  zero-crossing.  $Q_A$  and  $Q_B$  can be, respectively, expressed as

$$Q_A = (2/L_O) \cdot (V_{\text{IN}} - V_O) \cdot T_1^2 \quad (5)$$

and

$$Q_B = (2/L_O) \cdot [(V_{\text{IN}} - V_O) + (V_{\text{IN}} - V_O)^2/V_O] \cdot T_{\text{opt}}^2. \quad (6)$$

By equating (5) and (6),  $T_{\text{opt}}$  can be obtained as

$$T_{\text{opt}} = \sqrt{V_O/V_{\text{IN}}} \cdot T_1 \quad \text{for step-up } \Delta I_{\text{load}}. \quad (7)$$

Fig. 4(b) illustrates the occurrence of a large and rapid step-down  $\Delta I_{\text{load}}$ , for which LTO operations can be similarly derived with the assumption that the  $\Delta V_{\text{OS}}$  is much smaller than the targeted  $V_O$  level, resulting in the theoretically minimal  $\Delta V_{\text{OS}}$  and  $t_S$ .  $T_{\text{opt}}$  can be similarly derived and expressed as

$$T_{\text{opt}} = \sqrt{1 - V_O/V_{\text{IN}}} \cdot T_1 \quad \text{for step-down } \Delta I_{\text{load}}. \quad (8)$$

From (7) and (8), the LTO can switch  $V_{\text{LX}1-4}$  at the end of  $T_{\text{opt}}$  with  $Q_A = Q_B$  by monitoring  $T_1$ ,  $V_{\text{IN}}$ , and  $V_O$ , and then calculating the corresponding  $T_{\text{opt}}$ . In this manner,

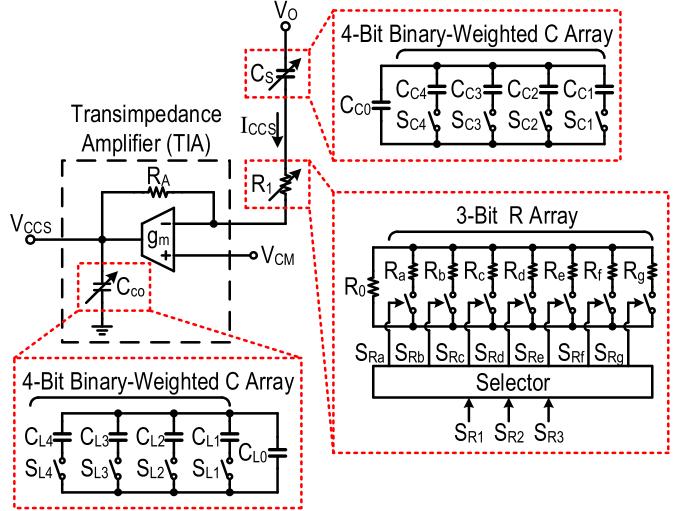


Fig. 8. CCS circuit.

the theoretically minimal  $\Delta V_{\text{US}}$ ,  $\Delta V_{\text{OS}}$ , and  $t_S$  can be obtained under different  $L_O$ ,  $V_{\text{IN}}$ , and  $V_O$ , since  $I_{\text{Co}}$  can reflect the variations in  $L_O$ ,  $V_{\text{IN}}$ , and  $V_O$  by its rising and falling slopes.

Fig. 5 shows the block diagram of the LTO, which includes a mode selector,  $T_1$  sensor,  $T_{\text{opt}}$  generator,  $T_2$  generator, and  $D_{\text{LTO}}$  generator. The mode selector has an adjustable load-transient threshold for initiating LTO operation, and detects

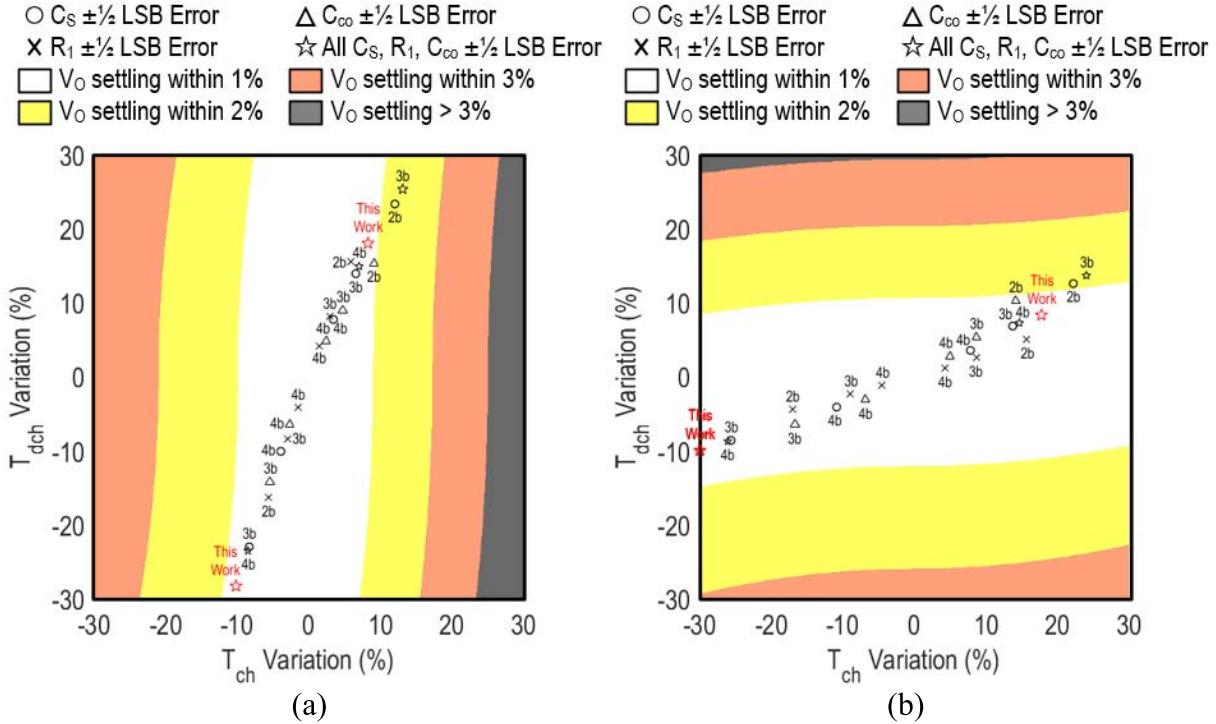


Fig. 9. Simulated variations in  $T_{\text{ch}}$  and  $T_{\text{dch}}$  with different resolutions of the CCS circuit against a (a) step-up  $\Delta I_{\text{load}}$  and (b) step-down  $\Delta I_{\text{load}}$ .

whether  $\Delta I_{\text{load}}$  is above the threshold as well as the step-up or step-down condition according to the direction of the  $V_{\text{CCS}}$  step. The  $T_1$  sensor,  $T_{\text{opt}}$  generator, and  $T_2$  generator generate pulses  $V_{T1}$ ,  $V_{\text{Topt}}$ , and  $V_{T2}$  with corresponding durations of  $T_1$ ,  $T_{\text{opt}}$ , and  $T_2$ , respectively, according to the  $V_{\text{CCS}}$  waveform. Moreover, the  $T_{\text{opt}}$  generator has two square-rooting (SQR) circuits for realizing (7) and (8). The  $D_{\text{LTO}}$  generator generates the  $D_{\text{LTO}}$  signal to govern  $V_{\text{PWM1-4}}$  during LTO operation, which comprises  $T_1$ ,  $T_{\text{opt}}$ , and  $T_2$ . The LTO operation ends at the end of  $T_2$ , after which the converter hands over control of  $V_{\text{PWM1-4}}$  to the  $V_O$  regulation loop, as described in detail in Section IV.

The accuracy of  $T_{\text{ch}}$  and  $T_{\text{dch}}$  affects  $\Delta V_{\text{US}}$ ,  $\Delta V_{\text{OS}}$ , and  $t_s$ . To analyze the required accuracy for the step-up load-transient response in Fig. 4(a), assume the nonidealities in both the  $T_1$  sensor and  $T_{\text{opt}}$  generator lead to a  $T_{\text{ch}}$  variation of  $x\%$ , while the nonidealities in the  $T_2$  generator lead to a  $T_{\text{dch}}$  variation of  $y\%$ . To achieve the theoretically minimal  $\Delta V_{\text{US}}$ , the following equation must be satisfied:

$$T_{\text{ch}} \cdot (1 + x\%) \geq T_1. \quad (9)$$

For example,  $V_{\text{IN}} = 3.3$  V and  $V_O = 1.8$  V. From (9),  $x \geq -42.4$ . To achieve  $V_O$  settling within  $z\%$  of its nominal value at the end of  $T_{\text{dch}}$ , the following equation must be satisfied:

$$|\Delta Q_B / C_O| < V_O \cdot z\% \quad (10)$$

where  $\Delta Q_B = (2/L_O) \cdot \{(V_{\text{IN}}/V_O) \cdot (V_{\text{IN}} - V_O) \cdot T_{\text{ch}}^2 \cdot [(1 + x\%)^2 - 1] + V_O \cdot (T_{\text{dch}} \cdot y\%)^2 \cdot \text{sgn}(-y)\}$  and is the error of  $Q_B$  at the end of  $T_{\text{dch}}$ . On the other hand, the required accuracies of  $T_{\text{ch}}$  and  $T_{\text{dch}}$  for the step-down load-transient response

in Fig. 4(b) can be similarly analyzed. Fig. 6(a) and (b) shows the required accuracy of both  $T_{\text{ch}}$  and  $T_{\text{dch}}$  for  $V_O$  settling within 1%–3% of its nominal value at the end of LTO operation against a step-up and step-down  $\Delta I_{\text{load}}$ , respectively.

#### IV. ARCHITECTURE OF THE FOUR-PHASE BUCK CONVERTER

Fig. 7 shows the architecture of the proposed four-phase buck converter with the proposed CCS calibration and LTO techniques. As aforementioned, the CCS senses and converts  $I_{\text{Co}}$  into  $V_{\text{CCS}}$ . During CCS calibration, the CCS calibration circuit calibrates the CCS to ensure  $I_{\text{CCS}}$  emulates a scaled replica of  $I_{\text{Co}}$  despite the  $Z_{\text{Co}}$  variations. When a large and rapid  $\Delta I_{\text{load}}$  occurs, the LTO enables all four phases  $\Phi_{1-4}$  and accurately controls the  $T_{\text{ch}}$  and  $T_{\text{dch}}$  of  $I_{\text{Lo1-4}}$ , resulting in the fastest  $V_O$  settling with the theoretically minimal  $\Delta V_{\text{US}}$ ,  $\Delta V_{\text{OS}}$ , and  $t_s$ . When in steady state or with a small  $\Delta I_{\text{load}}$ , the converter performs multiphase capacitor-current-mode control, during which the  $I_{\text{Co}}$  information, contained in  $I_{\text{CCS}}$ , is fed forward to the PWM comparators  $\text{CMP}_{1-4}$  for fast load-transient response, while  $V_O$  is fed back to the type-II compensator for precise  $V_O$  regulation. The type-II compensator integrates the error between  $V_O$  and  $V_{\text{REF}}$  to output the error signal  $V_C$ . The ramp generator generates the four-phase interleaved ramp signals  $V_{\text{ramp1-4}}$  to synchronize  $\Phi_{1-4}$ . The current-balancing (CB) controller balances the averages of  $I_{\text{Lo1-4}}$ , namely,  $I_{\text{Lo1-4,avg}}$ , by the master-slave method [6], in which  $\Phi_1$  is the master phase while  $\Phi_{2-4}$  are the slave phases. Accordingly,  $I_{\text{Lo2-4,avg}}$  track  $I_{\text{Lo1,avg}}$  by adding the additional error signals  $V_{\text{CB2-4}}$  to the sum of  $V_C$  and  $V_{\text{ramp2-4}}$ , respectively. Thus, the output  $D_1$  of  $\text{CMP}_1$

is determined by  $V_{CCS}$ ,  $V_C$ , and  $V_{ramp1}$ , while the outputs  $D_{2-4}$  are determined by  $V_{CCS}$ ,  $V_C$ ,  $V_{ramp2-4}$ , and  $V_{CB2-4}$ . Furthermore, the unity-gain bandwidth of the current-balance loop is designed to be much lower than that of the capacitor-current-mode control loop. Hence, operations of the CB controller lead to negligible  $V_O$  fluctuations. The APC controller adjusts the number of enabled phases from one  $\rightarrow$  two ( $EN_3$  pulled high)  $\rightarrow$  four ( $EN_3$  and  $EN_{2,4}$  pulled high) according to the average  $I_{load}$ , which is obtained from the sum of  $I_{Lo1-4,avg}$ . Moreover, to prevent the APC controller from limiting the load-transient response against large and rapid  $\Delta I_{load}$ , the LTO forces the APC controller to enable all four phases  $\Phi_{1-4}$  during  $T_{ch}$  and  $T_{dch}$ , as shown in Fig. 4(a) and (b). Further, during  $T_{ch}$ , the APC controller can estimate the enabled phases required after LTO operation by obtaining  $I_{Lo}$  from the  $\Phi_{1-4}$  LCSs, thereby eliminating possible  $V_O$  fluctuations in most cases. For step-up  $\Delta I_{load}$  which requires four-phase operation after LTO operation, since  $I_{Lo}$  is greater than  $I_{load}$  at the end of  $T_{ch}$ , the APC controller will enable all four phases right after LTO operation. However, since the  $\Phi_{1-4}$  LCSs do not measure  $I_{Lo1-4}$  during  $T_{dch}$ , for some other step-up  $\Delta I_{load}$ ,  $V_O$  will have another undershoot after LTO operation due to changes in the enabled phases from four to two. Specifically, this undershoot is due to step-up  $\Delta I_{load}$  requiring two-phase operation after LTO operation, but the APC controller estimates a four-phase operation during  $T_{ch}$ . Nevertheless, this issue can be eliminated by implementing  $\Phi_{1-4}$  LCSs capable of measuring  $I_{Lo1-4}$  during both  $T_{ch}$  and  $T_{dch}$ . For step-down  $\Delta I_{load}$ , as shown in Fig. 4(b), since  $T_{ch}$  is the last time interval during LTO operation, the APC controller can enable the required phases immediately after LTO operation.

## V. CIRCUIT IMPLEMENTATIONS

This section addresses the circuit implementations of the proposed four-phase buck converter. The following Sections V-A–V-E show the circuits of the CCS, CCS calibration, LTO, APC controller, and CB controller, respectively.

### A. CCS Circuit

Fig. 8 shows the CCS circuit, in which  $V_{CM}$  is the common-mode bias voltage of  $V_{CCS}$ . The adjustable  $C_S$ ,  $R_1$ , and  $C_{co}$  are, respectively, implemented in a 4-bit binary-weighted capacitor array  $C_{C1-4}$ , a 3-bit resistor array  $R_{a-g}$ , and a 4-bit binary-weighted capacitor array  $C_{L1-4}$ . The configurations of  $C_S$ ,  $R_1$ , and  $C_{co}$  are controlled by  $S_{C1-4}$ ,  $S_{R1-3}$ , and  $S_{L1-4}$ , respectively.  $S_{R1-3}$  selects one of the  $R_{a-g}$  to be paralleled with  $R_0$ , and the values of  $(R_0//R_A)$ ,  $(R_0//R_B)$ , ..., and  $(R_0//R_g)$  form an arithmetic progression. The CCS gain is defined as  $V_{CCS}/I_{Co}$  and can be expressed as the product of  $I_{CCS}/I_{Co} = 1/K$  and  $V_{CCS}/I_{CCS} = R_A$ , as shown in Fig. 1. Moreover, considering the voltage swing of  $V_{CCS}$  under the maximum  $\Delta I_{load}$ ,  $V_{CCS}/I_{Co}$  is designed as 1/2 in this paper. Since  $K = 2 \cdot R_A$ , the resultant  $C_S$ ,  $R_1$ , and  $C_{co}$  can be expressed as

$$C_S = C_O/(2R_A), \quad R_1 = R_{ESR} \cdot (2R_A) - (1/g_m) \cdot (1 + C_{co}/C_S), \quad \text{and} \quad C_{co} = L_{ESL} \cdot (2g_m). \quad (11)$$

In this paper,  $g_m$  and  $C_{co}$  are implemented by a folded-cascode OPAMP for high dc gain and wide unity-gain bandwidth; and for the negligible circuit delay of the CCS, the slew rate of the OPAMP is designed to be greater than the maximum  $\Delta I_{load}/\Delta t_{load}$ . Moreover,  $g_m = 150 \mu\text{A/V}$ ,  $C_{co}$ ,  $C_S$ , and  $R_1$  range from 90 to 375 fF, 567 to 1250 fF, 1.75 to 17.5 k $\Omega$ , respectively, and  $R_A = 300 \text{ k}\Omega$ . From (11), the calibration ranges of  $C_O$  and  $L_{ESL}$  are approximately 340–750 nF and 0.3–1.25 nH, respectively, while that of  $R_{ESR}$  can be as wide as 14.8–46.4 m $\Omega$ , resulting in easily achievable and reliable designs, even with large component variations.

The  $\pm 1/2$ -LSB errors of  $C_S$ ,  $R_1$ , and  $C_{co}$  can lead to variations in  $T_1$ ,  $T_{opt}$ , and  $T_2$ , all of which can cause deviations in the optimized load-transient response. For example,  $V_{IN} = 3.3 \text{ V}$ ,  $V_O = 1.8 \text{ V}$ ,  $\Delta I_{load}/\Delta t_{load} = 1.8 \text{ A}/5 \text{ ns}$ ,  $L_O = 220 \text{ nH}$ ,  $C_O = 620 \text{ nF}$ ,  $R_{ESR} = 20 \text{ m}\Omega$ , and  $L_{ESL} = 0.6 \text{ nH}$ . With  $\pm 1/2$ -LSB errors in  $C_S$ ,  $R_1$ , and  $C_{co}$ , for the step-up load-transient response, the simulated  $\Delta V_{US}$  variations are negligible, while the simulated  $t_S$  variations are approximately 3.2, 14, and 3.9 ns, respectively. On the other hand, for the step-down load-transient response, the simulated  $\Delta V_{OS}$  variations are negligible, while the simulated  $t_S$  variations are approximately 7.8, 8.7, and 8.1 ns, respectively. Thus, the required resolution of the CCS circuit is dominated by the requirement of  $t_S$ . Fig. 9(a) and (b) shows the simulated variations in  $T_{ch}$  and  $T_{dch}$  with different resolutions of the CCS circuit against a step-up and step-down  $\Delta I_{load}$ , respectively. The symbols  $\circ$ ,  $\times$ , and  $\Delta$  denote that only the  $C_S$ ,  $R_1$ , and  $C_{co}$  have  $\pm 1/2$ -LSB errors, respectively, while the symbol  $\star$  denotes that all of the  $C_S$ ,  $R_1$ , and  $C_{co}$  have  $\pm 1/2$ -LSB errors. In this paper, the  $\pm 1/2$ -LSB errors of the implemented 4-bit  $C_S$ , 3-bit  $R_1$ , and 4-bit  $C_{co}$  are sufficient for  $V_O$  settling within 1% at the end of LTO operation.

### B. CCS Calibration Circuit

Fig. 10(a)–(d) shows the CCS calibration circuit including the LCS, amplitude comparator, logic circuit, and PWM generator, respectively. Fig. 10(a) shows the LCS circuit [10], which senses  $I_{Lo1}$  to output  $V_{ILo1}$  during  $M_{P1}$  ON (and  $M_{N1}$  OFF). The common-gate (CG) amplifier ensures  $V'_{LX1} \approx V_{LX5}$ , and thus the current  $I_{SEN}$  through the senseFET  $M_{PS}$  equals  $I_{Lo1}/M$ , where  $M$  is the width ratio of  $M_{P1}$  to  $M_{PS}$ . Since the CG amplifier sinks a bias current  $I_B$  from  $I_{SEN}$ , another path with a current  $I_B$  is added to  $R_{SEN}$  for  $V_{ILo1} = R_{SEN} \cdot (I_{Lo1}/M)$ . Fig. 10(b) shows the amplitude comparator for obtaining and comparing  $\Delta V_{ILo1}$  and  $\Delta V_{CCS}$ , and generating the comparison result  $V_{comp}$ .  $\Delta V_{ILo1}$  ( $\Delta V_{CCS}$ ) is obtained from subtraction of  $V_{ILo1}$ 's ( $V_{CCS}$ 's) peak and average values from the sample–hold (S/H).  $D_{Cal}$  ( $D_{CalX}$ ) is the clock for sampling the peak (average) value. Different  $f_{sw}$  values lead to different  $\Delta I_{Lo1}$  and  $\Delta I_{CCS}$  swings in calibrating  $L_S$ ,  $C_S$ , and  $R_S$ , during which the respective  $S_{CalL}$ ,  $S_{CalC}$ , and  $S_{CalR}$  turn high for similar  $\Delta V_{ILo1}$  and  $\Delta V_{CCS}$  swings, thereby simplifying the comparator design. Fig. 10(c) shows the logic circuit for sequentially configuring  $S_{L1-4}$ ,  $S_{C1-4}$ , and  $S_{R1-3}$ , where the logic high of  $V_{Cal}$  indicates the duration of CCS calibration, while the logic highs of  $S_{CalL}$ ,  $S_{CalC}$ , and  $S_{CalR}$

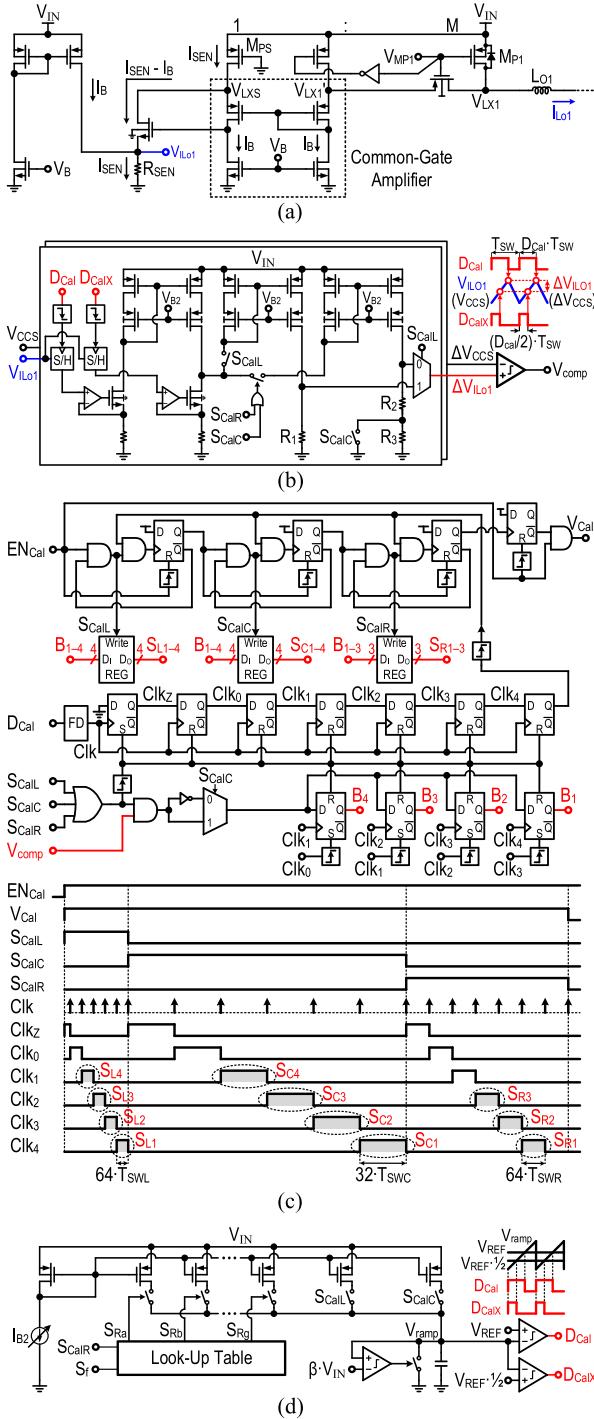


Fig. 10. CCS calibration circuit including (a) LCS, (b) amplitude comparator, (c) logic circuit, and (d) PWM generator.

sequentially indicate the durations of  $L_S$ ,  $C_S$ , and  $R_S$  calibration. The adjustment clock Clk of  $S_{L1-4}$ ,  $S_{C1-4}$ , and  $S_{R1-3}$  is generated from  $D_{Cal}$  via a frequency divider (FD). The respective Clk periods in configuring each bit of  $S_{L1-4}$ ,  $S_{C1-4}$ , and  $S_{R1-3}$  are  $64 \cdot T_{SWL}$ ,  $32 \cdot T_{SWC}$ , and  $64 \cdot T_{SWR}$ , respectively, where  $T_{SWL} = 1/f_{SWL}$ ,  $T_{SWC} = 1/f_{SWC}$ , and  $T_{SWR} = 1/f_{SWR}$ . When  $EN_{Cal}$  turns high, both  $V_{Cal}$  and  $S_{CalL}$  turn high, and the rising edge of  $S_{CalL}$  sets  $Clk_z$  high. Then, the subsequent five Clk rising edges make  $Clk_0-4$  sequentially

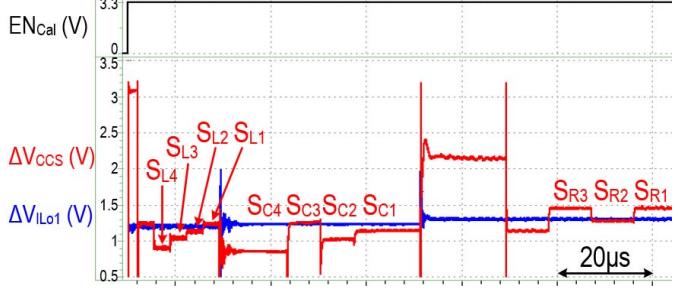


Fig. 11. Simulated waveforms for verifying the CCS calibration.

turn high. During the  $Clk_1-4$  highs, both  $B_{4-1}$  and  $S_{L4-1}$  are individually determined by  $V_{comp}$ , the comparison result of  $\Delta V_{ILo1}$  and  $\Delta V_{CCS}$  in Fig. 10(b). That is,  $S_{L1-4}$  are adjusted via successive approximations. The following  $Clk_4$  falling edge turns  $S_{CalL}$  low to end  $L_S$  calibration and turns  $S_{CalC}$  high to start  $C_S$  calibration. Then,  $S_{C4-1}$  and  $S_{R3-1}$  can be similarly determined. Finally, the falling edge of  $S_{CalR}$  turns  $V_{Cal}$  low to end CCS calibration. Fig. 10(d) shows the PWM generator circuit, which generates the respective PWM signals  $D_{Cal}$  and  $D_{CalX}$  with duty ratios of  $V_{REF}/(\beta \cdot V_{IN})$  and  $(1/2) \cdot V_{REF}/(\beta \cdot V_{IN})$  for sampling the peak and average values of both  $V_{ILo1}$  and  $V_{CCS}$  in Fig. 10(b). During  $L_S$ ,  $C_S$ , and  $R_S$  calibrations, the respective frequencies of both  $D_{Cal}$  and  $D_{CalX}$ , namely,  $f_{SWL}$ ,  $f_{SWC}$ , and  $f_{SWR}$ , are switched by  $S_{CalL}$ ,  $S_{CalC}$ , and  $S_{CalR}$ . In addition,  $f_{SWR}$  is adjusted by  $S_f$  via a lookup table, where  $S_f$  contains the calibrated  $S_{L3-4}$  and  $S_{C3-4}$  bits. Fig. 11 shows the simulated waveforms for verifying the CCS calibration. At the end of the  $L_S$ ,  $C_S$ , and  $R_S$  calibrations, their respective  $\Delta V_{CCS}$  and  $\Delta V_{ILo1}$  are all similar.

### C. LTO Circuit

Fig. 12(a) shows the LTO circuit.  $V_{BL}$  ( $V_{BH}$ ) is the adjustable threshold for enabling LTO when a step-up (step-down)  $\Delta I_{load}$  occurs. The logic high of  $V_{LTO}$  indicates the LTO is enabled, the logic high of  $S_U$  ( $S_D$ ) specifies the LTO is operating for a step-up (step-down)  $\Delta I_{load}$ , and the logic highs of  $V_{T1}$ ,  $V_{Top}$ , and  $V_{T2}$ , respectively, represent LTO operation in the  $T_1$ ,  $T_{opt}$ , and  $T_2$  regions. When a step-up  $\Delta I_{load}$  causes  $V_{CCS} < V_{BL}$ ,  $S_U$  turns high to change  $V_H$  from  $V_{BH}$  to  $V_{IN}$  to ensure  $V_{CCS}$  does not cross  $V_H$  and mistakenly pull  $S_U$  low in the  $T_{opt}$  region, while  $S_D$  remains low. Meanwhile,  $V_{LT}$  turns high to turn  $V_{T1}$ ,  $V_{LTO}$ , and  $D_{LTO}$  high.  $V_{T1}$ 's pulsewidth  $T_1$  is converted to a voltage  $V'_{T1}$  via a time-to-voltage converter ( $T \rightarrow V$ ). As  $V_{CCS}$  rises and crosses  $V_{CM}$ ,  $V_{ZC}$  turns high to turn  $V_{T1}$  low and  $V_{Top}$  high, while  $V_{TopREF}$  equals  $V'_{T1} \cdot (V_O/V_{IN})^{1/2}$  by the SQR circuit.  $V_{Top}$ 's pulsewidth  $T_{opt}$  is converted to  $V'_{Top}$  via a  $T \rightarrow V$ . As  $V'_{Top}$  rises and crosses  $V_{TopREF}$ ,  $V_{Top}$  turns low, and so  $V_{Top}$ 's pulse width  $T_{opt}$  equals  $T_1 \cdot (V_O/V_{IN})^{1/2}$ . Meanwhile,  $V_{T2}$  turns high and  $D_{LTO}$  turns low. As  $V_{CCS}$  falls and crosses  $V_{CM}$  again,  $V_{ZC}$  turns low to turn  $V_{T2}$  and  $V_{LTO}$  low, indicating the end of LTO operation. When a step-down  $\Delta I_{load}$  causes  $V_{CCS} > V_{BH}$ , the LTO operations can be derived similarly. Fig. 12(b) shows the SQR circuit.  $(V_O/V_{IN})^{1/2}$  is generated by comparing  $\beta \cdot V_O$  and a quadratic ramp  $V_2$  with an amplitude

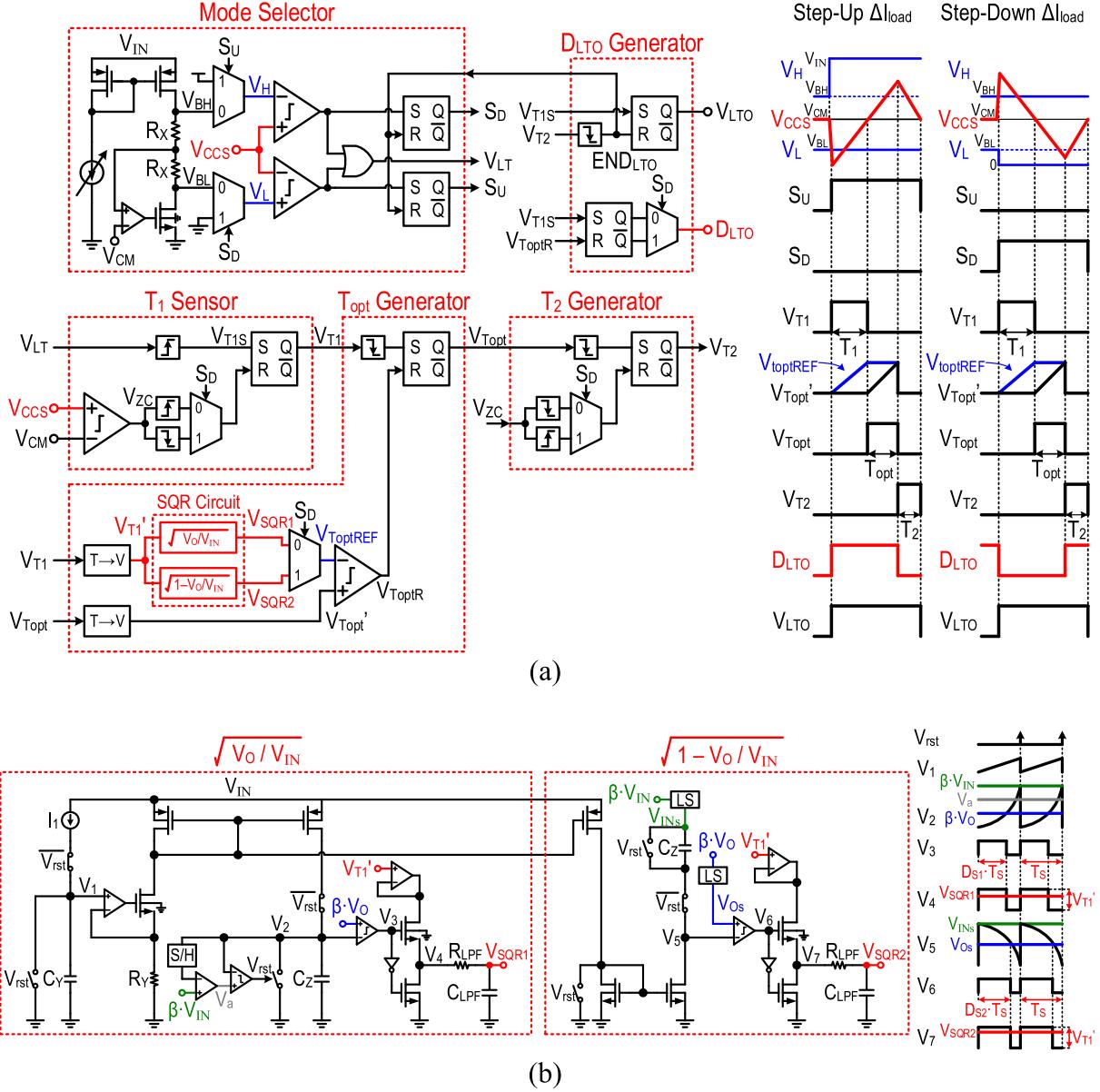
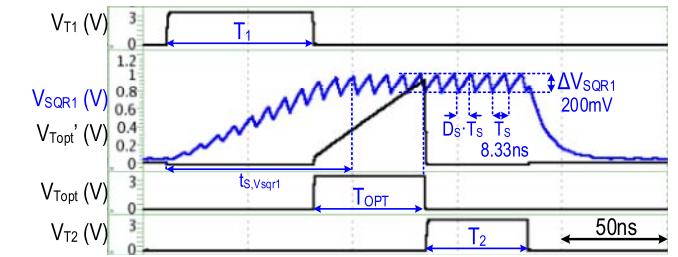


Fig. 12. (a) LTO circuit including its (b) SQR circuit.

of  $\beta \cdot V_{IN}$ , where  $V_2$  is generated by integrating a linear ramp  $V_1$  and resetting to GND by  $V_{rst}$  when  $V_2$ 's amplitude reaches  $\beta \cdot V_{IN}$ . The S/H and OPAMP compensate the error in  $V_3$ 's duty ratio  $D_{S1}$  due to the comparator delay [11], resulting in  $D_{S1}$  equaling  $(V_O/V_{IN})^{1/2}$ .  $V_3$  is level-shifted to  $V_4$  with an amplitude of  $V'_T$ .  $V_4$  is then low-pass filtered to  $V_{SQR1}$  with a dc of  $V'_T \cdot D_{S1} = V'_T \cdot (V_O/V_{IN})^{1/2}$ . On the other hand,  $(1 - V_O/V_{IN})^{1/2}$  is generated by comparing  $V_{Os}$  with the inverting quadratic ramp  $V_5$  with an amplitude of  $V_{INs}$ , where  $V_{Os}$  ( $V_{INs}$ ) is  $\beta \cdot V_O$  ( $\beta \cdot V_{IN}$ ) with a level shifter. The derivation of  $V_6$  ( $V_7$ ) is similar to  $V_3$  ( $V_4$ ), and the dc of output  $V_{SQR2}$  equals  $V'_T \cdot (1 - V_O/V_{IN})^{1/2}$ .

Fig. 13 shows the simulated waveforms of the SQR circuit for a step-up  $\Delta I_{load}$ . The design of the low-pass filter comprising  $R_{LPF}$  and  $C_{LPF}$  in Fig. 12(b) has a tradeoff between the settling time  $t_{S,Vsqr1}$  and ripple  $\Delta V_{SQR1}$ . The  $R_{LPF} \cdot C_{LPF}$

Fig. 13. Simulated waveforms of the SQR circuit for a step-up  $\Delta I_{load}$ .

must be sufficiently small to ensure  $t_{S,Vsqr1} < (T_1 + T_{opt})$ , while the  $R_{LPF} \cdot C_{LPF}$  must be sufficiently large to guarantee small  $\Delta V_{SQR1}$  and thus small  $T_{opt}$  variations. In this paper, the switching frequency  $T_S$  of the SQR circuit is designed as 120 MHz, while the  $R_{LPF} \cdot C_{LPF}$  is designed as 7 ns.

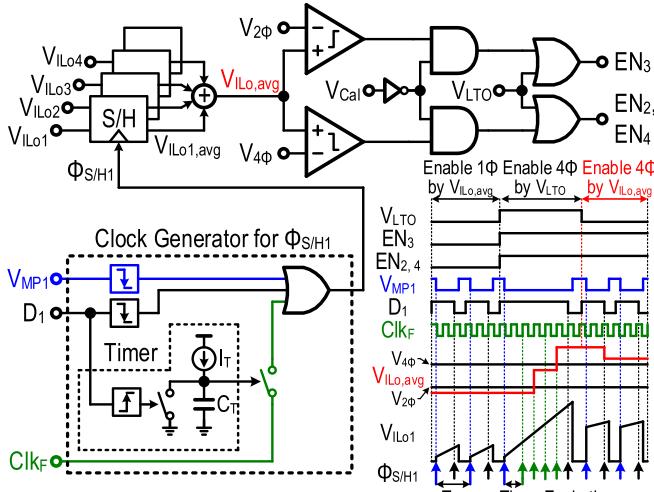


Fig. 14. APC controller circuit.

The simulated  $\Delta V_{SQRI}$  is about 200 mV, and the resultant worst case  $T_{\text{opt}}$  variation is about 3 ns.

#### D. APC Controller Circuit

Fig. 14 shows the APC controller circuit, which adjusts the enabled phases according to either  $V_{\text{Cal}}$ ,  $V_{\text{LTO}}$ , or by comparing the sum of  $I_{\text{Lo}1-4,\text{avg}}$  in voltage  $V_{\text{ILo},\text{avg}}$  with two adjustable boundaries  $V_{2\Phi}$  and  $V_{4\Phi}$ . During CCS calibration,  $V_{\text{Cal}}$  is high, and APC turns  $\text{EN}_{2-4}$  and  $\text{EN}_3$  low to enable  $\Phi_1$  only. During LTO operation,  $V_{\text{LTO}}$  is high, and APC turns  $\text{EN}_{2-4}$  and  $\text{EN}_3$  high to enable  $\Phi_{1-4}$ . By contrast, the APC controller enables one, two, or four phases when  $V_{\text{ILo},\text{avg}} < V_{2\Phi}$ ,  $V_{2\Phi} < V_{\text{ILo},\text{avg}} < V_{4\Phi}$ , or  $V_{\text{ILo},\text{avg}} > V_{4\Phi}$ , respectively.  $V_{\text{ILo}1-4,\text{avg}}$  are obtained by sampling  $V_{\text{ILo}1-4}$ 's peaks and valleys via  $S/H$ . Since the clock generators for the  $S/H$  clocks  $\Phi_{S/H1-4}$  are the same, only that for  $\Phi_{S/H1}$  is shown for simplicity. During steady state,  $\Phi_{S/H1-4}$  turn high at the falling edges of  $D_{1-4}$  ( $V_{\text{MP}1-4}$ ) to sample  $V_{\text{ILo}1-4}$ 's peaks (valleys), where  $V_{\text{MP}1-4}$  are the gate voltages of  $M_{\text{P}1-4}$  in Fig. 7. During the load-transient state ( $V_{\text{LTO}}$  is high), since  $V_{\text{ILo}1-4}$  can continue rising for several  $T_{\text{sw}}$  ( $= 1/f_{\text{sw}}$ ) with  $D_{1-4}$  high, there is no falling edge of  $V_{\text{MP}1-4}$  to S/H the valleys of  $V_{\text{ILo}1-4}$ ; thus,  $V_{\text{ILo},\text{avg}}$  cannot be updated. In this way, after LTO operation, the APC controller enables only one phase and then gradually enables the other three phases, leading to additional  $V_O$  fluctuations. To solve this problem, four timers and a clock  $\text{Clk}_F$  are used to estimate  $I_{\text{Lo}1-4,\text{avg}}$  during LTO operation. As shown in the waveforms of Fig. 14, if  $D_{1-4}$ 's rising edges do not occur over a specified time period, the timers expire, and  $\text{Clk}_F$  is used to turn  $\Phi_{S/H1-4}$  high to update  $V_{\text{ILo},\text{avg}}$ , where the frequency of  $\text{Clk}_F$  must be sufficiently high (four  $\cdot f_{\text{sw}}$  in this paper) to  $S/H$   $V_{\text{ILo}1-4}$  and update  $V_{\text{ILo},\text{avg}}$  several times during LTO operation. Therefore, the number of enabled phases can still be four immediately after LTO operation, thereby eliminating the additional  $V_O$  fluctuations.

#### E. CB Controller Circuit

Fig. 15 shows the CB controller circuit, which balances  $I_{\text{Lo}1-4,\text{avg}}$  by making  $I_{\text{Lo}2-4,\text{avg}}$  track  $I_{\text{Lo}1,\text{avg}}$ .  $I_{\text{Lo}1-4,\text{avg}}$  are

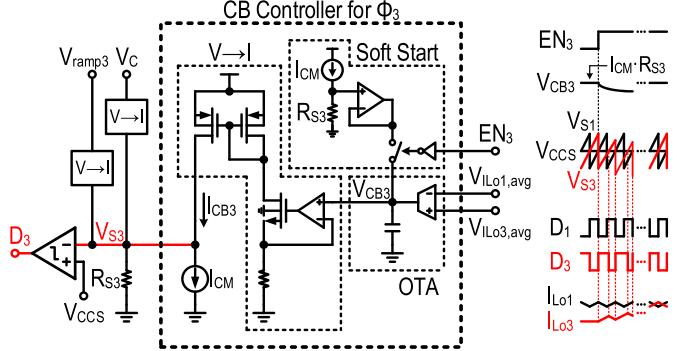


Fig. 15. CB controller circuit.

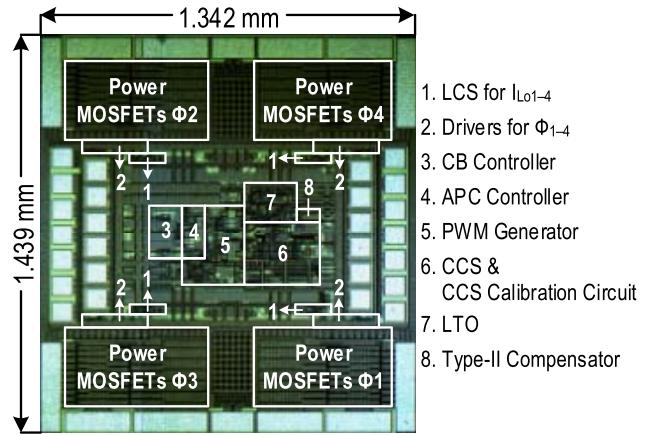


Fig. 16. Chip micrograph.

then converted into  $V_{\text{ILo}1-4,\text{avg}}$ , respectively. Since the circuits for  $\Phi_{2-4}$  are the same, only the part for  $\Phi_3$  is shown for simplicity. The OTA generates an error signal  $V_{\text{CB}3}$  by integrating the error between  $V_{\text{ILo}1,\text{avg}}$  and  $V_{\text{ILo}3,\text{avg}}$ . The voltage-to-current converter ( $V \rightarrow I$ ) converts  $V_{\text{CB}3}$  into  $I_{\text{CB}3}$ , and the resultant voltage  $I_{\text{CB}3} \cdot R_{\text{S}3}$  shifts  $V_{\text{S}3}$ 's level to change  $D_3$ 's duty ratio. The current source  $I_{\text{CM}}$  biases the common-mode voltage of  $V_{\text{S}3}$ . For example, if  $\text{EN}_3 = 1$  and  $V_{\text{ILo}1,\text{avg}} = V_{\text{ILo}3,\text{avg}}$ , the resultant  $I_{\text{CB}3} = I_{\text{CM}}$ , so the CB controller has no effect on  $V_{\text{S}3}$  and  $D_3$ . However, if  $V_{\text{ILo}1,\text{avg}} > V_{\text{ILo}3,\text{avg}}$ ,  $V_{\text{CB}3}$  falls and  $I_{\text{CB}3} < I_{\text{CM}}$ , so  $V_{\text{S}3}$  falls, resulting in an increase of  $D_3$ 's duty ratio and  $I_{\text{Lo}3,\text{avg}}$  (and  $V_{\text{ILo}3,\text{avg}}$ ), and vice versa. Moreover, a soft start is used to prevent large fluctuations in  $I_{\text{Lo}2-4}$  due to APC operations. Without the soft start,  $V_{\text{CB}3}$  is pulled to GND when  $\text{EN}_3 = 0$ , and the dc level of  $V_{\text{S}3}$  is lower than that of  $V_{\text{S}1}$  by  $I_{\text{CM}} \cdot R_{\text{S}3}$ . As  $\text{EN}_3$  is pulled high by the APC controller,  $V_{\text{CB}3}$  rises slowly due to the low bandwidth of the current-balance loop; as such,  $D_3$ 's duty ratio initially saturates at 1, and then decreases slowly to its steady-state value, causing large fluctuations in  $I_{\text{Lo}3}$  and  $V_O$ . With the soft start, the dc levels of  $V_{\text{S}3}$  and  $V_{\text{S}1}$  are the same when  $\text{EN}_3 = 0$ . Thus, as  $\text{EN}_3$  is pulled high, the initial duty ratio of  $D_3$  emulates that of  $D_1$ , thereby reducing the fluctuations in  $I_{\text{Lo}3}$  and  $V_O$ .

## VI. MEASUREMENT RESULTS

The converter is fabricated in TSMC 0.18- $\mu\text{m}$  CMOS process using 3.3-V devices. Fig. 16 presents the chip micrograph, the chip area of which is 1.93 mm<sup>2</sup>. For chip operation,

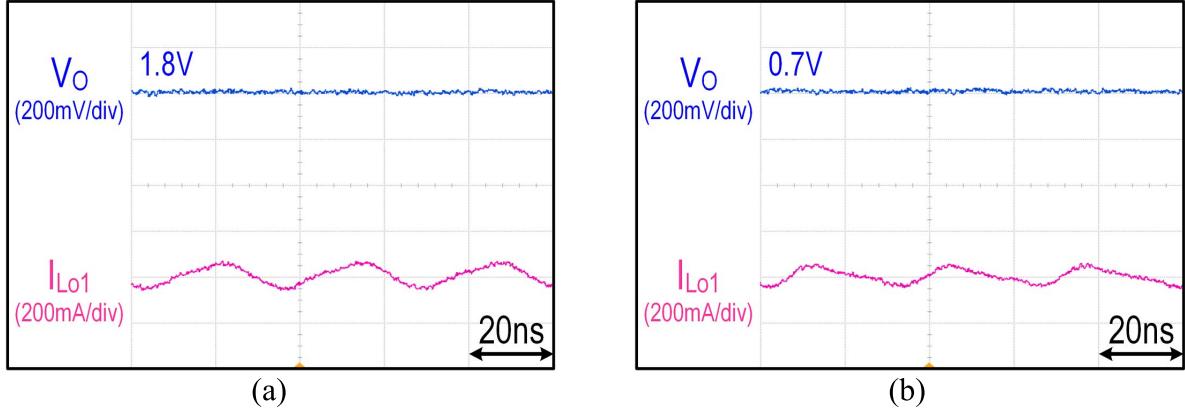


Fig. 17. Measured steady-state responses under (a)  $V_O = 1.8$  V and (b)  $V_O = 0.7$  V.

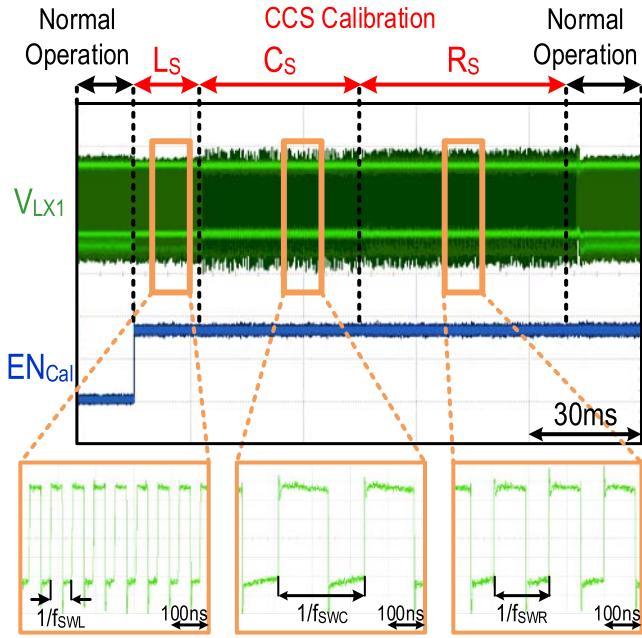


Fig. 18. Measured waveforms during CCS calibration.

$V_{IN}$  is 3.3 V,  $V_O$  ranges from 0.7 to 3 V, the maximum  $I_{load}$  is 2.5 A, and  $f_{sw}$  is 30 MHz. The output inductors  $L_{O1-4}$  are 220 nH. From the measured  $Z_{CO}$  of the selected output capacitor under  $V_O = 1.8$  V, the effective  $C_O$  is 620 nF, while  $f_{swl}$  and  $f_{swc}$  are selected as 17 and 4 MHz, respectively. Unless otherwise specified, the following results are measured under the nominal  $V_O$  of 1.8 V.

Fig. 17(a) and (b) shows the steady-state  $V_O$  and  $I_{L01}$  waveforms under  $V_O = 1.8$  and 0.7 V, respectively. Fig. 18 shows the measured waveforms during CCS calibration, which starts when  $EN_{Cal}$  is pulled high. The frequency change of  $V_{LX1}$  means that  $L_{ESL}$ ,  $C_O$ , and  $R_{ESR}$  are sequentially calibrated with the selected  $f_{swl}$  and  $f_{swc}$ , the resultant  $f_{swr}$  of which is 8 MHz. Fig. 19 shows the measured load-transient responses with and without CCS calibration, for which the LTO is enabled in both cases. Only in the case with CCS calibration can the LTO generate the optimal  $T_{ch}$  and  $T_{dch}$  during load transient, achieving an optimized load-transient response.

Fig. 20(a) and (b) presents the measured load-transient responses, both with and without LTO, against a step-up and step-down  $\Delta I_{load}/\Delta t_{load} = 1.8$  A/5 ns and  $-1.8$  A/5 ns, respectively. When the step-up  $\Delta I_{load}$  occurs without the LTO, the converter cannot instantly enable all four phases, resulting in non-optimized  $\Delta V_{US} = 225$  mV and  $t_S = 712$  ns. In contrast, with the LTO, the converter instantly enables all four phases and pulls  $V_{LX1-4}$  high to guarantee  $I_{Lo}$  charges the output capacitor with its steepest slope, resulting in  $\Delta V_{US} = 100$  mV and  $t_S = 133$  ns. For the step-up  $\Delta I_{load}$ , the theoretical minima of  $\Delta V_{US}$  and  $t_S$ , denoted as  $\Delta V_{US,min}$  and  $t_{S,min}$ , can be derived as (12) and (13), and are 89 mV and 126 ns, respectively.

$$\begin{aligned} \Delta V_{US,min} &= 1/(2C_O) \cdot [\Delta I_{load}^2 \cdot (L_O/4)/(V_{IN}-V_O) - \Delta I_{load} \cdot \Delta t_{load}]. \\ (12) \end{aligned}$$

$$\begin{aligned} t_{S,min} &= \Delta I_{load} \cdot \frac{L_O/4}{V_{IN}-V_O} \cdot \left\{ 1 + \sqrt{\frac{V_{IN}}{V_O} \left[ 1 - \frac{V_{IN}-V_O}{L_O/4} \cdot \frac{\Delta t_{load}}{\Delta I_{load}} \right]} \right\} \\ &\quad - \sqrt{2 \cdot (L_O/4) \cdot C_O \cdot 1\%}. \\ (13) \end{aligned}$$

When a step-down  $\Delta I_{load}$  occurs with the LTO, the measured  $\Delta V_{OS}$  and  $t_S$  are reduced from 102 to 75 mV and 370 to 110 ns, respectively. For the step-down  $\Delta I_{load}$ , the theoretical minima of  $\Delta V_{OS}$  and  $t_S$ , denoted as  $\Delta V_{OS,min}$  and  $t_{S,min}$ , can be derived by (14) and (15), and are 73 mV and 104 ns, respectively.

$$\begin{aligned} \Delta V_{OS,min} &= 1/(2C_O) \cdot [\Delta I_{load}^2 \cdot (L_O/4)/V_O - \Delta I_{load} \cdot \Delta t_{load}]. \\ (14) \end{aligned}$$

$$\begin{aligned} t_{S,min} &= \Delta I_{load} \cdot \frac{L_O/4}{V_O} \cdot \left\{ 1 + \sqrt{\frac{V_{IN}}{V_{IN}-V_O} \left( 1 - \frac{V_O}{L_O/4} \cdot \frac{\Delta t_{load}}{\Delta I_{load}} \right)} \right\} \\ &\quad - \sqrt{2 \cdot \frac{V_O}{V_{IN}-V_O} \cdot (L_O/4) \cdot C_O \cdot 1\%}. \\ (15) \end{aligned}$$

Fig. 21(a) shows the measured load-transient responses against a step-up  $\Delta I_{load}/\Delta t_{load} = 1.8$  A/5 ns with the APC controller disabled, in which  $\Phi_{1-4}$  are always enabled. The measured  $\Delta V_{US} = 92$  mV and  $t_S = 133$  ns, where the  $\Delta V_{US}$

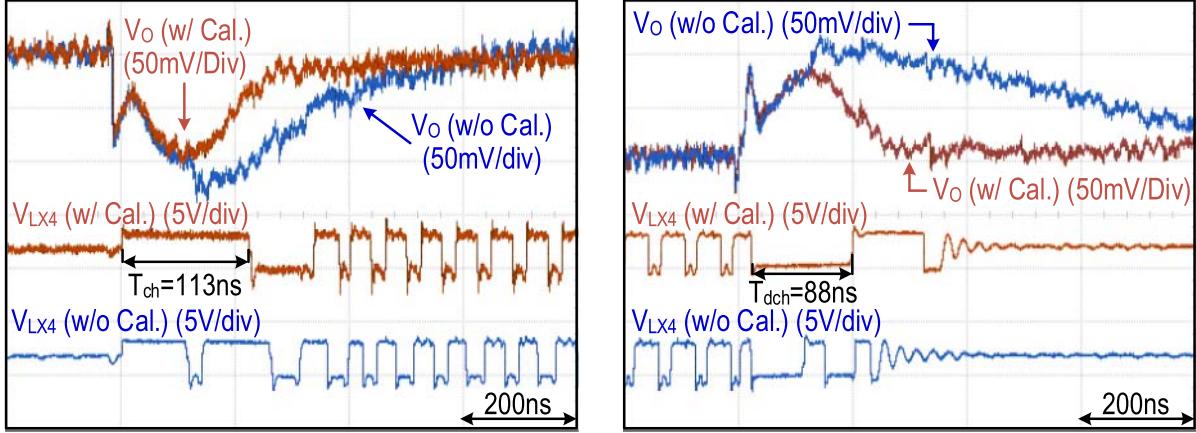


Fig. 19. Measured load-transient responses with and without CCS calibration, in which the LTO is enabled in both cases.

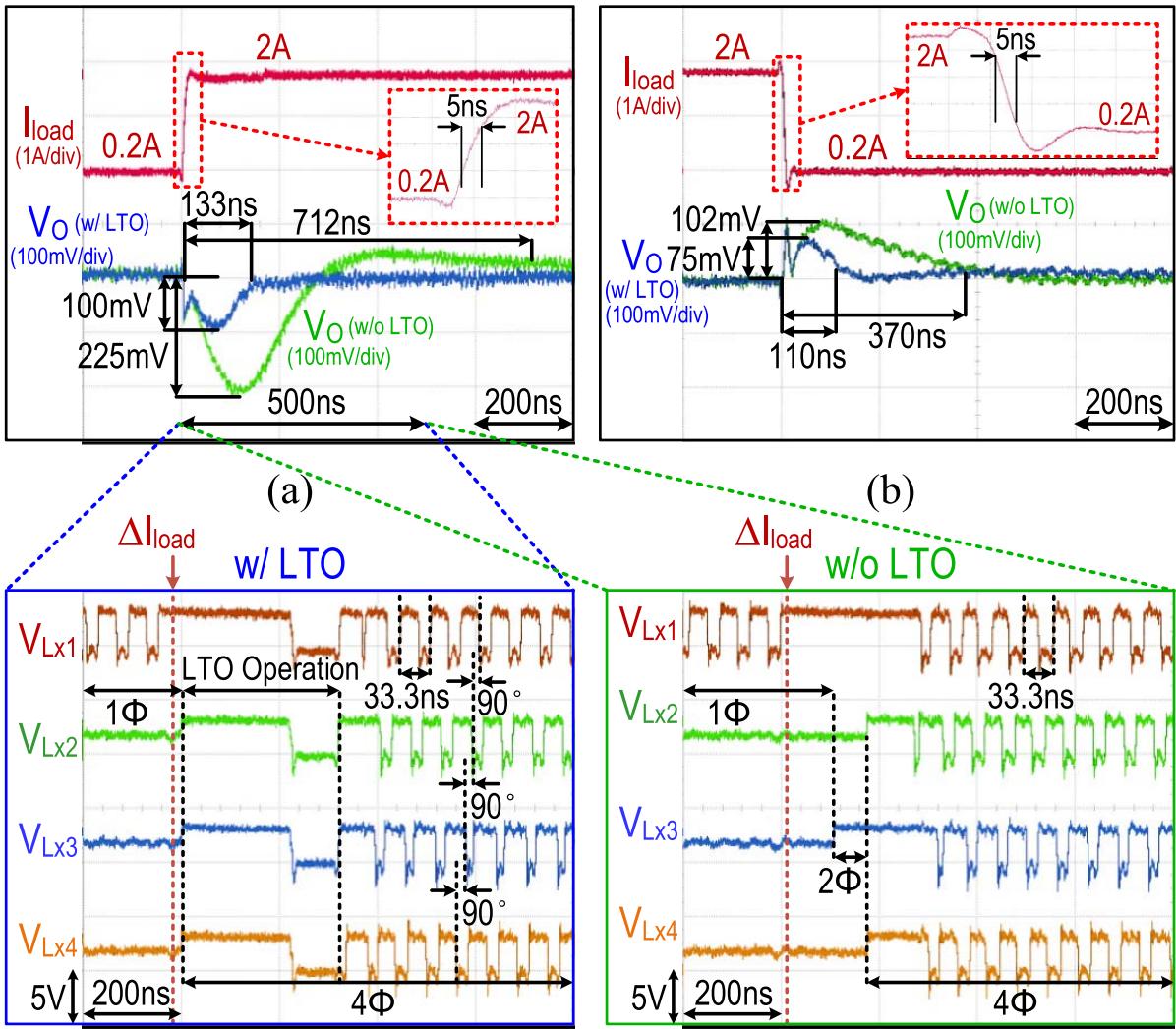


Fig. 20. Measured load-transient responses with and without LTO against (a) step-up  $\Delta I_{\text{load}}$  and (b) step-down  $\Delta I_{\text{load}}$ , in which the APC controller is enabled in both cases.

is closer to its theoretical minimum while the  $t_S$  is comparable to that in Fig. 20(a) with the APC controller enabled. The measured  $\Delta V_{\text{US}}$  is smaller due to the elimination of the circuit delay for enabling  $\Phi_{2-4}$  in the APC implementation described in this paper. Fig. 21(b) shows the measured load-transient

response against a step-down  $\Delta I_{\text{load}}/\Delta t_{\text{load}} = -1.8 \text{ A}/5 \text{ ns}$  with the APC controller disabled.

Figs. 22–24 show the measured load-transient responses under  $V_O = 1 \text{ V}$  and  $\Delta I_{\text{load}}/\Delta t_{\text{load}} = 1.8 \text{ A}/5 \text{ ns}$ . Fig. 22(a) and (b) shows the measured results without and with

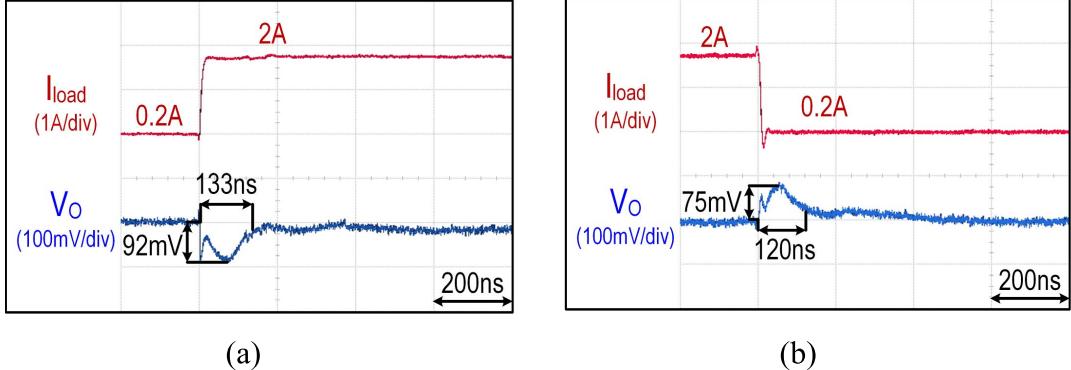


Fig. 21. Measured load-transient responses against a (a) step-up  $\Delta I_{load}$  and (b) step-down  $\Delta I_{load}$  with the APC controller disabled.

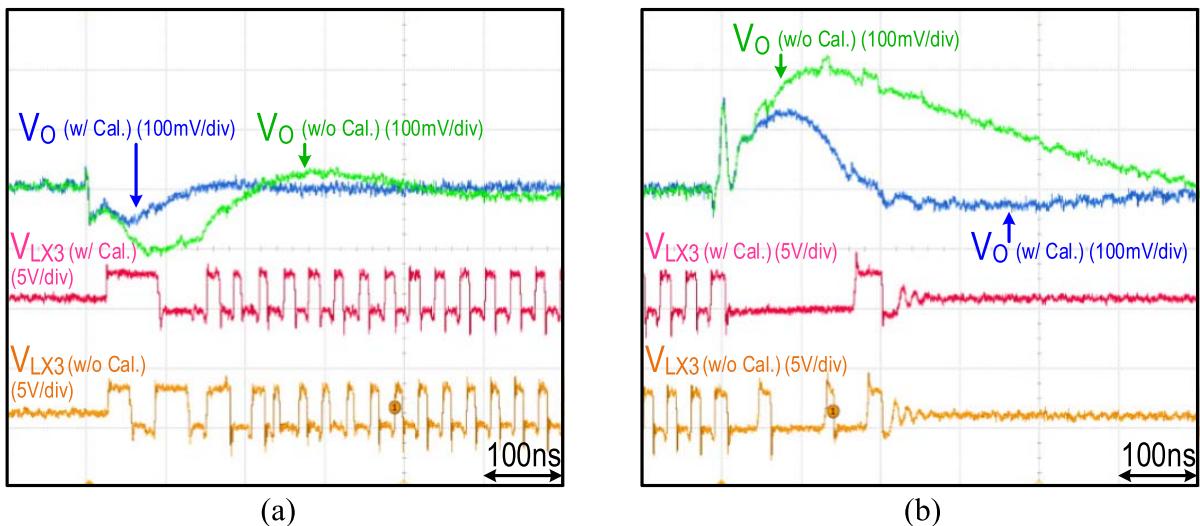


Fig. 22. Measured load-transient responses under  $V_O = 1$  V without and with CCS calibration against a (a) step-up  $\Delta I_{load}$  and (b) step-down  $\Delta I_{load}$ , in which the LTO is enabled in both cases.

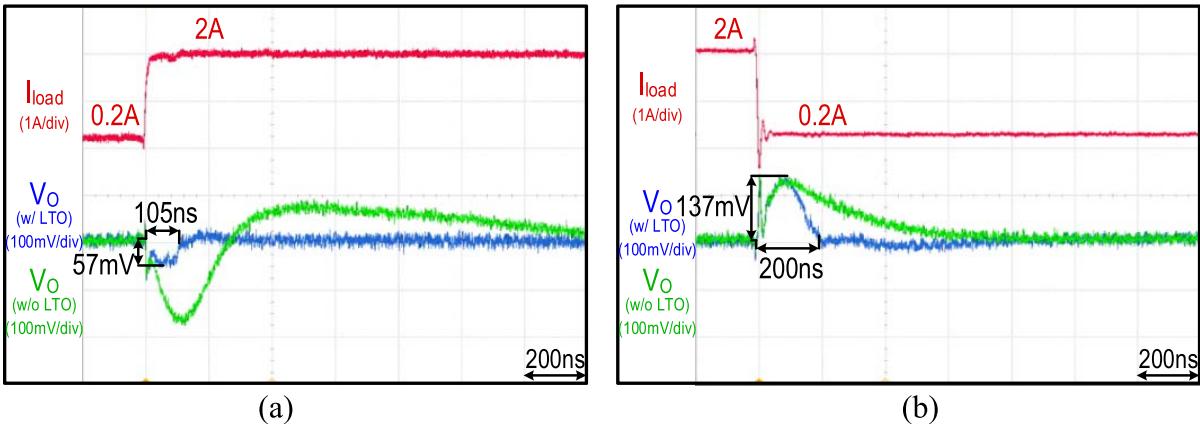


Fig. 23. Measured load-transient responses under  $V_O = 1$  V with and without LTO against a (a) step-up  $\Delta I_{load}$  and (b) step-down  $\Delta I_{load}$ , in which the APC controller is enabled in both cases.

CCS calibration against the respective step-up and step-down  $\Delta I_{load}$ , in which the LTO is enabled in both cases. Fig. 23(a) and (b) show the measure results with and without LTO against the respective step-up and step-down  $\Delta I_{load}$ , in which the APC controller is enabled in both cases. In Fig. 23(a), the measured  $\Delta V_{US} = 57$  mV and  $t_S = 105$  ns, which are near their respective theoretical minima of  $\Delta V_{US,min} = 55.2$  mV and  $t_{S,min} = 90.4$  ns. In Fig. 23(b), the measured

$\Delta V_{OS} = 137$  mV and  $t_S = 200$  ns, which also approach their respective theoretical minima of  $\Delta V_{OS,min} = 136.5$  mV and  $t_{S,min} = 197.3$  ns. Fig. 24(a) and (b) shows the measured results against the respective step-up and step-down  $\Delta I_{load}$  with the APC controller disabled.

Fig. 25 shows the measured efficiency  $\eta$  under different  $I_{load}$ . As seen, the APC controller leads to high efficiencies over a wide load range. For  $V_O = 1.8$  V, the measured

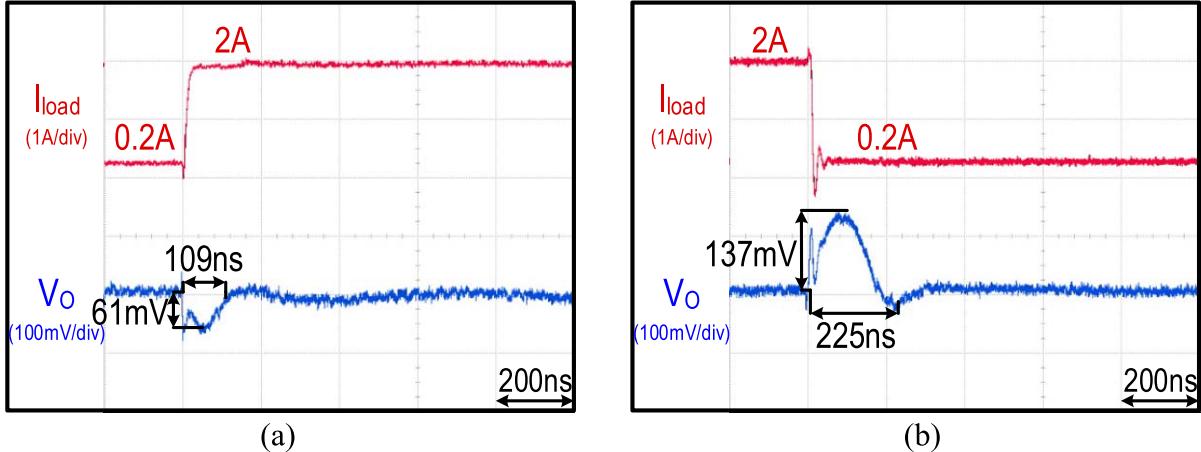


Fig. 24. Measured load-transient responses under  $V_O = 1$  V against a (a) step-up  $\Delta I_{load}$  and (b) step-down  $\Delta I_{load}$  with the APC controller disabled.

TABLE I  
MEASURED LOAD-TRANSIENT RESPONSES WITH DIFFERENT OUTPUT CAPACITORS

Output Capacitor	Nominal $C_O$ (nF)	Light-to-Heavy $\Delta I_{load}$ ( $1\Phi \rightarrow 4\Phi$ )			Heavy-to-Light $\Delta I_{load}$ ( $4\Phi \rightarrow 1\Phi$ )				
		Theoretical	Measured		Theoretical	Measured			
		$T_{ch}$ (ns)	$T_{ch}$ (ns)	$\Delta V_{US}$ (mV)	$t_s$ (ns)	$T_{dch}$ (ns)	$T_{dch}$ (ns)		
A	440	113	110	147	143	90	84	100	110
B	470		113	112	140		85	107	125
C	660		113	100	133		88	81	113
D	680		109	88	162		82	63	150

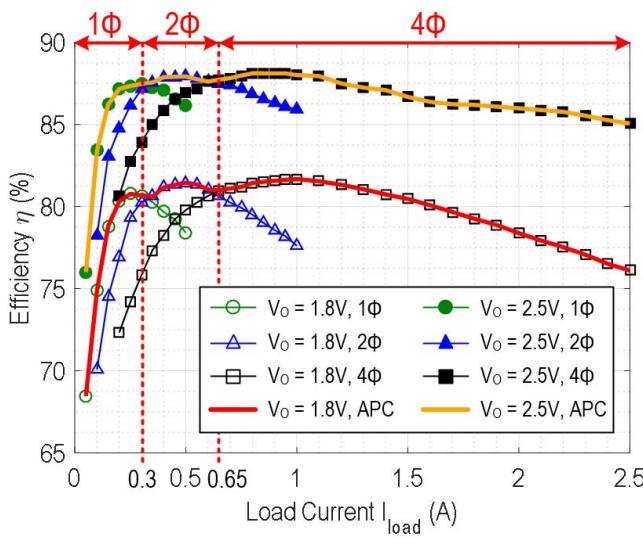


Fig. 25. Measured efficiency under different  $I_{load}$ .

peak efficiency  $\eta_{pk} = 81.7\%$  at  $I_{load} = 1$  A, while for  $V_O = 2.5$  V, the measured  $\eta_{pk} = 88.1\%$  at  $I_{load} = 900$  mA. Fig. 26 shows the simulated breakdown of quiescent current, where the total quiescent current consumption is 3.49 mA.

Table I lists the measured load-transient responses with different output capacitors, in which the measured  $T_{ch}$  and  $T_{dch}$  are all close to their theoretical values.

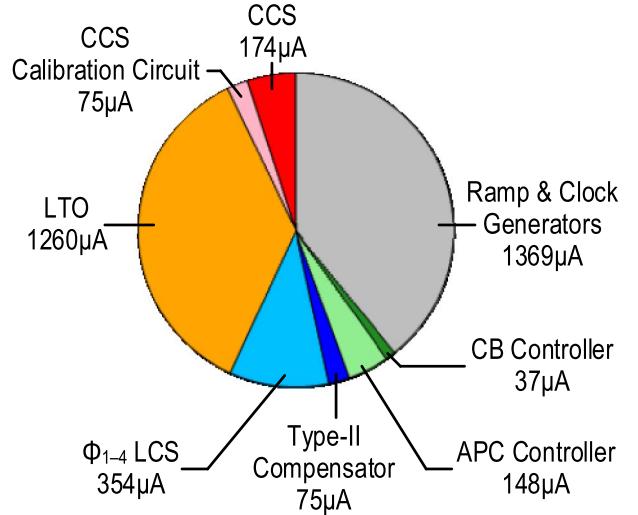


Fig. 26. Simulated breakdown of quiescent current.

Table II presents a performance comparison with other state-of-the-art multiphase buck converters. In [5]–[7], the theoretical minima of the  $\Delta V_{US}$ ,  $\Delta V_{OS}$ , and  $t_s$  are not available since  $\Delta I_{load}/\Delta t_{load} < \Delta I_{Lo}/\Delta t$ . Compared with other state-of-the-art multiphase buck converters, both the measured  $\Delta V_{US}$  ( $\Delta V_{OS}$ ) and  $t_s$  in this paper are the closest to their corresponding theoretical minima.

TABLE II  
PERFORMANCE COMPARISON WITH OTHER STATE-OF-THE-ART MULTIPHASE BUCK CONVERTERS

		ISSCC 2014 [5]	JSSC 2013 [6]	JSSC 2009 [7]	ISSCC 2017 [8]	This Work
Process ( $\mu\text{m}$ )		0.25	0.13	0.5	0.35	0.18
# of Phases, N		3	4	4	4	4
$f_{\text{SW}}$ (MHz)		0.5	100	32–35	25	30
$V_{\text{IN}}$ (V)		2.8–5.5	1.2	4–5	3.3	3.3
$V_{\text{O}}$ (V)		0.2–3.3	0.6–1.05	0.86–3.93	0.3–2.5	0.7–3.0
$L_{\text{O}}$ (nH)		2200	6	110	200	220
$C_{\text{O}}$ (nF)		66000	1.87	187	2470	620
$I_{\text{load(max)}}$ (A)		9	1.2	1	6	2.5
Light-to-Heavy Load-Transient Response	$V_{\text{IN}}$ (V)	5	1.2	4.9	3.3	3.3
	$V_{\text{O}}$ (V)	1.5	0.9	3.3	1.6	1.8
	$\Delta I_{\text{load}} / \Delta t_{\text{load}}$ (A/ns)	8 / 20000	0.18 / 800	<sup>(a)</sup> 0.3 / 30	4 / 5	1.8 / 5
	$\Delta I_{\text{Lo}} / \Delta t$ (A/ns)	0.0048	0.2	0.058	0.034	0.027
	$\Delta V_{\text{US}} / \Delta V_{\text{US,min}}$ (mV)	40 / – (1Φ → 3Φ)	60 / – (1Φ → 4Φ)	<sup>(b)</sup> 180 / – (4Φ → 4Φ)	103 / 91.2 = 1.13 (1Φ → 4Φ)	100 / 89 = 1.12 (1Φ → 4Φ) 92 / 89 = 1.03 (4Φ → 4Φ)
	$t_{\text{S}} / t_{\text{S,min}}$ (ns)	40000 / – (1Φ → 3Φ)	<sup>(b)</sup> 2000 / – (1Φ → 4Φ)	<sup>(b)</sup> 350 / – (4Φ → 4Φ)	190 / <sup>(d)</sup> – (1Φ → 4Φ)	133 / 126 = 1.06 (1Φ → 4Φ) 133 / 126 = 1.06 (4Φ → 4Φ)
Heavy-to-Light Load-Transient Response	$V_{\text{IN}}$ (V)	5	1.2	4.9	3.3	3.3
	$V_{\text{O}}$ (V)	1.5	0.9	3.3	1.6	1.8
	$\Delta I_{\text{load}} / \Delta t_{\text{load}}$ (A/ns)	8 / 20000	0.18 / 800	<sup>(a)</sup> 0.3 / 10	4 / 5	1.8 / 5
	$\Delta I_{\text{Lo}} / \Delta t$ (A/ns)	0.002	0.6	0.12	0.032	0.0328
	$\Delta V_{\text{OS}} / \Delta V_{\text{OS,min}}$ (mV)	40 / – (3Φ → 1Φ)	40 / – (4Φ → 1Φ)	<sup>(b)</sup> 180 / – (4Φ → 4Φ)	123 / 97.2 = 1.27 (4Φ → 1Φ)	75 / 73 = 1.03 (4Φ → 1Φ) 75 / 73 = 1.03 (4Φ → 4Φ)
	$t_{\text{S}} / t_{\text{S,min}}$ (ns)	40000 / – (3Φ → 1Φ)	<sup>(b)</sup> 2000 / – (4Φ → 1Φ)	<sup>(b)</sup> 450 / – (4Φ → 4Φ)	237 / <sup>(d)</sup> – (4Φ → 1Φ)	110 / 104 = 1.06 (4Φ → 1Φ) 120 / 104 = 1.15 (4Φ → 4Φ)
Peak Efficiency $\eta_{\text{pk}}$ (%)		90.2 ( $V_{\text{IN}} = 5\text{V}$ , $V_{\text{O}} = 1.5\text{V}$ )	82.4 ( $V_{\text{IN}} = 1.2\text{V}$ , $V_{\text{O}} = 0.9\text{V}$ )	83 ( $V_{\text{IN}} = 4.8\text{V}$ , $V_{\text{O}} = 3.3\text{V}$ )	88.1 ( $V_{\text{IN}} = 3.3\text{V}$ , $V_{\text{O}} = 2.5\text{V}$ )	88.1 ( $V_{\text{IN}} = 3.3\text{V}$ , $V_{\text{O}} = 2.5\text{V}$ ) 81.7 ( $V_{\text{IN}} = 3.3\text{V}$ , $V_{\text{O}} = 1.8\text{V}$ )
Chip Area (mm <sup>2</sup> )		6.25	<sup>(c)</sup> 1.76	3.3	1.88	1.93

(a) No measured waveforms provided. (b) Estimated from the measured waveforms. (c) Estimated without on-chip output capacitor.

(d)  $t_{\text{S,min}}$  cannot be derived since  $V_{\text{O}}$  does not settle within  $\pm 1\%$  of its steady-state value before the load transient.

## VII. CONCLUSION

CCS calibration and LTO techniques are proposed and implemented in a four-phase buck converter to optimize the load-transient response for theoretically minimal output-voltage undershoot  $\Delta V_{\text{US}}$ , overshoot  $\Delta V_{\text{OS}}$ , and settling time  $t_{\text{S}}$  despite variations in the output-capacitor's

impedance  $Z_{\text{Co}}$ . Compared with other state-of-the-arts, the proposed techniques can achieve the fastest load-transient response with  $\Delta V_{\text{US}}$ ,  $\Delta V_{\text{OS}}$ , and  $t_{\text{S}}$  the closest to their respective theoretical limits. For the next-generation high-speed converter designs in more advanced process nodes, smaller theoretically minimal  $\Delta V_{\text{US}}$ ,  $\Delta V_{\text{OS}}$ , and  $t_{\text{S}}$  could

be feasibly obtained. The proposed buck converter can also be connected in parallel with a low-dropout regulator to further reduce  $\Delta V_{US}$  and shorten  $t_S$ ; however, this could cause degraded efficiency if large and rapid  $\Delta I_{load}$  occur frequently. Furthermore, the proposed CCS calibration and LTO can be integrated with other techniques to optimize both the load-transient and reference-tracking responses for single-phase and multiphase dc–dc converters.

#### ACKNOWLEDGMENT

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**Yi-Wei Huang** (S'14) was born in Taipei, Taiwan, in 1988. He received the B.S. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 2010, where he is currently pursuing the Ph.D. degree.

His current research interests include power management, light energy harvesting, and wireless power transmission ICs.

Mr. Huang is an Honorary Member of the Phi Tau Phi Scholastic Honor Society, Taiwan.



**Tai-Haur Kuo** (S'87–M'90–SM'16) was born in Tainan, Taiwan, in 1960. He received the B.S. degree in electrical engineering from National Cheng Kung University (NCKU), Tainan, in 1982, and the M.S. and Ph.D. degrees in electrical engineering from the University of Maryland, College Park, MD, USA, in 1988 and 1990, respectively.

In 1982, he was a Military Police Officer; then, he was elevated to 2nd lieutenant, and finally promoted to the Military Police Captain of the Taipei Train Station, Taipei, Taiwan. From 1984 to 1986, he was an Analog Integrated Circuit (IC) Designer with the Industrial Technology and Research Institute (ITRI), Hsinchu, Taiwan. In 1989, he joined the Aerospace Technology Center of Allied-Signal, Columbia, MD, USA, where he conducted research on the design of monolithic ultrahigh-speed RTD-HEMT ICs. From 1990 to 1992, he was a Design Engineer with Integrated Device Technology, Santa Clara, CA, USA. He was a Project Manager with ITRI. In 2004, he joined Advanic Technologies, Tainan, as the President. In 2005, he joined Elite Semiconductor Memory Technology, Hsinchu, as a Vice President. He joined the Board of Directors at ChipMOS Technology in 2012, and in 2016, he joined Holtek Semiconductor, Zilltek Technology, and Taiwan IC Industry & Academia Research Alliance, which are all in Hsinchu. Since 1992, he has been with the Department of Electrical Engineering, NCKU, where he became a Professor in 1997, and is currently a Distinguished Professor. He currently holds 41 patents. His current research interests include data converters, delta-sigma modulators, class-D audio amplifiers, energy harvesting, and power management ICs.

Dr. Kuo received the Annual Personal Special Contribution Award from ITRI in 1986, the Outstanding Teaching Excellence Award from NCKU in 2012, the Outstanding Industry-Academy Cooperation Achievement Award from NCKU in 2012, the Technical Achievement Award, the Himax Award from the IEEE Tainan Section in 2015 and 2016, and the Outstanding Technology Transfer Award from the Ministry of Science and Technology of Taiwan in 2016. He was a co-recipient of four annual best analog IC-design awards from the Chip Implementation Center of Taiwan. He is with the Technical Program Committee of the IEEE International Solid-State Circuits Conference. He is also a Guest Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS.



**Szu-Yu Huang** (S'13) was born in Kaohsiung, Taiwan, in 1989. She received the B.S. and M.S. degrees in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 2012 and 2015, respectively.

Since 2016, she has been a Design Engineer with RichTek Corporation, Hsinchu, Taiwan. Her current research interests include power management ICs.

Ms. Huang is an Honorary Member of the Phi Tau Phi Scholastic Honor Society, Taiwan. She was a co-recipient of the annual best analog IC-design award from the Chip Implementation Center of Taiwan in 2014.



**Kuan-Yu Fang** was born in Tainan, Taiwan, in 1991. He received the B.S. and M.S. degrees in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 2013 and 2016, respectively.

Since 2016, he has been a Design Engineer with MediaTek Inc., Hsinchu, Taiwan. His current research interests include power management ICs.