IEEE JOURNAL OF

SOLID-STATE CIRCUITS

A PUBLICATION OF THE IEEE SOLID-STATE CIRCUITS SOCIETY



MARCH 2018 VOLUME 53 NUMBER 3 IJSCBC (ISSN 0018-9200)

SPECIAL SECTION ON THE 2017 IEEE CUSTOM INTEGRATED CIRCUITS CONFERENCE

EDITORIAL Guest Editorial 2017 IEEE Custom Integrated Circuits Conference
Guest Editorial 2017 IEEE Custom Integrated Circuits Conference
SPECIAL SECTION PAPERS
A Digital Filtering ADC With Programmable Blocker Cancellation for Wireless Receivers
Q. Wang, H. Shibata, A. Liscidini, and A. C. Carusone 68
A Quick Startup Technique for High-Q Oscillators Using Precisely Timed Energy Injection
A Low-Jitter Ring-Oscillator Phase-Locked Loop Using Feedforward Noise Cancellation With a Sub-Sampling Phase
Detector
A 2.4-GHz 16-Phase Sub-Sampling Fractional-N PLL With Robust Soft Loop Switching
An Area-Efficient Microprocessor-Based SoC With an Instruction-Cache Transformable to an Ambient Temperature
Sensor and a Physically Unclonable Function
A Reconfigurable Vernier Time-to-Digital Converter With 2-D Spiral Comparator Array and Second-Order
$\Delta \Sigma$ Linearization
On-Chip Jitter Measurement Using Jitter Injection in a 28 Gb/s PI-Based CDR
J. Liang, A. Sheikholeslami, H. Tamura, and H. Yamaguchi 75
A Broadband Class-AB Power Amplifier With Instantaneous Supply-Switching Efficiency Enhancement for Cable TV
Application
Channel-Adaptive ADC and TDC for 28 Gb/s PAM-4 Digital Receiver
A Chicago May 200 May 500 May
A 6-bit 0.81-mW 700-MS/s SAR ADC With Sparkle-Code Correction, Resolution Enhancement, and Background
Window Width Calibration Y. Yoon and N. Sun 78
A 50 MHz BW 76.1 dB DR Two-Stage Continuous-Time Delta–Sigma Modulator With VCO Quantizer Nonlinearity Cancellation
Cancellation
PWM/PFM Modes S I Kim W-S Choi R Pilawa-Podgurski and P K Hanumolu 81.

(Contents Continued on Back Cover)



REGULAR PAPERS	
An Injection Frequency-Locked Loop—Autonomous Injection Frequency Tracking Loop With Phase Noise	
Self-Calibration for Power-Efficient mm-Wave Signal Sources	825
A 9-bit 215 MS/s Folding-Flash Time-to-Digital Converter Based on Redundant Remainder Number System in	
45-nm CMOS	839
A Two-Way Interleaved 7-b 2.4-GS/s 1-Then-2 b/Cycle SAR ADC With Background Offset Calibration	
	850
An Eight-Lane 7-Gb/s/pin Source Synchronous Single-Ended RX With Equalization and Far-End Crosstalk	
Cancellation for Backplane Channels	
P. A. Francese, C. Menolfi, M. Braendli, M. Kossel, T. Morf, L. Kull, I. Oezkaya, Y. Leblebici, V. Cevher, and T. Toifl	861
A 10-Gb/s/ch, 0.6-pJ/bit/mm Power Scalable Rapid-ON/OFF Transceiver for On-Chip Energy Proportional	
Interconnects	873
A 0.45-0.7 V 1-6 Gb/s 0.29-0.58 pJ/b Source-Synchronous Transceiver Using Near-Threshold Operation	
WS. Choi, G. Shu, M. Talegaonkar, Y. Liu, D. Wei, L. Benini, and P. K. Hanumolu	884
A 1-V 0.25-μW Inverter Stacking Amplifier With 1.07 Noise Efficiency Factor L. Shen, N. Lu, and N. Sun	896
A 0.8-V Resistor-Based Temperature Sensor in 65-nm CMOS With Supply Sensitivity of 0.28 °C/V	
	906
An Auto-Zero-Voltage-Switching Quasi-Resonant LED Driver With GaN FETs and Fully Integrated LED Shunt	
Protectors	913
Quasi-Resonant Clocking: Continuous Voltage-Frequency Scalable Resonant Clocking System for Dynamic	
Voltage-Frequency Scaling Systems F. ur Rahman and V. Sathe	924
A 9-mm ² Ultra-Low-Power Highly Integrated 28-nm CMOS SoC for Internet of Things	
G. Samson, D. Park, K. Easton, R. Beraha, A. Newham, M. Lin, V. Rangan, K. Chatha, D. Butterfield, and R. Attar	936
80-kb Logic Embedded High-K Charge Trap Transistor-Based Multi-Time-Programmable Memory With No Added	
Process Complexity B. Jayaraman, D. Leu, J. Viraraghavan,	
A. Cestero, M. Yin, J. Golz, R. R. Tummuru, R. Raghavan, D. Moy, T. Kempanna, F. Khan, T. Kirihata, and S. S. Iyer	949