

A Wideband Receiver Employing PWM-Based Harmonic Rejection Downconversion

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Abstract—A harmonic rejection (HR) receiver that utilizes discrete-level pulsedwidth modulation (PWM) to implement a sinusoidal local oscillator (LO) with intrinsic HR is demonstrated. The PWM-LO is employed in a switching mixer. The receiver can be configured to provide additional HR, by employing multi-phase paths, with appropriate baseband gain coefficients. The PWM generator employs parallel delay-locked loops to implement a three-level natural-sampling dual-edge PWM sinusoidal LO signal, with rejection of the third, fifth, and seventh LO harmonics. Gain control using LO-path pulsedwidth control is demonstrated. The design is implemented in a 40-nm CMOS process. The receiver gain with HR is 26.4–30.1 dB in multi-phase LO configuration and 28–31.8 dB in single-phase configuration. The double-sideband noise figure at peak gain is 5.8 dB. The design demonstrates worst case HR3 and HR5 ratios of 47 and 49 dB without calibration for $f_{LO} = 100$ MHz in the multi-phase configuration, with a total power dissipation of 41.1 mW. With calibration, a single-phase peak harmonic rejection ratio (HRR) higher than 73 dB for the third, fifth, and seventh LO harmonics is demonstrated. Gain dependence of the HRR is studied.

Index Terms—Calibration, harmonic rejection (HR), pulsedwidth modulation (PWM), variable gain, wideband receiver.

I. INTRODUCTION

ROADBAND radio receivers are required in several applications, such as multi-standard cellular front ends, cable-modem receivers, and cognitive radio systems [1], [2]. Harmonic rejection (HR) is a critical requirement in the design of receivers for such systems, to ensure that energy near the harmonics of the local oscillator (LO) does not translate to baseband, along with the desired signal.

The degradation caused by harmonic response can be mitigated by using filters that allow only the signal band through, while attenuating energy near the LO harmonics (see [3], [4]). An active filter may also be used for this purpose [5]. The use of passive filter components can imply an area and cost

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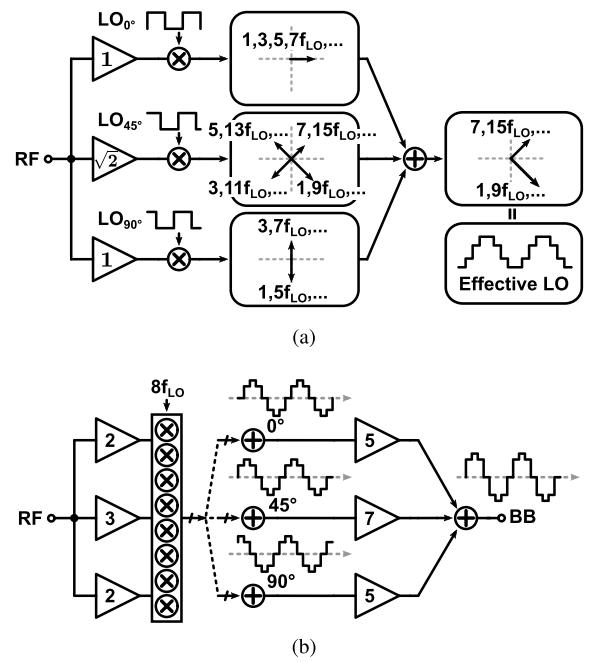


Fig. 1. Conventional HRM architecture. (a) Single-stage HRM. (b) Two-stage HRM.

penalty, while the use of active filters can lead to power and dynamic range degradation.

HR mixers (HRMs) described in [6]–[8], utilize a discrete-level approximation to a sine wave to minimize the harmonic response, while retaining the advantage of amplitude limiting on the LO port, similar to classical switching mixers. Such approaches typically employ a square wave, or a rectangular basis function and synthesize a discrete sinusoid by combining these basis functions with appropriate gain and phase shifts. For example, a frequently employed technique for implementing HRMs utilizes three periodic pulse waveforms with phase shifts of 0°:45°:90°, with respective gain scaling ratios of 1: $\sqrt{2}$:1 applied at RF or baseband, in order to approximate a discrete sinusoidal LO (see [6], [9], [10]). The approach with a one stage of scaled gain coefficients (see [6], Fig. 1(a)) is termed a single-stage HRM.

The ideal gain ratio of 1: $\sqrt{2}$:1 cannot be achieved in practice and is often approximated by integer ratios, such as 2:3:2 or 5:7:5, which introduces a gain error, and limits the achievable rejection. Combined with mismatch errors,

practically achievable HR ratio (HRR) in single-stage HRMs is limited to approximately 30–35 dB.

Two-stage HRMs ([9], Fig. 1(b)), synthesize discrete sinusoidal basis functions using single-stage HRMs, of the type above, and then use these discrete sinusoidal functions in yet another HRM stage, with phase shifts and appropriate gain scaling. If the first-order HRM reduces the harmonic levels present in the rectangular LO basis function by a factor α , then the second-stage HRM, further attenuates the harmonic levels by a similar factor, to achieve a net two-stage HRR of the order of α^2 . In addition to gain error, clock phase errors can also degrade HRR. The use of clock retiming in a single-stage HRM was proposed in [10] to solve the problem of clock phase error. The use of two-stage HR with clock retiming was shown in [11] with a measured HRR of approximately 70 dB.

Two-stage HRMs can provide excellent HR that is robust to process, voltage and temperature variations, but require increased complexity in the signal path because of the use multiple gains in the first and second stages, as shown in Fig. 1(b). Furthermore, additional amplifiers that are required to merge the outputs of the first stage increase power consumption. The complexity and power overhead increase significantly with the number of rejected harmonics.

In this paper, a single-stage HR wideband receiver is demonstrated, wherein a pulselength modulation (PWM) signal is used to represent a sinusoidal LO [12]. Since discrete-level PWM is employed, the LO can be directly applied to a switching mixer for frequency translating the input.

An often employed technique to generate a PWM signal is to compare an input signal to a ramp (see [13]). This approach is not well suited for the PWM-LO generation, because it would require a linear ramp operating at multi-GHz rate, and a fast and accurate analog comparator. Phase-locked loop-based PWM generation avoids the requirement for a ramp signal and an analog comparator [14], [15]. The LO signals required here are difficult to generate using this approach because of very high loop gain-bandwidth requirement. A key challenge in using these approaches is also the requirement for an adequately pure sinusoidal input signal.

A PWM-LO generator, which does not require a ramp or sinusoidal input signal, a high-speed analog comparator or have high loop gain-bandwidth requirement is proposed here. Section II explains the principle of the PWM-LO. Section III describes the circuit implementation. Section IV analyzes the noise performance of the proposed receiver. Section V discusses the measurement results and the conclusion follows in Section VI.

II. HARMONIC REJECTION WITH PWM

A sinusoidal LO signal can be represented by a PWM signal, as shown in Fig. 2. In this approach, the amplitude information of the sinusoidal LO signal is encoded in the duty cycle of a high-frequency rectangular pulse waveform with periodicity of f_{PWM} . The PWM signal can be represented by

$$y_{\text{PWM}}(t) = v_{\text{IN}}(t) + D(t) + H(t, f_{\text{PWM}}, v_{\text{IN}}) \quad (1)$$

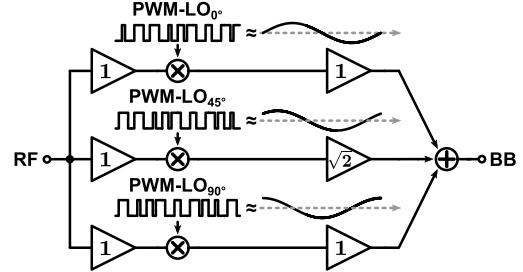


Fig. 2. Concept of the proposed HRM generator.

TABLE I
HRR WITH f_{PWM} ($V_{\text{LO}} = 0.8$)

f_{PWM}	HRR (dB)						
	3 rd	5 th	7 th	9 th	11 th	13 th	15 th
$4f_{\text{LO}}$	36	15	8	8	11	16	16
$6f_{\text{LO}}$	97	64	36	15	8	8	15
$8f_{\text{LO}}$	>100	>100	97	64	36	15	8
$10f_{\text{LO}}$	>100	>100	>100	>100	97	64	36

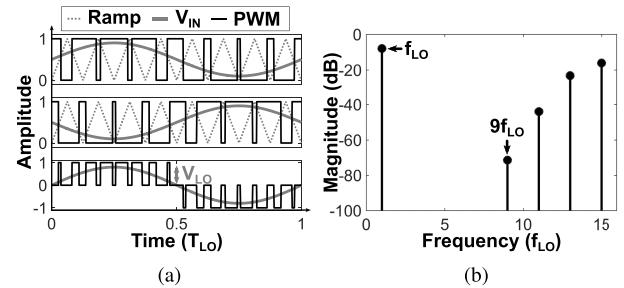


Fig. 3. Differential three-level NDE-PWM. (a) Waveform. (b) Spectrum.

where v_{IN} , D , and H are the input signal, distortion, and harmonics, respectively. Ideally, for a sinusoidal LO, the distortion and harmonics must be zero. This is made possible through the use of baseband natural-sampling PWM. If the PWM frequency, f_{PWM} , is sufficiently high, close-in harmonics of the LO signal can be suppressed in this representation. On the other hand, generating and controlling the PWM signal becomes increasingly challenging as f_{PWM} is increased.

Natural-sampling PWM can be implemented by modulating either one edge of the pulse train or both edges. For a given f_{PWM} , natural-sampling dual-edge PWM (NDE-PWM) has better harmonic response than natural-sampling trailing-edge PWM (NTE-PWM) [16]. This design employs $f_{\text{PWM}} = 8f_{\text{LO}}$ for NDE-PWM, as discussed below. For this case, NDE-PWM ideally rejects the odd harmonics of the LO signal below f_{PWM} , when f_{PWM} is eight times of LO frequency, f_{LO} (Table I). The even harmonics can be rejected by employing differential signaling [16]. As shown in Fig. 3(a), two NDE-PWM signals that are generated from two out-of-phase sinusoids can be used to generate a differential PWM-LO signal with three-level output (−1/0/1). This is called three-level

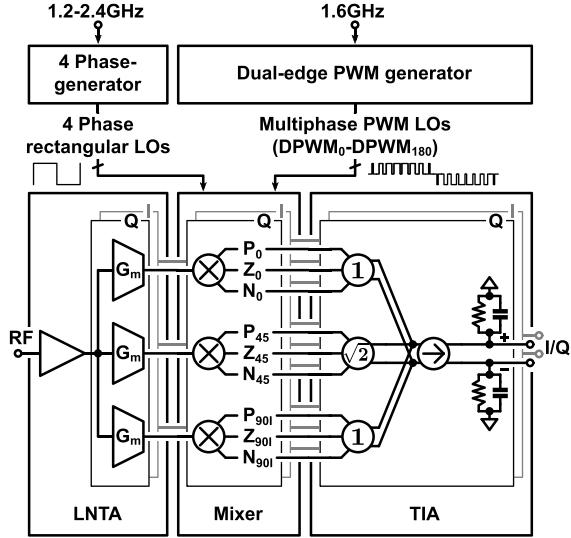


Fig. 4. Block diagram of the wideband receiver employing PWM.

NDE-PWM and it can be expressed as [17]

$$\begin{aligned} \text{LO}_{\text{PWM}}(t) &= V_{\text{LO}} \sin(2\pi f_{\text{LO}} t) \\ &+ \sum_{m=1}^{\infty} \left(\frac{4}{m\pi} \cos\left(\frac{m\pi}{2}\right) \right) \\ &\times \sum_{n=\pm 1, 3, \dots}^{\infty} \left(J_n\left(\frac{m\pi V_{\text{LO}}}{2}\right) \sin(2\pi(mf_{\text{PWM}} + nf_{\text{LO}})t) \right) \end{aligned} \quad (2)$$

where V_{LO} is the amplitude of LO signal expressed as a fraction of V_{DD} .

As can be seen from the above equation, the waveform has no direct components at harmonics of f_{LO} . On the other hand, the third, fifth, and seventh harmonics arise from $n = 13$, $n = 11$ and $n = 9$ for $m = 2$, respectively. The amplitudes of these components are negligible owing to the high order of the corresponding Bessel coefficient (Fig. 3(b)).

Three signal paths are shown in Fig. 2, with mutual phase shifts of 45° , however, the design can be configured such that the three paths have no relative phase shift, and are essentially in parallel. The design is said to be in multiphase configuration or single-phase configuration, depending on whether the mutual path-to-path phase shifts are 45° or 0° , respectively.

III. CIRCUIT IMPLEMENTATION

Fig. 4 shows the proposed HR wideband receiver with a three-level PWM-LO. The design spans a band from 100 to 600 MHz. HR is employed from 100–200 MHz, to ensure that the third harmonic is out-of-band, while the LOs from 300 to 600 MHz employ conventional quadrature downconversion. In the 100–200-MHz band, the conventional 50% duty cycle rectangular clock is replaced by a three-level PWM representation of a sinusoidal LO to reject harmonics.

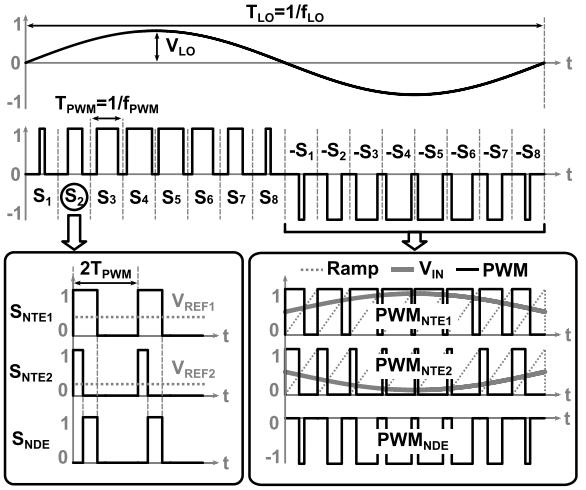


Fig. 5. Three-level NDE-PWM-based sinusoidal LO and its synthesis.

Sinusoidal PWM-LOs with HR are applied in three paths as shown in Fig. 4. By introducing a mutual 45° phase shift between the three PWM-LOs in combination with gain ratios of $1:\sqrt{2}:1$ at baseband, additional HR can be achieved. This can be distinguished from a two-stage HRM, which employs scaled gain coefficients in the RF signal path to synthesize multi-phase sinusoidal LOs, which are then used in combination with a second stage of baseband gain coefficients. Thus, the receiver has a single-stage configuration in the RF signal path. The PWM-LO signal can also be used to perform gain control within the first downconverter through duty cycle control.

A. Dual-Edge PWM Generator

An open-loop PWM generator is designed to generate the NDE-PWM signals to allow for high-frequency LO generation. A sinusoidal period of the LO is uniformly sampled at 16 points in time, every $1/2f_{\text{PWM}}$ s. These 16 symbols are further reduced to eight symbols by exploiting the polarity of the pulses, as shown in Fig. 5. Each of the eight symbols is then converted to an NDE-PWM signal.

NDE-PWM is not symmetric with respect to the center position of a pulse and, hence, it is difficult to generate directly in a synchronous system. However, NDE-PWM can be implemented using two differential NTE-PWMs with twice the PWM frequency of NDE-PWM (Fig. 5), where each NTE-PWM signal is shown to be generated by comparing a sinusoid and an inverted sinusoid to a ramp edge. An NDE-PWM symbol can similarly be generated using two NTE-PWM symbols.

The design employs 16 delay-locked loop (DLL)-based NTE-PWM symbol generators (SGs) (Fig. 6), where each generator provides a left-edge referred PWM pulse, corresponding to a pre-determined DC level. Seven OR gates, that are controlled by a pulse trigger, merge these NDE-PWM symbols into a continuous pulse stream. The reference voltages for determining the NTE-PWM symbols are derived using a global reference voltage, V_{REF} , and a resistor ladder. In this

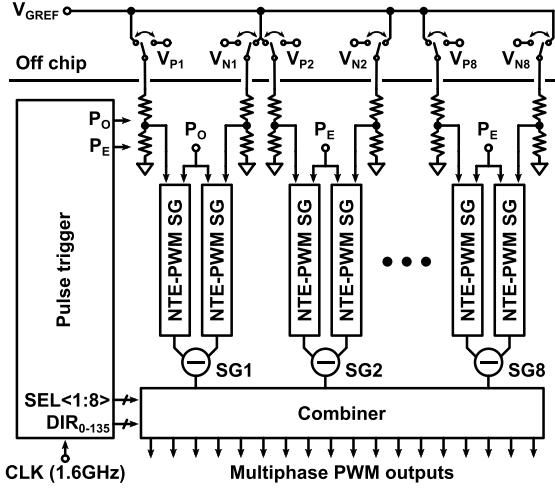


Fig. 6. Block diagram of the dual-edge PWM generator.

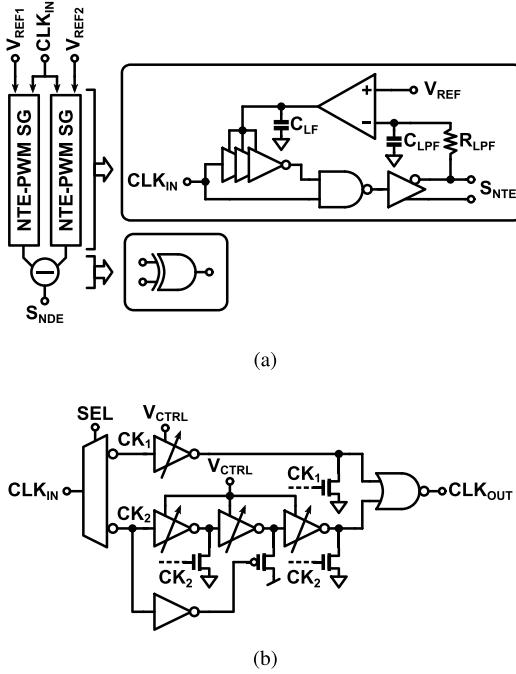


Fig. 7. SG. (a) NDE SG. (b) Delay line circuit.

design, the resistor ladder is designed for V_{LO} of 0.8 with a V_{GREF} of 709 mV.

1) *Symbol Generator*: Fig. 7(a) shows an NDE-PWM SG, which employs a pair of NTE-PWM SGs and an EXOR gate. In each NTE-PWM SG, a negative feedback loop is used in combination with a voltage-controlled delay line (VCDL) and operational transconductance amplifier (OTA) to adjust the duty cycle of the output pulse such that its average equals a pre-computed reference voltage (V_{REF}). Since the input voltage is at DC, the OTA bandwidth requirement is not critical. A folded cascode amplifier is adopted to achieve high output impedance in the OTA, which consumes 3.5 μ A. A starved current inverter whose delay is determined by the control voltage applied to a cascaded PMOS current source is used as a delay unit. Due to the widely varying pulselwidth as shown in Fig. 5, it is difficult to ensure sufficient delay range

with only analog control. Thus, coarse digital control is also employed in the delay line (Fig. 7(b)). Based on the delay value that is required, one of the two delay lines is employed. To generate a correct symbol every period, the delay line needs to adjust only the rising edge delay and be initialized before the next clock input signal arrives. Additional reset transistors are added to each output node of the delay line (Fig. 7(b)). These initialize each node when the delay line sees the falling edge of the input clock.

The open-loop transfer function of the NTE-PWM SG, $A_{Loop}(s)$, is given by

$$A_{Loop}(s) = \frac{G_m}{sC_{LF}} \frac{K_{DL}V_{DD}}{2\pi} \frac{1}{1 + \frac{s}{w_{LPF}}} \quad (3)$$

where G_m is transconductance of the OTA, K_{DL} is the VCDL gain in rad/s/V, V_{DD} is the supply voltage, and w_{LPF} is $1/(R_{LPF}C_{LPF})$. K_{DL} of an inverter type delay unit varies significantly with the applied control voltage. As K_{DL} increases, the loop-bandwidth approaches the pole of the lowpass filter (LPF) and thus the phase margin decreases. The phase margin for the worst case condition is simulated to be 37.8°, which is sufficient for the DC input to be locked.

2) *Pulse Trigger*: Fig. 8 shows the timing diagram for the generation of the PWM-LO at f_{LO} . The eight NDE-PWM symbols are assigned to individual NDE-PWM SGs (SG₁-SG₈ in Fig. 6). Multi-phase NDE-PWM signals employed in Fig. 2, are easily synthesized by changing the sequence of the symbols without an additional NDE-PWM SG. For example, if the NDE-PWM signal corresponding to 0° is started from S₁, the first symbol of the 45° NDE-PWM signal starts from S₃. For symbol resequencing, the required multi-phase NDE-PWM signals are 0°, 45°, 90°, and 135°. The NDE-PWM signals that are advanced by 180° in comparison, are implemented by changing the polarity of the differential LO outputs.

Each symbol is triggered by P_O and P_E signals that have a periodicity of $2T_{PWM}$ with a delay difference of T_{PWM} . In addition, P_O and P_E have a duty cycle of 75% instead of 50%. If a duty cycle of 50% is used for P_O and P_E , the pulselwidth of S_{NTE} in Fig. 7(a) can be distorted by the falling edges of these signals, when the required pulselwidth of S_{NTE} is comparable to this duty cycle. A duty cycle of 75% is implemented by combining the outputs of two dividers which are synchronized with the rising and falling edges of the master clock, CLK, as shown in Fig. 8(c).

SEL<1:8> signals in Fig. 8(a) sequentially select the eight NDE-PWM SGs. For example, the selection sequence for 0° PWM-LO of f_{LO} is [SG₁, SG₂, SG₃, SG₄, SG₅, SG₆, SG₇, SG₈], which corresponds to the symbol sequence of [S₁, S₂, S₃, S₄, S₅, S₆, S₇, S₈]. The selection sequence for 45° PWM-LO changes to [SG₃, SG₄, SG₅, SG₆, SG₇, SG₈, SG₁, SG₂] because the 45° PWM-LO is started from S₃. Thus the NDE-PWM SG corresponding to the selection signal is shifted by 2 according to the PWM-LO phase, as shown in Fig. 8(d).

The above selection operation must not disrupt the symbols, which can potentially occur when the time space between symbols is narrow. For example, the time space between

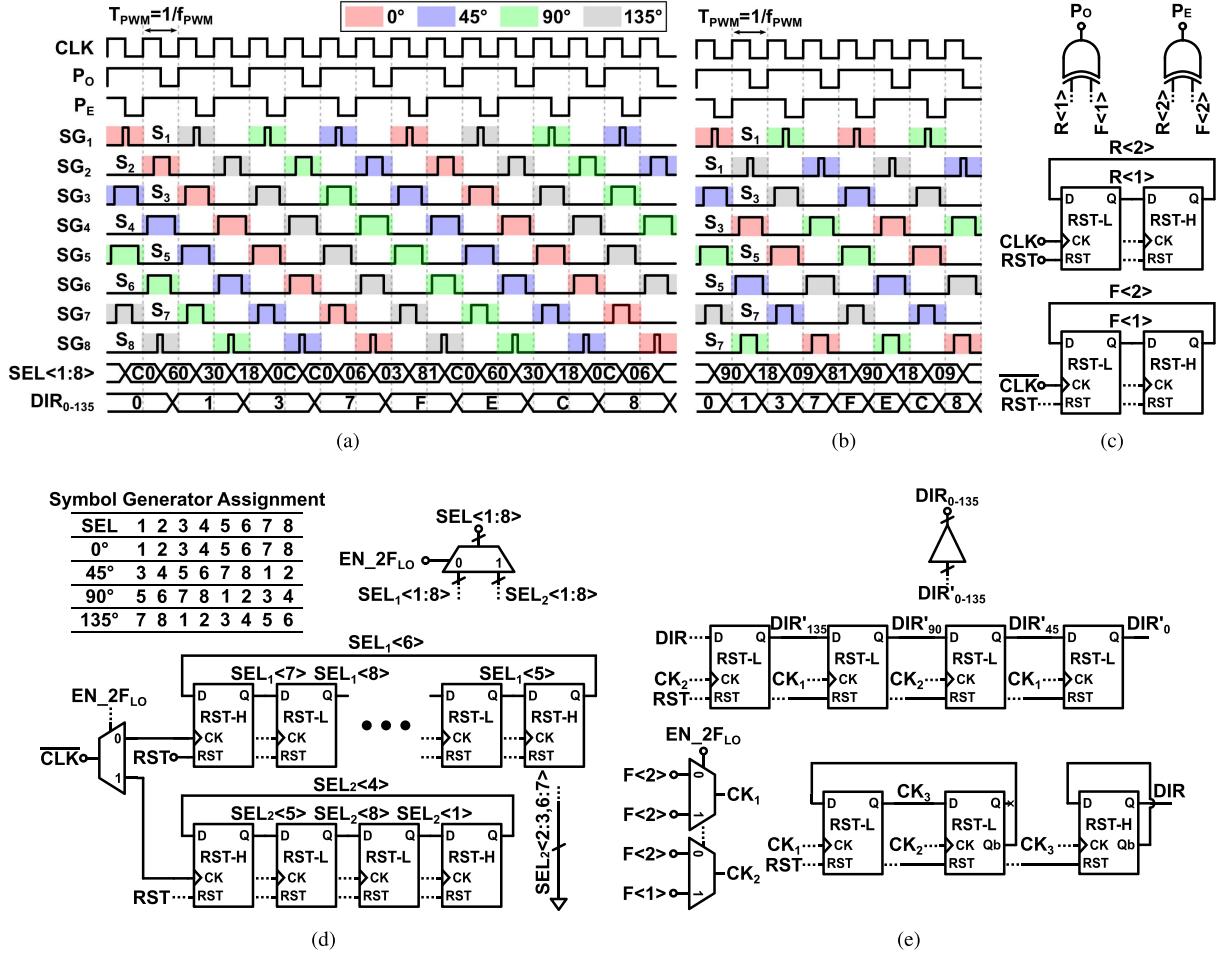


Fig. 8. Digital logic. (a) f_{LO} timing diagram. (b) $2f_{LO}$ timing diagram. (c) P_O and P_E generator. (d) $SEL\{1:8\}$ generator. (e) DIR_{0-135} generator.

S_4 and S_5 is 127 ps when f_{LO} and V_{LO} are 100 MHz and 0.8, respectively. To avoid this, $SEL\{1:8\}$ in Fig. 8(a) chooses both the current and the next symbols, and thus, seamless switching operation between symbols is achieved. This operation is implemented by the shift register in Fig. 8(d), which is comprised of two flip-flops that are initialized with a high value and six flip-flops with a low initial value.

The signals DIR_{0-135} determine the polarity of the symbols. Their transitions occur every $8T_{PWM}$ for f_{LO} synthesis. The time difference between DIR_{0-135} signals is $2T_{PWM}$. A shift register with four flip-flops triggered by $F(2)$ in Fig. 8(c) is used for this purpose, and its input is generated from a flip-flop whose output is inverted every $8T_{PWM}$ [Fig. 8(e)].

In order to increase f_{LO} , f_{PWM} can be increased. This, however, aggravates the narrow-pulse problem in the PWM generator. One approach to relieve the narrow-pulse limitation is to combine the 16 NTE-PWM symbols at baseband instead of pre-synthesis in the digital domain. In this paper, the sequence of the symbols is reordered instead increasing of f_{PWM} at the expense of the achievable HRR [11]. For example, the synthesis of $2f_{LO}$ can employ the sequence [$S_1, S_3, S_5, S_7, -S_1, -S_3, -S_5, -S_7$], which ensures that the narrowest pulsewidth is unchanged, while its HRR3 and HRR5 decrease to 40 and 18 dB, respectively. The fifth harmonic of 200 MHz is out-of-band and thus the reorganization of the symbol

sequence can be applied to generate $2f_{LO}$. Fig. 8(b) shows the timing diagram for $2f_{LO}$. The time difference between identical symbols in the multi-phase NDE-PWM signals is T_{PWM} and thus a NDE-SG which is triggered by P_O or P_E , that have a periodicity of $2T_{PWM}$, cannot function with multi-phase NDE-PWM signals. A pair of NDE-PWM SGs is thus assigned to a symbol. Consequently, the required selection signals are only $SEL\{1\}$, $SEL\{4\}$, $SEL\{5\}$, and $SEL\{8\}$. The selection signals are generated from a shift register comprised of four flip-flops in Fig. 8(d). The transition period of the polarity control decreases from $8T_{PWM}$ to $4T_{PWM}$, and thus, the DIR_{0-135} generator is reconfigured to be triggered by not only $F(2)$ but also $F(1)$, as shown in Fig. 8(e).

B. LNTA

Fig. 9 shows a single-ended low noise transconductance amplifier (LNTA) employed in the front end of the receiver (Fig. 2). The LNTA uses two stages to enhance gain. The first stage is an inverter-based amplifier, which provides input impedance matching. The second transconductance (G_m) combines the RF input signal and the output signal of the first stage for gain boosting. The input resistance of the first stage is given by

$$R_{IN} = \frac{R_{FB}}{G_m(R_{FB} || R_{o1})} \quad (4)$$

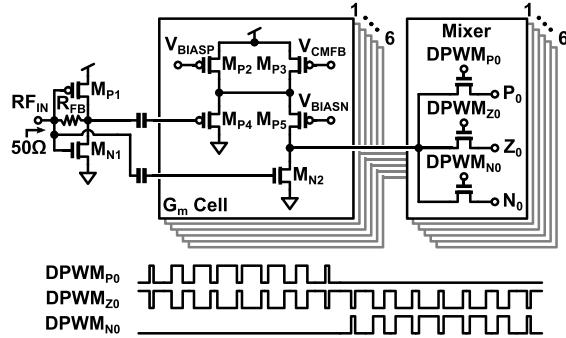


Fig. 9. Schematic of the LNTA and mixer.

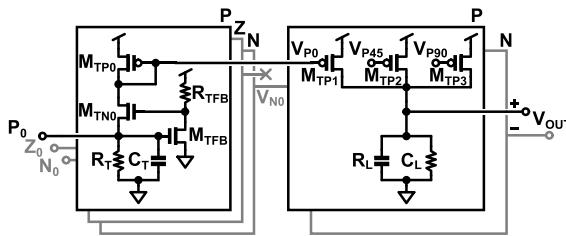


Fig. 10. Schematic of the transimpedance amplifier.

where G_{m1} is $g_{mp1} + g_{mn1}$, and R_{o1} is $r_{op1}||r_{on1}$. R_{FB} needs to be made large, in order to lower noise figure (NF). For achieving an input resistance of 50Ω , while considering R_{o1} , G_{m1} of 48 mS and R_{FB} of 575Ω are employed.

The noise of M_{P1} and M_{N1} is canceled in the current domain in the Gm-cell, using the noise cancellation principle [18], which improves the input stage NF. The first downconversion stage uses six paths to provide quadrature outputs with three phases in each output for the multi-phase configuration. Each downconversion path has a dedicated Gm-cell to avoid path-to-path interference that can occur during the overlap region between the multi-phase PWM signals. Each first-stage downconversion mixer is a single balanced mixer comprised of three switches instead of two switches (Fig. 9). The unbalanced differential P and N signals shown by DPWM_{P0} and DPWM_{N0} in Fig. 9 are applied to the mixer. The third switch provides a current path Z controlled by DPWM_{Z0} for the output of the Gm-cell when both P and N switches are off in the three-level NDE-PWM signal.

C. Transimpedance Amplifier

A common-gate stage is adopted for the transimpedance amplifier (TIA) at baseband (Fig. 10). The TIA combines the current mode outputs of the mixer paths. To achieve a low input impedance of the TIA, the transconductance of the input transistor, M_{TN0} , is boosted by the common-source amplifier comprised of M_{TFB} and R_{TFB}

$$R_{TIA} = \frac{1}{g_{mtn0}g_{mtfb}R_{TFB}}. \quad (5)$$

The TIA is the dominant source of the flicker noise in the design. Long-channel transistors hence are used to suppress this noise source. In addition, the resistor, R_T , is employed

for setting the bias instead of the current mirror to reduce the flicker noise. There are three input stages corresponding to P, Z, and N, but only P and N are translated into the voltage domain. The size ratio of M_{TP1} , M_{TP2} , and M_{TP3} is 1:1.42:1 for enhanced HR with multi-phase PWM-LOs.

D. HRR Calibration

Degradation of HRR in the proposed PWM-LO-based receiver can be expressed as a pulselwidth deviation in the PWM-LO. Consequently, all error sources can be compensated by controlling the reference voltages, V_P s and V_N s in Fig. 6. Each reference voltage is independently controlled for calibration by an external digital-to-analog converter instead of applying a common reference voltage (V_{GREF} in Fig. 6). The use of 16 reference voltages, however, makes it difficult to find the global optimal point with the highest HRR, because the many optimization variables lead to multiple local optimal points. For example, a duty cycle of 33% of the LO frequency completely rejects the third harmonic but does not reject the fifth harmonic. In this application, the minimum value of HR3, HR5 and HR7 ratios can be used as the criterion because the desired PWM-LO shows ideal rejection for the third, fifth, and seventh harmonics as shown in Fig. 3(b). Fig. 11(a) shows the simulation of HRR as a function of the reference voltage errors, V_{ERR1} and V_{ERR2} , in the two reference voltages that provide the left and right edges of S_1 in Fig. 5. It indicates that a gradient-based algorithm is not appropriate for finding the global optimal point due to the many local optimal points. A linear search algorithm is thus adopted, which is applied during the partial calibration as shown in Fig. 11(b). In this algorithm, $V_{REF}(1:16)$ are V_{P1-8} and V_{N1-8} in Fig. 6. The algorithm explores the combinations for which each reference voltage is independently varied with the other voltages held fixed. This is repeated N_{CAL} times. An N_{CAL} of 2 is experimentally selected in this paper. To improve the convergence rate of the linear search, the range and step of the reference voltages are tapered. For example, the first calibration is executed with a coarse range and step. After the first calibration, a finer range and step are applied, with initial reference voltages which are the values at the end of the first calibration. In this paper, three steps are employed to find the global optimal point accurately, as shown in Fig. 11(b).

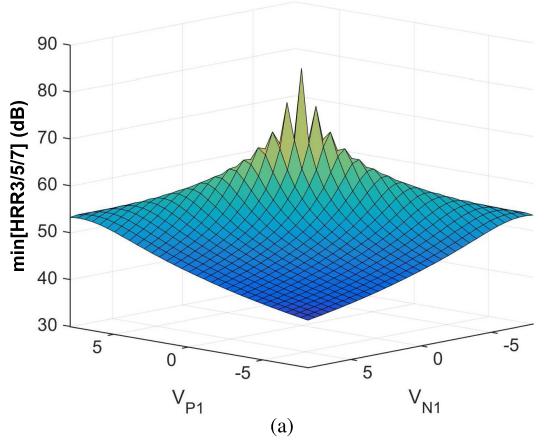
IV. NOISE

A. Noise Figure

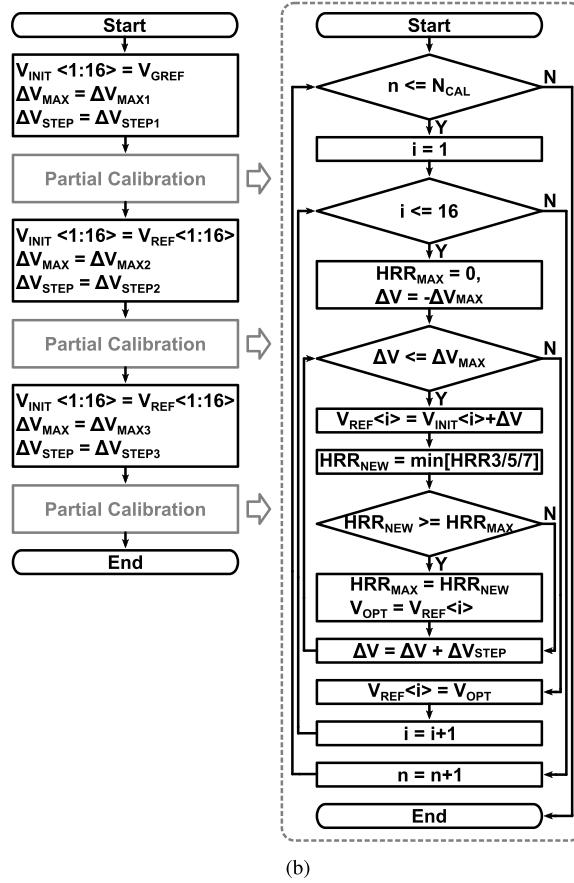
In this section, the NF is derived for the PWM-LO for synthesis of f_{LO} , i.e., without symbol resequencing. Baseband PWM is employed for the three-level NDE PWM-LO. From (2), the conversion gain of the receiver thus can be written as follows:

$$A_V = \sqrt{2}V_{LO} \left(\left(1 - \frac{R_{FB}}{R_S} \right) \kappa - g_{mn2} \right) \alpha R_{OL} \quad (6)$$

where R_S is the source resistance, R_{OL} is $(r_{op1}||r_{op2}||r_{op3}||R_L)$, κ is $((g_{mp4}g_{mp5})/(g_{mp4} + g_{mp5}))$,



(a)



(b)

Fig. 11. HRR calibration. (a) $\min[\text{HRR}3/5/7]$ with the error voltages. (b) HRR calibration algorithm.

and α is the ratio of the current flowing into the TIA, which can be defined as follows:

$$\alpha = \frac{\left(r_{\text{on}2} || r_{\text{op}5} \frac{g_{\text{mp}5}}{g_{\text{mp}4}} \right)}{\left(r_{\text{on}2} || r_{\text{op}5} \frac{g_{\text{mp}5}}{g_{\text{mp}4}} \right) + r_{\text{SW}} + R_{\text{TIA}}}$$

where r_{SW} is the ON-resistance of the switches in the mixer.

The noise generated from R_S , R_{FB} , M_{P1} , and M_{N1} in the first stage of the LNTA receives the benefit of reduced harmonic folding due to HR of the PWM-LO. Each noise output at the multi-phase paths is merged using a vector sum,

since each noise phase applied to the multi-phase paths is the same. The noise power due to those noise sources thus can be given by

$$N_{\text{OLNTA}1} = 16kT R_S \alpha^2 R_{\text{OL}}^2 T_{n_{\text{pwm}}}^2 \times \left[\left(\left(1 - \frac{R_{\text{FB}}}{R_S} \right) \kappa - g_{mn2} \right)^2 + 4R_S \beta^2 \eta \right] \quad (7)$$

where β is $(1/(2(R_{o1} + R_{\text{FB}}) + R_S))$, η is given by

$$\eta = R_{\text{FB}} \left(\frac{2R_{o1} + R_{\text{FB}}}{R_S} \kappa + g_{mn2} \right)^2 + (\gamma_p g_{mp1} + \gamma_n g_{mn1}) \left(R_{o1} \left(1 + \frac{R_{\text{FB}}}{R_S} \right) \kappa - g_{mn2} R_{o1} \right)^2$$

and $T_{n_{\text{pwm}}}^2$ is the noise folding factor of the three-level NDE PWM-LO, which is given by

$$T_{n_{\text{pwm}}}^2 = \frac{V_{\text{LO}}^2}{4} + \sum_{m=2,4,\dots}^{\infty} \frac{8}{(m\pi)^2} \sum_{n=1,3,\dots}^{\infty} J_n^2 \left(\frac{m\pi V_{\text{LO}}}{2} \right)$$

where $J_n(z)$ is the Bessel function of the first kind.

In a conventional HRM such as Fig. 1(a), the noise arising from the separated Gm cells cannot benefit from the above reduced harmonic folding, since the devices generating the noise are different and thus the phases of the noise sources are independent. By contrast, the noise of the separated Gm-cells in Fig. 9 also benefits from HR, because the PWM-LO signal inherently rejects harmonics. The noise output power in the multi-phase paths is linearly combined because the noise sources are independent of each other. The noise power of the Gm-cells at the output node can thus be described by

$$N_{\text{OLNTA}2} = 32kT \alpha^2 R_{\text{OL}}^2 T_{n_{\text{pwm}}}^2 \times \left[\gamma_p \kappa^2 \left(\frac{g_{mp2} + g_{mp5}}{g_{mp4}^2} + \frac{1}{g_{mp4}} + \frac{1}{g_{mp5}} \right) + \gamma_n g_{mn2} \right]. \quad (8)$$

There is no frequency translation or noise folding in the TIA. The noise output power due to the noise sources in the TIA can thus be expressed as follows:

$$N_{\text{OTIA}} = 8kT R_{\text{OL}}^2 \left[\frac{4(R_T + R_{\text{FB}} + \gamma_n g_{\text{mtfb}} R_{\text{FB}}^2)}{R_T^2} + 7.414\gamma_p g_{\text{mtfp}} + \frac{1}{R_L} \right]. \quad (9)$$

From (6)–(9), the double-sideband NF can be calculated as follows:

$$\text{NF} = \frac{\text{SNR}_i}{\text{SNR}_o} = \frac{N_{\text{OLNTA}1} + N_{\text{OLNTA}2} + N_{\text{OTIA}}}{2kT R_S A_V^2}. \quad (10)$$

Fig. 12 shows that (10) follows well the results of simulation and measurement. As V_{LO} increases, the NF decreases because the gain is linearly proportional to V_{LO} , as shown in (6).

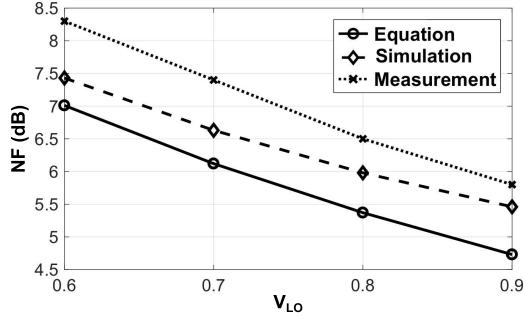
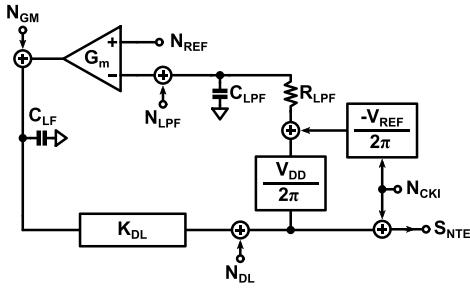
Fig. 12. NF with V_{LO} at 100-MHz LO.

Fig. 13. Linear model of the NTE-PWM SG for the phase noise analysis.

B. Phase Noise

1) *Phase Noise of the NDE-SG*: The PWM-LO is synthesized using the 16 NTE-PWM SGs, each of which employs a DLL (Fig. 7(a)). The propagation delay from the rising edge of the input clock, CLK_{IN} , to the rising edge of the output rectangular pulse, S_{NTE} , is independent of the control voltage of the VCDL in Fig. 7(a). On the other hand, the pulselwidth of S_{NTE} is determined by the delay of the VCDL. Hence, the average value of S_{NTE} , V_{avg} , can be expressed by the following equation when CLK_{IN} experiences a phase change of ϕ_n :

$$V_{avg} = \frac{\frac{V_{REF}}{V_{DD}} 2\pi}{2\pi + \phi_n} V_{DD} \approx V_{REF} - \frac{V_{REF}}{2\pi} \phi_n \quad (11)$$

where V_{REF} is the DC reference voltage.

A linear model of the NTE-PWM SG can be developed for phase noise analysis (Fig. 13), which uses (11). The noise transfer functions (NTFs) from various noise sources to the output can be derived from Fig. 13 as follows:

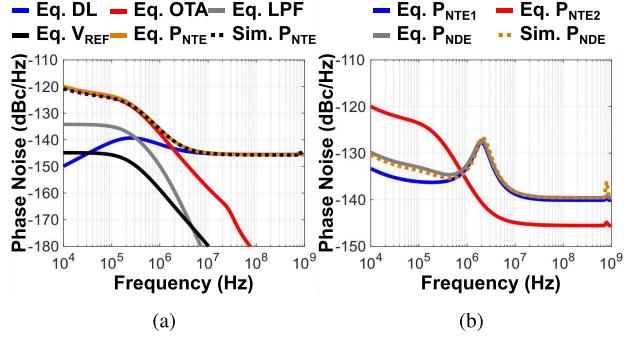
$$T_{CKI} = \frac{S_{NTE}}{N_{CKI}} = 1 + \frac{K_{DL} G_m V_{REF}}{T_{NTF}} \quad (12)$$

$$T_{DL} = \frac{S_{NTE}}{N_{DL}} = \frac{2\pi s C_{LF} \left(1 + \frac{s}{w_{LPF}}\right)}{T_{NTF}} \quad (13)$$

$$T_{LPF} = \frac{S_{NTE}}{N_{LPF}} = -\frac{2\pi K_{DL} G_m \left(1 + \frac{s}{w_{LPF}}\right)}{T_{NTF}} \quad (14)$$

$$T_{Gm} = \frac{S_{NTE}}{N_{Gm}} = \frac{2\pi K_{DL} \left(1 + \frac{s}{w_{LPF}}\right)}{T_{NTF}} \quad (15)$$

$$T_{VREF} = \frac{S_{NTE}}{N_{REF}} = \frac{2\pi K_{DL} G_m \left(1 + \frac{s}{w_{LPF}}\right)}{T_{NTF}} \quad (16)$$

Fig. 14. Comparison of the phase noise simulation results and equations. (a) Phase noise of S_{NTE2} for S_5 . (b) Phase noise of the NDE-SG for S_5 .

where

$$T_{NTF} = 2\pi s C_{LF} \left(1 + \frac{s}{w_{LPF}}\right) + K_{DL} G_m V_{DD} \quad (17)$$

where N_{CKI} and N_{DL} represent the phase noise of CLK_{IN} and VCDL, respectively. N_{LPF} and N_{VREF} model the voltage noise of the LPF and V_{REF} , respectively, and N_{Gm} is the current noise of the OTA used in the NTE-PWM SG.

From (12)–(16), the phase noise of S_{NTE} can be calculated by adding the single-sideband output noise powers, while considering the magnitude of the fundamental tone of a rectangular pulse

$$P_{NTE} = \mu_1^2 T_{CKI}^2 N_{CKI}^2 + T_{DL}^2 N_{DL}^2 + (T_{LPF}^2 N_{LPF}^2 + T_{Gm}^2 N_{Gm}^2 + T_{VREF}^2 N_{VREF}^2) \mu_2^2 \quad (17)$$

where $\mu_1 = (1/(\sin(\pi(V_{REF}/V_{DD}))))$, and $\mu_2 = (\pi/(8 \sin(\pi(V_{REF}/V_{DD}))))$.

The estimated phase noise using (17) matches well with the simulation result when an ideal clock of 800 MHz is applied, as shown in Fig. 14(a). The dominant noise sources for low and high offset frequencies are the OTA and VCDL, respectively. T_{DL} is a highpass response and thus the flicker noise generated by the VCDL is attenuated. By contrast, T_{Gm} is a lowpass response, and thus the flicker noise generated in the OTA is not suppressed. Equation (15) indicates that phase noise at low offset frequencies can be reduced by increasing the transconductance of the OTA, G_m . The noise of CLK_{IN} at low frequencies is boosted by $1 + (V_{REF}/V_{DD})$, where the maximum value of (V_{REF}/V_{DD}) is less than 0.5.

An NDE symbol, S_{NDE} , is generated using two NTE symbols and an XOR gate (Fig. 7(a)). The two NTE symbols have different duty cycles. These are synthesized by two different NTE-SGs and thus their noise sources are independent, except for the noise of CLK_{IN} . Hence, if the loop-bandwidth difference between the NTE-SGs is ignored, and the worst case T_{CKII} corresponding to larger V_{REF} , T_{CKII} , is used to estimate the phase noise, the phase noise of the S_{NDE} output, P_{NDE} , can be written as follows:

$$P_{NDE} = \left(\frac{a_{NTE1}}{a_{NDE}}\right)^2 P_{NTE1}|_{N_{CKI}=0} + \left(\frac{a_{NTE2}}{a_{NDE}}\right)^2 P_{NTE2}|_{N_{CKI}=0} + \left(\frac{T_{CKII}}{a_{NDE}}\right)^2 N_{CKI}^2 \quad (18)$$

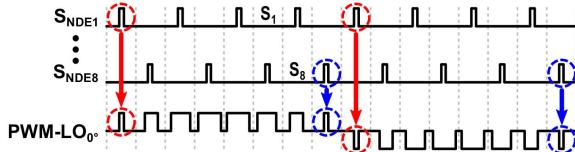


Fig. 15. Pulse selection for PWM-LO generation.

— $N_{CKI}@8f_{LO}$... Sim. P_{PWM} with $N_{CKI}=0$ — Eq. P_{PWM} with $N_{CKI}=0$
 — Eq. P_{PWM} with N_{CKI} ... Eq. P_{LO} with N_{CKI}

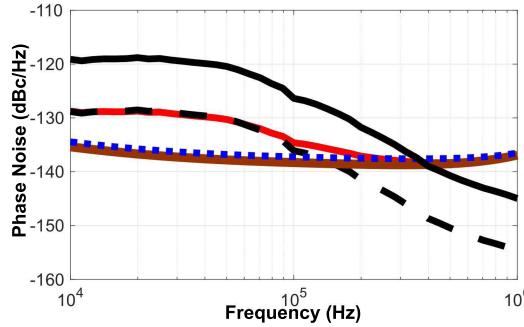


Fig. 16. Phase noise of PWM-LO.

where $a_{NTE1} = \sin(\pi(V_{REF1}/V_{DD}))$, $a_{NTE2} = \sin(\pi(V_{REF2}/V_{DD}))$, $a_{NDE} = \sin(\pi((V_{REF1} - V_{REF2})/V_{DD}))$, and V_{REF1} and V_{REF2} are the reference voltages for the two NTE-SGs, respectively. Fig. 14(b) shows that (18) follows the simulation results well.

2) *Phase Noise of the PWM-LO:* Individual pulses from the set $[S_1 - S_8]$ are applied to DPWM_P and DPWM_N (Fig. 9), respectively, once every half LO period ($1/2f_{LO}$) from a specific NDE-SG, (Fig. 15). The outputs of different NDE-SGs that have different duty cycles are combined and applied to the mixer switches, as shown in Fig. 9. The frequency of each these pulses, at DPWM_P and DPWM_N, thus decreases to one eighth of the NDE-SG output frequency. High-frequency noise for a sequence of specific pulses that is applied every $1/2f_{LO}$ can be assumed to be uncorrelated, while low-frequency noise is correlated. If we further assume that the loop-bandwidth difference between the NTE-SGs can be ignored, the phase noise of PWM-LO can be expressed as follows:

$$P_{PWM} = \sum_{n=1}^8 \left(\frac{4a_{NDE_n}}{8\pi V_{LO}} \right)^2 P_{NDE_n}|_{N_{CKI}=0} + \left(\frac{4T_{CKI_S4}}{8\pi V_{LO}} \right)^2 N_{CKI}^2 \quad (19)$$

where a_{NDE_n} and P_{NDE_n} represent a_{NDE} and P_{NDE} of the n th NDE-SG, respectively (18), and T_{CKI_S4} is the T_{CKI} corresponding to S_4 , which provides the worst case phase noise.

Fig. 16 shows that the estimated phase noise using (19) matches the simulation result well at low-frequency offsets when N_{CKI} and V_{LO} are 0 and 0.8, respectively. When CLK_{IN} has a low-phase noise of -126 dBc/Hz at 100-kHz frequency offset, which corresponds to the signal generator noise, at a

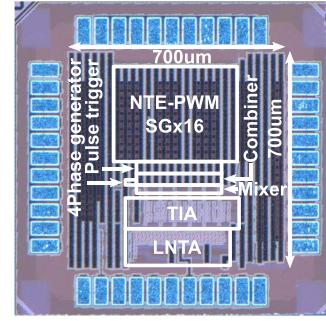


Fig. 17. Die microphotograph.

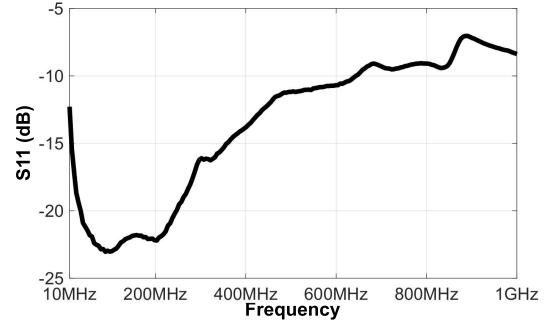
Fig. 18. S_{11} measurement results.

TABLE II
CURRENT CONSUMPTION BREAKDOWN (UNIT: mA)

	LNTA	TIA	Pulse trigger	Dual-edge PWM generator	Combiner ^(a)	Misc. ^(b)
Sim.	16.4	6.1	2.1	5.4	5.6	1.5
Meas.	13	5			13	

(a) Includes LO buffers.

(b) Includes the master clock input buffers, and bias generation circuits

carrier frequency of $8f_{LO}$, the dominant noise source at low offset frequencies is in fact, N_{CKI} , rather than any noise source in the design. To improve phase noise in low offset frequencies, V_{LO} needs to increase. If the dominant noise source determining the phase noise at low offset frequency is not N_{CKI} but N_{Gm} , then G_m needs to be increased.

For a conventional eight-phase HRM, if a duty cycle of 12.5% is used, then the phase noise of the LO can be described as follows:

$$P_{LO} = \left(\frac{1}{8 \sin(\pi/8)} \right)^2 N_{CKI}^2. \quad (20)$$

As shown in Fig. 16, the proposed PWM-LO and the conventional eight-phase HRM have a similar phase noise performance at low-offset frequencies.

V. MEASUREMENT

The receiver is implemented in a 40-nm CMOS process and its active area is $400 \mu\text{m} \times 600 \mu\text{m}$ (Fig. 17). S_{11} lower than -10 dB is measured over 100 to 600 MHz (Fig. 18). The total power consumption is 41.1 mW, out of which 16.9 mW is used in the digital section (Tables II and III).

TABLE III
PERFORMANCE SUMMARY AND COMPARISON

	This work		[19]	[10]	[9]	[11]
	HR	non-HR				
Architecture	Single-stage (PWM)	X	Discrete sampling	Single-stage (Phase Align.)	Two-stage	Two-stage (Phase Align.)
Variable Gain (dB)	3.7	X	X	X	X	X
LO Freq (GHz)	0.1-0.2	0.3-0.6	0.2-0.9	0.1-0.3	0.4-0.9	0.05-0.83
S11 (dB)	< -10		-	-	< -10	< -10
Gain (dB)	26.4-30.1	32-33	-0.5-2.5	12	34.4±2	12
DSB NF (dB)	5.8 / 6.5 ^(a)	5.4	18-20	11	4	11
IB/OOB-Band IIP3 ^(b) (dBm)	-20.1 / -15.1	-19.3 ^(d)	+10	+12	+3.5 / +16	+5.4 / N.A.
IB/OOB IIP2 ^(c) (dBm)	+31.4 / +36.2	+20.7 ^(d)	+53	+75	+46 / +56	+54 / N.A.
HRR3 (dB)	Multi-phase > 47 @ 100 MHz > 34 @ 200 MHz Single-phase: 73 with cal. @ 100 MHz	-	> 25	> 52	> 60	> 72
HRR5 (dB)	Multi-phase > 49 Single-phase: 76 with cal.	-	> 25	> 54	> 64	> 71
V _{DD} (V)	1.3 (Digital) / 1.4 (LNA) / 1.2 (Baseband)		1.2	1.3 (Digital) / 2.7 (Mixer)	1.2	1.2
Power (mW)	41.1 (Analog: 24.2)		19	69.8 (Analog: 59.4)	60 (Analog: 39.6)	67 (Analog: 33.9)
Process	40nm CMOS	65nm CMOS	110nm CMOS	65nm CMOS	65nm CMOS	130nm CMOS

(a) NF for $V_{LO} = 0.9$ and 0.8 respectively. Default mode for measurement is $V_{LO} = 0.8$.

(b) Out-of-Band IIP3 (OOB-IIP3) Frequency: 301.5 MHz and 502 MHz with $f_{LO}=100$ MHz.

(c) Out-of-Band IIP2 (OOB-IIP2) Frequency: 301.5 MHz and 302.5 MHz with $f_{LO}=100$ MHz.

(d) Only in-band IIP2 and IIP3 are defined for non-HR mode ($S_{11} < -10$ dB for interferers).

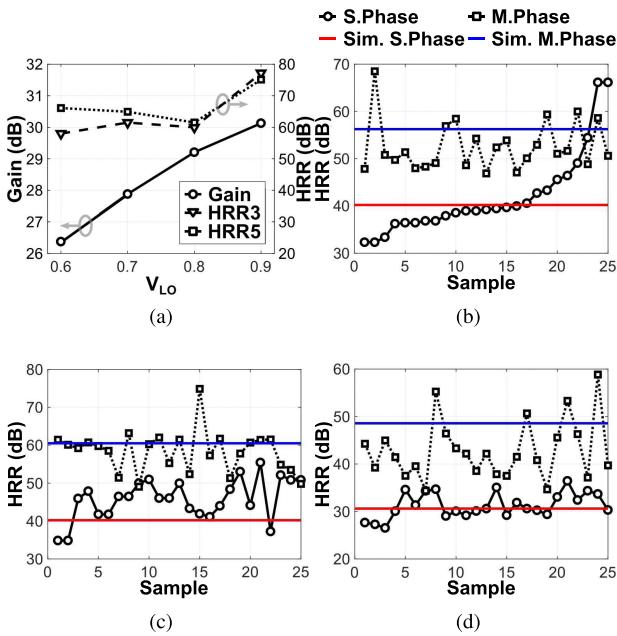


Fig. 19. Measurement results. (a) Gain control. (b) HRR3 for 100-MHz LO. (c) HRR5 for 100-MHz LO. (d) HRR3 for 200-MHz LO.

Fig. 19 shows the HRR and variable gain measurements. Gain control capability is demonstrated at 100 MHz. The amplitude of the LO fundamental is varied through pulsewidth control. Four different reference voltages (V_1-V_4) are employed in the NTE-PWM SG, which correspond to V_{LO} (Fig. 5) amplitudes of 0.6, 0.7, 0.8, and 0.9, respectively. V_{GREF} of 709 mV is used for V_3 , which is pre-designed with the resistor ladder, but 16 different voltages ($V_{P1}, V_{N1}, \dots, V_{P8}, V_{N8}$ in Fig. 6) are separately applied for

V_1 , V_2 and V_4 . As predicted by (6), the gain in the multi-phase LO configuration is linearly proportional to V_{LO} and varies from 26.4 to 30.1 dB with HR3 and HR5 ratios of approximately 60 dB at optimal reference voltage setting, as shown in Fig. 19(a), where S. Phase stands for single-phase and M. Phase indicates multi-phase.

The third and fifth HRRs are measured for 100 and 200 MHz LOs over 25 ICs without any calibration. A global reference voltage with a pre-designed resistor ladder, which corresponds to a V_{LO} of 0.8, is used for the measurement. The measurement results are sorted in ascending order of HRR3 of 100-MHz LO. With single-phase PWM-LO, HRR3s for the two frequencies are in the range of 32–66 dB and 27–36 dB, respectively. The means of measured HRR3s for two frequencies are 42 and 31 dB. These values are close to the average value of 40 and 31 dB extracted from Monte Carlo simulations, as shown in Fig. 19(b) and (d). The HRR of the 200-MHz LO is lower than that of the 100-MHz LO in a single-phase PWM-LO. This is because the reorganization of the pulse symbols used for the 200-MHz LO limits the achievable HRR to within 40 dB. Fig. 19(c) shows that HRR5, which is of importance for $f_{LO} = 100$ MHz only, is in the range from 35 to 55 dB, with an average value of 46 dB.

When the multi-phase configuration is employed, a HRR improvement of 12 dB is observed on the average, for both the LO frequencies. Fig. 19(b), however, shows that if the single-phase PWM HRR is initially high, the HRR improvement through the use of multi-phase PWM HR is reduced. There are 4 error sources that degrade the harmonic response of the three-level PWM-LO. They can be expressed by

$$\text{Error} = \Delta V_{\text{REF}} + V_{\text{OFF}} + \Delta V_{\text{th_PG}} + \Delta V_{\text{th_SW}} \quad (21)$$

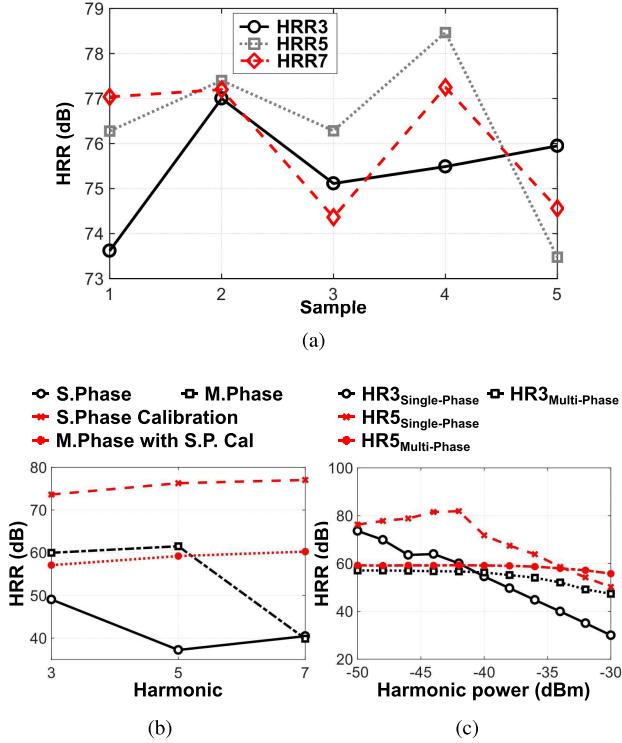


Fig. 20. Single-phase PWM calibration. (a) HRR measurement results. (b) Comparison of multi-phase PWM and single-phase PWM. (c) Sensitivity measurement results.

where ΔV_{REF} is the reference voltage error, V_{OFF} is the offset voltage of the OTA in Fig. 7(a), $\Delta V_{\text{th_PG}}$ is the V_{th} variation of the pass gate, and $\Delta V_{\text{th_SW}}$ is the V_{th} variation of the mixer switch. To generate multi-phase PWM-LOs for 100-MHz LO, the same symbol generators are used and thus ΔV_{REF} and V_{OFF} globally affect the multi-phase PWM-LOs, which can be suppressed by adopting dynamic element matching and chopping in the OTA. Thus, these errors are reduced upon merging the multi-phase PWM-LOs. By contrast, $\Delta V_{\text{th_PG}}$ and $\Delta V_{\text{th_SW}}$ impact multi-phase PWM-LOs individually and, hence, limit the achievable HRR improvement. In addition, the HRR sensitivity of the PWM-LO to the error increases with the HRR of the PWM-LO, as shown in Fig. 11(a), that is the sensitivity of the magnitudes and phases of the third and fifth harmonics to $\Delta V_{\text{th_PG}}$ and $\Delta V_{\text{th_SW}}$ increases as the HRR of PWM-LO increases.

The worst case HRR3 for f_{LO} of 200 MHz is lower than that of 100 MHz (Table III). Two OP-AMPS are assigned to a given symbol for the 200-MHz LO to generate multi-phase PWM-LOs, as shown in Fig. 8(b). V_{OFF} in (21) thus is not a global error for this case, and degrades the phase error and reduces HRR improvement at 200 MHz. This can be mitigated by employing chopping in the OTA.

Fig. 20 shows the measurement result of HRR after the single-phase PWM-LO is calibrated for 100-MHz LO by adjusting the 16 voltages ($V_{P1}, V_{N1}, \dots, V_{P8}, V_{N8}$ in Fig. 6) according to the calibration algorithm. The HRR3, HRR5, and HRR7 are measured over five ICs to confirm the accuracy of the proposed calibration algorithm. HRR3, HRR5, and

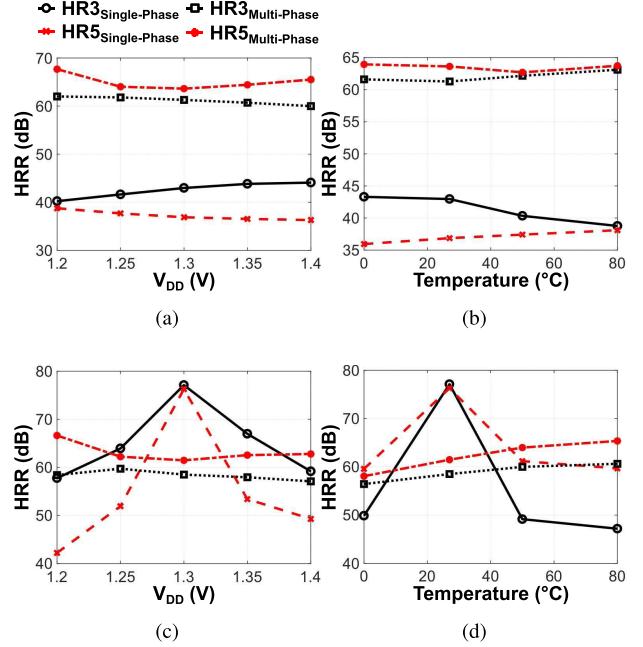


Fig. 21. Measurement results of HRR sensitivity (a) to V_{DD} without single-phase calibration, (b) to temperature without single-phase calibration, (c) to V_{DD} with single-phase calibration, and (d) to temperature with single-phase calibration.

HRR7 larger than 73 dB are achieved (Fig. 20(a)). In this case, the three paths in Fig. 4 use the same phase. With multi-phase PWM HR, HRR3 and HRR5 are degraded relative to a high value of single-phase PWM HRR because of the above explained reason (Fig. 20(b)). As shown in Fig. 20(c), the single-phase PWM-LO is sensitive to the input power because the effective LO waveform depends on the input voltage of the mixer. However, the multi-phase PWM-LO shows better HRR sensitivity. This is because the dependence of HRR on the signal amplitude appears as a global effect and hence is improved through multi-phase combination.

The sensitivities of HRR to variations in temperature and supply voltage, V_{DD} , are also measured for 100-MHz LO. V_{GREF} and the 16 reference voltages are linearly scaled with V_{DD} . With single-phase PWM, HRR variation of approximately 4 dB is measured for V_{DD} from 1.2 to 1.4 V and temperature from 0 °C to 80 °C when HRR is nominally 40 dB [Fig. 21(a) and (b)]. The sensitivities to V_{DD} and temperature, however, increases as HRR increases, as shown in Fig. 21(c) and (d). Fig. 21(b) and (d) indicates that the proposed calibration for single-phase PWM is effective for achieving robust HRR of nearly 50 dB without background calibration, in the presence of temperature variation. Multi-phase PWM shows better sensitivity of HRR because combining multi-phase LOs compensates global effects such as temperature and V_{DD} variations.

Worst case IIP3 of -20.1 dBm is measured, as shown in Fig. 22(a). The resistance of the mixer switch experiences significant non-linearity while the switch is turning on or off. This non-linearity can be especially significant for narrow pulsewidths. This is, however, not a problem for the linearity of the entire receiver, because the gain itself decreases for narrow

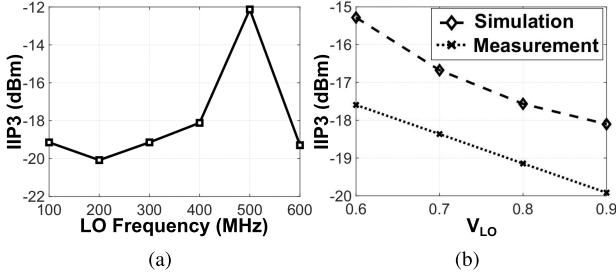


Fig. 22. Linearity. (a) IIP3 measurement results. (b) IIP3 with V_{LO} at 100-MHz LO.

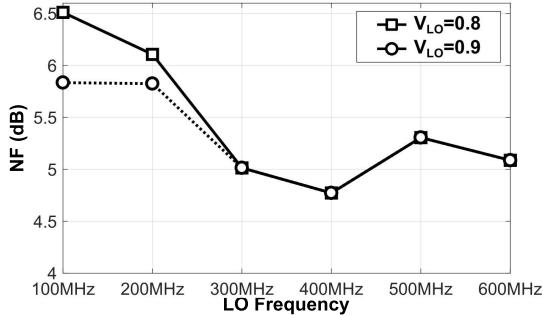


Fig. 23. double-sideband noise figure measurement results.

pulsewidths. For example, in Fig. 19(a), the gain decreases as V_{LO} decreases because the pulsewidth also decreases. Further in-band linearity is limited by the baseband stage. As such, in-band IIP3 actually increases as the pulsewidth decreases (Fig. 22(b)).

As explained in Section IV, the NF decreases with V_{LO} . This is also observed in the measurement of Fig. 23.

VI. CONCLUSION

This paper demonstrates the use of a PWM-based sinusoidal signal in the LO path. This approach makes it possible to simplify the signal path of the received signal. A three-level NDE PWM is adopted as a PWM-LO, which shows ideal rejection for the third, fifth, and seventh harmonics. To resolve the problems of high-bandwidth requirement for a high LO frequency, an open-loop PWM generator based on a parallel approach is proposed. Symbol generation using the DLL makes it possible to generate the PWM-LO without quantization noise. The use of the PWM-LOs in a multi-phase configuration with scaled baseband gain coefficients for enhanced HRR is also demonstrated.

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