1.4Gsearch/s 2-Mb/mm^2 TCAM Using Two-Phase-Pre-Charge ML Sensing and Power-Grid Pre-Conditioning to Reduce *Ldi/dt* Power-Supply Noise by 50%

Igor Arsovski, Akhilesh Patil, Robert M. Houle, Michael T. Fragano, Ramon Rodriguez, Raymond Kim, and Van Butler

***Abstract*— This paper describes two power-supply noise (*Ldi/dt*) management techniques implemented in a 14-nm ternary content-addressable memory (TCAM) compiler that allows a 2K x 640 b instance to perform 1.4Gsearches/s while achieving a density of 2 Mb/mm^2. This represents a 15% better performance and 10% better density than previous state-of-the-art TCAM. The first technique reduces the within-cycle noise by employing a two-phase match line (ML) pre-charge circuit which shuts off the pre-charge shoot-through current on easy-to-detect multi-bit mismatched MLs early in the cycle thereby approximately saving 60% of the ML power and reducing the within-cycle noise by 49.7%. The second technique is to reduce the multi-cycle noise by inserting targeted dummy search operations during low-current demand periods to flatten out current demand and reduce *Ldi/dt* noise by another 50%.**

***Index Terms*— FinFET, *Ldi/dt*, power saving, power-supply noise reduction, single-ended sensing, ternary content addressable memory (TCAM), two-phase match line (ML) pre-charge circuit.**

I. Introduction

CONTENT-ADDRESSABLE memory (CAM) is a special type of computer memory used to implement high-speed look-up tables. Like conventional static random access memories (SRAM), a CAM can be written or read by indexing the word line addresses. Unique to the CAM, however, is that every memory cell includes a dedicated bit-compare circuit that allows a search of the entire contents of the CAM to be performed in a single clock cycle. A data word supplied on the search bus is compared to each stored word concurrently, and the search results are returned to the match bus. If the searched data is found, the CAM returns a list of one or more storage addresses where the word was found.

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I. Arsovski, A. Patil, R. M. Houle, M. T. Fragano, and R. Rodriguez are with GLOBALFOUNDRIES, Essex Junction, VT 05402 USA (e-mail: akhilesh.patil@globalfoundries.com).

R. Kim is with GLOBALFOUNDRIES, Endicott, NY 05402 USA.

V. Butler is with Green Mountain Semiconductor, Burlington, VT 05401 USA.

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Since the CAM is designed to search its entire memory in a single operation, it provides the lowest latency hardware search solution. However, this powerful search operation comes at the cost of lower memory density and increased memory power when compared to a conventional SRAM. The TCAM density is degraded by the dedicated bit-compare circuits present in each bit cell, while the power (and consequently noise) increase comes from the fully parallel activation of all words during the search operation.

Ternary-CAM (TCAM) allows three matching states which include 1, 0, and "X" (i.e., don't care) for one or more bits in the stored data word. TCAM executes a fully parallel search of the entire memory contents and uses a wild-card pattern matching to return search results in a single clock cycle. This capability makes TCAM attractive for implementing fast hardware look-up tables in network routers, processor caches, and many pattern recognition applications. However, the push for higher performance and memory density coupled with high-parallel circuit activity creates noise challenges that if left unmitigated could result in timing fails in both TCAM and its surrounding logic.

The noise challenges mentioned above can be categorized into within-cycle noise and multi-cycle noise. The within-cycle noise arises due to the data-dependent current demand of the high-performance self-referenced match-line sensing scheme (SRSS) [2]. When fully active the TCAM activates every search line (SL) and every match line (ML) in the array, creating a current demand more than ten times that of a similar capacity SRAM array. To reduce power conventional SRSS uses pre-charge-to-GND ML sensing, which eliminates the need for resetting the SLs to ground every cycle reducing SL power by an average of 50%. However, the SRSS pre-charge phase also creates active shoot-through current through the mismatched-bit-compare circuits during ML pre-charge, causing mismatched-bit dependent ML current demand.

Multi-cycle noise occurs due to the current load step as the TCAM transitions from low (NOOP) to high (SEARCH) current demand across multiple cycles. During inactive periods, the TCAM draws very little current, and during READ and WRITE operations the TCAM is equivalent to a normal SRAM. But during a SEARCH operation there could be a large

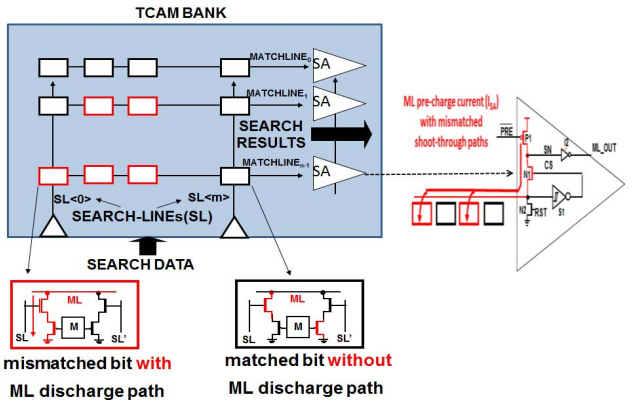


Fig. 1. TCAM implementation of the self-referenced sense amplifier sensing architecture.

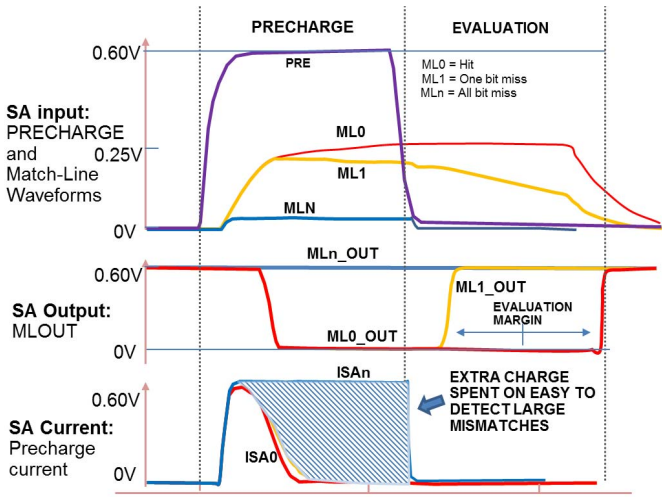


Fig. 2. Conventional SRSS waveforms highlighting wasted current spent on muti-bit mismatched MLs.

increase in current consumption where all compare circuits are active in parallel. The most severe *Ldi/dt* occurs when switching from an idle cycle [i.e., no operation (NOOP)] to a SEARCH operation in which all MLs miss in multiple bit positions. The resultant high *Ldi/dt* can cause significant voltage reduction (>15%) that can affect the performance of the TCAM and surrounding logic. To help alleviate this condition, most TCAMs designate a few bits of the word (e.g., 8 bits) for a pre-compare operation, so that the compare circuitry for the remaining bits in the word are only activated if the pre-select bits match. This technique helps to keep the average power as low as possible, but there will always be pathological cases where the majority of the main compare bits still are active.

II. Proposed Techniques

This paper describes two *Ldi/dt* management techniques to reduce within-cycle noise and multi-cycle *Ldi/dt* noise, implemented in a 14-nm FinFet technology TCAM. The work presented in this paper has 15% better performance and 10% better density than previous state-of-the-art TCAM [1]. The technique to reduce within-cycle noise consists of a two-phase ML pre-charge scheme which cuts the current on easy-to-detect multi-bit mismatched MLs early in the cycle and reduces ML power by 60%. To reduce multi-cycle noise, targeted dummy search operations are inserted during low-current demand periods to flatten out current demand and reduce *Ldi/dt* noise by 50%.

A. Two-Phase-Pre-Charge Self-Referenced Sensing Scheme

The main motivation that led to the development of the two-phase-pre-charge (TPP)-SRSS scheme is the challenge with the data-dependent current demand of the high-performance SRSS [2], as shown in Fig. 1. Each TCAM cell (shown as "M" in Fig. 1) consists of two SRAM bit cells (X and Y) that allow the ternary encoding, and two bit-compare devices that compare the data presented on the SLs to the data stored in the cell. When the search data are presented on the SL, the TCAM cell will effectively compute the exclusive-nor (M'∗SL + M∗SL') for each bit position and if M does not equal SL, then at least one bit will mismatch and there will be a conducting path from the overall word ML to the ground. To understand the benefits of the novel TPP-SRSS, it helps to first understand the operation of the conventional SRSS scheme as shown in Fig. 1.

The conventional self-referencing sense amplifier (Fig. 1) operates in two stages: pre-charge and evaluate. In the pre-charge phase (where RST = 0, PRE = 1), transistor P1 in each of the sense amplifiers tries to pre-charge the ML toward VDD. If the ML has many mismatched bits (MLN, where $N > 8$), transistor P1 will not be able to pull the ML high due to the shoot-through current in each mismatched bit. However, if the ML has zero mismatched bits (ML0) or one mismatched bit (ML1) or only a few mismatched bits, then the ML will start to pre-charge. As soon as the ML voltage crosses the threshold of inverter S1, the charge sharing node voltage drops to a level that biases n-fet N1 in the cut-off region and stops the ML pre-charge. At this point, each ML0 and ML1 is pre-charged to a unique level slightly above the threshold of its respective sense amplifier (SA). As soon as the ML voltage reaches this level, the pre-charge current from P1 is channeled to sensing node (SN) quickly charging it to VDD and switching MLOUT low. This completes the pre-charge phase with the waveforms as shown in Fig. 2. Since, each ML pre-charge voltage is self-referenced to its corresponding SA threshold (that is just above the trip point of S1, approximately Vtn) this sensing scheme shows very good process-voltage-temperature (PVT) independence.

The key advantage of the SRSS scheme is that each ML is pre-charged just to the level it needs to be at for its specific sense amp which enables significant performance and power improvements as compared to the conventional full rail pre-charge schemes, regardless of PVT. In addition to ML current saving, the SRSS also eliminates the need for SL reset, further reducing SL power by 50%. Assuming the same SL switching activity on both conventional pre-charge to rail and SRSS schemes, both methods require a pre-charge pulse which has a duration determined by a replica-bias circuit. Because the SRSS scheme only pre-charges to the level required by each ML sense amplifier (∼VDD/3), the SRSS method will always consume less power than the conventional method regardless

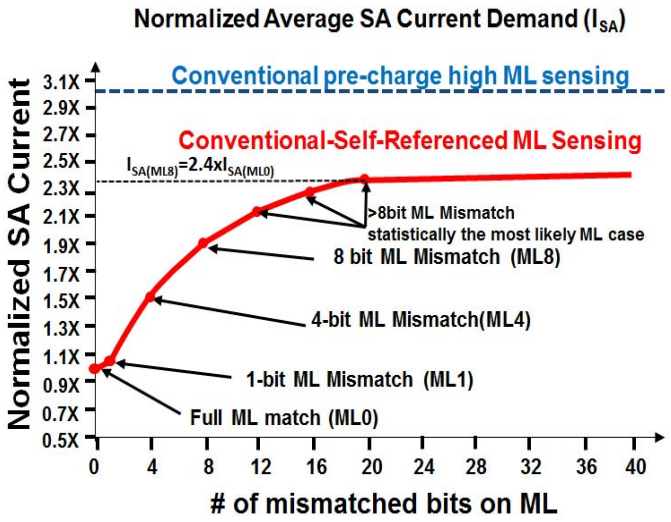


Fig. 3. Comparing the normalized SA current as a function of number of mismatched bits on both the ocnventional pre-charge to VDD [1] and self-referenced sensing.

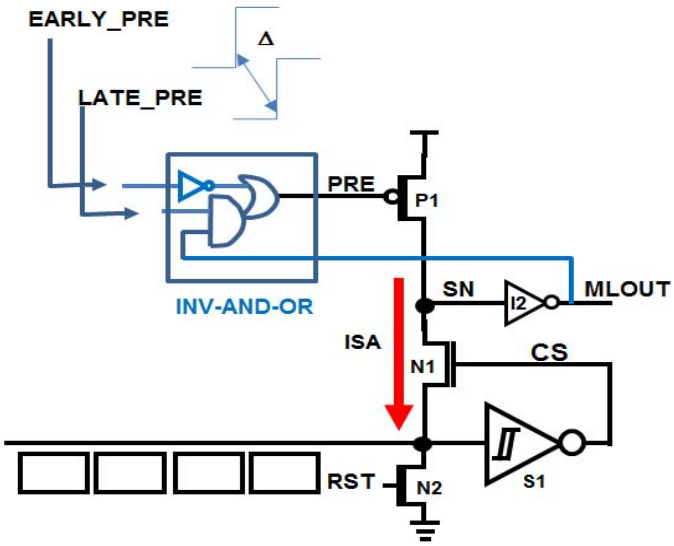


Fig. 4. TPP-SRSS highlighting changes to SRSS in blue.

of PVT and number of mismatched bits. In the case of a hit, neither scheme suffers shoot-through current, but the SRSS scheme will always consume less power than the conventional method because the self-referencing circuit will stop the pre-charge. In the case of a few-bit miss, where the ML would pre-charge to a level higher than the trip point of the inverter S1, the SRSS scheme will stop the pre-charge, but the conventional method will not. If there are many mismatched bits and the ML pre-charges to a level lower than the trip point of the inverter S1, then the SRSS would draw less current than the conventional because of the series resistance associated with the n-fet N1.

During the evaluation phase (where PRE = 0), ML0 acts like a capacitor keeping its pre-charged state, while ML1 starts to discharge through the mismatched-bit-compare circuit. As ML1 discharges, it quickly trips S1 causing SN and ML to quickly equalize and then discharge, bringing MLOUT1 back to its high state. This quick evaluation is the key advantage to the SRSS scheme, in that each ML is pre-charged just to the level it needs to be at for its specific sense amp, which enables significant performance and power improvements compared to the conventional full rail pre-charge schemes, regardless of PVT. However, as the number of mismatched bits increases, most of the current during the pre-charge phase is sunk to ground by the mismatched bits. This causes an active shoot-through current, with a magnitude that is dependent on the number of mismatched bits. Fig. 2 shows the waveforms for the self-reference sense amplifier scheme where the circuit simulations were done at VDD = 0.6 V and temperature = 125 °C. From the simulation results of the Self-Referenced ML sensing scheme one can see that this scheme consumes extra shoot-through current on easy-to-detect multi-bit mismatches while consuming less current on hard to detect matches and one-bit mismatches. Fig. 3 illustrates the normalized current demand for the hardest to distinguish ML cases [full match (ML0) and 1-b miss (ML1)] versus that of the easiest to detect all-bit mismatched MLs (MLN, where $N >> 0$). In the case of the full match (ML0), the SRSS sense amplifier consumes only enough current to pre-charge the ML capacitance to the threshold of the sense amplifier (about 1/3 VDD). This results in > 60% ML current saving when compared to the pre-charge-to-VDD ML sensing that pre-charges the MLs all the way to VDD [3], [5]. In addition to ML current saving, the SRSS also eliminates the need for SL reset, further reducing SL power by 50%. However, since the SRSS SL's are enabled during pre-charge, the SRSS creates shoot-though current though the mismatched XOR stacks consuming additional ML power. With most ML's having > 8 b mismatches, the current demand for an average SRSS ML is 2.4 × that of a match, nearing the ML current of pre-charge-to-VDD ML sensing schemes [3].

To maintain the performance and power benefits of the SRSS while also reducing the worst-case power consumption (due to the shoot-though current mentioned above), the TCAM described in this paper uses a TPP-SRSS, as shown in Fig. 4.

The early pre-charge phase is first used to make a gross differentiation between likely matches versus large mismatches, while the second pre-charge phase spends additional current to further differentiate the full match case from the few bit mismatch cases. To cut the current on easy-to-detect large mismatches, this circuit starts the phase one of the ML pre-charge with the EARLY_PRE signal. With the ML reset to GND, the pre-charge current flows though P1 and N1 and starts charging the MLs. MLs with a few bit mismatches charge up quickly thereby causing MLOUT to fall shortly after EARLY_PRE is asserted. In contrast, ML's with many mismatches will charge up more slowly, preventing or delaying the fall of MLOUT. If MLOUT is still high, after a replica-bias generated delay, when LATE_PRE starts the second phase of the pre-charge, the INV-AND-OR will stop the pre-charge current. Each SA makes its own decision whether to continue

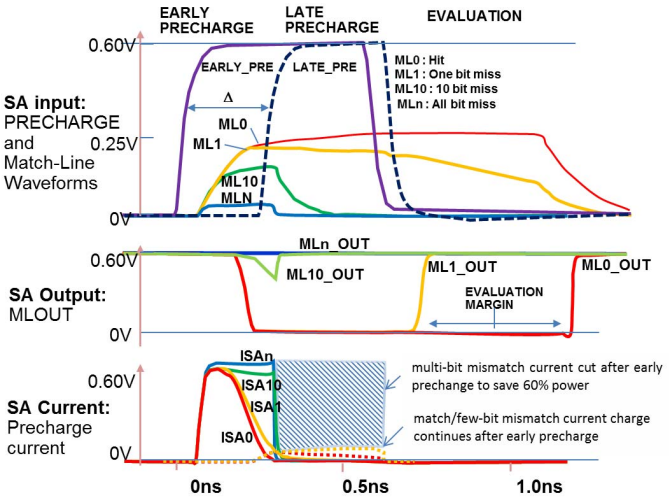


Fig. 5. TPP-SRSS simulation waveforms highlighting the current savings associated with multi-bit mismatched MLs.

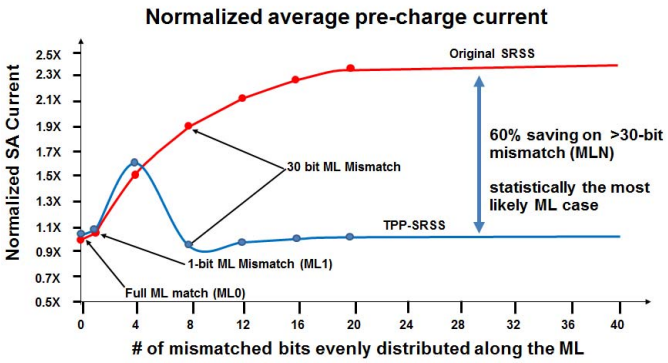


Fig. 6. Comparison of normalized SA current of conventional SRSS and TPP-SRSS.

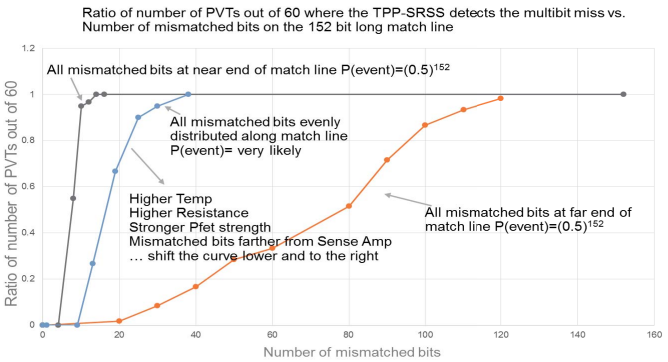


Fig. 7. Approximate probability: the TPP-SRSS INV-AND-OR circuit will detect a multi-bit miss across 60 extreme PVTs.

to supply current to the lightly mismatched ML's or cut the current and save power on ML's with many mismatched bits. MLs whose MLOUT signal is low continue to receive current, while MLs where the MLOUT signal is high stop pre-charging, saving $>$ 60% of the ML current. Fig. 5 shows the simulation results of a TPP self-referenced ML sensing scheme at 0.6 V and 125 °C. It shows the benefit of current savings achieved in this scheme when all the mismatched bits are at the near end of the ML. The multi-bit mismatch current is shut off after the early pre-charge phase to save nearly 60% of the total power. Fig. 6 shows the normalized SA current versus number of bits mismatched on ML comparison for the conventional SRSS and the TPP-SRSS circuit. The current savings in the TPP-SRSS scheme are more prominent after 8-bit ML mismatches. Since statistically most MLs have $>>$8 b mismatches on a 160-b-wide ML this scheme saves an average of 60% of the ML current power. A critical observation from Fig. 6 is that the circuit's ability to detect the current of the mismatched bits is strictly a function of the voltage at the near end of the ML relative to the trip point of the sense amplifier. In Fig. 6 (at 0.6 V and 125 °C), the TPP-SRSS scheme detected eight-mismatched bits all at the near end, which means that the circuit has the capability to perform an early detect on ML resistance equivalent to eight-XOR stacks.

Since, the TPP-SRSS scheme samples the output of the SRSS ML sense amp shortly after the pre-charge has started, the delay of the second phase pre-charge has to be large enough to complete the pre-charge when there are not any mismatched bits. This is accomplished by using a replica-biased ML timing circuit with no mismatched bits. When there are mismatched bits on the real ML the probability that the TPP-SRSS scheme will successfully detect a given number of mismatched bits depends on many factors: process, voltage, temperature, wire resistance, and the position of mismatched bits along the match line. Fig. 7 shows three different mismatched-bit placement scenarios for 60 different PVT's [five different p-fet/n-fet relative strengths $*$ two voltages (high/low) $*$ two temperatures (high/low) $*$ three ML resistances (high/nominal/low)]. The x-axis shows the number of mismatched bits on the ML, and the y-axis shows how many PVT's out of 60 resulted in an early detect as a function of number of number of mismatched bits on a 152-bit-long ML. The middle curve depicts the most likely scenario where the mismatched bits are evenly distributed along the ML. For this case, the TPP-SRSS circuitry successfully detected the multi-bit mismatch condition for all 60 PVT simulations when the number of mismatched bits exceeded 38. From the binomial distribution, assuming matched bits are equally likely as mismatched bits, the probability of getting N mismatched bits on a 152-bit-long main-compare ML is $(152! \times (0.5)^{152})/((152 - N)! \times N!)$ which can be approximated by the Gaussian distribution with a mean of $152 \times 0.5 = 76$ and a variance of $152 \times (0.5)^2 = 38$. Hence, the probability that most MLs will have more than 38 mismatched bits is very high (approximately 6.16σ or one minus $3.56e^{-10}$), and as such, the probability for the TPP-SRSS scheme to detect a multi-bit miss is nearly one. The left and right curves represent virtually impossible bounds where all mismatched bits are grouped together on either end of the ML. For example, the probability of having no mismatched bits in the first 20 near-end bit positions is less than 1 in a million (0.5^{20}, to be exact).

While the TPP-SRSS scheme may not be completely deterministic in nature, it will statistically limit the maximum current drawn by the TCAM during a search operation and

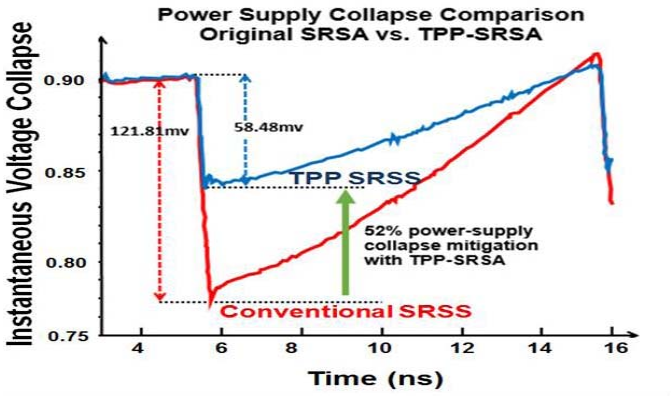


Fig. 8. Simulation showing TPP-SRSS power-supply noise collapse reduction.

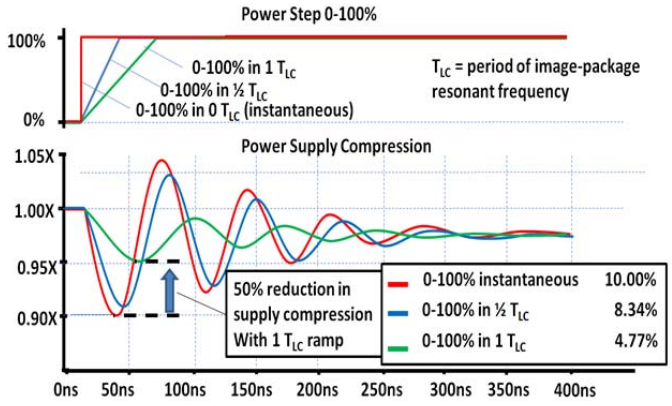


Fig. 9. Normalized load-step response and effect on power supply.

help prevent any user from placing the TCAM into some pathologically high current condition.

Fig. 8 shows the power supply collapse simulation comparison between a conventional SRSS and TPP-SRSS during a worst-case search event which is characterized as 8 bit of pre-compare hits and 152 bits of main compare misses on a 160-b-wide ML. The new TPP-SRSS scheme reduces the fast transient *Ldi/dt* power-supply noise by 52%.

B. Multi-Cycle di/dt Reduction Architecture

Large multi-cycle voltage swings on the power grid that services a large TCAM macro can wreak havoc on the timing and, if severe enough, the functionality of the TCAM and other nearby circuitry. Supplying sufficient decoupling capacitance via front-end-of-the-line structures is too area intensive to be cost effective and metal decoupling capacitors at higher levels of metal might not have a large enough charge reservoir to prevent localized power voltage swings. One way to reduce the amount of supply collapse is to reduce the power-step magnitude or to spread the power step over multiple cycles to reduce di/dt. The multi-cycle di/dt noise reduction technique described next (called the "HUM" method) helps to reduce the power-step magnitude for the worst-case search operation by nearly 50%.

Fig. 9 shows the power-supply noise on the TCAM grid as a function of the power step (di/dt). For the instantaneous

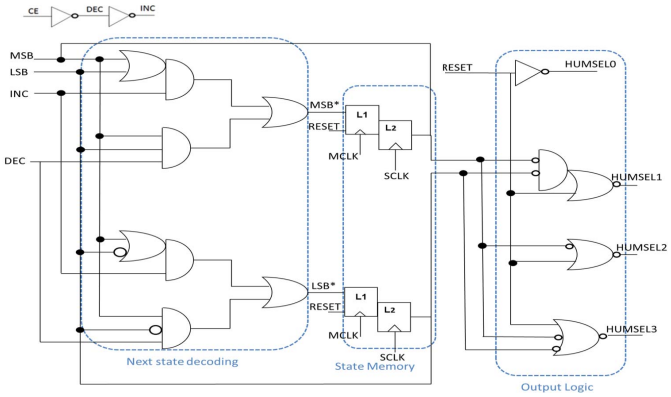


Fig. 10. Circuit diagram of the state machine used to implement the state multi-cycle di/dt scheme.

power step, the supply collapse is around 10%. (This would be the case when the entire TCAM macro transitions from NOOP to worst-case SEARCH). As the power step is spread across multiple cycles, the amount of supply collapse on the power rails is reduced. This amortization technique is the basic idea of the HUM method. The multi-cycle wake-up strategy is implemented by activating the TCAM from a low-power idle state, with no dynamic power consumption, to moderate-power HUM mode, where targeted dummy SEARCH operations are inserted in inactive TCAM blocks during low-power periods (such as NOOP's, READ's, and WRITE's) to amortize the overall di/dt. This technique is implemented by using a four-state state machine, the circuit diagram of which is shown in Fig. 10. The state variables MSB and LSB are used to denote the present state, whereas MSB$*$ and LSB$*$ are used to denote the next state. Activating chip enable (CE) causes DEC $=$ 0 and INC $=$ 1 and when the RESET signal is forced to a logic one, the L1 and L2 latches are both reset to zero (state S0 $\{\text{MSB} = 0, \text{LSB} = 0\}$). When RESET is de-asserted, the state machine proceeds through the sequence from S0 to S1->S2->S3 (since INC $=$ 1) on each master/slave clock cycle (MCLK/SCLK). The state transition table for the state machine is shown in Fig. 11. The output signals of the state machine HUMSEL [0:3] are then used to control the block fields in the TCAM. Fig. 12 shows the truth table for the output logic. Each block field in Fig. 13 is individually controlled by one of the four HUMSEL signals. HUMSEL0 controls the innermost four block fields of the TCAM, similarly HUMSEL1, HUMSEL2, and HUMSEL3, respectively, control the outer block fields as shown Fig. 13. So, for example, when the four innermost block fields are activated by the HUMSEL0 signal, a dummy SEARCH operation is performed in each of these block fields. On the next master/slave clock cycle, HUMSEL1 is activated and dummy search operations are performed in both HUMSEL0 and HUMSEL1 block fields. This pattern continues until state S3 is reached, where all block fields are performing dummy search operations. The chip stays in highest HUM mode power state S3 until a functional operation (READ/WRITE/SEARCH) is performed. When the chip is powered down (CE transitions from high to low) DEC $=$ 1 and INC $=$ 0, the state machine proceeds through the sequence S3->S2->S1->S0. In state S0 when the

INC	DEC	Current state	Next State
1	0	S0	S1
1	0	S1	S2
1	0	S2	S3
1	0	S3	S3
0	1	S0	S0
0	1	S1	S0
0	1	S2	S1
0	1	S3	S2

Fig. 11. State transition table for the state machine.

STATE	MSB	LSB	RESET	HUMSEL0	HUMSEL1	HUMSEL2	HUMSEL3
X	X	X	1	0	0	0	0
S0	0	0	0	1	0	0	0
S1	0	1	0	1	1	0	0
S2	1	0	0	1	1	1	0
S3	1	1	0	1	1	1	1

Fig. 12. Truth table for the output logic of the state machine.

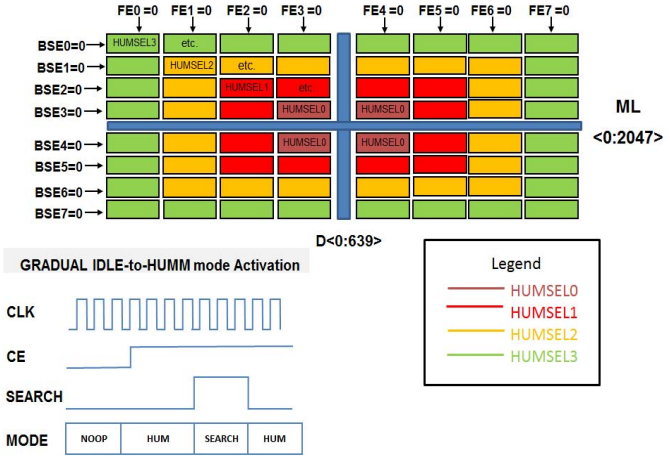


Fig. 13. Gradual NOOP-to-HUM mode activation pattern to activate the banks. The innermost (red) banks are activated first followed by the outer banks.

RESET signal is activated, the TCAM will transition to the power-OFF state.

Fig. 13 shows the gradual HUM mode activation when CE is activated, causing the TCAM to gradually transition from low-power idle mode (state S0) to moderate-power HUM mode (state S3). This particular TCAM is configurable up to 2K words where each word is 640 bits and can be divided into eight fields, such that each field contains 80 bits. Each word is divided into blocks of 256 TCAM cells, so that a 2-K word instance would have eight blocks. The

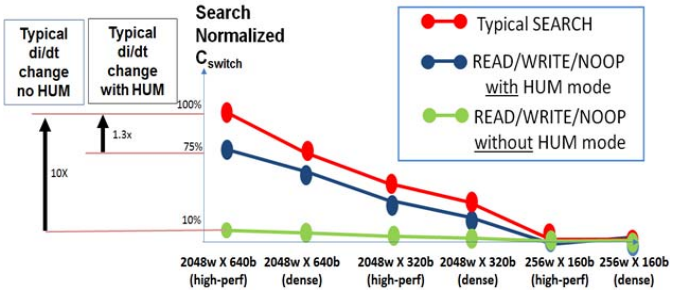


Fig. 14. Search normalized Cswitch for different operations across different TCAM configurations.

signals BSE⟨0:7⟩ and FE⟨0:7⟩ are the block search enable and field enable signals, respectively, to enable/disable each block-field unit. To minimize the impact on the neighboring TCAM logic, the insertion of dummy SEARCH operations start from the innermost TCAM block fields, and over multiple cycles, activates the outer TCAM block fields where *Ldi/dt* voltage collapse can cause timing fails in the logic surrounding the TCAM.

Since TCAM search operations activate all compare circuitry in parallel, the switching capacitance during a SEARCH operation is nearly ten times that of a READ/WRITE/NOOP operation on a 2K words and 640-bits-wide TCAM instance. This large delta in switching capacitance when going from SEARCH operations to non-SEARCH operations (or vice versa) causes a large *Ldi/dt* supply noise voltage spike. Fig. 14 shows the switching capacitance on the y-axis normalized to SEARCH operation for a variety of TCAM instances on the x-axis. The plot is a comparison for typical TCAM operation (READ, WRITE, and SEARCH) and the switching capacitance associated with each operation for HUM mode ON and OFF. When the HUM mode is ON dummy SEARCH operations are introduced during NOOP/READ/WRITE operations to reduce the switching capacitance by nearly eight times. The gradual transition from HUM to NOOP is controlled through CE input pin. When the CE signal is low, the TCAM is in a low-power mode with HUM mode OFF. The gradual wake-up pattern consists of activating the block fields which are at the center of the macro and then moving outwards over multiple cycles, reducing supply noise within the TCAM and surrounding logic. Fig. 15 shows the effect of a pattern consisting of 40 NOOP cycles followed by 100 HUM cycles, 100 SEARCH cycles, and 100 NOOP cycles consecutively. This plot shows the effect on the power-supply noise collapse when HUM mode is activated versus when HUM mode is OFF. Simulation results show that the usage of HUM mode results in 50% reduction in power supply noise compression.

The area associated with the multi-cycle di/dt noise reduction scheme, and all its control circuits does not increase the overall area of the TCAM macro because the necessary circuitry fits into an area that was previously occupied by filler cells required to match the bit-pitch subcircuits. Also, this architecture does not affect the performance of the TCAM as the control logic enabling the HUM mode is not a component of the circuitry of any critical paths.

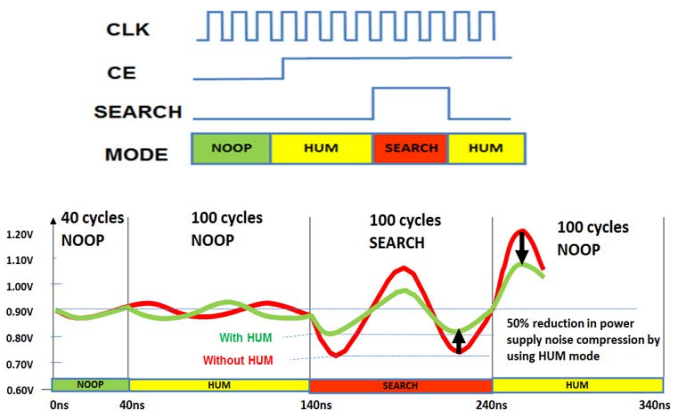


Fig. 15. Simulation result for a pattern of events on power supply. Peak-to-peak power-supply noise with and without HUM mode.

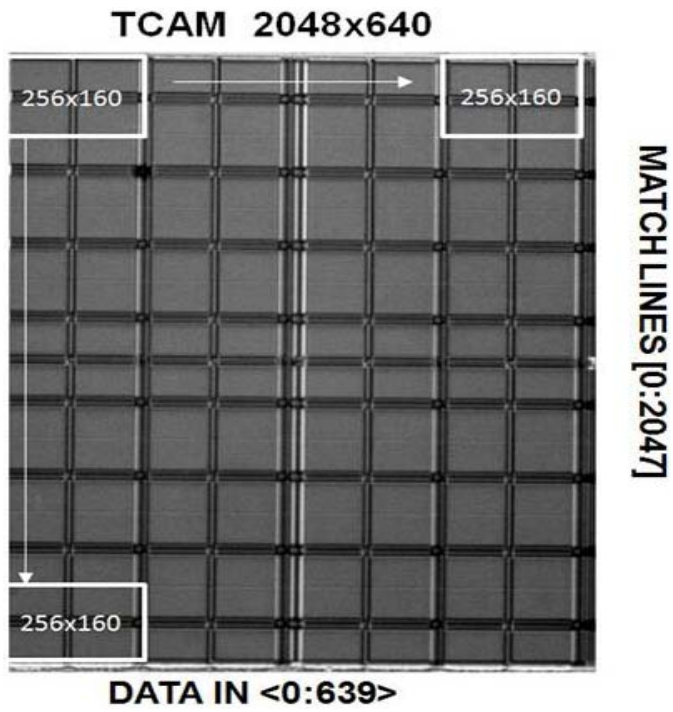


Fig. 16. Microphotograph showing a 2K × 640 TCAM fabricated in 14-nm FinFET technology.

While the HUM procedure does incorporate some additional non-functional cycles when going from NOOP state to operational state, this does not represent a significant burden to the system compared to the potential power noise problem it solves.

III. Hardware Results

The TCAM design in this test chip has a capacity of 1.310 Mb. At the macro level, it is arranged as 2048 entries with 640 bits per entry. This instance is arranged as a 16 × 4 matrix of 256 × 160-b individual block fields, fabricated in a 14-nm FinFET process spanning an area of 0.649 mm^2 to achieve a memory density of 2.01 Mb/mm^2. Fig. 16 shows the microphotograph of this TCAM macro. The instantaneous voltage observed on the on-chip supply

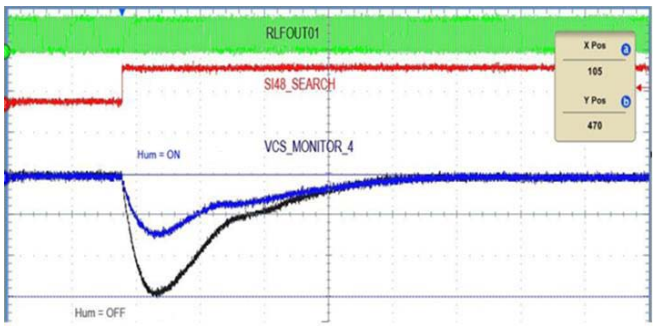
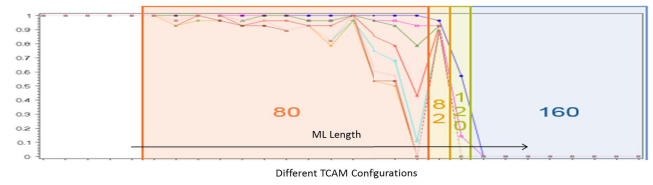
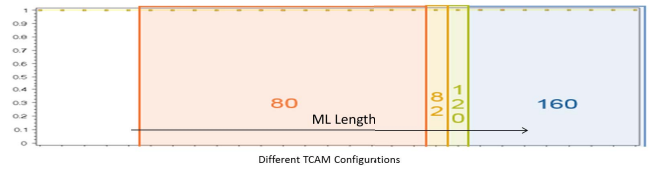


Fig. 17. Hardware result showing VCS supply collapse when SEARCH is active, with and without HUMM mode.



(a)



(b)

Fig. 18. Hardware showing yield improvement under pathological noise tests across extreme process splits with TPP-SRSS circuitry (a) disabled and (b) enabled.

monitors during a SEARCH operation is shown in Fig. 17 for HUM mode ON and OFF. For identical SEARCH activation, HUM mode pre-conditioned power supply shows 49% lower power-supply collapse. This agrees with the simulation results in Fig. 15 where there is 50% reduction in voltage collapse with HUM mode ON. From the power supply collapse noise measurement for the test-site configuration, it was observed that by enabling the TPP-SRSS circuit the power-supply noise was reduced by 49.7%, which agrees well with the simulation data as seen in Fig. 8.

Fig. 18 highlights the value of noise reduction scheme in the TCAM by showing the yield effects of shows pathological noise across extreme process splits with the TPP-SRSS circuitry disabled [Fig. 18(a)] and enabled [Fig. 18(b)]. This TCAM design is configurable by words, bits, and bits/ML, up to 2k words, 640 bits/word, and 160 bits/ML. Each ML is tested one at a time while all other MLs are configured to generate the maximum amount of noise. With the TPP-SRSS circuitry disabled, the yield drops off as the length of the ML increases. With the circuitry enabled, the pre-charge current for all the MLs with all-bit misses is greatly reduced, which reduces the power supply noise and completely recovers the yield.

Fig. 19 shows the McLeod [4] loop hardware measurement of this instance showing peak cycle time of 1.4 GHz at a VDD/VCS (logic supply to cell supply) of 0.80 V/0.90 V,

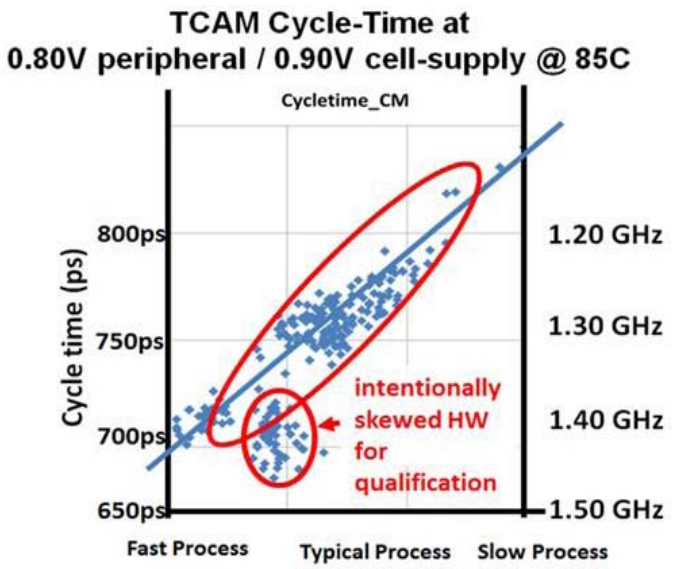


Fig. 19. McLeod loop measurements showing a 1.4-GHz maximum performance while consuming 580 mW of power.

TABLE I
COMPARISON WITH PREVIOUS STATE OF THE ART

	JSSC 2013 [2]	ISSCC 2014 [3]	VLSI 2015 [1]	This Work
Tech	32nm HKMG SOI	28nm HKMG	16nm Fin-FET	14nm Fin-FET
Density	0.84 Mb/mm2	0.61 Mb/mm2	1.80 Mb/mm2	2.01 Mb/mm2
Max Search Rate	1000 Msrch/s	400 Msrch/s	1250 Msrch/s	1400 Msrch/s
VDD VCS	0.95V -	0.85V -	0.80V -	0.80V 0.90V

85 °C while consuming 0.58 W of power. Table I provides a comparison of this work to previous state of the art with respect to density and performance.

IV. CONCLUSION

This design achieves a 15% higher performance, and 10% higher density than previous state of the art [1], and through the use of the two-phase pre-charge and HUM mode the load step on the power supply is reduced by 50%. As TCAM density and performance increase, power noise mitigation techniques such as the ones described in this paper will be of paramount importance.

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Igor Arsovski received the B.S. and M.S. degrees from the Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada, in 2001 and 2003, respectively.

He joined IBM, Essex Junction, VT, USA, in 2003, and moved to GLOBALFOUNDRIES in 2015. During the last 14 years, he has been the main architect of the TCAM compiler, responsible for the TCAM architecture and circuits from 90 to 7 nm. He is currently responsible for defining full PPA for the application specified integrated circuit memory offering, 2.5-D/3-D memory strategy, and IP definition for machine learning and automotive. He has authored or co-authored 15 papers and holds more than 80 patents, and is currently a Fellow in the GLOBALFOUNDRIES ASIC organization.

Akhilesh Patil received the B.Tech. degree in electronics and telecommunication engineering from the Vishwakarma Institute of Technology, Pune, India, in 2014, and the M.S.E. degree in electrical engineering from Arizona State University, Tempe, AZ, USA, in 2016.

He joined GLOBALFOUNDRIES, Essex Junction, VT, USA, in 2016 and since then he has been involved in ternary content-addressable memory circuit design and verification. His current research interests include custom circuit design, embedded memory compilers, and hardware architectures for machine learning and deep neural networks.

Robert M. Houle recieved the B.A. degree in mathematics and the B.S. degree in electrical engineering from the University of Vermont, Burlington, VT, USA, in 1974 and 1976, respectively, and the M.S. degree in electrical engineering from the University of Connecticut, Storrs, CT, USA, in 1980.

He was with IBM, Essex Junction, VT, USA, from 1980 to 2015, where he was involved in circuit design for microprocessors, with an emphasis on SRAM designs since 1996. He joined GLOBALFOUNDRIES, Essex Junction, in 2015, where he has worked exclusively in ternary content-addressable memory designs.

Michael T. Fragano received the B.S. and M.Eng. degrees in electrical engineering from Clarkson University, Potsdam, NY, USA, in 1995 and 1998, respectively.

In 1998, he joined the IBM Microelectronics Division, Essex Junction, VT, USA, where he has developed application-specific integrated circuit (ASIC) compilable memory arrays. He was involved in designing and leading the development of many generations of one-port SRAMs, multiport SRAMs, and ternary content-addressable memories (TCAMs). Since 2015, he has been with GLOBALFOUNDRIES, Essex Junction, VT, USA, where he has continued to lead the design and development of the ASIC TCAMs.

Ramon Rodriguez received the A.S. degree of Electrical Engineering Technology from Vermont Technical College, Randolph, VT, USA, in 1998.

He joined IBM, Essex, VT, USA, in 1998 as a VLSI Mask Layout Designer, where he continued as a Mask Layout Array Designer for single and multiport array designs until 2015. Since 2015, he has been with GLOBALFOUNDRIES, Essex Junction, VT, USA, where he is involved in ternary content-addressable memory layout design.

Raymond Kim received the B.S. and M.Eng. degrees from Cornell University, Ithaca, NY, USA, in 2005 and 2006, respectively.

In 2006, he joined the System and Technology Group, IBM, Endicott, NY, USA. He has been involved in several generations of custom circuit design, SRAM, and TCAM. Since 2015, he has been with GLOBALFOUNDRIES, Endicott, NY, USA, where he has been involved in application-specified integrated circuit memory group developing ternary content-addressable memory.

Van Butler received the B.Sc. degree in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, PA, USA, in 1999.

He is currently with Green Mountain Semiconductors on a contract to GLOBALFOUNDRIES. He was involved in circuit design and verification upon DRAM, SRAM, ternary content-addressable memory, and phase change memories.