

A Stacked CMOS Image Sensor With Array-Parallel ADC Architecture

Tomohiro Takahashi[✉], Yuichi Kaji, Yasunori Tsukuda, Shinichiro Futami, Katsuhiko Hanzawa, Takahito Yamauchi, Ping Wah Wong, Frederick T. Brady, *Member, IEEE*, Phil Holden, Thomas Ayers, Kyohei Mizuta, Susumu Ohki, Keiji Tatani, Hayato Wakabayashi, and Yoshikazu Nitta

Abstract—This paper presents a 4.1 megapixel, 280 frames/s, back-illuminated, stacked, global shutter (GS) CMOS image sensor with array-parallel analog-to-digital converter (ADC) architecture for region-control applications. The sensor solves an image distortion problem caused by rolling shutter in a pixel sub-array by utilizing a floating diffusion (FD) memory to implement GS operation. A newly developed circuit technique, the combination of active reset and frame correlated double sampling (CDS) operation, cancels V_{th} variation of pixel amplifier transistors as well as kTC noise. The active reset scheme suppresses output voltage variation of the pixel source follower. The chip supports 24-dB analog gain using a single-slope ADC and achieves 2.4e⁻ rms readout noise in the FD-memory-based GS. An intelligent sensor system with face detection derived from low-resolution images triggering high-resolution region-of-interest (ROI) output has been demonstrated with significantly reduced data bandwidth and low ADC power dissipation by utilizing the flexible area access function.

Index Terms—3-D integration, analog-to-digital converter (ADC), array-parallel ADC, back illuminated, block-parallel ADC, global shutter (GS), high frame rate, low noise, region control, region of interest (ROI), stacked.

I. INTRODUCTION

C MOS image sensors have evolved in performance with structures moving from basic front-illuminated and back-illuminated structures [1] to recent stacked structures [2]. The stacked structure enables tight integration of logic circuits as well as analog-to-digital converter (ADC) circuits, improving sensor performance and expanding sensor functionality [3]–[6]. The stacked structure is accomplished with 3-D integration techniques including wafer bonding [7], [8]. With regard to ADC architecture evolution, single ADC structures were used in charge-coupled device and initial CMOS image sensors. A column-parallel ADC architecture has been widely used for the past decade [9]. In an array-parallel ADC architecture, the ADCs are tiled under the pixel array,

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T. Takahashi, Y. Tsukuda, S. Futami, T. Yamauchi, K. Mizuta, S. Ohki, K. Tatani, H. Wakabayashi, and Y. Nitta are with Sony Semiconductor Solutions Corporation, Atsugi 2430014, Japan (e-mail: Tomohiro.B.Takahashi@sony.com).

Y. Kaji, K. Hanzawa, P. W. Wong, F. T. Brady, P. Holden, and T. Ayers are with Sony Electronics Inc., San Jose, CA 95112 USA.

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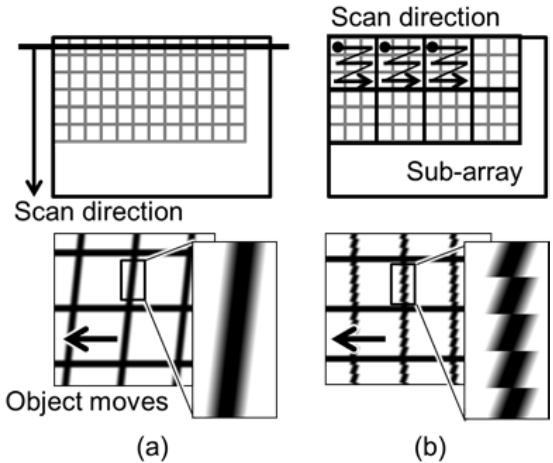


Fig. 1. Focal plane shutter distortion in (a) conventional column-parallel ADC architecture and (b) array-parallel ADC architecture.

an arrangement well suited for using a stacked structure for highly parallel readout. Only a few hundred pixels per ADC are readout to capture a whole image in the array-parallel ADC architecture, whereas thousands of rows of readout are needed in the conventional column-parallel ADC architecture. The array-parallel ADC performs massively parallel readout and significantly higher frame rate. In addition, the frame rate remains constant for various pixel resolutions and optical formats in the array-parallel ADC architecture because of its modularity [10], [11], [28].

A major problem with implementing an array-parallel ADC architecture is image distortion. Rolling shutter (RS) operation causes image distortion because the scan direction in conventional column-parallel ADCs moves from top to bottom. Focal plane distortion appears in an image when moving objects are captured as shown in Fig. 1(a). The scan direction in the proposed array-parallel ADC architecture from the first pixel to the last pixel is shown in Fig. 1(b). Focal plane distortion now appears inside a sub-array. It is difficult to correct this artifact as it is impossible to restore the lost information at the boundaries between sub-arrays. Post-processing of the image has limited success in correcting this type of focal plane distortion. Global shutter (GS) operation is, therefore, essential to remove this distortion in the array-parallel ADC architecture.

There are multiple types of GS techniques depending on how the memory elements are included in the pixel. We selected a floating diffusion (FD) memory as a storage

node instead of in-pixel memory. As compared to in-pixel memory, the FD memory has advantages regarding sensitivity, full-well capacity, and smaller pixel implementation with high fill factor because the memory size is smaller than that of in-pixel memory. Since it is difficult to completely cover the memory node with a light shield layer in the back-illuminated device structure, the smaller FD memory has better parasitic light sensitivity (PLS) performance than that of an in-pixel memory structure. The deterioration of PLS due to back-illuminated device can be suppressed by reducing A/D conversion times for single-frame readout in the array-parallel architecture.

One drawback of the FD-memory-based GS pixel is large temporal noise due to kTC noise [12]. Correlated double sampling (CDS) techniques widely used in single-slope ADCs (SS-ADCs) [9] cannot be applied to FD-memory-based GS because an FD reset operation before signal-level readout destroys stored signal electrons. A delta reset sampling (DRS) scheme that FD reset and reset level readout are performed after signal-level readout is used for FD-memory-based GS readout. A sample-and-hold approach to eliminating the pixel V_{th} variation has been proposed for the array-parallel architecture [13]–[15]. kTC noise still remains because of DRS operation. Soft reset and tapered reset approaches are applied to suppress reset noise [16], [17]. In these approaches, the feedback amplifier must be carefully designed to get high feedback gain achieving reset noise reduction. A new approach called capacitive-coupled noise cancelling has presented recently [18]. It suppresses reset noise well, but does not cancel kTC noise completely. It needs an extra one transistor and two capacitors inside each pixel, which degrades fill factor and becomes an obstacle to smaller pixel implementation for general silicon image sensor.

We proposed a new readout technique that combines active reset and frame CDS operation to address this drawback [19]. Active reset suppresses V_{th} variation of pixel amplifier transistors using a negative-feedback loop. That supports high analog gain settings of SS-ADC. Reset noise including kTC noise and V_{th} variation is cancelled by frame CDS. The combination of both schemes makes it possible to implement an array-parallel readout without image distortion while achieving high frame rate and low noise. The stacked chip with these improvements in an array-parallel ADC architecture was fabricated and successfully demonstrates GS operation.

The proposed array-parallel ADC architecture is applicable to Internet of Things (IoT) and edge computing perspective. A typical cloud-based system has problems such involving latency, network bandwidth, and storage cost because many cameras are streaming huge amounts of data. Therefore, edge computing that edge devices themselves perform some of processing workload can help to address these problems. Image sensors and camera system will become smarter and more intelligent. One important capability for smarter systems is a region-of-interest (ROI) function. ROI delivers only the data you need when it is needed, reducing system power consumption, enhancing processing speed, addressing network bandwidth limitation, and reducing data storage cost without impacting information quality. Image sensors should be able to

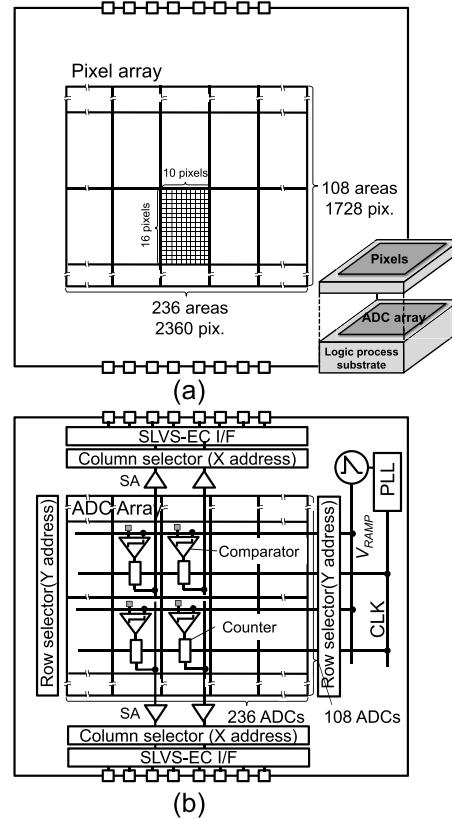


Fig. 2. Sensor block diagram with array-parallel ADC architecture. (a) Top chip. (b) Bottom chip.

adaptively control or change ROI data. For example, the sensor can output multiple ROIs and change each ROI window size frame by frame. The array-parallel ADC architecture is well suited to such a region-control sensor. This architecture offers flexible ROI control and sub-array control functions per region that are useful for surveillance and factory automation applications.

The remainder of this paper is organized as follows. Section II describes the detailed configuration of the array-parallel ADC architecture and the proposed circuit techniques. The combination of the active reset and frame CDS is presented. In Section III, experimental results of the developed sensor are shown and noise visibility is discussed. In Section IV, an intelligent system is presented for proof of concept of a region-control application. Finally, Section V summarizes the conclusion.

II. ARRAY-PARALLEL ADC ARCHITECTURE

A. Sensor Architecture

Fig. 2 shows a block diagram of the stacked sensor with array-parallel ADC architecture. As shown in Fig. 2(a), the top chip comprises the pixel array (2360×1728 pixels). The pixel array is separated into 236×108 sub-arrays, each sub-array containing 160 (10×16) pixels. As shown in Fig. 2(b), the bottom chip consists of an ADC array, a column selector, a row selector, a ramp generator, a phase-locked loop (PLL), sense amplifiers (SAs), and interfaces. The ADC array is composed

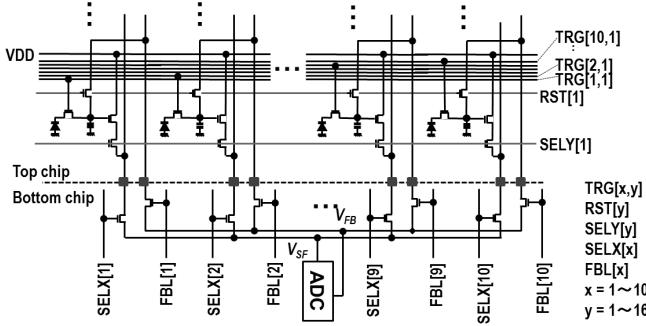


Fig. 3. Circuit diagram for sub-array control function.

of 236×108 individual ADCs, matching the number of pixel sub-arrays. The ADC uses an SS-ADC architecture. The ADC includes the current source for the pixel source follower load, a comparator, and a counter. A voltage ramp V_{RAMP} and an ADC clock CLK are generated by the ramp generator and the PLL, respectively. Both V_{RAMP} and CLK are distributed throughout the ADC array. V_{RAMP} wire is mesh structure to decrease parasitic resistance. CLK line is buffered at the edge of each ADC row. Each ADC is connected to the corresponding pixel sub-array and pixel output. The converted digital data are transferred from the ADC array to the interfaces by SAs. The sensor has a 16-channel output interface, each interface capable of 4.752 Gb/s per channel using a scalable low-voltage scaling interface with an embedded clock (SLVS-EC).

B. Sub-Array Control Function

The developed sensor has a flexible sub-array control function that can select a readout pixel position from within the 160 pixels and change their readout order by x - y address control signals from the column and row selectors. The sensor can also change the number of pixels read out; thus, it can set various scan directions and subsampling readout order. Fig. 3 shows the circuit diagram for the sub-array control function. The pixel utilizes a basic 4-Transistor (4T) structure. Each pixel contains a photodiode, a charge transfer gate, a charge storage node (FD memory), a reset transistor, a source follower amplifier, and a pixel select transistor. An extra overflow gate is required for the electrical shutter control at the beginning of the exposure period during background ADC operations [12], [15], [26].

Flexible pixel access is realized by x - y address controls implemented by both common horizontal control signals and vertical control signals. The horizontal control signals are implemented in the top chip, and the vertical control signals are implemented in the bottom chip. The pixel outputs are connected by vertical readout path V_{SF} in each column, and readout rows are selected by the conventional horizontal select line $SELY[y]$. An additional transistor is added to each vertical readout path, and columns are enabled by vertical select line $SELX[x]$. The vertical readout paths are mixed together onto V_{SF} . In this way, each pixel can be selected by activating the corresponding transistors controlled by horizontal $SELY[y]$ and vertical $SELX[x]$ lines, where x and y are the index representing horizontal and vertical pixel positions in a sub-array,

respectively ($x = 1\text{--}10$ and $y = 1\text{--}16$). There is a feedback path V_{FB} used to perform active reset. Similarly, individual pixel feedback can be selected by horizontal reset line (RST)[y] and vertical feedback loop line (FBL)[x]. An additional transistor is added to each vertical feedback path, and column feedback is selected by vertical FBL[x]. The vertical feedback V_{FB} is connected to the drain of the pixel reset transistor, and each row feedback is enabled by RST[y]. Two connections for the readout path and the feedback path are put per pixel pitch horizontally and per sub-array pitch vertically.

The ten pixels in a row of the sub-array have independent transfer gate control signals, transfer gate control signal (TRG)[x, y], running horizontally for RS operation. This independent shutter operation drives the pixel pitch of $4.8 \mu\text{m}$. The TRG wires can be combined together and the pixel pitch can reduce if only GS operation is required.

C. Active Reset Scheme With SS-ADC

The key techniques used to overcome reset noise in an FD-memory-based GS pixel are active reset with SS-ADC and frame CDS. Fig. 4 shows the proposed technique. The circuit structure of the active reset scheme is shown in Fig. 4(a). A negative-feedback loop is formed by connecting the output of feedback amplifier to the drain of the RST transistor. The pixel source follower output V_{SF} is very close to V_{REF} as long as the gain of the feedback amplifier is sufficiently large [20]. This negative-feedback loop counters V_{th} variation of the pixel amplifier transistor and is stored into each FD memory. After turning off the RST transistor, reset noise including kTC noise and reset feedthrough variation are also stored into the FD memory. Fig. 4(b) illustrates a timing diagram for the proposed FD-memory GS readout. A reset frame is assembled by reading the dark level at every pixel before transferring signal charge from photo diode (PD) to FD memory. A data frame is readout by reading signal level at every pixel after simultaneous transfer to the FD memory. Noise written into each pixel can be independently and completely cancelled with a frame CDS operation. Moreover, this feedback amplifier is the same circuit used in the comparator of the SS-ADC. The circuit can be shared because the feedback amplifier does not need careful gain tuning; it simply needs to be sufficiently large. The gain of the feedback amplifier is 47 dB. This flexibility and reuse help to keep ADC area small. Reducing ADC area can decrease the number of pixels in a sub-array providing faster frame rate.

Although noise and variations written into FD memory can be cancelled only by frame CDS operation, the benefit of an active reset scheme is high gain setting capability in the SS-ADC. Fig. 5(a) depicts the conventional 4T pixel structure without active reset. After turning off the RST gate, kTC noise and feedthrough variation appear in the voltage of the FD-memory V_{FD} . The voltage output of the pixel source follower V_{SF} reflects V_{th} variation of the individual pixel amplifier transistors so that the voltage spread of V_{SF} with no signal becomes large. The ramp voltage cannot cover this wide voltage distribution at high gain. In contrast, Fig. 5(b) shows the proposed active reset circuit. V_{FD} stores the V_{th} variation

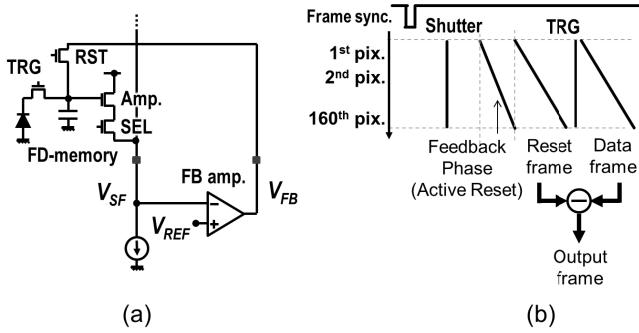


Fig. 4. Concept of active reset scheme and frame CDS combination. (a) Circuit diagram of active reset based on negative-feedback circuit. (b) Simplified timing diagram of FD-memory-based GS.

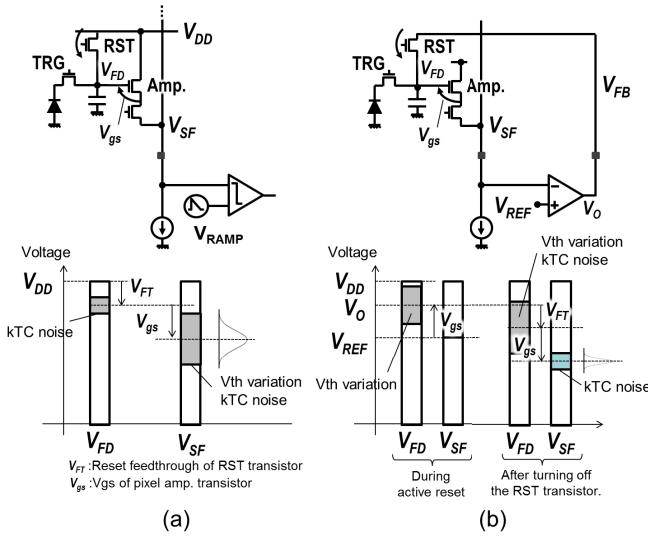


Fig. 5. Voltage diagram comparison between (a) conventional 4T pixel structure and (b) proposed active reset circuit structure.

of the pixel amplifier transistor so that V_{SF} approaches a constant V_{REF} by the negative-feedback loop. While the voltage range of V_{FD} is wide, the voltage range of V_{SF} becomes considerably narrowed after turning off the RST gate. As a result, the active reset scheme makes it possible to use high-gain settings when using small ramp swing in the SS-ADC.

D. Timing Chart

Fig. 6 shows a detailed timing chart of the proposed FD-memory-based GS readout. There are three phases: 1) feedback phase; 2) reset frame phase; and 3) data frame phase. Each phase consists of a combination of five circuit operations: auto zero (AZ), active reset, reference voltage V_{REF} readout (REF), dark-level readout (DK), and signal-level readout (SIG).

- 1) *Feedback Phase:* AZ and AR are performed independently within every pixel. The role of AZ is to cancel comparator offset. V_{REF} is sampled onto the capacitor on the ramp input to the comparator input. The purpose of the AR operation is to store the V_{th} variation of the pixel transistors into the FD memory as described in Section II-C. The negative-feedback loop works to

reduce the impact of V_{th} variation of these pixel transistors, which allows the use of a large 24-dB analog gain setting. After turning off the reset transistor, kTC noise is stored in the FD memory. V_{FD} can be changed for each gain setting by V_{REF} to suppress dark current levels.

- 2) *Reset Frame Phase:* AZ, REF, and DK are performed during the reset frame phase. The reset frame readout is performed with dual CDS [9]. The AZ operation uses analog CDS. The REF and DK operations use digital CDS. V_{REF} is read during REF time, and the dark level is read during DK time. Local CDS is performed by subtracting the output of REF from that of DK by the SS-ADC. The purpose of local dual CDS is to eliminate lower frequency noise effects.
- 3) *Data Frame Phase:* AZ, REF, and SIG are performed after transferring signal charge from the PD to the FD. The data frame readout is also performed with dual CDS. V_{REF} is read during REF time, and the signal level is read during SIG time. Finally, frame CDS is accomplished by subtracting the reset frame from the data frame.

The number of pixels read out from a sub-array is 160. The resolution of SS-ADC is 12 bit. The counter operates at 891 MHz, which allows 1.782-GHz counting. The total A/D conversion time of each pixel including the feedback phase, the reset frame phase, and the data frame phase is 22.14 μ s. The time delay between the reset frame and the data frame is 2.08 ms. Although the timing of the dark-level readout and the timing of the signal-level readout are separated from each other, kTC noise and V_{th} variation of the pixel amplifier transistors can be cancelled with frame CDS. To shorten the ADC time is important future work.

III. EXPERIMENTAL RESULTS

A. Fabricated Chip Specification

Fig. 7 shows microphotographs of the top and bottom chips. The top chip is a sensor chip fabricated with 90-nm one-poly-Si four-metal-layer image sensor process technology and includes the pixel array of 2360×1728 pixels. The number of effective pixels is 2300×1536 . The pixel pitch is 4.8 μ m. Sensitivity is $28\ 400e^-/lx \cdot s$. The bottom chip is a logic chip fabricated with 55-nm one-poly-Si seven-metal-layer CMOS process technology. The SAs and the interfaces are located on two sides of the chip as shown. Pixel data on the each side of the array are separately transferred to its corresponding SLVS-EC I/O. The frame memory to store the reset frame for frame CDS operation is outside of this stacked chip.

B. Noise Visibility

Visible noise in the output of the image using the array-parallel ADC architecture is discussed in this section. Column random noise (RN), column fixed pattern noise (FPN), row temporal noise (RTN), and row FPN observed in the conventional column-parallel ADC architectures look quite different in the array-parallel architecture. Fig. 8 shows a noise appearance comparison between the column and row

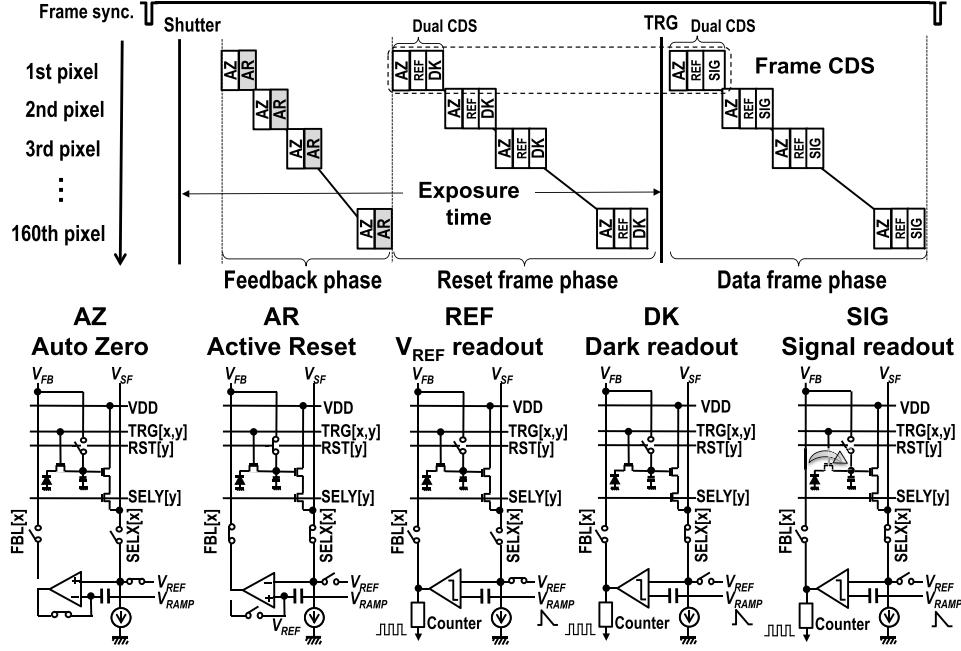


Fig. 6. Timing diagram for five circuit operations: AZ, active reset, V_{REF} readout, dark readout, and signal readout.

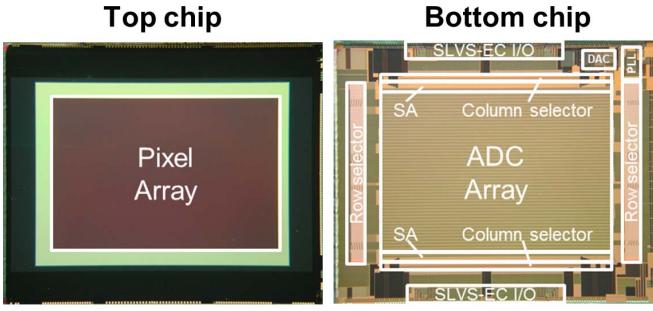


Fig. 7. Chip microphotographs: top sensor chip and bottom logic chip.

noises in the conventional column-parallel ADC architecture devices and the block and phase noises in the array-parallel ADC architecture. In the conventional column-parallel ADC architectures, vertical-line noise, column RN, and column FPN are caused by ADC variation. Therefore, ADC variation in a column-parallel architecture looks block RN and block FPN in an array-parallel ADC architecture. Because horizontal-line noises such as RTN and row FPN are caused by temporal signal vibration, it appears as phase RN and phase FPN in an array-parallel ADC architecture.

Fig. 9 shows simulated images to assess the impact of noise sources. The noise ratio of total RN and block RN is swept in the upper row of the table, and the noise ratio of total RN and phase RN is swept in the bottom row of the table. The size of a sub-array is 18×18 pixels in this simulation, slightly different than our implementation. Images with a noise ratio of total RN to column RN and RTN of 1/4 are shown for comparison. This image simulation shows that block noise has almost the same impact as column noise, whereas phase noise is less visible than the row noise at the same noise

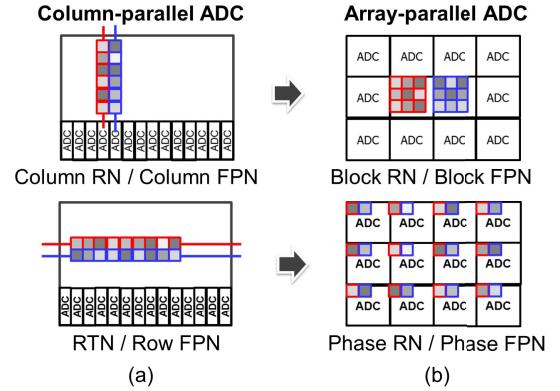


Fig. 8. Appearance of (a) column and row noises in the conventional column-parallel ADC architecture and (b) block and phase noises in the array-parallel ADC architecture.

ratio of 1/4. Because pixels read out simultaneously are not adjacent to each other in the array-parallel architecture. In other words, RTN requirements can be relaxed. N. B. noise criteria are not uniquely determined because they are determined by individual sensory evaluation of the human eye.

C. Chip Performance

Fig. 10 shows the effectiveness of the active reset scheme. The both graphs in Fig. 10 are measured in dark condition. The graph in Fig. 10(a) represents output signal distributions of the reset frame centered on their mean values under the conditions of active reset ON and OFF. The standard deviation with the active reset scheme enabled is $3.8 \text{ mV}_{\text{rms}}$, while it is $12.3 \text{ mV}_{\text{rms}}$ without engaging the active reset scheme. It is a realistic distribution to use a high-gain setting of 24 dB in the SS-ADC. The graph in Fig. 10(b) represents the output signal distribution of the output frame after frame CDS. The standard

	Column-parallel ADC	Array-parallel ADC			
Column RN vs Block RN					
RTN vs Phase RN					

Fig. 9. Noise comparison using simulated images with a different block RN and phase RN ratio to total RN.

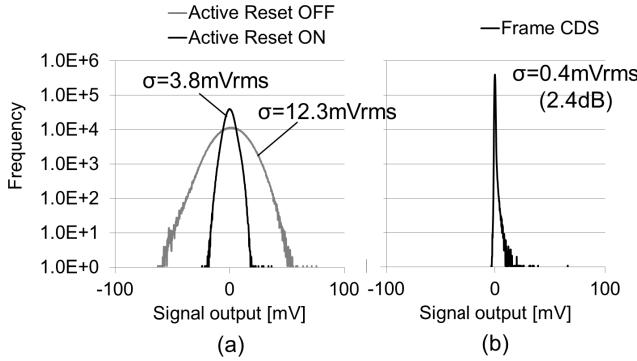


Fig. 10. Output signal distributions of (a) reset frame and (b) output frame after frame CDS centered by their mean values.

deviation has been decreased to $0.4 \text{ mV}_{\text{rms}}$ at an analog gain of 2.4 dB.

Fig. 11 shows the measured total RN and analog gain dependence under dark conditions in both RS mode and GS mode. The total RN in GS operation mode is $2.4\text{e}^{-}_{\text{rms}}$ at an analog gain of 24 dB due to the active reset scheme. The total RN in RS operation mode is also measured for comparison. The total RN in GS operation mode is almost exactly the square root of 2 times larger than that of RS operation mode. The main reason is that the proposed technique twice performs dual CDS operation in forming both reset and data frames. Thus, the number of samples increases by 2 times and noise is reduced by the square root of the number of samples. Additionally, the total RN of GS operation is affected by increasing $1/f$ noise and dark current shot noise due to the time difference between reset and data frame acquisition. Local dual CDS suppresses some lower frequency noise sources. The total RN of GS operation could be improved if the time difference between reset and data frames is reduced by shrinking the ADC size and decreasing the number of readout pixels by a single ADC.

Fig. 12 shows the measured sensor linearity. The horizontal axis is normalized exposure time, and the vertical axis shows

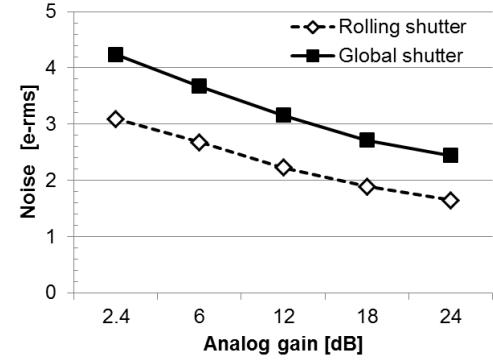


Fig. 11. RN characteristic.

12-bit sensor output codes for the pixel signal level. Nonlinearity is shown on the vertical axis and is within 0.33% of full scale. Table I summarizes the chip characteristics. A frame rate of 630 frames/s for RS readout and 280 frames/s for GS readout has been achieved. Total power consumption at full frame rate is 1.37 and 1.34 W in RS readout and GS readout modes, respectively. Intermittent readout at 60 frames/s can decrease the consumption to 0.46 and 0.51 W in RS readout and GS readout modes, respectively. The measured differential nonlinearity is under ± 0.3 LSB and measured integral nonlinearity is under 0.21% in RS readout and 0.33% in GS readout. The conversion gain of the pixel is $65 \mu\text{V/e}^{-}$. Total RN is $1.7\text{e}^{-}_{\text{rms}}$ in RS readout mode and $2.4\text{e}^{-}_{\text{rms}}$ in GS readout mode, with both at a 24-dB analog gain. Measured values of block RN and phase RN are 0.09 and $0.11\text{e}^{-}_{\text{rms}}$, respectively, in RS readout mode, while they are 0.14 and $0.20\text{e}^{-}_{\text{rms}}$, respectively, in GS readout mode. The ratio of total RN to both block RN and phase RN in both modes are sufficient to yield excellent images.

D. Performance Comparisons

Captured images in both RS readout and GS readout modes are shown in Fig. 13. Both images are captured from the same sensor. The focal plane distortion inside a sub-array

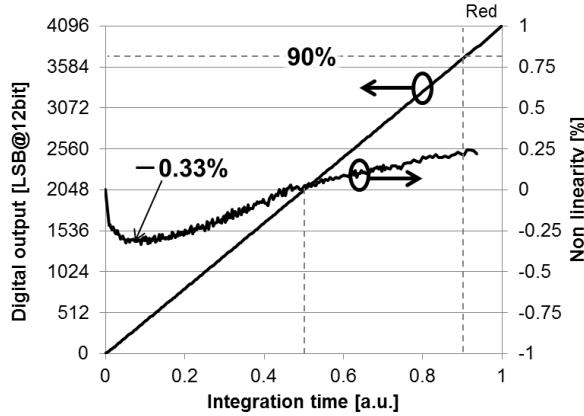


Fig. 12. Sensor linearity characteristic in FD-memory GS mode.

TABLE I
CHIP CHARACTERISTICS

	Rolling shutter	Global shutter (FD-memory)
Process	Top: 90nm 1Poly-4Metal Bottom: 55nm 1Poly-7Metal	
Supply voltage	2.9V/1.2V/1.1V	
Pixel size	4.8um(H) x 4.8um(V)	
# of effective pixels	2300 (H) x 1536 (V)	
# of total pixels	2360 (H) x 1728 (V)	
Sensitivity	28400e- lx/s	
Frame rate	630fps	280fps
Power dissipation	1.37W (630fps) 0.46W (60fps)	1.34W (280fps) 0.51W (60fps)
DNL	< ± 0.3LSB	
INL	< 0.21%	< 0.33%
Conversion gain	65uV/e-	
Total random noise	1.7e-rms (24dB)	2.4e-rms (24dB)
Block random noise	0.09e-rms (24dB)	0.14e-rms (24dB)
Phase random noise	0.11e-rms (24dB)	0.20e-rms (24dB)
Dynamic Range	71.8dB (2.4dB)	69.0dB (2.4dB)
Output interface	4.752Gbps/ch. X 16 SLVS-EC	

in RS readout mode is successfully eliminated with the proposed FD-memory-based GS readout mode. Table II compares recent back-illuminated GS sensor performance [21]–[26]. The organic film sensor of [25] is not a back-illuminated sensor. However, the organic photoconductive film does not constrain interconnect in the pixels as with the back-illuminated sensors. Frame rate and total readout RN of this paper are superior to these of other sensors. Sensitivity of this sensor is better than that of the front-illuminated GS sensor [26] because of the back-illuminated structure.

IV. REGION-CONTROL APPLICATIONS

The array-parallel ADC architecture has two unique features. The first one is fine ADC power control in ROI readout as shown in Fig. 14. ADC activation and standby in ROI readout mode are controlled by ADC block row and column wires. Power management is easier than the column-parallel ADCs because it is enough to operate ADCs corresponding to readout ROIs, and the other ADCs can be in standby.



Fig. 13. Captured images of the fabricated array-parallel ADC sensor in RS and GS modes.

TABLE II
PERFORMANCE COMPARISONS

	This work	[21] 2016	[22] 2016	[23] 2016	[24] 2011	[25] 2016	[26] 2016
Chip structure	BI Stacked	BI Stacked	BI Stacked	BI	BI	FI+OPF	FI+CoC
Pixel pitch [μm]	4.8	6.6	3.8	3.75	5.5	3.0	5.86
Storage Node for GS	FD	Digital DRAM	Cap.	Cap.	Cap.	FD	Mem.
# of pixels(H)	2360	644	4608	1024	4Mpix.	1920	3840
# of pixels(V)	1728	480	3480	800		1080	2160
Sensitivity [e-/lx·s]	28400	N/A	35000 (hole)	N/A	N/A	N/A	17500
Frame rate [fps]	280	129	5	50	45	60	480
Random noise [e-rms]	2.4	N/A	10 (hole)	8.5	10	4.4	3.3
Dynamic range [dB]	69.0	N/A	70.9	59	62.6	81.3	76.3

Bi: Back-illuminated, FI: Front-illuminated, OPF: Organic photoconductive film, CoC: Chip on chip

ADC power control

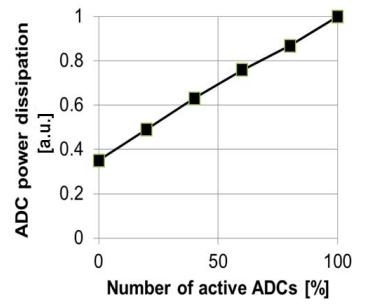
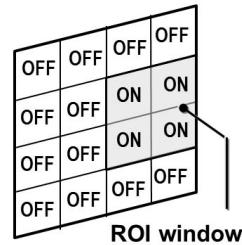


Fig. 14. ADC power management in ROI readout.

It is desirable to avoid ADC activation at every row readout from the view point of analog signal settling in the ADC circuitry and block level uniformity. The operated ADCs can be changed frame by frame in the proposed array-parallel ADC architecture, while they have to be changed line by line in the conventional column ADC architecture [27]. The second one is high-speed low-resolution image creation because the 2-D image can be readout at one ADC operation.

One of the region-control sensor applications, an intelligent sensor system with face detection and a high-resolution ROI output has been demonstrated as a proof-of-concept as shown in Fig. 15. The ROI window is detected using

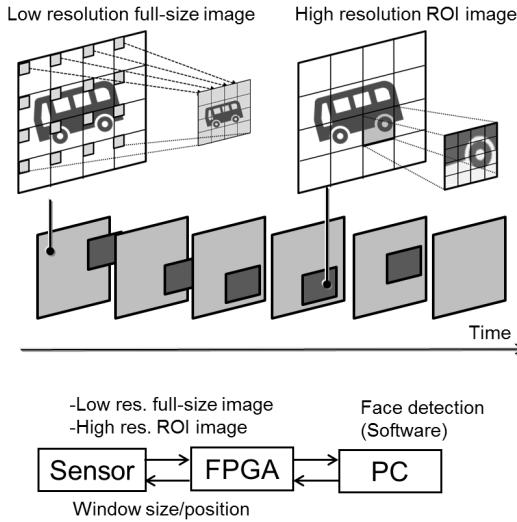


Fig. 15. Intelligent sensor system with face detection from low-resolution images and high-resolution region-of-interest output.

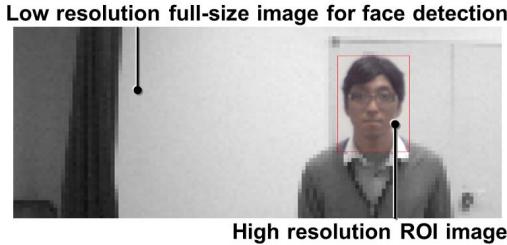


Fig. 16. Captured image combining high-resolution ROI image within extended low-resolution full-size image.

TABLE III
SYSTEM SPECIFICATION

Low resolution	Subsampling x10
High resolution for ROI	Full resolution x1
Face detection Algorithm	Based on OpenCV (Viola-Jones algorithm)
Number of ROI Windows	1
Minimum ROI size	20x20 pixels
Maximum ROI size	Full resolution
Output frame rate	30fps
Sensor frame rate	60fps (Maximum 280fps) Low res. 30fps High res. 30fps
Monitoring function	Data rate Stored data ADC power dissipation

low-resolution full-scale images. Then, the sensor outputs only an ROI image with high resolution. Low-resolution full-scale images and high-resolution ROI images are alternative output in this system. Fig. 16 shows the captured image of the system combining a high-resolution ROI image within the low-resolution full-scale image. The system specification is summarized in Table III. Power dissipation of the sensor

can be managed spatially and temporally. The system reduces required data bandwidth by over 10 \times compared to full-scale full-resolution output, while maintaining all critical information in the detected face.

V. CONCLUSION

Stacked CMOS image sensor with array-parallel ADC architecture has been proposed and demonstrated. This architecture enables massively parallel readout and flexible pixel control in sub-arrays. The key technology is the combination of an active reset scheme and frame CDS. This technique cancels pixel reset noise and allows high analog gain of 24 dB. As a result, 4.1 megapixel, 280 frames/s, back-illuminated, stacked, GS sensor with 2.4e $^{-}$ rms readout noise is realized. The smart ROI system dramatically extends the range of computer vision applications in an IoT world by utilizing this region-control-oriented sensor.

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Tomohiro Takahashi received the B.E. degree in communications engineering, the M.S. degree in information sciences, and the Ph.D. degree in communications engineering from Tohoku University, Sendai, Japan, in 2001, 2003, and 2006, respectively. He was a Post-Doctoral Fellow with the Japan Society for the Promotion of Science. He joined Sony Corporation, Atsugi, Japan, in 2007. He has been involved in the design and development of CMOS image sensors. His current research interests include an analog circuit design, an A/D converter, and sensor architectures.



Yuichi Kaji received the B.E. degree in electronics engineering from Kyushu University, Fukuoka, Japan, in 1999.

In 1999, he joined Sony LSI Design Inc., Atsugi, Japan, and is involved in the development of CMOS image sensors.



Yasunori Tsukuda received the B.S. and M.S. degrees in electronic engineering from Kobe University, Kobe, Japan, in 2001 and 2003, respectively.

In 2007, he joined Sony Corporation, Atsugi, Japan, and is involved in phase-locked loop design and the development of CMOS image sensors.



Shinichiro Futami received the B.S. degree in applied physics from the Tokyo Institute of Technology, Tokyo, Japan, in 1992.

He joined Sony Corporation, Atsugi, Japan, in 2000, and has been involved in the development of security large-scale integration and CMOS image sensors.



Katsuhiko Hanzawa received the B.S. and M.S. degrees in electronic engineering from Tohoku University, Sendai, Japan, in 2010 and 2012, respectively.

In 2012, he joined Sony Corporation, Atsugi, Japan, and has been involved in the development of CMOS image sensors.



Takahito Yamauchi received the M.S. degree in electronic engineering from Kobe University, Kobe, Japan, in 2014.

In 2014, he joined Sony Corporation, Atsugi, Japan, and is involved in the development of CMOS image sensors.



Ping Wah Wong received the B.Sc. (Eng.) degree from The University of Hong Kong, Hong Kong, in 1977, the M.S.E.E. degree from the University of Michigan–Dearborn, Dearborn, MI, USA, in 1985, and the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, USA, in 1989.

He was an Assistant Professor at Clarkson University, Potsdam, NY, USA, from 1989 to 1992. He was at research laboratories and product development units of companies including Coronet Industries, Mass Transit Railway, Hewlett Packard, Nethra, Insilica, Pixim, and Sony. He is currently with Sony Electronics Inc., San Jose, CA, USA, focusing on signal processing for image sensors. His current research interests include signal processing, data security, compression, and communications.

Dr. Wong was an Associate Editor of the *IEEE TRANSACTIONS ON IMAGE PROCESSING* from 1995 to 1997, and the *Electronic Imaging* from 2000 to 2012. He was a Co-Chair of the SPIE Conference on Security and Watermarking of Multimedia Contents from 1999 to 2009.



Frederick T. Brady (M'85) received the B.S. degree in physics from the New Mexico Institute of Mining and Technology, Socorro, NM, USA, in 1985, and the Ph.D. degree in electrical engineering from the University of Florida, Gainesville, FL, USA, in 1991.

Since 2013, he has been a Senior Manager of CMOS image sensor design and characterization with Sony, Rochester, NY, USA. He has authored 40 papers on various semiconductor topics and holds 25 patents. His current research interests include the design and evaluation of novel sensors.



Phil Holden received Degrees in electrical/industrial design, mathematics, and computer engineering from Sussex University, Brighton, U.K.

From 1988, he has been in Silicon Valley at companies such as Chromatic Research, C-Cube, and Pixim. Since 2012, he has been the Vice President of systems engineering with Sony-ISDC, San Jose, CA, USA.



Thomas Ayers received the B.S. and M.S. degrees in electrical engineering from the University of New York, Buffalo, NY, USA, in 1987 and 1989, respectively.

He was a Software Engineer at General Electric from 1989 to 1993. He was a DSP Software and an ASIC Hardware Design Engineer at Divicom from 1993 to 1995. He was a Systems Hardware and an SOC ASIC Design Engineer and a Manager/Director at C-Cube Microsystems from 1996 to 2000. He was the Vice President and an Engineer at Believe and Broadlogic from 2003 to 2006. He was the Vice President and an Engineer at Pixim and Sony from 2007 to 2014. Since 2014, he was the Vice President with the Image Sensor Design Center, Sony, San Jose, CA, USA.



Kyohei Mizuta received the M.S. degree in materials science and engineering from Yokohama National University, Yokohama, Japan, in 2007.

In 2007, he joined Sony Corporation, Atsugi, Japan. He has been involved in the development of CMOS image sensors.



Susumu Ohki received the M.S. degree in electrical and electronic engineering from Tokyo Metropolitan University, Tokyo, Japan, in 2002.

In 2004, he joined Sony Corporation, Atsugi, Japan, and is involved in the development of CMOS image sensors.



Keiji Tatani received the M.S. degree in physics from Osaka University, Osaka, Japan, in 2000.

In 2003, he joined Sony Corporation, Atsugi, Japan, and is involved in the development of CMOS image sensors. He is currently a General Manager with Sony Semiconductor Solutions Corporation, Atsugi, leading research and development of CMOS image sensor.



Hayato Wakabayashi received the B.E. and M.E. degrees in engineering science from Osaka University, Osaka, Japan, and the Ph.D. degree from Tohoku University, Sendai, Japan.

He joined Sony Corporation, Atsugi, Japan, in 2004, and moved to Sony Electronics Inc., San Jose, CA, USA, in 2016, where he has involved in the development of CMOS image sensor.

Dr. Wakabayashi is currently a Technical Program Committee Member of ISSCC.



Yoshikazu Nitta received the B.S. and M.S. degrees in electronic engineering from Tohoku University, Sendai, Japan, in 1986 and 1988, respectively.

From 2006 to 2016, he was with Sony Corporation, Atsugi, Japan, where was involved in the development of CMOS image sensors. Since 2016, he has been with Sony Semiconductor Solutions Corporation, Atsugi, where he is currently an in charge of technology development of CMOS image sensor.