A 0.8-V Resistor-Based Temperature Sensor in 65-nm CMOS With Supply Sensitivity of 0.28 °C/V

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***Abstract*— A 0.8-V resistor-based CMOS temperature sensor in 65-nm CMOS process with low supply sensitivity is presented. The temperature-to-voltage conversion gain is maximized by utilizing two types of on-chip resistors with positive and negative temperature coefficient. Reusing the resistor sensor frontend as a reference, the voltage generator of the subsequent A/D converter inherently removes the supply dependence of temperature-to-digital conversion. A 10-bit sub-ranging A/D converter employing 5-bit amplifying interpolation D/A converter enables low-voltage and low-noise A/D conversion. Over a range of −45 °C ∼ 85 °C, the proposed sensor achieves 0.12 $°C_{rms}$ temperature resolution with a conversion time of 10 μs. After a 2-point calibration, the sensor achieves an inaccuracy of less than +1.6/−1 °C while consuming 47 μW from 0.8-V supply voltage. Measured supply sensitivity is 0.28 °C/V over 0.6 ∼1.2 V, which is one of the lowest ever reported among sub-1-V temperature-to-digital converter designs.**

***Index Terms*— Low supply sensor, ratiometric sensing, resistor-based temperature sensor, supply insensitive temperature sensor.**

I. Introduction

A CMOS temperature sensor has traditionally been designed using a bipolar junction transistor (BJT) by taking the advantage of linear temperature-to-voltage relation in the difference of two base–emitter voltages [1]–[5]. While showing high linearity and accuracy, the BJT-based temperature sensor requires high supply voltage in order to bias BJT in forward-active region, thereby limiting its usage in applications, such as low-energy sensors, where operation under unstable sub-1-V supply voltage is expected [6].

To address this issue, there have been a number of different approaches that aim to realize accurate, non-BJT CMOS temperature sensors. For instance, [7] used dynamic threshold MOS transistor in sub-threshold region as a sensing element. In [8], an on-chip resistor is used as a temperature-sensing where temperature-dependent clock duty cycle was measured. In [9], a 9-bit resistor-D/A converter (DAC)-based successive approximation register (SAR) analog-to-digital converter (ADC) converts temperature to digital output. Reference [10] converts the temperature-dependent delay of CMOS gates into digital value. In [11], temperature-dependent discharging time constant is utilized to create a pulse whose pulsewidth is proportional to the temperature. In [6] and [12], the temperature-dependent frequency is measured by counter-based ADC. A phase-domain delta-sigma ADC senses the temperature-dependent phase shift of a bridge filter in [13]. References [14] and [15] use a resistor in the loop filter of a continuous-time delta-sigma A/D converter as a temperature-sensing element to realize a very high-resolution temperature sensor.

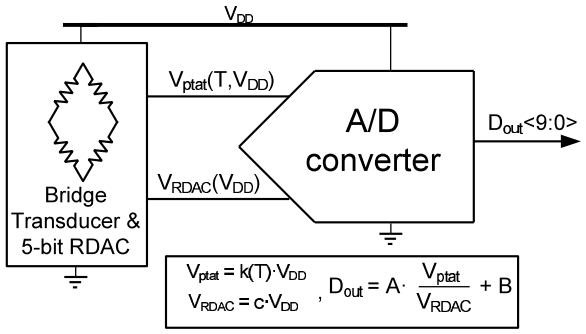

Fig. 1. Ratiometric measurement.

One design challenge of non-BJT/low-supply temperature sensors is high supply sensitivity. In applications where large supply noise or gradual long-term supply-drop is expected during the operation, it is necessary that the temperature to digital conversion process is robust against supply variation. However, many non-BJT temperature sensors that rely on temperature-dependent delay as the temperature sensing mechanism tend to be susceptible to supply voltage variation because the typical gate delay depends also on the supply voltage [6], [10].

In this paper, we utilize the ratiometric measurement technique in an on-chip resistor-based CMOS temperature sensor to improve the supply sensitivity problem. While similar resistor-based front-end has been demonstrated in previous works such as [14] and [15], the goal of this paper is to realize a small-area and medium-resolution temperature-to-digital converter (TDC) that is insensitive to supply voltage variation. As shown in Fig. 1, the key idea is to re-use the temperature-sensing resistor ladder as a reference DAC in the subsequent sub-ranging ADC, thereby inherently removing the supply dependence of temperature-to-digital conversion. Together with chopping and a low-noise interpolating DAC, the proposed TDC implemented in 65-nm CMOS process exhibits very low supply sensitivity of 0.28 °C/V, which is the lowest ever reported for temperature sensor operating under 1 V.

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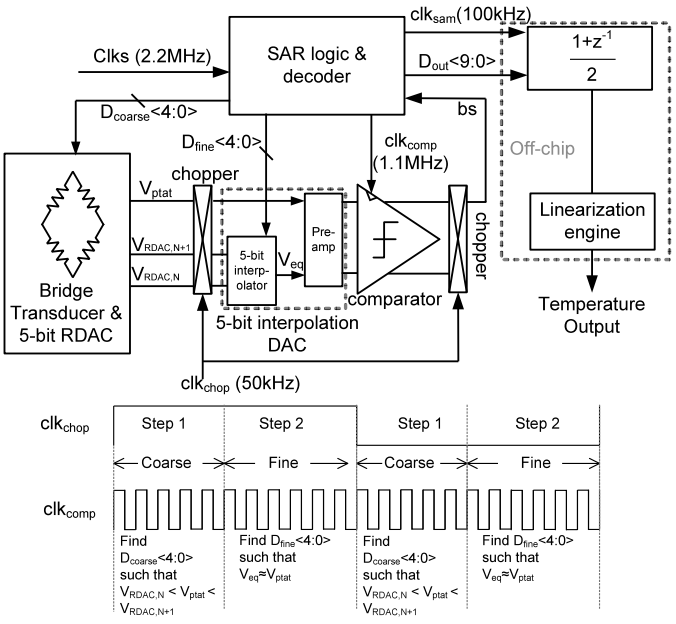

Fig. 2. Overall architecture and timing diagram of the proposed TDC.

The sensor achieves an inaccuracy of less than $+1.6/-1$ °C (2-point calibration) while consuming 47 μW from 0.8-V supply voltage. Since the presented temperature sensor relies neither on a high-gain opamp nor on BJTs, the architecture is highly scalable to advanced process node with even lower supply voltage.

This paper is organized as follows. Section II shows the architecture of the temperature sensor and A/D converter. Section III describes the details of key circuit designs. TDC noise analysis is in Section IV. Section V reports experimental result. We conclude the paper with summary in Section VI.

II. Architecture

Fig. 2 shows the overall temperature sensor architecture. The bridge transducer consists of two resistor ladders. The first ladder generates V_{ptat} by combining two types of on-chip resistors with positive and negative temperature coefficient in such a way that the temperature-to-voltage conversion gain is maximized. The second ladder, built using the same type of resistors, generates $V_{\text{RDAC},N}$ and $V_{\text{RDAC},N+1}$ that are first-order temperature independent.

The output voltages from the bridge transducer feed both the comparator and the 5-bit interpolation DAC with an embedded amplifier, both of which comprise a 10-bit sub-ranging A/D converter. An on-chip state machine drives the successive approximation register (SAR) logic and decoder to perform a two-step A/D conversion. In the first step, the state machine searches for coarse 5-bit $D_{\text{coarse}}[4:0]$ such that V_{ptat} is bounded by temperature-independent $V_{\text{RDAC},N}$ and $V_{\text{RDAC},N+1}$. In the second step, the state machine finds fine 5-bit $D_{\text{fine}}[4:0]$ such that the output voltage of 5-bit interpolating DAC with embedded preamplifier, V_{eq}, is successively driven as close as possible to V_{ptat}. Since V_{eq} is derived from temperature-independent voltages, the digital representation of absolute temperature can be found by combining $D_{\text{coarse}}[4:0]$ and $D_{\text{fine}}[4:0]$. The system-level chopping removes possible 1/f noise below the chopping frequency and offset within the analog signal chain and the comparator by digitally averaging two consecutive conversions[1] [5]. The 10-bit digital representation of the temperature is shipped off-chip for further processing for the temperature computation.

III. Implementation Details

A. Bridge Transducer

A key element of the proposed temperature sensor is the front-end resistor-based bridge transducer consisting of two resistor ladders. Since the power efficiency of temperature-to-digital conversion is primarily constrained by the efficiency of temperature-to-voltage conversion, maximizing the conversion gain leads to energy efficient temperature sensor design. To achieve this goal, two on-chip resistors having opposite temperature coefficient are combined in a constructive way.

More specifically, Fig. 3(a) displays simulated normalized resistance versus temperature characteristic of n-well and $P+$ poly resistor as R_p and R_n, respectively. Note that both n-well and $P+$ poly resistors are available as a programmable cell in a typical foundry process. The positive temperature coefficient in R_p is approximately $\text{TC}_p = +0.25\%/°\text{C}$ while the negative temperature coefficient in R_n is $\text{TC}_n = -0.064\%/°\text{C}$.[2] To maximize the temperature-to-voltage conversion gain, R_p and R_n are series-connected in the resistor ladder 1 as shown in Fig. 3(b), where the mid-point of the series connected resistors generates V_{ptat} as

$$V_{\text{ptat}} = \frac{R_p}{R_p + R_n} \cdot V_{\text{DD}}. \tag{1}$$

By choosing $R_n = 31$ kΩ and $R_p = 24.5$ kΩ, the denominator in (1) can be made relatively constant over wide range of temperature with a conversion gain of 660 μV/K. Such a resistance choice maximizes the temperature-to-voltage at the cost of slight linearity degradation. As a comparison, the conversion gain of ΔV_{BE} is typically around 140 μV/K [1]. Hence, it can be argued that the temperature-to-voltage conversion gain of the presented arrangement is considerably higher than the typical temperature-to-voltage conversion gain of BJT. Note that the residual nonlinearity in the overall temperature-to-digital characteristic can be corrected in the digital post-processing.

Denoted as ladder 2 in Fig. 3(b), the temperature-flat reference voltages are generated in the second resistor ladder, which is essentially a 5-bit thermometer-coded resistor D/A converter (RDAC). In this DAC, identical types of resistors are used so that voltages tapped out from the ladder are first-order temperature independent. Since V_{ptat} changes from roughly 0.2 to 0.4 V under 0.8-V supply over the full temperature range, we chose to use higher resistor values for the very top and bottom resistor in the DAC such that the full range

[1]The system-level chopping performance is limited by the ADC resolution, because it can only remove the noise or offset that is larger than the LSB of the TDC.

[2]Note that the voltage-dependence of n-well resistance introduces static nonlinearity, which can be calibrated out in digital polynomial correction.

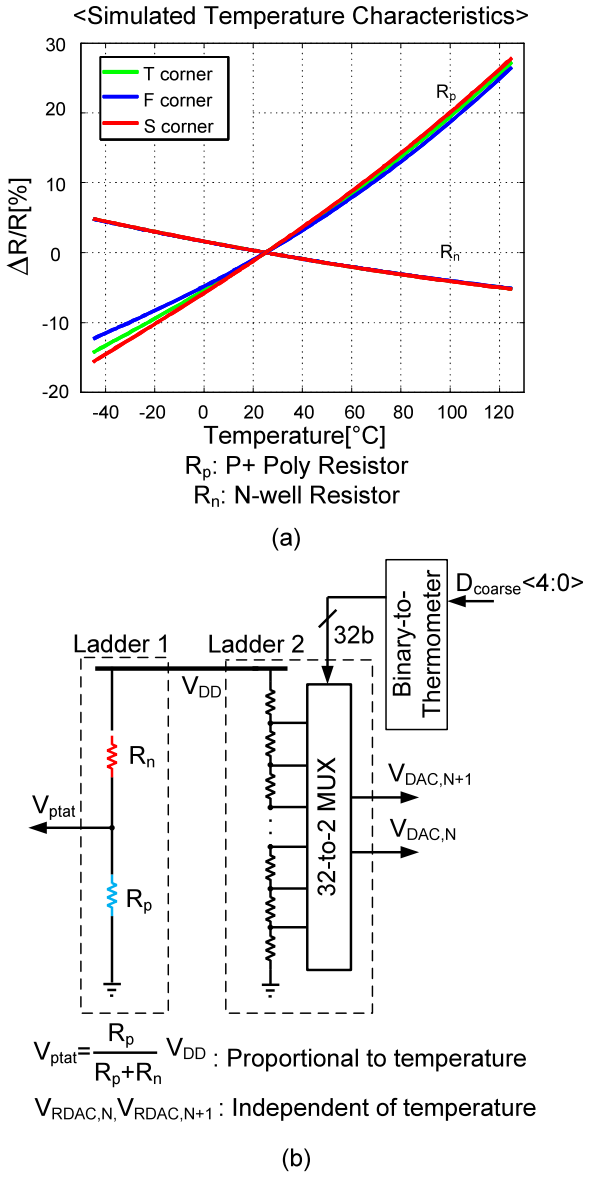

Fig. 3. (a) Simulated temperature versus resistance of $P+$ poly and n-well resistors over process variation. (b) Bridge transducer that generates V_{ptat} and 5-bit RDAC that generates temperature-flat references $V_{\text{RDAC},N}$ and $V_{\text{RDAC},N+1}$.

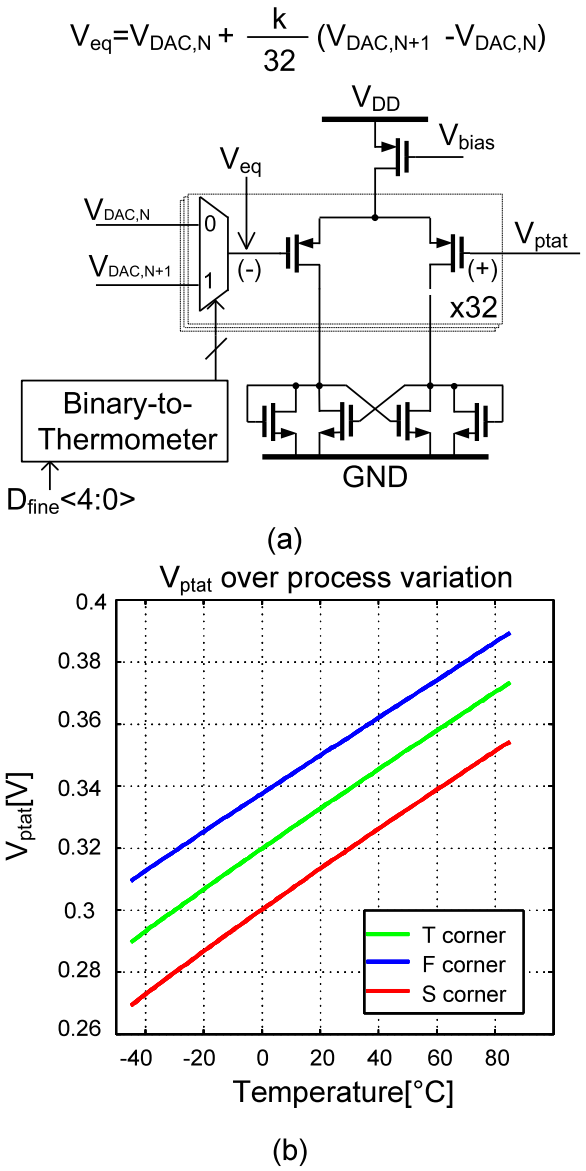

Fig. 4. (a) Circuit diagram of 5-bit interpolating DAC with an embedded preamplifier. (b) V_{ptat} range over process variation.

of the DAC output covers the V_{ptat} range with some margin. The 32-bit selection signal on this DAC is driven by the state machine as a result of first step of the A/D conversion, and is held constant during the second step of the A/D conversion when the fine conversion is performed. It is worth highlighting that both V_{ptat} and $V_{\text{RDAC},N}/V_{\text{RDAC},N+1}$ voltages are fractions of supply voltage V_{DD}. Therefore, both the input and reference voltages of the A/D conversion are identically affected by supply voltage variation, enabling first-order supply-independent temperature-to-digital conversion. Note that the n-well resistor tends to be voltage-dependent with relatively high voltage coefficient, which will eventually limit the achievable supply independence.

B. Interpolating DAC With Embedded Preamplifier

Fig. 4(a) shows the interpolating DAC with embedded preamplifier that provides fine reference voltage in the second step of the A/D conversion. The interpolation is carried out in the resistive interpolator that is implemented as a parallel-connected 32 source-coupled input differential pairs with a shared load. Negative input sides of 32 differential pairs are individually switchable to $V_{\text{RDAC},N}$ or $V_{\text{RDAC},N+1}$, and the positive sides of all pairs are commonly connected to V_{ptat}. Fig. 4(b) displays simulated V_{ptat} over full temperature range, suggesting that PMOS input pair must be used for an embedded amplifier to accommodate low common-mode voltage. The effective threshold voltage V_{eq} by this interpolation can be derived as

$$V_{\text{eq}} = V_{\text{DAC},N} + \frac{k}{32} \cdot (V_{\text{DAC},N+1} - V_{\text{DAC},N}) \tag{2}$$

where k is the total number of differential pairs whose gate is connected to $V_{\text{RDAC},N+1}$. As shown in Fig. 5, the simulated linearity of the interpolator is less than quarter LSB for 10-bit accuracy, which is beyond the target resolution of the overall

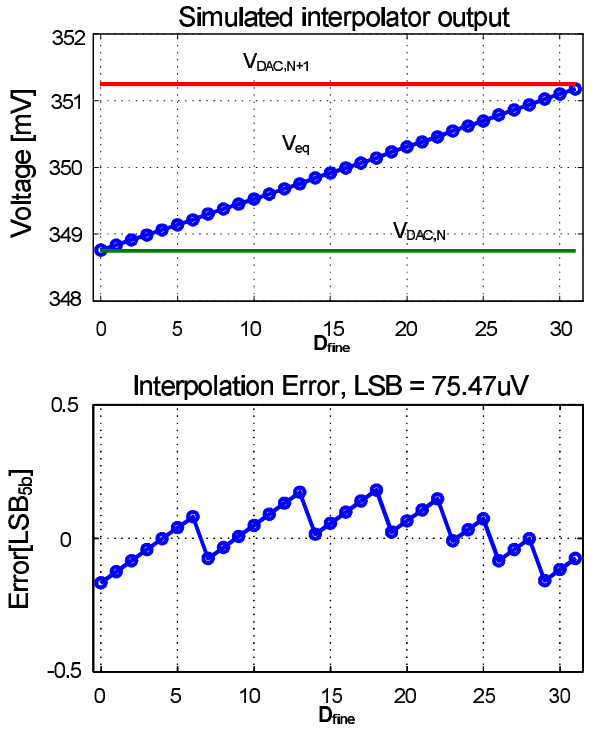

Fig. 5. Simulated input voltage waveforms of interpolating DAC.

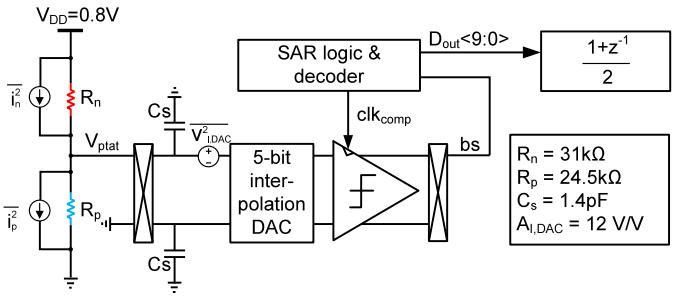

Fig. 6. Simplified schematic for noise analysis.

A/D conversion. Parallel-connected diode and cross-coupled load is adopted for high interpolator gain. Simulated results indicate that the interpolating DAC achieves gain of 12 V/V with −3-dB bandwidth of 13 MHz while drawing 30μA. The offset from the mismatch between differential pair is removed by system-level chopping. The input devices in the interpolating DAC operate in sub-threshold region for the highest current efficiency. The simulated output common-mode voltage of the embedded preamplifier is around 300 mV, and hence, a PMOS input pair is used in the design of the dynamic comparator in Fig. 2.

IV. TDC Noise Analysis

A simplified block diagram for the noise analysis is displayed in Fig. 6. There are two main noise sources in the TDC, both of which are referred to the V_{ptat} node for total noise estimation. First, the noise current from the front-end resistor ladder generates noise voltage $\overline{V^2_{\text{ptat}}}$ as

$$\overline{V^2_{\text{ptat}}} = \left(\overline{i^2_n} + \overline{i^2_p}\right)(R_n||R_p)^2 \ [V^2/\text{Hz}] \tag{3}$$

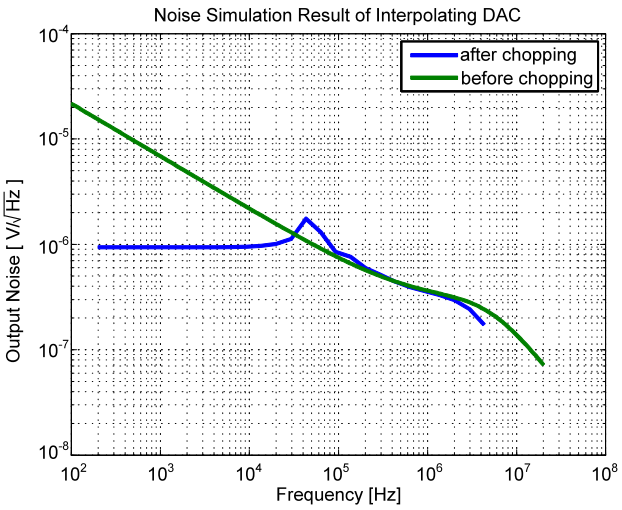

Fig. 7. Noise simulation result of an embedded amplifier in the interpolator.

where $\overline{i^2_n}$ and $\overline{i^2_p}$ are noise currents from R_n and R_p, respectively. To calculate the resulting resolution, this noise needs to be integrated over the noise bandwidth (NBW), leading to

$$\sigma V_{\text{ptat}} = \sqrt{\overline{V^2_{\text{ptat}}} \cdot \text{NBW} \cdot \pi/2} = \sqrt{2\frac{kT}{C_s}} = 76.9 \ \mu V_{\text{rms}} \tag{4}$$

where C_s is the total capacitance at V_{ptat} node. Note that this noise power needs to be halved when accounting for the total TDC resolution due to the $(1 + z^{-1}/2)$ averaging filter in the system-level chopping.

Second, the embedded amplifier in the interpolator generates both flicker and thermal noise which is modeled as $\overline{V^2_{I,\text{DAC}}}$. Fig. 7 shows SPICE simulation of both ac noise and periodic noise analysis with chopping enabled. The simulation indicates that the flicker noise is effectively removed by the chopping.[3] The total input-referred integrated noise can be calculated as

$$\sigma V_{I,\text{DAC}} = \frac{\sigma V_{\text{out,DAC}}}{A_{\text{IDAC}}} \tag{5}$$

where $\sigma V_{\text{out,DAC}}$ is the total integrated output noise after the chopping and A_{IDAC} is the gain of the embedded amplifier in the interpolator. We have carried out numerical integration of the output noise power using the output noise density graph shown in Fig. 7. After applying $(1 + z^{-1}/2)$ averaging filter to the result of numerical integration, the total integrated input-referred noise is obtained as $\sigma V_{I,\text{DAC}} = 50\mu V_{\text{rms}}$.

Total TDC resolution can be derived by combining both noise powers as

$$\text{TDC resolution} = \frac{\sqrt{\frac{\sigma V^2_{\text{ptat}}}{2} + \sigma V^2_{I,\text{DAC}}}}{K_{T2V}} = 0.118 \ ^\circ\text{C} \tag{6}$$

where $K_{\text{T2V}} = 660 \ \mu$V/K is the temperature-to-voltage conversion gain. Note that due to relatively high gain of the

[3]One can increase the chopping frequency to lower the noise density after the chopping. However, the total integrated noise in our TDC is already very close to the LSB of the entire data conversion. Therefore, increasing the chopping frequency brings only diminishing return in our case.

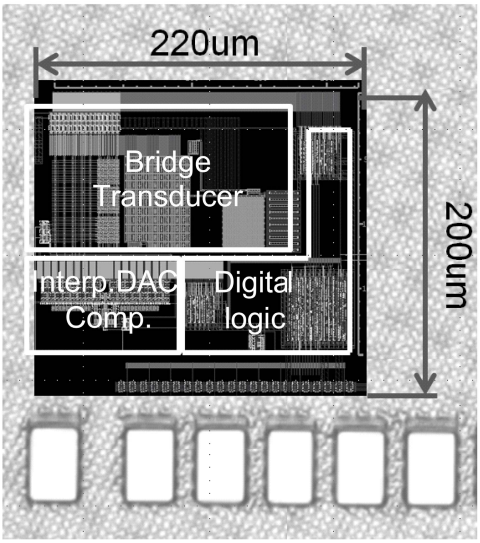

Fig. 8. Die photograph.

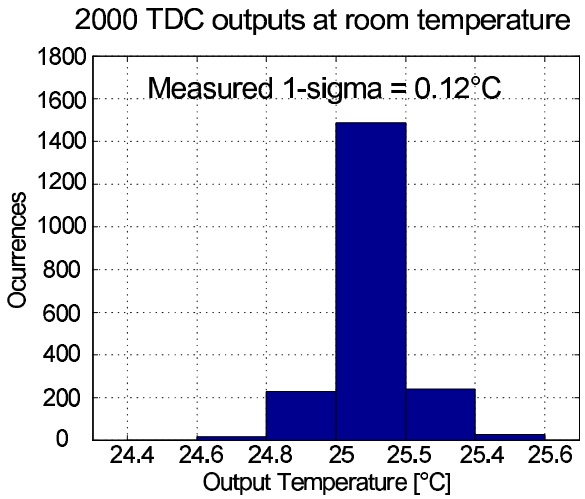

Fig. 9. Histogram of measured temperature at room temperature.

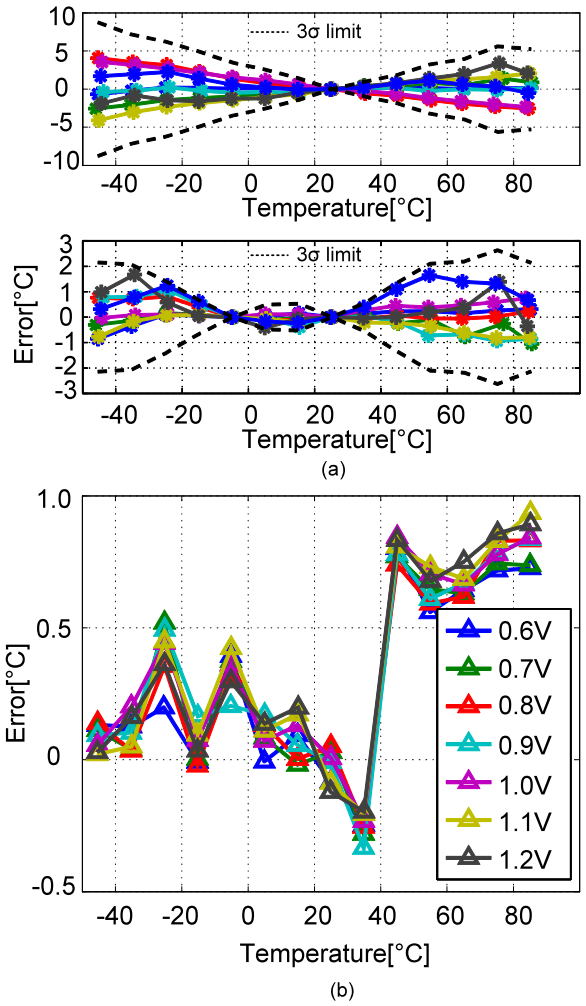

Fig. 10. (a) Inaccuracy after 1- and 2-point calibration with eight chips and (b) under seven different supply voltages from 0.6 to 1.2 V.

amplifier in the interpolator, the contribution of comparator input-referred noise is negligible.

V. Experimental Result

The chip has been fabricated in 65-nm CMOS process. The die photograph is displayed in Fig. 8, where the active area occupies only 0.044 mm^2. Area-efficient design is possible primarily, because this design does not need linear metal capacitor, which is typically required for higher resolution delta-sigma A/D converter design.

When running at conversion time of 10 μs, the entire temperature sensor including the resistor transducer and the two-step ADC consumes 47 μW under 0.8-V supply. To measure the resolution of the temperature sensor, Fig. 9 displays the distribution of 2000 digital outputs measured at the room temperature. Measured rms resolution is 0.12 °C, which matches very close to our estimated resolution of 0.118 °C.

Fig. 10(a) shows the measured inaccuracy of the temperature sensor over eight different chips. The digital output of the ADC after 2-point (-5 °C and 25 °C) calibration is bounded by $+1.6/-1$ °C. When 1-point trimming is used, the inaccuracy is ± 4 °C, which is rather higher. This is accounted for process uncertainty in on-chip resistors and is expected to improve by increasing the physical size of resistors without altering resistor values.

The supply sensitivity is the key characteristic of the presented TDC and this has also been measured. In this experiment, we first found the linear fitting coefficient at $V_{DD} = 0.8$ V and used the same coefficient for other supply voltages from 0.6 to 1.2 V with 0.1-V voltage step. The nominal power consumption when $V_{DD} = 0.8$ V is 47 μW, while the maximum power consumption when $V_{DD} = 1.2$ V is 96 μW. Fig. 10(b) shows measured inaccuracy over supply voltages, indicating that the temperature sensor output is insensitive to the supply values. The measured sensitivity is 0.28 °C/V, which is the lowest over widest supply range among recently published non-BJT and sub-1-V temperature sensors. Note that there are recently reported designs with even smaller supply sensitivity than our design such as [15], but the design in [15] utilizes virtual ground in a high-gain 1.8-V op amp, which can keep the output voltage of the bridge

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TABLE

	This work	[7]	[8]	[16]	[6]	[11]	[12]	[13]	[9]
Type	Resistor	DTMOST	Resistor	Resistor	VCO	Resistor	OSC	Resistor	Resistor
Process $[nm]$	65	160	16	65	65	90	180	180	180
Area $[mm^2]$	0.044	0.085	0.015	1.37*	0.004	0.18	0.22	0.72	0.18
Supply voltage $[V]$	**0.6∼1.2**	0.85∼1.2	0.7	0.75	0.85∼1.05	0.8∼1.2	1.2	1.6∼2	1.2∼2
Supply Sensitivity $[°C/V]$	**0.28**	0.45	N/A	N/A	34	4	0.36	-0.17/0.34†	0.625
Power $[\mu W]$	47.2	0.6	70	15	154	11.8	0.57	160	36
Temp.Range [°C]	-45∼85	-40∼125	-10∼90	0∼90	0∼100	-40∼125	-20∼80	-40∼85	0∼100
Resolution [°C]	0.121	0.063	1	1.75m	0.3	0.25	0.09	0.41m/0.88m†	0.25
Tconv $[sec]$	10u	6m	10u	100m	22	10m	8m	5m	12.5u
Inaccuracy(1-pt) [°C]	±4	±0.4	±3,5	N/A	N/A	N/A	N/A	±0.2	±0.5
Inaccuracy(multi-pt) [°C]	+1.6/-$1_{(2)}$	N/A	±$1,2_{(2)}$	$0.2_{(4)}$	±$0.9_{(2)}$	-$0.6/0.8_{(2)}$	±$0.76_{(2)}$	±0.07/±0.2‡	N/A
Energy/Conversion $[nJ]$	0.472	3.6	0.7	1500	3.4	118	4.56	800	0.45
FOM_{res} $[pJ°C^2]$	**6.9**∼13.8	14.3	700	4.6	300	7400	36.9	0.13	28.1

FOM_{res} = Energe/Conversion$\times(Resolution)^2$

† : Using p-poly resistor and n-poly resistor

‡ : 3-sigma inaccuracy after 1st-order polynomial fitting and systematic error removal

∗ : Area includes CMOS and FBAR

output nearly constant using the negative feedback. Such an arrangement significantly helps to reduce potential second-order impact (such as voltage-dependent resistance variation) that limits the supply sensitivity. On the other hand, our design works with supply voltage as low as 0.6 V and therefore belongs to a different category, where high-gain op-amp design is very challenging.

Table I summarizes the measured performance in comparison with recently published non-BJT temperature sensors. Proposed temperature sensor shows energy-efficient temperature-to-digital conversion with resolution figure of merit of 6.9 pJ $°C^2$ while achieving supply sensitivity of 0.28 °C/V.

VI. CONCLUSION

The low-voltage resistor-based temperature is presented in this paper. Reusing temperature-sensing resistor DAC as a reference voltage of the A/D converter enables supply-insensitive temperature-to-digital conversion. Two-step A/D conversion incorporates the resistive interpolator with embedded preamplifier to achieve the energy-efficient A/D conversion. Measured performance shows the lowest-reported supply sensitivity while achieving the state-of-the-art energy efficiency, suggesting that the presented design can be a promising TDC architecture for deeply scaled CMOS technology.

ACKNOWLEDGMENT

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