

A Digitally Controlled Fully Integrated Voltage Regulator With 3-D-TSV-Based On-Die Solenoid Inductor With a Planar Magnetic Core for 3-D-Stacked Die Applications in 14-nm Tri-Gate CMOS

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Abstract—A fully integrated digitally controlled buck voltage regulator, featuring hysteretic and pulse frequency modulation control for maximum light load efficiency, with 3-D through-silicon-via-based on-die solenoid inductor with a planar magnetic core in 14-nm tri-gate CMOS, demonstrates 111 nH/mm² inductance density and 80% conversion efficiency. The inductance density demonstrated is 20x higher than comparable on-die lateral- or spiral-based inductor densities leading to higher light load efficiency.

Index Terms—3-D-stacked die power delivery, 3-D TSVs, buck converters, digital control, fully on-die voltage regulators (VRs), light load efficiency, magnetic core-based inductors, solenoid inductors, through silicon vias (TSVs).

I. INTRODUCTION

FULLY integrated on-die voltage regulators (VRs) promise efficient and wide-range local power management with fast transient response while reducing losses in the off-die high-voltage power delivery network. Integrated buck VR designs for conventional 2-D packaged dies with different types of power inductor integration technologies have been reported [1]–[4]. Through-silicon-via (TSV)-based 3-D-stacked heterogeneous multi-die packages, however, demand more TSV-friendly and area-efficient inductor integration with minimal cost and process complexity overheads for locally integrated VRs in each of the dies in the 3-D stack. In addition, power density demands in the individual dies of the 3-D stack are quite low due to the stringent thermal constraints of the overall 3-D die stack. Therefore, the locally integrated VR designs need to target maximum

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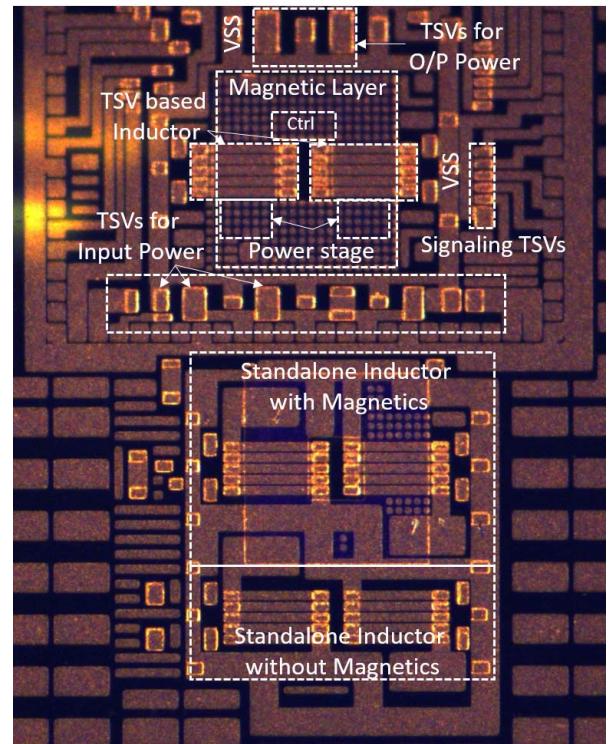


Fig. 1. Chip micrograph.

conversion efficiency mainly in the light load regime, while being sensitive to cost, complexity, and area overheads.

Integrated buck VR designs for high-power-density loads with different types of power inductor integration technologies have been reported [1]–[4]. In [1], planar lateral coupled power inductors with non-planar magnetic cores for higher inductance, quality factor, and current density are integrated on a separate silicon interposer die which is then wire bonded to the VR die on a common ball grid array laminate. High quality-factor air-core power inductors are integrated within

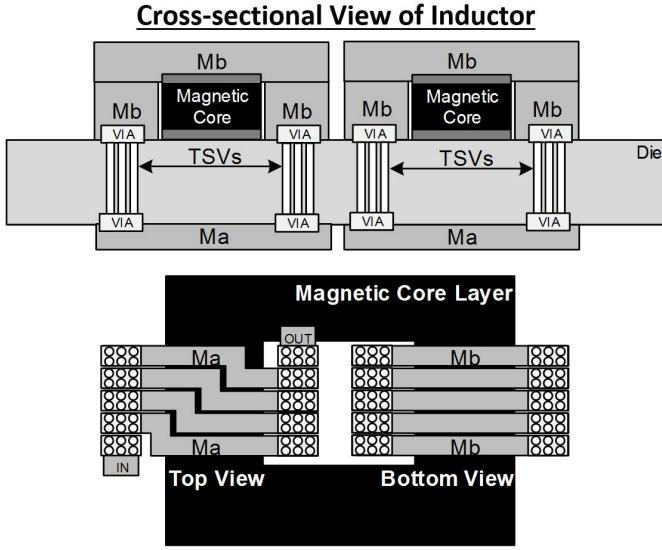


Fig. 2. Different views of the TSV-based solenoid inductor (not drawn to scale).

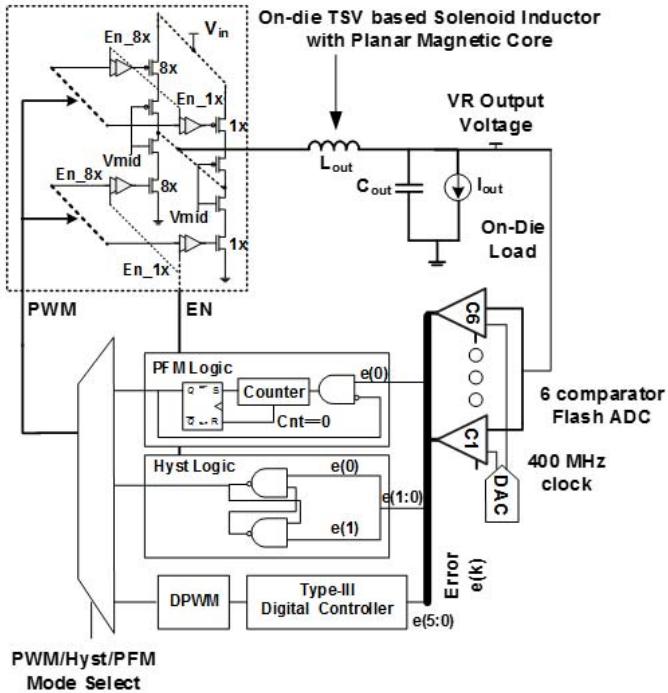


Fig. 3. Digitally controlled buck VR showing PFM, hysteretic, and PWM controller architecture.

the package layers in [2], utilizing the thick package core. In [3], on-die solenoid power inductors with multiple vertical windings around a high-permeability planar magnetic core, utilizing two thick top metal layers have been implemented, which allow for co-location of the load with the on-die VR. While all these options [1]–[3] are very attractive for high-power density loads, they become untenable for low-density light load applications from a cost, area, and complexity perspective. Planar lateral spiral inductors without magnetics are integrated directly on the VR die in [4], utilizing upper metal layers. These integrated VRs (IVRs) can be a very practical option for low-power density loads and can be co-located with

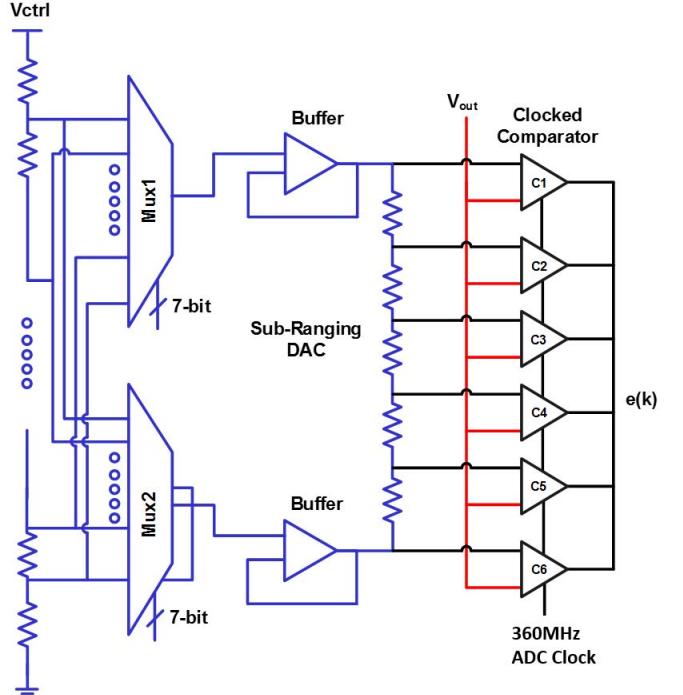


Fig. 4. Sub-ranging DAC-based windowed flash ADC architecture.

the load for reduced parasitic losses. However, the inductance density is too low which implies larger die area cost to build a reasonable value of inductance for higher light load efficiency.

In this paper, we demonstrate a fully integrated digitally controlled two-phase buck VR with on-die TSV-based solenoid inductors with multiple vertical windings, utilizing thick metal layers on the front and back sides of the die, as well as a planar magnetic core, implemented in 14-nm tri-gate CMOS. This inductor structure and on-die integration technology enables higher inductance density than that of on-die planar lateral spiral inductors [4] while utilizing the TSVs already available in 3-D die stacking. At the same time, it offers 1) superior scalability of inductor footprint and 2) fine dynamic voltage & frequency scaling (DVFS) domains via inductor co-location with the domain. The higher inductance density leads to small die area cost and better light load efficiency as will be shown from the measurement results later on in this paper. The digital VR controller enables easier reconfiguration, more efficient, and synthesizable design with fine-grain distributed DVFS domains, thus enhancing scalability and portability across process nodes.

The rest of this paper is organized as follows. Section II describes the architecture and design of the digitally controlled IVR. Section III explains the 3-D-TSV solenoid inductor with optional planar magnetic core and its associated design and modeling. Section IV presents the IVR measurement setup with Section V providing an overview of the silicon measurements, and Section VI concludes this paper by summarizing the key results.

II. DIGITALLY CONTROLLED INTEGRATED BUCK CONVERTER

A two-phase buck VR with on-die TSV-based solenoid inductors with a planar magnetic core is implemented in 14-nm

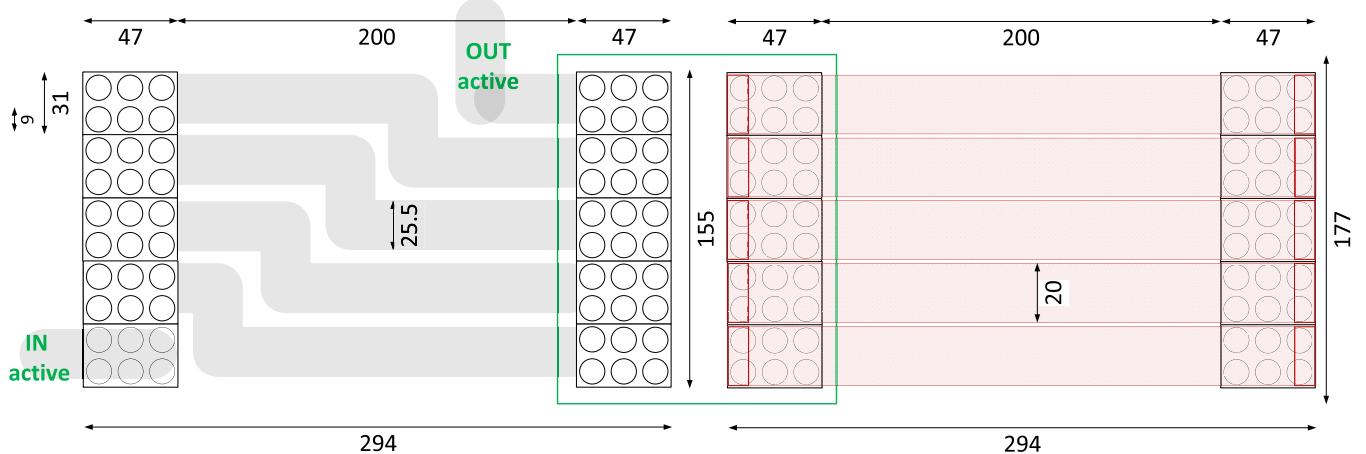


Fig. 5. Inductor layout details.

Measured Inductance (With & W/O Magnetics) Measured Resistance (With & W/O Magnetics)

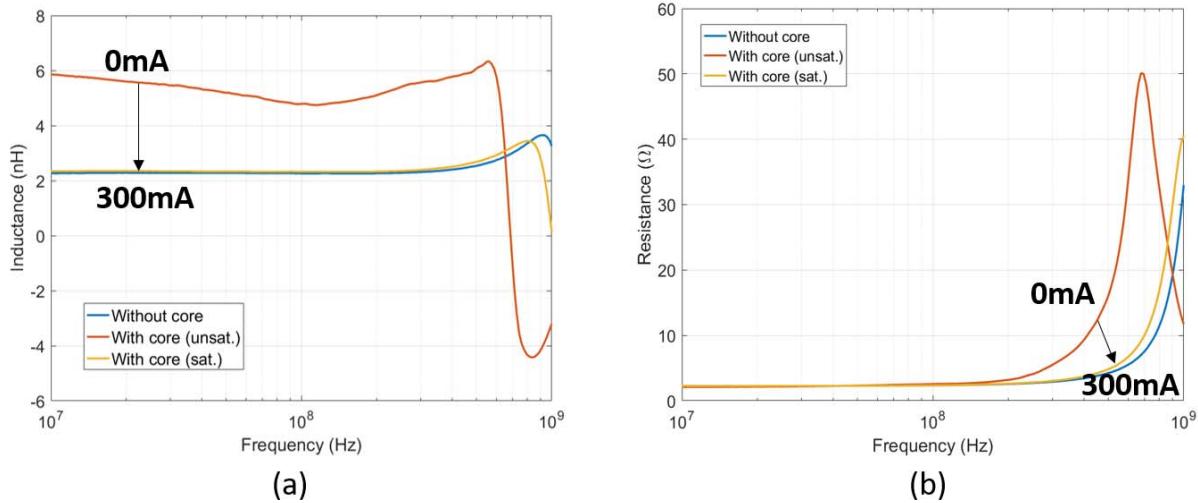


Fig. 6. (a) Measured inductance characteristics. (b) Measured resistance characteristics.

tri-gate CMOS alongside stand-alone inductor structures with and without magnetics to allow direct measurements of the inductor characteristics (Fig. 1). The inductor is built with 4.5-TSV-based vertical turns around the die with a high-permeability planar magnetic core using thick metal layers Ma and Mb on its front and back sides, respectively (Fig. 2). The stand-alone TSV-based solenoid inductor with magnetics has an inductance of 5.86 nH at 10 MHz and about 2.2 nH without the magnetic core. The magnetic core in a 3-D-TSV-based solenoid structure is optional and will be further elaborated in Section III.

The VR power stage (Fig. 3) consists of (1) cascade power switches to support VR input voltage as high as $2V_{max}$, and eight modular slices per phase that can be optimally enabled/disabled to maximize conversion efficiency up to 25-mA maximum load. A programmable dead time block was also integrated into the power train to allow for independent control of the dead time between the H-L and L-H transitions of the pulse width modulation (PWM) signals. The main

purpose of the dead time was to avoid the shoot through currents between the high side and the low side switches. The resolution of the dead time is around 20 ps with a total range of about 0.5 ns. A windowed flash ADC (Fig. 4) is used for V_{out} sampling and conversion to sampling error $e(k)$. A 7-bit DAC converts the V_{ref} code into reference voltages for the six comparators. The low offset of the comparators and the 7-bit DAC resolution provides tighter control over the window enabling high accuracy at the output voltage. ADC and DAC design choices are aimed at reducing area and power overheads of the analog front end [3]. A sub-ranging DAC architecture is used to reduce the number of 7-bit multiplexers from 6 to 2. Two 7-bit DACs generate the top and bottom reference voltages which are then buffered with a unity gain amplifier to drive a secondary resistor stack which generates the remaining four reference voltages. Such an architecture not only keeps the area in check but also allows for very fast V_{ref} update rates while minimizing overall power of the windowed flash ADC. A classic type-III digital linear controller running

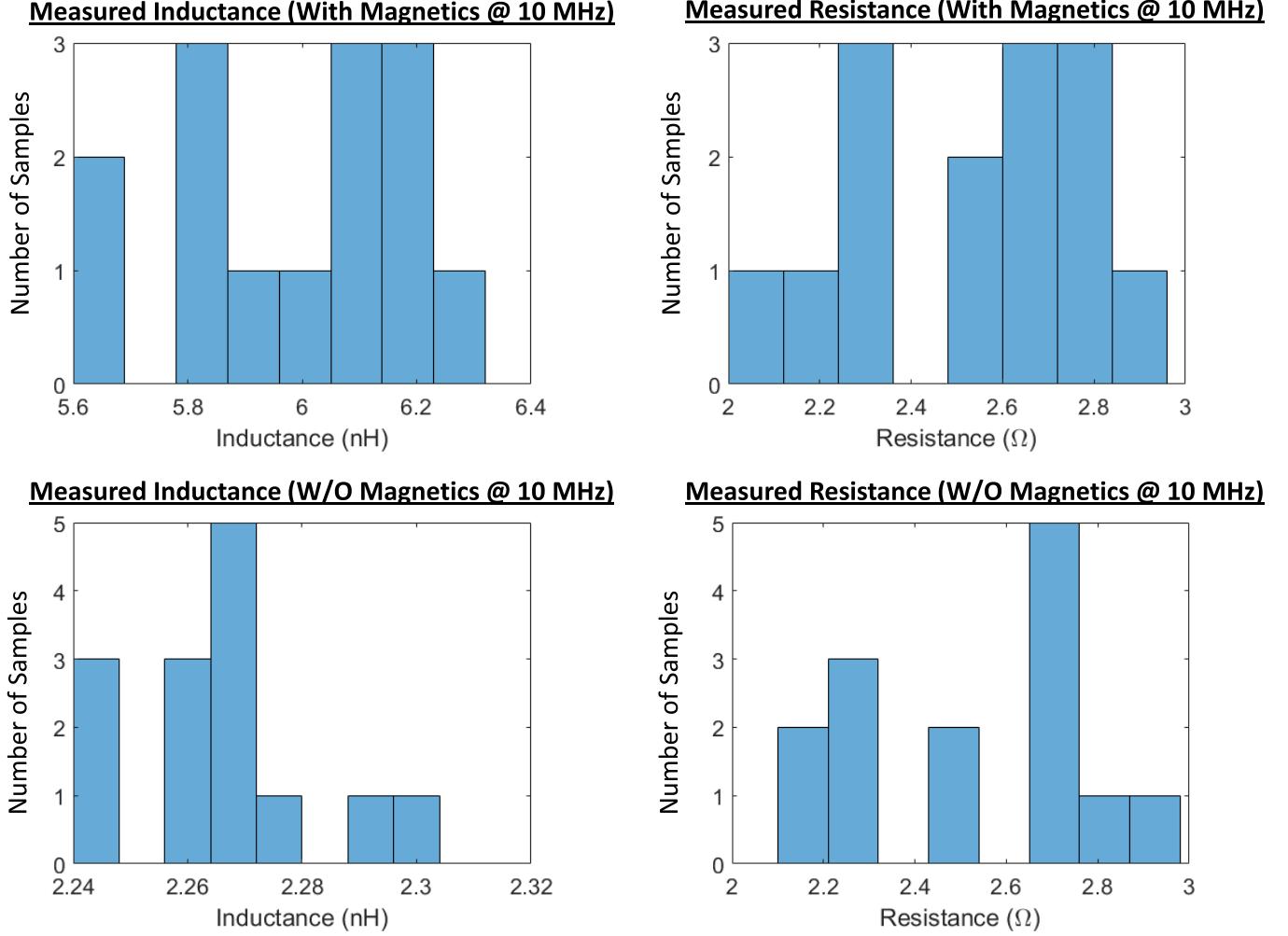


Fig. 7. Measured inductance and resistance characteristics for inductors with and without magnetics at 10 MHz.

at 90 MHz is demonstrated in the PWM mode for high load current applications as required. Since the output of the windowed flash ADC is thermometer encoded, a lookup table-based error processing is employed in the execution of the type-III compensator to save on area and power. The entire controller is implemented using fixed point arithmetic with appropriate overflow and underflow protections. The controller and ADC runs off a system clock at 360 MHz which is coming into the silicon through a GPIO. On-die input and output decoupling capacitors of 1 and 6 nF, respectively, are implemented using MIM capacitors.

Continuous conduction mode suffers from poor light load efficiency [6]–[12] and a loss breakdown reveals that the switching losses dominate the overall losses in such light load conditions. Variable frequency control techniques have demonstrated that the efficiency can be maintained flat across such light load profiles. There are several techniques in this category but the two most popular techniques are the hysteretic controller and the constant ON-time pulse frequency modulation (PFM) technique [6]–[10]. In this paper, both these techniques have been implemented for maximizing efficiency at the light loads typical for dies in 3-D stacks. Both techniques have single cycle response

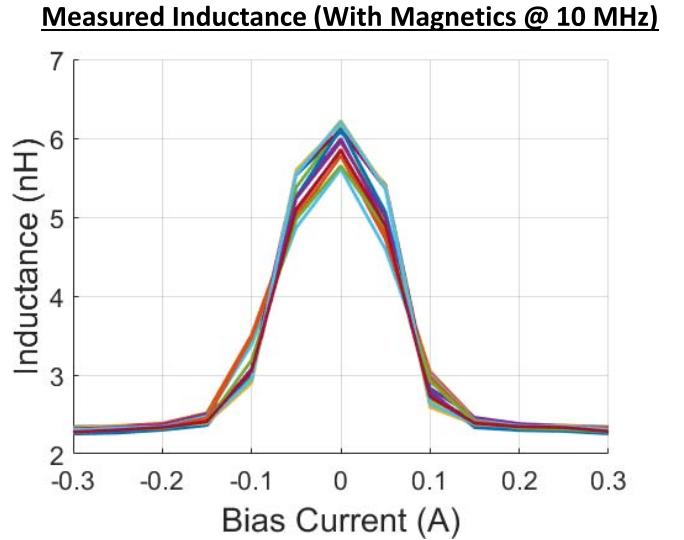


Fig. 8. Measured inductance as a function of dc bias current for the 3-D-TSV inductor with magnetic core.

times for any load disturbances. Therefore, in addition to being efficient they also provide extremely fast correction to any di/dt event. Subtle differences do exist between

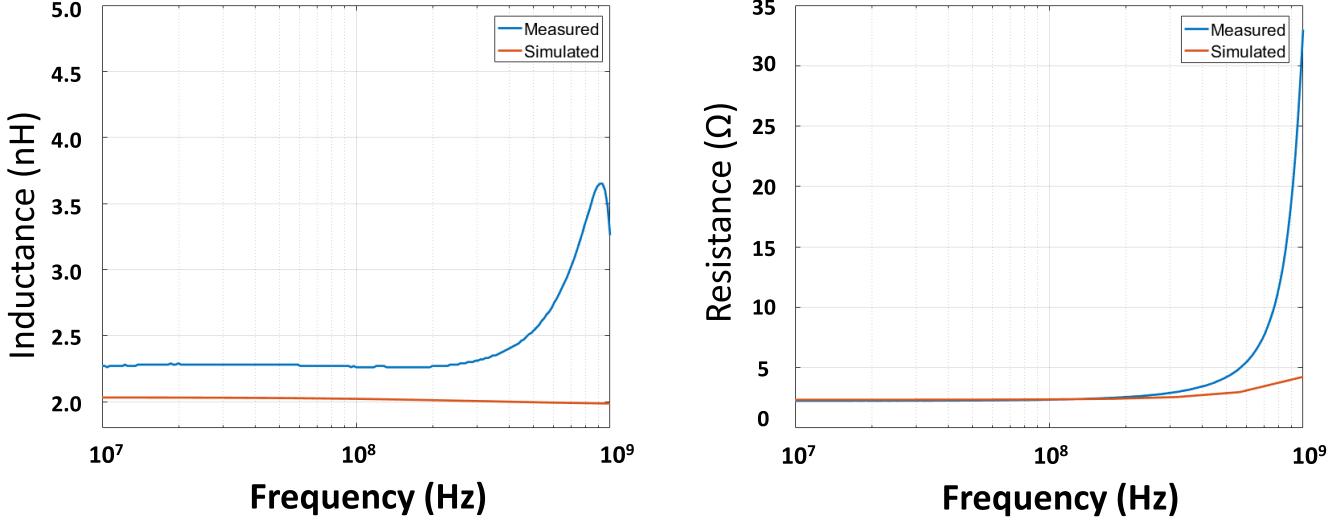


Fig. 9. Plot showing correlation of simulated finite-element model and measured inductor characteristics for TSV inductor with no magnetics.

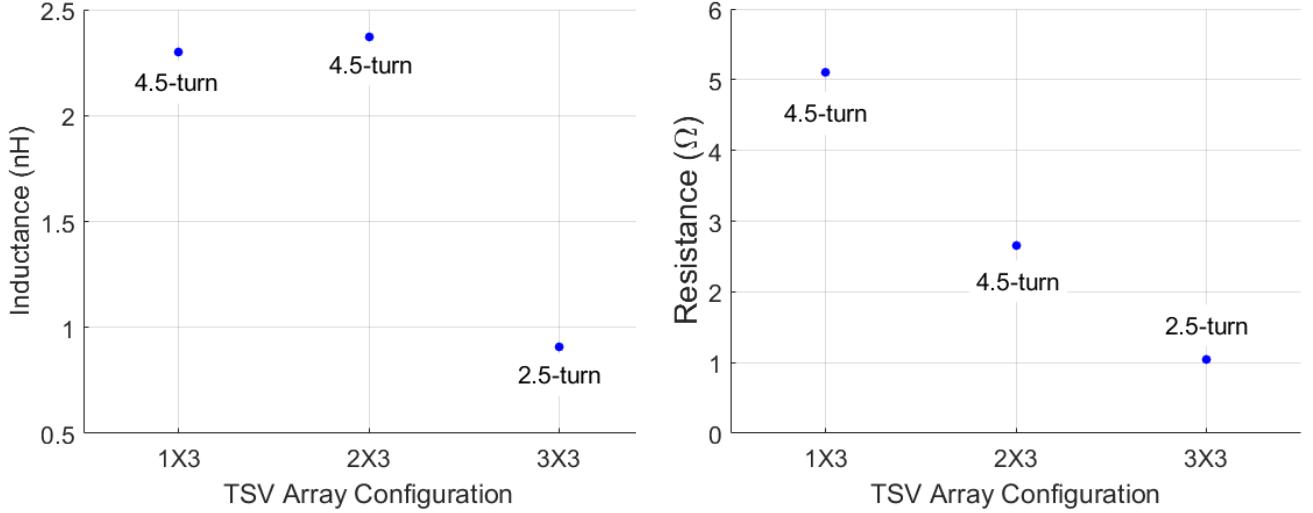


Fig. 10. Simulated inductance and resistance as a function of the TSV array configuration.

the two techniques and will be further explained in the following.

The hysteretic controller utilizes two comparators to detect the output voltage level and is also popularly referred to as the “bang–bang” controller. The comparator outputs are fed into a simple logic block which can be functionally mimicked as two cross-coupled NAND gates, as shown in Fig. 3. Such a structure not only ensures stable operation but allows the capability of providing a programmable hysteresis window [7]. This programmable window controls the overall ripple in the converter with the assumption that the delay in the comparators is small. The hysteresis levels and available output decoupling set the operating frequency at a specific load. Such a technique is commonly used when output voltage ripple is needed to be controlled. The hysteretic controller does not allow any control over the peak inductor current which is one of its biggest drawbacks. Furthermore, the technique needs to be

carefully designed as the delays in the loop need to be orders of magnitude smaller than that of the overall frequency of operation which may be hard in fully on-die converters with tiny values for its passives. The stability of the technique is also dependent on the type of decoupling capacitor and typically a larger equivalent series resistance (ESR) of the output capacitor ensures smooth and reliable operation.

The other VR control mode implemented for light loads is a constant ON-time PFM controller [8]–[10] which utilizes only a single comparator to regulate the output. When the output voltage hits the comparator threshold, the output of the comparator triggers an ON pulse. The width of the pulse is programmable through a counter, as shown in Fig. 3. The ON-time pulse delivers a fixed amount of energy per pulse and since the energy loss per pulse is constant, the switching frequency varies linearly with load current, thus providing flat conversion efficiency across a range of load currents. The

constant ON-time PFM technique directly controls the inductor peak current with the ON time deciding the peak value of inductor current. This is shown to be a key ingredient in controlling overall efficiency [12]. However, larger ON times at lighter loads can cause larger output ripple. If output ripple is a concern, the ON-time pulse width can be varied with output load to keep the output voltage ripple under control. This, however, will be at the expense of efficiency.

III. 3-D-TSV INDUCTOR DESIGN, MEASUREMENTS, AND MODELING

In light load applications, the value of inductance plays a vital role in determining overall efficiency. The value of inductance determines the peak current which in turn decides the energy delivered to the output in every switching pulse, thus influencing the overall switching frequency of the converter for a given load current. Since the switching losses are dominant at light loads a high value of inductance results in higher efficiency by switching fewer times. Therefore, it is of vital importance to have a large inductor value for higher light load efficiency.

There are several inductor structures published in the literature for high-density power loads [1]–[3], [5]. However, such structures are untenable from a cost, complexity, and area overhead perspective for low-density 3-D-stacked multi-die packages. Lateral spiral inductors can be co-located with the load and can be fully integrated in ultra-thin packages [4], but the poor inductance density implies larger die area cost to build a reasonable value of inductance for higher light load efficiency.

Recently, vertical solenoid structures with magnetics have been demonstrated in [3] and [5]. Such a vertical solenoid structure is generally attractive as the inductor is formed with multiple vertical windings around a planar magnetic core. While the magnetic laminations add to the cost, the multiple vertical windings provide an additional knob to control overall inductance at the cost of increased resistance. However, in light load domains, the increased resistance is not a significant adder to the overall conduction losses, and hence may be a useful knob in low-density stacked die applications. In addition, the 3-D TSVs add another dimension of using the entire height of the die which adds to the overall volume of the inductor increasing its inductance significantly. Such a vertical solenoid with multiple vertical windings using 3-D TSVs with an optional planar magnetic core is demonstrated in this paper.

The 3-D-TSV inductor is built with 4.5-TSV-based vertical turns around the die with a high-permeability planar magnetic core using thick metal layers Ma and Mb on its front and back sides, respectively (Fig. 2). Multiple TSVs are used in parallel to reduce the series resistance of the vertical windings. A single lamination magnetic core-based inductor is also shown to demonstrate the true potential of such IVRs. In order to measure their characteristics independently, stand-alone passive inductor structures identical to the ones used in the IVR were also fabricated. These inductors were wafer probed and measured using a network analyzer.

Fig. 5 shows the layout details of the 3-D-TSV inductor. Six TSVs, each with a diameter of 9 μm , are connected

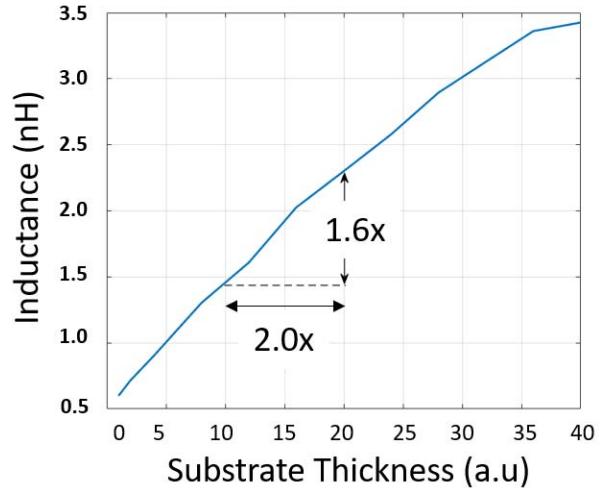


Fig. 11. Finite-element model-based simulation results of TSV inductor showing variation of inductance with substrate thickness.

in parallel to form a TSV array of size $47 \mu\text{m} \times 31 \mu\text{m}$. The width of the turns on layers Ma and Mb are 25.5 and 20 μm , respectively, to maximize the coupling between the windings while maintaining minimum design rules check (DRC) spacing requirements. The width of the inductor is kept at 200 μm (excluding TSV array) to maximize the inductance while keeping the resistance overhead manageable. The height of the inductor, which is equivalent to the height of the TSV, adds the third dimension to maximizing inductance and is roughly between 75 and 100 μm .

Fig. 6 shows the measured results of the 3-D-TSV stand-alone passive inductor structures both with and without magnetics. The inductor with the magnetic core measures an inductance of 5.86 nH at 10 MHz [Fig. 6(a)] with an area footprint of 0.0525 mm^2 , which leads to a total inductance density of 111 nH/mm^2 . As expected, the saturated inductance characteristic closely matches that of the inductor without a magnetic core. The inductor design without the magnetic core measures about 2.2 nH with the same area footprint. The ESR of about 2.7Ω is measured for either inductor structure. We can therefore conclude that the resistance of the inductor is not affected by the addition of the magnetic core, as shown in Fig. 6(b).

A histogram of inductance and resistance measurements made on 14 fabricated samples with and without magnetics at a frequency of 10 MHz is shown in Fig. 7. The median inductance for the samples with the magnetic core is 6.1 nH and the median ac resistance is 2.7Ω . The median inductance for the samples without magnetics is about 2.27 nH with roughly similar median resistances like the samples to magnetics at about 2.7Ω . The variation in inductors with the magnetic core is roughly $+/-6\%$ while the inductors without magnetics demonstrate a lower variation of about $+/-1.5\%$. This can be attributed to the non-uniformity of the magnetic material deposition across the samples. This is, however, is still within acceptable inductor tolerances of $+/-20\%$. The variation in ac resistance measures about $+/-50\%$ and is similar to the two inductor types. This can then be primarily attributed to

	N. Strucken JSSC'13	E. Burton APEC'14	H. Krishnamurthy ISSC'17	H. Krishnamurthy VLSI'14	This Work
Inductance Density (nH/sq-mm)	51.0	NA	10.0	5.5	20x 111.0

Fig. 12. Comparison of inductance densities of the proposed TSV-based inductor with state of the art.

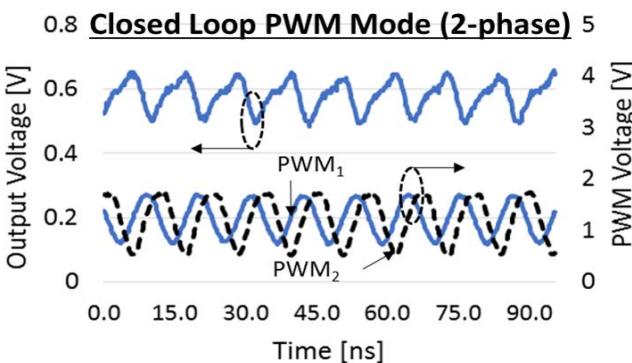


Fig. 13. Measured closed-loop waveform in linear type-III controller mode showing output voltage and PWM signals in two-phase operation.

the variation in TSVs rather than the non-uniformity of the magnetic material. The variation of inductance as a function of dc bias current is shown in Fig. 8. As evident from Fig. 8, the magnetic material saturates beyond 50 mA in current, dropping the inductance from about 6 to ~ 2.1 nH which is similar to that of the samples without the magnetic core.

A finite-element model of the fabricated air-core (without magnetics) inductor correlates with the measurements to within 10% at low frequency, as shown in Fig. 9. The high-frequency behavior is not well modeled due to the adjacent layout structures being excluded for simplicity. However, the discrepancy is $>> 10\%$ beyond 500 MHz which is well above the frequency range of operation of the IVR. The finite-element model can thus be used to study the effect of various parameters of the inductor aiding in the overall optimization.

The design methodology adopted in this proof of concept is to target a certain amount of inductance (> 2 nH without magnetic core) with a maximum area overhead of ~ 0.05 mm². The above design targets along with the ratio of inductance over the dc resistance were used to determine the best configuration of TSV array, trace width, and the number of turns.

The theoretical expression for the inductance of an infinite solenoid, shown in the following, can be used to provide an initial estimate of the number of turns required to achieve the desired target:

$$L = \mu_0 N^2 h \cdot \frac{W}{L} \quad (1)$$

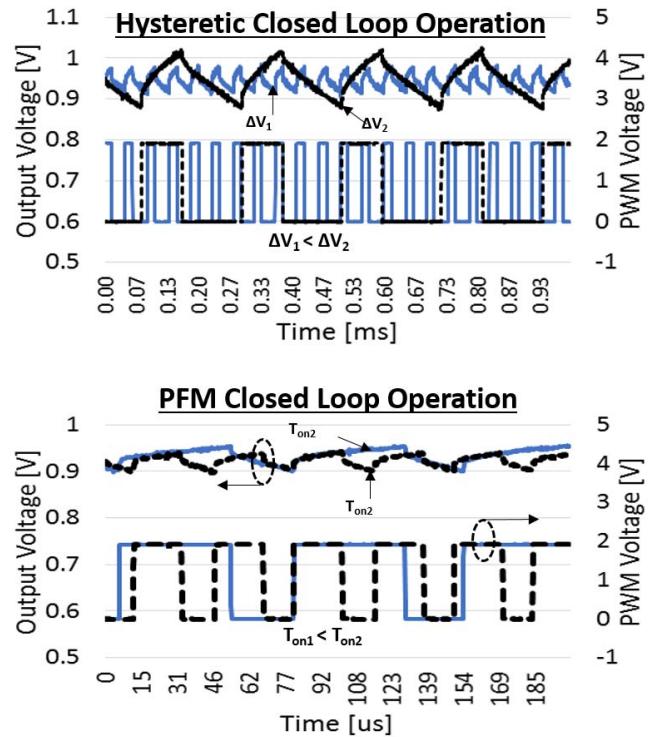


Fig. 14. Measured closed-loop waveforms for hysteretic and PFM controllers with programmable hysteresis levels and ON times, respectively.

In (1), “ h ” is the height of the die (~ 100 μ m), the number of turns is N , and the width and length (measured along the turns) of the inductor are W and L , respectively. Assuming a 1:1 aspect ratio of the footprint of the inductor, this leads to at least four turns being required to achieve the desired inductance target (> 2 nH).

Taking a closer look at the solenoid inductor structure, as shown in Fig. 5, it can be seen that the number of TSVs in the array also controls the maximum trace width that can be accommodated. For instance, a 1×3 array can have a trace width as wide as 9.5 μ m while a 2×3 array can have a trace width as wide as 25.5 μ m accommodating all the DRC rules. The 1×3 array is $> 2 \times$ lower in trace width, leading to larger number of turns but with increased resistance. Moreover, since the traces on Ma as shown in Fig. 5 are L shaped, the width

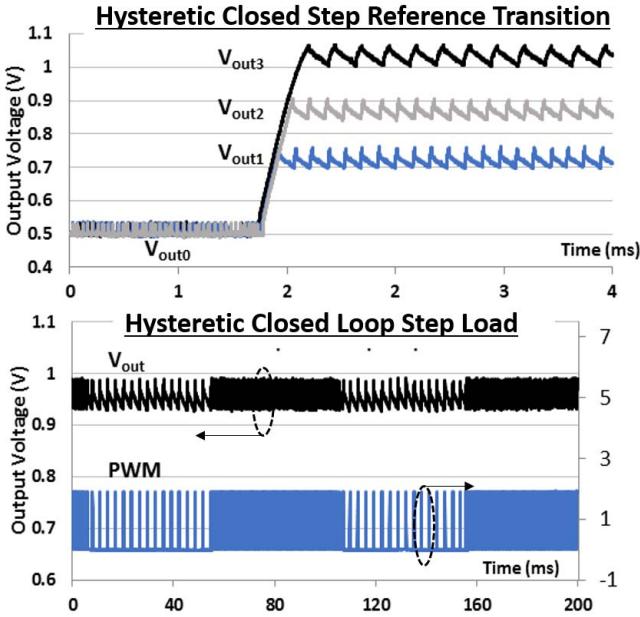


Fig. 15. Measured closed-loop response in hysteretic mode for reference step (0.5–0.7/0.85/1 V) and periodic load steps of 1.5–25 mA.

of the inductor must be greater than or equal to its length. The plots in Fig. 10 obtained from an finite element method simulation demonstrate the characteristics of three different TSV array configurations. The 3×3 array configuration allows only for a 2.5-turn inductor with the allowed area and winding constraints, and hence has inductance lower than that of the desired value. Although the 1×3 configuration results in the desired value of inductance its resistance is 5Ω which is prohibitively large to achieve $>80\%$ conversion efficiency. The 4.5-turn inductor with a 2×3 TSV array configuration, keeping in mind the DRC rules results in a trace width of $25.5 \mu\text{m}$. The minimum height of the inductor with 4.5 turns and a 2×3 TSV array resulted in a Y -dimension of $177 \mu\text{m}$. With the requirement that the width of the inductor be larger than the height and with the overall inductor area target of 0.05 mm^2 the overall X -dimension compliant to all DRC rules ended up being $294 \mu\text{m}$ resulting in an overall area of 0.052 mm^2 .

The B -field inside the TSV inductor-based vertical solenoid is relatively uniform, which allows for a near linear scaling of the inductance as a function of the die thickness, as shown in Fig. 11. Since the inductor structure uses the entire height of the die (75 – $100 \mu\text{m}$), the 3-D-TSV-based inductor structures can obtain large inductance values ($> 2 \text{ nH}$) without the need for any magnetics unlike [3], [5]. Adding a core to the structure further improves the inductance density by $2.5\times$, as can be seen in Fig. 6(a). A comparison of all the recently published on-die inductor work is shown in Fig. 12 and it can be seen that the 3-D-TSV inductors offer a $20\times$ improvement over equivalent lateral inductors. Thus, a 3-D-TSV-based solenoid inductor achieves the highest inductance density making it very attractive for fine-grained DVFS in 3-D die stacking applications.

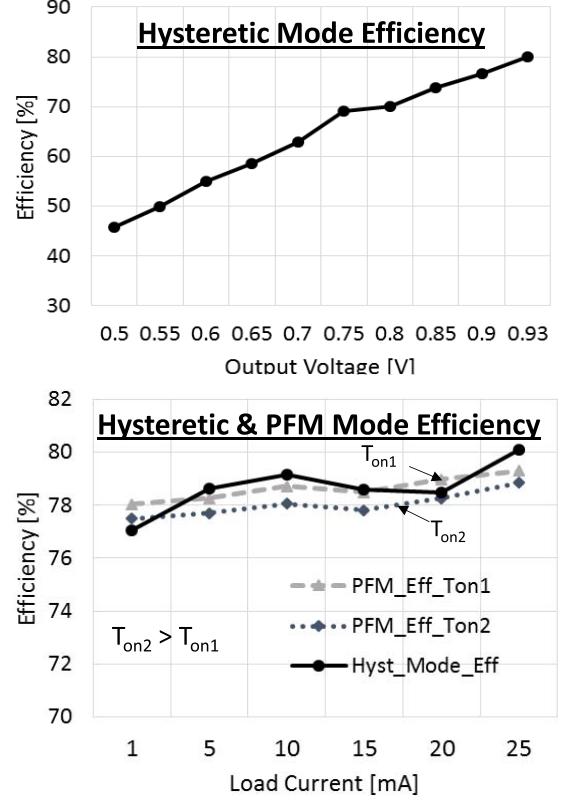


Fig. 16. Measured efficiency in PFM and hysteretic mode.

IV. TEST PROTOTYPE

The chip micrograph of the fully integrated digitally controlled two-phase 90-MHz buck VR with 3-D-TSV-based on-die vertical solenoid power inductors with planar magnetic core is shown in Fig. 1. As shown in Fig. 1, the chip was primarily divided into two regions with the top half of the design focusing on the fully on-die VR with the 3-D-TSV inductor structures while the bottom half implementing two identical stand-alone inductor structures for passive characterization. One of the passive structures was designed to include a planar magnetic core while the second was implemented without magnetics to compare and contrast the effect of the magnetic core. Another unique aspect of this prototype was that all the signaling and power to the chip was delivered through signaling and power TSVs to mimic a typical 3-D heterogeneous die stacking application. The input voltage for all measurements was 1.2 V with a programmable output voltage range of 0.4–1.1 V. On-die input and output decoupling capacitors of 1 and 6 nF, respectively, are implemented using MIM caps. Phase and slice shedding modes were implemented and variable frequency hysteretic control and constant ON-time PFM modes were implemented to maintain flat efficiency across the entire load range of up to 25 mA. The controller in PWM mode runs at a sampling frequency of 360 MHz which was brought in through general purpose I/Os. A field-programmable gate array-based serial interface was used to provide low-frequency digital bits to configure the IVR into the various modes.

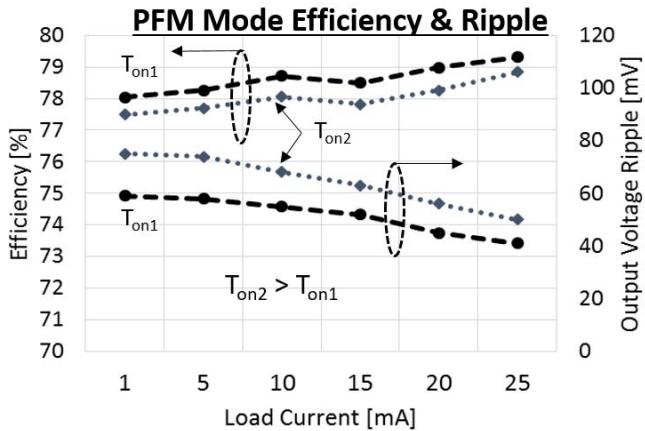


Fig. 17. Measurement results showing the effect of varying ON time in PFM mode on output voltage ripple at 25-mA load current.

V. IVR MEASUREMENT RESULTS

In this section, we present silicon measurement results for: 1) closed-loop operation in the PWM mode at 90-MHz switching frequency; 2) IVR performance metrics (efficiency and transient), for both hysteretic and PFM control; and 3) effect of the ON time in the PFM control on its efficiency and output voltage ripple. All VR measurements are performed for 1.2-V input voltage and for a range of output voltages between 0.4 and 1.1 V. Closed-loop regulation by the IVR in the PWM mode is demonstrated in Fig. 13 at an output voltage of 0.6 V with both phases active at a load current of 25 mA. The two-phase PWM signals along with the steady output voltage demonstrate that the 3-D-TSV inductor remains true to its characteristics even at 90 MHz across a large signal disturbance and could be employed for larger load domains as required. Closed-loop hysteretic and PFM control waveforms, with programmable hysteresis levels and ON times, are shown in Fig. 14. As expected, for the same load current, different hysteresis levels or ON times as the case may be result in different operating frequencies which primarily facilitate optimizing efficiency at the cost of output voltage ripple. Step reference transitions (0.5–0.7/0.85/1 V) and step load transitions (1.5–25 mA and vice versa at periodic intervals) measurements for the hysteretic controller show single cycle response for either transient event (Fig. 15).

Measurements across a wide range of load currents and output voltages show 80% peak conversion efficiency for 25-mA load current at 0.93-V output voltage (Fig. 16). While both hysteretic and PFM controllers achieve flat 77%–80% conversion efficiency across a 1.5–25-mA load current range at 0.93 V, the output ripple can increase by as much as 50% for lighter loads in PFM mode (Fig. 17). In addition, the ON time needs to be set optimally to maximize efficiency and minimize output ripple for PFM.

Fig. 18 shows the comparison table with the state of the art. The 3-D-TSV-based inductors have the highest inductance density of 111 nH/mm² which is 20× larger than the inductance density over lateral spiral inductors [4]. This translates to

	[1]	[2]	[3]	[4]	This Work
Year	2013	2014	2017	2014	2017
CMOS Technology	45 nm SOI	22 nm	14nm	22nm	14nm
Inductor Technology	2.5D Interposer IC Non-Planar Magnetic Core	Package Inductors Air Core	On-Die Solenoid Planar Magnetic Core	Lateral On-Die Air-Core	On-Die TSV based Solenoid with Planar Magnetic Core
F _{sw} (MHz)	200	140	100	500	90
L (nH)	12.5	1.5	1.5	1.5	4.8
C (nF)	48	NA	5	10	6
V _{in} (V)	1.8	1.7	1.5	1.5	1.2
V _{out} (V)	1	0.88	1.15	1	0.93
Peak Efficiency (%)	71	90	84	68	80
Efficiency @ 1.5mA I _{load} (%)	NA	NA	NA	<60	77
Inductance Density (nH/sq-mm)	51.0	NA	10.0	5.5	111.0
Controller	Digital	Analog	Digital	Digital PWM/Hys	Digital PWM/PFM/Hys

Fig. 18. Comparison table of the proposed work with state of the art.

higher light load efficiency across the entire load as compared to the IVR with lateral inductors. The inductance density of such 3-D-TSV structures is also 10× larger than that of solenoid inductors with a single magnetic lamination as discussed in [3].

VI. CONCLUSION

The industry's first fully integrated digitally controlled two-phase buck VR with on-die 3-D-TSV-based solenoid inductors with a planar magnetic core is demonstrated in 14-nm tri-gate CMOS for fine-grained power delivery/management domains of 3-D-stacked heterogeneous multi-die packages. This is the highest level of integration achieved on a buck converter, where the 3-D-TSV inductor and the IVR active circuits are integrated on the same monolithic die. The 3-D-TSV inductor measures an inductance density of 111 nH/mm² which is the highest reported for any power inductor to date demonstrating the true potential for such inductor structures. This is 20× better than inductors-based on planar spiral inductors [4]. The 3-D-TSV inductor structures without the planar magnetic core also demonstrates an inductance density of 42 nH/mm² which is > 8× higher than that of planar spiral inductors [4]. The IVR demonstrates stable closed-loop behavior with the 3-D-TSV inductor structures even at very high switching frequencies around 90 MHz. High light load efficiency with a peak of 80% has been demonstrated which remains relatively flat across the load range of 1.5–25 mA with both hysteretic and PFM control modes. In PFM control, the ON time needs to be set optimally to maximize efficiency and minimize output ripple for PFM. While the efficiency in this prototype is only slightly better than that of an equivalent low drop out regulator (LDO), the design parameters for obtaining larger inductance values as described in Section III can be used to improve efficiency at the cost of power density. In addition, any improvements to the TSV structure to improve resistance can improve the overall efficiency without compromising on power density.

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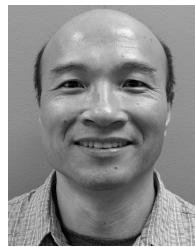
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