CHIMERA: A Field-Programmable Mixed-Signal IC With Time-Domain Configurable Analog Blocks

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***Abstract*— This paper presents a field-programmable mixed-signal IC named CHIMERA, for low-cost and rapid prototyping of mixed-signal systems. The proposed IC implements field-programmable analog functions with time-domain configurable analog blocks (TCABs). A single TCAB can be programmed to various analog circuits, including a time-to-digital converter, digitally-controlled oscillator, digitally-controlled delay cell, digital pulse-width modulator, and phase interpolator. The TCABs convey and process analog information using the frequency, pulse width, delay, or phase of digital pulses or pulse sequences, rather than using analog voltage or current signals for reduced susceptibility to attenuation and noise. The overall CHIMERA chip also includes arrays of configurable logic blocks (CLBs) and programmable arithmetic logic units (ALUs) for programmable digital functions. By programming the functionality of the TCAB, CLB, and ALU arrays and configuring the interconnects, the chip can implement various mixed-signal systems. A prototype IC fabricated with 65-nm CMOS technology demonstrates the versatile programmability of CHIMERA by being successfully operated as a 1-GHz phase-locked loop with a 12.3-ps$_{\text{rms}}$ integrated jitter, as a 50-MS/s analog-to-digital converter with a 32.5-dB SNDR, and as a 1.2-to-0.7 V DC–DC converter with 95.5% efficiency.**

***Index Terms*— Field-programmable mixed-signal IC, mixed-signal IC, mixed-signal system, reconfigurable architecture, reconfigurable mixed-signal IC.**

I. Introduction

THE fast emergence of Internet-of-Things applications requires the development of a variety of new mixed-signal ICs with fast production cycles and low cost. While FPGAs are established solutions for timely and low-cost prototyping of digital systems [1], [2], finding their counterparts for analog circuits is still an active research topic [3]–[9]. This paper provides an in-depth description of a new field-programmable IC for analog/mixed-signal circuits named CHIMERA [10], which solves the various challenges encountered in previous studies by performing analog functions in time domain.

To the best of our knowledge, this work is the first to present a field-programmable single unit analog block whose input-to-output function can be changed via programming. This is analogous to the configurable logic blocks (CLBs) used in digital FPGAs. By contrast, previous works involve unit blocks having fixed input-to-output functions, and only the interconnect blocks among them are programmable. For example, the work in [3] uses an array of transconductance (G_m) cells, where only the parametric characteristics, such as gain and bandwidth, are programmable. Further, although the field-programmable ICs in [5] and [6] contain diverse active circuits (e.g., OTAs, current mirrors, and Gilbert multiplier) and passive components, each block still has fixed functionality and the reconfigurable connections among the blocks enable the overall programmable function.

Most previously reported ICs [3]–[9] suffer from a loss in signal quality when signals propagate through the programmable interconnects in analog voltage or current forms. For instance, analog voltages propagating via long interconnects and switches are susceptible to attenuation, because of the resistance and capacitance of the circuit network. Additionally, their signal-to-noise ratio can be easily degraded by noise and interference coupled into the network. Even though inserting analog buffers (e.g., unity-gain amplifiers) can mitigate these issues to some degree, they are typically power hungry.

CHIMERA presented in this paper both achieves the programmable input-to-output functionality of its unit analog blocks and solves the scalability problem of the programmable interconnects, by conveying and processing analog information in the form of modulated digital pulses or pulse sequences. For instance, its proposed time-domain configurable analog blocks (TCABs) can be programmed to various analog circuits, including time-to-digital converters (TDCs), digitally-controlled oscillators (DCOs), digitally-controlled delay cells, digital pulse-width modulators (DPWMs), and phase interpolators (PIs). The TCABs receive and produce analog information in the form of digital pulses, whose frequency, delay, phase, or pulse width changes with the signal to be conveyed. Hence, the analog information expressed in the digital pulses can then reliably propagate through more scalable digital programmable interconnects (e.g., made of tri-state buffers and digital buffers) with less susceptibility to attenuation and noise.

In addition to the TCABs for the programmable analog functionality, CHIMERA also includes arrays of CLBs and arithmetic logic units (ALUs) for programmable digital functionality. Users can program both the functionality of the TCABs, CLBs, and ALUs and the connectivity among these blocks, thus implementing various mixed-signal systems. To demonstrate its programmability, a prototype IC fabricated with 65-nm CMOS technology is programmed as three representative systems: a 1-GHz phase-locked loop (PLL) with a 12.3-ps$_{\text{rms}}$ integrated jitter, a 50-MS/s analog-to-digital

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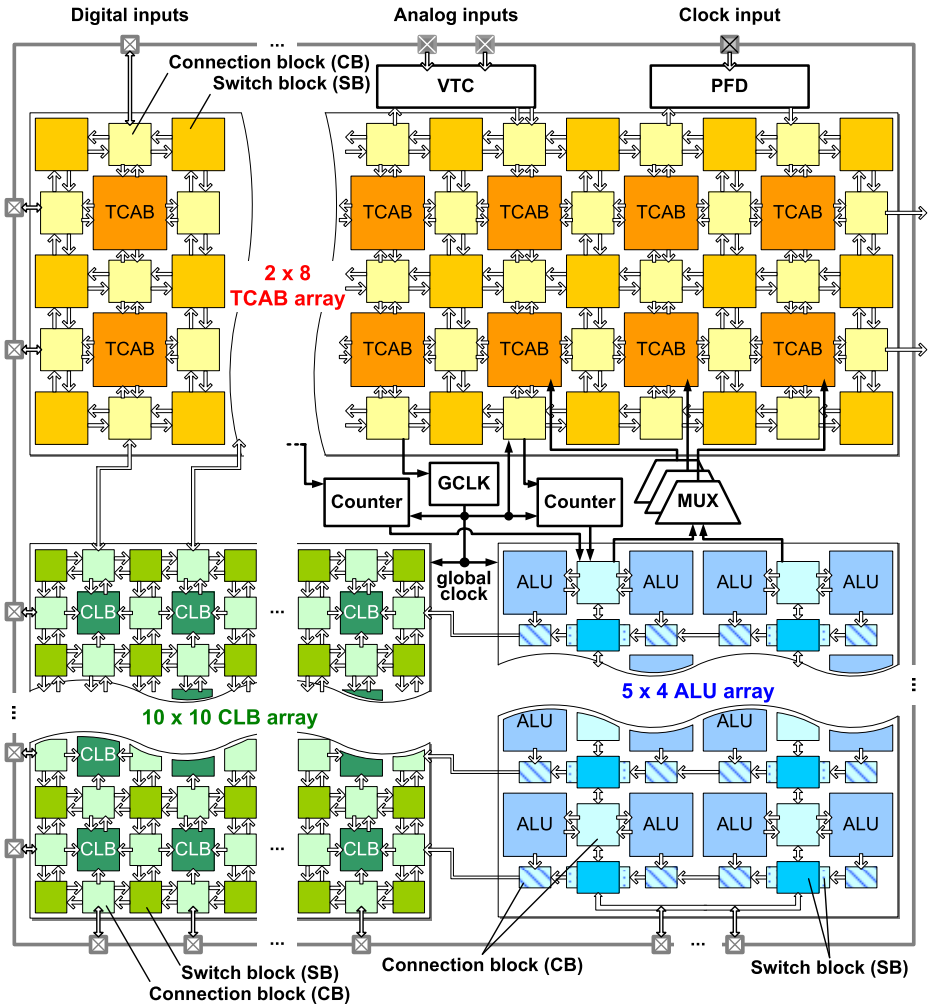

Fig. 1. Architecture and floorplan of the proposed field-programmable mixed-signal IC, CHIMERA.

converter (ADC) with a 32.5-dB SNDR, and a 1.2-to-0.7 V dc–dc converter with 95.5% efficiency.

The remainder of this paper is organized as follows. The overall architecture of CHIMERA is presented in Section II, followed by a description of the key unit block, TCAB, in Section III. Section IV covers the implementation of the other building blocks, the CLBs, ALUs, and gluing blocks connecting them. Section V presents the measurement results obtained from a fabricated prototype IC to demonstrate the versatile programmability of CHIMERA. Finally, Section VI concludes this paper.

II. Overall Architecture of CHIMERA

The integrated systems of today consist of tightly coupled analog circuits and digital logic blocks. In most cases, the digital blocks are included to perform a variety of adaptation or calibration tasks, and closely interact with the analog blocks. Further, as technology scales, digitally assisted analog design techniques [11] are being increasingly used to overcome the difficulties in analog circuit design (e.g., due to mismatch, non-linearity, gate leakage, or low supply voltage) by replacing some part of analog circuits with digital ones, or by mitigating the non-ideality effects of analog circuits with digital calibration. For example, it is usual in mixed-signal feedback systems to adopt a topology consisting of analog sensors, a digital controller, and analog actuators. An example can be found in digital PLLs, which are composed of a TDC, digital loop filter, and DCO. This mixed-signal feedback structure is also utilized when implementing dc–dc converters with an ADC, digital loop filter, and DPWM.

To program such mixed-signal feedback systems or digitally assisted analog systems, CHIMERA employs the architecture depicted in Fig. 1. The IC broadly consists of three arrays of TCABs, CLBs, and ALUs, respectively. In each array, the TCABs, CLBs, or ALUs are placed regularly, and are surrounded by wire tracks with connection blocks and switch blocks. The CHIMERA IC also includes gluing blocks, such as a voltage-to-time converter (VTC) block, phase-frequency detector (PFD) block, and counter blocks as interfaces between the arrays or between an array and the I/O.

Various analog/mixed-signal feedback systems can be programmed on CHIMERA by mapping their analog sensors and actuators to TCABs, and their digital controllers to ALUs or CLBs. The input-to-output function of each TCAB can be changed by the user, so that it performs the function of the analog blocks required in the target system. The Boolean

logic required by the system is programmed on the CLB array. Last, any digital arithmetic logic is programmed on ALUs. For instance, one can program a digital PLL on CHIMERA by configuring TCABs to operate as the TDC and DCO, and programming the digital loop filter into the ALUs and CLBs.

It should be noted that, when implementing the desired mixed-signal systems on CHIMERA, the required analog blocks (e.g., TDCs, DCOs, DPWMs, digitally-controlled delay cells, or PIs) are realized solely by programming the TCABs. In common, the listed analog blocks are basically time-domain analog circuits. That is, their inputs and outputs are binary digital pulses of which time-domain quantity (such as pulse width, frequency, delay, or phase) encodes analog information. Based on this observation, the key unit block, TCAB, which can change its input-to-output functionality to that of the time-domain analog blocks constituting mixed-signal feedback systems, such as digital PLL, ADC, and dc–dc converter, is proposed. A detailed description of the features and circuit implementation of TCAB is provided in Section III.

III. Time-Domain Configurable Analog Block

The fact that programmable analog function is achieved solely by the TCABs is one of the most noteworthy differences of CHIMERA when compared to previously reported approaches. As described, it contrasts to the works which include unit analog blocks whose input-to-output functions are fixed and unchangeable [3], [5], [6] and provide programmable function by reconfiguring the connections among the unit analog blocks [5], [6]. CHIMERA must also be distinguished from the approach in [8], where transistor-level programmability is provided by unit blocks that emulate the behavior of each transistor of the target system. Although this approach is suitable to program small-scale analog circuits (e.g., OTAs or analog filters), it is difficult to extend to the programming of the complex mixed-signal systems of today. In contrast, each TCAB in CHIMERA maps the functionality of a full analog circuit, rather than its detailed structural topology.

Another important aspect of the TCAB is that it processes signals in the time domain, receiving and producing digital pulses whose frequency, delay, phase, or pulse width presents the analog information. Fig. 2 illustrates the TCAB signal processing approach in comparison with the continuous voltage signals of conventional analog blocks. Instead of representing the analog information by voltage or current forms, the TCABs encode the information into the frequency, pulse width, delay, or phase of digital pulses. Interestingly, this approach is similar to that adopted by time-based ADCs to overcome the various challenges in ADC design (e.g., low supply voltage) as technology scales [11], [12].

Because the inputs and outputs of the TCABs are digital pulses that are less susceptible to noise or distortion than signals in voltage or current forms, CHIMERA can achieve high programmability of the signal propagation path. In fact, most previous works [3]–[9] process signals in analog voltage or current forms, which are sensitive to noise and distortion when the signals propagate through programmable interconnects. Because of such difficulties,

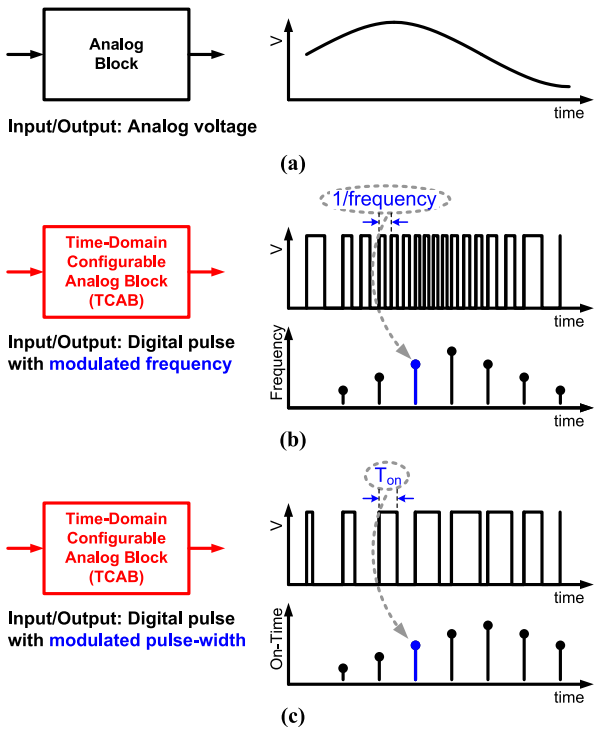

Fig. 2. Comparison of information representations. (a) Conventional analog blocks. (b) TCAB with pulse frequency modulation. (c) TCAB with pulse-width modulation.

[3] considers permanent connections between adjacent blocks without any programmability on signal path. Another implementation [7] employs programmable switches only between adjacent blocks. In [6], limited analog buffers (e.g., OTA-based unity-gain buffers) are inserted to convey analog signals farther, whereas most of the other interconnects are floating-gate-based switches with finite parasitic capacitance and resistance. Such transmission gate-based switches with the finite resistance (up to few hundred Ω) have limit on the level of flowing current to avoid the destruction of the functionality due to the voltage drop across the switches. On the other hand, the inputs and outputs of the TCABs, which are digital binary pulses, can reliably propagate through programmable interconnects. Further, the interconnect blocks connecting the TCABs are simply implemented with digital tri-state inverters and buffers. The digital inverters and buffers also suffer from the propagation delay variation under supply change, introducing absolute timing error. For example, a buffer chain with ten stages of fan-out four inverters in the technology where CHIMERA has been fabricated has a total propagation delay of 245 ps and delay sensitivity of 338 fs/mV to the supply. However, the relative time difference between time point of the current rising edge and the next rising edge (i.e., period), or the current rising edge and the next falling edge (i.e., on-time), which is the way of the TCAB represents information, is affected far less since the edges exhibit same delay change. As a result, the pulse-modulation-based time-domain representation of the analog information makes it easy to implement large-size TCAB arrays.

The following sections describe the circuit implementation of the TCABs, and explain how their input-to-output func-

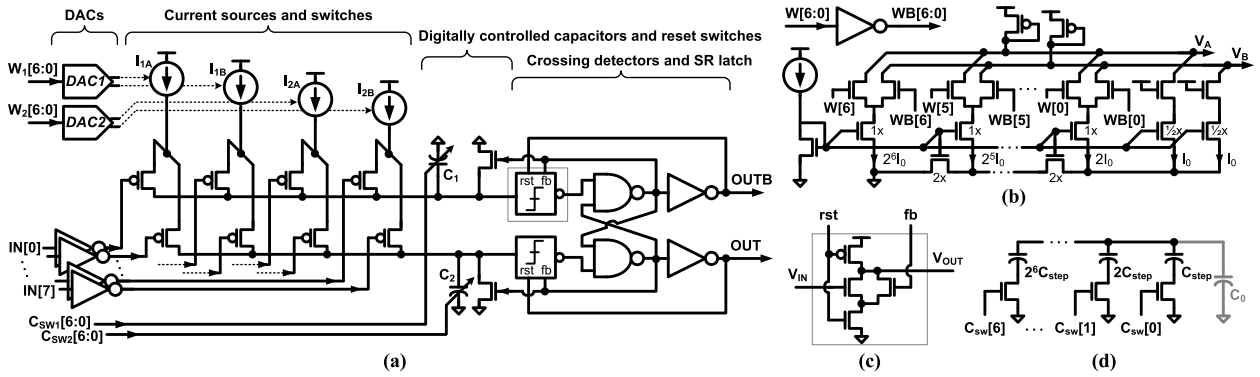

Fig. 3. Circuit implementations of the (a) proposed TCAB, (b) nMOS ladder-based current-steering DAC, (c) crossing detector, and (d) digitally-controlled capacitors.

tions can be changed. The TCAB array composition is also described.

A. Circuit Implementation of TCAB

Fig. 3(a) shows the circuit implementation of the proposed TCABs. Each TCAB consists of four switched current sources (whose output current level is controlled by the leading DACs), two digitally-controlled capacitors with reset switches, crossing detectors, and an SR-latch. The current sources I_{1A}/I_{1B} and I_{2A}/I_{2B} selectively charge the digitally-controlled capacitors C_1 and C_2, depending on how the switches under each current source are configured by the eight input signals IN[7:0]. Once a non-zero current flows to C_1 and the voltage across C_1 exceeds the established threshold voltage, the following crossing detector [Fig. 3(c)] switches to low, and the SR-latch toggles the OUT and $OUTB$ signals to logic 1 and logic 0, respectively. Simultaneously, C_1 is discharged, its voltage being reset to zero by the reset switch. C_2 will then be charged, whereas C_1 is maintained uncharged. When the voltage across C_2 exceeds the threshold, OUT and $OUTB$ toggle back to logic 0 and logic 1, respectively. This means that only one of the two capacitors is being charged at a time, in an alternating fashion, while the output pulses are being generated.

The modulation of the TCAB output pulses—which carries the analog information—is controlled by the way in which the capacitors are charged. That is, by adjusting the currents into C_1 and C_2, or the capacitances of C_1 and C_2, the time required for each capacitor to reach the threshold voltage (and, therefore, the time after which the output pulses are toggled) can be controlled.

The charging behavior depends on the configuration of the eight switches, which are turned on or off by IN[7:0]. When the switches are configured in such a way that constant current I_{C1} (or I_{C2}) flow into C_1 (or C_2), the time required for each output pulse to be asserted after C_1 (or C_2) starts charging is

$$t_{OUT} = \frac{V_{th}C_1}{I_{C1}} + t_{xing} + t_{logic}$$
$$t_{OUTB} = \frac{V_{th}C_2}{I_{C2}} + t_{xing} + t_{logic} \quad (1)$$

where V_{th} is the crossing detector threshold voltage, t_{xing} denotes the crossing detector delay, and t_{logic} is the delay of the logic gates from the SR-latch inputs to the $OUT/OUTB$ signal pins. In this case, the output pulses oscillate with an oscillation period given by

$$T_{period} = \frac{V_{th}C_1}{I_{C1}} + \frac{V_{th}C_2}{I_{C2}} + 2(t_{xing} + t_{logic} + t_{reset}) \quad (2)$$

where t_{reset} denotes the time it takes for one of the capacitor reset switches to be released from the moment the other capacitor reaches V_{th}. If the switch configuration changes in the middle of charging and no current flows to C_1 or C_2 for a moment, the voltage across the capacitor holds its value. When the switch configuration changes again and charging resumes, the output pulse is eventually asserted.

Another way to control the charging behavior is to change the current levels using the DACs. Each pair of current sources in the TCAB, I_{1A}/I_{1B} or I_{2A}/I_{2B}, is controlled by the leading DACs, so that the output currents within each pair are biased to be complementary to each other. That is, $I_{1A} + I_{1B}$ (or $I_{2A} + I_{2B}$) remains constant regardless of W_1 (W_2). If W_1 (W_2) increases, I_{1A} (I_{2A}) increases and I_{1B} (I_{2B}) decreases; the opposite happens if W_1 (W_2) decreases. To bias the paired current sources in this way, the nMOS ladder-based current-steering DAC generates two voltages, V_A and V_B, as shown in Fig. 3(b). Considering that multiple TCABs are included in CHIMERA, the DAC in [14] is adopted for the TCABs owing to its low-power consumption and compact size.

Last, it is also possible to adjust the charging rate by changing the capacitances of C_1 and C_2. Each capacitor is basically an array of binary weighted capacitors with switches that are turned on/off by C_{SW1}[6:0] or C_{SW2}[6:0], respectively, as shown in Fig. 3(d). Their equivalent output capacitances are

$$C_1 = C_0 + C_{step} \times \sum_{n=0}^{6} 2^n C_{SW1}[n]$$
$$C_2 = C_0 + C_{step} \times \sum_{n=0}^{6} 2^n C_{SW2}[n] \quad (3)$$

where C_{step} is the unit capacitance and C_0 includes all the parasitic capacitances of that node and the input capacitance of the ensuing crossing detector. Therefore, the charging rate is controlled via C_{SW1}[6:0] or C_{SW2}[6:0].

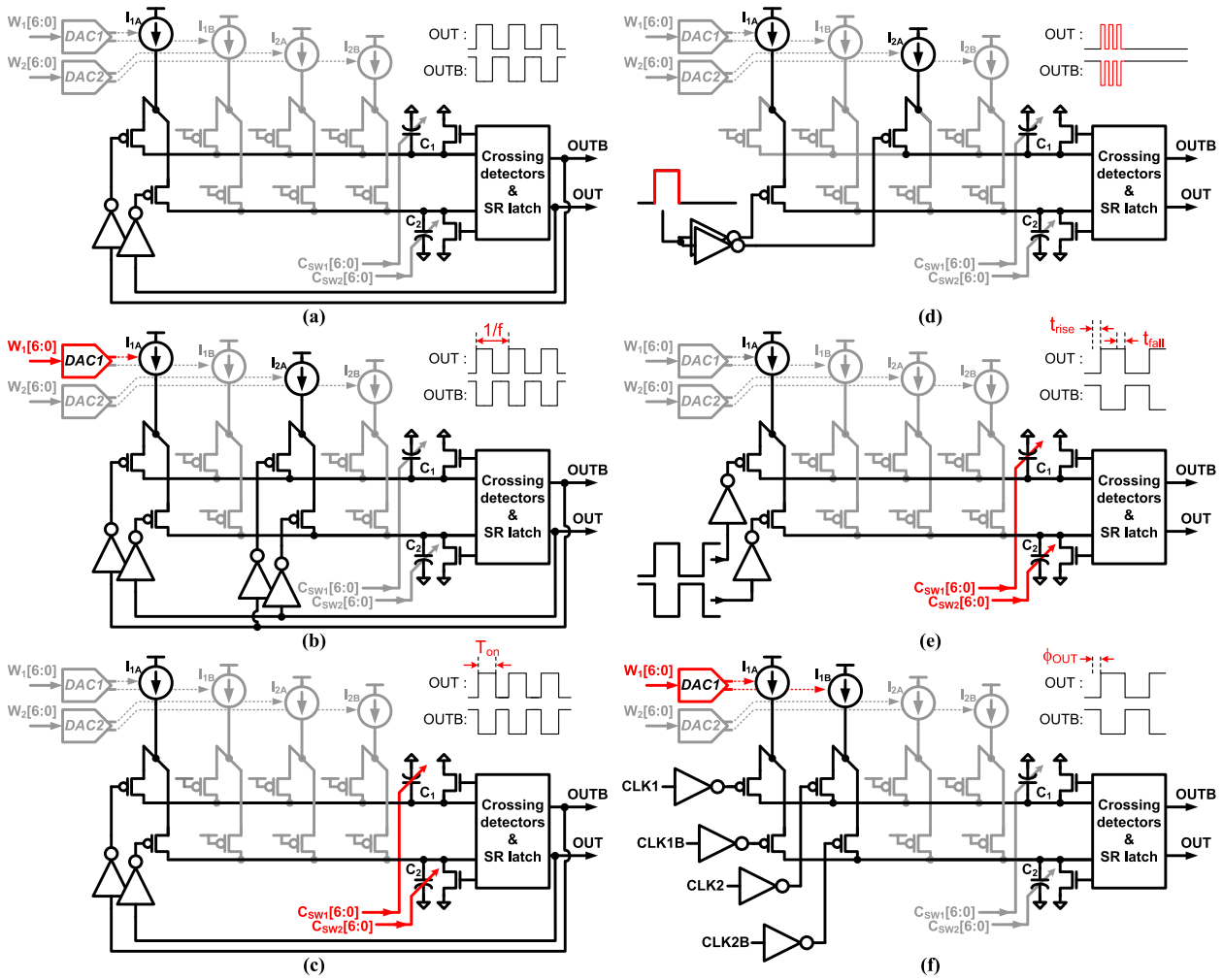

Fig. 4. TCAB configurations when it operates as a (a) fixed-frequency relaxation oscillator, (b) DCO, (c) DPWM, (d) gated oscillator, (e) delay cell, and (f) PI.

B. Versatile Programmability of TCAB

To explain how the input-to-output function of the TCAB changes, Fig. 4 shows a TCAB operating as six different analog blocks that are typically required when composing timing generation, data conversion, or power management ICs. As can be seen, its input-to-output function changes completely, depending on how the three kinds of inputs (i.e., *IN* for the switch configuration, W_1 and W_2 for the DACs, and C_{SW1} and C_{SW2} for the digitally-controlled capacitors) are controlled.

In the first example, as shown in Fig. 4(a), the TCAB operates as a relaxation oscillator [15]. In this configuration, OUT and $OUTB$ are connected back to $IN[1]$ and $IN[0]$, respectively. Because of the complementarity of OUT and $OUTB$, current I_{1A} is always fully steered to one of the two capacitors. Therefore, C_1 and C_2 are alternatively charged, and the output pulses are toggled. If C_1 and C_2 have the same capacitance, the configured TCAB operates as a relaxation oscillator, whose period (T_{period}) is

$$T_{period} = 2\left(\frac{V_{th}C_1}{I_{1A}} + t_{xing} + t_{logic} + t_{reset}\right). \quad (4)$$

By changing the current level of I_{1A} (via $W_1[6:0]$) or the capacitance values (via $C_{SW1}[6:0]$ and $C_{SW2}[6:0]$), the TCAB can be reconfigured to a different relaxation oscillator, with a different period.

A second example is shown in Fig. 4(b), where the TCAB operates as a DCO by connecting OUT to $IN[1]$ and $IN[5]$, and $OUTB$ to $IN[0]$ and $IN[4]$. In this configuration, currents I_{1A} and I_{2A} are always fully steered to one of the two capacitors, alternately charging C_1 or C_2. Assuming that t_{xing}, t_{logic}, and t_{reset} are relatively small compared with the charging time of the capacitors, the output frequency of the TCAB (f_{osc}) is given by (5), as a function of $W_1[6:0]$

$$f_{osc} \cong \frac{I_{1A} + I_{2A}}{2V_{th}C_1} = \frac{k \times W_1 + I_{2A}}{2V_{th}C_1} \quad (5)$$

where k is the gain from the DAC input to I_{1A} (i.e., $\Delta I_{1A}/\Delta W_1$).

A third example is shown in Fig. 4(c), where the TCAB, configured similar to Fig. 4(a), operates as a DPWM [15]. In this case, the capacitances of C_1 and C_2 are adjusted in a complementary fashion through $C_{SW1}[6:0]$ and $C_{SW2}[6:0]$, respectively, maintaining a constant sum of those two digital input codes: 127. The TCAB exhibits the same behavior

in Fig. 4(a), with an oscillation period given by (2), but with a duty-cycle of the output pulse OUT given by (6), as a function of C_{SW2}[6:0]

$$D = \frac{T_{on}}{T_{period}} = \frac{V_{th}C_2/I_{1A} + t_{xing} + t_{logic} + t_{reset}}{V_{th}C_1/I_{1A} + V_{th}C_2/I_{1A} + 2(t_{xing} + t_{logic} + t_{reset})} \cong \frac{C_0 + C_{SW2} \times C_{step}}{2 \times C_0 + 127 \times C_{step}}. \quad (6)$$

A fourth example is the gated oscillator shown in Fig. 4(d). In this case, an external input is connected to the input switches, so that the circuit oscillates only when the input is high. With this TCAB followed by a counter, one can emulate a TDC [16]. The counter records the number of edge transitions in the output pulse, which is proportional to the on-time of the input pulse. The output of counter—which is digital by nature—provides a quantized estimate of the input pulse width.

In the next example, as shown in Fig. 4(e), the TCAB is used as a digitally-controlled delay cell. A pair of complementary input signals is connected to IN[1:0] and steers the current I_{1A} between C_1 and C_2. In this case, only C_1 gets charged if IN[0] is high, and only C_2 gets charged if IN[1] is high. Therefore, the outputs do not oscillate and toggle only once, with the rising- or falling-edge delays being given by

$$t_{rise} = \frac{V_{th}C_1}{I_{1A}} + t_{xing} + t_{logic}, \quad t_{fall} = \frac{V_{th}C_2}{I_{1A}} + t_{xing} + t_{logic}. \quad (7)$$

By adjusting C_1 and C_2, the delay can be controlled linearly as a function of C_{SW1}[6:0] and C_{SW2}[6:0].

As a final example, the case of a TCAB operating as a PI is shown in Fig. 4(f). In this configuration, two pairs of complementary input signals steer the current I_{1A} and I_{1B}, respectively. The circuit generates a delay, which is a weighted sum of the delays from the two input pairs with different arrival times [17]. Thus, when the phase of *CLK1* (ϕ_{CLK1}) precedes that of *CLK2* (ϕ_{CLK2}) (i.e., $\phi_{CLK1} < \phi_{CLK2}$), the output phase ($\phi_{OUT}$) is given by

$$\phi_{OUT} = \phi_{CLK2} + 2\pi f \frac{CV_{th}}{I_{1A} + I_{2B}} - (\phi_{CLK2} - \phi_{CLK1}) \frac{I_{1A}}{I_{1A} + I_{2B}} \quad (8)$$

where f is the frequency of *CLK1* and *CLK2*. As W_1[6:0] increases, ϕ_{OUT} is obtained earlier, given that I_{1A} increases, while $I_{1A} + I_{1B}$ is maintained constant.

C. TCAB Array With Programmable Interconnects

As illustrated in Fig. 1, the TCAB array composition follows a traditional 2-D island-style architecture, which is commonly adopted among commercial FPGAs [18]. Multiple TCABs are regularly placed on a 2-D grid, and each TCAB is surrounded by wire tracks and programmable interconnect blocks—switch blocks and connection blocks. The directional four wires are placed both horizontally and vertically. The input and output

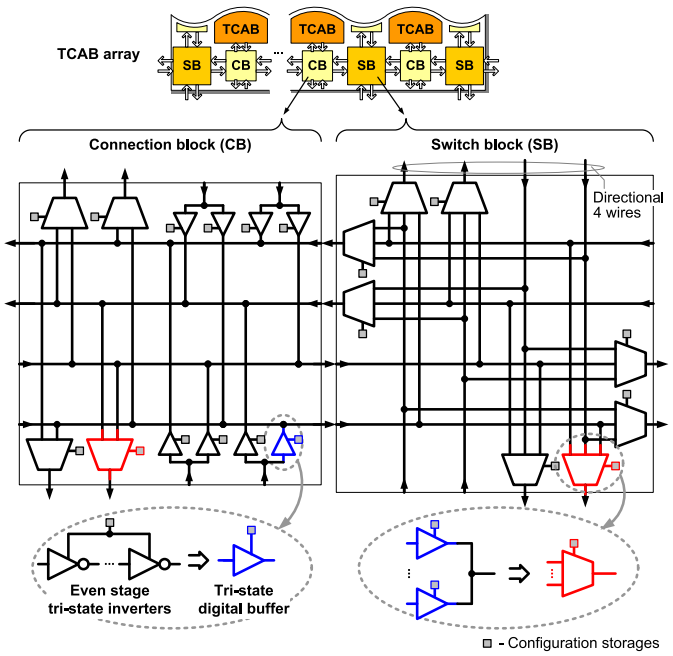

Fig. 5. Composition of the TCAB array, and block diagram of the programmable interconnects in the array.

signals of each TCAB are connected to the surrounding wire tracks via connection blocks. The adjacent wire tracks are interconnected via switch blocks placed at the intersection of the horizontal and vertical tracks.

Since the TCABs receive and produce digital pulses, the switch blocks and connection blocks in the TCAB array are simply implemented based on digital tri-state inverters, as shown in Fig. 5. Depending on which tri-state inverters are turned on, the connection block decides which routing wires to connect to the input and output signals of the TCABs. Likewise, the tri-state inverters in the switch blocks decide if the received signals go forward, left, or right. This programmable routing architecture follows that of commercial FPGAs [18], facilitating the high programmability of the signal paths.

When sizing the tri-state inverters for the switch blocks and connection blocks, the tradeoff between propagation delay and power should be considered. Optimization between the delay and power consumption of the CMOS gate is actually well-studied problem with the established solution. Many researches have proved that the fan-out of each stage should be about four for the optimum [19], [20]. Therefore, tri-state inverters for each connection block or switch block in the TCAB array are sized to be fan-out around 4, considering both the input capacitance of the next stage inverter and the capacitance of wire.

Among the input and output signals of the TCAB, only the input pulses (i.e., IN[7:0]) and output pulses (i.e., OUT and $OUTB$) are conveyed through the described programmable interconnects. For the other input signals (i.e., W_1[6:0], W_2[6:0], C_{SW1}[6:0], and C_{SW2}[6:0]), it is sufficient to program them with fixed constants or to directly connect them to the output of the ALU array. For example, the digital input codes are programmed with fixed constants when the TCAB

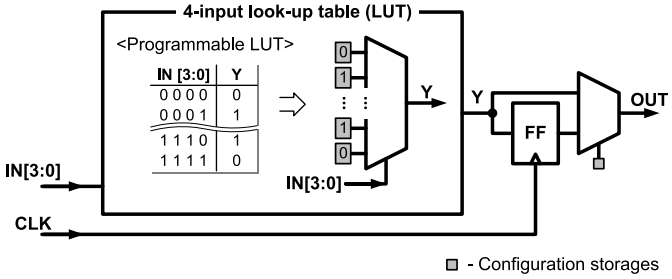

Fig. 6. Block diagram of the CLB in CHIMERA.

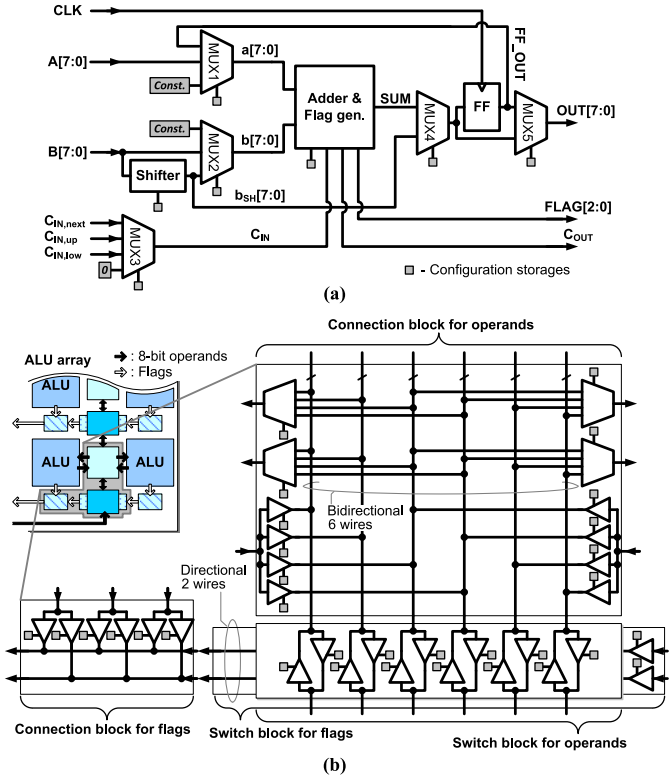

Fig. 7. (a) Block diagram of the programmable ALU. (b) Composition of the ALU array in CHIMERA.

is programmed as a fixed-frequency gated oscillator whose frequency does not have to change at run time. On the other hand, if the TCAB is programmed as a DCO whose output frequency must be controlled by its digital input code words in real time, these digital code words are either the result of some of the ALUs, or are received from outside the IC via I/O. To allow this case, the three TCABs in the lower left corner of the TCAB array have direct connections to the ALU array, as shown in Fig. 1. It means that the number of TCABs that can simultaneously receive the digital input codes from the ALU array is limited to three, even though the number of individual routing tracks in the ALU array is larger than three. However, the number is not small, considering the number of the path from digital filter to analog actuator is usually limited in the conventional mixed-signal feedback systems.

IV. Implementation of the Programmable Digital Blocks and Gluing Blocks

A. Configurable Logic Block Array

To allow the programming of arbitrary digital logic required for the target mixed-signal systems, the CHIMERA IC contains look-up table (LUT)-based CLBs. As shown in Fig. 6, each CLB consists of a programmable LUT whose output is connected to a D flip-flop, followed by a multiplexer that selects the final CLB output from either the output of the LUT or the output of the D flip-flop. The included LUT has 4 input bits and 16 rows. Therefore, a single CLB is capable of implementing any Boolean logic function with 4 inputs, depending on how the respective LUT is programmed. The programmed logic becomes either combinational or sequential, depending on the selection made by the multiplexer. For sequential logic, the CLBs also receive a common triggering clock for the D flip-flop from the global clock (GCLK) block. More complex logic functions, with more than 4 inputs, can be implemented by combining multiple CLBs.

The CLB array is composed of 100 CLBs together with connection blocks and switch blocks, following the 2-D island-style. The connection blocks and switch blocks in the CLB array are also implemented with digital tri-state inverters, like those in the TCAB array. The arbitrary digital logic written in Verilog is synthesized, and its place-and-route onto the CLB array is performed using the Verilog-to-Routing open-source academic software suite [21]–[23].

B. Arithmetic Logic Unit Array

Even though the CLB array can be programmed to perform any digital logic (including arithmetic logic), CHIMERA additionally contains the ALU array to avoid the area overhead or performance degradation that can occur when performing digital arithmetic operations using only the LUT-based CLBs. This strategy is similar to that of many modern FPGAs, which contain specific purpose blocks such as adders, multipliers, DSPs, or memory [24]. In the CHIMERA case, the ALU array is in charge of digital arithmetic. Therefore, any digital filters required in the target mixed-signal feedback systems can be programmed onto the ALU array with higher logic density and shorter critical path delays.

As illustrated in Fig. 7(a), each ALU includes an adder capable of both addition and subtraction, a shifter, a flip-flop, and five multiplexers, receiving up to two 8-bit operands and producing an 8-bit operation result and flag signals. It can be programmed to perform arithmetic operations such as addition, subtraction, accumulation, or arithmetic shift. For example, an ALU is configured as an accumulator that accumulates input B[7:0] if the included adder is programmed to perform addition and MUX1 through MUX5 are programmed to select FF_OUT, B[7:0], 0, SUM, and the output of MUX4, respectively. Arithmetic flags are produced as subsidiary results in every ALU. For instance, the flag bits indicate which of the two operands of the adder is larger, or whether the two are equal. The ALUs are also capable of supporting wider bit-width operands. By using two or three adjacent ALUs exchanging carries with each other, an extended 16-bit or 24-bit ALU can also be configured.

Overall, the ALU array is composed of 20 ALUs and two different sets of programmable interconnects. The 8-bit operands or results are conveyed through vertical bidirectional wire tracks, so that the signals can be conveyed either up or down. In contrast, the resulting flags are con-

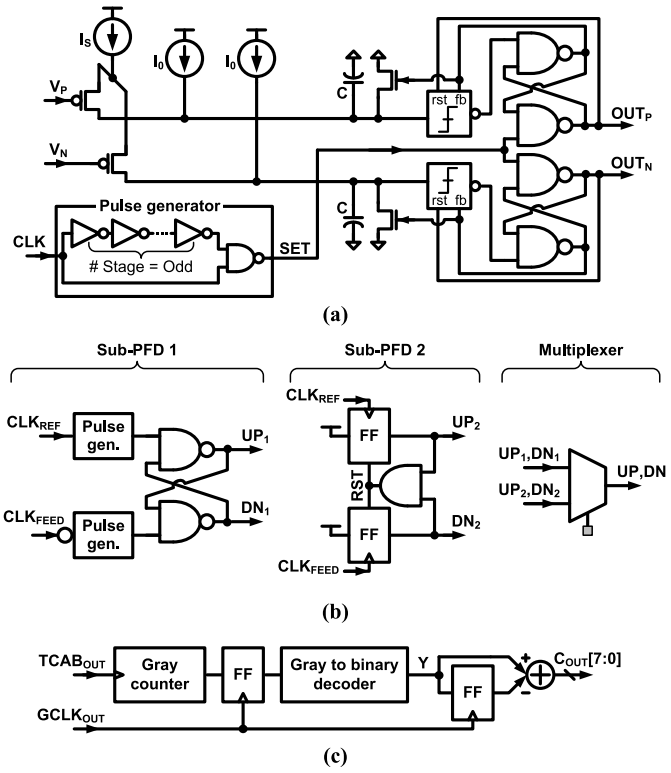

Fig. 8. Circuit implementation of a (a) VTC, (b) PFD, and (c) counter block.

veyed through horizontal wire tracks, and eventually transferred to the CLB array, as shown in Fig. 7(b). The connection and switch blocks in the ALU array are implemented with tri-state inverters, like those in the TCAB or CLB arrays. The ALU array can receive input operands from the counter blocks or from the outside, and feed its final results into the TCAB array or transmit them to the outside.

C. Gluing Blocks

The described three arrays of programmable function blocks interact with external I/O or with each other not only through direct connections, but also using gluing blocks, as illustrated earlier, in Fig. 1. Since all the TCABs, CLBs, and ALUs receive and produce binary digital signals, it would be possible to implement the IC with only direct connections among the three arrays. However, in this case, the CHIMERA IC would be limited to only receive digital pulses or binary digits as inputs. By adopting VTC and PFD that convert external signals to pulse-width modulated signals, the IC can accept various external analog signals as input. In addition, a counter block converts a pulse sequence into 8-bit binary digits when the information is transferred from the TCAB array to the ALU array. Last, a GCLK unit is used to generate and distribute a clock with optional frequency division.

First, the VTC—which is adopted to allow an external analog voltage to be used as input to the IC—is implemented and behaves similar to the TCABs, as shown in Fig. 8(a). Once CLK is asserted, the pulse generator creates a short pulse, SET, to force both OUT_P and OUT_N high, and release

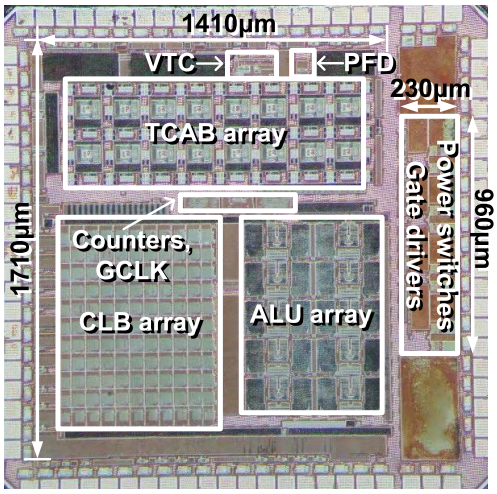

Fig. 9. Chip micrograph (active layers only).

the reset switches next to the capacitors. The current sources then start charging the capacitors. The current I_S is steered by the difference between V_P and V_N. Therefore, the time it takes for each output to make a falling-edge transition after the beginning of the capacitor charge (i.e., the pulse width of the output) is

$$T_{on,P} = \frac{CV_{th}}{I_0 + I_S - g_m(V_P - V_N)} + t_{xing} + t_{logic}$$
$$T_{on,N} = \frac{CV_{th}}{I_0 + I_S + g_m(V_P - V_N)} + t_{xing} + t_{logic} \quad (9)$$

where g_m is the input transistor transconductance, I_0 is output current level of the current source which directly charges each capacitor and I_S is output current level of the current source whose output is steered into two capacitors by input voltage difference [see Fig. 8(a)], and t_{xing} and t_{logic} denote the delays of the crossing detector and logic gates from the SR-latch inputs to OUT_P or OUT_N, respectively. As a result, V_P and V_N are converted into digital pulses whose pulse widths are a function of $V_P - V_N$.

Next, the PFD—which is adopted to convert the phase or frequency difference between two clock signals to pulse-width-modulated signals—is implemented, as shown in Fig. 8(b). It includes two sub-PFDs and a multiplexer to select the final result. The first sub-PFD can only compare the phases of two inputs with the same frequency. For example, if CLK_{REF} leads CLK_{FEED}, the pulse-width of UP_1 will be larger than that of DN_1, and vice versa. When the two inputs have the same phase, it generates UP_1 and DN_1 with identical pulse widths and 50% duty cycles. The second sub-PFD can evaluate both the phase and frequency difference of the two inputs. If the frequency of CLK_{REF} is higher than that of CLK_{FEED}, or if CLK_{REF} leads CLK_{FEED}, the pulse width of UP_2 will be larger than that of DN_2 and vice versa. If the two inputs have the same frequency and phase, it generates identical pulses on UP_2 and DN_2, with the very short pulse corresponding to the reset path delay of the flip-flops. In this way, the phase or frequency difference of the two inputs is converted into digital pulses.

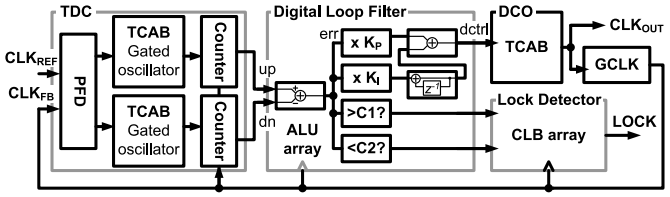

Fig. 10. CHIMERA configuration as a 1-GHz digital PLL.

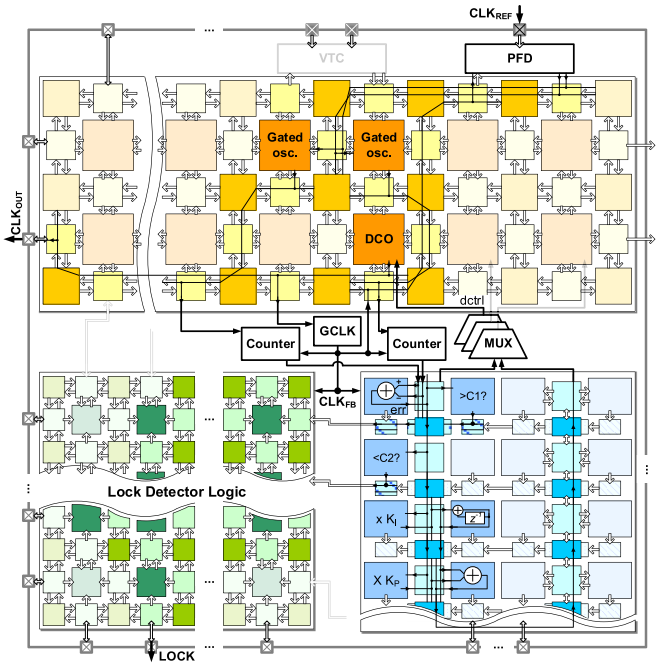

Fig. 11. Example placement and routing of the digital PLL in Fig. 10 on the CHIMERA IC.

Last, digital counter blocks are employed to interface the TCAB and ALU arrays. That is, a translation of the pulse-modulated information into a binary number is performed by the counters. Basically, they count the number of edge transitions in the output pulse train of the TCAB, as shown in Fig. 8(c). At every rising edge of the received $TCAB_{OUT}$, the gray counter [25] increases its output. The result is then sampled by the subsequent flip-flop, whose triggering clock is $GCLK_{OUT}$. Especially, a gray counter is adopted, instead of a binary counter, in order to minimize the risk of sampling the wrong bit stream, which frequently occurs if $GCLK_{OUT}$ is asserted while the counter output is transitioning. After being decoded into a binary number, the final count number, $C_{OUT}[7{:}0]$, is computed by subtracting the previous count number from the current count (i.e., $C_{OUT}[n] = Y[n] - Y[n-1]$). As a result, the counter block is capable of representing how fast the TCAB is generating the pulses.

V. Mixed-Signal System Examples and Experimental Results

A prototype IC was fabricated with 65-nm LP CMOS technology, operating with a 1.2 V supply. The chip micrograph is shown in Fig. 9. The chip occupies 2.411 mm^2, including the scan chain flip-flops storing a total of 12 626 configuration bits. In specific, the TCAB array occupies 0.534 mm^2 (including

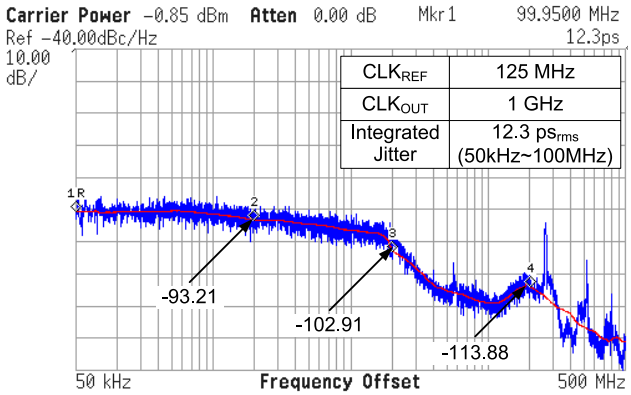

Fig. 12. Measured phase noise of the programmed digital PLL.

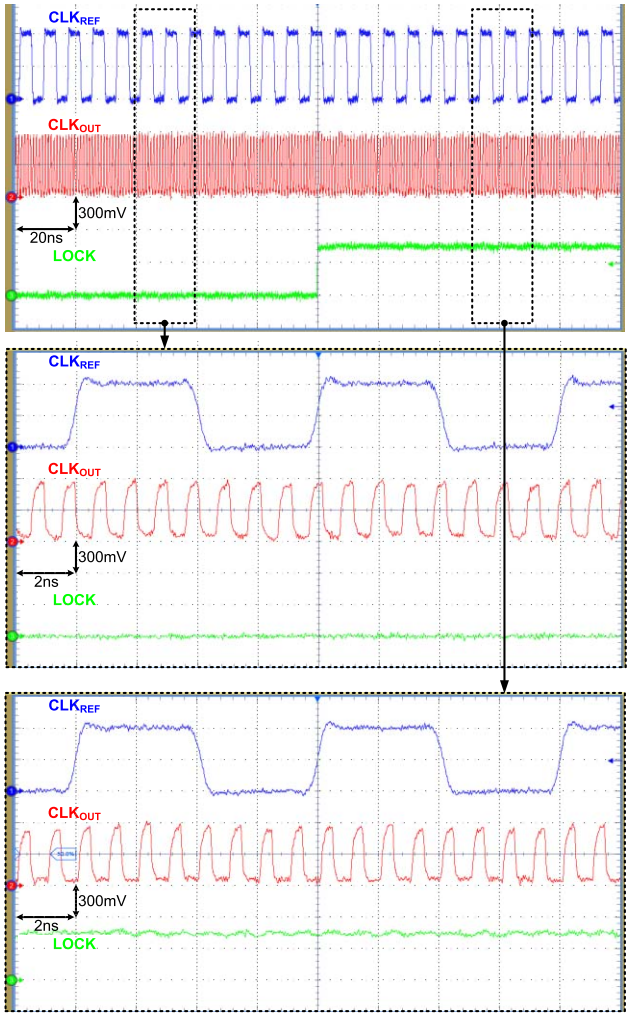

Fig. 13. Voltage waveforms measured during the initial locking transient of the programmed digital PLL.

123 282 μm^2 for 16 TCABs, 38 783 μm^2 for 42 CBs, and 33 058 μm^2 for 27 SBs), the CLB array occupies 0.523 mm^2 (including 15 288 μm^2 for 100 CLBs, 18 107 μm^2 for 110 CBs, and 61 710 μm^2 for 121 SBs), and the ALU array occupies 0.454 mm^2 (including 174 504 μm^2 for 20 ALUs, 63 292 μm^2 for 30 CBs, and 32 696 μm^2 for 30 SBs). The IC also includes a gate driver and on-chip power transistors, as dedicated blocks. The versatile programmability of CHIMERA is demonstrated by configuring the IC to three

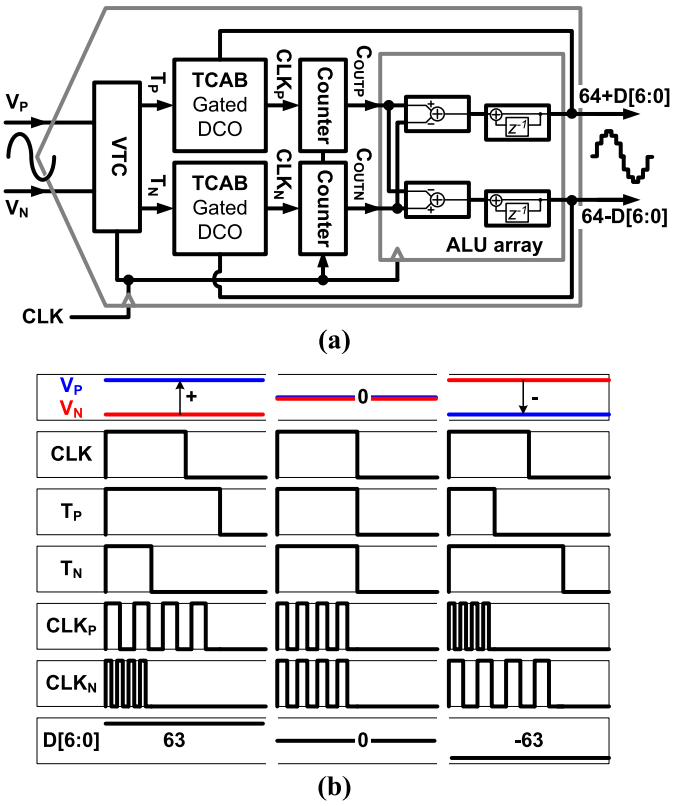

Fig. 14. (a) CHIMERA configuration as a 50-MS/s ADC. (b) Conceptual timing diagram of the ADC.

representative mixed-signal systems—a PLL, an ADC, and a dc–dc converter—and measuring the resulting characteristics.

When prototyping a system on a programmable device, software tools supporting system level description to generation of programming bit code are required. For CHIMERA, the process is partially implemented for the CLB array as described in Section IV-A. The considerations in [5], [6], and [8] would be the good start points when developing the software interface automating the rest procedures for CHIMERA (e.g., mapping of analog blocks to TCABs, decision of routing path of the input/output of the TCABs by turning on/off of the tri-state inverters).

The details on the configuration and measurement results of the three mixed-signal systems are presented in the following sections. In addition, the discussion on other mixed-signal system examples and useful cases of CHIMERA is also presented.

A. Digital Phase-Locked Loop

Fig. 10 illustrates the block diagram of a 1-GHz digital PLL with an 8× multiplication; Fig. 11 shows how this PLL can be programmed on CHIMERA. First, the PFD converts the timing error between the input reference clock and the feedback clock into two pulse widths. To quantize the two pulse widths, two TDCs are configured, as described in Section III-B. The ensuing digital loop filter consisting of proportional and integral paths [26] is mapped to ALUs, to compensate the timing error. A DCO is then implemented with a single TCAB, as described in Fig. 4(b). The GCLK block is also used, for

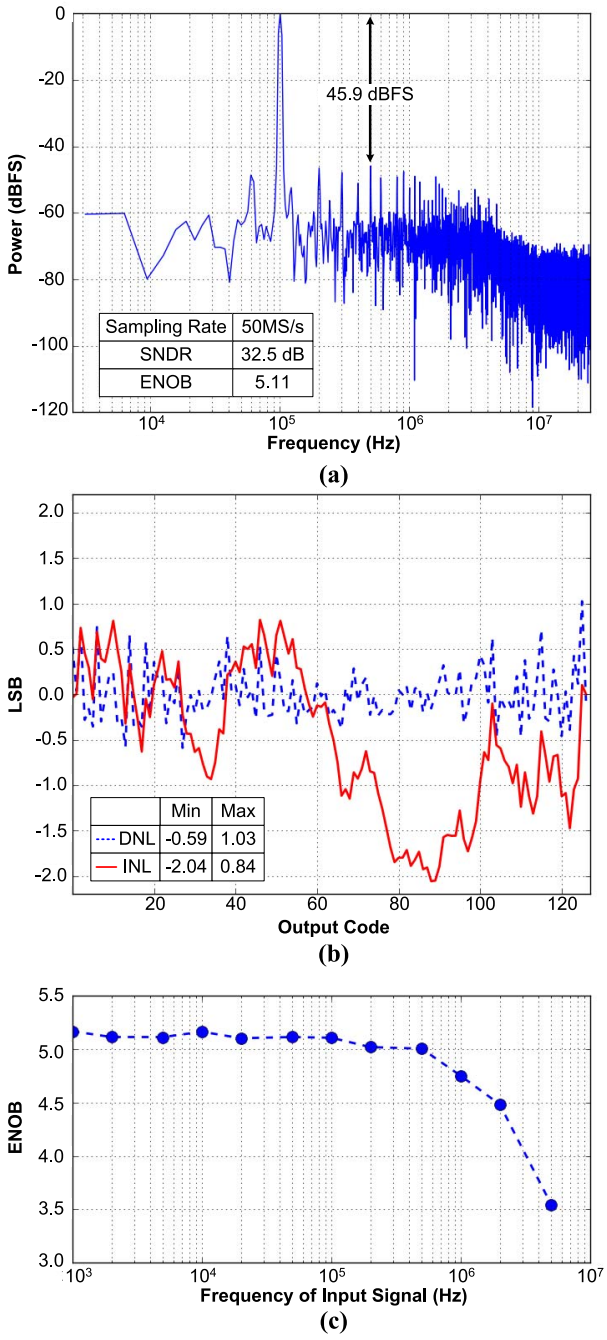

Fig. 15. Measured (a) dynamic performance, (b) static performance of the programmed ADC, and (c) ENOB versus input signal frequency.

dividing the DCO clock and distributing the divided clock. The lock detector logic, which indicates whether the PLL is in lock-condition, is programmed into ALUs and CLBs.

The programmed PLL successfully synthesizes a 1-GHz clock from a 125-MHz reference clock input. The TCAB programmed as DCO operates within the 0.98 to 1.08 GHz frequency range, with an average resolution of 0.78 MHz/bit. The phase noise characteristics of the PLL were measured, and are shown in Fig. 12. Its measured integrated jitter is 12.3 ps_{rms}, and the phase noise is −102.91 dBc/Hz at a 10-MHz offset. The power consumption is 33.6 mW. The CLK_{REF}, CLK_{OUT}, and $LOCK$ waveforms measured during the initial locking transient are shown in Fig. 13.

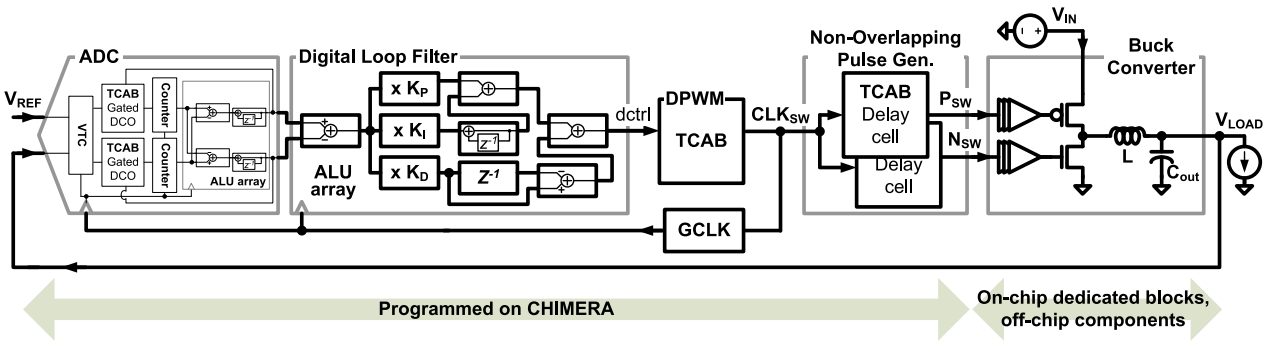

Fig. 16. CHIMERA configuration as a dc–dc converter.

B. Analog-to-Digital Converter

Fig. 14(a) illustrates the block diagram of a 7-bit, 50-MS/s ADC programmed on CHIMERA. The architecture and operation of the programmed ADC are as follows. First, the VTC converts $V_P - V_N$ (ΔV) into two pulses, T_P and T_N, with on-times ($T_{on,P}$ and $T_{on,N}$, respectively) given by (9). Then, the pulse widths of both pulses are quantized by the subsequent TDCs, each of which consists of a TCAB programmed as a gated oscillator and a counter. Each TCAB oscillates only when the received pulse T_P or T_N is high, and its oscillating period, $T_{period,P}$ or $T_{period,N}$, is controlled by adjusting the capacitance in the TCAB via the received digital code, $64 + D[6:0]$ or $64 - D[6:0]$. The feedback controller programmed onto the ALU array compares the two counter outputs—C_{OUTP} and C_{OUTN} which are proportional to $T_{on,P}/T_{period,P}$ and $T_{on,N}/T_{period,N}$, respectively—and adjusts the capacitances in the TCABs until the counter outputs are equal. If it is assumed that t_{xing}, t_{logic}, and t_{reset} in the TCAB and VTC are relatively small, the conditions to satisfy that equality are

$$\begin{aligned}\frac{T_{on,P}}{T_{period,P}} &= \frac{T_{on,N}}{T_{period,N}} \\ \frac{\frac{CV_{th}}{I_0+I_S-g_m\Delta V}}{\frac{(C_0+(64+D)C_{step})V_{th}}{I_{1A}}} &= \frac{\frac{CV_{th}}{I_0+I_S+g_m\Delta V}}{\frac{(C_0+(64-D)C_{step})V_{th}}{I_{1A}}} \\ \frac{C_0+(64-D)C_{step}}{I_0+I_S-g_m\Delta V} &= \frac{C_0+(64+D)C_{step}}{I_0+I_S+g_m\Delta V}. \end{aligned} \tag{10}$$

Then, a solution to (10) is determined so that D is proportional to $V_P - V_N$. This principle is illustrated with the conceptual timing diagram in Fig. 14(b), including a relative pulse width or period difference.

Fig. 15(a) shows the measured dynamic performance of the programmed ADC at 50 MS/s, with a 100-kHz sinusoidal input. The programmed ADC achieves an SNDR of 32.5 dB and an ENOB of 5.11, while dissipating 10.8 mW. Fig. 15(b) also shows the static performance of the ADC. The measured INL and DNL are in the ranges of -2.04 to 0.84 and -0.59 to 1.03 LSB, respectively. Fig. 15(c) plots the measured ENOB sweeping the frequency of input signal. The programmed ADC exhibits degraded ENOB in higher frequency of input signal due to the feedback path, introducing finite bandwidth under sampling frequency.

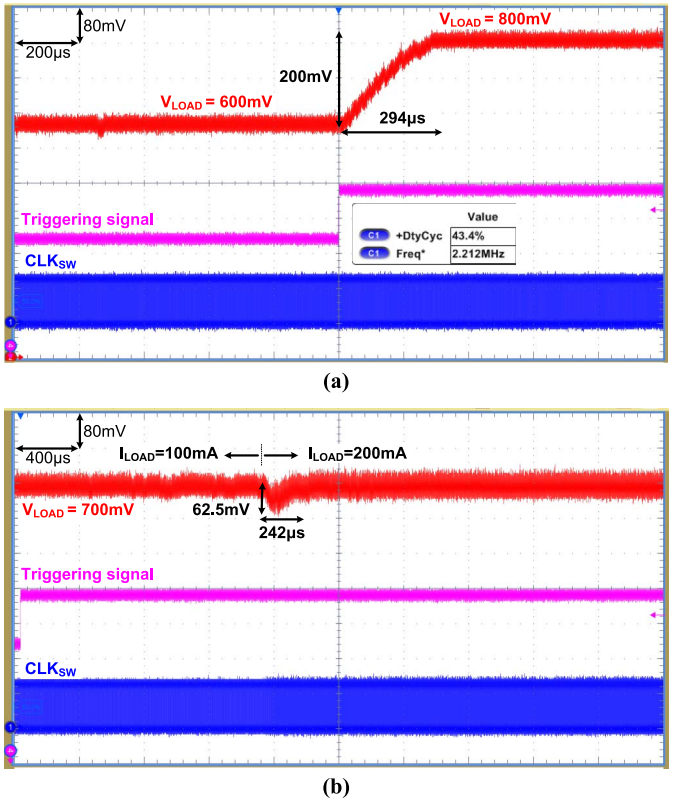

Fig. 17. Measured output voltage waveforms of the programmed dc–dc converter in (a) reference tracking (600 to 800 mV step transition with a 150-mA load current) and (b) load transient (100 to 200 mA step transition with a 700-mV output voltage).

Based on the measured results, the calculated FoM ($=$ power/$(2^{\text{ENOB}} \cdot f_{\text{sample}})$) is 6.25 pJ/conversion step. In [7] which presented the results of the programmed pipelined ADC, the reported FoM is 160 fJ/conversion step. The reported SNR and over-sampling frequency of the programmed $\Delta\Sigma$ ADC in [6] are 24.1 dB and 2.5 MHz, respectively. Meanwhile, the recent ADCs implemented in full custom fashion range in terms of the FoM from several tens to several hundreds of fJ/conversion step [27].

C. DC–DC Converter

Fig. 16 illustrates the configuration of CHIMERA as a dc–dc converter. The programmed dc–dc converter consists of the 7-bit ADC in Fig. 14(a), a digital PID compensator

TABLE I
COMPARISON OF CHIMERA WITH OTHER FIELD-PROGRAMMABLE DEVICES

	This work	[4] JSSC 03'	[3] ISSCC 08'	[5] JSSC 10'	[7] JSSC 11'	[6] TVLSI 13'	[8] TCAS-1 16'
Process	65 nm	N/A	130 nm	350 nm	65 nm	350 nm	65 nm
Type	Mixed-signal	Mixed-signal	Analog	Analog	Analog	Mixed-signal	Analog
Area	2.41 mm^2	N/A	1 mm^2	9 mm^2	0.31 mm^2	N/A	3.46 mm^2
Supply	1.2 V	3.3 V	1.2 V	2.4 V	1 V	2.4 V	1.2 V
The number of parameters	12,626	A few hundreds†	330	50,000	63	Tens of thousands†	35,408
Programmable analog function block	TCAB	X	X	X	X	X	X
Selectable analog block	TCAB	Tunable amplifer	Tunable G_m cell	Multiplier, transconductor, transistor, C	Zero crossing detector based configurable block	Multiplier, transconductor, transistor, C	Programmable transistor, R, C
The number of programmable elements	16 TCABs, 100 CLBs, 20 ALUs	32 CABs, 8 programmable digital blocks	55 tunable G_m cells	32 CABs	8 CABs	108 CABs, 108 CLBs	600 CABs
Programmable routing	O	△ (Limited)	X	△ (Limited)	X	△ (Limited)	△ (Limited)
Presented examples	PLL, ADC, DC-DC converter	A part of 300-baud modem	Analog filters	AM receiver, analog speech processor	Pipeline ADC, analog fiter	ADCs	bias circuits, analog filters

† denotes coarse estimation from the paper.

mapped to ALUs, a DPWM, and non-overlapping pulse generator implemented with the TCABs. To generate the non-overlapping pulses, two TCABs are configured as delay cells; their common input is CLK_{SW}, and the outputs are P_{SW} and N_{SW}, respectively. Each delay cell is configured with a fixed amount of delay, so that the rising delay for P_{SW} is shorter than that of N_{SW} and the falling delay of P_{SW} is longer than that of N_{SW}. The buck converter stage is composed of a gate driver and on-chip power transistors included as dedicated blocks within the fabricated IC, with an off-chip 3.3-μH inductor and 0.22-μF capacitor.

The measured reference tracking/load regulation waveforms are shown in Fig. 17. When V_{REF} has a step change from 600 to 800 mV, V_{LOAD} successfully tracks the step with a 294-μs settling time, supplying 150 mA to the load and switching at 2.2 MHz, as shown in Fig. 17(a). Fig. 17(b) demonstrates that the programmed feedback controller is also capable of regulating the load step transition (from 100 to 200 mA) in I_{LOAD}. The conversion efficiencies for different load conditions are presented in Fig. 18. While converting a 1.2-V input to a 0.7-V output and supplying 150 mA, the programmed dc–dc converter achieved a peak efficiency of 95.5%.

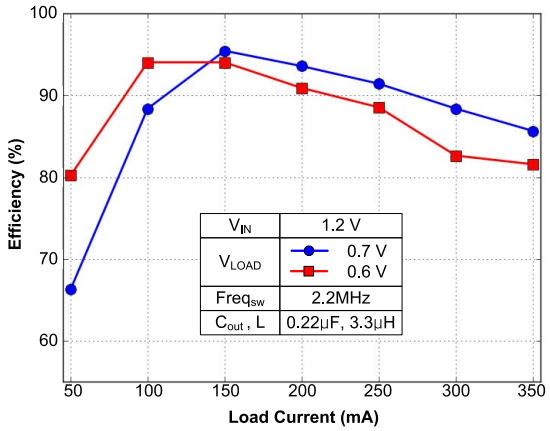

Fig. 18. Conversion efficiencies for different load conditions of the programmed dc–dc converter.

D. Other Possible Examples

In addition to the presented three representative systems above, CHIMERA is also capable of being programmed to other various mixed-signal systems. For example, digital delay-locked loops consisting of TDC, digital filter, and digitally controlled delay line can be programmed on CHIMERA. Further, CHIMERA is particularly useful when prototyping mixed-signal feedback systems adopting advanced digital filter techniques or digitally assisted analog systems with improved digital calibration and comparing their performance against to conventional ones by programming the both on CHIMERA. For example, in case of the digital PLLs, various digital filter implementations have been proposed to achieve optimum loop gain [28], fast locking or peaking-free jitter transfer function [17]. By programming the advanced PLLs on CHIMERA, their performance can be directly compared to the conventional PLL in Section V-A even without individual fabrication.

VI. CONCLUSION

This paper presented a field-programmable mixed-signal IC named CHIMERA, for low cost and rapid prototyping of mixed-signal systems. The proposed TCABs in CHIMERA

can be programmed to various analog circuits used in timing generation, data conversion, and power management ICs. CHIMERA also includes programmable digital blocks of CLBs and ALUs. Combining the TCABs, CLBs, and ALUs, the IC can be programmed to today's various mixed-signal systems. Table I presents a comparison of the proposed IC with previously published works. Unlikely most other works, which provide unit analog blocks with fixed functions, each TCAB is a truly reconfigurable block that can implement multiple analog functionalities via field-programming. Furthermore, CHIMERA can achieve high programmability of the signal propagation path, given that both the inputs and outputs to the TCABs are digital binary pulses. The prototype IC fabricated with 65-nm CMOS technology was programmed and operated as a 1-GHz PLL with a 12.3-ps_{rms} integrated jitter; as a 50-MS/s ADC with a 32.5-dB SNDR, and as a 1.2-to-0.7 V dc–dc converter with 95.5% efficiency. These results demonstrate both the successful operation of CHIMERA and its versatile programmability. In addition to the presented versatile programmability in this paper, there is room for improvement of CHIMERA in order to compete against the systems implemented in custom fashion in terms of performance. For example, the improvement in the linearity of the digitally-controlled capacitors or DACs in the TCABs to overcome the variation or mismatch during the fabrication would help achieve comparable performances.

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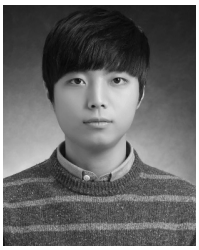

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