

Precision Passive-Charge-Sharing SAR ADC: Analysis, Design, and Measurement Results

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Abstract—This paper presents a passive-charge-sharing successive approximation register (SAR) analog-to-digital converter (ADC) that achieves 16-bit linearity. It is known that on-chip passive charge sharing suffers from poor linearity due to the unregulated reference voltage during bit trials. This paper gives a detailed analysis for the reasons of poor linearity for passive-charge-sharing SAR ADCs and proposes solutions. The proposed ADC architecture with one-reference-cap-per-bit and short switches addresses the issue of signal-dependent reference voltage droop during SAR ADC bit trials and orthogonalizes the bit weights. The calibration technique presented further calibrates the ADC to 16-bit linearity. In addition, the proposed architecture maximizes SNR by sampling on to the digital-to-analog converter (DAC) capacitor array, the first reported in this type of SAR ADC. This paper provides the foundation of building a precision SAR ADC out of on-chip reference capacitors. Measurement result from a prototype test chip shows ± 0.8 LSB (16-bit level) integrated non-linearity at 1 MSPS.

Index Terms—Active charge redistribution, ADC, passive charge sharing, reservoir capacitor, successive approximation register (SAR), system on chip.

I. INTRODUCTION

SUCCESSIVE approximation register (SAR) ADCs, having been in existence for many years, are known for their power efficiency, thereby making the architecture well suited to serve today's low-power system-on-chip applications. Recently, there has been a trend to push the speed of high-precision (>16 bits) SAR ADCs to beyond tens of mega samples per second (MSPS) [1], [2]. However, achieving precision and speed simultaneously is never a trivial task. The reference settling time is often a speed limiting factor. It is often limited by the package bond-wire *LC* resonance settling time, which does not scale down along with CMOS processing technology advancement. As CMOS technology scales down and the speed of SAR increases, reference settling limitation becomes even more significant.

Passive charge sharing has appeared in the recent literature as a way to achieve shorter reference settling time resulting in conversion speeds of 50 MSPS at 9 bits [3] by bypassing the bond-wire *LC* resonance. Another technique that achieves similar results is to integrate a large on-chip reference charge reservoir capacitor to achieve faster reference

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settling speeds [4]. Both of these approaches are suitable for only low-to-medium resolution SAR ADCs. For example, the latter technique suffers from a signal-dependent voltage droop across SAR bit trials, thereby preventing its use in precision converters beyond 16 bits.

In this paper, a new passive-charge-sharing SAR ADC architecture is proposed [5]. To demonstrate the performance, a 16-bit prototype SAR ADC test chip was fabricated in 55-nm technology. Since the speed advantage has already been explored in [3], [4], and [6], the primary focus of this paper has been to explore the viability of passive charge sharing in the precision domain. Measured results show ± 0.8 LSB integrated non-linearity (INL) at 16-bit level at 1 MSPS.

The remainder of this paper is organized as follows. Section II introduces the background of the passive-charge-sharing SAR and highlights some differences with traditional active charge-redistribution SAR. Section III presents the proposed ADC architecture and introduces how it operates. Section IV analyzes the fundamental principles of a charge-sharing SAR. Techniques unique to the proposed work that enable an improved linearity are discussed in Section V. Measurement results are included in Section VI.

II. BACKGROUND ON PASSIVE-CHARGE-SHARING SAR

SAR ADCs convert an analog input signal to digital code through the successive approximation of consecutive bit trials. Traditional charge-redistribution SAR converters rely on a precise reference voltage during bit trials, often from a large off-chip reference decoupling capacitor or from a high-speed buffer. During one SAR ADC conversion, the reference voltage is expected to settle at least N times (where N is the ADC resolution), and as a result the settling time typically consumes a large portion of conversion time. As the sample rate is increased beyond the MSPS rate, the reference settling is stressed and often limits the achievable linearity.

To address this speed bottleneck, a passive-charge-sharing SAR [3] pre-samples the reference voltage on chip and uses the pre-sampled reference charge to carry out the bit trials, as shown in Fig. 1. While seemingly similar, this architecture is fundamentally different from the traditional charge-redistribution SAR ADC. To discriminate, the traditional charge-redistribution SAR ADC is denoted as “*active charge redistribution*” and the charge-sharing SAR is denoted as “*passive-charge-sharing*” SAR [3]. The *active charge redistribution* uses a fixed voltage reference to supply any charge required to rebalance the sampled signal. The *passive charge sharing* uses pre-sampled reference charge to rebalance the sampled signal. One maintains a fixed voltage and supplies

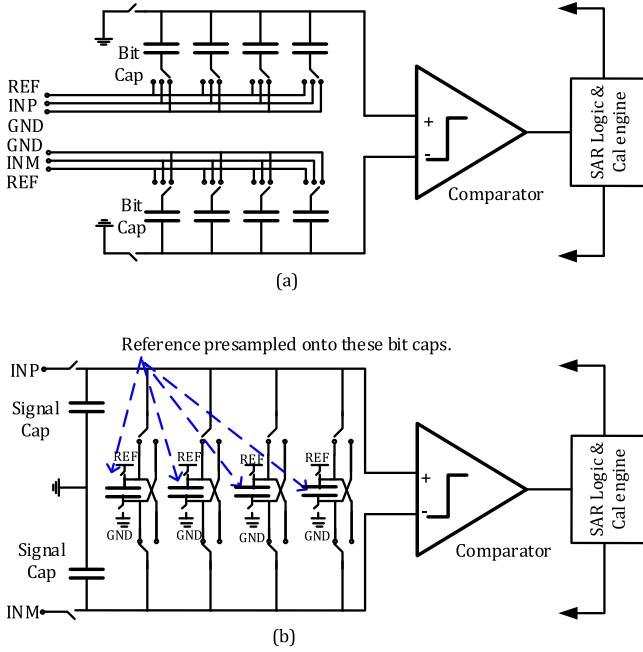


Fig. 1. Comparison of (a) charge-redistribution SAR and (b) passive-charge-sharing SAR. Passive-charge-sharing SAR pre-samples reference voltage on chip and uses this reference charge for bit trials.

variable charge, while the other begins with a fixed charge and needs to deal with a variable voltage. In short, this is a new type of SAR ADC.

The work in [3] has several drawbacks. The comparator input nodes are initialized to the input voltage and then converge to a common-mode voltage during the bit trials. Non-linear capacitance at the comparator input nodes will undergo a signal-dependent voltage change, leading to INL degradation, specifically at higher resolution. Second, the available reference charge is only limited to the charge stored on reference-sampling capacitors. Charge injection and clock feedthrough from the related reference-sampling switches will degrade the linearity. Third, the reference-sampling switch is difficult to design. The voltage on each side of the reference-sampling capacitor starts at V_{REF}/GND and settles to $V_{REF}/2$. Therefore, the related switches must remain ON through the full voltage range from V_{REF} to GND. This is very difficult to design in nanometer technologies using low supply voltages. Designing such a switch often requires the use of special low V_{th} devices, which increases cost, or a boosted gate voltage, which brings further design complexity and may negate its benefit.

Kapusta *et al.* [4] presented a similar idea of using “reservoir” capacitor. By pre-sampling the reference charge onto a large on-chip reservoir capacitor, more reference charge was available for the charge sharing. An alternative way of stating the benefit is that, because the reservoir capacitor can be relatively large, it is able to provide a relatively constant voltage. To achieve 14-bit linearity, Kapusta *et al.* [4] used a reservoir capacitor to SAR DAC capacitor ratio of $80\times$. This ratio is large and could represent a significant area penalty. Further, extending this approach to 16-bit linearity, the reservoir capacitor would need to be $320\times$ larger than

the SAR DAC capacitor. In this paper, we seek an alternative approach.

Before proposing our new structure, we would like to outline some key aspects of using “passive charge sharing.” While the idea of *passive charge sharing* seems appealing at first glance, a deeper analysis reveals some key drawbacks.

First, although this technique is claimed to work in the *charge* domain, the comparator, as the brain of the SAR ADC, still operates in the *voltage* domain. The pre-sampled reference, in the form of charge, is neither regulated nor replenished between successive bit trials. Therefore, the reference voltage is not constant. This fact presents a unique challenge, as explained later.

Second, in charge sharing: at the same time the reference charge is shared, the signal charge is also shared with the reference capacitor. This interchange of charge could easily degrade the pre-sampled reference charge and result in signal-dependent bit weights that are difficult to calibrate out. By using a large on-chip reservoir cap, this effect could be somewhat mitigated. However, for a precision SAR ADC, this might call for an unreasonably large on-chip reservoir capacitor, as discussed earlier.

Moreover, signal-dependent charge injection suddenly becomes a new challenge. This is because the usual assumption that the injected charge would be absorbed by a voltage reference is no longer valid, as we lack a regulated voltage reference during conversion. The signal-dependent charge injection may degrade the reference charge integrity, introducing nonlinearity.

To summarize, the absence of an active element that regulates the reference voltage makes it difficult to achieve a precision ADC with passive charge sharing. We will address all these potential issues in Section III–V.

III. PROPOSED ADC ARCHITECTURE

Fig. 2 shows the proposed ADC architecture. Fig. 2(a) shows a unit cell, where the notations of bottom plate nodes, top plate nodes, bit capacitor, reference capacitor, short switch, and “pre-charge” switch are labeled. The reference capacitor is sometimes also called reference reservoir capacitor or reservoir capacitor. Only four bits are shown in Fig. 2(b), but there are 16 bits. Fig. 3 shows a typical operation procedure for each bit illustrating the operation of the ADC.

Step 1: Signal Acquisition Phase: The signal is sampled onto the bit capacitors; at the same time, the reference voltage is sampled to the reference capacitors, as shown in Fig. 3(a). After this step, the input sampling switches and the reference-sampling switches will be opened.

Step 2: Beginning of the Conversion: A set of short switches [7] short the bottom plate nodes of every sampling capacitor together (bottom plate is the side of the capacitor connected to input during acquisition), as shown in Fig. 3(b). The differential signal voltage then shows up on the top plate nodes which are connected to the comparator.

Step 3: First Bit Decision: The comparator makes a decision for the first bit. Then the short switch in the first bit is opened and the first reference capacitor is inserted into the capacitor array *right side up* or *upside down* depending on the

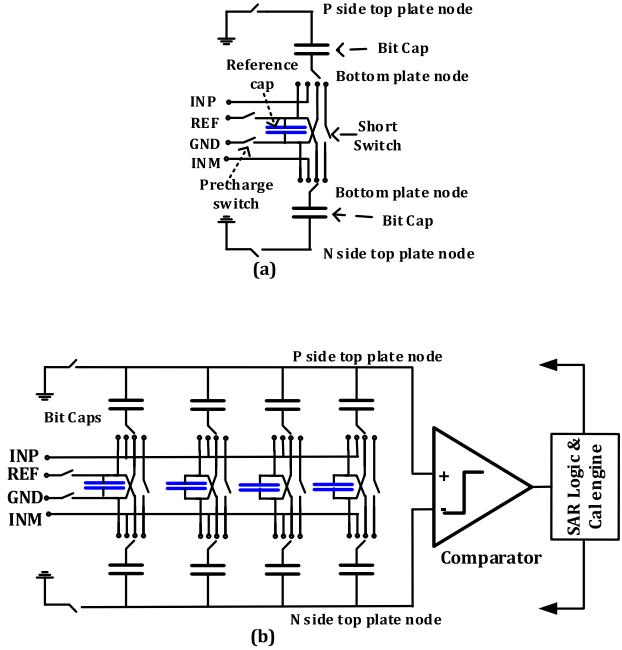


Fig. 2. (a) Unit cell. (b) Proposed ADC diagram.

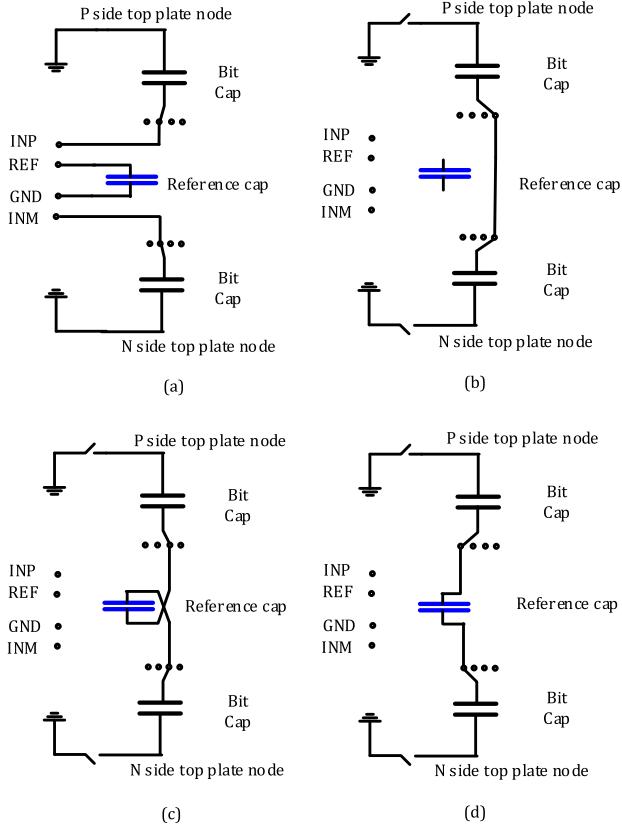


Fig. 3. Switch connection in different phases. (a) Acquisition. (b) Shorting bottom plates. Bit set to (c) Low and (d) Hi.

comparator decision, as shown in Fig. 3(c) or (d). Then, the first bit reference is going through a settling process. Since the reference is on chip, this settling process is only limited by the switch and bit capacitor RC time constant. Please note that at this time, all the short switches except for the first bit remain closed.

Step 4: Second Bit and All Remaining Bits: After the reference charge from bit 1 reference capacitor settles, the comparator makes the second bit decision. Then it opens the second short switch and inserts the second reference capacitor. After the second bit settles, a third bit is decided by the comparator and inserted and so on.

Compared to [3] in which the unit capacitor C_u serves as both the bit capacitor and the reference capacitor, this architecture separates the bit capacitor and the reference capacitor as C_u and C_{ref} . This enables the use of a larger reference capacitor to desensitize the effect of parasitic capacitances. Although this is similar to what appeared in [4], there are two key differences: 1) the introduction of a *short switch* for all bits which keeps all the bottom plates shorted and the reference capacitor untouched until applying of any particular bit decision and 2) each reference capacitor C_{ref} is associated with only one bit which removes the coupling between different bits. These differences are crucial to achieve 16-bit linearity and beyond. These steps will help to orthogonalize the bit weight from an entangled state, making a precision SAR ADC that is using passive charge sharing possible, which is to be explained in detail in Section V. Furthermore, this architecture also makes it possible to sample the input signal onto the bit capacitor C_u , removing the need for a separate signal sampling capacitor as done in [3] and [4]. Due to the reduced amount of sampled KT/C noise and the increased signal amplitude at comparator input which reduces the comparator referred-to-input noise, this improves the SNR by almost 6 dB, which is important for precision ADCs. The benefits from this architecture will be detailed in the next session on passive-charge-sharing techniques.

IV. FUNDAMENTALS BEHIND PASSIVE CHARGE SHARING

To achieve 16-bit linearity and beyond, a detailed analysis on passive-charge-sharing SAR ADC is required. As some of our conclusions later on may seem anti-intuitive, this section attempts to review and highlight some fundamentals behind passive charge sharing, while leaving technique specific discussion to Section V. We briefly talked about the differences of a charge-sharing SAR with a traditional SAR ADC back in Section II. In this section, we are going to highlight the difference in two aspects: the charge domain versus voltage domain, and the path dependence of charge sharing. Then we make a comparison of the one-reference-cap-per-bit versus a shared reservoir capacitor [4].

A. Charge Domain Versus Voltage Domain

In a traditional SAR ADC, there is a strict charge domain to voltage-domain mapping. Considering the ideal case where all capacitors are linear ideal capacitors, there is a linear relationship between reference voltage and the reference charge. While most real implementations would be fully differential due to various benefits, here for simplification, let us consider a single-ended N -bit traditional charge rebalance SAR ADC as in Fig. 4.

At the beginning of the conversion, all the signal charge is sampled on to the N -bit capacitor C_n where n ranges

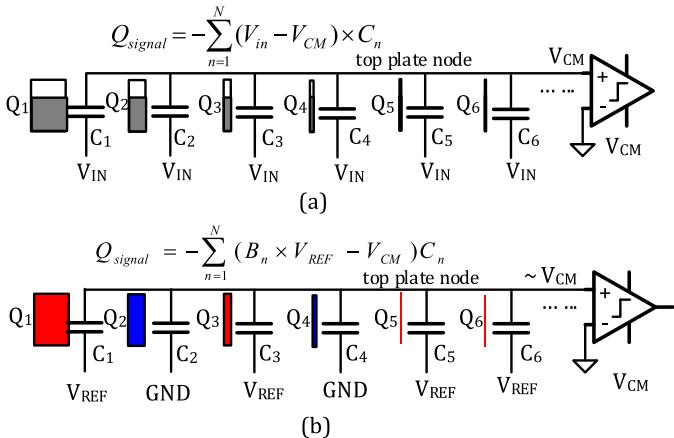


Fig. 4. Visualizing a charge-redistribution SAR ADC in charge domain.
 (a) Signal charge is acquired on the top plate node. (b) Signal charge is balanced by reference charge at the end of a conversion.

from 1 to N . We have

$$Q_{\text{signal}} = - \sum_{n=1}^N (V_{\text{in}} - V_{\text{CM}}) \times C_n \quad (1)$$

where V_{in} is the input voltage, V_{CM} is the common-mode voltage on which the top plates of the bit capacitors are sampling against, and Q_{signal} is the signal charge that get acquired on the top plate nodes during sampling.

At the end of the conversion, the reference charge balances out the signal charge in the following way:

$$Q_{\text{signal}} = - \sum_{n=1}^N (B_n V_{\text{REF}} - V_{\text{CM}}) \times C_n \quad (2)$$

where V_{CM} and C_n are the same as in (1), B_n is the bit decision for bit n , which could be 0 or 1, and V_{REF} is the reference voltage.

Fig. 4 shows a visualization of this process. In Fig. 4(a), the signal charge is acquired onto the top plates. In Fig. 4(b), the signal charge is decomposed into the combination of binary-weighted reference charge after the SAR conversion. The signal charge is effectively “redistributed” across different bit capacitors in a binary way. That is why it is called “charge-redistribution” SAR. This has often been the intuitive image for experienced SAR designers. A direct derivative from this would be that each bit’s weight is proportional to its capacitance value.

However, the comparator, which makes all bit decisions, does not work in charge domain. The comparator makes decision based on the voltage difference at its input terminals. A more detailed look at what happens is as follows: at the beginning of the conversion, the comparator sees a voltage difference:

$$V_{\text{comp}} = \frac{Q_{\text{signal}}}{\sum_{n=1}^N C_n} = V_{\text{CM}} - V_{\text{in}}. \quad (3)$$

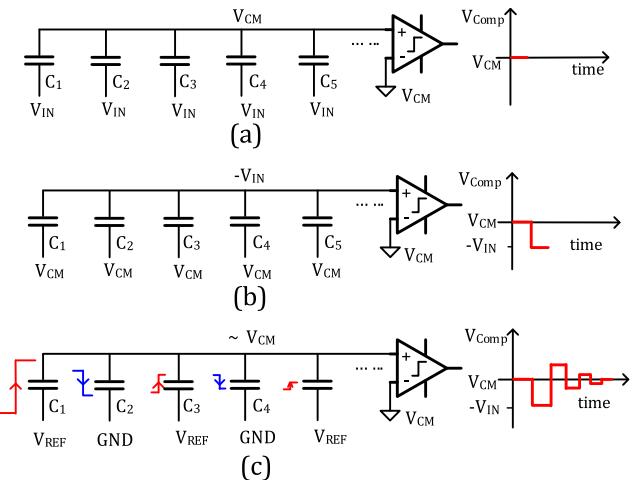


Fig. 5. Visualizing the traditional SAR ADC operation in voltage domain.
 (a) Signal acquisition phase. (b) Preparing for 1st-bit decision. (c) End of conversion.

After each bit decision, a binary-weighted voltage step $V_n = (B_n \times V_{\text{REF}} - V_{\text{CM}})(C_n / \sum_{k=1}^N C_k)$ at the comparator input nodes is applied. At the end of the conversion, the comparator input voltage difference converges to zero

$$V_{\text{comp}} = \frac{Q_{\text{signal}}}{\sum_{k=1}^N C_k} + \sum_{n=1}^N V_n \\ = \frac{Q_{\text{signal}}}{\sum_{k=1}^N C_k} + \sum_{n=1}^N \frac{(B_n \times V_{\text{REF}} - V_{\text{CM}})C_n}{\sum_{k=1}^N C_k} \equiv 0. \quad (4)$$

This process is visualized in Fig. 5. Equation (4) describes what actually governs the ADC operation. Equation (2) is only a derivative from (4) for a traditional charge-redistribution SAR. This derivation depends on a fact that (4) has a denominator, $\sum_{k=1}^N C_k$, which is common to all bits. Multiplying this denominator to both sides of (4) will lead to charge-domain expression (2).

We have recognized (4) instead of (2) as the equation which governs the ADC operation. Now let us try to reproduce (4) for the case of proposed passive-charge-sharing ADC. At the beginning of each conversion

$$V_{\text{comp}} = \frac{Q_{\text{signal}}}{\sum_{n=1}^N C_n} = V_{\text{CM}} - V_{\text{in}}. \quad (5)$$

This is the same as (3). Then after each bit decision, a reference capacitor is inserted, resulting in a voltage step V_n at comparator input, which can be expressed in (6), as shown at the bottom of this page. In (6), $C_{n\text{REF}}$ denotes the reference capacitor associated with bit n , B_n denotes the n^{th} bit decision, C_k denotes the bit capacitor of bit k , and C'_k denotes the serial connected bit capacitor C_k and the reference capacitor $C_{k\text{REF}}$.

$$V_n = (B_n V_{\text{REF}} - V_{\text{CM}}) \times \frac{C_{n\text{REF}} \left(\sum_{k=n+1}^N C_k + \sum_{k=1}^{n-1} C'_k \right)}{C_{n\text{REF}} \left(\sum_{k=n+1}^N C_k + \sum_{k=1}^{n-1} C'_k \right) + C_{n\text{REF}} C_n + C_n \left(\sum_{k=n+1}^N C_k + \sum_{k=1}^{n-1} C'_k \right)} \\ = (B_n V_{\text{REF}} - V_{\text{CM}}) \times f(C_1 \text{ to } N, C_{\text{REF},1 \text{ to } n}, n) \quad (6)$$

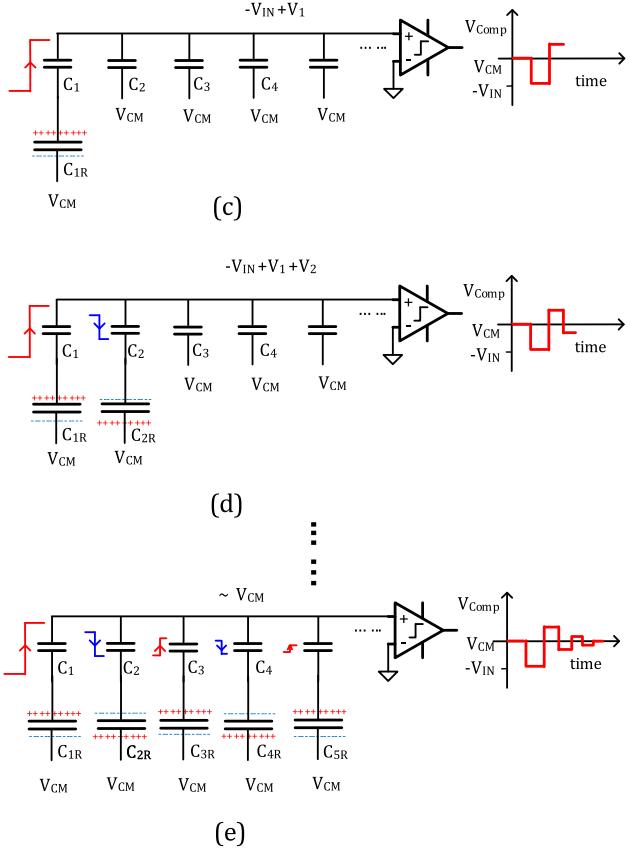


Fig. 6. Visualizing the charge-sharing SAR ADC operation in voltage domain. (a) Signal acquisition phase. (b) Preparing for first-bit decision. (c) Applying first-bit decision. (d) Applying second-bit decision. (e) End of conversion.

where $C'_k = (C_k C_{k\text{REF}} / C_k + C_{k\text{REF}})$. Equation (6) is a little tedious. In real design, the calculation can be done by a MATLAB script or any programming language.

At the end of the conversion, we have

$$V_{comp} = \frac{Q_{\text{signal}}}{\sum_{n=1}^N C_n} + \sum_{i=1}^N (B_n V_{\text{REF}} - V_{CM}) \times f(C_1 \text{ to } N, C_{\text{REF1 to } n}, n) \equiv 0. \quad (7)$$

Such a process is visualized in Fig. 6.

An interesting finding to point out here is, from (5) or (7), we can no longer derive an equation similar to (2), because the function $f(C_1 \text{ to } N, C_{\text{REF1 to } n}, n)$ is such a complex function that we can no longer find a common denominator as in (4). For this case, there is not a straightforward mapping between the voltage domain and the charge domain. It is usual for SAR designers to intuitively think in charge domain. For the proposed passive-charge-sharing SAR ADC, the voltage domain is easier to work with than the charge domain going forward.

We recognize (6) and (7) as the equations that describe the circuit behavior for the proposed passive-charge-sharing SAR ADC. Although (6) and (7) are complex and tedious, they are still linear equations as long as the all the capacitors involved are linear capacitors. With a proper design, we can still expect an SAR ADC with high linearity. Although not straightforward and non-intuitive, the bit weights can be

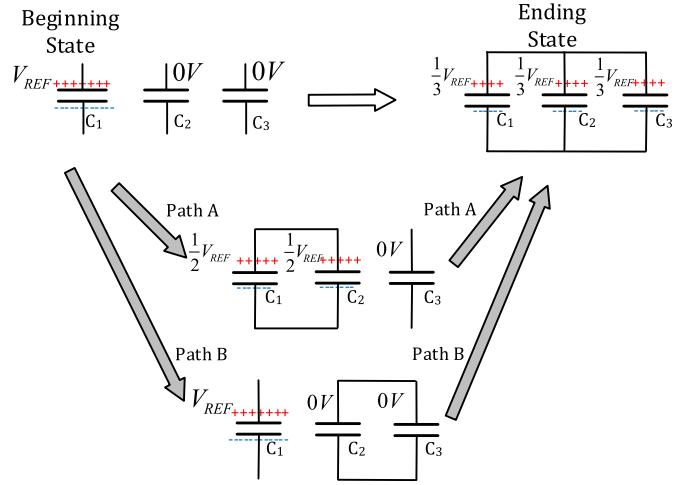


Fig. 7. No path dependence for parallel-connected capacitor array.

predicted accurately from the calculated voltage steps described in (6).

B. Charge-Sharing Path Dependence

In a charge-sharing SAR ADC, another interesting behavior is the path dependence. Here we consider two simplified cases: the first case is for parallel connected capacitors, where such a path dependence is not observed; the second case is with serial connected capacitors, where a path dependence is clearly observed.

In Fig. 7, a capacitor, pre-charged to V_{REF} , is going to share its charge with two other capacitors. We assume all capacitors in this example have the same capacitance. It could possibly go through two different paths as shown in path A and path B. A simple calculation would show that both paths result in same final voltage, $V_{\text{REF}}/3$, which is as expected.

In Fig. 8, the situation is a little different. A capacitor C_1 charged with V_{REF} is going to share its charge with two other capacitors C_2 and C_3 of the same capacitance value. In path A, it first shares its charge with C_2 and then C_3 is inserted in between. The resulting voltage across each capacitor would be $V_{\text{REF}}/2$ for C_1 , $V_{\text{REF}}/2$ for C_2 , 0 for C_3 . In path B, the two zero-charged capacitors C_2/C_3 are connected first. Then the charged capacitor C_1 is going to share its charge with these two serial-connected capacitors. The resulting voltage for these three capacitors would be $(2/3)V_{\text{REF}}$ for C_1 , $(1/3)V_{\text{REF}}$ for C_2 and $(1/3)V_{\text{REF}}$ for C_3 . The two paths started from exactly the same conditions and ended in the exactly the same capacitor array topology. However, the two different paths result in two completely different set of ending voltages.

With the proposed charge-sharing ADC, at the beginning of the conversion, all bit capacitors are connected in the configuration as in Fig. 3(b). At the end of the conversion, they are either connected as in Fig. 3(c) or (d), which are of the same capacitor array topology. However, as we have seen from the above examples, how the capacitor array topology evolves along the whole conversion cycle would be of interest to us. An interesting property discussed in Section V serves as the best example of this path dependence. This is not an issue for the traditional charge-redistribution SAR.

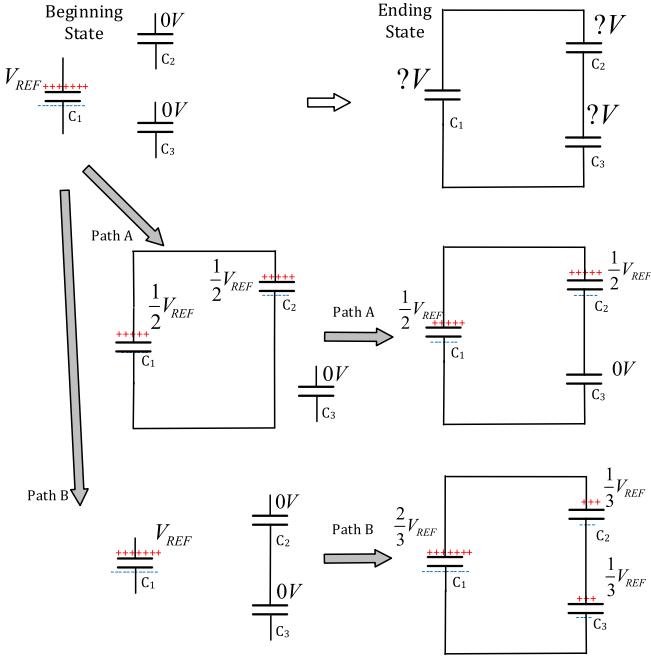


Fig. 8. Path dependence observed for serial-connected capacitor array.

C. One-Reference-Cap-Per-Bit Versus a Shared Reservoir Capacitor

In this paper, the one-reference-cap-per-bit was proposed and first implemented to help orthogonalize the bit weights. We argued one-reference-cap-per-bit is superior to shared reservoir capacitor without proof. For a shared reference reservoir capacitor, as the bit weight is signal dependent, equations representing the bit weights are not only tedious but also irrelevant to this paper. To retain the readability of this paper and also show why the one-reference-cap-per-bit is superior to a shared reservoir cap, the authors are presenting an intuitive comparison of the “capacitor array topology” in these two cases.

To make it simple, let us consider a special converter with only four bits using a shared reservoir capacitor, as shown in Fig. 9. For easy calculation, in this special converter, to illustrate the underlying principle, we assume every bit capacitor is exactly the same with a capacitance C . The shared reservoir capacitor has a value of $32C$.

Fig. 9(a) shows a case when at the end of a conversion for a full-scale signal, the ADC converges to a result of 1111. All the bit capacitors from the P side are connected to the positive terminal of the reservoir capacitors; all the bit capacitors from N side are connected to the negative terminal of the reservoir capacitors. The effective capacitance between the node $topp$ to the node $topn$ can be calculated to be $32/17C \approx 1.88C$.

Fig. 9(b) shows a case where at the end of the conversion for a mid-scale signal, the ADC converges to a result of 1001. Bits A and D are connected as P side/positive and N side/negative with Bits B and C as the opposite. To calculate the effective capacitance between $topp$ and $topn$ nodes, the capacitor array is re-arranged and re-drawn on the right. It can be easily seen or calculated that the effective capacitance between

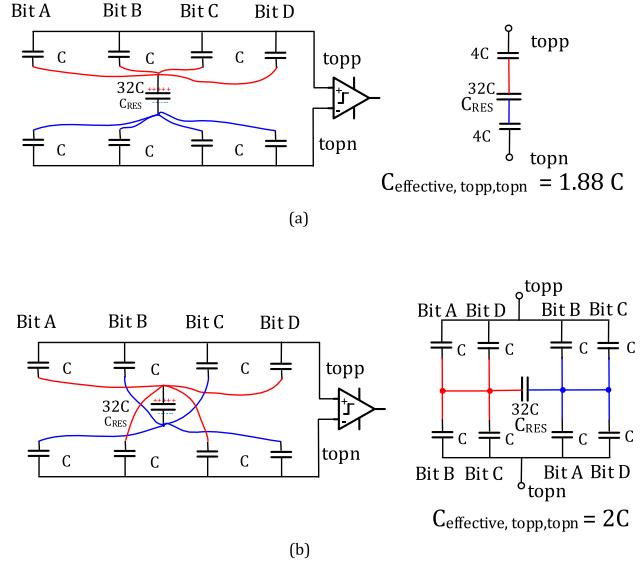


Fig. 9. Example of SAR ADC using shared reservoir capacitor. (a) End of conversion when input is at full scale and output code is 1111. (b) End of conversion when input is at midscale and output code is 1001.

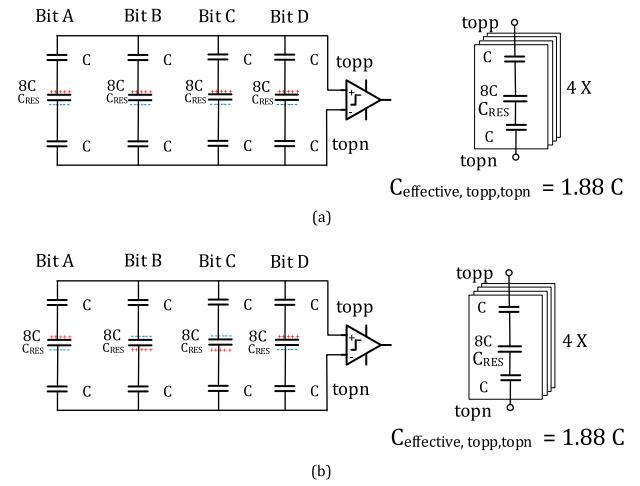


Fig. 10. Example of SAR ADC using one-reference-capacitor-per-bit. (a) End of conversion when input is at full scale and output code is 1111. (b) End of conversion when input is at midscale and output code is 1001.

$topp$ and $topn$ is $2C$. Note that this is inherently different to Fig. 9(a).

In these two cases, only the input signal is different: one is at full scale, and the other is at midscale. The difference in signal results in a different capacitor array topology at the end of the conversion. Since the passive-charge-sharing process depends on the capacitor array topology, the signal-dependent capacitor topology using a shared reservoir capacitor will make the bit weights signal dependent, which is undesired.

Fig. 10 shows an ADC with one-reference-cap-per-bit. In both Fig. 10(a) and (b), although the input signal is different, at the end of conversion, the effective capacitance between $topp$ and $topn$ nodes is exactly the same as $\sim 1.88C$. The change of capacitor array topology with a dedicated reference capacitor per bit is signal independent.

The one-reference-cap-per-bit solves the issue of signal-dependent capacitor array topology change and is therefore superior to a shared reservoir capacitor.

V. TECHNIQUES ON PASSIVE CHARGE SHARING

In this section, we will summarize several key techniques to achieve high linearity.

A. Decoupling Signal Charge From Reference Charge

As charge sharing is a passive process, the reference charge simply cannot be replenished between bit trials. If there is any signal charge that couples with the reference charge, it could seriously degrade the performance. The key to high linearity is to decouple the signal charge from the reference charge. To be more specific, for a given bit, the reference charge associated with this bit needs to remain untouched from the signal charge *before* and *at the time* of applying this particular bit decision. *After* applying the bit decision, it does not matter, however, how lower bits affect this bit's reference charge because the bit decision has been made. The *before*, *at the time*, and *after* terms will be used for discussion several times later on. To decouple signal charge from reference charge, the following will need to be done.

1) *Use of vcm-Based Switching (Decide and Set)*: The traditional SAR uses a test-and-toss algorithm: it carries out bit trials by setting a bit to high (1) and then decides whether to keep this bit high (1) or set it back to low (0) based on a comparator output. However, for a passive-charge-sharing SAR, once the reference charge is shared from the pre-sampled reference, there is no way to take it back accurately. This test-and-toss action degrades the reference charge “*before*” applying that particular bit trial result. The *vcm*-based switching algorithm [7], [9], herein referred to as decide and set, does not involve the test-and-toss of bits so it is a good fit for passive-charge-sharing ADCs. Our technique is similar to [9]: an explicit *vcm* voltage is not needed, as shown in Section V-A2. It, therefore, also saves a *vcm* buffer.

2) *Shorting Action*: For a given bit, before its bit decision, the bottom plates of the bit capacitors are kept shorted by a short switch. As a result, *at the time* the reference capacitor for any particular bit is inserted, the two bottom plates are always at exactly the same voltage ($\sim vcm$) so the reference capacitor does not see any signal charge, as shown in Fig. 11. This is a very crucial step to get to 16-bit linearity. This shorting action helps decouple the reference charge from the signal charge.

3) *Removing the Coupling From Previous Bit Decisions*: If the reference capacitors are shared between multiple bits, previous bit decisions will be remembered on the reference capacitors. Since bit decisions are always signal dependent, this will cause the lower bits to have signal-dependent bit weight. This should be avoided and every bit should have its dedicated reference capacitors. Having a dedicated reference capacitor per bit further decouples the signal charge from the reference charge *before* applying the reference charge.

B. Sequence-Dependent Bit Weight

Now that most signal-dependent bit weight has been taken care of, then the bit weight shows another very interesting

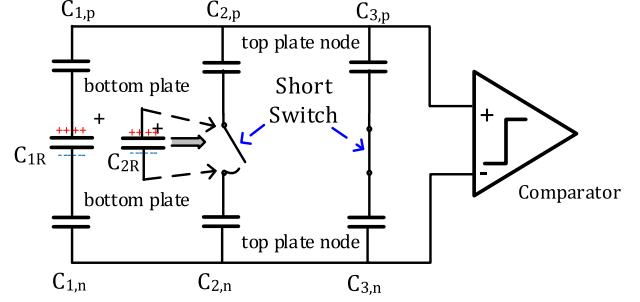


Fig. 11. Before connecting reference capacitor to the bit cap, the short switch keeps the two bottom plates nodes shorted; when inserted, the reference capacitor only see a common-mode signal, thus it remains untouched from the signal charge.

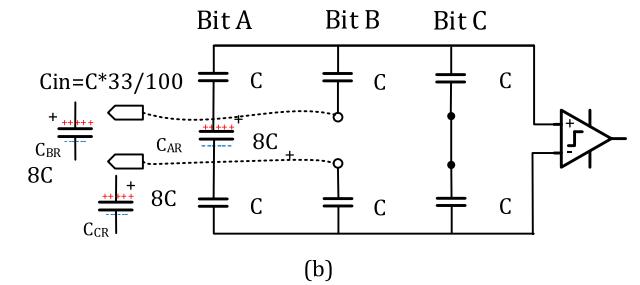
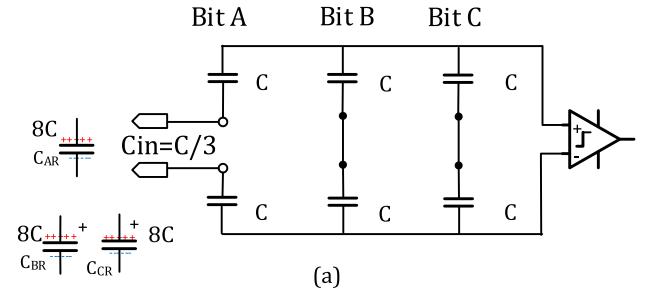


Fig. 12. When Bit A applies, it is connected to an effective capacitance $C/3$; when Bit B applies, it sees an effective capacitor $0.33C$.

property: even if two bits have exactly the same capacitor sizes their bit weights are slightly different from each other. The peculiarity is observed and confirmed in simulation with ideal components. This puzzling result unfolds a very interesting underlying property: as this ADC goes through these bit trials, the capacitor array topology changes; this system is no longer a linear time-invariant system but a linear time-variant system; although with the same bit capacitor and reference capacitor, the voltage steps at the comparator input nodes created by applying the reference charge are different.

Without loss of generality, let us consider an example with only three bits, as shown in Fig. 12. In this special converter, to illustrate the underlying principle, we assume every bit capacitor is exactly the same and each reference capacitor is $8 \times$ the size of the bit cap. Using basic charge-sharing principal, we can calculate the voltage step at the comparator input due to applying a bit “A” reference capacitor is

$$\Delta V_A = V_{\text{ref}} \frac{8C}{8C + C/3} \frac{\frac{1}{2}C}{\frac{1}{2}C + 1C} = \frac{8}{25} V_{\text{ref}} = 0.32 V_{\text{ref}}$$

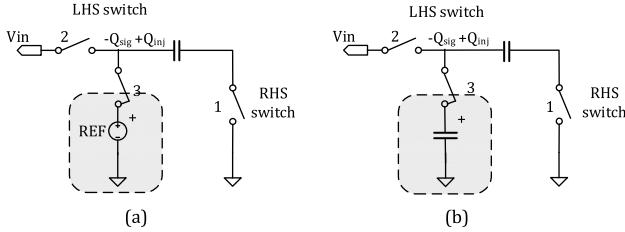


Fig. 13. Charge injection with bottom plates driven by a (a) voltage source and (b) reference cap.

The voltage step at the comparator input due to then applying a Bit B reference capacitor is calculated to be

$$\begin{aligned}\Delta V_B &= V_{\text{ref}} \frac{8C}{8C + \frac{33}{100}C} \frac{\frac{1}{2}C}{(\frac{1}{2}C + \frac{33}{34}C)} \\ &= \frac{273}{833} V_{\text{ref}} \approx 0.3277 V_{\text{ref}}.\end{aligned}$$

The voltage steps of these two bits are inherently different from each other. This should not be a big surprise after a detailed explanation in Section IV. This simple example illustrates a very interesting behavior: sequence dependence. This is a non-radix-2 ADC. The radix is less than 2 and is slightly different for each bit. The non-radix-2 bit weights are taken care of by calibration. The authors need to point out that because the radix is less than 2, some redundant bits are needed. Also it is worth mentioning that sequence dependence is different from signal dependence.

C. Signal-Dependent Charge Injection

In a traditional SAR ADC, a typical sampling circuit as shown in Fig. 13(a): at the end of signal acquisition, the normal practice is to open the right-hand-side (RHS) switch a little earlier than the left-hand-side (LHS) switch [8]. By doing this, the RHS switch charge injection is sampled onto the capacitor. This charge injection is signal independent, causing a signal independent offset at most. On the left-hand side, when the LHS switch is turned off, it will introduce a signal-dependent charge onto the bottom plate nodes. It is generally accepted that since this charge is only at the bottom plate nodes (the parasitic capacitor/junction capacitors) but not across the sampling capacitor, this is okay. We expect this charge will be absorbed by the near ideal driving voltage reference.

Due to the use of passive charge sharing, suddenly the previous assumption collapses as there is no ideal voltage reference involved, as shown in Fig. 13(b). We have to admit the injected charge, which is unfortunately signal dependent, is going to be mixed with the passive reference charge and degrade the ADC performance, which must be carefully taken care of. This effect could be mitigated with a larger reference capacitor but that is not an elegant solution.

In this paper, the proposed elegant solution is enforcing the short switches to short the LHS switch from P side and N side. By doing this, this signal-dependent-injected charge on the LHS would become a common-mode signal and a zero differential voltage. It might introduce a little common-mode voltage shift to the ADC RHS, which is minimal and a second-order effect.

D. Signal-Dependent Voltage Droop

There is often a concern that the bit weight is still signal dependent. This argument follows that as lower bits reference capacitors are inserted, these lower bits reference capacitors will inject reference charge to the upper bits. Because ADC bits decisions including the lower bit decisions are signal dependent, this injected reference charge is also signal dependent. You will notice the reference capacitor from the upper bits are still undergoing voltage droop during the lower bits trial period. This voltage droop would be signal dependent, unfortunately. In reality, yes, the lower bits decisions will inject signal-dependent reference charge to the upper bits reference capacitors when lower bits are applied. And we can also confirm that we see voltage droop at the upper bit reference capacitors. This is similarly reported in [4]. However, the contribution from upper bits has already been made when those upper bits were applied. Although signal-dependent charge is still drawn from upper bits *after* upper bits are applied, the bit weights do not shift and are still signal independent and orthogonal. The underlying reason is the reference capacitors are passive devices and the upper bits reference capacitors are effectively “dead” when lower bits reference capacitors are inserted. Any voltage change at the comparator input can only be attributed to the particular inserting bits, not the dead bits.

E. Calibration

The use of passive charge sharing leads to a non-radix-2 ADC in this paper so a traditional charge balance calibration (QBC) method cannot be used. There are two major differences when compared to a traditional SAR ADC: 1) this type of ADC needs to calibrate deeper and 2) this type of ADC needs to follow the same capacitor array topology evolution during calibration as in a normal conversion. A foreground QBC has been developed specifically for precision SAR ADCs architected with reference reservoir capacitors.

The main idea of this calibration is to preset the bit-under-calibration (BUC) to a high (low) setting and then run a partial SAR conversion with the lower bits to determine the magnitude of the BUC weight, while keeping all the bits above BUC irrelevant. To remove any possible offsets, the partial SAR conversion is carried out with BUC preset to Hi in a first run and then preset to Low in a second run. The difference between the two runs are taken to determine the bit weight after averaging a number of repeated runs to remove noise. An example is given in Fig. 14. As aforementioned, the capacitor array topology evolution in calibration must be identical to that in normal conversion to make the calibration work. To keep an identical capacitor array evolution, the upper bits are still switched to reference capacitors but the reference capacitors for those bits are discharged. Other than the fact that some of the bits are preset during calibration and some reference capacitors are discharged, the DAC undergoes the same operation during the calibration and conversion. By doing this, the calibration will take account of any mismatch/sequence-dependent-bit-weight/parasitic capacitance of the bit capacitors and the reference capacitors as a whole. As the upper bits will need the lower bits weights to calculate their bit weights, this

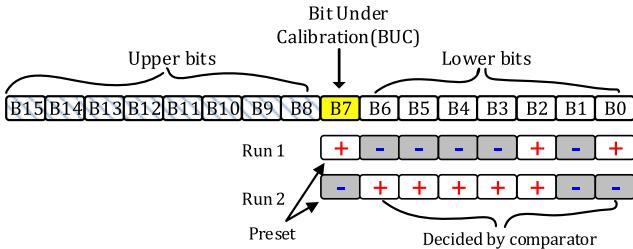


Fig. 14. Calibration example (calibrating bit 7): all upper bits are set to null, b7 is preset, and the lower bits are decided by comparator. There are also some redundancy bits but are omitted.

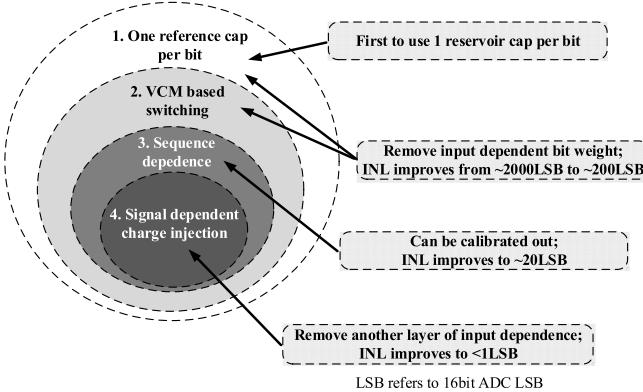


Fig. 15. Summary of the techniques to achieve high linearity for passive-charge-sharing SAR ADC.

calibration is bottom-up: lower bits are calibrated first. A more detailed description on the calibration can be found in [10]. The calibration engine is off-chip.

F. ADC Gain Error

As could be easily seen, this charge-sharing ADC will have inherent gain error which is proportional to the ratio of the reference capacitor to bit capacitor. A static gain error is acceptable in most cases. It could be solved by adding redundant bits. However, the gain error variation over process/voltage/temperature should be carefully designed. An easy way to improve the gain error variation is to implement the reference capacitors and the bit capacitors all in the same type of devices. This will keep the ratio of the bit capacitor to reference capacitor to a nearly constant number.

G. Summary

The following onion analogy in Fig. 15 gives a summary of what we discussed above. On the outmost layer of the onion is the use of one dedicated reference capacitor per bit. The next layer one would be using of decide and set. By peeling these two outmost layers off, we would be able to remove most of the signal-dependent bit weight and improve the INL to several hundreds of LSBs at 16-bit ADC level. The next layer is on the sequence-dependent bit weight. Understanding this effect and following its mechanism in calibration, one will be able to remove its effect by a calibration. This further improves the performance to the 20-LSB level. A next layer is to remove the signal-dependent charge injection. This should

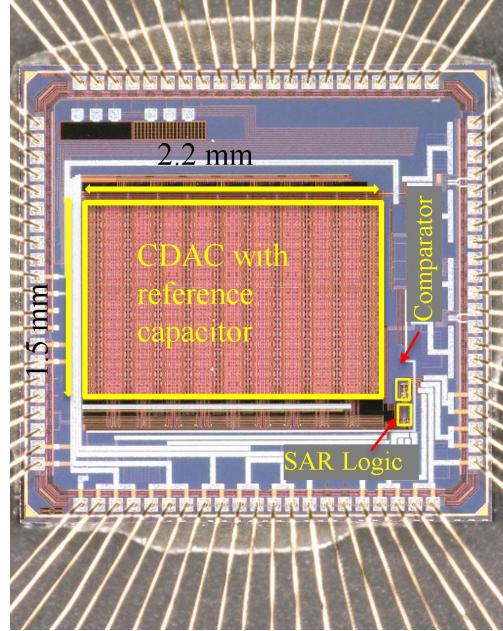


Fig. 16. Die photograph of the test chip.

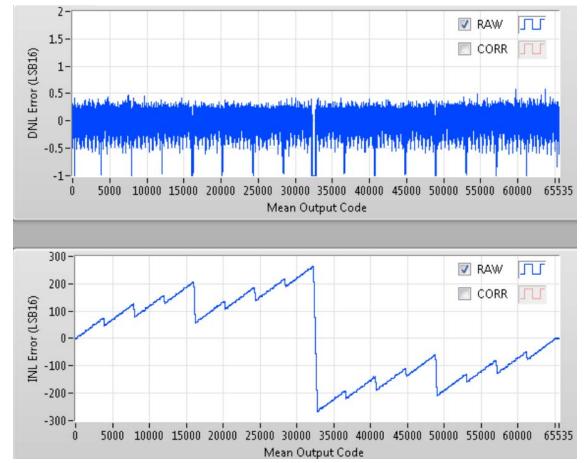


Fig. 17. Measured DNL/INL before calibration.

be able to reduce the INL to sub-LSB level. A passive-charge-sharing ADC is of no mystery than a traditional charge-redistribution SAR.

VI. MEASUREMENT RESULTS

The prototype chip is fabricated in a 55-nm technology. The die photograph is shown in Fig. 16. The total sampling capacitor size is 25.6 pF with 8 \times reference capacitor to bit capacitor ratio. Both the bit capacitor and the reference capacitor are made of method of moment capacitors.

As illustrated in Fig. 17, the un-calibrated INL can be as large as 250 LSBs, due to the sequence-dependence bit weight as discussed in Section V. This un-calibrated INL matches well with simulation as well as hand calculation based on (6).

An off-chip calibration is performed by balancing the upper bits weights with the lower bits [10]. When calibrating a certain bit, all bits above this BUC are connected to a fully discharged reference capacitor; the BUC is set to high or low; an

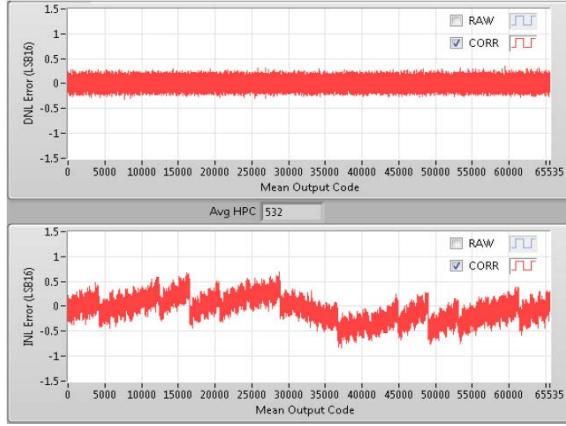


Fig. 18. Measured DNL/INL after calibration.

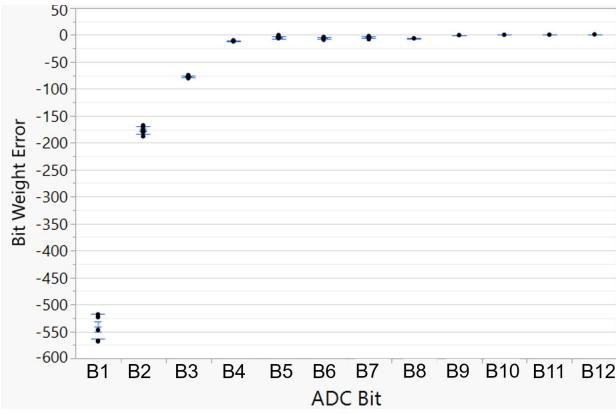


Fig. 19. Bit weight error distribution across seven different parts.

SAR conversion is performed for bits below BUC. By assuming the bits below a certain bit all have ideal values, the upper bit weights can be expressed using the lower bit weights. The BUC bit weight is then averaged over a number of cycles to reduce the noise. The calibrated bit weights are then used to produce the corrected ADC outputs. As seen in Fig. 18, the calibration algorithm has proven its ability to trim the part such that the INL is within ± 0.8 LSB at 16-bit level with no missing codes. The variation of the bit weights error from seven different parts is plotted in Fig. 19. As can be seen, the majority of the bit weight error comes from the sequence-dependent bit weight, which is about 1.7% of the bit weight; while the mismatch error accounts for about 0.15% of the bit weight.

A temperature cycle and a power supply variation were run on multiple parts to confirm the same coefficients hold over temperature/power supply variation. From Fig. 20, we can see that the calibration coefficients are also stable over temperature and power supply variation.

As the work is mainly focused on exploring the viability of passive-charge-sharing SAR ADC at 16-bit linearity, not all design aspects are optimized, while some aspects are sacrificed for a tape-out schedule purpose: 1) no internal clock generator was designed and the chip requires an external SAR clock to operate and 2) the DAC switches were designed using 3.3-V devices and powered by 3.3-V power supply while the

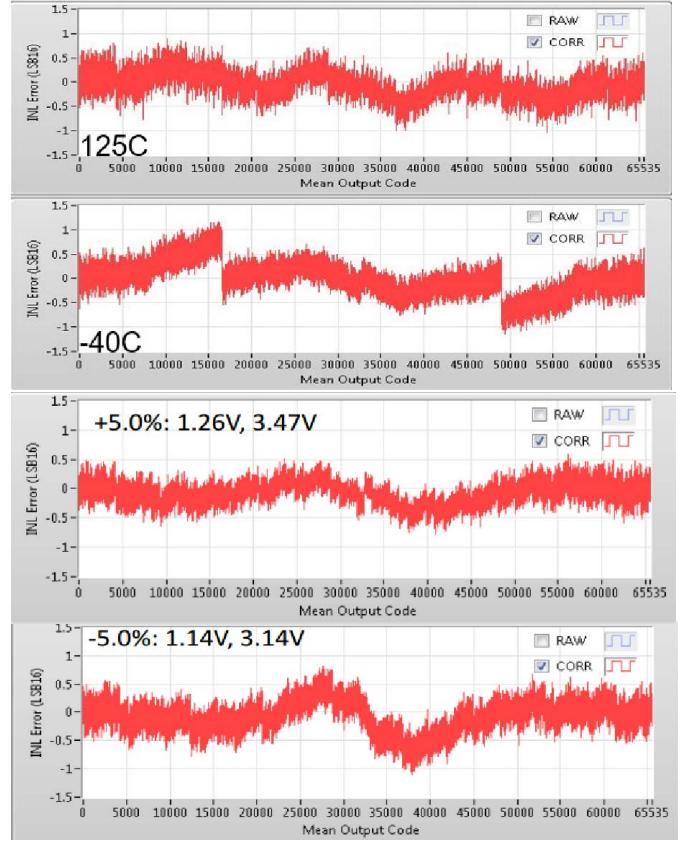


Fig. 20. Measured INL at high temperature/low temperature/high supply/low supply, after calibration at room temperature and nominal power supply.

TABLE I
COMPARISON WITH RECENT PASSIVE-CHARGE-SHARING SAR ADCS

	Craninckx[3]	Malki[6]	Kapusta[4]	This work
ADC Type	SAR	SAR	Interleave SAR with Flash	SAR
Charge sharing type	Passive	Passive	Passive w. reservoir cap.	Passive w. reference cap. per bit
Resolution [bit]	9	10	14	16
Speed	50MSPS	80MSPS	80MSPS	1MSPS
Power (mW)	0.29 (at 20MSPS)	6.0	31.1	6.95
INL [LSB]	+/- 0.6 (9-bit LSB)	+0.68/-0.7 (10-bit LSB)	+/- 1 (14-bit LSB)	+/- 0.8 (16-bit LSB)
SFDR[dB]	50.5	66.5	88.6	100
Cin[pF]	10	8/23	4.1	25.6
REF/VDD [V]	1.0/1.0	1.1/1.1	1.2/1.2	1.2/3.3
Area[mm ²]	0.08	0.08	0.5	3.3
FoM_S(dB)	154.1	153.2	164.7	159.6
Process	90nm	40nm	65nm	55nm

input signal range is limited to 1.2 V as the comparator was reused from a low-voltage design. The first one limits the SAR ADC operation speed as the SAR clock beyond 40 MHz is difficult to transmit through the chip IO. The second one decreases the DAC power efficiency by about 9 dB. However, as the main goal of this tape-out and the main topic of this paper is to research on the improving the linearity of the passive-charge-sharing SAR, these sacrifices are easily justified.

Table I gives a summary of the performance of the ADC from testing results and a comparison with other recent passive-charge-sharing ADCs. The figure of merit (FoM) is not competitive compared to the state-of-the-art SAR ADCs, but the linearity is the best among reported passive-charge-sharing SARs [3]–[5]. With a self-timed internal clock generator [4], a 3.3-V input signal range instead of 1.2-V reference, and a separate MSB ADC [11], [12] to resolve the first few MSBs, the FoM should be easily increased.

VII. CONCLUSION

This paper explored passive-charge-sharing SAR ADC for high-precision SAR ADC. A new passive-charge-sharing SAR ADC architecture with one-reference-cap-per-bit and short switch is proposed along with a calibration method addressing the necessary steps to achieve a 16-bit linearity. We showed that a linear ADC could be achieved using a small pre-sampled voltage charge reference on chip. This linearity holds up under temperature and voltage variation. Testing results validated the learning and proved that passive charge sharing is viable at the 16-bit level linearity for the first time. The presented work shows ± 0.8 LSB INL at 16-bit level. With this foundational work, a fast and precision SAR ADC (normally referring to ADCs beyond 16 bit and beyond 10 MSPS) should be achievable in the very near future [13].

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