Frequency and Power Scaling in mm-Wave Colpitts Oscillators

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***Abstract*— The maximum oscillation frequency depends on the oscillator topology and the loss of oscillator's active and passive components. The oscillator phase noise, and hence the oscillator figure-of-merit (FOM), degrades much faster than the well-known low-frequency expressions as the oscillation frequency reaches the maximum oscillation frequency. This paper covers the analysis and design of Colpitts oscillators with the best possible phase noise as the oscillation frequency approaches the maximum oscillation frequency while predicting the degradation in FOM. Experimental results corresponding to proof-of-concept differential Colpitts oscillator prototypes at 106 and 148 GHz that use a resonant biasing scheme to reduce phase noise, implemented in a 130-nm SiGe HBT BiCMOS technology, are presented. Ideally, the oscillator phase noise at a given frequency can be reduced by increasing the power consumption, while appropriately scaling the oscillator components. Such power scaling cannot be done indefinitely as it leads to impractical passive component values. Coupling identical oscillators is an alternate approach to enhance the phase noise. In this paper, a common-mode coupling scheme is introduced as a robust technique in reducing phase noise in millimeter wave frequencies. Experimental results of a 106-GHz 8-element common-mode coupled Colpitts oscillator, implemented in a 130-nm SiGe HBT BiCMOS technology, with a measured phase noise of −111 dBc/Hz at 1-MHz offset while consuming 90 mW are presented.**

***Index Terms*— Colpitts oscillator, coupled oscillator, millimeter wave (mm-wave), oscillator, phase noise, voltage-controlled oscillator (VCO).**

I. Introduction

THE exponential growth of data demand has caused millimeter wave (mm-wave) phased-array transceivers to gain traction for consumer (e.g., connectivity and 5G) and infrastructure (e.g., data centers, backhaul, and satellite communications) applications. To increase the overall data throughput over a given bandwidth, complex modulations may be used [1]. The use of complex modulations leads to stringent frequency synthesizer requirements. As an example, a 1024-quadrature amplitude modulation scenario requires an rms phase noise of less than 0.25° to limit the phase noise induced signal-to-noise ratio degradation to 1 dB [2]. Assuming a type II PLL frequency synthesizer topology, this requirement can translate to lower than −110-dBc/Hz phase noise specification at 1-MHz offset for the mm-wave voltage controlled oscillator (VCO) [2].

A significant body of work has been published in the area of mm-wave frequency generation using the commercial silicon processes. Frequency synthesizers with output frequencies as high as 500 GHz have been reported [3], [4]. A major block that determines the overall power consumption, tuning range, and phase noise of mm-wave frequency generation systems is the mm-wave oscillator. Much work in this area has been focused on increasing the oscillation frequency while delivering moderate to high output powers [5], [6]. The mm-wave oscillators can be categorized into fundamental and superharmonic oscillators; the latter includes push-push [7], triple-push [8], and self-mixing [9] topologies. Based on the results of [10], oscillator topologies can be investigated in terms of their maximum oscillation frequency and their dc-RF efficiency in mm-wave frequencies. However, it is unclear whether to use fundamental or superharmonic oscillator and which oscillator topology to use at mm-wave frequencies when lowest phase noise for a given power consumption is the objective. Theoretical and experimental study of the phase noise of mm-wave oscillators as the oscillation frequency approaches their maximum oscillation frequency can be very helpful in making such choices.

Given a certain power budget, circuit techniques can improve the achievable phase noise [12]–[14]. However, each oscillator topology has a lower bound of achievable phase noise set by the quality factor of the passives and properties of the active device; this bound rapidly increases as the oscillation frequency gets close to the maximum oscillation frequency of the chosen oscillator topology. Once an optimum design is achieved for a given topology and power consumption, the design may be appropriately scaled to reduce phase noise. In mm-wave implementations, however, passive component values of a scaled oscillator can quickly become impractical because of either the self-resonance frequency of large capacitors or the inductor values that become close to interconnect parasitics. Phase noise may be improved by coupling oscillators without requiring to scale the passive values [15], [16]. In this paper, frequency and power scaling in mm-wave frequencies will be analytically and experimentally treated for Colpitts oscillators with a focus on the active device limited operation. In Section II, analysis and simulation results of phase noise scaling will be presented. In Section III, measurement results of two differential Colpitts oscillators at 106 and 148 GHz will be discussed confirming the derived

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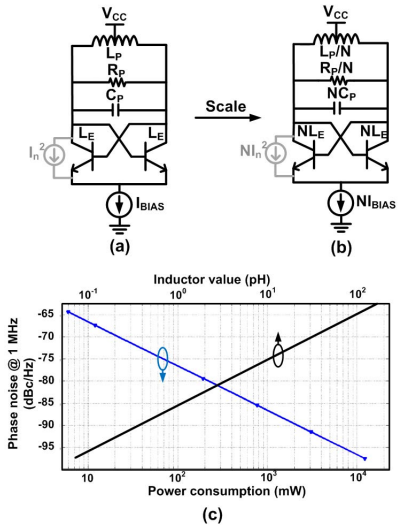

Fig. 1. (a) Schematic of a cross-coupled pair *LC* oscillator. (b) Schematic of a power-scaled cross-coupled pair *LC* oscillator. (c) Corresponding phase noise and inductor value as a function of power consumption; the unscaled design parameters are $L_P = 140$ pH, $Q = 10$, $I_{\mathrm{BIAS}} = 4$ mA, $L_E = 2$ μm, C_P is the parasitic capacitor of the cross-coupled pair, and the oscillation frequency is 73 GHz, which is very close to the maximum oscillation frequency for this topology (79 GHz).

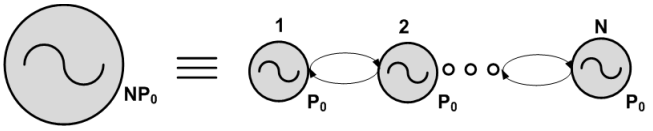

Fig. 2. Power scaling in a single oscillator compared with an array of coupled oscillators. Both schemes will consume N times the original power, leading to $10\log(N)$ improvement in phase noise.

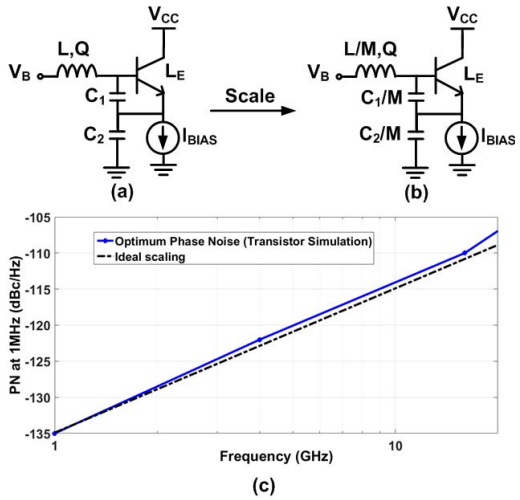

Fig. 3. (a) Schematic of a Colpitts oscillator. (b) Schematic of a frequency-scaled Colpitts oscillator. (c) Corresponding phase noise versus frequency. In simulations, $L = 7.9$ nH, $C_1 = C_2 = 6.5$ pF, $Q = 10$, $L_E = 5$ μm, $V_{\mathrm{CC}} = 1.6$ V, and $I_{\mathrm{BIAS}} = 6$ mA.

phase noise scaling in mm-wave frequencies. In Section IV, design and implementation of an 8-element common-mode-coupled 106-GHz oscillator is presented. Section V concludes this paper.

II. Power and Frequency Scaling

In this section, we quantify how phase noise scales with power consumption and oscillation frequency, especially as the frequency approaches the maximum oscillation frequency that a given topology and technology support.

A. Ideal Phase Noise Scaling

Under relatively general conditions, the following two statements are true for oscillator phase noise scaling.

1) *Power Scaling:* At a certain frequency f_0, the phase noise of an optimally designed oscillator can be reduced by $10\log(N)$ dB by scaling transistor sizes, current consumption, and passive elements admittances by N (topology-independent).
2) *Frequency Scaling:* For constant power consumption, the phase noise of an oscillator at Mf_0, constructed by scaling the passives of an f_0 oscillator increases by $20\log M$.

These simple rules can be readily observed from Leeson model or impulse sensitivity function model for phase noise [17]. Fig. 1(a) and (b) shows the scaling rule (1) for a conventional cross-coupled pair *LC* oscillator as an example.

Fig. 1(c) shows the simulated phase noise of a 73-GHz cross-coupled pair *LC* oscillator as a function of dc power consumption. The technology used in all simulations is a 130-nm SiGe HBT BiCMOS technology (8HP) to reflect the integrated implementations discussed in Section III. The size of the passive components can become impractical for large N. As shown in Fig. 1(c), to achieve the phase noise of -85 dBc/Hz at 1-MHz offset frequency away from a 73-GHz carrier, the inductor value should be chosen as 1 pH, which is not practical. Notice that in this example, the desired frequency is chosen very close to the maximum oscillation frequency of the topology, and therefore, the phase noise is pretty poor to begin with. This practical limitation poses a challenge in achieving low phase noise at mm-wave frequencies. To overcome this limitation, one solution is coupling multiple oscillators. As conceptually shown in Fig. 2, coupling N oscillators will ideally result in phase noise improvement of $10\log(N)$, which is the same as power scaling the core oscillator by a factor on N.

The frequency scaling rule is true if the quality factor of passive components remain constant under scaling and transistor parasitics is neglected, i.e., the transistor is modeled as a memory-less nonlinearity. Fig. 3(a) and (b) shows the frequency scaling rule for a Colpitts oscillator as an example. Fig. 3(c) shows the phase noise scaling for a Colpitts oscillator as a function of oscillation frequency. The phase noise of an optimally designed oscillator sharply deviates from this behavior as the oscillation frequency approaches the maximum oscillation frequency of the chosen topology. Therefore, frequency scaling of mm-wave oscillators need to be investigated in more detail.

B. Phase Noise of Frequency-Scaled mm-Wave Oscillators

Consider the Colpitts oscillator schematic shown in Fig. 4(a) and its simplified equivalent large-signal model in Fig. 4(b)

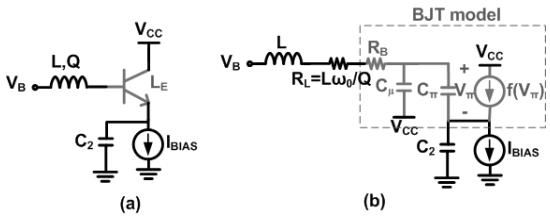

Fig. 4. (a) Schematic of an mm-wave Colpitts oscillator. (b) Simplified equivalent model of an mm-wave Colpitts oscillator using a simplified high-frequency large-signal transistor model.

where major transistor parasitics are included and $f(V_\pi) = I_s e^{V_\pi/\mathrm{mV}_T}$, where $m \approx 1.4$ in our technology. The maximum oscillation frequency of the transistor, as defined by the Mason invariance function [10], can be written as

$$f_{\max} = \frac{1}{4\pi}\sqrt{\frac{g_m}{(C_\pi + C_\mu)C_\mu R_B}} \tag{1}$$

where g_m is the small-signal transconductance of the device. In our 130-nm SiGe HBT technology, from simulations, for a transistor with emitter length $L_E = 8\ \mu$m, $f_{\max}$ is maximized for $I_{\mathrm{BIAS}} = 7$ mA. For this dc current, $R_B = 19\ \Omega$, $C_\pi = 101$ fF, $C_\mu = 9$ fF, and $g_m = 200$ mA/V resulting in $f_{\max} = 260$ GHz.

Maximum oscillation frequency of the Colpitts oscillator shown in Fig. 4 can be found by finding the C_2 capacitance value, which maximizes the frequency at which the real part of the impedance looking into the base of the transistor becomes zero. This procedure will lead to

$$f_{\max,\mathrm{colp}} = \frac{f_{\max}}{\sqrt{1 + g_m R_B \frac{C_\mu}{C_\pi}}} \tag{2}$$

which happens when $C_2 = C_\mu(1 + 2g_m R_b(C_\mu/C_\pi)) = 15$ fF resulting in $f_{\max,\mathrm{colp}} = 224$ GHz. Circuit level simulation shows $f_{\max,\mathrm{colp}} = 222$ GHz.

Fig. 5(a) shows an equivalent circuit for the simplified schematic of Fig. 4(b) where L, R_B, and C_μ are lumped into an equivalent series *RL* circuit at the oscillation frequency given by

$$f_0 = \frac{1}{2\pi\sqrt{L\left[\frac{C_\pi C_2}{C_\pi + C_2} + C_\mu\right]}}. \tag{3}$$

Given a transistor geometry and bias current, $f_{\max,\mathrm{colp}}$ will be fixed. For a certain inductor quality factor, startup condition can be satisfied for a minimum inductor size. In this section, we will start from this maximum frequency of oscillation and derive optimum scaling criteria as the desired oscillation frequency is reduced. The optimum scaling criteria are determined to reach lowest achievable phase noise at each frequency. At low-enough frequencies, the scaling criteria should converge to ideal scaling rules discussed in Section II-A.

For a small frequency range below the maximum oscillation frequency, (referred to as regime 1 in this paper), and as shown in the proceeding analysis, it is optimum to only scale the inductor to change the frequency of operation while keeping

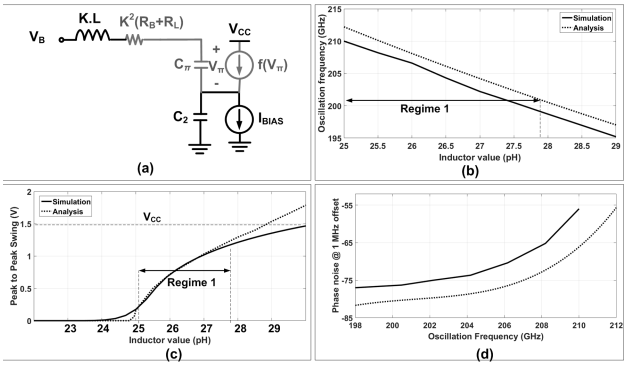

Fig. 5. (a) Equivalent model of the Colpitts oscillator in regime 1. Simulated and analytical (b) oscillation frequency as a function of inductor size, (c) oscillation amplitude as a function of inductor size, and (d) phase noise as a function of oscillation frequency. In transistor-level simulations, $L_E = 8\ \mu$m, $I_{\mathrm{BIAS}} = 7$ mA, and $V_{\mathrm{CC}} = 1.5$ V leading to $C_\pi = 103$ fF, $C_\mu = 9$ fF, $g_m = 200$ mA/V, $R_B = 19\ \Omega$, and $Q = 20$.

all other oscillator parameter constant. In this frequency range, it is not possible to pick passive components for the oscillator to work in the so-called voltage limited region of operation [11]. Fig. 5(b) shows the oscillation frequency as a function of inductor value. Amplitude of oscillation and phase noise of the simplified circuit shown in Fig. 5(a) can be derived analytically using quasi-periodic assumptions and averaging technique similar to the analysis shown in [19]. The peak-to-peak voltage swing across capacitor C_2 is given by

$$a_{\mathrm{pp},0} = \frac{4I_{\mathrm{BIAS}}L}{K1(R_B + R_L)C_2(1+\beta)}\frac{I_1\left(\frac{\beta a_{\mathrm{pp},0}}{2\mathrm{mV}_T}\right)}{I_0\left(\frac{\beta a_{\mathrm{pp},0}}{2\mathrm{mV}_T}\right)} \tag{4}$$

where $K = 1 + (C_\mu(C_\pi + C_2)/C_\pi C_2) \approx 2(1 + g_m R_B(C_\mu/C_\pi))$, $\beta = (C_2/C_\pi)$, and $I_1(.)$ and $I_0(.)$ are modified Bessel functions. In this regime, increasing the inductor value will sharply increase the oscillation amplitude, as shown in Fig. 5(c), when $Q_L = 20$. The sharp increase in the oscillation amplitude as a function of inductor value is the reason that in this regime, it is optimum to only scale the inductor value. As this equation shows, there are multiple ways to keep the change the oscillation amplitude. The objective here is to find the scaling condition that minimizes the phase noise as the oscillation frequency is reduced, and that is achieved in this regime by only scaling the inductor. As the oscillation amplitude reaches the voltage limited region [for values of the inductor larger than 28 pH in Fig. 5(c)], scaling rules should change.

Phase noise of the Colpitts oscillator due to the collector shot noise can be derived, as shown in [19]. An outline of derivations for the amplitude of oscillation and phase noise is presented in Appendix A for reference. The shot noise of the transistor can be written as

$$I_n(t) = \sqrt{2q\,I_{\mathrm{BIAS}}e^{(b_\pi + a_\pi\cos(\omega_0 t))/\mathrm{mV}_T)}}W(t) \tag{5}$$

where q is the charge of electron, a_π is the voltage swing across C_π, b_π is the dc voltage change across the base–emitter under steady-state oscillations ($b_\pi = 0$ in absence of oscillation) [19], and $W(t)$ is the standard white Gaussian noise. Due to the periodic nature of the base–emitter swing,

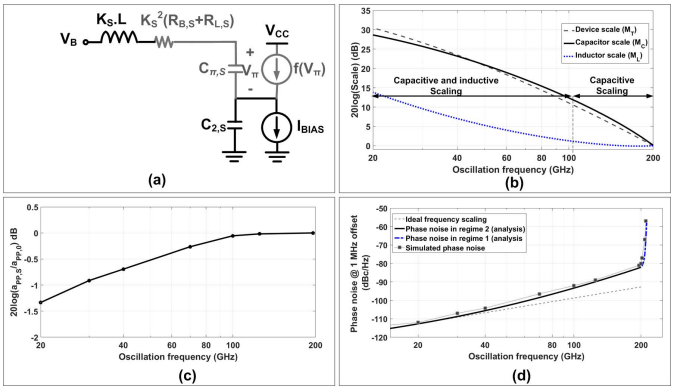

Fig. 6. (a) Equivalent model of the scaled Colpitts oscillator in regime 2. (b) Optimum device, capacitor and inductor scaling factors as a function of oscillation frequency. (c) Simulated normalized amplitude of oscillation as a function of oscillation frequency. (d) Analytical and simulated phase noise of the oscillator across the entire frequency scaling range (regimes 1 and 2) and comparison with ideal phase noise scaling.

this noise is cyclostationary. Note that b_π changes as a_π changes to keep the total dc current flowing through the transistor equal to $I_{\rm BIAS}$. Phase noise of the oscillator can be written as

$$L(\Delta f) = 10\log\left(\frac{\Gamma_{\rm rms}^2 q I_{\rm BIAS}}{C_2^2(1+\beta)^2 a_{\rm pp}^2}\right) \tag{6}$$

$$\Gamma_{\rm rms}^2 = \frac{\text{average}(e^{a_\pi \cos(T)/\text{mV}_T}(\sin(T))^2)}{\text{average}(e^{a_\pi \cos(T)/\text{mV}_T})} \tag{7}$$

where the average$[g(T)]$ operator finds the average of the function $g(T)$ over 2π. The denominator in (7) is to accommodate for the dc voltage change b_π as the voltage swing changes. For regime 1, $\Gamma_{\rm rms}^2$ varies from 0.5 to 0.2 as the voltage swing increases.

To design the optimum oscillator at frequencies below regime 1 (i.e., oscillator amplitude can and should reach the voltage limited region), referred to as regime 2, where the oscillation amplitude does not increase sharply with increasing L, capacitor C_2, transistor emitter length L_E, and base inductor L should all be scaled following:

$$f_{0,S} = \frac{f_0}{M} \tag{8}$$

$$C_{2,S} = M_C C_2 \tag{9}$$

$$L_{E,S} = M_T L_E \tag{10}$$

$$L_S = M_L L \tag{11}$$

where $f_{0,S}$ is the scaled frequency of oscillation, f_0 is the lowest oscillation frequency in regime 1, C_2 and L are the values of emitter capacitor and inductor at f_0, and L_E is the emitter length chosen for regime 1 ($L_E = 8$ μm for $I_{\rm BIAS} = 7$ mA), and scaling factors M_C, M_T, and M_L are constants that will be found later. To keep the quality factor of the inductor constant across frequency, $R_{L,S} = R_L(M_L/M)$. For the scaled device with emitter length $L_{E,S}$, $C_{\mu,S} = M_T C_\mu$, $R_{B,S} = (R_B/M_T)$, and $C_{\pi,S} = g_m\tau_f + M_T C_J$, where $g_m\tau_f$ is the intrinsic base–emitter capacitor and C_J is the base–emitter junction capacitor. For the 8-μm device, $g_m\tau_f =$ 78 fF and $C_J = 25$ fF. Similar to Fig. 5(a), in Fig. 6(a), the inductor L_S, resistor $R_{B,S}$, and capacitor $C_{\mu,S}$ are lumped into inductor $K_{\rm SL}$ and resistor $(R_{B,S}+R_{L,S})K_S^2$, where $K_S = 1+(C_{\mu,S}(C_{\pi,S}+C_{2,S})/C_{\pi,S}C_{2,S})$. For an optimally designed oscillator at a scaled down frequency, the following conditions must hold:

$$M_L(C_{\pi,S} \parallel C_{2,S} + C_{\mu,S}) = M^2(C_\pi \parallel C_2 + C_\mu), \tag{12}$$

$$a_{{\rm pp},S} = a_{{\rm pp},0}, \tag{13}$$

$$\text{minimize}(\text{PN}_M) \tag{14}$$

where $a_{{\rm pp},S}$ and $a_{{\rm pp},0}$ are the oscillation peak-to-peak swing across emitter capacitors at $f_{0,S}$ and f_0, and PN_M is the phase noise at the scaled frequency (f_0/M), respectively. PN_M is not normalized to frequency and is a function of scaled oscillation frequency. The equation describing PN_M will be defined as a function of scaling parameters and minimized through calculus. Condition (12) is showing that to scale the frequency by a factor of M, how LC needs to change in the Colpitts oscillator. Equation (13) is indicating that we are keeping the oscillation amplitude constant while frequency scaling is done (holding the oscillator swing at the verge of voltage limited region). In this regime, $(I_1(\beta a_{{\rm pp},S}/2\text{mV}_T)/I_0(\beta a_{{\rm pp},S}/2\text{mV}_T)) \approx 1$, and therefore, the amplitude of oscillation can be written as

$$a_{{\rm pp},S} \approx \frac{4 I_{\rm BIAS} L_S}{K_S(R_{B,S}+R_{L,S})C_{2,S}(1+\beta_S)} \tag{15}$$

where $\beta_S = (C_{2,S}/C_{\pi,S})$. Since the oscillation amplitude of is kept constant, from (6), the phase noise of the scaled oscillator can be written as

$$\text{PN}_M = \text{PN}_0 - 20\log(M_C(1+\beta_S)) \tag{16}$$

where PN_0 is the phase noise at frequency f_0 following (6). Equation (16) is derived by applying (8)–(11) in (6) to find the phase noise at scaled frequency. Applying conditions (12) and (13) into the phase noise equation phase noise (20), the optimum scaling factors to minimize phase noise can be derived as

$$M_T = \frac{R_B+R_L}{R_{B,S}+R_{L,S}} \frac{\left(\frac{C_\mu+C_2}{2C_\mu}\right)^2 M^2 - 1 + \left(\frac{C_\mu+C_2}{2C_\mu}\right)^2}{1+(M-1)\frac{C_J}{C_\pi}} \tag{17}$$

$$M_C = \frac{R_B+R_L}{R_{B,S}+R_{L,S}}\left(\frac{C_\mu+C_2}{C_2}\sqrt{M_T} - M_T\frac{C_\mu}{C_2}\right) \tag{18}$$

$$M_L = \frac{M^2(C_\pi \parallel C_2 + C_\mu)}{C_{\pi,S} \parallel C_{2,S} + C_{\mu,S}}. \tag{19}$$

These conditions are derived by finding roots to partial derivatives of the equation for phase noise (16), while holding conditions (12)–(13). These equations are solved numerically to find each scaling parameter as a function of oscillation frequency. Fig. 6(b) shows the plot of the scaling factors as a function of oscillation frequency. Two distinct scaling regions can be observed in this plot. Above 100 GHz, the inductor value is relatively constant and frequency scaling is achieved by scaling the capacitor and device sizes. This is because in this frequency range, the effective quality factor of the equivalent inductor is dominated by the scaled device base resistance $R_{B,S} = (R_B/M_T)$; hence, according to (19),

the amplitude of oscillation can be kept constant for maximum capacitor scaling ($a_{\mathrm{pp},S} \propto (L[M_{TC})/(R/M_T)]$). Maximum capacitor and device scaling while the amplitude of oscillation is constant will in turn result in minimum phase noise. Below 100 GHz, the inductor base resistance starts to affect the amplitude of oscillation and inductive scaling is required to reach minimum phase noise. Fig. 6(c) shows the transistor-level simulated amplitude of oscillation normalized to the amplitude of oscillation at f_0 (a_{pp}). Notice that the scaling criteria keep the amplitude of oscillation close to constant over the entire frequency scaling range. Fig. 6(d) shows the scaled oscillator phase noise over regimes 1 and 2. Transistor-level simulation of phase noise follows the derived phase noise scaling [see (6) and (16)] over the entire frequency scaling range. At lower frequencies, the phase noise scaling reaches the ideal 20log(M) phase noise scaling, as discussed in Section II-A. An extremely sharp phase noise degradation close to the oscillator maximum oscillation frequency (regime 1) is observed.

C. Conclusion on Frequency Generation in mm-Wave Frequencies

Frequency generation circuitry at mm-waves may utilize fundamental oscillators (e.g., Colpitts, cross-coupled LC, and so on), harmonic oscillators (e.g., push-push, triple-push, and so on), or frequency multipliers. The proper choice would depend on the specifications, such as the desired frequency range, phase noise, and power budget as well as the available technology (actives and passives). Furthermore, a frequency generation circuitry often relies on a phase-locked loop or frequency synthesizer where the performance of other blocks, such as frequency divider and reference signal, also plays a critical role in the behavior of the entire system. Therefore, a one-size-fits-all solution to the problem of mm-wave frequency generation may not be found. There are, however, certain general conclusions that can be derived based on the preceding analysis. First, using a low-frequency oscillator design approach and following the basic frequency scaling rules to reach a high-frequency oscillator can result in drastically sub-optimal designs at mm-wave frequencies (as the frequency approaches the maximum oscillation frequency of a given topology). Second, with the objective of optimizing phase noise and oscillator figure-of-merit (FOM) for a given oscillator topology and assuming constant overall resonator quality factor across frequency, there are two clear frequency regimes. At low-enough frequencies (e.g., below 60 GHz in the 130-nm SiGe Colpitts oscillator example), the use of frequency multiplier or harmonic extraction will lead to worse FOM and overall phase noise for a given power consumption. At frequencies comparable to the maximum oscillation frequency of a chosen topology (e.g., above 120 GHz in the 130-nm SiGe Colpitts oscillator example), the use of fundamental frequency oscillator will result in very poor oscillator FOM (i.e., high phase noise for a given power consumption). For example, to implement a 140-GHz Colpitts oscillator in the 130-nm SiGe technology, the use of a 70-GHz oscillator with a frequency multiplier will result in a much lower phase noise for a given power consumption. It is noteworthy that this deviation happens well before the region in which the oscillation amplitude starts decreasing.

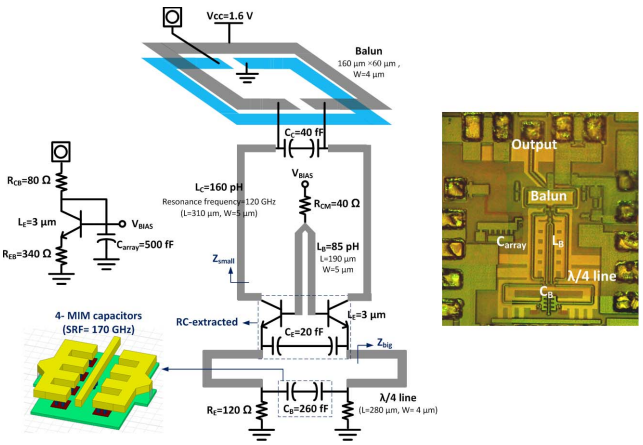

Fig. 7. Schematic and chip photograph of the 106-GHz Colpitts oscillator.

III. Implementation of mm-Wave Stand-Alone Colpitts Oscillators

In this section, we demonstrate implementation and measurement results of two mm-wave Colpitts oscillators that are designed at different mm-wave frequencies following the aforementioned design methodology. A 130-nm SiGe HBT BiCMOS process is used in all realizations.

In this technology, and ignoring layout parasitics, the maximum oscillation frequency that Colpitts topology can sustain is around 220 GHz. This value reduces to around 180 GHz once layout parasitics and other nonidealities are included. As such, to show the effect of transistor $f_{\max}$ on phase noise in this topology, and validate the aforementioned design approach, two Colpitts oscillators at 106 and 148 GHz are implemented. These two frequencies are chosen to represent the oscillator phase noise behavior in two different regions, i.e., sufficiently away and close to the maximum oscillation frequency of this topology. Design details of the 106-GHz oscillator are discussed first. The 148-GHz oscillator is designed as the frequency-scaled version of the 106-GHz oscillator.

Schematic and chip photograph of the 106-GHz oscillator are shown in Fig. 7. Differential Colpitts topology is used for its robustness to common-mode parasitics. The output is drawn from the collectors of the core BJT transistors and connected to the 50 Ω load through a balun. In the Colpitts topology, the core transistors need to see low impedance in the collectors to result in a large maximum oscillation frequency. Therefore, an impedance transformation network consisting of C_C and L_C is inserted between the balun and the collectors of BJT transistors. The capacitive divider network of the core comprises of BJT device capacitors C_π and metal-oxide-metal capacitors C_E with floating bottom-plate (to reduce the common-mode effective capacitor). C_E capacitors are implemented using third and fourth metal layers with $0.35-\mu$m spacing in between; these capacitors and interconnect parasitics up to fifth metal layer are derived by RC-extraction. All inductors and transmission lines are implemented as microstrip transmission lines with the signal routed on the 4-μm-thick top metal layer and the M_5 ground

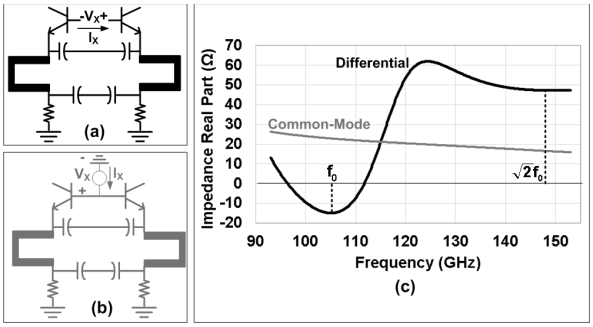

Fig. 8. Proposed Colpitts oscillator core (a) differential-mode excitation, (b) common-mode excitation, and (c) small-signal simulation of the impedance real part with differential- and common-mode excitations.

at 9-μm distance. The transistors are biased using a diode-connected transistor connected to the common node of the base inductors and resistors R_E. Use of resistors instead of current sources reduces the contribution of biasing circuitry to phase noise. Resistor R_{CM} is used to de-Q the base inductors in common mode. Quarter-wavelength ($\lambda/4$) transmission lines and C_B are used between R_E and core transistors emitters. Each C_B is implemented as four MIM capacitors with floating bottom-plate. This enables implementation of a very large capacitor value of 260 fF with a simulated self-resonance frequency of 170 GHz. In differential mode, C_B capacitors provide a low-impedance path to virtual ground at mm-wave frequencies. Therefore, in this mode, R_E is effectively shorted to ground and the impedance looking into the $\lambda/4$ line from the emitter side is high (Z_{big}). Therefore, R_E does not load the oscillator core. In addition, $\lambda/4$ line acts as an additional resonator in the oscillator, filters the injected noise from active core transistors, and reduce their effect on phase noise. Based on simulations, the use of the $\lambda/4$ resonator reduces the phase noise contribution of active core devices by 7 dB. In common mode, C_B capacitors are open-circuit. In this mode, the impedance looking into the $\lambda/4$ line from the emitter side is low preventing common-mode oscillations. Fig. 8 shows the simulated small-signal impedance real part of the proposed Colpitts oscillator core under differential- and common-mode excitations. For the common-mode excitation, the core is lossy across the frequency and unable to sustain oscillations. In differential mode, the core has negative input resistance in the 97–112 GHz frequency range; hence differential-mode oscillation in this frequency range is supported. The frequency range of 97–112 GHz is determined by the $\lambda/4$ line bandwidth. The chip consumes 11 mW from a 1.6-V supply for the lowest phase noise setting.

Measurement results of the implemented differential Colpitts oscillator are summarized in Fig. 9. Details of the measurement setup can be found in Appendix B. Fig. 9(a) shows the full W-band and close-in measured output spectrum directly read from the spectrum analyzer. Fig. 9(b) shows the de-embedded output power and oscillation frequency as a function of bias current. The oscillator has a measured maximum de-embedded output power of -6 dBm. Output power is within 3 dB of the peak output power across 105–108 GHz. Frequency tuning mechanism is through changing the bias current and consequently changing C_π.

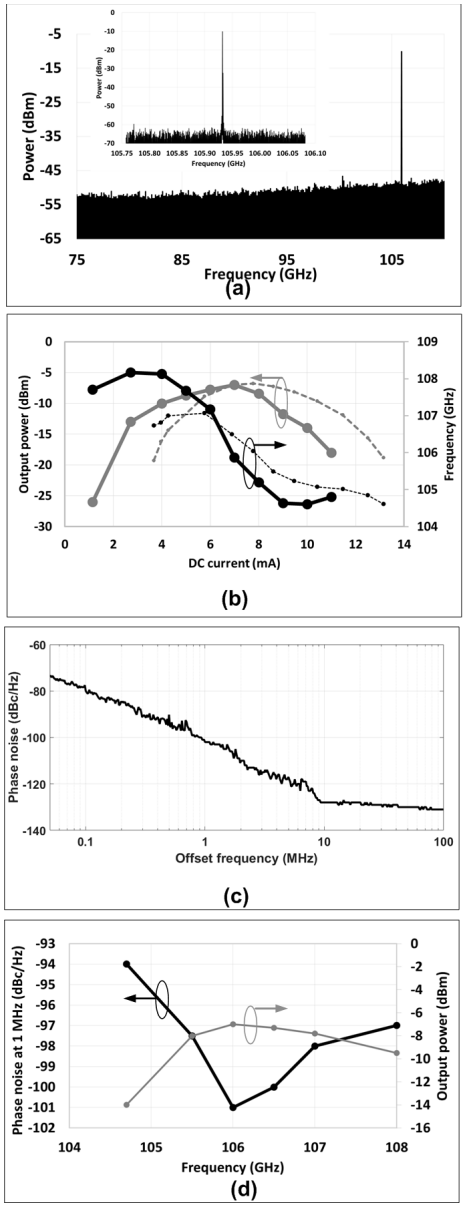

Fig. 9. Measurement results of the 106-GHz Colpitts oscillator (a) output spectrum, (b) output power and oscillation frequency versus bias current, (c) phase noise profile at 106 GHz, and (d) phase noise and output power versus oscillation frequency.

The oscillator has a measured phase noise of -102 dBc/Hz at 1-MHz offset [Fig. 9(c)] for a 106-GHz oscillation frequency.

Fig. 10 shows the schematic and chip photograph of the frequency-scaled 148-GHz oscillator. The design is similar to that of the 106-GHz oscillator, but adapted to 148 GHz according the scaling criteria discussed in Section II. Fig. 11 summarizes the measured results of the 148-GHz Colpitts oscillator. Fig. 12 shows good agreement between the measured results of the Colpitts oscillators and the simulated phase noises of the frequency-scaled Colpitts oscillator versus frequency, verifying the analysis discussed in Section II.

IV. Coupled mm-Wave Oscillator Arrays

As discussed in Section II-A, an optimally designed oscillator at a certain frequency and power consumption can

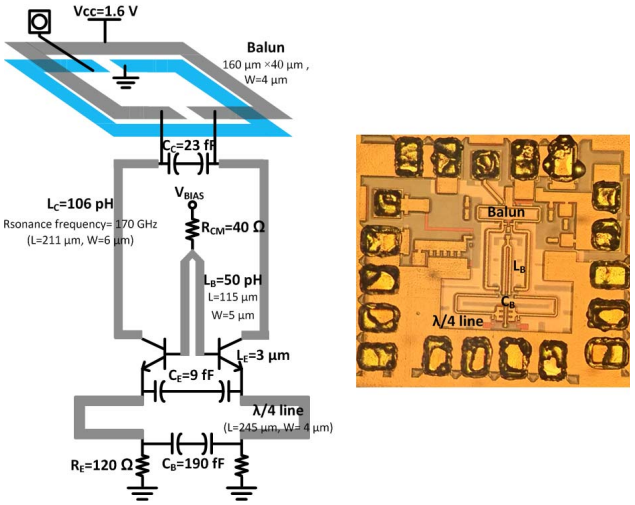

Fig. 10. Schematic and chip photograph of the frequency-scaled 148-GHz Colpitts oscillator.

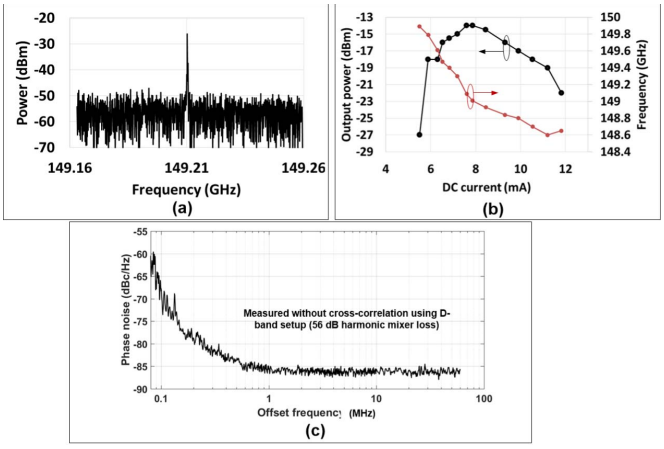

Fig. 11. Measurement results of the 148-GHz oscillator (a) output spectrum, (b) output power and oscillation frequency versus bias current, and (c) phase noise profile at 148 GHz.

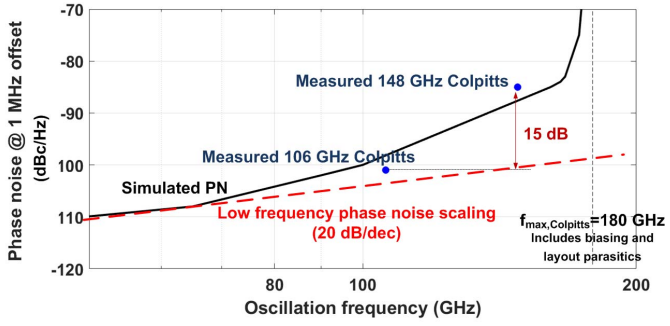

Fig. 12. Comparison of measured differential Colpitts oscillators with simulated optimum scaled phase noise of this topology.

be scaled to reduce phase noise. Because of the practical limitations of power scaling, phase noise may be alternatively improved by coupling. An ideal coupling scheme will not load the stand-alone oscillators while achieving the $10\log(N)$ dB phase noise improvement. We use a "common-mode coupling" scheme [18] that enables reaching close to the theoretical limit phase noise improvement ($10\log(N)$ dB for N elements) in

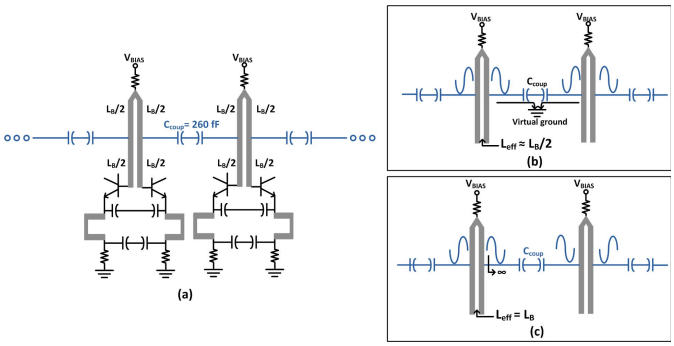

Fig. 13. (a) Proposed coupling scheme. (b) Differential-mode coupling (cannot be sustained). (c) Common-mode coupling.

practice, demonstrating very low phase noise in mm-wave frequencies.

Fig. 13(a) shows the concept of common-mode coupling employing the aforementioned 106-GHz differential Colpitts oscillator. Adjacent Colpitts oscillators are coupled through large coupling capacitors tapped from the center of the base inductors. In general, in-phase coupled oscillators may operate in differential or common mode. For this scheme, in the differential mode, as shown in Fig. 13(b), the large coupling capacitors essentially short the center tap of the base inductors to virtual ground, reducing the effective inductance seen by the core to $L_B/2$. Therefore, to support differential-mode coupled oscillations (not to be confused with the differential operation of a single Colpitts oscillator), the Colpitts oscillators would need to oscillate at $\sqrt{2}f_0$. As seen in Fig. 8, at this frequency, oscillations cannot be supported due to positive real part of the core impedance; hence, differential-mode coupled oscillation is suppressed in the coupled oscillators. In the common mode, the coupling network is open-circuit and does not load the oscillators; therefore, each core will oscillate as it would stand-alone. This property of the proposed coupling scheme leads to a couple of advantages. First, since the coupling network does not load the core oscillators, the required phase noise and the size of passives are completely de-coupled and in principle, one can achieve very low phase noise numbers. Second, the scheme is insensitive to series interconnect parasitic inductors as long as the differential-mode coupled oscillations cannot sustain (i.e., $L_{\text{par}} \ll L_B/2$). This means that the coupling scheme is robust to coupling mismatches, enabling the scheme to achieve close to theoretical limit improvement in phase noise due to coupling. The common-mode coupling concept is used to design and implement an 8-element coupled oscillator, as shown in Fig. 14. The implemented chip (Fig. 15) occupies an area of 1.7 mm × 1.4 mm and consumes 90 mW from a 1.6-V supply for the lowest phase noise setting. In a loop structure, each oscillator is coupled to its two neighbors using large floating-bottom-plate 260-fF capacitors. For the oscillators at the far left and far right, longer interconnect lines are needed to couple the oscillators. 660-μm lines are routed to connect these oscillators to the corresponding coupling capacitors. The outputs of the eight coupled oscillators are combined using a Wilkinson power combining tree with approximately 1.3-dB insertion loss per stage. The combined

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH SELECTED SILICON mm-WAVE OSCILLATORS

	This work Colpitts	This work 8-coupled	This work Colpitts	Ref. [15]	Ref. [12]	Ref. [13]	Ref. [3]	Ref. [21]	Ref. [23]	Ref. [24]	Ref. [25]
Frequency Range (GHz)	105-108	105-106	148.6-149.8	247-263	45-59.5	52-56.5	279-303	71-76	113.4-122.6	195	215-217
PN @100 kHz	-80	-90	-60	N/A	N/A	N/A	-50	-62	-60	-82.3	N/A
PN @ 1 MHz	-102	-111	-85	-94	-108	-103	-80.4	-93.5	-84	-97.2	-95
Power (mW)	6.4-12.8	64-95	9.6-16	227	132	36	105	36	5.6	38	79
Output power (dBm)	-6	-1	-13	4.1	1.5	N/A	-14	N/A	-15	6.5	5.6
Area (mm^2)	0.36	2.3	0.33	0.43	0.16	4	N/A	0.03	0.22	0.15	0.08
Tunability	No	No	No	Yes	Yes	Yes	Yes	Yes	Yes	No	No
Topology	Colpitts	8-element CM-coupled	Colpitts	8-element Standing wave	Triple push	Distributed Hybrid wave	Triple push	Gate-drain coupled	Inductor enhanced cross-coupled	Optimized feedback	Harmonic positive fb
Process	130 nm SiGe	130 nm SiGe	130 nm SiGe	65 nm CMOS	180 nm SiGe	65 nm CMOS	90 nm SiGe	28 nm CMOS	65 nm CMOS	55 nm SiGe	65 nm CMOS

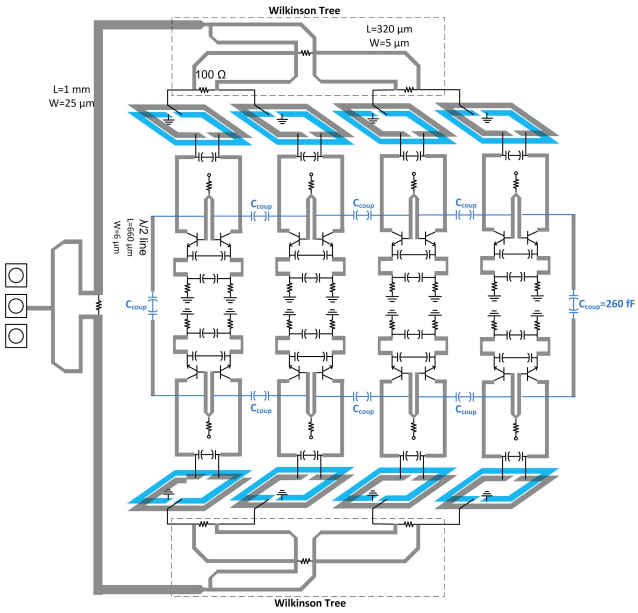

Fig. 14. Schematic of the 8-element common-mode coupled oscillator.

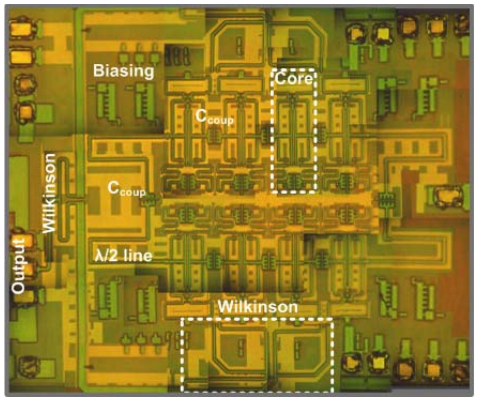

Fig. 15. Chip microphotograph of the 8-element common-mode coupled oscillator.

output directly drives the output 50 Ω. Fig. 16 shows the measurement results. The coupled oscillator has a measured de-embedded maximum output power of −0.4 dBm. The

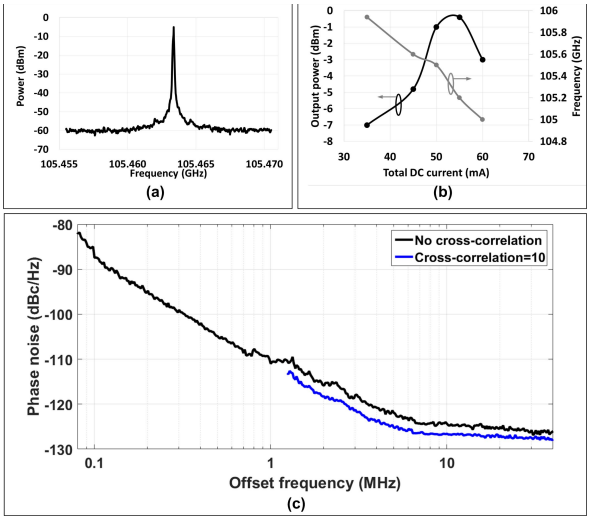

Fig. 16. Measurement results of the 8-element common-mode coupled oscillator. (a) Output spectrum directly read from spectrum analyzer. (b) De-embedded output power and oscillation frequency versus bias current. (c) Phase noise with 1 and 10 cross correlations at 105.6 GHz.

coupled oscillator frequency ranges from 105–105.6 GHz before output power drops more than 3 dB. At 105.4 GHz, the oscillator shows a measured phase noise of −111 dBc/Hz at 1-MHz offset. In the phase noise measurement with no cross correlation, the oscillator shows 20-dB/dec behavior below 1 MHz and it somewhat deviates from this behavior at higher offsets before hitting the phase noise floor. Cross correlation measurements with 10 times averaging show the continuation of the 20-dB/dec behavior at higher offsets and proves the deviation in the measurements without cross correlation to be due to inherent noise of the measurement setup. Table I shows the performance summary of implemented Colpitts oscillators in comparison with selected published silicon mm-wave oscillators. An important result of this paper is to show close to theoretical limit improvement in phase noise (9 dB) when relatively large number of oscillators (8 oscillators) are coupled. This has led to equal FOM of −192.6 dB for the one and 8-element coupled oscillators.

V. Conclusion

Oscillator phase noise is significantly modified from its textbook standard frequency-dependent behavior as the oscillation frequency approaches the maximum frequency that a given topology can support. A systematic approach to designing mm-wave Colpitts oscillators, with the object of achieving the lowest phase noise at a given power consumption, is presented. Analytical results and design procedures are verified experimentally through prototypes realized in a 130-nm SiGe HBT process.

Coupling oscillators is an effective method to reduce phase noise. A common-mode coupling scheme is proposed that leads to near ideal phase noise improvement with the number of coupled oscillators while it does not load individual oscillators. A 106-GHz 8-element common-mode coupled Colpitts oscillator is presented with a measured phase noise of -111 dBc/Hz at 1-MHz offset while consuming 90 mW reaching an FOM of -192.6 dB.

In most cases, the frequency of an oscillator must be tunable to enable frequency synthesis and locking to a stable low-frequency reference source. VCOs, utilizing varactors or arrays of switched capacitors, are commonly used as a tuning mechanism at lower radiofrequencies. At mm-wave frequencies, the quality factor of these tuning devices is very low and oftentimes significantly lower compared with the resonator. Methods that enable wide tuning range of mm-wave oscillators are the active areas of research. The phase noise limits shown in this paper provide an upper bound for what can be achieved in an mm-wave tunable oscillator as they primarily consider the effect of active devices at the oscillator core. The phase noise limits and design methodology for tunable mm-wave oscillators can be derived similarly knowing the tuning mechanism. The main point to consider is that the loss of active devices (limiting the $f_{\max}$) affects the phase noise significantly as the oscillation frequency increases. This would necessitate a modified design methodology for low phase noise mm-wave fixed- or tunable-frequency oscillator.

Appendix A
Derivation of Colpitts Oscillator Amplitude and Phase Noise

The oscillator phase noise can be derived by solving the oscillator nonlinear dynamical equations using quasi-harmonic approximations for state variables (voltages across capacitors and currents of inductors) and averaging [19]. The dynamical equations of the Colpitts oscillator of Fig. 5(a) can be written as

$$\dot{V_\pi} = \frac{I_L}{C} \tag{20}$$

$$\dot{V_2} = \frac{f(V_\pi) + I_L - I_{\text{BIAS}} + I_n(t)}{C_2} \tag{21}$$

$$\dot{I_L} = -\frac{K^2(R_B + R_L)I_L + V_2 + V_\pi}{\text{KL}} \tag{22}$$

where V_2 is the voltage across capacitor $C_{2,s}$ and I_L is the current of inductor KL. The approximate quasi-harmonic solutions for the state space variables may be expressed as

$$V_\pi(t) = \beta a_{\text{pp}}(t)/2\cos(\omega_0 t + \phi(t)) + V_{\pi,\text{dc}} + b_\pi(t) \tag{23}$$

$$V_2(t) = a_{\text{pp}}(t)/2\cos(\omega_0 t + \phi(t)) + V_{2,\text{dc}} - b_\pi(t) \tag{24}$$

$$I_L(t) = \frac{-(1+\beta)}{2\text{KL}\omega_0} a_{\text{pp}}(t)\sin(\omega_0 t + \phi(t)) \tag{25}$$

where $\beta = (C_2/C_\pi)$, and $V_{\pi,\text{dc}}$ and $V_{2,\text{dc}}$ are the dc voltages across C_π and C_2 in the absence of oscillations. By substituting these approximate solutions into the dynamical equations and applying the averaging technique, the amplitude and phase differential equations can be derived as

$$\dot{a_{\text{pp}}}(t) = -\frac{(R_B + R_L)\, a_{\text{pp}}(t)}{2\text{KL}} + \frac{2I_B}{C_2(1+\beta)} \frac{I_1\left(\frac{\beta a_{\text{pp}}}{2\text{MV}_T}\right)}{I_0\left(\frac{\beta a_{\text{pp}}}{2\text{MV}_T}\right)} \tag{26}$$

$$\dot{\phi}(t) = \frac{2I_n(t)}{C_2 a_{\text{pp}}(1+\beta)} \sin(\omega_0 t + \phi(t)). \tag{27}$$

The steady-state peak-to-peak oscillation amplitude can be found by the fixed point of amplitude differential equation leading to (4). Phase noise can be found by solving the stochastic phase differential equation (27) using (5) for $I_n(t)$. The steady-state value of $b_\pi(t)$ [b_π in (9)] can be found by equating the dc current of the transistor under large-signal operation to I_{BIAS}. The solution to the phase stochastic differential equation will lead to (6) and (7).

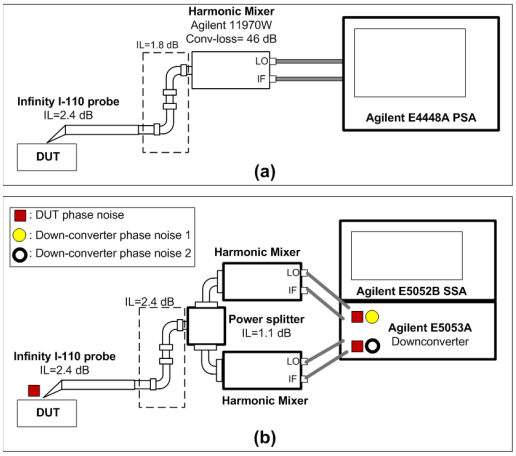

Fig. 17. (a) Spectrum measurement setup in W-band. (b) Phase noise measurement setup in W-band with cross-spectrum measurement capability.

Appendix B
Measurement Setup

Fig. 17 shows the W-band oscillator measurement setup. For spectrum measurements, the harmonic mixer conversion-loss calibration data are loaded to the spectrum analyzer. Cross-spectrum technique [22] is used for phase noise measurements using a W-band power splitter preceded by two harmonic mixers and a signal source analyzer. The cross-spectrum measurement technique is used to reduce the measurement phase noise floor by $5\log D$, where D is the number of averages in the cross-spectrum measurements.

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