

Analysis and Design of Ultra-Wideband mm-Wave Injection-Locked Frequency Dividers Using Transformer-Based High-Order Resonators

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Abstract—A transformer-based high-order resonator is proposed to improve the locking range (LR) of the millimeter-wave injection-locked frequency dividers (ILFDs). The LR limitations on ILFDs are discussed, and the operating principles of the proposed high-order resonator are analyzed based on their flattened phase response. The inductive gain peaking technique and the tail current source requirement are further analyzed for low power considerations. Two chips are fabricated in a 65-nm CMOS process to implement the proposed techniques; the first one measures an LR of 62.9% from 27.9 to 53.5 GHz while consuming 5.8 mW from a 1-V power supply and the second chip achieves an LR of 62.7% from 32.4 to 61.9 GHz while consuming only 1.2 mW from a 0.42-V power supply. The best figure of merit can achieve up to 24.7 GHz/mW.

Index Terms—Frequency divider, high-order resonator, inductive gain peaking, injection locked, injection-locked frequency divider (ILFD), locking range (LR), millimeter-wave, phase response, tail current source, transformer.

I. INTRODUCTION

THE great demands for the fifth generation (5G) wireless services make the millimeter-wave technology a key role in the future wireless communications [1]–[4]. The Ministry of Industry and Information Technology of the People’s Republic of China have recently allocated the 24.75–27.5- and 37–42.5-GHz bands for 5G mobiles research and development. The Federal Communications Commission in the United States also opens up vast amounts of the millimeter-wave spectrum, including 28 (27.5–28.35 GHz), 37 (37–38.6 GHz), and 39 GHz (38.6–40 GHz) bands. For millimeter-wave wireless systems, a wide operating bandwidth is more and more important to serve multi-band operations and multi-application integrations. Also, with different available frequency bands in China, the United States, and Europe, millimeter-wave

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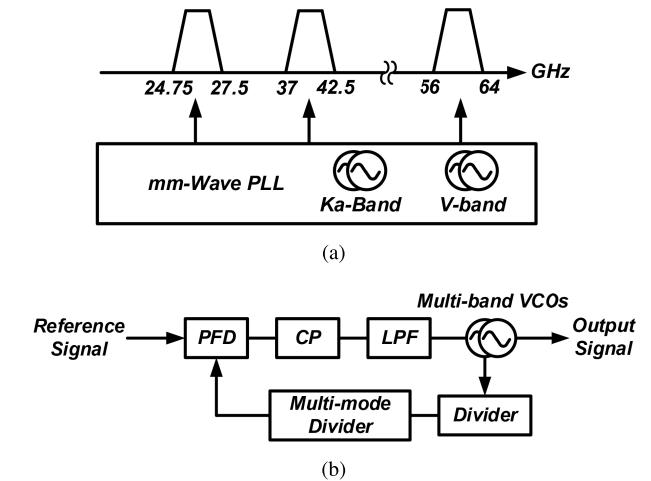


Fig. 1. (a) Frequency bands opened for 5G mobiles and the challenges in a wideband PLL design. (b) Conventional PLL-based frequency synthesizer, in which the first-stage frequency divider shown in Fig. 1(b) is often the bottleneck of the PLL design, which must operate in millimeter-wave frequency bands and also cover the bandwidth of the VCOs.

transceivers that can cover several frequency bands become meaningful for international roaming [Fig. 1(a)]. Among all the building blocks in the wideband millimeter-wave transceivers, the frequency synthesizers are the most challenge parts due to the complex architectures. Fig. 1(b) shows a conventional but mostly used phase-locked loop (PLL)-based frequency synthesizer. The first-stage frequency divider shown in Fig. 1(b) is often the bottleneck of the PLL design, which must operate in millimeter-wave frequency bands and also cover the bandwidth of the VCOs.

Several efforts have been made in designing the millimeter-wave wideband frequency dividers. The current-mode-logic (static) dividers [5]–[7], the regenerative dividers (Miller dividers) [8]–[10], and the injection-locked frequency dividers (ILFDs) [11]–[22] are the most attractive candidates for these applications. Current mode logic (CML) dividers achieve the widest bandwidth and occupy a very small chip area with no inductor required. However, their operating frequencies are often limited by the process node and need large supply currents to drive the circuits into high frequencies. Reference [6] used dynamic loads to expand the operating frequency and [7] used digital calibrations to handle the tuning requirement, which, however, still consume 4.8 [6] and 6.2 mW [7]. Miller dividers are able

to operate at higher frequencies with a narrower locking range (LR) compared with CML dividers although the power consumption is much lower [8]–[10]. The ILFDs are more attractive compared with other two kinds of frequency dividers. They can operate at very high frequencies with very low power consumption. However, the LR is usually narrow and many efforts have been made to overcome this challenge [11]–[22]. A shunt-peaking inductor [11] was applied to peak the second harmonic of the tail injection device, which boosted the injection signal and achieved a 7% LR at 19 GHz. A direct-injection method [12], [13] was used to achieve a better injection efficiency, and dual injection [14] was also used for efficiencies further enhancement. Some other injection methods were applied in [15] and [16] to increase the injection efficiency and achieved a good LR improvement. Apart from the injection efficiency consideration, the adaptive phase enhancement was implemented [17] and achieved a 20.5% LR. The frequency tracking [18] was another way to improve the LR, and it could reach up to 39.2% LR with only 2.9-mW power consumption. Multi-order resonance LC tanks were also used to increase the LR and the operating frequency [19]–[22], and two or more inductors are used in these multi-order designs. However, [19]–[21] used the multi-order tanks to decrease the effects of the parasitic and the ILFDs worked as distributed circuits. And in [22], two peaks in the LC -tank impedance were generated and dual-band operation was presented. However, all of these works have neglected the phase response of the high-order tanks and the LR was not sufficiently enlarged. Although good performances have been made in the previous works, the LR can still be improved to meet the process, voltage, and temperature (PVT) requirements in the multi-band millimeter-wave applications. The power consumption can get even less for better system design freedom, which may result in a much better figure of merit (FoM = Locking Range/Power Consumption).

In this paper, a transformer-based high-order resonator is proposed to improve the LR of the ILFD and an inductive gain peaking technique is used for lower power consumptions [23]. This paper expands the description in [23] to present more detailed analysis and design considerations of the high-order resonator used in ILFDs. Moreover, a deep analysis of power consumption reduction is presented in this paper with an inductive gain peaking technique and tail current source requirement discussion. Another new chip is fabricated to support the proposed analysis and achieves a better FoM. This paper is organized as follows. Section II analyzes the LR limitations and gives the design issues on the transformer-based high-order resonator. Section III analyzes the power consumption problems in ILFDs and gives two solutions. Section IV shows the circuit implementations and measurement results. Finally, conclusions are given in Section V.

II. LOCKING RANGE IMPROVEMENT USING HIGH-ORDER RESONATORS

A. Locking Range Limitations

To analyze the LR of the ILFD, a simplified behavior model of the conventional ILFD with direct injection is used and

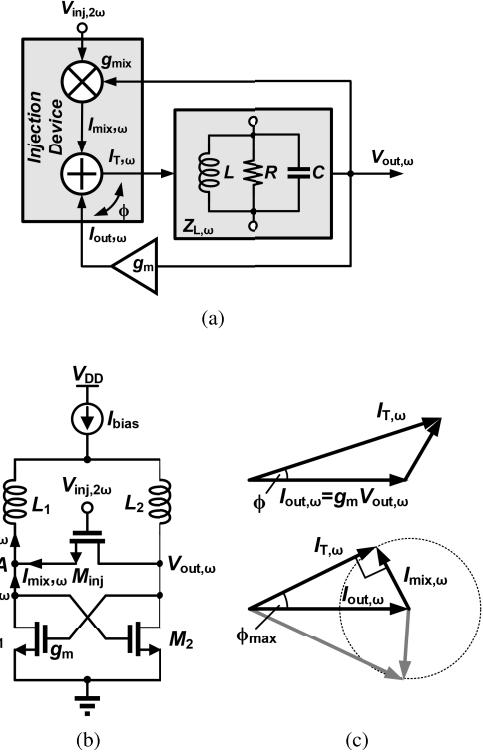


Fig. 2. (a) Simplified model of ILFD with LC -tank as a load resonator. (b) Conventional ILFD with direct injection. (c) Phasor diagram of the currents flowing into the adder.

shown in Fig. 2(a). The injection device M_{inj} here [Fig. 2(b)] is modeled as a mixer together with an adder, and the cross-coupled pair is modeled as a g_m gain cell with a feedback network to form an oscillator with the LC -tank Z_L . The operating principle is as follows. The injection voltage $V_{inj,2\omega}$ at the gate of M_{inj} is mixed with the output voltage $V_{out,\omega}$ at the drain (source) of M_{inj} through the injection device M_{inj} . Then, the mixed current $I_{mix,\omega}$ is added with $I_{out,\omega}$ generated from the cross-coupled pair at node A. The total current $I_{T,\omega}$ flows into the LC -tank and generates the output current [Fig. 2(b)]. According to [24], the LR can be calculated by assuming that the ILFD is under the locking condition and finding the edge of this condition. Coming back to the behavior model in Fig. 2(a), the current relationship in the adder is

$$I_{T,\omega} = I_{out,\omega} + I_{mix,\omega}. \quad (1)$$

Supposing the output voltage $V_{out,\omega}$ [working as the local oscillator (LO) signal for the mixer] is large enough so that the transconductance of the mixer g_{mix} is a constant

$$I_{mix,\omega} = g_{mix} V_{inj,2\omega} \quad (2)$$

$$I_{out,\omega} = g_m V_{out,\omega} \quad (3)$$

$$V_{out,\omega} = I_{T,\omega} Z_{L,\omega} \quad (4)$$

where g_m represents the transconductance of the cross-coupled pair, while $Z_{L,\omega}$ represents the impedance of the load resonator.

According to (3), the output voltage $V_{out,\omega}$ is in-phase with $I_{out,\omega}$, and the phasor diagram of $I_{T,\omega}$, $I_{mix,\omega}$ and $I_{out,\omega}$

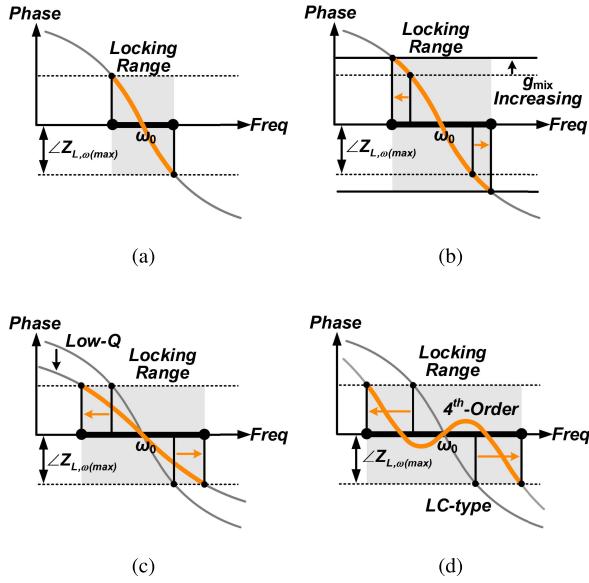


Fig. 3. (a) Locking range limitation based on phase condition. (b) Improve the LR by increasing g_{mix} . (c) Improve the LR by using low- Q LC-tank. (d) Improve LR by using the fourth-order resonator.

can be plotted, as shown in Fig. 2(c) with $I_{\text{out},\omega}$ representing $V_{\text{out},\omega}$. Here, ϕ is the phase difference between $I_{T,\omega}$ and $I_{\text{out},\omega}$ and can be calculated as

$$\phi = \angle I_{T,\omega} - \angle V_{\text{out},\omega}. \quad (5)$$

According to (4), the phase relationship between $V_{\text{out},\omega}$ and $I_{T,\omega}$ is

$$\angle V_{\text{out},\omega} = \angle I_{T,\omega} + \angle Z_{L,\omega}. \quad (6)$$

Therefore, comparing (5) and (6)

$$\phi = -\angle Z_{L,\omega}. \quad (7)$$

According to the phasor diagram shown in Fig. 2(c) and the phase differences calculated in (7), the phase differences between $I_{T,\omega}$ and $I_{\text{out},\omega}$ are generated by the complex impedance $Z_{L,\omega}$ and canceled out by the mixing current $I_{\text{mix},\omega}$. Consider $I_{\text{out},\omega}$ and $I_{\text{mix},\omega}$ (with the fixed injection power) having fixed amplitudes, and then, ϕ must have a maximum value ϕ_{\max} , and is plotted in Fig. 2(c)

$$\sin \phi_{\max} = \pm \frac{|I_{\text{mix},\omega}|}{|I_{\text{out},\omega}|}. \quad (8)$$

Solving (2), (3), and (8), the maximum phase shift caused by the resonator $\angle Z_{L,\omega(\max)}$ is

$$\angle Z_{L,\omega(\max)} = \pm \arcsin \left(\frac{g_{\text{mix}} |V_{\text{inj},2\omega}|}{g_m |V_{\text{out},\omega}|} \right). \quad (9)$$

Equation (9) shows the locking condition. When $\angle Z_{L,\omega}$ gets beyond (9), the ILFD will lose lock [Fig. 3(a)]. From this analysis, the LR can be increased in the following ways.

- 1) Increase the transconductance of the injection device [Fig. 3(b)]. This will increase the mixing current $I_{\text{mix},\omega}$ with the same injection voltage $|V_{\text{inj},2\omega}|$, which is not easy to be increased in millimeter-wave frequencies.

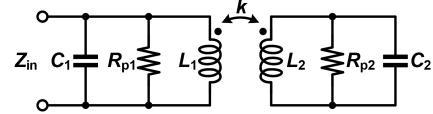


Fig. 4. Transformer-based fourth-order resonator.

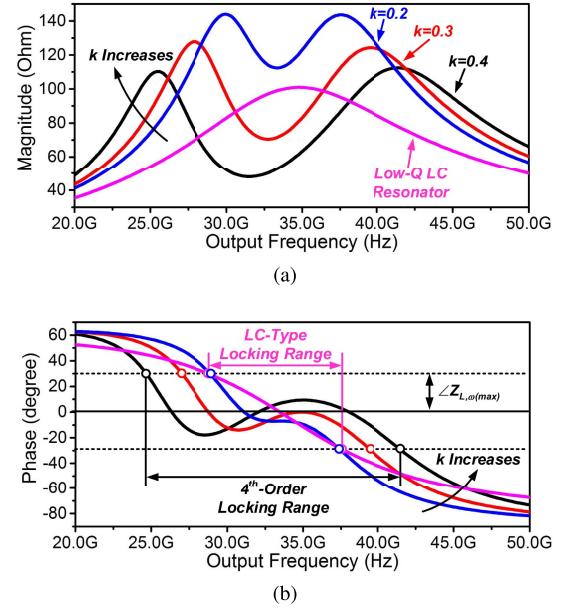


Fig. 5. Simulation results on the impedance of the resonator with different coupling factors (k) for the fourth-order transformer resonator and low- Q LC-tank. (a) Phase. (b) Magnitude.

- 2) Lower g_m and $|V_{\text{out},\omega}|$. However, this will face a lower output power and have risks of failure of oscillations. In addition, g_{mix} will get lower due to lower LO signal power.
- 3) Make the phase of the resonator $\angle Z_{L,\omega}$ flatten enough and having a value around zero over a wide frequency range [Fig. 3(c)]. When operating in wideband applications, $\angle Z_{L,\omega}$ cannot jump out of the upper or lower boundaries in (9).

The transconductance of the injection device can be optimized according to the method in [18], and thus, the solution (1) will not be discussed in this paper. Meanwhile, solution (2) has drawbacks in lowered output power. As a result, the main target of this paper is to achieve a flattened phase response for the load resonator $Z_{L,\omega}$.

It has to be mentioned that, the analysis shown in this section is based on a linear and simplified model of the ILFD. There is a complete nonlinear analysis that provides a more accurate prediction of the LR for ILFDs with a high-order load resonator in [25].

B. Transformer-Based High-Order Resonators

A low- Q LC-tank [Fig. 3(c)] has been first used in the injection-locked oscillator by Chan and Long [26] and a 56–65 GHz injection-locked frequency tripler was presented. However, a low- Q LC-tank faces start-up issues and more bias

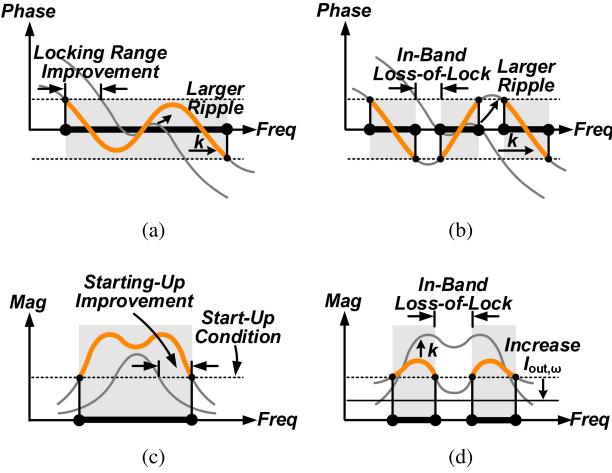


Fig. 6. Analysis on LR improvement based on the selection of coupling factor k . (a) Larger k will improve the LR due to larger phase ripple. (b) In-band loss-of-lock phenomena will occur as k getting even larger. (c) Fourth-order resonator is able to relax the start-up issue. (d) Larger $I_{\text{out},\omega}$ is needed to suppress the magnitude valley due to large k .

current is needed to sustain oscillating. On the other hand, the phase response for the low- Q LC -tank is not flattened enough, which drives us to find a better solution.

High-order transformer-based resonators are often used for wideband applications [27]–[32]. And in [31] and [32], the high-order transformer-based resonators have been used in the injection-locked frequency multipliers (ILFM) and achieved a good LR. Regarding with the ILFD, the high-order resonator shows a phase ripple around the center frequency and offers a much better LR [Fig. 3(d)].

In this design, we use a fourth-order transformer-based resonator to form the ILFD as shown in Fig. 4. The magnitude and phase response can be found in [31] and [32] and is not repeated hereafter. To get an insight on how the transformer-based fourth-order resonator improves the LR, simulations are performed with a comparison between the fourth-order resonators and the LC -tank (Fig. 5). As the phase response shown in Fig. 5(a), the LR can be improved significantly due to the phase ripple compared with the LC -tank, which means that a fourth-order resonator can be a better solution for ILFD.

A larger ripple will occur when the coupling factor k moves up, as shown in Figs. 5(a) and 6(a). This inspires us to find larger k to achieve a larger LR. However, when k is larger than a certain value, the ripple may move beyond $\angle Z_{L,\omega(\max)}$ [Fig. 6(b)], and an in-band loss-of-lock phenomenon will occur. This phenomenon may cause locking failure in a wideband PLL design and must be avoided. Thus, k has its maximum value to avoid in-band loss of lock.

The same result can be found when analyzing the magnitude response. Because the ILFD must work under oscillating status, the loop gain of the core oscillator [a loop through the adder, load resonator $Z_{L,\omega}$, and the cross-coupled pair g_m , as shown in Fig. 2(a)] must be above 1

$$g_m |Z_{L,\omega}| \geq 1. \quad (10)$$

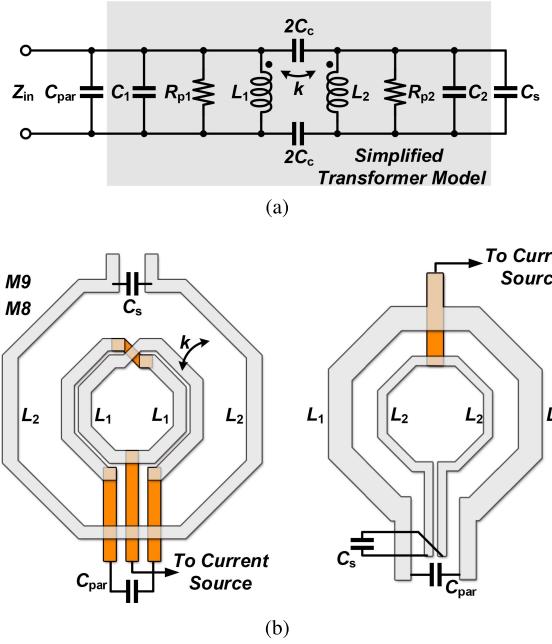


Fig. 7. (a) Equivalent resonator model based on the simplified transformer model in the DM. The parasitic capacitor from the cross-coupled pair C_{par} and the secondary tuning capacitor C_s is used for tuning. (b) Two kinds of transformer layout implementation.

This result shows that when the size of the cross-coupled pair and the bias current is chosen, the magnitude resonator must be large enough to sustain oscillating. Also, we can plot a line that equals to $1/g_m$ on the magnitude curve to judge the start-up condition [Fig. 6(c)]. From Figs. 5(b) and 6(c), moderate k can relax the start-up issue compared with the LC -tank, and a better LR is performed. However, as shown in Fig. 6(d), when k becomes even larger, the ILFD under some in-band frequencies will stop oscillating. This problem can be solved by using larger g_m to relax the start-up condition, which needs to increase the parasitics (increase the size of the cross-coupled pair) or increase the power consumption.

There is a slight difference between the ILFD and the ILFM in [31] and [32]. In [31] and [32], the injection current is low, which means that the maximum available ϕ is quite small. Therefore, the phase ripple in the ILFM must be controlled to a very small value to avoid the in-band loss-of-lock phenomenon. And in [31], a “phase plateau” is chosen in the phase response. However, in the ILFD, ϕ_{\max} is much larger (around 30° through simulation) and larger phase ripple can be applied without such concern.

Thanks to large ϕ_{\max} generated in the ILFD, there is no need of calibration which is applied in [31]. In this design, the phase ripple is designed less than 15° , which achieves a margin of more than 10° compared with ϕ_{\max} . Thus, the proposed ILFD still has a good performance under PVT variations even without any calibration.

C. Transformer-Based ILFD Synthesis

The key point in designing the transformer-based high-order ILFD is to choose k that can maximize the LR but avoid the

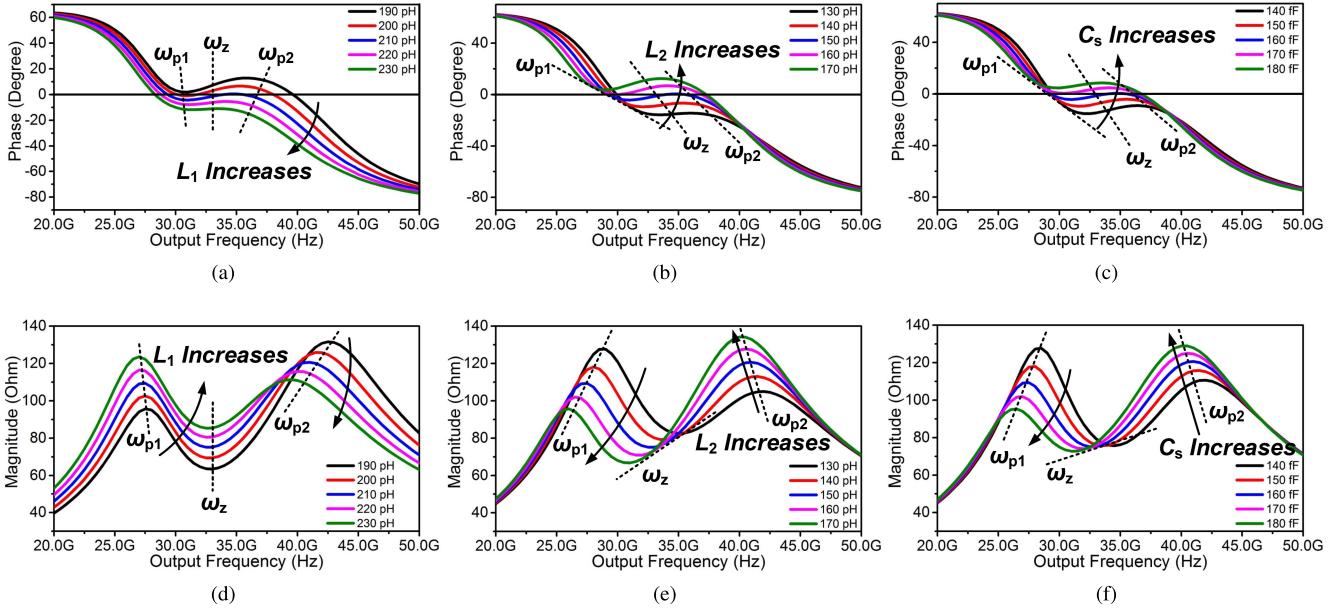


Fig. 8. Magnitude and phase response under the effect of L_1 , L_2 , and C_s (the effect of k is plotted in Fig. 5). Phase response with different values of (a) L_1 , (b) L_2 , and (c) C_s . Magnitude response with different values of (d) L_1 , (e) L_2 , and (f) C_s .

in-band loss-of-lock phenomena. According to the theoretical analysis of the LR, the first thing is to find $\angle Z_{L,\omega(\max)}$ under the minimum available injection power. From (8) and (9), $\angle Z_{L,\omega(\max)}$ is inversely proportional to the oscillating current $I_{\text{out},\omega}$ and proportional to the mixing current $I_{\text{mix},\omega}$, which are both strongly affected by the output voltage amplitude. This makes $\angle Z_{L,\omega(\max)}$ difficult to be calculated accurately. Fortunately, the ripple of the resonator phase response needs to be strictly within the boundary set by $\angle Z_{L,\omega(\max)}$ to support PVT variations, so that a large margin is needed and an accurate $\angle Z_{L,\omega(\max)}$ value is not very important to design the ILFD.

A conventional ILFD [Fig. 2(b)] circuit can be used to find $\angle Z_{L,\omega(\max)}$ by simulation. First, optimize the injection transistor M_{inj} using the method given in [18]. Then, set the cross-coupled pair and the load inductor to make the ILFD oscillate at the target frequency. At the same time, reduce the power consumption by adjusting the tail current source but make the ILFD remain oscillating, and this will not only save power but also reduce the oscillating current $I_{\text{out},\omega}$ to increase the LR according to (8). Finally, simulate the ILFD with the minimum available injection power and calculate the $\angle Z_{L,\omega(\max)}$ from the simulated $I_{\text{out},\omega}$ and $I_{\text{mix},\omega}$. In this design example, the calculated $\angle Z_{L,\omega(\max)}$ is 29.6°.

The next thing is to design the transformer. Fig. 7(a) gives the equivalent resonator model using the simplified differential mode (DM) transformer model [28] and neglects the substrate loss. Here, L_1 and L_2 are the inductance of each coil, C_1 and C_2 are the parasitic capacitors of the transformer, R_{p1} and R_{p2} are the equivalent parallel resistors that represent the loss of the transformer, and C_c represents the electric coupling of the two coils. As shown in [32], a larger inductance of the transformer may receive a larger magnitude of the impedance at a cost of a lower capacitance for the same tuning

frequency, which will consume less power. Thus, C_s is used here to tune the second coil, while the first coil is tuned by the parasitic capacitor C_{par} , which is generated from the cross-coupled pair, the injection transistor, and the output buffer. The target here is to find the optimum value of L_1 , L_2 , and k and then get its layout implementation. This can be done in three steps and shown in the following.

First, calculate the total parasitic capacitance C_{par} of the active devices from the ILFD circuit models and set up the equivalent resonator model shown in Fig. 7(a) in the simulator with L_1 , L_2 , k , and C_s as variables.

Next, tune these four variables in the simulator and find the optimum phase and magnitude response. Fig. 8 shows the effect of L_1 , L_2 , and C_s , while the effect of k is in Fig. 5. There are three important frequency points that determine the shapes of phase and magnitude response of the fourth-order resonator, ω_{p1} , ω_{p2} , and ω_z ,¹ as shown in Fig. 8. Four interesting things can be observed in Fig. 8.

- 1) The position of ω_z is almost not influenced by L_1 while changing by tuning L_2 and C_s .
- 2) The positions of ω_{p1} and ω_{p2} changed in the same direction with ω_z . In other words, when ω_z moves to a higher frequency as the L_1 , L_2 , and C_s are tuned, ω_{p1} and ω_{p2} also moves to a higher frequency.
- 3) When increasing L_1 , the phase and magnitude at ω_{p1} move to a higher value, while they move to a lower value at ω_{p2} . The influence from L_2 and C_s is opposite.
- 4) The influence from L_2 and C_s is almost the same.

¹These three frequency points are the poles (ω_{p1} and ω_{p2}) and zero (ω_z) in the transfer function of the resonator. The transfer function has been derived in [31] and [32] and is not shown in this paper. This paper only wants to give an intuitive guideline to optimize the fourth-order resonator and all the design procedures can be derived from simulation.

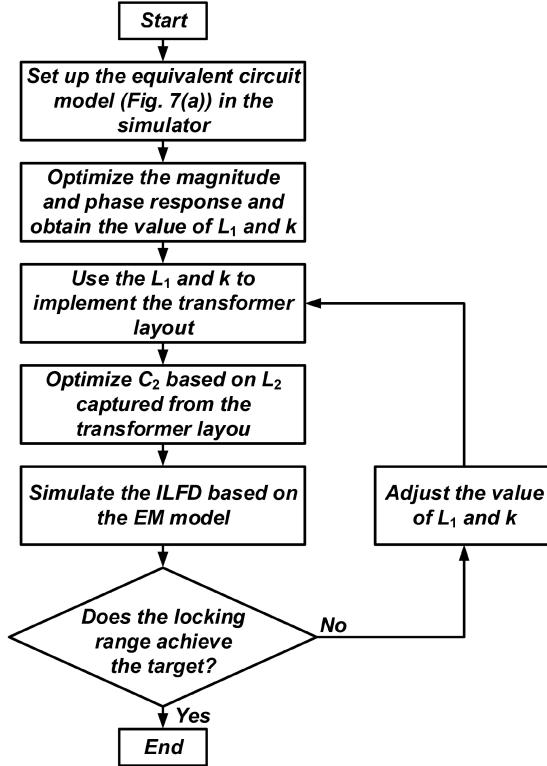


Fig. 9. Flowchart of the proposed ILFD synthesis procedure.

k influences the depth of the magnitude valley (ω_{p1} and ω_{p2} move far from the valley as k increases) from Fig. 5 and can be considered later. From these observations, we can set ω_z by tuning L_2 and C_s in the simulator and tune L_1 to make the phase ripple around 0° . However, these tuned L_1 and L_2 values may not be easy for layout implementation. Fortunately, L_2 and C_s have the same influence on the phase response. Therefore, we can first choose the value of L_1 and k to set the ripple, then find the value of L_2 from the transformer layout implementation, and tune C_s to obtain the targeted ω_z . Taking advantage of choosing L_2 flexibly, the transformer layout is able to be implemented easily.

Finally, using the value of L_1 , k , and L_2 from the layout implementation, tune C_s to obtain the targeted phase response. If the phase response cannot be tuned to the wanted shape, then adjust L_1 and k slightly and do some iterations.

There needs some iterations when putting the transformer into the whole circuit due to the inaccuracy of the calculated $\angle Z_{L,\omega(\max)}$. And some fine adjustment on L_1 and k is needed. Fig. 9 shows the design and optimization procedure of the proposed transformer-based ILFD.

A design example is given here for a frequency around 50 GHz. With the transistors optimized through [18], $\angle Z_{L,\omega(\max)}$ is 29.6° and the parasitic capacitance is 80 fF according to the simulation. L_1 can be set to 200 pH as our first try. k is mainly around 0.2–0.5 in the wideband design, so L_2 can be set to around 180 pH, which makes the transformer layout possible. Set up the model shown in Fig. 7(a) in the simulator and tune k and C_s . We can get a series phase curve as shown in Fig. 8 and then choose the optimum values of

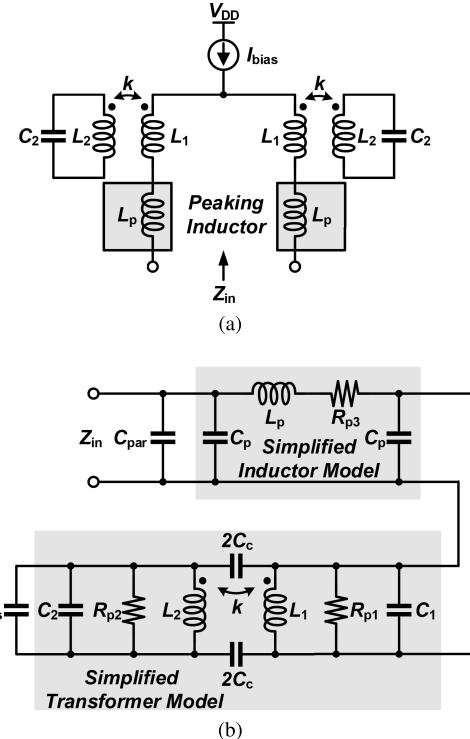


Fig. 10. Boosting $|Z_{L,\omega}|$ by inserting a peaking inductor L_p . (a) Load resonator with peaking inductor. (b) Simplified equivalent circuit of the load resonator with peaking inductor.

k and C_s that are 0.4 and 150 fF in this design. It is very lucky that the first try of L_1 achieves a good result, and we can set another value of L_1 through the first try if we do not have such a luck. Because all of the optimizations are based on the simplified circuit model, this optimization can be done very quickly even though there need some iterations. Finally, we can use the value of L_1 , k , and L_2 to implement the layout of the transformer and finish the design by simulating the ILFD based on the electromagnetic model.

III. POWER CONSUMPTION REDUCTION

Low power consumption is the most attractive property for the ILFD compared with other types of dividers [5]–[7], [10], and this section discusses some techniques to further reduce the power consumption.

A. Inductive Gain Peaking

In order to make the ILFD to oscillate, a large dc current is needed to form large g_m of the cross-coupled pair, which is used to cancel the loss in the load resonator. According to Barkhausen's criteria (10), larger $|Z_{L,\omega}|$ causes less requirement on g_m , which would save power. And this property is already used in Section II. Now, we need to find a way to further increase $|Z_{L,\omega}|$.

Additional inductor is implemented in series into the core resonator as L_p shown in Fig. 10(a). The input impedance can be obtained as

$$Z_{in} = j\omega L_p + Z_{L,\omega}. \quad (11)$$

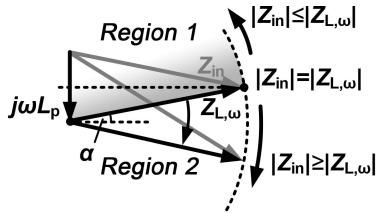


Fig. 11. Phasor diagram of the input impedance for the proposed inductive gain peaking.

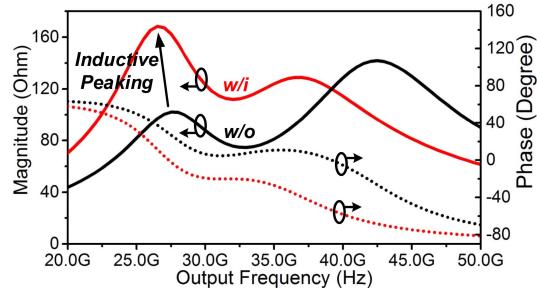


Fig. 12. Influence on the input impedance with or without peaking inductor.

Due to the complex impedance nature, the magnitude of the input impedance can be judged based on the phasor diagram, which is shown in Fig. 11. $Z_{L,\omega}$ shows a real impedance at the self-oscillating frequency, which is at the right angle with the peaking inductor L_p . As the operating frequency moves beyond the self-oscillating frequency, the load resonator $Z_{L,\omega}$ will move to a complex value and the vector $Z_{L,\omega}$ in Fig. 11 may rotate as the operating frequency is changed. There are two regions in Fig. 11 when the vector $Z_{L,\omega}$ rotates. In Region 1, $|Z_{in}|$ gets smaller than $|Z_{L,\omega}|$, while in Region 2, $|Z_{in}|$ gets larger than $|Z_{L,\omega}|$. Therefore, in order to boost the input impedance of the load resonator, we want the achieved $|Z_{in}|$ to be larger than the conventional $|Z_{L,\omega}|$. Fortunately, the ILFD works as the $\angle Z_{L,\omega}$ stays within a narrow boundary. Otherwise, it fails to lock. Therefore, the vector $Z_{L,\omega}$ may stay in Region 2 mostly and the peaking inductor will always improve the magnitude of the load impedance.

Another issue is that the peaking inductor must not influence the excellent characteristics generated by the high-order resonator. An equivalent circuit model of the peaking inductor together with the transformer is used to justify this matter and shown in Fig. 10(b). Also, the simulation of the load impedance is used with or without the peaking inductor. Fig. 12 shows the simulation results and the magnitude is increased at low frequencies. The impedance curves have similar shapes, while the flattened phase response has disappeared, as shown in Fig. 12. The reason for this phenomena is the phase of the inductor is 90° and when the inductor is in series with $Z_{L,\omega}$, the phase of the total impedance will move to a negative value, as shown in Fig. 11. However, this phase shift can be easily removed by retuning the capacitor of the transformer and the peaking inductor will not influence the LR of the ILFD.

However, the peaking inductor moves the ILFD to a lower operating frequency and shows a less phase ripple in Fig. 12.

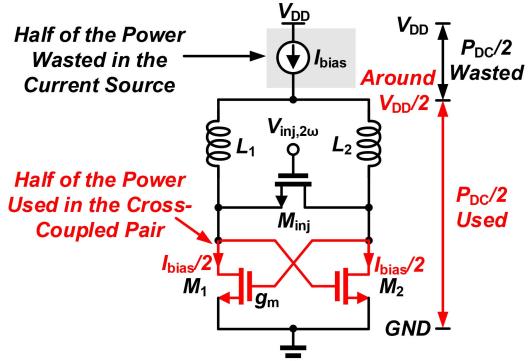


Fig. 13. Analysis on power dissipations in the current-biased ILFD.

This problem can be solved by re-adjusting the transformer. To some extent, the peaking inductor together with the load transformer can be seen as a transformer that combines the two components. The combining transformer has a larger primary inductance but a lower coupling factor. Therefore, it seems that the ILFD with the peaking inductor shows no difference with the transformer-based ILFD. The conclusion is true, no doubt, but there are some benefits when using the peaking inductor separately. First, the transformer will have a larger coupling factor when using the separated peaking inductor, and the layout implementation can be easier due to k reaching to about 0.4–0.5. Second, when using the peaking inductor, the total resonator works more like a distributed network, and the influence of the parasitic capacitances will be lowered. This means that a larger total inductance can be used in the load resonator to sustain the same operating frequency and save power.

B. Tail Current Source

The tail current source shows a great influence on the performance of oscillators, especially the phase noise [33], [34]. In [33], the tail current source with high output resistance improves the phase noise greatly, while in [34], removing the tail current source also achieves interesting performance. Therefore, the usefulness of the tail current source strongly depends on the design. Then is the tail current source a friend or a foe for the ILFD? For the injection-locked oscillators, the phase noise performance depends mostly on the injection signal and the LR [24], [35]. Thus, the tail current source seems no use in the ILFD and can be removed.

Considering an ILFD that uses a tail current source for current biasing, the dc voltage at the drain node of the cross-coupled pair is around half of the supply. Meanwhile, the current flowing through the tail current source is equal to the total current flowing through the cross-coupled pair, which means that only half of the dc power is used to generate negative transconductance and another part is wasted in the tail current source and shown in Fig. 13. By removing the tail current source, without increasing dc current, the voltage headroom can be saved as well as power consumptions. In order to save the power consumption, the tail current source can be removed so that a lower supply voltage can be applied while the dc current remains unchanged.

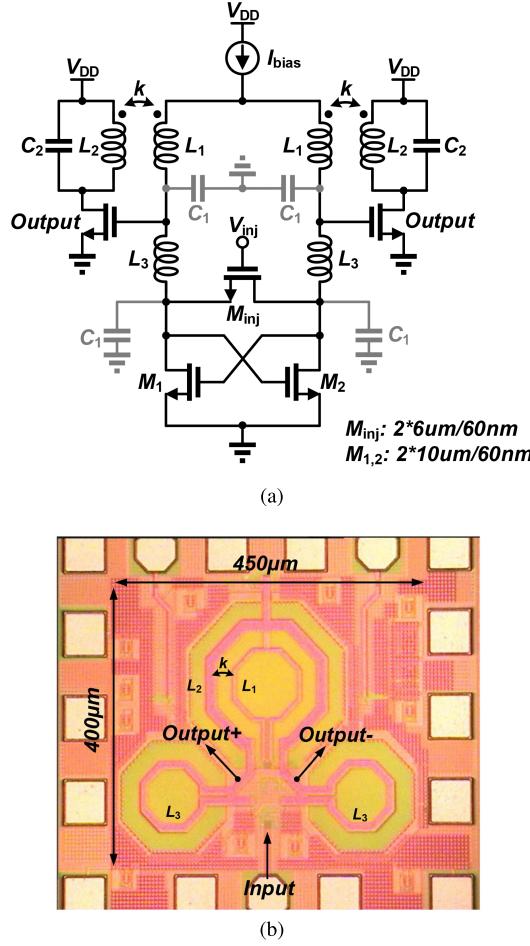


Fig. 14. Circuit implementation of chip one. (a) Schematic. (b) Die photograph.

However, eliminating the tail current source may drive the ILFD into voltage bias condition and variations in supply voltage may influence the performance of the ILFD. To verify this issue, we use the measured results that show no influence of eliminating the tail current source. The comparison of the measured phase noise performance based on the tail current source will be shown in Section IV.

IV. CIRCUIT IMPLEMENTATIONS AND MEASUREMENT RESULTS

A. Chip One: With Tail Current Source

The first chip is fabricated in the 65-nm CMOS process. The tail current source is applied in this ILFD to work under the 1-V supply for system considerations. The schematic of the first chip is plotted in Fig. 14(a) with a transformer-based fourth-order resonator and a peaking inductor. The input signal is injected directly into node \$V_{\text{inj}}\$ through a ground-signal-ground (GSG) pad. Using the design method shown in Section II-C, the transformer is designed as \$k = 0.32\$, \$L_1 = 210 \mu\text{H}\$, and \$L_2 = 180 \mu\text{H}\$, and the transformer is implemented using the layout shown on the right of Fig. 7(b). The simulated peak-to-peak voltage swing on the cross-coupled pair is from 340 to 660 mV_{pp}. Buffers are connected to the transformer

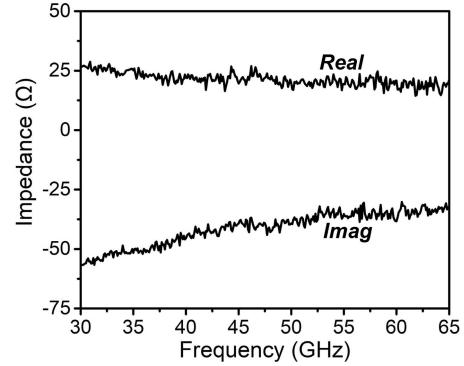


Fig. 15. Measured input impedance of the ILFD.

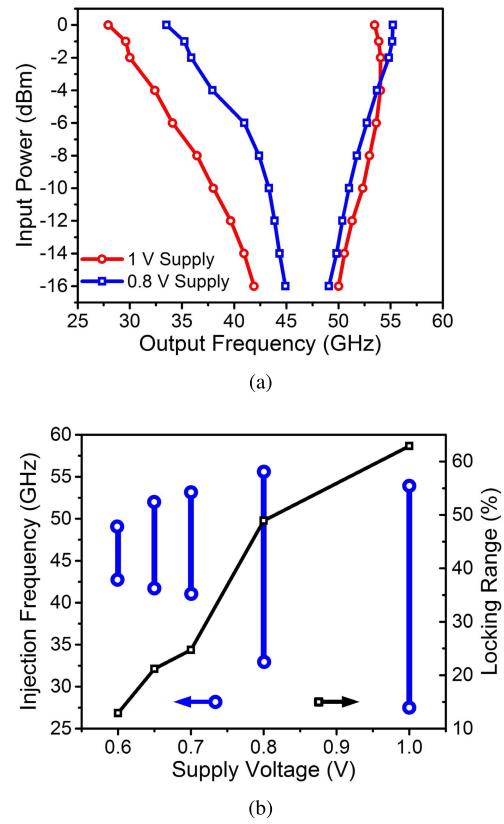
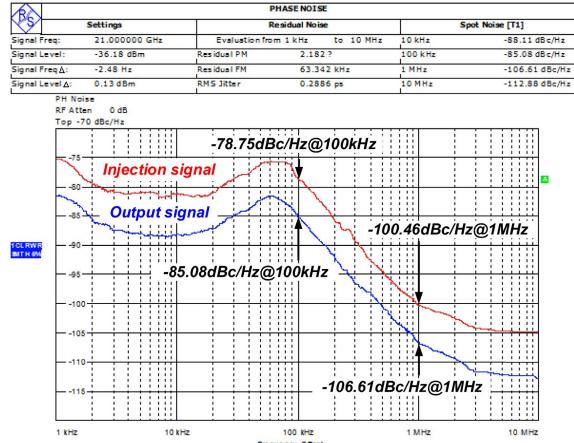


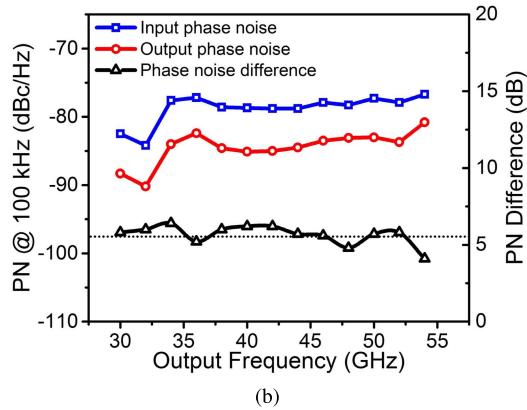
Fig. 16. (a) Measured input sensitivity curve of chip one under 1- and 0.8-V supply. (b) Measured LR under different supply voltages.

[the output node plotted in the chip photograph in Fig. 14(b)] to decrease the parasitic influences and a buffer feedback architecture [36] is proposed and the simulated output voltage swing is from 32 to 60 mV_{pp} with a 50- Ω load. The die photograph of chip one is shown in Fig. 14(b) and the core area is 450 $\mu\text{m} \times 400 \mu\text{m}$.

The injection signal is generated from an N5247 Keysight PNA, and a GSG probe is used for signal injection. The output is captured with a GSG probe and an FSU67 R&S Spectrum Analyzer. The insertion loss of the coaxial cable and the GSG probe is around 7 dB and it has been de-embedded. Fig. 15 shows the measured input impedance of the ILFD. The input sensitivity curve is measured and plotted in Fig. 16(a) under both 0.8- and 1-V supply. With 0-dBm injection signal



(a)

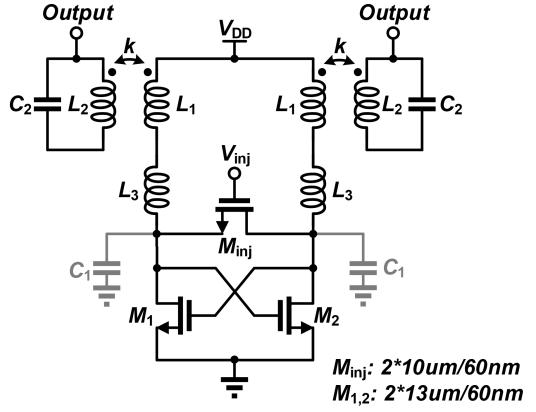


(b)

Fig. 17. (a) Measured phase noise plot of chip one at 42-GHz input frequency. (b) Measured phase noise difference between input and output of the ILFD at different frequencies.

and 1-V supply voltage, the first ILFD achieves a LR up to 25.6 GHz (from 27.9 to 53.5 GHz, 62.9% of the center frequency) while consuming 5.8-mW power. When the supply voltage gets down to 0.8 V, the LR goes to 21.7 GHz (from 33.5 to 55.2 GHz, 48.9% of the center frequency) with 3.2-mW power consumption. For the low voltage consideration, the proposed ILFD can work at a supply voltage below 0.8 V and the LR with low supply voltages is shown in Fig. 16(b). The first ILFD with the tail current source can work even with a 0.65-V supply, with 9.9-GHz LR remaining (from 41.8 to 51.7 GHz, 21.2% of the center frequency). The voltage variation in chip one with tail current source gets worse than that in chip two. The reason is when the supply voltage gets lower, and the non-ideal current source meets lower voltage headroom and generates less current. This will decrease the transconductance in the cross-coupled pair and makes that the ILFD fails the gain condition.

Phase noise performances are also measured. Fig. 17(a) shows the measured phase noise with a 42-GHz, 0-dBm injection signal. The phase noise difference is about 6 dB even at 10-MHz offset. There are some points in the phase noise plot. The phase noise difference is larger than 6 dB, and this is caused by the error in the phase noise measurement using the Spectrum Analyzer. It has to be mentioned that,



(a)

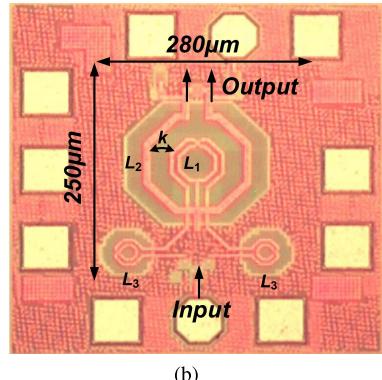


Fig. 18. Circuit implementation of chip two. (a) Schematic. (b) Die photograph.

when the offset frequency gets above 1 MHz, the noise floor of the Spectrum Analyzer becomes dominant. This makes the phase noise measurement inaccurate above 1-MHz offset [18]. Fig. 17(b) shows the input and output phase noise at 100-kHz offset with different injection frequencies of the whole band, and the phase noise differences are still about 6 dB at all frequencies with 2-dB degradation at 54 GHz, which is the edge of the LR.

B. Chip Two: Without Tail Current Source

The second chip is also fabricated in a 65-nm CMOS process. The tail current source is removed to save power and a 0.42-V supply is applied. The schematic of chip two is plotted in Fig. 18(a) with a similar design consideration in chip one. Here, the buffer feedback architecture is removed and the output buffers are connected to the secondary coil of the transformer [the output node plotted in the chip photograph in Fig. 18(b)]. To save the chip area, the primary coil of the transformer is designed with a double-coil inductor, and the transformer is implemented using the layout shown on the left of Fig. 7(b). The simulated voltage swing on the cross-coupled pair is similar to that in chip one, because the bias current and the load impedance are almost the same. The die photograph is shown in Fig. 18(b) and the core area is 280 μ m \times 250 μ m.

The measurement setup is the same with chip one. The input sensitivity curve is plotted in Fig. 19 with the supply voltage

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Ref.	Process	Topology	Supply Voltage (V)	Operation Frequency (GHz)	Locking Range @ 0 dBm (GHz)	PN Diff. (dBc/Hz)		Power (mW)	Core Area (mm^2)	FoM [†] (GHz/mW)
						100k	1M			
A. Ghilioni [6]	32nm	CML (Divide-by-4)	1	14-70*	32 (60%)	12	12	4.8	0.001	6.67
Y. Lin [10]	65nm	Miller	0.4	36.8-59.2‡	22.4‡(46.7%)	6	N/A	1.6	0.046§	14
W. Chen [13]	65nm	Forward-Body Bias	1	25-53.6	28.6 (72.8%)	6	10#	12.1	0.105§	2.36
T. Luo [14]	90nm	Dual Injection	0.8	38.8-51.2‡	12.4‡(27.6%)	N/A	N/A	0.8	0.192§	15.5
Y. Chao [18]	65nm	Frequency Tracking	0.8	53.4-79.4	26 (39.2%)	6#	6#	2.9	0.126	8.97
K. Takatsu [19]	65nm	Multi-Order	1.2	48.5-62.9	14.4 (25.9%)	N/A	N/A	1.65	0.125§	8.73
A. Imani [21]	130nm SiGe	Distributed	1.15	35-59.5*	18.5 (36.8%)	6	0#	3.8	0.046	4.9
This work #1	65nm	4th-Order	1	27.9-53.5	25.6 (62.9%)	6	6	5.8	0.18	4.41
This work #2		Transformer-Based	0.42	32.3-61.9	29.6 (62.7%)	6	6	1.2	0.07	24.7

* The divider is tuned to achieve this operation frequency, and the highest frequency band is selected in locking range comparison.

Captured from the measurement phase noise plot.

§ Captured from the chip photograph.

† FoM=locking range/power consumption (GHz/mW).

‡ The operation frequency and the locking range are captured from the measured input sensitivity curve under 0 dBm injection condition.

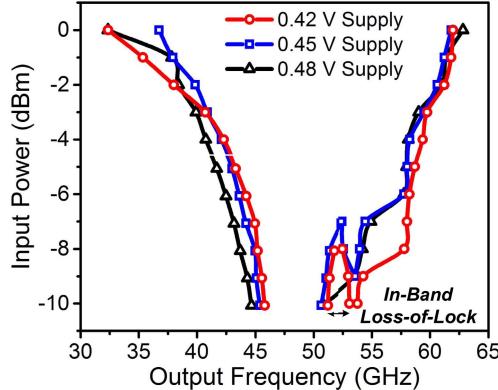
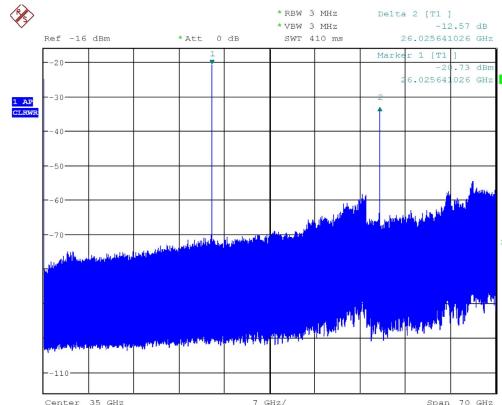


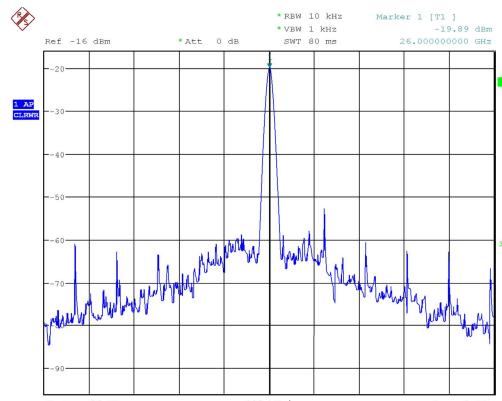
Fig. 19. Measured input sensitivity curve of chip two under 0.42-, 0.45-, and 0.48-V supply.

of 0.42, 0.45, and 0.48 V. The LR of chip two is 29.6 GHz (from 32.3 to 61.9 GHz, 62.7% of the center frequency) and consumes only 1.2 mW under 0.42-V supply. The supply voltage variation is an important property in this ILFD due to the removal of the tail current source, which makes the ILFD a voltage biasing circuit. The measured LR of 0.45-V supply is 25.1 GHz (from 36.7 to 61.8 GHz, 51.0% of the center frequency), and the LR of 0.48-V supply is 30.4 GHz (from 32.4 to 62.8 GHz, 63.9% of the center frequency). These results show that the operating frequencies are less influenced by the supply variation, and make the removal of the tail current source a good solution to save power. Meanwhile, according to the input sensitivity curve shown in Fig. 19, the in-band loss of lock appears under 0.42- and 0.45-V supply with injection power lower than -7 dBm. As mentioned in Section II-B, this phenomenon is caused by the phase ripple moving beyond $\angle Z_{L,\omega(\max)}$ at the low injection power condition.

Fig. 20 shows the measured output spectrum when the ILFD is locked at 26 GHz. There are spurs shown in Fig. 20(b) and these spurs are generated from the injection signal



(a)



(b)

Fig. 20. Measured output spectrum under 52-GHz, 0-dBm injection signal. (a) Full span settings in Spectrum Analyzer. (b) 1-MHz span and 10-kHz resolution bandwidth (RBW).

(N5247 Keysight PNA). Phase noise performances are shown in Fig. 21 with a 38-GHz, 0-dBm injection signal and a 62-GHz, 0-dBm injection signal. The phase noise difference is also about 6 dB at the offset frequencies from

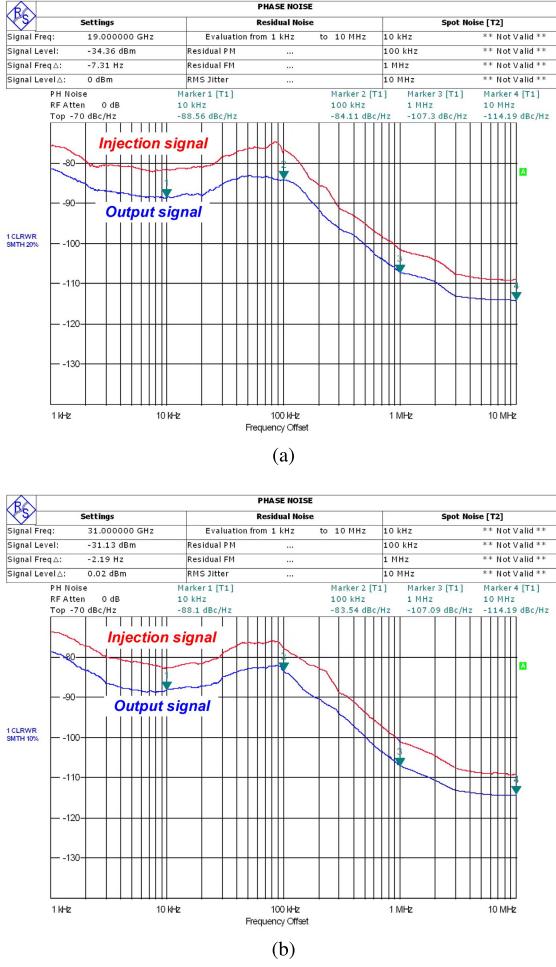


Fig. 21. Measured phase noise plot of chip two at (a) 38-GHz, 0-dBm injection signal and (b) 62-GHz, 0-dBm injection signal.

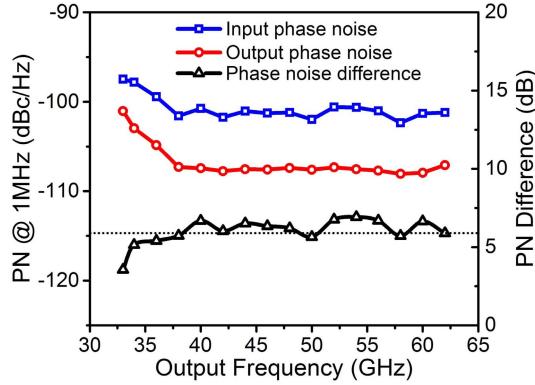


Fig. 22. Measured phase noise difference between input and output of the ILFD at different frequencies.

10 kHz to 10 MHz. The phase noise performance in the whole operating band is measured, and Fig. 22 shows the input and output phase noise at 1-MHz offset. The phase noise differences are about 6 dB, while 3-dB degradation is found at 33 GHz which is also the edge of the LR.

Table I compares the measured performance of the proposed two ILFDs with the state-of-the-art ILFDs. The proposed transformer-based ILFDs achieve much larger LR and the best FoM. The FoMs in [10] and [14] are also very high, because

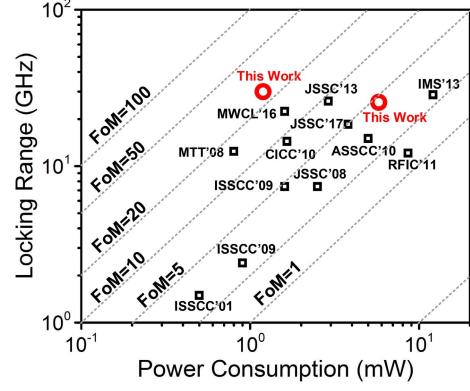


Fig. 23. FoM comparison.

both of them eliminate the tail current source, as mentioned in Section III-B. Therefore, they get benefits from reducing the power consumption greatly. Fig. 23 shows the FoM compared with the prior arts.

V. CONCLUSION

The LR limitation of the ILFD is discussed to find the solutions on improving the LR. By flattening the phase response of the load resonator, the LR is improved a lot with the help of the transformer-based high-order resonator. We discuss the design procedure of the transformer-based ILFD, which will decrease the cost of a high-order transformer design and save time. Furthermore, to reduce the power consumption, an inductive gain peaking technique is proposed with a discussion on the use of the tail current source. A better solution to save power is to remove the tail current source and the measurement results show a good improvement.

Two chips using the proposed transformer-based resonator are implemented. Chip one uses the tail current source for current biasing and measures a LR of 62.9% from 27.9 to 53.5 GHz with 1-V supply. As the supply voltage going down to 0.8 V, the LR can remain 48.9% from 33.5 to 55.2 GHz. This chip can work in low-voltage applications with a 21.1% LR at 0.65-V supply and consume only 1.16-mW power. The second chip removes the tail current source and measures a LR of 62.7% from 32.3 to 61.9 GHz with 0.42-V supply. This chip suffers little influence on voltage variation, which can work even under 0.48-V supply. The second chip consumes only 1.2-mW power, which corresponds to an FoM of 24.7 GHz/mW. The phase noise performances are measured for these two chips, and 6-dB phase noise differences are achieved, which are close to the theoretical value. To the best of our knowledge, the proposed ILFDs achieve the best FoM among all the state-of-the-art millimeter-wave ILFDs ever reported.

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