

A Time-Interleaved 12-b 270-MS/s SAR ADC With Virtual-Timing-Reference Timing-Skew Calibration Scheme

Hyun-Wook Kang, Hyeok-Ki Hong, Wan Kim, and Seung-Tak Ryu[✉], *Senior Member, IEEE*

Abstract—This paper presents a two-way time-interleaved (TI) 12-b 270-MS/s successive approximation register (SAR) analog-to-digital converter (ADC) with a virtual-timing-reference timing-skew calibration scheme, in which the timing-skew calibration spurs present in conventional calibration schemes are effectively suppressed with the deferred reference sampling edge. The proposed design runs in a true background mode of operation, whose accuracy is independent of the statistics and the wide-sense stationary property of the input. A 12-b 270-MS/s prototype ADC with the on-chip timing-skew and offset calibration circuits is fabricated in a 40-nm CMOS process, where the timing-skew calibration circuits occupy only 9.7% of the total core area, showing the simplicity and ease of integration of the calibration algorithm even in large-scale TI ADCs. The prototype achieves a peak SNDR of 60.2 dB and a Nyquist-rate SNDR of 59.7 dB while consuming 4.5 mW from a 0.9-V supply, which then results in a Walden FoM of 21.1 fJ/conversion-step.

Index Terms—Calibration, delay control, time-interleaved (TI) analog-to-digital converter (ADC), timing-skew, virtual-timing reference (VTR).

I. INTRODUCTION

ADVANCES in modern communication systems, such as ultra-wideband radios, software-defined radios, and WLAN standards, have driven the demand for high-speed, high-resolution, and low-power analog-to-digital converters (ADCs) [1], [2]. Pipelined ADCs have traditionally met and responded to those technical needs with their innate high-throughput data rate and highly expandable resolution, but they generally suffer from high-power consumption, wideband design difficulties, and lowered gain from process scaling in operational amplifiers. While favoring process scaling with digital friendly architectures, successive approximation register (SAR) ADCs, on the other hand, have limitations in terms of conversion speed due to the cyclic operational nature. As a means to accelerate the conversion rate, time-interleaving (TI)

Manuscript received December 29, 2017; revised March 15, 2018 and May 21, 2018; accepted May 23, 2018. Date of publication June 21, 2018; date of current version August 27, 2018. This paper was approved by Associate Editor Jeffrey Gealow. This work was supported by the Civil-Military Technology Cooperation Program of the Republic of Korea. (*Corresponding author: Seung-Tak Ryu*)

H.-W. Kang and S.-T. Ryu are with the School of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon 34141, South Korea (e-mail: stryu@kaist.ac.kr).

H.-K. Hong and W. Kim were with the School of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon 34141, South Korea. They are now with Samsung Electronics, Suwon 16677, South Korea.

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2018.2843360

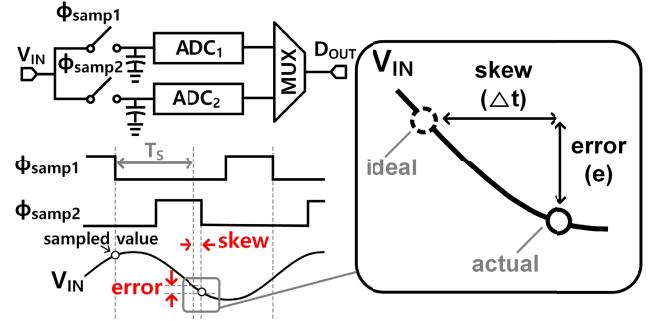


Fig. 1. Timing-skews and the corresponding errors in a TI architecture.

architectures have drawn a great deal of attention for their power efficiency at high speeds [3]. TI architectures, however, suffer greatly from their own artifacts, such as channel offset, gain, and sampling timing mismatches (or timing-skews) [4]. Apart from offset and gain mismatches, whose powers are constant over changes in the input frequency and the conversion rate, and thereby making them relatively straightforward to deal with in the digital domain, timing-skews exhibit a significant dependence on the input frequency. Fig. 1 shows how timing-skews introduce sampling errors in a TI architecture. The amount of error induced by the timing-skew from a single-tone sinusoidal input, $V_{IN}(t)$, with an amplitude A_{IN} can be expressed as [5]

$$e(t) \approx \delta V_{IN}(t)/dt \cdot \Delta t \quad (1)$$

$$= \omega_{IN} \cdot A_{IN} \cdot \cos(\omega_{IN} t) \cdot \Delta t \quad (2)$$

where Δt , e , and ω_{IN} represent the timing-skew, the corresponding voltage error, and the angular frequency of the input, respectively. As a sinusoidal signal, we can express the power of e to be (f_{IN} denotes the input frequency)

$$PSKEW = (4 \cdot \pi^2 \cdot f_{IN}^2 \cdot A_{IN}^2 \cdot \Delta t^2)/2. \quad (3)$$

Noting that the signal power of the input is equal to $A_{IN}^2/2$, the power ratio of the input signal to the skew tones can be expressed as

$$R_{\text{signal-to-SKEW}} = 1/(4 \cdot \pi^2 \cdot f_{IN}^2 \cdot \Delta t^2). \quad (4)$$

As shown in (3), the skew-induced error power grows quadratic as the input frequency increases, for a fixed value of skew Δt ; thus, it makes high-speed TI designs burdensome. Because of this phenomenon, ADCs with high-input frequencies require a timing-skew calibration scheme.

TABLE I
COMPARISON OF TIMING-SKEW CALIBRATION HARDWARE OVERHEADS

	Derivative-based Stepanovic [9]	Sign-equality-based Kang [10]
# of additional ADCs for timing-skew calibration	2 (Delayed ADC & REF-ADC)	1 (REF-ADC)
Resolution of additional ADC(s)	Full resolution of main channels	Low
Processing digital hardware	2-multipliers (full resolution of channels, comparable to 2-N-N full-adders where N is the resolution of main channels)	1-XOR gate & M-XOR and few AND gates (for "Inequality" block) where M is the resolution of REF-ADC
Cal. accuracy dependency on the (residual) offset and gain mismatches	Severely dependent	Nearly independent

With the growing interest in TI architectures, various timing-skew calibration schemes have been reported [3], [6]–[11].

The calibration algorithms proposed in [3], [7], and [8] make a good use of the autocorrelation property to mitigate timing-skews. Despite their advantages, those schemes impose strict requirements on the shape of the autocorrelation function and the statistics of the input as well as the premise of a wide-sense stationary input in which the calibration accuracy depends heavily on the number of samples. The number of samples for each skew analytic period should be large enough to make the input statistics relatively stationary over consecutive analysis periods [6], [9], [10]. These stringent requirements make them hard to operate in a true background mode with unknown inputs for certain applications where the statistics of the input readily change. Stepanovic and Nikolic [9] devised a way to calibrate skews on a sample-by-sample basis, rather than relying on the aggregated ADC output data and statistics. By employing a spare ADC to sample the input with a designed short time lag, the calibration scheme in [9] was able to find the instantaneous slope of the input, and thus the direction of skews, at any given calibration point. Disadvantages of such a calibration scheme include the changes in the ADC input load when the skew calibration is turned ON and OFF, and the complex calibration circuit blocks that occupy a relatively large part of the total core area [6], [10], [11]. In a similar derivative-based algorithm, the sign-equality-based (SEB) calibration algorithm in [10] eliminates the need for employing a delayed ADC channel to estimate the instantaneous slope of the input by taking the advantage of adjacent channel outputs, and it simplifies the calibration logic using only the sign bits to estimate the direction of skews. The hardware overheads in employing the SEB calibration in [10] are summarized and are compared to [9] in Table I.

Besides issues related to the calibration algorithms, a critical drawback of any timing-skew calibration scheme that uses an auxiliary ADC as a timing reference (REF-ADC) (see [7], [9], [10]) is that it is apt to introduce calibration spurs caused by the sampling kickbacks of those sampling the input at nearly the same time [6], as will be discussed in more detail in Section II-B. Stepanovic and Nikolic [9] employed a pseudorandom number generator (PRNG) to randomize the operating frequency of the REF-ADC. Such a randomized REF-ADC sampling scheme effectively blends

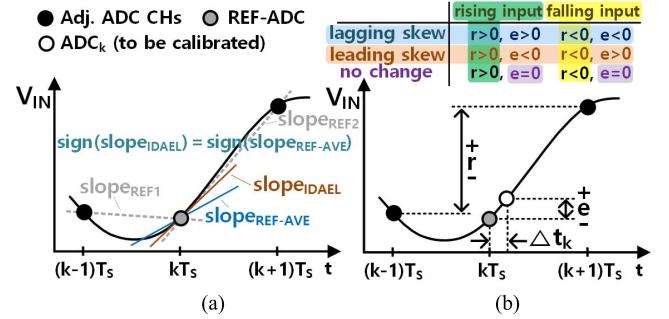


Fig. 2. Conceptual basis of the SEB timing-skew calibration algorithm. (a) Slope averaging and input derivative sign estimation. (b) Algorithmic operation in the digital domain [10].

and disperses the calibration spurs into noises and greatly improves the spurious-free dynamic range. However, because of such behavior, as is apparent, the noise floor increases and has no favorable influence on the overall performance in terms of SINAD and ENOB [12], [13]. In this paper, a virtual-timing-reference (VTR) timing-skew calibration scheme is proposed to defer the sampling edge of the REF-ADC in the actual time domain to prevent the sampling kickback from causing undesirable sampling errors in the main channels, while the REF-ADC samples preceding input values so as to form a virtual sampling edge of the REF-ADC as a clear timing reference for the calibration algorithm. In this way, the unwanted kickback from the REF-ADC is effectively deferred until channels sample the unhampered input.

A prototype two-way TI 12-b 270-MS/s SAR ADC was fabricated and tested to verify our concept. The remainder of this paper is organized as follows. Section II discusses the SEB timing-skew calibration algorithm with a few design concerns. Section III introduces the proposed algorithm in detail. Circuit implementations are discussed in Section IV, followed by presentation of the measurement results and the conclusion in Sections V and VI, respectively.

II. SIGN-EQUALITY-BASED TIMING-SKEW CALIBRATION AND DESIGN CONSIDERATIONS

As a foundation, the proposed design adapts some part of the SEB timing-skew calibration algorithm introduced in [10]. Fig. 2 shows the fundamentals of the algorithm in conceptual diagrams. Rather than using a supplementary ADC with a short artificial sampling clock skew to estimate the instantaneous slope of the input in [9], the SEB algorithm estimates the sign of the input derivative from the outputs of the adjacent sub-ADC channels and by averaging the two slopes, $slope_{REF1}$ and $slope_{REF2}$, as shown in Fig. 2(a), given that the dominant input spectrum power lies below the Nyquist frequency and that the input exhibits a finite slope detectable by the adjacent channels. Since the period T_s bears no meaningful information in the digital domain, the sign of the input derivative from the averaged reference slopes is extracted simply by subtracting two adjacent sub-ADC channel outputs [r in Fig. 2(b)] [10]. By comparing the sign-equality of r and e (the output difference between the REF-ADC and the channel to be calibrated), the algorithm can estimate whether the skew is leading or lagging behind the sampling

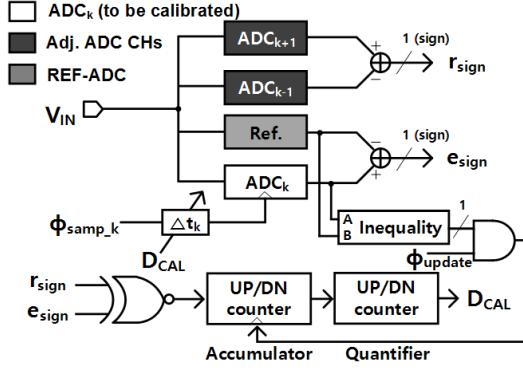


Fig. 3. Block diagram of the SEB timing-skew calibration algorithm [10].

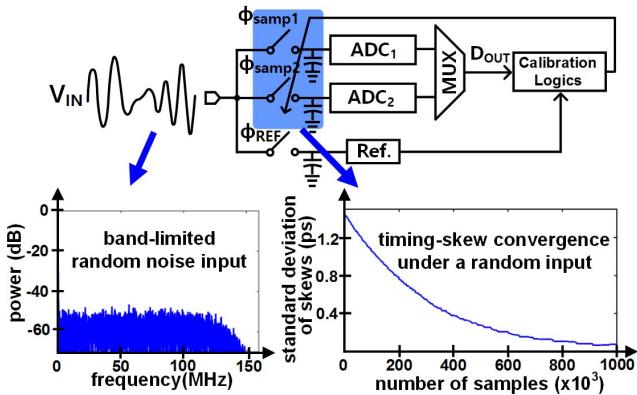


Fig. 4. Software simulated timing-skew calibration algorithm and its convergence with a band-limited random noise input (accumulation count = 32, calibration step size = 50 fs, resolution of REF-ADC = 6 b, and thermal noise power in the REF-ADC comparable to 5-LSB_{12b}).

edge of the REF-ADC. For instance, if both r and e are positive, it implies that the input is rising and that the sampling edge of the channel is lagging behind that of the REF-ADC; therefore, the sampling clock delay to the channel should be decreased. The opposite is true for unequal sign values in r and e . The algorithm makes no change in the delay control if the outputs of the REF-ADC and the channel are the same ($e = 0$), indicating that the skew direction cannot be discerned. Fig. 3 illustrates how the SEB algorithm detects the directions of skews in a block diagram. An XOR gate determines whether r_{sign} and e_{sign} are equal, and thus determines whether the skew is leading or lagging behind, while its skew directional value is accumulated using an up-down counter as a digital filter to block unwanted effects of noises, offset and gain mismatches, and initial skew-induced errors from aggravating the calibration accuracy [10]. The digitally filtered skew directional value is then quantified into digital values (D_{CAL}) through the quantifier, which then controls the digitally controlled delay line (DCDL) in each channel to adjust the delay to the sampling clock. Fig. 4 shows a software simulation exhibiting how the algorithm calibrates the timing-skew over time even under a Nyquist-rate band-limited random noise input, thereby verifying its independence from a wide-sense stationary input property. Note that the convergence speed is dependent on the designed accumulator

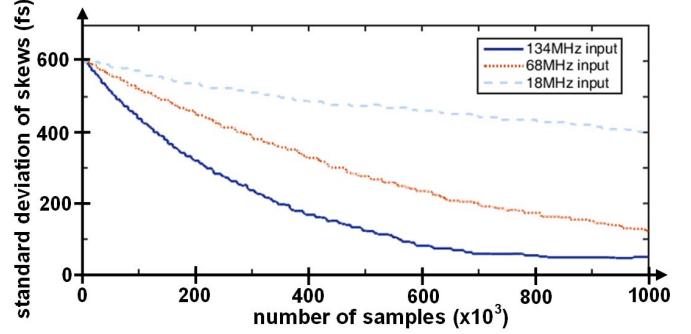


Fig. 5. Software simulated standard deviation of skews versus number of samples for various input frequencies (12-b 270-MS/s operations, calibration step size = 50 fs, resolution of REF-ADC = 6 b, and accumulation count = 32).

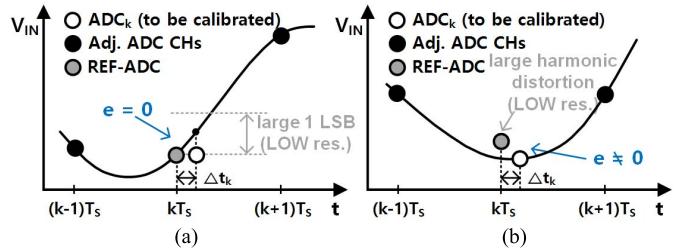


Fig. 6. Issues concerning the resolution of the REF-ADC. (a) Quantization step. (b) Harmonic distortions.

count, the calibration step size, the noise power, and the input frequency. The convergence curves over time for various input frequencies are shown in Fig. 5. For a high frequency input, the amount of error induced from a fixed value of skew is larger compared to slower inputs, and thus results in more frequent skew detections and faster calibration convergence. The convergence speed varies in relative proportion to the input frequency.

A. Concerns in Defining the Resolution of the REF-ADC

Despite the algorithmic simplicity of the SEB timing-skew calibration, a few factors should be taken care of concerning the resolution of the REF-ADC. To optimize the complexity and the overhead of the timing-skew calibration, the resolution of the REF-ADC should be minimized. Although the unwanted effects from noises, offset and gain mismatches, and initial timing-skews are well filtered-out through the accumulator, non-white error sources, such as harmonic distortions in the REF-ADC, greatly degrade the calibration accuracy. Thus, the number of occurrences of the non-zero error control signal ($e \neq 0$, a value that implies that the error value carries a meaningful information about the direction of skews) induced by skews should exceed that from harmonic distortions. Fig. 6 shows how the unwanted instances occur regarding the resolution and the harmonic distortions. For a low-resolution REF-ADC, the quantization step (LSB) is large, and the probability forming different digital outputs ($e \neq 0$) from a given skew is small, as shown in Fig. 6(a) (showing $e = 0$ even with a certain timing-skew). On the other hand, the probability in forming undesired control signals is high with relatively poor sampling network and device mismatch

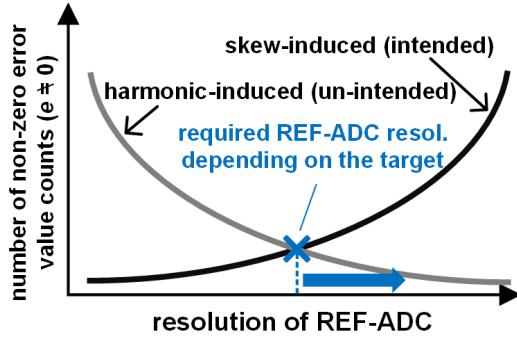


Fig. 7. Conceptual relationship between the resolution of the REF-ADC and the non-zero error value counts from skews and from harmonic distortions.

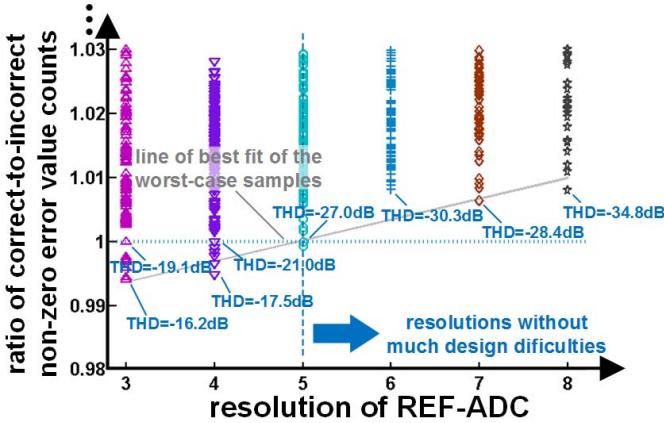


Fig. 8. Simulated ratio of correct-to-incorrect error control signal (non-zero error value) counts with harmonic distortions. (Simulated with a fixed 100-fs skew, 500-MSps conversion rate, and a near-Nyquist rate input. Harmonic distortions are modeled from SAR ADC capacitor mismatches ranging from 0.25% to 0.4% in unit capacitors.)

performance, as shown in Fig. 6(b), where the REF-ADC exhibits a distorted output and shows a non-zero error value even with the closely sampled values. To guarantee a certain degree of calibration accuracy, the resolution of the REF-ADC should be chosen so that the error control signal from skews far exceeds that from harmonic distortions, as shown in Fig. 7. Fig. 8 shows a software simulation conducted to determine how the resolution and the harmonic distortions of the REF-ADC impact the validity of the skew sign detection. Note that the correct count also includes some of the occurrences from distortions that are happen to be caused in the same sign of skews. The harmonic performance generally improves as the resolution increases for the same unit capacitor mismatches in the REF-ADC made with an SAR architecture; unit capacitor mismatches are employed to portray harmonic distortions in an SAR ADC. With the improvements in harmonic distortions and with smaller LSB steps as the resolution increases, the error value (e_{sign}) better reflects the effect from skews rather than that from harmonic distortions. For REF-ADC resolutions over 5 b, the non-zero error value counts induced by skews outweigh those from harmonic distortions even in the worst case. In our 12-b prototype ADC, a 6-b resolution REF-ADC was employed due to a concern for the design margin.

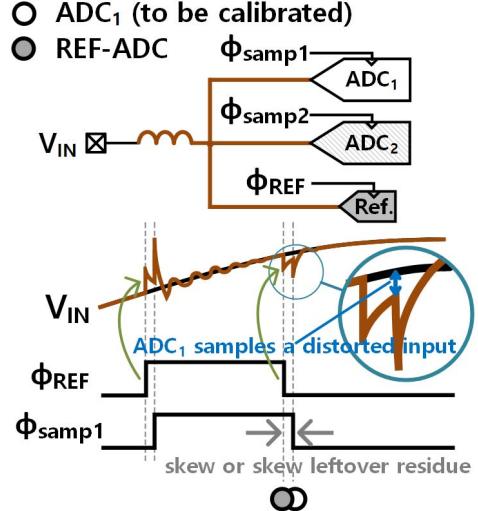


Fig. 9. Illustration showing the sampling kickback and the input ringing.

B. Sampling Kickbacks and Input Ringing

As previously mentioned, an important factor that should be carefully considered in designing an auxiliary ADC that samples the input at nearly the same time as the main channels (which is the REF-ADC in this paper) is the sampling kickbacks and the corresponding input ringing [6]. Fig. 9 illustrates how the sampling kickbacks and the input ringing are formed. With a TI-ADC input directly encountering a bondwire inductance, the input is vulnerable to ringing since the sampling capacitance gets sharply changed in a TI-ADC as the sampling switches are turned ON and OFF sequentially. A sudden start or end of the sampling phase causes a sudden change in the capacitance and its driving current seen from the input and causes an abrupt change in the input voltage with the ripples following it. The sampling kickback is also caused by the sampling clock fed through the overlap capacitances of the sampling switches to the input. Such kickbacks and ringing lead to unfavorable distortions in the input. Those effects are, however, well diminished if sufficient sampling time is provided and if there is an adequate time gap between the end and the start of the overlapping sampling phases of consecutive channels. This becomes a serious issue for the REF-ADC because it is artificially intended to conduct simultaneous sampling with the main channel. Because, there is a finite calibration step and a finite slope in the sampling clock, and because the calibration algorithm is designed to make the sampling edge of the channel toggle around that of the REF-ADC, there is likely to be many cases in which the REF-ADC sampling edge leads the calibrating channel by a small time gap, as shown in Fig. 9. In such a case, the channel samples a distorted input caused by the leading falling edge of the REF-ADC. Such behavior was observed in the measurements of our preliminary test-run chip fabrication with the SEB calibration algorithm, as shown in Fig. 10. In a four-way TI-ADC, the REF-ADC operates at 1/3 of the full conversion rate, so the channels are calibrated sequentially from CH4, CH3, CH2, and CH1 back to CH4. The timespan of the sampling phase of the REF-ADC is designed to be

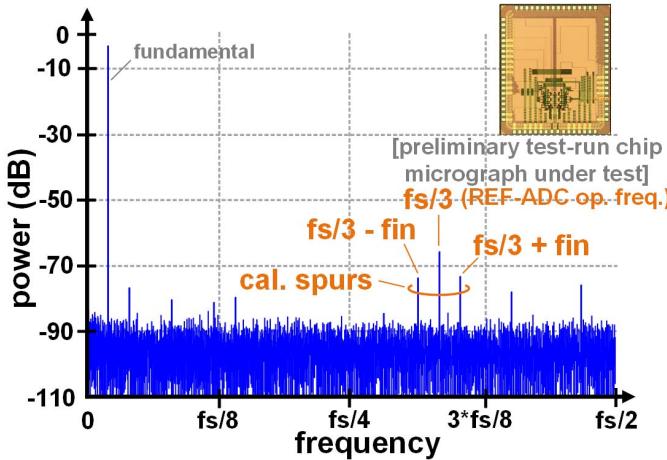


Fig. 10. Single sub-ADC channel spectrum measurement of a preliminary test-run chip fabrication of a four-way TI ADC with the SEB timing-skew calibration algorithm. (The operational frequency of the REF-ADC was 1/3 of the full conversion rate.)

identical to that of the subchannels with identical sampling circuits. As shown in Fig. 10, the calibration spurs caused by the sampling kickbacks and the input ringing are visible at the operational frequencies of the REF-ADC, whose tone powers are roughly equivalent to sampling errors on the order of $\pm 600 \mu V_{RMS}$.

Luu *et al.* [14] and Chen and Murmann [15] employed input buffers to suppress the kickbacks and the ringing by isolating the ADC from the input. While such an isolation greatly alleviates this phenomenon, the power consumption through the input buffers generally outweighs the ADC core itself, not to mention the design difficulties regarding the large bandwidth and high linearity requirements for high-speed and high-resolution ADCs.

III. PROPOSED VIRTUAL-TIMING-REFERENCE TIMING-SKEW CALIBRATION SCHEME

To mitigate the sampling kickbacks and the input ringing which cause unfavorable distortion in the sampled value of the main channels, this paper proposes a VTR timing-skew calibration scheme. Fig. 11 shows how the proposed scheme works in a conceptual diagram. With artificial time delays to the sampling clock and to the input of the REF-ADC, the occurrence of sampling kickbacks and its corresponding input ringing from the REF-ADC are deferred until the main channels sample the undistorted input without interruptions, while the delayed-input represents the input value preceded by a designed time delay. In this scheme, the REF-ADC samples the input at a virtual sampling edge, although its actual sampling edge is pushed further back with the designed delay. The REF-ADC operates completely unseen in the background to carry out its function to calibrate the timing-skews of the main channels without causing any disruption of the main channels.

A. Artificial Delays and Its Implementations

The proposed VTR timing-skew calibration algorithm requires two artificial delays for the REF-ADC as shown

in Fig. 11 with delayCLK and delayINPUT for different purposes. Here, delayCLK provides a fixed delay to the sampling clock of the REF-ADC so that the sampling edge of the REF-ADC artificially lags behind that of main channels. Thus, the sampling kickbacks and the corresponding input ringing induced by the REF-ADC's sampling edge are deferred until the main channels finish their sampling phases. This prevents the channels from sampling a distorted input. However, such a delay to the sampling clock alone has no desired effect due to the skew calibration algorithmic nature because the algorithm itself is intended to align the sampling edges of all channels to that of REF-ADC. If there is an artificial delay in the REF-ADC's sampling clock, the calibration algorithm will impose equivalent delays on each channel as well, thus counterbalancing the artificial delay. A straightforward solution to such an algorithmic contradiction is to deceive the calibration algorithm with a delayed input using delayINPUT , in which the values sampled by the REF-ADC reflect the input preceded by the designed input delay. Fig. 12 shows how the artificial delays and their mismatch affect the timing-skew calibration directions to which the channel sampling edges are aligned. With delayINPUT , the REF-ADC sees a delayed counterpart of the input, whose sampled value is then processed in the SEB timing-skew calibration algorithm as a reference to determine the directions of skews, thus forming a virtual timing-reference point. If two delays (delayCLK and delayINPUT) are identical, the virtual sampling edge processed in the calibration algorithm is at the original sampling edge of the REF-ADC without delays. On the other hand, if more time delay is provided in delayCLK than in delayINPUT , the virtual sampling edge lags behind the original. Given that the calibration range of each channel is sufficiently large, the mismatch in the artificial delays becomes a trivial concern in terms of the reference point, although the mismatch itself consumes and narrows the calibration range.

In the prototype ADC, delayCLK and delayINPUT were designed to be roughly 4 ps. Fig. 13 shows how those delays are implemented in the circuits. The inbound input delay to the REF-ADC is roughly 4 ps through a second-order low-pass filter, whereas the outbound delay of the sampling kickbacks and the ringing to the main channel is roughly greater than 25 ps thanks to the large sampling capacitor of the main channels. Such a large outbound delay, together with the artificial clock delay of 4 ps, provides sufficient time to guarantee that the main channel would be completely done with its sampling well before the input can be disturbed by the REF-ADC, considering that the falling time of the sampling clock is estimated to be roughly 15 ps. The calibration range of each channel was designed to be roughly ± 5 ps, with a rough offset delay of 5 ps ($t_{D,CENTER}$) to equally account for both leading and lagging skews. The artificial delay to the sampling clock of the REF-ADC (delayCLK and $t_{D,CENTER}$) is implemented by providing more capacitance to the inverter chain, as shown in Fig. 13. The standard deviation of the delay mismatch in delayCLK and delayINPUT from the process variation is estimated to be 150 fs whereas the delay mismatch from the temperature variation is estimated to be $10.4 \text{ fs}/^\circ\text{C}$,

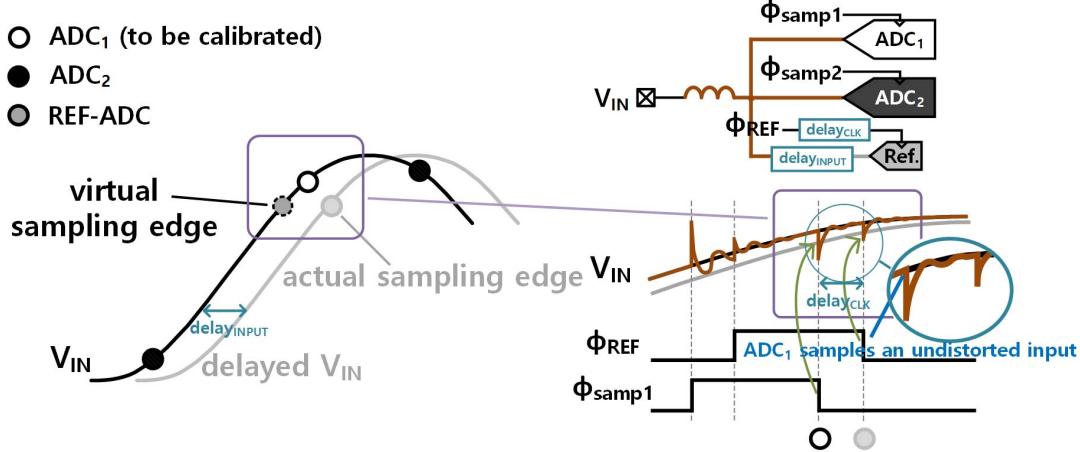


Fig. 11. Conceptual diagram of the proposed VTR calibration scheme.

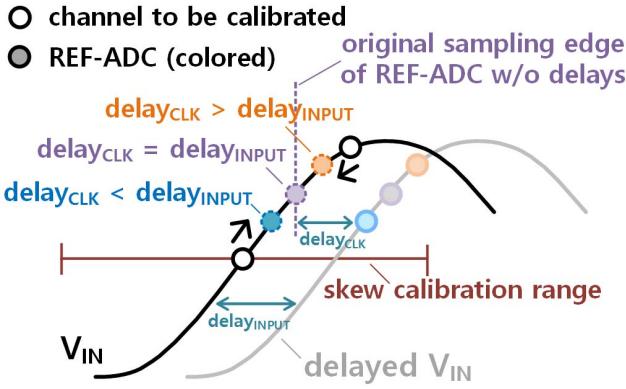


Fig. 12. Effects of delay mismatches in the input and the sampling clock of the REF-ADC on the timing-skew calibration directions to which the sampling edges of channels are aligned.

both of which are negligible compared to the controllable calibration range.

B. Effect of Sampling Kickbacks and Input Ringing of the Main Channels on the Calibration Algorithm

Just as the REF-ADC influences the input with its falling sampling edge, the main channels also disturb the input with their falling edges, which then distort the sampled values of the REF-ADC. As with the harmonic distortions, these non-white error sources cannot be filtered-out through the accumulator, and they do affect the calibration accuracy in the SEB timing-skew calibration algorithm, as previously mentioned in Section II-A. However, note that those main channel-induced kickbacks and ringing are greatly attenuated through the second-order filter, whose tone power is estimated to be less than -70 dBc, as shown in Fig. 10, with our preliminary test-run chip fabrication; the circuits comprising the sampling network in both the main channel and the REF-ADC are identical except the sampling capacitances.

Despite its estimated low kickback tone power, the number of occurrences of the error control signal ($e \neq 0$) induced by skews should outweigh the non-skew originated non-white errors, including the harmonic distortions of the REF-ADC

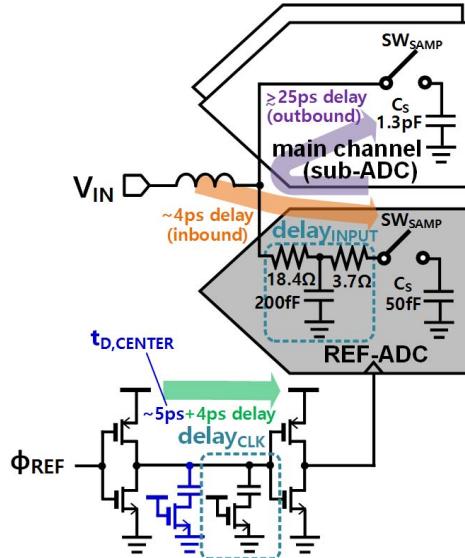


Fig. 13. Implementations of artificial delays in a single-ended representation.

and the sampling kickbacks from main channels, to guarantee a certain degree of skew calibration accuracy. Thus, the REF-ADC resolution requirement becomes tighter than what is shown in Fig. 8, considering both the harmonic distortions and the sampling kickbacks from the main channels; therefore, we chose a 6-b resolution rather than 4–5 b.

IV. IMPLEMENTATIONS

Fig. 14 shows the overall block diagram and the implementation of the proposed VTR and the SEB [10] timing-skew calibration algorithm. Using D-FFs following the output MUX, the adjacent channel outputs can be stored and used for the calibration algorithm. The XOR gate determines whether the skew is leading or lagging behind by exploiting the innate sign-equality checking function, and it feeds its control signal to the 32-count accumulator in each channel. The following quantifier transforms the digitally filtered control signal to a 9-b control value to maneuver the 9-b digitally controlled delay line to adjust the sampling clock in each channel.

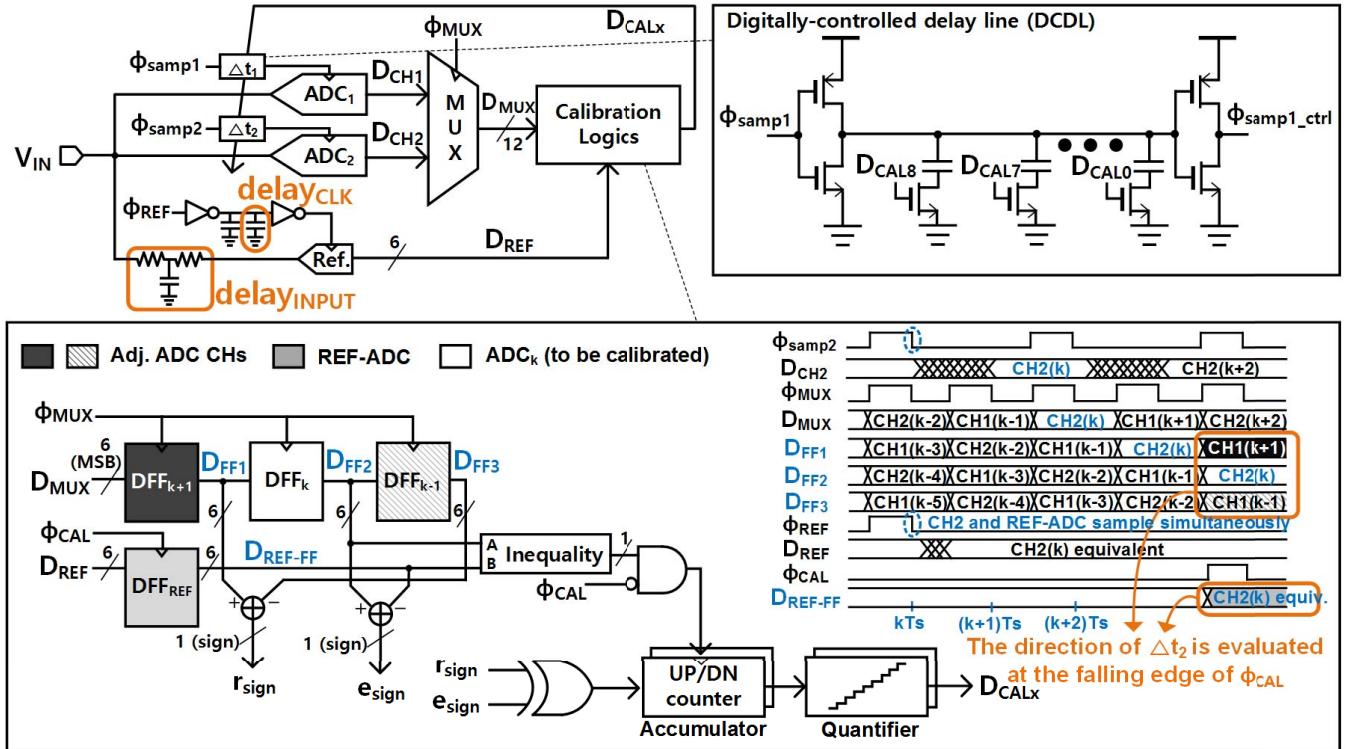


Fig. 14. Block diagram and implementation of the proposed VTR and SEB [10] timing-skew calibration algorithm.

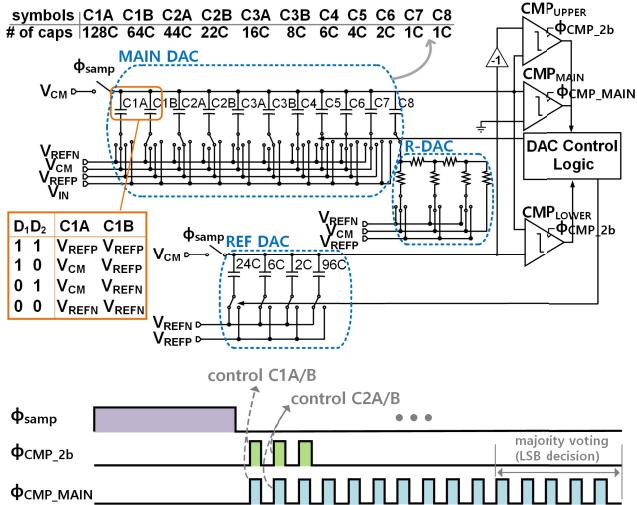


Fig. 15. Single-ended representation of a main channel SAR ADC with 2 b/cycle conversion cycles [16] and a 3-b R-DAC.

Fig. 15 shows a block diagram of a main channel SAR ADC in a single-ended representation for simplicity. A 2-b/cycle operation [16] is employed in the first three MSB decision cycles to accelerate the conversion speed and to spare 5-LSB cycles for adopting a majority voting scheme [17] to reduce the comparator noise. While the MSB 2-b switching logic could be direct (i.e., a 2-b comparator digital output 10 could directly map to V_{REFP} and V_{REFN} in C1A and C1B, respectively), a ternary-level thermometer switching scheme in [18] is employed to minimize the capacitor switching operations and, most importantly, to alleviate the static non-linearity

induced from switching unnecessarily redundant capacitors in contradictory directions. For instance, in conventional switching operations, if a 2-b digital output is 01, the bottom plate of C1A switches from V_{CM} to V_{REFN} , while that of C1B switches from V_{CM} to V_{REFP} to form a voltage change equivalent to switching only C1B from V_{CM} to V_{REFN} . In such a case, capacitor mismatches present in both capacitors C1A and C1B add up and cause a large mismatch in forming an intended decision threshold. By making the reference change minimal with the references of C1A, C2A, and C3A fixed to V_{CM} for 2-b digital codes 01 and 10, the static non-linearity is greatly alleviated around the mid code. Thanks to the improvements in the static non-linearity, the total capacitance of the capacitive-DAC can be designed 37% smaller than that of a conventional scheme to meet the same static non-linearity requirement. The total capacitance of the capacitive-DAC was designed to be 1.3 pF, which is close to the order of magnitude of the thermal noise limited capacitance of 0.7 pF. Redundancies are provided in between 2-b decision cycles to account for the gain mismatches between the REF DAC and the MAIN DAC, and also for the offset variations in CMP_{UPPER} and CMP_{LOWER} as their reference voltages (REF DAC) change. A 3-b R-2R DAC is employed in LSB decisions to prevent the MOM capacitor-based capacitive-DAC from being extremely long in the lateral direction in a concern for routing parasitic and gradient fabrication mismatches.

Fig. 16 shows a single-ended representation of the REF-ADC employing a conventional 6-b SAR ADC architecture with redundancies (non-binary 7 b) and a total sampling capacitance of 50 fF. The bandwidth of the sampling network in the main channels was designed to be roughly 500 MHz.

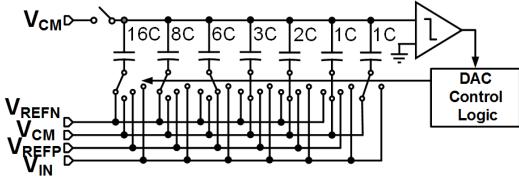


Fig. 16. Single-ended representation of a 6-b SAR-type REF-ADC (seven non-binary bits).

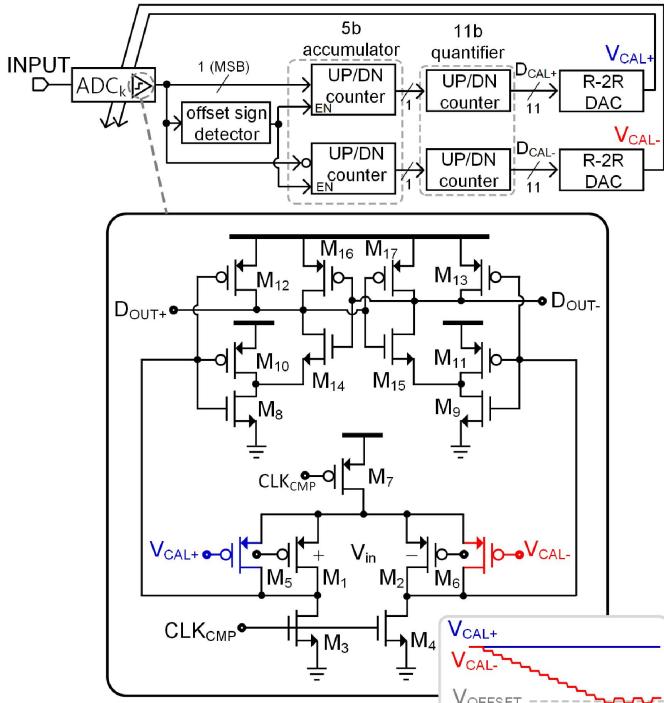


Fig. 17. Main comparator with offset calibration.

Such a large bandwidth beyond the Nyquist-rate input greatly helped alleviate the concerns for bandwidth mismatches between the REF-ADC and the main channels. The gain mismatches between the REF-ADC and the main channels are greatly alleviated through the bottom-plate sampling scheme.

The offset of each main channel is calibrated in the foreground with a dc zero input by analyzing the 32-count accumulated mean of the MSB polarity signs to take into account the overall offset-inducing errors, including the clock feedthrough and charge injection mismatches, besides the comparator offset itself, in which the effective offset is calibrated by adjusting the calibration control voltages (V_{CAL+} and V_{CAL-}) to the input-stage calibration pair (M_5 and M_6) of the main comparator, as shown in Fig. 17. The offset sign detector determines the polarity direction of the existent offset and enables only one single-ended control path while keeping the other control voltage at VDD. In such a scheme, only the amount of required mismatch-compensation current is supplemented through the calibration pair (M_5 or M_6), rather than operating in a true-differential mode in which the elevated common-mode supplemental currents through the calibration pair weaken the effect of the comparator inputs in making a bit decision, which in turn aggravates the noise performance. The low-noise double-tail-based dynamic comparator in [19] was employed

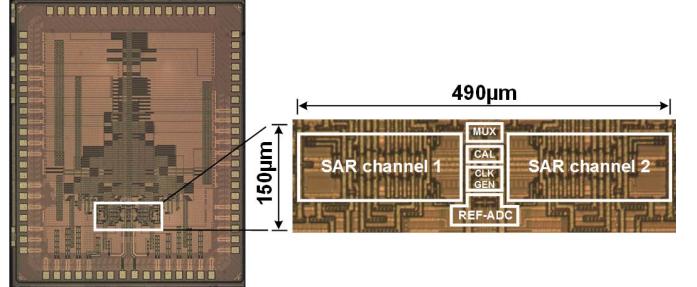


Fig. 18. Chip micrograph.

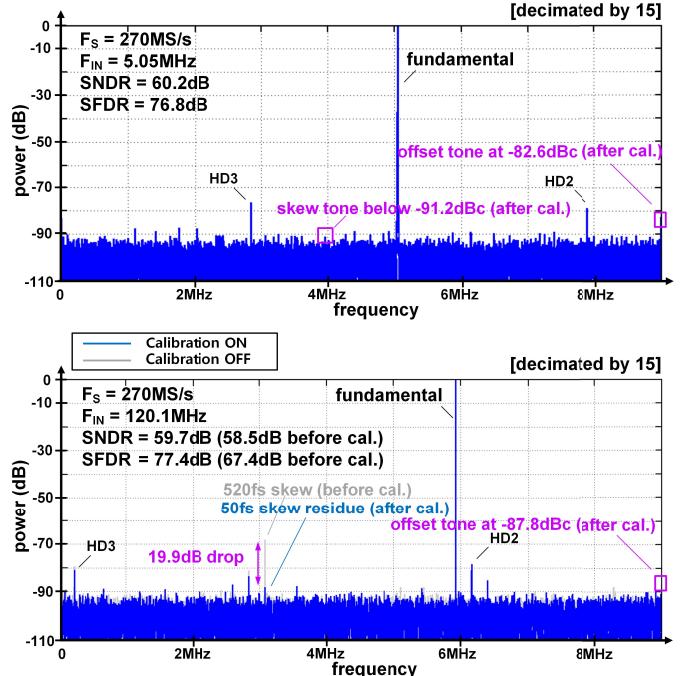


Fig. 19. Measured output spectra with 5.05- and 120.1-MHz inputs (number of samples = 32 768, output is decimated by 15).

in the prototype to improve the comparator noise performance. A PMOS input pair was used to suppress the flicker noise. The offsets of the adjacent comparators used for 2 b/cycle decisions (CMP_{UPPER} and CMP_{LOWER}) are calibrated in the background in relatively crude accuracy using a simple charge-pump calibration scheme in [20].

V. MEASUREMENT RESULTS

A prototype two-way TI 12-b 270-MS/s SAR ADC with the proposed (VTR timing-skew calibration scheme was fabricated in a 40-nm general purpose CMOS process as to verify our concept. The prototype consumed 4.5 mW from a 0.9-V supply, including the offset and timing-skew calibration circuits where the REF-ADC consumes only 0.13 mW. Fig. 18 shows a chip micrograph of the prototype. The proposed timing-skew calibration scheme including the 6-b REF-ADC, the calibration engine, and the 32-count accumulator as well as the 9-b quantifier in each channel occupies only 9.7% of the total active area. Fig. 19 shows the measured output spectra with 5.05- and 120.1-MHz inputs at a conversion rate of 270 MS/s.

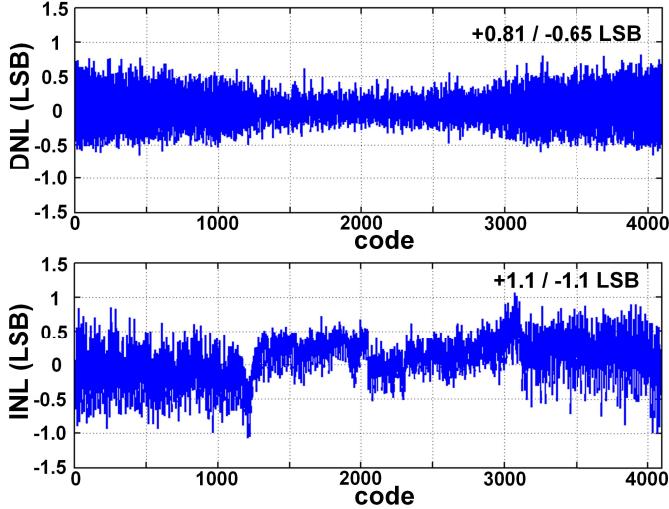


Fig. 20. Measured DNL and INL.

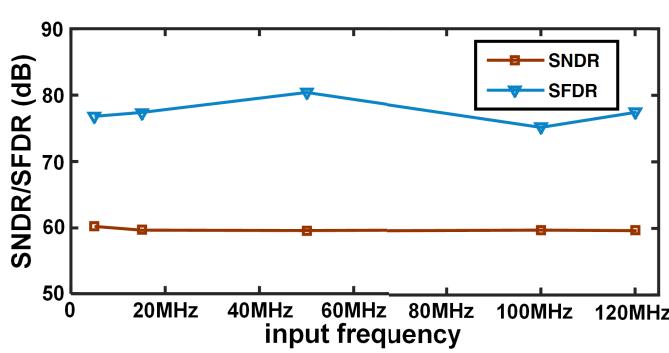


Fig. 21. Measured dynamic performance in relation to the input frequency at a sampling rate of 270 MS/s.

For a 5.05-MHz input, the timing-skew tone power decreased below the noise floor after timing-skew calibration, and it showed an SNDR and an SFDR of 60.2 and 76.8 dB, respectively. For a near-Nyquist-rate 120.1-MHz input, the effect of the timing-skew calibration became more dramatic with a 19.9-dB drop in the skew tone power (roughly from 520- to 50-fs skew). Thanks to the proposed VTR timing-skew calibration scheme, the calibration spurs induced from REF-ADC operation (it operates once in every 21 samples, or $f_{S,\text{REF-ADC}} = f_S/21$) were greatly suppressed in the output spectra of the TI main channels, completely concealing the timing-skew calibration operations.

The measured static non-linearity performance of the prototype is shown in Fig. 20. The measured differential non-linearity (DNL) and integral non-linearity (INL) were $+0.81/-0.65$ LSB and $+1.1/-1.1$ LSB, respectively. Fig. 21 shows the dynamic performance at a sampling rate of 270 MS/s for various input frequencies. The SFDR stayed above 75 dB after the timing-skew calibration. The performance was severely limited by noise, as is evident from the relatively stagnant SNDR over the change in the input frequency. The elevated noise level is greatly ascribed to the comparator noise in a tradeoff between the conversion speed and the noise integration time.

TABLE II
COMPARISON OF TIMING-SKEW CALIBRATION TECHNIQUES

	Wei JSSC '14 [3]	Ei-Chammas JSSC '11 [7]	Stepanovic JSSC '13 [9]	Luo VLSI '17 [21]	This Work
Timing-Skew Cal. Scheme	Autocorrelation on-based	Autocorrelation on-based	Derivative-based	Clock injection-based	VTR w/ SEB
Resolution	8b	5b	10b	10b	12b
fs	4000MS/s	1200MS/s	2800MS/s	2000MS/s	270MS/s
# of Channels	4	8	24	4	2
Timing-Skew Residue after Cal.	$\sim 30\text{fs}^{***}$ (-70dBc @ 1.89GHz)*	400fs	$\sim 190\text{fs}^{***}$ (-55.7dBc @ 1.38GHz)*	$\sim 140\text{fs}^{***}$ (-61dBc @ 991MHz)*	$\sim 50\text{fs}^{***}$ (-88dBc @ 120.1MHz)**
Domain of Cal. Engine / Detection	off-chip	off-chip	on-chip	on-chip	on-chip

* total residual timing-skew tone power estimated from plots shown in respective articles with near-Nyquist rate inputs

** residual timing-skew tone power from Fig. 19

*** estimated timing-skew in femto-seconds using (4) calculated from the estimated timing-skew tone power in * or **

TABLE III
PERFORMANCE SUMMARY AND COMPARISON

	C. Lin TCAS-I '16 [22]	J. Mulder ISSCC '15 [23]	A. Venca JSSC '16 [24]	This Work
Architecture	TI Pipelined-SAR	TI Pipeline	TI SAR-Δ	TI SAR
Technology	65nm CMOS	28nm CMOS	28nm CMOS	40nm CMOS
Resolution	12b	13b	12b	12b
fs	210MS/s	800MS/s	600MS/s	270MS/s
Power Supply	1.0V	1.0V/1.8V	1.2V/1.5V	0.9V
# of Channels	2	2	4	2
Timing-Skew (or residue after cal.)	$\sim 200\text{fs}^{***}$ (-78dBc @ 100MHz)*	$\sim 250\text{fs}^{***}$ (-65dBc @ 350MHz)*	$\sim 360\text{fs}^{***}$ (-64.5dBc @ 265MHz)*	$\sim 50\text{fs}^{***}$ (-88dBc @ 120.1MHz)**
SNDR _{PEAK}	63.5dB	59.2dB	60.7dB	60.2dB
SNDR _{Nyq}	60.1dB	57dB	58dB	59.7dB
Power	5.3mW	76.4mW	26.5mW	4.5mW
FoM _{Walden@Nyq}	30.3fJ/step	162.4fJ/step	68.0fJ/step	21.1fJ/step
Area	0.48mm ²	0.23mm ²	0.076mm ²	0.074mm ²

* total residual timing-skew tone power estimated from plots shown in respective articles with near-Nyquist rate inputs

** residual timing-skew tone power from Fig. 19

*** estimated timing-skew in femto-seconds using (4) calculated from the estimated timing-skew tone power in * or **

Table II summarizes and compares the prototype with previously published state-of-the-art timing-skew calibration algorithms. The proposed design exhibits the finest calibration accuracy in terms of the residual timing-skew for fully integrated (on chip) timing-skew calibration schemes. Table III summarizes the prototype performance and compares it to comparable state-of-the-art TI architectures. The prototype exhibits a peak and a near-Nyquist rate SNDR of 60.2 and 59.7 dB, respectively. The resulting Nyquist-rate Walden FoM is 21.1 fJ/conversion-step. The proposed design exhibits a trivial degradation in SNDR performance at the Nyquist-rate input, as a result of the timing-skew calibration algorithm, while the un-calibrated designs introduced in [22]–[24] show a noticeable drop as the input frequency increases.

VI. CONCLUSION

This paper proposed a VTR timing-skew calibration algorithm to defer the actual sampling edge of the REF-ADC to

prevent the main channels from sampling a distorted input. With the proposed scheme, the calibration spurs for operating the REF-ADC are effectively suppressed while the skews are calibrated unseen in the background. The prototype 12-b 270-MS/s two-way TI SAR ADC incorporating the proposed timing-skew calibration algorithm exhibits a competitive calibration accuracy in comparison to state-of-the-art timing-skew calibration designs with a residual skew estimated to be roughly 50 fs. The calibration algorithm is fully integrated and occupies only 9.7% of the total active area while the 6-b REF-ADC consumes only 0.13 mW. The prototype achieves a peak SNDR of 60.2 dB and a Nyquist-rate SNDR of 59.7 dB while consuming 4.5 mW (including all calibration and reference powers) from a 0.9-V supply. The resulting Walden FoM at the Nyquist-rate input is 21.1 fJ/conversion-step.

REFERENCES

- [1] K. Doris, E. Janssen, C. E. Janssen, A. Zanikopoulos, and G. van der Weide, "A 480 mW 2.6 GS/s 10 b time-interleaved ADC with 48.5 dB SNDR up to Nyquist in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2821–2833, Dec. 2011.
- [2] S. W. M. Chen and R. W. Brodersen, "A subsampling radio architecture for ultrawideband communications," *IEEE Trans. Signal Process.*, vol. 55, no. 10, pp. 5018–5031, Oct. 2007.
- [3] H. Wei, P. Zhang, B. D. Sahoo, and B. Razavi, "An 8 bit 4 GS/s 120 mW CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1751–1761, Aug. 2014.
- [4] D. Fu, K. C. Dyer, S. H. Lewis, and P. J. Hurst, "A digital background calibration technique for time-interleaved analog-to-digital converters," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1904–1911, Dec. 1998.
- [5] A. Zanchi and F. Tsay, "A 16-bit 65-MS/s 3.3-V pipeline ADC core in SiGe BiCMOS with 78-dB SNR and 180-fs jitter," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1225–1237, Jun. 2005.
- [6] J. Song, K. Ragab, X. Tang, and N. Sun, "A 10-b 800-MS/s time-interleaved SAR ADC with fast variance-based timing-skew calibration," *IEEE J. Solid-State Circuits*, vol. 52, no. 10, pp. 2563–2575, Oct. 2017.
- [7] M. El-Chammas and B. Murmann, "A 12-GS/s 81-mW 5-bit time-interleaved flash ADC with background timing skew calibration," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 838–847, Apr. 2011.
- [8] B. Razavi, "Design considerations for interleaved ADCs," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1806–1817, Aug. 2013.
- [9] D. Stepanovic and B. Nikolic, "A 2.8 GS/s 44.6 mW time-interleaved ADC achieving 50.9 dB SNDR and 3 dB effective resolution bandwidth of 1.5 GHz in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 971–982, Apr. 2013.
- [10] H.-W. Kang, H.-K. Hong, S. Park, K.-J. Kim, K.-H. Ahn, and S.-T. Ryu, "A sign-equality-based background timing-mismatch calibration algorithm for time-interleaved ADCs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 6, pp. 518–522, Jun. 2016.
- [11] T. Miki, T. Ozeki, and J. Naka, "A 2-GS/s 8-bit time-interleaved SAR ADC for millimeter-wave pulsed radar baseband SoC," *IEEE J. Solid-State Circuits*, vol. 52, no. 10, pp. 2712–2720, Oct. 2017.
- [12] C. Tao and A. A. Fayed, "A buck converter with reduced output spurs using asynchronous frequency hopping," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 11, pp. 709–713, Nov. 2011.
- [13] W. Kim *et al.*, "A 0.6V 12b 10 MS/s low-noise asynchronous SAR-assisted time-interleaved SAR (SATI-SAR) ADC," *IEEE J. Solid-State Circuits*, vol. 51, no. 8, pp. 1826–1839, Aug. 2016.
- [14] D. Luu *et al.*, "Background calibration using noisy reference ADC for a 12 b 600 MS/s 2× TI SAR ADC in 14 nm CMOS FinFET," in *Proc. IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2017, pp. 183–186.
- [15] S. Chen and B. Murmann, "An 8-bit 1.25 GS/s CMOS IF-sampling ADC with background calibration for dynamic distortion," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2016, pp. 69–72.
- [16] H. K. Hong *et al.*, "A decision-error-tolerant 45 nm CMOS 7 b 1 GS/s nonbinary 2 b/cycle SAR ADC," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 543–555, Feb. 2015.
- [17] P. Harpe, E. Cantatore, and A. van Roermund, "A 10 b/12 b 40 kS/s SAR ADC with data-driven noise reduction achieving up to 10.1 b ENOB at 2.2 fJ/conversion-step," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3011–3018, Dec. 2013.
- [18] H.-W. Kang, H.-K. Hong, S. Park, K.-J. Kim, K.-H. Ahn, and S.-T. Ryu, "Ternary-level thermometer C-DAC switching scheme for flash-assisted SAR ADCs," *IEICE Electron. Express*, vol. 12, no. 10, pp. 1–7, May 2015, doi: 10.1587/elex.12.20150302.
- [19] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A low-noise self-calibrating dynamic comparator for high-speed ADCs," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2008, pp. 269–272.
- [20] P. M. Figueiredo *et al.*, "A 90 nm CMOS 1.2 V 6 b 1 GS/s two-step subranging ADC," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2006, pp. 2320–2329.
- [21] L. Luo, S. Chen, M. Zhou, and T. Ye, "A 0.014 mm² 10-bit 2 GS/s time-interleaved SAR ADC with low-complexity background timing skew calibration," in *Proc. Symp. VLSI Circuits (VLSIC)*, Kyoto, Japan, Jun. 2017, pp. C278–C279.
- [22] C.-Y. Lin and T.-C. Lee, "A 12-bit 210-MS/s 2-times interleaved pipelined-SAR ADC with a passive residue transfer technique," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 7, pp. 929–938, Jul. 2016.
- [23] J. Mulder *et al.*, "An 800 MS/s 10 b/13 b receiver for 10 GBASE-T Ethernet in 28 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 1–3.
- [24] A. Venca, N. Ghittori, A. Bosi, and C. Nani, "A 0.076 mm² 12 b 26.5 mW 600 MS/s 4-way interleaved subranging SAR-ΔΣ ADC with on-chip buffer in 28 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2951–2962, Dec. 2016.



Hyun-Wook Kang received the B.S. degree (with high Hons.) in electrical engineering and computer sciences from the University of California, Berkeley, CA, USA, in 2011, and the M.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2013, where he is currently pursuing the Ph.D. degree.

His current research interests include power-efficient data converter and mixed-signal circuit designs.



Hyeok-Ki Hong received the B.S. degree in electrical engineering and IT business, the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2010, 2012, and 2016, respectively.

In 2016, he was a Researcher with the Information and Electronics Research Center, KAIST. He is currently a Research Staff Member with the Samsung Advanced Institute of Technology, Suwon, South Korea. His current research interests include data converters and mixed-signal circuit design.

Dr. Hong was a recipient of the Samsung HumanTech Award in 2011, 2012, and 2014, the IEEE SSCS Pre-Doctoral Achievement Award in 2016 ISSCC, and in 2015 as a co-recipient.



Wan Kim received the B.S. degree (Hons.) in electronic engineering from Inha University, Incheon, South Korea, in 2008, the M.S. degree in information and communications from the Gwangju Institute of Science and Technology, Gwangju, South Korea, in 2010, and the Ph.D. degree in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2016.

Since 2016, he has been a Senior Engineer with Samsung Electronics, Hwaseong, South Korea. His current research interests include digital calibration techniques for high-resolution data converters and low-noise mixed-signal circuit design for low-power applications.

Dr. Kim was a recipient of a silver prize in the Samsung HumanTech Paper Award in 2016.



Seung-Tak Ryu (M'06–SM'13) received the B.S. degree in electrical engineering from Kyungpook National University, Daegu, South Korea, in 1997, the M.S. and Ph.D. degrees from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 1999 and 2004, respectively.

From 2001 to 2002, he was a Visiting Researcher with the University of California, San Diego, CA, USA, sponsored through the Brain Korea 21 Program. In 2004, he joined Samsung Electronics, Kiheung, South Korea, where he was involved in mixed-signal IP design. From 2007 to 2009, he was an Assistant Professor with the Information and Communications University, Daejeon. Since 2009, he has been with the Department of Electrical Engineering, KAIST, where he is currently an Associate Professor. His current research interests include analog and mixed-signal IC design with an emphasis on data converters.

Dr. Ryu has been serving on the Technical Program Committees of the International Solid-State Circuits Conference and the Asian Solid-State Circuits Conference. He has also served as a Guest Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, and he is currently serving as an Associate Editor of the IEEE SOLID-STATE CIRCUITS LETTERS.