A Blocker-Tolerant RF Front End With Harmonic-Rejecting N-Path Filter

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***Abstract*— An RF front end with a harmonic-rejecting N-path filter is presented. It features tunable narrow-band filtering and high attenuation at the third- and fifth-order local oscillator (LO) harmonics at the LNA output, which improves the blocker tolerance at LO harmonics. The 0.2–1 GHz RF front end is implemented in a 65-nm CMOS process. The blocker 1-dB compression point (B1dB) is −2.4 dBm at a 20-MHz offset, and remains high at the third- and fifth-order LO harmonics. The reverse isolation of the LNA helps keep the LO emission below −90 dBm. A two-stage harmonic rejection approach offers a >51 dB harmonic-rejection ratio at the third- and fifth-order LO harmonics without calibration.**

***Index Terms*— Blocker, CMOS, direct conversion, harmonic rejection, linearity, N-path filter (NPF), receiver, SAW-less, software-defined radio.**

I. Introduction

TO RECEIVE a narrow-band signal with wide tuning range, a wideband receiver is the key block in a software-defined radio or cognitive radio system. The wideband receiver front end needs to tolerate out-of-band (OB) blockers and needs to have large harmonic rejection to eliminate the need for off-chip tunable bandpass filters. Thus, an on-chip filtering technique is required to filter out the OB blocker. Conventional on-chip RF filters, such as LC [1] or gm-C [2], suffer from either a low quality (Q) factor, small tuning range, or limited linearity [3]. The switched capacitor-based N-path filter (NPF) [3]–[7] offers a high Q factor, large tuning range, and good linearity, and is a good candidate for on-chip blocker filtering. Furthermore, the switched-capacitor approach benefits from the process scaling, which provides faster switches and a lower power clock generator [8].

When using N-path filtering at the RF input [see Fig. 1(a)], the RF N-path bandpass filters [3], [5], [7] and the mixer-first receivers [9], [10] directly attenuate the OB blocker at the input resulting in an excellent blocker tolerance; however, for systems where there are strict emission limits, local oscillator (LO) leakage can be a potential problem. Also, large capacitors are required to achieve narrow-band filtering due to the relatively small source impedance. Since the OB attenuation at the RF input node [V_{in} in Fig. 1(a)] is limited to the ratio of $R_{\text{ON}}/(R_{\text{ON}} + R_s)$, where R_{ON} is the switch-ON resistance, small R_{ON} is also required. These filters further exhibit spurious responses [5] at the harmonics of the LO signal, which there result in poor OB linearity. Preceding the NPF with an active LNA [see Fig. 1(b)], [11], [12] offers reverse isolation and reduces the LO leakage. Also, the LNA output impedance is larger than the 50-Ω source resistance, which reduces the capacitor sizes and relaxes the switch R_{ON} requirement. However, those receivers still have harmonic responses at the LNA output, which reduce the blocker tolerance for blocking signals close to the LO harmonic frequencies. Various harmonic-rejection mixing techniques [12]–[16] have been proposed. Using harmonic recombination in baseband [12] achieves a good harmonic-rejection ratio (HRR), but the harmonic attenuation (HA) at the LNA output is not improved. The current-driven passive mixer and two-stage harmonic rejection approach in [13] shows high HRR and good OB linearity. However, it offers only a moderate blocker 1-dB compression point (B1dB) at low blocker offset frequencies. The harmonic-rejection transimpedance amplifiers (TIAs) proposed in [16] reduce the harmonic downconversion after the baseband TIA for mixer-first receivers and current-driven mixers, though the harmonic downconversion before the TIA cannot be eliminated using this technique. In [17], a bandpass filter without the third harmonic response was proposed and its operation and performance was evaluated in simulation. However, that

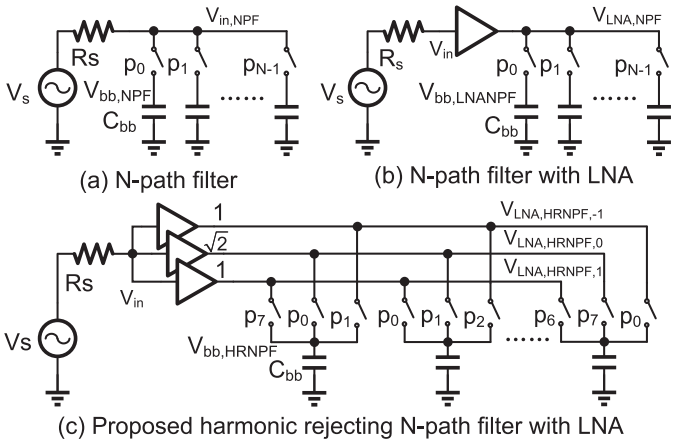

Fig. 1. (a) Conventional NPF. (b) Conventional NPF with LNA. (c) Proposed HR-NPF with LNA.

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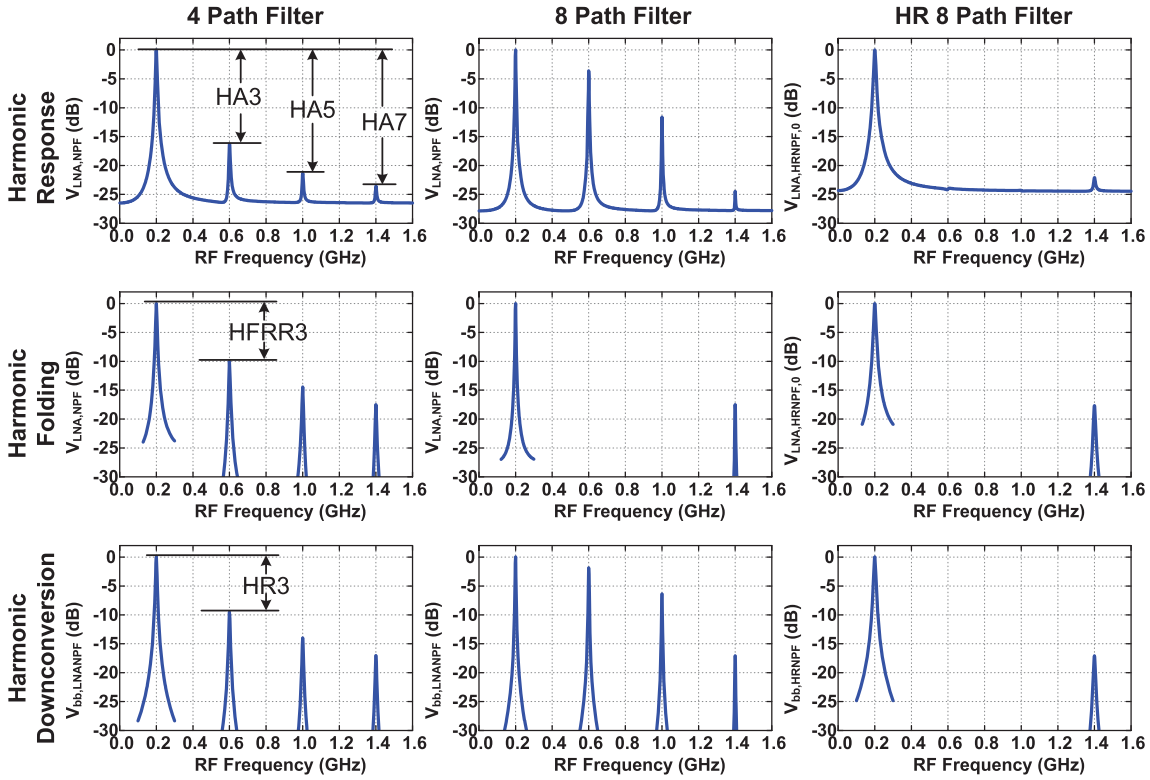

Fig. 2. Simulated harmonic response (top), harmonic folding (middle), and harmonic downconversion (bottom) in four-path filter (left), eight-path filter (center), and proposed HR-8PF (right) for a 0.2-GHz clock frequency.

approach cannot suppress the harmonic response before the recombination.

We propose a harmonic-rejecting NPF (HR-NPF), which reduces the harmonic responses at the third and fifth LO harmonics [see Fig. 1(c)] [18]. The active LNA provides a lower than −90 dBm LO leakage and high source impedance for the NPF. The harmonic responses are strongly attenuated by the HR-NPF, which improves the LNA blocker tolerance at LO harmonic frequencies. A receiver front-end prototype using the HR-NPF achieves a −2.4 dBm B1dB at only a 20-MHz blocker frequency offset, and the B1dB remains high at LO harmonics. The HR-NPF also offers additional harmonic rejection for the downconversion to achieve the two-stage harmonic rejection with >51 dB HRR at the third and fifth LO harmonics without calibration.

The rest of this paper is organized as follows. The concept and the analysis of the HR-NPF are developed in Section II. The RF receiver front end with an HR-NPF and the circuit implementation are described in Section III. Section IV provides the measurement results, and conclusions are presented in Section V.

II. Harmonic-Rejecting N-Path Filter

An NPF is a continuous-time switched-capacitor bandpass filter driven by N-phase $1/N$-duty-cycle non-overlapping clocks, which is well analyzed in [3], [5], and [6]. Due to the time-varying nature of the NPF, there are several frequency translation issues in the NPF compared with the linear-time-invariant filter. Using a differential architecture helps to mitigate the issues due to even-order harmonic. In this section, we first discuss the harmonic folding, harmonic response, and harmonic downconversion in a differential NPF, and then show the analysis of the HR-NPF.

A. Harmonic Response, Harmonic Folding, and Harmonic Downconversion in a Differential N-Path Filter

Fig. 2 shows the simulated harmonic response, harmonic folding, and harmonic downconversion of differential NPF with LNA [see Fig. 1(b)] and proposed HR-NPF with LNA [see Fig. 1(c)] for a 250-Ω LNA output resistor, a 10-Ω switch ON-resistor, an 80-pF baseband capacitor, and a 0.2-GHz clock frequency. These effects in an NPF are well analyzed in [6]. Considering the signal at LNA output, the harmonic response is the bandpass filtering function around the clock harmonics [see Fig. 2 (top)]. The HA is the ratio of the gain at desired signal frequency to the gain at clock harmonics. The HA of an NPF is

$$\mathrm{HA}_i = \frac{\mathrm{sinc}^2\left(\frac{\pi}{N}\right)}{\mathrm{sinc}^2\left(\frac{i\pi}{N}\right)}, \quad (i = \text{odd}) \tag{1}$$

where i is the order of clock harmonic, N is the number of paths in the NPF, and $\mathrm{sinc}(\mathrm{x}) = \sin(\mathrm{x})/\mathrm{x}$. Low HA degrades the blocker tolerance at the clock harmonics.

The folding of unwanted signals from clock harmonics to the desired signal band at the LNA output is called harmonic folding [see Fig. 2 (middle)]. The harmonic folding rejection ratio is the gain ratio of the desired RF signal to the signal

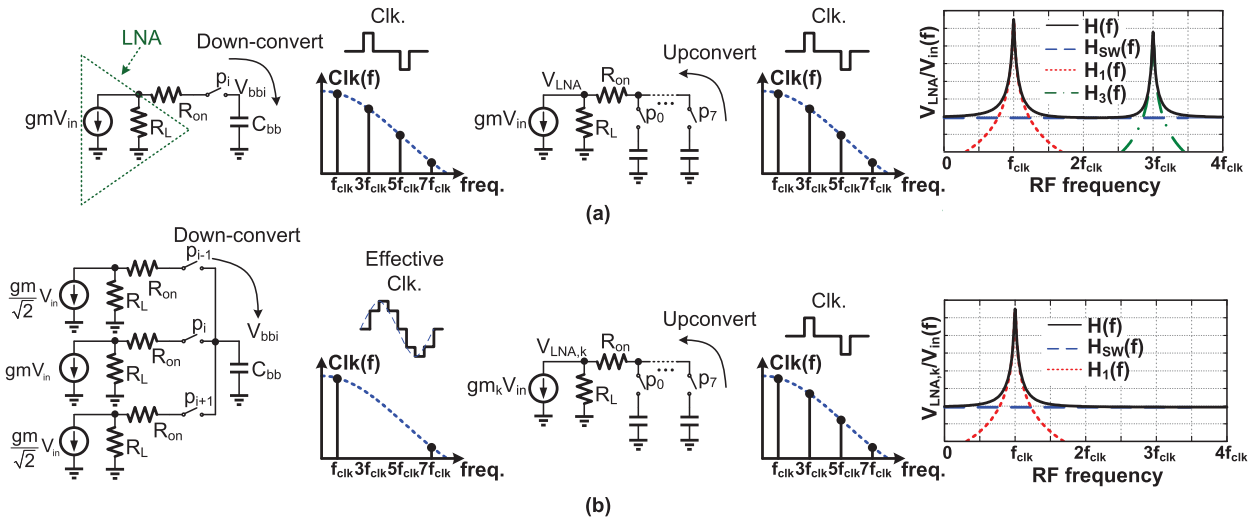

Fig. 3. Simplified model for the harmonic response analysis for a differential NPF at the output of the LNA; the LNA is modeled with a Norton equivalent. (a) For a conventional eight-path filter, the signals at $f_{\rm clk}$ and $3f_{\rm clk}$ are downconverted and then upconverted to RF input resulting in harmonic responses. (b) In the proposed HR-8PF, the harmonic downconversion from $3f_{\rm clk}$ is rejected by the effective LO, and the harmonic responses are improved. (Note that the gain and bandwidth of the HR-8 PF is different from conventional 8 PF.)

folded from clock harmonics, which is

$$\mathrm{HFRR}_i = \frac{\mathrm{sinc}\left(\frac{\pi}{N}\right)}{\mathrm{sinc}\left(\frac{i\pi}{N}\right)}, \quad (i = kN - 1, k \in \mathbf{Z}). \tag{2}$$

Since the RF signal is downconverted to the baseband capacitor, the NPF can also be used as a downconverter. The downconverting of unwanted RF signals at clock harmonics is called harmonic downconversion, which reduces the SNR for the desired signal. Also, the blockers at clock harmonics can be amplified, and saturate the baseband circuits. The HRR is the ratio of the conversion gain for the desired signal to that for the signals at clock harmonics, which is

$$\mathrm{HRR}_i = \frac{\mathrm{sinc}\left(\frac{\pi}{N}\right)}{\mathrm{sinc}\left(\frac{i\pi}{N}\right)}, \quad (i = \mathrm{odd}). \tag{3}$$

In the NPF, harmonic folding can be reduced by using more paths. Compared to a four-path filter, in an eight-path, the harmonic folding from the third and fifth clock harmonics filter is reduced (see Fig. 2); however, the harmonic response is worse than that of a four-path filter. The HA3 of an eight-path filter is only around 4 dB, which is much higher than the 19-dB HA3 in a four-path filter, and can reduce the blocker tolerance at that clock harmonic. Moreover, the HR3 of an eight-path filter is only 2 dB, which is worse than the 10-dB HR3 in a four-path filter.

In our proposed HR-8PF (see Fig. 1 (right)], the harmonic folding is improved by employing more paths, and the harmonic response and the harmonic downconversion are also improved. For a wideband receiver with a frequency range of 0.2–1 GHz, the HR-8PF improves the blocker tolerance at clock harmonics across the whole frequency range, since the seventh-order harmonic for the lowest clock frequency 0.2 GHz is 1.4 GHz, which is out of the desired input frequency range.

B. Analysis of the Harmonic-Rejecting N-Path Filter

Fig. 3 shows the simplified operation of the NPF and the proposed HR-NPF. In a conventional eight-path filter with an LNA, the RF signal is first downconverted to the baseband capacitors and then upconverted back to the LNA output, as shown in Fig. 3(a). The total frequency response consists of transfer functions due to the fundamental of the clock $H_1(f)$, third-order harmonic of the clock $H_3(f)$, and finite ON-resistance $H_{\rm SW}(f)$. In the proposed HR-8-path filter, the third-order clock harmonic is rejected during downconversion by combining the outputs of 3 LNAs with scaled transconductance [see Fig. 3(b)]. Thus, the filter transfer function due to the third-order clock harmonic $[H_3(f)]$ is removed, and the HA is limited only by switch $R_{\rm ON}$.

To calculate the transfer function of the HR-NPF, we use the similar approach in [7]. Fig. 4(a) shows a differential harmonic-rejecting eight-path filter (HR-8PF). The switches driven by p_i and p_{i+4} share the same baseband capacitor to eliminate the even-order harmonic responses [6]. To analyze the transfer function $V_{rf,k}/V_{\rm in}$, the LNAs are modeled as transconductor (gm) values with finite output impedance and $\mathrm{gm_k} = \mathrm{gm} \cdot \cos(\mathrm{k}\pi/4)$ $(\mathrm{k} = \{-1, 0, 1\})$, while the switches are modeled as ideal switches with finite ON-resistance. We first find the baseband voltage on one capacitor $C_{\rm bb}$ and then calculate the LNA output voltage using the superposition of $V_{\rm in}$ and $V_{{\rm bb},k}$.

gm with one switch can be modeled as a time-varying gm with finite output resistance, as shown in Fig. 4(b) [7], since in each time slot, only one switch is turned on for each gm. Since the switching function $\mathrm{SW_i}$ is

$$\mathrm{SW}_i(t) = \sum_{n=-\infty}^{+\infty} a_n e^{-j\frac{n\pi}{4}i} e^{jn\omega_{\rm clk}t} \tag{4}$$

where $a_n = sinc(n\pi/8)/8 \cdot exp(-jn\pi/8)$, the equivalent gm current with one switch [see Fig. 4(b)] in frequency domain

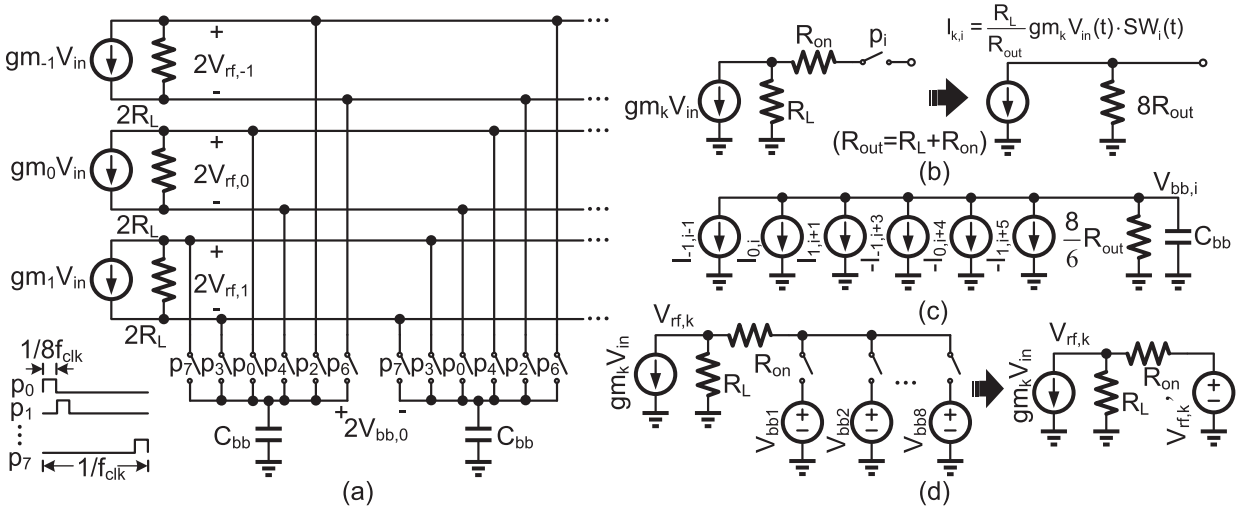

Fig. 4. (a) Differential HR-NPF with non-overlapping clocks. (b) Equivalent circuit of the LNA with a switch. (c) For one baseband capacitor, the currents from all the LNAs generate the baseband voltage $V_{\mathrm{bb},i}$. (d) All the baseband voltages are upconverted to the LNA output.

can be written as

$$I_{k,i}(\omega) = \frac{R_L}{R_{\mathrm{out}}} gm_k \sum_{n=-\infty}^{+\infty} a_n e^{-j\frac{n\pi}{4}i} V_{\mathrm{in}}(\omega - n\omega_{\mathrm{clk}}) \quad (5)$$

where $R_{\mathrm{out}} = R_L + R_{\mathrm{ON}}$. The RF current is downconverted to the baseband by the nth clock harmonic. The load resistor is $8 \cdot R_{\mathrm{out}}$, since the duty cycle of the clock is $1/8$. For each C_{bb}, the current from 6 gm values are summed up and generate the baseband voltage $V_{\mathrm{bb},i}$ shown in Fig. 4(c). The load resistor is $8/6 \cdot R_{\mathrm{out}}$. The baseband voltage is

$$V_{\mathrm{bb},i}(\omega) = [I_{-1,i-1}(\omega) + I_{0,i}(\omega) + I_{1,i+1}(\omega) - I_{-1,i+3}(\omega) - I_{0,i+4}(\omega) - I_{1,k+5}(\omega)] \cdot Z_{\mathrm{bb}}(\omega) \quad (6)$$

where Z_{bb} is the equivalent baseband impedance, which is $R_{\mathrm{bb}}/(1 + j\omega R_{\mathrm{bb}} C_{\mathrm{bb}})$ ($R_{\mathrm{bb}} = 4R_{out}/3$). The downconversion from even-order, third-, and fifth-order clock harmonic frequencies is rejected, since the gm values are scaled to the ratio of $0{:}1{:}\sqrt{2}{:}1{:}0{:}{-}1{:}{-}\sqrt{2}{:}{-}1$ in the different time intervals as in a harmonic rejection mixer. Since $\mathrm{gm_k} = \mathrm{gm} \cdot \cos(\mathrm{k}\pi/4)$, the baseband voltage can be derived as

$$V_{\mathrm{bb},i}(\omega) = \sum_{n=-\infty}^{+\infty} 4a_n e^{-j\frac{n\pi}{4}i} \frac{R_L}{R_{\mathrm{zout}}} gm V_{\mathrm{in}}(\omega - n\omega_{\mathrm{clk}}) Z_{\mathrm{bb}}(\omega), \times (n = 8l \pm 1, l \in \mathbf{Z}). \quad (7)$$

The output voltages of three LNAs can be considered as a superposition of the input gm and the upconverted $V_{\mathrm{bb},i}$ [see Fig. 4(d)]. The upconverted part $V'_{rf,k}$ is

$$V'_{rf,k}(\omega) = \sum_{m=-\infty}^{+\infty} \sum_{n=-\infty}^{+\infty} 32a_m a_n \frac{R_L}{R_{\mathrm{out}}} gm V_{\mathrm{in}} \times (\omega - (m+n)\omega_{\mathrm{clk}}) Z_{\mathrm{bb}}(\omega - m\omega_{\mathrm{clk}}) e^{j\frac{n\pi}{4}k} \times (m + n = 8q, m = \mathrm{odd}, n = 8l \pm 1, l, q \in \mathbf{Z}). \quad (8)$$

The desired signal frequency is $\omega_{\mathrm{clk}} + \omega_{\mathrm{bb}}$, so only the signals from $(1 - 8\mathrm{q})\omega_{\mathrm{clk}} + \omega_{\mathrm{bb}}$ will be folded into desired signal band. Since the third and fifth clock harmonics are rejected during downconversion, the HR-8PF does not have those harmonic responses. Ignoring the harmonic folding, the transfer functions for the kth LNA can be written as

$$\frac{V_{rf,k}(\omega)}{V_{\mathrm{in}}(\omega)} = \cos\left(\frac{k\pi}{4}\right) gm R_{on} || R_L + \left(\frac{R_L}{R_{\mathrm{out}}}\right)^2 \sum_{m=-\infty}^{+\infty} \times 32|a_m|^2 gm Z_{\mathrm{bb}}(\omega - m\omega_{\mathrm{clk}}) e^{-j\frac{m\pi}{4}k}, \ (m = 8l \pm 1, l \in \mathbf{Z}). \quad (9)$$

The transfer function only has bandpass filtering around $(8l \pm 1)\omega_{\mathrm{clk}}$; the third and fifth clock harmonic responses are rejected. Assuming the LNA output resistance is much larger than the switch ON-resistance ($R_L \gg R_{\mathrm{ON}}$), the bandwidth of the bandpass transfer function is $3/(2\pi R_L C_{\mathrm{bb}})$, the in-band (IB) gain is $128/3 \cdot |a_1|^2 gm R_L$, and the OB gain is $\sin(\mathrm{k}\pi/4)\mathrm{gm}R_{\mathrm{on}}$. Although the gm values in the three LNA branches are different, the IB gain of all the three branches is the same, since the gain is determined by the upconverted voltage $V'_{rf,k}$, and for each branch, $V'_{rf,k}$ has the same amplitude but a different phase shift. Compared with an NPF directly connected to the RF input, to achieve the same baseband bandwidth with the LNA, a smaller capacitor can be used resulting in a smaller chip area, since the LNA R_L is much larger than the 50-Ω RF source impedance. Additionally, larger OB attenuation can be achieved due to a larger R_L/R_{on} ratio.

The HR-NPF can be modeled as an RLC tank in series with R_{ON} as conventional NPF [5]. The equivalent RLC values are: $R_m = 32|a_1|^2 R_{\mathrm{bb}}$, $C_m = C_{\mathrm{bb}}/64|a_1|^2$, and $L_m = 1/(C_m \omega_{\mathrm{clk}}^2)$. Fig. 5(a) shows the calculated and behavioral-level simulated transfer function of the three LNA outputs [see Fig. 3(a)] as well as the RLC model for the middle LNA branch. The switches are driven by a 200-MHz eight-phase non-overlapping clock, and gm=30 mS, $R_L = 250\ \Omega$, $R_{\mathrm{ON}} = 1\ m\Omega$, and $C_{\mathrm{bb}} = 80$ pF. The simulated transfer

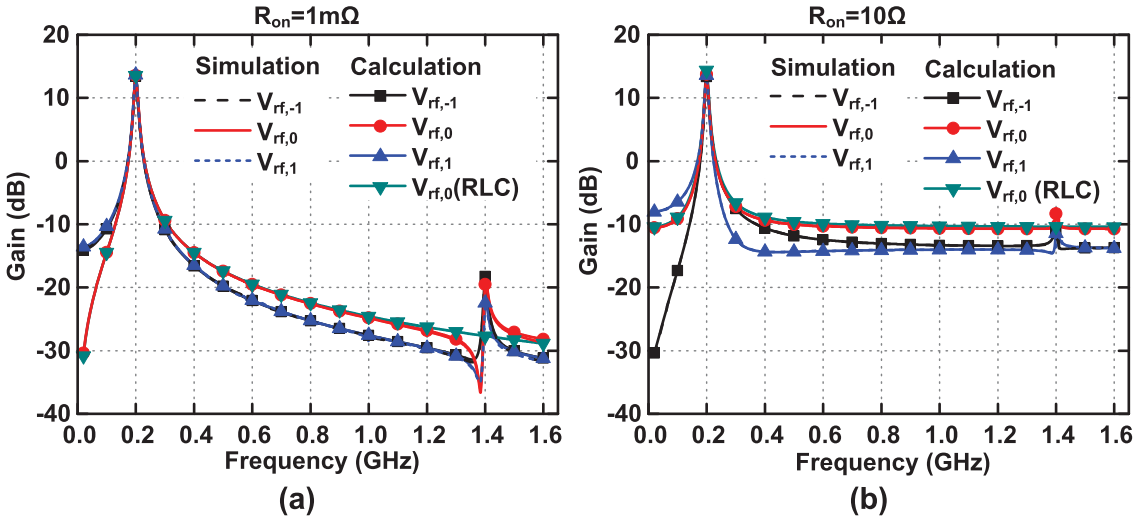

Fig. 5. Calculated [using (9)] and simulated transfer function of the HR-8PF with $R_{\rm ON}$ of (a) 1 mΩ and (b) 10 Ω.

function matches the calculation using (9) very well. The frequency response of the HR-8PF is very close to an *RLC* filter, and the center frequency is tunable. The difference of the different LNA outputs is caused by the phase shift in the upconverted voltage $V'_{rf,k}$.

To compare the HR-8PF [see Fig. 1(c)] with a conventional 8PF [see Fig. 1(b)], we assume that they have the same total LNA transconductance $\rm gm_{LNA}$, the LNA/sub-LNA load resistors of 8PF and HR-8PF are that $R_{L,LNA}$ and $3\rm R_{L,LNA}$, respectively, the baseband capacitors are $C_{\rm bb}$, the OB attenuation of the HR-8PF middle branch and 8PF is the same, and $R_{L,LNA} \gg R_{\rm ON}$. The sub-LNA in the middle branch of the HR-8PF has gm of $\rm gm_{LNA}/(1+\sqrt{2})$, and thus, the gain and $R_{\rm ON}$ of HR-8PF are $2/(1+\sqrt{2})$ and $1/(1+\sqrt{2})$ times that of the 8PF, respectively. The bandwidth of the HR-8PF is the same as 8PF. The LNA power of the two filters is the same, since they have the same gm. Assuming the clock generator power is proportional to the total switch capacitance and the capacitance of a switch is proportional to $1/R_{on}$, the clock generator power of the HR-NPF is $3/(1+\sqrt{2})$ times that of the 8PF.

C. Second-Order Effects

1) Finite Switch ON*-Resistance:* The finite switch ON-resistance limits the OB attenuation of the HR-NPF. The HR-8PF OB attenuation can be derived as $20\log(128|a_1|^2\rm R_L/[3R_{ON}\sin(k\pi/4)])$ for the kth LNA branch from (9). Fig. 5(b) shows the calculated and simulated transfer function of the HR-8PF with $R_{\rm ON} = 10\ \Omega$. The transfer curve of the LNA branch #−1 skews to the right, while that of the LNA branch #1 skews to the left at low frequency offset due to the phase shift in the upconverted voltage V'_{rf}. At larger frequency offset, the OB attenuation of those two branches is limited by the switch $R_{\rm ON}$ as expected.

2) Parasitic Capacitors: In a real circuit, the LNA and switches have parasitic capacitors. The switch capacitor at the baseband side can be considered a part of $C_{\rm bb}$. The parasitic capacitor at the output of the LNA will shift the filter center frequency and increase the IB loss as discussed in [7].

3) Mismatch Between the Branches: In an ideal HR-8PF, no RF currents around the third and fifth clock harmonics are downconverted to the baseband capacitors, and the harmonic responses are fully eliminated. However, in a real circuit, the cancellation of the harmonic components of the effective clock is limited by the gain and phase errors between the three branches. The finite $R_{\rm ON}$ also limits the HA. Defining $\rm HA'_{HR}$ as the HA (1σ) of the HR-8PF due to harmonic mixing and using the derivation in [13], $\rm HA3'_{HR}$ and $\rm HA5'_{HR}$ of an HR-8PF can be written as

$$\rm HA3'_{HR} = 3\frac{\sin^2\left(\frac{\pi}{8}\right)}{\sin^2\left(\frac{3\pi}{8}\right)}\left[\left(\frac{\sigma_A}{12}\right)^2+\left(\frac{\sigma_\phi}{4}\right)^2\right]^{-1/2}$$
$$\rm HA5'_{HR} = 5\frac{\sin^2\left(\frac{\pi}{8}\right)}{\sin^2\left(\frac{5\pi}{8}\right)}\left[\left(\frac{\sigma_A}{20}\right)^2+\left(\frac{\sigma_\phi}{4}\right)^2\right]^{-1/2} \quad (10)$$

where $\sigma_{\rm A}$ and σ_ϕ are the standard deviations of gain and phase errors. $\rm HA3'_{HR}$ is 30 dB for $\sigma_{\rm A} = 10\%$ and $\sigma_\phi = 3°$, which is better than the HA3 caused by a 10-Ω $R_{\rm ON}$ and a 250-Ω R_L (around 25 dB). Thus, the OB attenuation at the third- and fifth-order clock harmonics is mainly limited by the finite switch $R_{\rm ON}$ and can be as good as for other OB frequencies.

4) Clock Leakage: Generally, for an RF receiver, the asymmetric baseband circuit dc offset and charge coupling mainly generate the clock leakage [19]. Considering the circuit in Fig. 1(b) as a differential RF receiver with an eight-phase mixer, for the receivers using baseband TIA, the TIA input dc offset can be upconverted to $8f_{\rm clk}$ and its harmonics by the switches. However, if the dc offsets of each $V_{\rm bb}$ are not symmetric or the clock signal has mismatch, the clock leakage will appear at $f_{\rm clk}$. The clock charge injection is caused by the parasitic capacitor between the clock trace and the RF trace. It generates clock coupling due to the asymmetric parasitic capacitor or the clock signal mismatch.

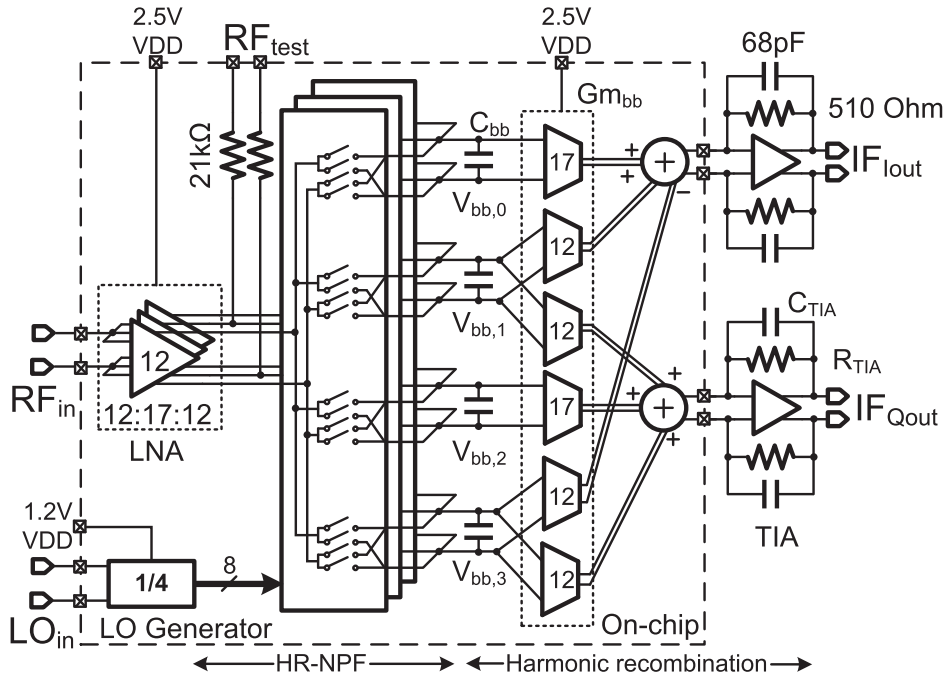

Fig. 6. Architecture of the blocker-tolerant RF front end.

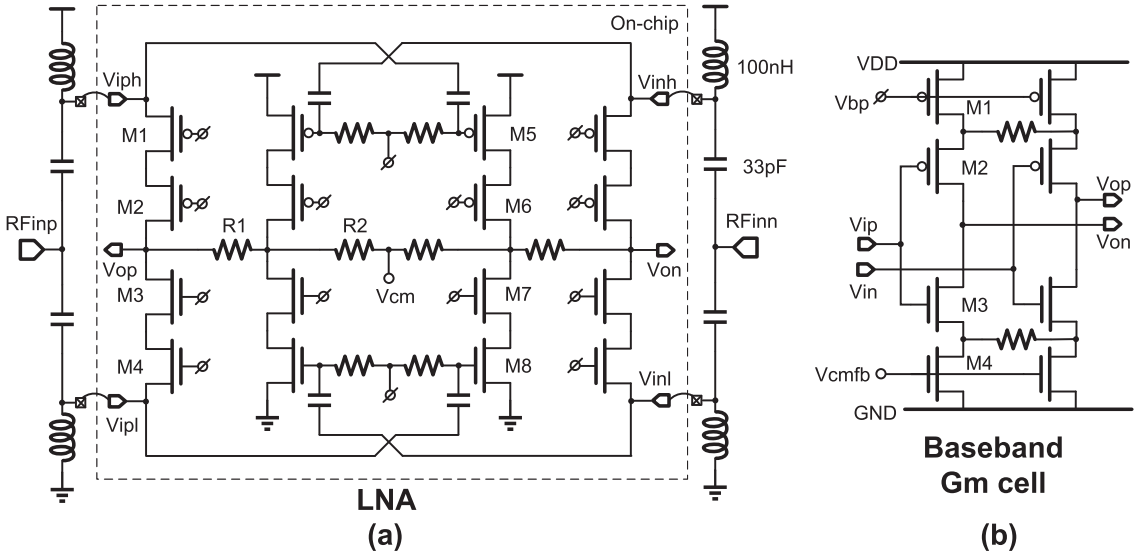

Fig. 7. Schematic of (a) LNA and (b) baseband gm cell.

In this paper, the baseband capacitors are connected to the gate of gm cells, and gm is biased by the LNA outputs. Thus, the dc offset of the gm cell input is much smaller than TIA. To reduce the clock charge injection, the clock traces should not overlap with the RF traces in the layout, thereby reducing the parasitic capacitance.

The reverse isolation of the LNA also helps to reduce the clock leakage. For the receivers using feedback LNA, the clock leakage is limited to around −80 dBm [20], since the feedback path limits the LNA reverse isolation. In this paper, noise-canceling LNA (NC-LNA) is used, and a cascode device helps to improve the reverse isolation.

III. RF Front End With Harmonic Rejecting N-Path Filter

A. RF Front-End Architecture

The architecture of the RF front-end prototype IC (see Fig. 6) consists of a broadband LNA with HR-NPF, baseband gm values, and an LO generator. All the switches in the HR-NPF are driven by eight-phase non-overlapping LO signals as the clock. The HR-NPF provides bandpass filtering with reduced harmonic responses at LNA outputs. Also, the RF signal is downconverted to the baseband capacitors in the HR-NPF with harmonic rejection. Since the downconverted voltage $V_{\mathrm{bb},i}$ has a phase shift $\exp(-\mathrm{j}n\pi\mathrm{i}/4)$ for the nth-order

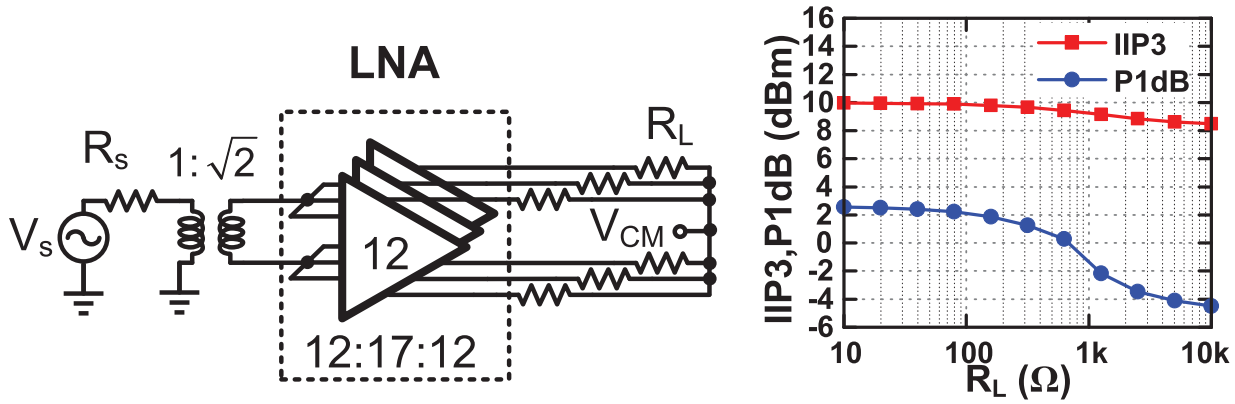

Fig. 8. Transistor simulated IIP3 and B1dB versus LNA load impedance for the LNA with a gm factor of 17.

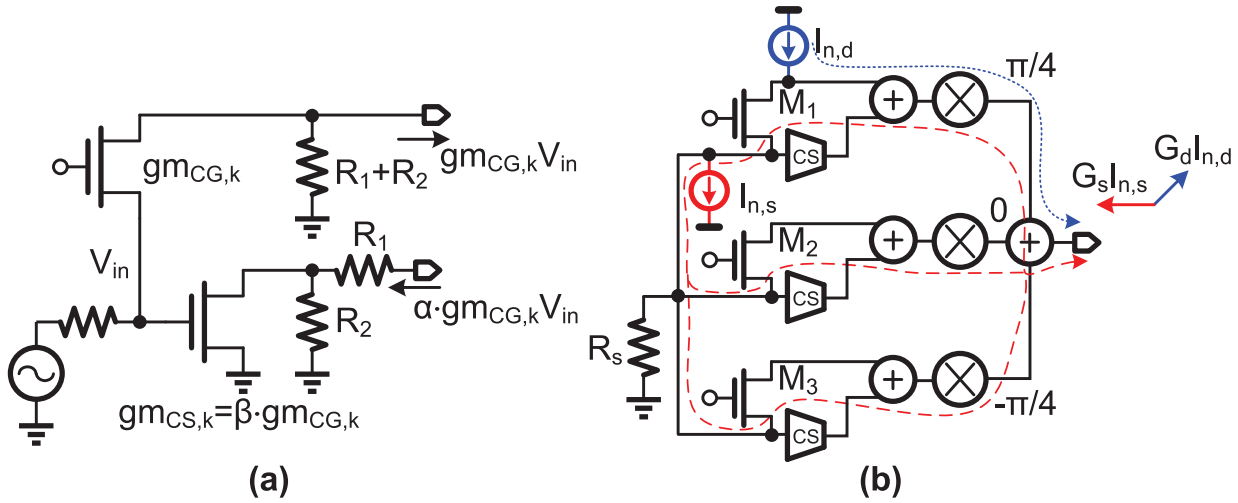

Fig. 9. (a) Simplified model of the NC-LNA. (b) Noise canceling in a harmonic-rejection mixer.

LO downconversion, the baseband gm values combines the baseband voltages with the gm factor of $\sin(i\pi/4)$ to realize a two-stage harmonic rejection architecture [13] and form in-phase and quadrature currents that drive off-chip TIAs. The conversion gain of the front end is

$$\mathrm{CG} = \frac{V_{\mathrm{IF}}}{V_{\mathrm{in}}} = \frac{\left(V_{\mathrm{bb},i-1}/\sqrt{2} + V_{\mathrm{bb},i} + V_{\mathrm{bb},i+1}/\sqrt{2}\right) gm_{\mathrm{bb}} R_{\mathrm{TIA}}}{V_{\mathrm{in}}} = \frac{4}{3}\mathrm{sinc}\left(\frac{\pi}{8}\right) gm R_L gm_{\mathrm{bb}} R_{\mathrm{TIA}} \quad (11)$$

where gm is the transconductance of the LNA and $\mathrm{gm_{bb}}$ is the transconductance of baseband gm both with a gm factor of 1, R_L is the LNA load resistance, and R_{TIA} is the feedback resistance in the TIA. The ideal $1:\sin(\pi/4)$ gm ratio is approximated as 17:12 in the LNA and baseband gm values. Generally, the HRR of a receiver is limited by the gain error of the gm and the LO phase error. In the two-stage harmonic rejection approach, the overall relative gain error is the product of the relative errors for the LNA and baseband gm values [13]. The gain error is negligible and the HRR is limited by the LO phase error, so that a high HRR can be achieved. Compared with HRR calibration techniques [12], two-stage harmonic rejection can achieve high HR3 and HR5 simultaneously. The HRR further helps to reduce the mixer noise figure (NF) thanks to the reduction of noise folding.

B. Circuit Implementation

Fig. 7(a) shows the schematic of the fully differential LNA, which is split into three sections with the relative sizes of 12:17:12. All sections are joined together at the inputs. M_1–M_4 is a current-reuse common-gate (CG) stage and M_5–M_8 is a current-reuse common-source (CS) stage. The total gm of the CG stage is 20 mS to achieve the 50-Ω impedance matching at each input. Current reuse improves the current efficiency and the gm ratio of the CS and CG branches is 4:1 to achieve a low NF. The CG stages are biased with off-chip inductors to avoid the noise contribution of an active current-source bias. The load resistor ratio is $R_1 : R_2 = 3 : 1$ and $R_1 + R_2$ is around 472 Ω. The output common mode is maintained at $V_{\mathrm{DD}}/2$ with an external regulator. The supply can vary from 1.8 to 2.5 V, and the cascode transistors guarantee a voltage drop smaller than 1 V across each device at 2.5 V so that thin-oxide transistors can be used. The baseband capacitors C_{bb} (see Fig. 6) have an effective 60-pF

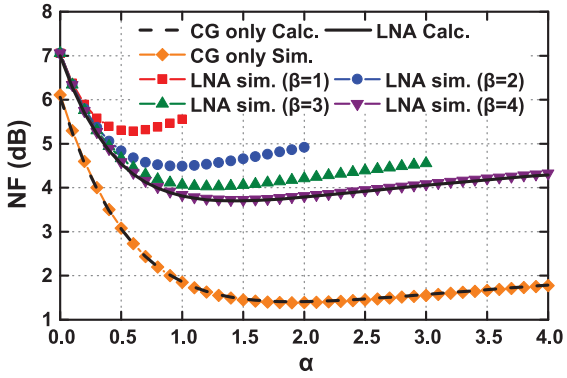

Fig. 10. Calculated and behavioral-level simulated front-end NF with noisy LNA versus factor α.

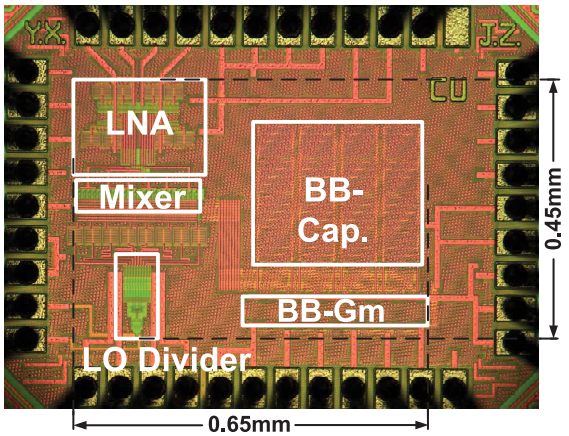

Fig. 11. Chip photograph.

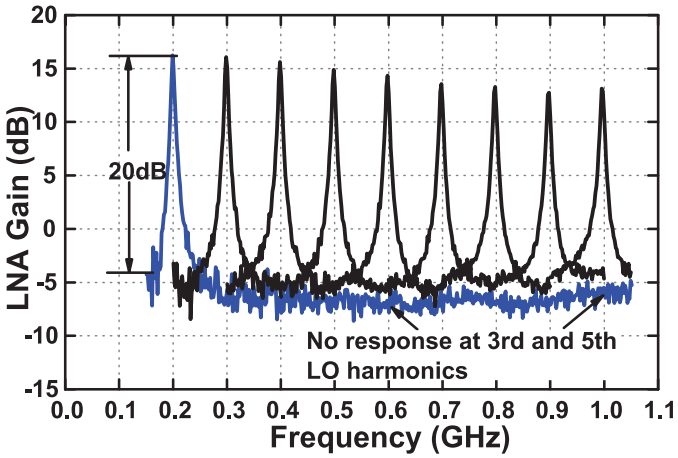

Fig. 12. LNA transfer function measured at RFtest for LO frequencies swept from 0.2 to 1 GHz with a 0.1-GHz step.

singled-ended capacitance and are realized with differential MIM capacitors and single-ended MOS capacitors.

The differential baseband gm [see Fig. 7(b)] also uses current-reuse and can operate from 1.8 to 2.5 V. M_2 and M_3 are the input transistors with resistive source degeneration to improve linearity. M_1 is a PMOS current source, while a common-mode feedback (CMFB) circuit drives the NMOS current source transistor M_4 to maintain the output common-mode voltage at $V_{DD}/2$. To ensure the common-mode voltage tracks $V_{DD}/2$ during power up, a soft-start LDO is used, and the LDO output ramp speed is lower than the speed of the CMFB circuit.

The LNA, switches, and gm cells are dc coupled[1] (see Fig. 6) to achieve higher OB linearity at low RF frequencies as in [12]. The dc coupling sets the source/drain voltage of the switch transistors to the LNA and gm common mode, i.e., $V_{DD}/2$, which can be as high as 1.25 V. The NMOS switch transistors are placed in a deep n-well and their body and source are connected together to keep source, drain, and body at the same dc voltage. The 1.2-V_{pp} LO signal is ac coupled to the gates of the switches, and the gate bias voltage is $V_{DD}/2$. The voltage drop across all transistor terminal pairs is then not larger than the supply voltage (1.2 V) of the LO signal, and thin-oxide switch transistors can be used. The ON-resistance of each switch is around 14 Ω.

C. Improvement of Out-of-Band Linearity

The HR-NPF improves the OB linearity of the receiver front end, since it has low OB gain before the baseband circuit and it reduces the voltage swing at the LNA output to improve the LNA linearity. The cascade IIP3 for a receiver is $1/A^2_{IIP3,tot} = 1/A^2_{IIP3,LNA} + G^2_{LNA}/A^2_{IIP3,BB}$ [21]. For the IB linearity, the baseband circuit is the bottleneck due to the large LNA gain. With the HR-NPF, the OB gain at the baseband capacitor is already reduced (see Fig. 6), and the harmonic downconversion from the third- and fifth-order LO harmonics is also rejected; thus, the baseband circuit will not limit the OB linearity, so that the LNA linearity becomes the bottleneck. The low OB impedance of the HR-NPF also helps to improve the LNA output linearity. Fig. 8 shows the transistor-level simulated IIP3 and P1dB versus load impedance for the LNA in Fig. 7(a). The LNA is driven by a port with a $1:\sqrt{2}$ balun, and the linearity is measured at the differential outputs of the LNA branch with a gm factor of 17. The small signal linearity (IIP3) and the large signal linearity (P1dB) are both improved with lower LNA load impedance, as shown in Fig. 8(b). The P1dB improves more than the IIP3 with lower impedance, since the LNA output will be clipped with a large input signal and high voltage.

D. Noise Analysis

NC-LNAs [22], [23] are widely used to achieve a low noise by canceling the noise from their CG transistor. However, if we split the NC-LNA into several branches to achieve the harmonic rejection, the CG noise cannot be fully canceled. In this section, we analyze the NC-LNA [see Fig. 7(a)] in the harmonic-rejection receiver front end (see Fig. 6). The simplified circuit of the kth branch of the LNA is shown in Fig. 9(a). $gm_{CG,k}$ and $gm_{CS,k}$ are the transconductances of the CG and CS branch, and $gm_{CG,k} = gm_{CG} \cdot \cos(k\pi/4)/\sum_{i=-1}^{1} \cos(i\pi/4)$

[1]However, when using dc coupling, the LNA IM2 products and flicker noise may leak to into baseband circuits.

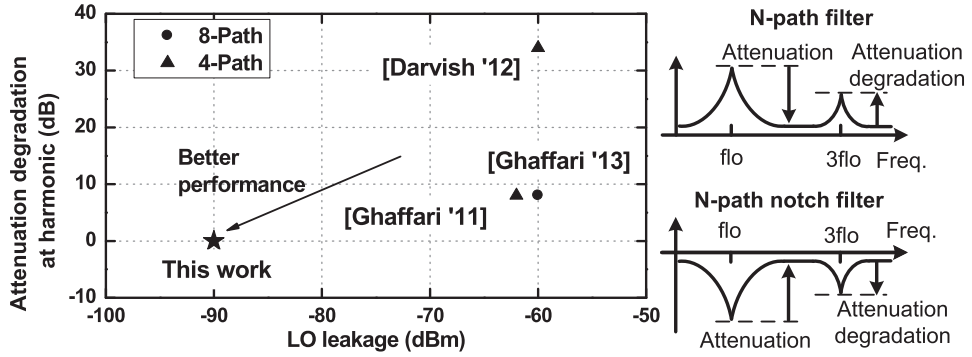

Fig. 13. HA performance compared with other NPFs.

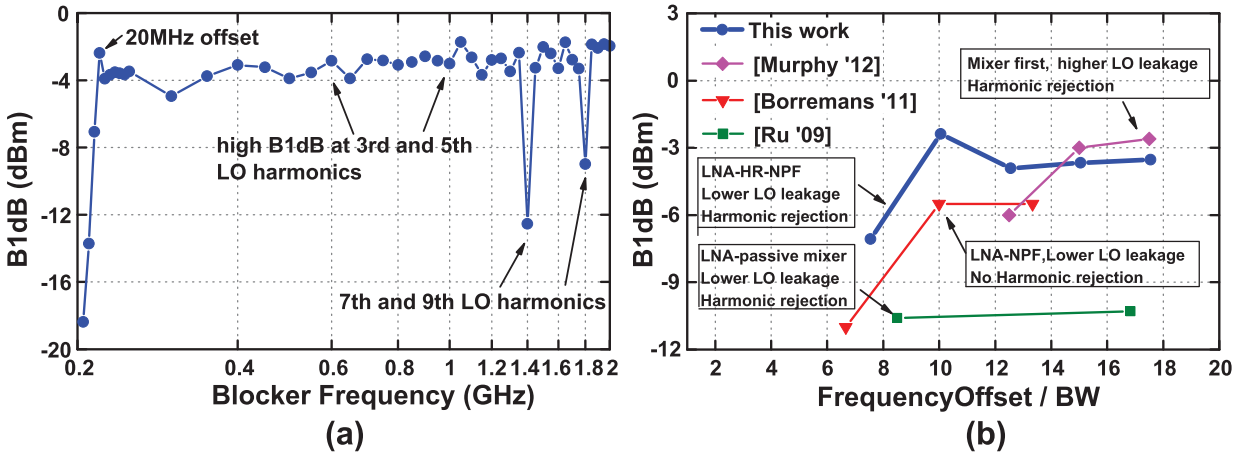

Fig. 14. (a) Measured blocker 1-dB compression point (B1dB) versus blocker frequency for an LO frequency of 0.2 GHz. (b) B1dB versus relative blocker frequency offset compared with other blocker tolerant RXs.

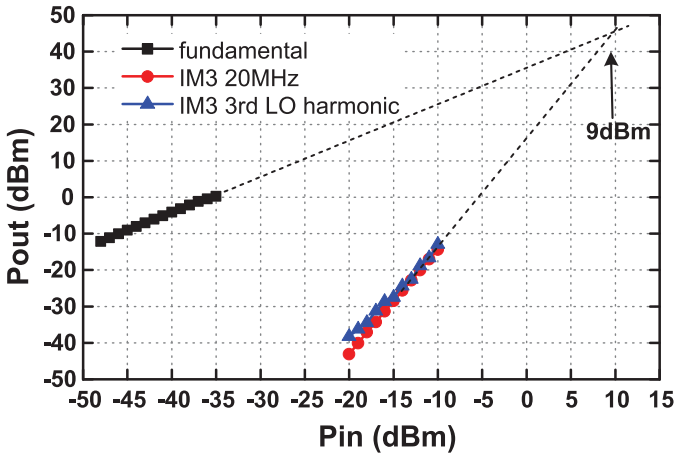

Fig. 15. Measured out-of-band IIP3 for the OB signal located at the 20-MHz offset and third-order LO harmonic.

and $\mathrm{gm_{CS,k}} = \beta \mathrm{gm_{CG,k}}$. The output currents of these two branches are $\mathrm{gm_{CG,k}V_{in}}$ and $\alpha \mathrm{gm_{CG,k}V_{in}}$, where $\alpha = \beta \mathrm{R_2}/(\mathrm{R_1} + \mathrm{R_2})$. Thus, the conversion gain can be written as $\mathrm{CG} = 2/3 \cdot \mathrm{sinc}(\pi/8)(1+\alpha)\eta_{\mathrm{gm}} \cdot \mathrm{gm_{CG}} R_L g m_{\mathrm{bb}} R_{\mathrm{TIA}}$, where η_{gm} indicates the gm efficiency, and $\eta_{\mathrm{gm}} = 2/(1+\sqrt{2})$, since all the $\mathrm{gm_k}$ values are combined as phasors after down-conversion, and $R_L = R_1 + R_2$.

The double-sideband (DSB) noise factor (F) due to R_s is $\mathrm{F_{Rs}} = 1/\mathrm{sinc}^2(\pi/8)$, since the noise from $(8l \pm 1)$th LO harmonics is folded into desired signal band and $\sum_{i=-\infty}^{\infty} sinc^2(i\pi/8) = 2$ $(i = 8l \pm 1)$. The CS transistor mean-square noise currents from different LNA branches are combined as scalars, since those noise sources are independent, and the output noise due to the LNA only has the noise folding from the $(8l \pm 1)$th LO harmonics thanks to the baseband harmonic recombination. Since $V_{n,CS}^2 = 4kT\gamma\, gm_{CS}(\alpha/\beta)^2(2/3 \cdot R_L g m_{\mathrm{bb}} R_{\mathrm{TIA}})^2 \cdot 2$, the additional DSB noise factor due to the CS stage is

$$F_{\mathrm{CS}} - 1 = \frac{1}{\beta}\left(\frac{2\alpha}{(1+\alpha)\eta_{gm}}\right)^2 \gamma \frac{1}{\mathrm{sinc}^2(\frac{\pi}{8})}. \tag{12}$$

The CS stage noise can be easily improved by increasing the gm ratio of CS and CG transistors β.

Using a similar analysis, the additional DSB noise factor due to the LNA load resistor is found to be $F_{\mathrm{RL}} - 1 = [2/(1+\alpha)/\eta_{gm}]^2 3R_L/R_s/sinc^2(\pi/8)$. Assuming a given LNA gain, $A = (1+\alpha)gm_{CG}R_L$, the noise factor can be written as

$$F_{\mathrm{RL}} - 1 = \frac{1}{A} \cdot \frac{12}{(1+\alpha)\eta_{gm}^2} \frac{1}{\mathrm{sinc}^2\left(\frac{\pi}{8}\right)}. \tag{13}$$

TABLE I
BREAKDOWN OF THE TRANSISTOR-LEVEL SIMULATED NOISE CONTRIBUTION

	R_s	CS stage	CG stage	R_L	Baseband Gm	Others
Noise Contribution	34.3%	11.1%	15.8%	20.6%	15.6%	2.6%

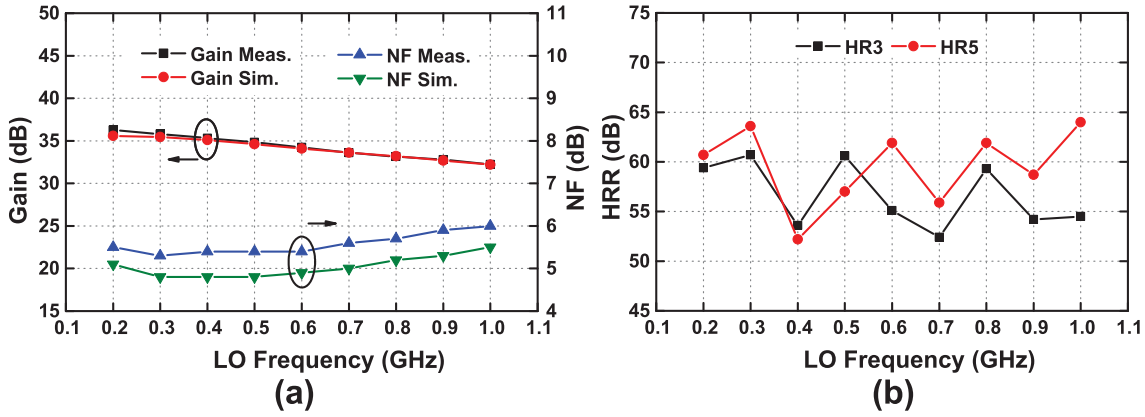

Fig. 16. (a) Measured and simulated conversion gain and NF. (b) Measured HRR versus LO frequencies.

The load resistor noise can be improved by increasing the LNA gain.

To analyze the CG noise contribution, we split the noise source into two current sources ($I_{n,d}$ and $I_{n,s}$), as shown in Fig. 9(b), and then calculate the output noise voltage from these two sources. $I_{n,d}$ is only transferred to the output by the mixer in one LNA branch, while $I_{n,s}$ is transferred to the output through all the branches. Thus, the output voltages $G_d I_{n,d}$ and $G_d I_{n,s}$ are not out-of-phase in the upper and lower LNA branches shown in Fig. 9(b), and the CG transistor noise cannot be fully canceled by tuning the gain of CS stage. The DSB noise factor due to CG transistors can be written as

$$F_{\mathrm{CG}}-1 = \left(\frac{2}{(1+\alpha)\eta_{gm}}\right)^2 \sum_{i=-1}^{1} \xi_i \left|\eta_{gm}\frac{1+\alpha}{2} - e^{-j\frac{i\pi}{4}}\right|^2 \gamma \frac{1}{\mathrm{sinc}^2(\frac{\pi}{8})} \tag{14}$$

where $\xi_i = cos(i\pi/4)/\left[\sum_{i=-1}^{1} cos(i\pi/4)\right]$ is the ratio of gm in the ith CG branch to the total gm in the CG stage. Since η_{gm} is also a constant, the NF due to the CG stage ($\mathrm{NF_{CG}}$) is only a function of α, which is the output current ratio of CS and CG stages. $\mathrm{NF_{CG}}$ versus α is shown in Fig. 10. The optimal $\mathrm{NF_{CG}}$ is not 0G, which indicates that the noise from the CG stage cannot be fully canceled. However, compared with the $\mathrm{NF_{CG}}$ without noise cancellation ($\alpha = 0$), the $\mathrm{NF_{CG}}$ with noise cancellation ($\alpha = 1.9$) is improved by 4.6 dB. To fully cancel the CG noise, we can remove M_1 and M_3 in Fig. 9(b) and only use M_2 to achieve the impedance matching, and then rescale the CS stages to achieve the harmonic rejection.

Considering $\eta_{\mathrm{gm}} = 0.828$, the total DSB noise factor of the front end due to R_s and NC-LNA can be written as

$$F = \left(1+\frac{1}{\beta}\cdot\frac{5.8\alpha^2\gamma}{(1+\alpha)^2} + \frac{5.8\sum_{i=-1}^{1}\xi_i\left|0.41(1+\alpha)-e^{-j\frac{i\pi}{4}}\right|^2\gamma}{(1+\alpha)^2} + \frac{1}{A}\cdot\frac{17.5}{(1+\alpha)}\right)\frac{1}{\mathrm{sinc}^2\left(\frac{\pi}{8}\right)}. \tag{15}$$

The NF lower limit is 1.4 dB, when $\beta = \infty$, $A = \infty$, and $\alpha = 1.9$. For a given LNA gain, the NF is a function of α and β. The calculated and behavioral-level simulated front-end NF versus α with different values of β for a noisy LNA is shown in Fig. 10 with $A = 19$ and $\gamma = 1$. The NF can be improved by increasing the ratio of the CS and CG stage (β). For the $\beta = 4$ condition, the optimal α is 1.4, and the minimum NF is 3.7 dB. In this paper, $\alpha = 1$ is used resulting in a 3.8-dB NF, which is close to the optimal value and 3.2 dB better than the

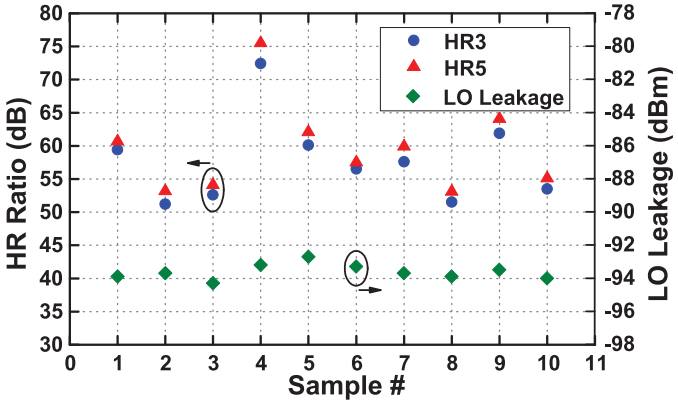

Fig. 17. Measured HRR with a 0.2-GHz LO and LO leakage with 1-GHz LO for ten samples.

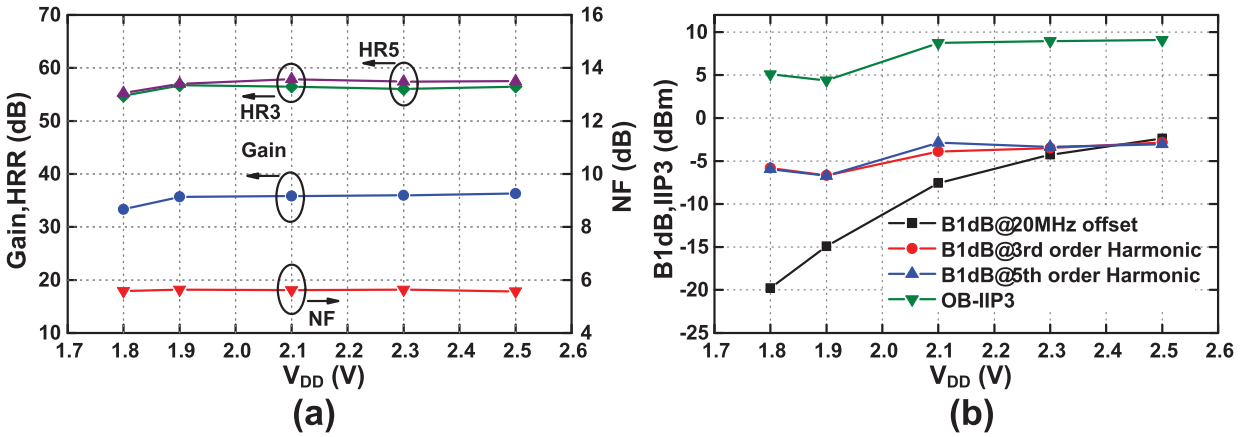

Fig. 18. (a) Gain, NF, and HRR and (b) OB-IIP3, OB-B1dB versus V_{DD} measurement with a 0.2-GHz LO.

NF without noise cancellation, which is 7 dB. The transistor-level simulated NF of the receiver, including the baseband gm, is 4.8 dB for a 0.4-GHz LO. The noise contribution breakdown for the simulation is shown in Table I.

IV. Experimental Results and Comparison

The chip was fabricated in a 65-nm CMOS process and the active area is 0.65×0.45 mm^2 (see Fig. 11). Typical measurements are done with a 2.5-V analog/RF supply to achieve maximal linearity and a 1.2-V LO supply. The performance for different analog/RF V_{DD} values between 1.8 and 2.5 V has also been measured. The measured S11 of each RF input is below -10 dB in the frequency range of 150 MHz–1.7 GHz. The remaining measurements have been done with an off-chip 180° hybrid driving the differential RF inputs, and the hybrid loss was calibrated out. The LNA output can be measured through the RF test output shown in Fig. 6, and the loss due to the resistor between LNA output and test output has been calibrated out in the measurement. The measured LNA transfer function (see Fig. 12) shows the effect of the HR-NPF; the different traces are for LOs from 0.2 to 1 GHz, spaced at 0.1 GHz [2]; the trace for an LO of 0.2 GHz shows an OB attenuation of around 20 dB and illustrates that there are no harmonic responses at the third and fifth LO harmonics, which are 0.6 and 1 GHz, respectively. The LNA, baseband gm, and LO generator consume 12 mA, 12 mA, and between 2 and 8 mA, respectively.

Fig. 13 shows the HA performance compared with various NPFs [5], [3], [24]. The attenuation degradation at the LO harmonics shows the difference between the attenuation at the third-order LO harmonic frequency and other OB frequencies. In contrast to the earlier work, the presented HR-NPF achieves high HA with low LO leakage and has zero degradation, which means that the OB rejection is flat around the third-order LO harmonic.

The B1dB versus blocker frequency was measured with an LO frequency of 0.2 GHz and an IB signal at 0.201 GHz, as shown in Fig. 14(a), since the worst case scenario for harmonic responses to blockers occurs for the lowest RF input frequency. For a blocker at a frequency offset of only 20 MHz, the B1dB is -2.4 dBm and the B1dB remains high at the third and fifth LO harmonics. The B1dB also remains high beyond the 1-GHz RF bandwidth of the front end. Only at the OB, LO harmonics at 1.4 GHz (seventh) and 1.8 GHz (ninth) is the B1dB reduced, but the interference from those harmonic frequencies can be filtered with an off-chip RF low-pass filter with a fixed bandwidth. Fig. 14(b) shows the B1dB for low frequency offsets compared with other blocker-tolerant receivers [11], [13], [25]. Frequency offset/intermediate frequency bandwidth (IFBW) is used as the x-axis to normalize the comparison, since the receiver bandwidths are all different. For [11], the BW after LNA and B1dB at low gain has been plotted for best performance. This paper achieves a higher B1dB at low frequency offsets thanks to the HR-NPF and high V_{DD}. The OB-IIP3 (see Fig. 15) is 9 dBm for an LO of 0.2 GHz. The OB-IIP3 at low frequency offset (two tones: 0.221 and 0.241 GHz) and at LO harmonics (two tones: 0.401 and 0.601 GHz) are nearly the same.

The gain, NF, and HR3 and HR5 versus LO frequency are shown in Fig. 16. The gain is 36 dB at 0.2 GHz and reduces to 32 dB at 1 GHz. The front-end NF is 5.5 dB at 0.2 GHz and 6 dB at 1 GHz. The measured HR3 and HR5 are both better than 51 dB at any LO frequency. The harmonic rejection of ten samples was measured at 0.2 GHz (see Fig. 17); the minimum HR3 is 51 dB and minimum HR5 is 53 dB. Those HRRs are achieved without calibration. Fig. 17 also shows the LO leakage of ten samples with 1-GHz LO, and the LO leakages are all lower than -90 dBm.

The gain, NF, and HRR versus V_{DD} with a 0.2-GHz LO are shown in Fig. 18(a). Those performances change only a little when V_{DD} is changed, since both the LNA and baseband gm are current-biased. The linearity versus V_{DD} is shown in Fig. 18(b). With higher V_{DD}, the OB linearity is improved thanks to larger headroom at each amplifier output. The B1dB at 20 MHz is improved more, since at that frequency, the blocker attenuation is limited by the filter order, though the clipping at amplifier output still limits the large signal linearity when V_{DD} is low.

[2]The LNA RF bandwidth is limited by the large LNA output impedance.

TABLE II
COMPARISON WITH THE STATE OF THE ART

		N-path filter			Blocker tolerant RX				
	This work	Darvishi JSSC '12	Ghaffari JSSC '13	Darvishi JSSC '13	Murphy JSSC '12	Borremans JSSC '11	Ru JSSC '09	Limpd JSSC '14	Murphy JSSC '15
Technology	65nm	65nm	65nm	65nm	40nm	40nm	65nm	28nm	28nm
RF Input	Differential	Single-ended	Differential	Differential	Single-ended	Differential	Differential	Differential	Differential
Offchip Inductor	4	0	0	0	0	2	2	2	0
Frequency (GHz)	0.2-1	0.4-1.2	0.1-1.2	0.1-1.2	0.08-2.7	0.4-6	0.4-0.9	0.4-6	0.1-3.3
LO leakage (dBm)	<-90	<-60	<-60	<-64	NR	NR	NR	NR	NR
B1dB(dBm)	-2.4@20MHz -2.8@3flo	NR	NR	7@50MHz	-6@25MHz	-5.5@20MHz[a]	-10@100MHz	-12@80MHz	0.5@8MHz -6.5@3flo
OB-IIP3 (dBm)	9	29	NR	26	13.5	10	18	8	11.5
Gain (dB)	36	12	-1.4	25	70	70	34	70	NR
NF (dB)[e]	5.4-6	10	1.6-2.5	2.7-3.1	1.4-2.4	3-8	3.5-4.4	1.8-3.1	1.7
BW (MHz)	2	21	NA	8	2	0.4-30	12	0.5-50	0.2-3
HA3 of NPF (dB)	20	20	14[b]	NR	NA	NA	NA	NA	NA
HR3/5 (dB)	>51/>52	NA	NA	NA	42/45	NR	>60/>64	70/75[c]	60/60
VDD (V)	1.2/2.5	1.2/2.5	NR	1.2	1.3	1.1/2.5	1.2	0.9	1
Power (mA)	26-32[d]	15.6	3.5-30mW	15-48	27-60	30-55mW	41-50	44.4	36.8-62.4
Active area (mm^2)	0.29	0.127	0.14	0.27	1.2	2	1	0.6	5.2

NR: not reported, NA: not applicable
a. RF filtering BW 15MHz, 6dB lower than max gain. b. For notch filter attenuation difference between fundamental and 3rd order harmonics is used as HA. c. with calibration.
d. Analog 24mA, Digital (clock) 2-8mA. e. 1-dB typical input balun loss should be included for RXs with differential inputs.

The comparison with the state of the art is shown in Table II. This paper has lower LO leakage as compared with other works. The B1dB is −2.4 dBm at 20-MHz offset, and remains high at the LO harmonics. The receiver in [16] also achieves high B1dB at the LO harmonics, but it does not have harmonic rejection at the RF input, which makes the B1dB at the LO harmonics lower than at other OB frequencies.

In the conventional receiver with NPF, it is hard to achieve a high OB linearity at LO harmonics due to the NPF harmonic response [5], [3], [7]. The harmonic rejection at baseband is achieved in [12], [16], and [26], but those receivers have a harmonic response before the downconversion; thus, the OB linearity at LO harmonics is still not as good as at other OB frequencies. In this paper, the HR-NPF rejects the harmonic downconversion before the baseband gm and reduces the LNA load impedance at LO harmonic frequencies, such that high OB-IIP3 and B1dB at the third- and fifth-order LO harmonics are achieved.

V. CONCLUSION

An RF front end with harmonic-rejecting N-path filtering is proposed in this paper. The HR-NPF achieves large OB attenuation and high HA at the LNA outputs, and thus, the front end achieves high B1dB at both low offset frequencies and the third and fifth LO harmonics to make sure the front end can tolerate an OB blocker at any frequency in the 0.2–1 GHz frequency range. This paper also achieves less than −90-dBm LO leakage and high HRR without calibration.

ACKNOWLEDGMENT

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