0.293-mm^2 Fast Transient Response Hysteretic Quasi-V^2 DC–DC Converter With Area-Efficient Time-Domain-Based Controller in 0.35-μm CMOS

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***Abstract*— A time-domain-control-based quasi-V^2 buck converter with small area, fast transient response, wide load current range, and constant switching frequency is proposed in this paper. The proposed time-domain-based controller achieves compact core area and simplified constant switching frequency control by replacing the conventional voltage-domain comparator with a phase detector having an adaptive detection window. Moreover, a coupling-based inductor current emulator is also proposed to support the discontinuous conduction mode operation in the light load. The proposed buck converter is implemented using 0.35-μm CMOS process. The core area of the proposed buck converter is only 0.293 mm^2. The measured peak efficiency in the continuous conduction mode is 92% and the end-to-end efficiency in the load current range of 25–700 mA is 73%. The undershoot/overshoot and recovery time with the up/down load current steps of 510 mA are 38/20 mV and 2.5/2.6 μs, respectively.**

***Index Terms*— Coupling-based inductor current emulator (C-ICE), dc–dc buck converter, fast transient response, hysteretic quasi-V^2 control, time-domain-based controller.**

I. Introduction

THE performance requirements of power management integrated circuits (PMICs) for mobile devices, such as smartphones and tablets, are becoming more challenging owing to their diverse applications, increasing functionalities, and decreasing feature size. Thus, the demand for a high-performance buck converter, which is the core building block of a PMIC for a battery-powered device, is also increasing. In addition to the power conversion efficiency, fast transient response, wide load current range, constant switching frequency, low output voltage ripple, and small size are the required features of the high-performance buck converter.

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In recent application processors for mobile devices, the load current steps dynamically. Thus, a fast transient response with recovery time in the order of several microseconds and less than 5%–10% of supply voltage droop is required in the buck converter. Many control schemes, such as the minimum time [1]–[3], V^2 [4]–[7], V^2I_c [8]–[10], and quasi-V^2 [11]–[14] controls, have been proposed to satisfy the fast transient response requirement. A minimum time control requires high computing power for determining the optimum timing to control the power FETs. Thus, minimum time control requires many analog computing blocks [1] or is often digitally implemented using a field-programmable gate array (FPGA) [2], [3]. The V^2 control consists of two feedback loops: the feed-forward path (FFP) and error correction path (ECP). The FFP carries high-frequency information on the capacitor current. Consequently, the V^2 control can quickly react to a load disturbance. However, the conventional V^2 control suffers from stability issues when an output capacitor with small equivalent series resistance (ESR), such as a ceramic capacitor, is used [15]. The stability issue is addressed by sensing the capacitor current by differentiating the output voltage [6], [7] but differentiating noisy output voltage is tricky and requires a large design effort. The V^2I_c and quasi-V^2 controls have been proposed to solve the stability issues of the V^2 control caused by the low current sensing gain, i.e., the small ESR. Instead of sensing current using the ESR of the output capacitor, the V^2I_c and quasi-V^2 controls achieves high current sensing gain using the designated current sensor and current emulator, respectively. However, the additional current sensor in the V^2I_c control increases the area and power consumption, and complicates the controller design.

The structure of the conventional hysteretic quasi-V^2 buck converter is shown in Fig. 1. As mentioned above, the quasi-V^2 control is similar to the V^2 control except that the feedback signal for the FFP, V_F, is generated from the current emulator. The current emulator functions as a 1st-order RC low-pass filter that averages out $V_X - V_{\mathrm{OUT}}$ [11]. Therefore, the current sensor can sense the inductor current ripple as long as the cut-off frequency of the filter is smaller than the switching freuqency [16]. Moreover, since the current emulator is a lossless sensor [17], it does not affect the efficiency of the buck converter. Owing to these advantages of the

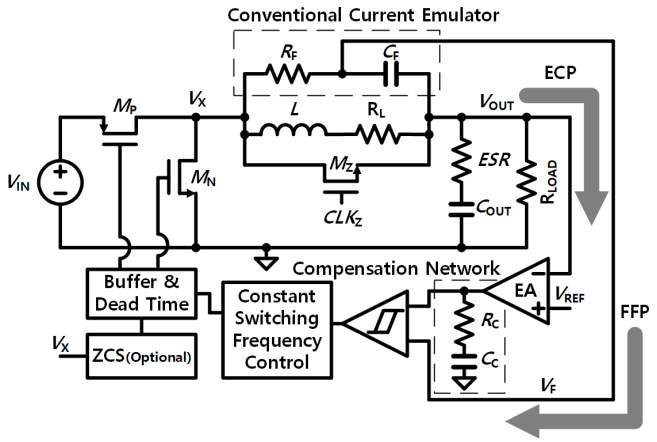


Fig. 1. Structure of the conventional hysteretic quasi-V^2 buck converter.

current emulator, many dc–dc converters with a current emulator have been proposed [10]–[14], [17]–[20]. However, the feedback paths of the conventional hysteretic quasi-V^2 buck converters are commonly designed in the voltage domain using an error amplifier (EA), comparator (COMP), and compensation network. The use of the EA and COMP results in static current consumption, vulnerability to variations, and larger area. Moreover, R_C and C_c in the compensation network are commonly very large. R_C and C_c were 5 kΩ and 4.7 nF, respectively, in [6] and 150 kΩ and 330 pF, respectively, in [11]. Therefore, the compensation network is often realized using off-chip components, which significantly increase the feature size and cost of a system.

On the other hand, the switching frequency variation in the hysteretic quasi-V^2 control is a significant issue because it makes the other building blocks in the system hard to control the electromagnetic interference (EMI) [21]. Thus, many constant switching frequency schemes have been proposed. In [18] and [22], a delay line was added in the feedback loop to fix the switching frequency. In [18], a control loop similar to a digital phase-locked loop (PLL) and a digitally controlled delay line (DCDL) were used. In [22], a voltage-controlled delay that inserts different delays at the rising and falling edges of a pulsewidth modulation (PWM) signal was added. However, the added delay lines increase the loop delay and degrade the transient response of the converter. Moreover, they require power- and area-consuming building blocks, such as a charge pump and loop filter. An adaptive on-time control was proposed to solve the switching frequency variation issue of constant on-time control in [12]. However, the immediate response to the load current step is limited in this scheme [9], which also degrades the transient response. In [13], [23], and [24], the hysteresis band of the COMP is adjusted to achieve constant switching frequency. Adjusting the hysteresis band does not cause an additional delay in the feedback loop. However, it requires a voltage-controlled resistor array [23] or digital-to-analog converter [24], or an additional control loop similar to PLL [13] is required to modulate the hysteresis band of the COMP. These building blocks are bulky and power hungry and can cause stability issues.

In this paper, a time-domain-control-based hysteretic quasi-V^2 hysteretic buck converter is proposed. The time-domain-based controller of the proposed buck converter significantly reduces the design complexity and core area, which make the integration of the converter easier. The constant switching frequency control is achieved by adjusting the hysteresis band as in [13], [23], and [24] but the controller configuration is simplified owing to the proposed time-domain-based control. In addition, in order to widen the load current range to the light load, a coupling-based inductor current emulator (C-ICE) is also proposed in this paper. The C-ICE supports more accurate zero current detection in the buck converter topology, which leads to the increase in the power conversion efficiency in the light load. The rest of this paper is organized as follows. The structure and operational details of the proposed buck converter are described in Section II and the implementation of the proposed buck converter is presented in Section III. The measurement results are given in Section IV and Section V gives the conclusion.

II. Proposed Time-Domain-Control-Based Hysteretic Quasi-V^2 Buck Converter

A. Structural Details

Fig. 2 shows the block diagram of the proposed buck converter. It contains a time-domain-based ECP and FFP, a phase detector with detection window (PDDW), C-ICE, frequency detector (FD), and clock generator with a zero current sensor (ZCS).

The time-domain-based ECP and FFP consists of two voltage-controlled delay lines (VCDLs) with low gain (VCDL-LG), two VCDLs with high gain (VCDL-HG), four multiplexers (MUXs) to support the continuous conduction mode (CCM) and discontinuous conduction mode (DCM) simultaneously, and three time amplifiers (TAs). The conventional voltage-domain-based ECP, which consists of an EA and compensation network, is replaced with two VCDL-HGs and three TAs. The VCDL-HGs delay $\mathrm{CLK_{EXT}}$ by an amount equivalent to the delay proportional to their input control voltages, V_{OUT} and V_{REF}. Thus, the voltage difference between V_{OUT} and V_{REF} is converted into the timing difference between the two outputs of the VCDL-HG. Subsequently, the timing difference is amplified by the three successive TAs. The high voltage-to-delay conversion gains of the VCDL-HGs and TAs offer sufficient gain to replace the EA in the voltage-domain ECP. On the other hand, the two VCDL-LGs add additional timing difference proportional to the difference between V_F and V_{REF}. The two VCDL-LGs function as the FFP in the conventional quasi-V^2 control. Thus, the proposed time-domain-based ECP and FFP functions in the same manner as the voltage-domain-based controller. The proposed time-domain-based controller makes the controller more area-efficient and lowers the design complexity.

The PDDW functions as the hysteretic COMP in the conventional quasi-V^2 control. It compares the timing difference between $\mathrm{CLK_{OUT}}$ and $\mathrm{CLK_{REF}}$, and generates a raw PWM signal ($\mathrm{PWM_{RAW}}$). In the proposed time-domain-based controller, the detection window of the PDDW functions as the hysteresis band of the conventional hysteretic COMP.

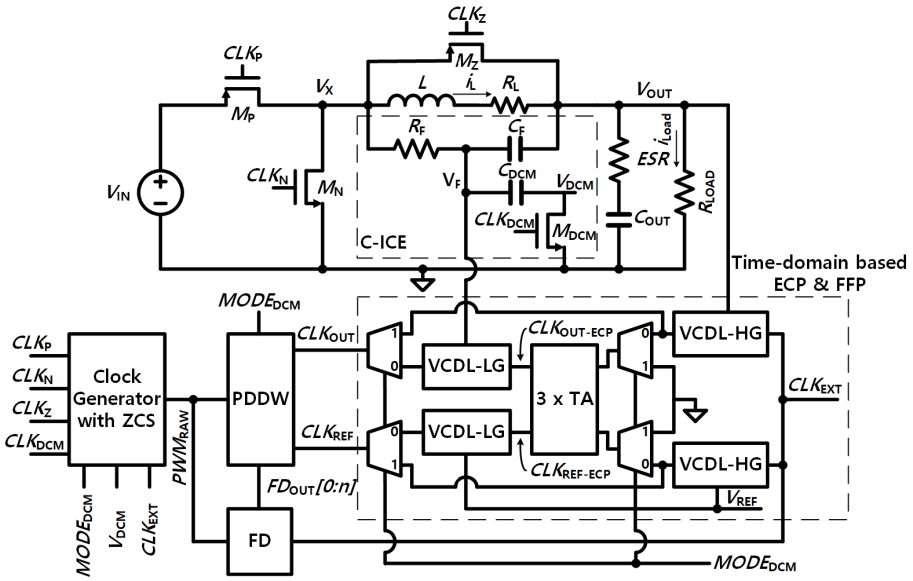


Fig. 2. Proposed hysteretic quasi-V^2 buck converter with a time-domain controller.

If the timing difference is larger than the detection window, $\mathrm{PWM_{RAW}}$ is set to HIGH or LOW depending on which one of $\mathrm{CLK_{REF}}$ or $\mathrm{CLK_{OUT}}$ leads the other. If the timing difference is within the detection window, $\mathrm{PWM_{RAW}}$ holds the state of the output as the conventional hysteretic COMP. The structural and operational details of the PDDW are described in Section III-C.

The size of the detection window of the PDDW is controlled by the output of the FD, $\mathrm{FD_{OUT}}$ [0:n], to fix the switching frequency. The FD is the counter-based time-to-digital converter as proposed in [23] and [24]. The switching frequency is detected by the number of counts made by the high-frequency clock, $\mathrm{CLK_{EXT}}$, during several periods of $\mathrm{PWM_{RAW}}$. The constant switching frequency control of the proposed structure is similar to the hysteresis band control method described in Section I. The details of the FD are described in Section II-C along with the constant switching frequency control of the proposed buck converter.

The C-ICE consists of a conventional current emulator C_{DCM} and M_{DCM} as shown in Fig. 2. Since V_F contains the information of the inductor current, it can be used to resolve the stability issues mentioned in Section I. In addition, the inductor current can successively be sensed under the variation on L because the inductor current sensing gain is L/R_FC_F [11]. However, V_F cannot be directly used in the zero current detection because the dc level of V_F follows the dc level of V_{OUT}. Thus, the proposed C-ICE couples the ripple of V_F to V_{DCM} using C_{DCM} and the zero current is detected from V_{DCM}. The additional details of the proposed C-ICE together with the operation of the DCM are described in Section II-D.

The clock generator with ZCS in Fig. 2 generates clock signals for M_P, M_N, M_Z, and M_{DCM}. M_P and M_N are the power FETs of the buck converter. M_Z is used to suppress the ringing of V_X in the DCM. M_{DCM} is used to hold V_{DCM} to ground (GND) when the operation of C-ICE ends. The structural and operational details of the clock generator with ZCS are described in Section III-D.

B. Operation Details of CCM

Fig. 3 shows the waveform of the proposed buck converter in the CCM. In the CCM, $\mathrm{MODE_{DCM}}$ is set to LOW. The clock generator with ZCS sets $\mathrm{CLK_{DCM}}$ to HIGH to hold V_{DCM} to GND and also sets CLK_Z to HIGH because ringing does not occur in the CCM. The switching frequency of the proposed buck converter (F_{SW}) is 2 MHz and the frequency of $\mathrm{CLK_{EXT}}$ is 100 MHz. As mentioned in Section III-A, $\mathrm{CLK_{EXT}}$ is delayed by the two VCDL-HGs and the timing difference between the outputs of the two VCDL-HGs is amplified by three successive TAs. The timing difference between the two outputs of TA (Δ_{ECP}) can be expressed as follows:

$$\Delta_{\mathrm{ECP}} = (V_{\mathrm{OUT}} - V_{\mathrm{REF}}) * K_{\mathrm{VCDL-HG}} * G_{\mathrm{TA}} \tag{1}$$

where $K_{\mathrm{VCDL-HG}}$ is the voltage-to-delay conversion gain of the VCDL-HG and G_{TA} is the timing difference amplification gain of the three TAs. Subsequently, $\mathrm{CLK_{OUT-ECP}}$ and $\mathrm{CLK_{REF-ECP}}$ are delayed by the two VCDL-LGs. The resultant timing difference between $\mathrm{CLK_{OUT}}$ and $\mathrm{CLK_{REF}}$ (Δ_{FFP}) can be expressed as follows:

$$\Delta_{\mathrm{FFP}} = \Delta_{\mathrm{ECP}} + (V_F - V_{\mathrm{REF}}) * K_{\mathrm{VCDL-LG}} \tag{2}$$

where $K_{\mathrm{VCDL-LG}}$ is the voltage-to-delay conversion gain of the VCDL-LG. PDDW generates $\mathrm{PWM_{RAW}}$ based on the following equation:

$$\mathrm{PWM_{RAW}} = \begin{cases} \mathrm{LOW} & \mathrm{If}\,\Delta_{\mathrm{FFP}} > D_{\mathrm{WIN}}/2 \\ \mathrm{HoldsOutput} & \mathrm{If}-D_{\mathrm{WIN}}/2 < \Delta_{\mathrm{FFP}} < D_{\mathrm{WIN}}/2 \\ \mathrm{HIGH} & \mathrm{If}-D_{\mathrm{WIN}}/2 > \Delta_{\mathrm{FFP}} \end{cases} \tag{3}$$

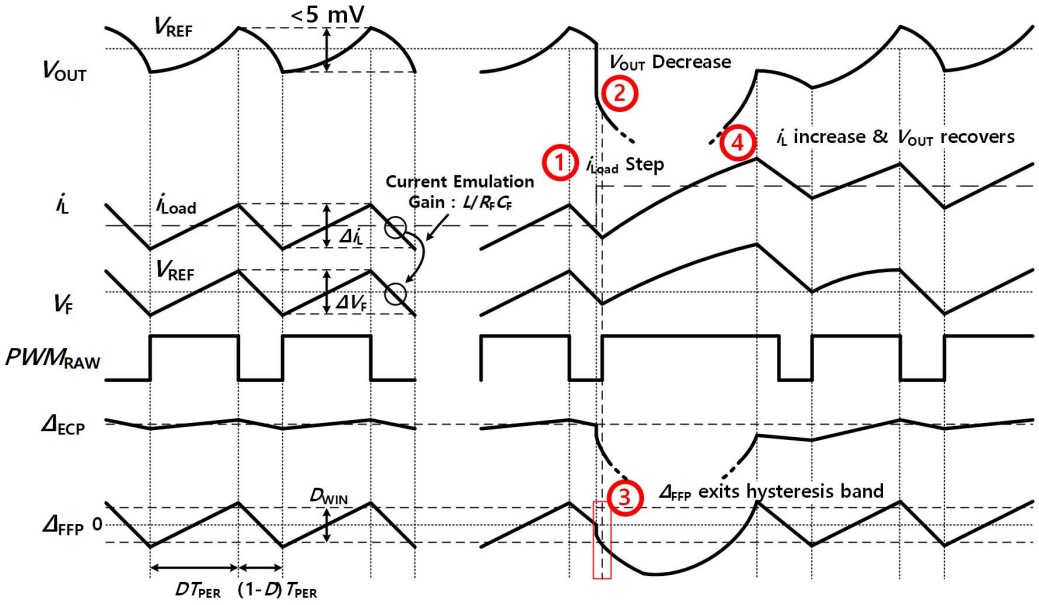


Fig. 3. Operational waveform of the proposed buck converter in the CCM.

where D_{WIN} is the size of the detection window of the PDDW. In the steady state of the proposed buck converter, Δ_{ECP} is very small because the difference between V_{OUT} and V_{REF} is maintained very small owing to the small ESR. Thus, the ripple of V_F, which indicates the inductor current, mainly determines Δ_{FFP}.

When the load current steps-up as shown in the right side of Fig. 3, V_{OUT} droops suddenly because of the ESR of the output capacitor [25]. Successively, the difference between i_L and increased i_{Load} decreases V_{OUT}. The sudden voltage droop and decrease in V_{OUT} result in the decrease of Δ_{ECP}, and consequently Δ_{FFP} becomes smaller than $-D_{\mathrm{WIN}}/2$ as shown in Fig. 3. Subsequently, M_P is turned on and i_L starts to increase. The large gain of VCDL-HG and the three TAs make the sufficient change Δ_{ECP} with the small decrease in V_{OUT}. In addition, Δ_{ECP} is updated at every 10 ns because the frequency of $\mathrm{CLK_{EXT}}$ is 100 MHz. As a result, the proposed time-domain-based ECP and FFP make fast transient response to the load current step.

C. Constant Switching Frequency Control

As briefly described, constant switching frequency is achieved by adjusting D_{WIN} based on the detection result of the FD. During the steady state of the CCM, the ripple of V_{OUT} is maintained small and therefore, Δ_{FFP} is dominantly determined by the ripple of V_F. Moreover, based on the operation in the CCM, Δ_{FFP} ranges from $-D_{\mathrm{WIN}}/2$ to $+D_{\mathrm{WIN}}/2$ as shown in Fig. 3. Therefore, D_{WIN} can be expressed as follows:

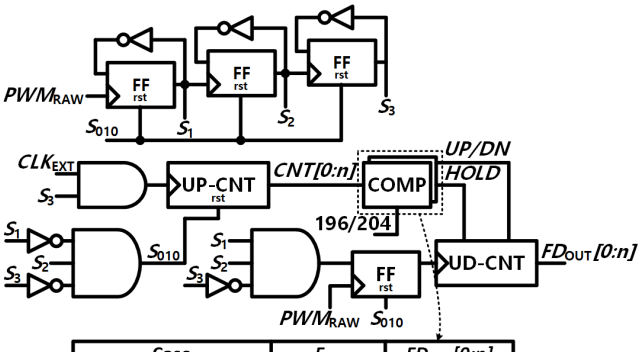
$$D_{\mathrm{WIN}} = \Delta V_F * K_{\mathrm{VCDL-LG}} = \Delta i_L * \frac{L}{R_F C_F} * K_{\mathrm{VCDL-LG}} \tag{4}$$

where ΔV_F and Δi_L are the amplitudes of V_F and i_L, respectively. From (4) and the relationship between the hysteresis band and switching frequency in [11] and [18], the switching frequency can be expressed as follows:

$$F_{\mathrm{SW}} = \frac{1}{T_{\mathrm{PER}}} = \frac{(1-D)\,D}{L}\frac{1}{V_{\mathrm{IN}}}\frac{1}{\Delta i_L} = \frac{D\,(1-D)\,V_{\mathrm{IN}} K_{\mathrm{VCDL-LG}}}{R_F C_F D_{\mathrm{WIN}}} \tag{5}$$

where T_{PER} and D are the period of $\mathrm{PWM_{RAW}}$ and $V_{\mathrm{OUT}}/V_{\mathrm{IN}}$, respectively. Thus, F_{SW} can be modulated by adjusting D_{WIN}. The constant switching frequency control mechanism of the proposed buck converter can also be derived intuitively from Fig. 3. If D_{WIN} increases, the ripple of Δ_{FFP} is enlarged, which prolongs the HIGH and LOW pulse widths of $\mathrm{PWM_{RAW}}$ and decreases the switching frequency; vice versa when D_{WIN} decreases.

The structure of the FD is shown in Fig. 4. The detection of F_{SW} is performed by converting the period of $\mathrm{PWM_{RAW}}$



Case	F_{SW}	$FD_{OUT}[0:n]$
$CNT[0:n] < 196$	$F_{SW} > 2$ MHz	Increase
$196 < CNT[0:n] < 204$	$F_{SW} \approx 2$ MHz	Hold
$204 < CNT[0:n]$	$F_{SW} < 2$ MHz	Decrease

Fig. 4. Structure of the FD.

into digital code using an up-counter (UP-CNT). The target switching frequency is 2 MHz and the UP-CNT is clocked by $\mathrm{CLK_{EXT}}$, whose frequency is 100 MHz. In addition, four periods of $\mathrm{PWM_{RAW}}$, which correspond to the HIGH pulsewidth of S_3, are converted into digital code in order to suppress the effect of clock jitter and external supply voltage noise on the VCDLs, TAs, and PDDW by the averaging effect. After four periods of $\mathrm{PWM_{RAW}}$ are converted into CNT[0:n], it is compared with 200 ± 4 using two COMPs. Then, $\mathrm{FD_{OUT}}$ [0:n] is adjusted based on the table included in Fig. 4. After four cycles of $\mathrm{PWM_{RAW}}$ are used for frequency detection, two successive cycles are used for the operation of the COMP and up/down counter (UD-CNT). Consequently, the operating frequency of the FD is six times lower than F_{SW}. Therefore, the constant switching frequency control of the proposed structure operates sufficiently slowly in order not to affect the operation voltage regulation loop [24]. CNT[0:n] is compared with 200 ± 4, not with 200, in order to suppress the dithering in $\mathrm{FD_{OUT}}$ [0:n]. Comparing CNT[0:n] with 200 ± 4 results in the variation of F_{SW} in the range of 2 ± 0.04 MHz. However, this amount of F_{SW} variation is sufficiently small to be mitigated by the EMI design efforts [12], [22].

D. Operational Details of DCM

The operational waveform of the proposed buck converter in the DCM is shown in Fig. 5. In the DCM, the outputs of the two VCDL-HGs bypass the three TAs and two VCDL-LGs, and they are directly applied to the PDDW by setting $\mathrm{MODE_{DCM}}$ to HIGH. Therefore, the voltage-to-time conversion gain is reduced to $K_{\mathrm{VCDL-HG}}$. In addition, the size of the detection window in the DCM ($D_{\mathrm{WIN-DCM}}$) is determined by the fixed and pre-determined control code instead of $\mathrm{FD_{OUT}}$ [0:n]. Δ_{FFP} in the DCM ($\Delta_{\mathrm{FFP-DCM}}$) can be expressed as follows:

$$\Delta_{\mathrm{FFP-DCM}} = (V_{\mathrm{OUT}} - V_{\mathrm{REF}}) * K_{\mathrm{VCDL-HG}}. \tag{6}$$

Considering the operation of the PDDW in (3), the switching of $\mathrm{PWM_{RAW}}$ is determined by the ripple of V_{OUT} in the DCM. Consequently, the proposed structure operates in the pulse-frequency modulation (PFM) function during the DCM.

The operation cycle of the DCM begins when $\Delta_{\mathrm{FFP-DCM}}$ becomes less than $-D_{\mathrm{WIN-DCM}}/2$ and M_P is turned on, as shown in Fig. 5. When V_{OUT} increases sufficiently to make $\Delta_{\mathrm{FFP-DCM}}$ larger than $D_{\mathrm{WIN-DCM}}/2$, M_P is turned off and M_N is turned on to decrease i_L. When the zero current is detected by the proposed C-ICE, M_N is also turned off to prevent i_L from being negative. After M_N is turned off, M_Z is turned on to suppress the ringing in V_X and M_{DCM} is turned on to hold V_{DCM} at GND until the subsequent operation cycle starts.

The most important issue in the DCM is the detection of the zero current of i_L. In the previous buck converters [12], [26], V_X was used for zero current detection. As i_L approaches zero, V_X also approaches GND as shown in Fig. 5. The slope of V_X approaching GND is proportional to the on-resistance of M_N. Since the proposed buck converter operates in the CCM and DCM simultaneously, the on-resistance of M_N should be very small to achieve high efficiency in the CCM. As a result, the slope of V_X approaching GND is small. In addition, the variation on the inductor, which is usually from -30% to $+30\%$, can further deteriorate the slope of V_X. As a result, a high-performance ZCS is required to achieve high accuracy.

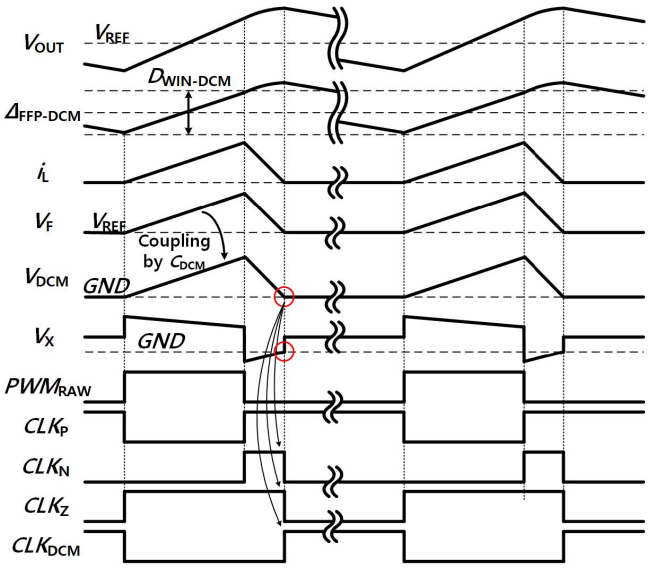


Fig. 5. Operational waveform of the proposed buck converter in the DCM.

In the proposed buck converter, the output of the C-ICE, V_{DCM}, is used for the zero current detection instead of V_X. The operation of the C-ICE in the DCM is as follows. Before the operation cycle of the DCM starts, M_{DCM} is turned on and V_{DCM} is held to GND. When the operation cycle of DCM starts and M_P is turned on, M_{DCM} is turned off and V_{DCM} becomes a floating node. Then, a change in V_F, which follows changes in i_L, is coupled to V_{DCM} through C_{DCM} as shown in Fig. 5. The coupling ratio from V_F to V_{DCM} is decided by C_{DCM}. The coupling ratio increases as C_{DCM} increase. However, large C_{DCM} reduces the amplitude of V_F and occupies large area. Thus, the size of C_{DCM} has to be decided considering the trade-off. After M_P is turned off and M_N is turned on, V_{DCM} also decreases following i_L. When i_L reaches zero, V_{DCM} also reaches GND. Therefore, by comparing V_{DCM} and GND, the zero current of i_L can be detected. When zero inductor current is detected and M_N is turned off, M_{DCM} is turned on and holds V_{DCM} to GND until the subsequent operation cycle of the DCM. The advantage of using V_{DCM} for the zero current detection is that V_{DCM} reaches GND with a steeper slope because the inductor current sensing gain of V_F is larger than that of V_X. When V_{OUT}, the on-resistance of M_N, L, R_F, C_F, and the coupling ratio between V_F to V_{DCM} is assumed as 1.8 V, 0.1 Ω, 2.2 μH, 100 kΩ, 5 pF, and 0.89, respectively, the slope of V_{DCM} approaching GND is 39 times larger than that of V_X i.e., they are 3204 and 81 mV/μs, respectively. In addition, V_F is robust to the inductance variation as described in the Section II-A, and therefore, the slope V_{DCM} is also tolerant to the inductance variation while the slope of V_X is not. Consequently, the zero current sensing accuracy and performance requirement of the ZCS can be relaxed using the proposed C-ICE. Moreover,

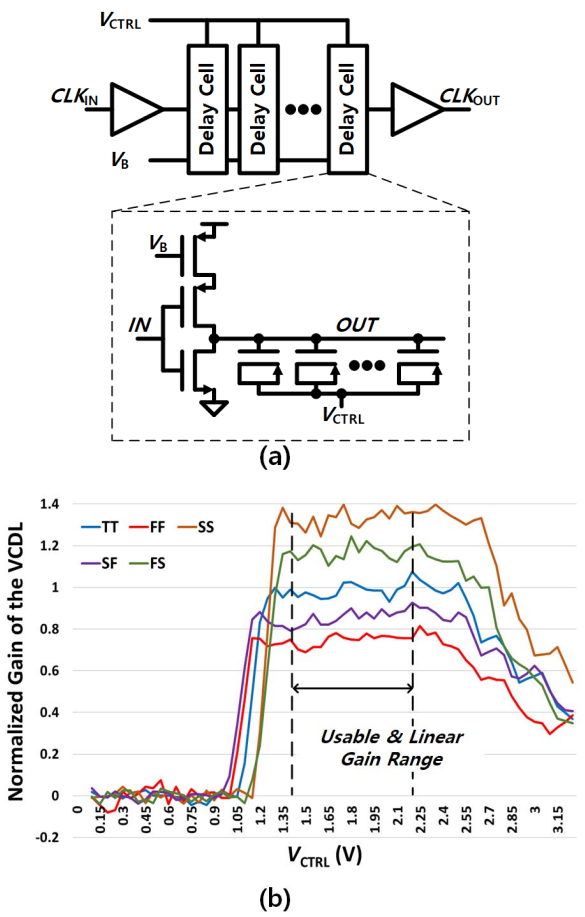


Fig. 6. (a) Structure of the VCDL. (b) Normalized voltage-to-time conversion gain of the VCDL.

V_{DCM} approaches GND from a positive voltage whereas V_X approaches GND from a negative voltage, which can affect the durability and reliability of the system.

III. Implementation Details

A. VCDL

As shown in Fig. 2, two types of VCDL are used in the proposed buck converter: VCDL-LG and VCDL-HG. The detailed structure of the VCDL is shown in Fig. 6(a). The difference between VCDL-LG and VCDL-HG is the number of delay cells used in each VCDL. VCDL-HG has a larger number of delay cells, and therefore has a larger voltage-to-delay conversion gain than VCDL-LG. Each delay cell in the proposed VCDL includes an inverter and PMOS capacitors connected in parallel at the inverter's output. The control voltage input, V_{CTRL}, changes the capacitance between V_{CTRL} and OUT and as a result, the delay of the delay cell is adjusted. The current of each delay cell is limited by the the control voltage, V_B. By limiting the current of each delay cell, large voltage-to-delay conversion gain can be achieved while consuming small power. The total power consumption of the four VCDLs is 423 μW, resulting in only 0.1% efficiency loss when V_{OUT} and i_{Load} are 1.8 V and 200 mA, respectively. Fig. 6(b) shows the normalized voltage-to-time conversion gain at five process corners. Usable and linear voltage-to-time conversion gain is obtained when V_{CTRL} ranges from 1.4 to 2.2 V because the gate capacitance increases with V_{CTRL} in this range. The output voltage range of the proposed structure is 1.5–1.8 V, and therefore, sufficient and linear gain is ensured in the operating range.

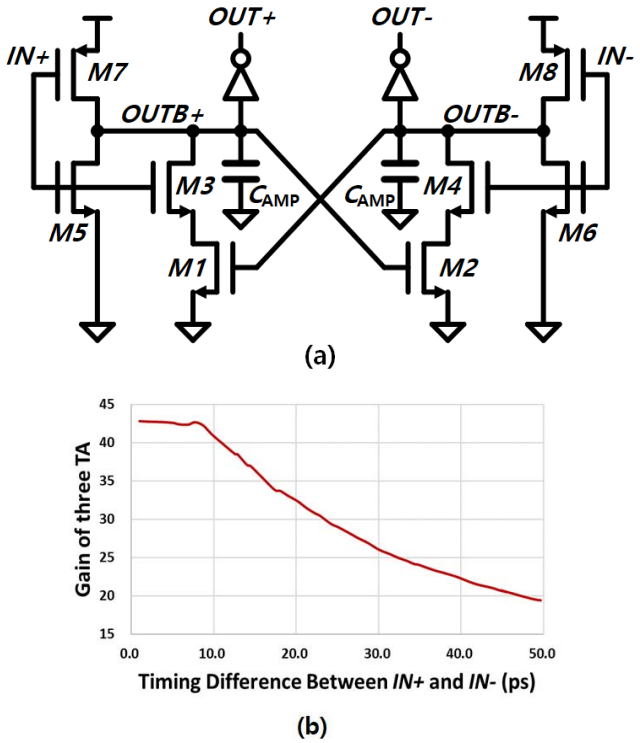


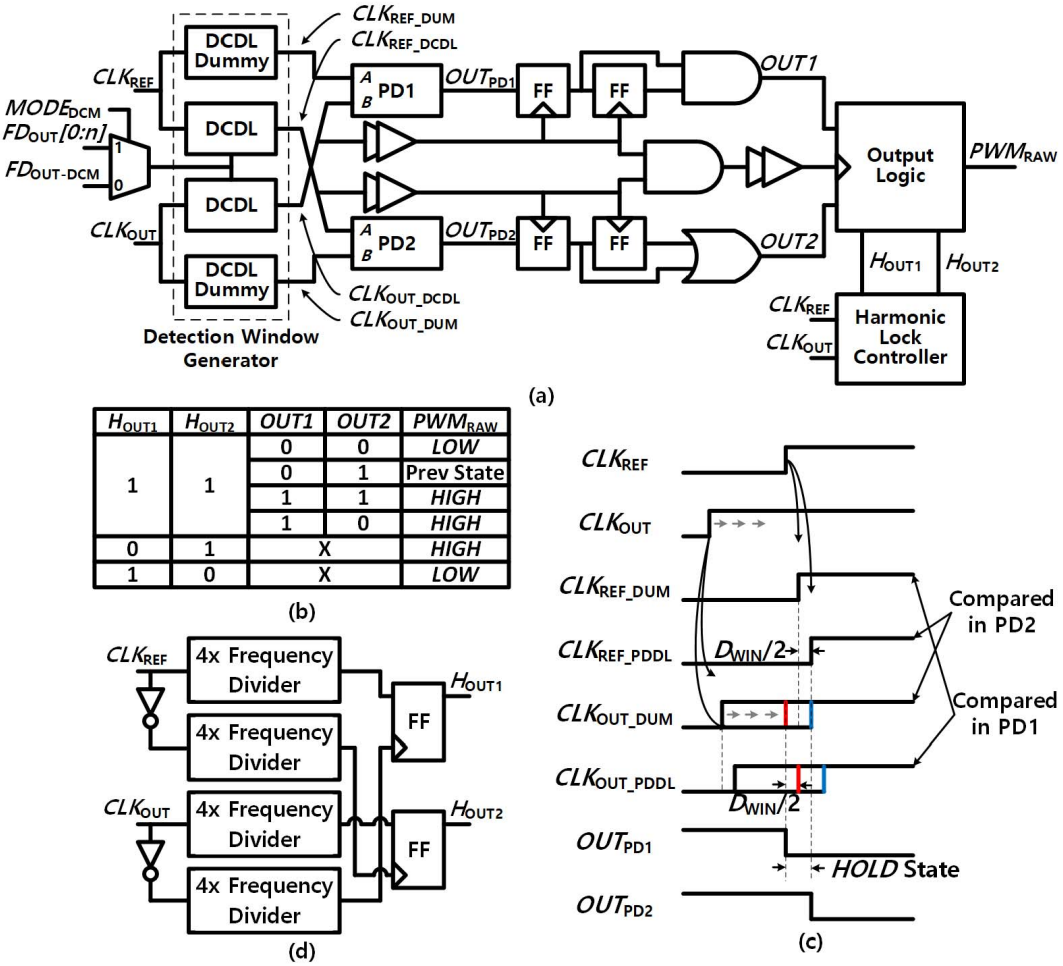
Fig. 7. (a) Structure of the TA. (b) Time amplification gain of the three successive TAs.

B. Time Amplifier (TA)

The structure of the TA in the proposed buck converter, shown in Fig. 7(a), is based on the TA in [27]. If the rising edge of IN+ arrives earlier than that of IN−, OUTB+ begins to be discharged before OUTB−. As a result, M_2 is turned off before M_1 is turned off, and hence, the discharging strengths of OUTB+ and OUTB− become different. Owing to the difference in the discharging strengths, the timing difference between IN+ and IN− is amplified to OUT+ and OUT−.

The important feature of the TA in [27] is the accurate amplification of the timing difference between the two inputs by two times. In the proposed buck converter, however, the TA is used to provide sufficient gain required in the ECP, which cannot be satisfied by only increasing the number of delay cells in the VCDL-HG. Therefore, the complex calibration circuit in [27] is removed and two capacitors C_{AMP} are added to increase the gain of the TA. The large capacitance of C_{AMP} extends the discharge time of OUTB+ or OUTB− with a slower input side. Consequently, the effect of the difference in discharging strengths is amplified and the time amplification gain increases.

The post-layout simulation result of the gain of the proposed TA according to the timing difference between IN+ and IN− is shown in Fig. 7(b). The maximum gain of 42.67, which



H_{OUT1}	H_{OUT2}	OUT1	OUT2	PWM_{RAW}
1	1	0	0	LOW
		0	1	Prev State
		1	1	HIGH
		1	0	HIGH
0	1	X		HIGH
1	0	X		LOW

Fig. 8. (a) Structure of the PDDW. (b) Lookup table of the output logic. (c) Operational waveform of the PDDW. (d) Structure of the harmonic lock controller.

corresponds to 32.6 dB, is obtained in the proposed TA. The gain of TA decreases as the timing difference between IN+ and IN− increases because the delay increase caused by the difference in discharging strengths becomes saturated [27]. However, the decrease in the gain does not cause problems because the timing difference in the two inputs to the TA, which is proportional to the difference between V_{OUT} and V_{REF}, is maintained very small.

C. PDDW

Fig. 8 shows the structure and operational details of the PDDW in Fig. 2. The two input clocks to PDDW, CLK_{REF} and CLK_{OUT}, are delayed by the DCDL and its dummy. The DCDLs are configured with a series connection of the ladder-type NAND-gate-based coarse delay line in [28] and the fine delay line used in [29]. The delay of the DCDL is controlled by FD_{OUT} [0:n] during the CCM for the constant switching frequency control and by the pre-determined control code, $FD_{OUT-DCM}$, during the DCM. The delay of the DCDL dummy is the intrinsic delay of the DCDL. The delay difference between the DCDL and its dummy generates the detection window for the PDDW. The rising edges of CLK_{REF_DUM} and CLK_{OUT_DCDL} are compared using PD1, and those of CLK_{REF_DCDL} and CLK_{OUT_DUM} are compared using PD2. PD1 and PD2 generate HIGH when the rising edge of the input B leads that of the input A. A sense-amplifier-based phase detector similar to that in [30] is used for PD1 and PD2. Then, OUT1 and OUT2 are determined by OUT_{PD1} and OUT_{PD2} of the current and previous cycles, respectively. OUT_{PD1} and OUT_{PD2} of the current and previous cycles are used to mitigate the effect of clock jitter and noises. The output logic generates PWM_{RAW} based on the lookup table in Fig. 8(b).

The detailed waveform demonstrating the generation of the detection window is shown in Fig. 8(c). When the rising edge of CLK_{OUT} leads CLK_{REF} by more than $D_{WIN}/2$, both OUT_{PD1} and OUT_{PD2} are HIGH. Then, PWM_{RAW} is set to HIGH, according to the lookup table in Fig. 8(b) and the inductor current increases. As CLK_{OUT} is delayed and leads CLK_{REF} by less than $D_{WIN}/2$, [marked with a red line in Fig. 8(c)], OUT_{PD1} becomes LOW. In this case, PWM_{RAW} holds the previous output. As CLK_{OUT} is delayed further and starts to lag CLK_{REF} by more than $D_{WIN}/2$ [marked with a blue line in Fig. 8 (c)], OUT_{PD2} also becomes LOW and PWM_{RAW} is set to LOW. Then, the inductor current starts to decrease. In this way, the rising edge of CLK_{OUT}

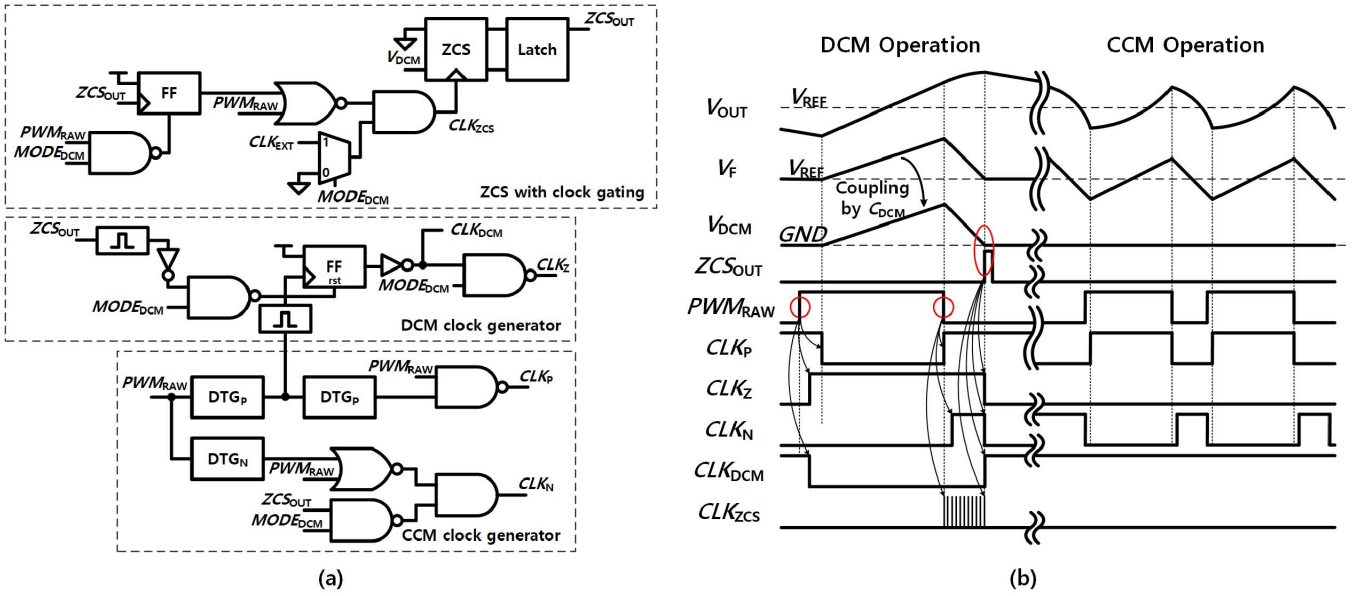


Fig. 9. (a) Structure of the clock generator with ZCS and (b) its operational waveform in the DCM and CCM.

moves back and forth around $\mathrm{CLK_{REF}}$ maintaining a delay difference less than D_{WIN}. The resolution of D_{WIN}, which is decided by the response of DCDL, can be affected by the PVT variation. The resolution of DCDL is 12.1, 8.77, and 16.2 ps at the TTTT, FFFF, and SSSS PVT corner, respectively, where capitals in each corner mean PMOS, NMOS, voltage and temperature corners, respectively. However, the frequency deviation caused by the variation on the DCDL is negligible because D_{WIN} is around few nanoseconds. The dithering of the $\mathrm{FD_{OUT}}$ [0:n] dominantly affects the switching frequency deviation as described in the Section II-C.

Fig. 8(d) shows the harmonic lock controller, shown in Fig. 8(a). The harmonic lock controller is included in the PDDW to prevent a harmonic lock, which often occurs in the design of a delay-locked loop [28]. The harmonic lock can occur when the proposed buck converter starts its operation or when the reference voltage changes. In order to prevent this issue, the harmonic lock controller in Fig. 8(d), which is composed of four 4× frequency dividers and two flip-flops, is used. H_{OUT1} and H_{OUT2} both become HIGH only when the timing difference between $\mathrm{CLK_{OUT}}$ and $\mathrm{CLK_{REF}}$ is smaller than their pulse widths. In this state, the output logic generates $\mathrm{PWM_{RAW}}$ according to OUT1 and OUT2 as shown in the lookup table in Fig. 8(b). Otherwise, when V_{OUT} is too LOW or HIGH, H_{OUT1} and H_{OUT2} force $\mathrm{PWM_{RAW}}$ as shown in Fig. 8(b). Since the 4× frequency divider is used, the proposed harmonic lock controller can prevent harmonic lock within two cycles.

D. Clock Generator With ZCS

Fig. 9 shows the structure and the operational waveform of the clock generator with ZCS in Fig. 2. In the CCM, $\mathrm{MODE_{DCM}}$ is LOW. As a result, the ZCS with clock gating and DCM clock generator are disabled for power saving by selecting GND using MUX and disabling FF, respectively.

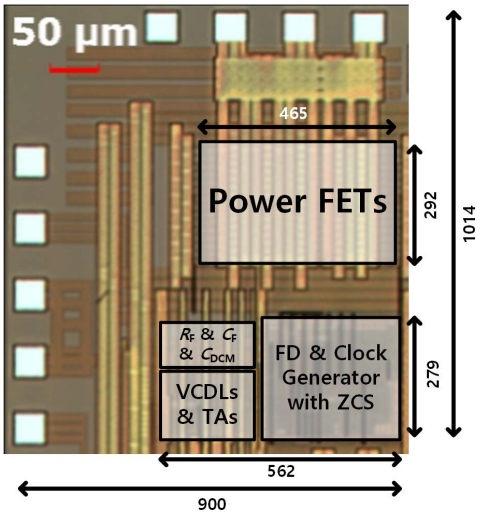


Fig. 10. Microphotograph and block placement of the proposed buck converter.

The CCM clock generator generates non-overlapping CLK_P and CLK_N from $\mathrm{PWM_{RAW}}$ using dead-time generators (DTGs) for M_P and M_N (DTG_P and DTG_N), as shown in Fig. 9(b).

The detailed operational waveform in the DCM is also shown in Fig. 9(b). In the DCM, $\mathrm{MODE_{DCM}}$ is HIGH and the ZCS with clock gating and DCM clock generator are enabled. At the rising edge of $\mathrm{PWM_{RAW}}$, $\mathrm{CLK_{DCM}}$ is set to LOW to enable the coupling operation of the proposed C-ICE. Simultaneously, CLK_Z is set to HIGH to turn off the M_Z. $\mathrm{CLK_{DCM}}$ and CLK_Z are triggered using the clock at the middle of two DTG_P in order to turn off M_{DCM} and M_Z before M_P is turned on. $\mathrm{CLK_{ZCS}}$ is gated during the high pulse of $\mathrm{PWM_{RAW}}$ to save the clocking power. After the falling edge of $\mathrm{PWM_{RAW}}$ arrives and i_L starts to decrease, $\mathrm{CLK_{ZCS}}$ is ungated by the NOR gate in the ZCS with clock gating

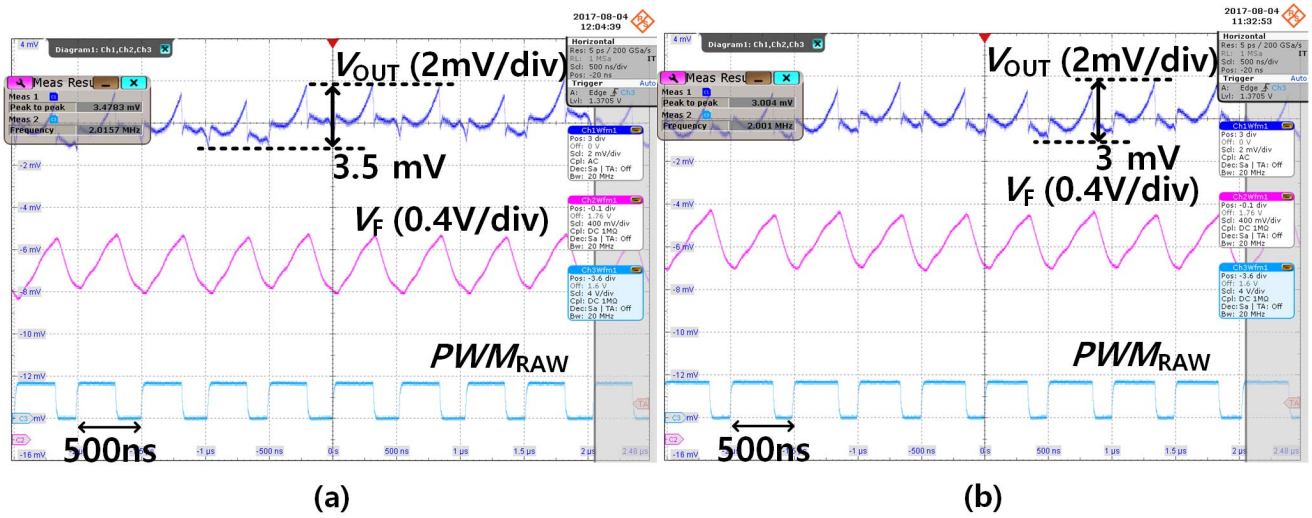


Fig. 11. Steady-state waveform in the CCM when the load current is 200 mA and V_{OUT} is (a) 1.5 and (b) 1.8 V.

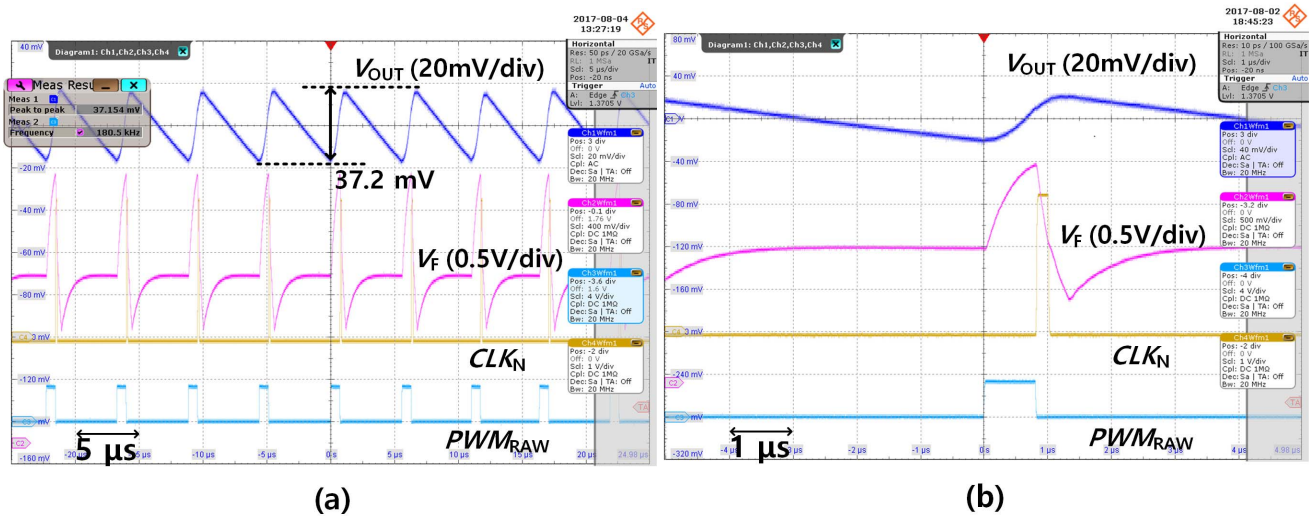


Fig. 12. (a) Steady-state waveform in the DCM when the load current is 50 mA and V_{OUT} is 1.6 V and (b) zoomed-in waveform of (a).

and is applied to ZCS. When V_{DCM} reaches GND, ZCS_{OUT} becomes HIGH and CLK_N is set to LOW to turn off M_N. Simultaneously, CLK_{ZCS} is gated again by the FF in the ZCS with clock gating for power saving until the falling edge of PWM_{RAW} arrives again in the subsequent operation cycle. In addition, CLK_Z becomes LOW to suppress the ringing and CLK_{DCM} becomes HIGH to hold V_{DCM} to GND at the rising edge of ZCS_{OUT}. In this way, CLK_{ZCS} is applied to COMP only when M_N is turned on when V_{DCM} approaches GND, leading to power saving.

IV. Experimental Results

The proposed time-domain control-based hysteretic quasi-V^2 buck converter is fabricated using the 0.35-μm CMOS technology. Fig. 10 shows the layout and detailed block placement of the proposed buck converter. R_F, C_F, and C_{DCM} of the proposed C-ICE are 100 kΩ, 5 pF, and 2.5 pF, respectively. The resultant coupling ratio from

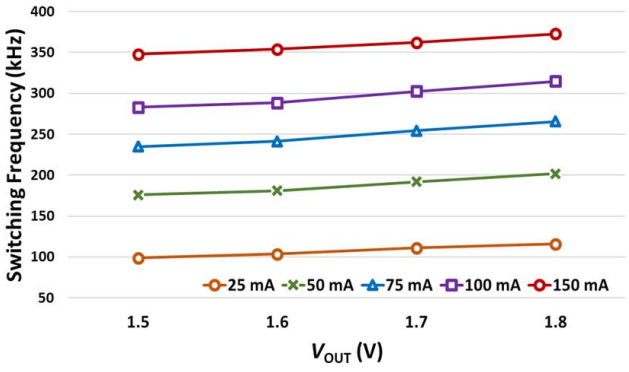


Fig. 13. Switching frequency of the proposed buck converter in the DCM under various operating conditions.

V_F to V_{DCM} with C_{DCM} of 2.5 pF is 0.89. The chip size and core area of the proposed buck converter are 0.913 and 0.293 mm^2, respectively. Owing to the proposed time-domain

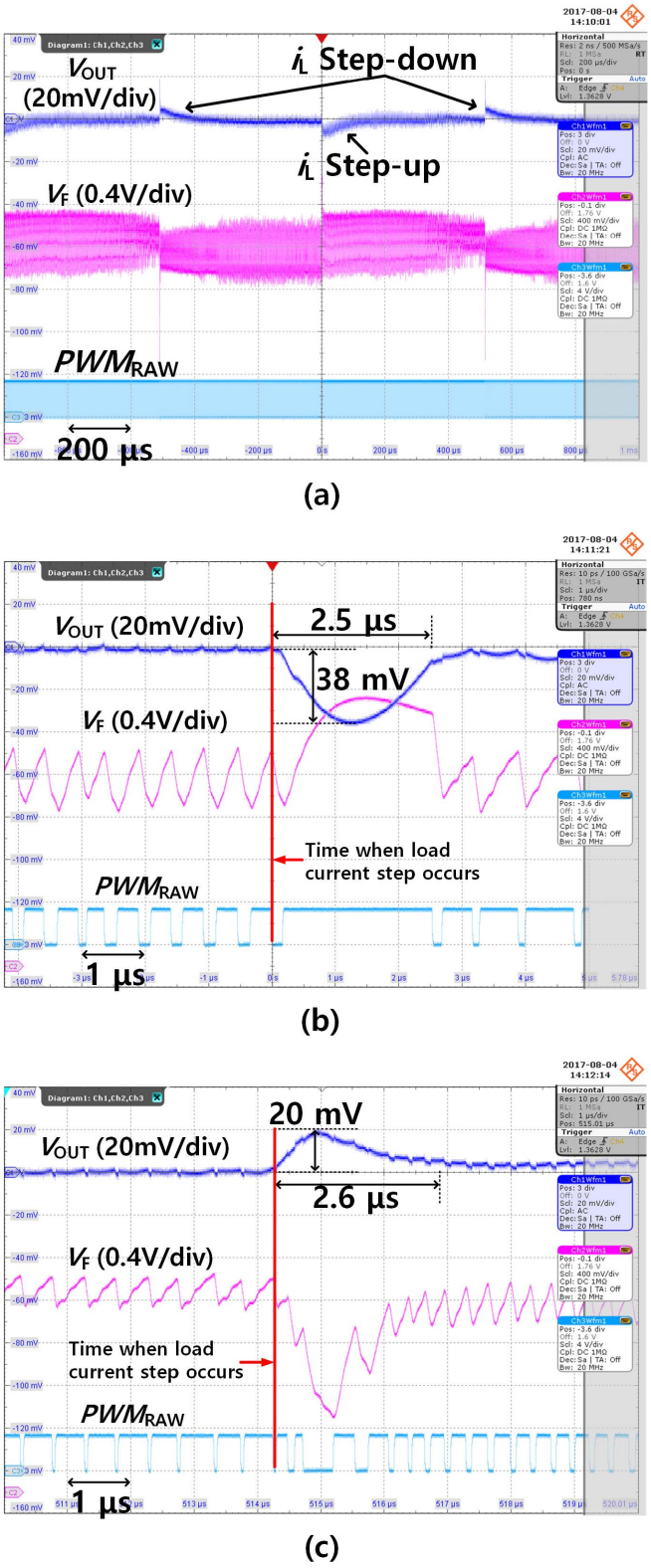


Fig. 14. Measured transient response of the proposed buck converter. (a) Waveform in large timescale. (b) When the load current steps-up. (c) When the load current steps down.

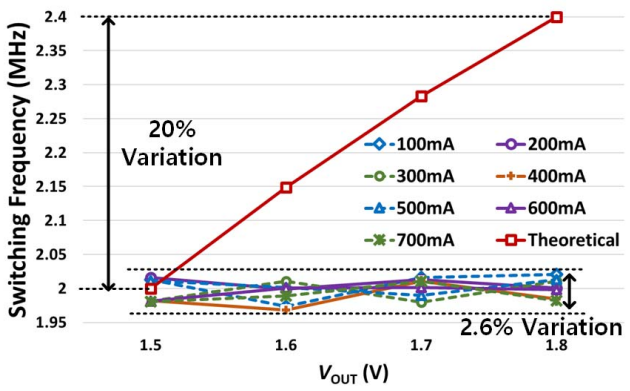


Fig. 15. Switching frequency of the proposed structure in the CCM under various operation conditions.

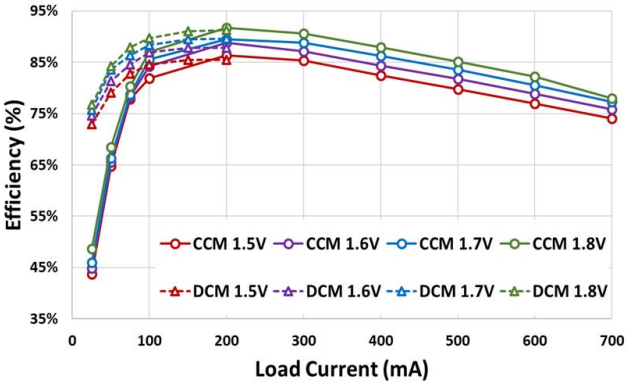


Fig. 16. Measured power efficiency of the proposed buck converter.

control, the proposed buck converter has a very compact core area.

Fig. 11 shows the steady-state waveforms of the proposed buck converter in the CCM. The output voltages in Figs. 11(a) and (b) are 1.5 and 1.8 V, respectively, and the load current is 200 mA. The ac-coupled V_{OUT} is measured in order to have a closer look of the ripple. The measured V_{OUT} ripple is less than 3.5 mV. The switching frequency is locked to 2 MHz over the entire output voltage range from 1.5 to 1.8 V.

The steady-state measurement results in the DCM when V_{OUT} and load current are 1.6 V and 50 mA, respectively, are shown in Fig. 12. As mentioned above, the proposed buck converter operates in the PFM function in the DCM mode. The measured ripple of V_{OUT} and switching frequency in this case are 37.2 mV and 180.5 kHz, respectively. Fig. 12(b) shows the zoomed-in measurement result when an operation cycle of the DCM starts. As described in Section II-D, CLK_N turns off M_N when V_F returns to its voltage level before the operation cycle starts. Fig. 13 summarizes the switching frequencies under different operating conditions.

Fig. 14 shows the measurement result of the transient response when V_{OUT} is 1.7 V and the load current steps between 170 and 680 mA. As shown in Fig. 14(a), the amplitude of V_F changes after the load current step occurs in order to fix the switching frequency at 2 MHz. The recovery time and voltage undershoot are 2.5 μs and 38 mV, respectively, when load current steps-up. The recovery time and overshoot voltage when the load current steps down are 2.6 μs and 20 mV, respectively.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

		Proposed	ISSCC 2009 [11]	TPE 2013 [12]	TCAS-I 2015 [13]	ISSCC 2015 [20]	TPE 2017 [31]
Control Scheme		Quasi–V^2 (Time Domain)	Quasi V^2	Quasi–V^2	Quasi–V^2	Quasi Current Mode	Current Mode
Technology (μm)		0.35 µm	0.35 µm	0.35 µm	0.35 µm	0.35 µm BCD	0.35 µm
Chip size including pads [mm^2]		0.913	1.8	1.9	0.884	0.929	2.242
Core Area [mm^2]		0.293	1.06*	0.74*	0.71*	0.518	0.92*
Input Voltage (V)		3.3	2.7–3.3	3.3–4.2	2.7–4.2	2.7–4.5	2.7–4.2
Output Voltage (V)		1.5–1.8	0.9–2.1	1.2	1.2	2	1.8
Inductor		2.2 µH	2.2 µH	4.7 µH	2.2 µH	4.7 µH	4.7 µH
Output Capacitor		4.7 µF	4.4 µF	8.9 µF	10 µF	10 µF	4.7 µF
Switching Frequency		2 MHz	3 MHz	750 kHz	1 MHz	1 MHz	1 MHz
Max Efficiency		92 %	93 %	86.6 %	95.65 %	95.5 %	95 %
Load Current Range (mA)		25–700	50–500	5–800	18–700	100–1000	60–600
Load Transient Response	ΔI_{LOAD} (mA)	510	300	500	300	400	400
	Settling Time I_{LOAD} Step UP/DOWN	2.5 µs /2.6 µs	2.4 µs /2.8 µs	3 µs /3.6 µs	3 µs /5 µs	4.8 µs /3 µs	2.4 µs /2.6 µs
	V_{OUT} Undershoot /Overshoot	38 mV /20 mV	38 mV /45 mV	53 mV /54 mV	48 mV /30 mV	35 mV /38 mV	88 mV /76 mV
DCM Support		O	X	O	O	X	X

* Extracted from the paper.

Fig. 15 shows the switching frequency of the proposed buck converter at various values of V_{OUT} and load current. The theoretical switching frequency without the constant frequency control is calculated from (5) assuming that D_{WIN} is constant. The measured switching frequency shows a variation between 1.968 and 2.021 MHz. The variation is caused by the finite frequency resolution of the FD and DCDL in the PDDW. However, the switching frequency variation is less than 2.6%, which can be managed through the EMI control.

The measured efficiency of the proposed buck converter is shown in Fig. 16. The peak efficiency of 92% is achieved when V_{OUT} and load current are 1.8 V and 200 mA, respectively. The efficiency below 200 mA is improved by the DCM with the PFM function. Owing to the DCM, end-to-end efficiency of more than 73% is achieved.

The performance of the proposed buck converter and the comparison with the previous structure are summarized in Table I.

V. CONCLUSION

A hysteretic quasi-V^2 buck converter with a controller realized in time-domain is presented in this paper. The proposed time-domain replaces the EA, hysteretic COMP, constant switching frequency controller, etc. in the voltage domain with simple circuits such as VCDL, TA, PDDW, and counter. Consequently, a very compact core area of 0.293 mm^2 is achieved using 0.35-μm CMOS process. The constant switching frequency control is enabled by the adjustable detection window of the PDDW. A constant switching frequency of 2 MHz with frequency variation less than 2.6% is achieved. Furthermore, the C-ICE is also proposed to improve the zero current sensing accuracy and to relax the performance requirement of the ZCS in the DCM. As a result, end-to-end power conversion efficiency of 73% is achieved in the load current range of 25–700 mA. Recovery time of 2.5 μs and undershoot of 38 mV are achieved with a load current step-up of 510 mA, and recovery time of 2.6 μs and overshoot of 20 mV are achieved with a load current step-down of 510 mA. The peak power conversion efficiency is 92%.

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