

# A 0.5-V 1.6-mW 2.4-GHz Fractional-N All-Digital PLL for Bluetooth LE With PVT-Insensitive TDC Using Switched-Capacitor Doubler in 28-nm CMOS

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**Abstract**—This paper proposes an ultra-low-voltage (ULV) fractional-N all-digital PLL (ADPLL) powered from a single 0.5-V supply. While its digitally controlled oscillator (DCO) runs directly at 0.5 V, an internal switched-capacitor dc-dc converter “doubles” the supply voltage to all the digital circuitry and particularly regulates the time-to-digital converter (TDC) supply to stabilize its resolution, thus maintaining fixed in-band phase noise (PN) across process, voltage, and temperature (PVT). The ADPLL supports a two-point modulation and forms a Bluetooth low-energy (BLE) transmitter realized in 28-nm CMOS. It maintains in-band PN of  $-106$  dBc/Hz [figure of merit (FoM) of  $-239.2$  dB] and rms jitter of  $0.86$  ps while dissipating only  $1.6$  mW at  $40$ -MHz reference. The power consumption reduces to  $0.8$  mW during the BLE transmission when the DCO switches to open loop.

**Index Terms**—All-digital PLL (ADPLL), Bluetooth low energy (BLE), digitally controlled oscillator (DCO), Internet of Things (IoT), process, voltage, and temperature (PVT) insensitive, regulator, switched-capacitor (SC) dc-dc doubler.

## I. INTRODUCTION

THE development of radios for Internet of Things (IoT) node devices has spurred research in ultra-low-power (ULP) all-digital PLLs (ADPLL) performing as local oscillators (LOs) [1]–[3]. The IoT concept entails stringent conditions on the size and weight of battery or other energy storage used to supply the IoT circuitry. In spite of the recent advancements, the IoT system lifetime is still limited by the power consumption of its radio, and in particular the LO. Energy harvesters can significantly extend the IoT lifetime up to the point of a perpetual operation, but they typically provide low voltages, often well below typical supply of CMOS circuits, i.e., within  $0.25$ – $0.8$ -V range [4]. This is likely to degrade performance of important ADPLL building blocks.

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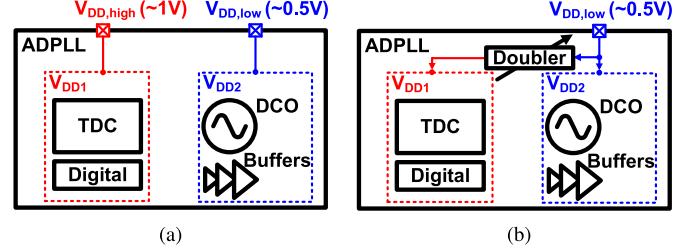


Fig. 1. Supply voltage of ADPLL (a) in prior art design (see [6]). (b) Proposed solution.

An inverter-based time-to-digital converter (TDC) is such an example. An inverter could be considered a basic time delay cell with regenerative properties, which benefits from CMOS scaling and offers the shortest controllable delay at low power consumption, but its delay (i.e. resolution of the TDC) can vary by more than  $\pm 50\%$  over process, voltage, and temperature (PVT) [5]. This unnecessarily increases the TDC size (i.e., range overhead) and power consumption, and can deteriorate in-band phase noise (PN) and spurious tones.

In [6], new system and circuit techniques were exploited to enhance efficiency of an ADPLL-based Bluetooth low-energy (BLE) transmitter. Although a digitally controlled oscillator (DCO) and an output stage of a power amplifier (PA) are designed in such a way as to operate directly at the low voltage of harvesters (i.e.,  $\sim 0.5$  V), the rest of ADPLL blocks still need  $\sim 1$  V to operate, as shown in Fig. 1(a).

Conventionally, magnetic-based dc-dc converters are used to boost an input voltage to a desired output voltage [4], [7]. However, an on-chip inductor is not yet suitable for integration due to its low quality ( $Q$ ) factor and increased losses. To overcome the efficiency issue, the inductor needs to be realized off-chip, resulting in an increase in size and cost of the system, which again may not fit in the IoT specification budget. On the other hand, the higher power density and  $Q$ -factor of an on-chip capacitor makes it a great choice for integration.

In this paper, we propose an ADPLL that is part of a BLE TX powered directly from a 0.5-V supply source. While the DCO is directly connected to 0.5 V, an internal regulated switched-capacitor (SC) dc-dc converter “doubler” boosts the low input voltage to  $\sim 1$  V internally and supplies the TDC and other digital circuitry, as shown in Fig. 1(b). The doubler is an

integral part of the TDC output normalization and uses a clock skipping technique to regulate the TDC supply in response to a background detection of its resolution, which is directly correlated with a delay/speed of digital logic. The doubler is specifically optimized for event-based loads, such as the TDC and the frequency reference (FREF)-based digital logic in the ADPLL, and uses an out-of-phase and multiphase approach, where phases generated from an internal ring oscillator (RO) are running at roughly  $\times 4$  of FREF clock rate. The proposed doubler features a low area overhead, low impact on the overall energy efficiency, and does not introduce any significant spurious tones into the system.

An architecture of the proposed ultra-low-voltage (ULV) ADPLL is described in Section II. Section III investigates the proposed PVT-insensitive TDC and the detailed background calibration. In Section IV, the design of a highly efficient SC dc-dc doubler/regulator to achieve small area and power overhead is discussed in detail. To compensate for the absence of low-dropout regulators, the clock skipping technique uses multiphase path for spurious reduction, which is then described and theoretically verified. Finally, to show the effectiveness of the proposed system, Section V discloses the experimental results.

## II. PROPOSED LOW-VOLTAGE ADPLL ARCHITECTURE WITH PVT TOLERANT TDC

To address the IoT's lofty goal of perpetual battery-less operation, several power management considerations are taken into account in the proposed ADPLL. The architecture utilizes a single 0.5-V supply for the entire design, as shown in Fig. 1(b). The supply voltage reduction results in significant power savings for the most power-hungry block, i.e., DCO [6], [8], and enables it to be supplied directly from energy harvesters. On the other hand, the TDC and all digital blocks, which consume relatively much less, are supplied from the proposed SC dc-dc converter that regulates the supply of TDC (and all other digital circuitry) to maintain the ADPLL's PN performance across voltage and temperature variations.

Fig. 2 shows a detailed block diagram of the proposed ULP/ULV ADPLL with an embedded SC doubling regulator. A  $\div 2$  divider following the DCO is used to generate four phases of a variable carrier clock, CKV[0:3], covering the Bluetooth frequency range of  $f_V = 2402\text{--}2478$  MHz. The BLE digital power amplifier (DPA) (acting here as an external  $50\text{-}\Omega$  load driver) is fed by the differential CKV[0]/CKV[2] clock signal.

The ADPLL comprises a reference phase accumulator, which receives a frequency command word (FCW), i.e., a ratio of the desired RF carrier frequency,  $f_V$ , to the reference frequency,  $f_R$ . The FCW is accumulated in each FREF cycle and generates a reference phase signal  $R_R[k]$ , which is provided to an arithmetic subtractor. All the four phases of the variable clock CKV[0:3] are routed to the phase detection circuitry that selects the phase whose rising clock edge is expected to be the closest to the rising clock edge of FREF. The prediction is done based on a fractional part of  $R_R[k]$ . The TDC quantizes a time difference between edges of the

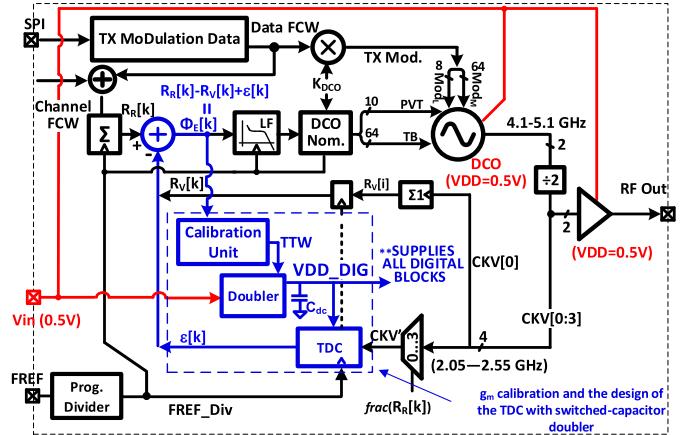


Fig. 2. Detailed block diagram of the proposed ADPLL-based BLE TX with background doubler-assisted PVT calibration for TDC resolution.

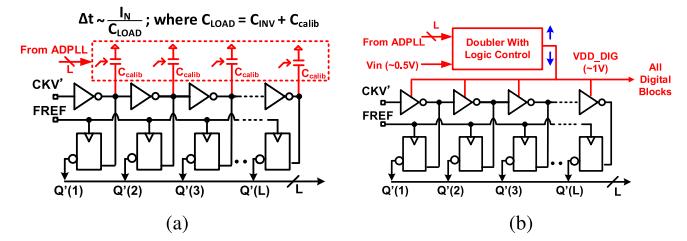


Fig. 3. Concept of TDC delay stabilization (a) through regulating capacitive load,  $C_{LOAD}$  [2]. (b) Proposed regulating doubler output,  $VDD\_DIG$ , via clock skipping, affecting charging current,  $I_N$ .

selected CKV phase (CKV') and FREF and generates a fractional error correction  $\epsilon[k]$ . On the other hand, edges of CKV[0] are counted and accumulated as  $R_V[k]$ , which is then combined with  $\epsilon[k]$  before fed to the arithmetic subtractor to generate the phase error (PHE)  $\phi_E[k]$ . After going through the type-II IIR loop filter,  $\phi_E[k]$  updates the DCO tuning word.

The TDC resolution  $\Delta t_{res}$  is kept constant across PVT via a calibration loop. This not only maintains the expected level of PN performance but it is also instrumental in keeping the TDC length as short as possible by not having, for example, to account during the design phase for the fast PVT corner. Furthermore, if  $\Delta t_{res}$  is fixed at an integer division of the CKV period  $T_R$ , then the conventional fine-resolution TDC normalizing multiplier could be greatly simplified or even entirely avoided if that division is a power-of-two integer. After the loop is settled, the calibration starts by observing  $\phi_E[k]$  and correlating it with  $R_R[k]$  to obtain a gradient  $\nabla$  for an LMS adaptation algorithm [3]. This regulates the supply of TDC to maintain its target resolution until the PHE perturbations due to the normalization error are minimized. Thus, in-band PN performance can be maintained across PVT variations. Details of the proposed calibration scheme will be discussed in Section III.

To further lower the power consumption, a dynamic programmable reference clock divider (see Fig. 2) can be engaged right after the loop is settled to scale down the ADPLL's effective reference clock rate  $f_R$  from 40 to 5 MHz or even lower, which reduces the dynamic power drain of digital logic while proportionately deteriorating the

in-band PN, as  $\mathcal{L}_{IB} \propto 1/f_R$ . In addition, once the ADPLL acquires the lock, the digital part of ADPLL can be shut down, thus ultimately improving the power efficiency [6]. The open-loop operation relies on the system tolerance to frequency drift, which must be well below the BLE limit of 400 Hz/ $\mu$ s [9].

### III. CALIBRATION FOR PVT-INSENSITIVE TIME-TO-DIGITAL CONVERTER

Traditionally, TDC gain is adjusted via a digital multiplier [5], controlled by an LMS adaptation algorithm [3]. A recent alternative is to maintain a constant TDC inverter delay with a feedback loop by digitally tuning the inverter loading capacitors [10], as shown in Fig. 3(a). However, that would require a higher driving strength of the inverter cells, and thus larger power consumption, since the inverter delay is proportional to  $C/g_m$ . Therefore, that appears less suitable for ULP applications. In [11], equidistant phases of an RO that is injection-locked to a DCO are used to quantize the DCO phase. However, a free-running frequency of RO could drift away from the locking range over temperature and cause the ADPLL to lose its lock.

To overcome the shift of delay characteristics of the TDC due to PVT, a second feedback path (Fig. 2), extending from the PHE  $\phi_E[k]$  to a calibration unit controlling the SC regulator, is proposed. After the ADPLL is locked, the calibration loop is enabled, and it keeps on working in the background to ensure a fixed  $\Delta t_{res}$  in case of temperature and voltage changes. As shown in Fig. 3(b), the PVT compensation is done by means of regulating the TDC supply voltage as an alternative to the tuning of inverter loading capacitors. The calibration mechanism strives to keep a fixed resolution independent of PVT. Each TDC tuning word (TTW) corresponds to a specific TDC resolution value and it is designed in such a way that ( $TTW_{max}/2$ ) is a function of the desired TDC resolution.

The TDC resolution  $\Delta t_{res}$  can be interpreted as the propagation delay  $t_{pd}$  of TDC inverters, which is the average delay time of a loaded inverter with high-to-low and low-to-high propagation delays ( $t_{pHL}$  and  $t_{pLH}$ , respectively) and can be stated as [12]

$$t_{pd} = \frac{t_{pHL} + t_{pLH}}{2} = \frac{1}{2} \left[ \frac{C_L \cdot V_{DD}}{K_n \cdot (V_{DD} - V_{thN})^\alpha} + \frac{C_L \cdot V_{DD}}{K_p \cdot (V_{DD} - V_{thP})^\alpha} \right] \quad (1)$$

where  $C_L$  is the inverter's load capacitance,  $V_{DD}$  is its supply voltage,  $V_{thN}$  and  $V_{thP}$  are the threshold voltages of nMOS and pMOS, respectively,  $K_n$  and  $K_p$  are the nMOS and pMOS trans-conductance, respectively, and  $\alpha < 2$  is suitable for short-channel devices [13]. Fig. 4 shows the SPICE simulated  $\Delta t_{res}$  across supply voltage. The blue line (crossed) indicates  $\Delta t_{res}$  predicted by (1). Note that as  $V_{DD}$  goes very low, the devices spend less time in saturation and (1) is no longer an accurate estimation for the inverter delay. Hence, some deviation between the simulations (dots) and equation (crossed line) at 0.7 V is observed. At a specific temperature and process (fixed  $K_{N/P}$ ,  $V_{thN/P}$ , and  $C_L$ ),  $\Delta t_{res}$  is a function of an instant supply voltage. Any tuning word greater/less than the targeted ( $TTW_{max}/2$ ) corresponds to a lower/higher  $\Delta t_{res}$  and

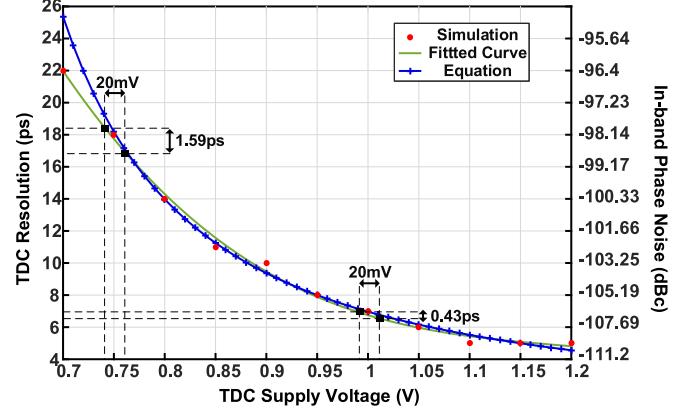


Fig. 4. SPICE simulation results of TDC resolution versus supply voltage, superimposed on model (1). Right y-axis: expected in-band PN calculated by  $\mathcal{L}_{IB} = (2\pi^2/12)(\Delta t_{res}/T_V)^2(1/f_R)$  [5], where  $T_V = 417$  ps and  $f_R = 40$  MHz.

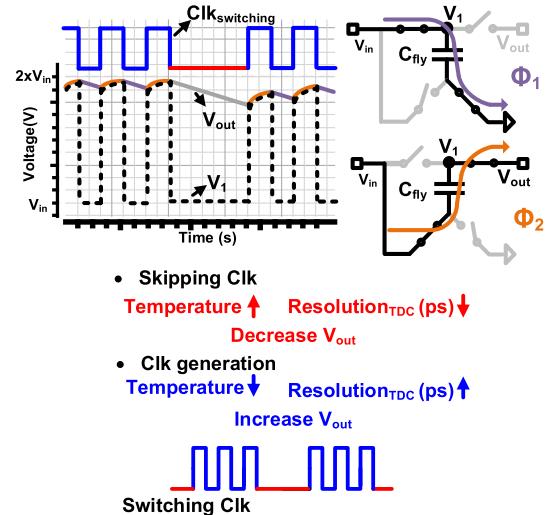


Fig. 5. Proposed principle of regulating doubler's output via clock skipping.

a higher/lower supply voltage. Therefore, in order to keep  $\Delta t_{res}$  fixed, ( $TTW_{max}/2$ ) can work as a threshold for skipping the doubler's switching clock cycles as introduced in the following.

Fig. 5 explains the principle of the proposed doubler's clock skipping. In this paper, a one-stage Dickson converter [14], [15] is realized to achieve a 1:2 step-up conversion. During  $\phi_1$ , the flying capacitor is charged by the input voltage ( $V_C = V_{in} - 0 = V_{in}$ ). At the beginning of  $\phi_2$ , the bottom plate is connected to the input and, due to the fact that charge cannot be transferred instantaneously, the top plate that is now connected to the output should become  $\times 2 V_{in}$  so that the voltage across the capacitor remains constant ( $V_C = 2 \times V_{in} - V_{in} = V_{in}$ ). As the decision is made in the calibration unit that the output voltage needs to be decreased, the doubler's clock generator is momentarily turned off and no more switching takes place in the doubler module and no charge is transferred to the output decoupling capacitor  $C_{dc}$ . The output voltage is then naturally let to slowly decrease until  $\Delta t_{res}$  reaches its target value.

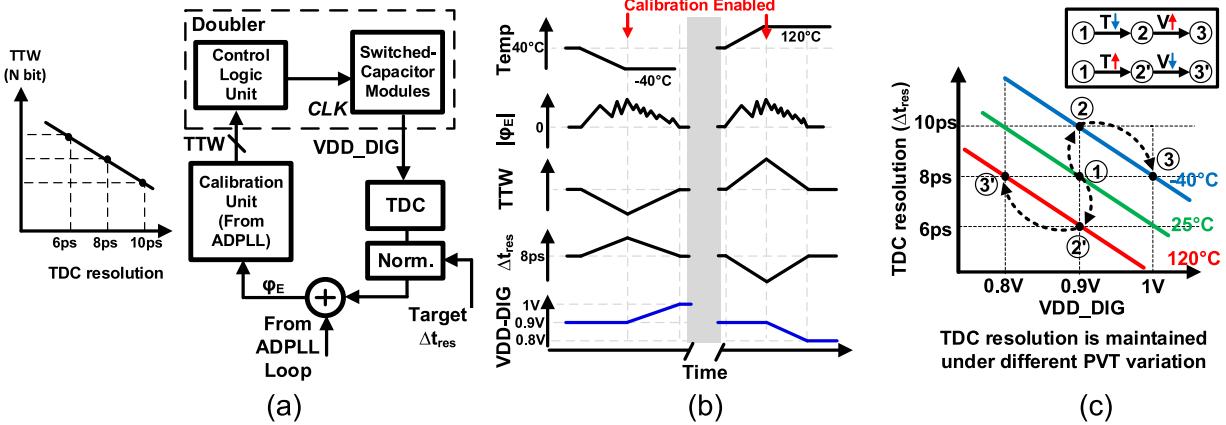


Fig. 6. Conceptual diagram of the proposed calibration for temperature variations to maintain TDC resolution. (a) Block diagram. (b) Waveforms. (c) Change in TDC resolution across voltage and temperature.

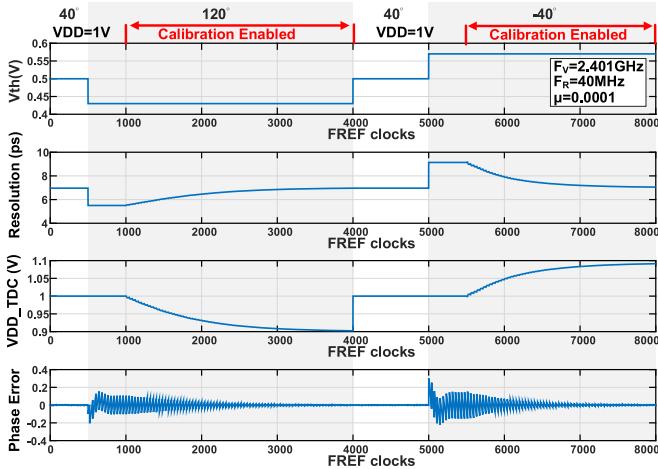


Fig. 7. Simulated results of the proposed calibration for exaggerated temperature variation and LMS bandwidth.

Fig. 6(a) presents a block diagram of the proposed calibration loop. The TDC output is normalized by the targeted resolution. If  $\Delta t_{res}$  deviates from the target, a periodical PHE perturbation is induced [16]. The PHE is then fed to the calibration unit that works based on an LMS algorithm trying to force  $\phi_E[k]$  to zero by adjusting a multi-bit digital TTW

$$\text{TTW}[k+1] = \text{TTW}[k] - \Delta \text{TTW}[k] \quad (2)$$

where  $\Delta \text{TTW}[k]$  is an adjustment code determined by  $\phi_E[k]$ .

Based on TTW, the switcher increases or decreases VDD\_DIG by skipping less or skipping more of the switcher's clock pulses. For example, if temperature decreases/increases,  $\Delta t_{res}$  increases/decreases and the calibration unit will generate a TTW lesser/greater than  $(\text{TTW}_{\max}/2)$  to tell the switcher to skip less/more cycles to increase/decrease VDD\_DIG in order to maintain  $\Delta t_{res}$  across PVT (1→2→3 and 1→2'→3' on Fig. 6).

To gain an insight into the calibration loop operation, Fig. 7 plots the simulated results for two cases of temperature at 120 °C and -40 °C. An LMS algorithm that keeps

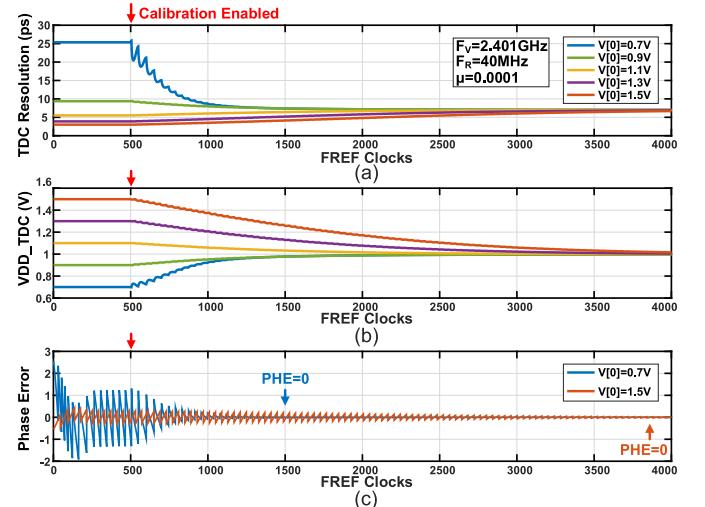


Fig. 8. Simulated results of the LMS algorithm with different starting supply voltages. (a) TDC resolution. (b) TDC supply voltage. (c) PHE.

regulating the TDC supply voltage  $V_{DD}$  until the PHE  $\phi_E$  perturbation is zero, is implemented as

$$V_{DD}[k+1] = V_{DD}[k] - \mu \cdot \phi_E[k] \cdot \frac{t_R[k] - t_V[k]}{\Delta t_{TARGET}} \quad (3)$$

where  $V_{DD}$  is the TDC supply voltage,  $\Delta t_{TARGET}$  is the target  $\Delta t_{res}$ ,  $\mu$  is a constant convergence step, and  $t_R[k]$  and  $t_V[k]$  are the reference and CKV timestamps, respectively. In each iteration, the error to the targeted resolution is observed and the supply voltage is regulated. The model uses (1) to generate  $\Delta t_{res}$  in each iteration. An increase/decrease in temperature leads to a decrease/increase in the MOS threshold voltage, which will result in the departure of  $\Delta t_{res}$  from its targeted value and the induction of PHE perturbations. In each case, the calibration is enabled after 500 FREF clock iterations to force the PHE perturbations to vanish.

To gain further insight, the simulations are then carried out with the ADPLL engaged in Fig. 8. Due to the nature of (1) and the fact that for voltages higher than 1.1 V, the change

in resolution is close to zero (see Fig. 4), it would be harder for the algorithm to converge to the target resolution. Fig. 8(c) shows the simulated result of  $\phi_E$  against that of FREF clock iteration. In the case where  $V_{DD[0]} = 0.7$  V,  $\phi_E$  converges to zero after 1500 clock cycles, while in the case where  $V_{DD[0]} = 1.5$  V, it takes more than 3500 cycles for  $\phi_E$  to reach zero.

Unlike the sudden temperature jumps in Fig. 7 simulations, the real temperature change rate in the considered applications is very low ( $<1$  °C/s). As a result, any significant PHE perturbations induced by temperature variations would occur very infrequently and so the calibration can be done without causing any disturbance to the ADPLL loop. Likewise,  $\mu$  in (3) is chosen to be very small, resulting in the calibration loop of a much narrower bandwidth than that of the ADPLL loop. This will make the ADPLL and the LMS adaptation loops nearly orthogonal to each other.

#### IV. DESIGN OF HIGH-EFFICIENCY SWITCHED-CAPACITOR DOUBLER/REGULATOR FOR EVENT-BASED LOAD

An SC dc-dc converter relies on only switches and capacitors to transfer and store energy; changing the number and arrangement of the elements results in a specific voltage conversion ratio (VCR). Although choosing a monolithic approach is attractive in many aspects, there are limitations directly related to these basic components [17].

In this design, metal–oxide–metal (MOM) capacitors are used as the flying capacitors to minimize the bottom-plate parasitic losses. MOM capacitors are built with the regular metal stack and, depending on the distance of the lowest metal layer to substrate, can achieve a relatively low substrate coupling. Compared to MOS capacitors that utilize the capacitance between the gate of a MOS transistor and its channel, MOM capacitors have a lower capacitance density, especially when only the top metal layers are used. By the choice of MOM capacitor and also the Dickson topology that has shown the best performance in terms of parasitic losses compared to other types of SC dc-dc converters [17], the parasitic losses are minimized in our design. Furthermore, due to typically low capacitance density of an integrated capacitor that results in the biggest area in the SC doubler design, the switch parasitics are far less imperative in the analysis of doubler losses.

The maximum voltage in the designed doubler does not reach above 1 V; hence, there is no need for the switches to withstand a higher than the nominal voltage rating. This makes it possible to use single thin-oxide switches. Furthermore, as the voltage increases along the doubler path and gets closer to the maximum available voltage ( $\sim 1$  V),  $V_{GS} - V_{th}$  of the switches decreases, thus making it harder to turn them on. To decrease the on-resistance of the switches without resorting to bootstrapping, an appropriate selection of nMOS and pMOS transistors can maximize  $V_{GS} - V_{th}$ .

##### A. Fundamental Analysis of Switched-Capacitor dc-dc Converters

To maintain the ULV ADPLL performance on a par with that corresponding to the optimal 1-V supply of nanoscale CMOS, the design of the SC booster should be considered

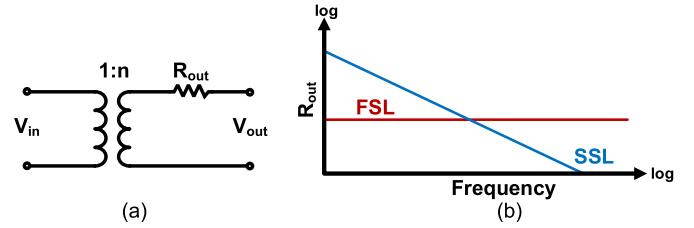


Fig. 9. (a) Idealized model of an SC converter. (b) Output impedance when  $R_{SSL} \approx R_{FSL}$ .

for optimum size of flying capacitor and power consumption overhead to achieve high efficiency.

To transfer charge between the input and output ports of the converter, capacitors must be charged and discharged, resulting in a voltage drop across the converter. This voltage drop can be represented as output impedance. An idealized model of the SC converter is shown in Fig. 9(a). This model consists of an ideal transformer with the expected “turns” ratio and the output impedance  $R_{out}$  that models the voltage drop across the output due to losses in the real converter.

To optimize the design for maximum efficiency, the output impedance  $R_{out}$  must be designed to be equal to the impedance seen at the load. There are two limits determining the output impedance: the slow-switching limit (SSL) and the fast-switching limit (FSL), which are related to the switching frequency [see Fig. 9(b)] [18].

For the SSL analysis, the finite resistance of the switches and capacitors is neglected and the output impedance is inversely proportional to the flying capacitors sizes and the switching frequency ( $R_{SSL} \propto (1/(C_{fly} \times f_{sw}))$ ). On the other hand, in the FSL analysis, the on-resistance of the switches is large enough, which prevents the capacitors from approaching equilibrium; and the impedance is characterized by constant current flows between the capacitors and is proportional to the on-resistance of the switches ( $R_{FSL} \propto R_{on}$ ). In the proposed doubler, the switches are designed to be large enough, so the output impedance is dominated by the SSL limit.

There are other losses in an SC converter, which would deteriorate the efficiency and have not been considered in the defined model. These are the switching losses that occur due to the bottom-plate parasitics of the flying capacitors, parasitic capacitance of the switches, and the dynamic losses of digital circuitry (mostly contributed by bulky buffers of the switches). Considering the rms power consumption of the TDC and ADPLL logics, the doubler is optimized for the maximum efficiency with the switching clock rate of 80 MHz and a total capacitor of 340 pF (divided between four separate modules).

##### B. Design Considerations for TDC as a Load

The timing operation of the TDC lies around the edges of FREF clock. Hence, it is reasonable to claim that a synchronous ripple on the TDC supply does not affect the TDC performance, as long as the instantaneous supply voltage is the same at all FREF clock edges. If it can be ensured that doubler’s output voltage stays the same within a margin of error at the FREF positive edge instances, the voltage droop

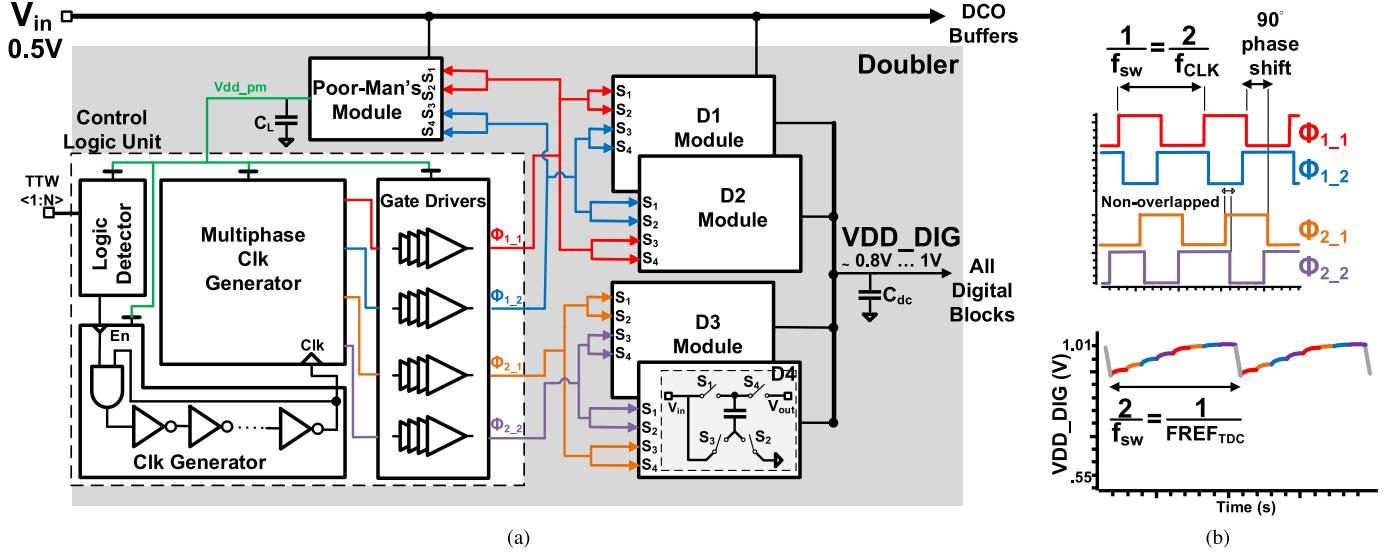


Fig. 10. (a) Detailed schematic of the proposed SC doubler. (b) Waveforms.

and overshoot in between the edges can be neglected. Even in the fractional frequency multiplication by ADPLL, the CKV phase whose rising edge is the closest to FREF rising edge is selected and fed to TDC to be propagated through the TDC's chain of inverters (see Fig. 2). In the worst case, the selected CKV edge is behind the FREF edge by  $(T_v/4) \approx 100$  ps, which is very small compared to the FREF period. The TDC supply voltage is settled to the required value well before the CKV edge arrival.

Although the average power consumption of the TDC and digital blocks is relatively low, a large amount of instantaneous current is drawn at each rising edge of FREF. This charge spike mainly sources from the output (decoupling) capacitor  $C_{dc}$  of the SC doubler and causes a voltage drop. The SC doubler compensates for this voltage drop by charging and discharging its flying capacitor, thus transferring enough charge to the output capacitor. By taking into account (1) and assuming the difference of trans-conductance and  $V_{th}$  of the nMOS and pMOS devices are negligible, the change in delay as a result of supply drop can be estimated as

$$\frac{dt_{pd}}{dV_{DD}} = \frac{-C((\alpha - 1)V_{DD} + V_{th})}{K_{N/P} \cdot (V_{DD} - V_{thN/P})^{\alpha+1}} \quad (4)$$

$$\frac{dt_{pd}}{t_{pd}} = -\frac{dV_{DD}}{V_{DD}} \frac{(\alpha - 1)V_{DD} + V_{thN/P}}{V_{DD} - V_{thN/P}}. \quad (5)$$

Equation (5) shows that by increasing the supply voltage, the change in  $\Delta t_{res}$  due to voltage variation is minimized. This agrees with the simulated results shown in Fig. 4, where a 20-mV variation at 0.75 V results in 1.59-ps variation in resolution, whereas the same amount of variation at 1 V leads to only 0.43 ps.

An SC dc-dc converter VCR is determined by its topology and the voltage conversion is performed by charging and discharging the flying capacitors in a two-phase operation scheme. If a single converter block is used, the output capacitor is charged in alternate phases. This means that there are times when the output capacitor is not being charged. To ensure the doubler output has the same voltage after a constant period

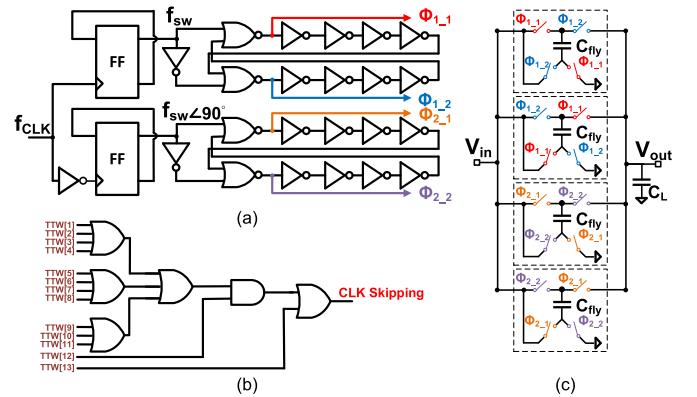


Fig. 11. Doubler circuit implementation. (a) Multiphase clock generator. (b) Logic detector. (c) Main doubler.

of time (i.e.,  $T_R = 1/f_R$ ), the same amount of charge should be transferred to its output capacitor between two consecutive FREF edges. In this paper, various modules work in an out-of-phase manner to make sure the output capacitor is charged without any interruptions.

Fig. 10 shows the detailed diagram of the SC doubler. The switching clock of  $f_{CLK}$  frequency is generated on-chip. The multiphase clock generator consists of two flip-flops and two non-overlapping clock generators. The flip-flops divide  $f_{CLK}$  by 2 and generate two new clock signals with mutual phase shift of 90° ( $\phi_1$  and  $\phi_2$ ). Based on these, the non-overlapping clock generator produces the non-overlapped and inverted clock signals. Fig. 11 shows the circuit implementation of various blocks inside the doubler.

The doubler uses the control loop to regulate the voltage supply of TDC via TTW by skipping the switching clock cycles when  $\Delta t_{res}$  is equal or better than the target, as described in Section III. The doubler consists of four main SC modules (D1–D4) that can be divided in two sets (D1/D2 and D3/D4). With a switching frequency of 80 MHz, the two sets are interleaved in order to reduce the output ripple. Furthermore, within each set, the modules work in an out-of-

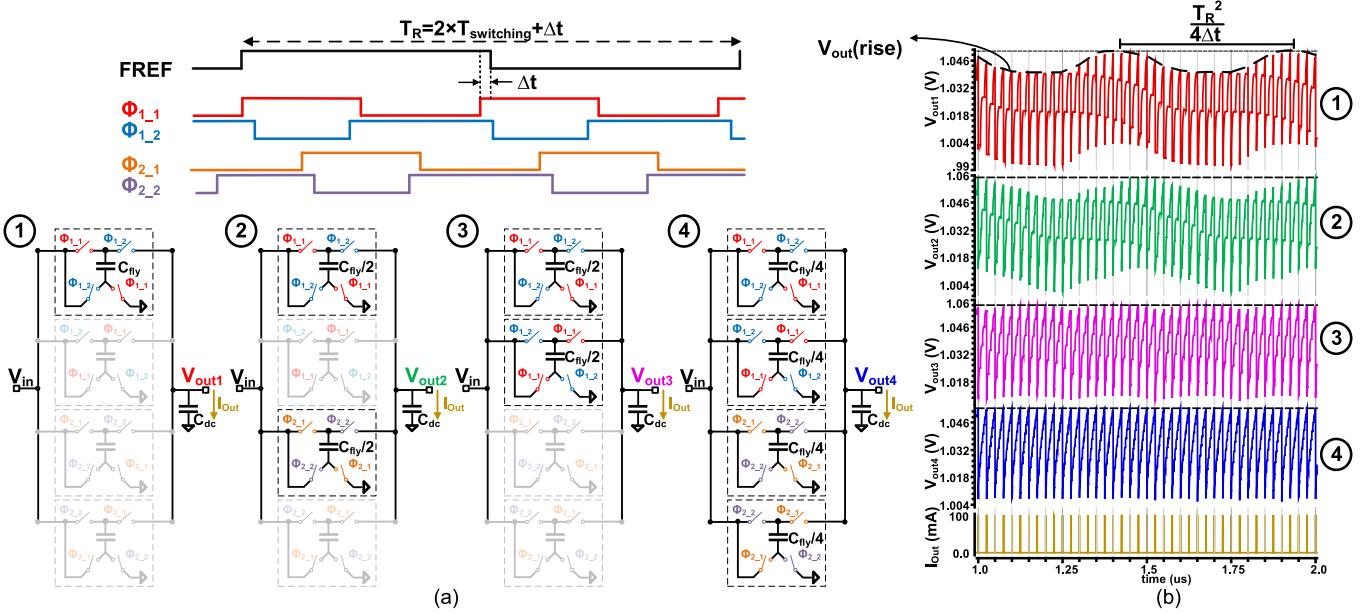


Fig. 12. Effect of out of phase and multiphase approach in load transient. (a) Different Cases. (b) Simulation result waveforms.

phase manner. In this way, the doubler transfers charge to the output capacitor without any interruptions, which guarantees the output voltage to have the same value at the positive edge of FREF in each cycle. The control logic unit of the doubler consists of a clock generator, which is enabled by a logic detector, a multiphase clock generator, which generates the four clock signals ( $\phi_{1,1}$ ,  $\phi_{1,2}$ ,  $\phi_{2,1}$ , and  $\phi_{2,2}$ ) for the SC modules and dedicated gate drivers for each clock signal. The “poor man’s” doubler is a smaller version of the main modules and is responsible for supplying the control logic unit. The proposed doubler utilizes a total of 340-pF MOM for the flying capacitor and can achieve a maximum efficiency of 85% at 1.5-mW output power.

### C. Out-of-Phase and Multiphase Approach in Load Transient

A TDC can be seen as a digital block where point of load regulation is important. It is common for digital circuits to support various different modes of operation and by switching from one mode to another; the transient load demand on the supply may change quickly. The timing operation of a TDC lies just around the edges of FREF clock. As the rising edge arrives, a large amount of current is drawn from the output capacitor  $C_{dc}$  of the doubler, which results in a voltage drop. As discussed earlier,  $\Delta t_{res}$  is vastly related to the supply voltage and so the doubler should provide the same voltage at each rising FREF edge. In other words, although the power capability of the doubler stays the same, it is obvious that its current capability needs to increase.

The SC doubler uses an internal free-running RO for its switching clock. The RO frequency would ideally be set to  $f_{CLK} = 4 \times f_R(\max)$ , where  $f_R(\max)$  of TDC is 40 MHz. The clock is then fed to the multiphase clock generator and is divided by two so that  $f_{switching} = (f_{CLK}/2) = 2 \times f_R(\max)$ . If  $f_{switching}$  is not exactly equal to  $2 \times f_R(\max)$ , then the

condition of repeatedly the same voltage at each rising edge of FREF clock cannot be generally guaranteed.

Fig. 12 investigates the use of out-of-phase and multiphase approach in an example case where  $T_R = 25$  ns and, due to PVT variations,  $T_{switching} = 12.2$  ns instead of the expected 12.5 ns. Fig. 12(a) presents four different cases where in case ①<sup>1</sup>: only one doubler module, in case ②: two modules with interleaved clock signals, in case ③: two modules in an out-of-phase approach, and finally in case ④: four modules with interleaved clock signals and in an out-of-phase approach are utilized. In all four cases, the total flying capacitor value  $C_{fly}$  remains the same. In the case where only one module is utilized, the flying capacitor is obviously  $C_{fly}$ , while in other cases, the flying capacitors are sized  $((C_{fly})/2)$  and  $((C_{fly})/4)$  for fair comparisons. Fig. 12(b) plots the simulated waveforms of the output voltage. The waveform at the bottom shows the output current drawn from  $C_{dc}$ , which illustrates the spiky nature of the TDC’s current profile. The current peaks are in response to the rising edges of FREF, where as much as 100 mA is suddenly drawn from the doubler and so a voltage drop occurs on the doubler’s output capacitor  $C_{dc}$ . The doubler must consequently increase its output voltage to exactly the same level as prior to the drop to properly handle the next rising edge.

Assuming  $T_R = 2k \times T_{switching} + \Delta t$ , where  $k$  is an integer and  $\Delta t$  presents a small time difference, the doubler’s output voltage at the rising edge of FREF clock in case ① can be approximately described as a sinusoidal function

$$V_{out(rise)} = V_{out0} + A \sin\left(2\pi \frac{4k \cdot \Delta t}{T_R^2} t\right) \quad (6)$$

<sup>1</sup>Note that the dc–dc converter is typically engineered such that the charging period is not long enough and/or  $C_{fly}$  is not large enough; otherwise the converter is overdesigned.

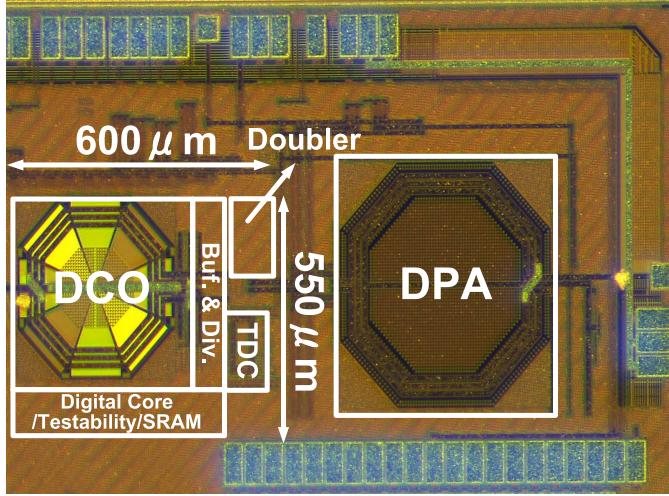


Fig. 13. Chip micrograph of the proposed ADPLL-based TX with the regulating voltage doubler.

where  $V_{\text{out}0} - A$  is the expected voltage in the ideal case  $\Delta t = 0$ , and  $V_{\text{out}0} + A$  is the amplitude of the sine wave in direct response to a charge transfer occurring during the time difference  $\Delta t > 0$ .

As presented in Fig. 12(b), in cases ① and ② where an out-of-phase approach is not applied, the output voltage cannot reach the target value unless many cycles have passed, whereas in cases ③ and ④, the output voltage gets very close to the targeted value at FREF rising edges. By choosing the configuration of case ④, the voltage variation at FREF edge would be at its smallest. Moreover, by constraining the operating frequency and the total size of flying capacitors to be constant, while acknowledging the minimal area and power overhead created by the extra switches and multi-phase clock generation circuitry compared to case ③, the charge from input to output of the doubler is transferred in smaller packages, hence, reducing the potential input current ripple.

## V. EXPERIMENTAL RESULTS

Fig. 13 shows the die micrograph of the proposed ADPLL that is fabricated in TSMC 1P9M 28-nm CMOS technology. The core area occupies  $0.33 \text{ mm}^2$  while the doubler core occupies only  $0.04 \text{ mm}^2$ .

Fig. 14 shows the measured output voltage of the SC doubler versus input voltage and across temperatures with the calibration loop engaged. As expected, the output voltage should proportionately follow the input voltage with roughly  $\times 2$  gain when the calibration is OFF. If the input voltage varies between 0.5 and 0.7 V, which may be the case for a solar cell subjected to different light intensities, the calibration loop limits the output voltage variation to less than 30 mV. Based on Fig. 4, the change in TDC resolution  $\Delta t_{\text{res}}$  for voltages higher than 1.1 V is very low. This makes it more difficult for the calibration loop to converge to the targeted resolution (also supported by Fig. 8); hence, the output voltage experiences a small rise at higher inputs. Moreover, at  $-40^\circ \text{C}$  (circular markers in Fig. 14), when the TDC requires higher

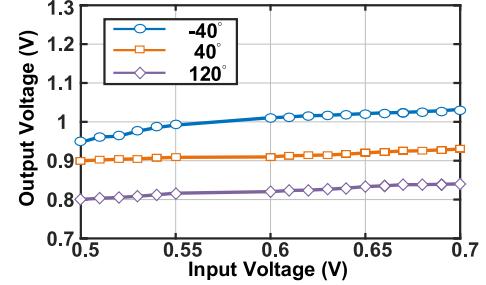


Fig. 14. Measured doubler output voltage across input voltage and temperature when the calibration is enabled.

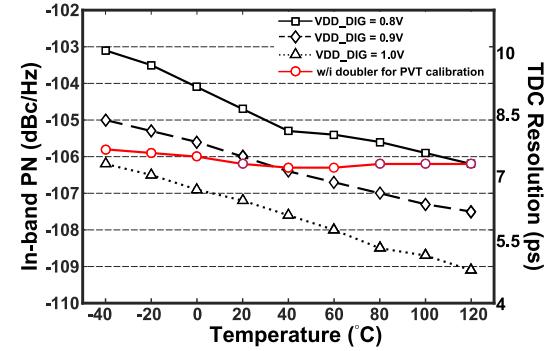


Fig. 15. Measured in-band PN/TDC resolution at 2.444 GHz at different temperatures:  $-40^\circ$  to  $120^\circ$ .

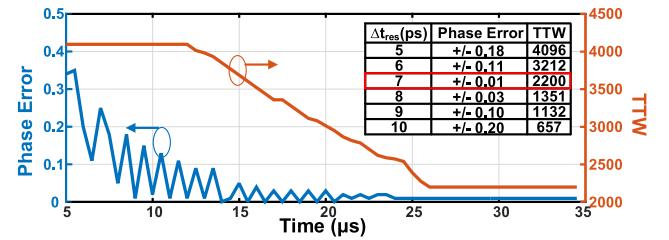


Fig. 16. Measured real-time signals during TDC calibration.

supply voltage to maintain the target resolution, the measurement shows a drop at low input voltages. This is due to the fact that an SC doubler can never exactly “double” the input voltage because of the losses. This is not an issue at  $40^\circ \text{C}$  and  $120^\circ \text{C}$  as the doubler can easily provide the required 0.9 and 0.8 V from  $V_{\text{in}} = 0.5 \text{ V}$  by skipping clock pulses.

Fig. 15 shows the measured in-band PN and  $\Delta t_{\text{res}}$  across temperature and supply voltage. As expected, when the PVT calibration is disabled, the in-band PN performance varies by 5–6 dB across temperature. On the other hand, when the PVT calibration is enabled, the PN performance maintains  $-106 \text{ dBc/Hz}$  within 0.5 dB across the  $-40^\circ \text{C}$ – $120^\circ \text{C}$  range.

Fig. 16 presents the measured real-time samples of the digital PHE and TTW during the calibration. Prior to enabling the calibration, PHE exhibits large perturbations, which then keep on reducing until TTW reaches its final value corresponding to the target  $\Delta t_{\text{res}}$ . The embedded table illustrates the measured TTW for different  $\Delta t_{\text{res}}$ .

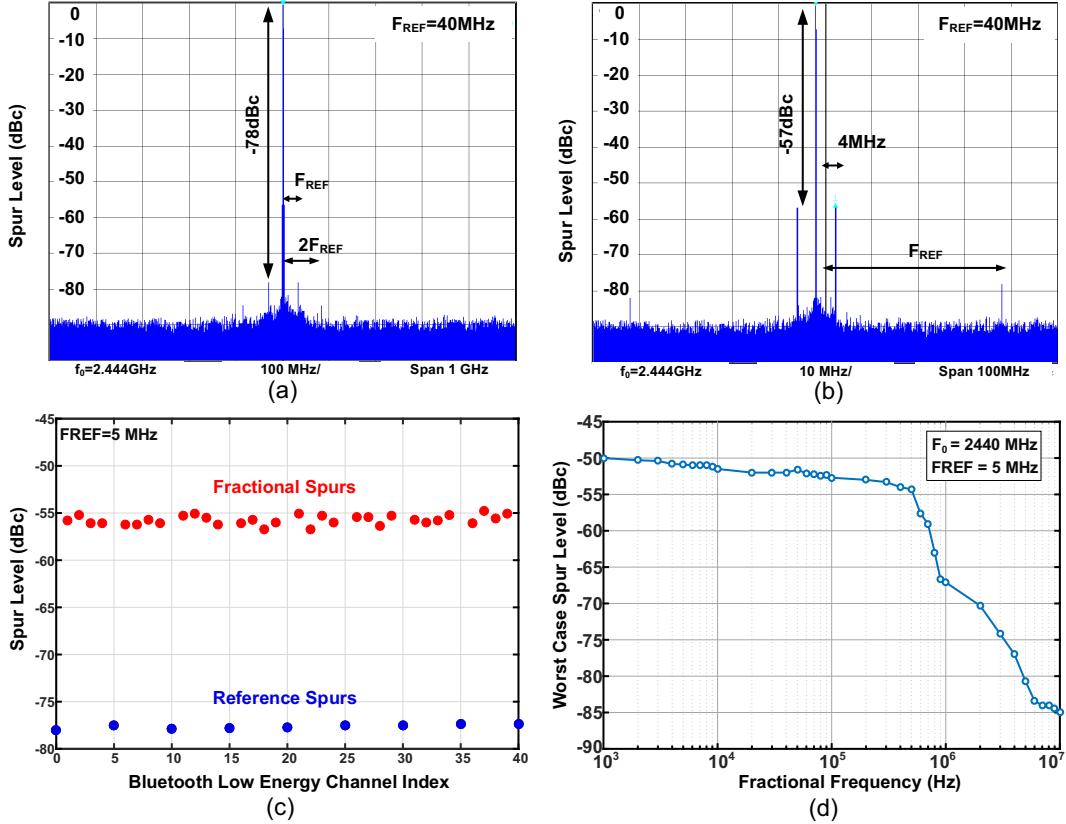


Fig. 17. Measured ADPLL spectra for (a) integer-N and (b) fractional-N channels. (c) Spurs across BLE channels. (d) Largest fractional spurs for fractional frequencies away from 2440 MHz integer-N channel ( $V_{\text{in}} = 0.5 \text{ V}$ ).

Fig. 17(a) and (b) demonstrates low levels of measured spurs while the ADPLL is supplied by the doubler ( $V_{\text{in}} = 0.5 \text{ V}$ ): reference ( $-78 \text{ dBc}$ ) and fractional ( $-57 \text{ dBc}$ ), thus verifying the robustness of the proposed supply regulation scheme. Fig. 17(c) exhibits the measured spurs across BLE channels where  $\text{FREF} = 5 \text{ MHz}$ . Fig. 17(d) exhibits the largest fractional spurs for fractional frequencies away from 2440 MHz integer-N channel.

Fig. 18 shows the measured PN at the worst case temperature condition of  $-40^\circ \text{C}$  (in light of Fig. 15) with and without regulating engagement of the SC doubler. Lower temperatures increase the TDC inverter delay, so at  $-40^\circ \text{C}$ , the in-band PN naturally degrades to  $-102.5 \text{ dBc/Hz}$ , which corresponds to an average  $\Delta t_{\text{res}}$  of  $\sim 11 \text{ ps}$  while its internal supply voltage is  $\sim 0.8 \text{ V}$ . By supplying the TDC by the SC doubler and utilizing its regulating feature, the automatic response of the calibration loop is to increase the SC doubler's voltage, thus, speeding up the TDC inverters to the desired 7 ps level, corresponding to the measured  $-106.3 \text{ dBc/Hz}$ . When used as a BLE LO at undivided 40-MHz FREF and with the calibration, the ADPLL consumes 1.6 mW with an integrated PN jitter of 0.86 ps.

Fig. 19(a) plots the measured doubler's efficiency  $\eta$  across its load power. The ADPLL's power breakdown is illustrated in Fig. 19(b) and (c) in closed-loop and open-loop [6] operations. In closed-loop operation, the power consumption of ADPLL excluding the DCO is 1 mW. This power is provided

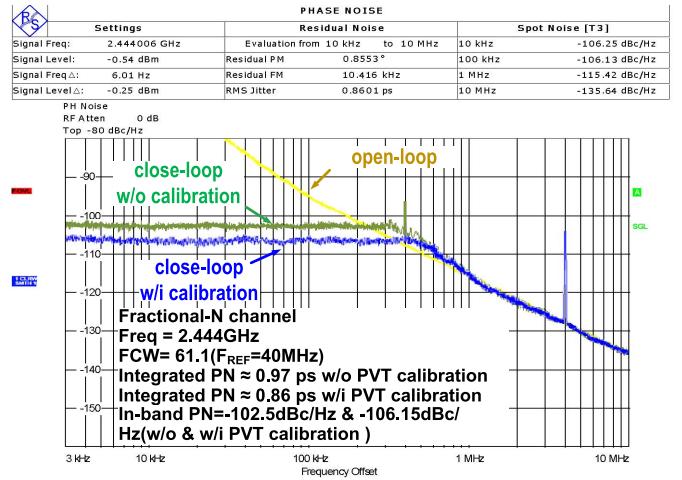


Fig. 18. Measured PN at  $-40^\circ \text{C}$  at 2.44 GHz with/without PVT calibration and at open/closed loop.

by the doubler at  $\eta = 84\%$ . Hence, the power drain by the doubler is 0.2 mW. Although only the DCO divider is powered by the doubler at open loop, the efficiency drop at lower powers results in roughly the same amount of power consumption by the doubler. The DPA is directly supplied by  $V_{\text{in}} = 0.5 \text{ V}$  and consumes 3 mW at  $P_{\text{out}} = 0 \text{ dBm}$  [6].

The proposed architecture achieves the performance that exceeds the traditional PLLs/ADPLLs powered by 0.5-V

TABLE I  
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART ADPLLS

	This work	ESSCIRC' 15 [2]	ISSCC' 14 [1]	VLSI' 14 [10]	ESSCIRC' 12 [19]	ISSCC' 18 [31]
<b>CMOS Technology</b>	28nm	28nm	40nm	28nm	32nm	65nm
<b>Supply Voltage (V)</b>	<b>0.5</b>	1.05	0.9-3.3	1.05	1.05	1
<b>Frequency Reference (MHz)</b>	40	40	32	40	40	26 w/ doubler
<b>Feature for PVT Calibration</b>	TDC+Doubler ( $g_m$ Calibration)	No	No	Yes	TDC+FLL	Gain-and-Offset
<b>Tuning Range (GHz)</b>	2.05-2.55 (22%)	2.05-2.55 (22%)	2.1-2.7 (25%)	1.5-2.1 (34%)	4.2-5 (17.4%)	2.0-2.8 (34%)
<b>in-band PN (dBc/Hz) @100kHz Offset</b>	<b>-106</b> (-40 to 120°C)	-101	-90	-108	-100	-101 ~ -108
<b>Integrated PN (ps)</b>	0.86	0.88	1.7	0.8	0.93	0.53
<b>PLL FoM* (dB)</b>	<b>-239.2<sup>†</sup></b>	-239	-236	-231	-236	-246
<b>Reference/Fractional Spurs (dBc)</b>	-78 / -57	-79 / -58	-70 / -38	-94 / N/A	N/A / -51.9	-72 / -56
<b>ADPLL Power Consumption (mW)</b>	open-loop close-loop	0.8 <sup>†</sup> 1.6 <sup>†</sup>	1.4	0.9	11	3.0
<b>Active Area (mm<sup>2</sup>)</b>	0.33	0.33	0.2	0.22	0.36	0.23

\*  $FoM = 10 \log_{10}[\sigma^2_{jitter} \cdot (P_{DC,PLL}/1\text{mW})]$  <sup>†</sup>including DC-DC converter

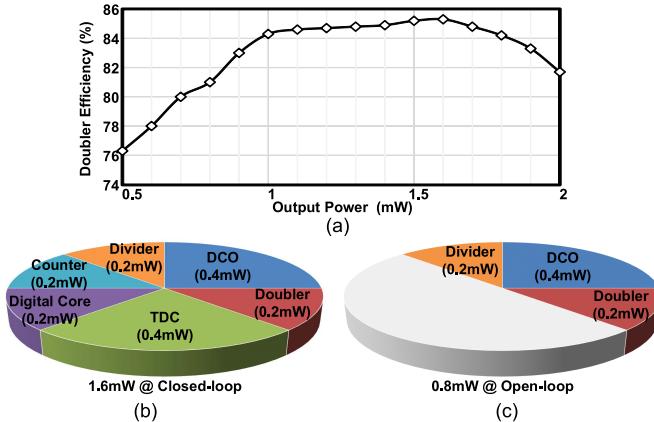


Fig. 19. (a) Measured efficiency of doubler across output power. ADPLL power breakdown at (b) closed loop and (c) open loop.

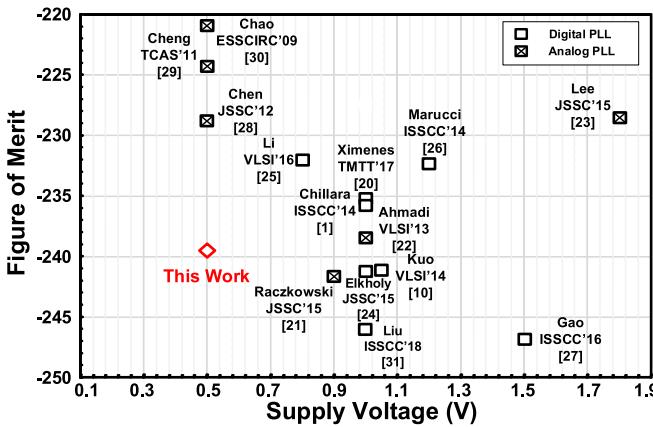


Fig. 20. Figure of merit comparison of state-of-the-art.

supply and maintains the expected performance on a par with the state-of-the-art ADPLLS operating at a  $\sim 1$ -V native voltage level of digital circuitry, including the TDC, as shown in Fig. 20. Table I summarizes the performance comparison with the state-of-the-art ADPLLS.

## VI. CONCLUSION

This paper presents a ULV BLE ADPLL for IoT applications. To meet the IoT specifications in regards to the battery size and lifetime, attempts have been made to bring down the supply voltage (as low as 0.5 V) so that the ADPLL can be directly supplied by energy harvesters. While the critical RF blocks (DCO and DPA) are directly supplied by the 0.5-V supply, an SC dc-dc doubler is utilized to boost the input voltage to  $\sim 1$  V to be used for the TDC and digital blocks. Moreover, a second feedback loop is added to the ADPLL architecture to account for PVT variations and helps to maintain a fixed TDC resolution and consequently in-band PN by regulating the TDC's supply voltage.

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