A Broadband Class-AB Power Amplifier With Instantaneous Supply-Switching Efficiency Enhancement for Cable TV Application

Jeffrey Lee, *Member, IEEE*, Ray Gomez, *Senior Member, IEEE*, and Sudhakar Pamarti, *Member, IEEE*

***Abstract*— A broadband power amplifier is presented, combining a Class-AB core with a novel supply-modulation technique, instantaneous supply switching. High-f_t NPN cascodes switch the amplifier signal current to high supply or low supply rails depending on instantaneous signal magnitude. Current-mode switching at gigahertz rates enhances efficiency for bandwidths well beyond existing envelope trackers. The 1.35-W peak power and efficiency of 13.6% at 14-dB peak-to-average-power ratio (PAPR) are observed. The combination of P_{out}, large fractional bandwidth, and high-PAPR efficiency exceeds prior art.**

***Index Terms*— BiCMOS, SiGe, broadband amplifiers, cable television (CATV), data over cable service interface specification (DOCSIS) 3.1, instantaneous supply switching (ISS), power amplifiers (PAs).**

I. Introduction

MODERN cable television (CATV) systems provide not only one-way broadcast programming, but also high-speed two-way communications between customers and the internet. Cable modems are a primary source of internet connectivity for millions of consumers worldwide, backhauling local WiFi communications for residential and business customers. Modern high-spectral-efficiency CATV systems, such as those based on the data over cable service interface specification (DOCSIS) 3.1 standard, increasingly depend on complex signal modulation, with high-order constellations (≥256-QAM), multi-carrier signaling orthogonal frequency-division multiplexing (OFDM) and multi-channel aggregation.

Fig. 1 illustrates the layout of a typical hybrid optical-fiber/coaxial cable CATV plant. Note that customer-premise cable modems and set-top boxes in a community communicate with a so-called "fiber node," via shared coaxial cable. The fiber node then communicates two-way traffic with the cable headend, similar in function to the wireline telephone central office. The bidirectional QAM signals often have a high peak-to-average-power ratio (PAPR), up to 14 dB. The DOCSIS 3.1 standard also requires high fractional bandwidth and output power. It uses frequency bands of approximately 5–200 and 50–1200 MHz for *Upstream* (customer to headend) and *Downstream* (headend to customer) signals, respectively. Typical cable modems require upstream peak output power of about 1 W. Typical fiber nodes require downstream peak power of about 10 W, and may use costly GaAs or GaN PAs [1]. CATV signals generally have higher PAPR and fractional bandwidth than WiFi protocol signals (e.g., 802.11. ac). Conventional power amplifiers (PAs) commonly have low efficiency under high-PAPR conditions, because of the high supply voltages and large bias currents necessary to avoid clipping the signal peaks. This leads to higher costs for power supplies, thermal management, and battery backup. Existing PA products for such applications may apply Class-A design [2], which achieves at best 4% average efficiency, as we will show. It is therefore desirable to extend the PA design art for high PAPR/high fractional bandwidth signals.

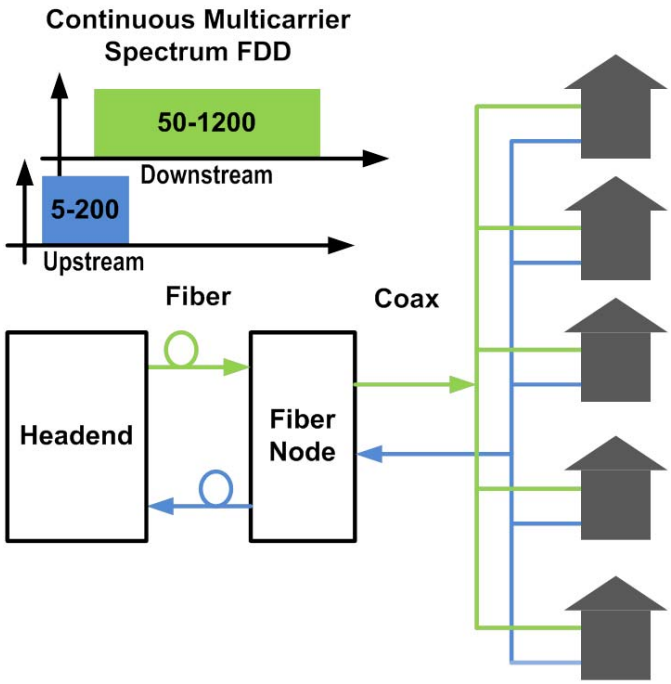

Fig. 1. CATV distribution architecture.

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J. Lee was with the Department of Electrical Engineering, University of California, Los Angeles, Los Angeles, CA 90095 USA, and also with Broadcom Ltd., Irvine, CA 92617 USA. He is now with Maxlinear Inc., Carlsbad, CA 92008 USA (e-mail: jylee0125@gmail.com).

R. Gomez was with Broadcom Ltd., Irvine, CA 92617 USA (e-mail: raygomez809@gmail.com).

S. Pamarti is with the Department of Electrical Engineering, University of California, Los Angeles, Los Angeles, CA 90095 USA (e-mail: spamarti@ucla.edu).

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Various techniques have been proposed to improve PA average efficiency. Some reduce average bias current, such as Class-AB/B/C; others reduce average supply voltage, such as supply switching (SS) (Class-G), envelope tracking (ET/Class-H), and envelope elimination and restoration (EER) [3]. There are also load modulation strategies, like Doherty [4], outphasing [5], and dynamic load modulation. Switching PAs, e.g., Class-D/E/F [6], can achieve high peak efficiency. RF PA design art using these schemes alone or in combinations achieves good efficiency for narrowband signals with high PAPR [7]–[12]. However, Class-G/ET/EER techniques are limited by supply modulator bandwidth (typically tens of megahertz) and modulator circuit power. Existing load modulation techniques and switching techniques often have limited bandwidth due to the use of tuned circuits. Existing arts lack effective techniques to enhance efficiency for broadband signals with high PAPR.

To address the challenge, we proposed a novel high-speed current-mode instantaneous SS (ISS) technique, combined with a broadband push–push Class-AB PA core in [13]. ISS here refers to supply modulation fast enough to follow not only slow envelope variations in a narrowband RF signal but also fast enough to follow the *instantaneous* amplitude of a broadband signal with spectral occupancy of many hundreds of megahertz.

In this topology, the cascode transistors necessary for high-voltage tolerance in a common-source PA are simultaneously used for SS, in response to the signal amplitude. A high-voltage supply is selected when the signal amplitude is large, and a low-voltage supply is selected when the signal amplitude is low. As is well established, the current-mode switching is naturally fast enough to make ISS possible. This technique can theoretically achieve better efficiency than envelope-based supply-modulation schemes (e.g., Class-G/ET/EER).

In this paper, Section II will describe and analyze the ISS technique. Problems that were found to arise from high-speed current-mode switching are discussed, together with the solutions that were developed and implemented. Expressions are derived for the ideal efficiency of ISS, including optimization of the supply voltages. These results are expressed in terms of the signal probability density function (PDF), so that the effectiveness of ISS versus other PA topologies can be assessed for specific applications.

Section III addresses circuit design details. The resistive shunt-feedback PA core is analyzed to derive small-signal characteristics. Auxiliary circuits, including the SS driver and output common-mode impedance control network are also described and analyzed. With this information, we examine efficiency more realistically, including the power dissipation of the auxiliary circuits and losses due to voltage and current headroom as required for adequate linearity.

Selecting 7.5/4.5 V as PA core supply rails, this 0.18-μm SiGe BiCMOS PA achieves 13.6% power-added efficiency (PAE) for a 15–215-MHz noiselike signal, with near-Gaussian PDF and 14-dB PAPR. It shows superior efficiency compared to the existing art for large fractional bandwidth, high-PAPR RF signals. Measurement results and the conclusion are presented in Sections IV and V, respectively.

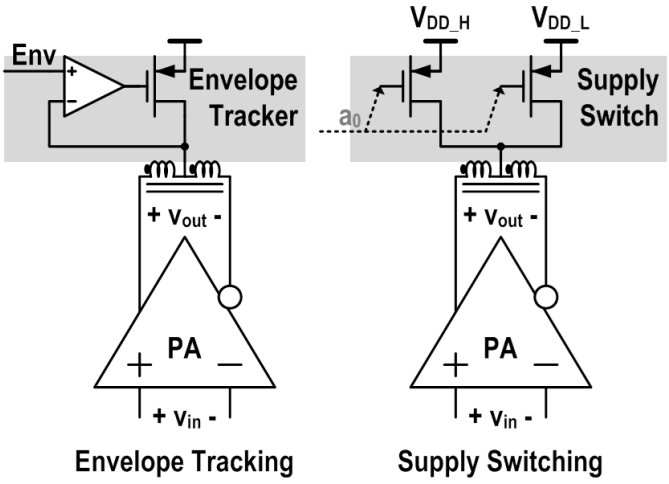

Fig. 2. Conventional supply modulation approaches.

II. Current-Mode Instantaneous Supply Switching

Supply modulation is an established category of techniques for amplifier efficiency enhancement. The PA supply is modulated dynamically in response to some signal parameter in order to save dc power. Two prior supply modulation approaches are illustrated in Fig. 2. One is ET, where the supply follows the signal envelope *continuously*; another is conventional voltage-mode SS, where the supply changes in *discrete steps* in response to the envelope. However, both approaches require high driving power for the large top-side PMOS devices. They also suffer from limited supply modulation bandwidth as mentioned earlier. ET is limited by the switch-mode power supply bandwidth [14], and voltage mode SS is limited by CV^2f losses due to rapid switching of parasitic capacitances.

The limited bandwidth of existing supply modulation techniques constrains the potential efficiency improvement. For example, it may not be possible to use the full signal envelope as input to the supply modulator. The envelope may require smoothing (low-pass filtering) of some form to match the modulator bandwidth. The modulated supply may then be forced to remain closer to its maximum value to prevent clipping after sudden jumps in the envelope. CATV signals have bandwidths on the order of 1 GHz, much greater than contemporary cellular or WAN signal formats. High-speed supply modulation is therefore essential in CATV applications, but also relevant to future wireless applications as standards incorporate higher bandwidth signals.

A. Proposed Current-Mode Supply Switching

To resolve these drive power and bandwidth issues, we propose a current-mode SS technique. In Fig. 3, the bipolar junction transistor (BJT) current-mode switch is integrated in a push–push differential PA, switching the current between V_{DD_H} and V_{DD_L}. Here, we want to highlight that the current-mode switches are also the cascode devices which serve to increase gain and protect the low-voltage NMOS input devices. Therefore, there is almost no extra cost for the

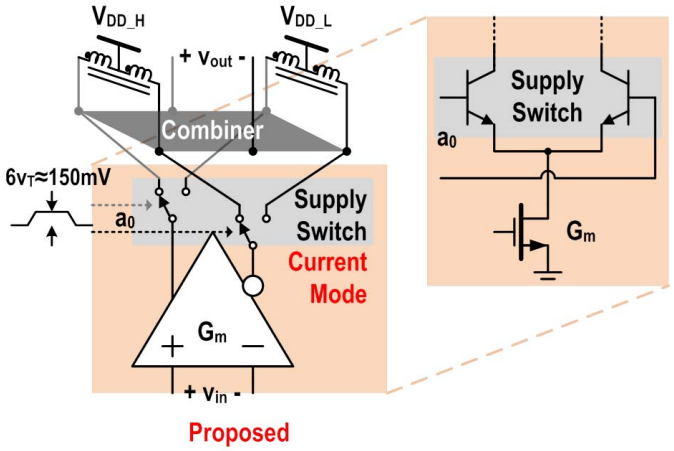

Fig. 3. Proposed BJT current-mode SS.

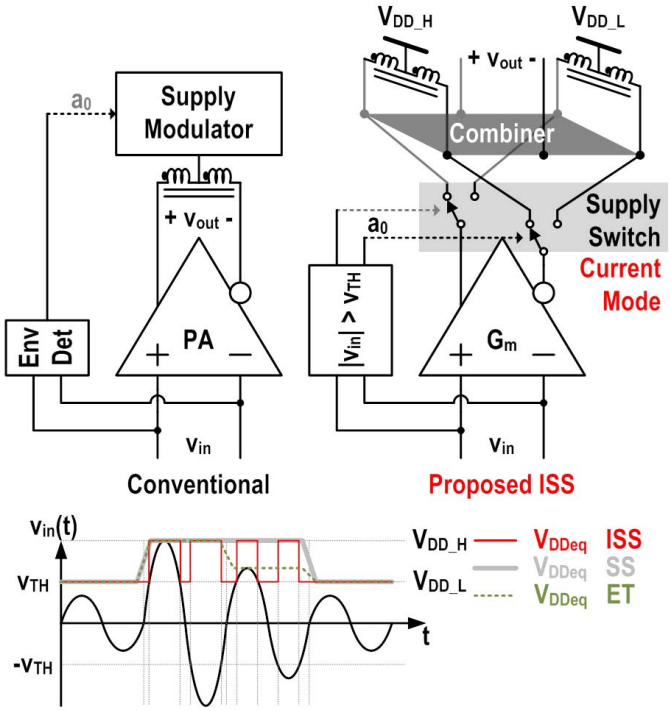

Fig. 4. Conventional supply modulator versus proposed ISS technique.

switches. Unlike existing art, where the PMOS top-side switch has to be large enough to prevent excessive voltage drop, the NPN switch here only needs to meet current density and linearity requirements, and can be much smaller with reduced parasitics. The embedded NPN also has naturally high f_t, compared to embedded or external PMOS devices, and this also contributes to reduced parasitics. Another advantage of the proposed solution is that only 6 $v_T \simeq 150$ mV is required for driving the BJT current-mode switch, which is much smaller than the typical gate drive that would be required for a top-side PMOS switch. In turn, the smaller switch size and smaller driving voltage contribute to lower drive power and better efficiency. Moreover, it is well known that very fast current-mode switching is relatively straightforward, even up to gigahertz rates. This efficient high-speed switching makes ISS possible. We can now explore the modulation bandwidth advantage of ISS in more detail.

The modulation bandwidth of ET is limited to $k_1 f_{\mathrm{SW}}$, where k_1 is the achievable ratio between the modulation bandwidth and the switch-mode converter frequency f_{SW}. This ratio k_1 is of course much less than unity. The converter frequency f_{SW} is in turn limited to $k_2 f_t$, where $k_2 \ll 1$ allows enough time constants of the switch driver circuit for full switching. Combining these, we get $\mathrm{BW_{ET}} \leq k_1 k_2 f_{t,\mathrm{PMOS}}$ (assuming a discrete PMOS switch is used for ET). Estimating $k_1 = k_2 = 0.1$, we get a bandwidth limit of ET equal to 0.01 times the f_t of the discrete off-chip PMOS device, perhaps on the order of tens or hundreds of megahertz.

There are several time constants to consider in our proposed ISS scheme. Complete switching will require on the order of 10 time constants. One time constant is due to the transit time of the NPNs as the cascodes switch between rails. Given that the NPN f_t is 28 GHz, this is not a significant limitation. Another time constant is the product of the switch-drive circuit output resistance and the base capacitance of the NPNs. This is mitigated by sizing the driver appropriately. A third time constant is approximately determined by the product of $1/g_{m,\mathrm{NPN}}$ and $C_{\mu,\mathrm{NPN}}$. This time constant corresponds to the time needed for current through the collector-base capacitance to become negligible. It is even shorter than $1/f_{t,\mathrm{NPN}}$. Therefore, the bandwidth of our proposed scheme is limited by the SS driver in Fig. 11, which is an inverter-chain-based driver. Its toggle rate is limited to about 1/(8 fan-out-4 inverter delays) [20], which is about 2 GHz in 0.18-μm CMOS. This matches our simulation and measurement results. Testing of our PA was carried out with a 1-GHz switching rate, since this was adequate to achieve optimum PAE.

B. Instantaneous Supply Switching

Once again, ISS means that the PA selects its supply depending on the signal's instantaneous magnitude, rather than its envelope. If the magnitude of the signal is greater than the threshold V_{TH}, $V_{\mathrm{DD\_}H}$ is selected; otherwise, $V_{\mathrm{DD\_}L}$ is selected. The architecture and operating principle of ISS are shown in Fig. 4. Here we use a sinusoidal signal with peak amplitude greater than V_{TH} and three envelope steps for illustration. When the envelope is smaller than the V_{TH}, $V_{\mathrm{DD\_}L}$ is always selected.When the envelope is greater than V_{TH}, there are some moments that the magnitude is larger than V_{TH} and some moments when it is smaller than V_{TH}. A major difference in the proposed ISS technique versus existing art is that at these moments, the supply is switched to $V_{\mathrm{DD\_}L}$ to save dc power. In this way, we can overcome the efficiency limitations of classic linear PAs. For example, an ideal Class-A PA has an efficiency upper bound of 50% for sinusoids. If ISS is applied to a Class-A PA, we can achieve greater than 50% efficiency for sinusoids, ideally up to 60%. In other words, ISS can achieve better efficiency than SS and ET even for *constant-envelope signals*. Note that current-mode SS can also be applied to high-speed ET if this is desired. Furthermore, more than two supply levels can be used, for further

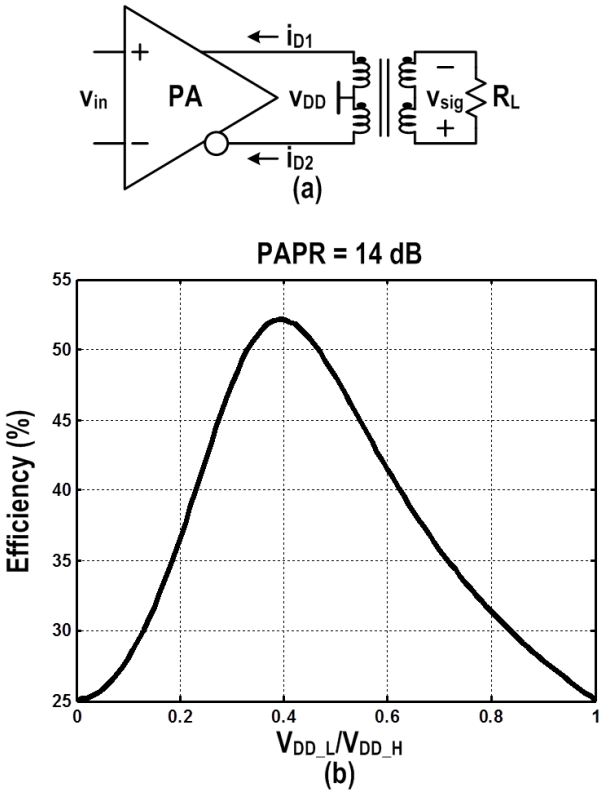

Fig. 5. (a) Differential push–push PA. (b) Achievable efficiency with target signal and Class-B with ISS.

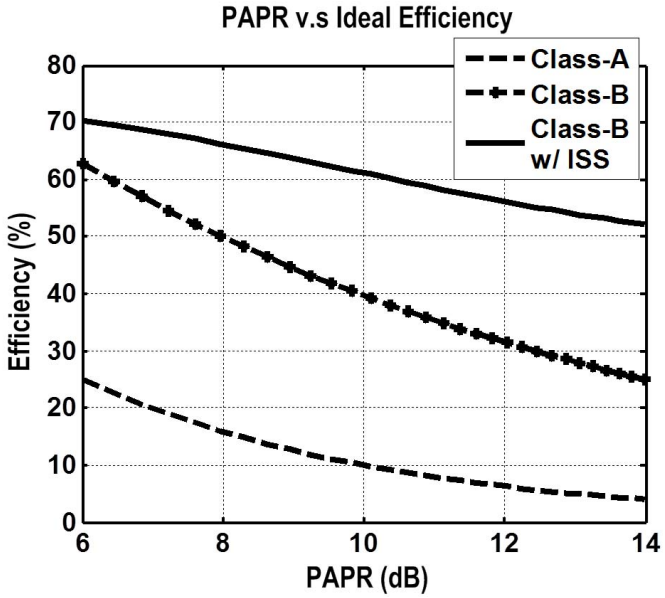

Fig. 6. Ideal efficiency with 14-dB PAPR Gaussian-distributed signal.

efficiency improvement. A disadvantage of additional supply levels (besides complexity) is the extra parasitic capacitance that will be seen at the output nodes due to NPN collector-base and collector-substrate capacitance.

We now analyze ideal efficiency for the target DOCSIS 3.1 CATV signals, assuming zero excess voltage and current headroom and an infinite SS rate. We compare the ideal efficiency between Class-A, Class-B, and Class-B with proposed ISS by considering the differential push–push PA topology in Fig. 5(a). DOCSIS 3.1 uses OFDM multi-carrier QAM signals. Multicarrier signals such as these tend to have near-Gaussian voltage probability density functions, due to the central limit theorem. True Gaussian signals have infinite PAPR, with very infrequent large peaks. OFDM signals will have some naturally bounded PAPR, depending on the details of the signal format. For practical purposes, the peak voltage (v_{peak}) here is clipped to five standard deviations ($\sigma = v_{\text{rms}}$), which leads to 14-dB PAPR. Here PAPR is defined as $(v_{\text{peak}}/v_{\text{rms}})^2$ instead of $(v_{\text{peak}}/v_{\text{rms}})^2/2$. The latter definition is used in some RF literature, and is the ratio of the average power of a full-amplitude sinusoid to the average power of the actual signal. Clipping to five standard deviations does not significantly degrade the performance of DOCSIS 3.1 systems.

In the Class-A case, V_{DD} must be greater than $v_{\text{peak}}/2$ and i_{bias} must be greater than $2\ v_{\text{peak}}/R_L$, therefore the minimum dc power (P_{dc}) to avoid clipping is v_{peak}^2/R_L. The average output power (P_{out}) is v_{rms}^2/R_L. Hence we have average power efficiency (η) of $v_{\text{rms}}^2/v_{\text{peak}}^2 = 1/\text{PAPR}$. For our target signal (PAPR = 14 dB or a linear power ratio of 25:1), Class-A can ideally achieve 1/25 = 4% efficiency. Linear power ratio is $10^{(\text{PAPR}/10)}$; in other words PAPR expressed in linear instead of dB units. It is equal to the square of the voltage ratio.

In the Class-B case, the V_{DD} limit is same as for Class-A. The current follows the signal: $i_{\text{bias}} = 2|v_{\text{sig}}|/R_L$. The minimum average P_{dc} is therefore

$$P_{\text{dc}} = V_{\text{DD}} \int_{-v_{\text{peak}}}^{v_{\text{peak}}} i_{\text{bias}} f(v_{\text{sig}}) dv_{\text{sig}} = \sqrt{\frac{2}{\pi}} v_{\text{peak}} \frac{v_{\text{rms}}}{R_L} \qquad (1)$$

where $f(v_{\text{sig}})$ is the PDF of the Gaussian-distributed output voltage signal. We get $\eta = \sqrt{\pi/(2 \cdot \text{PAPR})}$. For our target signals, Class-B can achieve 25% theoretical efficiency.

In our proposed operating mode, Class-B with ISS, i_{bias} is same as for Class-B. $V_{\text{DD\_}H}$ must be greater than $v_{\text{peak}}/2$. The supply-rail transitions occur when $V_{\text{out}} = 2V_{\text{DD\_}L}$. The minimum average P_{dc} is then

$$P_{\text{DC}} = \int_0^{2V_{\text{DD\_}L}} 2V_{\text{DD\_}L} i_{\text{bias}} f(v_{\text{sig}}) dv_{\text{sig}} + \int_{2V_{\text{DD\_}L}}^{v_{\text{peak}}} 2V_{\text{DD\_}H} i_{\text{bias}} f(v_{\text{sig}}) dv_{\text{sig}}. \qquad (2)$$

Ideal efficiency versus $V_{\text{DD\_}L}$ is shown in Fig. 5(b). For our target signal, Class-B with ISS can achieve 52% efficiency when the optimum value of $V_{\text{DD\_}L}$ is chosen. This is much better than conventional Class-A and Class-B efficiency under such high-PAPR conditions. Fig. 5 shows that $V_{\text{DD\_}L}$ cannot be too low, otherwise the supply would barely switch. It also cannot be too high; otherwise no power would be saved. Fig. 6 shows PAPR versus achievable efficiency for a Gaussian-distributed signal. Our proposed ISS technique is strongly advantageous relative to Class-A and Class-B for high-PAPR signals.

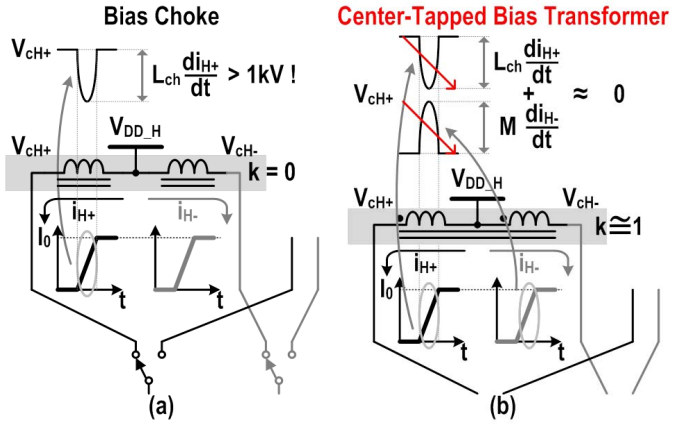

Fig. 7. (a) Magnetic flux change and voltage jumps with RF choke bias. (b) Reduction using center-tapped bias transformer.

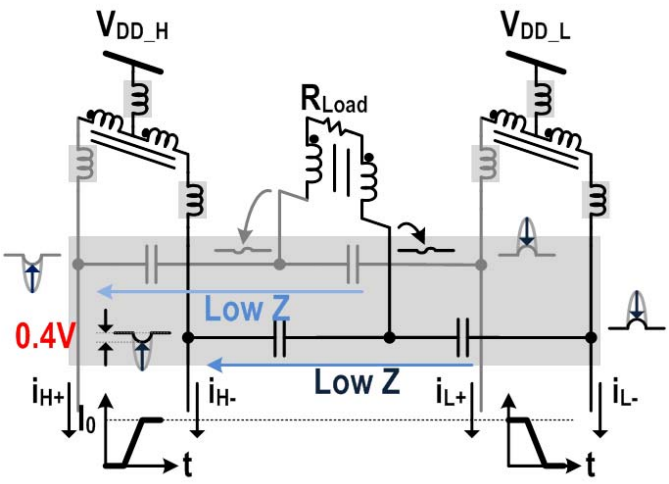

Fig. 8. Residual magnetic flux change and voltage jumps due to parasitic inductance and reduction with the proposed capacitive coupling combiner.

C. Potential Issues and Solutions

One major potential issue for current-mode ISS is the magnetic flux change in the bias chokes while rail switching. As shown in Fig. 7(a), if the PA is biased with conventional RF chokes and the current is switched from one rail to another, the NPN collectors see very large voltage jumps due to Ldi/dt. For example, in a typical broadband PA design using bias chokes with value of 3 μH, with current switching threshold 100 mA and transition time 250 ps, the flux change would theoretically cause a voltage jump greater than 1 kV, which is of course not practical.

This issue is resolved first by using a center-tapped bias transformer instead of individual chokes. As the current switches from one rail to the other, the sum of the currents in transformer windings remains constant. Because the transformer windings are coupled with $k = 1$ (ideally), there is no net flux change, and therefore no voltage jump during a rail transition. The center-tapped transformer is needed anyway to reject Class-AB common-mode current changes, so it does not impose an additional cost. Fig. 7(b) illustrates how this works. When the current is switching from V_{DD_L} to V_{DD_H}, the V_{ch+} node has a flux change and voltage jump due to the left inductor, which is same as the jump that occurs using an RF choke. Because of the mutual coupling, there is another flux change with the same amplitude but with opposite direction. These two flux changes cancel each other out. Note that in CATV applications, a ferrite-core transformer is required due to the low-frequency cutoff (5 MHz); but in wireless applications, an on-chip transformer could be used. Another way to understand this is that the center-tapped transformer has high differential-mode impedance from self-inductance (L_{ch}) plus mutual inductance (M), but low common-mode impedance from L_{ch} minus M. The SS operates on the common mode, and the low impedance of the transformer fixes the flux change issue.

In practice, the bias transformer has parasitic leakage-inductance due to its package leads and also due to printed circuit board (PCB) traces, IC traces, bond wires, etc.; the equivalent model is shown in Fig. 8. The parasitic leakage inductance was modeled as 2 nH in series with each transformer lead, including the center tap. The residual voltage jump due to flux changes in the leakage inductances is now 2.4 V. This is much better than before, but still unacceptably large. Such jumps would encroach on the device headroom significantly, affecting efficiency and linearity.

To resolve the residual flux change issue, we proposed the *capacitive coupling combiner*, as shown in Fig. 8. The combiner is composed of two large equal-size capacitors between V_{DD_H} and V_{DD_L} branches. The large capacitors maintain low impedance over the full frequency range. Note that the voltage jumps due to flux changes across the capacitors are equal and opposite. The low-impedance capacitive path between the two rails allows these jumps to offset each other. The voltage jumps due to flux changes in the parastic inductances are reduced from 2.4 to 0.4 V at the NPN collectors. Since the collector jumps are equal and opposite, the jump at the midpoint of the split and at the load is less than 10 μV in simulations.

The capacitive combiner is implemented with both internal and external capacitors. The internal capacitors (∼30 pF) take care of the high-frequency switching transients without suffering from extra package and PCB trace equivalent series inductance. External capacitors (∼1 nF) on the PCB are necessary for the low-frequency limit of CATV upstream signals (5 MHz); internal capacitors of this magnitude would have excessive ground parasitics. The extra combiner pins are shared with the center-tapped bias transformers and common-mode chokes to the IC.

III. Circuit Implementation

To demonstrate ISS for CATV applications, this PA was designed and fabricated in the TowerJazz 0.18-μm SiGe QF process. This process features high-breakdown-voltage BJT transistors and standard 0.18-μm CMOS devices. The complete PA architecture is shown in Fig. 9.

We use pseudo-differential common-source NMOS transistors biased in Class-AB as the input stage, cascoded with BJT NPN transistors as the proposed current-mode supply switches. The push–push differential architecture doubles the

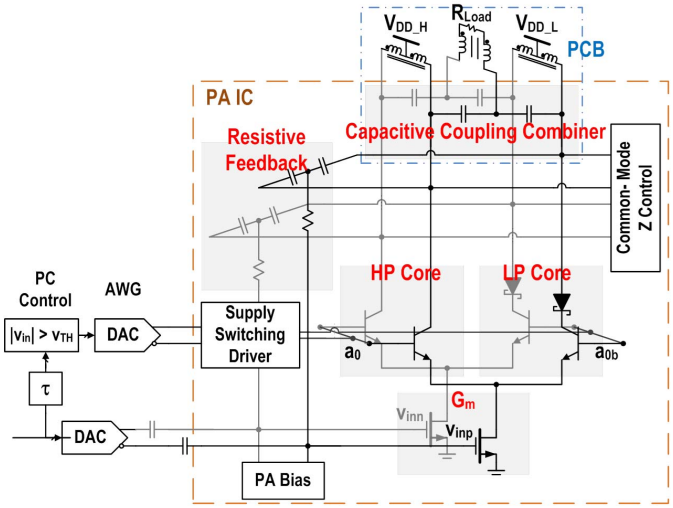

Fig. 9. PA schematic and test bench.

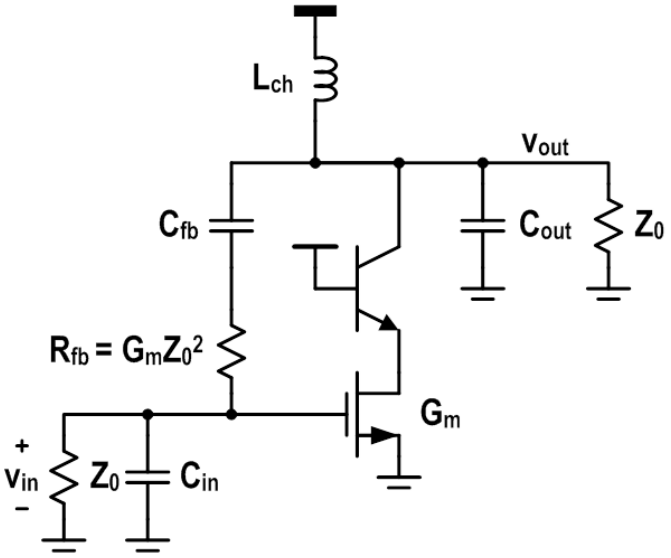

Fig. 10. Small-signal equivalent circuit of resistive shunt-feedback PA core.

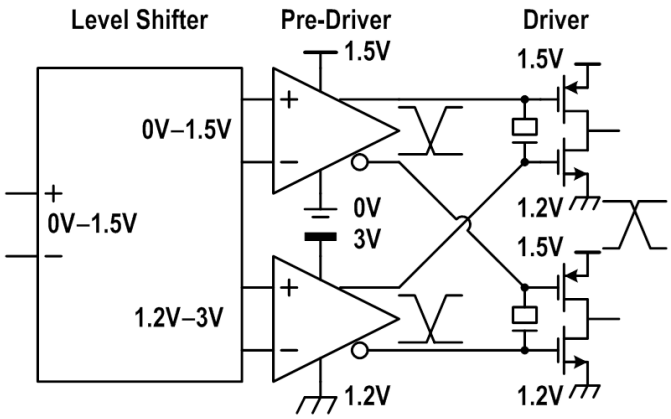

Fig. 11. SS driver.

output swing and suppresses even-order distortion. The high-power (HP) core is connected to $V_{DD\_H} = 7.5$ V, whereas the low-power (LP) core is cascoded with Schottky diode clamps for protection and then connected to $V_{DD\_L} = 4.5$ V. The clamp diodes are necessary when the supply is switched from V_{DD_H} to V_{DD_L} with strong signal magnitude. The PN junction from base to collector at LP core would turn ON without the diodes, leading to severe distortion and reliability issues. Moderate drawbacks of the clamp diodes are added capacitance and the extra headroom they require.

The PA is biased through center-tapped transformers, which prevent large voltage jumps. The proposed capacitive coupling combiner couples signal to the balun, and reduces jumps due to residual flux change in the parasitic inductances of the load circuit. Finally, a broadband 1:1 common-mode choke serves as the balun, coupling to a single-ended 75-Ω load. Resistive shunt feedback is used for wideband input and output impedance matching. The SS driver and output common-mode impedance control network are also included, and will be discussed later.

A. Resistive Shunt-Feedback PA Core

The differential-mode half circuit of the PA core is shown in Fig. 10. The shunt-feedback resistor $R_{\text{fb}} = G_m Z_0^2$ is for broadband input and output impedance matching. The voltage gain of this topology is $-A_v = -(G_m Z_0 - 1)$. The shunt-feedback topology provides output matching with better efficiency than a shunt resistor (R_{ter}) to ac ground. Power dissipation in R_{fb} is $P_{\text{out}}/(A_v + 1)$, which is very small compared to dissipation in $R_{\text{ter}} = P_{\text{out}}$. The bandwidth of the PA is from ω_{p1} to min $[\omega_{p2}, 1/(C_{\text{in}} Z_0)]$, where

$$C_{\text{fb}} \cong L_{\text{ch}}/(A_V Z_0^2) \tag{3}$$

$$\omega_{p1} \cong Z_0/(2L_{\text{ch}}) \tag{4}$$

$$\omega_{p2} \cong 2\omega_{T_{\text{BJT}}}/(\alpha G_{m_{\text{BJT}}} Z_0), \quad \alpha \cong 0.6 \tag{5}$$

$$1/(C_{\text{in}} Z_0) \cong \omega_{T_{\text{CMOS}}}/A_V. \tag{6}$$

The f_T of the NPN BJT and NMOS transistors in this process are 28 and 56 GHz, respectively. Substituting these process parameters, the PA has estimated voltage gain of 20 dB and bandwidth from 6 MHz to 1.3 GHz. Note that the input common-source devices are NMOS for higher input bandwidth, and the cascode devices are BJT for high-voltage tolerance. $\text{BV}_{\text{CBO}} = 18$ V is the critical breakdown metric (not $\text{BV}_{\text{CEO}} = 8$ V) since the NPN bases have low-impedance drive.

B. Supply-Switching Driver

The SS driver is shown in Fig. 11. It is comprises a level shifter cascaded with pre-driver and driver inverters. We use CMOS inverter drivers instead of current-mode logic (CML) drivers to save power at the expected SS rates. Note that the target signals have high PAPR, so peaks are relatively infrequent. The Class-B CMOS drivers naturally have lower quiescent power consumption than CML drivers. The level shifter [15] transfers the SS control signal to two paths. One path maintains the input 0–1.5 V levels; the second path level shifts upward to 1.2–3 V. The voltage crossings are intentionally asymmetric to establish make-before-break

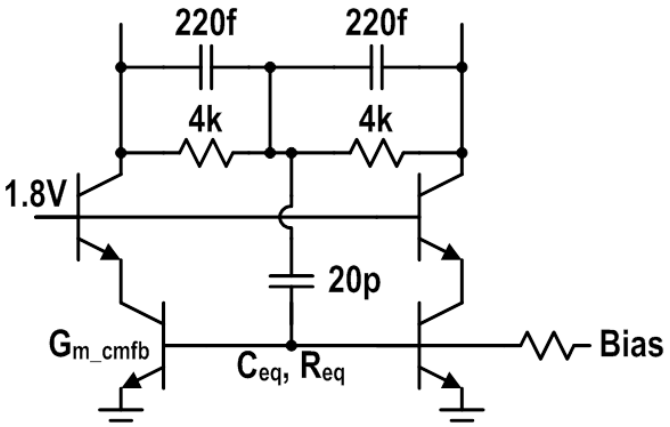

Fig. 12. Output common-mode impedance control network.

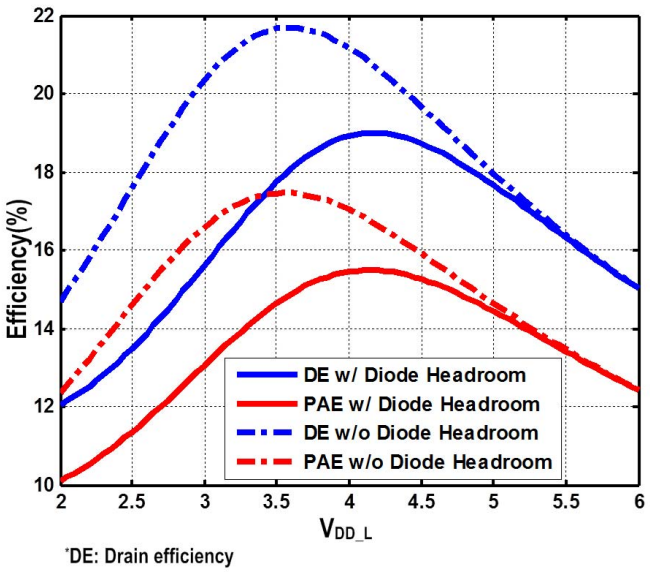

Fig. 13. Drain efficiency and PAE estimate with auxiliary circuits and headroom losses.

action in current-mode switching; this minimizes flux-change-induced voltage jumps. Varactors at the gates of the drivers time align the signals in the two paths (0–1.5 and 1.2–3 V). The swing was increased from 6 v_T = 150 to 300 mV to ensure that the current is fully switched from one power rail to another. Simulated SS bandwidth is approximately 2 GHz. The driver consumes less than 10 mW for typical signals, whereas ISS saves total dc power greater than 250 mW.

C. Output Common-Mode Impedance Control Network

The push–push Class-AB PA core generates large output common-mode current. The center-tapped bias transformer has low common-mode impedance at relatively low frequencies. Hence the output common-mode voltage signal is small enough that it does not constrict low-frequency differential swing and P_{SAT}. However, the parasitic leakage inductances have common-mode impedance proportional to frequency. At high frequencies, the increasing output common-mode voltage signal reduces the achievable undistorted differential swing, which limits P_{SAT}. To improve this, the common-mode impedance control network in Fig. 12 is paralleled with the collectors of the PA core. It has a high differential impedance of 4 kΩ and a low common-mode impedance of $(1 + 4k/R_{\mathrm{eq}})/G_{m\_\mathrm{cmfb}}$. Note that the value of feedback capacitors and resistors (220 fF and 4 kΩ) are designed to have the same ratio of C_{eq} to R_{eq} of common emitter G_m cell for flat frequency response. The simulation shows that the output common-mode impedance control network can achieve 10-GHz BW with common-mode impedance less than 50 Ω.

The dc current of common-mode feedback circuit is in total about 50 mA, 25 mA for each HP/LP core. The CMFB circuit can absorb up to ∼50-mA peak common-mode current.

D. Efficiency Estimation in Real Practice

The previous ideal efficiency calculation for ISS assumes zero voltage and current headroom. However, these are not negligible in practice. The headroom voltages of the high-voltage and low-voltage cores are 0.9 and 2 V, respectively. The low-voltage core requires higher voltage headroom due to the protection diodes (0.7 V) and residual flux change jumps (0.4 V). Note that in this paper, we use the term "voltage headroom" rather than "knee voltage." The current headroom (Class-AB standing current) is 50 mA. There is a tradeoff between current headroom and linearity due to g_m variation. When the Class-AB standing current is too low, the input-stage g_m variation over the full signal swing was found to be too large to easily invert using a digital predistortion (DPD) engine developed for this PA. Class-AB standing current is the major efficiency bottleneck in this design. An input stage with less transconductance variation is highly desirable.

Fig. 13 shows that our design can achieve drain efficiency (DE) and PAE of 19% and 15.5% when $V_{\mathrm{DD\_L}}$ is biased at 4.2 V. DE and PAE, with and without Schottky clamp-diode drop are compared in Fig. 13. Efficiency measurements were performed by averaging over an extended modulated waveform, long enough to observe the full PAPR. The power of auxiliary circuits was included, but unlimited SS speed was still assumed. $V_{\mathrm{DD\_L}}$ was increased to 4.5 V for more headroom and linearity in subsequent measurements.

IV. Measurement Results

The test setup uses a PC-controlled arbitrary waveform generator (Keysight M8190A AWG) to produce the RF input signal and SS control waveforms. Fig. 14 shows the prototype PCB and PA die photograph. The output of the PA drives an F-type coaxial connector and the 75-Ω CATV system. The chip area is 2.4×2.4 mm^2, which is pin limited (36-ball wafer-level BGA). The active area is 1.2×1.2 mm^2.

Fig. 15(a) is a plot of measured S-parameters. The PA achieves 20-dB power gain over a range of 8 to 750 MHz (3-dB points). The bandwidth discrepancy between the earlier estimate and measurement is due to the relatively large parasitic capacitance of PCB routing. The PA also achieves good input and output impedance matching over this range,

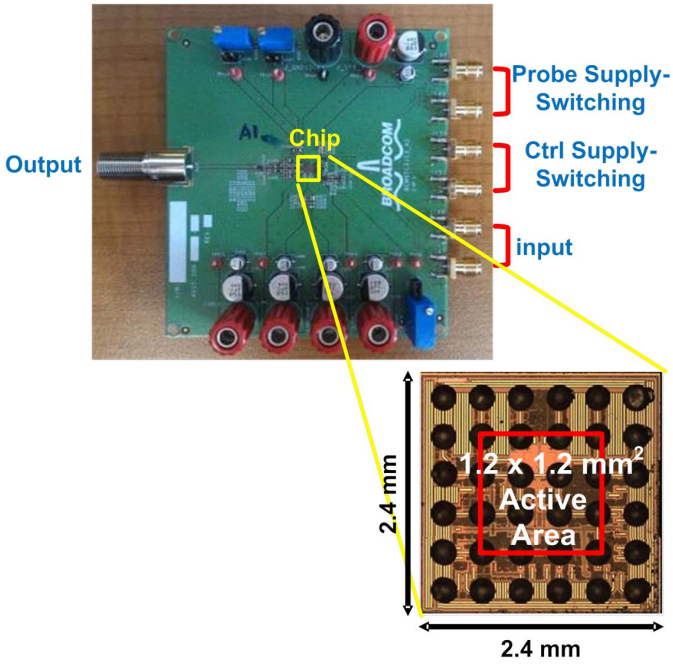

Fig. 14. PCB and die photograph.

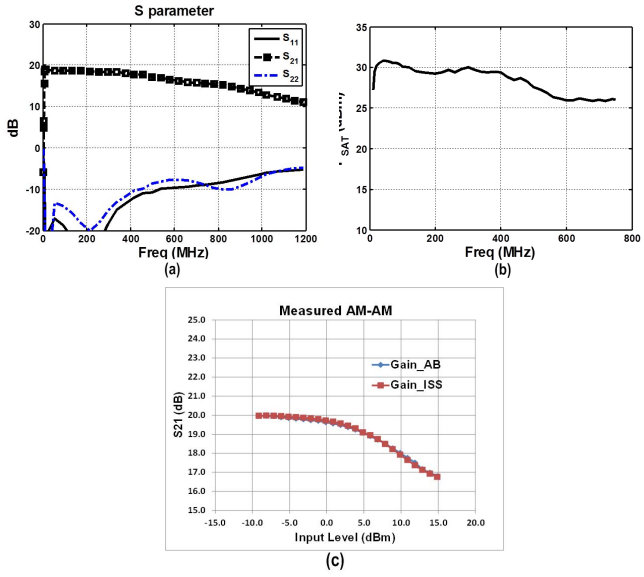

Fig. 15. Measured (a) S-parameters, (b) P_{SAT}, and (c) AM–AM at 50 MHz.

with return losses better than 8 dB. Fig. 15(b) shows measured P_{SAT}. Peak CW P_{SAT} is 31.3 dBm. This drops to 26 dBm above 400 MHz due to increasing output common-mode impedance from parasitic leakage inductance. Note that P_{SAT} would drop more without the output common-mode impedance control network. BW and P_{SAT} may be improved in the future with revised PCB design. Fig. 15(c) shows the AM–AM behavior of the PA at 50 MHz.

To verify the high-PAPR capability of this PA, we first demonstrate the output spectrum and constellation of a 10 Msym/s 256-QAM signal at carrier frequency of 100 MHz with PAPR of 9.6 dB. The PA achieves 23.6-dBm average output power, −34.8 dBc ACPR, and 2.25% error vector

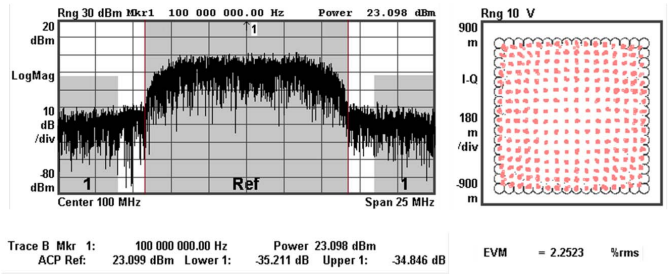

Fig. 16. Measured spectrum and constellation of 256-QAM signal.

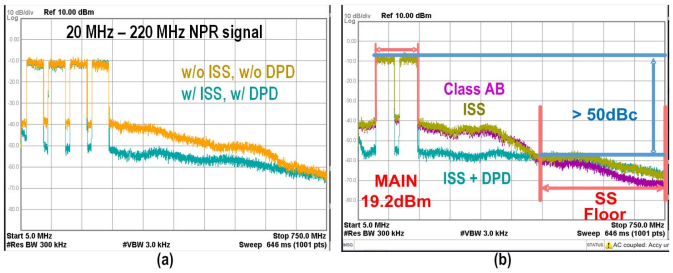

Fig. 17. Measured spectrum of (a) 20–220 MHz NPR with DPD and (b) 50–150 MHz NPR signal with DPD.

magnitude (EVM) in Fig. 16. The PAE is improved from 17% to 22.6% by applying ISS with 1-Gb/s switching rate. Consumer-grade CATV equipment designed to the DOCSIS standard is expected to reach about −40 dB EVM for 256-QAM, and about −50 dB EVM for 1024-QAM. A novel broadband DPD algorithm was applied to the PA to achieve the linearity requirements [17].

We also demonstrate performance with a 14-dB PAPR, 20-to-220 MHz noise-power-ratio (NPR) test signal with three 12-MHz notches across the band in Fig. 17(a). NPR testing is a well-established technique for evaluating broadband communication systems, such as DOCSIS [16]. NPR testing uses white Gaussian noise signals with notches. The notches allow observation of any in-band noise and distortion contributed by the system under test, and accurate measurement of signal-to-noise-and-distortion ratios. NPR notch depth can be correlated with EVM measurements [21]. PAPR was controlled by clipping, as mentioned earlier.

With this test signal, the PA achieves average power of 20 dBm with −27-dBc notch depth and side-band rejection ratio across the frequencies. The PAE is improved from 9% to 13.6% with ISS and 1-Gb/s switching rate. Note that the measured data, output power, and linearity are the same with or without ISS. The measured PAE is close to the estimated efficiency; the discrepancy is due to the finite SS rate. To prove that this DPD algorithm can be applied with ISS, we further illustrating the effectiveness of DPD applied to this PA. The notch depth/side-band rejection is improved with DPD from −27 to −40 dBc across band. The residual distortion increases at very low frequencies due to even-order effects; this may be addressed in the future work.

We also used a 14-dB PAPR, 50-to-150 MHz NPR test signal with a 12-MHz notch centered at 100 MHz. Results are presented in Fig. 17(b). We compare three cases: PA operating in Class-AB, Class-AB with ISS (1-GHz SS rate),

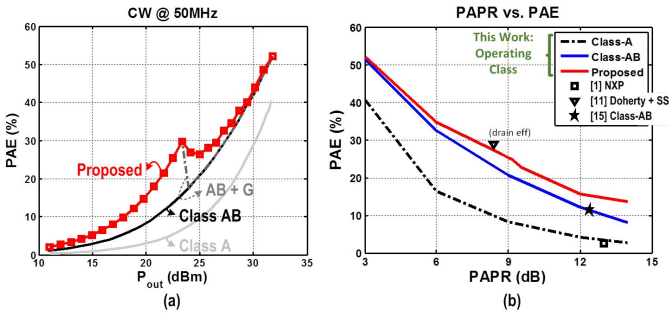

Fig. 18. Measured (a) CW efficiency at 50 MHz and (b) PAE versus PAPR.

TABLE I
COMPARISON TABLE

	This Work*		[1] NXP*	[12] ISSCC 2015	[18] ISSCC 2010	[19] ISSCC 2015
Bandwidth	8-750 (MHz)		5-205 (MHz)	3.71-4.3 (GHz)**	5.2-13 (GHz)	2-6 (GHz)
Fractional BW(%)	794		625	15	95	115
PA Technique	Proposed (Class AB + Instantaneous Supply Switching)		Class A	Class D^{-1} + Class G Doherty	Class AB	Class AB
Peak P_{out} (dBm)	31.3		29.25***	26.7	25.2	22.4
PAE (%)	22.6 (PAPR 9.6dB) 256QAM	13.6 (PAPR 14dB) NPR	2.5 (PAPR 13dB)	28.8**** (PAPR 8.4dB) 16QAM	11.2 (PAPR 6dB) BPSK	11.4 (PAPR 12.4dB) 64QAM OFDM
EVM (dB)	-31.3	N/A	N/A	<-21.5	<-24.6	< -28
ACPR(dB)	34.8	>27	>58	>31.5	N/A	N/A
Process	180nm SiGe		N/A	65nm CMOS	65nm CMOS	90nm CMOS
Area (mm^2)	5.76		25(package)	3.2	0.895	0.698

*External EM **Single channel only ***P_{1dB} ****Drain Efficiency

and Class-AB with ISS plus DPD. ISS improves PAE from 9% to 13%, and the notch depth/side-band rejection is improved with DPD from −30 to −47 dBc. Although SS artifacts increase the distortion floor somewhat at high frequencies, this effect is well below the main signal power spectrum (>50 dB). Fig. 18(a) shows measured test results with a CW sinusoid at 50 MHz. Class-AB with ISS has superior efficiency relative to established PA classes even with CW signals for the first 7 dB of power backoff.

Fig. 18(b) shows PAE versus PAPR for Class-AB with ISS at 1-Gbs SS rate shows superior efficiency versus standard wideband Class-A and Class-AB [18], [19] PAs, including the start-of-the-art commercial CATV upstream product [1]. It also achieves comparable efficiency to the narrowband Doherty switching PA with conventional supply modulation in [12]. The following waveforms were used in Fig. 18(b): for 3-dB PAPR, a single tone; for 6-dB PAPR, two tones; for 9-dB PAPR, four tones; for 9.6-dB PAPR, a 256-QAM signal; for 12-dB PAPR, a NPR signal clipped to $\pm 4\sigma$; and for 14-dB PAPR, a NPR signal clipped to $\pm 5\sigma$. Measured results are compared to recent literature in Table I, confirming our superior average efficiency for high-PAPR signals, high fractional bandwidth signals.

V. CONCLUSION

Broadband, efficient PA techniques are needed in anticipation of the forthcoming multi-carrier and multi-band communication standards. This paper has demonstrated a high-speed supply-modulation approach, ISS. Combined with a Class-AB core, it achieves superior efficiency for broadband high-PAPR signals. The intended application of this paper is CATV upstream/downstream, but extension to other systems is possible. Higher bandwidth or power may be obtained by using a greater step-up ratio (versus 1:1 in this paper).

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Jeffrey Lee (S'06–M'17) received the B.S. and M.S.E.E. degrees from National Taiwan University, Taipei, Taiwan, in 2006 and 2008, and the Ph.D. degree in electrical engineering from the University of California, Los Angeles (UCLA), Los Angeles, CA, USA, in 2017.

From 2013 to 2017, he was an Intern at Broadcom Ltd., Irvine, CA, USA, where he developed novel designs for efficient and linear broadband power amplifiers and algorithms for digital predistortion. He held a Graduate Student Fellowship at UCLA from 2010 to 2011, where he focused on microwave switch-mode power amplifiers, and was a Broadcom Graduate Student Fellow from 2012 to 2013. He is currently an Engineering Staff Member with Maxlinear, Inc., Carlsbad, CA, USA. His current research interests include RF, microwave, and broadband mixed-signal circuit designs.

Ray (Ramon) Gomez (M'81–SM'10) received the B.S. degree in biomedical engineering from Case Western Reserve University, Cleveland, OH, USA, in 1981, the M.S.E.E. degree from Stanford University, Stanford, CA, USA, in 1982, and the Ph.D. degree in electrical engineering from the University of California, Los Angeles, CA, USA, in 1993.

From 1982 to 1986, he was a Technical Staff Member at TRW Inc., Redondo Beach, CA, USA, where he involved in designing high-performance radios for aerospace applications. From 1993 to 1995, he was a member of the Disk-Drive Read Channel Design Team, Cirrus Logic, Austin, TX, USA. From 1995 to 2017, he was with Broadcom Ltd., Irvine, CA, USA, where he focused on CMOS RF circuits for cable and broadcast television tuners and DBS satellite set-top box tuners, and MoCA multimedia home networking. He is currently an Independent Consultant and an Adjunct Professor with the Electrical Engineering and Computer Science Department, University of California, Irvine, CA, USA. He holds over 100 U.S. patents and has contributed to numerous journal and conference papers. His research interests included the development of circuits and architectures for direct-sampling RF transceivers, digitally assisted RF circuits, and efficient broadband amplifiers.

Dr. Gomez was named a Broadcom Fellow in 2006 for his contributions to RF tuner design.

Sudhakar Pamarti (S'98–M'03) received the B. Tech. degree in electronics and electrical communication engineering from IIT Kharagpur, Kharagpur, India, in 1995, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, San Diego, CA, USA, in 1999 and 2003, respectively.

From 1995 to 1997, he was with Hughes Software Systems, New Delhi, India, where he was involved in the development of embedded software and firmware for a wireless-in-local-loop communication system. From 2003 to 2005, he was with Rambus Inc., Sunnyvale, CA, USA, where he was involved in high-speed I/O circuits. He is currently a Professor of electrical engineering with the University of California, Los Angeles, CA, USA.

Prof. Pamarti was a recipient of the National Science Foundation's CAREER Award for developing digital signal conditioning techniques to improve analog, mixed-signal, and radio frequency integrated circuits. He currently serves on the Technical Program Committee of the IEEE International Solid-State Circuits Conference and the Custom Integrated Circuits Conference, and as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS: Part I—REGULAR PAPERS.