A SAW-Less Tunable RF Front End for FDD and IBFD Combining an Electrical-Balance Duplexer and a Switched-*LC* N-Path LNA

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***Abstract*— This paper proposes a surface-acoustic wave (SAW)-less tunable RF front end (RF-FE) using an electrical-balance duplexer (EBD) integrated with a switched-LC N-path low-noise amplifier (LNA). The EBD cancels the transmitter–receiver (TX–RX) leakage at the RX frequency by dynamically optimizing the balance of a hybrid transformer, which enables in-band full-duplex (IBFD) operation. A transconductor-based LNA in parallel with a switched-LC N-path network creates input and output notches to reject TX leakage for frequency-division duplexing (FDD) operation. The LNA's signal-handling capability is enhanced via optimum switch biasing. Fabricated in 0.18-μm SOI CMOS, the RF-FE offers >50-dB tunable rejection from the TX port to LNA output at both TX and RX frequencies, for all 3GPP bands from 0.7 to 1 GHz (i.e., FDD case). It is the first tunable RF-FE including an LNA that achieves +70-dBm TX-path IIP_3, and <−100-dBm IM_3 at +20-dBm TX power when a full-duplex spaced jammer is applied at the antenna (FDD case). It is also the first to handle >+30-dBm in-band TX power while cancelling the self-interference by >50 dB (i.e., IBFD case). The RF-FE consumes 62.5 mW at 1 GHz with 11.7-dB RX cascaded NF, 3.6-dB TX insertion loss, and 9.62 mm^2 active area.**

***Index Terms*— Electrical-balance duplexer (EBD), in-band full duplex (IBFD), local thermal equilibrium (LTE)-frequency-division duplexing (FDD), low-noise amplifier (LNA), RF front-end (RF-FE), SOI CMOS, switched-*LC* N-path filtering, tunable.**

I. Introduction

TO ENHANCE the data rate in mobile communications, multi-band operation is necessary for commercial cellular handsets. In local thermal equilibrium (LTE) advanced, and toward 5G, the frequency-division duplexing (FDD) operation is commonly used, in which the transmitter (TX) and receiver (RX) work simultaneously, but at different frequency bands. To support FDD, the RF front end (RF-FE) has to provide adequate isolation between the TX and RX at two frequencies: 1) the TX frequency (f_{TX}), to prevent the high-power TX leakage from causing the RX low-noise amplifier's (LNA) gain compression and 2) the RX frequency (f_{RX}), to prevent TX-generated noise from RX de-sensitization [1]–[5].

The key challenge posed by FDD-LTE is that the TX-to-RX duplex spacing is as low as 40 MHz depending on the bands specification. Conventionally, surface-acoustic wave (SAW) duplexers are used to ensure sufficient isolation at both frequencies [Fig. 1(a)]. Yet, with an increasing number of bands defined toward 5G, numerous SAW resonators would be required, significantly increasing the RF-FE complexity and cost.

Recently, canceller-based RF-FEs emerge as a promising alternative to eliminate bulky off-chip resonator-based filters [1]–[5]. A canceller circuit subtracts a copy of the unwanted TX leakage at the RX input. Besides potentially providing a tunable isolation solution for FDD, cancellers also enable in-band full duplex (IBFD) [6]. IBFD is a promising candidate for future communications, allowing for increased data rate or lower power consumption [7]. In IBFD operation, the TX and RX operate simultaneously, at the same frequency ($f_{TX} = f_{RX}$) and time [8]–[14].

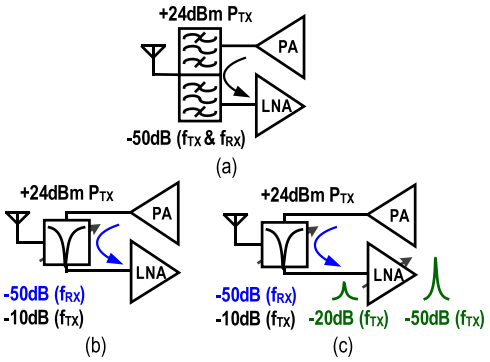

Fig. 1. (a) SAW duplexer isolates at both f_{RX} and f_{TX}. (b) Tunable single-notch EB duplexer. (c) Proposed: EBD isolates at f_{RX} and GB N-path LNA at f_{TX}.

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Several implementation challenges exist for such cancellers. First, the canceller must sufficiently reduce the TX leakage to avoid RX de-sensitization. Second, the canceller itself must handle the large TX power, avoiding device breakdown effects, while having sufficient linearity such that higher order intermodulation products do not degrade the system's post-cancellation self-interference-to-noise-and-distortion ratio [15]. Finally, the cancellation BW is critical to support modern standards. Assume an IBFD system with a 10-dB gain LNA, for a given +24-dBm TX power, with a −100-dBm link budget for third-order intermodulation distortion (IM_3) at LNA output, the cancellers are required to reach >+65-dBm input-referred third-order intercept point (IIP_3) at 50-dB isolation [16].

Several works have addressed the tradeoffs between these challenges. For example, [9] and [10] all use an architecture with a traditional copy-and-subtract path and achieve high isolation with relatively wide isolation BW, but can only handle limited TX power and exhibit poor linearity due to the use of nonlinear components within the canceller [16]. Alternatively, a circulator-based approach is proposed in [8] and [11]. However, the N-path passive mixers used directly at the antenna interface have similar limitations with respect to in-band linearity performance.

The electrical-balance duplexer (EBD) [17]–[21] [Fig. 1(b)] is another promising topology to solve this RF cancellation problem. In an EBD, a hybrid transformer provides an impedance balance between the antenna and a so-called balance network (Z_{BAL}) such that the TX leakage is nulled in the secondary winding of the hybrid transformer. EBDs exhibit high cancellation due to high-accuracy impedance tuning in Z_{BAL} (i.e., >+50 dB) [22]. Furthermore, high linearity and power-handling capability can be achieved by stacking SOI switch devices, because the EBD consists entirely of passive devices [20], [23], [24].

However, due to rapid variations of the antenna's impedance across frequency, EBDs are usually unable to provide sufficient isolation at both f_{TX} and f_{RX}, requiring a highly complex Z_{BAL} (i.e., [25]), at the cost of a large area (8.28 mm^2). The EBD in [23] and [24] only offers >50-dB isolation at f_{RX}, while the isolation at f_{TX} is degraded to less than 10 dB due to the frequency dependence of Z_{ANT}. By employing an off-chip tunable SAW filter placed prior to the on-chip LNA, the TX leakage is suppressed >40 dB in the FDD mode. To reduce size, cost, and complexity, an alternative to the tunable SAW filter in [23] and [24] is desired.

In this paper, we propose a tunable RF-FE prototype that integrates the gain-boosted (GB) switched-*LC* N-path LNA of [26] together with the EBD of [24] [Fig. 1(c)]. The LNA is self-interference resilient through rejection notches at both the RF inputs and outputs, by adding shunt inductors in the feed-forward N-path network. This technique enables high linearity, better large-signal handling capability, and dual-frequency TX-to-RX isolation. Furthermore, this paper expands on [26] with in-depth design details on the LNA, EBD-LNA co-design and its overall performances. In the proposed architecture, the EBD is set to cancell at f_{RX}, inherently providing an "IBFD mode." Except for the fact that the TX is set to a different frequency in FDD operation, no changes are made to the system when switching between FDD and IBFD operation modes. At the same time, the GB N-path filter reduces the TX leakage (FDD) and improves out-of-band (OOB) linearity (IBFD mode).

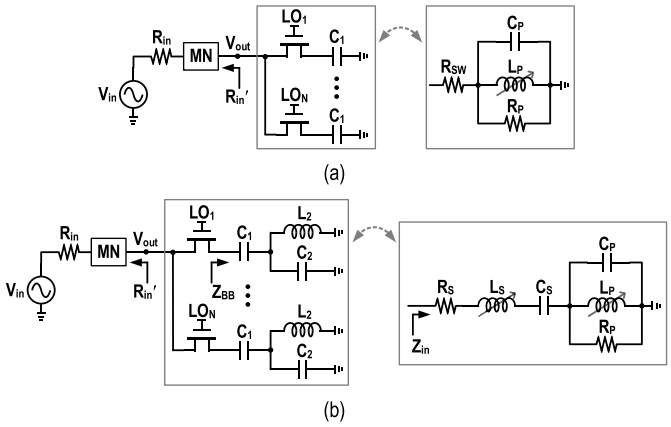


Fig. 2. (a) N-path bandpass filter and its parallel RLC model at its passband around f_{LO} [27]. (b) Lose-in notches offered by a switched-*LC* N-path network and its passband around f_{LO} and notches response can be modeled by connecting a bandpass filter in series with a bandstop filter. Switch ON-resistance (R_{SW}) is embedded in R_S. An up-converted MN is assumed to aid the stopband rejection by boosting R'_{in}.

Fabricated in 0.18-μm SOI CMOS, the RF-FE shows >50-dB tunable rejection from the TX input to the LNA output at both TX and RX frequencies, for all 3GPP bands from 0.7 to 1 GHz. It is the first tunable RF-FE including an LNA that achieves +70-dBm TX-path IIP_3 and <−100-dBm IM_3 at +20-dBm TX power when a full-duplex spaced (FDS) jammer is applied at the antenna (FDD case) and the first that handles >+30-dBm in-band TX power while providing >50-dB self-interference cancellation (IBFD case). It consumes 62.5 mW operating at 1 GHz with 11.7-dB RX cascaded NF and 3.6-dB TX insertion loss, and occupies 9.62 mm^2 active area.

II. Switched-LC N-Path Filter With Close-In Notches

A typical passive N-path filter using switches and capacitors can realize a frequency-tunable bandpass response at V_{out} [Fig. 2(a)], being a versatile alternative to SAW filters. The bandpass response can be modeled by a parallel RLC network at the vicinity of its center frequency (f_{LO}) [27]. The OOB rejection is governed by the ON-resistance (R_{SW}) of the N-path switches, and OOB impedance looking back to the input R'_{in_OOB}, and is estimated [27] as ($N = 4$)

$$\alpha \approx 20\log\left(\frac{\pi^2}{8}\cdot\frac{R_{SW}}{R'_{in\_OOB}+R_{SW}}\right). \quad (1)$$

Obviously, large R'_{in_OOB} and small R_{SW} are desired for higher OOB rejection. In (1), $\pi^2/8$ is the reciprocal of the approximated passband insertion loss in case that the in-band source impedance R'_{in_IB} is much larger than R_{SW}. For a reasonable frequency coverage (e.g., 0.7 to 1 GHz in this paper), an *LC*-based matching network (MN) can be used to upconvert the nominal 50-Ω source impedance R_{in} to a higher value. For instance, the OOB rejection improves

by 11.5 dB when $R'_{\text{in\_OOB}} = 4R_{\text{in}}$, $R_{\text{in}} = 50\ \Omega$, and $R_{\text{SW}} = 4\ \Omega$. Yet, the close-in rejection is only determined by an equivalent RC response: $f_{\text{RC}} = 1/[\pi(R'_{\text{in}} + R_{\text{SW}})C_1]$ that sets the passband -3 dB BW.

Creating notches (upper and lower sidebands) near f_{LO} to enhance the OOB rejection is possible [28]. The idea is to place a bandpass filter in series with a bandstop filter. Extending this concept to the design of an N-path filter, two notches can be created by upconverting the baseband (BB) impedance Z_{BB} to f_{LO}, as shown in Fig. 2(b). Z_{BB} is given by

$$Z_{\text{BB}} = \frac{L_2 s^2 \cdot (C_1 + C_2) + 1}{sC_1 \cdot (C_2 L_2 s^2 + 1)}. \tag{2}$$

The BB notch happens at $Z_{\text{BB}} = 0$. By zeroing the numerator, the BB notch frequency is

$$f_{\text{nt\_BB}} = 1/2\pi\sqrt{L_2(C_1 + C_2)} \tag{3}$$

which depends on the total capacitance value. As C_1 and L_2 are to be large, C_2 can be modeled as their parasitic. The RF notch frequency of the switched-LC N-path filter is

$$f_{\text{nt\_RF\_}N} = f_{\text{LO}} \pm f_{\text{nt\_BB}}. \tag{4}$$

The series resistor R_S determines the deepness of the notches, and R_P determines the passband gain. Supposing $R_S = 0$ and $R_P = \infty$, the input-impedance Z_{in} becomes

$$Z_{\text{in}} = \frac{C_S L_S C_P L_P \cdot s^4 + (C_S L_S + C_P L_P + C_S L_P) \cdot s^2 + 1}{sC_S \cdot (C_P L_P s^2 + 1)}. \tag{5}$$

The two notches can be symmetrical at f_{LO} by setting an equal resonance in both filters, bandpass, and bandstop, i.e., $C_S L_S = C_P L_P$. Thus, the notches happen at $Z_{\text{in}} = 0$ by zeroing the numerator

$$f^2_{\text{nt\_RF\_PS}} = \frac{(2C_S L_S + C_S L_P) \pm \sqrt{C_S^2 L_P^2 + 4C_S^2 L_S L_P}}{8\pi^2 \cdot C_S^2 L_S^2}. \tag{6}$$

For instance, at $f_{\text{LO}} = 1$ GHz, two close-in notches at 945 MHz and 1.055 GHz are possible with components: $C_S = 4.86$ pF, $L_S = 5.24$ nH, $C_P = 400$ pF, and $L_P = 63.4$ pH. Substituting $C_S L_S = 1/(2\pi f_{\text{LO}})^2$ into (6), $f_{\text{nt\_RF\_PS}}$ is expressed with respect to f_{LO}

$$f^2_{\text{nt\_RF\_PS}} = f^2_{\text{LO}} + 2\pi^2 f^4_{\text{LO}} \cdot \left(C_S L_P \pm \sqrt{C_S^2 L_P^2 + \frac{C_S L_P}{\pi^2 f^2_{\text{LO}}}} \right). \tag{7}$$

Mapping (4) to (7), the stopband filter is modeled with C_S

$$C_S \approx \frac{1}{8\pi^4 f^4_{\text{LO}} \cdot L_2 L_P (C_1 + C_2)} \tag{8}$$

and $L_S = 1/[(2\pi f_{\text{LO}})^2 C_S]$. The passband filter is modeled [27] as $C_P = \pi^2 C_1/4$ and $L_P = 1/[(2\pi f_{\text{LO}})^2 C_P]$ for $N = 4$.

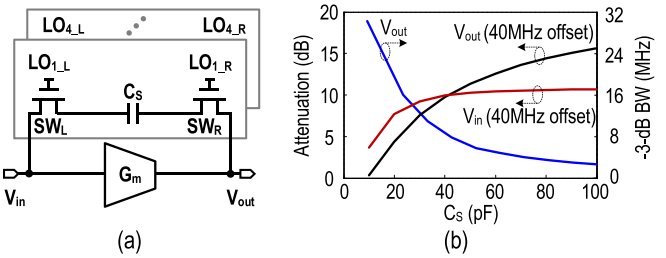


Fig. 3. (a) GB N-path LNA [30]. (b) Input and output attenuation versus C_S. The in-band -3-dB BW drops rapidly with enlarging C_S.

III. GB N-Path LNA and Its Variants

Unlike the passive N-path filter, a GB N-path LNA [Fig. 3(a)] offers not only input-impedance matching and passband gain but also higher Q bandpass responses at the input and output to improve the OOB linearity [29]–[31]. In addition, it features the Miller effect boosting the effective capacitance of the feedforward capacitors (i.e., area reduction), and lowering the effective ON-resistance of the N-path switches (i.e., power reduction).

When f_{RX} and f_{TX} are as close as 40 MHz, large C_S and small ON-resistance of SW_L (R_{SWL}) and SW_R (R_{SWR}) are crucial to improve the attenuation at f_{TX}. From simulations [Fig. 3(b)], the input rejection at 40-MHz offset saturates at $\sim$10 dB when $C_S = 50$ pF, under $R'_{\text{in}} = 200\ \Omega$, $R_L = 50\ \Omega$, $R_{\text{SWL}} = R_{\text{SWR}} = 4\ \Omega$, and $G_m = 70$ mS. Upsizing C_S to 100 pF only adds 3.5 dB more output rejection at 40-MHz offset, but almost no extra input rejection. Finally, an oversized C_S will shrink the passband BW substantially. For N-path filters, the in-band -3-dB BW and OOB rejection are always a tradeoff.

It is possible to enhance the output rejection by adding two shunt capacitors C_{SH1} and C_{SH2} to the feedforward N-path network to create close-in notches at the output, named the GB switched-C N-path LNA [32], as shown in Fig. 4(a). Under the same parameters of Fig. 3(b) and $C_{\text{SH1,2}} = 50$ pF, the simulated input and output rejections at 40-MHz offset are improved by 2.5 and 11.5 dB, respectively, as Fig. 4(b) illustrates. Meanwhile, the passband BW only decreases by 1.6 MHz when comparing $C_{\text{SH1,2}} = 0$ and 50 pF. However, since R_{SWL} (R_{SWR}) is virtually grounded by C_{SH1} (C_{SH2}) at the OOB frequency, the close-in rejection at both input and output cannot benefit from the Miller effect, implying a larger LO power budget. Similarly, the size of $C_{\text{SH1,2}}$ cannot benefit from the Miller effect, impacting the area efficiency.

Although the output rejection depends on the total shunt capacitances, the input rejection is dominated by C_{SH1}. From simulations, C_{SH1} aids the input rejection effectively [Fig. 4(c)] but not C_{SH2} [Fig. 4(d)]. Considering that the input rejection is more critical to reduce the TX leakage, C_{SH2} can be downsized with respect to C_{SH1} to reduce the die area and parasitic effects. A similar scenario happens for R_{SWL} and R_{SWR}. Simulated with $C_S = C_{\text{SH1,2}} = 50$ pF, ideally 10 dB more input rejection is achieved when R_{SWL} is downsized from 30 to 0 Ω [Fig. 4(e)], while R_{SWR} does not contribute to input rejection [Fig. 4(f)].

As shown in Fig. 5(b), adding an inductor L_{SH1} in series with C_{SH1} [Fig. 5(a)] can enhance both the input and output

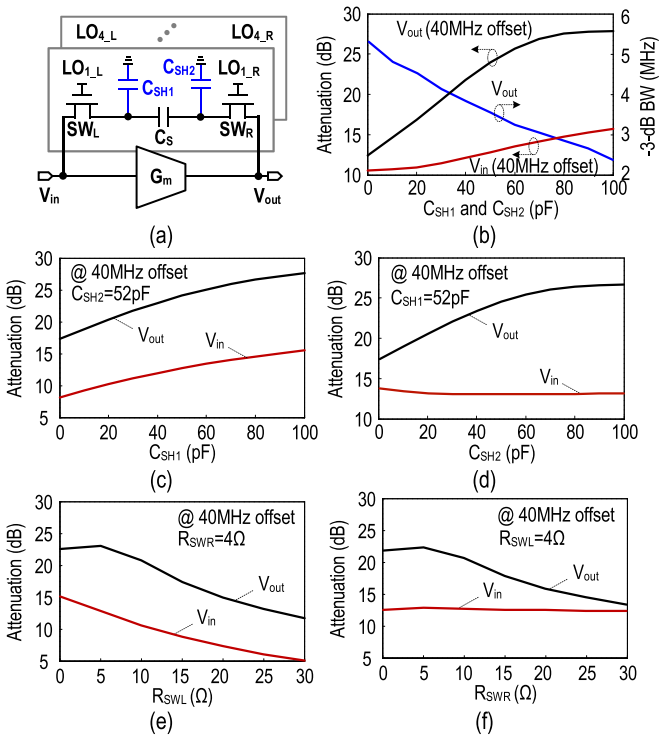


Fig. 4. (a) GB switched-C N-path LNA [32]. (b) Input and output attenuation increases when enlarging C_{SH1} and C_{SH2}, but the in-band -3-dB BW decreases. (c) C_{SH1} contributes to both the input and the output attenuations. (d) C_{SH2} only contributes to the output attenuation. (e) SW_L determines both the input and output attenuation. (f) SW_R only determines output attenuation. Output notch is created due to the current cancellation. Simulated with $C_S = 50$ pF and $G_m = 70$ mS at 1 GHz.

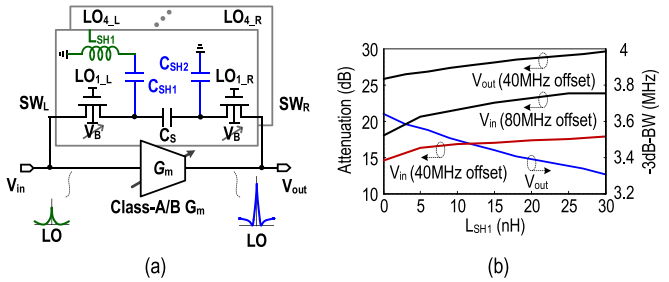


Fig. 5. (a) Proposed switched-LC N-path LNA with class-A/class-B G_m. (b) Adding L_{SH1} enhances both input and output attenuation without sacrificing -3 dB BW. After adding L_{SH1}, an input notch is created. Simulated with $C_S = C_{SH1} = C_{SH2} = 50$ pF and $G_m = 70$ mS at 1 GHz.

rejections at close-in frequencies. Specifically, an input notch is created, and the output notch spacing from f_{LO} is reduced without sacrificing the passband BW. As shown in Fig. 5(b), the simulated input rejection improves 3.2 dB at 40-MHz offset and 6.1 dB at 80-MHz offset as L_{SH1} increases from 0 to 30 nH. The output rejection also improves by 4.1 dB at 40-MHz offset and 2.5 dB at 80-MHz offset. The main expense is the chip area occupied by the spiral inductors.

The improved input rejection enhances the LNA linearity [33], especially for the FDS jammer test, in which the equally duplexed TX leakage and an OOB jammer (at $2 \times f_{TX} - f_{RX}$) generate IM_3 falling at f_{RX}. The IM_3 term determines the OOB-IIP_3, which is

$$\text{OOB-IIP}_3 = (2P_{TX} + P_{JMR} + A_{LNA} - P_{IM3})/2 \quad (9)$$

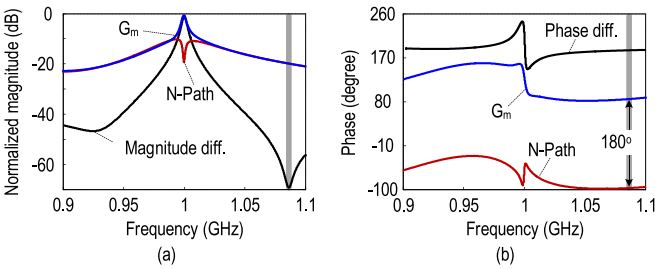


Fig. 6. (a) Normalized magnitude and (b) phase responses of the currents of G_m and N-path network. When the magnitudes of the two currents are equal, the notch occurs when their phase difference is 180°.

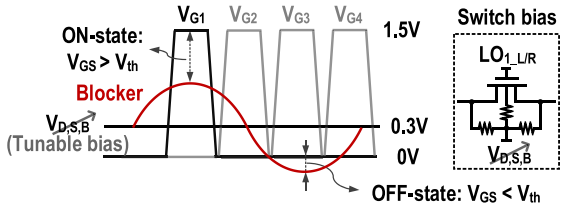


Fig. 7. N-path switches (SW_L and SW_R) voltage biasing for handling a large blocker.

where P_{TX} and P_{JMR} are the power of the TX leakage and jammer, respectively and A_{LNA} is the gain of the LNA. With improved rejection Δ_{TX} at f_{TX} and Δ_{JMR} at f_{JMR}, P_{IM3} reduces by $2 \times \Delta_{TX} + \Delta_{JMR}$, and OOB-$IIP_3$ improves by $\Delta_{TX} + \Delta_{JMR}/2$.

Unlike input rejection, output rejection does not effectively contribute to the LNA linearity improvement since the IM_3 term is already generated at f_{RX} prior to reaching the output. In fact, high output rejection mainly relaxes the linearity requirements of the following RX chain.

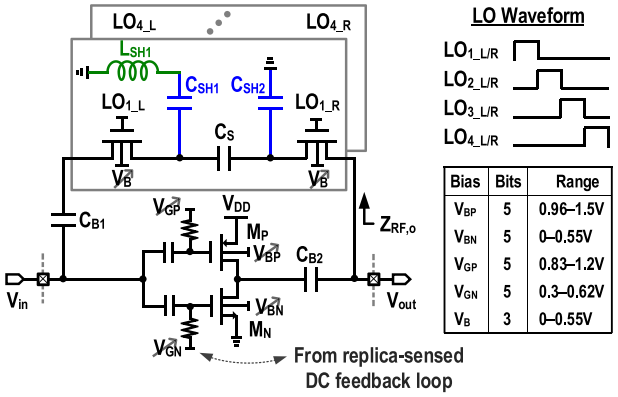
The close-in output notch is due to the zeros generated by current cancellation between the two paths: the switched-LC N-path network and G_m [28]. In Fig. 6, the notch occurs where the two signal currents are equal in magnitude and 180° out of phase. Interestingly, the notch can be located at the lower or the upper sideband of f_{LO} by tuning the bias of the N-path switches or the body/gate bias of G_m, thus, adjusting the phase response [28].

IV. Implementation of GB Switched-LC N-Path LNA

A. Optimally Biased N-Path Switches

To handle large blockers, the gate/drain/source bias ($V_{G,D,S}$) of the N-path switches has to be considered during both ON and OFF periods. During the ON period, the voltage difference, $V_G - V_S$, should be large in order to achieve a low ON-resistance. In fact, the LO swing should be greater than the maximum swing of the interferer by at least a threshold voltage V_{th} (Fig. 7) to prevent unwanted turn OFF. During the OFF period, a negative voltage difference of $V_G - V_S$ aids to prevent any undesired turn ON of the N-path switches when a large interferer is present. It is crucial to ensure that the minimum LO swing is not larger than the interferer swing by at least a V_{th} during the OFF period (Fig. 7).

With an LO swings between 0 and 1.5 V, the optimum N-path switch bias ($V_{D,S,B}$) is 0.3 V, which leads to a simulated input-referred OOB-blocker caused -1-dB IB-gain



Bias	Bits	Range
V_{BP}	5	0.96–1.5V
V_{BN}	5	0–0.55V
V_{GP}	5	0.83–1.2V
V_{GN}	5	0.3–0.62V
V_B	3	0–0.55V

Fig. 8. Schematic of the proposed switched-*LC* N-path LNA. Bias voltages are programmed for fine tuning the linearity.

compression (OOB-iB$_{1dB}$) of +13.2 dBm. The OOB-iB$_{1dB}$ drops by 3.3 dB for $V_{D,S,B} = 0$ V, which implies the OFF-state case is not handled well. Also, the OOB-iB$_{1dB}$ will degrade by 4.5 dB if a fixed $V_{D,S,B} = 0.6$ V is set. The linearity of the LNA is closely related with the LO swing. The simulated OOB-iB$_{1dB}$ can reach +19.2 dBm when having a 2-V LO swing and $V_{D,S,B} = 0.7$ V, at the price of power consumption when using thick-oxide devices with higher parasitic capacitance. Unlike [32], that ac couples to allow gate biasing, the overdrive voltage of the N-path switches is adjusted here by programming $V_{D,S,B}$. This approach avoids the parasitic capacitance of the ac-coupling capacitors from degrading the effective LO swing, and thereby LO generator (LOGEN)'s power efficiency, which reduces the power consumption by 10 mW.

B. Device Sizing and Performance Tradeoffs

Fig. 8 details the schematic of the GB switched-*LC* N-path LNA. C_S is designed with a value of 52 pF, with $L_{SH1} = 15$ nH and $C_{SH1} = 80$ pF and $C_{SH2} = 52$ pF. For the inverter-like class-A/class-B G_m, accurate tunable bias voltages (5-bit resolution) for both the body ($V_{BP,N}$) and gate ($V_{GP,N}$) are designed, enabling optimization of the small-signal linearity [34]. The switch bias $V_{D,S,B}$ is implemented with 3-bit resolution, covering 0 to 0.55 V (0.3-V nominal). The series capacitors $C_{B1,2}$ are added to ensure the switch bias tuning. All biases are programmable via a serial-parallel interface.

The large-signal linearity of the LNA is determined by its load impedance and G_m. The load impedance is dominated by the up-converted OOB-impedance $Z_{RF,o}$ (Fig. 8) from the N-path switched-*LC* network. G_m (88 mS) does not vary with the input power level as long as $Z_{RF,o}$ is close to zero, which is around +9 dBm in simulation. The G_m is biased with a dc feedback loop in Fig. 9(a), in which V_{GN} changes adaptively with V_{GP} (tuned by a current mirror) while keeping the output dc level of G_m at $V_{DD}/2$. To avoid blocker-caused output dc variation, we employ a 10×-downsized G_m replica [Fig. 9(a)]. The simulated phase margin of the dc feedback loop is 95°.

The inductor L_{SH1} adds an extra degree of freedom to trade the power consumption with the stopband rejection achieved by the GB N-path LNA. The power consumption of this LNA is thus reduced compared to sub-100 nm

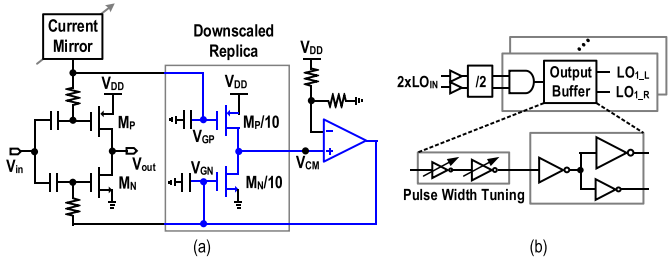


Fig. 9. (a) Output dc level of the G_m stage is set by mirroring it to a downscaled replica under a dc feedback loop. (b) 25%-duty-cycle LOGEN.

implementations with similar rejection [32], [35], even when using a 0.18-μm SOI CMOS technology with a much lower f_T. To ensure the OOB rejection is not limited by the ON-resistance of the N-path switches, $R_{SWL} = 2\ \Omega$ (SW$_L$: 160/0.18 μm) and $R_{SWR} = 4\ \Omega$ (SW$_R$: 80/0.18 μm) are selected. As discussed in Section III, R_{SWR} does not impact the input filtering response that is deemed as the most critical to combat with the OOB interference.

Thanks to smaller SW$_R$, the LOGEN saves 10.5-mW dynamic power and finally consumes 57.2 mW at 1 GHz, of which 65% is due to the LO switch drivers. Fig. 9(b) shows the 25%-duty-cycle LOGEN [36]. Differential master clocks $2 \times$ LO$_{IN}$ are provided externally. The output buffer of LOGEN is designed with four inverter stages, where the first two stages are designed in a tunable fashion (3-bit resolution) to allow the change of the pulse width of the LO waveforms (±10% range). The last two stages are designed with a fan-out of 2 and 0.6 in terms of equivalent capacitive load to both enable the drive of the large SOI N-path switches, and optimize the power consumption. The simulated phase noise is −165 dBc/Hz at 40-MHz offset from Spectre's pss and pnoise at 1 GHz, which is mainly dominated by the input buffer and "AND" logic. The frequency divider Div/2 does not contribute noise to the output LO waveforms because the rising/falling edges are derived from the $2 \times f_{LO}$ pulses.

The LNA is studied in two modes: default and high rejection; depending mainly on the bias voltage of the N-path switches and the LO overlap. In the default mode, the V_{BP} (V_{GP}) of G_m are 1.2 (1.08) V and 0.3 (0.45) V for transistors M_P and M_N (Fig. 8), respectively, and $V_{D,S,B}$ is 0.3 V. The LO waveforms are non-overlapped. Compared to the default mode, the high-rejection mode is achieved by reducing $V_{D,S,B}$ of the N-path switches (to 0.12 V) to enlarge the switch overdrive voltage and overlapping the LO waveforms through tuning the PMOS/NMOS size ratio of the LOGEN's output buffer, thus reducing the ON-resistance of the N-path switches and, subsequently, improving the rejection for close-by frequencies. However, reducing $V_{D,S,B}$ causes undesired turn ON during the LO's OFF period when large TX leakage appears at the LNA's input, and overlapping LO waveforms leads to crosstalk between paths, resulting larger LO leakage and gain drop [27].

V. Fully Integrated Tunable RF-FE With EBD and GB Switched-LC N-Path LNA

The single-ended EBD from [24] is re-employed here for co-design and integration with the proposed N-path LNA.

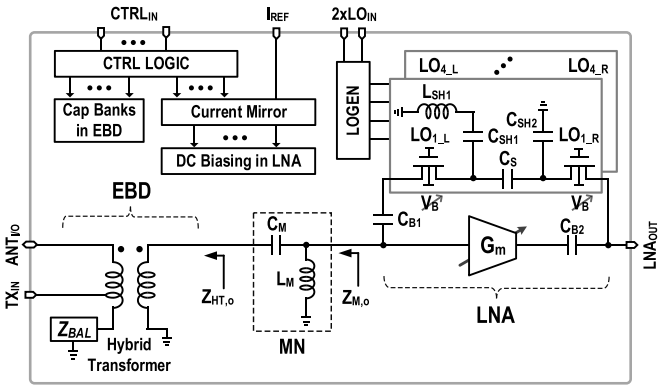


Fig. 10. Proposed RF-FE. The EBD contains a hybrid transformer and a balance-impedance network ($Z_{\rm BAL}$) [24], and it is connected with the switched-*LC* N-path LNA through an *LC*-MN.

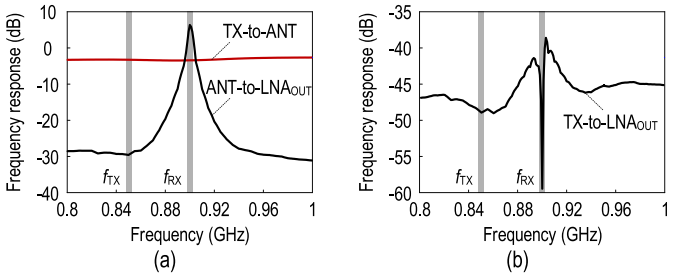


Fig. 11. Simulated frequency response for EBD-LNA. (a) ANT-to-$\rm LNA_{OUT}$ path and TX insertion loss. (b) TX-to-$\rm LNA_{OUT}$ isolation response.

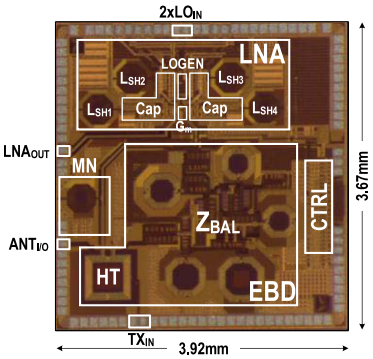


Fig. 12. Chip micrograph of the RF-FE (EBD + LNA).

It balances an off-chip ANT impedance ($Z_{\rm ANT}$) with an on-chip balance network ($Z_{\rm BAL}$) to cancel TX-to-LNA interference using a hybrid transformer. The EBD achieves TX-to-LNA isolation via IB cancellation, supporting the IBFD application. EBDs can only provide sufficient TX–RX isolation at either $f_{\rm RX}$ or $f_{\rm TX}$ due to the limited isolation BW, considering the frequency dependence of a real antenna. In [24], the EBD provides >50-dB isolation at $f_{\rm RX}$ to cancel the TX-generated noise by tuning $Z_{\rm BAL}$. To support FDD, a tunable SAW filter is used in [24] to suppress the high-power TX leakage, which occupies a rather large area. Here, the GB switched-*LC* N-path LNA is utilized instead of the tunable SAW to suppress the remainder of the TX leakage.

The proposed RF-FE is shown in Fig. 10, including the single-ended EBD, switched-*LC* N-path LNA and an *LC* inter-stage MN. The TX input tap of the hybrid transformer is skewed toward $Z_{\rm BAL}$ to reduce the RX insertion loss. The magnitude of $Z_{\rm BAL}$ is tuned to be larger than the optimum TX–RX isolation impedance (∼30 Ω) at $f_{\rm TX}$ to improve the TX insertion loss, while preserving a >50-dB cancellation condition at $f_{\rm RX}$ [24]. Before connecting to the switched-*LC* N-path LNA, an *LC*-MN is introduced to up-transform $Z_{{\rm HT},o}$, since a large transformed impedance $Z_{M,o}$ enhances the TX leakage attenuation of the N-path filtering. Based on (1), the estimated ultimate OOB rejection is

$$\alpha \approx 20\log\left[\frac{\pi^2}{8}\cdot\frac{R_{\rm SWL}+R_{\rm SWR}}{R_{M,{\rm TX},o}(1+A_O)+R_{\rm SWL}+R_{\rm SWR}}\right] \quad (10)$$

where $R_{M,{\rm TX},o}$ is the resistance of $Z_{M,o}$ at $f_{\rm TX}$ and A_O is the open-loop gain of the LNA. Due to the gain stage, $R_{M,{\rm TX},o}$ is boosted to $R_{M,{\rm TX},o}$ $(1+A_O)$ [31]. The OOB ultimate attenuation can be enhanced by increasing A_O and enlarging the N-path switches. However, A_O is limited by the G_m linearity which implies higher dynamic power to drive larger switches. Thus, the up-transformed $R_{M,{\rm TX},o}$ provides additional freedom to balance the attenuation, A_O, and power consumption. With $R_{M,{\rm TX},o}=300\ \Omega$, and the ultimate OOB attenuation is ∼45 dB with $A_O=10$ dB, $R_{\rm SWL}=2\ \Omega$, and $R_{\rm SWR}=4\ \Omega$.

The EBD-LNA *LC*-MN is implemented with a series capacitor C_M (1.15 pF) and a shunt inductor L_M (12.84 nH) to achieve a resonance frequency of ∼850 MHz, when considering the parasitic capacitance from both the metal lines and the LNA (∼1.2 pF). The RF-FE is simulated in ADS by using the extracted S-parameters of a spectre-simulated switched-*LC* N-path LNA and an EMX-simulated model for the hybrid transformer, inductors and interconnects. The simulated frequency responses are shown in Fig. 11, where the $f_{\rm RX}$ and $f_{\rm TX}$ are 900 and 850 MHz, respectively. For the TX path, the insertion loss is −3.3 dB [Fig. 11(a)]; in the RX path the TX attenuation is observed as >35 dB at ≥40 MHz offset from the small-signal viewpoint. The ANT-to-LNA gain is 6.3 dB, of which the EBD insertion loss is 3.5 dB, and the LNA's gain is simulated to be 9.8 dB. In Fig. 11(b), the proposed RF-FE provides ∼50-dB TX-to-$\rm LNA_{OUT}$ isolation at $f_{\rm TX}$ (40-MHz offset), reduced by 9.8-dB LNA gain (referred to the LNA input) at $f_{\rm RX}$.

VI. Measurement Results

The RF-FE is fabricated in 0.18-μm SOI CMOS. In Fig. 12, the RF-FE occupies a total chip area of 14.4 $\rm mm^2$, with 9.62 $\rm mm^2$ active area. An on-chip series-parallel interface denoted CTRL programs all voltage biasing and tuned capacitor banks. Two external supplies were used for the nominal and I/O supply references (1.5 and 2.5 V, respectively). The chip is tested on printed circuit boards and measured without any RF buffers, directly sourcing or loading all SMA ports with the 50-Ω instruments. The measurement results cover both FDD and IBFD operations. Although the effect of a real antenna's impedance is not tested in this paper, this does not limit the EBD to provide TX–RX isolation with a real antenna since $Z_{\rm BAL}$ is a complex tunable-impedance structure [37]. $Z_{\rm BAL}$ is designed to isolate at $f_{\rm RX}$ (>40 dB) and provide

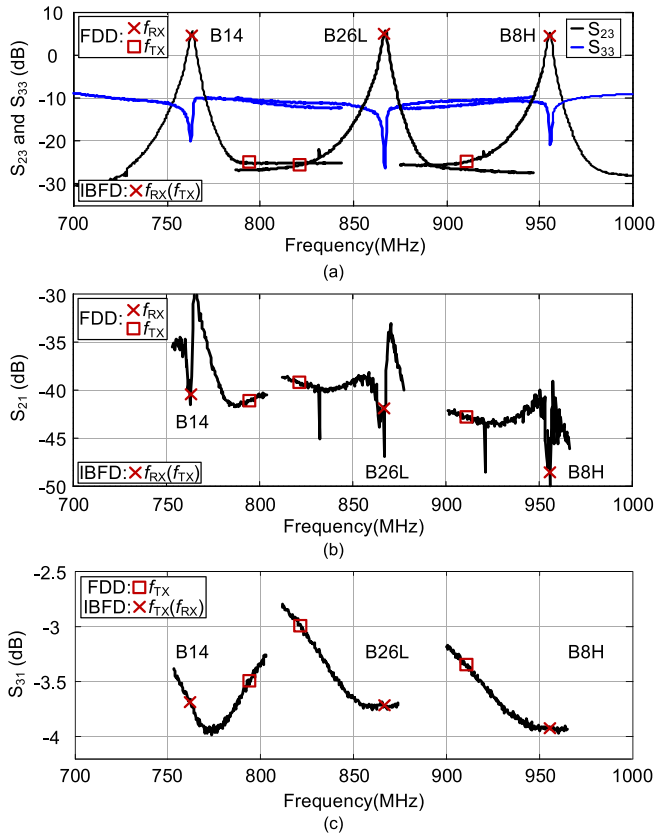


Fig. 13. Measured frequency response for both the FDD and IBFD operations at the LNA's default mode. The TX input, LNA output, and ANT input/output map to ports 1, 2, and 3, respectively. (a) ANT-to-LNA path. (b) TX-to-LNA_{OUT} isolation at both f_{TX} and f_{RX}. (c) TX insertion loss.

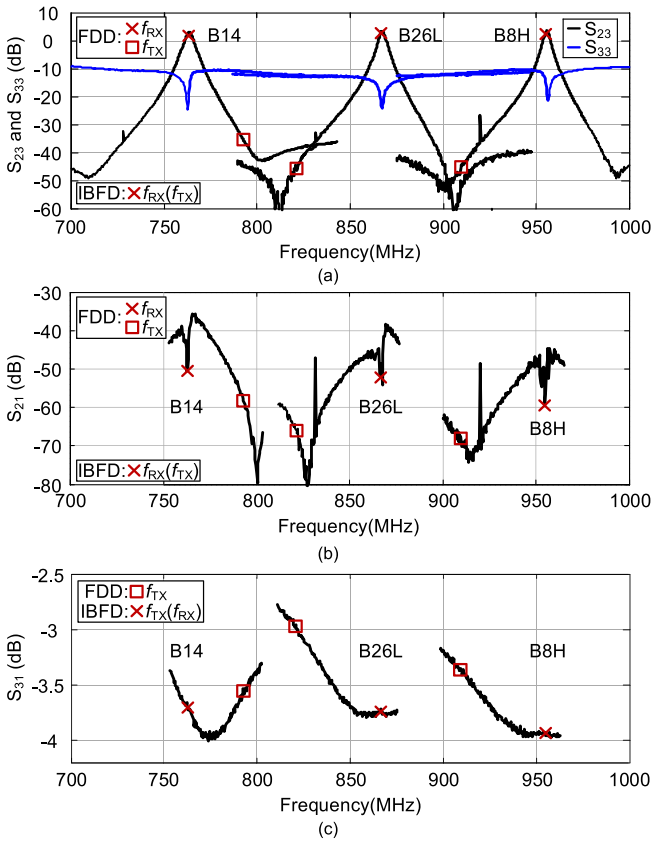


Fig. 14. Measured frequency response for both the FDD and IBFD operations at the LNA's high-rejection mode. The TX input, LNA output, and ANT input/output map to ports 1, 2, and 3, respectively. (a) ANT-to-LNA path. (b) TX-to-LNA_{OUT} isolation at both f_{TX} and f_{RX}. (c) TX insertion loss.

impedance optimization flexibility at f_{TX} (>10-dB isolation) for better loss in FDD mode, increasing the complexity of Z_{BAL} and limiting the isolation BW at f_{RX} [23], [24]. In addition, a signal generator is used to generate the TX signal; even its noise floor is much smaller than a typical power amplifier which is around −130 dBm/Hz for LTE. However, after −50-dB rejection in the EBD, the noise added to the LNA input is −180 dBm/Hz which is much smaller than the −174 dBm/Hz noise floor from 50 Ω (the same noise specification in a typical SAW-based FDD system).

The RF-FE is measured with off-chip impedance MNs at TX input (port 1) and LNA output (port 2). The antenna is referred to as port 3 in subsequent measurements. A 4.7-pF shunt capacitor is added at the TX input port, and an *LC* network with 13-nH series inductor and 2.4-pF shunt capacitor added at the LNA output port. In Fig. 13(a), the frequency response (S_{23} and S_{33}) at ANT-to-LNA response is shown for FDD (band 14, band 26L, and band 8H) and IBFD operation at the default mode, in which the passband gain at f_{RX} ranges from 4.8 to 5.5 dB with a −3-dB BW of 3.8 MHz. In FDD operation, the rejection at f_{TX} varies from −31 to −30.2 dB. The IB S_{33} < −18 dB is consistently measured at different bands. Fig. 13(b) shows the measured TX-to-LNA_{OUT} frequency response (S_{21}), demonstrating the isolation at both f_{TX} and f_{RX} for FDD and IBFD operations in the default mode. The isolation BW is 30 MHz at f_{TX} for >44-dB isolation (FDD operation), which is determined by the bandpass response of the N-path filter. The isolation at f_{RX} is due to the Z_{BAL} tuning of the EBD, which is >40 dB with 3.2-MHz BW (FDD and IBFD operations). Fig. 13(c) illustrates the measured co-optimized TX insertion loss (S_{31}), which ranges from 2.9 to 3.5 dB for FDD operation and from 3.7 to 3.9 dB for IBFD operation. Further, loss optimization is not possible for reverse bands (e.g., B14), and B14 has a 30-MHz TX–RX frequency offset compared to 45 MHz for B26 and B8 in FDD operation. Deep notches disappear at around f_{TX} [Fig. 13(a)] in the default mode should be due to the reduced duty cycle of LO waveforms and the wire resistance in the N-path filter network.

In the high-rejection mode, Fig. 14(a) shows the measured S_{23} and S_{33}, where the passband gain at f_{RX} ranges from 1.1 to 1.8 dB for FDD and IBFD operations. The rejection at f_{TX} varies from −48.5 to −39.4 dB in FDD operation. The measured TX-to-LNA_{OUT} isolation (S_{21}), shown in Fig. 14(b), reveals an isolation of >55 and >50 dB for 10.4- and 1.5-MHz BW in FDD operation at f_{TX} and f_{RX}, respectively, and >50 dB for 1.5-MHz BW in IBFD operation at f_{RX} (f_{TX}). Fig. 14(c) displays the measured co-optimized TX insertion loss (S_{31}), which ranges from 2.9 to 3.6 dB for FDD operation and from 3.7 to 3.9 dB for IBFD operation in the high-rejection mode.

In Fig. 15(a), the measured OOB-IIP_3 is +26.7 and +35.1 dBm for the default and high-rejection modes in both FDD and IBFD operations, respectively, at ANT-to-LNA path.

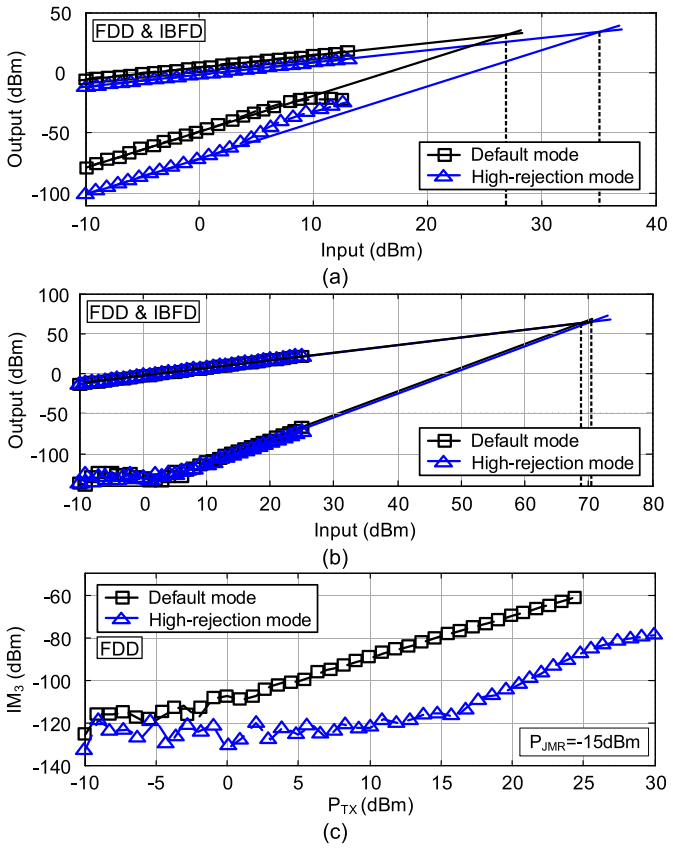


Fig. 15. (a) Measured ANT-to-LNA path OOB-IIP$_3$ for both FDD and IBFD operations. (b) Measured TX-to-ANT path IIP$_3$ for both FDD and IBFD operations. (c) IB-IM$_3$ at LNA output in FDS jammer test for FDD operation.

The two test tones are located at 785 and 825 MHz, and the generated IB-IM$_3$ tone is at 865 MHz. For the OOB-IIP$_3$ measurements, a set of dielectric filter banks are added to isolate the two signal generators. Also, attenuators ($\sim$10 dB) are used at the RF-FE input and output ports to improve port matching, while reducing the sensitivity to impedance mismatch [20]. At the TX-to-ANT path, the measured IIP$_3$ is $+70$ and $+71$ dBm as shown in Fig. 15(b) for the default and high-rejection modes, respectively, in both FDD and IBFD operations. This is improved with respect to the results obtained in [24]. Close scrutiny revealed the TX leakage remainder at the LNA input generates an IM$_3$ product that travels to the antenna, and the SAW-side tuned capacitor banks were designed to be less linear than this paper's LNA input (which rejects both tones directly at the input). Thus, it is the authors' belief that this test is the first time where the actual Z_{BAL} linearity limits are observed at the antenna port.

Fig. 15(c) shows the measured IB-IM$_3$ versus TX power in FDD operation, for both the default and high-rejection modes for FDS jammer test, where a jammer is applied to the ANT port at the full-duplex frequency spacing from the TX signal ($2 \times f_{\mathrm{TX}} - f_{\mathrm{RX}}$) and the IM$_3$ measured at the LNA output. In Fig. 15(c), the noise floor is around -120 dBm. The measured IM$_3$ increases above the noise floor in the default mode from around -2-dBm TX power, while around $+16$ dBm in the high-rejection mode. The test

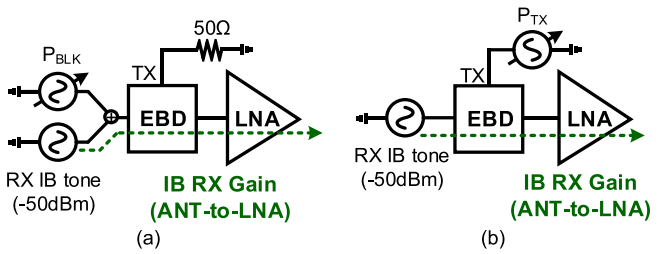


Fig. 16. Measurement setup for (a) blocker-caused OOB-iB$_{1\mathrm{dB}}$ (TX port is terminated to 50 Ω) in FDD and IBFD operations and (b) TX-caused OOB-iTX$_{1\mathrm{dB}}$ (FDD operation) and iTX$_{1\mathrm{dB}}$ (IBFD operation).

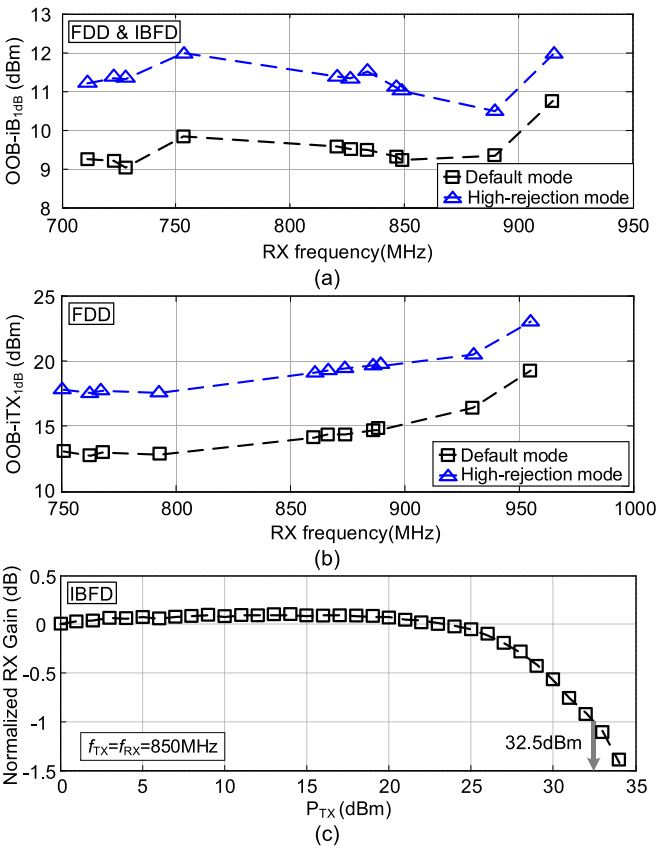


Fig. 17. Measured (a) blocker-caused OOB-iB$_{1\mathrm{dB}}$ for FDD and IBFD operations and (b) TX-caused OOB-iTX$_{1\mathrm{dB}}$ versus f_{RX} at 40-MHz offset for ANT-to-LNA path in FDD operation. (c) Measured TX-caused gain compression (iTX$_{1\mathrm{dB}}$) in IBFD operation.

was done at 825-MHz f_{TX}, 785-MHz f_{JMR}, and 865-MHz f_{RX}, and the jammer power is -15 dBm (3GPP standard specification). To the authors' knowledge, this is the first time an integrated dual-frequency-tunable RF-FE including the LNA achieves such a high linearity (e.g., $>+70$-dBm TX-path IIP$_3$ and below -100-dBm IM$_3$ at $+20$-dBm TX power for the FDS-test) in FDD operation.

Fig. 16(a) shows the measurement setup for OOB-iB$_{1\mathrm{dB}}$, with the TX port terminated with 50 Ω to avoid reflection. The blocker is applied to the ANT port and located at 40 MHz offset from f_{RX} and in Fig. 17(a) the measured OOB-iB$_{1\mathrm{dB}}$ in FDD and IBFD operations varies from $+9.1$ to $+10.8$ dBm for the default mode and from $+11.2$ to $+12$ dBm for the high-rejection mode. The measurement setup for input-referred

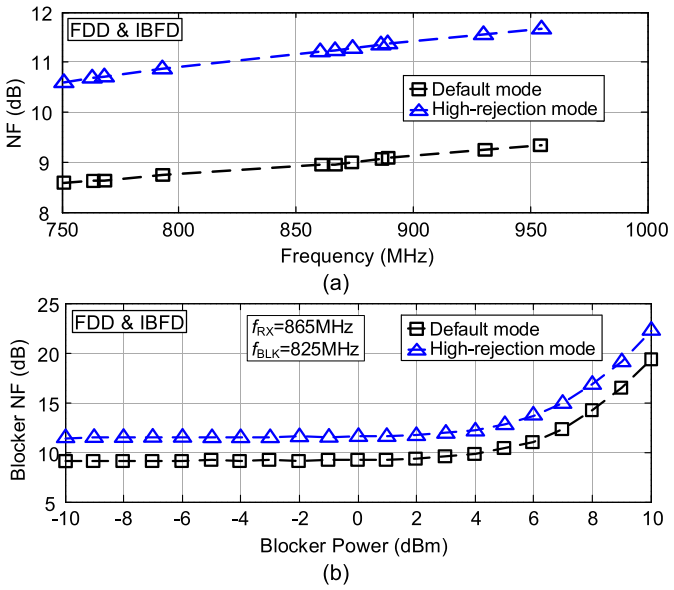


Fig. 18. Measured (a) NF and (b) blocker NF (blocker at 40-MHz offset) at ANT-to-LNA path for both the default and high-rejection modes in FDD and IBFD operations. The NF and blocker NF is measured with TX port terminated to 50 Ω.

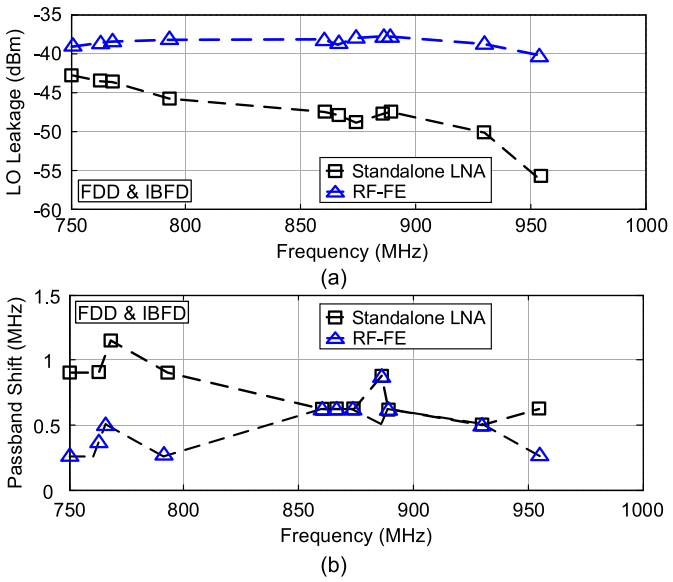


Fig. 19. (a) Measured LO leakage at antenna port versus frequency. (b) Measured center-frequency shifting versus frequency in ANT-to-LNA path.

OOB-TX-caused −1-dB RX gain compression, OOB-iTX$_{1dB}$, is also shown in Fig. 16(b). The measured OOB-iTX$_{1dB}$ [Fig. 17(b)] varies from +13.4 to +19 dBm for the default mode and from +17.8 to +23.1 dBm for the high-rejection mode in FDD operation. Both OOB-iB$_{1dB}$ and OOB-iTX$_{1dB}$ are dominated by the LNA. The variation (∼5 dB) across f_{RX} is due to the varied isolation profile versus frequency provided by EBD. Based on the measurement setup in Fig. 16(b) with equal f_{RX} and f_{TX} in IBFD operation, the measured iTX$_{1dB}$ reaches as high as +32.5 dBm at 850 MHz, as shown in Fig. 17(c), indicating the RF-FE has a very high in-band power-handling. When two in-band TX signals (+10 dBm) are injected to TX port, the estimated IM$_3$ (from the EBD's isolation and the LNA's linearity) at the LNA's output is −96.2 (−121.7) dBm at the default (high-rejection) mode for IBFD operation, which is dominated by the LNA in-band IIP$_3$ that is +3.4 (+4.6) dBm at the default (high rejection) mode.

Fig. 18(a) shows the measured NF (with the TX port terminated with 50 Ω) for FDD and IBFD operations, which ranges between 8.7 and 9.2 dB from 0.7 to 1 GHz for the default mode and 10.6 to 11.7 dB for the high-rejection mode. To ease the integration of the EBD and LNA, inter-stage power matching is employed, instead of noise matching [21], which could improve the RX-path cascaded NF. When compared to the stand-alone LNA measurement, the measured NF increases by ∼4 and ∼5 dB for the default and high-rejection modes, respectively. For the blocker-NF measurement, a dielectric filter is used to suppress the noise power at 865 MHz of the signal generator which provides the blocker. The NF increase due to blocker is mainly due to the reciprocal mixing between blocker and LO phase noise [38] and blocker-caused compression. In Fig. 18(b), the measured blocker NF is 12.3 dB (default mode) and 15 dB (high-rejection mode) at a +7 dBm CW blocker at 40-MHz offset (from an 865-MHz f_{LO}). This is compliant with the 3GPP limit of 15 dB, while the specified maximum blocker power is only −15 dBm for LTE. However, in order not to impact the noise floor at the LNA's output, the LO phase noise should be improved to −170 dBc/Hz, given a ∼+5-dBm TX power appearing at the LNA input. The LO leakage is measured at the antenna port of the RF-FE for FDD and IBFD operations and shown in Fig. 19(a), ranging from −41.8 to −37.2 dBm, where the increase compared to LNA-only case [26] is estimated to be caused by the hybrid transformer and on-chip MN's impedance translational effect. The LO power leakage can be reduced in differential architecture [27]. In addition, the center-frequency shifting due to input capacitance of N-path network [39], [40] is measured versus LO frequency for FDD and IBFD operations, which is shown in Fig. 19(b), ranging from 0.24 to 0.62 MHz, which is better than the LNA-only case at <850 MHz since L_M of the MN (Fig. 10) resonates with the input parasitic capacitance of the LNA. The passband center-frequency shifting can be addressed by post-emphasis digital equalization [41].

Table I presents the performance summary of our RF-FE and compares it with the state-of-the-art works with the RX [3], [8], [12] and the LNA [21], [24]. This paper features a highly integrated RF-FE for FDD and IBFD operations, meanwhile achieving comparable performances when benchmarked with the state-of-the-art works. When compared to [24], even if the RX-path cascaded NF is worse, it saves 4.4× of area by omitting the SAW filters. On the other hand, compared to [3], [8], [12], and [21], this paper achieves better large-signal performance and higher TX–RX isolation.

Future work must address the limited EBD cancellation BW and reduction of the RX-path cascaded NF, which is 3GPP compliant but not very competitive, and handle the standard-FDD TX power level (+24 dBm). To cover wide-BW LTE channels, a more complex Z_{BAL} for EBD [25] could help to track impedance variations of the antenna across frequency to increase the cancellation BW, and the N-path LNA plus

TABLE I
COMPARISON WITH THE STATE OF THE ART

		This Work		TMTT'17 [24]	ISSCC'16 [8]	TMTT'16 [21]	JSSC'17 [3]	JSSC'15 [12]
FDD & IBFD	Architecture	Single-ended EBD + GB switched-*LC* N-path LNA		Single-ended EBD + tunable SAW-filter + LNA	Circulator-FE + RX chain with BB TX-cancel	Single-ended EBD + LNA	Distributed TX + mixer-first RX	Mixer-first RX + VM downmixer
	FDD/IBFD capable	FDD & IBFD		FDD & IBFD	IBFD (& TDD)	FDD & IBFD	FDD & IBFD	FDD & IBFD
	RF range (GHz)	0.7 to 1.0		0.7 to 1.0	0.6 to 0.8	1.6 to 2.2	0.3 to 1.5	01.5 to 3.5
	Area (mm^2)	14.4 (9.62 active)		64 (6.62 EBD+LNA)	1.4	0.35	7.2*	2
	Technology (CMOS)	0.18µm SOI		0.18µm SOI & SAW	65nm	0.18µm	65nm	65nm
		Default	High-rejection					
	Power (mW)	62.5	57.3	12	159	10.5	300[E]	23 to 56
	Supported Z_{ANT} (VSWR)	<2.3:1[E]	<2.3:1[E]	<2.3:1	N/R	<1.3:1	3:1	N/A
	RX gain (dB)	4.8 to 5.5	1.1 to 1.8	7.5 to 8.8	42 incl. BB	5 (sim.)	24 to 32 incl. BB	24 incl. BB
	In-band RX-path IIP_3 (dBm)	+6.4	+7.6	-3	-33 @ 42dB gain	+6.2	N/R	+9/+19
	OOB RX-path IIP_3 (dBm)	+26.7	+35.1	+42	+19	+5.9	N/R	+22
	OOB-iB_{1dB} (dBm)	+9 to +10.8	+11.2 to +12	+4 to +11	N/R	N/R	-2.2	N/R
	RX cascaded NF (dB)	8.7 to 9.2	10.6 to 11.7	7.6 to 8.9	11.5 (IBFD)	6.3 to 6.8	7	10.3 to 12.3
	Blocker (dBm) @ 15-dB NF	+8.2	+7	N/R	N/R	N/R	N/R	N/R
FDD	TX-RX isolation (dB)	>44(f_{TX}) & >40(f_{RX})	>55(f_{TX}) & >50(f_{RX})	50	20 (40 incl. BB)	>50	>23	>27
	Isolation BW (MHz)	30(f_{TX}) & 3.2(f_{RX})	10.4(f_{TX}) & 1.5(f_{RX})	>2	10[E] (13.5[E] incl. BB)	100[E]	N/R	16.25
	TX insertion loss (dB)	2.9 to 3.5	2.9 to 3.6	2.6 to 3.4	1.7	2.8 to 3.4	0	N/A
	FDS-IM_3 (dBm) @ P_{TX} (dBm)	-70 @ +20	-102 @ +20	-76 @ 20	N/R	N/R	N/R	N/A
	OOB-iTX_{1dB} (dBm)	+19	+23.1	+25 (+27.5: +10mA)	-4	N/R	+13	N/A
IBFD	TX-RX isolation (dB)	>40	>50	50	20 (40 incl. BB)	>50	>23	>27
	Isolation BW (MHz)	3.2	1.5	>2	10[E] (13.5[E] incl. BB)	100[E]	N/R	16.25
	TX insertion loss (dB)	3.7 to 3.9	3.7 to 3.9	2.6 to 3.4	1.7	2.8 to 3.4	0	N/A
	Max. P_{TX} @ ANT (dBm)	+29.2	+29.2	+27	-5.7[E]	+19.2	+19	N/A
	iTX_{1dB} (dBm)	+32.5	+32.5	30.4	-4[E]	+22.6	+19	N/A
	IM_3 [RX_{OUT}] (dBm) @ P_{TX} (dBm)	-96.2[E] @ +10	-121.7[E] @ +10	N/R	-87[E] @ -20	N/R	N/R	-68[E] @ -16.4

N/R: Not Reported, N/A: Not Applicable, [E]: Estimated, *: Incl. PA.

filtering-by-aliasing techniques [42] should be further developed to provide both wide in-band BW and sharp rejection at near-by TX leakage. These techniques will incur chip area and power consumption penalties, whereas this paper intended to focus on the conceptual demonstration of the EBD plus N-path LNA operation. In the LNA, the reduction of frequency-translational harmonic response and LO leakage must be analyzed and considered. The harmonic-folding response seriously desensitizes the LNA: when harmonic blockers are present, the N-path structure converts them down to f_{LO} at the output. The most severe harmonic-folding term happens on $3 \times f_{\mathrm{LO}}$, which is only rejected $\sim$23 dB for blockers near $3 \times f_{\mathrm{LO}}$. To address this, a bandpass filter can be added at the input of the LNA to help improve harmonic-folding issue [43], while sacrificing the gain and NF. Another feasible method is to use the eight-path network, since the nearest folding term happens from $7 \times f_{\mathrm{LO}}$. However, this comes at the cost of harmonic selectivity and power consumption since more switches must be driven by the LOGEN [27]. The harmonic-folding effect of the LNA is also affected by the antenna-impedance variation, since the OOB impedance of duplexer is not constant. Thus, the overall response of RF-FE is not a simple cascaded response and its dependence needs further study.

VII. CONCLUSION

This paper proposes a tunable RF-FE for both IBFD and FDD-LTE, for all 3GPP bands in the 0.7 to 1 GHz range, in the 0.18-μm SOI CMOS technology. It achieves high signal-handling capability and high TX-to-LNA isolation at both f_{TX} and f_{RX}.

The LNA [26] features a switched-*LC* N-path feedforward network with gain boosting, and optimum biasing to handle the high-power TX leakage at a small frequency offset, and achieves high linearity (+26.2 dBm OOB-IIP_3 and +8-dBm OOB-iB_{1dB} in the stand-alone LNA measurement). Power reduction techniques in the LOGEN and transconductor lower the power consumption, especially given the 0.18-μm technology node (48.4 to 62.5 mW). Finally, it achieves state-of-the-art blocker NF at high blocker levels.

The tunable RF-FE combining the EBD and LNA achieves dual-frequency isolation. For the first time, such a system including the LNA achieves <-100 dBm of IM_3 at +20 dBm of TX power for the FDS jammer test in FDD operation. Similarly, a TX-path IIP3 of +70 dBm is demonstrated (at this level of integration) for the first time. Finally, the RF-FE can handle up to +32.5-dBm IB TX power for IBFD operation, paving the way to FDD-comparable link budgets—an order of magnitude beyond the state of the art, all while also being backward compatible with FDD, although the limited TX–RX isolation BW and reduction of cascaded NF in RX path should be further developed to fit practical RF-FEs.

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