A Successive Approximation Recursive Digital Low-Dropout Voltage Regulator With PD Compensation and Sub-LSB Duty Control

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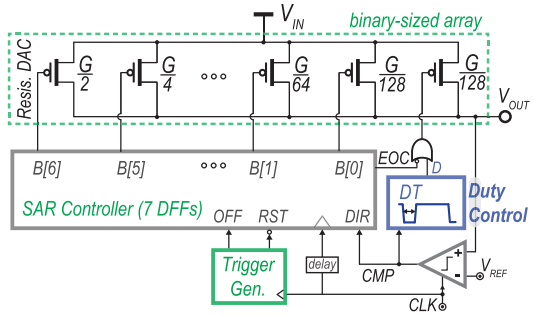
***Abstract*— This paper presents a recursive digital low-dropout (RLDO) regulator that improves response time, quiescent power, and load regulation dynamic range over prior digital LDO designs by 1-2 orders of magnitude. The proposed RLDO enables a practical digital replacement to analog LDOs by using an SAR-like binary search algorithm in a coarse loop and a sub-LSB pulse width modulation duty control scheme in a fine loop. A proportional-derivative compensation scheme is employed to ensure stable operation independent of load current, the size of the output decoupling capacitor, and clock frequency. Implemented in 0.0023 mm^2 in 65 nm CMOS, the 7-bit RLDO achieves, at a 0.5-V input, a response time of 15.1 ns with a figure of merit of 199.4 ps, along with stable operation across a 20 000× dynamic load range.**

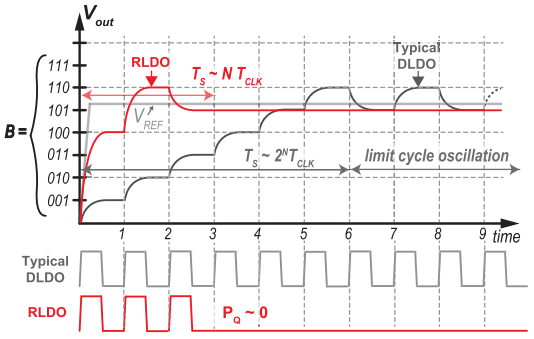
***Index Terms*— Binary search, digital low-dropout (DLDO), LDO, linear regulator, power management, proportional derivative (PD), successive approximation (SAR), voltage regulator.**

I. Introduction

MODERN sub- or near-threshold SoC designs feature multiple power domains to dynamically track the maximum energy efficiency point (62 mV to 0.45 V [1]–[8]) in response to application demands. Analog low-dropout (LDO) regulators [9]–[16] can generate such voltages in a small area with rapid response times (e.g. TR = 0.65 ns [16]). However, the input voltage, V_{in}, is typically brought on-chip via either a high-efficiency switching dc–dc converter or an external harvesting source, both with low-voltage sub- or near-threshold outputs (e.g., 0.5 V), where analog LDOs have difficulty in operating due to low-voltage headroom. On the other hand, digital LDOs (DLDOs) [17]–[26], which replace a single saturated pMOS power transistor with an array of pMOS power transistors operating in the linear region, can operate down to 0.5 V since less headroom is required. Most switch-array-based DLDOs rely on an integral controller to linearly search (via a 1-bit ADC) for the pMOS array conductance that realizes the nearest output voltage, V_{out}, to the desired target, V_{ref}. For N-bit control, linear search can take up to 2^N cycles. To expedite conversion, prior work has suggested adding a proportional term via a multi-bit ADC [22], [23]. However, the achievable response times are 44–4000 ns [22], [23], which is not sufficient for many digital loads.



(a)



(b)

Fig. 1. (a) Block-level diagram of the proposed RLDO. (b) Illustrative V_{out} response to a 0-to-V_{ref} step when the rate of change of V_{out} is much faster than the clock frequency, f_{CLK}, to explicitly show the binary search process.

Intuitively, binary search, illustrated in Fig. 1(a), can find the required array conductance in *exponentially* shorter time, i.e., *O(N)* cycles, and therefore, can enable exponentially faster response, T_R, and settling, T_S, times [Fig. 1(b)] than linear search. Unfortunately, a DLDO employing a binary search algorithm suffers from large staircase overshoots/undershoots during the N-step binary search, along with large steady-state error, as will be discussed in Sections III and V. These challenges rendered binary search control impractical as a main regulation scheme ever since the first introduction of switch-array DLDOs in [17] and [18].

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To enable a pragmatic binary search-based DLDO [27], the large staircase overshoots/undershoots during binary search steps are avoided by operating from a clock whose frequency is faster than the time constant of the load. Since doing so nominally renders a DLDO fully unstable due to the erroneous successive decisions, stability is obtained in the proposed design via a variable-coefficient PD compensation scheme described in Section III. To eliminate steady-state errors, a hysteretic pulse width modulation (PWM) control scheme is proposed in Section IV that also enables sub-LSB load current regulation. Additionally, loop-interruption logic is implemented in Section V to avoid large overshoot/undershoot that can result when a sudden I_L or ΔV_{in} step change occurs in the middle of the binary search [after deciding the first few most significant bits (MSBs)].

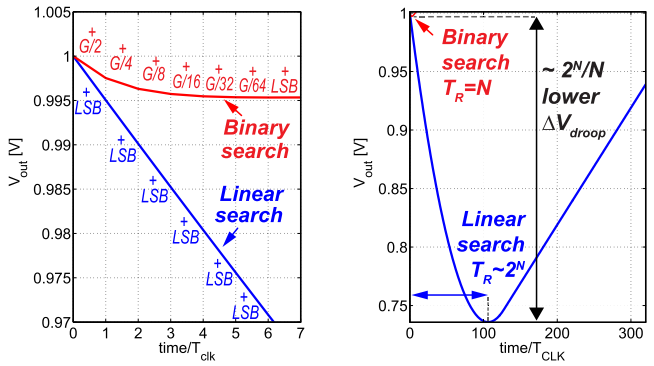


Fig. 2. Transient V_{out} response of a 7-bit linear search and binary search DLDOs to 0-to-$I_{L,\text{max}}$ load step. (a) Close-in. (b) Far-out. Both LDOs have the same total array conductance, G, where $G\,\Delta V_{\text{dropout}}$ matches $I_{L,\text{max}}$.

II. Successive Approximation Digital LDO Topology and Operation

A. SAR LDO Architecture

A conceptual 7-bit binary search DLDO is illustrated in Fig. 1(a). The array of 2^N equal-size pMOS fingers in barrel-based linear-search DLDOs [18], [28] is replaced with N binary-weighted pMOS switches (pMOS DAC), with a total conductance G, controlled via an SAR register. An additional switch of weight equal to the LSB is included for duty control (described later in Section IV).

1) V_{ref}-Step Transient Response: Fig. 1(b) shows the transient V_{out} response of representative 3-bit linear search and binary search DLDOs to a 0-to-V_{ref} input reference step (only 3 bits are shown for illustrative simplicity). For illustration purposes only, f_{CLK} is set to be slower than the rate of change of V_{out} in this example to allow enough time for V_{out} to settle before taking each bit-decision. Here, the pMOS array is initially turned off. At the first positive edge after V_{ref} step-increase, the comparator output goes to high, and hence under binary search the MSB switch is turned on. As a result, V_{out} starts to increase from zero initial voltage until it settles at the corresponding $G/2$ voltage level. At the following positive clock, V_{out} is still less than V_{ref}, therefore, the next MSB switch in the array is turned on which increases V_{out} to the $(3/4)G$ voltage level. At the third clock cycle, V_{out} is larger than V_{ref}, and therefore, the SAR register turns off the second bit, $B(1)$, while simultaneously turning on the LSB.

As illustrated in Fig. 1(b), a binary search DLDO achieves $2^N/N$ faster settling time than baseline linear-search DLDOs. Furthermore, the SAR controller requires only N DFFs instead of 2^N DFFs for a barrel shifter, reducing control area by $2^N/N$. Along with a $2^N/N$ reduction in the number of cycles to reach V_{ref}, clock power is thus reduced by $N^2/2^{2N}$. Importantly, a binary search DLDO does not suffer from limit-cycle oscillations as in baseline linear-search DLDOs, enabling $1/2^N$ lower quiescent current, I_Q, and hence higher current efficiency, where the entire SAR controller is clock-gated and only a single DFF is clocked during duty control, as discussed later in Section IV. Prior schemes [24], [26] have been proposed to reduce I_Q of linear search, however, they come at a reduced dc accuracy, as will be discussed shortly. On the other hand, to reduce area and quiescent power in a linear-search DLDO, it is in principal possible to replace the 2^N barrel shifter by an N-bit up/down counter driving binary-sized pMOS fingers. While this modified architecture reduces the number of required DFFs, and hence quiescent power (by $2^N/N$), it results in significant periodic noise in the on-chip supply lines due to limit-cycle oscillation of the binary weighted, as opposed to unary-sized, pMOS fingers.

2) $I_{L,max}$-Step Transient Response: Fig. 2(a) illustrates the transient V_{out} response of representative 7-bit linear search and binary search DLDOs to a full-range 0-to-$I_{L,\text{max}}$ load step. Compared to a baseline linear search DLDO which turns on only a single finger (with an LSB conductance of $G/2^7$) after the load step, the SAR architecture turns on half of the total array conductance, $G/2$, after the first clock cycle. In the second clock cycle, the recursive digital low-dropout (RLDO) turns on an additional quarter of the array conductance, $G/4$, and so on in a binary-subsiding manner. The proposed SAR architecture therefore requires only N clock cycles to respond to a full load step compared to 2^N in a baseline linear-search DLDO, enabling a much smaller response time and ΔV_{droop}. However, in reality, the output voltage droop, ΔV_{droop}, increases the finger current to $G/2^N(\Delta V_{\text{dropout}} + \Delta V_{\text{droop}})$ due to linear-mode operation of the pMOS transistors, and hence, the DLDO response time is a fraction, $\alpha < 1$, of the simplified current-source case: $T_{R,\text{DLDO}} = \alpha_1 2^N T_{\text{clk}}$; $T_{R,\text{RLDO}} = \alpha_2\ N T_{\text{clk}}$, as shown in Fig. 2(b).

B. Performance Comparison: Speed-Power Tradeoff Improvement via SAR Control

One of the main design objectives of a DLDO is to minimize the output voltage droop to a sudden load step. Nominally, consuming K× higher I_Q (e.g., via a higher f_{CLK} in a DLDO) enables K× faster T_R, and hence the speed-power product is fixed for a given architecture. Therefore, the product of T_R and normalized quiescent current is employed as a figure of merit (FOM) [29] for a normalized comparison among various LDOs

$$\text{FOM} = T_R \hat{I_Q} = \frac{C_{\text{out}}\,\Delta V_{\text{droop}}}{I_{L,\text{max}} - I_{L,\text{min}}} \frac{I_Q}{I_{L,\text{max}} - I_{L,\text{min}}} \tag{1}$$

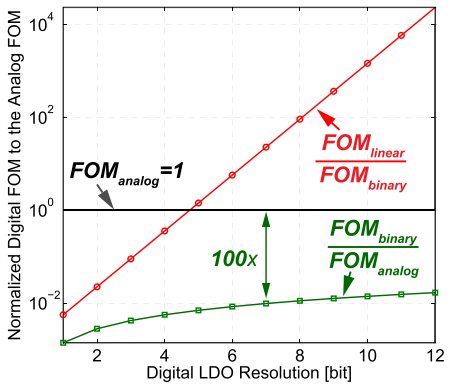


Fig. 3. FOM of a linear-search DLDO and a binary search RLDO normalized to the analog LDO FOM for the same process technology, $I_Q/\Delta I_L$, and C_{out} versus the required resolution N.

where the load step test is performed between $I_{L,\min}$ and $I_{L,\max}$ with a load rise/fall time less than $T_R/10$[1] and I_Q is the quiescent current incurred during the periodic load swing test and not the best case I_Q. A binary search DLDO inherently achieves a $2^{2N}/N$ smaller (i.e., better) FOM than a baseline linear-search DLDO due to the $2^N/N$ faster response time and the reduced quiescent power afforded by the $1/2^N$ lower number of switching DFFs at steady-state. Fig. 3 illustrates the FOMs for an analog LDO, and linear and binary search DLDOs.

III. Variable-Coefficients Proportional-Derivative Compensation

In order to filter out the unacceptably large staircase overshoots and undershoots of the SAR conversion steps in Fig. 1(b), it is necessary to take the SAR decisions at a faster rate than the rate of change of V_{out}. However, this can lead to erroneous successive decisions during the SAR conversion and hence an unstable response. This is why prior art binary search architectures were not practically feasible [30], [31]; instead, prior art SAR switching was utilized only as a mid sub-array helper DLDO [32]. In order to enable a pragmatic SAR-based LDO, a PD compensation scheme is proposed to establish a multi-rate *fast-slow* control loop that observes (samples) V_{out} at a fast clock speed, f_{CLK}, to eliminate the SAR conversion overshoots and undershoots, while allowing the integrator to accumulate at a rate close to the output pole frequency, $f_c \sim f_L$ to avoid instability.

A. Stability Analysis of DLDOs Using a Bode Diagram Approach

Fig. 4(a) illustrates a piecewise linear small-signal ac model of a binary search DLDO without PD compensation in the Z-domain. The initial load conductance, $G_L = 1/R_L$ and the initial (i.e., prior to the ith iteration) pMOS array conductance, $G_p(i-1)$, in Fig. 4(a) establish the dc operating point around which the ac response to the input small-signal disturbance, ΔV_{ref}, is evaluated.

The comparator samples quantizes the input error signal $e(t) = V_{\text{ref}} - V_{\text{out}}(t)$. In the beginning of the conversion, the SAR controller has the highest gain (via switching the MSB conductance) to facilitate a rapid response time via a large loop bandwidth. As the SAR algorithm converges, the step size at the ith iteration decreases (i.e., $M(i) \times \text{LSB} = G/2^i$), and thus the gain, $K(i)$, decreases in a binary-subsiding manner, until the gain reaches the LSB value. For the purpose of stability analysis, the SAR register is assumed to accumulate the instantaneous error, $M(i)e[k]$ rather than $M(i)e[i]$, to determine the number of turned on pMOS fingers, $B[k]$.

The zero-order-hold equivalent of the output RC network, comprising $G_p(i-1)$, R_L, and C_{out}, can be found as $(1-z_L)/(z-z_L)$, where $z_L = e^{-f_L/f_{\text{CLK}}}$ is the output pole, which is determined by the ratio between the equivalent output-load frequency, $f_L = (G_L + G_p(i-1))/C_{\text{out}}$, and the DLDO sampling clock, f_{CLK}. Therefore, the open-loop transfer function of such a second-order feedback control loop is given by

$$G(z) = \frac{K(i)(1-z_L)z}{(z-1)(z-z_L)} \tag{2}$$

and hence $G(z)$ has two poles: the loop integrator pole on the unity circle ($z = 1$) and the output pole, z_L.

It can be shown that the open-loop gain $G(s)$ of the corresponding continuous-time system using *impulse-invariance* transformation [33] of the digital LDO in (2) is given by

$$G(s) = \frac{\omega_n^2}{s(s+2\eta\omega_n)}. \tag{3}$$

Therefore, the open-loop gain $G(s)$ contains two poles, where the Z-domain poles, $z = 1$ and z_L, map to, the $s = 0$ and f_L, in the S-domain. Fig. 4(b) illustrates the Bode diagram of a DLDO, where the integrator pole ($s = 0$) asymptote intersects the 0-dB axis at $f_I = \omega_n/(2\eta)$. It can be shown that $f_I = \beta f_{\text{CLK}} \ln(M(i) \times \text{LSB} + 1)$, where β is a proportionality factor less than unity. Therefore, for a given output-load frequency, f_L, increasing the sampling frequency, f_{CLK}, or the array conductance step, M, both serve to increase f_I, which shifts the magnitude plot upward, as shown in Fig. 4(b). This boosts the unity-gain frequency or loop bandwidth, $\omega_{\text{GC}} = (f_L f_I)^{1/2}$, and hence enables a faster response time, however, at a reduced phase margin (PM) and stability as set by: $\text{PM} = 90^\circ - \tan^{-1}(f_I/f_L)^{1/2}$. This speed-stability tradeoff sets the allowable values for the design variables f_{CLK} and M, and hence the upper bound on the achievable response time for a given design. The speed-stability tradeoff becomes tighter with reduced current values: at a fixed f_{CLK} and M, f_L becomes more dominant with smaller loads, which increases the relative separation between the two poles (f_L and f_I) and hence reduces the PM and eventually results in an oscillatory response at light loads, as in Fig. 5(a).

In theory, loop stability can be ensured by guaranteeing enough PM at each conversion step, i, in the piecewise linear model. To maintain a fixed integrator asymptote crossing (f_I)

[1]Otherwise, when the rise/fall time of the load-current swing is comparable to T_R, the measured T_R becomes the unit-*ramp* response time and not the unit-*step* response time. This invalidates the measured FOM since the output voltage droop, ΔV_{droop}, due to a unit-*ramp* current is much smaller than the droop in the unit-step current case.

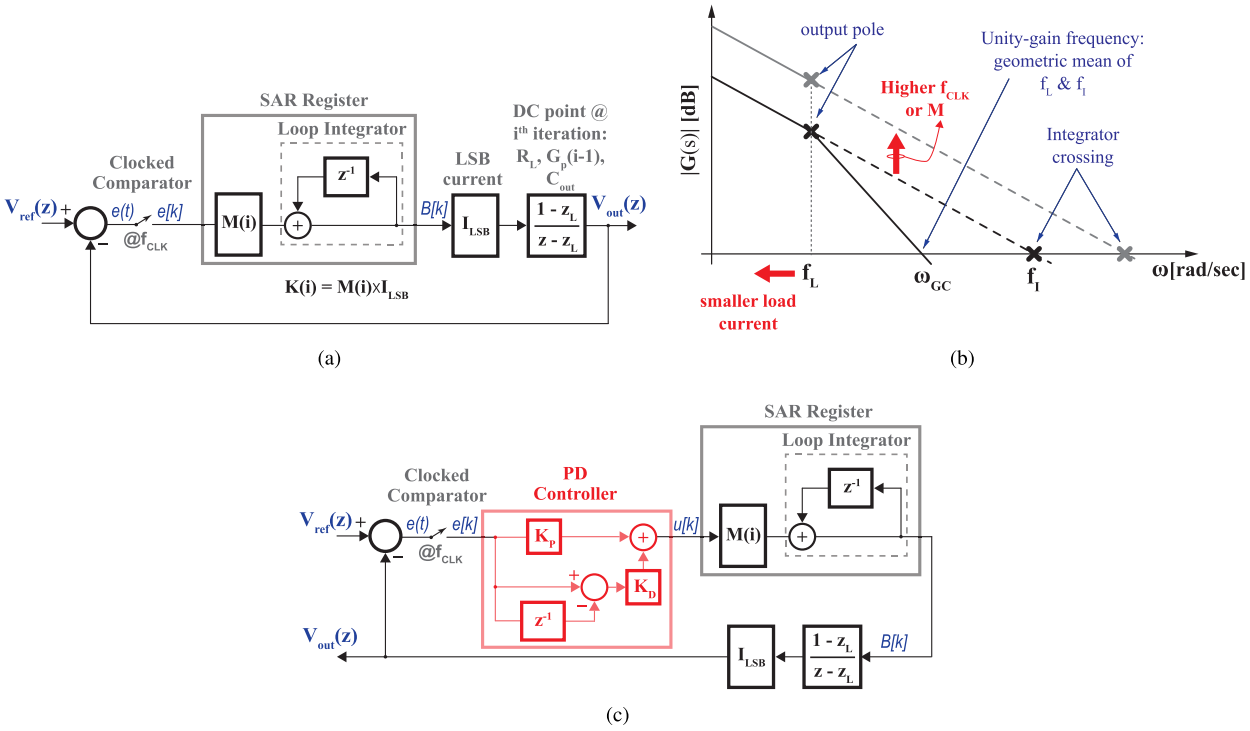


Fig. 4. RLDO model. (a) Small-signal ac model. (b) Bode diagram. (c) RLDO with PD controller. The SAR controller acts as a variable-gain discrete-time integrator.

and ensure stable operation, f_{CLK} should be linearly reduced, from the LSB stable clock rate, $f_{\text{CLK,LSB}}/(N-i+1)$, every iteration i. Unfortunately, in order to avoid significant overshoots and undershoots during the initial SAR conversion steps, f_{CLK} should be scaled *exponentially* the other way around in a binary increasing manner, i.e., $2^i f_{\text{CLK,LSB}}$, such that $f_{\text{CLK,MSB}}$ at the first iteration is faster than the MSB slew rate, $\text{MSB}\times\Delta V_{\text{dropout}}/C_{\text{out}} \times 1/\Delta V_{\text{ov}}$, where ΔV_{ov} is the allowed overshoot magnitude, or $1/(2T_R)$, for $\Delta V_{\text{ov}} = \Delta V_{\text{droop}}$. Therefore, a DLDO incorporating binary search is inherently unstable, or otherwise, provides an output with unacceptably large overshoots and undershoots.

B. Adaptive Zero Insertion Through Variable-Coefficients PD Compensation

In order to enable a pragmatic SAR-based LDO, a zero is added at f_L to the open-loop transfer function in (3) through an adaptive *PD* compensation scheme, converting the LDO into a first order system.

1) Proportional Derivative Control Law and Action: Intuitively, the barrel shifter in a linear search DLDO should ideally be locked once the output voltage reverses the direction of its slope and starts to increase toward V_{ref} (e.g., after turning on three fingers in Fig. 6) to avoid overshoot. In other words, the loop integrator should be incremented (+1 state) only when V_{out} has a negative slope (*derivative term*) while V_{out} is less than V_{ref} (*proportional term*). Similarly, the loop integrator should be decremented (−1 state) only when V_{out} is trending upward, i.e., with a positive slope, while V_{out} is larger than V_{ref}. Otherwise, the loop integrator value should be kept fixed (0 state). This behavior can be described by the control law of the proposed PD compensator as

$$\begin{aligned}&\text{if } (V_{\text{out}}[k] < V_{\text{ref}}) \,\&\, (dV_{\text{out}}/dt < 0) \text{ increment}\\ &\text{elseif } (V_{\text{out}}[k] > V_{\text{ref}}) \,\&\, (dV_{\text{out}}/dt > 0) \text{ decrement.}\end{aligned} \quad (4)$$

TABLE I
PD CONTROL ACTION

P term	D term	PD output
$\frac{1}{2}(V_{ref} - V_{out}[k])^*$	$\frac{1}{2}(V_{out}[k-1] - V_{out}[k])^*$	$u[k]$
+1/2	+1/2	+1
+1/2	-1/2	0
-1/2	+1/2	0
-1/2	-1/2	-1

The illustrated proportional term logic in (4) can be implemented through the quantized error voltage, $e[k] = (V_{\text{ref}} - V_{\text{out}}[k])$, which is +1 when $V_{\text{ref}} > V_{\text{out}}$, and −1 when $V_{\text{out}} > V_{\text{ref}}$. The derivative term logic in (4) can be evaluated through the difference $(e[k]-e[k-1])$ which is equivalent to $\Delta V_{\text{out}}[k] = (V_{\text{out}}[k-1] - V_{\text{out}}[k])$. Therefore, the PD control law in (4) can be implemented through the addition of the aforementioned two terms as $u[k] = K_P e[k] + K_D \Delta V_{\text{out}}[k]$, where $u[k]$ is the PD output that is provided to the loop integrator (i.e., barrel shifter or SAR register), K_P and K_D are the proportional and derivative coefficients, and $\Delta V_{\text{out}}[k]$ is the derivative term. Table I illustrates the PD output across the possible values of the proportional and derivative terms.

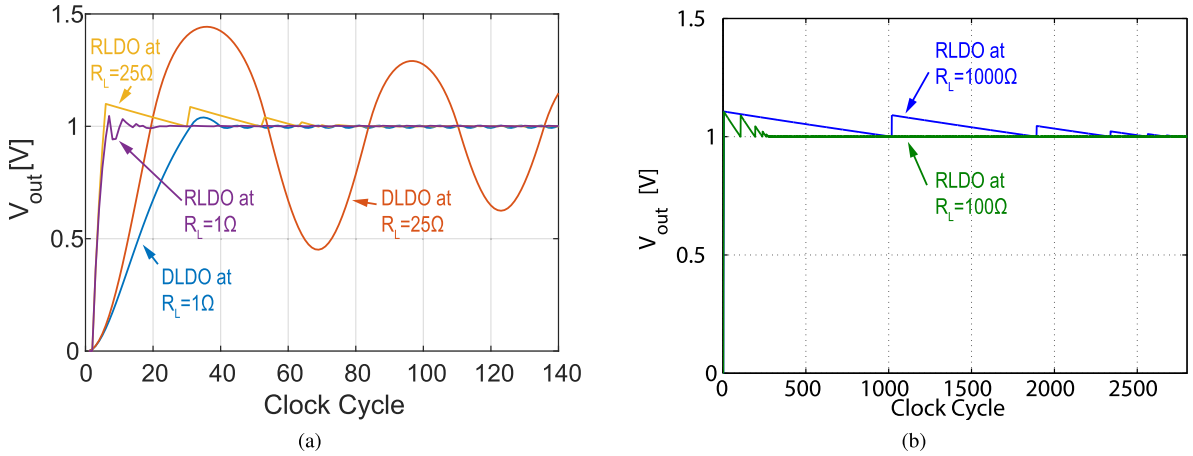


Fig. 5. (a) Transient V_{out} simulations of a 7-bit RLDO with the proposed PD compensation, and a 7-bit DLDO at peak current $R_L = 1\ \Omega$ and at light current $R_L = 25\ \Omega$ ($V_{\text{in}} = 2$ V, $V_{\text{ref}} = 1$ V, $G = 5\ \Omega^{-1}1$, $C_{\text{out}} = 1/(2\pi)$). (b) Simulations of the PD-compensated RLDO at $R_L = 100$ and $1000\ \Omega$. The RLDO V_{out} overshoot, due to MSB turn on, can be reduced with higher sampling frequency, f_{CLK}.

2) Stability Improvement With PD Compensation: To illustrate the effect of the proposed PD compensation on the LDO frequency response, PD compensation is incorporated in the small-signal model in Fig. 4(c). Using a backward-difference approximation to the differentiation operator, $de(t)/dt$, the discrete equivalent of a continuous-time PD compensator, $K_P e(t) + K_{D_C} de(t)/dt$, can be found as $K_P e[k] + K_{D_C}(e[k] - e[k-1])/T_{\text{CLK}}$. Therefore, the PD compensation inserts a zero at $-K_P/K_{D_C}$ (or $-K_P/K_D \times f_{\text{CLK}}$) to the corresponding continuous-time open-loop transfer function in (3). Unfortunately, conventional series PD compensators have fixed coefficients (K_P and K_D) at run time. Consequently, the added zero cancels the phase lag of the output pole $f_L = 2\eta\omega_n$ only when $-K_P/K_{D_C}$ is more dominant than f_L (high currents), limiting the achievable I_L dynamic range. On the other hand, in this paper, each P and D term is individually quantized before the addition, enabling adaptation of the inserted zero with the output pole while ensuring the P and D terms have equal weights in the final output.

To illustrate the difference in the control action between the proposed and the conventional PD compensator, consider the case when V_{out} is much less than V_{ref}, yet is slowly approaching V_{ref}. In this case, the conventional PD outputs $+1$, since the D term, $\Delta V_{\text{out}}[k]$, is negative with a magnitude much less than the positive P term, $(V_{\text{ref}} - V_{\text{out}}[k])$. On the other hand, the proposed PD output is zero, since the P and D terms are quantized individually before the addition, and hence the P term is $+1$ while the quantized D term is -1.

To account for the quantization effect, an input, $e[k]$, dependent quantization gain is added to the P and D coefficients such that $K_P = k_p \times k_{Qp}(e[k])$, where $|k_{Qp} \times e[k]|$ is 1, and similarly, $K_D = k_d \times k_{Qd}(e[k])$ where $|k_{Qd} \times \Delta e[k]|$ is 1. Therefore, k_{Qp} is simply $1/|v_{\text{out}}[k]|$, where V_{ref} is set to zero under small-signal operation. The D-term difference $e[k] - e[k-1]$ can be evaluated by $(V_{\text{out}}[k-1] - V_{\text{out}}[k])$ which is equivalent to $(G_p(i) + G_L)v_{\text{out}}[k]/C_{\text{out}} \times T_{\text{CLK}}$ or essentially $f_L/f_{\text{CLK}} \times v_{\text{out}}[k]$, for sufficiently small values of T_{CLK}. Therefore, the D-term quantization gain k_{Qd} becomes $f_{\text{CLK}}/(f_L v_{\text{out}}[k])$ so that $|k_{Qd} \times \Delta e[k]|$ is 1. Consequently, the resulting zero $-K_P/K_{D_C}$ in (3) becomes $-f_L$, which perfectly cancels the output pole and enables a single-pole system with PM of 90°, as shown in Fig. 4(b), irrespective of C_{out}, R_L, $M(i)$, and f_{CLK}. Fig. 5(b) verifies the proposed PD compensation efficacy in realizing stable operation irrespective of I_L. In summary, inclusion of the third idle state effectively implements cycle-skipping and adapts the rate at which the integrator updates its value, $f_c = f_{\text{CLK}}/m$ for integer m, with the output rate, f_L, to maintain the output pole, e^{-f_L/f_c}, inside the unity circle.

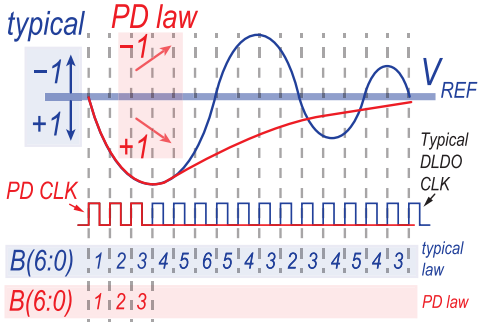


Fig. 6. DLDO transient V_{out} response with and without the proposed PD compensator.

IV. Sub-LSB Hysteretic PWM Control

A. Minimum Current Limit of Linear Search-Based DLDOs

1) DC Accuracy Limitation: In a linear search DLDO, limit cycling modulates the duty cycle of the n oscillating fingers at $f_{\text{CLK}}/(2n)$ to maintain the average V_{out} close to V_{ref}. Unfortunately, such duty-cycle modulation fails to provide the desired V_{out} level, as the current of cycling ON/OFF LSBs becomes comparable to I_L and hence gives a more pronounced

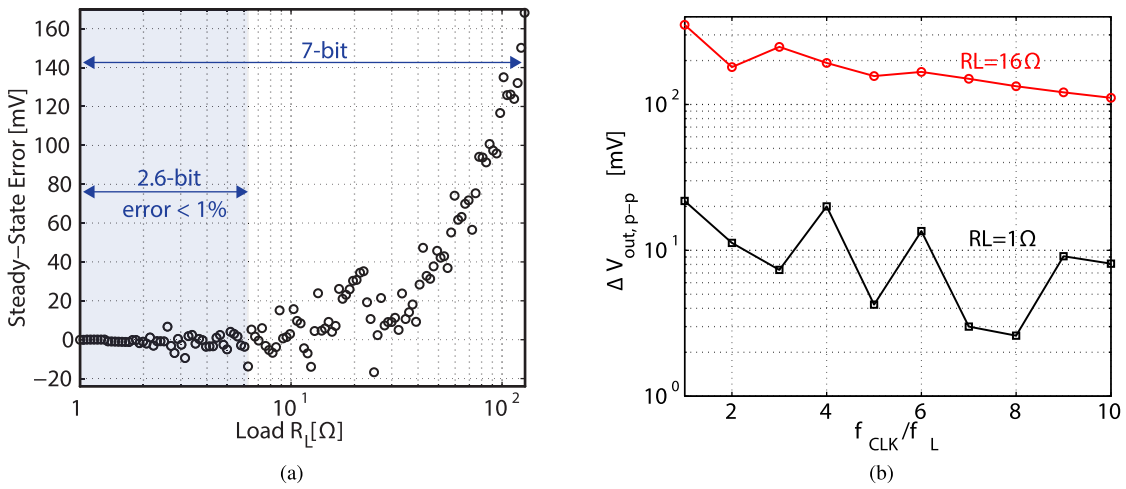


Fig. 7. Setting limits of digital LDOs minimum current. (a) Simulated steady-state error versus R_L at $f_{\rm CLK} = 10 \times f_L$. (b) Simulated steady-state $V_{\rm out}$ ripple $\Delta V_{\rm out,p\text{-}p}$ versus $f_{\rm CLK}/f_L$ of a 7-bit shifter-based DLDO with $V_{\rm ref} = V_{\rm in}/2$. The sudden jumps in the ripple voltage is due to the change in the mode of oscillation.

$V_{\rm out}$ steady-state error, especially at large dropout voltages. For instance, in a 7-bit barrel-based DLDO, the steady-state error exceeds $\pm 1\%$ $V_{\rm ref}$ when I_L is $2^{2.6}$ below $I_{L,\rm max}$ for $V_{\rm ref} = V_{\rm in}/2$ [Fig. 7(a)].

2) V_{out} Peak-to-Peak Ripple Limitation: Limit-cycle oscillations result in an output voltage ripple, $\Delta V_{\rm out,p\text{-}p}$, proportional to the number of limit-cycling fingers, n. As I_L is reduced, the output peak-to-peak ripple increases since the effect of the limit-cycling fingers on $V_{\rm out}$ is more pronounced at lighter loads, as illustrated in Fig. 7(b). $\Delta V_{\rm out,p\text{-}p}$ can be reduced by increasing the DLDO operating frequency, $f_{\rm CLK}$, and hence the DLDO output ripple frequency $f_{\rm CLK}/(2n)$, beyond the output RC network corner f_L, as in Fig. 7(b). Unfortunately, the higher $f_{\rm CLK}$ results in a lower damping factor η and eventually an oscillatory response, as discussed in section III-A. For a 7-bit DLDO, when $V_{\rm ref} = 0.9\ V_{\rm in}$, the load current range with a peak-to-peak ripple below 50 mV is limited to $2^{6.7}$.

Therefore, the LDO minimum I_L is typically limited by the acceptable steady-state error level, at large $\Delta V_{\rm dropout}$, and the allowable output voltage ripple, at small $\Delta V_{\rm dropout}$, of the limit-cycling LSB(s), and hence the resolution N, which determines both, defines the achievable dynamic range $I_{L,\rm max}/I_{L,\rm min}$. Unfortunately, increasing the resolution N comes with a worse transient FOM, as in Fig. 3.

B. Minimum Current Limit in a Binary Search DLDO

On the other hand, after the SAR conversion, $V_{\rm out}$ becomes within one $I_L \times$ LSB of the desired target, $V_{\rm ref}$. Since the RLDO does not exhibit limit-cycle oscillations, the pMOS array conductance G_p converges to $G_{\rm ref} \pm$ LSB at steady-state, where $G_{\rm ref}$ is the pMOS conductance that makes $V_{\rm out}$ matches $V_{\rm ref}$ and the final $V_{\rm out}$ value is $V_{\rm in} \times G_p/(G_p + G_L)$. As a result, the worst case error becomes $\sim \pm(({\rm LSB})/(G_L(1 + G_{\rm ref}/G_L))) \times V_{\rm in}$ or $\pm(({\rm LSB})/G_L)\Delta V_{\rm dropout}$. As the load current, G_L, is reduced or $\Delta V_{\rm dropout}$ is increased, the worst case steady-state error increases. Therefore, the load dynamic range

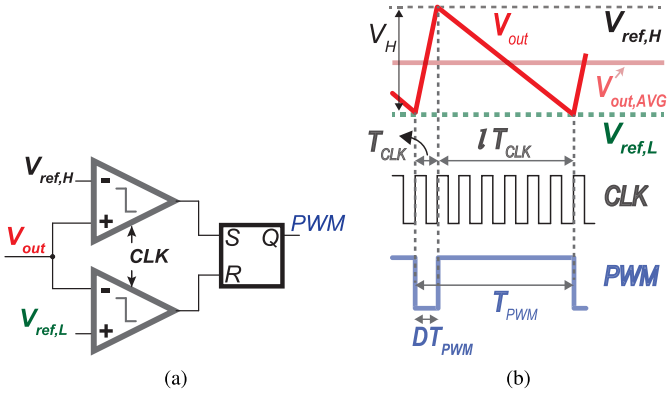


Fig. 8. Hysteretic dual-bound controller. (a) Top-level schematic. (b) Operation.

$I_{L,\rm max}/I_{L,\rm min}$ with certain error$-\%$ becomes limited to: error$-\% \times 2^N$, e.g., $(N - 6.6)$ bits range for a $\pm 1\%$ $V_{\rm ref}$ error. Therefore, the second challenge of the SAR LDO architecture, after its inherent instability (Section III), is the limited dc accuracy that made such SAR architecture previously impractical.

C. Hysteretic PWM Control

To mitigate the accuracy problem as well as enable sub-LSB I_L regulation, a redundant LSB switch is employed while the duty ratio, D, of its gate voltage is modulated like a lossy switched-mode buck converter. Instead of the periodic 10–70 mV ripple encountered during limit cycling in prior DLDOs [28], a dual-bound ($V_{{\rm ref},H}$, $V_{{\rm ref},L}$) hysteretic PWM controller is used to generate the redundant LSB drive signal. Once the SAR controller brings $V_{\rm out}$ to within the hysteretic window, the SAR controller is clock-gated and the PWM control is enabled. Here, the same SAR P-term comparators are reused, as will be discussed, to set or reset an SR latch that provides the gate voltage, *PWM*, of the redundant LSB, as in Fig. 8.

The average output value of a dual-bound hysteretic PWM control scheme is half of the hysteresis height, $V_H/2$,

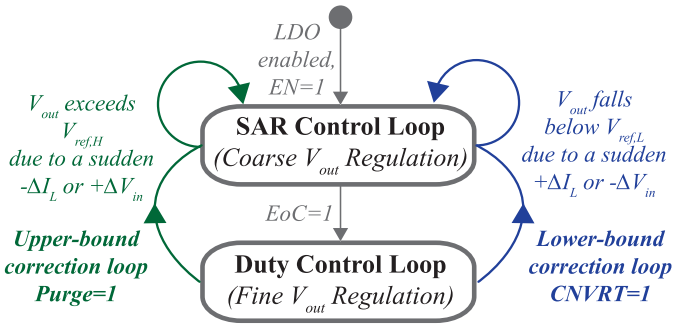


Fig. 9. Top-level state diagram of the proposed RLDO.

as in Fig. 8(b). Therefore, the steady-state error in a DLDO can be eliminated by setting the hysteresis bounds at $V_{\text{ref},H} = V_{\text{ref}} + V_H/2$ and $V_{\text{ref},L} = V_{\text{ref}} - V_H/2$, under a high sampling rate. Furthermore, at light loads, the minimum current supplied by the DLDO can go below the LSB finger current by $I_{\text{sub-LSB}} = (1/(l+1))I_{\text{LSB}}$ [Fig. 8(b)], with zero steady-state error and without the ripple exceeding V_H, unlike limit-cycle oscillation. Therefore, the achievable effective LSB, and thus the dynamic range, is extended by $\log_2(l+1)$ bits. The PWM controller also limits the cycling switches to only a single pMOS finger which reduces the steady-state quiescent power.

V. Circuit Implementation

The proposed RLDO incorporates the three techniques discussed above: SAR switching, adaptive PD compensation, and sub-LSB PWM control. As shown in Fig. 9, once the RLDO is enabled (EN = 1), the SAR control loop is initiated and the number of turned on pMOS fingers is adjusted to coarsely set V_{out} to V_{ref}. Once EoC is asserted, the duty-cycle controller is enabled to perform sub-LSB fine regulation. If, during duty control or SAR conversion steps, a sudden load-current ΔI_L or input-voltage ΔV_{in} step occurs that knocks V_{out} outside the control hysteresis, upper- and lower-bound correction logic restarts the SAR operation by asserting CNV.

A. Proportional-Derivative Compensator Implementation

The PD compensator output can take on one of three values, either $+1$, -1, or 0; thus, two variables, INC and DEC, are used to represent the PD output state. Table II illustrates the relationship of these variables, when K_P and K_D are set to 1/2. The INC and DEC signals are not static signals that take on a fixed value but rather act as pulsed signals, since they are used as clock inputs to the SAR logic in the RLDO.

A clocked sense amplifier can be considered as a differential *quantized* AND gate, as in Fig. 10(a). Thus, when the quantized difference $\Delta V^* = [V_+ - V_-]^*$ between the input analog signals is 1, the sampling clock propagates through the positive output O_p of the proposed gate and vice versa for the negative output O_n. Fig. 10(b) illustrates the quantized gate-level implementation of the truth table of the PD compensator, where $e_x^*[k]$ represents the quantized error $[V_{\text{ref},x} - V_{\text{out}}[k]]^*$. The PD essentially acts as an XNOR gate, where it gives a true (pulsing) output when the number of true inputs is even as shown in Table II.

TABLE II
Truth Table of PD Compensator

From Block Diagram	Logic Inputs		Logic Outputs	
u[k]	e^*	ΔV_{out}^*	*INC*	*DEC*
+1	1	1	CLK	0
0	1	0	0	0
0	0	1	0	0
-1	0	0	0	CLK

The schematic of the implemented PD compensator is shown in Fig. 11. The two *PWM* comparators, COMP_H and COMP_L, implement the proportional term and thus provide the quantized errors $[V_{\text{ref},H} - V_{\text{out}}[k]]^*$ and $[V_{\text{ref},L} - V_{\text{out}}[k]]^*$, respectively. They establish a hysteresis where all the RLDO circuitry is disabled for minimal I_Q and V_{out} comes to a halt. The comparators DIFF_H and DIFF_L implement the differential term $\Delta V_{\text{out}}^*[k]$.

The derivative term $(V_{\text{out}}[k-1] - V_{\text{out}}[k])$ of the PD compensator is implemented through the bottom-plate sampling circuit illustrated in Fig. 11 comprised of a footer nMOS switch and a 560-fF sampling capacitor. When the sampling clock *M2G* is high, the value of V_{out} is stored across the sampling capacitor. When *M2G* is low, the voltage of the negative comparator terminal becomes the difference term $(V_{\text{out}}[k] - V_{\text{out}}[k-1])$. The difference is then compared to a virtual ground through the comparators DIFF_H and DIFF_L to produce the quantized difference term $[V_{\text{out}}[k-1] - V_{\text{out}}[k]]^*$. A replica sample and hold circuit is employed to sample $V_{\text{ref},L}$ ($\approx V_{\text{out}}$) in order to establish a virtual ground at the positive terminal of the comparators, so that errors due to charge-injection, clock feed-through, or comparator kickback noise are canceled via the inherent symmetry. The sampling switches M1 and M2 in Fig. 11 are enabled from INC and DEC instead of CLKL and CLKH so that the difference ΔV_{out} accumulates and becomes $(V_{\text{out}}[k] - V_{\text{out}}[k-m])$. Therefore, if an erroneous DIFF_H or DIFF_L comparison results due to kT/C noise, the difference increases until it overpowers this error, as shown in Fig. 12.

When V_{out} is within hysteresis, OOH is reset low through the two SR latches in Fig. 11. Thus, the footer nMOS sampling switches are statically enabled through the OR gate that propagates the complement of OOH to the sampling switch gate in Fig. 11. Once V_{out} is outside hysteresis, the rising edge of the first clock pulse CLKL or CLKH might trigger the comparators DIFF_L and DIFF_H when the difference $(V_{\text{out}}[k] - V_{\text{out}}[k-1])$ is small, and hence, the comparison result becomes stochastic. As a result, a clock pulse might be lost, which would increase the RLDO response time. To prevent this, the *first edge pass* logic in Fig. 11 allows the first clock pulse CLKL (CLKH) to pass directly to INC (DEC) irrespective of the DIFF_L (DIFF_H) comparison result.

B. Regulation-Loop Interruption Logic

1) Lower-Bound Correction Loop: During duty control, the redundant LSB current can fail to bring the output voltage

Fig. 10. Quantized gate-level implementation. (a) Equivalence of a clocked comparator to a quantized AND gate. (b) Quantized gate-level implementation of the PD compensator truth table in Table II.

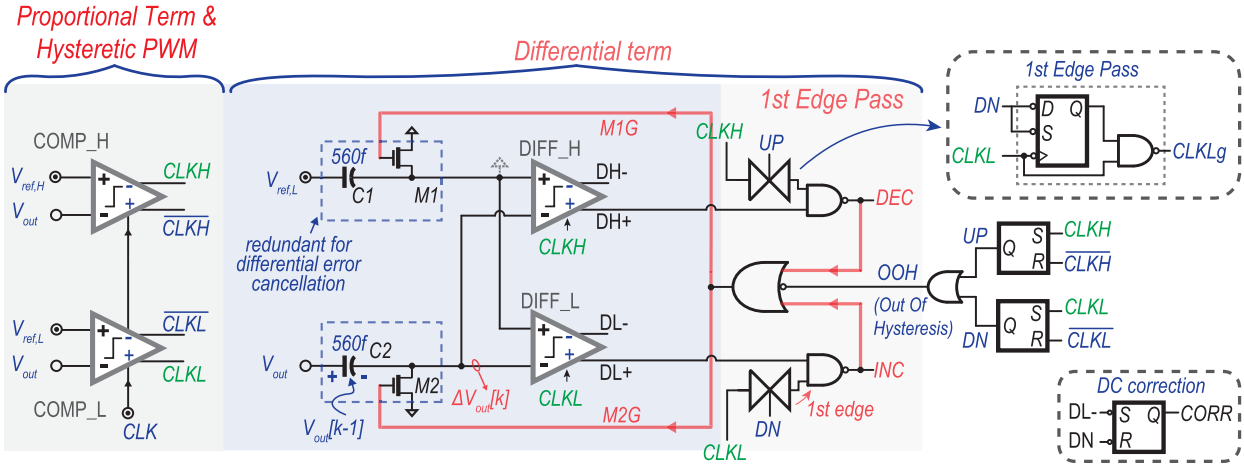


Fig. 11. Top-level schematic of the implemented PD compensator, including PWM comparators, derivative term comparators, and bottom-plate sampling circuitry. Insets illustrate the *first edge pass* and *dc correction* logic.

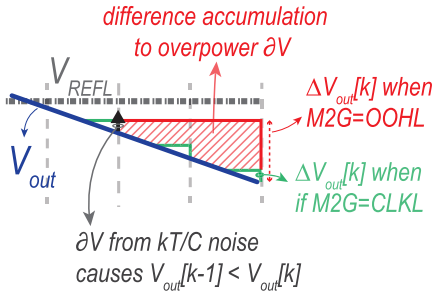


Fig. 12. Difference accumulation to overpower kT/C noise due to a small sampling capacitor size.

above $V_{\text{ref},L}$ if a large load-current increase $+\Delta I_L$ or a large input-voltage decrease $-\Delta V_{\text{in}}$ occurs. Therefore, lower-bound trigger logic is employed to restart the SAR search with the MSB, $B(6)$, on and the remaining pMOS transistors off, by asserting CNV_D, created by AND-ing the redundant LSB gate signal, PWM, and INC.[2] In the worst case, the lower-bound trigger logic takes two clock cycles to turn on the MSB switch, and hence the clock frequency is set by the required response time as: $f_{\text{CLK}} > 2/T_R$.

To avoid artificial undershoots that may be introduced if a large $+I_L$ or $-V_{\text{in}}$ step change occurs in the middle of the SAR conversion steps after deciding the first few MSBs, a branch-prediction scheme[3] is implemented. As in Fig. 13(a), when two consecutive INC edges result without any DEC assertion in-between during the SAR bit-cycling, the branch-prediction logic predicts that there is a disturbance, $+\Delta I_L$ or $-\Delta V_{\text{in}}$, that is large in amplitude, and therefore, the remaining unchecked l bits in the switch array may not be able to compensate for this disturbance. To verify this, the branch-prediction logic temporarily enables the remaining unchecked l bits in the SAR register by asserting *on*, as in Fig. 16(a) where $B(2:0)$ and PWM LSB $B(-1)$ are temporarily enabled. If V_{out} exceeds $V_{\text{ref},H}$ (i.e., DEC = 1), then the present disturbance, $+\Delta I_L$ or $-\Delta V_{\text{in}}$, can be successfully accounted for through the remaining l bits and the SAR operation can be continued as normal. This is similar to a *branch-not-taken* in pipeline hazards terminology. Otherwise, if V_{out} is still slewing downward below $V_{\text{ref},L}$ despite the l bits being turned on, then the SAR search should be restarted. This is equivalent to a *branch-taken* in pipeline design. Here, a third INC edge results although the l bits are turned on, and hence the branch-prediction logic restarts the SAR search operation at $B[k] = 7'b0111111$ [$B(6)$ is on] by asserting CNV_{SAR}, as in Fig. 16(a).

[2]INC pulse is produced by passing CLKL through *first edge pass* logic, during PWM control.

[3]The proposed scheme is similar to branch-prediction solutions that avoid CPU pipeline hazards in computer architecture.

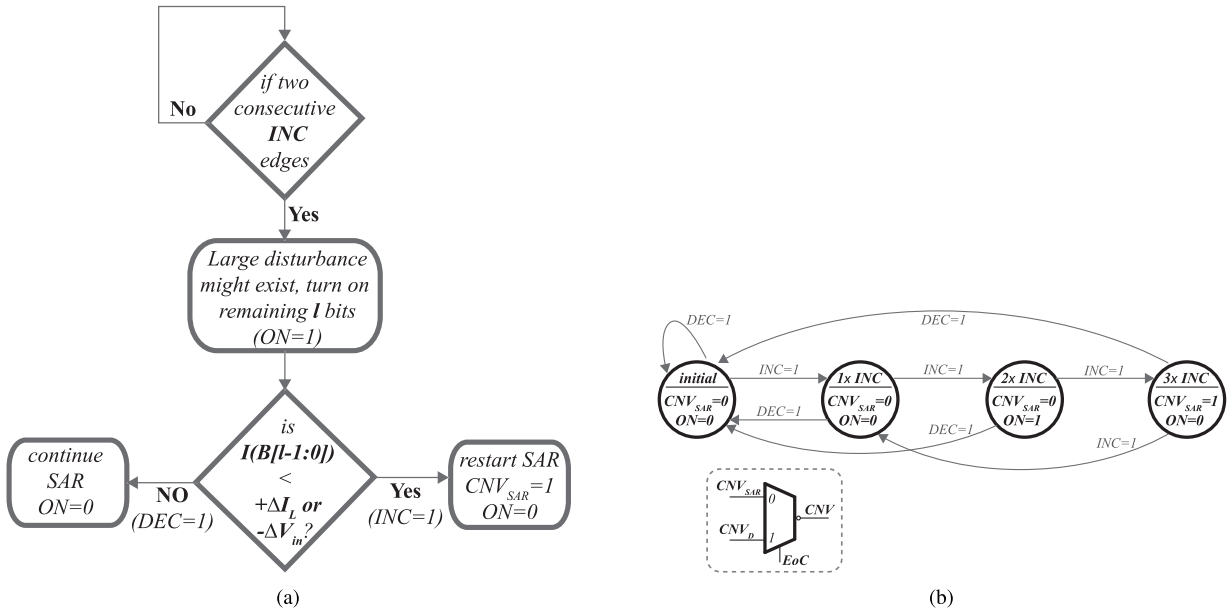


Fig. 13. Proposed branch-prediction (a) flowchart and (b) state-diagram implementation. Inset: the SAR reset CNV selection based on EoC through an output multiplexer.

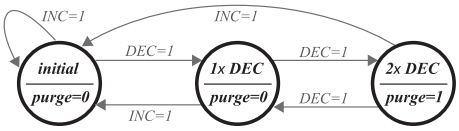


Fig. 14. State-diagram implementation of the upper bound.

```
// initially B=7'b1111111 and i=6
BinarySearch(B(6:0),i)

  turn on B(i); //perturb phase

  //observe phase
  if (posedge DEC)
       turn off B(i);

  if (posedge INC)
     keep B(i) on;
     if i=0
       return;
     else
       return BinarySearch(B,i-1);
```

Fig. 15. SAR backbone pseudocode.

Branch prediction is implemented using a 3-bit sequence detector, as in Fig. 13(b). The *Moore* state-machine asserts its outputs, ON $=$ 1 and $\mathrm{CNV_{SAR}} = 1$, when it recognizes two and three INC edges in succession, respectively. The state-machine resets to its initial state when a DEC edge results. As shown in the inset in Fig. 13(b), a 2-input multiplexer is used to select the complement of either CNV_D or $\mathrm{CNV_{SAR}}$ as the SAR controller restart signal, CNV, based on the present active control loop, as determined by EoC.

2) Upper-Bound Correction Loop: During duty control, a large disturbance can make the output voltage exceed $V_{\mathrm{ref},H}$, even though the redundant LSB is turned off. Similarly, in the middle of the N-step SAR conversion, a sudden $-\Delta I_L$ or $+\Delta V_{\mathrm{in}}$ can result in increasing V_{out} above $V_{\mathrm{ref},H}$, (i.e., overshoot), despite the turn off of the last determined bit during SAR bit-cycling. This indicates that the already determined bits, e.g., $B(6:3)$ in Fig. 16(b), hold the wrong value due to the unaccounted $-\Delta I_L$ or $+\Delta V_{\mathrm{in}}$ disturbance. Such interruptions during SAR control (or PWM) should be corrected by disabling all the switch-array pMOS fingers immediately instead of wasting time investigating the remaining bits [e.g., $B(2:0)$ in Fig. 16(b)], and increasing the V_{out} overshoot. The proposed lower-bound trigger logic is implemented through a 2-bit sequence detector, as shown in Fig. 14. The sequence detector asserts its output, *purge*, when two DEC edges occur in succession, as in Fig. 16(b) when turning off $B(3)$ is not enough to stop overshooting. On the other hand, the *Moore* machine resets to its initial state when an INC edge occurs. After turning off the whole pMOS switch array through the activated *purge*, the lower-bound logic restarts the SAR search operation when the output voltage, V_{out}, falls below $V_{\mathrm{ref},L}$ due to any $+\Delta I_L$ or $-\Delta V_{\mathrm{in}}$ disturbance, as in Fig. 16(b) when the PWM LSB $B(-1)$ is not enough to supply the required I_L.

3) DC Correction Loop: PD compensation has the disadvantage that it can reduce the steady-state dc accuracy. During binary search, the pMOS DAC array is sequentially turned on, starting from the MSB, until V_{out} reverses the direction of its slope and starts to increase toward the hysteresis window after turning on *B(i)*. Since the pMOS array current depends on the dropout voltage, as V_{out} increases, the current of the pMOS array, including the last turned on finger *B(i)*, decreases and V_{out} can get stuck below $V_{\mathrm{ref},L}$ without reaching the hysteresis window.

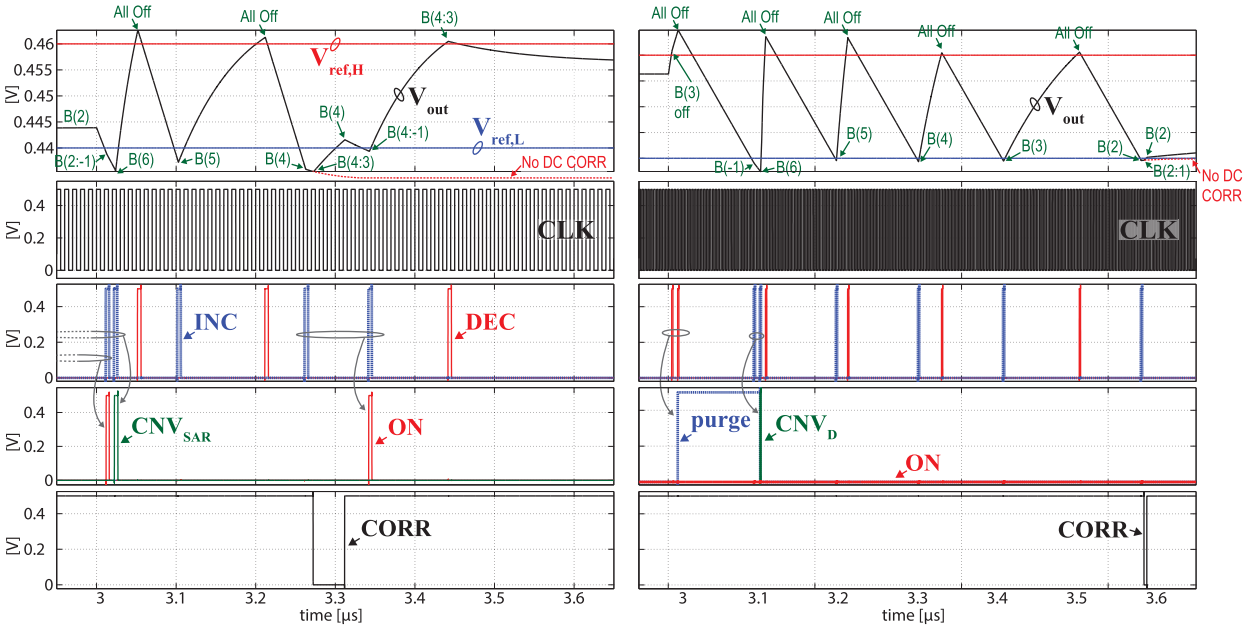


Fig. 16. RLDO simulated response to a periodic load swing between 40 and 200 μA within 200 ps, $V_{\text{in}} = 0.5$ V, $V_{\text{ref}} = 0.45$ V, $C_{\text{out}} = 0.4$ nF, and $f_{\text{CLK}} = 100$ MHz, demonstrates the effectiveness of the interruption loops in circumventing artificial overshoots/undershoots. When I_L is 40 μA, the RLDO converges to $B(2)$ in the ON-state, while the remaining switches in the OFF-state ($I_{\text{LSB}} \sim 10$ μA). At $I_L = 200$ μA, the SAR converges to $B(4:3)$ on. (a) Response when I_L increases from 40 to 200 μA during the fifth SAR iteration. (b) Response when I_L decreases from 200 to 40 μA during the fourth SAR iteration.

In order to avoid such case, the next MSB switch *B(i-1)* is turned on, as an extra *safety step*, although the present bit, *B(i)*, is enough to charge V_{out} toward the hysteresis. When V_{out} is less than $V_{\text{ref},L}$ and is increasing, the sampling clock propagates to the negative output of DIFF$_L$, DL−, in Fig. 11, which is employed to set a dc correction flag CORR. As a result, the next MSB in the switch array, *B(i-1)*, is temporarily turned on to provide an extra half-*B(i)* conductance in parallel to the present investigated bit, *B(i)*, to ensure the rapid increase of V_{out} toward $V_{\text{ref},L}$ and hence avoid any possible condition of V_{out} being stuck below $V_{\text{ref},L}$. Once V_{out} exceeds $V_{\text{ref},L}$, DN in Fig. 11 is reset low which clears the dc correction flag CORR, and hence, the temporarily turned on bit is turned back off. For instance, in Fig. 16(a), $B(3)$ is turned on immediately at the next rising clock edge, via CORR, until V_{out} exceeds $V_{\text{ref},L}$. A similar architecture can follow to avoid the case of V_{out} being stuck above $V_{\text{ref},H}$.

C. Successive Approximation Controller

The RLDO's SAR logic follows a perturb and observe algorithm to determine the value of each bit in the pMOS switch array (Fig. 15). In the perturb phase, one bit in the switch array is turned on in order to test its output current value in comparison to the load current I_L. In the observe phase, the comparison result of the output voltage V_{out} with the desired target V_{ref} determines the value of the binary bit being tested through DEC and INC, coming from the PD controller to avoid oscillatory response as discussed. If V_{out} exceeds V_{ref} due to the present bit output current, DEC is set high, and the present bit under test is turned off. Otherwise, if V_{out} falls below V_{ref}, INC transitions from 0 to 1, and the present bit being tested is left on and the conversion process proceeds to the next MSB until all the bits in the switch array have been determined. Fig. 16 shows a simulated timing diagram and response of two representative load steps.

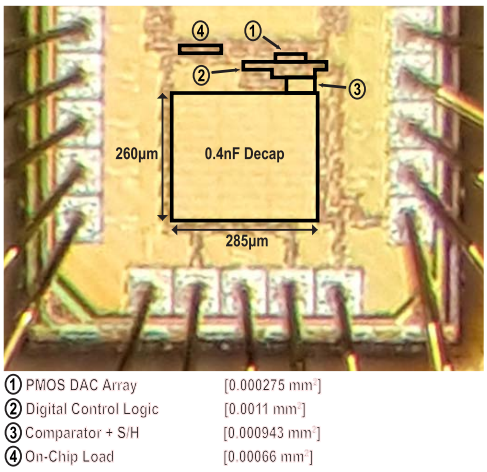


Fig. 17. Die photo of fabricated RLDO.

VI. Experimental Verification

A 7-bit RLDO was implemented in 0.0023 mm^2 in 65-nm CMOS, including the pMOS DAC array, SAR control logic, comparators, sample and hold circuits, an on-chip load, and 0.4-nF on-chip decoupling capacitance (Fig. 17).

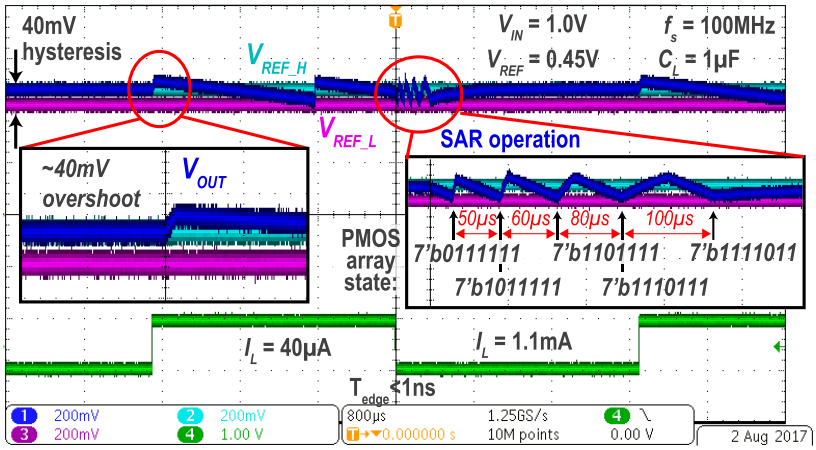


Fig. 18. Measured transient response of the RLDO to periodic square-wave load current variation with $V_{\mathrm{IN}} = 1$ V, $V_{\mathrm{OUT}} = 0.45$ V, and $C_{\mathrm{out}} = 1$ μF.

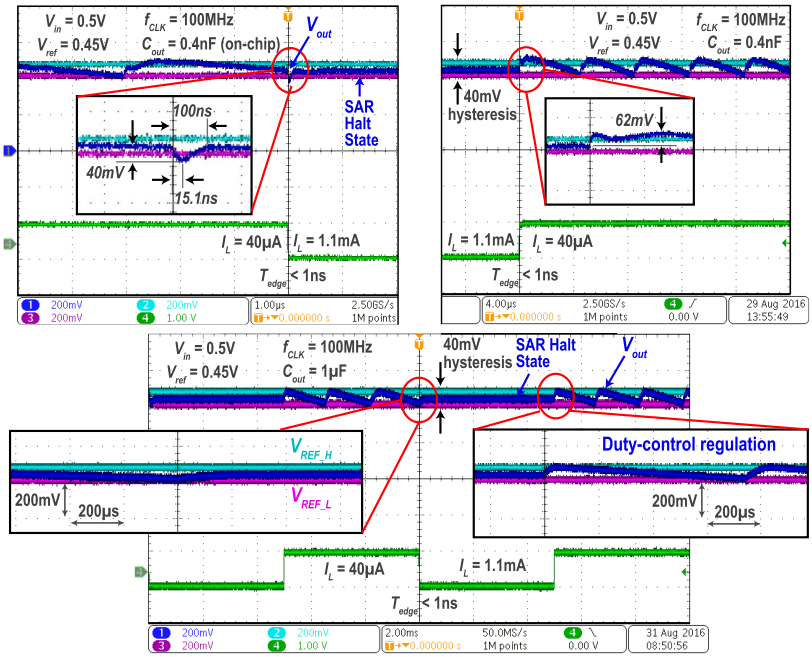


Fig. 19. Measured transient response of the RLDO to a periodic square-wave load current variation with $V_{\mathrm{IN}} = 0.5$ V, $V_{\mathrm{OUT}} = 0.45$ V, and $C_{\mathrm{out}} = 0.4$ nF (top). When $C_{\mathrm{out}} = 1$ μF, the RLDO remains stable during periodic positive and negative load steps (bottom).

A. Transient Measurements

1) Mitigating the Speed-Stability Challenge in SAR LDOs: Taking SAR decisions at a faster rate than the rate of change of V_{out} (i.e., f_L) in the hope of reducing the large staircase overshoots and undershoots of binary search results in erroneous successive decisions during the SAR conversion and hence an unstable response. Fig. 18 illustrates reliable SAR convergence despite employing a much faster clock frequency, 100 MHz, than the output time constant, 411.64 μs, thanks to the proposed PD compensation. Here, when I_L is 40 μA, the PWM controller tries to maintain V_{out} at V_{ref}. On the other hand, when I_L increases to 1.1 mA, V_{out} starts to discharge downward until it falls below $V_{\mathrm{ref},L}$ [Fig. 18 (inset)]. As a result, the lower-bound trigger logic restarts the coarse binary search with $B(6)$ on and the remaining pMOS transistors off, and hence V_{out} rapidly increases until it exceeds $V_{\mathrm{ref},H}$. At that moment, DEC is activated to turn off $B(6)$ and V_{out} discharges

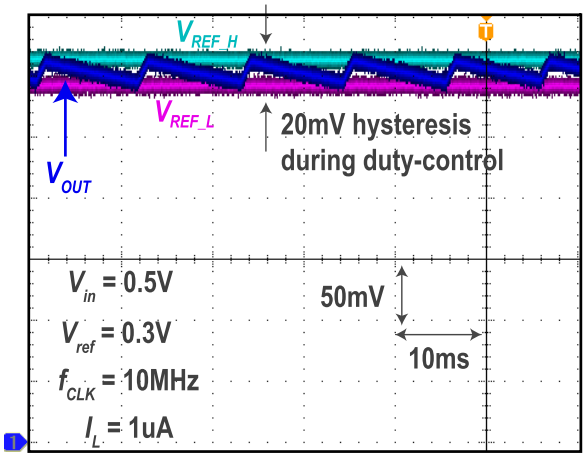
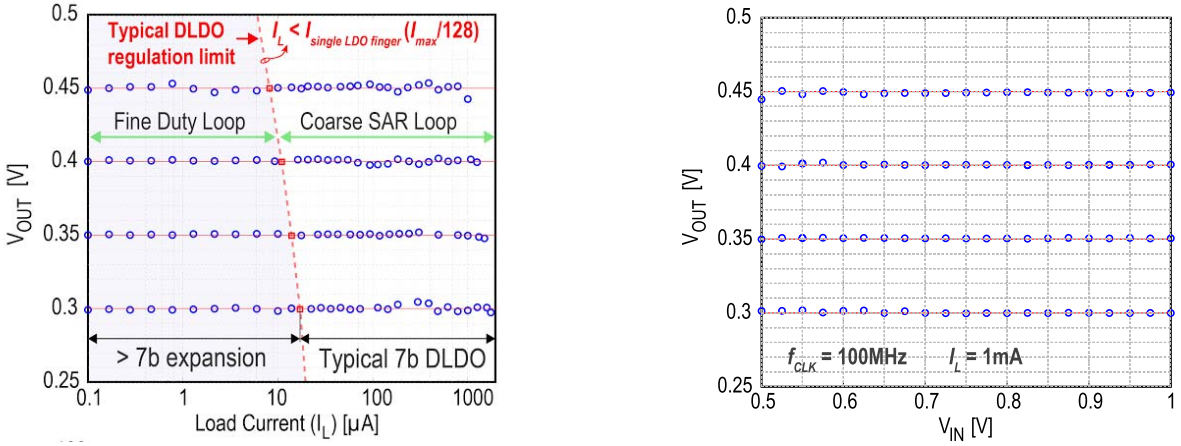


Fig. 20. Measurement of output voltage ripple during PWM duty control.

until it reaches $V_{\mathrm{ref},L}$, and then binary search continues in a similar manner. The measured duration between the turn on of the successive pMOS DAC switches is approximately 50,



(a) (b)

Fig. 21. (a) Line regulation measurement at a clock frequency of 100 MHz and a load current of 1 mA. (b) Load regulation measurement at $f_{\mathrm{CLK}} = 10$ MHz and $V_{\mathrm{in}} = 0.5$ V.

60, 80, and 100 μs, as in Fig. 18. Therefore, although V_{out} is sampled and observed at a high rate (100 MHz) to reduce overshoots/undershoots, the SAR register is updated only at a rate close to the output time constant, which enables stable operation. On the other hand, if the input 100 MHz clock instead directly ran the SAR register, $B(6)$ would be left on since V_{out} does not exceed $V_{\mathrm{ref},H}$ in the following clock cycle (and rather takes $\sim$2 μs to reach $V_{\mathrm{ref},H}$). This would result in an erroneous $B(6)$ decision, and the SAR operation would never converge. As shown in Fig. 18, V_{out} increases with binary-weighted slew rates across the successive iterations. When the SAR controller turns on $B(2)$, V_{out} settles to within the hysteresis window, and hence $B(2)$ can provide the required I_L ($I_{\mathrm{LSB}} \sim 275$ μA). As shown, the RLDO reaches a complete halt-state at steady-state with minimal quiescent power, where the SAR and PWM controllers are gated off. To realize below $\pm 4\%$ steady-state error, the PWM controller can be enabled once V_{out} is within the hysteresis.

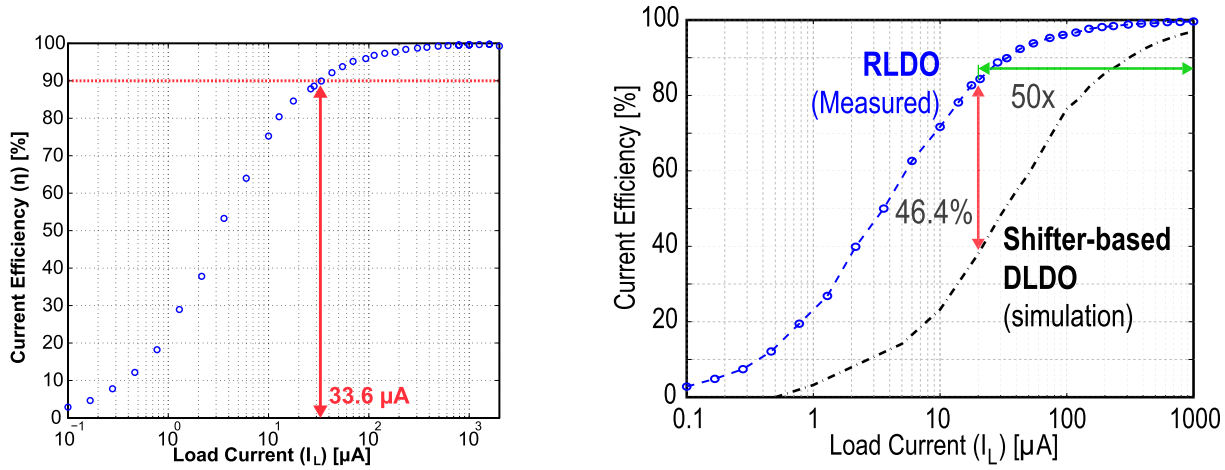
The correct SAR-loop conversion is further verified at all possible I_L and V_{in} values via the measured load and line regulation plots in Fig. 21. Thanks to the PD compensation and dc correction loop, the LDO is able to make the correct successive decisions and reach the target V_{ref} even while employing high speed clocks ranging between 10 and 100 MHz, all without getting stuck outside the hysteresis.

2) Exponential Improvement in FOM via Binary Search: Fig. 19 shows the measured transient response of the RLDO for periodic (at 1 kHz) on-chip load changes between 40 μA and 1.1 mA with 1 ns rise/fall time. The RLDO at $V_{\mathrm{in}} = 0.5$ V maintains less than 40 mV undershoot below $V_{\mathrm{ref}} = 0.45$ V (not $V_{\mathrm{ref},L}$), for a quiescent current of 14 μA at a clock frequency of 100 MHz, thereby achieving a response time of 15.1 ns and a settling time of 100 ns. After the I_L step increase, the SAR operation is restarted with $B(6)$ on and the remaining bits off. For a $\Delta V_{\mathrm{dropout}}$ of $\sim$90 mV, the MSB current is $\sim$845 μA. Therefore, $B(6)$ slows down the V_{out} discharge rate until the following clock edge, after 10 ns, when $B(5)$ is turned on, which reverses V_{out} direction and brings V_{out} back to within the hysteresis, and hence T_R is ideally 10 ns. In contrast, a modeled 65-nm shifter-based linear-search DLDO with the same fan-out capability provides $25\times$ ($>2^N/N$) and $13.7\times$ slower T_R and T_S, respectively, while consuming $2^7\times$ the quiescent current. Thus, the RLDO achieves an FOM of 199.4 ps at $V_{\mathrm{IN}} = 0.5$ V, while the modeled 65-nm DLDO achieves 638 ns, illustrating higher than $2^{2N}/N$ FOM improvement as predicted from theory. The RLDO's measured overshoot is 62 mV which demonstrates the effectiveness of the proposed upper-bound trigger logic to disable the pMOS switches of $B(6:5)$ immediately rather than waiting to check the remaining bits $B(4:0)$, after 1.1 mA to 40 μA change. Afterward, V_{out} is regulated by the duty controller to its steady-state value of 0.45 V.

3) PD Compensation Efficacy: Fig. 19 also shows the efficacy of the proposed PD compensation scheme—stable load step tests were performed even with a 1 μF external capacitor to make the output pole, f_L, $2500\times$ more dominant than $f_{\mathrm{CLK}} = 100$ MHz, which would render a baseline DLDO fully oscillatory. As shown in Fig. 19, the well-behaved first-order-like V_{out} response confirms the elimination of the integrator pole from the loop dynamics, as predicted from the theory in Section III, thereby realizing a single-pole system, and hence, achieving stable operation irrespective of C_{out}, I_L, and conductance step M.

B. Steady-State Measurements

1) Mitigating Limited DC Accuracy in SAR DLDOs: Fig. 20 demonstrates the efficacy of the PWM controller. At a current $20\times$ less than I_{LSB} ($\approx$20 μA at $\Delta V_{\mathrm{dropout}} = 0.2$ V), the PWM controller regulates V_{out} with $<0.2\% V_{\mathrm{ref}}$ steady-state error (20.3-bit), all with I_L-independent peak-to-peak ripple of 20 mV. Fig. 21 demonstrates that the proposed PWM control mitigates the challenge of limited current range with acceptable dc accuracy in binary search DLDOs, and in fact achieves load regulation with less than $\pm 2\% V_{\mathrm{in}}$ steady-state error for a hysteresis window of ± 10 mV across a



(a) (b)

Fig. 22. Measured current efficiency η. (a) At $V_{\text{in}} = 0.5$ V and $V_{\text{out}} = 0.3$ V ($f_{\text{CLK}} = 10$ MHz), demonstrating efficiency higher than 90% from 33.6 μA to 2 mA. (b) At $V_{\text{in}} = 0.5$ V and $V_{\text{out}} = 0.45$ V ($f_{\text{CLK}} = 10$ MHz).

Design	Okuma, CICC 2010	Kim, ISSCC 2016	Nasir, TPE 2016	Lee, JSSC 2017	This Work
Process	65nm	65nm	130nm	28nm	**65nm**
Active area [mm^2]	0.042	0.029	0.114	0.021	**0.0023**
Control	Time-Driven	Event-Driven	Time-Driven	Time-Driven	**SAR/PD/PWM**
V_{IN} [V]	0.5	0.5 – 1.0	0.5 – 1.2	1.1	**0.5 – 1**
V_{out} [V]	0.45	0.45 – 0.95	0.45 – 1.14	0.9	**0.3 – 0. 45**
Load range (I_L)	10μA – 250μA (25x)	7.2μA – 3.5mA (486x)	100μA – 4.6mA (46x)	4mA - 200mA (50x)	**100nA – 2mA (20,000x)**
PMOS-Array resolution	8-bit	10-bit	7-bit	6.6-bit	**7-bit**
Effective resol. ($\log_2(I_L$ range))	4.6-bit	8.9-bit	5.5-bit	5.6-bit	**14.3-bit**
Load range with η>90%	25μA – 250μA (10x)	150μA – 500μA (3.3x)	2.9mA-4.6mA (1.6x)	N.R.	**33.6μA – 2mA (60x)**
C_L [nF]	100	0.4	1	23.5	**0.4**
Quiescent I_Q [μA] during load transient test	2.7	12.5†	221	110†	**14**
V_{droop} @ load step size for load transient test	40mV @ 0.2mA	22mV @ 0.2mA	40mV @ 0.7mA	120mV @ 180mA	**40mV @ 1.06mA**
Response time T_R [ns] for load transient test	20000	44	57	4000*	**15.1**
FOM** for load transient test [ns]	270	2.75	18.04	2.44*	**0.199**
Load step rise/fall time for load transient test††	N.R.	N.R.	N.R.	4μs*	**< 1ns**
Peak current efficiency η [%]	98.7	96.3	98.3	99.94	**99.8**
Sampling clock range	1MHz – 10MHz (10x)	200MHz	5MHz – 75MHz (15x)	N.R.	**1MHz – 240MHz (240x)**
Load regulation [mV/mA]	0.65	N.R.	< 10 across range	N.R.	**< 5.6 across range**
Line regulation [mV/V]	3.1	N.R.	N.R.	N.R.	**2.3**
Settling time [μs]	240	80	1.1	20	**0.1**

N.R. = Not Reported

† I_Q consumption during transient test was not reported, min(I_Q) is assumed

* Observed from transient plots

**FOM = C_{out} $\Delta V_{droop}/(I_{max}-I_{min})$ x $I_Q/(I_{max}-I_{min})$, P. Hazucha et al., JSSC'05

†† load rise/fall time should be < T_R/10 for a valid measurement

Fig. 23. Comparison of the RLDO with prior art DLDOs.

20 000× load dynamic range (14.3-bit: from 100 nA to 2 mA). Without PWM control, the dynamic range would be limited to 2.64× (1.4-bit). In this design, the PWM controller is only enabled after the SAR fully converge and not within the intermediate iterations, which trades accuracy for power. Therefore, for $I_L > I_{\text{LSB}}$, the PWM controller may or may not be enabled depending on whether the SAR-halt-V_{out}-value resides within the target hysteresis or not. This enables $< \pm 2\% V_{\text{ref}}$ and $< 0.6\% V_{\text{ref}}$ steady-state error when the PWM is disabled and enabled, respectively, as in Fig. 21(a). For $I_L < I_{\text{LSB}}$, the PWM controller is always enabled, and hence the steady-state error is $< \pm 0.6\%$, even when $V_{\text{ref}} \sim V_{\text{in}}/2$, as shown in Fig. 21(a). In a non-PWM-modulated 7-bit DLDO, the minimum supplied current cannot go below I_{LSB} due to accuracy and ripple limitations. Fortunately, PWM control can effectively perform V_{out} regulation below the single finger current, enabling extension of the LDO effective resolution, $\log_2(I_{L,\text{max}}/I_{L,\text{min}})$, from 7 to 14.3 bit, with a worst case load regulation of 5.6 mV/mA. As shown in Fig. 21(b), a line regulation of 2.3 mV/V is achieved.

2) Exponential Improvement in Quiescent Power: Fig. 22 verifies the exponential $(1/2^N)$ improvement in the quiescent power of the RLDO architecture over baseline linear-search designs. A peak current efficiency of 99.8% for 0.5 to 0.3 V conversion is achieved. More importantly, the RLDO achieves a current efficiency greater than 90% from 33.6 μA to 2 mA, a 60× load current dynamic range [Fig. 22(a)], and hence, achieves the widest load range with efficiency higher than 90% as compared to 1.6× (even with fine-grain clock gating of the barrel shifter [34]), 3.3×, and 10× in the prior art (Fig. 23).

Furthermore, as depicted in Fig. 22(b), current efficiency greater than 84.4% is achieved across a 50× dynamic range at 0.5 to 0.45 V, exceeding a simulated barrel-based DLDO by 46.4%.

C. Performance Summary

From load regulation measurements and transient tests at various f_{CLK} frequencies ranging from 1 to 240 MHz, the RLDO with PD compensation and PWM regulation is stable irrespective of I_L, f_{CLK}, and C_{out}. In comparison to prior art DLDOs in Fig. 23, the RLDO at 0.5 V achieves the fastest response (3×) and settling (11×) times, largest load dynamic range, smallest area (9.13×), and best FOM (13.8×).

VII. Conclusion

This paper has described a new recursive DLDO architecture that improved response time, settling time, active area, and quiescent power over conventional and augmented linear search-based DLDOs via the use of a successive approximation control scheme with PD compensation. Additionally, the RLDO's dynamic load range and steady-state error performance were enhanced through duty control of an additional LSB transistor.

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