A 13-mW 64-dB SNDR 280-MS/s Pipelined ADC Using Linearized Integrating Amplifiers

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***Abstract*— A 12-bit pipelined analog-to-digital converter (ADC) using a new integration-based open-loop residue amplifier topology is presented. The amplifier distortion is cancelled with the help of an analog linearization technique based on a tunable input-driven active degeneration. Amplifier gain and nonlinearity errors are detected in background using split-ADC calibration technique. The mismatch between the two half-ADCs is minimized by sharing the residue amplifier between the two half-ADCs and adding the calibration offset over time. Based on this "split-over-time" calibration architecture, a two-lane prototype ADC was fabricated in 28-nm CMOS that achieves 64-dB signal-to-noise + distortion ratio and 77dB spurious-free dynamic range at Nyquist input after calibration. Operating at 280 MS/s, the ADC consumes 13 mW from 1-V supply, exhibiting a Schreier figure-of-merit of 164.3 dB. By dissipating only 0.4 mW in the residue amplifiers, the linearization technique helps the ADC achieve an improvement of at least 3 dB in Schreier FoM over existing state-of-the-art ADCs with comparable architectures.**

***Index Terms*— Analog correction, analog-to-digital conversion (ADC), background calibration, linearization, pipelined ADC, residue amplifier, split-ADC, switched-capacitor circuits.**

I. Introduction

In analog-to-digital converters (ADCs), noise is often the key bottleneck that plays a defining role in the choice of the ADC architecture. For high-resolution ADCs, noise requirements from the backend can impose a severe penalty on the overall ADC power consumption. Hence, in order to reduce the noise contribution of the backend, gain has to be introduced in the signal chain. This has made pipelined ADCs with residue amplification the most popular architecture for high-resolution applications. This is also reflected in [1] where pipelined ADCs (including pipelined SARs) have dominated the region of >10-bit ENOB.

Since gain plays a vital role in pipelined ADC architecture, residue amplifiers often dominate the overall ADC power budget. As a result, the power efficiency of residue amplifiers has been the focus of extensive research over the years. Residue amplification essentially involves building a voltage by delivering an input-dependent charge to a load capacitor in a given time period. The load capacitor can be driven differentially by a minimum of four transistors, and the power efficiency of an amplifier is determined by how efficiently these transistors are driven and the amount of settling accuracy allowed for the output voltage.

Traditionally, residue amplifiers have been implemented by using high-gain opamps in closed-loop configuration with the gain being set by a passive feedback network [2], [3]. Although capable of achieving excellent gain accuracy, these implementations suffer from excessive circuit overhead and require a high amount of settling. In the recent years, efforts have been made to improve the power efficiency of residue amplifiers by reducing the settling accuracy and the circuit overhead within the amplifier to a minimum by utilizing a combination of digital calibration and alternative amplifier topologies, such as zero-crossing-based circuits (ZCBC) [4]–[6], ring amplifiers (RAMP) [7]–[9], partially settling open-loop amplifiers [10], and inverter-based amplifiers [11]–[13]. Although these have been fairly successful in improving the power efficiency, they still retain a significant amount of overhead for driving the input transistors.

Another recently introduced topology that has shown excellent power efficiency is the dynamic amplifier [14]–[17]. A dynamic amplifier combines a simple open-loop gain structure with integration-based amplification. Integration-based settling requires the lowest possible bandwidth for achieving a certain gain. When combined with negligible circuit overhead, it ensures that nearly all the current is spent on charging the load capacitor, making this amplifier potentially the most power-efficient residue amplifier topology.

Dynamic amplifier, however, suffers from serious drawbacks with regard to gain accuracy. Its low linearity makes it necessary to resolve a large number of bits (6 bits in [16], 5 bits in [17]) to lower the input signal swing for the residue amplifier. Due to a smaller input swing, a higher gain is required from the amplifier. And a high gain is challenging to achieve at high speed and resolution, with both [16], [17] opting for a reduced input range for later stages.

In order to avoid such restrictions on the amplifier gain and input swing, a non-linearity compensation technique is required which ideally does not introduce significant overhead. Also, considering the susceptibility of open-loop integration to process-voltage-temperature (PVT) variations, the compensation technique should be combined with background detection with fast convergence. Amongst the several amplifier nonlinearity calibration techniques reported in the literature, split-ADC technique [18]–[20] is one of the very few which satisfies all of the above criteria. In [20], the split-ADC technique is used in conjunction with fully digital post-processing to calibrate nonlinearity. While digital detection of non-linearity can be

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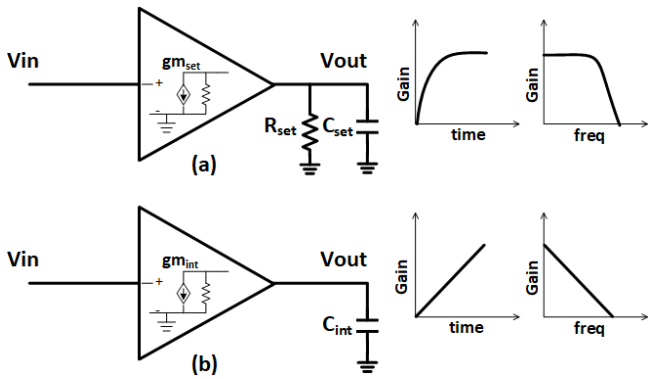

Fig. 1. Settling versus integrating amplifier.

slowed down to reduce its power, digital correction has to operate at the ADC sampling rate, and can exhibit significant power dissipation.

This paper presents an integrating amplifier that achieves good power efficiency along with good linearity with the help of an analog linearization technique. The nonlinearity is detected in background with the help of split-ADC architecture. The linearization technique allows the amplifier to be used for a wider input signal swing at the expense of minimal circuit overhead.

This paper is organized as follows. Section II provides an overview of the power efficiency and design challenges associated with an integrating amplifier. Section III describes the proposed integrating amplifier and the linearization technique. Section IV discusses the ADC implementation. Finally, Sections V and VI present the measurement results and conclusion.

II. Integrating Amplifiers

Most amplifiers used for residue amplification consist of an opamp with a finite dc gain and a settling speed defined by its 3-dB bandwidth. The opamp can be used in closed-loop configuration where the gain is determined by the feedback factor, often a capacitive ratio. Another option is to use it in open-loop where the amplifier is loaded by a resistor which, along with the input gm, defines the gain of the amplifier. While there are several differences in the open-loop and closed-loop configurations, the gain in both cases settles exponentially, as shown in Fig. 1(a). As a result, the gain error decreases exponentially with time, due to which the output time constant τ is designed to be much smaller than the amplification period.

In integrating amplifiers, the gain increases linearly with time, as shown in Fig. 1(b). For an ideal integration, the integrating amplifier needs to possess infinite dc gain and an infinitesimally small bandwidth (i.e., $\tau \to \infty$). However, in reality, the output impedance of the integrating amplifier will be finite. Hence, in this paper, the integrator behavior is approximated by keeping the settling lower than 0.05 τ. For that amount of settling, the integrating amplifier deviates by less than 2.5% with respect to an ideal integrator, which is considered acceptable for the scope of this paper. A settling of $<0.05\ \tau$ requires the integrating amplifier to have an intrinsic gain that is 20 times higher than the desired discrete-time gain.

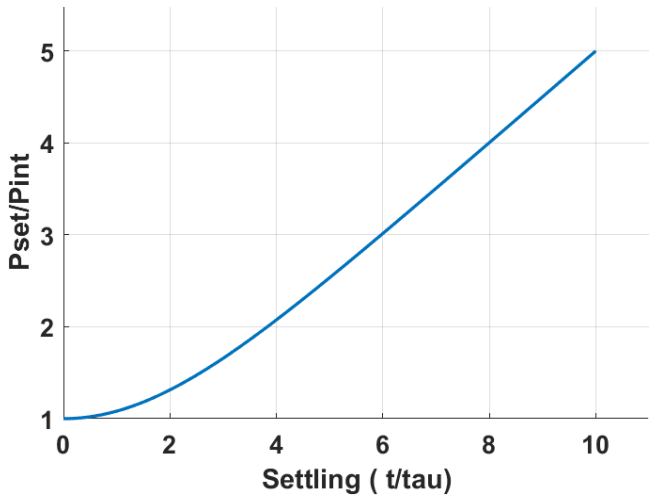

Fig. 2. Normalized settling amplifier power versus settling.

A. Power Efficiency

While the intrinsic gain requirement is relatively high, the integrating amplifier trades it off with power consumption. The power efficiency of an integrating amplifier can be quantitatively analyzed by comparing the gm required to achieve the same gain and SNR. The gain of the integrating amplifier A_{int} can be expressed as

$$A_{\text{int}} = \frac{\text{gm}_{\text{int}}}{C_{\text{int}}} \cdot T_a \tag{1}$$

where gm_{int} and C_{int} are the integrating amplifier's transconductance and load capacitance, respectively, and T_a is the amplification time. With respect to the integrating amplifier, the transconductance required by a settling amplifier gm_{set} with a settling accuracy of $N\tau$ to achieve the same voltage gain and SNR in the same amplification time T_a can be calculated as (see the Appendix)

$$\frac{\text{gm}_{\text{set}}}{\text{gm}_{\text{int}}} = \frac{N}{2}\frac{(1-e^{-2N})}{(1-e^{-N})^2}. \tag{2}$$

The gm of a settling amplifier normalized to an integrating amplifier is shown in Fig. 2. It can be seen that for higher values of settling, a settling amplifier consumes $N/2$ times the power of an integrating amplifier for the same gain and SNR.

B. Design Challenges

Although integrating amplifiers offer a much more power-efficient way of amplification, they suffer from some major design issues. These issues have so far limited their application in high-resolution ADCs and need to be addressed.

1) Jitter: For an exponentially settling amplifier, the amplifier output reaches close to its final value well before the sampling point, as shown in Fig. 3, making the sampled output voltage insensitive to any jitter in the sampling clock. However, as the integrating amplifier settles linearly, any uncertainty in the sampling moment will directly appear as noise on the output voltage sampled by the succeeding stage. Since clock jitter has a multiplicative effect on the amplifier

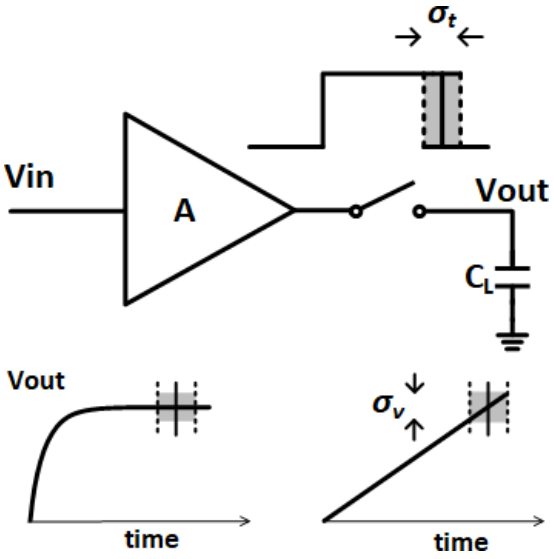

Fig. 3. Effect of clock jitter in settling versus integrating amplifier.

output voltage, the resulting noise is directly proportional to the slope of the output and can be expressed as

$$\text{Output jitter-induced noise voltage,} \quad \sigma_v = V_{\text{in}} \frac{\text{gm}}{C_L} \sigma_t \quad (3)$$

where σ_t is the rms jitter in the sampling clock. Ignoring the input parasitics, the SNR at the amplifier output resulting purely from clock jitter can be calculated as

$$\text{SNR}_{\text{jitter}} = \frac{(A_i V_{\text{in}})^2}{\left(V_{\text{in}} \frac{\text{gm}}{C_L} \sigma_t\right)^2} = \frac{T_a^2}{\sigma_t^2}. \quad (4)$$

It can be inferred from (4) that as the amplification period decreases, the jitter-induced noise will become more significant. This implies that for higher ADC clock speeds, it can be beneficial to use interleaving to minimize the impact of clock jitter on the ADC SNR.

2) Gain and Nonlinearity: As seen in (1), the integrator gain strongly depends on the input gm, making it very susceptible to PVT variation. In addition, the open-loop nature of the integrating amplifier also makes it more vulnerable to input distortion. So in order for application in high-resolution ADCs, calibration of these amplifier non-idealities is essential.

Calibration consists of detecting the amplifier linear and non-linear gain errors and subsequently correcting them. While the error detection is usually performed in digital, the error correction can be implemented in either digital or analog domain. Digital correction of gain errors has been widely reported in the literature [10], [12], [18]–[21]. Although it simplifies the analog implementation of the amplifier, digital correction entails certain costs. First, digital correction of gain error will result in an amplifier signal swing that is different from the specification it was designed for, causing the SNR to deviate from its desired value.

Second, while the digital detection can be carried out at a lower frequency, the digital hardware for correcting the gain and non-linearity errors has to operate at the ADC sampling speed. The digital nonlinearity correction usually involves a lookup table (LUT) which stores a set of codes that are multiplied by a coefficient and added to the ADC output to compensate for the amplifier distortion [19]. The resolution of the LUT codes and the coefficient is determined by the required ADC resolution and the inherent amplifier distortion. And the size of this LUT, together with the ADC sampling speed, determines the area and power consumption of the digital calibration hardware.

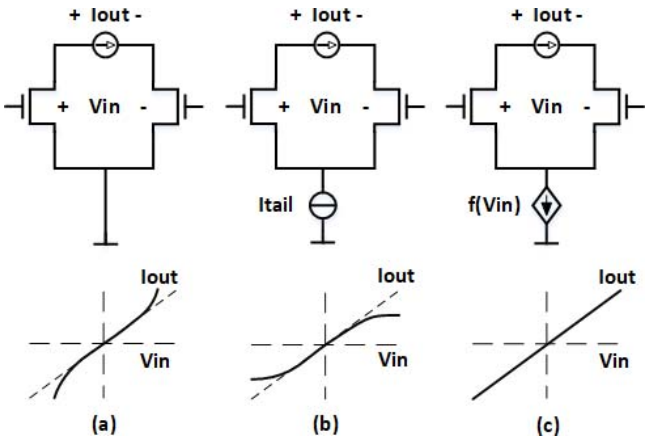

Fig. 4. Linearization principle.

As the linearity requirements from the amplifier are relaxed, the power consumption attributed to the digital correction hardware will increase. Considering this design tradeoff's potential to limit the benefits of using calibration, an analog correction scheme, where the errors are resolved directly within the amplifier, can provide a much more attractive alternative.

While linear gain errors can be easily fixed by tuning a bias current, as demonstrated in [13], no such straightforward solutions are available for correcting nonlinearity. A few analog correction schemes for non-linearity have been published [22]–[24]. While Miyahara *et al.* [22] provide excellent non-linearity cancellation [>14-bit spurious-free dynamic range (SFDR)], it can only be used for closed-loop amplifiers. Yu *et al.* [23], [24] provide linearization techniques for open-loop amplifiers with limited settling. But they achieve limited success in cancelling the amplifier distortion (<10-b SFDR) and are not suitable for application in high-resolution ADCs

III. Linearized Integrating Amplifier

A. Linearization Principle

The proposed linearization technique [25], as shown in Fig. 4, is based on two observations as follows.

1) Consider a differential common-source amplifier with the input transistors biased in deep weak inversion (WI). If their sources are tied to ground, which means that there is no restriction on the tail current, then this amplifier displays an expanding V–I characteristic.
2) If the tail current is restricted by adding an ideal current source, then the amplifier would shift to a compressing V–I characteristic.

Between these two opposing distortion paradigms, a midpoint for the tail current characteristic can be found for which the amplifier exhibits a perfectly linear gm. This can be calculated by assuming that the input transistors are biased in WI saturation region. Then the quiescent current through the input transistors can be expressed as

$$I_{D1} = I_{D2} = I_S e^{\frac{V_g - V_s - V_{\text{th}}}{nV_T}} \tag{5}$$

where V_g and V_s are the bias gate and source voltages of the input pair, respectively, V_{th} is the threshold voltage, I_s is the saturation current, and n is a technology parameter. If a differential input voltage ΔV_{id} is applied to the input pair, the differential output current and the tail current can be expressed as

$$\Delta I_o = I_{D1} - I_{D2} = I_S e^{\frac{V_g - V_s - V_{\text{th}}}{nV_T}} \left(e^{\frac{\Delta V_{\text{id}}}{2nV_T}} - e^{\frac{-\Delta V_{\text{id}}}{2nV_T}} \right) \tag{6a}$$

$$I_{\text{tail}} = I_{D1} + I_{D2} = I_S e^{\frac{V_g - V_s - V_{\text{th}}}{nV_T}} \left(e^{\frac{\Delta V_{\text{id}}}{2nV_T}} + e^{\frac{-\Delta V_{\text{id}}}{2nV_T}} \right). \tag{6b}$$

For the input pair to be perfectly linear, the differential current should have a perfectly linear relationship with the differential input voltage, which can be defined as

$$\Delta I_o = \text{Gm} \Delta V_{\text{id}} \tag{7}$$

where Gm is the desired differential transconductance of the input pair. By using (6a), (6b) and (7), the I_{tail} can be expressed as

$$I_{\text{tail}} = \text{Gm} \Delta V_{\text{id}} \frac{\left(e^{\frac{\Delta V_{\text{id}}}{2nV_T}} + e^{\frac{-\Delta V_{\text{id}}}{2nV_T}} \right)}{\left(e^{\frac{\Delta V_{\text{id}}}{2nV_T}} - e^{\frac{-\Delta V_{\text{id}}}{2nV_T}} \right)} = \text{Gm} \Delta V_{\text{id}} \coth \left(\frac{\Delta V_{\text{id}}}{2nV_T} \right). \tag{8}$$

By using Taylor series expansion, (8) can be expressed as

$$I_{\text{tail}} = 2nV_T \text{Gm} \left(1 + \left(\frac{\Delta V_{\text{id}}}{2nV_T} \right)^2 + \cdots \right). \tag{9}$$

This behavior can be approximated by using the sum of the output currents of two WI transistors driven by ΔV_{id}. However, as the sum would be extremely sensitive to PVT and Monte Carlo variations, independent circuit parameters are required to tune and match the sum of currents closely to the desired I_{tail} characteristic.

B. Linearization Parameters

In order to tune the tail current characteristic, the following tail current parameters are made programmable, as illustrated in Fig. 5.

1) Tail bias voltage, which is tuned by using a programmable current digital-to-analog converter into a bias diode.
2) Input attenuation, which determines the extent with which the tail current modulates with the input signal. This attenuation is implemented by using a programmable capacitor array to ground to tune the drive strength of the input.

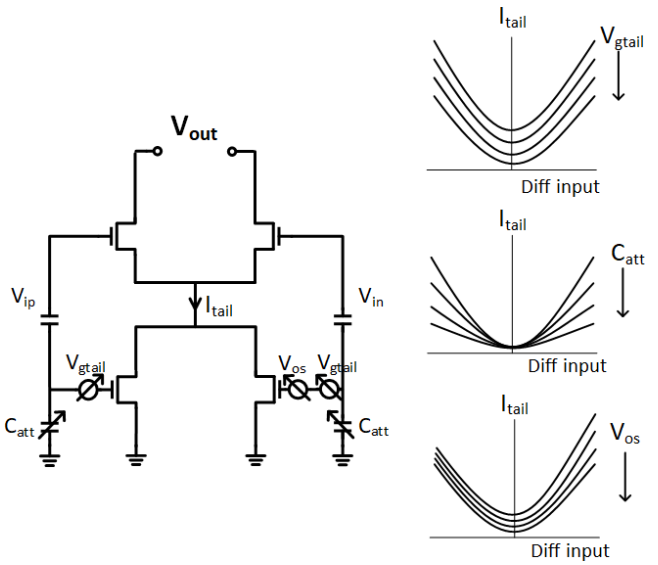

Fig. 5. Linearization parameters.

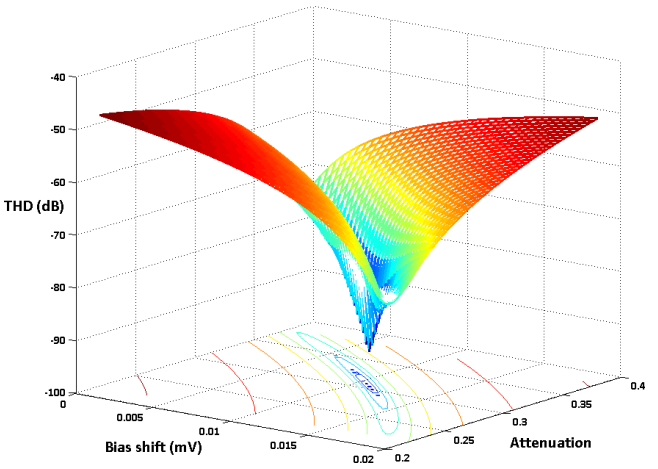

Fig. 6. Simulated Amplifier total harmonic distortion versus linearization parameters.

These two knobs establish how closely the tail current characteristic approximates the ideal function, hence having a significant effect on the linearity of the amplifier. This is reflected in Fig. 6, which shows the simulated total harmonic distortion (THD) (considering the first five harmonics) of a 250-MHz switched-capacitor amplifier using the proposed integrating amplifier shown in Fig. 7, with an input swing of 300-mVp–pdiff and a gain of 4×, as these two parameters are swept. It can be seen that over the entire search space of combinations of these two parameters, a unique set can be found for which the amplifier distortion exhibits a minimum, where the THD is <-90 dB. Due to the uniqueness of this combination of parameters, it is easier for the calibration to locate this minimum. Also, this minimum can be found for every PVT corner, just at a slightly different spot. Fig. 8 shows the deviation of the amplifier output from its ideal value. For an input swing of 300-mVp–pdiff, the error reduces from nearly -40 to -55 dB by sweeping only C_{att} and nearly -90 dB after linearization with both C_{att} and V_{gtail}.

While these two tuning parameters are very effective against odd-order distortion, they only adjust the circuit symmetrically.

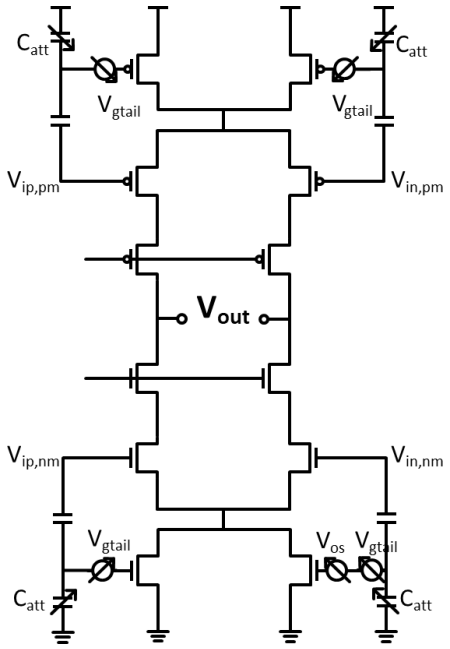

Fig. 7. Proposed integrating amplifier topology.

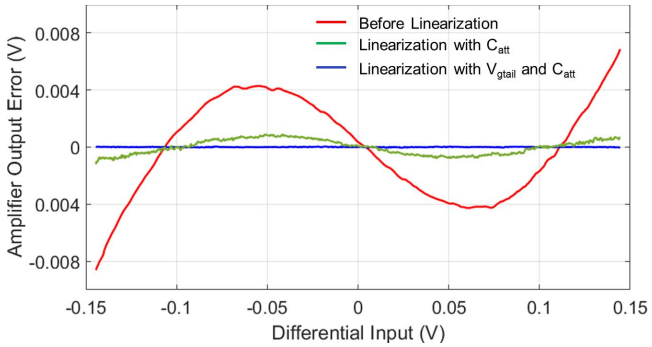

Fig. 8. Amplifier output error voltage before and after linearization.

Due to the high inherent distortion of the WI input pair, any offset or gm mismatch in the amplifier creates a significant even-order distortion. In order to avoid this from limiting the overall amplifier linearity, this mismatch is compensated for by adding an extra tunable offset in the tail current source, as seen from Fig. 5, with the help of an additional programmable current source in the bias diode of one of the tail transistors. This offset provides a knob to correct for the imbalance arising out of any mismatch in the amplifier. It should be noted that this tunable tail current offset does not cancel the inherent offset of the amplifier, but merely corrects the even-order distortion by counteracting the imbalance in the amplifier.

C. Implementation

Based on the proposed linearization technique, an integration-based amplifier was implemented with the input being driven through both NMOS and PMOS sides, as shown in Fig. 7. Since the linearization technique requires the transistors to be biased in deep WI region, the amplifier power efficiency benefits from an excellent gm/I_d ratio. Cascode devices are used to boost the output impedance of the amplifier. The effect of parasitic gate–drain capacitances of the input transistors is cancelled with the help of cross-coupled neutrodyning caps. The tail current offset is implemented only in the NMOS tail, as it can correct for the entire amplifier imbalance by itself.

Although the integrating amplifier has a tail current source, it does not provide a reliable common-mode (CM) control. Hence, two current sources, tied to the output and driven by a switched-cap CM feedback loop, are used to regulate the output CM level. These current sources are one-fourth the size of the input pair to limit their impact on total amplifier noise.

Table I shows a comparison of the proposed amplifier with other recent residue amplifier topologies from the literature. It can be seen that the linearization technique allows this topology to achieve a linear gain with lowest settling and power overhead.

IV. ADC Implementation

In order to test the efficiency of the proposed integrating amplifier, it was incorporated in a two-lane 14-bit SHA-less pipelined ADC, as shown in Fig. 9. A resolution of 3-bit per stage was chosen along with a residue amplifier gain of 4× as a compromise between ADC power efficiency and design ease. Stages 2–5 are scaled by a factor of 2 with respect to stage 1 in order to save power. The ADC errors are detected in digital with the help of split-ADC calibration technique. All pipeline stages are calibrated for amplifier gain and non-linearity errors. The residue amplifiers in the first two stages utilize all three linearization parameters. Due to lower accuracy requirements, stages 3–5 are implemented with only the tail bias and offset parameters without the coupling cap between input and tail nodes.

A. Calibration Architecture

In split-ADC technique [18]–[20], an ADC is split into two identical half-ADCs. These two half-ADCs digitize the same input sample, but are forced to take different trajectories by injecting an offset between the two ADC references. The two ADC outputs can be averaged to obtain the overall offset-free digital output, while their difference can be used to detect any non-idealities in the half-ADCs. Each of the non-idealities—gain error, even-order, and odd-order distortion—produces a unique artifact in the difference signal, as seen from Fig. 10, which can be used to estimate the magnitude of the respective non-ideality present in the residue amplifier.

Once the digitized outputs are generated, they are imported into MATLAB where the difference signal is generated and processed. This difference signal is driven toward a straight line by tuning the ADC stage gains and linearization parameters. The gain errors are corrected in two steps—coarse manual adjustments of the on-chip programmable bias and off-chip automatic fine tuning of the digital gain in MATLAB. In a future prototype, the coarse tuning of the on-chip bias can be substituted by an on-chip constant gm-biasing circuit, which makes the amplifier gain more immune to PVT variations.

TABLE I
SUMMARY OF POPULAR RESIDUE AMPLIFIER TOPOLOGIES

	Settling Requirements	Linearity	Power Overhead
Closed-loop amplifier	High, > 2τ shown in [20]	High	Moderate to high. High DC loop gain required to achieve accurate closed-loop gain. Inverter-based amplifier [11-13] simplify overhead with help of calibration
Open-loop settling amplifier	Moderate to high, 1.5τ shown in [10]	Low, needs calibration	Medium. Requires moderate DC gain
Zero-Crossing Based [4-6]	Low	Moderate, requires an offset-compensation	Medium. Requires an accurate comparator
Ring Amplifier [7-9]	Low, uses slew-based charging before stabilizing	Moderate to high	Medium. Requires 2 stages of inverters to drive the output stage
Dynamic Amplifier [14-17]	Low	Low. [14-17] resolve large number of bits before amplification	Negligible
Proposed Integrating Amplifier	Low, <0.05τ	Low, high after linearization	Extremely low. ~1dB SNR drop due to input loss from driving tail current

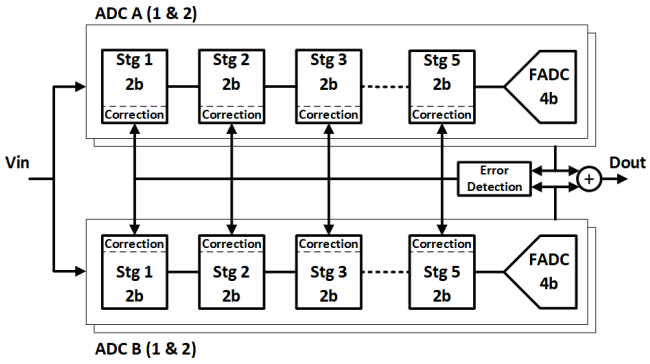

Fig. 9. ADC architecture.

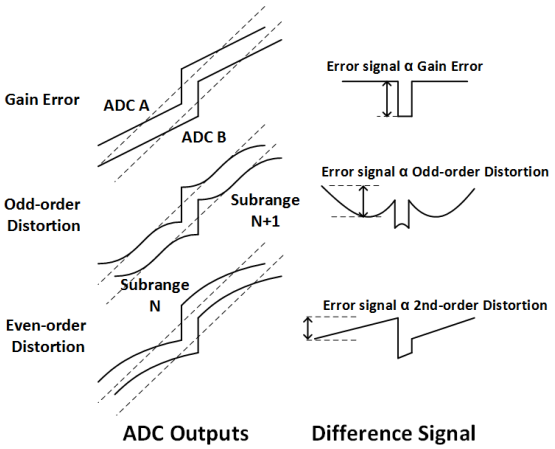

Fig. 10. Split-ADC calibration of gain and distortion errors.

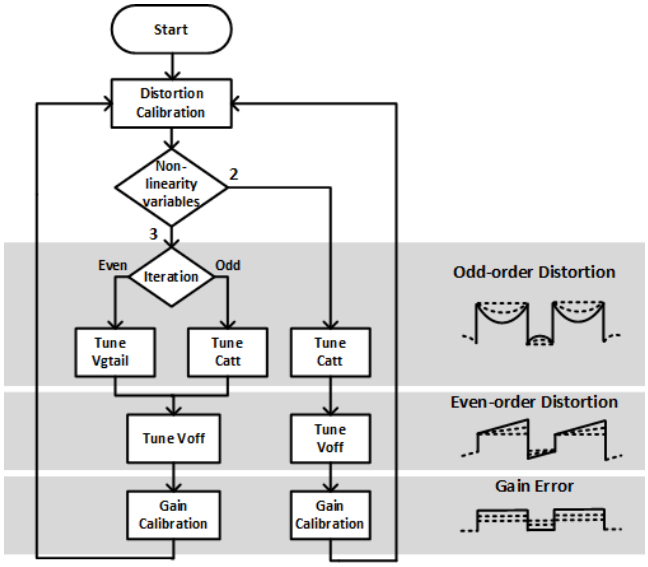

Fig. 11. Stage calibration flowchart.

Fig. 11 represents the calibration procedure followed for stages 1 and 2. To test the efficacy of the linearization parameters, the non-linearity calibration algorithm was designed with two different flows that swept 1) only the capacitive attenuation C_{att} and tail offset V_{os}, or 2) all three variables. While the former provides a simpler calibration algorithm, the latter allows a greater control over the tail current. By sweeping all three variables, the tail transistors can be tuned sufficiently to better approximate the optimum tail current characteristic, leading to a much better linearization. Since both C_{att} and V_{gtail} affect the odd-order distortion, they are adjusted in separate iterations. The non-orthogonalities between nonlinearity and gain calibration are resolved by running them over multiple iterations as discussed in [20].

The artifacts shown in Fig. 10 correspond to a difference of two completely identical ADCs. However, in reality, these two ADCs would not be identical and there will always be a certain mismatch between these two ADCs. Since this design utilizes open-loop residue amplifiers, this mismatch will be even more pronounced. There are several techniques which deal with gain mismatch between the two half-ADCs [19], [20] with relatively less additional complexity. However, the mismatch between the distortion components presents much more

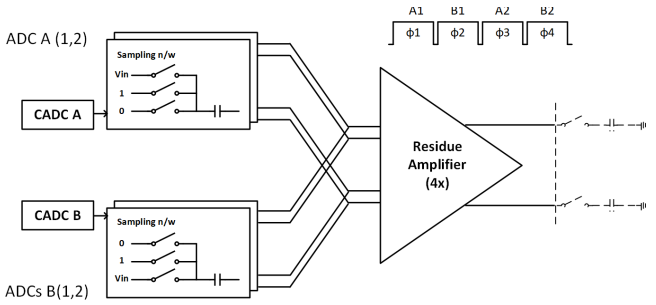

Fig. 12. Split-ADC MDAC architecture with 2× interleaving.

difficult obstacles. The most significant issue is that the mismatch between the 3rd-order distortions in the two half-ADCs also results in an even-order distortion, which also produces a linear slope in the difference signal. Hence, this half-ADC mismatch would directly interfere with the detection of even-order distortion coming from the amplifier. This makes it imperative to minimize the mismatch between the two half-ADCs.

B. MDAC

Fig. 12 shows the split-ADC MDAC architecture. In order to reduce the mismatch between the two half-ADCs, the residue amplifier is shared between them. To still realize the split-ADC technique, the offset is added over two separate clock phases. This "split-ADC over time" technique is similar to the perturbation-based method shown in [26]. However, rest of the ADC hardware—coarse ADCs (CADCs), capacitive DACs (cap-DACs), and other miscellaneous logicis physically split into two. It should be noted that as there is no charge redistribution, once the input signal has been sampled at stage 1 sampling cap, that charge remains on the cap until it is reset. This means that, theoretically, the same cap can be used again for the amplification phase of the other half-ADC, resulting in significant area savings. However, due to charge sharing between the sampling cap and the input parasitic cap of the amplifier, the latter half-ADC will always see a smaller input swing, creating a gain mismatch between the half-ADCs. Hence, separate sampling caps were used for the two half-ADCs.

The ADC timing scheme to implement this offset addition over time is shown in Fig. 13. In order to avoid using idle periods for the residue amplifier, the ADC sampling speed is doubled by using two time-interleaved lanes with a single residue amplifier shared between them. This also allows the ADC to be implemented with an even-phase (four-phase) clocking scheme instead of an odd-phase (three-phase) scheme. Two interleaved sampling networks are used for each half-ADC stage while the CADCs, operating at twice the speed, are also shared between the two lanes. Sharing the CADCs and, more importantly, the residue amplifier between the ADC lanes helps in significantly reducing the interleaving errors.

While the stage 1 sampling networks for half-ADCs A and B sample together, in order to share the residue amplifier, the residue of half-ADC B has to wait one clock cycle. This asymmetrical clocking is necessary only in stage 1, as that extra clock cycle delay creates the required latency between split-ADCs A and B residues for the backend stages.

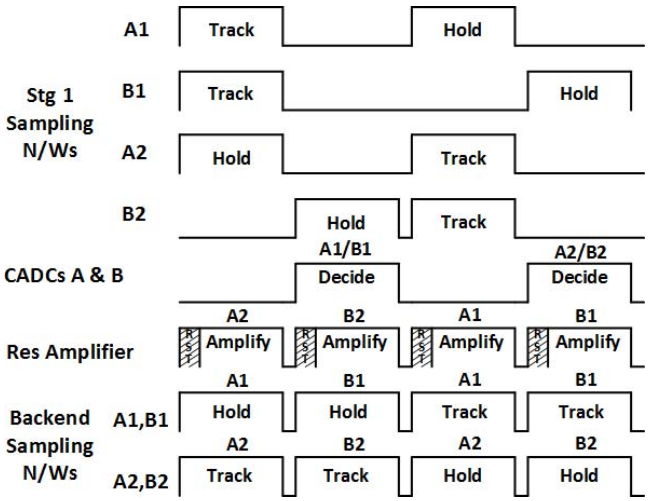

Fig. 13. ADC timing scheme.

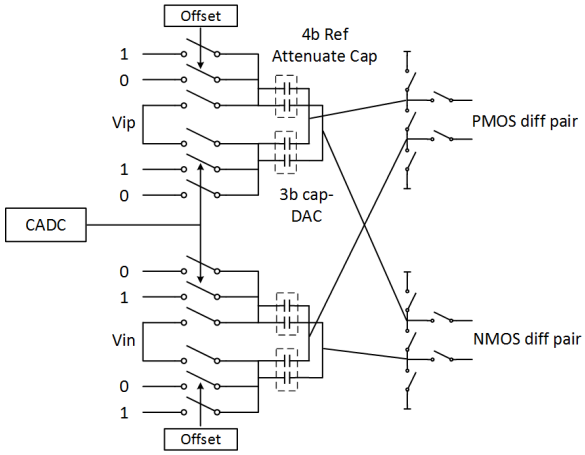

Fig. 14. Stage 1 CDAC.

Due to the latency of one extra clock cycle between the CADC decision and residue amplification, this timing scheme allows an entire clock cycle for the CADCs to make a decision.

This eases the speed requirements from the comparators, allowing for their optimization for low power. A simple strong-arm latch connected to the input through a differential pair was utilized in this design.

Due to the susceptibility of the integration-based amplifier toward memory effects, all the caps and differential nodes within the amplifier need to be reset using switches. This is performed during a reset pulse to purge all previous signal content before the amplification phase begins. This reset is also used to establish the bias for all the differential pair and tail transistor inputs. This allows the use of differential sampling [12] to mitigate the propagation of CM variations between stages.

The cap-DAC network is shown in Fig. 14. The sampling paths for the PMOS- and NMOS-side of the amplifier are entirely separated to allow independent biasing points. The MDACs and the CADCs are designed with 1 V and ground as reference voltages with the help of reference attenuation capacitors. These are part of the sampling cap, but unlike the 3-bit cap-DAC, they are switched based on a static code.

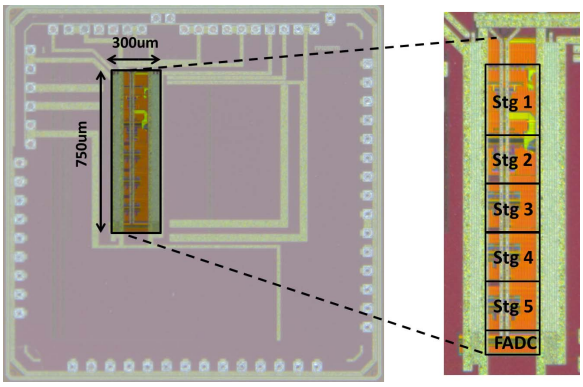

Fig. 15. Chip micrograph.

The attenuation capacitors are implemented as 4-bit thermometer cap-DACs, and can be programmed to introduce the offset required for split-ADC calibration. This offset cap-DAC is only included in the first pipeline stage as it is sufficient to introduce the offset in only the first stage of the ADC.

As the open-loop integrating amplifier has an inherently low bandwidth, the bandwidth requirements from the sampling networks of stages 2–5 and the fine ADC (FADC) are relaxed. Hence, their sampling switches no longer need to be low-ohmic, and can be scaled down accordingly. This leads to power and area reduction in the switching and clock distribution networks. As for the switch linearity requirements, they are most stringent in the first stage, and reduce by 2 bits after every stage. Hence, clock bootstrapping was used in the first stage, while simple transmission gates were utilized for the remaining stages.

For the 4-bit FADC, capacitive interpolation was used to generate the references. Since there is no over range present in the FADC, the comparator offset needs to be low. This was accomplished by using auto zeroed preamplifiers to reduce the 3σ offset from 42 to 13mV.

V. Measurement Results

The prototype ADC was implemented in 28-nm 1-V CMOS process and occupied an overall area of 0.22 mm^2, as shown in Fig. 15. This includes the bias, clock tree, output digital interface, and an input digital test interface. The on-chip circuits for amplifier linearization parameters occupy around 2% of the total area. The reference voltages use off-chip decoupling caps and are provided to the ADC through separate pads. The ADC digital outputs are subsampled by an output digital interface, and then imported into MATLAB for error detection. Based on the detected error signal, the calibration loop sets the configuration bits for the respective analog correction parameter using the input digital test interface. By running the calibration iteratively as described in [20], the overall ADC calibration reaches convergence in less than 100-K samples while running completely in background.

Sampling at 280 MS/s, the ADC dissipates an overall power of 13 mW from a 1-V supply. Out of this, 6 mW is attributed to clocking circuits, 1 mW for the reference bias and 2 mW for the reference voltages. The 4 mW is drawn from the analog supply, which includes the stage amplifiers, comparators, decoders, and other digital logic. Simulations indicate that majority of that power is spent on logic, as the amplifiers are extremely low power and consume less than 0.4 mW in total.

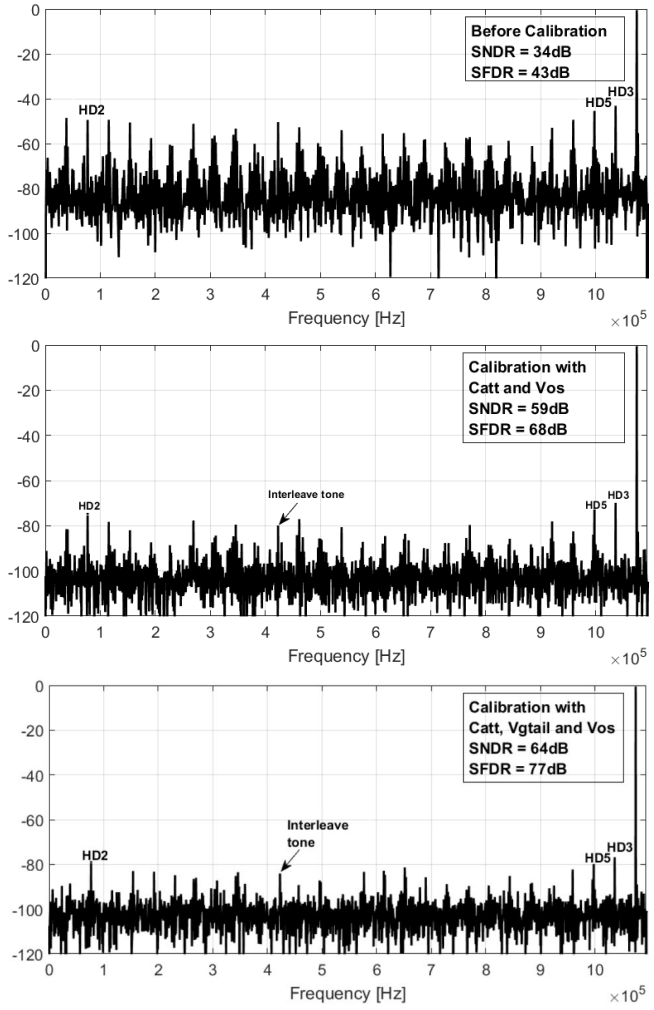

Fig. 16. ADC spectrum before and after calibration.

Since the amplifier non-linearity is corrected in analog domain, the error correction part of the calibration consumes negligible power. And due to the fast convergence speed of the split-ADC calibration, the error detection can be run at a lower clock speed to minimize its impact on the overall ADC power consumption.

Fig. 16 shows the ADC output spectrum (after subsampling by a ratio of 129) before and after calibration (with two/three linearization parameters) for an input frequency close to 137.5 MHz and an input swing of 1.1 V_{ppdiff}. The remaining 8% headroom is reserved for the addition of calibration offset. This offset can be optimized and reduced once the calibration has converged. After gain and non-linearity calibration with two linearization parameters, the signal-to-noise + distortion ratio (SNDR) is improved by more than 25 dB. However, the overall ADC resolution is still limited by distortion, with an SFDR of 68 dB. By using all three linearization parameters, all the harmonics are suppressed to about −80-dB level, with

TABLE II
PERFORMANCE COMPARISON

		Shin, JSSC '14	Dolev VLSI '13	Oh VLSI '13	Lim JSSC '15	This work
Technology		55nm	65nm	130nm	65nm	28nm
Amplifier Topology		ZC-Based	Pulsed Bucket Brigade	Time-based Charge Pump	Ring Amplifier	Integrating Amplifier
Supply (V)		1.1	1	1.3	1.2/0.75	1
ADC FS (Vppd)		2	-	2.4	2	1.2
Fs (MHz)		200	200	70	100	280
SNDR (dB)		63.2	57.6	62.6	56.6	64
SFDR (dB)		76	82*	81*	64.7	77
Power (mW)		30.7	11.5	6.38	2.5	13
FoM	Schreier (dB)	158.3	157	161.5	159.6	164.3
	Walden (fJ/conv)	130	92.8	61.3	44.5	35.8

* at low signal frequency

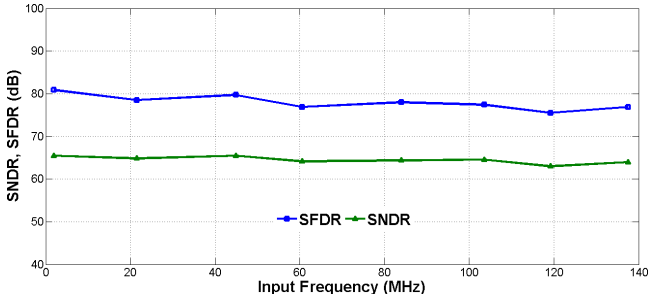

Fig. 17. ADC SNDR and SFDR versus input frequency.

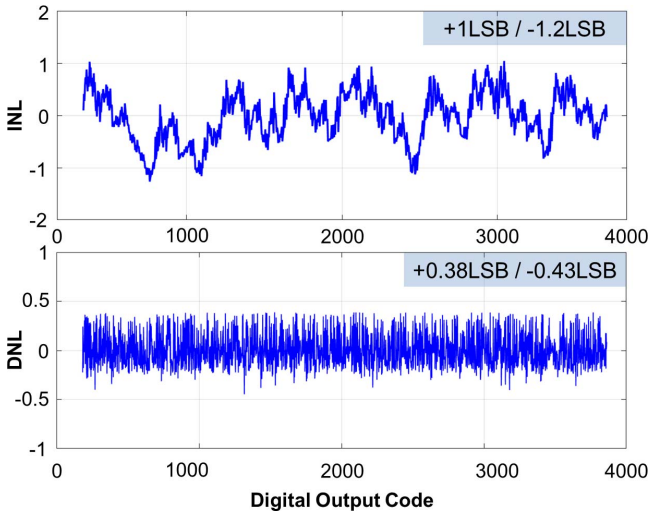

Fig. 18. ADC integral non-linearity and differential non-linearity after calibration.

HD2, 3, and 5 being the dominant tones. The two lanes show good matching and the only interleaving error visible appears to be due to lane gain mismatch. This could be due to a mismatch between the sampling cap of the two lanes. With the help of calibration, the ADC shows an overall 77-dB SFDR and 64-dB SNDR. Similar performance is achieved by the ADC over four different die samples after calibration.

One of the non-idealities limiting the ADC linearity is the cap-DAC mismatch. Since the capacitive matching is normally much higher than the amplifier distortion, the effect of cap-DAC mismatch is visible only after calibration. Although the cap-DAC mismatch can also be calibrated using split-ADC calibration as shown in [27], it is not focused on in this paper.

The ADC was tested at multiple input frequencies to check the effectiveness of amplifier linearization, and exhibits a fairly stable performance of >10.3-bit ENOB over the entire frequency range, as shown in Fig. 17. The ADC static performance is represented in the integral non-linearity (INL) and differential non-linearity (DNL) plots as shown in Fig. 18. At 12-bit level, the ADC exhibits a worst case INL of $+1/-1.2$ LSBs and a DNL of $+0.38/-0.43$ LSBs.

Table II summarizes the performance of the prototype ADC. As evident from [1], the ADC power efficiency strongly depends on its architecture. Hence, in order to conduct a fair evaluation of the proposed amplifier's performance, the prototype ADC is compared with other pipelined ADCs with similar architecture, sampling speed, and resolution.

This paper achieves a Walden figure-of-merit (FoM) of 35.8 fJ/conv and a Schreier FoM, a much more accurate measure for noise-limited ADCs, of 164.3 dB. As seen from Table II, when compared to other state-of-the-art pipelined ADCs, this paper shows an improvement of at least 3 dB in Schreier FoM. When compared to other ADC designs with integration-based dynamic amplifiers [15]–[17], this paper shows similar or better SFDR for a much higher input signal swing and frequency with the help of the proposed linearization scheme.

VI. CONCLUSION

This paper presented a 12-bit pipelined ADC employing an open-loop integration-based amplifier. The input distortion of the integrating amplifier was cancelled by using an input-driven tail current source. The behavior of the tail current source was tuned with the help of circuit parameters driven by a calibration loop to perfectly linearize the amplifier. The amplifier gain error and non-linearity were detected in background through split-ADC calibration technique. Fabricated in 28-nm 1-V digital CMOS, the ADC demonstrated an ENOB of 10.34 bit at 280 MS/s with a power consumption

of 13 mW, displaying an overall Schreier FoM of 164.3 dB. The linearization scheme allows this work to achieve excellent linearity while displaying an improvement of at least 3 dB in Schreier FoM over other comparable state-of-the-art designs

APPENDIX
POWER EFFICIENCY OF INTEGRATING VERSUS SETTLING AMPLIFIERS

The gain for an integrating amplifier is expressed in (1). For the same amplification period, a conventional settling amplifier would exhibit a gain A_{set} expressed as

$$A_{\text{set}} = \text{gm}_{\text{set}} R_{\text{set}} (1 - e^{-T_a / R_{\text{set}} C_{set}}) \tag{10}$$

with gm_{set}, R_{set}, and C_{set} being the settling amplifier's transconductance, output impedance, and load capacitance, respectively. If a settling of $N\tau$ is assumed for this amplifier, then (10) can be rewritten as

$$A_{\text{set}} = \text{gm}_{\text{set}} R_{\text{set}} (1 - e^{-N}). \tag{11}$$

Comparing the two amplifiers for the same gain, (1) and (11) can be equated, resulting in a transconductance ratio of

$$\frac{\text{gm}_{\text{int}}}{\text{gm}_{\text{set}}} = \frac{1}{T_a} C_{\text{int}} R_{\text{set}} (1 - e^{-N}) = \frac{1}{N} \frac{C_{\text{int}}}{C_{\text{set}}} (1 - e^{-N}). \tag{12}$$

The ratio of C_{set} and C_{int} can be found by comparing the input-referred (single-ended) noise powers in these two cases as calculated in [10] and [28], respectively,

$$v_{n,\text{set}}^2 = \frac{kT}{A_{\text{set}} C_{\text{set}}} \frac{(1 - e^{-2N})}{(1 - e^{-N})} \tag{13}$$

$$v_{n,\text{int}}^2 = \frac{2kT}{A_{\text{int}} C_{\text{int}}}. \tag{14}$$

By equating these two expressions

$$\frac{C_{\text{int}}}{C_{\text{set}}} = 2 \frac{(1 - e^{-N})}{(1 - e^{-2N})}. \tag{15}$$

Using (12) and (15), the ratio between the two gm's can be expressed as

$$\frac{\text{gm}_{\text{set}}}{\text{gm}_{\text{int}}} = \frac{N}{2} \frac{(1 - e^{-2N})}{(1 - e^{-N})^2}. \tag{16}$$

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