A 65-nm CMOS I/Q RF Power DAC With 24- to 42-dB Third-Harmonic Cancellation and Up to 18-dB Mixed-Signal Filtering

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***Abstract*— A 700-MHz to 1.6-GHz RF power digital-to-analog converter with programmable integrated harmonic cancellation and mixed-signal filtering is presented. Harmonic cancellation is implemented by splitting the power amplifier (PA) into segments, driving different segments of the PA with phase-shifted versions of the local oscillator (LO) signals, and summing at the output. Mixed-signal filtering is realized in a similar fashion but with segments driven with delayed versions of the input data. The phase shift and data delays are reconfigurable and implemented to operate across a wide frequency range. To boost efficiency, 25% duty cycle LO signals are used. A technique to correct for IQ constellation distortion induced by these 25% duty cycle LO signals is introduced and verified in measurements. The transmitter (TX) operates at a maximum sample rate of 500 MSa/s and achieves an output power of 25.6 dBm for an output load of 100 Ω when harmonic cancellation is enabled. The TX demonstrates 24–42 dB of 3rd harmonic cancellation for continuous wave signals across a 700-MHz to 2-GHz frequency range, achieving an HD3 as low as −57 dB. The TX achieves an HD3 reduction of 33 dB and an 18-dB notch at 40-MHz offset with 20-MHz long-term evolution data.**

***Index Terms*— Active cancellation, CMOS, digital-to-analog converter (DAC), power amplifier (PA), RF, switched-capacitor PA (SCPA), wideband transmitter (TX).**

I. Introduction

DIGITAL power amplifiers (PAs) have become increasingly attractive due to their technology scalability and the ability to use them as the core of an RF digital-to-analog converter (DAC). RF DACs are attractive as they allow for digital input data to be translated directly to RF output signals [1]–[9], [17]. This direct conversion from digital to RF allows for ease in reconfiguring the transmitter (TX) to meet different standards. Recent work on multi-standard digital PAs [2]–[4] has demonstrated digital PAs as a viable option for flexible TXs. By making the digital PA wideband, the RF DAC can be made frequency flexible, making this a promising candidate for a reconfigurable, frequency-flexible TX. However, there are at least two major issues which must be addressed before this becomes a practical and efficient solution: harmonic emissions and quantization noise.

Fundamentally, digital PAs, which operate as switching PAs, generate strong harmonic content. Digital PAs generate a square wave, either in voltage or current, which is then filtered with an output network. The power of each harmonic attenuates with $1/n^2$ for a square wave, where n is the harmonic number. This means that without additional filtering, the 3rd harmonic is only 9.5 dB lower than the fundamental in power. Typically, these harmonics are suppressed using a narrowband, high-order fixed filter. A reconfigurable TX would require a large bank of these filters, which would be costly and add additional loss from the switch network. Due to this, an integrated and reconfigurable solution is desirable, in conjunction with a wideband output network.

Additionally, as is intrinsically the case with all DACs, an RF DAC generates quantization noise. This can cause issues with coexistence in frequency division duplex systems, as a nearby receiver (RX) can be desensitized by this quantization noise. In the long-term evolution (LTE) standard for example, an RX could be offset only by 40 MHz. Oversampling or adding resolution to the DAC is a commonly used technique to reduce quantization noise, but is generally costly either in power or in area. If the RX frequencies are known, selectively filtering at those frequencies may be a less costly option.

Previous art has demonstrated reconfigurable harmonic cancellation [10], [16], [17] and mixed-signal filtering [5], [6], [11], [17] schemes. Some of these works utilize similar techniques which rely on splitting the PA, driving different pieces with different versions of the input signals, and then summing at the output. This paper expands upon these techniques by combining them and extending them to make them frequency flexible. We also seek to push power levels for harmonic cancellation toward cellular levels, which are significantly higher than previously demonstrated work. These techniques will be configurable and frequency flexible as long as the input signal generation is also configurable and operates across a wide frequency range. In Section II, the cancellation techniques as well as their requirements are described in detail. In Section III, chip implementation details are discussed, with a focus on the PA arrays, local oscillator (LO) generation chain, and data delay generation. Section IV presents measure-

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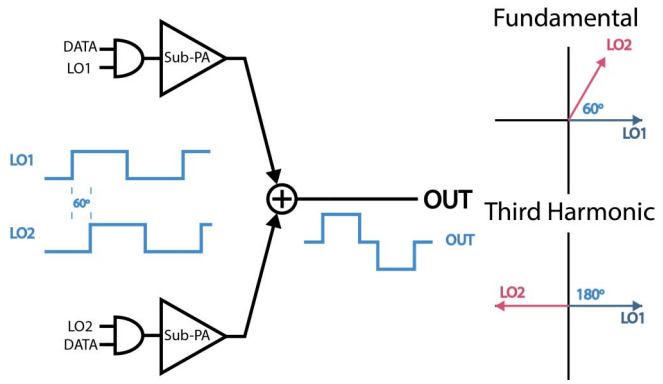

Fig. 1. Harmonic cancellation block diagram.

ment results of the TX including harmonic and mixed-signal filtering for both continuous wave (CW) and modulated signals. Finally, Section V concludes by summarizing this paper and highlighting future directions to improve these techniques.

II. Cancellation Techniques

A. Harmonic Cancellation

The harmonic cancellation technique was first demonstrated for the purposes of nulling the 2nd harmonic [10]. This paper extends this technique to a wide frequency range and significantly higher power level. Our implementation uses two sub-PAs with equal weights driven with LO signals phase shifted (nominally) by 60°, which are then summed at their outputs (Fig. 1). If the two sub-PAs are perfectly matched, the 3rd harmonic is completely cancelled, while the fundamental is reduced by 1.25 dB. In practice, cancellation is limited by matching between the two PAs and their output networks. In this implementation, any single harmonic, as well as every odd multiple of that harmonic, can be cancelled by adjusting the phase shift. This paper focuses on the 3rd harmonic as it is generally the most dominant one in a differential TX. The phase shifts are implemented to operate across a wide frequency range in order to ensure frequency flexibility.

B. Mixed-Signal Filtering

A mixed-signal technique to attenuate undesired TX output spectrum at certain frequencies was demonstrated recently [5], [6]. In this paper, we demonstrate its compatibility with harmonic cancellation. In this scheme, a delay line is used to generate delayed versions of the input data. These delayed versions are used to drive different sub-PAs which are summed at the output, implementing a programmable finite-impulse response (FIR) filter (Fig. 2). By changing the amount of delay for each sub-PA, notches can be placed at specific frequencies relative to the center frequency. Coefficients in this scheme are limited to real, positive, and fractional values which must be multiples of the $1/N_{\mathrm{PA}}$, where N_{PA} is the number of sub-PAs. It is possible to further extend this to include negative and purely imaginary coefficients by adding extra switching circuitry, but these capabilities have not been included in this current demonstration.

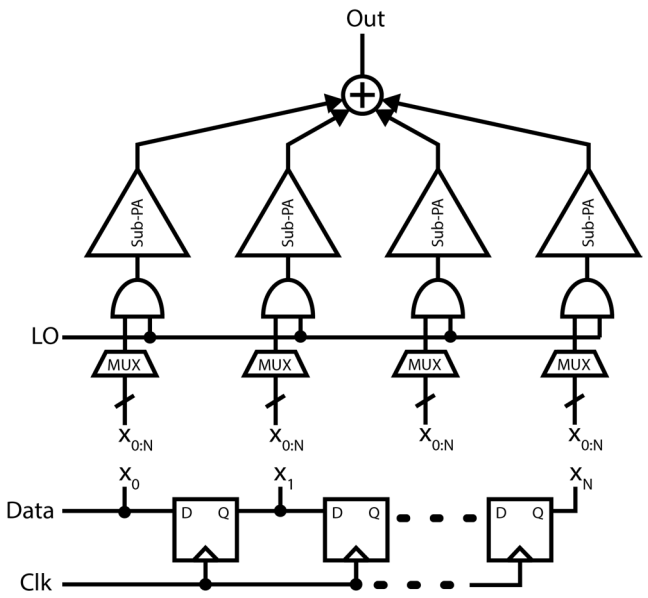

Fig. 2. Mixed-signal filtering schematic.

C. Limitations of Techniques

Both of the previously described techniques (i.e., harmonic cancellation and mixed-signal filtering) rely on summing sub-PAs with different input signals. The linearity of this summation is a critical requirement which becomes difficult at high signal levels due to increased device nonlinearity. This imposes a restriction on the PA topology, ruling out topologies such as inverse Class D which inherently have an input code-dependent output impedance, causing summation to become nonlinear. A secondary effect of varying output impedance is that the input code to output voltage transfer function becomes nonlinear. Even with predistortion to correct for this nonlinearity, the effectiveness of these techniques is limited, with one example employing a Class-E PA demonstrating only 8 dB of mixed-signal notching [6]. Thus, the topology used must inherently have a constant output impedance.

Another critical requirement for a high level of cancellation is good matching between the sub-PAs. In order to quantify this, and to examine other mismatch effects that impact the cancellation, we can analyze a linear model of two sub-PAs which are power combined at the output using a transformer (Fig. 3). In the case of harmonic cancellation, V_1 and V_2 represent the outputs of the 0° and 60° sub-PAs. For mixed-signal filtering, V_1 and V_2 represent sub-PAs implementing different filter coefficients. The use of a linear model here is reasonable as it is dictated by the linearity requirements for the PA. Each sub-PA can be modeled in this fashion using a Thévenin equivalent, grouping all impedances on the sub-PA side into a single Z_S (Fig. 4). Impedance mismatches on the secondary side of the transformer which come from the output network (transformer, board, chip pads, etc.) are modeled with shunt impedances Z_C, Z_B, and Z_T. The output voltage is given by

$$v_o = K\left[(V_1+V_2)\left(1+\frac{Z_C}{Z_T}+\frac{Z_C}{Z_B}\right)+n^2 Z_s\left(\frac{V_1(1+\varepsilon)}{Z_B}+\frac{V_2}{Z_T}\right)\right] \quad (1)$$

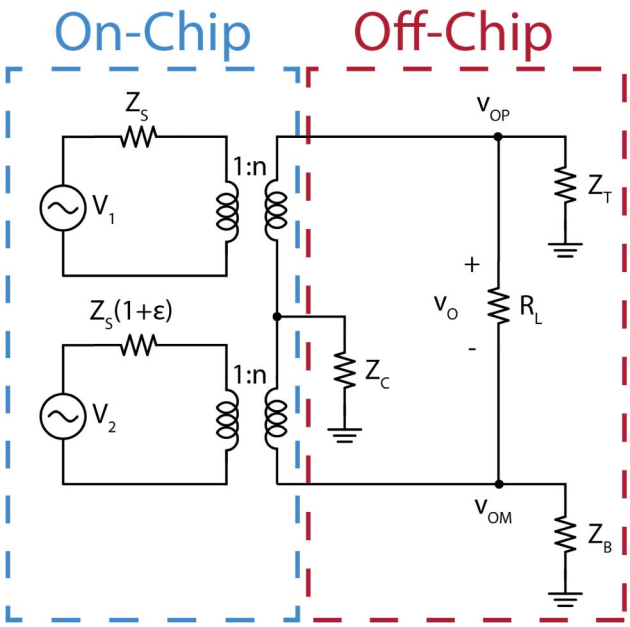

Fig. 3. Linear model of two sub-PAs summing.

where K is the coefficient that depends on the transformer turn ratio n and the various impedances. The first term demonstrates that we want $V_1 = -V_2$ for perfect cancellation. V_1 and V_2 represent the 3rd harmonic for harmonic cancellation and the fundamental at the notch frequency for mixed-signal filtering. The remaining two terms show that any mismatch in the shunt impedances Z_B and Z_T, as well as Z_S, leaves a residual term that limits our cancellation.

III. Circuit Implementation

A. Top Level

The TX is implemented using a Cartesian architecture in order to simplify the LO generation (as compared to a polar architecture) (see Fig. 5). The simplification enabled by Cartesian can be understood by examining how the mixed-signal filter output $y(t)$ is generated in both architectures

$$y(t) = \sum_{k}^{N} A(n - n_k) \sin(\omega_{LO} t + \phi(n - n_k)) \quad (2)$$

$$y(t) = \sum_{k}^{N} I(n - n_k) \cos(\omega_{LO} t) + Q(n - n_k) \sin(\omega_{LO} t) \quad (3)$$

where n is the current input code, whereas each n_k corresponds to the data delay corresponding to the kth sub-PA. For the polar architecture—whose input–output relationship is given in (2)–each sub-PA must generate its own LO signal due to using delayed versions of the phase input. Here, the number of unique LO signals is linear with the number of coefficients. In the Cartesian case—whose input–output relationship is given in (3)—the LO signals are shared between all sub-PAs. Thus, in contrast to the polar architecture, the number of LO signals is constant with respect to the number of coefficients.

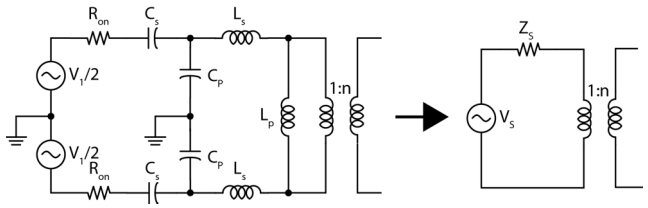

Fig. 4. In a linear model, the complex output network of a PA can be converted to a Thévenin equivalent.

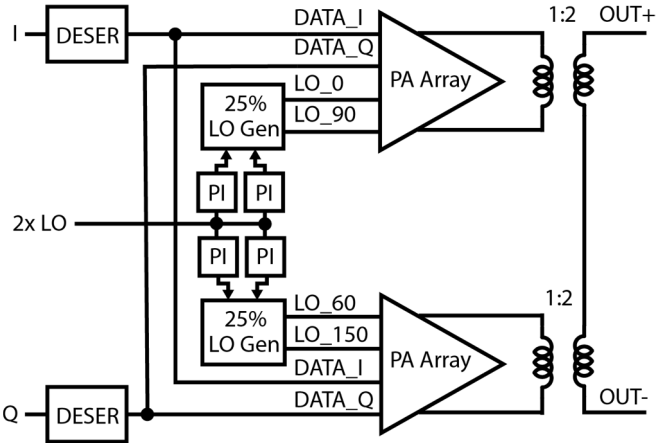

Fig. 5. Top-level schematic.

This design implements two LO phases and four mixed-signal filter coefficients, resulting in a total of eight sub-PAs. The sub-PAs are grouped into two PA arrays that are driven with the same LO phase. The two PA arrays are power combined at the output with a series-stacked 1:2 transformer to increase the maximum output power. Due to the importance of symmetry in these cancellation techniques, the PA arrays and transformer network were laid out as shown in Fig. 6, with the middle of the chip representing a line of symmetry. In each sub-PA, B_0 is the LSB cell, while B_1 through B_3 are increasing binary-weighted cells. T_0 through T_{15} are thermometer-weighted cells which switch in the order given in their name. Finally, D is a dummy cell. All components in the top-level block diagram, including the transformer, were implemented on-chip, and no off-chip passive components were used in the output network.

B. Power Amplifier Array

Each sub-PA is implemented as an 8-bit segmented DAC with four binary bits with an additional sign bit. The unit cell of this DAC is a differential switched-capacitor PA (SCPA) [12]. Each unit cell consists of a differential SCPA cell, including its series capacitors and final buffers (Fig. 7). Device stacking is used to increase the maximum output power while still ensuring the safety of the devices. The sub-PAs are laid out in two abutting PA arrays, which are shown in Fig. 8. External to these arrays, delayed versions of the I/Q data are retimed and mixed with I/Q LO signals. These drive inverter-based level shifters (LSs) which translate these signals from $0 \rightarrow V_{DD}$ to $V_{DD} \rightarrow 2V_{DD}$ for the PMOS input and

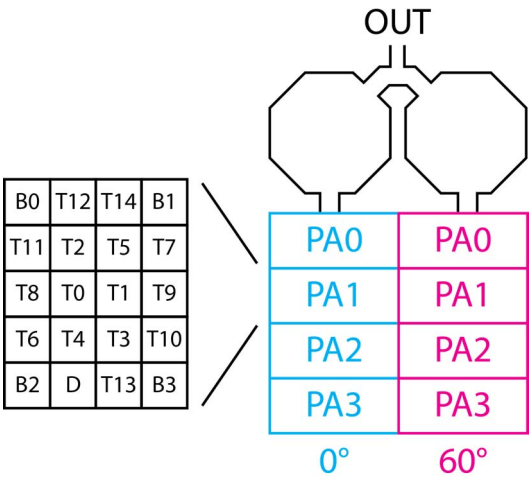

Fig. 6. Layout of sub-PA (left) and transformer and PA arrays (right).

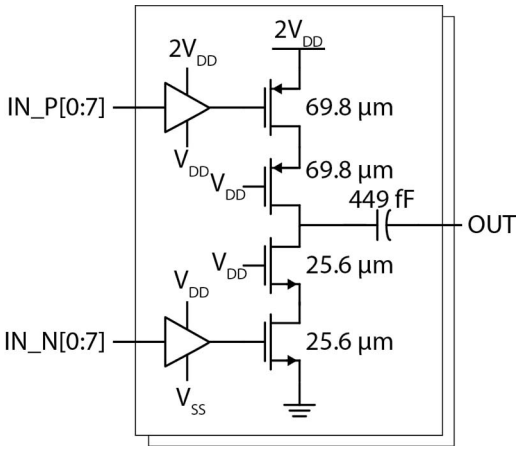

Fig. 7. Differential half of SCPA sub-PA, with transistor sizing and series capacitor value for a thermometer-weighted cell.

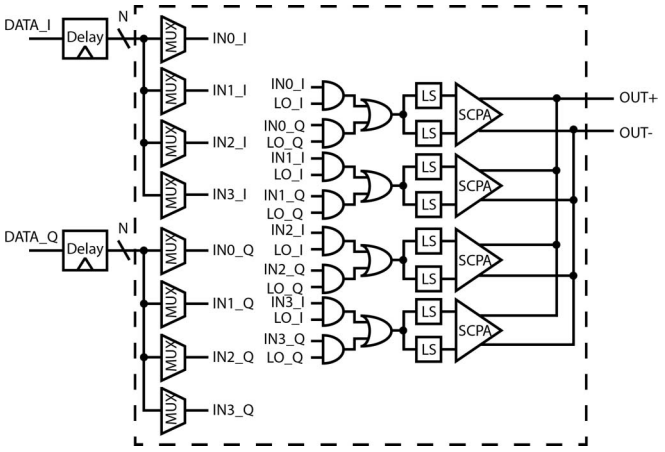

Fig. 8. PA array schematic in the dashed box.

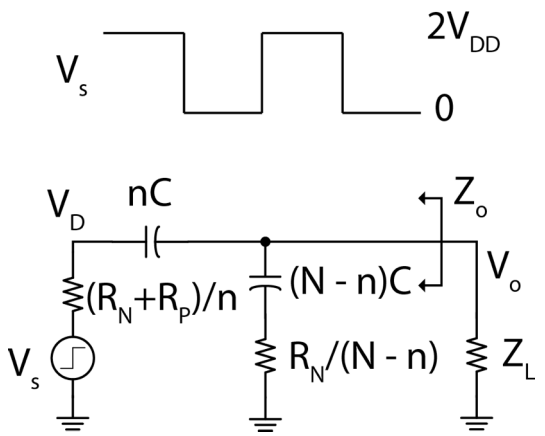

Fig. 9. Model of SCPA operating at different input codes.

$0 \rightarrow V_{DD}$ for the NMOS input. Though the NMOS LS is not strictly necessary, it is included to match the delay through both NMOS and PMOS input paths to reduce crowbar current.

The matching requirements drove the layout of the PA to be a regular array of unit cells. Due to this regularity, we generated the layout of the PA with custom layout generator scripts using the Berkeley analog generator (BAG) framework [13] (built upon Synopsis PyCell [14]), which has many features which aid regular, hierarchical layouts. In contrast to synthesis tools, the author of the BAG layout generator must specify exactly where to draw individual layout elements such as wires, vias, and transistors. The generator can be written to generate layouts given a variety of physical parameters provided by the user, such as the number of fingers per device and width of supply rails. One generator creates the differential unit cell, while another generator instantiates each unit cell with the correct cell types (thermometer, binary, and dummy), and places them in an array to form the overall PA.

The SCPA topology was chosen due to the linearity requirement of the cancellation techniques. If the pull-up and pull-down resistances are matched, the SCPA has a constant output impedance, regardless of input code. This characteristic is demonstrated by analyzing the linear model in Fig. 9, where R_N is the pull-down resistance, and R_P is the pull-up resistance. From (4), it is clear that there is no dependence of the output impedance on input code n if $R_N = R_P$. In practice, the linearity of this summation is limited by nonlinearity in device output impedance. Increasing the input code increases the output power and the current through the transistors. This increases the swing on the drain of NMOS and PMOS stacks, increasing nonlinearity in the devices as the output impedance varies more across each period. Thus, we can model R, C as having a dependence on the input code n. This code-dependent output impedance can limit harmonic cancellation. However, simulations indicate that this is not the primary limiting factor in the harmonic cancellation

$$Z_o = \frac{\left(\frac{R_N+R_P}{2} + \frac{1}{sC}\right)\left(R_N + \frac{1}{sC}\right)}{N\left(\frac{R_N+R_P}{2} + \frac{1}{sC}\right) + \frac{n}{2}\left(R_N - R_P\right)}. \tag{4}$$

C. Phase-Shifted LO Generation

Phase interpolators (PIs) were used for LO signal generation to enable frequency flexibility in the harmonic cancellation.

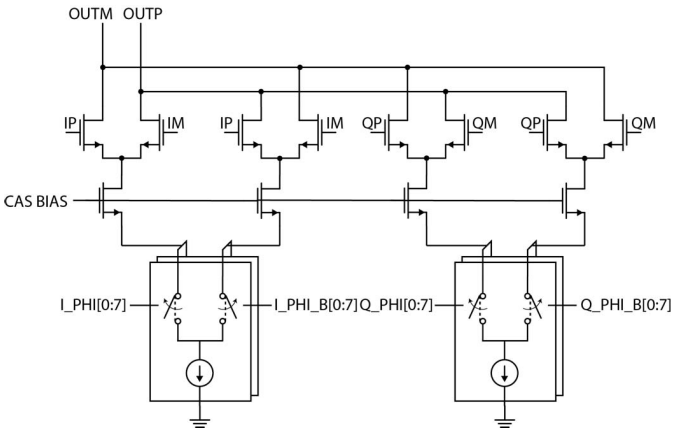

Fig. 10. Gilbert-cell-based PI.

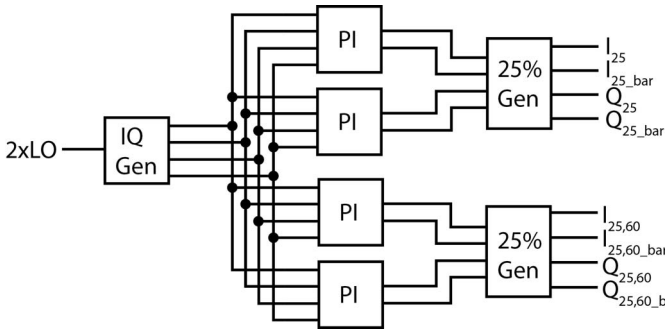

Fig. 11. LO generation network.

The PIs are Gilbert cell based [3] and operate over a wide frequency range by modifying the PI bias current (see Fig. 10). A decoder converts the 9-bit phase code into 8-bit I and Q phase codes, which are used to weigh the I/Q LO signals to generate other phases.

The LO generation path is shown in Fig. 11. The TX uses 25% duty cycle signals, which require 50% duty cycle LO signals to generate. Since this design has two LO phases, a total of four PIs are required. An external signal at $2f_{\mathrm{LO}}$ is taken from off-chip and divided down to generate I/Q LO waveforms at f_{LO}. These are fed into four 9-bit PIs, which each have a range of 360°. The PIs are organized into two pairs of PIs, each of which drive a 25% LO generator to produce 25% duty cycle versions of the I/Q LOs. The phase code of each PI is programmed through a scan chain.

This TX uses 25% duty cycle LO signals [8], [9] in order to improve the efficiency in the peak amplitude cases. Typically in digital Cartesian TXs, the I/Q combination is done at the output of the PAs [6], [7]. The 25% duty cycle I/Q LO signals are non-overlapping, which allows them to be combined at the PA input using an OR gate, as seen in Fig. 12. When data is transmitted with $I = Q$, the input to the PAs becomes a 50% duty cycle waveform. In order to visualize the efficiency benefit of using 25% duty cycle, we consider the peak power case of $I = Q = 255$. The summing out of phase lowers the output power in the 50% duty cycle case (Fig. 13). The output power of the 25% case $P_{O,25}$ is higher than the 50%

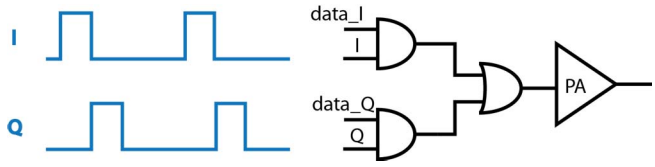

Fig. 12. Schematic for 25% duty cycle IQ combining.

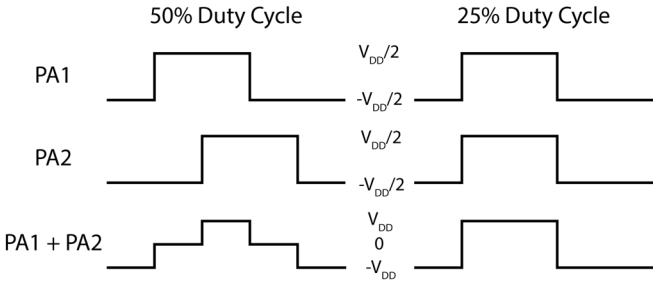

Fig. 13. Output waveforms of two SCPAs combined at the output, comparing the 50% versus 25% input duty cycle LO waveforms.

case $P_{O,50}$ by 3 dB. The drain efficiency is given by (5), with the output power divided by the sum of the output power P_o, resistive losses $P_{L,R}$, and capacitive losses $P_{L,C}$. The resistive loss is assumed to be proportional to output power through a constant k. Given that $P_{O,25} > P_{O,50}$, (6) shows that the 25% duty cycle case has a higher efficiency

$$\eta = \frac{P_O}{P_O + P_{L,R} + P_{L,C}} = \frac{P_O}{P_O + kP_O + P_{L,C}} \tag{5}$$

$$\frac{\eta_{25}}{\eta_{50}} = \frac{1 + \frac{P_C}{(1+k)P_{O,50}}}{1 + \frac{P_C}{(1+k)P_{O,25}}} > 1. \tag{6}$$

Using a 25% duty cycle LO with non-zero rise and fall times can lead to distortion in the I/Q constellation. One way to quantify this distortion is by measuring an "IQ/I ratio"—i.e., the ratio of the 50% duty cycle LO output waveform's magnitude to the magnitude of the 25% duty cycle LO output waveform. The 50% output waveform is defined as the PA output when driven by $I = Q$. Similarly, the 25% output waveform is defined as the PA output when driven with either $I = 0$ or $Q = 0$. Ideally, the IQ/I ratio is 3 dB, but the actual value can differ because the sum of the I and Q output waveform may not equal the IQ output waveform (Fig. 14). Additionally, the rise and fall time of the SCPA is input code dependent, meaning the IQ/I ratio is also input code dependent. If $R_N = R_P$, analyzing Fig. 9 gives us (7), where V_D represents the voltage at the drain of the SCPA

$$V_D = \frac{1 + s\frac{n}{N}RC}{1 + sRC}V_s. \tag{7}$$

One way to correct this distortion is to tune the duty cycle of the 25% waveforms, which allows the ratio of output power between the 50% and 25% output waveform to be controlled. In our implementation, we control this duty cycle indirectly by tuning the duty cycle of the 25% LO signals that drive the sub-PAs. This is simpler than controlling the output waveform duty cycle, and avoids duty cycle mismatch between unit elements.

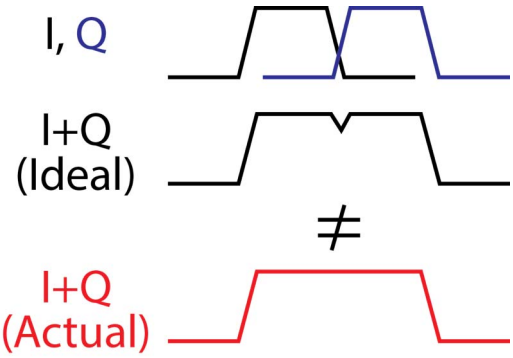

Fig. 14. Differences in 50% output waveform and sum of 25% output waveforms.

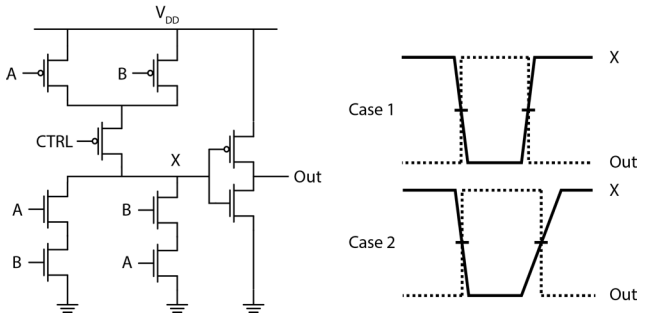

Fig. 15. Duty cycle control circuitry for 25% duty cycle LO signals, with X node and idealized output given for different values of CTRL.

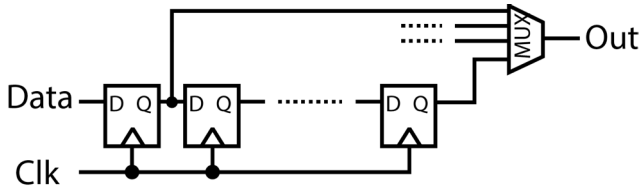

Fig. 16. Data delay line schematic.

This duty cycle control was implemented as a part of the 25% LO generation circuitry (Fig. 15). The rising edge of the first stage is sped up or slowed down based on the CTRL signal, which is set through a scan chain, changing the switching point of the rising edge and duty cycle of the overall waveform. This edge is then fed through an inverter to return it to a fast edge rate. The duty cycle correction was designed with a wide enough tuning range to correct for variation due to process corners.

D. Delay Generation

The data delay line is implemented using a chain of flip-flops operating at the data rate (see Fig. 16), with a maximum delay of 25 clock periods. This allows for a notch to be placed at an offset of as close as $f_s/50$ from the center frequency, where f_s is the sample rate. This implementation was chosen due to its relative simplicity. Unlike an inverter-based delay line, the delay of each element depends only on the data rate as long as the flip-flops can operate at that same data rate. This delay generation remains frequency flexible as long as delay line operates at the desired f_s.

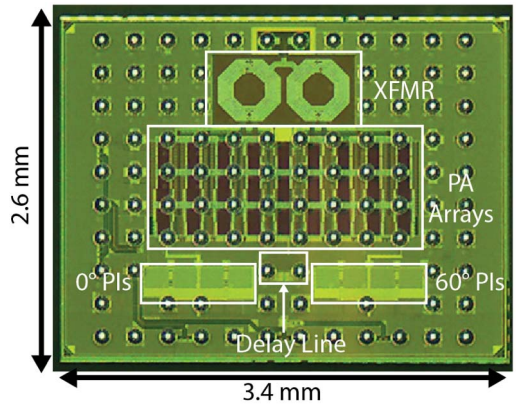

Fig. 17. Chip die photograph.

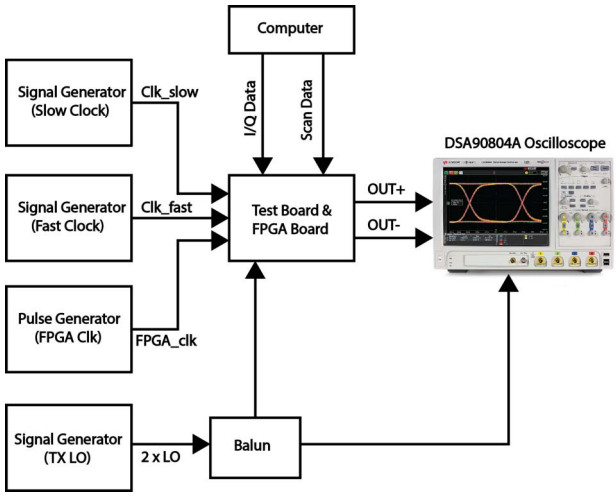

Fig. 18. Test setup.

The outputs of this delay line are fed to a set of MUXs associated with each sub-PA. The select bits of each MUX are set through a scan chain, and each MUX can be set independently of one another, allowing for full programmability of the mixed-signal FIR filter.

IV. Measurement Results

A. Prototype and Testing Setup

A prototype was fabricated in an 65-nm Taiwan Semiconductor Manufacturing Company (TSMC) general purpose process, measuring 2.6 mm × 3.4 mm, with an active area of 3.6 mm^2, including the transformer (see Fig. 17). The prototype operates with a PA supply voltage of 2.4 V and analog and digital supply voltages of 1.2 V. The TX measurements were performed at a maximum sample rate of 500 MSa/s. The die was flip chip assembled onto a test PCB, and the test setup is shown in Fig. 18. Both scan and I/Q data are sent from the computer to the field-programmable gate array (FPGA) board. The scan data is packaged and sent to the test board, while the I/Q data are written to a memory in the FPGA and continuously transmitted to the test board. The output network of the board consists of a pair of differential traces which are then connected to two subminiature version A (SMA)

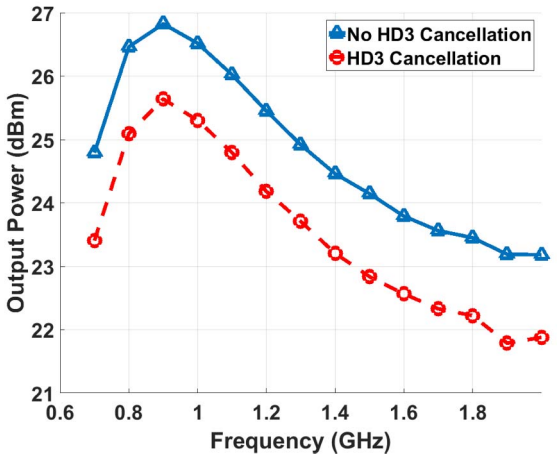

Fig. 19. Output power versus frequency.

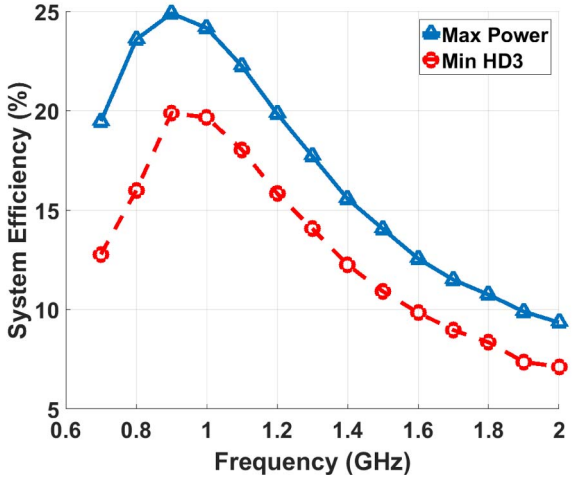

Fig. 20. System efficiency.

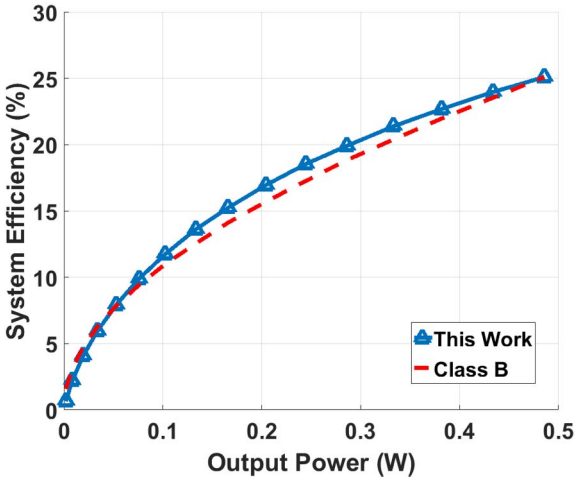

Fig. 21. System efficiency back off at 900 MHz.

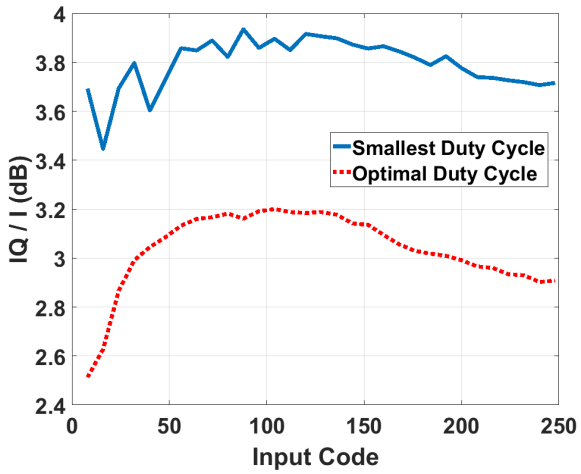

Fig. 22. $I+Q/I$ with the smallest duty cycle and optimal duty cycle setting at 900 MHz.

connectors, laid out symmetric along the center of the chip. These SMA connectors are then connected to two ports of a high-speed oscilloscope using a pair of matched cables. Each port has an impedance of 50 Ω, meaning the chip drives a differential load of 100 Ω. This setup was used in order to maintain the symmetry needed to maximize cancellation, as is analyzed in Section II. The use of two ports or an external balun can be avoided by summing the harmonic cancellation sub-PAs at their outputs, before the transformer input. The 3rd harmonic of each PA array is cancelled, limiting the effect of asymmetry on the off-chip network on the harmonic cancellation.

B. Output Power and Efficiency

Output power and efficiency were measured for both the maximum power case with no phase shift between PA arrays, and the harmonic cancellation case. The TX achieves 26.8 dBm/25.6 dBm output power in these two cases, at $f_{\mathrm{LO}} = 900$ MHz (Fig. 19). The 1.2-dB difference in output power is close to what is expected when the PA arrays are summed 60° out of phase. A system efficiency of 25%/20% (Fig. 20) and a back-off characteristic better than Class B are observed (Fig. 21). This relatively low efficiency can be partially attributed to the output network having a low loaded Q in order to implement a wideband PA.

C. 25% Duty Cycle and IQ Constellation

The "IQ/I ratio" described previously was measured in order to quantify the effectiveness of duty cycle control in correcting the IQ constellation. The measurements were conducted with the PA arrays summing in phase. IQ/I was measured by sweeping the input code with steps of eight for two different duty cycle settings. In the optimal setting, this ratio varies from 2.5 to 3.2 dB across input code (Fig. 22). The 1st quadrant of the IQ constellation was measured to better visualize the differences between the two settings. The optimal setting is visually more rectangular, which correlates with the IQ/I plots (Figs. 23 and 24). All other measurements in this section were taken with the optimal duty cycle setting.

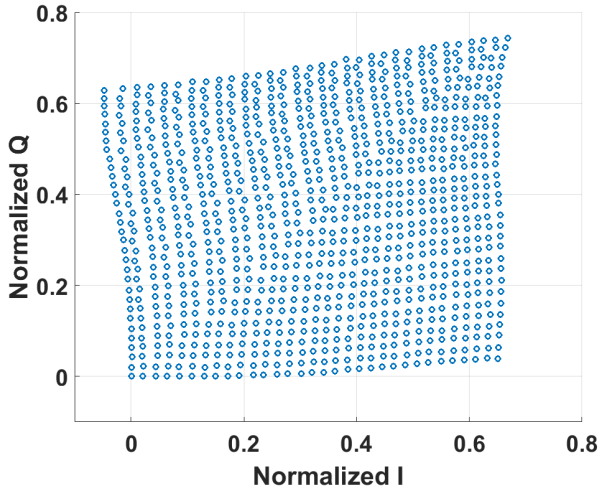

Fig. 23. IQ constellation first quadrant with the lowest duty cycle setting, at 900 MHz, with code steps of eight.

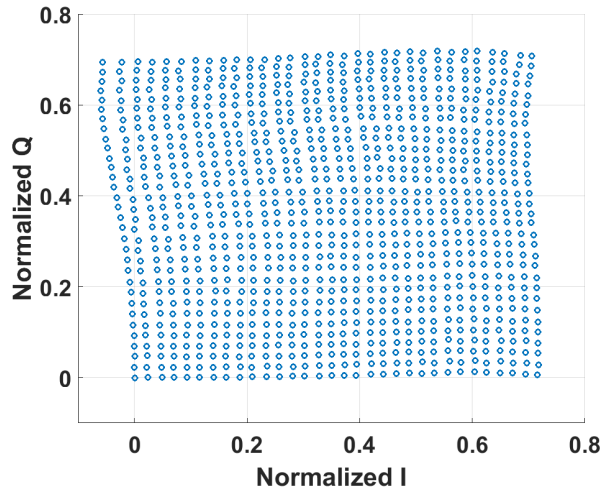

Fig. 24. IQ constellation first quadrant with the optimal duty cycle setting, at 900 MHz, with code steps of eight.

D. Harmonic Cancellation

To measure the CW HD3 cancellation, we first set $I = Q = 255$. The phase codes of one pair of PIs are fixed while the other is swept around a small range around the ideal 60°. The fundamental harmonic and the 3rd harmonic are recorded from the oscilloscope's fast Fourier transform. The HD3 cancellation is defined as the difference between the HD3 at the setting which maximizes the power and the minimum HD3. This measurement is repeated for different frequency points across the 700 MHz–2 GHz range, with steps of 100 MHz. A HD3 cancellation of 24–42 dB is measured across this frequency range (Fig. 25 and 26). The frequency dependence is likely due to the two PA arrays and their output networks having different mismatch characteristics across frequency.

CW HD3 cancellation was also measured with an external balun which transforms a differential 100 Ω to a single-ended 50 Ω, which is then connected to a spectrum analyzer

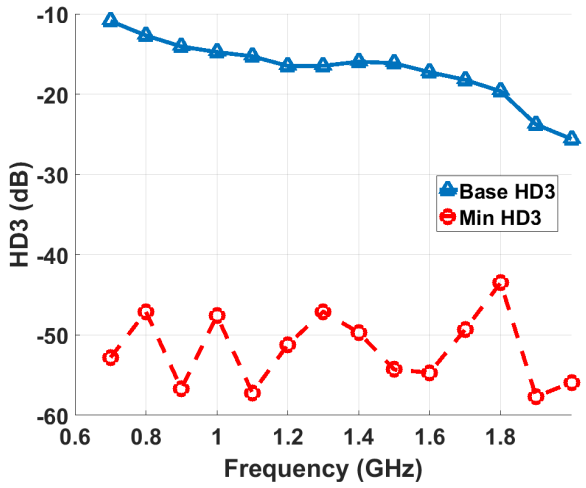

Fig. 25. CW HD3 for the maximum power and harmonic cancellation cases.

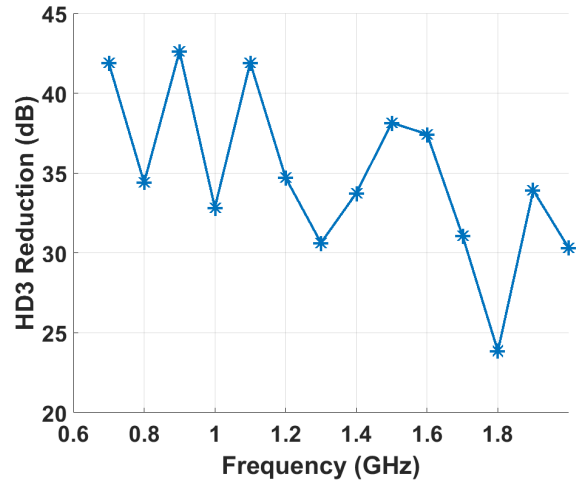

Fig. 26. CW HD3 reduction versus frequency.

(Fig. 27). The same measurement procedure as the oscilloscope setup is used. Though the shape of the reduction differs from the oscilloscope case, the maximum and minimum values are very similar across the same frequency range. This demonstrates the insensitivity of this technique to different load impedances, as long as symmetry in the output network is maintained.

E. Modulated Data Measurements

HD3 cancellation tests with modulated data were performed with 20-MHz RF bandwidth LTE data at 9-dB peak-to-average power ratio (PAPR) with a sample rate of 500 MSa/s, with $f_{LO} = 900$ MHz. The fundamental harmonic and the 3rd harmonic are reduced by 1.2 and 34 dB, respectively (Fig. 28). This gives an overall HD3 reduction of about 33 dB, which is less than the 42 dB measured in the CW case. This can be attributed to the variation of HD3 cancellation across code, due to mismatch in the DAC nonlinearity characteristics of the two PA arrays.

The same 20-MHz LTE data at 9-dB PAPR was used for the mixed-signal filtering tests, with $f_{LO} = 900$ MHz. The

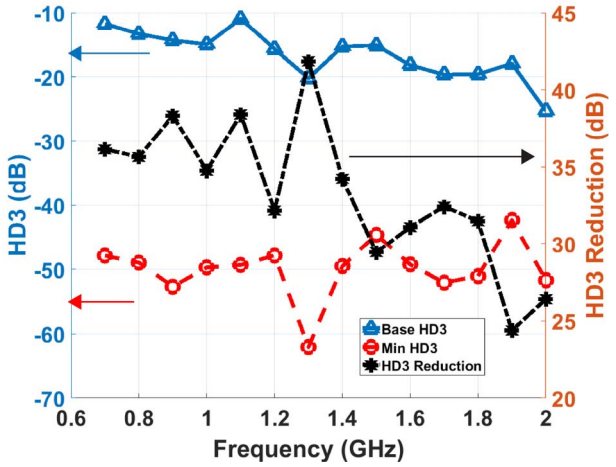

Fig. 27. CW HD3 reduction with external balun.

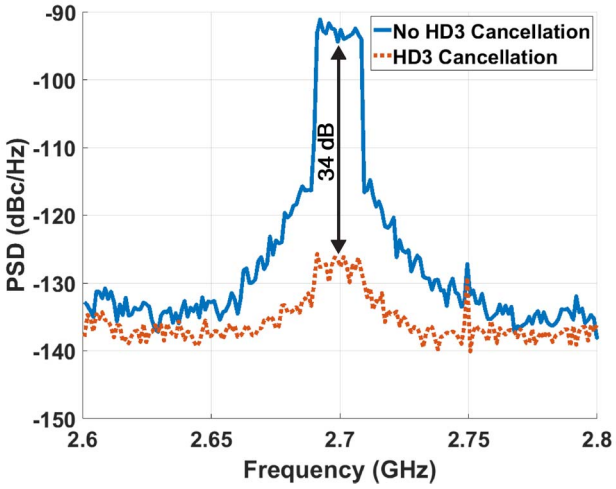

Fig. 28. Power spectral density (PSD) of 3rd harmonic with cancellation for 20-MHz 9-dB PAPR LTE signal at 900 MHz. PSD is normalized to the maximum CW output power at 900 MHz.

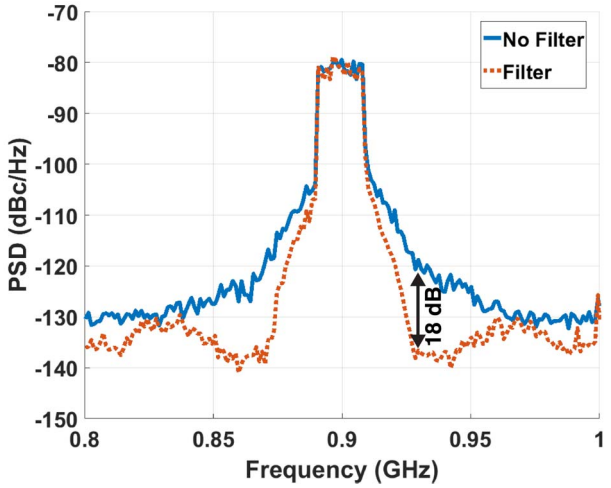

Fig. 29. PSD with mixed-signal filter notching enabled at 40-MHz offset for 20-MHz 9-dB PAPR LTE data at 900 MHz, with $n_0 = 0$, $n_1 = 6$, $n_2 = 8$, and $n_3 = 14$. PSD is normalized to the maximum CW output power at 900 MHz.

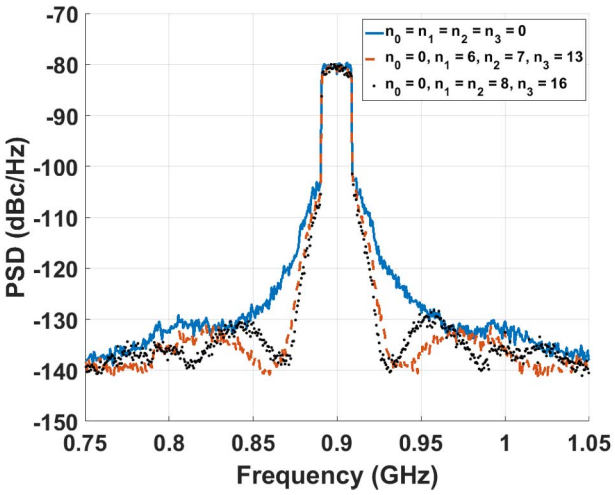

Fig. 30. PSD of different mixed-signal filter settings, with 20-MHz 9-dB PAPR LTE data.

delay lines were configured to place notches at 31.25 and 41.67 MHz to filter out a 20-MHz bandwidth at a 40-MHz offset. Delays of $n_0 = 0$, $n_1 = 6$, $n_2 = 8$, and $n_3 = 14$ were set to achieve this, where each n_k corresponds with (2). A maximum notch of 18 dB and an average reduction of 14 dB across the 20-MHz bandwidth is achieved, without the use of predistortion (Fig. 29). Additionally, the mixed-signal filter is demonstrated to be reconfigurable with different filter configurations (Fig. 30).

An error vector magnitude (EVM) measurement was also taken to quantify the linearity of the constellation. The TX achieved an EVM of 4.94% (−26.1 dB) for a 16 quadrature amplitude modulation (QAM) constellation at a symbol rate of 125 MSym/s (Fig. 31). A maximum code of 224 was used. The EVM measurement consisted of transmitting points in the 16 QAM constellation in a long, random sequence at 125 MSym/s. There was no predistortion used in this EVM measurement, highlighting the linearity of the SCPA and the effectiveness of the duty cycle correction in reducing distortion in the constellation.

Table I compares this work to prior art. This work achieves comparable harmonic cancellation with previous work utilizing digital PAs [10], [15], [16], but with >15 dB higher power than the closest previous work. Effective cancellation becomes increasingly difficult at higher output power levels due to increased device nonlinearity caused by larger output voltage swings. This paper also demonstrates harmonic cancellation with modulated data, comparable to the results achieved with CW measurements. Comparable mixed-signal filtering numbers are achieved at similar output power levels as prior art [5], [6], though this paper focused on notching a closer in frequency, and for a wider data bandwidth. Mixed-signal filtering becomes more challenging with wider data bandwidth as the effect of the dynamic nonlinearity of the PA is more pronounced, increasing the noise floor and limiting the linearity of summation.

TABLE I
COMPARISON TABLE

	[10]	[15]	[16]	[5]	[6]	This Work
Architecture	HR SCPA	Conduction Angle Calibration	33% Duty Cycle PA	Mixed-Signal Filtering	Mixed-Signal Filtering	HR and Filtering SCPA
Technology	40 nm	40 nm	40 nm	65 nm	65 nm	65 nm
Peak Power	8.9 dBm	1.2 dBm	20 dBm	30.3 dBm[1]	29.9 dBm	25.6 dBm[2]
Frequency	0.9 GHz	2.4 GHz	< 1GHz	2.2 GHz	2.4 GHz	0.7–1.6 GHz
Peak Efficiency	43%[3]	39%[3]	43%[4]	34%[4]	38.3%[4]	20%[4]
HD (CW)	HD2: -65 dB HD3: -46 dB HD4: -42 dB	HD2: -50 dB	HD3: -57.7 dB	N/A	N/A	HD3: -57 dB
HD Reduction (CW)	HD2: 48dB HD3: 17 dB HD4: 24 dB	HD2: 23 dB	N/A	N/A	N/A	HD3: 42 dB
Notch Depth @ f_{offset}	N/A	N/A	N/A	24 dB @ 140 MHz	8 dB @ 100 MHz	18 dB @ 40 MHz
Noise Floor @ f_{offset}	N/A	N/A	N/A	-149 dBc/Hz @ 140 MHz	-134 dB/Hz @ 100 MHz	-137 dBc/Hz @ 40 MHz
Modulation Bandwidth	N/A	N/A	N/A	1.4 MHz	20 MHz	20 MHz
EVM @ Sample Rate Symbol Rate	N/A	N/A	N/A	-29.2 dB[5] 560 MSa/s 20 MSym/s	-20 dB[5] 200 MSa/s 20 MSym/s	-26.1 dB[6] 125 MSa/s 125 MSym/s

Table 1. [1]23Ω load, [2]100Ω load, [3]Drain efficiency, [4]System efficiency, [5]64QAM, [6]16QAM

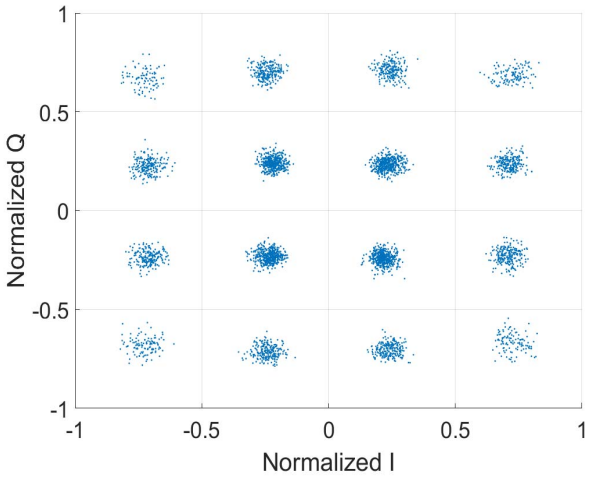

Fig. 31. EVM of −26.1 dB for 16 QAM at a data rate of 125 MS/s.

V. CONCLUSION

This paper demonstrates a wideband RF DAC with integrated harmonic cancellation and mixed-signal filtering with no external passive components in a 65-nm chip. The filtering techniques are designed to be reconfigurable and frequency flexible as to alleviate the need for an output filter. This paper demonstrates harmonic cancellation at much higher output power levels than previously demonstrated, approaching levels desired by cellular applications. Linearity of summation, critical to the effectiveness of these techniques, drove the choice of PA topology, as well as the symmetry of the PA and output network layouts. A technique to correct for IQ constellation distortion when using 25% duty cycle LO signals is proposed and demonstrated to be effective. This paper achieves a peak output power of 25.6 dBm operating at a peak sample rate of 500 MSa/s, while attaining a 3rd harmonic cancellation of 24 to 42 dB across a 700 MHz–2 GHz range. This paper also demonstrates up to 33 dB of 3rd harmonic cancellation and up to 18 dB of notching with 20-MHz bandwidth LTE data. Future work includes generating a good scheme for the harmonic cancellation with sub-PAs of non-uniform weights and expanding the mixed-signal filtering to be able to implement complex coefficients.

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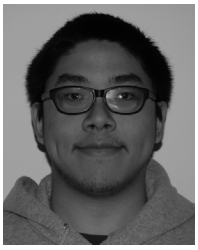

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