A Capacitively Coupled, Pseudo Return-to-Zero Input, Latched-Bias Data Receiver

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***Abstract*— A power and area efficient, capacitively coupled receiver for short links is presented. The proposed architecture enables a wide input common-mode range by utilizing on-chip ac-coupling capacitors, which avoids the use of large, off-chip capacitors or slow, rail-to-rail input stages. The small coupling capacitance and bias switches generate a pseudo return-to-zero pulse that is latched into the receiver via digital feedback. This input latching reduces the effects of baseline wander caused by unbalanced data streams without the need for encoding or scrambling. In addition, the full-scale digital feedback is used as the receiver output, enabling direct interface with standard digital cells. The architecture is implemented in a 130-nm SiGe BiCMOS and 45-nm CMOS silicon-on-insulator (SOI) technology. The 130-nm SiGe BiCMOS design achieves a peak data rate of 10 Gb/s at 5.1 mW, while a peak efficiency of 0.46 mW/Gb/s is recorded at 8 Gb/s. The 45-nm CMOS SOI design achieves a peak data rate of 30 Gb/s at 12.02 mW, with a peak efficiency of 0.24 mW/Gb/s at 25 Gb/s. Both the SiGe BiCMOS and CMOS SOI designs exhibit BERs of $<10^{-12}$ with PRBS15 data as small as 100 mV and occupy 0.012 and 0.007 mm^2, respectively, including the on-chip coupling capacitance.**

***Index Terms*— Baseline wander, BiCMOS integrated circuits, capacitive coupling, digital feedback, latch, pulse receiver.**

I. Introduction

With an increasing number of traditional analog and RF operations moving into the digital domain, the demand for high-speed data transfer in data converters, memories, and processing systems continues to grow. Furthermore, the expansion of mobile and attritable platforms imposes strict area, power, and thermal limitations, curbing their ability to achieve high data throughput. To meet throughput objectives while operating within these constraints, I/O circuitry must maximize both area and power efficiencies.

One challenge with achieving highly efficient data transfer is long and lossy channels. Data transceivers' power efficiency trend exhibits an order of magnitude decrease for every 30 dB of loss, due to primarily the equalization required [1]. Therefore, to achieve both high-speed and highly efficient data transfer, low-loss channels are essential. One solution that provides such a medium is 3-D integrated circuits (3-D-ICs). The 3-D-IC integration significantly decreases the length of I/O channels, their associated loss, and impedance discontinuities between disparate circuit technologies [2]. Packaging options such as flip chip, backside and through VIAs, microbumps, and the close proximity methods all increase the practicality of 3-D-ICs, while enabling both dc- and ac-coupled connections [2], [3]. In addition to reduced channel loss, 3-D-ICs also enable the integration of various specialized technologies into a highly compact multi-chip design [2], [3]. However, challenges with packaging dissimilar technology interfaces persist. To achieve the desired I/O density between applicable layers, a coupling scheme that alleviates packaging and common-mode range challenges are needed.

DC-coupled solutions [Fig. 1(a)] require a shared common-mode bias between transmitter and receiver that is vital

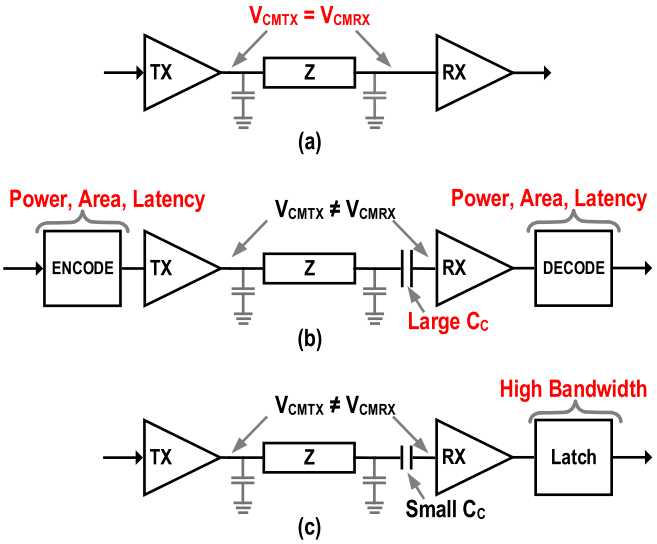

Fig. 1. Transceiver block diagrams for (a) dc-coupling, (b) large off-chip capacitive coupling, and (c) small on-chip capacitive ac-coupling.

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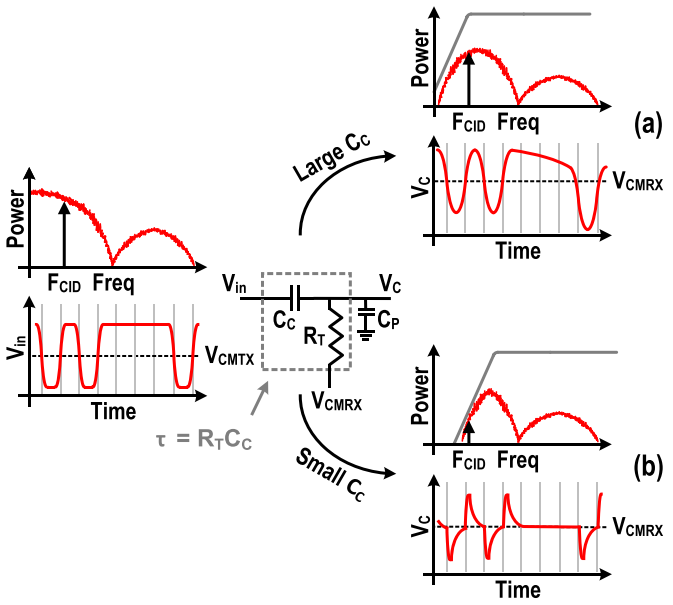

Fig. 2. Time and frequency representations of NRZ input signal. (a) Off-chip large capacitor ac-coupled signal. (b) On-chip small capacitor ac-coupled signal.

to performance. However, differences in technology biasing requirements, circuit architectures, varying ground planes, and dc channel loss can introduce an offset between the transmitter common mode and the receiver's acceptable input range. Various input-stage architectures have been proposed as solutions [4]–[8], but these topologies add devices and parasitics to the signal path, increasing power consumption, and limiting data rate.

In lieu of dc-coupling, board or package mounted capacitive ac-coupling [Fig. 1(b)] introduces a high-pass response, filtering the signal's common mode, and enabling separate biases at the transmitter and receiver [9]. The high-pass response attenuates the signal's low-frequency content, causing bit errors in arbitrary non-return-to-zero (NRZ) data streams [Fig. 2(a)]. Data encoding (e.g., 8b/10b) avoids these errors by eliminating dc-imbalanced data patterns, bounding the frequency content of the signal above the high-pass channel corner frequency. Unavoidably, these schemes increase power, area, and latency, while decreasing the effective data rate. In addition, large off-chip coupling capacitors limit I/O density, inhibit vertical integration and introduce impedance discontinuities that require complex and high power frequency equalization [9].

Alternatively, on-chip ac-coupling capacitors [Fig. 1(c)] occupy a much smaller footprint and eliminate impedance discontinuities in the board or package. Chip-to-chip capacitors can also be built more densely than dc connections in die-stacking applications [10], [11]. However, the limited achievable capacitance increases low-frequency attenuation, as shown in Fig. 2(b). This requires increased encoding overhead or the addition of hysteresis. Previous hysteresis architectures implement output crossed-coupled transistors [11], output cross-coupled inverters [12], and combined linear and non-linear path [13] schemes to achieve this required latching. Alternatively, feed-forward restore circuitry can be used to recover consecutive identical digits (CIDs) in ac-coupled data applications [14].

In this paper, we present a compact, high-speed I/O receiver architecture that addresses the presented challenges, enabling fully integrated ac-coupled chip-to-chip links. An input bias latching technique mitigates inter-symbol interference (ISI) and removes the need for encoding through the implementation of input hysteresis. In addition, the latched-biasing scheme ensures an optimal bias across process, voltage, and temperature (PVT) by employing common-mode feedback (CMFB) and a replica bias circuit. A full-scale CMOS digital output drives the input bias latching while providing a direct rail-to-rail interface for further on-chip digital processing. Together, these features enable low-latency, power-efficient, and high-speed data reception. This architecture has been successfully implemented in both a 130-nm SiGe BiCMOS technology and a 45-nm CMOS silicon-on-insulator (SOI) technology.

Section II discusses the ac-coupling of NRZ data streams. Section III introduces the proposed input latched-biasing technique, while Section IV reviews both the SiGe BiCMOS and the CMOS SOI designs. Section V details the measurement results, with concluding remarks given in Section VI.

II. AC-Coupled Data Transfer

NRZ bitstreams are wideband signals composed of a dc common mode, fundamental, and odd harmonics. With arbitrary data, the bitstream frequency varies due to the presence of CIDs [15]–[17]. These CIDs shift the averaged fundamental frequency, as described in (1), where CID represents the integer number of identical digits

$$F_{\mathrm{CID}} = \frac{\text{Bit Rate}}{2 \cdot \text{CID}}. \tag{1}$$

The occurrence of arbitrary CIDs can give rise to asymmetries between the number of 1's and 0's. The result of which is data imbalance, causing the bitstream frequency content to experience transient shifts between the data-rate fundamental (bit rate/2) and near-dc [14]. Long CIDs are of particular concern in ac-coupled data receivers as the near-dc frequencies generated are attenuated through the input network, modeled in Fig. 2 with the coupling capacitor (C_C) and termination resistance (R_T). This attenuation induces ISI and leads to baseline wander at the coupled input, which can cause deterministic jitter at the output and, when large enough, result in bit errors [18].

A. Large Off-Chip AC Coupling

With long strings of CIDs present in a data stream, the frequency content of the signal can drop below the high-pass response of the ac coupling, impacting data reception [Fig. 2(a)]. Traditionally, large off-chip capacitors are utilized to decrease the coupling corner frequency ($f_C = 1/(2\pi R_T C_C)$), enabling the reception of CIDs of finite-length. Fig. 3 models an input NRZ waveform including one CID (gray); the amplitude ($V_{\mathrm{in\_pk}}$), transition time (T_T), and bit-period (T_B) are labeled. Passing this NRZ signal through a large coupling capacitance results in a coupled input [Fig. 3 (black)] which slowly decays to its bias due to its large RC time constant ($\tau = R_T C_C$). While this slow rate of decay

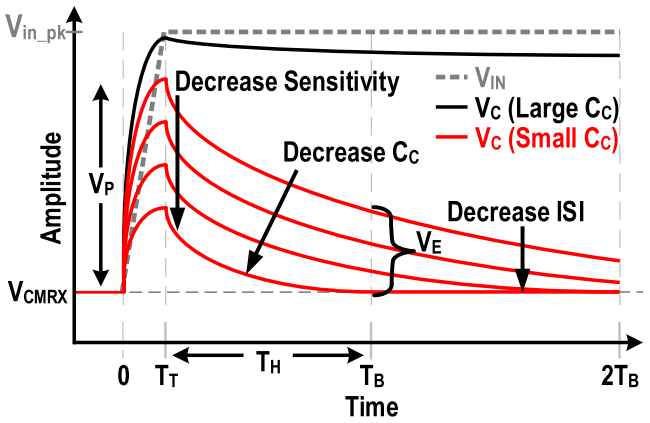

Fig. 3. Time-domain NRZ input signal and large off-chip capacitor ac-coupled signal with varying C_C values.

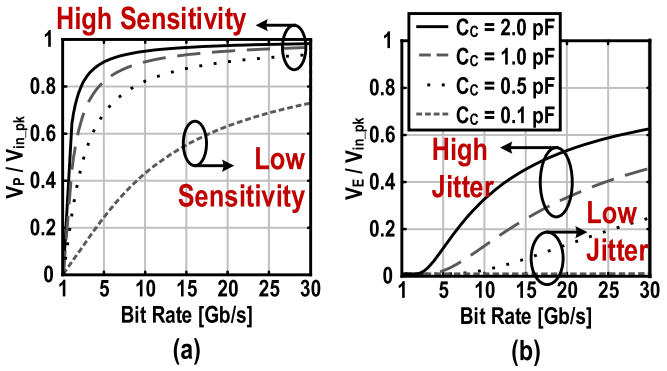

Fig. 4. Normalized receiver. (a) Peak coupled voltage, and (b) residual voltage error, with T_T set to 0.1 T_B.

enables the reception of a limited number of CIDs, the coupled signal will ultimately decay to the fixed common-mode bias voltage of the receiver's coupled node (V_{CMRX}) regardless of how large the capacitance. This reflects a departure from the intended NRZ signaling and results in various levels of ISI present during subsequent bit periods.

To minimize the impact of this ISI, encoding is used to ensure robust reception irrespective of the data. Encoding bounds the maximum number of CIDs presents in a given bitstream, therefore, ensuring a minimum F_{CID}. Then with proper capacitor sizing, the high-pass corner of the ac-coupling is placed below the minimum F_{CID}, which limits decay of the coupled signal and the associated ISI. In this way, there is a direct tradeoff between encoding overhead (power, area, latency, and effective data rate) and capacitor size with a smaller capacitor typically requiring an increased encoding burden.

B. Small On-Chip AC Coupling

By moving the coupling capacitor on-chip, the density and impedance challenges presented by off-chip capacitive coupling are avoided. However, capacitor-sizing limitations decrease the coupled node's time constant and transform the NRZ transitions into narrow bi-polar return-to-zero (RZ) pulses (i.e., return to a fixed common-mode bias, V_{CMRX}). Furthermore, no pulse is generated during CIDs due to the lack of NRZ transitions. This is shown in Fig. 3 by the coupled responses (red) of four different small, on-chip capacitors. Although these narrow pulses do not allow CIDs to be recovered, the number of bits affected by ISI is decreased. A voltage error (V_E) is generated whenever the coupled pulse width exceeds that of one T_B and can be viewed on a bit-by-bit basis as the difference between V_{CMRX} and the node potential at time T_B.

Thorough modeling of the input network and waveform is needed to maximize the coupled amplitude (V_P) while also minimizing the value of V_E for a given T_B. The transfer function of the ac-coupling input network showing in Fig. 2 is approximated by (2), with C_P representing the receiver parasitic capacitance

$$\frac{V_C}{V_{\mathrm{IN}}} = \frac{sR_TC_C}{sR_T(C_C+C_P)+1}. \tag{2}$$

The receiver input-coupled signal (V_C) is derived by passing the NRZ input through the coupling network described in (2). Ignoring C_P, the resulting signal is given by (3), with m being the slope of the input transition ($m = V_{\mathrm{in\_pk}}/T_T$)

$$V_C(t) = u(t)\cdot m\tau\left(1-e^{\frac{-t}{\tau}}\right) - u(t-T_T)\cdot m\tau\left(1-e^{\frac{-(t-T_T)}{\tau}}\right). \tag{3}$$

The two timeframes of this response correspond to the transition response ($0 < t < T_T$) and the subsequent decay time ($T_T < t$). The hold time (T_H) of each bit period is equal to $T_B - T_T$. Evaluating (3) at time T_T results in the coupled amplitude V_P. Note that the value of V_P directly relates to C_C. Fig. 4(a) shows this amplitude, normalized to the input amplitude ($V_P/V_{\mathrm{in\_pk}}$), as a function of the data rate for several values of C_C, assuming $R_T = 50\ \Omega$ along with a T_T of 0.1 T_B. This amplitude, along with the gain of the receiver, set the sensitivity of the design, where increasing values of C_C and gain contribute to more sensitivity. In addition, the magnitude of V_E is found by evaluating (3) at time T_B. Fig. 4(b) depicts the effects of bit rate on V_E normalized to the input amplitude ($V_E/V_{\mathrm{in\_pk}}$) with varying values of C_C. This error is translated into output deterministic jitter by gain in the receiver with decreasing values of C_C contributing less jitter.

As demonstrated by Fig. 4(a) and (b), when C_C is increased, both V_P and the V_E rise, increasing the receiver sensitivity at the expense of ISI jitter. Alternately, decreasing C_C decreases the receiver sensitivity while improving ISI performance. This design tradeoff is further exacerbated at higher speeds where a shrinking T_B increases V_E, which ultimately limits the achievable data rate of a given capacitance value due to the accumulation of voltage error and the resulting ISI.

Although a small C_C will generate a bi-polar RZ pulse train with minimal ISI [Fig. 2(b)], the lack of a coupled pulse during CIDs will result in bit errors. Without a transition in the data during CIDs, the coupled node will decay rapidly to V_{CMRX} and will result in indeterminate input states inside the receiver's sensitivity region. The level of data encoding can

be increased in order to generate a pulse for every data value; however, this excessively increases encoding overhead.

Alternatively, the required encoding can be eliminated by adding hysteresis to the receiver, creating a latching effect of previous bit's value. This can extend the receiver's output low cutoff bandwidth below the input high-pass corner down to dc, resulting in the ability to hold the correct output state for indefinite CIDs. However, the inclusion of cross-coupled output-latching techniques [11], [12] limits the achievable high-cutoff bandwidth due to capacitive output loading, while the combination of linear and non-linear paths [13] increases the receiver's power and area consumption. Furthermore, output and combination latching schemes ignore jitter contributions at the input nodes, which can also set a limit on achievable data rates. The addition of a parallel dc path to the coupling capacitor enables a feed-forward restore method [14] of low-frequency content with minimal bandwidth implications. However, the dc connection limits acceptable input common-mode range, hence reversing the common-mode benefits of ac-coupling. To leverage the large acceptable input common-mode range provided by ac-coupling, dc paths should be avoided. Yet the latching scheme must not ignore the input node nor overly load the receiver in order to achieve high speed, low-jitter error free recovery of arbitrary data, and avoid any encoding overhead.

III. Proposed Input Latched-Bias Receiver

As noted earlier, previous works have utilized hysteresis to recover NRZ data streams from bi-polar pulse trains. In the proposed latching scheme [Fig. 5(a)], however, dynamic digitally controlled input bias switches are used to implement hysteresis at the coupled input rather than at the output of the receiver. By leveraging a truly capacitive input, this technique supports a wide acceptable input common-mode range, while the latched input biases maximize sensitivity, mitigate ISI, and accommodate an indefinite number of CIDs without encoding. Both the coupling and latching are implemented on-chip to minimize area, power consumption, and impedance discontinuities.

A. Input Bias Latching

With small on-chip coupling capacitances generating pulse widths constrained by T_B, each bit-period can be considered independently. This simplifies the relationship between two adjacent bits, as only two scenarios exist; they are either equal ($b_0 = b_1$) or unequal ($b_0 \neq b_1$). Equal adjacent bits (i.e., CIDs) lack a transition and can be viewed as a hold of the previous value, whereas unequal adjacent bits include a transition whose frequency content is determined by the transition slope m. Thus, all the information within a bitstream is captured within the bit transition polarity and timing [10], [11], [18]. During a transitional bit period, high-frequency energy is coupled into the receiver. If V_P of the coupled signal surpasses the receiver sensitivity threshold, the amplified, and subsequently buffered, digital output signal (BIT,$\overline{\text{BIT}}$) toggles. Alternately, during a static bit period, no energy is coupled, therefore, not toggling the receiver output.

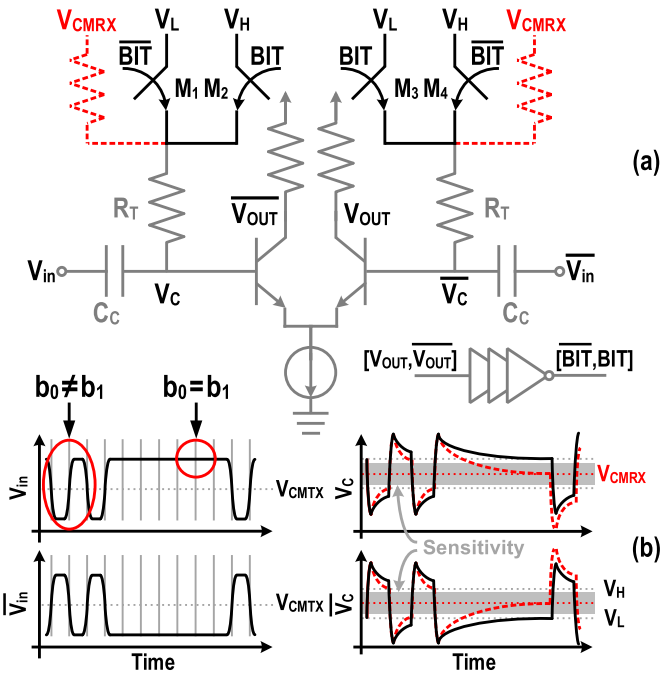

Fig. 5. (a) Capacitively coupled differential pair with fixed (red) or latched (black) bias schemes. (b) Waveforms data of the input ($V_{\text{in}}, \overline{V}_{\text{in}}$) and capacitive-coupled nodes ($V_C, \overline{V}_C$) in the presence of a toggling data stream and CIDs.

With a conventional fixed common-mode bias in the differential receiver amplifier [Fig. 5(a) (red)], the input RZ pulse returns to V_{CMRX} after the input toggles. Both input nodes ($V_C, \overline{V_C}$) enter the sensitivity region (gray), rendering subsequent data recovery impossible [Fig. 5(b)]. In the proposed latched-biasing scheme [Fig. 5(a) (black)], separate bias voltages (V_H, V_L) are selectively applied to the differential input via two pairs of switches [M1–M4 in Fig. 5(a)]. These separate bias conditions maintain an offset between the differential inputs, ensuring that each decay to distinct potentials outside of the sensitivity region of the amplifier [Fig. 5(b)]. This latching scheme generates a pseudo RZ (PRZ) pulse that serves as an intrinsic 1-bit memory of the previous bit value. The bias offset, equal to the difference between the two biases ($\Delta V = V_H - V_L$), and size of C_C set the hysteresis level of the receiver.

Selection of the valid biasing condition for each of the differential inputs is done based on the output of the receiver (BIT, $\overline{\text{BIT}}$). This forms a feedback loop, which introduces a feedback delay (T_{FB}) equal to the time between an incoming bit transition and application of a new bias state at the coupled input. This results in a self-timed, high-speed, toggled bias latching receiver that accurately recovers an indefinite string of CIDs.

B. PRZ Waveform Characteristics

The RZ pulse of a fixed bias receiver and the PRZ pulse of the proposed design share fundamental characteristics. The addition of bias switches has minimal impact on the time constant of the coupled node ($\tau = R_T C_C$). Therefore, assuming the same input signal and input network, the RZ and PRZ pulses have equal peak amplitudes and decay rates, as shown

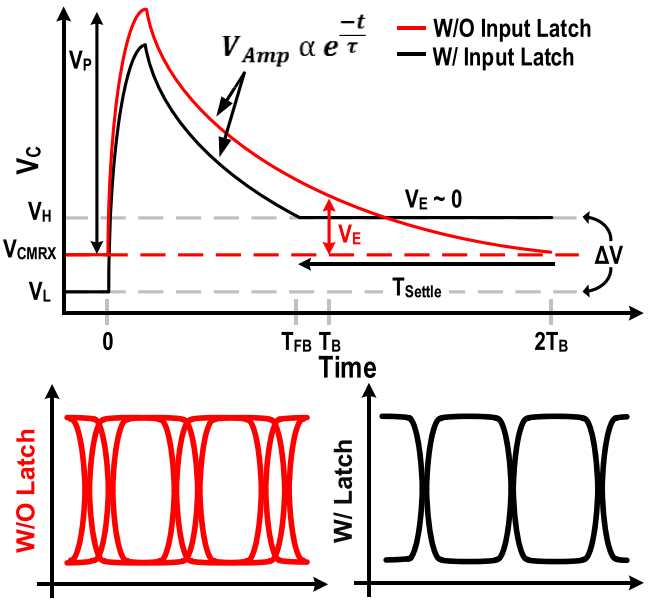

Fig. 6. Comparison of RZ and PRZ pulse characteristics and resulting output eye diagrams.

in Fig. 6. However, the pulses diverge from one another as the PRZ signal experiences the transient shift in bias voltage at time T_{FB}. By toggling the input bias, the total voltage decay time is reduced, thereby reducing the effective PRZ settling time. Unlike the tradeoff described in Fig. 4, the peak amplitude V_P is maintained while the error voltage V_E is decreased, simultaneously preserving receiver sensitivity and reducing ISI. In addition, the reduced settling time enables the PRZ receiver to support higher data rates than that of an RZ pulse receiver. These features represent key advantages over previous hysteresis schemes while also minimizing output loading and power consumption.

By modifying the RZ pulse given in (3), the PRZ waveform can be expressed by (4). During the decay of the coupled pulse, the node's bias is toggled at time T_{FB}. This leverages the exponential decay of the previous bias and decreases the settling time of the input node

$$V_{\mathrm{C\_PRZ}}(t) = V_C(t) + u(t - T_{\mathrm{FB}}) \cdot \Delta V \left(1 - e^{\frac{-(t-T_{\mathrm{FB}})}{\tau}}\right). \quad (4)$$

Assuming the same signal swing and input network utilizing the CMOS SOI design values presented in Section IV-B, the PRZ receiver achieves a V_E value 1.7 times smaller than a fixed bias RZ receiver at 28 Gb/s. This reduction in V_E leads directly to lower p–p jitter values.

Together, the design of the input network and latched-biasing govern the PRZ pulse characteristics. While the functional operation is possible for a variety of parameters, optimal sensitivity and jitter performance require the co-design of the input network, the bias latching, and the bias switch control loop. These fundamental characteristics are expressed in terms of V_P, ΔV, and T_{FB}, respectively, and are used in Fig. 7 to describe optimal PRZ functionality.

In general, due to the offset biases of the PRZ receiver, pulses can experience V_E values that are positive, zero, or negative. Using V_E as an analogy for ISI performance, Fig. 7 depicts three sets of waveforms to portray the effects of individually varying V_P, ΔV, and T_{FB} on the PRZ pulse, holding two variables constant while varying the third. Utilizing the 45-nm CMOS SOI implementation presented in Section IV-B, the simulated jitter performance for all three cases is also included in Fig. 7 (right).

In Fig. 7, the coupled signal is assumed to include a single transition at time zero from a low to high value. The black waveforms and simulated data points represent a $\pm 20\%$ region around an optimized pulse that achieves near zero V_E due to its settling time approaching T_B. In contrast, the red waveforms depict V_P, ΔV, and T_{FB} values that result in settling time greater than T_B and their associated positive or negative V_E.

First, the coupled amplitude V_P is varied in Fig. 7(a). Here, small V_P values decay into the sensitivity region prior to the application of the new bias V_H at T_{FB}. This results in negative V_E values and an increased settling time due to re-charging of the node back to V_H. Similarly, large V_P values decay quickly toward the previous bias prior to T_{FB}. However, after the new bias is applied, the exponential decay slows due to the decreased voltage difference and results in a settling time greater than T_B and a positive V_E. The simulated jitter in Fig. 7(a) (right) exhibits a minimum near 90 mV, representing the case where the coupled amplitude decays to V_H just as the new bias is applied.

In Fig. 7(b), as ΔV is varied, a large ΔV again causes the PRZ pulse to decay below V_H prior to T_{FB}. Although re-charging of the node increases the settling time, the signal remains outside the sensitivity region throughout the PRZ pulse in this instance. Alternatively, small ΔV values allow the signal to enter the sensitivity region with only nominal improvements in the settling time over that of a fixed bias design. Fig. 7(b) (right) shows a symmetric response for both positive and negative V_E values around the minimum jitter point. A sharp increase in jitter is seen with exceptionally small values of ΔV due to the latch becoming weak as the two bias voltages approach one another.

Finally, Fig. 7(c) shows the effects of T_{FB} variation. Similar to a small V_P scenario, a large T_{FB} allows the pulse to decay below its new bias, requiring a longer time for the input to settle. For a smaller T_{FB}, the increased bandwidth of the feedback loop allows the receiver to latch more quickly. However, a slight rise in output jitter is seen for extremely fast T_{FB}, as shown in Fig. 7(c) (right). In this scenario, the large exponential decay that occurs prior to the new bias being applied is not fully leveraged, resulting in a longer than necessary settling time for a fixed T_B. Note that smaller T_{FB} values can yield better performance if T_B is decreased.

Across all three simulations in Fig. 7, much higher jitter is exhibited when the PRZ pulse decays into the sensitivity region compared to pulses which do not. This stems from the introduction of glitches into the receiver output and feedback control signal. Note that the bias feedback loop has a maximum gain which sets the minimum ΔV needed to ensure rail-to-rail operation. If the pulse decays below this level, an incorrect bias state can be temporarily applied, due to increased switch resistance, introducing excessive amounts

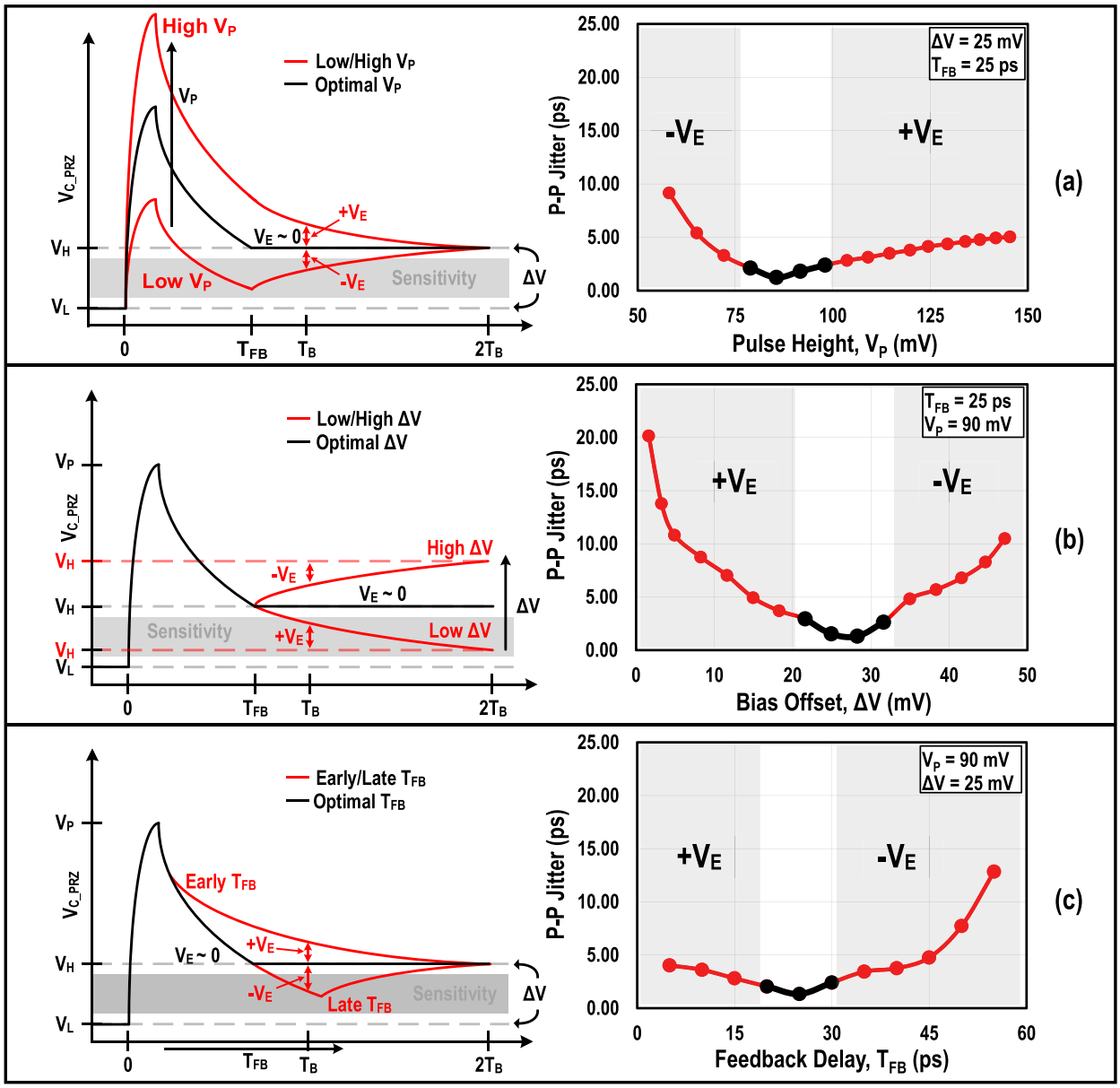

Fig. 7. Coupled PRZ waveforms highlighting the induced V_E and associated simulated jitter using the 45-nm CMOS SOI implementation at 28 Gb/s. (a) Varying V_P. (b) Varying ΔV. (c) Varying T_{FB}. Input signal 100-mV differential = V_P of 90 mV.

of jitter. In addition, all three parameters exhibit worsening performance at extreme values. However, to obtain peak performance, a balance of V_P, ΔV, and T_{FB} must be achieved with their interdependencies leveraged to compensate for the variation. Ultimately, the ideal case for a PRZ pulse is for T_B and T_{FB} to be coincident. Such a pulse results in maximum V_P and minimum settling time with no associated error voltage ($V_E = 0$), ensuring maximum sensitivity and minimal jitter for a given T_B. While similar analyses can be applied to a receiver regardless of hysteresis implementation, it is important to note that ISI generated in preceding nodes must be separately considered in order to quantify total ISI.

IV. Circuit Implementation

A. 130-nm SiGe BiCMOS Receiver

The first implementation of the proposed receiver is realized in a 130-nm SiGe BiCMOS process (f_T = 200 GHz) [19].

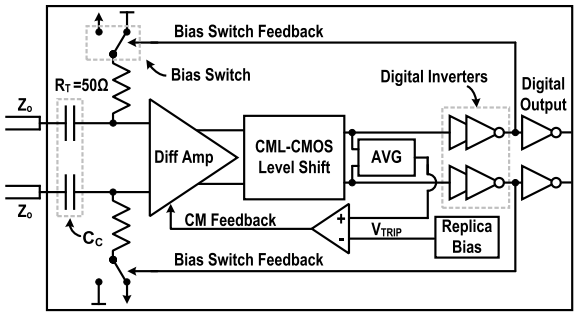

Fig. 8. Block diagram of the 130-nm SiGe BiCMOS receiver implementation.

The block diagram of this design, shown in Fig. 8, is comprised of the input coupling network, a differential amplifier with the proposed bias switches, a subsequent CML-to-CMOS level shifter, and digital output buffers. As discussed in Section III, the input network is composed of the coupling

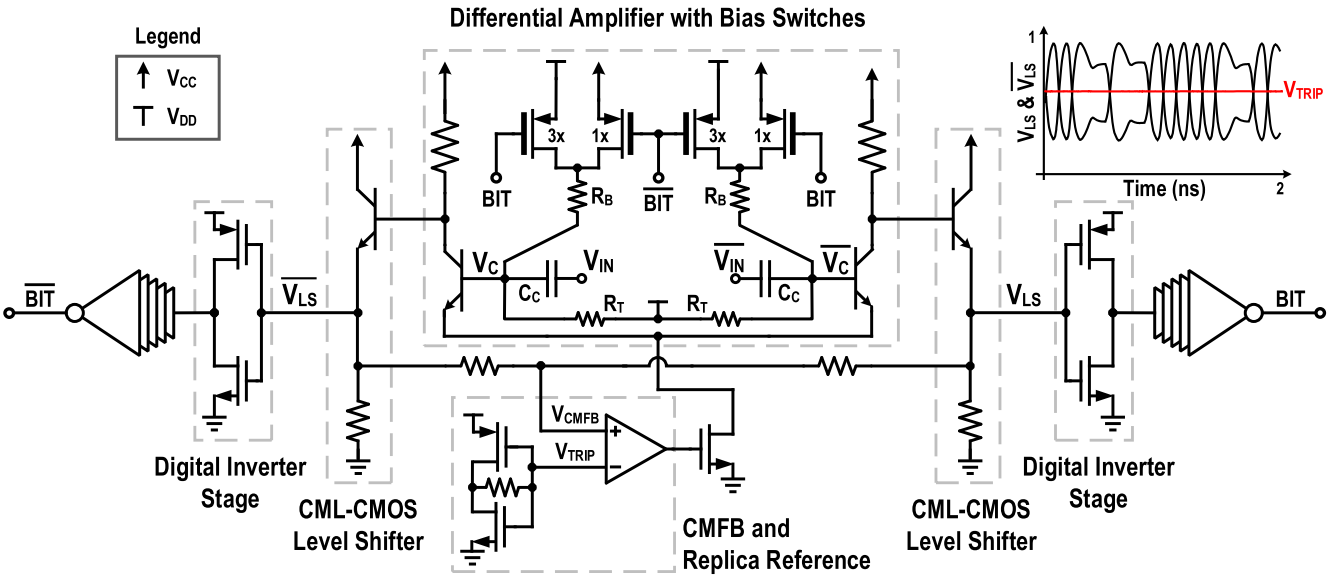

Fig. 9. Schematic of the 130-nm SiGe BiCMOS receiver implementation.

capacitors and termination resistance, which together, set the rate-of-decay of the coupled signal.

The full receiver schematic is shown in Fig. 9. Here, the coupling capacitance is implemented using the available, high-level metal–insulator–metal capacitors to limit substrate parasitics. A value of 1.3 pF is chosen for C_C, ensuring both an adequate coupled amplitude and a pulse decay time within the minimum bit period of 100 ps. V_H and V_L levels of 1.225 and 1.2 V, respectively, are generated from V_{CC} and V_{DD} through bias switch resistances.

After the input coupling, a differential amplifier is realized using high-f_T SiGe HBT devices, which improve the receiver bandwidth and gain over that of a 130-nm CMOS implementation. Directly interfacing this amplifier with the digital output and feedback proves difficult, as the output common-mode of the amplifier is not compatible with the subsequent full-scale CMOS digital buffering. Foregoing a second ac-coupling stage, which would simply re-introduce the need for latching, a high speed, dc level-shift is created using a SiGe common-collector (CC) stage. After the amplifier gain, the CC stage translates the incoming pulses from the I/O voltage domain down to the digital voltage domain. The level-shifted nodes (V_{LS}, $\overline{V_{\mathrm{LS}}}$) then drive several inverter stages, which amplify the signal to create a rail-to-rail digital waveform. The digital output (BIT, $\overline{\mathrm{BIT}}$) drives the bias switches with a feedback delay of ∼130 ps, latching each pulse at the amplifier input. In addition, the full-scale digital output enables a direct interface with standard digital libraries, facilitating high levels of digital integration [20], [21].

Within the receiver, PVT variations introduce skew between the CC output common-mode and the following inverter trip voltage (V_{TRIP}). When this occurs, duty-cycle distortion is introduced in the receiver output, closing the output eye and limiting the maximum data rate. To overcome this limitation, an automatic biasing scheme is implemented. Using a self-biased replica of the first inverter stage, the voltage V_{TRIP} is generated, marking the center of the inverter transfer function. At this voltage, the digital inverter exhibits its highest linearity and transimpedance. This is of importance as the amplitude of the input signal is small for which the inverter acts as an amplifier. Through the CMFB, the output common-mode of the CC is compared and aligned to V_{TRIP} by adjustment of the amplifier current bias.

The level-shifted and aligned signal then drives a chain of pseudo-differential CMOS inverters that generate the rail-to-rail output of the receiver. In addition, this output is used to toggle the input bias latches, maintaining the receiver state without additional circuitry. Sufficient gain in the feedback path ensures the input offset ΔV is amplified to full scale and maintains the previous state indefinitely. However, if the value of the feedback gain is too small to latch ΔV, the digital feedback does not reach full scale, resulting in a "soft" latch. During such an occurrence, the input pulses decay past the input biases and enter the sensitivity region, increasing jitter and potentially resulting in bit errors, as described in Section III-B.

B. 45-nm CMOS SOI Receiver

A second implementation of the proposed architecture is fabricated in a 45-nm CMOS SOI technology. To improve upon the speed and latency performance of the 130-nm design, minimum length, 45-nm CMOS devices are used to realize the amplifier core, reducing its area along with its required voltage headroom. This technology choice has the dual impact of lowering the power consumption of the receiver while eliminating the need for a CML-to-CMOS stage bridging the analog and digital domains. Instead, the lower supply voltage of the receiver enables the direct connection of the receiver output to the digital buffers. In this way, the feedback delay is reduced to approximately 30 ps, benefiting from the removal of level shifters as well as the increased speed of 45-nm inverters.

To fully leverage the higher speed receiver core, the input network is resized to minimize the decay time of the PRZ pulse and, thus, increase the potential bit rate of the receiver.

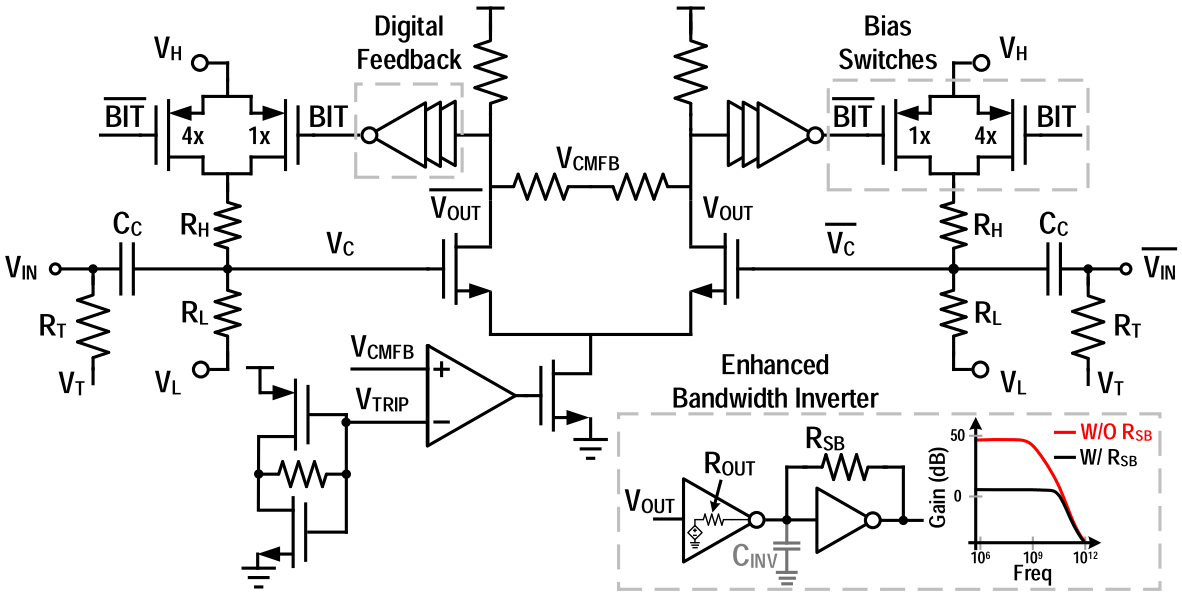

Fig. 10. Schematic of the 45-nm CMOS SOI receiver implementation.

A 125-fF interdigitated capacitor is utilized for ac coupling, leveraging the fine pitch of the 45-nm metals, and significantly reducing the footprint of the input network. In addition, the input resistance of the 130-nm implementation is replaced by two separate resistors: a termination resistance (R_T) outside of the capacitor and bias resistors (R_H, R_L) within the coupling capacitor. By separating these two functions, the time constant of the input network and strength of the bias switches can be tuned independently of the channel matching. This allows for optimization of the PRZ time constant and bias offset while improving the wide bandwidth termination compared to the 130-nm SiGe design. The bias resistors R_H and R_L values were chosen as 430 and 90 Ω, respectively. These values maintain a small RC time constant while allowing fine adjustment of ΔV through variation of V_L (500 mV) and V_H (525 mV).

At the output of the receiver, unlike the digital feedback, latency is of little concern. However, the bandwidth of the output buffers is critical in maximizing the data rate by limiting rise/fall times. To extend the bandwidth of the eight-stage output buffer, a self-biasing resistor is added to every other inverter stage. This addition extends the pole of the previous inverter from $1/(R_{\mathrm{OUT}}C_{\mathrm{INV}})$ to $1/((R_{\mathrm{OUT}}||R_{\mathrm{SB}})C_{\mathrm{INV}})$. Simulations show the 3-dB bandwidth of the first two inverter stages increase from 1.1 to 33 GHz with the addition of R_{SB}, as shown in Fig. 10. Each extended bandwidth buffer trades low-frequency gain to provide a flat broadband response. While this technique increases the number of stages required to achieve rail-to-rail operation, it ensures that frequency independent gain is applied to the output, limiting the introduction of jitter. In addition, by centering the input bias at the inverter trip point, the CMFB self-biased architecture, mimicking the SiGe design, ensures the inverters operate at peak gain while minimizing duty-cycle distortion.

In Fig. 10, the schematic of the 45-nm implementation is shown. As in the 130-nm SiGe design, CMFB is compared with a replica inverter bias to set the amplifier output

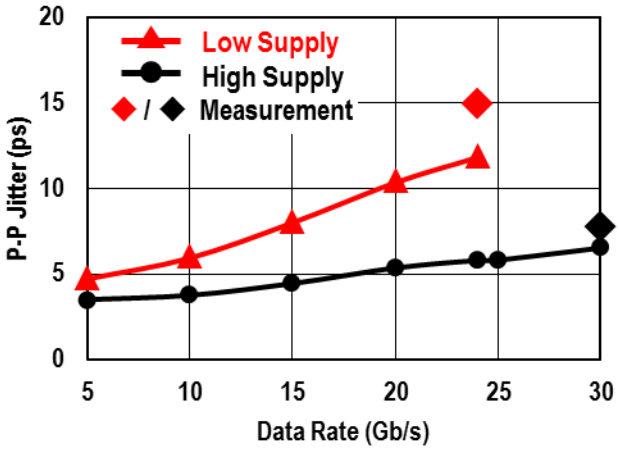

Fig. 11. Simulated p–p jitter of the 45-nm CMOS SOI receiver versus data rate and compared with peak power efficiency and data rate measurements.

common-mode. This ensures robust performance across PVT variations. Fig. 11 shows the simulated peak-to-peak (p–p) jitter across data rate as well as measured peak performance in both a low- and a high-supply condition: a V_{DD} of 1 and 1.3 V, respectively. The simulation test bench includes transmitter $\mathrm{RJ_{RMS}} = 200$ fs to imitate the measurement setup and results agree well with the experimental data. The low-supply condition achieves peak power efficiency point at 24 Gb/s, while the high-supply condition trades additional power for increased bandwidth. The low-supply condition systematically results in higher p–p jitter due to an increase in T_{FB}, resulting from the feedback inverters being current starved.

V. Measurement Results

The die micrographs of both implementations are shown in Fig. 12. Including the on-chip coupling capacitance, the 130 and 45 nm designs occupy 0.012 and 0.070 mm^2 of area, respectively. The implemented receivers are measured using PRBS15 data generated by a Keysight 8195A Arbitrary Waveform Generator, and the output is monitored

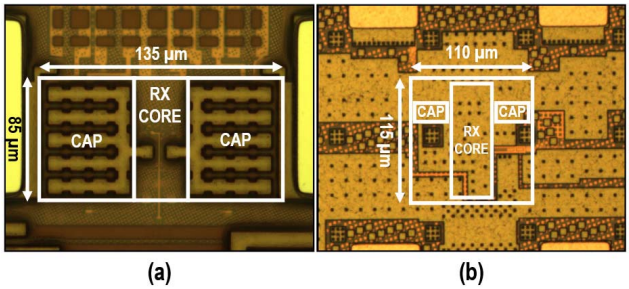

Fig. 12. (a) SiGe BiCMOS die micrograph. (b) CMOS SOI die micrograph.

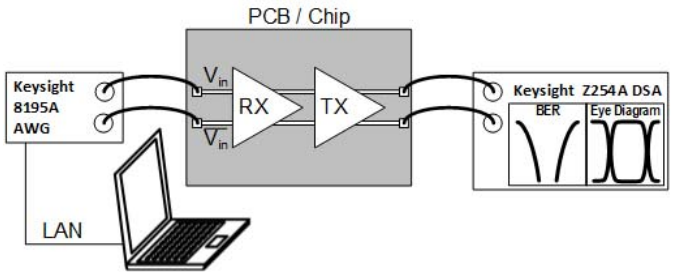

Fig. 13. Measurement setup.

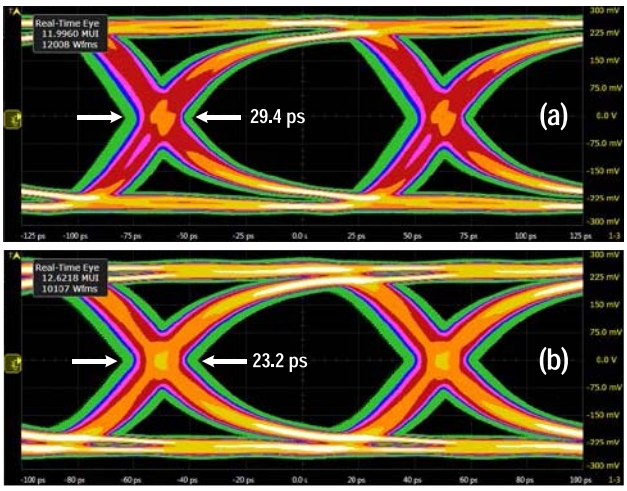

Fig. 14. SiGe BiCMOS output eye. (a) Low-supply condition peak efficiency at 8 Gb/s. (b) High-supply condition peak data rate at 10 Gb/s.

with a Keysight Infiniium Z204A Digital Signal Analyzer. Simulations show PRBS15 data sufficiently stresses the proposed architecture due to the PRZ signal decay and latching occurring in less than one-bit period. This results in minimal added ISI when the receiver is presented with CID lengths greater than 15. The measurement setup is shown in Fig. 13, where a current mode driver is included on-chip to enable feed-through testing, while adding minimal jitter to the receiver output.

A. 130-nm SiGe BiCMOS

In the first implementation, the fabricated die is stud-bumped and flipped onto an FR4 PCB with 2.5-cm transmission lines for data I/O, with a modeled channel loss

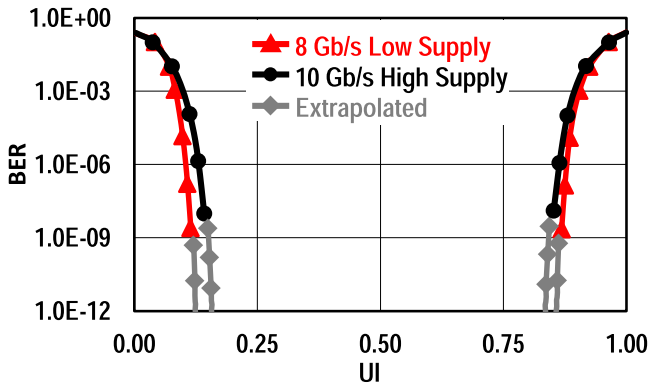

Fig. 15. SiGe BiCMOS BER bathtub curve at 8 Gb/s in the low-supply condition and 10 Gb/s in the high-supply condition.

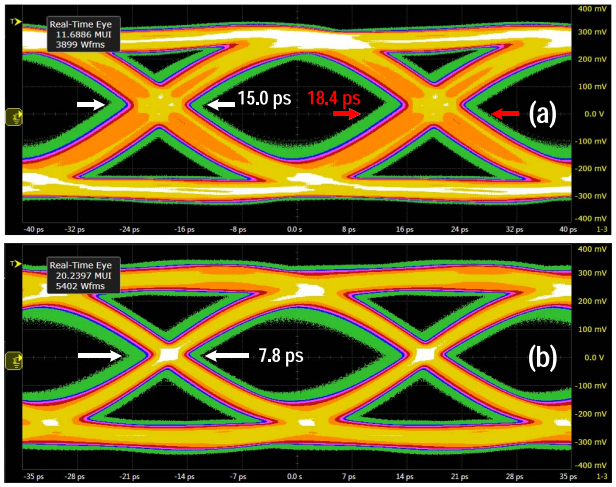

Fig. 16. CMOS SOI output eye. (a) Low-supply condition peak efficiency at 24 Gb/s. (b) High-supply condition peak data rate at 30 Gb/s.

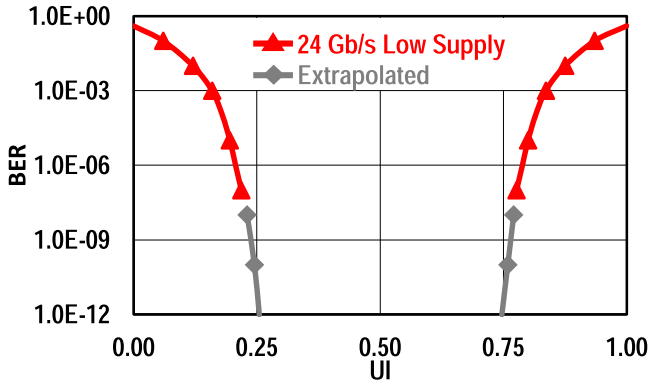

Fig. 17. CMOS SOI BER bathtub curve at 24 Gb/s in low-supply condition.

of 3 dB at 5 GHz. A 100-mV p–p differential signal is used as stimulus while performance is recorded under both low- and high-supply condition: V_{CC}/V_{DD} of 1.8/1.2 and 1.9/1.3 V, respectively. In the low-supply condition, the design achieves 29.4-ps p–p jitter at a rate of 8 Gb/s while consuming 3.7 mW. An eye diagram from this test condition is shown in Fig. 14(a). In the high-supply condition, a maximum bit rate of 10 Gb/s is reached while generating 23.2-ps p–p jitter and consuming 5.1 mW. The corresponding eye diagram for this test is also given in Fig. 14(b). The bit-error-rate (BER) curve for both

TABLE I
COMPARISON OF AC-COUPLED DATA RECEIVERS

		This Work†				JSSC06† [11]	VLSI07† [13]	TCASII14 [12]	JSSC16 [22]	JSSC16 [17]
Technology		**130 nm SiGe BiCMOS**		**45 nm CMOS SOI**		180 nm CMOS	90 nm CMOS	65 nm CMOS	14 nm CMOS	28 nm CMOS SOI
Coupling	Type	**AC On-Chip**				AC On-Chip	AC On-Chip	AC On-Chip	AC/ Pad-to-Pad	DC / On-Chip Cap. Term.
	Value	**1.3 pF**		**125 fF**		150 fF	80 fF	1 pF	N/A	30 pF
Signaling		**Differential**								Single-Ended
Encoding Req.		**No**								Yes
Die Area [mm^2]		**0.012[1]**		**0.007[1]**		0.043[1]	0.045[1]	0.20[1]*	0.045[1]	0.011[1]
Supply Condition		**Low**	**High**	**Low**	**High**	3	14	32 (4 Ch.)	32 (4 Ch.)	20
Aggregate Data Rate [Gb/s]		**8**	**10**	**24**	**30**					
Power Eff. [mW/Gb/s]		**0.46[1]**	**0.51[1]**	**0.25[1]**	**0.40[1]**	3.33[1]	2.29[1]	0.58[1A]	1.05[1B]	0.17[1BC]

† Clockless RX [1] RX Only * Estimated
[A] EQ (Analog) & Clocked Sampler
[B] Excludes Clocking Power
[C] Req. DC balanced data, includes deserializer

conditions is shown in Fig. 15, with the DSA reporting a statistical BER of less than 10^{-12} in both conditions.

B. 45-nm CMOS SOI

For testing the second implementation, custom RF/dc probes are used to characterize the standalone die with a modeled channel loss of 2 dB at 15 GHz. A 200-mV p–p differential bitstream is used as the input and performance is recorded under both the low- (1 V V_{DD}) and high-supply (1.3 V V_{DD}) conditions. In the low-supply condition, the design achieves 15.0-ps p–p jitter at 24 Gb/s with a peak efficiency of 0.25 mW/Gb/s. An eye diagram from this test condition is shown in Fig. 16(a). In the high-supply condition, a maximum bit rate of 30 Gb/s is reached while generating 7.83-ps p–p jitter and consuming 12 mW; the corresponding eye diagram is given in Fig. 16(b). The low-supply condition BER curve is given in Fig. 17, with the DSA reporting a statistical BER of less than 10^{-12}. The BER curve for the high-supply condition at 30 Gb/s is excluded due to bandwidth limitations in the test setup. Also, it should be noted that in the low-supply condition at 24 Gb/s, the output signal includes a differential offset, which increases the p–p jitter at the zero-crossing to 18.4 ps, as shown in Fig. 16(a). With this adjustment, the eye diagram and BER bathtub curve are in close agreement. Across five dies which were tested at 28 Gb/s, the receiver p–p jitter ranges from 8.6 to 10.4 ps.

C. Comparison

Table I summarizes the receivers' performance and compares to other high-speed receivers that utilize on-chip capacitive coupling. For full transceiver designs, only the receiver values are cited, where possible. In the 130-nm version of the architecture, the design compares favorably in efficiency and area despite the data-rate lagging recent works. Its lower speed performance primarily owing to the slower switching speed of full swing 130-nm CMOS inverters available in the SiGe BiCMOS technology. With the move to a 45-nm CMOS SOI technology and the improvements listed in Section IV-B, the proposed architecture achieves comparable data rates to the cited works while having the smallest active area footprint. In addition, the 45-nm receiver achieves the highest power efficiency among all receivers that do not require data encoding. Normalizing for differential signaling, the design achieves the best-reported power and area efficiency.

VI. CONCLUSION

A fully integrated, ac-coupled data receiver is presented with digitally latched input biases. The proposed latching generates a pseudo RZ pule that minimizes deterministic ISI and baseline wander while eliminating the need for the encoding typically associated with ac-coupled data-links. CMFB circuitry monitors and controls bias conditions to ensure optimal signal levels across PVT conditions, reducing duty-cycle distortion. Full-scale CMOS output levels control the bias latching and enable direct interface to standard digital cells. A 130-nm SiGe BiCMOS design is capable of sustained data rates up to 10 Gb/s in a high-supply condition, while a peak power efficiency of 0.46 mW/Gb/s at 8 Gb/s in a low-supply condition is demonstrated. A 45-nm CMOS SOI implementation operates up to 30 Gb/s in a high-supply condition while a peak power efficiency of 0.25 mW/Gb/s at 24 Gb/s is achieved in a low-supply condition. The architecture is suitable for both short, localized board-level and stacked-die applications, and benefits from technology scaling.

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REFERENCES

[1] D. Friedman. (2016). *Subcommittee Wireline-2016 Trends*. [Online]. Available: http://isscc.org/wp-content/uploads/2017/07/-ISSCC2016_Trends.pdf

[2] O. Viitala and J. Ryynänen, "Chip-to-chip communications using capacitive interconnects," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2010, pp. 2888–2891.

[3] C.-W. Huang, K.-J. Liu, Y.-J. Huang, M.-K. Chen, Y.-L. Lin, and M.-D. Ker, "Design of AC-coupled circuit for high-speed interconnects," in *Proc. IEEE Global High Tech Congr. Electron.*, Nov. 2012, pp. 87–90.

[4] X. Wu, P. Palmers, and M. S. J. Steyaert, "A 130 nm CMOS 6-bit full Nyquist 3 GS/s DAC," *IEEE J. Solid-State Circuits*, vol. 43, no. 11, pp. 2396–2403, Nov. 2008.

[5] M. Aguirre, C. Heredia, H. Torres, R. Palomera, and M. Jimenez, "Design of a CMOS 1.8 V low voltage differential signaling receiver," in *Proc. 45th Midwest Symp. Circuits Syst. (MWSCAS)*, vol. 2, Aug. 2002, pp. II-647–II-650.

[6] H.-C. Chow and W.-W. Sheen, "Low power LVDS circuit for serial data communications," in *Proc. Int. Symp. Intell. Signal Process. Commun. Syst.*, Dec. 2005, pp. 293–296.

[7] M.-D. Ker and C.-H. Wu, "Design on LVDS receiver with new delay-selecting technique for UXGA flat panel display applications," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2006, p. 4.

[8] P. Xiao, D. Kuchta, K. Stawiasz, H. Ainspan, J.-H. Choi, and H. Shin, "A 500 Mb/s, 20-channel CMOS laser diode array driver for a parallel optical bus," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 1997, pp. 250–251.

[9] Y. Dong *et al.*, "AC-coupling strategy for high-speed transceivers of 10 Gbps and beyond," in *Proc. IFIP Int. Conf. Very Large Scale Integr.*, Oct. 2007, pp. 84–87.

[10] S. Mick, J. Wilson, and P. Franzon, "4 Gbps high-density AC coupled interconnection," in *Proc. IEEE Custom Integr. Circuits Conf.*, May 2002, pp. 133–140.

[11] L. Luo, J. M. Wilson, S. E. Mick, J. Xu, L. Zhang, and P. D. Franzon, "3 GB/s AC coupled chip-to-chip communication using a low swing pulse receiver," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 287–296, Jan. 2006.

[12] T. Kim, S. Jang, S. Kim, S.-H. Chu, J. Park, and D.-K. Jeong, "A four-channel 32-Gb/s transceiver with current-recycling output driver and on-chip AC coupling in 65-nm CMOS process," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 61, no. 5, pp. 304–308, May 2014.

[13] M. Hossain and A. C. Carusone, "A 14-Gb/s 32 mW AC coupled receiver in 90-nm CMOS," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2007, pp. 32–33.

[14] G. R. Gangasani *et al.*, "A 32 Gb/s backplane transceiver with on-chip AC-coupling and low latency CDR in 32 nm SOI CMOS technology," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2474–2489, Nov. 2014.

[15] P. A. Francese *et al.*, "A 16 Gb/s receiver with DC wander compensated rail-to-rail AC coupling and passive linear-equalizer in 22 nm CMOS," in *Proc. ESSCIRC 40th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2014, pp. 435–438.

[16] E. Fang, G. Asada, R. Kumar, S. Hale, and M. Leary, "A 5.2 Gbps hypertransport integrated AC coupled receiver with DFR DC restore," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2007, pp. 34–35.

[17] B. Dehlaghi and A. C. Carusone, "A 0.3 pJ/bit 20 Gb/s/wire parallel interface for die-to-die communication," *IEEE J. Solid-State Circuits*, vol. 51, no. 11, pp. 2690–2701, Nov. 2016.

[18] J. Wilson *et al.*, "Fully integrated AC coupled interconnect using buried bumps," *IEEE Trans. Adv. Packag.*, vol. 30, no. 2, pp. 191–199, May 2007.

[19] B. Mathieu *et al.*, "An AC coupled 10 Gb/s LVDS-compatible receiver with latched data biasing in 130 nm SiGe BiCMOS," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Oct. 2017, pp. 1–4.

[20] J. J. McCue *et al.*, "A time-interleaved multimode $\Delta\Sigma$ SRF-DAC for direct digital-to-RF synthesis," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1109–1124, May 2016.

[21] L. Duncan *et al.*, "A 10-bit DC-20-GHz multiple-return-to-zero DAC with >48-dB SFDR," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3262–3275, Dec. 2017.

[22] C. Thakkar, S. Sen, J. Jaussi, and B. Casper, "A 32 Gb/s bidirectional 4-channel 4 pJ/b capacitively coupled link in 14 nm CMOS for proximity communication," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 3231–3245, Dec. 2016.

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