A Fully On-Chip 80-pJ/b OOK Super-Regenerative Receiver With Sensitivity-Data Rate Tradeoff Capability

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***Abstract*— This paper presents an ultra-low power super-regenerative receiver suitable for ON–OFF keying modulation and provides analytical insight into its design procedure. The receiver is fabricated in 40-nm CMOS technology and operates in the ISM band of 902–928 MHz. Binary search algorithm through successive approximation register architecture is being exploited to calibrate the internally generated quench signal and the working frequency of the receiver. Employing an on-chip inductor and a single ended to differential architecture for the input amplifier has made the receiver fully integrable, eliminating the need for external components. A power consumption of 320 μW from a 0.65-V supply results in an excellent energy efficiency of 80 pJ/b at 4-Mb/s data rate (DR). The receiver also employs an analog to digital converter that enables soft-decisioning and a convenient sensitivity-DR tradeoff, achieving sensitivity of −86.5, and −101.5 dBm at 1000- and 31.25-kbps DR, respectively.**

***Index Terms*— Low-voltage receiver, medical implant communication service (MICS), ON–OFF keying (OOK), selectivity, sensor network, super-regenerative oscillator, super-regenerative receiver (SRR), ultra-low power (ULP), wake-up radio (WUR).**

I. Introduction

THE rapid growth of the wireless communication market has persisted over the past years, and by the advent of the Internet-of-Things (IoT) notion, and desire for a ubiquitous wireless connection, the demand for more flexible and versatile wireless devices and communication is ever increasing. There still remain a number of major challenges to be addressed on the way to fully realizing IoT world, one of which is power consumption. To maintain a reliable wireless link between an access point, and, for an example, a smart toy, over a comparatively long distance and long period of time, the smart toy should be empowered with an ultra-low power (ULP) transceiver that at the same time offers reasonable performance. Medical implant communication service, wireless sensor networks, and wake-up radio (WUR) applications are also examples of areas that having an ULP transceiver seems appealing.

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Various architectures for ULP receivers have been recently studied, and plenty of works have offered decent performance while lowering the power consumption to milliwatt and sub-milliwatt range [1]–[24]. Among all the differences and similarities of these works, they can be differentiated on the basis of their architecture into two generic categories: 1) linear receivers [1]–[8]; in which a local oscillator (LO) signal is used to down-convert the desired signal from radio frequencies to baseband and 2) nonlinear, envelope detector (ED)-based receivers [9]–[24]. The latter category is more suitable for simple modulation schemes, in which demodulation is performed by extracting the data overlaid in the envelope of the incoming signal, using an ED. Fig. 1 depicts simple block diagrams of such ULP receivers. Linear receivers [Fig. 1(a)] tend to be more robust, however, more power consuming. Channel selection done by the synthesizer and gain and noise figure (NF) of the receiver is less sensitive to process/voltage/temperature (PVT) variations. On the other hand, a synthesizer consumes significant portion of the power budget, limiting linear receivers to milliwatt range. Although sub-milliwatt linear receivers have been reported through innovative low-power circuit design techniques, they usually compromise the performance of the LO generation block, which is the most important advantage of linear architecture over the other group. For instance, Kopta *et al.* [1] employs a ring oscillator for LO generation, resulting in poor phase noise, and consequently sensitivity. Similarly, Cheng *et al.* [5] relies on injection locking to an external LO signal, to improve the phase noise of its internal voltage-controlled oscillator (VCO), and Cha *et al.* [8] completely assumes external LO signals. In another example, Heiberg *et al.* [7] uses an extremely low-voltage supply, and in that way requires as many as eleven on-chip inductors to realize an accommodating circuitry.

Nonlinear receivers, on the other hand, are inherently low power, however, more prone to interference, and less robust. Nonetheless, they can be differentiated in the following three sub-categories.

1) Uncertain-IF receivers (UIF) [9]–[13], where a free-running ring oscillator realizes the LO signal that down-converts the desired signal to an uncertain IF, from which point the data are extracted by means of an ED [Fig. 1(b)].
2) Super-regenerative receivers (SRR) [14]–[22], which is based on the super-regenerative oscillator (SRO) architecture and there is no explicit frequency conversion scheme [Fig. 1(c)].

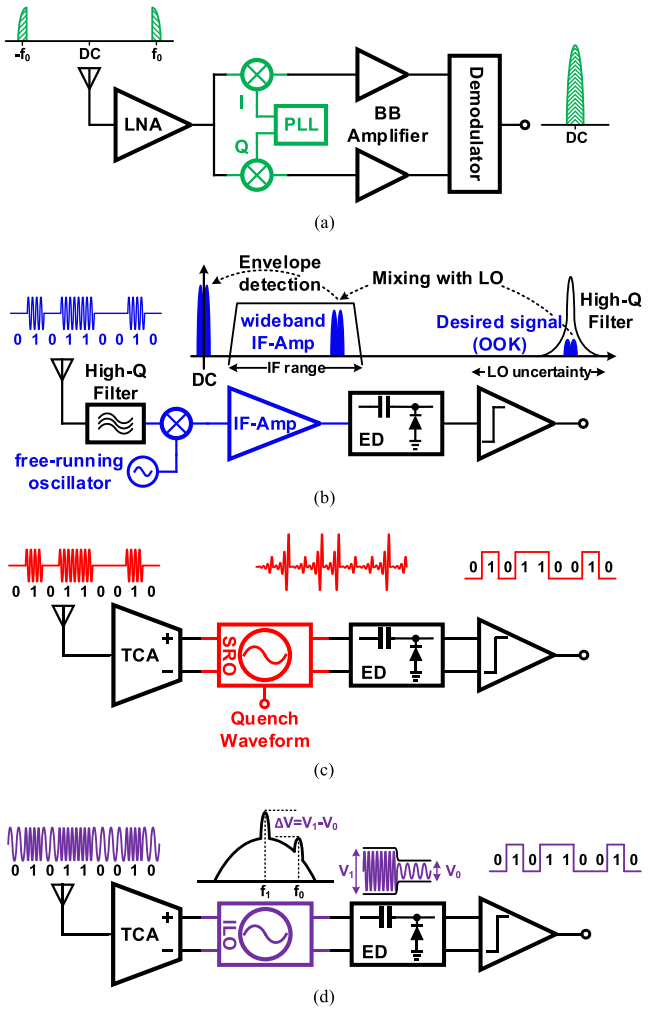

Fig. 1. Conceptual block diagram of (a) linear, (b) uncertain-IF, (c) super-regenerative, and (d) injection-locking receivers.

3) Injection locking oscillator (ILO) receivers [23], [24], which is similar to SRO, and uses a tuned oscillator as a frequency to amplitude conversion block to extract frequency-shift keying (FSK)-modulated data from the incoming signal [Fig. 1(d)].

UIF receivers are susceptible to interference, since they indiscriminatingly down-convert a wide range of frequency spectrum to the baseband through an envelope detection, and therefore usually require a high-Q input filter. ILO receivers' architecture is similar to that of SRR, although the reception mechanism is different. An ILO employs a tuned oscillator and injection locking concept [25] to receive and demodulate an FSK-modulated signal, while an SRR modulates the bias current of its oscillator and relies on the transient response of the oscillator. As such, an SRR is capable of receiving ON–OFF keying (OOK), and ASK, in addition to FSK modulation. Moreover, modulating the bias current of the oscillator, as will be discussed in Section II, can theoretically result in a more selective bandpass filter, compared to an oscillator with a constant bias current as in ILO receivers. Therefore, it is possible for an SRR to achieve better performance than that of an ILO counterpart, in similar conditions.

While SRR can provide decent performance even at sub-100 μW range it suffers from some fundamental challenges that this paper tries to address. For instance, an SRR requires multiple calibration schemes to guarantee its proper performance. Without the required calibrations, the SRR performance could degrade significantly. Chen *et al.* [21] have offered such calibration measures, however, this has dramatically increased power consumption; it employs a fractional-N synthesizer that needs to be running incessantly, except for short period of reception, to set the operating frequency. As will be explained in Section III, the amplitude variation of the SRO can also cause an unknown frequency offset between the desired channel and its operating frequency. The presented work in this paper utilizes an amplitude-lock loop (ALL) to set the amplitude of the oscillation at a constant level to address this issue.

There is also a tradeoff between sensitivity and power consumption on one hand and the power of the back-radiated signal on the other hand. For instance, Copani *et al.* [18], Ayers *et al.* [19], and Bohorquez *et al.* [20] have removed the input isolating amplifier from the receiving path, and by doing so improved sensitivity and significantly lowered the power consumption. However, the back-radiated signal in these cases could potentially be strong and depending on different regulations might not be allowed. This tradeoff is studied in Section II in more depth. Integrability is another challenge; in order to improve the receiver performance, particularly power consumption, sensitivity and selectivity, many works [17]–[20] have incorporated external components. Bohorquez *et al.* [20] are employing a custom designed antenna as the resonator, and Ma *et al.* [17] needs as many as six external components in addition to a balun, making them less attractive for low-cost applications. Rezaei *et al.* [26] have reported a fully integrated receiver that incorporate various calibration schemes to ensure the proper functionality of the receiver while achieving the best performance of a fully integrated SRR. In this paper, the authors show that the proposed receiver is quite flexible in terms of trading off data rate (DR) for sensitivity. In contrast to conventional OOK receivers, here an analog to digital converter (ADC) is employed to convert the received signal, and by doing so has enabled the physical layer to spread a low DR signal on a higher baud rate stream and gain a remarkable sensitivity improvement.

Section II reviews the generic theory behind a SRR trying to provide insights into the complex mathematical studies published regarding the super-regenerative systems. Section III presents the proposed receiver architecture and examines the practical issues inherited in this concept, and measures to mitigate these problems. The circuit implementation is explained in Section IV and provides the simulation results of the key building blocks. Extensive measurements data are presented in Section V, and finally Section VI concludes this paper.

II. General Theory of Super-Regeneration

An SRR, as shown in Fig. 2(a), constitutes an input transconductance amplifier (TCA) isolating the antenna from, and coupling the incoming signal to the SRO, an ED extracting the amplitude of the oscillation, and a comparator that decides whether or not the received signal was *Zero* or *One*, based on the amplitude of oscillation. The SRO can be modeled as a

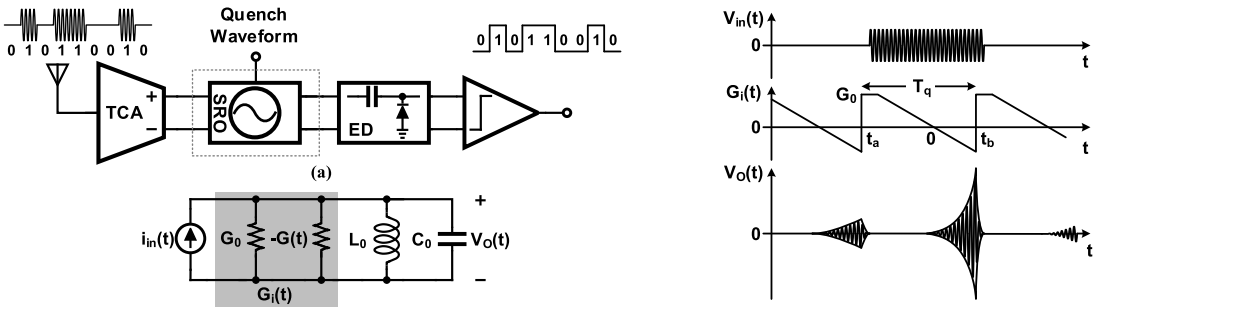

Fig. 2. (a) Simple block diagram of the SRR. (b) Parallel resonant RLC model of an SRO. (c) Generic example of an SRO oscillation amplitude with and without injected signal.

parallel resonant circuit as shown in Fig. 2(b), however, unlike conventional oscillators with constant negative conductance and steady oscillation, the negative conductance in an SRO is modulated, with a periodic signal usually called the *quench* signal, and therefore the oscillation repeatedly grows and decays. The presence or absence of the incoming signal affects the transient response of the oscillator and its oscillation build-up. As seen from Fig. 2(c), when the SRO is coupled with a tuned input signal, the oscillation starts faster, and therefore grows larger than the case where there is no input signal and the oscillation builds up merely due to noise.

Super-regenerative (SR) idea dates back to early days of electronics design [27] and has been rigorously studied ever since [28]–[33]. For the most part, these studies are similar in approach and results, and start from the characteristic differential equation of system Fig. 2(b) as following [32]:

$$\frac{1}{C_0}\frac{di_{\text{in}}(t)}{dt} = \frac{d^2V_O(t)}{dt^2} + \frac{G_i(t)}{C_0}\frac{dV_O(t)}{dt} + \left({\omega_0}^2 + \frac{1}{C_0}\frac{dG_i(t)}{dt}\right)V_O(t) \quad (1)$$

in which $\omega_0 = (1/\sqrt{L_0C_0})$ is the center frequency of the resonant network, and $G_i(t) = G_0 - G(t)$ is the instantaneous conductance of the tank. As shown in [32], the particular solution, V_{O_p}, for the differential equation (1), when $i_{\text{in}}(t) = I_0\cos(\omega_i t)$ can be expressed as

$$V_{\text{Op}}(t) = K_s\,p(t)\frac{I_0\omega_i}{C_0\omega_0}\int_t^{t_a} s(\tau)\sin(\omega_i\tau)\sin(\omega_0(t-\tau))d\tau \quad (2)$$

where K_s, $p(t)$, and $s(t)$ are super-regenerative gain, normalized output envelope, and the sensitivity curve of the SRO, and are defined as

$$K_s = \exp\left(\frac{-1}{2C_0}\int_0^{t_b} G_i(\tau)d\tau\right) \quad (3a)$$

$$p(t) = \exp\left(\frac{1}{2C_0}\int_t^{t_b} G_i(\tau)d\tau\right) \quad (3b)$$

$$s(t) = \exp\left(\frac{1}{2C_0}\int_0^{t} G_i(\tau)d\tau\right). \quad (3c)$$

By defining $S(\omega) = \mathcal{F}\{s(t)\}$ as the Fourier transformation of $s(t)$, (2) can be estimated by

$$V_{\text{Op}}(t) \approx K_s K_r\,p(t)\frac{I_0}{G_0}|H_{\text{BPF}}(\omega_i)|\cos(\omega_0 t + \angle S(\omega_0 - \omega_i)) \quad (4)$$

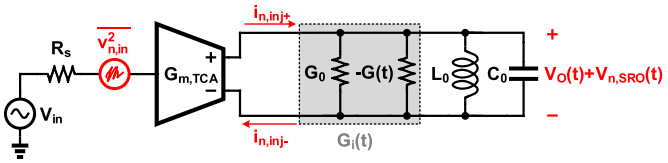

Fig. 3. Simple noise model of a generic SRO and input isolating amplifier.

where $K_r = (G_0/2C_0)S(0)$ is the SRO regenerative gain, and $H_{\text{BPF}}(\omega)$ models a bandpass filter around ω_0, governing the frequency response of the SRR to the input excitation signal $i_{\text{in}}(t)$, defined as

$$H_{\text{BPF}}(\omega) = \frac{\omega S(\omega_0 - \omega)}{\omega_0 S(0)}. \quad (5)$$

Equation (4) suggests that the SRO output voltage fundamentally depends on the behavior of $G_i(t)$, therefore it is essential to establish a method that can predict the performance of an SRR, given the parameters of such system[1] and its corresponding $G_i(t)$ signal. Assuming a simple OOK modulation, to find the bit error rate (BER) of a given SRR at a given input signal power level, the probability density function (PDF) of the peak SRO output voltage should be found in two cases; first, when there is no excitation at the input and oscillation starts due to the system noise (which is interpreted as *Zero*), and second, when the incoming signal at ω_0 with power P_{in} is applied to the input (and is interpreted as *One*). Consider Fig. 3, in which $\overline{v^2_{n,\text{in}}}$ models the input referred noise of the SRR, including noise of the antenna and receiver, that is noise due to $G_{m,\text{TCA}}$ block, tank loss G_0, and negative conductance block $-G(t)$. Therefore, the injected noise current into the SRO tank, i.e., $\overline{i^2_{n,\text{inj}}}$, can be related to the receiver NF as following:

$$\overline{i^2_{n,\text{inj}}} = \overline{(i_{n,\text{inj}+} - i_{n,\text{inj}-})^2} = G^2_{m,\text{TCA}}\overline{v^2_{n,\text{in}}} = 4kTR_SG^2_{m,TCA}NF. \quad (6)$$

Note that the NF in (6), that is also being used in this analysis, refers to the small signal model for a linear RLC network as shown in Fig. 3, and depends weakly on the variation of $-G(t)$, therefore, it can be calculated around $-G_i(t) \approx 0$, and assumed constant elsewhere.

[1]Such as noise figure, the resonator components value and quality factor, the input amplifier transconductance, and etc.

For the case of input *Zero* [i.e., $i_{\text{in}}(t) = 0$], the SRO output voltage V_O is merely generated due to the injection of $\overline{i_{n,\text{inj}}^2}$ into the SRO tank. Assuming $\overline{i_{n,\text{inj}}^2}$ has a white noise profile, the resulting noise voltage can be modeled as a bandpass noise [34], where the SRO tank frequency response is represented by (5); therefore, the bandpass noise can be expressed in quadrature form $V_{n,\text{SRO}}(t) = V_{n,\text{SRO},i}(t)\cos(\omega_0 t) - V_{n,\text{SRO},q}(t)\sin(\omega_0 t)$, with $\overline{V_{n,\text{SRO},i}^2} = \overline{V_{n,\text{SRO},q}^2}$ as the in-phase and quadrature components. Substituting (6) into (4), to find the power of the in-phase and quadrature noise component results in

$$\begin{aligned}\overline{V_{n,\text{SRO}}^2} &= \overline{V_{n,\text{SRO},i}^2} = \overline{V_{n,\text{SRO},q}^2} \\ &= \underbrace{K_r^2 K_s^2 \frac{G_{m,\text{TCA}}^2}{G_0^2}}_{A_{\text{SRR}}^2} \underbrace{4kTR_{\text{SNF}}\,\Delta f_{\text{ENB}}}_{\overline{v_{n,\text{in}}^2}} \\ &= A_{\text{SRR}}^2 \overline{v_{n,\text{in}}^2} \Delta f_{\text{ENB}} \end{aligned} \tag{7}$$

where A_{SRR} is the SRR small signal gain, and $\Delta f_{\text{ENB}} = \int_0^\infty |H_{\text{BPF}}(f)|^2 df$ is the equivalent noise bandwidth (ENB) of the SRO frequency response. The envelope of the SRO output voltage due to the input *Zero* can then be found by $V_{O,\text{Zero}} = \sqrt{V_{n,\text{SRO},i}^2 + V_{n,\text{SRO},q}^2}$, and its peak voltage has a Rayleigh distribution [34], with a PDF expressed as

$$\text{PDF}_{\text{Zero}}(V) = \frac{V}{\overline{V_{n,\text{SRO}}^2}} e^{-\frac{V^2}{2\overline{V_{n,\text{SRO}}^2}}} U(V) \tag{8}$$

where $U(V)$ is the unit step function.

In the case of the input *One*, the incoming signal V_{in} is amplified by A_{SRR} and is added to the bandpass noise of the SRO tank. Therefore, the envelope of the SRO output voltage due to input *One* can be found as $V_{O,\text{One}} = \sqrt{(A_{\text{SRR}} V_{\text{in}} + V_{n,\text{SRO},i})^2 + V_{n,\text{SRO},q}^2}$, and has a Rician distribution [35] with a PDF expressed as

$$\text{PDF}_{\text{One}}(V) = \frac{V}{\overline{V_{n,\text{SRO}}^2}} e^{-\frac{V^2 + A_{\text{SRR}}^2 V_{\text{in}}^2}{2\overline{V_{n,\text{SRO}}^2}}} I_0\left(\frac{A_{\text{SRR}} V_{\text{in}} V}{\overline{V_{n,\text{SRO}}^2}}\right) U(V) \tag{9}$$

where $I_0(V) = \frac{1}{\pi}\int_0^\pi e^{V\cos\phi} d\phi$ is the modified Bessel function of the first kind and order zero.

In contrast to [35], the BER of the SRR is determined at the output of the SRO instead of the ED, for two main reasons; first, the small signal gain of the SRR is usually high enough to neglect the additive noise of the following stages, and second, the ED can have a nonlinear gain profile complicating the calculation of final PDFs. Therefore, assuming a pseudo-random sequence with equal *Zero*s and *One*s probability for the incoming OOK signal, the BER of the SR receiver can be calculated from

$$\text{BER} = \frac{1}{2}\int_{V_{\text{th}}}^{\infty} PDF_{\text{Zero}}(V) dV + \frac{1}{2}\int_0^{V_{\text{th}}} PDF_{\text{One}}(V) dV \tag{10}$$

where V_{th} is the comparator threshold voltage; the incoming data are interpreted as *One*, if the peak voltage is higher than V_{th}, and *Zero* if it is lower.

Although (10) provides an accurate measure to find the SR receiver BER, at a given input signal level, it is not an intuitive measure. It is more intuitive to find the sensitivity of the receiver, P_{sen}, at a given BER. To do so, the SNR at the output of the SRO, $\text{SNR}_{\text{SRO,out}}$, can be found and equated to the minimum SNR that is required to detect the incoming OOK signal at a certain BER, $\text{SNR}_{\text{SR,min}}$, as following:

$$\text{SNR}_{\text{SR,min}} = \text{SNR}_{\text{SRO,out}} = \frac{\mu_1(\text{PDF}_{\text{One}})^2}{\mu_1(\text{PDF}_{\text{Zero}})^2} \approx \frac{A_{\text{SRR}}^2 V_{\text{in}}^2}{\frac{\pi}{2}\overline{V_{n,\text{SRO}}^2}} \tag{11}$$

where $\mu_1(\text{PDF}_X)$ is the expected value of random variable X. It is important to note that random variables represented by PDF_{One}, and PDF_{Zero}, are the oscillation amplitude of the SRO, for the input signals *One*, and *Zero*, respectively. Therefore, $\mu_1(\text{PDFOne})^2$, and $\mu_1(\text{PDFOne})^2$ correspond to the signal and noise power at the output of the SRO. Equation (7) can be substituted into (11), and then rearranged to find the sensitivity of the receiver as

$$P_{\text{sen}} = -174 + NF + SNR_{\text{SR,min}} + 10\log\left(\frac{\pi}{2}\Delta f_{\text{ENB}}\right). \tag{12}$$

Equation (12) is similar to the sensitivity of conventional linear receiver, except for the bandwidth. In conventional linear receivers, demodulation is being carried out at the baseband, where a sharp filter can select the desired signal band and filter out the rest. In this case, the noise bandwidth that is used to calculate sensitivity is limited to the signal bandwidth. This is not the case in an SR receiver; the noise bandwidth in (12) is determined by the selectivity of the SR oscillator, or in other word the ENB of the bandpass filter H_{BPF} in (5). Fig. 4 illustrates the performance of a generic SRR in two simple $G_i(t)$ cases, with such attributes that result is similar A_{SRR} for better comparison. As seen from Fig. 4(a), in a pulse-shaped quench signal, $G_i(t)$ is just above zero for most of the cycle, and abruptly jumps to a negative value, resulting in a wide sensitivity function $s(t)$, and narrow $H_{\text{BPF}}(\omega)$ [Fig. 4(b)]. Using (8)–(10), PDF_{Zero}, PDF_{One}, and the BER curves of the system for a different input signal power can be estimated. Fig. 4(c) depicts two graphs mapped into a single plot: 1) PDF_{Zero}, PDF_{One} at different P_{in} levels versus SRO output voltage (V_{SRO}) and 2) the corresponding BER curves versus a hard-decision decoder threshold voltage V_{th}. For instance, for a -93 dBm input, the BER reaches as low as 4×10^{-4} when $V_{\text{th}} \approx 40$ mV. Fig. 4(d), in contrast, shows a simple sawtooth quench signal in which $G_i(t)$ starts from G_0 and linearly increases during the quench cycle. This results in a much narrower $s(t)$, and wider $H_{\text{BPF}}(\omega)$ with higher ENB. Recalling from (12), at a certain BER level, the sensitivity of the sawtooth quench signal suffers from its excess ENB. Considering Fig. 4(b) and (e), $(\text{ENB}_{\text{sawtooth}}/\text{ENB}_{\text{pulse}}) = (5/1.1) \approx 6.5$ dB, which is translated to the sensitivity difference for identical BER level in Fig. 4(c) and (f).

III. Receiver Architecture

Fig. 5 shows a simple block diagram of the designed SRR including its calibration loops. The receiver works in three modes: 1) Frequency calibration mode, in which the

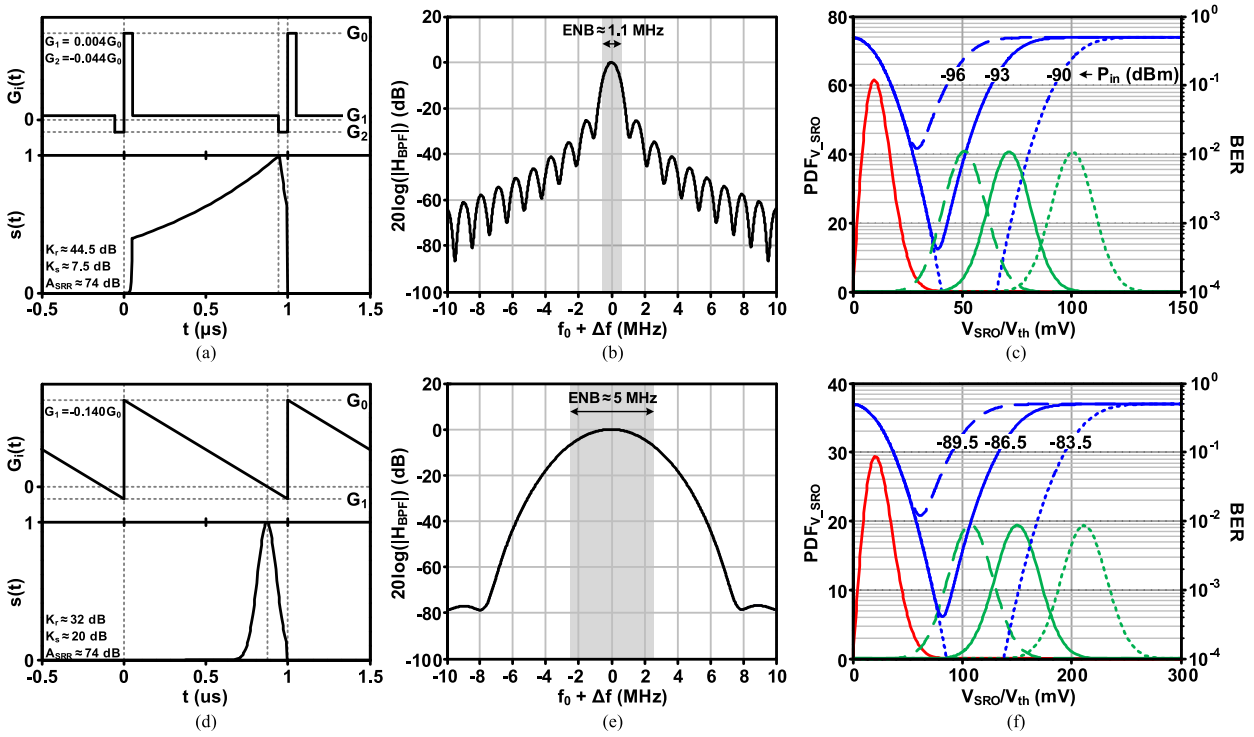

Fig. 4. Two simple cases of $G_i(t)$; Left column shows the $G_i(t)$ signals and the corresponding sensitivity curves $s(t)$. The frequency response of the SRO tank regarding the presented $G_i(t)$ signal and its ENB is depicted in the middle. The right column shows the PDF of the SRO output amplitude for *Zero*, and *One* input with three different power levels, versus the SRO amplitude V_{SRO}, and the corresponding BER curve versus the threshold voltage V_{th}.

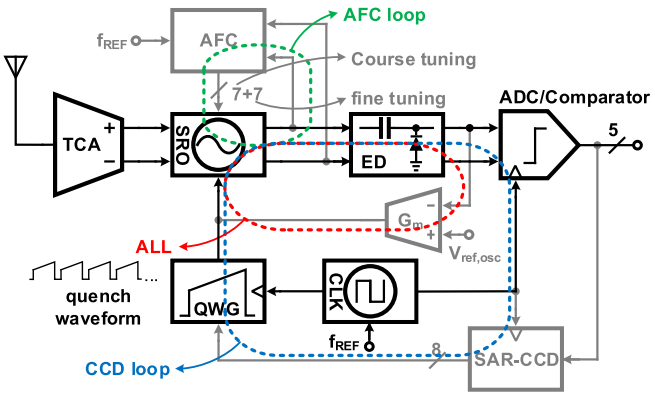

Fig. 5. Block diagram of the designed SRR, including calibration loops.

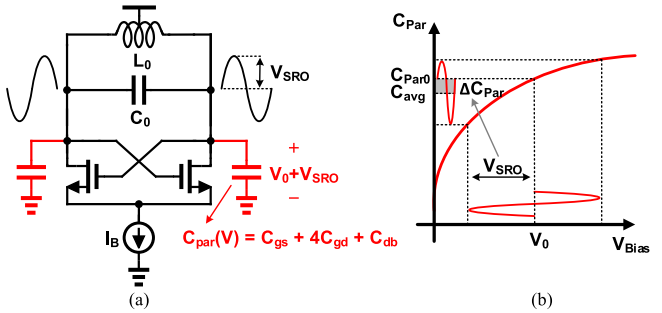

Fig. 6. (a) Effect of non-linear parasitics on the frequency calibration. (b) Different oscillation amplitudes, results in different parasitic values, and an offset frequency Δf.

center frequency of the SRO tank is tuned to the desired signal frequency; 2) Critical current detection (CCD) mode, where the SRO critical bias current is being searched for and found; and 3) RX-mode, in which the SRR is working and demodulating the incoming OOK signal.

A. Calibration Modes

In conventional linear receivers, the down-conversion of the desired signal is done by means of multiplying it with an LO signal, generated from a synthesizer. Although it is a power hungry block, a synthesizer can precisely control the reception frequency of the receiver. In an SR receiver, however, the center frequency of the SRO tank circuit determines the reception frequency of the receiver; therefore, a frequency calibration scheme is necessary to ensure its proper performance. Chen *et al.* [21] have employed a VCO (as the SRO) and a programmable integer-N PLL to adjust the resonance frequency of the SRO tank. When the calibration phase is over, the varactor voltage is held on a capacitor, the PLL is powered down and the receiver transits to RX-mode. The voltage captured by the capacitor is subject to, mainly, leakage and coupling with other signals and needs to be updated rather frequently, which drastically increases the power consumption. In this design, a DCO is employed at the core of the receiver as the SRO. This enables digitally control of the SRO frequency and getting rid of the need for frequent calibration cycles, reducing the power consumption. In this case, the frequency calibration is only needed, when the operating frequency changes. Regardless of the method used to adjust the desired

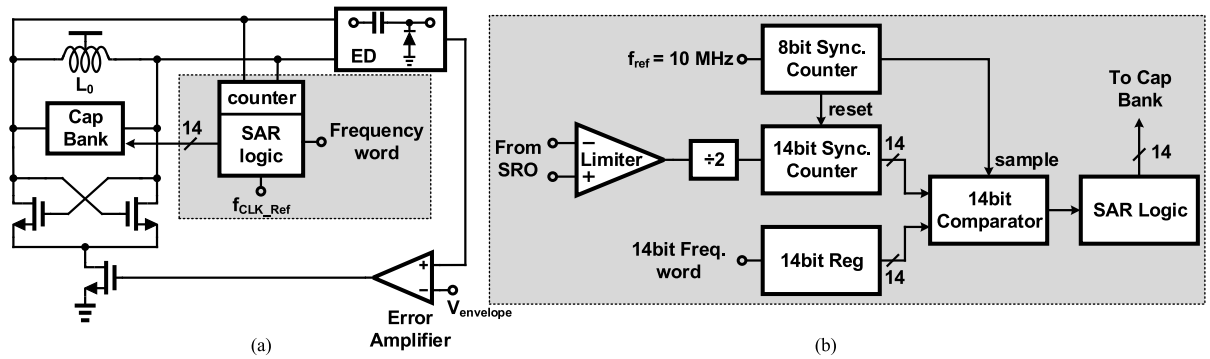

Fig. 7. (a) ALL keeps the oscillation amplitude at a constant and low level. (b) Automatic frequency calibration (AFC) sets the working frequency through a binary search algorithm done by 14-bit SAR.

frequency, there is always an intrinsic error associated with the calibration scheme.

Consider Fig. 6(a) in which a simple NMOS cross-coupled LC oscillator is depicted. To measure and therefore adjust the operating frequency, the oscillator needs to oscillate with some non-zero oscillation amplitude. The oscillation frequency can be found from

$$f_{\mathrm{SRO}} = \frac{1}{2\pi\sqrt{L_0\left(C_0 + \frac{C_{\mathrm{Par}}}{2}\right)}} \tag{13}$$

where $C_{\mathrm{Par}} = C_{\mathrm{gs}} + 4C_{\mathrm{gd}} + C_{\mathrm{db}}$ is the nonlinear voltage-dependent parasitics of the cross-coupled NMOS transistors. As seen from Fig. 6(b), at zero oscillation amplitude ($V_{\mathrm{SRO}} = 0$), the parasitics caps are biased at V_0. At non-zero oscillation amplitude, this bias point becomes modulated, and as a result of a nonlinear characteristics, the average parasitics capacitance that the tank circuitry senses decreases. It is impossible to set the desired frequency at the operating bias point of the SRO, since the SRO works in the quenched mode for the most part, where there is no oscillation. This means there would be an inevitable oscillation amplitude-dependent offset between the desired operating frequency and the calibrated one. The larger the amplitude of the oscillation is, the more deviation is introduced into C_{Par} and consequently f_{SRO}. This offset remains constant as long as the amplitude of the oscillation during frequency calibration phase is kept unchanged; otherwise, this offset varies unpredictably with the unknown amplitude of the oscillation. One way to keep the amplitude of the oscillation constant is to inject enough bias current into the SRO to make the oscillation amplitude voltage limited (similar to [21]). Although this makes the offset frequency constant and predictable, it results in the largest offset and requires comparatively large bias current. An alternative approach, as shown in Fig. 7(a) is to employ an ALL, that works simultaneously with the automatic frequency calibration (AFC) block, keeping the amplitude of the oscillation at a constant and low level. This approach not only saves power during frequency calibration phase and produces smaller offset, but also mitigates the leaked back-radiated oscillation as much as about 20 dB.

The AFC which is comprised of two 14-bit and 8-bit synchronous counters and a successive approximation register

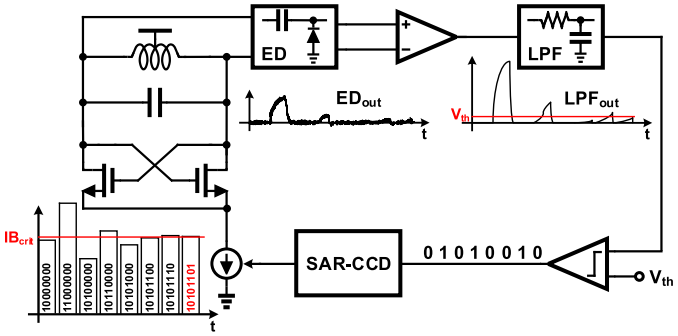

Fig. 8. CCD loop. Simulations showed this architecture can find $\mathrm{IB_{Crit}}$ with around %1 accuracy; therefore, an 8-bit SAR is employed to acquire this resolution.

(SAR) unit performs a binary search to set the SRO operating frequency. As shown in Fig. 7(b), the 8-bit counter, shares the same reference 10-MHz clock used to control Quench signal. It periodically counts from zero to a programmable number N_{count8}, resulting constant cycles of $T_{\mathrm{count}} = (N_{\mathrm{count8}}/10)\ \mu\mathrm{s}$. During these cycles, the 14-bit counter counts the zero crossings of a buffered, and divided by 2 version of the SRO output. At the end of each cycle, the result of this countdown is compared to a preset frequency control word, to determine whether or not the SRO frequency is below or above the target frequency. This approach, although simple, results in two major issues; first, there is a frequency error of $|\Delta f_{\mathrm{DCO}}| \leq (1/T_{\mathrm{count}})$ in the final result, and, second, the power consumption of the 14-bit counter is significantly high, as it is clocked at the SRO frequency. However, since the receiver does not require frequent frequency calibration, N_{count8} can be increased to reduce the frequency calibration error, with negligible overall power penalty.

A similar approach is employed to detect the critical current of the SRO ($\mathrm{IB_{Crit}}$) [21]. Once the frequency calibration is complete, and the capacitor bank state is stored accordingly, another binary search loop, as shown in Fig. 8, is activated to detect $\mathrm{IB_{Crit}}$. This method also intrinsically bears the offset problem. Theoretically, $\mathrm{IB_{Crit}}$ is defined as the point at which $G_i(t) = 0$, or in other word the oscillation is about to start, and therefore it is impossible to detect the exact critical current. Simulation shows $\mathrm{IB_{Crit}}$ can be found with

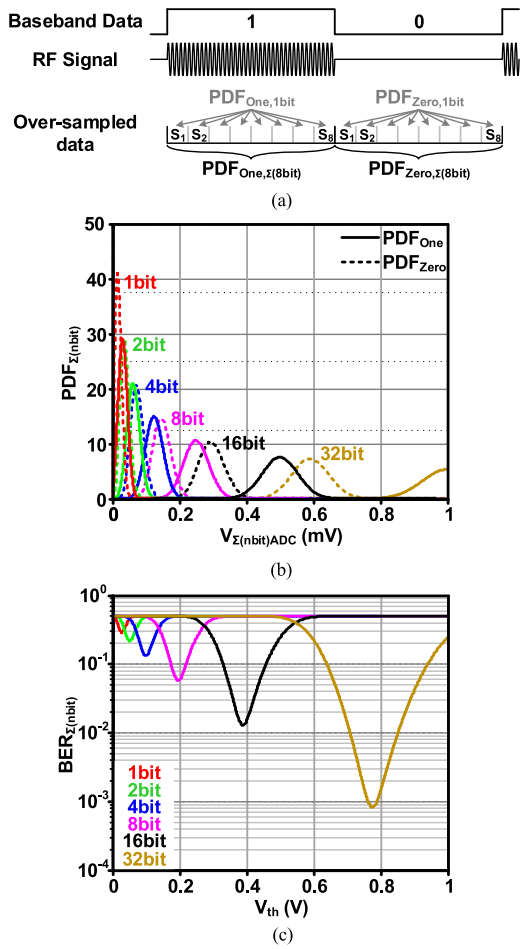

Fig. 9. (a) Baseband data, RF signal, and over-sampled data at the receiver, for an 8× over-sampling receiver. (b) Signal Zero and One PDF for accumulation of various number of bits, and (c) resulting BER for each case. These graph are MATLAB simulation results for the actual Quench signal shown in Fig. 17(b) and $P_{\text{in}} = -104$ dBm.

around 1% accuracy[2]; therefore, an 8-bit SAR is employed to realize the binary search. Once IB_{Crit} is detected, the quench wave generator (QWG) module generates the quench signal proportionally, which is described in Section IV-D.

B. RX Mode; Soft Decisioning and Data Rate-Sensitivity Tradeoff

In this mode, calibration loops are all off, and the clock generator module synchronizes the ADC and quench signal. The envelope of the SRO reaches its peak exactly at the end of the quench signal cycle, and is quenched steeply at the beginning of the next cycle; therefore, the output of ED is sampled exactly at the end of the cycle. Since the SRR is non-coherent, the sampling rate should be at least twice the data baud rate to adhere to the Nyquist criteria. The SRR is a sample data system, where it samples the envelope of the RF signal every quench period. Recalling (12), doubling the sampling rate, or in other word quench frequency f_q,

[2]It should be noted that the accuracy of IB_{Crit} detection depends on the closed-loop gain of system Fig. 8, and its comparator V_{th}. An additional calibration loop is required to set V_{th} in a way that guarantees an accuracy of 1%. However, in this design V_{th} is controlled manually to compensate for the lack of this additional calibration loop.

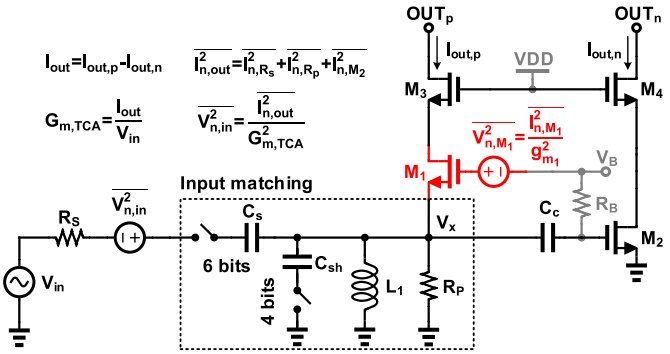

Fig. 10. Isolation amplifier along with the tunable input matching network. Assuming an acceptable input matching condition, the effect of the M_1 noise, $\overline{V^2_{n,M_1}}$, is cancelled at the output.

doubles the ENB of the SRO tank frequency response (H_{BPF}) and consequently degrades the sensitivity by 3 dB.[3] This design employs an ADC, enabling soft-decision decoding of the received data stream. In the conventional way of using a comparator and hard-decision decoding, the sensitivity suffers from the higher quench rate. For instance, when $f_q = 2f_{\text{Baud}}$, the second sample bears no additional info; it is either the same as the first one (00 or 11), in which case it is interpreted as the incoming data (0 or 1), or it is contradictory (01 or 10), where the output is not valid. However, by employing an ADC and soft-decision decoding, the amplitude of the ED output, as a measure of the signal power, can be extracted and the decision can be made from the accumulation of the consecutive samples amplitude. In fact, the soft-decision decoding can improve sensitivity by about 2.2 dB [36]. Moreover, this technique can be extended by means of oversampling the incoming data to improve the sensitivity even more. Fig. 9(a) shows conceptual baseband, RF, and oversampled signals for an 8× oversampling receiver. Higher DR can be traded off to employ higher oversampling rate and therefore achieving better sensitivity. Fig. 9(b) and (c) shows the PDF of signals *Zero* and *One*, and their corresponding BER, for different oversampling rates. It can be seen that by employing an oversampling rate of 32, the receiver can achieve a sensitivity of -104 dBm[4] at a lower DR.

This enables the receiver to estimate the power of the incoming signal and if possible adjust and optimize the communication link parameters. For example, if the power of the incoming signal drops, the receiver can detect it and ask transmitter to lower the transmitted DR. Now the receiver can make use of the over-sampled data, accumulate multiple cycles and therefore trade DR for sensitivity. Having an ADC instead of a comparator also makes it possible to use an adaptive gain control scheme that improves the dynamic range of the receiver.

[3]Compared to a coherent receiver, in which the sampling rate and DR are equal.

[4]The Quench signal of Fig. 17(b) has been used for this simulation, and as will be seen from Fig. 18, the oversampling rate of 32 has resulted in $-89-(-104) = 15$ dB sensitivity improvement, which is equal to its corresponding theoretical oversampling gain of $10\log 32 = 15$ dB.

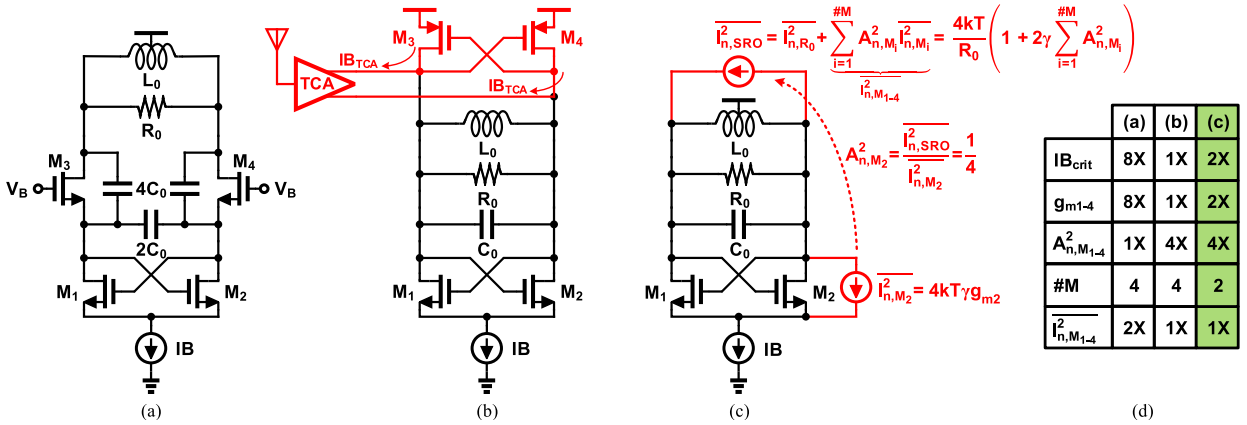

Fig. 11. Possible choices for the SRO and noise/power comparison. (a) Bias current switching differential Colpitts, (b) CMOS cross-coupled, and (c) NMOS cross-coupled oscillator. (d) Power consumption and output noise comparison for the presented oscillator choices. The NMOS cross-coupled oscillator is the preferred choice for this design.

IV. Circuit Implementation

A. Isolating Transconductance Amplifier (TCA)

The TCA, shown in Fig. 10, couples the antenna and SR oscillator. As discussed in Section II, the fundamental functionality of the SR receiver does not hinge on the presence or absence of the input amplifier. Moreover, the noise contribution of the input amplifier increases the overall NF of the system, degrading the SR sensitivity. It is only the issue of a strong back-radiated signal that mandates employing an input isolating amplifier. A CS-CG architecture provides a single-ended to differential conversion of the input signal without a need for a bulky external (or internal) balun, with an acceptable NF. Assuming $R_p||(1/g_{m1}) \approx (1/g_{m1})$, and $g_{m1} = g_{m2}$, the thermal noise due to M_1 is cancelled at the output. Cascode transistors $M_{3,4}$, do not contribute to the NF significantly, however, they enhance the backward isolation, and increase the output impedance of the TCA, minimizing the loading effect of its output impedance on the SR oscillator tank.

Being part of an ULP system, the input matching cannot be satisfied by means of M_1 transistor, as it would require much more bias current. Therefore, inductor $L_1 \approx 14.5$ nH with $Q \approx 10$ forms the tunable input matching network of the receiver along with the switchable shunt and series capacitor banks C_{sh} and C_s, and meanwhile provides a path for M_1 bias current.

The transconductance gain of the TCA, $G_{m,\text{TCA}}$, then becomes

$$G_{m,\text{TCA}} = 2g_{m1}\frac{V_x}{V_{\text{in}}} = 2g_{m1}\sqrt{\frac{R_p||\frac{1}{g_{m1}}}{4R_S}} \approx 2g_{m1} \approx 7 \text{ mmho}. \tag{14}$$

Assuming a matched input, the total input referred noise power of the TCA is, therefore, comprised of the contribution of R_S, R_p, and M_2 as following:

$$\overline{V^2_{n,\text{in,TCA}}} = 4kT\left(R_S + \frac{R_p}{4(1+R_p g_{m1})^2} + \frac{\gamma}{4g_{m1}}\right). \tag{15}$$

The simulations also show a backward isolation of better than 70 dB. That is for a stable and continuous 100-mV oscillation at the output of the SRO, the SRR radiates a -80 dBm signal.

B. Super-Regenerative Oscillator (SRO)

Being the heart of the SRR, it is worth scrutinizing different choices for an SRO. Fig. 11 shows three different options that are widely being used in SRR designs:

1) differential Colpitts oscillator with bias current switching scheme (Fig. 11(a), [20]);
2) CMOS cross-coupled oscillator (Fig. 11(b), [15]);
3) NMOS cross-coupled oscillator [Fig. 11(c), this design].

Assuming an identical inductor and transistors aspect ratios in all three cases, IB_{Crit} of Colpitts and CMOS cross-coupled oscillators are four times as much and half that of NMOS cross-coupled oscillator, respectively. The total output noise of this stage, $\overline{I^2_{n,\text{SRO}}}$, is also of importance, and is required to calculate the NF used in (6). Considering Fig. 11, there are three types of noise sources contributing to $\overline{I^2_{n,\text{SRO}}}$; loss of the tank, i.e., R_0, thermal noise of transistors M_{1-4}, and the tail bias current IB. Recalling from (6) that NF was defined for $\text{IB} \approx \text{IB}_{\text{Crit}}$, it can be deduced that the noise associated with the bias current source IB does not contribute to $\overline{I^2_{n,\text{SRO}}}$, since the SRO is not oscillating and this noise source can be considered a common-mode injection and neglected.

We define A^2_{n,M_i} as the conversion gain from the thermal noise source of transistor M_i to the output [as shown in Fig. 11(c)], so that $\overline{V^2_{n,\text{SRO}}} = \sum_{i=1}^{\#M} A^2_{n,M_i}\overline{I^2_{n,M_i}}$, where $\overline{I^2_{n,M_i}}$ and $\#M$ represent the thermal drain noise of transistor M_i, and number of transistors in the SRO. Although A^2_{n,M_i} for the differential Colpitts is four times smaller than that of cross-coupled counterparts, it has higher $\overline{I^2_{n,\text{SRO}}}$ due to its higher IB_{Crit}. Fig. 11(d) compares the normalized current consumption and output noise of the aforementioned three SRO choices. By taking the TCA bias current into account, as shown in Fig. 11(b), PMOS transistors $M_{3,4}$ generate significantly more noise, and consequently the CMOS cross-coupled SRO manifests higher NF. A symmetrical inductor

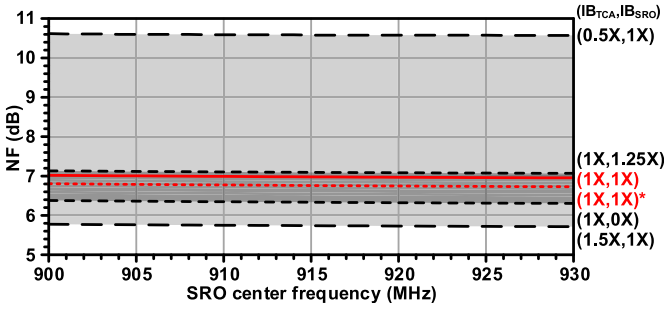

Fig. 12. Simulated NF of the SRR, measured at the output of the SRO, for different scenarios. The solid red line in the middle shows the NF when TCA is biased at its nominal value $IB_{TCA} = 150\mu$ A, and the SRO is biased at critical current $IB_{TCA} = IB_{Crit}$. The one with asterisk (*), shows the case when tunable input matching network switches are assumed ideal.

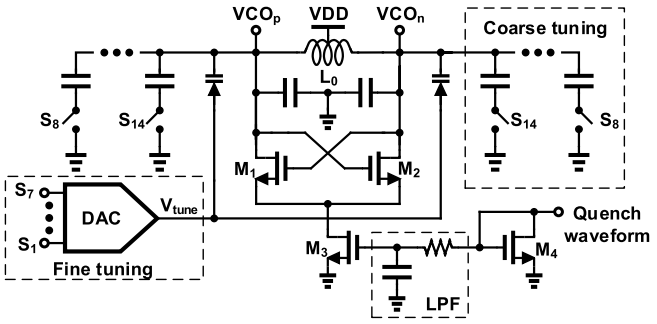

Fig. 13. Schematic of the designed SRO. Coarse tuning is done through switching a 7-bit binary weighted capacitor bank, while a 7-bit DAC controls two varactor for fine frequency tuning. The fine tuning MSB covers twice the coarse tuning LSB to rid the possibility of frequency gap.

with a differential inductance of $L_0 \approx 27$ nH and $Q \approx 13$ is used in the tank, resulting $R_0 \approx 2$ kΩ, which translates to $IB_{Crit} \approx 80$, and 40 μA for the NMOS, and CMOS cross-coupled SRO, respectively. Although the NMOS architecture requires slightly more bias current, it can use a lower supply voltage (VDD = 0.65 V in this design) and reduce the overall power consumption, beside manifesting superior NF. The NF of the SR receiver (when $IB_{SRO} = IB_{Crit}$) can now be found from

$$NF = 1 + \underbrace{\frac{R_p/R_S}{4(1+R_p g_{m1})^2}}_{\text{Matching Net.}} + \underbrace{\frac{\gamma}{4g_{m1}R_S}}_{\text{TCA}} + \underbrace{\frac{1+2\gamma}{4g_{m1}^2 R_0 R_S}}_{\text{SRO}} \approx 6.2 \text{ dB} \quad (16)$$

assuming $\gamma = 1$. Simulated NF of the receiver (at the output of the SRO) is shown in Fig. 12, for multiple scenarios of (IB_{TCA}, IB_{SRO}) pair. When the TCA is biased at nominal bias current $IB_{TCA} = 150$ μA, and SRO is biased at its critical current $IB_{SRO} = IB_{Crit}$, the NF of the system is about 7 dB. This plot justifies our assumption for (6), that NF is weakly dependent of $-G(t)$. As IB_{SRO} varies from 0 to IB_{Crit}, and finally to $1.25IB_{Crit}$, and consequently $G(t)$ changes from G_0 to 0, and to $-(G_0/4)$, respectively, NF varies for less than 1 dB. This weak relation is expected, since the SRO is the smallest contributing noise source in (16).

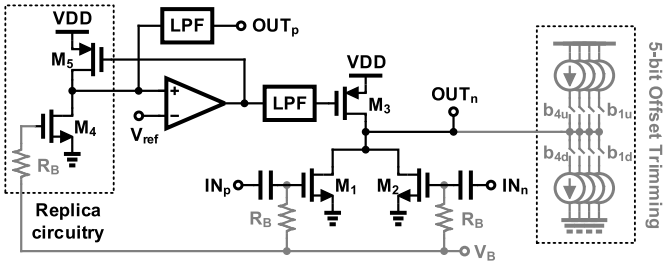

Fig. 14. Pseudo differential ED circuitry. Two sets of 4-bit source and sink (up and down) switchable current sources form a 5-bit offset trimming scheme.

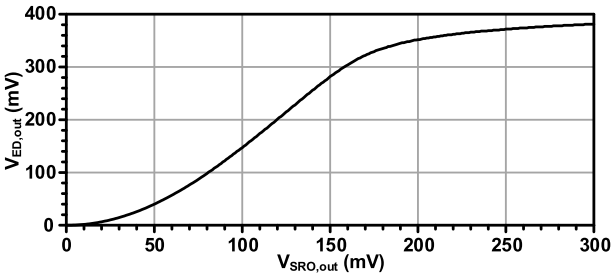

Fig. 15. Gain profile and input-output characterization of the ED. Dotted lines represent constant envelope, and solid lines show actual SRO envelope as the ED input.

The tunable matching network introduces about 0.3-dB loss,[5] mostly through the on resistance of the series switches.[6]

The final SRO design is shown in Fig. 13. The tank consists of a 7-bit capacitor bank, and a varactor, which its control voltage is driven by a 7-bit DAC, for coarse- and fine-frequency tuning, respectively. The MSB step of the fine tuning is designed to cover more than twice as much of the coarse tuning LSB to ensure there will be no frequency gap, in any various corners, temperatures, and mismatch conditions. The tuning range encompasses ±10% of the center frequency (915 MHz) to ensure that the desired band is completely covered. A fine resolution of around 100 KHz is achieved at the center frequency.

C. Envelope Detector

A pseudo-differential pair ($M_{1,2}$) forms a common-mode amplifier with an active load (M_3), as shown in Fig. 14. The envelope amplitude of the SRO output signal is amplified through the second-order nonlinearity of $M_{1,2}$, resulting in a nonlinear gain profile. It is worth noting that due to the exponential growth nature of the SRO output, its envelope has considerably high bandwidth, which should be accounted for in the ED circuitry design. This puts a tradeoff on the size of M_{1-3}; smaller transistors expose less parasitics and consequently higher bandwidth and gain, but on the other hand the output voltage suffers from a significant mismatch, and vice versa. A feedback loop along with a replica circuitry is

[5]That is in TT corner. In worst case scenario of SS corner, the loss increases to around 0.8 dB. Note that to accommodate the low voltage supply, low V_{th} devices are employed for the switches.

[6]These switches are controlled by a 1.1-V supply to lower their on resistance. However since they are static switches, no current is drawn from 1.1-V supply and it does not contribute to power consumption.

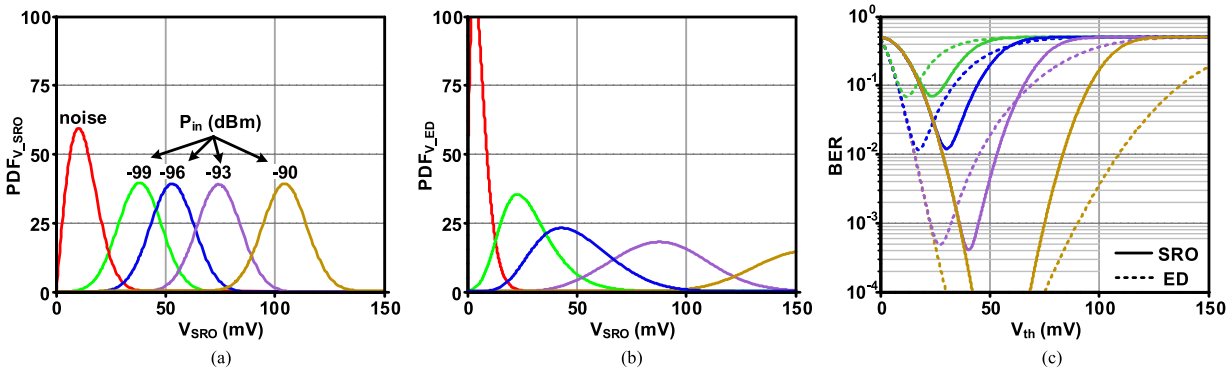

Fig. 16. (a) PDF of signals Zero and One, at the output of the SRO for multiple input signal power levels. (b) PDF of the same signals after passing through nonlinear gain profile of the ED and adding the output noise of the ED to them. (c) BER of the corresponding signals, calculated at the output of the SRO (solid lines), and the output of the ED (dotted lines).

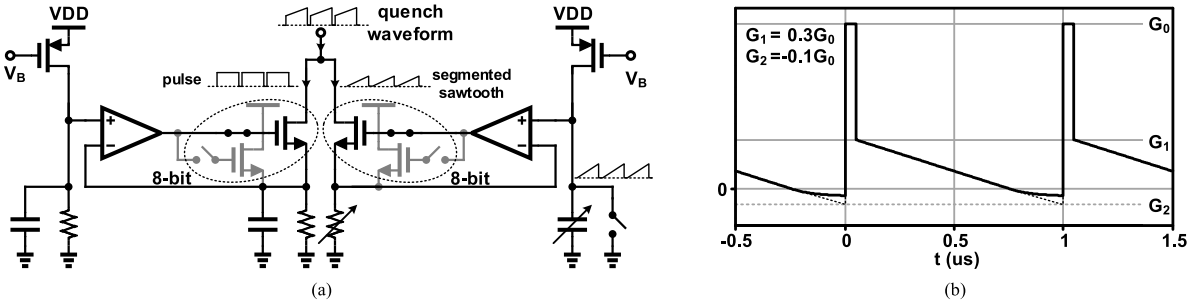

Fig. 17. (a) QWG schematic; a pulse and a sawtooth generator combined. (b) Actual quench signal used for BER calculation. The linear $G_i(t)$ signal is depicted in dotted line.

used to set the bias voltage of the ED, as well as to provide a pseudo differential output for the ED. Fig. 15 shows the ED input-output characteristics, considering the following stage loading and post-layout parasitics. Monte Carlo simulation for the output bias point shows $3\sigma \approx \pm 50$ mV; therefore, a 5 bit trimming offset cancellation is added to the output, reducing the offset to around 3 mV.

Using the ED gain profile, and knowing its output noise power of $\overline{v_{n,\mathrm{ED}}^2} \approx 1.8 \times 10^{-6}\ V^2$, the BER at the output of the ED can now be calculated. Fig. 16(a) and (b) shows MATLAB simulation results for the PDF of signals *Zero* and *One*, at the output of the SRO, and ED, respectively, and Fig. 16(c) shows their corresponding BER for multiple input signal power level. As it was expected, ED has little to no effect on the BER, since the gain of the preceding stages is considerably high (almost 74 dB). It should also be noted that as long as the ED has a monochromatic gain profile, its nonlinearity does not affect the overall BER.

D. Quench Wave Generator

Fig. 4 suggests that the best Quench signal is the one with zero slope, where $G_i(t)$ is just above zero for most of the cycle, and suddenly jumps to a negative value [Fig. 4(a)]. However, in reality for an ULP receiver, it is extremely hard to guarantee a stable and precise $G_i(t)$, let alone that the detection of the bias current at which $G_i(t) = 0$ is associated with some intrinsic error. Therefore, in this design, performance is compromised in return for robustness. A modified sawtooth waveform is chosen as shown in Fig. 17(a), and it is comprised of a pulse and a segmented sawtooth with equal duty cycle, both of which can be tuned with 8 bit accuracy. In this way, the performance of the SRR is much less sensitive to the errors in detection of $\mathrm{IB_{Crit}}$, and therefore variations of $G_i(t)$.

So far, it was presumed that $G(t)$ is linearly dependent on $\mathrm{IB_{SRO}}$; however, as the oscillation amplitude grows (when $G_i(t) < 0$), the ratio of large signal conductance of the cross-coupled transistors (G_{LS}) to its small-signal one (G_{SS}) starts to drop from initial value of one. Therefore, the exact value of $G_i(t)$ not only depends on time but also the amplitude of the oscillation. As a result, (1) becomes a nonlinear time variant differential equation. Beside the fact that analytical solution for such a system is very complicated and does not provide intuitive results, $G_i(t)$ and the oscillation amplitude does not have closed-form relation and should be estimated from simulations. Therefore, an iterative process is taken, to simulate the SRR performance due to nonlinearity of $G(t)$. First a linear $G_i(t)$ model [dotted line in Fig. 17(b)] is used to compute (9), and its corresponding $\overline{V_{\mathrm{SRO}}}$ is calculated. Provided the value of $\overline{V_{\mathrm{SRO}}}$, an exponentially saturating profile [solid line in Fig. 17(b)] for $G_i(t)$ is chosen so that at the end of the quench cycle, $G_i(t) = G_0 - G_{\mathrm{LS}}$, where G_{LS} corresponds to the large signal conductance of the cross-coupled transistors with oscillation amplitude of $\overline{V_{\mathrm{SRO}}}$.

Fig. 18 illustrates transient noise simulation results of the designed SRR with $f_q = 1$ MHz and $P_{\mathrm{in}} = -87$ dBm, along with the analytical prediction of (8)-(10) with $P_{\mathrm{in}} = -89$ dBm using the iterative process explained above, showing an acceptable agreement between the analytical results and transistor-level simulations.

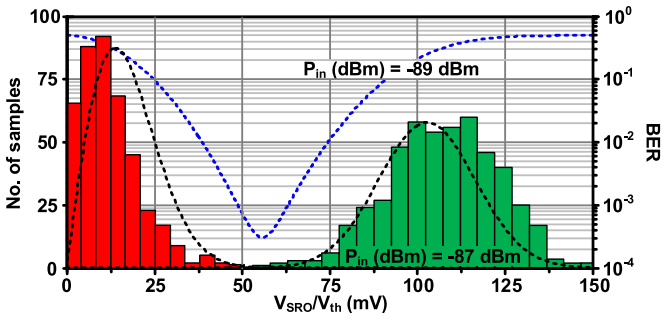

Fig. 18. Histogram for transient noise simulation of the designed SRR, sampled at the output of the SRO for the input signal $P_{\text{in}} = -87$ dBm. The dotted line shows the prediction of the BER for the same system and input signal $P_{\text{in}} = -89$ dBm. The mathematical analysis overestimates the sensitivity by about 2 dB.

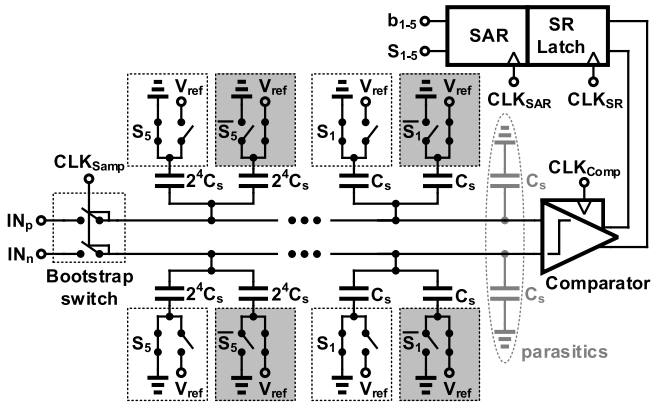

Fig. 19. 5-bit SAR differential ADC. Parasitics and loading of the comparator input, make up for the non-switchable unit capacitor C_s.

E. ADC

A 5-bit differential SAR-ADC based on [37], as shown in Fig. 19, captures the amplitude of the ED output. To accommodate with the low-voltage supply of 0.65 V, sampling switches are bootstrapped, and a double-tail latch-type voltage sense amplifier [38] as shown in Fig. 20(a) is also employed as the comparator. Two 4-bit capacitor banks, realized by NMOS transistors, are also added to the pre-charged nodes Di. As a result ± 15 mV offset cancellation with ± 1 mV resolution is provided. A 10-MHz master clock is used to generate all necessary clocks as partly shown in Fig. 20(b). The 5-bit output of the ADC is finally registered and stored one cycle to be read. Note that due to the differential architecture of the ADC, the sampled signal has a 4-bit resolution.

V. Measurement Results

The SR receiver is fabricated in the TSMC 40-nm CMOS technology and occupies an active area of 0.9×0.5 mm^2, as shown in Fig. 21, while consuming about 0.5 mA in the RX mode. It also draws less than 1 μA of leakage current when turned off. Table I summarizes the power breakdown of the SR receiver. The isolating TCA consumes most of the power, and while it does not play a fundamental role in the performance of the SR receiver (as shown in Section II), it may not be removed. Although [18]–[20] have removed the isolating amplifier to decrease the power consumption, as explained

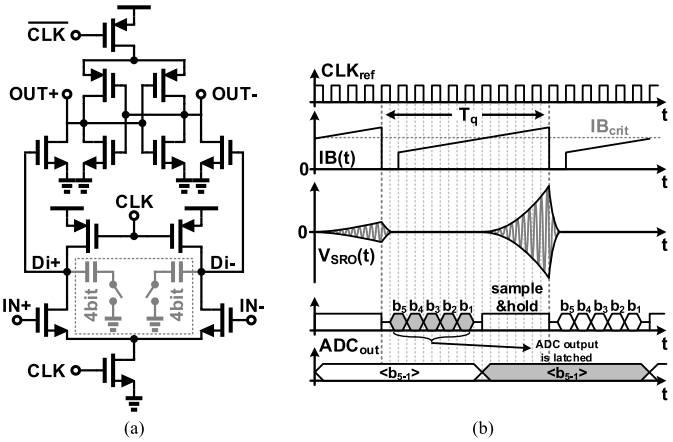

Fig. 20. (a) Voltage sense amplifier used as the clocked comparator with 4-bit offset cancellation. (b) Timing of the ADC. After the ED output is sampled at the end of quench cycle, the 5-bits output of the ADC are latched in the next cycle in tandem and latched to be read.

TABLE I
Power Breakdown of the Receiver

Individual Block		Operating Mode	
TCA	300 μA	RXM	500 μA
SRO	80 μA	AFC	2.6 mA
QWG	40 μA	CCD	700 μA[1]
ED	50 μA	OFF	< 1 μA
ADC	10 μA		

[1]The exact number varies, depending on the path that binary search takes to complete.

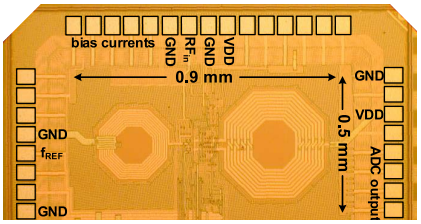

Fig. 21. Die micro-photograph of the designed SRR.

earlier, this would result in a very strong unwanted back-radiation. It is, however, possible to tradeoff sensitivity and power consumption, by decreasing the bias current of the TCA. In this case, the NF increases and sensitivity drops. Considering the power breakdown of the receiver in Table I, (16), and Fig. 12, and assuming $g_{m1} \propto \text{IB}_{\text{TCA}}$, it can be inferred that reducing IB_{TCA}, decreases the overall receiver figure-of-merit (FoM), defined as

$$FoM = 10 \log \left(\frac{DR}{P_{\text{DC}} P_{\text{Sens}}} \right) \tag{17}$$

where DR is the received signal data rate. The back-radiated power of the SR receiver is measured to be around -105, and -90 dBm, in the RX and calibration modes, respectively.

The receiver can be tuned from 800 to 980 MHz, fully covering the ISM band of 902–928 MHz. The step size of frequency tuning varies at the high and low end of its range; however, at the midband frequency of 915 MHz, it has a resolution of roughly about 35 KHz, achieving 12.5 effective bits of resolution. Fig. 22 shows the input return loss of the

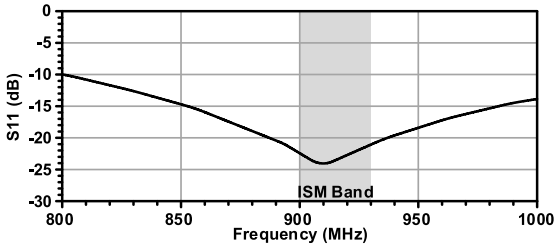

Fig. 22. Measured SRR input matching after tuning.

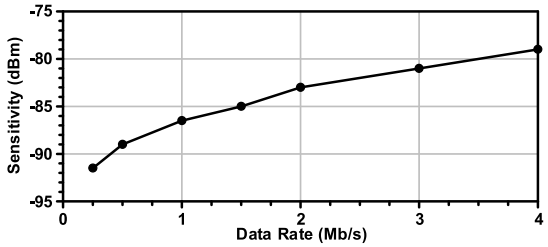

Fig. 23. Measured Sensitivity versus DR, while the ADC works as a simple comparator.

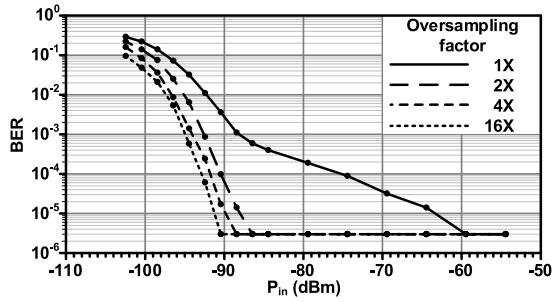

Fig. 24. Measured BER versus input signal power, for different oversampling factors ($f_q = 1$ MHz). As expected, oversampling improves the receiver sensitivity, and can be employed to tradeoff sensitivity and DR.

SR receiver. Fig. 23 shows the measured sensitivity of the SR receiver at BER $= 0.1\%$, for different DRs, and quench rate of twice as much. The quench signal is optimized at each DR point independently for the best sensitivity, in contrast to [26], in which the optimal quench signal shape at 1 Mb/s was scaled for the rest of DRs, accordingly. As expected, the sensitivity improves at lower DRs. In another approach the sensitivity and DR, as explained in Section III-B, can be traded off without the need for directly changing the quench rate of the SR receiver. Fig. 24 shows the receiver BER versus input signal power, for various oversampling factors, at constant quench rate $f_q = 1$ MHz. BER improves significantly at higher P_{in} level, and less considerably for very weak input signals, due the exponential relation between BER and SNR. This approach to tradeoff DR for sensitivity is very robust; the quench signal does not need to be optimized for a new data/quench rate. It can be optimized at a single sampling rate, and the ADC data can be used to restore the data at different DRs. The receiver becomes saturated for input signal as strong as -50 dBm.

To study the selectivity performance of the designed SRR, a single tone interferer, at different offset frequencies, was

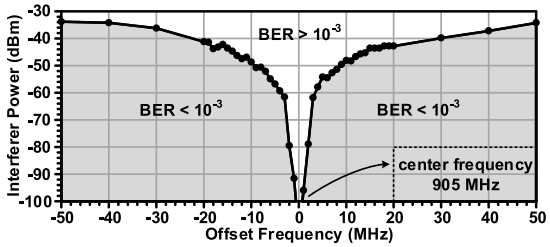

Fig. 25. Measured interferer rejection versus offset frequency. A single tone interferer was added to the OOK signal at 905 MHz and swept within ± 50 MHz, and BER was measured to find the interferer level at which BER falls below 10^{-3}.

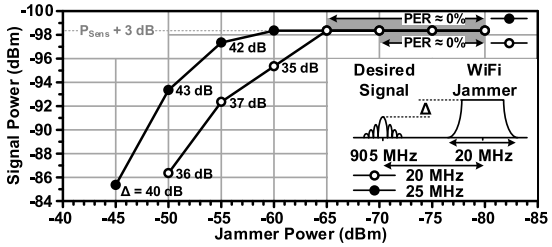

Fig. 26. Wideband interferer measurement. A wide interferer that emulates a non-overlapping Wi-Fi jammer was added to the desired OOK signal at 905 MHz, and data throughput 31.25 kbps ($f_q = 1$ MHz). The signal and interferer power level was measured for PER $<\%10$, in two cases: 1) the jammer is located 20 MHz apart, in which the jammer rejection is around 35 to 37 dB and 2) the jammer is located 25 MHz apart, in which the jammer rejection is around 40 to 43 dB. Note that for with $P_S = P_{\text{Sens}} + 3 = -98.5$ dBm and jammer power below -70, and -65 dBm the PER ≈ 0 , respectively.

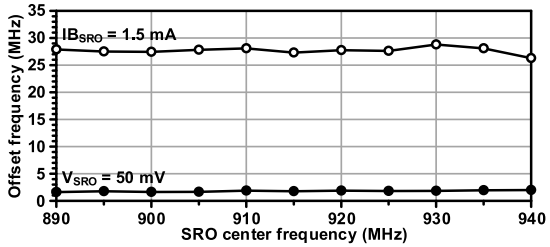

Fig. 27. SRO offset frequency, measured in two cases: 1) constant SRO bias current $\text{IB}_{\text{SRO}} = 1.5$ mA and 2) constant SRO oscillation amplitude $V_{\text{SRO}} = 50$ mV. The latter case not only results in smaller offset frequency, but also has less variation and the calibration phase in this case consumes 10 times less power.

applied to the receiver, while the desired signal is at $P_{\text{Sens}}+3 = -86$ dBm with a DR of 0.5 Mb/s. The receiver is tuned to work at 905 MHz, and a quench rate of 1 MHz. As seen from Fig. 25, the receiver can maintain a BER $\leq\%0.1$ for an interferer as strong as -50 dBm, when located 10 MHz apart. It is also conceivable that the SRR is incorporated as a Wi-Fi[7] WUR, therefore, the wideband interference behavior of the receiver is of interest. A Wi-Fi signal was generated and placed 20 and 25 MHz apart to emulate a non-overlapping channel interference. The receiver is tuned as described above, and the signal is sent in packets with a 512-bits-long preamble, and a DR of 31.25 kb/s. As seen from Fig. 26, the receiver

[7]Although Wi-Fi radio operates mainly in 2.4-GHz ISM band, as seen in Section II, the center frequency of the radio does not play a determining role in the performance of the SRR.

TABLE II
PERFORMANCE TABLE AND COMPARISON TO PRIOR WORKS

Publication	[21]	[20]	[19]	[15]	[24]	[17]	[39]	This Work
Year	2007	2009	2010	2011	2011	2013	2015	2016
Frequency (GHz)	2.4	0.4	2.4	2.4	0.9	0.4	2.4	0.9
Architecture	SRO	SRO	SRO	SRO	Inj. Lock	SRO	Low-IF	SRO
SRO resonator Intrinsic Q_0	On-Chip 10	Off-Chip >130	Bondwire NA	Bondwire NA	Off-Chip 13[1]	Off-Chip NA[2]	Off-Chip NA[3]	On-Chip 13
Single-ended RF Input	No	No	No	No	Yes	No	Yes	Yes
Modulation	OOK	OOK	BFSK	OOK	FSK	OOK	OOK	OOK
P_{Sens} (dBm) @ DR (kb/s)	-80 500	-99 40	-75 2000	-75 5000	-73 5000	-80 500	-83 1000	-86.5 1000
Rejection (dB) @ f_{offset} (MHz) @ DR (kb/s)	10 3 NA	27[4] 0.6 40	20 15 NA	NA	12 5 5000	15 3 1000	30 10 1000	23 3 500
Power (μW)	2800	400	350	534	420	123	227	320
Supply (V)	1.2	0.8	0.65	1.2	0.7	0.8	0.6	0.65
Active area (mm^2)	1	0.5	0.55	4.45[5]	1.65[5]	0.49	0.8	0.45
Technology (nm)	130	90	180	90	180	90	65	40
FOM[6]	192	209	207	205	204	206	209	212

[1]Five low-cost inductors.
[2]Two high-Q air coils.
[3]Three high-Q inductors.
[4]$P_{Sig} = P_{Sens} + 6$
[5]Total area including TX.
[6]$FOM = 10\log(DR/P_{DC}P_{Sens})$.

can provide up to 43 dB interferer rejection, and tolerate an interferer as strong as −45 dBm. Fig. 27 shows the offset between the frequency that is set by the calibration scheme, and frequency at which the SR receiver shows its maximum sensitivity. The calibration is being done in two scenarios: 1) the bias current of the SRO is kept constant at $IB_{SRO} = 1.5$ mA and 2) the amplitude of the oscillation is kept constant through the ALL at $V_{SRO} = 50$ mV. In the latter case, since the amplitude of the oscillation is always constant and fairly close to zero, the nonlinear parasitics of the SRO tank circuit do not vary considerably and the offset frequency is comparatively small (below 2 MHz). However, in the former case, due to larger oscillation amplitude, the offset is considerably larger. Note that although in the former case the offset is also almost constant, due to PVT variation it might slightly change for different chips or environments, and therefore even a 10% variation can be translated into 2 to 3 MHz of unpredictable offset, degrading the performance of the SR receiver.

The measurement process was run for about a year and the results and receiver's performance remained consistent over the course of this time. Although the receiver was not measured at extreme thermal conditions, it was mounted on a transceiver board along with a +33-dBm OOK transmitter that increased the ambient temperature considerably. The receiver's performance did not change by turning the transmitter on and off. Table II compares this work against the state-of-the-art. The FoM for this paper is calculated for DR = 31.25 kb/s case, and, to the best of the authors' knowledge, achieves the highest among reported SR receivers.

VI. CONCLUSION

An ULP-SRR was presented that in addition to being fully on-chip employs various calibration schemes to guarantee robust performance. Mathematical modeling and in-depth analysis of a SRO behavior, and, from that, an SRR was presented. This analysis enables one to estimate the receiver's BER at a given signal power, or sensitivity at a given BER. The receiver exploits low-voltage techniques to work with a 0.65-V supply, resulting an excellent energy efficiency of 80 pJ/b at the 4 Mb/s DR with a sensitivity of −79 dBm. An integration-oriented design has resulted in a receiver without either external inductor or balun. The receiver is using a 5-bit ADC to determine the amplitude of the incoming signal instead of a simple comparator, and this has enabled the receiver to tradeoff DR for sensitivity in the baseband post-processing stage, achieving an excellent sensitivity of −101.5 dBm at 31.25 kb/s DR and 43-dB wideband interferer rejection.

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