A *D*-Band Digital Transmitter with 64-QAM and OFDM Free-Space Constellation Formation

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***Abstract*— A *D*-band I/Q RF-DAC featuring two 6-bit DAC elements driven in quadrature, each with its own on-die antenna, and a total effective isotropic radiated power (EIRP) of 13.2 dBm, is demonstrated in a 45-nm SOI-CMOS technology. The carrier signal is first amplified by the 30-dB gain LO path and is directly modulated by the 12 baseband bit streams, without linear upconversion or power amplification. QPSK, 8-PSK, 16-QAM, 32-QAM, and 64-QAM single-carrier (SC) and OFDM constellations are formed in free space and measured above the die at data rates up to 12 Gb/s and at distances over 15 cm. The large-signal bandwidth—from the carrier input pad to the output of the transmitter above the antennas—is 130–142 GHz and was obtained by sweeping the frequency of the *D*-band external carrier, modulating it on die at 0.4 Gb/s using 16-QAM format, and measuring the error vector magnitude (EVM) with an instrumentation receiver. The highest data rate of 12 Gb/s was measured for QPSK SC modulation with a corresponding EVM of −12.2 dB. Lower maximum data rates of 7 Gb/s with −14.3-dB EVM and 3.6 Gb/s with −19-dB EVM were observed for 16-QAM and 64-QAM formats, respectively. Spectral shaping and OFDM transmission were also demonstrated at up to 2.5 Gb/s. The prototype consumes a total of 1.25 W, with an energy efficiency of 104 pJ/b.**

***Index Terms*— CMOS, digital transmitter, direct modulation, mm-wave, OFDM, QAM, RF-DAC, SOI.**

I. Introduction

FULLY digital mm-wave transmitters based on RF-DACs have been proposed in recent years as the potential solutions to improve the energy efficiency and to increase the data rate of mm-wave wireless terminals, because they do not require broadband linear upconversion and power amplifier (PA) back-off. Typically, the RF-DAC output stage operates in deep saturation at maximum efficiency. Until now, the mm-wave implementations of digital transmitters have been limited to simpler modulation formats, such as QPSK [1]–[6], 4-PAM [7], 8-QAM [3], 9-QAM [6], and 16-QAM [1], [2], [5], due to the difficulty of designing high modulation-depth digital modulators at mm-wave frequencies.

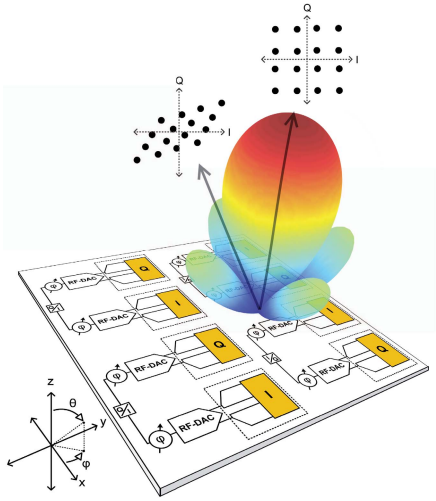

Fig. 1. Free-space constellation formation concept.

In this paper, we expand on the highest frequency and the highest modulation order digital mm-wave transmitter introduced in [8]. The circuit was implemented in a 45-nm SOI-CMOS process and features a new digital I/Q RF-DAC architecture with free-space quadrature summation of independently amplitude- and phase-modulated carrier signals (Fig. 1). The key benefit of spatial combining is that the transmitter output power and the link budget gain 4–5 dB from the array factor and from averting the losses of on-chip passive power combiners. The transmitter also features transistor gate segmentation in the RF power-DAC output stage, which, for the first time, allows for the demonstration of 64-QAM single-carrier (SC) and OFDM transmission at *D*-band without upconversion. The carrier frequency selected in this paper is based on the requirements for Phase III of the DARPA ELASTx program [9].

This RF-DAC is different from our previous work at *W*-band [6], [10] and 45 GHz [11], which use a switched-PA output stage without transistor segmentation and would require ≥14 antenna elements to synthesize 64-QAM signals. Compared to those RF-DACs, the proposed architecture suffers from a reduction in the PAE when averaged over all transmitted signal constellations because, unlike a switched-PA or a

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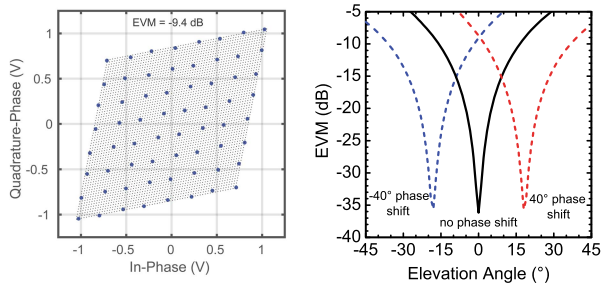
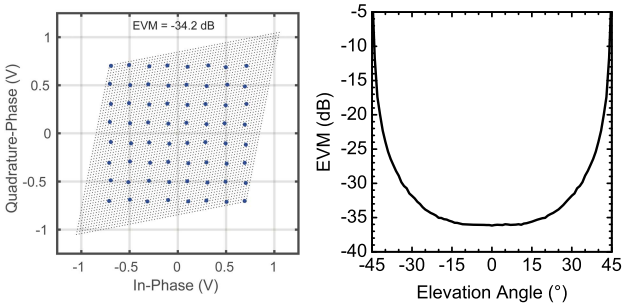


(a) (b)

Fig. 2. (a) Spatially distorted 64-QAM constellation as seen by a receiver located at $\theta = 10°$ (elevation), $\phi = 45°$ (azimuth). (b) Simulated EVM for an OFDM 64-QAM signal as a function of elevation angle. Dashed curves: beam steering with $\pm 40°$ phase shifts between the I and Q transmit elements.



(a) (b)

Fig. 3. (a) 64-QAM constellation with digital phase correction as seen by a receiver located at $\theta = 10°$ (elevation), $\phi = 45°$ (azimuth). (b) Simulated EVM for an OFDM 64-QAM signal with digital phase correction as a function of elevation angle.

digital-PA output stage, the proposed RF-DAC output stage uses a Gilbert-cell-based amplitude modulator that is always fully biased, trading off back-off efficiency for the increased modulation speed. At lower frequencies, where antennas are bulky and transistors exhibit higher power gain and isolation, this concept can be implemented by direct on-chip I/Q summation in the output stage, as recently demonstrated for a multi-octave 1–32-GHz RF-DAC [12].

In addition to the material covered in [8], this paper presents a detailed analysis of the impact of modulation depth and beam steering on system performance, as well as the transistor-level schematics of all blocks and new measurement results.

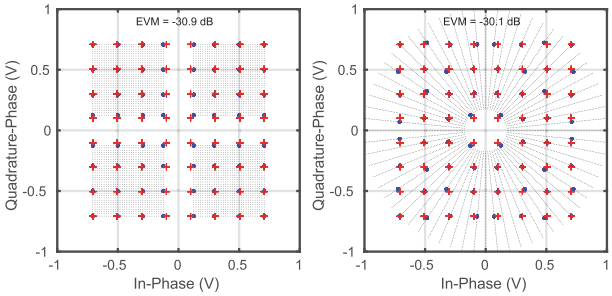
II. System Considerations

A. Free-Space Constellation Formation

In this paper, free-space constellation formation is used to avoid the insertion loss and poor isolation of on-die I/Q passive summation circuits at >100 GHz and to benefit from the array factor gain, which increases the maximum transmit power level beyond what is possible with on-chip power combining. The isolation between antenna elements, greater than the isolation of an on-chip power combiner, minimizes the parasitic load pulling between the in-phase (I) and the quadrature-phase (Q) RF-DAC elements and reduces the impact of their output impedance variations.

Despite its benefits, as illustrated in Fig. 1, this I/Q RF-DAC concept suffers from a deterministic distortion of the transmitted symbols when received at a location away from the intended direction of transmission. The latter phenomenon occurs, because the independently modulated I- and Q-carrier signals add at the desired phase only along a single direction or plane. It was first reported in [1] and is absent in traditional phased arrays. Nevertheless, it can be corrected in an I/Q array by incorporating dedicated phase shifters in each transmit element. The phase correction is supplementary to the fixed phase difference introduced by the I/Q hybrid used to generate the I and Q LO phases.

The deterministic symbol distortion is illustrated in Fig. 2(a) for a 64-QAM constellation as the receiver is moved by 10° along the elevation plane (θ in Fig. 1) away from the desired location. Fig. 2(b) plots the error vector magnitude (EVM) at different elevation angles from which a −20-dB information beamwidth [1] of ±5° along the elevation plane can be determined. Fig. 2(b) also demonstrates that the information beamwidth can be readily steered by introducing relative phase shifts between the I and Q elements. Since the individual I and Q elements are independently modulated, the spacial distortion can be corrected if the location of the receiver is known *a priori*. Fig. 3(a) illustrates how the digital phase correction can be applied for a 64-QAM constellation whereas Fig. 3(b) demonstrates correction for an OFDM 64-QAM signal for different angles of reception. The EVM degradation that can be observed in Fig. 3(b) when the receiver is displaced from the 0° position is a result of quantization noise since a smaller portion of the total number of symbols can be used.



(a) (b)

Fig. 4. 64-QAM constellation modulated with (a) ideal 2 × 6-bit I/Q transmitter with 15-dB modulation depth and (b) ideal 6 + 6-bit polar transmitter with 15-dB modulation depth.

B. Modulation Depth

An important but often overlooked metric in digital transmitters is the modulation depth, which is defined as the ratio of maximum to minimum amplitude levels that can be generated ($\text{MD} = V_{tx,\max}/V_{tx,\min}$). A low modulation depth manifests itself as LO leakage and increased EVM for the low amplitude symbols. This is illustrated for both the digital I/Q architecture and the digital polar architecture [13] in Fig. 4, where the 64-QAM signals are modulated with 15 dB of modulation depth. The modulation depth is especially important at mm-wave frequencies where most transistors have poor isolation due to increasing signal leakage through C_{gd} and C_{ds}.

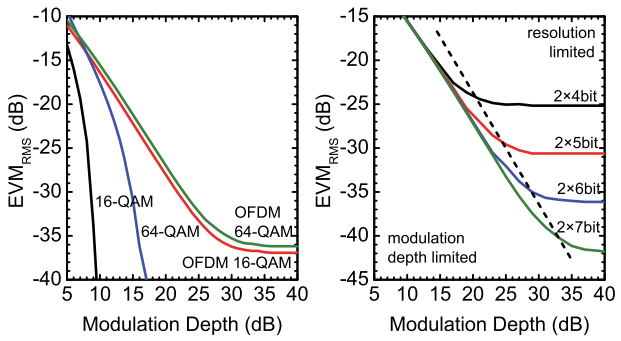


Fig. 5. Simulated EVM as a function of (a) modulation depth and modulation format and (b) modulation depth and the number of bits. The bits are encoded as 1's complement, i.e., 1 sign bit $+ n - 1$ magnitude bits for each I and Q RF-DAC.

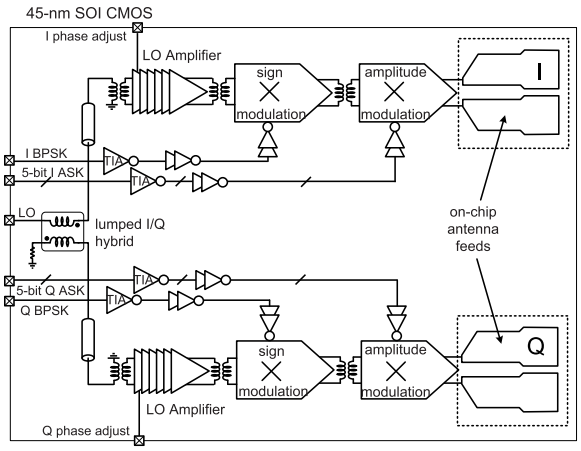


Fig. 6. Block diagram of the 130–142-GHz I/Q RF power-DAC.

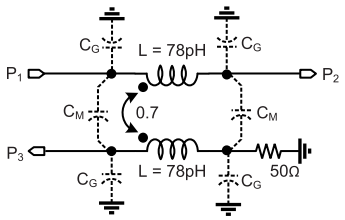


Fig. 7. Schematic of the lumped transformer-based I/Q hybrid.

The modulation depth requirements for a digital transmitter depend on the characteristics of the signals that need to be generated. Fig. 5(a) illustrates the impact of modulation depth on the EVM for SC signals as well as for multi-carrier OFDM signals. The general trend is that the high dynamic range signals and signals with large peak-to-average power ratios (PAPRs) require larger modulation depth. This is particularly relevant for the OFDM signals since they are characterized by even larger PAPRs.

As shown in Fig. 5(b), the EVM of a digital I/Q transmitter can either be modulation depth limited or resolution limited. For OFDM signals, an insufficiently high modulation depth increases the quantization noise as if the resolution of the I/Q RF-DAC was too low. The higher quantization noise appears both as degraded EVM and higher spectral emissions in the adjacent channels.

Finally, it should be noted that the EVM and the effective number of bits (ENOB) are related alternative parameters that characterize the SNR. However, unlike EVM that describes the modulation accuracy of a signal with a high PAPR, ENOB characterizes the modulation accuracy of a sinusoid.

C. Two-Stage Modulation Architecture

Unlike the *W*-band circuit in [14], where the modulation of the carrier signal was performed in the output stage, in this paper it is split over two stages—a sign (BPSK) modulator followed by a single-quadrant amplitude modulator [12], [15]. The advantage of the two-stage modulator architecture is threefold: 1) it reduces the number of devices that are off in the output amplitude modulation stage, which in turn reduces the capacitive losses and improves the PAE; 2) it avoids the asymmetries introduced by the inductive layout parasitics of the Gilbert cell since only single-polarity amplitude symbols need to be generated in the output stage; and 3) it has smaller footprint and smaller *LC* delay differences between transistor segments, allowing for a higher modulation depth. The BPSK modulator is placed first, because it can operate in saturation mode, without distortion. By applying the amplitude modulation in the last stage, the power output stage and all the preceding circuits can be operated deep into saturation, at maximum PAE, with minimal distortion and maximum modulated carrier bandwidth. Nevertheless, since the output stage is biased at constant current and has a more complex topology, its efficiency is lower than that of a switched power amplifier, even when saturated.

The block diagram of the proposed proof-of-concept two-element I/Q RF-DAC is shown in Fig. 6. It consists of two 6-bit RF-DAC elements, each with its own differential antenna. The external *D*-band carrier (LO) signal is first split into quadrature phases by an on-die 90° hybrid and then amplified by the LO amplifiers in each DAC element. The twelve independent data bit streams are provided through an on-chip high-speed 50Ω-matched interface which is realized with the transimpedance amplifiers.

III. Circuit Design

A. LO Distribution

The lumped I/Q hybrid is based on the transformer topology shown in Fig. 7, which was first proposed in [16] at GHz frequencies and was later scaled to the *W*-band [14], [17], [18]. Equations (1)–(2) are used to establish the required coil inductances (L) and coupling factor (k) for the symmetric transformer [16]. Unlike [16], the lumped mutual capacitances (C_M) and capacitances to ground (C_G) are fully absorbed into the parasitics of the transformer layout. The transformer layout geometry, coil width, and coil spacing to the ground plane are adjusted with the help of an EM simulator [19] to obtain the required parasitic capacitances as per (3) and (4). A square transformer geometry is preferred over an octagonal layout to take advantage of charge crowding

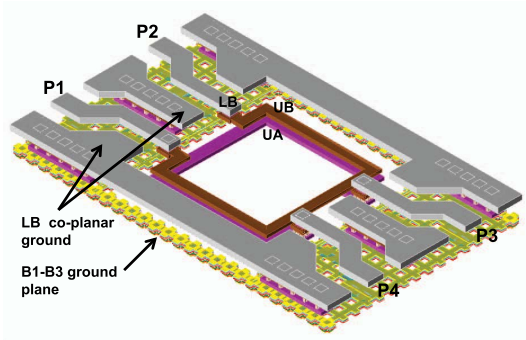


Fig. 8. To-scale 3-D layout view of the 138-GHz I/Q hybrid.

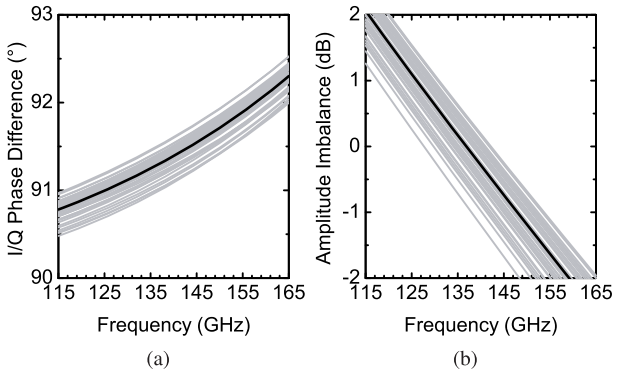


Fig. 9. Monte Carlo simulation of the 3-σ variation of (a) phase difference and (b) amplitude imbalance of the 138-GHz I/Q hybrid.

near the corners, which contributes to C_M and C_G.

$$k = \frac{1}{\sqrt{2}} \tag{1}$$

$$L = \frac{Z_0}{2\pi f_0 \sqrt{1-k^2}} \tag{2}$$

$$C_M = \frac{Lk}{Z_0^2} \tag{3}$$

$$C_G = \frac{L(1-k)}{Z_0^2} \tag{4}$$

A 3-D rendering of the 138-GHz I/Q hybrid is shown in Fig. 8. The total area of the transformer is $48.5 \times 48.5\ \mu\text{m}^2$. The primary/top coil of the transformer (UB layer) is made narrower than the secondary/bottom coil (UA layer) to compensate for the additional inductance introduced by the vias needed to contact the bottom coil. The input/output ports of the hybrid are contacted with grounded coplanar waveguides, G-CPW, formed in the top Alucap layer, LB, and which are used to route the LO signals. Monte Carlo simulations with 40 iterations were conducted to predict the impact of process variation on the amplitude imbalance and phase difference of the I/Q hybrid across the 115–165-GHz frequency range and are shown in Fig. 9. When 3-σ deviations in the metal and dielectric layer thicknesses are considered, the phase error and amplitude imbalance remain lower than 0.52° and 1 dB, respectively.

B. D-Band LO Amplifier

The schematic of the LO amplifier is reproduced in Fig. 10 and consists of six gain stages. The MOSFETs in the first stage are sized such that it can be matched to the 50-Ω input line through a transformer, which also performs single-ended to differential signal conversion. The role of the next three stages is to provide sufficient amplification and common-mode rejection without consuming excessive dc power. Fig. 11(a) reproduces the measured MSG of fully wired n-MOSFETs and p-MOSFETs with 780-nm gate finger widths throughout the *D*-band. The power gain of both transistors remains higher than 6 dB up to 170 GHz and is comparable or larger than the MAG of the best SiGe HBTs in this frequency range [20]. To further maximize the power gain per stage, all the LO amplifier stages feature differential cascodes biased at a drain current density of 0.29 mA/μm from a 1.1-V supply. The last two stages are each scaled by a factor of 2 to fully saturate the BPSK and ASK modulation stages. Transformers are used for interstage matching, dc biasing, and dc blocking. The matching networks separating the 10-mA stages also include a 10-fF capacitor placed in shunt. This capacitor is introduced to reduce the transformer ratio from two (130:70 pH) to one (70:70 pH), which is easier to form in the 45-nm SOI-CMOS back end. Including the insertion loss of the transformers, each stage provides >4 dB of gain for a total of 26 dB of small-signal gain [Fig. 12(a)].

Phase tuning is introduced in the LO amplifier by replacing the 10-fF capacitor of the first stage with a pair of $40 \times 0.78\ \mu\text{m} \times 40$ nm accumulation-mode MOS varactors. The simulated phase adjustment as a function of varactor control voltage is reproduced in Fig. 12(b). A phase adjustment of ±9.5° is possible with this scheme at 138 GHz with a corresponding small-signal amplitude error of ±2 dB. Similarly as for the I/Q hybrid, some small-signal amplitude error can be tolerated since the whole transmitter is operated in deep saturation. Fig. 12(a) reproduces the simulated large-signal gain of the amplifier at the two extremes of the phase adjustment range.

C. Direct Sign and Amplitude Modulators

The sign (BPSK) and amplitude (ASK) power modulator stages, shown in Fig. 13(a) and (b), are implemented with a common-gate Gilbert cell topology with series stacking. The modulator topology is termed *common-gate* since the input signal is applied directly to the source terminals of the Gilbert cell quad transistors through a transformer. This arrangement is selected instead of a Gilbert cell topology with bottom common-source devices [7], [14] since the quality factor of the input impedance looking into the source terminals of the common-gate Gilbert cell is lower at *D*-band, allowing for a wider bandwidth inter-stage matching network. The operation of the modulators is based on digitally modulating their large-signal transconductance. For the BPSK modulator, only the sign of the transconductance is modulated

$$G_m(b_{\text{sign}}) = G_m(-1)^{b_{\text{sign}}}. \tag{5}$$

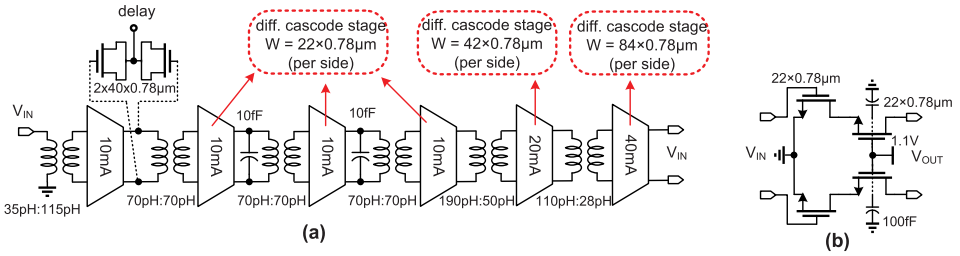


Fig. 10. (a) Block diagram of the *D*-band LO amplifier. (b) Schematics of the 10-mA LO stage.

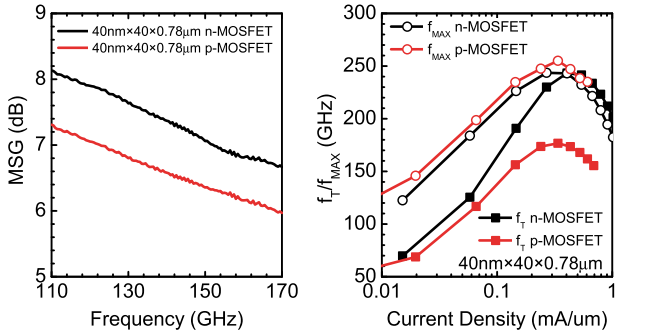


Fig. 11. Measured (a) MSG versus frequency and (b) f_{MAX}, f_T versus I_{ds}/W characteristics of 40×40 nm $\times$ 780 nm n-MOSFETs and p-MOSFETs.

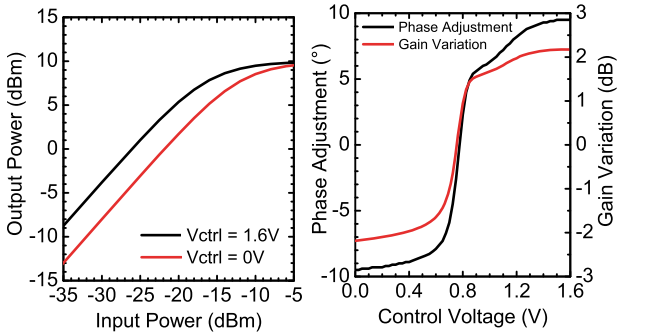


Fig. 12. (a) Simulated large-signal transfer characteristics of the LO amplifier. (b) Simulated phase adjustment and small-signal gain variation of the LO amplifier as a function of control voltage.

The ASK modulator stage is realized as a single-quadrant Gilbert cell by adding the common-gate MOSFETs M_5 and M_6, which provide a fixed transconductance, in parallel with MOSFETs M_1-M_4, which are used to modulate the transconductance. The latter are segmented into binary-weighted groupings of 1, 2, 4, 8, and 16 gate fingers, each controlled by a separate bit stream, b_0 to b_4. For the highest amplitude code, the signal passing through the fixed transconductance MOSFETs M_5 and M_6 adds constructively with the signal passing through M_1 and M_4, whereas for the lowest amplitude code, M_1 and M_4 are switched OFF and the signal passing through M_3 and M_2 cancels a portion or all of the signal through the fixed transconductance MOSFETs M_5 and M_6. The code-dependent transconductance of the ASK modulator stage can therefore be expressed as

$$G_m(b_0,\ldots,b_{n-1}) = G_{m,\mathrm{fixed}} - G_m^{'}\left(\sum_{i=0}^{n-1}(-1)^{b_i}2^i\right). \quad (6)$$

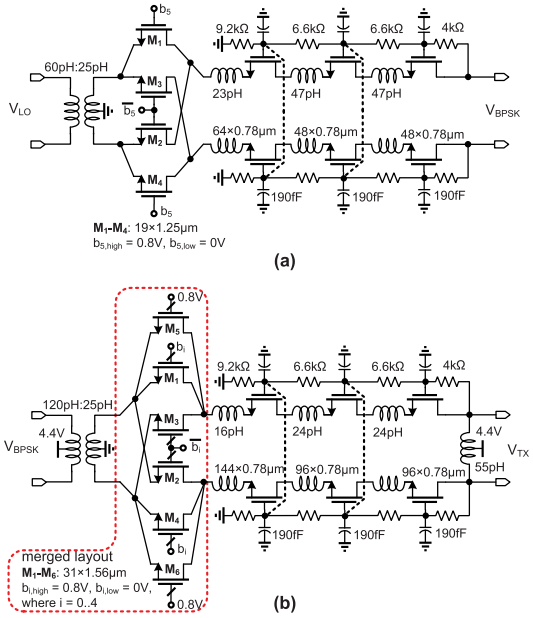


Fig. 13. Schematic of (a) stacked sign modulator and (b) stacked output stage used for 5-bit ASK modulation.

For maximum modulation depth, the gates of $M_{5,6}$ are sized with the same widths as the total of all the binary-weighted gate segments of $M_{1,2,3,4}$ reducing the modulation function to

$$G_m(b_0,\ldots,b_{n-1}) = G_m^{'}\left(2^n - 1 - \sum_{i=0}^{n-1}(-1)^{b_i}2^i\right). \quad (7)$$

As shown in Fig. 14, to minimize parasitics and device mismatch, all MOSFETs that form the amplitude modulator core are laid out as a single active area ($6 \times 31 \times 1.56\ \mu$m $\times$ 40 nm). Wide source and drain straps in the top copper metal layer are used to connect all the segments and to minimize the inductive parasitics. The latter are critical for delay matching all the segments and maximizing the modulation depth [14].

By placing appropriately sized capacitors between the gates of the MOSFETs in the stack and ground, the gain and voltage swing at the output of the series stack are maximized [21] while simultaneously achieving broadband large-signal matching to the antenna impedance. The dc voltage drop per transistor remains 1.1 V, within the recommended safe operating region of the MOSFETs. At *D*-band, three series-stacked devices proved optimal in maximizing the gain and output power for both the BPSK and ASK modulator stages.

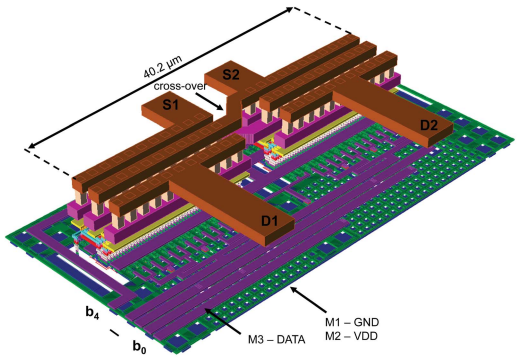


Fig. 14. To-scale 3-D layout of the 138-GHz segmented Gilbert cell.

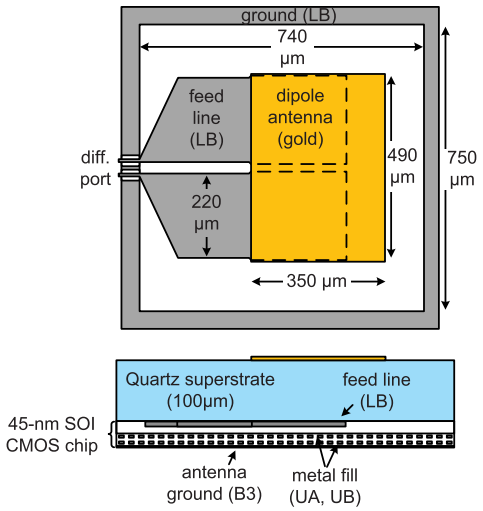


Fig. 15. Layout and cross section of the 138-GHz differential dipole antenna.

D. Antenna

The differential dipole antenna topology from [22] was selected and is shown in Fig. 15. It is based on the single-ended antenna first introduced in [23] and is preferred because it avoids the lossy differential-to-single-ended conversion that would degrade the power-added efficiency of the transmitter. The dipole antenna was formed by a gold-plated quartz superstrate placed on top of the silicon chip. An on-chip feed layer is used to electromagnetically couple the antenna without the need of a direct ohmic contact, thereby increasing its efficiency while keeping a simple planar fabrication procedure. This arrangement allows for an on-chip ground plane to shield from the dielectric and modal losses of the silicon substrate [24].

The optimum superstrate thickness in terms of radiation efficiency for this frequency range is 50 μm [25]. However, a 100-μm superstrate thickness was selected to maximize the bandwidth, critical to achieve high data rates, at the expense of $\approx$10% degradation in radiation efficiency. As shown in Fig. 16, the simulated antenna gain is 1.85 dBi and the efficiency is 34%.

IV. Experimental Results

The circuit was manufactured in a 45-nm SOI-CMOS process with eleven metal layers, two of which are

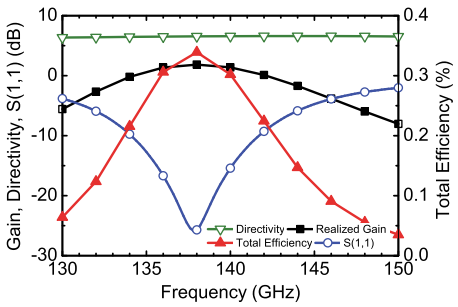


Fig. 16. Simulated antenna gain, directivity, reflection loss, and efficiency as a function of frequency. An 100-Ω port impedance is used for the S_{11} simulation.

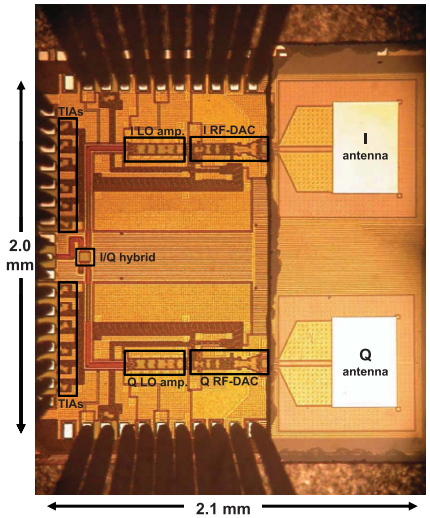


Fig. 17. Die micrograph of the 138-GHz I/Q power-DAC chip-quartz assembly.

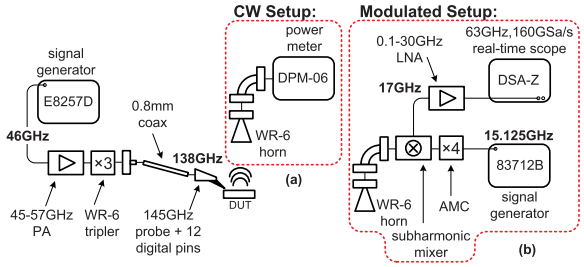
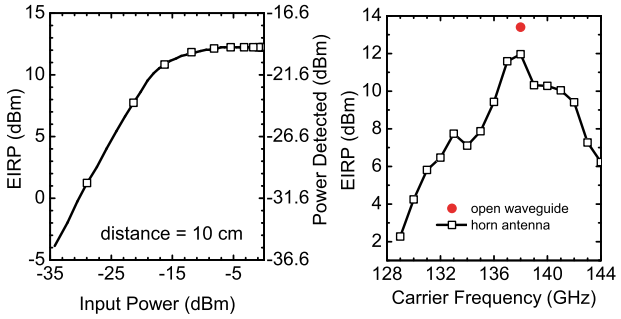


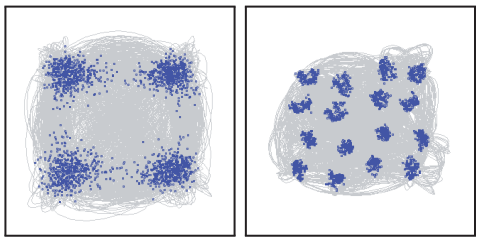
Fig. 18. Free-space measurement setups for (a) continuous wave (CW) output power and (b) modulated (multi-)carrier spectra and EVM.

1.2-μm-thick Cu layers and the top is a 2.2-μm-thick Al layer. The measured f_T/f_{MAX} of the fully wired n-MOSFETs and p-MOSFETs with 780-nm gate finger widths are 243/244 and 178/255 GHz, respectively [Fig. 11(b)]. The total die area, including the on-die antenna feeds and all pads, is 2.0 $\times$ 2.1 mm^2. The quartz superstrate containing the differential dipole antennas was fabricated separately and was manually positioned on the SOI-CMOS chip. A microphotograph of the chip-quartz assembly is reproduced in Fig. 17. The measurements were conducted on die, through the air, at distances up to 15.2 cm, using the setups in Fig. 18(a) and (b).



(a) (b)

Fig. 19. Measured (a) EIRP versus input power at 138 GHz and (b) EIRP versus frequency.



QPSK, -12.2 dB EVM, 6 GSym/s, 12 Gb/s

16-QAM, -14.6 dB EVM, 1.25 GSym/s, 5 Gb/s

Fig. 20. Measured constellations at 135 GHz and a distance of 10 cm for QPSK and 16-QAM signals without DPD. The EVM is normalized to the signal rms value.

To establish the center frequency of the circuit and the correct drive level for the input LO signal, the output power was measured for an unmodulated carrier above the die, as shown in Fig. 18(a). A *D*-band power sensor was used directly in order to minimize de-embedding and calibration uncertainties. Peak effective isotropic radiated power (EIRP) values of 12.2 and 13.2 dBm were obtained with a 23.8-dBi rectangular horn and with an open waveguide, respectively. The antenna gain of the open waveguide was calculated through the effective aperture ($A_e = 0.81$ ab [26]) with

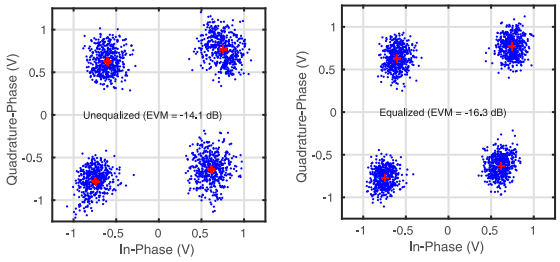
$$G_{\text{open-waveguide}} = \frac{4\pi A_e}{\lambda^2} = \frac{4\pi (0.81 \cdot ab)}{\lambda^2}. \tag{8}$$

The effective aperture at 138 GHz for a WR-6 waveguide ($a = 1.651$ mm and $b = 0.8255$ mm) results in an antenna gain of 4.7 dBi. The EIRP averaged over several measurements at different heights up to 69 mm was 13.2 dBm. Accurate measurements beyond 69 mm were not possible due to the lower antenna gain of the open waveguide and limited sensitivity of the power sensor.

The setup loss up to the probe tips, at the LO input of the die, was measured from 110 to 170 GHz with a two-tier VNA calibration and de-embedded to establish the exact input power. From the bottom-left corner of Fig. 19(a), the EIRP-P_{in} gain is 32.4 dB. By accounting for the on-chip antenna gain, the $P_{\text{out}}-P_{\text{in}}$ gain is 30.6 dB. The measured EIRP versus frequency is shown in Fig. 19(b) with a peak-EIRP value occurring at 138 GHz.

In the modulated carrier measurements, the power meter was replaced with a subharmonic LO down-convert mixer whose IF output is amplified and displayed on a 63-GHz bandwidth real-time oscilloscope, as shown in Fig. 18(b). The twelve data streams come from off-chip and were manually aligned with the 1-ps adjustment accuracy of the external pattern generator. The total noise figure of the down-convert mixer and IF amplifier used in the experiments was 11 dB. For the initial modulated measurements without corrections, a carrier frequency of 135 GHz was selected since it is where the on-chip I/Q hybrid has the least amount of intrinsic imbalance. The measured QPSK and 16-QAM constellations are reproduced in Figs. 20 and 21(a) achieving a data rate of 12 Gb/s for QPSK and 5 Gb/s for 16-QAM. To separate the linear from the non-linear EVM contributions, the QPSK constellation in Fig. 21(a) was also equalized with a linear 14-tap FIR filter computed in MATLAB through an LMS algorithm. Fig. 21(b) shows the equalized constellation, which has 2.2-dB improvement in EVM. The remaining −16.3 dB EVM is most likely due to non-linear contributions and would require a non-linear memory digital pre-distortion (DPD) algorithm.

To correct for the modulation accuracy and increase the modulation order, a memory-less DPD based on a 2-D lookup



(a) (b)

Fig. 21. Measured constellation at 135 GHz for QPSK at 10 Gb/s (5 GSym/s) (a) before and (b) after linear equalization.

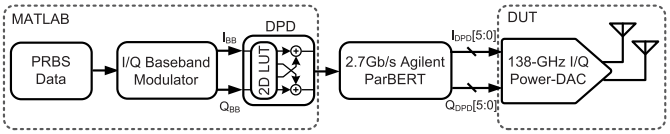
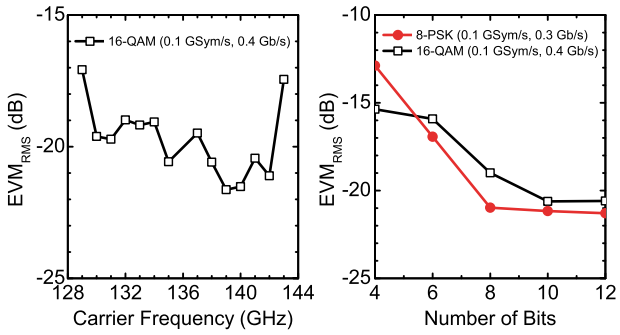


Fig. 22. Block diagram of the setup used for DPD measurements.



(a) (b)

Fig. 23. Measured (a) EVM of a 16-QAM signal versus carrier frequencies and (b) EVM of 138-GHz, 16-QAM, and 8-PSK signals with DPD versus the total number of I and Q bits used. The EVM is normalized to the signal rms value.

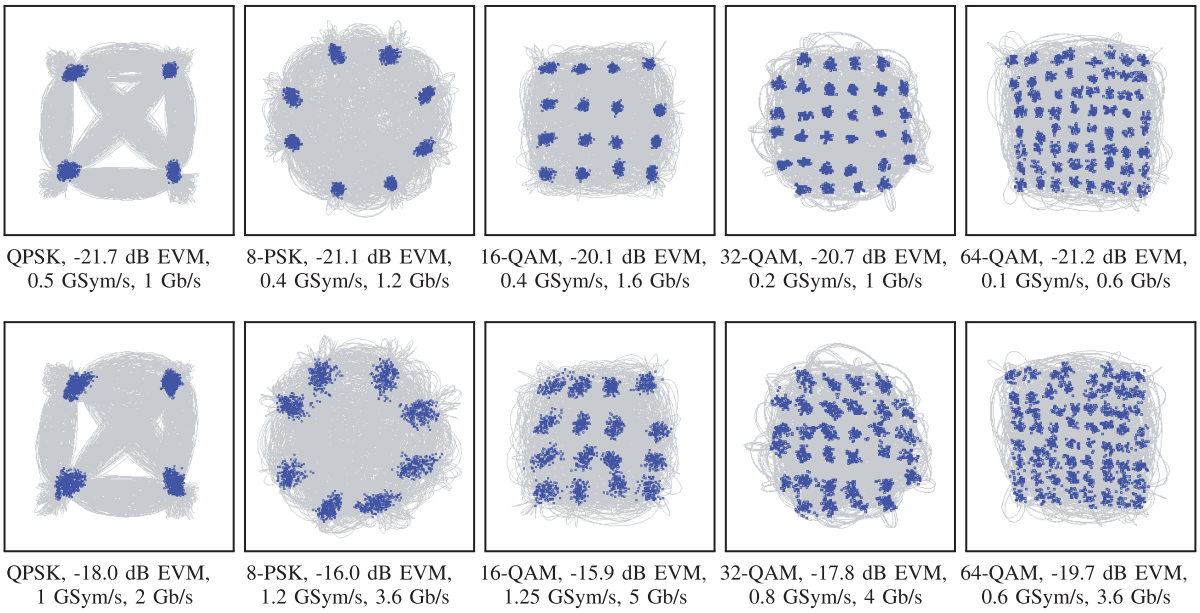
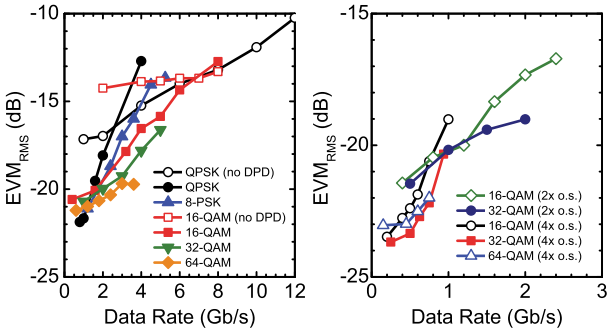
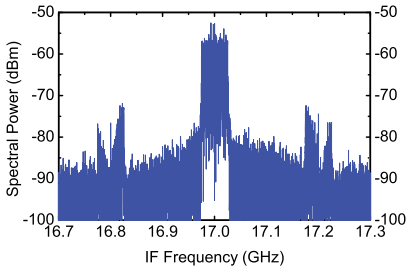


Fig. 24. Measured constellations at 138 GHz and at a distance of 10 cm for various modulation formats and data rates with DPD. The EVM is normalized to the signal rms value.

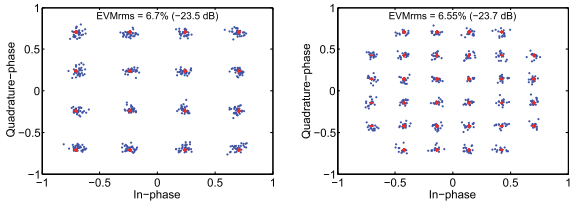


(a) (b)

Fig. 25. Measured EVM versus data rate at 138 GHz for (a) various single-carrier modulation formats and (b) various OFDM signals with oversampling ratios of 2 and 4, respectively.



(a)



(b) (c)

Modulation Format	16-QAM OFDM	32-QAM OFDM
FFT/Sampling Rate	200 MHz	200 MHz
RF Bandwidth	50 MHz	50 MHz
SCS	781.25 kHz	781.25 kHz
Data Rate	200 Mb/s	250 Mb/s
# Sub-carriers	64	64
FFT Length	256	256
Effective Oversampling Ratio	4	4

(d)

Fig. 26. (a) Measured spectra of a 138-GHz OFDM signal with a 200-MHz FFT rate. Measured constellations for (b) 138-GHz 16-QAM OFDM signal and (c) 138-GHz 32-QAM OFDM signal. (d) Summary of the OFDM signal characteristics. The EVM is normalized to the signal rms value.

table (2-D-LUT) was used in all the remaining measurements. A block diagram of the setup used for the DPD measurements is shown in Fig. 22. The LUT training was done by running a calibration sequence and recovering the resulting I and Q signals with the external down-converter and real-time oscilloscope from Fig. 18(b). The calibration sequence involved triggering the oscilloscope with a large pulse generated by the DUT and then sweeping through all I/Q code words at a relatively slow rate (e.g., 100-MHz rate). A serpentine trajectory was selected for an I/Q sweep to minimize large jumps that may introduce error.

Using DPD, the EVM of a 0.4-Gb/s 16-QAM signal was measured at different carrier frequencies to precisely characterize the frequency range over which the I/Q RF-DAC can transmit with high modulation accuracy. As shown in Fig. 23(a), an EVM better than −19.2 dB was achieved from 130 to 142 GHz. The measured EVM for 8-PSK and 16-QAM modulation formats versus the total number of I and Q bits used are summarized in Fig. 23(b). The results show that in this frequency range, there is a little benefit to using more than 8 bits (4 I and 4 Q bits) to transmit an 8-PSK signal

TABLE I
STATE-OF-THE-ART DIGITAL TRANSMITTERS AT >60 GHz

Ref.	Tech.	TX Architecture	Freq. (GHz)	Modulation Format	Data Rate (Gb/s)	EVM_{RMS} (dB)	Antenna	# of Antennas	Peak EIRP (dBm)	Back-off (dB)	P_{DC} (mW)
This work	45nm SOI CMOS	I/Q RF-DAC	130 - 142	OFDM 64QAM 32QAM 16QAM QPSK	3.6 (64QAM) 7 (16QAM) 12 (QPSK)	-19.7 (64QAM) -14.3 (16QAM) -12.2 (QPSK)	on-chip with Quartz superstrate	2	13.2	0	1255
[8]	45nm SOI CMOS	I/Q Switched-PAs	100	9QAM QPSK	10 (QPSK)	-11.9 (QPSK)	on-chip with Quartz superstrate	2	15.7	0	1270 (QPSK)
[3]	40nm CMOS	I/Q Modulator	114	8QAM QPSK	10 (QPSK)	-9.3 (QPSK)	wirebond	1	5.6*	0	220
[7]	32nm SOI CMOS	I/Q RF-DAC	94	4PAM QPSK	20 (QPSK)	-12.4 (QPSK)	no	--	4**	0	220
[1]	65nm CMOS	I/Q RF-DAC	60	16QAM QPSK	6 (QPSK)	-16.2 (QPSK)	on-PCB	8	22	6	382
[5]	40nm CMOS	Polar RF-DAC	60	16QAM QPSK	6.7 (16QAM)	-18.1 (16QAM)	no	--	10.8**	5	70***

*Estimated from information available in the paper, **Saturated output power measured on-chip
***Excludes contribution of baseband

and more than 10 bits (5 I and 5 Q bits) to transmit a 16-QAM signal.

DPD also made it possible to transmit higher order modulation formats, such as 32- and 64-QAM. Free-space constellations measured at 10 cm above the die for various SC modulation formats are reproduced in Fig. 24. Systematic distortion in the constellations can be observed when comparing the same modulation format at different data rates. These were most likely caused by LO drifts during the LUT calibration procedure since they appear greater that an LSB. This source of distortion can likely be eliminated by employing an iterative calibration procedure as it was done in [12]. The EVM degradation with increasing data rate can likely be alleviated through the use of a memory-based DPD algorithm. It should be noted that for cases where the symbols begin to merge, the EVM metric from the Keysight VSA is optimistic since it does not correctly account for the impact of erroneous symbols. The EVM of the measured constellations, with and without DPD, are summarized in Fig. 25(a) for data rates up to 12 Gb/s. The highest data rate was achieved with QPSK modulation.

Multi-carrier QPSK, 16-QAM, 32-QAM, and 64-QAM OFDM signals were also successfully generated with the I/Q RF-DAC and recovered by the real-time oscilloscope. The downconverted spectra and the EVM of 138-GHz 16-QAM and 32-QAM OFDM signals with 0.2-GHz FFT rates are shown in Fig. 26. From the measured EVM of -23.7 dB and the simulation results in Fig. 5(b), the ENOB is approximately 2×4 bit. The maximum data rate of 2.4 Gb/s was achieved for OFDM signals with 16-QAM modulation format and -16.7 dB EVM. Fig. 25(b) shows the EVM results as a function of data rate for various OFDM signals. Higher OFDM data rates were achieved by increasing the FFT rate and/or by increasing the number of sub-carriers (i.e., reducing the effective oversampling ratio).

The total power consumption is 1.25 W, with an energy efficiency of 104 pJ/b for QPSK, 125 pJ/b for 16-QAM, and 312 pJ/b for 32-QAM formats. The performance of the proposed I/Q RF-DAC is summarized and compared with the state of the art in Table I.

V. CONCLUSION

A 2×6-bit I/Q RF power-DAC transmitter with on-die antennas was demonstrated for the first time at 138 GHz. This circuit is the only one to achieve direct 64-QAM and OFDM modulation of a mm-wave carrier without upconversion or back-off. The highest data rate of 12 Gb/s was obtained with SC QPSK modulation. Multi-carrier QPSK, 16-QAM, 32-QAM, and 64-QAM OFDM signals were also successfully formed in free space, above the die, and recovered at a maximum data rate of 2.4 Gb/s for 16-QAM OFDM. The >30 dB of gain and 13.2 dBm EIRP were made possible at more than half the f_{MAX} frequency of the 45-nm SOI-CMOS technology through the use of series-stacked supercascode topologies.

As expected, the SC and OFDM transmission measurements show that the EVM degrades with increasing data rates and that the achievable data rates are lower for higher order modulation formats. It is clear from these experiments that a larger number of bits are needed to achieve better EVM and higher data rates when using 32-QAM, 64-QAM, and OFDM modulation format. In addition, it should be mentioned that the data rate and bit efficiency are largely limited by the antenna bandwidth and not by the RF power-DAC architecture or circuit topologies. Both will improve with wider bandwidth antennas.

Although the overall power consumption is high, in a transmitter implementation with on-chip VCO and PLL, most of the 140-GHz LO tree blocks, introduced here for testing purposes, would be removed, reducing power consumption. Moreover, this architecture is easily scalable to more advanced CMOS nodes. Measurements of 22-nm FDSOI building blocks at *W*- and *D*-band show that the power consumption of the LO tree and of the digital circuits will continue to decrease because of the power supply reduction from 1.1 to 0.8 V.

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Sorin P. Voinigescu (M'90–SM'02–F'17) holds the Stanley Ho Chair in Microelectronics and is the Director of the VLSI Research Group in the Electrical and Computer Engineering Department at the University of Toronto which he joined in 2002. He received the MSc degree in electronics from the Polytechnic Institute of Bucharest, Romania, in 1984, and the PhD degree in electrical and computer engineering from the University of Toronto, Canada, in 1994. During the 1984–1991 period, he worked in microwave and quantum semiconductor device and circuit research, and as an Assistant Professor in Bucharest. Between 1994 and 2002 he was first with NORTEL and later with Quake Technologies in Ottawa, Canada. In 2008–2009 and 2015–2016, he spent sabbatical leaves at Fujitsu Laboratories of America, Sunnyvale, California, at NTT's Device Research Laboratories in Atsugi, Japan, at UNSW in Sydney, Australia, and at Robert Bosch GmbH in Germany, exploring technologies and circuits for 128GBaud fiber-optic systems, 300Gb/s mm-wave radio transceivers, imaging and radar sensors. Dr. Voinigescu co-founded and was the CTO of two fabless semiconductor start-ups: Quake Technologies and Peraso Technologies. He was a member of the International Technology Roadmap for Semiconductors RF/AMS Committee between 2008 and 2015, served on the TPC and ExCom of the IEEE CSICS from 2003 until 2013, and is a member of the ExCom of the IEEE BCICTS. He received NORTEL's President Award for Innovation in 1996 and is a co-recipient of the Best Paper Award at the 2001 IEEE CICC, the 2005 IEEE CSICS, and of the Beatrice Winner Award at the 2008 IEEE ISSCC. His students have won several Best Student Paper Awards at IEEE VLSI Circuits Symposium, IEEE IMS, IEEE RFIC, and IEEE BCTM. In 2013 he was recognized with the ITAC Lifetime Career Award for his contributions to the Canadian Semiconductor Industry.