Design Considerations for a 100 Gbit/s SiGe-BiCMOS Power Multiplexer With 2 V_{pp} Differential Voltage Swing

Christopher Uhl, Horst Hettrich, and Michael Möller, *Member, IEEE*

***Abstract*— This paper presents design considerations for an 8:1 multiplexer (MUX) circuit in a SiGe BiCMOS technology intended to be monolithically integrated together with a plasmonic Mach–Zehnder modulator on a single chip. It is shown why a power MUX (PMUX) architecture, where the final MUX selector stage directly drives the load, is beneficial to obtain high data rates and high output voltage swings at comparatively low power consumption. Therefore, the relation between the clock input amplitude and parasitic capacitances on the rise time of the PMUX is analyzed. Owing to the importance of the clock signal to the PMUX performance, design considerations for the clock distribution are presented. The design concept is proven by electrical measurements that demonstrate a record performance by clear output eye diagrams at 100 and 140 Gbit/s with 2.0 V_{pp} and 1.2 V_{pp} differential output voltage swing, respectively. The 2.6 mm × 1.7 mm MUX chip is implemented in IHP SG13G2 SiGe BiCMOS technology and consumes 7.15 W on a single −5.5-V supply voltage.**

***Index Terms*— BiCMOS integrated circuits, clocks, DC offset, duty-cycle error, electrooptic modulators, multiplexing, plasmons, silicon germanium.**

I. Introduction

A POWER multiplexer (PMUX) is a simple driver concept where the final 2:1 selector (SEL) at the output is utilized to directly drive the load. Since the differential output of a SEL toggles between high and low state, the PMUX concept can be applied for simple non-return-to-zero (NRZ) on-off keying (OOK) modulation schemes (PAM 2). In data centers, such a modulation scheme can be used even at high data rates of 100 Gbit/s and above because of the comparably short optical cable length. No power consuming processing at the transmitter or the receiver side is required for NRZ-OOK.

The PMUX concept was initially realized in [1] in a SiGe bipolar technology with $f_T = 72$ GHz, where an electroabsorption modulator was driven with 2.0 V_{pp} differential voltage swing at 50 Gbit/s. In the scope of the European Research and Development Project PLASMOfab, a novel plasmonic Mach–Zehnder modulator (MZM) under development [2]–[4] shall be integrated with a PMUX in a novel silicon photonics process. Therefore, the top metal layer in IHP SG13G2 SiGe BiCMOS process is going to be replaced by a photonic layer which carries the plasmonic MZM (cf. Fig. 1). Special design considerations that arise from the monolithical integration of the PMUX circuit together with this plasmonic MZM have already been discussed in [5]. The main feature of the MZM is its small active length down to 10 μm [2], [3], whereby the MZM can be assumed as lumped capacitance as small as 3 fF [4]. By driving the MZM via short interconnects (cf. Fig. 1), no far-end termination is required. By that, the output voltage swing is doubled compared to a conventional design with an external MZM. A SG$\overline{\text{S}}$ (signal, ground, inverse signal) electrode configuration allows for a differential drive of the plasmonic MZM with 2 V_{pp} differential voltage swing at a 100-Gbit/s data rate.

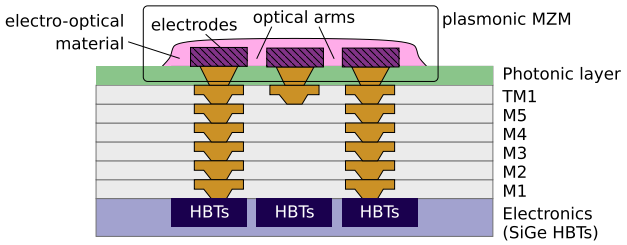

Fig. 1. Intended monolithical integration of a plasmonic MZM and a MUX in a silicon photonics BiCMOS process.

A first prototype of the PMUX in a SiGe BiCMOS technology with $f_T = 300$ GHz with a 50-Ω load instead of an integrated MZM was recently reported in [5]. It achieves record voltage swings of 2.0 V_{pp} and 1.2 V_{pp} at data rates of 100 and 140 Gbit/s, respectively.

One intriguing advantage of the PMUX concept is that its capability to reach high-operating speeds at comparatively high output voltage swings is mainly determined by the circuitry of the clock path rather than that of the data path (cf. [5]). As the clock is a stationary single-frequency signal, it does not suffer from pattern effects. This is a great benefit for the design if high-operating speed and voltage swing are aimed at which makes the PMUX well suited as a MZM driver. However, as the clock has a direct impact on the output eye

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C. Uhl and M. Möller are with the Chair of Electronics and Circuits, Saarland University, 66123 Saarbrücken, Germany (e-mail: christopher.uhl@eus.uni-saarland.de).

H. Hettrich is with the Chair of Electronics and Circuits, Saarland University, 66123 Saarbrücken, Germany, and also with MICRAM Microelectronic GmbH, 44801 Bochum, Germany.

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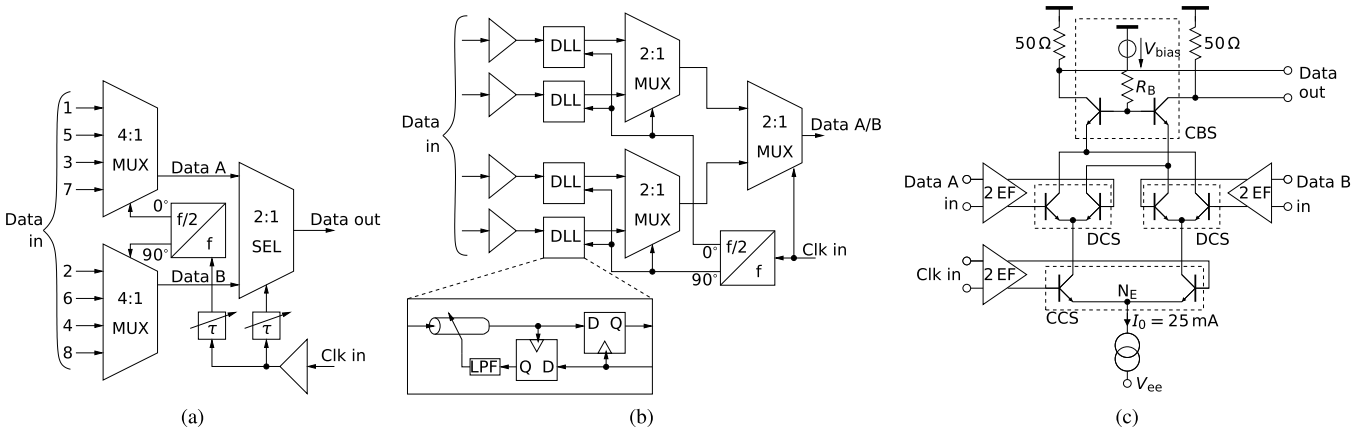


Fig. 2. Simplified block diagrams of the (a) 8:1 PMUX and (b) 4:1 Sub-MUX blocks. (c) Simplified circuit diagram of the final 2:1 SEL stage.

diagram of the PMUX, high requirements (high amplitude, low skew, low common-mode, low dc offset) need to be met. This is especially challenging as the presented PMUX is driven by a single-ended clock source over a wide frequency range of 50–70 GHz corresponding to 100–140 Gbit/s at the PMUX output. In this paper, the design considerations for the PMUX to reach a high swing at high-operating speeds are presented. Owing to the great importance of the performance of the clock circuitry for the PMUX performance, design considerations for the clock distribution to match the delay between the clock and data and to avoid or reduce systematic jitter and dc offset in the clock signal are presented.

The paper is organized as follows. The architecture of the PMUX is introduced in Section II, together with a detailed analysis of the relation between clock signal, parasitic capacitances, and eye diagram quality at the PMUX output. In Section III, design considerations for the clock distribution in order to achieve a high PMUX performance are presented. Measurement results of the PMUX are shown in Section IV.

II. PMUX Circuit Design Considerations

Fig. 2(a) shows the block diagram of the 8:1 PMUX. The input clock is buffered and fed via a clock distribution circuitry into the final 2:1 SEL and a 1:2 frequency divider that provides the clock signal for the preceding 4:1 MUX stages (cf. Section III). The block diagram of the 4:1 MUX stages is shown in Fig. 2(b). It consists of a frequency divider and 2:1 MUX stages which form a tree structure. The frequency dividers are synchronized by a reset concept in order to ensure that the MUX inputs are multiplexed in a pre-determined order. The eight data inputs of the total 8:1 MUX are fed single-ended to the chip which is possible because of the comparatively low input data rate of 100 Gbit/s/8 = 12.5 Gbit/s and offers the advantage of requiring less bondpads and external connectors. As all circuitry within the chip is operated differentially, a simple current switch (CS) in the data input buffer provides a single-ended to differential conversion. To ensure proper sampling of the input data, a delay locked loop [DLL, cf. Fig. 2(b)] aligns the data inputs to the clock of the first MUX stage by a delay line with one unit interval adjustable range. The function principle of this DLL architecture is explained in detail in [6].

In contrast to other high-speed MUX circuits [7], [8], no output buffer and no master-slave D flip-flop for retiming are used at the chip output. Instead, a PMUX concept is utilized where the output load is driven directly by the final 2:1 SEL stage. In the corresponding simplified circuit diagram in Fig. 2(c), the operating current I_0 is switched by the clock CS (CCS) alternately to one of two data CSs (DCSs). The inherent advantages of this architecture are already demonstrated in [1] and [5] and can be summarized as follows. A jitter or a phase shift of the data input does not appear at the output as long as the clock is within the clock phase margin (CPM). This is because the data input signals remain constant during the switching period of the CCS. Thus, the output rise time is controlled mainly by the CCS rather than by the DCS. As the CCS directly impacts the output signal of the PMUX, it allows to decrease the rise time of the output signal, and thereby to increase the speed of the circuit simply by increasing the clock input amplitude. It is this inherent advantage that predestines the SEL stage as an output driver that reaches a high output power (voltage swing) and a high-operating speed, simultaneously. That is why the MUX with this output stage is branded a PMUX.

As the plasmonic MZM is intended to be driven by a differential voltage swing of at least 2 V_{pp} at 100 Gbit/s, an operating current of $I_0 = 25$ mA is chosen that provides a differential voltage swing of 2.5 V_{pp} at the internal 50-Ω on-chip load and of 1.25 V_{pp} (differential) at the external 50-Ω oscilloscope load. To have enough headroom for this high output voltage, a bias voltage of $V_{\mathrm{bias}} = 1.2$ V is applied to the base of the common-base stage (CBS) [cf. Fig. 2(c)] via a resistive voltage divider. By that, the transistors are operated slightly above their maximum collector–emitter voltage, however, as the base of the transistors in the CBS is not open but terminated by $R_{\mathrm{B}} \approx 350\ \Omega$ and the collector current of the CBS transistors is mainly determined by the emitter current, slightly exceeding the maximum collector–emitter voltage leads only to a negligible current multiplication effect in the transistors. Transistors with the largest available emitter area of 0.63 $\mu\mathrm{m}^2$ are used for the CCS, the DCS, and the CBS. The peak current for the maximum transit frequency of this transistors is intentionally exceeded by approximately 35% because dynamic simulations with High

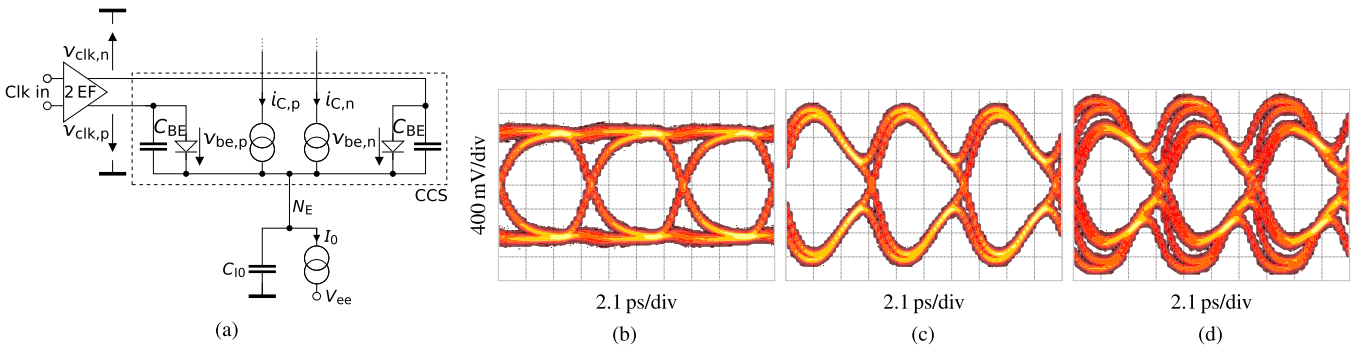


Fig. 3. (a) Equivalent circuit for analysis of the CCS. (b)–(d) Simulated eye diagrams of a 2:1 SEL at 140 Gbit/s using the transistor model of (a). In (b), it is $C_E = 0$, $C_{I0} = 0$. In (c), the CCS is driven by a pure odd-mode clock signal and $C_E = 46$ fF, $C_{I0} = 0$. In (d), the CCS is driven single-ended and $C_E = 46$ fF, $C_{I0} = 20$ fF.

Current Model (HICUM) confirm an increased performance compared to using two transistors in parallel with a higher total emitter area. Measurements at room temperature demonstrate the operation of up to $I_0 = 40$ mA corresponding to 2.0 V_{pp} (differential) at the external 50-Ω oscilloscope load with still good output eye quality at 100 Gbit/s (cf. Section IV).

In order to optimize the high speed performance of the final 2:1 SEL stage, first the relation between the output signal rise time and the applied clock signal needs to be known. This relation can be shown based on the simplified equivalent circuit of the CCS of Fig. 3(a). In this equivalent circuit, a simple transistor model with transfer function $i_C = I_S \exp(v_{be}/V_T)$ (I_S: saturation current and V_T: thermal voltage), and base–emitter capacitance $C_{BE} = C_{BE,d} + C_{BE,j}$ (diffusion and junction capacitance) is used. In order to obtain an easy to interpret analytical model that shows off the main influence factors on the rise time, the base resistor is neglected for this equivalent circuit. Transistor-level simulations with Vertical Bipolar Inter-Company (VBIC) models with and without base resistance have shown that the base resistance only changes the described effects quantitatively, but does not alter the concluding design considerations. The current source I_0 is modeled by its output capacitance C_{I0}. By decomposing the CCS clock input voltage and output current in time domain into their even-mode and odd-mode parts

$$i_C^+ := \frac{1}{2}(i_{C,p} + i_{C,n}), \quad i_C^- := \frac{1}{2}(i_{C,p} - i_{C,n}) \tag{1}$$

$$v_{clk}^+ := \frac{1}{2}(v_{clk,p} + v_{clk,n}), \quad v_{clk}^- := \frac{1}{2}(v_{clk,p} - v_{clk,n}) \tag{2}$$

the odd-mode CCS output current is expressed without further approximations as

$$i_C^- = i_C^+ \tanh\left(\frac{v_{clk}^-}{V_T}\right). \tag{3}$$

During the switching period of the CCS, the data input is static. This allows considering the DCSs to act as CBSs with a comparatively high cutoff frequency. Thus, the rise times at the DCS input and output are approximately the same, whereby the input current i_C^- determines the rise time of the PMUX data output. Equation (3) shows how to reduce the rise time of i_C^-. First, an increase of v_{clk}^- reduces the rise time as the tanh function is driven into the saturation region, and thus output currents close to the static levels are reached earlier. Second, i_C^- directly depends on the even-mode output signal i_C^+. This is utilized to reduce the PMUX data output rise time. With the help of the following analysis, the circuit can be designed to introduce an overshoot to i_C^+ at the beginning of each bit period and reduce the rise time by that. By neglecting the base–emitter diode current in comparison to β_0 (dc current gain) times higher collector current, according to (1) and Fig. 3(a), it is $i_C^+ = I_0/2 + i_{cap}$, where i_{cap} denotes the total current through all capacitances at the node N_E (2 C_{BE}, C_{I0}). Based on the model in Fig. 3(a), the ordinary differential equation

$$i_{cap} + \left(\frac{C_E V_T}{i_{cap} + I_0/2} + \tau_F\right)\frac{\mathrm{d}\, i_{cap}}{\mathrm{d}\, t} = C_E \tanh\left(\frac{v_{clk}^-}{V_T}\right)\frac{\mathrm{d}\, v_{clk}^-}{\mathrm{d}\, t} + \frac{1}{2}C_{I0}\frac{\mathrm{d}\, v_{clk}^+}{\mathrm{d}\, t} \tag{4}$$

for i_{cap} is derived, where τ_F is the transit time and $C_E = C_{I0}/2 + C_{BE,j}$. As it is $i_C^+ = I_0/2 + i_{cap}$, the maximum overshoot of i_C^+ occurs at the peak value of i_{cap}, where $\mathrm{d}\, i_{cap}/\mathrm{d}\, t = 0$. Thus, according to (4), the peak value of i_{cap} and thus the overshoot of i_C^+ can directly be controlled by the right side of (4), which contains two terms.

The first term on the right side of (4) is proportional to the time derivative of the odd-mode clock input signal $\mathrm{d}\, v_{clk}^-/\mathrm{d}\, t$, and thus leads to a peak value of i_{cap} at the beginning of each bit period. This term causes the aforementioned overshoot in i_C^+, which is utilized to shorten the data output rise time. The term is proportional to the odd-mode clock input amplitude v_{clk}^- and to the total capacitance C_E at the node N_E. The corresponding effect is exemplarily demonstrated for a change in C_E by a comparison of simulations with and without parasitic capacitance C_E in Fig. 3(b) and (c), respectively. The eye diagram with C_E shows a clear reduction of the rise time to reach 90% of the static levels from 4.8 to 3.6 ps. A similar behavior is observed by varying the odd-mode clock input amplitude v_{clk}^-. As a consequence of the overshoot in i_C^+, the eye diagram shows a significant overshoot. This overshoot is a valuable benefit that helps to reach the high-operating speed as it compensates for bandwidth limitations introduced by parasitics of the circuit and the bondwire interface.

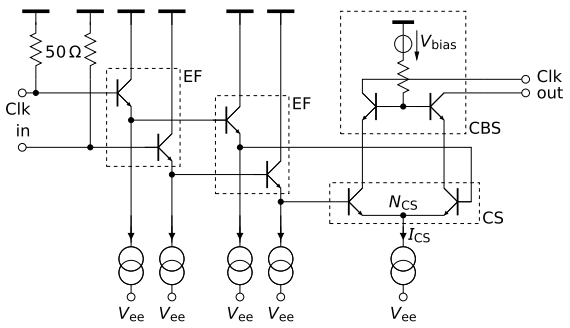


Fig. 4. Simplified circuit diagram of the clock input buffer of the 8:1 MUX.

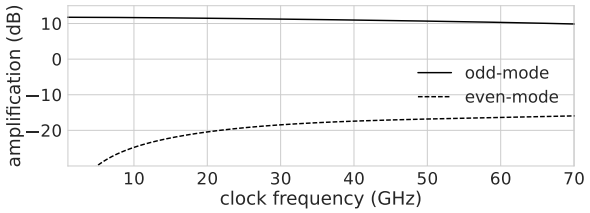


Fig. 5. Simulated odd- and even-mode amplification of the input clock buffer with parasitic layout extraction.

As design criteria to obtain a short data output rise time, C_E and the odd-mode clock input amplitude v_{clk}^- need to be high. The main contribution to C_E is the base–emitter junction capacitance $C_{\text{BE},j}$ of the CCS transistors. Because of the comparatively large transistor size due to the high-operating current I_0, this capacitance already is high. A high odd-mode clock input voltage swing v_{clk}^- of up to 2 V_{pp} (differential) at the CCS input is achieved by a clock buffer circuit that drives the CCS.

The second term on the right side of (4) also contributes to the overshoot in i_C^+. It is proportional to the time derivative of the even-mode clock input signal $\mathrm{d}\,v_{\text{clk}}^+/\mathrm{d}\,t$ and to the current-source capacitance C_{I0}. However, an even-mode clock input signal $\mathrm{d}\,v_{\text{clk}}^+/\mathrm{d}\,t$ at the fundamental clock frequency f_{clk} decreases the rise time only for every second data bit, while it increases it for the other data bits. The simulation in Fig. 3(d) visualizes the impact of this effect on the eye diagram. As a consequence for the design, the contribution of the second term on the right side of (4) shall be minimized. This can be accomplished by minimizing C_{I0} and the CCS even-mode clock input amplitude v_{clk}^+. The capacitance C_{I0} consists of the transistor capacitance of the current source and of layout capacitances. The minimum transistor size for the current source I_0 is limited by the maximum dc current density at the transistor terminals in order to prevent electromigration. Therefore, for a low C_{I0}, the interconnect length is minimized on the emitter node N_E [cf. Fig. 3(a)]. In order to obtain a low even-mode clock input amplitude v_{clk}^+, the even-mode component of the chip input clock is suppressed already at the clock input buffer. In the following, design considerations for this buffer and the succeeding stages of the clock distribution are presented.

III. Clock Distribution Design

A. Clock Input Buffer Optimization

At the PMUX chip clock input, an input buffer that consists of a pair of two cascaded emitter followers (EFs) that drive a CS and a CBS (cf. Fig. 4) amplifies the input clock for the subsequent stages. The input buffer is followed by a chain of buffers (cf. Section III-B) that distribute and amplify the clock. The input buffer is driven by an external single-ended clock source. Thus, a high even-mode clock component is present at the input. As stated in Section II, an even-mode component has a severe impact on the PMUX eye diagram, and therefore needs to be suppressed. In addition, the even-mode input signal leads to a dc offset at the output of the clock input buffer by homodyne mixing of the odd- and even-mode clock input components at the nonlinear characteristic curve of the CS [6]. A dc offset is problematic as it propagates through the subsequent clock buffers which can significantly amplify it. This effect is analyzed in more detail in Section III-C. By that, a high dc offset can appear at the final 2:1 SEL and impact the output eye diagram. Although such a dc offset can be compensated for by applying a corrective dc voltage, it is best if it is already minimized at the clock input buffer. As a design measure to reduce both the even-mode component and the dc offset at the output of the clock input buffer, the capacitance at the node N_{CS} is minimized (cf. Fig. 4). This is achieved by using transistors with an emitter area of 0.38 μm^2, which enable a compact layout with small parasitic capacitances while still allowing for a current I_{CS} of 10 mA and a corresponding differential output voltage swing of 1 V_{pp}. The small signal simulation of the odd- and even-mode amplification including layout parasitic extraction by Assura QRC in Fig. 5 shows a good common-mode rejection of the clock input buffer of more than 25 dB up to frequencies of 70 GHz. Thus, the even-mode component at the output of the clock input buffer can be considered as neglectable.

The choice of the single-ended chip clock input amplitude is a tradeoff between the clock amplitude and dc offset at the output of the clock input buffer. A higher clock input amplitude increases the dc offset. This follows from [6], where it is shown that the dc offset that results from an even-mode input signal is approximately proportional to both the even- and odd-mode clock input amplitudes. Thus, the dc offset rises quadratically with the single-ended clock input amplitude, whereas the clock output amplitude of the clock input buffer only rises linearly and even goes into saturation. On the other hand, decreasing the clock input amplitude worsens the signal-to-noise ratio. For the presented PMUX chip, a clock input power of 0 dBm represents a good tradeoff between dc offset and noise in the used frequency range of 50–70 GHz.

B. Clock to Data Phase Adjustment

For proper operation of the final 2:1 SEL, the clock phase needs to be kept within the CPM of the final 2:1 SEL. This is accomplished by an adjustable delay line concept that provides sufficiently low skew between the data and clock at the input of the 2:1 SEL. As shown in the overall block diagram in Fig. 2(a), the half-rate input clock is distributed

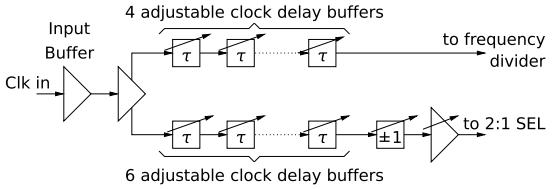


Fig. 6. Clock distribution of the 8:1 PMUX design.

to both the final 2:1 SEL and the frequency divider for the preceding 4:1 MUXs. The path through the frequency divider and the 4:1 MUXs to the data input of the final 2:1 SEL introduces a significant delay. To match the phases between the clock and data at the input of the final 2:1 SEL, a cascade of clock buffers is introduced to add a corresponding delay. However, to compensate for the delay of the data path, a high (>15) number of clock buffers would be required in the path to the final 2:1 SEL. This would significantly increase the total power consumption of the PMUX chip. Furthermore, a cascade of such a high number of buffers is prone to dc offset amplification (cf. Section III-C). Finally, it is very challenging to match the delays of both paths over temperature, process mismatch, and operating frequency range. Therefore, a different approach is used where the clock phase between the path to the frequency divider and the path to the final 2:1 SEL can be adjusted externally by 360° from the minimum operating frequency of 50 GHz, and thus allows for adjusting the phase within the CPM. This is achieved by a total of 10 adjustable clock delay buffers that enable a phase adjustment range of 180° and by a switchable clock inverter that provides additional 180°. The block diagram of this clock distribution is shown in Fig. 6. The clock input buffer (cf. Section III-A) drives the same type of buffer that utilizes two instead of one CSs to split the clock signal to the two paths. In the path to the frequency divider, four adjustable clock delay buffers and in the path to the final 2:1 SEL, six adjustable delay buffers are placed. The higher number of buffers in the 2:1 SEL path is chosen to obtain a sufficiently high differential clock input amplitude of up to 2 V_{pp} to create the intended overshoot at the CCS of the final 2:1 SEL (cf. Section II). Therefore, an additional clock buffer with adjustable output current is used to drive the final 2:1 SEL.

The delay of the adjustable delay buffers is controlled commonly for each path by externally applied control voltages. A simplified circuit diagram of one of the delay buffers is shown in Fig. 7. The two transadmittance stages (TASs) in the dashed TAS block commutate the operating current I_{TAS} between the two CSs depending on the applied control voltage V_{ctrl}. By that, the delay can be adjusted between a short delay path consisting of two cascaded EF pairs and a long delay path with the additional EF3 pair. Although the additional EF leads to different dc operating points of the two CSs, the resulting different base–collector capacitances do only slightly influence the RF performance. The dimensioning of the resistors R_{EF3} is a design tradeoff. Increasing R_{EF3} increases the delay of the longer path, and thus allows for a larger adjustable delay range. However, an increase of R_{EF3} reduces the bandwidth of the circuit. For the presented PMUX design, $R_{\mathrm{EF3}} = 100\ \Omega$

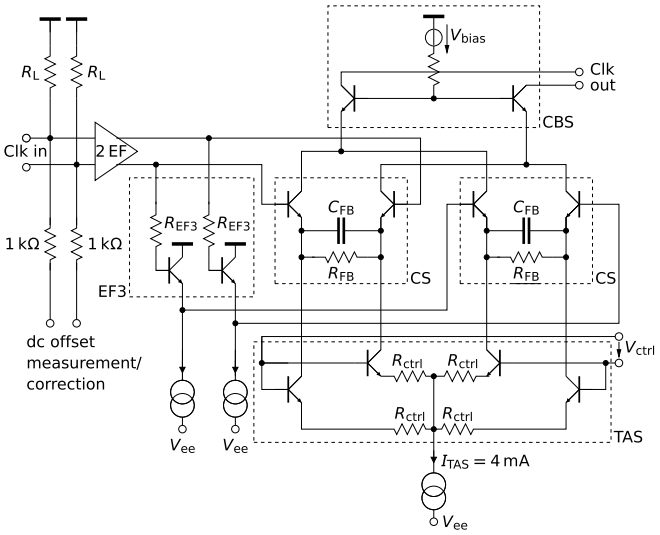


Fig. 7. Simplified circuit diagram of a single adjustable clock delay buffer.

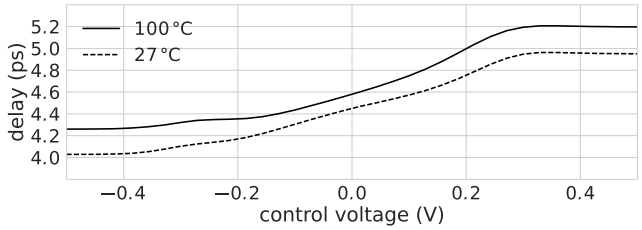


Fig. 8. Simulated delay of the delay buffer in Fig. 7 versus delay control voltage V_{ctrl}.

and an operating current of 3 mA for EF3 were chosen that allow for a delay adjustment range of 1 ps per buffer and a bandwidth of more than 70 GHz. Small transistors with an emitter area of 0.13 $\mu\mathrm{m}^2$ for the CSs and for EF3 in combination with $R_{\mathrm{L}} = 100-\Omega$ termination resistors are used in order to obtain this high bandwidth at a moderate power consumption. The simulation in Fig. 8 demonstrates that the delay is nearly linearly depending on the control voltage V_{ctrl}. The delay of the buffers increases slightly with temperature, however, as this effect occurs in both clock paths, it partly cancels out such that the phase between the two paths for a temperature change from 27 °C to 100 °C only changes by a maximum of 10° that is significantly below the simulated CPM of approximately 70° for the highest clock operating frequency of 70 GHz. Nevertheless, as the phase between the data and clock can be adjusted by 360°, a re-calibration in principle is possible.

To reduce the dc offset gain of the cascade of delay buffers, *RC* emitter degeneration by $R_{\mathrm{FB}} = 125\ \Omega$ and $C_{\mathrm{FB}} = 40$ fF is introduced to the CSs. By that, a static dc offset at the input is amplified by a lower gain (≈1.1 for $V_{\mathrm{ctrl}} = \pm 0.4$ V) than the RF clock signal (≈1.7 at 50 GHz for $V_{\mathrm{ctrl}} = \pm 0.4$ V). The dc gain in principle could be reduced further by increasing R_{FB}, however, a dc gain of more than one was requested for the present design in order to allow for low-speed tests. The capacitance C_{FB} was optimized by circuit simulations.

A trade-off exists, as an increasing C_{FB} improves the lower cutoff frequency of the buffer but also increases its layout area which comes with parasitic capacitances, and thus worsens the common-mode rejection of the CS. To not introduce an additional static dc offset, the resistors $R_{\mathrm{ctrl}} = 80\ \Omega$ of the TAS need to be matched. However, this is easy to achieve as no RF signal is applied to the resistors R_{ctrl} which, thus, can be chosen with a large area to obtain low mismatch.

As both introducing *RC* emitter degeneration into the CSs as well as cascading three EFs can lead to instability [9], [10], critical layout parts and the dimensioning of the EFs are optimized in this regard. To analyze the stability, an approach based on [11] is used by investigating the driving point admittance $\underline{Y}_{\mathrm{p}} = \underline{I}_{\mathrm{p}}/\underline{V}_{\mathrm{p}}$ at a port under consideration, where $\underline{I}_{\mathrm{p}}$ is the current flowing into that port when a voltage $\underline{V}_{\mathrm{p}}$ is applied to the port. If the driving point admittance $\underline{Y}_{\mathrm{p}}$ exhibits a negative real part within a frequency region and its imaginary part crosses zero with the positive slope within this region, the circuit is unstable [12]. The driving point admittance is investigated at the input of each EF pair and both CSs by small signal simulations with parasitic layout extraction by Assura QRC. By optimization of critical layout parts, especially at the EF output and collector nodes, the stability of the circuit is ensured.

C. Clock Delay Buffer Chain Optimization

Although the measures described in the preceding sections significantly reduce the clock dc offset, all previous 2:1 SEL designs [6] as well as the one presented here show a strong rise of clock dc offset in a certain frequency range close to the intended operating frequency. In principle, such an offset can be compensated in the PMUX design by feeding a complimentary dc current into the load resistors R_{L} of each clock delay buffer (cf. Fig. 7). However, it is advisable to understand the root cause of such a strong frequency dependent dc offset in order to address this effect by adequate design considerations. A clock dc offset causes a duty-cycle distortion of the clock signal and vice versa. Thus, the amplification of the duty-cycle distortion is a measure for the dc offset gain. In [13], an analytical model is presented which describes the duty-cycle distortion amplification

$$F_{\mathrm{DCD}} = \frac{\sum_{l=\mathrm{even}} H(l f_{\mathrm{clk}})\, \mathrm{e}^{\mathrm{j}\, 2\pi l f_0\ t_d}}{\sum_{k=\mathrm{odd}} H(k f_{\mathrm{clk}})\, \mathrm{e}^{\mathrm{j}\, 2\pi k f_0\ t_d}} \tag{5}$$

of a linear channel with transfer function $H(f)$ and delay time t_d at the clock frequency f_{clk}. Equation (5) can also be applied to a chain of clock buffer cells (cf. Fig. 9) of the type shown in Fig. 7. In this case, $H(f)$ is represented by the transfer function in between the CSs of two succeeding clock buffers, i.e., the transfer function of the CBS of the preceding buffer cell, of the transmission line and of the EFs of the buffer cell are under consideration. In [13], a passive, monotonous decreasing transfer function $H(f)$ is considered, and therefore, all contributions at harmonics of f_{clk} to the sums of (5) are neglected which leads to a duty-cycle distortion amplification F_{DCD} that rises over frequency. In contrast, for the active broadband PMUX clock buffers considered here,

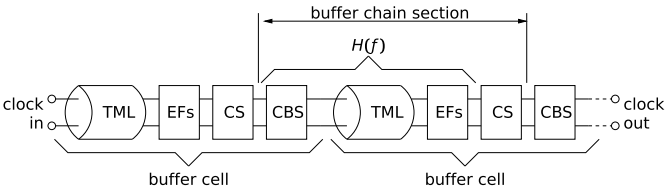


Fig. 9. Block diagram of a generic chain of clock buffers used for analysis of the duty-cycle distortion amplification.

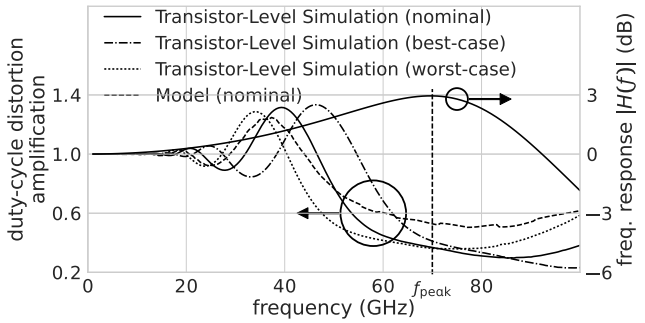


Fig. 10. Simulated frequency response $H(f)$ of the clock delay buffer in Fig. 7 (for $V_{\mathrm{ctrl}} = -0.4$ V) and corresponding duty-cycle distortion amplification factors of this buffer circuit obtained by transistor-level simulations and by applying (5).

$H(f)$ is not a monotonous function that requires to consider also the contributions at harmonics of f_{clk}. This leads to an interesting and performance influencing frequency dependent behavior with peaks of the duty-cycle distortion amplification F_{DCD} as demonstrated in the following.

To achieve a high bandwidth in the PMUX clock path design, the EFs in the clock delay buffers are dimensioned to introduce a peaking to the frequency response $H(f)$ near the cutoff frequency of the buffer. This commonly used measure to increase the bandwidth of a buffer has a direct impact on the duty-cycle distortion amplification. This is demonstrated for one of the delay buffers of Fig. 7. In Fig. 10, the simulated transfer function $H(f)$ shows a peak at a frequency $f_{\mathrm{peak}} \approx 70$ GHz. By applying (5), this peak in $H(f)$ lowers the duty-cycle distortion amplification around the peak frequency f_{peak}. Thus, the EF peaking does not only help to improve the buffer bandwidth but also to reduce the duty-cycle distortion. For clock frequencies f_{clk} at even fractions of f_{peak} ($f_{\mathrm{peak}}/2 = 35$ GHz, $f_{\mathrm{peak}}/4 = 17.5$ GHz, ...), the peak in $H(f)$ contributes to the numerator of (5) at even harmonics of f_{clk}, and thus leads to peaks of the duty-cycle distortion amplification F_{DCD}. At these peaks, F_{DCD} is significantly larger than one, which is critical as a duty-cycle distortion at the input of the clock buffer chain gets amplified by each buffer cell, and thus leads to a significant duty-cycle distortion at the output. In Fig. 10, the transistor-level simulation shows a qualitatively comparable behavior to the model (5), however, quantitative deviations occur as the model assumes a linear transfer function $H(f)$ in between the CSs of the buffer cells and does not account for large signal effects and not for the *RC* emitter degeneration applied to the CSs in Fig. 7. According to this result, eye diagram simulations of the total PMUX in Fig. 11 demonstrate that the PMUX data output is severely affected, if the clock frequency matches the peak frequency of

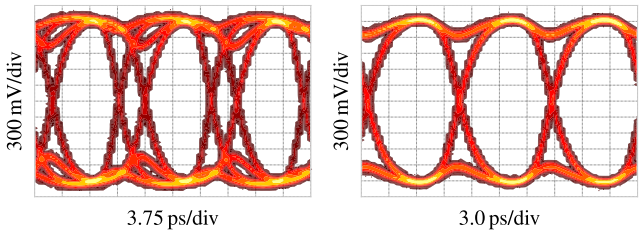
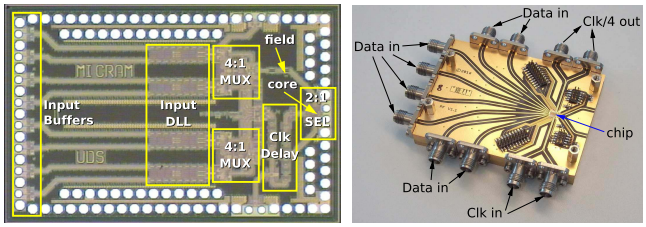


Fig. 11. Simulated PMUX output eye diagrams at 80 Gbit/s (left) with a clock frequency $f_{\mathrm{clk}} = 40$ GHz within the duty-cycle distortion amplification peak in Fig. 10 and at 100 Gbit/s (right) with a clock frequency $f_{\mathrm{clk}} = 50$ GHz beneath the peak.



(a) (b)

Fig. 12. (a) Photomicrograph of the presented 8:1 PMUX chip (4.42 mm^2). (b) Assembly in an RF-module.

TABLE I
SIMULATED CURRENT AND POWER CONSUMPTION OF EACH CIRCUIT BLOCK

Circuit block	current in mA	power in W
Final 2:1 SEL/output stage	155	0.85
Distribution/Delay of 50 GHz ... 70 GHz clock	390	2.15
4:1 MUXs, frequency dividers	330	1.82
Data input buffers, Input DLL	420	2.31

the duty-cycle distortion amplification. This effect especially needs to be taken into account if a design with a broad frequency range is aimed at or if the design has large headroom in speed to be robust to process variations in a product design. For the example circuit, simulations with the best case and worst case VBIC transistor models show a significant variation in the peak frequency (cf. Fig. 10). To prevent this effect, the peaking of the EFs could be reduced; however, this would also reduce the bandwidth, and thus the maximum data rate of the PMUX. The presented PMUX design thus represents a tradeoff which allows for a clock operating frequency range of 50–70 GHz with low duty-cycle distortion amplification, i.e., without the need of an offset compensation at the clock delay buffers.

IV. MEASUREMENT RESULTS

The 2.6 mm × 1.7 mm 8:1 PMUX chip [cf. Fig. 12(a)] is fabricated in IHP SG13G2 BiCMOS technology ($f_T/f_{\max}$ = 300 GHz/500 GHz). The chip consumes 1.3 A at a single −5.5-V supply, corresponding to 7.15 W. As given in Table I, only 0.85 W is consumed by the PMUX

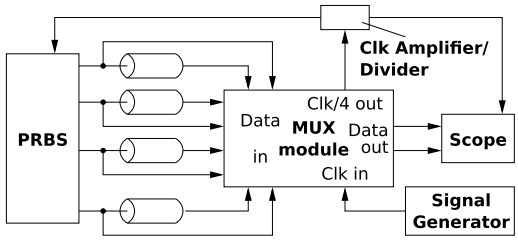


Fig. 13. Measurement setup.

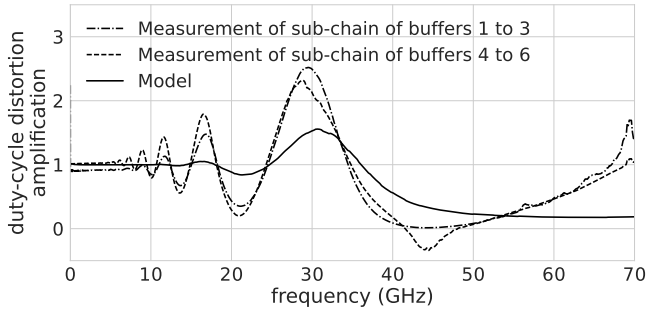


Fig. 14. Comparison of the measured duty-cycle distortion amplification of the presented 8:1 PMUX chip for two sub-chains with three clock delay buffers each to the calculation of the duty-cycle distortion amplification according to the model in Section III-C.

final 2:1 SEL stage that represents the actual plasmonic MZM driver (for the nominal operating current $I_0 = 25$ mA, cf. Section II). In the design process, the focus was laid on the optimization of the power consumption of the final 2:1 SEL and the distribution of the high-speed clock rather than on low-speed blocks. For characterization, the chip is assembled in an RF module as shown in Fig. 12(b). No active cooling is required to distribute the heat from the PMUX chip. The temperature was measured at two positions on the chip via integrated diodes which have been calibrated in an oven. One diode is placed directly beneath the transistors of the output driver (core) and the other diode is placed in a distance of 350 μm (field). The corresponding positions are marked in the chip photomicrograph in Fig. 12(a). In the field position, the temperature rises from 59 °C directly after power on to 72 °C after complete heat-up of the module. At the core position, the temperature rises from 112 °C to 127 °C. Although the applied semiconductor technology is not qualified yet, from the experiences of a similar technology it can be expected that no long-term reliability issues will be caused by this comparably high temperature [14]. To ensure reproducible measurement results, all of the following measurements were performed after the module was fully heat-up. The measurement setup is shown in Fig. 13. All of the high-speed I/Os, except the PMUX output, are connected via bondwires and microstrip lines to K-connectors. The PMUX output is measured on the die by a 67-GHz Infinity probe and connected to a DCA-J 86100C sampling scope with an 86118A H01 sampling head and an 86107A precision timebase. An E8257D signal generator is used as half-rate single-ended clock source. Four independent $2^9 - 1$ pseudo-random bit sequences (PRBSs) are generated by a MP1800A bit pattern generator with four MU181020B modules. To obtain eight PMUX input data signals, each of

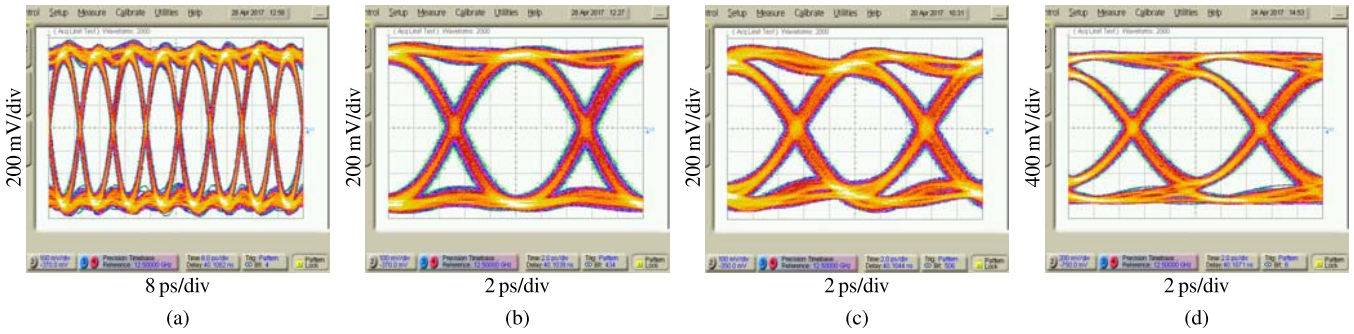


Fig. 15. Measured on-die differential output eye diagrams at 100 Gbit/s. (a)–(c) With a nominal differential output voltage swing of 1.2 V_{pp}. (d) With an increased differential output voltage swing of approx. 2.0 V_{pp}. For the measurements in (c) and (d), 6-dB, 67-GHz attenuators were used that severely impair the signal quality.

the generated four data signals is connected to two inputs via different cable lengths to de-correlate the input signals. An additional output of the MUX chip provides the input clock divided by four as a clock source for the bit pattern generator and to trigger the sampling scope.

The duty-cycle distortion amplification of the delay buffers in the clock distribution (cf. Fig 6) is determined for one sample chip by measuring the dc offset voltages at the inputs and outputs of two sub-chains consisting of three buffers each via on-chip high-ohmic (1 kΩ) resistors (cf. Fig. 7). Fig. 14 shows the corresponding duty-cycle distortion amplification which can be shown to be approximately equal to the measured ratio of the dc offset voltages. Both the model evaluation and the measurements show peaks at comparable frequencies, which confirms that these peaks result from the peaking of the EF transfer function according to Section III-C. The measured peaks have a higher magnitude than the ones in the model due to additional dynamic large signal effects which cannot be accounted for by the linear transfer function $H(f)$ that is obtained by small-signal simulations. For the frequency range of 50 GHz to nearly 70 GHz, the measured duty-cycle distortion amplification is below one. Thus, the delay buffer chain does not amplify a dc offset that is present at its input.

Eye diagram measurement results of the PMUX have already been presented in [5] and are shown, here, again to demonstrate the performance related to the topics of this paper. Fig. 15(a) and (b) shows clear opened eye diagrams for the intended data output rate of 100 Gbit/s. The differential output voltage swing is 1.2 V_{pp} at the 50-Ω load of the sampling scope. When the 50-Ω load is replaced by the integrated MZM in the next development step, this voltage will double. In addition, the load capacitance of the plasmonic MZM of approximately 3 fF [4] is much lower than the bondpad capacitance of typically 20 ... 40 fF, and thus an even higher bandwidth is expected. To demonstrate that the PMUX is capable to operate at higher output voltage swings, the operating current I_0 [cf. Fig. 2(c)] has been increased. By that, the eye diagram in Fig. 15(d) was obtained which shows approximately 2.0 V_{pp} differential output voltage swing at the 50-Ω load with still good eye quality. To be able to measure such a high output voltage swing, 6-dB, 67-GHz attenuators needed to be placed into the signal path. These attenuators severely degrade the signal quality as can be seen by comparison of the eye diagrams in Fig. 15(b) and (c), which were both measured for nominal output current. In order to demonstrate the inherent high-speed capability, the data rate of the PMUX was increased to 140 Gbit/s, corresponding to the maximum clock frequency of 70 GHz of the clock signal generator. As the PRBS generator is only able to provide data signals up to 14 Gbit/s (corresponding to 112 Gbit/s at the output of the 8:1 MUX), its input clock was additionally divided by 2 for these measurements. This means that each two subsequent input bits of the 8:1 MUX are equal leading to a repetition of each sequence of 8 bits at the MUX output. Although, this does not represent a true PRBS sequence any more, the highest frequency components that limit the performance still are included in the data output signal. The measured output eye diagram in Fig. 16 is still clearly open at a differential output voltage swing of 1.2 V_{pp}. In [5], it has been demonstrated that the eye diagram quality is mainly limited by the measurement equipment for this data rate.

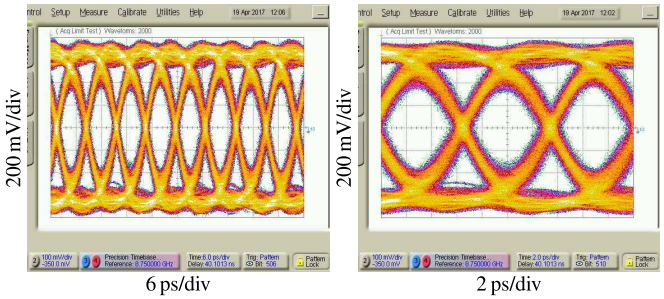


Fig. 16. Measured on-die differential output eye diagrams at 140 Gbit/s with a nominal differential output voltage swing of 1.2 V_{pp}.

V. Conclusion

In this paper, it was demonstrated that the PMUX concept offers high speed and voltage swings. The performance is substantially related to the clock rather than to the data path. In particular, the output current of the CCS in the final 2:1 SEL determines the rise time, the overshoot, and the voltage swing of the output data. As the clock directly influences the output eye quality, a clock distribution concept was proposed that provides a clock signal of high quality to the final 2:1 SEL. Design considerations for the single stages

of the clock distribution allow for a high clock amplitude, a low dc offset and for an adjustment of the clock phase. The validation of the proposed design considerations was demonstrated by measurements of the PMUX that achieves a record performance of 1.2 V_{pp} differential output voltage swing at 140 Gbit/s.

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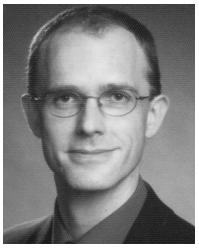
Christopher Uhl was born in Sankt Wendel, Germany, in 1989. He received the M.Sc. degree in mechatronics from Saarland University, Saarbrücken, Germany, in 2013, where he is currently pursuing the Ph.D. degree in electrical engineering.

Since 2013, he has been a Research Assistant with the Chair of Electronics and Circuits, Saarland University. His current research interests include optimization methods of (broadband) high-speed BiCMOS circuits with special regard to switched broadband amplifiers and clock distribution circuits.

Horst Hettrich was born in Saarbrücken, Germany, in 1986. He received the Dipl.-Ing. degree in mechatronics from Saarland University, Saarbrücken, Germany, in 2009, where he is currently pursuing the Ph.D. degree in electrical engineering.

From 2009 to 2015, he was a Research Assistant with the Chair of Electronics and Circuits, Saarland University. In 2015, he joined Micram Microelectronic GmbH, Bochum, Germany. His current research interests include broadband amplifiers and optical modulator drivers.



Michael Möller (M'06) was born in Bebra, Germany, in 1965. He received the Dipl.-Ing. degree in electrical engineering from FH Giessen, Giessen, Germany, in 1987, and the Dipl.-Ing. and Dr.-Ing. degrees in electrical engineering from Ruhr-University Bochum, Bochum, Germany, in 1991 and 1999, respectively.

He was a Research Engineer with Arbeitsgruppe Halbleiterbauelemente, Ruhr-University Bochum, with Prof. H.-M. Rein, where he was a major contributor to the development of high-speed demonstration circuits as key components in fiber-optical transmission systems. Many of his chip designs, which he developed with team members and partners have achieved world records for speed and performance. In 1999, he joined Micram Microelectronic GmbH, Bochum, Germany, after completing the development of the world's first integrated 40- and 80-Gb/s receiver chips. In 2001, he was promoted to Vice President of Engineering and named as an Executive Board Member. In 2005, he was a Professor of electronics and circuits with Saarland University, where he is working on the exploration of performance limits of integrated high-speed circuits and on the development of circuit design and optimization methods for performance enhancement at high-operating speeds.