

A Time-Resolved Four-Tap Lock-In Pixel CMOS Image Sensor for Real-Time Fluorescence Lifetime Imaging Microscopy

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Abstract—A programmable sub-nanosecond time-gated four-tap CMOS lock-in pixel (LIP) image sensor that uses an in-pixel pulse generator (PG) is developed for time-resolved (TR) biomedical imaging applications, such as a fluorescence lifetime imaging microscopy (FLIM). We demonstrate the system’s effectiveness with simulations and measurements. Using pixel-level PG circuits, very narrow time windows (TWs) that are less than 0.8 ns can be used for charge modulation. This rapid gating allows very weak signals from living cells to be captured with a high signal-to-noise ratio (SNR). The prototype CMOS imaging system displays a fast intrinsic response of 170 ps at 472 nm and a very low temporal random noise of 0.85 e-rms at 45 frames/s under truly correlated-double-sampling operation using two-stage charge transfer. Four outputs from the LIPs allow real-time fluorescence lifetimes (FLTs) measurement, even from samples with multiple FLT components.

Index Terms—CMOS image sensor (CIS), fluorescence lifetime imaging microscopy (FLIM), four-tap CMOS lock-in pixel (LIP), high signal-to-noise ratio (SNR), sub-nanosecond time gating, time resolved (TR) imaging.

I. INTRODUCTION

FLUORESCENCE-BASED time-resolved (TR) image analysis techniques are effective and useful methods in the life sciences and medical diagnostics. Among specific techniques, fluorescence lifetime imaging microscopy (FLIM) is typically used in biomedical research to investigate cellular mechanisms as well as fundamental biological functions.

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Advanced all-solid-state imaging devices for FLIM, such as a charge-coupled device (CCD) with optional electron-multiplication (EM) readout, a picosecond gated intensified-CCD (I-CCD), a single-photon avalanche diode (SPAD), and a TR CMOS image sensor (CIS), have recently been reported [1]–[5]. These devices can be implemented in more compact settings than traditional FLIM systems, such as time-correlated single-photon counting (TCSPC) systems [6]. However, some challenges remain for imaging devices based on CCD or SPAD, such as their need for specialized fabrication processes, use of high voltages, and great circuit complexity. CIS technology provides many opportunities for introducing new functions in imaging devices [7]–[14]. Recent TR CIS systems with two taps for each pixel have opened up the possibility of real-time fluorescence lifetime (FLT) imaging [12], [13]. Moreover, they have excellent signal charge storability, remarkably low temporal noise, and high-efficiency signal utilization. However, several limitations arise if a two-tap CIS measures a sample that includes several fluorescence components with different exponential decay curves. The two sample FLTs cannot be measured exactly in real time; thus, the two components cannot be discriminated in a captured image. In addition, the use of narrow sampling widths (<1 ns) for high time resolutions is disallowed by the driving capability of clock driver and the stray *RC* components on the chip.

Furthermore, in this paper, we propose a four-tap lock-in pixel (LIP) CIS that uses an internal pulse generator (PG) to attain sub-nanosecond time windows (TWs) for FLT imaging [14]. To enable real-time FLT measurements, a low-noise signal and rapid data acquisition are essential. Thus, we used lateral electric field charge modulation (LEFM) [15]–[17] in the sensor’s four-tap LIPs to minimize noise and increase the sampling rate. The narrow TWs generated in the pixel-level PG also increase the sensor’s signal-to-noise ratio (SNR) and time resolution.

This paper is organized as follows. Section II describes the proposed four-tap pixel architecture that uses LEFM, the in-pixel PG for sub-nanosecond time gating, and the overall sensor architecture. After describing the architecture of the developed TR CIS, Sections III and IV contain the discussion on the sensor performance and the benefits of FLT measurements of our proposed CIS, respectively. Section V summarizes and interprets our results.

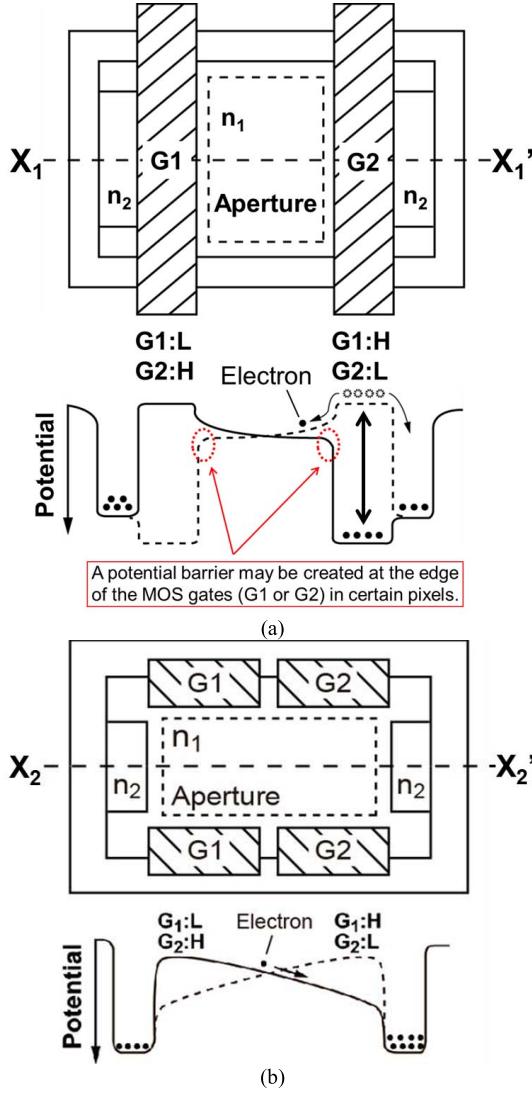


Fig. 1. Simplified two-tap charge modulators. (a) Conventional LIP. (b) LEFM LIP.

II. FOUR-TAP LOCK-IN PIXEL WITH IN-PIXEL PULSE GENERATOR

Advanced CIS technologies offer a range of possibilities for improving the performance and the functionality of CMOS imaging devices. LIP imaging is a new-generation imaging technique for CMOS sensors. LIPs can extend the applications of solid-state imaging devices within the fields of biomedical and real-time range imaging [15]–[24]. As shown in Fig. 1(a), when an image sensor uses a conventional LIP, each pixel transfers photo-induced charges to two charge-accumulation regions synchronously through the gate of an MOS transistor (G1 or G2) [7]–[9]. Two n-type layers (n_1 and n_2) formed on a lightly doped p-type epitaxial layer are used for storage in each charge modulator (or pixel). However, conventional LIP CISs that use direct gating for charge modulation face great challenges, in achieving high-speed charge transfer and a low-noise detection signals. The ability to transfer single electrons is essential for biological applications. The electric field generated by the typical modulation method with the MOS gates cannot easily achieve the high-speed directional

charge transfer to the charge storage region from the photo-sensitive region. Because of an inappropriately tuned electric field, a potential barrier may be created at the edge of the MOS gate, thus preventing single electrons from being transferred in some pixels. Photo-induced charges can also be lost from the detection signal when charges stored in the channel of the MOS gate are fed back into the photo detector. While, electrons are transferred by the gating operation, electrons are captured in traps at a boundary between silicon (Si) and silicon dioxide (SiO_2), these traps sometimes cause incomplete charge transfer that results in additional noise.

However, as shown in Fig. 1(b), a two-tap LIP using LEFM gates allows a higher electric field to be applied to each channel in the aperture area (n_1 region). This structure has two pairs of transfer gates (G1 and G2) for applying a lateral electric field along the carrier path. The depleted potential gradient along the channel is transformed by the supply bias voltages that are supplied by the LEFM gates. As shown in Fig. 1(b), an electron generated in the aperture area (light-sensitive area) is transferred to the storage diodes (SDs) (n_2 regions) by the different LEFM gate voltages. Simultaneously, a very steep potential gradient is formed that facilitates high-speed charge transfer in the charge modulator. LEFM gating also has the advantage of eliminating the backward charge re-transfer that can occur in conventional transfer gates, thus resulting in a significant increase in the SNR.

A. Design of the Proposed Lock-In Pixel Using LEFM

Fig. 2 shows a pixel layout, an equivalent circuit schematic of the proposed four-tap LIP, and a whole image of the designed pixel architecture with a pixel-level PG for LEFM gates. The entire pixel area that includes a light-sensitive region and charge SDs is covered by a p+ pinning layer to reduce dark current and to achieve complete charge transfer. The pixel comprises a pinned photodiode (PPD), four pinned SDs (PSDs), four pairs of LEFM transfer gates (TGs) (TG1–TG4), in which each transfer gate is equipped with a charge drain gate (TD) for draining unnecessary signal electrons, and a PG block that enables rapid charge modulation, as shown in Fig. 2(a). As can be seen in the equivalent pixel schematic of Fig. 2(b), each of the four source followers (SFs) for reading the signals from the PSDs is connected to a low-noise column analog-to-digital converter (ADC), following the correlated multiple sampling (CMS) technique [25]–[27]. The gates, TGs and TD, modulate the signal charges at the aperture area. According to the LEFM-control clocks (CK_TG1–CK_TG4), the signal charge is transferred to the targeted PSD from the PPD (see Fig. 9). After each gating operation finishes, the TD gate is always opened by a CK_TD pulse to flush superfluous charges in the PPD and to simultaneously reduce the parasitic light sensitivity (PLS). Each PSD has a large full-well capacity (FWC) of 5500 electrons. Fig. 2(c) is a whole image of the actual layout of the TR pixel with two light-sensitive areas and a shared PG block. One in-pixel PG block for generating extremely narrow TWs is shared between the LEFMs of two pixels to fit more pixels into the same sensor area. The size of two pixels with a shared PG block is $44.8 \mu\text{m} (\text{H}) \times 22.4 \mu\text{m} (\text{V})$, and the effective pixel size

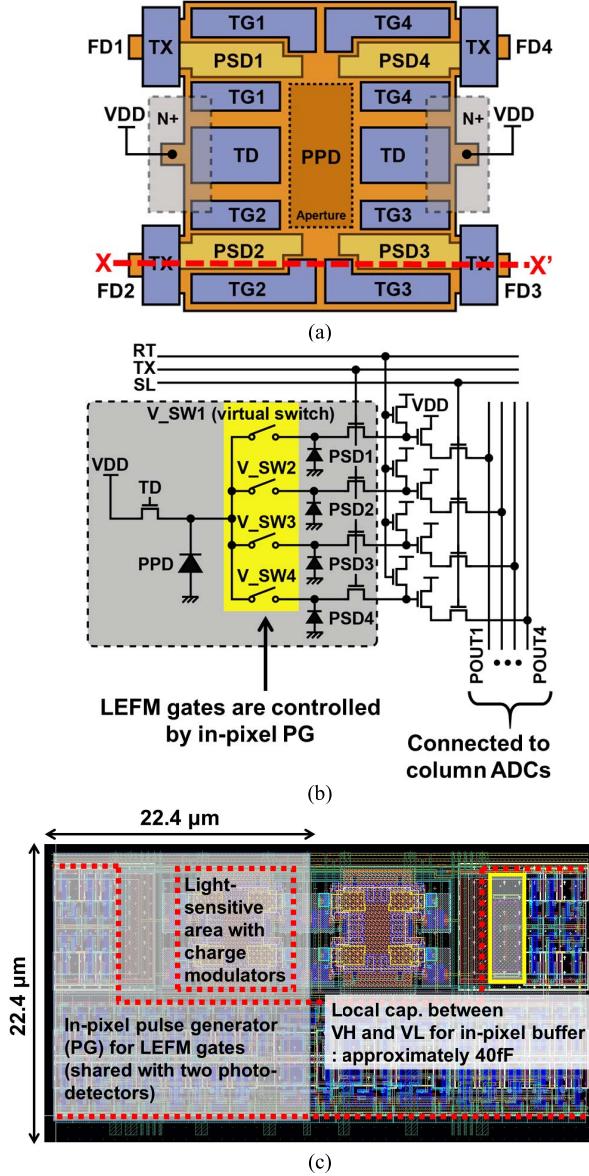


Fig. 2. Developed four-tap CMOS LIP. (a) Layout. (b) Equivalent schematic. (c) Whole image of the pixel architecture with an internal PG for LEFM gates.

is $22.4 \mu\text{m}$ (H) $\times 22.4 \mu\text{m}$ (V). In addition, a 40-fF local capacitor is placed in each PG block between the power lines (VH and VL) to instantaneously provide a large current that drives the narrow gating TWs.

We used the SPECTRA device simulator to model the proposed pixel design, as shown in Fig. 3. Fig. 3(a) shows the 3-D potential distribution during the transfer phase ($\text{TG1} = \text{TG2} = \text{TG4} = \text{TD} = -1 \text{ V}$, $\text{TG3} = 2.2 \text{ V}$). As observed from the simulation, the potential barriers between the PPD and the PSDs are controlled properly by the voltages applied to the LEFM gates. Fig. 3(b) shows simulated signal carrier paths from the aperture area to the designated storage region, which is PSD3 in this case. The red dotted circles denote the initial positions of photo-induced electrons and the black dotted lines indicate the trajectory of the electrons. The region in which electrons are accumulated is determined by the gate voltages of TG1, TG2, TG3, TG4,

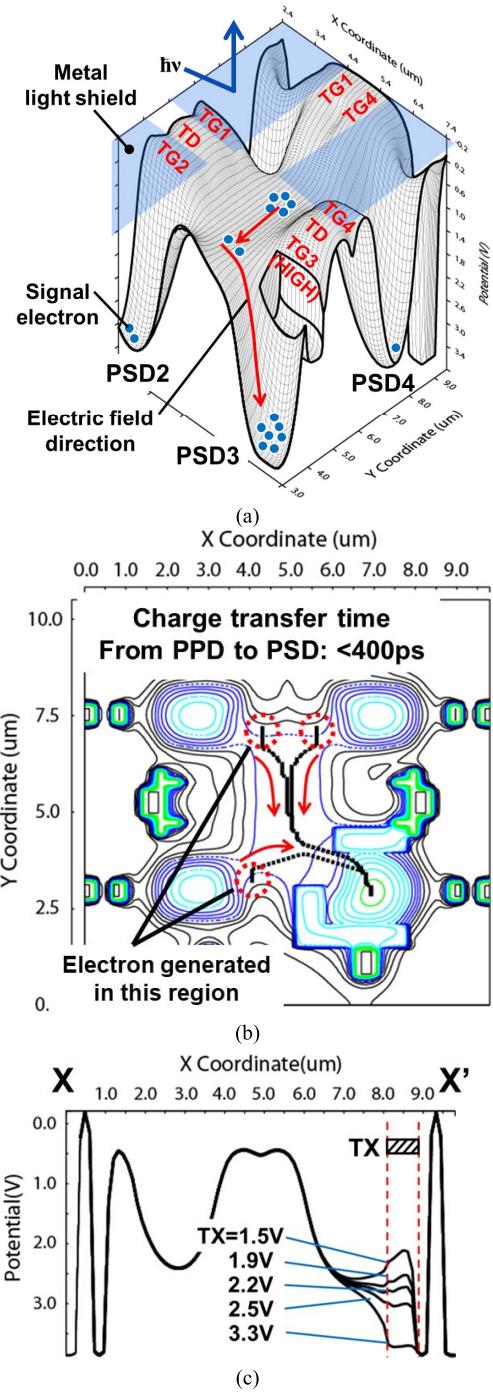


Fig. 3. Device simulation results when TG3 is only activated. (a) 3-D device simulation. (b) Signal carrier traveling path with the equipotential lines during charge transfer mode. (c) Two-stage charge transfer with varying the voltage of TX gate.

and TD. This simulation confirmed that the charge-transfer time from the initially generated position to PSD3 should be less than 400 ps even if the initial position is far away from PSD3.

Finally, Fig. 3(c) shows a depleted potential diagram along the line from X to X' (see Fig. 2). This allowed us to confirm that two-stage charge transfer from the PSD to a floating diffusion (FD) node is possible. Two-stage charge transfer is very important for achieving the low-noise signal

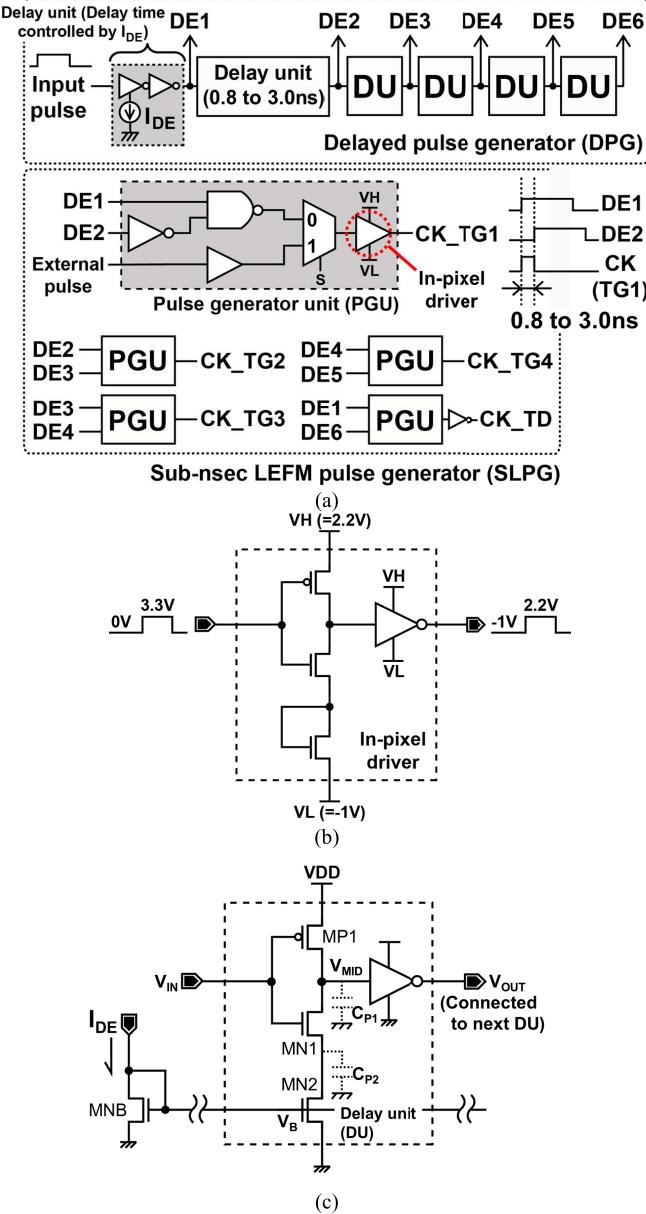


Fig. 4. In-pixel PG for sub-nanosecond time gating. (a) Block diagram of in-pixel PG. (b) Schematic of in-pixel driver with a diode-connected transistor. (c) Schematic of tunable DU.

readout because truly correlated-double sampling (CDS) is implemented with two-stage charge transfer. As observed from the simulation result, the barrier between the PSD and FD nodes is well controlled by TX gate voltages, from 1.5 to 3.3 V. No potential pocket or barrier occurs when a high driving voltage is applied to the TX gate (ON state).

B. In-Pixel Pulse Generator for Sub-Nanosecond Time Gating

Fig. 4 shows the PG blocks that generate TWs narrower than 1 ns. The internal PG block can be divided neatly into two parts, as shown in Fig. 4(a). The first part is a delayed PG (DPG) with tunable delay units (DUs) that use an inverter chain, and the other is a sub-nanosecond LEFM PG (SLPG). An input pulse from the external timing generator enters into

the DPG via many repeater clock buffers on the chip to reduce the effect of parasitic capacitances. The input pulse is delayed by six DUs, and the delay interval can range from 0.8 to 3.0 ns. This interval sets the pulselength of the TW for charge modulation. The delayed pulses (DE1 to DE6) are fed in pairs to each PG unit (PGU) in the SLPG. The PGU comprises logic gates, a multiplexer that chooses between internal and external operating modes, and an LEFM driver. These in-pixel PG blocks allow a very narrow TW to be realized, which improves the sensor's time resolution. Fig. 4(b) shows the circuit schematic of in-pixel LEFM driver with a diode-connected NMOS transistor for supplying the negative voltage to the TG and TD gates. Through this driver circuit, the initial voltage range, 0 V to 3.3 V, is successfully shifted to the operation range of the LEFM gates, -1 V ($=V_L$) to 2.2 V ($=V_H$).

A detailed circuit schematic of each DU in the DPG is shown in Fig. 4(c). This schematic shows that the two-stage delay chain comprises a current-starved inverter (CSI) and simple CMOS inverter that supplies phase correction. The delay gate uses the structure of a logic inverter (transistors MP1 and MN1) and delays the output slope by discharging capacitances C_{P1} and C_{P2} (the junction capacitances of the MOS transistors). The drain current of MN2 is controlled by the bias voltage V_B . Depending on the transition of the input signal, the slew rate of the output signal is either controlled by the bias transistor, MN2 (for the rising input edge), or is determined by the strength of MP1 that pulls the output node up to V_{DD} (for the falling input edge). We also simulated DUs with different bias conditions using CAD circuit simulator.

The simulation results for DUs are presented in Fig. 5; these include the transitions of voltages V_{IN} [Fig. 5(a)], V_{MID} [Fig. 5(b)], V_{OUT} [Fig. 5(c)], and the waveform after the in-pixel buffer [Fig. 5(d)]. The transient response of Fig. 5(b) can be divided roughly into the following three periods: 1) an initial period in which V_{IN} is low, 2) a switching period during the transition of V_{IN} from low to high, and 3) a discharge period after V_{IN} changes from low to high. During the initial period, capacitance C_{P2} is discharged to zero through the bias transistor MN2 (for $V_B > 0$) and capacitance C_{P1} is charged to V_{DD} through MP1. During the switching period, the rising edge of V_{IN} switches MN1 ON and MP1 OFF. As a result, V_{OUT} approaches common level, V_{CM} , i.e., the point at which the discharge period begins. At the same time, the drain-source conductance of MP1 is decreased when the output node is practically disconnected from the power line. The bias transistor MN2 reduces the total current flowing through MP1 and MN1. The observed output voltage drop from V_{DD} to V_{CM} can be attributed to charge sharing between capacitances C_{P1} and C_{P2} . During the discharge period the high input voltage keeps MN1 fully turned on, which connects the junction capacitances of the MOS transistors, C_{P1} and C_{P2} , in parallel. The discharge rate of these capacitances depends primarily on the bias voltage V_B , which controls the gate of the bias transistor MN2.

For this simulation, the bias current I_{DE} was varied from 3 to 50 μ A at intervals of 1 μ A. First, a square-wave input signal (period = 15 ns and pulselength = 10 ns) was introduced

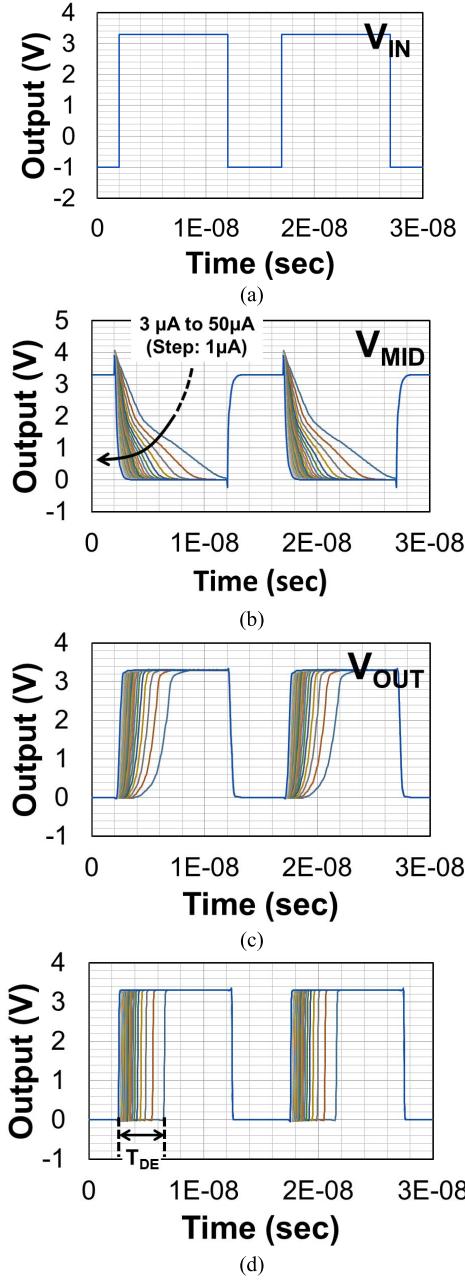


Fig. 5. Simulation results of tunable DU with the different bias currents (I_{DE}). (a) Input pulse. (b) Waveform of V_{MID} node. (c) Output waveform of DU. (d) Waveform after buffering.

into the first DU in the DU chain as shown in Fig. 4(a). Then according to the bias currents, the delay time T_{DE} changes exponentially as shown in Fig. 5(c) and (d). By using the programmable DU, the pulsewidth of TW can be varied flexibly from extremely fast time gating to relatively slow time gating depending on its applications.

C. Architecture of the Sensor Chip

Fig. 6(a) shows a fabricated chip micrograph. The sensor comprises an array of the four-tap TR LIPs described above [128 (H) \times 128 (V)], internal pixel-level LEFM PGs for the gates (TG1, TG2, TG3, TG4, and TD), an inverter tree with the clock drivers, low-noise, and wide-dynamic-range

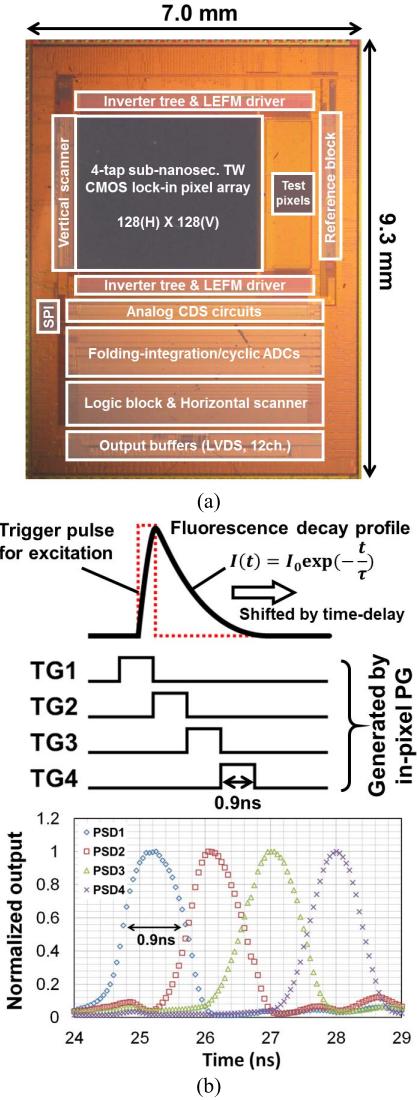


Fig. 6. Fabricated chip. (a) Micrograph. (b) Simplified timing with sub-nanosecond TWs.

column-parallel ADCs [26], [27] for signal output, a digital logic block for data processing, and a vertical/horizontal scanner for pixel addressing. Fig. 6(b) shows a conceptual measurement diagram using the four taps and measured output signals from each PSD while scanning a sample with a 472-nm pulsed laser diode (Laser pulselength: 120 ps). From this timing diagram, four points on the fluorescence decay profile are captured simultaneously by the generated sub-nanosecond TWs. This sampling strategy makes it possible to observe double-exponential decay components of the sample without TW scanning, and the combined data-sampling method with the multiple time gating and time sweeping can allow the more flexibility for the FLIM measurement. Through these methods with the multi-tap TR CIS, the FLIM measurement time is also dramatically reduced in comparison with conventional fully TW scanning methods [9]–[11]. To demonstrate the time-gating performance, a set of four TWs was shifted by an external delay controller at 50 ps time intervals. The charge generated in the PPD is clearly split into the four storage regions, from PSD1 to PSD4. We conclude

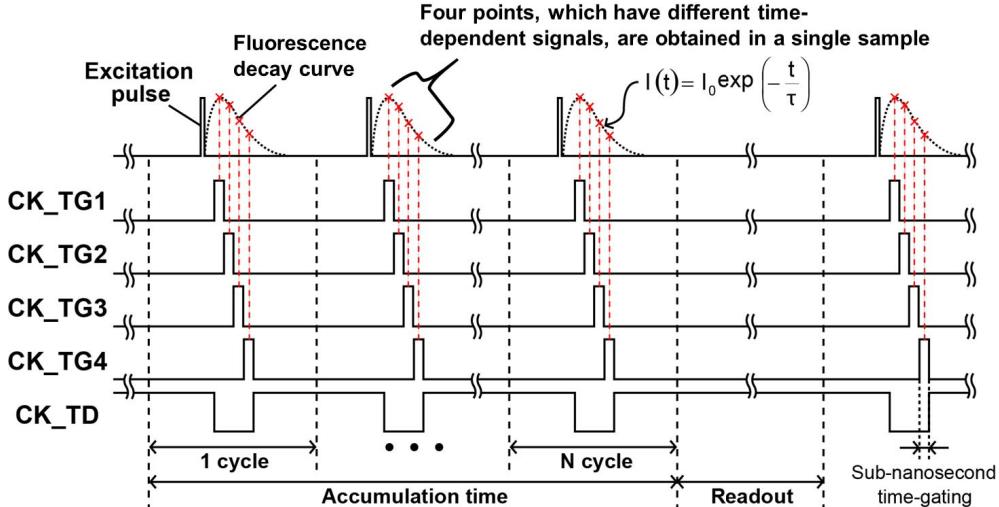


Fig. 7. Timing diagram for implementing the four-tap TR CIS.

that a high SNR real-time FLT measurement system can be realized by using the FLIM imager with sub-nanosecond time gating. More details of the prototype sensor operation are described in Sections III and IV.

III. IMPLEMENTATION AND PERFORMANCE OF PROTOTYPE TR CIS

We fabricated the above-described TR CIS with pinned PD 0.11- μm 1-poly 4-metal CMOS technology. The die size of the chip is 7.0 mm (H) \times 9.3 mm (V) as shown in Fig. 6(a). In this section, we discuss the operation of the TR CIS in terms of fundamental sensor performance.

Fig. 7 shows the timing diagram for operating the four-tap TR CIS. This scheme has the following two parts: 1) an accumulation period (global shutter-type sensor operation) and 2) a readout period (typical rolling shutter-type sensor operation). During the accumulation period, four narrow TWs (CK_TG1, CK_TG2, CK_TG3, and CK_TG4) generated in the PG block are produced in sequence for capturing a signal from the target sample. CK_TD is always high for draining the uninteresting charges in the PPD unless one of the CK_TGs is high. In other words, each charge-accumulation cycle comprises four TWs for driving charge transfer to the PSDs and one draining pulse for the cleaning the PPD. To gather enough signal charges to achieve a sufficiently high SNR, many accumulation cycles are required. During the readout period, the charges accumulated in the PSDs are sampled through a low-noise column ADC. During this phase, CK_TD is always high, while the CK_TGs are low.

To measure the decay profile of emitted light from sample in a short time period, four-tap outputs of developed LIP are employed, as shown in Fig. 7. Four points (\times marks on decay curve), each of which have different time-dependent signals, are sampled by each cycle of the pixel operation. Compared with typical measurement methods [9]–[11], [20], [24], the proposed measurement method using four-tap outputs is more effective and can estimate the decay distribution much more quickly.

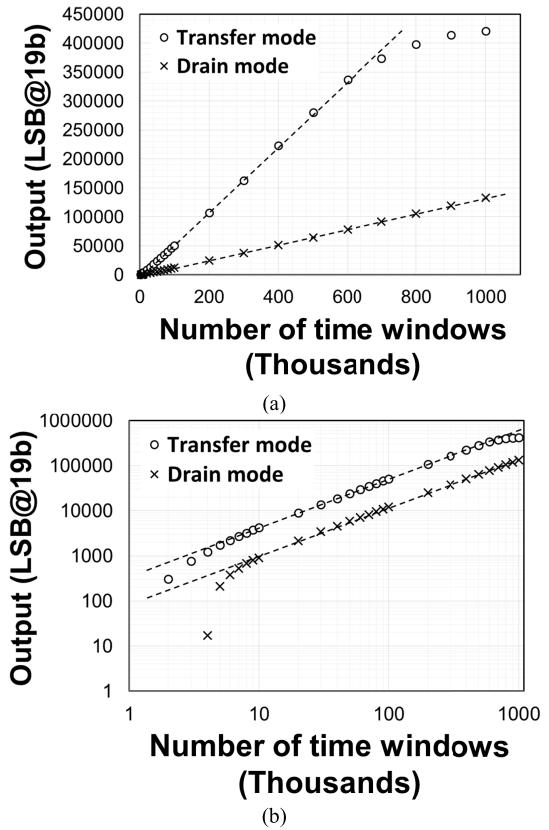


Fig. 8. Measured photoelectric conversion characteristics of the developed TR imager as a function of the number of TWs (@472 nm, width of TW = 2.4 ns). (a) Linear scale. (b) Logarithmic scale.

The linearity plots of the prototype TR CIS are shown in Fig. 8. Fig. 8(a) and (b) shows the linear characteristics as a function of the number of TWs (or light pulses) on linear and logarithmic scales, respectively. In this measurement, the number of TWs ranged from 0 to 1 million, and a 472-nm laser diode and a pulselwidth of TW of 2.4 ns were employed. Two plots, for operation in the charge-transfer

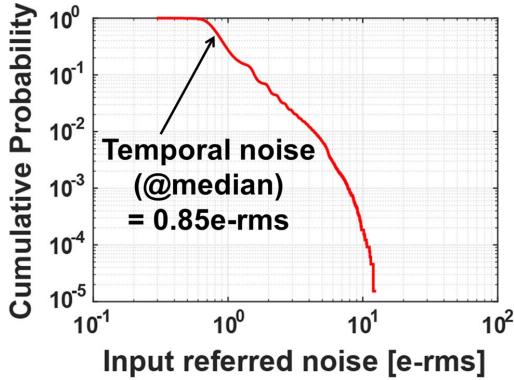


Fig. 9. Temporal random noise of the developed TR imager (@45 frames/s, analog gain = 128).

phase (\circ marks) and the charge-drain phase (\times marks) are included in the figure. In the charge-transfer phase, signal charges are captured and integrated by TW with the TD gateoff. In the charge-drain phase, however, control signals for the TWs (CK_TG1~TG4: normal operation and CK_TD: always high) are set to drain the charge generated in the PPD. The results show a quite high extinction ratio (ER) of approximately 81% even though we used a narrow TW for this measurement. This is a significant characteristic for achieving precise high-resolution FLT measurements.

Fig. 9 shows the input-referred temporal random noise of the developed TR CIS. An extremely low noise level is achieved for FLT imaging when chip-cooling is employed with the Peltier-embedded pin grid array (PGA)-type package. The measured noise level of 0.85 e-rms at the median value as attained with an analog gain of 128 and 45 frames/s sensor operation speed. Sub-electron noise performance is a greatly helpful feature for biomedical imaging applications.

Fig. 10 shows the measured intrinsic response of the developed TR CIS. In biological research, fast intrinsic response is essential for obtaining accurate measurements. The horizontal axis is the delay time of the TW, which is shifted from -0.3 to 1.25 ns at intervals of 50 ps. The narrow TW with 1-ns pulsewidth is used and the pulsed laser light which is perfectly synchronized the trigger signal from the sensor board is scanned and integrated by the TWs. To obtain the pure sensor response to the input signal, the integrated signal is differentiated. Then, the sensor response is reproduced as shown in Fig. 10(a), and it is termed the intrinsic response in the paper. Each value captured with a different delay time is calculated from the averaged pixel value with a selected region of interest (ROI), in this case, 10×10 pixels. The measured decay distributions are bounded by the intrinsic response of the imager unless complicated compensation techniques are used. Our proposed LIP imager has faster intrinsic response of 170 ps at 472 nm (FWHM: 120 ps and peak power: 48 mW), compared with the other state-of-the-art TR imaging devices [7]-[13], which will allow FLT measurements of sub-nanosecond length, using only simple deconvolution techniques. A pixel-to-pixel variation of the intrinsic response with the ROI is measured as shown in Fig. 10(b). The measured variation to the impulse response at 472 nm is 52 ps_{rms}. From

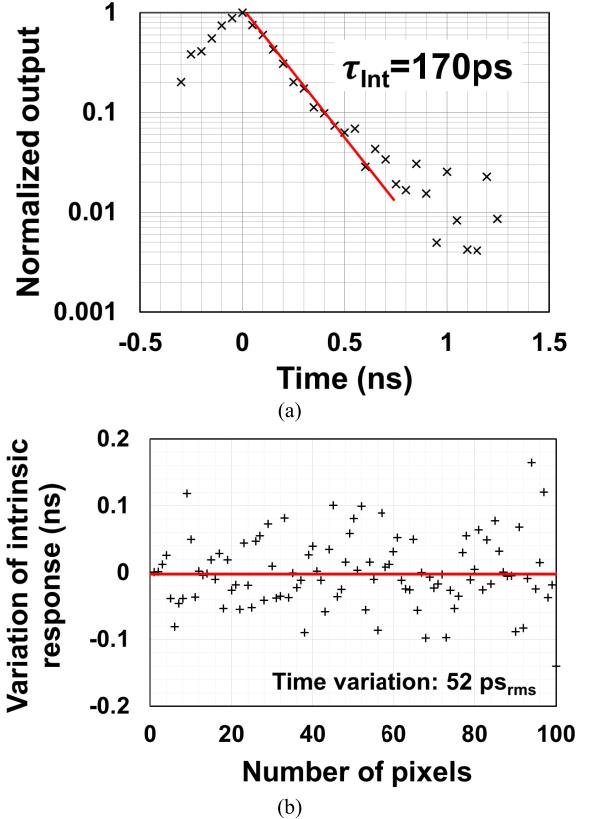


Fig. 10. Sensor response at 472 nm. (a) Intrinsic response. (b) Variation of the intrinsic response with 10 by 10 pixels.

this result, we confirmed that the pixel-to-pixel response of the prototype TR CIS is quite uniform.

Fig. 11 shows measurement results for confirming the function of the proposed in-pixel PG block with variable TWs. As mentioned earlier, the DUs' performance directly affects the width of TW. We measured and plotted the output values of the prototype CIS with different TW widths that were scanned by a 472-nm pulsed laser light source. To vary the width of TW, a range of bias currents (I_{DE}), 3.6, 4.8, 20.0, and 50.0 μ A, were supplied to the DU. The width of the TW is determined by the delay time (T_{DE}) of the DU, and the dominant component for deciding the delay time is the discharge time (T_{DISCH}) of the parasitic capacitances, C_{P1} and C_{P2} . This discharge time can be expressed by the following simple formula:

$$T_{DISCH} = (C_{P1} + C_{P2}) \cdot \frac{V_{CM} - V_P}{I_{DE}} \quad (1)$$

where C_{P1} and C_{P2} are the junction capacitances of the MOS transistors, V_{CM} is the common level that denotes the starting point for the discharging period of C_{P1} and C_{P2} after changing V_{IN} from low to high [approximately $V_{CM} = V_{DD} \times C_{P1}/(C_{P1} + C_{P2})$], and V_P typically equal $V_{DD}/2$ terminating the generated time interval T_{DE} . As mentioned in Section II, the width of TW is varied by mainly I_{DE} in the DU and each pixel has six DUs. It leads to increase a momentary current flow and can sometimes cause a severe IR drop problem. In addition, the clock skew partially subserves the TWs' asymmetry. As a result, the width uniformity of TWs

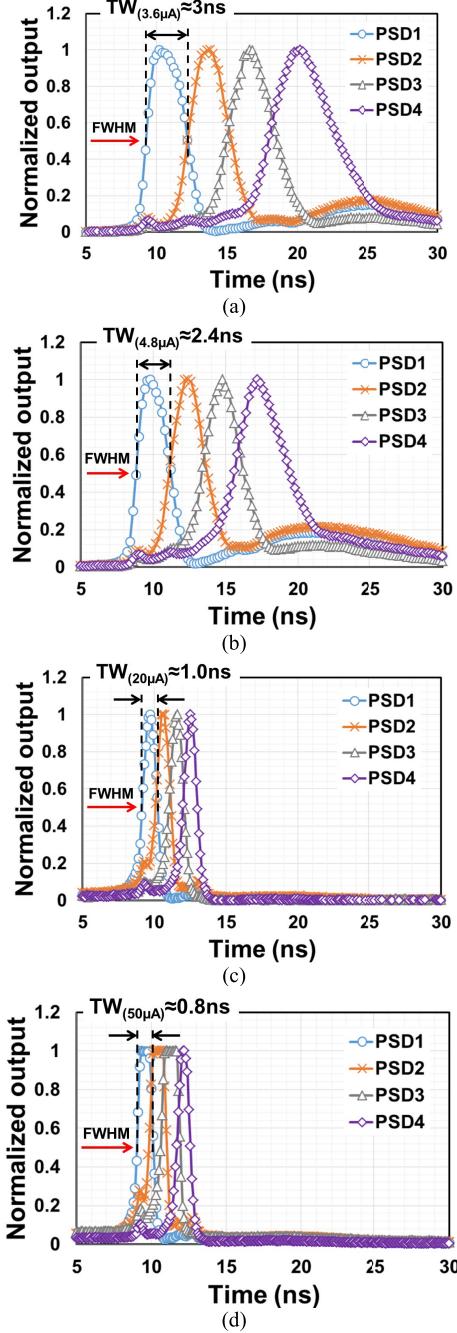


Fig. 11. Programmable TW by using in-pixel PG. (a) $I_{DE} = 3.6 \mu A$. (b) $I_{DE} = 4.8 \mu A$. (c) $I_{DE} = 20.0 \mu A$. (d) $I_{DE} = 50.0 \mu A$.

is varied by the bias current. The evaluated results with four different bias cases are as follows: 1) time variation of TWs (t_{TW_VARI}) = $0.94 \text{ ns}_{\text{rms}}$, when $I_{DE} = 3.6 \mu A$; 2) $t_{TW_VARI} = 0.62 \text{ ns}_{\text{rms}}$, when $I_{DE} = 4.8 \mu A$; 3) $t_{TW_VARI} = 0.05 \text{ ns}_{\text{rms}}$, when $I_{DE} = 20 \mu A$; and 4) $t_{TW_VARI} = 0.17 \text{ ns}_{\text{rms}}$, when $I_{DE} = 50 \mu A$. From the results, the TW variation is minimized with the bias current of $20 \mu A$ as shown in Fig. 12, and this bias setup is used for all TR measurements in this paper. The signal crosstalk between each tap is occurred due to the parasitic RC components and the clock skew, and it is sometimes employed to generate the signal offset and degrade the signal dynamic-range. In this case, however,

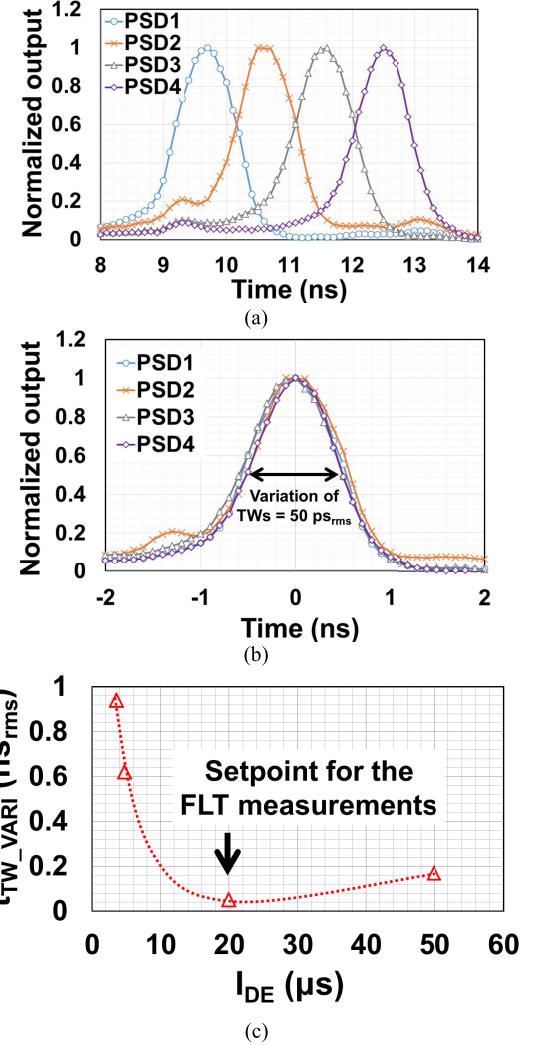


Fig. 12. Time-gated output at $I_{DE} = 20 \mu A$. (a) Enlarged. (b) Time-shifted. (c) Variation (rms value) of tap-to-tap width.

the TW variation and the amount of the crosstalk are allowably small and uniform at $I_{DE} = 20 \mu A$ as can be seen from Fig. 12(a). Thus, the tap-to-tap offset, which is generated by a non-uniformity of TW, can be relatively easily compensated by the off-chip processing. In addition, photo-response non-uniformity (PRNU) of the developed TR CIS is measured to confirm the spatial uniformity. The measured PRNU is 0.6% at $I_{DE} = 20 \mu A$ and it has sufficiently good spatial uniformity. In Fig. 11(a) and (b), the secondary distributions are observed, because some slow charge components, which are generated in a deep-depletion region of the PPD, are simultaneously overflowed to the all PSDs after finishing all time-gating operations. These secondary distributions can be ignored when the FLT are calculated and solved by using the biased-substrate structure. Even though some components limit practical time gating with our developed TR CIS, the measured time-gating capability is sufficiently rapid and flexible, as shown in Figs. 11 and 12. The measured TW widths are compared with simulated results in Fig. 13. In this plot, the supplied bias current is the independent variable, and the TW width is the dependent variable, which is plotted for each case with a

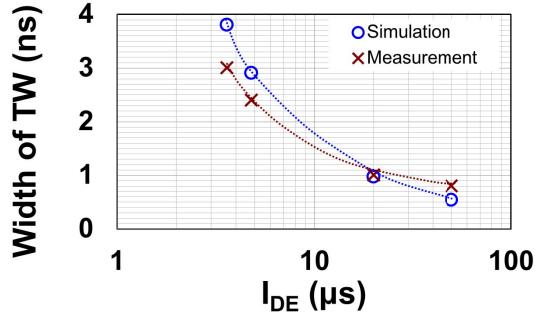


Fig. 13. Measured TW with different bias currents (I_{DE}).

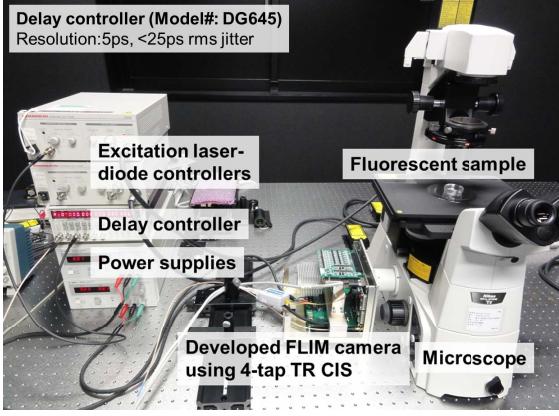


Fig. 14. Measurement setup for FLT imaging.

simulated curve and measured points. The measurement results generally agree with simulations.

IV. EXPERIMENTAL RESULTS OF FLIM AND DISCUSSION

To measure the FLTs, the FLIM can be typically performed in the time and frequency domains [28], [29]. The frequency-domain FLIM using multi-tap TR CIS is suitable for faster measurements and it is also very effective to cancel the influence of the system response. Whereas, in case of the time-domain FLIM, it can observe the whole decay profiles and the analysis of the acquired data is relatively simple. Basically, the developed FLIM system using the four-tap TR CIS can be operated both in the time and frequency domains. Fig. 14 shows a photograph of the prototype time-domain based FLT measurement setup. The system comprises a microscope, an excitation light source with a controller, a high time-resolution delay controller (model no. DG645, 5 ps time resolution, <25 ps rms jitter) for shifting the excitation trigger signal, and our self-developed four-tap LIP TR CIS for capturing FLT images. The measurement system volume can be miniaturized and optimized with an internal delay controller (on-chip or on-board) and a smaller light source module.

The measurement results for testing the four-tap LIP are shown in Fig. 15. To capture the images in Fig. 15(a) and (b), an array of four-tap TWs are shifted by the external time-delay controller. The measurement conditions are as follows: delayed time from the origin ($\Delta t_d = 0$ ns) Δt_d is 1.6 ns, TW width is 2.4 ns, sample is a fluorescent microbead (product no. F8838, size: 15 μ m, measured lifetime: approximately 3.7 ns), and

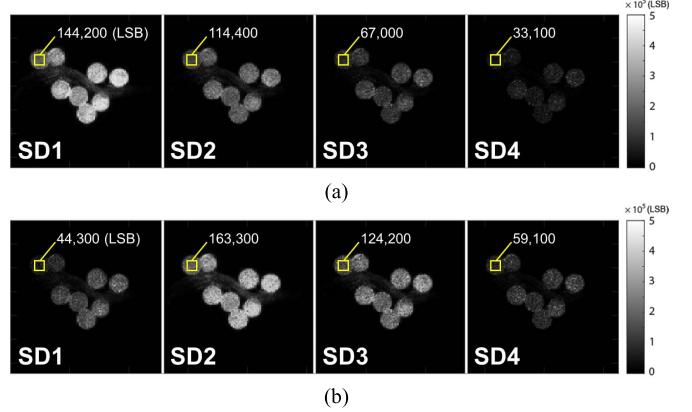


Fig. 15. Captured images of fluorescent microbeads with different time delays (@Ex. 374 nm, width of TW = 2.4 ns). (a) $\Delta t_d = 0$ ns. (b) $\Delta t_d = 1.6$ ns.

the excitation wavelength is 374 nm. In addition, the excitation light is limited by an optical bandpass filter embedded in the prototype measurement system, as shown in Fig. 14. As can be seen from Fig. 15, different time-dependent signals are captured by each TW, which are sequentially driven by the pixel-level PGs. The values in the yellow boxes express the averaged signal output as LSBs. These results demonstrate that fluorescent decay profiles can be estimated effectively using the proposed FLIM system with the developed four-tap TR CIS.

The FLTs of different types of fluorescent acrylic panels (blue, green, and orange) were measured as shown in Fig. 16. Fig. 16(a) shows the FLT measurement results while using a conventional time-gating method with a time delay. The measured FLT values are very close to the reference FLT values, those were measured by a TCSPC system. For example, the measured FLT of the blue acrylic panel = 1.0 ns (reference value = 0.9 ns), of the green acrylic panel = 3.0 ns (reference value = 3.0 ns), and of the orange acrylic panel = 6.4 ns (reference value = 6.7 ns). An exposure time for each sampled point is 24.4 ms. Total data acquisition times, which exclude the data dumping time to a measurement instrument such as a laptop computer, for measuring the blue, green, and orange acrylics, are 0.81, 1.3, and 1.46 s. We did not use any compensation method such as deconvolution for this test, because the intrinsic response of the developed TR CIS is sufficiently fast to observe the lifetime components larger than 500 ps. But the deconvolution method is still very attractive and an effective signal processing tool for improving the measurement accuracy. Fig. 16(b) demonstrates the effectiveness of the four-tap pixel using the narrow TWs. Only two or three frames are necessary for accurately estimating the sample's FLT decay curve.

Fig. 17 shows a color FLT image of a HeLa cell with 4', 6-diamidino-2-phenylindole (DAPI) (nucleus), bound to F-actin, and ATTO488 modified with phalloidin. These markers are excited by a 374-nm laser diode (pulse FWHM: 74 ps maximum peak power: 47 mW) and a 472-nm laser diode (pulse FWHM: 120 ps, maximum peak power: 48 mW), respectively. The image of Fig. 17(a) is an intensity image of the fluorescent sample that is captured by the prototype TR

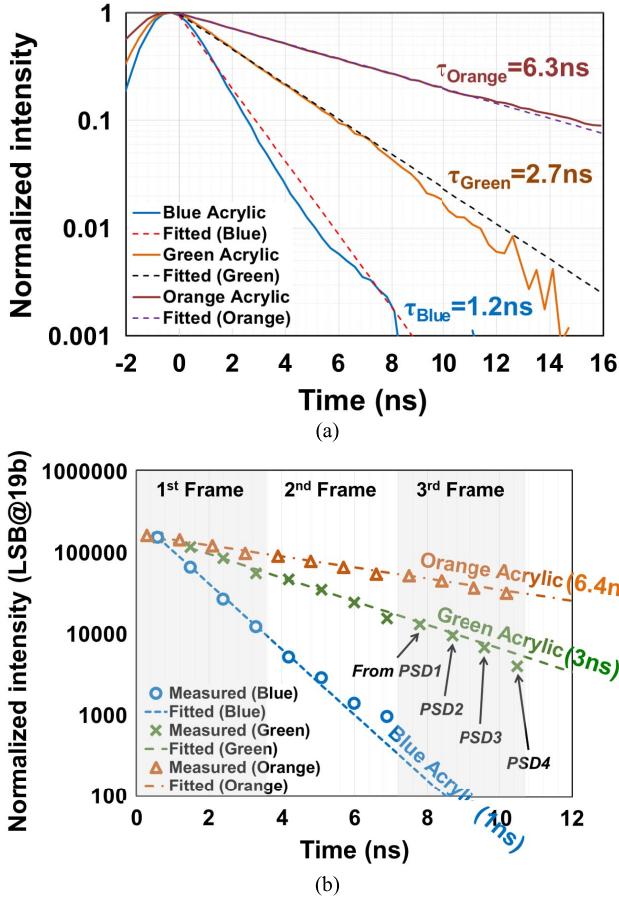


Fig. 16. FLT measurement results from fluorescent acrylics. (a) Single-tap measurement. (b) Four-tap measurement.

TABLE I
PERFORMANCE SUMMARY

Parameter	Value
Process technology	0.11 μm 1P4M CIS process
Total area	7.0 (H) mm X 9.3 (V) mm
Number of effective pixels	128 (H) X 128 (V)
Pixel size	22.4 (H) μm X 22.4 (V) μm
Number of output ports (per pixel)	4
Conversion gain	133 $\mu\text{V/e-}$
Full well capacity (@ SD)	5,500 e-
Fill factor	3.5 % (w/o ML), 26.3 % (w/ ML)
Full scale of ADC (ΔV_{REF})	0.75 V
Temporal random noise (@ 45 fps)	0.85 e-rms (@ median value)
Intrinsic response (@ 472nm LD)	170 ps
Pulse width of TW (using in-pixel PG)	0.8 ns to 3.0 ns
PRNU (@ time-gated mode)	0.6 %
Frame rate (Max.)	45 fps
Power consumption (@ 45 fps)	600 mW

CIS with 472-nm excitation. The observed FLT components of DAPI (maximum emission wavelength = 461 nm) and ATTO488-phalloidin (Emission wavelength = 523 nm) are

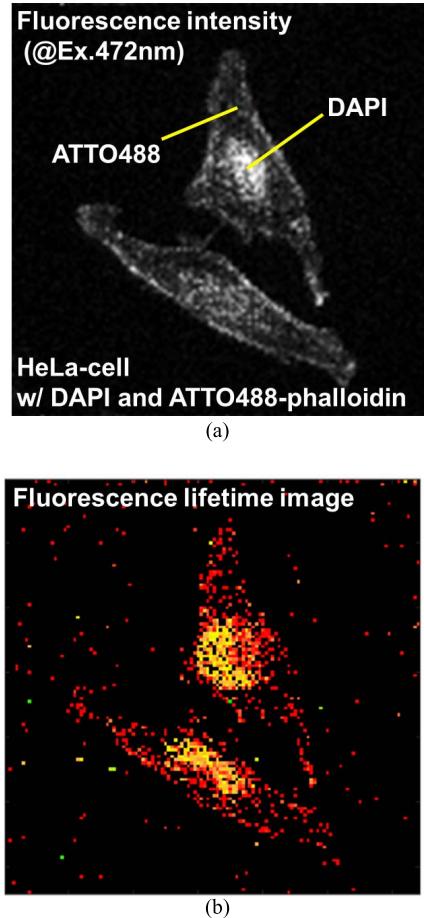


Fig. 17. Captured images. (a) Monochrome fluorescence intensity. (b) Color mapped FLT on HeLa-cell with DAPI bound to F-actin and ATTO488 modified with phalloidin (@DAPI: Ex. 374 nm, Emi. 461 nm; ATTO488: Ex. 472 nm, Emi. 523 nm).

mapped with different colors, as shown in Fig 17(b). In this measurement, single tap of the developed TR CIS is used for eliminating the uncertain component such as a tap-to-tap sensitivity variation, and an exposure time for obtaining the FLT image is set to 65.8 ms. The measured FLTs of DAPI and ATTO488-phalloidin were approximately 3–4 ns and 5–6 ns, respectively. A remarkably clear FLT image of a single cell is captured by the FLIM system even though the two FLT values of DAPI and ATTO488-phalloidin are quite close. The sensor performance and characteristics are summarized in Table I. This TR CIS has an extremely low temporal random noise level of 0.85 e-rms at 45 frames/s, large FWC for each PSD at 5500 e-, and a high pixel-conversion-gain of 133 $\mu\text{V/e-}$, as well as the very fast intrinsic response of 170 ps at 472 nm. A fill factor (FF) of the developed LIP with LEFM is 3.5 % without a microlens (ML), but the effective FF with the on-chip ML can be increased up to approximately 26%. A small FF is one of the weaknesses of the LEFM-based LIP image sensors. This disadvantage can be improved by using a backside illuminated (BSI) and a multiple (≥ 3) charge transfer pixel structures.

Table II compares our prototype's performance with that of other state-of-the-art fluorescence imaging devices. Owing to the pixel-level PG block, the proposed four-tap LIP has a large

TABLE II
COMPARISON WITH STATE-OF-THE-ART FLUORESCENCE IMAGING DEVICES

Number of pixel	Detector type	Pixel size (μm)	Number of taps	CG ($\mu\text{V/e-}$)	Fill factor (%)	Random noise (e-)	FWC (e-)	Intrinsic response (ns)	Ref.
212(H) 212(V)	Optional EM-CCD	17	2	0.43 (LSB/e-)	44	13.72	not stated	not stated	JBO'12 [1]
160(H) 120(V)	SPAD	15	1	16.5 (mV/ph.)	21	1.33 (mV, pixel noise)	not stated	not stated	JSSC'16 [3]
1024(H) 1024(V)	CMOS lock-in pixel	5.6	2	not stated	39 (@QE)	45	45k	not stated	[6] & SPIE'15 [7]
256(H) 256(V)	CMOS lock-in pixel (DOM)	7.5	1	80	4.6	2.0	3.8k	2.0 (@374nm)	TED'12 [10]
512(H) 310(V)	CMOS lock-in pixel (DOM)	5.6	1	not stated	5.6	not stated	not stated	0.15 (@374nm)	JJAP'16 [11]
128(H) 256(V)	CMOS lock-in pixel (LEFM)	11.2	2	76.3	12.3	1.2	6.93k	0.46 (@472nm)	TBioCAS'17 [13]
128(H) 128(V)	CMOS lock-in pixel (LEFM)	22.4	4	133	3.5 (w/o ML) 26.3 (w/ ML)	0.85 (@30fps)	5.5k	0.17 (@472nm)	This work

pixel pitch. However, excluding the pixel size, the prototype shows the sensor performance characteristics requisite for improving its time-resolving capability over the performance of comparable imaging devices, such as a large capacity for in-pixel storage, higher pixel-conversion gain, better noise performance, large FWC, and a fast intrinsic response.

V. CONCLUSION

This paper proposes and tests a sub-nanosecond time-gated four-tap CMOS LIP image sensor that is intended to be used in solid-state FLIM imaging systems. A very narrow TW (<1 ns) and short intrinsic response time are achieved by optimizing the pixel structure and eliminating any potential barrier between the PPD and PSD. In addition, using a novel four-tap LIP architecture with sub-nanosecond TWs, double-exponential decay components can be measured in a single frame or only a few frames. Thus, the FLT measurement time can be reduced drastically, thus making a real-time FLT imaging system feasible.

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