

A 65-nm CMOS Low Dropout Regulator Featuring >60-dB PSRR Over 10-MHz Frequency Range and 100-mA Load Current Range

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Abstract—One of the most critical attributes of low dropout regulators (LDOs) in increasingly complex systems on chip (SoCs) is high-power supply rejection ratio (PSRR), not only over a wide frequency range but also over a large load current range. This paper presents an LDO, realized in 65-nm CMOS, featuring >60-dB PSRR over a 10-MHz frequency range and a 100-mA large load current range. The high PSRR is achieved by an adaptive feed forward ripple cancellation (FFRC) technique embodying an adaptive load current tracking scheme. By means of embodying an NMOS-based power stage, the LDO also achieves very low dropout voltage of 80 mV and features very small overshoot and undershoot of 2 and 4 mV, respectively.

Index Terms—Feedforward ripple cancellation (FFRC), frequency compensation, high power supply rejection ratio (PSRR), low dropout regulator (LDO), system on chip (SoC).

I. INTRODUCTION

ADVANCED systems on chip (SoCs) employ increasingly lower voltage supplies and feature denser integration and higher operation speed, in part by the ever-decreasing feature size of CMOS fabrication processes. In view of the low supply voltage and the ensuing reduced signal swing, it is imperative that the noise in the supply voltage is commensurably low, particularly for submodules that are sensitive to supply noise, such as high-performance data converters, low-noise RF amplifiers [1], and phase-locked loops [2].

The power management for complex SoCs typically involves several switching regulators followed by several low dropout regulators (LDOs). Because the output of a switching regulator is noisy where the switching noise is typically several tens of millivolts, it is imperative that the power supply rejection ratio (PSRR) of the LDO is high over a wide frequency range and large load current range. The former is increasingly important in view of recent efforts to realize switching regulators whose switching frequency extends to the megahertz range to reduce the size of the off-chip passive components [3], [4]. The latter, on the other hand, is imperative in view of the increasing complexity and wide space (load

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current) variations [5] of modern SoCs. Similarly, it is also not surprising that analog circuits, such as voltage references [6] and switching class D amplifiers [7], also emphasize high PSRR.

The reported approaches to obtain high PSRR in LDOs include the pre-regulated supply means [8]–[10] and the feedforward ripple cancellation (FFRC) method [11]–[17]. The former is realized by additional circuits such as the cascode transistor topology [9], [10] and passive low-pass filter [8]. However, as the additional circuits are in series with the LDO power transistor, the dropout voltage can become intolerably high (e.g., >0.5 V), thereby compromising the power efficiency. FFRC, on the other hand, is advantageous as the dropout voltage is not compromised. This is because FFRC involves the augmentation of a parallel feedforward signal path from the power supply to the LDO output to mitigate the supply noise transmission. The effectiveness of the FFRC technique is largely ascertained by the gain of the said augmented feedforward signal path, where the optimal feedforward gain is a dynamic parameter that varies with the load current [12], [13]. A reported FFRC LDO [11] featuring a constant feedforward gain improves PSRR but only within a limited space variation, i.e., a limited load current range of 1–25 mA. Several reported approaches have attempted to address this. For example, a reported design [14] adopted a built-in 1-bit quantizer to alter the feedforward gain based on the load current condition. However, this approach is effective only to a limited extent due to the coarse quantization. Another reported approach [13] adopted the gain calibration methodology, but the hardware overhead penalty is somewhat high. An improved design [12] suggested a variable-gain feedforward path and demonstrated good PSRR over a wider load current range (from 10 to 140 mA). However, the efficacy of this approach is limited under light-load conditions, e.g., <10 mA. In short, although the design art of FFRC LDO is somewhat mature, state-of-the-art LDOs remain inadequate to provide high PSRR over a wide frequency range and over a large load current range.

In the perspective of low dropout voltage, the NMOS LDO (i.e., an LDO embodying an NMOS transistor for the power transistor) [18]–[21] is sometimes used instead of its PMOS LDO counterpart. This is because the common drain power stage of the NMOS LDO can tolerate lower dropout voltage without deteriorating its static output accuracy [19].

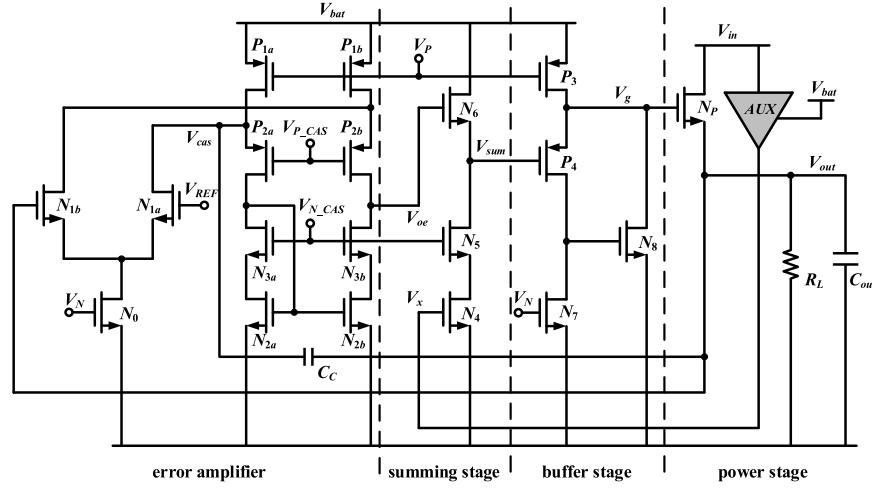


Fig. 1. Schematic of the LDO.

Furthermore, the NMOS LDO features lower output impedance, thereby leading to a small overshoot and undershoot during load transients [19], [20], [22]. Nevertheless, one shortcoming of the NMOS LDO is that the gate voltage of the NMOS power transistor may exceed the input voltage of the LDO, particularly when dropout voltage is low. To accommodate this, the NMOS LDO requires a higher supply voltage for the control circuit therein to provide an appropriate power transistor gate voltage [18]–[21]. This need for higher supply voltage is easily accommodated in SoCs because of the available power sources to the SoC (e.g., the battery) [19], [21].

In this paper, we present an NMOS LDO featuring a high PSRR (>60 dB up to 10 MHz) and over a large load current range (100 μ A–100 mA). The high PSRR is achieved by means of an adaptive FFRC technique embodying an adaptive auxiliary amplifier with a gain-tracking feature to adaptively adjust its gain to the optimal value, independent of the load current variations. We employ an NMOS power transistor to obtain two attractive attributes. First, the LDO achieves a low dropout voltage—the worst case of 80 mV when the load current is 100 mA. Second, the LDO achieves a competitive small overshoot and undershoot of 2 and 4 mV, respectively, when measured from a 100-mA output current transient with 1 μ s rising/falling time. The static current dissipation of the LDO realized in 65-nm bulk CMOS process is ~40 μ A.

Section II delineates the design of the LDO and the pertinent design considerations. Section III describes the measurement results of the LDO, and Section IV draws the conclusion.

II. DESIGN OF THE LDO

This section delineates the design of the LDO, and the pertinent design techniques and considerations. Simulations are also provided to verify the analysis and derivations thereto.

Fig. 1 depicts the schematic of the LDO comprising an NMOS power transistor (N_P), the adaptive auxiliary amplifier (AUX), an error amplifier (EA), summing stage (SUM), buffer stage (BUF), and frequency compensation capacitor (C_C). The load of the LDO is modeled as a resistor (R_L) with an output capacitor (C_{out}). The LDO requires two power supplies,

V_{bat} and V_{in} , respectively, the battery voltage and the input of the LDO. V_{bat} provides power for all the sub-clocks, save for N_P . V_{in} , on the other hand, is the output of the switching regulator and provides power for N_P , and is also the input of the adaptive AUX.

In this schematic, the NMOS power transistor enables a low dropout voltage of ~80 mV when the load current is 100 mA (see Section II-C). Furthermore, it enables a small output impedance attribute leading to small overshoot/undershoot during load transients. The adaptive AUX improves the PSRR with low overheads in terms of power, area, etc., thereby offering an adequately high PSRR at frequencies of interest (e.g., 100 kHz–10 MHz when V_{in} is the output of a switching regulator). Of particular interest, the gain-tracking scheme adaptively optimizes the PSRR over a large load current range (see Section II-A). The BUF serves to drive N_P and features a wide bandwidth of ~60 MHz by employing a shunt feedback transistor N_8 . The wideband feature of the BUF facilitates the stability of the LDO and assures the effectiveness of the AUX over a wide frequency range.

In Sections II-A–II-C, we will delineate the LDO in the perspective of PSRR, stability, and dropout voltage, respectively.

A. Power Supply Rejection Ratio

Fig. 2 depicts the conceptual block diagram of the LDO, where the error amplifier, summing stage, buffer stage, and the adaptive auxiliary amplifier are denoted as EA, SUM, BUF, and AUX, respectively.

The two noise sources in Fig. 2 include the battery output ripple at V_{bat} and the switching regulator output ripple at V_{in} . In an NMOS LDO, the noise at V_{in} is usually of primary interest [21]. This is because, in an NMOS LDO, the current supplied by the battery is only to the control circuit and is low (e.g., collectively the EA, SUM, BUF, and AUX consume <1 mA). In view of this, the battery output ripple can be easily and significantly suppressed without incurring excessive IR drop at V_{bat} by placing a relatively large series

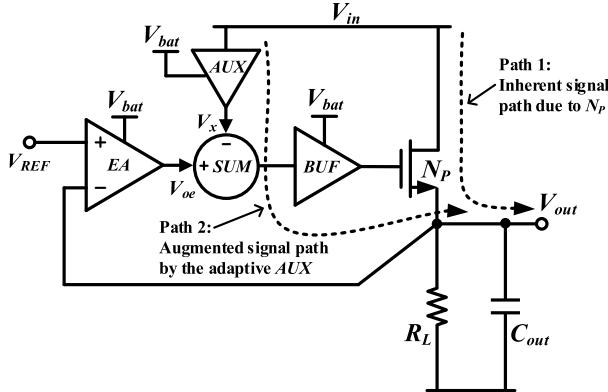


Fig. 2. Conceptual block diagram of the LDO.

resistor (e.g., $\sim 100 \Omega$) and an input capacitor (e.g., several microfarad) [23] at V_{bat} .

The PSRR of the LDO is enhanced by the mutual compensation of two signal paths from V_{in} to V_{out} , i.e., Path 1 (the inherent signal path due to the power transistor, N_P), and Path 2 (the augmented signal path by the adaptive AUX). Consider now this mutual compensation mechanism.

On the basis of Mason's gain formula [24], the PSRR of the LDO is

$$\text{PSRR} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{A_F(s)}{1 - L(s)} \quad (1)$$

where $A_F(s)$ is the feedforward gain from V_{in} to V_{out} , and $L(s)$ is the sum of the loop gain of the signal loops in the LDO.

From Fig. 2, $A_F(s)$ comprises two components, respectively, Path 1 and Path 2 from V_{in} to V_{out}

$$A_F(s) = g_{\text{dsp}} Z_{\text{out}} + A_x A_{\text{sum}} g_{\text{mp}} Z_{\text{out}} = g_{\text{dsp}} Z_{\text{out}} (1 - A_x A_{\text{int_p}}) \quad (2)$$

where

g_{dsp}	output conductance of N_P ;
Z_{out}	output impedance at node V_{out} ;
A_x	gain of the adaptive AUX;
A_{sum}	gain of the SUM and is designed to ~ -1 by appropriately sizing N_4 and N_6 (see Fig. 1);
g_{mp}	transconductance of N_P ;
$A_{\text{int_p}} = g_{\text{mp}}/g_{\text{dsp}}$	intrinsic gain of N_P .

From (1) and (2), the PSRR of the LDO can be optimized by ascertaining that $A_F(s) = 0$, specifically that $A_x = 1/A_{\text{int_p}}$.

Fig. 3 depicts the conceptual block diagram of the adaptive AUX whose gain is $A_x = V_x/V_{\text{in}} = 1/A_{\text{int_p}}$. The adaptive AUX comprises an OTA, feedback network (formed by R_{X1} and R_{X2}), NMOS (N_X), dependent current source (I_x , that provides dynamic biasing current to N_X), and an independent current sink (I_R , that sinks the current flowing through R_{X1} and R_{X2}). The output of the adaptive AUX V_x is the output of the OTA. A_x is designed to be equal to $1/A_{\text{int_p}}$ and can track its variations due to load current variations by two steps. First, A_x is designed to be equal to $1/A_{\text{int_x}}$, where $A_{\text{int_x}}$ is

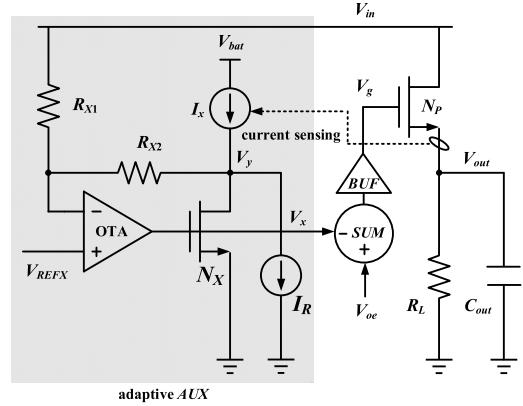


Fig. 3. Conceptual diagram of the adaptive AUX.

the intrinsic gain of N_X . Second, $A_{\text{int_x}}$ is designed to be equal to $A_{\text{int_p}}$ by means of realizing N_X as a scaled replica of N_P with a ratio of 1/500. We will now delineate these two steps in turn.

In Fig. 3, the OTA and NMOS (N_X) constitute a two-stage opamp, where V_y is the output of the said two-stage opamp. R_{X1} and R_{X2} form the feedback network, and they are designed to be identical so that $V_y/V_{\text{in}} = -1$. The gain from V_x (the output of the adaptive AUX) to V_y largely equals to $-A_{\text{int_x}}$ because the output resistance of the current sources, I_x and I_R , and the resistance of R_{X2} are designed to be substantially larger than the output resistance of N_X . On this basis, A_x can be derived as

$$A_x = \frac{V_x}{V_{\text{in}}} = \frac{V_y/V_{\text{in}}}{V_y/V_x} = \frac{1}{A_{\text{int_x}}} \quad (3)$$

Fig. 4 depicts the schematic of the adaptive AUX, where $A_{\text{int_x}}$ is designed to be equal to $A_{\text{int_p}}$ by three means. First, as N_X is designed with the same channel length as the power transistor N_P , they experience the same degree of short channel effects. Second, N_X and N_P are designed to carry the same current density by a current sensing scheme and by the current sink I_R that minimizes the loading effect of R_{X1} and R_{X2} . Third, V_{ds} of N_X and V_{ds} of N_P are designed to be equal by a reference voltage, $V_{\text{REFX}} = V_{\text{in}} - V_{\text{out}}/2$, i.e., N_X is a scaled replica of N_P both in terms of geometry and biasing conditions. In this fashion, the adaptive $A_x (=1/A_{\text{int_p}})$ can innately track $1/A_{\text{int_p}}$ even when $A_{\text{int_p}}$ varies due to load current variations. The gain tracking capability of the auxiliary AUX degrades as ripple magnitude at V_{in} increases. This is because the gain of V_y/V_{in} is negative, and hence when V_{ds} of N_P increases as V_{in} increases, V_{ds} of N_X decreases, and vice versa. Nevertheless, as V_{in} is the output of switching regulator whose voltage ripple, in general, is of several tens of millivolt, the gain tracking capability of the auxiliary AUX is largely unaffected—e.g., our measurement (see Fig. 17) shows that the adaptive AUX can achieve ~ 20 -dB PSRR improvement despite 60-mV ripple on V_{in} .

The bandwidth of A_x ascertains the efficacy of the adaptive AUX over frequency, and the OTA in the adaptive AUX is dynamically biased (see Fig. 4) to improve the PSRR over

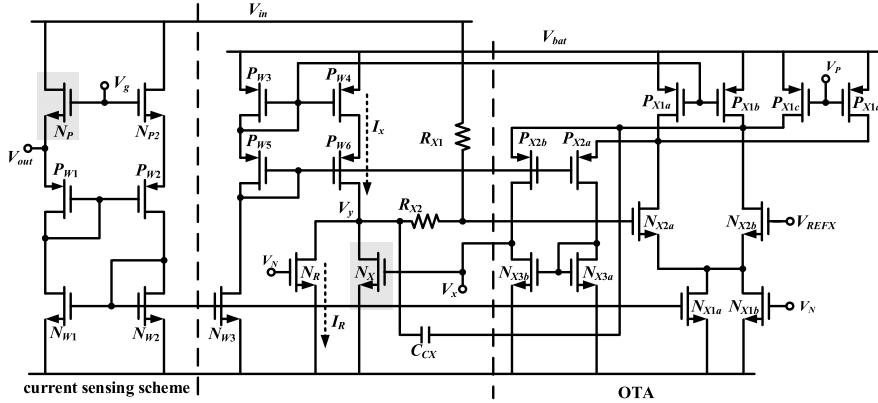


Fig. 4. Schematic of the adaptive AUX.

TABLE I
TRANSISTORS SIZE AND POWER BREAKDOWN OF THE LDO

Block (current)	Device	Parameter	Block (current)	Device	Parameter
Error amplifier in Fig. 1 (10 μ A)	N_0	2.4 μ m/0.6 μ m	Adaptive AUX in Fig. 4 (8 μ A)	N_{P2}	6 μ m/0.06 μ m
	P_{1a}, P_{1b}	6 μ m/1 μ m		P_{W1}, P_{W2}	128 μ m/0.2 μ m
	P_{2a}, P_{2b}^*	16 μ m/0.3 μ m		N_{W1}, N_{W2}	64 μ m/2 μ m
	N_{1a}^*, N_{1b}^*	8 μ m/1 μ m		N_{W3}	32 μ m/2 μ m
	N_{2a}^*, N_{2b}^*	2 μ m/1 μ m		P_{W3}, P_{W5}	16 μ m/0.4 μ m
	N_{3a}, N_{3b}	20 μ m/0.6 μ m		P_{W4}, P_{W6}	128 μ m/0.4 μ m
Summing stage and buffer stage in Fig. 1 (14 μ A)	P_3	16 μ m/1 μ m		P_{X1c}, P_{X1d}	8 μ m/0.4 μ m
	P_4^*	0.5 μ m/0.3 μ m		N_X	24 μ m/0.06 μ m
	N_4^*	0.5 μ m/0.3 μ m		N_{X1a}	16 μ m/2 μ m
	N_5^*	2 μ m/1 μ m		N_R	0.6 μ m/0.6 μ m
	N_6^*	0.5 μ m/0.3 μ m		P_{X1a}^*, P_{X1b}^*	5 μ m/1 μ m
	N_7	1.2 μ m/0.6 μ m		P_{X2a}^*, P_{X2b}^*	8 μ m/0.4 μ m
	N_8	0.4 μ m/0.1 μ m		N_{X1b}^*	4.8 μ m/0.6 μ m
	N_P	3000 μ m/0.06 μ m		N_{X2a}^*, N_{X2b}^*	24 μ m/0.3 μ m
Compensation capacitors	C_C	2.5pF		N_{X3a}^*, N_{X3b}^*	8 μ m/0.4 μ m
	C_{CX}	0.1pF		R_{X1}, R_{X2}	100k Ω
Resistors					

* thick gate oxide I/O transistor.

a wide frequency range under heavy-load conditions. On the other hand, under light-load conditions, the PSRR is intrinsically high in high frequencies (see (6) and Fig. 7). In view of this, the ensuing primary design consideration is to improve the PSRR in the low frequencies whilst minimizing the power dissipation due to the adaptive AUX. The dynamic-biasing feature leads to a low current consumption of the adaptive AUX at light-load condition; 20% of the total quiescent current of the LDO. Table I tabulates the size of the transistors, resistors, and capacitors depicted in Figs. 1 and 4 and the current consumption of each block of the LDO; the biasing circuit consumes 8 μ A.

Fig. 5 depicts the optimal $A_x (=1/A_{int_p})$ derived from (2) and the simulated A_x of the adaptive AUX versus I_{load} ranging from 100 μ A to 100 mA. The PSRR improvement due to the adaptive AUX is also illustrated and is compared with the case when A_x is otherwise a fixed value. It can be observed from Fig. 5 that A_x closely tracks $1/A_{int_p}$ with the discrepancy of <1 dB (i.e., $\sim \times 1.1$) when $1/A_{int_p}$ experiences substantial variation of 3.7 dB (i.e., $\sim \times 1.5$) over large load

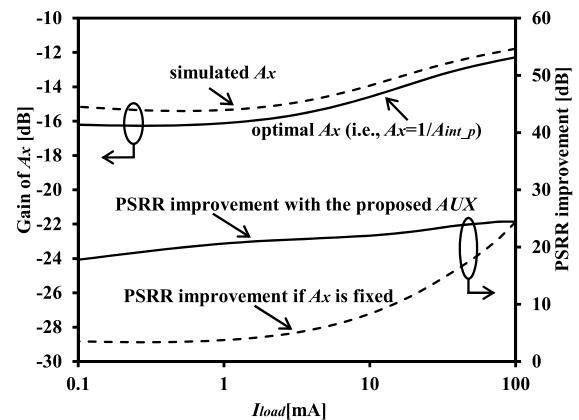


Fig. 5. Simulated A_x and the optimal A_x , and PSRR improvement for fixed A_x and for the adaptive AUX.

current variations (100 μ A–100 mA). Because of the adaptive A_x , the adaptive AUX substantially improves the PSRR by between 18–24 dB over the 100 μ A to 100 mA load current

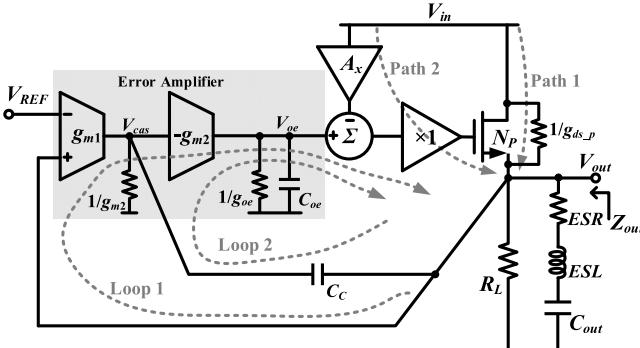


Fig. 6. Small signal model of the LDO for PSRR analysis.

range; worst case is 18 dB at $I_{\text{load}} = 100 \mu\text{A}$. By comparison, when A_x is a fixed value and optimized for 100-mA load current, the degree of PSRR improvement decreases substantially—to 4 dB at $I_{\text{load}} = 100 \mu\text{A}$.

Consider now the analytical model of the LDO depicted in Fig. 6 for modeling PSRR. As aforementioned, arising from the adaptive AUX, there are two feedforward paths, Path 1 and Path 2. Due to C_C , there are two signal loops, Loop 1 and Loop 2. On the basis of (1) and (2), the PSRR of the LDO can be derived as

$$\text{PSRR}_v = \frac{A_F(S)}{1 - L(s)} = \frac{g_{\text{dsp}}Z_{\text{out}}(1 - A_x A_{\text{int_p}})}{1 + \frac{g_{\text{mp}}Z_{\text{out}}A_{\text{oe}}(1 + s\frac{C_C}{g_{\text{m1}}})}{(1 + s\frac{C_{\text{oee}}}{g_{\text{oe}}})(1 + s\frac{C_C}{g_{\text{m2}}})}} \quad (4)$$

where

$A_{\text{oe}} = g_{\text{m1}}/g_{\text{oe}}$	dc gain of the EA;
g_{m1}	transconductance of differential input pair (i.e., N_{1a} and N_{1b} in Fig. 1);
g_{oe}	equivalent output conductance at the output of the error amplifier V_{oe} ;
C_{oe}	capacitance associated with node V_{oe} ;
g_{m2}	transconductance of P_{2a} in Fig. 1.

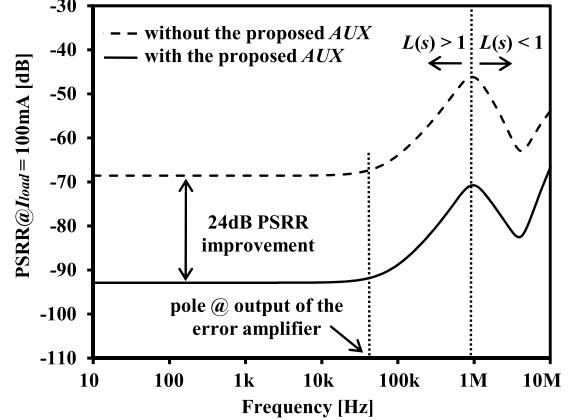
It is worthy to note that as $L(s)$ decreases as frequency increases, (4) can be decomposed into two parts with respect to frequency by comparing $L(s)$ with 1 (unity). The PSRR of the LDO for the case of $L(s) > 1$ and $L(s) < 1$ can be respectively expressed as

$$\text{PSRR}|_{L(s)>1} = \frac{1}{A_{\text{oe}}A_{\text{int_p}}}\left(1 - A_x A_{\text{int_p}}\right)\left(1 + s\frac{C_{\text{oe}}}{g_{\text{oe}}}\right) \quad (5)$$

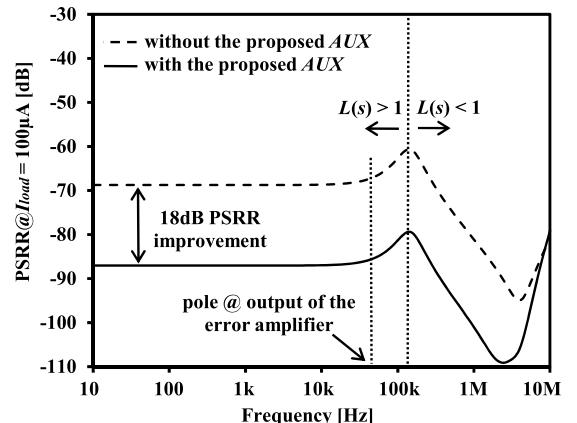
$$\text{PSRR}|_{L(s)<1} = g_{\text{dsp}}Z_{\text{out}}\left(1 - A_x A_{\text{int_p}}\right). \quad (6)$$

Note that (5) is a simplified expression without considering the terms of $(1 + sC_C/g_{\text{m1}})$ and $(1 + sC_C/g_{\text{m2}})$ in (4). This is because at low frequency where $L(s) > 1$, $(1 + sC_C/g_{\text{m1}}) \approx 1$, and $(1 + sC_C/g_{\text{m2}}) \approx 1$ in the LDO.

From (5) and (6), the PSRR characteristics of the LDO can be summarized by the following three salient points. First, the adaptive AUX enhances the PSRR by introducing the term $(1 - A_x A_{\text{int_p}})$ into (5) and (6). Second, the PSRR degrades from frequencies beyond $f = g_{\text{oe}}/2\pi C_{\text{oe}}$ due to the pole at the output of the EA. Third, the PSRR conversely improves at high frequencies when $L(s) < 1$ because the PSRR is



(a)



(b)

Fig. 7. Simulated PSRR of the LDO with and without the adaptive AUX for (a) $I_{\text{load}} = 100 \text{ mA}$ and (b) $I_{\text{load}} = 100 \mu\text{A}$.

largely unaffected by $L(s)$ when $L(s) < 1$, and because of the capacitive characteristic of Z_{out} which decreases with frequency.

Fig. 7 depicts the simulated PSRR of the LDO with and without the adaptive AUX, and under heavy-load ($I_{\text{load}} = 100 \text{ mA}$) and light-load ($I_{\text{load}} = 100 \mu\text{A}$) conditions. Note that in the case without the adaptive AUX, $V_{\text{in}} = 1.2 \text{ V}$ with ac noise is applied only to the power transistor, while $V_{\text{in}} = 1.2 \text{ V}$ without ac noise is applied to the adaptive AUX. In this fashion, the biasing conditions of the LDO are the same for both cases, thereby a fair comparison. The same setup is also applied for our hardware measurement. The simulations in Fig. 7 validate our aforementioned analysis and derivations from the following perspectives.

- In Fig. 7(a), when $I_{\text{load}} = 100 \text{ mA}$, the adaptive AUX significantly improves the PSRR throughout the 10 Hz–10 MHz frequency range—by more than 20 dB from 10 Hz to 4 MHz, and subsequently to 13 dB at 10 MHz.
- In Fig. 7(b), when $I_{\text{load}} = 100 \mu\text{A}$, the adaptive AUX similarly significantly improves the PSRR but in a narrower frequency range—by ~18 dB from 10 Hz to 4 MHz, and decreases to 0 dB for frequencies beyond 7 MHz. This is not unexpected because as

- delineated earlier, the adaptive AUX is dynamically biased where its bandwidth is limited when I_{load} is low.
- 3) In the high-frequency range, the PSRR is intrinsically higher when $I_{\text{load}} = 100 \mu\text{A}$ than $I_{\text{load}} = 100 \text{ mA}$. This is because, at high frequencies, the PSRR is ascertained by g_{dsp} [see (6)], which decreases as the load current decreases. In other words, the 0-dB improvement beyond 7 MHz in item 2) is not disadvantageous because the PSRR is already very high.
 - 4) The PSRR for both $I_{\text{load}} = 100 \text{ mA}$ and $I_{\text{load}} = 100 \mu\text{A}$ expectedly degrades at the pole frequency of the EA output ($\sim 60 \text{ kHz}$). This observation is congruous to our derivation in (5).
 - 5) The PSRR improves when $L(s) < 1$, whose corresponding frequency is $\sim 100 \text{ kHz}$ and $\sim 1 \text{ MHz}$ for $I_{\text{load}} = 100 \mu\text{A}$ and $I_{\text{load}} = 100 \text{ mA}$, respectively. This frequency increases with load current because it is ascertained by g_{mp} [see (4)].
 - 6) Finally, in the PSRR plots, a trough is observed for both load current conditions. This phenomenon is because Z_{out} reaches its minimum value at $\sim 3 \text{ MHz}$ due to the ESR ($10 \text{ m}\Omega$) and ESL (0.5 nH) associated with the $4.7 \mu\text{F}$ C_{out} .

In addition to the load current variations, the LDO is similarly expected to feature high PSRR over PVT variations. This is likewise obtained by means of the gain-tracking feature of the adaptive AUX. The PSRR of the LDO is simulated under 20 PVT corners [five process corners \times two temperature corners (0°C and 80°C) \times two V_{bat} corners (2.4 and 3.2 V)]. Fig. 8 (a) and (b) depicts the simulated PSRR when $I_{\text{load}} = 100 \text{ mA}$ and $I_{\text{load}} = 100 \mu\text{A}$, respectively, and for the cases with and without the adaptive AUX. As expected, the effectiveness of the adaptive AUX is robust against PVT variations, where the adaptive AUX offers a PSRR improvement of 23–24 dB and 15–26 dB when $I_{\text{load}} = 100 \text{ mA}$ and $I_{\text{load}} = 100 \mu\text{A}$ (to 2 MHz), respectively.

In practice, it is also important to ascertain the effect of transistor mismatch on the performance of the LDO. This is because transistor mismatch causes the mismatch between the current density of N_x and N_P (see Fig. 3), thereby degrading the effectiveness of the adaptive AUX. To ascertain this, a 200-run Monte Carlo simulation on PSRR is carried out under the worst case PVT corner and at the worst case frequency for both $I_{\text{load}} = 100 \text{ mA}$ and $I_{\text{load}} = 100 \mu\text{A}$; on the basis of our corner simulations in Fig. 8, the worst case PVT corner for both $I_{\text{load}} = 100 \text{ mA}$ and $I_{\text{load}} = 100 \mu\text{A}$ is when process corner = SS, $V_{\text{bat}} = 2.4 \text{ V}$ and temperature = 80°C , and the worst case frequency are 1 MHz and 100 kHz, respectively.

Fig. 9 (a) and (b) depicts the statistics of the 200-run Monte Carlo for $I_{\text{load}} = 100 \text{ mA}$ and $I_{\text{load}} = 100 \mu\text{A}$, respectively. When $I_{\text{load}} = 100 \text{ mA}$, the PSRR at 1 MHz is a high mean value of 71 with 7 dB standard deviation. When $I_{\text{load}} = 100 \mu\text{A}$, the PSRR at 100 kHz is a high mean value of 80 dB with a smaller standard deviation of 3 dB. Put simply, the effectiveness of the adaptive AUX to improve the PSRR remains high despite transistor mismatches. Of particular interest, under the same PVT corner, the PSRR

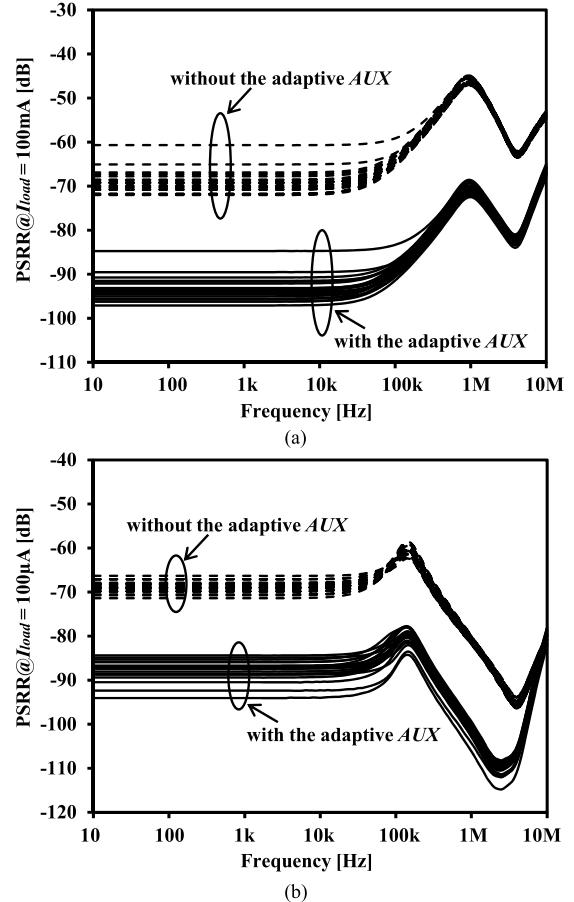


Fig. 8. PVT corner simulation results of the LDO for (a) $I_{\text{load}} = 100 \text{ mA}$ and (b) $I_{\text{load}} = 100 \mu\text{A}$.

without the adaptive AUX is a low $\sim 46 \text{ dB}$ at 1 MHz when $I_{\text{load}} = 100 \text{ mA}$ and a relatively low $\sim 64 \text{ dB}$ at 100 kHz when $I_{\text{load}} = 100 \mu\text{A}$. Also, the PSRR spread for $I_{\text{load}} = 100 \text{ mA}$ is larger than that for $I_{\text{load}} = 100 \mu\text{A}$, because the gain of N_x (and N_P) is more sensitive to current density variations (arising from transistor mismatches) when I_{load} is relatively large (see Fig. 5).

B. Stability

Consider now the stability, an imperative practical consideration. The stability of the LDO will be discussed by considering the simulated loop gain (and phase) of the adaptive AUX and the main control loop in turn.

The adaptive AUX (Fig. 4) comprises a two-stage amplifier and a resistive feedback network. The Ahuja frequency compensation [25] is adopted here to stabilize the signal loop with a frequency compensation capacitor, C_{CX} . Fig. 10 depicts the simulated loop gain of the adaptive AUX for $I_{\text{load}} = 100 \mu\text{A}$ and $I_{\text{load}} = 100 \text{ mA}$, where it can be seen that the adaptive AUX is stable for both cases. Specifically, when $I_{\text{load}} = 100 \mu\text{A}$, the unity gain bandwidth, and the phase margin (PM) are 6 MHz and 86° , respectively. When $I_{\text{load}} = 100 \text{ mA}$, the unity gain bandwidth is $\sim 5\times$ higher (30 MHz) because the adaptive AUX is dynamically biased, and the PM is 77° .

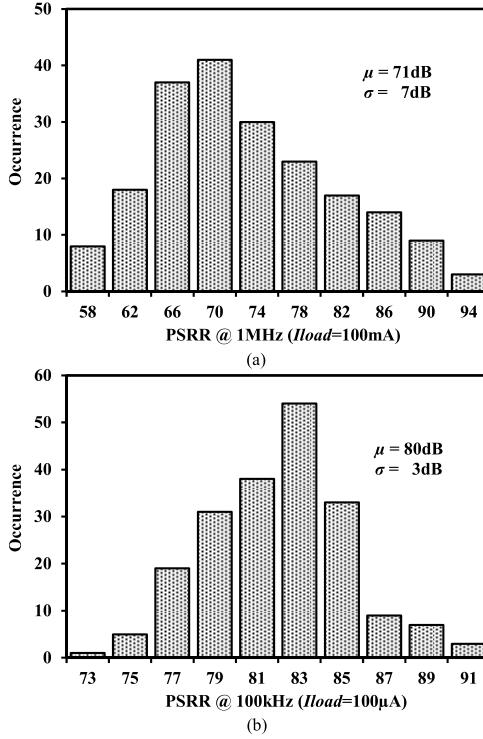


Fig. 9. Monte Carlo simulations of PSRR for 200 samples of the LDO (a) when $I_{\text{load}} = 100 \text{ mA}$ and frequency = 1 MHz and (b) when $I_{\text{load}} = 100 \mu\text{A}$ and frequency = 100 kHz.

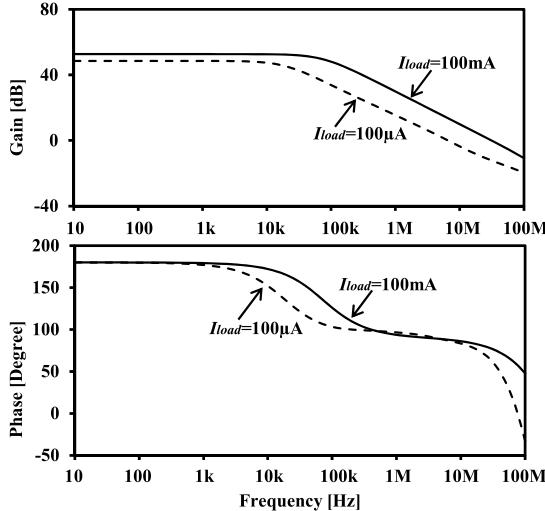


Fig. 10. Loop gain of the adaptive AUX for $I_{\text{load}} = 100 \mu\text{A}$ and 100 mA.

Consider now the main loop of the LDO which is stabilized using a reported frequency compensation [26]. Specifically, a wideband buffer is employed to drive the power transistor, thereby pushing the pole at the power transistor gate to high frequency. A frequency compensation capacitor C_C is employed to create an inner feedback loop, under the heavy-load condition, to split the pole at the output of the EA and the pole at the LDO output. Note that under the light-load condition, the inner feedback loop is inactive. Under this condition, as the LDO output pole is located at a very low frequency,

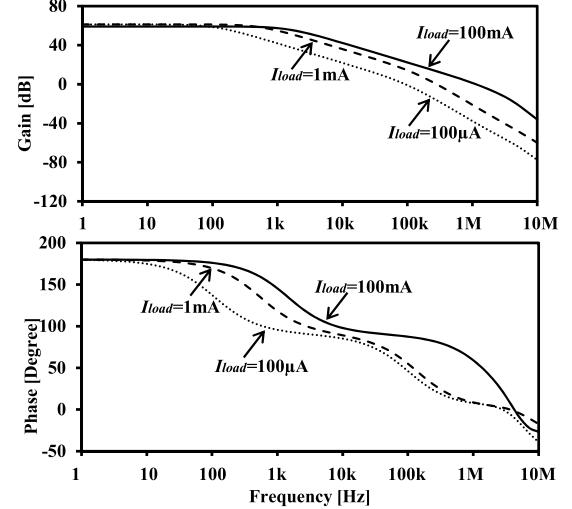


Fig. 11. Loop gain of the main control loop for $I_{\text{load}} = 100 \mu\text{A}$, 1 mA, and 100 mA.

the LDO is hence inherently stable. For completeness, a brief pole-zero analysis under different load conditions is presented in the Appendix.

Fig. 11 depicts the simulated loop gain of the main control loop $T(s)$ under different I_{load} ranging from 100 μA to 100 mA. From the plots, the PM for the cases when $I_{\text{load}} = 100 \text{ mA}$, $I_{\text{load}} = 1 \text{ mA}$, and $I_{\text{load}} = 100 \mu\text{A}$ are 60°, 30°, and 50°, respectively. These simulations are largely congruous with [26], where the worst case PM ($\sim 30^\circ$) occurs at medium load condition.

In summary, both the adaptive AUX and the main control loop are stable under various load conditions.

C. Dropout Voltage

The reduced dropout voltage deteriorates the static output accuracy of the LDO because the low dropout voltage may push the power transistor into the triode region. This, in turn, degrades the power stage gain and hence the dc loop gain. Subjected to this constraint, the minimum dropout voltage of state-of-the-art LDOs, particularly for those adopting PMOS power transistor, is often large ~ 200 mV.

The NMOS LDO accommodates a lower dropout voltage by adopting the NMOS power transistor. With the NMOS power transistor, the power stage (see Fig. 1) is realized as a common-drain configuration. The dc gain of the power stage A_{POW} can be expressed as

$$A_{\text{POW}} = \frac{g_{\text{mp}}}{g_{\text{mp}} + g_{\text{dsp}}} = \frac{1}{1 + 1/A_{\text{int_p}}}. \quad (7)$$

From (7), it can be seen that as long as $A_{\text{int_p}} \gg 1$, A_{POW} is largely insensitive to $A_{\text{int_p}}$. Consequently, A_{POW} and the dc loop gain of the LDO experience less degradation. This remains true even though $A_{\text{int_p}}$ suffers substantial reduction when the power transistor enters into the triode region due to low dropout voltage. Put simply, the LDO can achieve a low dropout voltage without compromising its static output accuracy.

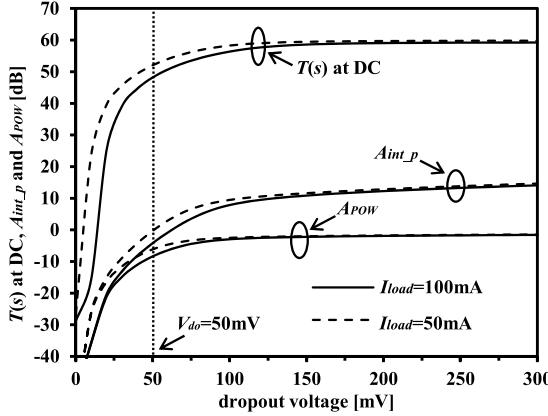


Fig. 12. Simulated $T(s)$ at dc, $A_{\text{int_}p}$, and A_{POW} versus dropout voltage at $I_{\text{load}} = 50$ mA and 100 mA.

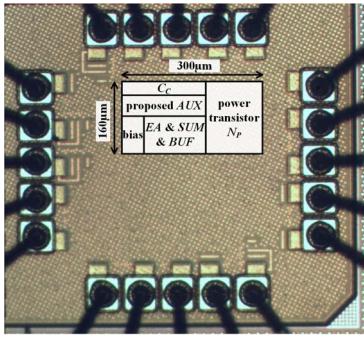


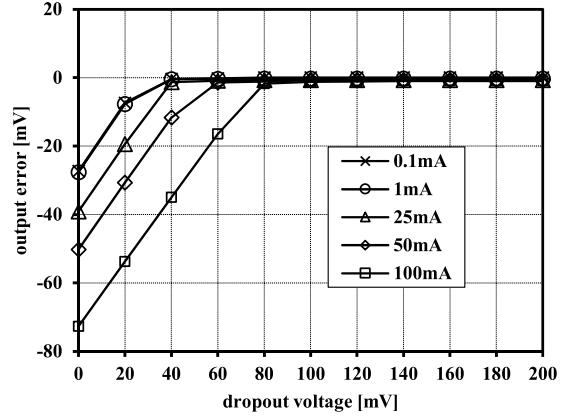
Fig. 13. Microphotograph of the LDO.

To verify this, we plot in Fig. 12 the simulated $T(s)$ at dc (i.e., the dc loop gain), A_{POW} , and $A_{\text{int_}p}$ versus dropout voltage V_{do} of the LDO at $I_{\text{load}} = 100$ mA and $I_{\text{load}} = 50$ mA. It can be seen that A_{POW} and the $T(s)$ at dc decrease by only 5 and 7 dB, respectively, despite $A_{\text{int_}p}$ suffering a substantial reduction of 18 dB under the condition of $V_{\text{do}} = 50$ mV and $I_{\text{load}} = 50$ mA. For completeness, to achieve $<\pm 0.1\%$ static output error, $T(s)$ at dc would need to be greater than 54 dB, which is the case here. On this basis, the minimum dropout voltage of the LDO is ~ 50 and ~ 80 mV when the $I_{\text{load}} = 50$ mA and $I_{\text{load}} = 100$ mA, respectively.

III. MEASUREMENT RESULTS

Fig. 13 depicts the microphotograph of the LDO fabricated in 65-nm bulk CMOS process. The active area of the LDO is ~ 0.05 mm², and the LDO requires an off-chip C_{out} of 4.7 μ F. To mitigate potential issues arising from the parasitic resistance and inductance of the bonding wires, the Kelvin connection [11] is adopted. The nominal voltage of V_{bat} , V_{in} , V_{out} , and V_{REFX} (see Fig. 3) of the LDO are 2.5, 1.2, 1, and 0.7 V, respectively. The quiescent current of the LDO is ~ 40 μ A.

The static characteristics, line regulation, minimum dropout voltage, and load regulation of the LDO are depicted in Fig. 14. Fig. 14(a) depicts the measured static output error ($V_{o,e} = V_{\text{out}} - V_{\text{REF}}$) versus dropout voltage ($V_{\text{do}} = V_{\text{in}} - V_{\text{out}}$) for different load current conditions ($I_{\text{load}} = 0.1, 1, 25, 50$,



(a)

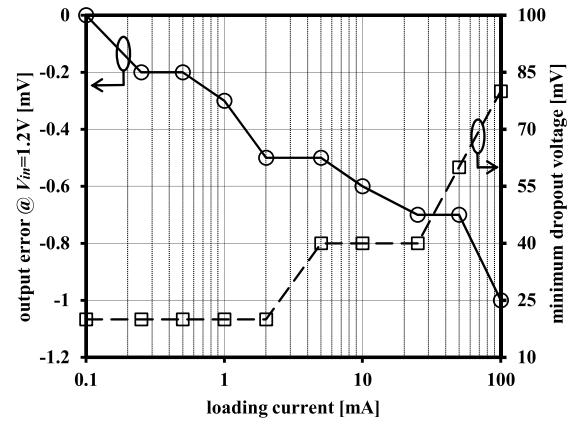


Fig. 14. (a) Measured static output error versus dropout voltage under different I_{load} . (b) Measured V_{out} versus I_{load} when $V_{\text{in}} = 1.2$ V

and 100 mA). The line regulation of the LDO is 8.75 mV/V when the load current is 100 mA. We attribute the excellent line regulation to the high PSRR (~ 90 dB of the LDO) at dc, arising from the adaptive AUX. The minimum dropout voltage with <2 -mV output error is a low 80 mV when $I_{\text{load}} = 100$ mA. As expected, the minimum dropout voltage reduces with lower I_{load} and is a low 60 and 40 mV when $I_{\text{load}} = 50$ and 25 mA, respectively. This low dropout voltage is attributed to the adoption of the NMOS power transistor embodied in the LDO.

Fig. 14(b) depicts the output error versus load current under the nominal condition where $V_{\text{in}} = 1.2$ V. The load regulation of the LDO is 10 μ V/mA. The excellent load regulation is a consequence of a small closed-loop output resistance [22], arising from the low output resistance of NMOS power transistor and from sufficient loop gain.

Fig. 15(a) depicts the load transient response of the LDO measured at $V_{\text{in}} = 1.2$ V for 100 μ A–100 mA I_{load} variations with 1- μ s rising and falling time. Fig. 15(b) depicts the detailed waveform (scaled in time) near the rising edge of I_{load} in the bottom trace in Fig. 15(a). When I_{load} falls from 100 mA to 100 μ A, the overshoot voltage and the settling time are 2 mV and 20 μ s, respectively. On the other hand, when I_{load} rises from 100 μ A to 100 mA, the undershoot voltage and

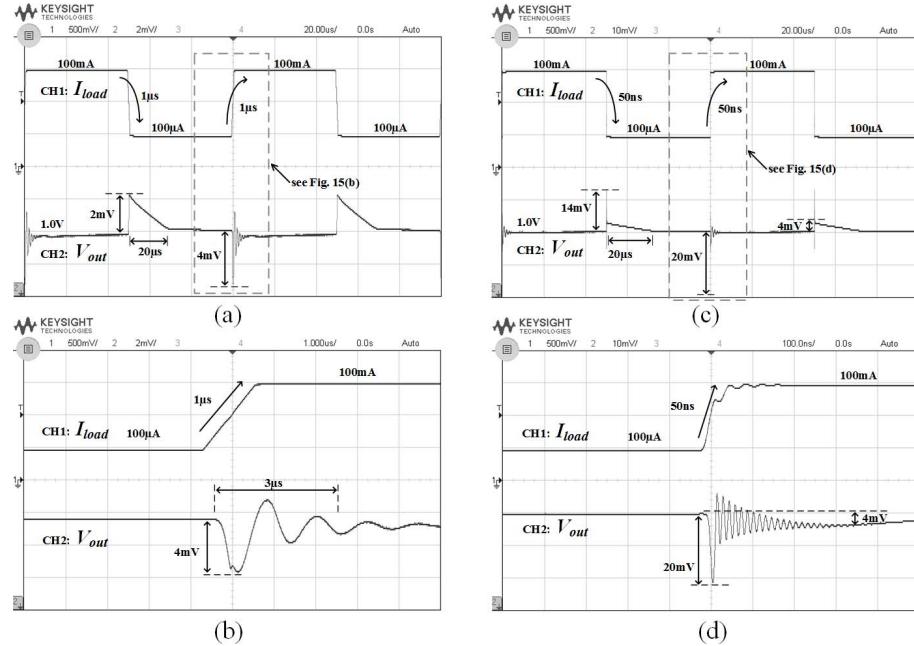


Fig. 15. (a) Measured V_{out} under 100-mA load transient with 1- μ s rising and falling time. (b) 1- μ s rising edge of the load transient. (c) Measured V_{out} under 100-mA load transient with 50-ns rising and falling time. (d) 50-ns rising edge of the load transient.

TABLE II
BENCHMARKING THE LDO AGAINST REPORTED LDOs

	This work	[11]	[15]	[16]	[17]
Technology (CMOS)	65nm	0.13 μ m	65nm	0.18 μ m	0.18 μ m
Power transistor	NMOS	PMOS	PMOS	PMOS	PMOS
Maximum I_{load}	100mA	25mA	25mA	100mA	100mA
Nominal V_{in}	1.2V*	1.2V	1.2V	1.8V	1.8V
V_{out}	1.0V	1.0V	1.0V	1.6V	1.6V
Minimum dropout	80mV	150mV	150mV	200mV	200mV
C_{out}	4.7μF	4 μ F	4.7 μ F	capless	capless
Load regulation	10μV/mA	48 μ V/mA	40 μ V/mA	140 μ V/mA	N.A.
Quiescent current	40μA	50 μ A	150 μ A	55 μ A	71 μ A
Overshoot/Undershoot	2mV/4mV	15mV/10mV	12mV/12mV	120mV/80mV	100mV/110mV
PSRR @ heavy-load	Heavy I_{load} 100mA	25mA	25mA	50mA	50mA
	100kHz 89dB	62dB	61dB	61dB	50dB
	1MHz 70dB	67dB	61dB	72dB	76dB
	10MHz 62dB	50dB	47dB	37dB	0dB
PSRR @ light-load	Light I_{load} 100μA	1mA	1mA	1mA	N.A.
	100kHz 81dB	67dB	61dB	50dB	
	1MHz 95dB	80dB	63dB	65dB	
	10MHz 75dB	59dB	55dB	42dB	
Area	0.048mm²	0.049mm ²	0.14mm ²	0.018mm ²	0.033mm ²

*The load regulation, transient response, and PSRR are measured with the nominal $V_{in}=1.2V$ in this work.

the settling time are 4 mV and 3 μ s, respectively. The small overshoot and undershoot voltages (<0.4% the output voltage) are largely attributed to the NMOS power transistor that offers a small output resistance of $\sim 1/g_{mp}$, and to the 4.7 μ F C_{out} . The 20- μ s overshoot settling time is longer than the 3- μ s undershoot settling time because the bandwidth of the regulation loop is narrower under light-load conditions than under heavy-load conditions (see Fig. 11). Fig. 15(c) depicts the load transient response of the LDO for 100 μ A–100 mA

I_{load} variations with 50-ns rising and falling times. Fig. 15(d) depicts the detailed waveform (scaled in time) near the rising-edge of I_{load} in the bottom trace in Fig. 15(c). The transient response depicted in Fig. 15(c) and (d) is largely the same as those in Fig. 15(a) and (b) in terms of overshoot (~4 mV), undershoot (~4 mV), and their settling time (20 and 3 μ s, respectively). However, 20- and 14-mV spikes are observed at the rising edge and the falling edge, respectively. The duration of the spikes is ~30 ns, which is largely the same as the 50-ns

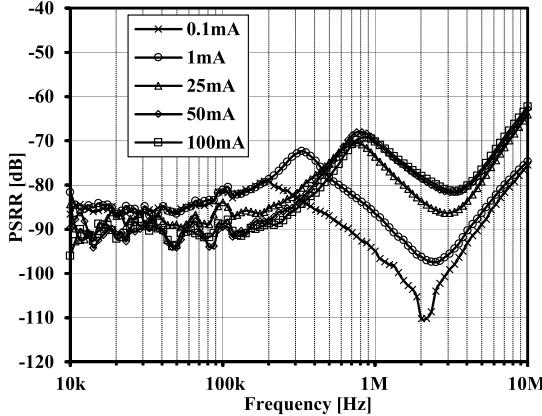


Fig. 16. Measured PSRR for I_{load} ranging from $100 \mu\text{A}$ to 100 mA .

rising and falling time. This voltage spike is expected in view of the presence of the ESL of C_{out} [27].

Fig. 16 depicts the measured PSRR of the LDO under various load current conditions, $I_{\text{load}} = 100 \mu\text{A}, 1, 25, 50$, and 100 mA . The PSRR of the LDO is measured with the Agilent E5061B network analyzer and the Picotest J2120A line injector. A noise with -20-dBm noise power (equivalent to 60-mV peak-to-peak voltage ripple) is applied to $V_{\text{in}} = 1.2 \text{ V}$, while V_{bat} is powered by a constant 2.5 V . The PSRR exceeds 80 dB in the relatively low-frequency range from 10 to 100 kHz and under all load current conditions. In the higher frequency range from 100 kHz to 10 MHz , $>60\text{-dB}$ PSRR is achieved for all load current conditions. In the high-frequency range, the PSRR expectedly worsens when the frequency exceeds the resonant frequency of C_{out} , $\sim 3 \text{ MHz}$, because the ESL of the capacitor dominates at frequencies beyond 3 MHz . C_{out} utilized in the LDO is the TDK CLL series capacitor.

Fig. 17 (a) and (b) compares the measured PSRR with and without the adaptive AUX for $I_{\text{load}} = 100 \text{ mA}$ and $I_{\text{load}} = 100 \mu\text{A}$, respectively. In the low-to-mid frequency range (10 kHz – 1 MHz), the adaptive AUX improves (over the case without the adaptive AUX) the PSRR by 25 and 16 dB when $I_{\text{load}} = 100 \text{ mA}$ and $I_{\text{load}} = 100 \mu\text{A}$, respectively. We attribute the substantial PSRR improvement observed over the wide I_{load} range to the adaptive AUX adaptively optimizing its gain despite the load current variations. In the mid-to-high frequency range (1 – 10 MHz), the PSRR improvement, when $I_{\text{load}} = 100 \text{ mA}$, is 23 dB at 1 MHz , and it is 7 dB at 10 MHz . For the case of $I_{\text{load}} = 100 \mu\text{A}$, there is no PSRR improvement beyond 4 MHz , because the bandwidth of the adaptive AUX is narrower when I_{load} is relatively small. This is of little consequence because the PSRR, in this case, is already high. In short, the PSRR improvement due to the adaptive AUX is very worthwhile.

Fig. 18 depicts the measured output noise of the LDO when $I_{\text{load}} = 100 \text{ mA}$ and $V_{\text{in}} = 1.2 \text{ V}$, measured with the R&S FSUP signal source analyzer. The output noise density at 10 Hz and 1 kHz are $2 \mu\text{V}/\sqrt{\text{Hz}}^{1/2}$ and $65 \text{nV}/\sqrt{\text{Hz}}^{1/2}$, respectively. The thermal noise dominates at frequencies beyond 1 kHz where the noise density is $40 \text{nV}/\sqrt{\text{Hz}}^{1/2}$. The primary noise contributor in LDOs is the voltage reference noise [28],

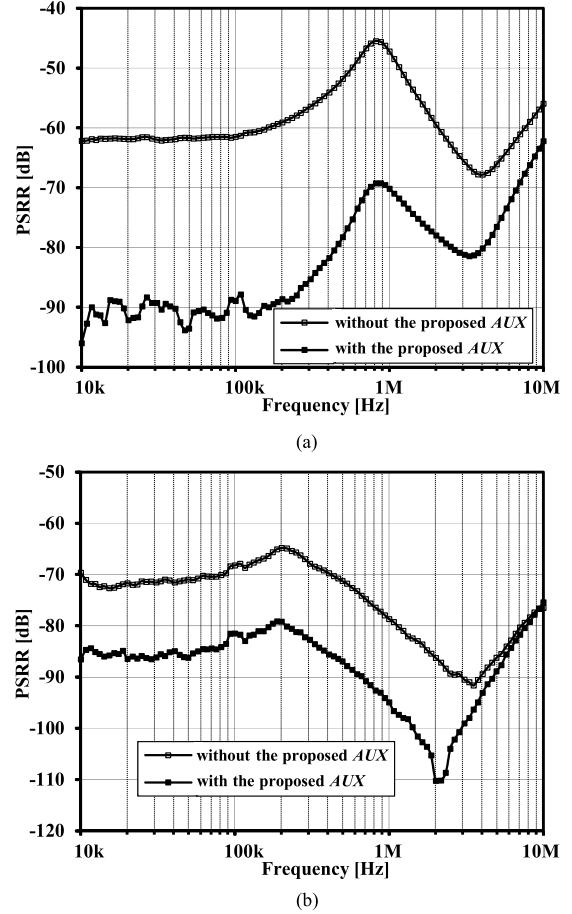


Fig. 17. Measured PSRR with and without the adaptive AUX when (a) $I_{\text{load}} = 100 \text{ mA}$ and (b) $I_{\text{load}} = 100 \mu\text{A}$.

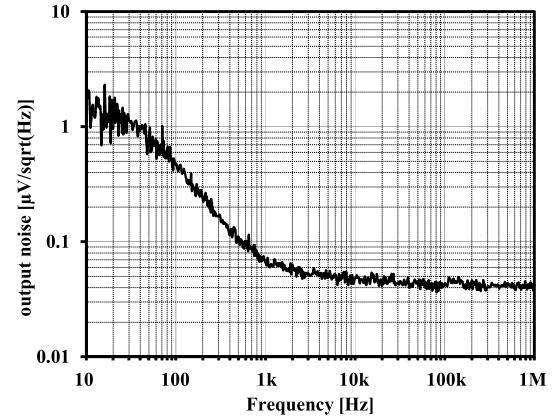


Fig. 18. Measured output noise of the LDO.

and a lower LDO output noise can be obtained with a lower noise voltage reference [6], [29]. In this LDO, the reference voltage is externally generated.

Table II benchmarks the LDO against state-of-the-art high-PSRR LDOs; PSRR is benchmarked at 100 kHz , 1 MHz , and 10 MHz in accordance to the switching frequency of switching regulator. The LDO features the highest PSRR over all state-of-the-art LDOs in Table I, save at 1 MHz where the LDOs [16], [17] reported slightly higher PSRR (only at

the 1 MHz point) but at lower heavy I_{load} (50 mA versus 100 mA in this LDO). Of particular interest, the LDO is the only design that achieves >60-dB PSRR throughout the 10-MHz frequency range and for 100-mA load current range. In contrast, the PSRR of state-of-the-art LDOs are high only over a limited load current range (<50 mA) and/or limited frequency range. The highest load current (100 mA) of the LDO is more than 2 \times larger and the lowest load current (100 μ A) is an order of magnitude lower than the reported designs [11], [15]–[17]. Put simply, the LDO features the highest PSRR for three orders of magnitude change in the load current (100 μ A–100 mA) while the reported competing LDOs suffer lower PSRR despite having a substantially lower load current range of less than two orders of magnitude.

The LDO employs an NMOS as the power transistor instead of PMOS; several other LDOs [18]–[21] employ the same. By this means, the LDO features the lowest dropout voltage, the best load regulation, and the smallest overshoot and undershoot. The smallest overshoot and undershoot attribute also obtained in part from the 4.7- μ F output capacitor. As expected, the overshoot and undershoot of capless LDOs (i.e., LDOs do not utilize output capacitor) [16], [17] are $\sim 10\times$ larger than LDOs with output capacitor [11], [15]. The active area of the LDO is one of the largest; the power transistor occupies a significant area for the sake of providing 100-mA maximum load current, and the adaptive AUX incurs area as well. For completeness, the quiescent current of the LDO is comparable with other designs.

IV. CONCLUSION

We have presented the design of a 65-nm CMOS LDO embodying an adaptive FFRC technique with an adaptive load current tracking scheme. The LDO features very high PSRR over a wide frequency range and large load current range, low dropout voltage, and small overshoot and undershoot.

APPENDIX

The stability of the main control loop of the LDO is succinctly delineated in this appendix.

Fig. 19 depicts the small signal model of the main control loop, and Table III tabulates the pole-zero position of the main control loop under different load conditions, with and without C_C . C_C introduces an inner frequency compensation loop, a pole (p_3), and a zero (z_1).

Under the heavy-load condition, the inner loop splits p_1 and p_2 to address the increased pole frequency of p_1 due to the large load current. The pole splitting effect relies on the loop gain of the inner frequency compensation loop, $T_{\text{inner}}(s)$ —this is the Miller compensation. Note that an oversized C_C results in a complex pole pair because the inner loop also shifts p_3 to a lower frequency. In our LDO, the optimal value of C_C is ~ 2.5 pF to achieve a good stability and to avoid the complex pole pair.

Under the light-load condition, the main control loop is inherently stable even without C_C . This is because p_1 and p_2 are widely separated. Note that the inner loop barely affects p_1 and p_2 under the light load for the following reason.

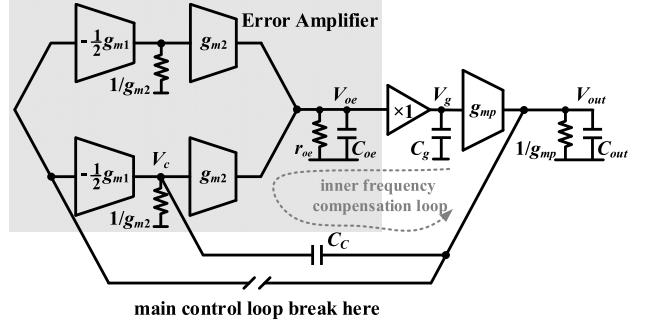


Fig. 19. Small signal model for stability analysis.

TABLE III
POLE-ZERO POSITION OF THE MAIN CONTROL LOOP WITH AND WITHOUT C_C UNDER LIGHT LOAD AND HEAVY LOAD

	Light-load	Heavy-load
Without C_C	p_1 low freq. $\xrightarrow{p_2}$ high freq.	unstable $\xrightarrow{p_1 p_2}$ high freq.
With C_C	p_1 low freq. $\xrightarrow{p_2}$ $\xrightarrow{p_3 z_1}$ high freq.	p_1' low freq. $\xrightarrow{p_2' p_3' z_1}$ high freq.

p_1 : pole at V_{out} ($\approx g_{\text{mp}}/2\pi C_{\text{out}}$), p_2 : pole at V_{oe} ($\approx 1/2\pi r_{\text{oe}}C_{\text{out}}$),
 p_3 : pole at V_C ($\approx g_{\text{m}2}/2\pi C_C$), z_1 : zero introduced by C_C , ($\approx 2g_{\text{m}2}/2\pi C_C$),
 p_1' : modulated p_1 by C_C , p_2' : modulated p_2 by C_C , p_3' : modulated p_3 by C_C .

From Fig. 19, $T_{\text{inner}}(s)$ can be expressed as

$$T_{\text{inner}}(s) = \frac{g_{\text{mp}}g_{\text{m}2}sC_C}{(g_{\text{mp}} + sC_{\text{out}})(1/r_{\text{oe}} + sC_{\text{oe}})(g_{\text{m}2} + sC_C)}. \quad (\text{A1})$$

On the basis of (A1), $T_{\text{inner}}(s)$ has a maximum value of $T_{\text{inner_max}} = C_C g_{\text{mp}} r_{\text{oe}} / C_{\text{out}}$ and this occurs within the frequency range of $g_{\text{mp}}/2\pi C_{\text{out}} < f < 1/2\pi r_{\text{oe}} C_{\text{oe}}$. Under the light load condition, $T_{\text{inner_max}}$ is less than 1 due to the small g_{mp} , and hence the inner frequency compensation loop is inactive.

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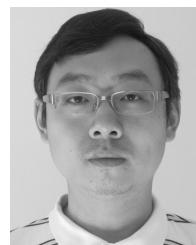
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