An 84.6-dB-SNDR and 98.2-dB-SFDR Residue-Integrated SAR ADC for Low-Power Sensor Applications

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***Abstract*— This paper presents an asynchronous-clocking successive approximation register (SAR) analog-to-digital converter (ADC) suitable for ultralow-power fine-precision sensor applications whose signal bandwidth is in the kilohertz range. The performance-limiting issues of comparator noise and capacitor mismatch in SAR ADC are resolved by a residue integration scheme combined with a dynamic element matching (DEM), achieving a high resolution without imposing extra burden on the design of residue amplifier and comparator. The prototype 16-bit 2 kS/s SAR ADC is fabricated using 180-nm CMOS process in an area of 0.68 mm^2. Measurements show 84.6-dB signal to noise and distortion ratio and 98.2-dB spurious-free dynamic range at the Nyquist input frequency. The ADC dissipates 7.93 μW from supply voltage of 1.8 V and achieves a Schreier figure of merit of 165.6 dB.**

***Index Terms*— Analog-to-digital converter (ADC), dynamic element matching (DEM), low-power sensor application, Nyquist-rate ADC, successive approximation register (SAR) ADC.**

I. Introduction

IMPLANTABLE sensor nodes have demanded low-power implementation of high-resolution analog-to-digital converters (ADCs) for acquiring bio-potential signals of a few-kilohertz bandwidth. Successive approximation register (SAR) ADC [1]–[4] has been the most popular architecture in sensor applications thanks to superior energy efficiency and robustness against process/voltage/temperature (PVT) variations. In high-resolution applications, however, comparator noise eventually limits the maximum achievable effective-number-of-bits (ENOBs).

To relieve the bottleneck from the comparator noise, residue amplification schemes [5]–[7] have been considered to achieve a finer resolution. However, the requirement of high-precision analog circuits for a large inter-stage gain also limits the maximum achievable ENOBs. Although there have been approaches with a smaller inter-stage gain [7], it requires increased sampling capacitance and also suffers from comparator noise when residue is insufficiently amplified.

As an alternative, noise-shaping delta–sigma modulators (DSMs) [8], [9] have been conventionally taken to implement high-resolution ADC. Large amount of input gathered through long accumulation time and the use of 1-bit quantizer greatly improve the ENOB. However, the need of high-frequency clock for oversampling and the digital post-processing for decimation filtering present significant burden in power consumption. Therefore, it has not been popular in ultralow-power sensor applications.

This paper presents a 2 kS/s 16-bit SAR ADC with a residue integration (RI) scheme which alleviates the design complexity of analog circuits. The proposed RI scheme is combined with a DSM loop. There have been hybrid architectures [10], [11] which combine SAR and DSM for noise shaping with oversampling principles. Though they achieved good energy efficiencies, the output eventually contains boosted noise at high frequency, hence requiring a post-processing by decimation filter. On the other hand, the DSM loop in the proposed ADC is mainly for confining the integrator output range for good linearity rather than for noise shaping as in the oversampling/noise-shaping (OS/NS) SAR ADCs. The proposed ADC is the Nyquist-rate converter with no need of decimation filtering.

The prototype ADC fabricated with 180-nm CMOS process shows 84.6-dB signal to noise and distortion ratio (SNDR) and 98.2-dB spurious-free dynamic range (SFDR) at the Nyquist-rate input frequency. Recursive use of a sub-SAR block with a smaller capacitance than that of conventional 16-bit SAR ADCs also helps the reduction of power consumption. The ADC consumes 3.97 nJ per conversion. Section II introduces the proposed architecture, and Section III describes circuit implementation. Section IV shows analyses to estimate the effects of imperfections. Section V summarizes the measurement results, and Section VI concludes this paper.

II. Architecture

A. Proposed Architecture

Fig. 1 briefly explains the concept of residue amplification. If the first-stage ADC generates n bit, required inter-stage gain is 2^n for applying a full-scaled input to the second stage. However, since practical amplifier has limited output

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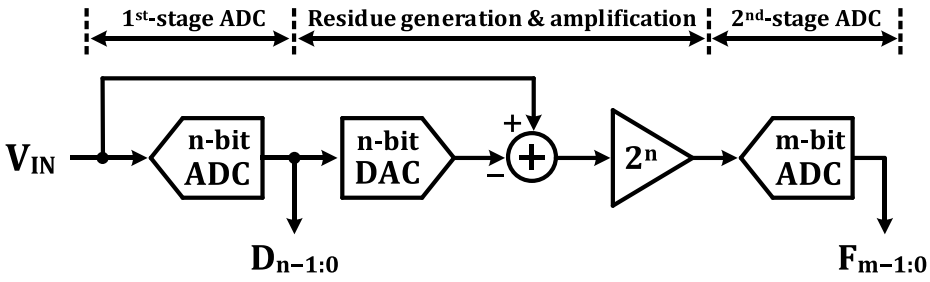

Fig. 1. Concept of residue amplification.

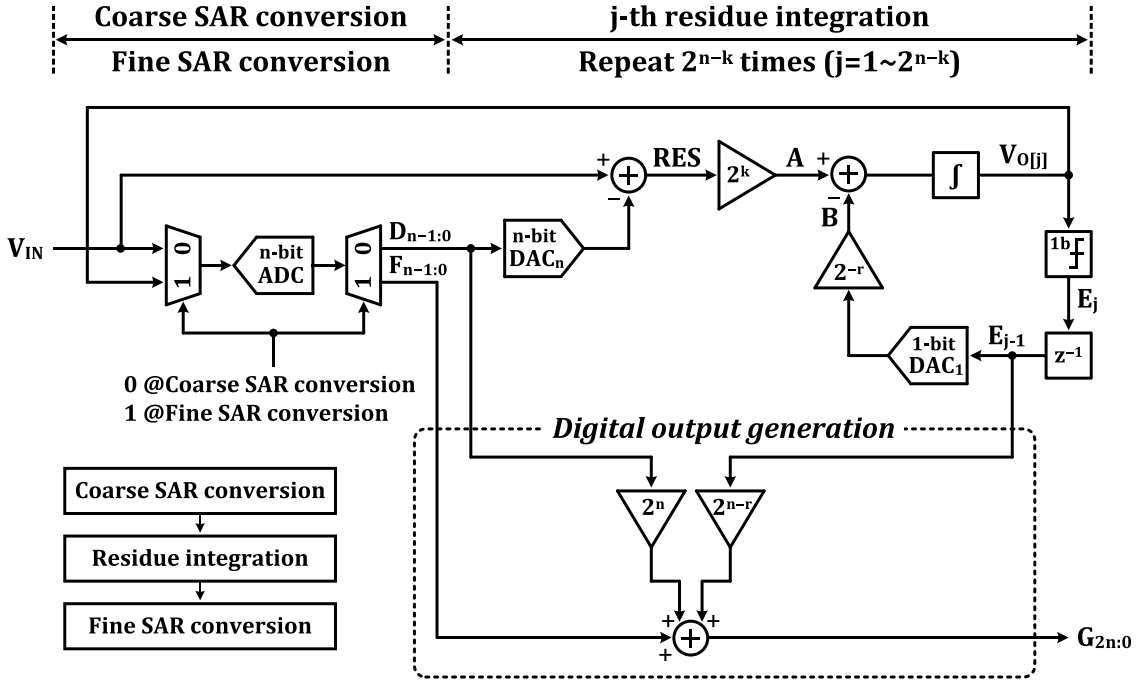

Fig. 2. Overall architecture of proposed SAR ADC.

voltage range (OVR), the open-loop gain becomes decreased as the output swing increases, resulting in linearity error in conversion characteristic. Though a smaller inter-stage gain [7] can be used to alleviate the non-linearity issue, it requires additional power consumption and area for generating extra reference voltages or performing extra decision procedure for the second-stage conversion. It eventually limits the maximum achievable resolution due to comparator noise.

The proposed SAR ADC consists of two functional blocks: 1) SAR conversion and 2) RI (Fig. 2). The first step is a coarse SAR conversion which performs a quick and dirty initial evaluation for n most-significant-bits (MSBs). The residue is then amplified by a small gain of 2^k which is much smaller than 2^n. The amplified residue is repeatedly accumulated 2^{n-k} times, performing a total inter-stage gain of 2^n. Therefore, this step integrates error induced by representing the input with the coarsely evaluated MSBs. During this repeated accumulation process, the integrator output can exceed the safe OVR boundaries. To effectively confine the amplifier output swing, the integrator is combined with a 1-bit quantizer, forming a DSM loop [8], [9]. This residue subtraction greatly relieves the requirements of the amplifier gain and improves linearity. The final step is performed by the same SAR block used in the coarse conversion to obtain digital codes corresponding to the remaining residue, generating n least-significant-bits (LSBs).

B. Residue Integration

Fig. 3 graphically illustrates how the integrator output changes during one conversion process. The initial residue (RES) after the completion of n-bit coarse SAR conversion is

$$\mathrm{RES} = V_{\mathrm{IN}} - \mathrm{DAC}_n[D_{n-1:0}] \tag{1}$$

where V_{IN} and DAC_n $[D_{n-1:0}]$, respectively, indicate the input and n-bit digital-to-analog converter (DAC) output (DAC_n) driven by the coarse MSB code ($D_{n-1:0}$). During the RI process, each residue amplification by 2^k (A) is followed by a subtraction with the DSM feedback. The subtraction is performed through a 1-bit DAC (DAC_1) which is represented by a gain of 2^{-r} (B). The subtraction result after the first cycle is

$$V_{O[1]} = 2^k \cdot \mathrm{RES} - 2^{-r} \cdot \mathrm{DAC}_1[E_0] \tag{2}$$

where $V_{O[1]}$ is the amplifier output and E_0 is the initial DSM output. The integrator output ($V_{O[j]}$) after the jth cycle is

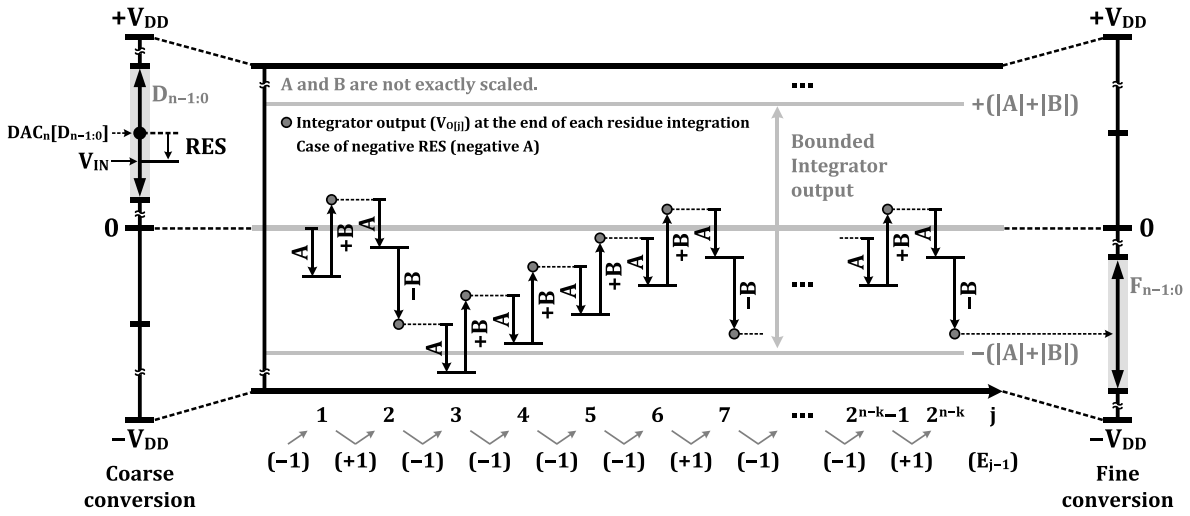

Fig. 3. Overall operation of proposed SAR ADC.

derived as

$$V_{O[j]} = V_{O[j-1]} + 2^k \cdot \mathrm{RES} - 2^{-r} \cdot \mathrm{DAC}_1[E_{j-1}] = j \cdot 2^k \cdot \mathrm{RES} - 2^{-r} \cdot \sum_{i=1}^{j} \mathrm{DAC}_1[E_{i-1}]. \quad (3)$$

Therefore, the final value ($V_{O[2^{n-k}]}$) after the 2^{n-k}th RI becomes

$$V_{O[2^{n-k}]} = 2^n \cdot V_{\mathrm{IN}} - 2^n \cdot \mathrm{DAC}_n[D_{n-1:0}] - 2^{-r} \cdot \sum_{j=1}^{2^{n-k}} \mathrm{DAC}_1[E_{j-1}] \quad (4)$$

which is then converted by SAR to obtain the LSBs ($F_{n-1:0}$).

The operation of DSM effectively confines the integrator output to help maintain a high open-loop gain of amplifier. By (2) and (3), the integrator output ($V_{O[j]}$) is bounded by

$$-(|2^k \cdot \mathrm{RES}| + |2^{-r} \cdot \mathrm{DAC}_1[E_{j-1}]|) \le V_{O[j]} \le +(|2^k \cdot \mathrm{RES}| + |2^{-r} \cdot \mathrm{DAC}_1[E_{j-1}]|) \quad (5)$$

only if $|2^k \cdot \mathrm{RES}| \le |2^{-r} \cdot \mathrm{DAC}_1[E_{j-1}]|$. It is graphically explained in Fig. 3, where the residue becomes bounded between $-(|A| + |B|)$ and $+(|A| + |B|)$ if $|A| \le |B|$. The maximum of $|2^k \cdot \mathrm{RES}|$ is $2^k \cdot (V_{\mathrm{DD}}/2^n)$ and $|2^{-r} \cdot \mathrm{DAC}_1[E_{j-1}]|$ is $2^{-r} \cdot V_{\mathrm{DD}}$ if V_{DD} is used as the reference voltage of ADC and DAC as well as supply voltage. Therefore, to meet the bounding condition of $|2^k \cdot \mathrm{RES}| \le |2^{-r} \cdot \mathrm{DAC}_1[E_{j-1}]|$, r should be smaller than or equal to $n - k$. On the other hand, the $\max(|V_{O[j]}|)$ increases as r decreases. Therefore, r and k can be optimized for given n, considering the condition of $r \le n - k$ as well as the amplifier OVR.

C. Digital Output

The second-SAR operation approximates $V_{O[2^{n-k}]}$ with the same DAC_n to obtain fine n-bit LSBs ($F_{n-1:0}$). The final residue can be expressed as

$$\begin{aligned} V_{O[2^{n-k}]} - \mathrm{DAC}_n[F_{n-1:0}] &= 2^n \cdot V_{\mathrm{IN}} - 2^n \cdot \mathrm{DAC}_n[D_{n-1:0}] - \mathrm{DAC}_n[F_{n-1:0}] - 2^{-r} \cdot \sum_{j=1}^{2^{n-k}} \mathrm{DAC}_1[E_{j-1}] \\ &= 2^n \cdot V_{\mathrm{IN}} - 2^{n-1} \cdot \mathrm{DAC}_1[D_{n-1}] - \cdots - 2^0 \cdot \mathrm{DAC}_1[D_0] - 2^{-1} \cdot \mathrm{DAC}_1[F_{n-1}] - \cdots \\ &\quad - 2^{-r} \cdot \mathrm{DAC}_1[F_{n-r}] - \cdots - 2^{-n} \cdot \mathrm{DAC}_1[F_0] \\ &\quad - 2^{-r} \cdot (\mathrm{DAC}_1[E_0] + \mathrm{DAC}_1[E_1] \cdots + \mathrm{DAC}_1[E_{2^{n-k}-1}]) \end{aligned} \quad (6)$$

which becomes zero. Note that all E_j have an identical weight of 2^{-r}, which corresponds to the weight of F_{n-r} (Fig. 4). Therefore, the sum of all E_j can provide an overlapped code range between MSBs and LSBs. If $n - k$ is set to be greater than or equal to $r + 1$, it has the significant figures ranging from F_{n-r} up to $D_{n-k-r-1}$, providing an overlapped code range for redundancy to compensate the comparator error in the first-coarse conversion stage. In addition, extra error occurs during the RI. V_{IN} may change while it is approximated only by the initially obtained fixed code. The overlapped code also compensates this error to a certain extent, which will be described with detailed analysis later. To form a 16-bit ADC in this paper, we set n, k, and r to 8, 3, and 2, respectively. The sum of $E_{31:0}$ has an overlapped range between D_2 and F_6. Since the average of the sum is 16 and its weight corresponds to that of F_6, the output is represented with a 17-bit code ($G_{16:0}$) with a code offset of 1024. A subtraction of 1024 leads to the final 16-bit output code.

III. Implementation

A. ADC Configuration

The proposed ADC consists of a capacitor digital-to-analog converter (CDAC), an amplifier (AMP), and two comparators, respectively, for SAR conversion (COMP_SAR) and a quantizer for DSM (COMP_RI) (Fig. 5). It is designed with

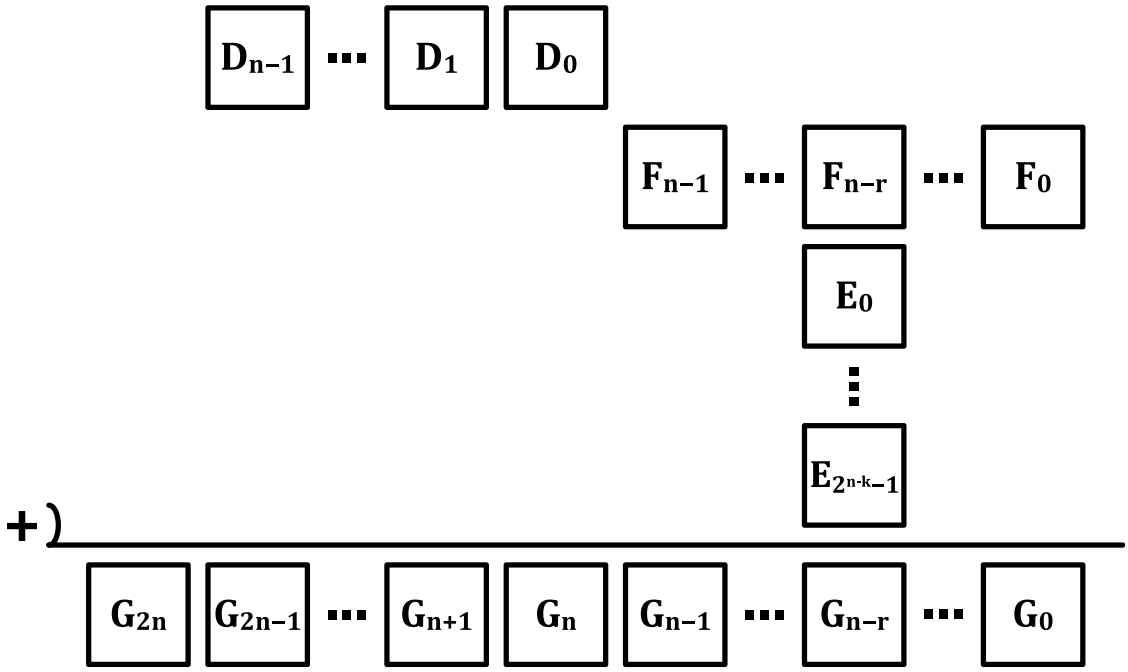

Fig. 4. Digital output generation.

fully differential manner to suppress common-mode noise with input signal doubled. The CDAC is composed of three capacitor groups: 1) capacitors (C_F) for coarse 8-bit decision; 2) larger capacitors (C_S) for taking the 8-bit coarse code during RI; and 3) a capacitor (C_E) used for a 1-bit DAC to reflect DSM output (E_{j-1}) during RI. The use of smaller capacitance C_F speeds up the coarse MSB conversion [Fig. 5(a)]. After the completion of the coarse conversion, the MSBs are applied to C_S during the RI while C_F is configured as an integration capacitor for DSM [Fig. 5(b)]. At the end of RI, the total residue becomes automatically sampled in C_F and is converted through the same 8-bit SAR operation used in the coarse conversion [Fig. 5(a)]. Therefore, by setting $n = 8$, $k = 3$, and $r = 2$, RI with a step gain of 2^3 is repeated 2^5 times, resulting in an inter-stage gain of 2^8. Since r is less than $n-k$, the integrator output is bounded by DSM operation. For given design parameters, the total capacitance for C_F becomes 128 C for 8-bit coarse and fine SAR conversions, and those for C_S and C_E are, respectively, set to 1024 and 32 C since 2^k and 2^{-r} are determined by C_S/C_F and C_E/C_F. Therefore, the ADC requires only 1184 C in total which is much fewer than that of the conventional 16-bit SAR ADC with a binary-weighted CDAC.

A series of timings for conversion is internally generated as in the asynchronous ADC architecture [12] (Fig. 6). When $\Phi_{\text{SAR\_SAMP}}$ is high (T_{IDLE}), switches for C_F are closed to track the differential input signal ($V_{\text{IN}} = V_{\text{IN}}^+ - V_{\text{IN}}^-$). The conversion process (T_{ACT}) begins with a falling transition of $\Phi_{\text{SAR\_SAMP}}$. It is followed by a pulse at $\Phi_{\text{SAR\_CONV}}$, where quick and coarse asynchronous SAR logic runs to obtain 8-bit MSBs ($D_{7:0}$). A merged-capacitor switching scheme [13] is employed for saving switching energy during SAR conversion. The 2^5-times non-overlapped activations of $\Phi_{\text{RI\_SAMP}}$ and $\Phi_{\text{RI\_EVAL}}$ perform switched-capacitor-based integration with RI logic. The completion of RI leads to another pulse at $\Phi_{\text{SAR\_CONV}}$ to perform the same asynchronous SAR conversion for fine 8-bit LSBs ($F_{7:0}$). The conversion result updates the output registers at every rising edge of $\Phi_{\text{SAR\_SAMP}}$. The residue amplifier is turned ON only at the output evaluation phase [14] to save power consumption. In this paper, the conversion time (T_{ACT}) is about 2 μs and the frequency of $\Phi_{\text{RI\_SAMP}}$ and $\Phi_{\text{RI\_EVAL}}$ is about 20 MHz. The coarse SAR conversion, RI, and fine SAR conversion, respectively, occupy about 150, 1600, and 150 ns, and the remaining active time is taken by timing margin for robust operation.

B. Residue Integration With DEM

Fig. 7 describes detailed circuit configuration during the RI. After the first-RI step, the differential integrator output ($V_{O[1]} = V_{O[1]+} - V_{O[1]-}$) becomes

$$V_{O[1]} = V_{O[1]}^+ - V_{O[1]}^- = 2^3 \cdot \text{RES} - 2^{-2} \cdot (E_0 - \overline{E_0}) \cdot V_{\text{DD}} \quad (7)$$

where $\text{RES} = V_{\text{IN}} - V_{\text{DD}} \cdot (((D_7 - \overline{D_7})/2^1) + \cdots + ((D_0 - \overline{D_0})/2^8))$. E_0 is initially set to 0 ($\overline{E_0} = 1$). $V_{O[j]}$ after the jth RI is derived as

$$\begin{aligned} V_{O[j]} &= V_{O[j]}^+ - V_{O[j]}^- \\ &= V_{O[j-1]} + 2^3 \cdot \text{RES} - 2^{-2} \cdot (E_{j-1} - \overline{E_{j-1}}) \cdot V_{\text{DD}} \\ &= j \cdot 2^3 \cdot \text{RES} - 2^{-2} \cdot \sum_{i=1}^{j} (E_{i-1} - \overline{E_{i-1}}) \cdot V_{\text{DD}}. \end{aligned} \quad (8)$$

By (7) and (8), it is bounded as

$$\begin{aligned} &-(\max\ (|2^3 \cdot \text{RES}|) + |2^{-2} \cdot (E_{j-1} - \overline{E_{j-1}}) \cdot V_{\text{DD}}|) \\ &\le V_{O[j]} \le +(\max(|2^3 \cdot \text{RES}|) + |2^{-2} \cdot (E_{j-1} - \overline{E_{j-1}}) \cdot V_{\text{DD}}|) \end{aligned} \quad (9)$$

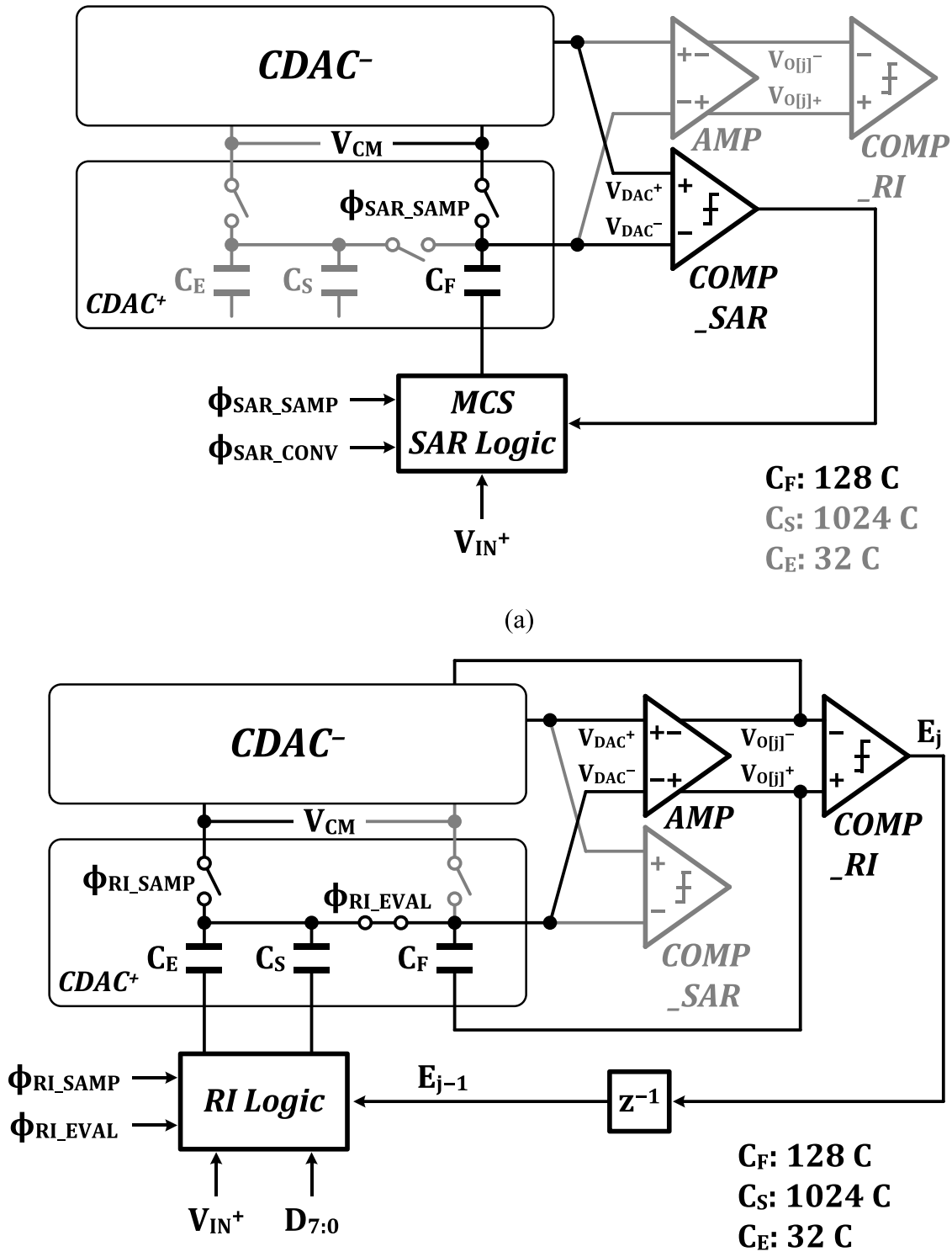

Fig. 5. Circuit configuration (a) at coarse/fine conversion and (b) at RI.

so that

$$-9 \cdot \frac{V_{\mathrm{DD}}}{2^5} \leq V_{O[j]} \leq +9 \cdot \frac{V_{\mathrm{DD}}}{2^5} \tag{10}$$

since $\max\left(|2^3 \cdot \mathrm{RES}|\right) = (V_{\mathrm{DD}}/2^5)$ and $|2^{-2} \cdot (E_{j-1} - \overline{E_{j-1}}) \cdot V_{\mathrm{DD}}| = 2^{-2} \cdot V_{\mathrm{DD}}$. Equation (10) reveals that the amplifier output swing is bounded to less than only 30% of V_{DD}.

Utilizing 2^5-times repeated cycles for the RI, dynamic element matching (DEM) [15], [16] is also employed for 5 MSBs (Fig. 7). The capacitors ($C_{S7:S3}$) for $D_{7:3}$ are implemented with a segmented capacitor array which consists of

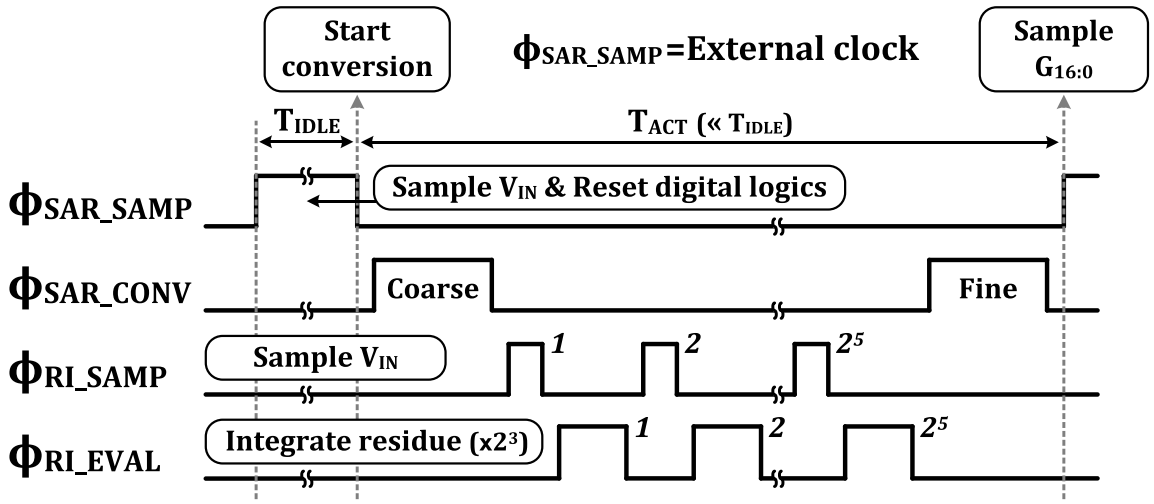

Fig. 6. Operation sequence with timing diagram.

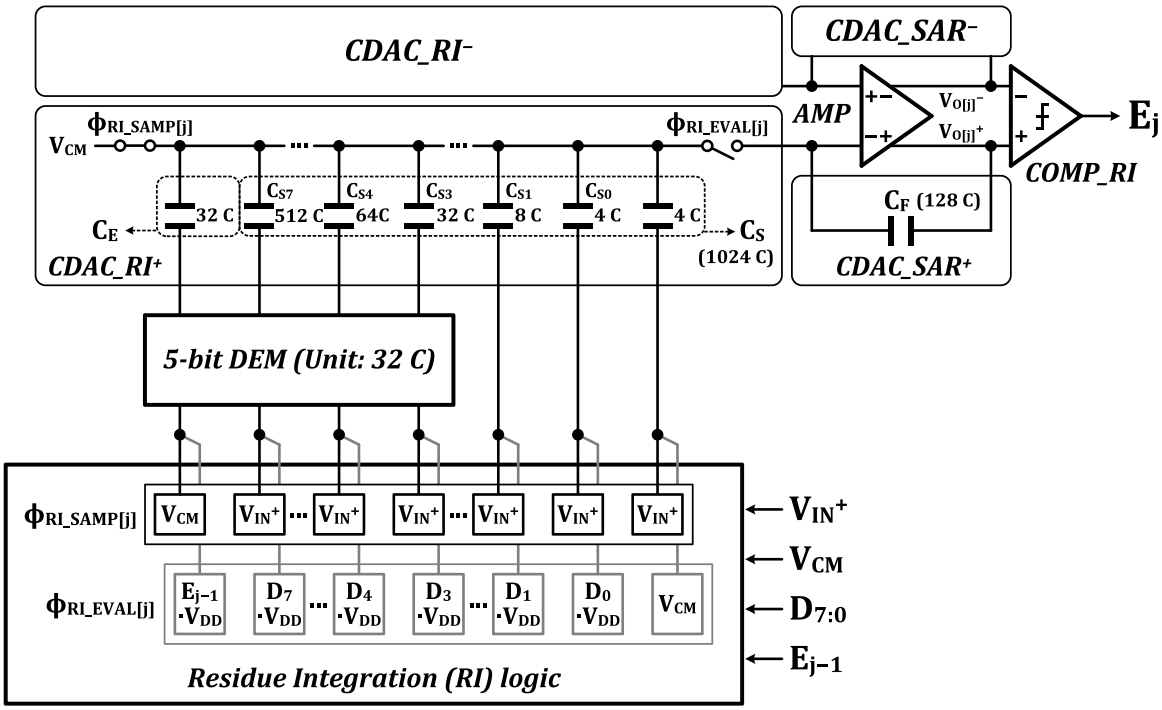

Fig. 7. RI with 5-bit DEM.

31 capacitors whose capacitance is 32 C. The 31 capacitors and C_E form a set of 32 identical capacitors for DEM. By rotating the roles of each capacitor, the 2^5 cycles for the RI support a full one-cycle rotation for capacitance averaging. It suppresses the effect of capacitor mismatch among $C_{S7:S3}$ and C_E.

C. Amplifier and Comparator

A transconductance-based (Gm-based) amplifier [17] is adopted for the residue amplification. The designed amplifier achieves a dc gain of 85.2 dB (Fig. 8). Since the amplifier output becomes the input for 8-LSBs conversion, the gain requirement achieving less than 0.5-bit error becomes about 4000 or 72 dB with the inter-stage gain of 2^3. Though this requirement is further relieved to around 60 dB by DSM, maximizing the small-signal gain is important for compensating possible non-linearity caused by large-signal behavior and robust operation under PVT variations. Simulated phase margin is 60.5° which is acquired at the frequency whose gain crosses 2^3 since the amplifier is used in a gain of 2^3 feedback configuration. Simulated input-referred noise density (Fig. 9) of the residue amplifier reveals that $1/f$ noise is the dominant noise source. The root-mean-square input-referred noise [17] integrated from 1 Hz to 1 GHz is 203 μV. The comparator is formed with a strong-ARM stage [18] followed by an

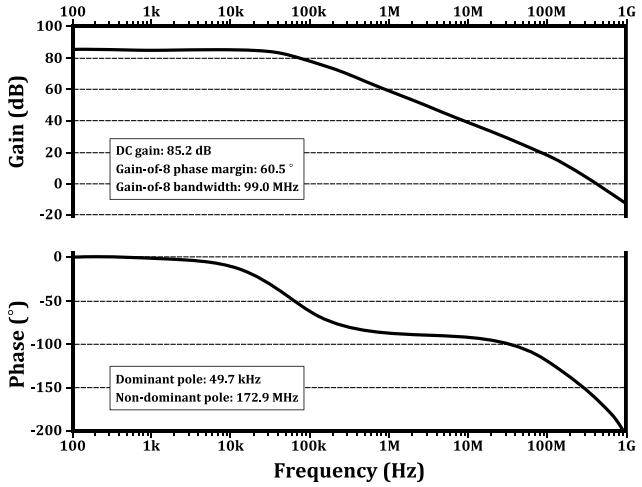

Fig. 8. Transfer characteristics of residue amplifier.

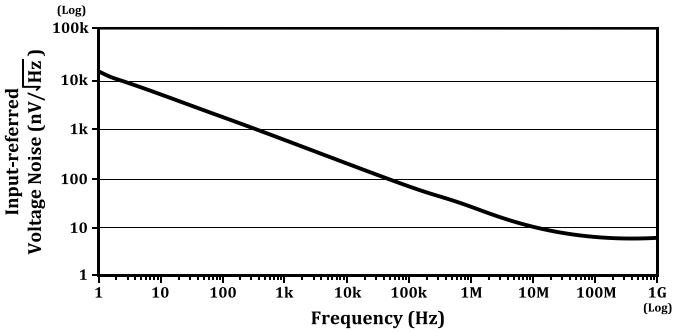

Fig. 9. Input-referred noise density of residue amplifier.

RS latch. For the asynchronous-clocking operation, the comparator autonomously generates "comparison end" signal when decision is completed, and passes it to digital logic with resetting the comparator [3].

Monte-Carlo simulations with 1000 hits are conducted for input offset voltages of amplifier and comparator. Simulated standard deviations (σ) are, respectively, 16.8 and 7.1 mV. The input offsets can be problematic by excessively increasing the integrator output swing. Though the DSM can alleviate this problem to some extent, more attention needs to be paid to analyze the effect of offsets.

IV. Analysis

A. Amplifier Offset

Assuming $V_{\rm OS}$ is the input-referred offset voltage of the residue amplifier, the integrator output ($V_{O[j]}$) contains the effect ($V_{O\cdot{\rm OS}[j]}$) of the offset. $V_{O[j]}$ at the jth RI step is derived as

$$V_{O[j]} = j\cdot 2^3\cdot {\rm RES} - 2^{-2}\cdot\sum_{i=1}^{j}(E_{i-1}-\overline{E_{i-1}})\cdot V_{\rm DD} + V_{O\cdot{\rm OS}[j]} \tag{11}$$

where $V_{O\cdot{\rm OS}[j]} = ((C_F + j\cdot(C_S+C_E))/C_F)\cdot V_{\rm OS} = (1 + j\cdot(33/4))\cdot V_{\rm OS}$ (Fig. 10). If $V_{\rm OS}$ is assumed to be constant,

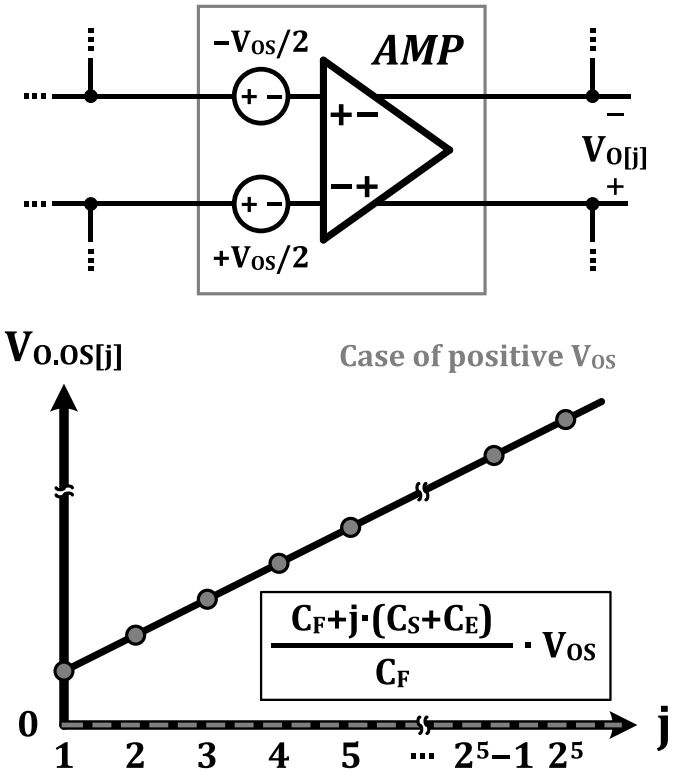

Fig. 10. Effect of amplifier offset during RI.

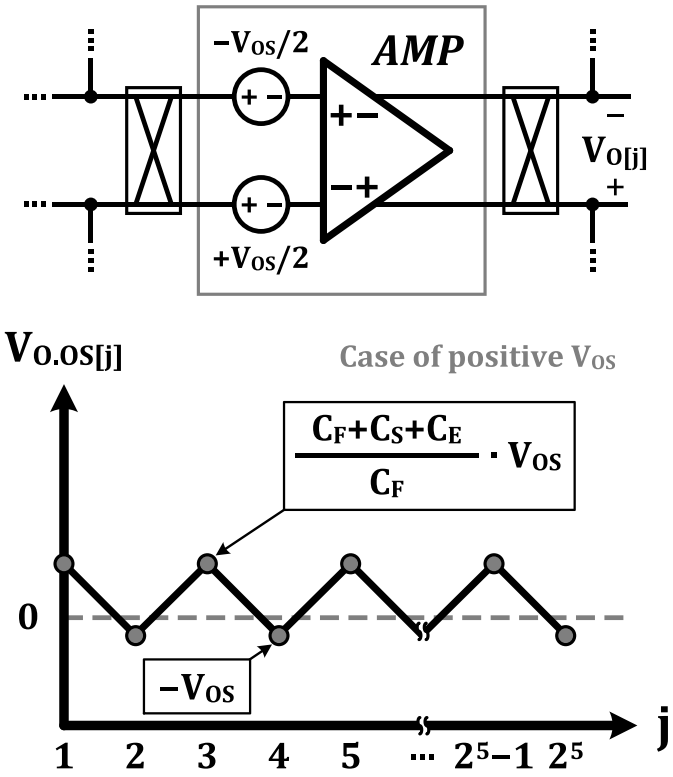

Fig. 11. Suppression of offset-induced error by chopping at residue amplifier.

$V_{O\cdot{\rm OS}[j]}$ can become excessively large and drives $V_{O[j]}$ outside the amplifier OVR as RI proceeds.

Auto-zeroing [19] or correlated double sampling [20], [21] could be employed for offset cancellation. But, in those

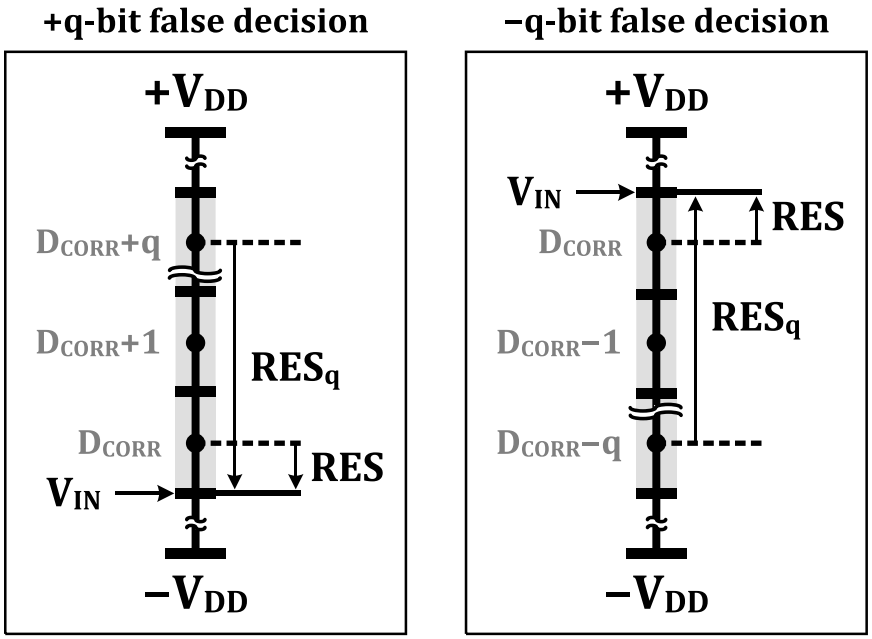

Fig. 12. Non-ideal residue (maximum case) with ±q-bit false decision at coarse conversion due to comparator offset.

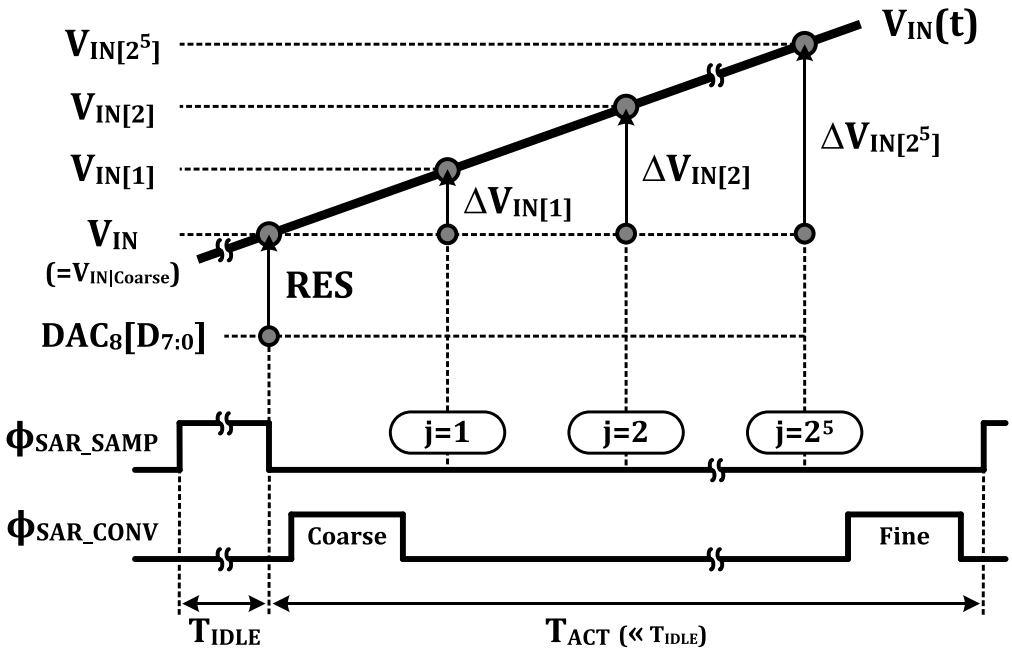

Fig. 13. Residue accumulation by failure of transient V_{IN} representation with a fixed coarse code.

schemes, the amplifier should be always turned ON to hold feedback configuration, causing extra power consumption. Instead, this paper employs a chopping [22] (Fig. 11) which alternately changes signal paths whenever Φ_{RI_EVAL} becomes high to compensate the effect of offset. Then, $V_{O.OS[j]}$ becomes

$$V_{O.OS[j]} = \begin{cases} +\dfrac{C_F+C_S+C_E}{C_F} = +\dfrac{37}{4}\cdot V_{OS} & j = \text{odd number} \\ -V_{OS} & j = \text{even number.} \end{cases} \tag{12}$$

Thus, it is bounded without integration, and the offset-induced term at the final $V_{O[2^5]}$ is only $-V_{OS}$ regardless of input. With a modification of (10) to reflect the effect of amplifier offset, $V_{O[j]}$ is confined as

$$-\left(9\cdot\frac{V_{DD}}{2^5}+\frac{37}{4}\cdot|V_{OS}|\right) \le V_{O[j]} \le +\left(9\cdot\frac{V_{DD}}{2^5}+\frac{37}{4}\cdot|V_{OS}|\right) \tag{13}$$

if $((V_{DD}/2^5) + (37/4)\cdot|V_{OS}|) \le 2^{-2}\cdot V_{DD}$ or $|V_{OS}| \le (7/(2^3\cdot 37))\cdot V_{DD}$. Therefore, the chopping effectively reduces the effect of offset with additional suppression of $1/f$ noise of the amplifier.

TABLE I
POWER BREAKDOWN

Power breakdown (μW)			
Analog	Amplifier	1.44	3.18
	CDAC_SAR	0.03	
	CDAC_RI	1.72	
Digital	COMP_SAR	0.04	4.75
	COMP_RI	0.09	
	CDAC control logic (SAR Logic & RI Logic)	4.57	
	Backend adder	0.04	
Total power consumption			7.93

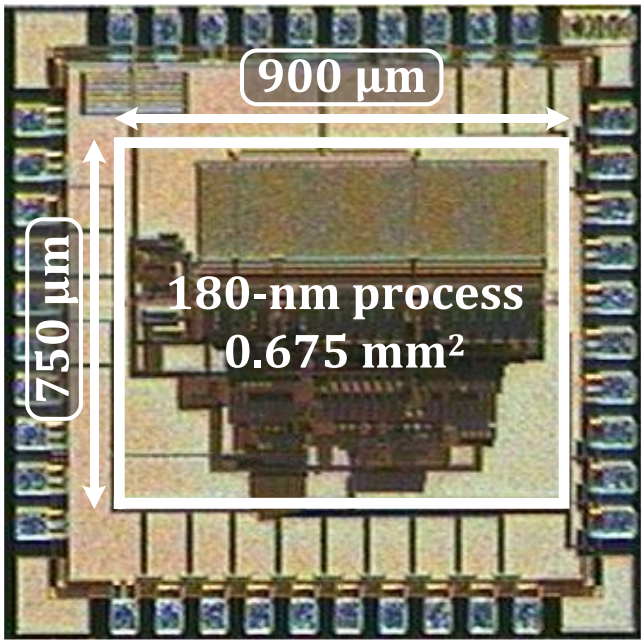

Fig. 14. Die photograph.

B. Comparator Offset

The comparator offset induces a false decision in the coarse SAR conversion (Fig. 12). The false decision causes an extra increase in the integrator output. If the comparator makes q-bit error ($D_{\mathrm{CORR}} \pm q$) from correct decision (D_{CORR}), the integrator output ($V_{O[j]}$) after the jth RI step becomes

$$V_{O[j]} = j \cdot 2^3 \cdot \mathrm{RES}_q - 2^{-2} \cdot \sum_{i=1}^{j} (E_{i-1} - \overline{E_{i-1}}) \cdot V_{\mathrm{DD}} \quad (14)$$

where RES_q represents the residue by q-bit false SAR decision. Since $\max(|2^3 \cdot \mathrm{RES}_q|) = (2q+1) \cdot (V_{\mathrm{DD}}/2^5)$ (Fig. 12), it is confined by DSM as

$$-(2q+9) \cdot \frac{V_{\mathrm{DD}}}{2^5} \le V_{O[j]} \le +(2q+9) \cdot \frac{V_{\mathrm{DD}}}{2^5} \quad (15)$$

if $(2q+1) \cdot (V_{\mathrm{DD}}/2^5) \le 2^{-2} \cdot V_{\mathrm{DD}}$, thus $q \le (7/2)$.

C. Bandwidth Limitation by Failure of Input Tracking

Analyses from Sections II to IV-B assume the case of dc input. However, the input can change during the RI. Therefore, the failure of input representation with a fixed coarse code is also a significant factor of increase in the amplifier output swing (Fig. 13).

The residue (RES_j) resulted from an additional change ($\Delta V_{\mathrm{IN}[j]}$) of input during RI becomes

$$\mathrm{RES}_j = (V_{\mathrm{IN}[j]} - V_{\mathrm{IN}}) + \mathrm{RES} = \Delta V_{\mathrm{IN}[j]} + \mathrm{RES}. \quad (16)$$

The integrator output ($V_{O[j]}$) after the jth RI step can be modified as

$$V_{O[j]} = j \cdot 2^3 \cdot \mathrm{RES} + 2^3 \cdot \sum_{i=1}^{j} \Delta V_{\mathrm{IN}[i]} - 2^{-2} \cdot \sum_{i=1}^{j} (E_{i-1} - \overline{E_{i-1}}) \cdot V_{\mathrm{DD}} \quad (17)$$

which is confined by DSM as

$$-\left(2^3 \cdot \max(|\Delta V_{\mathrm{IN}[j]}|) + 9 \cdot \frac{V_{\mathrm{DD}}}{2^5}\right) \le V_{O[j]} \le +\left(2^3 \cdot \max(|\Delta V_{\mathrm{IN}[j]}|) + 9 \cdot \frac{V_{\mathrm{DD}}}{2^5}\right) \quad (18)$$

if $2^3 \cdot \max(|\Delta V_{\mathrm{IN}[j]}|) + (V_{\mathrm{DD}}/2^5) \le 2^{-2} \cdot V_{\mathrm{DD}}$, or $\max(|\Delta V_{\mathrm{IN}[j]}|) \le 7 \cdot (V_{\mathrm{DD}}/2^8)$.

The maximum allowable input frequency (f_{IN}) is closely related to $\max(|\Delta V_{\mathrm{IN}[j]}|)$. To bound the integrator output within amplifier OVR ($\max(|V_{O.\mathrm{AMP}}|)$), $\max(|\Delta V_{\mathrm{IN}[j]}|)$ should satisfy the following condition:

$$\max(|\Delta V_{\mathrm{IN}[j]}|) \le \min\left(\frac{\max(|V_{O.\mathrm{AMP}}|)}{2^3} - 9 \cdot \frac{V_{\mathrm{DD}}}{2^8}, 7 \cdot \frac{V_{\mathrm{DD}}}{2^8}\right). \quad (19)$$

For a sinusoidal input (V_{IN}) with a full-scaled amplitude, or

$$V_{\mathrm{IN}} = V_{\mathrm{DD}} \cdot \sin(2\pi f_{\mathrm{IN}} \cdot t) \quad (20)$$

the maximum value of time derivative, $2\pi f_{\mathrm{IN}} \cdot V_{\mathrm{DD}}$, gives the boundary condition for the worst case. Equating $\max(|\Delta V_{\mathrm{IN}[j]}|)$ to $2\pi f_{\mathrm{IN}} \cdot V_{\mathrm{DD}} \cdot T_{\mathrm{ACT}}$, (19) leads to the maximally convertible input frequency (f_{IN})

$$f_{\mathrm{IN}} \le \frac{1}{2\pi \cdot V_{\mathrm{DD}} \cdot T_{\mathrm{ACT}}} \cdot \min\left(\frac{\max(|V_{O.\mathrm{AMP}}|)}{2^3} - 9 \cdot \frac{V_{\mathrm{DD}}}{2^8}, 7 \cdot \frac{V_{\mathrm{DD}}}{2^8}\right). \quad (21)$$

By applying T_{ACT} of 2 μs designed in this paper, the bandwidth is revealed to be a range of kilohertz.

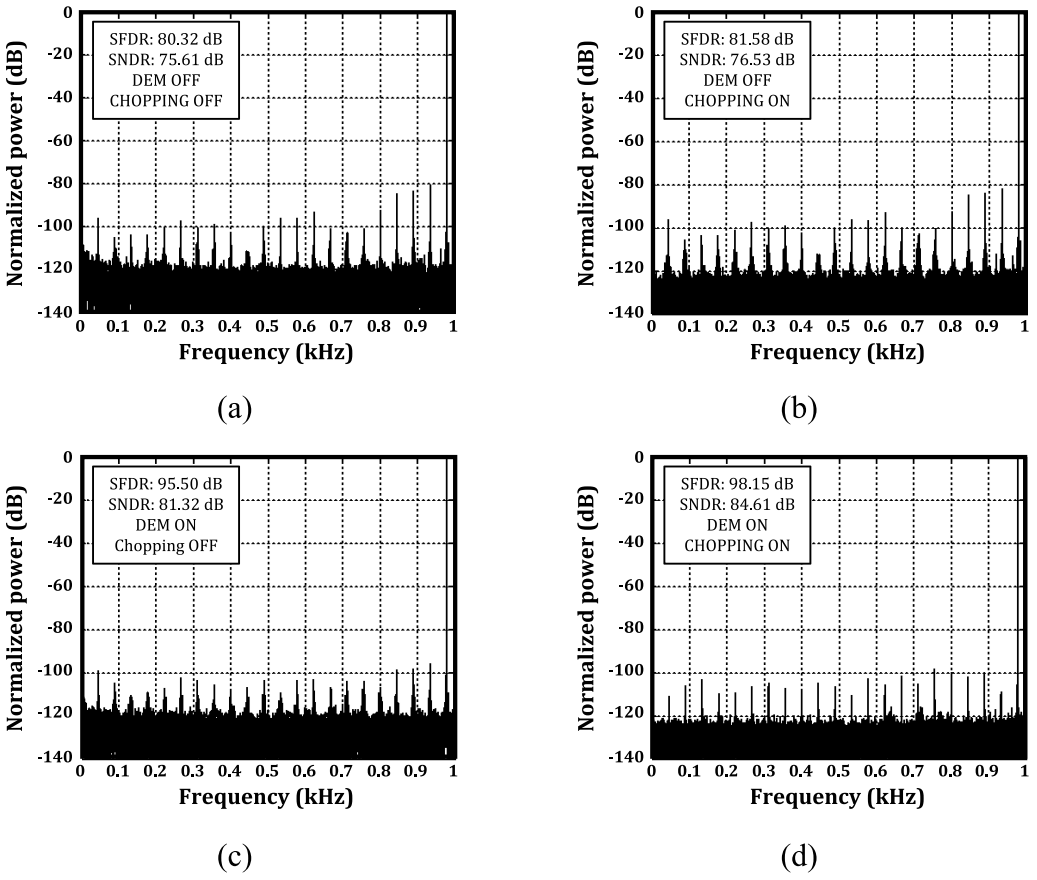

Fig. 15. Nyquist-rate FFT spectra (a) with neither chopping nor DEM, (b) with chopping only, (c) with DEM only, and (d) with both chopping and DEM.

D. Integrator Output Within Amplifier OVR

Considering all the issues mentioned above, the integrator output ($V_{O[j]}$) after the completion of the jth RI step is derived as

$$V_{O[j]} = j\cdot 2^3 \cdot \mathrm{RES}_q + 2^3 \cdot \sum_{i=1}^{j} \Delta V_{\mathrm{IN}[i]} - 2^{-2} \cdot \sum_{i=1}^{j} (E_{i-1} - \overline{E_{i-1}}) \cdot V_{\mathrm{DD}} + V_{O.\mathrm{OS}[j]} \quad (22)$$

and confined by DSM as

$$-\left(2^3 \cdot \max(|\Delta V_{\mathrm{IN}[j]}|) + (2q+9) \cdot \frac{V_{\mathrm{DD}}}{2^5} + \frac{37}{4} \cdot |V_{\mathrm{OS}}|\right) \le V_{O[j]} \le +\left(2^3 \cdot \max(|\Delta V_{\mathrm{IN}[j]}|) + (2q+9) \cdot \frac{V_{\mathrm{DD}}}{2^5} + \frac{37}{4} \cdot |V_{\mathrm{OS}}|\right) \quad (23)$$

if $2^3 \cdot \max(|\Delta V_{\mathrm{IN}[j]}|) + (2q+1) \cdot (V_{\mathrm{DD}}/2^5) + (37/4) \cdot |V_{\mathrm{OS}}| \le 2^{-2} \cdot V_{\mathrm{DD}}$. The boundaries should be within the amplifier OVR for maintaining a high open-loop gain. The simulated amplifier shows a small-signal dc-gain of over 80 dB (Fig. 8) and maintains over 70 and 60 dB even at an output swing of 0.72 and 0.78 V_{DD}, respectively.

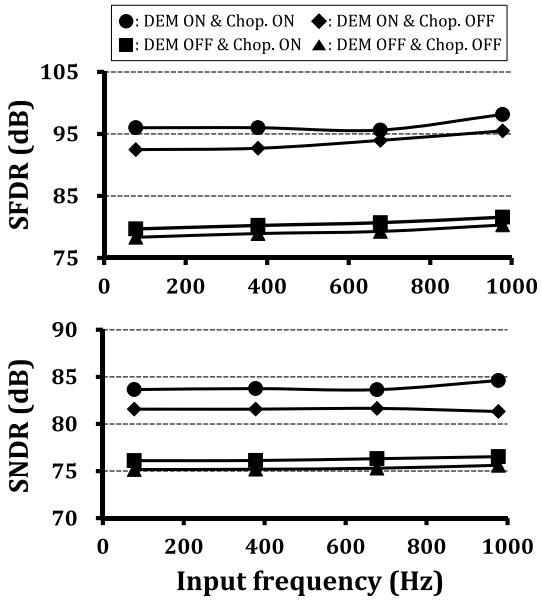

Fig. 16. SNDR and SFDR versus input frequency according to use of chopping and DEM at a sampling rate of 2 kS/s.

V. Measurement

The designed 16-bit SAR ADC was implemented using 180-nm CMOS process. Active area is 0.68 mm^2 (Fig. 14).

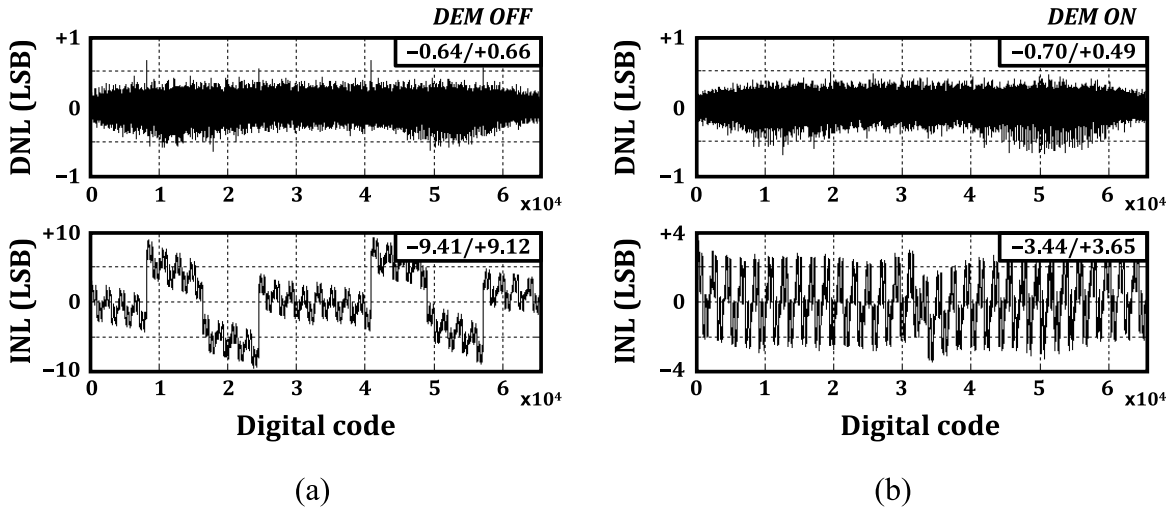

Fig. 17. Measured linearity (a) without DEM and (b) with DEM at a sampling rate of 2 kS/s.

TABLE II
PERFORMANCE COMPARISON WITH NYQUIST-RATE ADCS

	This work	VLSI'16 [23]	VLSI'16 [2]	ASSCC'16 [24]	ISSCC'14 [25]	VLSI'14 [26]	ISSCC'10 [27]	ISSCC'04 [28]	VLSI'04 [29]
Architecture	SAR	SAR	SAR	SAR	SAR	pipe SAR	pipe SAR	Pipelined	Cyclic
Technology [nm]	180	40	130	55	65	180	250	180	130
Resolution [bit]	16	15	14	16	14	18	18	14	16
Supply [V]	1.8	-	1.5	1.2	0.8	5.0/1.8	5.0/2.5	1.8	3
f_s [kS/s]	2	20	1	1000	32	5000	12500	10000	500
Power [μW]	7.93	1.17	1.3	6950	0.352	30520	105000	112000	6000
$SFDR_{Nyquist}$ [dB]	98.2	95.1	95.4*	-	78.5	-	82.0	99.0	-
$SNDR_{Nyquist}$ [dB]	84.6	74.1	75.0*	81.0**	69.7	98.6*	80.0	73.0	77.4
FOM_S [dB]	165.6	173.4	160.9*	159.6**	176.3	177.7*	157.7	149.5	153.6
Area [mm^2]	0.68	0.32	-	4.10	0.18	5.74	4.50	15.05	0.50

FOM_S=SNDR+10·log(f_s/2/Power); *with low frequency input; **with SNR as well as low frequency input

The unit capacitance of CDAC is 20.28 fF in an area of 7.5 μm × 6.5 μm, which is the smallest available metal–insulator–metal (MIM) capacitance with given technology. The ADC consumes 7.93 μW from a supply of 1.8 V at 2 kS/s (Table I). Analog and digital parts, respectively, dissipate 3.18 and 4.75 μW. The full range differential input amplitude is up to ±1.8 V_{pp} or 3.6 $V_{pp.diff}$.

Fig. 15 shows measured Nyquist-rate fast Fourier transform (FFT) spectra. An input signal of 977.777 Hz was applied. The 2^{16} samples were taken to obtain FFT spectrum. Seven-term Blackman–Harris window was adopted to minimize spectral leakage. The effects of chopping and DEM are quantified with SFDR and SNDR. Compared with Fig. 15(a) and (c), the chopping suppresses dc and low-frequency noise, as shown in Fig. 15(b) and (d). DEM reduces harmonic power, resulting in over 15 dB improvement in SFDR [Fig. 15(c) and (d)]. With both chopping and DEM, the ADC achieves an SNDR of 84.6 dB and an SFDR of 98.2 dB, respectively. The high SFDR and SNDR are maintained in the whole range of the input frequency (Fig. 16).

The effect of DEM can be seen by linearity measurements. The best fit straight line method was used for the linearity assessment. While the original integral non-linearity (INL) is −9.41/+9.12 LSB without DEM [Fig. 17(a)], it is improved to −3.44/+3.65 LSB with DEM [Fig. 17(b)]. Note that DEM is applied to only 5 MSBs. Remaining non-linearity is dominated by repeated 32 patterns in INL diagram. Since upper 5-MSB capacitors are well averaged by DEM, the outstanding INL is mostly caused by capacitor mismatch on the lower three MSB capacitors for D_2, D_1, and D_0; more by D_2 and less by D_0. It is because the effect of error is amplified by 2^5 times by RI, while the capacitance of 16, 8, and 4 C for D_2, D_1, and D_0 are relatively small.

Table II compares performance with previous works on high-resolution (≥14 bit) Nyquist-rate ADCs [2], [23]–[29]

TABLE III
PERFORMANCE COMPARISON WITH OS/NS SAR ADCS

	This work	ISSCC'16 [10]	ISSCC'16 [11]	ESSCIRC'16 [30]
Technology [nm]	180	55	160	130
Supply [V]	1.8	1.2	1.8	1.2
f_s [kS/s]	2	1000	11290	2000
Bandwidth [kHz]	1	1	20	125
Power [μW]	7.93	15.7*	1650*	61*
SFDR [dB]	98.2	105.1	-	95.0
SNDR [dB]	84.6	101.0	98.3	74.0
FOM_S [dB]	165.6	179.0	169.1	167.1
Area [mm^2]	0.68	0.072	0.16	0.13

FOM_S=SNDR+10·log(Bandwidth/Power)
*without power consumption for decimation filtering

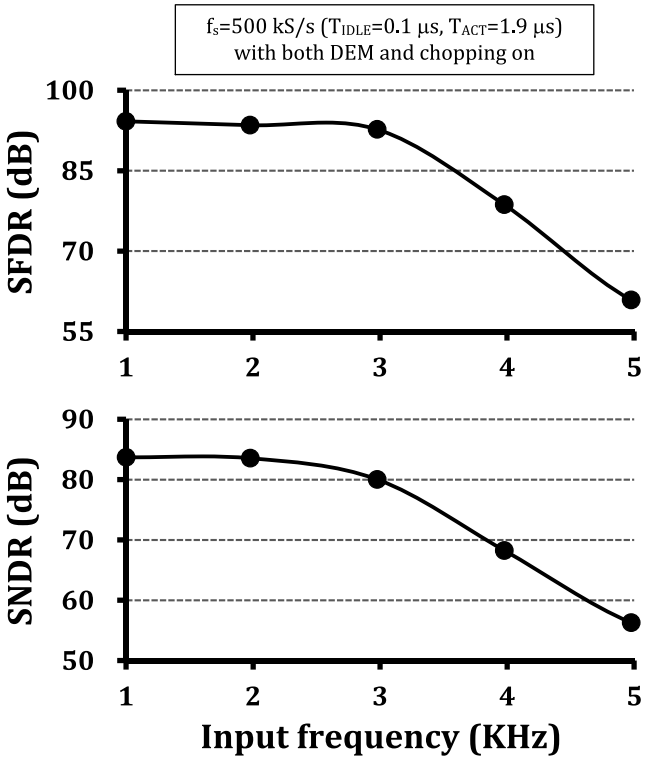

Fig. 18. SNDR and SFDR versus input frequency at maximum sampling rate (500 kS/s).

with similar targets of sampling rate. Among ADCs with SNDR of above 80 dB, this paper achieves the lowest power consumption. The proposed ADC is promising for ultralow-power implantable applications for acquiring fine-precision bio-potential signals whose bandwidth is typically within 1 kHz. The figure of merit (FOM) of the proposed residue-integrated SAR ADC is also comparable to those of the previously reported OS/NS SAR ADCs [10], [11], [30] (Table III). Note that, unlike the proposed ADC, OS/NS SAR ADCs need post-processing for decimation filtering whose power consumption is not included in the table. In addition, since the proposed ADC consumes most of energy in digital circuits (Table I), implementation using scaled CMOS process would further improve FOM.

VI. CONCLUSION

This paper presents a low-power fine-precision asynchronous-clocking SAR ADC architecture for sensor applications. The proposed RI scheme combined with a DEM alleviates the effect of performance-limiting factors in the conventional SAR ADC, such as comparator noise and capacitor mismatch. The fabricated 16-bit ADC in 180-nm CMOS achieves 84.6-dB SNDR, 98.2-dB SFDR, and 7.93-μW power consumption at 2 kS/s.

We demonstrated this paper as a Nyquist-rate ADC. As the bandwidth is limited to about 1 kHz due to the failure of fast input tracking, performance evaluation was conducted at the Nyquist sampling rate of 2 kS/s. However, the total conversion time (T_{ACT}) is only about 2 μs driven by internally generated timings. Most of the time (498 μs) was spent in stand-by state for the input tracking. This fast conversion capability can give a great benefit when applied to multi-channel sensor applications. The sampling rate can be increased up to 500 kS/s while convertible signal bandwidth is still in the kilohertz range (Fig. 18). It makes a big difference from the conventional high-resolution approach with delta–sigma ADCs which require a long time integration for each conversion. For example, the proposed ADC can be applied to an array sensor supporting up to 250 channels of 1-kHz-band bio-potential signals. With a time-interleaved switching for 250 channels, the processing of 500 kS/s can provide the Nyquist-rate conversion for all the channels. Thus, the proposed architecture can be useful for multi-channel sensor applications requiring a high-precision conversion as well as ultralow power consumption.

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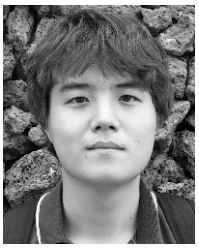

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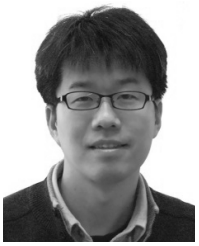

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