

An Analog-Assisted Tri-Loop Digital Low-Dropout Regulator

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Abstract—This paper presents an analog-assisted (AA) output-capacitor-free digital low-dropout (D-LDO) regulator with tri-loop control. For responding to instant load transients, the proposed high-pass AA loop momentarily adjusts the unit current of the power switch array, and significantly reduces the voltage spikes. In the proposed D-LDO, the overall 512 output current steps are divided into three sub-sections controlled by coarse/fine loops with carry-in/out operations. Therefore, the required shift register (SR) length is reduced, and a 9-bit output current resolution is realized by using only 28-SR bits. Besides, the coarse-tuning loop helps to reduce the recovery time, while the fine-tuning loop improves the output accuracy. To eliminate the limit cycle oscillation and reduce the quiescent current, a freeze mode is added after the fine-tuning operation. To reduce the output glitches and the recovery time, a nonlinear coarse word control is designed for the carry-in/out operations. The D-LDO is fabricated in a 65-nm general purpose CMOS process. A maximum voltage undershoot/overshoot of 105 mV is measured with a 10-mA/1-ns load step and a total capacitor of only 100 pF. Thus, the resulting figure-of-merit is 0.23 ps.

Index Terms—Amplifier, analog assisted (AA), coarse/fine tuning, digital control, fully integrated voltage regulator (FIVR), limit cycle oscillation (LCO), low-dropout (LDO) regulator, nonlinear control, output-capacitor-free, power management.

I. INTRODUCTION

TO EXPLORE higher power efficiencies, multiple divided voltage domains and fine-grained supply voltage management have been developed for energy-efficient digital systems and system-on-chips (SoCs), which allows each voltage domain to be optimized independently. To fulfill this target, hierarchical power delivering networks (Fig. 1) have been widely adopted, where the battery voltage is converted into

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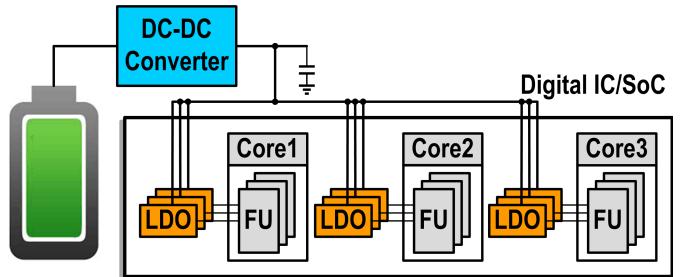


Fig. 1. Hierarchical power delivering network in a digital IC/SoC.

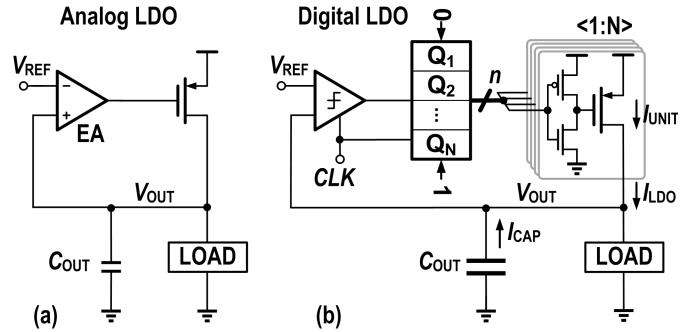


Fig. 2. Basic topologies of the conventional. (a) A-LDO. (b) D-LDO.

intermediate voltage using a dc–dc converter with high efficiency [1], and then multiple low-dropout (LDO) regulators are employed to provide the fine-grained supply management for the function units (FUs).

The analog LDO (A-LDO) shown in Fig. 2(a) is suitable for noise-sensitive analog/RF load circuits, since it can achieve fast transient response with low-quiescent current (I_Q) and good power supply rejection [2]–[6]. Moreover, in the past decade, the output-capacitor-free A-LDO has been popular for reducing the bill of materials and removing the bond-wire effects by full integration [7]–[9]. When the supply voltage goes down to a near-threshold level for energy-efficient loads, LDOs are still needed for fine-grained voltage domains and individual load performance/power optimization. Nevertheless, there may not be sufficient voltage headroom for the analog error amplifier (EA) to turn ON the power transistor in an A-LDO. Thus, a large power transistor would be required. Moreover, it is hard to implement a high loop gain for the EA with such low supply voltage.

Recently, the digital LDO (D-LDO) [10]–[30] gets significant attention due to its low-voltage operation capability and process scalability. As shown in Fig. 2(b), the baseline D-LDO [10] consists of a clocked comparator acting as a 1-bit analog-to-digital converter (ADC), a bidirectional shift register (SR) serving as an integrator, and a power switch

array with equally sized switches. The output voltage V_{OUT} is regulated per the comparator output, through which the number of the turned-on power switches is digitally tuned with a thermometer code by adding “0s” or “1s” to the bidirectional SR. However, the baseline D-LDO faces the fundamental tradeoffs among transient response speed, output current resolution, and power consumption. As the SR shifts only one count per sampling cycle, a prompt response to the load variation requires a very high sampling frequency f_s , which increases the I_Q proportionally. Therefore, the D-LDOs usually require a large C_{OUT} to handle load transients. Meanwhile, although only one bit of the SR output will be toggled in one cycle in the baseline design, all the clock inputs, and the clock buffers in the long SR consume power in every cycle. Also, the transistor leakage current increases proportionally with the SR length. Therefore, when a long SR length is used for a high output accuracy, the static power increases accordingly.

Asynchronous D-LDOs were proposed to reduce the SR power consumption [13]–[15]. In the asynchronous D-LDO, the clocked comparator is triggered by the output of its pre-stage comparator, eliminating the synchronous clock and thus the SR static power. However, the asynchronous logics are more sensitive to process, voltage, and temperature (PVT) variations, degrading the circuit robustness especially under low supply voltages [19]. In addition, the above-mentioned power and speed tradeoff still exists in the asynchronous D-LDO designs.

To advance the power and speed tradeoff, after a load transient event is detected, coarse/fine-tuning strategies were used to speed up the response process by shifting multiple counts per cycle, or by turning-on/off larger power switches per bit (regarded as coarse tuning) [12], [13], [16], [17]. In steady-state, the fine-tuning loop operates at a lower f_s and provides a higher resolution, with much lower power consumption. Alternatively, multi-bit quantization results can be obtained with a multi-bit ADC [20]–[22] or a time-to-digital converter [23]. Then, the digitized V_{OUT} can operate with binary search control [19], [20], [25] and/or other sophisticated compensation algorithms [21]–[24].

To reduce the SR length while maintaining the output accuracy, a binary code can be used. However, the binary-code control methods may suffer from three drawbacks. First, there might be large V_{OUT} glitches happening during the most significant bit (MSB) code transition, due to the gate-drive buffer delay mismatches. Second, there are more switching activities with the binary-code control than the thermometer-code control, e.g., all the power switches will be toggled during the MSB transition with the binary-code control, which indicates that the thermometer-code control is much more energy efficient. Third, the increased number of bits in the ADC expands the power consumption and the circuit complexity.

Besides, D-LDOs have intrinsic output ripple, also known as limit cycle oscillation (LCO), induced by the inherent quantization error generated by the ADC with a finite resolution. In [26], to prevent a high-mode LCO, an auxiliary power switch, controlled by a feed-forward path, is added in parallel

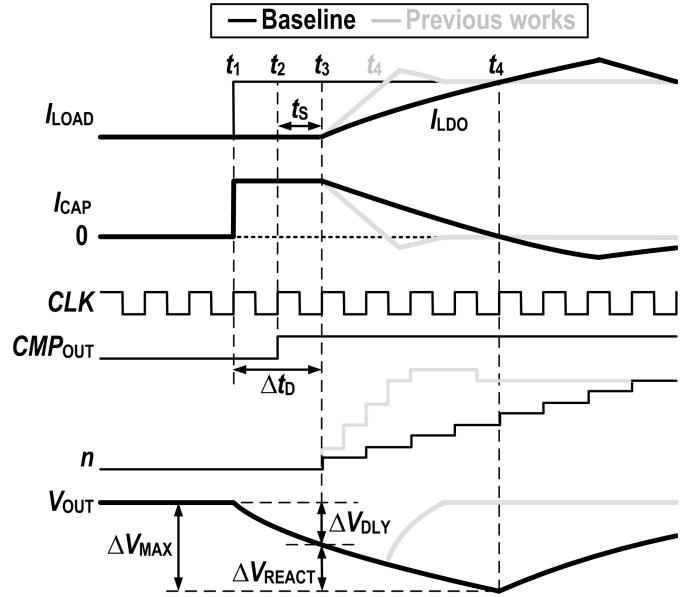


Fig. 3. Voltage undershoot analysis of the previous D-LDO works.

to the main control loop, suppressing the LCO to mode 1 only. In [13], to eliminate the LCO in the asynchronous D-LDO, a freeze mode is enabled by an external command from the load. Alternatively, for the synchronous D-LDO, a dead-zone (DZ) scheme can be used to remove the LCO [27]. However, to reduce the dc error, the size of the DZ should adapt to the PVT variations. Therefore, a tracking-bound method is utilized to minimize LCO under PVT variations in [28].

In this paper, an analog-assisted (AA) loop is added in parallel to the main digital loop, to instantly respond to the load steps without additional power. In addition, a coarse-tuning loop, a fine-tuning loop, together with the AA loop, forms the tri-loop to achieve high accuracy, fast recovery, and low I_Q . To further reduce the I_Q , a freeze mode operation is enabled after the V_{OUT} entered the DZ for a fixed amount of time. Besides, it was found that certain glitches would happen during the carry-in/out operations. A glitch reduction technique with nonlinear coarse word control is proposed to tackle this problem. All the above-mentioned techniques help the proposed D-LDO to be a well-rounded design.

This paper is organized as follows. Section II describes the operation principle of the AA D-LDO. Section III presents the circuit implementations and the design considerations. Section IV exhibits the measurement results and the respective analyses. Then, Section V draws the conclusion.

II. OPERATION PRINCIPLES OF THE ANALOG-ASSISTED D-LDO

A. Transient Response of Conventional D-LDOs

We analyze first the load transient response of the baseline D-LDO design shown in Fig. 2(b). Here, n stands for the number of the turned-on power switches, I_{UNIT} is the unit current provided by one turned-on power switch, the total D-LDO output current $I_{\text{LDO}} = n \times I_{\text{UNIT}}$, and I_{CAP} is the current provided by the output capacitor C_{OUT} . Further, CLK drives

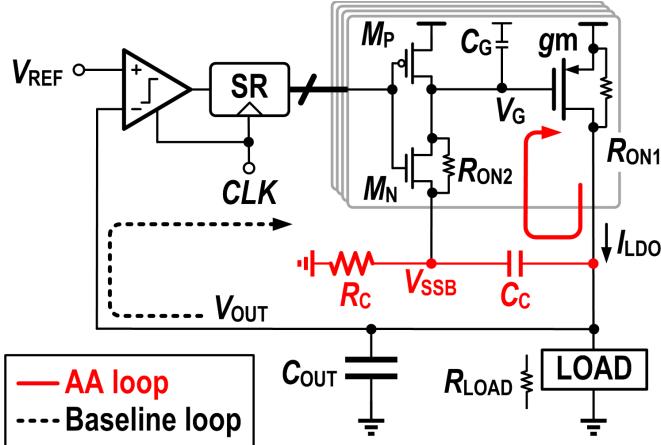


Fig. 4. Topology of the proposed AA D-LDO.

synchronously both the comparator and the SR. Fig. 3 sketches the transient waveforms of the baseline design and the previous works. When the I_{LOAD} steps up at t_1 within a very short transition time, the comparator and the SR cannot react instantly due to the limited f_s and the logic delays. Before the digital loop can react, C_{OUT} keeps being discharged by I_{CAP} which goes to the load. At t_2 (synchronized with the clock rising edge), the comparator output CMP_{OUT} is toggled. And then, the SR begins to shift at t_3 , which is one sampling cycle (t_S) after t_2 . At t_3 , I_{LDO} starts to increase to support I_{LOAD} , and I_{CAP} starts to decrease. After certain sampling cycles, I_{LDO} equals to I_{LOAD} , and the direction of I_{CAP} reverses at t_4 . Then, V_{OUT} stops dropping and starts climbing. Therefore, the maximum V_{OUT} droop (ΔV_{MAX}) is contributed by both ΔV_{DLY} and ΔV_{REACT} , where ΔV_{DLY} is the voltage droop determined by the delay between the load step (t_1) and the SR response (t_3) instants (presented as Δt_D), while ΔV_{REACT} is the voltage droop occurred during the time that the SR needed to shift to a targeted value (from t_3 to t_4). It is found that the maximum Δt_D will be $2 \times t_S$ if the load current step happens right after the clock rising edge. With some typical parameters as an example: $C_{OUT} = 1 \text{ nF}$, $\Delta I_{LOAD} = 10 \text{ mA}/1 \text{ ns}$, and $f_s = 10 \text{ MHz}$, a maximum ΔV_{DLY} of 2 V can happen, not to mention the ΔV_{REACT} .

Therefore, although the coarse-tuning and/or multi-bit quantization techniques used in the previous designs can successfully reduce the ΔV_{REACT} and the recovery time by quickly driving n to the targeted value, those schemes only work after the Δt_D , which still lacks an instant response to the load step and has no effect on reducing ΔV_{DLY} .

B. Operation of the Analog-Assisted D-LDO

Following the above analysis, I_{LDO} needs to react immediately at the transient instant, as ΔV_{DLY} is the limiting factor for reducing ΔV_{OUT} . Therefore, as shown in Fig. 4, an AA D-LDO topology is proposed to eliminate the Δt_D . In this topology, other than the conventional SR loop (dotted line), an AA loop is inserted (solid line). This is achieved by coupling ΔV_{OUT} to V_{SSB} node (V_{SSB}) of the gate-drive inverters through a high-pass network, simply constructed

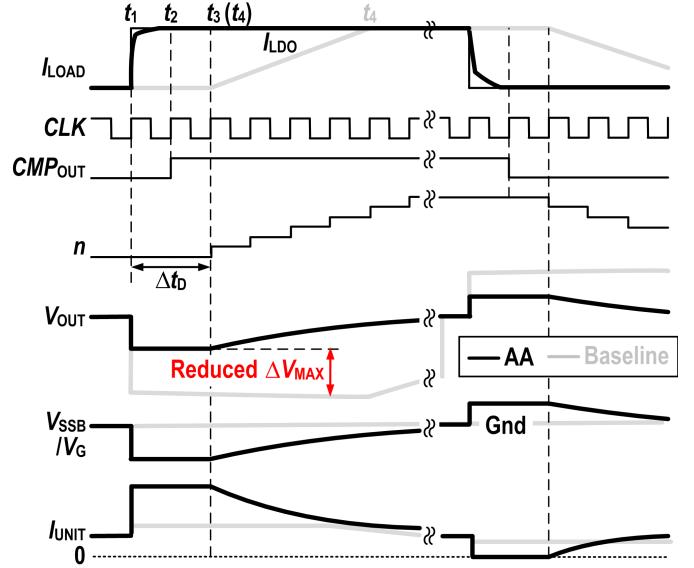


Fig. 5. Conceptual transient waveforms of the proposed AA D-LDO that reduces ΔV_{MAX} .

$$I_{UNIT_NORM} = I_{UNIT} @ V_{OUT_NORM}, I_{UNIT_TEMP} = I_{UNIT} @ V_{OUT_TEMP}$$

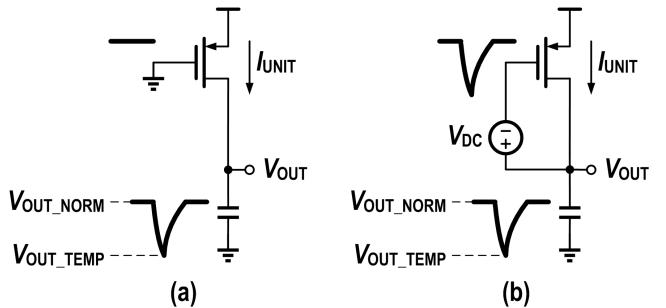


Fig. 6. Equivalent circuits to evaluate the momentary I_{UNIT} with (a) conventional connection and (b) AA loop.

by two passive components C_C and R_C . With this AA loop, V_{SSB} is ac coupled to V_{OUT} and is dc biased to the ground. It is noted that the current spikes from the gate-drive inverters will be filtered by C_C , thus, there is no obvious V_{SSB} fluctuation during switching. Since there is no active circuit introduced, the total I_Q does not increase. Meanwhile, the low-voltage operation merit of the D-LDO is maintained.

Fig. 5 illustrates the load transient response process of this AA D-LDO. When V_{OUT} undershoot/overshot occurs, ΔV_{OUT} is coupled to V_{SSB} and consequently transferred to the gate (V_G) of the turned-on power switches through M_N of the inverters. Therefore, before the digital main loop can respond, V_{GS} and thus I_{UNIT} of the turned-on power switches will be momentarily adjusted. In other words, the high-pass path enables a momentary I_{LDO} to compensate the load step. The V_{OUT} droop is thereby mainly determined by the $I_{UNIT_TEMP}/I_{UNIT_NORM}$ ratio (defined as K), where I_{UNIT_TEMP} and I_{UNIT_NORM} are the temporary and nominal I_{UNIT} values, respectively.

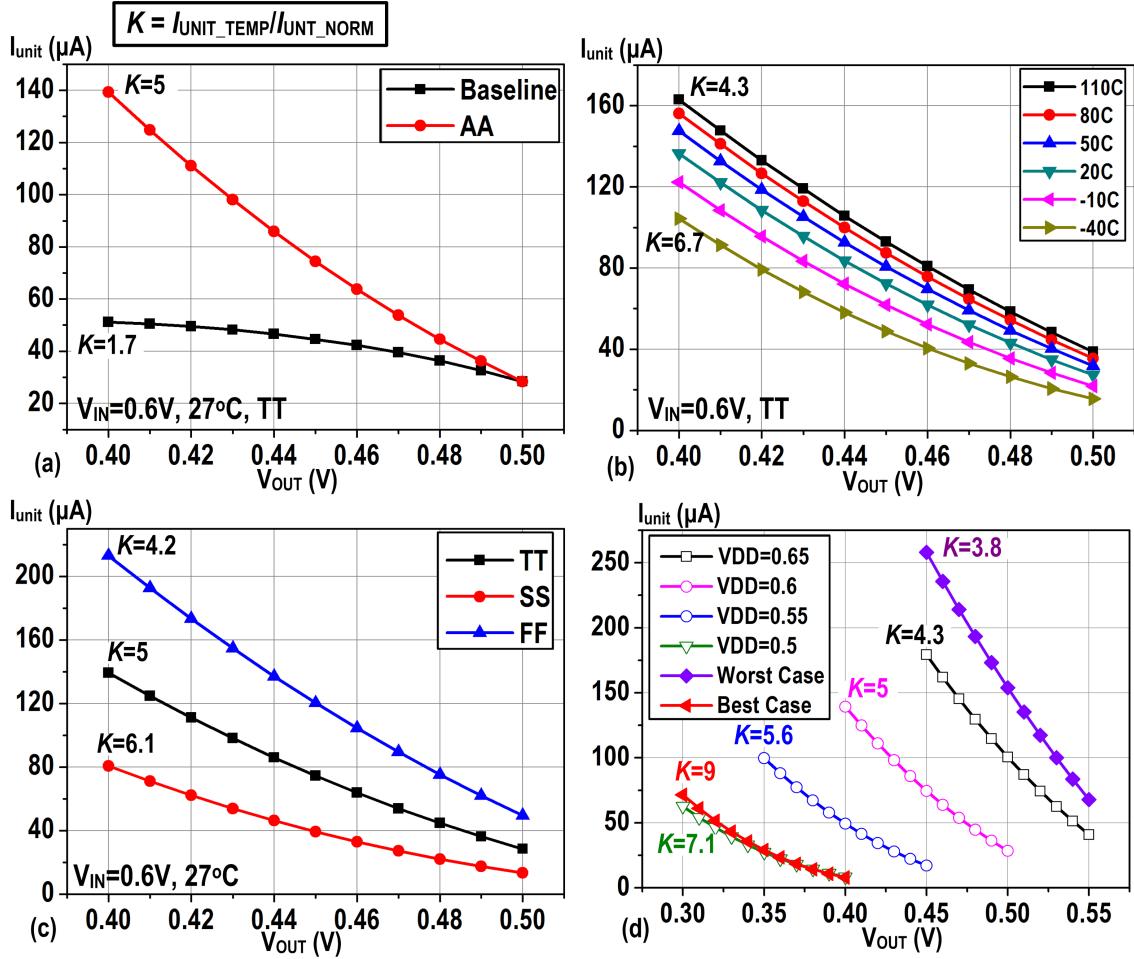


Fig. 7. (a) Simulated I_{UNIT} comparison between the conventional and the AA D-LDOs, when V_{OUT} ranging from 0.4 to 0.5 V with $V_{IN} = 0.6$ V and $V_{REF} = 0.5$ V at 27°C and TT corner. (b) I_{UNIT} of the AA D-LDO with temperature ranging from -40°C to 110°C , with $V_{IN} = 0.6$ V and TT corner. (c) I_{UNIT} of the AA D-LDO with typical, slow, and fast corners, at 27°C and $V_{IN} = 0.6$ V. (d) I_{UNIT} of the AA D-LDO with V_{IN} ranging from 0.5 to 0.65 V at 27°C and TT corner, the worst case with $V_{IN} = 0.65$ V, FF corner and at 110°C , and the best case with $V_{IN} = 0.5$ V, SS corner and at -40°C .

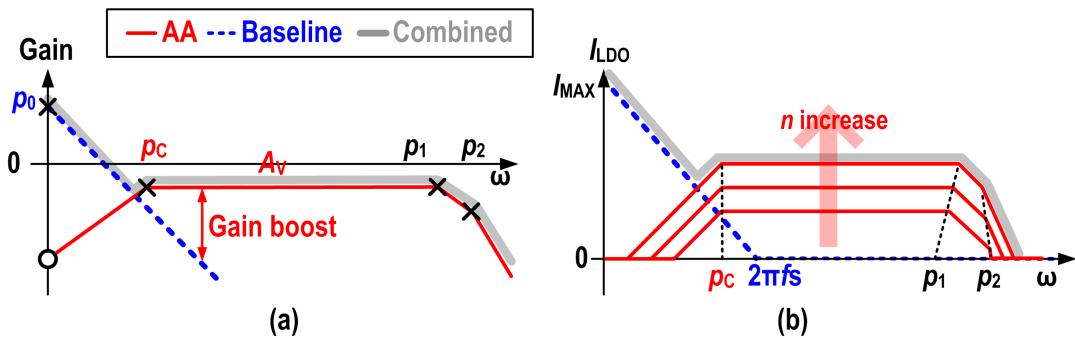


Fig. 8. Frequency responses of (a) loop gains and (b) overall output currents of the conventional loop, the AA loop, and the proposed D-LDO combining these two loops.

To evaluate the maximum I_{UNIT} variations at the transient instant in the AA and the baseline schemes, K is investigated with the equivalent circuit shown in Fig. 6. When V_{OUT} is swept from V_{OUT_NORM} to V_{OUT_TEMP} , only V_{DS} of the power switch changes in the baseline scheme, while both V_{GS} and V_{DS} change in the AA scheme. As shown in Fig. 7(a), with the additional coupled ΔV_{GS} , the AA scheme achieves $K = 5$

with 0.6-V power supply and 0.5-V V_{REF} at 27°C and TT corner. On the contrary, the baseline scheme only achieves $K = 1.7$ in the same circumstance, with the contribution of the V_{DS} variation only. As such, more momentary I_{UNIT} can be delivered with the proposed AA scheme, thus, significantly reducing ΔV_{DLY} . To maintain the same ΔV_{MAX} with the AA scheme, C_{OUT} can be smaller or even eliminated.

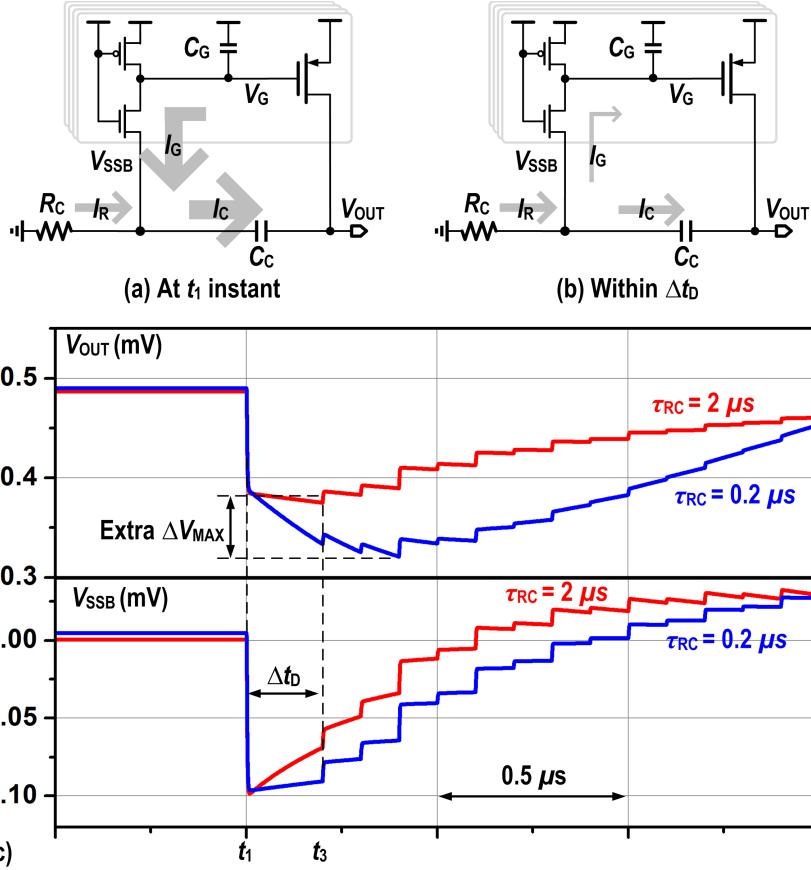


Fig. 9. Current directions (a) at t_1 instant and (b) within Δt_D . (c) Simulated transient waveforms of V_{SSB} and V_{OUT} with 0.2- and 2- μ s high-pass filter time constants.

This output-capacitor-free feature means it sufficiently supports the output-capacitor-less case, but not necessarily. It can also drive a large capacitive load, which will be further discussed in Section II-E.

The I_{UNIT} changing ratio K with the AA loop under PVT variations have also been evaluated as shown in Fig. 7(b)–(d). Fig. 7(b) shows that K decreases from 6.7 to 4.3 when the temperature ranges from -40°C to 110°C , with $V_{IN} = 0.6$ V and TT corner. Fig. 7(c) indicates that a maximum K value of 6.1 is achieved in the SS corner, while it is 4.2 in the FF corner, all at 27°C and $V_{IN} = 0.6$ V. Moreover, Fig. 7(d) shows that K decreases from 7.1 to 4.3 with V_{IN} ranging from 0.5 to 0.65 V, at 27°C and TT corner. And finally, a worst case $K = 3.8$ value is found out with $V_{IN} = 0.65$ V, FF corner and 110°C operation temperature, while a best case $K = 9$ with $V_{IN} = 0.5$ V, SS corner and -40°C operation temperature. In sum, a minimum $K = 3.8$ is achieved within a 100-mV ΔV_{OUT} range, confirming the effectiveness of this scheme under certain PVT variations.

C. Small Signal Analysis

Fig. 8(a) shows the loop gains with the pole and zero locations of the baseline and the proposed regulators. The baseline D-LDO can be modeled as a two-pole system: the SR acts as a discrete-time integrator, and can be modeled as a dc pole p_0 in the s -domain [24], [31], whereas the

second pole $p_1 \approx 1/((R_{ON1}||R_{LOAD}) \cdot C_{OUT})$ is located at the output node. R_{ON1} and R_{LOAD} represent the overall resistances of the turned-on power switch array and the equivalent load resistance, respectively. The delay between the comparator and SR, only introducing phase shift [32], maintains the two-pole magnitude-frequency response of this loop. The parasitic pole p_2 that located at V_G of the power switch array can be neglected since it is far away from the unity gain frequency (UGF). A dc zero z_0 , and a pole $p_C \approx 1/(R_C \cdot C_C)$ has been introduced by the AA loop. Then, the passband voltage gain A_V can be calculated as

$$A_V = n \cdot g_{m_UNIT} \cdot \left(\frac{R_{ON1_UNIT}}{n} || R_{LOAD} \right) \\ = g_{m_UNIT} \cdot (R_{ON1_UNIT} || n R_{LOAD}) \quad (1)$$

where g_{m_UNIT} and R_{ON1_UNIT} are the unit transconductance and on-resistance of one power switch. Since the control word n changes inversely proportional to R_{LOAD} , the product of n and R_{LOAD} can be considered as a constant. Hence, A_V is invariant to load conditions. Although p_1 will shift to low frequency in light load conditions, in this design A_V is smaller than 1 which ensures stability. The AA loop significantly boosts the high frequency gain in the combined loop gain of the proposed D-LDO (bold gray line). Table I summarizes its poles, zero, and gain.

TABLE I
POLES, ZERO, AND GAIN OF THE AA D-LDO

	Value	From
p_0	0	SR
p_1	$1/(R_{ON1} R_{LOAD} \cdot C_{OUT})$	Load
p_2	$1/(R_{ON2} \cdot C_G)$	V_G
p_c	$1/(R_C \cdot C_C)$	AA
z_0	0	AA
A_V	$g_m \cdot (R_{ON1} R_{LOAD})$	AA

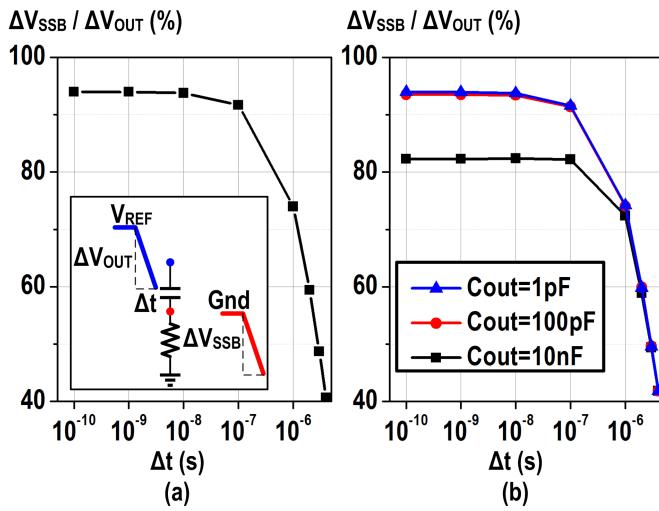


Fig. 10. Simulated ΔV_{OUT} to ΔV_{SSB} transition ratios versus (a) V_{OUT} changing time (Δt) and (b) I_{LOAD} changing time, with $C_{OUT} = 1\text{ pF}$, 100 pF , and 10nF , where $\Delta I_{LOAD} = 10\text{ mA}$.

Fig. 8(b) illustrates the bandpass effects in the I_{LDO} perspective, where more turned-on power switches leads to higher boosting of I_{LDO} . Then, the AA D-LDO would exhibit better load transient performances at larger load conditions.

D. R_C and C_C Selections

To save silicon area, the R_C and C_C values of the high-pass filter should be small. However, its time constant $\tau_{RC} = R_C \cdot C_C$ should be large enough to maintain a low and flat V_{SSB} value during t_D ($0.2\text{ }\mu\text{s}$, if $f_S = 10\text{ MHz}$) to stop the V_{OUT} droop, considering the main digital loop cannot respond instantly and there is no I_{CAP} . As shown in Fig. 9, for $\tau_{RC} = 0.2\text{ }\mu\text{s}$, which is comparable to t_D , V_{SSB} will be charged up quickly by R_C , and V_{OUT} will keep decreasing. Therefore, to ensure a small V_{SSB} variation within Δt_D , we choose $\tau_{RC} = 2\text{ }\mu\text{s}$, which is $10 \times$ larger than Δt_D , implying that the extra ΔV_{MAX} is negligible.

For a given τ_{RC} , a large R_C and a small C_C can be used to save silicon area, as capacitor is relatively more area consuming. However, a small C_C will cause a ΔV_{OUT} to ΔV_{SSB} attenuation due to the capacitor-dividing effect caused by both the power switch gate capacitor C_G and the parasitic capacitors

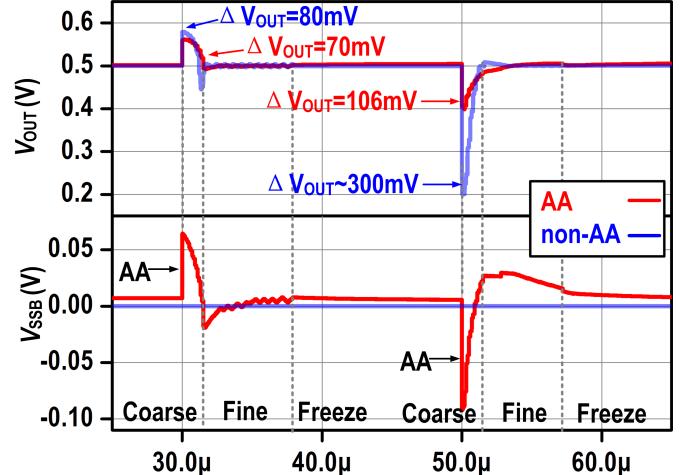


Fig. 11. Simulated transient waveforms comparison between the proposed (AA) and non-AA design, when I_{LOAD} changes from 2 to 12 mA with 1-ns transition time. The proposed design is with $C_C = 100\text{ pF}$ and $C_{OUT} = 0\text{ pF}$, while the non-AA design is with $C_{OUT} = 100\text{ pF}$.

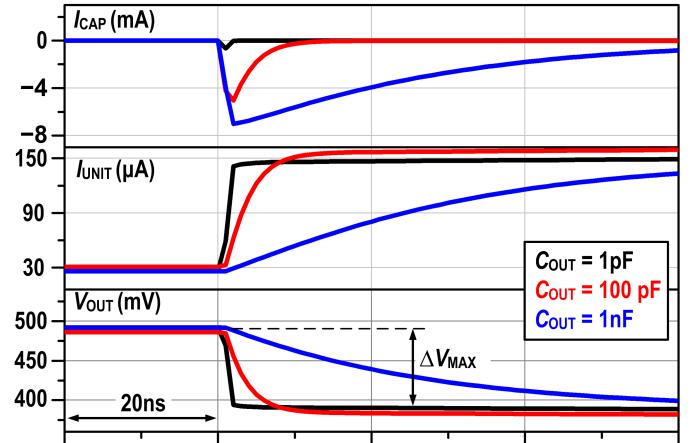


Fig. 12. Simulated load transient waveforms of V_{OUT} , I_{UNIT} , and I_{CAP} , with $C_{OUT} = 1\text{ pF}$, 100 pF , and 1 nF , respectively.

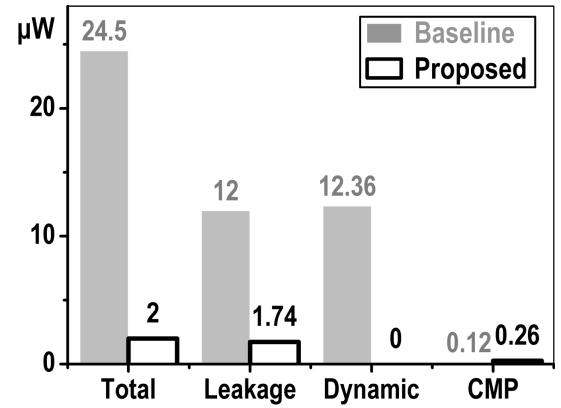


Fig. 13. Power loss breakdowns of the baseline and the proposed designs with $V_{IN} = 0.6\text{ V}$ and $f_S = 10\text{ MHz}$.

C_P at V_{SSB} . Here, C_P derives mainly from the bottom-plate parasitic capacitor of C_C and the parasitic junction capacitors from the inverters. Then, the passband gain A_V is attenuated

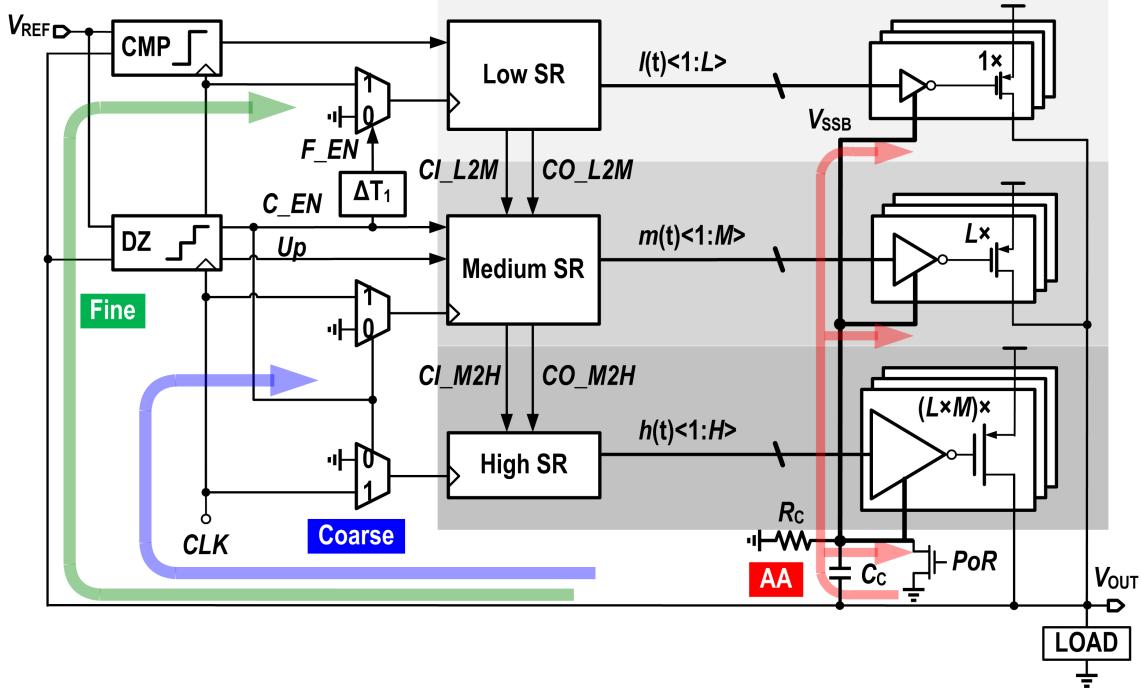


Fig. 14. Full schematic of the proposed AA D-LDO with tri-loop control and carry-in/out.

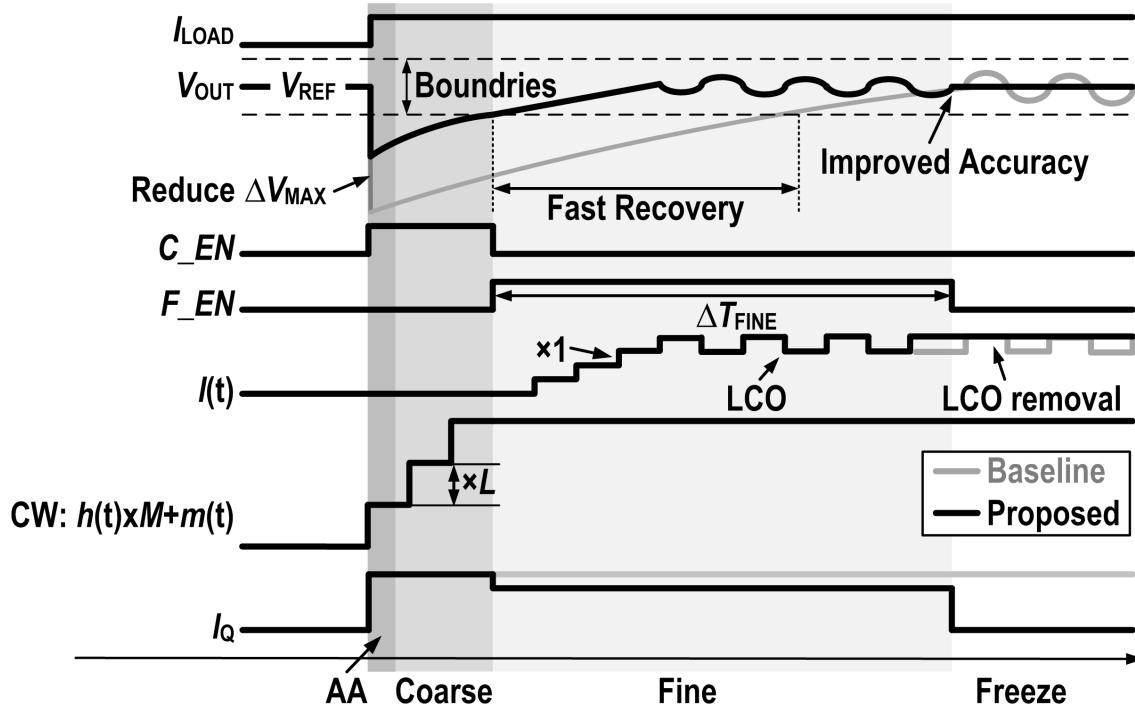


Fig. 15. Conceptual transient waveforms of the tri-loop controlled D-LDO.

by $20 \cdot \log(C_C/(C_C + C_G + C_P))$ (dB). Thus, a C_C of 100 pF is used to make this effect negligible.

The ΔV_{OUT} to ΔV_{SSB} transition ratio is also discussed here. For $\tau_{RC} = 2\mu s$, when V_{OUT} changes much faster than this time constant, ΔV_{OUT} can be considered to be transited to ΔV_{SSB} without attenuation. The simulated ΔV_{OUT} to ΔV_{SSB} transition ratio versus V_{OUT} changing time (Δt) is given

in Fig. 10(a), with the capacitor-dividing effect included. There will be less than 2% transition ratio deviation if V_{OUT} changes within 100 ns.

Fig. 11 presents the simulated V_{OUT} and V_{SSB} transient waveforms comparison between the proposed (AA) and non-AA design, with a 2–12 mA load step and 10-MHz f_S . The proposed design is with $C_C = 100$ pF and $C_{OUT} = 0$ pF,

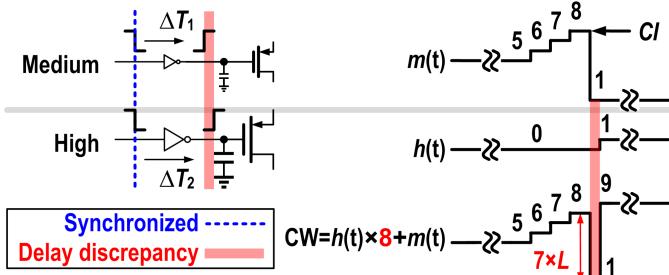


Fig. 16. Glitch is generated when $M = H = 8$, and delay discrepancy is presented.

while the non-AA design is with $C_{OUT} = 100$ pF. A 70-mV overshoot and 106-mV undershoot are achieved with the proposed design, while it is 80 and 300 mV for the non-AA design, indicating the effectiveness of the AA D-LDO scheme and the value selections on R_C and C_C . Also from Fig. 11, the V_{SSB} node only changes with V_{OUT} variations, and will not fluctuate with the current spikes from the gate-drive inverters, because it is clamped by C_C .

E. C_{OUT} Effects on Stability and Transient Response

The C_{OUT} value is non-zero in most applications because the load circuits will contribute parasitic capacitance to C_{OUT} . As mentioned above, although the proposed structure can be output-capacitor-free, it can also drive large load capacitors without any stability concerns for the following reasons. First, the gain of the AA loop A_V is smaller than 1, which is good for the stability. Second, since the transient response performance is mainly determined by the AA loop, the UGF of the digital main loop can be designed with a lower value that guarantees the stability in light load and large C_{OUT} conditions.

For the transient response, a large C_{OUT} will reduce the bandwidth of the AA loop by moving p_1 to a lower frequency, which will smooth the ΔV_{OUT} edge and then reduce the ΔV_{OUT} to ΔV_{SSB} transition ratio. Fig. 10(b) shows the ΔV_{OUT} to ΔV_{SSB} transition ratio versus I_{LOAD} changing time, with $C_{OUT} = 1$ pF, 100 pF, and 10 nF. When C_{OUT} is 1 and 100 pF, the transition ratios almost match to that in Fig. 10(a); while when C_{OUT} is considerably large, the transition ratio is reduced especially for short changing time, which attenuates the desirable momentary I_{UNIT} reaction.

Nonetheless, ΔV_{MAX} will not be increased, as more I_{CAP} can be provided by a larger C_{OUT} . Fig. 12 shows the voltage undershoot waveforms with $C_{OUT} = 1$ pF, 100 pF, and 1 nF, respectively. When $C_{OUT} = 1$ pF, V_{OUT} will drop drastically at the load step instant, where negligible I_{CAP} is provided and ΔV_{MAX} is determined by the momentarily adjusted I_{UNIT} . On the other hand, with an increased C_{OUT} , both V_{OUT} droops and I_{UNIT} adjustment exhibit slower rates, while the larger I_{CAP} maintains the ΔV_{MAX} .

III. IMPLEMENTATION AND DESIGN STRATEGIES

A. Proposed Tri-Loop Architecture

For low-power applications, the quiescent current is one of the major concerns. The baseline D-LDO design that uses a

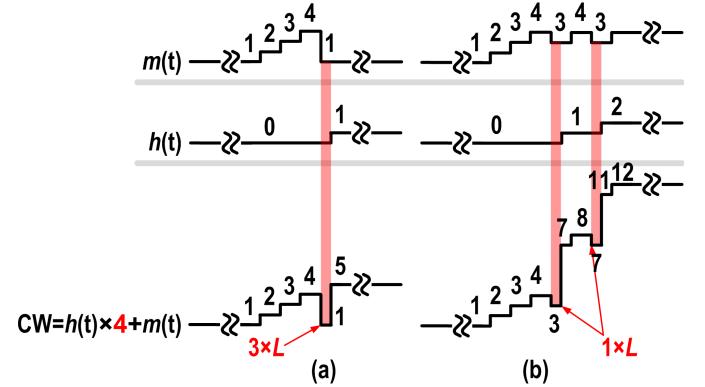


Fig. 17. (a) Possible solution. (b) Proposed nonlinear coarse word control for glitch reduction.

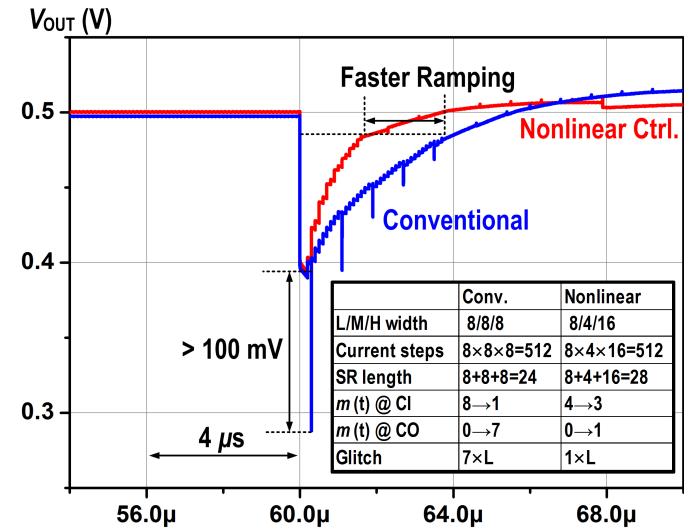


Fig. 18. Simulated V_{OUT} transient waveforms with and without the proposed nonlinear coarse word control scheme for glitch reduction.

long SR length not only gets a slow transient response, but also suffers from large leakage power loss. Fig. 13 shows the simulated power loss breakdown of the baseline and the proposed D-LDOs, with $V_{DD} = 0.6$ V and $f_S = 10$ MHz. For the baseline design, the leakage power loss, proportional to the SR length, accounts for about half of the total power loss.

To address this issue, the power switches in the proposed design are divided into three sub-sections (named “low,” “medium,” and “high”), and each sub-section has one unary power switch array, as illustrated in Fig. 14. The SR lengths in these three sub-sections are L , M , and H , and the corresponding power switch unit sizes are $1 \times$ LSB, $L \times$ LSB, and $(L \times M) \times$ LSB, respectively. Meanwhile, the instant SR values are $l(t)$, $m(t)$, and $h(t)$, respectively. Carry-in (CI_L2M) and carry-out (CO_L2M) operations can be performed between the “low” and “medium” sub-sections, and between the “medium” and “high” sub-sections (using CI_M2H and CO_M2H). To maintain the monotonicity of the output current, the PMOS multiplications in the medium

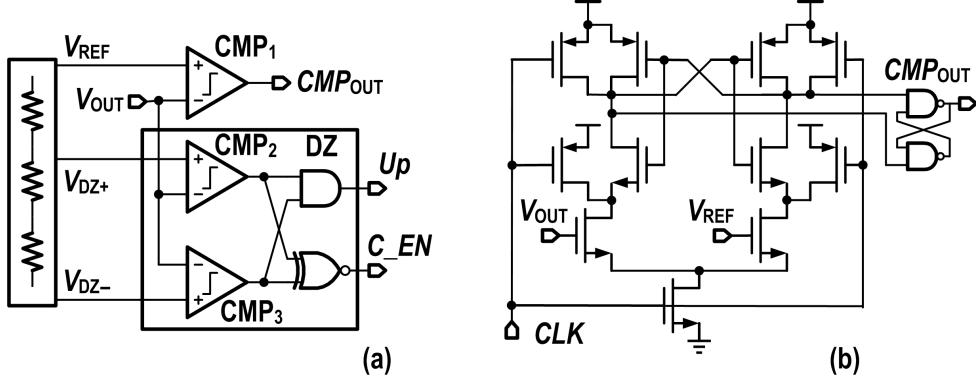


Fig. 19. (a) Block diagram of the DZ control. (b) Schematic of the comparator.

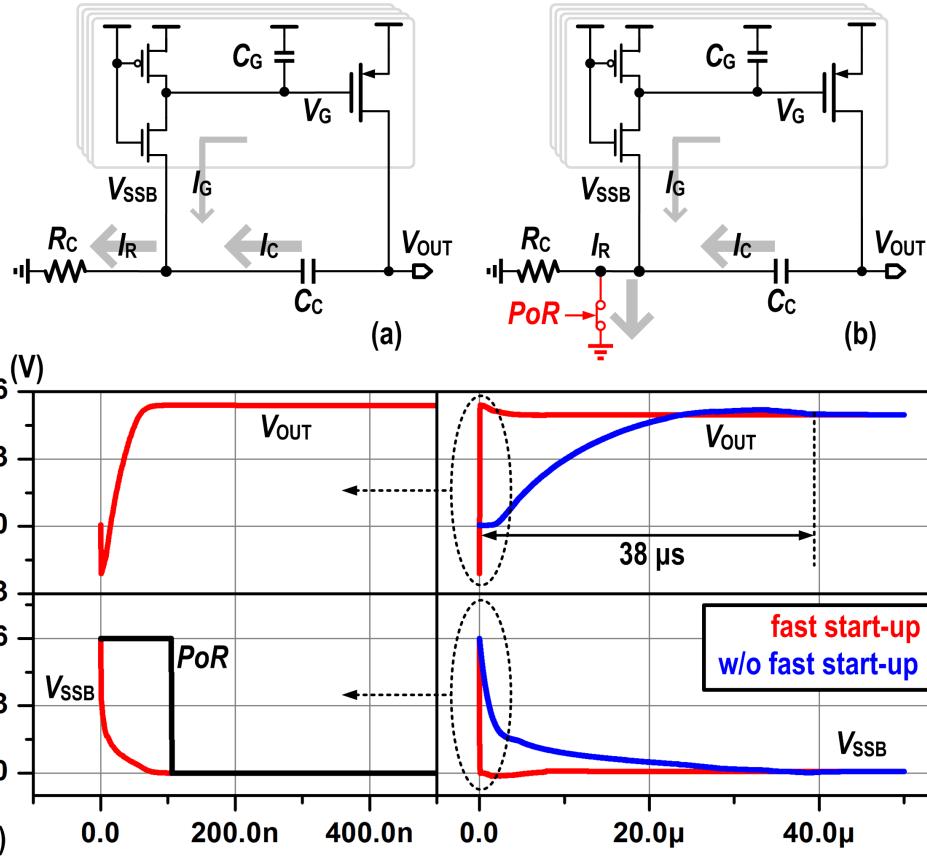


Fig. 20. Current directions of (a) startup and (b) fast startup. (c) Simulated V_{OUT} and V_{SSB} transient waveforms with and without the fast startup scheme, when $V_{OUT} = 0$ and $V_{SSB} = 0.6$ V initially.

and the high sub-sections are achieved with multiple matched fingers, and all the power switches are placed in a switch array in the layout with dummy switches. Thus, the overall 512 current steps can be implemented by using only $L+M+H$ SR bits, and the leakage power loss is significantly reduced from 12 to 1.74 μ W.

The “low” sub-section is controlled by the fine loop, while the “medium” and “high” sub-sections are controlled by the coarse loop. Meanwhile, the AA loop is controlling the V_{SSB} node of all the three sub-sections. The transient waveforms of the tri-loop control scheme are plotted in Fig. 15 and

explained as follows. For the AA loop, all the V_{SS} nodes of the gate-drive inverters are connected to V_{SSB} , and ac coupled to V_{OUT} through the high-pass network. The gate-drive inverters are sized proportional to the power switches that they are driving. As discussed before, this loop reduces ΔV_{MAX} without high f_S and large C_{OUT} . Meanwhile, V_{OUT} is sensed by two DZ comparators for a three-level quantization. When V_{OUT} exceeds the DZ boundaries, C_EN becomes 1 and indicates the coarse-tuning enabled, while Up determines whether the “medium” SR shifts up or down. And the carry-in/out between “medium” and “high” sub-sections allows a

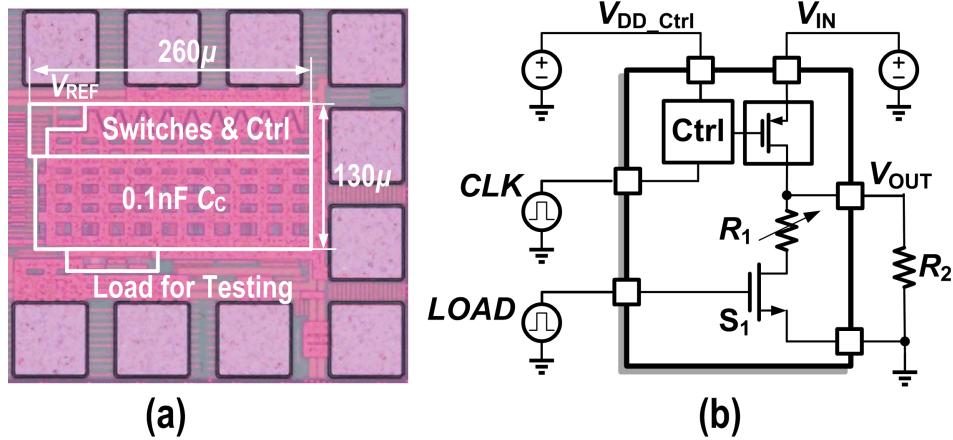


Fig. 21. (a) Chip microphotograph. (b) Measurement setup of the proposed D-LDO.

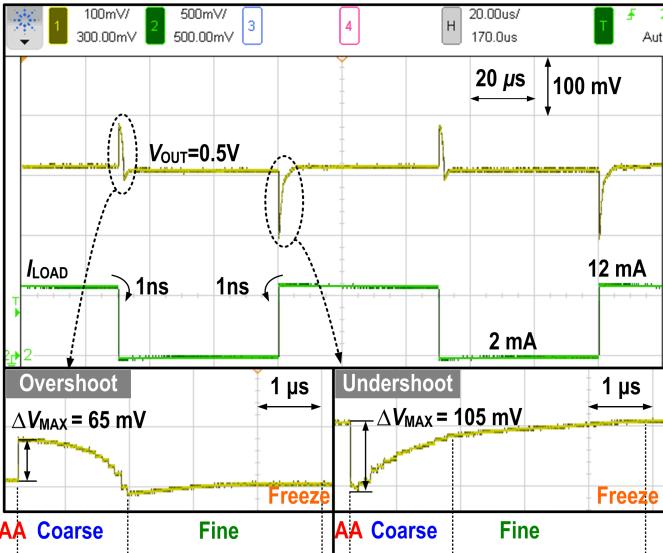
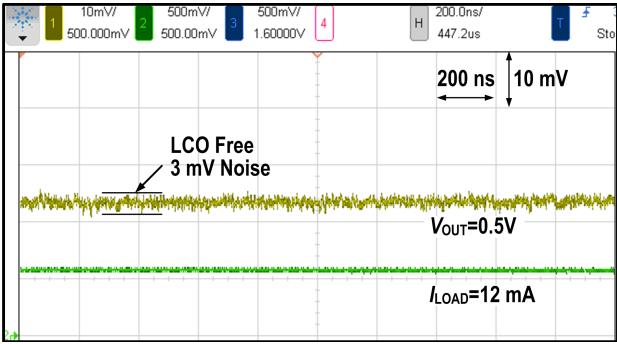
Fig. 22. Measured load transient response with $f_S = 10$ MHz, 2–12 mA load step within 1-ns transition time.

Fig. 23. Measured steady-state output voltage.

maximum $H \times M$ coarse current steps, each weighs $L \times \text{LSB}$. A coarse control word $\text{CW} = h(t) \times M + m(t)$ is utilized to indicate the instant number of turned-on coarse power MOS, while the overall control word equals to $\text{CW} \times L + l(t)$. In coarse tuning, CW will shift 1 count per clock cycle, which is equivalent to L counts shift for the overall control

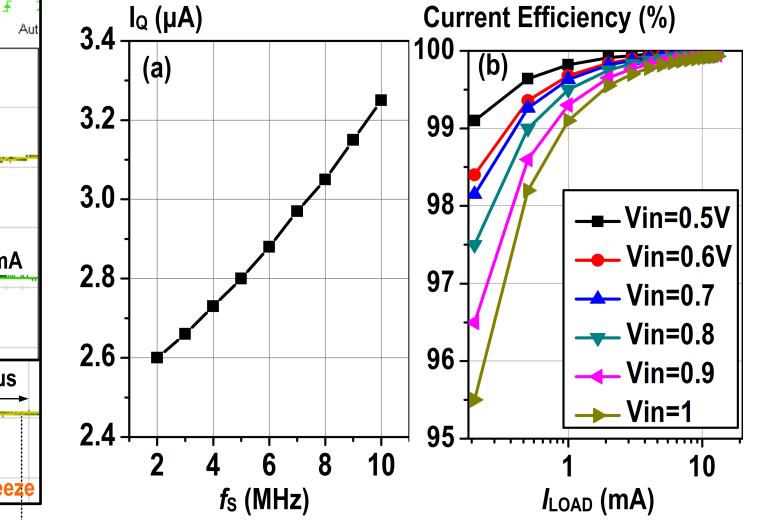


Fig. 24. Measured (a) quiescent current versus sampling frequency and (b) current efficiency versus loading current.

word. This drives V_{OUT} quickly back to the preset boundaries, and thus reducing the recovery time. When V_{OUT} is pulled within the boundaries, the coarse-tuning is terminated while the fine tuning is activated. Then, the overall control word shifts 1 LSB per cycle, regulating V_{OUT} to V_{REF} slowly but with improved output accuracy. To remove LCO, the fine-tuning terminates after a ΔT_{FINE} duration, and a freeze mode is enabled afterward. Subsequently, all the flip-flops stop with the clock-gating technique, thereby removing LCO and the dynamic power losses. The remaining active components in the freeze mode are the DZ comparators that wake up the D-LDO. Since the AA scheme allows the utilization of a low frequency clock (10 MHz), the two additional comparators only consume a small amount of power ($0.26 \mu\text{W}$). Therefore, the overall power loss is reduced from 24.5 to $2 \mu\text{W}$, as given in Fig. 12.

B. L, M, H Value Selections and Glitch Reduction

For the selection of the L, M, H values, it is straightforward to have $L = M = H = (512)^{1/3} = 8$ to achieve the minimum total SR length and thus the smallest leakage power

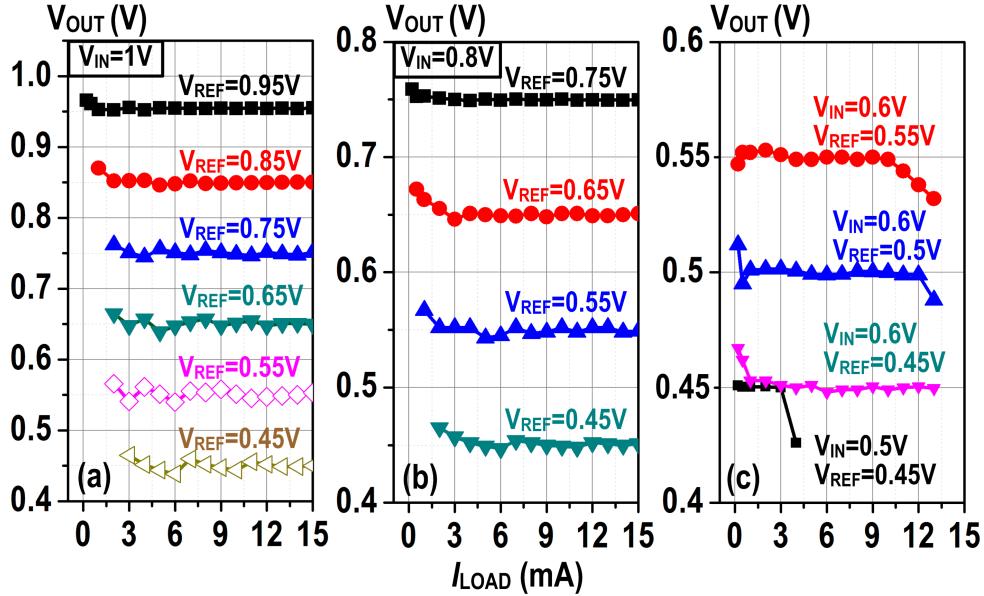


Fig. 25. Measured load regulations when (a) $V_{IN} = 1\text{ V}$, (b) $V_{IN} = 0.8\text{ V}$, and (c) $V_{IN} = 0.6$ and 0.5 V .

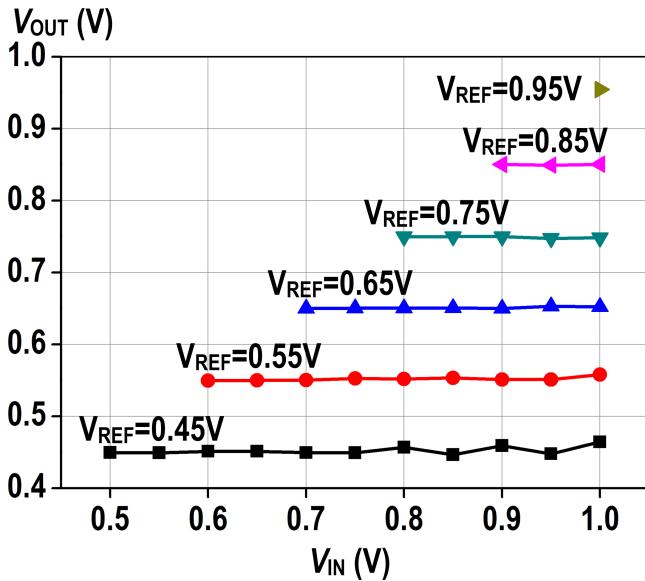


Fig. 26. Measured line regulations.

loss. However, a significant glitch issue may occur with this scheme, which is caused by the delay discrepancy of the gate-drive inverters between the “medium” and the “high” sub-sections, as illustrated in Fig. 16. For an ideal carry-in operation, when $m(t)$ reaches 8, it will be reset to 1 while $h(t)$ will add 1 to itself to achieve an 8-to-9 transition. Nevertheless, with the delay discrepancy, which stems from the different delay time ($\Delta T_1 \neq \Delta T_2$) between the inverters output signals although their inputs are synchronized, the add 1 of $h(t)$ typically lags from the reset of $m(t)$, making an 8-to-1-to-9 actual transition and thus a large glitch with a current strength of $7 \times L \times \text{LSB}$.

To reduce such a glitch, a possible solution is to reduce the “medium” SR length, e.g., $M = 4$ and $H = 16$. This keeps $M \times H$ constant to maintain the required resolution, while increases the total SR length only by 4. In this solution, the

carry-in operation takes place when $m(t) = 4$, by resetting $m(t)$ to 1 and adding 1 to $h(t)$, as shown in Fig. 17(a). Then, a 4-to-1-to-5 transition ($3 \times L$ glitch) may occur, which is still not favorable. An even smaller M value, although results in a smaller glitch, is not applicable due to the exponential increment in the total SR length.

To further reduce the glitch, a nonlinear coarse word control scheme, based on $M = 4$ and $H = 16$, is proposed to minimize the glitch as shown in Fig. 17(b). For the carry-in operation, $m(t)$ will be reset to 3 instead of 1, making a 4-to-3-to-7 transition and only $1 \times L$ glitch. Similarly, $m(t)$ will be set to 1 instead of 3 for carry out. Furthermore, this scheme also leads to a faster ramping of the coarse word. The simulated V_{OUT} undershoot with and without the nonlinear coarse word control is given in Fig. 18, showing that the glitch is reduced by more than 100 mV, and a 2- μs faster recovery time. The glitch reduction performances and comparison are also summarized in Fig. 17.

C. Comparators and Shift Registers

The block diagram of the DZ control is given in Fig. 19(a). A resistor ladder is used to generate V_{REF} and the DZ boundaries (V_{DZ+} and V_{DZ-}). All the comparators are using the same topology from Fig. 19(b), where a latch stores the output signal. When CLK is low, the internal nodes of the first stage will be pre-charged to a high voltage without changing the output of the NAND-type latch. When CLK is high, the comparing operation is executed. The clocked comparator reduces the static current consumption, and allows low operation voltages as all the transistors are fully turned-on/off, requiring no voltage headroom.

Here, the bidirectional SR is similar to that in [10], where D-type flip-flops and multiplexers are used. Set and reset functions have been added to each SR bit to easily enable the nonlinear coarse word control scheme. In addition, the sampling clock of all sub-sections can be gated to save the quiescent current.

TABLE II
COMPARISONS WITH THE STATE-OF-THE-ART WORKS

	[12] 2016	[16] 2016	[21] 2016	[11] 2017	[25] 2017	[30] 2017	This work
Process	130nm	65nm	65nm	28nm	65nm	65nm	65nm
Area [mm ²]	0.355	0.1	0.029	0.021	0.076***	0.016	0.034
Type	Digital	Digital	Digital	Digital	Digital	Analog	Digital
Architecture	SR Based	SR based	ADC Based	SR Based	SAR/PD	N.A.	SR+AA
V _{IN} [V]	0.5-1.2	0.6-1.1	0.5-1	1.1	0.5-1	0.6	0.5-1
V _{OUT} [V]	0.45-1.14	0.4-1	0.45-0.95	0.9	0.3-0.45	0.3-0.55	0.45-0.95
Max. f _S [MHz]	400	500	200	N.A.	240	N.A.	10
Min. I _Q [μ A]	24	82	12.5	110	14	32	3.2
Resolution / SR bits	7bit/128	10bit/96	N.A.	6.6bit/25	N.A.	N.A.	9bit/28
C _{TOT} * [nF]	1	1	0.4	23.5	0.4	0.04	0.1
ΔI_{LOAD} [mA]	1.4	98	0.4	180	1.06	10	10
ΔV_{OUT} [mV]	90	55	40	120	40	133.9	105
I _{LOAD} Trans. T [ns]	N.A.	20	N.A.	4000	1	150	1
FOM** [ps]	76.5	0.45	1.11	7.75	56	1.7	0.23

* The total capacitance C_{TOT} includes C_{OUT} and C_C , where $C_{OUT} = 0$ and $C_C = 0.1$ nF in this work.

** FOM = $C_{TOT} \Delta V_{OUT} I_Q / I_{MAX}^2$ [33].

*** Including the active area and on-chip 0.4nF capacitor.

D. Fast Startup

The AA scheme may have a slow startup, if V_{OUT} is low and V_{SSB} has a positive initial value, e.g., $V_{OUT} = 0$ and $V_{SSB} = 0.6$ V. As shown in Fig. 20(a), the possible initial charge on C_G needs to be discharged through R_C , which is, however, a high impedance path. This can be solved by adding a power-on-reset (*PoR*) switch to V_{SSB} by passing R_C , as shown in Fig. 20(b). This switch, controlled by a *PoR* signal, also resets all the SRs in the D-LDO during power on. The simulated waveforms of V_{SSB} and V_{OUT} with and without the fast startup scheme are given in Fig. 20(c), in which a clear improvement on startup speed can be observed.

IV. MEASUREMENT RESULTS

The proposed D-LDO was fabricated in a 65-nm general purpose CMOS process with an effective area of 0.034 mm², excluding the pads and load circuits for testing. The chip microphotograph is given in Fig. 21(a). In this prototype, the 100-pF C_C consumes about 60% silicon area. A larger C_C here will make little improvement on the gain of the passband, since the above-mentioned capacitor-dividing effect is now negligible. A smaller C_C may be used when the area budget is low, sacrificing the transient performance. The measurement setup is shown in Fig. 21(b), where an on-chip resistor R_1 is connected in series with a switch S_1 that is driven by an on-chip buffer. The light load current is set by an off-chip resistor R_2 . The measured load transient response to the load steps of 2–12 mA with 1-ns transition time is shown in Fig. 22. With $V_{IN} = 0.6$ V, $V_{OUT} = 0.5$ V, $f_S = 10$ MHz, $C_C = 100$ pF, and $C_{OUT} = 0$ pF, we measured a 65-mV voltage overshoot and a 105-mV undershoot, which is mainly contributed by

the AA loop. No significant glitch is observed due to the proposed nonlinear coarse word control. The zoom-in steady-state output voltage is shown in Fig. 23, where no LCO is found because of the freeze mode scheme. Only 3-mVpp output noise, which mainly comes from the measurement equipment, is observed.

The measured quiescent current versus the sampling frequency is given in Fig. 24(a), where a 3.2 μ A is measured at $f_S = 10$ MHz. This confirms the effectiveness of the power reduction scheme of the three-sub-section division, as well as the freeze mode scheme. Fig. 24(b) shows the current efficiencies versus loading current under different input voltages, and a minimum 95.5% current efficiency is achieved.

This design manages to work with 0.5–1 V V_{IN} , 0.45–0.95 V V_{OUT} , and the load current range is from 0.2 to 13 mA in the nominal condition ($V_{IN} = 0.6$ V, $V_{OUT} = 0.5$ V). The measured load regulations have been given in Fig. 25, with loading current ranging from 0.2 to 13 mA, at $V_{IN} = 0.5$, 0.6, 0.8, and 1 V, respectively. The maximum load regulation is 2.3 mV/mA. Moreover, the measured line regulations have been presented in Fig. 26, and a maximum line regulation of 30 mV/V was observed.

Table II compares the performances of the proposed D-LDO with the state-of-the-art works, including both the A-LDOs and D-LDOs. With the AA loop, this paper achieved a reasonable (105 mV) output voltage undershoot responding to a 2–12 mA load step within the shortest transition time (1 ns), using the lowest sampling frequency (10 MHz), and the smallest total capacitance ($C_C + C_{OUT} = 0.1$ nF) among the state-of-the-art D-LDO works. Additionally, the three-sub-section division and the carry-in/-out operations realize

a 9-bit resolution (512 current steps) using only 28-SR bits, which significantly reduces the leakage power loss. Moreover, the dynamic power loss is removed by the freeze mode. Therefore, a low-quiescent current of $3.2 \mu\text{A}$ is realized. By applying the widely adopted figure-of-merit (FOM) of speed [33] for comparison, an FOM of 0.23 ps is achieved.

V. CONCLUSION

Digital LDO can operate at low input voltages and scale with processes. However, its response time is highly related to the sampling frequency and therefore the power consumption, which is the fundamental tradeoff in LDO designs. In this paper, an AA loop was inserted into the D-LDO to provide a momentary I_{UNIT} adjustment at the load transient instants without additional power consumption, which significantly reduces the output voltage undershoot and overshoot. Additionally, all the power switches are divided into three sub-sections with the DZ boundaries and the carry-in/out operations, controlled by three loops. This scheme reduces the total SR length and thus the transistor leakage power loss, and improves the recovery time and output accuracy. The freeze mode operation is employed to remove the LCO, and to further reduce the quiescent current, without sacrificing the transient response. Moreover, a nonlinear coarse word control scheme is proposed not only to reduce the output glitches, but also to further improve the recovery time. Hence, all these proposed/employed schemes combined lead the comprehensive D-LDO design to a 0.23-ps FOM of speed.

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Dr. Lu served as a Technical Program Committee Member of several IEEE conferences and a reviewer for many journals/conferences. He was a recipient of the Outstanding Postgraduate Student Award of Guangdong (Canton) Province 2008, the IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award 2013–2014, and the IEEE CAS Society Outstanding Young Author Award 2017.



Seng-Pan U (Ben) (S'94–M'00–SM'05–F'16) received the B.Sc. and M.Sc. degrees in 1991 and 1997, respectively, and the dual Ph.D. (Hons.) degrees in high-speed analog IC design from the University of Macau (UM), Macau, China, and the Instituto Superior Técnico (IST), Lisbon, Portugal, in 2002 and 2014, respectively.

From 1999 to 2001, he was a Visiting Research Fellow with the Integrated CAS Group, Center of Microsystems, IST, Lisbon. In 2001, he co-founded the Chipidea Microelectronics (Macau) Ltd., Macau, as the Engineering Director, and since 2003, he has been the Corporate VP-IP Operations Asia Pacific for devoting in advanced Analog and Mixed-Signal (AMS) Semiconductor IP product development. The company was acquired in 2009 by the world leading EDA & IP provider Synopsys Inc. (NASDAQ: SNPS), currently as Synopsys Macau Ltd. Since 1994, he has been with the Faculty of Science and Technology, UM, where he is currently a Professor and the Deputy Director of the State-Key Laboratory of AMS VLSI. He is also the Corporate Senior Analog and Mixed-Signal Design Manager and a Site General Manager with Synopsis Macau. He has authored or co-authored more than 140 publications, four books (Springer and China Science Press) in the area of VHF SC filters, analog baseband for multistandard wireless transceivers, and very high-speed TI ADCs. He co-holds ten U.S. patents.

Dr. U received approximately 30 research and academic/teaching awards. He was a co-recipient of the 2014 ESSCIRC Best Paper Award. He is also the Advisor for approximately 30 various international student paper award recipients, such as the SSCS Pre-Doctoral Achievement Award, the ISSCC Silk-Road Award, the A-SSCC Student Design Contest, the IEEE DAC/ISSCC Student Design Contest, ISCAS, MWSCAS, and PRIME. He was a recipient of the 2012 IEEE SSCS Outstanding Chapter Award as the Macau Founding Chairman. He received the Science and Technology (S&T) Innovation Award of the Ho Leung Ho Lee Foundation in 2010, and also the State S&T Progress Award in 2011. He also received both the 2012 and 2014 Macau S&T Invention and Progress Awards. In recognition of his contribution in academic research and industrial development, he received the Honorary Title of Value in 2010 by the Macau SAR Government. He was also elected as the "Scientific Chinese of the Year 2012." He is the Founding Chairman of the IEEE SSCS and the Chairman of the CAS/COM Macau Chapter. He is appointed a member of the S&T Commission of China Ministry of Education. He was the IEEE SSCS Distinguished Lecturer 2014–2015 and the A-SSCC 2013 Tutorial Speaker. He has also been a reviewer of various IEEE journals, such as the IEEE JSSC, the IEEE TCAS, and the IEEE TVLSI. He was the Program Committee/Chair of the IEEJ AVLSIWS, the IEEE APCCAS, ICICS, PRIMEAsia, and the IEEE ASP-DAC'16. He is currently a TPC Member of ISSCC, A-SSCC, and RFIT, and the Analog Subcommittee Chair of VLSI-DAT. He is also an Editorial Board Member of the Journal AICSP.



Rui P. Martins (M'88–SM'99–F'08) was born in 1957. He received the bachelor's, master's, Ph.D. degrees, and the Habilitation for Full-Professor in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), TU of Lisbon, Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively.

He has been with the Department of Electrical and Computer Engineering/IST, TU of Lisbon, since 1980. Since 1992, he has been on leave from IST, TU of Lisbon (now University of Lisbon since 2013), and is with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macau, China, where he is currently a Chair-Professor since 2013. In FST, he was the Dean of the Faculty from 1994 to 1997 and he has been the Vice-Rector of the UM since 1997. From 2008, after the reform of the UM Charter, he was nominated after open international recruitment and reappointed in 2013 as the Vice-Rector (Research) until 2018. Within the scope of his teaching and research activities, he has taught 21 bachelor's and master's courses and, in UM, has supervised (or co-supervised) 40 theses, Ph.D. (19), and master's (21). He was a Co-Founder of Chipidea Microelectronics, Macao, (now Synopsys) from 2001 to 2002, and in 2003, he created the Analog and Mixed-Signal VLSI Research Laboratory, UM, elevated in 2011 to the State Key Laboratory of China (the first in engineering in Macao), being its Founding Director. He has co-authored six books, 12 book chapters, 400 papers, in scientific journals (126) and in conference proceedings (274),

and other 62 academic works, in a total of 505 publications, and holds 25 patents, USA (23) and Taiwan (2).

Dr. Martins was a recipient of two government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999, and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001. He received the IEEE Council on Electronic Design Automation Outstanding Service Award 2016. He was the Founding Chairman of both the IEEE Macau Section from 2003 to 2005 and the IEEE Macau Joint-Chapter on Circuits and Systems (CAS)/Communications from 2005 to 2008 [2009 World Chapter of the Year of IEEE CAS Society (CASS)]. He was the General Chair of the 2008 IEEE Asia-Pacific Conference on CAS, and was the Vice President for Region 10 (Asia, Australia, and the Pacific) of IEEE CASS from 2009 to 2011. He was the Vice President (World) Regional Activities and Membership of the IEEE CASS from 2012 to 2013, and an Associate Editor of the IEEE TRANSACTIONS ON CAS II: EXPRESS BRIEFS from 2010 to 2013, nominated a Best Associate Editor of T-CAS II for 2012–2013. He was a member of the IEEE CASS Fellow Evaluation Committee from 2013 to 2014, and the CAS Society Representative in the Nominating Committee, for the election in 2014, of the Division I (CASS/EDS/SSCS)—the Director of the IEEE. He was the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference—ASP-DAC'2016. He was a Nominations Committee Member of the IEEE CASS in 2016 and is currently the Chair of the IEEE CASS Fellow Evaluation Committee (Class 2018). In 2010, he was elected, unanimously, as a Corresponding Member of the Portuguese Academy of Sciences, Lisbon, being the only Portuguese Academician living in Asia.