Super Class-AB Recycling Folded Cascode OTA

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***Abstract*— A super class-AB version of the recycling folded cascode (RFC) operational transconductance amplifier (OTA) is proposed. The use of an adaptive bias circuit for the input differential pair provides dynamic current boosting and increased gain-bandwidth product (GBW). Moreover, use of local common-mode feedback (LCMFB) at the load of the differential pair further improves these performance parameters and provides high current efficiency. Measurement results of a test chip prototype fabricated in a 0.5-μm CMOS process show an increase in slew rate and GBW by a factor of 34 and 3, respectively, versus the conventional RFC OTA using the same supply voltage and bias currents. Overhead in other performance metrics is small.**

***Index Terms*— Amplifiers, analog integrated circuits, class-AB circuits, CMOS integrated circuits, folded cascode (FC) amplifier.**

I. Introduction

THE operational transconductance amplifier (OTA) is a basic building block in several analog and mixed-signal integrated circuits. The continuously growing market of mobile and portable electronic devices and the evolution of CMOS technologies have made the OTA a critical design analog block in many systems, in terms of overall power consumption and performance. Many applications rely on the availability of high-gain wideband OTAs operating with the low supply voltage and power requirements demanded by modern CMOS processes in these scenarios.

One of the most widely used architectures either as single-stage amplifier or as the first stage of a multi-stage topology, is the folded cascode (FC) OTA. Its popularity comes from a good tradeoff between gain and signal swing. The PMOS input FC OTA has become the preferred choice over the NMOS input version due to its lower flicker noise, higher non-dominant poles, and lower input common-mode level compatible with single NMOS switches in switched-capacitor (SC) applications [1], [2].

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Despite the advantages of the FC OTA, it is not well suited to the current demand of achieving the highest performance with the lowest power consumption. This is mainly due to the current sources employed at the folding stage, which drive the largest currents without providing any transconductance to the OTA [2] and limit the slew rate (SR). Several approaches have been reported to address this issue and hence to improve the performance of the FC OTA, which basically rely on replacing these current sources by active current mirrors. Thus, multi-path schemes have been proposed [3], [4]. However, they lead to complex architectures with extra low-frequency pole–zero pairs, which can be a limiting factor in high-frequency applications. Another approach was presented in [2] coined as recycling FC (RFC) OTA, improving both gain-bandwidth product (GBW) and SR. Further refinements to the RFC OTA were proposed in [5]–[7], adding extra dc current sources or active current mirrors. However, all these techniques have limited power efficiency since the active current mirrors employed lead to internal replication of large dynamic currents at the additional branches [8]. Moreover, SR is improved by using scaled current mirrors, which also scale quiescent current by the same factor and hence static power.

A power-efficient approach to get class-AB amplifiers was proposed in [8]. It allows large dynamic currents not limited by the quiescent currents and (to a first-order approach) proportional to V_{id}^4, with V_{id} the differential input voltage. Since dynamic currents in conventional class-AB differential amplifiers are often proportional to V_{id}^2, the OTAs proposed in [8] were coined as "super" class-AB OTAs. Besides very large SR, the most salient feature of super class-AB OTAs is that they exhibit high power efficiency since they are single-stage topologies where large dynamic currents are generated directly at the output transistors, without internal replication (apart from the unavoidable replication at the output current mirror for single-ended outputs). However, super class-AB techniques (and hence their inherent advantages) have been restricted so far to the current mirror OTA architecture. In this paper, we propose to extend these techniques to the RFC OTA, thus combining the benefits of both approaches.

The organization of this paper is as follows. In Section II, the FC and RFC OTAs are briefly described, and the principle of operation of the proposed super class-AB RFC OTA is presented. The small-signal and large-signal performances of the super class-AB RFC OTA are analyzed in Sections III and IV, respectively. Fully differential (FD) versions are discussed in Section V and a design methodology

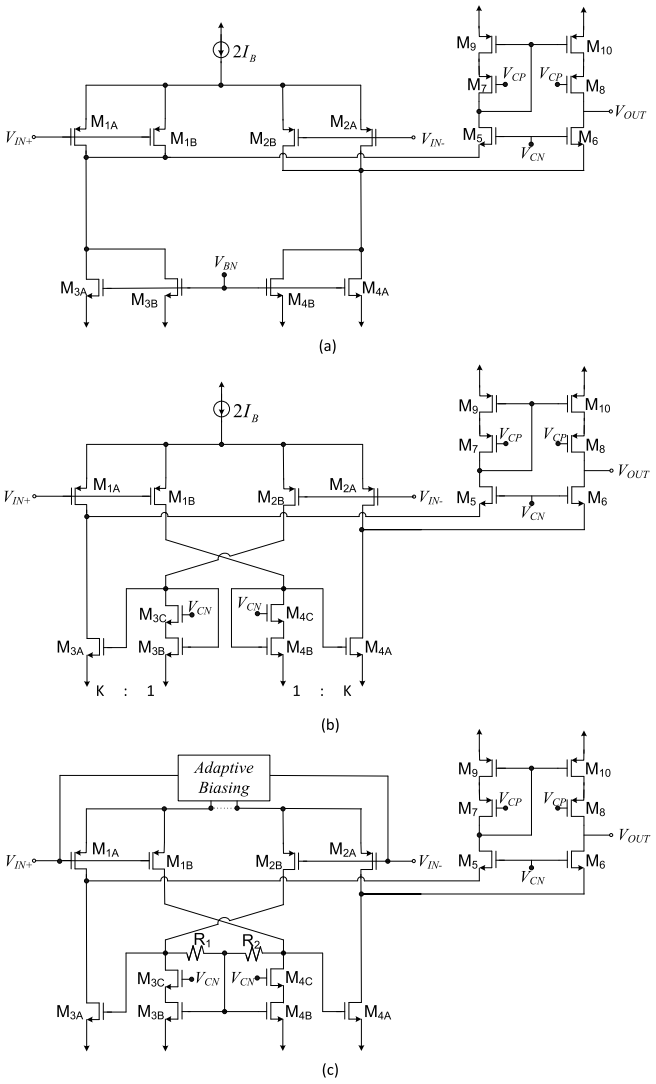

Fig. 1. (a) FC OTA. (b) RFC OTA. (c) Super class-AB RFC OTA.

is outlined in Section VI. Measurement results of the FC, RFC, and super class-AB RFC OTAs are presented in Section VII.

II. Principle of Operation

The conventional (class A) PMOS-input FC OTA is shown in Fig. 1(a). Note that the differential pair transistors M_1–M_2 have been split into two identical transistors (M_{1A}–M_{1B} and M_{2A}–M_{2B}). The same has been done with the current sources M_3 and M_4 at the folding stage (split into M_{3A}–M_{3B} and M_{4A}–M_{4B}). This has been done just to ease comparison with the other topologies described in this section. The differential pair bias current source $2I_B$ provides a quiescent current $I_B/2$ to M_{1A}, M_{1B}, M_{2A}, and M_{2B}. If each pair of current sources at the folding stage (M_{3A}–M_{3B} and M_{4A}–M_{4B}) provides a dc current $2I_B$, then the remaining transistors M_5–M_{10} are biased with a current I_B.

Fig. 1(b) shows the PMOS-input RFC OTA [2]. It is designed by replacing the current sources at the folding stage by active current mirrors with current ratio $1{:}K$, and reconnecting the differential pair transistors. Note that if factor $K = 3$, power consumption is the same as for the FC OTA of Fig. 1(a). Transistors M_{3C}–M_{4C} are included to improve accuracy of the current mirrors. This arrangement increases the transconductance, GBW, and SR of the OTA without the need to increase current consumption, since folding is made by active current mirrors with current gain K which scale the signal currents generated by the differential pair. The conventional FC OTA requires a large dc current just to invert (fold) the differential pair signal current, without providing current gain and thus wasting static power. Note also that the RFC OTA can be regarded as a three-current mirror OTA with an additional signal path formed by the extra differential pair M_{1A} and M_{2A} cross-connected to the folding nodes at the output branch.

Despite the advantages of the RFC OTA, its power efficiency is limited, due to two main reasons: First, current gain K scales both dynamic and static currents. Hence, although SR is K times higher than for the FC OTA it is still proportional to I_B and thus proportional to the static power consumption. Second, the active current mirrors included lead to internal copy of dynamic currents, degrading current efficiency [8].

Fig. 1(c) shows a power-efficient super class-AB implementation of the RFC OTA proposed here, which solves these shortcomings. An adaptive bias circuit replaces the constant current source $2I_B$ that bias the differential pair. This way, low static currents can be set and at the same time dynamic currents not limited by I_B can be generated at the differential pair for large input signals. Moreover, transistors M_{3B}–M_{3C} and M_{4B}–M_{4C} in the RFC OTA are rearranged by connecting the gates of M_{3B} and M_{4B} and feeding the common mode of the drain voltages of M_{3C} and M_{4C} back to the resulting common gate node by the two matched resistors with equal resistance $R_1 = R_2 = R$. This technique, known as local common-mode feedback (LCMFB) [9], allows further increase of the dynamic currents without scaling static currents. In the absence of input signal, there is no voltage drop in R_1 and R_2, so M_{3A}–M_{3B} and M_{4A}–M_{4B} act as conventional current mirrors. However, for a large positive V_{id}, current I_{1B} in M_{1B} is lower than current I_{2B} in M_{2B}, leading to a voltage drop $\Delta V = R(I_{2B} - I_{1B})/2$ in R_1 and R_2. This voltage drop is added to the quiescent gate voltage of M_{3A} and subtracted from the quiescent gate voltage of M_{4A}, yielding a large output current leaving the OTA. Analogously, for a large negative V_{id} voltage drop $\Delta\ V = R \cdot (I_{2B} - I_{1B})/2$ is negative, leading to a large output current entering the OTA. Hence, SR is improved without increasing quiescent currents.

Besides improved dynamic performance, LCMFB also increases small-signal performance thanks to the small-signal current gain provided by the LCMFB resistors and the ac small-signal ground at the common gate of M_{3B}–M_{4B}. An in-depth analysis of the small-signal and large-signal operation of the super class-AB RFC OTA is presented in Sections III and IV, respectively.

Several choices can be made for the adaptive biasing of the differential pair in Fig. 1(c). Three possibilities are reported in [8]. In this paper, two dc level shifters have been cross-coupled to the differential pair transistors, as shown in the detailed schematic of Fig. 2. These level shifters are

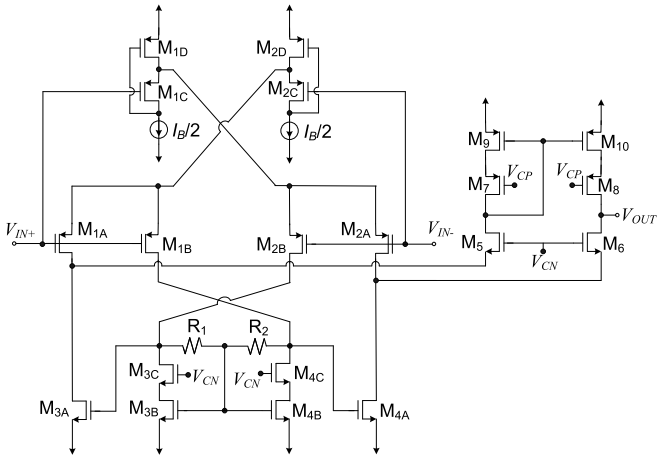

Fig. 2. Detailed implementation of the super class-AB RFC OTA.

implemented by the flipped voltage followers (FVFs) [10] M_{1C}–M_{1D} and M_{2C}–M_{2D}, biased with a dc current $I_B/2$, yielding a dc level shift $V_B = V_{SG1C} = V_{SG2C}$. Under quiescent conditions $V^Q_{SG1A} = V^Q_{SG1B} = V^Q_{SG2A} = V^Q_{SG2B} = V_B$, hence, M_{1A}, M_{1B}, M_{2A}, and M_{2B} have equal quiescent currents equal to $I_B/2$ regardless of process, supply voltage or temperature (PVT) variations (but not mismatch). This static current can be made very low by choosing low I_B. However, for a nonzero input signal V_{id}, voltage $V_{SG1A} = V_{SG1B}$ is increased by V_{id} and voltage $V_{SG2A} = V_{SG2B}$ is decreased by V_{id}. This leads to dynamic currents not limited by I_B. Also, an increment in transconductance by a factor 2 is achieved compared to the conventional biasing of Fig. 1(a) and (b), where only $V_{id}/2$ is added to $V_{SG1A,B}$ and subtracted from $V_{SG2A,B}$. However, a 50% extra bias current is used versus FC OTA and RFC OTA [Fig. 1(a) and (b)].

The minimum supply voltage of the OTA is $V_{DD,min} = |V_T| + 3|V_{DS,sat}|$, with $|V_{DS,sat}| = |V_{GS}| - |V_T|$ the drain–source saturation voltage. Hence, the circuit can operate at moderately low voltage. In fact, FVFs are suited to low supply voltage, since the drain voltage of $M_{1C,2C}$ is set to $V_{DD} - V_{SG1D,2D}$. Hence, the input range of the FVFs in Fig. 2 and thus the common-mode input range (CMIR) of the OTA is $|V_{TP}| - |V_{DS,sat1C}|$ to keep M_{1C}–M_{2C} in saturation. Note that it does not increase with the supply voltage. In the process employed $V_{TP} = -0.96$ V, so with $|V_{DS,sat1C}| = 0.1$ V, CMIR = 0.86 V. The CMIR of the RFC OTA of Fig. 1(b) is $V_{DD} - |V_{SS}| - 2|V_{DS,sat}| - |V_{TP}|$, that for a 2-V supply leads to 0.84 V, a similar value. If a higher CMIR (and supply voltage) is required for the proposed OTA, a dc level shift made by a source follower can be included in the FVF loop [10].

III. Small-Signal Performance

Analysis of the small-signal operation of the proposed super class-AB RFC OTA is presented in this section, as well as comparison with the FC and RFC OTAs.

A. Small-Signal Transconductance, Gain, and GBW

The small-signal transconductance of the FC OTA is

$$G_{m\mathrm{FC}} = 2 \times g_{m1\mathrm{A}} \tag{1}$$

and that of the RFC OTA is

$$G_{m\mathrm{RFC}} = g_{m1\mathrm{A}}(1 + K) \tag{2}$$

with g_{m1A} being the transconductance gain of transistor M_{1A}. Note that for the typical value $K = 3$, $G_{m\mathrm{RFC}}$ is twice $G_{m\mathrm{FC}}$ using the same static power. The transconductance of the super class-AB RFC OTA of Fig. 2 is

$$G_{m\mathrm{AB}} = 2 \cdot g_{m1\mathrm{A}}[1 + g_{m3\mathrm{A}}(R||r_{o2\mathrm{B}})] \tag{3}$$

with r_{o2B} being the small-signal drain–source resistance of transistor M_{2B}. The factor 2 in (3) is due to the extra transconductance provided by the adaptive bias circuit of the differential pair, and the factor $1 + g_{m3A}(R||r_{o2B})$ is due to the LCMFB configuration. Note that choosing

$$R > \frac{K - 1}{2g_{m3\mathrm{A}}} \tag{4}$$

transconductance of the super class-AB RFC OTA is larger than that of the RFC OTA, where it has been assumed that $R \ll r_{o2B}$.

The output resistance of the FC OTA is

$$R_{o,\mathrm{FC}} \approx g_{m6}r_{o6}\left(\frac{r_{o2\mathrm{A}}||r_{o4\mathrm{A}}}{2}\right)||g_{m8}r_{o8}r_{o10} \tag{5}$$

and that of the RFC and super class-AB RFC OTA is

$$R_{o,\mathrm{RFC}} = R_{o,\mathrm{AB}} \approx g_{m6}r_{o6}(r_{o2\mathrm{A}}||r_{o4\mathrm{A}})||g_{m8}r_{o8}r_{o10}. \tag{6}$$

Hence, both the conventional RFC and super class-AB RFC OTAs enhance low-frequency gain compared to the FC OTA due to the higher transconductance and output resistance. If design condition (4) is met, the super class-AB RFC provides more gain than the RFC OTA due to the increased transconductance, which is also responsible for the same increase in GBW. Expressions for the GBW of the FC, RFC, and super class-AB RFC OTAs are

$$\mathrm{GBW_{FC}} = \frac{2g_{m1\mathrm{A}}}{2\pi C_L} \tag{7}$$

$$\mathrm{GBW_{RFC}} = \frac{(K+1)\,g_{m1\mathrm{A}}}{2\pi C_L} \tag{8}$$

$$\mathrm{GBW_{AB}} = \frac{2g_{m1\mathrm{A}}}{2\pi C_L}[1 + g_{m3\mathrm{A}}(R||r_{o2\mathrm{B}})]. \tag{9}$$

Note that as R increases, GBW of the super class-AB RFC OTA also increases. However, larger values for the LCMFB resistors lead to a decrease in the non-dominant poles associated with the drain of M_{3C} and M_{4C}. Hence, a tradeoff between GBW increase and phase margin (PM) degradation exists in the choice of R.

B. Stability Analysis

The FC, RFC, and super class-AB RFC OTAs have a dominant pole $\omega_{p1} = -1/(R_{\mathrm{out}}C_{\mathrm{out}})$ set by the output terminal, with $C_{\mathrm{out}} \approx C_L$ the output capacitance of the OTA. They also have a non-dominant pole $\omega_{p2} \approx -g_{m5}/C_{p5}$ corresponding to the source terminals of M_5 and M_6, with C_{p5} the intrinsic capacitance at the source of M_5, which is C_{gs5} plus other smaller capacitances. In addition, the RFC

introduces a pole–zero pair due to the active current mirrors M_{3A}–M_{3B} and M_{4A}–M_{4B}, $\omega_{p3} \approx -g_{m3B}/(C_{gs3A} + C_{gs3B})$, and $\omega_{z1} \approx -(1+K)\omega_{p3}$. Since this pole–zero pair is associated with NMOS devices, it is usually at relatively high frequency. However, large K values increase C_{gs3A} and thus decrease ω_{p3}. For this reason, practical K values in the RFC are around 2–4 [2].

In the proposed super class-AB RFC, the virtual signal ground at the common gate of M_{3B}–M_{4B} cancels the effect of C_{gs3B} and C_{gs4B}, but R_1 and R_2 increase the resistance at the nodes corresponding to the drains of M_{3C} and M_{4C}. Hence, the non-dominant pole ω_{p3} becomes $\omega_{p3} \approx -1/[(R||r_{o2B})C_{gs3A}]$ and is the lowest frequency non-dominant pole even for moderate R values, yielding a PM in this case

$$\begin{aligned}\text{PM} &\approx 90^\circ - \tan^{-1}\left(\frac{\text{GBW}}{f_{p3}}\right) \\ &\approx 90^\circ - \tan^{-1}\left\{2g_{m1A}(R||r_{o2B})\frac{C_{gs3A}}{C_L}[1+g_{m3A}(R||r_{o2B})]\right\}.\end{aligned} \tag{10}$$

Hence, to get, e.g., a target PM = 60°, the minimum load capacitance under these conditions is

$$C_{L,\min} \approx 3.46 g_{m1A}(R||r_{o2B})[1 + g_{m3A}(R||r_{o2B})]\, C_{gs3A}. \tag{11}$$

Note from (10) that a large R value leads to a significant PM degradation. This has traditionally limited the performance of LCMFB schemes [9]. Fortunately, in super class-AB OTAs it is not necessary to use large R values to achieve very high SR and current efficiency, since the adaptive biasing of the differential input pair allows large voltage drops at the resistors without requiring large resistance values or large static power consumption.

C. Noise Analysis

An analysis of the equivalent input noise of the FC, RFC, and super class-AB RFC OTAs is presented in Appendix A. Regarding thermal noise, note from this analysis that the higher dc gain of the RFC and super class-AB RFC reduces the influence of the transistors in the output branch on the input-referred noise, as expected. It is not possible to determine the topology with the lowest thermal noise, as it depends on g_m and R values chosen. However, just to have a numerical example, assuming that $g_{m1A} = g_{m3B} = g_{m9} = g_{m3A}/3$ and that $R = 10/g_{m3B}$, the RFC OTA and super class-AB RFC OTA have a 18% and 55% lower input-referred thermal noise than the FC OTA, respectively. A higher R value further decreases the input noise due to the increased dc gain, but it also degrades PM as described previously.

Concerning flicker noise, note from the analysis of Appendix A the reduction of flicker noise achieved in the super class-AB RFC OTA, which is due to the lower influence of the NMOS transistors (which generate the larger flicker noise) when the noise generated by them is referred to the input, thanks to the larger dc gain.

IV. Large-Signal Performance

A critical factor in the settling performance of the OTA is the SR. Assuming a capacitive load, it is given by SR = $I_{o\max}/C_{\text{out}}$, with $I_{o\max}$ the maximum output current, and $C_{\text{out}} \approx C_L$ if as usually load capacitance C_L is much larger than the intrinsic capacitance at the output node. The SR of the FC OTA of Fig. 1(a) is

$$\text{SR}_{\text{FC}+} = \text{SR}_{\text{FC}-} = \frac{2I_B}{C_L} \tag{12}$$

since the maximum current sourced to the load of sunk from it is $2I_B$. Symmetrical positive and negative slews are achieved, but the maximum output current is limited by the bias current. Hence, a tradeoff between SR and static power consumption arises. The SR in the RFC OTA is approximately [2]

$$\text{SR}_{\text{RFC}+} = \text{SR}_{\text{RFC}-} = \frac{2KI_B}{C_L} \tag{13}$$

which is higher than for the FC OTA for $K > 1$ but still experiencing the same tradeoff.

The approximate theoretical SR of the super class-AB RFC OTA of Fig. 2 is deduced in Appendix B, yielding

$$\text{SR}_+ \approx \frac{\beta_{3A}}{2C_L}\left(\sqrt{\frac{\beta_{2B}}{2\beta_{3B}}}A + \frac{R_1\beta_{2B}}{4}A^2\right)^2 \tag{14}$$

$$SR_- \approx \frac{\beta_{4A}}{2C_L}\left(\sqrt{\frac{\beta_{1B}}{2\beta_{4B}}}A + \frac{R_2\beta_{1B}}{4}A^2\right)^2 \tag{15}$$

with $\beta_i = \mu C_{\text{ox}}(W/L)_i$ and A being the amplitude of the differential input step. Note that a large value not bound by I_B can be achieved. Expressions (14) and (15) are a theoretical limit. In practice values of SR are lower since some transistors leave the saturation region for large input steps (e.g., by the limitation of drain voltage set by the cascode transistors) and due to the second-order effects which are not accounted for in the simple MOS square-law model. However, these expressions reflect that large SR can be achieved without increasing static power and show the main parameters influencing SR.

V. Fully Differential Version

An FD version of the OTA of Fig. 2 can be simply obtained by replacing the output current mirror by two matched current sources and including a common-mode feedback (CMFB) circuit. The analysis of Sections III and IV essentially applies to this FD implementation. However, as for the FD RFC OTA, there is a potential asymmetry in the charge/discharge rate of the outputs that can be balanced by a fast and accurate CMFB [2].

An alternative FD implementation is shown in Fig. 3 based on [11]. The gates of M_9 and M_{10} are connected to the gates of M_{2D} and M_{1D}, respectively. Hence, current in M_{1D} and M_{2D} is copied to the output branches, increasing G_m of the OTA and therefore its dc gain and GBW.

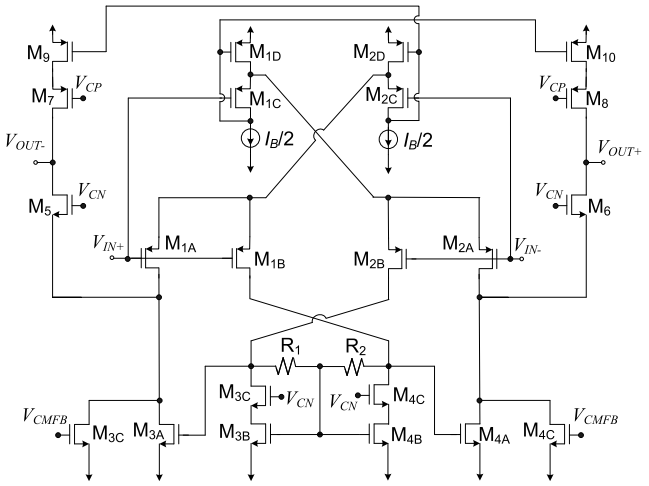

Fig. 3. FD super class-AB RFC OTA.

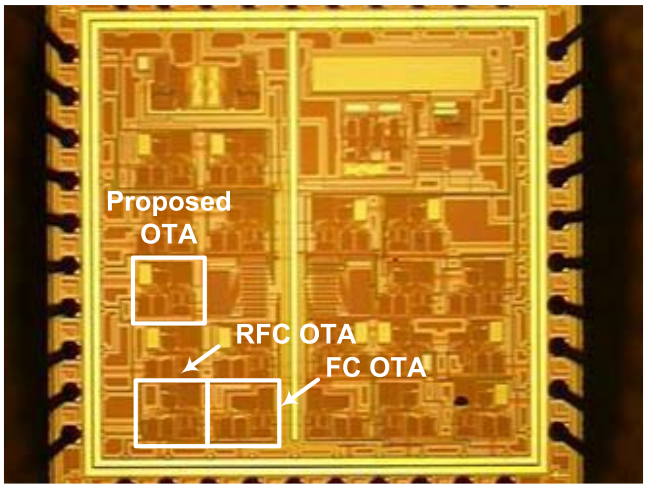

Fig. 4. Test chip microphotograph.

VI. Design Methodology

Amplifier design is application specific, so it is difficult to outline a generic design strategy. However, in most cases GBW, PM, and SR are the key design criteria. Hence, (9), (10), (14), and (15) can be used as a starting point for a preliminary hand-calculation design of a super class-AB RFC OTA. Common design practices can be used for choosing the transistor aspect ratios [2]. Thus, input transistors M_{1A}, M_{1B}, and M_{1C} and M_{2A}, M_{2B}, and M_{2C} have typically large aspect ratio and are biased in moderate or even weak inversion to increase GBW and minimize input offset and noise. Moreover, this choice also reduces their $|V_{DS,sat}|$, maximizing CMIR as discussed in Section II. A critical design choice is the value of R, as it represents a tradeoff between increase of GBW, SR, reduction of input noise and increase of PM, and silicon area. For a given power budget (hence I_B), C_L and minimum PM, (10) can be used to estimate the maximum R, which can then be used in (9) to estimate the GBW and (to a first-order approach) the SR using (14) and (15). This procedure can be the starting point to refine R value and aspect ratios during computer simulations.

VII. Simulation and Measurement Results

The super class-AB RFC of Fig. 2 was fabricated in a 0.5-μm double-poly, three-metal n-well CMOS technology with nominal NMOS and PMOS threshold voltages of $V_{TN} = 0.67$ V and $V_{TP} = -0.96$ V, respectively. Both the FC and RFC OTAs of Fig. 1(a) and (b) are also fabricated on the same test chip prototype for comparison purposes. The three OTAs were available on the chip in both open loop and in unity-gain closed-loop configuration. Resistors R_1 and R_2 were made by a high resistance polysilicon layer available in the technology. They have a nominal value of 10 kΩ and were interdigitized and surrounded by dummy strips for improved matching. Similar conventional matching techniques were also used for the transistors. A microphotograph of the three OTAs is shown in Fig. 4, where their relative area requirements can be observed. Transistor dimensions are summarized in Table I.

TABLE I
Transistor Aspect Ratios

Transistor	W/L (μm/μm)
M_{1A}-M_{2A}	190/0.6
M_{1B}-M_{2B}	190/0.6
M_{1C}-M_{2C}	190/0.6
M_{1D}-M_{2D}	60/0.6
M_{3A}-M_{4A}	180/0.6
M_{3B}-M_{4B}	60/0.6
M_{3C}-M_{4C}	60/0.6
M_5-M_6	120/0.6
M_7-M_8	200/0.6
M_9-M_{10}	200/0.6

The supply voltages employed in all the measurements were ± 1 V, and the bias current I_B was 10 μA. Externally applied cascode bias voltages V_{CP} and V_{CN} were -0.5 and 0.3 V, respectively. An off-chip ceramic load capacitor of 47 pF was connected to the output of the OTAs for measurements. As the OTA outputs were directly connected to bonding pads and the test probe is connected without a buffer, the total load capacitance is increased by the pad, board, and test probe capacitance. The estimated total value of C_L is hence of approximately 70 pF.

Fig. 5 shows the simulated open-loop ac small signal response of the amplifiers. The dc gain of the FC, RFC, and super class-AB RFC is 60.3, 68.4, and 76.8 dB, respectively. Note the increased value of the super class-AB RFC OTA versus the RFC OTA due to the LCMFB technique, as expected. The GBW of the FC, RFC, and super class-AB RFC is 500.7 kHz, 975 kHz, and 3 MHz, respectively. Hence, the super class-AB RFC OTA shows an increase in GBW by a factor 6 when compared to the FC OTA and about 3 versus the RFC OTA. The PM of FC, RFC, and super class-AB RFC is 89°, 86.7°, and 75.1°, respectively. At 3 MHz, the PM of the RFC OTA is 79.6° so the super class-AB RFC OTA leads to a degradation of 4.5° for the reason described in Section III-B.

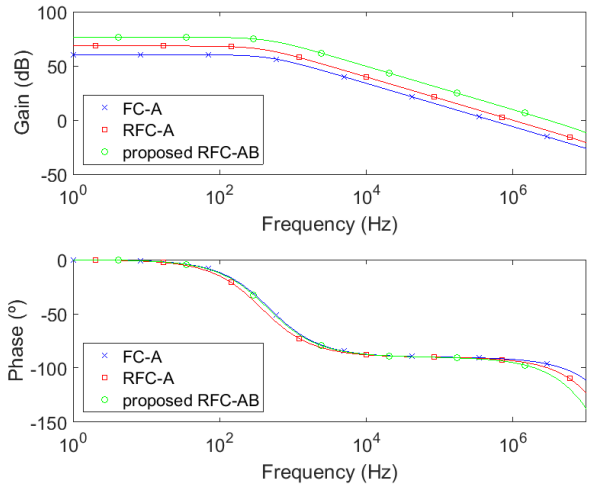

Fig. 5. Simulated ac open-loop response of the FC, RFC and super class-AB RFC OTAs.

The experimental setup employed for different measurements is shown in Fig. 6. For output current measurements, as shown in Fig. 6(a), the OTAs in open-loop configuration were driven by the differential output of an Agilent 33522A arbitrary waveform generator, and the output was connected to a transresistance amplifier for voltage-to-current conversion. The resulting voltage was applied to a Tektronix TDS 5104 oscilloscope for capture and display.

As shown in Fig. 6(b), for time-domain measurements the Agilent 33522A signal is applied to the OTAs in unity-gain closed-loop configuration and the unbuffered output is directly connected to the TDS 5104 oscilloscope using a conventional test probe. For distortion analysis, the output signal was applied to a Hewlett Packard 89410A Vector Signal Analyzer. The HP 89410A was also used for frequency response measurements, as shown in Fig. 6(c), using a chirp sweep. The setup employed for noise measurements is shown in Fig. 6(d). An external amplifier with a gain 10 was used to amplify noise, and its output was connected to the HP 89410A.

Fig. 7 shows the measured output current of the three OTAs for a differential input voltage ranging from -0.2 to 0.2 V. Note that the output current of the FC and RFC OTA is limited by the bias current as they operate in class A. The super class-AB RFC OTA features much larger output currents for large input signals, not limited by the bias current.

The measured response the OTAs using a 1-MHz, 0.5-V periodic square wave with dc level of -0.3 V at the input is shown in Fig. 8, as well as the input waveform. Note the faster settling of the proposed super class-AB RFC OTA. The measured SR_+ for the FC OTA and RFC OTA is 0.20 and 0.38 V/μs, respectively. The measured SR_+ for the super class-AB RFC OTA is 13.2 V/μs, which corresponds to an increase factor of 66 and 34.7 versus the FC and RFC OTAs, respectively, for the same quiescent current and C_L. An 8% undershoot is observed at the falling edge, which is attributed to the adaptive biasing when it operates with very low input voltages. Note, however, that the output is damped in a cycle, denoting the stable closed-loop operation of the amplifier.

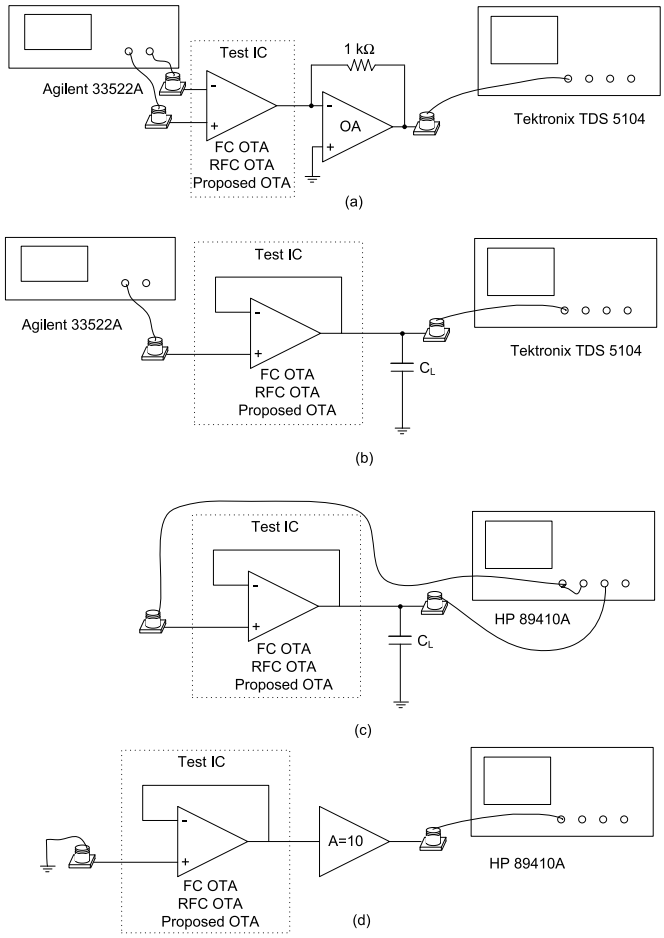

Fig. 6. Measurement setup. (a) Output current measurements. (b) Time-domain measurements. (c) Frequency response measurements. (d) Noise measurements.

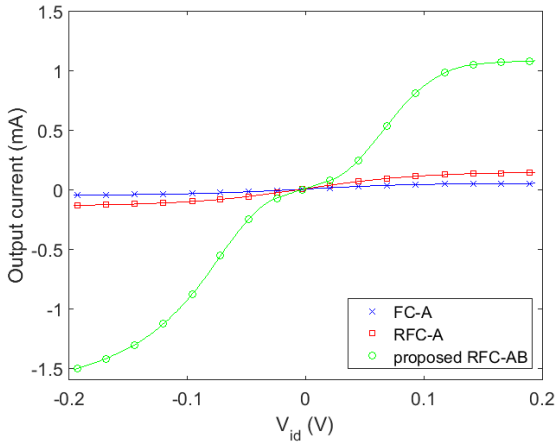

Fig. 7. Measured output current of the FC, RFC, and super class-AB RFC OTAs versus differential input voltage.

No overshoot/undershoot is observed for small input steps, as expected from the PM of 75.1°.

Fig. 9 shows the measured total harmonic distortion (THD) of the three OTAs for an input sinusoid of 25 kHz and peak-to-peak amplitude ranging from 200 mV to 1 V. Note that

TABLE II
SUMMARY OF MEASUREMENT RESULTS AND PERFORMANCE COMPARISON

Parameter	FC OTA	RFC OTA	Proposed OTA	[12]	[13]	[14]	[15]	[16]	[17]
CMOS process	0.5 µm	0.5 µm	0.5 µm	0.18 µm	0.18 µm	0.35 µm	0.5 µm	0.18 µm	0.18 µm
Supply voltage	±1 V	±1 V	±1 V	0.8 V	0.5 V	1 V	±1.25 V	0.7 V	1.8 V
Capacitive load	70 pF	70 pF	70 pF	8 pF	20 pF	15 pF	25 pF	20 pF	200 pF
Fully differential	No	No	No	Yes	Yes	No	No	No	Yes
Compensation	Load cap.	Load cap.	Load cap.	Load cap.	Miller	Miller	RNMC	RNMC	Load cap.
SR+	0.20 V/µs	0.38 V/µs	13.2 V/µs	0.14 V/µs	2.89 V/µs	2.53 V/µs	2.7 V/µs	1.8 V/µs	74.1 V/µs
SR-	-0.66 V/µs	-1.5 V/µs	-25.3 V/µs	--	--	-1.37 V/µs	-3.3 V/µs	-3.8 V/µs	--
Pos. Settling	2.70 µs	1.72 µs	120 ns	--	--	224 ns	--	1.3 µs	--
Neg. Settling	1.84 µs	560 ns	100 ns	--	--	--	--	1 µs	--
THD	-37.8 dB @25kHz, 0.5V_{pp}	-47.4 dB @25kHz, 0.5V_{pp}	-55.5 dB @25kHz, 0.5V_{pp}	-52 dB @1kHz, 0.5V_{pp}	-40dB @0.4V_{pp}	--	-47.1 dB @2V_{pp}	-40.1 dB @250kHz 0.4V_{pp}	--
DC gain (*)	60.3 dB	68.4 dB	76.8 dB	51 dB	52 dB	88.3 dB	63.4 dB	57.5 dB	72 dB
PM (*)	89º	86.7º	75.1º	60º	--	66.1º	83º	60º	50º
GBW	530 kHz	980 kHz	3.4 MHz	57 kHz	2.5 MHz	11.67 MHz	4.9 MHz	3 MHz	86.5 MHz
CMRR @DC	97 dB	111 dB	112 dB	--	78 dB	40 dB	80 dB	19 dB	--
PSRR+ @DC	73 dB	82 dB	92 dB	--	76 dB	40 dB	61.2 dB	52.1 dB	--
PSRR-@DC	93 dB	104 dB	113 dB	--	--	--	--	66.4 dB	--
Eq. input noise @1MHz	35 nV/√Hz	30 nV/√Hz	23 nV/√Hz	--	80 nV/√Hz	<60 nV/√Hz	--	100 nV/√Hz	--
Power	80 µW	80 µW	100 µW	1.2 µW	110 µW	197 µW	437.5 µW	25.4 µW	11.9 mW
Area	0.022 mm^2	0.026 mm^2	0.030 mm^2	0.057 mm^2	0.026 mm^2	0.157 mm^2	0.029 mm^2	0.020 mm^2	0.070 mm^2

(*) Simulation

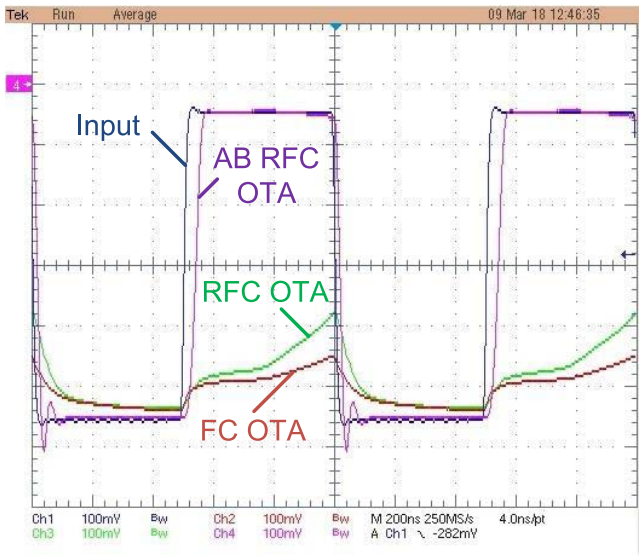

Fig. 8. Measured response of the FC, RFC, and super class-AB RFC OTAs to a square input signal.

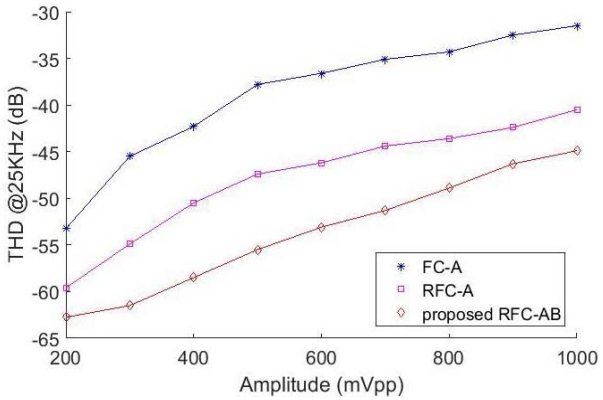

Fig. 9. Measured THD versus input amplitude of the FC, RFC, and super class-AB RFC OTAs.

the proposed super class-AB RFC OTA achieves the lowest distortion, which is attributed to the higher dc open-loop gain and the improved settling performance. The main contribution to distortion in the three OTAs is due to the second harmonic, as expected for single-ended topologies.

A summary of the main measurement results obtained for the three OTAs is provided in Table II, also including data for other OTAs reported to date for comparison. GBW is approximated by the measured bandwidth of the OTAs in unity-gain configuration, since the non-dominant poles are beyond the unity-gain bandwidth. Note that the proposed OTA improves both small-signal and large-signal performances, in agreement with the analysis presented in Sections III and IV. Increase in the measured GBW versus the value in simulation for the proposed OTA is mainly attributed to process variations of the polysilicon resistors implementing R. Parameters like common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR), and equivalent input noise density are enhanced mainly due to the higher dc gain of the proposed OTA. The drawbacks are the lower value of the PM, the 25% extra quiescent power consumption due to the added current sources $I_B/2$ in the adaptive biasing, and a 15% extra silicon area due to the adaptive biasing and the resistors. It is also possible to scale down by a factor n transistors M_{1C} and M_{2C},

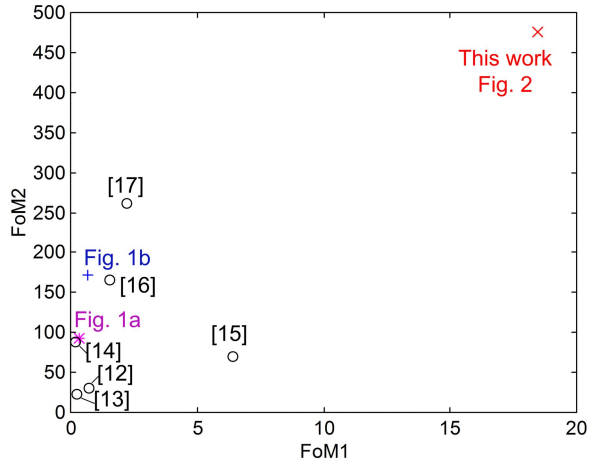

Fig. 10. Performance comparison using two FoM.

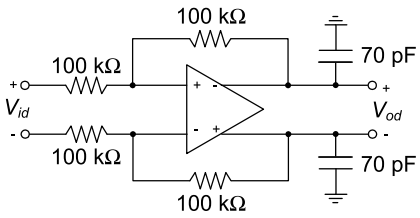

Fig. 11. Circuit for simulation of FD OTAs.

TABLE III
SIMULATION RESULTS—FD OTAS

Parameter	Conventional FD OTA	FD OTA Fig. 3
SR+	9 V/μs	9 V/μs
SR-	-9 V/μs	-10 V/μs
THD @ 100 kHz 0.5Vpp	-63 dB	-72 dB
DC gain	74.6 dB	76 dB
PM	76º	74º
GBW	3 MHz	4.1 MHz
Eq. input noise @1MHz	15 nV/√Hz	14 nV/√Hz
Power (inc. CMFB)	140 μW	140 μW

scaling by the same factor the FVF bias current and leading to just a $25/n\%$ extra power.

To simplify comparison with the OTAs in Table II, two conventional figures of merit (FoMs) have been employed: $\text{FoM}_1 = \text{SR} \cdot C_L/I_{\text{supply}} = I_{\max L}/I_{\text{supply}}$, where I_{supply} is the total current consumption, which evaluates large-signal performance versus power, and $\text{FoM}_2 = 100 \cdot \text{GBW} \cdot C_L/I_{\text{supply}}$ (MHz · pF/μA) which indicates small-signal performance versus power. The results are presented graphically in Fig. 10. Note that the super class-AB RFC OTA shows improved performance for both FoMs.

Both the conventional FD implementation of the super class-AB RFC OTA (replacing the output PMOS current mirror by two matched current sources) and that of Fig. 3 are tested in simulation. Time-domain simulations were done using the configuration of Fig. 11. The same component dimensions, supply voltage, and bias currents as for the single-ended version were employed. The CMFB circuit of [18] controlling NMOS current sources was used in both OTAs to get a fast and accurate CMFB loop. Table III summarizes the main results, evidencing the improvement of the OTA of Fig. 3.

VIII. CONCLUSION

A simple modification of the RFC OTA has been proposed, which leads to a super class-AB implementation. The use of adaptive biasing of the differential pair and LCMFB leads to the improved small-signal and large-signal performances. Measurement results show a significant increase in SR and GBW as well as fast settling. The OTA can be employed in low-voltage low-power circuits requiring a good performance/power tradeoff.

APPENDIX A

The most relevant noise sources in CMOS analog circuits are thermal and flicker noise. Assuming operation in saturation, a simplified expression of the spectral density of the noise current of a MOS transistor is [19]

$$I_n^2(f) = 4\delta k_B T g_m + \frac{K_f g_m^2}{\text{WLC}_{\text{ox}} f} = 4\delta k_B T g_m + \frac{2\mu K_f I_D}{L^2 f} \tag{A-1}$$

with k_B being Boltzmann's constant, T being the absolute temperature, μ being the carrier mobility, and K_f being a technology-dependent parameter which is also dependent on device characteristics. Factor δ varies from 1/2 to 2/3 from weak to strong inversion. The first and second terms in (A-1) correspond to the thermal and flicker noise, respectively. Expression (A-1) represents a good tradeoff between simplicity, accuracy, and validity in all the inversion regions.

Assuming as usually that all noise sources are uncorrelated, and for simplicity the same δ factor for all transistors, the input-referred mean-square thermal noise of the FC OTA in a bandwidth Δf is

$$\overline{v_{\text{nt,inFC}}^2} = \frac{2\delta k_B T \Delta f}{g_{m1\text{A}}} \left(2 + \frac{g_{m3\text{A}}}{g_{m1\text{A}}} + \frac{g_{m3\text{B}}}{g_{m1\text{A}}} + \frac{g_{m9}}{g_{m1\text{A}}}\right) \tag{A-2}$$

and that of the RFC OTA is

$$\overline{v_{\text{nt,inRFC}}^2} = \frac{8\delta k_B T \Delta f}{g_{m1\text{A}}\,(1+K)^2} \left[1 + K^2 + (1+K)\frac{g_{m3\text{A}}}{g_{m1\text{A}}} + \frac{g_{m9}}{g_{m1\text{A}}}\right] \tag{A-3}$$

which for the implemented value of $K = 3$ becomes

$$\overline{v_{\text{nt,inRFC}}^2} = \frac{2\delta k_B T \Delta f}{g_{m1\text{A}}} \left(\frac{5}{2} + \frac{g_{m3\text{A}}}{g_{m1\text{A}}} + \frac{1}{4}\frac{g_{m9}}{g_{m1\text{A}}}\right). \tag{A-4}$$

The expression for the super class-AB RFC OTA is

$$\overline{v_{\text{nt,inAB}}^2} = \frac{2\delta k_B T \Delta f}{g_{m1\text{A}}} \left[\begin{array}{l} \dfrac{g_{m3\text{A}} + g_{m9}}{g_{m1\text{A}}(1+g_{m3\text{A}}R)^2} + \dfrac{1+2(g_{m3\text{A}}R)^2}{(1+g_{m3\text{A}}R)^2} \\ + \dfrac{1}{g_{m1\text{A}}} \left(\dfrac{g_{m3\text{A}}R}{1+g_{m3\text{A}}R}\right)^2 \left(g_{m3\text{B}} + \dfrac{1}{\delta R}\right) \end{array}\right] \tag{A-5}$$

when $R \gg 1/g_{m3\text{A}}$ becomes

$$\overline{v_{\text{nt,inAB}}^2} \approx \frac{2\delta k_B T \Delta f}{g_{m1\text{A}}} \left(2 + \frac{g_{m3\text{B}}}{g_{m1\text{A}}} + \frac{1}{\delta g_{m1\text{A}} R}\right). \tag{A-6}$$

Concerning flicker noise, assuming again uncorrelated noise sources and the same K_f for all the transistors of the same type (NMOS or PMOS), the expression for the input-referred spectral noise density of the FC OTA is

$$V^2_{\text{nf,inFC}}(f)=\frac{2K_{fp}}{C_{\text{ox}}fW_1L_1}\left[1+\left(\frac{L_1}{L_9}\right)^2+2\frac{K_{fn}}{K_{fp}}\frac{\mu_n}{\mu_p}\left(\frac{L_1}{L_3}\right)^2\right] \tag{A-7}$$

and for the RFC OTA it is

$$V^2_{\text{nf,inRFC}}(f)=\frac{2K_{fp}}{C_{\text{ox}}fW_{1\text{A}}L_{1\text{A}}}\left[\begin{array}{l}\dfrac{1+K^2}{(1+K)^2}+\dfrac{2}{(1+K)^2}\left(\dfrac{L_{1\text{A}}}{L_9}\right)^2\\ \quad+\dfrac{K_{fn}}{K_{fp}}\dfrac{\mu_n}{\mu_p}\dfrac{K}{1+K}\left(\dfrac{L_{1\text{A}}}{L_{3\text{B}}}\right)^2\end{array}\right]. \tag{A-8}$$

The input-referred flicker noise spectral density of the super class-AB RFC OTA is

$$V^2_{\text{nf,inAB}}(f)=\frac{K_{fp}}{2C_{\text{ox}}fW_{1\text{A}}L_{1\text{A}}(1+g_{m3\text{A}}R)^2}\times\left\{\begin{array}{l}1+2\left(\dfrac{L_{1\text{A}}}{L_9}\right)^2+3\dfrac{K_{fn}}{K_{fp}}\dfrac{\mu_n}{\mu_p}\left(\dfrac{L_{1\text{A}}}{L_{3\text{A}}}\right)^2\\ +(g_{m3\text{A}}R)^2\left[2+\dfrac{K_{fn}}{K_{fp}}\dfrac{\mu_n}{\mu_p}\left(\dfrac{L_{1\text{A}}}{L_{3\text{B}}}\right)^2\right]\end{array}\right\}. \tag{A-9}$$

In our design all the transistors were implemented with the same L (the minimum one available in the technology), so that expressions for the flicker noise of the FC OTA, RFC OTA with $K=3$, and super class-AB RFC OTA with $R\gg 1/g_{m3\text{A}}$ are

$$V^2_{\text{nf,inFC}}(f)=\frac{4K_{fp}}{C_{\text{ox}}fW_1L_1}\left(1+\frac{K_{fn}}{K_{fp}}\frac{\mu_n}{\mu_p}\right) \tag{A-10}$$

$$V^2_{\text{nf,inRFC}}(f)=\frac{4K_{fp}}{C_{\text{ox}}fW_{1\text{A}}L_{1\text{A}}}\frac{3}{8}\left(1+\frac{K_{fn}}{K_{fp}}\frac{\mu_n}{\mu_p}\right) \tag{A-11}$$

$$V^2_{\text{nf,inAB}}(f)\approx\frac{4K_{fp}}{C_{\text{ox}}fW_{1\text{A}}L_{1\text{A}}}\frac{3}{8}\left(\frac{2}{3}+\frac{1}{3}\frac{K_{fn}}{K_{fp}}\frac{\mu_n}{\mu_p}\right). \tag{A-12}$$

Appendix B

The theoretical SR for the super class-AB RFC OTA of Fig. 2 will be derived for simplicity using the conventional square-law drain current model for transistors in the saturation region, and neglecting channel length modulation and short-channel effects. Thus, if a large positive V_{id} is applied, current in transistor $M_{2\text{B}}$ becomes

$$I_{2\text{B}}=\frac{\beta_{2\text{B}}}{2}\left(\sqrt{\frac{I_B}{\beta_{1\text{B}}}}+V_{\text{id}}\right)^2 \tag{B-1}$$

with $\beta_i=\mu_pC_{\text{ox}}(W/L)_i$. Current in transistors $M_{1\text{A}}$ and $M_{1\text{B}}$ becomes negligible. Hence, a differential current $I_d=I_{2\text{B}}-I_{1\text{B}}\approx I_{2\text{B}}$ flows in $M_{1\text{B}}$–$M_{2\text{B}}$, yielding a current $I_d/2$ flowing through the resistors. Current in transistors $M_{3\text{B}}$, $M_{3\text{C}}$, $M_{4\text{B}}$, and $M_{4\text{C}}$ is $I_{\text{cm}}=(I_{2\text{B}}+I_{1\text{B}})/2\approx I_{2\text{B}}/2$. Therefore, current in transistor $M_{3\text{A}}$ becomes

$$I_{3\text{A}}=\frac{\beta_{3\text{A}}}{2}\left(\sqrt{\frac{2I_{\text{cm}}}{\beta_{3\text{B}}}}+\frac{R_1I_d}{2}\right)^2\approx\frac{\beta_{3\text{A}}}{2}\left(\sqrt{\frac{I_{2\text{B}}}{\beta_{3\text{B}}}}+\frac{R_1I_{2\text{B}}}{2}\right)^2 \tag{B-2}$$

while current in $M_{4\text{A}}$ becomes negligible due to the large negative swing at its gate created by the voltage drop at R_2. This increases the drain voltage of $M_{4\text{A}}$ and drives $M_{2\text{A}}$ into deep triode. The large current $I_{3\text{A}}$ is mirrored by the PMOS current mirror M_9–M_{10}, yielding an output current

$$\begin{aligned}I_{\text{out}}&\approx\frac{\beta_{3\text{A}}}{2}\left(\sqrt{\frac{2I_{\text{cm}}}{\beta_{3\text{B}}}}+\frac{R_1I_d}{2}\right)^2\\&\approx\frac{\beta_{3\text{A}}}{2}\left(\sqrt{\frac{\beta_{2\text{B}}}{2\beta_{3\text{B}}}}V_{\text{id}}+\frac{R_1\beta_{2\text{B}}}{4}V^2_{\text{id}}\right)^2.\end{aligned} \tag{B-3}$$

Hence, for a differential input step of A volts, the SR_+ is resulted in (14). Similarly, for a large negative $-V_{\text{id}}$ it can be found that the output current is

$$I_{\text{out}}\approx-\frac{\beta_{4\text{A}}}{2}\left(\sqrt{\frac{\beta_{1\text{B}}}{2\beta_{4\text{B}}}}V_{\text{id}}+\frac{R_2\beta_{1\text{B}}}{4}V^2_{\text{id}}\right)^2 \tag{B-4}$$

where the minus sign denotes current entering the OTA. Thus, for a differential input step A, (15) is obtained.

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