An AC Input Inductor-Less LED Driver for Efficient Lighting and Visible Light Communication

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***Abstract*— This paper presents an ac-powered inductor-less light-emitting diode (LED) driver, which can simultaneously provide efficient illumination and data transmission capability by modulating light output. The proposed driver does not have passive components' speed limitation compared to the conventional switching converter-based driving solutions for visible light communication (VLC). Besides this, harmful low-frequency flicker is mitigated with an accurate 1/*x* circuit and the dimming compensation method. In addition, the digitalized power stage and controller utilized in the proposed driver can achieve smooth transitions among multiple current paths, while the keep-and-restore technique and auxiliary turn-on switch help to further increase the VLC data rate. The integrated circuit of the proposed driver is implemented and fabricated with a 0.35-μm, 120-V high-voltage CMOS process. Measurement results show that under a 110-V_{AC}, 60-Hz input, the peak efficiency of the proposed design is over 89% and the low-frequency flicker is reduced to below 10%. The driver supports up to 8-Mb/s on–off keying non-return-to-zero data transmission for a 1-m distance between the LED module and the receiver.**

***Index Terms*— 1/*x* circuit, ac–dc, converter free, flicker, inductor less, light-emitting diode (LED) driver, ON–OFF keying non-return-to-zero (OOK-NRZ) modulation, visible light communication (VLC).**

I. Introduction

LIGHT-EMITTING diodes (LEDs), as an emerging lighting source with a combination of low energy consumption, long lifetime, and improved physical robustness, are edging out their conventional counterparts, such as incandescent and fluorescent lights [1]. In addition to providing efficient illumination, LEDs can be powered up immediately and can be switched ON and OFF frequently without affecting their lifetime. Recently, this fast switching capability of LEDs has drawn increasing attention as it can offer high-speed free-space optical data transmission, which is known as visible light communication (VLC) [2]. The most remarkable advantage of the VLC technique is that, as shown in Fig. 1, it can be integrated into LED lamps, making it possible to offer general lighting and data transmission simultaneously, without the additional energy and cost of radio frequency (RF) antenna and transmitter. Therefore, it promises an energy- and cost-effective solution for applications such as indoor positioning and the Internet-of-Things. Compared to other wireless data communication approaches, VLC modulates and transmits data with light, which is not only intrinsically free of electromagnetic interference but also provides more secure indoor data transmission as light is easily blocked by walls. Moreover, with the RF spectrum becoming more and more valuable in this era of booming data, the utilization of VLC can also help to alleviate the increasing demand for limited spectrum resources.

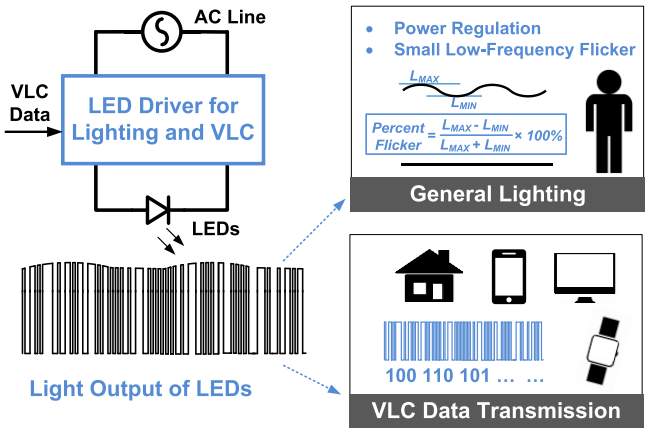

Fig. 1. Concept of LED driver for both illumination and VLC.

The driver circuit, as the essential part of a VLC LED lighting system, is employed to power up the LEDs and to switch them ON and OFF according to the pattern of VLC data [3]. Over a 1-Gb/s data rate has been demonstrated with white LEDs in the laboratory [4]. However, it was achieved without considering efficiency and cost. The practical implementation of a VLC LED driver concurrently achieving efficient lighting and high data-rate communication and without compromising other performance measures is still challenging. Several requirements should be satisfied at the same time. As shown in Fig. 1, for the purpose of general lighting, the average LED power as well as the brightness needs to be regulated while the harmful low-frequency optical flicker (<3 kHz) has to be minimized for the health consideration [5]. This is especially important in commonly used ac-powered lamps,

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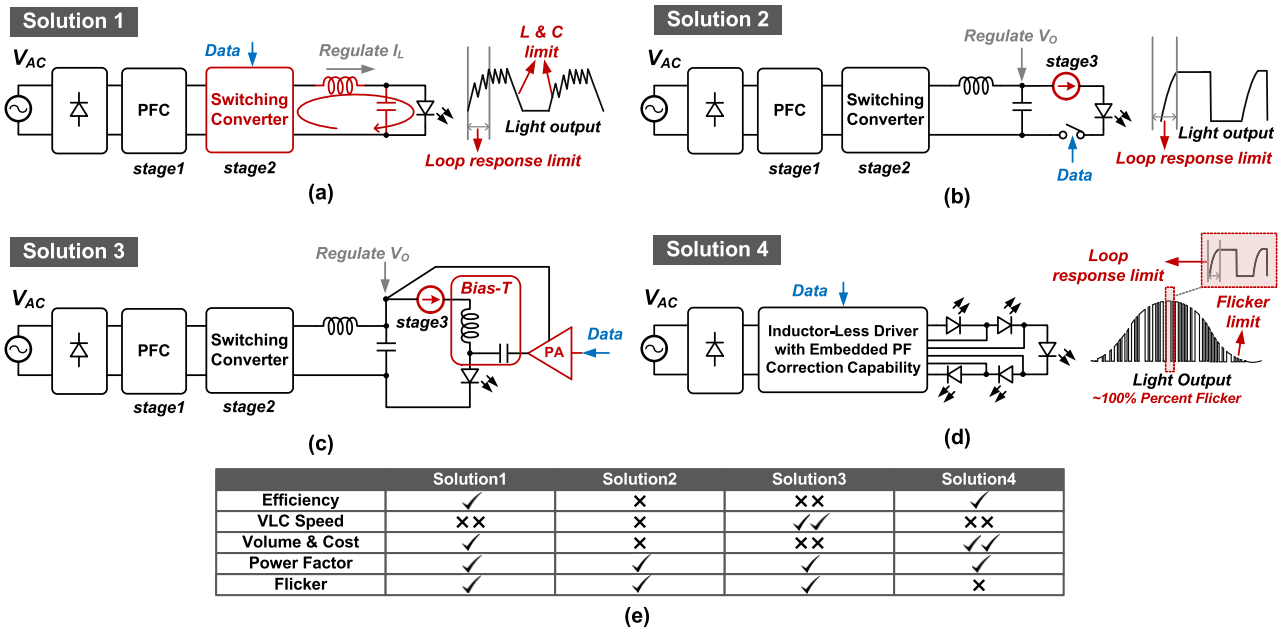

	Solution1	Solution2	Solution3	Solution4
Efficiency	✓	×	××	✓
VLC Speed	××	×	✓✓	××
Volume & Cost	✓	×	××	✓✓
Power Factor	✓	✓	✓	✓
Flicker	✓	✓	✓	×

(e)

Fig. 2. System diagrams of possible dual-purpose LED driving solutions with conventional VLC dimming methods. (a) Two-stage. (b) Three-stage. (c) Three-stage with power amplifier. (d) Conventional inductor-less driver. (e) Comparison table.

in which flicker at the double-line-frequency (100 or 120 Hz) dominates. Besides this, the power factor (PF) also needs to be considered for ac-powered systems because a poor PF will introduce considerable energy loss on the ac line [6]. Moreover, a high switching speed is always desired for the purpose of VLC, so the driver should not be the bottleneck for the entire data transmission channel. Meanwhile, it is equally important that the introduction of a VLC feature should not greatly affect other measures, such as volume, cost, and efficiency.

LED drivers with various topologies for general lighting applications have been reported [7]–[15]. However, most existing drivers can hardly support the VLC data transmission. Some of the conventional drivers with pulse width modulation (PWM) dimming capability can modulate the optical signal, yet with a limited data rate. Fig. 2(a) gives one typical example of a conventional ac-input LED driver. A two-stage topology is utilized for both a high PF and small flicker, while the LED current is well regulated with the control loop of the switching converter in the second stage. Thus, in order to modulate the brightness of LEDs, the whole second stage has to be enabled or disabled. As a result, the changing slope of the LED current is limited by both low-loop bandwidth and bulky inductor and capacitor, and the switching speed is below 10 kHz in most of these designs [8]. An alternative possible solution is shown in Fig. 2(b) to regulate the current with an extra current stage. The similar concept is employed in some previously reported designs [12], [13]. Thus, the passive components limitation can be eliminated and the data rate can be improved to over hundreds of kilohertz. However, the extra stage on the power delivery path will degrade the system's overall efficiency, and the switching speed will also be limited by the bandwidth of this current regulation stage. Fig. 2(c) illustrates another possible solution with the VLC data transmission technique employed in some research works for investigating the maximum data-rate capability of the LED [4]. The average power regulation and VLC data transmission are independently controlled with the help of a bias-tee and a power amplifier. Then, combined with the complicated RLC pre-equalization network to extend the modulation bandwidth of LED, an over hundreds of megahertz data rate can be achieved with this type of driver. However, low efficiency and high cost are preventing this method from being utilized in practical systems.

The conventional inductor-less LED driver (also named converter-free LED driver), as shown in Fig. 2(d), is widely adopted for general lighting [15]–[17]. In this driver, the LEDs are connected in series and can be bypassed by different power switches according to the input voltage. Therefore, at any time of each cycle, most of the power from the ac mains will be delivered to the LEDs. Although more LEDs have to be employed in this driver for providing enough voltage, it removes most of bulky and expensive off-chip components and has no switching losses. Thus, for the low to moderate power LED driving systems, it shows the advantages of good efficiency and compact size. Besides, by shaping the input current of this single-stage driver, PF correction functionality and average power regulation can be achieved simultaneously. Meanwhile, unlike switching converter-based topologies, the inductor-less driver is basically composed of several linear current regulation loops and requires no passive components for power regulation, so it can theoretically provide high switching speed for VLC. However, the light outputs of these drivers usually vary significantly at the double-line-frequency, which is not only a harmful optical flicker but also seriously undermines the effectiveness of data transmission.

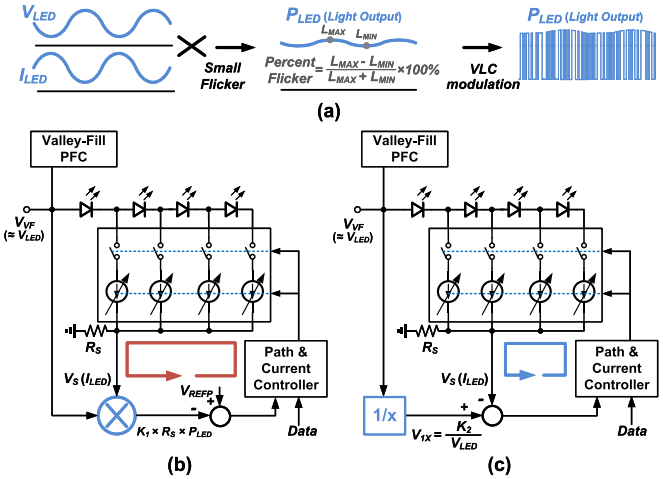

Fig. 3. (a) Concept of flicker reduction for inductor-less driver. (b) Conventional solution with a multiplier. (c) Proposed solution with a $1/x$ block.

Fig. 2(e) summarizes the advantages and drawbacks of the above LED driving solutions for VLC applications, showing that none of these drivers can meet the requirements of practical implementation. To address the limitations of the conventional solutions, this paper presents an ac-input inductor-less LED driver, with enhanced VLC switching speed and reduced flicker suitable for the integration of the data transmission feature with the inductor-less LED driver [19].

The rest of this paper is organized as follows. In Section II, several critical design considerations about flicker, smooth transition, and VLC speed enhancement are discussed. Possible solutions for each consideration are also presented and compared. In Section III, the overview of the architecture of the proposed inductor-less driver is given first and then the circuit implementation of each block is described. Finally, the experimental results are presented in Section IV, followed by the conclusion in Section V.

II. Design Considerations for Inductor-Less VLC LED Driver

A. Reduction of Low-Frequency Flicker

Low-frequency flicker is the primary constraint on the integration of VLC capability into inductor-less LED drivers. The significant variation of the light output increases the difficulty for the receiver to set the threshold for distinguishing data "1" from "0". For most conventional inductor-less drivers with around 100% flicker, as shown in Fig. 2(d), data recognition becomes almost impossible at the valley of the light output.

The light output intensity of a single LED is determined by its forward current, while in the inductor-less driver, various numbers of LEDs are powered up depending on the input voltage. Thus, the reduction of flicker for the inductor-less driver can be achieved by stabilizing the product of the LED current I_{LED} and the effective LED voltage V_{LED} (representing the enabled number of LEDs on the string), just as illustrated in Fig. 3(a). Thus, I_{LED} goes in the opposite direction to the V_{LED} changes.

Fig. 3(b) and (c) gives two possible approaches to implement this flicker reduction concept, with an example of four segments of LEDs. Since the LED current needs to be adjusted to deal with the flicker issue instead of achieving power factor correction (PFC), a valley-fill PFC circuit, is added in both approaches to improve the PF and to ensure the input voltage V_{VF} being high enough to turn-on at least the first segment of LEDs [20]. This valley-fill circuit is naturally not a perfect circuit for very high PF, while it can provide acceptable PF (>0.9) with advantages of simple topology and efficient volume, which is more suitable for the low to moderate power LED drivers. This simple PFC circuit only includes capacitors and diodes, so it will not introduce too much performance degradation in terms of efficiency and size compared to solution 4 in Fig. 2(d).

The approach utilized in Fig. 3(b) to reduce flicker is straightforward. A multiplier is employed to derive the product of the LED current and voltage [18]. Then, the feedback loop will clamp the output of the multiplier so as to be equal to a reference voltage V_{REFP}. Therefore, if the effective LED voltage is close to the input voltage V_{VF}, the LED power is kept as a constant and can be written as

$$P_{\mathrm{LED}} = \frac{V_S}{R_S} \times V_{\mathrm{LED}} \approx \frac{V_{\mathrm{REFP}}}{K_1 \times R_S} \tag{1}$$

where K_1 is the gain of the multiplier and R_S is the resistance of the current sensing resistor. Yet for VLC applications, this approach introduces one apparent drawback: with one slow stage inside the regulation loop, the multiplier will greatly degrade the loop bandwidth as well as the VLC data rate. Meanwhile, the demands for both high speed and high accuracy significantly increase the complexity and power consumption of the multiplier.

The alternative indirect approach in Fig. 3(c), which is proposed in this design, processes the input voltage with a $1/x$ circuit outside the regulation loop. Then, the output of the $1/x$ circuit V_{1X}, which is accurately inversely proportional to the input voltage V_{LED}, is taken as a reference voltage for the later current regulation loop. The LED power can be written as

$$P_{\mathrm{LED}} = \frac{V_S}{R_S} \times \frac{K_2}{V_{1X}} \approx \frac{K_2}{R_S} \tag{2}$$

where K_2 is the gain of the $1/x$ circuit. By comparing (1) and (2), it can be seen that both of these approaches can stabilize the LED power so as to be almost constant, while the second approach can have a faster loop, as the $1/x$ circuit is excluded from the regulation loop. Also, the $1/x$ circuit has little impact on the VLC speed; thus it can be designed with low bandwidth to save power. Therefore, the second approach is adopted in the proposed design.

B. Smooth Current Transition

In the inductor-less driver, the LED current needs to flow through different switches, depending on the input voltage. Therefore, how the current transits from one path to another becomes another crucial consideration.

Fig. 4(a) shows a conventional digital approach, in which the input voltage is constantly monitored and compared with

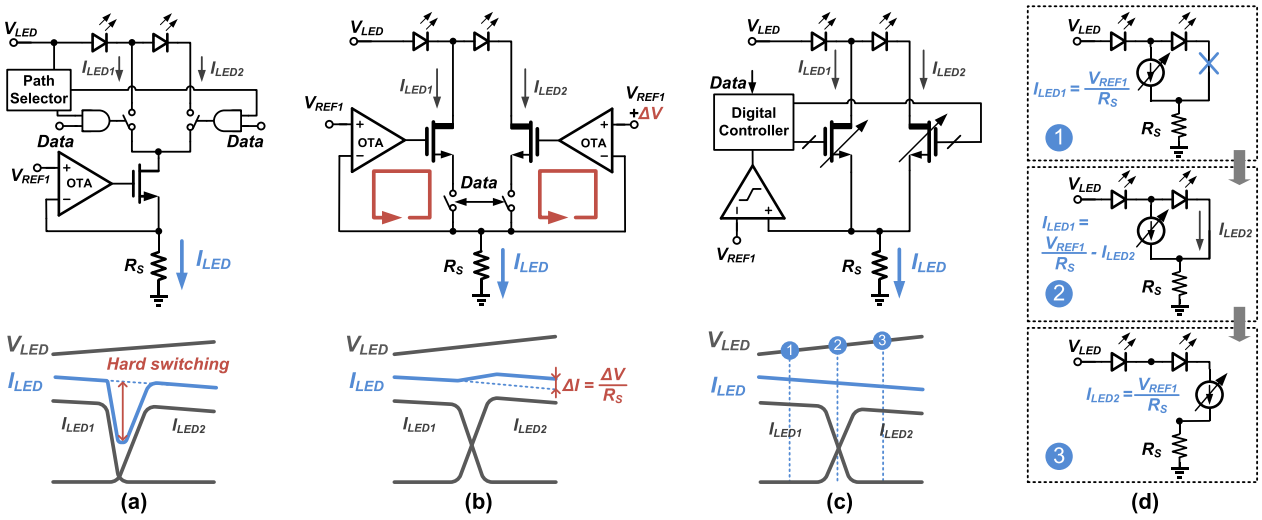

Fig. 4. Comparison of the current path transition approaches. (a) Conventional digital approach. (b) Conventional analog smooth transition approach. (c) Proposed digital smooth transition approach. (d) Three phases of smooth transition procedure.

the preset threshold voltages to make the switching decision. However, these preset voltages cannot perfectly match the LED voltages because of the process and temperature variations, resulting in hard switching with inevitable significant overshoot or undershoot of the LED current. This uncertainty during the transition will cause bit error for VLC data transmission, so it should be avoided.

The analog approach in Fig. 4(b) can well address the hard switching issue with the multi-loop configuration [15], [18]. As the input voltage changes, adaptive commutation of the LED current between different power transistors can be achieved without sensing the input voltage and the voltage of each segment of LEDs. However, when this approach is extended to a topology with N segments of LEDs, where N is usually larger than 6, another two issues need to be taken into consideration. First, in this analog approach, the transition order of the current paths is guaranteed by the small difference ΔV of the two reference voltages for the adjacent regulation loops, as shown in Fig. 4(b). Therefore, this ΔV should be designed to be large enough (e.g., 20 mV) to avoid the false-path transition caused by the input offset of the analog operational transconductance amplifier (OTA). Yet, a large ΔV is undesired for the flicker consideration, especially for the large N case, in which the difference between the first and the last reference voltage is $(N-1)\times\Delta V$. The second issue of this analog approach is the significant increase of the static power for N OTAs if the driver is used for high-speed data transmission. Unlike in the conventional inductor-less drivers, the OTAs need to be fast enough to catch up with the VLC input data, which can be up to several megahertz frequency. Therefore, the power losses on these OTAs cannot be ignored.

Fig. 4(c) illustrates the proposed approach for VLC applications, which takes the advantages of both the conventional digital and analog approaches. The power transistors are segmented into a group of cells, and the current is regulated by adjusting the equivalent resistance of the transistors with the digital bits provided by the digital controller. Then, the concept of adaptive commutation of the analog approach in Fig. 4(b) is mimicked and implemented with a digital way, which always provides a robust transition order with logic circuits and is more energy efficient compared with the analog approach.

The procedure of the smooth transition is illustrated in Fig. 4(d). When the input voltage is not high enough to light up the second segment of LEDs (phase 1), all of the LED current flows through the first path although the second path is fully activated. Then, when the input voltage goes up (phase 2), the LED current partially flows through the second path, and the controller still regulates the total current to avoid overshoot or undershoot. As V_{VF} continuously goes up, finally, all of the current will flowthrough the second path in phase 3 while the first path is fully turned off. This transition procedure is reversible and does not depend on the variation of the input voltage and the voltage of each LED segment.

C. Enhancement of Switching Speed

As described in Section I, despite the passive component limitation being eliminated in the inductor-less LED drivers with multiple linear regulation loops, the realization of a high data rate is still a challenge for the regulation loop with limited bandwidth. The data turning from "1" to "0" can usually be accomplished immediately by directly switching OFF all the power switches connected to the LEDs, while the procedure of turning from "0" to "1" has to slow down because the LED power needs to be regulated by a control loop when data are "1" for the purpose of general lighting. Thus, considering the stability, it always takes time for the loop to settle down to the expected state. For previously reported digitally controlled power management circuits, such as digital switching converters and digital low-dropout regulators [21]–[23], to speed up the transient response requires a high-speed quantization circuit (ADC or comparator) and, afterward, high-speed digital blocks. However, all of these circuits are power hungry. Besides this, to balance the transient

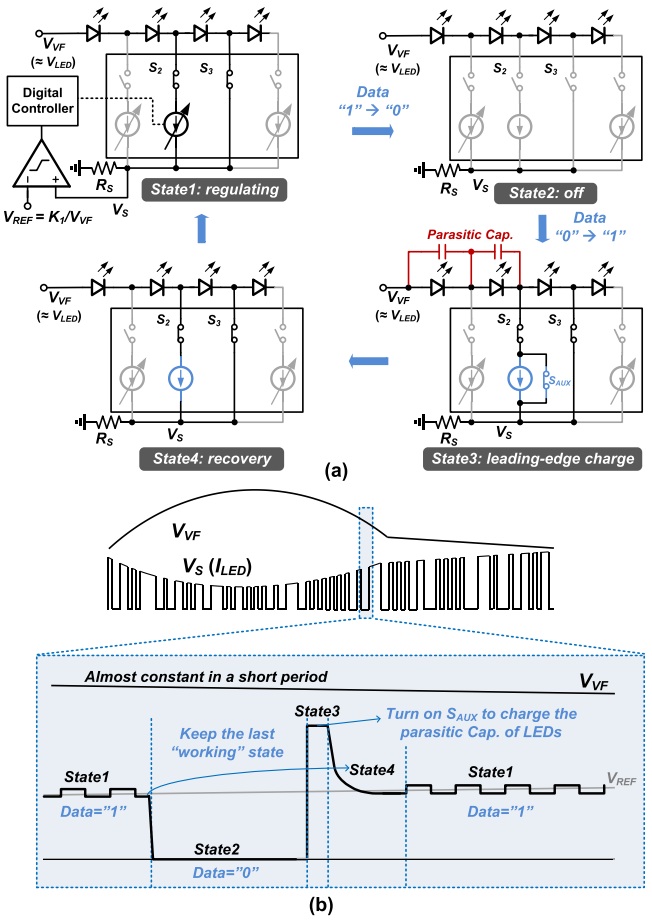

Fig. 5. Concept of switching speed enhancement with the keep-and-restore technique and the auxiliary switch. (a) Working states. (b) Key waveforms.

response time and system stability, complicated compensators and control schemes have to be employed.

The proposed digital controller in this design can achieve a faster turn-on speed efficiently with a keep-and-restore technique. Fig. 5 illustrates the principle with an example of a four-segment configuration. For a specified V_{VF}, two adjacent power switches (S_2 and S_3) are enabled in State1 (data = 1), while the LED current is regulated by adjusting the current flowing through S_2. It should be noted that in State1 in Fig. 5(a), the current may flow only through path2 or partially through path3. Then, as data changes from "1" to "0" (State2), S_2 and S_3 are shut down to turn off the LEDs, while the last regulation state is kept in the digital controller. In this case, the driver can be restored to its former "working" state right after the next data turns from "0" to "1" by simply enabling S_2 and S_3 without a loop control. This keep-and-restore technique can be effective because V_{VF} changes slowly compared to the VLC signal. Therefore, V_S can easily catch up with V_{1X} from the restored state even with 1-bit quantization and a slow digital integrator.

To further increase the turn-on speed, an auxiliary transistor S_{AUX} is enabled at the leading edge. The LEDs' parasitic capacitors can be charged in a short time (State3) with the large current through S_{AUX}. After State3, the controller will wait in the restored state for another clock cycle (State4) to let V_S be stable. Then, it will restart the regulation loop.

III. Circuit Implementation

A. System Architecture

Based on the earlier discussions, the system architecture of the proposed inductor-less LED driver with fast VLC capability and low optical flicker is illustrated in Fig. 6. For the off-chip part, a valley-fill circuit is placed after a bridge rectifier to provide a good PF [18], [20], while 12 segments of LEDs are connected to the on-chip power switches (S_1–S_{12}). As the input voltage V_{VF} varies, two of these switches are accordingly activated to provide paths for the LED current, ensuring that the effective LED voltage V_{LED_EFF} is always close to V_{VF}. Meanwhile, a charge-based $1/x$ circuit senses and processes the V_{VF} to derive the output V_{1X}, which is accurately inversely proportional to V_{VF}. Then, V_{1X} is taken as a reference voltage for the later current regulation loop.

The regulation is accomplished by adjusting the current paths and transistors' sizes with a digital controller. The VLC input data, modulated with ON–OFF keying non-return-to-zero (OOK-NRZ) code, enables the entire controller when it is "1", and deactivates the power switches when it is "0". For the case of only illumination, in which data are set to "1" without any signal modulation, the product of V_{LED_EFF} and I_{LED} is regulated so as to be almost constant regardless of the change of input voltage. While for the data transmission case, the LED current I_{LED} is modulated by the VLC signal, so the flicker will also be affected by the ratio of "1" and "0" in each short period. Thus, this design requires the ratio of numbers "1" and "0" to be fixed in each short period to ensure a small low-frequency flicker (<3 kHz). This can be achieved either by a coding method (e.g., Manchester coding) or by inserting a group of compensation codes "1" or "0" after a series of data.

B. Power Stage

Each power switch inside the digitalized power stage is implemented with a cascode structure, as illustrated in Fig. 7(a). A high-voltage transistor M_{HV} is put on the top to protect the low-voltage transistors and it will be switched when the VLC data changes or the LED current transition happens. Under M_{HV}, a low-voltage transistor M_{LV} is divided into 63 cells. By enabling a different number of cells, its equivalent resistance can be adjusted to regulate the LED current. Therefore, the 64 combinations, including the case that all cells are OFF, can be realized with a 6-bit logic signal before the local decoder for each current path. Besides this, an auxiliary transistor M_{AUX} is put in parallel with M_{LV}. It will be enabled in a short period (about 10 ns in this design) at each leading edge of the VLC signal to enhance the turn-on speed.

It should also be noted that, because the product of effective LED voltage and LED current is designed to be almost constant, the current capacity required for each power switch scales down from S_1 to S_{12}. The peak current for each switch can be easily calculated if the turn-on voltage for each segment of LEDs is determined. The sizes of the transistors inside each switch are also scaled based on the calculated peak current.

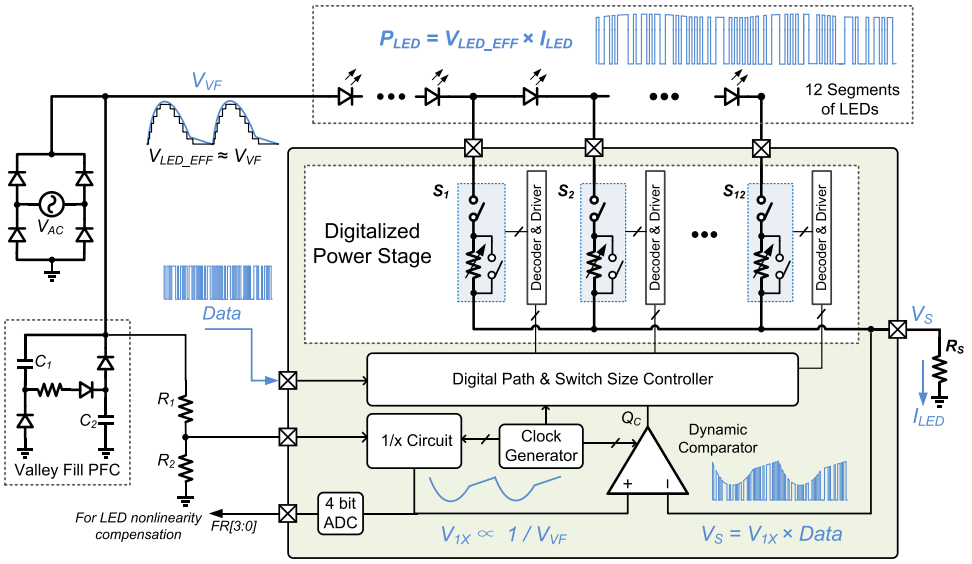

Fig. 6. System diagram of the proposed inductor-less VLC LED driver.

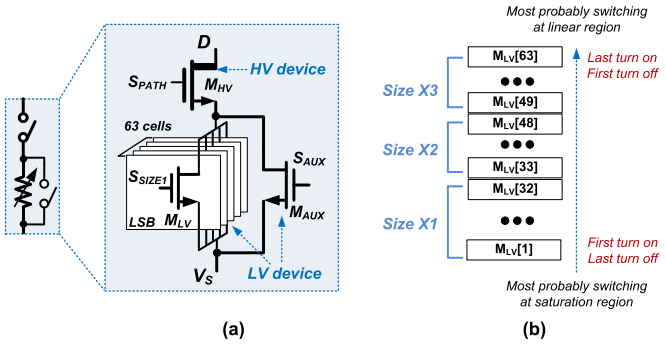

Fig. 7. (a) Implementation of the on-chip power switch with the cascode structure. (b) Implementation of cells of M_{LV} with weighted sizes.

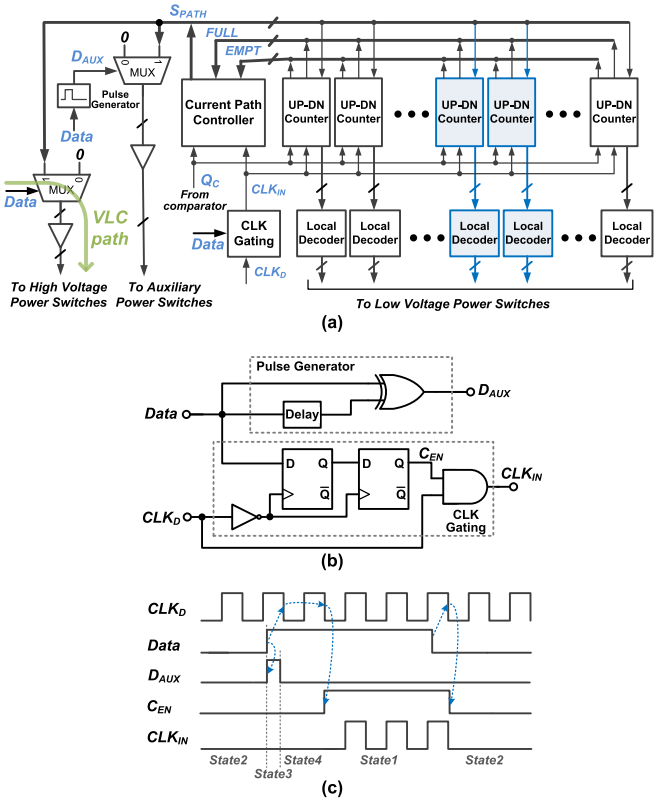

Fig. 8. (a) Implementation of digital controller. (b) Schematic of pulse generator and CLK gating block. (c) Key waveforms.

Inside each of the power switch, the 63 cells of M_{LV} are controlled by a thermometer code provided by the local decoder and only 1-bit cell will be switched ON or OFF for each clock cycle. As illustrated in Fig. 7(b), the weighted sizes are implemented for these cells because of the switching order. For example, the switching of cell M_{LV} [63] (the last cell to be turned on) most probably happens when the transistor locates at the linear region (small voltage drop on power switch), while the switching of cell M_{LV} [1] (the first cell to be turned on) usually happens when the transistor locates at the saturation region (large voltage drop on power switch). Therefore, in order to stabilize the LSB current changing for different conditions, M_{LV} [63] is designed with a larger size compared to M_{LV} [1].

C. Digital Controller

Fig. 8 shows the detailed implementation of the proposed digital controller. For the current regulation, a main current path controller is included for deciding which two high-voltage transistors (current paths) are enabled, while the corresponding bidirectional counters (UP-DN counters) and local decoders are enabled to change the sizes of the digitalized low-voltage transistors, thereby adjusting the LED current. With the help of the bidirectional counter, the transistor size will increase one bit when the output of the comparator Q_C is high and decrease one bit when Q_C is low. If the counter is full (empty), the main current path signal S_{PATH} will shift left (right) one bit. Accordingly, the enabled high-voltage transistors, counters,

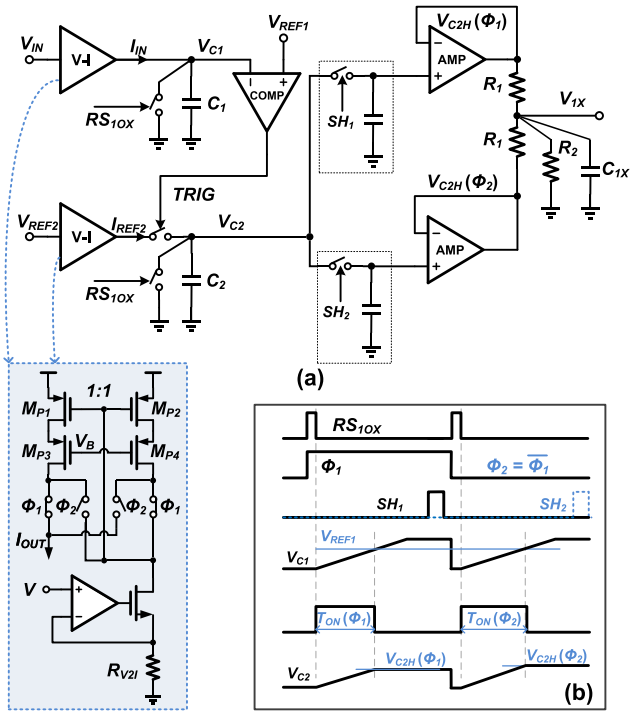

Fig. 9. (a) Schematic of $1/x$ circuit. (b) Key waveforms.

and decoders are all changed to ensure that the effective LED voltage is always close to $V_{\rm VF}$. It should be noted that the long metal routings between the digital controllers and the local decoders may cause time mismatch of the control signals, so gray code is adopted in this design to avoid spurious outputs.

For the data transmission, the VLC signal can explicitly reach the high-voltage power transistors with the fast VLC path (green line in Fig. 8) regardless of the states of the controller and the low-power transistors. All four of the states illustrated in Fig. 5 for the fast VLC transmission can be simply realized with a pulse generator and a CLK gating circuit, as shown in Fig. 8(b), while the diagrams of the key waveforms are also given in Fig. 8(c). After State2 (data = 0), at the leading edge of the VLC data, the auxiliary switch is enabled in a short period with signal $D_{\rm AUX}$ (duration of State3 is set to around 10 ns in this design) to further enhance the turn-on speed. The keep-and-restore technique is implemented with a CLK gating block, and an on-chip clock $\rm CLK_D$ is enabled or disabled by the asynchronized VLC signal data to obtain a local clock $\rm CLK_{IN}$ for the controller. Therefore, the working states of the low-voltage power transistors are kept when data are low, and can also be easily restored when data are turning from low to high. The D flip-flops are triggered by the negative edge of $\rm CLK_D$, avoiding the asynchronized data-caused glitches and providing one clock cycle for State4.

D. 1/x Circuit

Fig. 9 shows the schematic and key waveforms of the $1/x$ circuit utilized in the proposed driver. First, it converts the input voltage $V_{\rm IN}$ and a reference voltage $V_{\rm REF2}$ to $I_{\rm IN}$ and $I_{\rm REF2}$ with voltage-to-current (V–I) converters and uses the currents to charge two matched capacitors (C_1 and C_2) [24]. When V_{C1} reaches $V_{\rm REF1}$ within a period of time $T_{\rm ON}$, a triggered signal TRIG will stop the charging procedure, and the charges held on C_1 and C_2 can be written as

$$Q_{C1} = C_1 \times V_{\rm REF1} = T_{\rm ON} \times I_{\rm IN} \tag{3}$$

$$Q_{C2} = C_2 \times V_{C2} = T_{\rm ON} \times I_{\rm REF2}. \tag{4}$$

Therefore, if the same resistor ($R_{\rm V2I}$) and ratio of the current mirror ($M_{\rm P1}$:$M_{\rm P2}$ = 1:1) are used in both V–I converters and C_1 has the equal capacitance with C_2, from (3) and (4), the voltage held on C_2 can be re-written as

$$V_{C2} = \frac{V_{\rm REF1} \times I_{\rm REF2}}{I_{\rm IN}} = \frac{V_{\rm REF1} \times V_{\rm REF2}}{V_{\rm IN}}. \tag{5}$$

Since $V_{\rm REF1}$ and $V_{\rm REF2}$ are two reference voltages, V_{C2} is inversely proportional to the input voltage $V_{\rm IN}$, theoretically independent of the process, supply voltage, and temperature variations. Yet, there are still mismatches in this circuit affecting the accuracy of the output, especially for the procedure of V–I conversion. Even worse, the V–I converter needs to operate properly in a large input range while the current mismatch depends on its bias condition. A lower $V_{\rm IN}$ leads to a smaller overdrive voltage of $M_{\rm P1}$ ($M_{\rm P2}$) and higher inaccuracy of current mirroring. In order to solve above issues, the transistors in the current mirror are swapped during each reset period. Then, $V_{\rm C2H}$ in two configurations are sampled alternately and held separately as $V_{\rm C2H}$ (Φ1) and $V_{\rm C2H}$ (Φ2). Then, with the help of the amplifiers and resistor dividers, these two sampled voltages are averaged and scaled down to V_{1X}, and can be written as

$$\begin{aligned} V_{1X} &= \frac{2R_2}{2R_2 + R_1} \cdot \frac{V_{\rm C2H}(\Phi 1) + V_{\rm C2H}(\Phi 2)}{2} \\ &\approx \frac{2R_2}{2R_2 + R_1} \cdot \frac{V_{\rm REF1} \times V_{\rm REF2}}{V_{\rm IN}}. \end{aligned} \tag{6}$$

Then, the input-dependent mismatch can be greatly reduced with this modified V–I converter. Although it takes more clock periods to get the accurate final output, the $1/x$ circuit has adequate speed to catch up with the slow input voltage $V_{\rm IN}$. To verify the effectiveness of $1/x$ circuit with the modified V–I converter, Monte Carlo simulation with 100 runs is conducted and the results are shown in Fig. 10(a). When the input signal $V_{\rm IN}$ varies from 0.5 to 1.5 V, the 100 curves of the normalized product of $V_{\rm IN}$ and V_{1X}, representing the gain and linearity of the $1/x$ circuit, are kept in a limited range with a variation less than $\pm 2\%$ for the worse case. For comparison, the simulation results with the conventional V–I converter are also given in Fig. 10(b). The proposed approach achieves up to 3 times improvement in the gain stability.

E. Dynamic Comparator

In order to provide fast 1-bit quantization for the digital controller, a high-speed comparator is required in the proposed inductor-less driver. Meanwhile, the offset of the comparator should be small enough compared to V_{1X} (can be below

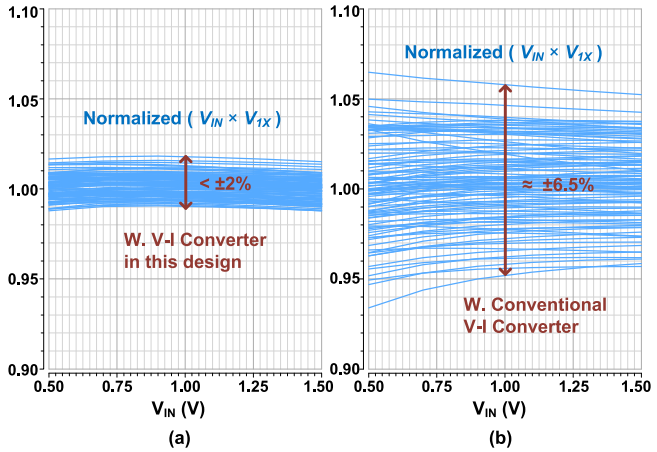

Fig. 10. Monte Carlo simulation results of the normalized product of $V_{\rm IN}$ and V_{1X} (a) with V–I converter in this design and (b) with conventional V–I converter.

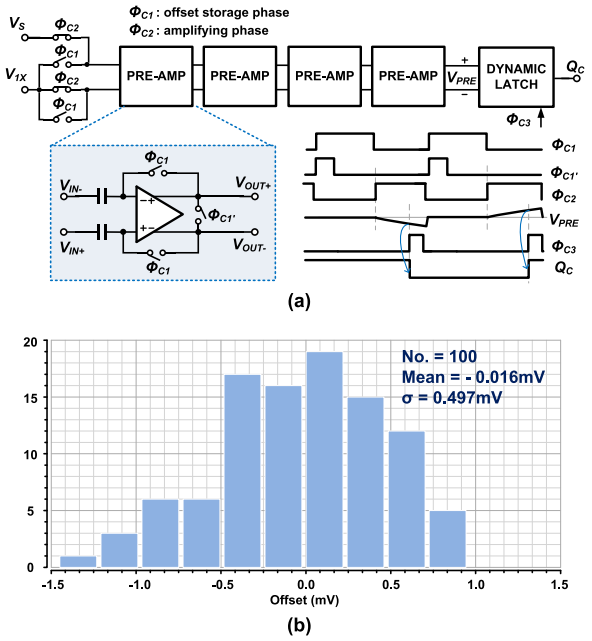

Fig. 11. (a) Schematic of auto-zero dynamic comparator. (b) Monte Carlo simulation results of input offset of the dynamic comparator.

100 mV in this design). Otherwise, the uncertainty of this offset may cause the increase of the flicker. Fig. 11(a) shows the auto-zero dynamic comparator employed in this design and the key waveforms. Four-stage pre-amplifiers are put before the dynamic latch to enhance the bandwidth for the fast regulation, while the auto-zero technique is used for each pre-amplifier to reduce the offset. In the offset storage phase (Φ_{C1}), each of the pre-amplifiers is set to the unity-gain negative feedback configuration so its offset is stored on the input capacitors. Then, this stored voltage is turned upside down and superimposed on the input voltage during the amplifying phase (Φ_{C2}), cancelling out the input offset in each stage. At the end of Φ_{C2}, the dynamic latch samples the differential output of the fourth stage $V_{\rm PRE}$ and converts it into

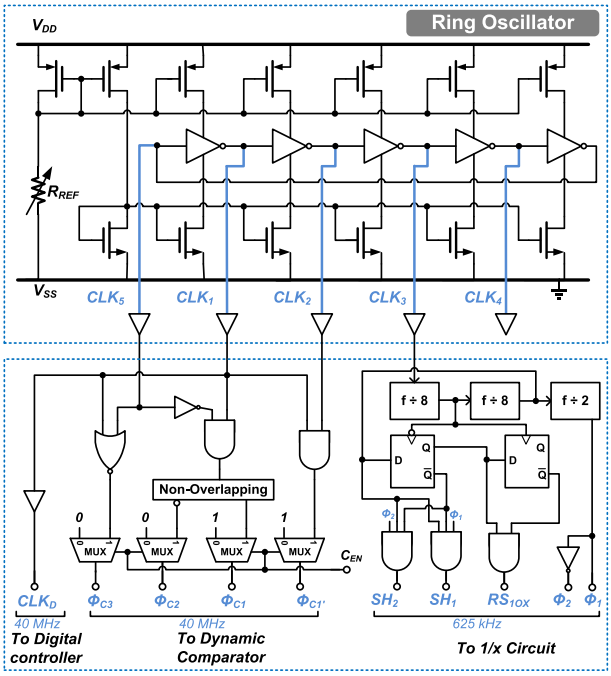

Fig. 12. Clock generator.

the digital output Q_C. Fig. 11(b) illustrates the distribution of the input offset of the comparator for the Monte Carlo simulation with the 40-MHz clocks. It can be seen that the standard deviation of the input offset is below 0.5 mV in this case. As a result, V_S can precisely track V_{1X} to avoid the degradation of flicker.

F. Clock Generator

Fig. 12 shows how to generate the clocks for the on-chip blocks with varied demands for frequencies and phases. A five-stage current-starved ring oscillator is employed to provide the fast-interleaved clocks ($\rm CLK_1$–$\rm CLK_5$). In this design, the clock frequency is adjusted to 40 MHz with an off-chip variable resistor $R_{\rm REF}$. Among the clocks, $\rm CLK_1$ is utilized for the synchronized digital controller, while three clocks can generate more phases for dynamic comparator with the logic gates and the non-overlapping circuit. The clocks for the digital controller and dynamic comparator are all with the frequency of 40 MHz. For the 1/x circuit, the requirement for the working frequency is much smaller, so the clock is first put into the frequency dividers. Then, with the help of flip-flops and logic gates, the slow clocks with the frequency of 625 kHz, including Φ_1, Φ_2, $\rm SH_1$, $\rm SH_2$, and $R_{\rm S1OX}$, are generated for the implementation of 1/x circuits.

IV. Measurement Results

The proposed driver IC was fabricated with a 0.35-μm, 120-V CMOS process. Fig. 13 shows the chip micrograph, and the occupied area is about 4.2 $\rm mm^2$. Fig. 14 illustrates the PCB of the proposed driver board and LED array board. Besides the driver IC, the proposed driver board also includes an off-chip diode bridge and a valley-fill circuit. It can also be seen

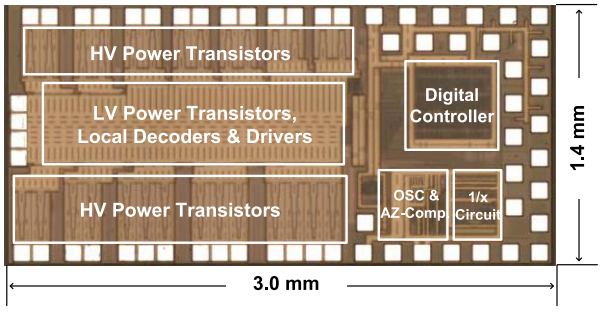

Fig. 13. Chip micrograph of the proposed driver IC.

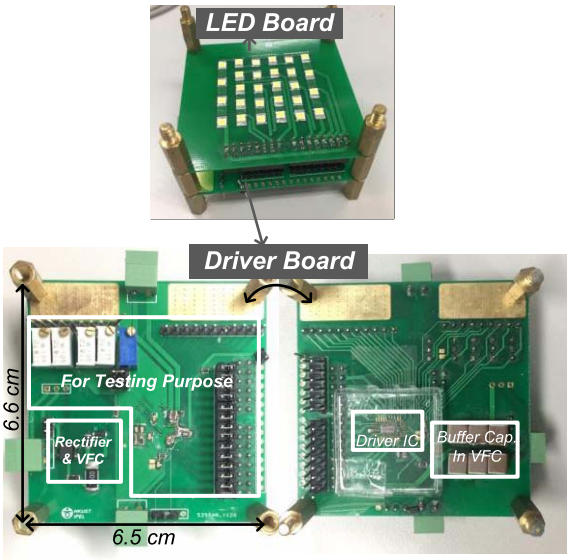

Fig. 14. PCB of the proposed driver board and LED array board.

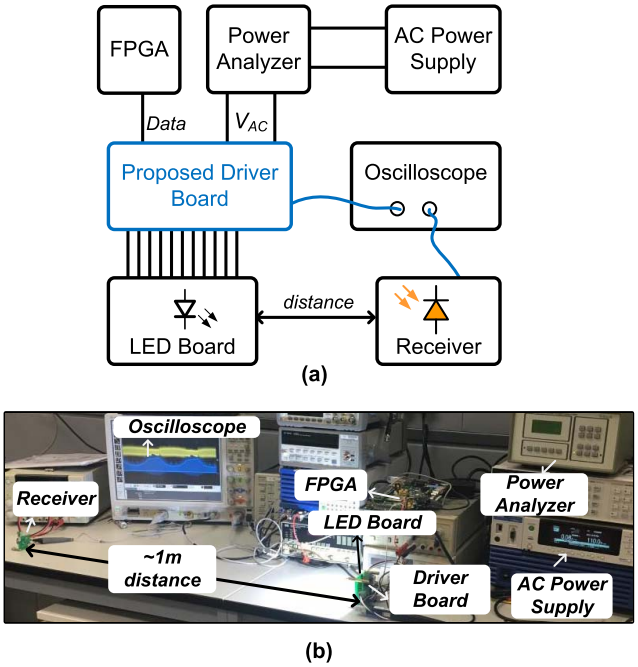

Fig. 15. Test setup. (a) Diagram. (b) Photograph.

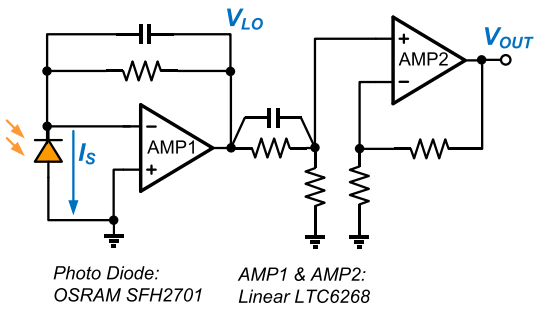

Fig. 16. VLC receiver.

that most of the PCB area of this demonstration driver board is utilized for the testing purpose. The LED board, including 28 commercial cool-white 6-V LEDs connected in series [25], is employed as both the lighting source and the VLC data transmitter. The LED string is divided into 12 segments based on the segment optimization method in [18], and the numbers of LEDs for each segment are 9, 1, 1, 1, 1, 2, 2, 2, 2, 2, 2, and 3, respectively. For each of the 6-V LED, the measured parasitic capacitance is around 150 pF at 0 V and around 500 pF at the operation voltage. Compared to the conventional switching converter-based drivers, more LEDs need to be used in this design, which will increase the cost and volume of the LED board. Yet, it should also be noted that the LED board in Fig. 14 is built for the convenient demonstration of the proposed dual-purpose driver, so its volume and cost have great potential to be scaled down by integrating all the LEDs in one package, as what has been demonstrated in [17]. Fig. 15 shows the diagram and photograph of the test setup for the proposed inductor-less driver. The NRZ-OOK data are encoded and provided by an field programmable gate array (FPGA) and then sent to the driver. Fig. 16 illustrates the VLC data receiver used in the setup, including a fast photodiode and two stages of high-speed amplifiers. The prototype VLC driver is designed and tested under 110-V_{AC}, 60-Hz input (peak voltage is around 155 V after the rectifier), while the idea of integration of VLC data transmission with the inductor-less driver and all of the techniques utilized in this design also applies to other voltage applications, e.g., 220 V_{AC}, with a suitable high-voltage process. The driver IC is powered by an external 3.3-V dc supply for the ease of testing since it is not the focus of this design. An on-chip regulator can be easily implemented to replace this dc supply in the future design [18].

First, the proposed inductor-less driver is measured at the condition without data transmission, which means that the VLC input data are set to "1." Fig. 17(a) shows the measured key waveforms. It can be seen that, as V_{VF} varies up and down, the voltage on the current sense resistor Vs, well-matched with the output of the $1/x$ circuit V_{1X}, goes in an opposite direction to V_{VF}. The product of V_{VF} and V_S is kept almost constant, representing a small variation on the total LED power. However, as shown in Fig. 17(a), the measured light output V_{LO} has around 12.2% flicker. Apparently, that is a significant variation compared to the waveform of the product of V_{VF} and V_S. Two contributors are responsible for this inconsistency. The subsidiary contributor is the difference of V_{VF} and V_{LED_EFF},

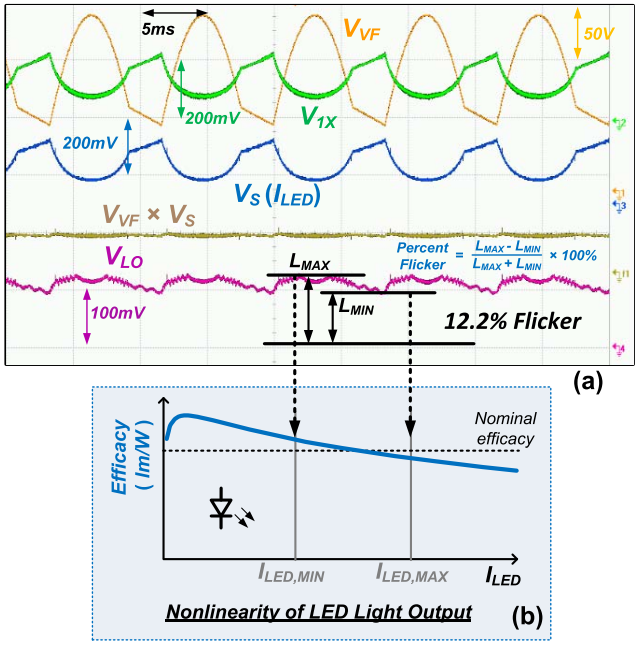

Fig. 17. (a) Measured key waveforms without data transmission and dimming compensation. (b) Diagram of LED efficacy versus LED current.

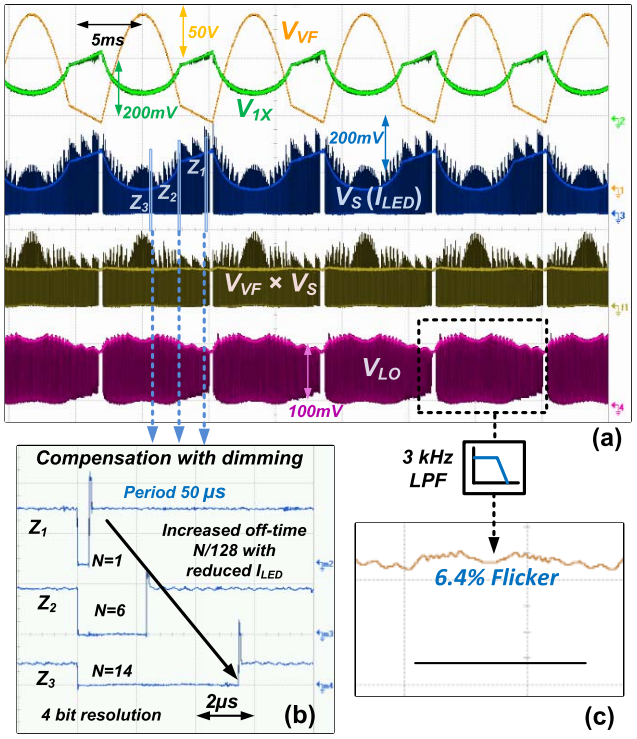

Fig. 18. (a) Measured key waveforms with dimming compensation and without data transmission. (b) Zoomed-in view waveforms of V_S. (c) Waveform of the filtered light output.

resulting in glitches in the light output, while the second contributor is the degradation of the LED light efficacy with the increased current, as shown in Fig. 17(b), having a more significant impact on the flicker.

The fast dimming capability provided by the proposed driver can be naturally utilized to further reduce this

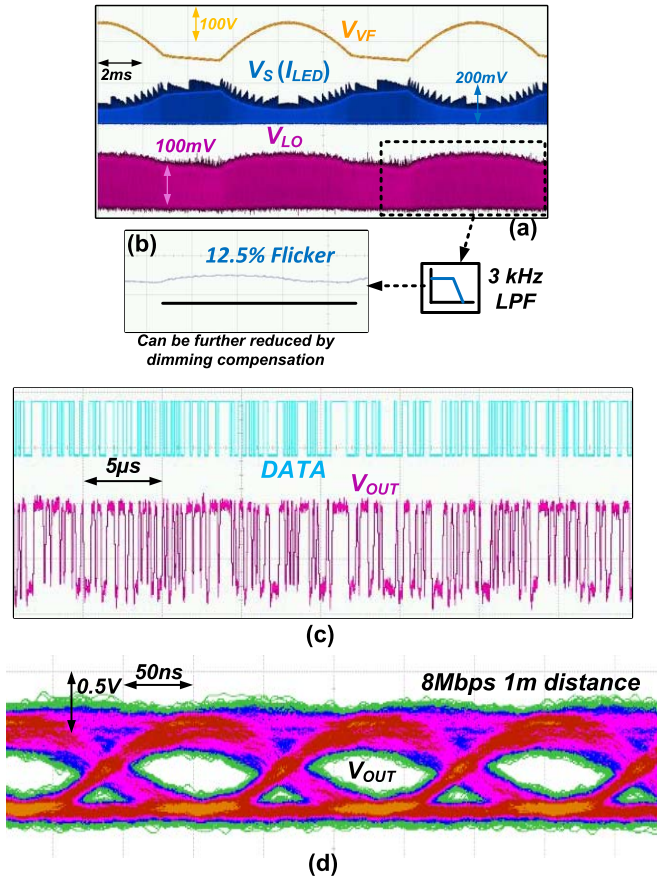

Fig. 19. (a) Measured key waveforms with data transmission. (b) Waveform of the filtered light output (c) Zoomed-in view waveforms of input VLC data and light output. (d) Eye diagram.

non-linearity-introduced flicker. As illustrated in Fig. 6, the V_{1X} is digitalized with an ADC, which is implemented with a simple single-slope architecture and has 4-bit output FR [3:0]. Then, the digital output is fed back to the controller to adjust the PWM dimming duty ratio. As a result, the LEDs are switched OFF for a longer time when the current goes down. Fig. 18(a) illustrates the measured key waveforms with a 20-kHz dimming CLK for flicker reduction, while Fig. 18(b) provides the zoomed-in view waveforms of the LED currents at different periods of one ac line cycle. As shown in Fig. 18(c), though this 20-kHz dimming can be measured in the light output, it has little impact on human health. In fact, the flicker is almost halved with this method as $V_{\rm LO}$ is filtered by a 3-kHz low-pass filter.

Fig. 19 shows the measurement results of the proposed driver for both lighting and data transmission. A pseudorandom binary sequence with the length of 2^8-1 bits is generated from the FPGA and sent to the proposed driver. The measured $V_{\rm VF}$, V_S, and $V_{\rm LO}$ at 110-$V_{\rm AC}$ input with 8-Mb/s data rate are illustrated in Fig. 19(a). The filtered light output is also given in Fig. 19(b), indicating about 12.5% flicker. By inserting a series of compensation codes "1" or "0" after the VLC signal, the flicker can also be further reduced with dimming compensation, but the effective data rate will be affected by several percentage points. Fig. 19(c) shows the comparison of the input VLC data with the receiver output, while Fig. 19(d)

TABLE I
PERFORMANCE COMPARISON WITH PREVIOUS AC-INPUT LED DRIVERS

	ISSCC2013 [9]	JSSC2012 [10]	TPEL2012 [11]	ISSCC2013 [15]	ISSCC2016 [16]	JSSC2017 [18]	This Work
Process	0.35-μm CMOS	0.35-μm BCDMOS	Discrete Components	1-μm 450V BCDMOS	0.18-μm 85V BCDMOS	0.35-μm 120V CMOS	0.35-μm 120V CMOS
Chip Area	22.1 mm^2	0.75 mm^2	-	9.64 mm^2	0.77 × 3 mm^2	1.85 mm^2	4.2 mm^2
Driver Type	Buck Resonant Switching Converter	Fly-back Switching Converter	Fly-back & Buck/Boost Switching Converter	Inductor-Less Linear	Inductor-Less Linear	Inductor-Less Linear with Valley Fill PFC	Inductor-Less Linear with Valley Fill PFC
Off-chip Power Switch	HV GaN-FET & LV MOSFET	800 V MOSFET	600 V MOSFET × 3	No	No	No	No
Magnetics	Inductors (850nH & 12μH)	Transformer (1.8mH)	Transformer (80μH) Inductors (500μH & 30μH)	No	No	No	No
Max. Power	22 W	12 W	33.6 W	22 W	34 W	7.8 W	8 W #
Input Voltage	110 V_{AC}	180-260 V_{AC}	90-264 V_{AC}	110/220 V_{AC}	120 V_{AC}	110 V_{AC}	110 V_{AC}
Power Factor	0.96	0.96	> 0.99*	0.99	0.996	0.925	0.904
Percent Flicker	~ 100 %*	~ 30 %*	< 3 %*	~ 100 %*	~ 100 %*	17.3 %+	6.4 %+
Peak Efficiency	89.4 %	85 %	85.5%	93.4 %	83 %	87.6 %	89.2 %

* Not reported in the paper. Estimated from the measured waveforms.
+ Measured with photodiode.
# 28 of 1W LEDs are utilized for testing.

TABLE II
PERFORMANCE COMPARISON WITH PREVIOUS DUAL-PURPOSE LED DRIVERS

	TPEL2014 [13]	TIA2015 [26]	SR2016 [27]	VLSIC2015 [12]	This Work
Process	Discrete Components	Discrete Components	0.5-μm 50V CMOS	0.35-μm 20V CMOS	0.35-μm 120V CMOS
Chip Area	N.A.	N.A.	2.41 mm^2	8 mm^2 *	4.2 mm^2
Driver Type	LLC Switching Converter	Buck Switching Converter	Buck Switching Converter	Boost Switching Converter	Inductor-Less Linear
Input Voltage	340-400 V_{DC}	110/120 V_{AC}	50 V_{DC}	3-5 V_{DC}	110 V_{AC}
Magnetics	Transformer (332μH) Inductor (47.6μH)	Inductor (470μH)	Inductor (18μH)	Inductor (4.7μH)	No
Modulation Scheme	VPPM	VPPM	VPPM	VPPM & OOK	OOK
Max. Power	80 W	5.8 W	4.59 W	5.4 W	8 W #
Data Rate	47 kbps	2 Mbps	1 Mbps	266.6 kbps	8 Mbps
Distance	10 m	1 m	1 m	~ 2 m	1 m
BER	$<10^{-7}$ @4m, $<10^{-5}$ @10m	Not Reported	Not Reported	<10% @2.2 m	$<10^{-6}$ @1m
Peak Driver Efficiency +	95.1%	88.6 %	85.8 %	92 %	89.2%

* Including 2.25 mm^2 chip area for baseband.
+ All the results for peak efficiency are at the full load condition without data transmission.
# 28 of 1W LEDs are utilized for testing.

illustrates the measured eye diagram at a 1-m distance with bit error rate (BER) below 10^{-6}. The data rate is mainly limited by the bandwidth of the phosphor-based white LED. If a high-quality communication with the stricter BER is required, redundancy can be added in the coding for error correction while the maximum data rate will also be reduced in this case.

Table I shows the comparison of the performance of this paper with prior art ac-input LED drivers for lighting purposes only. The proposed design rules out the bulky off-chip power transistors and magnetics, which are widely utilized in ac LED drivers with complex topologies based on switching converters, so it is more effective in terms of system volume and cost. The proposed driver achieves competitive efficiency (89.2%) and at the same time successfully addresses the low-frequency flicker issue. More than half of the power losses for the proposed driver are wasted on the valley-fill circuit and the rectifier, while the rest of the power loss is due to the voltage drop on the power switches. The measured PF (0.904), determined by the topology of the valley-fill circuit, is not as high as those conventional inductor-less drivers, but it is sufficient for meeting most of the regulations for the low to moderate power LED drivers.

The comparison of this paper with previous dual-purpose LED drivers is also summarized in Table II. The proposed design can be directly powered from the ac source, which is more applicable for practical applications. Furthermore, both high-efficiency and a high data rate are achieved without increasing of the hardware complexity and system expense.

V. CONCLUSION

An 8-W, 89.2% efficiency inductor-less LED driver is demonstrated for simultaneous illumination and VLC applications. The proposed topology rules out the bulky magnetics

in the design and eliminates the passive components that introduced data transmission speed limitation. An 8-Mb/s peak data rate can be achieved with two turn-on speed enhancement techniques. Meanwhile, an accurate $1/x$ circuit and dimming compensation method help to mitigate the harmful low-frequency flicker to below 10%. This design can be extended from binary communication (OOK) to a multi-level coding scheme, which can further increase the data rate, with only a small increase in the complexity of the digital controller.

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