A Dual-Loop Synthesizer With Fast Frequency Modulation Ability for 77/79 GHz FMCW Automotive Radar Applications

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***Abstract*— The implementation of wideband mm-wave radars for automotive applications necessitates wideband, fast, and precise linear frequency modulation generation. In this paper, we propose to use dual-loop phase-locked loop (PLL) architecture for this task. The frequency modulation dynamics are analyzed for this architecture. The results are employed to implement a SiGe BiCMOS fully integrated 75–83 GHz frequency-modulated continuous-wave synthesizer. Performance enhancements were achieved by utilizing the bulk-drain parasitic variable capacitance of P-channel transistors, embedded in a gm-boosted Colpitts VCO, for frequency control. This mechanism together with the dual-loop PLL architecture provides low loop bandwidth variation over the whole output frequency range, −97 dBc/Hz phase noise at 1-MHz offset, and maximal modulation rate of 100 GHz/ms.**

***Index Terms*— 79 GHz, automotive, dual loop, fractional-*N*, frequency-modulated continuous wave (FMCW), low noise, millimeter-wave radar, phase noise, phase-locked loop (PLL), radar, SiGe, *W*-band.**

I. Introduction

WIDEBAND mm-wave radars are gaining popularity in automotive applications in recent years. This is due to their inherent superiority in harsh weather conditions and low cost. Using a frequency-modulated continuous-wave (FMCW) technique, mm-wave radars provide high distance resolution and precise velocity measurement, both critical to short- and medium-range detection [1]. They also provide superior spatial resolution, compared to lower frequency radars, which are essential in long-range detection.

In order to take advantage of these features the ability to generate fast and linear frequency modulation over a wide frequency range is required. Designing a synthesizer for mm-wave applications evokes an additional challenge. At high carrier frequencies phase noise worsens, limiting the signal-to-noise ratio of the radar system in the presence of strong clutter, which is typical to automotive scenarios [2].

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When designing an FMCW phase-locked loop (PLL), therefore, a delicate balance must be maintained between different tradeoffs. Maintaining this balance imposes stringent requirements on synthesizer loop design including precise bandwidth and settling response. However, it is challenging to maintain constant loop properties due to variations in component characteristics, especially in the voltage-controlled oscillator (VCO) gain, across the required wide frequency range. Moreover large changes in the loop properties during frequency modulation can hinder modulation linearity even after initial settling.

Several approaches were proposed to mitigate the bandwidth variation. Loop-gain calibration irrespective of whether digital [3] or analog [4], although efficient in most cases, is not applicable for frequency modulation as the loop operation point changes rapidly through the modulation. Alternatively, VCO frequency response can be linearized using averaging varactors [4] or a combination of PMOS and NMOS varactors [5]. However, such linearization is quite delicate and can degrade in process or temperature variation. Another approach is using a dual-loop PLL architecture with wideband integral path and narrowband proportional path. This architecture was used, in [6], in order to achieve constant bandwidth across wide frequency range and in [7] to simplify loop calibration. The inherent robustness to integral path VCO gain variation and stable bandwidth, due to constant biasing of the proportional path, nominates this architecture to be a good candidate for frequency-modulated synthesizers.

An analysis of single-loop PLL dynamics in the context of linear frequency modulation was presented [8]. In this paper, we show a detailed analysis of the dual-loop PLL dynamics in the context of wideband linear frequency modulation and present the implementation of a fully integrated 77/79 GHz dual-loop FMCW synthesizer.

A key component in the implemented system is a low-noise dually controlled gm-boosted Colpitts VCO, which uses the bulk voltage of its cross-coupled pair for secondary frequency control.

Bulk voltage is commonly used for frequency control in low-voltage inverter ring VCOs utilizing its effect on the threshold voltage of the VCO stage transistors [9] or the current source [10], thus changing the stage delay. In *LC* VCOs, it was recently used for fine frequency tuning in a high-frequency oscillator utilizing the variability of the bulk–drain parasitic capacitance of the cross-coupled pair [11]. In this paper, we propose using the latter in addition to a conventional

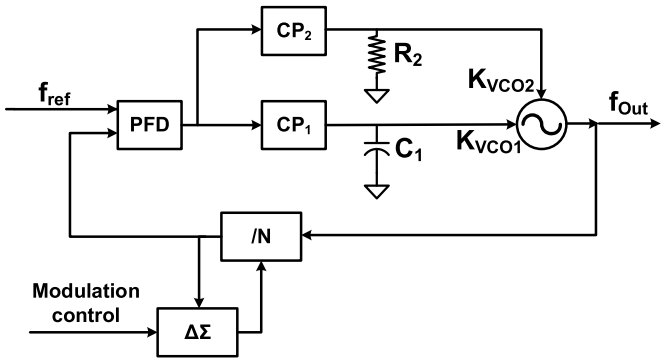


Fig. 1. Block diagram of type-II 2nd-order dual-loop fractional-N PLL.

varactor, thereby, providing a low-gain secondary frequency control method.

This paper is organized as follows. In Section II, the dynamics of a general dual-loop PLL during a linear frequency modulation are described. Section III presents the dually controlled VCO that was developed for the dual-loop PLL implementation. The complete FMCW synthesizer system is described in Section IV. In Section V, the measurement results of the system are reported. Finally, conclusions are drawn in Section VI.

II. Frequency Modulation Dynamics in a Dual-Loop PLL

To determine the tradeoffs in the synthesizer design it is important to model not only the PLL characteristics at constant frequency but also its response to frequency modulation.

The response to linear frequency chirp was studied, in [8], for a standard single-loop 2nd-order PLL using a linearized model. Here, we adapt the results to a dual-loop design and discuss the effect of VCO gain variation on both architectures.

We consider a dual-loop fractional-N PLL as presented in Fig. 1. It consists of a phase-frequency detector (PFD) for which output is connected to two control paths, each containing a charge pump (CP) and a passive filter. Both paths are connected to a dually controlled VCO. The VCO output is fed back to a fractional-N divider closing the control loop. The frequency modulation is generated by sweeping the division ratio of the fractional-N divider.

In general, the loop filters of the paths can be arbitrary. However, in most dual-loop designs, one of the paths is designed to have an integral transfer function at low frequencies and the second to have a proportional transfer function at low frequencies.

This configuration, together with wide VCO tuning range at the integral path and narrow tuning range at the proportional path, provides several advantages. It provides low sensitivity to CP and filter noise due to the low VCO gain at the proportional path. It also provides stable loop bandwidth across the whole tuning range since the voltage at the proportional control path is quite constant in steady state [6]. In the context of wideband frequency modulation, the latter is very important as it allows approximate linear time-invariant analysis of the loop dynamics as follows.

A. Dual-Loop PLL Frequency-Domain Linear Model

First, we describe the transfer functions of both paths with the filters shown in Fig. 1. The transfer function of the integral path is

$$H_{\text{path1}}(s) = \frac{I_{\text{CP1}}}{sC_1} \tag{1}$$

where I_{CP1} is the CP current of the integral path and the transfer function of the proportional path is

$$H_{\text{path2}}(s) = I_{\text{CP2}} R_2 \tag{2}$$

where I_{CP2} is the CP current of the proportional path.

Both transfer functions are multiplied by their respective VCO gains: K_{VCO1} and K_{VCO2} (measured in hertz to volt), combined and substituted into the well-known PLL linearized model [12]. The result is the following PLL loop transfer function:

$$\text{GH}(s) = \frac{I_{\text{CP1}} K_{\text{VCO1}} \left(1 + \frac{s}{\omega_z}\right)}{s^2 C_1 N} \tag{3}$$

where N is the PLL division ratio and ω_z is the zero produced by combining both control paths, and is determined by the following:

$$\omega_z = \frac{I_{\text{CP1}}}{I_{\text{CP2}}} \frac{K_{\text{VCO1}}}{K_{\text{VCO2}}} \frac{1}{R_2 C_1}. \tag{4}$$

B. Response to Linear Frequency Ramp

A frequency ramp can be introduced to the PLL by modulating the reference frequency or by changing the $\Delta\Sigma$ input. When using the latter method, it is important to take into account the signal transfer function of the $\Delta\Sigma$ modulator. Here, we assume this transfer function is unity, as is the case in MASH modulators.

Assuming a ramp of amplitude ΔF_{ramp} and duration ΔT_{ramp} is required, the needed $\Delta\Sigma$ input modulation in s domain is

$$\Delta N(s) = \frac{\Delta F_{\text{ramp}}}{\Delta T_{\text{ramp}}} \frac{1}{f_{\text{ref}} s^2} \tag{5}$$

where f_{ref} is the reference clock frequency. The frequency deviation from the ideal ramp at the PLL output can be expressed using (5), and the PLL closed loop transfer function resulting in

$$e(s) = f_{\text{out}}(s) - f_{\text{out}}^{\text{ideal}}(s) = \frac{\Delta F_{\text{ramp}}}{\Delta T_{\text{ramp}} s^2} \frac{-1}{1 + \text{GH}(s)}. \tag{6}$$

Substituting (3) into (6) and with some manipulation, we arrive at the following:

$$e(s) = \frac{\Delta F_{\text{ramp}}}{\Delta T_{\text{ramp}}} \frac{-1}{\left(\omega_n^2 + 2\zeta\omega_n s + s^2\right)} \tag{7}$$

where $\omega_n^2 = I_{\text{CP1}} K_{\text{VCO1}} / C_1 N$ and $\zeta = I_{\text{CP2}} K_{\text{VCO2}} R_2 / 2\omega_n N$ are the frequency and damping factor of the closed loop complex pair.

To obtain the settling time, (7) is transformed back to time domain, assuming under-damping ($\zeta \leq 1$)

$$e(t) = \frac{\Delta F_{\text{ramp}}}{\Delta T_{\text{ramp}}} \frac{e^{-\zeta\omega_n t}}{\omega_n \sqrt{1 - \zeta^2}} \sin\left(\sqrt{1 - \zeta^2}\omega_n t\right). \tag{8}$$

Note that ω_n is determined by the first path characteristics, whereas $\zeta\omega_n = I_{\mathrm{CP2}}K_{\mathrm{VCO2}}R_2/2N$ is mainly determined by the second path components and the division ratio. Hence, the settling time is only dependent of K_{VCO2}/N (as long as $\zeta \leq 1$), which can be designed to be quite constant across the tuning range, as shown in Section III. If the system becomes over-damped ($\zeta > 1$), however, the settling time worsens and becomes heavily dependent of the first path parameters. Hence, PLL parameters should be set such that even for minimal K_{VCO1} in the region of interest, the system will still be under-damped.

The PLL closed-loop bandwidth can also be expressed in terms of ζ and ω_n

$$f_{\mathrm{BW},-3\ \mathrm{dB}} = \frac{\zeta\omega_n}{\zeta}\sqrt{1+2\zeta^2+\sqrt{(1+2\zeta^2)^2+1}}. \quad (9)$$

For moderately under-damped system ($0.6 < \zeta < 1$), (9) is quite insensitive to ζ variation, assuming constant $\zeta\omega_n$, changing only 25% over the whole $0.6 < \zeta < 1$ range.

Furthermore, in the dual-loop architecture, the PLL loop retains stability even when K_{VCO1} drops drastically at the tuning range edges. This result is contrary to the single-loop design where all three characteristics (settling time, bandwidth, and stability) are highly sensitive to VCO gain variation.

Low first path gain can, however, limit the maximal modulation rate through the PLL output frequency slew rate

$$\mathrm{SR} = \max\frac{df_{\mathrm{out}}}{dt} \approx \frac{1}{2}\frac{I_{\mathrm{CP1}}K_{\mathrm{VCO1}}}{C_1} \quad (10)$$

and produce high-input steady-state phase offset

$$\Delta\phi_{\mathrm{in,ss}} = \lim_{s\to 0} s\frac{2\pi e(s)}{\mathrm{Ns}} = \frac{-\Delta F_{\mathrm{ramp}}}{\Delta T_{\mathrm{ramp}}}\frac{2\pi C_1}{I_{\mathrm{CP1}}K_{\mathrm{VCO1}}} \quad (11)$$

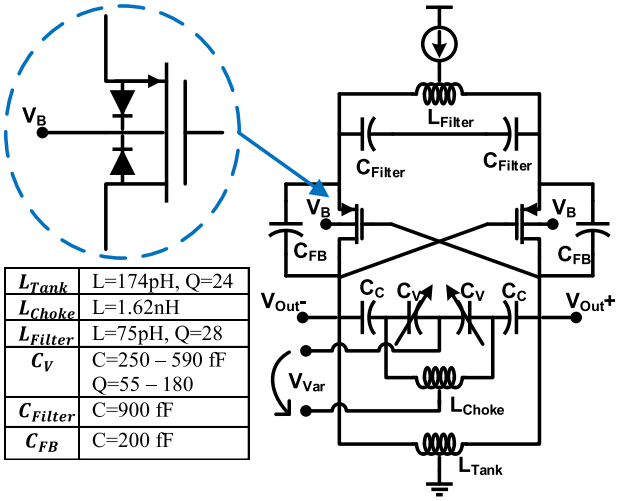
which may hinder the PLL locking. Therefore it is preferable to increase the gain of the first path, thereby putting the system well in the under-damped region ($0.6 < \zeta < 1$), and thus improving both slew rate and phase offset without a major effect on settling.

Additional high-frequency poles can be added to one or both filters for stronger out-of-band suppression, which is usually needed to meet the ripple and phase noise requirements. In a well-behaved design, one where the poles frequencies are well above the loop bandwidth, they do not change the abovementioned results drastically. However, they can have a moderate effect on the settling if the system is highly under-damped.

We now turn to the implementation of the synthesizer, first describing the dually controlled VCO fit for the abovementioned PLL (Section III), then describing the full FMCW generation system implementation in Section IV.

III. Dually Controlled VCO With Bulk Control

In order to allow a fast frequency chirp, it is required to have a continuous and sufficiently wide tuning range VCO while maintaining low phase noise. The aforementioned requirement coupled with the physical constraints of available MOS varactors implies that the VCO will also have a huge gain variability across the tuning range, making the need for a second control path essential, as shown in Section II. Therefore, we have implemented a 10% continuous tuning range dual-control K-band gm-boosted Colpitts VCO with inductive degeneration shown in Fig. 2.



L_{Tank}	L=174pH, Q=24
L_{Choke}	L=1.62nH
L_{Filter}	L=75pH, Q=28
C_V	C=250 – 590 fF Q=55 – 180
C_{Filter}	C=900 fF
C_{FB}	C=200 fF

Fig. 2. Schematic of low phase noise gm-boosted Colpitts VCO with an NMOS varactor, high gain, primary frequency control, and a parasitic bulk-drain capacitance, low gain, secondary frequency control.

A. High-Gain gm-Boosted Colpitts VCO With Inductive Tail

The gm-boosted Colpitts topology combines the favorable impulse sensitivity function of Colpitts oscillators and the power efficiency and startup qualities of the cross-coupled topology, increasing the small signal loop gain of the Colpitts topology by a factor of $(2 + (C_{\mathrm{FB}}/C_{\mathrm{Filter}}))$, where C_{FB} is the drain–source capacitance and C_{Filter} is the differential capacitance from source to ground that completes the Colpitts feedback, as demonstrated in [13]. PMOS transistors were utilized since they contribute less flicker and thermal noise for the same transconductance as compared to NMOS transistors. PMOS transistors also have a higher gate impedance relative to heterojunction bipolar transistors (HBTs) which translates to overall lower VCO phase noise at the expense of higher needed quiescent current. These PMOS devices are thin oxide with an $f_{\max}$ of 45 GHz, in order to provide the required gain for startup with reasonable parasitic capacitance. The transistor source voltage is biased at 1.3 V to avoid reliability issues.

Due to the high frequency of operation, the conventional design that uses two current sources to present the needed high impedance to ground is suboptimal and will impact feedback path effectiveness and inject extra noise. Instead, we use an inductive degeneration to present the needed high impedance at the fundamental frequency so that the capacitive feedback path will be effective. Since this topology also uses a cross-coupled pair, we must also present a high impedance at the 2nd harmonic as shown in [14], which is common mode. We take advantage of the differential inductor coupling coefficient, $k_{\mathrm{filter,diff}}$, to present a much smaller inductance at the 2nd harmonic and together with the common-mode capacitance obtain the needed resonance as shown in (12) (if we neglect the common contribution of the main tank)

$$Z_{\mathrm{CM}} \approx s(1-k_{\mathrm{filter,diff}})L_{\mathrm{filter}}||\frac{1}{sC_{\mathrm{CM}}} \quad (12)$$

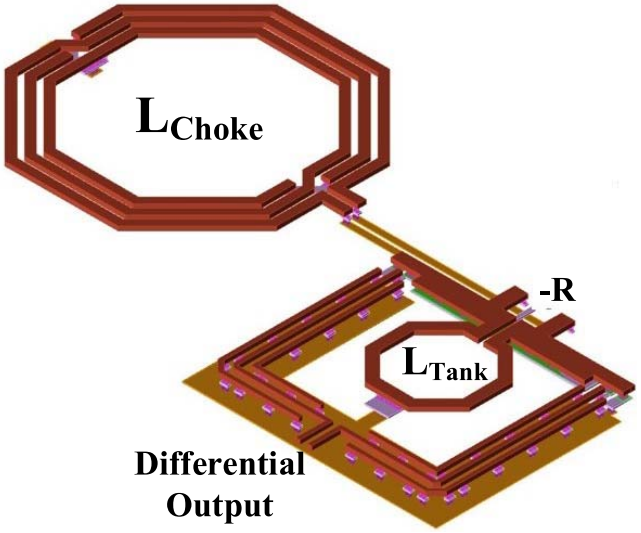


Fig. 3. 3-D view of the VCO *LC* tank with choke inductor.

where $C_{\rm CM}$ represents all of the common-mode capacitance including the tank, transistors, and feedback capacitors.

As stated previously, high-gain varactors are needed to obtain the required continuous tuning range. Since the varactors are ac biased, it is necessary to introduce the needed dc voltage while minimizing noise injection to the tank. Such noise will be modulated by the varactors and will greatly increase AM-to-PM conversion of the VCO. In the case of the conventional resistive RF choke, the phase noise contribution of such a source can be approximated as a narrowband frequency modulation, as shown in the following equation:

$$\mathcal{L}_{\rm choke}(f_{\rm off}) = \frac{4K_bTR_{\rm choke}K_{\rm Var}^2}{f_{\rm off}^2} \tag{13}$$

where $K_{\rm Var}$ is the VCO gain and can reach up to 1.8 GHz/V, $f_{\rm off}$ is the offset frequency, K_b is Boltzmann's constant, T is the temperature in degrees kelvin, and $R_{\rm choke}$ is the choke resistor value. At the implemented values, the contribution of this noise source to the overall phase noise dominates. Therefore, a choke inductor was used instead of a resistor, mitigating most of this noise as shown in [15]. A 3-D view of the *LC* tank including the RF choke inductor is shown in Fig. 3. A separate inductor was preferred over the transformer coupled tank shown in [16] in order to prevent Q degradation of the tank and to simplify the design procedure.

B. Secondary VCO Control Path

Due to the relatively high operating frequency, as compared to the cutoff frequency of the PMOS devices in this technology ($f_{t,\rm PMOS} \approx 45$ GHz), large devices are required to ensure startup. As a result, the drain–bulk junction capacitance will also be fairly large. Equation (14) describes the drain–bulk junction capacitance under the assumption of reverse bias

$$C_{J,\rm BD}(V_B) = \frac{A_DC_{j0}}{\sqrt{1+\frac{V_B-V_D}{V_{\rm bi}}}} \tag{14}$$

where V_B is the bulk voltage, V_D is the drain voltage, A_D is the drain–bulk junction area, C_{j0} is the junction capacitance density for zero bulk–drain voltage, and $V_{\rm bi}$ is the built-in potential of the junction [17].

We clearly have a parasitic varactor that can be used as a second frequency control path. Furthermore, as demonstrated in [18], the transistor effective noise depends only on the tank loss (Q) and the topology. This finding means that the body effect caused by changing the bulk bias will not have an adverse effect on phase noise performance. Also, since the parasitic diode capacitance is only a small fraction of the entire resonator capacitance ($\sim$1.5%), its variability does not affect the total quality factor of the VCO. Actually, apart from keeping the diode in reverse bias, the only constraint the second control path has is to maintain a sufficient small signal VCO loop gain for all operational bulk voltages.

Assuming a high tank quality factor, the frequency of the VCO is represented by

$$f_{\rm VCO}(V_{\rm Var}, V_B) \cong \frac{1}{2\pi\sqrt{L_{\rm tank}[C_{\rm fix}+C_V(V_{\rm Var})+C_{J,\rm BD}(V_B)]}} \tag{15}$$

where $L_{\rm tank}$ is the tank inductance, $C_{\rm fix}$ is the fixed tank capacitance including the Colpitts and parasitic capacitance, and C_V is the main varactor effective capacitance for dc voltage $V_{\rm Var}$. In the general case, the effective capacitance of each varactor is dependent of the signal amplitude, which is controlled by both tuning voltages. However, in the proposed design, the quality factor of the main varactor is much higher than the inductor quality factor; hence, the signal amplitude is stable across the tuning range. Therefore, it was assumed in (15) that each varactor capacitance is dependent only of its tuning voltage.

The VCO gain for each control voltage can be derived as in [4]. The main control gain is

$$\begin{aligned} K_{\rm Var}(V_{\rm Var}, V_B) &= \frac{\partial f_{\rm VCO}}{\partial V_{\rm Var}}(V_{\rm Var}, V_B) \\ &= -2\pi^2 L_{\rm tank} f_{\rm VCO}^3(V_{\rm Var}, V_B)\frac{dC_V}{dV_{\rm Var}}(V_B) \end{aligned} \tag{16}$$

and similarly, the secondary varactor control path gain is

$$\begin{aligned} K_B(V_{\rm Var}, V_B) &= \frac{\partial f_{\rm VCO}}{\partial V_B}(V_{\rm Var}, V_B) \\ &= -2\pi^2 L_{\rm tank} f_{\rm VCO}^3(V_{\rm Var}, V_B)\frac{dC_{J,\rm BD}}{dV_B}(V_B). \end{aligned} \tag{17}$$

The gain variability of each control voltage, therefore, is dependent of its respective varactor variability and of the VCO frequency variation set by both tuning voltages.

In the main control path, $dC_V/dV_{\rm Var}$ changes rapidly across the tuning range and is the dominant factor in the gain variability, yet, it is almost independent of V_B as its tuning range is negligible. In the second control path, however, $dC_{J,\rm BD}/dV_B$ is quite constant as V_B is stable during the frequency modulation. Therefore the gain variability comes mainly from the change in $f_{\rm VCO}$ across the tuning range, which is roughly 30% for a 10% tuning range.

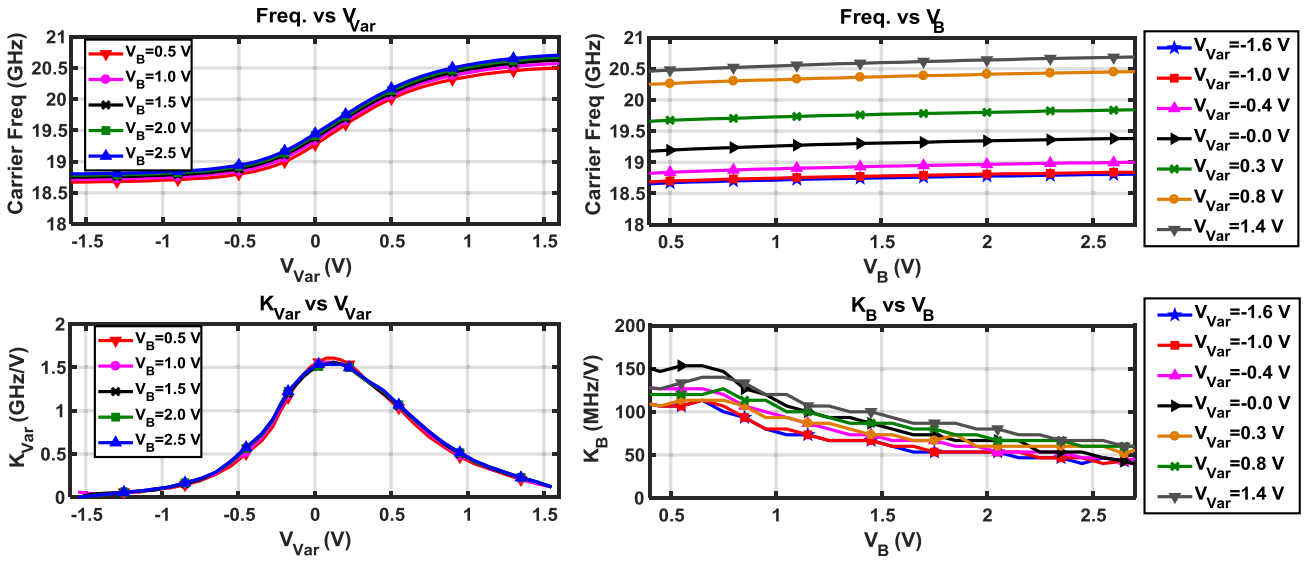


Fig. 4. Measured VCO frequency and gain ($K_{\mathrm{Var}} = (\partial f_{\mathrm{out}}/\partial V_{\mathrm{Var}})$, $K_B = (\partial f_{\mathrm{out}}/\partial V_B)$) versus primary and secondary control voltages (V_{Var}, V_B).

To calculate the loop variability across the frequency, we substitute (17) into the expression for $\zeta\omega_n$ from Section II

$$\zeta\omega_n = -2\pi^2 I_{\mathrm{CP2}} R_2 f_{\mathrm{ref}} L_{\mathrm{tank}} f_{\mathrm{VCO}}^2 \frac{dC_{J,\mathrm{BD}}(V_B)}{dV_B}. \quad (18)$$

Hence, as long as the PLL is under-damped, both the PLL settling time and bandwidth are proportional to f_{VCO}^2 and only a mild variation of about 25% over the 10% tuning range is expected.

The VCO frequency and gain, as a function of the control voltages, were characterized in measurement. The measured output frequency range is $18.7 - 20.6$ GHz with $\pm 0.7\%$ shift across the -40 °C to 85 °C temperature. Fig. 4 shows measured VCO output frequency and gain across both control voltages. As expected the main control path gain has high variability across the frequency range but is hardly affected by the second path. The second control path gain, however, has around 30% variability across V_{Var}, as predicted by (17) for constant bulk voltage V_B.

IV. Fully Integrated FMCW Synthesizer System

Following the advantages of the dual loop discussed in Section II, a fully integrated FMCW synthesizer system, based on the dual-loop architecture was developed for the 77/79 GHz band [19].

The synthesizer's block diagram is shown in Fig. 5. The synthesizer consists of a K-band dual-loop fractional-N PLL with internal modulation control and a times four frequency multiplier. The dual-loop PLL is constructed similarly to the one described in Section II with two differences. First, the second path is implemented using series resistors connected directly to the PFD, instead of a CP; thus the effective CP current is

$$I_{\mathrm{CP2}} = V_{\mathrm{dd}}/R_2 \quad (19)$$

with V_{dd} being the supply voltage. Such connection reduces the phase noise contribution of the second path at the expense

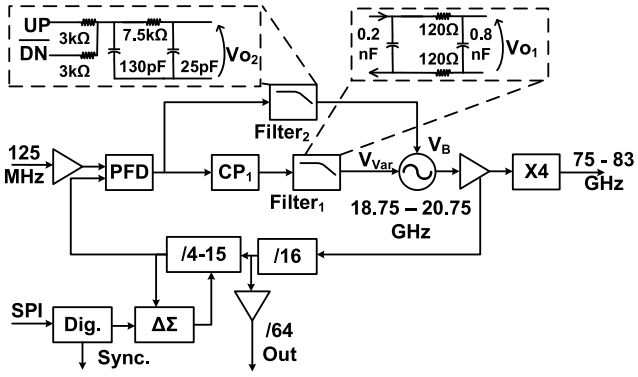


Fig. 5. Block diagram of a fully integrated 75–83 GHz FMCW generator, employing a dual-path fractional-N PLL with internal modulation control.

of less bandwidth flexibility. Mismatch between up and down signals also worsens; however, it is not a major issue due to the presence of input phase offset during the modulation. Second, additional poles are introduced to both filters for better out-of-band phase noise suppression.

Both paths are feeding the dual-control VCO described in Section III. The feedback divider consists of an HBT current-mode logic constant prescaler (with division by 16) and a variable CMOS extended multi-modulus divider providing 4 to 15 division ratio. The PLL uses a constant reference clock of 125 MHz, and frequency modulations are generated internally using a digital controller and a 16-bit 3rd-order MASH modulator. The controller can generate sawtooth and triangular modulations, as well as a continuous wave of constant frequency. The PLL output is up-converted from K-band to W-band using an integrated times four frequency multiplier.

A. Charge Pump Design

To avoid the need for external capacitors, a low current and low-noise CP is required. As mentioned in Section II, during fast frequency modulation the input phase offset can

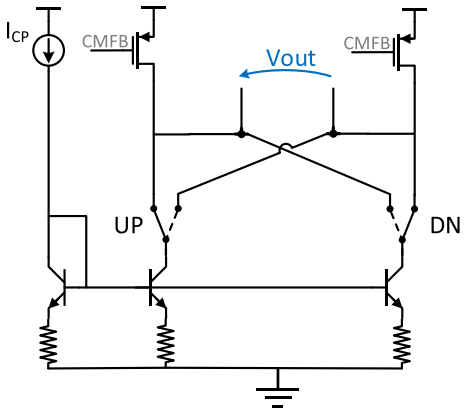


Fig. 6. Simplified schematic of the differential current-steering CP.

become non-negligible. This phase offset has a major effect on output noise in most low-noise CP architectures, degrading the overall PLL performance [8]. Therefore, we use a simpler current-steering architecture with constant dc current, shown in Fig. 6, for which output noise is independent of input phase and produces less noise for high-input phase due to a smaller amount of noise contributors. Degenerated HBTs were used as the bottom current sources for low noise and high linearity. The top current sources are biased by the common-mode feedback and are implemented by long channel PMOS transistors for low flicker noise. Current switches were also implemented using HBTs which are biased in active operation region for smaller charge injection. The CP was optimized for low-noise yielding output noise spectral density of 14 and 1.6 pA/$\sqrt{\text{Hz}}$ at 1 and 100 kHz, respectively, for $I_{\text{CP}} = 80\ \mu\text{A}$.

B. PLL Loop Optimization

PLL loop design suffers from a fundamental tradeoff. The bandwidth must be high enough for a short settling time and low enough for sufficient phase noise suppression at high offset frequencies, which is a crucial feature in FMCW radar applications [2]. Thus, secondary path unity gain frequency was set to 140 kHz such that all in-band noise sources are suppressed above 1-MHz offset frequency to below the VCO noise level.

The first path gain was set such that $\zeta = 0.6$ for maximal main VCO gain ($K_{\text{Var}}^{\max} = 1.6$ GHz/V), hence the system stays under-damped for $K_{\text{Var}} \geq 0.6$ GHz/V which holds true, according to Fig. 4, for $f_{\text{VCO}} = 19 - 20.25$ GHz. As a result, due to (9) and (18), a variability of only 25% is expected in settling time and loop bandwidth across the 76–81 GHz output frequency range. Substituting the first path parameters into (10), the maximal PLL slew rate ranges from 185 to 460 GHz/ms. Therefore, for a 100 GHz/ms frequency modulation rate, the maximal expected steady-state input phase offset is $\phi_{\text{ss}}^{\max} = 100°$, highlighting the need for a CP with low noise at high phase offsets.

Simulated primary and secondary path transfer functions at the middle of the VCO band ($K_{\text{Var}} = 1.5$ GHz/V, $K_B = 100$ MHz) are shown in Fig. 7.

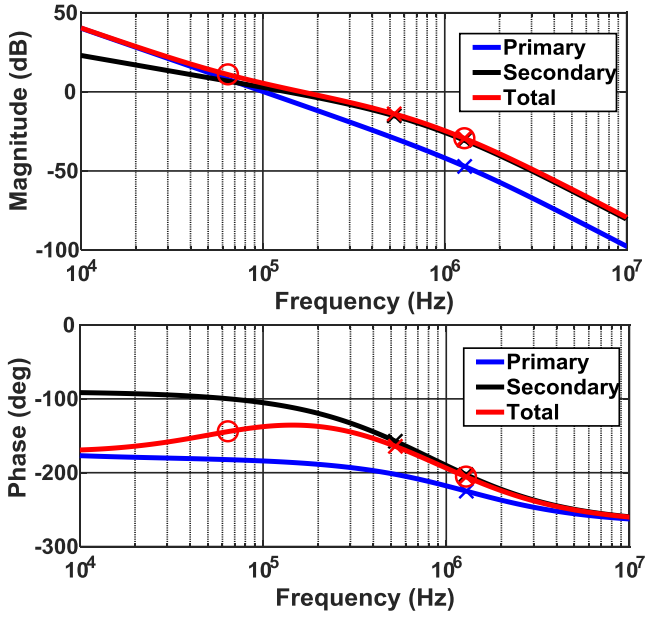


Fig. 7. Simulated PLL primary and secondary path transfer functions. Zeros and poles are depicted by ◯ and ×, respectively. The primary path is dominant in low frequencies while the secondary path is dominant at the unity gain crossing, thereby preserving the system bandwidth even when the primary path gain drops at the tuning range edges.

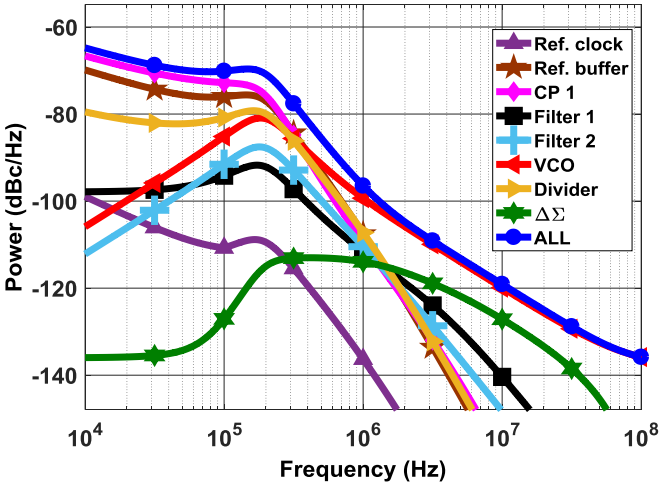


Fig. 8. Simulated closed-loop phase noise contribution of each component normalized to 79-GHz carrier. All in-band noise components and $\Delta\Sigma$ quantization noise are suppressed above 1-MHz offset.

Simulated phase noise contribution of different components is shown in Fig. 8. The CP noise is dominant at low offset frequencies but it is suppressed, together with other in-band noise sources, below the VCO noise level at frequencies above 1 MHz.

C. PLL System Dynamics Simulation

For steeper roll-off and improved $\Delta\Sigma$ noise suppression, additional high-frequency poles were inserted in both filters. However, the presence of additional poles in the loop filter may damage the settling response if they are located too

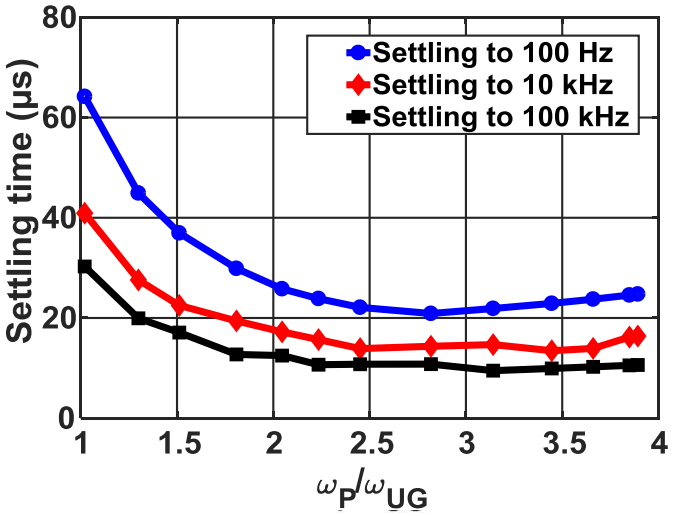


Fig. 9. Simulated frequency error settling response time to input frequency ramp with modulation rate of 20 GHz/ms versus high-frequency pole ω_p location with respect to the PLL loop unity gain crossing ω_{UG}.

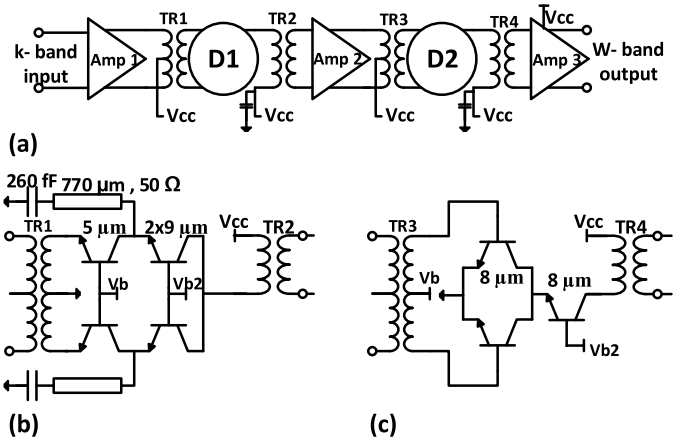


Fig. 10. (a) Block diagram of the multiplier. (b) Schematic of the first doubler D1. (c) Schematic of the second doubler D2. For better readability, in differential structures, device parameter values are denoted only on the upper half.

close to the loop unity gain frequency. To assess the effect, a behavioral Simulink model was created using different component characteristics at the middle of the frequency range where the VCO gain is maximal. Using the model, a frequency ramp (modulation rate: 20 GHz/ms) simulation was conducted for various high-frequency pole locations. The error settling time is shown in Fig. 9 as a function high-frequency pole ω_p location with respect to the PLL loop unity gain crossing ω_{UG}. Note that high-frequency poles do not impact the settling when $\omega_p > 2\omega_{\mathrm{UG}}$. The first high-frequency pole was set to $3\omega_{\mathrm{UG}}$, to allow some robustness for process and temperature variations. Additional poles cannot be placed at the same frequency due to the passive topology of the loop filters and were, thus, placed at a higher frequency as shown in Fig. 7.

D. Frequency Multiplier Design

The multiplier chain consists of two doublers and three amplifiers, as shown in Fig. 10. The multiplier topology was optimized for spectral purity where the first doubler is a common-base stage and the second doubler is a common-source stage as analyzed in [20]. A cascode topology is used for its impedance buffering which increases the operational bandwidth and, on the first doubler, introduces an intermediate node which is optimal for filtering. A Class-B biasing approach was used for maximal 2nd-harmonic current using a digital-controled current mirror for delicate bias tuning. To improve spectral purity, a dedicated 4th-harmonic trap was implemented within the first doubler. A transformer-coupled approach is used for matching between the stages and filtering and feeding the dc. The overall multiplier chain consumption is 129 mA from a 2.7 V supply.

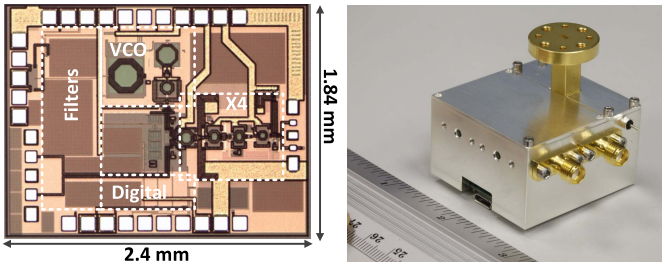


Fig. 11. Full synthesizer die micrograph and packaging photograph.

V. Fabrication and Measurement Results

The synthesizer was fabricated with Global Foundries 130-nm BiCMOS technology. The total die size is 2.4×1.84 mm^2 including access pads (core size 2×1.4 mm^2). The fabricated die was packaged along with an off-the-shelf low-voltage differential signaling crystal oscillator, universal serial bus serial to parallel interface chip, supply regulators, and W-band waveguide. Die and packaging photographs are shown in Fig. 11. Measurements of the synthesizer differential output were carried out in a single-ended manner, with the other output 50-Ω terminated.

A. Constant Frequency Measurements

The synthesizer total measured power consumption is 590 mW from 1.3 and 2.7 V supplies. Output power measured at the chip output is 5–6.5 dBm (8–9.5 dBm differential) across the 75–83 GHz range. When measured at the package output, power was reduced by approximately 3.3 dB and additional 0.6 dB across the −40 °C to 85 °C temperature range, as depicted in Fig. 12. Uwanted PLL harmonics are suppresed by the multiplier to a level lower than 40 dBc including 1st, 2nd, 3rd, and 5th PLL harmonics.

Output phase noise was measured at various carrier frequencies in fractional-N mode and is presented in Fig. 13. Phase noise at 1-MHz offset ranges from −97 to −100 dBc/Hz at room temperature with 2-dB degradation across −40 °C to 85 °C temperature. As was expected, above 1-MHz offset all in-band noise sources and the $\Delta\Sigma$ quantization noise are suppressed below the VCO noise level. The synthesizer is stable in all frequencies, despite the low phase margin, due to the inherent stability of the dual-loop architecture. Phase noise is stable across the output frequency

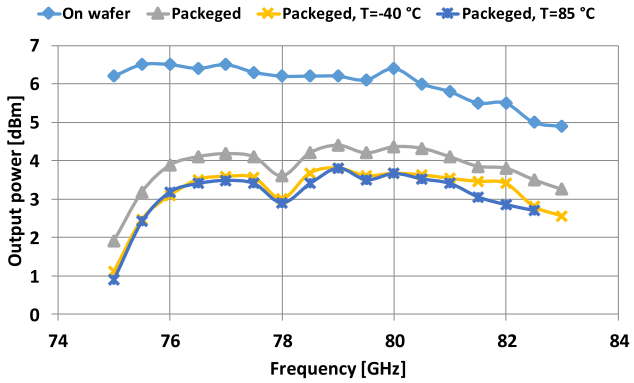


Fig. 12. Measured synthesizer's single-ended output power versus frequency on wafer and at package output.

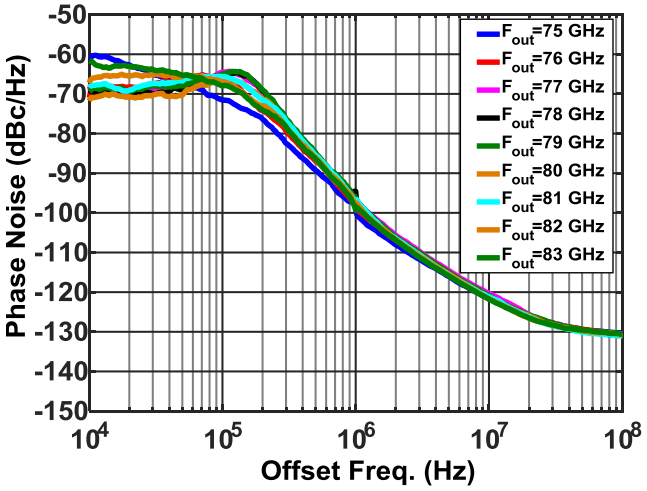


Fig. 13. Measured synthesizer's phase noise for different output frequencies in fractional-N mode. Phase noise stability across the output frequency range is due to the unique dual-path implementation.

range, especially in the 76–81 GHz range, affirming the bandwidth stability prediction in Section II. At the edges of the tuning range, where main varactor gain drops drastically, the system becomes under-damped and the bandwidth is slightly lower.

B. Frequency Modulation Measurements

It is not practical to measure frequency modulation at the W-band output due to its high bandwidth (up to 8 GHz). Therefore, dynamic measurements were performed by sampling an internal $f_{\text{out}}/64$ output (L-Band) shown in Fig. 5. This signal was demodulated using a spectrum analyzer and dedicated software (Agilent VSA), and the results were normalized back to the W-band.

Maximal modulation rate of 100 GHz/ms was achieved at the 75–81 GHz range. When sweeping the full 8-GHz output range, a maximal rate of only 40 GHz/ms was achieved. The rate decrease is due to drastic drop in the main VCO control gain, which decreases the maximal slew rate and over-damps the system. A 5 GHz over 50-μs sawtooth ramp with 15-μs returning time and an 8 GHz over 200-μs sawtooth ramp with 60-μs returning time are shown in Fig. 14.

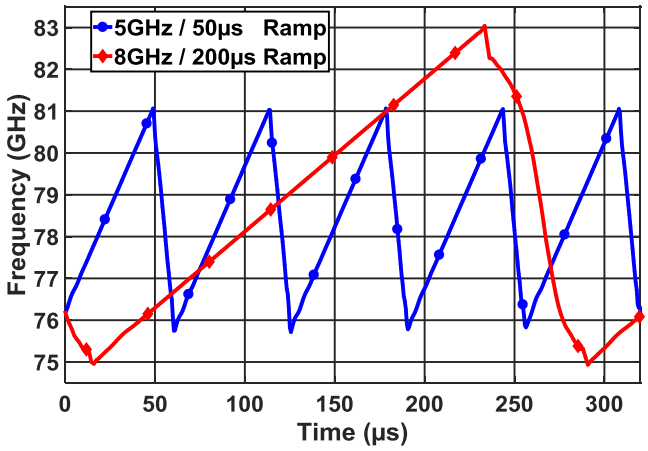


Fig. 14. Measured 5 GHz over 50-μs sawtooth ramp with 15-μs returning time and an 8 GHz over 200-μs sawtooth ramp with 60-μs returning time.

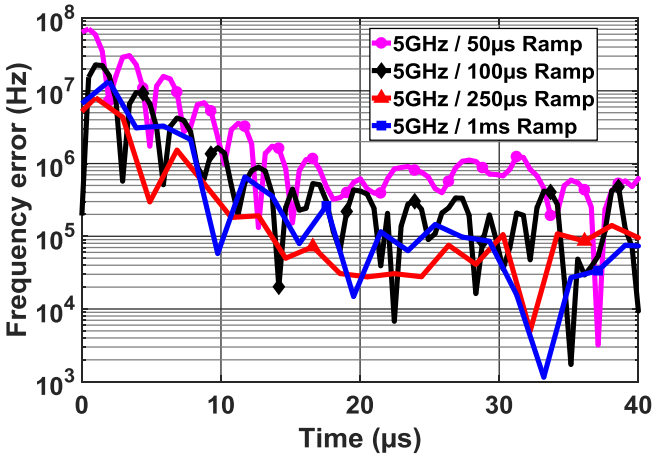


Fig. 15. Measured frequency error at the beginning of the ramp for various modulation rates.

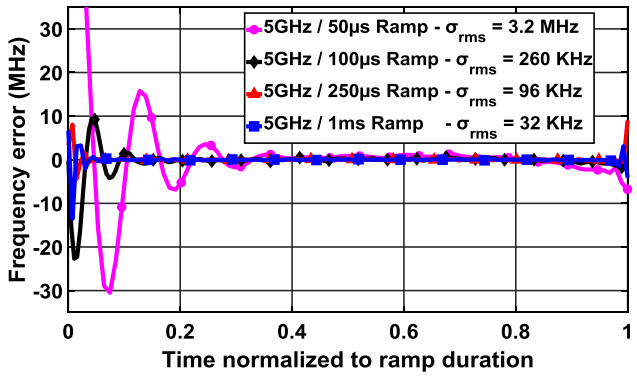


Fig. 16. Measured frequency error for 5-GHz ramp with various modulation rates versus time (normalized by ramp duration). The error rms values were calculated ignoring the first 5% of the chirp time to exclude settling.

To assess settling time and modulation linearity, the frequency deviation from the ideal modulation was measured. Initial settling of frequency error for different modulation rates is shown in Fig. 15, and frequency error versus normalized time for different modulation rates is shown in Fig. 16.

TABLE I
PERFORMANCE COMPARISON TO STATE OF THE ART

	This work	[21]	[22]	[23]	[24]
PLL architecture	**Dual loop Frac-N**	Dual PLL	Frac-N	Frac-N	VCO only
Integration level	**Fully**	Partially	Fully	Fully	VCO only
Center frequency [GHz]	**79**	80	61.4	79	78.5
$\mathcal{L}(f_{off.} = 1\,MHz)$ [dBc/Hz] for frac-N mode at 25°C	**-97**	-94	-86	-83	-99
Modulation bandwidth [GHz]	**8**	24	3	5	8.5
Modulation rate [GHz/ms] : Frequency error RMS [kHz]	**5/1 : 32** **5/0.25 : 96** **5/0.1 : 260** **5/0.05 : 3200**	20/3.8 : 318	0.96/0.64 : 170 0.96/0.32 : 208 0.96/0.16 : 246	0.312/1 : 960	-
Power consumption [mW]	**590**	1557	310	320	-
Technology	**130 nm SiGe BiCMOS**	SiGe	130 nm SiGe BiCMOS	65 nm CMOS	130 nm SiGe BiCMOS

The root-mean-square (rms) error values were calculated ignoring the first 5% of the chirp time to exclude some of the settling.

It can be seen that the settling rate is constant for different modulation rates, which is consistent to (8).

Finally, an overall comparison to the prior art is given in Table I. This paper presents lowest phase noise at 1-MHz offset of all of the integrated synthesizers and the lowest frequency modulation error for a given modulation rate.

VI. CONCLUSION

The characteristics of the dual-loop PLL architecture were analyzed in the context of wideband linear frequency modulation. The architecture was shown to have several key advantages: inherent robustness to VCO gain variation across the tuning range, high slew rate, and enhanced loop filter flexibility compared to the single-loop architecture.

In addition, we demonstrated that MOS transistor parasitic bulk–drain capacitance can be used for adding a second controlling method to a MOS VCO turning it into a dually controlled oscillator without degrading performance.

This analysis and the novel VCO controlling method were used to construct a fully integrated 77/79 GHz band FMCW signal generator in 130-nm SiGe BiCMOS yielding state-of-the-art performances including a loop bandwidth stability over the output frequency range, −97 dBc/Hz phase noise at 1-MHz offset, and a maximal modulation rate of 100 GHz/ms.

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