A 6-bit 0.81-mW 700-MS/s SAR ADC With Sparkle-Code Correction, Resolution Enhancement, and Background Window Width Calibration

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***Abstract*— This paper presents a 6-bit high-speed successive approximation register analog-to-digital converter (ADC) with sparkle-code correction. By quantizing the comparator decision time (CDT), the sparkle codes are identified and corrected, reducing the error rate from 10^{-4} to below 10^{-9}. Furthermore, CDT quantization enables 1-bit increase in the ADC resolution by setting the detection boundary to be ±0.25 LSB. Thus, only five comparison cycles are needed to reach 6 bits, leading to an increased ADC speed. A novel dither-based background calibration technique is devised to accurately control the CDT detection window size and ensure process, temperature, and voltage robustness. A prototype ADC in 40-nm CMOS achieves 35.3-dB signal-to-noise/distortion ratio (SNDR) and consumes 0.81 mW while sampling at 700 MS/s.**

***Index Terms*— Analog-to-digital converter (ADC), comparator metastability, digital background calibration, resolution enhancement, sparkle code, successive approximation register (SAR).**

I. Introduction

SUCCESSIVE approximation register (SAR) analog-to-digital converter (ADC) is a popular ADC architecture due to its low power, low area, and low design complexity. In the past, it has been primarily used for low-speed applications. Recently, its speed has been greatly increased due to both technology advances and circuit innovations. On the technology side, because SAR ADC is highly digital, its speed naturally increases with CMOS scaling. On the circuit side, several techniques have been developed, including asynchronous clocking [1]–[4], multi-bit-per-cycle [2], [5], [6], comparator alternation [3], and loop unrolling [7]–[10]. Nowadays, single-channel SAR ADCs can reach 1 GS/s with an excellent energy efficiency of 30-fJ/conversion-step [3], [11], [12].

As the SAR ADC speed increases, the problem of sparkle codes becomes more severe and can cause significant increase in bit error rate (BER). Low BER is necessary for many applications. For example, WLAN and instrumentation require BER to be lower than 10^{-9} and 10^{-12}, respectively [13]. For an SAR ADC, sparkle codes are mainly due to comparator metastability [14]–[16]. Although metastability does not degrade the ADC performance much in terms of signal-to-noise/distortion ratio (SNDR) due to its rare occurrence, it may require complicated error corrections to meet the BER specifications [17].

For a synchronous SAR ADC, metastability means the comparator cannot fully regenerate within one comparison cycle, causing wrong outputs. For an asynchronous SAR ADC, when metastability happens in the MSB comparisons, the entire ADC conversion may not finish within the allocated conversion time (the LSB comparisons may not even start), leading to sparkle codes. To solve this problem, the ready detector after the comparator can be skewed, so that it provides a time-out function; that is, if the comparator takes longer than a preset maximally allowed time duration, the SAR operation will proceed to the next comparison cycle without waiting for the comparator to fully resolve. This essentially puts an upper limit on the worst case comparison time and accelerates the overall conversion process. Thus, it reduces the probability of having unfinished SAR comparison cycles. Nevertheless, it increases the probability of the other type of sparkle codes: if the comparator has not fully resolved, the recorded digital outputs can be wrong. As a result, the overall ADC sparkle-code rate may not reduce.

There are several ways to reduce the sparkle-code rate. One method is to simply allocate more time for the comparator to resolve, but this sacrifices the ADC speed. Another method is to reduce the comparator regeneration time constant by sizing up transistors; however, it has limited effect once the comparator load is dominated by self-loading. There is a technology limit. In addition, up-sizing transistors can greatly increase power. To avoid large speed or power penalty, researchers recently developed several sparkle-code correction techniques [18]–[20]. The core idea is that if we know which comparison cycle is in metastability, we can deduce that the differential comparator input in that cycle must be very close to 0. As a result, we know where the input is and can recover the right ADC output even though we may not know the comparison result due to metastability. There are several ways to sense metastability. One approach is to detect non-differential DAC control signals [18]. If one pair of the DAC control signal is non-differential, the corresponding comparison cycle is assumed to be in metastability. This scheme works well

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for a synchronous SAR ADC, but may not be suitable for an asynchronous SAR that waits for each comparison to fully resolve before moving to the next cycle. For example, if the nth comparison cycle is in metastability, it is still probable that it can finish within the total allocated SAR ADC conversion time, but the $(n+1)$th comparison cycle may not have time to finish and end up with a non-differential DAC control. In this case, the metastability cycle would be misidentified. The other approach is to directly sense the comparator decision time (CDT) [19], [20]. When metastability happens, the CDT is elongated. Thus, metastability can be detected by comparing the CDT with a reference delay using an array of 1-bit time-to-digital converters (TDCs). This scheme works for both synchronous and asynchronous SAR ADCs. Nevertheless, both the CDT and the reference delay are sensitive to process, temperature, and voltage (PVT) variations. Careful foreground hand tuning is used to set an appropriate reference delay in [19] and [20], but it cannot track environment changes.

This paper presents a novel sparkle-code reduction technique for high-speed SAR ADCs. It builds upon the basic idea of CDT quantization of [19], but it ensures PVT robustness by devising a new background calibration technique. Moreover, it makes use of CDT quantization to gain 1-bit increase in the ADC resolution. It works by setting the reference delay τ to match the CDT when the comparator sees a ± 0.25-LSB input. Background calibration of τ is enabled by injecting a 0.5-LSB pseudo-random dither to the SAR ADC. If τ is set correctly, the probability of the comparator seeing an input within ± 0.25 LSB during all SAR conversion cycles is 50%, which is independent of the ADC input because of the injected uncorrelated dither. Thus, by continuously monitoring the rate of TDC outputs being 1, τ can be background-tuned to the desired value. Furthermore, by setting the CDT window to be ± 0.25 LSB, the ADC resolution can be increased by 1 bit by making use of the TDC output, which effectively performs a 0.5-LSB quantization. This means that the proposed architecture can use a 5-bit SAR ADC to obtain 6 bits. The reduction in the number of comparison cycles increases the ADC speed.

A prototype ADC equipped with the proposed technique is built in 40 nm [21]. The measured sparkle-code rate is reduced from 10^{-4} to below 10^{-9}. The SNDR is increased from 30.2 to 35.3 dB, which validates the 1-bit resolution enhancement. It samples at 700 MS/s and consumes 0.81 mW, leading to a Walden figure-of-merit (FoM) of 24 fJ/conversion-step.

This paper is organized as follows. Section II shows the cause of sparkle codes and reviews the CDT-based sparkle-code removal technique. Section III presents the proposed technique with background calibration and resolution enhancement. Section IV discusses the prototype ADC design. The measurement results are in Section V.

II. Metastability-Induced Sparkle-Code Error

A. Review of High-Speed SAR ADC Design

Before we discuss metastability-induced sparkle codes, let us first review the design of a high-speed SAR ADC. Fig. 1(a) shows the widely used asynchronous clocking scheme that uses a self-oscillating loop to generate a repeated comparator clock signal [1]. The comparator ready is detected by an XOR gate. The benefit of using asynchronous clocking is twofold. First, it reduces the total comparison time. Second, it removes the need for an external high-speed comparator clock, whose generation and distribution can be power consuming.

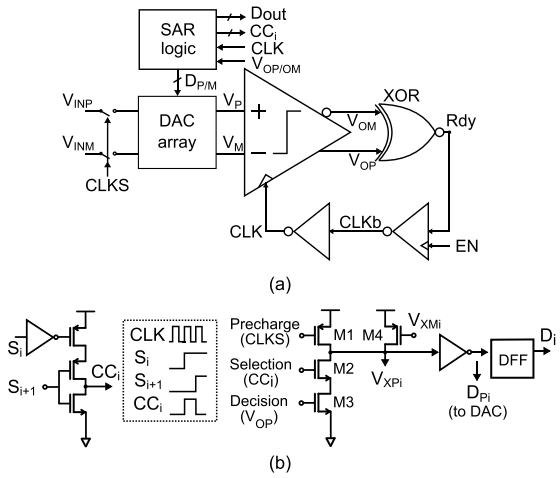

Fig. 1. (a) Asynchronous clocking. (b) Dynamic SAR logic.

Dynamic SAR logic in Fig. 1(b) is also widely used in high-speed SAR ADCs [3], [18]. It uses a simple dynamic logic gate to altogether perform reset, bit selection, DAC switching, and data latching. Pull-up transistor ($M1$) precharges the nodes $V_{\mathrm{XPi/XMi}}$ during the sampling phase. The comparison cycle signal CC_i is high during the ith comparison cycle. Thus, once the comparator is triggered, its output $V_{\mathrm{OP/OM}}$ can directly propagate through $M3$ to drive the DAC capacitors via an inverter buffer, thereby minimizing the time that the SAR logic takes. When the ith comparison finishes, CC_i falls to low, and thus, the ith comparison result is stored at the $V_{\mathrm{XPi/XMi}}$. An optional keeper M_4 can be added to protect the output against charge leakage.

B. Causes of Sparkle Codes

As mentioned in Section I, there are two sources of metastability-induced sparkle codes in an asynchronous SAR ADC. Which source dominates depends on how the comparator and the ready detector are designed. In one case, we can skew the comparator and the ready detector in such a way that the ready signal is not produced while the comparator is resolving a small input. This way, we wait for the comparator outputs to fully resolve before proceeding to the next comparison cycle. The merit of this approach is that as long as there is enough time to finish a given comparison cycle, the recorded result is almost guaranteed to be correct. However, the drawback is that when metastability happens and one comparison cycle takes too long, later comparison cycles may not have time to even start, leading to sparkle codes. Furthermore, even if the comparator is not in metastability, the applied skew delays the generation of the ready signal and slows down each comparison cycle, which is undesirable especially when speed is a top priority.

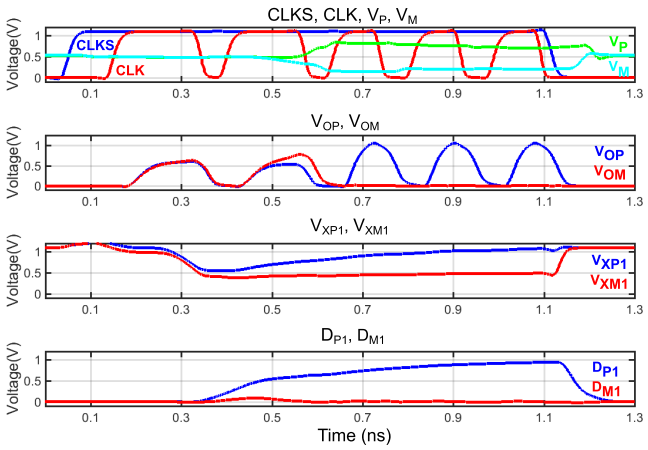

Fig. 2. Time-domain waveforms when MSB comparison is metastable.

In the other case, we can skew the comparator and/or the ready detector in an opposite direction so that the ready signal is generated even if the comparator has not fully resolved [1]. This essentially puts an upper limit on the maximum time that each comparison cycle takes. It ensures that the SAR operation would not be stuck at any comparison cycle. More importantly, it reduces the time for each comparison cycle, thereby accelerating the ADC speed by around 20% in simulation compared with the first case of waiting for the comparator to fully resolve every time. The drawback of this approach is that if the comparator output has not fully resolved, the latched comparison result may be wrong. Fig. 2 shows the waveform of a 5-bit SAR ADC that does not wait for the comparator to fully resolve when the MSB comparison is in metastability. Node voltages are plotted in different rows and color coded for separation. The subscript "1" indicates that the plotted signals correspond to the MSB comparison cycle. Since the comparator outputs $V_{\mathrm{OP/OM}}$ are not fully regenerated during the MSB comparison cycle, they stay close to each other around half V_{DD}. This leads to non-differential latch outputs $V_{\mathrm{XP1/XM1}}$ and DAC control signals $D_{P1/M1}$ during the second MSB comparison, causing wrong conversion results. In this case, the final ADC output is 00111, but the correct one should be 01111, indicating a sparkle code.

C. CDT Quantization and Sparkle-Code Removal

The fundamental cause for sparkle code is metastability, which happens when the comparator input is very close to zero (typically well within 0.1 LSB). This means that we already have an accurate conversion result before metastability happens. Thus, if we know which comparison cycle is in metastability, we can reproduce the correct ADC output based on prior comparison cycle outputs.

Because a long CDT is a direct manifestation of metastability, we can detect it by comparing the CDT with a reference delay τ, as shown in Fig. 3 [19]. The latch works as a 1-bit TDC. It is triggered during every comparison cycle. Its output is stored in an array of DFFs ($T_4 \sim T_0$) according to the comparison cycle CC_i for a 5-bit SAR ADC. This way,

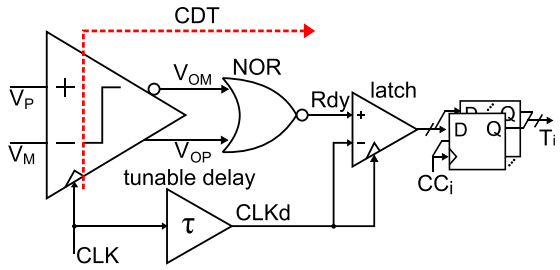

Fig. 3. CDT quantizer.

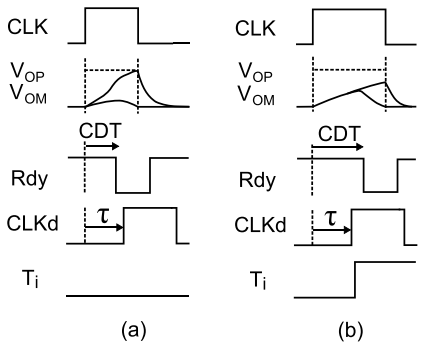

Fig. 4. Operation of the CDT quantizer. (a) Large input. (b) Small input.

when comparator metastability happens, we not only detect it but also know when it happens.

The operation of the CDT quantizer is shown in Fig. 4; when the comparator input is large, the CDT is shorter than the reference delay τ, resulting in $T_i = 0$. By contrast, when the comparator is in metastability, the CDT becomes longer than τ, yielding $T_i = 1$. Note that the CDT quantizer functions correctly as long as Rdy is accurate at the rising edge of $CLKd$, which can be guaranteed without any modification to the classic SAR ADC asynchronous clocking scheme. When the CDT is very close to τ, the T_i-storing D flip-flop (DFF) can be in metastability. Nevertheless, since the DFF is not inside the SAR loop, it does not need to be reset and thus can have much longer time to resolve than that of the comparator. Moreover, latch pipelining can be applied after the DFF to further substantially reduce the CDT quantizer metastability rate down to a negligible level [22].

Fig. 5(a) shows the timing diagram for a 5-bit SAR ADC in normal operation. Fig. 5(b) shows the case when the third comparison is metastable, leading to $T_2 = 1$. In this case, we can directly obtain the correct ADC output based on D_4 and D_3. We do not even need to know D_2 to D_0. In other words, when we see $T_i = 1$, we can directly assign D_i to D_0. Table I summarizes how the ADC output is corrected for any comparison cycle with a long CDT. For $T_2 = 1$, $\overline{D_4 D_3 D_2 D_1 D_0}$ is replaced by $\overline{D_4 D_3 011}$.

The CDT-based metastability detection works well in concept, but faces the challenge of PVT variation. Both the CDT and the reference delay τ vary with PVT. As shown in Fig. 6, if PVT variation elongates the CDT but shortens τ, T_i can be 1 even when the comparator is not in metastability. By contrast, if the CDT is shortened but τ is elongated, T_i can

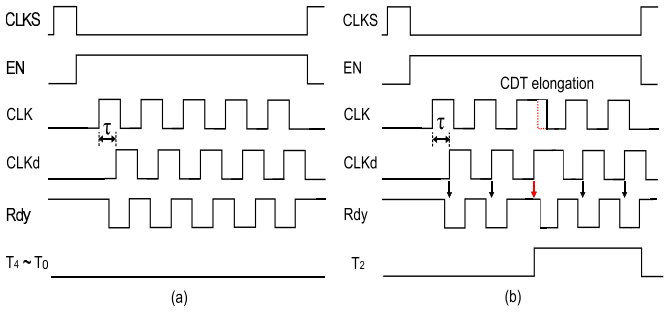

Fig. 5. Waveform (a) normal operation and (b) metastability in the third cycle.

TABLE I
MAPPING FROM THE RAW ADC OUTPUT TO THE CORRECTED OUTPUT

	D_4	D_3	D_2	D_1	D_0	T
$T_4 = 1$	0	1	1	1	1	1
$T_3 = 1$	D_4	0	1	1	1	1
$T_2 = 1$	D_4	D_3	0	1	1	1
$T_1 = 1$	D_4	D_3	D_2	0	1	1
$T_0 = 1$	D_4	D_3	D_2	D_1	0	1

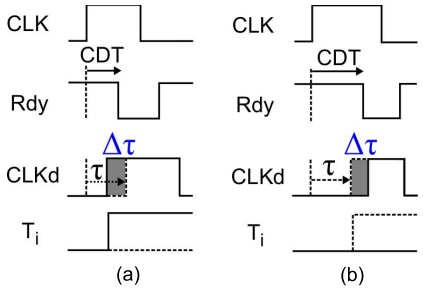

Fig. 6. PVT variation of the reference delay. (a) Large input. (b) Small input.

be 0 when metastability occurs. Both the cases cause metastability to be misidentified, leading to performance losses. Prior works rely on foreground manual tuning to set the correct reference delay τ [19], [20], but it cannot track environmental changes.

III. Proposed Sparkle-Code Correction Technique With Background Window Width Calibration and 1-bit Resolution Enhancement

A. Choice of τ and 1-bit Resolution Enhancement

The value of the reference delay τ needs to be set carefully as it marks the detection boundary. Let us define the value of the comparator input that produces an equal delay of τ as W, where W is inversely proportional to τ. The TDC can be considered as a window detector. It detects the comparator input that falls inside $[-W, +W]$. When the comparator input is within $\pm W$, the TDC output is 1, otherwise, the TDC output is 0. W needs to be set properly. It cannot be larger than 1 LSB, as otherwise, even when the comparator is in normal operation with an input greater than 1 LSB, it would be identified as being in metastability, causing ADC resolution degradation. W cannot also be too small, as otherwise, a long CDT may not be detected by the TDC, leaving some sparkle codes uncorrected.

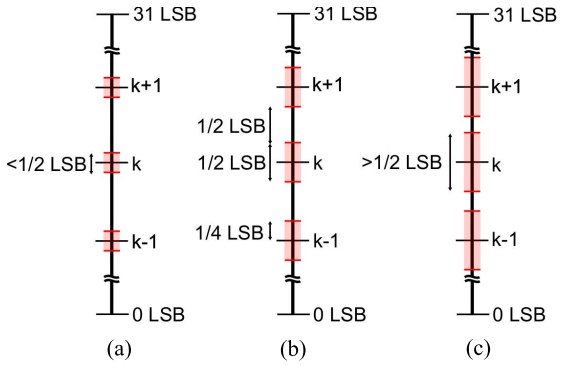

Fig. 7. Choice of the window width $W(\tau)$. (a) $W < 0.25$. (b) $W = 0.25$. (c) $W > 0.25$.

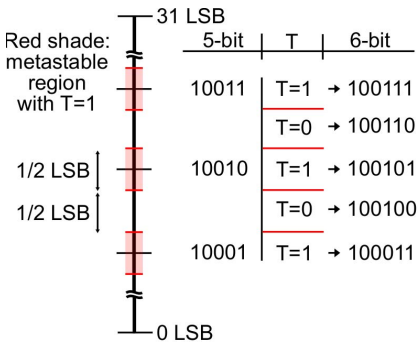

Fig. 8. Example of 1-bit enhancement with $W = 0.25$ LSB.

We choose the value of τ such that its corresponding W is 0.25 LSB. In other words, if the comparator input is within ± 0.25 LSB, its CDT is longer than τ, and the TDC output will be 1. Choosing $W = 0.25$ LSB ensures that all sparkle codes due to metastability are identified. More importantly, it enables 1-bit increase in the ADC resolution.

Fig. 7 compares three cases of W. The black vertical line indicates the ADC input–output ranging from 0 to 31 LSB for a 5-bit ADC. The red-shaded part indicates the region over which one TDC output T_i is 1. It is clear that if $W = 0.25$ LSB, the shaded and unshaded regions evenly divide up the ADC input–output range. This indicates that one extra bit can be obtained by making use of T_i. If we define $T = T_4||T_3||T_2||T_1||T_0$ (|| means OR operation. $T = 1$ when any T_i is 1), then T provides a 0.5-LSB quantization and can be directly concatenated with the corrected 5-bit ADC output $\overline{D_4 D_3 D_2 D_1 D_0}$ to obtain a 6-bit ADC output, as $\overline{D_4 D_3 D_2 D_1 D_0 T}$. This is also shown in Table I. T is now the new LSB of the 6-bit ADC: $T = 1$ when the input is in the red-shaped regions, and $T = 0$ otherwise.

Fig. 8 shows several example codes. A 6-bit digital output is obtained by using T as the new LSB. This is made possible by setting $W = 0.25$ LSB. It allows sparkle codes to be corrected along with 1-bit resolution enhancement.

B. Background Calibration of the Reference Delay τ

Since the window width W is set by the delay τ, τ needs to be controlled accurately. Nevertheless, this is non-trivial, because the delay is sensitive to PVT variations. Foreground calibration was used in [19] to manually tune τ, but it

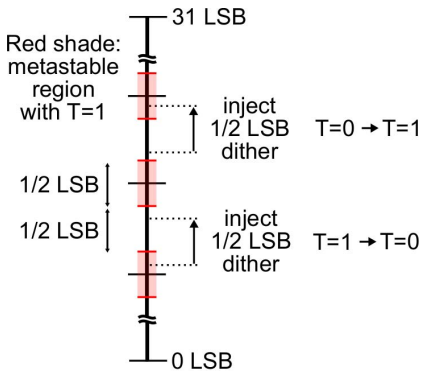

Fig. 9. Dither-based background calibration of window width W.

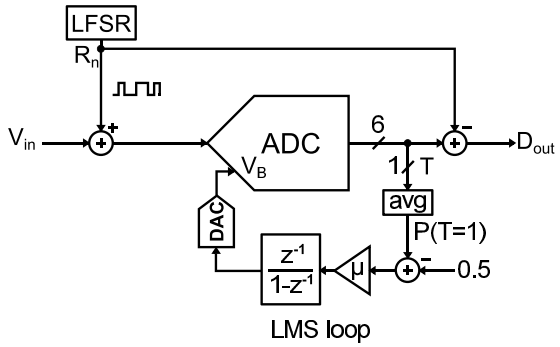

Fig. 10. Background calibration.

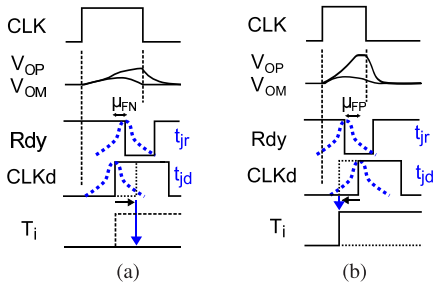

Fig. 11. Sparkle code from (a) false negative error and (b) false positive error.

cannot ensure robustness when voltage or temperature drifts. Background calibration is necessary to ensure PVT robustness.

The background calibration technique of [23] can be used to ensure $W = 0.25$ LSB. The key idea is based on monitoring the probability of $T = 1$. As shown in Fig. 7, as W increases, the red-shaded region enlarges, and thus there is a higher probability of $T = 1$ assuming a random input. Hence, by monitoring $P(T = 1)$ and adjusting τ to keep $P(T = 1) = 50\%$, we can ensure that $W = 0.25$ LSB across PVT variation.

The relationship between $P(T = 1)$ and the improvement in signal-to-quantization ratio (SQNR) can be derived as follows [23]:

$$\Delta\text{SQNR} = -10\log_{10}(1 - 3P + 3P^2) \tag{1}$$

where $P \equiv P(T = 1)$. It confirms that the maximum SQNR improvement is 6 dB and is achieved at $P(T = 1) = 50\%$.

This background calibration scheme works well for a busy ADC input. However, if the ADC input is a fixed dc value, the measured $P(T = 1)$ becomes strongly input-dependent and no longer correlates well with W. For example, if the dc input is right at the center of a red-shaded region of Fig. 7(b), $P(T = 1) = 100\%$ even though $W = 0.25$ LSB. This can cause τ to be incorrectly adjusted.

To increase the robustness of this background calibration technique, we propose to inject a 0.5-LSB pseudo-random dither into the SAR ADC during the ADC sampling phase. The addition of the dither, together with the inherent ADC noise, makes $P(T = 1)$ less dependent on the ADC input. As shown in Fig. 9, if an input falls into a $T = 1$ region, adding a dither pushes it into a region with $T = 0$, and vice versa. This way, to the first order, $P(T = 1)$ is decoupled from the ADC input. Even with a fixed dc input, $P(T = 1)$ depends on the window width W. Only the W value of 0.25 LSB ensures $P(T = 1) = 50\%$ with the 0.5-LSB dither injection. As a result, the proposed background calibration technique with dither can work for ADC inputs with various amplitudes, frequencies, and statistical distributions.

To prevent the signal-to-noise ratio degradation, the added dither is subtracted out from the ADC output in the digital domain. The tradeoff for adding the dither is reduced input signal swing by 1 LSB or 0.6 dB. This is to ensure that the summation of the input signal and the dither is within the full ADC range. Since this signal swing reduction is small, it is tolerable for most applications.

The operation of the proposed background calibration technique is shown in Fig. 10. The dither from the linear feedback shift register (LFSR) is injected to the input. $P(T = 1)$ is estimated in the background by passing T through a digital averager. Any deviation of $P(T = 1)$ from 50% is sensed and fed back using a classic least-mean-square adaptive filter loop [24] to tune V_B to ensure that $P(T = 1)$ stays close to 50%.

C. Metastability Detection Error Due to Jitter

The proposed metastability detection is a time-domain measurement and thus can produce error in the presence of jitter. The error can be classified into two types: false negative error and false positive error.

False negative error means that the comparator input is inside the window of ±0.25 LSB, but the CDT detector output $T_i = 0$. For example, the ADC input is 0.24 LSB, and T_4 should be 1 but turns out to be 0 due to jitter. This leads to a small error in the ADC output, but it is not a sparkle code, which is defined as a code whose error is greater than 2 LSB in this paper. Since 0.24 LSB is not very small, the comparator still has enough time to fully resolve. As a result, the 5-bit ADC conversion result is correct. The only error is in T and is small thus not a sparkle code. A false negative error produces a sparkle code only when the comparator input is very small and causes incorrect MSB codes, but still has $T = 0$. To calculate this probability, let us examine Fig. 11(a). In the presence of a very small comparator input, the nominal CDT is elongated by a time denoted as μ_{FN} without considering jitter. However, due to jitter, both arrival times of Rdy and $CLKd$,

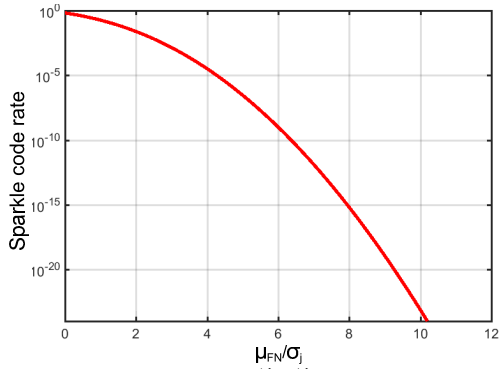

Fig. 12. Simulation of the false negative detection error rate.

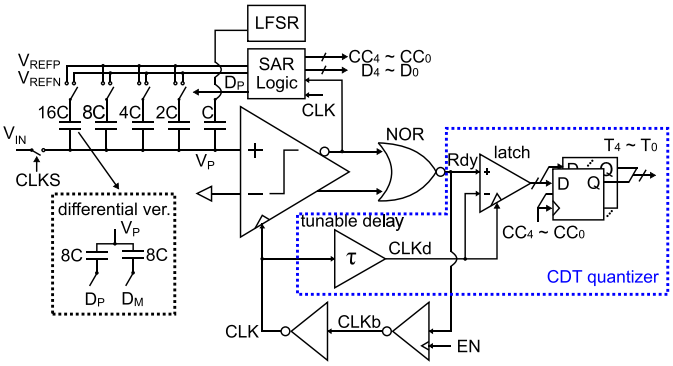

Fig. 13. Architecture of the proposed SAR ADC.

marked as t_{jr} and t_{jd}, follow normal distributions. Their differential jitter is denoted as σ_j, which is mainly caused by the thermal noise in the comparator, the XOR gate, the tunable delay line, and the latch. Note that since both t_{jr} and t_{jd} originate from the same comparator clock CLK, the jitter in CLK, which is the common mode jitter, does not matter. $T = 0$ happens when the differential jitter outweighs the CDT elongation μ_{FN}. Thus, we can derive the probability of a false negative error-induced sparkle code:

$$P\left(\frac{\mu_{FN}}{\sigma_j}\right) = \frac{1}{\sqrt{2\pi}} \int_{\frac{\mu_{FN}}{\sigma_j}}^{\infty} e^{-\frac{u^2}{2}} \cdot \mathrm{du} = \frac{1}{2}\left[1 - \mathrm{erf}\left(\frac{\frac{\mu_{FN}}{\sigma_j}}{\sqrt{2}}\right)\right] \tag{2}$$

where erf is the error function. The result is plotted in Fig. 12. The CDT elongation μ_{FN} is typically more than ten times larger than the rms jitter σ_j, and thus, the rate of false negative error-induced sparkle code is below 10^{-20}. For example, in the prototype ADC, to produce a sparkle code as in Fig. 2, μ_{FN} is 14 ps while σ_j is only 1.2 ps in simulation, resulting in a negligible sparkle-code rate.

False positive error means that the measured $T_i = 1$ but its corresponding comparator input is actually outside the window of ± 0.25 LSB. For example, the ADC input is 0.26 LSB but $T_4 = 1$. Since the comparator is not in metastability, the original ADC output $D_{out} = 100\,000$ is actually correct, but because $T_4 = 1$, D_{out} is mapped to 011111 using Table I. Since this error is small, it is not a sparkle code. A false positive error produces a sparkle code only when the comparator input is larger than 2 LSB but still produces $T_i = 1$. To calculate this probability, we can use the same procedure as for the false negative error-induced sparkle-code calculation, and it is easy to show that it is given by

$$P\left(\frac{\mu_{FP}}{\sigma_j}\right) = \frac{1}{2}\left[1 - \mathrm{erf}\left(\frac{\frac{\mu_{FP}}{\sigma_j}}{\sqrt{2}}\right)\right] \tag{3}$$

where μ_{FP} represents the CDT differences between the comparator inputs of 0.25 and 2 LSB [see Fig. 11(b)]. It can be estimated as $\mu_{FP} \approx \ln(2/0.25) \cdot \tau_{rg} \approx 2\tau_{rg}$, where τ_{rg} is the comparator regeneration time constant. μ_{FP} does not depend on the size of LSB. Typically, it is an order of magnitude higher than the rms jitter σ_j. Taking the prototype ADC as an example, μ_{FP} is 18 ps or $15\sigma_j$. This translates to a very low sparkle-code rate below 10^{-25}.

In summary, the proposed technique cannot completely eliminate all sparkle codes in the presence of jitter, but it can suppress the sparkle-code rate to be lower than 10^{-20} for a practical design with a typical CDT timing separation greater than ten times of the rms jitter.

IV. Prototype SAR ADC Design

Fig. 13 shows the single-ended schematic of the prototype ADC. The real implementation is fully differential. The core is a 5-bit asynchronous SAR. After sampling using the bootstrapped switches, EN turns high and starts the first comparison [Fig. 5(a) shows the timing diagram]. A dynamic NOR gate detects when the comparison finishes. After two inverter delays, it triggers the comparator reset and then initiates the next comparison. To speed up the ADC, the comparator and the NOR are skewed in such a way that the ready signal can be regenerated before waiting for the comparator to completely resolve. We essentially adapt the second design scheme discussed in Section II-B. It avoids being stuck at a given comparison cycle in the presence of metastability. The main source for sparkle codes in this design is an incorrect comparator output when metastability occurs (see Fig. 2). These sparkle codes are detected by the CDT quantizer and corrected using Table I. A 20-bit LFSR produces the dither needed for the background reference delay calibration.

The SAR logic counts the comparison cycle [CC_i being 1 indicates the $(5 - i)$th comparison cycle] and records the comparator outputs ($D_4 \sim D_0$) using dynamic logic circuits of Fig. 1(b) to increase speed and save power.

The use of a 0.5-LSB dithering doubles the total cap DAC size. Thus, in the end, the overall DAC size of the prototype ADC is the same as a classic 6-bit SAR. The size of the custom-made unit metal-oxide-metal (MoM) capacitor is 0.25 fF. It saves area and power, but is still sufficient for 6-bit matching accuracy. The DAC switching scheme of [25] is adapted to reduce the DAC switching power. By splitting DAC capacitors in half, it effectively realizes V_{cm}-based switching but without the need to connect capacitors to V_{cm}.

Fig. 14(a) shows the schematic of the three-stage comparator used in this ADC. The comparator input referred noise is 1 mV. It does not consume any static current and only

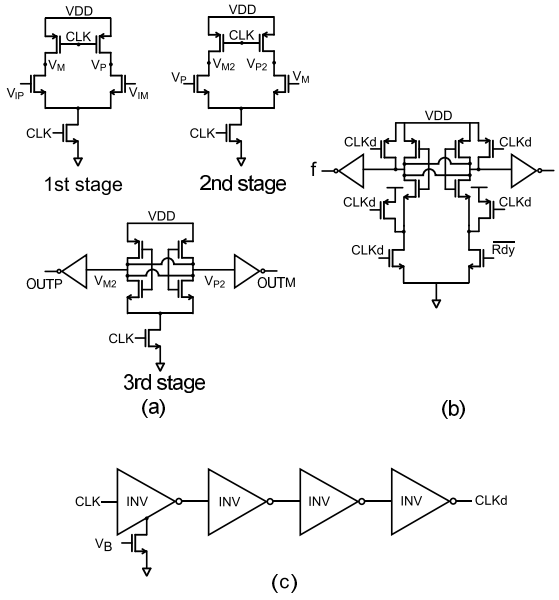

Fig. 14. Schematics of (a) comparator, (b) latch, and (c) tunable delay.

consumes dynamic current during evaluation. It consists of two dynamic pre-amplifier stages and one regeneration latch stage. It is faster than the strong-arm latch as it avoids vertically stacking multiple layers of transistors, which slows down the regeneration phase. It is also found to be faster than the two-stage dynamic comparator of [26]. First, it avoids the use of a PMOS tail in the latch stage, which is slower than having an NMOS tail. Second, the proposed three-stage comparator only uses a single clock phase CLK, while the two-stage design requires both CLK and $CLKb$. $CLKb$ needs additional buffering to drive the PMOS load, which slows down the asynchronous clocking loop (see Fig. 1). Third, the use of two pre-amplifier stages with reduced load on each stage supports a wider bandwidth than a single pre-amplifier with a heavier load. Last but not least, all signal path transistors in the proposed two pre-amplifiers operate in the saturation region and thus provide a large gain to shorten the time needed for the regeneration phase. By contrast, the load transistor ($M10$ and $M11$) of the pre-amplifier in [26] operates in the linear region, leading to a small pre-amplifier gain and requiring more regeneration time.

Fig. 14(b) shows the schematic of the latch in the CDT quantizer. As $CLKd$ and $\overline{Rdy}$ are both zero at sampling, the tail transistor is removed for the fast latching, since fewer number of transistors are stacked. The tunable delay line is shown in Fig. 14(c). It uses the standard current-starved inverter followed by three buffers. V_B is controlled externally. The delay can be tuned from 30 to 150 ps by varying V_B from 1.1 to 0.4 V. This range is sufficient to ensure that the delay can be set correctly to obtain $W = 0.25$ LSB.

V. Measurement Results

The prototype ADC built in 40-nm LP CMOS occupies 0.003 mm^2. The power supply voltage is 1.1 V, and the differential input signal swing is 1.4-V peak-to-peak. Fig. 15 shows the die photograph.

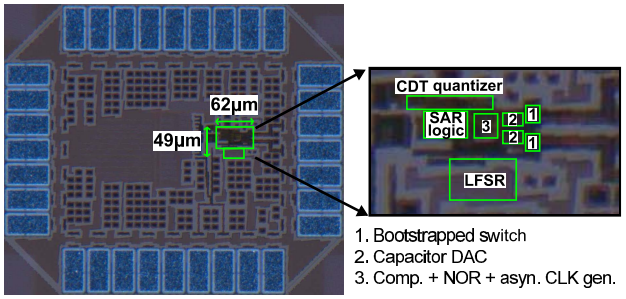

Fig. 15. Chip die photograph.

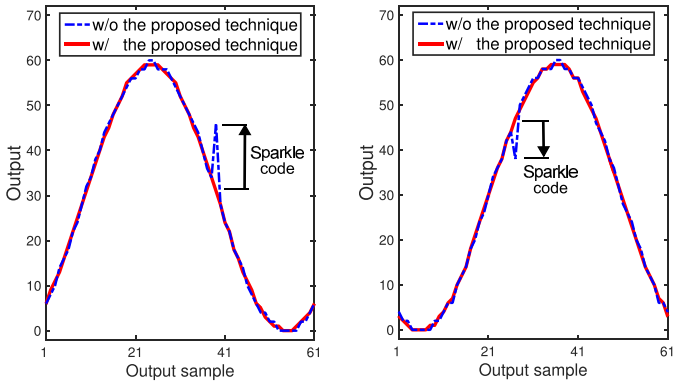

Fig. 16. Measured ADC output waveform with sparkle codes.

Fig. 16 shows two measured ADC output waveforms with sparkle codes: one sparkle code happens at the MSB and the other occurs at the second MSB. With the proposed technique, both sparkle codes are detected and corrected using Table I.

Since the thermal noise can also cause small bit flips, we define the detection of a sparkle code event only when the ADC error is greater than 2 LSB in 5-bit scale (or 4 LSB in 6-bit scale) as mentioned earlier. The measured sparkle-code occurrence is 1.9×10^5 out of 2×10^9 samples, leading to an error rate of approximately 10^{-4}. With the proposed sparkle-code reduction technique, we cannot measure any sparkle code, which indicates that the proposed technique has suppressed the sparkle-code rate to be below 5×10^{-10}.

Fig. 17 shows the histogram of the measured locations of the sparkle codes before correction. As expected, since metastability can happen during any comparison cycle, sparkle codes show up at all major MSB transitions. They do not show up at lower LSBs, because LSB errors cannot produce a sparkle code with error magnitude greater than 4 LSB in the 6-bit scale. We have also measured the magnitude distribution of the sparkle-code errors, which is shown in Fig. 18. The largest error magnitude is 17 LSB, which happens when the MSB comparison is in metastability. Reason for the asymmetric distribution of the above-mentioned histograms is thought to be mismatches between the two differential half circuits. It is found from post-layout extraction that there is a 10% systematic mismatch between the parasitic capacitances at the comparator output nodes, causing unbalanced outputs.

We have also measured the uncorrected sparkle-code rate as a function of the sampling frequency. The sparkle-code rate is normalized to the value at 700 MHz. The measurement

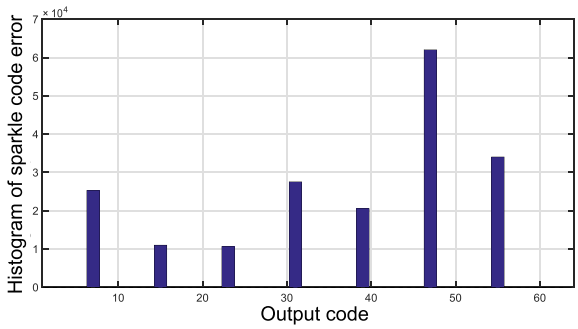

Fig. 17. Histogram of the location of the sparkle codes.

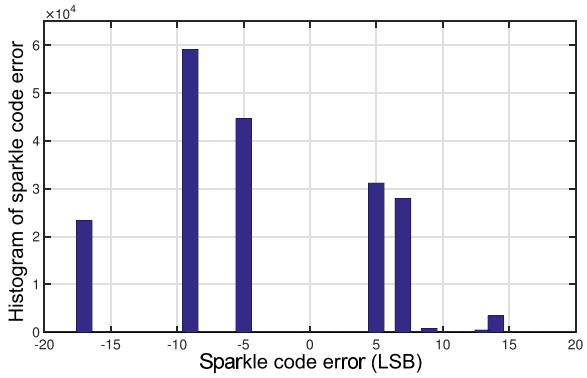

Fig. 18. Histogram of the magnitude of the sparkle codes.

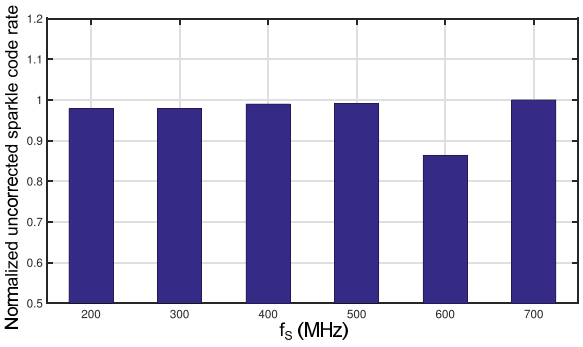

Fig. 19. Measured sparkle-code rate versus sampling frequency.

result of Fig. 19 shows that the sparkle-code rate remains almost flat across the sampling frequencies from 200 to 700 MHz. This shows that the dominant source for sparkle codes is incorrect comparator output, not unfinished SAR operation. This measurement result is expected, as we adapt the design scheme of allowing the comparator ready signal to be produced even if the comparator has not fully resolved, as mentioned in Section IV. By contrast, for the asynchronous design without skewing the comparator and/or the ready detector, the unfinished SAR operation would be the main cause. In this case, slowing down the ADC sampling rate would provide more time for the comparator to resolve outputs to the valid levels, thereby substantially reducing the sparkle-code rate. Therefore, sparkle-code rate at 200 MHz would be much smaller than that at 700 MHz. Also, there would be much fewer sparkle codes at the first and

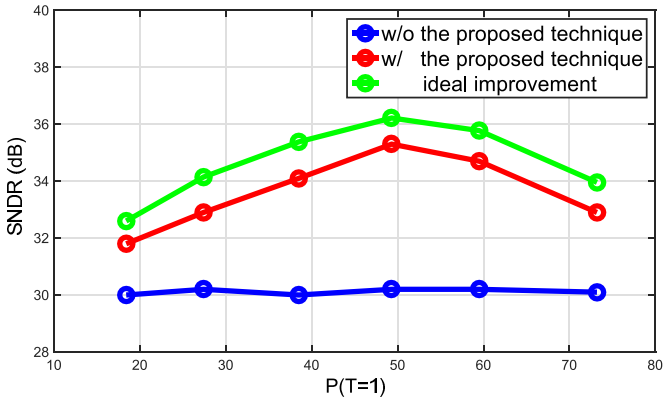

Fig. 20. SNDR versus the probability of $T = 1$.

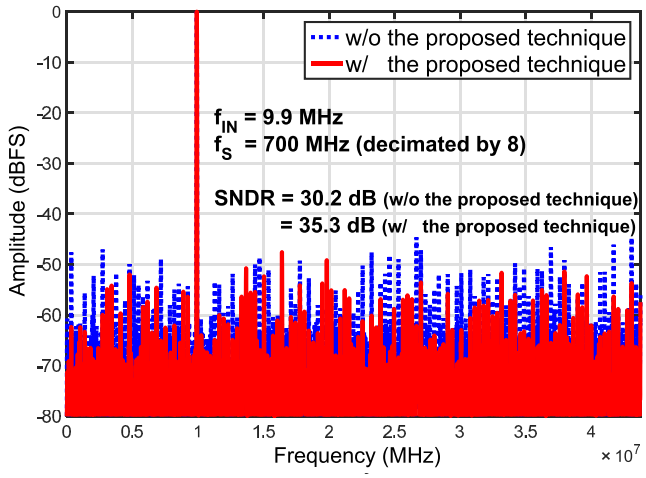

Fig. 21. Measured ADC spectrum (2^{13} points).

second MSB codes than at the third MSB codes. However, neither of them are consistent with the measurement results in Figs. 17 and 19.

The measured resolution improvement using the proposed technique versus $P(T = 1)$ is shown in Fig. 20. As expected, $P(T = 1) = 50\%$ leads to the largest SNDR improvement. The green curve indicates the theoretical upper limit for the resolution improvement from (1). The measured result follows it. There is a small 1-dB difference, which is due to ADC noise and capacitor mismatch that are not considered in (1). The measurement result of Fig. 20 also validates the proposed background calibration technique: by adjusting the delay τ and keeping $P(T = 1) = 50\%$ in the background, we can ensure robust operation across PVT variation. Measurement shows that 10^3 samples are sufficient to provide an accurate estimate for $P(T = 1)$ in the background with a standard deviation of 1%. Assuming $P(T = 1)$ is adjusted by 1% during every background calibration cycle, the total convergence time is less than 5×10^4 samples or 0.1 ms, even considering a pessimistic calibration starting point of $P(T = 1) = 0$ or $P(T = 1) = 100\%$.

Fig. 21 shows the measured ADC spectrum. The sampling rate is 700 MS/s, and the output is decimated by 8 to simplify testing. The measured SNDR of the 5-bit ADC core is 30.2 dB.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	This work	[18]	[19]	[7]	[9]	[12]	[27]
Feature							
Sparkle-code reduction	**O**	O	O	X	X	X	X
1-bit resolution enhancement	**O**	X	X	X	X	X	X
Background calibration	**O**	X	X	-	-	-	-
Chip performance							
Technology (nm)	**40 LP**	65	28 SOI	40	40 LP	40	28 SOI
Type	**SAR**	3b/c TI SAR	TI SAR	LU SAR	SAR	ciSAR	TI SAR
Sampling rate (GS/s)	**0.7**	1.25*	0.64*	1.25	0.7	1	1.25*
Bits	**6**	6	6	6	6	6	6
SNDR (dB)	**35.3**	30.3	25.2	31.8	34.8	34.6	33.8
ENOB	**5.57**	4.74	3.89	4.99	5.5	5.46	5.32
Power (mW)	**0.81**	1.38*	5.3*	7.26	0.95	1.26	4*
Area (mm^2)	**0.0031**	0.008	0.14	0.014	0.004	0.00058	0.009
FOM (fJ/conv-step)	**24.4**	41.3	555	183	30.0	28.7	80.1
*single-channel performance							

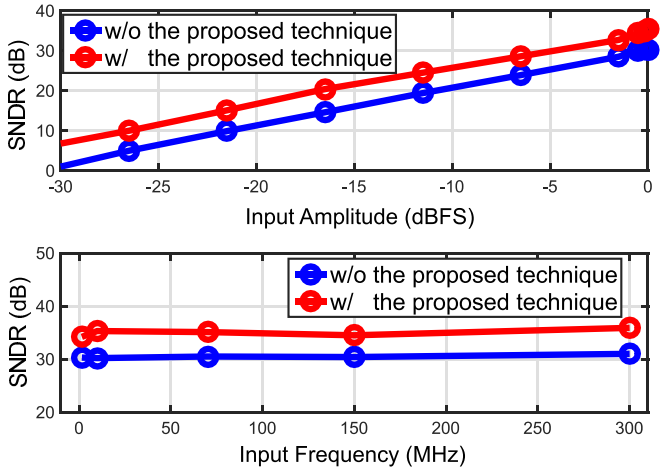

Fig. 22. SNDR versus input amplitude and frequency.

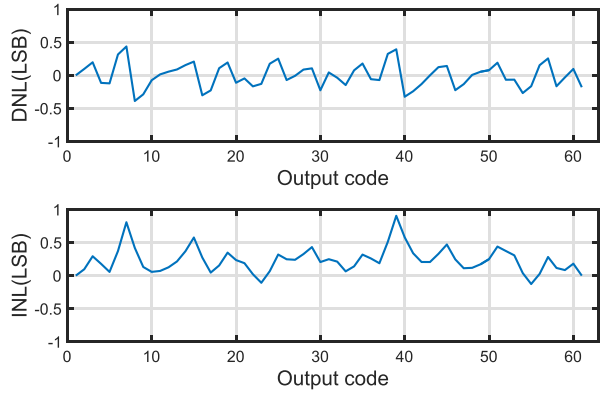

Fig. 23. Measured DNL and INL plots.

It increases to 35.3 dB with the proposed resolution enhancement technique. The measured SNDR versus input amplitude and frequency is shown in Fig. 22. Consistent SNDR improvement is obtained. The measured integral non-linearity (INL) and differential non-linearity (DNL), shown in Fig. 23, are +0.9/−0.1 and +0.5/−0.4 LSB, respectively, limited by capacitor mismatch.

The measured total ADC power is 0.81 mW. The total analog power consumed by comparator, asynchronous clock generation, and CDT quantizer is 0.4 mW. Further power breakdown cannot be measured as they share the same analog supply. SPICE simulation shows that the CDT quantizer consumes 33% of the total analog power, and thus, its power is estimated to be 0.13 mW. The measured reference power is 0.07 mW. The measured digital power consumed by SAR logic and LFSR is 0.34 mW.

Table II compares the performance of this ADC with other works with similar resolution and speed. Its measured Walden FoM of 24.4 fJ/conversion-step is in-line with the state-of-the-art ADCs. The key highlights of this paper are: 1) it can correct metastability-induced sparkle code; 2) it provides 1-bit resolution enhancement; and 3) the tuning of the reference delay can work in the background.

VI. CONCLUSION

This paper presented a sparkle-code correction technique for high-speed single-channel SAR ADCs. It can reduce the sparkle-code error rate by more than four orders of magnitude. Moreover, it can increase 1-bit ADC resolution by setting the metastability detection window to be 0.25 LSB. The robustness of the proposed technique is ensured by a novel dither-based background calibration technique based on probability measurement.

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