

Single Photon-Counting Pixel Readout Chip Operating up to 1.2 Gcps/mm² for Digital X-Ray Imaging Systems

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Abstract—This paper presents the design of a PXF40—an ultrafast single photon-counting (SPC) readout front-end electronics implemented in a CMOS 40-nm technology dedicated to hybrid pixel detectors. The prototype application specific integrated circuit core is a matrix of 432 pixels (24×18) with a $100 \mu\text{m} \times 100 \mu\text{m}$ size. The single processing channel consists of a charge-sensitive amplifier (CSA), a discriminator, and a 24-bit counter with logic circuitry. The input signal is amplified and formed only by the CSA stage. Depending on the CSA input transistor current value, it can operate in two modes: FAST and FAST_HC with higher current. The measured power dissipation per channel $P = 45 \mu\text{W}$ and noise ENC = $212 \text{ e}^- \text{ rms}$ for the FAST mode, while $P = 100 \mu\text{W}$ and ENC = $185 \text{ e}^- \text{ rms}$ for the FAST_HC mode, respectively. The readout chip can count up to 1.2 Gcps/mm^2 based on 10% dead-time loss input rate parameter, which is currently the fastest SPC-based solution.

Index Terms—Charge-sensitive amplifier (CSA), front-end electronics, high count rate, pixel detector, single photon counting (SPC), X-ray imaging.

I. INTRODUCTION

SiTRIP and pixel silicon detectors have been successfully applied in numerous high-energy physics experiments for nearly four decades. They also pave the way for the use of different digital X-ray imaging applications in material science, biology, and medicine [1]–[3]. The development of such kinds of systems opens the door for new applications and extends the list of their usage. The architecture of a digital X-ray imaging application contains an X-ray source, a target object, and a detecting system. The detecting system usually consists of a sensing element connected to a readout application specific integrated circuit (ASIC), which is connected to an external host system.

Depending on the way in which the radiation quantum is transferred into an electrical charge, the sensing elements can

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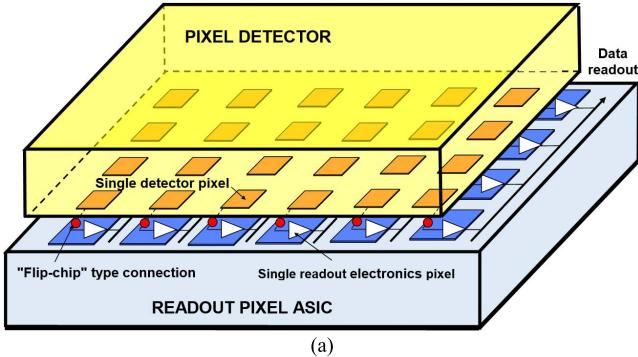
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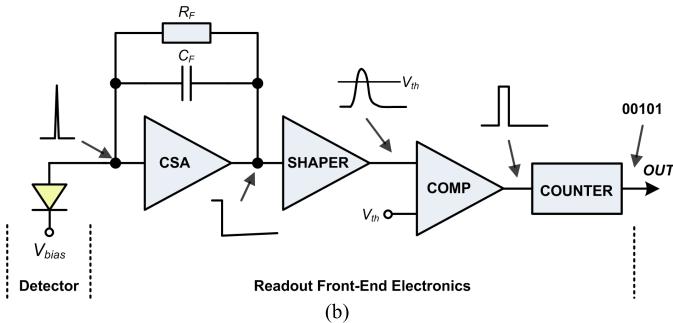
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be classified as indirect or direct conversion type. The indirect detection sensing element converts the impinging photon energy in two phases. During the first phase, the sensing element (e.g., scintillator material) converts the photon energy into visible light flash. Secondly, the light flash is detected by a silicon photodiode in a readout ASIC underneath the sensing material. Examples of applications based on indirect detection combined with photon-counting image sensor are [4] and [5]. Contrary to indirect detection, in direct detection, the photon energy is directly converted into electrical charge in a single phase, and this is the reason why direct detection-type sensors offer better spatial resolution and X-ray-to-charge conversion efficiency than indirect type sensors do. Direct conversion-based detectors are preferable in medical applications, where the reduction in radiation dose applied to the patient is very important. The direct conversion-based detectors are built with semiconductor materials, which are chosen depending on the application requirements.

Another detection system classification is based on the way in which the front-end channel processes the input charge generated by a photon and distinguishes an integration-type and a single photon-counting (SPC)-type system. In the case of integrating-type system, the input charges are integrated over a given exposure time. Thus, the information related to the individual photon energy is lost and only in the case of monochromatic photons' flux, the exact number can be determined. In addition, during exposition time, they also integrate noise, which degrades the signal-to-noise ratio and dynamic range of the detecting system. The second approach is the SPC, which has become more and more popular in recent years. In the SPC detector, each impinging photon generates charge in a single detector pixel (or strip), which is processed independently by a single readout front-end channel [see Fig. 1(a)]. The readout channel usually consists of a charge-sensitive amplifier (CSA), a pulse-shaping amplifier (shaper), a comparator (also called discriminator), and a counter [see Fig. 1(b)] [6]. If a pulse amplitude at the comparator input is above the applied threshold voltage, the counter value is incremented. Due to the multichannel nature of such readout ASICs, the requirements for low-noise signal processing [7], [8] and readout channels' analog parameters' homogeneity [9] are usually the most important and challenging as well.



(a)



(b)

Fig. 1. (a) 2-D hybrid pixel detector system: each detector pixel is connected to an independent pixel of a readout channel in the ASIC. (b) Simplified architecture of a readout channel operating in the SPC mode.

The SPC-based signal processing technique is typically applied in 2-D hybrid pixel detectors [10]–[19], where the sensor and the readout front-end electronics pixels have the same geometry and are connected using the flip chip bonding technique [see Fig. 1(a)]. In addition, the hybrid detectors allow using different sensors and readout ASIC materials to meet the system requirements. For medical applications involving higher photon energies, the high-Z sensor material is preferable (like CdTe, CdZnTe, and GaAs).

The main advantages of SPC detectors compared to the integration-type detectors are as follows:

- 1) very high dynamic range determined by counter depth;
- 2) noiseless imaging (properly set discriminator threshold cuts off the noise and only valid photon-related hits are counted);
- 3) the possibility of counting photons only within a given energy window in systems with two or more discriminators.

However, SPC systems are slower than integrating detectors in terms of count rate (number of photon/s) which can be processed per pixel.

Coping with high intensity of input pulses by the SPC systems paves the way for their use in medical X-ray imaging applications, which usually operate with high photon flux (see Table I, where Gcps/mm^2 means giga count per second/ mm^2). In the case of material science experiments based on synchrotron radiation detection, there is an emerging need to operate with a very high photon flux of low energy (e.g., 8-keV photons).

In this paper, a new approach facing high count rate of the SPC is presented. The authors analyzed the CSA transmittance

TABLE I
GENERAL SPECIFICATION FOR X-RAY IMAGING
AND COMPUTED TOMOGRAPHY [20]

	Mammography	General X-ray radiography	Computed tomography
Count rate [Gcps/mm ²]	0.05	0.001 – 0.5	1
Pixel pitch [μm]	typ. 85	typ. 150	55 – 1000
Energy range [keV]	28 – 40	70 – 120	80 – 140

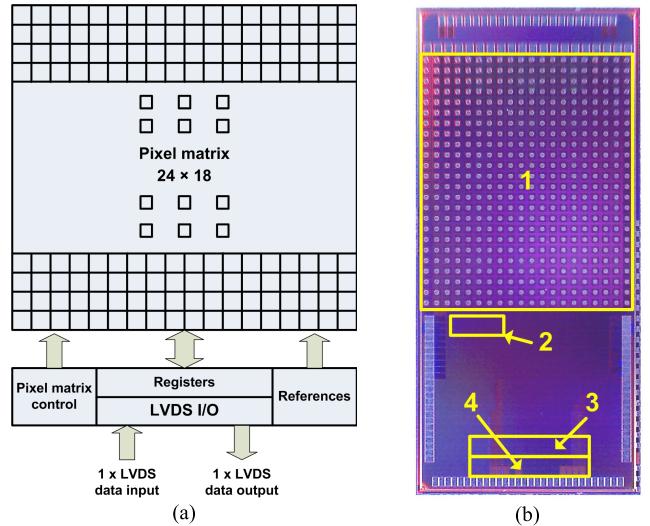


Fig. 2. Prototype chip. (a) Simplified block diagram. (b) Photograph with marked functional blocks: (1) pixel matrix, (2) references, (3) pixel matrix control and registers, and (4) LVDS I/O.

function pole locations and their influence on its output waveforms, which implies count rate performance, and chose deep submicrometer 40-nm CMOS technology to achieve possible short CSA output pulse, which is the key to improve the readout front-end electronics speed performance. In addition, the use of deep submicrometer technology allows reducing the silicon area of the single-pixel digital part and keeping and/or increasing its functionality at the same time. It enables fitting the single pixel in the smaller pitch or increasing the analog part functionality and performance.

This paper presents the design and tests of integrated circuit called PXF40 operating in the SPC mode able to cope high photon's flux intensity, which breaks the limit of 1 Gcps/mm². This paper consists of four sections. The architecture details of the prototype ASIC are described in Section II. Section III provides theoretical analysis of the fast pulse signal processing in the CSA. Measurement results with an emphasis on the count rate performance are presented in Section IV.

II. PROTOTYPE ASIC ARCHITECTURE

The prototype PXF40 IC core is a matrix of 24×18 square pixels with a pitch of $100 \mu\text{m}$. At the ASIC bottom part, there are periphery blocks [reference bias blocks, registers, LVDS I/O blocks, and pixel matrix control block (see Fig. 2)].

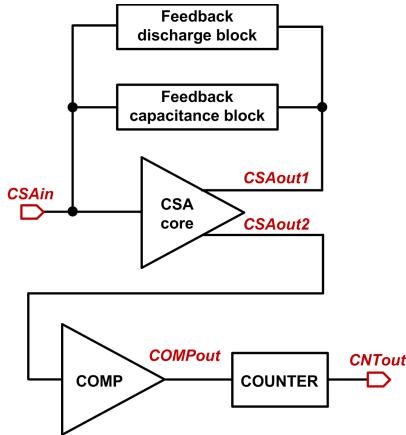


Fig. 3. Block diagram of the presented readout front-end electronics analog part.

The chip was designed for testing different circuitry:

- 1) new blocks for fast signal processing operating in the SPC mode, which are the main subject of this paper;
- 2) modified blocks for inter-pixel communication mode to eliminate the effects of charge sharing, which becomes visible for a small pixel size [21]–[24].

Each of these operates individually and requires to set the CSA in a different mode. In addition, the inter-pixel communication mode is enhanced by two shapers (fast and slow), one discriminator, and four comparators. In this mode, the emphasis is put on the pixel-to-pixel gain and noise uniformity, whereas in the fast signal processing mode it is on the high count rate performance.

When the pixel matrix operates in the SPC mode, each pixel processes the input pulses independently (acquisition phase) and the pulses are counted by a 24-bit ripple counter in each pixel separately. When the data acquisition phase finishes, the pixels' counters form column shift registers. The data from these registers are shifted out via an LVDS transmitter. The main shift register is also used to control the channels' operation, whose configuration is received by the LVDS receiver.

A. Readout Front-End Electronics Architecture for Fast Signal SPC mode

The fast signal processing path consists of a CSA, a comparator, and a 24-bit ripple counter (see Fig. 3).

The CSA core is a voltage amplifier based on a folded cascode architecture (see Fig. 4). The CSA input transistor M1 was selected as a PMOS type with dimensions of $W = 18 \mu\text{m}$, $L = 0.2 \mu\text{m}$ and it is supplied by voltage $V_{ddm} = 0.9 \text{ V}$, while the rest of the CSA circuitry (and analog blocks) is supplied by $V_{dda} = 1.2 \text{ V}$. This enables to reduce power consumption; especially, in our case where the transistor M1 drain current I_{DM1} is of the order of tens of microamperes. The M1 transistor dimensions were chosen to achieve a possible low value of the equivalent noise charge (ENC) [6], [7], which is a measure of a circuit noise performance. We assumed that the detector capacitance C_{DET}

can be in a range from 50 to 150 fF, which is a typical value in the case of hybrid pixel detectors for a given pixel pitch and detectors parameters. The CSA output stage consists of two source followers to separate the CSA feedback circuitry from the next stage of the processing chain.

The CSA feedback circuitry consists of capacitance and discharge and leakage current compensation blocks (see Fig. 4). The CSA capacitance block core is a set of seven MOM-type capacitors (one for C_{F1} and six for C_{F2}) of 1.2 fF each. The capacitor $C_{F1} = 1.2 \text{ fF}$ is fixed, while the value of the capacitor C_{F2} can be digitally programmed from 1.2 fF to $1.2 + (0.6; 1.2; 2.4) \text{ fF}$, where values of capacitances in parenthesis are controlled by a 3-bit word. The separation of the CSA feedback C_F capacitance into two C_{F1} and C_{F2} capacitors is a result of a tradeoff between its gain, noise, and stability issues [25], [26]. The role of this block is to provide gain switching in the case of the fast signal processing mode (low, medium, and high gain) and gain correction to achieve good pixel-to-pixel gain uniformity in the case of the inter-pixel communication mode, which is important for the proper photon allocation to hit pixel.

When an X-ray photon hits a detector pixel, it generates in its active volume a number of electron-hole pairs proportional to the photon's energy, which induces a short current pulse at the pixel electrodes. This current pulse charges the CSA feedback capacitance C_F giving at the CSA output a voltage step. The feedback discharge block is responsible for the effective CSA feedback capacitance C_F fast discharging and for the detector leakage current I_{LEAK} compensation at the same time. The CSA discharge block is based on the Krummenacher feedback structure [27], and it shapes the CSA output as a short voltage pulse of the width in nanoseconds range. This allows us to omit the problem of the CSA output saturation for a high rate of input pulses. The discharge feedback structure can be modeled as two equivalent feedback paths:

- 1) resistive dc path of $R_F = 2/g_{M11}$ value, assuming $g_{M11} = g_{M12}$, to provide a path between the CSA input and output;
- 2) inductive path of $L_F = (2 \times C_X)/(g_{M12} \times g_{M14})$ value to provide detector leakage current I_{LEAK} compensation.

The C_X capacitance equals 1.34 pF and it is based on 16 parallel connected 1.8V-PMOS transistor with the following dimensions: $W = 5.5 \mu\text{m}$ and $L = 2 \mu\text{m}$.

The discharge current I_{KRUM} can be changed within a wide range from 0.1 to 300 nA (allowing a stable circuit operation), which gives effective resistance R_F values from 1 GΩ to 0.6 MΩ.

Depending on the CSA input transistor M1 current I_{DM1} value for the effective CSA feedback resistance R_F of the order of MΩ, the input stage operates in the following modes:

- 1) FAST mode: $I_{DM1} \approx 20 \mu\text{A}$ (CSA GBW = 5.3 GHz);
- 2) FAST_HC mode with higher current value: $I_{DM1} \approx 60 \mu\text{A}$ (CSA GBW = 8.4 GHz).

Both modes are dedicated to high-speed pulse processing (input pulse time processing around tens of nanoseconds). However, FAST_HC mode provides lower noise at the cost of higher current.

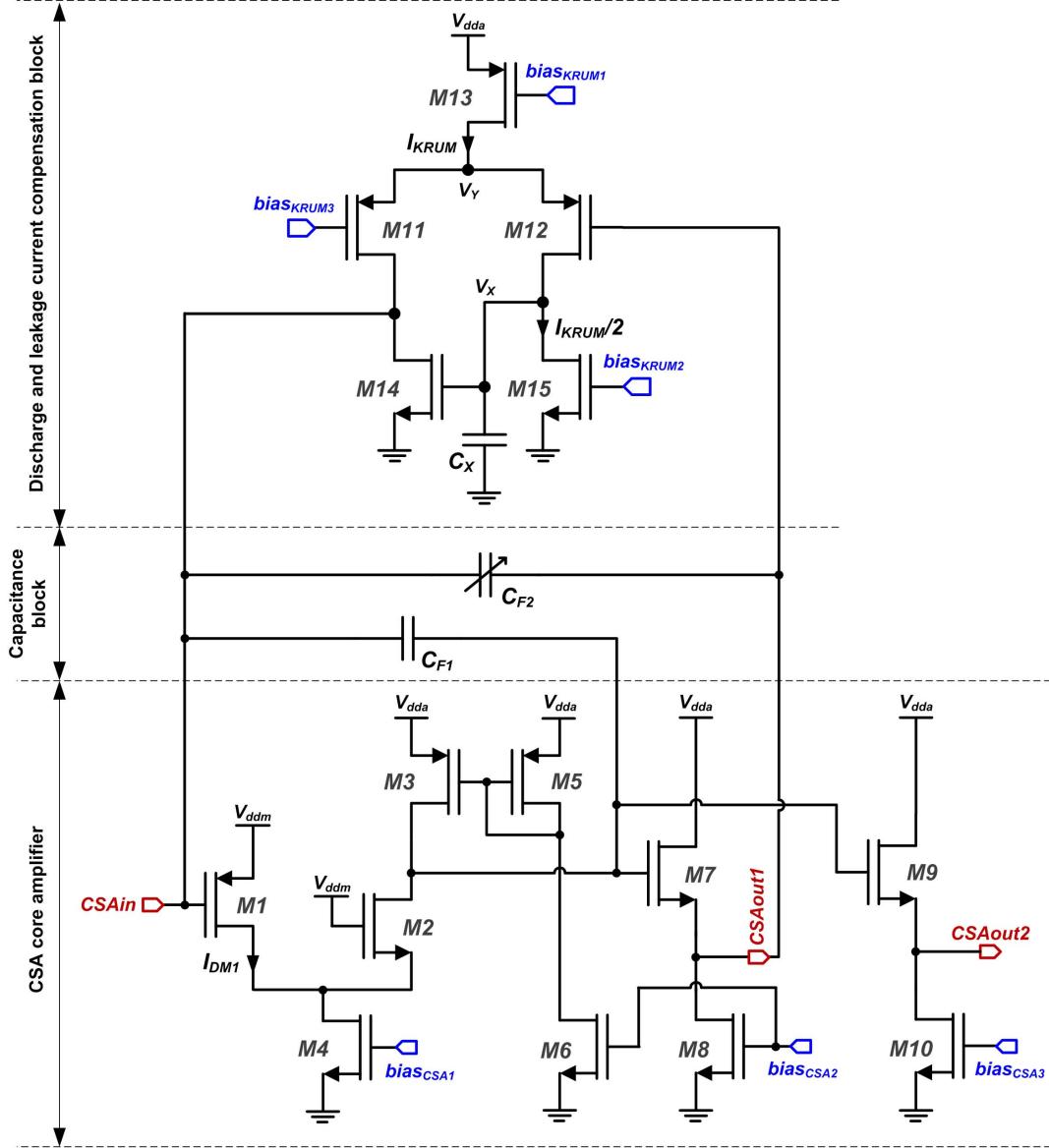


Fig. 4. Architecture of the CSA blocks: core amplifier, feedback capacitance, discharge and leakage current compensation.

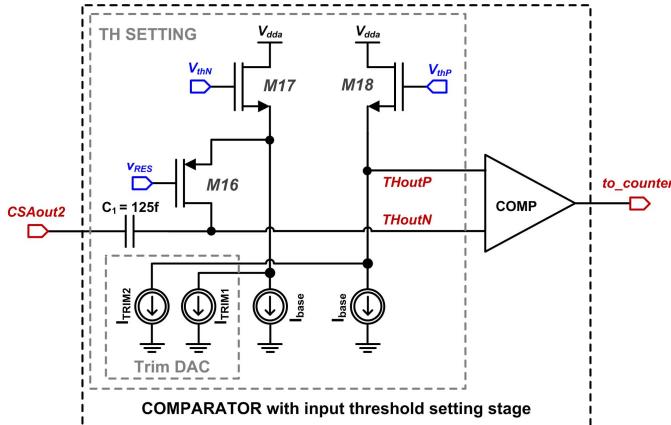


Fig. 5. Architecture of threshold setting stage at the comparator input.

The CSA is followed by an ac-coupled comparator block (see Fig. 5). A discriminator threshold is set globally in the pixel matrix by applying a differential voltage $V_{thP} - V_{thN}$

to all pixels (to the gates of the source followers M17–M18).

Due to mismatch effects (comparator offsets, dc level spread from pixel to pixel, etc.), the effective threshold level at the discriminator input (which is equal to $V_{S18} - V_{S17}$, where V_{Sx} is the M_x transistor source voltage) can significantly vary from pixel-to-pixel. The threshold setting block provides not only threshold setting functionality, but also the correction of the effective threshold level at the discriminator input in each pixel independently. Each pixel includes a 7-bit trimming digital-to-analog converter (trim DAC), which is used to correct the comparator input offset voltage. The trim DAC is implemented according to the binary weighted current sources architecture. In nominal case with zero comparator offset, the currents $I_{TRIM1} = I_{TRIM2} = I_{DAC}/2$, where $I_{DAC} = I_{TRIM1} + I_{TRIM2}$ is constant as a function of the trim DAC digital code. In the case of non-zero offset, the currents I_{TRIM1} and I_{TRIM2} are unequal. Thus, unequal transistors' M17 and M18 drain currents are related to different their gate-source V_{GS} voltages.

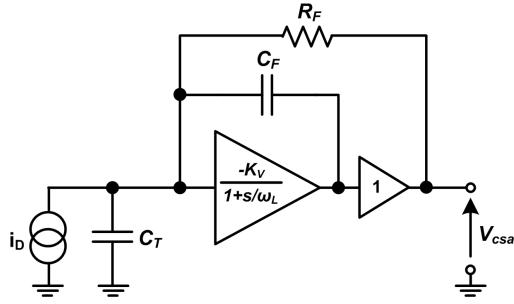


Fig. 6. Simplified model of the presented CSA stage.

By changing $I_{\text{TRIM}1}$ and $I_{\text{TRIM}2}$ currents by the same amount in the branches nearly linear differential voltage $V_{S18} - V_{S17}$ in terms of trim DAC control value is obtained.

The presented ASIC single-pixel size is $100 \mu\text{m} \times 100 \mu\text{m}$; however, it is mostly occupied by the circuitry needed for inter-pixel communication mode. The circuitry for fast signal processing occupies around 25% of the single-pixel area.

III. PULSE SIGNAL PROCESSING AND RATE CAPABILITY CONSIDERATIONS

The simplified model of the CSA stage, described in Section II-A, is presented in Fig. 6. The presented parameters are the following: K_V is the dc amplifier voltage gain, ω_L is the angular corner frequency related with amplifier high-impedance internal node $\omega_L = 1/(R_L \times C_L)$, R_F is the effective CSA feedback resistance, C_T represents all capacitances connected between the amplifier input and ground

$$C_T = C_{\text{DET}} + C_{g1} \quad (1)$$

where C_{DET} is the detector pixel capacitance (including parasitics) and C_{g1} is the CSA input transistor M1 gate capacitance.

The input CSA transmittance function $T(s)$ in general form can be expressed as [6]

$$T(s) = \frac{T_0}{s^2 + as + b} \quad (2)$$

where

$$T_0 = \frac{g_{m1}}{\zeta} \quad (3)$$

$$a = \frac{g_{m1} \times C_F}{\zeta} \quad (4)$$

$$b = \frac{g_{m1}}{\zeta \times R_F} \quad (5)$$

where g_{m1} is the CSA input transistor M1 transconductance and

$$\zeta = C_T C_L + C_T C_F + C_L C_F. \quad (6)$$

The transmittance function (2) can be analyzed using two approaches. Usually, in the detector readout systems denominator of (2) has two widely separated real poles, thus $T(s)$ can be rewritten as

$$T(s) = \frac{R_F}{(1 + s \times \tau_F) \times (1 + s \times \tau_R)} \quad (7)$$

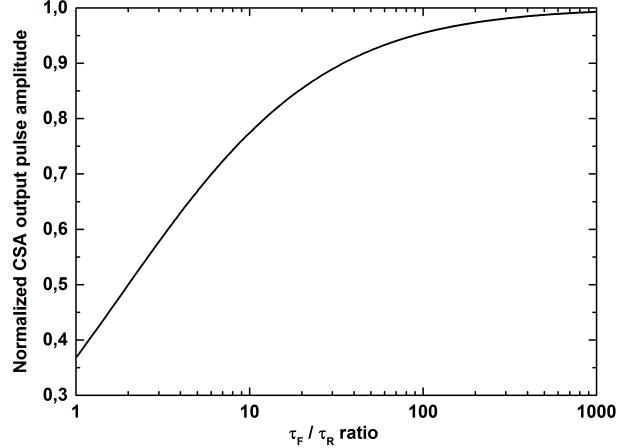


Fig. 7. Normalized CSA output pulse amplitude V_{ampl} in terms of τ_F/τ_R ratio.

where τ_F is the CSA feedback time constant

$$\tau_F = R_F \times C_F \quad (8)$$

and τ_R is the CSA output pulse rise time constant

$$\tau_R = \frac{\zeta}{g_{m1} \times C_F} \approx \frac{C_T \times C_L}{g_{m1} \times C_F}. \quad (9)$$

Taking the inverse Laplace transform of (7), the input amplifier pulse response in terms of input charge q_{in} is obtained as

$$V_{\text{out}} = \frac{q_{\text{in}}}{C_F} \frac{\tau_F}{\tau_R - \tau_F} (e^{-\frac{t}{\tau_R}} - e^{-\frac{t}{\tau_F}}). \quad (10)$$

The CSA output pulse amplitude V_{ampl} in terms of input charge q_{in} is equal to

$$V_{\text{ampl}} = \frac{q_{\text{in}}}{C_F} \times \left(\frac{\tau_F}{\tau_R} \right)^{\frac{\tau_R}{\tau_R - \tau_F}}. \quad (11)$$

Fig. 7 presents the normalized CSA output pulse amplitude V_{ampl} value in terms of τ_F/τ_R ratio according to (11).

Operating with a high rate of input pulses requires fast pulse signal processing by the input stage. Equation (10) reveals that to process input pulse in a shorter time, the CSA feedback time constant τ_F has to have a smaller value. At the same time according to (11), decreasing the ratio τ_F/τ_R , the lower fraction of the CSA output pulse amplitude maximum theoretical value

$$V_{\text{amplMAX}} = \frac{q_{\text{in}}}{C_F} \quad (12)$$

is obtained. This has a direct negative impact on the ENC according to the formula

$$\text{ENC} = \frac{q_{\text{in}}}{V_{\text{ampl}}} \times V_{\text{CSArms}} \quad (13)$$

where V_{CSArms} is an rms noise voltage at the CSA output.

The just discussed approach reveals the influence of the ratio τ_F/τ_R on the CSA output amplitude and ENC values. However, when $\tau_F \rightarrow \tau_R$ (the input stage operates in a transimpedance mode), one should take more general approach. When the discriminant of the transmittance

function (2) denominator is positive, the roots are real and its inverse Laplace transform is expressed as

$$T(t) = T_0 \times \frac{e^{-\frac{a}{2}t} \sinh\left(\frac{\sqrt{a^2-4b}}{2}t\right)}{\frac{\sqrt{a^2-4b}}{2}} \quad (14)$$

where

$$\sinh(t) = \frac{e^t - e^{-t}}{2}. \quad (15)$$

This case gives a similar formula for the input amplifier pulse response as in (10) and can be considered as a unipolar pulse shaping. However, when the discriminant is negative, the roots are complex conjugated and the pulse response of (2) is expressed as

$$T(t) = T_0 \times \frac{e^{-\frac{a}{2}t} \sin\left(\frac{\sqrt{4b-a^2}}{2}t\right)}{\frac{\sqrt{4b-a^2}}{2}}. \quad (16)$$

Opposite to the pulse response from (14), this pulse response contains a sinusoidal term multiplied by an exponential one. This means that the pulse response has an oscillatory behavior. The CSA output pulse response shape can be controlled by the a and b coefficient values. When the CSA output pulse response has only one significant undershoot, it in approximation can be considered as a bipolar pulse shaping.

Having in mind the conclusions from the above paragraph and taking into consideration the transmittance function from (2) to have real poles, the following condition can be stated:

$$R_F C_F > 4 \frac{\zeta}{g_{m1} \times C_F}. \quad (17)$$

In the case, when $C_L \gg C_F$, condition (17) can be approximated as

$$R_F C_F > 4 \frac{(C_{DET} + C_{g1}) \times C_L}{g_{m1} \times C_F}. \quad (18)$$

To conclude the above consideration, the CSA output pulse shape, amplitude, and noise performance can be controlled by changing the ratio τ_F/τ_R . In the case of the fast signal processing circuit, the CSA feedback time constant τ_F is a small value, due to a small value of the R_F resistance. For instance, for the phase margin around 50°, the τ_R should be at least 3 times smaller than τ_F , which requires a larger value of the CSA input transistor M1 drain current. Thanks to the technology development, faster readout ASICs can be built. In general, the smaller feature technology size, the smaller value of the right side expression in (18) can be achieved as a result of the CSA core amplifier high-impedance output node capacitance C_L decrease (related with total transistor drain capacitance C_{dd}), while the transconductance g_{m1} and capacitance C_{g1} values are slightly dependent on the technology (when transistors operate in weak inversion region in deep submicrometer technologies). In addition, the higher the transistor transconductance g_{m1} value is needed, the higher the transistor current I_{DM1} is required. It allows to operate with a smaller value of the CSA feedback time constant τ_F and improves CSA speed performance at the same time.

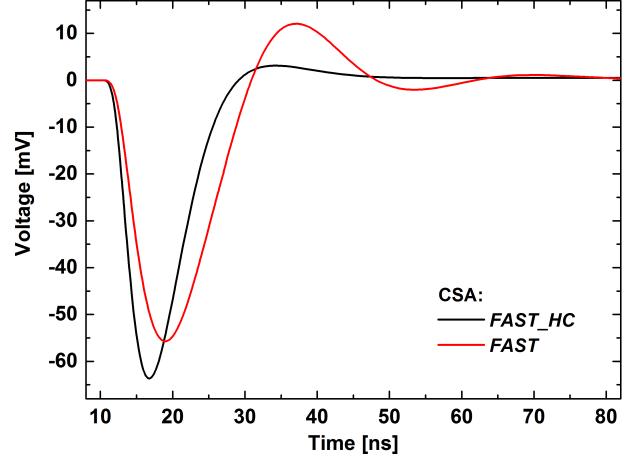


Fig. 8. CSA output waveforms for the CSA in the FAST_HC and FAST modes—post-layout simulations.

A. Post-Layout Simulations of Pulse Signal Processing Chain

Schematic simulations' results are consistent with the conclusions coming from the theoretical analysis discussed in the previous paragraphs. However, to be more consistent with the measurements, post-layout simulations are required, especially in the case of fast signal processing by the input stage. Capacitances used in the processing chain are of the order of several femtofarads. Thus, including parasitic capacitances existing in a layout structure is crucial, because they can affect the output waveform parameters.

Post-layout simulated CSA output waveforms for nominal input charge $q_{in} = 2200 e^-$ (corresponding to a photon energy of 8 keV impinging on a silicon detector with an average energy required to create electron-hole pair equals 3.6 eV) operating in two discussed modes [see (14) and (16)] are presented in Fig. 8. The CSA feedback time constants τ_F for both cases are nearly equal and $\tau_F \approx 4$ ns. However, there is a difference between the τ_R values for the FAST and the FAST_HC mode, which is related to the difference of the input transistor transconductance g_{m1} values. For the FAST mode, the input transistor drain current $I_{D1} = 20 \mu A$, which gives transconductance $g_{m1} = 0.38 \text{ mA/V}$, and for the FAST_HC mode, the input transistor drain current $I_{D1} = 60 \mu A$, which gives transconductance $g_{m1} = 0.84 \text{ mA/V}$. Higher current means lower τ_R value and higher power dissipation but lower noise. The simulated noise for the FAST and FAST_HC modes are, respectively, $ENC = 158$ and $104 e^- \text{ rms}$.

IV. MEASUREMENTS

The measurements results were performed with the IC bump bonded to a silicon pixel detector (see Fig. 9). The single-pixel detector size matched the readout channel pixel size— $100 \mu \text{m} \times 100 \mu \text{m}$. During the measurement, the $320\text{-}\mu\text{m}$ -thick detector was biased up to 150 V and holes were collected by the readout channels. To control measurement set-up dedicated software in LabView was written, which was responsible for the realization of the communication protocol and automatic data analysis. The 8-keV energy beam used

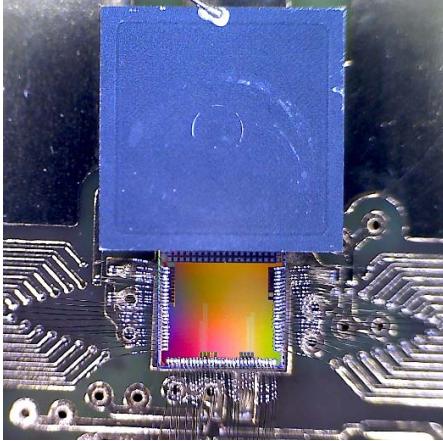


Fig. 9. Photograph of the prototype ASIC with attached detector.

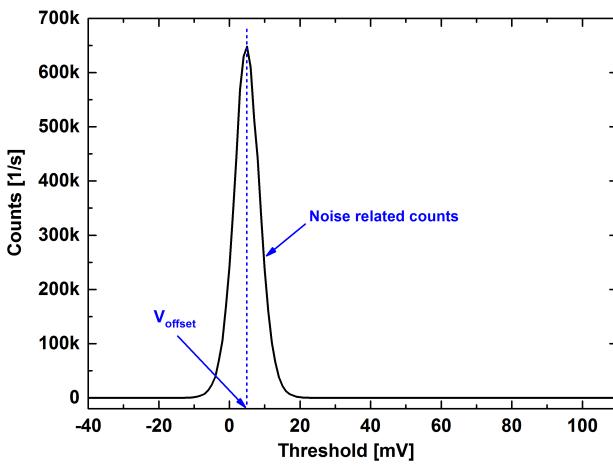


Fig. 10. Exemplary threshold scan for a single pixel with no input charge applied.

in the IC characterization process was provided by the 9-kW X-ray source. The photon's flux uniformly illuminated six rows of the IC pixel matrix.

The IC operated with nominal power supply voltages.

- 1) *Analog Part:* $V_{\text{ddm}} = 0.9$ V for the CSA input transistor branch and $V_{\text{dda}} = 1.2$ V for the rest of the analog circuitry.
- 2) *Digital Part:* $V_{\text{core}} = 1.2$ V for digital core and $V_{\text{LVDS}} = 1.8$ V for communication LVDS standard-based blocks.

Under nominal power supply voltages, the measured power consumption per single channel is about $45 \mu\text{W}$ for the FAST and $100 \mu\text{W}$ for the FAST_HC mode.

A. Pixel Matrix Measurement Methodology

In the case of a binary readout channel architecture, to determine the readout front-end electronics analog parameters, a number of so-called threshold scans are needed. The threshold scan contains information about the registered number of counts at the discriminator output within a given acquisition time in terms of threshold voltage applied globally to all

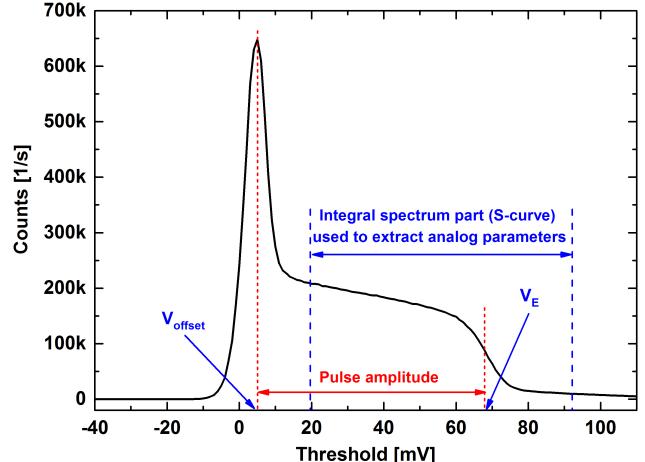


Fig. 11. Exemplary threshold scan for a single pixel for the detector illuminated with X-ray photons of a given energy.

channels. Fig. 10 presents an example of the threshold scan with no input charge applied. In this case, counts related to noise (which are also called as noise hits or noise counts) only around the discriminator input dc voltage are registered.

The noise count rate versus threshold voltage can be expressed by the Rice formula [28]. The horizontal coordinate of the noise count maximum value determines a discriminator input offset value (see Fig. 10). In the case of a system with white noise input, a first-order bandpass filter, and with offset equals zero, the noise count rate f_n at the discriminator output is expressed as

$$f_n(V_{\text{TH}}) = f_0 \exp\left(-\frac{V_{\text{TH}}^2}{2\sigma_n^2}\right) \quad (19)$$

where f_0 is the noise count maximum value for $V_{\text{TH}} = 0$, V_{TH} is the effective comparator threshold, σ_n is the comparator input rms noise voltage. In the case of the non-zero input offset voltage V_{offset} , (19) can be expressed as

$$f_n(V_{\text{TH}}) = f_{0F} \exp\left(-\frac{(V_{\text{TH}} - V_{\text{offset}})^2}{2\sigma_n^2}\right) \quad (20)$$

where f_{0F} is the noise count rate at $V_{\text{TH}} = V_{\text{offset}}$, which is used later for the offset correction and discussed in Section IV-B.

Fig. 11 presents an example of the threshold scan for the detector illuminated with X-ray photons of a given energy. The gain and input referred noise values can be extracted from a part of an integral spectrum (so-called "S-curve"). To calculate both the gain and input referred noise, the integral spectrum part is fitted to the modified error function [6]

$$f(V_{\text{TH}}) = \frac{a}{2} \left(1 - \text{erf}\left(\frac{V_{\text{TH}} - V_E}{\sqrt{2}\sigma}\right)\right) (bV_{\text{TH}} + c) \quad (21)$$

where V_E is the comparator threshold for a given X-ray energy, σ is the noise related to the pixel electronic noise and fluctuation of a signal for a given absorbed energy (usually $\sigma \approx \sigma_n$), a is the average number of input pulses of given energy, and $(bV_{\text{TH}} + c)$ is the linear term to model the charge sharing effect.

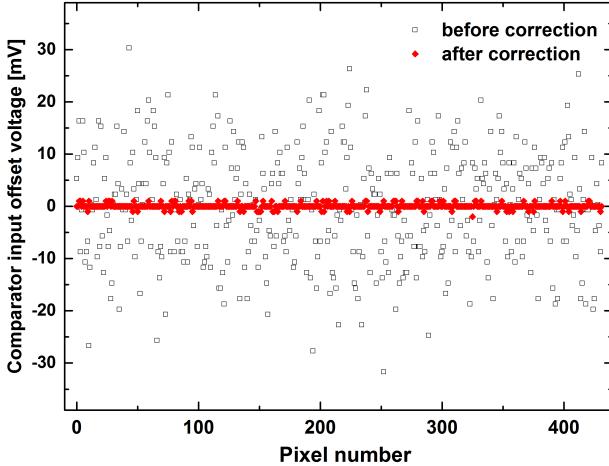


Fig. 12. Comparator offset voltage before and after correction versus pixel number.

B. Offset, Gain, and Noise Measurements

The first step of the IC characterization was an offset level correction. Based on the measured noise count rate data with no charge applied to the channel input, an offset voltage at the discriminator input in each channel can be extracted. Fig. 12 presents the measured dc offset at the discriminators' inputs before and after correction. The pixel-to-pixel offset spread of the whole IC pixel matrix before the correction was $\sigma = 10.6$ mV, and it was reduced to $\sigma = 0.5$ mV after loading proper digital values to trim DACs, which sets $I_{\text{TRIM}1}$ and $I_{\text{TRIM}2}$ currents in each channel independently (see Fig. 5). The comparator offset correction step is required, where one global threshold common to all pixels is applied.

Gain and noise measurements were performed using a monochromatic 8-keV X-ray source. Each of the CSA stages in the pixel matrix was set to the high-gain mode (effective CSA feedback capacitance $C_F = 2.4$ fF).

The pixels' analog parameters (charge gain k_q and noise ENC) were measured for three different I_{KRUM} current settings [which set the CSA discharge feedback structure effective resistance R_F (see Fig. 4): 1) $I_{\text{KRUM}} = 60$ nA (according to simulation $R_F \approx 2.9$ M Ω); 2) $I_{\text{KRUM}} = 140$ nA ($R_F \approx 1.3$ M Ω); and 3) $I_{\text{KRUM}} = 230$ nA ($R_F \approx 0.9$ M Ω), for both the FAST and the FAST_HC input stage operating modes.

The main parameter which influences the CSA output waveform is discharge feedback structure's effective resistance R_F . Histograms of the measured charge gain k_q in terms of the I_{KRUM} current for the FAST and FAST_HC modes are presented in Figs. 13 and 14, respectively (histograms based on 108 pixels uniformly illuminated by an X-ray beam).

Histograms of the measured noise ENC for the FAST and FAST_HC modes are shown in Figs. 15 and 16, respectively. Table II presents mean value (m. v.) and standard deviation (st. dev.) of charge gain k_q and noise ENC values corresponding to the data shown in Figs. 13–16.

Higher I_{KRUM} value gives a lower value of the CSA feedback resistance R_F , which implies charge gain k_q decrease and noise ENC increase for both operation modes. When the CSA operates with lower R_F value, the noise sources

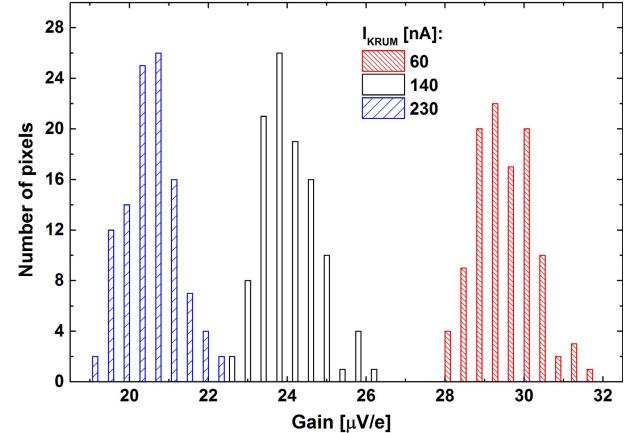


Fig. 13. Histograms of the measured charge gain k_q for the CSA in the FAST mode for three different I_{KRUM} current settings.

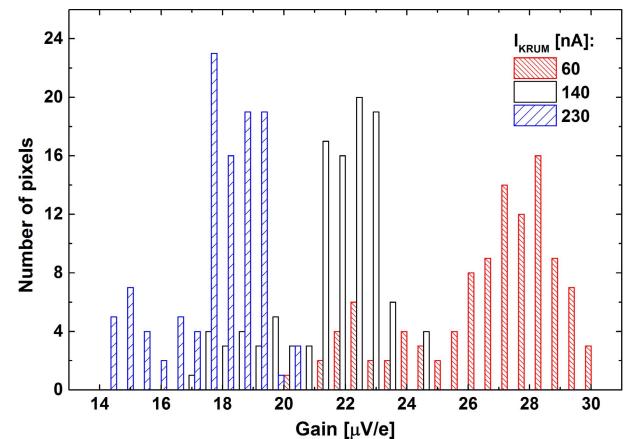


Fig. 14. Histograms of the measured charge gain k_q for the CSA in the FAST_HC mode for three different I_{KRUM} current settings.

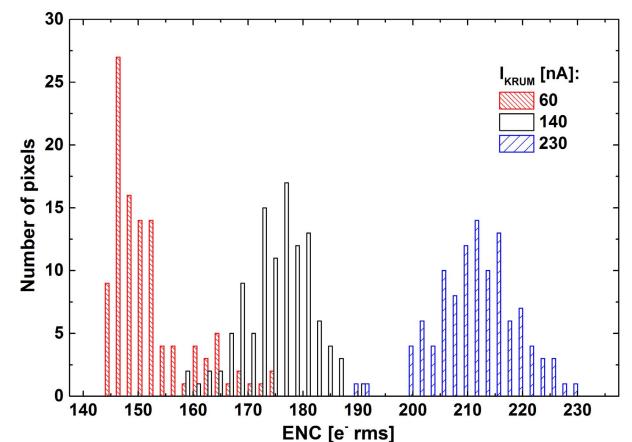


Fig. 15. Histograms of the measured noise ENC for the CSA in the FAST mode for three different I_{KRUM} current settings.

coming from the feedback discharge block dominates on noise performance.

For a given I_{KRUM} value, the FAST_HC mode provides lower ENC value than the FAST mode, which results from the higher value of the CSA input transistor transconductance g_{m1} .

TABLE II
PROTOTYPE ASIC MEASURED PERFORMANCE IN TERMS OF OPERATION MODE AND I_{KRUN} CURRENT

I_{KRUN} [nA]	FAST mode						FAST HC mode					
	Gain [$\mu\text{V/e^-}$]		ENC [$e^- \text{ rms}$]		10% dead time loss input rate [#] [Mcps]		Gain [$\mu\text{V/e^-}$]		ENC [$e^- \text{ rms}$]		10% dead time loss input rate [#] [Mcps]	
	m.v.	st. dev.	m.v.	st. dev.	m.v.	st. dev.	m.v.	st. dev.	m.v.	st. dev.	m.v.	st. dev.
60	29.5	0.75	153	7.0	6.44	0.59	26.7	2.39	147	7.7	6.22	0.52
140	24.0	0.72	176	6.0	9.79	1.15	21.6	1.65	158	6.3	10.42	1.27
230	20.4	0.67	212	7.2	12.24	1.46	17.7	1.46	185	7.0	12.16	1.41

m. v. – mean value ; st. dev. – standard deviation,

[#] calculated assuming $N_{\text{OUT}}/N_{\text{IN}} = 0.9$.

TABLE III
PROTOTYPE ASIC MEASURED PERFORMANCE FOR FAST_HC MODE FOR $I_{\text{KRUN}} = 140$ nA IN
TERMS OF THE EFFECTIVE CSA FEEDBACK CAPACITANCE C_F

C_F [fF]	Gain mode	Gain [$\mu\text{V/e^-}$]		ENC [$e^- \text{ rms}$]		10% dead time loss input rate [#] [Mcps]	
		m.v.	st. dev.	m.v.	st. dev.	m.v.	st. dev.
2.4	high	21.6	1.65	158	6.3	10.42	1.27
4.2	medium	15.4	1.06	169	7.6	8.47	0.94
6.6	low	10.8	0.71	190	10.4	6.53	0.49

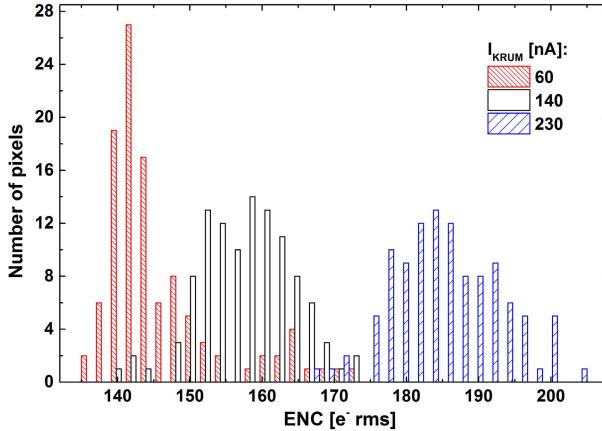


Fig. 16. Histograms of the measured noise ENC for the CSA in the FAST_HC mode for three different I_{KRUN} current settings.

In addition, the lower R_F value, the higher the difference between noise performances for both discussed operating modes. The presented readout front-end channel can provide lower values of the ENC at the cost of the R_F value increase. However, setting higher values of R_F is contrary to operating with high fluxes of incoming photons and it is out of the scope of this paper.

Table III presents mean value and standard deviation of charge gain k_q and noise ENC values for the CSA operating in the FAST_HC mode for $I_{\text{KRUN}} = 140$ nA (fixed CSA feedback resistance R_F) in terms of the effective CSA feedback capacitance C_F . The lower the capacitance C_F value, the higher the charge gain and lower noise ENC.

The analog parameters' standard deviation values from Tables II and III show the influence of variation of the effective CSA feedback resistance R_F , which has the most significant impact on the parameters' values variation.

C. High Count Rate Measurements

The high count rate measurements were performed using a monochromatic 8-keV X-ray source with the applied voltage of 45 kV and current changed within the range from 10 to 200 mA with 32 steps. Each photon absorbed by the detector generates a cloud of charge q_{in} , which as electrons and holes move toward the target detector electrodes spreads out. It may happen that the cloud shares across two (or more) neighboring pixels (charge sharing effect), which are seen as an output pulse amplitude loss in the target readout channel and as unwanted output pulse at the neighboring (or rest) readout channel. To avoid double counting of the same photon, the comparators' threshold was set at the half of the incoming photons energy (corresponding to the half of input charge q_{in}). In addition, to limit the number of noise counts in the readout system, the threshold should be set enough high compared to the noise level. In our worst case [the FAST mode for $I_{\text{KRUN}} = 230$ nA, where $\text{ENC} = 212$ e^- and $q_{\text{in}} = 2200$ e^- , (see Table II)], $V_{\text{TH}}/\sigma_n \approx 5$ in (19) gives noise counts in single readout channel at the negligible level. The higher the average pulses' rate, the higher probability that two or more consecutive output pulses overlap—so-called pile-up effect [6]. This influences the output pulse amplitude measurement accuracy and leads to the loss of counts. Based on the loss of counts, the system count rate performance can be characterized by the 10% dead-time loss input rate parameter. This parameter bases on the determination of the input pulse rate N_{IN} at which the output count rate $N_{\text{OUT}} = 0.9 \times N_{\text{IN}}$. The 10% dead-time loss input rate parameter can be expressed in a unit of photons/mm⁻² · s⁻¹ when it additionally includes information about the single readout pixel size.

Fig. 17 presents the family of curves of the measured count rate performance for the CSA operating in the FAST_HC mode and $I_{\text{KRUN}} = 230$ nA. It represents the count rate

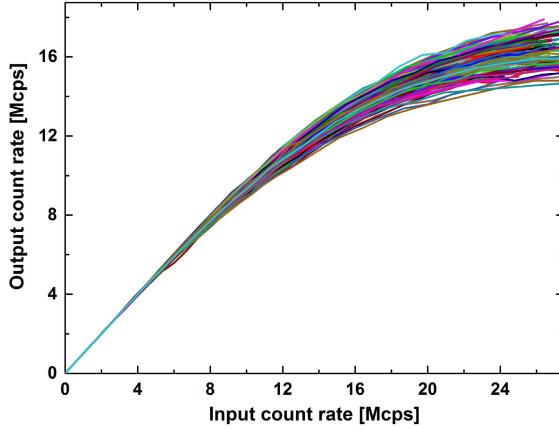


Fig. 17. Measured count rate performance for the CSA in the FAST_HC mode for $I_{\text{KRUM}} = 230$ nA.

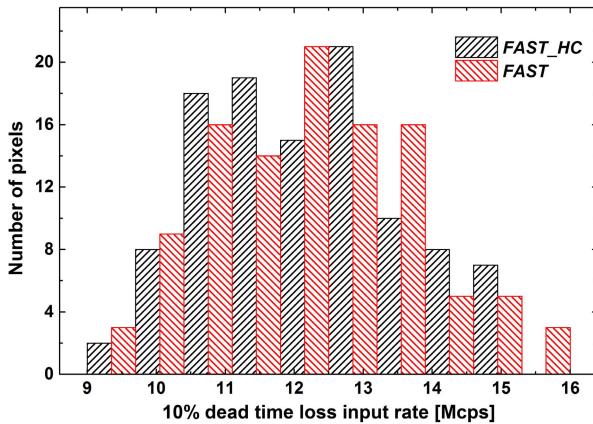


Fig. 18. Histogram of the measured 10% dead-time loss input rate for the CSA in the FAST and FAST_HC modes for $I_{\text{KRUM}} = 230$ nA.

performance of 108 pixels uniformly illuminated by X-ray beam in terms of input photons flux. The horizontal axis (input count rate) of this plot was scaled under the assumption that for the first six points (X-ray source current changed linearly from 10 to 20 mA) the count rate related losses are negligible.

Fig. 18 presents the histogram of measured 10% dead-time loss input rate performance for $I_{\text{KRUM}} = 230$ nA for the FAST and FAST_HC in high gain modes. For a given CSA operation mode, the higher the I_{KRUM} current (lower the CSA feedback resistance R_F value), the lower the CSA feedback discharge time constant τ_F , implies higher count rate performance (see 10% dead-time loss input rate parameter in Table II). In addition, for a given I_{KRUM} current, 10% dead-time loss input rate parameter's values are comparable for both operation modes.

Fig. 19 presents the averaged out from analyzed pixels count rate performance for the CSA in the FAST_HC mode for $I_{\text{KRUM}} = 140$ nA in terms of the effective CSA feedback capacitance C_F . The readout front-end electronics count rate performance decreases as the C_F is changed as 2.4, 4.2, and 6.6 fF (high, medium, and low gain mode, respectively), which is a result of the CSA feedback time constant τ_F change for the fixed CSA feedback resistance R_F (see Table III). The longer

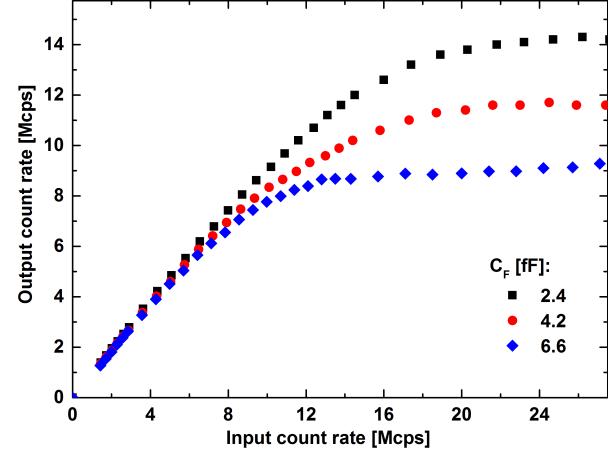


Fig. 19. Measured averaged out count rate performance for the CSA in the FAST_HC mode for $I_{\text{KRUM}} = 140$ nA in terms of the effective CSA feedback capacitance C_F .

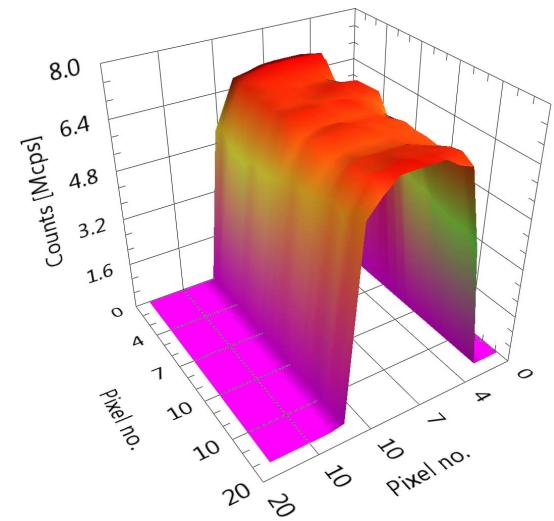


Fig. 20. Exemplary measured beam profile for the CSA in the FAST_HC mode for $I_{\text{KRUM}} = 230$ nA for a given X-ray tube current.

CSA feedback time constant τ_F , the longer time needs CSA output to come back to baseline, which directly impacts on its speed performance. In the case of operation in the lower gain mode (higher capacitance C_F value), it is possible to process input signal as fast as in the high gain mode. This can be done by increasing the I_{KRUM} current (decreasing resistance R_F value), however at the cost of noise ENC increase.

The example of the measured beam profile for the CSA in the FAST_HC mode for $I_{\text{KRUM}} = 230$ nA for a given X-ray tube current is presented in Fig. 20. The prototype system detecting active area is $1.8 \text{ mm} \times 1.8 \text{ mm}$ (18×18 pixels matrix). The SPC processing mode allows achieving a high dynamic range in numbers of counted impinging photons between neighboring/located in close proximity pixels by several orders of magnitude (depending on the beam profile).

To conclude, it is possible for the CSA in the FAST mode to operate as fast as in the FAST_HC mode, however at the price of higher noise ENC value. For a high count rate application,

TABLE IV
COMPARISON OF COUNTING CHIPS IN SUBMICROMETER CMOS TECHNOLOGIES

Chip [ref]	Medipix 3RX [19, 29]	PXD18k [29]	Eiger [12]	UFXC32k [31]	This work – PXF40	
					FAST_HC	FAST
Process	130 nm	180 nm	250 nm	130 nm	40 nm	
Pixel size [μm^2]	55 × 55	100 × 100	75 × 75	75 × 75	100 × 100	
Power/pix. [μW]	9	23	–	26	100	45
ENC [$e^- \text{ rms}$]	80	168	175	235	185	212
10% dead time loss input rate ^a [cps/mm ²]	0.87×10^8	0.61×10^8	1.46×10^8	2.20×10^8	1.216×10^9	1.224×10^9

^a static PWR consumption for minimum dead time τ_p of the front-end electronics .

calculated using minimum dead time and assuming $N_{\text{OUT}}/N_{\text{IN}} = 0.9$ according to the formula: $N_{\text{OUT}} = N_{\text{IN}} \cdot \exp(-N_{\text{IN}} \cdot \tau_p)$.

it is better to process input charges q_{in} in a bipolar shaping way (in our case the FAST mode) than in a unipolar shaping way (FAST_HC mode). The bipolar shaping reduces (or in ideal case eliminates) input pulses rate dependent baseline shift better than unipolar shaping. However, the readout channel output amplitude reduction implies noise degradation [6].

The presented readout front-end electronics' 10% dead times loss input rate reach up to 1.22 Gcps/mm², which according to the authors' knowledge is the fastest SPC solution for pixel detectors. These parameters' values were calculated based on the pixel size 100 $\mu\text{m} \times 100 \mu\text{m}$ (including blocks for inter-pixel communication). Having in mind that a single pixel with blocks needed for only fast signal processing would occupy the silicon area of 50 $\mu\text{m} \times 50 \mu\text{m}$, it additionally would increase by a factor of 4 the value of the 10% dead-time loss input rate parameter per area.

V. CONCLUSION

In this paper, we presented a prototype pixel readout IC implemented in CMOS 40-nm technology operating in an SPC mode for hybrid semiconductor detectors for low-energy X-ray imaging systems. The authors analyzed the CSA transmittance function pole locations and their influence on its output waveforms, which implies count rate performance, and chose deep submicrometer 40-nm CMOS technology to achieve possible short CSA output pulse, which is the key to improve the readout front-end electronics speed performance. The overall performance of the ASIC in comparison with that of other designs is summarized in Table IV. The main advantages of the presented solution are high count rate performance with an acceptable noise level and power consumption at the same time, which can make it a preferable solution for an application using high-intensity X-ray radiation. The high count rate measurements show that the described readout front-end electronics is, according to the authors' knowledge, currently the fastest SPC-based solution. The presented readout front-end electronics' 10% dead-time loss input rate parameter breaks the limit of 1 Gcps/mm². The presented parameter's values were calculated based on the pixel size 100 $\mu\text{m} \times 100 \mu\text{m}$ (including blocks for inter-pixel communication). Our future plan is to design next version of the proposed solution with the functionality of selection of photons within a given energy window occupying the silicon area of 50 $\mu\text{m} \times 50 \mu\text{m}$, which would additionally increase the value of the 10% dead-time loss input rate parameter.

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