Low-Jitter Multi-Output All-Digital Clock Generator Using DTC-Based Open Loop Fractional Dividers

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***Abstract*— An all-digital reconfigurable multi-output clock generator is presented. A digital phase-locked loop provides a high-frequency clock to multiple independent open loop $\Delta\Sigma$ fractional dividers (FDIVs). A high resolution digital-to-time converter (DTC) whose range is calibrated in background is used to achieve low-jitter performance that is insensitive to process, voltage, and temperature variations. The proposed open loop FDIV operates over a wide frequency range of 20 MHz–1 GHz, and has programmable spread spectrum modulation and instantaneous frequency switching capabilities. Fabricated in a 65-nm process, the prototype FDIV occupies an active area of 0.017 mm^2. At 1-GHz output frequency, it consumes 3.2 mW from 0.9-V supply and achieves a worst case integrated jitter of 1.44 ps_{rms}.**

***Index Terms*— Digitally controlled delay line (DCDL), delay line, digital phase-locked loop (PLL), digital-to-time converter (DTC), dynamic voltage and frequency scaling (DVFS), dynamic frequency scaling (DFS), electromagnetic interference (EMI) reduction, fractional divider (FDIV), fractional-N, frequency switching, frequency synthesizer, spread spectrum clock generator (SSCG), wide bandwidth (BW).**

I. Introduction

ADVANCED system-on-chips (SoCs) perform many diverse analog, digital, mixed-signal, and radio frequency functions. An SoC typically includes a wide variety of modules such as multicore processors, memories, I/O interfaces, power management, and wireless transceivers [1]. Each of these modules operates in their own dedicated clock domain that is optimized for the desired performance. For example, I/O interfaces require low-jitter high-frequency clocks, while a processor may require spread spectrum clocking (SSC) to reduce electromagnetic interference (EMI) [2] or fast frequency switching to support power saving techniques such as dynamic frequency scaling (DFS) [3], [4]. Modern multicore processors also require dynamically adjustable per core clock generator that needs to provide fast frequency switching with no frequency overshoot and tight settling time, power, and area constraints [5], [6]. To meet these diverse requirements, SoC clock generators are typically implemented as the fractional-N phase-locked loops (FNPLLs) [7]. But, PLL bandwidth (BW) limits the minimum achievable settling time during frequency switching, and limits the amount of EMI reduction [8]. Two-point modulation technique with calibrated modulation paths can overcome the BW limitation [9], [10]. However, the very slow settling time of the calibration limits its usage in the dynamically adjustable SoC clock generators. Alternatively, open loop modulation based on multi-phase switching or digital delay lines can achieve excellent EMI reduction and precise modulation depth [2], [11], but they suffer from the large deterministic jitter (DJ).

In view of these drawbacks, we propose a reconfigurable all-digital clock generator using open loop fractional dividers (FDIVs) [12]. Using a low-jitter high-frequency clock provided by a digital PLL, multiple independent output clocks are generated within a frequency range of 20–1000 MHz. The open loop architecture overcomes the BW limitation of FNPLLs and achieves nearly unlimited spread spectrum modulation and instantaneous frequency switching without any frequency overshoot. The proposed background calibrated $\Delta\Sigma$ quantization error cancellation scheme implemented using a high resolution digital-to-time converter (DTC) helps to achieve excellent jitter performance.

Rest of this paper is organized as follows. A brief overview of fractional-N frequency synthesis and modulation techniques is presented in Section II. Architectural design details of the proposed open loop FDIV are presented in Section III, while Section IV provides circuit design details including comprehensive linearity analysis of the DTC. Measured results from the test chip are shown in Section V and key contributions of this paper are summarized in Section VI.

II. Fractional-N Modulation Techniques

A. Closed Loop: Fractional-N PLLs

Block diagram of a conventional digital FNPLL is shown in Fig. 1(a). Fractional-N operation is achieved by dithering the feedback divider using a $\Delta\Sigma$ modulator. A time-to-digital converter (TDC) detects the phase error between reference and dithered feedback clocks [13]. The TDC output is filtered by a digital loop filter and used to control the frequency of a digitally controlled oscillator (DCO). The jitter performance is dictated by the PLL BW and optimizing it under conflicting

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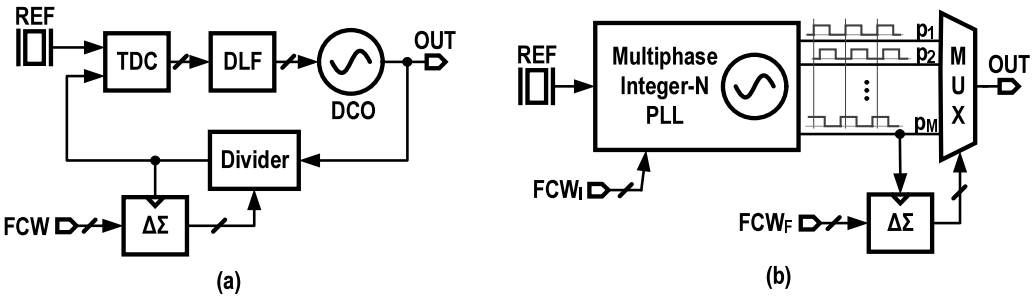

Fig. 1. Block diagram of conventional fractional-N synthesizers using (a) $\Delta\Sigma$ digital FNPLL and (b) $\Delta\Sigma$-based phase switching.

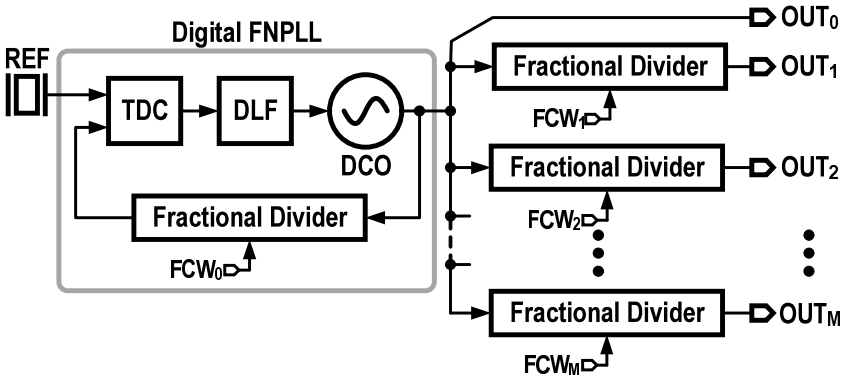

Fig. 2. Block diagram of the proposed multi-output all-digital clock generation unit using open loop FDIVs.

requirements is a challenge. A narrow PLL BW helps to low-pass filter the shaped quantization noise, but this comes at the expense of the limited modulation BW, slow settling time, and inadequate filtering of the oscillator phase noise. Quantization noise cancellation (QNC) techniques [13]–[15] can help to overcome this tradeoff, thereby achieving excellent jitter performance. Two-point modulation techniques can further extend modulation BW [16], but they are susceptible to mismatch between the two modulation paths. Background gain calibration [9], [10] can be used to correct path mismatches across process, voltage, and temperature (PVT) variations, but very slow convergence of the calibration makes this approach unsuitable for SoC clock generators where the output frequency and modulation parameters have to be switched dynamically.

B. Open Loop: Multi-Phase Switching

Open loop frequency synthesis based on the phase switching was proposed to mitigate the modulation BW limitation of FNPLLs [17]–[20]. Fractional-N synthesis was performed by rotating M equally spaced clock signals, $[p_1, p_2, \ldots, p_M]$, all of which have the same frequency and phase separation of $2\pi/M$ [rad] between adjacent signals [see Fig. 1(b)]. These clock phases are typically generated using either ring oscillators embedded in integer-N PLLs [17] or standard quadrature generation techniques [20]. A digital phase accumulator integrates fractional frequency control word, $\mathrm{FCW_F}$, and generates control sequence of the phase multiplexor. For example, when $M = 16$ and the fractional part ($\alpha_{FR} = 1/16$) the phase multiplexor is controlled according to the following periodic sequence: $[p_1, p_2, \ldots p_M, p_1, \ldots]$, resulting in an output period equal to $T_O \cdot (1 + \alpha_{FR})$. Because the output frequency resolution is governed by minimum phase separation, phase interpolators are sometimes used to improve resolution [18], [21], [22]. Finer frequency resolution can be achieved by using a digital $\Delta\Sigma$ modulator to drive the phase accumulator [18], [20]. In [21], a QNC technique is proposed by directly modulating the voltage controlled oscillator (VCO) of the multi-phase clock generator to cancel the shaped quantization error. Consequently, open loop modulation and low phase noise performance were achieved simultaneously. However, it requires relatively accurate knowledge of the VCO gain, K_{VCO}, for perfect QNC, which makes it sensitive to PVT variations. Besides, this approach cannot provide multiple independent outputs, as the multi-phase clock generator cannot be shared. The non-linearity of the digital-to-phase conversion degrades spurious and phase noise performance. VCO delay cells and the routing paths have to be precisely matched to minimize the performance degradation [23]. Finally, the need to drive multiple high-frequency clocks may significantly increase the power consumption of this approach. In view of the aforementioned drawbacks of existing open loop modulators, we propose an open loop FDIV architecture that can achieve low-jitter and fine resolution.

III. Proposed Clock Generator

The proposed clock generator is shown in Fig. 2. It is composed of a digital FNPLL that generates low-jitter high-frequency (~5 GHz) output clock, $\mathrm{OUT_0}$, from a 50-MHz reference clock and open loop FDIVs that generate multi-

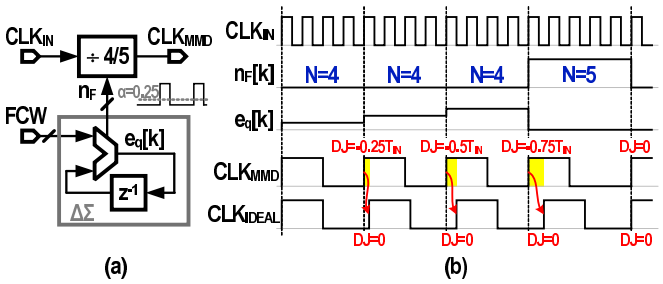

Fig. 3. (a) Block and (b) timing diagrams of a $\Delta\Sigma$ FDIV.

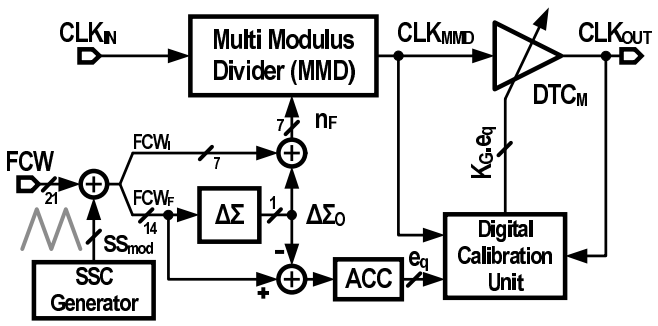

Fig. 4. Simplified block diagram of the stand-alone open loop $\Delta\Sigma$ FDIV.

ple independent output clocks, $\mathrm{OUT_m}$, $m = 1, 2, \ldots, M$. This paper focuses on the design and implementation of the open loop FDIV, while FNPLL design details can be found in [24]. Each mth FDIV is controlled by a dedicated frequency control word, $\mathrm{FCW_m}$, such that its output frequency, F_m is equal to

$$F_\mathrm{m} = \frac{F_0}{N_\mathrm{m} + \alpha_\mathrm{m}} \tag{1}$$

where N_m and α_m are the integer and fractional division ratios, respectively. Such an FDIV can be implemented using the so-called $\Delta\Sigma$-FDIV architecture, where the divider modulus is dithered by a $\Delta\Sigma$ modulator [25]. Because the proposed FDIV is based on this architecture, it is instructive to first review the behavior of $\Delta\Sigma$-FDIV. To this end, consider a simple dual-modulus divider whose division ratio (4/5 in this example) is controlled by a first-order $\Delta\Sigma$ modulator. A division ratio of 4.25 ($N = 4$ and $\alpha = 0.25$) is realized by dividing the input by 4 for three cycles and by 5 for one cycle in a repetitive manner, as shown in Fig. 3. Comparing output clock, $\mathrm{CLK_{MMD}}$ to the ideal clock, $\mathrm{CLK_{IDEAL}}$ reveals that DJ in the amount of $0.25T_\mathrm{IN}$ is added in the first cycle, which accumulates to $0.75T_\mathrm{IN}$ by the third cycle. In the fourth cycle, output clock aligns with the ideal clock (DJ $= 0$) and this DJ pattern repeats every four cycles. This DJ behavior is a direct result of truncating FCW and can be expressed in terms of $\Delta\Sigma$ truncation error, e_q, as

$$\mathrm{DJ}[k] = -e_\mathrm{q}[k] \cdot T_\mathrm{IN}. \tag{2}$$

Because DJ can be nearly as large as T_IN, which is prohibitive in many applications, it must be suppressed. When FDIV is embedded in the feedback path of an FNPLL, $\Delta\Sigma$ quantization error is filtered by PLL's low-pass transfer function. For a stand-alone open loop FDIV, the quantization error can only be canceled in time-domain [18].

A simplified block diagram of the proposed open loop FDIV is shown in Fig. 4. It consists of a multi-modulus divider (MMD) followed by a DTC that performs QNC. The input FCW is composed of 7-bit integer and 14-bit fractional frequency control words denoted as $\mathrm{FCW_I}$ and $\mathrm{FCW_F}$, respectively. $\mathrm{FCW_I}$ controls the integer division ratio (N) from 4 to 127, while $\mathrm{FCW_F}$ controls the fractional part α, resulting in a division ratio of $N + \alpha$. As shown in Fig. 4, $\mathrm{FCW_F}$ is truncated to 1 bit using a first-order $\Delta\Sigma$ modulator and added to $\mathrm{FCW_I}$. The $\Delta\Sigma$ modulator output, $\Delta\Sigma_\mathrm{O}$, is added to $\mathrm{FCW_I}$ to control an extended range MMD [24], which seamlessly switches the divider between two consecutive integer values to produce the desired output fractional frequency, $F_\mathrm{IN}/(N+\alpha)$. However, as described earlier, truncation error, e_q, introduced by the $\Delta\Sigma$ modulator directly appears as DJ in the output clock. Noting that instantaneous quantization error, e_q, causes an output DJ of $e_\mathrm{q} \times T_\mathrm{IN}$, we propose to cancel it by adding an equal and opposite amount of phase shift to the divider output. To this end, a DTC ($\mathrm{DTC_M}$), whose gain is calibrated to be T_IN is used. The timing diagram in Fig. 3 shows the added phase shift by the DTC, where output clock matches the ideal clock and DJ is completely canceled. In contrast to phase interpolator-based QNC [18], DTC-based QNC offers better linearity and lower power consumption. But to perfectly cancel the $\Delta\Sigma$ quantization noise, the DTC gain has to be calibrated to match the input clock period, T_IN, using a digital calibration unit. The DTC gain is calibrated by digitally scaling its input e_q by a calibration factor K_G. The details of proposed calibration are described next. In the context of FNPLLs, the feedback FDIV clock (FB) will be phase-locked to the reference clock (REF), and an accurate DTC-based QNC scheme can be realized as in [14] and [15]. The TDC output (ERR) simply detects the residual quantization noise, and a least mean square (LMS) correlation technique can precisely set the calibration factor K_G. These techniques cannot be applied in the proposed stand-alone open loop FDIV, as we cannot detect the residual quantization noise. In view of this bottleneck, we propose a new accurate QNC calibration scheme that does not require a reference clock. The details of proposed calibration are described next.

A. Background DTC Gain Calibration

The basic concept of proposed digital calibration technique is shown in Fig. 5. It is based on a digital delay-locked loop (DLL) and does not require any external reference clock. D-flip-flop, $\mathrm{DFF_S}$, synchronizes MMD output with the input clock, $\mathrm{CLK_{IN}}$ while a second flip-flop, $\mathrm{DFF_R}$, which is matched to $\mathrm{DFF_S}$ delays the synchronized clock by one input clock cycle, T_IN. Consequently, the time difference between the two flip-flop outputs, $\mathrm{CLK_S}$ and $\mathrm{CLK_R}$, equals one input clock period, T_IN, as illustrated in the timing diagram in Fig. 5. A simple digital DLL consisting of a bang-bang phase detector (BBPD) and a digital calibration filter locks $\mathrm{CLK_S}$ and $\mathrm{CLK_R}$, thereby setting the DTC, $\mathrm{DTC_M}$, delay range to T_IN. Under this condition, digital filter output rep-

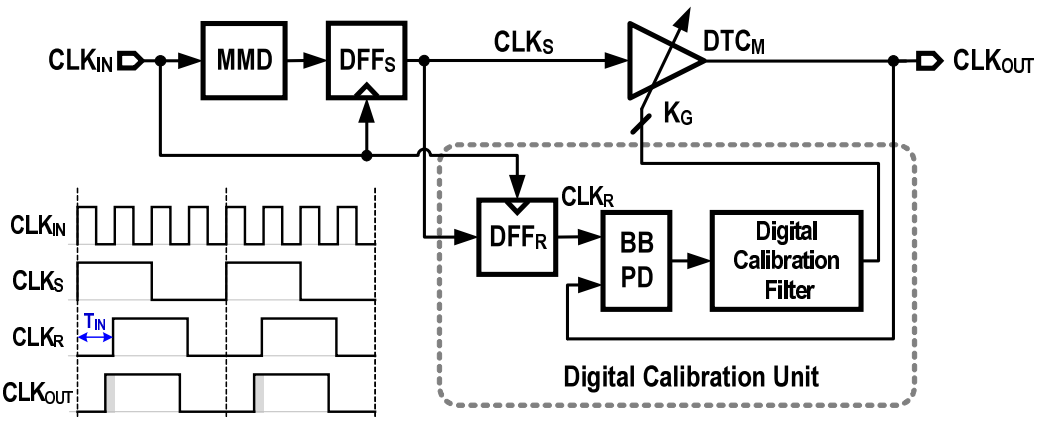

Fig. 5. Block and timing diagrams of the open loop FDIV with foreground calibration of DTC gain.

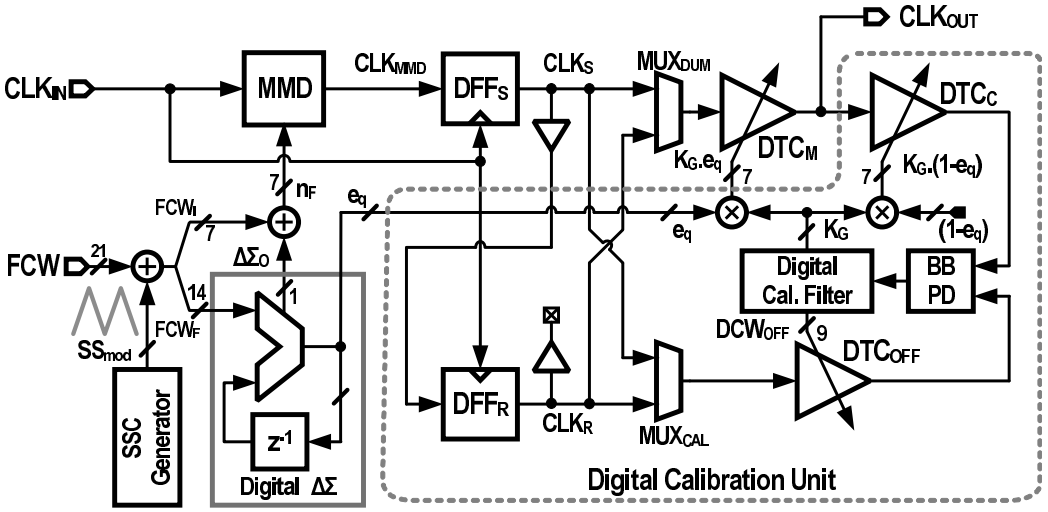

Fig. 6. Detailed block diagram of the proposed open loop FDIV with background calibration of DTC gain.

resents the DTC range and can be used as the gain calibration factor K_G to scale the $\Delta\Sigma$ error signal e_q (see Fig. 4). However, this way of calibrating the DTC gain in a foreground manner is susceptible to supply and temperature variations and can result in severely degraded performance across different operating conditions.

To mitigate this, calibration is performed in background by placing a complementary delay line, DTC_C, in the DLL feedback path, as shown in Fig. 6. The main delay line, DTC_M, is controlled by delay control word, $DCW_M = K_G \cdot e_q$, while the complementary delay line, DTC_C, is controlled by $DCW_C = K_G \cdot (1\text{-}e_q)$. In steady state, DLL establishes the sum of DTC_M and DTC_C delays to be equal to T_{IN} as shown as follows:

$$e_q \cdot K_G \cdot T_{DTC,M} + (1\text{-}e_q) \cdot K_G \cdot T_{DTC,C} = T_{IN} \tag{3}$$

where $T_{DTC,M}$ and $T_{DTC,C}$ represent full-scale delays of DTC_M and DTC_C, respectively. The sensitivity of gain calibration factor K_G to PVT is greatly reduced by matching the two DTCs ($T_{DTC,M} = T_{DTC,C}$), resulting in

$$K_G \cdot T_{DTC,M} = T_{IN}. \tag{4}$$

Note that, in any practical DTC, zero-input code produces nonzero minimum DTC delay, T_O, which appears as an offset and degrades the calibration accuracy. To overcome this, an equal delay is introduced in the reference time path using an offset delay line, DTC_{OFF}, which cancels T_O delay of DTC_M and DTC_C. Initial offset calibration step is done, by bypassing DFF_R using a multiplexor, MUX_{CAL}, and setting $K_G = 0$ so that the inputs to the main and complementary DTCs are zero. After the DLL is locked, DTC_{OFF} delay will match the offset delays of the DTC_M and DTC_C in addition to any input-referred BBPD offset. This offset delay control word, DCW_{OFF}, is held and used in normal operation. Fig. 7 shows the behavioral time-domain simulation results of the proposed FDIV for $\alpha = 2^{-14}$, where K_G settles in less than 1 μs, and jitter reduces to less than 1 ps_{rms}.

As the current drawn from the DTC_M depends on its input code DCW_M, adding the complementary DTC_C makes total current drawn by DTC independent of the input code DCW_M. This is crucial in achieving high linearity and minimizing supply induced DJ. While background digital calibration ensures minimal DTC gain variation across PVT, the overall jitter performance will then be greatly impacted by the integral

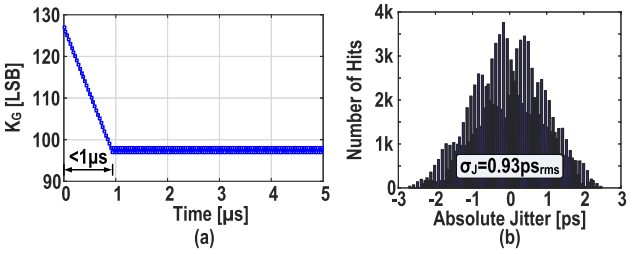

Fig. 7. Time-domain behavioral simulation results. (a) Calibration settling and (b) jitter histogram after calibration.

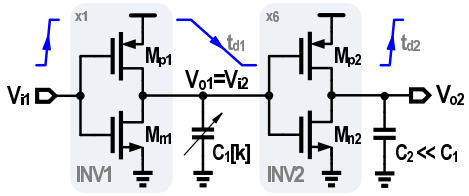

Fig. 8. Schematic of a single-stage DTC.

non-linearity (INL) of the DTC, which manifests at the output as fractional spurs and DJ. Therefore, it is crucial to design highly linear DTCs. In Section IV, we analyze delay generation process of the DTC to understand the main factors that impact its linearity performance.

IV. DTC Design and Linearity Analysis

DTC limits FDIV jitter performance in multiple ways. First, DTC adds phase jitter, which scales in inverse proportion to power consumption [26]. The jitter-power product of DTCs was shown to scale linearly with the full-scale delay range in current-mode logic-based implementations, and quadratically in CMOS implementations [27]. In view of this tradeoff, we chose a relatively high-frequency (∼5 GHz) input clock to limit the required DTC range to 200 ps. Second, DTC quantization error appears as output jitter. Increasing the number of DTC bits increases the input operand width of digital multiplier and degrades power efficiency. So DTC resolution is limited to 7 bit (∼2 ps) to satisfy the timing requirements of the 7×7 digital multiplier running at 1-GHz output clock. Finally, but more importantly, DTC INL limits the overall jitter and spurious performance. Despite its importance, DTC linearity is not well studied in the literature so far. Our goal in this section is to analyze the delay generation process of DTCs using accurate analytical models.

A. DTC Linearity Analysis

A DTC can be implemented using a cascade of two CMOS inverters as shown in Fig. 8, where first inverter, INV1, is loaded with a digitally programmable capacitor bank to act as a linearly programmable delay element. The second inverter, INV2, acts as a voltage comparator. For N_{DTC}-bit DTC, the input digital control word, k, can take any value from 0 to full-scale, $k_{\mathrm{fs}} = 2^{\mathrm{N_{DTC}}} - 1$. The total delay of the DTC, $t_{\mathrm{d}}[k]$, for a control word, k, is the sum of the delay of two inverters $t_{\mathrm{d1}}[k]$ and $t_{\mathrm{d2}}[k]$. INL of the DTC can calculated from the total delay expression using

$$\mathrm{INL}[k] = (t_{\mathrm{d}}[k] - t_{\mathrm{d}}[0]) - \frac{k}{k_{\mathrm{fs}}}(t_{\mathrm{d}}[k_{\mathrm{fs}}] - t_{\mathrm{d}}[0]) \tag{5}$$

where k_{fs} is the full-scale input code word.

Assuming a step input, first-order analysis of inverter delay [28], can be used to estimate INV1 delay $t_{\mathrm{d1}}[k]$. α-power law MOS model [29], [30] is used to account for the impact of velocity saturation. As shown in the Appendix by (9), $t_{\mathrm{d1}}[k]$ is directly proportional to its load capacitance $t_{\mathrm{d1}} \propto C_1[k] = C_{\mathrm{o}} + k\,C_{\mathrm{u}}$, where C_{o} is the total load capacitance when all the $2^{\mathrm{N_{DTC}}} - 1$ switched capacitors are OFF and $k\,C_{\mathrm{u}}$ is extra capacitance when k unit capacitor cells are switched ON.

There are three main contributors to DTC static non-linearity. First, random mismatch between the unit cells in the capacitor bank introduces non-linearity. For a standard binary weighted capacitor bank, k is represented by binary-coded digital control word, $\mathrm{dcw_i}$, as

$$k = \sum_{i=0}^{N_{\mathrm{DTC}}-1} 2^i \cdot \mathrm{dcw_i} \tag{6}$$

$C_1[k]$ expression is modified to account for random mismatches between the unit cells as follows:

$$C_1[k] = C_o + \sum_{i=0}^{N_{\mathrm{DTC}}-1} 2^i \cdot \mathrm{dcw_i} \cdot C_{\mathrm{u}}[k]. \tag{7}$$

The expected worst case $\mathrm{INL_{pk}}$ occurs at mid-code transition. Increasing the unit cell size helps to minimize the resulting INL. To ensure $\mathrm{INL_{pk}} < (1/2)$ LSB for a 3σ yield, the relative standard deviation of the unit capacitor ($\sigma_{\mathrm{C}}/C_{\mathrm{u}}$) must satisfy

$$\frac{\sigma_{\mathrm{C}}}{C_{\mathrm{u}}} \leq \frac{0.5}{3\sqrt{2^{N_{\mathrm{DTC}}} - 1}}. \tag{8}$$

To obtain 8-bit accuracy, a 1% $\sigma_{\mathrm{C}}/C_{\mathrm{u}}$ is necessary, which sets the minimum size for C_{u}. Second, C_1 non-linearity from the capacitor bank and INV2 input capacitance will cause $t_{\mathrm{d1}}[k]$ to change non-linearly with the load capacitance. Finally, changing C_1 will also change the delay of the second inverter, $t_{\mathrm{d2}}[k]$ non-linearly [31], [32] because of the strong dependence of $t_{\mathrm{d2}}[k]$ on the slow rise/fall times of INV1 output. This behavior becomes the dominant factor as the required DTC delay range increases.

The above-mentioned first-order analysis is accurate only if the input rise/fall times are small and it also does not account for short circuit current. As a result, it cannot be used to accurately describe $t_{\mathrm{d2}}[k]$. So we derived analytical expression of the inverter output waveform directly by solving the differential equations that describe temporal evolution of INV2 output [30] (see the Appendix). Input waveform v_{i2} for INV2 is approximated by a falling ramp with a slope of $-1/\tau_{\mathrm{F}} \approx d\,v_{\mathrm{o1}}/dt = -1/2t_{\mathrm{d1}}$. Ignoring short circuit current flowing through M_{n2}, INV2 delay, $t_{\mathrm{d2}}[k]$, has a non-linear dependence on the fall time $\tau_{\mathrm{F}}^{(\alpha_{\mathrm{p2}}/(\alpha_{\mathrm{p2}}+1))}$ as shown by (12) in the Appendix. This directly leads to detrimental impact on the DTC INL.

A 65-nm CMOS process technology is used to assess the accuracy of the analysis. Transistor widths have been selected

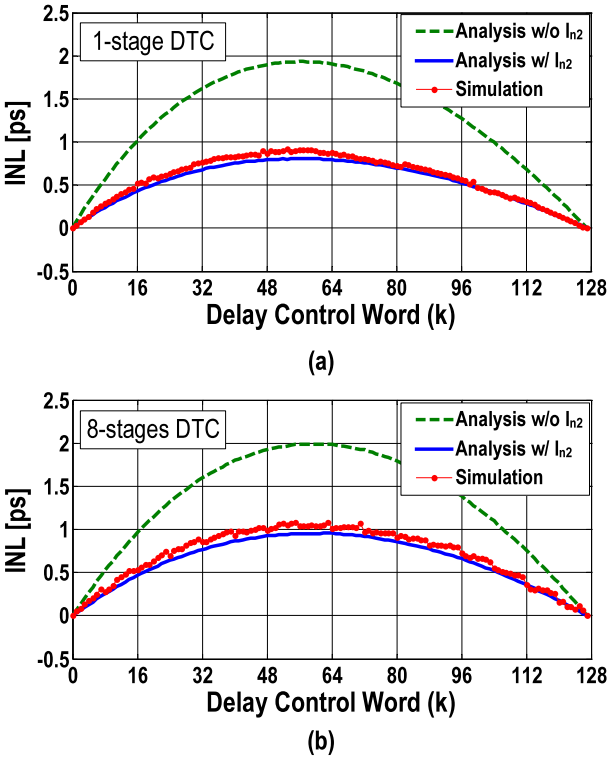

Fig. 9. Linearity analysis and simulation results for (a) single-stage DTC and (b) eight-stage DTC.

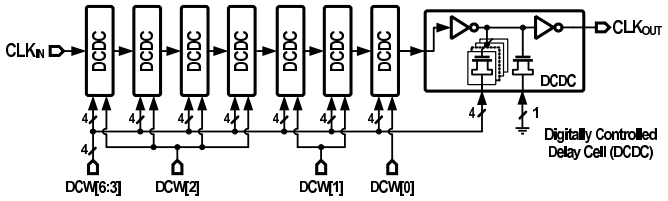

Fig. 10. Block diagram of the eight-stage DTC.

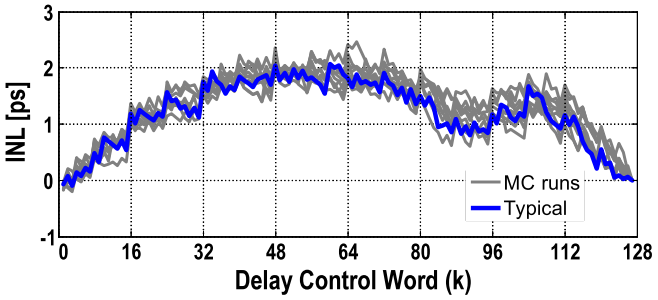

Fig. 11. Post-layout Monte-Carlo simulations for the DTC INL.

to achieve equal drain currents $I_{\mathrm{Don}} = I_{\mathrm{Dop}}$ at $V_{\mathrm{GS}} = V_{\mathrm{DS}} = V_{\mathrm{DD}}$. The size of INV2 is six times bigger than INV1, to achieve fast rise time at DTC output. Transistors parameters are extracted using the method described in [29], where $\alpha_{\mathrm{n1,2}} \approx \alpha_{\mathrm{p1,2}} \approx 1.5$ and $n_{1,2} \approx p_{1,2} \approx 0.32$. A 7-bit capacitor bank (i.e., $k_{\mathrm{fs}} = 127$) is used with unit cell $C_{\mathrm{u}} = 2.8$ fF and OFF capacitance $C_{\mathrm{o}} = 220$ fF. A supply voltage of 1 V and $C_2 = 25$ fF is used. The effective resolution of DTC is about 2 ps. The calculated INV1 and INV2 delays match closely with transistor-level (BSIM4 models) transient simulations. Fig. 9(a) shows our analysis captures the shape of the INL but it deviates from the simulated INL. This discrepancy is mainly caused by the short circuit current flowing through M_{n2}. As M_{n2} operates in linear region, its current, I_{n2}, can be approximated by a linear function similar to [30]. Using the normalized output voltage expression, v_{o2}, in (21), the total delay and the INL of the DTC can be calculated. As shown in Fig. 9(a), the calculated INL results from the revised analysis, which accounts for I_{n2}, closely matches transistor-level transient simulations.

B. Multistage DTC Design

The required DTC incremental delay range (~256 ps) can be realized using a single delay stage in principle. However, the unit capacitor cell has a maximum ratio between its ON and OFF capacitance, which considerably increases the offset delay of the DTC, T_{O} as the incremental delay range increases. This may increase the total DTC delay to more than 500 ps. The input clock period to the DTC can be as small as 1 ns with a small pulsewidth of 250 ps (much smaller than DTC total delay). This means in practice, a single-stage DTC cannot realize the required incremental delay range, because the slow edge rates would swallow the pulse generated at the DTC output. This mandates segmentation by cascading multiple DTCs [33]. As shown by previous linearity analysis, the inverter delay is a strong non-linear function of its input rise/fall time. We propose a scalable segmentation technique (see Fig. 10), which can decouple the achieved incremental delay from input clock pulsewidth.

The segmentation control distributes the desired delay equally among all the delays cells. Each delay cell consists of a CMOS inverter loaded with a tunable 16-unit capacitor bank. The 4 MSBs of DCW control 15 capacitors in all the delay cells, while each of the 3 LSBs control one unit capacitor in different delay cells, as shown in Fig. 10. This ensures a maximum load capacitance deviation of at most one unit capacitor over the entire range of the DCW. This segmentation scheme helps to maintain almost the same rise/fall time among all the stages, which improves the DTC INL. The presented linearity analysis of single-stage DTC can be easily extended to multistage DTC. Fig. 9(b) demonstrates the calculated INL compared to transistor-level simulations for an eight-stage DTC. The segmented architecture helps to reduce the maximum current spike drawn from the supply. It also helps to reduce the integrated jitter performance of the DTC. In the actual implementation, non-linear MOS capacitors were employed to maintain very compact design at the expense of slightly degraded linearity performance. Post-layout Monte-Carlo simulations shown in Fig. 11 indicate about 1 LSB peak INL, where LSB is equal to about 2 ps.

DTC non-linearity leads to imperfect QNC. For a first-order $\Delta\Sigma$ modulator, the quantization noise (e_{q}), and hence the DTC control word, have a sawtooth periodic pattern with frequency $F_{\mathrm{FRAC}} = \alpha F_{\mathrm{OUT}}$ as shown in Fig. 3, which passes through the DTC non-linearity and produces a periodic signal with F_{FRAC} frequency and waveform similar to DTC INL characteristics.

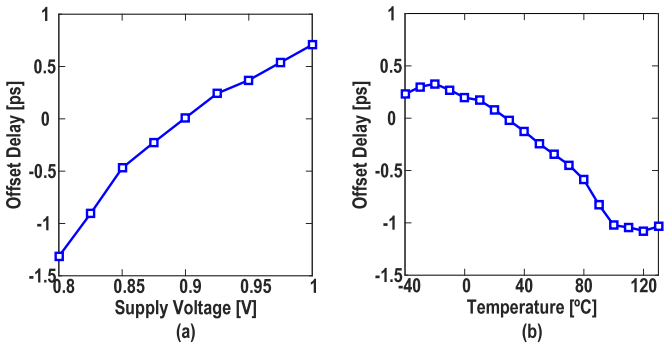

Fig. 12. Impact of (a) supply voltage and (b) temperature variations on the time offset between the DLL clock paths after the offset calibration step.

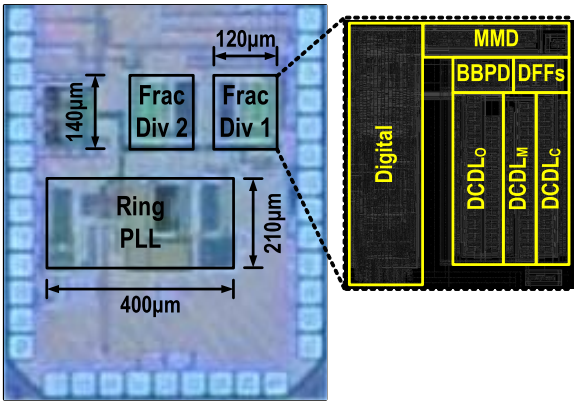

Fig. 13. Die micrograph of the clock generation unit and zoomed-in FDIV layout.

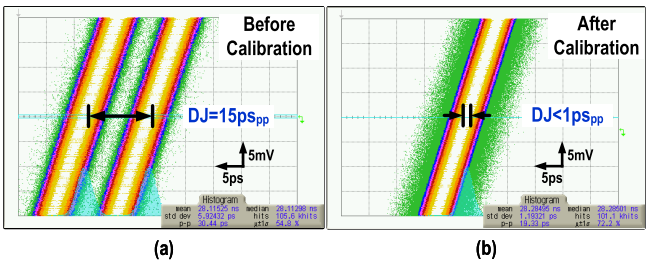

Fig. 14. Measured jitter histograms at 975-MHz FDIV output frequency. (a) Before and (b) after DTC calibration.

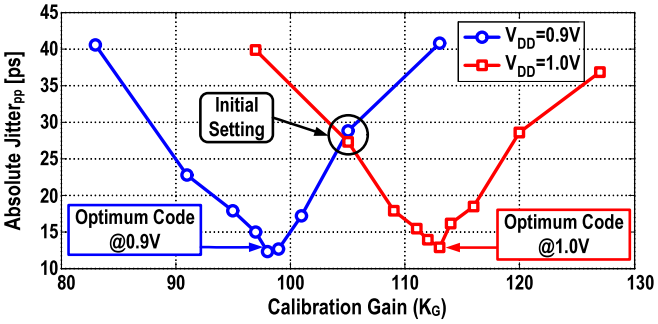

Fig. 15. Measured absolute peak-to-peak jitter as a function of the gain calibration code (K_G) for different supply voltages.

This introduces a maximum DJ equals to the peak of the INL characteristics, from which we can calculate the rms jitter value and the spur level at F_{FRAC}.

Any inaccuracy in the DTC gain calibration, leads also to imperfect QNC. First, any drift in the time offset between DLL clock paths will translate to an error in the calibration factor K_G and eventually translate to DJ at the output clock. Fig. 12 demonstrates transistor-level simulation results of the time offset between DLL clock paths across supply and temperature variations after the offset foreground calibration step. Second, any mismatch between main $T_{DTC,M}$ and complementary $T_{DTC,C}$ incremental delay range, will also translate to an error in the calibration factor K_G and eventually translate to DJ at the output clock. This is evaluated using Monte-Carlo simulations with 200 runs, where the mean and standard deviation of $dT = T_{DTC,M} - T_{DTC,C}$ equal to -0.76 and 1.67 ps, respectively. This error can be reduced by increasing the size of the DTC delay cell at the expense of higher power consumption or calibrated using an extra foreground calibration step.

V. Measurement Results

A prototype clock generator was fabricated in a 65-nm process and the die photograph is shown in Fig. 13. Layout of the FDIV is shown on the right. Active area is 0.12 mm^2 of which the digital PLL occupies 0.084 mm^2 and two FDIVs each occupy only 0.017 mm^2. The PLL design is based on the ring-based digital PLL presented in [24]. It multiplies a 50-MHz reference frequency and provides a 5-GHz output. In order to clearly identify the additive phase jitter and spurious performance of the proposed stand-alone FDIV, it is fully characterized using a 5-GHz clean external clock. The measured integrated jitter (10 kHz–40 MHz) of the 5-GHz clock is less than 0.2 ps$_{rms}$. Measured results of the FDIV at 975-MHz output frequency (5-GHz input clock and fractional division of 5.125) are presented next. Fig. 14 shows the measured jitter before and after the DTC calibration. In the absence of DTC gain calibration, $\Delta\Sigma$ quantization error leakage limits the DJ to 15 ps [Fig. 14(a)]. DTC gain calibration reduces the quantization error leakage significantly resulting in a DJ of less than 1 ps [Fig. 14(b)]. To illustrate the sensitivity of output jitter to environmental changes and the ability of calibration unit to track them, peak-to-peak jitter is plotted as a function of the gain calibration code for different supply voltages in Fig. 15. DTC gain decreases as supply voltage (V_{DD}) increases, and the optimal calibration code (K_G) shifts from 98 at V_{DD} of 0.9 V to 113 at V_{DD} of 1.0 V. The calibration loop always converges to the optimum calibration code regardless of the output frequency. The peak-to-peak jitter at the optimal gain setting is 13 ps.

The phase noise performance of the stand-alone FDIV is measured using Agilent E5052B signal source analyzer (SSA). Fig. 16(a) shows the measured phase noise plot of the FDIV output (after divide-by-2) when the integer and fractional divide ratios are set to 5, and 2^{-10}, respectively. The additive jitter of the FDIV is mostly deterministic and is due to DTC quantization error and INL. The worst case fractional spur is

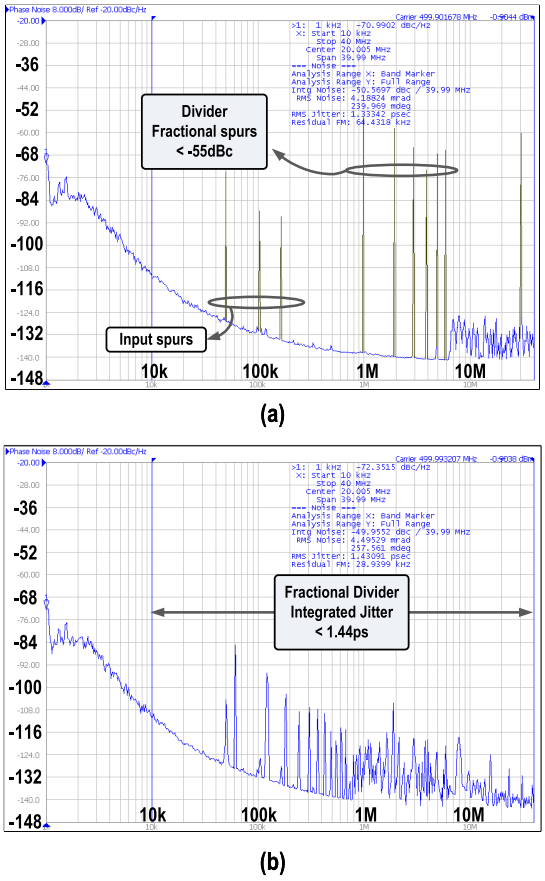

Fig. 16. Measured phase noise performance of the stand-alone FDIV when (a) $\alpha = 2^{-10}$ and (b) $\alpha = 2^{-14}$.

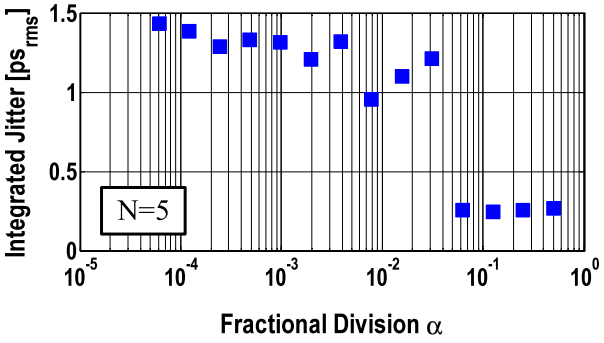

Fig. 17. Measured rms jitter integrated from 10 kHz to 40 MHz as a function of fractional division ratio (α).

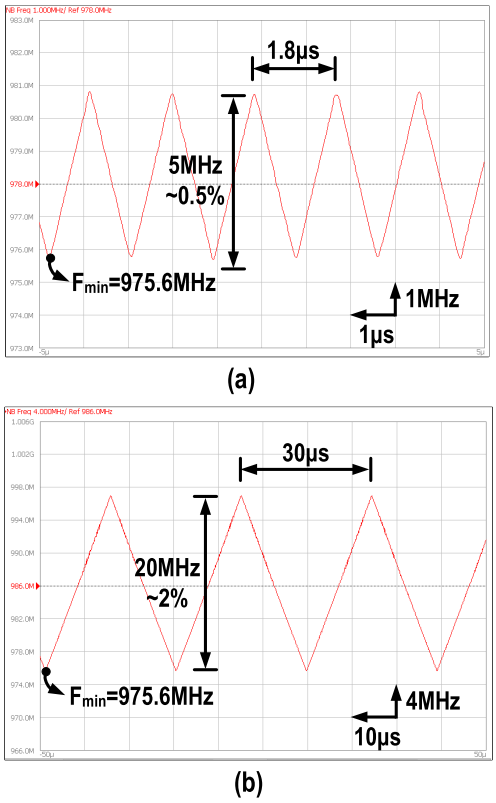

Fig. 18. Measured spread spectrum frequency modulation of the FDIV output in time-domain in case of (a) 550-kHz triangle wave with 0.5% modulation depth and (b) 33-kHz triangle wave with 2% modulation depth.

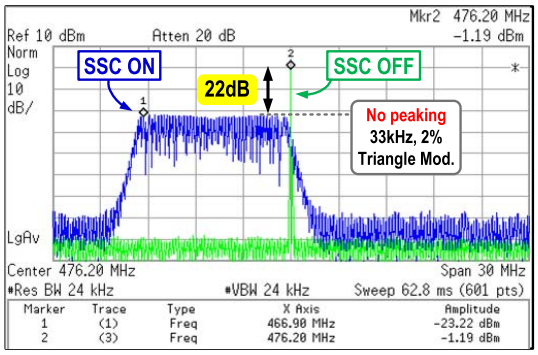

Fig. 19. Measured FDIV output spectrum with and without SSC.

better than −55 dBc. This translates to an estimated DJ of 3.55 ps, using Fourier analysis of a periodic sawtooth phase deviation [35]. The measured integrated jitter from 10 kHz to 40 MHz is about 1.3 ps_{rms}. The worst case phase noise performance occurs when the fractional part α approaches 0 or 1. When an α of 2^{-14} is used, the measured integrated jitter increased to about 1.44 ps_{rms}, as shown in Fig. 16(b). Fig. 17 shows the measured integrated jitter for different fractional division ratios.

Spread spectrum modulation capability of the FDIV is characterized in both time and frequency domains. Fig. 18(a) plots the measured output frequency as a function of time, when a 0.55-MHz triangle wave with 0.5% modulation depth is used. Because of the open loop architecture of FDIV, modulation BW is unlimited, and the triangle wave in the plot has very sharp transitions indicating no filtering even with this very wide-BW modulation signal. The modulation depth can be varied precisely to control the amount of EMI reduction depending on the application, unlike SSCGs that use direct VCO modulation technique [36]. Fig. 18(b) shows the measured output frequency as a function of time, using a standard 33-kHz triangle modulation and a modulation depth of 2%. FDIV output spectra (after divide-by-2) shown in Fig. 19 illustrate a peak EMI reduction of better than 22 dB is achieved. This excellent reduction is due to unlimited modulation BW of the open loop FDIV.

TABLE I
FDIV PERFORMANCE SUMMARY

	Elkholy [24] JSSC'16	Li [7] ISSCC'12	Tsai [34] ISSCC'15	Jang [10] VLSIC'15	De Caro [11] JSSC'10	De Caro [2] JSSC'15	This Work
Architecture	Frac-N DPLL	Frac-N DPLL	Frac-N DPLL	Frac-N DPLL (2-Point Mod.)	Digital Period Synthesizer	Digital Period Synthesizer	Frac-N Divider
Technology [nm]	65	22	16	65	65	28	65
Supply [V]	0.9	1	0.52-0.8	1.2	1.2	1	0.9
Input Freq. [GHz]	0.05	0.025-0.2	0.2	0.025	1.27	3.3	5.0*
Output Freq. [GHz]	2.0-5.5	0.6-3.6	0.25-4.0	2.5	0.18-1.27	0.2-3.3	0.02-1.0
Integrated Jitter [ps_{rms}]	1.9	10	3.3	N/A	12.8	3.16	1.44**
Instantaneous Switching	No	No	No	No	Yes	Yes	Yes
SSC Capability	Yes	Yes	Yes	Yes	Yes	Yes	Yes
EMI Reduction	N/A	N/A	24dB @ 0.5% of 3GHz [RBW=30kHz]	18dB @ 0.5% of 2.5GHz [RBW=30kHz]	20.5dB @ 6% of 750MHz [RBW=100kHz]	27dB @ 10% of 1GHz [RBW=100kHz]	22.3dB @ 2% of 1GHz [RBW=24kHz]
Power Consumption	4.0mW @5GHz	18.4mW @3.6GHz	9.3mW @3GHz	6.0mW @2.5GHz	19.8mW @1.27GHz	10.3mW @1GHz	3.2mW @1GHz
Power Eff. [mW/GHz]	0.8	5.1	3.1	2.4	15.6	10.3	3.2†
Area [mm^2]	0.084	0.03	0.029	0.05	0.044	0.031	0.017†

* Provided externallay or internally using the PLL reported in [24], ** Measured using external 5GHz input clock with 200fs_{rms} jitter,
† For a single stand-alone FDIV, and does not account for the integrated PLL.

TABLE II
MOSFET MODEL EQUATIONS USED IN CALCULATION

NMOS	PMOS
$\frac{I_n}{V_{DD}} = \begin{cases} 0 & \upsilon_i < n \\ K_{sn}(\upsilon_i - n)^{\alpha_n} & \upsilon_o \geqslant \upsilon'_{don} \\ K_{ln}(\upsilon_i - n)^{\frac{\alpha_n}{2}}\,\upsilon_o & \upsilon_o < \upsilon'_{don} \end{cases}$	$\frac{I_p}{V_{DD}} = \begin{cases} 0 & 1-\upsilon_i < p \\ K_{sp}(1-\upsilon_i - p)^{\alpha_p} & 1-\upsilon_o \geqslant \upsilon'_{dop} \\ K_{lp}(1-\upsilon_i - p)^{\frac{\alpha_p}{2}}(1-\upsilon_o) & 1-\upsilon_o < \upsilon'_{dop} \end{cases}$
$\upsilon'_{don} = \upsilon_{don}\left(\frac{\upsilon_i - n}{1-n}\right)^{\frac{\alpha_n}{2}}$	$\upsilon'_{dop} = \upsilon_{dop}\left(\frac{1-\upsilon_i - p}{1-p}\right)^{\frac{\alpha_p}{2}}$
where $\upsilon_i = V_{GS}/V_{DD}$, $\upsilon_o = V_{DS}/V_{DD}$, $n = V_{THn}/V_{DD}$, $\upsilon_{don} = V_{DOn}/V_{DD}$, $K_{sn} = I_{DOn}/(V_{DD}(1-n)^{\alpha_n})$, $K_{ln} = I_{DOn}/\left(V_{DD}(1-n)^{\frac{\alpha_n}{2}}\upsilon_o\right)$	where $\upsilon_i = 1 - V_{SG}/V_{DD}$, $\upsilon_o = 1 - V_{SD}/V_{DD}$, $p = \lvert V_{THp}\rvert/V_{DD}$, $\upsilon_{dop} = \lvert V_{DOp}\rvert/V_{DD}$, $K_{sp} = I_{DOp}/(V_{DD}(1-p)^{\alpha_p})$, $K_{lp} = I_{DOp}/\left(V_{DD}(1-p)^{\frac{\alpha_p}{2}}\upsilon_o\right)$

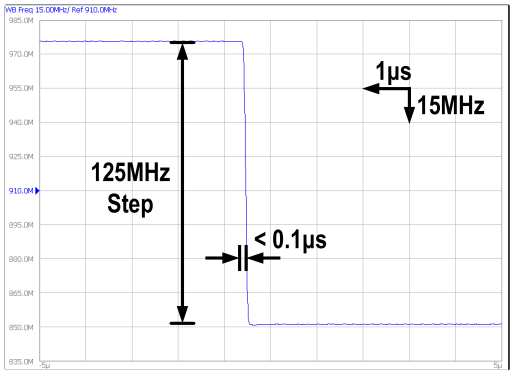

Fig. 20. Measured instantaneous frequency switching of the FDIV.

Instantaneous frequency switching capability of the FDIV was measured by changing the fractional part from 1/8 to 7/8, which translates to a frequency step of about 125 MHz. The resulting output frequency plotted as the function of time in Fig. 20 shows that switching time is less than 100 ns, which is limited by the instrument. Power consumption of all the blocks scales almost linearly with output frequency except for the MMD, whose power scales with input clock frequency. The total power consumption is about 3.2 mW at 1-GHz output frequency and about 1.1 mW at 100-MHz output frequency. Table I shows the performance summary and comparison to state-of-the-art designs. The proposed fractional-N clock generator achieves excellent jitter performance of less than 1.5 ps_{rms}. The all-digital implementation of the divider occupies the smallest area compared to state-of-the-art designs.

VI. CONCLUSION

In conclusion, an all-digital generic multi-output clock generator is proposed to meet diverse clocking requirements in SoCs. The proposed open loop FDIV architecture achieves excellent jitter performance by canceling $\Delta\Sigma$ quantization error using a DTC. Robust performance is achieved across PVT variations by using background calibration. The measured results of the FDIV indicate a low peak-to-peak jitter, excellent spread spectrum EMI reduction, and instantaneous frequency switching.

APPENDIX

The α-power law MOS model [29], [30] has four parameters: the velocity saturation index (α), the drain current (I_{DO}) at $V_{GS} = V_{DS} = V_{DD}$, the drain saturation voltage (V_{DO}) at $V_{GS} = V_{DD}$, and the threshold voltage (V_{TH}). After normalizing the model parameters to supply voltage (V_{DD}), NMOS and PMOS model equations, ignoring channel length modulation, are listed in Table II.

As shown in Fig. 8, it is reasonably accurate to assume step input for INV1, where the switching threshold can be defined at $V_{DD}/2$. NMOS device M_{n1} is in saturation and PMOS device M_{p1} is in cutoff during the output transition from V_{DD} to $V_{DD}/2$. Neglecting the non-linearities in load capacitance C_1, normalized output voltage, v_{o1}, is determined by solving the current differential equation $I_{n1} = -C_1 V_{DD} \cdot d v_{o1}/dt$. The high-to-low propagation delay of the first inverter is given by

$$t_{d1} = t|_{v_{o1}=0.5} = \frac{C_1}{2K_{sn1}(1\text{-}n_1)^{\alpha_{n1}}} = \frac{C_1 V_{DD}}{2\, I_{DOn1}}. \tag{9}$$

For INV2, the fast (or step) input assumption is not valid, and we have to consider the slow falltime of the input edge similar to [29] and [30]. The normalized input voltage of INV2 can be expressed as

$$v_{i2} = \begin{cases} 1, & t < 0 \\ 1\text{-}t/\tau_F, & 0 < t < \tau_F \\ 0, & t > \tau_F \end{cases} \tag{10}$$

where the ramp slope can be approximated from INV1 output as $-1/\tau_F \approx d v_{o1}/dt = -1/2t_{d1}$. To solve the differential equation using analysis in [29], the short circuit current flowing through the NMOS device M_{n2} is neglected, and only the current through PMOS device M_{p2} is considered $I_{p2} = +C_2 V_{DD} \cdot d v_{o2}/dt$. The normalized output voltage waveform and the low-to-high propagation delay of the second inverter are expressed by

$$v_{o2} = \frac{K_{sp2}\tau_F}{C_2} \cdot \frac{(t/\tau_F - p_2)^{\alpha_{p2}}}{\alpha_{p2}+1} \tag{11}$$

$$\begin{aligned} t_{d2} &= t|_{v_{o2}=0.5} - 0.5\tau_F \\ &= \tau_F(p_2 - 0.5) + \left(\frac{C_2(\alpha_{p2}+1)}{2K_{sp2}}\right)^{\frac{1}{\alpha_{p2}+1}} \cdot \tau_F^{\frac{\alpha_{p2}}{\alpha_{p2}+1}} \end{aligned} \tag{12}$$

Then, the total delay equals

$$t_d[k] = A(C_o + k \cdot C_u) + B(C_o + k \cdot C_u)^{\frac{\alpha_{p2}}{\alpha_{p2}+1}} \tag{13}$$

where parameters A and B are given by

$$A = \frac{p_2}{K_{sn1}(1\text{-}n_1)^{\alpha_{n1}}} \tag{14}$$

$$B = \left(\frac{C_2(\alpha_{p2}+1)}{2K_{sp2}}\right)^{\frac{1}{\alpha_{p2}+1}} \left(\frac{1}{K_{sn1}(1\text{-}n_1)^{\alpha_{n1}}}\right)^{\frac{\alpha_{p2}}{\alpha_{p2}+1}}. \tag{15}$$

The second term of t_d is a non-linear function of k and directly appears as INL. For more accurate results, we have to consider the short circuit current I_{n2}, the differential equation is modified to $I_{p2} - I_{n2} = +C_2 V_{DD} \cdot d v_{o2}/dt$. During output transition from 0 to $V_{DD}/2$, it is reasonably accurate to assume, the PMOS device M_{p2} is in saturation, while NMOS device M_{n2} operates in linear region as long as $v_{o2} < v'_{don}$. To solve the differential equation explicitly, I_{n2} is approximated similar to [30] as

$$I_{n2}/V_{DD} = K_{ln2}(1\text{-}x - n_2)^{\frac{\alpha_{p2}}{2}} v_{o2} \simeq S(x - p_2) \tag{16}$$

where $x = t/\tau_F$ is the normalized time variable and S is the current slope factor. Then, the differential equation and its solution can be expressed by

$$\frac{d v_{o2}}{dx} = \frac{\tau_F}{C_2}(K_{sp2} \cdot (x - p_2)^{\alpha_{p2}} - S(x - p_2)) \tag{17}$$

$$v_{o2} = \frac{\tau_F}{C_2}\left(\frac{K_{sp2}(x - p_2)^{\alpha_{p2}+1}}{\alpha_{p2}+1} - \frac{S}{2}(x - p_2)^2\right). \tag{18}$$

By substituting v_{o2} of (18) in (16), we can calculate S by equating the approximate and the exact NMOS current in the linear region at $x = 0.5$ point

$$S = \frac{K_{sp2} \cdot (x - p_2)^{\alpha_{p2}}}{\alpha_{p2}+1} \times \left.\frac{K_{ln2} \cdot (1\text{-}x - n_2)^{\alpha_{n2}/2} \cdot \tau_F/C_2}{1 + 0.5(x - p_2) \cdot K_{ln2} \cdot (1 - x - n_2)^{\alpha_{n2}/2} \cdot \tau_F/C_2}\right|_{x=0.5}. \tag{19}$$

When v_{o2} reaches v'_{don}, M_{n2} enters saturation region. The onset of this region of operation ($x = x_{satn}$) can be found by equating (18) to v'_{don} where $v_i = 1\text{-}x$. Then, the differential equation and its solution can be expressed by

$$\frac{d v_{o2}}{dt} = \frac{\tau_F}{C_2}(K_{sp2}(x - p_2)^{\alpha_{p2}} - K_{sn2}(1\text{-}x - n_2)^{\alpha_{n2}})$$

$$\begin{aligned} v_{o2} = v'_{don} &+ \frac{\tau_F}{C_2} \cdot \frac{K_{sp2}}{\alpha_{p2}+1} \\ &\times ((x - p_2)^{\alpha_{p2}+1} - (x_{satn} - p_2)^{\alpha_{p2}+1}) \end{aligned} \tag{20}$$

$$+ \frac{\tau_F}{C_2} \cdot \frac{K_{sn2}}{\alpha_{n2}+1} \times ((1\text{-}x - n_2)^{\alpha_{n2}+1} - (1\text{-}x_{satn} - n_2)^{\alpha_{n2}+1}). \tag{21}$$

Then, the low-to-high propagation delay of INV2 can be calculated as $t_{d2} = \tau_F\,(x_{m2} - 0.5)$, where x_{m2} is the normalized time value at which $v_{o2} = 0.5$. Then, the total delay and the INL of the DTC can be simply calculated.

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