# A 0.44-fJ/Conversion-Step 11-Bit 600-kS/s SAR ADC With Semi-Resting DAC

Sung-En Hsieh and Chih-Cheng Hsieh

***Abstract*— This paper presents an 11-bit ultralow voltage energy efficient successive approximation register (SAR) analog-to-digital converter (ADC). With the proposed semi-resting (SR) digital-to-analog convertor (DAC) switching scheme, this paper consumes only 6%–13.5% switching energy, compared to the state-of-the-art works. In addition, the SR switching scheme effectively reduces the differential nonlinearity and integral nonlinearity to be 1/2, compared to the conventional approach under the same matching conditions. With the proposed SR DAC switching scheme, this paper can handle the same input swing using a half supply and consume smaller power consumption. A cascade-input comparator is developed to consume only 49% of the power and 66% of the decision time with a threefold front-stage gain boost. The test chip occupies a core area of 0.035 mm$^2$ in 90-nm CMOS technology. The prototype consumes 187 nW at 600 kS/s with a single 0.3-V supply voltage. The achieved effective number of bits and spurious-free dynamic range at Nyquist input are 9.46 bits and 73 dB, respectively. The resultant Walden's figure of merit (FoM) and Schreier's FoM are 0.44 fJ/conversion-step and 180.8 dB, respectively.**

***Index Terms*— Low power, low voltage, successive approximation register analog-to-digital converter (SAR ADC).**

## I. Introduction

THE Internet-of-Things (IoT) enables an enormous number of physical devices to cooperate with each other through the Internet. In IoT nodes, successive approximation register (SAR) analog-to-digital converters (ADCs) are widely used because of their outstanding energy efficiency at moderate speed and resolution (up to hundreds of kilohertz with 8–12-bit resolution) [1]. State-of-the-art works (SAR ADCs) [2]–[14] have demonstrated a constantly improving and ultralow power consumption performance with technology evolution.

For switching energy reduction, the merged capacitor switching (MCS) [2], [3] reduces the bottom plate's voltage swing with a penalty of an extra reference voltage. The direct switching (DS) procedure [4] and the input-range-adaptive switching procedure [5] use coarse conversion and align switching at the fine conversion to omit the unnecessary trial-and-error digital-to-analog convertor (DAC) switching, which saves power. However, additional circuits for coarse/fine conversion and redundancy are needed with power and conversion time penalties. Merge and split (MAS) [6] and charge-averaging switching (CAS) [7] have demonstrated an ultralow switching energy consumption at the conversion phase by the merging operation of the bottom plate, but at the price of extra reset energy. With the shifting operation of the bottom plate at the MSB conversion, shifted monotonic switching (SMS) [8] and monotonic multi-switching (MMS) [9] effectively reduced the switching energy of the DAC. However, SMS and MMS suffer from the dynamic comparator offset and VCM reference inaccuracy.

The comparator is another power-hungry block of the SAR ADC. To reduce the comparator's power consumption, two-step ADC architectures [4], [10], [11] with coarse and fine conversions were proposed. The noise requirement, as well as power consumption of the comparator in coarse conversion, is relaxed. However, the mismatch between the coarse and fine conversions needs to be dealt with. An extra design effort like a redundancy arrangement is required. The majority voting [12] technique was proposed to relax the noise specification and power consumption of the comparator at non-critical conversion with the penalty of a complex critical decision detection circuit. Without full-swing discharging operation at the preamplifier's output of the comparator, a bidirectional comparator [13] effectively reduced the dynamic energy with the requirement of an additional sensing circuit.

To overcome the mentioned drawbacks, this paper proposes a semi-resting (SR) [14] switching scheme that uses the top-plate sampling and merging operations of the DAC for an MSB decision without any energy consumption. By using two identical 10-bit sub-ADCs to deal with the conversions of the input ranges of $0 > V_{ip} - V_{in} > -2V_{dd}$ and $2\ V_{dd} > V_{ip} - V_{in} > 0$, the resulting 11-bit ADC has a double input range (DIR) ($\pm 2V_{dd}$), compared to the conventional approach ($\pm V_{dd}$). This requires a relaxed (half) noise requirement of the comparator, sample-and-hold (S/H) circuit, VCM generator reference, and programmable amplifier with SNR loss. From a different perspective, the proposed SR technique can handle the same input swing ($\pm V_{ref}$) using a half supply to effectively reduce the ADC's power. Without the need of reset energy and an extra reference voltage, the proposed SR scheme consumes an average DAC switching energy of 23.1 CV$^2$ with a reduction of 91%, 86.4%, 89.9%, and 90.1% compared to the monotonic switching (MS) [15], DIR [16], DS [4], and MAS switching [6] procedures, respectively.

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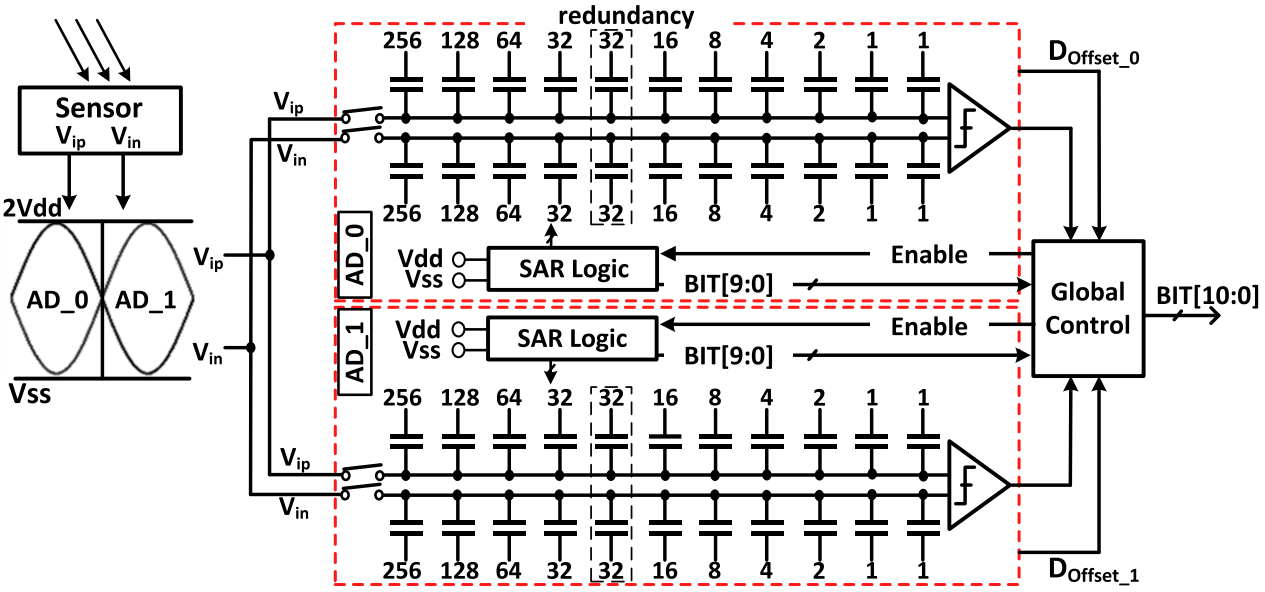



Fig. 1. Proposed SAR ADC architecture.

Considering the linearity performance, the worst DNL peak usually happens at the MSB transition determined by the ratio of MSB and total capacitance in the conventional architecture. In the proposed SR switching scheme, the linearity at the MSB transition, depending on the alignment of two sub-ADCs, is guaranteed by the implemented foreground calibration rather than the capacitance ratio. This effectively reduces the matching requirement and unit capacitance value of the DAC as well. For power and noise reduction, a cascade-input (CI) comparator is developed to realize a boosted pre-amplifier gain without using a complex two-step architecture and critical detection decision circuit. The implemented prototype achieves an figure of merit (FoM) performance of 0.44 fJ/conversion, which is only half of the best-reported result [4].

The rest of this paper is organized as follows. Section II introduces the proposed ADC architecture and SR switching procedure. Section III describes the circuit implementation. The measurement results and performance comparison are provided in Section IV. Finally, conclusions are given in Section V.

## II. Proposed SAR ADC Architecture

Fig. 1 shows the architecture of the proposed 11-bit SAR ADC which is composed of two 10-bit sub-ADCs (AD_0 and AD_1) and one global control unit. Each 10-bit sub-ADC consists of a 9-bit C-DAC with one redundant bit (32 C: additional 64 LSB searching range), a comparator, and an SAR logic block. With the proposed SR and top-plate sampling techniques, a $2^{(N-2)}$-bit DAC is implemented for $N$-bit conversion which is only half of the conventional approaches with $2^{(N-1)}$-bit DAC. The AD_0 and AD_1 are designed to handle the conversions of the input ranges of $0 > V_{ip} - V_{in} > -2\ V_{dd}$ and $2\ V_{dd} > V_{ip} - V_{in} > 0$, respectively. By detecting the signal polarity (MSB) after the sampling phase, one of the 10-bit sub-ADCs is disabled (resting) for power reduction, that is, the SR DAC operation. Since one of the two sub-ADCs is disabled after the MSB decision and consumes no power, the power overhead from the extra sub-ADC is negligible. Considering the area, which is dominated by the DAC in SAR ADC, the proposed SR switching uses a smaller DAC ($0.25\times$ size) in each sub-ADC to achieve the same matching performance. Moreover, the total input range is effectively doubled to $\pm 2\ V_{dd}$, which is $\pm 0.6$ V at 0.3 V in this paper. Double-boosted S/H and local-boosted switches are implemented for linearity and the accuracy requirement under 0.3-V operation with special leakage control.

### A. Semi-Resting Switching Procedure

Fig. 2 shows a 4-bit example of the proposed SR switching procedure. It shows that only a 2-bit DAC is required for a 4-bit ADC conversion. During the sampling phase, the bottom plates of PDAC_1/NDAC_0 and PDAC_0/NDAC_1 are reset to $V_{dd}$ and $V_{ss}$, respectively. If the MSB $=$ 1, AD_0 is disabled and AD_1 solely takes over the remaining 10-bit conversion. Then, the bottom plates of AD_1 are merged together to generate the common-mode level of $V_{dd}/2$ by the charge averaging operation of the bottom-plate capacitor. The top-plate voltage shifts of PDAC_1 and NDAC_1 are $-V_{dd}/2$ and $+V_{dd}/2$, respectively, to generate the required total differential voltage shift of $-V_{dd}$ for the MSB-1 decision ($V_{ip} - V_{in} > V_{dd}$?) without consuming switching energy. If the MSB $= 0$, AD_1 is disabled and the bottom plates of chosen AD_0 are then merged together to create a differential voltage shift of $+V_{dd}$ on the top plates for the MSB-1 decision ($V_{ip} - V_{in} > -V_{dd}$?).

With the fixed common-mode voltage ($V_{dd}$) of $V_{PDAC}$ and $V_{NDAC}$, the remaining conversions of MSB-2 to LSB are accomplished in an MCS-based [2], [3] operation by switching the corresponding bottom plates from $V_{dd}/2$ to $V_{dd}$ or $V_{ss}$,

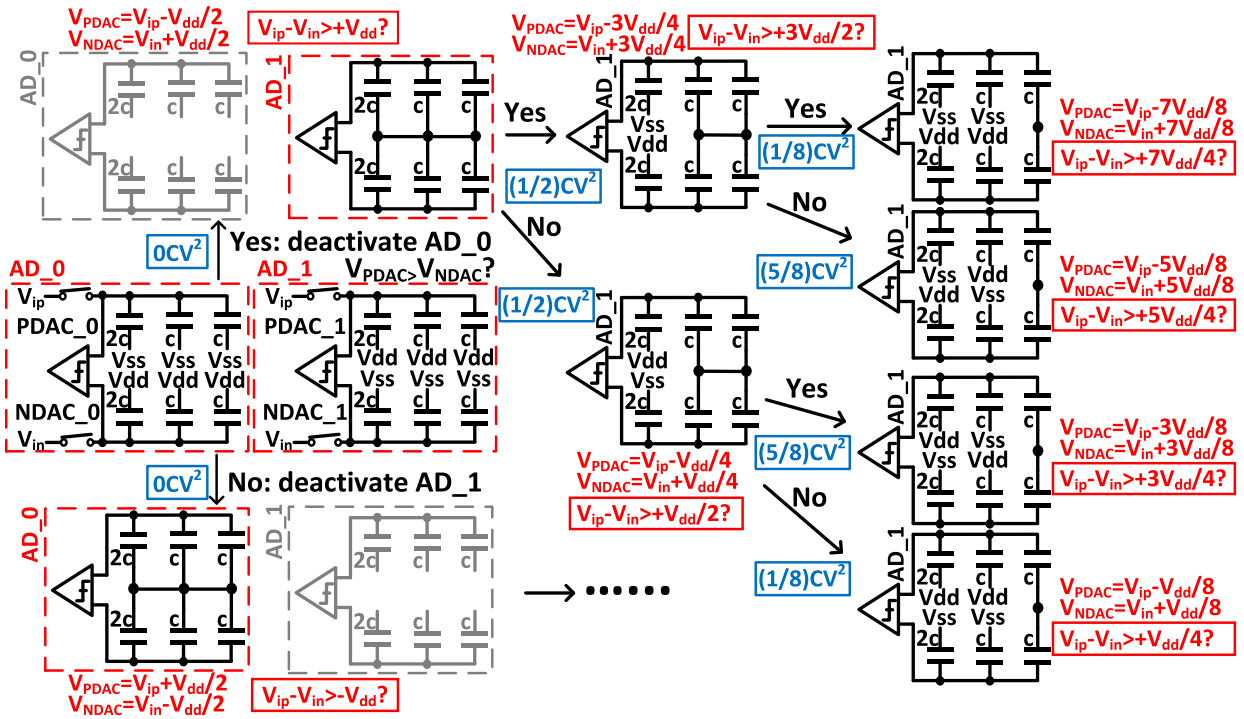



Fig. 2. 4-Bit conversion example of the proposed SR DAC.

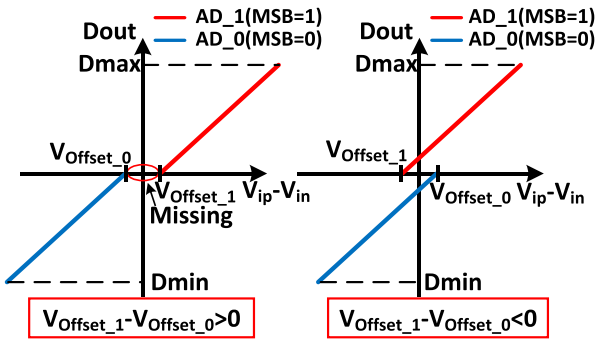



Fig. 3. Overall transfer curve without redundancy.

based on the comparison results. For example, if the MSB-1 comparison result = 1 ($V_{ip}$–$V_{in}$ > $V_{dd}$), the 2 C of P-DAC and N-DAC of the selected sub-ADC are switched to $V_{ss}$ and $V_{dd}$, respectively. This creates the required differential voltage shift of −1/2 $V_{dd}$ ($V_{ip}$–$V_{in}$ > 3/2 $V_{dd}$?). In contrast, when the comparison result = 0 ($V_{ip}$–$V_{in}$ < $V_{dd}$), the 2 C of P-DAC and N-DAC of the selected sub-ADC are switched to $V_{dd}$ and $V_{ss}$, respectively. This creates the required differential voltage shift of 1/2 $V_{dd}$ ($V_{ip}$–$V_{in}$ > 1/2 $V_{dd}$?). The same procedure is conducted until the last bit is converted.

### *B. Digital Foreground Calibration*

Considering the offset mismatch between the sub-ADCs (AD_0 and AD_1) which may cause a missing code error as shown in Fig. 3, a 64 LSB (±17 mV) redundancy is implemented with inserted 32 C to cover the variation-induced mismatch. From HSPICE simulation, the sigma value of the implemented comparator offset is 3.4 mV under a 0.3-V voltage supply. In this paper, the implemented overlap range of two transfer curves is 17 mV to cover an over three-sigma variation (one mismatch sigma = $3.4 \times \sqrt{2} = 4.8$ mV). This avoids missing codes.

With the insertion of redundancy and digital foreground calibration, the two sub-ADC's transfer curves are overlapped at the transition range ($V_{ip} - V_{in} \simeq 0$) to avoid missing codes, as shown in Fig. 4. The redundancy is used to extend the convertible input range of each sub-ADC to create a sufficiently overlapped range for foreground calibration. In the calibration operation, the $V_{dd}$ level is applied to both $V_{ip}$ and $V_{in}$ at the beginning. Then, the converted output codes, $D_{offset\_1}$ and $D_{offset\_0}$ of AD_0 and AD_1, are recorded, respectively. By extracting the offset difference ($D_{offset\_1} - D_{offset\_0}$) and adding it back to the converted code in the normal operation, the offset error is canceled out off-chip in the digital domain, and the transfer curves of the two sub-ADCs are aligned together. Furthermore, with a 5% supply variation and a 45 °C temperature variation, the post-layout simulation shows that the induced dynamic offsets are 0.083 and 0.48 LSB, respectively. Therefore, the process, voltage, and temperature variation of the comparator is tolerable with an infrequent and periodical foreground calibration. The required data mapping operation of the foreground calibration can be realized by a simple binary adder, which is common in ADCs with error tolerance (redundancy, sub-radix, and DAC calibration). Since the foreground calibration is activated only once at the startup stage or infrequently depending on the environment, the induced power penalty is negligible.

### *C. Switching Energy*

The average switching energy (including conversion and reset operations) of well-known techniques is derived and

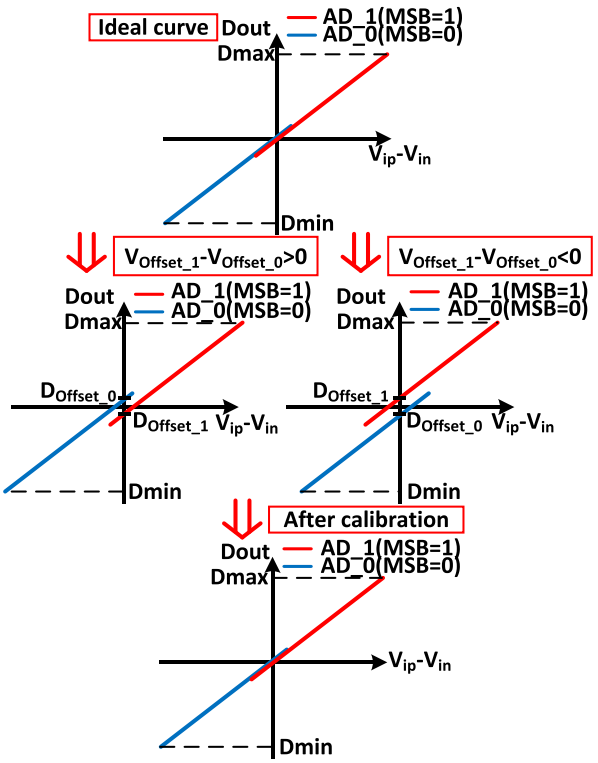



Fig. 4. Overall transfer curve and calibration flow with redundancy.

compared. For the case that every digital output code has the same occurrence rate and assuming $n$-bit conversion with an identical input range ($\pm V_{\text{ref}}$) for comparison, the average switching energy of MAS [6], MS [15], SMS [8], and MCS [2], [3] methods with reset energy is derived as follows:

$$E_{\text{merge and split}} = (2^{n-2} - 2^{-1} - 2^{n-4})CV_{\text{ref}}^2 + \sum_{i=2}^{n-1} 2^{n-i-3}(1 - 2^{-i+1})CV_{\text{ref}}^2 \quad (1)$$

$$E_{\text{monotonic}} = \sum_{i=1}^{n-1} (2^{n-2-i})CV_{\text{ref}}^2 \quad (2)$$

$$E_{\text{SMS}} = \sum_{i=1}^{n-2} (2^{n-5-i})CV_{\text{ref}}^2 \quad (3)$$

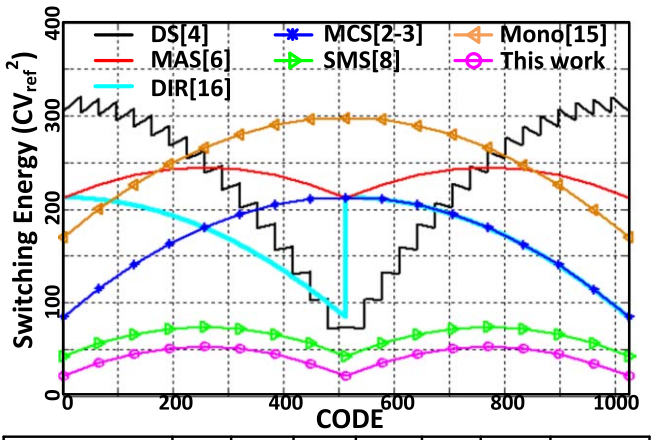
$$E_{\text{MCS}} = \sum_{i=1}^{n-1} 2^{n-2-2i}(2^i - 1)CV_{\text{ref}}^2. \quad (4)$$

The average switching energy of an $n$-bit SAR ADC using the SR switching procedure without a redundant bit (w/o rd) is derived as follows:

$$E_{\text{SR}} = \sum_{i=1}^{n-2} 2^{n-5-2i}(2^i - 1)CV_{\text{ref}}^2 \quad (5)$$

Including the energy consumption of redundancy switching, the average switching energy is

$$E_{\text{SR}} = (2^{n-9} - 2^{-4})CV_{\text{ref}}^2 + \sum_{i=1}^{n-2} 2^{n-5-2i}(2^i - 1)CV_{\text{ref}}^2 \quad (6)$$




| Switching energy | DIR | DS | MAS | MCS | SMS | Mono | This work |
|---|---|---|---|---|---|---|---|
| $CV^2$ | 169.7 | 229.7 | 233.9 | 170.2 | 31.8 | 255.5 | 23.1 |

Fig. 5. Switching energy versus output code.

Fig. 5 shows the DAC switching energy curves of a 10-bit conversion case, including both sampling and conversion phases versus the digital output code, using the proposed SR switching procedure and other well-known techniques. Due to the reduced bottom-plate swing and switching capacitance, the proposed SR DAC consumes an average switching energy of 23.1 $CV_{\text{ref}}^2$ (including 32 C redundancy). This is only 13.5% of MCS/DIR [16] (170.2 $CV_{\text{ref}}^2$/169.7 $CV_{\text{ref}}^2$) and around 6%–10% of the others (DS: 229.7 $CV_{\text{ref}}^2$, MAS: 233.9 $CV_{\text{ref}}^2$) without any extra common-mode reference voltage and reset energy.

The capacitor array has the unwanted bottom-plate parasitic effect due to the existence of a metal to substrate capacitor. After the layout extraction, the parasitic capacitance of the bottom plate is around 10% of the DAC capacitance. The charging and discharging operations of the bottom-plate parasitic capacitors also consume switching energy during the conversion. Assuming the bottom-plate parasitic capacitance of each bit is a ratio of the corresponding top-plate capacitance and binary weighted, the average bottom-plate switching energies of MAS, MS, SMS, MCS, and the proposed SR are derived as follows:

$$E_{\text{merge and split}} = (2^{n-2} + 2^{n-4} + 2^{-2} - 1)CV_{\text{ref}}^2 \quad (7)$$

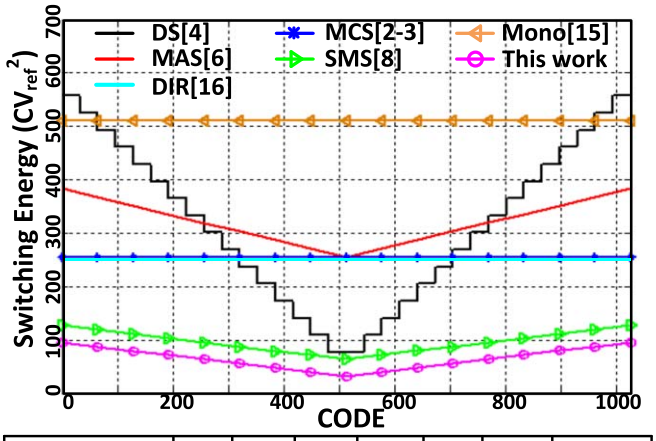
$$E_{\text{monotonic}} = (2^{n-1} - 1)CV_{\text{ref}}^2 \quad (8)$$

$$E_{\text{SMS}} = (2^{n-5} - 2^{-3} + 2^{n-4})CV_{\text{ref}}^2 \quad (9)$$

$$E_{\text{MCS}} = (2^{n-2} - 2^{-1})CV_{\text{ref}}^2 \quad (10)$$

$$E_{\text{SR}} = (2^{n-4} - 2^{-3})CV_{\text{ref}}^2 \quad (11)$$

Since the bottom-plate swing of the SR scheme is only 0.25 $V_{\text{dd}}$ compared to $V_{\text{dd}}$ or 0.5 $V_{\text{dd}}$ of the others, it consumes the smallest bottom-plate related switching energy. Fig. 6 shows the bottom-plate switching energy curves versus the digital output. The SR switching procedure consumes an additional 63.9 $CV_{\text{ref}}^2$ switching energy due to the bottom-plate parasitic capacitors, which is 20.1%, 20.5%, 25%, 25%, 66.6%, and 12.5% for DS, MAS, MCS, DIR, SMS, and MS, respectively. Moreover, this paper uses an $n-2$-bit capacitor array for $n$-bit




| Switching energy | DIR | DS | MAS | MCS | SMS | Mono | This work |
|---|---|---|---|---|---|---|---|
| $CV^2$ | 255.5 | 312 | 312 | 255.5 | 95.9 | 511 | 63.9 |

Fig. 6. Bottom-plate switching energy versus output code.

conversions which is only half, compared to the conventional approaches with the $n-1$-bit DAC. The unwanted bottom-plate parasitic capacitance is further reduced with the shorter bottom-plate routing.

Overall, this paper achieves the lowest DAC switching energy and bottom-plate switching energy without issues of the reset energy, two-step architecture, common-mode shift, and additional voltage reference, as compared to the other methods.

### D. Non-Linearity

The top-plate sampling SAR ADC's linearity is dominated by the mismatch of the capacitor array and signal-dependent parasitic capacitance of the comparator input device. Using the device and parasitic models provided by the foundry, the simulated error induced by signal-dependent capacitance with full-range input sweeping is smaller than 0.1 LSB for an 11-bit ADC under the 0.3-V supply.

Considering the non-linearity from the unit capacitor mismatch, the worst DNL/integral nonlinearity (INL) error usually occurs at the largest capacitance switching with the largest toggling number of the unit capacitor. The reported subranging SAR ADCs (for example, first 2-bit guess: F2G [17]) show an improved DNL/INL performance by omitting the largest toggling capacitance with a complex coarse/fine operation and switching control. In this paper, for an 11-bit case, the DNL/INL value of the SR scheme at code 1024 is calibrated to be zero by the implemented foreground calibration, as mentioned in Section II-B. Since each sub-ADC uses the same capacitance of the 11-bit ADC to handle the 10-bit resolution, the non-linearity performance is expected to be improved twofold. Fig. 7 shows the simulated DNL/INL performances of an 11-bit example for different switching schemes with the same matching conditions of the MSB capacitor (sigma = 0.2%). The achieved INL peak of the SR scheme is 0.51 LSB, which is only 0.5× and 0.57× that of the conventional MCS and F2G schemes, respectively. Therefore, to achieve the same INL performance, the unit capacitor of each sub-ADC can be further reduced to 1/4 (0.25× size). The total DAC area of the two sub-ADCs can be reduced by half.

## III. Implementation of Key Building Blocks

To operate at 0.3 V with a doubled input range and shifted common mode voltage, the S/H circuit and the dynamic comparator in this paper need special design considerations.

### A. Double-Bootstrapped Sample-and-Hold

In SAR operation, the top-plate voltage converges to the input common-mode voltage ($V_{\rm com}$) at the end of conversion. Therefore, the channel (drain-to-source) voltages of sampling switches of $V_{\rm ip}$ and $V_{\rm in}$ during the conversion are $|V_{\rm com}-V_{\rm in}|$ and $|V_{\rm com}-V_{\rm ip}|$, respectively. The varied drain-to-source voltage of sampling switches during conversion causes a signal-dependent leakage and affects linearity. Due to the DIR ($\pm 2\ V_{\rm dd}$) and shifted common-mode voltage ($V_{\rm dd}$) in the SR scheme, the varied range of the drain-to-source voltage of sampling switches is doubled. This makes the leakage current at the hold phase and the linearity of resistance at the sampling phase worse. The simulated effective number of bits (ENOB) of the conventional bootstrapped S/H circuit [15] drops from 13 to 11 bits due to the adverse signal-dependent effects.

To deal with the mentioned issue, the double-boosted S/H with adaptive body voltage biasing [17] is adopted, as shown in Fig. 8. The additional gate M2s is implemented for input isolation at the holding phase, which is described in detail. To avoid the body leakage from forward-biased parasitic diodes in the bootstrapping operation, the body node of PMOS devices in the S/H circuit is connected to the proper bias with a separated-well design, as shown in Fig. 8. By doing this, the leakage current is negligible from the HSPICE simulation. This paper also uses the same boosted control signal for the sampling switches of two sub-ADCs to avoid the timing mismatch. At the sampling phase, the body nodes of cascaded sampling switches (M1 and M3) are connected to $V_{\rm in}$ to eliminate the body effect (source-to-body voltage $V_{\rm sb}=0$) and keep the turn-ON resistance constant with a fixed gate-to-source voltage ($V_{\rm gs}$) and $V_{\rm sb}$ for $\pm 2\ V_{\rm dd}$ input swing. At the holding phase, the gate and body nodes of cascaded sampling switches (M1s and M3s) are connected to ground for a better "OFF" operation. At the same time, the internal node between M1s and M3s is reset to the input common-mode level ($V_{\rm dd}$) by turning on M2s to minimize the signal-dependent channel leakage during conversion. From HSPICE simulation, the leakage current of the proposed S/H is reduced from 10.1 nA to 112 pA. The simulated ENOB is over 13 bits with the eliminated body effect and reduced signal-dependent leakage current.

### B. Cascade-Input Comparator

For the conventional two-step comparator in Fig. 9 [4], the gain of the front stage can be expressed as follows [8]:

$$A_{\rm preamp}=\frac{\Delta V_o}{\Delta V_i}=\frac{g_m\times(V_{\rm DD}-V_{\rm oen})}{I_{\rm cm}} \tag{12}$$

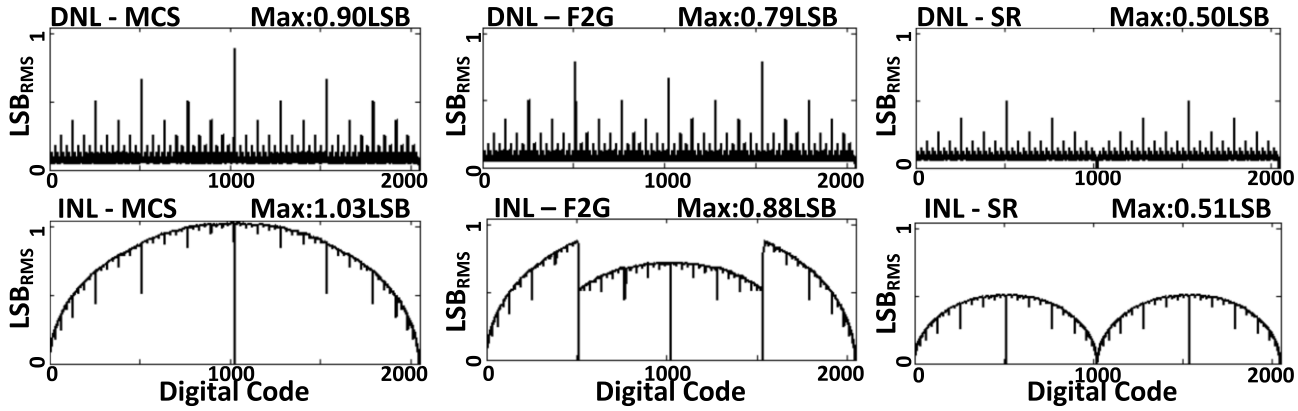



Fig. 7. Static performance of 11-bit ADC with MCS, F2G, and the proposed SR switching schemes.

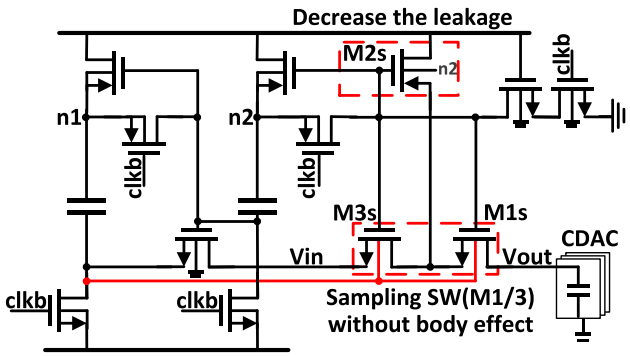



Fig. 8. Proposed S/H circuit.

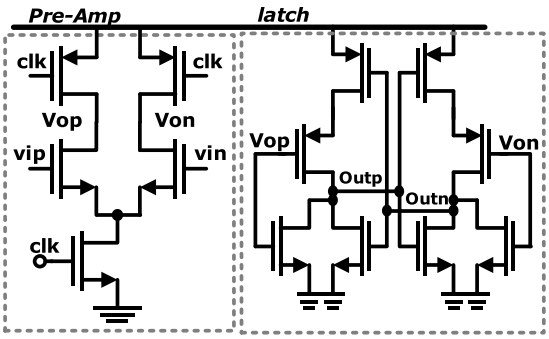



Fig. 9. Schematic of the conventional two-step comparator.

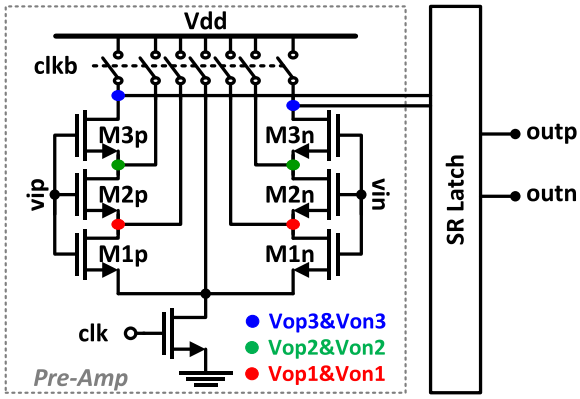



Fig. 10. Proposed CI comparator.

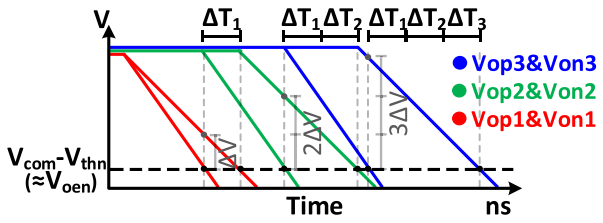



Fig. 11. Output behaviors of the CI pre-amplifier.

where $I_{cm}$ is the common-mode current of the pre-amplifier pair, and $V_{oen}$ is the output level to enable the cross-coupled latch. This shows that the preamplifier's gain is independent of output loading ($C_{load}$) and input pair device sizing. Therefore, to increase the preamplifier's gain and noise performance, the CI comparator is proposed, as shown in Fig. 10. Fig. 11 shows the output behaviors of the CI pre-amplifier. At the reset phase, all the internal nodes ($V$op 1–3, $V$on 1–3) of the stacking input pairs (M1p/M1n, M2p/M2n, and M3p/M3n) are reset to $V_{dd}$ for initialization. In the comparison procedure, the input pairs M1p/M1n (1st) to M3p/M3n (3rd) are activated sequentially and chronologically with the corresponding ramping-down outputs. Since the input level of each input pair needs to be large enough (near $V_{thn}$) to weakly turn ON the input devices to enable the amplification, the input difference is equivalently amplified in succession from nodes Vop1/Von1 to Vop3/Von3 before the latch decision. This operates like a multi-stage voltage-to-time converter (VTC). First, the M1 pair is activated to generate the time difference $\Delta T_1$ on Vop1/Von1 from the V-to-T (V2T) conversion defined by the turn-on threshold voltage of the input pair ($< V_{com}-V_{thn}$, $V_{com}$: input common mode, $V_{thn}$: threshold voltage of input device). When Vop1/Von1 levels are discharged to a low enough level ($< V_{com}-V_{thn}$) to activate the M2 pair, M2p and M2n are sequentially turned on with a different starting point ($\Delta T_1$). After the V2T conversion phase of M2p and M2n, an additional $\Delta T_2$ (ideally, $\Delta T_1 = \Delta T_2$) is generated and the resulting time difference on Vop2/Von2 is "$\Delta T_1 + \Delta T_2$." The time differences $\Delta T_1$, $\Delta T_2$, and $\Delta T_3$ generated from the M1, M2, and M3 pairs are uncorrelated to each other and result in threefold amplification ($\Delta T_{overall} = \Delta T_1 + \Delta T_2 + \Delta T_3 = 3\Delta T$). As a result, the effective front-stage gain is increased threefold with a three-stacking cascaded input pair in this design, compared to the conventional

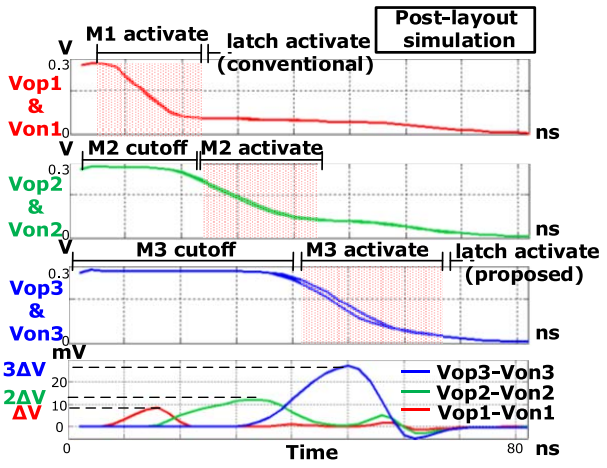



Fig. 12. Post-layout simulation result of the CI pre-amplifier.

architecture with a single input pair (M1p/M1n only). The post-layout simulation in Fig. 12 shows the multi-stage VTC behavior of the proposed pre-amplifier with a threefold gain enhancement.

The input-referred noise of the CI comparator ($\sigma_{\text{comp}}$) can be formulated as

$$\sigma_{\text{comp}}^2 = \frac{\sigma_{\text{one}}^2}{S} + \frac{\sigma_{\text{latch}}^2}{(SA_{\text{input}})^2} \tag{13}$$

where $\sigma_{\text{one}}$ is the input-referred noise of the input pair (one stacking), $A_{\text{input}}$ is the gain of the input pair (one stacking), $S$ is the cascaded number of input pairs, and $\sigma_{\text{latch}}$ is the noise of the cross-coupled latch. This shows that the noise contributions of the input pair ($\sigma_{\text{one}}$) and latch ($\sigma_{\text{latch}}$) are effectively reduced by the cascaded number of $S$. The simulated comparator noise, compared with different stacking numbers of the input pair with and without the ideal (noise free) latch, is summarized in Table I. For an ideal (noise free) latch, this shows that the comparator noise is improved by a factor of around $\sqrt{S}$ (as expected) by considering the preamplifier's contribution only. For a noisy latch, this shows that the comparator noise (dominated by the latch's contribution) is improved by a factor of around $S$ (as expected) due to the effective gain boosting of the CI structure. In contrast, the conventional approach of adding loading capacitance at the output nodes of the preamplifier can only reduce the noise of the input pair and not the latch noise. This limits the achievable noise reduction performance. With the threefold boosted front-stage gain and reduced latch noise, the proposed CI comparator consumes only 49% of the power and 66% of the decision time to achieve the same input-referred noise as the simulation, compared to the conventional approach with loading insertion.

### C. Capacitor Array Arrangement

Since the top-plate level is interfered with by the bottom-plate noise after the sampling phase, the insertion of a bottom-plate filtering capacitor [18] is used to reduce the noise interference from the bottom plate during conversion. With the inserted capacitor $C_{\text{bot}}$ (180 fF) and a total filtering capacitance of 240 fF, the integrated noise power during conversion is reduced to 53%, compared to the conventional implementation, as shown in Fig. 13.

TABLE I
COMPARISON TABLE OF CI COMPARATOR WITH 1–3 STACKING NUMBER

| | Energy | w/o ideal latch | | w/i ideal latch | |
|---|---|---|---|---|---|
| | | noise | factor | noise | factor |
| S=1 | $1CV^2$ | 1290uV | 1x | 845uV | 1x |
| S=2 | $2CV^2$ | 666uV | 0.51x | 496uV | 0.58x |
| S=3 | $3CV^2$ | 451uV | 0.34x | 361uV | 0.42x |

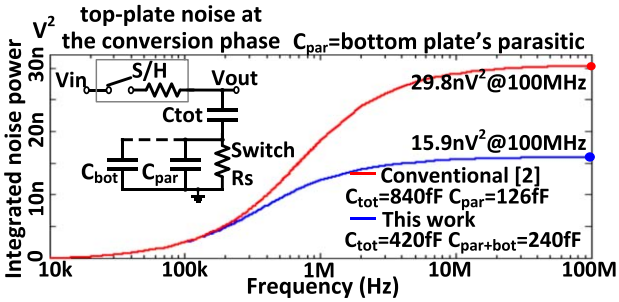



Fig. 13. Integrated noise power with the additional bottom-plate filtering capacitor insertion.

For a DAC matching dominated ADC design, a 4× capacitance increase of the DAC results in a 1-bit performance enhancement of the ADC. With the proposed SR switching technique, the unit capacitor of each sub-ADC can be reduced to 1/4 (0.25× size) to achieve the same matching performance, compared to the VCM-based switching procedure. Therefore, even with two sub-DACs, the overall input loading of the SR switching procedure and the corresponding power requirement of the input driver are all reduced by half. The chosen $C_{\text{total}}$ for each sub-ADC is 420 fF with a resultant INL error of 0.7 LSB.

From the extracted result, the parasitic capacitance induced by the comparator at the DAC input is 6.5 fF with a gain loss of 1.12% and a resulting SNR degradation of 0.1 dB. Considering the kickback noise which is critical at the small-input decision, the simulated kickback coupling is 0.035 at 1 LSB input. Therefore, although the DAC capacitance is decreased in this paper, the gain loss and kickback issues induced by the comparator are negligible.

To avoid a distortion of the overall transfer curve from the gain mismatch between the two sub-ADCs induced by the parasitic effect, an overall gain loss smaller than 7% is achieved with a careful layout. The MATLAB simulation shows that the degradation of ENOB is smaller than 0.02 bits even with a 10% parasitic mismatch between the two sub-ADCs.

## IV. MEASUREMENT RESULTS

A prototype chip was fabricated in 90-nm CMOS with a core area of 0.0354 mm$^2$ (295 $\mu$m × 120 $\mu$m), as shown in Fig. 14. Fig. 15 shows the static performance of the implemented 11-bit ADC with a 0.3-V supply and 600 kS/s. The DNL and INL are +0.37/−0.63 and +0.72/−0.71 LSB, respectively. The discontinuity of INL at the MSB transition is 0.56 LSB after foreground calibration. Fig. 16 shows the

TABLE II
COMPARISON TABLE WITH THE STATE-OF-THE-ART WORKS

| | H.-Y. Tai ISSCC-14[4] | J.-Y. Lin TCAS-I-15[6] | P. Harpe JSSC-13[12] | L. Chen JSSC-17[22] | M. Ahmadi TVLSI-15[21] | H.-Y. Tai VLSI-12[23] | Y.-J. Chen JSSC-16[10] | This work | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Technology | 40nm | 90nm | 65nm | 65nm | 65nm | 90nm | 90nm | 90nm | | |
| Supply Voltage(V) | 0.45 | 0.3 | 0.6 | 0.7 | 0.5 | 0.35 | 0.4 | **0.26** | **0.3** | **0.34** |
| Ideal input swing | ±Vref | ±Vref | ±Vref | ±Vref | ±Vref | ±Vref | ±Vref | ±2Vref | | |
| Ideal input swing(V) | ±0.45 | ±0.3 | ±0.6 | ±0.7 | ±0.5 | ±0.35 | ±0.4 | **±0.52** | **±0.6** | **±0.68** |
| Sample rate (kS/s) | 200 | 90 | 40 | 100 | 250 | 100 | 250 | **300** | **600** | **600** |
| Resolution (bit) | 10 | 10 | 12 | 11 | 10 | 10 | 10 | 11 | | |
| DNL (LSB) | 0.44 | 0.38 | 0.97 | N/A | 0.36 | 0.3 | 0.43 | 0.63 | | |
| INL (LSB) | 0.45 | 0.66 | 1.9 | 1.57 | 0.47 | 0.6 | 0.67 | 0.72 | | |
| Power (nW) | 84 | 35 | 97 | 645 | 290 | 170 | 200 | **90.2** | **187** | **238** |
| ENOB (bit) | 8.95 | 8.38 | 10.1 | 10.5 | 8.45 | 9.06 | 8.63 | **9.25** | **9.46** | **9.75** |
| FoM (fJ/c.-s.) | 0.85 | 1.17 | 2.2 | 4.5 | 3.3 | 3.2 | 2.02 | **0.49** | **0.44** | **0.46** |
| Active Area ($mm^2$) | 0.0065 | 0.031 | 0.076 | 0.03 | 0.072 | 0.032 | 0.04 | 0.035 | | |

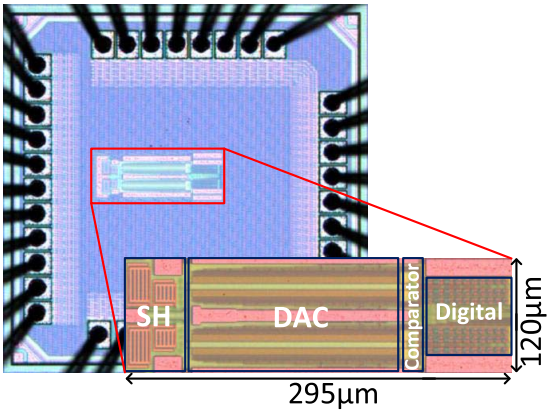



Fig. 14. Chip micrograph.

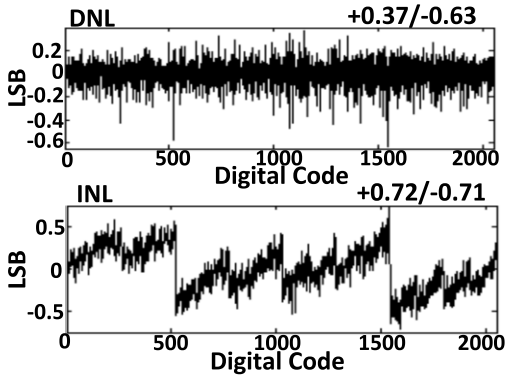



Fig. 15. Measured static performance.

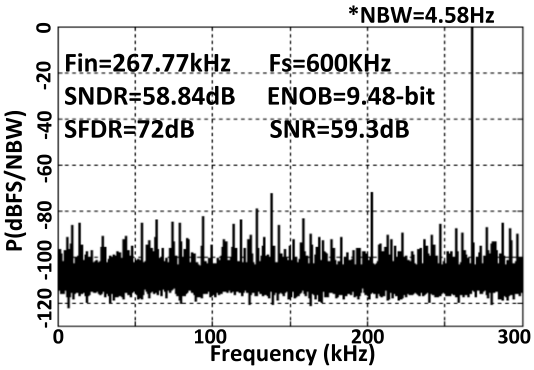



Fig. 16. Measured four-time averaged 131072-bin fast Fourier transform plot.

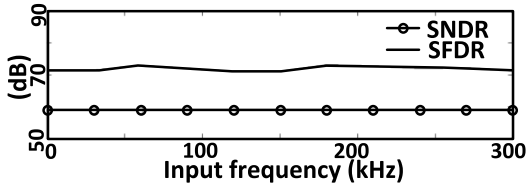



Fig. 17. SNDR and SFDR versus input frequency.

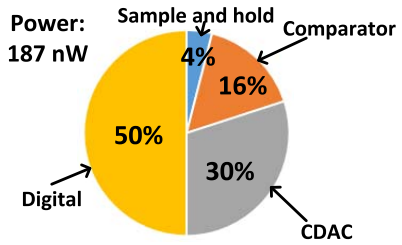



Fig. 18. Measured power dissipation and distribution.

measured dynamic performance with Nyquist-rate inputs. With a Nyquist-rate input (267.77 kHz), the measured SNR, signal-to-noise and distortion ratio (SNDR), spurious-free dynamic range (SFDR), and ENOB are 59.3 dB, 58.84 dB, 72 dB, and 9.48 bits, respectively. The achieved ENOB performance is limited by the designed comparator noise, which is intentionally over budget (for an 11-bit ADC), considering the power efficiency. The post-layout simulation result of the comparator input-referred noise and kT/C noise are 0.746 and 0.257 LSB, respectively. By putting all these non-ideal effects together into the MATLAB simulation (an 11-bit ADC behavior model with SR), the resultant ENOB is 9.59 bits which almost matches the measurement result. The input-referred noise of the comparator is optimized, based on the design consideration of best power efficiency. The ENOB performance can be further improved at a cost of dramatically increasing the power consumption of the comparator, which is not efficient. Fig. 17 shows the stable SNDR and SFDR performances versus input frequency at a 600 kS/s sample rate. Fig. 18 shows that the measured power consumption is 187 nW with a distribution of 4% for the S/H, 16% for comparator, 30% for DAC, and 50% for digital control. The overall power

consumption is dominated by the digital part due to the reduction of switching energy and comparator power. In terms of digital circuits, to handle the same input swing, the supply voltage, and power consumption are twofold and fourfold smaller, respectively, compared to others works. Therefore, this paper simultaneously achieves the advantages of low digital power and switching energy. Table II shows the performance summary and comparison table. This paper achieves a fast sampling rate of 600 kS/s at a low operational voltage of 0.3 V. With the proposed SR DAC, CI comparator, and corresponding design for low-voltage operation, the implemented 11-bit ADC achieves Walen's FoM [19] of 0.44 fJ/conversion-step and Schreier's FoM [20] of 180.8 dB. With a nominal supply of 0.3 V and a variation of over $\pm 10\%$, the prototype shows a stable power efficiency performance, smaller than 0.5 fJ/conversion-step.

## V. Conclusion

This paper presents a 0.3-V 11-bit 600-kS/s SAR ADC in 90-nm CMOS. With the proposed SR switching procedure, this paper consumes only 6%–13.5% switching energy, compared to the state-of-the-art works. The INL performance is also improved twofold with SR switching and the corresponding foreground calibration. The developed CI comparator consumes only 49% of the power and 66% of the decision time with a threefold front-stage gain boost. The prototype achieves an SNDR of 58.7 dB, an ENOB of 9.46 bits, a power consumption of 187 nW, and a resulting FoM of 0.44 fJ/conversion-step, which is currently the lowest among the state-of-the-art works.

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