

Simultaneously Broadband and Back-Off Efficient mm-Wave PAs: A Multi-Port Network Synthesis Approach

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Abstract—Spectrally efficient operation with high power and high efficiency at deep backoff will be critical for the next generation of millimeter-wave (mm-wave) transmitters for 5G and beyond. In addition, as larger non-contiguous chunks of the mm-wave spectrum open up, dynamic frequency reconfiguration while ensuring high spectral and energy efficiency can become a key toward optimal utilization of spectral resources. In this paper, we present a generalized network synthesis approach that enables simultaneous frequency and back-off reconfigurability in an mm-wave power amplifier (PA) architecture to maintain high-efficiency operation with spectrally efficient codes across a wide frequency range. We show that frequency reconfigurability and back-off enhancement can be treated in a similar fashion with dynamic impedance synthesis. The method is based on the synthesis of a multi-port combiner network that exploits the interaction of mm-wave DAC cells switched asymmetrically to synthesize the optimal impedances across the 2-D space of reconfiguration: frequency and backoff. As a proof of concept, a PA is presented in 0.13- μm SiGe BiCMOS process, which operates across 30–55 GHz with peak P_{sat} of 23.7 dBm at 40 GHz, output collector efficiency η_{out} of 34.5% and 22% at the 0- and -6-dB backoff, respectively. The PA maintains $\eta_{\text{out}} > 16\%$ at -6-dB backoff across the range. Non-constant modulation is demonstrated with data rates up to 4 Gb/s across the frequencies from 30 to 50 GHz.

Index Terms—5G, backoff, broadband, digital power amplifier (PA), Doherty, loadpull, millimeter-wave (mm-wave), outphasing, PA, power combining.

I. INTRODUCTION

MILLIMETER-WAVE (mm-wave) applications are now expected to pervade multiple domains from cellular communication for 5G and beyond, point-to-point links for backhaul and for short-distance ultrafast links, automotive radars, gesture sensing, and localization [1], [2]. Particularly for cellular applications, these systems are expected to operate over multiple disjointed frequency bands between 28–86 GHz and beyond, and with a high peak-to-average power ratio (PAPR) signals such as 64-QAM OFDM with

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PAPR of around 9.6 dB and higher. While such flexible frequency diverse operations can enable robust links particularly for non-line-of-sight channels, this presents extremely challenging requirements on the system architecture and its scalability. It can be understood that the current solution of dedicated frequency specific transmitter/power amplifier (PA) designs with massive MIMO arrays might be possible for very few bands, but this fails to be a scalable and efficient solution when a large number of bands open up requiring massive area overhead. However, such flexible frontend (e.g., the PA) that simultaneously generates high power with high peak and back-off efficiency across an extensive mm-wave range is extremely challenging [3]. There is a well-known tradeoff between output power, peak efficiency, back-off efficiency, and bandwidth of PAs, particularly at mm-wave frequencies. Higher output power typically requires higher impedance transformation ratio that tradeoffs with efficiency of the combiner network [4]. Furthermore, broadband performance typically requires higher order complex networks that also tradeoff with efficiency [5]. On the other hand, classical back-off efficient architectures such as Doherty, employs a frequency-dependent resonant impedance transformation network typically designed at a center frequency. Maintaining high back-off efficiency across a broad range of mm-wave frequencies in an efficient manner can enable a universal frontend for mm-wave applications and can transform system design, but is extremely challenging.

This tradeoff can be visualized in Fig. 1, which shows the efficiency degradation of a classical class AB PA with both frequency and backoff. In both conditions, the efficiency degrades drastically because the optimal impedance condition is only satisfied at the peak power at the center frequency. To extend the range of efficient operation across the frequency axis, typical broadband PA designs attempt to create the optimal loadpull impedances at the PA output for *peak power operation* across the spectral range [Fig. 1(a)]. This is typically done with high-order complex matching networks that are typically very inefficient, particularly for high impedance transformation ratios with lossy passives. This leads to a strong tradeoff between the output power and efficiency. On the other hand, to extend the efficient operation range across the back-off axis, i.e., to enable high back-off efficiency, techniques such as Doherty attempts to create the optimal impedance conditions at peak and single or multiple back-off power levels *at a given frequency* [Fig. 1(b)]. Such techniques can offer improvement at the center frequency, but

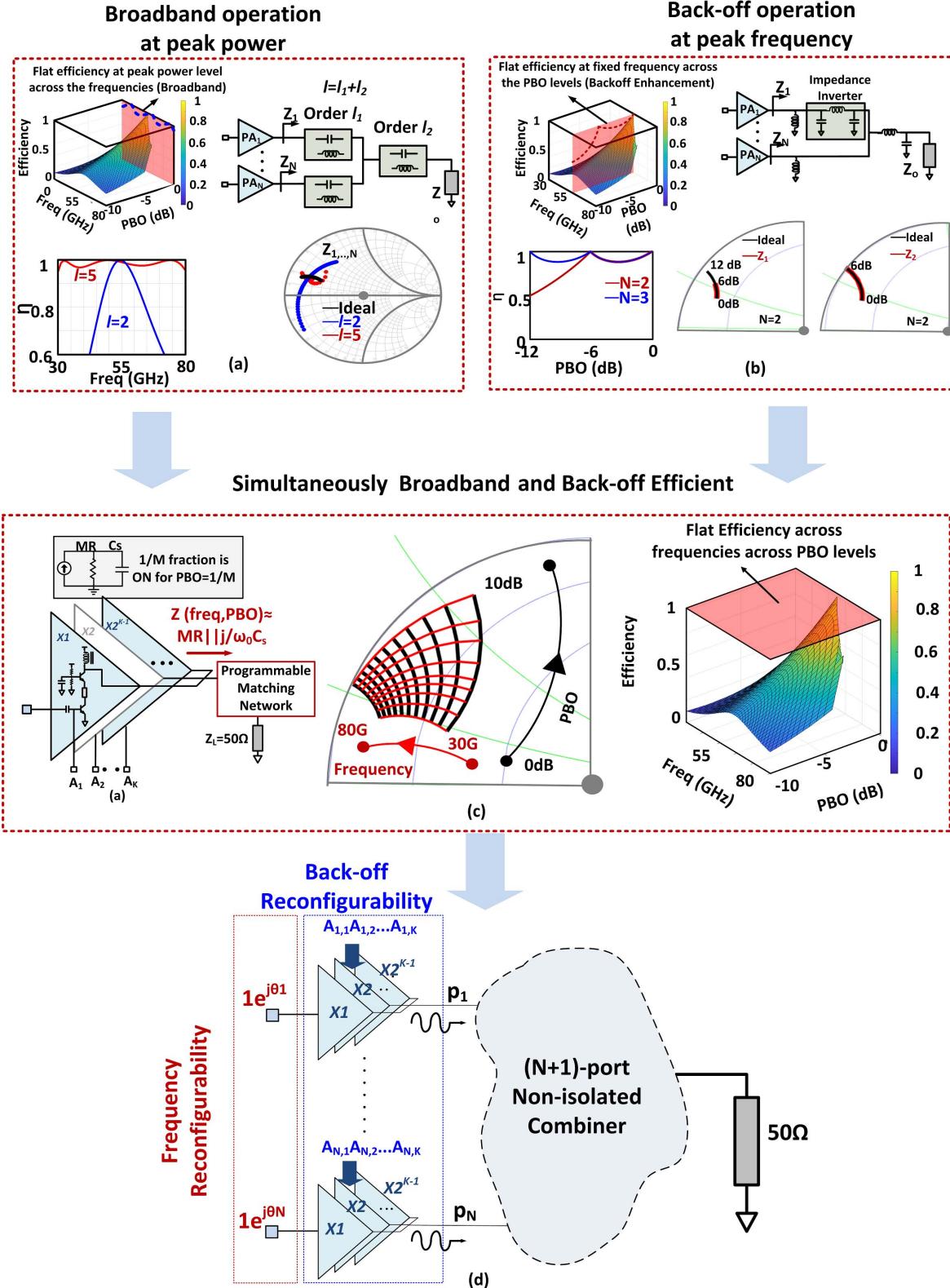


Fig. 1. Optimal impedance of a PA is a function of both output power and frequency (a). Efficiency of a typical class-B PA degrades as we move away from peak power at center frequency. *Broadband operation at P_{sat}* achieved through a higher order network that allows the PA impedance to follow closely to the ideal path on the Smith Chart. This however, trades off with efficiency. (b) *Back-off efficiency enhancement at a given center frequency f_0* achieved through a two-way Doherty. The impedances seen by the PA follows close to the ideal impedance curve until 6 dB-PBO ($N = 2$). (c) Simultaneous frequency and power reconfigurability needs the impedances to follow close to the 2-D space of frequency and PBO. (d) Proposed concept of simultaneous frequency and back-off reconfigurable architecture exploiting mutual interactions of multiple mm-wave DAC cells in a multi-port non-isolated network for 2-D impedance synthesis.

can be inefficient for high output power and performs poorly at a different frequency of operation. Therefore, typically, the classical architectures achieve either frequency reconfigurability at a fixed-peak power level or power back-off (PBO) reconfigurability at a fixed frequency. Our motivation lies in developing a scalable architecture that can enable simultaneously high peak and back-off efficiency across the wide mm-wave frequency range leading towards a programmable transmitter frontend [Fig. 1(c)]. *This paper presents a general framework of exploiting mutual load-pulling in a complex non-isolated network of multiple PA cells that can enable such dual frequency and back-off reconfigurability.* The rest of this paper is organized as follows. Section II presents the prior works and proposes the network synthesis approach for attaining spectrally efficient frequency reconfigurability or dual-frequency back-off reconfigurability. Section III discusses the design and implementation of the PA in the $0.13\text{-}\mu\text{m}$ SiGe BiCMOS process. Section IV presents our measurement results and Section V presents the conclusion.

II. FREQUENCY BACK-OFF DUAL-RECONFIGURABILITY WITH GENERALIZED MULTI-PORT ARCHITECTURES

Prior works on silicon-based PAs at mm-wave frequencies [6]–[32] have demonstrated high efficiency in watt-level range of output power. However, the operable frequency range and back-off efficiency of most of these topologies are still limited by the bandwidth of the output matching network designed for the peak power and center frequency. Impedance tracking to ensure current and voltage saturation and waveform shaping is a key to optimal efficiency operation. For wideband operation at a peak power, this can be ensured with a higher order matching network that can track the optimal impedance path against frequency (1-D). This is shown in the comparison between the second- and fifth-order networks in Fig. 1(a).¹ The synthesis of such wideband networks with ideal passives could be similar to Chebyshev/Butterworth/any other existing methods in [33] and [34]. However, with lossy passives, the efficiency of such networks tradeoffs with the order of the network, especially for high impedance transformation ratio required for high output power. On the other hand, for a *fixed frequency*, the back-off efficiency enhancement techniques try to track the impedance for optimal operation against output power level (1-D), as shown in Fig. 1 (b) [27]–[32], [35]–[37]. Typically, the peak and back-off efficiency, and bandwidth of these architectures tradeoff with output power.

As shown in Fig. 1, the commonality in the reason for efficiency degradation due to impedance mismatch as we deviate from the designed fixed frequency and power level allows us to treat the frequency and back-off reconfigurability in the same fashion. Consider a mm-wave DAC cell with an ideal programmable matching network which, depending on the PBO level ($1/M$) and frequency (ω_0), can synthesize the optimal impedance of $Z_{\text{opt}}(1/M \text{ PBO}, \omega_0) = MR\|j/(j\omega C_s)$

¹The network order shown is of the order l , with order l_1 in each branch and order l_2 after the combined node, $l = l_1 + l_2$.

to ensure simultaneous voltage and current saturation at back-off for optimal operation [Fig. 1(c)]. *Enabling such 2-D dynamic impedance synthesis can result in achieving a flat efficiency across both frequency and backoff, leading to a simultaneous frequency-reconfigurable, energy and spectrally efficient PA.* As shown in Fig. 1(c), the red curves represent the optimal impedances for frequency reconfigurability for various PBO levels across 30–80 GHz, and the black curves correspond to the desired impedances for PBO reconfigurability for various frequencies. This paper presents a method to generate this programmable impedance network through a generalized non-isolated multi-port combiner network synthesis approach among an array of interacting mm-wave DAC cells [38], as shown in Fig. 1(d).

A. Frequency Reconfigurability at Peak Power: Multi-Port Γ -Conjugated Networks and Examples

In our previous work [39], [40], unlike traditional symmetric power combining, we showed that an array of PA cells driven at appropriate phases and interacting through a carefully designed non-isolated asymmetrical combiner network can exploit this controlled interaction to generate the optimal load-pull impedances for an extremely broad range of frequencies. The important point to note is that this can be achieved by employing lower order networks in the combiner enabling high efficiency combining as well. Due to the nature of asymmetry, this synthesizes a quasi-higher order matching network with lower number of passive elements [40]. Unlike a symmetrical network, such generalized asymmetrical network performance is bound by a multi-port (N -port) Bode–Fano limit that is N times that of a symmetric N -port combiner. Therefore, when designed properly, the combiner allows optimal power combination and increases the network order simultaneously, thereby allowing higher power generation across a broad range of frequencies.

While an extensive discussion on how to analytically synthesize the network was presented in [40], we will provide a brief summary of it in this section to show how it can be extended for 2-D reconfigurability for both frequency and backoff. Consider an array of amplifier cells with phase control combining in a non-isolated asymmetrical combiner in Fig. 2(a). We will provide an example of an asymmetrical network and the optimal phase control to generate a broadband performance. Let us consider a simplified example of two-way combined PA with lossless matching network of order two in each branch. Approximately, modeling the PA by the conjugate of the loadpull impedance ($Z_{\text{opt}} = Z_s^*, Z_s = R\|1/j\omega C_s$) as shown in Fig. 2(a), it can be shown that the network needs to satisfy for maximal efficiency [40]

$$\Gamma_1\Gamma_2 - \frac{1 - \Gamma_1}{2} \cdot \frac{1 - \Gamma_2}{2} = 0 \quad (1)$$

where $\Gamma_i = (Z_i - Z_o)/(Z_i + Z_o)$, Z_i is the impedance looking back into each of the branches, and Z_o is the reference impedance [Fig. 2(c)]. To ensure the peak operation of both the PAs, where the amplifiers are sized as $\text{PA}_2 = s\text{PA}_1$, we need

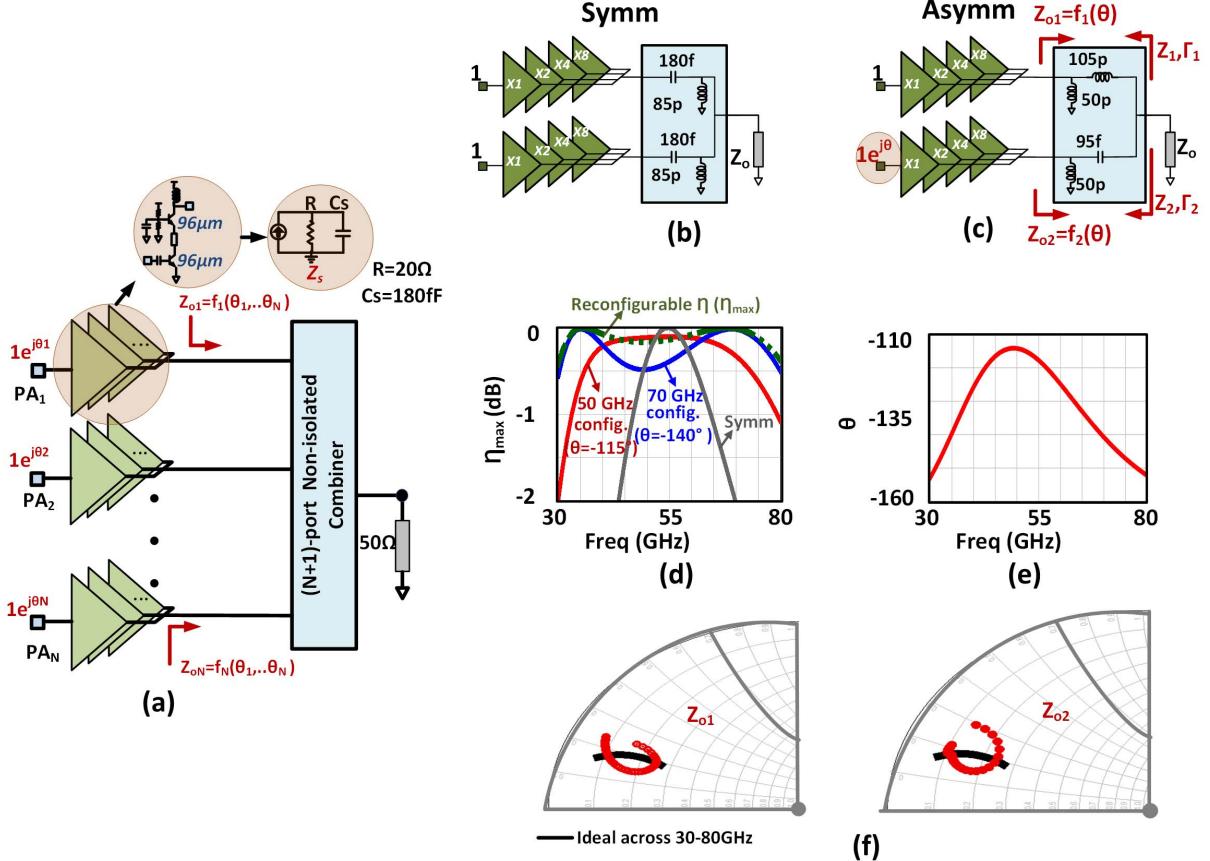


Fig. 2. (a) General PA architecture with N PAs combining through $(N+1)$ -port combiner network. (b) Example two-way symmetrical combiner with matching network of order two in each branch. (c) Example two-way asymmetrical combiner with matching network of order two in each branch. This combiner is the Γ -conjugated network with $\Gamma_2 \approx \Gamma_1^*$ at the center frequency. (d) Efficiency comparison of symmetrical versus asymmetrical along with instantaneous bandwidth for a given phase configuration ($\theta = -115^\circ$ for 40 GHz and $\theta = -140^\circ$ for 70 GHz). (e) Phase offset for optimal asymmetrical combiner two-way. (f) Impedances presented to PA cells for two-way asymmetrical combiner follow the ideal impedances against frequency actively.

to satisfy [40]

$$\frac{1-s}{1+s} = \frac{1}{2} \cdot \frac{(1-|\Gamma_2|^2)(1+\Re(\Gamma_1)) - (1-|\Gamma_1|^2)(1+\Re(\Gamma_2))}{\left|1 - \frac{1-\Gamma_1}{2} \cdot \frac{1-\Gamma_2}{2}\right|^2}. \quad (2)$$

If we consider the PAs to be of same size with $s = 1$, from (2) we get

$$\frac{1 + \Re(\Gamma_1)}{1 - |\Gamma_1|^2} = \frac{1 + \Re(\Gamma_2)}{1 - |\Gamma_2|^2}. \quad (3)$$

Interestingly, $\Gamma_2 = \Gamma_1$ in (3) gives the traditional symmetrical solution; however, the asymmetrical Γ -conjugated solution that satisfies (3) is given as

$$\Gamma_2 = \Gamma_1^*. \quad (4)$$

Substituting the relation (4) in (1), we get

$$|\Gamma_i| = \left| \frac{1 - \Gamma_i}{2} \right|. \quad (5)$$

While there are multiple solutions that exist to achieve the asymmetrical conditions in (4) and (5), an example of a combiner with conjugate matching in each branch (inductor

and capacitor pair) for a two-way combiner with $96\text{-}\mu\text{m}$ -sized-stacked PA cells ($20\Omega \parallel 180\text{ fF}$ at 60 GHz [40]) is shown in Fig. 2(c). As can be seen, the asymmetrical network maintains a reconfigurable η ($>95\%$) across 35–75 GHz compared to sharp narrowband response of the symmetrical case [Fig. 2(b)–(e)]. Given, the $(N+1)$ -port combiner, the optimal phase condition for the available power at the i th port [Fig. 1(d)] can be shown as

$$p_i \propto S_{N+1,i}^*, \quad (6)$$

where the S-parameters are defined with respect to the complex source impedances [40]. The required phase control for attaining the frequency reconfigurability is also shown in Fig. 2(e). This can also be seen in Fig. 2(f) with the impedance paths Z_{o1} and Z_{o2} at the output of the two PA cells following the optimal curve against frequency for the asymmetrical combining network, graphically showing the effectiveness of the impedance synthesis operation. While the driving conditions can be adjusted at each frequency for optimal performance, as can be seen in Fig. 2(d), the optimal phase conditions are not very sensitive to the frequency. Therefore, even if the phase is not adjusted, the performance is very broadband. This figure shows the PA performance

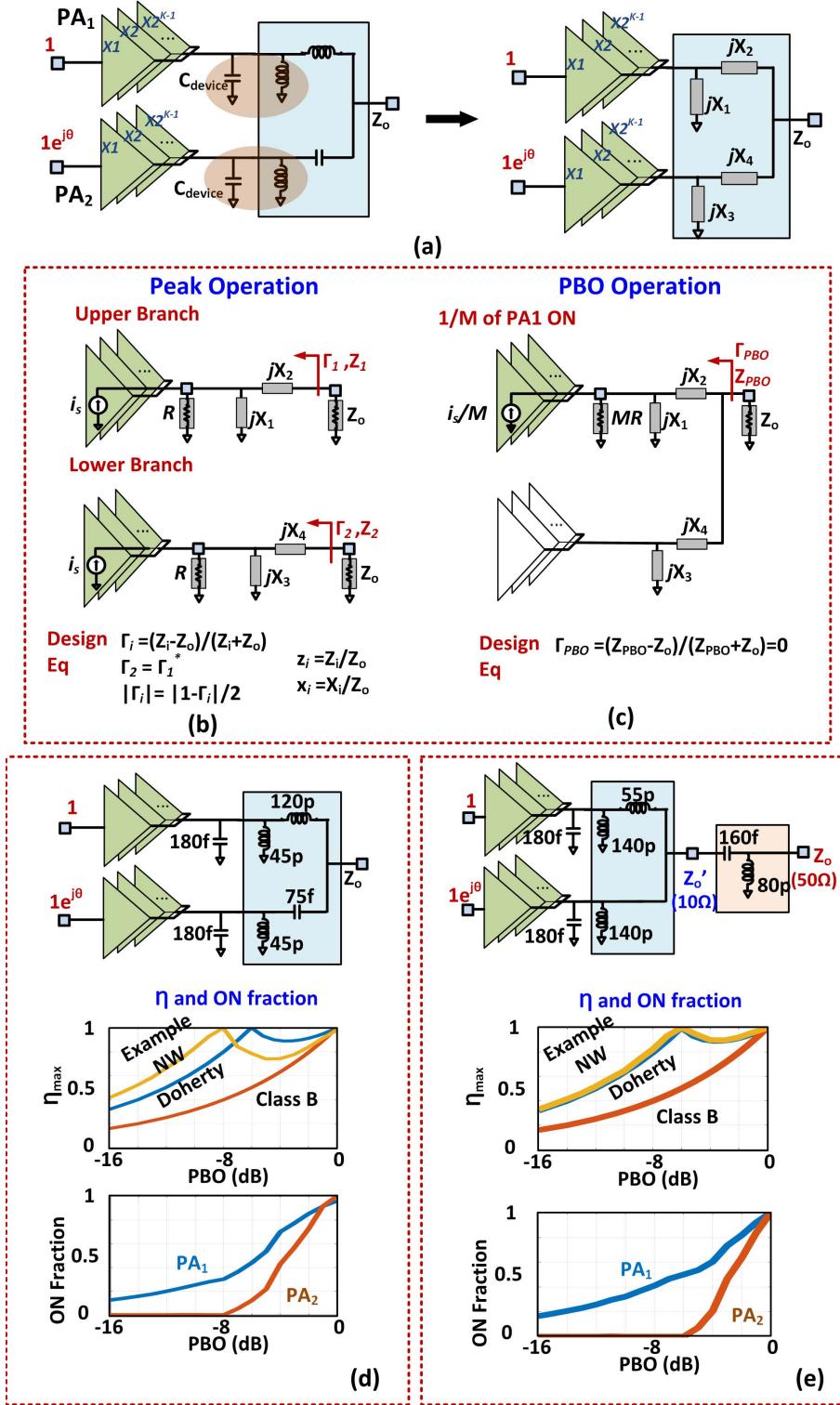


Fig. 3. (a)–(c) Three-port network synthesis approach to back-off reconfigurability with four energy storage elements. Synthesized networks achieve 100% efficiency at peak power level and at the desired PBO level of (d) –8 dB and (e) –6 dB.

against frequency when it is configured for 50- and 70-GHz operations. In both cases, as the phase remains constant, the performance is still very broadband. This quasi-higher order network synthesis along with power combination allows us to loosen the tradeoffs among the output power, efficiency, and frequency range.

B. Back-Off Reconfigurability: Multi-Port Network Synthesis Methodology and Examples

The expressions developed in (1)–(5) will allow us to develop network synthesis examples for back-off reconfigurability too at a *fixed frequency*. As before, there are no unique solutions, but for the ease of analysis and

Synthesizing Networks to tailor PBO levels

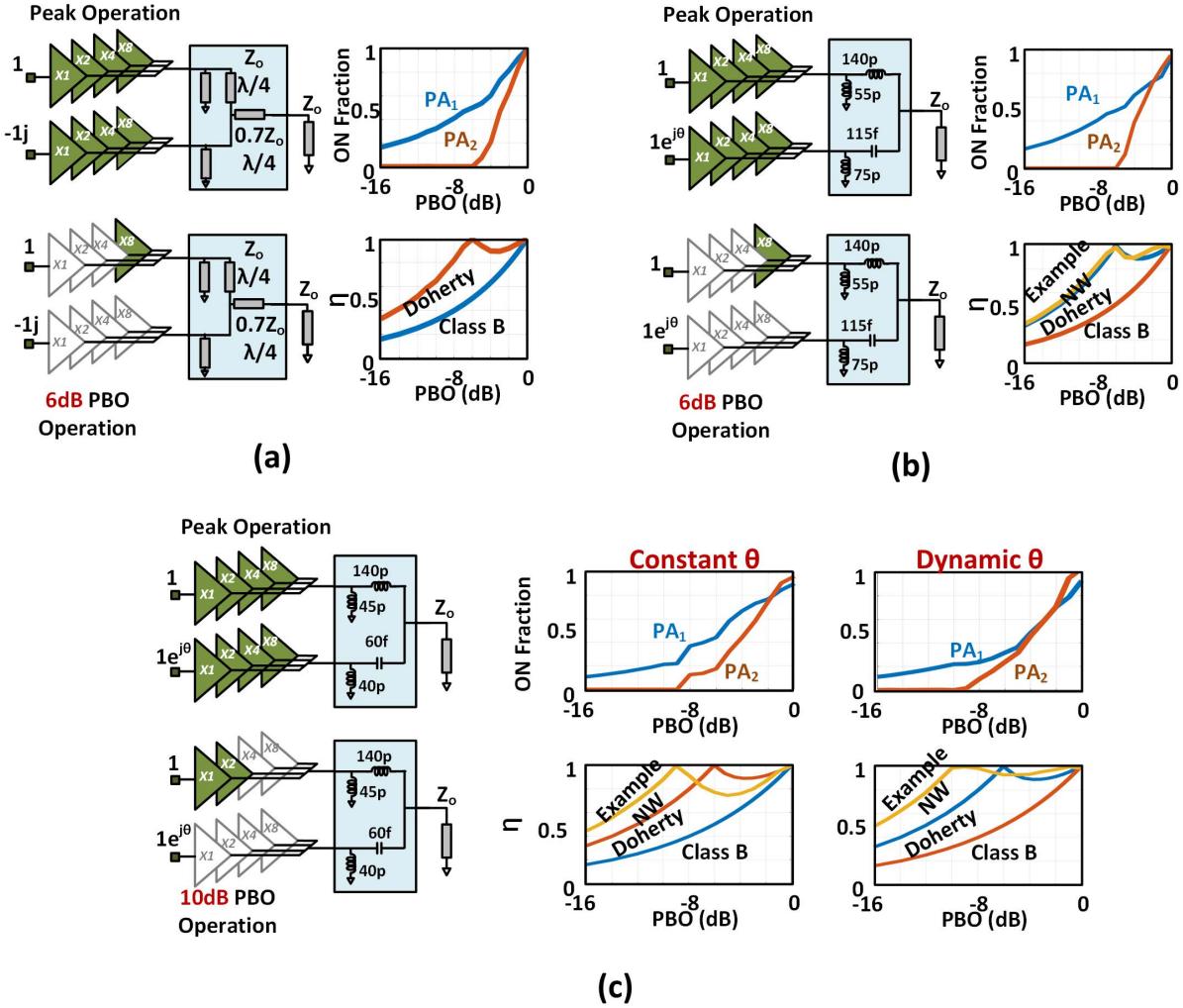


Fig. 4. Back-off reconfigurability architecture synthesis with Γ -conjugated combiner architecture. (a) Doherty network with quarter-wave T-lines. (b) Example lumped network with elements that achieves the performance close to Doherty. (c) Example lumped network designed for enhanced operation up to 10 dB. Addition of dynamic phase control to attain a flat efficiency up to 10 dB.

understanding, we will consider a simplified network with a 2nd-order matching network ($l_1 = 2$, $l_2 = 0$, and $l = 2$) in each branch similar to the previous example that achieved frequency reconfigurability [Fig. 3]. At a given frequency, for the peak operation, expressions (4) and (5) can be solved for the three-port network for optimal efficiency. While at a PBO level of $1/(2M)$, we can consider one of the PAs to be completely shut off, while a fraction $1/M$ of the other PA remains on. This is easy to understand since if each PA delivers $P_{\text{sat}}/2$, then at $1/2M$ back-off level, one possible solution is that one PA is completely off, and $1/M$ of the other PA delivers $P_{\text{sat}}/2M$ when presented with the optimal back-off impedance. This reduces the back-off solution to a two-port network synthesis problem.

1) *Condition (a) (Peak Operation):* As shown in Fig. 3(a) and (b), the output capacitances (C_s) are merged into single reactances (jX_1 and jX_3) at the operation frequency. The two impedances looking back into the

network are Z_1 and Z_2 which can be normalized as $z_1 = Z_1/Z_o = (R/Z_o)\|(jX_1/Z_o) + (jX_2/Z_o) = r\|jx_1 + jx_2$ and $z_2 = Z_2/Z_o = (R/Z_o)\|(jX_3/Z_o) + (jX_4/Z_o) = r\|jx_3 + jx_4$. The peak operation conditions in (4) and (5) are equivalent to

$$z_2 = z_1^* \quad (7)$$

$$|z_{1,2} - 1| = 1. \quad (8)$$

Solving for the real and imaginary parts of (7), we can derive

$$x_1 = x_3 \quad (9)$$

$$x_4 = -x_2 - \frac{2r^2x_1}{r^2 + x_1^2}. \quad (10)$$

Equations (8)–(10) give us three equations with four unknown impedances (x_i), which can be solved for peak efficiency.

2) *Condition (b) (Back-Off Operation):* Let us consider a back-off operation case at PBO level of $1/2M$, where we

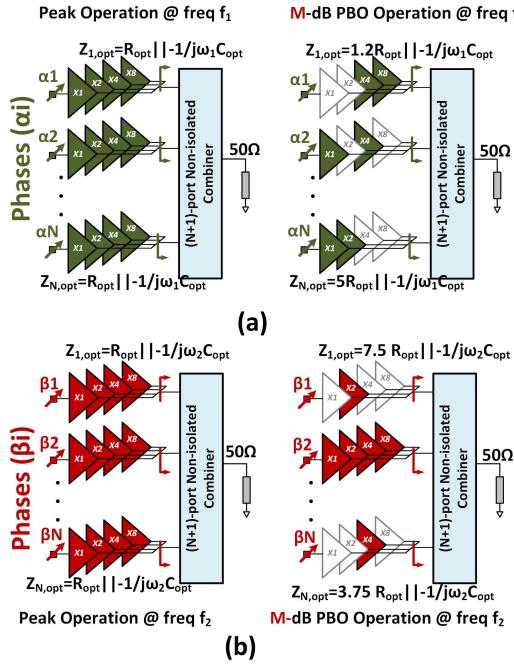


Fig. 5. Concept of dual reconfigurability with asymmetric network and code synthesis approach: peak and PBO operation at frequencies (a) f_1 and (b) f_2 . For the same PBO level (say M dB), the network ensures that there exists different set of codes for different frequencies for efficient operation to enable the dual reconfigurability.

assume that one PA is completely shut off and $1/M$ fraction of the other DAC cell is turned on. Therefore, to ensure optimal efficiency operation, the DAC cell needs to see an output impedance of $MR \parallel j/(\omega C_s)$. This reduces to a two-port network synthesis problem that satisfies

$$\Gamma_{PBO} = 0, \quad Z_{PBO} = Z_o. \quad (11)$$

From Fig. 3(c), $Z_{PBO} = (MR \parallel jX_1 + jX_2) \parallel (jX_3 + jX_4)$. Putting this in (11), we get

$$\frac{1}{MR \parallel jx_1 + jx_2} + \frac{1}{jx_3 + jx_4} = 1. \quad (12)$$

3) Numerical Examples—Example 1: The expressions in (8)–(10), (12) give us five real equations with five variables (four impedances x_i and back-off level M). This, therefore, fixes the PBO level at which enhancement occurs. A design example is shown in Fig. 3(a) with double-stacked SiGe PA, where the solution leads to $x_1 = x_3 \approx -2$, $x_2 \approx 0.9$, $x_4 \approx -0.7$, and $M = 3$ implying optimal back-off level to be approximately 8 dB. The calculated three-port network along with the expected PBO performance is shown in Fig. 3(d). At the expected PBO level of $1/2M = 1/6 \approx -8$ dB, the second PA shuts off while $M = 1/3$ of the first PA remains on for efficient operation as expected. Controlling the exact PBO can be achieved with additional network that transforms Z_0 to Z'_0 which can be solved for, along with the unknown impedances (x_i). An example of such topology for a desired back-off level $PBO = -6$ dB, i.e., $M = 2$ is shown in Fig. 3(e).

4) Numerical Examples—Combiner Optimization for Desired Back-Off Levels: The methodology described allows us to have an analytical approach to lumped network synthesis

for peak and back-off operation at a given frequency. This is very powerful since this allows us to emulate traditional topologies such as classical Doherty [Fig. 4(a)] and multi-level Doherty with analytically derived lumped element networks. In addition, by relaxing the efficiency requirements to greater than 95% at close to the peak power level and given backoff, simple 2nd-order networks can be designed and optimized for various back-off levels (6 and 10 dB) as shown in Fig. 4(b) and (c). All the configurations shown here have the same conjugated network topology as in the broadband asymmetrical design (Fig. 2) but with optimized values of the network parameters.

C. Simultaneous Frequency PBO (Dual) Reconfigurability

The conceptual architecture of a dual-reconfigurable PA architecture is shown in Fig. 5 and consists of an array (N) of mm-wave DACs combining in a generalized non-isolated ($N + 1$)-port network. At the peak operating point, all the combining PA cells are fully on, and the combining cells are driven at the appropriate frequency-dependent static phase configuration as determined by the combiner network [40]. This ensures optimal peak operation across the frequency range, which is similar to the mode of operation as in Fig. 2.

To generate a given PBO level ($P_{PBO} = P_{peak}/\alpha (\alpha > 1) = M - \text{dB}$) at a given frequency f_1 with optimal efficiency, there exists certain set of asymmetric PA codes representing the on-fraction of the DACs, which ensures each of them sees the desired code-dependent optimal impedance. This is shown with the impedance expressions in Fig. 5(a) for operation at backoff. However, to generate the same PBO at a different frequency in the mm-wave range, the network needs to ensure that another combination of the asymmetric switching codes exists for optimal operation of the combining DAC cells at their respective code levels [Fig. 5(b)]. In a two-way combiner PA, this implies that the topology allows two pairs of on-fractions (M_1 and M_2) such that $2/\alpha = 1/M_1 + 1/M_2$ for two different operating frequencies. Therefore, if these conditions were met, the roles of the DAC cells vary across frequency with fine granularity enabling efficient peak as well as back-off operation across a broad mm-wave frequency range. It can be noted that the driving phase conditions at a given frequency do not change with backoff removing the necessity for digital predistortion (DPD) and phase remapping at the input.

The 2-D impedance synthesis in dual-reconfigurable networks are co-synthesized and co-optimized to allow this operation mode. An example of the co-designed network for this dual configurability is shown in Fig. 6. As can be seen, the combiner network follows the simple 2nd-order Γ -conjugated topology with optimized parameter values. When driven with the optimal phase conditions across frequency [Fig. 6(f)], this network allows the synthesis of the asymmetric switching codes to enable an efficient operation against frequency and at backoff simultaneously. This is illustrated in the 3-D plot of efficiency against the dual axes of frequency (30–80 GHz) and backoff (up to –10-dB PBO) in Fig. 6(e). The combiner achieves nearly more than 90%

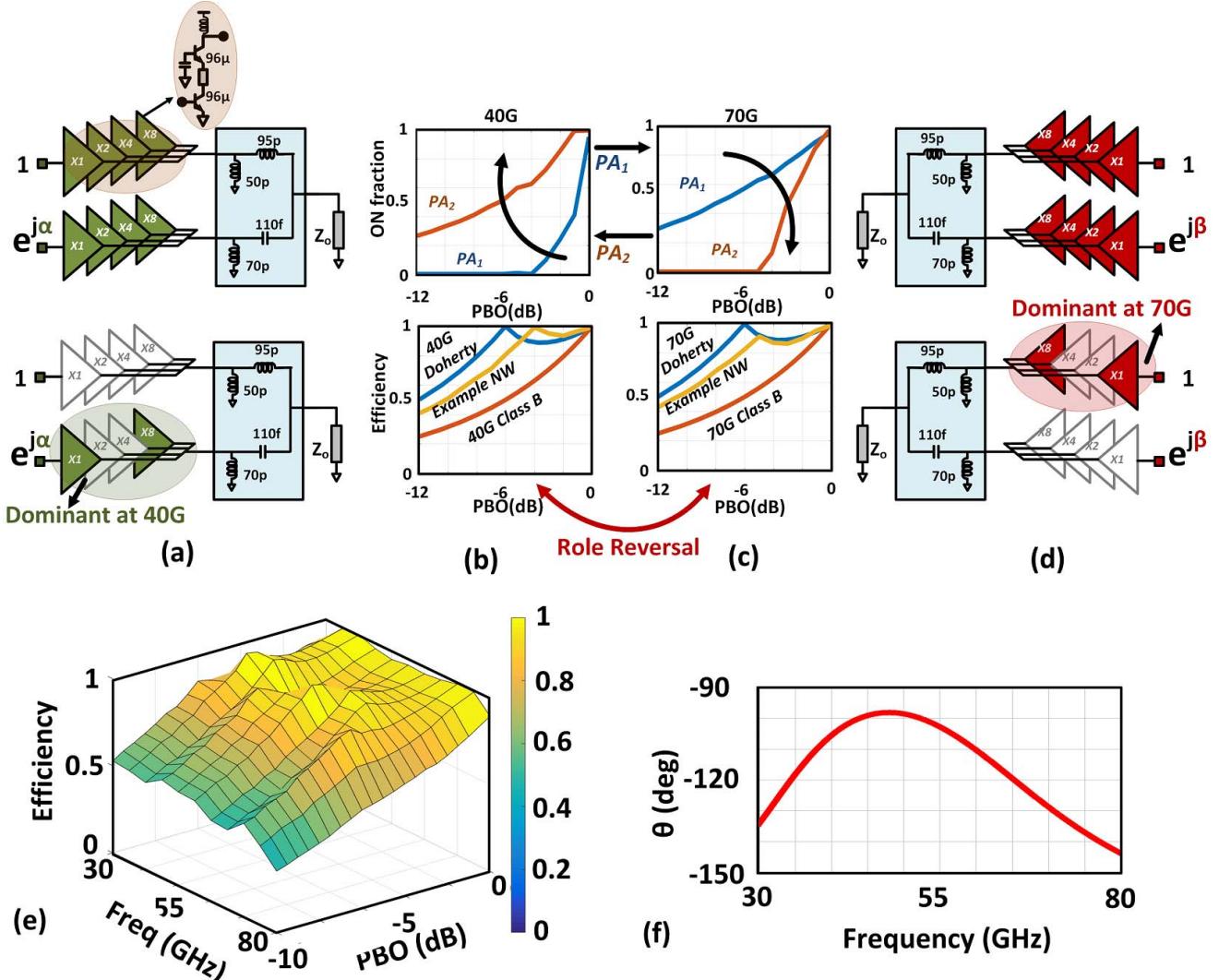


Fig. 6. Simultaneous frequency and back-off reconfigurability in a two-way combiner. Example (a) and (b) operation across PBO levels at 40 GHz and (c) and (d) operation across PBO levels at 70 GHz. (e) 3-D efficiency plot across frequency-PBO axes. (f) Optimal phase drive across the frequency. (a)–(d) show that the roles of the combining PAs switch across PBO levels across frequencies.

efficiency with a static phase control in one branch with high efficiency upto 50% at 10-dB backoff across the entire range.

The frequency-dependent switching codes are illustrated in Fig. 6(a)–(d). At the lower portion of the frequency range (at 40 GHz), for efficiency enhancement at deep PBO levels, PA₁ shuts off completely and PA₂ acts like a main PA ($1/M_1 = 0$, $1/\alpha = 1/2M_2$) as shown in Fig. 6(a) and (b). However, at the higher frequency end (at 70 GHz), the roles of these PAs switch and PA₁ now acts like a main PA for efficiency enhancement at deep PBO levels ($1/M_2 = 0$, $1/\alpha = 1/2M_1$), while PA₂ shuts off as shown in Fig. 6(c) and (d). This role reversal maintains a PBO performance almost similar to Doherty across a broad frequency range. Functionally, this emulates an array of mm-wave switchable narrowband Dohertylike PAs across wide spectrum. In this topology, this functionality is achieved through a generalized treatment of mutually controlled interactions in an asymmetrical, compact, and low-loss combiner to enable optimal operation across frequency and backoff simultaneously.

D. Comparison With Traditional Architectures

1) *Proposed Architecture Versus Class-B Versus Doherty:* Fig. 7 shows the comparison of the proposed architecture across 40–70 GHz with a class-B topology designed with a 2nd-order symmetrical combiner ($l = 2$) and a Doherty architecture [similar to the one in Fig. 1(b)], both of which are designed at 55 GHz. With lossless passives, the proposed network performs Dohertylike operation at 55 GHz, but the role reversal in the network allows an extremely broadband performance as seen by much higher efficiency at 40 and 70 GHz at backoff compared to the classical Doherty architecture. When losses are considered with $Q_{\text{ind}} = Q_{\text{cap}} = 20$, the simplicity of the proposed network results in higher efficiency ($\approx 70\%$ at 55 GHz) even at the center frequency and performs significantly better across the mm-wave range compared to both class-B and Doherty ($\approx 60\%$ at 55 GHz) as shown in Fig. 7. As shown in the figure, the combiner maintains peak efficiency of 65%–70% at 40 and 70 GHz, while that of the Doherty is 40%–45%. Moreover at

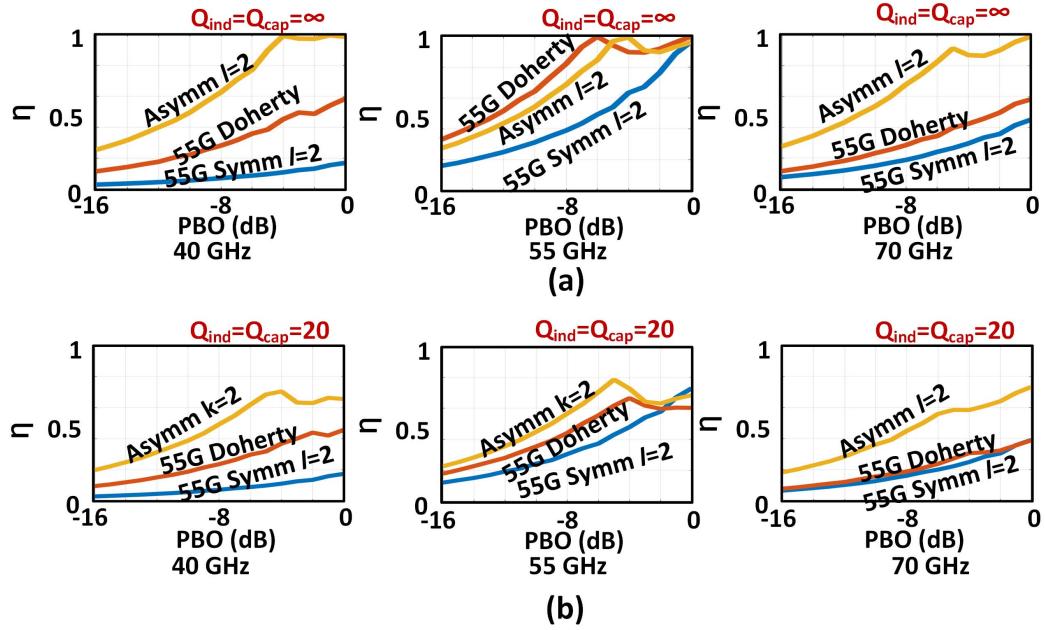


Fig. 7. Comparison of the proposed combiner with symmetrical and Doherty (both designed at 55 GHz) with (a) lossless passives and (b) lossy passives.

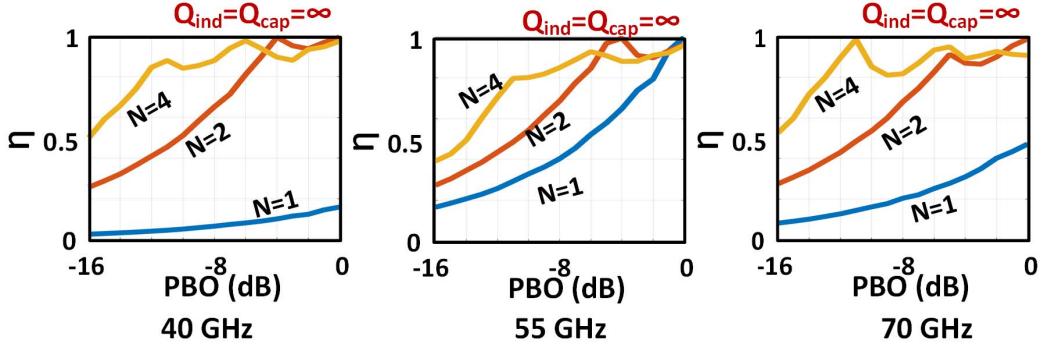


Fig. 8. Performance of the proposed architecture with the number of combining stages (N).

the PBO level of 6 dB, the designed asymmetrical combiner achieves 65% and 55% while the custom Doherty achieves 30% and 25%, respectively, at 40 and 70 GHz (Fig. 7).

2) *Versus Number of Stages*: With an increase in the number of combining stages, network order is increased due to the asymmetry, thus, synthesizing a higher quasi-order matching network. Therefore, for the same power level, this enables a higher bandwidth operation in addition to a larger back-off region as could be seen in Fig. 8.

3) *Versus Process Variations*: Fig. 9 shows the effect of process variations on the proposed structure designed for 30–80 GHz along with the Doherty structure designed at 55 GHz. As could be seen, when process variations are considered, the proposed single combiner performs optimally across the frequencies at the peak power level. We could see that the proposed combiner has the better distribution and higher efficiency across PBO levels of 6 and 9.6 dB even when the finite quality factor passives are considered.

III. mm-WAVE PA DESIGN AND IMPLEMENTATION

A close co-design process between the constituent PA cells and the output combiner is followed for co-optimization of peak power and efficiency across the frequency range. The PA is implemented in a 0.13- μm SiGe BiCMOS process.

A. mm-wave DAC

1) *Choice of the Unit PA Cell*: A double-stacked topology for a PA design has a higher gain, PAE, higher optimum impedance, and hence, higher efficiency matching network when compared with a common-emitter PA cell for the same output power [13], [14]. The optimum intra-stack matching is necessary to pump the maximum power from the bottom transistor to the next upper transistor in the stacked structure. For a wideband performance, the double-stack configuration with inductor/t-line for intra-stack matching is chosen in our design. The PA cells in the output stage are scaled double-

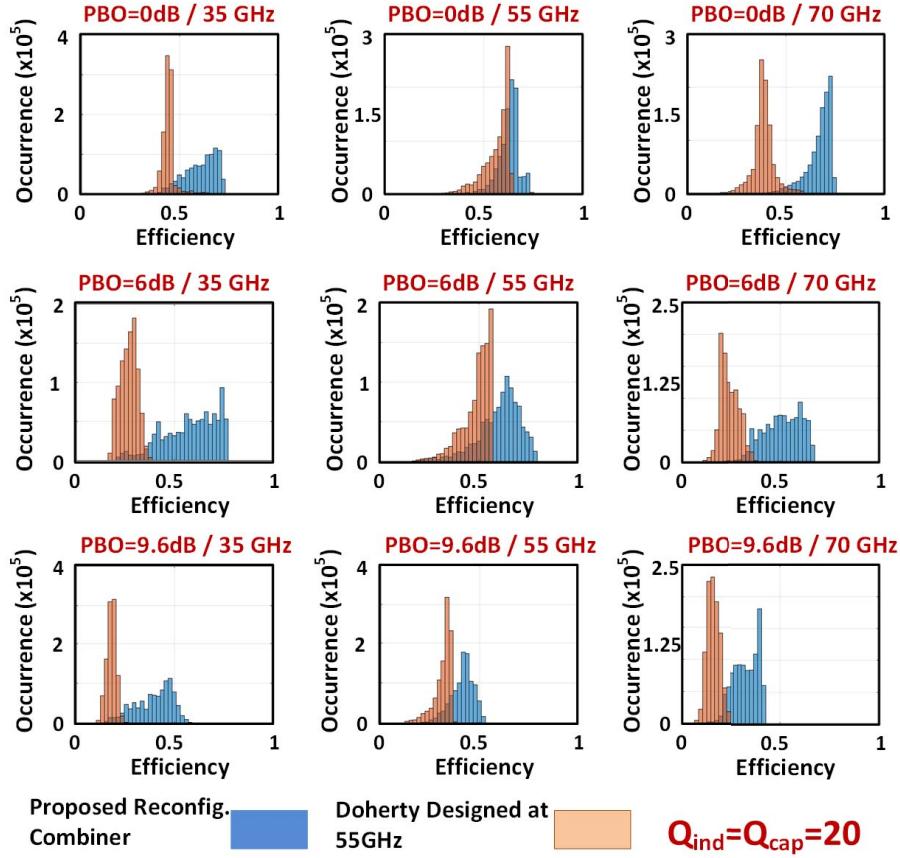


Fig. 9. Performance against process variations. Efficiency distributions of the proposed architecture and Doherty designed at 55 GHz across the range and various PBO levels with passives with $Q = 20$.

stacked PAs with MSB transistors sized $4 \times 12 - \mu\text{m}$ in each branch.

2) *DAC Resolution*: In this architecture, at the deep PBO level, one of the PAs shuts off while other provides the desired power level. For 16-QAM, there are three amplitude levels of the ratio $1:(\sqrt{5}/3):(1/3)$, while the corresponding power ratios are $1:(5/9):(1/9)$. At the deep backoff (corresponding to the lowest power level), one of the PAs shuts off giving $1/2M = 1/9$ or $M = 4.5$. For a 3-bit DAC with an optimal back-off impedance, it is easy to show that the quantization error for the lowest power level $e_{\text{quant,min}} = 13\%$. For a 4-bit DAC, this can be evaluated to be ≈ 0 . In addition, we also take into account the effect of this across the frequency range of operation and the non-idealities of optimal matching. While the DPD technique could enhance system performance, as a proof of concept, we avoid DPD and the associated complexity with a 4-bit structure.

Each of these PA cells is a 4-bit binary-weighted mm-wave-stacked DAC. These main stage PA cells operate from 4-V supply. The capacitors used for intra-stack matching at the base of the stacked transistor are absorbed in the parasitics in both the branches for all the digital bits. The design and layout of the output MSB stage and the 4-bit mm-wave DAC output stage are shown in Fig. 10. The figure shows the simulated waveforms that are showing the alignment of the voltage swings of the lower and upper stack transistors for the optimal power generation across 30–60 GHz. The figure also

shows the simulated output power of the various cells in the DAC that shows the ratioed power generation.

B. Combiner Design

The combiner in this paper was designed following the methodology described in Section II-C to ensure that the PAs operate close to peak efficiency and across the PBO throughout the frequency range. Fig. 11 shows the details of the combiner and the output stage. The combiner is realized with shielded micro-strip transmission lines with the top Al metal layer of $4 \mu\text{m}$ thickness and with MIM-caps. As can be seen, the combiner follows the Γ -conjugated network topology with the elements being realized with t-lines. Fig. 11 shows the simulated performance of the output PA stage with the combiner across the frequencies 30–60 GHz for few sets of digital codes.

C. Complete PA Architecture

The complete schematic of the proof-of-concept PA is shown in Fig. 11(b). The input signal splits into two branches driving the first 2-bit thermal-coded pre-driver stage that drives the 2-bit driver stage that finally powers the 4-bit main stage. The driver amplifiers are common-emitter stages and operate from a 1.6-V supply. Half the driver cells (sized $4 \times 6 \mu\text{m}$) in each branch drives the MSB main PA, while the other half drives the rest of the output DAC cell in each

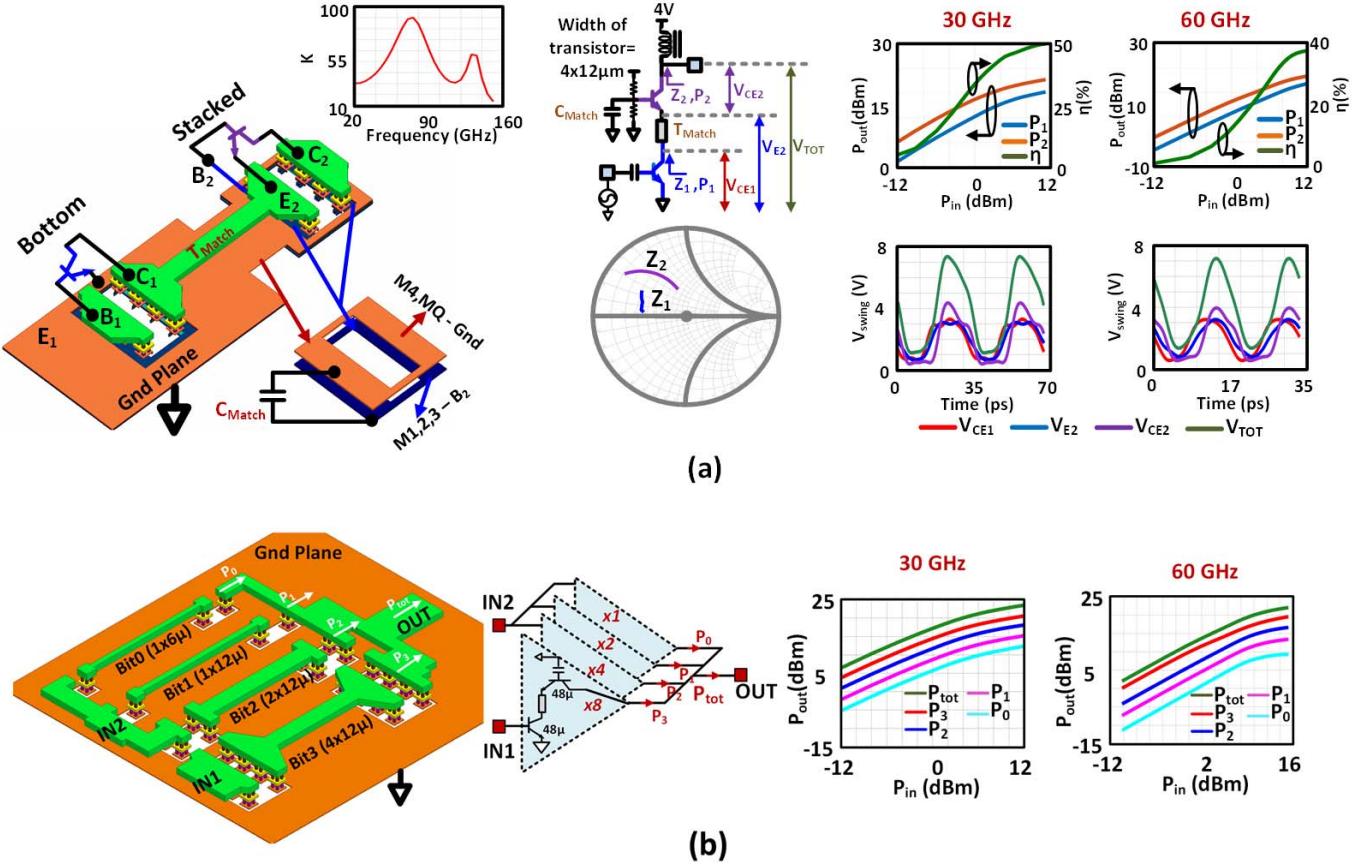


Fig. 10. Layout and simulated performance of (a) MSB mm-wave DAC cell and (b) output 4-bit mm-wave DAC cell.

branch. This allows us to save power in the driver stages by shutting down half the driver stages if less than half of the main PA is turned on (Codes 1–8). Amplitude control is achieved by controlling the digital code of the PA cells for an efficient operation. The optimal phase shift required between the branches varies between $\approx 80^\circ$ and 120° across the frequencies 35–70 GHz. The phase tuning could be achieved by means of variable delay lines through varactors [40]. Since the varactors are lossy, the losses in the delay line need to be minimized. Therefore, instead of generating the required 80° – 120° phase shift through delay lines, we chose to have a static phase shift of 100° achievable through asymmetrical matching networks as shown in Fig. 11(b) and the variable delay line to account for 20° in each branch. However, in integration with the transmitter system, this phase shift could be achieved at the baseband avoiding the need for the lossy varactors. The inter-stage matching networks are designed to have wideband performance.

IV. MEASUREMENT RESULTS

The PA is implemented in the 0.13- μm SiGe BiCMOS process with reported peak f_t/f_{\max} of 220/280 GHz for the transistors with the lowest metal contacts. The microphotograph of the chip is shown in Fig. 11(b) and the chip measures $1.95 \times 0.95 \text{ mm}^2$. The main stage PA cells operate from 4-V supply while the driver cells operate from 1.6-V supply.

A. Continuous-Wave Measurement

The PA was characterized for the large-signal measurement across 30–60 GHz where the PA is reconfigured at each frequency through phase control. This is achieved by configuring the variable delay line with the varactor control between 0 and 2 V. The measurement setup is shown in Fig. 12(a). The input is fed from Agilent N5183A signal generator either directly to the chip (for 30–40 GHz) or through Norden-millimeter N14-4650 (frequency quadrupler) for input beyond 40 GHz. The output power is read through Agilent E4416A power meter through either the power sensor N8487A (upto 50 GHz) or V8486A (50–75 GHz). The measured output-stage collector efficiency for digital codes across 30–55 GHz is shown in Fig. 12. The plots are all color coded. The blue marked points imply that, PA₂ dominates in the code word, while red point implies that PA₁ dominates in the code word. The black curve corresponds to class AB operation with no digital control. As can be seen, at the peak power, both the PAs are fully on indicating near equal contribution of the output power as expected.

At backoff, there is a noticeable role reversal of the combining PAs across the frequencies. For the lower end of the frequency range below 40 GHz, as can be seen, the drain efficiency is higher when codeword of PA₂ > PA₁ for the same output power. In other words, PA₂ dominates for higher efficiency at deep backoff. As explained in Section II-C, this

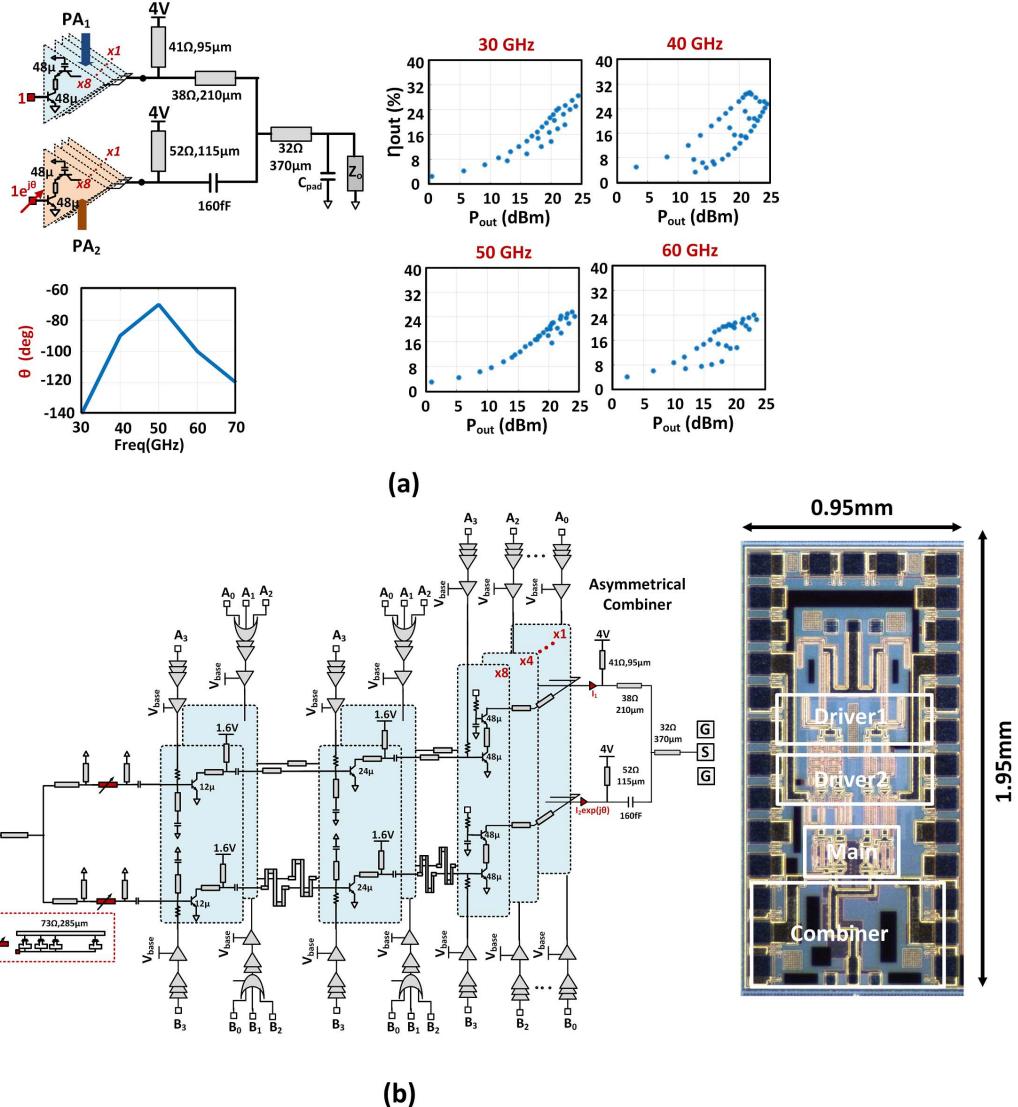


Fig. 11. PA schematic and performance. (a) Simulated performance of the output stage with the combiner across 30–60 GHz for few digital codes. (b) Schematic of the two-port simultaneous broadband and back-off efficient PA and the chip micrograph.

happens because optimal impedances are synthesized when the codeword of PA₂ > PA₁. At 40 GHz, both the PAs contribute near equal amount of power at the backoff. Beyond 40 GHz, the roles switch and PA₁ now dominates at the higher end of spectrum for higher efficiency at deep backoff. Here, the impedances seen by the PA cells are optimum when the codeword of PA₂ < PA₁ is seen. This role reversal of the combining PAs at back-off levels across the frequency is a key toward the dual-reconfigurable operation. An efficiency enhancement of upto 2.2× over the class AB operation is measured for 6-dB PBO and up to 2.8× is measured for ≈9-dB PBO when compared with class-AB operation.

The measured output power (P_{out}), output collector efficiency (η_{out}), and PAE (%) at peak 3, 6, and 9-dB backoff across the frequencies are shown in Fig. 13(a). A peak P_{sat} of 23.7 dBm is measured at 40 GHz with PAE of 28.5% and output collector efficiency (η_{out}) of 34.5%. As shown in the figure, the PA could be actively configured to maintain

$\eta_{\text{out}} > 24\%$ and $\eta_{\text{out}} > 16\%$ at peak power level and 6-dB PBO, respectively, across 30–55 GHz. The figure also shows PAE of the digital PA when compared to a class-AB operation for various back-off levels. Even up to 9-dB backoff when the input power P_{in} is constant, the digital PA shows a significant efficiency enhancement.

B. Modulation Measurement

The measurement setup for measuring the PA performance with non-constant envelope modulations is shown in Fig. 14(a). The phase modulated IF at 2–4 GHz from a 65-GS/s Keysight M8195A arbitrary waveform generator is up-converted through an external mixer as an input to the chip. The synchronized amplitude bits are sent dynamically for the non-constant envelope modulation schemes directly into the chip. The output is later down-converted through an identical mixer, then captured by a 20-GHz real-time oscilloscope with

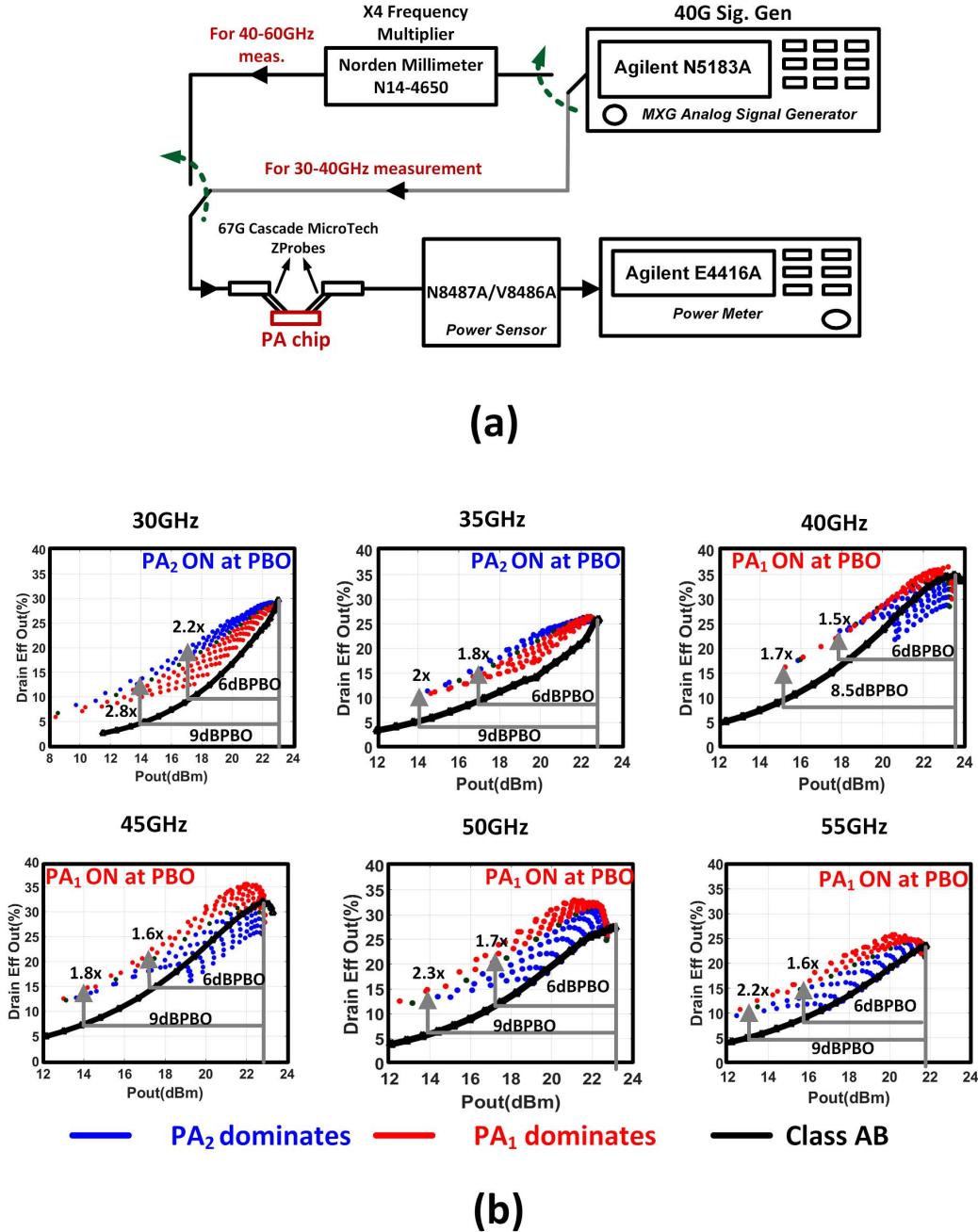


Fig. 12. (a) Measurement setup across 30–60 GHz. (b) Measured performance (output collector efficiency against output power) across all digital codes across 30–55 GHz.

a sampling rate of 80 GS/s, and analyzed through the VSA software on PC. The amplitude bits are time synchronized with on-chip digital buffers. The measured QPSK constellations (PAPR = 0 dB) at carrier frequencies of 30 and 50 GHz are shown in Fig. 14(b). The modulated waveforms have an average measured power of 19.4 and 18.4 dBm, with η_{out} of 22.7% and 25.2% and EVM of -22.5 and -25.1 dB, respectively, at data rate of 2 Gb/s as shown in Fig. 14(b).

In order to enable spectrally efficient 16-QAM constellations (PAPR = 2.6 dB) with the asymmetric switching codes, first the phase rotations at the output due to the different code

settings need to be taken into account. This is done once by sending all the digital codes to the chip, and the output phase rotations are recorded from the oscilloscope. This is illustrated in Fig. 14(c) that shows the phase variations of the different codes at a carrier frequency of 50 GHz. The phase dispersion for most of the codewords is within a cone of $\pm 7^\circ$. The low phase rotation with backoff can be analytically understood from the phase of the combining power waves in the three-port network [Fig. 14(d)]. For the optimal peak operation, the PA cells are driven according to $\angle(p_2/p_1) = \angle(S_{32}/S_{31})^*$ [40], which can be simplified to show $S_{31}p_1 = k_1 e^{j\psi}$,

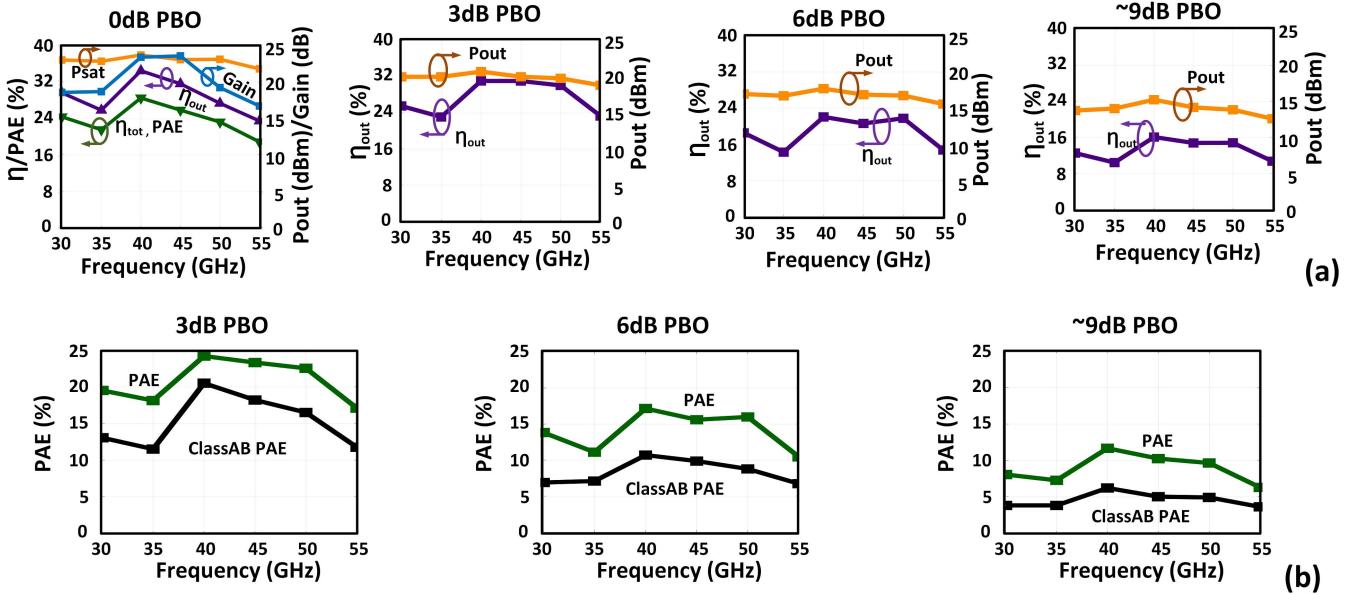


Fig. 13. (a) Measured P_{sat} , η_{out} at PBO levels of 0, 3, 6, and 9 dB across 30–55 GHz. (b) Measured PAE for the digital PA compared to class-AB operation showing significant improvement even at higher back-off levels.

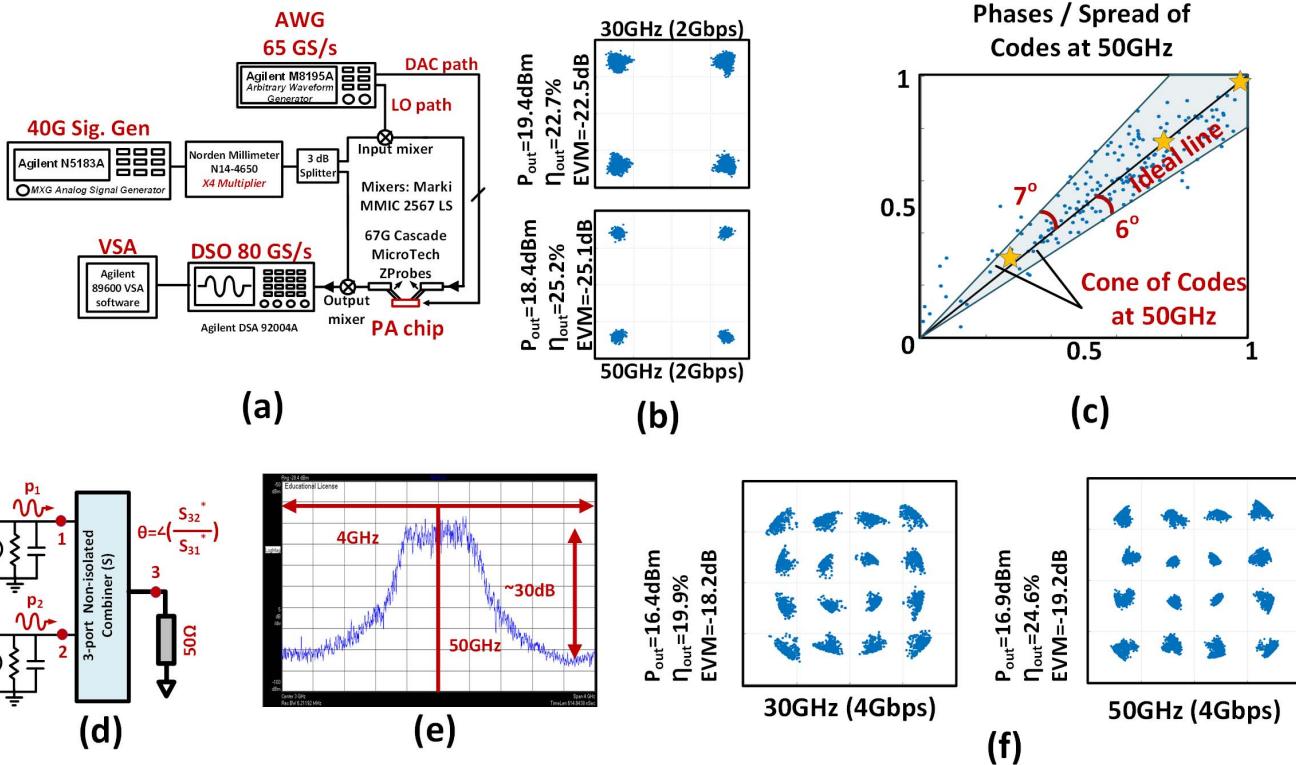


Fig. 14. Modulation measurement. (a) Measurement setup at 50 GHz. (b) Measured QPSK at 30 and 50 GHz. (c) Cone containing all the digital codes at 50 GHz showing a phase dispersion of < 7°. (d) Three-port combiner network. (e) Measured spectrum of 16-QAM at 50 GHz at data rate of 4 Gb/s with ACLR ~ 30 dB. (f) Measured 16-QAM at 30 and 50 GHz.

$S_{32}p_2 = k_2 e^{j\psi}$, where ψ , k_1 , and k_2 are the real constants. Therefore, at peak power, the phase of the output power wave is given by $\angle p_{out,pk} = \angle(S_{31}p_1 + S_{32}p_2) = \psi$. At backoff, when one PA is turned off (i.e., $p_1 = 0$), we still have $\angle p_{out,PBO} = \angle S_{32}p_2 = \psi$. This explains the low phase

rotations between the signals and the back-off levels, since this is already encompassed in the combiner design and the input phase drive.

To avoid any need for phase pre-distortion, the codewords are chosen in such a way that the desired amplitudes fall on

	This Work	ISSCC'16 [39]	RFIC '17 [9]	RFIC '13 [10]	ISSCC '17 [28]	TMTT '16 [25]	JSSC '13 [32]
Frequency of Operation (GHz)	30-55	40-65	29-57	33-46 (PA) / 42.5 (PowerDAC)	26-44	46-50	45
Technology	0.13 μ m SiGe	0.13 μ m SiGe	28nm bulk CMOS	45nm CMOS SOI	0.13 μ m SiGe	45nm CMOS SOI	45nm CMOS SOI
Architecture	Dual Freq-PBO Reconfig. Arch.	Asymmetric Two way combiner	Broadband Series Power Combiner	8way Power Combined/ 3 bit mm-Wave Power DAC	Multiband Doherty	2 Triple Stacked PA	Active phase-shift Doherty
Peak P_{sat} (dBm)	23.7 @40G	23.6 @55G	16.6 @30G	27.2 / 23.4	17.1 @37G	22.4 @46G 20.6 @50G	18
Gain at P_{sat}	23.4 @40G	18.8 @55G	~7* @30G	~12* / ~7.4*	~10* @37G	17.4 @46G 19.5 @50G	8
Peak PAE (%)	28.5 @40G	27.7 @55G	24.2 @30G	10.7 / 6.7	22.6 @37G	42.5 @46G 23.8 @50G	20
Peak η (%)	28.5 @40G 34.5*** @40G	28 @55G 32.7*** @55G	~35* @30G	11.7/8.2	~25.1* @37G 27.6*** @37G	42.5 @46G 23.8 @50G	~24*
Peak η at 6dB back-off (%)	17.5 @40G 22*** @40G	10 @55G 11*** @55G	~10* @30G	5/5.8	~17* @37G 26*** @37G	~18*	~24*
Peak η at 9dB back-off (%)	12 @40G 16.1*** @40G	6 @ 55G 7*** @55G	~5* @ 30G	-/4*	~10.8* @37G 20*** @37G	~10*	~16*
$P_{\text{sat},1\text{dB}}$ Bandwidth (GHz)	20 (30-50G)	25(40-65G)	>22*(26-48G)	>13*(33-46G)	14(28-42G)	>6*(42-48G)	-
PAE,1dB Bandwidth (GHz)	20 (30-50G)	20(40-60G)	~12*(26-38G)	>13*(33-46G)	-	~6*(43-49G)	-
Modulation/ DataRate(Gbps) / P_{out} (dBm) / η_{out} (%)	16QAM/4/16.4/19.9 @30GHz 16QAM/4/16.9/24.6 @50GHz	16QAM/2/ 14.8/- 64QAM/3/12.8 /- @60 GHz	64QAM/6/5.9/>2.3 @34G	-	64QAM/3/9.5/19.2 @37GHz	-	-
Area (mm ²)	1.85 (0.96**)	1.02(0.36**)	0.16**	4.16	1.76	0.28(0.08**)	0.45

*Estimated from the plots. **Active chip Area. ***Output collector efficiency

Fig. 15. Comparison with the state of art mm-wave PAs.

the same line as shown in Fig. 14(c). The measured 16-QAM constellations at carrier frequency of 30 and 50 GHz with average measured power of 16.4 and 16.9 dBm, with η_{out} of 19.9% and 24.6% and EVM of -18.2 dB and -19.2 dB, respectively, at data rate of 4 Gb/s are shown in Fig. 14(f). The measured spectrum in Fig. 14(e) shows that the chip could achieve ACLR of approximately 30 dB. Fig. 15 summarizes the measured performances of the chip and shows the comparison with the recent state-of-art mm-wave PAs in CMOS/SiGe processes. As can be seen, the reported PA maintains high P_{sat} with high efficiency across a dual combination of wide PBO and wide frequency range.

V. CONCLUSION

In this paper, we present a generalized multi-port network synthesis approach for enabling 2-D reconfigurability (simultaneous frequency and back-off reconfigurability) in a PA architecture. The method presents a general treatment of exploiting mutual interactions of an array of mm-wave DACs in an asymmetric mm-wave combiner synthesizing the optimal impedances across the dual-reconfigurability space. As a proof of concept, a silicon-based PA is presented in a 0.13- μ m SiGe BiCMOS process that operates between 30 and 55 GHz. It demonstrates peak P_{sat} of 23.7 dBm at 40 GHz and η_{out} of 34.5% and maintains $\eta_{\text{out}} > 24\%$ at the peak power and $\eta_{\text{out}} > 16\%$ at -6 -dB backoff across the range. The PA is

capable of efficient multi-Gb/s communication with spectrally efficient codes over a wide mm-wave frequency span.

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