

A 50 MHz BW 76.1 dB DR Two-Stage Continuous-Time Delta-Sigma Modulator With VCO Quantizer Nonlinearity Cancellation

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Abstract—A two-stage continuous-time $\Delta\Sigma$ modulator with voltage-controlled oscillator based quantizer (VCOQ) is presented. The presented modulator suppresses the VCOQ voltage-to-frequency nonlinearity through dual path cancellation to achieve high linearity. As an added advantage, this architecture exhibits strong immunity to the first stage quantization error leakage to the output due to gain mismatches between the two stages. Fabricated in a 65 nm CMOS technology, the prototype modulator operates at 1.5 GS/s and achieves 76.1 dB SNR, 73.5 dB SNDR, 88 dB SFDR, and 76.1 dB dynamic range (DR) in 50 MHz bandwidth. This prototype demonstrates robust performance with less than 1.5 dB variation in SNDR for $\pm 10\%$ gain mismatch between the two stages. Also, the SNDR variation remains within 1 dB for a temperature variation of 0°C–80°C. The modulator consumes 51.8 mW of power leading to a Walden FoM of 134 fJ/conv-step.

Index Terms—Continuous time $\Delta\Sigma$ modulators, dynamic element matching, frequency feedback, oversampling converters, two-stage ADCs, VCO-based ADCs, VCO quantizer.

I. INTRODUCTION

IN MODERN wireless standards such as LTE-Advanced, the required ADC bandwidth due to carrier aggregation can be higher than 20 MHz. Also, due to the limited filtering capability of the RF frontend, a high amplitude blocker signal can be present at the ADC input. Therefore, high dynamic range (DR > 70 dB) and wide-bandwidth (BW > 20 MHz) ADCs are essential components in these receivers. Continuous-time (CT) $\Delta\Sigma$ modulators [1], [2] provide implicit anti-alias filtering and excellent power efficiency while achieving more than 70 dB DR with tens of megahertz of bandwidth [3], [4]. However, to achieve a high DR along with a high bandwidth, these modulators are often designed with a third or higher order loop filter along with multibit quantizers and gigahertz (GHz)

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sampling frequencies [5]–[10]. Designing precise analog comparators at GHz sampling frequencies in deep submicron processes is a challenging task. Moreover, mismatch shaping in a multibit feedback DAC requires explicit dynamic element matching (DEM), which introduces additional delay in the feedback path and limits the maximum achievable sampling frequency.

With the development of time-based quantization techniques, voltage-controlled oscillator based quantizers (VCOQs) have become a popular choice for replacing conventional voltage-based multibit quantizers [5], [7], [11]–[17]. When used as a voltage-to-frequency (V-to-F) converter, VCOQs have the desirable properties of high sampling frequency, inherent first-order noise shaping, and implicit DEM [11]. Despite the above advantages, the highly nonlinear V-to-F transfer characteristic of a VCOQ leads to performance degradation. When the VCOQ is used in a $\Delta\Sigma$ modulator, this nonlinearity degrades the distortion performance and limits the achievable SNDR [11]. In order to suppress the distortion, the order of the loop filter has to be increased more than that required for meeting the quantization noise specification, leading to a higher power consumption and stability issues. To overcome this nonlinearity issue, the VCOQ has also been used as a voltage-to-phase converter [5], [12]. Although voltage-to-phase conversion solves the VCOQ nonlinearity problem, it requires an explicit DEM which is one of the major power dissipating blocks at GHz range sampling frequencies. Also, introducing a DEM in the feedback path increases the excess loop delay (ELD) and degrades the stability of the modulator.

In this paper, a two-stage CT $\Delta\Sigma$ modulator with VCOQ is presented. The proposed architecture [18] implements an overall fourth-order noise transfer function (NTF) to achieve a high DR with a low oversampling ratio (OSR). This two-stage architecture offers the benefit of VCOQ nonlinearity cancellation [14], which improves the SFDR when compared with a single-stage fourth-order VCOQ-based $\Delta\Sigma$ modulator with frequency feedback. As an added advantage, this architecture exhibits robust performance against DAC gain mismatches between the two stages. In this modulator, the VCOQs are used with frequency feedback; thus, they benefit from having an implicit DEM. The implicit DEM enables implementation of the modulator with a multibit quantizer and reduced ELD

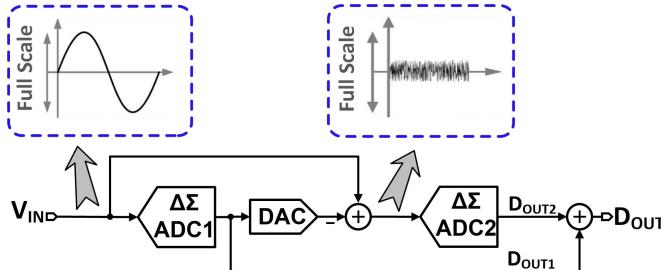


Fig. 1. Block diagram of the proposed VCO-based two-stage CT $\Delta\Sigma$ modulator architecture.

to operate at GHz sampling frequencies. Moreover, the dual return-to-zero (DRZ) DAC [5], [19] makes the modulator immune to data related inter-symbol interference (ISI), which often limits the performance in CT $\Delta\Sigma$ modulators operating at GHz sampling frequencies.

This paper is organized as follows. Section II details the modulator architecture, voltage-controlled oscillator (VCO) nonlinearity cancellation principle, sensitivity analysis highlighting the effect of gain mismatch between the two stages, and design choices for the two stages with MATLAB simulations. Section III describes the circuit design details of the two-stage CT $\Delta\Sigma$ modulator. Section IV presents the measurement results of a prototype ADC fabricated in a 65 nm CMOS process. Section V concludes this paper.

II. MODULATOR ARCHITECTURE

In a $\Delta\Sigma$ modulator with VCOQ, the inability of the $\Delta\Sigma$ loop to completely suppress the VCO nonlinearity is attributed to the large voltage swing at the VCOQ input. The two-stage architecture shown in Fig. 1 provides a solution to reduce the impact of a VCO's V-to-F nonlinearity. Here, the input is fed into the first stage $\Delta\Sigma$ ADC1. Since $\Delta\Sigma$ ADC1 processes the full scale input signal, the output of $\Delta\Sigma$ ADC1 consists of shaped quantization noise and the harmonic components generated due to VCOQ V-to-F nonlinearity. The output of the $\Delta\Sigma$ ADC1 is then subtracted from the input using an inter-stage DAC to generate a residue voltage. This residue voltage consists of the shaped quantization noise and the harmonic components generated by $\Delta\Sigma$ ADC1; thus, the residue voltage is small in amplitude and random in nature as shown in Fig. 1. Since the second stage $\Delta\Sigma$ ADC2 processes this residue signal, the second stage VCOQ does not generate harmonic distortion. The final output is the sum of the outputs from both the stages. In this architecture, the quantization error and VCOQ nonlinearity from the first stage $\Delta\Sigma$ ADC1 are canceled and the final output consists of the input signal and the shaped quantization error from the second stage $\Delta\Sigma$ ADC2 as demonstrated by the following analysis. For this analysis, $\Delta\Sigma$ ADC1 and $\Delta\Sigma$ ADC2 are considered to be discrete-time (DT) modulators with DT representations of the loop transfer function $L(z)$, signal transfer functions (STFs), and the NTFs. By making this assumption, the anti-alias filtering property of a CT implementation is not taken into account. However, the analysis demonstrates the in-band properties of the proposed two-stage modulator.

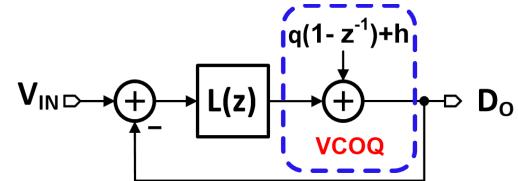


Fig. 2. Block diagram of a $\Delta\Sigma$ modulator with a VCOQ.

The block diagram of a $\Delta\Sigma$ modulator with a VCOQ is shown in Fig. 2. Here, q represents the VCOQ quantization noise and h represents the harmonic component arising from the V-to-F nonlinearity of the VCOQ. The output D_o of the modulator is given by

$$D_o = V_{in}STF + (q(1 - z^{-1}) + h)NTF \quad (1)$$

where $STF = L(z)/(1 + L(z))$ is the signal transfer function and $NTF = 1/(1 + L(z))$ is the noise transfer function of the modulator. As expected, the quantization noise q gets an extra order of noise shaping than the order of the NTF determined by $L(z)$ as shown by (1).

Similarly, for the proposed two-stage modulator as shown in Fig. 1 with VCOQs in both the stages, the output D_{out1} of the first stage is

$$D_{out1} = V_{in}STF_1 + (q_1(1 - z^{-1}) + h)NTF_1 \quad (2)$$

where STF_1 and NTF_1 are the first stage STF and NTF, respectively, q_1 represents the first stage VCOQ quantization noise, and h represents the harmonic component arising from the V-to-F nonlinearity of the first stage VCOQ. Also, the output of the second stage D_{out2} is given by

$$\begin{aligned} D_{out2} = & (V_{in} - V_{in}STF_1)STF_2 \\ & - (q_1(1 - z^{-1}) + h)NTF_1STF_2 \\ & + q_2(1 - z^{-1})NTF_2 \end{aligned} \quad (3)$$

where STF_2 and NTF_2 are the second stage STF and NTF, respectively, and q_2 represents the second stage VCOQ quantization noise. Note that the second stage VCOQ does not contribute to the generation of harmonic distortion. The final output is the sum of the two stages given by

$$\begin{aligned} D_{out} = & V_{in}(STF_1 + STF_2 - STF_1STF_2) \\ & + (q_1(1 - z^{-1}) + h)NTF_1(1 - STF_2) \\ & + q_2(1 - z^{-1})NTF_2. \end{aligned} \quad (4)$$

From (4), we see that $(q_1(1 - z^{-1}) + h)NTF_1$ is scaled by a factor of $(1 - STF_2)$. By design, the in-band $|1 - STF_2|$ is small enough so that the effect of $(q_1(1 - z^{-1}) + h)NTF_1(1 - STF_2)$ can be neglected. Therefore, we can approximate (4) by

$$D_{out} \approx V_{in} + q_2(1 - z^{-1})NTF_2. \quad (5)$$

From (5), it is observed that the final output consists ideally of the input signal and the quantization noise from the second stage shaped by $(1 - z^{-1})NTF_2$. Here the first stage acts as a redundant stage and does not contribute to the noise shaping provided by the overall modulator. The utility of the first stage is to improve the linearity of the overall modulator through

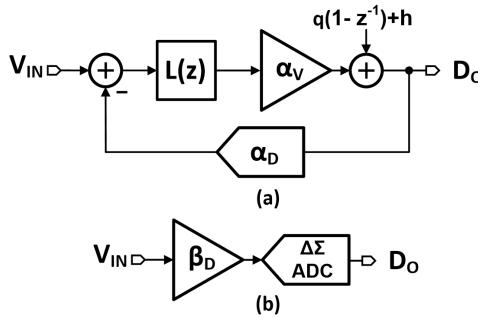


Fig. 3. (a) Block diagram of a VCOQ-based $\Delta\Sigma$ modulator with VCOQ and DAC errors. (b) Equivalent model for the modulator.

harmonic cancellation. Even when highly nonlinear VCOQs are used in both the stages, the two-stage modulator offers improved linearity compared to the standalone second stage with a VCOQ. This is in contrast to multistage $\Delta\Sigma$ modulator architectures like multi-stage noise-shaping (MASH) [1] or Sturdy-MASH (SMASH) [20] $\Delta\Sigma$ modulators. For a MASH $\Delta\Sigma$ modulator, the first stage quantization noise gets canceled at the output and the second stage quantization noise gets shaped by the product of the NTFs of the two stages. For a SMASH $\Delta\Sigma$ modulator, the quantization noise from both the stages gets shaped by the product of the NTFs of the two stages at the output. Thus MASH and SMASH architectures provide effective higher order noise shaping using low-order individual stages. However, both the MASH and the SMASH architectures rely upon the extraction of the quantization error of the first stage quantizer, which is not readily available for a VCOQ. The proposed architecture on the other hand enables the use of a VCOQ in a high-order $\Delta\Sigma$ modulator (second stage) and solves the VCOQ nonlinearity problem by using a redundant first stage without adding extra order of quantization noise shaping. Next, the effects of VCO's V-to-F gain variations and the effects of DAC gain variations on the two-stage architecture are analyzed.

A. Sensitivity Analysis of the Two-Stage Architecture

The block diagram of a $\Delta\Sigma$ modulator with VCOQ is shown again in Fig. 3(a). Here α_V is the VCOQ conversion gain and α_D is the feedback DAC conversion gain. Here, α_V is equal to [13]

$$\alpha_V = \frac{2N K_{VCO}}{F_s} \quad (6)$$

where K_{VCO} denotes the V-to-F gain of the VCO, N is the number of VCO phases, and F_s is the sampling frequency. Because K_{VCO} is very sensitive to process, voltage, and temperature (PVT) variations, it is difficult to ensure a stable value of α_V in practice. Also, α_D depends on the DAC bias current, which is also sensitive to PVT variations.

The output D_o of the modulator is given by

$$D_o = V_{in} \left(\frac{1}{\alpha_D} \right) \frac{\alpha_D \alpha_V L(z)}{1 + \alpha_D \alpha_V L(z)} + \frac{q(1 - z^{-1}) + h}{1 + \alpha_D \alpha_V L(z)} \quad (7)$$

$$D_o = V_{in} \beta_D \text{STF}' + (q(1 - z^{-1}) + h) \text{NTF}' \quad (8)$$

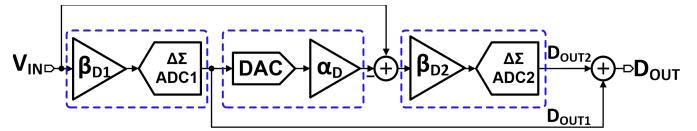


Fig. 4. Block diagram of the proposed two-stage modulator with VCOQ and DAC errors.

where $\text{STF}' = \alpha_D \alpha_V L(z) / (1 + \alpha_D \alpha_V L(z))$ is the modified STF and $\text{NTF}' = 1 / (1 + \alpha_D \alpha_V L(z))$ is the modified NTF of the modulator. Also $\beta_D = (1/\alpha_D)$ is the inverse of the feedback DAC gain. In (7), the product $\alpha_D \alpha_V$ should ideally be equal to unity. From (8), it is observed that a variation in α_D leads to a gain error in the STF' of the modulator. Thus, the $\Delta\Sigma$ modulator can be modeled as shown in Fig. 3(b) in the presence of VCO and DAC gain errors.

Similarly, the proposed two-stage modulator can be modeled as shown in Fig. 4. Here $\beta_{D1} = (1/\alpha_{D1})$ and $\beta_{D2} = (1/\alpha_{D2})$ are the inverse of the feedback DAC gains for $\Delta\Sigma$ ADC1 and $\Delta\Sigma$ ADC2, respectively. Also, α_D is the inter-stage DAC gain. The outputs from the first stage, second stage, and the final combined output are given by (9), (10), and (11), respectively:

$$D_{out1} = V_{in} \beta_{D1} \text{STF}'_1 + (q_1(1 - z^{-1}) + h) \text{NTF}'_1 \quad (9)$$

$$\begin{aligned} D_{out2} = & (V_{in} - V_{in} \beta_{D1} \alpha_D \text{STF}'_1) \beta_{D2} \text{STF}'_2 \\ & - (q_1(1 - z^{-1}) + h) \text{NTF}'_1 \alpha_D \beta_{D2} \text{STF}'_2 \\ & + q_2(1 - z^{-1}) \text{NTF}'_2 \end{aligned} \quad (10)$$

$$\begin{aligned} D_{out} = & V_{in} \beta_{D1} \text{STF}'_1 + q_2(1 - z^{-1}) \text{NTF}'_2 \\ & + V_{in} \beta_{D2} \text{STF}'_2 (1 - \alpha_D \beta_{D1} \text{STF}'_1) \\ & + (q_1(1 - z^{-1}) + h) \text{NTF}'_1 (1 - \alpha_D \beta_{D2} \text{STF}'_2) \end{aligned} \quad (11)$$

where STF'_1 and NTF'_1 are the $\Delta\Sigma$ ADC1 modified STF and NTF, and STF'_2 and NTF'_2 are the $\Delta\Sigma$ ADC2 modified STF and NTF, respectively. Ideally, the product $\alpha_D \beta_{D2} \text{STF}'_2$ should be equal to unity. Under this condition, from (11), the first stage quantization error q_1 gets perfectly canceled at the output. Since $\alpha_D \beta_{D2} = (\alpha_D / \alpha_{D2})$ is the ratio of the gains of the two DACs having the same reference current, this ratio is unity in this architecture. Moreover, this ratio is insensitive to the variation in DAC conversion gains due to PVT variations. Thus, the proposed two-stage architecture shows robust performance across PVT variations and DAC gain variations. Equation (11) reduces to the following:

$$\begin{aligned} D_{out} = & V_{in} \beta_{D1} \text{STF}'_1 + q_2(1 - z^{-1}) \text{NTF}'_2 \\ & + V_{in} \beta_{D2} \text{STF}'_2 (1 - \alpha_D \beta_{D1} \text{STF}'_1) \\ & + (q_1(1 - z^{-1}) + h) \text{NTF}'_1 (1 - \text{STF}'_2). \end{aligned} \quad (12)$$

From (12), to achieve a fourth-order noise shaping from the proposed two-stage modulator, NTF'_2 needs to have a third-order noise shaping. Thus, the second stage needs to have a third-order loop filter and q_2 gets fourth-order noise shaped. Since $\text{NTF}'_2 = 1 - \text{STF}'_2$, from (12), the first stage quantization noise to the final output is given by $q_1(1 - z^{-1}) \text{NTF}'_1 (1 - \text{STF}'_2) = q_1(1 - z^{-1}) \text{NTF}'_1 \text{NTF}'_2$. q_1 must have higher order noise shaping than q_2 so that the in-band quantization noise is determined by q_2 . Thus, NTF'_1 needs to provide at least

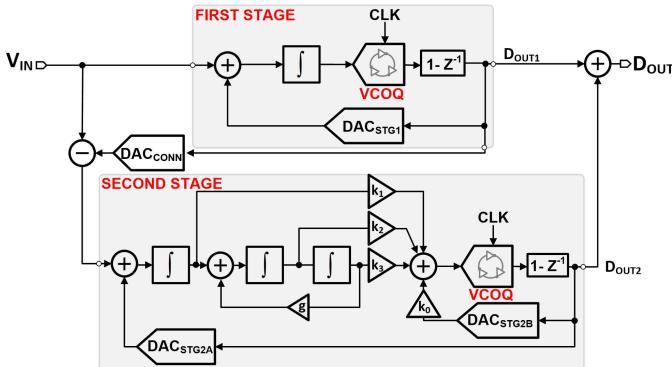


Fig. 5. Block diagram of the proposed two-stage modulator.

first order noise shaping so that q_1 is overall fifth-order noise shaped. For this reason, a first-order loop filter is used for the first stage. NTF₁ and NTF₂ for the two stages are given by (13) and (14), respectively. Note that NTF'₁ = NTF₁ and NTF'₂ = NTF₂ when $\alpha_{D1}\alpha_{V1} = 1$ and $\alpha_{D2}\alpha_{V2} = 1$, respectively

$$\text{NTF}_1 = 1 - z^{-1} \quad (13)$$

$$\text{NTF}_2 = \frac{(1 - z^{-1})(1 - 1.969z^{-1} + z^{-2})}{(1 - 0.664z^{-1})(1 - 1.674z^{-1} + 0.7705z^{-2})}. \quad (14)$$

The proposed two-stage architecture is shown in Fig. 5. The two stages of the modulator are described next.

1) Modulator First Stage: The first stage of the two-stage architecture is a $\Delta\Sigma$ modulator with a first-order loop filter and a 20-level VCOQ. Here, NTF'₁ provides first-order noise shaping. A first-order NTF'₁ ensures that the first stage quantization error has an extra order of noise shaping compared with the noise shaping of the second stage quantization error. Thus, the modulator becomes robust against performance degradation due to the first stage quantization error leakage to the output due to a gain mismatch in the interstage DAC. This is validated in Section II-B through MATLAB behavioral simulations. It is to be noted that an open-loop VCOQ can also be used as the first stage. A two-stage $\Delta\Sigma$ modulator with an open-loop VCOQ in the first stage is discussed in Appendix A. The two-stage $\Delta\Sigma$ modulator with an open-loop VCOQ-based first stage exhibits higher variation of SQNR with DAC gain variations compared with the proposed two-stage modulator. Moreover, by putting the VCOQ in a $\Delta\Sigma$ loop in the first stage, the first stage STF is made independent of the changes in K_{VCO} due to PVT variations as shown in (8).

2) Modulator Second Stage: Since the second stage of the modulator defines the overall modulator performance, a third-order loop filter has been selected for the second stage to achieve more than 13-bit resolution with an OSR of 15 and a 20-level quantizer. This leads to an SNR of 84 dB. The loop filter coefficients of the second stage are calculated using an impulse invariance transformation [21] and tabulated in Table I along with the target specification for the second stage CT $\Delta\Sigma$ modulator.

B. MATLAB Behavioral Simulations

The power spectral density (PSD) of the open-loop VCOQ from a MATLAB simulation is shown in Fig. 6(a). The

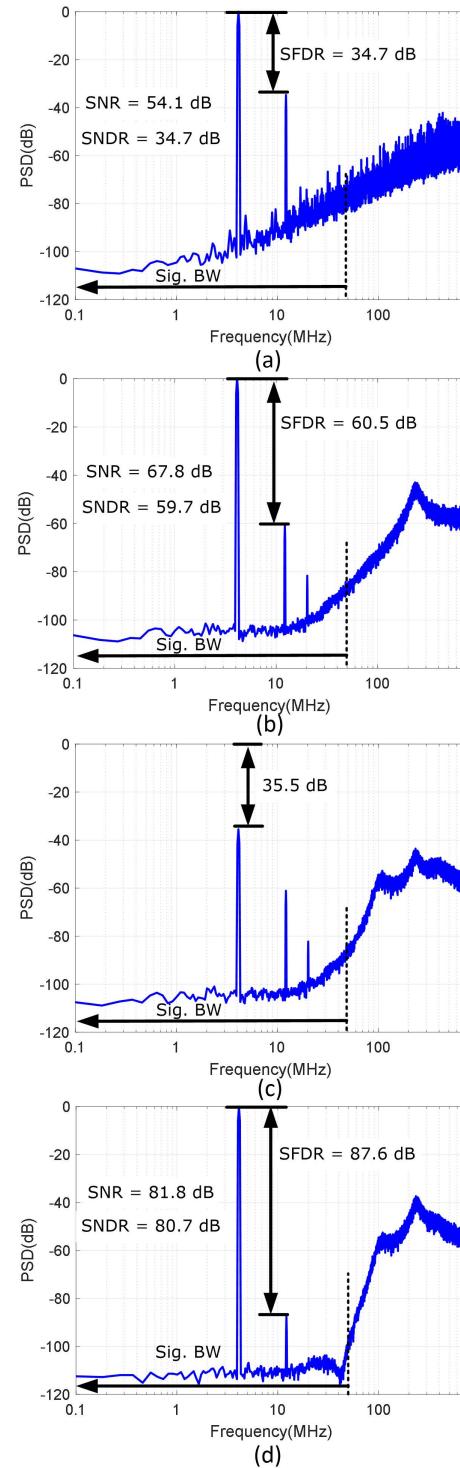


Fig. 6. Simulated PSD for a 4 MHz –3 dBFS input signal for an (a) open-loop VCO. (b) First stage output, (c) second stage output, and (d) final output of the proposed two-stage modulator.

nonlinear coefficients of the pseudo-differential VCO are extracted from Cadence schematic level simulations and incorporated into the MATLAB VCO model. The simulated PSDs of the first stage output, second stage output, and the final combined output for the proposed two-stage modulator are shown in Fig. 6(b)–(d), respectively, for a 4 MHz –3 dBFS

TABLE I
SECOND STAGE $\Delta\Sigma$ MODULATOR SPECIFICATIONS
WITH LOOP FILTER COEFFICIENTS

Second Stage Specifications	Loopfilter Coefficients
Loop-filter Order = 3	$K_0 = 0.805$
NTF Order = 4	$K_1 = 0.24$
OSR = 15	$K_2 = 0.044$
$F_s = 1.5$ GHz	$K_3 = 0.904$
BW = 50 MHz	$g = 0.03$
Quantizer = 20 levels	
ELD = 0.5 Ts	
OBG = 2.5	

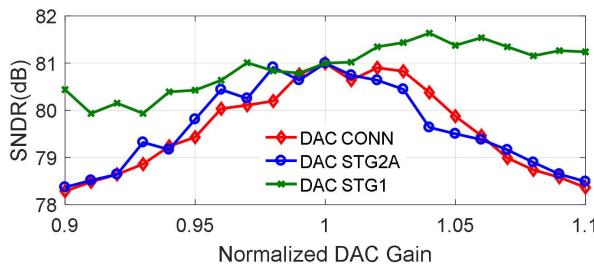


Fig. 7. SNDR versus DAC gain mismatches from the two-stage modulator MATLAB model for a -3 dBFS 4 MHz input signal.

input tone. The two-stage modulator architecture has an 87.6 dB SFDR and a peak SNR/SNDR of 81.8 dB/80.7 dB for a 50 MHz signal bandwidth. The third harmonic component at the first stage output [Fig. 6(b)] due to the VCOQ nonlinearity is suppressed at the final output [Fig. 6(d)] and improves the SFDR by 27.1 dB. Also, from Fig. 6(c), it is observed that the input signal gets attenuated by 35.5 dB at the input to the second stage. This validates the assumption that the residue signal is small in amplitude and random in nature. Thus, the second stage does not contribute to the generation of harmonic distortion.

Next, the robustness of the modulator against the gain mismatch between the two stages is analyzed. The SNDR variation with DAC gain error for the proposed two-stage modulator is shown in Fig. 7. The proposed architecture shows 2.5 dB variation in SNDR for $\pm 10\%$ gain mismatch between the two stages. In comparison, the two-stage architecture in [14] degrades the SNDR by 4.5 dB for the same variation in the DAC gain mismatch. Thus, the proposed architecture with second-order and fourth-order NTF provides improved sensitivity to the DAC gain mismatches over the first-order and second-order NTF-based architecture in [14]. This is further validated through measurements in Section IV.

C. Comparison With a Standalone Fourth-Order Modulator

The proposed two-stage architecture and a standalone fourth-order modulator (second stage is used as an independent modulator) as shown in Fig. 8 are compared through MATLAB simulations. The SNR/SNDR versus the input amplitude for the two modulators is shown in Fig. 9 for a 4 MHz input frequency. It is observed that although the SNR and the DR of the two modulators are identical, the proposed two-stage architecture improves the peak SNDR by 6.2 dB. For a

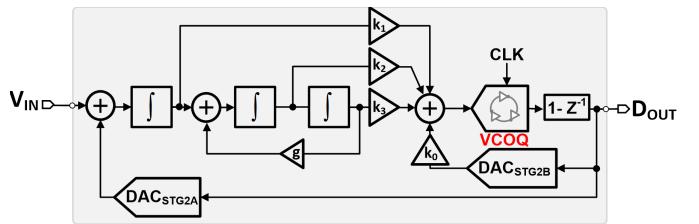


Fig. 8. Block diagram of the standalone fourth-order modulator.

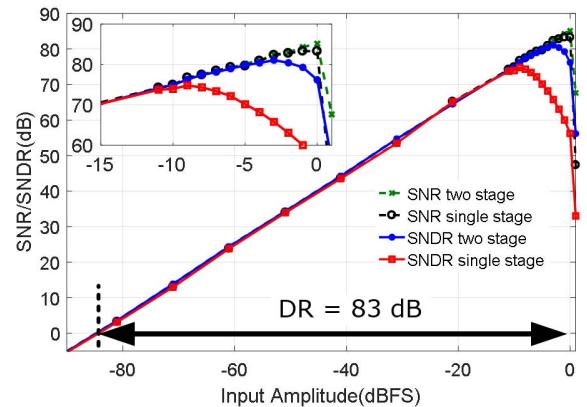


Fig. 9. SNR/SNDR versus input amplitude plot for the proposed two-stage modulator and the standalone fourth-order modulator in Fig. 8 for a 4 MHz input signal.

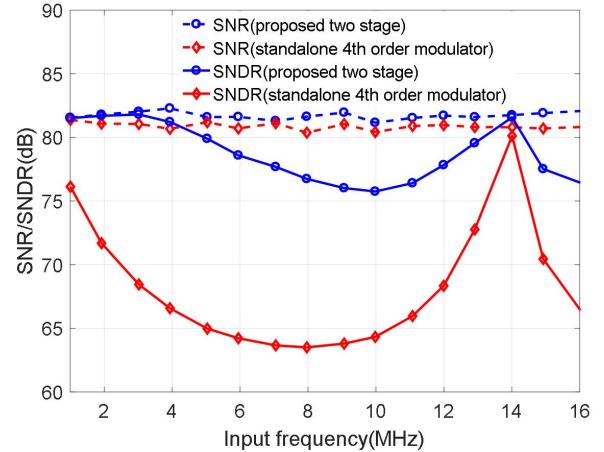


Fig. 10. SNR/SNDR versus input frequency for the proposed two-stage modulator and the standalone fourth-order modulator for a -3 dBFS input amplitude.

-3 dBFS input signal, the SNDR is improved by 15 dB compared with the single-stage modulator in Fig. 8.

The simulated SNR/SNDR with input frequencies in the range from 1 to 16 MHz and -3 dBFS input amplitude is shown in Fig. 10 for the proposed two-stage modulator (blue curve) and the standalone fourth-order modulator (red curve). Since the third-order harmonic distortion is the dominant distortion component due to pseudo-differential VCOQs, the SNR/SNDR is shown for input frequencies up to 16 MHz so that the third harmonic falls in-band (50 MHz bandwidth). It is observed that the proposed two-stage modulator has

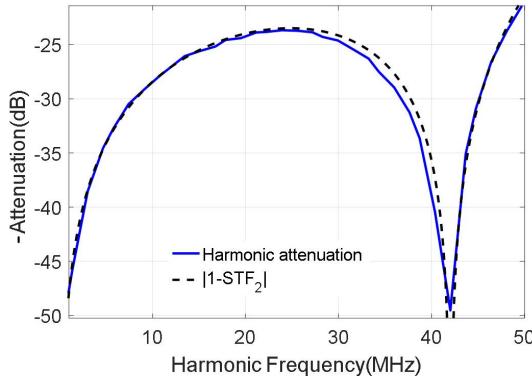


Fig. 11. Maximum attenuation of harmonic component versus harmonic component frequency for the proposed two-stage CT $\Delta \Sigma$ modulator.

less variation in SNDR over the input frequency range when compared with the standalone fourth-order modulator. Another observation here is that the SNDR improves for input frequencies near 14 MHz for both the modulators, which is explained in the next section.

D. Impact of STF₂ on Harmonic Attenuation

In (12), $(q_1(1-z^{-1})+h)\text{NTF}'_1(1-\text{STF}'_2)$ represents the first stage quantization noise and harmonic components leakage to the final output. Here, $(q_1(1-z^{-1})+h)\text{NTF}'_1$, which represents the shaped quantization noise and harmonic components at the first stage output, is scaled by a factor of $(1-\text{STF}'_2)$. $|1-\text{STF}'_2|$ represents the magnitude of $(1-\text{STF}'_2)$ shown by the dotted line in Fig. 11. Also, MATLAB simulation results for maximum possible attenuation of the harmonic components from the first stage for the proposed two-stage CT $\Delta \Sigma$ modulator is shown by the blue solid line across the bandwidth. As expected, with lower magnitude of $(1-\text{STF}'_2)$, the harmonic attenuation increases. The worst case attenuation of the harmonic components by the second stage is 20 dB in the signal bandwidth. Also, the harmonic cancellation improves for harmonic frequencies around 42 MHz. This explains the improved SNDR for input frequencies near 14 MHz (third harmonic component at 42 MHz) as shown by the blue solid line in Fig. 10 for the proposed two-stage modulator.

E. Improving Harmonic Attenuation by Digital Filtering

For the proposed two-stage modulator, adding a digital filter before the final addition as shown in Fig. 12 will improve the harmonic cancellation. This is explained with the help of (12). With the added digital filter at the output of the first stage, (12) gets modified as follows:

$$\begin{aligned} D_{\text{out}} = & V_{\text{in}}\beta_{D1}\text{STF}'_1 H + q_2(1-z^{-1})\text{NTF}'_2 \\ & + V_{\text{in}}\beta_{D2}\text{STF}'_2(1-\alpha_D\beta_{D1}\text{STF}'_1) \\ & + (q_1(1-z^{-1})+h)\text{NTF}'_1(H-\text{STF}'_2). \quad (15) \end{aligned}$$

By selecting $H = \text{STF}'_2$, the term $(q_1(1-z^{-1})+h)\text{NTF}'_1(H-\text{STF}'_2)$ can be canceled out. Thus, the suppression of quantization noise and the harmonic components from the first stage is no longer limited by the attenuation provided by

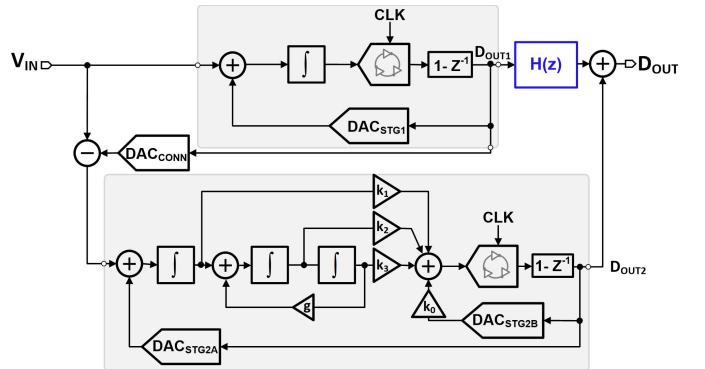


Fig. 12. Block diagram of the modulator with the digital post-processing filter $H(z)$.

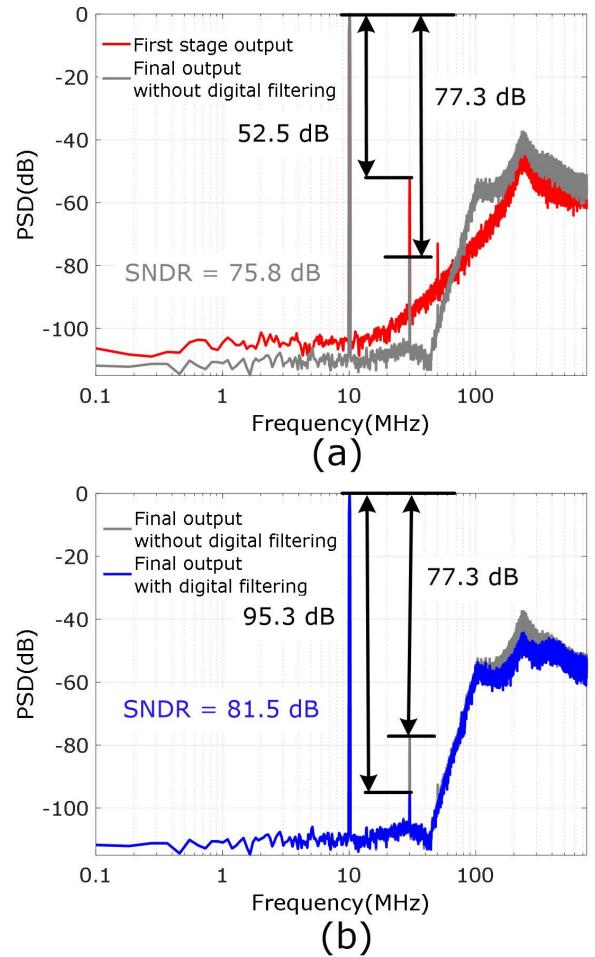


Fig. 13. PSDs for a 10 MHz -3 dBFS input signal for the proposed two-stage modulator (a) without digital filtering and (b) with digital filtering.

$|1-\text{STF}'_2|$ and the cancellation is improved. Here, STF'_2 is the STF of the DT $\Delta \Sigma$ modulator with third-order loop filter from which the loop filter coefficients for the equivalent CT $\Delta \Sigma$ modulator are derived using an impulse invariance transformation. Thus, $H = \text{STF}'_2 = 1 - \text{NTF}'_2$, where NTF'_2 is given by (14) when $\alpha_{D2}\alpha_{V2} = 1$. The MATLAB simulated PSDs with and without digital filtering block $H(z)$ are shown in Fig. 13. For a 10 MHz -3 dBFS input

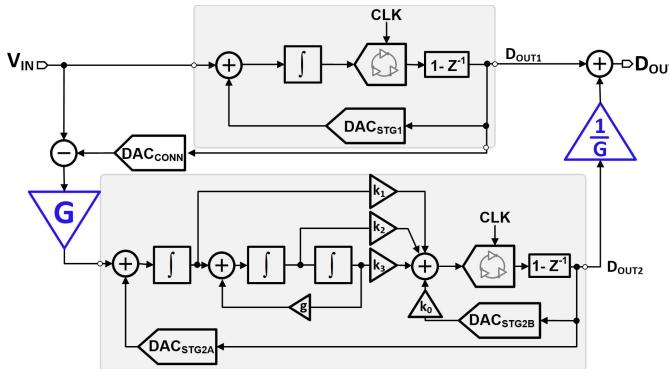
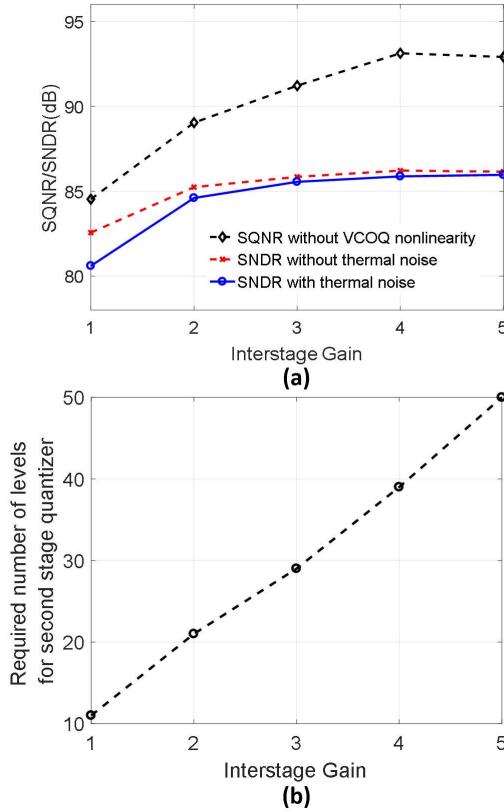
Fig. 14. Block diagram of the modulator with interstage gain G .

Fig. 15. (a) SNDR versus interstage gain. (b) Required number of VCOQ levels for the second stage versus interstage gain.

signal, without digital filtering [Fig. 13(a)], the third harmonic is attenuated by 24.8 dB. With the added digital filter [Fig. 13(b)], the third harmonic is further attenuated by 18 dB. The improvement in SNDR and SFDR by using digital post-processing is also shown from the measured results in Section IV.

F. Effect of Interstage Gain

In this section, the effect of having an interstage gain G as shown in Fig. 14 on the performance of the proposed modulator is discussed. The SQNR/SNDR versus the interstage gain for the proposed two-stage modulator from MATLAB simulations is plotted in Fig. 15(a) for a 4 MHz -3 dBFS input

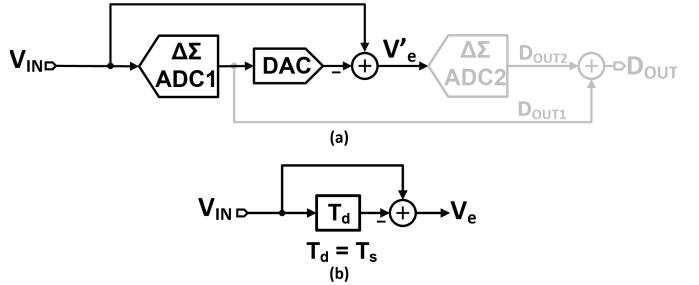


Fig. 16. Block diagram of the (a) residue signal generation at the second stage input and (b) residue signal generation by subtracting a delayed signal from itself.

signal. With thermal noise and the VCOQ nonlinearity disabled, the SQNR increases with interstage gain. With thermal noise disabled and the VCOQ nonlinearity enabled, the SNDR saturates for interstage gains more than two. This is due to the third harmonic distortion limiting the SQNR. With both the thermal noise and the VCOQ nonlinearity enabled, the SNDR improves for an interstage gain of two and then saturates. The number of levels needed for the second stage VCOQ for interstage gains values one to five is shown in Fig. 15(b) for a 50 MHz 0 dBFS input signal. The required number of levels needed for the second stage quantizer increases linearly with interstage gain. When the second stage is designed for higher interstage gain (say two), the DR of the second stage will reduce by 6 dB when the second stage is used as a standalone fourth-order modulator with the same number of quantizer levels. Due to the reduced DR for the standalone fourth-order modulator with higher interstage gains, the design choice was to keep the interstage gain at unity.

G. Number of Quantizer Levels

The block diagram of the residue signal generation at the second stage input is shown in Fig. 16(a). The input to the second stage is the difference between the direct input signal and the delayed input signal through the first stage and DAC_{CONN}. This delay is equal to one sampling clock T_s . Another residue signal generation is shown in Fig. 16(b) by subtracting a delayed signal from itself. The power of the signal component present at the input to the second stage v'_e is shown as the red line in Fig. 17 for different input frequencies. It is observed that the signal component at the input to the second stage increases at a rate of 20 dB/decade. The blue line plots the signal component in the residue signal v_e where the residue signal is generated by subtracting the signal from a delayed version of itself (the delay being equal to one clock period T_s). These two plots are in close agreement. From Fig. 17, it is observed that for the highest frequency input signal, the signal component present at the second stage input is attenuated by 12 dB. Thus, the number of quantizer levels needed for the second stage is also less compared with the number of quantizer levels in the first stage. From Fig. 9, it is also observed that for an input signal amplitude less than 10 dBFS, the standalone second stage provides high linearity. Thus, for the proposed two-stage modulator, the input signal component present at the second stage input

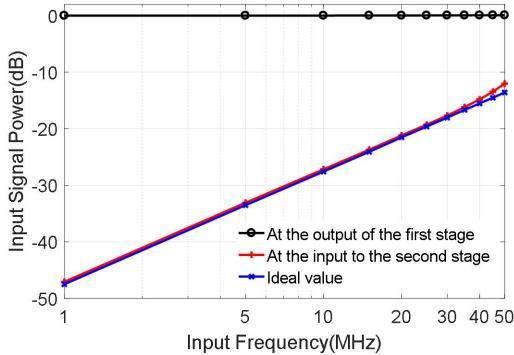


Fig. 17. Signal component at the second stage input versus input frequency.

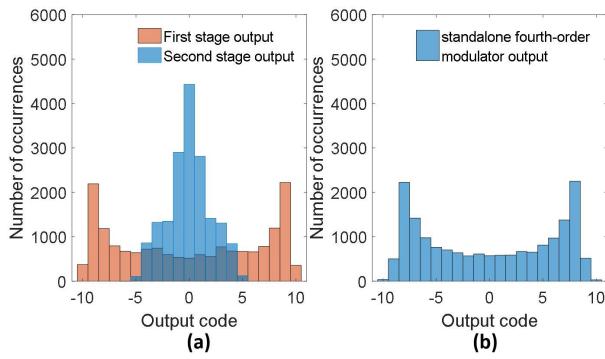


Fig. 18. Histogram of the output code for (a) proposed two-stage modulator and (b) standalone fourth-order modulator for a 50 MHz 0 dBFS input signal.

even for the highest input frequency is small enough not to generate harmonic tones. It is to be noted that the input signal component at the input to the second stage can further be reduced by using an input delay compensation network as in [22]. In [22], a high interstage gain of 10 was used. Thus, it was necessary to attenuate the input signal component to avoid the saturation of the second stage quantizer. In this design, since the interstage gain is unity, even without using an explicit delay compensation network, the amplitude of the signal component at the input to the second stage is small enough (12 dB attenuated) not to saturate the second stage. Thus, no delay compensation network is used in this design. The effect of having an explicit delay compensation network in this design is discussed in Appendix B.

Fig. 18(a) and (b) shows the histograms of the output codes using 16k output samples from the proposed two-stage modulator and the standalone fourth-order modulator, respectively. For a 0 dBFS 50 MHz input signal, the second stage uses only 11 levels of the quantizer. This observation is in agreement with the attenuation of the signal level observed from Fig. 17. When the second stage is used as a standalone fourth-order modulator, all the 20 levels of the second stage quantizer are used. Thus, having a 20-level quantizer for the second stage enables the operation of the second stage as a standalone fourth-order modulator with the same full scale input signal range as that of the two-stage modulator. This is not optimum in terms of overall modulator power and area but provides flexibility during testing to

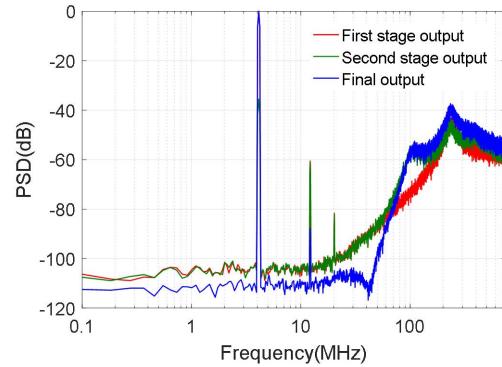


Fig. 19. Simulated PSD of the proposed two-stage modulator at the first stage output, second stage output, and the final output.

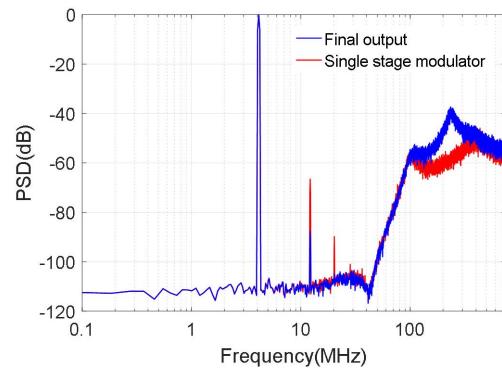


Fig. 20. Simulated PSD of the proposed two-stage modulator and the standalone fourth-order modulator.

measure the second stage performance. If this feature is not needed, the number of levels for the second stage VCOQ, DAC_{STG2A}, and DAC_{STG2B} can be reduced (to 11 levels) to optimize the second stage power without compromising the performance.

H. First Stage Power Scaling

The two stages of the proposed modulator are designed for different thermal and the flicker noise requirements. The thermal noise, flicker noise, and the shaped quantization noise and harmonic components from the first stage are input to the second stage and then canceled at the final output. Thus, the thermal and flicker noise requirements from the first stage can also be relaxed similar to the relaxed quantization noise and linearity requirements. In this design, the input resistance of the second stage determines the overall modulator thermal noise level and the value of this resistor is kept low enough to meet the overall noise requirement. The first stage input resistance is scaled higher (four times the second stage input resistance). Scaling the input resistance of the first stage helps to reduce the first stage opamp power due to a reduced capacitive feedback load and the DAC_{STG1} current. The PSDs of the outputs from each stage are overlaid in Fig. 19 to get a better visibility of the first stage thermal noise cancellation effect. The PSDs in Fig. 19 indicate that the thermal noise along with the quantization noise from the first stage gets canceled at the final output. In Fig. 19, the first stage SNR

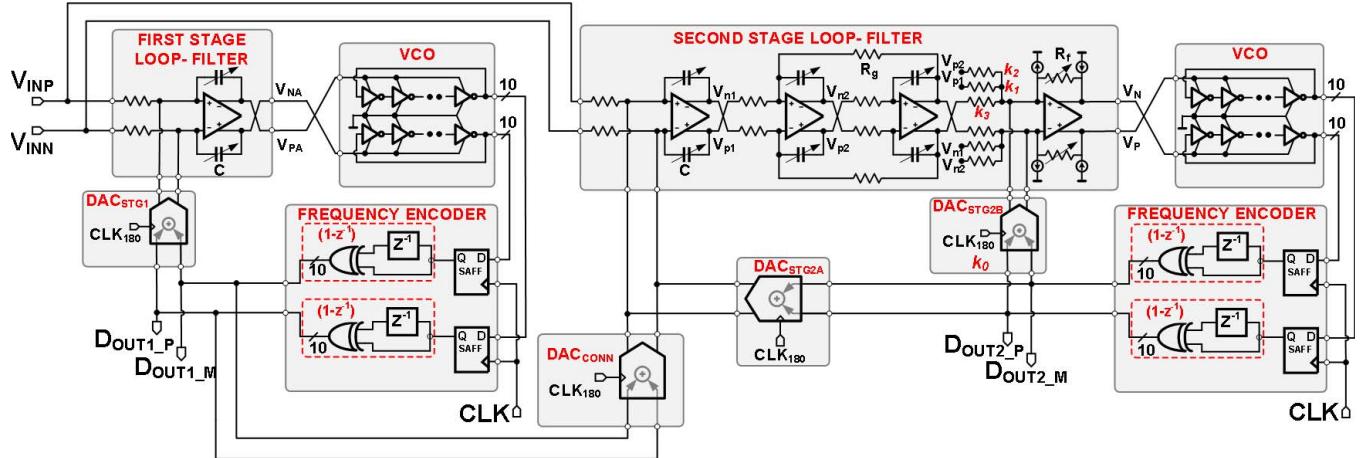


Fig. 21. Schematic of the proposed architecture.

is 67.8 dB due to higher thermal and quantization noise levels and the final output SNR improves to 81.8 dB after cancellation. The standalone second stage PSD is plotted along with the proposed two-stage modulator PSD in Fig. 20. The in-band quantization and thermal noise floor are the same for both cases. This verifies that for the proposed modulator, the SNR is determined by the second stage SNR; thus, the first stage is optimized for power with relaxed thermal noise and linearity requirements.

III. CIRCUIT DETAILS

The schematic of the two-stage CT $\Delta\Sigma$ modulator is shown in Fig. 21. The first stage consists of a first-order loop filter followed by a VCO and frequency encoder. DAC_{STG1} is the feedback DAC for the first stage. The third-order loop filter of the second stage is implemented as a hybrid of feedforward and feedback paths. The second stage loop filter is also followed by a VCO and frequency encoder. DAC_{STG2A} is the main feedback DAC and DAC_{STG2B} is the ELD compensation DAC for the second stage. DAC_{CONN} is the inter-stage DAC that subtracts the output of the first stage from the input to generate the residue. Both the loop filters are implemented using two-stage feedforward compensated opamp-based active-*RC* integrators for linearity requirements [23]. The *RC* time constants can be tuned by the 4-bit capacitor banks. Both stages are designed with half a clock cycle ELD. The VCOQs in both the stages are clocked with the rising edge of the clock and all the DACs are clocked with the falling edge of the clock. Next, the key building blocks of the modulator are described.

A. Loop Filter Amplifiers

The amplifiers in the integrator have a two-stage feedforward compensated architecture as shown in Fig. 22. Feedforward compensation conserves the gain bandwidth product of the opamp and minimizes the ELD caused by the integrator. A telescopic cascode amplifier is used in the first stage, and the second stage is implemented with a common source amplifier. Two separate common-mode feedback circuits are used

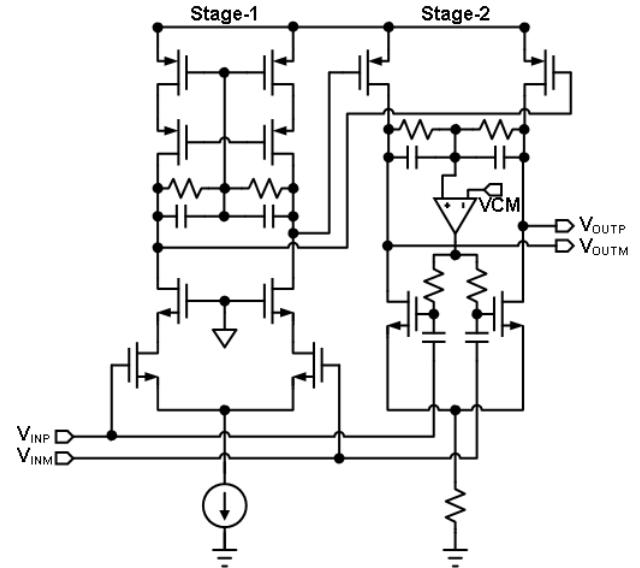


Fig. 22. Schematic of a two-stage feedforward compensated opamp.

to set the output common-mode voltages of both the stages independently. The first stage uses a self-biased common-mode feedback and the second stage uses a common-mode feedback amplifier to set the common-mode voltages. AC coupling capacitors are used to implement the feedforward path from the input to the second stage. The amplifiers consume 4 mA of current and achieve 60 dB dc gain with a 4 GHz unity gain bandwidth.

B. VCO Quantizer

The quantizers in both the stages use a pseudo-differential VCO architecture, each consisting of two VCOs. Each of these VCOs is a 10-delay stage ring oscillator. A single delay cell is a cross-coupled inverter as shown in Fig. 23. The supply rails of the VCO are controlled by the adder differential output V_P and V_N . I_0 provides dc offset voltages for V_P and V_N , which are set to 250 mV above the common mode voltage. Additionally, the VCO's nominal current I_{VCO} is provided at

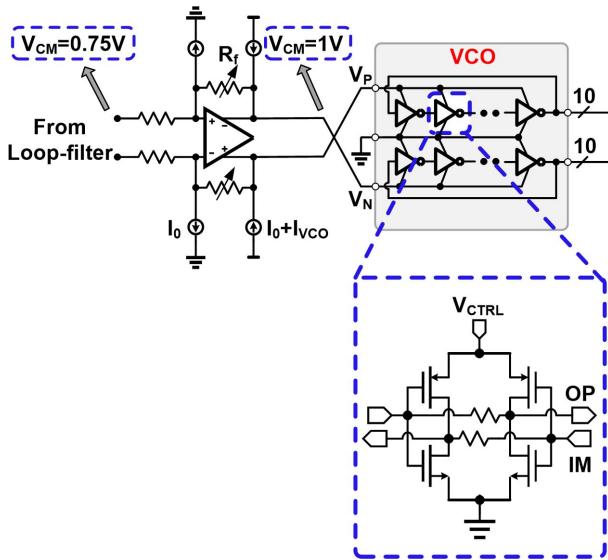


Fig. 23. VCO and summer amplifier.

V_P and V_N . The output of the VCO's phase is quantized using sense amplifier flip-flops. The quantized phase is then fed to a frequency encoder. The positive and negative outputs from a pseudo-differential quantizer are then subtracted in the current domain at the DAC outputs.

C. Feedback DACs

In this design, DAC_{CONN} , which subtracts the first stage output from the input to generate the residue, is the most critical DAC in terms of static and dynamic errors. The output of the VCOQ is barrel shifted, which shapes the static mismatches in the DAC current elements. To reduce sensitivity to dynamic errors caused by clock jitter and data-dependent ISI, DAC_{CONN} uses DRZ DACs to create a non-return-to-zero (NRZ) pulse shape [5], [19]. A single current element of DAC_{CONN} is shown in Fig. 24(a) and the timing waveforms for the switches are shown in Fig. 24(b). Here, D_{IN} is the input data for the DAC. Depending upon D_{IN} being 0 or 1, the switches are controlled according to D_{p1} , D_{p2} , D_{n1} , and D_{n2} to generate the DRZ current pulse shape. For simplicity, the control signals for the switches connected to the common-mode voltage are not shown. They turn ON when the other two switches connected to the same current source are OFF.

The first stage feedback DAC_{STG1} error gets canceled at the final output. Also, the second stage feedback DAC_{STG2A} processes the quantization error from the first stage, which is random in nature. Thus, the linearity requirements of DAC_{STG1} and DAC_{STG2A} are less stringent and standard NRZ DACs are used.

IV. MEASUREMENT RESULTS

The prototype ADC was fabricated in TSMC 65 nm GP CMOS process and assembled in a 60 pin QFN package. It occupies an active area of 0.35 mm^2 . The test board,

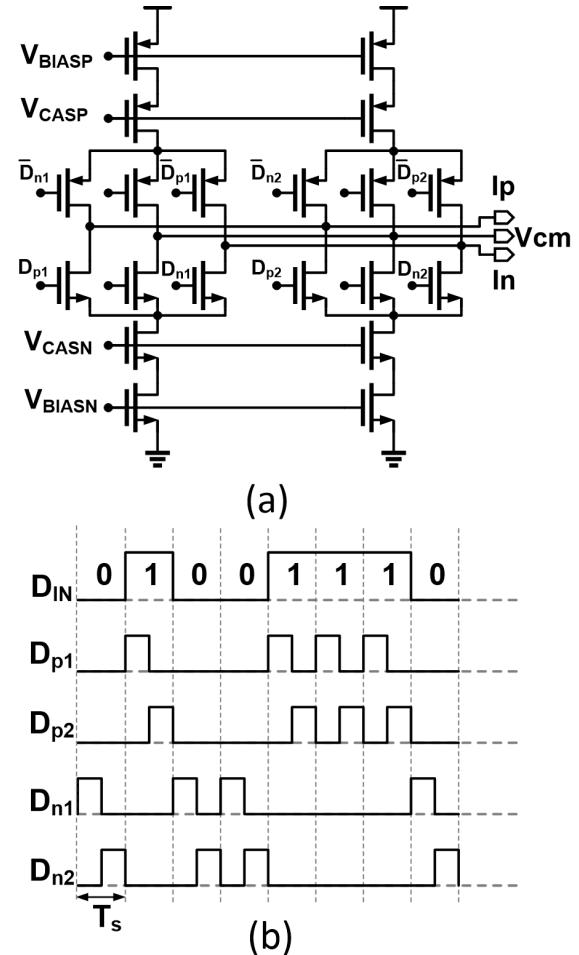


Fig. 24. (a) Schematic of a DRZ DAC current cell. (b) Timing waveforms for the DAC switches.

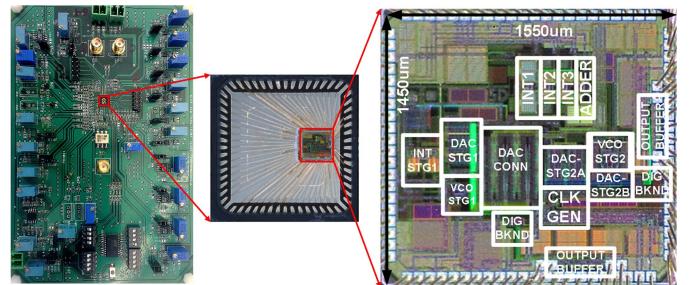


Fig. 25. Photograph of the test board, the package, and the die.

package, and die micrograph are shown in Fig. 25. A four-layer PCB was used to characterize the chip. The test setup is shown in Fig. 26. A passive bandpass filter (Allen Avionics F4526-10P0) was used to eliminate distortion from the input signal source. The sinusoid was then converted into a differential signal using a balun (Minicircuits-ADT1-6T). The modulator output, which was brought out of the chip at full rate, was captured using a logic analyzer (Tektronix TLA7012). The modulator was clocked by a clock source generated from an arbitrary waveform generator (Tektronix AWG7122B). This clock was also used by the logic analyzer to synchronously capture the output data.

TABLE II
PERFORMANCE COMPARISON

Architecture	VCO based $\Delta\Sigma$					Conventional $\Delta\Sigma$				
Reference	This work		[5] Reddy VLSI' 15	[14] Zhu ESSCC' 14	[15] Taylor VLSI' 12	[10] Huang ISSCC' 17	[6] Yoon ISSCC' 15	[8] Dong ISSCC' 14	[24] Shettigar ISSCC' 12	[9] Bolatkale ISSCC' 11
Tech (nm)	65	65	40	65	16	28	28	90	45	
Area (mm ²)	0.35	0.5	0.16	0.075	0.217	0.34	0.9	0.12	0.9	
Fs (GHz)	1.5	1.2	1.6	2.4	2.15	1.8	3.2	3.6	4	
Power(mW)	51.8	54	5.5	39	54	78	235	15	256	
BW (MHz)	50	50	40	37.5	125	50	45.7	36	125	
Fin (MHz)	1	4	10	1	8	7.49	40	5.93	30	
DR(dB)	76.1		72	62.5	73	74.8	85	90	83	
SNR (dB)	76.1		71.7	68.7	71	72.6	76.1	84.6	76.4	
SNDR (dB)	73.5	72.2	69.1	71.5	66.8	70	71.9	74.6	72.6	
SNDR* (dB)	73.5	72.3	72.4							
ENOB	11.9	11.7	11.2	11.6	10.8	11.3	11.65	12.1	11.8	
ENOB*	11.9	11.7	11.7							
FOM_1 (dB)	166		161.7	161.1	162.8	168.4	173.1	172.9	176.8	
FOM_2 (dB)	163.3	162	158.9	161	165.8	160	165.5	162.7	155.5	
FOM_2^* (dB)	163.3	162.1	162.2							
FOM_3 (fJ/conv.)	134	156	222	176	38.6	201	67.2	177.7	737	
FOM_3^* (fJ/conv.)	134	153.8	152							

* values after digital post-processing (power of the digital filter not included).

$$FOM_1 = DR + 10\log_{10}\left(\frac{BW}{Power}\right), FOM_2 = SNDR + 10\log_{10}\left(\frac{Power}{SNDR}\right), FOM_3 = \frac{Power}{2 \cdot BW \cdot 2^{(SNDR - 1.76) / 6.02}}$$

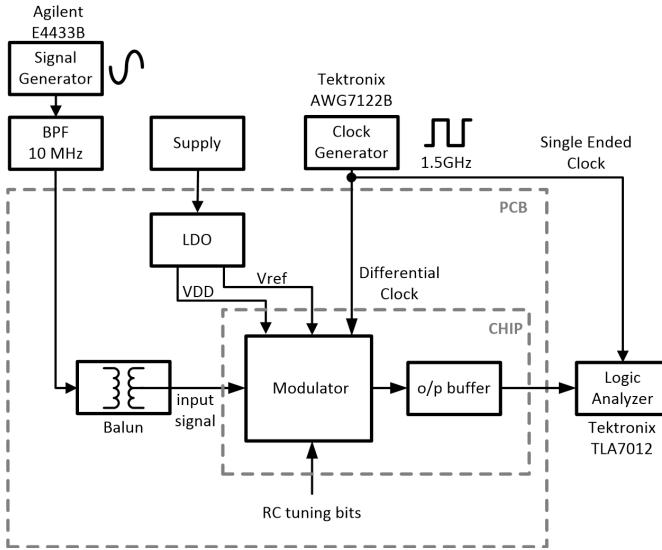


Fig. 26. Block diagram of the test setup.

Clocked at 1.5 GHz, the ADC consumes 51.8 mW. The power breakdown is 25.3 mW for opamps, 13.5 mW for DACs, 7.8 mW for VCOQs, 2 mW for clock generation, and 3.2 mW for digital buffers. The measured SNR and SNDR are plotted as a function of the input amplitude as shown in Fig. 27(a) and the output PSD with a 1 MHz –3 dBFS input signal is shown in Fig. 27(b). For a –3 dBFS 1 MHz input signal, the ADC achieves 88 dB SFDR and a peak SNR/SNDR of 76.1/73.5 dB for a 50 MHz signal bandwidth. The resulting Walden and Schreier FoMs are 134 fJ/conv-step and 166 dB, respectively. The performance of the ADC is summarized in Table II.

The measured output waveform and the PSD of the first stage output, second stage output, and the final combined

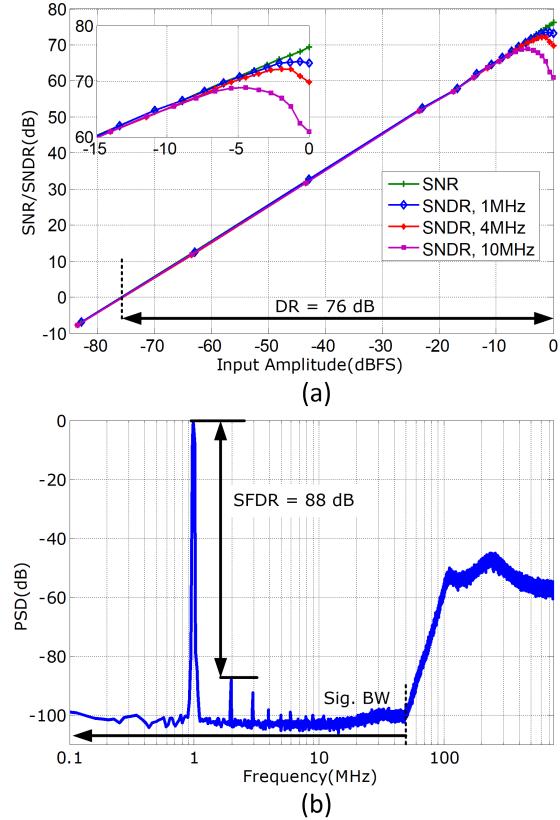
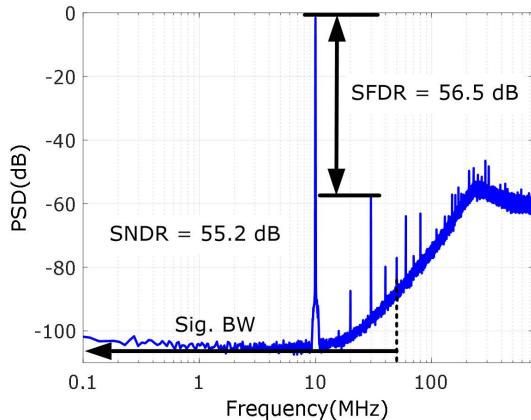
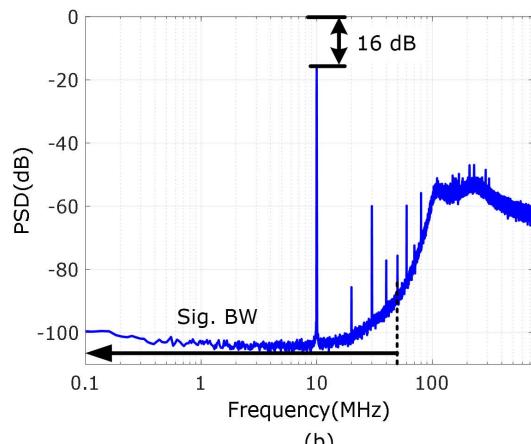


Fig. 27. (a) SNR/SNDR plot versus input amplitude. (b) Measured PSD for a 1 MHz –3 dBFS input signal.

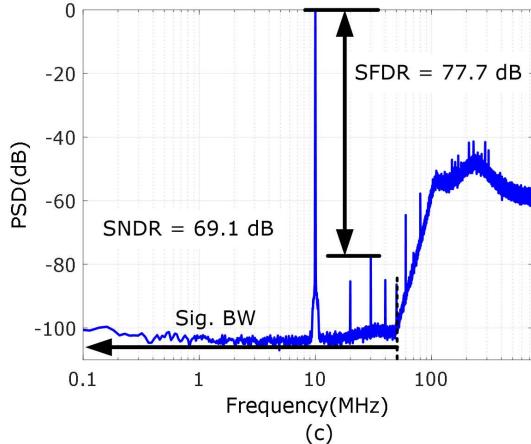
output are shown in Fig. 28(a)–(c), respectively, for a 10 MHz –4 dBFS input tone. The ADC achieves 77.7 dB SFDR and a peak SNR/SNDR of 76.1 dB/69.1 dB for a 50 MHz signal bandwidth. The third harmonic component at the first stage output [Fig. 28(a)] due to the VCOQ nonlinearity is



(a)



(b)



(c)

Fig. 28. Measured PSD for a 10 MHz -4 dBFS input signal at (a) first stage output, (b) second stage output, and (c) final output.

suppressed at the final output [Fig. 28(c)] and improves the SFDR by 21.2 dB.

The architectural benefits of the proposed two-stage CT $\Delta\Sigma$ modulator are demonstrated by comparing it with a single-stage modulator. The single-stage modulator is formed by switching OFF the DAC_{CONN} and using the second stage as a standalone modulator as shown in Fig. 29(a). The measured PSDs of the two-stage modulator (blue curve) and the single-stage modulator (red curve) are shown in Fig. 29(b) for a 10 MHz -4 dBFS input signal. As expected, both the

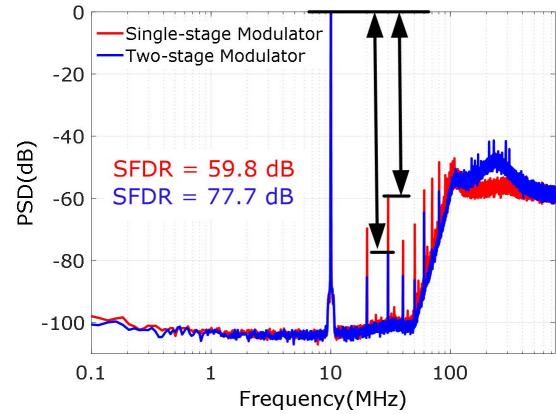
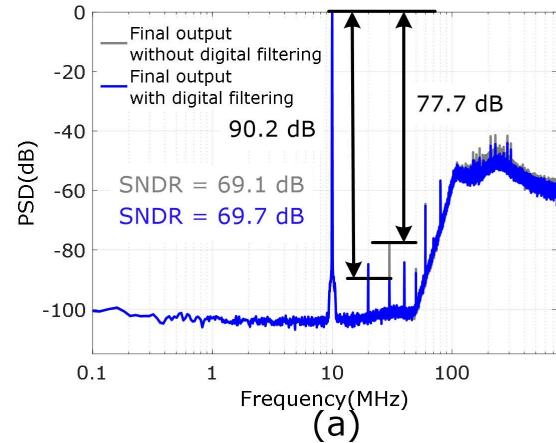
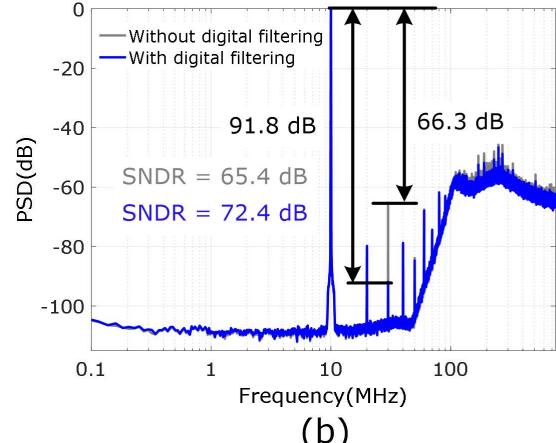


Fig. 29. (a) Block diagram of the single-stage standalone modulator. (b) Measured PSD for a 10 MHz -4 dBFS input signal for the proposed two-stage modulator (blue curve) and the single-stage modulator (red curve).



(a)



(b)

Fig. 30. Measured PSD with and without digital filtering for a 10 MHz (a) -4 dBFS input signal and (b) 0 dBFS input signal.

modulators have the same SNR and the proposed two-stage architecture improves the linearity by 17.9 dB compared with the single-stage VCOQ-based modulator with frequency feedback. The measured SNR is 76.1 dB for the standalone second stage and 81 dB from MATLAB system level simulations. Increased clock jitter due to the ringing of the internal supplies and ground nodes is most likely a cause for the degradation of the noise floor.

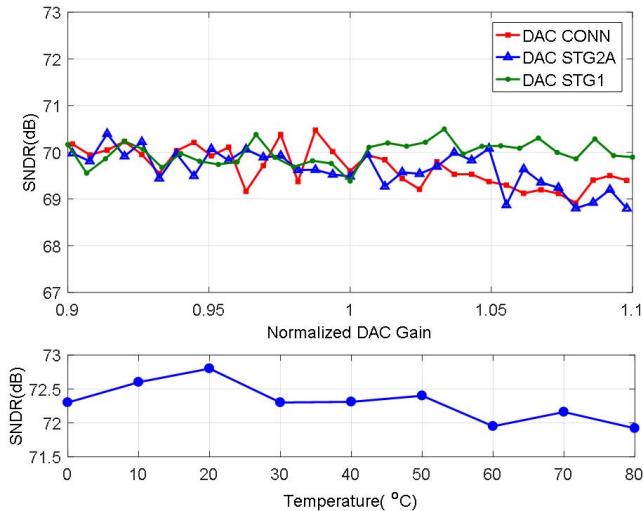


Fig. 31. (a) Measured SNDR versus DAC gain mismatches for a 1 MHz -3 dBFS input signal. (b) Measured SNDR versus temperature for a 1 MHz -0.5 dBFS input signal.

The measured PSDs with and without digital backend filtering for a 10 MHz input signal are shown in Fig. 30(a) and (b) for -4 and 0 dBFS input amplitudes, respectively. With added digital filtering, the third harmonic component is attenuated and the SNDR is no longer limited by the third harmonic from the VCOQ nonlinearity. The SNDR improves from 65.4 to 72.4 dB for the 10 MHz 0 dBFS input signal. The peak SNDR improves from 69.1 dB (for -4 dBFS input amplitude) without filtering to 72.4 dB (for 0 dBFS input amplitude) with filtering.

The robustness of the modulator against the gain mismatch between the two stages is validated through measurement by varying the DAC gains by $\pm 10\%$ and measuring the SNDR for a 1 MHz -3 dBFS input signal in Fig. 31(a). Less than 1.5 dB variation of SNDR is observed for $\pm 10\%$ gain mismatch between the two stages. Although the SNDR variation is 2.5 dB from MATLAB simulations, the increased noise floor from the second stage overshadows the effect of the DAC gain mismatch. Thus, the measured variation of SNDR with the DAC gain mismatch appears to be less than that observed in simulation. The sturdiness of the modulator with temperature variation over 0°C -80°C is shown in Fig. 31(b). Less than 1 dB variation of SNDR is observed over the temperature range. Table II also compares this design with state-of-the-art CT $\Delta\Sigma$ modulators having similar bandwidth and resolution. The proposed modulator achieves the highest SNR among the reported VCO-based $\Delta\Sigma$ ADCs. Also, compared with [14], the proposed modulator offers higher DR and improved robustness against DAC gain mismatches.

V. CONCLUSION

The proposed two-stage CT $\Delta\Sigma$ modulator with VCOQs and implicit DEM provides the benefits of high sampling frequency and wide bandwidth and improves linearity through VCOQ nonlinearity cancellation. This architecture with a second-order NTF for the first stage and a fourth-order NTF

for the second stage exhibits strong immunity to the first stage quantization error leakage to the output due to gain mismatches between the two stages and temperature variations. Furthermore, a dual-RZ DAC makes the modulator robust against DAC dynamic errors due to clock jitter and data-dependent ISI. The prototype modulator fabricated in a 65 nm CMOS technology achieves 73.5 dB SNDR and 88 dB SFDR over the 50 MHz bandwidth. Finally, the measured SNDR variation remains within 1.5 dB for $\pm 10\%$ gain mismatch between the two stages and a temperature variation of 0°C -80°C .

APPENDIX A JUSTIFICATION FOR A SECOND-ORDER NTF FOR THE FIRST STAGE

Another variant of the two stage architecture is shown in Fig. 32 in which an open-loop VCOQ is used for the first stage. Here, the first stage provides a first-order NTF. SNR variations with DAC gain errors are shown in Fig. 33 for the proposed two-stage modulator and the modulator shown in Fig. 32. For the architecture in Fig. 32, higher in-band quantization noise from the first stage results in an overall modulator SNR below 80 dB. Also, the proposed two-stage modulator shows 2.5 dB variation in SNR for $\pm 15\%$ gain errors between the two stages. In comparison, an open-loop VCOQ-based two-stage modulator degrades the SNR by 9 dB for the same variation in the DAC gain errors. This indicates that the proposed architecture is less sensitive to the DAC gain errors compared with the two-stage modulator architecture variant shown in Fig. 32.

The magnitudes of the STF and the NTF for the first stage of the modulator are shown in Fig. 34. The first stage quantization error has a second-order noise shaping. The STF_1 for the in-band frequencies is almost flat with a 0.4 dB peaking at the band edge. Since no ELD compensation is used for this stage, the STF_1 peaks at higher frequencies. This can be problematic in the presence of out-of-band signals and needs to be addressed by appropriate filtering prior to the modulator.

APPENDIX B EFFECT OF SECOND STAGE INPUT DELAY COMPENSATION

An input delay compensation network with a delay of one sampling period T_s is added to the residue generation network as shown in Fig. 35 and simulated in MATLAB. The power of the signal component present at the input to the second stage with and without the delay is plotted in Fig. 36 for different input frequencies and a 0 dBFS input amplitude. With an added delay of T_s to the direct signal path to match the combined delay of the first stage and DAC_{CONN} , the signal component in the residue signal is reduced as shown by the plot in the dotted line. For both cases, the signal component increases at a rate of 20 dB/decade. Next, the effectiveness of the delay compensation network to improve the overall modulator SNDR is evaluated. The SNDR as a function of the input frequency is shown in Fig. 37 with and without the input delay compensation. As expected, the SNDRs of the proposed two-stage modulator with and without the delay compensation are in agreement. This is due to the fact that even without the

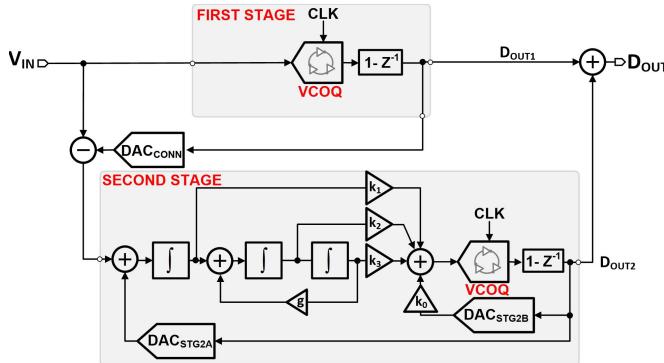


Fig. 32. Block diagram of a two-stage modulator with open-loop VCOQ-based first stage.

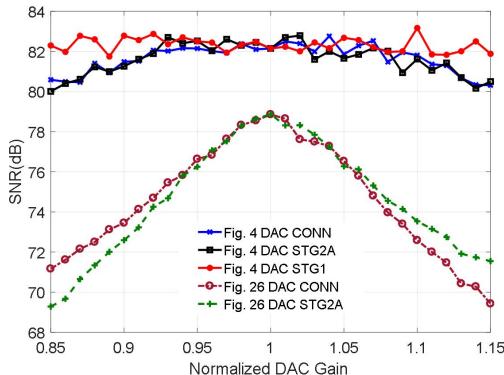


Fig. 33. SNR versus DAC gain mismatches for the proposed two-stage modulator and the modulator in Fig. 32 for a -3 dBFS 4 MHz input signal.

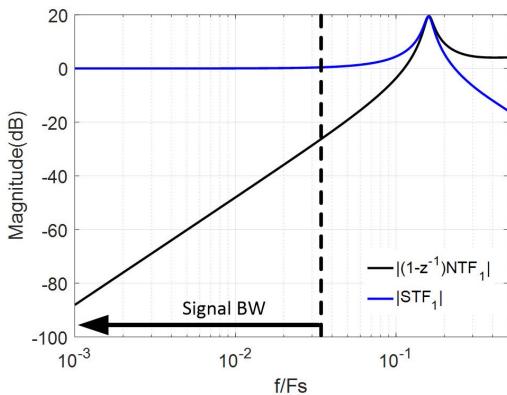


Fig. 34. Magnitude of the STF and the NTF for the first stage of the modulator.

delay compensation network, the signal component present at the second stage input is small enough not to generate any harmonic components and only a limited number of quantizer levels are used for a full scale input signal. In conclusion, even though adding a delay to the direct input path to the second stage decreases the signal component at the second stage input, it does not affect the SNDR or DR of the modulator. Thus, in this design, no delay compensation network was added, which also helped to reduce the modulator design complexity.

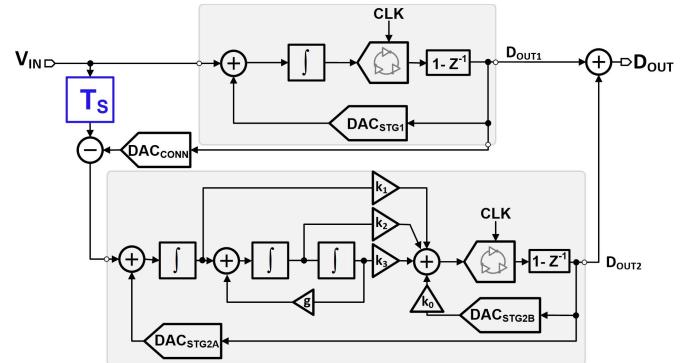


Fig. 35. Block diagram of the proposed modulator with an input delay compensation block.

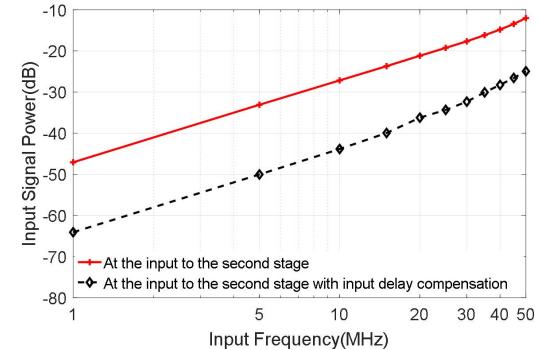


Fig. 36. Signal component at the second stage input versus input frequency with and without input delay compensation.

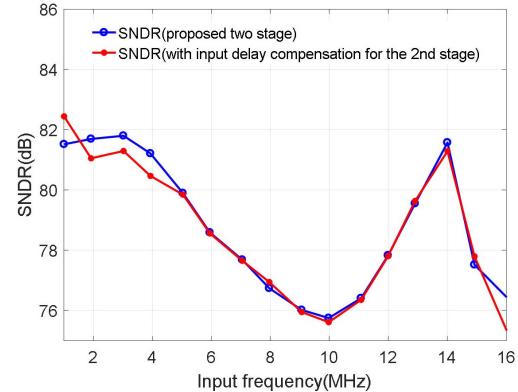


Fig. 37. Simulated SNDR versus input frequency with and without input delay compensation.

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