Comments and Corrections

Corrections to "Split-Array, C-2C Switched-Capacitor Power Amplifiers"

Zhidong Bai, *Student Member, IEEE*, Ali Azam, *Student Member, IEEE*, Dallas Johnson, *Student Member, IEEE*, Wen Yuan, *Student Member, IEEE*, and Jeffrey S. Walling, *Senior Member, IEEE*

FOLLOWING the publication of [1], it was pointed out that there were two errors in Table I, related to [2], listed as [38] in the original paper. The work represented in [2] did not use digital predistortion and the matching network consisted of an on-chip transformer (XFMR). The corrected table is presented below as Table I.

TABLE I
COMPARISON TO PRIOR ART

	This Work	[21]	[20]	[23]	[8]	[38]	[39]	[40]
CMOS Process (nm)	65	65	65	130	65	40	45-SOI	28
Supply (V)	2.4	1.2/2.4	1.3	3	1.2	0.5	1.2/2.4	1.2
Resolution (bits)	13-MP	9-IQ	13-IQ	7-MP	9-Polar	9-Polar	10-Polar	8-Polar
Center Frequency (GHz)	1.8	2.0	2.4	1.8	2.2	2.2	3.5	3.2
Peak P_{out} (dBm)	24	20.5	22.8	26	23.3	14.6	25.3	24.9
Peak SE (%)	40	20.0	34*	24.9	38	26	30.4	42.7#
Modulation	LTE 1.4 MHz 64-QAM	LTE 10 MHz 64-QAM	SC 22MHz, 64 QAM	LTE 10 MHz 64-QAM	802.11g 20 MHz 64-QAM	20 MHZ, OFDM 64-QAM	10 MHz, 32 Carrier 256-QAM	20MS/s 256-QAM
Average P_{out} (dBm)	18.9	14.5	15	20.9	16.8	6.2	17.1	17.5
Average SE (%)	21.2	12.2	NA	15.2	21.8	10.7	21.4	21.3#
EVM (%-rms)	2.65	3.6	3.98	3.5	3.98	1.6	1.0	2.39
ACLR (dBc)	-30.5/-30.9	-30.7/-31.0	<-43	-30.3/-31.7	NA	-46/-46	-45	-31.3
Matching Network	On-Chip LC	On-Chip LC	XFMR	On-Chip LC	XFMR	XFMR	On-Chip LC	XFMR
DPD	Yes	Yes	Yes	Yes	No	No	Yes	No

*Includes Frequency Generation #Drain Efficiency

REFERENCES

[1] Z. Bai, A. Azam, D. Johnson, W. Yuan, and J. S. Walling, "Split-array, C-2C switched-capacitor power amplifiers," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1666–1677, Jun. 2018.

[2] M. Hashemi, Y. Shen, M. Mehrpoo, M. S. Alavi, and L. C. N. de Vreede, "An intrinsically linear wideband polar digital power amplifier," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3312–3328, Dec. 2017.

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