A Time-Based Receiver With 2-Tap Decision Feedback Equalizer for Single-Ended Mobile DRAM Interface

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***Abstract*— A time-based (TB) receiver (RX) with a 2-tap TB decision feedback equalizer (DFE) is proposed for mobile DRAM interface. The TB RX consists of a voltage-to-time converter (VTC), a TB DFE, and a time comparator. The VTC converts the RX input voltage to a time difference between two VTC outputs by using the difference in clock-to-Q delays between two latches with different input offset voltages. The TB DFE inserts an additional delay to one of the two VTC outputs and bypasses the other VTC output to increase the time opening. The time comparator makes a decision with the first arriving edge of the two outputs of the TB DFE. While the feedback loop delay must be less than 1 UI for proper operation in the conventional voltage-based DFE, the TB DFE allows the feedback loop delay up to 1.43 UI in this paper. A transmitter (TX) transmits a single-ended signal of 200-mV swing by using an n-over-n voltage-mode driver. The transceiver in a 65-nm CMOS process achieves a 12.5 Gb/s with a 0.8-V supply through a 15-inch FR-4 channel of 14-dB loss. The TX and RX chip consume 4.3 and 3.4 mA, respectively. The energy efficiency is 0.49 pJ/b.**

***Index Terms*— Decision feedback equalizer (DFE), feedback loop delay larger than 1 UI, low power, low supply, single-ended, time based (TB), TB receiver (RX), transceiver, voltage-to-time converter (VTC).**

I. Introduction

MOBILE DRAMs are widely used in portable electronic devices [1], where high-speed interface operation is performed to exchange video data between mobile DRAMs and CPU. Because portable electronic devices are battery powered, the low-power consumption is the primary concern in the high-speed mobile DRAM interface.

Two methods are generally considered for low-power mobile DRAM interface [1]. One is to reduce the channel signal swing, and the other is to reduce the supply voltage. Reducing the channel signal swing, reduces the transmitter (TX) signaling power proportionally because the current flowing through the channel and the termination resistors is proportional to the channel signal swing. However, the reduced signal swing requires a large gain of the receiver (RX) front-end circuit [2], and hence increases the RX power consumption. The supply voltage reduction decreases the dynamic power consumption of the transceiver [3]. However, the supply voltage reduction limits the maximum data rate of the transceiver because of the reduced transconductance (g_m) and the increased delay time of the transceiver circuit. To increase the data rate, a parallelism is generally used at the transceiver circuits [3]–[5]. However, the RX front-end circuit, which consists of a pre-amplifier and an equalizer, still suffers from the low supply voltage because of its full-rate operation. As a result, transceivers in 65-nm process with the supply voltage less than 0.8 V show the data rate less than 8 Gb/s in the literature [4]–[6]. A continuous-time linear equalizer (CTLE) or a decision feedback equalizer (DFE) is mostly used in the RX front-end circuits to increase the maximum data rate by widening the eye opening [5]–[8]. Because a CTLE has analog nature, its performance is degraded at low supply voltage. The peaking frequency and the gain of CTLE are reduced due to the reduced transconductance and the increased loading [7]; this is called the g_m/C constraint. In the case of DFE, the maximum data rate is limited by the feedback loop delay, which increases at low supply voltage. A look-ahead architecture and a soft-decision architecture are reported to alleviate the feedback loop delay problems [9], [10]. However, the feedback loop delay is still required to be less than 1 UI for proper operation of DFE circuits.

This paper reports a time-based (TB) RX to eliminate the g_m/C constraint at low supply voltage [11]. The TB RX consists of a voltage-to-time converter (VTC), a TB DFE, and a time comparator. The VTC converts the RX input voltage to the time difference between two outputs of the VTC. The VTC is implemented by using two differential latches with different input offset voltages, such that, the difference between the clock-to-Q delays of the two latches is proportional to the difference between the RX input voltage and a reference voltage. Because the clock-to-Q delay increases as the supply voltage is reduced, the VTC gain (the ratio of the output time difference with respect to the input voltage) increases as the supply voltage is reduced. Thus, the proposed VTC is free

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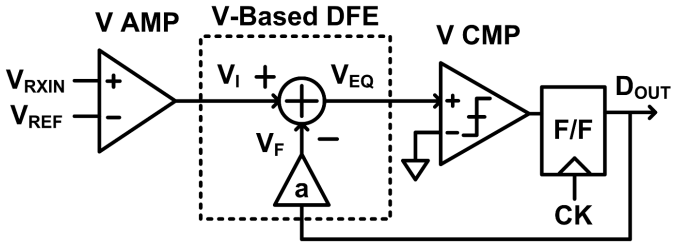

Fig. 1. Conventional VB RX.

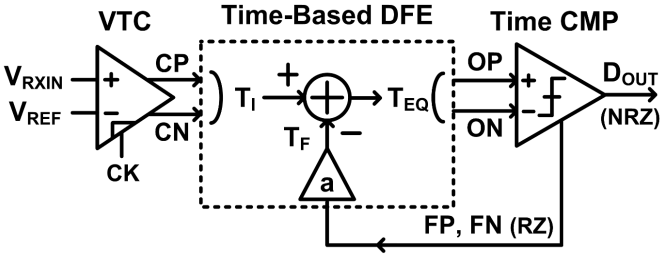

Fig. 2. Proposed TB RX.

from the g_m/C constraint at low supply voltage. The TB DFE inserts an additional delay to one of the two VTC outputs to increase the eye opening in time axis. The proposed TB RX extends the upper limit of the feedback loop delay up to 1.43 UI; this helps to increase the maximum data rate. The proposed single-ended transceiver including the TB VTC and the TB DFE achieves the data rate of 12.5 Gb/s with a 0.8-V supply and a 65-nm CMOS process.

This paper is composed as follows. Section II describes the architecture of the proposed TB RX. Section III provides the circuit implementation of the proposed transceiver. Section IV presents the measurement results and the comparison with previously published works. Section V concludes this paper.

II. Architecture of Time-Based Receiver

A conventional RX consists of a voltage-based (VB) pre-amplifier, a VB DFE, and a VB comparator (Fig. 1); V_I is the VB pre-amplifier output, V_F is the feedback signal to compensate inter-symbol interference (ISI), and V_{EQ} is the compensated signal which is $V_I - V_F$. The VB comparator makes a decision by comparing V_{EQ} with a reference voltage. The proposed TB RX consists of a VTC, a TB DFE, and a time comparator (Fig. 2). The VTC accepts a differential input voltage ($V_{\mathrm{RXIN}} - V_{\mathrm{REF}}$) and a clock signal (CK) as input and generates two clock-like signals (CP, CN) as output, such that, CP and CN remain at "0" when CK is "1," transition from "0" to "1" while CK is "0," and transition back to "0" when CK returns to "1." The delay times from the falling edge of CK to the rising edge of CP and CN depend on the differential input voltage of two latches that constitute the VTC. When $V_{\mathrm{RXIN}} - V_{\mathrm{REF}}$ is 0 at the falling edge of CK, CP, and CN have the same delay time T_{REF}. When $V_{\mathrm{RXIN}} - V_{\mathrm{REF}}$ is positive at the falling edge of CK, CP transitions to "1" earlier than CN, the delay time of CP (T_{CP}) is less than T_{REF} and that of CN (T_{CN}) is larger than T_{REF} (Fig. 3). The difference in the delay times of CP and CN ($T_I = T_{\mathrm{CP}} - T_{\mathrm{CN}}$) is approximately proportional to $V_{\mathrm{RXIN}} - V_{\mathrm{REF}}$; $|T_I|$ corresponds to the time difference between the rising edges of CP and CN, and T_I is negative when CP rises earlier than CN.

Because the channel ISI reduces the magnitude of $V_{\mathrm{RXIN}} - V_{\mathrm{REF}}$ at the falling edge of CK, the time difference $|T_I|$ is also reduced by ISI. The TB DFE compensates for ISI by enlarging the reduced time difference. The TB DFE accepts two pairs of clock-like signals (CP, CN, FP, and FN) as input and generates a pair of clock-like signals (OP, ON) as output. The time difference between the rising edges of OP and ON (T_{EQ}) is set to $T_I - T_F$; T_F is the additional delay time to compensate ISI in the TB DFE. The DFE operation in time domain is explained in Fig. 4. If the previous decision data $D_{\mathrm{OUT}}(n-1)$ is "0" (FP = "0," FN = "1," and $T_F > 0$), CN is delayed and CP remains unchanged; ON is a delayed version of CN with an additional time delay of $|T_F|$ and OP is a replica of CP without additional time delay. If the previous decision data $D_{\mathrm{OUT}}(n-1)$

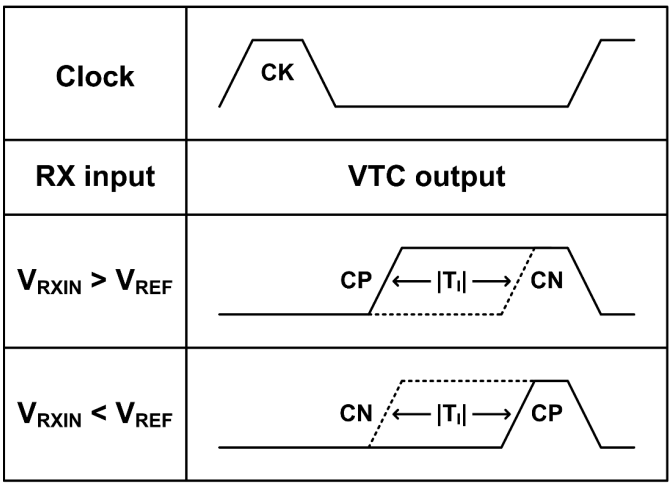

Fig. 3. Voltage-to-time conversion in TB RX.

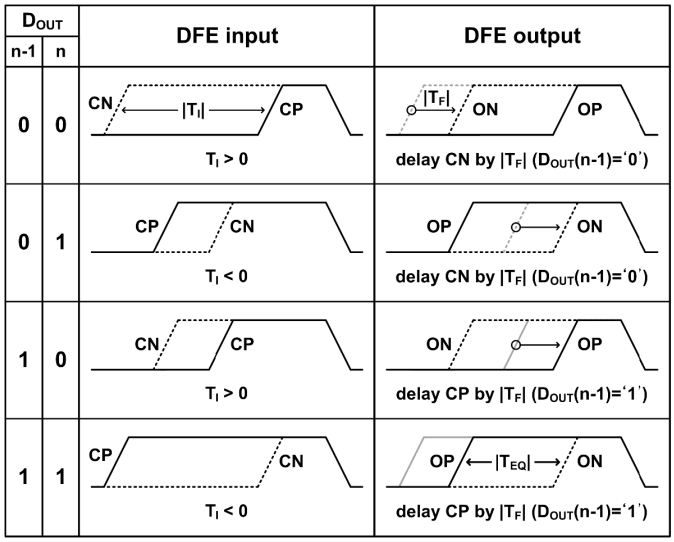

Fig. 4. Operation of TB DFE.

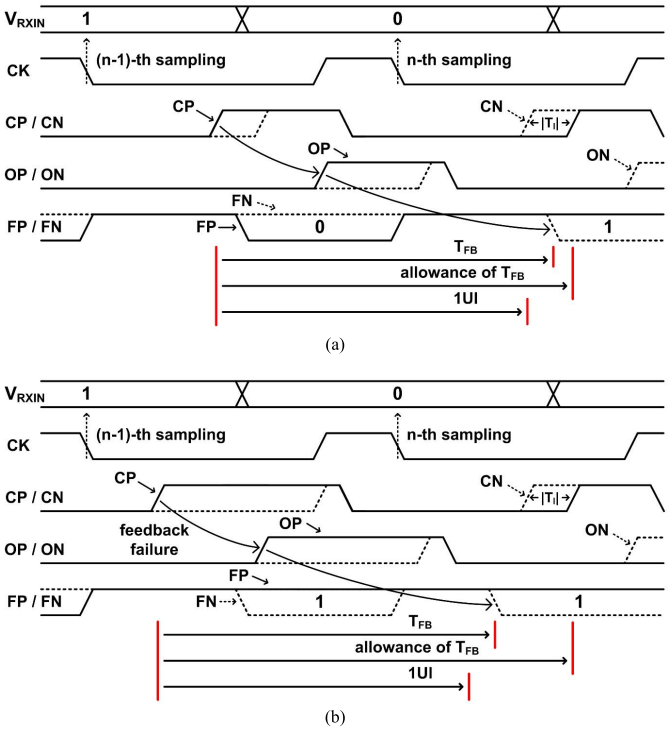

Fig. 5. Timing diagrams of TB DFE operation. (a) V_{RXIN} = "010" and (b) V_{RXIN} = "110".

is "1" (FP = "1," FN = "0," and $T_F < 0$), CP is delayed and CN remains unchanged; OP is a delayed version of CP with an additional time delay of $|T_F|$ and ON is a replica of CN without additional time delay. T_{EQ} is the time difference between the rising edges of OP and ON; T_{EQ} is negative if the rising edge of OP comes before ON. For the case of two successive data input of "00," $T_F > 0$, $T_I > 0$, $|T_{\mathrm{EQ}}| = |T_I - T_F| < |T_I|$ (Fig. 4). For "01," $T_F > 0$, $T_I < 0$, $|T_{\mathrm{EQ}}| = |T_I - T_F| > |T_I|$. For "10," $T_F < 0$, $T_I > 0$, $|T_{\mathrm{EQ}}| = |T_I - T_F| > |T_I|$. For "11," $T_F < 0$, $T_I < 0$, $|T_{\mathrm{EQ}}| = |T_I - T_F| < |T_I|$. Thus, at transition of data input ("01," "10"), $|T_{\mathrm{EQ}}| > |T_I|$, and at no transition of data input ("00," "11"), $|T_{\mathrm{EQ}}| < |T_I|$; the TB DFE increases the output time window $|T_{\mathrm{EQ}}|$ at transition of data input, where the input time window $|T_I|$ is reduced by ISI.

The time comparator consists of two stages of SR latches in series; the first stage accepts the TB DFE output signals (OP, ON) as input and generates an RZ feedback signal (FP, FN) as output, and the second stage accepts FP and FN as input and generates a digital decision data (D_{OUT}) as output. At the first arriving rising edge of two inputs (OP, ON) after the falling transition of CK, the time comparator decides FP, FN, and D_{OUT} (Fig. 4). The timing diagram of the proposed TB RX is shown in Fig. 5(a) with the successive data input of "010"; where the VTC output (CP, CN) and the TB DFE output (OP, ON) are presented for the 2nd and the 3rd data input ("10"), and the time comparator output (FP, FN) is presented for the 1st and the 2nd data input ("01").

In the conventional VB RX, VB amplifiers suffer from small transconductance, small voltage gain and small output voltage swing at low supply voltage. On the other hand, in the TB RX, the VTC can provide a large voltage-to-time gain at low supply voltage because the delay time increases as the supply voltage is reduced. In addition, because the VTC outputs are full-swing signals, they can provide enough voltage difference to the following stage; the full-swing signal improves the RX input sensitivity, reduces the feedback loop delay of the TB DFE circuit, and reduces the design burden of the following stages [12]. Above all, the TB DFE allows the feedback loop delay (T_{FB}) larger than 1 UI, while the loop delay must be less than 1 UI for proper operation in the VB DFE; this significantly increases the maximum data rate in the TB DFE at low supply voltage. T_{FB} is determined by the sum of the delay times of the TB DFE, the time comparator, and the buffers between the time comparator and the TB DFE. The allowance of T_{FB} is the time interval from the earlier rising edge of the $(n-1)$th CP or CN to the rising edge of the nth CP or CN which is used for DFE (Fig. 5); this allowance of T_{FB} is different for different combinations of V_{RXIN} (Table I) because the V_{RXIN} combination determines the nth rising edge of CP or CN which is used for DFE. With a data transition between the $(n-1)$th and nth V_{RXIN}, the allowed T_{FB} is larger than 1 UI. With no data transition, the allowed T_{FB} is less than 1 UI. For the case of V_{RXIN} = "010" or "101" with a data transition [the 1st case in Table I, Fig. 5(a) ("010")], T_{FB} is allowed up to 1 UI + $|T_I|$ at the nth V_{RXIN} because the later rising edge of the nth CP or CN is used for DFE, and the $(n-1)$th earlier edge occurs 0.5 $|T_I|$ earlier than the reference time (T_{REF} after the falling edge of CK) and the nth later edge occurs 0.5 $|T_I|$ later than the reference time. For the case of V_{RXIN} = "100," "011," "000," or "111" with no data transition between the $(n-1)$th and nth V_{RXIN} (the 3rd and the 4th cases of Table I), the allowance of T_{FB} is reduced to 1 UI $-|T_F|$ or 1 UI because the earlier edge of the nth CP or CN is used for DFE. Thus, when 1 UI < T_{FB} < 1 UI + $|T_I|$, a feedback failure occurs in the 3rd or the 4th case of Table I because the correct feedback does not reach the TB DFE yet at the earlier edge of the nth CP or CN and the corresponding nth edge is modified with the pre-charged state (V_{DD}) of feedback signals (FP, FN); as a result, both nth edges of CP and CN have the same value of "1" as feedback signal. Although the DFE does not work correctly,

TABLE I
MAXIMUM ALLOWANCE OF FEEDBACK LOOP DELAY (T_{FB}) FOR DIFFERENT RX INPUT PATTERNS

case	input pattern '(n-2)-th, (n-1)-th, (n)-th'	allowance of T_{FB}
1	'010' '101'	1UI + $\|T_I\|$
2	'110' '001'	1UI + $\|T_I\|$ + $\|T_F\|$
3	'100' '011'	1UI - $\|T_F\|$
4	'000' '111'	1UI

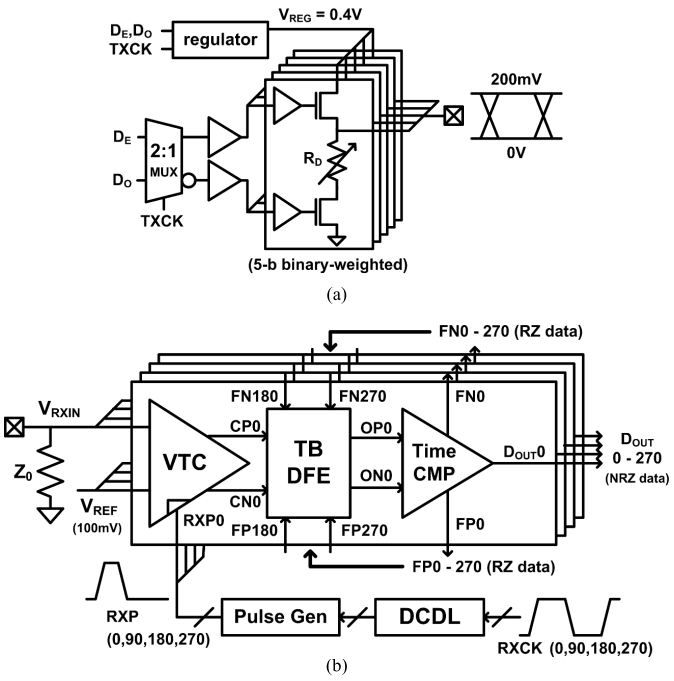

Fig. 6. (a) TX circuit. (b) RX circuit.

the RX makes a correct decision because $|T_I|$ is large enough in these cases. Besides, the feedback failure at the $(n-1)$th bit provides an additional time gain of $|T_F|$ at the nth bit because the $(n-1)$th TB DFE output arrives at the time comparator without the TB DFE delay of $|T_F|$; this increases the allowance of $T_{\rm FB}$ to 1 UI + $|T_I|+|T_F|$ for the case of "110" or "001" data input [the 2nd case in Table I, Fig. 5(b)]. It helps provide successful feedback to the nth bit even with a reduced $|T_I|$ due to residual ISI. Because the 1st case of Table I determines the worst case for $T_{\rm FB}$, $T_{\rm FB}$ must be less than 1 UI + $|T_I|$. Up to now, only a 1-tap DFE is considered; the TB DFE is applicable to a multi-tap DFE, also. A multi-tap DFE would increase $|T_I|$ significantly and hence the maximum data rate; a large VTC gain would also increase $|T_I|$. A multi-phase operation increases the period of the VTC clock (CK) in Fig. 3; the increased period of CK allows a lower g_m/C_L and hence increases the VTC gain and $|T_I|$. In this paper, $T_{\rm FB}$ is allowed up to 1.43 UI at 12.5 Gb/s because the 2nd-tap DFE and the four-phase operation enhances $|T_I|$ to 0.43 UI.

III. Circuit Implementation

A TX consists of an n-over-n voltage-mode driver, a pre-driver, a 2:1 mux, and a regulator [Fig. 6(a)]. A switch-type regulator is used to generate the supply voltage $V_{\rm REG}$ of the n-over-n voltage-mode driver because it eliminates the static current of the regulator itself [2], [13]. With $V_{\rm REG}$ of 400 mV, the low-frequency channel signal swing driven by the voltage-mode driver is 200 mV. For matching the output impedance to the channel characteristic impedance, the ON-resistance of the pull-up path is controlled by adjusting the number of slices and that of the pull-down path is controlled by adjusting the resistor (R_D). The RX block has a quarter-rate structure and a quarter RX block consists of a VTC, a TB DFE,

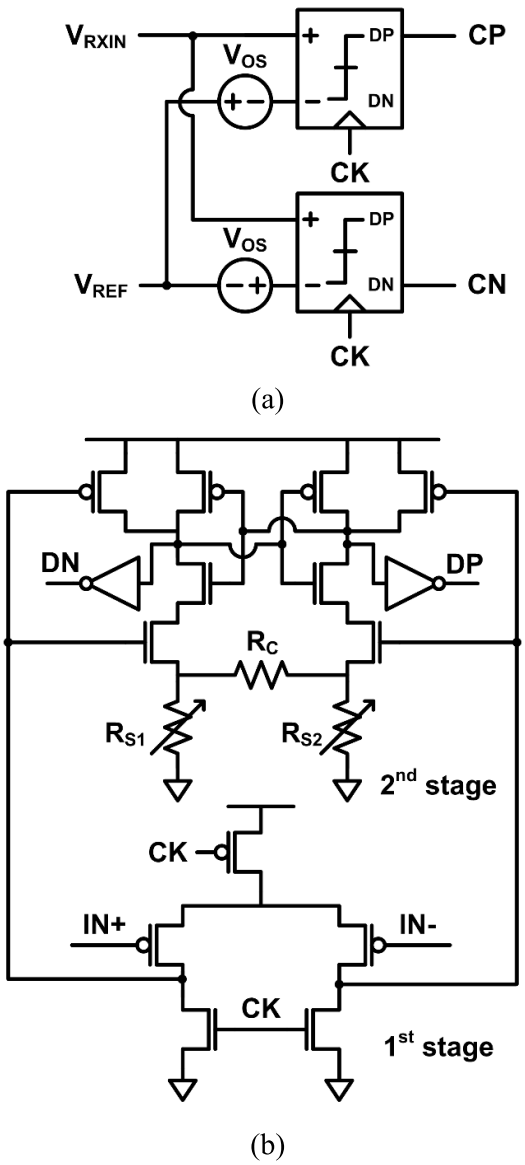

Fig. 7. (a) VTC circuit. (b) VB comparator circuit in VTC.

and a time comparator [Fig. 6(b)]. Four-quarter RX blocks are synchronized by using quarter pulses generated by the pulse gen block. A 2-tap TB DFE is adopted for the TB DFE.

Each VTC in a quarter RX block consists of two differential comparators [Fig. 7(a)]; one comparator has a positive offset voltage ($+V_{\rm OS}$), and the other has a negative offset voltage ($-V_{\rm OS}$). The upper comparator of Fig. 7(a) has the clock-to-Q delay time of $C_L/G_m \times \ln(V_{\rm DD}/|V_{\rm OS}+V_{\rm RXIN}-V_{\rm REF}|)$; G_m is the transconductance of the comparator, C_L is the output load capacitance, and $V_{\rm RXIN}-V_{\rm REF}$ is the differential input voltage sampled at the falling edge of CK. The clock-to-Q delay time is calculated from the latch regeneration time with the initial differential input voltage of $V_{\rm OS}+V_{\rm RXIN}-V_{\rm REF}$ at the falling edge of CK. Similarly, the clock-to-Q delay time of the lower comparator of Fig. 7(a) is $C_L/G_m \times \ln(V_{\rm DD}/|V_{\rm OS}-V_{\rm RXIN}+V_{\rm REF}|)$.

Each comparator of Fig. 7(a) is implemented with a two-stage latch-type comparator [Fig. 7(b)]; the first stage amplifies

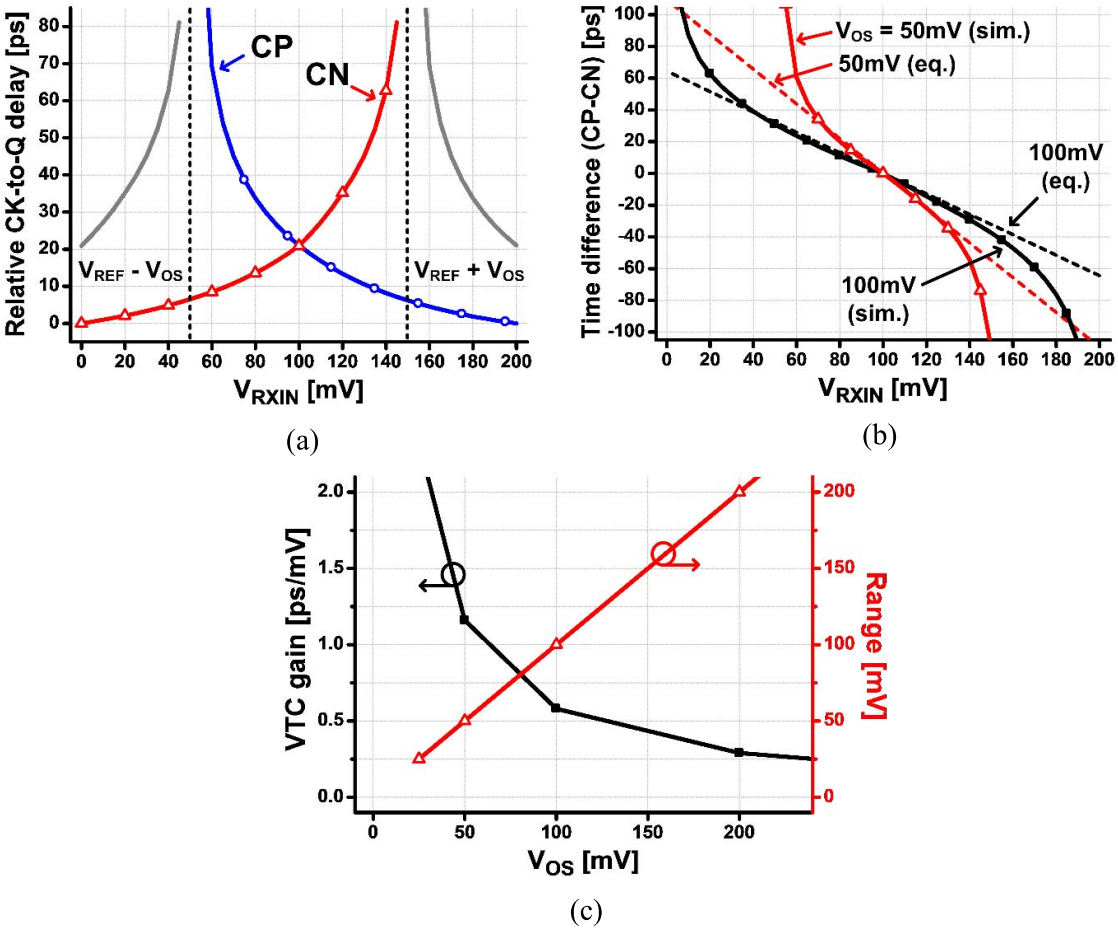

Fig. 8. (a) Clock-to-Q delays of CP and CN (T_{CP}, T_{CN}) when V_{OS} = 50 mV. (b) Time difference T_I ($T_{CP} - T_{CN}$). (c) VTC gain and the range (<10% non-linearity) of the linear region of the VTC gain based on (1) and (2) versus V_{OS}.

an input signal and the second stage operates as a latch. The source-degenerated resistors (R_C, R_{S1}, and R_{S2}) reduce the transconductance to increase the VTC gain and adjust V_{OS} to change the valid range of V_{RXIN}. When CK is "1," DP and DN are pre-discharged to V_{SS}. When CK becomes "0," either DP or DN transitions to V_{DD} after a clock-to-Q delay starting from the falling edge time of CK. With the variations of process (TT, FF, and SS), supply voltage (±25 mV at 0.8 V), and temperature (−25 °C–125 °C), the nominal VTC gain of 1.15 ps/mV changes in the range from 0.68 to 1.8 ps/mV at V_{OS} of 50 mV. However, in spite of the variations, the minimum VTC gain of 0.68 ps/mV is still large enough for the proper operation of the following TB DFE and time comparator circuits.

Fig. 8(a) and (b) presents the post-layout simulation results for the VTC circuit with V_{REF} = 100 mV and V_{OS} = 50 mV; the left-hand side curves of Fig. 8(a) centered around the axis of $V_{RXIN} = V_{REF} - V_{os}$ correspond to the clock-to-Q delay time of the upper comparator of Fig. 7(a), and only the positive output (DP) of the upper comparator is taken as the VTC output (CP). Similarly, only the negative output (DN) of the lower comparator of Fig. 7(a) is taken as the VTC output (CN). The VTC works in the range of V_{RXIN} from $V_{REF} - V_{os}$ to $V_{REF} + V$os; in this range of V_{RXIN}, both CP and CN transition from "0" to "1" after the clock-to-Q delay of the corresponding latch starting from the falling edge of CK. The time difference T_I between the rising edges of CP and CN is given by (1). By using a Taylor series, the logarithmic terms in (1) are simplified into a linear term as follows:

$$T_I = \frac{C_L}{G_m} \times \left(\ln \frac{V_{DD}}{|V_{OS} + (V_{RXIN} - V_{REF})|} - \ln \frac{V_{DD}}{|V_{OS} - (V_{RXIN} - V_{REF})|} \right) \quad (1)$$

$$T_I \approx \frac{-2}{V_{OS}} \cdot \frac{C_L}{G_m} \cdot (V_{RXIN} - V_{REF}). \quad (2)$$

The VTC gain $|T_I/(V_{RXIN} - V_{REF})|$ is controlled by V_{OS} as can be seen in (2). The VTC gains are 1.15 and 0.66 ps/mV for V_{OS} of 50 and 100 mV, respectively, in this paper [Fig. 8(b)]. The VTC gain [s/V] can be translated into a voltage gain [V/V] by considering the slew rate [V/s] of CP and CN. When the slew rate of CP and CN is 500 mV/20 ps, the VTC gain of 1.15 ps/mV corresponds to the voltage gain of 28.8 V/V. This large voltage gain helps reduce the RX input sensitivity, that is, the large voltage gain enhances the RX input sensitivity. As shown in (1) and (2), the VTC gain is inversely proportional to the transconductance (G_m); this reduces the design burden of the comparator. The curve of (2) with C_L/G_m = 29 ps agrees well with the simulated results in the linear region [Fig. 8(b)]. As V_{OS} increases, the VTC gain decreases and

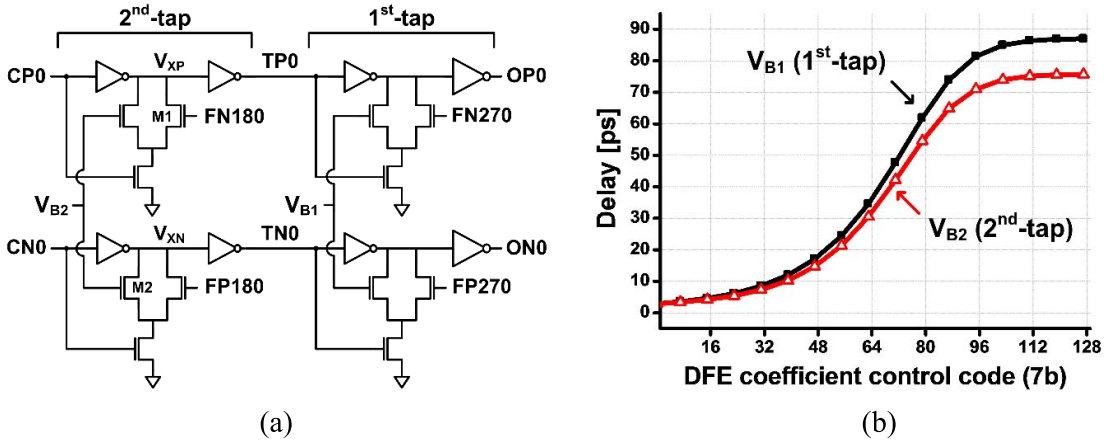

Fig. 9. (a) TB DFE circuit (a quarter circuit). (b) TB DFE delay.

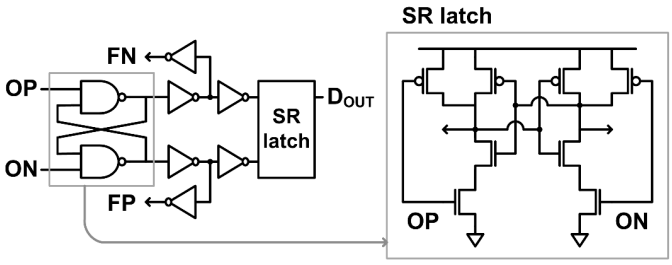

Fig. 10. Time comparator circuit.

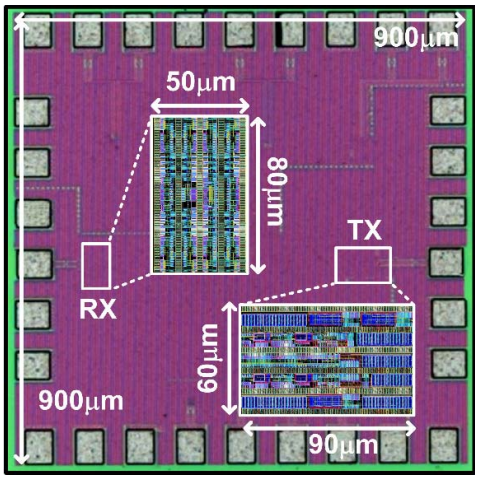

Fig. 11. Chip micrograph and layout.

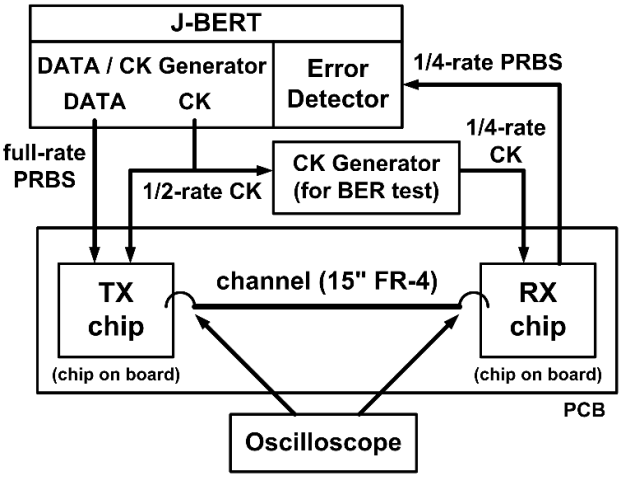

Fig. 12. Test setup for the transceiver system.

the range of the linear region increases [Fig. 8(c)]. The non-linearity of the VTC gain is less than 10% for V_{RXIN} within the range from $V_{\mathrm{REF}} - V_{\mathrm{OS}}/2$ to $V_{\mathrm{REF}} + V_{\mathrm{OS}}/2$ as estimated with (1) and (2). When V_{OS} is larger than 200 mV, the linear VTC gain with the non-linearity less than 10% is maintained within the entire input swing range (200 mV) of V_{RXIN} in this paper, but the VTC gain is reduced to 0.29 ps/mV according to (2). Because the RX input sensitivity is more important than the linearity in the targeted DRAM interface, V_{OS} is chosen to be 50 mV in this paper.

Fig. 9(a) presents a 2-tap TB DFE circuit in a quarter RX block [Fig. 6(b)]. The 2nd-tap delay is applied prior to the 1st-tap delay to reduce the DFE loop delay for the 1st-tap and to increase $|T_I|$ of Table I. Each tap consists of two inverters in series connection and a pull down path is connected at the 1st inverter output node. By controlling the slew rate of the falling edge of the 1st inverter output at each tap, an adjustable delay is added to the rising edge of OP0 or ON0. Because the control codes (FN180, FP180) are differential RZ data, only one of CP0 or CN0 is selected at a time for the delay. When FN180 = "1" and FP180 = "0" at the rising edges of CP0 and CN0, a minimal delay occurs at CP0 as V_{XP} is rapidly discharged due to the large overdrive voltage of M1 and a large delay occurs at CN0 as V_{XN} is slowly discharged due to the small overdrive voltage of M2. V_{B1} and V_{B2} are generated from the 1st- and the 2nd-tap DFE coefficients by using two 7-b R–$2R$ DACs. As the 7-b control code increases, both V_{B1} and V_{B2} decrease. The simulated delay ranges from 2.8 to 87 ps by changing V_{B1}, and from 2.8 to 75 ps by changing V_{B2} [Fig. 9(b)]; the delay represents the time difference between the real delay and the minimal delay. This difference in the delay range is due to the larger-sized inverters used for V_{B1}.

A time comparator in a quarter RX block consists of two SR latches in series connection (Fig. 10). The first stage provides

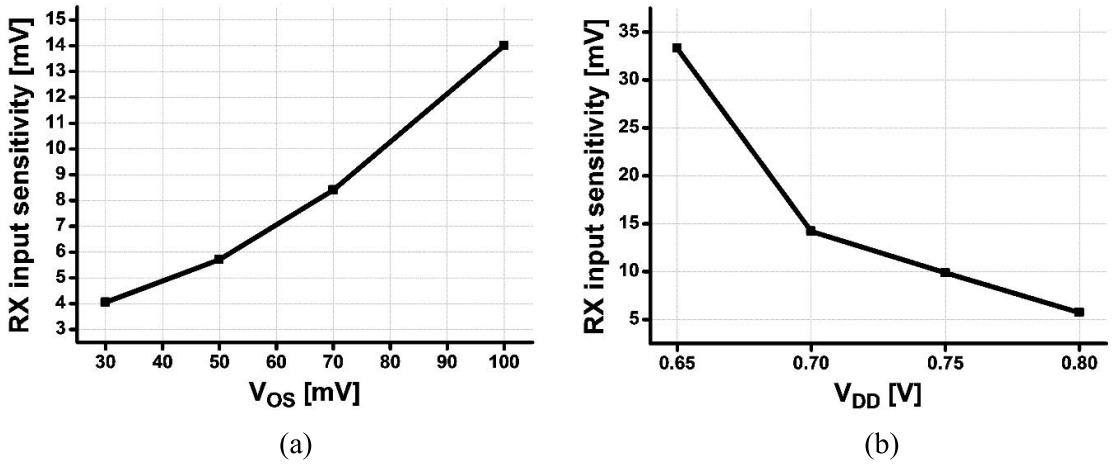

Fig. 13. Measured RX input sensitivity with 12.5 Gb/s versus (a) V_{OS} and (b) supply voltage.

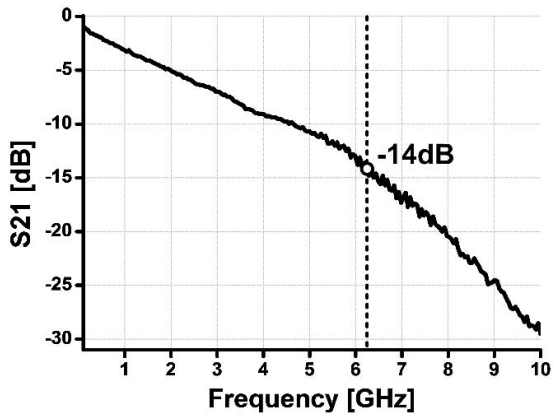

Fig. 14. Channel response of 15" FR-4.

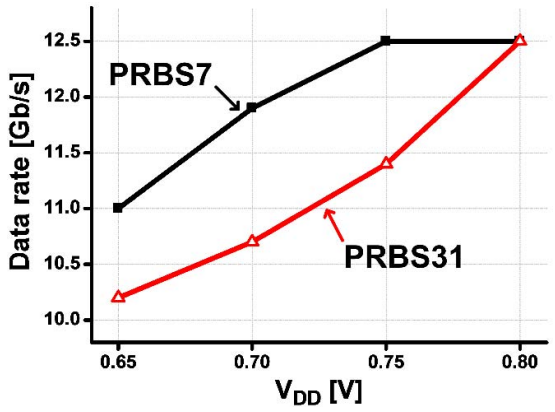

Fig. 15. Maximum operating data rate of RX with 15" FR-4 and 200-mV input versus supply voltage.

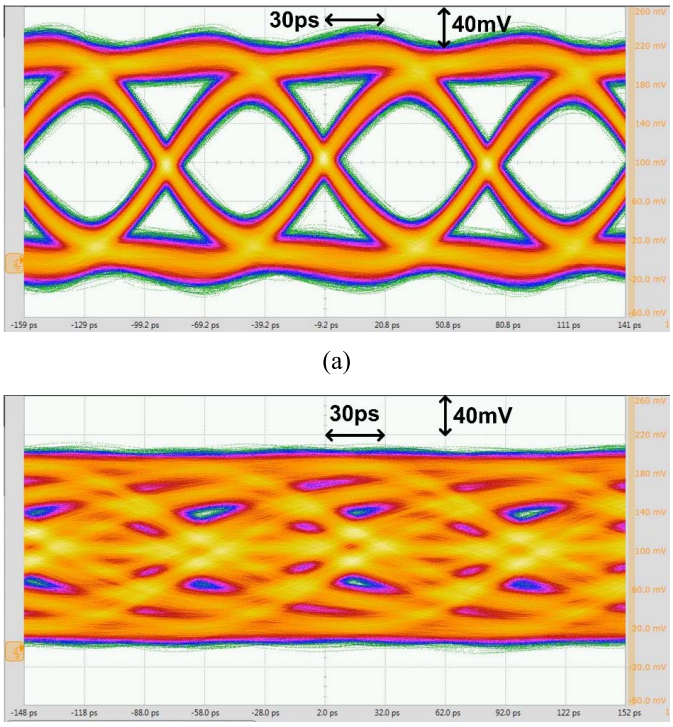

Fig. 16. Measured eye diagrams with 12.5-Gb/s PRBS31 and 15" FR-4. (a) TX output and (b) RX input.

differential RZ signals (FN, FP) to the DFE and the second stage SR latch. The second stage generates a nonreturn to zero (NRZ) output (D_{OUT}). When both inputs (OP, ON) are zero, two outputs (FP, FN) are pre-charged to V_{DD}. When the rising time of OP comes before ON, FP remains at V_{DD} and FN transitions to V_{SS}; this changes the output (D_{OUT}) to V_{DD}. When the rising time of ON comes before OP, FN remains at V_{DD} and FP transitions to V_{SS}; this changes the output (D_{OUT}) to V_{SS}.

The feedback loop delay for the 1st-tap DFE (the 1st-tap T_{FB}) is the sum of two delay times; one is the delay from TP0 to OP0 in Fig. 9(a), the other is the delay from OP to FN in Fig. 10. Similarly, the 2nd-tap T_{FB} is the sum of two delay times; one is the delay from CP0 to OP0 in Fig. 9(a), the other is the delay from OP to FN in Fig. 10. As shown in Section II, the 1st-tap T_{FB} is allowed up to 1.43 UI at 12.5 Gb/s in this paper. The worst case of the 1st-tap T_{FB}

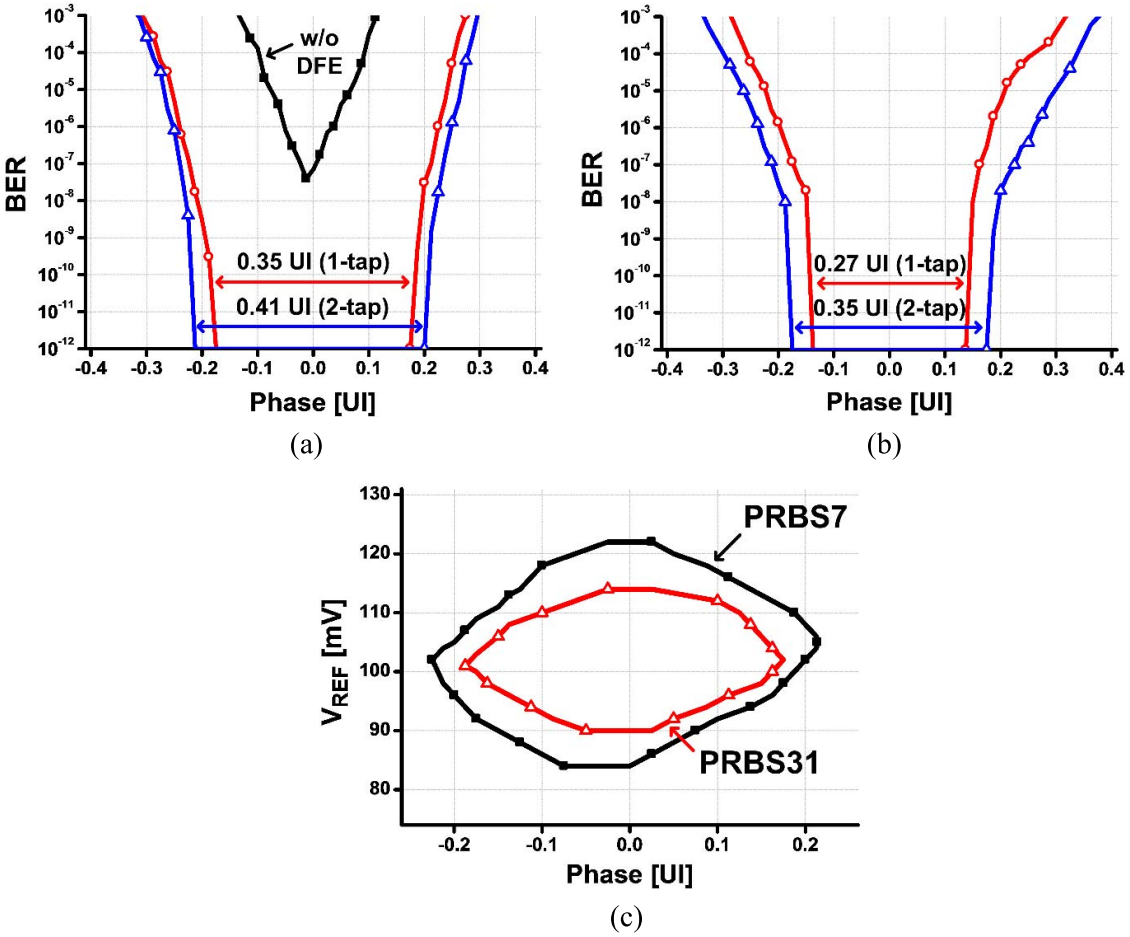

Fig. 17. Measured bathtub curves with 15" FR-4 and 12.5-Gb/s inputs of (a) PRBS7 and (b) PRBS31. (c) Measured on-chip eye diagram with 2-tap TB DFE with 12.5-Gb/s data and 15" FR-4.

corresponds to the 1st case of Table I. To verify that the 1st-tap T_{FB} of the worst case is less than 1.43 UI for proper DFE operation, a post-layout simulation is conducted with a channel of 14-dB loss at 6.25 GHz. An input of "101" is assumed to calculate the worst case for the 1st-tap T_{FB} (the 1st case of Table I); the current bit is "1," the 1st-tap bit is "0," and the 2nd-tap bit is "1" (the leftmost "1"). With this input, the timing margins for the 1st and the 2nd-tap T_{FB} are 0.15 and 0.06 UI, respectively, at 12.5 Gb/s according to the post-layout simulation; the timing margin corresponds to the difference between T_{FB} and the allowed T_{FB}. The small timing margin of 0.06 UI for the 2nd-tap T_{FB} is not a concern because a feedback failure of the 2nd-tap DFE helps increase the time difference at the input of the 1st-tap DFE.

IV. Measurement Results

The proposed transceiver chip was fabricated in a 65-nm CMOS process (Fig. 11). For both the bit error rate (BER) test and the eye measurement (Fig. 12), the TX and RX chips are located on a PCB, and they are connected through a 15" FR-4 microstrip line on the same PCB. In [11], the TX and RX chips are located on different PCBs, and they are connected through a 0.5" FR-4 microstrip line, a 1 m SMA cable, a 3" or a 12" FR-4 channel, and a 0.5" FR-4 microstrip line. A full-rate (12.5 Gb/s) PRBS data is supplied by a BER tester (J-BERT N4903A); the full-rate data is converted into two half-rate data [D_E, D_O of Fig. 6(a)] inside the TX chip. The BER tester supplies a half-rate clock to both the TX chip and a clock generator; the clock generator supplies a quarter-rate clock to the RX chip with an adjustable delay. To measure the RX input sensitivity, the BER tester supplied a full-rate PRBS7 data directly to the RX chip without going through either a TX chip or a channel. The RX input sensitivity refers to the minimum voltage eye opening at the RX input node with BER $<$ 1E-12. No DFE was used in the measurement. For V_{OS} of 30, 50, 70, and 100 mV at 12.5 Gb/s, the measured RX input sensitivity are 4, 5.7, 8.4, and 14 mV, respectively [Fig. 13(a)]; this is because the VTC gain decreases as Vos increases as shown in (2). The RX input sensitivity increases from 5.7 to 33.3 mV as the supply voltage is reduced from 0.8 to 0.65 V at V_{OS} of 50 mV and 12.5 Gb/s. [Fig. 13(b)]. To evaluate the performance of the TB DFE circuit in the RX chip, the maximum data rate with BER $<$ 1E-12 was measured for different values of supply voltage. In the measurement, full-rate PRBS7 and PRBS31 data were applied to the RX chip through a 15" FR-4 channel. The loss of the channel is 14 dB at 6.25 GHz [Fig. 14]. At the supply voltage larger than 0.65 V, the maximum data rate of the

TABLE II
PERFORMANCE COMPARISON OF LOW-SUPPLY TRANSCEIVER

	JSSC'08 [6]	JSSC'13 [5]	ISSCC'15 [4]	This work
Tech (nm)	65	65	65	65
Single-ended /Differential	Differential	Differential	Single-ended	Single-ended
Supply voltage (V)	0.85	0.8 / 0.75	0.7	0.8
Data rate (Gb/s)	10	8	6	12.5
Channel swing	100mVppd	200mVppd	200mVpp	200mVpp
Channel loss (dB)	7	8.4	-	14
Equalizer	CTLE	CTLE	-	2-tap DFE
Energy efficiency (pJ/b)	*3.6	*0.66	0.48 (*0.58)	0.49

* includes the multi-phase clock generation circuits

TABLE III
PERFORMANCE COMPARISON WITH DFE WORKS

	JSSC'09 [14]	JSSC'09 [15]	JSSC'12 [16]	ISSCC'14 [17]	JSSC'15 [18]	This work		
Data rate (Gb/s)	10	12	15	16	10	12.5		
Architecture	DFE + IIR	5-tap DFE	2-tap DFE	3-tap DFE	2-IIR+1-tap DFE	2-tap DFE		
Tech (nm)	65	45 SOI	45 SOI	65 GP	28 LP	65 GP		
Supply voltage (V)	1.0	1.0	1.2	0.7	1.0	0.75	0.8	
Channel swing	600mVppd	600mVppd	800mVppd	-	150mVppd	200mVpp		
Channel loss (dB)	23.2	15	14.5	18	24	14		
PRBS length	7	7	7	7	7	7	7	31
Eye opening	45%	32%	24%	46%	33%	33%	41%	35%
Energy efficiency (pJ/b)	0.68	0.91	0.5	0.25	0.41	0.19	0.22	

RX chip with the TB DFE exceeds 10 Gb/s [Fig. 15]. At the supply voltage of 0.75 V, the RX chip achieves 12.5 Gb/s with PRBS7 data; the timing margin (BER $<$ 1E-12) is 0.33 UI and the RX chip consumes 3.1 mA. At the supply voltage of 0.8 V, the maximum data rate exceeds the equipment (J-BERT) limit of 12.5 Gb/s. The transceiver including the TX and RX chips was measured with the setup of Fig. 12. The TX chip transmits a 12.5 Gb/s data with 200 mV dc swing [Fig. 16(a)] to the RX chip through a 15" FR-4 channel; the eye opening is closed at the RX input [Fig. 16(b)]. The bathtub curves and on-chip eye diagrams were measured at the RX input with PRBS7 and PRBS31 inputs. Without DFE, the bathtub curve shows no timing margin (BER $<$ 1E-12) for both cases. With the 2-tap DFE, the timing margin is 0.41 UI for the PRBS7 input [Fig. 17(a)], and 0.35 UI for the PRBS31 input [Fig. 17(b)]. For the PRBS7 input, the control codes of the 1st- and 2nd-tap DFE coefficients are 63 and 40 out of 127 (7-b binary); they are translated to $T_F = 34.6$ and 11 ps at 12.5 Gb/s in Fig. 9(b). For the PRBS31 input, they are 64 and 47 out of 127; the corresponding T_F are 36 and 14.7 ps at 12.5 Gb/s. The signal latency from the quarter-rate VTC clock to the quarter-rate NRZ outputs [D_{OUT}0–270 in Fig. 6(b)] varies from 394 to 470 ps; this variation is generated by the residual ISI and the uncompensated DFE delay due to the feedback failure. When sampling the quarter-rate NRZ outputs at the following stage, the variation of latency is reflected as jitter. However, the jitter is translated into an enough timing margin of $\pm$1.53 UI due to the quarter-rate clock scheme. The on-chip eye opening of 24 and 38 mV were measured for the PRBS31 and PRBS7 input, respectively [Fig.17(c)]. The TX and RX chips consume 4.3 and 3.4 mA of current at the supply voltage of 0.8 V. The energy efficiency of the transceiver is 0.49 pJ/b. Compared with low-supply transceiver circuits published in the literature, this paper achieves the highest data rate at the supply voltage below 0.85 V and a channel loss over 10 dB (Table II). Among DFE circuits, this paper shows the lowest energy efficiency (Table III).

V. CONCLUSION

To increase the maximum data rate of single-ended mobile DRAM interface, a TB RX circuit is proposed by eliminating

the g_m/C constraint of the conventional VB RX front-end circuit. The TB RX circuit consists of a VTC, a 2-tap TB DFE, and a time comparator. The VTC converts the RX input voltage to a time difference between the rising edges of two outputs of the VTC by using the difference in the clock-to-Q delay times between two latches with different input offset voltages. The TB DFE further increases the time difference between the rising edges of two outputs of the VTC to compensate ISI; this is achieved by inserting additional delay to one of two outputs of the VTC and bypassing the other output of the VTC without adding additional delay. The following time comparator makes a decision at the earlier rising edge of two outputs of the DFE. Because the VTC gain is inversely proportional to g_m/C, the VTC provides a large gain at low supply voltage, and improves the RX input sensitivity to 5.7 mV at 12.5 Gb/s. The TB DFE works properly with the feedback loop delay up to 1.43 UI in this paper; this greatly helps to increase the maximum data rate. The proposed transceiver chip was implemented in a 65-nm CMOS process. With the TB DFE, the RX chip achieves the data rate of 12.5 Gb/s through a 15" FR-4 channel with 14-dB loss at the supply voltage of 0.75 V. The TX and RX chips consume 4.3 and 3.4 mA at 0.8 V. The energy efficiency is 0.49 pJ/b.

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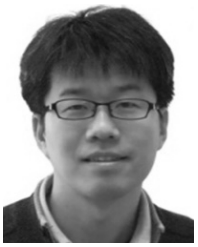

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