Patent Abstracts

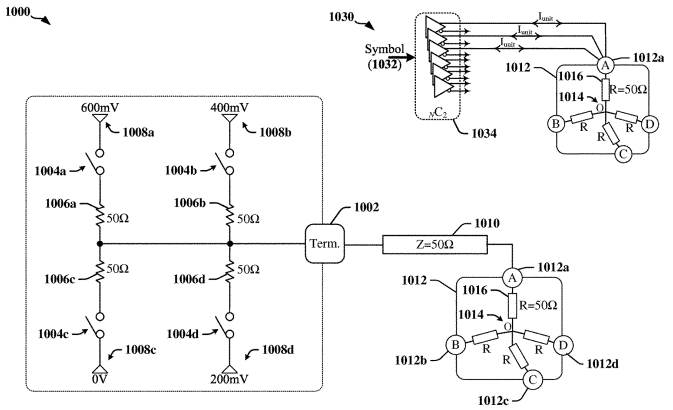
The Patent Abstracts cited are intended to provide the minimum information necessary for determining interest. The full text and images can be obtained from the U.S. Patent Office at http://www.uspto.gov.

9,710,412 July 18, 2017

N-Factorial Voltage Mode Driver

Inventors: Shoichiro Sengoku (San Diego, CA)
Assignee: Qualcomm Incorporated (San Diego, CA)
Filed: May 15, 2014

Abstract— System, methods and apparatus are described that provide an N-factorial (N!) voltage-mode driver. A method communicating on an N! interface includes encoding data in a symbol to be transmitted over the N wires of the interface, and for each wire of the N wires, calculating a resultant current for the wire by summing current flows defined for two or more two-wire combinations that include the wire, and coupling a switchable voltage source to the each wire. Each bit in the symbol defines a current flow between a pair of the N wires that is one of a plurality of possible two-wire combinations of the N wires. The switchable voltage source may be selected from a plurality of switchable voltage sources in order to provide a current in the each wire that is proportionate to the resultant current calculated for the each wire.

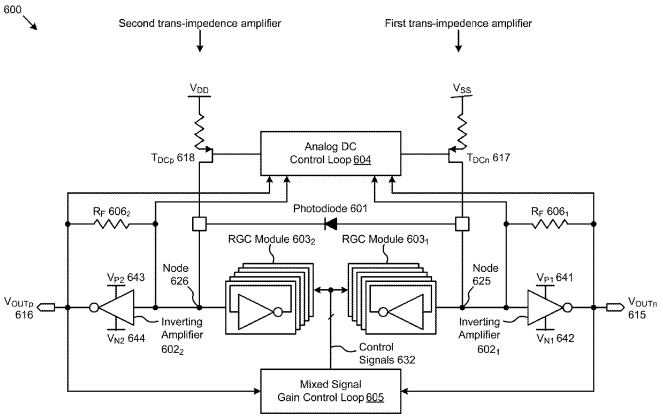


9,716,480 July 25, 2017

Trans-Impedance Amplifier With Replica Gain Control

Inventors: James Lawrence Gorecki (Santa Clara, CA) and Irene Quek (Santa Clara, CA)
Assignee: Inphi Corporation (Santa Clara, CA)
Filed: September 19, 2016

Abstract— This disclosure relates to the field of amplifiers for multi-level optical communication and more particularly to techniques for trans-impedance amplifiers (TIA) with gain control. The claimed embodiments address the problem of implementing a low cost TIA that exhibits high linearity, low noise, low power, and wide bandwidth. More specifically, some claims are directed to approaches for providing TIA gain control using a plurality of inverter-based replica gain control cells controlled by a feedback loop to manage the current into the amplifying output stage and thereby the TIA output voltage.

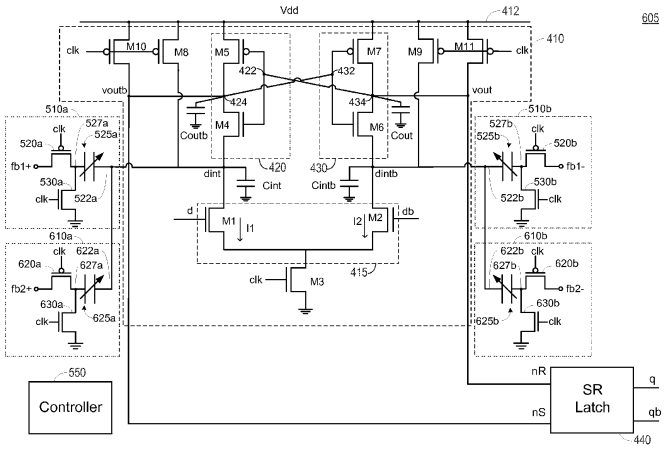


9,722,828 August 1, 2017

Switch Capacitor Decision Feedback Equalizer With Internal Charge Summation

Inventors: Li Sun (San Diego, CA), Xiaohua Kong (San Diego, CA), Zhi Zhu (San Diego, CA), Miao Li (San Marcos, CA), and Dong Ren (San Diego, CA)
Assignee: Qualcomm Incorporated (San Diego, CA)
Filed: September 23, 2015

Abstract— In one embodiment, a receiver comprises a latch configured to receive a data signal and to latch symbols of the received data signal, and a decision feedback equalizer



Digital Object Identifier 10.1109/JSSC.2017.2788258

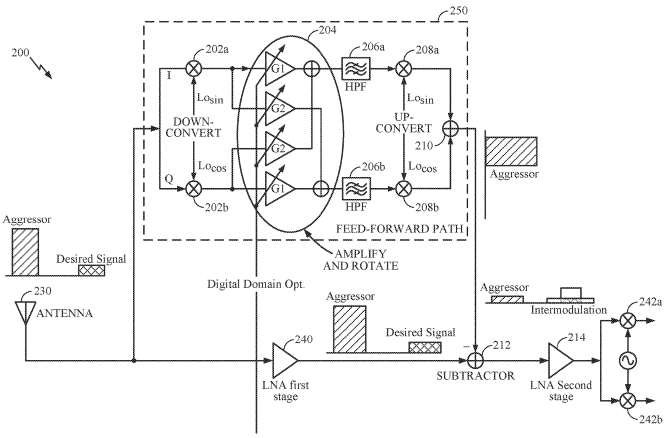
comprises a first feedback capacitor having first and second terminals, the first terminal being coupled to a first internal node of the latch. The decision feedback equalizer also comprises a first plurality of switches configured to alternatively couple the second terminal of the first feedback capacitor to a first feedback signal and a ground, the first feedback signal having a first voltage that is a function of a bit decision corresponding to a first previous symbol in the data signal preceding a current symbol in the data signal.

9,729,179 August 8, 2017

Feed-Forward Interference Cancellation in a Receiver

Inventors: Mohammad Emadi (San Jose, CA), Mazhareddin Taghivand (Campbell, CA), and Yann Ly-Gagnon (San Francisco, CA)
Assignee: Qualcomm Incorporated (San Diego, CA)
Filed: June 23, 2016

Abstract—Systems and methods for interference cancellation in a receiver of wireless signals include receiving a signal comprising an aggressor and a desired signal. The received signal is amplified in a low noise amplifier (LNA) to generate an amplified received signal. The aggressor is extracted from the received signal in a feed-forward path between an input of the LNA and an output of the LNA, to generate an extracted aggressor and the extracted aggressor is subtracted from the amplified received signal to provide the desired signal. An amplify and rotate block in the feed-forward path is used to align a phase of the aggressor to a phase of the amplified received signal in order to enable the subtraction.

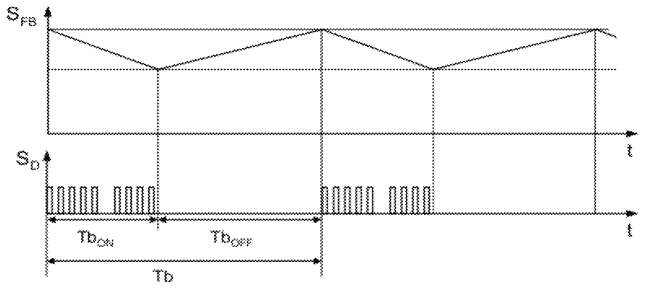


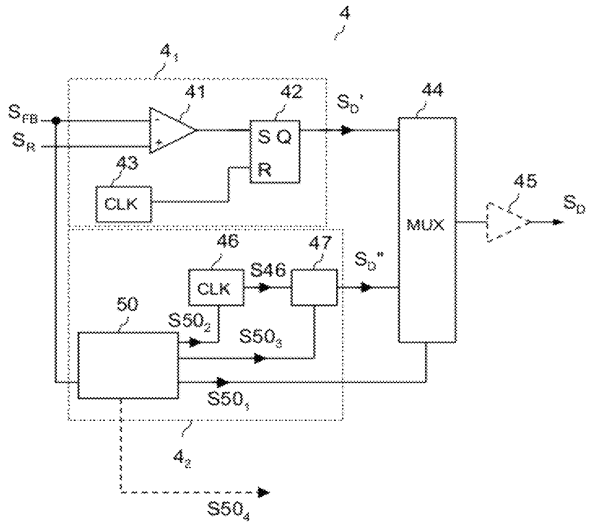
9,735,673 August 15, 2017

Burst-Mode Operation of a Switching Converter

Inventors: Siu Kam Kok (Sims Ville, SG), Mingping Mao (Singapore, SG), and Xiaowu Gong (Singapore, SG)
Assignee: Infineon Technologies AG (Neubiberg, DE)
Filed: March 30, 2011

Abstract—In accordance with an embodiment, a method of driving a switching element in a switching converter includes generating a feedback signal that is dependent on the output voltage, driving the switching element in a plurality of subsequent burst cycles, determining a burst frequency, and adjusting an effective switching frequency in at least one burst cycle dependent on the determined burst frequency. Each burst cycle includes a burst-on period and a subsequent burst-off period, and determining the burst frequency includes evaluating a duration of at least one burst cycle.



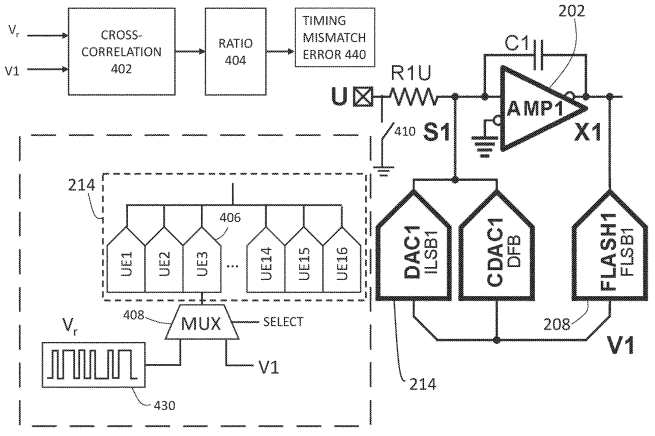


9,735,797 August 15, 2017

Digital Measurement of DAC Timing Mismatch Error

Inventors: Jialin Zhao (Santa Clara, CA), Qingdong Meng (Belmont, MA), Yunzhi Dong (Weehawken, NJ), and Jose Barreiro Silva (Bedford, MA)
Assignee: Analog Devices, Inc. (Norwood, MA)
Filed: November 23, 2016

Abstract—For analog-to-digital converters (ADCs) which utilize a feedback digital-to-analog converter (DAC) for conversion, the final analog output can be affected or distorted by errors of the feedback DAC. A digital measurement technique can be implemented to determine timing mismatch error for the feedback DAC in a continuous-time delta-sigma modulator (CTDSM) or



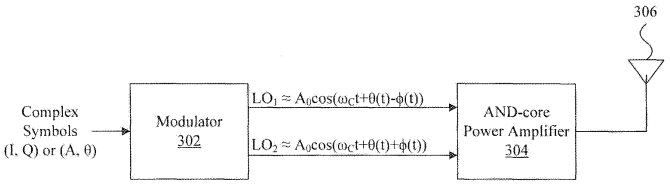
in a continuous-time pipeline modulator. The methodology utilizes cross-correlation of each DAC unit elements (UEs) output to the entire modulator output to measure its timing mismatch error respectively. Specifically, the timing mismatch error is estimated using a ratio based on a peak value and a value for the next tap in the cross-correlation function. The obtained errors can be stored in a look-up table and fully corrected in digital domain or analog domain.

9,742,367 August 22, 2017

Outphasing Transmitter Systems and Methods

Inventors: Alex Ahmad Mirzaei (Irvine, CA) and Hooman Darabi (Laguna Niguel, CA)
Assignee: Avago Technologies General IP (Singapore) Pte. Ltd. (Singapore, SG)
Filed: July 29, 2015

Abstract— The present disclosure is directed to a system and method for performing the outphasing technique without using a combiner at the output of two power amplifiers to reduce loss and distortions.

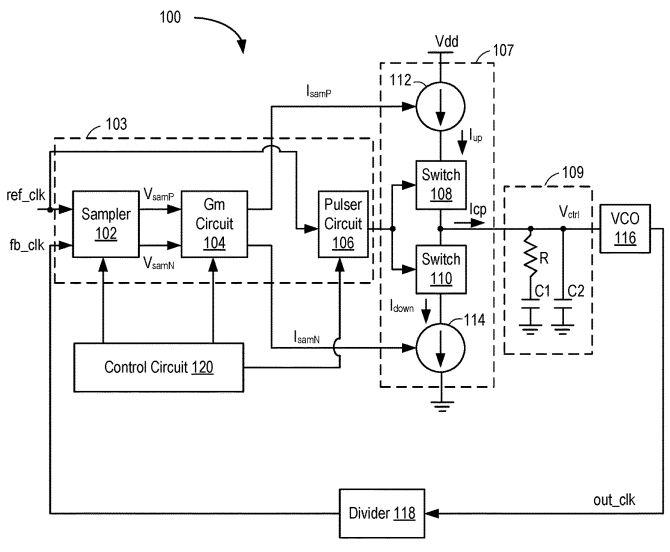


9,742,380 August 22, 2017

Phase-Locked Loop Having Sampling Phase Detector

Inventors: Mayank Raj (San Jose, CA), Parag Upadhyaya (Los Gatos, CA), and Adebabay M. Bekele (San Jose, CA)
Assignee: Xilinx, Inc. (San Jose, CA)
Filed: June 1, 2016

Abstract— An example a phase-locked loop (PLL) circuit includes a sampling phase detector configured to receive a reference clock and a feedback clock and configured to supply a first control current and a pulse signal. The PLL further includes a charge pump configured to generate a second control current based on the first control current and the pulse signal. The PLL further includes a loop filter configured to filter the second control current and generate an oscillator control voltage. The PLL further includes a voltage controlled oscillator (VCO) configured to generate an output clock based on the oscillator control voltage. The PLL further includes a frequency divider configured to generate the reference clock from the output clock.

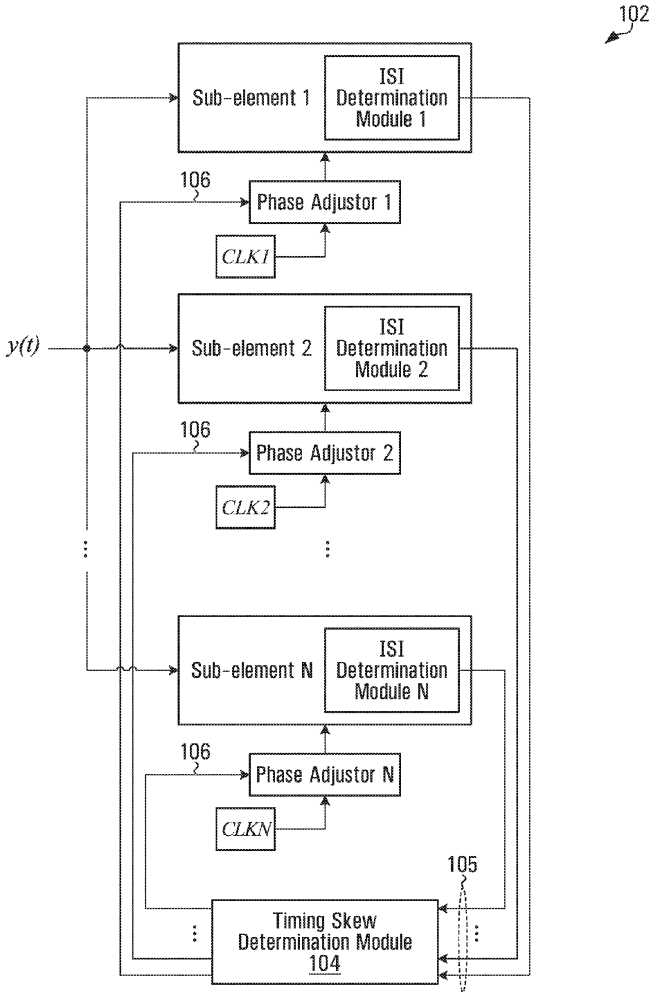


9,742,594 August 22, 2017

System and Method for Adjusting Clock Phases in a Time-Interleaved Receiver

Inventors: Stephane Dallaire (Gatineau, CA) and Benjamin Smith (Ottawa, CA)
Assignee: Inphi Corporation (Santa Clara, CA)
Filed: December 7, 2016

Abstract— Clock timing skew may occur during operation of a time-interleaved receiver. It would be beneficial to try to determine if there is timing skew, and if there is, then address it, such as by reducing or eliminating some or all of the timing skew. Embodiments are described herein that may achieve this. In one embodiment, a method includes generating at least two clocks having the same frequency but a different phase. Intersymbol interference (ISI) values are then determined, one for each of the clocks, by: for each clock, sampling a signal using the clock and determining a value representing ISI based on the sampled signal. A clock phase of at least one of the clocks is adjusted in response to at least one of the ISI values being different from a reference ISI value.

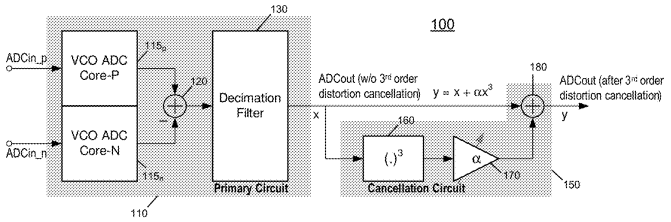


9,748,963 August 29, 2017

Reducing Distortion in an Analog-to-Digital Converter

Inventors: Abdulkerim L. Coban (Austin, TX) and Mustafa H. Koroglu (Austin, TX)
Assignee: Silicon Laboratories Inc. (Austin, TX)
Filed: June 21, 2016

Abstract—In one embodiment, an apparatus includes: a first voltage controlled oscillator (VCO) analog-to-digital converter (ADC) unit to receive a first portion of a differential analog signal and convert the first portion of the differential analog signal into a first digital value; a second VCO ADC unit to receive a second portion of the differential analog signal and convert the second portion of the differential analog signal into a second digital value; a combiner to form a combined digital signal from the first and second digital values; a decimation circuit to receive the combined digital signal and filter the combined digital signal into a filtered combined digital signal; and a cancellation circuit to receive the filtered combined digital signal and generate a distortion cancelled digital signal, based at least in part on a coefficient value.

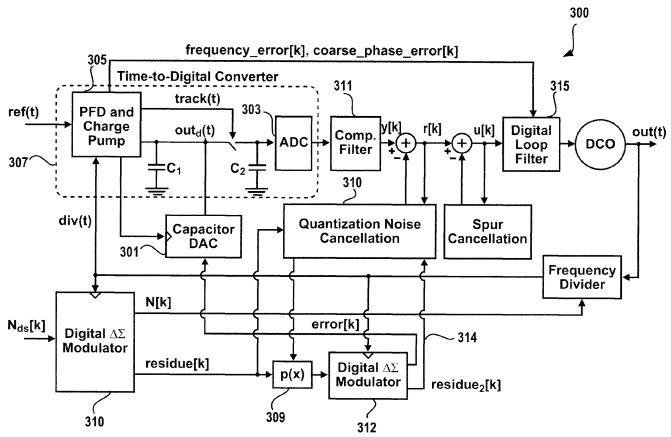


9,762,250 September 12, 2017

Cancellation of Spurious Tones Within a Phase-Locked Loop With a Time-To-Digital Converter

Inventors: Michael H. Perrott (Nashua, NH)
Assignee: Silicon Laboratories Inc. (Austin, TX)
Filed: July 31, 2014

Abstract—A phase-locked loop (PLL) includes a spur cancellation circuit that receives a residue signal indicative of a first frequency and receives a residual phase error signal and generates a spur cancellation signal. A summing circuit combines the spur cancellation signal and a first phase error signal corresponding to a phase difference between a reference signal and a feedback signal in the PLL and generates a second phase error signal with a reduced spurious tone at the first frequency.

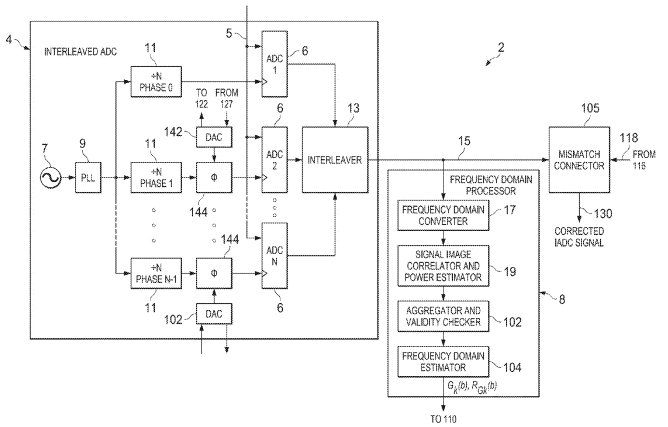


9,762,254 September 12, 2017

Continuous Tracking of Mismatch Correction in Both Analog and Digital Domains in an Interleaved ADC

Inventors: Sashidharan Venkatraman (Hyderabad, IN), Sthanunathan Ramakrishnan (Bangalore, IN), and Jaiganesh Balakrishnan (Bangalore, IN)
Assignee: Texas Instruments Incorporated (Dallas, TX)
Filed: August 8, 2016

Abstract—A system includes a first tracking filter configured to track a frequency domain mismatch profile between component analog-to-digital convertors (ADCs) of an interleaved ADC (IADC), and a second tracking filter configured to a track a frequency independent timing delay mismatch and a timing delay mismatch correction error based on frequency domain mismatch profile estimates. An output of the first tracking filter determines a correction of a frequency dependent mismatch profile in an output of the interleaved ADC and an output of the second tracking filter determines a correction of the timing delay mismatch correction error in the output of the interleaved ADC.

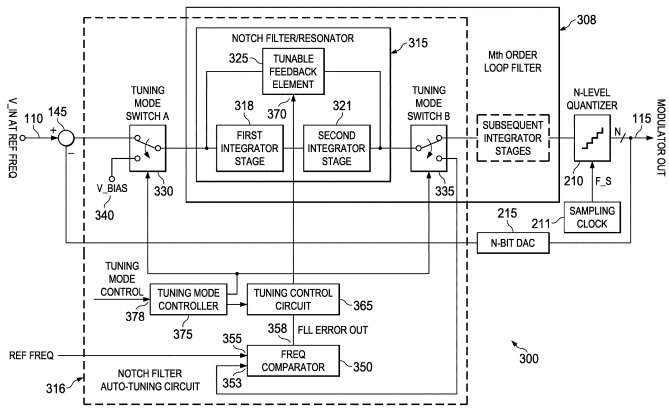


9,762,259 September 12, 2017

Sigma-Delta Analog-To-Digital Converter With Auto Tunable Loop Filter

Inventors: Xiao Pu (Plano, TX), Krishnaswamy Nagaraj (Plano, TX), and Peng Cao (Richardson, TX)
Assignee: Texas Instruments Incorporated (Dallas, TX)
Filed: January 9, 2017

Abstract—A notch filter in a sigma-delta modulator loop filter increases SNR by limiting in-band quantization noise around a frequency to which the notch filter is precisely tuned. A tuning mode controller isolates the notch filter from other loop filter stages. A bias voltage is applied to the notch



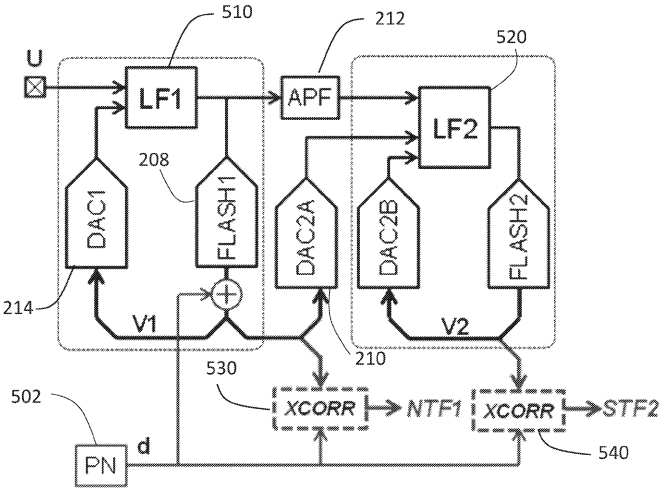
filter, causing it to resonate. Tuning mode switches insert the notch filter into a frequency-locked loop ("FLL") circuit as a variable frequency oscillator component of the FLL. An ADC operational mode input signal is applied to the FLL as a reference signal. A tuning control component of the FLL adjusts a tunable feedback element in the notch filter to drive the FLL error signal to zero in order to precisely tune the notch filter to the center frequency of the ADC input signal. Tuning inputs to the tunable feedback element are then latched prior to re-inserting the notch filter into the modulator.

9,768,793 September 19, 2017

Adaptive Digital Quantization Noise Cancellation Filters for Mash ADCs

Inventors: Qingdong Meng (Belmont, MA), Hajime Shibata (Toronto, CA), Richard E. Schreier (New Castle, CA), Martin Steven McCormick (Cambridge, MA), Yunzhi Dong (Weehawken, NJ), Jose Barreiro Silva (Bedford, MA), Jialin Zhao (Santa Clara, CA), Donald W. Paterson (Winchester, MA), and Wenhua W. Yang (Lexington, MA)
Assignee: Analog Devices Global (Hamilton, BM)
Filed: November 30, 2016

Abstract—For continuous-time multi-stage noise shaping analog-to-digital converters (CT MASH ADCs), quantization noise cancellation often requires accurate estimation of transfer functions, e.g., a noise transfer function of the front end modulator and a signal transfer function of the back end modulator. To provide quantization noise cancellation, digital quantization noise cancellation filters adaptively tracks transfer function variations due to integrator gain errors, flash-to-DAC timing errors, as well as the inter-stage gain and timing errors. Tracking the transfer functions is performed through the direct cross-correlation between the injected maximum length linear feedback shift registers (LFSR) sequence and modulator outputs and then corrects these non-ideal effects by accurately modeling the transfer functions with programmable finite impulse response (PFIR) filters.

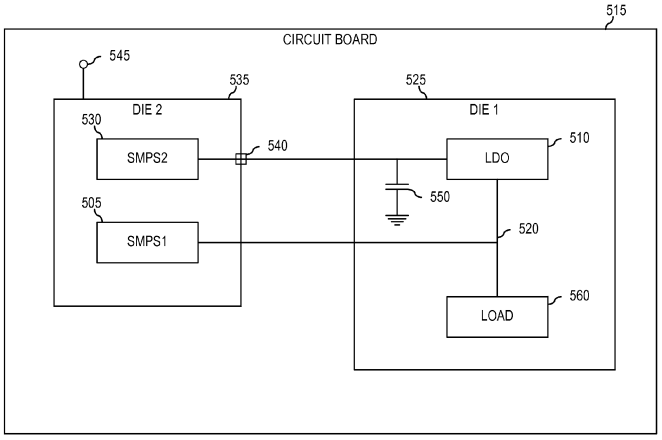


9,785,222 October 10, 2017

Hybrid Parallel Regulator and Power Supply Combination for Improved Efficiency and Droop Response With Direct Current Driven Output Stage Attached Directly to the Load

Inventors: James Thomas Doyle (Carlsbad, CA), Zhengming Fu (San Diego, CA), Farsheed Mahmoudi (San Diego, CA), Amirali Shayan Arani (San Diego, CA), and Nazanin Darbanian (San Diego, CA)
Assignee: Qualcomm Incorporated (San Diego, CA)
Filed: December 22, 2014

Abstract—Operational mode changes in a system-on-a-chip (SoC) integrated circuit in a complex device such as a mobile phone cause spikes in current demand which can cause voltage droops that disrupt operation of the SoC. A hybrid parallel power supply connects a switching-mode power supply and a low-dropout voltage regulator in parallel to provide high efficiency and fast response times. Integration of the voltage regulator on the SoC reduces parasitic impedance be between the voltage regulator and the load to aid in reducing voltage droops. The switching-mode power supply and the low-dropout voltage regulator can regulate their outputs to slightly difference voltage levels. This can allow the switching-mode power supply to supply most of the SoC's current demands.

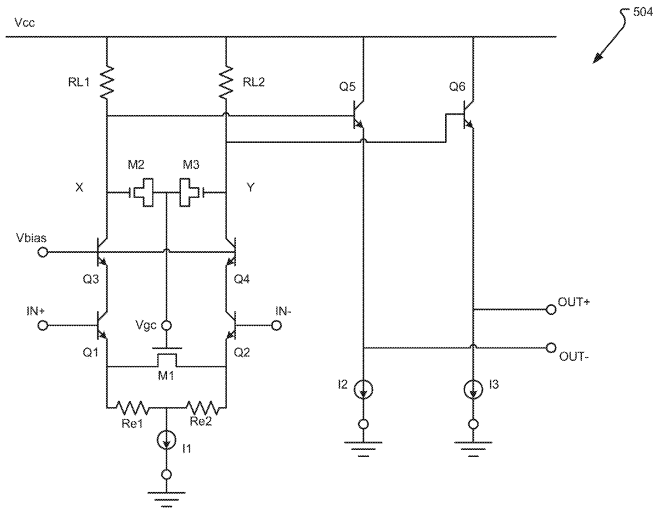


9,787,272 October 10, 2017

Linearizing and Reducing Peaking Simultaneously in Single-to-Differential Wideband Radio Frequency Variable Gain Trans-Impedance Amplifier (TIA) for Optical Communication

Inventors: Chakravartula Nallani (San Jose, CA), Rahul Shringarpure (San Jose, CA), Georgios Asmanis (Lake Forest, CA), Faouzi Chaahoub (San Jose, CA), and Kishan Venkataramu (Santa Clara, CA)
Assignee: Avago Technologies General IP (Singapore) Pte. Ltd. (Singapore, SG)
Filed: October 30, 2015

Abstract—An amplifier, a circuit, and an optical communication system are provided. The disclosed amplifier may include a first transistor receiving



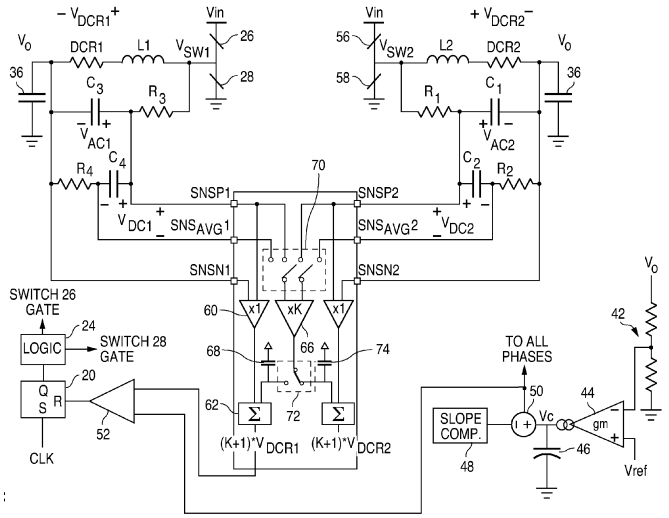
a first portion of an input signal received at the amplifier, a second transistor receiving a second portion of the input signal, an automatic gain control signal that is dynamically adjustable in response to variations in an output of the amplifier, and a varactor that has its capacitance adjusted by changes in the automatic gain control signal and, as a result, adjusts a position of a pole in a transfer function of the amplifier.

9,793,800 October 17, 2017

Multiphase Switching Power Supply With Robust Current Sensing and Shared Amplifier

Inventors: Yingyi Yan (Fremont, CA) and Yi Ding Gu (Pleasanton, CA)
Assignee: Linear Technology Corporation (Milpitas, CA)
Filed: April 4, 2017

Abstract— In a multiphase, current mode controlled switching power supply, current through the inductors in the various phases is sensed to determine when to turn off the switching transistors. An AC current feedback path, sensing the ramping ripple current, is separate from the DC current path, sensing the lower frequency average current. A shared differential amplifier has its inputs multiplexed to receive only the DC component signals from all the phases. The gain of the amplifier is set so that the DC sense signal has the proper proportion to the AC sense signal. The output of the amplifier is sampled and held for each phase using a second multiplexer. The AC sense signal and the amplified DC sense signal, for each phase, are combined by a summing circuit. The composite sense signal is applied to a comparator for each phase to control the duty cycle of the associated switch.

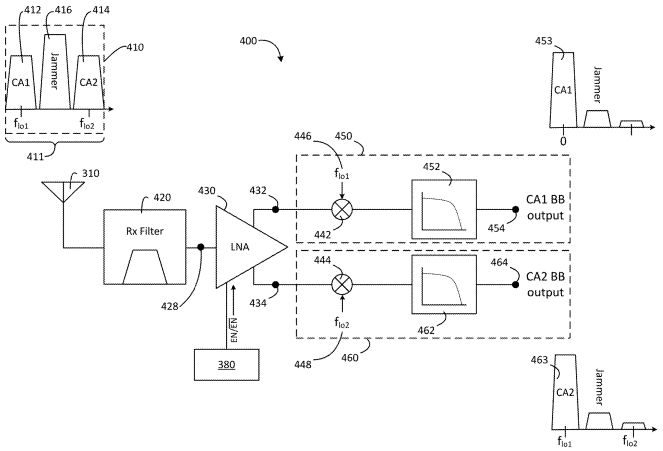


9,800,273 October 24, 2017

Wideband High Linearity LNA With Intra-Band Carrier Aggregation Support

Inventors: Sherif Abdelhalem (San Diego, CA), Bassel Hanafi (San Diego, CA), and Hasnain Lakdawala (San Diego, CA)
Assignee: Qualcomm Incorporated (San Diego, CA)
Filed: March 1, 2017

Abstract— A device and method for amplifying signals is provided. The device can have an input to receive an input signal having a first desired signal on a first carrier, a second desired signal on a second carrier, and one or more interfering signals. The device can have a first carrier aggregation (CA) chain for use with the first desired signal and a second CA chain for use with the second desired signal. The first and second CA chains can be coupled to the input. The first and second CA chains can have a plurality of transconductance stages. Each of the transconductance stages can be configured as a high impedance stage or a low impedance stage. The transconductance stages can be selectively activated to incrementally adjust the transconductance, and therefore the input impedance, of each of the CA chains.

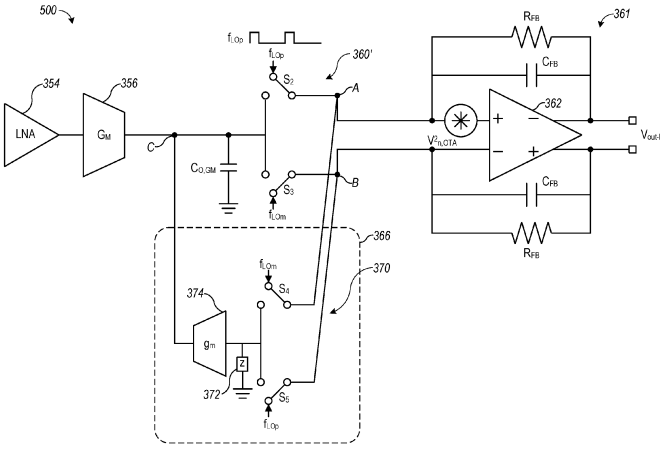


9,800,280 October 24, 2017

Noise Suppression in Radio Frequency Receivers

Inventors: Hajir Hedayati (San Diego, CA), Milad Darvishi (San Diego, CA), and Jeremy Dunworth (La Jolla, CA)
Assignee: Qualcomm Incorporated (San Diego, CA)
Filed: June 7, 2016

Abstract— A radio frequency (RF) receiver device may include a receive path including a first amplifier. The device also includes a first mixer coupled to an output of the first amplifier and to an input of a second amplifier. Further, the device may include an auxiliary path including a second mixer coupled between an output of the first mixer and an input of the first mixer.

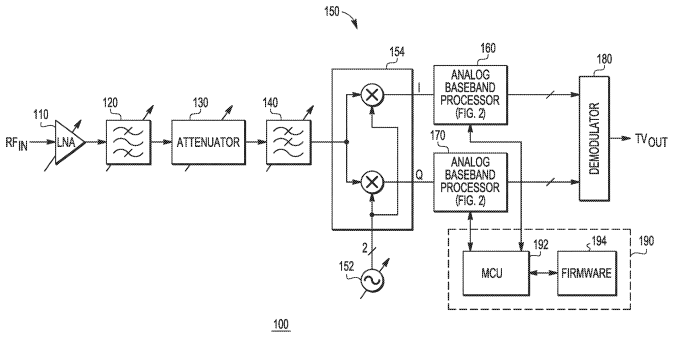


9,800,281 October 24, 2017

Signal Processor Suitable for Low Intermediate Frequency (LIF) or Zero Intermediate Frequency (ZIF) Operation

Inventors: Abdulkerim L. Coban (Austin, TX), Alessandro Piovaccari (Austin, TX), Ramin K. Poorfard (Austin, TX), and James T. Kao (Los Gatos, CA)
Assignee: Silicon Laboratories Inc. (Austin, TX)
Filed: March 28, 2017

Abstract— A signal processor for a radio frequency (RF) receiver includes a signal processing path having first and second programmable gain amplifiers and first and second offset correction circuits. The first offset correction circuit receives a first digital offset correction word and corrects a first offset of the first programmable gain amplifier by adding a first value corresponding to the first digital offset correction word to an input of the first programmable gain amplifier. The second offset correction circuit receives a second digital offset correction word and corrects a second offset of the second programmable gain amplifier by adding a first value corresponding to the second digital offset correction word to an input of the second programmable gain amplifier. A controller measures offsets of the first and second programmable gain amplifiers during a calibration, and provides the first and second offset correction words in response to the offsets.

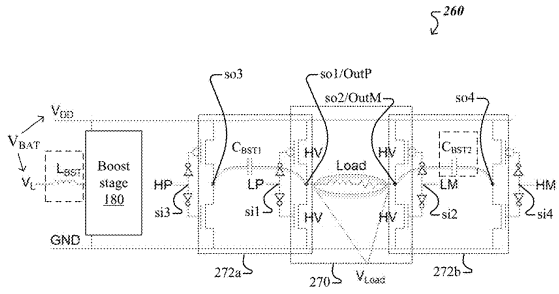


9,806,682 October 31, 2017

Multilevel Class-D Amplifiers

Inventors: Bruno Marcone (Mezzanino, IT) and Francesco Rezzi (Cava Manara, IT)
Assignee: Marvell International Ltd. (Hamilton, BM)
Filed: February 22, 2016

Abstract— Implementations of a class-D amplifier can be used to amplify an input analog signal and provide to a load a multilevel amplified signal having an amplitude larger than a voltage level of a power source used by the class-D amplifier.



if V_L=V_{BAT}, then V_{DD}=V_{BST}; OR
if V_L=N/A, then V_{DD}=V_{BAT}

9,806,727 October 31, 2017

Integrated Circuit Having a Clock Deskew Circuit That Includes an Injection-Locked Oscillator

Inventors: Marko Aleksi (Mountain View, CA) and Brian S. Leibowitz (San Francisco, CA)
Assignee: Rambus Inc. (Sunnyvale, CA)
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Abstract— Methods and apparatuses featuring an injection-locked oscillator (ILO) are described. In some embodiments, an ILO can have multiple injection points and a free-running frequency that is capable of being adjusted based on a control signal. In some embodiments, each injection point of an ILO can correspond to a phase tuning range. In some embodiments, a circuit can include circuitry to detect a phase boundary between two adjacent phase tuning ranges. In some embodiments, a circuit can use the detected phase boundary to switch between the two adjacent phase tuning ranges.