

# A 512-Gb 3-b/Cell 64-Stacked WL 3-D-NAND Flash Memory

Chulbum Kim, Doo-Hyun Kim, Woopyo Jeong, Hyun-Jin Kim, Il Han Park, Hyun-Wook Park, JongHoon Lee, JiYoon Park, Yang-Lo Ahn, Ji Young Lee, Seung-Bum Kim, Hyunjun Yoon, Jae Doeg Yu, Nayoung Choi, NaHyun Kim, Hwajun Jang, JongHoon Park, Seunghwan Song, YongHa Park, Jinbae Bang, Sanggi Hong, Youngdon Choi, Moo-Sung Kim, Hyunggon Kim, Pansuk Kwak, Jeong-Don Ihm, Dae Seok Byeon, Jin-Yub Lee, Ki-Tae Park, and Kye-Hyun Kyung

**Abstract**—A 64-word-line-stacked 512-Gb 3-b/cell 3-D NAND flash memory is presented. After briefly examining the challenges that occur to a stack, several technologies are suggested to resolve the issues. For performance enhancement, a novel program method hiding two-page data loading time is presented. This paper also discusses an electrical annealing improving reliability characteristic by removing holes in shallow traps. In addition, a valley tracking read for reducing timing overhead at a read retry is introduced by fast finding optimal read levels. Finally, a high-speed self-test mode for IO operation is presented. The chip, designed with the fourth generation of V-NAND technology, achieved an areal density of 3.98 Gb/mm<sup>2</sup> and operated up to 1 Gb/s at 1.2 V.

**Index Terms**—3-bit per cell, 3-D NAND, 64 word-line(WL) stack, cache program, error correction, NAND flash memory, reliability, self IO test, V-NAND.

## I. INTRODUCTION

THE advent of emerging technologies, such as cloud computing, big data, the Internet of Things, and mobile computing, is producing tremendous amount of data. In the era of big data, storage devices with versatile characteristics are required for ultra-fast processing, higher capacity storage, lower cost, and lower power operation. NAND flash memory itself and solid state disks employing NAND flash memory are great solutions to these storage applications. However, the difficulty of shrinking cell structure in the conventional planar NAND has slowed annual bit growth. On the contrary, the sizes of the memory array using the 3-D NAND technology have nearly doubled every year [1], [2], since the first mass productive chip employing the 3-D NAND technology is introduced for the first time in 2014 [3]. Fig. 1 compares the areal bit density (Gb/mm<sup>2</sup>) of the NAND flash devices published in the ISSCC from 2011 to 2016 [1]–[13]. The areal bit density of the planar NAND has increased annually by 26%; however, the 3-D NAND has increased its areal bit density annually by 50%. This shows that the 3-D NAND technology is a breakthrough

Manuscript received April 19, 2017; revised June 17, 2017; accepted July 15, 2017. Date of publication August 15, 2017; date of current version December 26, 2017. This paper was approved by Guest Editor Takashi Kono. (*Corresponding author: Chulbum Kim.*)

The authors are with Flash Product and Technology, Memory Business, Samsung Electronics Company, Ltd., Hwaseong 445-701, South Korea (e-mail: irontg@gmail.com).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2017.2731813

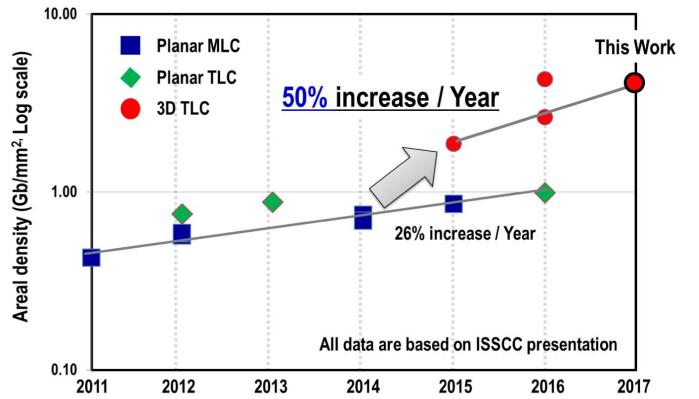


Fig. 1. Annual bit growth trend between 2-D NAND and 3-D NAND.

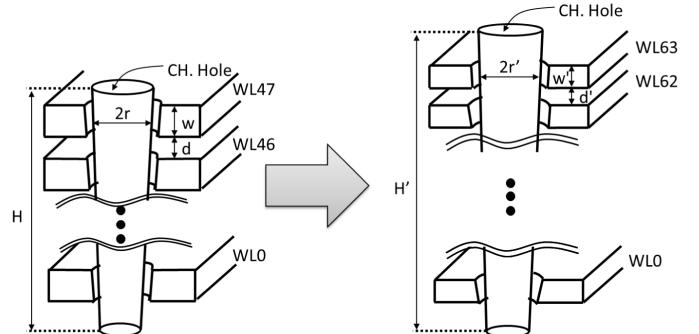


Fig. 2. WL stacking method in the 3-D NAND technology.

technology, changing the annual bit growth slope of the NAND flash memory.

As the generation of the 3-D NAND evolves, the way to increase the array area efficiency has been to vertically stack more and more word-lines (WLs). The high aspect ratio etching required for the 3-D NAND has limited the reduction in the diameter and space of the channel hole. As a result, increasing array efficiency has been restricted by the etching technology. Fig. 2 shows the WL stacking method for the increasing array area efficiency in the 3-D NAND technology. To alleviate etching difficulty, it is essential to shrink the gate structure vertically to minimize the total height. However, due to the vertical scaling, the following serious problems occur: 1) as the thickness of WL is decreases, the resistance of WLs increases; 2) as the space between WLs decreases,

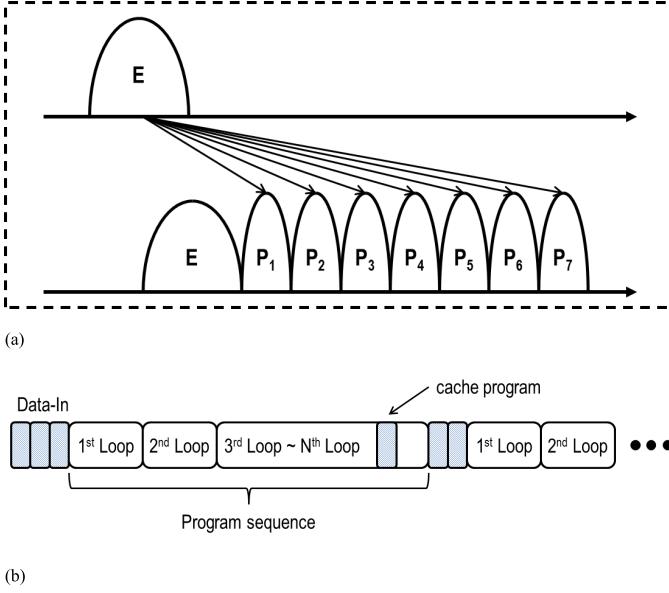


Fig. 3. (a) HSP used in 3-D NAND. (b) Conventional cache program in 3-D NAND.

the coupling capacitance increases; 3) the interference between adjacent WLs becomes large; and 4) cell reliability deteriorates due to the short-channel effect and lateral spreading [14].

To tackle these issues, this paper presents novel techniques for improving programming speed, enhancing reliability, and reducing overhead during error correction in Section II. Next, a high-speed IO built-in self-test (BIST) technique and a 1.2 VCCQ IO technique are introduced in Section III. The architecture and features of the fabricated chip are in Section IV. Finally, key parameter comparison with the previous 3-D NAND products and the conclusion of this paper is presented in Section V.

## II. PERFORMANCE IMPROVEMENT TECHNIQUES

### A. First Two-Loop Program With Data Loading

3-D NAND uses a 3-bit high-speed program (HSP) that programs three pages at a time to enhance program throughput, because the coupling effects between adjacent WL's cells are negligible. Thus, 3-bit HSP starts program operation after receiving three consecutive data loadings. Fig. 3 shows a concept of the HSP and a cache program scheme used in the 3-D NAND.

In the existing cache program [15], caching data were not possible at the start of program operation, because all latches were occupied by user data at that time. For instance, for a 3-b/cell, an empty latch is available when a program operation is performed, and several of total seven states are programmed and terminated. At this point, users can load data from the first of the next three pages, and the data loading can work simultaneously with program operation.

We propose a first two-loop program with a data loading technique. In this scheme, the first loop of the 3-bit HSP begins immediately after the first page data load completes. The second page data can be loaded while the first loop of the program operation. Two cases arise, because the operating

time of the first loop is fixed, while the data loading time is variable depending on the user's conditions, such as IO bandwidth and IO control between NAND chips. Fig. 4 shows a comparison between two cases. Case 1 is a case where the data loading time of a page is shorter than the operating time of the first and second loops. Case 2 is the opposite case, where the data loading time of a page is longer than the operating time of the first and second loops. For case 1, the second loop of program operation starts immediately at the end of the first loop. On the other hand, in case 2, the second loop of program operation starts immediately after the loading the second page data. When the data loading of total three pages is completed, the program operation proceeds to the end without pause. This approach can effectively reduce overall program operation time, since the data loading of two pages can be shared with the first and second program loops.

Next, latch operations for the first two-loop program with data loading are described in detail during the first and second loop of program operation. A mapping table of program states and binary codes of each programmed state are shown in Fig. 5(a). The program states from P1 to P4, where the data of the first page are 0, are chosen to be programmed at the first loop. At the first loop, the P5, P6, and P7 states are remained in the erase states. After the second page data are entered, the states of P6 and P7 whose data are 0 are programmed together with the states from P1 to P4 at the second loop. At this point, the P5 state is still in the erase state. After the last page data are entered, the P5 state whose data are 0 is selected to be programmed finally at the third loop. After the third loop, all states from P1 to P7 are programmed together. The program start voltage of P5 state is slightly larger than that of the other states, which is negligible, because the start voltage of P5 is still far from the voltage that P5 state begins to pass the verify.

In conclusion, it has been presented to program some program states in the first and second program loops to cache two pages without adding latches. The program method reduces the time overhead reduction to 60 us, assuming 1-Gb/s IO operation. Since the gain is inversely proportional to the IO frequency, the time gain is higher at lower IO frequencies.

### B. Two-Step Annealing Pulse

For the 3-D NAND using a charge trap flash memory cell [16], one of the major reliability degradations is originated from the hole captured in a shallow trap during erase operation. Due to the low-energy level, at various temperature conditions after programming, these holes will behave unexpectedly during the retention period. Holes injected during the erase operation exist not only in a trap layer below the gate but also in the trap layer between the gates. The holes trapped at the interface sites between the gates drift to other gates along the trap layer and are also de-trapped to the poly-silicon channel. These behaviors are shown in Fig. 6. During the retention period after programming, the holes flowing toward adjacent programmed cells are eliminated by electron-hole recombination. In addition, the threshold voltage of an

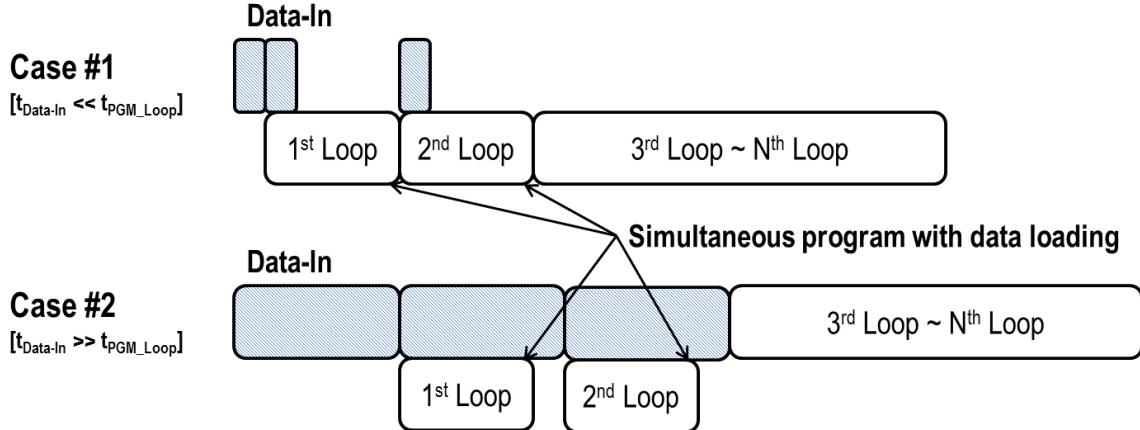


Fig. 4. Two examples of the first two-loop program with data loading according to different loading times.

	E	P1	P2	P3	P4	P5	P6	P7
1 <sup>st</sup> Page	1	0	0	0	0	1	1	1
2 <sup>nd</sup> Page	1	1	0	0	1	1	0	0
3 <sup>rd</sup> Page	1	1	1	0	0	0	0	1

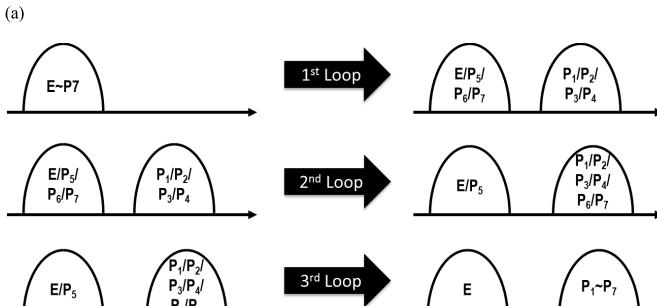


Fig. 5. (a) Mapping table of binary code and program states. (b) Behavior of a program states during the first two-loop program with data loading.

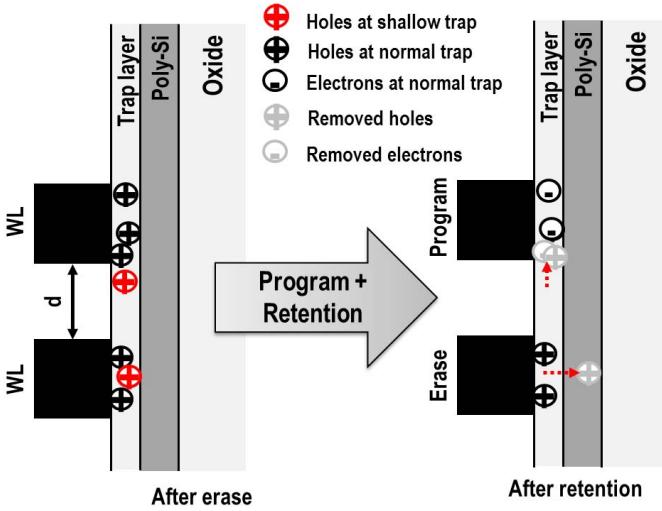


Fig. 6. Illustration of holes' behavior after programming and retention.

erased cell during retention can be increased by a de-trapping phenomenon similar to a soft programming. It has previously been reported to electrically anneal holes in a shallow trap to

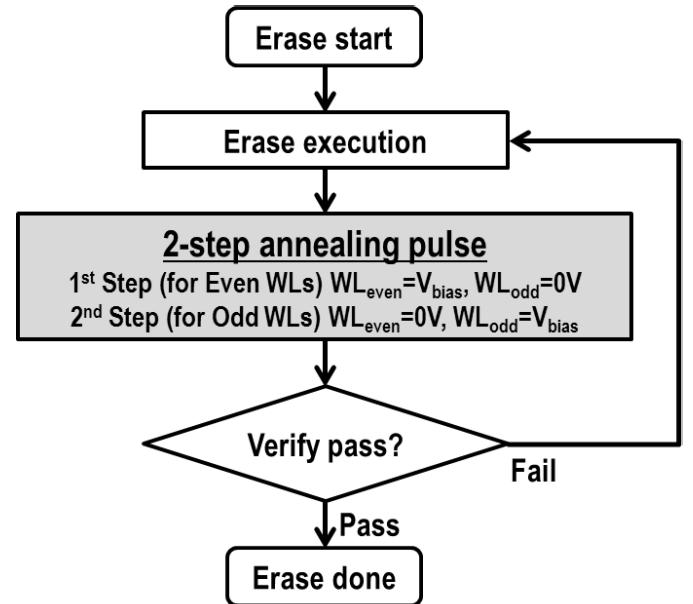


Fig. 7. Flowchart of the Erase with a two-step annealing pulse.

compensate degradation for retention by applying bias voltage to all of the gates [17].

In this paper, we introduce a two-step annealing pulse technique for improving reliability in the 3-D NAND structure compared with 1-D electrical annealing. Fig. 7 shows the flow diagram for the two-step electrical annealing process. First of all, after the erase operation, a high-voltage pulse of  $V_{\text{bias}}$  for electrical annealing is applied to even-numbered WLs while biasing odd-numbered WLs and poly-Si channel to ground. Next,  $V_{\text{bias}}$  is applied to the odd-numbered WLs while biasing the even-numbered WLs and poly-Si channel to ground.  $V_{\text{bias}}$  for removing holes trapped in a shallow trap should be chosen carefully to avoid programming erased cells; 2-D electrical annealing can compensate the holes in two directions. The holes in the shallow trap move from the gate to the channel, and this is the first direction. The other holes in the shallow trap move away from the gate to a distant space that does not affect lateral spreading, and this is the second direction; 2-D

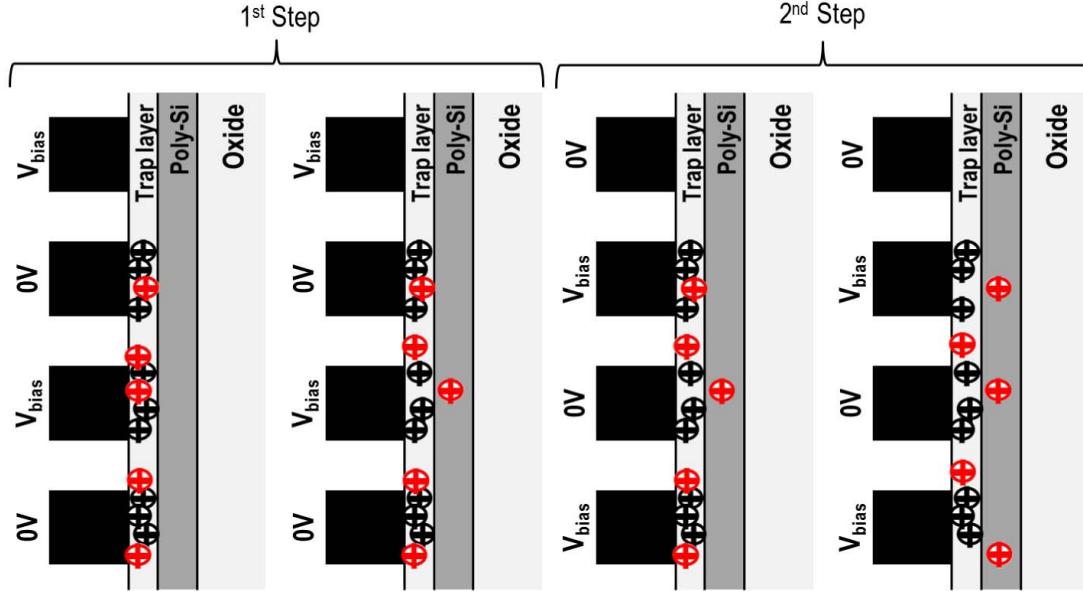


Fig. 8. Behavior of the holes trapped in the shallow trap during the two-step annealing pulse.

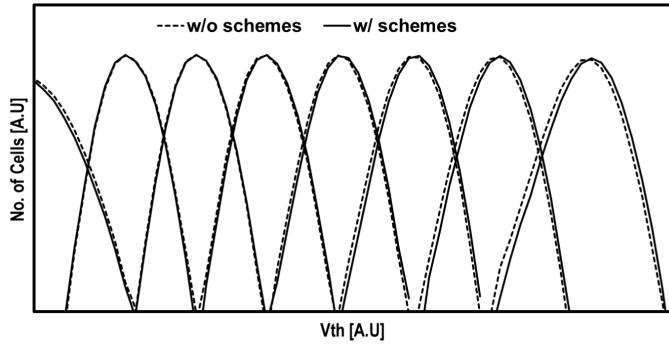


Fig. 9. Measured comparison results of  $V_{th}$  distribution after retention. Real line: result of a two-step annealing pulse. Dotted line: result without annealing scheme.

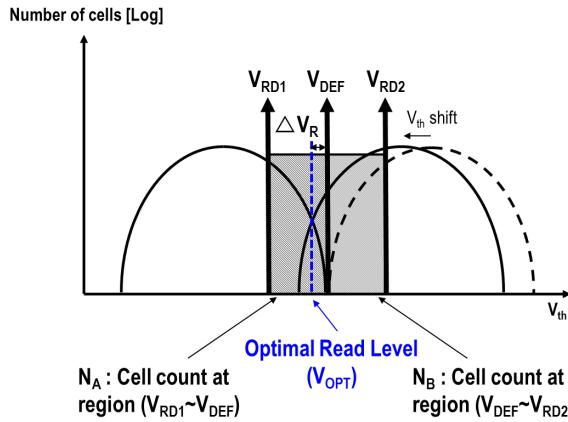


Fig. 10. Optimal read level shift according to the  $V_{th}$  shift of the upper state.

annealing pushes the holes out of the gates and removes the holes to the poly-silicon channel. Fig. 8 shows the conceptual behavior of the holes during the annealing process.

As shown in Fig. 9, the measurement result of the  $V_{th}$  distribution after retention shows that the two-step annealing

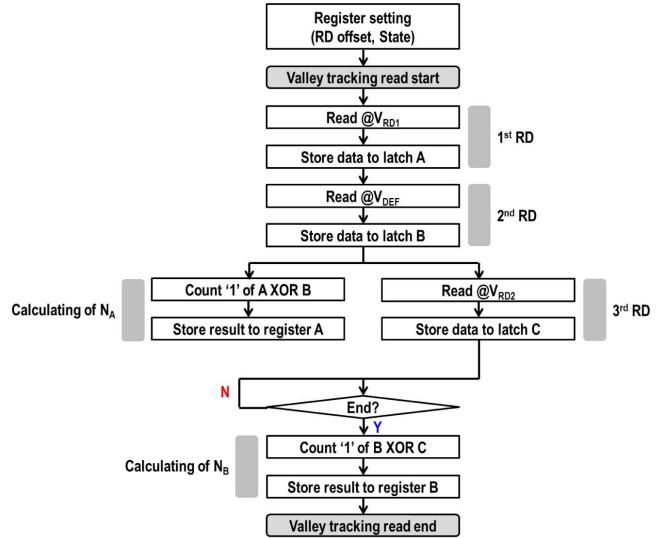


Fig. 11. Flowchart of the valley tracking read scheme.

helps to improve the reliability characteristics. By optimizing the core design, we can improve bit error rate (BER) up to 7% and reduce the timing overhead of the scheme to less than 3% of overall erase operation time.

### C. On-Chip Valley Tracking Read

Under the complex combinations of program-erase cycles and retention time, the  $V_{th}$  distribution of the programmed and erased cells is shifted upward or downward. These  $V_{th}$  shifts make error bits increase at the default read level. Read retrying with an optimal read voltage in response to the shift of  $V_{th}$  can be a good solution for reducing errors. For the read retry, additional reads are essential and the number of reads for tracking valley between  $V_{th}$  distributions is a key parameter for performance. To suppress performance degradation due to

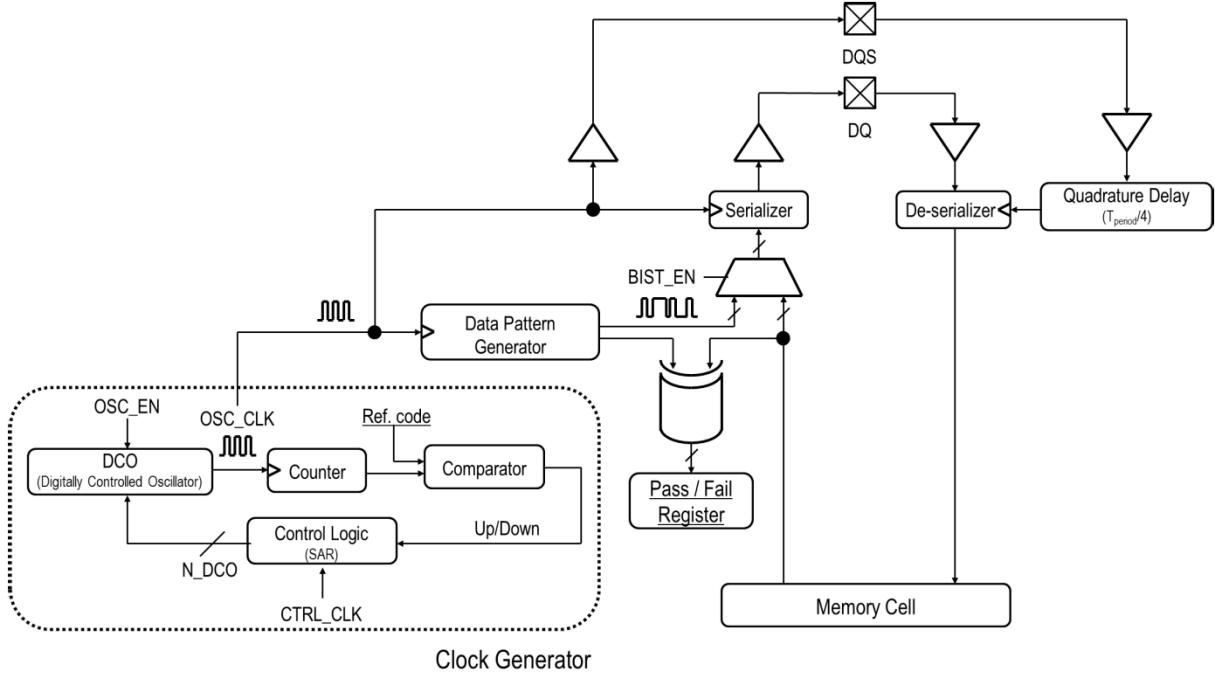


Fig. 12. Schematic of high-speed BIST with an auto clock generator.

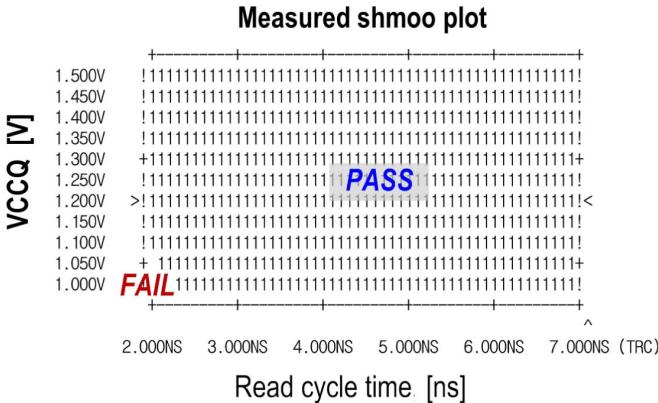


Fig. 13. Read cycle shmoo at 1.2-V IO supply voltage.

error correction, we propose a read algorithm that adaptively searches for the optimal read voltage that minimizes the number of error bits.

Fig. 10 shows an example where the upper state is shifted downward due to charge loss during retention. Error bits at the default read level ( $V_{DEF}$ ) increase significantly compared with those of the initial cycle. In this case, error bits can be minimized if users move the optimal read level ( $V_{OPT}$ ) to the left in the  $V_{DEF}$  and retry read operation at the  $V_{OPT}$ . The optimal read level can be calculated based on the number of cells to the left and right of the  $V_{DEF}$ .  $N_A$  represents the number of cells with  $V_{th}$  between the two adjacent read voltages on the left ( $V_{RD1}$  and  $V_{DEF}$ ), and  $N_B$  represents the number of cells on the right ( $V_{DEF}$  and  $V_{RD2}$ ). The optimal read level can be estimated assuming that  $\Delta V_R$  is proportional to the difference between  $N_A$  and  $N_B$ . The equations below

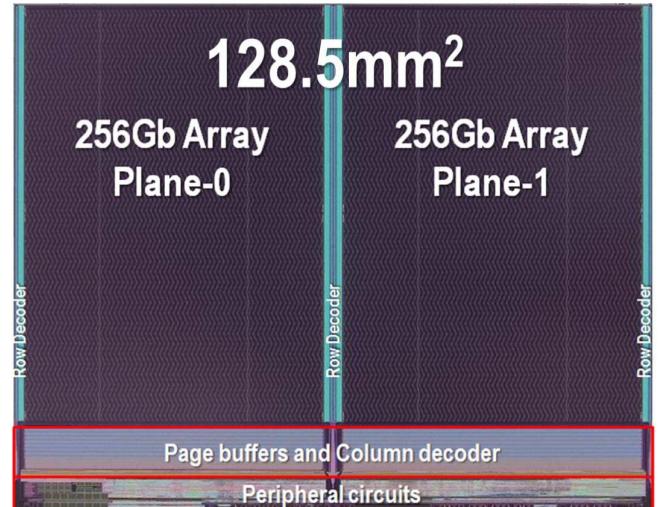


Fig. 14. Die photography of a 512-Gb 3-b/cell NAND flash chip.

summarize the algorithm

$$\Delta V_R = \alpha \cdot (N_A - N_B) \quad (1)$$

$$V_{OPT} = V_{DEF} + \Delta V_R. \quad (2)$$

If  $N_A$  is greater than  $N_B$ , it means that the valley has shifted left from  $V_{DEF}$ . On the other hand, if  $N_B$  is greater than  $N_A$ , it means that  $V_{OPT}$  has shifted right from  $V_{DEF}$ . The voltage shift,  $\Delta V_R$ , is calculated as  $\alpha \times (N_A - N_B)$ . The proportional coefficient  $\alpha$  can be pre-defined empirically. If the chip provides the value of  $N_A$ ,  $N_B$ , and  $\alpha$ , then the host controller can change the read level to  $V_{OPT}$  after calculation.

TABLE I  
COMPARISON WITH PREVIOUS WORK

	ISSCC15 [2]	ISSCC16 [3]	<u>This Work</u>
Bits per cell	3	3	3
Density	128Gb	256Gb	512Gb
Chip size	68.9mm <sup>2</sup>	97.6mm <sup>2</sup>	128.5mm <sup>2</sup>
Arial density	1.86Gb/mm <sup>2</sup>	2.62Gb/mm <sup>2</sup>	3.98Gb/mm <sup>2</sup>
Technology	3D NAND 32 stacked WL	3D NAND 48 stacked WL	3D NAND 64 stacked WL
Organization	16KB / Page 384 Pages / Block 2732 Blocks / Die	16KB / Page 576 Pages / Block 3776 Blocks / Die	16KB / Page 768 Pages / Block 5748 Blocks / Die
I/O Bandwidth	Max. 1Gb/s	←	←
VccQ	1.8V	←	1.8V / 1.2V
tBERS	3.5ms (Typ.)	←	←
tPROG	700us	660us	700us
tR (4KB)	45us	45us	60us

The chip itself counts and stores the number of cells  $N_A$  and  $N_B$  in each area in the chip's internal register. Fig. 11 shows the state diagram of the valley tracking read, which operates with a single command. The chip supports a feature that reads three times without user command intervention and counts the number of cells at each region. Thus, the user would not need to issue three separate read commands and then compare the read data. The valley search algorithm requires a read offset voltage and a target state to be corrected, and these data have to be inputted before starting the algorithm. The results of each read operation with three different levels are stored and the calculated results of  $N_A$  and  $N_B$  are stored in registers contained in a peripheral circuit during the operation. Since the on-chip cell count operation time is less than 10 us, the counting  $N_A$  can proceed simultaneously during the third read operation to minimize logic operating overhead. On-chip operation removes three times of data out, command, and address sequence between reads. Therefore, assuming that the data output time is 16 us and the command issue time is approximately 1 us, the on-chip valley tracking read saves more than 50 us than the off-chip operation in terms of overall time overhead.

### III. IO OPERATIONS

#### A. High Speed Built-In Self-Test

The maximum available operating frequency at a wafer-level test was limited to tens of MHz, because the IO channels were shared with multiple chips to maximize throughput and

reduce test time. Hence, the evaluation of high-speed paths is only available at a package or module level. Under this test flow, failures occurring in the high-speed path cannot be screened out before the package assembly process. The high-frequency test at the package level increases cost, because whole dies with a multi-chip package are abandoned if failure occurs. To resolve this issue, we propose a high-speed BIST, as shown in Fig. 12. The BIST block consists of a clock generator with a variable frequency range, a data pattern generator, and a data comparator. BIST operations are done with three steps: 1) the clock generator adjusts the clock frequency automatically; 2) the data pattern generator creates pre-defined data according to the generated clock; and 3) the data comparator determines pass or fail after the comparison between the expected data and the data transported through a BIST chain. The clock generator consists of a code comparator, a successive approximation register (SAR) for the control, a digitally controlled oscillator (DCO), and a counter. The BIST automatically generates a high-speed clock based on the DCO. The generated DCO clock counts the number of cycles for the OSC\_EN and a slow signal inputted from a tester. The counter code is compared with the reference code, which is the number of counting the OSC\_EN by the tester's slow clock. The comparison result gives a feedback to the DCO control logics to increase or decrease the DCO clock frequency using up or down code. To generate the DCO code, the SAR logics are used to reduce the DCO frequency locking time. This locking process is repeated to generate the BIST clock with the target frequency until the reference code and the counter

code are matched. After the data pattern generation based on the DCO clock, data are written to the memory cells, and data read from the memory cells are compared with the pre-defined data. The comparison results are latched in the pass/fail register. From the tester, the pass/fail information can be read out. The BIST circuits operate through an internal loopback path to test the high-speed paths without the influence of external test environments. Therefore, the BIST scheme enables testing of the high-speed paths at the wafer level without any changes to the measurement environment, while maintaining the maximum operating speed of the device.

### B. 1.2-V IO Operation

This paper supports dual IO supply voltage VCCQ of 1.2 and 1.8 V. In addition to the performance of high-speed data rates, a low-voltage IO operation is required for the reduction of overall system power consumption. Fig. 13 shows the measured read shmoo plot. In this figure, the *x*-axis and the *y*-axis describe the read cycle time and IO supply voltage, respectively. The shmoo plot displays pass and fail windows for read data while changing the IO voltages and read cycle times. As a result, this paper achieved a read cycle of 2.0 ns corresponding to 1-Gb/s IO bandwidth performance and saved IO power consumption by 40% at 1.2-V IO supply voltage.

## IV. CHIP ARCHITECTURE

A microphotograph of the 512-Gb 3-b/cell NAND flash chip is shown in Fig. 14. The chip size is 128.5 mm<sup>2</sup> and it is a two-plane architecture implemented to maximize throughput. Each plane has 2874 blocks and of which size is 12 MB. One block consists of 768 pages of which size is 16 KB.

## V. CONCLUSION

The 512-Gb 3-b/cell NAND flash memory manufactured using the 64-stacked WL process has been announced. The areal density was 3.98 Gb/mm<sup>2</sup>, an increase of 51.9% over the previous work [2]. The first two-loop program with data loading effectively reduces *t*<sub>PROG</sub>. Two-step annealing has been proposed to compensate for the increased lateral spreading due to the vertical scaling and the BER after retention can be increased by 7%. Adopting these approaches can maintain program performance even when the cell characteristics are degraded. The on-chip valley tracking read has been proposed to minimize read retry time. Also, the suggested high-speed BIST allows testing of the maximum frequency IO operation at the wafer level. The device supports a 1.2-V IO supply voltage to reduce power consumption. Table I summarizes the key parameters of this paper.

## REFERENCES

- [1] J. W. Lim *et al.*, “A 128 Gb 3 b/cell V-NAND flash memory with 1 Gb/s I/O rate,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 130–131.
- [2] D. Kang *et al.*, “256 Gb 3b/cell V-NAND Flash memory with 48 stacked WL layers,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2016, pp. 130–131.
- [3] K.-T. Park *et al.*, “Three-dimensional 128 Gb MLC vertical NAND flash-memory with 24-WL stacked layers and 50 MB/s high-speed programming,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 334–335.
- [4] K. T. Park *et al.*, “A 7 MB/s 64 Gb 3-bit/cell DDR NAND flash memory in 20 nm-node technology,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 212–213.
- [5] N. Shibata *et al.*, “A 19 nm 112.8 mm<sup>2</sup> 64 Gb multi-level flash memory with 400 Mb/s/pin 1.8 V toggle mode interface,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 422–423.
- [6] D. Lee *et al.*, “A 64 Gb 533 Mb/s DDR interface MLC NAND flash in sub-20 nm technology,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 430–431.
- [7] Y. Li *et al.*, “128 Gb 3b/cell NAND flash memory in 19 nm technology with 18 MB/s write rate and 400 Mb/s toggle mode,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 436–437.
- [8] G. Naso *et al.*, “A 128 Gb 3 b/cell NAND flash design using 20 nm planar-cell technology,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 218–219.
- [9] M. Helm *et al.*, “A 128 Gb MLC NAND-flash device using 16 nm planar cell,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 326–327.
- [10] S. Choi *et al.*, “A 93.4 mm<sup>2</sup> 64Gb MLC NAND-flash memory with 16 nm CMOS technology,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 328–329.
- [11] M. Sako *et al.*, “A low-power 64 Gb MLC NAND-flash memory in 15 nm CMOS technology,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 128–129.
- [12] S. Lee *et al.*, “A 128 Gb 2 b/cell NAND flash memory in 14 nm technology with t<sub>PROG</sub>=640 μs and 800 MB/s I/O rate,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2016, pp. 138–139.
- [13] T. Tanaka *et al.*, “A 768 Gb 3 b/cell 3D-floating-gate NAND flash memory,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2016, pp. 142–144.
- [14] D. Kang *et al.*, “256 Gb 3 b/cell V-NAND flash memory with 48 stacked WL layers,” *IEEE J. Solid-State Circuits*, vol. 52, no. 1, pp. 210–217, Jan. 2017.
- [15] T. Cho *et al.*, “A dual-mode NAND flash memory: 1 Gb multi-level and high-performance 512-Mb single-level modes,” *IEEE J. Solid-State Circuits*, vol. 36, no. 11, pp. 1700–1706, Nov. 2001.
- [16] J. Jang *et al.*, “Vertical cell array using TCAT (terabit cell array transistor) technology for ultra high density NAND flash memory,” in *Proc. Symp. VLSI Technol.*, Jun. 2009, pp. 192–193.
- [17] C. C. Yeh *et al.*, “Novel operation schemes to improve device reliability in a localized trapping storage SONOS-type flash memory,” in *IEDM Tech. Dig.*, Dec. 2003, pp. 173–176.



**Chulbum Kim** received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2001, 2003, and 2008, respectively.

At KAIST, he was involved in research fields including infrared sensor imaging systems and CMOS image sensor. In 2008, he joined Samsung Electronics Corporation, Hwasung, South Korea, where he has been involved in the design of NAND flash memories. From 2008 to 2011, he designed and developed toggle DDR I/O and data-path circuits. Since 2012, he has participated in the development of 32-layer 3-D NAND flash memory to 64-layer 3-D NAND flash memory. His current research interests include designs for core algorithms and logic circuits for 3-D NAND flash memory.



**Doo-Hyun Kim** was born in Seoul, South Korea, in 1982. He received the B.S., M.S., and Ph.D. degrees from the School of Electrical Engineering and Computer Science, Seoul National University, Seoul, South Korea, in 2005, 2007, and 2011, respectively.

In 2011, he joined Samsung Electronics Company Ltd., Hwaseong, South Korea, as a Senior Engineer, where he was involved in the design of 2-bit and 3-bit V-NAND flash memory mass production of all the generations from the world’s first 24 stacks to fourth 64 stacks. His current research interests include the high performance, reliability, and low power of V-NAND flash memory, and developing a new product of the next generation V-NAND flash memory.



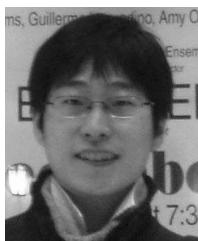
**Woopyo Jeong** received the B.S. and M.S. degrees in electrical engineering from Yonsei University, Seoul, South Korea, in 1991 and 1993, respectively, and the Ph.D. degree in electrical and computer engineering from Purdue University, West Lafayette, IN, USA, in 2004.

In 1993, he joined Samsung Electronics Company, Hwaseong, South Korea, where he was involved in research and development for DRAM. After his graduation, he rejoined the Mobile DRAM Design Team. Since 2007, he has been with the NAND Flash Circuit Design Team. He has been involved in developing 3-D vertical NAND as a Project Leader.



**Hyun-Jin Kim** received the B.S. degree from Ewha Womans University, Seoul, South Korea, in 1999, the M.S. degree from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2001, and the Ph.D. degree from The University of Texas at Austin, USA, in 2012, all in electrical engineering.

She joined Samsung Electronics Company, Hwaseong, South Korea, in 2003. From 2003 to 2008, she was involved in the design of high-speed graphics DRAMs. Since 2012, she has been involved in NAND flash memory design. Her current research interests include high-speed CMOS interface circuits, clocking circuits, and signal integrity.



**Il Han Park** received the Ph.D. degree in electrical engineering from Seoul National University, Seoul, South Korea, in 2009.

He is currently with the Flash Design Team, Samsung Electronics Company, Hwaseong, South Korea.



**Hyun-Wook Park** received the B.S. and M.S. degrees in electronics engineering from the Kyungpook National University, Daegu, South Korea, in 2004 and 2006, respectively.

Since 2006, he has been involved in the development of NAND flash memory with the Flash Design Team, Samsung Electronics Company, Hwaseong, South Korea. His current research interests include the development of high performance 3-D NAND flash memory.



**JongHoon Lee** received the B.S. and M.S. degrees in electrical engineering from Kook-Min University, Seoul, South Korea, in 2002 and 2004, respectively.

At Kook-Min University, he was involved in research fields including analog integrated circuits. In 2004, he joined Samsung Electronics Corporation, Hwaseong, South Korea, where he has been involved in the design of NAND flash memories. From 2004 to 2015, he designed and developed core algorithms and analog circuits for planar NAND devices (SLC 1 Gb ~ TLC 128 Gb). Since 2016, he has been involved in the development of 64-layer 3-D NAND flash memory. His current research interests include designs for core algorithms and analog circuits for 3-D NAND flash memory.



**JiYoon Park** received the B.S. degree in electrical engineering from Korea University, Seoul, South Korea, in 2006.

In 2006, he joined Samsung Electronics Corporation, Hwaseong, South Korea, where he has been involved in the design of NAND flash memories. From 2006 to 2011, he participated in the development of 59-nm to 14-nm technology NAND flash memory. Since 2012, he has participated in the development of 32-layer 3-D NAND flash memory to 64-layer 3-D NAND flash memory. His current research interests include designs for core algorithms and logic circuits for 3-D NAND flash memory.



**Yang-Lo Ahn** received the B.S. degree in electrical engineering from Kyung Hee University, Suwon, South Korea, in 2007.

In 2007, he joined Samsung Electronics Corporation, Hwaseong, South Korea, where he has been involved in the design of NAND flash memories. From 2007 to 2012, he designed and developed layout P&R Engineering. Since 2012, he has participated in the development of planar NAND flash memory to 64-layer 3-D NAND flash memory. His current research interests include designs for logic circuits for 3-D NAND flash memory.



**Ji Young Lee** received the B.S. degree in electronics engineering from Ajou University, Suwon, South Korea, in 2005, and the M.S. degree in optical communications engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2008.

In 2008, she joined Samsung Electronics Corporation, Hwaseong, South Korea, where she has been involved in the design of NAND flash memories. She is involved in developing the next generation NAND flash memory. Her current research interests include circuit design for V-NAND.



**Seung-Bum Kim** was born in Seoul, South Korea, in 1978. He received the bachelor's degree in electrical engineering from the University of Sogang, Seoul, South Korea, in 2006, and the master's degree from the College of Information and Communication Engineering, Sungkyunkwan University, South Korea, in 2017.

In 2006, he joined the Memory Division, Samsung Electronics Company, Ltd., Hwaseong, South Korea. He has been a member of the Flash Design Team, since he has been with Samsung. His current research interests include the physics of V-NAND, algorithm, digital logic circuit, analog circuit, and mixed signal.



**Hyunjun Yoon** received the B.S. and M.S. degrees in electrical and electronic engineering from Yonsei University, Seoul, South Korea, in 2004 and 2009, respectively.

He is currently with the Memory Division, Samsung Electronics Company, Hwaseong, South Korea, where he is a Hardware Designer, developing flash memory.



**Jae Doeg Yu** received the B.S. degree in electrical engineering from Yonsei University, Seoul, South Korea, in 2008.

In 2008, he joined Samsung Electronics Corporation, Hwasung, South Korea, where he has been involved in the design of NAND flash memories. He is involved in developing the next generation NAND flash memory. His current research interests include circuit design for V-NAND.



**Seunghwan Song** was born in South Korea in 1988. He received the B.E. and M.E. degrees from Sogang University, Seoul, South Korea, in 2013 and 2015, respectively.

Since then, he has been with Samsung Electronics Corporation, Hwasung, South Korea, where he is currently an Engineer of the Flash Design Technology and Research and Development.



**Nayoung Choi** received the B.S. degree in semiconductor systems engineering from Sungkyunkwan University, Seoul, South Korea, in 2010.

In 2011, she joined Samsung Electronics Company Ltd., Hwaseong, South Korea, where she has been involved in the design of NAND flash memories. She is currently involved in developing the next generation NAND flash memory. Her current research interests include circuit design for V-NAND.



**YongHa Park** was born in South Korea in 1990. He received the B.E. degree from SungKyunKwan University, Suwon, South Korea, in 2015.

Since then, he has been with Samsung Electronics Corporation, Hwasung, South Korea, where he is currently an Engineer of the Flash Design Technology and Research and Development.



**NaHyun Kim** received the B.S. and M.S. degrees from the College of Information and Communication Engineering, Sungkyunkwan University (SKKU), Suwon, South Korea, in 2012 and 2014, respectively.

At SKKU, her research interests include mixed-signal circuit design and EMC. She is currently with the Memory Division, Device Solution Business, Samsung Electronics Corporation, Hwasung, South Korea, where she has been involved in the design of NAND flash memories. She has been engaged in the development of 64-layer 3-D NAND flash memory.



**Jinbae Bang** received the B.S. degree in electrical engineering from Kwangwoon University, Seoul, South Korea, in 2015.

In 2015, he joined Samsung Electronics Company Ltd., Hwaseong, South Korea, where he has been involved in the design of NAND flash memories. He is currently involved in developing the next generation NAND flash memory. His current research interests include circuit design for V-NAND.



**Hwajun Jang** received the B.S. degree in electrical engineering from Chungang University, Seoul, South Korea, in 2012.

Since 2012, he has been with Samsung Electronics Corporation, Hwasung, South Korea, where he has been involved in the design of NAND flash memories. From 2012 to 2016, he worked in the Physical Implementation Team of 3-D NAND flash memory. He participated in the development of the 14-nm technology NAND flash memory to 64-layer 3-D NAND flash memory. His current research interests include designs and verifications for logic circuits for 3-D NAND flash memory.



**Sanggi Hong** was born in South Korea in 1991. He received the B.E. degree from Sungkyunkwan University, Suwon, South Korea, in 2015.

Since then, he has been with Samsung Electronics Company, Hwaseong, South Korea, where he is currently an Engineer of the Flash Design Technology and Research and Development.



**JongHoon Park** received the B.S. degree in electrical engineering from Ajou University, Gyeonggi, South Korea, in 2014.

Since 2014, he has been with Samsung Electronics Corporation, Hwasung, South Korea, where he has been involved in the design of NAND flash memories. He participated in the development of 14-nm technology NAND flash memory to 64-layer 3-D NAND flash memory. His current research interests include designs and verifications for logic circuits for 3-D NAND flash memory.



**Youngdon Choi** was born in Seoul, South Korea. He received the B.S. (with highest honors), M.S., and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 1999, 2001, and 2005, respectively. His Ph.D. dissertation was related to the design of flat panel display link.

From 2003 to 2005, he was with Anapass Inc., Seoul, where he was involved in the circuit design for flat panel display solutions. In 2005, he joined Samsung Electronics Company (SEC), Ltd., Hwaseong, South Korea, where he was involved with the circuit design for post DDR3. From 2008 to 2014, he was involved in PRAM core and analog circuit design. From 2014 to 2015, he was a Visiting Scholar with the University of California at Berkeley, USA, under the guidance of Prof. B. Nikolic. His current research interests include high-speed link, low-power CMOS circuits, and new memory design, such as Resistive RAM and Magnetic RAM. He is currently a Project Leader with the Flash I/O Group, SEC.



**Moo-Sung Kim** received the B.S. degree in electronic engineering from Youngnam University, Gyeongsan, South Korea, in 1998, and the M.S. degree in electronic engineering from the Pohang University of Science and Technology, Pohang, South Korea, in 2000.

He joined Samsung Electronics Company, Ltd., Hwaseong, South Korea, as a SRAM Device Engineer. In 2003, he became a NAND Flash designer and developed 70-, 50-, 30-, and 20-nm class planar NAND flash. He is currently a Principal Engineer with Samsung Electronics. His current research interests include 10-nm class planar NAND and vertical NAND flash memory for high performance and low power.



**Dae Seok Byeon** received the B.S. degree in electrical engineering and the M.S. and Ph.D. degrees in SOI device and power semiconductor device from Seoul National University, Seoul, South Korea, in 1992, 1994, and 1999, respectively.

Since 1999, he has been with Samsung Electronics Corporation, Hwasung, South Korea, where he has been leading Samsung's NAND flash memory design over 15 years. He had been a Team Leader of various world first commercialized NAND products, such as 0.12  $\mu\text{m}$  1 Gb, 90 nm 2 Gb, 63 nm 8 G, 51 nm 16 G, 32 nm 32 G, 35 nm, and 41 nm 32 G, and successfully commercialized the 2-bit and 3-bit NAND Flash Memory products. He has played an active role in advancing the design of 3-D NAND product using vertical channel structure and the core algorithm for next generation non-volatile memory device. He is currently a Master with the Memory Division of Samsung. He holds over 40 papers and over 130 patents related to memory technology.

Dr. Byeon has served as a Memory Subcommittee Member of the International Solid-State Circuits Conference and a Cooperative Board Member of The Institute of Electronics and Information Engineers, South Korea.



**Hyunggon Kim** received the B.S. and M.S. degrees in electrical engineering from Hanyang University, Seoul, South Korea, in 1997 and 1999, respectively.

He was with Hanyang University, where he was involved in the fault tolerance system. In 1999, he joined Samsung Electronics Company Ltd., Hwaseong, South Korea, where he has been involved in the design of NAND flash memories. His current research interests include digital circuit design and verification for NAND flash.



**Jin-Yub Lee** received the B.S. and M.S. degrees in electrical engineering from Sogang University, Seoul, South Korea, in 1994 and 1996, respectively.

In 1996, he joined Samsung Electronics Company Ltd., Hwasung, South Korea, as a Flash Design Engineer. He was the Starter of a fusion memory one NAND in 2004, where he has been leading many Flash projects based on the MLC/TLC cells. He has been responsible for designing and product engineering 3-D NAND Flash memories. He is currently the Vice-President with Samsung Electronics Company Ltd., where he is involved in path finding to the next generation 3-D NAND.



**Pansuk Kwak** received the B.S. degree in electrical engineering from Kwangwoon University in 1997.

In 1997, he joined Samsung Electronics Corporation, Hwasung, South Korea, where he is currently with the Memory Division leading the design of NAND flash devices. His current research interests include the physical design of NVM.



**Ki-Tae Park** received the B.S. degree in electronics engineering from Kyungbook National University, South Korea, in 1993, and the M.S. and Ph.D. degrees in machine intelligence and system engineering from Tohoku University, Japan, in 1993 and 1999, respectively.

From 1999 to 2001, he was a Research Associate involved in nano-CMOS devices, low power circuits, 3-D shared memories, and artificial retina chips with Tohoku University. From 2001 to 2004, he was with Halo LSI, NY, USA, working in circuit embedded flash and NAND compatible high density SONOS technology. He joined Samsung Electronics Corporation, Hwasung, South Korea, in 2004, and has been involved in design of MLC and TLC NAND flash memory products. He had been responsible for designing world's first TLC NAND for SSD application. He also has been responsible for developing world's first 3-D NAND product using vertical layer-stacking technology. He is currently a Vice-President with Samsung. He holds over 100 U.S. patents.

Dr. Park received several achievement awards from Samsung for his outstanding work.



**Jeong-Don Ihm** received the B.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 1992, and the M.S. degree in electronic engineering from Seoul National University, Seoul, South Korea, in 1996.

He joined LG Semiconductor, Seoul, in 1996, where he was involved in DRAM design. In 2004, he joined Samsung Electronics Corporation, Hwasung, South Korea, where he was involved in the design of high-speed DRAMs. In 2012, he moved to the NAND Flash Design Team and was involved in developing NAND IO and data-path circuit design.



**Kye-Hyun Kyung** received the B.S., M.S., and Ph.D. degrees in control and instrumentation engineering from Seoul National University, Seoul, South Korea, in 1986, 1988, and 1994, respectively.

After receiving the Ph.D. degree, he joined Samsung Electronics Corporation, Hwasung, South Korea, as a DRAM Design Engineer. In 2009, he started his new career as a NAND Flash Designer and developed toggle DDR2 NAND flash. He is currently an Executive Vice-President of the Flash Memory Division, Samsung Electronics. His current research interests include 10-nm class planar NAND and the next-generation V-NAND flash memory for high performance and low power.