

# A Nyquist Rate SAR ADC Employing Incremental Sigma Delta DAC Achieving Peak SFDR = 107 dB at 80 kS/s

Ahmad AlMarashli<sup>✉</sup>, Student Member, IEEE, Jens Anders, Senior Member, IEEE,  
Joachim Becker, Senior Member, IEEE, and Maurits Ortmanns, Senior Member, IEEE

**Abstract**—This paper introduces an architecture and design for high-resolution high-linearity Nyquist rate successive approximation register (SAR) analog-to-digital converters (ADCs) using a hybrid capacitive and incremental  $\Sigma\Delta$  digital-to-analog converter (DAC). The proposed architecture benefits from an intrinsically linear 1.5-bit  $\Sigma\Delta$  DAC to resolve the fine bits of the SAR ADC after a coarse conversion phase with a monotonically switched capacitive DAC (CDAC). The achieved linearity relies neither on a highly matched CDAC nor on any dynamic linearization techniques but on a single calibration of the coarse CDAC using the available  $\Sigma\Delta$  DAC at startup. Therefore, the CDAC can be sized solely upon noise requirements. The SAR ADC employs two parallel dynamic comparators for improved power efficiency. A prototype was fabricated in a 40-nm CMOS, with power supplies of 1.1 and 2.5 V. It occupies an active area of only 0.074 mm<sup>2</sup>. The prototype achieves a measured peak spurious free dynamic range (SFDR) of 107 dB and peak signal to noise and distortion ratio (SNDR) of 84.8 dB at 80-kS/s Nyquist rate operation with 5.3-kHz input. The measured performance at the Nyquist frequency, limited by signal source quality, is SFDR = 99.5 dB and SNDR = 83.5 dB. The core power consumption is 110  $\mu$ W. In oversampling mode, the ADC achieves an SNDR above 90 dB over a 5-kHz bandwidth.

**Index Terms**— $\Sigma\Delta$  digital-to-analog converter (DAC), capacitive DAC (CDAC), hybrid comparator, hybrid DAC, oversampling analog-to-digital converter (ADC), successive approximation register (SAR) ADC, self-calibration.

## I. INTRODUCTION

SUCCESSIVE approximation register (SAR) analog-to-digital converters (ADCs) have received significant attention for their excellent power efficiency when employing modern deep sub-micrometer CMOS technologies and the best efficiency is achieved for applications with moderate resolution [1]–[3]. Still, in many applications such as sensor readouts, biomedical signal processing, or applications such as digital lock-in detection, high-resolution and high-linearity Nyquist rate ADCs are required. While common Nyquist rate SAR ADCs showed limited effective resolution,

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The authors are with IFM, University of Ulm, D-89081 Ulm, Germany (e-mail: ahmad.almarashli@uni-ulm.de).

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some recent SAR designs investigated high resolutions above 14 bits [4]–[7], while maintaining the beneficial power efficiency. The linearity was limited mainly due to mismatch errors resulting in effective resolutions below 13 bits. A major increase of the effective resolution of the SAR architecture was achieved with oversampling, comparator noise and/or mismatch error shaping techniques [4], [8]–[10]. However, all those techniques rely mainly on a non-reset decimation filter, which includes memory; thus, it does not allow Nyquist rate operation and therefore makes them unsuitable for many applications, including, for example, multiplexed sensor array readouts. Incremental- $\Sigma\Delta$  ADCs achieve very high resolution in a Nyquist rate due to their periodic reset after every sample. However, those were so far developed for quite low Nyquist frequencies and were mainly evaluated for static or dc-like inputs [11], [12].

To achieve high-resolution Nyquist rate conversion, pipelined and partly time-interleaving ADCs were used [13]–[16]. Those required power-hungry residual amplifiers and resulted mainly in a degraded spurious free dynamic range (SFDR). Moreover, pipelining the SAR ADC structure makes it much less digital and scaling friendly, and therefore, those designs were implemented mostly and preferably in relatively old technology nodes [14]. On the other hand, a sophisticated calibration unit was needed for almost all Nyquist rate ADCs with above 12-bit resolutions, potentially together with dynamic linearization techniques and/or dedicated analog circuitry for calibration [4]–[7], [13], [14]. This again imposed in most cases a major additional area and power consumption for the ADCs.

To mitigate the mentioned shortcomings and introduce a high-resolution Nyquist rate SAR ADC, this paper presents a technique to implement a hybrid digital-to-analog converter (DAC) in the feedback path of the SAR ADC [17]. The novel hybrid DAC does not rely on a full-resolution binary-scaled capacitive DAC (CDAC) array, but instead uses an incremental  $\Sigma\Delta$  DAC to resolve the fine DAC steps after the most significant bit (MSB) steps, which are performed with a coarse CDAC. The  $\Sigma\Delta$  DAC also performs a startup calibration of the coarse CDAC and allows linearity that exceeds the nominal resolution. Because of a linear  $\Sigma\Delta$  DAC output, there is no need for any background calibration or active linearization during ADC operation. The design targets a nominal resolution of 16 bits at a Nyquist sampling frequency

of 80 kS/s. In Section II, the proposed DAC is introduced and compared with conventional structures. The SAR ADC architecture is shown and discussed in Section III. Section IV presents the calibration technique. Then, the transistor level circuit details are shown in Section V. Measurement results are presented in Section VI before this paper is concluded in Section VII.

## II. HYBRID DAC FOR HIGH-RESOLUTION SAR ADC

### A. Conventional DAC Structures

The charge redistribution CDAC is the most common implementation within SAR ADCs. Due to its simplicity, it has been preferred over other DAC architectures, with the exception of current mode DACs, for high-speed implementations [7], [18]. Conventionally, a binary-weighted capacitor array is used for low-resolution implementations. However, due to the exponentially growing capacitor array size and limitations related to parasitics and area constraints, a full-resolution binary-scaled capacitor array is not a practical solution for higher resolutions. Therefore, two main approaches are used to implement the DAC in SAR ADCs. The first approach uses a split CDAC, which splits the capacitor array into an MSB array and one or more sub-arrays connected via a series bridge capacitor(s). Thereby, all arrays can share the same unit capacitor size, which saves chip area and relaxes the mentioned layout limitations [19], [20]. Nevertheless, the structure is very sensitive to parasitics related to the bridge capacitor(s), and the whole DAC needs to be calibrated to the full resolution. The second approach uses a hybrid architecture combining both conventional capacitive charge redistribution and resistive voltage scaling DACs [21], [22]. This approach also relaxes the DAC design with a reduced  $C_{\max}/C_{\min}$  ratio, which leads to a reduced area. In fact, both approaches are useful to reduce the overall DAC capacitance and therefore enhance the speed for moderate-resolution ADCs. However, they both require a large calibration and/or linearization effort, which makes them have lower area and power efficiency for high-resolution ADCs.

Therefore, the most power-efficient SAR ADCs employ CDACs at moderate to low speed [1]–[3] and moderate to low resolution. Some use a sub-fF unit capacitor with a custom layout in [3], which was similarly applied in [1], bringing the design close to the  $kT/C$  noise limit. On the other hand, in addition to the basic CDAC architecture and architectural changes, most innovations in the last decade were concerned with switching schemes, where major dynamic power savings were achieved [1], [2].

### B. Incremental $\Sigma\Delta$ DAC for SAR ADC

Two major drawbacks limited the effective resolution of Nyquist rate single-step SAR ADCs: the need for high-resolution calibration and the lack of area- and power-efficient calibration tools to provide it. To remove these limitations, the idea of using an incremental  $\Sigma\Delta$  DAC in the SAR ADC was proposed in [23].  $\Sigma\Delta$  DACs are well known to produce high resolution and linearity, but due to their oversampling and noise-shaping operation, they cannot be directly incorporated into the SAR ADC, since a sample-to-sample conversion is

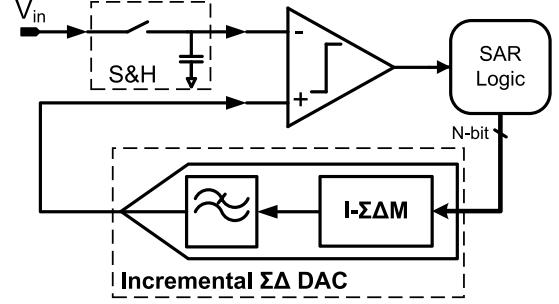


Fig. 1. SAR ADC with incremental  $\Sigma\Delta$  DAC [23].

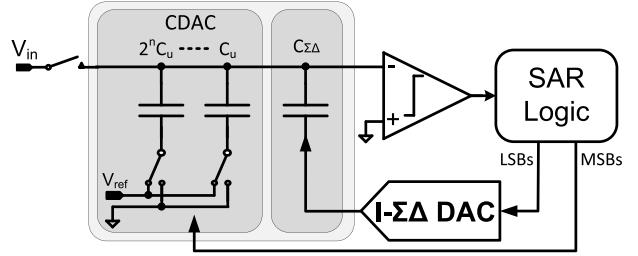


Fig. 2. Conceptual diagram of the hybrid DAC in SAR ADC.

needed. Therefore, it was proposed to periodically reset the  $\Sigma\Delta$  DAC and operate it in an incremental fashion. As shown in Fig. 1, the I- $\Sigma\Delta$  DAC comprises a digital  $\Sigma\Delta$  modulator followed by an analog reconstruction filter. Using a 1-bit modulator output, an intrinsically linear D/A interface is achieved and no DAC calibration is required. In [23], the I- $\Sigma\Delta$  DAC was proposed to achieve the full resolution of the SAR ADC, and the analog reconstruction filter approximated an optimal filter response.

However, the realization of the complete SAR DAC as a single I- $\Sigma\Delta$  DAC with optimized analog filter came mainly with three disadvantages. First, the I- $\Sigma\Delta$  DAC provides unnecessarily a full-resolution output at the SAR logic rate—rather than the overall ADC Nyquist rate—which puts stringent requirements on the power and area of the reconstruction filter. Second, using the optimized filter, the DAC output is available only at a specific time step and does not smoothly settle over time; besides requiring accurate timing, this does not allow one to trade off between speed and redundancy, which is a mandatory feature to relax DAC speed and resolution. Finally, to achieve good noise performance, this implementation required large capacitors for both input sampling and for a full-scale DAC and analog reconstruction filter, besides the high power required for the high-speed full-resolution DAC.

### C. Proposed Hybrid Capacitive and Incremental $\Sigma\Delta$ DAC

To benefit from the CDAC simplicity and the  $\Sigma\Delta$  DAC intrinsic linearity, the proposed DAC introduces a hybrid structure of the two DACs [17]. This allows a high-resolution conversion while depending neither on strict element matching in the CDAC nor on a demanding optimized analog filter for a Nyquist rate I- $\Sigma\Delta$  DAC [23]. Fig. 2 shows a basic diagram of the proposed hybrid DAC, which combines two

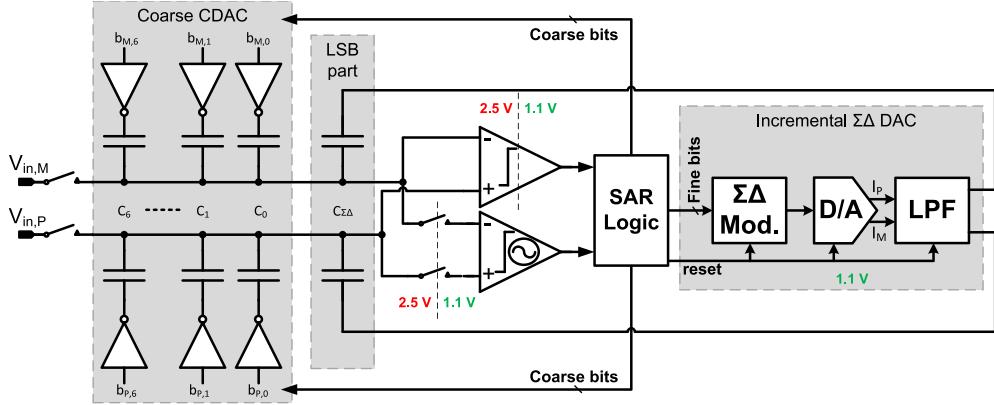


Fig. 3. Proposed SAR ADC architecture.

parts. The first one is an  $n$ -bit binary-weighted capacitor array switched on a common reference voltage  $V_{ref}$  to perform the coarse MSB steps of the SAR search. The second part uses a single capacitor ( $C_{LSB}$ ) with its bottom plate connected to the output of a  $\Sigma\Delta$  DAC for the subsequent least significant bit (LSB) steps. These steps are achieved by applying scaled voltages at the LSB capacitor bottom plate instead of the scaled capacitors. Similar concepts were applied in the hybrid R-C DACs, where the LSB part was achieved with a resistive DAC connected to the bottom plate of the smallest capacitor in the CDAC [22]; similarly, a ramp generator was used in [24]. However, the use of the proposed I- $\Sigma\Delta$  DAC comes with two major advantages: flexibility for bit scaling and intrinsic linearity; together, they both allow for a remarkable extension of the DAC resolution and linearity.

The sampling capacitor in Fig. 2 is formed by both DAC parts, which are connected together at the top sampling plate. Therefore, equivalent to a conventional one-step SAR ADC, the successive search takes place via charge redistribution on the capacitors' top plates throughout the two DAC phases. Scaling  $C_{\Sigma\Delta}$  in Fig. 2 against the CDAC unit capacitor size  $C_u$  allows one to match the  $\Sigma\Delta$  DAC output full scale with the CDAC LSB size, and it optionally defines an additional redundancy between the two DAC parts. The proposed architecture introduces the following advantages compared with conventional SAR ADCs.

- 1) The sampling capacitor size can be solely chosen to fulfill  $kT/C$  noise limits, without upscaling due to  $C_{min}$  or due to matching requirements.
- 2) The CDAC design is highly relaxed since the sampling capacitor is split into fewer fractions, allowing larger unit capacitor size compared with pure high-resolution CDAC designs.
- 3) No matching critical bridge capacitor is needed.
- 4) With 1- or 1.5-bit output, the  $\Sigma\Delta$  DAC linearity is not affected by component mismatch. Thus, calibration is only needed for the coarse CDAC array, and the mismatch between the two parts represents only a gain error on the ADC fine bits, which is easily calibrated.
- 5) The  $\Sigma\Delta$  DAC benefits from a noise-free scaling through ( $C_{\Sigma\Delta}/C_{total}$ ); therefore, also its own output can have rather coarse resolution, which is not required to

satisfy the noise performance corresponding to the full ADC resolution.

- 6) The  $\Sigma\Delta$  DAC input is defined by the digital word from the SAR logic; this introduces great flexibility in defining the SAR search steps and/or adding selective redundancy, while conventionally, these steps are fixed and hard coded during the CDAC design.
- 7) Also the ADC resolution is digitally defined and traded off for speed, where the  $\Sigma\Delta$  DAC allows a reduced or extended resolution by readjustments of the SAR steps and number of  $\Sigma\Delta M$  averaged samples.
- 8) The self-calibration of the CDAC using the  $\Sigma\Delta$  DAC, as detailed in Section IV, allows linearization beyond the nominal resolution.

### III. INCREMENTAL $\Sigma\Delta$ ENHANCED SAR ARCHITECTURE

Fig. 3 shows a block diagram of the hybrid capacitive and incremental  $\Sigma\Delta$  DAC within the proposed SAR ADC architecture.

#### A. Mixed Monotonic and Differential Conversion

The CDAC features a top-plate sampling directly at the coarse comparator inputs, which allows for a sign detection after sampling and before DAC switching. This, together with a monotonically switching CDAC, halves the required DAC unit elements without the need for a second reference in the CDAC [25]. The monotonic switching is only used for the coarse CDAC, while the following LSBs are differentially switched by the  $\Sigma\Delta$  DAC; this avoids any even order harmonics observed by a purely monotonic switching DAC, while the monotonic switching scheme advantageously reduces the common mode (CM) voltage from 2.5 V into the 1.1-V domain during the coarse phase of the SAR search. Fig. 4 shows the transient response of the SAR ADC comparator inputs, exposing the two switching phases within one conversion cycle.

At which position the nominal ADC resolution is split between the two DAC parts represents a design choice, which allows one to balance the complexity of the CDAC against the speed limitation at increased resolution in the  $\Sigma\Delta$  DAC, which obviously needs oversampling for operation. The CDAC

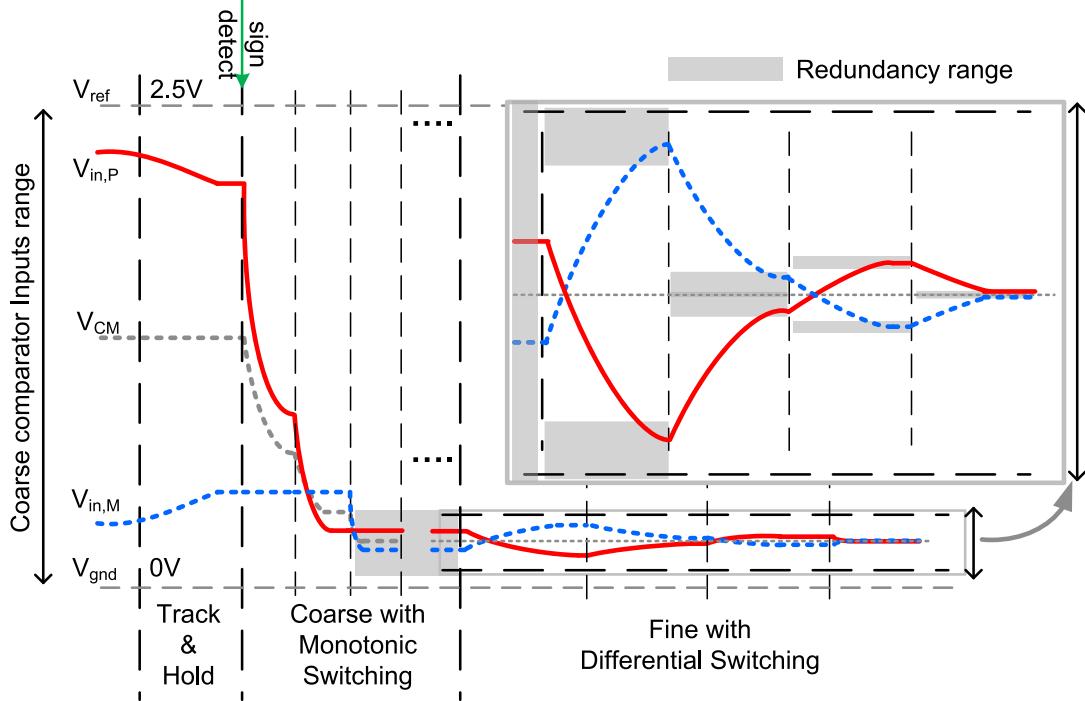


Fig. 4. SAR ADC transient response (comparator inputs).

is not required to satisfy the ADC full resolution but only its own coarse resolution. Therefore, increasing the CDAC resolution moves it from a rather simple layout and design with advantageous matching due to large unit devices, gradually into a more complex design with significant overhead and critical matching. On the other hand, a higher resolution in the  $\Sigma\Delta$  DAC requires longer conversion cycles and stronger filtering after the  $\Sigma\Delta$  DAC, both translating into slower conversion and increased power. In this design, we decided on a simple 7-bit CDAC implementation (whose layout could be almost fully automated), which leaves 9 bits plus redundancy for the  $\Sigma\Delta$  DAC.

#### B. Dual-Comparator Structure

Fully dynamic comparators have been used for low to moderate resolutions achieving remarkably low power levels [1], and combined with comparator noise averaging, they showed further resolution improvement [4], [26]. On the other hand, oscillator-based comparators like the edge-pursuit [5] and eye-opening comparators [27] introduced a more efficient comparator power scaling with reduced overdrive voltage for high-resolution decisions. However, these oscillator-based designs suffered from high sensitivity to CM variations. Therefore, a dual-comparator structure is implemented in this design as shown in Fig. 3 [28]. This includes a fully dynamic comparator for the initial coarse CDAC phase with monotonic switching, where the CM varies significantly, but which is tolerated by the PMOS input dynamic comparator. Subsequently, an eye-opening comparator is used for the later noise-critical comparisons. It works with differential input steps, a small input range, and a fixed CM voltage as shown in Fig. 4, which when combined, significantly relaxes the LSB decisions.

#### C. Incremental $\Sigma\Delta$ DAC

The DAC in Fig. 3 consists of the 7-bit CDAC and an incremental  $\Sigma\Delta$  DAC. The third-order digital  $\Sigma\Delta$  modulator truncates its output by a 1.5-bit quantizer and shapes the quantization noise to high frequencies. The 1.5-bit quantization guarantees an intrinsic linearity without dependence on element matching in the digital-to-analog interface following the modulator in Fig. 3. The last block of the  $\Sigma\Delta$  DAC is an analog low-pass filter, which suppresses the shaped noise from the modulator and drives the bottom plate of the LSB capacitor ( $C_{\Sigma\Delta}$ ) in Fig. 3. The ADC nominal resolution is digitally determined by the SAR logic and is only limited by the noise suppression in the analog filter, while featuring a reconfigurable  $\Sigma\Delta$  modulator. To prevent any memory effect in the ADC and ensure a Nyquist rate operation with a sample-to-sample input output conversion, the  $\Sigma\Delta$  DAC is reset after every single SAR conversion, thus making the  $\Sigma\Delta$  DAC operate incrementally. The  $\Sigma\Delta$  DAC could also be reset after every fine bit decision during a SAR conversion, but this turned out to be disadvantageous: for a single conversion, the memory of the  $\Sigma\Delta$  DAC successively tracks the actual input value, and does not lead to distortion but to an even faster settling, whereas multiple resets would need the new value to be built up from zero, which would require more settling time.

#### D. Input Sampling and Dual Supply Operation

The hybrid architecture allows to benefit from two supply voltages. The input sampler, the 7-bit CDAC, and the coarse comparator operate at 2.5 V in Fig. 3, which allows one to increase the input full scale signal, which is sampled at the higher supply, and therefore reduces the required—noise

limited—sampling capacitance. The fine comparator together with the  $\Sigma\Delta$  DAC and the logic circuits operate at 1.1 V in Fig. 3, which reduces their power consumption and implementation area by fully benefiting from transistor scaling.

### E. Redundancy

Conventionally, redundancy is used to relax the DAC settling in SAR ADCs at high sampling frequencies. However, although the proposed ADC targets high resolution at relatively low conversion rates, redundancy within the SAR steps is essential for the proposed design. A redundancy range after the coarse conversion allows for later correction for errors within the coarse phase. The redundancy also allows recovery of the offset mismatch at the hand-over point between the two comparators (coarse to fine phase). Moreover, redundancy during the fine conversion of the  $\Sigma\Delta$  DAC relaxes its output settling by allowing a faster non-complete settling to full resolution at intermediate steps of the  $\Sigma\Delta$  DAC.

Consequently, a redundancy bit is added at the beginning of the fine phase, which allows one to recover all errors below the 7-bit CDAC accuracy in the coarse phase (offset, mismatch, and erroneous decisions). Furthermore, sub-binary steps with 1.8 radix are used for the fine conversion with the  $\Sigma\Delta$  DAC. Advantageously, in the proposed architecture, the  $\Sigma\Delta$  DAC redundancy can be digitally reconfigured and optimized and its implementation is explained in Section V-B.

## IV. SELF-CALIBRATION

Calibration of the CDAC is required for any SAR ADC with above moderate resolution [5], [14]. It is often accompanied by mismatch shaping, dithering, or other linearization techniques to achieve medium to high resolution [4], [9], [10], [26]. The calibration takes place either once at startup or during ADC operation, also either continuously in the background or occasionally in the foreground. In most cases, a dedicated analog component (an auxiliary DAC for instance) is required to perform the calibration; the accuracy of this component mostly determines the calibration performance [29].

### A. Calibration Concept

1) *CDAC Linearity*: The binary-weighted coarse CDAC will have a manufacturing related mismatch, which needs calibration. Therefore, the CDAC capacitors are estimated with at least the full ADC resolution in order to digitally correct them. In the proposed hybrid DAC, the  $\Sigma\Delta$  DAC is a suitable and efficient measurement tool for CDAC calibration.

2) *CDAC Scale Mismatch*: The full scale range of the  $\Sigma\Delta$  DAC has to be matched to the LSB size of the CDAC (including redundancy). Otherwise, a gain error between the coarse and the fine digital outputs would appear.

3) *Hybrid Comparator Offset*: A large offset mismatch between the coarse and the fine comparator could cause the voltage range, into which the coarse conversion phase steers the CDAC voltages, to be outside the conversion range of the fine DAC as indicated in Fig. 4. An offset mismatch larger than the maximum input range of the fine DAC must be avoided,

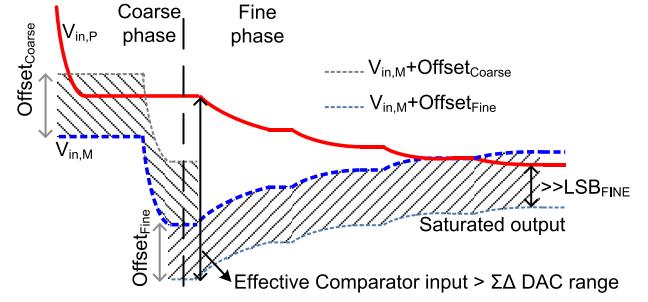


Fig. 5. Large hybrid comparator offset mismatch leading to saturated DAC output.

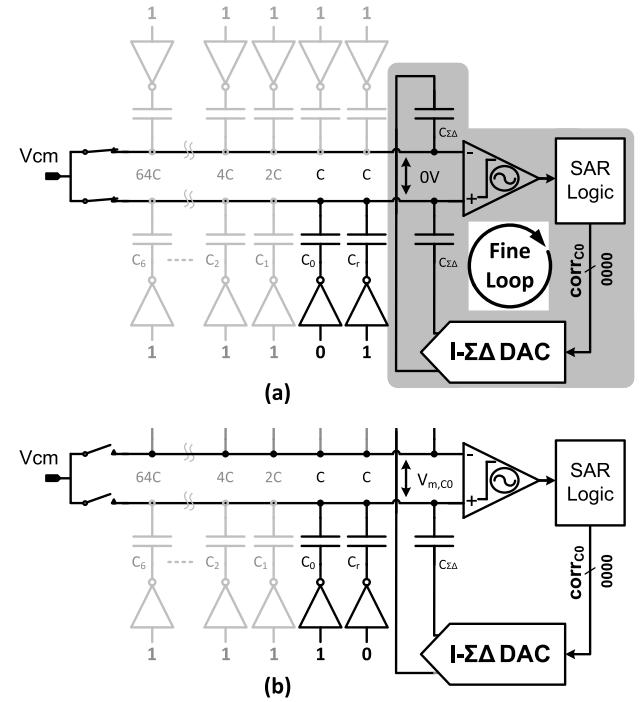


Fig. 6. SAR ADC calibration of the positive CDAC LSB. (a) Zero sampling. (b) Charge redistribution.

as illustrated in Fig. 5. Since designing the redundancy for the worst case offset mismatch would lead to extended SAR conversion time, this was avoided by using an additional low-resolution CDAC for offset compensation.

### B. Calibration Procedure

1) *CDAC Error Estimation*: The mismatch error estimation is achieved by measuring the individual capacitors in the CDAC using the fine loop of the SAR ADC (SAR,  $\Sigma\Delta$  DAC, and fine comparator). So as not to saturate the  $\Sigma\Delta$  DAC output, only the capacitor mismatch is measured instead of the total capacitance [30]. The estimation starts with the LSB capacitor in the CDAC, which is measured against an additional reference capacitor  $C_r$  with nominally equal size, as shown in Fig. 6. The estimation is continued to the larger capacitors until the MSB capacitor, which is measured against the sum of all smaller capacitors to the right of the MSB

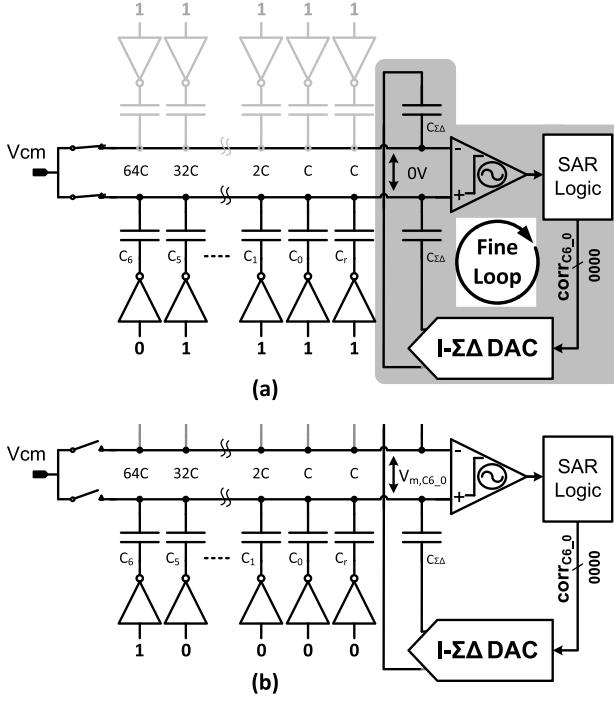


Fig. 7. SAR ADC calibration of the positive CDAC MSB. (a) Zero sampling. (b) Charge redistribution.

in Fig. 7, and the previously estimated mismatch values on these smaller capacitors are accumulated accordingly.

2) *Mismatch of  $C_r$ :* Since  $C_r$  represents the calibration reference, upon which  $C_0 - C_6$  are calibrated, a mismatch in  $C_r$  does not affect the linearity of the CDAC. But a mismatch in  $C_r$  still leads to a gain error between the CDAC and the  $\Sigma\Delta$  DAC. Therefore, the actual digital representation of  $C_r$  is estimated using the same calibration concept, except without swapping the switching with another CDAC capacitor. Therewith, a digital representation of the actual  $C_r$  is obtained relative to the  $\Sigma\Delta$  DAC, which matches the gain error between the two DAC parts.

3) *ADC Output Correction:* Identical to the explanation above and as indicated in Figs. 6 and 7 for the positive CDAC, the digital correction values are estimated for the negative CDAC. This whole calibration is run once at startup, when the estimated digital correction values are stored, while the stored correction values are then operated continuously on the SAR ADC output. The output correction is performed by an arithmetic addition of the appropriate digital correction values to the ADC digital output.

## V. CIRCUIT IMPLEMENTATION

### A. Input Sampling and Capacitor Array

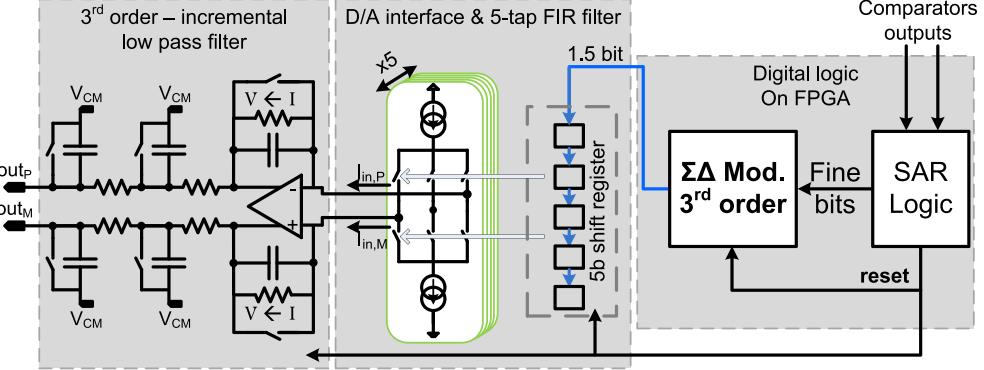
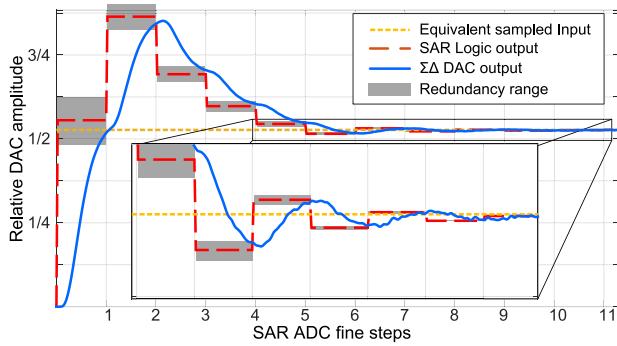
The ADC features top-plate sampling of the analog inputs using a pair of boot-strap switches operating at 2.5 V. The sampling switches receive the sampling clock after buffering and boosting it close to double the supply voltage. Each switch is connected to one of the two common top plates of the CDAC arrays, which are also connected to the two comparator inputs, respectively. Due to the hybrid DAC structure, there is

basically no matching related requirement on the unit capacitor size, as it forms only a 7-bit array. Therefore, the sampling capacitance is solely sized for a 16-bit kT/C noise level, which yields 16 pF as the sampling capacitance for each CDAC side for an approximate 4 V<sub>p-p</sub> differential input voltage. The low linearity requirements, the relaxed switching speed of the CDAC, and the added redundancy at the end of the coarse conversion phase allow for a standard binary-weighted implementation of the C-array. The CDAC is implemented using metal–oxide–metal (MOM) capacitors with a unit capacitance of 127.6 fF. This comparably large unit capacitor highly relaxes the CDAC layout, which was even semi-automated in a patterned fashion both for unit cells positioning and internal routing.

### B. Incremental $\Sigma\Delta$ DAC With Analog Reconstruction Filter

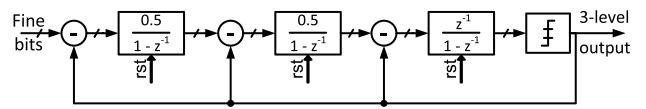
Fig. 8 shows the implementation of the I- $\Sigma\Delta$  DAC in the proposed architecture in Fig. 3. The digital  $\Sigma\Delta$  modulator receives a reset signal, which always brings the DAC to the same initial state before a new ADC conversion. The same reset signal also nullifies the state of the analog reconstruction filter in Fig. 8. Within an ADC cycle, both the  $\Sigma\Delta$  modulator and the LP-filter do not see the reset signal and feature a transfer function as a normal LP  $\Sigma\Delta$  DAC. The digital  $\Sigma\Delta$  modulator receives the fine bits as a digital input from the SAR logic. In this prototype, the digital part comprising the SAR logic and the  $\Sigma\Delta$  modulator was implemented on a field programmable gate array (FPGA) for the sake of debugging, reconfigurability, and testing flexibility. The three-level output of the  $\Sigma\Delta$  modulator is converted to the analog domain by a current mode finite impulse response (FIR) filter, which feeds an active RC followed by two passive RC low-pass stages to obtain an overall third-order low-pass reconstruction filter of the I- $\Sigma\Delta$  modulator. The filter linearity defines the overall ADC linearity, but the  $\Sigma\Delta$  DAC output benefits from passive downscaling by the feed-in factor  $C_{\Sigma\Delta}/C_{total}$  to the comparator inputs in Fig. 3, which relaxes its linearity requirements. However, better linearity in the DAC allows one to acquire better calibration beyond ADC limits, since during calibration the thermal noise-limited resolution can be improved by averaging, whereas the linearity would not benefit at all.

1)  *$\Sigma\Delta$  DAC Steps and Filter Output Settling:* The last SAR step using the coarse CDAC is about 18 mV, due to binary scaling of the 2.5-V reference and the additional attenuation due to  $C_{\Sigma\Delta}$  and the offset CDAC. To achieve 1-bit redundancy, the  $\Sigma\Delta$  DAC full-scale step at the comparator input equals  $2 \times 18$  mV; therefore, the  $\Sigma\Delta$  DAC full scale is about  $FS_{\Sigma\Delta} = 0.77$  V, due to scaling by  $(C_{total}/C_{\Sigma\Delta})$ . Instead of conventional binary scaling, the  $\Sigma\Delta$  DAC uses redundancy through non-binary 1.8-radix steps, to relax the output settling as illustrated in Fig. 9. Therefore, the output is scaled with weights of  $FS_{\Sigma\Delta}/1.8^n$  ( $n = 1 : 12$ ), by, respectively, scaling the digital word to the  $\Sigma\Delta$  DAC. This redundancy allows errors up to 5% during the intermediate steps (less than 5-bit accuracy), instead of 0.1% which is required for 10-bit settling. Therefore, the required settling time is reduced from  $7\tau$  (10 bits) to  $3.5\tau$  (5 bits), where  $\tau$  is

Fig. 8. Incremental  $\Sigma\Delta$  DAC with input and control from the SAR logic.Fig. 9. Transient response of the  $\Sigma\Delta$  DAC output in the SAR ADC.

the reconstruction filter time constant. The filter characteristic is determined by system level simulation, which provides a tradeoff between the filter cut-off frequency and the output settling time (equivalent to  $\Sigma\Delta M$  over sampling ratio (OSR)) to reach the required output accuracy. Therefore, the filter is designed with a cutoff at 800 kHz and the values of  $R$  and  $C$  satisfying this cutoff are chosen to have a similar area consumption for a better layout.

**2) Digital Modulator:** Fig. 10 shows the implemented  $\Sigma\Delta$  modulator; it is a single-loop third-order 1.5-bit  $\Sigma\Delta$  modulator [31]. A 1.5-bit architecture was selected to avoid a multi-bit DAC with its own non-linearity. A multi-stage noise shaping structure is not used to avoid matching problems in the reconstruction filter. A third-order architecture was chosen as a compromise between reconstruction filter complexity and reasonable sampling frequency. The three-level quantizer and the incremental operation allow for more aggressive scaling of the coefficients compared with free-running  $\Sigma\Delta$  [31]. Thus, the optimal scaling from [31] was further optimized in MATLAB in a constrained fashion for high signal to quantization noise ratio and for using only binary-weighted scaling, which can be implemented using binary shifts in order to avoid digital multipliers in the implementation. This results in close to optimal scaling and does not limit the DAC performance. The  $\Sigma\Delta$  modulator operates at 150 MHz and the I- $\Sigma\Delta$  DAC uses 100 samples per conversion for a 9.5-bit Nyquist rate resolution. This was based on the  $\Sigma\Delta$  DAC

Fig. 10. Third-order incremental digital  $\Sigma\Delta$  modulator.

system simulation including filter settling, to achieve an ADC sample rate of 80 kS/s. Fig. 11 includes a time diagram of the SAR ADC showing the time allocated for each SAR step during one conversion at 80 kS/s.

**3) Current-Mode FIR Filter:** The incremental  $\Sigma\Delta$  modulator digital output has to be filtered by an analog reconstruction filter. Feeding the 1.5-bit output signal directly into an active  $RC$  filter would put stringent requirements on the operational amplifiers, since the 1.5-bit signal would include full scale steps at the full rate of the digital modulator. Consequently, in the proposed implementation, the  $\Sigma\Delta$  output is smoothed by a five-tap current-mode FIR filter before being fed to the active  $RC$  filter, as shown in Fig. 8.

Fig. 12 shows the behavioral model simulation results of the  $\Sigma\Delta$  DAC; thereby, the FIR filter coefficients include a random mismatch with 10% variance. The 1000-point histogram shows that the signal to noise and distortion ratio (SNDR) remains within 1 dB of the nominal value, with a  $3\sigma$  yield; therefore, matching constraints on current elements are very relaxed. To generate the 1.5-bit output levels, a bipolar current tap is used with  $2\text{-}\mu\text{A}$  unit current, as shown in Fig. 13. The intrinsically linear three-level current output is obtained by simultaneously switching a single PMOS and NMOS current source per tap as p/m, m/p, or z/z on the CM voltage, where p is positive, m is negative, and z is dump. The cascode transistors are biased in the sub-threshold region to provide a high output impedance and allow low-voltage operation together with the switches, which use low threshold voltage transistors.

Due to process, voltage, and temperature (PVT) variations, a high gain error at the  $I$ -to- $V$  conversion through the active  $RC$  could potentially limit the DAC range. Therefore, a reference current is generated via  $V$ - $I$  based biasing [32]. This is achieved using a reference voltage regulated over a resistor that has the same size and shape and is placed close

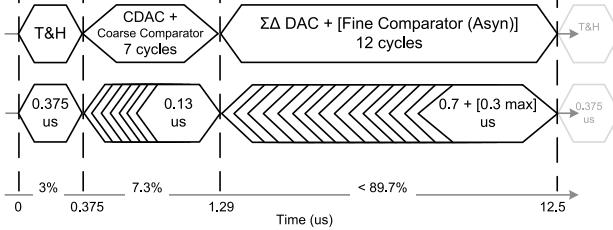
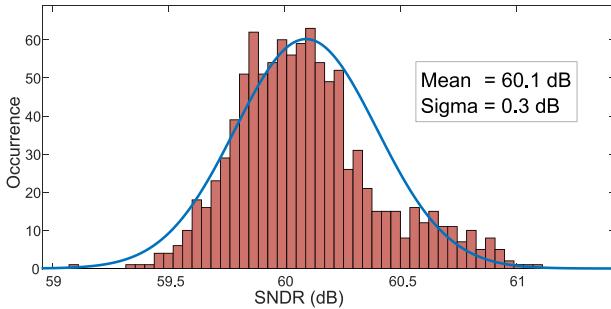


Fig. 11. SAR ADC time diagram for 80-kS/s operation.

Fig. 12. SNDR histogram of the  $\Sigma\Delta$  DAC with 10% random mismatch on the FIR filter tap coefficients, in a behavioral simulation.

to the resistor performing the  $I$ -to- $V$  conversion. Thereby, the biasing voltages of the current tap in Fig. 13 are generated by mirroring this reference current, which heavily reduces the impact of process- and temperature-related gain errors.

4) *Amplifier Design*: From Fig. 8, the op-amp within the active  $RC$  filter drives two low-pass  $RC$  stages; therefore, its output settling speed and stability are relaxed. Also, a limited gain-bandwidth does not degrade the filter linearity; it even leads to a minor increase to the effective low-pass filtering. Nonetheless, the amplifier is required to stabilize the output of the preceding current sources fast enough to prevent any input dependent distortion at the D/A interface. Moreover, the op-amp must allow the DAC full-scale swing at its output and provide a dynamic current to drive the passive  $RC$  stages fast enough to not slow down the fine conversion loop. The op-amp features a three-stage positive feedback structure [33], shown in Fig. 14. A class-AB output stage dynamically drives the load without any major output swing limitation. The biasing voltages are generated with local current mirrors, which receive and regenerate a common reference current from an on-chip beta-multiplier circuitry. The CM feedback error amplifier (not shown in Fig. 14) is a replica of the first stage but with NMOS diode load. The op-amp has a gain-bandwidth product of 62 MHz after  $RC$  extraction.

5)  $\Sigma\Delta$  DAC Reconfigurability: Unlike conventional SAR design, where the LSB size is physically fixed in the CDAC design, the LSB size in this design is defined by the digital word at the input of the  $\Sigma\Delta$  DAC, its architecture, and sampling rate. Therefore, the LSB size can be digitally readjusted, up to a limit allowed by the analog filter performance. Simulations show that about 3-bit increased performance (above nominal design) can be obtained by adjustments of the SAR steps and OSR without changing the analog filter. This flexibility comes at a minor cost of extended digital signal representation

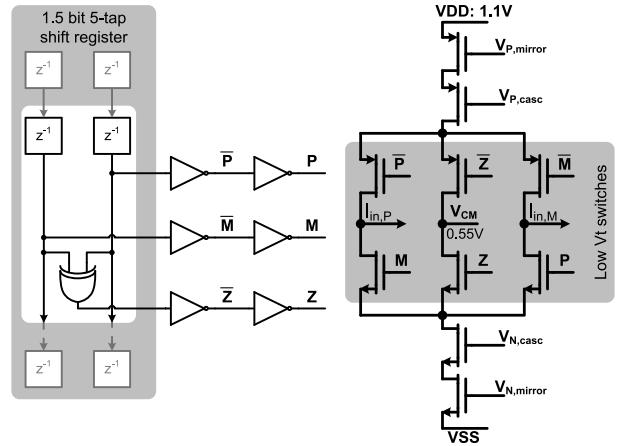


Fig. 13. 1.5-bit current tap of the semi-digital FIR filter with control signals from the shift register.

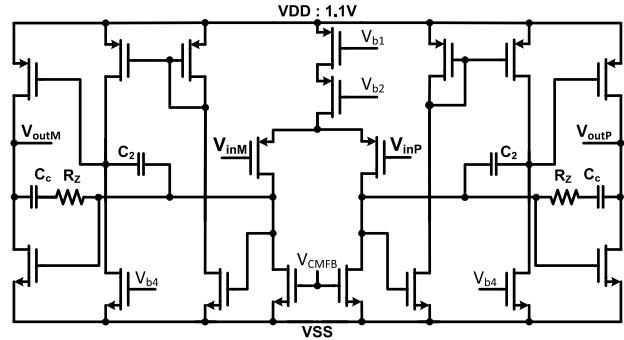


Fig. 14. Three-stage positive feedback compensation op-amp.

and higher OSR of the  $\Sigma\Delta M$ , while both are associated with higher power when used. But it allows for configurability after manufacturing; if only the reduced resolution is used, there is no extra power, because the additional bits would simply not be switched. This possibility of extending the nominal resolution can be beneficially used during calibration of the coarse CDAC with the fine  $\Sigma\Delta$  DAC in order to extend the calibration accuracy and thus the achieved linearity.

### C. Hybrid Comparator Implementation

1) *Dynamic Comparator With Dual Supply*: The coarse comparator resolves the seven MSB decisions based on the CDAC, which are followed by a redundancy decision within the fine conversion phase to recover errors below the seventh MSB size. The coarse comparator receives differential inputs with a varying CM, which is conceptually a drawback of the monotonic switching, as it may result in a varying comparator offset potentially leading to output distortion. However, the always decreasing and signal-independent CM voltage of the monotonic switching scheme is turned into an advantage for this design as it allows one to move from the high supply used for input sampling to the low supply used in the fine comparator. Simultaneously, the errors due to CM changes do not exceed the 7-bit coarse accuracy. Therefore, they will be

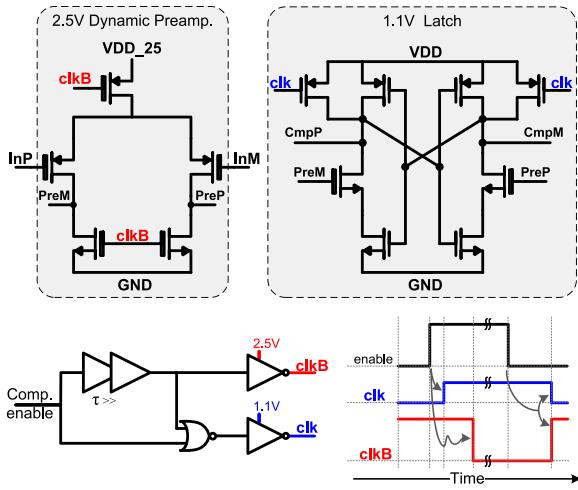


Fig. 15. Dynamic coarse comparator with overlapping clocks.

covered by the redundancy and cured using the hybrid DAC and comparator concept.

The coarse comparator operates from the 2.5-V supply and employs a fully dynamic structure similar to [4] and [28]. PMOS input transistors are used in the dynamic preamplifier, to manage the decreasing CM voltage. A dynamic latch with reset follows the preamplifier. It operates at the core 1.1-V supply, while having 2.5-V input transistors to translate the preamplifier differential voltage into a regeneration current difference. The comparator circuit implementation is shown in Fig. 15 together with the clock generation for the two stages. The overlapping clocks are needed to release the latch reset before receiving the preamplifier dynamic differential output.

2) *Eye-Opening Comparator Implementation:* A voltage-controlled oscillator (VCO)-based eye-opening comparator is used for the fine decisions of the SAR ADC as in [27]. Conventional low-noise comparators consume high power during all SAR decisions, while comparators based on majority voting can step into a low-noise high-power mode (or use redundant decisions) based on additional logic for metastability sensing [4]. On the other hand, the eye-opening comparator smoothly scales the power consumption with its overdrive over SAR decisions without a need for additional sensing circuitry. The basic concept is that the differential input is fed into two competing current-starved VCOs. Even with a small voltage difference, the VCOs will develop a significant phase difference over time and a decision is made, when this phase difference is large enough. Thus, the “eye” is automatically opened for the decision [27]. The thermal noise is present as jitter at the inverter outputs and is integrated both over the inverter chains and also over time, and therefore the noise is averaged while the signal is integrated. The phase detector (PD) implements a dead zone, which prevents a latching decision due to jittery phase shifts. Therefore, the dead zone in the PD determines the noise level and the comparator delay by preventing fast decisions.

In contrast to the original implementation, in the proposed hybrid concept with the monotonically switched coarse CDAC,

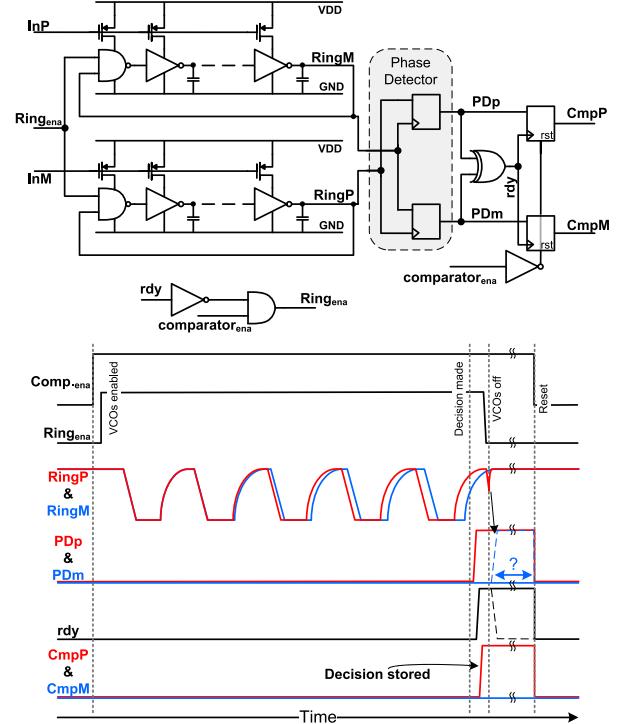


Fig. 16. VCO-based eye-opening comparator with automatic turn-OFF and output storage logic.

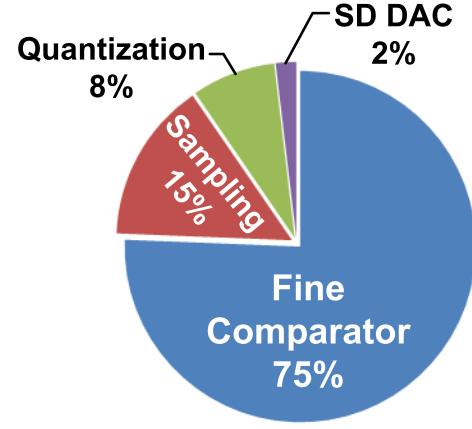


Fig. 17. ADC noise breakdown based on transient simulations.

the fine conversion phase receives a relatively small input range with differential switching, as indicated in Fig. 4. This relaxes the implementation effort. Fig. 16 shows the schematic of the eye-opening comparator used in this design. The limited input range allowed the exclusion of the time amplifier [27] by adaptation of the dead zone in the PD, which also reduces the mismatch. The comparator receives an enable signal from the SAR logic, and then it enables the internal VCOs; thereafter, the VCOs automatically turn OFF after decision making to save their dynamic power, which is dominantly consumed in the two VCOs. To prevent erroneous decisions due to a wrongly re-latched disable edge (at the falling edge of Ring<sub>ena</sub> in Fig. 16), two flip-flops were added to store the PD decisions and provide the comparator output.

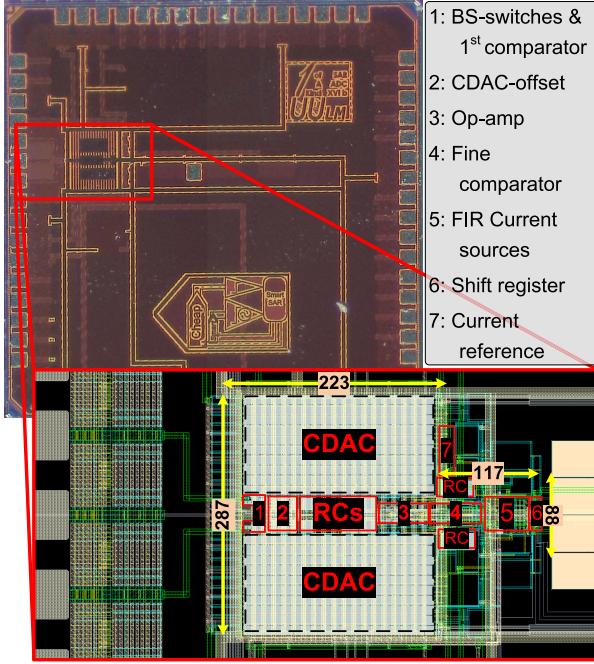


Fig. 18. SAR ADC chip photograph and layout.

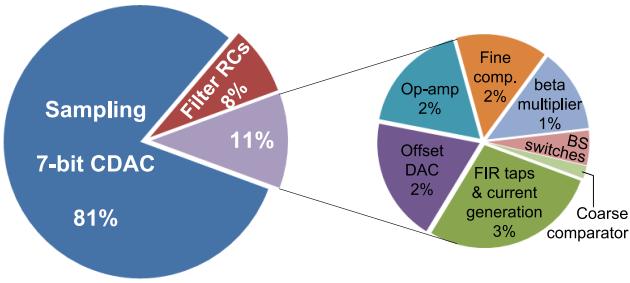


Fig. 19. Approximate distribution of the area consumption.

3) *Coarse Offset Mismatch Compensation:* Based on the mismatch simulation, the offset in the coarse comparator has a standard deviation of about 18 mV, and about 4 mV for the eye-opening comparator, with the expectation of some increase of the eye-opening comparator offset, due to non-available statistical models in the process design kit files for the used “moscaps”. Since designing the redundancy for the worst case offset mismatch would lead to extended conversion time, this was avoided by adding a small 4-bit CDAC for offset calibration. Therefore, the redundancy is designed to recover errors (including offset) within an LSB of the coarse CDAC, which is about 18 mV, which recovers a major part of the offset mismatch. On the other hand, the offset calibration CDAC is used to cover the worst case mismatch with a full scale of 68 mV. The offset compensation CDAC is a 4-bit differentially switched capacitor array; it has an MSB size equal to  $2C_{LSB}$  of the coarse CDAC. Therefore, it does not consume any mentionable area. An important aspect for using this compensation is that it neither requires calibration nor does it need to match the CDAC capacitors, which all makes

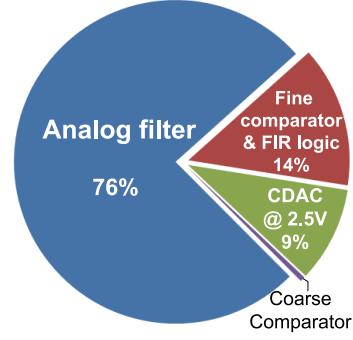


Fig. 20. Distribution of the chip core power consumption.

it a quite affordable solution to safeguard against excessive offset mismatch.

#### D. Noise Breakdown

In conventional SAR ADCs with CDAC, the ADC noise is mainly determined by the comparator noise besides the sampling noise. In the proposed design, the  $\Sigma\Delta$  DAC is an additional noise source through the analog reconstruction filter. However, the  $\Sigma\Delta$  DAC output benefits from noiseless scaling (to the ADC input) by  $C_{\Sigma\Delta}/C_{\text{total}} = 6/128$  (see Fig. 3); equivalently, the filter noise can be around 27 dB higher than the comparator noise; therefore, it is very relaxed. Fig. 17 shows the ADC noise breakdown, which is dominated by the comparator noise, while the filter noise in the  $\Sigma\Delta$  DAC adds a non-significant share of 2%.

## VI. MEASUREMENTS

The proposed SAR ADC with the hybrid DAC was fabricated in a 40-nm CMOS process with an active area of only  $0.074 \text{ mm}^2$ . Fig. 18 shows the die photograph with the ADC layout. An approximate distribution of the area consumption is shown in Fig. 19. The active area is dominated by the sampling capacitor concurrently forming the coarse CDAC array, which was scaled for 16-bit performance. Given the dominance of the CDAC area consumption, the advantage of the hybrid DAC using the  $\Sigma\Delta$  modulator becomes very obvious. If a 16-bit CDAC would need to be scaled for matching, its size would be significantly larger and thus would produce a larger area consumption. The second dominant area consumption (though non-comparable with the CDAC) comes from the RC filters used in the analog low-pass filter in the  $\Sigma\Delta$  DAC and the relatively big resistors used for biasing and reference current generation. Still, the RC filters only need 10% of the CDAC.

The ADC core power consumption was estimated from parasitic-extracted simulations to be  $101 \mu\text{W}$ , while in the measurements, the analog filter and reference generation caused a 10% increase to approximately  $110 \mu\text{W}$ . Fig. 20 shows the power consumption distribution. In this first prototype, the analog filter is the dominant power consumer with more than three quarters of the total consumption, which is mainly statically consumed from the 1.1-V power supply. On the other hand, only about 9% of the power is

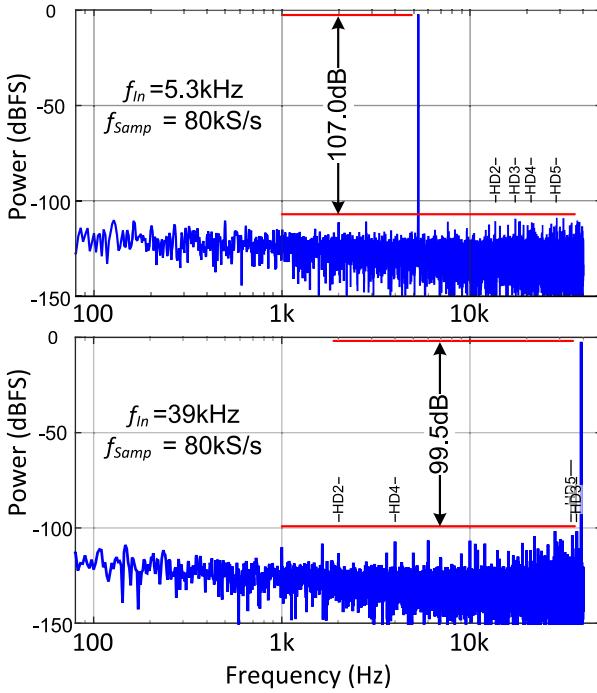


Fig. 21. SAR ADC output spectra.

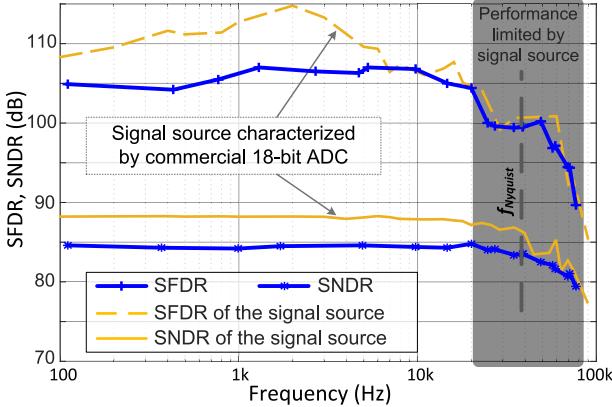


Fig. 22. Measured SAR ADC dynamic performance in the first and second Nyquist bands.

consumed from the 2.5-V CDAC reference, and less than 1% is consumed from the 2.5-V power supply. A synthesis of the digital part (currently implemented on an FPGA) in the same technology using Synopsys software occupied less than 5% of the reported area and consumed about 30% of the reported power consumption; this shows that the area is insignificant, but the power consumption could be reduced in the next prototype by choosing a  $\Sigma\Delta$  DAC with higher order, thus a lower sampling rate, and using low-power digital libraries.

The ADC is measured at a sampling frequency ( $f_S$ ) of 80 kS/s, with a full-scale sinusoidal input. Fig. 21 shows ADC output spectra for two input frequencies. The measured peak SFDR is 107 dB, and SFDR remains above 104 dB for input frequencies below  $f_S/4$ . Beyond  $f_S/4$ , the SFDR is limited

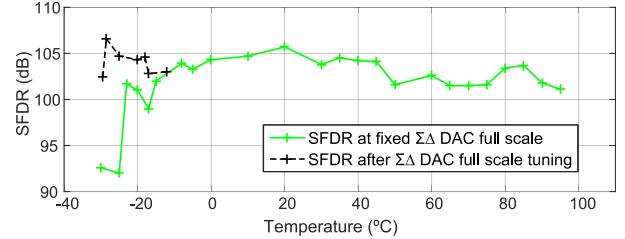


Fig. 23. Measured SFDR over temperature variation.

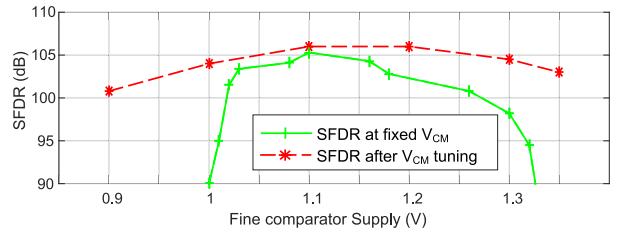


Fig. 24. Measured SFDR over supply voltage variation.

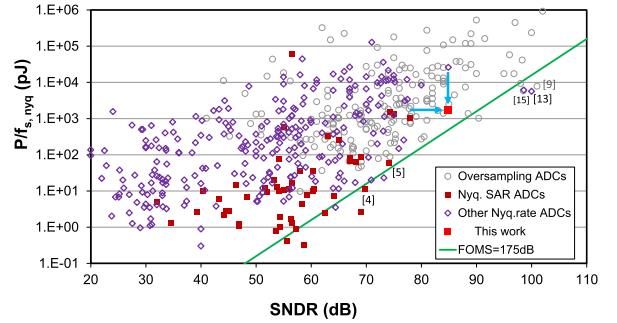


Fig. 25. State-of-the-art ADCs' performance: energy/Nyquist sample [34].

by the quality of the used signal source (Stanford Research DS360). Fig. 22 shows the measured SNDR and SFDR over input frequencies of the presented prototype together with the measurements of an 18-bit commercial ADC [35] (applying the same signal range as that used for chip measurements), to determine the limitation of the source.

The measured SNDR is 84.8 dB at an input frequency of  $f_S/4$ ; it remains above 83.5 dB for the entire Nyquist-bandwidth, which is about 10 dB above the state-of-the-art performance for Nyquist rate SAR ADCs [34]. The ADC is measured also in the second Nyquist band, where the SNDR and SFDR are mainly limited by the signal source; nonetheless, the measured SNDR and SFDR up to 71 kHz remain above 81 and 94 dB, respectively.

#### A. Measurements Over Temperature and Voltage Variation

Due to PVT variations, the scaling factor between the coarse and fine DAC outputs can drift from its nominal value. This is corrected by a digital calibration of the gain error between the two parts (one element calibration). This gain correction could be even integrated as a background calibration, for example, by dedicating one time slot per SAR conversion cycle, in a similar fashion to the background offset calibration in [36].

TABLE I  
PERFORMANCE SUMMARY AND NYQUIST RATE ADCS' COMPARISON

	Harpe [4] ISSCC'14	Bannon [14] VLSI'14	Xu [13] ISSCC'17	Krämer [7] JSSC'15	Shim [5] JSSC'17	Zhang [12] JSSC'17	This work
Architecture	SAR	Pipe. SAR	Pipe. SAR	SAR	SAR	I- $\Sigma\Delta$	SAR
Technology	60 nm	180 nm	65 nm	40 nm	40 nm	180 nm	40 nm
Resolution (bit)	14	18	14 (8+10-red.)	14	15	16	16
Area (mm <sup>2</sup> )	0.18	5.74	0.342	0.236	0.315	0.5	<b>0.074</b>
Power Supply (V)	0.8	5 / 1.8	not rep.	2.5 / 1.2	not rep.	1.5	2.5 / 1.1
Power ( $\mu$ W)	0.35	30520	21800	54500	1.17	34.6	110 + 30 <sup>+</sup>
f <sub>s,nyq</sub> (kS/s)	32	5000*	35000	35000	20	2	80
SNDR <sub>nyq</sub> (dB)	69.7	98.6*	75.1	74.4	74.1	96.1**	<b>83.5<sup>x</sup>- 84.8</b>
SFDR (dB)	78.5	not rep.	90-103.1	90-99	78-95.1	not rep.	<b>99.5<sup>x</sup>- 107</b>
FOM <sub>S</sub> (dB)	176.3	177.7*	164.2	159.5	173.4	170.7**	168.1 <sup>x</sup> -169.4

\* Reported for single input at  $f_{in} = f_s/5000$ . <sup>x</sup> limited by the accuracy of the signal generator cf.22

\*\* Reported at  $f_{in} = 800$  Hz.

+ Additional power estimated for digital.

Fig. 23 shows the measured SFDR, which remains above 100 dB for the whole temperature range—except for very low temperatures, where the drop is mainly due to an excessively decreased full scale of the  $\Sigma\Delta$  DAC leading to a saturated fine DAC output. To verify this, the dashed curve in Fig. 23 is measured after externally up-tuning the  $\Sigma\Delta$  DAC full scale.

Also, supply variations can affect the ADC performance; especially as the fine comparator shows a sensitivity to CM changes, it is equivalently affected by supply changes. In Fig. 24, the measurement results are shown over supply change of the fine comparator. The solid curve shows the drop in performance due to a changing supply voltage; even though almost  $\pm 10\%$  supply variation is tolerated while SFDR is above 100 dB, the performance drop is obvious. As a countermeasure, the red dashed curve shows the same measurements over supply change, but with the CM ( $V_{CM}$ ) tuned to track the supply changes. This keeps the SFDR over 100 dB for a supply voltages from 0.9 to 1.35 V. Advantageously,  $V_{CM}$  tuning could be implemented by readjusting the reset phase of the monotonically switched CDAC based on the supply voltage variation.

### B. Performance Comparison

Fig. 25 compares the power efficiency of the design to the state of the art: all other reported Nyquist rate ADCs in state-of-the-art survey [34] are one order of magnitude worse in either power efficiency or performance. Only [14] (and its

recent application in [16]) reported higher Nyquist rate performance, but measurements are reported only at a single input frequency of  $f_{in} = f_s/5000$ , without specifying dynamic linearity (SFDR). Also, [14] consumes about 75x higher core area than the presented design. On the other hand, commercial ADCs reported higher performance as in [37]. Table I presents a design summary and comparison with a selection of state-of-the-art Nyquist rate ADCs performing high-resolution high-efficiency conversion. As discussed in Section I, I- $\Sigma\Delta$  ADCs—despite oversampling the input—perform a Nyquist rate operation and provide very high resolution for relatively low conversion rates. Due to the DAC hybrid nature in the proposed SAR ADC, the I- $\Sigma\Delta$  DAC provides only coarse resolution; therefore, it features relaxed speed and noise requirements compared with I- $\Sigma\Delta$  ADCs, which makes it a better candidate especially for higher conversion rates. According to Table I, the presented prototype competes the state of the art in terms of linearity; in contrast to the state of the art, this is achieved not at the cost of more area consumption, but even at the lowest reported area.

### C. Calibration Beyond ADC Resolution

The measured superior linearity is achieved by the proposed hybrid DAC and by a one-time calibration of the coarse CDAC using the available intrinsically linear  $\Sigma\Delta$  DAC. The use of the  $\Sigma\Delta$  DAC is advantageous for the calibration performance. First, the calibration nominal resolution is improved by reducing the SAR LSB fine step below the one used for ADC normal

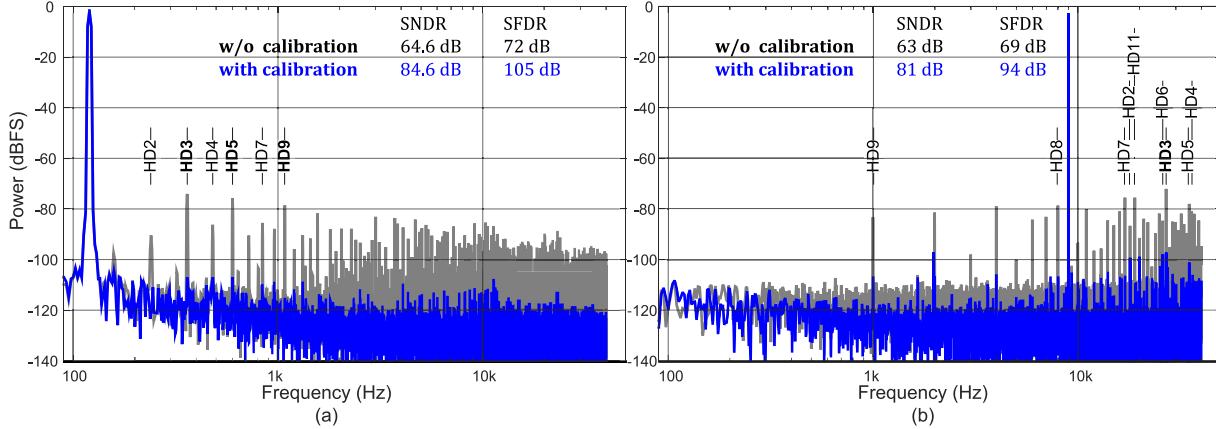


Fig. 26. SAR ADC output spectra with and without calibration at  $f_{\text{Smp}} = 80 \text{ kS/s}$ . (a)  $f_{\text{in}} = 120 \text{ Hz}$ . (b)  $f_{\text{in}} = 71 \text{ kHz}$ .

operation, together with relaxed timing during the startup calibration. Also, the  $\Sigma\Delta$  modulator performance benefits from relaxed timing. However, with the aforementioned modifications, the calibration output would be limited by random fluctuation due to noise. Nevertheless, this fluctuation together with (white) sampling noise is averaged out by repeated measurements. Therefore, to improve the calibration performance above the ADC effective resolution,  $2^8$ -time oversampling has been used during calibration. Finally, the influence of the low-frequency noise within the SAR loop (mainly in the comparator) and the sampling distortion is also reduced. This is achieved by repeating the conversion in one calibration step, first on the zero sampled input, then after CDAC switching (including mismatch effect as described in Section IV), and subtracting the two. This attenuates the low-frequency noise in a similar fashion to correlated double sampling. Thereby, a factor of  $x2$  more samples is required. Consequently, calibration requires about  $2^{13}$  Nyquist cycles for  $2 \cdot 8$  capacitors in the CDAC.

Together, this allows one to perform the calibration beyond the SAR ADC resolution with no additional analog components. For comparison, Fig. 26 shows two ADC output spectra before and after calibration, on two input frequencies near dc and near the end of the second Nyquist band.

## VII. CONCLUSION

This paper presented a novel architecture to implement hybrid DACs for high-resolution SAR ADCs. The proposed hybrid DAC employs the intrinsic linearity of an I- $\Sigma\Delta$  DAC to linearize the whole SAR ADC. The I- $\Sigma\Delta$  DAC provides both linear steps for SAR LSBs and a startup calibration. The proposed technique benefits from scaled technology nodes, making this high-resolution SAR ADC scaling friendly, from which an outstanding linearity is measured. This is achieved with a unique self-calibration while requiring neither extra circuitry nor extensive layout effort.

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**Ahmad AlMarashli** (S'14) was born in Damascus, Syria, in 1985. He received the B.Sc. degree (with Hons.) in communication engineering from the Higher Institute for Applied Science and Technology (HIAST), Damascus, in 2007, and the M.Sc. degree in communication technologies from the University of Ulm, Ulm, Germany, in 2012, where he is currently pursuing the Ph.D. degree with the Institute of Microelectronics.

He was a Research Assistant with HIAST from 2008 to 2010. His current research interests include analog and mixed-signal IC design with a focus on high-resolution Nyquist data converters.



**Jens Anders** (SM'17) received the master's degree from the University of Michigan, Ann Arbor, MI, USA, in 2005, the Dipl.-Ing. degree from the Leibniz University Hannover, Hannover, Germany, in 2007, and the Ph.D. degree from the École polytechnique fédérale de Lausanne, Lausanne, Switzerland, in 2011.

From 2013 to 2017, he was an Assistant Professor of biomedical integrated sensors with the Institute of Microelectronics, University of Ulm, Ulm, Germany. He is currently a Full Professor and the Director of the Institute of Theory of Electrical Engineering, University of Stuttgart, Stuttgart, Germany. He has authored or co-authored several books and book chapters and approximately 100 journal and conference papers. His current research interests include circuit design for sensing applications, including materials science and biomedical and quantum sensing.

Dr. Anders was a recipient of some nationwide scientific awards in Germany.



**Joachim Becker** (M'04–SM'16) received the Dipl.-Phys. degree in physics from the University of Heidelberg, Heidelberg, Germany, in 2001, and the Dr.-Ing. degree (with Highest Hons.) from the University of Freiburg, Freiburg im Breisgau, Germany, in 2009.

He joined the Department of Microsystems Engineering, University of Freiburg, in 2002, managing a new media teaching program. In 2008, he joined the Department for Microelectronics, University of Ulm, Ulm, Germany, as a Tenured Research Assistant. He has authored or co-authored more than 80 internationally published papers. His current research interests include mixed-signal design and reconfigurable analog circuits.

Mr. Becker was a recipient of the Multimedia Award from the University of Freiburg in 2005 and the Best Poster Award of the IEEE International Conference on Microelectronic Systems Education in 2007, and was the winner of the Cadence Ph.D. Student Design Contest in 2008. He was also a recipient of the Wolfgang-Gentner-Nachwuchsförderpreis for his outstanding doctoral thesis for the promotion of young academics in 2010.



**Maurits Ortmanns** (M'04–SM'11) received the Dr.-Ing. degree in microsystems engineering from the Institut für Mikrosystemtechnik, University of Freiburg, Freiburg im Breisgau, Germany, in 2004.

From 2004 to 2005, he was with Sci-Worx GmbH, Hannover, Germany, where he was involved in the field of mixed-signal circuits for biomedical implants. In 2006, he was an Assistant Professor of integrated interface circuits with the Institute for Microsystems Engineering, University of Freiburg. Since 2008, he has been a Full Professor with the

Faculty of Electrical Engineering and Computer Science, University of Ulm, Ulm, Germany, where he is the Head of the Institute of Microelectronics. He holds several patents. He has authored the book *Continuous-Time Sigma-Delta A/D Conversion* and several other book chapters and more than 200 IEEE journal and conference papers. His current research interests include mixed-signal integrated circuit design, and self-correcting and reconfigurable analog

circuits, with a special emphasis on data converters and biomedical applications.

Prof. Ortmanns was a recipient of the VDI and the VDE Award for his master studies in electrical engineering from Saarland University, Saarbrücken, Germany, in 1999, the ITG Publication Award 2015, the Best Student Paper Awards at MWSCAS 2009 and SampTA 2011, and the Faculty's Teaching Award 2012 and 2015. He was a Program Committee Member of the European Solid State Circuits Conference, the Design Automation and Test Conference, and the European Conference on Circuit Theory and Design, an Associate Editor of the *IEEE TRANSACTIONS OF CIRCUITS AND SYSTEMS I*, a Guest Editor of the *IEEE Journal Solid State Circuits*, and is currently an Associate Editor of the *IEEE TRANSACTIONS OF CIRCUITS AND SYSTEMS II*. He was a Technical Program Committee Member of the IEEE International Solid-State Circuits Conference from 2012 to 2016, an Executive Committee Member of the ISSCC from 2013 to 2016, and the European TPC Chair of the ISSCC from 2015 to 2016.