

# A Reconfigurable Architecture Using a Flexible LO Modulator to Unify High-Sensitivity Signal Reception and Compressed-Sampling Wideband Signal Detection

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**Abstract**—The direct RF-to-information converter unifies high-sensitivity signal reception and compressed-sampling (CS) wideband signal detection into a rapidly reconfigurable and easily scalable architecture occupying 0.56 mm<sup>2</sup> in 65-nm CMOS. In reception mode, the DRF2IC RF frontend consumes 46.5 mW from 1.15 V and delivers 40-MHz RF bandwidth, 41.5-dB conversion gain, 3.6-dB noise figure, and –2 dBm B1dB. In CS wideband detection mode, 66-dB operational dynamic range, 40-dB instantaneous dynamic range, and 1.43-GHz instantaneous bandwidth are demonstrated, and six interferers each 10 MHz wide scattered over a 1.27-GHz span are detected in 1.2  $\mu$ s consuming 58.5 mW.

**Index Terms**—Analog-to-information converter, cognitive radio (CR), compressed sampling (CS), dynamic spectrum access, frequency-translational noise-cancelling (FTNC) receiver.

## I. INTRODUCTION

SOON billions of new devices ranging from personal health monitoring devices to smart cars and unmanned aerial vehicles will compete with mobile phones for access to an increasingly congested electromagnetic spectrum. The current paradigm of pre-allocating spectrum for use by designated classes of devices will no longer be sufficient to guarantee access to all. Advances in cognitive radio (CR) [1]-based dynamic shared spectrum access (DSSA) systems will force us to rethink the radio transceiver. In many scenarios, a static radio link will be replaced by, or supplemented with, multiple short dynamic links. Future CR terminals will rapidly gain awareness of their fast changing spectrum environment and

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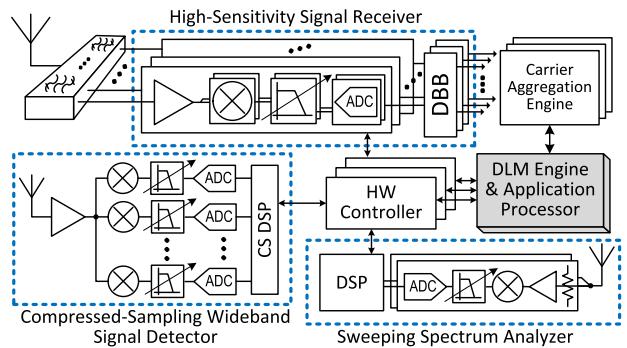


Fig. 1. Conceptual illustration of a spectrum-aware CR receiver frontend suitable for dynamic spectrum access.

opportunistically access a shared pool of spectrum spanning, e.g., 600 MHz–6 GHz.

Spectrum sensing [2] is a key component of CR. A spectrum-aware CR receiver (CR-RX) for DSSA [3] shown in Fig. 1 will include a sweeping spectrum analyzer, a wideband signal detector, a dynamic link management (DLM) engine, and a high-sensitivity signal receiver. The DLM engine will use information from the sweeping spectrum analyzer and the wideband signal detector to reconfigure the signal receiver in order to opportunistically access the shared pool of spectral bands. Sweeping spectrum analyzers are a key to detecting weak incumbents or finding gaps in the crowded spectrum. Compressed-sampling (CS) architectures have the potential to enable energy-efficient, rapid, wideband signal detection.

The direct RF-to-information converter (DRF2IC) [4] is a flexible architecture that unifies the three critical functions of a CR-RX highlighted in Fig. 1. While CS signal detectors [5]–[12], sweeping spectrum analyzers [13]–[18], and high-sensitivity signal receivers [19]–[24] have been demonstrated on chip, these functions are currently implemented in distinct hardware blocks. Going forward, functionally flexible and rapidly reconfigurable architectures compactly implemented on silicon will be needed to achieve the cost, size, and power targets in mass-market applications. This new generation of multi-function CR-RX architectures will need to quickly switch between their reception and detection modes

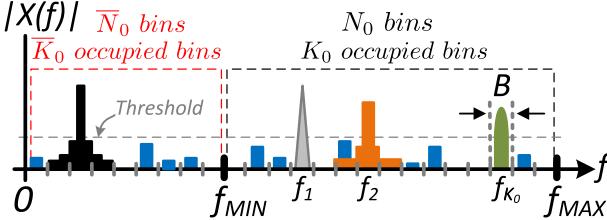


Fig. 2. Spectrum of a signal with frequency components above a threshold occupying only  $K_0$  of the total  $N_0$  bins in  $\mathcal{F}_0 = [f_{\text{MIN}}, f_{\text{MAX}}]$  and  $\overline{K}_0$  of the total  $\overline{N}_0$  bins in  $\overline{\mathcal{F}}_0 = (0, f_{\text{MIN}})$ .

as required by the deployment scenario. Building upon the direct-conversion RF chain, typically preferred for signal reception, and combining it with a flexible local oscillator (LO) modulator and CS signal processing, the DRF2IC [4] comprehensively presented here unifies high-sensitivity reception, swept narrowband detection, and CS wideband detection into a single, compact, reconfigurable architecture.

This paper is organized as follows. Section II describes the goal of this paper. Evolution of the CS RF frontend (RFFE) and a brief introduction to the essentials of CS theory are provided in Section III-A. The DRF2IC concept is introduced in Section III-B, and its operation is analyzed in Section IV. The DRF2IC architecture and key circuit blocks are described in Section V. Measurement results, comparison to the state of the art (SoA), and conclusions are in Sections VI–VIII.

## II. PROBLEM FORMULATION

To motivate this paper, LTE licensed-assisted access (LAA) [25] is considered as a usecase of DSSA, where time division duplex (TDD) mode LTE terminals form an anchor link in a licensed band and opportunistically form additional links in an unlicensed band. An important feature of LTE-LAA ensuring fair coexistence with Wi-Fi terminals is a listen-before-talk mechanism [25], where the LTE terminals perform energy-detection-based clear channel assessment (CCA) before opportunistically transmitting on unused channels in the unlicensed band. A possible channel access mechanism for LTE-LAA can include a two-step sensing procedure: 1) rapidly detecting the location of strong signal components within the unlicensed band to construct a channel exclusion list and 2) performing CCA for a specified minimum amount of time on a set of candidate channels outside of the exclusion list to check for weak Wi-Fi incumbents.

Fig. 2 shows a snapshot of the dynamic spectrum environment that the LTE-LAA terminal may have to operate in. We use a real-valued signal  $x(t)$  to model the spectrum, where the Fourier transform  $X(f)$  of the signal vanishes outside of some known frequency ranges  $\mathcal{F} = (0, f_{\text{MAX}}]$ . We assume that  $\mathcal{F}$  is partitioned into  $N$  bins, where  $N = f_{\text{MAX}}/B$  and each bin is of width  $B$  Hz. Up to  $K$  of these bins, where  $K \ll N$  are occupied by components of  $X(f)$  with a bandwidth of at most  $B$  Hz and with power that exceeds a predefined threshold.

We note that the spectrum of the signal  $x(t)$  is sparse when considering frequency components above this threshold as shown in Fig. 2. We further assume that

of the  $N$  total bins in  $\mathcal{F}$ ,  $N_0$  bins are contained in  $\mathcal{F}_0 = [f_{\text{MIN}}, f_{\text{MAX}}]$  and  $\overline{N}_0$  bins are contained in  $\overline{\mathcal{F}}_0 = (0, f_{\text{MIN}})$ . The frequency components of the signal that exceed a predefined threshold in  $\mathcal{F}_0$  are assumed to occupy only  $K_0$  bins, where  $K_0 \ll N_0 < N$ .

An LAA deployment example is considered where the unlicensed band  $\mathcal{F}_0$  includes  $N_0 = 50$  channels of width  $B = 20$  MHz.<sup>1</sup> To further motivate this paper, a future 5G deployment is considered where TDD-LTE is performed in dense small-cell environments with a heterogenous mix of multiple (e.g., 20 or more) terminals, relays, and access points. The TDD subframe duration is assumed to be  $300 \mu\text{s}$  with a roughly 17% (50 us) overhead for control signaling [26]. This extremely short-duration subframe is designed to enable fast link-direction switching in order to achieve the 1-ms round-trip latency goal of 5G. Adding an additional  $25 \mu\text{s}$  for the above-proposed two-step sensing procedure for LTE-LAA leads to a TDD subframe with a reasonable 25% overhead.

The spectral mask around large signal components in  $\mathcal{F}_0$  with received power greater than, e.g.,  $-20$  dBm, is considered when constructing a channel exclusion list.<sup>2</sup> It is assumed that six adjacent channels (three on each side of the carrier) surrounding each of the  $K_0$  large signals located at carrier frequencies  $f_1, f_2 \dots f_{K_0}$ , as shown in Fig. 2 are unusable for transmission, as the leakage into these adjacent channels may exceed the required CCA energy detection threshold of  $-82$  dBm [25]. Assuming  $K_0 = 6$ , the exclusion list consists of 42 channels. We are thus left with eight usable candidate channels out of the  $N_0 = 50$  total channels in  $\mathcal{F}_0$ . The LTE-LAA terminal now must randomly select a channel from the candidate list and perform high-sensitivity energy detection for a CCA duration of  $9 \mu\text{s}$  [25]. If the chosen channel contains energy above the CCA threshold, the LTE-LAA terminal must randomly select a different channel on the candidate list. Assuming that at least two CCA trials are needed to find a suitable channel in the candidate list, we are left with  $7 \mu\text{s}$  for the wideband detection of  $K_0$  large signals in  $\mathcal{F}_0$ .

In addition to developing a reconfigurable architecture that unifies high-sensitivity reception, swept narrowband detection, and CS wideband detection, the CS detection specific goal of this paper is to: 1) efficiently find the location of the  $K_0$  frequency components in the wanted, e.g., unlicensed band  $\mathcal{F}_0$  while; 2) reduce the impact of noise and  $\overline{K}_0$  signal components in the unwanted band  $\overline{\mathcal{F}}_0$ ; and 3) achieve a wideband detection time in the order of  $1 \mu\text{s}$  to further reduce the TDD-LTE subframe overhead or to accommodate additional CCA steps while maintaining a reasonable overhead.

## III. DIRECT RF-TO-INFORMATION CONVERTER ARCHITECTURE DEVELOPMENT

The key challenge in developing circuit architectures to implement CS RF or analog-to-information converters is gen-

<sup>1</sup>The U.S. President's Council of Advisors on Science and Technology in 2012 recommended sharing government spectrum ranging from 2.7 to 3.7 GHz with non-governmental entities. It is anticipated that various CR-DSSA systems will be deployed in this spectrum.

<sup>2</sup>The LTE-LAA receiver's blocker 1-dB compression point or a blocker noise figure [19] performance in the unlicensed band may also be considered when constructing the channel exclusion list.

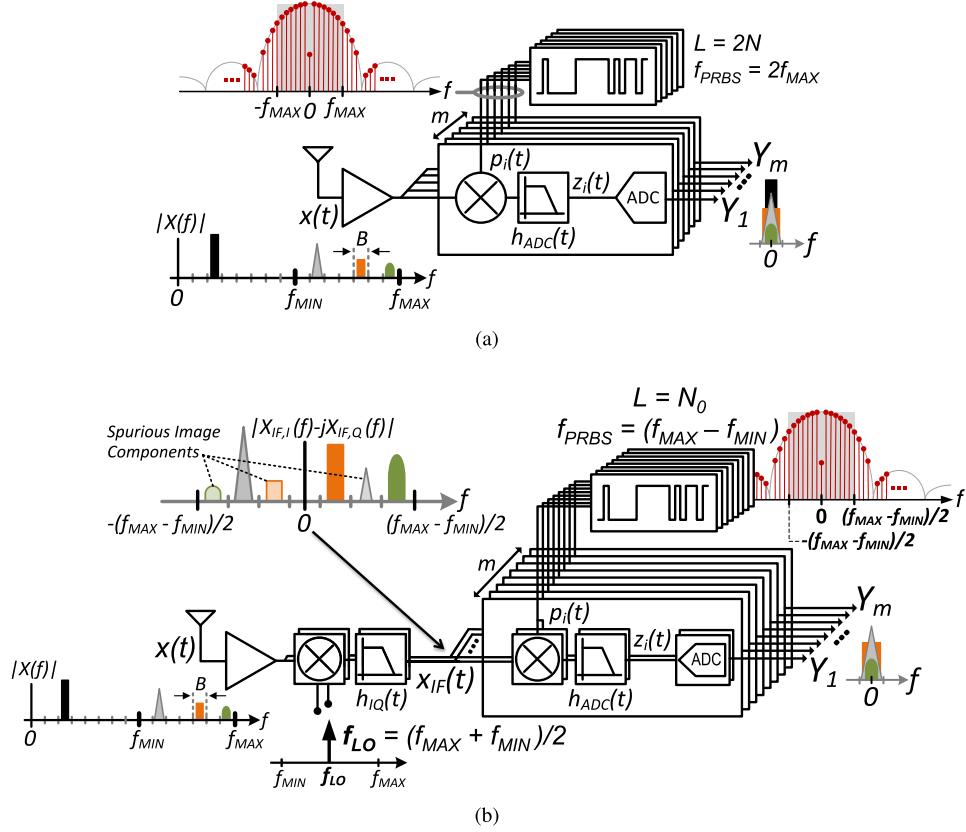


Fig. 3. Existing CS RFFE used for rapid detection of sparse wideband signals. (a) MWC [5]–[7]. (b) QAIC [8]–[10].

erating a sufficient number of independent measurements in the RF or analog domain. In this section, we first briefly review existing CS wideband detection solutions. The modulated wideband converter (MWC) and the quadrature analog-to-information converter (QAIC) are discussed. Both architectures use multi-branch RFFEs.

We highlight that while the MWC has several beneficial properties, its maximum frequency is limited by the clock frequency of its periodic pseudo-random bit sequence (PRBS) generators and it is susceptible to noise and large signal components in  $\mathcal{F}_0$  when configured to detect signals in  $\mathcal{F}_0$ . The QAIC addresses this by performing wideband quadrature downconversion ahead of analog mixing with PRBSs at IF. However, the dual heterodyne architecture of the QAIC suffers from spurious responses at IF caused by IQ imbalance in its wideband downconverter. We then show how the DRF2IC compactly adds wideband detection to a direct-conversion frequency-translational noise-cancelling (FTNC) receiver by introducing pseudo-random LO modulation consolidating multiple CS measurements into one hardware branch to overcome the limitations of both the MWC and the QAIC.

#### A. Existing Compressed-Sampling RF Frontends for Wideband Sensing

In a stationary spectrum environment, a traditional sweeping spectrum analyzer may be used to sequentially examine all  $N$  bins in Fig. 2, one at a time, to find the location of the  $K$  large signal components. However, sweeping spectrum analyzers

suffer from a tradeoff between resolution bandwidth and scan time, which makes them unsuitable for searching a large number of channels over a wide frequency range in a short period of time in a rapidly changing spectrum environment [8]. Results from CS theory [27]–[30] show that if the spectrum of a signal is *sparse* (i.e.,  $K \ll N$ ), it is possible to detect the location of the  $K$  occupied bins in  $\mathcal{F}$  with only  $R$ , where  $K < R \ll N$ , independent linear measurements. This can be done with high detection probability ( $P_D$ ) employing  $\Lambda \approx K \cdot R \cdot N$  multiplications in CS DSP using the orthogonal matching pursuit (OMP) algorithm [31], [32] even if the locations of these  $K$  bins are changing rapidly and are not known in advance. Furthermore, in contrast with Nyquist rate approaches employing a single branch with a high sampling rate analog-to-digital converter (ADC) or multiple branches with lower rate ADCs, hardware branches producing each CS measurement need only an ADC sampling frequency  $f_{ADC} \approx B$  Hz, thereby ensuring that the aggregate sampling rate  $R \cdot B$  Hz is proportional to the information bandwidth  $K \cdot B$  Hz and is much smaller than the Nyquist bandwidth  $f_{NYQ} = 2f_{MAX} = 2N \cdot B$  Hz.

*1) Modulated Wideband Converter:* The MWC [5]–[7] shown in Fig. 3(a) mixes its input signal  $x(t)$  at RF with PRBSs  $p_i(t)$  of length  $L = 2N$  and low-pass filters the mixer outputs to produce  $z_i(t)$ , which are then sampled at a low rate ( $f_{ADC} \approx B$ ) to produce CS measurements  $Y_i$ . Nominally, each of the  $m$  branches in the MWC RFFE produces only one measurement, and therefore,  $m = R$  branches driven by

TABLE I

MWC, QAIC, AND DRF2IC SYSTEM PARAMETERS.  $C_M, C_Q > 1$  ARE IMPLEMENTATION-DEPENDENT CONSTANTS

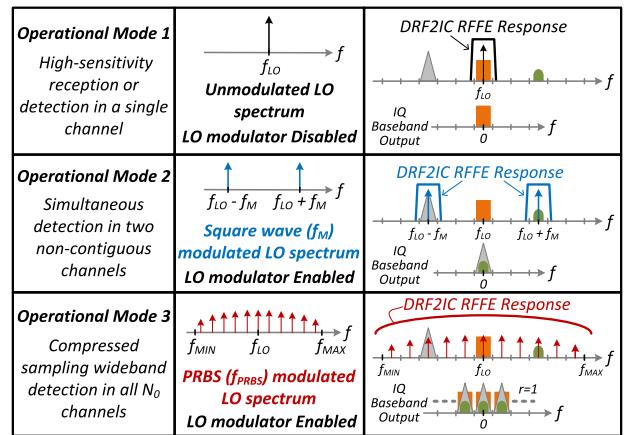
|             | <b>MWC</b>          | <b>QAIC</b>                       | <b>DRF2IC</b>                     |
|-------------|---------------------|-----------------------------------|-----------------------------------|
| $z_i(t)$    | $x(t)p_i(t)$        | $\{x(t)e^{j\omega_{LO}t}\}p_i(t)$ | $x(t)\{e^{j\omega_{LO}t}p_i(t)\}$ |
| $f_{LO}$    | -                   | $(f_{MAX} + f_{MIN})/2$           |                                   |
| <i>Span</i> | $[0, f_{MAX}]$      | $[f_{MIN}, f_{MAX}]$              |                                   |
| $L$         | $[2f_{MAX}/B]$      | $[(f_{MAX} - f_{MIN})/B]$         |                                   |
| $f_{PRBS}$  | $2f_{MAX}$          | $(f_{MAX} - f_{MIN})$             |                                   |
| $R$         | $[C_M K \log(N/K)]$ | $[C_Q K_0 \log(N_0/K_0)]$         |                                   |

$R$  unique PRBSs  $p_i(t)$  with low cross correlation are needed. The number of multiplications needed in the OMP when used with the MWC is  $\Lambda = 4K \cdot R \cdot N$  [7]. The MWC system parameters are listed in Table I. While the energy consumed by the MWC can be significantly lower than a traditional sweeping spectrum analyzer when searching a large number of channels over a wide frequency range, its RFFE architecture does not scale well to higher frequencies [6], as the required PRBS clock frequency  $f_{PRBS} \geq 2f_{MAX}$  scales up with the maximum frequency of interest  $f_{MAX}$ . Furthermore, since the PRBSs have frequency content spanning from dc to  $f_{MAX}$ , spectral information from  $\bar{\mathcal{F}}_0$  and  $\mathcal{F}_0$  is mixed down, filtered, and sampled by the ADCs. Given that we are only interested in detecting signal components in  $\mathcal{F}_0$ , the MWC unnecessarily adds noise to measurements  $Y_i$  from  $\bar{\mathcal{F}}_0$  and suffers from undesired blocking effects in the RFFE when strong unwanted signal components are present in  $\bar{\mathcal{F}}_0$ .

2) *Quadrature Analog-to-Information Converter:* The QAIC [8]–[10] shown in Fig. 3(b) employs frequency downconversion in order to restrict RF bandwidth before performing analog mixing with PRBSs at IF. This enables the QAIC to efficiently detect the  $K_0$  signal components in  $\mathcal{F}_0$  while reducing the impact of noise and unwanted signal components in  $\bar{\mathcal{F}}_0$ . The resulting complex signal  $x_{IF}(t)$  at IF is then mixed with PRBSs  $p_i(t)$  of length  $L = N_0 < N$  and low-pass filtered to produce IQ analog output pairs  $z_i(t)$ , which are then sampled at  $f_{ADC} \approx B$  to produce complex measurements  $Y_i$ . The number of multiplications needed in the QAIC-OMP is  $\Lambda = K_0 \cdot R \cdot N_0$  [8]. In [9],  $m = R$  branches (see Table I) are required, since each IF branch produces only one measurement. The QAIC RFFE scales well to higher frequencies, since it uncouples the PRBS clock frequency  $f_{PRBS}$  from  $f_{MAX}$ . Specifically,  $f_{PRBS} \geq (f_{MAX} - f_{MIN})$  is required [8]. In scenarios where  $f_{MIN} \gg 0$ , the energy efficiency and the sensitivity performance of the QAIC are significantly improved compared with the MWC when detecting signal components in  $\mathcal{F}_0$  [8].

However, the wideband IQ downconverter used in the QAIC RFFE suffers from frequency-independent IQ imbalance caused primarily by non-idealities in the quadrature LO generator as well as frequency-dependent IQ gain and phase imbalance caused by mismatches in the wideband frequency responses of analog components at IF [8]. This limits the instantaneous dynamic range (IDR) of the QAIC due to the presence of spurious signal components at wideband IF caused by the finite suppression of the image frequencies  $[-f_{MAX}, -f_{MIN}]$ , as shown in Fig. 3(b). Low-complexity

TABLE II  
CONVERSION GAIN PROFILES OF THE DRF2IC RFFE



digital methods for frequency-independent IQ imbalance compensation have been demonstrated [33]. While methods for compensating frequency-dependent IQ imbalance have also been demonstrated [34], this type of imbalance caused primarily by mismatches in the wideband IF transimpedance amplifier (TIA) responses may no longer be accurately corrected at digital baseband (DBB), since mixing with a PRBS folds the wideband IF spectrum of width  $N_0 B$  Hz onto a single channel of width  $B$  Hz at baseband.

### B. Using a Modulated LO to Transform an FTNC into the DRF2IC

The proposed DRF2IC [4] RFFE employing an FTNC receiver [19]–[22] with two direct-conversion IQ branch pairs, a flexible LO generator, and a DBB circuitry is shown in Fig. 4. In mode 1, the DRF2IC performs signal reception or detection in a single channel using a standard quadrature LO at  $f_{LO}$  to generate a single RF conversion gain response around  $f_{LO}$ , as shown in Table II. In mode 2, an LO at  $f_{LO}$  is modulated with a square wave at  $f_M$ . The resulting LO now consists of two tones at  $(f_{LO} - f_M)$  and  $(f_{LO} + f_M)$ . This, then, generates two RF responses around the two LO tones enabling simultaneous detection of two non-contiguous channels.

For CS wideband detection in mode 3, an LO at  $f_{LO}$  is modulated with a PRBS of length  $N_0$  and clock frequency  $f_{PRBS}$ , thereby upconverting to  $f_{LO}$  the Fourier line spectra of the PRBS [35] centered at dc. The resulting LO spectrum thus consists of a series of tones centered at  $f_{LO}$  and spaced by the desired resolution bandwidth  $B = f_{PRBS}/N_0$ . This PRBS modulated LO is then used to drive the passive mixers in the FTNC, thereby upconverting the baseband low-pass filter response to multiple RF frequencies separated by  $B$  to create a very wide *bandpass RF response* with a 3-dB bandwidth extending from  $f_{MIN} = (f_{LO} - f_{PRBS}/2)$  to  $f_{MAX} = (f_{LO} + f_{PRBS}/2)$ . The IQ analog output pairs  $z_i(t)$  contain all  $N_0$  bins of width  $B$  from  $\mathcal{F}_0$ . These bins are folded into  $(2r+1)$ , where  $r = 0, 1, 2, \dots$  complex IF frequencies separated by  $B$ , as shown in Fig. 5.

Multiple CS measurements may be extracted from a single analog branch at the cost of increased sampling rate per branch

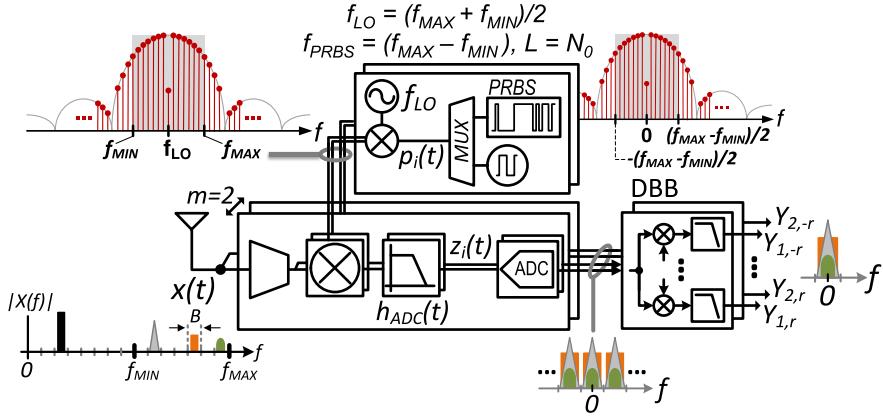


Fig. 4. Using a modulated LO to transform an FTNC into the proposed DRF2IC.

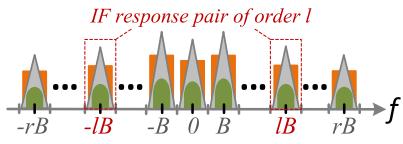


Fig. 5. Higher order IF responses in the DRF2IC RFFE analog IQ outputs resulting from mixing with PRBS-modulated LOs.

and added DSP complexity [7]. This is an important degree of freedom that we exploit to generate a sufficient number of CS measurements from the  $m = 2$  IQ branch pairs in an FTNC receiver in order to rapidly detect up to  $K_0 = 6$  signal components. Each of the IQ analog outputs is multiplied by  $2r$  orthogonal complex exponentials of frequencies that are integer multiples of  $B$  in the DBB to extract  $2r$  higher order IF responses in addition to the response at dc. Thus, the total number of measurements  $Y_i$ , produced by the DRF2IC RFFE is  $R = m(2r + 1)$ . The number of multiplications needed in the DRF2IC-OMP is  $\Lambda = K_0 \cdot R \cdot N_0$ . The CS detection mode parameters of the DRF2IC are listed in Table I.

The DRF2IC inherits the benefits of the FTNC receiver [19]–[22] in signal reception mode. In CS wideband detection mode, the DRF2IC inherits key advantages from both the MWC and the QAIC while avoiding the drawbacks of each architecture. It uncouples the PRBS clock frequency  $f_{PRBS}$  from  $f_{MAX}$  in contrast with the MWC. In contrast with the QAIC, the DRF2IC uses a direct-conversion RF chain with narrow bandwidth IQ analog components at baseband, thereby avoiding frequency-dependent IQ imbalance and extracts multiple measurements from each analog IQ branch pair. While the DRF2IC does suffer from finite suppression of image frequencies extending from  $-f_{MAX}$  to  $-f_{MIN}$  caused primarily by quadrature errors in its LO generator, this type of frequency-independent IQ imbalance may be compensated using low-complexity methods [33] at DBB (see Sections V-C and VI).

#### IV. ANALYSIS OF THE DRF2IC OPERATION

Consider an in-phase branch of the DRF2IC RFFE consisting of a low-noise transconductance amplifier (LNTA), a passive mixer, and a TIA, as shown in Fig. 6. The

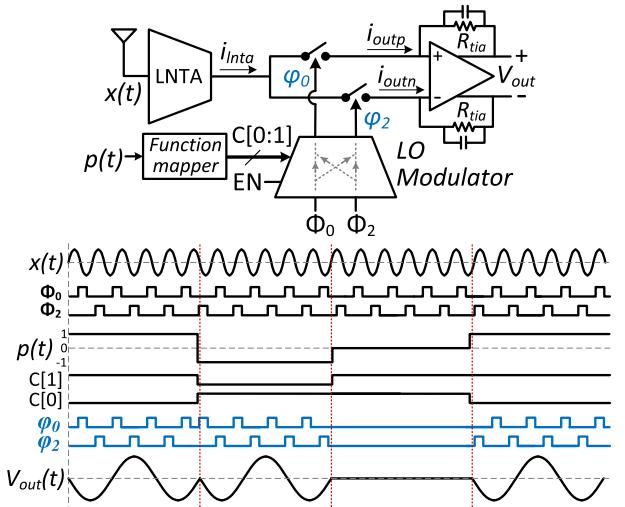


Fig. 6. Modeling the use of a modulated LO to simultaneously downconvert and multiply the input signal  $x(t)$  with a piecewise constant function  $p(t)$ .

RF output current  $i_{Inta}$  of the LNTA is downconverted by the passive mixer consisting of two switches that are driven by two non-overlapping clocks  $\phi_0$  and  $\phi_2$ . Assuming ideal switches, the mixer output currents  $i_{outp}$  and  $i_{outn}$  are equal to  $i_{Inta}$  multiplied by the associated clock pulses  $\phi_0$  and  $\phi_2$ , which are modeled as piecewise constant functions alternating between 0 and 1. The TIA differential output voltage is  $V_{out} = x(t)G_m(\phi_0 - \phi_2)(R_{tia}/C) = x(t)G_m(R_{tia}/C) \sum_{n=-\infty}^{\infty} (\alpha_{0,n} - \alpha_{2,n})e^{j2\pi n f_{LO} t}$ , where  $\alpha_{0,n}$  and  $\alpha_{2,n}$  are the Fourier coefficients and  $f_{LO}$  is the frequency of the clock pulses  $\phi_0$  and  $\phi_2$ .

When disabled ( $EN = 0$ ), the LO modulator passes the standard in-phase 25% duty-cycle input LO pair  $(\Phi_0, \Phi_2)$  to its output  $(\phi_0, \phi_2)$ . When enabled ( $EN = 1$ ), the LO modulator operation is described by

$$(\phi_0, \phi_2) = \begin{cases} (\Phi_0, \Phi_2) & \text{when } C[1:0] = (1, 0) \\ (\Phi_2, \Phi_0) & \text{when } C[1:0] = (0, 1) \\ (0, 0) & \text{when } C[1:0] = (1, 1) \end{cases} \quad (1)$$

where the control signal pair  $C[1:0]$  is used to define the transfer function of the LO modulator. The LO modulator

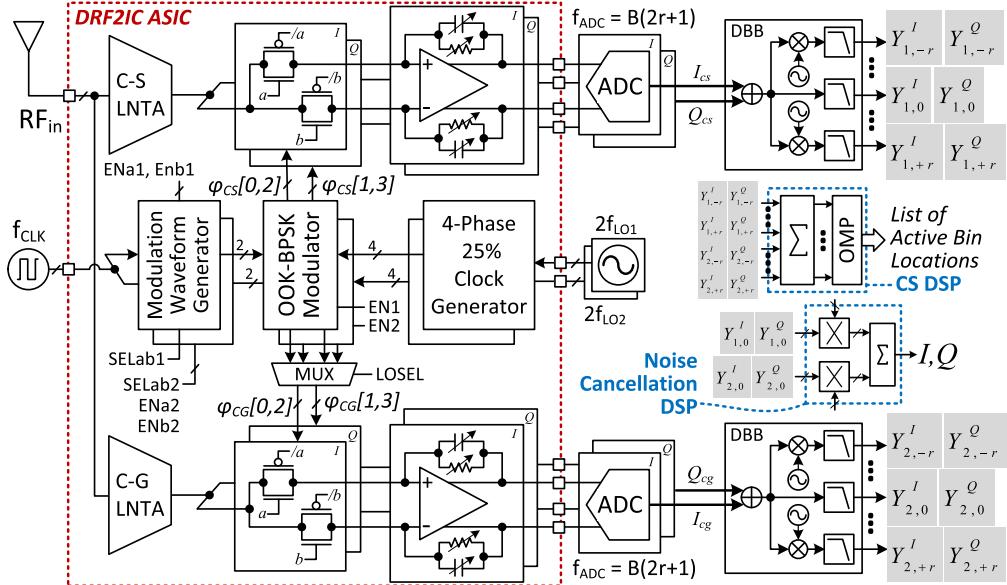


Fig. 7. DRF2IC system architecture. Unifying data reception and rapid wideband signal detection into a single reconfigurable architecture using the FTNC, a flexible LO modulator, and CS DSP.

either maintains or flips the polarity of its differential output pair ( $\phi_0, \phi_2$ ) relative to its input ( $\Phi_0, \Phi_2$ ) when its control signals C[1] and C[0] are the complements of each other. When C[1] = C[0] = 1, both outputs of the LO modulator are held at logic level 0. The Fourier coefficients of the TIA differential output voltage  $V_{\text{out}}$  are

$$\alpha_n = \begin{cases} (\beta_{0,n} - \beta_{2,n}) & \text{when } C[1:0] = (1, 0) \\ (\beta_{2,n} - \beta_{0,n}) & \text{when } C[1:0] = (0, 1) \\ 0 & \text{when } C[1:0] = (1, 1) \end{cases} \quad (2)$$

where  $\alpha_n = (\alpha_{0,n} - \alpha_{2,n})$ . Noting that the Fourier coefficients of the clock pulses  $\Phi_0$  and  $\Phi_2$  are  $\beta_{0,n} = (1/4)(\sin(n\pi/4)/(n\pi/4))e^{-jn\pi/4}$  and  $\beta_{2,n} = \beta_{0,n}e^{-jn\pi}$ , the Fourier coefficients of the TIA differential output voltage  $V_{\text{out}}$  may now be expressed as

$$\alpha_n = \begin{cases} \frac{1}{4}(1-e^{-jn\pi})\frac{\sin(n\pi/4)}{n\pi/4}e^{-jn\pi/4} & \text{when } C[1:0] = (1, 0) \\ \frac{1}{4}(e^{-jn\pi}-1)\frac{\sin(n\pi/4)}{n\pi/4}e^{-jn\pi/4} & \text{when } C[1:0] = (0, 1) \\ 0 & \text{when } C[1:0] = (1, 1) \end{cases} \quad (3)$$

where only the odd coefficients of  $\alpha_n$  are non-zero when C[0] and C[1] are the complements of each other. Since the TIA has a low-pass response, we are only interested in the low-frequency components of the mixer output. Setting  $n = -1, 1$  and the input signal  $x(t) = \cos[(\omega_{\text{LO}} + \Delta\omega)t]$  with  $\Delta\omega \ll \omega_{\text{LO}}$ , the TIA output voltage is

$$V_{\text{out}} = \begin{cases} \mathcal{K} \cos(\Delta\omega t + \pi/4) & \text{when } C[1:0] = (1, 0) \\ -\mathcal{K} \cos(\Delta\omega t + \pi/4) & \text{when } C[1:0] = (0, 1) \\ 0 & \text{when } C[1:0] = (1, 1) \end{cases} \quad (4)$$

where  $\mathcal{K} = \sqrt{2}G_m R_{\text{tia}}/\pi$ . When the LO modulator is enabled and a piecewise constant function  $p(t)$  with three discrete values  $\{1, -1, 0\}$  is mapped to the control signal pair C[1:0] using

$$C[1:0] = \begin{cases} (1, 0) & \text{when } p(t) = 1 \\ (0, 1) & \text{when } p(t) = -1 \\ (1, 1) & \text{when } p(t) = 0 \end{cases} \quad (5)$$

the output of the DRF2IC in-phase branch in Fig. 6 may be described compactly as  $V_{\text{out}} = \tilde{\mathcal{K}}\{p(t) \cos(\omega_{\text{LO}}t)\}x(t)$ , where  $\tilde{\mathcal{K}} = 2\sqrt{2}G_m R_{\text{tia}}/\pi$ . The DRF2IC can therefore simultaneously downconvert and multiply an input signal  $x(t)$  with a two- or three-level piecewise constant function  $p(t)$ .

## V. DRF2IC SYSTEM IMPLEMENTATION

### A. System Architecture and Configuration Options

In mode 1, the DRF2IC system in Fig. 7 employs the RFFE common-source (C-S) and common-gate (C-G) LNTA paths with the noise cancellation DSP to form an FTNC receiver [19]–[21]. Both the C-S and C-G path mixers are driven with the same 25% duty-cycle, four-phase LO by setting LOSEL to 0, and both LO modulators are disabled by setting EN1 and EN2 to 0, as shown in Table III. When receiving a single channel, only the middle branches  $Y_{1,0}^I$  and  $Y_{1,0}^Q$  and  $Y_{2,0}^I$  and  $Y_{2,0}^Q$  of the C-S and C-G path DBB blocks are used. While not demonstrated in this paper, we note that multiple adjacent channels may be received by increasing the TIA bandwidth and ADC sampling rate and enabling vector modulators in the DBB.

In mode 2, only one LO modulator is enabled (EN1 = 1 and EN2 = 0), and the modulation waveform generator is set to generate a square wave (SELab1 = 0, ENa1 = 0, and ENb1 = 1). Both the C-S and C-G path mixers are driven

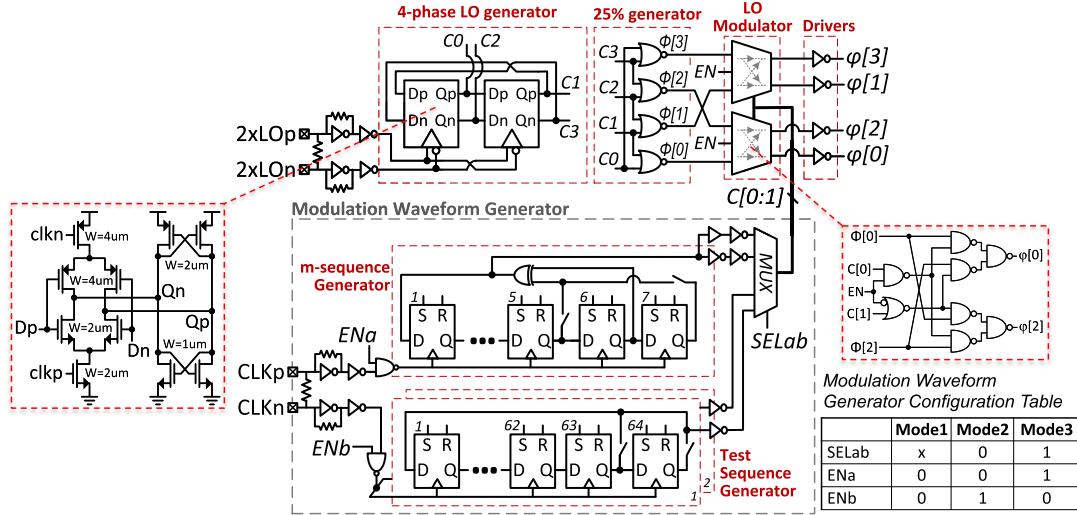


Fig. 8. Block diagram and configuration options of the modulated LO generator consisting of a 25% duty-cycle, four-phase clock generator, an LO modulator, and a programmable modulation waveform generator. The waveform generator includes an m-sequence generator and a test sequence generator.

TABLE III  
DRF2IC RFFE CONFIGURATION OPTIONS AND THE  
ASSOCIATED CONTROL SIGNAL SETTINGS

|         | LOSEL | EN1 | EN2 | SELab1 | EN12 | SELab2 | EN22 | Modulation Waveform | CS LO | CG LO                                      |
|---------|-------|-----|-----|--------|------|--------|------|---------------------|-------|--|
| Mode 1  | 0     | 0   | 0   | x      | 0    | 0      | x    | 0                   | 0     | -  |
| Mode 2  | 0     | 1   | 0   | 0      | 0    | 1      | x    | 0                   | 0     | Single Tone                                |
| Mode 3a | 1     | 1   | 1   | 1      | 1    | 0      | 1    | 1                   | 0     | $P_1(t)\exp(jw_{lo1})$                     |
| Mode 3b | 1     | 1   | 1   | 1      | 1    | 0      | 1    | 1                   | 0     | $P_1(t)\exp(jw_{lo1})P_2(t)\exp(jw_{lo2})$ |

with the same ( $\text{LOSEL} = 0$ ) square-wave modulated LO to implement simultaneous detection in two non-contiguous channels with noise cancellation.

In CS mode 3, both LO modulators are enabled ( $\text{EN1} = 1$  and  $\text{EN2} = 1$ ), and the waveform generators are configured to generate independent PRBSs by setting  $\text{SELab1} = 1$ ,  $\text{ENa1} = 1$ , and  $\text{ENb1} = 0$ , and  $\text{SELab2} = 1$ ,  $\text{ENa2} = 1$ , and  $\text{ENb2} = 0$ . The C-S and C-G path mixers are now driven with two independent sets of LOs ( $\text{LOSEL} = 1$ ) modulated with two distinct PRBSs. Using CS DSP, the DRF2IC performs wideband signal detection in a single band (*mode 3a*) by setting  $f_{\text{LO1}} = f_{\text{LO2}}$  in Fig. 7 or in two disjoint bands (*mode 3b*) using distinct LOs, where  $f_{\text{LO1}} \neq f_{\text{LO2}}$ .

### B. RFFE Chip Implementation

The modulated LO generator shown in Fig. 8 consists of a 25% duty-cycle, four-phase LO generator, an ON-OFF-keyed (OOK) BPSK LO modulator, LO drivers, and a modulation waveform generator. The 25% duty-cycle, four-phase LO generator and LO drivers together consume 7 mW from 1.15 V at 2.21 GHz. The modulation waveform generator consists of two function generators: 1) a maximal-length pseudo-random sequence (m-sequence) generator [35] and 2) a user definable test sequence generator. The test sequence generator consists of a pair of series connected, programmable length flip-flop arrays with feedback. User-defined test sequences are loaded into the two independent flip-flop arrays through a serial

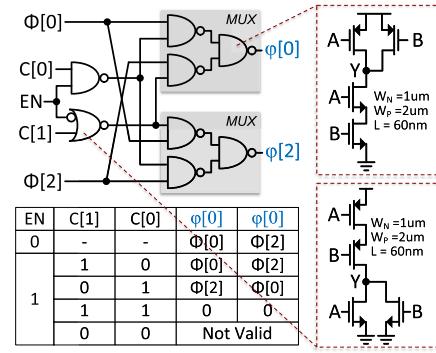


Fig. 9. Schematic and truth table of the OOK-BPSK LO modulator core consisting of two custom high-speed NAND logic-based multiplexers and control logic.

peripheral interface (SPI). The two flip-flop arrays are loaded with independent logic sequences in order to represent a three-level (+1, 0, -1) test sequence as defined in (5). A two-level ( $\pm 1$ ) test sequence may be formed by loading the true and complemented versions of a logic sequence into the two flip-flop arrays. The m-sequence generator employs a linear feedback shift register architecture consuming 1.7 mW at a clock frequency of 1.27 GHz. Its length may be set to 63 or 127. The 2-bit output ( $C[1:0]$ ) of the modulation waveform generator controls the LO modulator functionality, and either the m-sequence or the test sequence may be passed to its output through the multiplexer.

The LO modulator in Fig. 8 consists of two modulator cores. Each OOK-BPSK modulator core shown in Fig. 9 uses two custom designed high-speed NAND logic-based multiplexers and control logic. The modulator core has three valid output states. When  $\text{EN} = 0$ , the core passes the input LO signal to its output unaltered. When  $\text{EN} = 1$ , the core either maintains or flips the polarity of its output pair relative to its input when the logic values of the control signals  $C[0]$  and  $C[1]$  are the complements of each other. When  $C[1] = C[0] = 1$ , both outputs of the core are set to 0. Each core consumes 720  $\mu$ W from 1.15 V when the input LO signal frequency is

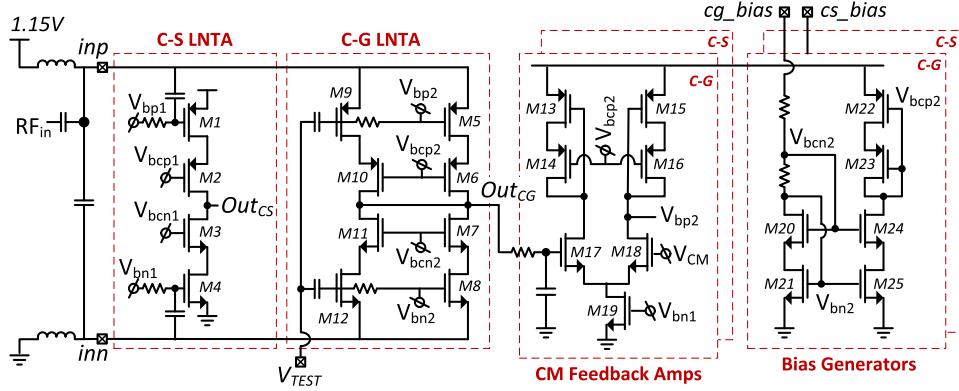


Fig. 10. C-S and C-G LNTA combination with bias and common-mode feedback circuitry. A portion of the C-G LNTA (transistors M9–M12) is used to calibrate the RFFE in noise cancelling reception mode.

2.54 GHz and a control signal pair C[1:0] switching frequency is 1.27 GHz.

The C-S and C-G LNTA combination with bias and common-mode feedback circuitry is shown in Fig. 10. The cascoded inverter is used as the core circuit block in both LNTAs, and the bias current of each core may be set externally. An input return loss of  $-12$  dB or better from 600 MHz to 3 GHz is achieved by setting the C-G LNTA transconductance to 30 mS. The C-S LNTA delivers 113 mS of transconductance gain, and the pair together consumes 15.5 mA from 1.15 V. In noise cancelling reception mode, a portion of the C-G LNTA core, transistors M9–M12, is used for system calibration. During calibration, the input (RF<sub>in</sub> in Fig. 10) is  $50\ \Omega$  terminated, and a continuous wave (CW) test signal is applied to the test input pin  $V_{TEST}$ . The test signal couples into the C-S LNTA path and stimulates a signal in the C-S path IQ output. A complex sum of the C-S and C-G IQ outputs is formed, and the gain of the two paths are co-optimized to minimize this sum, thereby achieving optimal noise cancellation. Once the system is calibrated, the test input  $V_{TEST}$  is grounded through a capacitor.

The passive mixer, the TIA, and the TIA operational transconductance amplifier (OTA) schematics are shown in Fig. 11. The passive mixers use transmission gates, and the TIAs are implemented with two-stage Miller-compensated OTAs. The TIAs use 4-bit programmable feedback resistors and 3-bit programmable feedback capacitors for gain and baseband bandwidth range control. The four TIAs together consume 24 mW from 1.15 V.

The DRF2IC RFFE chip shown in Fig. 12, including SPI circuitry and power supply bypass capacitors, was implemented in 65-nm CMOS. The total area occupied by the RFFE (LNTAs, passive mixers, TIAs, and the modulated LO generator) is  $0.56\text{ mm}^2$ . The area penalty of the LO modulators, the m-sequence generator, and the test sequence generator is less than 10% of the total RFFE area.

### C. Digital Baseband and CS DSP

The IQ imbalance compensation logic followed by a single slice of the DBB logic is shown in Fig. 13. The LO signals

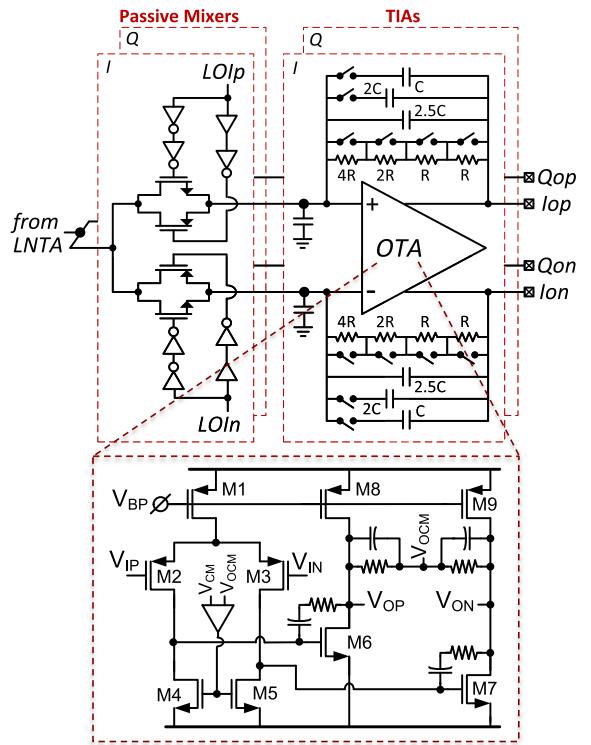


Fig. 11. Passive mixers, TIA, and TIA OTA Schematic. The TIA includes 4-bit programmable resistors and 3-bit programmable capacitors in feedback for gain and bandwidth control. The TIA uses a two-stage Miller-compensated OTA.

with quadrature error are modeled as  $\tilde{\phi}_I(t) = \delta_{11}^* \phi_I(t) + \delta_{12}^* \phi_Q(t)$  and  $\tilde{\phi}_Q(t) = \delta_{21}^* \phi_I(t) + \delta_{22}^* \phi_Q(t)$  with  $\phi_I(t) = (\phi_0 - \phi_2)$  and  $\phi_Q(t) = (\phi_1 - \phi_3)$  as described in Section IV. Here,  $\delta_{11}^*$ ,  $\delta_{12}^*$ ,  $\delta_{21}^*$ , and  $\delta_{22}^*$  are constants with  $\delta_{11}^* = (1 + \epsilon/2)\cos(\gamma/2)$ ,  $\delta_{22}^* = (1 - \epsilon/2)\cos(\gamma/2)$ ,  $\delta_{12}^* = -(1 + \epsilon/2)\sin(\gamma/2)$ , and  $\delta_{21}^* = -(1 - \epsilon/2)\sin(\gamma/2)$ ,  $0 < \epsilon \ll 1$  and  $\gamma$  represents a small phase shift [8]. A calibration procedure described in Section VI is used to derive coefficients  $\{\delta_{11}, \delta_{12}, \delta_{21}, \delta_{22}\}$  shown in Fig. 13.

The DBB slice shown in Fig. 13 is used to extract a higher order IF response of order  $l$  with indices  $\pm l$ , where  $l = 1, 2, \dots, r$ . With the RFFE TIA bandwidth  $f_{TIA} = B(2r + 1)/2$

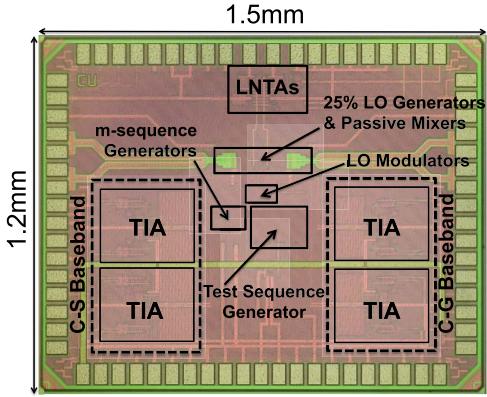


Fig. 12. DRF2IC RFFE chip with a 0.56-mm<sup>2</sup> active area implemented on 65-nm CMOS.

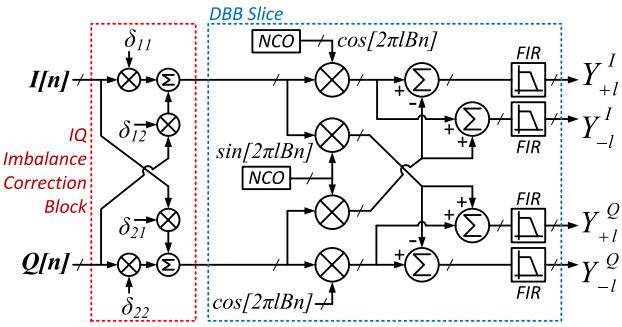


Fig. 13. IQ imbalance correction logic followed by a single slice of the DBB logic block used to extract a pair of complex measurements  $Y_{+l}^I$  and  $Y_{+l}^Q$  and  $Y_{-l}^I$  and  $Y_{-l}^Q$  from an IF response of order  $l$  with indices  $\pm l$ .

and the ADC frequency  $f_{\text{ADC}} \geq B(2r+1)$ , the  $2r$  IF responses shown in Fig. 5 can be extracted using  $r$  DBB slices. The frequency of the numerically controlled oscillator (NCO) is set to  $f_{\text{NCO}} = LB$  to extract the IF response pair with indices  $\pm l$ . The bandwidth of the finite impulse response (FIR) low-pass filters in the DBB is set to  $f_{\text{FIR}} = B/2$ . The response at dc is not processed by a DBB slice, and it is extracted by low-pass filtering with  $f_{\text{FIR}} = B/2$ . Therefore, the two DBB sections shown in Fig. 7 use  $4r$  NCOs and  $4(2r+1)$  FIR filters.

I and Q outputs are summed to form measurements  $(Y_0^I - jY_0^Q)$  and  $(Y_{\pm l}^I - jY_{\pm l}^Q)$ . The OMP [31], [32] algorithm is used in the CS DSP block. The OMP is a simple greedy heuristic for sparse recovery, which forms an estimate of the signal support (or occupied bins) one element at a time. It offers an attractive tradeoff between algorithm simplicity and recovery guarantees. The DRF2IC requires  $\Lambda = 2(2r+1)N_0$  complex multiplications and additions per detected signal in its CS DSP. The DBB and CS DSP are implemented off-chip in software.

## VI. EXPERIMENTAL RESULTS

The *high-sensitivity mode 1* performance of the DRF2IC RFEE chip is summarized in Table IV. At 2.1 GHz, the RFFE chip delivers 40 MHz of RF bandwidth and 41.5-dB conversion gain consuming 46.5 mW from 1.15 V. A  $-75$  dBm in-channel CW signal at 2-MHz offset from the LO is used when determining the swept B1dB performance shown

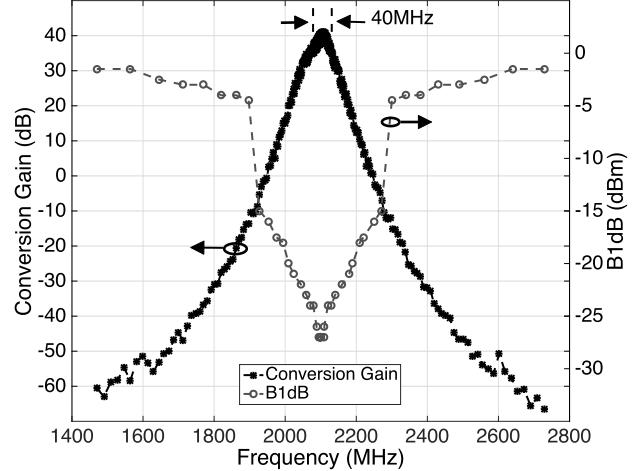


Fig. 14. DRF2IC RFFE conversion gain and swept B1dB performance in mode 1.

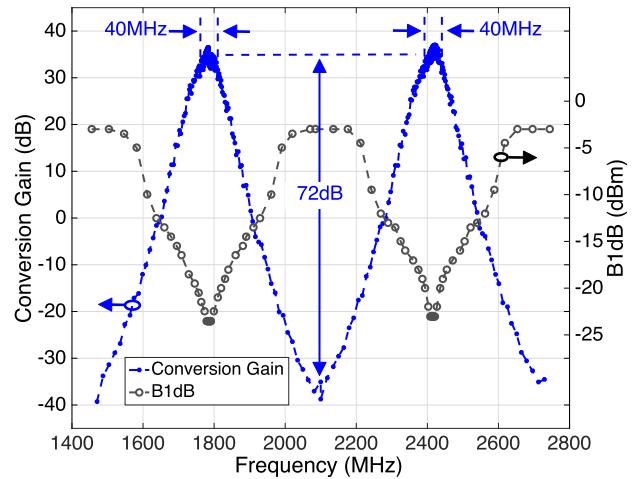


Fig. 15. DRF2IC RFFE conversion gain and swept B1dB performance in mode 2.

in Fig. 14. A CW blocker is swept in frequency, and for each frequency setting, the blocker power is swept until the in-channel CW signal observed at baseband is attenuated by 1 dB. An out-of-channel B1dB of  $-2$  dBm is achieved when the blocker is located at 1.47 or 2.73 GHz. The DRF2IC RFEE achieves 3.6-dB noise figure (NF) after cancellation,  $-26$  dBm P1 dB,  $-11$  dBm in-channel IIP3, and  $+4$  dBm out-of-channel IIP3 with tones at 200- and 395-MHz offset from the LO in mode 1.

In *detection mode 2*, the test sequence generator (see Fig. 8) length is set to 64, and a logic sequence representing four periods of a square wave is loaded into the flip-flop array. With the modulation waveform generator clock set to 1.26 GHz, an effective modulation frequency  $f_M$  of 315 MHz is achieved. With  $f_{\text{LO}}$  set to 2.1 GHz, the RFFE response now consists of two 36-dB conversion gain peaks with 40 MHz of RF bandwidth at 1.785 and 2.415 GHz, as shown in Fig. 15. The RFFE chip consumes 50 mW and simultaneously senses two non-contiguous channels with a cancelled NF of 7.3 dB rejecting an out-of-channel blocker at the midband frequency of 2.1 GHz by 72 dB. Compared with the reception mode,

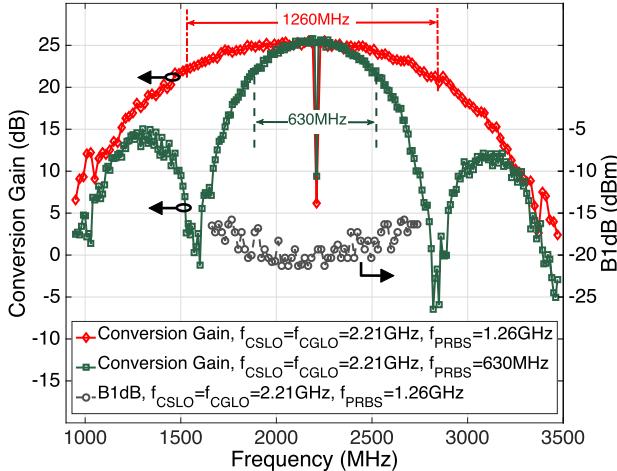


Fig. 16. DRF2IC RFFE conversion gain and swept B1dB performance in CS detection mode 3a, where signal detection is performed in a single wideband frequency span.

an NF degradation in this mode is expected and is due to noise downconversion from two RF channels and gain reduction.

In *wideband detection mode 3a*, the C-S and C-G paths driven by PRBS (m-sequence)-modulated LOs deliver 25-dB conversion gain (see Fig. 16) with a 1.26-GHz span ranging from  $f_{\text{MIN}} = 1.58\text{ GHz}$  to  $f_{\text{MAX}} = 2.84\text{ GHz}$  when  $f_{\text{LO1}}$  and  $f_{\text{LO2}}$  are set to 2.21 GHz, the m-sequence length  $L$  is 63, and clock frequency  $f_{\text{PRBS}}$  is set to 1.26 GHz. The resolution bandwidth  $B$  is 20 MHz with these settings. A  $-60\text{ dBm}$  CW signal at 2.232 GHz (2-MHz offset from the center of the bin upper adjacent to midband at 2.21 GHz) is used when determining the swept B1dB performance shown in Fig. 16. The CW blocker is swept through each of the 63 bins 8-MHz offset from bin center. When observed at baseband, the CW signal and the CW blocker appear at 2 and 8 MHz, since downconversion with a PRBS-modulated LO aliases the signal spectrum such that a portion from each of the 63 bins appears at baseband. For each frequency setting, the CW blocker power is swept until the 2-MHz tone observed at baseband is attenuated by 1 dB. The B1dB is better than  $-22\text{ dBm}$  at midspan and up to  $-15\text{ dBm}$  at the edges  $f_{\text{MIN}}$  and  $f_{\text{MAX}}$ . Also shown in Fig. 16, a resolution bandwidth  $B = 10\text{ MHz}$  and span = 630 MHz ranging from  $f_{\text{MIN}} = 1.895\text{ GHz}$  to  $f_{\text{MAX}} = 2.525\text{ GHz}$  are achieved when  $L$  is 63 and  $f_{\text{PRBS}}$  is set to 630 MHz.

The DRF2IC's ability to suppress image frequencies in wideband detection mode 3a is demonstrated in Fig. 17. LO modulation is disabled (RFFE is configured to mode 1), and a calibration procedure employing a test RF signal consisting of a single  $-44\text{ dBm}$  tone 5-MHz offset from the LO is used to estimate the coefficients  $\{\delta_{11}^*, \delta_{12}^*, \delta_{21}^*, \delta_{22}^*\}$  described in Section V-C. A  $2 \times 2$  matrix with  $\delta_{11}^*$  and  $\delta_{22}^*$  as diagonal elements and  $\delta_{12}^*$  and  $\delta_{21}^*$  as off-diagonal elements is inverted to derive the IQ impairment compensation coefficients  $\{\delta_{11}, \delta_{12}, \delta_{21}, \delta_{22}\}$ , as shown in Fig. 13. LO modulation is then enabled, and the DRF2IC RFFE is configured to mode 3a with a resolution bandwidth of 20 MHz and a span of 1.26 GHz.

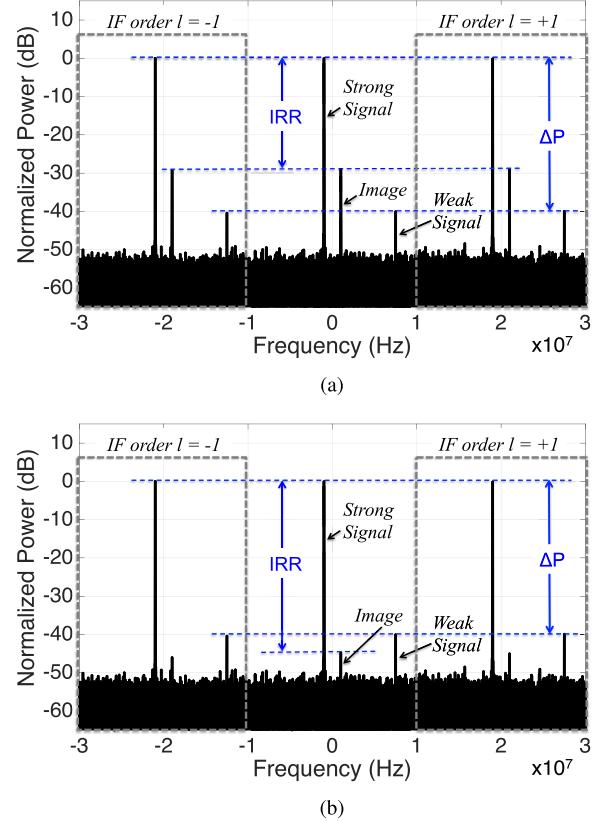


Fig. 17. Spectrum of the DRF2IC RFFE complex baseband signal ( $I - j \cdot Q$ ) in wideband detection mode 3a demonstrating (a) uncorrected IRR of 29 dB and (b) digitally corrected IRR of 45 dB. (a) IQ imbalance compensation disabled. (b) IQ imbalance compensation enabled.

centered at 2.21 GHz by setting  $f_{\text{LO1}} = f_{\text{LO2}} = 2.21\text{ GHz}$ ,  $L = 63$ , and  $f_{\text{PRBS}} = 1.26\text{ GHz}$ . A test signal consisting of two tones is used to demonstrate image suppression. The  $-27\text{ dBm}$  strong tone is located at 2.069 GHz ( $-1\text{ MHz}$  offset from the bin center of 2.07 GHz and 141 MHz below the LO center of 2.21 GHz). The  $-67\text{ dBm}$  weak tone is located at 2.5175 GHz ( $+7.5\text{ MHz}$  offset from the bin center of 2.51 GHz and 300 MHz above the LO center). Since downconversion with a PRBS-modulated LO causes each of the 63 bins to simultaneously appear at baseband, the normalized spectrum of the complex baseband signal ( $I - j \cdot Q$ ) shown in Fig. 17 includes wanted tones at  $-1$  and  $+7.5\text{ MHz}$  in addition to a spurious tone at  $+1\text{ MHz}$  caused by the finite suppression of the strong signal's image at  $-2.069\text{ GHz}$ . By programming the TIAs to deliver a bandwidth above 30 MHz, the response centered at dc in addition to higher order responses centered at  $-20\text{ MHz}$  ( $l = -1$ ) and  $20\text{ MHz}$  ( $l = +1$ ) may be observed, as shown in Fig. 17. While the uncompensated image rejection ratio (IRR) in Fig. 17(a) is roughly 29 dB, the worse case digitally compensated IRR in Fig. 17(b) is 45 dB. The digitally suppressed spurious tone is 5 dB below the weak signal, thereby enabling an IDR ( $\Delta P$ ) of 40 dB or better.

The DRF2IC system in wideband detection mode 3a is scaled as shown in Fig. 18 from detecting 3 bins to detecting 6 bins with a width of 10 MHz with its  $m = 2$  IQ branch pairs by increasing the ADC clock frequency  $f_{\text{ADC}}$  from 63 to 105 MHz and increasing the number of measurements

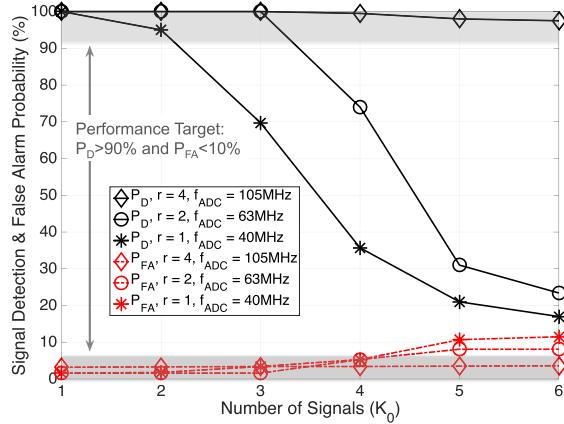


Fig. 18. DRF2IC in CS detection mode 3 is scaled from detecting 3 bins to detecting 6 bins with a  $P_D > 90\%$  and  $P_{FA} < 10\%$  by increasing the number of DBB slices ( $2r$ ) and ADC clock frequency ( $f_{ADC}$ ) from 2 and 40 MHz to 8 and 105 MHz.

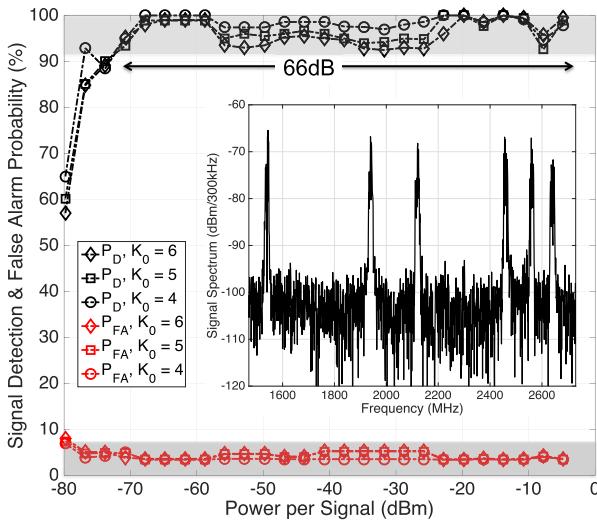


Fig. 19. DRF2IC performance in CS detection mode 3a. The location of up to 6 bins with a width of 10 MHz scattered over a 1.27-GHz span is found in 1.2  $\mu$ s while maintaining  $P_D > 90\%$  and  $P_{FA} < 10\%$ . Inset: spectrum of a test signal with six occupied bins.

$R = m(2r + 1)$  from 10, where  $r = 2$ , to 18, where  $r = 4$ . When  $f_{ADC} = 63$  MHz and  $R = 10$ , a detection probability  $P_D > 90\%$  and a false alarm  $P_{FA} < 10\%$  are maintained for up to  $K_0 = 3$  bins. To generate each pair of  $P_D$  and  $P_{FA}$  data points in Fig. 18, 125 experiments are conducted where the location of the  $K_0$  occupied bins are changed from one experiment to the next. Each of the  $K_0$  bins is set to a power of  $-54$  dBm. When  $f_{ADC} = 105$  MHz and  $R = 18$ ,  $K_0 = 6$  bins are detected with  $P_D > 90\%$  and  $P_{FA} < 10\%$ . With the system appropriately scaled, the CS DSP uses 125 samples from each of the  $R = 18$  measurements and detects up to 6 occupied bins with a width of 10 MHz scattered over a 1.27-GHz span in 1.2  $\mu$ s, as shown in Fig. 19. The minimum and maximum detectable signal levels are  $-71$  and  $-4.8$  dBm with  $P_D > 90\%$  and  $P_{FA} < 10\%$ , thus achieving a 66-dB operational dynamic range.

In wideband detection mode 3b, two disjoint bands can be simultaneously monitored by uncoupling the C-S and C-G

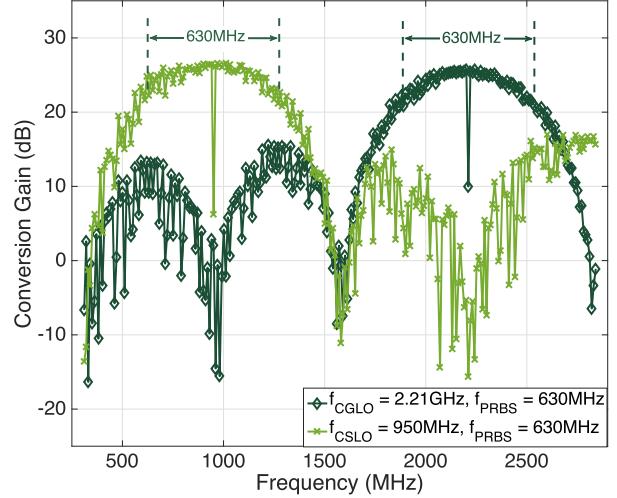


Fig. 20. DRF2IC RFFE conversion gain in CS detection mode 3b, where signal detection is performed in two disjoint wideband frequency spans.

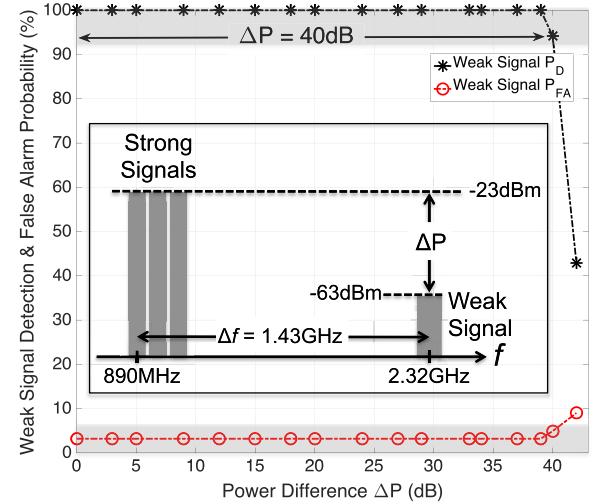


Fig. 21. IBW and IDR of the DRF2IC RFFE in CS detection mode 3. Inset: spectrum of the test signal.

paths and driving their mixers with distinct LOs modulated with PRBSs. Setting  $f_{CSLO} = 950$  MHz,  $f_{CGLO} = 2.21$  GHz, and  $f_{PRBS} = 630$  MHz, the DRF2IC RFFE now delivers two disjoint wideband frequency spans extending from 635 MHz to 1.265 GHz and from 1.895 to 2.525 GHz, as shown in Fig. 20.

The IDR in Fig. 21 is measured by sweeping the power of a weak interferer at 2.32 GHz while fixing the power of three strong interferers at 890 MHz. The IDR ( $\Delta P$  in Fig. 21) is the maximum power difference between the strong and weak interferers, such that  $P_D > 90\%$  and  $P_{FA} < 10\%$  are maintained for the weak interferer. An IDR of 40 dB [6.64 effective number of bits (ENOBs)] and an instantaneous bandwidth (IBW) of 1.43 GHz are achieved. The calibration approach in [6] may be used to further improve IDR. The DRF2IC RFFE consumes 58.5 mW from 1.15 V in wideband detection modes 3a and 3b.

To demonstrate *fast mode switching* in Fig. 22, a tone at 2.105 GHz and a 20-MHz noiselike signal at 2.44 GHz are used to measure the DRF2IC RFFE mode switching time.

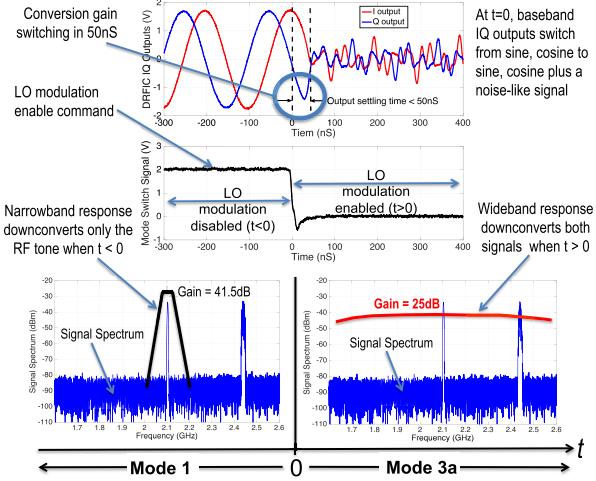


Fig. 22. DRF2IC RFFE requires 50 ns to switch from high-sensitivity reception mode to CS wideband detection.

TABLE IV

DRF2IC RFFE PERFORMANCE IN MODE 1 COMPARED WITH AN SOA FTNC RECEIVER

|                                | FTNC [21]            | This Work [4]     |
|--------------------------------|----------------------|-------------------|
| CMOS Technology [nm]           | 28                   | 65                |
| RX Frequency [MHz]             | 600-3000             | 600-3000          |
| RF Bandwidth [MHz]             | 6                    | 40                |
| Number of LO Phases            | 8                    | 4                 |
| Noise Figure [dB]              | 1.8-3 <sup>[a]</sup> | 3.6               |
| Out-of-channel IIP3 [dBm]      | +10                  | +4                |
| B1dB [dBm]                     | -2.5 <sup>[b]</sup>  | -2 <sup>[c]</sup> |
| Supply Voltage [V]             | 1                    | 1.15              |
| Power [mW]                     | 38.8-70              | 46.5              |
| Active Area [mm <sup>2</sup> ] | 5.2 <sup>[d]</sup>   | 0.56              |

[a] Measured NF is 1.8dB in low NF mode and 3dB in harmonic blocker rejection mode

[b] B1dB is measured with the blocker 80MHz offset from the 2GHz carrier. The blocker offset ( $\Delta f$ ) to TIA bandwidth (TIA3dB) ratio is  $(\Delta f / \text{TIA3dB}) = 80/3 = 26.7$

[c] B1dB is measured at 540MHz offset from 2.1GHz carrier (note that  $\Delta f / \text{TIA3dB} = 27$ )

[d] Reported area includes 200kHz bandwidth TIAs. The estimated area with 3MHz bandwidth TIAs is 1.2mm<sup>2</sup>.

Initially, in reception mode with  $f_{LO} = 2.1$  GHz, the RFFE downconverts the RF tone to baseband and rejects the noiselike signal. At time  $t = 0$ , the RFFE is switched from high-sensitivity reception to wideband detection mode by enabling LO modulation, and the baseband signal switches from a 5-MHz sinusoid to a superposition of the sinusoid and the noiselike signal in 50 ns.

## VII. DISCUSSION AND COMPARISON TO THE STATE OF THE ART

The performance of the DRF2IC as a signal receiver in mode 1 summarized in Table IV parallels the SoA FTNC [21] receiver when adjusted for signal bandwidth. It delivers a 76-dB spurious free dynamic range (SFDR) adjusted to a 1-MHz bandwidth. Thus, the performance of the DRF2IC as a signal detector in mode 1 compares favorably with recently published spectrum analyzers on chip [13]–[18] shown in the top-right cluster of Fig. 23. While the cross correlation spectrum analyzer [13] delivers an 89-dB SFDR, it consumes an estimated six times more energy compared with the

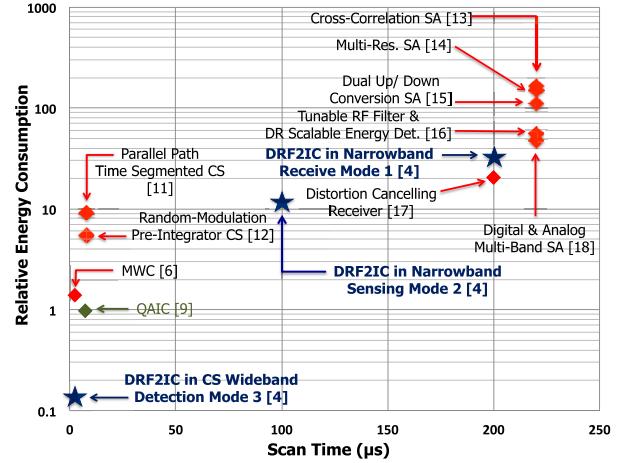


Fig. 23. DRF2IC chip in various modes compared with CS signal detectors and traditional sweeping spectrum analyzers.

DRF2IC in mode 1. The DRF2IC in mode 2 can bifurcate a frequency range of interest and sweep through this range while performing signal detection in a pair of channels at a time, thereby delivering a useful combination of moderate sensitivity (7.3-dB NF), sweep time, and energy consumption, as shown in the center of Fig. 23.

The DRF2IC delivers the best reported combination of speed and energy consumption when compared with recently published CS wideband detectors on chip [6], [9], [11], [12] shown in the bottom-left cluster of Fig. 23. Contrasted with the QAIC [9] and MWC [6] in Table V, the DRF2IC requires only two PRBSs to produce enough measurements to detect six signal components with the standard two IQ branch pairs in an FTNC receiver by using the higher order IF responses resulting from downconversion with a PRBS-modulated LO. In contrast, the QAIC in [9] requires eight PRBSs and eight IF branches to detect three signals. Requiring only a small number of PRBSs, the DRF2IC can select m-sequences with the desired optimal flat spectral profiles. Compared with the MWC [6], the DRF2IC reduces the PRBS length and clock frequency by 5.8 times while also enabling an estimated 5.8 times reduction in complexity (i.e., number of multiplications) of the CS DSP [31], [32] for a frequency range of interest extending from 2.7 to 3.7 GHz and a resolution bandwidth  $B = 10$  MHz. When computing the number of multiplications required in the CS DSP per detected signal component,  $R = 2(2r + 1) = 6$  with  $r = 1$  is used for the DRF2IC and the MWC, whereas  $R = m = 8$  is used for the QAIC. The DRF2IC achieves up to a 12.2 times reduction in RFFE energy consumption per detected interferer. It achieves up to a 17.4 times improvement in CS RF frontend FOM =  $P_{RFFE}/(m \cdot f_{ADC} \cdot 2^{ENOBs})$ , where  $P_{RFFE}$  is the RF frontend (including LNA, PLL, and ADCs) power,  $m \cdot f_{ADC}$  is the aggregate sampling rate, and  $2^{ENOBs}$  is the measured IDR.

The DRF2IC compactly adds CS wideband detection to an FTNC receiver by introducing pseudo-random LO modulation. The active area of the DRF2IC RFFE, including the LO modulation circuitry, is 0.56 mm<sup>2</sup>, as shown in Fig. 12. The area needed to implement LO modulation is less than 0.06 mm<sup>2</sup>,

TABLE V  
DRF2IC PERFORMANCE IN CS WIDEBAND DETECTION MODE COMPARED WITH OTHER CS SIGNAL DETECTOR CHIPS

|  |            | <b>QAIC [9]</b> | <b>MWC [6]</b> | <b>This Work [4]</b> |
|--|------------|-----------------|----------------|----------------------|
| Number of Branches in the RFFE                     |            | 16              | 5              | 4                    |
| Aggregate Sampling Rate*                           | [MHz]      | 320             | 525            | 420                  |
| Number of Detected Signals                         |            | 3               | 4              | 6                    |
| Measured Input Frequency Range                     | [GHz]      | 2.7-3.7         | 0-0.9          | 0.635-2.84           |
| Measured RFFE Chip Power                           | [mW]       | 80              | 704            | 58.5                 |
| Required Number of Independent PRBSs               |            | 8               | 5              | 2                    |
| *PRBS length                                       |            | 127             | 740            | 127                  |
| *PRBS clock frequency                              | [GHz]      | 1.27            | 7.4            | 1.27                 |
| *Estimated RFFE Power with LNA, PLL, ADCs          | [mW]       | 120             | 897 #          | 110                  |
| Scan Time  | [us]       | 4.4             | 1.2            | 1.2                  |
| RFFE Energy per Scan                               | [nJ]       | 528             | 1076           | 132                  |
| RFFE Energy per Detected Signal                    | [nJ]       | 176             | 269            | 22                   |
| Relative RFFE Energy per Detected Signal           |            | 8               | 12.2           | 1                    |
| &Estimated Number of Multiplications in the CS DSP |            | 1016            | 4440           | 762                  |
| Measured Instantaneous Dynamic Range               | [ENOBs]    | 3               | 6.1            | 6.6                  |
| Measured Instantaneous Bandwidth                   | [GHz]      | 1               | 0.9            | 1.43                 |
| Detector RFFE Figure of Merit (FOM)                | [pJ/conv.] | 46.9            | 24.9           | 2.7                  |

\* All systems are scaled to a common input frequency range:  $f_{\min}=2.7\text{GHz}$  to  $f_{\max}=3.7\text{GHz}$

# A single shared shift register bank (length 740, clock 7.4GHz) for all branches in [7] is assumed

& Number of multiplications per detected signal per sample when scanning 2.7-3.7GHz with B=10MHz

which is roughly 10% of the 0.5-mm<sup>2</sup> area occupied by the implemented FTNC receiver in [4].

### VIII. CONCLUSION

The DRF2IC presented here is a reconfigurable architecture employing a flexible LO modulator and two direct-conversion IQ branch pairs. It has the potential to significantly reduce RF hardware area and complexity in a spectrum-aware CR receiver by introducing functional flexibility. The DRF2IC compactly unifies noise cancelling reception and CS wideband detection into a single RFFE.

In reception mode, the DRF2IC parallels the performance of the SoA FTNC receiver. In CS wideband detection mode, the DRF2IC retains key advantages of both the MWC and the QAIC while avoiding the drawbacks of each architecture. In contrast with the MWC, it scales easily to higher frequencies by uncoupling the PRBS clock frequency from the maximum frequency of interest. It employs a direct-conversion RF chain in contrast with the QAIC. Coupling its two IQ branch pairs, the DRF2IC can perform noise cancellation in a single channel or CS detection over a single wideband frequency span. The DRF2IC RFFE has a unique feature that allows the user to uncouple its two IQ branch pairs and perform CS detection in two disjoint wideband frequency spans, thereby achieving an SoA combination of energy consumption, IBW, and IDR.

The DRF2IC prototype chip can switch from high-sensitivity signal reception to CS wideband signal detection in roughly 50 ns. The functional flexibility combined with fast reconfigurability of the DRF2IC has the potential to enable future CR terminals that rapidly gain awareness of their fast changing spectrum environment and opportunistically gain access to a shared pool of fragmented spectrum while meeting the cost, size, and power targets in mass-market applications.

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