

A 500-MHz Bandwidth 7.5-mV_{pp} Ripple Power-Amplifier Supply Modulator for RF Polar Transmitters

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Abstract—The parallel combination of a switching and a linear amplifier in the supply modulator for RF power amplifiers (PAs) has the potential to enhance energy efficiency while achieving wider bandwidth and lower ripple output voltage. In this paper, a linear amplifier that features a buffered-switching Class-AB bias scheme is presented for the supply modulator in polar-transmitter structures achieving 500 MHz of small-signal 3-dB bandwidth at a 1.2-V supply. The linear amplifier absorbs and cancels up to 60 mA of ripple current from the switching amplifier. As such, the ripple in the output voltage of the hybrid linear-switching supply modulator is less than 7.5 mV_{pp}. The switching amplifier provides most of the signal current for greatest efficiency owing to a proposed rail-to-rail current-sensing circuit. Current feedback in the switching amplifier achieves 1.68-MHz unity-gain bandwidth at 6-MHz switching frequency. Harmonic distortion in the output voltage of the supply modulator is below 40 dBc at 0.8 V_{pp} sinusoidal input up to 9 MHz. The peak efficiency is 87.7% for a 8.25-Ω load, while the maximum output power is 23.6 dBm for a 4.99-Ω load. The chip measures 1.35 mm² in a 65-nm standard bulk CMOS process.

Index Terms—Class-AB bias, current feedback, current sensing, envelope elimination and restoration, hybrid supply modulator (HSM), open-loop gate driver polar transmitter, three-stage amplifier, wide bandwidth.

I. INTRODUCTION

POLAR transmitter architectures offer superior energy efficiency and sufficient linearity for the high peak-to-average power ratio (PAPR) signals of modern wireless communication

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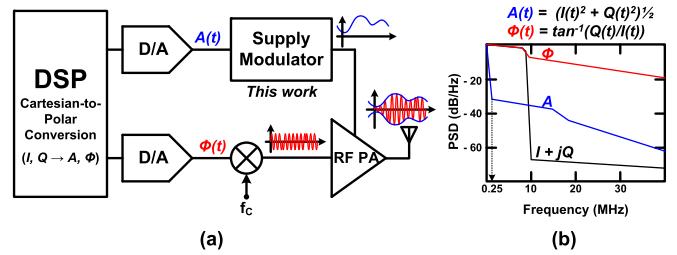


Fig. 1. (a) Architecture of a polar modulated transmitter. (b) Power spectral density of polar modulated signals.

systems [1]–[4]. Owing to the Cartesian-to-polar conversion in the architecture as shown in Fig. 1(a), the constant-amplitude phase signal ($\phi(t)$) is amplified by an efficient switched-mode power amplifier (PA) while the envelope signal ($A(t)$) is modulated at the supply of the PA by a supply modulator. However, due to the non-linearity in the Cartesian-to-polar transformation, $\phi(t)$ and $A(t)$ occupy much wider bandwidths, compared to the in-phase and quadrature phase signals as shown in Fig. 1(b) [4]–[6]. Furthermore, ripples at the output of the supply modulator generate spurious tones at the output of the polar architecture. Therefore, the supply modulator used in such transmitter systems must have a wide bandwidth, low ripple, and high energy efficiency for a high fidelity restoration of the amplitude information [7].

Among the various advanced supply modulator structures [3], [8]–[12], the hybrid supply modulator (HSM) shown in Fig. 2 has been widely utilized [2], [13]–[23]. The HSM is composed of two parallel amplifiers: an energy efficient switching amplifier and a wide bandwidth linear amplifier. The switching amplifier provides several 100 mW of power to the PA drain with an efficiency greater than 90%. However, it has a limited signal bandwidth and produces severe switching ripple. An increase in the switching frequency up to several 100 MHz could improve the signal bandwidth and ripple issues at the expense of increased switching loss, degrading efficiency. Fortunately, most of the energy of the polar-modulated envelope signal is concentrated at low frequency. For the 802.11-g orthogonal frequency-division multiplexing (OFDM) envelope signal, more than 80% of the energy is concentrated between DC to 250 kHz, as illustrated in Fig. 1(b) [7]. Hence, in the

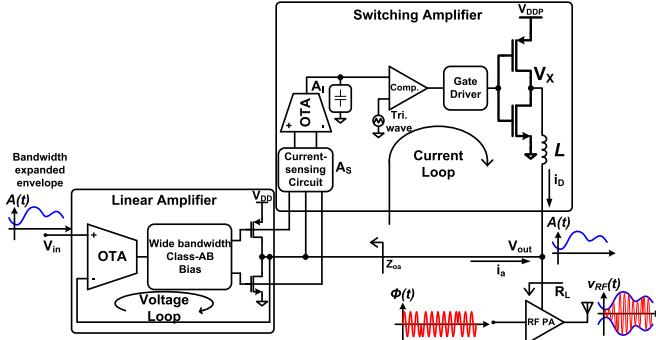


Fig. 2. Block diagram of the HSM.

HSM, the switching amplifier provides most of the signal current at low frequency, while the linear amplifier supplies the residual current at high frequency to set the output voltage with minimum ripple by absorbing the ripple current from the switching amplifier. As such, the structure of the HSM combines high efficiency, low ripple, and wide bandwidth.

Although the HSM structure has been extensively investigated, the switching amplifier feedback loop has not been rigorously analyzed with supporting measurement results. Furthermore, the small-signal bandwidth of the supply modulator should be increased to at least 100 MHz, required for the 802.11-g OFDM signals to have less than 2% error-vector-magnitude (EVM) [16] and to have a margin to meet the mandated spectral mask [6]. Delay mismatch between envelope and phase paths may further degrade EVM, adding to the importance of a wide bandwidth of the supply modulator.

To overcome these current design difficulties, this paper presents the design of an energy efficient HSM with a linear amplifier having a small-signal bandwidth wider than 500 MHz. In-depth analysis of the current feedback loop in the switching amplifier provided in Section II illustrates the procedure to maximize the bandwidth of the current feedback loop at a given switching frequency, leading to further improvement in efficiency. Simplified circuit schematics and initial measurement results of the linear amplifier were presented in [24]. This paper presents detailed schematics, in-depth analysis for both the voltage and current feedback loops, and more substantial measurement results.

This paper is organized as outlined in this section. Section II provides the theoretical analysis of the current feedback loop of the switching amplifier. Section III presents the design details of the linear amplifier including gain-boosting, Class-AB bias, and modified nested-Miller compensation (NMC). Section IV examines the design of the switching amplifier including the current-sensing circuit, integrator, gate driver, and current loop. Section V presents simulation and measured results. Finally, conclusions are provided in Section VI.

II. ANALYSIS OF THE CURRENT FEEDBACK

The switching amplifier acquires a scaled current from the output stage of the linear amplifier as its input signal through a current sensor, as shown in Fig. 2. The sensor transforms the received current signal to a voltage signal with a gain A_S .

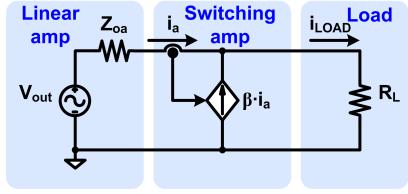


Fig. 3. Simplified circuit model of the HSM [13].

This voltage signal serves as an error signal to the current loop and is integrated by a following integrator with a gain of A_I . To minimize the integrated error signal by producing a pulsewidth modulated voltage waveform according to the integrated errors at node V_X and thus, generating output current through an inductor; a comparator compares the integrated error signal with an internally generated triangular waveform. The output current flows to an RF PA load and to the linear amplifier. Indeed, the switching amplifier forms a current feedback loop. Owing to this current amplification in the feedback, most of the power in the signal is supplied by the efficient switching amplifier rather than the linear amplifier, which improves the efficiency of the supply modulator. This feedback mechanism is similar to the property of a single bipolar-junction-transistor (BJT)s base current being minimized by its local current feedback. To maximize the benefit from the current feedback, it is important for the current feedback to provide high gain and sufficient bandwidth [14], [21]. However, like a conventional switched-mode DC-DC converter, the loop bandwidth should be less than the switching frequency. Otherwise, switching noise will contaminate the feedback loop. Therefore, in order to maximize its bandwidth at a given switching frequency, an accurate analysis of the current feedback loop encompassing the switching amplifier should be performed.

Fig. 3 shows a conceptual schematic of the HSM for the analysis of the current feedback loop of the switching amplifier. An ideal voltage source and an output resistor provide a simplified model for the linear amplifier with its output impedance, while a current sensor and a dependent current source with a gain of β model the switching amplifier [13]. For simplicity, a load PA is modeled with a resistor, R_L . In order to investigate the current feedback operation, the conceptual diagram is rearranged similar to the T-model of a BJT, as illustrated in Fig. 4(a). Consequently, an additional dependent current source is inserted, as shown in Fig. 4(b). This added dependent current source has no impact on the original characteristics of the current loop. From Fig. 4(c), it is apparent that the current feedback is formed from the relationship between these two dependent current sources. To find the loop gain of the current feedback, the current feedback loop should be broken by cutting the relationship between the two dependent current sources. Thus, one dependent current source is replaced with a test independent current source as the input i_x , while the other dependent current source serves as the output in the feedback, respectively [25], [26]. Finally, the voltage source in Fig. 4(c) is eliminated for AC analysis as depicted in Fig. 4(d). The loop gain of the current feedback,

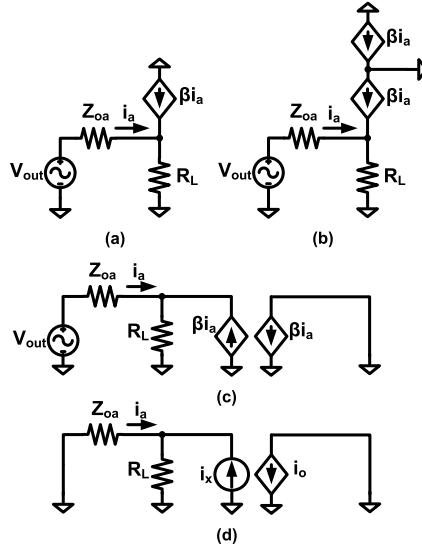


Fig. 4. (a) AC model for analysis of the current feedback. (b) AC model with a newly added dependent current source. (c) Rearranged AC model. (d) AC model without a NFB [25].

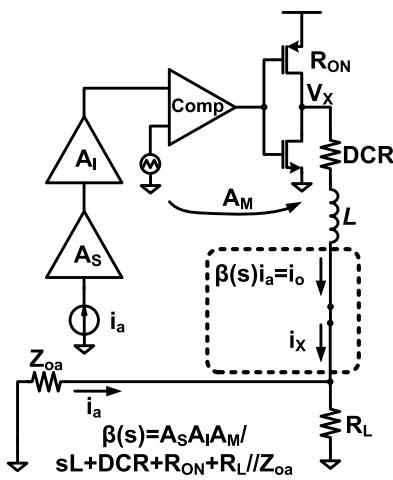


Fig. 5. Simplified block diagram of the HSM for current feedback analysis.

$T(s)$, is then defined as

$$T(s) = \frac{i_o(s)}{i_x} \quad (1)$$

where

$$-i_a(s) = \frac{R_L}{Z_{oa}(s) + R_L} i_x \quad \text{and} \quad i_o(s) = -\frac{\beta(s) R_L}{Z_{oa}(s) + R_L} i_x. \quad (2)$$

An expression for $\beta(s)$ can be derived directly by considering a redrawn HSM schematic, under the assumption that the current feedback loop is eliminated by breaking the current path, as illustrated in Fig. 5. The gain terms A_S and A_I are from the current sensor and the error integrator, respectively. The non-linear switching components such as the comparator and the power inverter are considered to be linear components with a gain of A_M , assuming that the switching frequency is higher than the loop bandwidth. This simplification is similar to a conventional DC-DC converter feedback analysis, at the expense of reduced precision [27]. The inductor creates a

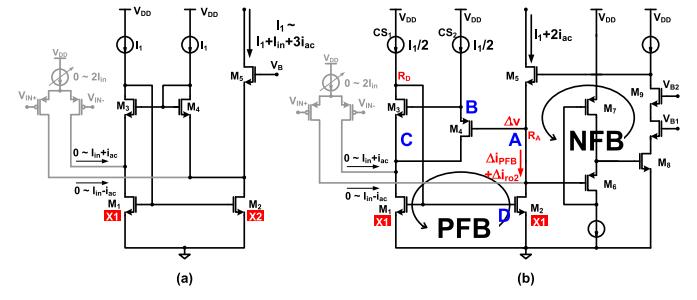


Fig. 6. (a) Conventional current mirror for high output impedance [28]. (b) Proposed buffered high output-impedance current mirror.

low-pass filter by forming a pole with the sum of the resistances in the inductor current path, $DCR + R_{ON} + R_L || R_{OA}$. Hence, the current-loop gain induces negative feedback (NFB) with

$$T(s) = -\frac{A_S(s)A_I(s)A_M R_L}{(sL + DCR + R_{ON} + R_L || Z_{oa}(s))(Z_{oa}(s) + R_L)}. \quad (3)$$

At low frequency, the denominator simplifies to $(DCR + R_{ON} + Z_{oa})R_L$, which ranges from 2 to 4 Ω for a PA load of $R_L = 5 \Omega$. Because of the cascaded active gains, A_S and A_I , the loop gain at low frequency is sufficiently large enough to suppress the current from the linear amplifier. Detailed loop design is shown in Section IV-C.

III. DESIGN OF THE LINEAR AMPLIFIER

Stringent design requirements of the HSM such as a wide bandwidth and a low ripple voltage while driving a heavy PA load are directly related to the design of the linear amplifier. To compensate the attenuation caused by the heavy PA load, a three-stage amplifier structure with a gain-boosting technique is utilized. To realize an ultra-wide bandwidth and a high current driving capability without increasing the static current consumption, a buffered-switching Class-AB (BS-Class-AB) bias scheme is proposed.

A. Gain-Boosting Scheme

Local NFB typically has been utilized to implement regulated cascode current mirrors for gain enhancement in gain-boosting amplifiers [29]. It is important to note that, for wide bandwidth applications, the local NFB in regulated cascode current mirrors should have a dominant pole at a relatively high frequency. Otherwise, a pole-zero doublet is induced in the frequency response of the gain-boosting amplifier by the local NFB, and thereby, settling time of the amplifier is severely degraded [29]. Thus, adopting a local positive feedback (PFB) along with the local NFB for gain enhancement is a promising solution for wide bandwidth gain-boosting amplifiers.

Fig. 6(a) shows a conventional current mirror with a PFB to boost the output impedance of the mirror [28]. Although it performs well as a current mirror, it is, unfortunately, not applicable to the gain stage(s) of rail-to-rail input amplifiers. One of the main reasons is that the input current from the differential pair of input stage varies by the input common-mode level from 0 to $I_{in} \pm i_{AC}$, and thus, the output current

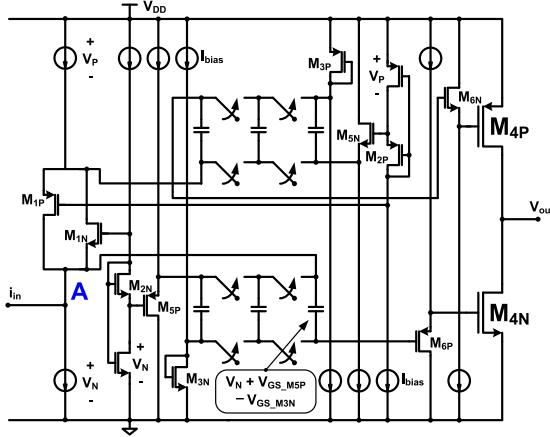


Fig. 7. Proposed BS-Class-AB scheme for wide bandwidth and low-voltage operation.

of this current mirror flowing through M_5 changes depending on the input current level. The main culprit of the output bias current shift is the size difference between M_1 and M_2 in Fig. 6(a).

The proposed buffered high-impedance current mirror shown in Fig. 6(b) has both a PFB and a NFB to achieve a wide bandwidth as well as a high gain. Operation of the PFB, which is formed by M_1 , M_2 , M_4 , and M_3 , is described as follows. When the voltage of node A is increases, the current through the output resistance r_o of M_2 increases. At the same time, the voltages of nodes B and C are also increased because of the source following behavior of M_4 and M_3 , respectively. Then, owing to an increased current though r_o of M_1 , node D becomes lower, and thus, the current of M_2 decreases. By this feedback mechanism, current bias variations caused by voltage changes in node A are suppressed. In other words, the impedance of node A is increased, which thereby increases the output impedance of the current source at the drain node of M_5 .

To further enhance the gain and stability of the current mirror, an NFB structure is combined together with the PFB, as shown in Fig. 6(b). Owing to this NFB, the impedance at the source of M_5 becomes even smaller at low frequency, thereby decreasing the loop gain of the PFB to far less than 1. Thus, the PFB loop is stable. Nonetheless, the impedance boosting effect from the PFB remains unchanged since the impedance boosting effect is not related to the source impedance of M_5 , which is shown in Appendix A. Furthermore, the burden of the NFB to obtain high gain is mitigated by the PFB, pushing the dominant pole of the NFB loop to be higher than 1 MHz. The unity-gain bandwidth (UGB) of the NFB loop with the impedance boosting by the PFB is simulated by breaking the loop and inserting a test voltage source at the gate of M_5 and, is approximately 1.9 and 0.9 GHz for the NMOS and PMOS sides, respectively. The front stage of the linear amplifier is designed to have 95 dB of gain.

B. BS-Class-AB Bias Scheme

The proposed BS-Class-AB scheme is depicted in Fig. 7. The final-stage transistors M_{4N} and M_{4P} of the linear

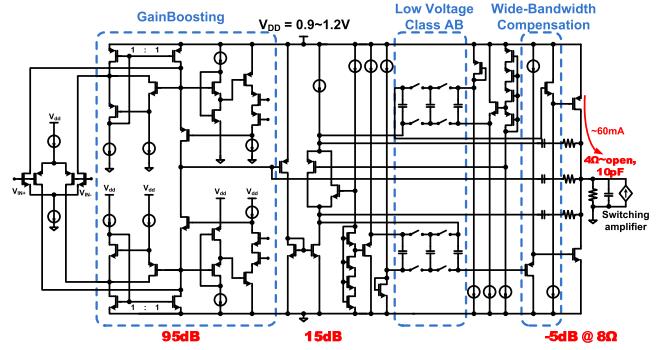


Fig. 8. Complete schematic of the presented wide bandwidth linear amplifier.

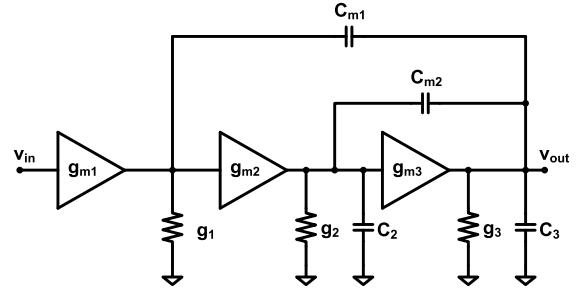


Fig. 9. Three-stage amplifier for frequency compensation analysis.

amplifier are driven by source followers M_{6N} and M_{6P} . Because of the large size of M_{4N} and M_{4P} ($135\ \mu\text{m}/0.1\ \mu\text{m}$ and $405\ \mu\text{m}/0.1\ \mu\text{m}$, respectively), the sum of the gate capacitances is $630\ \text{fF}$. The source followers M_{6N} and M_{6P} drive the gate capacitances while providing reduced gate capacitances to the high-impedance node A because of their own NFB in the source follower structure. By this method, the effective parasitic capacitance at node A is significantly reduced from 630 to $50\ \text{fF}$. It is worth noting that the reduced gate capacitance is only available when the gain of the source follower is close to 1. Not only wide bandwidth but also low-voltage operation is achievable because the switched capacitor circuit in the BS-Class-AB shifts the DC voltage bias. In the NMOS side of BS-Class-AB, for example, the charged DC bias voltage in the switched capacitor is $V_N + V_{GS_M5P} - V_{GS_M3N}$. Since V_{GS_M6P} is designed to be the same as V_{GS_M5P} and V_{GS_M3N} is the same as V_{GS_M4N} . As a result, the idling current through the output M_{4N} (M_{4P}) is adjusted by the bias current of M_{3N} (M_{3P}) and the size ratio of M_{3N} (M_{3P}) and M_{4N} (M_{4P}). To avoid severe gain attenuation through capacitive division from node A to M_{6N} and M_{6P} , greater than 500-fF capacitors are utilized. Owing to this BS-Class-AB structure, the linear amplifier achieves a 500-MHz bandwidth, and provides a 60-mA peak current with 13-mA static current consumption from a 1.2-V supply.

C. Compensation

Fig. 8 shows a complete schematic of the linear amplifier. The linear amplifier is designed to have an overall DC gain of 105 dB with a load of $8\ \Omega$ and operate for the supply voltages ranging from 0.9 to 1.2 V. Since this amplifier has three gain stages, it has three high-impedance nodes.

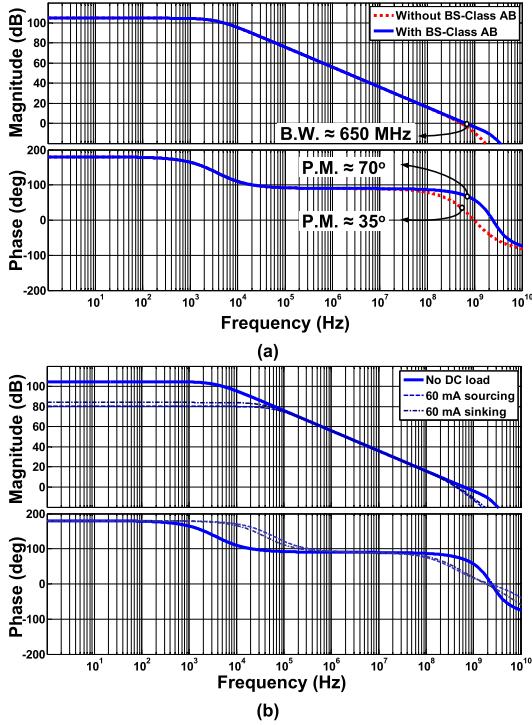


Fig. 10. Frequency responses of (a) NMC and the NMC with the BS-Class-AB bias scheme and (b) with no DC load and ± 60 -mA DC current loads.

Therefore, an NMC scheme is adopted to ensure stability given a load varying from 4Ω to an open circuit. Fig. 9 shows a block diagram of the NMC amplifier, where $g_{m(1,2,3)}$, $g_{(1,2,3)}$, and $C_{(2,3)}$ are the transconductance, output conductance, and parasitic capacitance at the output of each stage, respectively. The natural frequency and damping factor are

$$w_n = \alpha \sqrt{\frac{g_{m2}g_{m3}}{C_2}} \quad (4)$$

and

$$\zeta = \frac{\alpha}{2} (4g_3 + 3g_{m3}) \sqrt{\frac{C_2}{g_{m2}g_{m3}}} \quad (5)$$

where $\alpha = 1/(2\sqrt{C_3})$. To obtain a maximally flat response, ζ should be $1/\sqrt{2}$ [30], resulting in a natural frequency of

$$w_n = \frac{1}{\sqrt{2}C_3} \left(g_3 + \frac{3g_{m3}}{4} \right). \quad (6)$$

Considering that g_3 and C_3 are mostly determined by the RF PA load, g_{m3} is the only controllable design variable in (6). This implies that an increase in the bias current at the final stage of the linear amplifier is the sole plausible option to obtain a wide bandwidth. On the other hand, the BS-Class-AB scheme offers reduced power consumption. For a fixed ζ of $1/\sqrt{2}$, the BS-Class-AB scheme decreases C_2 from 630 to 50 fF, and thereby, decreases g_{m2} by the same factor as shown in (5).

Fig. 10(a) shows the frequency responses of the NMC with and without the BS-Class-AB with design parameters as follows: $g_{m1} = 0.83$ mS, $g_{m2} = 3.78$ mS, $g_{m3} = 138.45$ mS, $g_1 = 1/48860$ mS, $g_2 = 1/1.62$ mS, $g_3 = 1/0.005$ mS,

$C_1 = 35.27$ fF, $C_3 = 20$ pF, $C_{m1} = 208$ fF, and $C_{m2} = 63$ fF. C_2 is 630 fF for NMC without the BS-Class-AB and 50.2 fF for NMC with the BS-Class-AB. Since ζ and w_n are proportional to C_2 , the UGB and phase margin (PM) of the NMC with the BS-Class-AB are better than NMC without BS-Class-AB. If only NMC is applied, then the UGB should be lower than 200 MHz for proper PM. This analysis shows that the UGB of NMC with the BS-Class-AB is approximately 650 MHz with a PM of approximately 70°. It is worth noting that when ± 60 -mA DC current loads are applied, the frequency response changes accordingly, the bandwidth and PM decrease to 430 MHz and 41°, respectively, due to a change in the small-signal parameters, and especially an increased g_2 , as shown in Fig. 10(b).

IV. DESIGN OF THE SWITCHING AMPLIFIER

The design of an efficient switching amplifier is another important task for the HSM. A current-sensing circuit receives a scaled output current from the linear amplifier and transforms it to a voltage signal for comparison with an internally generated triangular waveform. The comparator output becomes a pulsedwidth modulated signal, which defines the amount of output current to an RF PA load and through an inductor. Current-loop optimization based on the accurate analysis in Section II is crucial for the stability and the efficiency of the HSM.

A. Accurate Current-Sensing Circuit

The current-sensing circuit plays a significant role in achieving high power efficiency of the HSM. This is because the linear amplifier should produce additional output current to cancel the amplified error current from the switching amplifier due to any error of current sensing [14]. One of the conventional current-sensing schemes is to use a current mirror technique by sharing the gate and source voltages between the main output devices and a sensing device with an $N : 1$ ratio [13], [16]. Small output resistance r_o in 65-nm devices, however, makes it difficult to accurately replicate the current because a V_{DS} difference between the main and sensing devices causes unacceptable error. Current sensing with local feedback is a possible alternative in long channel devices [14]. However, it requires three amplifiers: two rail-to-rail input-folded cascode amplifiers and another transimpedance amplifier.

The presented current-sensing circuit shown in Fig. 11(a) utilizes an amplifier A_{SENSE} and a feedback resistor R_S . With this structure, it guarantees the same V_{DS} between the main and sensing devices by maintaining V_{out} and V_{outs} at the same potential, which eliminates the error regardless of the small r_o in 65-nm devices. This results in accurate current sensing with a 50:1 ratio, and the copied current induces a voltage drop across R_S . With the use of a 50-dB open-loop gain rail-to-rail input-output-swing Class-AB amplifier for A_{SENSE} , the feedback loop has a bandwidth of 75 MHz. A 1-kΩ resistor for R_S is chosen to have a 26 dB of current-sensing gain A_S . To see the efficacy of the presented current-sensing circuit, the HSM is simulated with three different DC inputs, 0.2, 0.6, and 1 V, and the output current of the linear

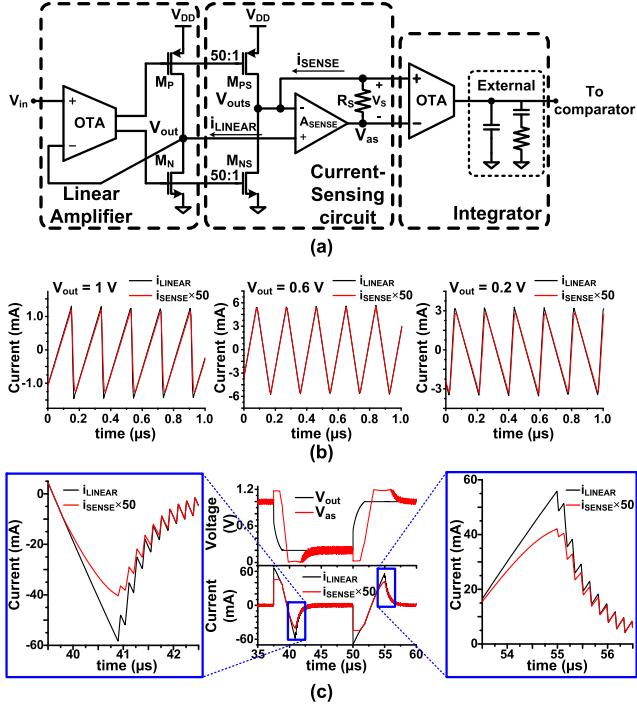


Fig. 11. (a) Proposed current-sensing circuit and an integrator in the switching amplifier. (b) Simulated output current of the linear amplifier and fiftyfold sensed current with three different DC inputs applied to the HSM. (c) Simulated voltage and current waveforms when a pulse signal varying from 0.2 to 1 V are applied to the presented HSM.

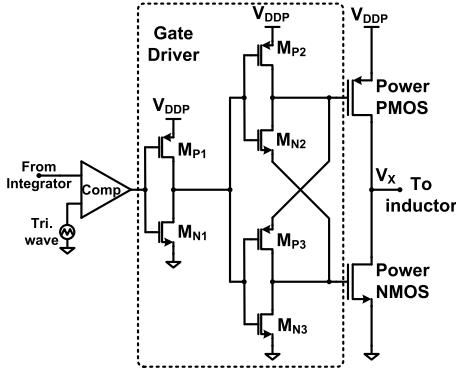


Fig. 12. Open-loop dead-time control gate driver.

amplifier is overlaid with the 50 times amplified sensed current in Fig. 11(b). As shown, the amplified sensed currents closely follow the output current waveforms of the linear amplifier at three different DC bias cases of V_{out} while consuming $240\text{-}\mu\text{A}$ static current from a 1.2-V supply. However, when the current-sensing circuit receives greater than $200\text{ }\mu\text{A}$ to sense 10 mA of current at supply rails such as 0.2 or 1 V of V_{out} , due to a large voltage drop across R_S , the A_{SENSE} amplifier may saturate and generate a certain amount of error. This phenomenon happens when the HSM receives a pulse signal varying from 0.2 to 1 V as an input, as shown in Fig. 11(c).

B. DC-DC Conversion Circuits

The sensed voltage, V_s in Fig. 11(a), is the input signal of the integrator which is composed of a rail-to-rail

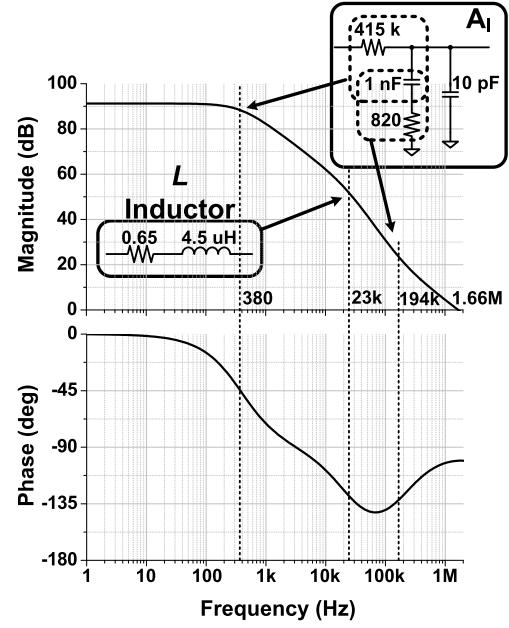


Fig. 13. Simulated frequency response of the current feedback.

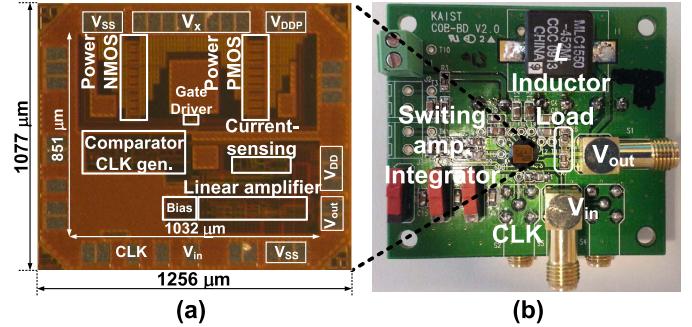


Fig. 14. (a) Chip micrograph. (b) PCB for measurement.

input-folded cascode amplifier, external compensation capacitors, and a resistor. The low frequency gain of the amplifier is 53 dB for high current-loop gain to help reduce the output current of the linear amplifier. The integrator is designed to consume 0.6 mA from a 1.2-V supply. Values of the external components are detailed in Section IV-C.

The output voltage of the integrator is compared with a triangular waveform signal, as shown in Fig. 12. The triangular waveform signal is internally generated with two windowing comparators for upper and lower limits of the triangular waveform and a switched current source/sink. The comparator shown in Fig. 12 employs a conventional cross-coupled hysteresis structure [10] for less than 7 ns of decision delay with $160\text{ }\mu\text{A}$ of static current consumption with a 1.2-V supply.

The important roles of the gate driver for the main power PMOS and NMOS devices of the switching amplifier are as follows: 1) short-circuit currents through main power PMOS and NMOS at the switching transient should be minimized; 2) short-circuit currents through the gate driver itself also need to be removed; and 3) given the temporal performance (propagation time and rising/falling time) between different

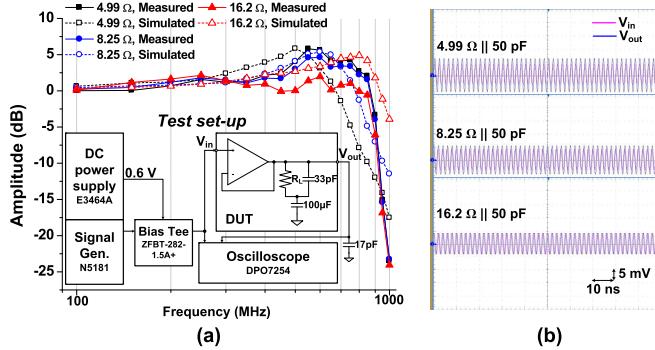


Fig. 15. Small-signal 3-dB bandwidth of the linear amplifier. (a) Simulation and measurement results with three different load conditions and the test set-up. (b) Measured input and output waveforms at 500-MHz small-signal.

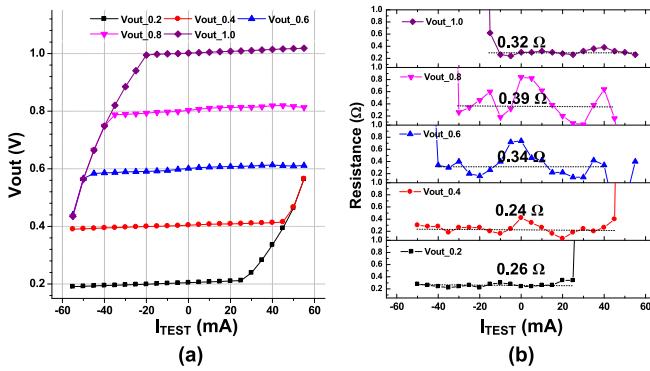


Fig. 16. DC output-impedance measurement with an external current source (Keithley 2400). (a) Measured output voltages across various I_{TEST} with five different DC bias conditions. (b) Output resistance.

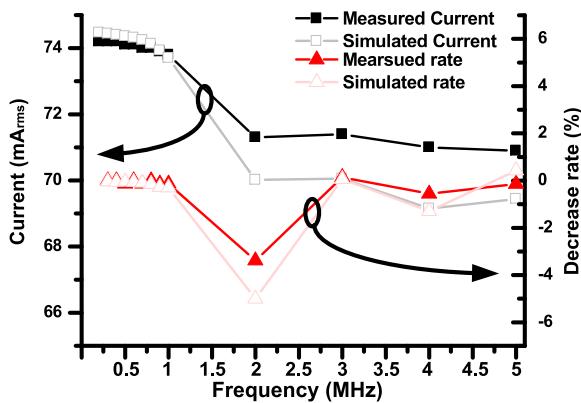


Fig. 17. Simulated and measured rms value of the inductor current and decrease rates.

architectures for the gate driver, the simplest architecture is more favourable. To meet all three of the requirements simultaneously, an open-loop dead-time control gate driver shown in Fig. 12 is proposed. Owing to its simple implementation, the size of the gate driver becomes small, as shown in Fig. 14(a).

C. Current-Loop Design

It is advantageous for the efficient switching amplifier to provide current to follow low frequency signals since most of

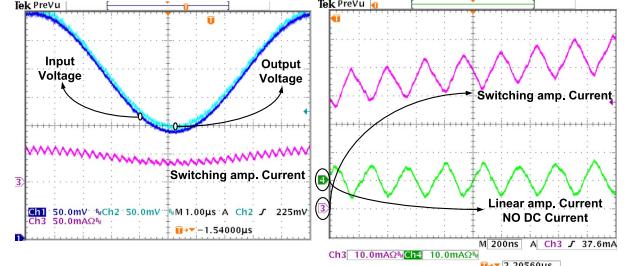
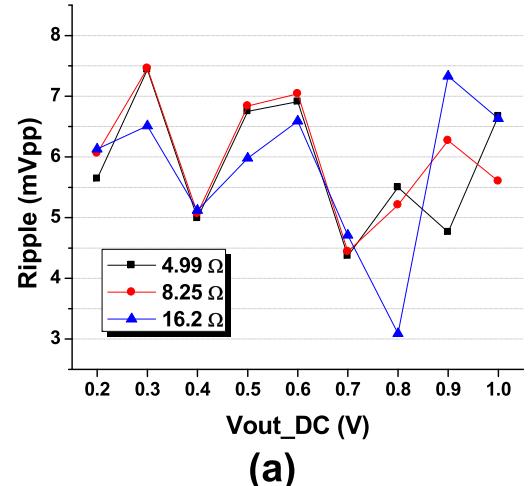


Fig. 18. Measured waveforms of the input and output voltages with currents. Ripple current from the switching amplifier is canceled by the current provided by the linear amplifier.



Voltage waveforms of V_X (upper) and V_{out} (lower)

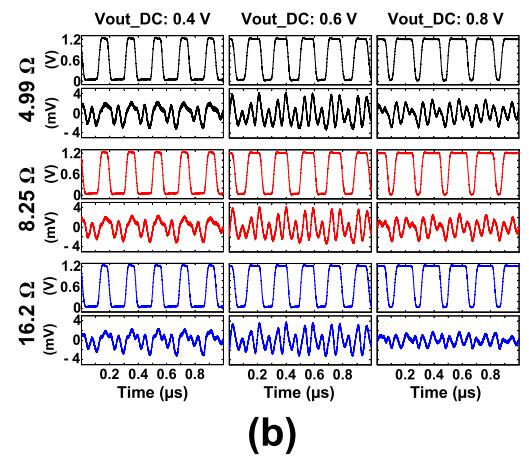


Fig. 19. (a) Measured output ripple peak-to-peak voltage at V_{out} for different load conditions. (b) Measured voltage waveforms for V_X (output of power MOSFETs) and AC-coupled V_{out} .

the signal energy for OFDM is concentrated at low frequency, from DC to 250 kHz. As such, a 20 dB of current-loop gain up to 250 kHz is targeted, given a switching frequency of 6 MHz. Furthermore, considering the slew rate limitations, the inductor value is determined by [31]

$$L \leq \frac{R_L}{2\pi f_{\text{target}}} \sqrt{\left(\frac{V_{DD}}{v_a}\right)^2 - 1} \quad (7)$$

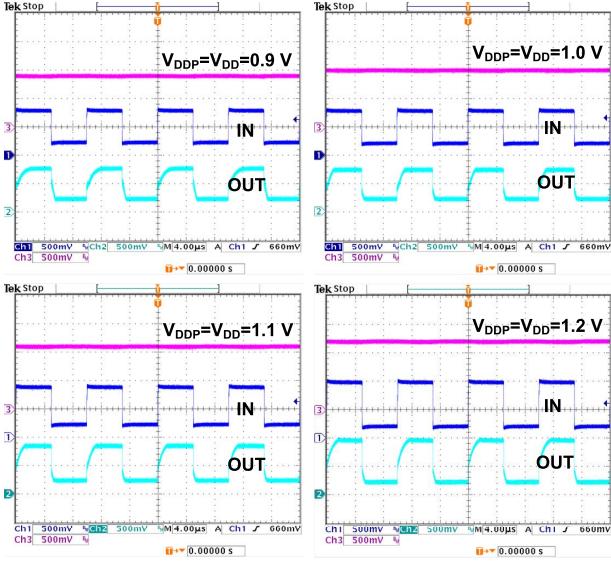


Fig. 20. Measured step responses with V_{DD} and V_{DDP} swept from 0.9 to 1.2 V.

where f_{target} is the target frequency and v_a is the signal amplitude at f_{target} . For a 800 mV_{PP} voltage swing at 250 kHz, 4.5 μH of inductance provides sufficient margin. With the net parasitic resistance of the inductor and printed circuit board (PCB) traces amounting to approximately 0.05 Ω , the power transistors are designed with a 0.3 Ω of R_{ON} resistance. Since the measured R_{oa} is 0.3 Ω (Fig. 16) at DC, 3 dB of current-loop gain is obtained from the inductor path. With 26 dB of A_S , 53 dB of A_I , and 9 dB of A_M , the DC gain becomes 91 dB. The simulated frequency response of the designed current feedback loop is shown in Fig. 13. With an external 1 nF capacitor and equivalent output resistance of 415 k Ω , the integrator has a dominant pole at 380 Hz. In addition, inductor series resistance and other resistances, such as DCR, R_{ON} and $R_L \parallel R_{\text{oa}}$, introduce a second pole at 23 kHz. Even with the two poles in the loop, the PM of the current feedback is over 75° owing to the insertion of a compensation zero by a series resistance, 820 Ω . This compensation zero is located at around 200 kHz, and the UGB of the loop is 1.66 MHz.

V. SIMULATION AND MEASUREMENT RESULTS

Fig. 14(a) shows the chip micrograph of the presented HSM. To minimize parasitic resistance and inductance at the output node of the linear amplifier and power MOSFETs, the outputs of the linear amplifier and power MOSFETs are located in close proximity to the pads. Furthermore, several pads are allocated to important nodes such as V_x , V_{out} , and power supplies. To minimize the effect of the switching noise to the linear amplifier, power rails between the switching and linear amplifiers are separated in the chip layout. The chip was fabricated in a 65-nm CMOS process and occupies 1.35 mm². For the wide bandwidth measurement, the chip was directly attached and bonded to the test PCB, as shown in Fig. 14(b). In order to accurately measure the input signal as it is received by the chip-on-board, two SMA connectors

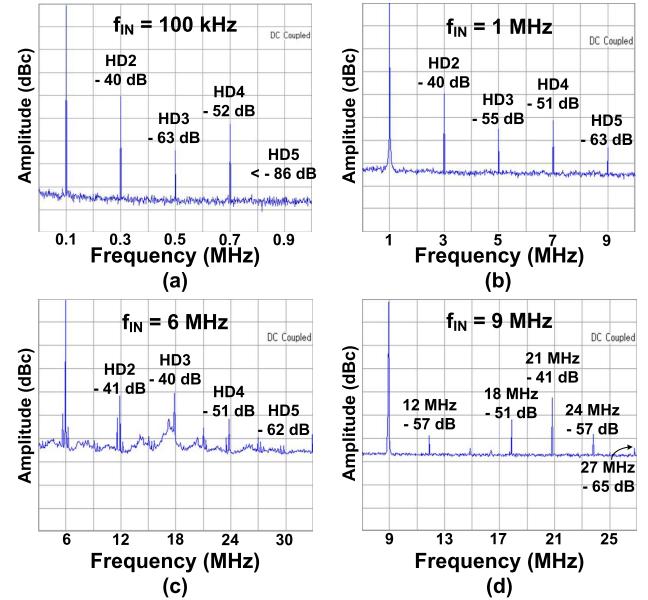


Fig. 21. Measured output spectra when a 0.8-V peak-to-peak sinusoidal input is applied to the HSM at various frequencies. (a) 0.1 MHz. (b) 1 MHz. (c) 6 MHz (close to switching frequency). (d) 9 MHz.

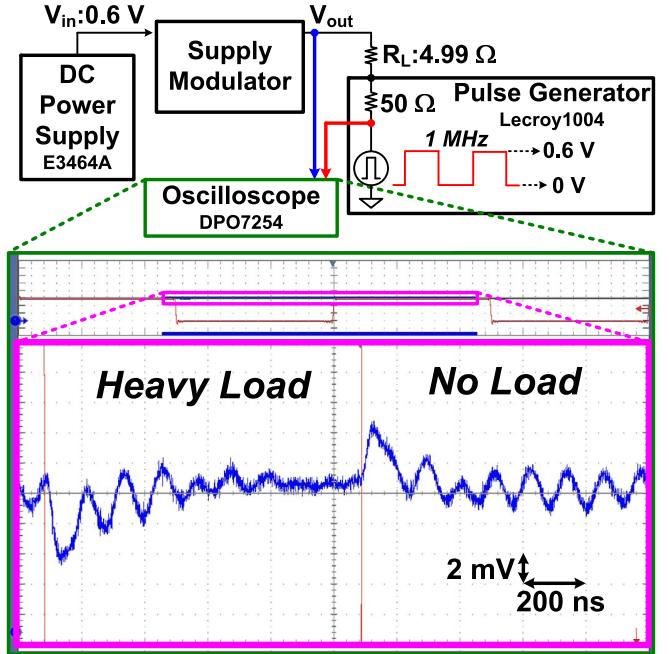


Fig. 22. Measured a load regulation characteristic showing less than 4-mV over- and undershoot.

for V_{in} are soldered into the PCB near the chip. An inductor MLC1550-452ML is chosen for L with less than 10 m Ω of DC resistance (DCR) and 34 MHz of self-resonant frequency, enabling wider loop bandwidth of the current loop and better efficiency of the HSM.

To characterize the linear amplifier (Figs. 15 and 16) isolated from the other circuits, the inductor L is de-soldered from the PCB while a 100- μF capacitor is inserted in series with the load resistance. This series capacitor emulates an open-load condition at DC and has no effect on the high frequency ($\gg 1$ kHz) characteristics.

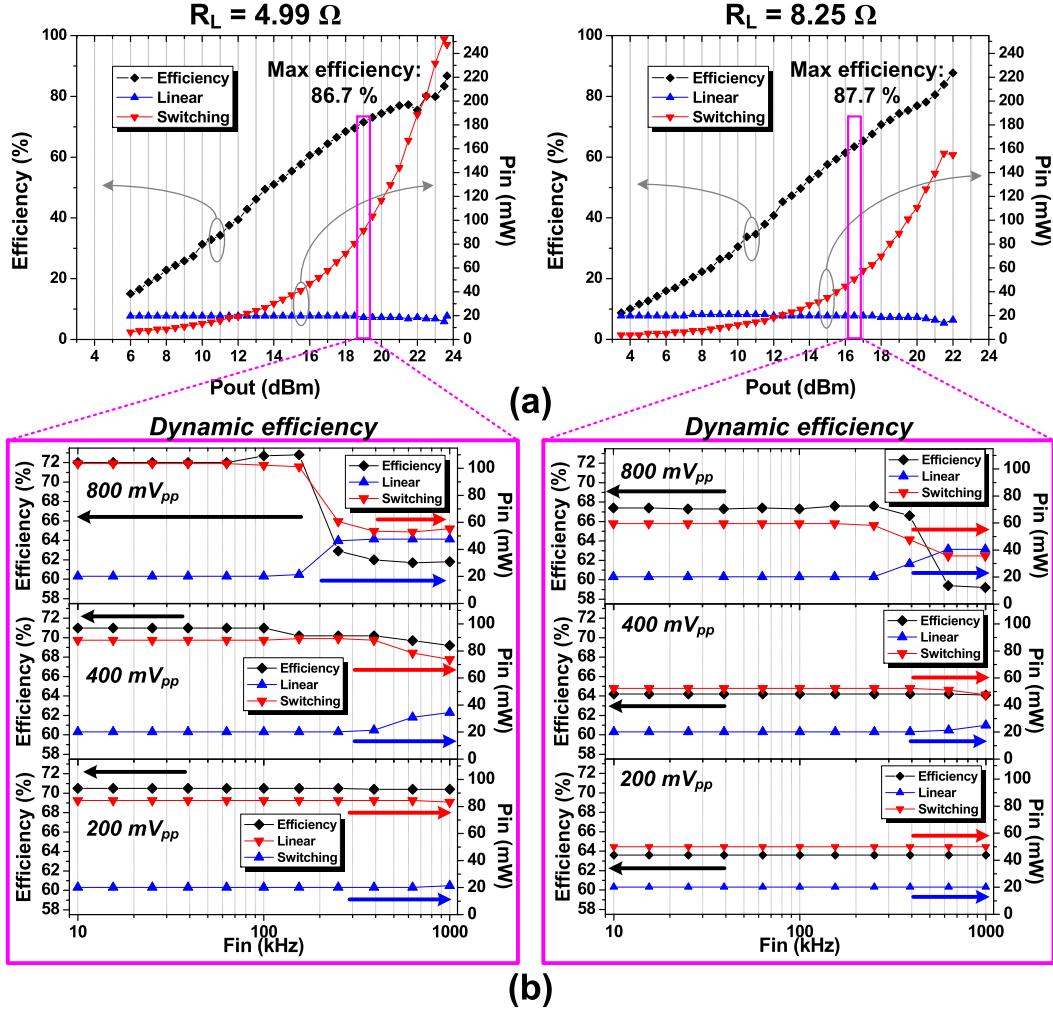


Fig. 23. Measured input powers to the non-switching and switching blocks and efficiency of the HSM showing 87.7% of peak efficiency with a 4.99- and a 8.25- Ω loads, when an input is (a) DC signal for the static efficiency and (b) sine-wave signal for the dynamic efficiency.

A 3-dB small-signal bandwidth is measured across three different load conditions: 4.99, 8.25, and 16.2 Ω with a 50-pF capacitance in parallel for all three cases. The transfer function from 100 MHz to 1 GHz is shown in Fig. 15(a). A signal generator provides a 5-mV amplitude of AC input voltage at 600-mV DC voltage through a bias tee. We observed feedback from the output V_{out} to the input V_{in} due to parasitic coupling, especially in the case when the phase difference between them is significant. As such, both V_{in} and V_{out} are measured simultaneously to determine the gain accurately. Fig. 15(b) shows measured V_{in} and V_{out} waveforms at 500 MHz.

The output resistance and current driving capability of the linear amplifier are measured by inserting a DC test current I_{TEST} to V_{out} while measuring V_{out} with five different DC voltage inputs at V_{in} (thereby, five different V_{out} conditions). As shown in Fig. 16(a), the linear amplifier has proved to be better at current sinking for high DC input voltages, and better at current sourcing for low DC input voltages. The output resistance of the linear amplifier is directly obtained by calculating the ratio of voltage difference at V_{out} to current difference at I_{TEST} for each current step as depicted in Fig. 16(b). The average resistance within

the normal operation range (dotted line) is shown in each panel. The switching amplifier is designed to provide a signal current ranging from DC to 1.68 MHz, which is the UGB of the current feedback loop. To measure the current-loop bandwidth, the root-mean-square (rms) output currents of the switching amplifier driving a 8.25- Ω load was measured while a sinusoidal AC signal centered at 0.6 V with a 50-mV amplitude across various frequencies was applied to the input of the HSM. The measured currents are shown in Fig. 17 along with the simulation results. The amount of the current provided by the switching amplifier through the inductor begins to decrease at a few 100 kHz because of the insufficient current-loop gain at these frequencies, and more rapidly between 1- and 2-MHz consistent with the designed bandwidth (Section II).

As shown in Fig. 18, the linear amplifier cancels the switching ripple current by providing an out-of-phase current of the switching amplifier current with a negligible low-frequency current signal, substantially reducing the voltage ripple. The results shown confirm that the proposed current-sensing circuit works well without producing noticeable offset, which improves the power efficiency of the HSM by removing

TABLE I
COMPARISON OF STATE-OF-THE-ART SUPPLY MODULATORS

	Kitchen JSSC [8]	Pinon ISSCC [9]	Sung PE [11]	Kwak JSSC [13]	Shrestha JSSC [16]	Hassan ISSCC [17]	Liu ISSCC [18]	Tan JSSC [21]	This Work
Structure	LDO/ Switching	Switching	Dual switching	HSM	HSM	HSM	HSM	HSM	HSM
V _{DD} (V)	3.3/3.6	2.9~4.3	3.3	3.5	1.2	5.5	2.4	1.2	1.2
Max power (dBm)	30.8	33	30	33.5	22.7	28.3	29	23	23.6
Switching frequency (MHz)	10	130	2, 110	2	118	N.R.	25	50	6
Inductor (μH)	5.3	0.11	4.7, 0.051	4.7, 1	0.08	1, 0.3	0.2	0.1	4.5
Max efficiency (%)	75.5	83	86.5 ^a	88.3	87.5	83 ^b	88.7 ^b	88.3	87.7
3 dB small signal bandwidth (MHz)	4	15	40	10	285	N.R.	69.2	Not measured ^c	500 – 850 ^d
MAX ripple voltage (mV _{pp})	N.R.	N.R.	N.R.	12	12.1 ^e	N.R.	N.R.	8	7.5
Process	0.25 μm CMOS	0.25 μm BiCMOS	180 nm CMOS	0.35 μm CMOS	65 nm CMOS	180 nm CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS

^ameasured with a 2.62 V_{rms} signal

^bmeasured with a 20 MHz LTE envelop signal

^csimulated unity-gain-bandwidth 700 MHz with a 5 Ω || 2 pF load.

^d500 MHz measured at 4.99 Ω || 50 pF load, 850 MHz measured at 16.2 Ω || 50 pF load.

^emeasured ripple voltage 4.3 mV_{rms} at switching frequency

the need of an additional DC current provided by the linear amplifier.

To accurately characterize the ripple voltage, V_{out} was directly measured for various input voltages at V_{in} (thereby, various output voltages V_{out}) from 0.2 to 1 V and three different load conditions, as presented in Fig. 19(a). The ripple voltage shows no significant dependence on the load condition, which implies that the output resistance of the linear amplifier at 6-MHz switching frequency stays firm across three load conditions. Fig. 19(b) shows voltage waveforms of V_X and AC-coupled V_{out} at three different load conditions. The maximum ripple voltage is 7.5 mV_{pp} at 0.3 V of V_{out} and 8.25- Ω load condition.

Fig. 20 demonstrates robust operation of the HSM from 0.9 to 1.2 V of supply voltage with a 4.99- Ω load owing to the proposed BS-Class-AB bias scheme for low-voltage operation. The input and output voltages range from 0.2 V to $V_{\text{DD}} - 0.2$ V. Rise and fall times are less than 2 μs , mainly due to the slew rate limits from the inductor in the switching amplifier according to (7).

Full swing (0.8-V peak-to-peak) sinusoidal waveforms at various frequencies were applied to the HSM with a 4.99- Ω load in order to measure the harmonic distortion using a spectrum analyzer (SA) (Keysight, E4445A). A wide bandwidth (DC–2 GHz, two cascaded HAT-20+) 40-dB attenuator was connected to the input of the SA for SA protection. As presented in Fig. 21(a), for a 100-kHz input signal, the fundamental tone was measured at –38 dBm while other harmonic tones were less than –40 dBc compared to the fundamental tone. At a 1-MHz full swing input signal Fig. 21(b), a fundamental tone was measured at –38.1 dBm. Harmonic distortion was

measured less than –40 dBc. As expected, in the case that the switching frequency and the input signal were spectrally close to each other, the output spectrum contained several tones surrounding the harmonics of the –38.8-dBm fundamental tone, as well as noise floor fluctuations, as shown in Fig. 21(c). With input signal at 9 MHz far higher than the current-loop bandwidth, the HSM drives a 4.99- Ω load with less than 3-dB loss. As shown in Fig. 21(d), tones from the 6-MHz switching frequency f_{sw} are also clearly visible at 12, 18, and 24 MHz. Note that the fundamental signal tone and tones from switching noise generate inter-modulation distortion at 21 MHz ($2 \times f_{\text{sw}} + f_{\text{in}}$). However, owing to the high-gain wide bandwidth linear amplifier, any distortion from the HSM is far below the fundamental signal tone (≥ 40 dBc).

The load regulation is characterized in Fig. 22 by measuring the output voltage V_{out} , when the switching load varies from 54.99 Ω to an open. A DC signal of 0.6 V is applied as the input voltage to the HSM, connected to 4.99 Ω of R_L . To make a non-linear switching load, the other node of R_L is not grounded, but, instead, connected to a pulse generator (LeCroy, ArbStudio 1004) producing a 1 MHz, 0-, and 0.6-V pulse signal. As such, when the pulse is 0.6 V, the HSM sees no load (open). Owing to the proposed compensation and the loop analyses, the voltage and current loops are stable and robust to the non-linear load. Measured undershoot and overshoot are less than 4 mV.

Fig. 23(a) and (b) shows the static and dynamic efficiencies of the HSM and the input power to each amplifier. (Switching amplifier including all digital switching logic and linear amplifier including all static circuits.) The static efficiencies are measured by changing an input DC voltage

(and thereby, changing V_{out}) under load conditions of either 4.99 or 8.25 Ω . Maximum power provided by the presented HSM is 23.65 dBm for a 4.99- Ω load, and peak efficiency is 87.7% for a 8.25- Ω load. As expected, the input power to the switching amplifier increases with P_{out} , confirming that the switching amplifier supplies the dominant portion of the required power to drive the load. Because of the high PAPR, most PAs in transmitters frequently operate far below their maximum output power, resulting in the HSM operating far below its maximum output power. Therefore, efficiency in low-power regions such as 12–14 dBm is also important. At 10-dB back-off, and at 13.6 dBm for a 4.99- Ω load and 12 dBm for a 8.25- Ω load, efficiencies are about 50% and 41%, respectively. This design achieves 10% improvement in 10-dB back-off efficiency compared to [16] using a 5.3- Ω load, while achieving similar 10-dB back-off efficiency compared to [21] using a 5- Ω load. The dynamic efficiencies of the HSM are measured with an input of three different sinusoidal signals centered at 0.6 V with varying amplitudes (200, 400, and 800 mV_{PP}), by changing the frequency of the input signal. As expected, when the input is a high-speed sine-wave with large amplitude, the linear amplifier assists to develop the output voltage at the expense of a decrease in efficiency.

Table I summarizes the measured performance of this paper in comparison with the state-of-the-art in supply modulator designs reported in the literature. While a combined switching and linear regulator in series and a stand-alone switching regulator shows less than 83% peak efficiency, all HSMs in the table report peak efficiencies greater than 83%. The presented HSM has a measured small-signal bandwidth greater than a 500 MHz at three different load conditions while guaranteeing less than 7.5-mV_{PP} ripple voltages across all DC output voltages.

VI. CONCLUSION

In this paper, a HSM with a 500-MHz bandwidth linear amplifier for polar transmitters was presented. In order to accurately design the current loop in the switching amplifier such that the current-loop bandwidth given the switching frequency is widened with sufficient PM, we offered an analysis of the current feedback mechanism in a supply modulator, introducing an equivalent separation of the loop or analysis. In addition, a wide bandwidth linear amplifier utilizing PFB and NFB, a current-sensing circuit, and an open-loop dead-time control gate driver for a HSM were presented. The proposed linear amplifier offers a 3-dB bandwidth of 500 MHz and operates at a 0.9 –1.2 V supply with a BS-Class-AB bias scheme in 65-nm CMOS. The analysis of the frequency response for the linear amplifier proves that a buffer used in the BS-Class-AB reduces power consumption and improves the PM. The linear amplifier cancels the ripple current without

supplying low frequency current significantly owing to the proposed current-sensing circuit. The measured peak-to-peak ripple voltage is less than 7.5 mV_{PP}. Peak efficiency is measured to be 87.7% while the 10-dB back-off efficiency is greater than 40%.

APPENDIX

A. Analysis of the Positive Feedback Loop

The mechanism of PFB shown in Fig. 6 is detailed by numerical formula. If the gain of the source follower M_4 is unity, then the gain from node A to node D becomes

$$-\frac{R_D}{\frac{1}{g_{m3}} + r_{o1}} \times \frac{1}{1 + g_{m1}R_D} \approx -\frac{1}{\frac{g_{m1}}{g_{m3}} + g_{m1}r_{o1}} \quad (8)$$

where R_D is the open-loop impedance of node D [26]. Negative gain means that the voltage of node D decreases when the voltage of node A increases. The lowered voltage of node D results in a decrease in M_2 current. The amount of variation in current Δi_{PFB} is expressed by

$$\Delta i_{\text{PFB}} = -\frac{g_{m2}\Delta v}{\frac{g_{m1}}{g_{m3}} + g_{m1}r_{o1}} \quad (9)$$

where Δv is the voltage variation of node A. Then, the impedance of the node A is equal to

$$R_{A_PFB} = \frac{\Delta v}{\Delta i} = \frac{\Delta v}{\Delta i_{\text{PFB}} + \Delta i_{r_{o2}}} \quad (10)$$

where $\Delta i_{r_{o2}}$ is the variation in current through r_o , $\Delta v/r_{o2}$. From (9) and (10), the impedance of node A becomes

$$R_{A_PFB} = \frac{\left(\frac{g_{m1}}{g_{m3}} + g_{m1}r_{o1}\right)r_{o2}}{\frac{g_{m1}}{g_{m3}} + g_{m1}r_{o1} - g_{m2}r_{o2}}. \quad (11)$$

By controlling $g_{m1}r_{o1}$ and $g_{m2}r_{o2}$ for accounting for the term, g_{m1}/g_{m3} , at least in theory, R_{A_PFB} is able to be infinity.

B. Analysis of Compensation for the Linear Amplifier

The g_3 and C_3 are the equivalent conductance and capacitance at the output node V_{out} which are given in Fig. 7 by $g_3 = g_{M4P} + g_{M4N} + g_{\text{load}}$ and $C_3 = C_{\text{par3}} + C_{\text{load}}$, where C_{par3} models the parasitics in the third stage. C_{m1} and C_{m2} represent compensation capacitors. Here, C_1 , the parasitic capacitance at the output of the first stage, is ignored since it does not seriously affect the transfer function compared to the Miller capacitor C_{m1} . The open-loop gain transfer function of this three-stage amplifier can be given by (12), as shown at the bottom of this page, with DC gain $A_{DC} = g_{m1}g_{m2}g_{m3}/g_{1g2g_3}$ and dominant pole $w_d = g_{1g2g_3}/C_{m1}g_{m2}g_{m3}$.

From the denominator of (12), the natural frequency w_n and damping factor ζ are given by

$$w_n = \sqrt{\frac{g_{m2}g_{m3}}{C_3(C_{m2} + C_2)}} \quad (13)$$

$$A_v(s) = \frac{g_{m1}g_{m2}g_{m3}}{g_{1g2g_3} + sC_{m1}g_{m2}g_{m3}} \times \frac{g_{m2}g_{m3} - s(C_{m2}g_{m2} + C_{m1}g_{m2}) - s^2C_{m1}(C_2 + C_{m2})}{g_{m2}g_{m3} + s(C_{m2}(g_3 + g_{m3} - g_{m2}) + C_2g_3 + C_3g_2) + s^2C_3(C_{m2} + C_2)} \quad (12)$$

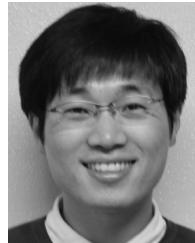
and

$$\zeta = \frac{C_{m2}(g_3 + g_{m3} - g_{m2}) + C_2 g_3 + C_3 g_2}{\sqrt{4g_m g_{m3}} C_3 (C_{m2} + C_2)}. \quad (14)$$

With the reasonable assumption in this design that $C_2(4g_3 + 3g_{m3} - 3g_{m2}) \gg C_3 g_2$, and $4g_3 + 3g_{m3} \gg 3g_{m2}$ and the fact that C_{m2} is chosen to be three times larger than C_2 [30], the natural frequency and damping factor are simplified as in (4) and (5).

REFERENCES

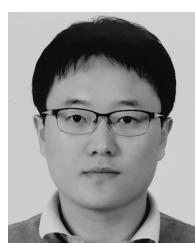
- [1] D. Chowdhury, L. Ye, E. Alon, and A. Niknejad, "An efficient mixed-signal 2.4-GHz polar power amplifier in 65-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1796–1809, Aug. 2011.
- [2] F. Wang, D. F. Kimball, D. Y. Lie, P. M. Asbeck, and L. E. Larson, "A monolithic high-efficiency 2.4-GHz 20-dBm SiGe BiCMOS envelope-tracking OFDM power amplifier," *IEEE J. Solid-State Circuits*, vol. 42, no. 6, pp. 1271–1281, Jun. 2007.
- [3] P. Reynaert and M. S. J. Steyaert, "A 1.75-GHz polar modulated CMOS RF power amplifier for GSM-EDGE," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2598–2608, Dec. 2005.
- [4] Y. Li *et al.*, "Circuits and system design of RF polar transmitters using envelope-tracking and SiGe power amplifiers for mobile WiMAX," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 5, pp. 893–901, May 2011.
- [5] J. S. Walling and D. J. Allstot, "Linearizing CMOS switching power amplifiers using supply regulators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 7, pp. 497–501, Jul. 2010.
- [6] J. S. Walling and D. J. Allstot, "Design considerations for supply modulated EER power amplifiers," in *Proc. WAMICON*, Apr. 2013, pp. 1–4.
- [7] F. Wang *et al.*, "Wideband envelope elimination and restoration power amplifier with high efficiency wideband envelope amplifier for WLAN 802.11g applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2005, pp. 645–648.
- [8] J. N. Kitchen, C. Chu, S. Kiaei, and B. Bakkaloglu, "Combined linear and Δ -modulated switch-mode PA supply modulator for polar transmitters," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 404–413, Feb. 2009.
- [9] V. Pinon, F. Hasbani, A. Giry, D. Pache, and C. Garnier, "A single-chip WCDMA envelope reconstruction LDMOS PA with 130 MHz switched-mode power supply," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2008, pp. 564–636.
- [10] M. Hassan, L. E. Larson, V. W. Leung, and P. M. Asbeck, "A combined series-parallel hybrid envelope amplifier for envelope tracking mobile terminal RF power amplifier applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. 1185–1198, May 2012.
- [11] S. Sung *et al.*, "Envelope modulator for 1.5-W 10-MHz LTE PA without AC coupling capacitor achieving 86.5% peak efficiency," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8282–8292, Dec. 2016.
- [12] A. Zai, D. Li, S. Schafer, and Z. Popovic, "High-efficiency X-band MMIC GaN power amplifiers with supply modulation," in *IEEE MTT-S Int. Microw. Symp. (IMS)*, Jun. 2014, pp. 1–4.
- [13] T. W. Kwak, M. C. Lee, and G. H. Cho, "A 2 W CMOS hybrid switching amplitude modulator for EDGE polar transmitters," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2666–2676, Dec. 2007.
- [14] W. Y. Chu, B. Bakkaloglu, and S. Kiaei, "A 10 MHz bandwidth, 2 mV ripple PA regulator for CDMA transmitters," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2809–2819, Dec. 2008.
- [15] J. T. Stauth and S. R. Sanders, "Optimum biasing for parallel hybrid switching-linear regulators," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1978–1985, Sep. 2007.
- [16] R. Shrestha, R. V. D. Zee, A. D. Graauw, and B. Nauta, "A wideband supply modulator for 20 MHz RF bandwidth polar PAs in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1272–1280, Apr. 2009.
- [17] M. Hassan, P. M. Asbeck, and L. E. Larson, "A CMOS dual-switching power-supply modulator with 8% efficiency improvement for 20 MHz LTE envelope tracking RF power amplifiers," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 366–367.
- [18] X. Liu, H. Zhang, M. Zhao, X. Chen, P. K. T. Mok, and H. C. Luong, "A 2.4 V 23.9 dBm 35.7%-PAE -32.1dBc-ACLR LTE-20 MHz envelope-shaping-and-tracking system with a multiloop-controlled AC-coupling supply modulator and a mode-switching PA," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 38–39.
- [19] J.-S. Paek *et al.*, "A -137 dBm/Hz Noise, 82% efficiency AC-coupled hybrid supply modulator with integrated buck-boost converter," *IEEE J. Solid-State Circuits*, vol. 5, no. 11, pp. 2757–2768, Nov. 2016.
- [20] S. H. Yang *et al.*, "A single-inductor dual-output converter with linear-amplifier-driven cross regulation for prioritized energy-distribution control of envelope-tracking supply modulator," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 36–37.
- [21] M. Tan and W.-H. Ki, "An efficiency-enhanced hybrid supply modulator with single-capacitor current-integration control," *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 533–542, Feb. 2016.
- [22] J. J. Yan, C. Hsia, D. F. Kimball, and P. M. Asbeck, "Design of a 4-W envelope tracking power amplifier with more than one octave carrier bandwidth," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2298–2308, Oct. 2012.
- [23] M. Tan and W.-H. Ki, "A 100 MHz hybrid supply modulator with ripple-current-based PWM control," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 569–578, Feb. 2017.
- [24] C. Kim, C.-S. Chae, Y.-S. Yuk, Y.-G. Kim, J. K. Kwon, and G.-H. Cho, "A 105 dB-gain 500 MHz-bandwidth 0.1Ω-output-impedance amplifier for an amplitude modulator in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2010, pp. 88–89.
- [25] G.-H. Cho, *Analysis and Design of Electronic Circuits*. Seoul, South Korea: Hongrun Publishing Company, 2008.
- [26] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*. Oxford, U.K.: Oxford Univ. Press, 2004.
- [27] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. New York, NY, USA: Springer, 2001.
- [28] V. V. Ivanov and I. M. Filanovsky, *Operational Amplifier Speed and Accuracy Improvement*. Norwell, MA, USA: Kluwer, 2004.
- [29] K. Bult and G. J. G. M. Geelen, "A fast-settling CMOS op amp for SC circuits with 90-dB DC gain," *IEEE J. Solid-State Circuits*, vol. 25, no. 6, pp. 1379–1384, Dec. 1990.
- [30] W. M. Sansen, *Analog Design Essentials*. Secaucus, NJ, USA: Springer-Verlag, 2006.
- [31] N.-I. Kim, "An analog/digital mixed-mode high power audio amplifier with high efficiency and high fidelity," Ph.D. dissertation, School Elect. Eng., KAIST, Daejeon, South Korea, Dec. 2003. [Online]. Available: <https://library.kaist.ac.kr/search/catalogSearch/thesis/thesisList.do>



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