

A Digitally Controlled Fully Integrated Voltage Regulator With On-Die Solenoid Inductor With Planar Magnetic Core in 14-nm Tri-Gate CMOS

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Abstract—A fully integrated digitally controlled two-phase buck voltage regulator (VR) with on-die solenoid inductors with a planar magnetic core is demonstrated in 14-nm tri-gate CMOS for fine-grained power delivery/management domains of high power density in system-on-chips while enabling ultra-thin (z -height) packages. The VR achieves 1-A/mm² power density for 400-mA load current with a measured peak efficiency of 84% at 100-MHz switching frequency including a digital PWM with >9 bits (8 ps) of resolution.

Index Terms—Buck converter, DPWM, dual edge modulation DPWM, fully integrated voltage regulator, high frequency, high resolution digital controller, on-die solenoid inductor, planar magnetic core.

I. INTRODUCTION

FULLY integrated voltage regulators (IVRs) promise efficient and wide-range local power delivery and management capability with fast transient response for fine-grain dynamic voltage and frequency scaling (DVFS) domains of high power density in complex system-on-chips (SoCs). The tradeoff between having a platform regulator versus an on-die regulator to achieve best power savings is workload and application dependent. Furthermore the choice of on-die regulators be it switching or linear regulators could also be application specific. For example, a combination of external switching regulators and on-die linear regulators with bypass was reported in [1]. Higher dropout voltages result in lower overall efficiency but [1] reports overall power savings due to DVFS despite the low drop out losses. Fully on-die buck-based switching regulators (VRs) provide higher overall efficiency and power density across a wide range of voltages and currents. However, integration of high-quality power inductors

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that can support high current density with minimal losses is a major challenge.

Integrated buck VR designs with different types of power inductor integration technologies have been reported [2]–[4]. Fig. 1 shows a pictorial representation of the inductor state of the art and their relative co-location with the load die. In [2], planar lateral coupled power inductors with non-planar magnetic cores for higher inductance, quality factor, and current density, are integrated on a separate silicon interposer die which is then wire-bonded to the VR die on a common ball grid array laminate. While an interposer die for inductor integration enables small inductor footprint, parasitic impedances of the wire-bonds degrade inductor quality, overall VR performance, and efficiency. In addition, the total thickness (z -height) of the packaged two-die stack is too large for ultra-thin form factor systems. High quality-factor air-core power inductors are integrated within the package layers in [3], utilizing the thick package core. However, they are difficult to integrate in ultra-thin coreless packages with few package layers. Also, scalability of the inductor footprint to fine domains is limited. Furthermore, since the inductors cannot be co-located with the SoC DVFS domains for both of these inductor options, scalability to finer domains is curtailed. Planar lateral spiral inductors without magnetics are integrated directly on the VR die in [4], utilizing upper metal layers. Although this option is suitable for realizing ultra-thin packaged dies and the inductor footprint can be scaled to finer domains, the quality factor and inductance density are too low to support high current density needed for viable on-die power conversion.

In this paper, we demonstrate a fully integrated digitally controlled two-phase high frequency buck VR with on-die solenoid power inductors with multiple vertical windings around a high-permeability planar magnetic core, utilizing two thick-top metal layers, implemented in 14-nm tri-gate CMOS (Fig. 2). This inductor structure and on-die integration technology enable lower losses and higher current density than the on-die planar lateral spiral inductor without magnetics [4]. At the same time, it offers: 1) superior scalability of inductor footprint; 2) finer DVFS domains via inductor co-location with the domain; and 3) easier realization of ultra-thin

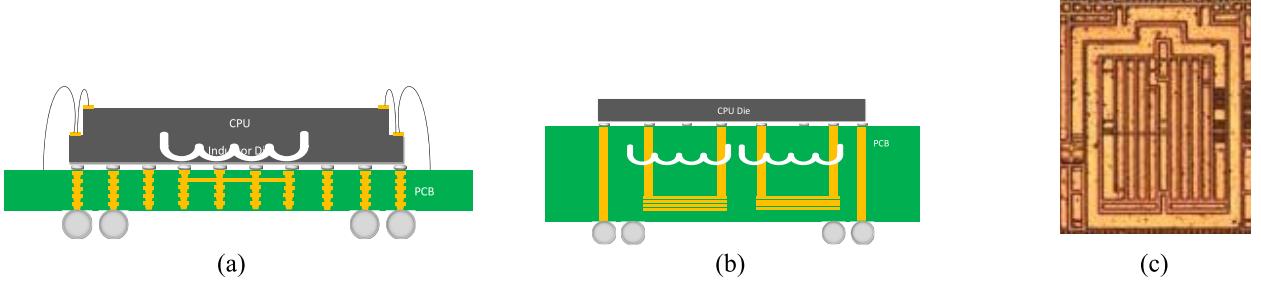


Fig. 1. Inductor state of the art. (a) Spiral inductors with integrated magnetics on interposer die. (b) In-package air core inductors. (c) On-die spiral inductors co-located with load.

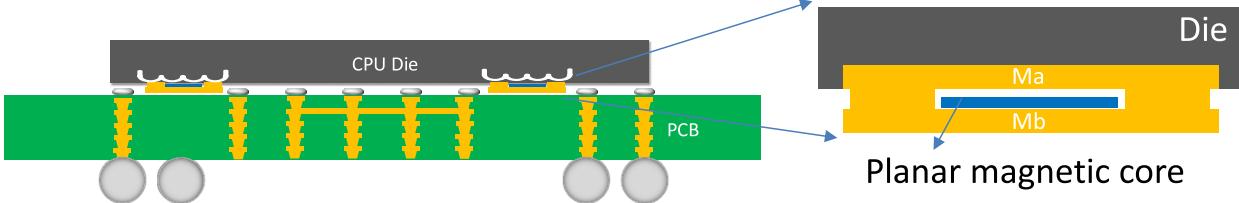


Fig. 2. Fully on-die solenoid inductor with planar magnetic core co-located with load.

packaged dies, compared to inductor technologies implemented in [2] and [3]. The digital VR controller enables easier reconfiguration, more efficient and synthesizable design with fine-grain distributed DVFS domains further enhancing scalability and portability across process nodes.

The rest of this paper is organized as follows: Section II details the solenoid inductor with planar magnetics and its associated design and modeling. Section III describes the architecture and design of the digitally controlled IVR. Section IV provides an in-depth detail of the digital pulse width modulation (PWM) architecture for synchronous high-accuracy oversampled systems. Section V presents the measurement setup with Section VI providing an overview of the silicon measurements, and Section VII concludes the paper by summarizing the key results.

II. MAGNETIC INDUCTOR DESIGN AND MODELING

Designing inductors with magnetics on a CMOS die are extremely challenging. The quality of the inductor is vital in achieving a high-efficiency high-density VR. For low-frequency IVRs the dc resistance is critical but for high switching frequency (50–250 MHz) IVRs both the dc and ac resistance determine overall efficiency. Furthermore in continuous conduction mode the inductance value determines the overall rms current through the FETs which can lead to significant impact on overall efficiency of the IVR. The co-location of the inductor with load, its structure, number of turns, presence of magnetics with single or multiple laminations, all present different optimization knobs on efficiency, power density, cost, and process complexity. The main objective in this paper is to adopt an inductor structure that is co-located with the load and provides high efficiency at high power density with minimal cost and process complexity.

Lateral spiral inductors can be co-located with the load and can be fully integrated in ultra-thin packages, [4] but the poor inductance density and large dc resistance make the approach unattractive for high-density loads. Spiral inductor structures with two layers of high-permeability magnetic material are discussed in [2]. Such a topology has been shown to demonstrate high inductance density and quality factor at relevant frequencies of the IVR. However, such a structure requires two sets of magnetic laminations adding to the overall cost and process complexity.

A vertical solenoid structure with magnetics has been demonstrated in [5]. Such a vertical solenoid structure is attractive as it forms the winding layers around a planar magnetic core. Reference [5] employs several layers of magnetic laminations to lower eddy current losses and demonstrates a Q of 17 for a 4-nH inductor at 100 MHz which could lead to high IVR efficiencies. However, the cost and process complexity implications of multiple laminations could make such a structure impractical for high volume manufacturing on advanced process nodes.

The on-die solenoid inductor (Fig. 2) designed in this paper is a vertical solenoid with multiple vertical turns around a high-permeability planar magnetic core utilizing two thick-top metal layers Ma ($6 \mu\text{m}$) and Mb ($12 \mu\text{m}$). A single lamination magnetic core is used to balance process complexity with inductance density as compared to structures in [2], [4], and [5]. The total thickness of the magnetic material that forms the inductor core is limited by practical constraints such as those arising from film stress and patterning requirements. With a given area constraint for density (0.15 mm^2 in our case), the solenoid inductor structure leads to a tradeoff between the number of turns and the width of each turn. With perfect coupling between the turns of the inductor, the inductance increases as N^2 , while the dc resistance only

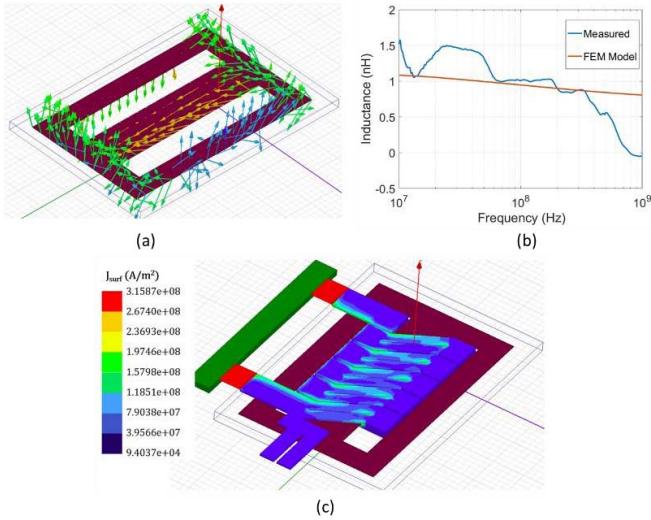


Fig. 3. Inductor modeling results from high frequency structure simulator. (a) H-field lines in inductor FEM model. (b) Comparison of inductance from FEM simulation and measurement versus frequency. (c) Current density plot of the inductor at 100 MHz.

increases linearly with N , where N is the number of turns. However, increasing the number of turns also leads to a lower self-resonant frequency for the inductor, which limits the operating frequency of the converter. A lower value of N allows for wider turns and lower dc resistance, but at large operating frequencies, the ac resistance of the inductor is limited by skin and proximity effects. A five turn solenoid inductor is designed in the given area constraint to maximize inductance, while minimizing dc resistance with appropriate trace widths for optimal coupling between the windings.

Since the material that forms the magnetic core is thin and anisotropic, the magnetic flux lines generated by a current passing through the inductor do not complete the loop inside the core. This makes purely analytical, reluctance-based models infeasible, and necessitates the use of a 3-D finite-element modeling (FEM) tool to model the inductor. An H-field vector plot for the inductor is shown in Fig. 3(a).

A comparison of the inductance obtained from the FEM simulation versus the measured inductance across frequency is shown in Fig. 3(b). The model predicts the inductance to within reasonable accuracy for the desired frequency range. However, since the model does not account for frequency dependent saturation effects, the matching between simulation and measurement degrades at higher frequencies. The current density in the inductor winding at 100 MHz is shown in Fig. 3(c). As expected, the ac resistance is limited by skin and proximity effects.

III. DIGITALLY CONTROLLED INTEGRATED BUCK CONVERTER

Despite their excellent bandwidth and infinite resolution PWM capabilities, analog controllers do not scale well with process generations. Furthermore high-speed analog design on digitally tuned processes is extremely challenging. Digital controllers on the other hand provide scalability, programmability, easier reconfiguration, and portability across process nodes which can significantly improve time to market on advanced

sub-micrometer process nodes. Moreover in recent years, digital controllers have demonstrated viability and feasibility for high switching frequency IVRs and coupled with the ease of accommodating multiple modes, digital controllers are becoming a very attractive choice for fine-grained power delivery [4].

Fig. 4 shows the functional block diagram of the digitally controlled fully on-die buck VR. A two-phase power train with a programmable dead time generator switching at 100 MHz is implemented. A fully on-die vertical solenoid inductor with a planar magnetic core as described in Section II is implemented using two thick metal layers Ma and Mb. The same VR with external discrete inductors embedded in the membrane probe card [Fig. 9(b)], in place of on-die inductors, is also implemented for meaningful comparisons. A windowed flash ADC samples the output voltage at 400 MHz and generates a digital error $e[k]$, which is fed into a classic Type-III controller to generate a duty cycle word $d[k]$. The digital PWM block takes the duty cycle word and generates the PWM pulses for the two-phase power train. More details on each block are provided in the following sections.

A. Power Train Design

High frequency on-die buck VRs bring with them a particular set of tradeoffs and challenges, namely, as follows.

- 1) The benefit of routing a higher voltage into the die and reducing the current density in the package proportionally.
- 2) High-frequency operation that is both, enabled and demanded, by the small-valued on-die passives.
- 3) Low-voltage nominal CMOS transistors that can ease integration yet require careful design and optimization. Consequently, the buck VR power stage (Fig. 1) consists of: 1) cascode power switches to support VR input voltage as high as $2 V_{max}$; 2) 16 modular slices that are optimally enabled/disabled in binary multiples to maximize conversion efficiency across a wide range of load currents; and 3) a layout that is carefully drawn to minimize the skew between the high-side and low-side PWM signals between various modules to prevent shoot through current.

Cascode stacking of MOS transistors was enabled by higher source/drain-to-body and gate-to-body ratings ($\sim 2 V_{max}$) compared to the V_{max} ratings of gate-to-source/drain. The two cascode transistors that connect to the switch node can simply be biased to the “mid” voltage, and the swing on the switch node due to the high-side and low-side FETs turning on/off causes the cascode transistors to also follow suit. The power stage comprised of 16 modular slices to enable binary scaling of switching losses with load current and keep the VR efficient at light load conditions. A programmable deadtime block is also integrated into the power train to allow for independent control of the deadtime between the H-L and L-H transitions of the PWM signals. The main purpose of deadtime is to avoid the shoot through currents between the high side and the low side.

B. Analog to Digital Converter

In a digital controller, the high-speed opamp-based compensator is replaced with the digital circuitry executing

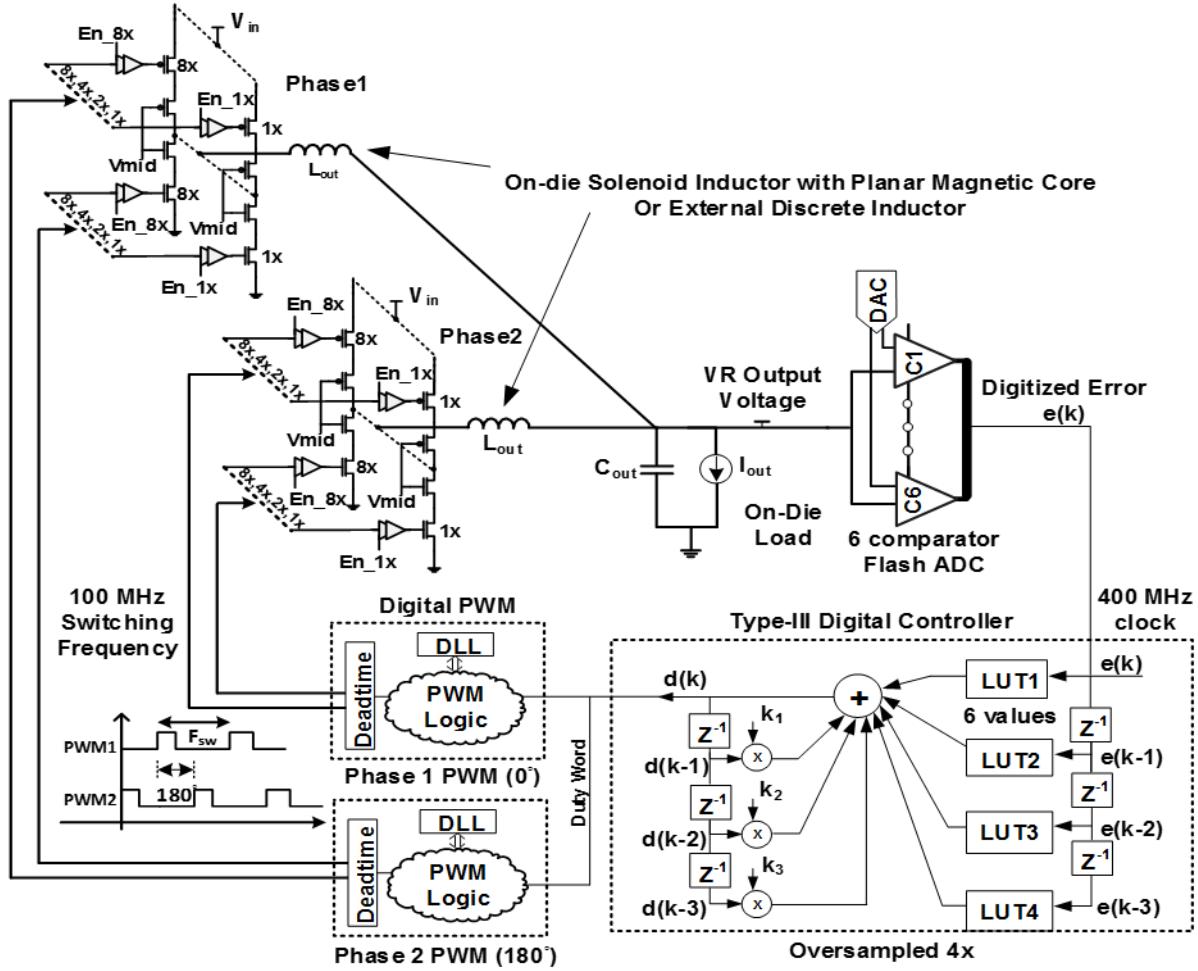


Fig. 4. Functional block diagram of the two-phase digitally controlled IVR with a fully on-die solenoid inductor with planar magnetics.

a difference equation. Such a controller needs a digital representation of the error between the measured output voltage V_{out} and voltage reference V_{ref} . A windowed flash ADC results in a lower power and area requirement, because it requires fewer comparators in the ADC, as compared to traditional ADC approaches [6].

Six low offset comparator-based windowed flash ADC is used to sample and convert V_{out} to sampled error $e(k)$ [Fig. 5(a)]. A 7-bit DAC converts the V_{ref} code into reference voltages for the six comparators. The low offset of the comparators and the 7-bit DAC resolution provide tighter control over the window enabling high accuracy at the output voltage. ADC and DAC design choices are aimed at reducing area and power overheads of the analog front end. A sub-ranging DAC architecture is used to reduce the number of 7-bit multiplexers from six to two. Two 7-bit DACs generate the top and bottom reference voltages which are then buffered with a unity gain amplifier to drive a secondary resistor stack which generates the remaining four reference voltages. Such an architecture not only keeps the area in check but also allows for very fast V_{ref} update rates while minimizing overall power of the windowed flash ADC.

The low offset high-speed comparator is detailed in Fig. 5(b). It consists of a sample-and-hold (S/H) stage,

three cascaded pre-amplifier stages, a high-gain latch, and a local non-overlapping clock generator. This design utilizes three active load pre-amplifiers with switched capacitors for input offset cancellation [7]. The waveforms of the non-overlapping clocks for switched capacitors and latches are illustrated in Fig. 5(b). The high gain of the pre-amplifiers improves the absolute input referred offset [8]. During the hold phase, both the complimentary channels of the S/H are connected to V_{out} and the offset voltage is stored on the capacitors. During the sample phase, V_{out} and V_{ref} are compared along with aforementioned offset voltage providing a self-calibrated offset mechanism. The resulting design is a very low offset high-speed comparator which is ideally suited for windowed flash ADC designs. A Monte Carlo simulation with 500 samples was run at a 400-MHz clock frequency and is included in Fig. 5(b). The mean offset of $32 \mu V$ with a standard deviation of $0.29 mV$ demonstrates the low offset capability of the comparator.

C. Digital Controller

The digital control law generates a duty cycle command $d[k]$ based on the voltage error $e[k]$. The compensator is implemented with difference equations. It is possible to implement many types of compensators such as a PID,

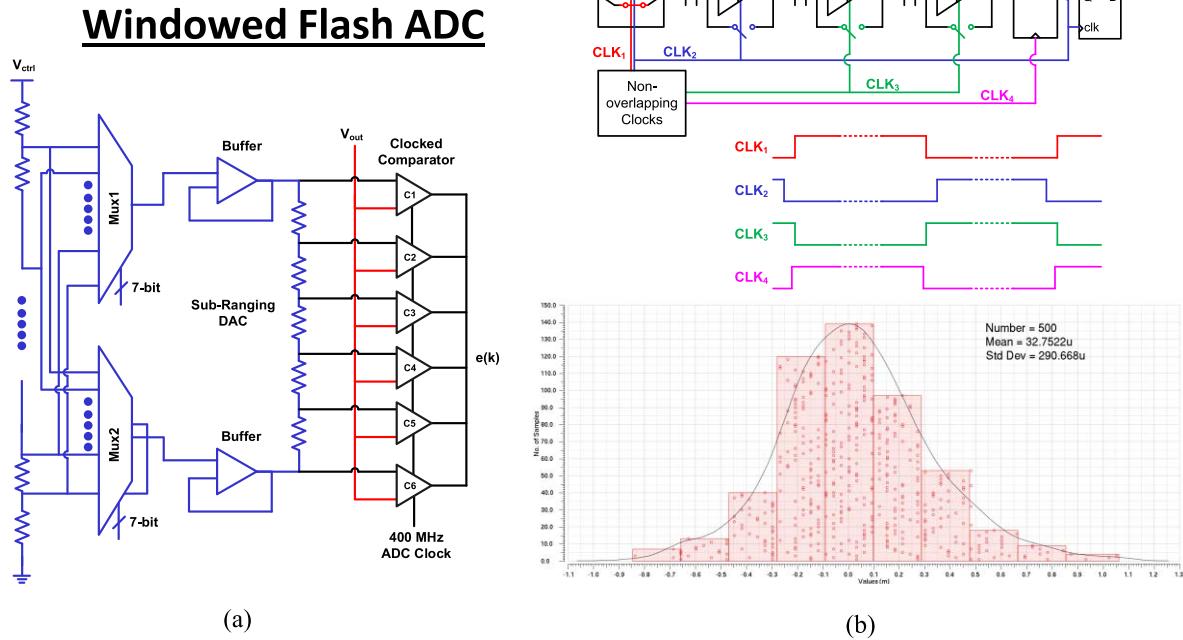


Fig. 5. (a) Architecture of the windowed flash analog to digital converter (ADC) with a sub-ranging digital to analog converter (DAC). (b) Detailed block diagram of the high-speed latched comparators with offset cancellation, the non-overlapping clocks, and the Monte Carlo simulation of input offset voltage.

Type II, or Type III [9]. A Type III digital control law is implemented using lookup tables to reduce multiplication operations which not only lowers power but also improves overall delay of the multiply accumulate block which can help in enabling faster clock speeds if the application so demands. The Type III compensator, which implements an integrator, two poles and two zeros, is designed following a K -factor approach [10], and this can be written in the form of a difference equation as follows:

$$\begin{aligned} d(k) = & a_1 e(k) + a_2 e(k-1) + a_3 e(k-2) + a_4 e(k-3) \\ & + k_1 d(k-1) + k_2 d(k-2) + k_3 d(k-3) \end{aligned}$$

The multiplication factors a_1 , a_2 , a_3 , and a_4 are implemented using lookup tables, as shown in Fig. 4, and are configured using registers. All data is updated with every new output voltage sample. Fixed point arithmetic is used to implement the multiply accumulate block of the difference equation running at 400 MHz. Overflow and underflow protection is also added to provide control over the duty cycle limits which ranges between 0 and 100%. The resulting duty cycle command $d[k]$ is then sent to the digital PWM (DPWM) block.

IV. DIGITAL PWM GENERATION

Digital control implementations for VRs have a DPWM block that generates a duty cycle pulse from an input digital word. Traditionally a hybrid implementation of employing a counter for coarse resolution and a delay line for fine resolution results in the best tradeoff between area and power [11]–[13]. Oversampled digital filters generate multiple

duty cycle words in a single switching period. This complicates the generation of PWM pulses and can cause erroneous PWM generation. Inaccurate DPWM generation creates non-uniform and non-monotonic PWM generation which may adversely affect the overall performance of the IVR and may even result in instability. An ideal DPWM scheme provides dual edge modulation, where both the rising and falling edges of the DPWM pulse can be modulated based on the duty cycle. In addition, if a new duty cycle word is generated during a switching cycle, it should ideally be reflected in the next switching edge. This minimizes phase delay improving overall transient response. Traditional DPWM also involves asynchronous logic which can add significant amounts of verification and validation negating the benefits of a synthesizable design. We propose a method that is effectively synchronous (can be validated with standard static timing tools), and still meets all the requirements listed above.

A. Proposed Digital PWM Generation

A simplified block diagram of the DPWM scheme along with its timing diagram is shown in Fig. 6. A delay-locked loop (DLL) provides delayed versions of the system clock “sys_clk” which in our case is 400 MHz. Feeding the system clock directly into the DLL precludes the need for a delay line per phase, thus reducing area and power overheads. The duty cycle word coming out of the controller $d[k]$ is split into a fine and coarse resolution structure. The DLL resolution sets the fine bits (LSB) while the overall switching frequency as a fraction of the system clock sets the coarse bits (MSB). A phase counter (PC) is used to determine the

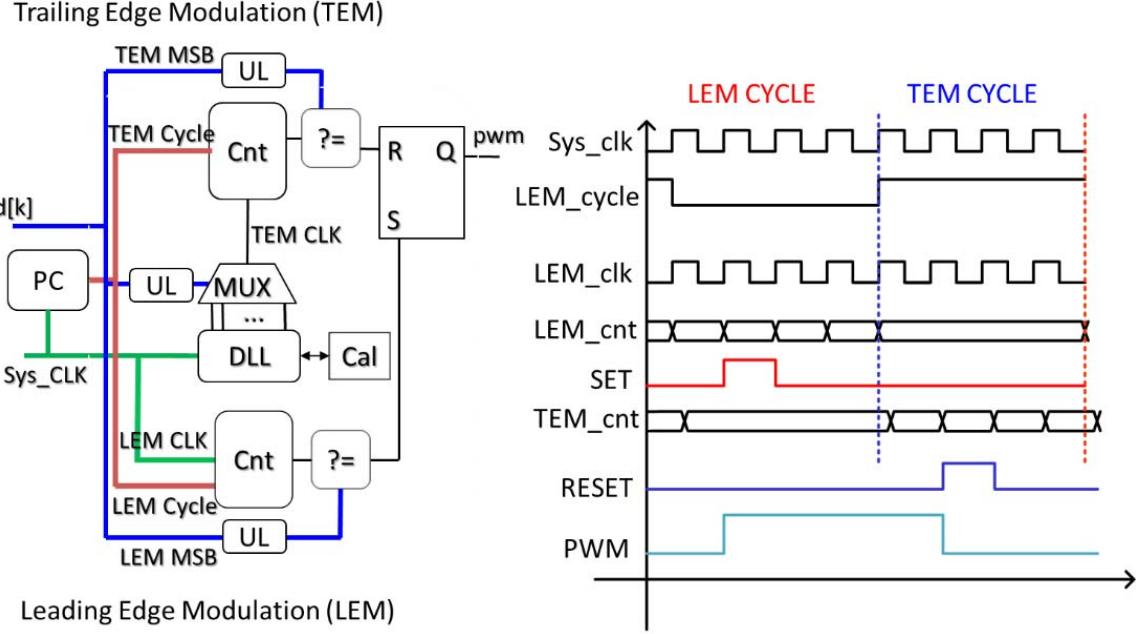


Fig. 6. (a) Single phase, hybrid DPWM architecture. (b) Example timing diagram.

overall switching frequency and divides the switching period into two equal halves, the leading edge modulation (LEM) and trailing edge modulation (TEM) cycles, respectively. The start value of the PC sets the phase shift for the two-phase DPWM to 180° . The DPWM utilizes “update” latches (ULs) with enable/disable features making the latches transparent to duty cycle updates or inhibiting updates during critical execution, thus precluding an asynchronous design while also improving the accuracy of DPWM execution in oversampled controllers. The timing diagram of the DPWM architecture is shown in Fig. 6(b). During the TEM cycle, the TEM clock, which is a delayed version of the system clock, enables the TEM counter. When the output of the counter matches the TEM MSB, a RESET pulse is generated that determines the falling edge of the DPWM. However, during the TEM cycle, the TEM ULs are disabled and so none of the new values of the duty cycle word are seen by the TEM counters and comparison logic. The LEM ULs are, however, transparent during this time and see all the new values generated by the digital controller which would be then used in determining the SET pulse during the next LEM cycle. Similar execution happens during the LEM cycle where the TEM ULs are now enabled while the LEM cycle executes the duty cycle value received during the previous TEM cycle. This ping pong between the LEM and TEM ULs helps to prevent erroneous execution and enable effectively a synchronous design while improving overall accuracy in oversampled controllers.

B. High Resolution Monotonic DPWM Generation

To accommodate high dc accuracy for the output, high frequency operation necessitates a very high resolution (<10 ps) in any DPWM scheme. This delay is smaller than most standard cell delays even on advanced process nodes. To overcome this challenge a combination of inverters with variable sizing is

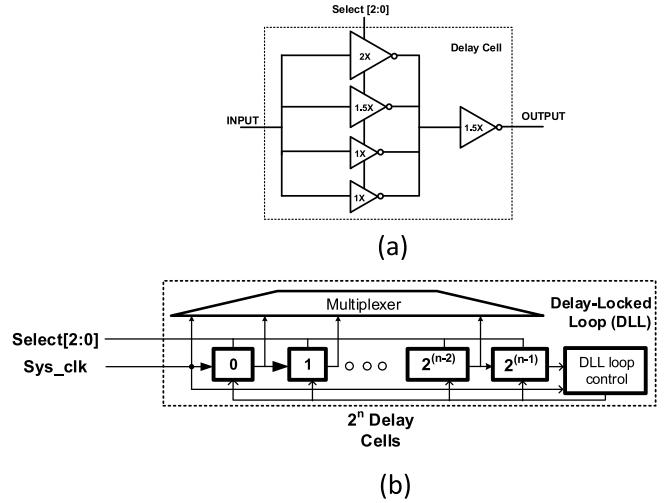


Fig. 7. (a) Variable sizing buffer design. (b) Delay line calibration module.

proposed in this paper, as shown in Fig. 7(a). A digital tuning word referred to as Select [2:0] provides 3-bit control over the overall gate delay of the equivalent buffer. The effective delay depends upon the equivalent sizing of the first stage inverter driving the gate of the second stage. Another major challenge in generating monotonic DPWM across process voltage and temperature (PVT) is to ensure that the delay line is always locked to the system clock referred to as the sys_clk in Fig. 7(b). The calibration block shown in Fig. 7(b) needs to overcome the delay variations of the equivalent buffers across PVT which could have a large variation. The proposed delay line calibration logic provides two types of adjustment: controlling the size of the buffer in order to control its delay, as well as controlling the number of buffers that lock

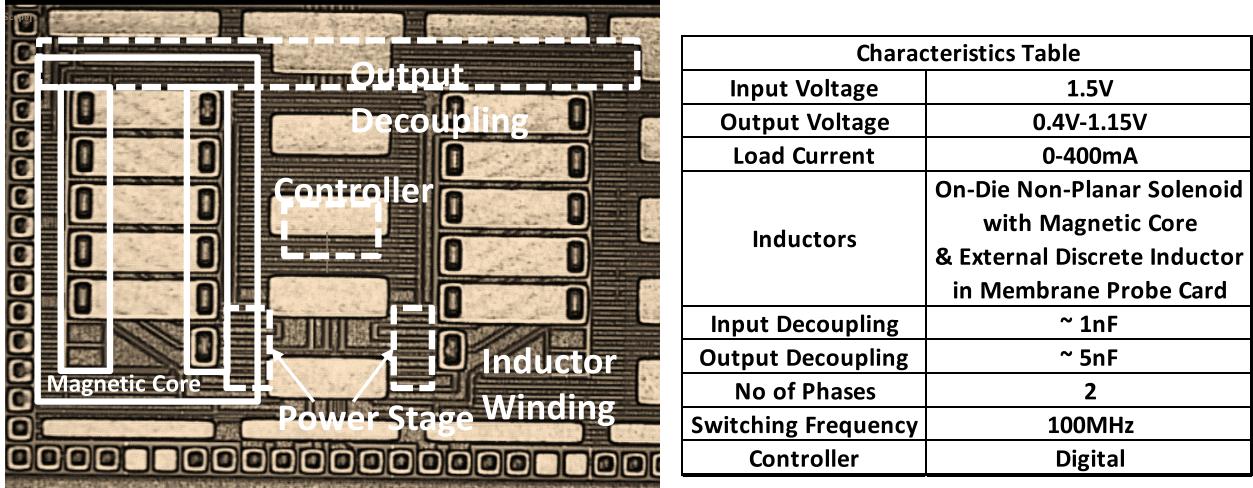


Fig. 8. Chip micrograph and characteristics table.

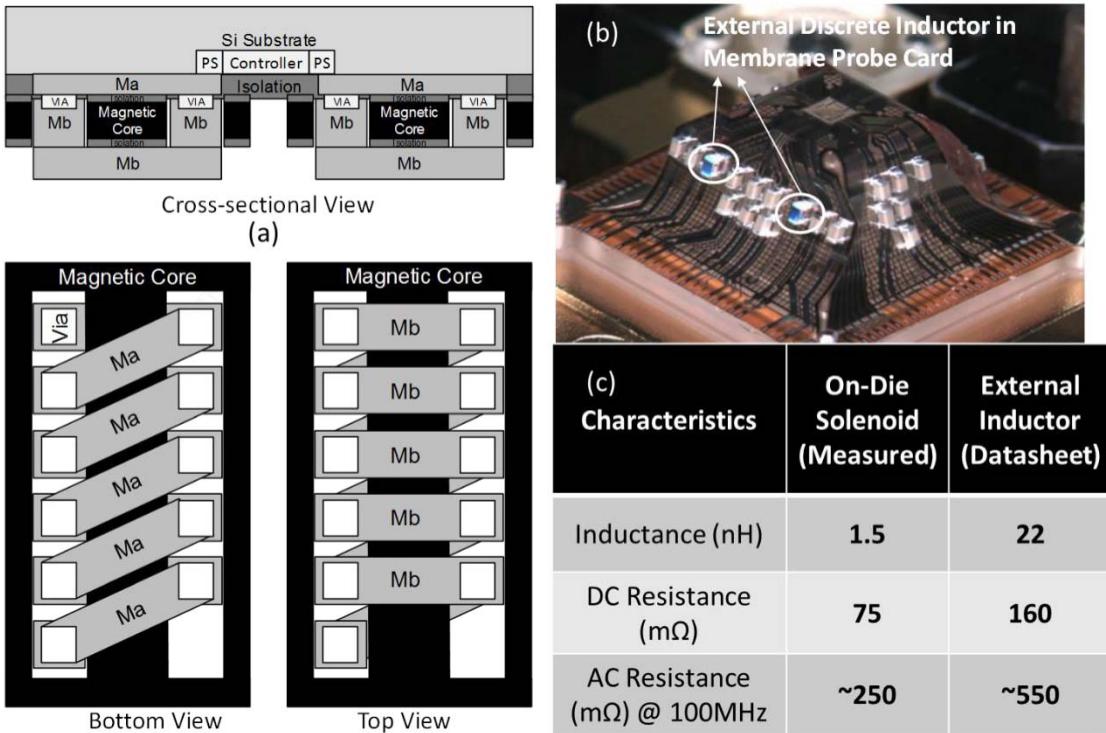


Fig. 9. (a) Cross-sectional, top, and bottom views of on-die solenoid inductor. (b) External discrete 0402 inductor on membrane probe card. (c) Inductor metrics comparison table.

to a single clock period. These two schemes provide sufficient range to counter the PVT variations in the delay line.

V. TEST PROTOTYPE

The chip micrograph of the fully integrated digitally controlled two-phase 100-MHz buck VR with on-die solenoid power inductors is shown in Fig. 8. The total area of the die including the inductors was 0.4 mm². The two phase inductors occupied roughly 0.3 mm² of the total area, as shown in Fig. 8. The input voltage for all measurements was 1.5 V with a programmable output voltage range of 0.4–1.2 V. On-die input and output decoupling capacitors of 1 and 5 nF,

respectively, are implemented using high-density MIM caps. Phase and slice shedding modes were implemented to improve efficiency as a function of the load. The controller runs at a sampling frequency of 400 MHz which is brought in through general purpose I/Os. Along with the inductors for the IVR, identical passive inductor structures were built on the test die for inductor characterization. In addition an external membrane probe discrete inductor was also accommodated to provide meaningful comparisons. An field-programmable gate array-based serial interface was used to provide low-frequency digital bits to configure the IVR into various modes.

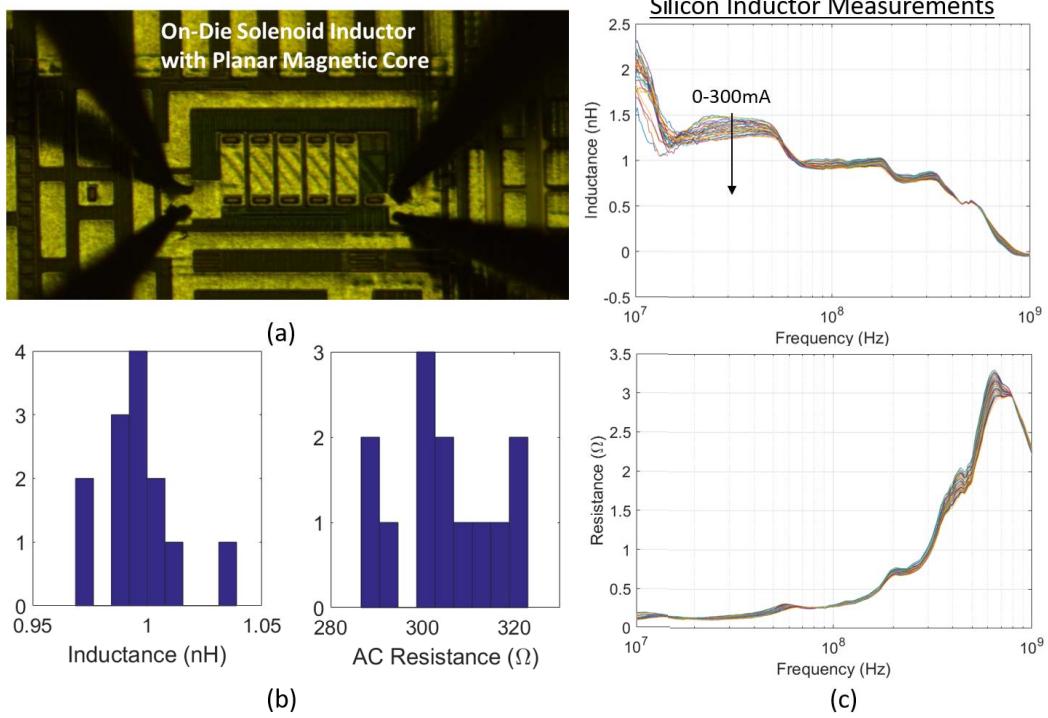


Fig. 10. (a) Standalone inductor measurement setup. (b) Inductance and ac resistance measurements across multiple dies at 100 MHz. (c) Measured inductance across frequency as a function of dc bias current between 0 and 300 mA.

VI. MEASUREMENT RESULTS

In this section, we present silicon measurement results for: 1) inductor structures; 2) PWM resolution for the digital controller; 3) IVR performance metrics (efficiency and transient); and 4) efficiency and output impedance of IVRs with on-die and external inductor structures. Cross-sectional, top, and bottom views of the on-die inductor are shown in Fig. 9. The views showcase a solenoid inductor structure with five vertical turns around a high-permeability planar magnetic core utilizing two thick-top metal layers Ma ($6 \mu\text{m}$) and Mb ($12 \mu\text{m}$). The external 0402 Murata inductor along with its key metrics is shown in Fig. 9(c). A higher inductance with reasonable dc resistance and a Q of >20 is typical of external discretes and such an inductor is chosen to reduce impacts of the parasitic impedances of the inductor connections to the VR die. The standalone inductor measurement setup is shown in Fig. 10(a). A histogram of inductance and resistance measurements made on 13 fabricated samples at 100 MHz is shown in Fig. 10(b). The median inductance is 0.998 nH and the median resistance is 303.4 m Ω at 100 MHz. The measured dc resistance is 75 m Ω . The highest inductance of about 1.5 nH is measured at about 30 MHz. The variation of inductance as a function of dc bias current is shown in Fig. 10(c). As evident from Fig. 10(c), there is about a 16% change in inductance for a total change in dc bias currents from 0 to 300 mA. The peak quality factor of the inductor structure is about 3.

The DPWM is linear and monotonic (Fig. 11), and achieves 8-ps resolution that translates to 3-mV output voltage steps. This translates to a DPWM resolution of >9 bits at the 100-MHz clock frequency. The output voltage settling time of $\sim 0.7 \mu\text{s}$ for reference voltage steps from

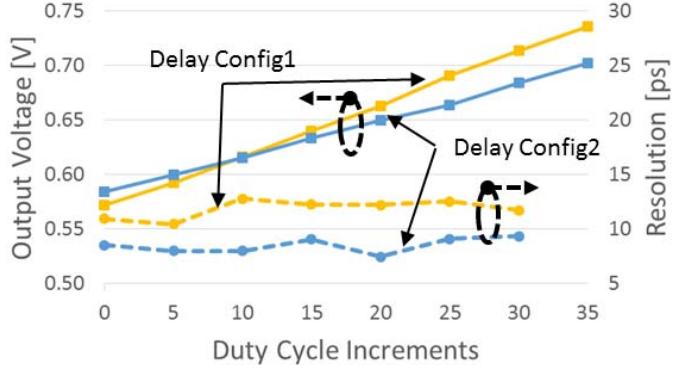


Fig. 11. Output voltage and PWM resolution for different duty cycle values for two delay configurations.

0.45 to 0.95/0.6 V demonstrates an output voltage slew rate of $\sim 0.75 \text{ V}/\mu\text{s}$ (Fig. 12). Load regulation for a periodic 125-mA load current step and input line regulation for periodic 1.5- to 1.6-V input voltage transients at 100–200 μs repetition intervals are also demonstrated. Two-phase operation reduces output ripple by 2 \times compared to the single phase mode over the entire output voltage range. Ripple is even lower for the VR with external inductor. The relatively high ripple seen can be attributed to the limited amount of output decoupling capacitor. In real applications, the amount of area available for on-die decoupling would be larger and the number of phases for larger load currents would be higher. Both of these factors would significantly reduce the output voltage ripple.

Combinations of slice and phase shedding at lower load currents achieve a flat 80%–84% conversion efficiency across a 90–330 mA load current range, for 1-A/mm 2 max current

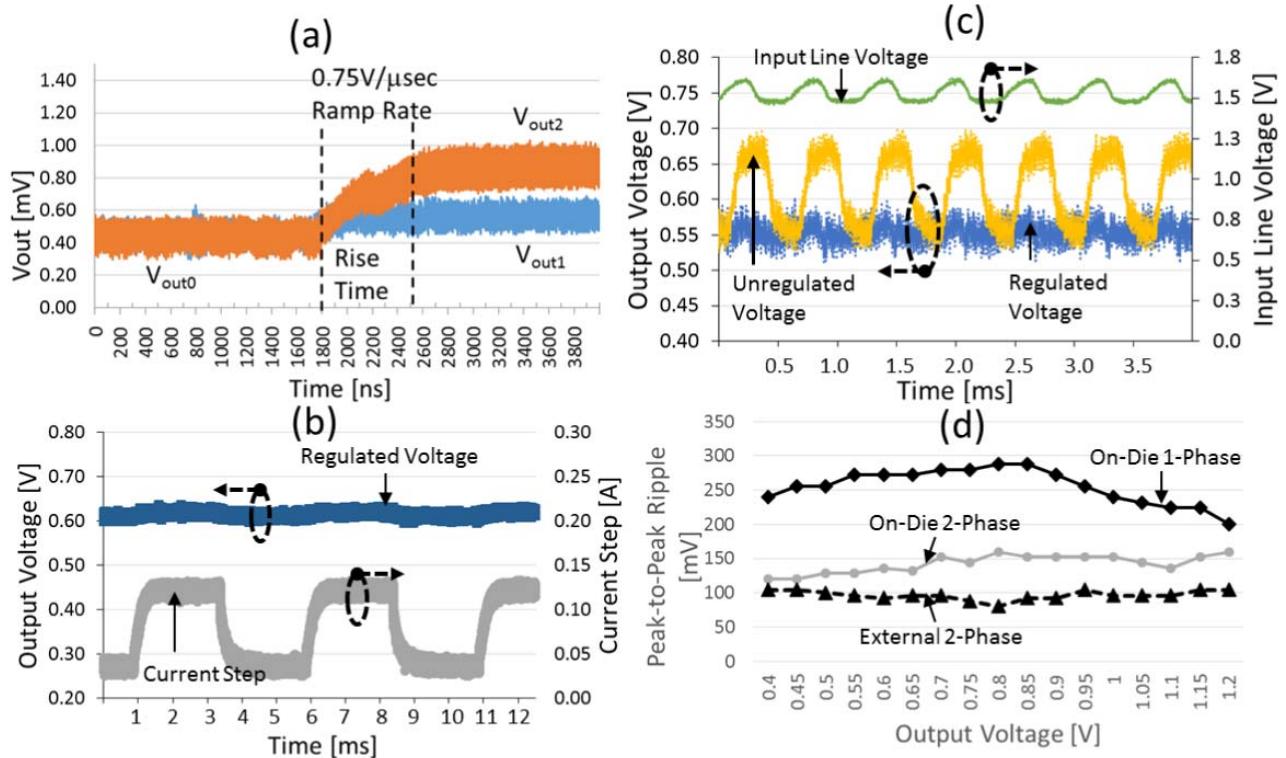


Fig. 12. (a) Measured closed-loop response for reference step (0.45–0.95/0.6 V). (b) Load step of 125-mA periodic steps. (c) Line Step 1.5–1.6 V steps. (d) Peak-peak voltage ripple for on-die and external inductor.

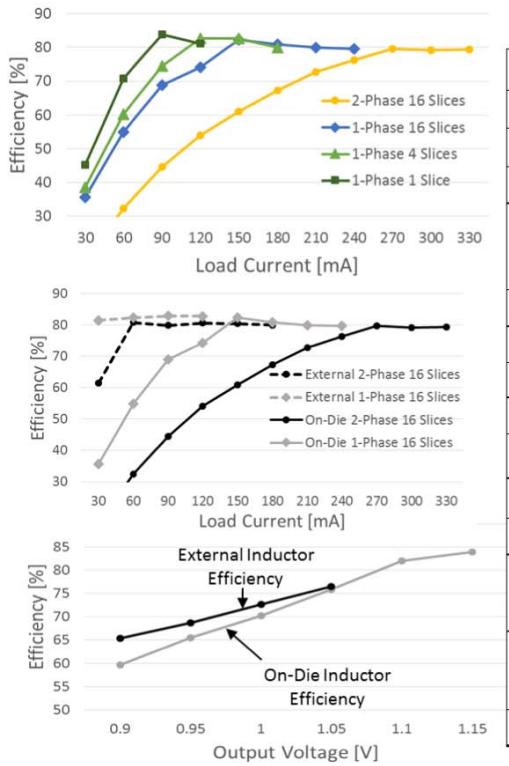


Fig. 13. Measured efficiency plots of on-die inductor VR across load; Comparison of efficiency of on-die and external inductor VRs across output voltage and across load; Comparison of work with state of art.

density at 1.15 V (Fig. 13). The inductor performance degrades with increasing current, and the magnetic inductor core saturates beyond 330 mA, thus setting the regulation limit of

the converter. The large signal magnetic saturation current limit of the inductor, including both dc and switching ripple currents, is around 1.5 A per phase. A pie chart showing the

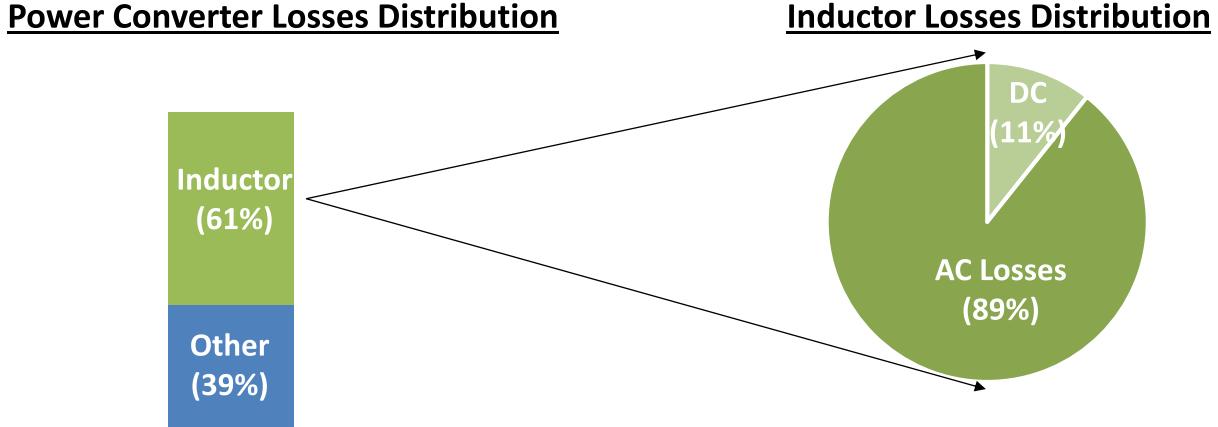


Fig. 14. Distribution of losses within power converter, and losses distribution within solenoid inductor.

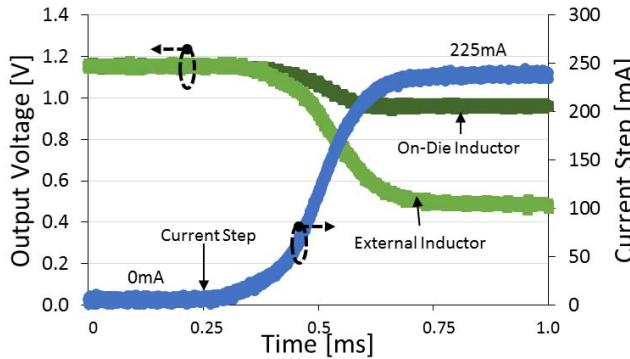


Fig. 15. Open loop output voltage droop for on-die and external inductor VR setups for a 225-mA current step.

breakdown of losses of the on-die IVR is presented in Fig. 14. About 60% of the overall converter losses are attributed to the inductor. In addition, ac loss components, including core and winding losses contribute to 90% of the inductor losses. Fig. 13 also shows the measured efficiency of the external inductor along with that of the on-die inductor and it is evident that the efficiency is higher for the VR with external inductor than the on-die inductor at the same operating points. However, the external inductor setup is unable to load high current at smaller dropouts unlike the on-die inductor. This can be primarily attributed to the larger dropouts across the interconnect impedances as explained in [1]. The dc resistances can be large but the ac resistances play an even bigger role especially at 100's of MHz thus requiring a much larger dropout to deliver the same amount of current significantly impacting the power density. The measured open loop output voltage droop, in response to a load current step of 225 mA, is 2.5× higher for the external inductor than the on-die inductor, as shown in Fig. 15. The lower dropout enables higher power density for the VR with on-die inductor.

VII. CONCLUSION

The industry's first fully integrated digitally controlled two-phase buck VR with on-die solenoid inductors with a planar magnetic core is demonstrated in 14-nm tri-gate CMOS for fine-grained power delivery/management domains of high

power density in SoCs while enabling ultra-thin (z -height) packages. This is the highest level of integration achieved on a buck converter where the inductor and IVR active circuits are integrated on the same monolithic die. The VR achieves 1-A/mm² power density for 400-mA load current with a measured peak efficiency of 84% at 100-MHz switching frequency which is very comparable to the existing state of the art but with a 5× improvement in power density and 16% improvement in efficiency over equivalent point of load converters with spiral inductors. Digital PWM with >9 bits (8 ps) of resolution is discussed which preserves synchronous operation with high accuracy for oversampled digital filters. A comparison between on-die and external discrete inductor structures is also provided with the associated tradeoffs emphasizing that while external inductors provide better efficiency than the on-die inductor structures can help maximize the overall power density and is best suited for fine-grain DVFS domains of high power density in complex SoC on ultra-thin coreless packages.

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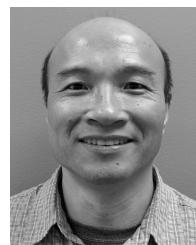
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