A 0.18-μm CMOS Image Sensor With Phase-Delay-Counting and Oversampling Dual-Slope Integrating Column ADCs Achieving $1e^-_{rms}$ Noise at 3.8-μs Conversion Time

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***Abstract*— A CMOS image sensor (CIS) is presented, simultaneously achieving low noise and high frame rate. The imager innovatively employs column-parallel dual-slope (DS) integrating analog-to-digital converters (ADCs) based on a phase-delay-counting principle and using oversampling to suppress the readout thermal noise. A noise analysis of the DS-integrating ADC in correlated-double-sampling operation is provided to prove the low-noise advantage of the proposed architecture. Furthermore, the design considerations of the presented architecture are derived based on the analysis of nonideality effects. Based on these analytical results, design tradeoffs are discussed and applied in the test chip. The test chip, fabricated in a 4M1P 0.18-μm CIS technology, contains a 128 × 128 pixel array. The measurement results show that each of the 128 column-level ADCs converts a pixel in 3.8 μs and achieves a noise floor of $1e^-_{rms}$. The chip consumes 49 mW excluding the I/O power and 59 mW including the I/O power, resulting in a very good figure of merit value of 1.4 and 1.7 [e^-.nJ], respectively.**

***Index Terms*— Column analog-to-digital converters (ADCs), DS ADC, dual slope (DS), DS integrating ADC, high speed, image sensors, jitter, low noise, phase counting, ring oscillators, settling time, thermal noise.**

I. Introduction

In INDUSTRIAL, surveillance, and automotive applications, low-light-level imaging is an important feature. Achieving low-noise performance, however, usually goes together with low speed due to the need for multiple-sampling operation [1], [2], [4] and high-gain amplifiers [2]–[4]. An elegant approach with an incremental sigma–delta (ISD) analog-to-digital converter (ADC) [5] and its variant with feed-forward architecture and floating-point conversion [6] have been proposed to suppress the readout thermal noise and the ADC quantization error, while maintaining a relatively fast conversion. However, the low-power inverter-based approach of [5] is sensitive to power–voltage–temperature variations in the column-level circuitry, as there may be thousands of ADCs working simultaneously. The approach with floating-point ISD of [6], although improving the conversion speed by an adaptive reference adjustment mechanism, requires an extra comparator, a calibration mechanism for references, and a floating-point correction scheme. Furthermore, a 12-bit conversion with the second-order ISD architecture requires more than 100 samples, imposing low-crosstalk design challenges to the global distribution of clocks, reference, and power supplies.

This paper presents, for the first time, an imager employing column dual-slope (DS) integrating ADCs based on the phase-delay-counting principle and using oversampling to suppress pixel thermal noise, achieving simultaneously $1e^-_{rms}$ noise and 3.8 μs line conversion time. The main reasons for adopting the DS integrating ADCs as column-parallel ADCs are that they are insensitive to the variations of the column analog elements and the counting frequency, as well as that they suppress the thermal noise of the previous stages [9]. In addition, different from traditional edge-based counting in column ramp-based ADCs [7], in which only one edge of an oscillator node is used, the phase-delay-counting principle [10], [11], [31] utilizes all the edges of all oscillator nodes for counting and boosting the conversion speed up 16 times in this paper, without significant power increase. The phase-delay-counting operation in this paper is based on the coarse-and-fine counting principle, where the oscillator phase states and the coarse counter outputs are taken at the end of the conversion as the fine conversion values and the coarse conversion values, respectively.

This paper is organized as follows. Section II describes the CMOS image sensor (CIS) architecture and the block diagram. The noise analysis is provided in Section III. Section IV discusses in detail the nonidealities of the circuits. Section V presents the circuits implementation, while Section VI shows the experimental results of the test chip. Section VII concludes this paper.

II. CMOS Image Sensor Architecture

A. Block Diagram

Fig. 1(a) shows the block diagram of the image sensor employing column-parallel DS integrating ADCs with the phase-delay-counting principle. The image sensor consists

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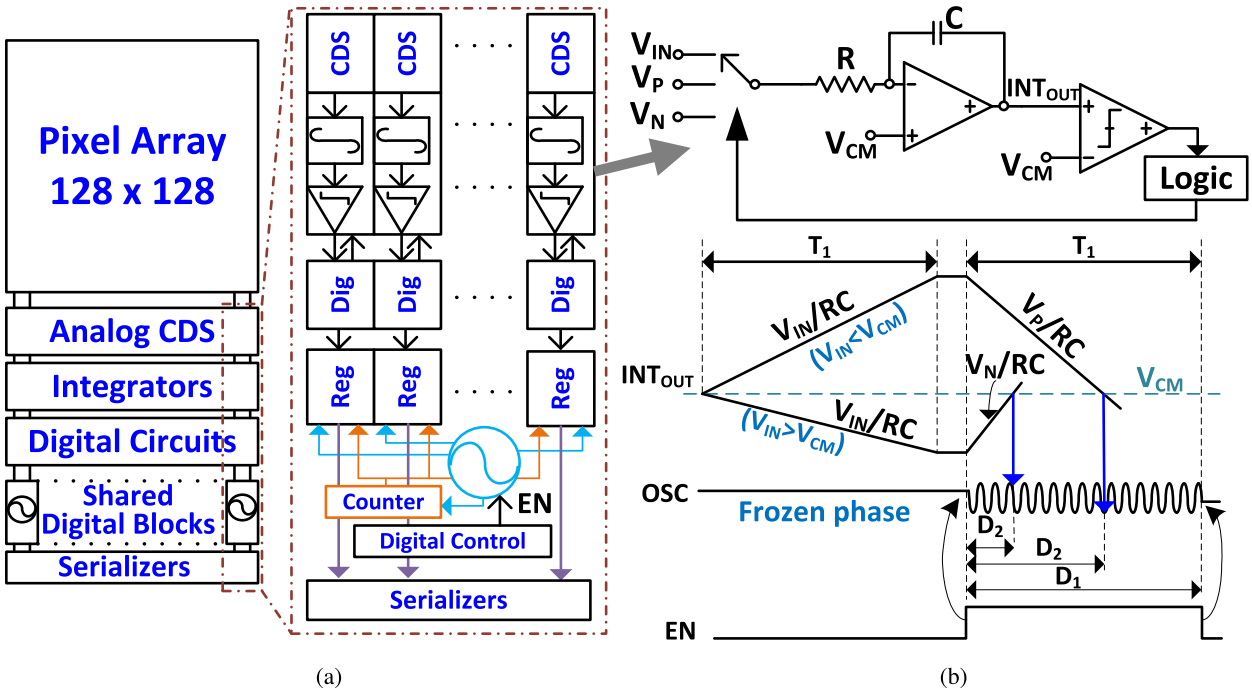


Fig. 1. (a) Block diagram of the image sensor. (b) Simplified schematic and timing diagram of the DS integrating ADC.

of a 5.5–μm 128 $\times$ 128 pixel array and column readout circuits, including correlated-double-sampling (CDS) buffers, DS integrating ADCs, and digital circuitry. In every column, through the analog CDS buffer, the pixel signals are applied at the input of the DS integrating ADC, consisting of an RC integrator and a comparator as well as a counter and a ring oscillator, shared for every 16 columns. The reasons for using a ring oscillator for 16 columns are that 16 is a medium divider of 128, and that 16 columns leave enough space for a layout with good isolation for each ring oscillator. When the comparator trips, the counter value and the phase state of the ring oscillator are captured in the coarse and fine registers, respectively. These values are then read out through a set of serializers.

A simplified schematic of the RC integrator of the DS integrating ADC is shown in Fig. 1(b) as well. First, the input signal V_{in} is applied to the integrator input during the first integration for a certain period T_1, which determines the resolution of the conversion. Then, depending on the ending value of the integrator output INT_{OUT}, which represents the input polarity, either the reference voltage V_P or V_N is connected to the integrator input during the second integration. The input voltage can be determined as

$$\frac{V_{\text{in}}}{RC} D_1 T_{\text{clk}} = \frac{V_{\text{ref}}}{RC} D_2 T_{\text{clk}}, \quad \text{hence } V_{\text{in}} = V_{\text{ref}} \frac{D_2}{D_1} \tag{1}$$

where RC is the integrator time constant; $D_{1,2}$ are the digitized values of the first and the second integration, respectively; T_{clk} is the counting clock period to digitize the two integrating periods; and V_{ref} is V_P if V_{in} is smaller than V_{CM} or V_N if V_{in} is greater than V_{CM}. The main benefit of the dual-polarity approach is that the input operating range is doubled [12]. Equation (1) shows that the DS integrating ADCs, like all DS ADCs, are independent of the variations of the RC values and the counting frequency, which is of great benefit to the column readout circuits that use fast column oscillators to improve the conversion speed. In this design, as shown in Fig. 1(b), the first integration time T_1 is digitized by the oscillator in the second integrating period, as a result of which a 50% reduction in oscillator power is realized as the oscillator is enabled only in the second half of the conversion. The operations of the shared ring oscillator and the shared counter are not impacted by the triggering actions in the columns thanks to the buffers used.

B. Column ADC Operating Principle

Fig. 2 shows the simplified schematic of the column readout circuit, while Fig. 3 shows the timing diagram of the circuit in Fig. 2 for 1 pixel CDS readout operation. Through the CDS buffer OP1, the pixel reset level and the pixel signal level are, respectively, shifted to the appropriate working levels. The effect of the capacitor on the node V_1 is to make the CDS buffer more stable and tolerant to the switching actions at the input of the opamp OP2, which was connected to V_P or V_N. Then, the CDS buffer output V_1 and the references V_P and V_N share the same buffer OP2 to drive the integrator. A capacitor is also added to the output of the opamp OP3 to reduce the noise bandwidth of the integrator.

In Fig. 2, in order to implement the phase-delay-counting, the phase states of the ring oscillator shared for every 16 columns are recorded for the fine conversion, while the coarse conversion is performed in the shared counter, which is triggered by one predetermined phase node P_{COUNT} in the shared ring oscillator. The shared counter outputs and the phases of the shared ring oscillator are, respectively,

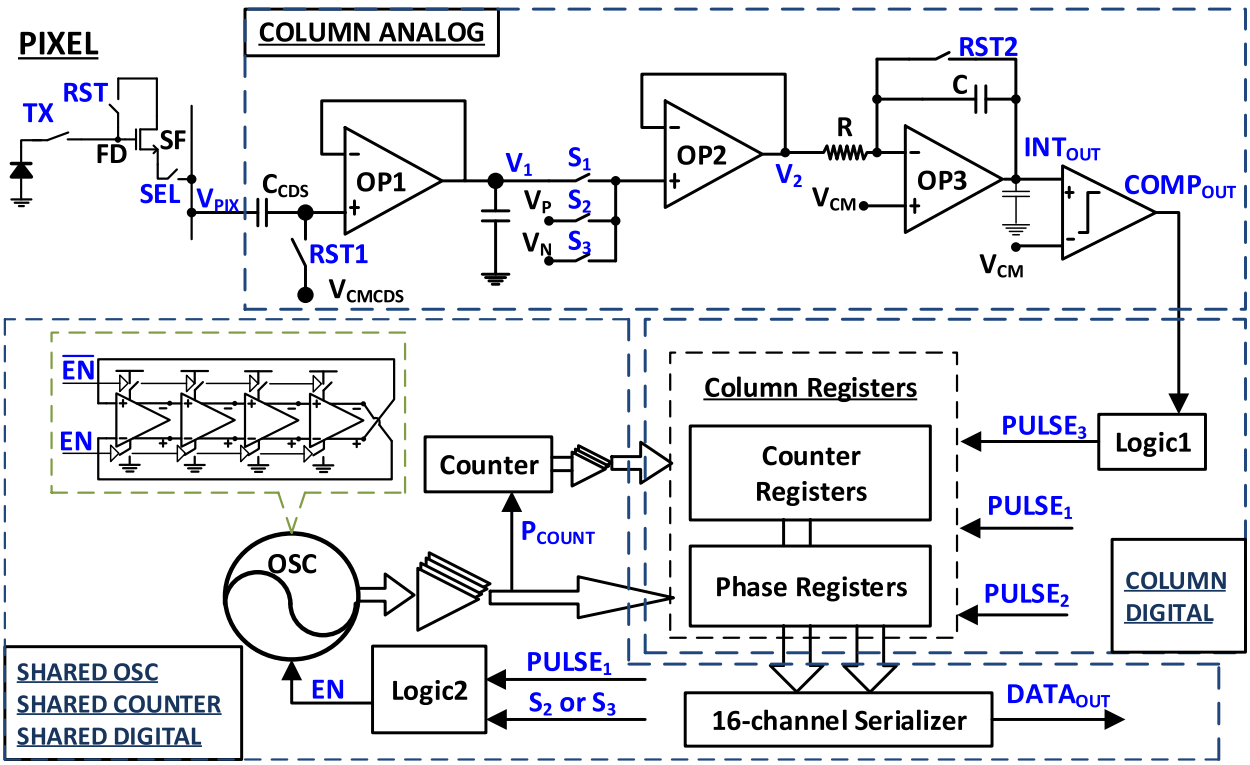


Fig. 2. Simplified schematic of the column readout circuitry.

captured at the counter and the phase registers in every column during the rising edges of the pulses $PULSE_{1,2,3}$. While the pulse $PULSE_3$ is generated from the comparator output $COMP_{\rm OUT}$ to capture the coarse and fine values when the second integrating slope crosses the comparator common-mode level, the pulses $PULSE_2$ and $PULSE_1$ record these values at the beginning and the ending of the second integration, respectively. As shown in Fig. 3, the second integrating period is the difference between pulses $PULSE_3$ and $PULSE_2$, and the first integrating period is the difference between pulses $PULSE_1$ and $PULSE_2$. In our design, as shown in Fig. 2, and in more detail in Fig. 4, the ring oscillator is designed with four stages of differential inverters with enable/disable switches controlled by the enable pulse EN. The table in Fig. 4 also shows the 16 phase delay states, each of which is a unique combination of the logic levels of all eight oscillator nodes. Therefore, one oscillator period T_0 is composed of 16 delay units t_d. As a result, in combination with (1), the input voltage can be determined as follows:

$$V_{\rm in} = V_{\rm ref}\frac{M_1T_0 + n_1t_d}{M_0T_0 + n_0t_d} = V_{\rm ref}\frac{16M_1 + n_1}{16M_0 + n_0} \qquad (2)$$

where $M_{0/1}$ and $n_{0/1}$ are, respectively, the coarse and the fine counting values of the first and the second integrating slopes. As shown in the timing diagram in Fig. 3 and the oscillator schematic in Fig. 4, the oscillator is enabled and disabled by, respectively, activating and deactivating simultaneously the top and the bottom current-source transistors. This helps to preserve the phase state of the oscillator to eliminate counting error accumulation in the oversampling operation [10], which is shown in Fig. 3 as well for an oversampling ratio (OSR) of 4. Indeed, the oversampling operation extends the input dynamic range, because the first integrating slope T_1 is divided into smaller portions, preventing the integrator output $\rm INT_{OUT}$ from being saturated due to a long integration time.

III. Noise Analysis

As noise is a key characteristic in imagers, in this section, both the thermal noise and the jitter noise of the proposed ADC are analyzed and discussed in detail.

A. Thermal Noise Behavior of the DS Integrating ADC in CDS Operation

Fig. 5(a) shows the noise effects in single-slope (SS) and DS integrating converters. Assume that the input-referred noise $n(t)$ at the input of both the SS and DS integrating converters represents all the noise caused by analog components of the whole readout chain, including the pixel, the CDS buffer, and the ADC. As shown in Fig. 5(a), for the SS conversion, the input-referred noise when the SS ramp crosses the input voltage is $n(t_2)$, where t_2 is the crossing moment. For the DS integrating case, on the other hand, the input-referred noise is integrated together with the input signal and the reference in the first and the second integrating slopes, respectively, according to $\int_0^{t_1}(V_{\rm in} + n_1(t))dt$ and $\int_{t_1}^{t_1+t_2}(V_{\rm ref} + n_2(t))dt$, where $n_1(t)$ and $n_2(t)$ are the input-referred noise when the CDS buffer output and the reference voltage are applied to the DS integrating ADC, respectively. The magnitude of the noise $n_2(t)$ is considered to be smaller than that of the noise $n_1(t)$, because it is easier to maintain a clean reference path than to achieve a low-noise readout path. For the sake of simplicity,

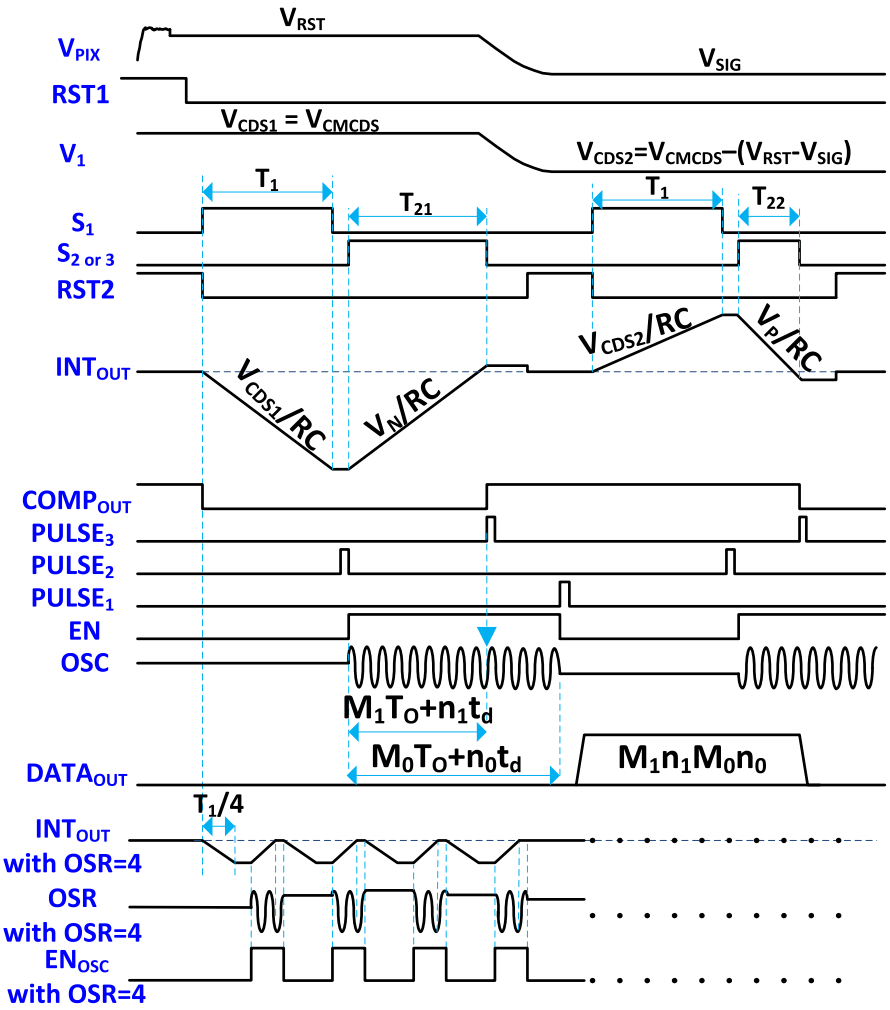
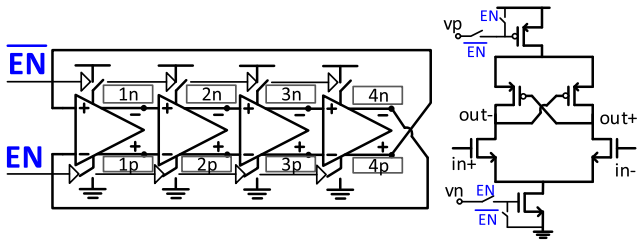


Fig. 3. Timing diagram of the readout circuit for one CDS readout operation in the case of a single conversion and oversampling with OSR = 4.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1n	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
1p	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
2p	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0
2n	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
3n	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0
3p	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1
4p	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0
4n	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1

Fig. 4. Schematics of the shared ring oscillator and the differential inverter stage used, as well as the 16 phase delay states within one oscillator cycle.

we assume that $n_2(t) \equiv n_1(t) \equiv n(t)$. Hence, (1) can be expressed as $V_{\text{in}} = (t_2/t_1)V_{\text{ref}} + (1/t_1)\int_0^{t_{\text{int}}} n(t)dt$, where t_1 is both the time for a full ramp of the SS conversion and the first integrating slope period of the DS integrating ADC to ensure that the conversion resolutions of the two conversions are the same; t_2 is the duration of the second integrating slope of the DS integrating ADC; and $t_{\text{int}} = t_1 + t_2$. Similar to the lossless integral noise work in [16] and the CDS noise work in [13] and [14], the noise power spectral density (PSD) (V^2/Hz) in the output of the DS integrating conversion can be determined as

$$S_{\text{DS}}(f) = 4\left(\frac{t_{\text{int}}}{t_1}\right)^2 S_n(f)\text{sinc}^2(\pi f t_{\text{int}})\sin^2(\pi f t_{\text{CDS}}) \quad (3)$$

where $S_n(f)$ is the PSD of the input-referred noise $n(t)$; t_{CDS} is the time interval between the two conversions in the CDS operation. t_{CDS} must be greater than t_{int} for the CDS operations. It can be seen from (3) that the DS integrating conversion filters the input-referred thermal noise with a low-pass filtering function of $\text{sinc}^2(\pi f t_{\text{int}})$, while the SS conversion behaves as an all-pass filtering system.

Fig. 5(b) shows the comparison between the noise transfer function of the DS integrating ADC and the SS ADC. The DS integrating ADC noise transfer function is plotted for two cases: an integration time t_{int} of 1 and 2 μs. It is shown clearly that the DS integrating ADC suppresses the

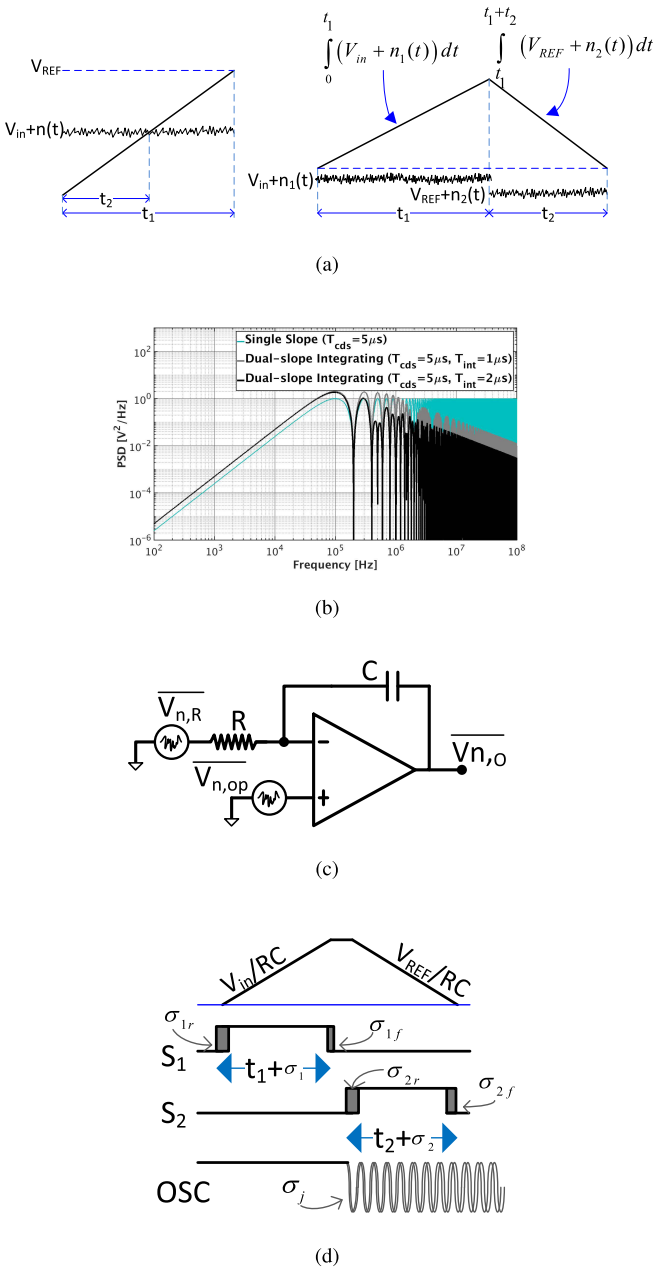


Fig. 5. Noise analysis. (a) Noise effects in SS and DS integrating conversions. (b) Noise PSD for the SS and the DS integrating ADCs. (c) Equivalent noise model of the RC integrator. (d) Jitter noise model.

high-frequency noise like a first-order low-pass filter. The longer the integration time $t_{\rm int}$ is, the lower the cutoff frequency achieved, resulting in less noise. From (3), the -3 dB low-pass cutoff frequency can be estimated as $f_{-3\ \rm dB} \approx 0.45/t_{\rm int}$. Additionally, the CDS operation suppresses the low-frequency noise as well, and the shorter the CDS interval $t_{\rm CDS}$ is, the higher the cutoff frequency of this high-pass filter, resulting in stronger $1/f$ noise suppression. Therefore, a careful timing diagram is of high importance in our architecture to optimize the tradeoff between $t_{\rm CDS}$ and $t_{\rm int}$, where the former always needs to be greater.

For more insight into the noise calculation, Fig. 5(c) shows an equivalent thermal noise model of the integrator. It can be seen from Fig. 5(c) that the resistor thermal noise is also suppressed by the function $\text{sinc}^2(\pi f t_{\rm int})$, because this noise is integrated by the integrator. However, the integrator opamp noise appears at the integrator output in the time domain as

$$v_{n,o}(t) = v_{n,\rm op}(t) + \frac{1}{RC}\int_0^t v_{n,\rm op}(\tau)d\tau. \tag{4}$$

Then, the integrator opamp noise is present in the DS integration equation as

$$V_{\rm in} = V_{\rm REF}\frac{t_2}{t_1} + [v_{n,\rm op}(t_{\rm int}) - v_{n,\rm op}(t_1)]\frac{RC}{t_1} + \frac{1}{t_1}\int_0^{t_{\rm int}} v_{n,\rm op}(\tau)d\tau. \tag{5}$$

It can be seen from (5) that the integrator opamp noise is partly suppressed by the low-pass filtering function of $\text{sinc}^2(\pi f t_{\rm int})$ as in (3) and partly suppressed by the ratio RC/t_1, which is greater than 10 in this design.

Similarly, the integrator reset noise is also suppressed by this ratio. With the reset noise $V_{n,\rm RST2}$ caused by the RST2 switch of the integrator present, the input voltage of the DS integrating ADC can be determined as

$$V_{\rm in} = t_2 \times V_{\rm REF}/t_1 + V_{n,\rm RST2} \times RC/t_1. \tag{6}$$

The oversampling operation achieves better noise performance, because the total integrating time is proportionally increased with the OSR value. It can be seen from (6) that the reset noise is suppressed by the factor RC/t_1. Since, in our design, RC is 40 ns, and t_1 can be larger than 600 ns for the multiple sampling option, this noise is strongly suppressed. Therefore, t_1, and OSR in the multiple sampling case, are very important parameters in deciding the total noise. OSR determines the maximum value of t_1 that the integrator is not saturated. This also means that the noise is higher if either R or C becomes larger. In section IV, the nonlinearity of the circuit will be discussed, showing that highly linear designs are achieved with high RC values, therefore, at the cost of higher noise.

The noise budgeting for the pixel, the CDS buffer, the unity-gain buffer, the resistor, the integrator, and the integrator reset action is also addressed in this section. Similar to works in [30] and [2], based on noise equations in [32], the input-referred noise at the CDS buffer input $V_{\rm PIX}$ in Fig. 2 in a digital CDS operation can be determined as

$$\overline{V_{n,\rm Vpix}}^2 = 2\left(F_{\rm SF}{}^2\xi_{\rm SF}k_BT\frac{\omega_{\rm INT}}{gm_{\rm SF}} + k_BT\frac{\omega_{\rm INT}}{gm_1} + k_BT\frac{\omega_{\rm INT}}{gm_2} + k_BTR \times \omega_{\rm INT} + k_BT\frac{\omega_{\rm INT}}{gm_3} + \frac{k_BT}{C_{\rm load}}\left(\frac{RC}{t_1}\right)^2 + \frac{k_BT}{C}\left(\frac{RC}{t_1}\right)^2\right) \tag{7}$$

where $F_{\rm SF}$ is the noise gain of the pixel source follower; $gm_{\rm SF}$, gm_1, gm_2, gm_3 are the transconductances of the pixel source follower, the CDS-buffer opamp, the unity-buffer opamp, and the integrator opamp in Fig. 2, respectively; $\xi_{\rm SF}$ is the pixel source follower excess noise factor; $\omega_{\rm INT}$ is the low-pass filtering cutoff frequency of the integrator; and $C_{\rm load}$ is the load capacitance of the integrator opamp. For a coarse noise

estimation, we assume that $t_{\text{int}} = 1000$ ns, $RC = 40$ ns, $t_1 = 720$ ns, $F_{\text{SF}} = 1.5$, $\xi_{\text{SF}} = 2$, $gm_{\text{SF}} = gm_1 = gm_2 = gm_3 = 70$ μS, and $C_{\text{load}} = 100$ fF. The rms noise values contributed by the pixel, the CDS buffer, the unity-gain buffer, the resistor, the integrator, opamp, and the reset noise are then 27, 13, 13, 2.7, 17, and 8 μV_{rms}, respectively. Therefore, the total rms input noise value contributed by these analog components is 53 μV_{rms}. This rms noise value is lower with a longer integration time t_{int} and better opamp biasing conditions.

B. Clock Jitter Analysis

In the DS integrating ADC, as shown in Fig. 5(d), the jitter noise in the oscillator, and in the integrating slope periods (t_1 and t_2) controlled by the pulses S_1 and S_2, contributes directly to the error of the integrating periods and the digitized values D_1 and D_2. Since the pulses S_1 and S_2 are synchronized with a clean clock, their jitter effect is negligible. Regarding the jitter noise caused by the ring oscillator, since the full resolution of the first integrating period is measured in every conversion, the jitter-accumulated noise of the ring oscillator is tracked and its effect is minimized within one conversion. The work in [18] has shown in detail that the ring oscillator jitter over time is

$$\delta^2(t) = \kappa^2 t + \zeta^2 t^2 \tag{8}$$

where κ is the thermal jitter noise factor and ζ is the flicker jitter noise factor. It can be seen from (8) that the total jitter noise is dominated by the thermal noise for short measurement times, and by the flicker noise for long measurement times. Equation (1) can then be expressed as

$$\frac{V_{\text{in}}}{V_{\text{ref}}} = \frac{D_2 t_d + e_j(t_2)}{D_1 t_d + e_j(t_1)} \approx \frac{D_2}{D_1}\left(1 + \frac{e_j(t_2)}{D_2 t_d} - \frac{e_j(t_1)}{D_1 t_d}\right) \tag{9}$$

where $e_j(t_2)$ and $e_j(t_1)$ are the errors caused by the oscillator jitter at the end of the t_2 conversion and at the end of the t_1 conversion when the oscillator is disabled, respectively. Since the first integrating period is digitized during the second slope, the accumulated jitter noise of the second integrating period is covered by that of the first integrating period as $e_j(t_1) = e_j(t_2) + e_j(t_2 \rightarrow t_1)$, where $e_j(t_2 \rightarrow t_1)$ is the accumulated error of the oscillator from the end of the t_2 conversion to the end of the t_1 conversion. Similar to (8), the variance of $e_j(t_2 \rightarrow t_1)$ is determined as $\delta^2(t_2 \rightarrow t_1) = \kappa^2(t_1 - t_2) + \zeta^2(t_1 - t_2)^2$. Therefore, from (9), we have the total oscillator-induced jitter noise power of the conversion determined as

$$\delta^2(V_{\text{in}}) = {V_{\text{ref}}}^2 \frac{(D_1 - D_2)D_2}{{D_1}^4}\theta \tag{10}$$

where θ is defined as $\theta = \kappa^2 D_1/t_d + 2\zeta^2(D_1 - D_2)D_2$. It can be seen from (10) that the maximum oscillator-induced jitter noise power is around $((\kappa^2/4D_1t_d) + (\zeta^2/8)){V_{\text{ref}}}^2$. Assume for example that $\zeta = 5 \times 10^{-5}$ and $\kappa = 10^{-8}$ [$\sqrt{\text{sec}}$], which is more than twice the maximum values from [18], and that $D_1 t_d = 100$ ns, then the maximum oscillator-induced rms jitter noise at the output is $(V_{\text{ref}}/2^{15.3})$. This means that the maximum oscillator-induced rms jitter noise is lower than 1 least significant bit (LSB) for resolutions less than 15.3 bit. Or in other words, in a 12-bit conversion, the oscillator jitter effect can be neglected. Therefore, exploiting this margin in this paper, a differential structure is selected for the oscillator delay units, because it is highly immune to power supply noise, even though its jitter noise is higher than that of the inverter-based ring oscillator [17].

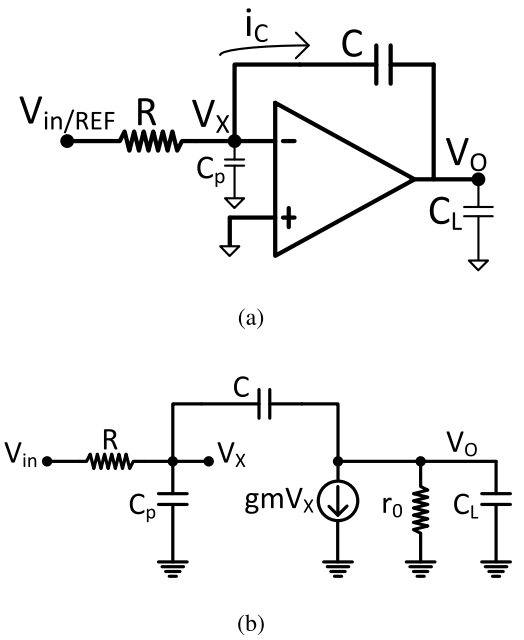


Fig. 6. Schematic of (a) nonideal integrator and (b) integrator equivalent circuit.

In addition, it can be concluded that by converting the t_1 period repetitively in every A/D conversion, also the effect of the oscillator jitter noise is reduced to being negligible. Such repetitive t_1 conversions do not take extra conversion time nor consume more power, because the shared ring oscillator is always enabled for a pulsewidth of t_1 in the second integrating slope to cover all the rising edge moments of the 16 pulses $PULSE_3$ of the 16 columns sharing the ring oscillator.

IV. Impact of Nonidealities

A. Nonideal Opamp

In this section, the impact of the non-ideal opamp on the integrator performance is investigated, gaining in particular a greater insight into the integrator circuit achieving its transient response. Fig. 6(a) shows the schematic of the RC integrator with a non-ideal opamp with finite dc gain A_{dc} and finite gain-bandwidth (GBW). Fig. 6(b) shows the equivalent circuit of the integrator in Fig. 6(a). From the equivalent circuit in Fig. 6(b), the frequency-domain integrator transfer function is

$$\begin{aligned}\frac{V_O(s)}{V_{\text{in}}(s)} &= \frac{-A_{\text{dc}}(1 - s\tau_z)}{A_{\text{dc}}(1 - s\tau_z)s\tau_{\text{int}} + (1 + s\tau_L)(1 + s\tau_{\text{int}})} \\ &= \frac{-A_{\text{dc}}(1 - s\tau_z)}{(1 + s\tau_1)(1 + s\tau_2)}\end{aligned} \tag{11}$$

where A_{dc} is the opamp dc gain; $\omega_z = 1/\tau_z = gm/C$ is the system zero; $\tau_L = r_0(C + C_L)$ and $\tau_{\text{int}} = RC$; and

$\tau_1 \approx 1/\text{GBW}$ and $\tau_2 \approx A\tau_{\text{int}}$. However, the frequency-domain response of the integrator input is $V_{\text{in}}(s) = V_{\text{in}}/s$, because it is intentionally switched at the beginning of the first and the second integrating slopes. Similar to works in [20] and [22]–[24], by taking the inverse Laplace transform [21] of (11), the input voltage, similar to (1), can approximately be determined as

$$\frac{V_{\text{in}}}{V_{\text{REF}}} = \frac{1 - e^{-t_2/\tau_2} + \frac{\tau_1+\tau_z}{\tau_2}e^{-t_2/\tau_1}}{1 - e^{-t_1/\tau_2} + \frac{\tau_1+\tau_z}{\tau_2}e^{-t_1/\tau_1}} \approx \frac{1 - e^{-t_2/\tau_2}}{1 - e^{-t_1/\tau_2}} \approx \frac{t_2}{t_1}\left(1 + \frac{t_1 - t_2}{2A_{\text{dc}}\tau_{\text{int}}}\right). \tag{12}$$

It can be seen from (12) that the conversion is more linear if either A_{dc} or τ_{int} increases. If a maximum nonlinearity of 1% is the design target, the minimum value of the opamp gain A_{dc} must satisfy

$$A_{\text{dc}} > \frac{50t_1}{RC}. \tag{13}$$

The opamp dc gain requirement is relaxed by increasing RC or reducing t_1, which, however, increases the thermal noise, as shown in (7).

Additionally, the removal of the components $(\tau_1 + \tau_z/\tau_2)e^{-t_2/\tau_1}$ and $(\tau_1 + \tau_z/\tau_2)e^{-t_1/\tau_1}$ in (12) is based on the fact that $\tau_2 \gg \tau_1$ and $\tau_2 \gg \tau_z$. While the component e^{-t_1/τ_1} in the denominator can be neglected, because the condition $t_1 \gg \tau_1$ can easily be achieved, the component e^{-t_2/τ_1} in the numerator, however, is significant if t_2 is small enough, resulting in an undesired nonlinearity. Section VI will discuss this issue through the integral nonlinearity (INL) measurement result, showing that the nonlinearity is significant for an input signal around the common-mode voltage. This issue can be eased off by increasing the opamp GBW, at the expense of extra power.

B. Offset Problem

In this section, the offset problem caused by analog circuits is discussed. Assume that the offset voltages of the opamps OP1, 2, and 3 and the comparator in Fig. 2 are V_{O1}, V_{O2}, V_{O3}, and V_{OC}, respectively. In the integration equation, these offset voltages are present as

$$V_{\text{in}} = (V_{\text{REF}} - V_{O2} - V_{O3})\frac{t_2}{t_1} - \left(V_{O1} + V_{O2} + V_{O3} + V_{\text{OC}}\frac{RC}{t_1}\right). \tag{14}$$

It can be seen from (14) that, for CDS signals of the same polarity, the offset value $(V_{O1} + V_{O2} + V_{O3} + V_{\text{OC}}(RC/t_1))$ is removed by the digital CDS operation. Then, the CDS signal can be determined as

$$V_{\text{CDS}} = (V_{\text{REF}} - V_{\text{OS}})\frac{\Delta t_2}{t_1} \tag{15}$$

where $(V_{\text{OS}} = V_{O2} + V_{O3})$; and $\Delta t_2 = t_{22} - t_{21}$ is the CDS timing value of the second integration slope. It can be seen from (15) that the error caused by the offset is similar to the gain error.

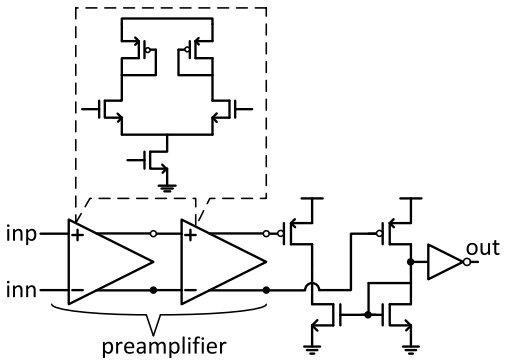


Fig. 7. Schematic of the comparator.

For strong-illumination conversions, since the offset voltages behave oppositely with two signals of opposite polarities, they are canceled and the CDS signal can be determined as

$$V_{\text{CDS}} = (V_P - V_{\text{OS}})\frac{t_{21}}{t_1} + (V_N + V_{\text{OS}})\frac{t_{22}}{t_1}. \tag{16}$$

Therefore, in order to calibrate a dual-polarity DS integrating ADC, both the offset-induced references $(V_P - V_{\text{OS}})$ and $(V_N + V_{\text{OS}})$ are needed to be determined.

For a simpler approach, the autozeroing technique can be applied to opamps OP2 and 3 to suppress the offset voltage V_{OS}. Since this paper has focused on improving the low-noise, high-speed, and low-power performances, the calibration methods and the autozeroing technique have not been implemented.

V. Circuit Implementation

A. Design of the Column ADC

In the designed test chip, the resistor values are programmable in the range of [250 kΩ:2 MΩ], while the capacitor values are in the range of [50 fF:200 fF]. For the sake of design simplicity, the three opamps OP1, OP2, and OP3 in Fig. 2 have the same sizes and are of the 5T structure to obtain a dc gain of 55 dB, which satisfies the condition in (13) with $RC = 200$ ns and t_1 smaller than 2.2 μs. Regardless of the oversampling option, this spares enough design margin for the CDS line time target to be less than 4 μs.

Fig. 7 shows a simplified schematic of the comparator used in the column ADCs. The 2 preamplifier stages, which are designed in the gm_n/gm_p configuration, reduce the offset and the kickback noise effect of the output stage.

B. Digital Back End

Fig. 8 shows the detailed block diagram of the column digital back end. As indicated previously in Fig. 2, the oscillator and the counter are shared by 16 columns. Similar to the pulse P_{COUNT} in Fig. 2, in this design, the phase node P_5, which is equivalent to the node $3n$ of the oscillator in Fig. 4, triggers the counter to operate the coarse counting. In every column, there are registers for the counter output and the oscillator phase states, a multiplexer, and logic blocks. The coarse and fine conversions are, respectively, operated when the counter

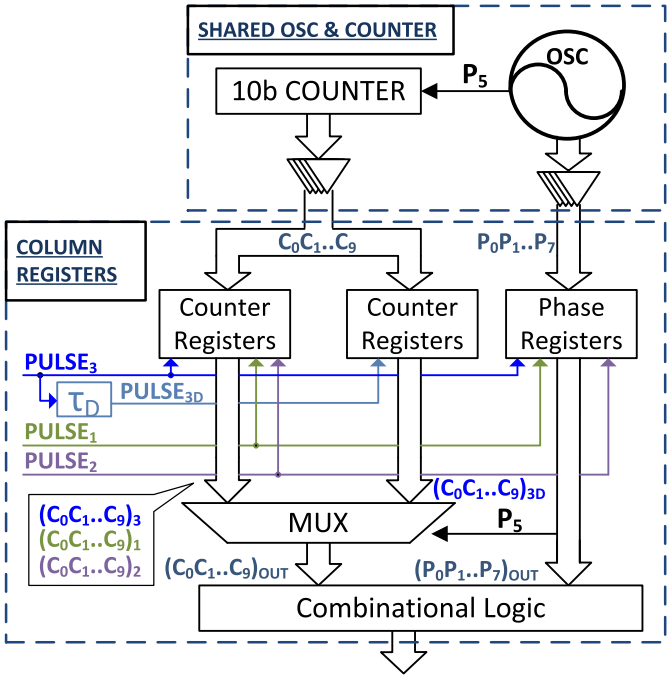


Fig. 8. Simplified block diagram of the column digital back end with the CMC operation.

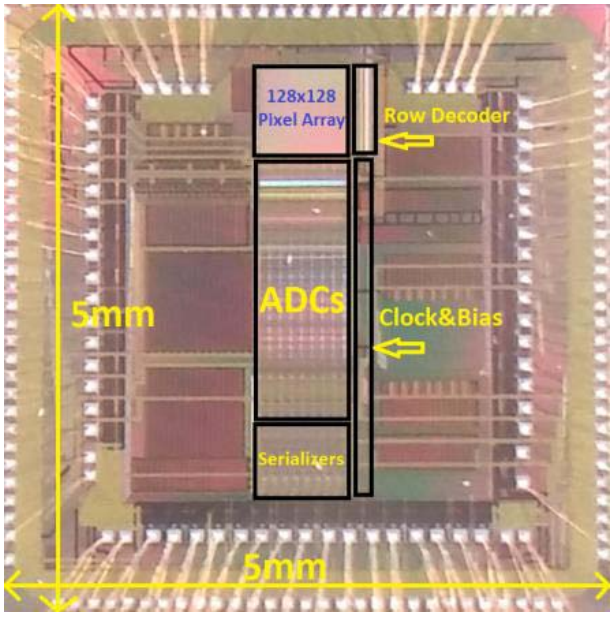


Fig. 9. Die photograph of the imager chip.

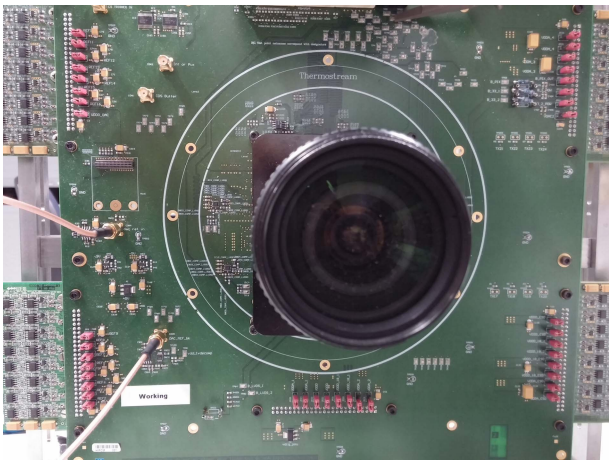
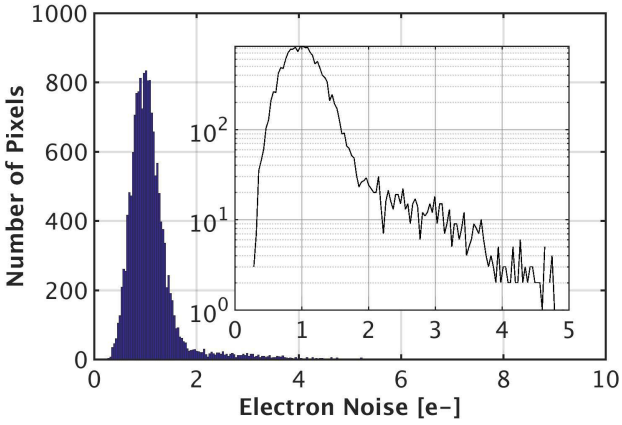


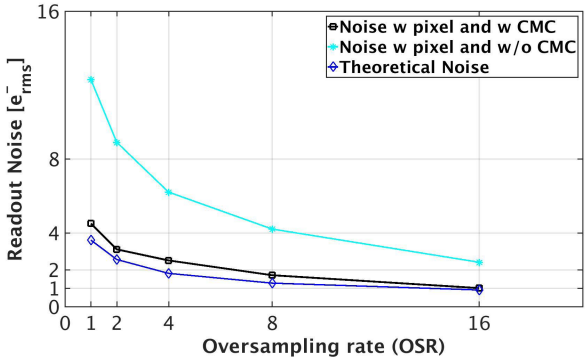
Fig. 10. Designed PCB board and the attached lens for the chip testing.

registers capture the counter outputs and the phase registers capture the oscillator phase nodes. The capturing actions in registers are triggered by the pulses $PULSE_{1,2,3}$. Since the shared counter is designed with 10 bits and the number of phase states is 16, the maximum resolution of one conversion is 13 bit. However, higher resolutions are achieved through the oversampling operation.

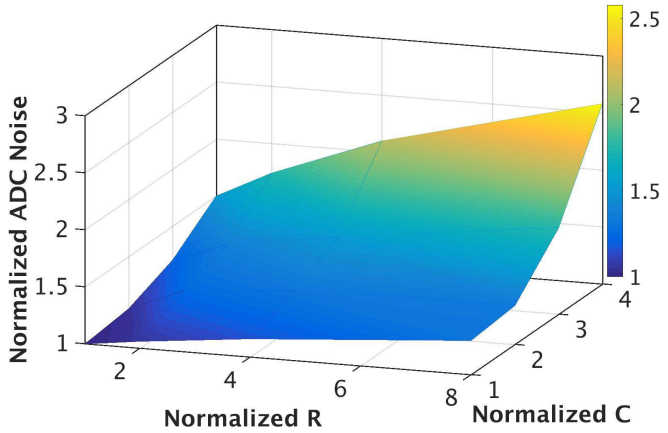
Different from [10] and [31], where the coarse and fine values are recorded when the oscillator is disabled, leaving enough time for the counter to update, in our design a coarse miscounting may occur when $PULSE_3$ captures right after the rising edge of the counting clock P_5 when the counter is likely yet to update. As these results in a conversion error of 16 LSB, in our block column digital circuitry, the coarse miscounting cancellation (CMC) technique is introduced. In our design, since the node $3n$ is used as the coarse counting pulse, the phase states from 3 to 9 in Fig. 4 are considered as sensitive states, in which the counter is highly likely not yet to respond to the rising edge of pulse $3n$. Meanwhile, in the remain states, the counter has enough time to update. The idea of the CMC technique is that in these sensitive states from 3 to 9, the capturing action in the counter register is delayed, leaving enough time for the counter to respond. As shown in Fig. 8, the CMC technique uses the delayed pulse $PULSE_{3D}$ of $PULSE_3$



(a)

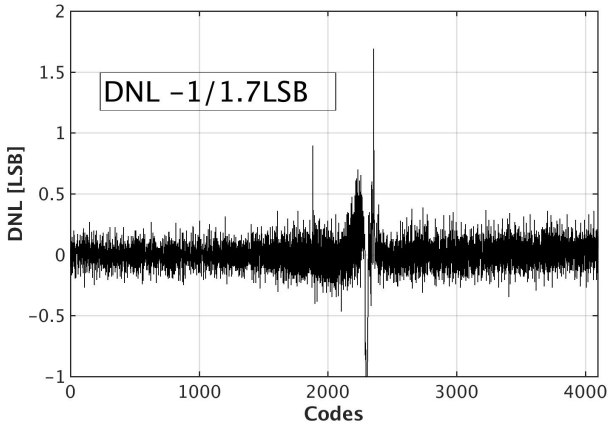


(b)

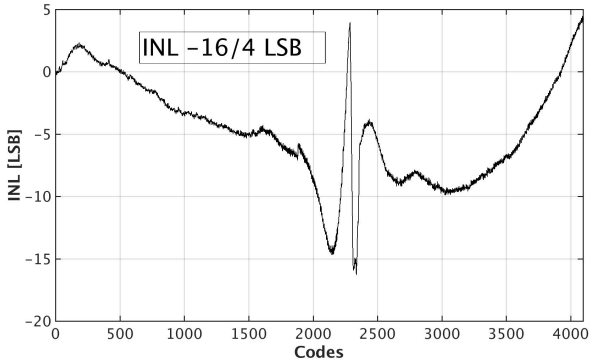


(c)

Fig. 11. (a) Measured noise histogram. (b) Measured readout noise as a function of the OSR with and without CMC. (c) Measured ADC noise as a function of the normalized values of integrator R and C.



(a)



(b)

Fig. 12. (a) Measured DNL. (b) Measured INL.

to capture the counter output as well: when the oscillator node P_5 is captured as "1" by $PULSE_3$, the counter output $(C_0C_1..C_9)_{3D}$ captured by $PULSE_{3D}$ is selected; otherwise, the counter output $(C_0C_1..C_9)_3$ at $PULSE_3$ is selected. When the phase node P_5 is high, the counter has been triggered and its output is supposed to update before P_5 is low. Based on Fig. 4, it can be seen that the counter needs to respond faster than the pulsewidth of P_5, or $7 \times t_d$, where t_d is the oscillator unit delay. In this prototype chip, the oscillator frequency is around 520 MHz, which is equivalent to the condition that t_d is around 120 ps.

VI. Measurement Results and Discussion

Fig. 9 shows the die photograph and core features of the test chip. The chip has been fabricated in a 4M1P 0.18-μm CIS technology, occupying an area of 5×5 mm^2. The chip consists of a 5.5 μm$\times$5.5 μm 128$\times$128 focal plane array with 128 column-parallel DS integrating ADCs. As shown in Fig. 2, each column ADC consists of a column analog part, a column digital part, and a shared digital back end, of which the lengths are, respectively, 460, 1100, and 1000 μm. Since the digital blocks dominate the area budget, their size can significantly be reduced in more scaled CMOS technologies. Fig. 10 shows the measurement setup with a designed ten-layer printed circuit board (PCB) and the attached lens for the chip testing. The reference voltages V_P and V_N and the common-mode voltage V_{CM} are set to 2.1, 1.5, and 1.8 V, respectively.

Fig. 11 shows the noise measurement results and the estimated noise. Fig. 11(a) shows the noise histogram of the prototype chip in both linear and logarithmic displays after 50 frames. For resistor and capacitor values of the integrator in the columns of, respectively, 250 kΩ and 200 fF, a readout

TABLE I
PERFORMANCE COMPARISION WITH THE STATE-OF-THE-ART IMAGERS

References	[7] [TED'09]	[1] [ISSCC'10]	[5] [JSSC'11]	[28] [TED'12]	[29] [ISSCC'15]	[3] [ISSCC'16]	[26] [ISSCC'16]	[27] [TED'16]	[8] [TED'16]	This work
Technology	350nm	90nm	130nm	180nm	90/65nm	130nm	65/45nm	90/65nm	130nm	180nm
Architecture	Monolithic	Monolithic	Monolithic	Monolithic	Stacking	Monolithic	Stacking	Monolithic	Monolithic	Monolithic
ADC types	2-step SS	Pseudo multi-slopes	ISD	2-stage cyclic	SS	Dual-gain SS	3-stage cyclic	2-stage cyclic	PWM-SD	DS integrating
Conv. Gain	46μV/e$^-$	116μV/e$^-$	80μV/e$^-$	63μV/e$^-$	76.6μV/e$^-$	91μV/e$^-$	92μV/e$^-$	93.5μV/e$^-$	54μV/e$^-$	**96μV/e$^-$**
Resolution	11b	10/12b	12b	12b	12b	12b	12b	14b	12b	12b (8 ENOB)
T_{pixel} Frame/s	4μs 700	66μs 6	6.85μs 120	1.93μs 120	- 30	16μs 5	- 240	1.93μs 120	2.7μs 60	**3.8μs** **2056**
Noise	490μV_{rms} 10.6e^-_{rms}	128μV_{rms} 1.1e^-_{rms}	152μV_{rms} 1.9e^-_{rms}	189μV_{rms} 3.0e^-_{rms}	100μV_{rms} 1.3e^-_{rms}	282μV_{rms} 3.5e^-_{rms}	331.2μV_{rms} 3.6e^-_{rms}	337μV_{rms} 3.6e^-_{rms}	65μV_{rms} 1.2e^-_{rms}	**102**μV_{rms} **1**e^-_{rms}
Power	36mW	280mW	180mW	2670mW	532mW	1970mW	3000mW	3200mW	50mW	**49/59mW**[+]
FPA	320×240	8M	2.1M	33M	20.68M	250M	33M	33M	580×450	128×128
FoM [e$^-$.nJ]	7.1	6.4	1.7	2.0	1.1	5.5	1.36	2.9	3.84	**1.4/1.7**[++]

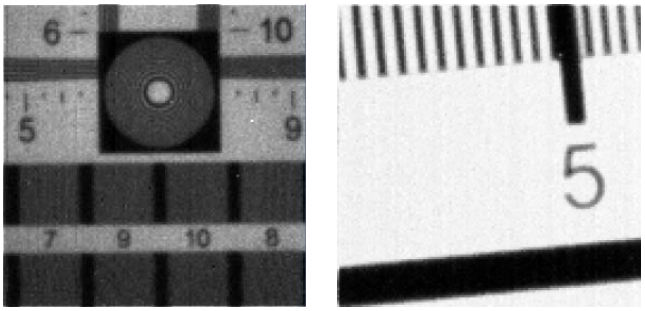
[+] The power values of 49mW and 59mW are without and with the I/O, respectively.

[++] The FoM values of 1.4[e$^-$.nJ] and 1.7[e$^-$.nJ] are without and with the I/O power, respectively.

noise of 102 μV_{rms}, which is approximately equivalent to 1e^-_{rms} with the pixel conversion gain of 96 μV/e$^-$, is obtained with an OSR of 16 within a line readout time of 3.8 μs. The total time for an A/D conversion (OSR = 16) is 1600 ns. Each fractional DS integrating operation takes 95 ns with the first integrating time t_1 of 45 ns. The gap between two adjacent fractional DS integrating conversions is 5 ns. The total integrating time of the first integrating slope is 720 ns and the maximum total integration time t_{int} of the conversion is 1520 ns.

Fig. 11(b) shows the estimated noise and the measured noise as a function of the OSR with and without the CMC technique. It can be seen from Fig. 11(b) that the measured readout noise is effectively suppressed by increasing the OSR. The reason of the noise reduction with multiple oversampling is that, with higher OSR values, the total integrating time gets longer resulting in lower low-pass cutoff frequencies, which are $0.45/t_{\text{int}}$, the LSB becomes smaller, because the bit resolution gets higher, and the noise suppression is stronger, as shown in (7). Additionally, the noise results in Fig. 11(b) show that the high noise due to the coarse miscounting, as discussed earlier, is indeed eliminated by the proposed CMC technique. The transfer gate of the pixel is always kept OFF during the noise measurement. Fig. 11(c) shows the normalized ADC noise measured over the normalized values of R and C of the integrator, mentioned in Section V. It can be seen that the noise is higher when either the integrator resistor R or the capacitor C increases and vice versa, which agrees with (7).

Fig. 12 shows the differential nonlinearity (DNL) and INL performance of the designed DS integrating ADC in 12-bit resolution. The measured DNL in Fig. 12(a) is worst case within $-1/+1.7$ LSB, and is well within ± 0.5 LSB for most of the digital codes. Fig. 12(b) shows the measured INL performance of the ADC. The achieved INL is within $-16/+4$ LSB of the 12-bit resolution, which is equivalent to a nonlinearity of 0.49%, which is sufficient for imager applications. The large spikes in both the DNL and INL plot occur around the input-polarity transition point, where the input signal is slightly either larger or smaller than the integrator common-mode voltage. As discussed earlier in Section IV, this effect can be explained based on (12) where the exponential component $(\tau_1 + \tau_z/\tau_2)e^{-t_2/\tau_1}$ in the numerator is significant for input signals around the common-mode level of the integrator. And when the GBW of the integrator opamp OP3 gets higher, the spikes in the DNL and INL graphs get narrower. A better DNL/INL performance is then achieved, be it at the cost of more power and higher noise, as shown in (7) where the integrator noise rises, because the noise bandwidth of the integrator opamp increases. In other words, there is a direct tradeoff between linearity and power-noise performance. Furthermore, the missing codes occur within 10 LSBs of the 12-bit resolution in the DNL graph. In this design, this middle range is equivalent to the input signal of $(V_P - V_N)/2 = 0.3$ V. The photon shot noise is calculated to be 5.4 mV with the pixel conversion gain of 96 μV/e$^-$. Additionally, if all the missing codes within this 10-LSB range would be fixed to one value, the maximum error of



(a) (b)

Fig. 13. Captured images in (a) low-light and (b) normal-light conditions.

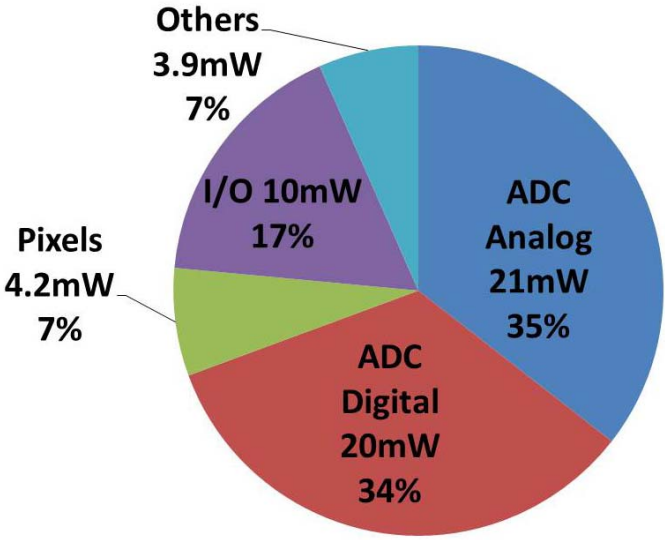


Fig. 14. Breakdown of the power consumption of the imager chip.

them is only 1.4 mV, which is smaller than the photon shot noise by a factor of 4. In this case, the signal-to-noise ratio would only drop from 34 to 33 dB. As a result, these missing codes are not critical. This DNL/INL characterization has been presented here to describe the ADC nonidealities; the missing code issue may not even have been detected if the ADC nonlinearity is demonstrated by scanning the pixel integration time as in [33]. The DNL/INL measurement has been done with integrator resistor and capacitor values of 250 kΩ and 200 fF, respectively.

Fig. 13 shows two images captured by the designed chip. While the picture in Fig. 13(a) is captured at a low light level of 0.1 lx and with a distance to the object of 2 m, the picture in Fig. 13(b) is captured at a normal light level of 10 lx with a distance to the object of 30 cm. At 3.8 μs conversion time, the total power consumption is 49 mW excluding the I/O, and is 59 mW including the I/O. Fig. 14 shows the chip power consumption breakdown. Similar to [5], the figure of merit (FoM) used here is

$$\text{FoM} = \frac{\text{Power} \times \text{Noise } [\text{e}^-_{\text{rms}}]}{\text{Pixels} \times \text{FrameRate}} \times 10^9 \ [\text{e}^-.\text{nJ}]. \qquad (17)$$

The calculated FoM for our design is 1.4 and 1.7 [e$^-$.nJ], respectively, for the cases without and with the I/O power. These are excellent values compared with the state of the art. Table I shows the performance comparison of this paper with published state-of-the-art realizations. The FoM values of the works in [26] and [29] are lower than that of this paper, because they were done in 3-D-stacked architectures of lower technology nodes. The architecture presented in this paper would also achieve a higher conversion speed in more advanced technologies as the stage delay t_d would be lower at a lower power consumption, improving the FoM; indeed the digital parts take the largest portion of the total power consumption.

VII. Conclusion

A DS integrating ADC utilizing the phase-delay-counting principle for column-parallel imager readout circuitry has been presented and verified with an image sensor chip of a 5.5–μm 128 $\times$ 128 pixel array fabricated in a 1P4M 0.18-μm CIS technology. A full analysis of the noise and nonidealities of the circuit gives insight into the circuit design and performance. The presented ADC suppresses the readout noise with a low-pass filtering characteristic. The readout noise is lower with a longer integration time t_1 due to the lower low-pass cutoff frequency. When the integrator RC value is higher, the ADC is more linear, but the noise performance gets worse. By increasing the GBW of the integrator opamp, the nonlinearity for input voltage levels around the integrator common-mode voltage is reduced, however, at the cost of increased noise. The measurement results have shown that a readout noise value of 1e^-_{rms} is achieved by combining the DS integrating conversion with the oversampling operation. With the pixel conversion gain of 96 μV/e$^-$, FoM values of 1.4 and 1.7 [e$^-$.nJ] have been achieved without and with the I/O power, respectively. These are excellent values compared to the state of the art. Additionally, the CMC method has been demonstrated to solve the coarse miscounting errors caused by the slow response of the counter.

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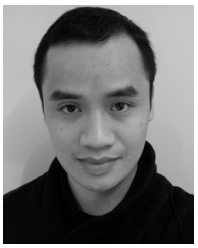

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