

A Low-Jitter Ring-Oscillator Phase-Locked Loop Using Feedforward Noise Cancellation With a Sub-Sampling Phase Detector

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Abstract—Ring-oscillator (RO)-based phase-locked loops (PLLs) are very attractive for system-on-chip applications for their compactness and tuning range, but suffer from high jitter and supply noise sensitivity. This paper presents a sub-sampling phase detector (SSPD)-based feedforward noise cancellation (FFNC) technique to improve these drawbacks of the RO PLL. The FFNC scheme utilizes the already available SSPD output to perform cancellation with high sensitivity while utilizing low power and area overhead. The 2- to 2.8-GHz RO PLL proof-of-principle prototype occupies 0.022 mm² active area in 65 nm CMOS; it achieves a 633 fs rms jitter at 2.36 GHz with 5.86 mW power consumption and an figure of merit (FOM_{jitter}) of -236.3 dB. The cancellation reduces the jitter by 1.4x, the phase noise by 10.2 dB to -123.5 dBc/Hz at 300-kHz offset, and the RO supply sensitivity by 19.5 dB for a 1 mV_{pp} 100-kHz noise tone on the RO supply.

Index Terms—CMOS, feedforward, low area, low jitter, noise cancellation, phase-locked loop (PLL), RF, ring oscillator (RO), sub-sampling.

I. INTRODUCTION

PHASE-LOCKED loops (PLLs) are critical building blocks in modern system-on-chip (SoC) systems and it is very desirable to design PLLs with low jitter in a power-and area-efficient manner.

Due to the various device noise sources in the PLL, the zero crossings of the output clock deviate from the ideal transition points a.k.a. jitter. Looking at the spectrum of the output clock, the noise results in phase-noise side bands around the center frequency and can be divided into in-band and out-of-band components, depending on the noise frequency being smaller or larger than the PLL bandwidth (BW). The in-band component is usually dominated by the noise from the tri-state phase-frequency detector (PFD)/charge pump (CP) and reference (REF) and the out-of-band noise components are dominated by the voltage-controlled oscillator (VCO) noise. For low-jitter applications, *LC*-based VCOs with good intrinsic phase-noise performance have been typically used.

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The good phase-noise performance of *LC* VCOs allows the usage of a small loop BW resulting in reduced in-band noise. The *LC* oscillator is also preferred for its high supply noise immunity. However, they occupy a large area and have a low tuning range. This makes ring oscillators (ROs) an attractive alternative given their small size and high tuning range, but ROs suffer from poor phase noise and supply sensitivity, making their usage in low jitter applications challenging. The focus of this paper is to address these two issues of RO PLL to make them a viable substitute for *LC* PLL.

We present an example of the phase-noise performance of a typical PFD-based Type-II RO PLL [1] shown in Fig. 1(a). The phase noise plot with $F_{\text{ref}} = 49.15$ MHz from a crystal oscillator (XTAL), divide ratio $N = 48$, output frequency $F_{\text{out}} = 2.36$ GHz, loop BW = 2.5 MHz, and an RO with phase noise of -100 dBc/Hz at a 1-MHz offset is shown in Fig. 1(c). The PFD/CP noise dominates the in-band noise and the RO noise dominates the out-of-band noise. The in-band component can be reduced by adopting a sub-sampling phase detector (SSPD) [2]–[10], as shown in Fig. 1(b), and now the in-band noise is dominated by the XTAL, which can be as low as -125 dBc/Hz. To further reduce the phase noise, the PLL BW has to be increased to suppress the RO noise. However, the BW of a Type-II PLL is limited to approximately $F_{\text{ref}}/10$ for stability concerns [1] and is often kept smaller than $F_{\text{ref}}/20$ to minimize the REF spurs [11]. The attempt to increase F_{ref} for BW enhancement is, however, restricted to about 100 MHz by the availability of clean quartz crystals. For this reason, our analysis during the remainder of this paper uses the above-mentioned example PLL parameters with F_{ref} of 49.15 MHz, unless specified otherwise. The phase-noise plot for the SSPD PLL with these parameters is shown in Fig. 1(c). Note that the XTAL is the dominant noise source up to 25 kHz and at higher noise frequencies, the RO noise dominates and gives the phase noise plot a hump like shape.

This band from 25 kHz to 5 MHz contributes about 75% of the overall jitter making the noise attenuation in this band essential for the jitter reduction. To reduce the noise in this band, a number of design techniques can be used. In [12], the PLL is cascaded with a low noise sub-sampling delay-locked loop (DLL) that filters the RO noise. This additional DLL is a negative feedback system that is more immune to process, voltage and temperature (PVT), but it requires an additional DLL filter. The DLL also needs an additional SSPD to sample the PLL output at a high rate, which consumes

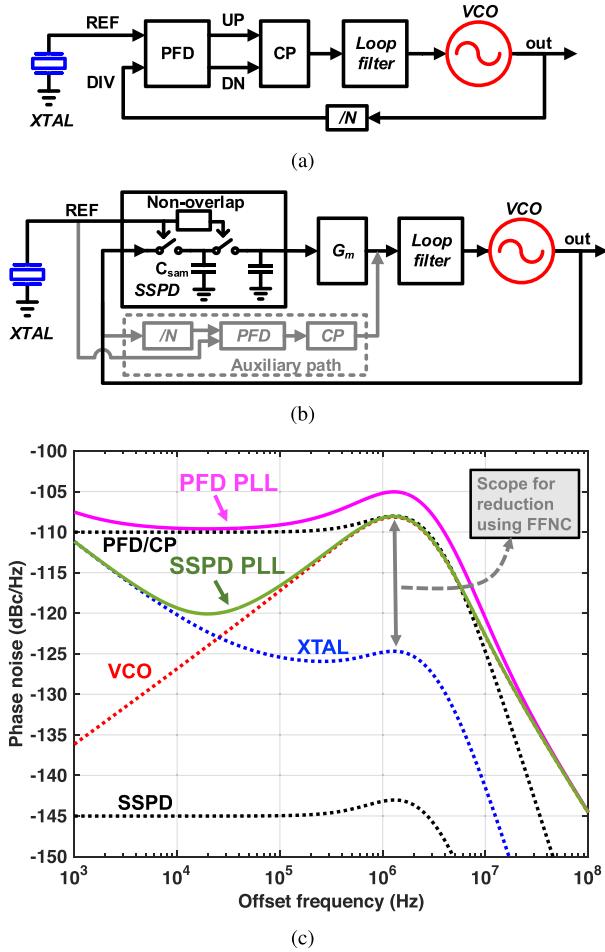


Fig. 1. (a)Traditional RO-based tri-state PFD PLL. (b)RO-based SSPD PLL. (c) Phase noise plot for both the architectures for an $F_{\text{ref}} = 49.15$ MHz, $N = 48$, PLL BW = 2.5 MHz, and an RO with a phase noise of -100 dBc/Hz at a 1-MHz offset showing the need for FFNC.

additional power. In [13], the PLL loop architecture is switched to a Type-I architecture to ease the BW requirements and a BW of $F_{\text{ref}}/2$ is achieved. In [14] and [15], the incoming REF frequency is doubled using a frequency doubler before giving it to the PLL loop, effectively doubling the achievable loop BW.

In this paper, we explore feedforward noise cancellation (FFNC) [16], which can be used in tandem or independent of the above-mentioned techniques. In FFNC, the output noise is extracted and canceled in a feedforward fashion outside of the PLL loop, thus making it possible to overcome the PLL-BW limitations. In our approach, we demonstrate that the already available PLL PD can be used for noise extraction, and the PD output can be fed directly to a voltage-controlled delay line at the PLL output to perform FFNC with very low area or power overhead [17]. The key feature of the presented SSPD-based FFNC PLL is it can simultaneously achieve low PD noise (by using SSPD) and low RO noise contribution (by using FFNC).

The other major concern in RO PLLs is their high susceptibility to supply noise due to the sensitivity of the RO frequency to the supply voltage [18]. The problem is particularly severe in modern SoC systems where the PLL is in the vicinity

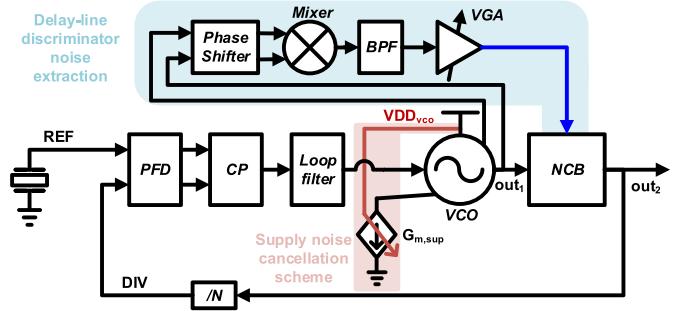


Fig. 2. PLL with delay-line discriminator-based FFNC [16] scheme and conventional supply noise-cancellation scheme [24].

of constantly switching digital circuits. To minimize these disturbances on the PLL supply, voltage regulation has been traditionally used [19]–[22]. In addition to supply regulation, further reduction can be achieved by employing supply noise cancellation [18], [23]–[26], which can either eliminate the need for regulation or relax the stringent power supply rejection ratio and BW requirements for the regulators. These cancellation schemes (Fig. 2) typically provide an additional cancellation path from the VCO supply to the output. The gain of this cancellation path ($G_{m,\text{sup}}$) is adjusted to null the effect of supply noise at the PLL output.

In the FFNC scheme proposed here, we will demonstrate that the PD extracts the phase noise due to the supply noise as well as due to the device noise and cancels both of them from the PLL output.

This paper is organized as follows. Section II gives a brief overview of SSPD-based PLLs. In Section III, we compare existing FFNC architectures with the proposed SSPD-based FFNC. Section IV gives a detailed time-domain and frequency-domain analysis of SSPD-based phase-noise and supply noise cancellation. Sections V and VI discuss the circuit implementation and measurement results, respectively. The conclusions follow in Section VII.

II. SUB-SAMPLING-PHASE-DETECTOR-BASED PLLS

In a traditional tri-state PFD-based PLL the VCO output is divided by using a frequency divider to obtain the feedback signal DIV. The PFD/CP then compares DIV and the reference, REF, to generate the error current pulses that are filtered and then negatively fed back onto the VCO tuning port. Due to the feedback divider, the REF and PFD/CP noise get multiplied by N^2 [2]. For $N = 48$, the N^2 noise gain results in a 34 dB enhancement of noise from these blocks. In an SSPD PLL, the divider in the feedback path is eliminated. Now the PD/CP noise does not get multiplied by N^2 , thus resulting in the noise on REF becoming the dominant in-band contributor [2].

In a Type-II SSPD PLL in lock, the VCO edges are aligned with the REF edges. Any deviation in the VCO phase shifts the VCO edge and the SSPD samples a non-zero voltage. Based on this voltage, the transconductor (G_m) generates an error current which is integrated by the loop-filter capacitor. This integrated voltage now controls the VCO and locks the PLL. The noise from the SSPD sampling switch is calculated as

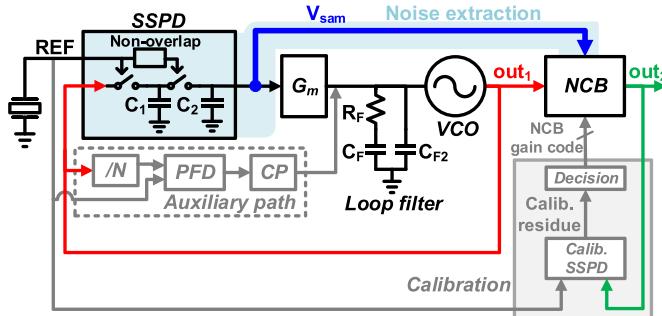


Fig. 3. Proposed SSPD-based FFNC PLL with calibration scheme for accurate cancellation; the output of the SSPD is used to drive the NCB; the auxiliary path used to guarantee locking to the correct REF harmonic is also shown.

–145 dBc/Hz (using [2]) for a small C_{sam} of 100 fF and a VCO amplitude (A_{vco}) of 0.5 V. With such low SSPD noise, the noise in REF, which is multiplied by N^2 , becomes the dominant in-band noise contributor. The REF noise varies with the quality of the crystal, but a standard available –160 dBc/Hz crystal has its noise amplified by 34 dB [20 log(48)] resulting in a in-band noise of –126 dBc/Hz. This value is at least 10 dB better than the in-band noise achieved in similar PLLs using PFD/CP architecture [3].

Without feedback divider the SSPD PLL can potentially lock to any harmonic of REF. To lock to the correct harmonic, an auxiliary PLL with a divider, PFD and CP is typically used in parallel to the SSPD loop [2]. The auxiliary loop can be disabled after the VCO locks to the correct frequency to eliminate its power consumption and noise.

III. PROPOSED FEEDFORWARD NOISE-CANCELLATION LOOP

The proposed FFNC and its operation in the time domain are shown in Fig. 3. To reduce the jitter of output of the RO, out_1 , we need to first measure the noise. The SSPD extracts the noise information and feeds it to the noise cancellation block (NCB) which consists of a voltage-controlled delay. The delay introduced by the NCB cancels the jitter in out_1 and generates a signal out_2 with lower jitter. To illustrate that the proposed approach is very compact and high performance, we now first compare this approach to earlier work, before going into a detailed analysis.

FFNC in an RO PLL has been previously demonstrated in [16] but the noise measurement was performed using a delay-line discriminator (DLD) as shown in Fig. 2. Two phases of the RO are passed through a cascade of a phase shifter, mixer, bandpass filter (BPF), and variable gain amplifier (VGA) to generate the error signal. This error signal is used by the NCB to cancel the noise from out_1 . This noise measurement approach requires substantial additional circuitry, consuming area and power. In contrast, in the proposed SSPD-based FFNC, the already available output of the SSPD is directly given to the NCB for cancellation, since it contains all the necessary jitter information. The SSPD, as part of the PLL feedback loop, already extracts the error present in the VCO output by comparing it with the low-jitter REF. This extracted

error can perform the FFNC directly, thus making this a very low area and power overhead solution.¹

The SSPD FFNC scheme also offers high noise-measurement gain in comparison to the delay-line discriminator-based FFNC at low offset frequencies. We use the same PLL parameters as in the previous section to calculate the noise extraction gain at an offset frequency $F_{\text{off}} = 1$ MHz. In the DLD-based FFNC, assuming the phase shifter provides two orthogonal sinusoidal signals of 1-V voltage swing, the phase-to-voltage gain of the mixer can be calculated as $(F_{\text{off}}/F_{\text{out}})\pi/4$ V/rad. This gives a gain of –69.5 dBV/rad. To compensate for this attenuation, a high-gain VGA is needed to amplify the extracted noise before applying it to the NCB. In the proposed SSPD-based FFNC, the noise-measurement phase-to-voltage gain from VCO output to SSPD output is equal to the SSPD gain, $K_{f,\text{SSPD}}$ (in V/rad), which is equal to A_{vco} V/rad [2]. This translates to –6 dBV/rad for a A_{vco} of 0.5 V. Because of this high gain, the output of the SSPD can be directly applied to the NCB without the need for a high-gain VGA. This high gain basically stems from the fact that the REF samples the high slew rate VCO signal [10]. This high gain offers high sensitivity which is only limited by the REF noise, multiplied by N^2 , which can be as low as –126 dBc/Hz as discussed earlier.

The proposed FFNC approach could in principle also be implemented in a PFD-based PLL but the noise extraction gain is smaller due to the divider in the extraction path. The SSPD scheme has the additional advantage of readily providing a sampled voltage as its output which can be conveniently used to control the NCB. In a PFD, the phase error is captured as the pulsewidth difference between the UP and DN pulses, which needs further processing to generate the NCB control voltage.

IV. ANALYSIS OF THE PROPOSED FFNC

A. Time-Domain Analysis

Modeling the FFNC operation in time domain gives us insights on the NCB requirements for cancellation. The output of the VCO is a clock transitioning with a slope of $K_{t,\text{SSPD}}$ (in V/s) as shown in Fig. 4. After the Type-II PLL locks, when no noise is present, the SSPD driven by REF samples a zero voltage to maintain steady state. In the presence of noise, assume the VCO's crossing is perturbed by ΔT_{VCO} as shown in Fig. 4. Now, the SSPD samples a non-zero voltage V_{sam} given by $V_{\text{sam}} = K_{t,\text{SSPD}} \cdot \Delta T_{\text{VCO}}$. This V_{sam} contains the information regarding the extent of perturbation in the VCO output and can be used to move the edge back by ΔT_{VCO} . This is achieved by having V_{sam} control the delay from the variable delay line in the NCB. When the voltage-to-delay conversion gain of the NCB is $G_{t,\text{NCB}}$ (in s/V), the delay introduced by the NCB, ΔT_{NCB} , is given

¹A related approach has been used to cancel the effect of phase noise in an I/Q receiver [27]. There, a sub-sampling PLL is used to generate the local oscillator for demodulation. The digital sub-sampling time-to-digital converter output of the PLL is used in the baseband circuitry to correct the constellation points resulting in improved error vector magnitude.

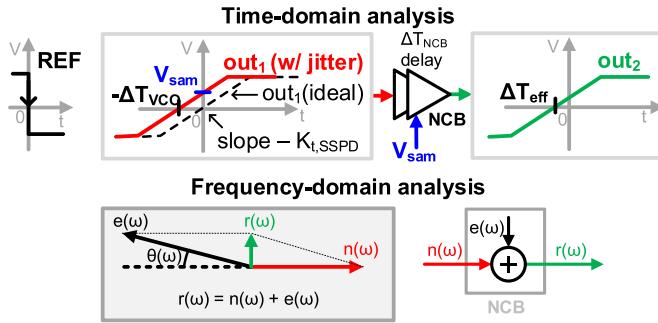


Fig. 4. Time-domain and frequency-domain analysis of the proposed noise cancellation scheme.

by $\Delta T_{\text{NCB}} = T_0 + G_{t,\text{NCB}} \cdot K_{t,\text{SSPD}} \cdot \Delta T_{\text{VCO}}$ where T_0 is the constant propagation delay associated with the NCB. The zero crossing of the output of the NCB is now effectively shifted by a total amount $\Delta T_{\text{eff}} = \Delta T_{\text{NCB}} - \Delta T_{\text{VCO}}$ given by

$$\Delta T_{\text{eff}} = T_0 + (G_{t,\text{NCB}} \cdot K_{t,\text{SSPD}} - 1) \cdot \Delta T_{\text{VCO}}. \quad (1)$$

By ensuring $G_{t,\text{NCB}} = 1/K_{t,\text{SSPD}}$, the jitter due to ΔT_{VCO} is canceled and ΔT_{eff} becomes a fixed constant T_0 .

B. Frequency-Domain Analysis of FFNC

Studying the FFNC in the frequency domain provides further insight into the gain requirements from the NCB and amount of permissible phase shift (delay) that can be tolerated in the cancellation path.

1) Requirements for Noise Cancellation: To completely cancel a noise phasor $n(\omega)$, a phasor $e(\omega)$ with the same magnitude and opposite phase needs to be added as shown in Fig. 4. The resultant phasor after cancellation $r(\omega)$ is given by $r(\omega) = n(\omega) + e(\omega)$. The magnitude of $r(\omega)$ is given by $|r(\omega)| = (\|n(\omega)\| - |e(\omega)| \cos(\theta(\omega)))^2 + [|e(\omega)| \sin(\theta(\omega))]^2)^{1/2}$. In practice, it is relatively easy to maintain $|n(\omega)| \approx |e(\omega)|$, however, a phase error $\theta(\omega)$, is harder to avoid. Now $|r(\omega)|$ can be approximated as

$$|r(\omega)| \approx |n(\omega)|\sqrt{2 - 2 \cos(\theta(\omega))}. \quad (2)$$

We obtain a net reduction as long as $|r(\omega)| < |n(\omega)|$ which translates to $(2 - 2 \cos(\theta(\omega)))^{1/2} < 1$ or $|\theta(\omega)| < 60^\circ$. This criterion will be used to determine the BW of cancellation once we model the additional phase shift introduced in the cancellation path.

2) Phase-Domain Model for FFNC PLL: The phase-domain model of the proposed SSPD FFNC PLL, which is largely based on the model developed in [2], is shown in Fig. 5. The phase noise before and after cancellation are denoted by $\phi_{\text{out}1}$ and $\phi_{\text{out}2}$, respectively. Before we analyze the individual noise contributions to $\phi_{\text{out}1}$ and $\phi_{\text{out}2}$, we define commonly used transfer functions and observe their behavior as a function of frequency. The SSPD, shown in Fig. 6, is realized as a double switch sampler for reasons discussed in Section V. The transfer function of the PD has to take into account the charge sharing between the capacitors C_1 and C_2 and the sample/hold

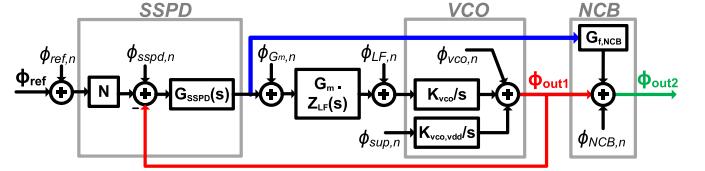


Fig. 5. Phase-domain model of the PLL with the proposed SSPD-based FFNC shown in Fig. 3.

action of the PD. An empirical formula for the SSPD transfer function G_{SSPD} , similar to the one derived in [11], is

$$G_{\text{SSPD}}(j\omega) = \frac{K_{f,\text{SSPD}}}{1 + \frac{j\omega}{C_1 F_{\text{ref}}/C_2}} e^{(-j\pi\omega/\omega_{\text{ref}})} \frac{\sin(\pi\omega/\omega_{\text{ref}})}{(\pi\omega/\omega_{\text{ref}})}$$

and $G_{\text{SSPD}}(j\omega) \approx K_{f,\text{SSPD}}$ for $\omega \ll \omega_{\text{ref}}$. The loop gain of the PLL, $\text{LG}(j\omega)$, is

$$\text{LG}(j\omega) = G_{\text{SSPD}}(j\omega) \cdot G_m \cdot Z_{\text{LF}}(j\omega) \cdot \frac{K_{\text{vco}}}{j\omega}. \quad (3)$$

The PLL BW ω_{bw} is the frequency where the loop gain $|\text{LG}(j\omega)| = 1$ and $|\text{LG}(j\omega)|$ can be approximated as $\gg 1$ for $\omega \ll \omega_{\text{bw}}$, and ≈ 0 for $\omega \gg \omega_{\text{bw}}$. The cancellation path gain $G_{\text{can}}(j\omega)$, which is the gain from the SSPD input to $\phi_{\text{out}2}$ via the SSPD and NCB is given by

$$G_{\text{can}}(j\omega) = G_{\text{SSPD}}(j\omega) \cdot G_{f,\text{NCB}} \quad (4)$$

where $G_{f,\text{NCB}}$ (in rad/V) is the voltage-to-phase gain of the variable-delay line in the NCB

When $G_{f,\text{NCB}} = 1/K_{f,\text{SSPD}}$, $G_{\text{can}}(j\omega)$ can be approximated as 1 for $\omega \ll \omega_{\text{ref}}$, and 0 for $\omega \gg \omega_{\text{ref}}$. For $C_1 = C_2$ the magnitude and phase response of G_{can} is shown in Fig. 7(a). Based on (2), the effective noise cancellation BW is calculated as $\omega_{\text{ref}}/7.8$, i.e., the frequency where the phase shift reaches -60° .

We now derive two Transfer functions (TFs) for each noise source $\phi_{\text{name},n}$ shown in Fig. 5: one to $\phi_{\text{out}1}$, called $\text{TF}_{\text{name},1}$, and one to $\phi_{\text{out}2}$, called $\text{TF}_{\text{name},2}$.

a) SSPD and REF noise contribution:

$$\begin{aligned} \text{TF}_{\text{sspdi},1}(j\omega) &= \frac{\text{LG}(j\omega)}{1 + \text{LG}(j\omega)} \\ \text{TF}_{\text{sspdi},2}(j\omega) &= \text{TF}_{\text{sspdi},1}(j\omega) + \frac{G_{\text{can}}(j\omega)}{1 + \text{LG}(j\omega)}. \end{aligned} \quad (5)$$

Both the SSPD noise transfer functions for an ω_{bw} of $\omega_{\text{ref}}/20$ are shown in Fig. 7(b). At lower ω , the SSPD noise passes directly to both outputs without multiplication with N [2]. At higher ω , the SSPD noise contribution to $\phi_{\text{out}1}$ is filtered by the low-pass loop transfer function, but the SSPD noise contribution to $\phi_{\text{out}2}$ is higher (for $\omega > \omega_{\text{ref}}/10$) due to the presence of the additional term $G_{\text{can}}(j\omega)/(1 + \text{LG}(j\omega))$ stemming from the direct coupling of the SSPD noise to $\phi_{\text{out}2}$ via the feedforward path. At these frequencies $\omega > \omega_{\text{bw}}$, the additional term can be approximated to $G_{\text{can}}(j\omega)$ which has a magnitude response shown in Fig. 7(a). It is observed that even with this additional coupling at high frequencies, the SSPD noise has negligible impact on the output phase noise as it

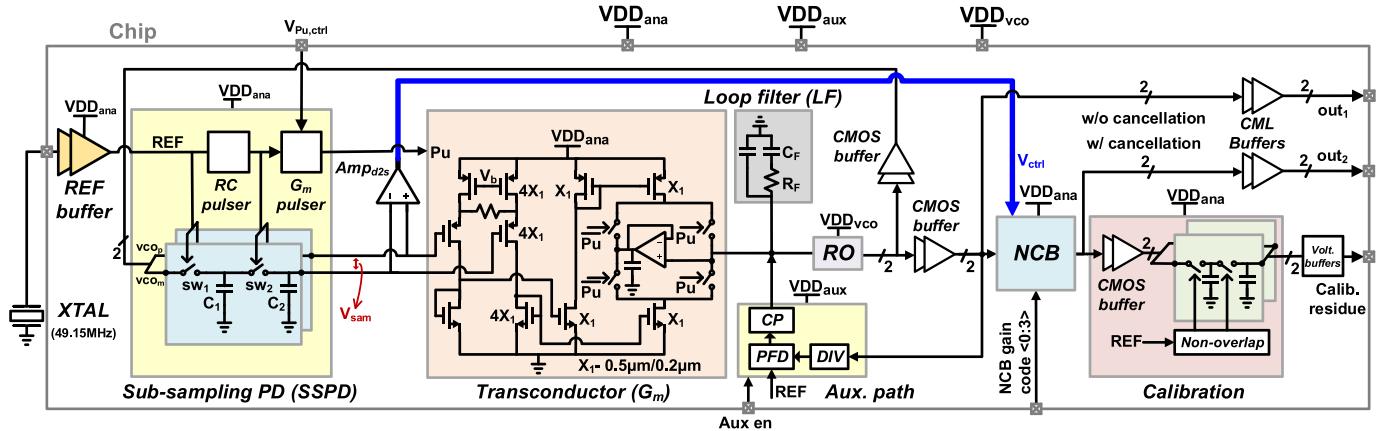


Fig. 6. Prototype PLL chip circuit diagram of the proposed subsampling PLL with FFNC.

is dominated by the VCO contribution at these frequencies [see Fig. 1(c)].

The noise sources of the XTAL and the REF buffer both contribute to the noise in the REF clock $\phi_{ref,n}$. The REF noise transfer functions are $TF_{ref,1}(j\omega) = N \cdot TF_{sspd,1}(j\omega)$ and $TF_{ref,2}(j\omega) = N \cdot TF_{sspd,2}(j\omega)$. The TF's have the same shape as the SSPD TFs and only vary by a factor of N . Because of this multiplication factor N , the REF contributes more noise than the SSPD and ultimately limits the amount of attenuation that can be achieved by using the proposed FFNC scheme.

b) VCO noise contribution:

$$\begin{aligned} TF_{vco,1}(j\omega) &= \frac{1}{1 + LG(j\omega)} \\ TF_{vco,2}(j\omega) &= TF_{vco,1}(j\omega) (1 - G_{can}(j\omega)). \end{aligned} \quad (6)$$

The VCO noise transfer functions for an ω_{bw} of $\omega_{ref}/20$ are shown in Fig. 7(b). The VCO noise is suppressed by a factor of $1 - G_{can}(j\omega)$ at out_2 . $TF_{vco,1}$ has a high pass response with ω_{bw} as its cutoff frequency. The low-frequency roll-off in $TF_{vco,1}$ is determined by the PLL loop order. The PLL loop architecture is generally limited to two integrators owing to stability issues making a sharper in-band roll-off transfer function not possible. However, with cancellation, a higher roll-off is achieved in $TF_{vco,2}$ as shown in Fig. 7(b). This results in higher attenuation of the VCO noise at out_2 . This higher attenuation is achieved up to $\omega_{ref}/7.8$ as predicted by the cancellation transfer function (G_{can}) analysis performed earlier [see Fig. 7(a)]. After $\omega_{ref}/7.8$, there is an increase of about 2 dB (upto ω_{ref}) in VCO contribution due to FFNC. This increase, however, is not a major concern from a integrated jitter perspective as long as ω_{ref} is high enough to make the VCO phase noise low at these frequencies.

c) Loop-filter noise contribution: For modeling simplicity, the loop filter resistor noise is referred to the VCO input (similar to [2]). This noise has the following transfer functions:

$$\begin{aligned} TF_{LF,1}(j\omega) &= \frac{K_{vco}/j\omega}{1 + LG(j\omega)} \\ TF_{LF,2}(j\omega) &= TF_{LF,1}(j\omega) (1 - G_{can}(j\omega)) \end{aligned} \quad (7)$$

the noise undergoes a suppression of $1 - G_{can}(j\omega)$ at out_2 , which can be leveraged to minimize the PLL area. The loop-filter zero capacitor C_F is typically the largest component [28], [29], so to minimize area, C_F has to be decreased while R_F^2 has to be increased to maintain the same compensation zero location, G_m has to be decreased to maintain the same PLL loop dynamics. However, this increases the noise contribution from R_F . However, with the FFNC cancellation of this resistor noise, the net noise contribution from R_F can be brought down back to the original value. Example for the SSPD PLL parameters discussed earlier, the loop filter noise contribution for an R_F of 4 and 20 K Ω is shown in Fig. 7(c). The loop filter noise contribution peak for a R_F of 4 K Ω is -125 dBc/Hz. For an R_F of 20 K Ω the capacitor can be reduced by 5 \times , from 50 to 10 pF, but the phase noise increases by 7 dB at out_1 . However, thanks to the cancellation the noise contribution peak is brought down to -124 dBc/Hz at out_2 after FFNC as shown in Fig. 7(c). Therefore, a PLL using FFNC can be designed with a 5 \times smaller filter zero capacitor in comparison to a PLL without FFNC.

d) Noise-cancellation-block contribution: The NCB noise directly couples to the output and has the transfer functions $TF_{ncb,1}(j\omega) = 0$ and $TF_{ncb,2}(j\omega) = 1$. This calls for an NCB design whose noise is non-dominant compared to other noise sources after cancellation.

e) Summary of noise cancellation and calibration: The proposed FFNC technique reduces the VCO noise with an effective BW of $\omega_{ref}/7.8$, targeting the frequency band where the majority of VCO noise contribution appears. In addition, the FFNC scheme also cancels the loop filter resistor noise enabling the reduction of loop filter area without net noise penalty. The REF noise sets the minimum achievable noise floor after cancellation and the REF crystal and buffer have to be chosen appropriately for maximum performance. For successful noise cancellation it is essential to have the cancellation path gain $G_{can} = 1$. To calibrate this gain, we utilize the supply noise cancellation properties of this FFNC scheme discussed below.

²The designer has to take into account the increase in REF spur associated with increase in R_F while designing.

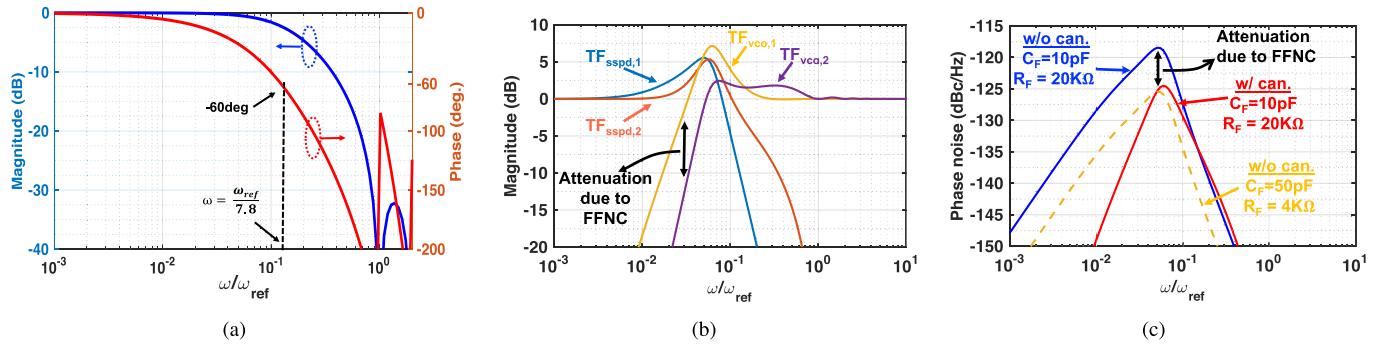


Fig. 7. (a) Bode plot of cancellation path transfer function $G_{\text{can}}(j\omega)$ showing the cancellation BW, i.e., the frequency where the phase reaches -60° . (b) Magnitude plot showing the transfer functions for SSPD (before cancellation— $\text{TF}_{\text{ssdp},1}$ and after cancellation— $\text{TF}_{\text{ssdp},2}$) and VCO (before cancellation— $\text{TF}_{\text{vco},1}$ and after cancellation— $\text{TF}_{\text{vco},2}$). (c) PLL loop filter optimization achieved by using FFNC—PLL loop filter phase noise contribution based on the PD model showing similar noise performance between a loop filter with a large 50-pF capacitor before cancellation and a filter with a small 10-pF capacitor after cancellation.

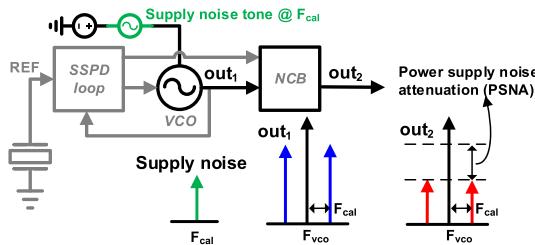


Fig. 8. Illustration of supply noise-induced spurs in the PLL output. The FFNC scheme reduces the spur by an amount shown as PSNA.

C. Supply Noise Cancellation

A supply noise tone at a frequency F_{cal} results in side bands around the VCO frequency in the output spectrum shown in Fig. 8. The SSPD extracts this spurs along with other noise present in the VCO output and then cancels the spurs via the NCB resulting in power supply noise attenuation (PSNA). The supply noise transfer functions (Fig. 5) for an RO are

$$\begin{aligned} \text{TF}_{\text{sup},1}(j\omega) &= \frac{K_{\text{vco,vdd}}/j\omega}{1 + \text{LG}(j\omega)} \\ \text{TF}_{\text{sup},2}(j\omega) &= \text{TF}_{\text{sup},1}(j\omega)(1 - G_{\text{can}}(j\omega)) \end{aligned} \quad (8)$$

where $K_{\text{vco,vdd}}$ is the voltage-to-frequency gain from the VCO supply to its output. It is observed that the VCO supply noise contribution is also suppressed by a factor of $1 - G_{\text{can}}(j\omega)$ due to cancellation.

D. FFNC Calibration

The SSPD gain terms $K_{t,\text{SSPD}}$ (in V/s) and $K_{f,\text{SSPD}}$ (in V/rad) are related as $K_{f,\text{SSPD}} = K_{t,\text{SSPD}}/2\pi F_{\text{out}}$. Also the NCB gain terms $G_{t,\text{NCB}}$ (in s/V) and $G_{f,\text{NCB}}$ (in rad/V) are related as $G_{f,\text{NCB}} = 2\pi F_{\text{out}} G_{t,\text{NCB}}$. For effective cancellation both the time-domain and phase-domain analysis show the same requirements, i.e., $G_{t,\text{NCB}} = 1/K_{t,\text{SSPD}}$ or $G_{f,\text{NCB}} = 1/K_{f,\text{SSPD}}$.

Therefore, to achieve effective cancellation we apply a foreground calibration scheme to digitally program $G_{f,\text{NCB}}$ that exploits the fact that the optimal phase noise and supply noise cancellation require the same condition, i.e., $G_{\text{can}} \approx 1$ or $G_{f,\text{NCB}} = 1/K_{f,\text{SSPD}}$. During calibration, a low-frequency

test tone at F_{cal} is applied to the supply (Fig. 8). The resulting spurs in out_2 at $F_{\text{out}} \pm F_{\text{cal}}$ are demodulated using an SSPD in the calibration circuit (Fig. 3). The calibration residue at F_{cal} is then correlated with the original test tone to determine the spur amplitude. A decision block optimizes the NCB gain code setting for maximum cancellation of the supply spurs, yielding the optimal setting for noise cancellation as well.

This calibration can be performed at low frequency, e.g., 50 kHz, since the goal is to calibrate the FFNC gain but not the phase shift occurring at higher offset frequencies. In our work the decision logic was implemented off-chip for testing flexibility (see Sections V and VI), but this approach can be easily implemented on chip. For example, [24] implemented a loop with similar hardware requirements on chip for supply noise cancellation calibration.

The resolution required for programming $G_{f,\text{NCB}}$ depends on the amount of cancellation required from the FFNC. In our prototype, we target a phase noise cancellation better than 10 dB, leading to a precision requirement better than 30% (see Section V).

V. PLL AND FFNC CIRCUIT IMPLEMENTATION DETAILS

This section gives the circuit design details of the PLL and FFNC building blocks and provides simulation data based on a design in a standard 65-nm CMOS GP technology with a 0.94-V supply. The chip diagram of the SSPLL with FFNC featuring the various sub-blocks is shown in Fig. 6.

A. Reference Buffer

The REF buffer to buffer the XTAL output to drive the SSPD is designed as a four-stage inverter chain. Its typical simulated phase noise with a power consumption of 0.1 mW is shown in Fig. 9. In the FFNC scheme the REF is used to measure the noise and cancel it from the output making the REF noise (multiplied by N^2) the minimum achievable noise at the output after cancellation. For this reason, it is advisable to keep the REF noise below the output phase noise being targeted in the application. The REF buffer has a phase noise performance of -156.4 dBc/Hz at 300-kHz offset making the minimum achievable phase noise after cancellation at 300-kHz offset equal to -122.8 dBc/Hz.

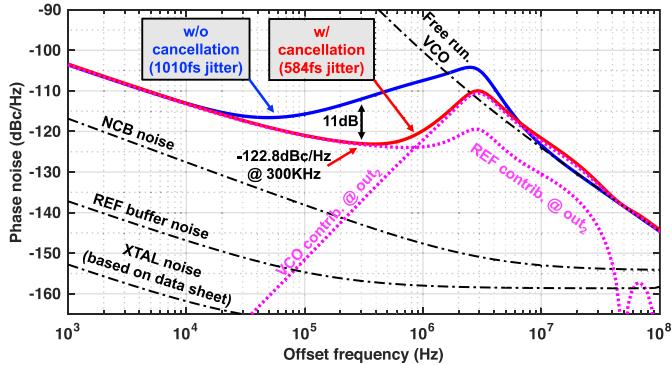


Fig. 9. Typical simulated phase noise profiles of the VCO, REF buffer, and NCB (see text for component details). Simulated phase noise w/ and w/o cancellation showing a phase noise reduction by 11 dB to -122.8 dBc/Hz at 300 kHz after cancellation.

B. SSPD and Transconductor Design

The SSPD needs to sample the incoming VCO signal using the REF signal and generate a voltage corresponding to the error in the zero crossing of the VCO. The VCO is initially sampled at the falling edge of REF by the switch sw_1 and stored on to the capacitor C_1 (Fig. 6). As calculated in Section II, with a sampling capacitor of 100 fF the SSPD noise contribution becomes negligible in comparison to the REF buffer contribution. To drive the NCB with this sampled voltage, it has to be held on a separate node before the arrival of the positive edge of the REF signal. This is done by sampling it with switch sw_2 on to C_2 . The control signal for sw_2 has to be non-overlapping with REF to do this. Using a common non-overlap generator would introduce additional noise in the sw_1 sampling clock. This noise would be added to the REF path, that gets multiplied by N^2 and would be detrimental to the in-band noise performance of the PLL. For this reason we use an open loop RC -based pulser to generate the non-overlap clock for sw_2 . The pulser takes the REF and passes it through a RC filter to obtain a delayed version of REF as shown in Fig. 10. These two signal are now used to generate the pulse which is non-overlapping with REF. Since this pulser takes the REF and produces the pulse in a open loop fashion, it does not affect the noise performance of the REF which determines the in-band noise performance of the PLL. Increasing the ratio C_1/C_2 can be considered to increase the cancellation BW. However, increasing C_1 results in increased SSPD power dissipation since C_1 is used to sample the VCO clock. Decreasing C_2 increases the clock feedthrough and charge injection from sw_2 leading to larger REF spurs. In view of these trade-offs, C_1 was chosen equal to C_2 in this current design.

The transconductor Gm schematic is shown in Fig. 6; the effective G_m is reduced by switching it on for only a short duration during each REF cycle using a pulse P_u whose on time is controlled externally for testing flexibility [2].

C. VCO Design

The VCO is implemented as a five-stage RO. The delay stages are implemented as pseudo-differential cross-coupled inverter stages [20] (Fig. 10). The inverter PMOS

and NMOS (W/L) are chosen to be $(20\mu\text{m}/0.2\mu\text{m})$ and $(10\mu\text{m}/0.2\mu\text{m})$, respectively, to minimize noise. The VCO frequency is controlled by varying the resistance of the NMOS transistor whose gate voltage is controlled by V_{tune} . This changes the RC time constant and the delay associated with each stage. Its typical simulated phase noise with a power consumption of 3.5 mW is shown in Fig. 9.

D. NCB Design

The SSPD output is a differential signal obtained by sampling the differential VCO outputs. This differential signal V_{sam} is converted into a single ended voltage V_{ctrl} by using the amplifier Amp_{d2s} (Fig. 10). The NCB is a variable delay line, whose delay is controlled by the control voltage V_{ctrl} that is fed to the current starved delay stages. Depending on V_{ctrl} , the current in the PMOS and NMOS is changed, which in turn changes the delay of the stage. The NCB gain $G_{f,NCB}$ is determined by the capacitance on the delay stage output node. As discussed in Section IV, the attenuation requirement of about 10 dB sets the accuracy with which this capacitance has to be tuned. In this design, we use a digital capacitor bank C_b controlled by the 4 bit “NCB gain code” to perform this tuning. The unit load capacitance in C_b is realized using an NMOS with a (W/L) of $(4\mu\text{m}/0.2\mu\text{m})$ as shown in Fig. 10. Fig. 11 shows the typical transient simulations of the NCB. The output clock waveforms for various values of V_{sam} (SSPD output) have been plotted. It can be seen that the zero crossings of the clock vary with respect to V_{sam} , thus providing the controlled variable delay needed from the NCB. The variation of the delay as a function of V_{sam} is also shown in Fig. 11. The typical simulated phase noise is shown in Fig. 9. As desired, the phase noise of NCB at the output is lower than the REF noise contribution. It is observed that the NCB becomes the dominant noise source only after hundreds of megahertz offset frequencies. At these frequencies, if the NCB noise is a hindrance to achieve very low noise floor, it is recommended to use a simple BPF after the NCB to suppress the noise. An other approach can be to increase the power consumption in the NCB to reduce the noise to the desired level. The typical simulated NCB power consumption is 0.5 mW.

E. Simulated PLL Performance

To evaluate the performance of the 2.36-GHz PLL with 49.15-MHz REF, individual sub-blocks of the PLL have been simulated at a typical process corner and temperature using Cadence Spectre. The noise profiles of the sub-blocks are then used in the phase-domain model derived in Section IV to generate the PLL phase-noise plot in MATLAB, shown in Fig. 9. After cancellation, the in-band PLL noise is dominated by the REF buffer and the out-of-band noise is dominated by the VCO. The rms jitter is reduced from 1010 to 584 fs. The phase noise at an offset of 300 kHz is reduced to -122.8 dBc/Hz after cancellation and further attenuation is limited by the REF noise floor (Fig. 9). It is observed that even with no NCB gain error, the attenuation achieved at 300 kHz is only 11 dB. This is because further attenuation is limited by the REF noise. This makes the rms jitter after cancellation

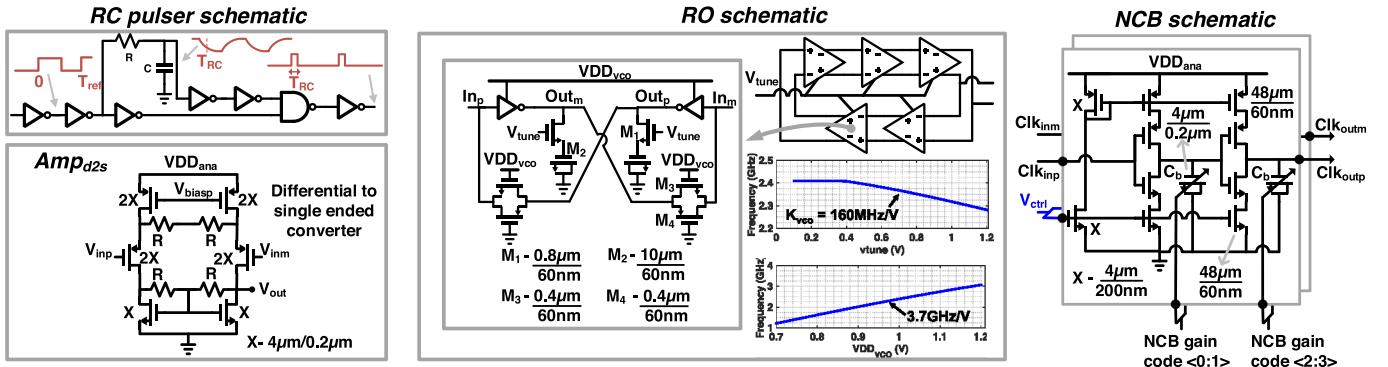
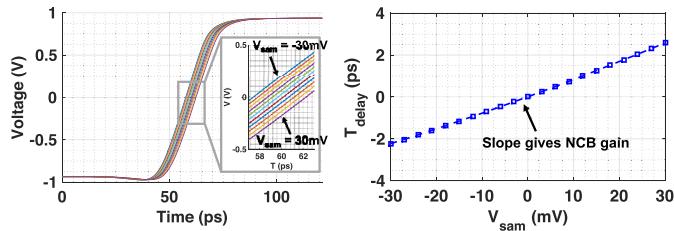
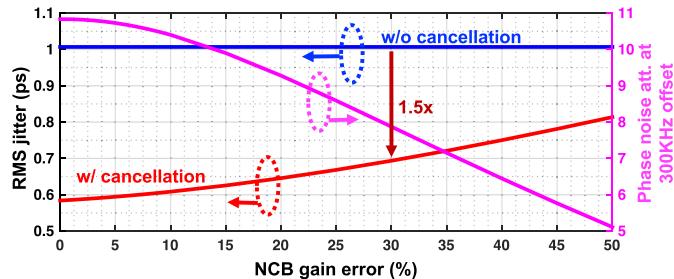


Fig. 10. PLL sub-block schematics.

Fig. 11. Transient simulation of Ampd2s and NCB showing NCB output clock waveforms as a function of V_{sam} (SSPD output). Right: delay in the output clock as a function of V_{sam} .Fig. 12. Typical simulated phase noise attenuation at 300-kHz offset as a function of the NCB gain error. The rms jitter versus NCB gain error plot shown in Fig. 12. Even with an NCB gain error as large as 30%, the FFNC still achieves a 1.5 \times jitter reduction and a phase-noise attenuation at 300 kHz better than 8 dB.

relatively insensitive to NCB gain error at small values. The rms jitter versus NCB gain error plot shown in Fig. 12. Even with an NCB gain error as large as 30%, the FFNC still achieves a 1.5 \times jitter reduction and a phase-noise attenuation at 300 kHz better than 8 dB.

VI. EXPERIMENTAL RESULTS

The test setup for the PLL along with the die photograph is shown in Fig. 13. The device under test is controlled with a serial to parallel interface. The PLL output is taken off-chip using current-mode logic buffers. The output of this buffers are fed into a 180° hybrid to extract the differential component that is measured using a Agilent 4446A spectrum analyzer. The VCO tune voltage and the calibration outputs are also monitored using voltage buffers.

The REF for the PLL is provided from a 49.15-MHz Crytek CCHD-957-25 crystal oscillator with a vendor specified

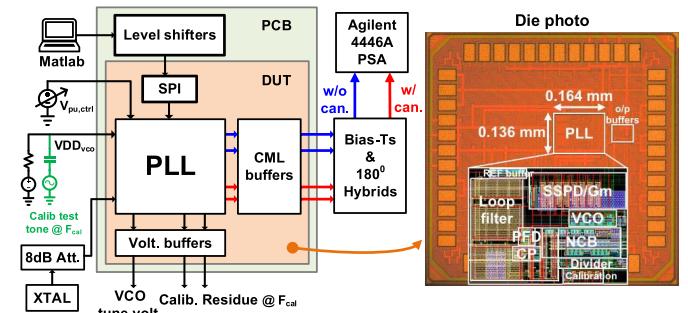


Fig. 13. Diagram of the test setup and die photograph with layout in inset.

-168-dBc/Hz noise floor with 3.3-V supply. However, the crystal output had to be first attenuated to bring its swing down to 1.2 V to be compatible with our prototype chip. The PLL occupies an active area of 0.022 mm² and consumes 5.86-mW power in which 3.1 mW is consumed by the VCO.

At startup, the aux. PLL locks the VCO to the desired F_{out} and the VCO supply is adjusted to center the tune voltage to supply voltage (VDD)/2.³ After this, the auxiliary path is switched off by toggling the “Aux en” bit and the SSPD path is enabled. The SSPD loop BW is set by adjusting the G_m pulser width by varying the voltage $V_{pu,ctrl}$ as shown in Fig. 13. To perform the NCB gain calibration, a 0.3 mV_{pp} test tone of 50 kHz is applied onto the VCO supply using a decoupling capacitor and the calibration output, Calib. residue, is monitored for the residual tone at 50 kHz. As the NCB gain code is swept the calibration output is observed and the code value which gives the minimum Calib. residue is determined and set for the remainder of the test.

A. Phase-Noise Measurement

The measured phase noise w/ and w/o cancellation is shown in Fig. 14(a) (top). At an offset of 300 kHz, the phase noise is attenuated by 10.2 dB from -113.3 to -123.5 dBc/Hz. The jitter integrated from 1 kHz to 100 MHz reduces from 890 to 633 fs rms with cancellation. The PLL achieves an

³In the current prototype the supply adjustment is done off-chip for testing flexibility, but in a production design this can be achieved with an automatic coarse frequency tuning loop.

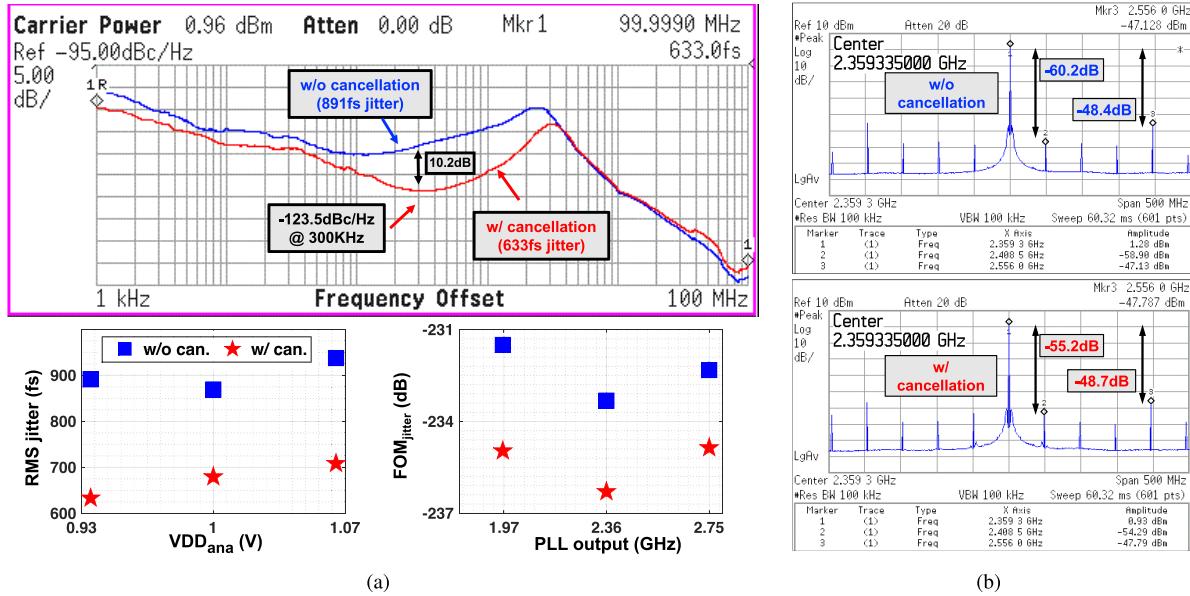


Fig. 14. (a) Measured phase noise w/ and w/o cancellation showing an rms jitter reduction from 891 to 633 fs (top). Measured rms jitter (versus) supply voltage and FOM_{jitter} (versus) output frequency (bottom). (b) Measured PLL output spectrum w/o cancellation and w/ cancellation showing REF spurs.

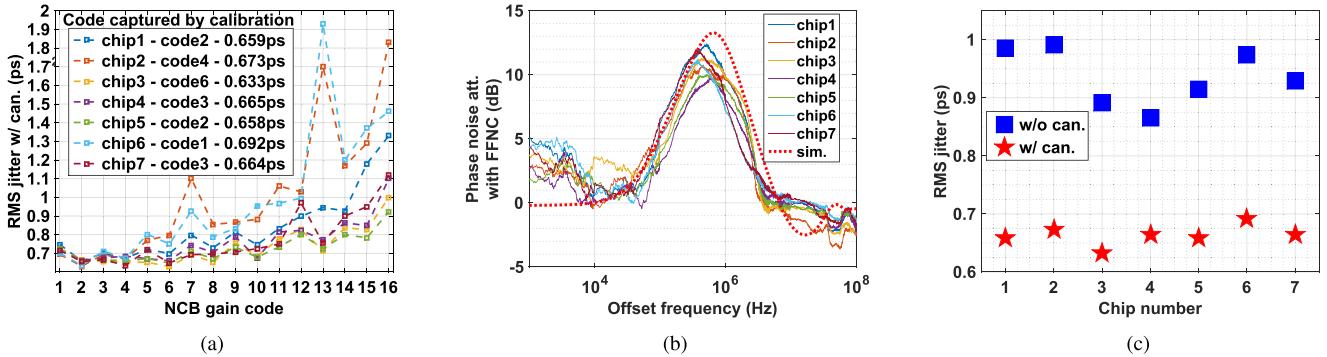


Fig. 15. Measurements from multiple samples. (a) NCB Calibration–output jitter after cancellation as a function of NCB gain codes. Inset: code determined by calibration and the corresponding jitter numbers. (b) Phase-noise attenuation achieved with cancellation across samples. (c) RMS jitter w/ and w/o cancellation across samples.

FOM_{jitter} [30] of -236.3 dB with cancellation. The measured phase-noise attenuation is in good agreement with the simulation result as shown in Fig. 15(b) (chip3).

B. Performance Across Output Frequency and Supply Variation

The supply voltage, VDD_{ana}, for the Ref. buffer, SSPD loop and the NCB is varied by 13% from 0.935 to 1.065 V. The output jitter at 2.36 GHz w/ and w/o cancellation is shown in Fig. 14(a) (bottom). It is observed that the jitter after cancellation is below 710 fs rms across supply variation. Over the 1.97- to 2.75-GHz tuning range, a FOM_{jitter} of -235 dB or better is maintained after cancellation [Fig. 14(a) (bottom)].

C. Reference-Spur Measurement

The PLL output spectrum shown in Fig. 14(b) has REF spurs of -60.2 dBc w/o cancellation and -55.2 dBc w/ cancellation. The additional coupling of the REF to out₂ via

the NCB is the likely source of the degradation in REF spur. An additional spur at an offset of $4F_{\text{ref}}$ at -48.7 dBc w/o and at -48.4 dBc w/ cancellation is also observed.

D. Power-Supply Sensitivity Measurement

Generally in an SoC environment the PLLs RO is provided with a dedicated low dropout regulator [20]. Therefore, to test the supply sensitivity of the PLL, a small tone of 1mV_{pp} at F_{sup} frequency is applied at the RO supply node directly. This results in spurs at the the oscillator output at an offset frequency of F_{sup} . The spurs are measured w/ and w/o cancellation and their difference represents the achieved PSNA. The output spectrum plot showing a PSNA of 19.5 dB for a 100 kHz tone is shown in Fig. 16(a). The frequency F_{sup} is now varied and the measured PSNA versus F_{sup} is shown in Fig. 16(b). The PSNA obtained from the phase-domain model for varying NCB gain errors is also shown. From (8) it can be seen that very high cancellation can be achieved at low frequencies if the NCB gain is exactly equal to $1/K_{\text{SSPD}}$.

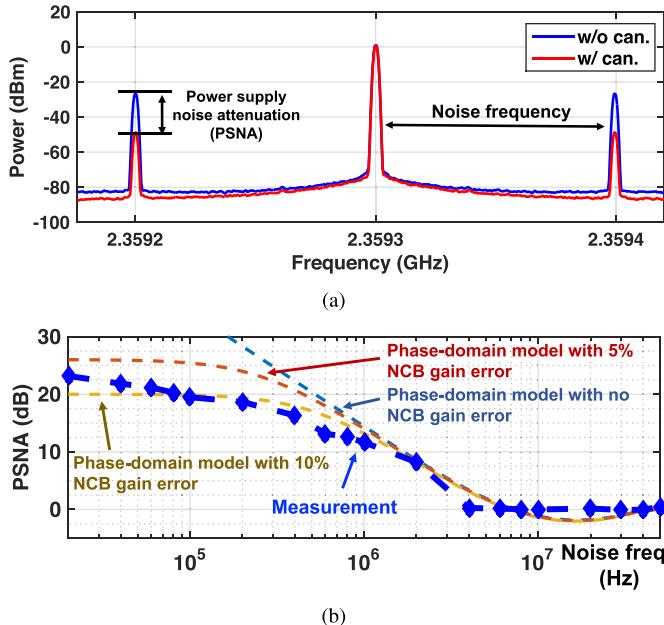


Fig. 16. Measured VCO PSNA with a 1-mVpp noise tone. (a) PLL output spectrum w/ and w/o cancellation showing the PSNA due to cancellation for a 100-kHz noise tone. (b) Measured PSNA versus noise tone frequency and comparison with the results obtained from the phase-domain model for various NCB gain error values.

and as the error increases, the attenuation comes down. The phase-domain model predicted PSNA for various values of NCB gain error is also shown in Fig. 16(b) for comparison.

E. Measurements Across Multiple Samples

To determine the variation in performance across multiple samples, a total of seven chips were tested. At the measurement startup, calibration is run to determine the optimal NCB gain code for each sample. The gain code determined by the calibration scheme and corresponding jitter numbers are shown in Fig. 15(a) (inset). Fig. 15(b) also shows the jitter measured (versus) NCB gain code. The phase-noise attenuation curves measured across samples demonstrate good agreement with each other as shown in Fig. 15(b). The jitter numbers across samples, w/ and w/o cancellation are shown in Fig. 15(c). A minimum of 633 fs and maximum of 692-fs jitter were recorded across samples.

F. Comparison to the State of the Art

The PLL performance summary is shown in Table I. A significant performance improvement has been obtained over the earlier FFNC RO PLL [16]. Fig. 17(a) shows the jitter versus power plot for state-of-the-art integer-N RO PLLs that can be driven from a crystal oscillator [5], [11], [12], [16], [31]–[36]. The presented PLL *without cancellation* has an $\text{FOM}_{\text{jitter}}$ of -233.3 dB and is on par with other state-of-the-art RO PLLs. However, *with cancellation*, the $\text{FOM}_{\text{jitter}}$ improves by 3 to -236.3 dB. State-of-the-art LC PLLs still offer a better $\text{FOM}_{\text{jitter}}$ [see Fig. 17(b)], however, they require significantly larger area. The presented PLL opens up new perspectives for replacing LC PLLs in area-constrained SoC applications. In

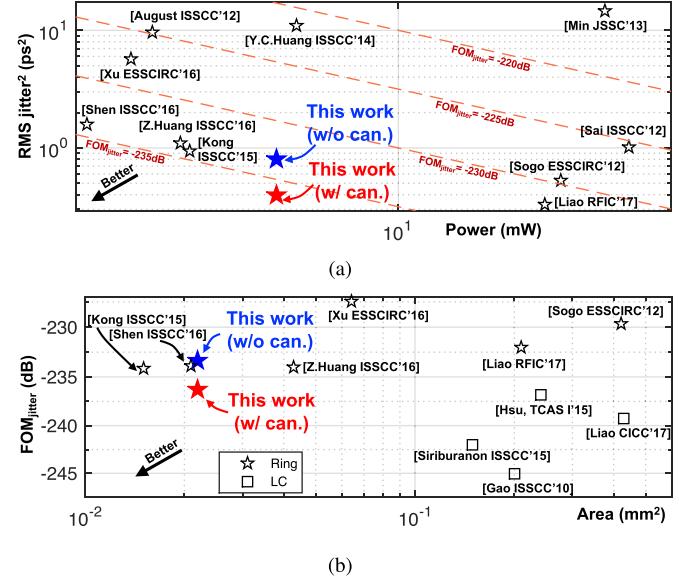


Fig. 17. Comparison to the state-of-the-art integer-N PLLs. (a) Power (versus) jitter comparison with other RO PLLs. (b) $\text{FOM}_{\text{jitter}}$ (versus) area comparison, including LC PLLs.

TABLE I
COMPARISON TO THE STATE-OF-THE-ART INTEGER-N RO PLLS

	ESSCIRC'12 [Sogu12]	JSSC'13 [Min13]	ISCC'15 [Kong15]	ISCC'16 [Z.Huang16]	RFIC'17 [Liao 17]	This work
Architecture	SSPD	FFNC	Type-I PLL	Cascaded PLL	SSPD	SSPD FFNC
Technology (nm)	65	90	45	65	130	65
Voltage (V)	1.2	1.2	1	1.2	1.3	0.935
Oscillator type	Ring	Ring	Ring	Ring	Ring	Ring
Reference (F_{ref}) (MHz)	130	10	22.6	67.74	50	49.15
Tuning range (GHz)	NA	3.5–7.1	2.0–3.0	1.1–2.1	0.8–1.3	1.97–2.75
Area (mm ²)	0.42	0.12	0.015	0.043	0.21	0.022
Norm. area ¹	19.09	2.88	1.42	1.95	2.39	1
Output freq. (GHz)	2.08	5	2.39	2.1	1.2	2.36
Power (mW)	20.4	24.7	4	3.84	19	5.86
Ref. spur at F_{ref} offset (dBc)	-47.8	-64.8	-65	-45	NA	-55.2
PSNA (dB) (Noise pow. / freq.)	NA	NA	NA	24 (-74/1)	NA	19.5 (-56/0.1)
Phase noise (dBc/Hz) (MHz)	-119.1 (1.4)	-105 (1)	-113.8 (1)	-108.3 (1)	-121.67 (1)	-119.1 (1)
RMS jitter (ps) (Integ. Range) (MHz)	0.73 (0.001–10)	3.8 (0.01–10)	0.97 (0.001–200)	1.05 (0.001–50)	0.57 (0.01–100)	0.63 (0.001–100)
$\text{FOM}_{\text{jitter}}^2$ (dB)	-229.7	-214.5*	-234.1	-234	-231.2*	-236.3
*- calculated from values NA - Not available				¹ Normalized area = $[(65\text{nm}/\lambda)^2(\text{Area}/0.022\text{mm}^2)]$		
				² $\text{FOM}_{\text{jitter}} = 10 \log_{10}[(\text{RMSjitter}/1\text{s})^2(\text{Power}/1\text{mW})]$		

addition to an excellent jitter performance, the presented PLL also offers a power supply noise attenuation of up to 20 dB

VII. CONCLUSION

This paper explored an SSPD-based FFNC technique to reduce noise of RO-based PLLs. The proposed FFNC implementation leverages the available SSPD to extract the noise present in the output of the VCO with high sensitivity. Noise cancellation is performed with a variable delay line after the PLL resulting in an FFNC solution with minimal power and area overhead. The cancellation reduces loop filter noise, enabling a reduction of the filter's area,

which makes up a significant portion of the RO-PLL's area footprint. The cancellation scheme also reduces the jitter caused by supply noise, hence, making the PLL more suitable for an SoC application. The experimental demonstration of the noise-cancellation technique in a 65-nm RO PLL at 2.36-GHz achieves a $1.4\times$ reduction of the jitter down to 633-fs rms, corresponding to a FOM_{jitter} of -236.3 dB. In addition, a 19.5-dB power supply noise suppression is demonstrated for a 100 kHz 1 m V_{pp} noise applied on the VCO supply.

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