An Injection Frequency-Locked Loop—Autonomous Injection Frequency Tracking Loop With Phase Noise Self-Calibration for Power-Efficient mm-Wave Signal Sources

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***Abstract*— This paper presents a fast and autonomous injection frequency tracking and locking technique. In the present injection-locking system, a quadrature injection-locked oscillator (QILO) is third harmonically locked to a quadrature voltage-controlled oscillator (QVCO). In the frequency tracking loop, the frequency difference between QVCO and QILO is extracted using the QILO's amplitude modulated (AM) envelope waveform. The AM frequency of the envelope signal bears frequency difference between the two oscillators. The envelope signal is further converted to pulse signal which subsequently drives digital feedback control circuitry to update the QILO's output frequency so that it can track the third harmonic of the injection QVCO. The frequency calibration process is purely autonomous, self-initiating whenever the AM modulated envelope waveform is generated. The feedback signal is primarily processed in the digital domain, resulting in a compact, fast, and power-efficient injection frequency-locked loop (IFLL). By incorporating a phase noise (PN) calibration routine after completing the frequency calibration, the presented IFLL resolves the intractable issue of PN degradation at the edge of the slave oscillator's injection locking range. This results in a large injection frequency tracking range of 26.5–29.7 GHz which is only limited by the QILO's *LC* tank tuning range. The IFLL realized in 0.13-μm CMOS consumes 2.4 mW with a negligible area penalty. Overall chip size including QVCO, QILO, and IFLL is 1 × 1 mm^2.**

***Index Terms*— Feedback, fifth-generation (5G), frequency-locked loop, injection locking, *LC* oscillator, phase noise (PN), phase-locked loop (PLL), voltage-controlled oscillator (VCO).**

I. Introduction

A HARMONICALLY injection-locked oscillator (ILO) is widely used for microwave and millimeter (mm)-Wave applications [1]–[5]. The distinctive feature of establishing frequency locking simultaneously with frequency multiplication in the harmonic ILO can eliminate power hungry high-frequency divider networks. This brings the merit of high power efficiency to the phase-locked loop (PLL)-based high-frequency synthesis [6]. The harmonic ILOs are also better positioned to achieve higher spectral purity than fundamental oscillators at high frequency. This is because phase noise (PN) of the subharmonic ILOs scales with 6 dB per every octave frequency scaling between the frequencies of master injection oscillators and slave harmonic ILOs. Whereas the PN degradation in fundamental oscillators could be worse than the theoretical 6-dB/octave PN upscaling because of more emphasized active and passive devices noise particularly at mm-Wave band over 60 GHz [7].

However, one critical drawback in the harmonically injection locking-based high-frequency signal generation is that the injection frequency locking range (Δf_L) of a slave ILO is very narrow due to a relatively small third-harmonic power compared with a fundamental signal power, typically less than a few percentage of the ILO's nominal free-running frequency. There are substantial efforts to increase Δf_L by either open-loop or closed-loop control system configurations. One dominant open-loop approach is to increase the strength of an injection signal power relatively to that of an ILO signal power via multiport injections together with lowering the ILO *LC* tank quality factor (Q) [8], [9]. The Δf_L improvement in the open-loop approach will be incremental and strongly traded with dc power dissipation which could increase substantially as the operating frequency increases toward mm-Wave regime.

More systematic locking range enhancement can be achieved by calibrating the ILO frequency to track injection frequencies with a closed-loop control. As shown in Fig. 1, so far most of feedback-based ILO frequency calibration schemes leverage the frequency error detection between a master voltage-controlled oscillator (VCO) and a slave ILO to initiate the feedback loop for updating the ILO frequency. This is essentially a cascade of another PLL with referencing to the master VCO output frequency. The example in Fig. 1(a) utilizes a third-harmonic injection locking oscillator (X3-ILO) to rescale the master VCO's frequency range for a given

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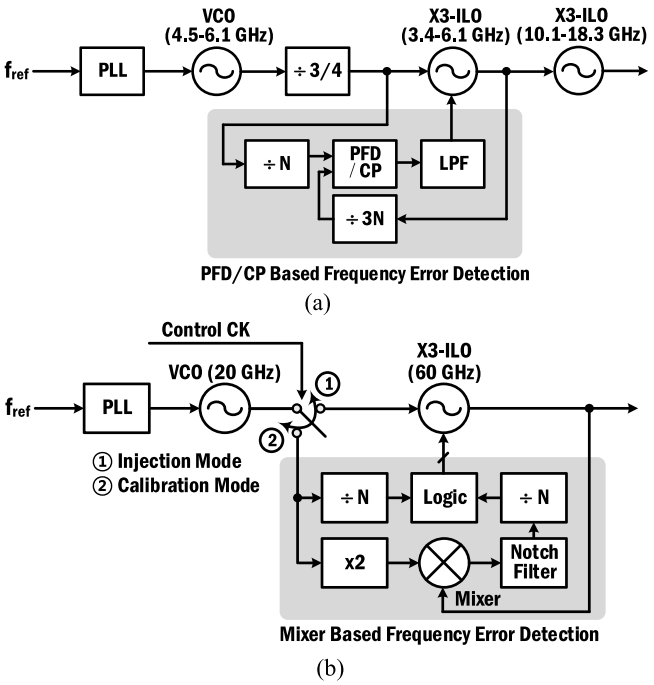


Fig. 1. Prior hardware examples for harmonic injection frequency tracking system based on frequency detection techniques for microwave and mm-Wave applications. (a) PFD-/CP-based frequency error detection at RF to microwave frequencies [10]. (b) Mixer-based freqeuncy error detection at mm-Wave frequencies [12].

frequency planning. Then, a series of frequency-phase detector (PFD) and charge pump (CP) detect and generate frequency error information for calibrating the X3-ILO in a low-frequency domain scaled down by a factor of N [10], [11]. Depending on the frequency division factor N and X3-ILO output frequency, the feedback loop could be subjected to the speed, power, and performance tradeoffs, potentially demanding significant dc power at high frequencies; for instance, another example of the harmonically injection-locked PLL in [11] consumes more than100-mW dc power for suppressing rms jitter below 100 fs at 20 GHz.

The frequency error detection using a mixer in the mm-Wave domain shown in Fig. 1(b) also causes excessive dc power penalty claimed by the system complexity involved in the frequency conversion and afterward complicate signal processing to convert the analog mixer outputs to digital control logic signals [12]. Although successfully demonstrating integration of the ILO calibration loop into a 60-GHz time-division duplex system in [12], the PLL-based ILO calibration incurs another system latency which is comparable to or even longer than the primary PLL settling time, difficult to applicable to fast frequency division duplex or frequency hopping systems. A fast settling time in the ILO calibration loop is critical to minimize system latency.

More recent approaches utilizing ring oscillators-based injection frequency calibration techniques would be suitable for RF frequency of several gigahertz or below [21]–[23]. However, their operation is questionable at the high-end microwave band and mm-Wave domain since they are mostly relying on reference pulse alignment based on phase detection and charge pump integration, of which nonlinearity could be considerably worse at the microwave and mm-Wave frequencies. It is also remained to be seen that the interpolative phase-coupled oscillator approach in [22] would carry any practical importance over mm-Wave band since the dynamic power dissipation could be substantial. For a wide injection frequency tracking range through fast and power-efficient close-loop ILO calibration at microwave to mm-Wave bands, this paper presents an injection frequency-locked loop (IFLL) that autonomously adjusts the output frequency of a quadrature ILO (QILO) to the third harmonic of a master quadrature VCO (QVCO) frequency [13].

The proposed IFLL directly utilizes an amplitude modulation (AM) effect inbred in the nonlinear injection pulling phenomena of the QILO to detect the frequency error between the QVCO and QILO [14], [15]. This eliminates the hardware complexity and the system latency associated with sensing frequency error between the VCO and X3-ILO in Fig. 1, resulting in faster calibration loop speed with higher power efficiency and smaller form factor, compared with the prior works. The main application space of the system is for signal sources with a low latency for fifth-generation (5G) mm-Wave wireless communications. Section II details the IFLL architecture in the system level and more specific building block circuits design is provides in Section III. The experimental results are presented in Section IV, and this paper is concluded in Section V.

II. Injection Frequency-Locked Loop (IFLL)

A. IFLL Architecture

Fig. 2 illustrates the proposed injection-locking system where the X3-QILO ($f_{\rm osc}$: 26.4-30 GHz) is injection locked to the third harmonic of the QVCO output frequency ($f_{\rm inj}$: 8.8–10 GHz). The feedback chain comprised of an envelope detector, limiter, lock detector, M-divider, feedback controller, and 5-b counter constitute the IFLL for tracking injection frequency. The tracking and calibration of the X3-QILO output frequency primarily relies on the frequency detection or FM-to-AM conversion capability of the QILO under injection pulling state when the QILO is unlocked to the QVCO [16]. Namely, when the third-harmonic frequency of an injection signal, $3f_{\rm inj}$, deviates beyond the intrinsic Δf_L of the QILO, the QILO loses lock and starts to be pulled by the QVCO. This instigates frequency modulated sideband tones of which beat frequencies are spaced by $f_{\rm AM}$ as shown in Fig. 2. These sideband tones essentially modulate amplitude of the QILO output at node ① in Fig. 2. From [16], the AM modulation frequency ($f_{\rm AM}$) is given as

$$f_{\rm AM} = \sqrt{(f_{\rm osc} - 3f_{\rm inj})^2 - \left(\frac{\Delta f_L}{2}\right)^2}. \quad (1)$$

When $f_{\rm osc} - 3f_{\rm inj} \gg \Delta f_L/2$, $f_{\rm AM}$ is approximated to the frequency difference of $f_{\rm osc} - 3f_{\rm inj}$. In the proposed IFLL, the AM modulated signal is demodulated using an envelope detector at node ② followed by a rail-to-rail amplification through a limiter, producing a pulse signal at node ③. The pulse signal is then fed to the **M**-divider and lock detector to initiate feedback process in the digital domain.

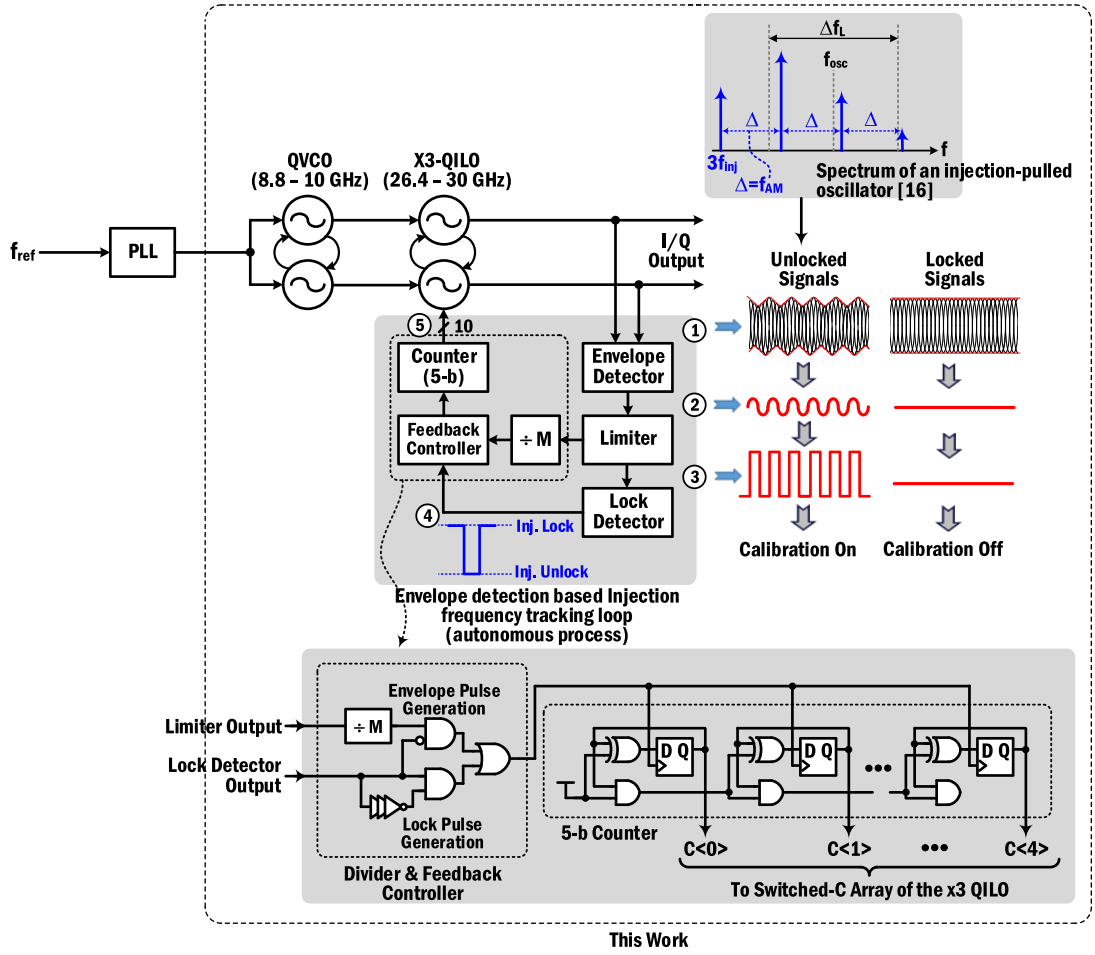


Fig. 2. Block diagram of the proposed IFLL employing envelope detection-based injection frequency tracking loop.

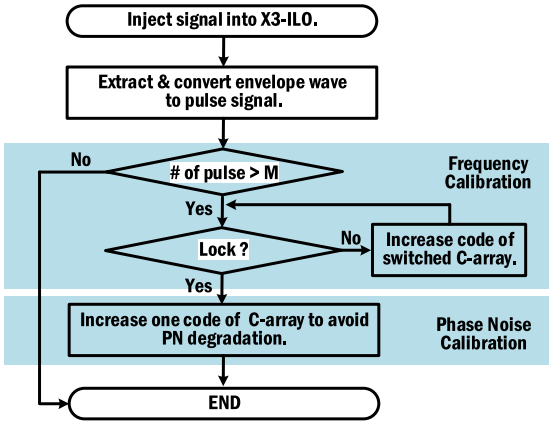


Fig. 3. Flowchart of the frequency and PN calibration in the proposed IFLL shown in Fig. 2.

As illustrated in Fig. 3, the feedback loop acquires frequency locking first and then calibrates PN. When unlocked, the lock detector disables the lower path of the feedback controller and the divider enables the upper path of the feedback controller in Fig. 2 after counting **M** consecutive pulses. Consequently, the 5-bit counter increases *LC* tank capacitance by 1-LSB capacitance (ΔC) in the switched-C array [node ⑤] of the X3-QILO, decreasing frequency of the QILO by Δf corresponding to the ΔC change. This feedback control is an autonomous process being initiated by the envelope pulse wave of the X3-QILO and persists until the QILO can track the injection frequency, calibrating the QILO output frequency. Thus, the frequency tracking range is limited only by the tuning range of the X3-QILO.

When locked, the lock detector outputs a lock signal which disables the upper path of the feedback controller. When locked at the edge of the locking range, the PN degradation of the X3-QILO is significant. Thus, as a final step in the calibration, the lower path of the feedback controller creates one more pulse to increase the *LC* tank capacitance by 1-LSB ΔC. This pushes the X3-QILO frequency closer to the third harmonic of injection frequency, thereby preventing the PN degradation at the edge of the locking range (more detailed in the following section). By using the envelope wave of the X3-QILO output signal as a control signal to enable calibration circuit, the proposed calibration scheme does not require any external control signals.

B. System Modeling of the Frequency Tracking in the IFLL

A linearized frequency tracking model can be derived based on the intuitive transient behavioral model illustrated in Fig. 4.

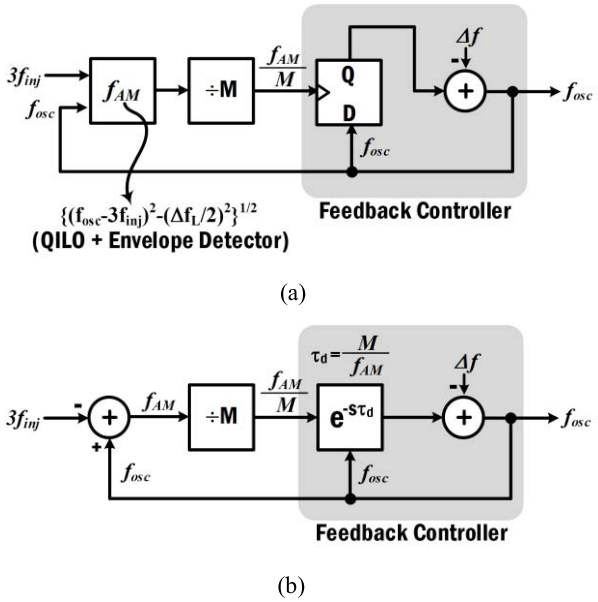


Fig. 4. System modeling of the frequency tracking in the IFLL. (a) Behavioral transient model with a conceptual state machine (D flip-flop) in the frequency domain to emulate a clocked transient frequency update. (b) Linearized frequency-domain model.

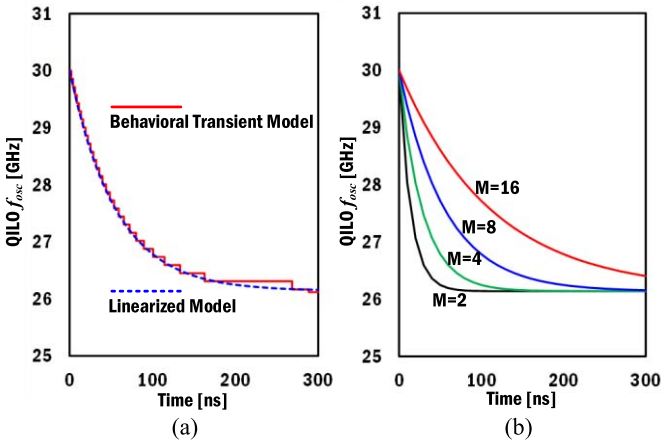


Fig. 5. First-order frequency settling behaviors in the frequency tracking models in Fig. 4. (a) Comparison between the transient and linearized models ($M = 8$, $3f_{\text{inj}} = 26.14$ GHz, and nominal $f_{\text{osc}} = 30$ GHz). (b) Settling times for several different division ratios M in the linearized model ($3f_{\text{inj}} = 26.14$ GHz and nominal $f_{\text{osc}} = 30$ GHz).

In the transient model shown in Fig. 4(a), a discrete time-domain feedback loop changes the X3-QILO frequency every loop cycle. To emulate the frequency update per every clock cycle driven by the **M**-divider, the transient model contains a conceptual frequency-domain state machine (D flip-flop). From (1), the frequency of the X3-QILO envelope wave after nth loop cycle $f_{\text{AM},n}$ can be expressed as

$$f_{\text{AM},n} = \sqrt{\{f_{\text{osc}} - 3f_{\text{inj}} + (1-n)\Delta f\}^2 - \left(\frac{\Delta f_L}{2}\right)^2}. \quad (2)$$

The output frequency of the QILO f_{osc} is subtracted with Δf every M-cycle of the envelope period ($1/f_{\text{AM},n}$) until the calibration finishes. Therefore, by summing every M-time of the envelope period, the locking time (t_{lock}) can be found by the following equation:

$$t_{\text{lock}} = \sum_{n=1}^{N} \frac{M}{f_{\text{AM},n}}, \quad \text{where} \quad N = \left\lceil 1 + \frac{f_{\text{AM}}}{\Delta f} \right\rceil. \quad (3)$$

N meaning total number of the IFLL update is the smallest integer greater than or equal to $1 + f_{\text{AM}}/\Delta f$. The estimation of t_{lock} requires a numerical calculation.

To facilitate analysis of the control loop dynamics, the transient feedback model is linearized in Fig. 4(b) with assuming $f_{\text{AM}} \approx f_{\text{osc}} - 3f_{\text{inj}} \gg \Delta f_L/2$. The time delay in the frequency update after counting **M** consecutive pulses by the **M**-divider is modeled as $e^{-s\tau_d}$ where $s = j\omega$ and $\tau_d = \mathbf{M}/f_{\text{AM}}$ which after all determines the feedback loop speed. In the linear model, the amount of step frequency decrease Δf in the switched-C array is expressed as

$$\Delta f = e^{-s\tau_d} f_{\text{osc}} - f_{\text{osc}} \quad (4)$$

which can be reduced to a rational form of (5) with a truncated Taylor approximation of $e^{-s\tau_d} \approx 1 - s\tau_d$.

$$\Delta f \approx -s\tau_d f_{\text{osc}} = -s\frac{\boldsymbol{M}}{f_{\text{AM}}} f_{\text{osc}}. \quad (5)$$

By substituting f_{AM} with $f_{\text{osc}} - 3f_{\text{inj}}$, overall transfer function can be found as

$$H(s) = \frac{f_{\text{osc}}}{3f_{\text{inj}}} = \frac{1}{1 + s\frac{\boldsymbol{M}}{\Delta f}} = \frac{1}{1 + s\tau_{\text{IFLL}}} \quad (6)$$

where $\tau_{\text{IFLL}} = M/\Delta f$ represents the IFLL time constant. The Δf is determined by the capacitance resolution in the X3-QILO switched C-array. For the case of $\mathbf{M} = 8$ with the X3-QILO $f_{\text{osc}} = 30$ GHz and $3f_{\text{inj}} = 26.14$ GHz, the frequency settling behaviors in the transient and linearized models are compared in Fig. 5(a), verifying the first-order loop dynamics are exactly matched for both cases.

Apparently, as shown in Fig. 5(b), a smaller **M** leads to a faster frequency tracking capability while increasing vulnerability to irregular pulse noises. In fact, the divider plays the role of a pulse filter to filter out irregular burst pulses; namely, for frequency update it requires counting a faithful **M** consecutive pulse wave, ignoring burst pulses less than **M**. A large **M** results in more robust operation against digital pulse noises at the expense of a longer loop settling time. In this paper, the choice of $\mathbf{M} = 8$ is rather judgmental after full process corner simulations, resulting in no observable sensitivity to sporadic digital pulse noises. Fig. 6 shows typical SPECTRE transient simulation results of the injection frequency locking characteristics. The simulation settings are X3-QILO $f_{\text{osc}} =$ 30.1 GHz, $3f_{\text{inj}} = 28.3$ GHz, $M = 8$, and $\Delta f = 142$ MHz. From (6), $\tau_{\text{IFLL}} = M/\Delta f = 8/142$ MHz ≈ 56.3 ns. The 90%–99% settling time corresponds to 2.3-to-4.6τ_{IFLL} and ranges from 129.5 to 260 ns, which is exactly matched with SPECTRE simulations, confirming validity of the linearized freqeucy tracking sysem models in Fig. 4. In Fig. 6, the first flat ~20 ns is static offset time for discharging charge pump

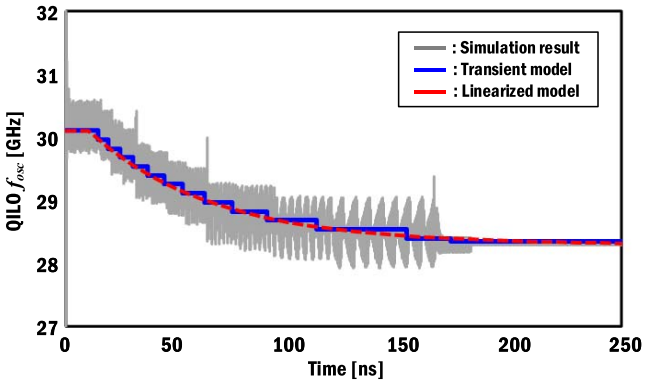


Fig. 6. Comparison of the frequency tracking system models with SPECTRE time-domain transient simulations ($M = 8$, $3f_{\text{inj}} = 26.14$ GHz, and nominal $f_{\text{osc}} = 30$ GHz).

output capacitor to enable the frequency tracking feedback loop.

C. Optimal Frequency Resolution of QILO for Phase Noise Calibration

Theoretically, the PN in the third-harmonic ILOs will be degraded by 9.5 dB, compared with that of injection signals, because of 3× frequency upscaling factor. However, the PN at the edges of the locking range becomes worse than the analytical value because the PN of the ILOs becomes dominant, although the frequency would still be locked to the injection signals. This effectively narrows locking range. In practical sense by taking into account of the PN degradation effect, the effective locking range is approximated to 60% frequency locking range, as reported in [6]. In order to avoid the PN degradation at the edges of locking range, the proposed IFLL adopts a control method that pushes frequency of the QILO f_{osc} toward the center of locking range, as a final step in the frequency calibration routine shown in Fig. 3.

For example, let us assume that the QILO is unlocked and the injection locking range Δf_L equals to 3 LSBs of the switched-C array of the X3-QILO as shown in Fig. 7(a). The calibration circuit gradually moves f_{osc} closer to $3f_{\text{inj}}$ per each feedback loop cycle and finally the QILO could be locked to the injection signal at the edge of locking range as illustrated in Fig. 7(b) and subjected to the PN degradation. To avoid the noise degradation, that is, to lock within the effective locking range, the feedback controller carries out one more LSB update in the switched-C array after an initial injection locking. Consequently, f_{osc} can move into the effective Δf_L and the QILO is no longer subjected to the PN degradation, as shown in Fig. 7(c). Note that in Fig. 7(b) and (c), for clarity purpose the frequency tone of $3f_{\text{inj}}$ is shifted toward f_{osc} with the steps of 1-LSB frequency code (Δf) determined by the 1-LSB switched C-array capacitance code—in reality, the X3-QILO f_{osc} will be shifted toward $3f_{\text{inj}}$ with the same steps.

Fig. 8 shows two failure cases of calibrating PN when the frequency resolution Δf in the switched-C array is smaller or larger than the requirement. First, when the QILO is locked at the right edge of Δf_L as shown in Fig. 8(a), if $\Delta f < 0.2\Delta f_L + f_{\text{AM,MIN}}$, where $f_{\text{AM,MIN}}$ is the minimum

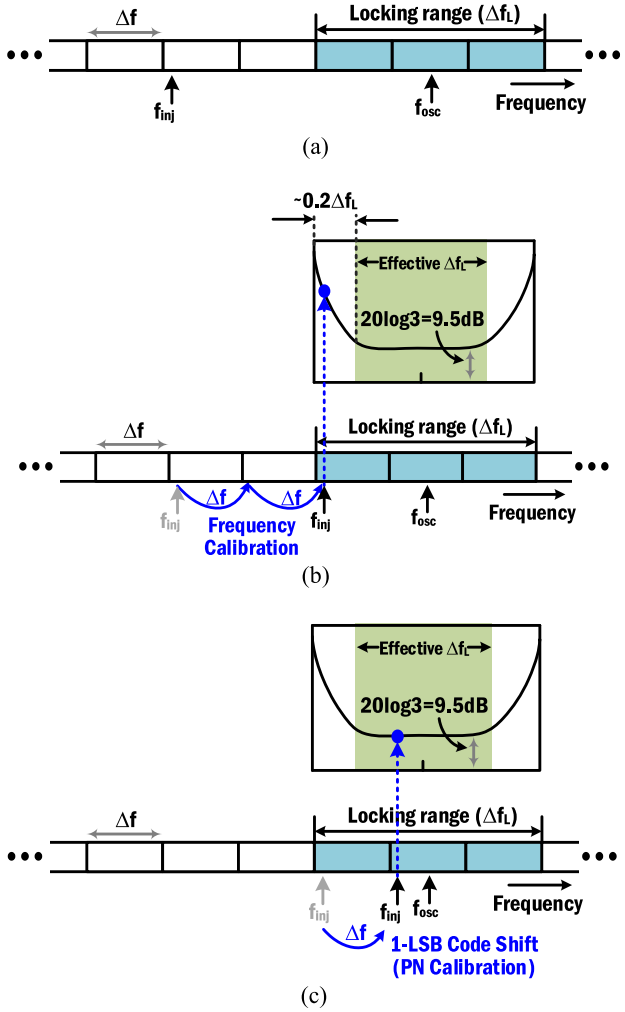


Fig. 7. Conceptual diagram of frequency and PN calibration in the IFLL. (a) Injection frequency ($3f_{\text{inj}}$) distancing about 2 LSB frequency codes (Δf) away. (b) Frequency calibration and frequency locking at the edge of the X3-QILO locking range. (c) PN calibration by pushing 1-LSB Δf.

detectable frequency by the envelope detector and limiter, the $3f_{\text{inj}}$ tone could fall outside of the effective Δf_L even after one extra Δf is shifted to the right. Also, the $3f_{\text{inj}}$ tone could fall outside of Δf_L after the Δf calibration if $\Delta f > 0.5$ ($0.8\ \Delta f_L + f_{\text{AM,MIN}}$) in Fig. 8(b). For successfully PN calibration by pushing one LSB code, the relationship between Δf_L of the QILO and Δf of the switched-C array should meet the following condition:

$$0.2\Delta f_L + f_{\text{AM,MIN}} \le \Delta f \le 0.5(0.8\Delta f_L + f_{\text{AM,MIN}}). \quad (7)$$

In this paper, by setting Δf to satisfy (7), the X3-QILO is locked within the effective locking range ($\sim 0.6 \cdot \Delta f_L$) despite its slight variations depending on natural frequency over the process corners and temperature in simulations. More specifics on the design parameters are disclosed in Section III.

III. Building Block Designs

A. QVCO and QILO

The QVCO shown in Fig. 9 generates and injects 8.8–10 GHz quadrature signal to the following X3-QILO shown in Fig. 10. The QILO is third harmonically locked to the

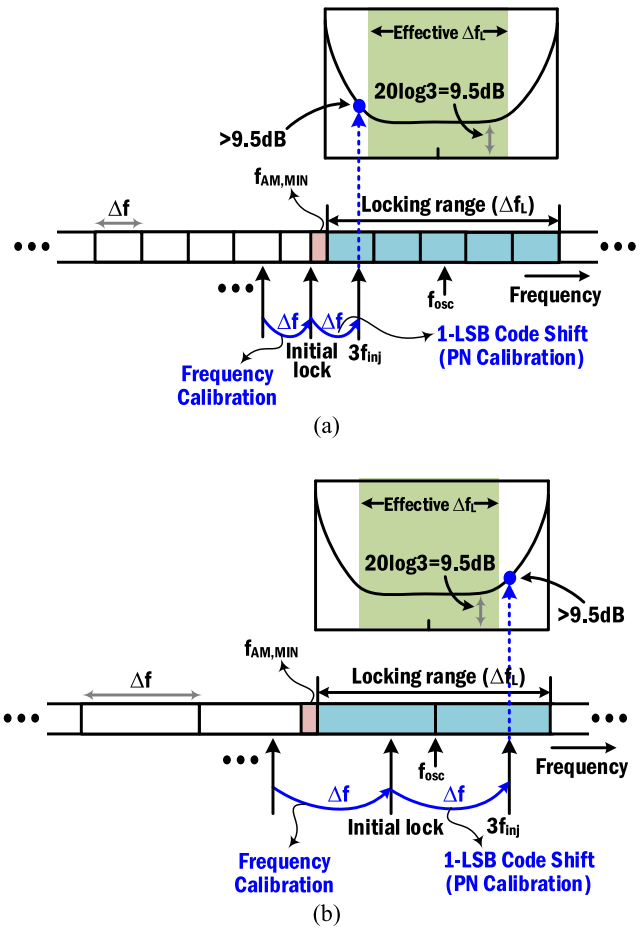


Fig. 8. PN calibration errors because of incorrect frequency resolution (Δf) in the QILO. (a) Case of $\Delta f < 0$. $2\Delta f_L + f_{\mathrm{AM,MIN}}$. (b) Case of $\Delta f > 0.5$ ($0.8\Delta f_L + f_{\mathrm{AM,MIN}}$). $f_{\mathrm{AM,MIN}}$ is the minimum detectable frequency by the envelope detector and limiter.

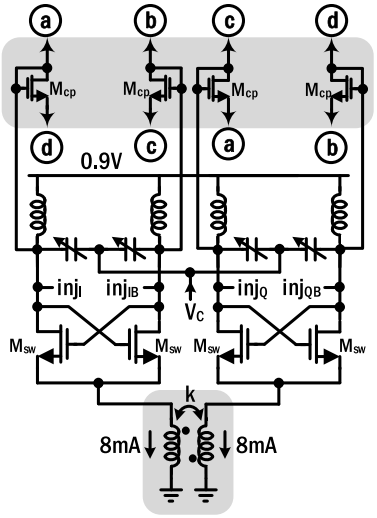


Fig. 9. Schematic of the QVCO for $f_{\mathrm{inj}} = 8.8$–10 GHz.

QVCO and outputs 26.4–30 GHz quadrature signals. For better PN with high quadrature (I/Q) phase accuracy, the QVCO adopts dual coupling networks comprised of super-harmonic inductive coupling (SHC) [17], [18] and symmetric in-phase injection-coupling (IPIC) [19]. While the SHC requires additional area for tail coupled-inductor, it can achieve good PN

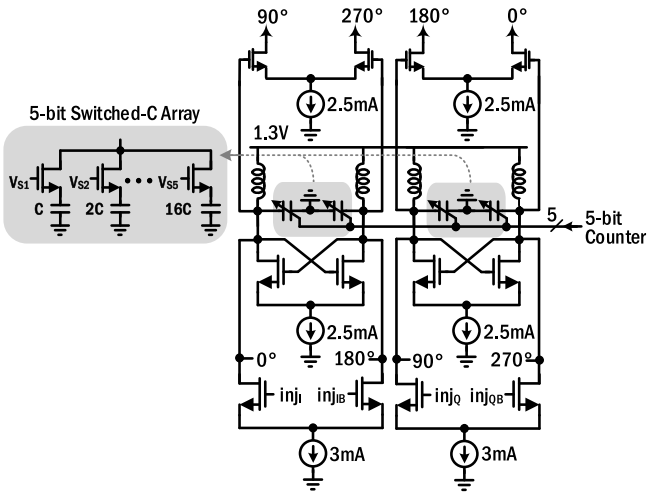


Fig. 10. Schematic of the X3-QILO for $f_{\mathrm{osc}} = 26.4$–30 GHz.

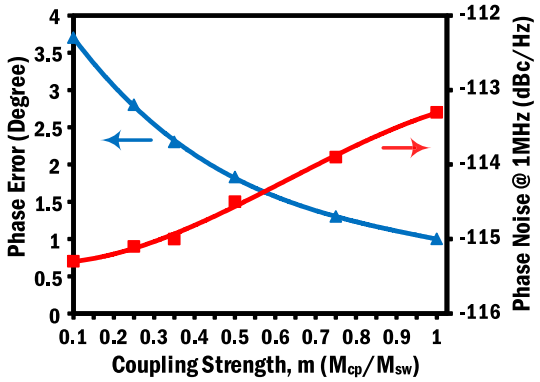
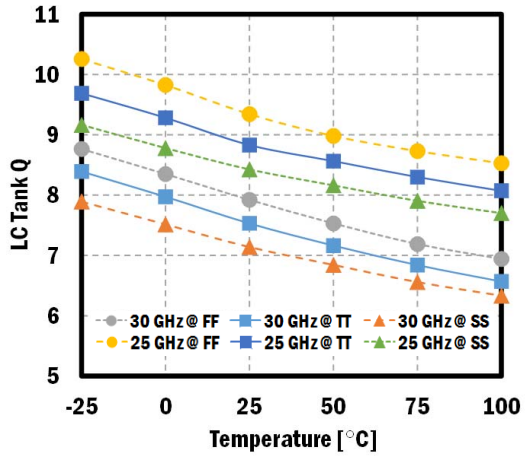


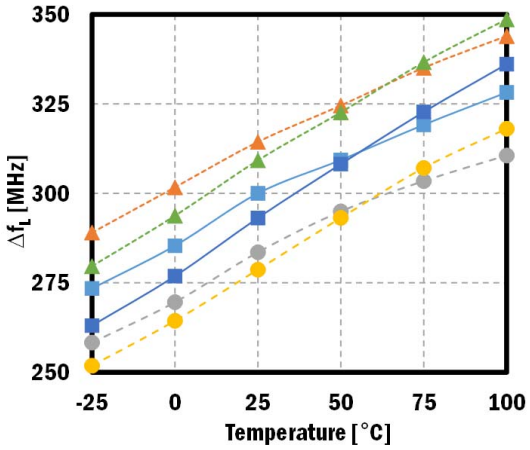
Fig. 11. Simulation results of I/Q phase accuracy and PN of the QVCO at 10 GHz with assuming a conservative 2% *LC* tank varactor mismatch.

compared with other types of coupling network. To define the phase direction clearly, the IPIC diode network is incorporated. It is important to define the I/Q phase directivity clearly in the injection QVCO and the phase direction needs to be matched with that of the X3-QILO since the randomness of I/Q phase could cause the X3-QILO to fail locking even with the injection frequency equal to the X3-QILO free-running frequency.

The sizing of the NMOS-based diode in Fig. 9 is subjected to a tradeoff between I/Q phase accuracy and PN. Without any *LC* tank mismatch, the I/Q phase error is negligible. Fig. 11 shows the simulated PN and I/Q phase error of the dual coupled QVCO with assuming 2% *LC* tank varactor mismatch, a conservative assumption possibly due to slight layout mismatch effects between the I/Q *LC* tanks, versus coupling strength **m** defined by the size ratio of $M_{\mathrm{cp}}/M_{\mathrm{sw}}$. As expected, the larger **m** makes more accurate quadrature phasing at the cost of PN degradation. Using SHC, it can improve PN by ~2 dB, compared with the IPIC-QVCO without SHC. In our design, the coupling strength is set to be 0.35 to ensure better than −115 dBc/Hz of PN at 1-MHz offset at 10 GHz while allowing phase error of less than 2.5° in simulations under the conservative premise. Each *LC* tank consumes 8 mA with a supply voltage of 0.9 V.

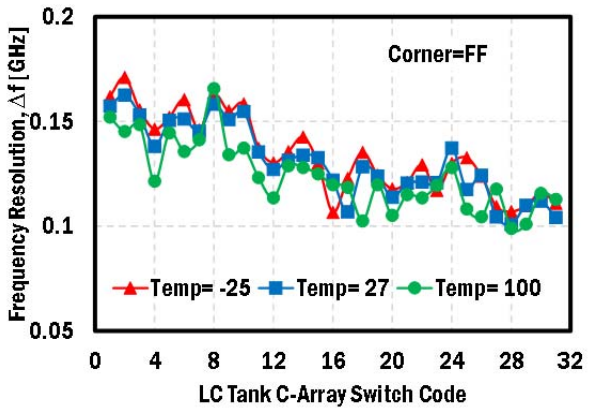


(a)



(b)

Fig. 12. Simulation results of (a) QILO *LC* tank Q and (b) Δf_L over the temperature change from −25 °C to 100 °C in FF/TT/SS corners.



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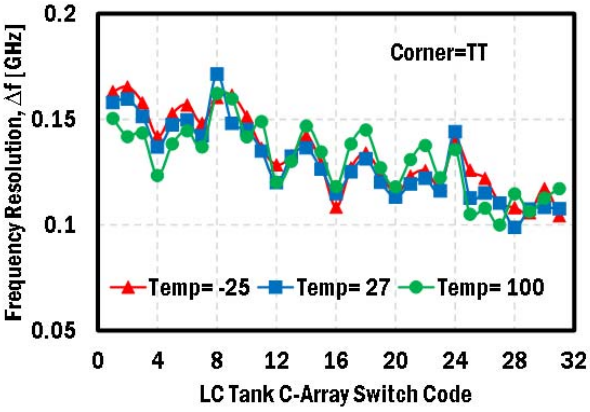
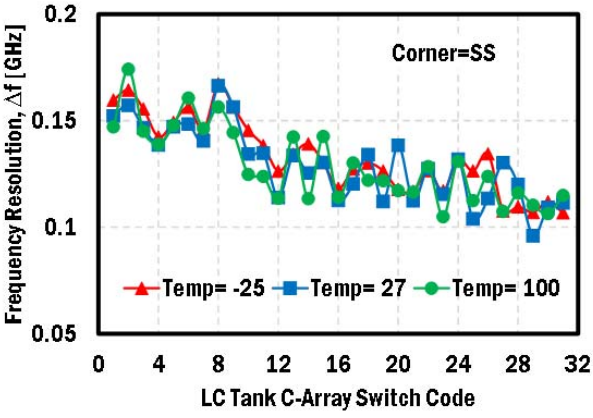


(b)



(c)

Fig. 13. Process corner simulation results of the QILO frequency resolution Δf at T = −25 °C, 27 °C, and 100 °C. (a) Process corner model = FF. (b) Process corner model = TT. (c) Process corner model = SS.

The X3-QILO employs two identical oscillators that consist of coupling transistors, 5-bit switched-C arrays, *LC* tanks, and injection transistors. The quadrature signals injection achieves a wide locking range with high I/Q phase accuracy, compared to single-side differential injection. Therefore, the bit number of switched-C array can be optimized for achieving wider frequency calibration range. The QILO utilizes the third harmonic of the injection current to establish frequency locking with locking range typically less than 3% due to relatively small third-harmonic power compared with the fundamental signal power. To calibrate out the narrow locking range, the 5-bit switched-C array in each *LC* tank of the X3-QILO is controlled by a 5-bit counter from the feedback path.

The frequency-locking range Δf_L is inversely proportional to the *LC* tank Q [16]. The tank Q decreases with temperature increasing due to a higher thermal resistance effect. Fig. 12(a) shows typical simulation results of the QILO *LC* tank Q variation over the temperature change from −25 °C to 100 °C for FF/TT/SS process corners. It is seen that the *LC* tank Q varies from 6.5 to 9.7 over the frequency range of 25–30 GHz. The corresponding Δf_L ranges from 252 to 348 MHz, over all combinations of the process corner models and temperature variations, as can be shown in Fig. 12(b). In the TT corner, Δf_L is typically 300 MHz with ∼12% variation over the temperature change. With 26.4–30 GHz 5-bit tuning range, the nominal Δf is 112.5 MHz. The peak-to-peak Δf variation ranges 100–170 MHz, over all combinations of switched-C array codes, process corners (FF/TT/SS), and temperature variations from −25 °C to 100 °C in simulations (Fig. 13). This is close enough to the theoretical optimum Δf MIN–MAX range of 120–150 MHz from (7) for the 1-LSB PN calibration, assuming Δf_L = 300 MHz and $f_{\mathrm{AM,MIN}}$ = 60 MHz, and no failure case is observed in the process corners

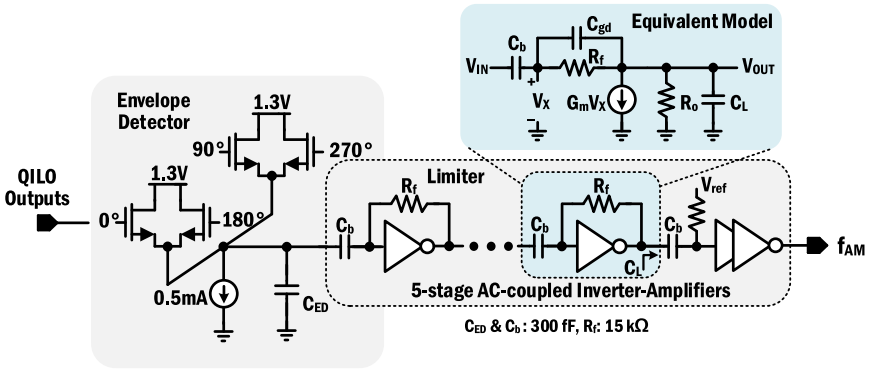


Fig. 14. Schematic of the envelope detector and limiter comprised of five-stage inverter–amplifier followed by CMOS inverters.

and temperature simulations as well as in the measurements (see Fig. 22). The current consumption of each core VCO cell is 8 mA from a supply voltage of 1.3 V.

B. Envelope Detector and Limiter

Fig. 14 shows the schematic of the envelope detector and limiter. The quadrature signals of the X3-QILO are applied to the envelope detector which consists of a source follower, a load capacitor C_{ED}, and a current source. The envelope wave is held at the load capacitor of which discharging time constant depends on the impedance of the active load and bias circuit. The output signal of the envelope detector will be a constant dc value when injection-locked condition, while it will produce a sinusoidal signal of which frequency is governed by (1) when injection-unlocked state. Since the envelope wave under unlocked status exhibits a small swing of typically less than 50 $\mathrm{mV_{pp}}$, the limiter is cascaded next to the envelope detector to convert the envelope wave to rail-to-rail pulses.

The limiter is a cascade of five stages ac-coupled CMOS inverter amplifiers followed by full-swing CMOS inverters. After amplifying the small envelop wave, the inverters generates rail-to-rail pulses with logic threshold being referenced to V_{ref}. To filter out low-frequency envelope wave when the envelope detector senses quasi-lock or to prevent false pulses due to switching noise in the switched-C array, the overall gain response of the limiting amplifiers is bandpass shaped by leveraging node poles and zeroes created by the transistor parasitics, C_{ED}, C_b, and R_f. The operational frequency range of the IFLL is determined by the frequency response of the limiter. Fig. 15 shows typical simulated gain response of the five-stage limiting amplifiers chain. The minimum detectable frequency ($f_{\mathrm{AM,MIN}}$) is around 60 MHz, about 20-dB gain crossing point in the gain response. The amplitude of the envelope wave becomes smaller as the frequency gap of $|f_{\mathrm{osc}} - 3f_{\mathrm{inj}}|$ increases. Thus, it requires higher gain from the series limiting amplifiers as the frequency offset (or f_{AM}) increases to develop a strong voltage swing enough for driving the inverters to generate pulse signal. In simulations, the maximum detectable frequency ($f_{\mathrm{AM,MAX}}$) is around 6 GHz where the overall gain of the limiting amplifiers is about 40 dB (Fig. 15). Note that since $f_{\mathrm{AM,MAX}}$ is far greater than the

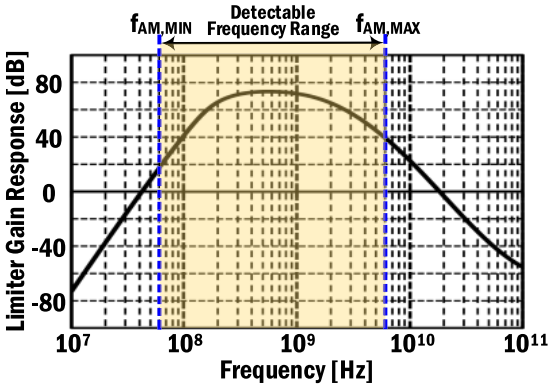


Fig. 15. Simulation results of the limiter gain response.

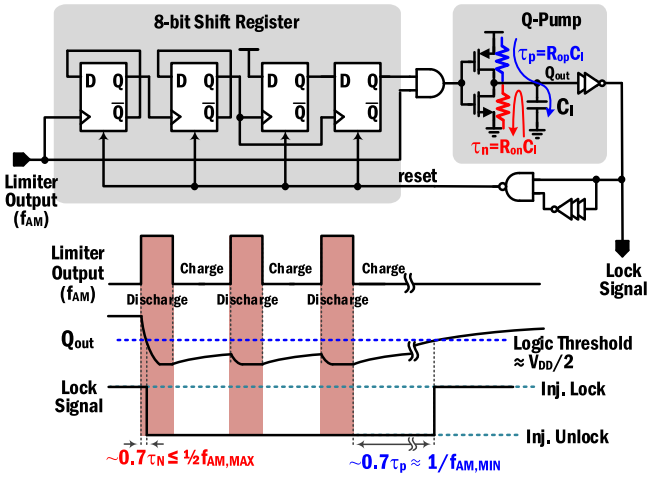


Fig. 16. Lock detector and conceptual timing diagram for generating lock signal.

X3-QILO MIN–MAX frequency interval ($=f_{\mathrm{MAX}} - f_{\mathrm{MIN}}$), there is no limitation on the maximum detectable frequency as long as the $3f_{\mathrm{INJ}}$ injection frequency falls inside the MIN–MAX frequency range.

C. Lock Detector

To initiate the PN calibration, we need to create a lock signal first, judging the frequency acquisition is completed by the feedback loop. Fig. 16 shows the schematic and timing

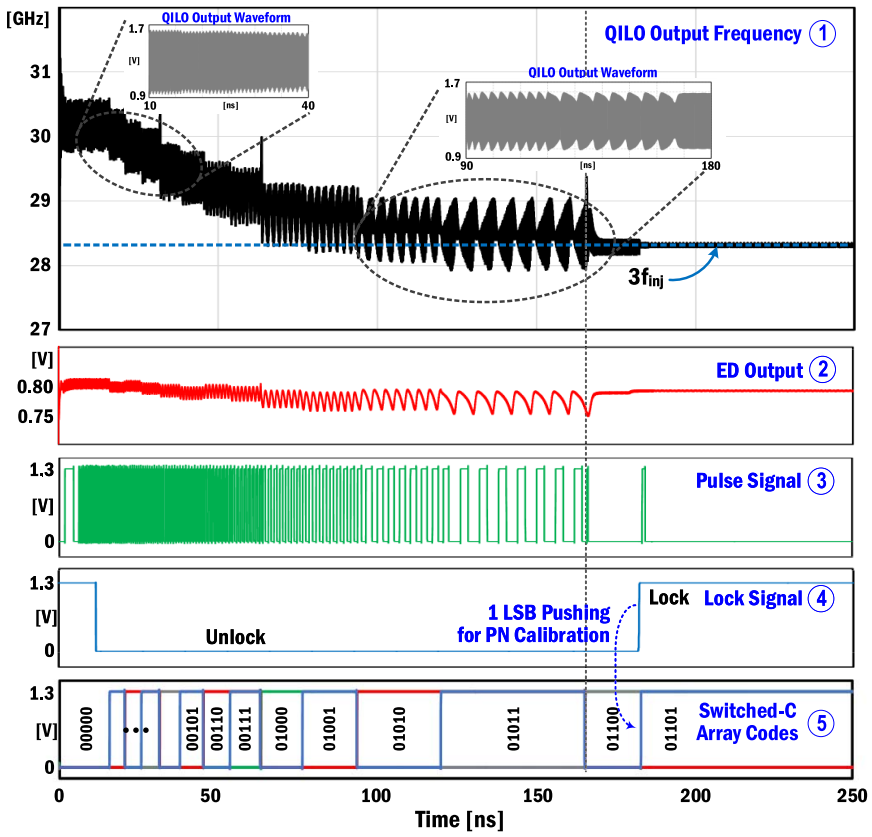


Fig. 17. Typical SPECTRE transient simulation results when the initial free-running frequency of the QILO, $f_{\rm osc}$, is 30.1 GHz and the QVCO output freqeuncy, $f_{\rm inj}$, is 9.43 GHz.

diagram of the lock detector. It consists of an 8-bit shift register and a charge (Q)-pump. When unlocked, the contiguous sequential pulses from the proceeding limiter are applied to the lock detector. Subsequently, the shift register and AND gate produce pulses after counting eight consecutive pulses and drives the Q-pump that discharges the integration capacitor C_I (2 pF) progressively. Then, the lock signal becomes "low," which enables the upper path of the feedback controller to update the QILO frequency in Fig. 2. The limiter may generate irregular pulses due to small signal disturbance during settling time, which could cause false signal to update the QILO frequency. To prevent this malfunction, the shift register drives the AND gate only after evaluating eight consecutive pulses, as a way to making sure that the pulse is generated because of the frequency unlocked state.

After completing the frequency calibration, there will be no envelope signal and the AND gate output becomes "low." Then, the Q-pump charges C_I. Consequently, the lock signal transits from "low" to "high." This disables the upper path but enables the lower path of the feedback controller in Fig. 2 for 1-LSB capacitance code shift to calibrate PN. The C_I charging and discharging times are determined by the time constants of τ_p ($=R_{\rm op}C_I$) and τ_n ($=R_{\rm on}C_I$), respectively. $R_{\rm op}$ and $R_{\rm on}$ are turn-ON resistance of the PMOS and NMOS, respectively, in the Q-pump. We set the design condition of $0.7\tau_n \le 1/(2f_{\rm AM,MAX})$ to guarantee discharging of C_I below logic threshold level ($\approx V_{\rm DD}/2$) of an inverter during the pulse ON-time period in the frequency calibration mode. Also, τ_p is designed to meet $0.7\tau_p \approx 1/f_{\rm AM,MIN}$ by sizing the PMOS to generate lock signal for PN calibration approximately within one clock period of the maximum envelope pulse period. In this paper, $f_{\rm AM,MIN}$ is about 60 MHz, resulting in 20–25 ns of additional time for the PN calibration. Therefore, the complete IFLL calibration time will be the frequency-locking time calculated in Section II-B plus the PN calibration time, resulting in <300 ns for 99% settling time.

IV. IFLL Transient Simulation Results

Fig. 17 shows typical transient simulation results at each designated node of the IFLL in Fig. 2 when the output of the QVCO $f_{\rm inj}$ is 9.43 GHz and initial free-running frequency of the QILO, $f_{\rm osc}$ is 30.1 GHz. The envelope magnitude is a nonlinear function of $f_{\rm AM}$ and due to the far distance between $3f_{\rm inj}$ and $f_{\rm osc}$, the QILO is unlocked and output envelope magnitude is small (less than 50 $\rm mV_{pp}$) at the beginning of the calibration, <20 ns in Fig. 17 ① and ②. However, the limiter produces rail-to-rail pulses due to a large gain, more than 60 dB at $f_{\rm AM} = 1.8$ GHz, in Fig. 17 ③ and initiates the frequency calibration loop, decreasing $f_{\rm osc}$ to 28.3 GHz ($3f_{\rm inj}$) progressively in a nonlinear fashion as the switched-C array code being updated per every eight clock cycle of the $f_{\rm AM}$ in Fig. 17 ⑤.

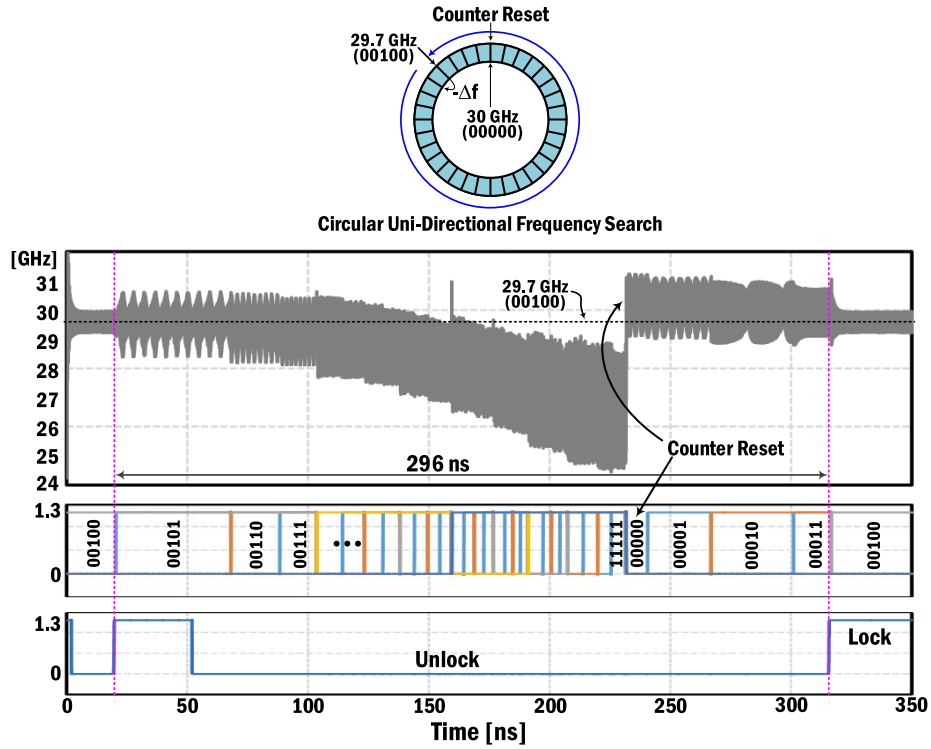


Fig. 18. Typical SPECTRE transient simulation results of a worst case frequency tracking in the presented circular uni-directional frequency search—when the QILO frequency is intentially lowered by 1-LSB Δf from the initial 29.7 GHz of injection-locked freqeuncy at 20 ns, the IFLL searches the 29.7 GHz by one-cycle rotating the 5-bit counter within 296 ns, approximately the same as the 99% settlilng time estimated by the linear feedback model (6).

When $f_{\rm osc}$ approaches toward the edge of the locking range (300 MHz) at around 130 ns, the AM modulation effect in the QILO output becomes more prominent in the sub window in Fig. 17 ①. After eight pulses the feedback counter updates the switched-C array code to 01100, locking the QILO to the QVCO at the edge of the locking range. Subsequently, after frequency locking the Q-pump starts to charge C_1 creating lock signal which pushes one more LSB code up to 01101 at around 175 ns in Fig. 17 ④ and ⑤, pushing $f_{\rm osc}$ closer to 28.3 GHz to calibrate PN in Fig. 17 ①. Note that the 8-bit SR plays as a pulse filter, requiring eight consecutive pulses to drive the Q-pump; for instance, due to a brief transient waveform uncertainty there are burst of irregular pulses after locking in Fig. 17 ③ at ∼180 ns, which are, however, ignored by the pulse filter, as discussed in Section II-B.

A worst-case freqeuncy tracking scenario in the presented circular uni-directional frequency searching scheme is shown in Fig. 18. Suppose the X3-QILO is initially locked to 29.7 GHz (equivalent switched-C code: 00100). Then, the QILO frequency is intentionally decreased by 1-LSB Δf to 00101 at 20 ns. This initiates the freqeuncy tracking loop which incrases the switched-C code sequentially all the way up to its maximum (11111), alternatively decreasing the X3-QILO frequency successivley down to the minimum of 26.4 GHz around 230 ns. After that, the 5-bit counter modulo-32 operation refreshes the switched-C code to its minimum (00000). This forces the X3-QILO frequency to its maximum and the IFLL continues decreasing the frequency until it is locked to the initial 29.7 GHz. This uni-directional downward freqeuncy searching eliminates any directional ambuigity in tracking frequncy and is clearly modeled by subtracing Δf in the feedback model shown in Fig. 4. The overall frequency searching time by circulating the 5-bit counter values over one cycle is governed by the settling time characterized in (6), completing the frequency re-acquisition in ∼300 ns as expected in Fig. 18.

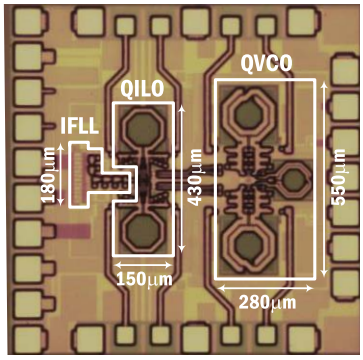


Fig. 19. Chip photograph of the IFLL integrated with the QVCO and X3-QILO (chip size including pads: 1 × 1 mm^2).

V. Experimental Results

Fig. 19 shows the chip photograph of the proposed IFLL integrated with the QVCO and X3-QILO, manufactured in 0.13-μm CMOS process. The IFLL is characterized with

TABLE I
PERFORMANCE SUMMARY AND COMPARISON OF THE CALIBRATION CIRCUIT

	Tech	Feature	Locking Range (%) (w/o Calibration)	VDD (V)	Power (mW)	Area (mm^2)	Locking Time	Operation
JSSC 2013 [12]	65nm CMOS	PLL+Mixer +Doubler	11.2 (0.5)	1.2	65	~0.95*	< 42.7 us	Externally Controlled
This Work	130nm CMOS	Envelope Detector	11.4 (1)	1.3	2.4	0.015	< **300 ns	Autonomous

*Estimation based on chip photograph. **Estimation based on simulations.

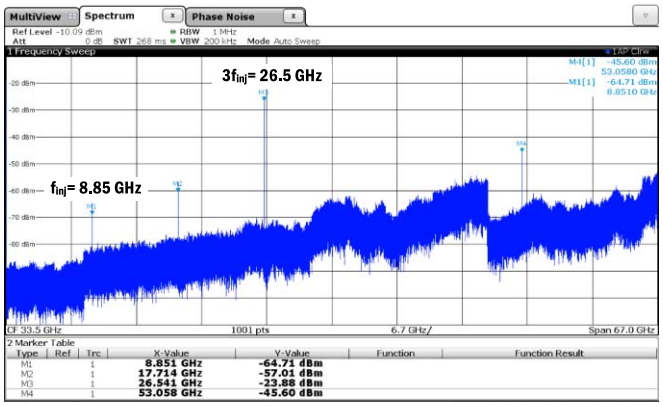
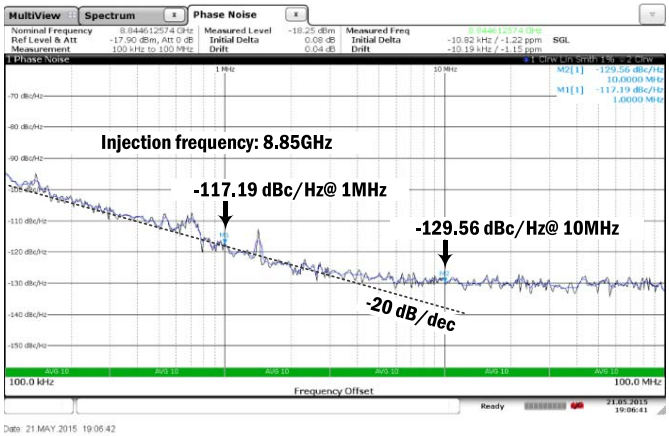
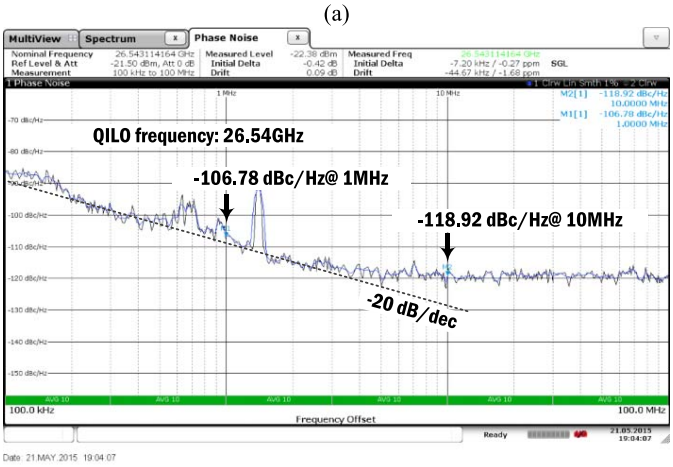


Fig. 20. Typical measured power spectrum at the output of QILO after injection locking by the IFLL (f_{inj} = 8.85 GHz and $f_{\text{osc}} = 3f_{\text{inj}}$ = 26.5 GHz).



(a)



(b)

Fig. 21. Measured PN performance. (a) At the output of the QVCO (f_{inj} = 8.85 GHz). (b) At the output of the QILO ($f_{\text{osc}} = 3f_{\text{inj}}$ = 26.54 GHz).

on-wafer testing using GSSG probes for RF signal transition at the VCOs outputs. Since all digital circuits are driven autonomously by the envelope pulse, no external control clock is required. The typical measured power spectrum at the output of the X3-QILO after being third harmonically injection locked by the IFLL is shown in Fig. 20 where f_{inj} from the QVCO is 8.85 GHz and f_{osc} (=$3f_{\text{inj}}$) from the X3-QILO is 26.5 GHz. The measured peak output power at 26.5 GHz is −23 dBm after some power loss from the measurement cables and probe transition. The injection signal at 8.85 GHz is suppressed by more than 40 dBc in the X3-QILO (Fig. 20).

The measured typical PN of the QVCO at 8.84 GHz is −117.2 and −129.6 dBc/Hz at 1- and 10-MHz offsets, respectively, as shown in Fig. 21(a). When the QILO is third-harmonically locked by the QVCO, the PN degradation is consistently about 10.5 dB at both 20 dB-rolloff and flat regions, resulting in the PN of −106.8 and −118.9 dBc/Hz at 1- and 10-MHz offsets, respectively, at 26.54 GHz in Fig. 21(b).

More comprehensive PN measurement results over frequency are shown in Fig. 22. The measured QVCO PN at 5-MHz offset ranges from −130 dBc/Hz at 8.8 GHz to −115 dBc/Hz at 9.9 GHz, as shown in Fig. 22 ①. With the IFLL disabled and by decreasing the QVCO f_{inj} from 9.9 to 9.8 GHz, the QILO can maintain locking from 29.7 GHz down to 29.4 GHz (Δf_L = 300 MHz, QILO free-running f_{osc} = 29.55 GHz) but the PN degrades by 18–20.5 dB at the edges of Δf_L from the minimum of −107.5 dBc/Hz in Fig. 22 ②. Thus, more effective locking range claiming only 10–10.5 dB PN degradation from the QVCO PN is from 29.48 to 29.66 GHz (180 MHz), which is 60% of Δf_L as shown in Fig. 22 ③ and ④. However, when the IFLL enabled, the QILO can track the QVCO injection frequencies and exhibit consistent 9–10 dB PN degradation with ±1 dB error for the entire measurement range from 26.4 to 29.7 GHz in Fig. 22 ③.

To verify the functionality of the PN calibration, the PN calibration routine is ON/OFF controlled externally. When the X3-QILO's free-running f_{osc} is 29.7 GHz and the QVCO's

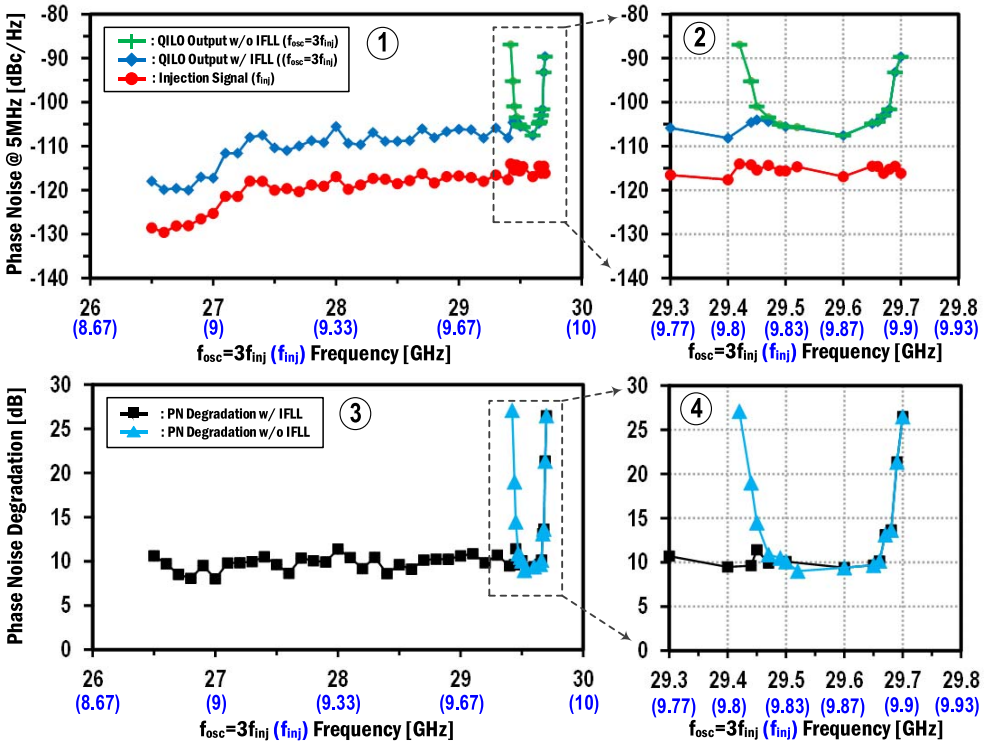


Fig. 22. Measured QVCO and QILO PNs with and without enable the IFLL [① and ②], and the PN degradation in the QILO with and without enabling the IFLL [③ and ④].

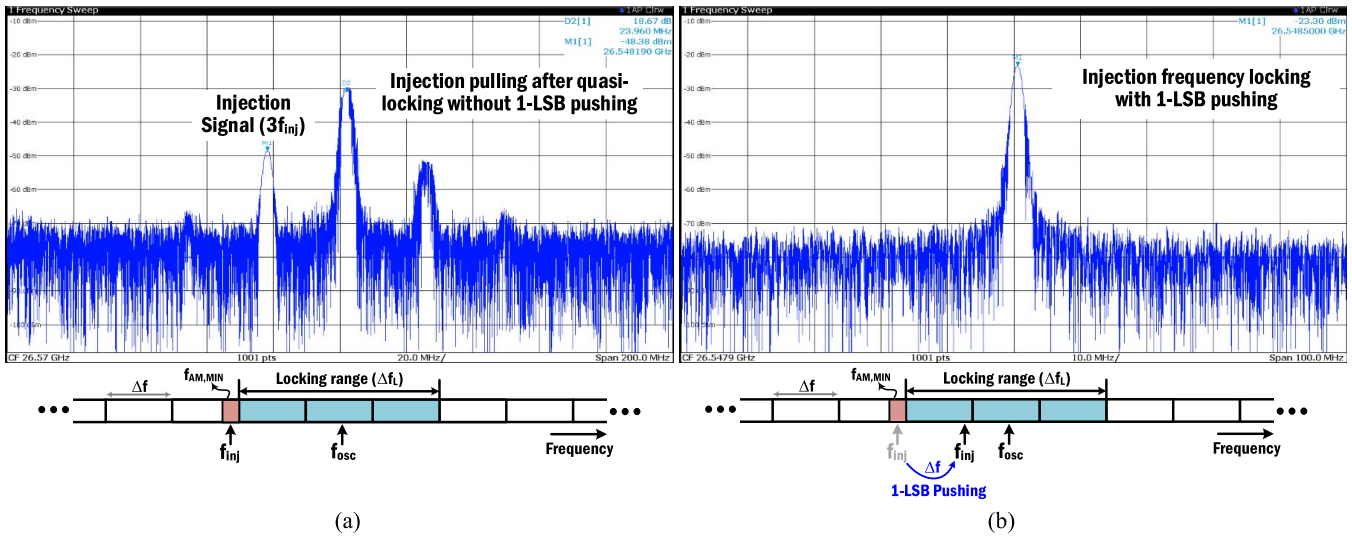


Fig. 23. Functional verification of the PN calibration when the QILO ($f_{\rm osc}$ = 29.7 GHz) is quasi-locked to the third harmonic of QVCO ($3f_{\rm inj}$ = 26.548 GHz) at the edge of the locking range (a) with disabling and (b) with enabling the 1-LSB pushing PN calibration routine.

$3f_{\rm inj}$ is 26.548 GHz, by disabling the PN calibration routine the IFLL calibrates the X3-QILO frequency to be closer to 26.548 GHz. But, a quasi-locking to the injection frequency is taken place near the edge of the locking range because of the finite detectable frequency resolution of $f_{\rm AM,MIN}$ which is estimated as 60 MHz as discussed in Section III-B. Consequently, this prompts the injection pulling phenomena and instigates side tones in Fig. 23(a). The offset frequency from the edge of the locking range can be estimated by the frequency distance between the side tones, which is 23.9 MHz in Fig. 23(a). When PN calibration is turned on, the QILO can be fully locked to the QVCO after 1-LSB Δf pushing and no side tone is observable in Fig. 23(b).

Fig. 24 details power consumption and area penalty by each function block. The QVCO and QILO, excluding 50-Ω test buffers, consume 14.4 and 20.8 mW from the supply voltage of 0.9 and 1.3 V, respectively. The total power consumption in the calibration circuits is 2.4 mW, where most of the dc power

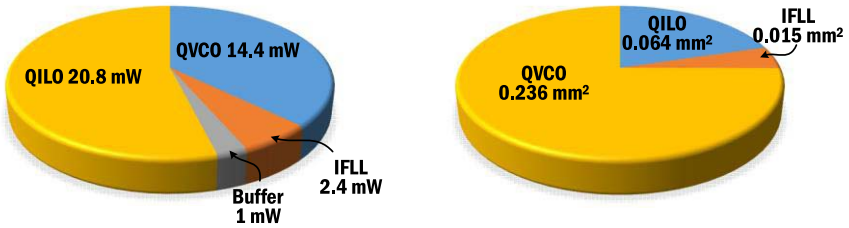


Fig. 24. Details of (a) dc power dissipation and (b) area penalty by each function block.

TABLE II
PN PERFORMANCE COMPARISON WITH PRIOR STATE OF THE ART

	Tech	Phase	Frequency (GHz)	VDD (V)	Power (mW)	Phase Noise (dBc/Hz@1MHz offset)	Chip Area (mm^2)	Feature
ISSCC 2013 [20]	130nm SiGe	Diff.	27.9-37.8	1.5	10 (VCO only)	-103.6 @32.9 GHz	1.93	BiCMOS Cross-coupled Pair VCO
JSSC 2011 [17]	65nm CMOS	Quad.	67.2-67.7	1.2	68	-95 @60 GHz	0.8 (QILO only)	PLL+QILO w/ Dual Injection
JSSC 2013 [12]	65nm CMOS	Quad.	58.1-65	1.2	137	-96 @61.5 GHz	3.8	PLL+QILO + Calibration Circuit
This Work	130nm CMOS	Quad.	26.5-29.7	1.3	*38.6 (**49.7)	-106.8 @26.5 GHz	1	QVCO+QILO + Calibration Circuit

*Without VCO output buffers.
**With including VCO output buffers for measurement with 50-Ω instruments.

is dissipated by static current of the envelope detector and the limiter [Fig. 24(a)]. The area penalty by the calibration circuits is negligible, as can be shown in Fig. 24(b).

Table I summarizes the measured performance of the IFLL and comparison with prior mixer-based calibration technique [12]. In the proposed IFLL, the frequency calibration is initiated autonomously by detecting a slave VCO's envelope disturbance bearing the frequency difference between a master injection VCO and the slave VCO. Once, the envelope information is converted to a pulse signal via series of envelope detector and limiter, all feedback control loop is configured in the pure digital domain, which can simplify the calibration hardware and achieve a fast speed. Furthermore, the envelope signal is a low-frequency signal, claiming a small dc power dissipation from the digital feedback circuitry. These lead to more than 140 times faster locking time with 27 times less power dissipation, while achieving equivalent 11.4% of frequency locking range with much smaller area penalty, compared with the prior work. Also, the proposed IFLL entails PN calibration and the PN performance of the LO generator is on a par with other state-of-the-art designs when the frequency is scaled to similar ranges, as compared in Table II.

VI. CONCLUSION

This paper presents a power-efficient and hardware-economic mixed-mode injection frequency tracking feedback system. In the proposed IFLL, the frequency error between a master injection VCO and a slave locking VCO is extracted from the slave VCO's envelope waveform using an envelope detector. The frequency of the envelope wave bears the frequency error information which is subsequently converted into pulse frequency by a limiting amplifier. This pulse signal enables digital feedback circuitry to update the slave VCO's output frequency so that it can track the injection frequency in a closed-loop control manner. This frequency calibration persists until the two VCOs become locked by each other. Thus, the calibration process is purely autonomous, self-initiating whenever the AM modulated envelope waveform is generated. This completely eliminates any external control signal and relevant hardware associated with generating the control signal. This not only greatly simplifies the feedback control system but it can also achieve much higher power efficiency and faster calibration speed with much smaller area penalty, compared with prior state of the arts. Finally, by incorporating a PN calibration routine the proposed injection-locking system can resolve the intractable issue of PN degradation at the edge of the slave VCO's injection locking range, resulting in one of the largest injection frequency tracking ranges.

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