Low-Power Noise-Immune Nanoscale Circuit Design Using Coding-Based Partial MRF Method

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***Abstract*— Reliability is one of the major concerns for ultralow power circuit designs. Markov random field (MRF) techniques have been applied to logic circuits to resist random noise when operating under ultralow supply voltage or sub-threshold voltage. Although conventional MRF networks can be easily mapped onto simple logic circuits, it becomes difficult when the circuits are large and complex. In this paper, we present a general coding-based partial MRF (CPMRF) method for multi-logic operations in one basic unit, which is referred to as a CPMRF pair. A CPMRF pair saves circuit area by sharing a common MRF network. It also inherits noise immunity from the MRF theory while obtaining noise immunity from the coding structure as a combination of robust "1s" and "0s." The resulting architectures become more cost effective than conventional ones. To validate the performance of our proof-of-concept design, we fabricated a carry-lookahead adder implemented by the proposed CPMRF pairs using IBM 130-nm CMOS technology. Measurement results indicate that the CPMRF CLA can achieve high noise tolerance with 20% improvement while occupying 37.7% less area and reducing power consumption by 93% compared with the master-and-slave MRF CLA design.**

***Index Terms*— Carry-lookahead adder, clique energy, low power, Markov random field (MRF), noise immunity, probabilistic design.**

I. Introduction

THE continuous miniaturization of electronic components has enabled rapid growth of microelectronics over the past decades. One of the most important attributes of nanoscale devices is their low-power consumption. However, when the supply voltage is scaled down, the energy difference between logic states is comparable to the surrounding noise, rendering the resulting circuit vulnerable to operational uncertainty and logic failures [1]. These signal errors are dynamic in nature, occurring anywhere in the circuit, and are difficult to detect by regular testing methodologies [1]. Such errors are often referred to as "dynamic errors." As the dimensions of devices scale down further into the nanometer realm, one of the major challenges we will need to confront is the increasing prevalence of dynamic errors in nanoscale logic circuits.

An error-free logic operation is assumed in the design of conventional CMOS digital circuits and systems. It implies that conventional circuit designs mainly focus on the data transmission errors due to capacitive–inductive crosstalk [2], [3], ground bounce, and IR drops [4]. However, this assumption is not applicable to circuit designs in the nanoscale realm when an ultra-low supply voltage is adopted. Because the uncertainty in signal faults is inherent in nanoscale computing systems, conventional design methods (crosstalk [5], ground bounce [6], and IR drops [7]) cannot effectively solve the random noise problems, which are intrinsic to nanoscale VLSI systems [8], [9]. Implementing reliable Boolean functions by using noisy logic gates was first proposed by Von Neumann [10]. With noisy gates, conventional noise-immunity techniques, such as triple modular redundancy (TMR) [11], will add hardware redundancy to handle faults. However, due to these logic gates also being prone to errors, intrinsic noise can significantly interfere with individual redundant modules, and thus noisy signals often lead to incorrect results of the voters in TMR. As a result, the TMR-based structures cannot effectively solve the random intrinsic noise that often occurs in nanoscale circuits.

Recently, three new alternative and innovative probabilistic techniques were proposed. They are stochastic computation (SC) [12]–[18] at the number representation level, algorithmic noise tolerant (ANT) techniques [19]–[21] at the algorithmic level, and probabilistic CMOS (PCMOS) [22] at the circuit level. SC is an un-weighted number representation, which represents a number by a bitstream. For example, 0.3 is represented as a stochastic bitstream "1, 0, 0, 1, 1, 0, 0, 0, 0, 0" where the probability of the occurrence of bit "1" represents the value. Although stochastic representation can be implemented by much simpler logic compared with

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traditional representation, the propagation delay of SC systems is proportional to the length of bitstreams, which renders such techniques unsuitable for high-speed VLSI design. In addition, a few SCs have been implemented for noise-tolerant circuit designs under an ultra-low supply voltage. Based on ANT, the design in [19] focuses on low-complexity and reduced precision redundancy (RPR) modules to compensate for errors in the main computing unit. This technology is power efficient since the main unit operates under a low supply voltage, while the RPR modules are supplied at a regular voltage. If the main unit and the RPR modules work under the same ultra-low supply voltages, dynamic errors can influence both the main unit and the RPR modules such that the performance loss cannot be compensated for. Another probabilistic technique, PCMOS, is a model used in noise-tolerant designs [22]. Its performance depends on the chosen noise model. However, there is no prior knowledge about the distribution of intrinsic noise in nanoscale circuits. Therefore, such a model is not suitable for noise tolerant designs.

In contrast to the above approaches, Markov random field (MRF) theory is applied on circuit designs as a probabilistic-based technique to deal with the issue of noise. Recently, many researchers have adopted this approach in the circuit design to handle dynamic errors [23]–[34]. In the probabilistic framework, it is unreasonable to assume each logic value, as each node in a real circuit can stay correct at all times. What we can expect is that the probability distribution of these values will have the highest likelihood in a correct logic state. The appropriate mathematical framework according to the analysis is MRF, which optimizes the values of a large set of random variables so that their overall joint probability is a global maximum. In a logic circuit, hundreds of internal logic signal paths exist from the inputs to the outputs. Only one set of variable assignments has the highest probability of being correct, and the correct set corresponds to the optimum setting. The propagation of logic states through the network is orchestrated such that the distribution of each variable is at its local probability maximum in order to achieve the correct logic values at the output. Through this design paradigm, MRF circuits can achieve high noise immunity under ultra-low supply voltages [24]. However, there exist significant shortcomings of traditional MRF designs due to its complex hardware architecture. MRF-based circuits often require 20 times the number of transistors as compared to traditional circuit implementations. To minimize this shortcoming, area-performance optimization becomes the major challenge for using MRF-based designs. An area-efficient MRF structure [31] and a master-and-slave (MS) [28] MRF can achieve about 50% area saving compared to the original MRF circuits. However, the MS-based units experience a performance loss as studied in [33]. An area-sharing cyclic structure was proposed in [30] having high area efficiency with shared structures. Unfortunately, the structures cannot implement the complete MRF clique energy functions, and thus the system performance is limited. A hardware-efficient feedback-based design combines the idea of MRF and the Schmitt trigger to enhance the noise immunity based on the MS design, but it increases power consumption and time delay [34]. Meanwhile, the traditional MRF design pays attention to the structure of each logic operation, which limits this method for further VLSI structure design.

In this paper, we propose a coding-based partial MRF (CPMRF) method for multi-logic operations. First, we divide the MRF clique energy, U, into two subsets $\{U_0, U_1\}$. Here, U_0 is the clique energy corresponding to logic output "0," while U_1 is for logic output "1." In logic circuits, there arise many instances of asymmetric gates, including NAND, NOR, AND, as well as OR gates. For example, a NAND gate has an asymmetric probability distribution for its output (three logic "1" outputs versus one logic "0" output) when its inputs satisfy the Bernoulli distribution. We discovered that some asymmetric gates can be paired with others such as an AND–NOR pair to complement the clique energy with each other, referred to as complementary pairs. On the contrary, there are non-complementary gate pairs, such as a NOR–NOR pair. Based on these observations, we propose a CPMRF method using complementary gate pairs and non-complementary gate pairs. In the previous work, a partial-clique-energy MRF design [35] was carried out to investigate its area efficiency. However, it has some limitations: 1) it only considers designs for complementary gate pairs; 2) output logic operations must correspond to input logic operations; and 3) it does not summarize a general mapping method. Aiming to overcome these limitations, the proposed CPMRF, which combines the idea of partial-clique-energy with the idea of strong/weak outputs implemented by the coding structures, achieves: 1) general mapping methods for both complementary and non-complementary gate pairs and 2) multi-logic operations not limited to input logic operations. Therefore, the prime novelty of the proposed CPMRF method lies in offering: 1) a general design method to achieve multi-logic operations by specially designed coding structures for partial MRF gate pairs and 2) large area and power savings while maintaining high noise immunity.

The rest of this paper is organized as follows. Section II clearly introduces the MRF theory and previous MRF circuit designs. Section III presents a general CPMRF design method for complementary gate pairs and non-complementary gate pairs. In Section IV, we implement an 8-bit CPMRF carry-lookahead adder using the IBM 130-nm process to prove the effectiveness of the proposed method. This paper is concluded in Section V.

II. MRF-Based Circuit Design Methodology

The MRF circuit design is based on the MRF theory [27]. It involves the mapping from a multi-level Boolean logic circuit to an MRF network followed by the mapping from an MRF network to MRF standard cells. In this section, we will introduce some basic concepts and the mapping processes involved in the MRF design.

A. Markov Random Field Theory

Let $\mathbf{X} = \{x_0, x_1, \ldots, x_n\}$ be a set of random variables. A graph example is shown in Fig. 1, where

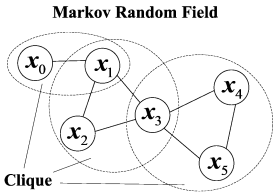

Fig. 1. Graph example of MRF.

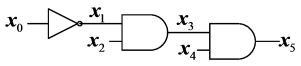

Fig. 2. Logic circuit.

$X = \{x_0, x_1, \ldots, x_5\}$. These variables are connected to each other either directly or indirectly. The subset of X, in which variables are directly connected with each other, is defined as a clique [24]. In Fig. 1, cliques are $\{x_0, x_1\}$, $\{x_1, x_2, x_3\}$, and $\{x_3, x_4, x_5\}$. Variables in a clique show obvious dependence marked by edges between two variables in Fig. 1. In these subsets, one directly connected variable beside the other is called a neighbor [24]. x_0 is a neighbor of x_1. The probability of an MRF variable depends only on its neighborhood. These variables form an MRF if the collections of the random variables satisfy positivity, which means the probability of a variable can be neither negative nor zero and markovianity, which means that a variable must be independent of others except for those in its neighborhood [27].

B. Mapping a CMOS-Circuit to an MRF Network

The transformation from multi-level CMOS circuits to an MRF network is as follows.

1) Variables in an MRF graph correspond to input/output nodes in a logic circuit with the logic values "0" or "1."
2) Edges in an MRF graph represent the dependence between the input/output nodes corresponding to a variable and its neighborhood in a clique.

Followed by the above rules, a logic circuit, shown in Fig. 2, can be mapped to an MRF network in Fig. 1. The input/output nodes $x_0, x_1, \ldots, x_5$ correspond to the same variables in Fig. 1. The input/output nodes in a logic gate form a clique in Fig. 1. Three logic gates represent three cliques. After the transformation, we can apply the MRF theory to the nodes in a circuit. According to the Hammersley–Clifford theorem, the joint probability for the whole set of nodes in a circuit is the product of all clique energy functions [24]

$$P(X) = \prod_{c \in C} \frac{1}{Z} \exp\left(\frac{-U_c(x_c)}{k_b T}\right) \tag{1}$$

where Z is a normalization constant, C is the set of all cliques, $U_c(x_c)$ represents the clique energy for a clique x_c, and $k_b T$ is the thermal energy. Note that the reliability of a circuit can be translated to the likelihood of the joint probability for all correct states, which is represented by their clique energy in (1). Thus, maximizing the reliability of a circuit is analogous to achieving the highest joint probability for all correct states corresponding to the lowest clique energy [23].

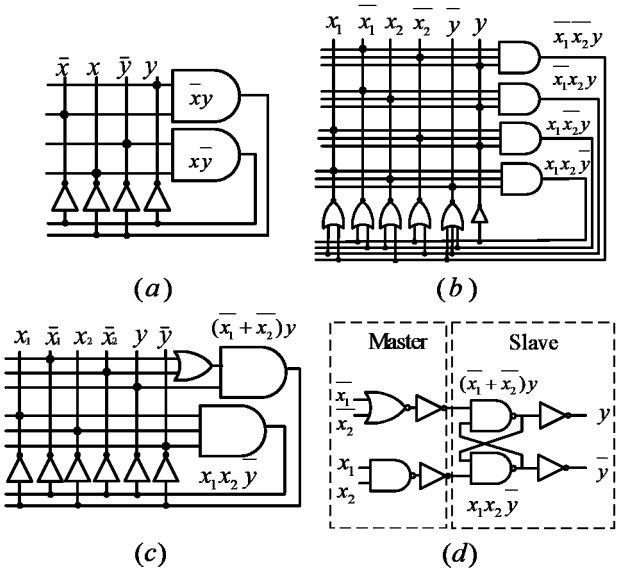

Fig. 3. MRF circuits. (a) MRF inverter [24]. (b) MRF NAND [24]. (c) Area-efficient MRF NAND [31]. (d) MS MRF NAND [28].

TABLE I
ENERGY TRUTH TABLE OF AN INVERTER

Input x	Output y	State	Clique Energy $U(x,y) = -(\bar{x}y + x\bar{y})$
0	0	incorrect/invalid	0
0	1	correct/valid	-1
1	0	correct/valid	-1
1	1	incorrect/invalid	0

C. Mapping an MRF Network Onto an MRF-Based Circuit

High-performance basic MRF logic gates are designed to obtain an MRF-based circuit mapped from an MRF network. Note that we can maximize the joint probability by minimizing the clique energy instead, as shown in (1). The rules of an MRF-based design are intended to satisfy the requirement that the clique energy of correct logic states should be lower than that of incorrect logic states as the following points.

1) The energy truth table is formed by the clique energy terms of the valid/invalid input–output states. Assume that $f(x_0, x_1, \ldots, x_n)$ is an operation function for the input $\mathbf{X} = \{x_0, x_1, \ldots, x_n\}$ in the same clique, $f = 0$ when the MRF network operates incorrectly, otherwise $f = 1$.
2) Let the clique energy $U_c(x_c) = -\sum_i f_i(x_0, x_1, \ldots, x_n)$ be the entire state (i represents the different input values, for example, $i = 0$ refers to $\{0, 0, \ldots, 0\}$) of an operation, where the design of the MRF-based elements depends on the function $U_c(x_c)$, where $f_i = 1$.

The energy truth table of an inverter [see Fig. 3(a)] is shown in Table I, including its correct and incorrect states. The energy function $U(x, y) = -(\bar{x}y + x\bar{y})$ represents the clique energy of an inverter (the rules of symbolic Boolean logic in terms of

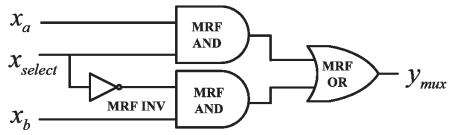

Fig. 4. Local mapping-based MRF MUX.

algebraic operations are shown in [25]). In Fig. 3(a), the upper NAND can implement the clique energy function x'' and the lower NAND is designed for the implementation of xy''. These two NAND gates help strengthen the input and output signals. Although there are feedback loops in the MRF circuit design, the structures are still considered to be combinational logic, since the output only depends on its present inputs. Obviously, the feedback loop in combinational noise-tolerant logic is a characteristic of the MRF-based design, which comes from the clique energy function. The MRF-NANDshown in Fig. 3(b) is a direct hardware implementation based on the clique energy as follows [24]:

$$U(x_1, x_2, y) = -(\overline{x_1 x_2}y + \overline{x_1}x_2 y + x_1\overline{x_2}y + x_1 x_2\overline{y}). \quad (2)$$

The MRF-NAND structure is modified based on an equivalent transformation of clique energy function [28]

$$U(x_1, x_2, y) = -[(\overline{x_1} + \overline{x_2})y + x_1 x_2\overline{y}]. \quad (3)$$

Fig. 3(c) shows a cost-effective structure of an MRF-NAND based on the equivalent transformation in (3). The MS MRF-NAND in Fig. 3(d) separates the truth table into two groups, and it is the most area-efficient implementation compared with the others. Nevertheless, the complexity of MRF elements is still a bottleneck for an MRF-based VLSI design. For example, the MRF-based MUX in Fig. 4 consumes 6∼12 times the area of a traditional MUX. Clearly, there is an issue of excessive area required for a complex logic design, since each logic gate should be replaced by a corresponding MRF version in the circuit.

III. Coding-Based Partial MRF Methodology

In this section, a CPMRF method is proposed based on sub-clique energy where the clique energy is asymmetric. First, a PMRF AND–NOR pair is proposed as an example for complementary pairs.

According to the truth table of an AND–NOR pair in Table II, the partial clique energy U_p of AND is

$$\begin{aligned} U_{p-\mathrm{AND}}(x_1, x_2, y) &= -\overline{x_1}\cdot x_2\cdot\overline{y} - x_1\cdot\overline{x_2}\cdot\overline{y} - \overline{x_1}\cdot\overline{x_2}\cdot\overline{y} \\ &= -(\overline{x_1\cdot x_2})\cdot\overline{y} \end{aligned} \quad (4)$$

while the partial clique energy of NOR is

$$\begin{aligned} U_{P-\mathrm{NOR}}(x_1, x_2, y) &= -\overline{x_1}\cdot x_2\cdot\overline{y} - x_1\cdot\overline{x_2}\cdot\overline{y} \;\; - x_1\cdot x_2\cdot\overline{y} \\ &= -(x_1 + x_2)\cdot\overline{y}. \end{aligned} \quad (5)$$

We can use one of the $U_{P-\mathrm{AND}}$ terms $\overline{x_1}\cdot\overline{x_2}\cdot\overline{y_{\mathrm{AND}}}$ to represent the lost clique energy of NOR

$$U_{\mathrm{NOR}} = U_{P-\mathrm{NOR}} - \overline{x_1}\cdot\overline{x_2}\cdot\overline{y_{\mathrm{AND}}} \quad (6)$$

TABLE II
Truth Table of an AND–NOR Pair

Input			Valid output			
x_1x_2			AND y_{AND}		NOR y_{NOR}	
0	0	0	$U_{\mathrm{p-}AND}$	$\overline{x_1}\cdot\overline{x_2}\cdot\overline{y_{AND}}$	U_1	1
0	1	0		$\overline{x_1}\cdot x_2\cdot\overline{y_{AND}}$	$\overline{x_1}\cdot x_2\cdot\overline{y_{NOR}}$	0
1	0	0		$x_1\cdot\overline{x_2}\cdot\overline{y_{AND}}$	$x_1\cdot\overline{x_2}\cdot\overline{y_{NOR}}$	0
1	1	1	U_1	$x_1\cdot x_2\cdot\overline{y_{NOR}}$		0

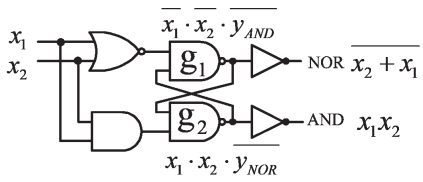

Fig. 5. Compensation clique energy-based structure for an AND–NOR pair.

and one of the $U_{P-\mathrm{NOR}}$ terms $x_1\cdot x_2\cdot\overline{y_{\mathrm{NOR}}}$ to represent the lost clique energy of AND

$$U_{\mathrm{AND}} = U_{P-\mathrm{AND}} - x_1\cdot x_2\cdot\overline{y_{\mathrm{NOR}}}. \quad (7)$$

The clique energy to represent the lost energy terms of an AND–NOR pair is

$$U_{C-\mathrm{AND-NOR}} = -x_1\cdot x_2\cdot\overline{y_{\mathrm{NOR}}} - \overline{x_1}\cdot\overline{x_2}\cdot\overline{y_{\mathrm{AND}}}. \quad (8)$$

Equation (8) is just an addition of the lost clique energy of NOR in (6) and the lost clique energy of AND in (7). In (8), the term $\overline{x_1}\cdot\overline{x_2}\cdot\overline{y_{\mathrm{AND}}}$ of AND can also be regarded as a compensation for the lost clique energy of NOR, while the term $x_1\cdot x_2\cdot\overline{y_{\mathrm{NOR}}}$ of NOR can be regarded as a compensation for the lost clique energy of AND. Therefore, we simplify the joint clique energy of an AND–NOR pair based on (6)–(8), as shown in Table II

$$\begin{aligned} U_{\mathrm{AND-NOR}} &= -(x_1\cdot x_2\cdot\overline{y_{\mathrm{NOR}}} + \overline{x_1}\cdot\overline{x_2}\cdot\overline{y_{\mathrm{AND}}}) \\ &\quad -(\overline{x_1}\cdot x_2\cdot\overline{y_{\mathrm{NOR}}} + x_1\cdot\overline{x_2}\cdot\overline{y_{\mathrm{NOR}}}) \\ &\quad -(\overline{x_1}\cdot x_2\cdot\overline{y_{\mathrm{AND}}} + x_1\cdot\overline{x_2}\cdot\overline{y_{\mathrm{AND}}}) \\ &= U_{C-\mathrm{AND-NOR}} - (x_1\oplus x_2)\cdot\overline{y_{\mathrm{NOR}}} \\ &\quad -(x_1\oplus x_2)\cdot\overline{y_{\mathrm{AND}}} \end{aligned} \quad (9)$$

Based on (8), a clique energy-based structure used to compensate the lost terms in AND and NOR is shown in Fig. 5. We add the following coding unit in Fig. 6 to the compensation clique energy-based structure, which confers advantages based on the following analysis. From the energy viewpoint, the coding unit achieves the full NOR–AND joint clique energy in (9). Gates g1 and g2, which form the feedback structure, can implement the compensation function $U_{C-\mathrm{AND-NOR}}$. Gates g4 and g5 shown in Fig. 6 are proposed for the corresponding clique energy

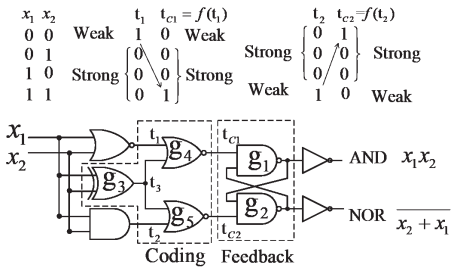

Fig. 6. Coding-based structure for a complementary AND–NOR pair with two logic operations.

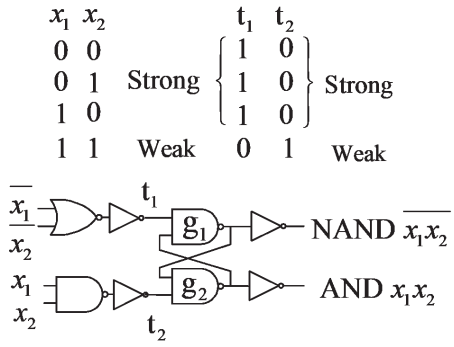

Fig. 7. MS [28] structure with only one kind of logic.

$(x_1 \oplus x_2)\cdot\overline{y_{\mathrm{NOR}}}$ and $(x_1 \oplus x_2)\cdot\overline{y_{\mathrm{AND}}}$, respectively. From the probability viewpoint, the coding unit can strengthen the input bits. The structure in Fig. 7 is the traditional MS-MRF structure, which has an MS structure (NAND–NAND feedback), while the design only considers the energy relation while neglecting the probability match between the master and the feedback loop. Therefore, there is a performance loss according to the study [33].

As we mention in the introduction, a gate, such as a NAND gate, has an asymmetric output property, characterized by different output correct probabilities for being digital "1" and "0" when the input follows the Bernoulli distribution. Assume "strong" represents high correct probability and "weak" represents low correct probability. For example, the inputs of a NANDgate are x_1, x_2; the output is y; under the presence of noise, the probability of an input being weak is $p_w (0 \le p_w \le 0.5)$, while the probability of the input being strong is $1 - p_w$. Assume that the symbol $p(y|x_1x_2)$ represents the conditional probability of output y being strong

$$\begin{aligned} p(1|00) &= 1 - p_w^2 \\ p(1|01) &= 1 + p_w^2 - p_w \\ p(1|10) &= 1 + p_w^2 - p_w \\ p(0|11) &= (1 - p_w)^2 \\ p(1|00) &\ge p(1|01) = p(1|10) \ge p(0|11). \end{aligned} \tag{10}$$

Therefore, for such input pairs, the NAND has higher noise tolerance for being {00, 01, 10} rather than {11}. In terms of the output bits, the NAND has a higher noise tolerance when being "1" than "0." For an MS structure, the master unit and the slave unit are both composed of asymmetric

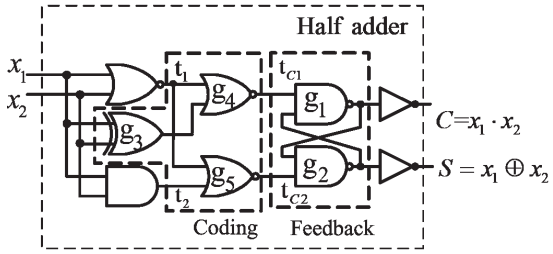

Fig. 8. Coding-based structure for a complementary AND–XOR pair.

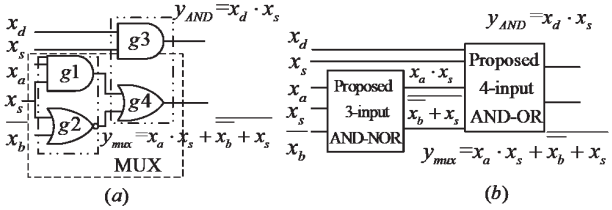

Fig. 9. (a) Mixed mapping MUX. (b) CPMRF pair-based MUX structure.

elements. Therefore, the probability match can influence the performance of the two-level structure. Both t_1 and t_2 shown in Fig. 7 are operated by NOR and NAND gates, which then have strong bits and weak bits. If the strong bits out of the first level are connected to the higher noise-tolerant input pair of NAND–NAND feedback structure, the effect of noise will be weakened again. However, if the weak bit (such as the bit "1" of t_2) is connected to the weak input pair of next level such as {11} for g_2, the effect of noise will be amplified. Therefore, the MS structure experiences significant performance losses when the output of g_2 is "0" since this bit overlaps two cascade weaknesses. We also propose a coding-based structure for a complementary asymmetric and symmetric AND–XOR pair in Fig. 8, which can achieve the functions of the carry bit and the sum bit of a half adder. The coding structure shown in Fig. 8 helps the weak bit "1" of t_1 and t_2 transfer to strong bit "0" of t_{c1} and t_{c2} and prevent the two-cascade weakness from overlapping. Therefore, the proposed structure has higher noise tolerance than the conventional MRF structures. Based on the above examples for AND–XOR and AND–NOR, a large number of complementary modules are possible: NAND–OR, AND–XOR (XNOR), OR–XOR (XNOR), NAND–XOR (XNOR), NOR–XOR (XNOR); NAND–AND, NOR–OR, and XOR–XNOR, are self-complementary pairs designed by logic transformation. In the same complementary module, two logic operations can share a common MRF network.

The above complementary pairs can also construct a MUX-AND block for multiple logic operations used in fast tree-based carry-lookahead adders for selecting the carry bit. This case study extends the two inputs to three-input AND–NOR pairs for MUX function based on the following transformation:

$$y_{mux} = x_a \cdot x_s + x_b \cdot \overline{x_s} = x_a \cdot x_s + \overline{\overline{x_b} + x_s}. \tag{11}$$

Both g_1 and g_2 shown in Fig. 9(a) can achieve $x_a \cdot x_s$ and $\overline{\overline{x_b} + x_s}$ in (11) by the proposed coding-based AND–NOR

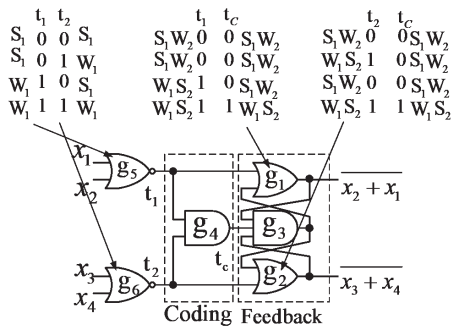

Fig. 10. Non-complementary CPMRF pair: NOR–NOR, where S_1W_2 refers to strong for the first level and weak for the second level achieving the two cascades complementary instead of weaknesses overlap.

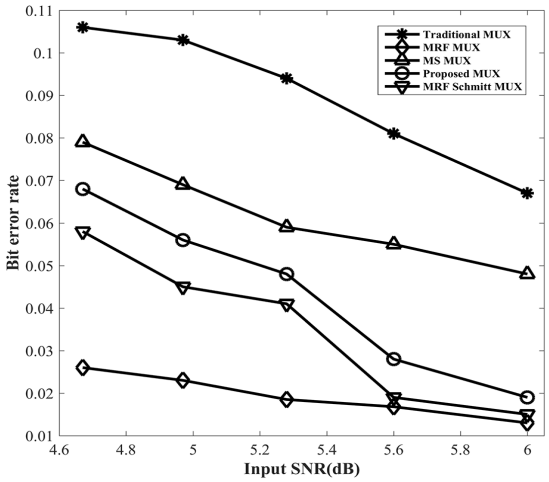

Fig. 11. BER results for a MUX.

structure shown in Fig. 9(b). g_4 shown in Fig. 9(a) is utilized for the MUX function by $x_a \cdot x_s + \overline{\overline{x_b} + x_s}$. We group g_3 and g_4 together to form a four-input AND–OR module shown in Fig. 9(b). The logic operations, AND and OR, share a common MRF network to achieve area efficiency.

We further extend complementary pairs to non-complementary pairs for more general designs. A non-complementary NOR–NOR pair is shown in Fig. 10. The intermediate signals t_1 and t_2 are the outputs of gates g_5 and g_6, which have the high correct probability of bit "0" referred to strong bit "0" for the first level (S_1) and the low correct probability of bit '1' represented by symbol W_1. We use gate g_4 for coding and then for the second level feedback OR–OR structure: g_1 and g_2, outputting strong bit "1," can compensate the loss of the first level, achieving two complementary cascades instead of overlapping weaknesses.

The effectiveness of the proposed area-efficient method is illustrated by the transistor counts for the above structures in Figs. 6, 8–10, and 12. In Table III, the conventional MRF design [24] for each structure requires the largest number of transistors. The proposed method saves at least 61.7% transistors compared with the conventional MRF [24], while it saves at least 17.9% transistors compared with MS [28].

TABLE III
TRANSISTOR COUNT COMPARISON FOR DIFFERENT STRUCTURES

	MRF [24]	MS [28]	MRF-Schmitt [34]	proposed
	Reduction*			
AND-NOR	61.7%	17.9%	28%	46
AND-XOR	61.7%	43.9%	46.5%	46
MUX-AND	68.6%	33.3%	19.1%	76
NOR-NOR	71.7%	39.3%	46.9%	34
Two 4-bit even parity generators	51.6%	46.2%	36.9%	174
Two binary comparators	67.9%	33.0%	45.4%	118
A 3-line to 8-line decoder	68.4%	40.8%	46.6%	174
An 8-bit CLA	64.4%	37.7%	35.1%	1374

*Reduction = (other structure-proposed)/other structure

Compared with the MRF-Schmitt design [34], it saves at least 19.1% of transistors. The area saving in the proposed method benefits from the shared MRF network in a gate pair for multiple logic operations. The noise-tolerant performance of the proposed method for a MUX, shown in Fig. 11, was investigated in an HSPICE simulation, where the performance was evaluated by measuring the bit error rate (BER) under varying input signal-to-noise ratios (SNRs). The simulation was operated at 0.25-V supply voltage using a 130-nm BSIM4 model. Additive white Gaussian noise (AWGN) was generated in MATLAB and was combined with noise-free signals for all inputs. Fig. 11 shows the BER results of a traditional non-MRF MUX, a conventional MRF [24] MUX, an MS [28] MUX, an MRF-Schmitt [34] MUX, and a proposed MUX. Compared with an MS MUX, the proposed MUX has at least 14% lower BER. The improvement can be explained by the general mapping process from a circuit to the corresponding CPMRF network. Generally, mapping a circuit onto the CPMRF network involves two major steps.

1) Designing a shared PMRF network for a pair of two logic gates based on the partial clique energy functions.
2) Designing a coding structure to complement the rest clique energy and transform weak bits to strong bits avoiding weak bit cascade.

These two steps guarantee that the implementation of the clique energy for the internal valid states is the same as that in the MS design. In addition, the coding structure in the proposed method utilizes the combination of the inner noise tolerance of asymmetric logic gates such as the robust output "1" in a NAND gate and the robust output "0" in a NOR gate in order to transform weak bits into strong bits. In this way, the noise-tolerance capability is ensured through redundancy in the CPMRF method by the MRF theory and the inner noise tolerance of logic gates. This explains why the proposed CPMRF method has better BER results than the MS method. Since a logic gate pair shares a common MRF network in the CPMRF method, it can save more area than the MS method. In Fig. 11, it is shown that the conventional MRF [24] design has the best noise tolerance under various SNRs, while the MRF-Schmitt [34] design has the second-best

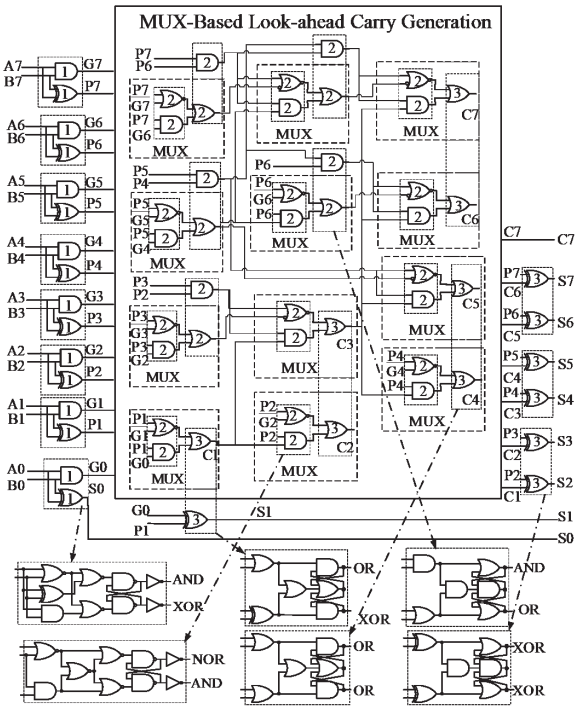

Fig. 12. Proposed CPMRF carry-lookahead adder.

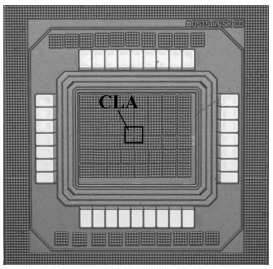

Fig. 13. Die photograph of the proposed CLA.

noise tolerance. This is because the conventional MRF method maps completely all possible valid sates without any loss of the clique energy, while the MRF-Schmitt [34] method combines the high noise tolerance of the MRF and Schmitt trigger circuits. However, the conventional MRF design is very complex to implement and consumes large area overhead. The MRF-Schmitt design consumes more hardware than the proposed design as well. Considering hardware cost, the proposed method achieves a better tradeoff between area cost and noise tolerance.

IV. Chip Implementation

We designed an 8-bit carry-lookahead adder chip to integrate the proposed CPMRF pairs. Each CPMRF pair is marked in a gray rectangle, as shown in Fig. 12. The proposed CLA chip employs the IBM 130-nm CMRF8SF process. The die photograph is shown in Fig. 13. In Table IV, we summarize the performance of the proposed chip in terms of its area, power consumption, and BER. To assess the noise-tolerance capability of the proposed chip, we built a testing platform

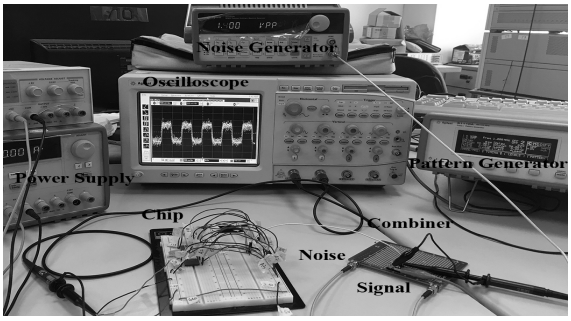

Fig. 14. Testing platform.

TABLE IV
Performance of the Proposed CLA

Process	IBM130nm
Area	84.8um×67.6 um
Power Consumption	125nW/MHz@0.25V 540nW/MHz@0.9V 700nW/MHz@1.0V 880nW/MHz@1.1V 1080nW/MHz@1.2V
BER	4.11e-04@4.68dB 7.24e-05@6.02dB 4.77e-07@8.05dB

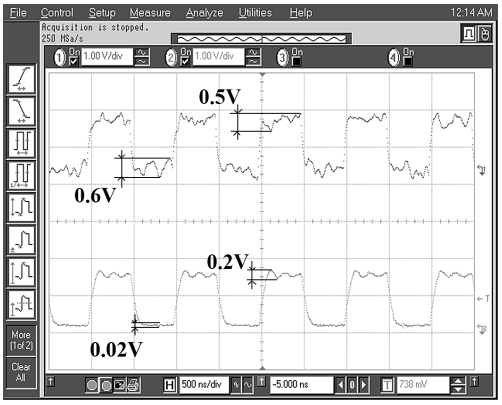

Fig. 15. Measured waveforms of input (upper) and output (lower) of the proposed chip under 6.02-dB SNR.

shown in Fig. 14. We used an Agilent 33120A 15-MHz Function/Arbitrary Waveform Generator to generate random noise and an Agilent 81110A Pattern Generator to provide the input noise-free signal and combine them together by a combiner to mimic the noisy environment as the input injected to the proposed CLA circuit.

As shown in Fig.15, the input and output waveforms were measured under the interference of noise with 6.02-dB SNR at a core voltage of 0.25 V. The largest peak variance of both the high levels and low levels of input and output signals is marked in Fig. 15. It is found that the quality of the output signal is much better than the noisy input signal, especially for the low logic levels. The above conclusion is also supported

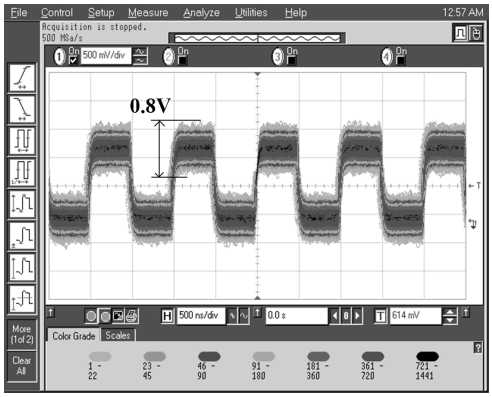

Fig. 16. Eye pattern of the input signal of the proposed CLA chip under 6.02-dB SNR.

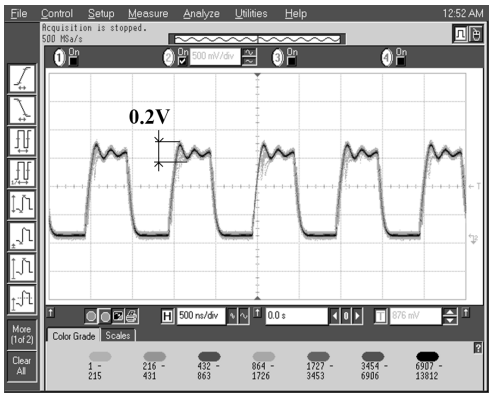

Fig. 17. Eye pattern of the output signal of the proposed CLA chip under 6.02 dB.

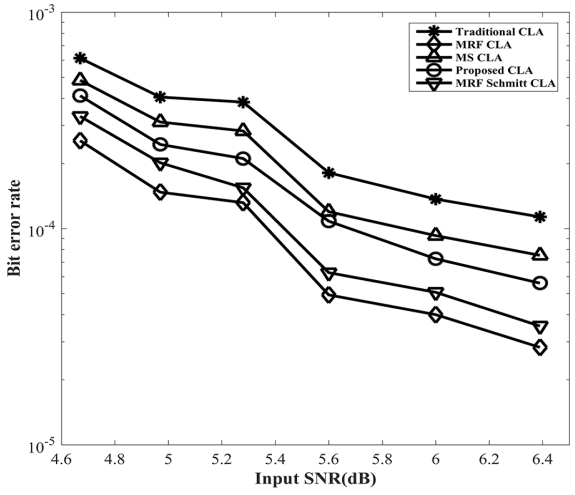

Fig. 18. BER comparison under different SNRs.

by the observed waveforms of the input and output signals, which is shown in Figs. 16 and 17. Furthermore, we measured the BER of the proposed CLA under different levels of noise power evaluated by SNR. Fig. 18 is the comparison of BER measurements for a conventional CLA (constructed by normal logic gates), a full MRF CLA [29], an MS CLA [28], an MRF-Schmitt CLA [34], and the proposed CPMRF CLA. Since other designs have been implemented in silicon and measured in [28], [29], and [34], all comparisons are based on the previous results, including the analysis, the measurement, and the performance of the chips qualitatively. Results are consistent with the theoretical analysis in [28], [29], and [34]. The results in Fig. 18 indicate good noise resilience of the proposed CLA chip under the interference of high noise power. Compared with an MS CLA [28], the proposed CLA is characterized by a 20% reduction in BER with 37.7% area saving. Although a full MRF CLA [29] has the lowest BER (28% lower than the proposed CLA), it consumes 64.4% more transistor area. The MRF-Schmitt CLA [34] has 29% lower BER than the proposed CLA, but it cost 35.1% more transistor area. The observation that the BER of the MRF-Schmitt CLA is close to that of the conventional MRF is consistent with what is presented in [34]. Although the proposed adder requires about three times the transistor number used in a non-MRF traditional design, it achieves about 51% the reduction of BER. For power savings, the proposed CLA only consumes 125 nW/MHz, which saves 93% of the power consumption of an MS CLA [28] at a supply voltage of 0.25 V. As indicated in [34], the MRF-Schmitt CLA consumes more power than the MS CLA. Although it has a better BER than the proposed method, it uses much more power and requires more transistors. Therefore, the proposed MRF circuit is a promising design, which can satisfy a great balance between the demanding requirements of noise immunity, power consumption, and hardware cost.

V. Conclusion

In this paper, we propose a low-power CPMRF method for multi-logic operations in order to achieve a better tradeoff between chip area and noise immunity at low power supply voltage. First, we put forward an idea of partial clique energy corresponding to the full clique energy used in the conventional MRF design [24]. The partial clique energy is intended to combine multiple logic operations within a shared MRF network. Second, a coding unit is built based on the benefit of asymmetric gates. We also propose general coding units for complementary pairs and non-complementary pairs. Using this CPMRF method, we fabricated an 8-bit CLA chip using IBM 130-nm technology. In the chip validation, the proposed CPMRF CLA achieves significant area saving and power saving compared with the traditional MRF design [29] and exhibits relatively high noise immunity. In comparison with the MS design [28], the proposed CLA outperforms MS CLA with 20% BER improvement, 37.7% area saving, and 93% power saving at a supply voltage of 0.25 V. Considering the automation of the whole process, the CPMRF pairs proposed in this paper can be generalized into corresponding standard cells in cell-based designs by hardware description languages in the existing EDA flows. Macro blocks formed by a large set of logic operations (standard cells) can also be transformed into the corresponding CPMRF designs by the same approaches listed in this paper. Additionally, by following the mapping rules, designers can easily construct their own CPMRF mapping cells to replace the old versions. The information can be included along with other parameters, such

as size and delay in a database. In terms of the functional verification of the proposed design, it can easily be achieved by simply comparing the outputs of the traditional non-MRF auto-transformation design with the outputs of the CPMRF auto-transformation design. The comparisons can be performed by XOR gates. When the outputs of these XOR gates are all "0," it represents that the proposed CPMRF design has passed the functional verification. Therefore, the proposed CPMRF method can effectively overcome the bottlenecks of previous MRF designs and is undoubtedly beneficial to low-power nanoscale VLSI chip design.

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REFERENCES

[1] T. Rejimon, K. Lingasubramanian, and S. Bhanja, "Probabilistic error modeling for nano-domain logic circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 17, no. 1, pp. 55–65, Jan. 2009.

[2] M. A. Elgamel and M. A. Bayoumi, "Interconnect noise analysis and optimization in deep submicron technology," *IEEE Circuits Syst. Mag.*, vol. 3, no. 4, pp. 6–17, 2003.

[3] M. V. Heijningen, M. Badaroglu, S. Donnay, G. G. E. Gielen, and H. J. D. Man, "Substrate noise generation in complex digital systems: Efficient modeling and simulation methodology and experimental verification," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 1065–1072, Aug. 2002.

[4] A. V. Mezhiba and E. G. Friedman, "Scaling trends of on-chip power distribution noise," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 12, no. 4, pp. 386–394, Apr. 2004.

[5] O. Milter and A. Kolodny, "Crosstalk noise reduction in synthesized digital logic circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 11, no. 6, pp. 1153–1158, Dec. 2003.

[6] S. Van den Berghe, F. Olyslager, D. de Zutter, J. de Moerloose, and W. Temmerman, "Study of the ground bounce caused by power plane resonances," *IEEE Trans. Electromagn. Compat.*, vol. 40, no. 2, pp. 111–119, May 1998.

[7] T.-H. Chang, "Minimizing switching noise in a power distribution network using external coupled resistive termination," *IEEE Trans. Adv. Packag.*, vol. 28, no. 4, pp. 754–760, Nov. 2005.

[8] R. P. Jindal, "Compact noise models for MOSFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2051–2061, Sep. 2006.

[9] W. Jun, "Consideration of noise for efficient energy design of deep submicron VLSI chips," in *Proc. Asia–Pacific Microw. Conf.*, Dec. 2005, p. 4.

[10] J. Von Neumann, "Probabilistic logics and the synthesis of reliable organisms from unreliable components," in *Automata Studies*, C. E. Shannon and J. McCarthy, Eds. Princeton, NJ, USA: Princeton Univ. Press, 1956, pp. 43–98.

[11] J. Han, J. Gao, P. Jonker, Y. Qi, and J. A. B. Fortes, "Toward hardware-redundant, fault-tolerant logic for nanoelectronics," *IEEE Design Test Comput.*, vol. 22, no. 4, pp. 328–339, Jul. 2005.

[12] B. D. Brown and H. C. Card, "Stochastic neural computation. I. Computational elements," *IEEE Trans. Comput.*, vol. 50, no. 9, pp. 891–905, Sep. 2001.

[13] W. Qian, M. D. Riedel, H. Zhou, and J. Bruck, "Transforming probabilities with combinational logic," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 30, no. 9, pp. 1279–1292, Sep. 2011.

[14] G. Sarkis and W. J. Gross, "Efficient stochastic decoding of non-binary LDPC codes with degree-two variable nodes," *IEEE Commun. Lett.*, vol. 16, no. 3, pp. 389–391, Mar. 2011.

[15] A. Naderi, S. Mannor, M. Sawan, and W. J. Gross, "Delayed stochastic decoding of LDPC codes," *IEEE Trans. Signal Process.*, vol. 59, no. 11, pp. 5617–5626, Nov. 2011.

[16] Q. T. Dong, M. Arzel, C. Jego, and W. J. Gross, "Stochastic decoding of turbo codes," *IEEE Trans. Signal Process.*, vol. 58, no. 12, pp. 6421–6425, Dec. 2010.

[17] J. Chen, J. Hu, and G. E. Sobelman, "Stochastic iterative MIMO detection system: Algorithm and hardware design," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 4, pp. 1205–1214, Apr. 2015.

[18] Y. Liu and K. K. Parhi, "Lattice FIR digital filter architectures using stochastic computing," in *Proc. IEEE Int. Conf. Acoust., Speech Signal Process. (ICASSP)*, Apr. 2015, pp. 1027–1031.

[19] I.-C. Wey, C.-C. Peng, and F.-Y. Liao, "Reliable low-power multiplier design using fixed-width replica redundancy block," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 1, pp. 78–87, Jan. 2015.

[20] B. Shim, S. R. Sridhara, and N. R. Shanbhag, "Reliable low-power digital signal processing via reduced precision redundancy," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 12, no. 5, pp. 497–510, May 2004.

[21] B. Shim and N. R. Shanbhag, "Energy-efficient soft error-tolerant digital signal processing," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 4, pp. 336–348, Apr. 2006.

[22] P. Korkmaz, B. E. S. Akgul, and K. V. Palem, "Energy, performance, and probability tradeoffs for energy-efficient probabilistic CMOS circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 8, pp. 2249–2262, Sep. 2008.

[23] I. R. Bahar, J. Chen, and J. Mundy, "A probabilistic-based design for nanoscale computation," in *Nano, Quantum, and Molecular Computing: Implications to High Level Design and Validation*, S. K. Shukla and R. I. Bahar, Eds. Norwell, MA, USA: Kluwer, 2004, ch. 5, pp. 133–156.

[24] K. Nepal, R. I. Bahar, J. Mundy, W. R. Patterson, and A. Zaslavsky, "Designing logic circuits for probabilistic computation in the presence of noise," in *Proc. 42nd IEEE Des. Autom. Conf.*, Jun. 2005, pp. 485–490.

[25] J. Chen, J. Mundy, Y. Bai, S.-M. C. Chan, P. Petrica, and R. I. Bahar, "A probabilistic approach to nano-computing," in *Proc. IEEE Non-Silicon Comput. Workshop*, Jun. 2003, pp. 1–8.

[26] I.-C. Wey, Y.-J. Lan, and C.-C. Peng, "Reliable ultra-low-voltage low-power probabilistic-based noise-tolerant latch design," *Microelectron. Rel.*, vol. 53, no. 12, pp. 2057–2069, 2013.

[27] S. Z. Li, "Mathematical MRF models," in *Markov Random Field Modeling in Image Analysis*. New York, NY, USA: Springer, 2009, pp. 1–28.

[28] I.-C. Wey, Y.-G. Chen, C.-H. Yu, A.-Y. Wu, and J. Chen, "Design and implementation of cost-effective probabilistic-based noise-tolerant VLSI circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 11, pp. 2411–2424, Nov. 2009.

[29] I.-C. Wey, Y.-G. Chen, C. Yu, J. Chen, and A.-Y. Wu, "A 0.18μm probabilistic-based noise-tolerate circuit design and implementation with 28.7db noise-immunity improvement," in *Proc. IEEE Solid-State Circuits Conf.*, Nov. 2006, pp. 291–294.

[30] Y. Li, X. Li, J. Hu, and S. Yang, "Area-sharing cyclic structure MRF cirucits design in ultra-low supply voltage," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2015, pp. 2353–2356.

[31] K. Nepal, R. I. Bahar, J. Mundy, W. R. Patterson, and A. Zaslavsky, "Optimizing noise-immune nanoscale circuits using principles of Markov random fields," in *Proc. 16th ACM Great Lakes Symp. VLSI*, 2006, pp. 149–152.

[32] K. Liu, T. An, H. Cai, L. Naviner, J.-F. Naviner, and H. Petit, "A general cost-effective design structure for probabilistic-based noise-tolerant logic functions in nanometer CMOS technology," in *Proc. IEEE EUROCON*, Jul. 2013, pp. 1829–1836.

[33] A. R. Kermany, N. H. Hamid, and Z. A. Burhanudin, "A study of MRF-based circuit implementation," in *Proc. Int. Conf. Electron. Des.*, Penang, Malaysia, Dec. 2008, pp. 1–4.

[34] I.-C. Wey and Y.-J. Shen, "Hardware-efficient common-feedback Markov-random-field probabilistic-based noise-tolerant VLSI circuits," *Integration, VLSI J.* vol. 47, no. 4, pp. 431–442, 2014.

[35] Y. Li, J. Hu, H. Lu, and J. Chen, "Area-efficient partial-clique-energy MRF pair design with ultra-low supply voltage," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Montreal, QC, Canada, May 2016, pp. 261–264, doi: 10.1109/ISCAS.2016.7527220.

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