A 290-mV, 3.34-MHz, 6T SRAM With pMOS Access Transistors and Boosted Wordline in 65-nm CMOS Technology

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***Abstract*— This paper presents a six-transistor bitcell SRAM with pMOS access transistor. Utilizing pMOS access transistor results in lower zero-level degradation (ZLD) and, hence, higher read stability. In addition, the access transistor connected to the internal node holding V_{DD} acts as a stabilizer and counter balances the effect of ZLD. In order to improve the writability, wordline (WL) boosting is exploited. WL boosting also helps to compensate the lower speed of the pMOS access transistor compared with nMOS transistor. To verify our design, a 2-kb SRAM is fabricated in the TSMC 65-nm CMOS technology. Measurement results show that the maximum operational frequency of the test chip is at 3.34 MHz at 290 mV. The minimum energy consumption is measured as 1.1 fJ/bit at 400 mV.**

***Index Terms*— CMOS 65-nm technology, low energy, low voltage, negative wordline (WL) boosting, six-transistor (6T) SRAM, speed improvement, subthreshold circuits, very large scale integrated, volatile memories, yield.**

I. Introduction

ULTRALOW-POWER applications, such as sensor networks, pacemakers, and many portable devices, require extreme energy constraints for longer battery life. It is shown that very low energy operation is achieved when power supply is in the near or subthreshold region [1]. By reducing the supply voltage of a system on chip (SOC), the dynamic energy is reduced quadratically at the expense of increased delay. As clock cycle time is reduced to accommodate increased delay, leakage power and energy contributions become significant [2]. One of the approaches to reduce this component is to shut down the macro after completing the task [2]. Unfortunately, SRAM power cannot be switched OFF without losing its data. Even reducing its power supply voltage requires a careful consideration owing to its data stability, and read margin and write margin (WM). Therefore, SRAM blocks are the main bottleneck to reduce the operating supply voltage of SOCs [3]. Another challenge of SRAM blocks is their low speed in the subthrehsold region due to the reduced supply voltage and stability issue. In addition to the stability challenge of SRAMs, the low speed of subthreshold circuits and specifically SRAM arrays limit the complexity of the tasks that these circuits can perform. It is also required to develop subthreshold circuits operating at higher speeds that can perform more complex tasks [4].

Conventional six-transistor (6T) SRAM bitcell has contradicting requirements for read stability and writability. For example, decreasing the access transistor width improves the read stability, while it decreases the WM. This conflict becomes even more emphasized in the subthreshold region. The design in [5] utilizes a two-step wordline (WL) boosting to overcome this conflict. The designs proposed in [6] and [7] have improved both read margin and WM at the expense of increased bitcell area, reduced speed, removing half-selected cells, and not being able to utilize differential sensing. The main drawback of single-ended sensing versus differential sensing is its slow sensing speed and not being immune to common-mode noise. In addition, not incorporating half-selected cells requires higher area and more complexity for the extra needed sense amplifiers and peripheral circuitry [8]. Moreover, because of not having bit-interleaving, single-error correction and double-error detection schemes may not be adequate in mitigating soft errors [9].

A 6T bitcell operating in the subthreshold region is reported in [6]. This asymmetrical and single-ended 6T bitcell uses one pass gate instead of two nMOS access transistors, and to overcome the small sensing window and vulnerability to process variation, they significantly increase the sizes of each transistor in each bitcell. One main weakness of this design is its relatively low speed operation. Several 65-nm designs have proposed bitcells with extra number of transistors. For example, in [7], a single-ended 8T bitcell is fabricated that is capable to operate as low as 350 mV. This design suffers from low-speed single-ended sensing and is not able to assimilate half-selected cells. The proposed bitcell in [10] utilizes nine transistors to enable differential sensing. They also show that utilizing pMOS access transistors makes their bitcell less susceptible to the process variation effect. This design operates at the speed of 200 kHz at 350 mV. Do *et al.* [11] utilized a system-level approach to reduce the SRAM supply voltage for image and video specific applications. In order to avoid the worst case read scenario, the stored data in columns are randomized to make the distribution of the 0 and 1 s close to 50%. They show that the 8T bitcell in [7] can operate at 200 mV when utilizing data randomization. Researchers have designed SRAM cell with pMOS access transistors in an emitter-coupled logic-CMOS process [12]. With pMOS

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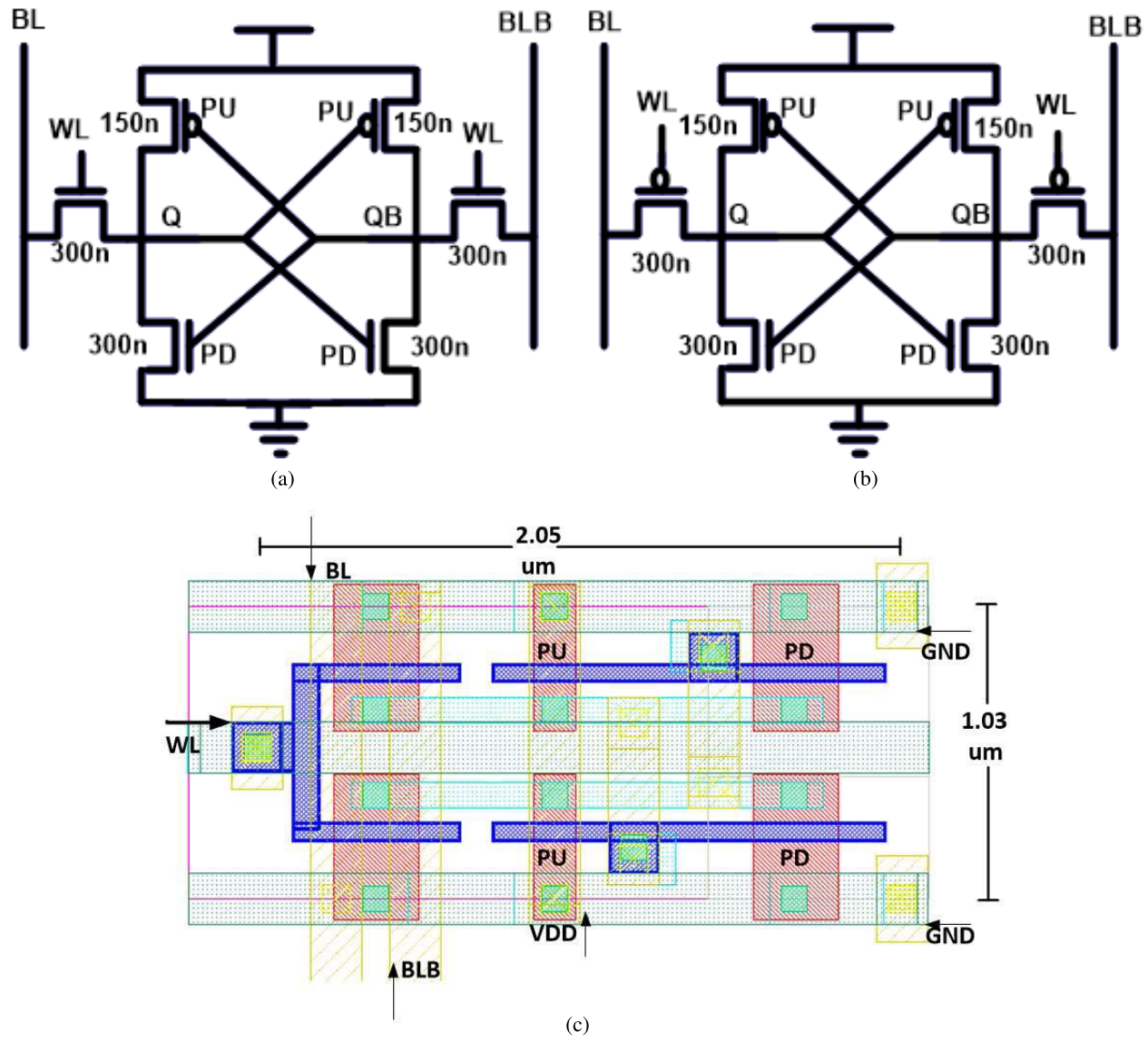


Fig. 1. (a) 6T-NA. (b) 6T-PA. (c) Layout of 6T-PA.

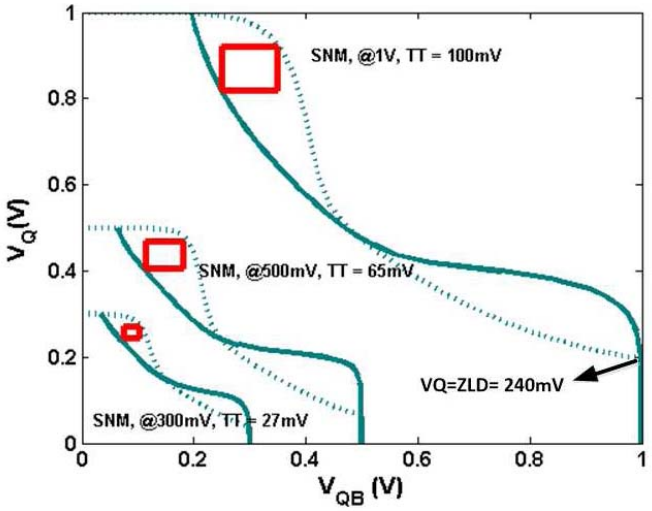
access transistor, the authors claimed that they could reduce the power supply voltage by additional 0.5 V compared with nMOS access transistor.

In this paper, we propose a 6T bitcell optimized for low-voltage applications. In order to improve the read stability of the bitcell during read operation, we utilize pMOS access transistors, as they can provide better read stability compared with the nMOS transistors. In addition, the access transistor connected to node that holds V_{DD} in the proposed bitcell, unlike the conventional 6T bitcell, is fully on and mitigates the zero-level degradation (ZLD). Moreover, to overcome the weak writability of the new bitcell, WL boosting is exploited. Even though the WL boosting emphasizes on the ZLD, however, unlike the conventional 6T bitcell, the access transistor connected to the internal node with high voltage also increases its robustness against ZLD. Moreover, WL boosting also enhances the speed of operation. In addition, differential sensing is exploited in our design.

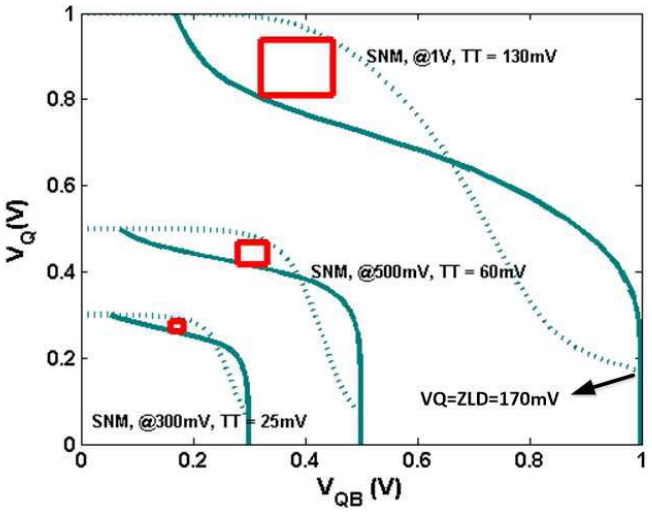
The rest of this paper is organized as follows. In Section II, we investigate the read stability of the 6T bitcell with pMOS access transistor through simulations and analytical analysis. In Section III, we describe the improvement of the writability utilizing WL boosting. The boosted circuit implementation is discussed in Section IV. In Section V, the read and leakage current of the new bitcell are compared with that of the conventional 6T bitcell. Measurement results and comparison with the previous published results are provided in Section VI. Finally, in Section VII, conclusions are drawn.

II. Read Stability of 6T SRAM Bitcell With pMOS Access Transistors

The 6T bitcell with nMOS access transistor (6T-NA) and 6T bitcell with pMOS access transistor (6T-PA) are shown in Fig. 1(a) and (b). The layout of the 6T-PA is also shown in Fig. 1(c). The read butterfly curves of the 6T-NA and 6T-PA during read operation are shown in Fig.2. Fig. 2 shows that



(a)



(b)

Fig. 2. Read butterfly curves at TT corner for (a) 6T-NA and (b) 6T-PA ($T = 25$ °C).

the 6T-PA has higher static noise margin (SNM) compared with the 6T-NA at 1 V and the SNM is almost the same at 500 and 300 mV. To compare the read stability of both bitcells, we perform 1k Monte Carlo read simulations of both bitcells at the same condition. Fig. 3 shows the behavior of node QB of both bitcells. As shown in Fig. 3, for the 6T-NA, data flip occurs 105 times (i.e., yield = 89.5%), while only one data flip occurs for the 6T-PA (i.e., yield = 99.9%). Assuming, without loss of generality, the node QB in both 6T bitcells is high; the BLB remains high, while BL starts discharging. In this process, node Q acquires non-zero potential known as ZLD. A larger ZLD can adversely affect the read stability of an SRAM bitcell. Since, a pMOS transistor has lower mobility, for the iso-area, the cell ratio (C_R) in the superthreshold region is increased by a factor of $(\mu_n/\mu_p)(=2.5)$ as follows [13]:

$$C_R = \frac{\mu_n W_n / L_n}{\mu_p W_a / L_a} \tag{1}$$

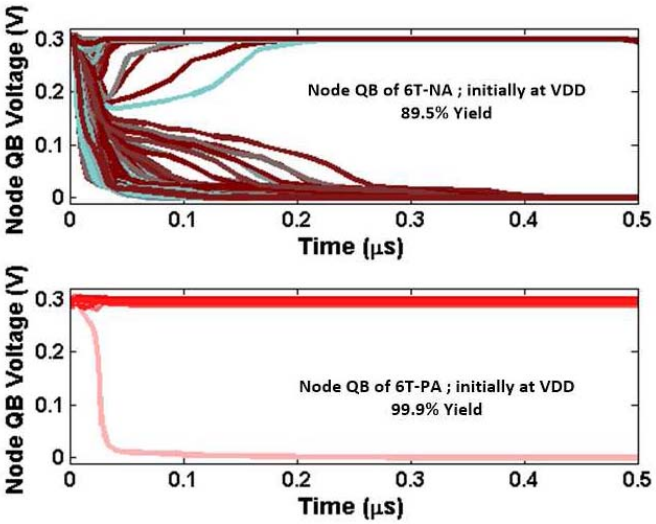


Fig. 3. 1k Monte Carlo read simulation for 6TPA and 6TNA bitcells at 300 mV. Data flip occurs when node QB makes a transition from V_{DD} to 0.

TABLE I
nMOS/pMOS TRANSISTOR PARAMETERS IN THE 65-nm CMOS TECHNOLOGY

Transistor Type	V_{t0}	λ	η
NMOS	400 mV	99 m	90 m
PMOS	370 mV	110 m	133.2 m

where $W_n(L_n)$ and $W_a(L_a)$ are the width (length) of the pull-down (PD) and access transistors, and μ_n and μ_p are the mobility of the nMOS and pMOS transistors, respectively.

The subthreshold current can be expressed by [14], [15]

$$I_{\text{sub}} = \mu C_{\text{ox}} \frac{W}{L}(n-1)v_T^2 e^{\frac{(V_{\text{GS}}-V_{\text{th}})}{nv_T}} \left(1 - e^{\frac{-V_{\text{DS}}}{v_T}}\right) \tag{2}$$

$$V_{\text{th}} = V_{t0} - \lambda V_{\text{BS}} - \eta V_{\text{DS}} \tag{3}$$

where μ is the charge carrier mobility, C_{ox} is the gate–oxide capacitance, v_T is the thermal voltage, V_{GS} is the MOSFET's gate–source voltage, and n is the subthreshold slope factor. V_{t0} represents the zero-biased threshold voltage of a MOSFET. Parameters λ and η represent the body effect coefficient and drain induced barrier lowering (DIBL) coefficient of a MOSFET, respectively. The parameters V_{t0}, λ, and η for the nMOS and pMOS transistors in the 65-nm CMOS technology are presented in Table I. The body effect and DIBL coefficient multiplied by V_{DS} and V_{BS}, respectively, can be assumed negligible compared with the zero-biased threshold voltage. Although n varies between 1.3 and 1.5, for convenience, it can be assumed to be equal for nMOS and pMOS transistors in the subthreshold region [16].

We define the driving strength ratio (D_R) in the subthreshold region as the driving strength ratio of the PD transistor to the access transistor. Considering V_{tp} and V_{tn} as the zero-biased threshold voltages of pMOS and nMOS transistors,

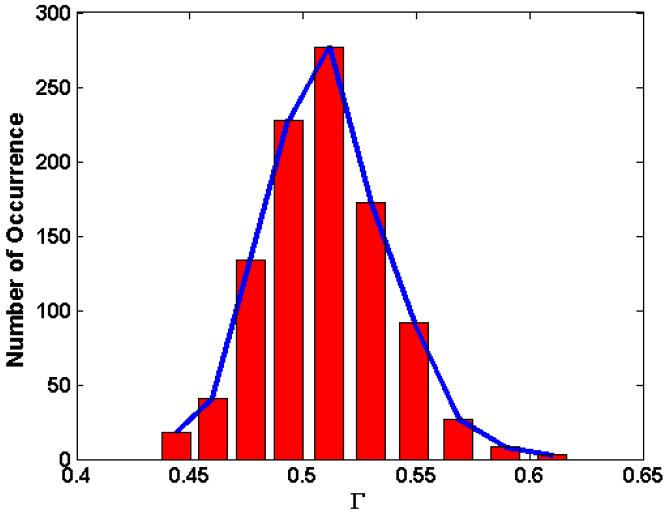


Fig. 4. Γ variation at 1k Monte Carlo simulations at 0.3 V.

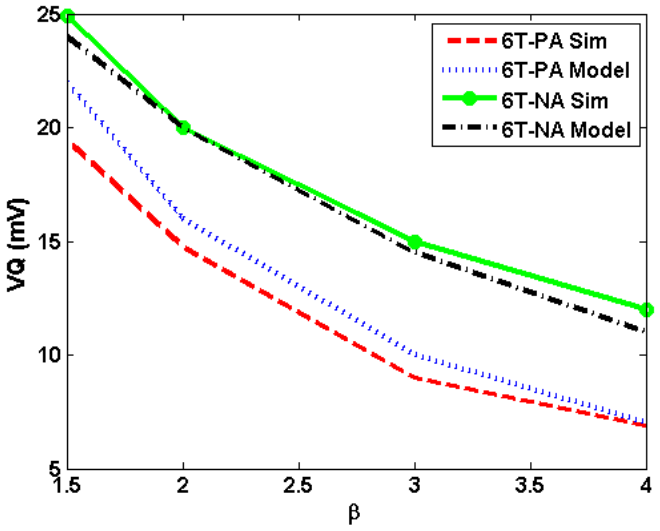


Fig. 5. Analytical and simulated ZLD versus β for both 6T-NA and 6T-PA at 290 mV, TT corner, 25 °C.

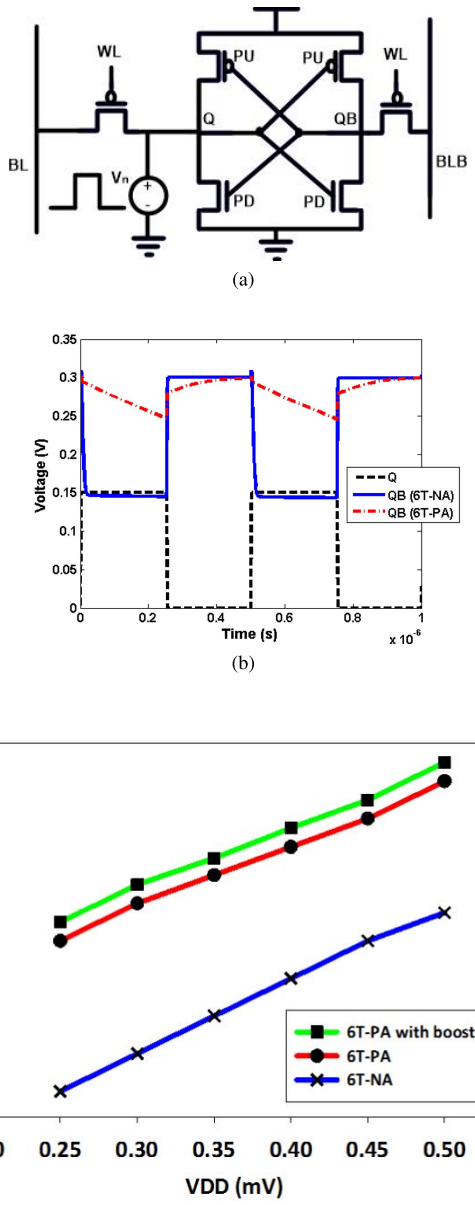


Fig. 6. (a) Schematic for simulating read stability of the 6T-PA cell with single-ended noise. (b) Transient simulation of node QB for 6T-NA at the FS corner and 6T-PA at the SF corner when the single-ended noise of 150 mV is applied on node Q at V_{DD} = 300 mV. (c) Maximum tolerable single-ended noise during read operation at the FS corner for 6T-NA and the SF corner for 6T-PA with and without boosting, T = 25 °C.

respectively, and assuming

$$\alpha_n = e^{\frac{-V_{tn}}{nv_T}}, \quad \alpha_p = e^{\frac{-|V_{tp}|}{nv_T}} \tag{4}$$

$$\Gamma = \frac{\alpha_n}{\alpha_p}, \quad \Lambda = \frac{\mu_n}{\mu_p}, \quad \beta = \frac{W_n/L_n}{W_p/L_p} \tag{5}$$

and D_R in the subthreshold region can be expressed as

$$D_R = \Gamma \cdot \Lambda \cdot \beta. \tag{6}$$

The difference of the D_R ratio with C_R is the Γ factor, which is called the subthreshold C_R modification factor. This parameter is exponentially dependent to the difference of the zero-biased threshold voltages of pMOS and nMOS transistors ($V_{tp} - V_{tn}$). Fig. 4 exhibits that the variation of this factor in 1k Monte Carlo samples at the supply voltage of 0.3 V is between 0.66 and 0.44. Since $\Lambda = 2.48$, for β equal to 1, the D_R value varies from 1.1 to 1.5, and still provides a higher driving strength of the PD transistor compared with the access transistor for lower ZLD. For the 6T-NA, Λ is equal to 1 and the threshold voltage mismatch between access and the PD transistor causes variation in Γ. The variation in Γ due to threshold voltage mismatch is between 0.84 and 1.34. The following comments can be raised based on the results. For the iso-area, the D_R value of the 6T-PA is greater than that of 6T-NA in the subthreshold region. To make D_R of the 6T-NA greater than 1.1 (minimum D_R of 6T-PA), the width of the PD transistor has to be 30% larger than the access transistor to cope with the variation of Γ. The most suitable technologies for providing stable 6T-PA

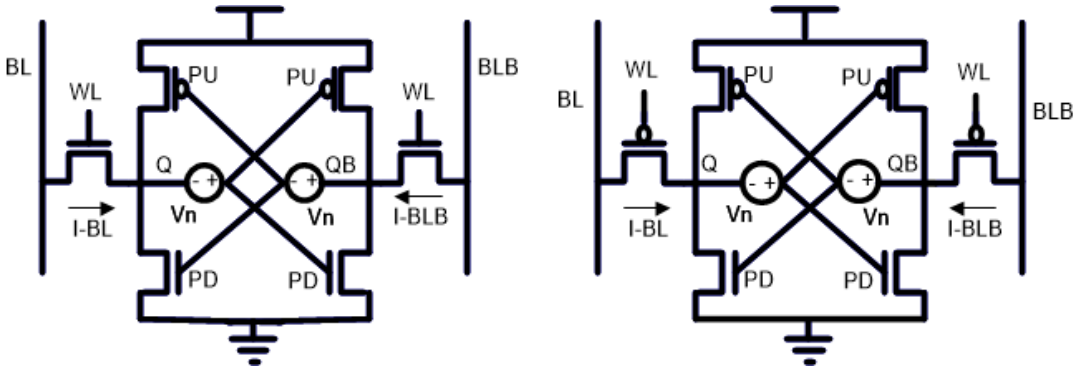


Fig. 7. Test setup with two differential noise sources for (a) 6T-NA and (b) 6T-PA.

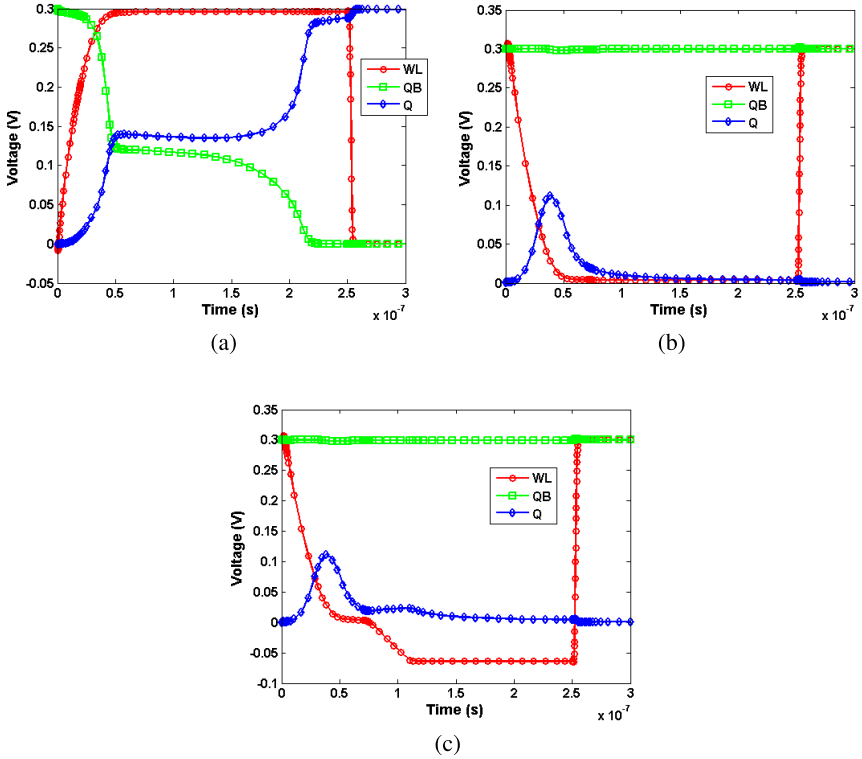


Fig. 8. Transient behavior of internal nodes at 300 mV when the differential noise of ±25 mV is applied on (a) 6T-NA at the FS corner, (b) 6T-PA at the SF corner, and (c) 6T-PA with −65 mV of WL boosting at the SF corner at $T = 25$ °C. Data flips in 6T-NA while 6T-PA and 6T-PA with WL boost remain stable.

bitcells in the subthreshold operation are those with $|V_{tp}| > V_{tn}$ (i.e., $\Gamma > 1$). The optimum 6T-PA bitcells implemented in these technologies are smaller and, hence, consume lower amounts of energy.

In the following, we calculate the ZLD of both bitcells analytically. The subthreshold current of the access and the PD transistors of the 6T-NA is given in (7) and (9)

$$I_A = I_0 \frac{W_A}{L_A} e^{\left(\frac{V_{\rm DD}-V_Q-V_{tn}-\lambda V_Q+\eta(V_{\rm DD}-V_Q)}{n v_T}\right)}\left(1-e^{-\frac{V_{\rm DD}-V_Q}{v_T}}\right) \quad (7)$$

$$I_0 = \mu_n C_{\rm ox}(n-1)v_T^2 \quad (8)$$

$$I_D = I_0 \frac{W_D}{L_D} e^{\left(\frac{V_{\rm DD}-V_{tn}+\eta V_Q}{n v_T}\right)}\left(1-e^{\frac{-V_Q}{v_T}}\right). \quad (9)$$

In order to find the ZLD (V_Q), we equalize the current flowing through the access transistor with that of PD transistor (*i.e.*, $I_A = I_D$). By equalizing these two currents, for $V_{\rm DD} = 0.3$ and $n = 1.5$, we can achieve

$$e^{\left(\frac{-V_Q}{n v_T}\right)^{2.7}} = \frac{\beta}{2}\left(e^{\left(\frac{-V_Q}{n v_T}\right)^{1.4}} - e^{\left(\frac{-V_Q}{n v_T}\right)^{2.9}}\right). \quad (10)$$

Recalling from (5), β is equal to $(W_D/L_D/W_A/L_A)$. To solve for V_Q, we first solve for $e^{(-V_Q/nv_T)}$, from which V_Q can be calculated.

Similar to the 6T-NA bitcell, we can calculate V_Q for the 6T-PA as

$$V_Q = v_T \times ln\left(\frac{-1}{\frac{\frac{\mu_p}{\mu_n}e^{\left(\frac{V_{tn}-V_{tp}}{n v_T}\right)}}{\beta} - 1}\right). \quad (11)$$

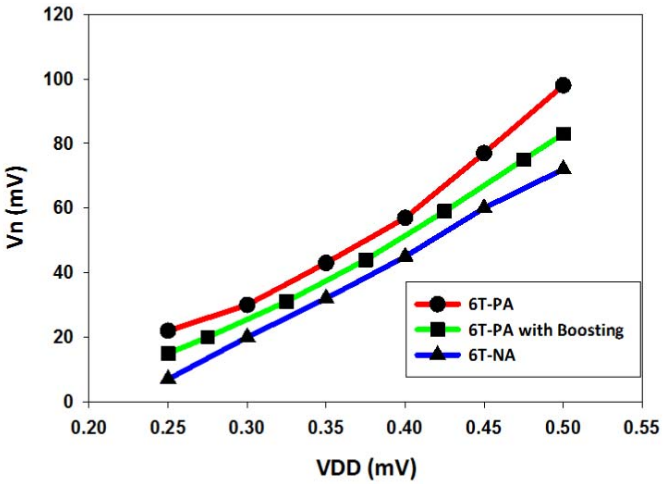


Fig. 9. Maximum tolerable differential noise during read operation versus V_{DD} at the FS corner for 6T-NA and the SF corner for 6T-PA with and without boosting, $T = 25$ °C.

Fig. 5 shows V_Q obtained analytically from (10) and (11) and from simulation for both 6T-NA and 6T-PA at 300 mV. This figure shows that the 6T-PA suffers less from ZLD.

As mentioned before, unlike the 6T-NA, the 6T-PA provides better read stability partly owing to the access transistor connected to the internal node with high voltage V_{DD}. To further investigate this behavior, we applied a single-ended positive noise [Fig. 6(a)] to both cells at node retaining logic 0. Single-ended noise mimics the read disturb behavior of the cell and can be correlated with cell stability during the read operation. As shown in Fig. 6(b), when a pulse of 150 mV is applied to the node Q of the 6T-NA bitcell, the node QB decreases down to 146 mV. However, the node QB in the 6T-PA discharges down to 246 mV. Fig. 6(c) shows the simulation results of a single-ended voltage noise source applied on the bitcells in worst case corners as a function of supply voltage. As shown in Fig. 6, the 6T-PA can tolerate much higher single-ended noise compared with the 6T-NA. For example, at 0.3 V, the 6T-PA can tolerate 215 mV of single-ended noise, whereas the 6T-NA tolerates 135 mV. By applying WL boosting, V_{GS} of the right access transistor increases, and this causes the right access transistor to become more resistive in holding the node QB at V_{DD}. In other words, the right access transistor partially offsets the effect of ZLD. Therefore, the 6T-PA can tolerate up to 225 mV of single-ended noise when -65 mV of WL boosting is applied at 0.3 V [shown in Fig. 6(c)].

The stability of the 6T-PA is also compared with the 6T-NA when two differential noise sources are incorporated in the bitcells, as shown in Fig. 7(a) and (b) [17]. Fig. 8(a)–(c) shows the transient behavior of node Q and QB during a read operation when a differential noise of 25 mV is applied on the 6T-NA, 6T-PA, and 6T-PA with WL boosting. As shown in Fig. 8, a data loss occurs for the 6T-NA, and data remain stable for both cases of 6T-PA. Moreover, when WL boosting is applied on the 6T-PA, the node QB remains close to V_{DD}, and the node Q of the 6T-PA shows higher ZLD. In total, the 6T-PA with boosting shows less stability compared with when WL boosting is not available. Fig. 9 shows the maximum differential noise tolerated by the 6T-NA and 6T-PA with and without boosting as a function of V_{DD}.

The proposed sizing of the 6T-PA shown in Fig. 1(a) achieves a read yield of 99.99%. The yield is obtained by counting the number of correct read operations in 10k Monte Carlo simulations. Monte Carlo simulation results show that to achieve the same read stability of the 6T-PA bitcell, the PD transistors of 6T-NA bitcell has to be sized 60% larger, which results in 20% larger bitcell area.

III. Writability Analysis

As described in Section II, the 6T-PA has improved SNM compared with the 6T-NA; consequently, the 6T-PA has lower WM compared with the 6T-NA.

Fig. 10 shows the butterfly curves of write operation for 6T-NA and 6T-PA for their worst corners. The worst corner for writing into the 6T-NA is the SF corner (nMOS slow and pMOS fast) and the worst corner for writing into the 6T-PA is the FS corner. For example, the WM of the 6T-PA and the 6T-NA is equal to 12 and 27 mV, respectively, at 300 mV. Fig. 11(a) shows the WM of both bitcells at worst corners versus supply voltage (V_{DD}). As shown in these figures, the 6T-PA has lower WM compared with the 6T-NA. Assuming both bitcells have logic zero initially in Fig. 1, the right access transistor of the 6T-NA is fully on ($V_{GS} = V_{DS} = V_{DD}$) and starts to discharge the QB node. On the other hand, the left-access transistor is also fully on ($V_{GS} = V_{DS} = V_{DD}$) and helps in writing by raising the voltage of node Q to ZLD level. For the 6T-PA, the left access transistor is fully on similar to that of the 6T-NA. However, as opposed to the 6T-NA, since the BLB and the WL are both at 0, V_{GS} is constructed between the WL and node QB. During the write process, where the node QB starts discharging, the right-access transistor starts getting weaker as the V_{GS} decreases and it turns off when the node QB goes below the threshold voltage V_{tp}. Therefore, the 6T-PA bitcell has reduced writability compared with the 6T-NA.

Fig. 11(b) shows the write-yield percentage of write operation of both 6T-NA and 6T-PA bitcells at 250 mV at worst corners. The write yield is achieved by counting the successful write operations in 10k Monte Carlo simulations at the worst corner. As shown in this figure, the yield of the 6T-PA is 22% less than that of the 6T-NA. To overcome the weak writability of the 6T-PA, we utilize negative WL boosting. As shown in Fig. 11(b), by applying 40 mV of negative WL boosting on the 6T-PA bitcell, the yield percentage increases up to 99.99%. The boosting circuitry and the permitted range are explained in Section IV.

IV. WL Boosting Circuit Implementation

Fig. 12 shows a 5–32 row decoder with two booster circuits and the corresponding control block. The booster circuit is externally programmable to provide WL boost and no boost options. The boosting option is selected when signal mode-select is asserted high. Together with the CLK-EN signal, the MSB address bit, A, selects one of the two booster circuits. When both of these signals make positive transition,

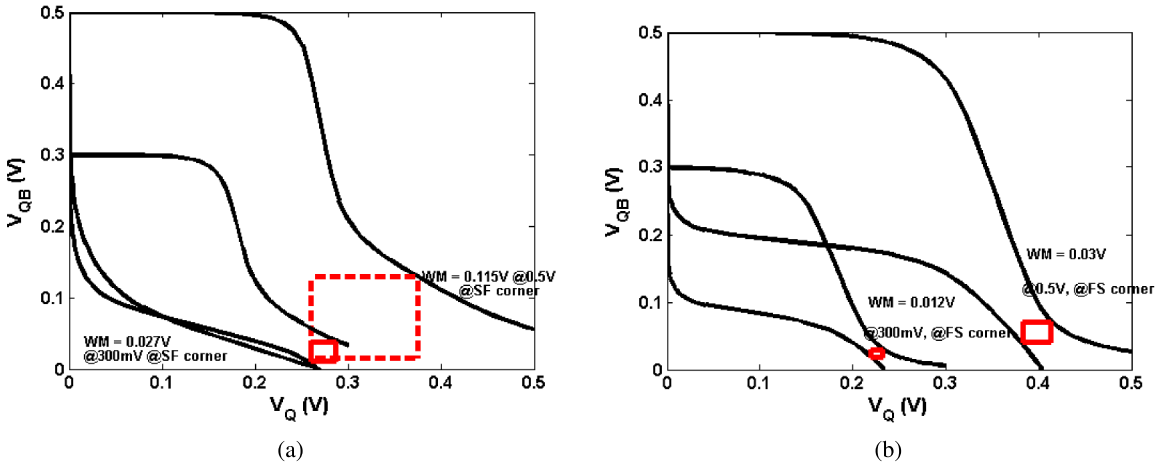


Fig. 10. WM butterfly curves at $V_{DD} = 0.3$ V and $V_{DD} = 0.5$ V for (a) 6T-NA at the SF corner and (b) 6T-PA at the FS corner, $T = 25$ °C.

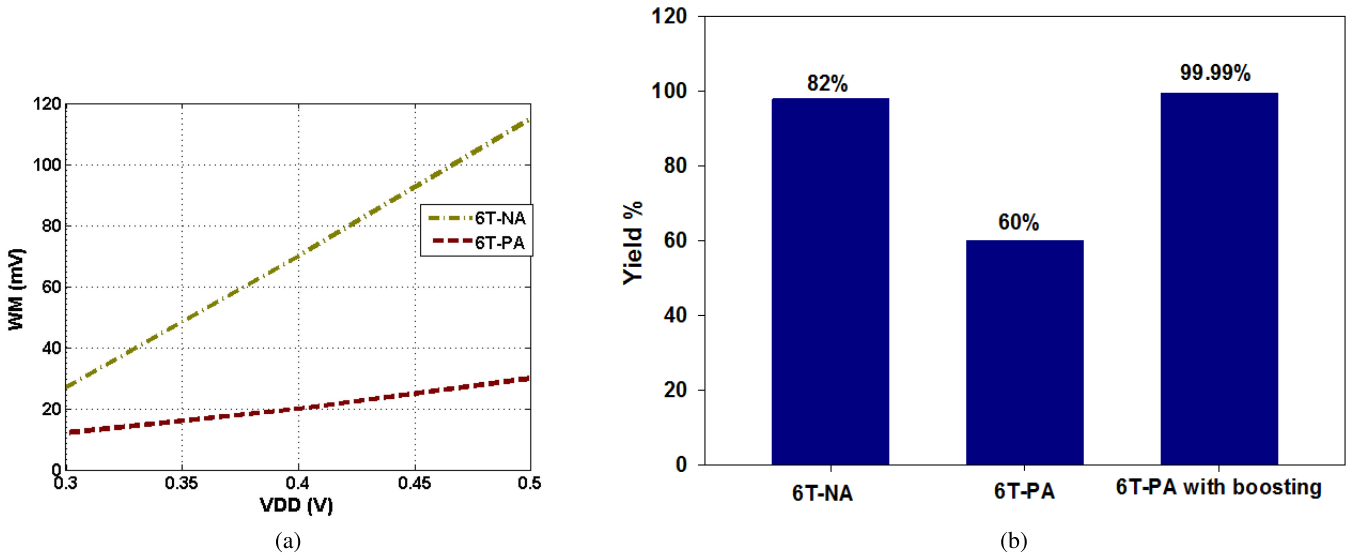


Fig. 11. (a) WM versus V_{DD} for 6T-NA at the SF corner and 6T-PA at the FS corner, $T = 25$ °C. (b) Write yield percentage of 6T-NA, 6T-PA, and 6T-PA with negative WL boosting at 250 mV.

the output of the corresponding NAND gate goes low switching OFF N1. The Miller capacitance between the gate and the drain of N1 makes its drain voltage negative. Since the N2 transistor is ON, the Vboost goes to the negative voltage, and this will negatively boost the selected WL in the decoder. Fig. 13(a) shows the read and write yield of the proposed 6T-PA bitcell versus boost voltage (V-Boost) at 300 mV. The yield percentage is achieved by counting the number of successful read (write) operations in 10k Monte Carlo read (write) operations. As shown in this figure, the minimum boosting voltage required to achieve 100% write yield is −40 mV. Moreover, the read failure starts happening when −100 mV of WL boosting is applied. Therefore, the permitted range of WL boosting is between −40 and −100 mV at 300 mV of supply voltage. Fig. 13(b) shows the permitted range of WL boosting, minimum required WL boosting voltage for write operation, and maximum level of WL boosting for read operation at different supply voltages. As shown in this figure, the permitted range of WL boosting increases by increasing the supply voltage.

The boosted voltage is a function of the Miller capacitance, the capacitance of the Vboost node shown in Fig. 12, and the supply voltage. Fig. 14 shows the boost voltage versus Miller capacitance at different supply voltages. The negative boost value increases by increasing the Miller capacitance and the supply voltage.

Fig. 15 shows the access time and power consumption of the 5-bit decoder with booster circuit connected to the memory array versus Miller capacitance. As shown in this figure, by increasing the Miller capacitance, the access time decreases, while the power consumption increases. The energy consumption versus Miller capacitance shown in Fig. 14 is calculated by multiplying the access time by the power consumption. As shown in this figure, the minimum of the energy consumption occurs when a 200 fF is utilized for the Miller capacitance.

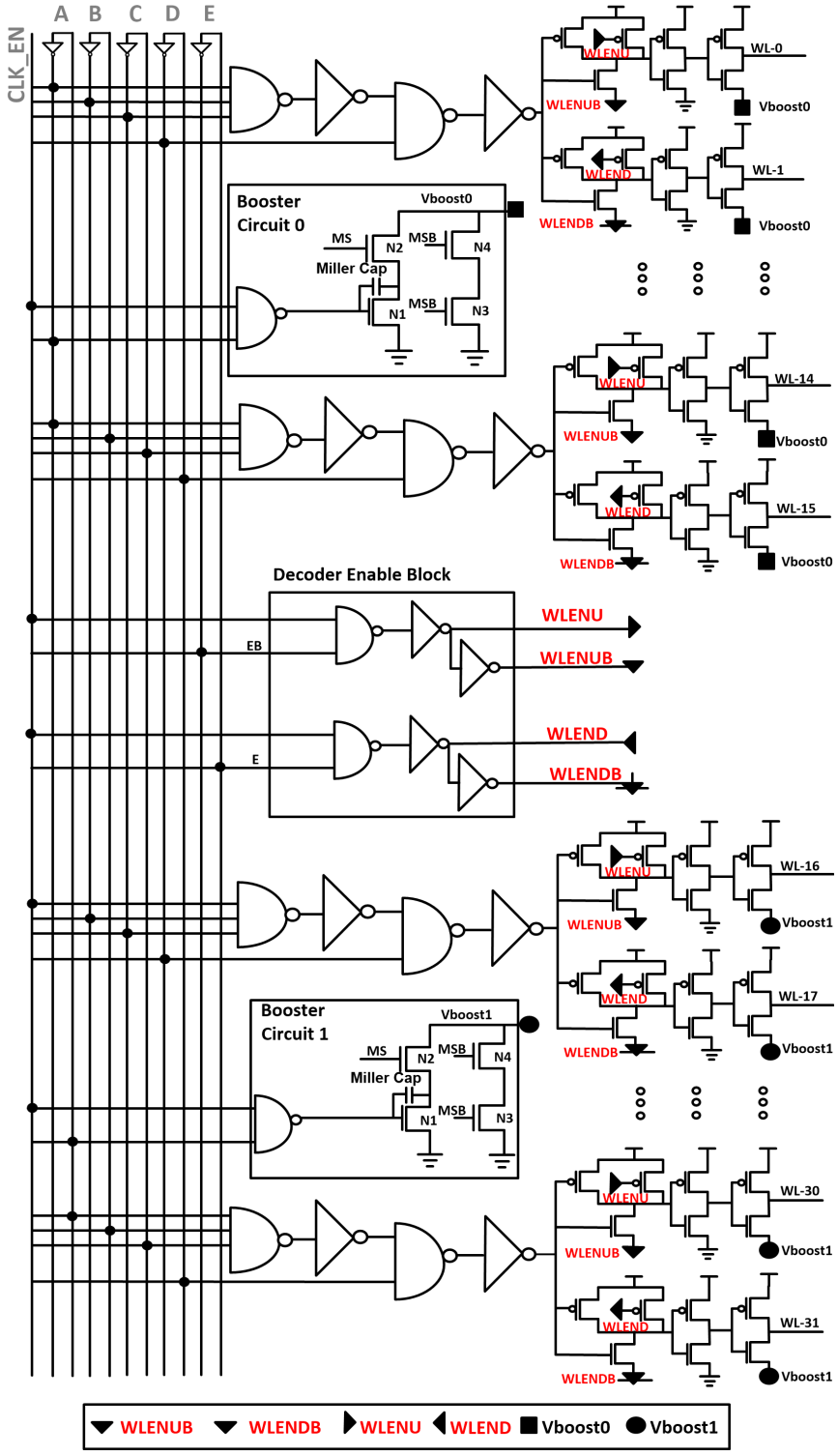
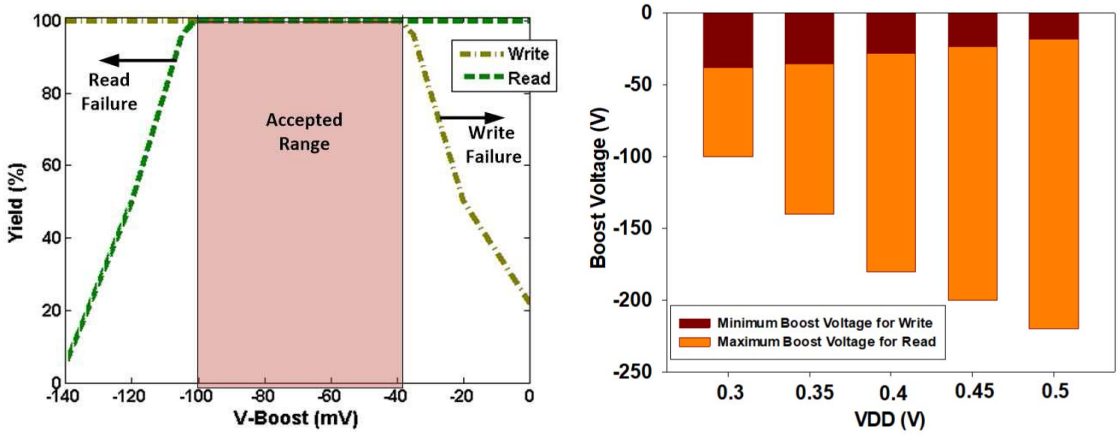


Fig. 12. Implementation of 5-bit row decoder with negative WL booster circuit.

The Miller capacitance in the booster circuit is implemented with metal–insulator–metal (MIM) capacitor provided by the foundry, as top-level metals can be utilized reducing the area overhead for the implementation. Since the MIM capacitors are constructed by top metal layers, they are positioned on top of the decoder with no area overhead. However, since low-level metals are utilized in constructing MOS capacitances, the decoder area increases by 11%. In addition, for subthreshold operation, MIM capacitors provide a reliable alternative to the MOS-based capacitors. The MOS gate capacitance is inherently non-linear, and also has leakage associated with it. Simulation results show that a 200-fF capacitance realized through gate oxide is impacted by process variation in the subthreshold voltage regime, which leads to 30-mV variation



(a) (b)

Fig. 13. (a) Write and read yield versus boosted WL voltage at 300 mV. The colored area shows the accepted range of WL boosting. (b) Permitted range of WL boosting versus V_{DD}.

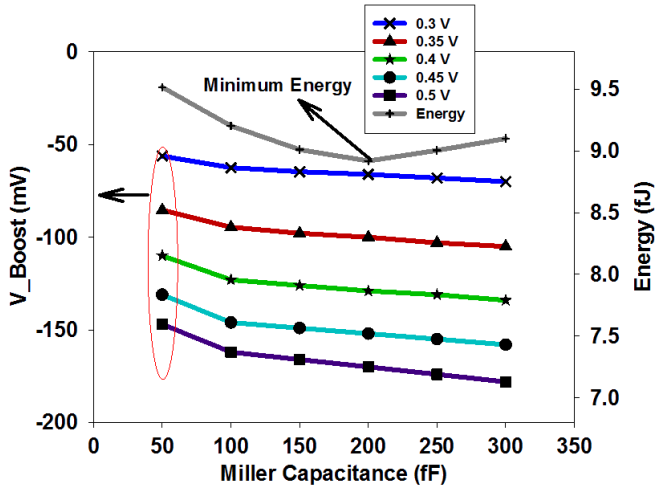


Fig. 14. Boost voltage of the WL versus Miller capacitance at different supply voltages, TT corner, 25 °C and energy consumption of the 5-bit row decoder versus Miller capacitance at 300 mV, TT corner, 25 °C.

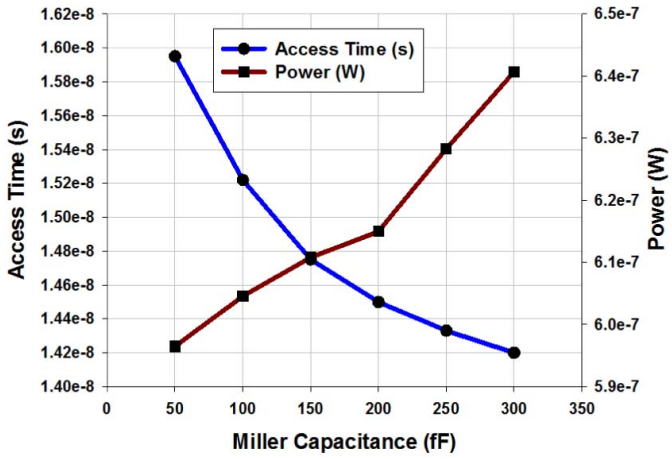


Fig. 15. Access time and power consumption of the 5-bit row decoder versus Miller capacitance at 300 mV, TT corner, 25 °C.

in the boost voltage at 0.5 V. Fig. 16 shows 10k Monte Carlo simulation of the boost voltage when Miller capacitance is utilized at different supply voltages. As shown in this figure, the variation of the boosted voltage is about 9.9 mV at 0.5 V.

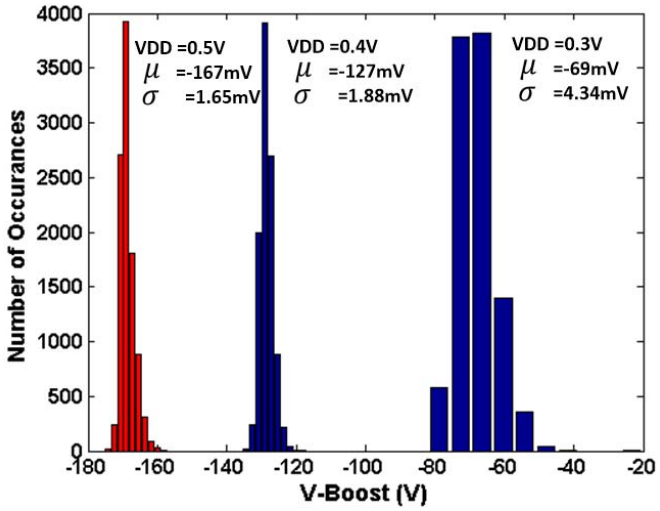


Fig. 16. 10k Monte Carlo simulation of boosted WL voltage at 0.3, 0.4, and 0.5 V.

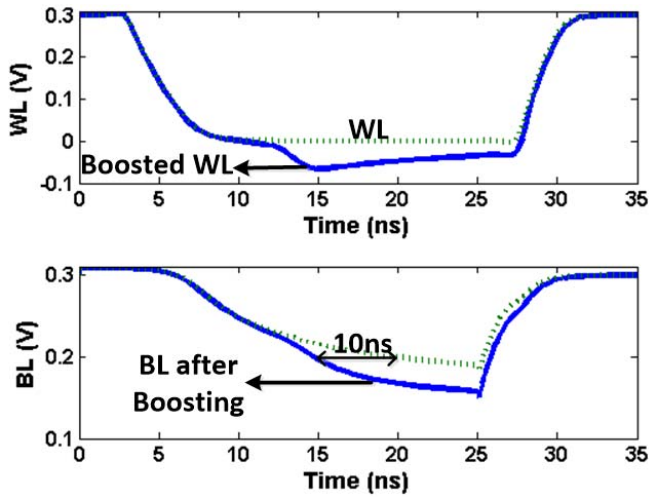


Fig. 17. Simulated timing of WL and BLs for boosted and non-boosted options at 300 mV, TT corner, 25 °C.

Fig. 17 shows the transient simulation of WL with and without boosting. When the WL is negatively boosted, the time required to develop 100 mV of differential voltage (ΔBL) is

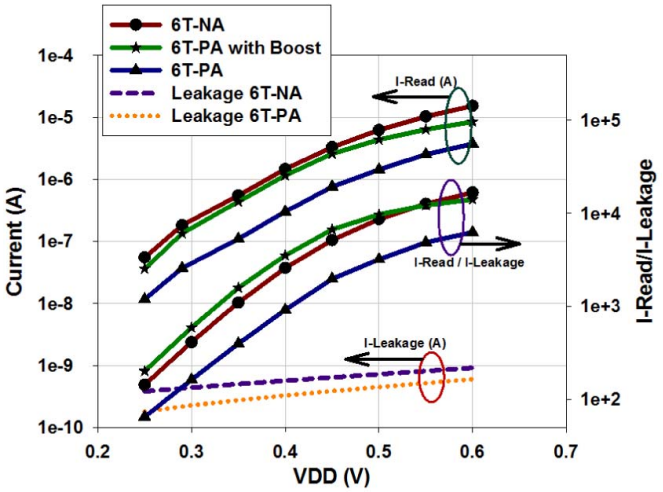


Fig. 18. Read current, leakage current, and read current to leakage current ratio of the 6T-NA and 6T-PA bitcells versus supply voltage, at TT corner, 25 °C.

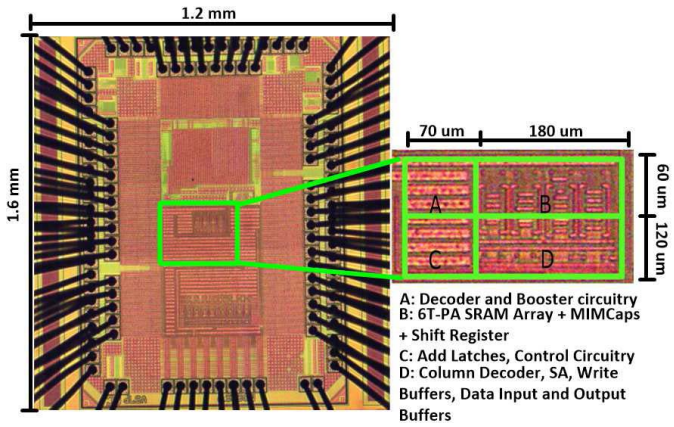


Fig. 19. Micro-graphic image of the fabricated chip in the 65-nm CMOS technology.

reduced by 10 ns. In addition, simulation results show that activating the booster circuitry increases the average consumed total current by 2.6%.

V. Read and Leakage Current

Amongst other factors, the SRAM read current (I_{Read}) determines its operational speed. In particular, I_{Read} can be constrained either by the driver transistor or access transistor. For example, for the conventional 6T-NA cell, the saturated access transistor limits the read current. The driver transistor is typically designed to be stronger to ensure read stability, and is capable of sinking larger current. Situation is similar for the 6T-PA, where the saturated pMOS access transistor limits the cell current. However, owing to its small mobility, I_{Read} is substantially smaller. Fig. 18 shows I_{Read} of both bitcells. As shown in this figure, for the iso-area, I_{Read} of the 6T-NA is higher than that of the 6T-PA bitcell. For example, I_{Read} of the 6T-NA and the 6T-PA at 290 mV is 180 and 36 nA, respectively. Negative WL boosting enhances I_{Read} of the 6T-PA substantially, specifically in the subthreshold region. For example, a negative WL boost of 65 mV at V_{DD} of 290 mV increases the read current to 140 nA.

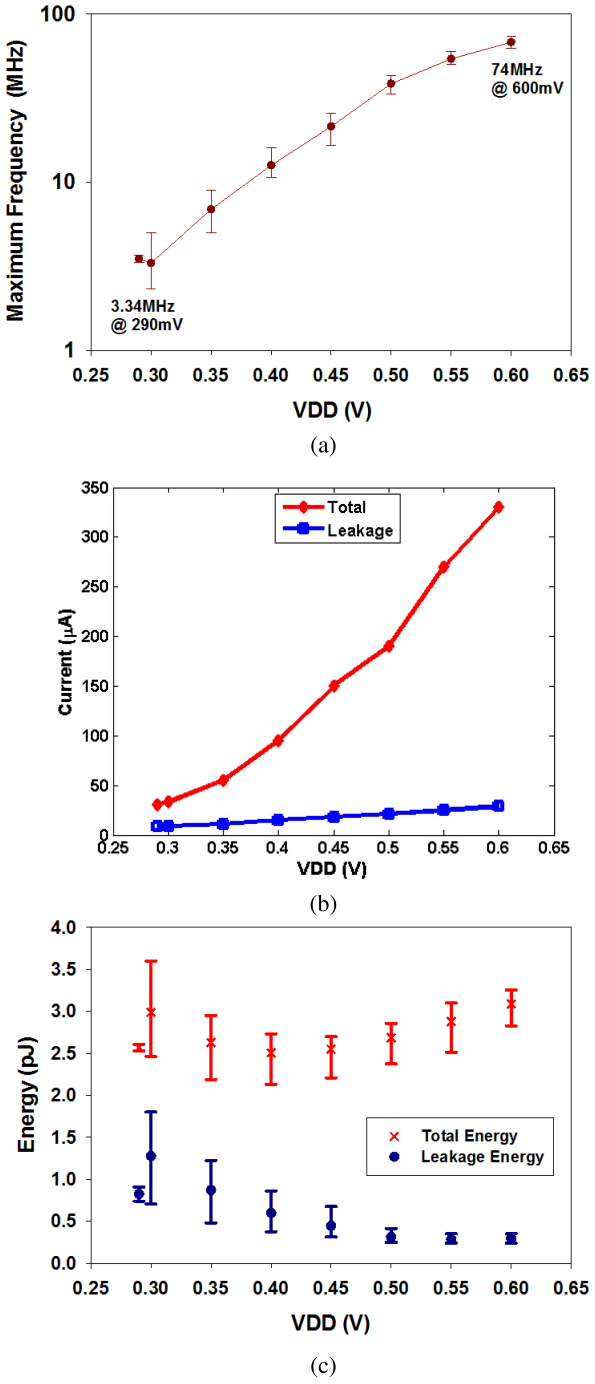


Fig. 20. (a) Measured frequency of operation with respect to the supply voltage. (b) Measured total current and leakage current with respect to the supply voltage. (c) Total energy and leakage energy with respect to the supply voltage. $T = 25°$.

Fig. 18 also shows the leakage current (I_{Lakage}) of the 6T-NA and 6T-PA bitcells. The leakage current for the 6T-NA and the 6T-PA at 290 mV is 0.44 and 0.22 nA, respectively. Therefore, an SRAM array with 6T-PA cell has the potential to reduce its leakage current.

A sense amplifier requires sufficient differential voltage to make reliable decision, which necessitate not only high cell read current, but also low as possible leakage current through unselected cells in the column. Consequently, the ratio

TABLE II
COMPARISON WITH CHOSEN PREVIOUS SUBTHRESHOLD SRAMS

Design	Technology (nm)	Cell Type	Size (kb)	V_{min} (mV)	$I_{Leakage}$ (nA/b)	Speed (MHz) @ 0.35 V [a]	E_{min} (fJ/b)	EDP ($\times 10^{-21}$ J.s/b) @ 0.35 V	Cell Area (μm^2)
This Work	65	6T	2	290	4.25	9.2	1.1	0.125	2.15
JSSC08 [6]	130	6T	2	210	119	0.45	0.55	1.22	4
JSSC13 [18]	65	7T	32	260	N.A	8.5	0.175 [c]	N.A [b]	N.A [b]
JSSC08 [7]	65	8T	256	350	0.024	0.025	0.5	20	N.A [b]
JSSC16 [11]	65	8T	32	200	0.034	2	0.031	0.015	1.35
JSSC13 [10]	65	9T	2	220	N.A [b]	1.2	0.3	15.16	4.6

[a] The speed is extracted based on the given data for each reference.
[b] Not Available.
[c] The energy data is reported only for 260 mV.

of I_{Read}/I_{Lakage} is an important parameter that restricts the number of cells in a column. Fig. 18 shows this ratio for 6T-NA and 6T-PA cells. As expected, the 6T-NA cell is substantially better compared with the 6T-PA, and however, a negative WL voltage boost significantly improves this ratio, specifically for sub-350-mV operation.

VI. TEST CHIP MEASUREMENT AND IMPLEMENTATION

A test chip with 2-kb SRAM was designed and fabricated in the TSMC 65-nm GP CMOS technology. The I/Os in this technology operate at 2.5 V and are capable of interfacing with the core logic at 1 V. We designed level shifters capable of shifting 200-mV input to 1 V, and vice versa. The die photograph is shown in Fig. 19. To test the functionality of each die, we performed write and read access with random data. A total of ten dies were measured, and found to meet functional requirements. Within these samples, all of them were able to operate at 310 mV, nine of the dies were able to operate at 300 mV, and two at 290 mV.

Fig. 20(a) shows the measured maximum operational frequency versus supply voltage. Each vertical bar shows the maximum, minimum, and the average measured data. The maximum frequency is achieved as high as 3.34 MHz at 290 mV. At 0.6 V, the maximum frequency achieved was 74 MHz.

Fig. 20(b) shows the measured total and leakage current. The total current was measured while performing successive write and read operation at different addresses. The average of this current is shown in the Fig. 20(b). The leakage current was measured, while the macro was inactive. The total and leakage current are measured as 30 and 8.5 μA, respectively, at 290 mV. Measurement results show that the total average current increases by 3% when the booster circuit is activated.

The energy consumption can be computed by dividing the power consumption by the maximum frequency. The total and leakage energy consumption is shown in Fig. 20(c). The minimum total energy is calculated as 1.1 fJ/bit at 400 mV, and the leakage energy is calculated as 0.37 fJ/bit at 290 mV.

Table II summarizes and compares the key features of our design with the previous subthreshold SRAMs that include the 6T [6], 7T [18], 8T [7], [11], and 9T [10] bitcells. Comparing our design with the designs shown in Table II reveals that utilizing 6T-PA bitcell and incorporating WL boosting enables us to reduce the supply voltage to 290 mV, which is lower than V_{min} reported for the 8T in [7]. The design in [6] and [10] was able to further reduce the V_{min} close to 200 mV at the cost of significant additional bitcell area. The design in [11] has reduced V_{min} of 350 mV of the 8T in [7] by manipulating the stored data at the system level that eliminates the worst case data distribution in each column. This design reveals that how system-level approaches can improve the key parameters of application specific SRAMs.

To perform a comparison on the speed of these designs, we reported the speed of all the memory macros at 350 mV. It shows that our design can operate at higher speed due to the combination of differential sensing and negative WL boosting

compared with the designs in [6], [7], [11], and [18]. The 9T bitcell in [10] utilizes differential sensing, and however, non-minimum length transistors and high threshold voltage (low speed) transistors are used in their bitcell.

To enable reliable low-power operations, we overdesigned drivers and peripheral circuits specially the circuits connected to the IOs, such as level shifters, latches, buffers, and flip-flops, which, in turn, increase the leakage current and the energy consumption.

Finally, we compare the energy-delay-product (EDP) per bit of all designs in Table II. It shows that except for the design in [11] which is optimized for video specific applications, our design has the lowest EDP per bit.

VII. Conclusion

For the subthreshold operation, the conventional nMOS access 6T SRAM cell suffers from poor read margin and WM. In this paper, a 6T SRAM bitcell with pMOS access transistors and enhanced read margin and WM operating in the subthreshold region is proposed. We utilize pMOS access transistors to increase the stability of the bitcell during read operation. This is verified by simulation and analytical analysis. To overcome with the weak writability of the proposed 6T bitcell, we utilize WL boosting.

The negative WL boosting also helps to compensate the loss of speed of the pMOS access transistors. A 2-kb SRAM is fabricated in the 65-nm TSMC technology. The measurement results show 3.34 MHz of speed and 8.5 μA of leakage current at 290 mV. The minimum energy is observed as 1.1 fJ/bit at 400 mV.

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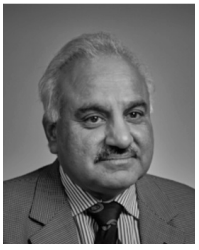

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