

A Battery-Powered Wireless Ion Sensing System Consuming 5.5 nW of Average Power

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Abstract—This paper presents a battery-powered wireless ion sensing platform featuring complete sensing-to-transmission functionality. A 1 mm × 1.2 mm chip fabricated in 65 nm includes a 406 pW potentiometric analog front end, a 780 pW 10-bit SAR ADC, a 2.4 GHz power-oscillator-based wireless transmitter that consumes an average of 2.4 nW during a 10-sample/sec transmission rate, two timing generation oscillators that each consume 140 pW, and a 3:1 switched-capacitor dc–dc converter with 485 pW of quiescent power that achieves the efficiencies of 96.8% and 70.5% at 60 and 3.9 nW loads, respectively. The chip connects to a screen-printed ion-selective electrode responsive to sodium ions, and *in vitro* testing across an NaCl solution concentration range of 0.1–100 mM exhibited a linear near-Nernstian response with a slope of 71 mV/log₁₀[Na⁺]. When all blocks are operating, the system consumes an average of 5.5 nW.

Index Terms—Biosensing, *in vitro*, ion-selective electrodes (ISEs), near-zero power, power oscillator, reference-free SAR analog-to-digital converter, relaxation oscillator, ultra-low-power.

I. INTRODUCTION

ADVANCES in sensors and wireless technologies have enabled new and exciting classes of wearable devices for applications in precision athletics, health, and wellness. However, growth in the wearables market has been slower than many expected, in part due to challenges related to device size, battery life, and sensing capabilities. For example, many current wearables with relatively sophisticated capabilities are larger than desired, in part due to the requirement of a large battery, which is necessary to have acceptable battery life given the relatively high power consumption of underlying circuits. In addition, many wearable devices currently measure only a small handful of physical or electrophysiological parameters such as pressure [1], motion [2], temperature [3], electrocardiography (ECG) [4], or electroencephalography (EEG) [5].

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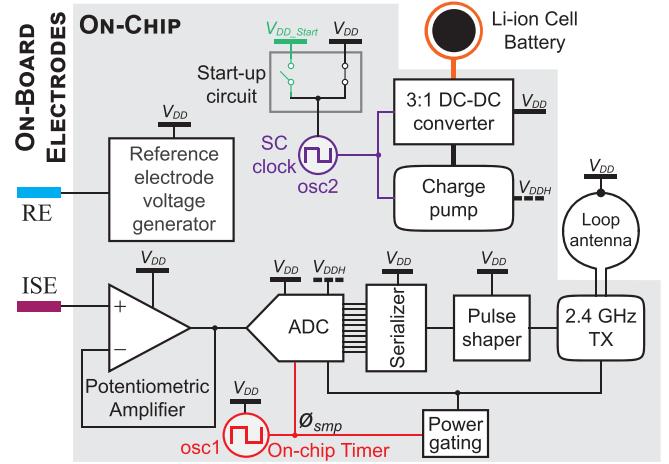


Fig. 1. Block diagram of the wireless ion sensing system.

While such parameters might be useful for general well-being or for very specific medical use-cases, more sophisticated sensing functionality is desired to make information derived from wearables more actionable and/or impactful across a wide range of applications.

Measurement of physiochemical parameters, for example ion homeostasis in sweat, blood, saliva, or tears, can potentially provide valuable additional insight into a user's overall health status. For example, measurement of sodium together with heart rate may enable real-time assessment of the risk of congestive heart failure, while monitoring of sodium and calcium may enable diagnosis or monitoring of syndrome of inappropriate anti-diuretic hormone secretion or hyponatremia. While previous work has demonstrated real-time sensing of ion concentration is possible on the body via low-cost patches, temporary tattoos, and other form factors [6]–[8], such sensors were not integrated with small, ultra-low-power sensing instrumentation, and/or wireless communication functionality.

This paper presents the design of a sensing system that integrates ion-selective electrodes (ISEs) with ultra-low-power sensor instrumentation, a wireless transmitter, and power management circuits [9]. A block diagram of the system is shown in Fig. 1. All circuit blocks, described in detail in Section II, are carefully designed and optimized to consume nW power levels (or lower) in order to ensure ultra-long operation under battery power, or in the future implementations via small energy harvesters (e.g., [10], [11]). Measurement results,

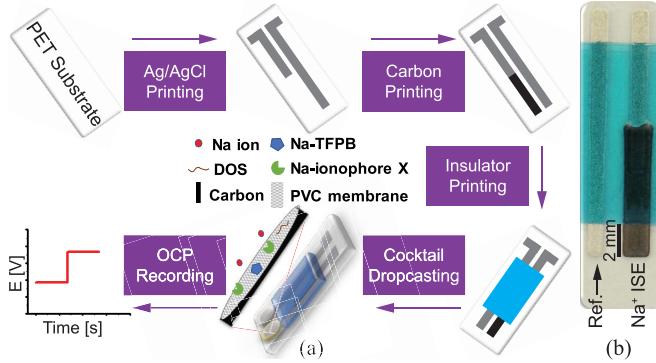


Fig. 2. (a) Fabrication procedure of the ISE. (b) Photograph of a fabricated ISE.

presented in Section III, reveal the nW-level power consumption with acceptable system-level performance, including *in vitro* results of sodium ion sensing.

II. WIRELESS ION SENSING PLATFORM

The proposed ion sensing system, shown in Fig. 1, comprises an ion-selective electrode that interfaces to a high-impedance potentiometric amplifier. A co-fabricated reference electrode (RE) is driven by a reference voltage generator, and is used to set the solution potential. The output of the potentiometric amplifier is digitized by a 10 S/s reference-free charge-sharing analog-to-digital converter (ADC). Digital samples are then serialized, shaped, and then sent to a 2.4 GHz RF transmitter. The overall wireless sensing system is powered from a 1.8 V supply, for example, from a small on-board battery, which is divided by a 3:1 switched-capacitor dc–dc converter to generate a 0.6 V supply voltage, V_{DD} , used by the majority of the circuits on-chip. A second supply voltage, $V_{DDH} = 1.2$ V, is generated by an on-chip charge pump for the purposes of increasing the I_{ON}/I_{OFF} ratio of critical transistors via boosted gate driving or super cutoff gating. A startup circuit is employed to ensure the dc–dc converter is clocked during cold-start before the switched-capacitor output is stabilized. Power gating, implemented with thick-gate transistors, is utilized to minimize the leakage current of the critical blocks during the off-state. A serial peripheral interface (SPI) bus is implemented to perform benchtop calibration to characterize each block in Fig. 1. Design considerations and implementation details of each block are presented in Sections II-A–II-E.

A. Fabrication of ISEs and Implementation of the Potentiometric Front End

The ISE and RE were fabricated utilizing screen-printing technology by employing an MPM-SPM semi-automatic screen printer (Speedline Technologies, Franklin, MA, USA). Fig. 2(a) outlines the overall fabrication procedure. A sequence of a silver/silver chloride (Ag/AgCl) and graphite layers followed by an insulator layer were printed on a polyethylene terephthalate (PET) substrate, followed by a curing step in a convection oven after the printing step of each layer.

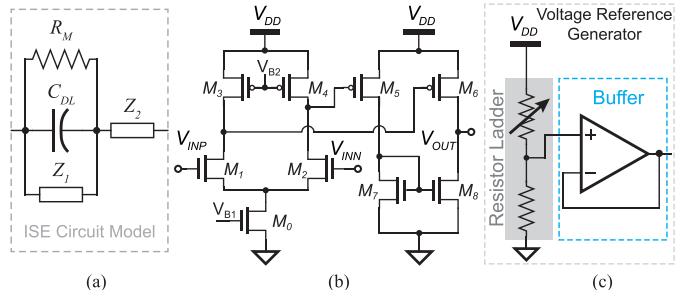


Fig. 3. (a) Equivalent circuit model of the ISE. (b) Schematic of the potentiometric amplifier. (c) Schematic of the reference voltage generator.

Specifically, the Ag/AgCl ink was cured at 85 °C for 10 min, the carbon ink at 80 °C for 10 min, and the insulator layer at 90 °C for 15 min.

The ISE was then modified with a membrane consisting of 1 mg of sodium ionophore X, 0.55 mg of sodium tetrakis (3,5-bis[triuoromethyl]phenyl) borate (Na-TFPB), 33 mg of polyvinyl chloride (PVC), and 65.45 mg of bis (2-ethylhexyl) sebacate (DOS), all dissolved in 660 mL of nitrogen-purged tetrahydrofuran (THF). Up to 4 μL of the sodium ion (Na^+) selective membrane cocktail was then drop-cast on the carbon indicator electrode and left overnight to dry under ambient conditions.

The reference membrane, containing electrolytes and forming a nanoporous structure that allows the exchange of electrolytes with the solution and provides a stable potential insensitive to changes in the ion concentration over a large concentration range, was prepared by dissolving 78.1 mg of Polyvinyl butyral resin BUTVAR B-98 (PVB) and 50 mg of NaCl in 1-mL methanol. Then, the RE was modified by 3 μL of PVB membrane and left to dry overnight alongside the ISE in ambient conditions.

As shown in Fig. 2(b), the fabricated ISE consists of a pseudo-RE, driven by the on-chip reference voltage generator, and a working carbon electrode, which interfaces with the on-chip potentiometric amplifier. A blue insulator was screen-printed over the surface of the electrode pattern to confine the electrode and contact areas and prevent contamination leakage. The electrodes are disposable and an equivalent circuit model [12] is shown in Fig. 3(a), where R_M is the membrane resistance, C_{DL} is the double-layer capacitance, Z_1 is the Warburg diffusional element, and Z_2 represents mobile cation and anion transport through a hydrated film.

To handle the ~0.2–0.5 V input range from the ~GΩ ISE [dominated by R_M in Fig. 3(a)] under the constraints of a 0.6 V supply voltage, a two-stage differential-to-single-ended amplifier with at most three stacked transistors is employed with a 0.3 V output swing, a 50 dB gain, and a 57 Hz unity-gain bandwidth, as shown in Fig. 3, and configured in unity-gain feedback to operate as an impedance buffer. Simulation results show that the potentiometric amplifier achieves ~TΩ input impedance, sufficiently large for interfacing with the ~GΩ ISE, and an output noise of 40 μV. An MOS-bipolar pseudo-resistor-based ladder with a tuning step of 10 mV is implemented to generate a reference voltage,

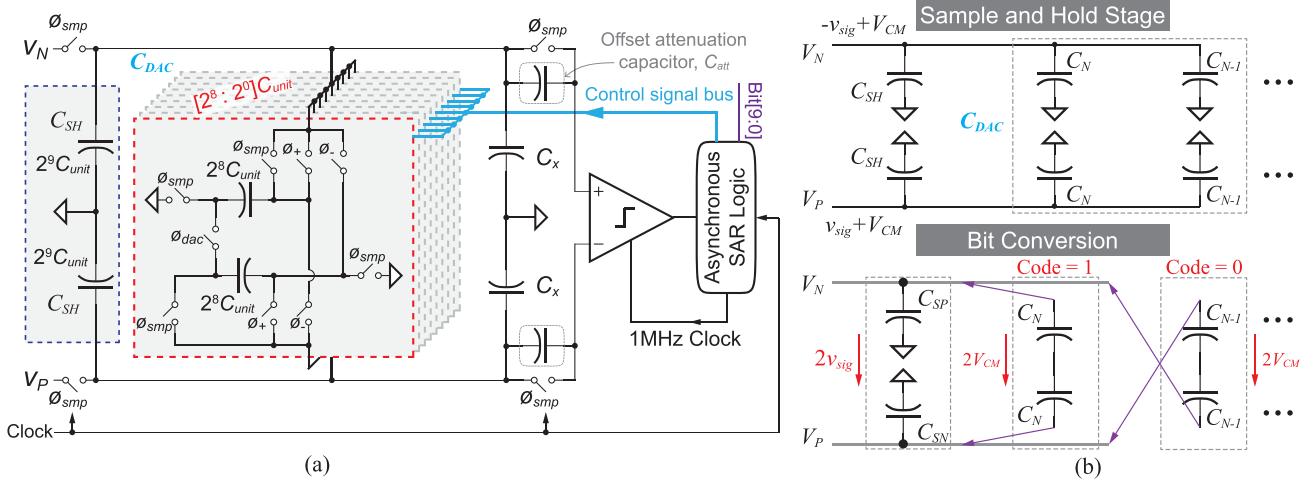


Fig. 4. (a) Schematic of the reference-free charge-sharing ADC with offset-attenuation. (b) Charge-sharing during sample/hold and bit conversion.

with a simulated $380 \mu\text{V}$ variation across 0°C to 100°C and a standard deviation of 4.8 mV due to process variation. This voltage is then buffered by a two-stage amplifier, which directly drives the RE (Fig. 1).

B. Implementation of the ADC and Digital Processing Unit

The output of the potentiometric amplifier interfaces directly to a fully integrated SAR ADC with all necessary peripheral circuitry included. Though previous works have demonstrated SAR ADC structures that achieve power efficient operation, most such solutions require external blocks such as reference generators which can consume even more power than the ADCs [13]. Thus, a reference-free charge-sharing SAR ADC architecture [14] is utilized for digitization in the proposed ion sensing system, where energy from the signal itself is bottom-plate sampled and then charge-shared across the capacitive digital-to-analog converter (DAC) during bit cycling. The overall schematic of the SAR ADC is shown in Fig. 4(a). Here, the input signals, V_N and V_P , which can be represented by $-v_{sig} + V_{CM}$ and $+v_{sig} + V_{CM}$, respectively, are first sampled onto both the sample and hold capacitors, C_{SH} , and the binary-weighted DAC capacitors, C_1 to C_N . During bit conversion, as shown in Fig. 4(b), the differential signal, $2v_{sig}$, is mapped to a charge signal, $Q_{sig} = 2v_{sig}C_{SH}$. In the meantime, V_{CM} is extracted and converted to reference charge, ($Q_N = 2V_{CM}C_N$). The binary-weighted Q_N are then successively connected to V_P and V_N to approximate Q_{sig} until the residual charge between V_P and V_N converges to zero.

The comparator was implemented with an energy-efficient dynamic two-stage topology [15], and is shown in Fig. 5(a). The first stage [indicated by the dashed box in Fig. 5(a)] amplifies the differential input signals from $V_{\{\text{INP},\text{INN}\}}$ to $V_{\{\text{FP},\text{FN}\}}$, while the second stage consists of both a simple voltage amplification stage and a positive feedback loop to achieve rail-to-rail outputs, $V_{\{\text{OUTP},\text{OUTN}\}}$. The input referred noise, σ_V , of the comparator, which is dominated by the input pair of the first stage, is given by

$$\sigma_V = \frac{8kT}{C_P} \frac{\phi_t}{V_{\text{threshold}}} \quad (1)$$

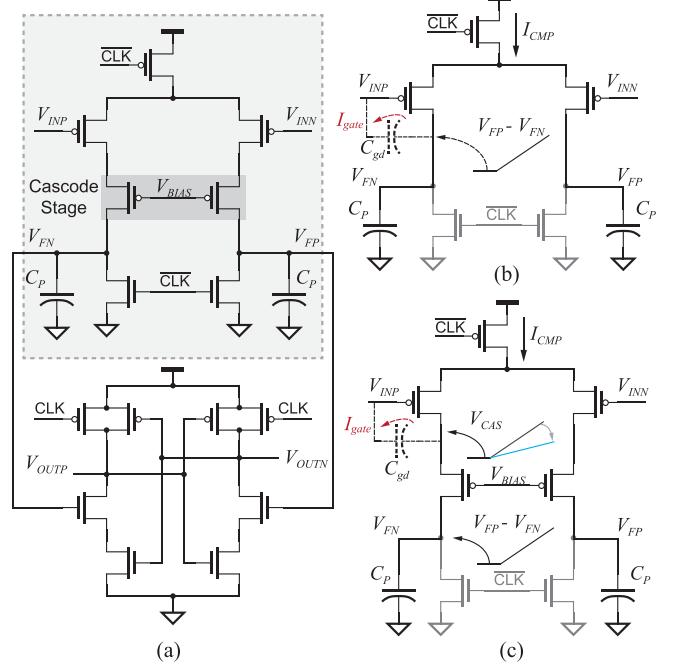


Fig. 5. (a) Schematic of the energy-efficient two-stage comparator. Differential kick-back current to the comparator input (b) without cascode stage and (c) with cascode stage.

where C_P is the parasitic capacitance at the output nodes of the first stage, ϕ_t is the thermal voltage, and $V_{\text{threshold}}$ is the threshold voltage at which the first stage stops and the second stage takes over. To achieve a 10-bit resolution at 0.6 V , C_P was designed to be larger than 40 fF as indicated by (1), and tunable for comparator offset calibration.

Kick-back noise can also be very significant in dynamic comparators. Conventionally, the magnitude of the kick-back noise can be minimized by employing a large capacitor at the comparator input, $C_{\text{cmp,in}}$, which effectively creates a low input impedance. However, in the proposed structure, $C_{\text{cmp,in}}$ consists of C_{att} in series with C_{DAC} . With a gate-drain capacitance $C_{\text{gd}} > 5 \text{ fF}$ in the input stage of the comparator, significant kick-back noise (hundreds of μV) can

be observed at the input of the comparator and thus must be carefully considered in this design. As shown in Fig. 5(b), when the clock signal is high (i.e., when the first stage is in voltage amplification phase), voltages that approximate ramps, $V_{\{rampN,rampP\}}$, are generated at the output nodes of the first stage, which can be given by

$$V_{\{rampN,rampP\}} = \frac{I_{CMP}}{2C_P}t, \quad (2)$$

where I_{CMP} is the dc operating current of the first stage of the comparator. $V_{\{rampN,rampP\}}$, in return, introduce a kick-back current, I_{gate} , via the drain-to-gate capacitor, C_{gd} , of the input transistor pair, which can be computed as

$$I_{gate} = \frac{I_{CMP}}{2C_P}C_{gd}. \quad (3)$$

During each comparison cycle, the first stage operates for a period of T_{int} before the second stages begins to work. T_{int} is given by

$$T_{int} = \frac{2C_P}{I_{CMP}}V_{threshold}. \quad (4)$$

As a result, the total charge variation introduced by the kick-back current during one comparison cycle can be calculated by

$$Q_{var} = V_{threshold}C_{gd}. \quad (5)$$

Though, to the first order, Q_{var} can be canceled out since it shows on both inputs as a common-mode signal, it can effectively introduce an offset due to the mismatch in the input pair as well as in the DAC. More concerning, however, is that signal-dependent charge variation can be observed during the comparison, which would introduce non-linearities. To address kick-back related issues, in the proposed ADC a cascode pair was implemented to isolate the output node from the inputs of the first stage, thus minimizing the signal-dependent charge variation [16], as illustrated in Fig. 5(c). Simulation results reveal a greater than $3\times$ reduction in signal-dependent charge variation by reducing the differential voltage amplitudes at the drain of the input pair.

Since the operation of the charge-sharing ADC is based on the redistribution of the signal charge, Q_{SIG} , sampled during the sample and hold phase plus an error charge, Q_{ERR} during bit conversion phase, non-linearities will be introduced if Q_{ERR} changes as bit conversion proceeds. On the other hand, comparator offsets, due to transistor-matching issues or unequal kick-back, can lead to time-varying Q_{ERR} and thus non-linearities in charge-sharing SAR ADCs [17]. The proposed design employs, in addition to capacitive comparator offset calibration and cascode kick-back reduction transistors, an offset-attenuation capacitor, C_{att} , to isolate the comparator input from the DAC and the sample and hold capacitor. Fig. 6(a) shows a simplified block diagram of the charge-sharing ADC and the input offset voltage of the comparator (V_{os}) without an attenuation capacitor. Here, offset charge, Q_{os} , can be calculated by

$$Q_{os} = V_{os}(C_{SH} + C_{DAC}). \quad (6)$$

As shown in (6), while V_{os} is manifested as a fixed voltage, the charge domain offset, Q_{os} , changes during bit conversion

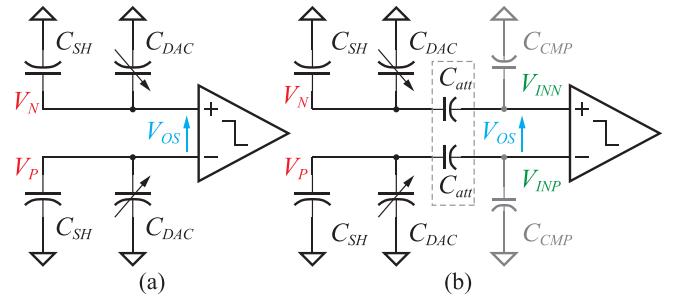


Fig. 6. Comparator offset in charge-sharing SAR ADC (a) without C_{att} and (b) with C_{att} .

as C_{DAC} alters, thereby introducing signal-dependent offset and deteriorating linearity. The offset-attenuation capacitor, C_{att} , employed in this paper, on the other hand, isolates V_{os} from C_{DAC} . As shown in Fig. 6(b), the offset charge at $V_{\{P,N\}}$ becomes

$$Q_{os,att} = V_{os} \frac{C_{att}(C_{SH} + C_{DAC})}{C_{att} + C_{SH} + C_{DAC}}. \quad (7)$$

For fast prototyping, C_{att} is implemented with a 3 pF metal-insulator-metal (MIM) capacitor, while the total capacitance of the C_{SH} and C_{DAC} ($C_{unit} = 44$ fF) is 45 pF, though techniques such as placing capacitors in series or customized metal capacitors can render a smaller C_{unit} . Therefore, $C_{SH} + C_{DAC} \gg C_{att}$ and (7) becomes

$$Q_{os,att} \approx V_{os}C_{att}. \quad (8)$$

The offset charge observed at $V_{\{P,N\}}$ thus becomes constant during bit conversion, as indicated by (8), thereby minimizing the nonlinearity introduced by the input offset voltage of the comparator. On the other hand, the decision making of the comparator is performed at the input of the comparator in voltage domain, $V_{\{INP,INN\}}$. As shown in Fig. 6(b), C_{att} can also divide $V_{\{P,N\}}$ via C_{CMP} , the input capacitance of the comparator. However, since $C_{att} \gg C_{CMP}$ ($C_{CMP} = \sim 10$ fF), the input voltages at the comparator inputs $V_{\{INP,INN\}} \approx V_{\{P,N\}}$, indicating that C_{att} has negligible impact on the dynamic input signal to the comparator. Simulation results reveal a DNL of $+2.1/-1$ LSB with a 2 mV comparator offset without attenuation capacitors [Fig. 6(a)], while a DNL of $+0.7/-0.7$ LSB is achieved by employing the attenuation capacitor, C_{att} , indicating an over $2\times$ linearity improvement, in good accordance with the above-mentioned analysis. The switches in the DAC are designed with minimum size to reduce charge injection, yet to increase on-conductance and minimize non-linearities, they are activated by the charge pump supply, V_{DDH} (Fig. 1), for a $3\times$ improvement in R_{OFF}/R_{ON} .

To further minimize power at low sampling rates, the ADC is primarily implemented with long-length and high- V_t transistors, and is asynchronously controlled. Specifically, despite requiring a sampling rate of only 10 S/s, the ADC runs instantaneously during bit cycling at a clock rate of 1 MHz. After bit cycling is complete the ADC is clock-gated and placed into a low-power sleep state until the next 10 Hz sample clock edge. The 1 MHz clock is generated by the asynchronous unit as the

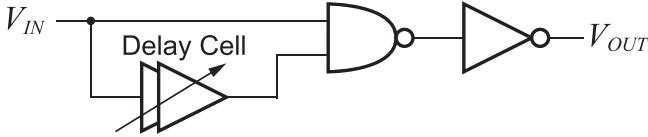


Fig. 7. Schematic of the pulse shaper logic with tunable delay.

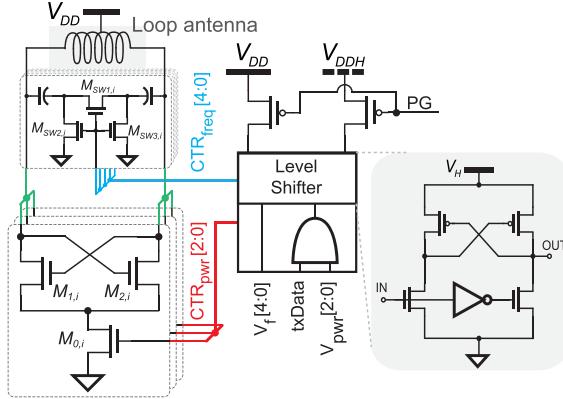


Fig. 8. Schematics of direct-RF power oscillator transmitter.

SAR logic ripples through the 10 controlling slices [18]. The 10 Hz sampling clock is generated by a low-power capacitive-discharging on-chip oscillator (“osc1” in Fig. 1) [19], whose power consumption is 140 pW when operating at 10 Hz. To the best of our knowledge, no prior-art SAR ADCs achieve sub-nW power levels at 10s of samples per second when including all biasing, clocking, and other necessary peripheral circuits; prior-art that does report sub-nW power of the ADC core (e.g., [20] which consumes 650 pW at 50 S/s) does not include the power of such peripheral circuits.

Since the transmitter is active during a logic “1,” and as described as follows the TX active power dominates system power budget, the 10-bit ADC output is serialized and passed through pulse-shaping logic to reduce the pulselwidth for a logic “1.” The delay cell in the conventional pulse shaper shown in Fig. 7 to minimize the active time of the TX, thus saving TX power overhead.

C. Implementation of the 2.4-GHz RF Transmitter

The 2.4 GHz TX utilizes a direct-RF power oscillator architecture, shown in Fig. 8, using an on-board 2.8 mm diameter loop antenna as both a radiative and resonant element. Such direct-RF power oscillator structures provide inherent impedance matching to loop antennas and can be readily gated down to very low leakage power levels [21].

In this design, a center tap in the loop antenna is connected to V_{DD} , which provides power to the negative resistance generator. Conventionally, negative resistance is achieved via a cross-coupled pair with a tail current source, whose current can be controlled via a binary-weighted current-mirror approach. Current control is useful to control oscillation amplitude, and therefore the amount of radiated power. However, the operation of a current-mirror transistor requires

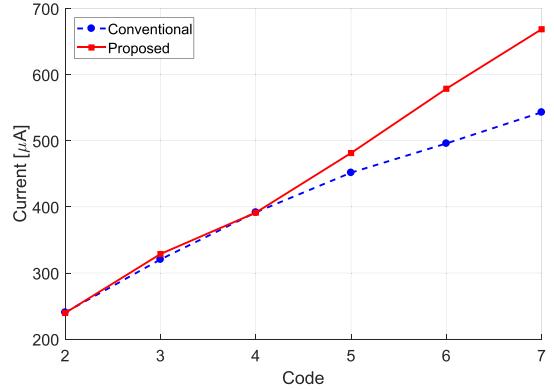


Fig. 9. Simulated current tuning ability of the proposed (triode-mode) and conventional (saturation-mode) tail devices in an RF power oscillator.

$V_{DS} > V_{sat,sub-Vt} \approx 100$ mV in subthreshold to maintain operation in saturation. This V_{DS} requirement degrades the gate-to-source voltage headroom of the cross-coupled transistors. When more tail current transistors are turned ON to increase current, the gate-to-source voltage of the cross-coupled transistors need to be increased accordingly, which is difficult under a fixed supply. At a low supply voltage (e.g., 0.6 V in this design), the increased gate-to-source voltage squeezes V_{DS} of the tail current transistor and therefore degrades the effects of current tuning due to the channel length modulation.

In the proposed design, the tail current sources in [21] are replaced with three triode-mode switches and each of them controls a pair of binary-weighted cross-coupled devices. By turning ON and OFF the switch transistors, different weight cross-coupled devices are activated, thus controlling the value of current injected into the LC tank. Since the switch transistors are completed turned ON and OFF, $V_{DS,M0,i}$ is near zero when it is ON. Therefore, the gate-to-source voltage of the cross-coupled pair is maximized, eliminating the conflict between $V_{DS,M0,i}$ and $V_{GS,M1(\text{or } 2),i}$ when increasing the current. The current tuning range of the TX is thereby increased by 41%, as shown in Fig. 9.

Increasing the number of the cross-coupled pairs will provide better control ability and higher resolution, but the leakage current will also increase proportionally. As the TX is deeply duty-cycled, the standby power matters here. Since three pairs can fulfill the requirements in this application, the number of controlling bits is set to be three to achieve a good tradeoff between tuning ability and standby power.

While the TX in this design is ON-OFF keying (OOK) modulated by turning a fixed number of tail switches completely ON and OFF, the improved linearity of the triode-mode switches may be useful in the future designs that employ amplitude-modulated signals. The triode-mode switches also decrease the transistor size and parasitic capacitance by 84% by maximizing the gate-source voltage V_{GS} of the cross-coupled devices. For the same radiation frequency, the reduced parasitic capacitance permits a larger antenna (0.3 mm larger in diameter) and therefore increases the radiation efficiency (by 16.6% from simulation) and transmitter output power. To further minimize the parasitic capacitance introduced by the

cross-coupled devices, $M_{1,i}$ and $M_{2,i}$ are implemented with low- V_t devices so that they can conduct the same current with $20\times$ less size than the high- V_t devices. On the other hand, $M_{0,i}$ does not have a size limitation, and is thus implemented with high- V_t transistors, which, when sized up for the equivalent on-conduction of a thin-oxide low- V_t transistor, achieves $100\times$ lower leakage current in the OFF mode.

The center frequency of the TX is controlled by the value of inductance and capacitance. The capacitor is implemented using a 5-bit binary-weighted array of digitally activated MIM capacitors, totaling 590 fF, and the inductor is implemented using a single-turn circular loop of copper on the board, which are both fairly temperature insensitive. The parasitic capacitance of the transistor may vary by a small amount with temperature, however, which is negligible compared with the 590 fF MIM capacitor. The relatively stable environment temperature of the application (wearable devices) of this design further ensures the frequency stability. To reduce the on-resistance of the digital switches and minimize the impact on the quality factor of the antenna, level shifters operating from V_{DDH} are used to drive the differential switches that connected to the capacitors.

The TX is deeply duty-cycled, and activated once every 100 ms, transmitting at an instantaneous data rate of 4 Mb/s. Between transmissions, the TX is set to an ultra-low-power sleep state by gating the tail transistors and power gating the control signals and level shifters, the latter of which reduces leakage power by $4\times$.

D. On-Board Antenna Design

The power oscillator's loop antenna was implemented as a single-turn circular loop of 1 oz (i.e., 35 μm thick) copper on an FR-4 substrate. In many cases, antennas for small portable electronic devices are electrically small, and their radiation efficiency increases with the physical size of the antenna [22]. Generally, the largest antenna permissible under application-driven size constraints is chosen. In the present application, the antenna should be made to be no larger than the size of a $\sim 3\text{--}5$ mm coin cell battery. In addition, η_{rad} of electrically small antennas increases with frequency, and thus the antenna should support a self-resonant frequency as high as possible, though in close proximity to an industrial, scientific, and medical (ISM) band (e.g., 2.4 GHz).

Fig. 10(a) illustrates simulated η_{rad} of a circular coil with a trace width of 0.4 mm and a diameter of 2.8 mm, when this antenna is connected to the power oscillator via two 4 mm bonding wires and the parasitics of a 9×9 mm² QFN package. Here, it can be seen that operating at higher frequencies offers improved η_{rad} . However, the power oscillator requires the antenna to look inductive, and thus it is forbidden to choose the carrier frequency beyond the self-resonant frequency [8 GHz in Fig. 10(a)]. In addition, the parasitic capacitance of the bonding pads and electrostatic discharge diodes restricts the maximum resonant frequency since it decides the minimum resonant-tuning capacitance. Based on the layout-extracted parasitic capacitance (150 fF), a maximum resonant frequency of 3.8 GHz is achieved, as shown in Fig. 10(a),

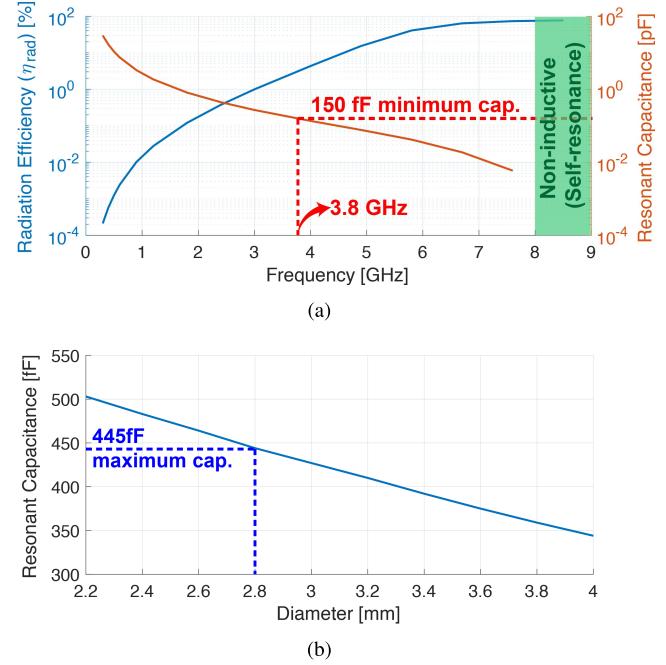


Fig. 10. Antenna optimization. (a) η_{rad} and the required capacitance for resonance of a 2.8 mm diameter TX antenna with two 4 mm bond wires. (b) Required resonant capacitance for different size of antennas connected with minimum-estimated parasitic inductance (6.3 nH from two 4 mm bond wires).

which offers sufficient margin to safely operate in the 2.4 GHz ISM band. If the size of the antenna were increased to afford increased η_{rad} , the resulting required resonant capacitance would decrease, as shown in Fig. 10(b). This helps set a bound on the maximum tolerable tuning capacitance for the present size, and a guideline for how much tuning capacitance would be needed if future designs were to use a slightly larger antenna size.

Note that while an on-chip antenna could have provided a fully integrated solution [23], on-chip antennas tend to suffer from: 1) low radiation efficiency, η_{rad} , due to the limited dimension, thus usually requiring operation at high frequencies (e.g., >10 GHz) which is not suitable for low-power applications and 2) larger capacitors to tune an on-chip antenna which will occupy a large core area and make it difficult to control the resonance at a fine step. On the other hand, in the proposed application the form factor of the overall system is determined by the source device, for example, a battery. Therefore, an on-board antenna can achieve higher η_{rad} and provides more design flexibility, and is thus employed here.

E. Implementation of the Power Management Unit

The overall system is powered by a 1.8 V battery, which is converted to 0.6 V via a 3:1 switched-capacitor dc–dc converter. Since the switching frequency is low (10 Hz) and load power is only a few nW, careful consideration must be taken to minimize the leakage power. Amongst possible switched-capacitor dc–dc converter topologies, the Dickson topology can achieve $6.3\times$ and $1.8\times$ lower leakage power

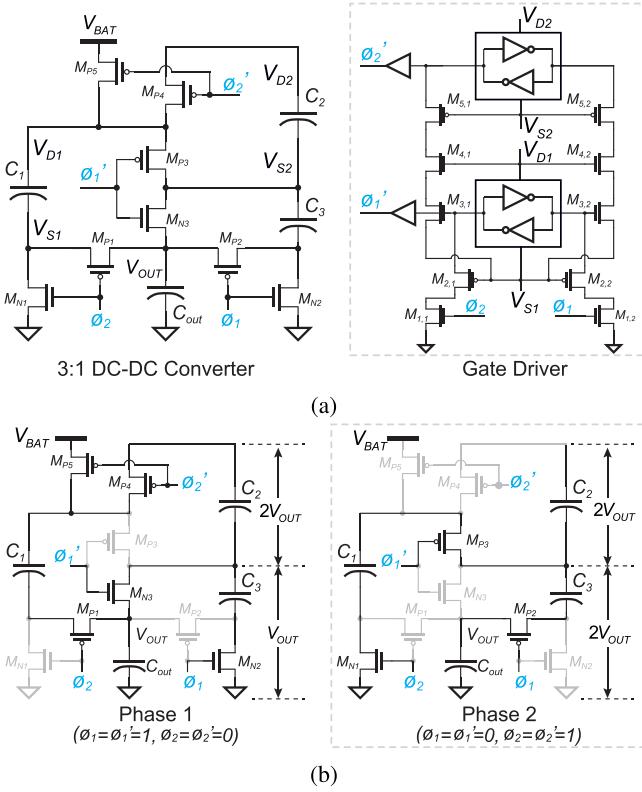


Fig. 11. nW power switched-capacitor dc-dc converter. (a) Architecture and gate driver. (b) Connection during phase 1 ($\phi_1 = \phi'_1 = 1, \phi_2 = \phi'_2 = 0$) and phase 2 ($\phi_1 = \phi'_1 = 0$ and $\phi_2 = \phi'_2 = 1$).

than the Ladder and Fibonacci topologies when configured for a similar ratio and with the same on resistance. In addition, the Dickson topology has low short-circuit current and good slow-switching limit (SSL) performance metrics [24], and is thus chosen for this design. The implemented converter is shown in Fig. 11 along with its gate driver and states during its two phases of operation. The employed power switches are implemented using thin-oxide standard-\$V_t\$ transistors, which for the same on-resistance, offer 19× lower leakage than low-\$V_t\$ devices. Off-chip ceramic capacitors (each 1 μF and 1 × 0.5 mm²) are employed to support the large instantaneous current draws from the TX, while also enabling a low SSL impedance during continuous operation. To ensure proper operation, the main ESD supply voltage is connected to the battery voltage. In addition, multiple diodes are stacked to prevent breakdown and reduce the leakage and turn-on current.

At steady state, the three flying capacitors divide the supply voltage into several voltage domains. To reduce leakage power and the risk of breakdown, the circuit is driven by cascode level shifters, which are powered from the local power capacitor connected to the relevant switch in each voltage domain. For example, the terminals across capacitor \$C_1\$ provide the power rails for the driver to switch transistors \$M_{N3}\$ and \$M_{P3}\$. To do so, clock signals \$\phi_2\$ and \$\phi_1\$, which are referenced between GND and 0.6 V, drive NMOS transistors \$M_{1,1}\$ and \$M_{1,2}\$ in the gate driver, respectively, which generate two pull-down signals connected to the sources of \$M_{2,1}\$ and \$M_{2,2}\$, which toggle the latch formed by a pair of cross-coupled

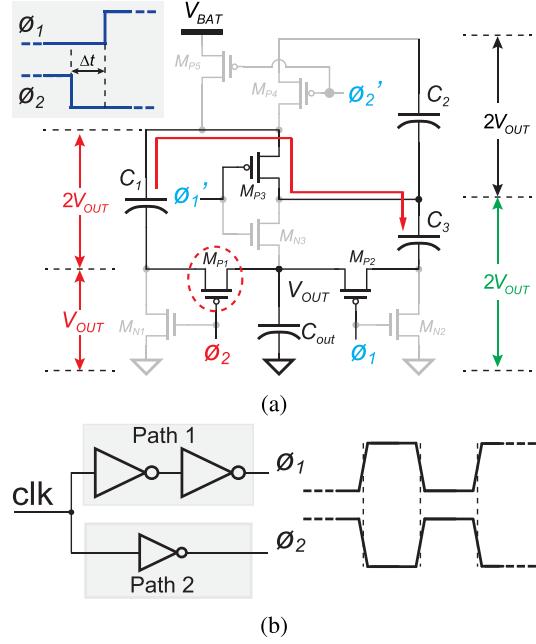


Fig. 12. (a) Power dissipation introduced by the delay of ϕ_1 and ϕ_2 . (b) Circuit to generate the aligned ϕ_1 and ϕ_2 .

inverters to either the ON or OFF position. The output of the latch is then buffered and then used to drive \$M_{N3}\$ and \$M_{P3}\$ (signal \$\phi'_1\$). Similarly, NMOS transistors \$M_{3,1}\$ and \$M_{3,2}\$ in the gate driver reproduce these signals to drive the level shifter above them, whose voltage is generated via the rails of capacitor \$C_2\$, and used to drive \$M_{P4}\$ (signal \$\phi'_2\$). Since \$C_1\$ and \$C_2\$ provide a two times larger voltage to the driver than \$C_{out}\$, transistors \$M_{N3}\$ and \$M_{P3-5}\$ are sized accordingly smaller to reduce parasitic capacitance and leakage power.

During switching, delay of the two differential clock signals can introduce unnecessary short-circuit power dissipation. For example, if \$\phi_2\$ switches from “1” to “0” earlier than \$\phi_1\$ at the end of phase 2 (when \$\phi_1 = 0\$ and \$\phi_2 = 1\$), as illustrated in Fig. 12(a), \$M_{P1}\$ would turn on and cascade \$C_1\$ and \$C_{out}\$, generating a voltage of \$3V_{OUT}\$ at the top plate of \$C_1\$. Since \$M_{P3}\$ would still be on in this situation, the voltage difference between the top plate of \$C_1\$ and \$C_3\$ generates a short-circuit current. Simulations of a baseline design without short-circuit current optimizations reveals a short-circuit power can be larger than the rest of the dc-dc converter’s power. To minimize short-circuit current, the circuit in Fig. 12(b) is used to generate differential aligned clock signal to drive the switched-capacitor circuit. Faster inverters with even numbers are used in path 1 and slow inverters with odd number are used in path 2 to keep the delay the same while generating the differential clock signal. In this manner, quiescent power is reduced by at least 21%.

III. MEASUREMENT RESULTS

The wireless ion sensing chip was implemented in a 1 mm × 1.2 mm 65 nm CMOS chip, and was packaged and soldered to an FR-4 substrate PCB with a 2.8 mm on-board loop antenna. For testing and debugging purposes, a 9 × 9 mm² QFN package

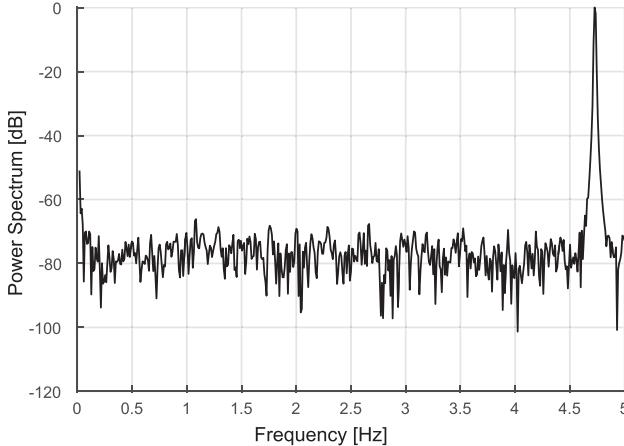


Fig. 13. Measured 128-time averaged 1024-bin FFT plot of the charge-sharing ADC.

was employed. In a future design iteration, many of the chip pads could be left unconnected, and a chip-on-board bonding strategy would significantly reduce the occupied chip footprint. Small diameter batteries (e.g., down to 4.8 mm) could also be used to provide power in a very small form factor. During testing, the dc–dc converter provided a 0.6 V supply to all load circuits.

A. Benchtop Measurements

Measurement results show the potentiometric amplifier consumed 406 pW when operating from a 0.6 V supply. This includes the power required to drive the capacitors in the SAR ADC. At 10 S/s, the reference-free SAR ADC was measured to consume 780 pW, including the power of the 4.2 pW charge pump (Fig. 1), which, to the best of our knowledge, is the lowest power 10-bit 10 S/s ADC with all peripheral circuits integrated. The measured input referred noise of the comparator was 350 μ V. Since different spectrum tests were required to characterize the performance of the ADC in a different environment while the ADC was operating at very low frequency (down to a few Hz), to accelerate the measurement a 1024-point fast fourier transform (FFT) was calculated. However, since the frequency band of interest was only 0–5 Hz, a 1024-bin FFT provided a frequency resolution better than 0.005 Hz, which is good enough for the purpose of benchmarking the ADC effective number of bits (ENOB). To achieve an accurate noise floor measurement, as shown in Fig. 13, a 128-times averaged 1024-point FFT with Hanning windowing was performed, and an ENOB of 8.3 bits was measured (ENOB degradation was mainly introduced by comparator noise and DAC parasitics), for an energy efficiency of 244 fJ/conv-step. At such a low sampling frequency, measured efficiency was dominated by leakage power. Fig. 14(a) shows the measured figure-of-merit (FoM) at different sampling frequencies. At 1 kS/s, the ADC power was 2.4 nW and the measured ENOB was 8.31 bits, resulting in an efficiency of 7.6 fJ/conv-step, further illustrating the leakage dominance at low sampling rates. When operating from 0.6 to 0.8 V with a sampling rate

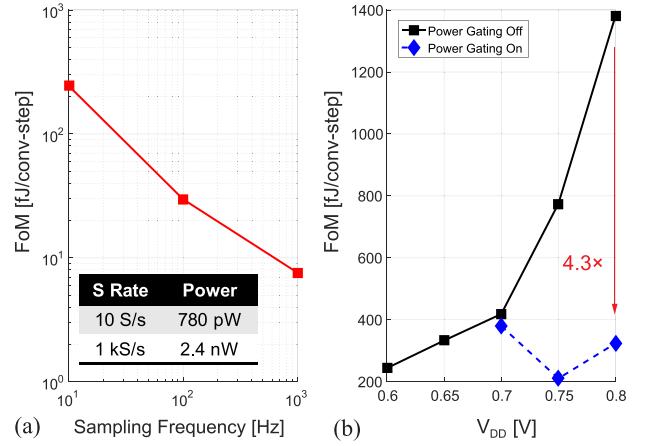


Fig. 14. Measured FoM of the ADC (a) when operating at a different sampling frequency and (b) when operating from different supply voltages at 10 S/s, achieving an FoM better than 379 fJ/conv-step.

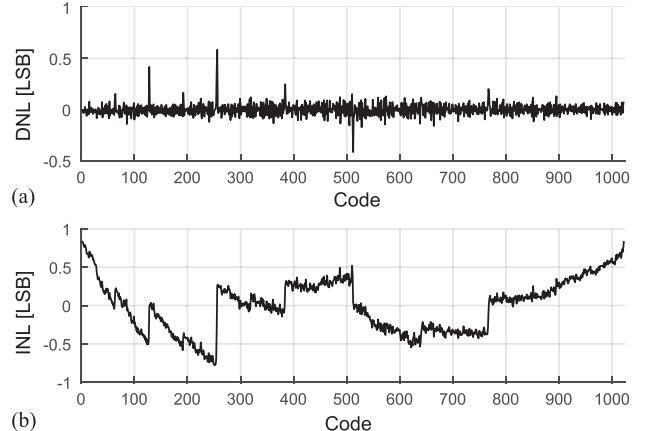


Fig. 15. Measured (a) DNL and (b) and INL of the reference-free charge-sharing ADC.

of 10 S/s, the measured FoM varied from 244 fJ/conv-step at 0.6 V to 1381.2 fJ/conv-step at 0.8 V without power gating, as shown in Fig. 14(b). Power gating, which could be enabled when $V_{DD} > 0.7$ V, improved the FoM significantly (e.g., 4.3 \times at 0.8 V) by reducing leakage in the sleep mode, and ensured an FoM better than 379 fJ/conv-step across the supply ranges from 0.6 to 0.8 V. The measured DNL and INL were $-0.36/0.58$ and $-0.77/0.84$ LSB, respectively, as shown in Fig. 15.

At 1 m distance, the TX radiated -64.6 dBm of power as measured by a $\lambda/4$ whip antenna. Fig. 16(a) shows the measured output spectrum measured at ~ 10 cm with a $\lambda/4$ whip antenna when operating with 4 Mb/s OOK modulation. When transiently powered by C_{out} , a 1μ F 1×0.5 mm 2 capacitor, the TX consumed 154.5μ W of instantaneous power, corresponding to a bias current of 257μ A, set by the default power control code “010.” The startup time of the TX was measured to be <52 ns, as shown in Fig. 16(b). The measured sleep-mode power of the TX was 500 pW, thus achieving an average power of 2.4 nW after duty-cycling to 100 b/s (i.e., 10 S/s).

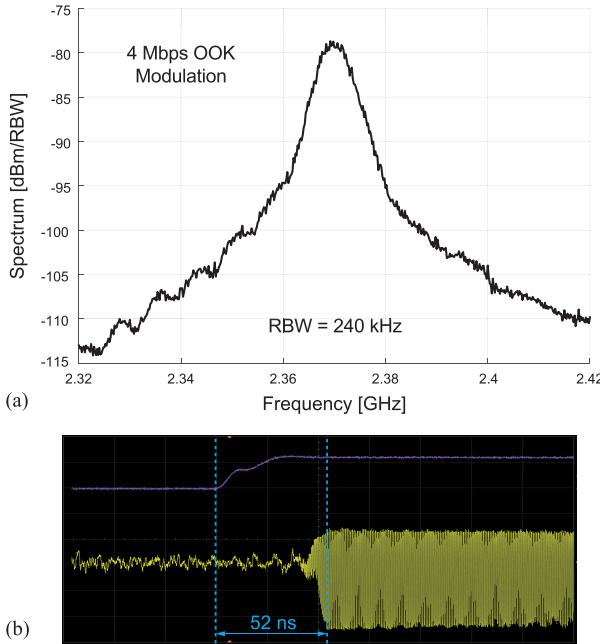


Fig. 16. (a) Spectrum measured using a $\lambda/4$ whip antenna placed ~ 10 cm from the on-board loop antenna with 4-Mbps OOK modulation. (b) Measured TX startup time.

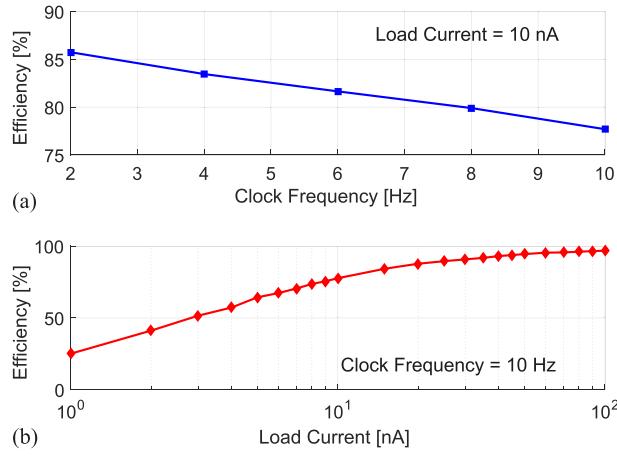


Fig. 17. Measured efficiency of the dc-dc converter versus (a) clock frequency and (b) load current.

Clocked by the reference-free relaxation oscillator, the switched-capacitor dc-dc converter operated between 2–10 Hz. The measured efficiency of the dc-dc converter at different frequencies with 10 nA load current is shown in Fig. 17(a), while Fig. 17(b) shows measured efficiency with a different load current when operating at 10 Hz. As shown in Fig. 17(b), the dc-dc converter achieved a peak efficiency of 96.8% when operating with a load current of 100 nA.

Table I shows the power breakdown of the whole ion sensing system. Together, all of the load circuits in the wireless ion sensing system consumed 3.9 nW. At this load, the dc-dc converter achieved an efficiency of 70.5%, for a total system power consumption of 5.5 nW.

TABLE I
POWER BREAKDOWN OF THE ION SENSING SYSTEM (DEFAULT IN pW)

AFE	Buffer	ADC	Timer	TX	DC-DC Eff.	Total
406	15×2	780	140×2	2.4 nW	70.5%	5.5 nW

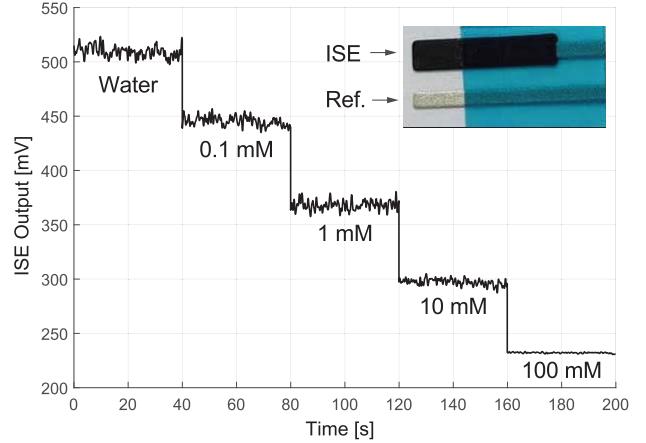


Fig. 18. *In vitro* ion concentration measurements with Na^+ -selective electrode.

B. In Vitro Tests

The ion sensing system was measured *in vitro* with 0.1–100 mM NaCl concentration with the SPI configured to the default tuning set. The Ag/AgCl RE, consisting of a polymeric PVB membrane, was biased by the ladder-based reference generator at 500 mV to provide a stable, midsupply solution potential for the ISE output recording (Fig. 18). The ADC was configured as pseudo-differential structure: the input V_N in Fig. 4, was connected to the output of potentiometric amplifier while V_P was biased through a voltage buffer [Fig. 2(b)] at midsupply, resulting in a 0.7 LSB DNL degradation. The charge-sharing ADC, when operating at 10 S/s, required an input switching power less than 16 pW ($\sim 2\%$ of the total ADC power), which was well within the sourcing capability of the potentiometric amplifier and thus takes no extra power in the signal driver. In addition, an on-board ceramic capacitor was utilized after the potentiometric amplifier to minimize the large instant current spikes that might occur during sampling. The *in vitro* test was performed by first using pure water as background, giving ~ 510 mV output as shown in Fig. 18. Samples with different NaCl concentrations were then dropped onto the electrode and recorded for approximately 40 s before additional solution was added. Note that the variation on the reference voltage shows as a common-mode voltage and thus can be rejected. On the other hand, the systematic error will affect the reference voltage for digitization in ADC and therefore effectively introduces an ADC offset error which, however, does not matter in the proposed application since, for example, as shown in Fig. 18, the offset error will only effectively shift the y-axis, which can be calibrated out during normal system operation. The *in vitro* measurements shown in Fig. 18 exhibit a linear, near-Nernstian response with a response slope of $71 \text{ mV}/\log_{10}[\text{Na}^+]$, as better

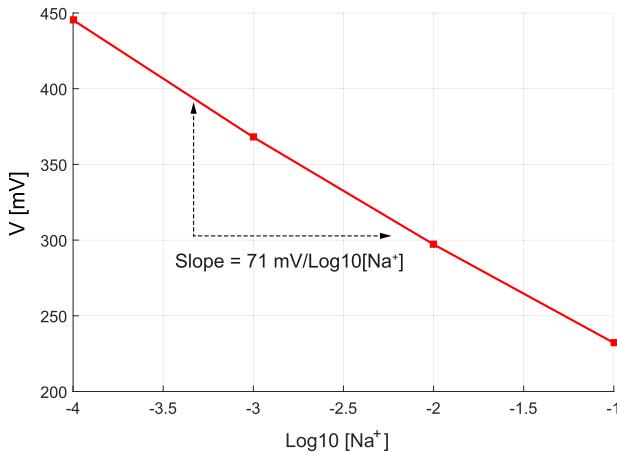


Fig. 19. *In vitro* measurements demonstrate that the wireless sensing platform achieves a linear response to the ion concentration.

Technology	65 nm CMOS
Chip area	1 mm × 1.2 mm
TX frequency	2.37 GHz
TX output power	-64.6 dBm @ 1 m
TX start-up time	52 ns
ADC ENOB	8.3 bits
ADC FOM	244 fJ/conv @ 10 S/s 7.7 fJ/conv @ 1 kS/s
SC DC-DC eff.	96.8% @ 100 nA 70.5% @ 6.5 nA

Power consumption [pW]	
Pot. Amp.	406
ADC	780 @ 10 S/s
TX	500 (standby) 154 μW (active) 2.4 nW (average @ 100 bps)
Oscillator	140 @ 10 Hz

Fig. 20. Tables summarizing chip measurement results.

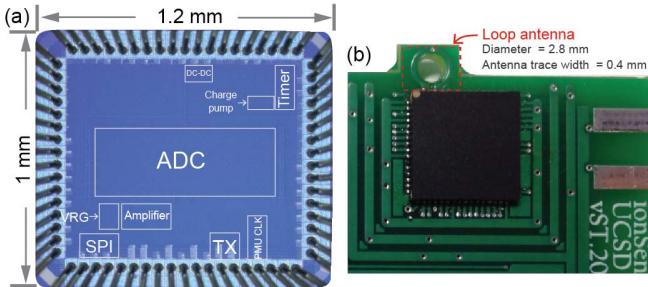


Fig. 21. (a) Die photograph of the proposed ion sensing chip. (b) PCB photograph.

shown in Fig. 19, thereby indicating the ability of the proposed system to accurately detect and wireless transmit ion concentration with only 5.5 nW of power. Note that the proposed ion sensing system can be adapted to measure other ions such as potassium, chloride, and so on, by using different ionophores. A table summarizing system performance is shown in Fig. 20, and the die and PCB photographs are shown in Fig. 21.

IV. CONCLUSION

An ultra-low-power battery-connected wireless ion sensing system has been presented in this paper. The platform comprises ISEs, a potentiometric amplifier, a reference-free charge-sharing SAR ADC with offset-attenuation, a digital processing unit including a serializer and a pulse shaper, a 3:1 Dickson switched-capacitor dc–dc converter, a direct-RF

power oscillator employing triode-mode switches, and low-power relaxation oscillators for clock generation. Measurements reveal a total system power consumption of 5.5 nW, resulting in the lowest power wireless ion sensing system to date. *In vitro* testing shows a near-Nernstian response to varying Na^+ concentrations, indicating the ability of the proposed system to accurately detect and wireless transmit ion concentration at near-zero power levels.

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