

# A 4.2-mW 10-MHz BW 74.4-dB SNDR Continuous-Time Delta-Sigma Modulator With SAR-Assisted Digital-Domain Noise Coupling

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**Abstract**—This paper introduces a high-order continuous-time (CT) delta-sigma modulator (DSM) that applies digital-domain noise coupling (DNC) based on the structural advantages of the successive-approximation register (SAR) analog-to-digital converter (ADC), which makes the implementation of second-order noise coupling very simple. Due to digital-domain implementation as well as the SAR ADC where the key building blocks are embedded for the proposed DNC, compact size and efficient power consumption could be designed. For low circuit noise, a feedback DAC is implemented with a tri-level current-steering DAC. Tri-level data-weight averaging (TDWA) improves the linearity of the DAC. With the proposed DNC and TDWA, a prototype CT DSM fabricated in a 28-nm CMOS achieves a peak 74.4-dB SNDR and an 80.8-dB dynamic range (DR) for a 10-MHz BW with an oversampling ratio of 16, resulting in a Schreier FoM<sub>DR</sub> of 174.5 dB. The chip area occupies 0.1 mm<sup>2</sup>, and the power consumption is 4.2 mW.

**Index Terms**—Analog-to-digital converter (ADC), continuous-time delta-sigma modulator (CT DSM), digital-domain noise coupling (DNC), noise coupling, successive-approximation register (SAR), tri-level data-weight averaging (TDWA).

## I. INTRODUCTION

IN WIRELESS communication systems, continuous-time (CT) delta-sigma modulators (DSMs) are widely used in the receiver chain due to their various advantages such as a relaxed opamp requirement and an inherent anti-aliasing characteristic. As higher dynamic range (DR) and low oversampling ratio (OSR) are preferred for CT DSMs for high sensitivity of the receiver, the design becomes difficult because the stability must be guaranteed even for a high-order loop filter and/or high linearity is required for a multi-bit feedback (FB) DAC in the case of employing a multi-bit quantizer.

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While the stability of a single-loop structure is somewhat inferior to that of other structures, the multi-stage noise shaping (MASH) structure [1], [2] shows good loop stability since the internal FB loops consist of lower order loop filters. On the other hand, the mismatch between the analog and digital transfer functions in the MASH structure limits the performance. Alternatively, sturdy MASH (SMASH) has the advantage of eliminating the digital filter in the MASH structure, but in the case of CT implementation for the SMASH structure, an absolute *RC* time constant-based delay design is required for an extraction of the quantization error from the main loop, resulting in increasing design complexity [3].

Recently, noise coupling structures have attracted designers' attention in that they can reduce the complexity of the loop filter [4], [5]. However, an additional noise coupling filter implemented in the analog domain with active components becomes additional overhead, specifically, hardware complexity, power consumption, and process-voltage-temperature (PVT) sensitivity.

In order to reduce the design burden of the previous analog-domain noise coupling (ANC), in this paper, a digital-domain noise coupling (DNC) structure is proposed to implement the noise coupling filter in the digital domain [6]. This allows the realization of a very simple second-order noise coupling filter and eliminates the power-consuming opamps. In addition, the building blocks required for implementing the proposed DNC structure can be implemented hardware efficiently by utilizing the structural advantages of the successive-approximation register (SAR) analog-to-digital converter (ADC).

The rest of this paper is organized as follows. Section II discusses the proposed DNC structure in comparison with the ANC structure. Section III then describes the detailed circuit implementation utilizing an SAR ADC as a quantizer. The measurement results of the prototype modulator are presented in Section IV followed by conclusions in Section V.

## II. NOISE COUPLING STRUCTURE

### A. Previous Analog-Domain Noise Coupling

Signal processing for noise coupling in DSMs, as well as in a noise shaping SAR ADC, reported to date has been implemented in the analog domain, including noise coupling filters [5], [7]. In addition, a self-coupling technique has

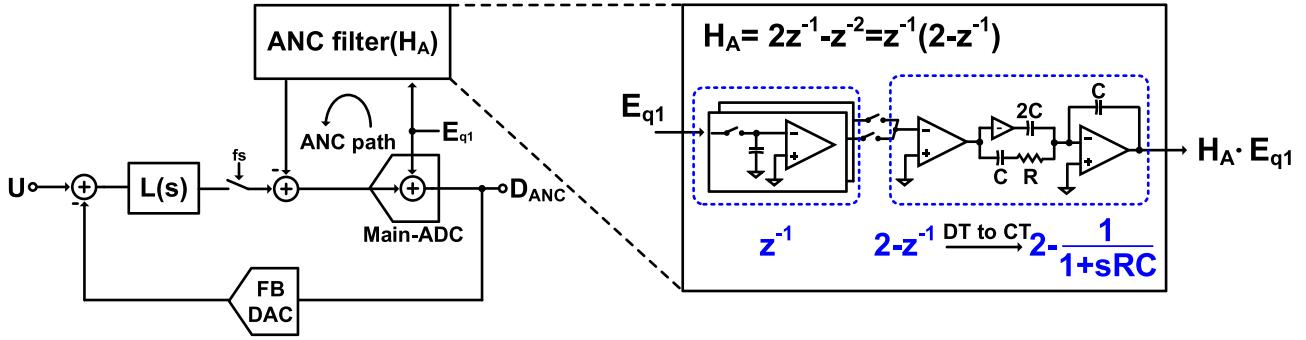


Fig. 1. Block diagram of ANC structure with the detailed second-order ANC filter.

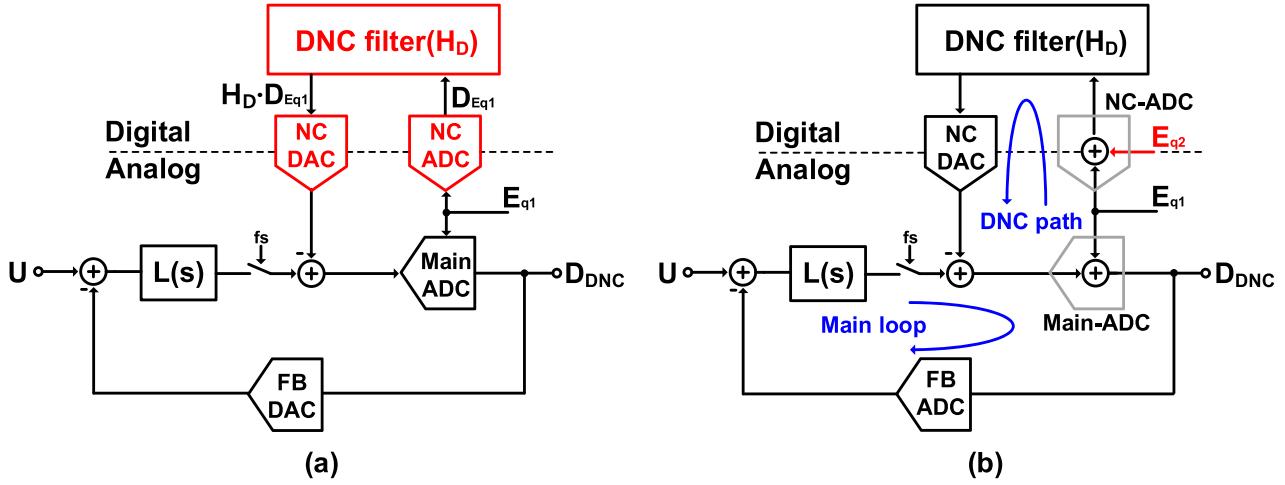


Fig. 2. Proposed DNC. (a) Block diagram. (b) Linearized model with quantization errors.

been proposed to improve noise shaping characteristic with no extra opamp [23], but the structure could only achieve additional first noise shaping. Fig. 1 shows a block diagram of a CT DSM employing ANC. The quantization error generated by the main-ADC,  $E_{q1}$ , is filtered by an ANC filter,  $H_A$ , and subtracted from the next input. The output of the noise coupling modulator is derived as

$$D_{ANC} = STF \cdot U + NTF \cdot (1 - H_A) \cdot E_{q1} \quad (1)$$

where signal transfer function (STF) is  $L(s)/(1 + L(s))$  and noise transfer function (NTF) is  $1/(1 + L(s))$ . Note that the FB DAC can be modeled with a unity gain. Due to the noise coupling, the quantization error,  $E_{q1}$ , is shaped not only by NTF but also by  $1 - H_A$ , as shown in (1). For example, if  $H_A$  is  $2z^{-1} - z^{-2}$ , then  $1 - H_A$  becomes a second-order high-pass filter, giving an additional second-order noise shaping characteristic to  $E_{q1}$ , aside from NTF. Recently, a second-order ANC structure for CT DSM [5], as shown in Fig. 1, was proposed. In the design, the required discrete-time finite-impulse response filter,  $H_A$ , could be successfully emulated by an opamp-based CT analog filter. Nevertheless, the opamps for filter implementation are another source of power overhead and complexity. In addition, since the  $RC$  values in the analog filter are sensitive to PVT variation, the noise coupling characteristic may vary, especially in poorly controlled processes.

#### B. Proposed Digital-Domain Noise Coupling

The design burden imposed by the ANC filter can be drastically reduced by implementing the noise coupling filter,  $H_A$ , in the digital domain (DNC) since it can easily be implemented with only delays and an adder. Fig. 2(a) presents a conceptual block diagram of the proposed DNC structure. For digital-domain  $H_D$ , the quantization error,  $E_{q1}$ , must be converted into a digital code through an ADC, referred to as a noise coupling ADC (NC-ADC). The digitized  $E_{q1}$ ,  $D_{E_{q1}}$ , is then processed in the digital domain by a DNC filter,  $H_D$ . The filtered  $E_{q1}$  in the digital domain,  $H_D \cdot D_{E_{q1}}$ , is coupled with the next input in the analog domain through an NC-DAC. While the filter complexity of  $H_D$  can be significantly reduced due to the digital-domain implementation, aside from the complexity by NC-ADC and NC-DAC, additional quantization error,  $E_{q2}$ , is generated as depicted in Fig. 2(b). From a linearized model, the output of the proposed DNC architecture can be derived as

$$D_{DNC} = STF \cdot U + NTF \cdot (1 - H_D) \cdot E_{q1} - NTF \cdot H_D \cdot E_{q2}. \quad (2)$$

While  $E_{q1}$  is shaped by both the main loop (NTF) and the DNC path ( $1 - H_D$ ),  $E_{q2}$  is only shaped by the main loop since the frequency response of  $H_D$  is flat at low frequency, which means the quantization noise power of  $E_{q2}$  is likely to

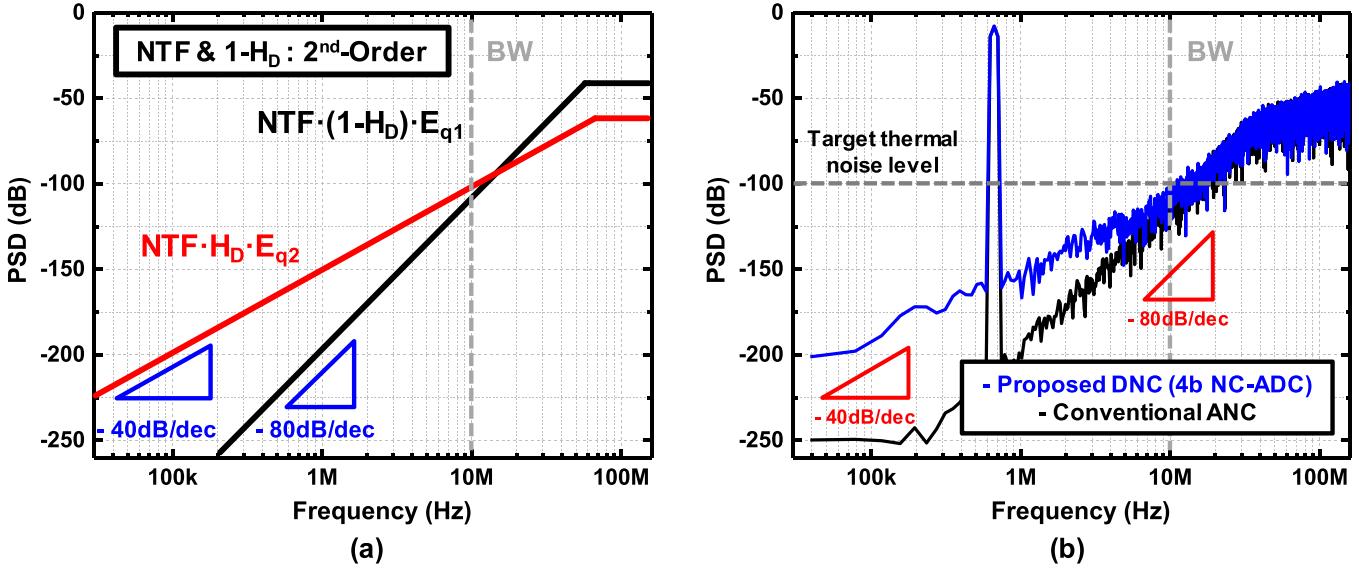


Fig. 3. (a) Frequency-domain characteristic with  $E_{q1}$  and  $E_{q2}$ . (b) Behavioral simulation FFT result with ANC and DNC.

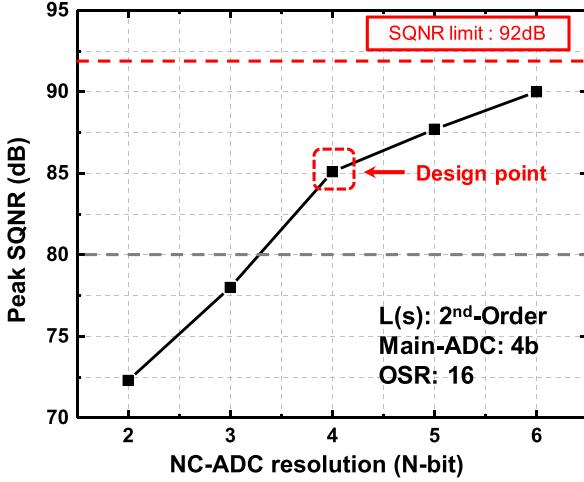


Fig. 4. Peak SQNR according to the resolution of NC-ADC.

limit the performance. However, basically, since  $E_{q2}$  is smaller than  $E_{q1}$  because  $E_{q2}$  is the quantization error of  $E_{q1}$ , the effect of  $E_{q2}$  can be made negligible by properly choosing the resolution of the NC-ADC.

### C. Effect of $E_{q2}$

To discuss the effect of  $E_{q2}$  in greater detail, the frequency domain characteristic with quantization errors is shown in Fig. 3(a). Here, it is assumed that NTF and  $1 - H_D$  are second order.  $E_{q1}$  is, then, filtered by a fourth-order noise shaping characteristic. Unlike the ANC scheme, since  $E_{q2}$  is shaped by  $NTF \cdot H_D$ , the low-frequency characteristic of the noise power spectral density is limited to that of a second-order modulator. The overall frequency response of the shaped noise in the proposed DNC shows two slopes ( $E_{q1}$  and  $E_{q2}$ ) dominated by  $NTF \cdot (1 - H_D)$  in high-frequency region and  $NTF \cdot H_D$  in low-frequency region, respectively. The second-order noise shaping characteristic may limit the SNR performance, but the noise floor limited by  $E_{q2}$  can be

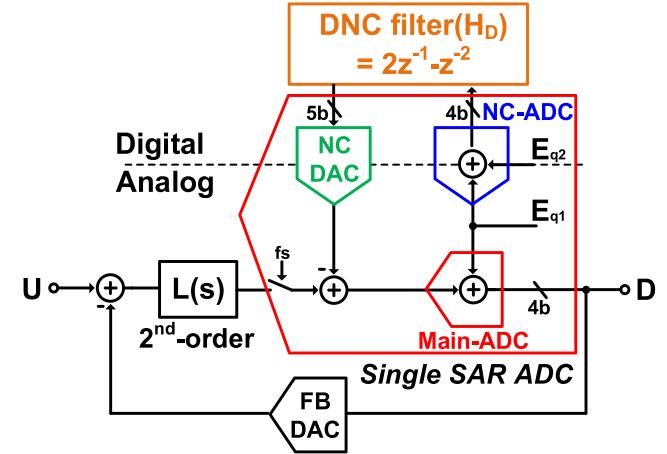


Fig. 5. Block diagram of the proposed modulator with the second-order DNC filter.

pushed down by increasing the resolution of the NC-ADC. Fig. 3(b) shows the behavioral simulation fast Fourier transform (FFT) result of the proposed DNC compared with the ANC scheme. As discussed earlier, the DNC exhibits higher quantization noise level than that of the ANC scheme due to the second-order noise-shaped quantization error,  $E_{q2}$ , in the low-frequency region. Nevertheless, since the entire performance in the signal band is likely to be determined by thermal noise, the shaped noise of the proposed DNC scheme with a 40 dB/dec rolloff in the low-frequency region can have a negligible effect on a certain target SNR, as briefly illustrated with an example of a certain target thermal noise level. Therefore, the proposed DSM architecture can still be applicable for high SNR application with properly chosen NC-ADC resolution.

### D. Design Choices

In order to determine the resolution of the NC-ADC, it is necessary to first determine the specifications of other building blocks. For an SNDR higher than 70 dB, the target

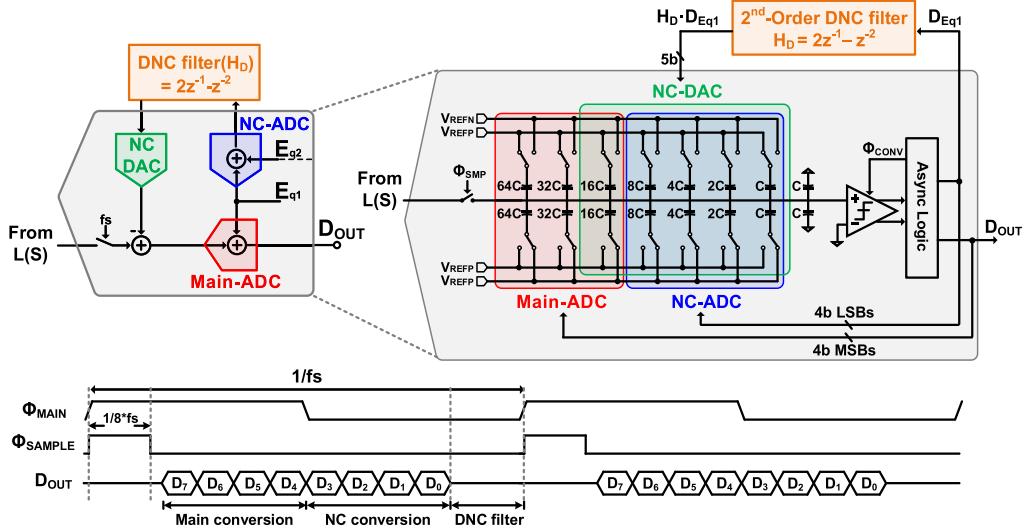


Fig. 6. DNC implementation with 8-bit single SAR ADC.

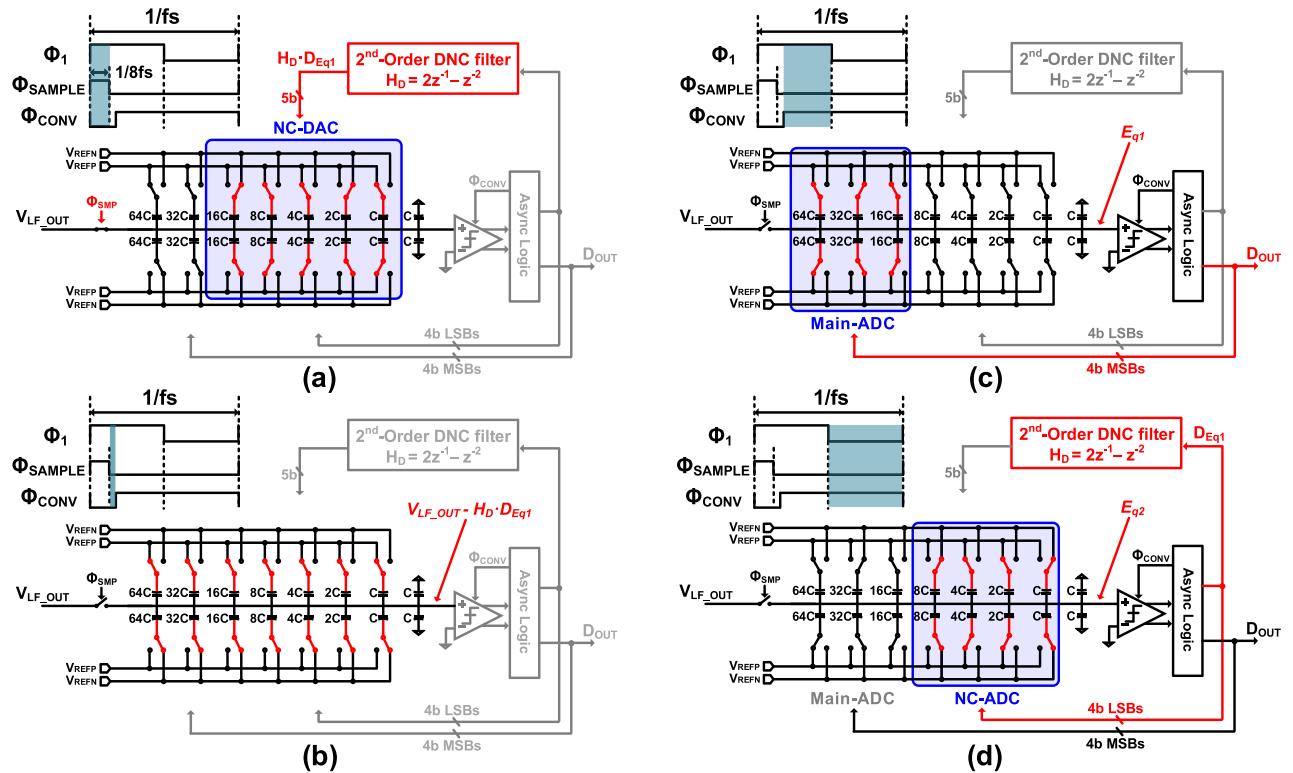


Fig. 7. SAR operation for noise coupling. (a) Sampling. (b) Subtraction. (c) Main A/D conversion. (d) NC A/D conversion and digital processing (2nd-order DNC filter).

signal-to-quantization-noise ratio (SQNR) was determined to be higher than 80 dB. For clock frequency lower than 500 MHz, the OSR has been chosen to be 16, which leads to a sampling frequency of 320 MHz. In order to reduce the complexity of the loop filter, the DNC filter is determined to be second order, and thus the loop filter is designed to be second order. As a result, fourth-order noise shaping is obtained. Considering the complexity of the FB DAC, the matching requirement, and the data-weight averaging (DWA) complexity, the resolution of the main-ADC is chosen to be 4-bit. Based on these design choices, the required resolution of

the NC-ADC can be determined. Fig. 4 shows the peak SQNR performance according to the resolution of the NC-ADC with the design choices explained earlier. Note that the performance of the proposed architecture will be enhanced as the resolution of the NC-ADC increases, and the performance will eventually converge to that of ANC. The maximum SQNR of the proposed design is 92 dB, and it is noted as the SQNR limit in Fig. 4. It is quite clear that a low-resolution NC-ADC would not satisfy the target SQNR, whereas a high-resolution NC-ADC is likely to increase the design complexity. Since 4 bit is the lowest resolution for the NC-ADC that satisfies

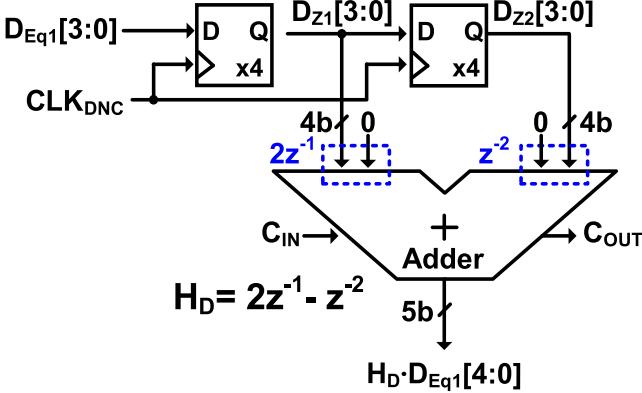


Fig. 8. Implementation of the second-order DNC filter.

the target SQNR of 80 dB, the actual accuracy required for the NC-ADC is 8-bit equivalent considering the 4-bit main-ADC.

### III. CIRCUIT IMPLEMENTATION

#### A. SAR-Assisted Digital-Domain Noise Coupling

The most important advantage of the proposed DNC architecture is that the noise coupling filter can simply be designed in the digital domain. The proposed architecture, however, may appear to be complicated with additional building blocks such as the NC-ADC, NC-DAC, and subtractor. However, it should be noted that these key building blocks can be embedded in a single SAR ADC, as shown in Fig. 5. The details of each building block in the single SAR ADC are presented in Fig. 6. The single SAR ADC is implemented with an 8-bit resolution. The total size of SAR CDAC is 256 C with a 0.7-fF unit capacitor ( $C$ ). This 8-bit SAR ADC can work as a 4-bit main-ADC utilizing 3-bit MSB capacitors (64 C, 32 C, and 16 C). As in [8], MSB decision can be conducted with no capacitor switching owing to the split-capacitor DAC. The remaining 4-bit LSB capacitors are used for the 4-bit NC-ADC to digitize the quantization error,  $E_{q1}$ . In addition, the 5-bit LSB capacitors (16 C, 8 C, 4 C, 2 C, and C) in the ADC are reused for the 5-bit NC-DAC without requiring an extra capacitor. The subtraction for noise coupling can also be implemented by simply utilizing the structural advantage of the SAR ADC. Note that any error induced by the NC-DAC is suppressed by the loop filter. By embedding all the required functions for digital noise coupling in this SAR ADC, a CT DSM with the proposed DNC technique can be implemented in a very hardware-efficient manner.

Fig. 7 explains the detailed operation and circuit configuration in each phase of the proposed SAR-assisted DNC. During the signal tracking at the top node of the capacitor-DAC [Fig. 7(a)], the bottom nodes of the 5-bit LSB capacitors for NC-DAC are connected to the references according to the output of the DNC filter,  $H_D \cdot D_{Eq1}$ . Here,  $D_{Eq1}$  is the digital representation of the quantization error,  $E_{q1}$ . As soon as the input tracking is done, as shown in Fig. 7(b), the 5-bit NC-DAC switches back to the common level, realizing noise coupling by subtraction of  $V_{LF\_OUT} - H_D \cdot D_{Eq1}$ , where  $V_{LF\_OUT}$  is the output of the loop filter. With the noise-coupled

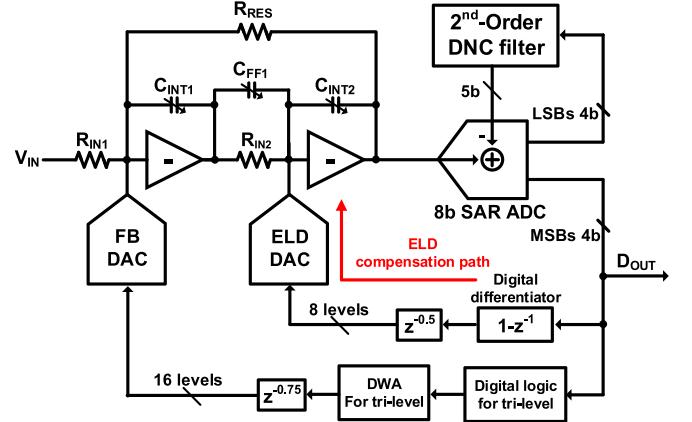


Fig. 9. Overall schematic of the proposed fourth-order CT DSM.

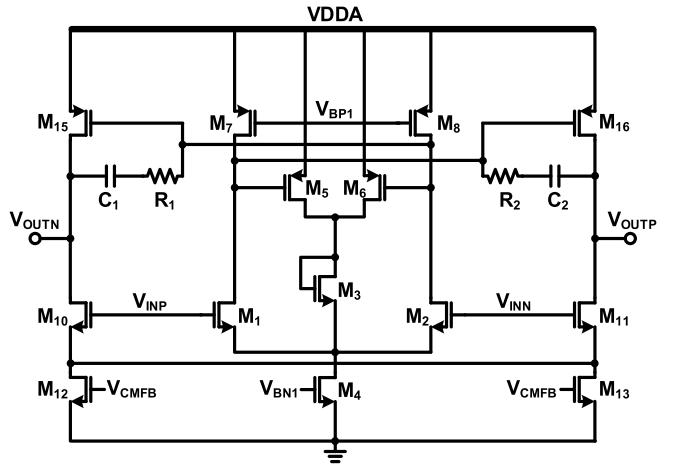


Fig. 10. Hybrid feedforward amplifier for the first integrator.

input, the 4-bit main A/D conversion is performed [Fig. 7(c)] utilizing 3-bit MSB capacitors in a successive-approximation manner. The resulting 4-bit  $D_{OUT}$  is the output of the main-ADC and is given to the FB DAC of the modulator. When the main A/D conversion is done, the quantization error,  $E_{q1}$ , is left at the top node of the capacitor-DAC as a residue. Unlike previous ANC techniques [5], [7], the proposed SAR-assisted DNC scheme does not require  $E_{q1}$  sampling, as  $E_{q1}$  becomes the direct input to the coming NC-ADC. Fig. 7(d) illustrates the following NC-ADC operation. After this fine conversion, the residue voltage at the top node is  $E_{q2}$ , as explained earlier. Note that the consecutive operation of the main-ADC and the NC-ADC is only an 8-bit SAR ADC operation. The resulting 4-bit output from the NC-ADC is  $D_{Eq1}$  and  $D_{Eq1} = E_{q1} + E_{q2}$ . After the entire 8-bit conversion,  $D_{Eq1}$  is transferred to the DNC filter for noise filtering in the digital domain. The result of the DNC filter then goes back to the ADC for noise coupling, as explained earlier. In a real implementation, the SAR ADC works in an asynchronous manner in order to avoid high-speed internal clock generation [9], [10].

Fig. 8 shows the second-order DNC filter implementation in detail. It is implemented in a very compact manner with only registers and one 5-bit adder. Due to the digital-domain

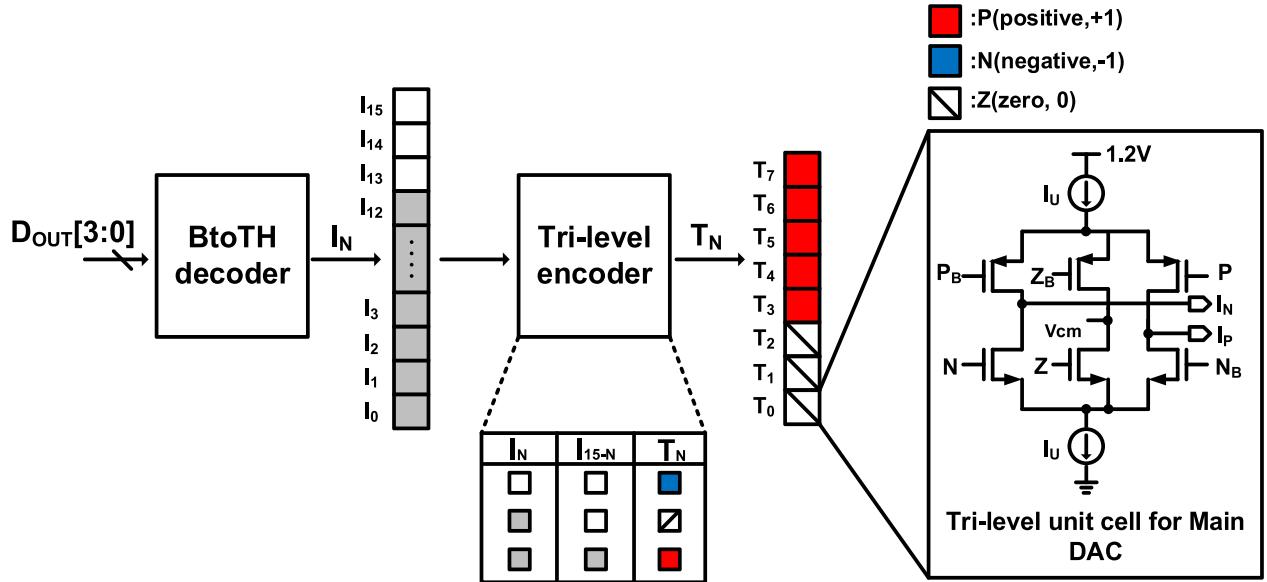


Fig. 11. FB DAC with tri-level coded data.

implementation,  $2z^{-1}$  is implemented simply by one clock delay and 1-bit shift in a 5-bit adder. The output of the adder ( $H_D \cdot D_{Eq1}$ ) directly controls the 5-bit LSB capacitors of the NC-DAC. The carry-in ( $C_{IN}$ ) is set to 1 for the two's complement-based subtraction, and the carry-out ( $C_{OUT}$ ) determines the polarity of the noise coupling.

#### B. Fourth-Order CT DSM With Second-Order DNC Filter

The overall block diagram shown in Fig. 9 is a fourth-order CT DSM with the proposed second-order DNC. The loop filter consists of second-order feedforward topology with capacitive feedforward. The amplifier used in the first integrator is shown in Fig. 10. In general, since the first integrator is the most power-consuming block in the modulator, a hybrid opamp with feedforward and Miller frequency compensation is used for the first integrator to maximize the gain bandwidth [3], [11]. This topology is basically similar to a general two-stage opamp topology, but differs in that the direct input path through  $M_{10}$ ,  $M_{11}$  is added to the output stage for feedforward. The simulated opamp characteristic for the first integrator including the loading effect shows 51 dB of dc gain and 700 MHz of unity-gain bandwidth, respectively. Considering the large output swing range of the last integrator in the loop filter, the second integrator utilizes a conventional two-stage opamp.

In CT DSMs, excess loop delay (ELD) should be taken care of [12]–[14]. Since an ELD DAC signal can be easily injected to the input of the last integrator, a differentiation function is required for ELD DAC. Unlike the previous ELD compensation design utilizing an analog-domain differentiator with two DACs [15], in this design, the ELD compensation is implemented with only one DAC (ELD DAC) owing to the digital-domain differentiator, as shown in Fig. 9. Owing to the oversampling characteristic, the difference between adjacent codes is small, and thus the ELD DAC could be implemented with eight unary cells.

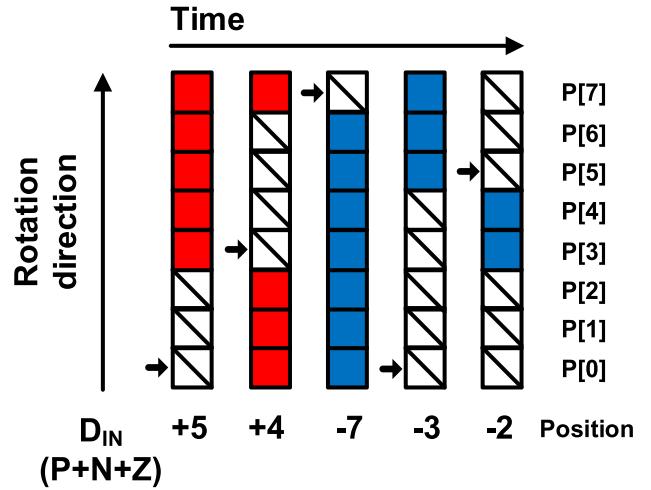


Fig. 12. Switching sequence principle of TDWA.

#### C. Tri-Level Data-Weight Averaging

In this design, the FB DAC is implemented with a current-steering DAC architecture with unit cells having three levels: positive, negative, and zero. As shown in Fig. 11, the 4-bit binary  $D_{OUT}$  from the main-ADC is encoded into tri-level coded data ( $T_N$ ) via thermometer decoding ( $I_N$ ) in order to reduce circuit noise by reducing the number of unit cells of the FB DAC by half [16]. Fig. 11 also shows the unit cell of the tri-level FB DAC. The cell consists of sourcing (PMOS) and sinking (NMOS) current sources with three pairs of NMOS-PMOS switches for tri-level switching. Both the sourcing and sinking current sources are cascoded, and the switching transistors controlled by the signals P, N, and Z operate in the triode region. The current DAC follows a stacked unit cell structure [24], and the current sources are designed for matching of 0.75% standard deviation for 12-bit linearity (when DWA is disabled). For code zero, both the NMOS and

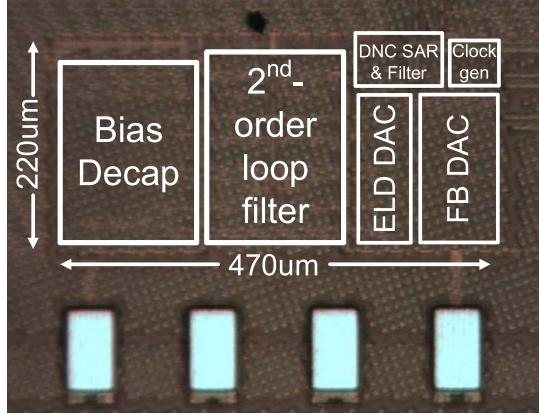


Fig. 13. Die photograph.

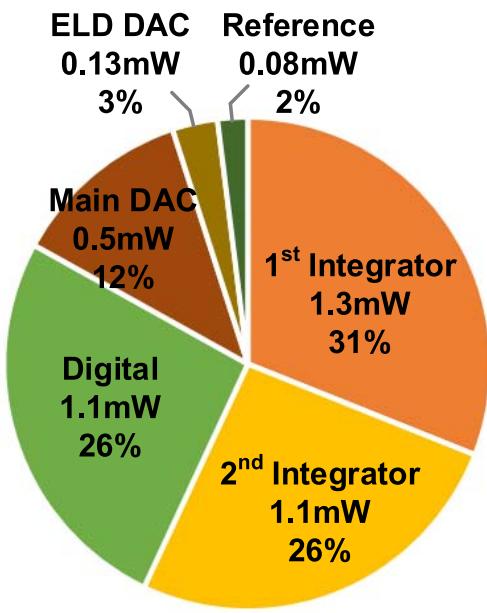


Fig. 14. Power breakdown.

PMOS switches controlled by signal “Z” and “ $Z_B$ ” are ON, making the output current zero. Accordingly, zero-state cells do not contribute to noise and nonlinearity of the FB DAC.

Fig. 12 shows the switching sequence of the proposed tri-level DWA (TDWA). Unlike the conventional bi-level DWA [17], [18] in which the location of the positive (or negative) one is utilized as a pointer, the operation of the proposed TDWA is based on the positions of zero-state cells. Initially, the pointer indicates location P[0]. When  $D_{IN}$  is +5, for example, it is composed of three zeros and five positive ones. Hence, the three zeros are located at P[0]–P[2], and the five ones are filled in the remaining positions. Since the next code is +4 and the location of zeros ended at P[2] in the previous code, the position of zeros begins from P[3] and they are filled up to P[6] with four ones filled thereafter. The following TDWA operation with -7 has one zero at P[7] and the remaining positions are filled with negative ones. By performing this rotational operation, the cell switching sequence is randomized, resulting in improved dynamic linearity.

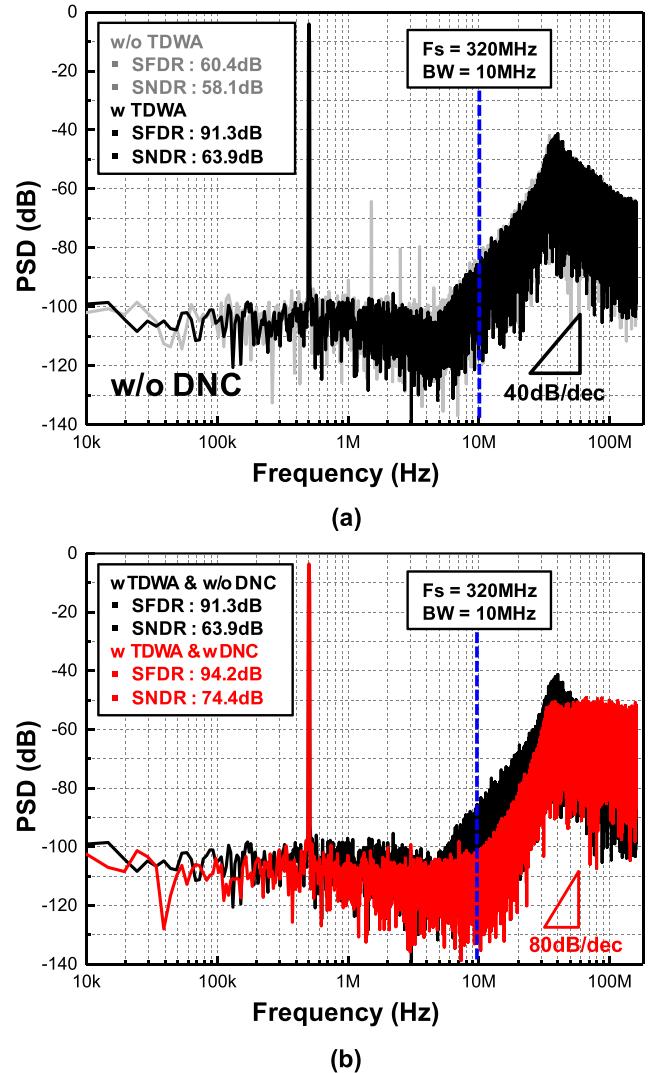


Fig. 15. Measured output spectra with and without (a) TDWA and (b) DNC.

#### IV. MEASUREMENT RESULTS

A prototype CT DSM was implemented in a 28-nm CMOS process. A die photograph is shown in Fig. 13. The core size is 0.1 mm<sup>2</sup>, and the area occupied by the proposed SAR and second-order DNC filter is only 3% of the core size. For an OSR of 16, the proposed CT DSM is clocked at 320 MHz for a 10-MHz bandwidth. Fig. 14 shows the power breakdown of the prototype. The total power consumption is 4.2 mW under supply voltages of 1.2 V for DACs and 1.1 V for the remaining blocks. The most power-consuming block is the loop filter, which accounts for 57% of the total power consumption. Despite the low OSR, the power consumed in the loop filter is greater than expected, as it is not optimized for the opamp design. The digital blocks including key building blocks of the DNC and the references for the SAR ADC consume 28%.

Fig. 15 shows the measured FFT spectrums with a 502-kHz input signal. In order to illustrate the effect of TDWA, Fig. 15(a) shows the measured FFT spectrums without DNC. When both the DNC and TDWA are disabled, the achieved

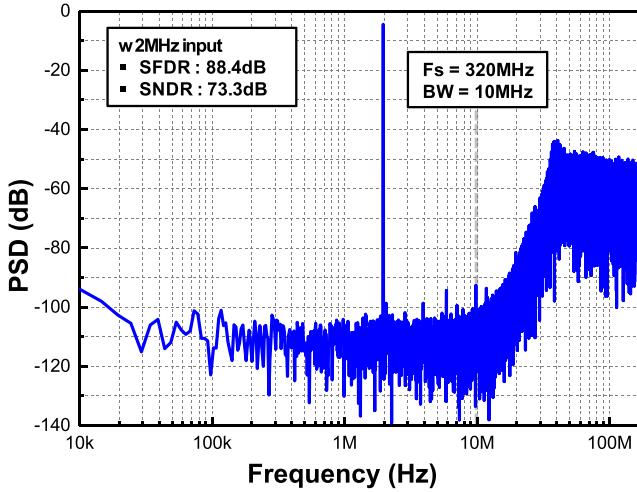


Fig. 16. Measured output spectrum with 2-MHz input frequency.

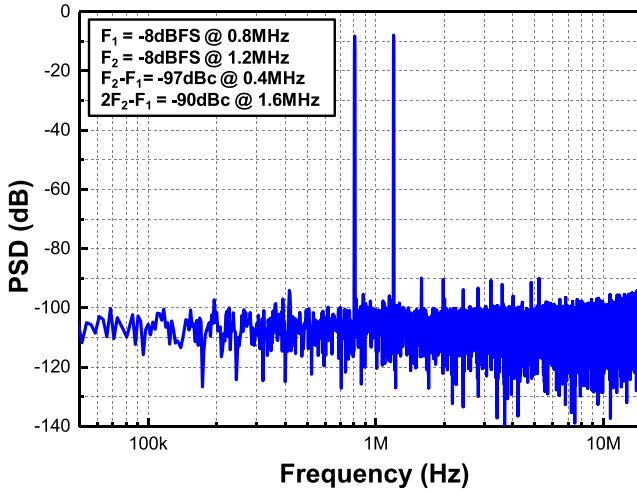


Fig. 17. Measured output spectrum with two tones.

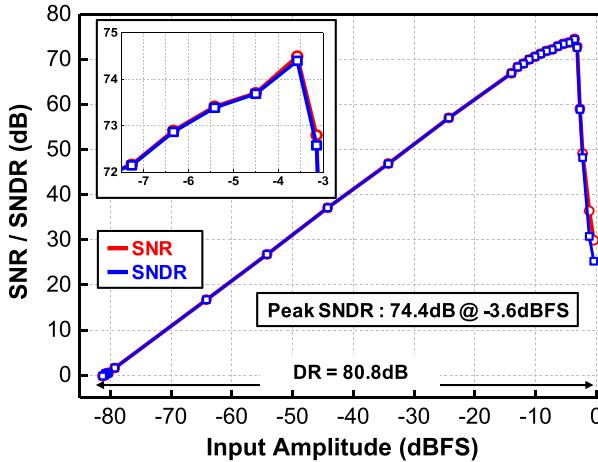


Fig. 18. Measured SNDR according to input amplitudes.

SNDR is 58.1 dB with considerable harmonic tones and a noise floor. When the TDWA is enabled, the SFDR is substantially improved by 31 dB, from 60.4 to 91.3 dB, but still with

TABLE I  
PERFORMANCE SUMMARY AND COMPARISON

	This work	[19]	[20]	[21]	[22]
Process [nm]	<b>28</b>	130	40	65	65
Area [mm <sup>2</sup> ]	<b>0.1</b>	0.08	0.02	0.04	0.03
Supply [V]	<b>1.1/1.2</b>	1.2	-	1.1	1.0
Fs [MHz]	<b>320</b>	640	600	650	1000
OSR	<b>16</b>	32	30	32.5	50
BW [MHz]	<b>10</b>	10	10	10	10
SNDR [dB]	<b>74.4</b>	75.3	67.4	68.6	72.2
SFDR [dB]	<b>94.2</b>	94.1	-	77.0	77.8
DR [dB]	<b>80.8</b>	78.5	68.7	71.2	77.0
Power [mW]	<b>4.2</b>	7.2	1.9	1.8	1.6
FoM <sub>S_DR</sub> [dB]	<b>174.5</b>	169.9	165.8	168.6	175.0
FoM <sub>S_SNDR</sub> [dB]	<b>168.1</b>	166.7	164.5	166.0	170.2

$$\text{FoM}_{S\_DR} = \text{DR} + 10 \cdot \log_{10} (\text{BW}/\text{Power})$$

$$\text{FoM}_{S\_SNDR} = \text{SNDR} + 10 \cdot \log_{10} (\text{BW}/\text{Power})$$

a second-order noise shaping characteristic. When both the DNC and TDWA are enabled as shown in Fig. 15(b), the noise floor is significantly improved due to the fourth-order noise shaping, resulting in a peak 74.4-dB SNDR within a 10-MHz signal bandwidth. Fig. 16 shows the measured FFT spectrum for a higher input frequency within the signal bandwidth. With a 2-MHz input signal, a peak SNDR of 73.3 dB and SFDR of 88.4 dB at -4 dBFS are achieved. The measured two-tone test is shown in Fig. 17. With -8 dBFS inputs at 0.8 and 1.2 MHz, second inter-modulation (IMD<sub>2</sub>) and third inter-modulation (IMD<sub>3</sub>) are -89 and -82 dBc, respectively. Fig. 18 shows the measured DR of 80.8 dB. The full scale of the modulator input signal (0 dBFS) is 1 V<sub>pp</sub>. Table I provides a detailed comparison with other designs with the same input bandwidth of 10 MHz. We could achieve outstanding Schreier FoM of 174.5 dB for DR with the smallest OSR 16 among comparable designs, owing to the proposed second-order DNC.

## V. CONCLUSION

This paper demonstrates the first CT DSM design with a DNC scheme utilizing a single SAR ADC, which makes the noise coupling filter compact and power efficient. Due to the digital implementation, the noise coupling filter performance is expected to be tolerant to PVT variation. Despite the low OSR of 16, the prototype modulator with a second-order loop filter achieved a Schreier FoM of 174.5 dB for a signal bandwidth of 10 MHz.

## ACKNOWLEDGMENT

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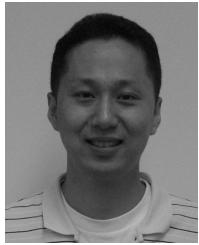
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