A 16-Element 4-Beam 1 GHz IF 100 MHz Bandwidth Interleaved Bit Stream Digital Beamformer in 40 nm CMOS

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***Abstract*— A 1 GHz intermediate frequency, 16-element, 4-beam digital beamformer facilitates multi-in multi-out, 5G mobile, and other emerging communication standards. Digital beamforming has been limited by high power consumption, large die area, and the need for a large number of analog-to-digital converters (ADCs). The proposed digital beamformer addresses these issues by combining interleaved bit stream processing (IL-BSP) with power- and area-efficient continuous-time bandpass delta-sigma modulators (CTBPDSMs). Compared to conventional DSP, IL-BSP reduces both power and area by 80%. The new CTBPDSM architecture reduces ADC area by 67% and the energy per conversion by 43% with a power- and area-efficient three-stage nested G_m-C op-amp and a passive summer. With an 11.2 dB array gain, the digital beamformer achieves a 58.5 dB signal to noise and distortion ratio and a 59.6 dB SNR over a 100 MHz bandwidth. Thanks to the accurate digitization and digital processing, the measured beam patterns of the four simultaneous beams are near ideal.**

***Index Terms*— 5G mobile communication, bit stream processing (BSP), delta-sigma modulation, digital beamforming (DBF), linear antenna array, linearity, multi-in multi-out (MIMO), phased array, receiver.**

I. Introduction

5G wireless systems will use millimeter-wave bands to support more users and deliver higher data rates [1]. However, millimeter-wave systems face severe link-budget challenges due to high path losses and the lower diffraction of millimeter-wave signals [2], [3]. Large array beamforming is an essential technology to make up for the reduced link budgets with array gain and to establish a reliable wireless connection through multi-in multi-out (MIMO) algorithms.

Digital beamforming (DBF) has several advantages over analog beamforming (ABF) including accurate beam patterns, multiple receive beams without SNR penalty, adaptive interference suppression, simplified calibration, and fully reconfigurable beam shape flexibility [4]. Seamless generation of multiple simultaneous beams in DBF allows us to exploit MIMO techniques for improved reliability and higher data rates. For example, transmit diversity improves resistance to multipath fading by receiving a single data stream via multiple beams [5]. Spatial multiplexing, in which different data streams are received through different beams, can also achieve higher data rates or further reduce the SNR requirement of the receiver [6]. However, DBF is limited in practice by high power consumption and large die area [7].

To reduce the power dissipation, [8] presents a digital beamformer implemented with a bit stream processing (BSP) approach. This BSP beamformer prototype achieves 64% lower power and 68% smaller area compared to a conventional DSP-based beamformer. BSP saves power and area by implementing complex digital multiplication with simple multiplexers (MUX) and reducing the number of decimators from the number of channels to the number of beams. However, the digital beamformer prototype in [8] is limited to 20 MHz bandwidth, eight elements, and two simultaneous beams.

Paving the way for large scale MIMO for 5G communication, we present a digital, 16-element, 4-beam beamformer with a 100 MHz bandwidth. A 4 GS/s analog-to-digital converter (ADC) with an oversampling ratio (OSR) of 20 supports a 100 MHz bandwidth. A challenge is that the approach in [8] necessitates that the digital circuitry also runs at 4 GHz, which is difficult in 40 nm CMOS. Furthermore, it is critical to have power- and area-efficient ADCs, as 16 are needed. To overcome these challenges, we introduce interleaved BSP (IL-BSP), which reduces both power and area by 80% compared to a DSP implementation. We also utilize compact and efficient continuous-time bandpass delta-sigma modulators (CTPBDSMs), which occupy only 1/3 of area and consume 43% less energy per conversion than the ADCs in [8].

This paper is an extension of [9] and is organized as follows. Section II compares the ADC power consumption for DBF and ABF. Section III details the implementation of the IL-BSP. Section IV presents the circuit implementation of the CTBPDSM, and Section V introduces the system architecture of the IL-BSP digital beamformer. Section VI provides measured results of the prototype beamformer IC, and Section VII concludes this paper.

II. ADC Power Comparison for Digital and Analog Beamforming

Although DBF requires a large number of ADCs, if the ADCs are noise limited then the total ADC power for DBF and ABF is comparable.

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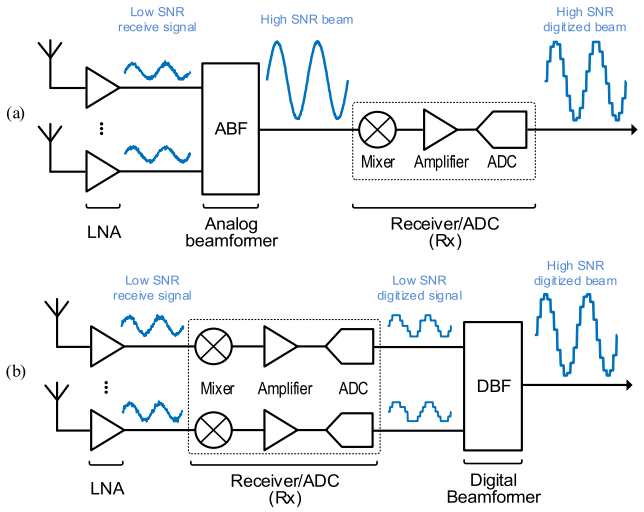

Fig. 1. System architectures of (a) analog and (b) digital beamforming.

A. Thermal Noise Limited

Although DBF requires a large number of ADCs, the array gain in DBF greatly relaxes the ADC SNR requirement. Furthermore, if we assume that the ADCs are noise limited, then the total ADC power is the same for both cases.

ABF necessitates a high ADC SNR to quantize the high SNR beam since beamforming is performed prior to the ADC [Fig. 1(a)]. Although DBF necessitates several ADCs, the SNR requirement of a single ADC can be greatly relaxed, as the lower SNR signals from the individual ADCs combine to generate a high SNR beam [Fig. 1(b)]. The SNR requirement of the ADCs in ABF and in N-element DBF is expressed as

$$\mathrm{SNR_{ABF}} = \mathrm{SNR_{target}} \tag{1}$$

$$\mathrm{SNR_{DBF}} = \frac{\mathrm{SNR_{target}}}{N} \tag{2}$$

where $\mathrm{SNR_{target}}$ is the SNR requirement of the system, $\mathrm{SNR_{ABF}}$ is the SNR requirement of the single ADC in ABF, and $\mathrm{SNR_{DBF}}$ is the SNR requirement of one of the ADCs in DBF. As shown in (1) and (2), $\mathrm{SNR_{DBF}}$ is N times lower than $\mathrm{SNR_{ABF}}$, as N-element DBF exploits a digital array gain of N. (Receive signals from channels constructively interfere to generate N^2 times higher signal power, and uncorrelated noise from channels produce N times greater noise power.)

With an assumption that the ADCs in DBF and ABF have the same Schreier figure of merit (FoM), the total power consumption of the ADCs in ABF and DBF can be represented as

$$P_{\mathrm{ABF}} = \frac{\mathrm{SNR_{ABF}} * \mathrm{BW}}{\mathrm{FoM}_s} \tag{3}$$

$$P_{\mathrm{DBF}} = \frac{\mathrm{SNR_{DBF}} * \mathrm{BW}}{\mathrm{FoM}_s} * N \tag{4}$$

where P_{ABF} is the power consumption of the ADC in ABF and P_{DBF} is the power consumption of all ADCs in DBF. As $\mathrm{SNR_{DBF}}$ is N times lower than $\mathrm{SNR_{ABF}}$, the total power consumption of all the ADCs in DBF is the same as the single ADC power consumption in ABF when the ADCs are limited by noise.

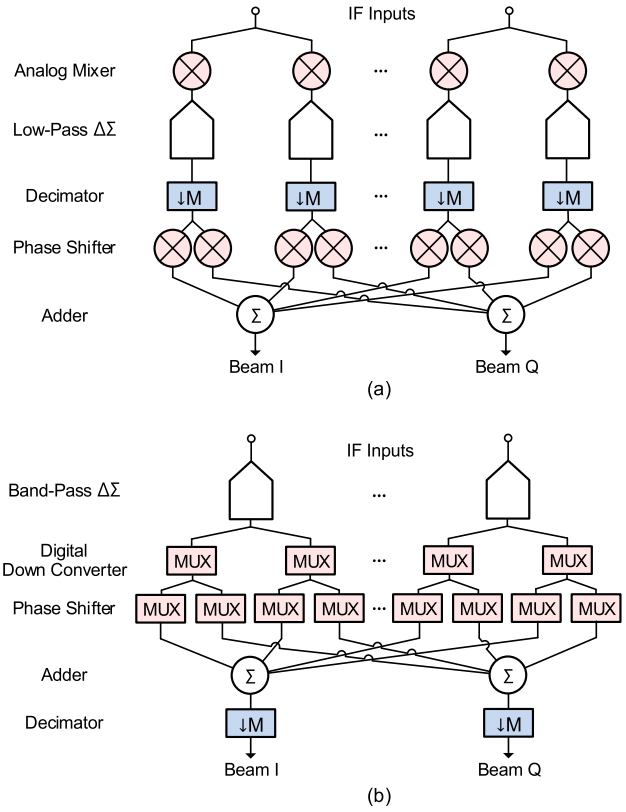

Fig. 2. Digital beamformers in (a) DSP and (b) BSP implementations.

B. Interference Limited

When a beamformer receives M interference signals, the total received input power of an ADC can be represented as $(\sum_{m=1}^{M} I_m)+S$, where I_m is the mth interference power and S is the signal power. In this case, the SNR requirement of the ADC becomes $10\log_{10}((\sum_{m=1}^{M}(I_m/S))+1)$ dB higher. For example, when we have one interferer that sends the exact the same power as the signal transmitter at the same distance, the SNR requirement of the ADC in a digital beamformer increase by 3.01 dB (0.5 bit effective number of bits). The SNR requirement for an analog beamformer does not increase by as much because the interference is attenuated. If the mth interference is attenuated by N_m dB, the SNR requirement of an ADC in an analog beamformer increases by $10\log_{10}((\sum_{m=1}^{M}(I_m/s)10^{-(N_m/10)})+1$ dB, which is lower than for DBF.

III. Digital Beamforming Architecture

A. Bit Stream Processing Digital Beamformer

To understand bit stream beamforming, we first consider more conventional digital beamformer architecture with conventional DSP and low-pass delta-sigma modulators as shown in Fig. 2(a). Analog mixers downmix the receive signals and then low-pass delta-sigma modulators convert the downmixed signals to bit streams. Decimators convert the bit streams to low-sample-rate high-resolution digital signals. Phase shifting through digital multiplication and finally, addition of the phase-shifted signals generates a beam.

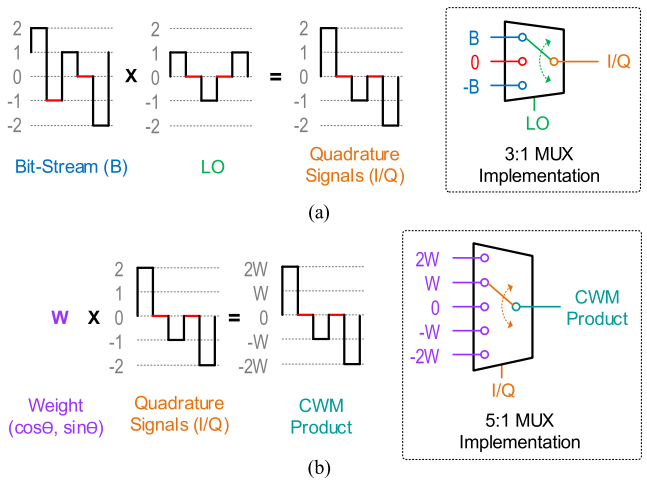

Fig. 3. MUX-based (a) digital downconversion and (b) CWM implementation in BSP.

In contrast, BSP implements high-speed digital multiplication with simple MUX operating directly on the low-resolution bit streams from bandpass ADCs [Fig. 2(b)], removing the need for a power and area hungry decimator in each channel [8]. A BSP digital downconverter (DDC) directly downconverts the bit stream from intermediate frequency (IF) to base band, by multiplying the bit stream with a digital local oscillator (LO) signal. The low-resolution quantizer in the CTBPDSM generates the five-level $(-2, -1, 0, 1, 2)$ bit stream. A sampling frequency 4 times higher than the LO frequency results in a sampled LO signal represented as three levels $(-1, 0, 1)$, as shown in Fig. 3(a). In [8], this multiplication operation is implemented with a 3:1 MUX using the three-level LO as the MUX select. The product of the multiplication between the three-level LO and the five-level bit stream remains a five-level signal.

Complex weight multiplication (CWM) can be expressed in a matrix form as

$$\begin{bmatrix} I_k' \\ Q_k' \end{bmatrix} = \begin{bmatrix} \cos(k\theta) & \sin(k\theta) \\ -\sin(k\theta) & \cos(k\theta) \end{bmatrix} \begin{bmatrix} I_k \\ Q_k \end{bmatrix} \tag{5}$$

$$\theta = 2\pi f_c \frac{d\sin\psi}{c} \tag{6}$$

where I_k and Q_k are the downconverted signals from the kth element, I_k' and Q_k' are the phase-shifted outputs, and the θ is a constant phase for a given incident angle (ψ) and center frequency (f_c) as represented in (8). Because multiplication in CWM scales the bit stream with a weight [$\cos(k\theta)$ or $\sin(k\theta)$] it is efficiently implemented with a 5:1 MUX with the bit stream as the MUX select [Fig. 3(b)].

An important advantage of BSP is the reduced number of decimators. As shown in Fig. 2(a), in the DSP approach each antenna element requires a decimator, however, with BSP there is only one decimator per beam [Fig. 2(b)]. This is an advantage because a high-speed decimator requires extensive high-speed addition, which consumes a significant amount of power. It is shown in [8] that the decimation filters consume 87% of the DBF power in a conventional DSP implementation. Thanks to the reduced number of decimators and MUX-based multiplication, the eight-element two-beam digital beamformer in [8] reduces power consumption by 64% and area by 68% compared to a conventional DSP implementation.

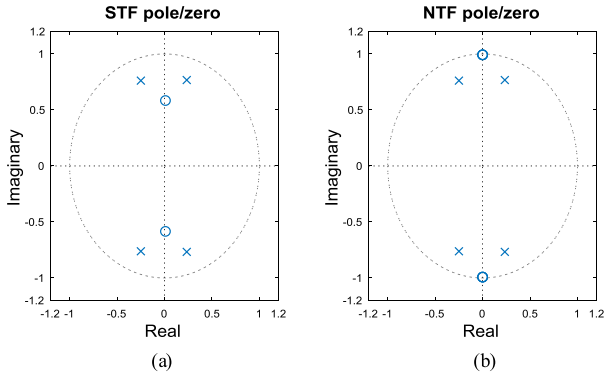

Fig. 4. (a) STF and (b) NTF pole/zero placement of the 4th-order bandpass delta-sigma modulator.

B. Interleaved Bit Stream Processing Digital Beamformer

The ADC in this paper digitizes the received signals at 4 GS/s for a 100 MHz bandwidth. This also requires the digital circuitry to run at 4 GHz, which is challenging for the BSP MUX logic and especially challenging for the decimators. While the adders in the decimators have input bit widths more than 20-bit, 40 nm CMOS can only perform an 8–10 bit addition in one clock cycle with 40 ps of setup and hold time [10]. To address this challenge, we introduce IL-BSP to halve the clock rate and reduce both power and area significantly.

IL-BSP performs a two-stage decimation with an initial decimation by two at the digital downconversion to reduce the subsequent digital processing rate to 2 GHz. As we will see, this initial decimation by two is very efficient because it takes advantage of the nulls in the noise transfer of the bandpass modulator and also exploits a nearly free two-stage cascaded integrated comb (CIC) filter in the digital downconversion to baseband I and Q signals. After this $2\times$ decimation, CWM, summation and final decimation of the beam signals run at 2 GHz.

The initial decimation by two takes advantage of the fortuitous aliasing of noise shaping nulls in the bandpass modulator. For bandpass modulators, the center frequency is chosen to be one-fourth of the sampling frequency to facilitate efficient digital downconversion. With this ratio of center and sampling frequencies, the sampled LO waveforms can be represented as -1, 0, and 1, so that DDC can be implemented with simple MUX.

To understand the decimation process, we first consider the noise transfer function (NTF) of the bandpass modulator and the corresponding downmixed NTF. Fig. 4 shows the pole and zero placements for the 4th-order bandpass modulator in this paper. Because the NTF zeros of the bandpass modulator occur in complex conjugate pairs, the NTF of the 4th-order bandpass modulator has two zeros at 1/4 F_s and two more zeros at 3/4 F_s [Fig. 4(b)] [11]. Therefore, the 4th-order bandpass modulator shapes quantization noise from 1/4 F_s and 3/4 F_s with a -40 dB/decade slope, as shown in Fig. 5(a). Downmixing of the bandpass NTF with the 1/4 F_s LO leads to the NTF

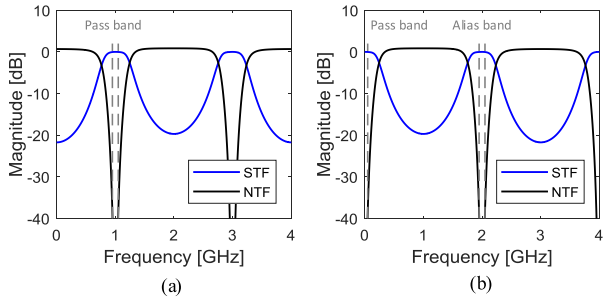

Fig. 5. Frequency domain representation of (a) quantization noise from the 4th-order bandpass $\Delta\Sigma$, and (b) after downmixing.

in Fig. 5(b), with noise shaping nulls at dc, $F_s/2$ and F_s. Downsampling by two to a sampling rate of $F_s/2$ takes advantage of the fact that the noise null at $F_s/2$ aliases onto the signal of interest.

A low-cost two-tap CIC filter takes advantage of the 0s in the LO sequence to further minimize any aliasing artifacts associated with downmixing. This allows the downmixing to baseband I and Q and the downsampling by two to be combined in an elegant way. The transfer function of a 1st-order CIC decimation filter is expressed as follows:

$$H(z) = \frac{1 - z^{-2}}{1 - z^{-1}} = 1 + z^{-1}. \tag{7}$$

We begin by considering a 1st-order CIC decimation filter and a $2\times$ decimator placed after the digital downconversion and DBF to generate half rate I and Q signals [Fig. 6(a)]. Because every other LO value is always zero [see Fig. 3(a)], every other I/Q value and every other I/Q beam value are also zero. Due to these zero values, the CIC filter block $(1 + z^{-1})$ repeats each value twice and the subsequent downsampler simply samples one of these repeated values to produce a 2 GS/s beam. More efficiently, the approach in Fig. 6(b), simplifies the filter and decimator with a digital delay (z^{-1}) to produce the same I/Q beams with reduced circuit complexity.

IL-BSP [Fig. 6(c)] moves the digital delay and the $2\times$ downsamplers of Fig. 6(b) to the front of the DBF block. The combination of the digital delay and downsamplers acts as an interleaver that outputs the even-numbered data as I, and the odd-numbered data as Q. The interleaver allows the digital beamformer to run at half speed without losing any performance or accuracy (Fig. 7). Removing the zeros means ignoring all zero value LO inputs to the DDC. Therefore, DDC is implemented with a 2:1 MUX, driven by the LO values, simplifying circuit implementation, and reducing power consumption.

C. Comparison

Fig. 8 compares power and area of 16-element 4-beam 1 GHz IF digital beamformers implemented with a conventional DSP approach and with the IL-BSP approach. The 16 decimators in DSP consume 84% of the total digital power and occupy 52% of the total area. Although the DDC and CWM in IL-BSP dissipate a comparable amount of power to DDC and CWM in DSP, the IL-BSP decimators only consume 14 mW, which is far lower than 290 mW for the DSP decimators. Moreover, MUX-based multiplication in IL-BSP reduces the area of CWM by 68%. Consequently, IL-BSP reduces both power and area by 80% compared to a conventional DSP implementation. The entire IL-BSP digital beamformer with 16 elements and 4 beams consumes only 68 mW and occupies 0.0625 mm^2.

IV. Continuous-Time Bandpass Delta-Sigma Modulator

A. Advantages over Discrete-Time Low-Pass Nyquist ADC

The continuous-time bandpass delta-sigma modulator has several advantages. A continuous-time modulator has inherent anti-alias filtering. As discussed in [12], the NTF of the 4th-order CTBPDSM in Fig. 9 can be expressed as

$$\mathrm{NTF}(z) = \frac{1}{1 - L(z)} \tag{8}$$

where $L(z)$ is the discrete-time transfer function from the quantizer output, through the feedback DACs and the resonators, back to the quantizer input. The NTF is expressed in the z-domain because the quantization noise is sampled by the quantizer. The signal transfer function (STF) of the modulator can be expressed as

$$\mathrm{STF}(s, z) = \frac{G(s)}{1 - L(z)} \tag{9}$$

$$= G(s)\,\mathrm{NTF}(z) \tag{10}$$

where $G(s)$ is the transfer function of the feed-forward path. As $s = j2\pi f$ and $z = e^{j2\pi f/f_s}$, (10) can be rewritten as

$$\mathrm{STF}(f) = G(j2\pi f)\,\mathrm{NTF}\left(e^{j2\pi f/f_s}\right). \tag{11}$$

Fig. 10 shows the frequency domain representations of $G(j2\pi f)$, $\mathrm{NTF}\left(e^{j2\pi f/f_s}\right)$, and $\mathrm{STF}(f)$. Although the NTF has zeros in the pass-band [Fig. 10(b)], the poles of the resonators [Fig. 10(a)] cancel the NTF zeros, making a reasonably flat STF gain. On the other hand, the STF gain in the alias bands is much lower because there are no resonator poles [Fig. 10(c)]. Therefore, interference in the alias bands is attenuated, which greatly relaxes anti-alias filtering requirements.

Another advantage of the bandpass modulator approach is that digital mixing does not suffer from I/Q mismatch, mixer noise, dc offset, and flicker noise. Bandpass digitization also halves the number of required ADCs because the quadrature signals share an ADC. On the other hand, two low-pass modulators are required to digitize I and Q signals.

B. Wide Bandwidth ADC

Emerging standards require relatively wide ADC bandwidths for high data rates. The 4th-order CTBPDSM achieves a 100 MHz bandwidth with a 4 GHz sampling rate and an OSR of 20. Furthermore, small-area and low power consumption are critical as DBF has a large number of ADCs. We reduce power and area with various techniques including: 1) digital array gain; 2) redesign of the feedback DACs; 3) a passive summer; 4) a compact *RC*-based resonator; and 5) a three-stage nested G_m-C op-amp.

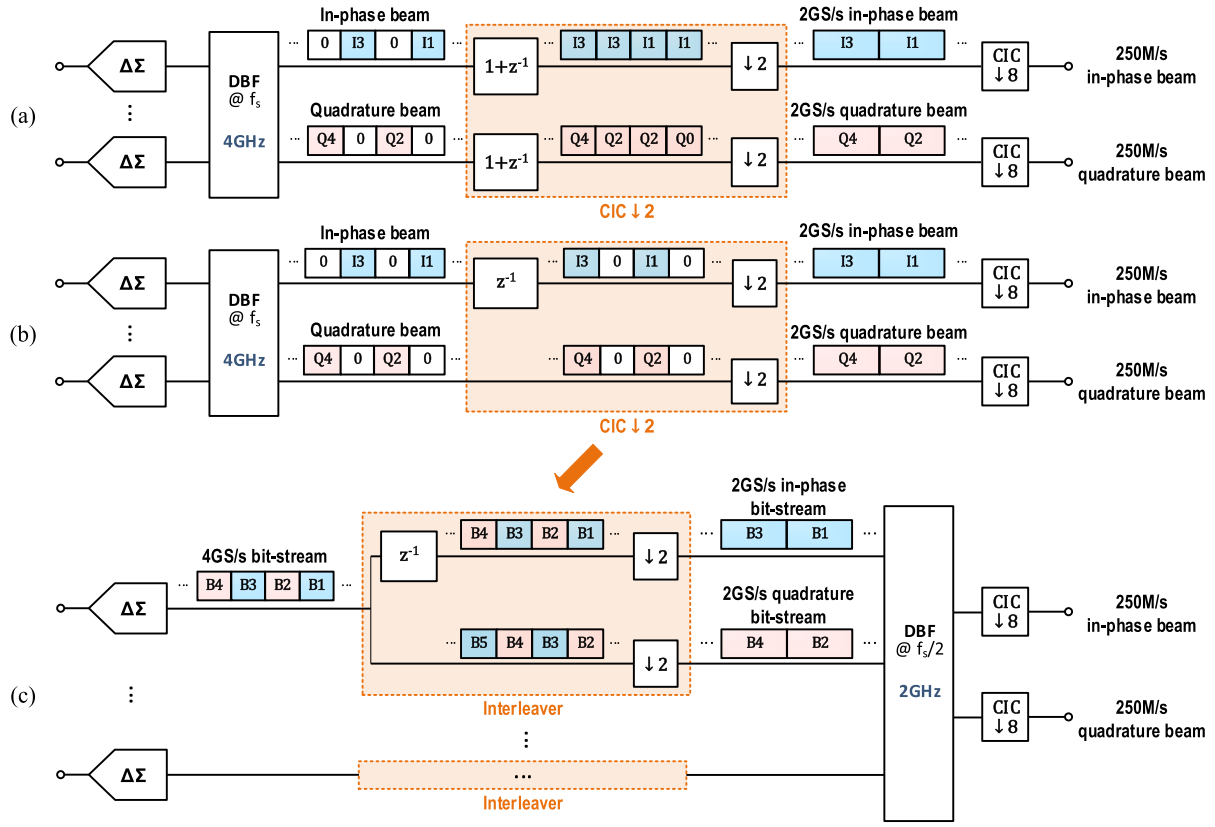

Fig. 6. (a) Two-stage CIC filter and (b) equivalent implementation of the filter following a BSP DBP block. (c) IL-BSP DBF with an interleaver in front of the DBF block.

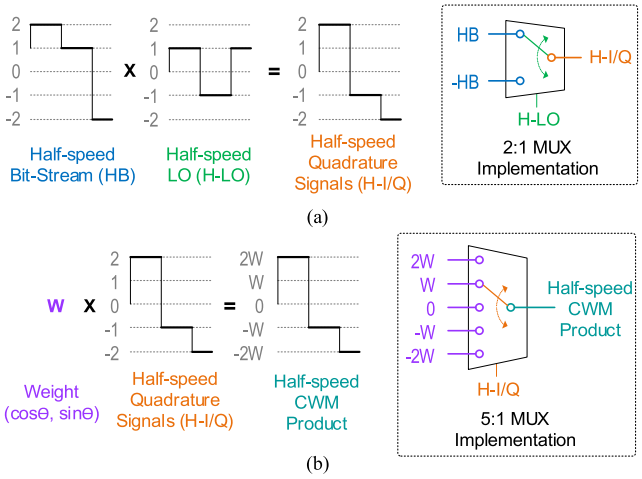

Fig. 7. MUX-based (a) digital downconversion and (b) CWM implementation in IL-BSP.

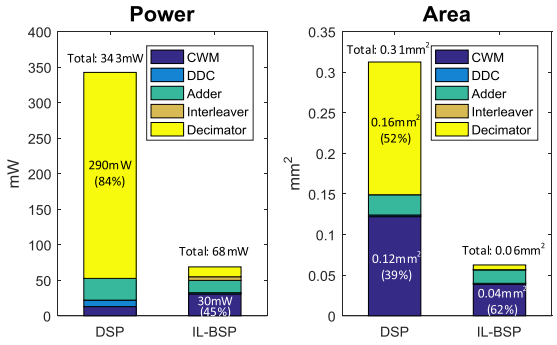

Fig. 8. Power and area comparison between DSP and IL-BSP.

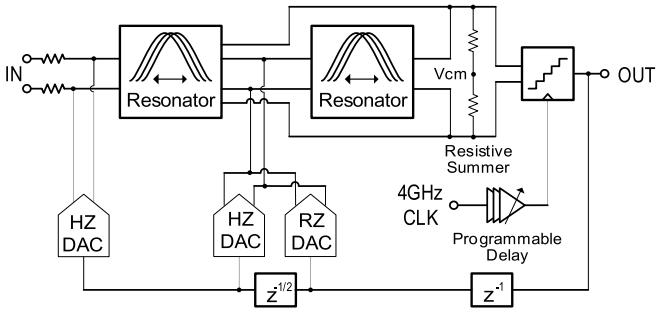

Fig. 9. Fourth-order continuous-time bandpass delta-sigma modulator.

1) Digital Array Gain: We exploit the high digital array gain to lower the SNR requirement of the individual ADCs. An advantage of DBF is that it performs highly accurate digital downconversion, and CWM, so that array gain is close to the theoretical limit. This prototype benefits from a near-ideal 11.2 dB array gain, which significantly lowers SNR requirements of the ADCs.

2) Elimination of the First Return-to-Zero DAC: We modify the DAC feedback to further save power and area [13]. Conventionally, a continuous-time bandpass modulator requires a pair of feedback DACs, consisting of a return-to-zero (RZ) DAC and a half-clock-delayed RZ (HZ) DAC for each resonator to perfectly transform a discrete-time modulator into a

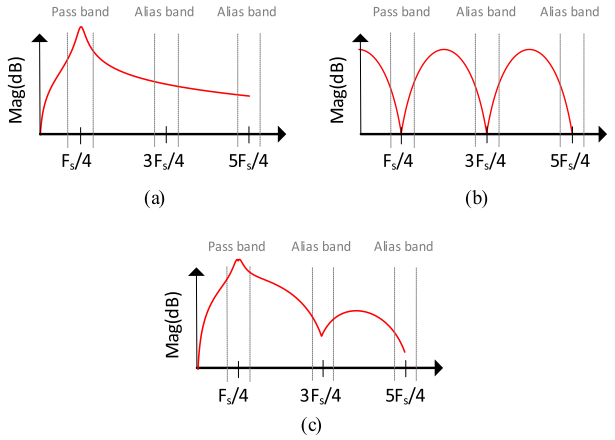

Fig. 10. Frequency domain representations of the (a) resonator, (b) noise transfer function, and (c) STF of the CTPBDSM.

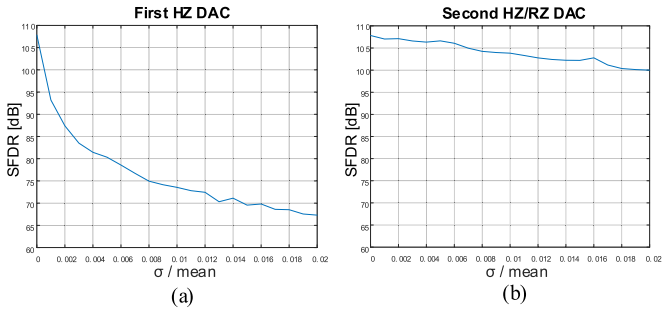

Fig. 11. Effect of mismatch in the (a) first-stage DAC and (b) second-stage DAC on the SFDR of the modulator.

continuous-time modulator. Based on the calculations in [14], the current of the first-stage RZ DAC is made much smaller than that of the first-stage HZ DAC. Due to the small current of the first-stage RZ DAC, proper tuning of the second-stage DACs can remove the need for the first-stage RZ DAC, reducing system noise and power consumption.

The SFDR of the CTPBDSM is limited by the mismatch of the first-stage DAC, as the first resonator attenuates the non-linearity of the second-stage DACs (Fig. 11). The average output current of the first-stage DAC is 70 μA, and its standard deviation is 1.4 μA. The measured SFDR of the modulator is 66 dB, and the schematic of the first-stage RZ DAC is shown in Fig. 12.

3) Passive Summer: A passive summer further reduces power and area. We replace the power hungry active trans-impedance amplifier used in [8] with a resistive summer that adds the output current of the first resonator with the output current of the second resonator. Consequently, the CTBPDSM consumes 20% less power and occupies 10% less area.

4) High Intermediate Frequency (IF): The single op-amp-based *RC* resonator in Fig. 13 is used instead of a bulky *LC*-tank resonator. As discussed in [13], the resonator transfer function $T(s)$ and center frequency w_0 are

$$T(s) = \frac{w_o s}{s^2 + w_o^2} \tag{12}$$

$$w_0 = \frac{1}{2R_pC_p} \tag{13}$$

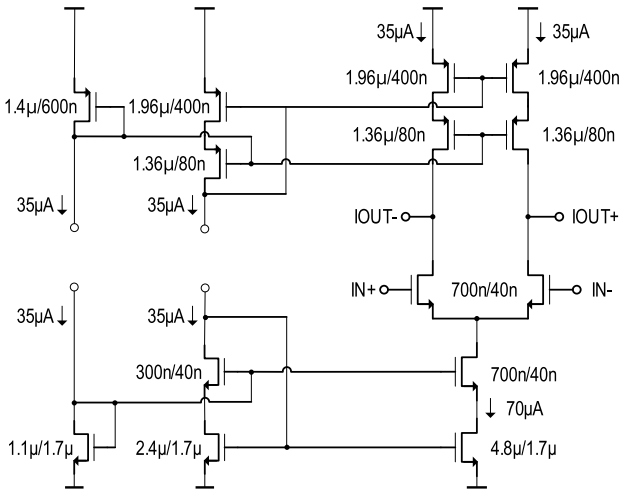

Fig. 12. Schematic of the first-stage RZ DAC.

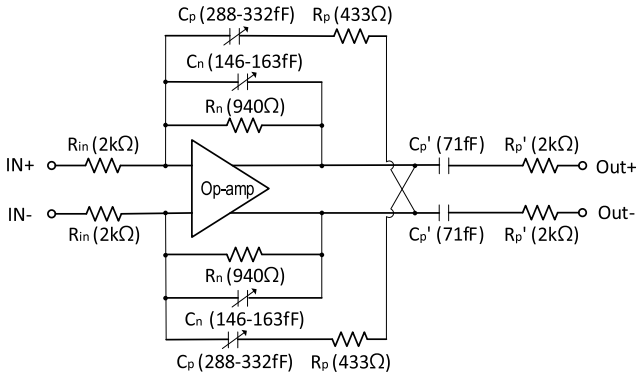

Fig. 13. *RC*-based single op-amp resonator.

when $C_p = 2C_n$ and $R_n = 2R_p$. As indicated by (13), the center frequency is inversely proportional to R_p and C_p. The high IF frequency of 1 GHz, allows the use of smaller resistors and capacitors to reduce the area of the resonators. As a result, the resonator size is only 0.003 mm^2 and the CTBPDSM occupies 0.01 mm^2. To account for PVT variation, the resonator center frequency is tuned with a 3-bit trim of C_p and C_n (Fig. 13).

5) Three-Stage Nested Gm-C Op-Amp: Compared to switched-capacitor-based discrete-time modulators, continuous-time modulators have relaxed op-amp bandwidth constraints [12]. We use the three-stage cascaded G_m-C structure in Fig. 14 which gives a good tradeoff between gain and bandwidth [15]. The first resonator op-amp consumes 5.4 mW and provides 13.22 GHz unity gain bandwidth, 71 dB dc gain with 100 fF load capacitance (i.e., the input capacitance of the second resonator).

V. System Architecture

As shown in Fig. 15, the 16-element 100 MHz bandwidth digital beamformer generates four simultaneous beams. The 16 CTBPDSMs digitize the 16 1 GHz IF inputs to create 4 GS/s five-level bit streams. The interleavers have the data rate by interleaving the digitized bitstreams into 2 GS/s quadrature signals. The 2:1 MUX-based DDCs downconvert

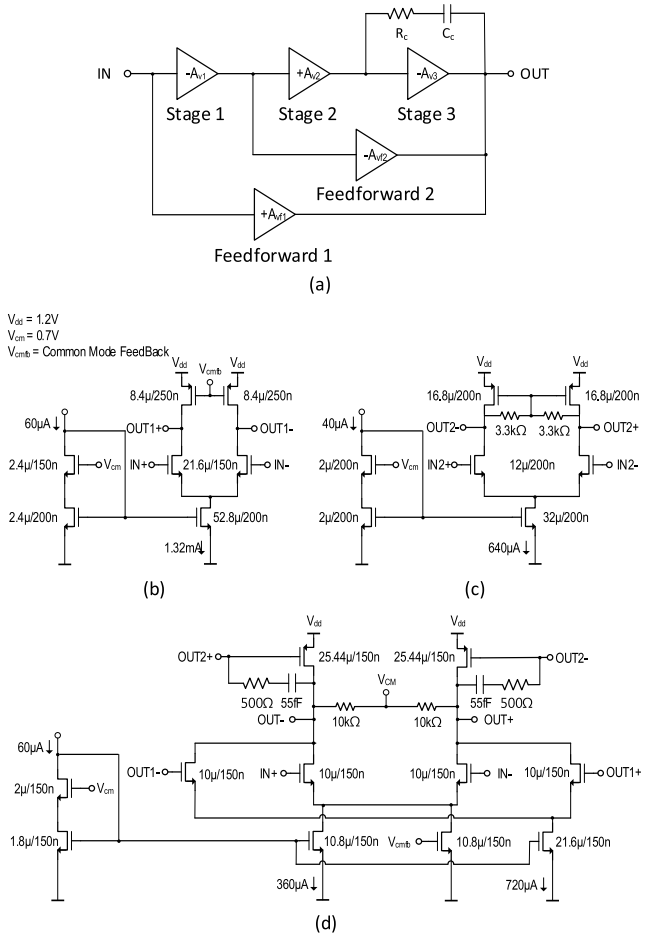

Fig. 14. (a) Three-stage nested G_m-C operational amplifier. Schematic of (b) stage 1, (c) stage 2, and (d) stage 3 with feed-forward amplifiers.

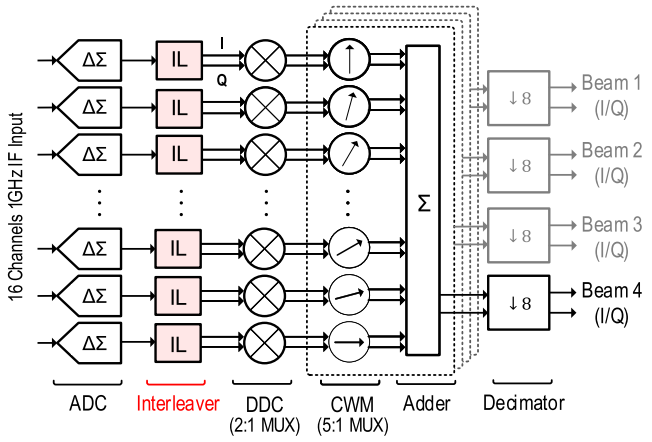

Fig. 15. System architecture of the prototype digital beamformer.

the quadrature signals to base band without adding noise or mismatch. The CWMs shift phase of the downconverted signals with complex weights set by 6-bit registers, resulting in a 0.02° main beam direction resolution. After phase shifting, the adder creates 2 GS/s quadrature beams. Finally, the decimators produce 13-bit 125 MS/s quadrature beams. The prototype digital beamformer has four sets of 16 CWMs, adders, and decimators, to produce four independent simultaneous beams for MIMO.

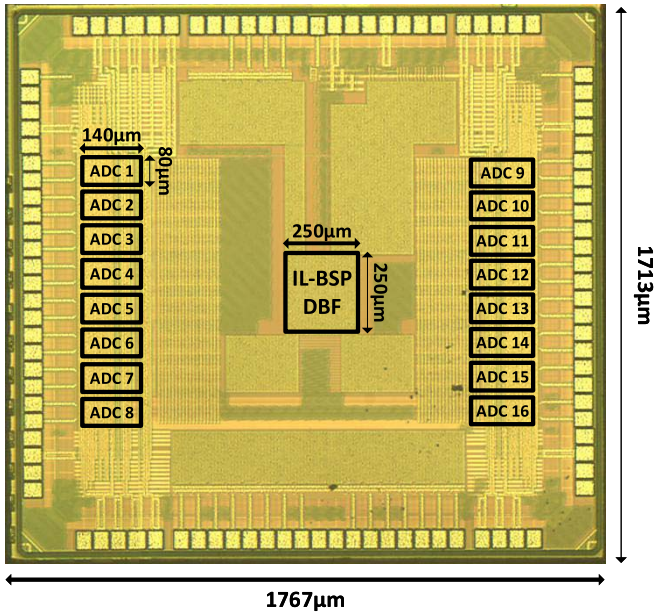

Fig. 16. Die micrograph (0.24 mm^2 of active area in 40 nm CMOS).

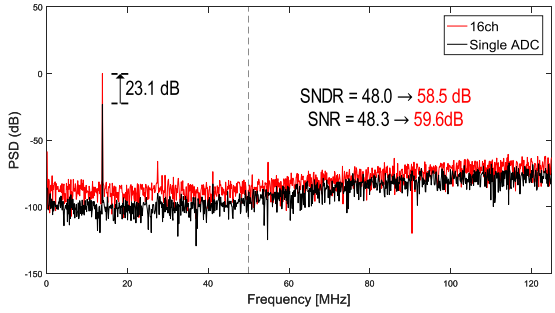

Fig. 17. Measured power spectral density of a single CTBPDSM and overall 16-element beamformer (input frequency: 1.013 GHz).

Fig. 16 shows a die micrograph of the prototype 16-element digital beamformer. The prototype is fabricated in ten-metal 40 nm CMOS and packaged in an 88-lead quad flat no-leads package. It occupies a core area of 0.24 mm^2, including the 16 CTBPDSMs and the DBF circuitry.

VI. Measurements

A. CTBPDSM

As shown in Fig. 17 the average measured single ADC signal to noise and distortion ratio (SNDR) over a 100 MHz bandwidth is 48 dB. The overall 16-element array achieves a measured SNDR of 58.5 dB which corresponds to a 10.5 dB improvement from the array. The measured array gain is 11.2 dB, with 59.6 dB SNR from the entire array.

Comparison With State-of-the-Art: Fig. 18 compares the area and Walden FoM [29] of this ADC with other state-of-the-art CTPBDMs. In addition to having the smallest area (0.01 mm^2) the prototype has one of the best FoMs (365 fJ/conv). Compared to [8], the prototype has 5 times higher bandwidth (100 MHz) and a 4 times higher center frequency (1 GHz), while using 43% less energy per conversion.

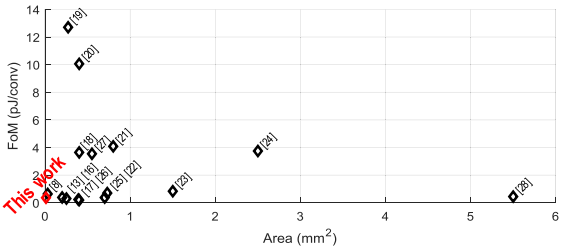

Fig. 18. Area and FoM comparison between the CTBPDSM in this paper and other state-of-the-art CTBPDSMs.

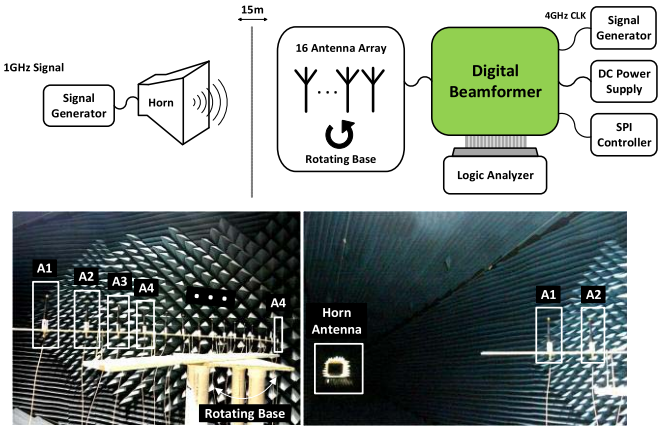

Fig. 19. Anechoic chamber test setup (top) and pictures showing 16 quarter-wave whip antennas (A1–A16), spaced at $\lambda/2$ (15 cm) increments on a rotating base (bottom).

B. Beam Pattern

1) Wireless Measurements: The resistive input and continuous-time operation allows the prototype device to be directly connected to a linear array of 16 quarter-wave whip antennas, spaced at $\lambda/2$ increments, without external LNAs. The 16-element antenna array is placed on a rotating base in an anechoic chamber to measure azimuth beam patterns (Fig. 19). A horn antenna with antenna gain of 15 dBi transmits a 15 dBm 1.006 GHz continuous wave signal from a distance of 15 m. An array of whip antennas each with an antenna gain of 1.3 dBi receives the -25 dBm signal. Beam patterns are measured over incidence angles from $-90°$ to 90° with a step size of 2.5°. This wireless test is performed without an RF front end. The RF signal is fed directly into the resistive input of the continuous-time ADCs. The ADC noise figure is 26 dB. Fig. 20 shows the measured beam patterns overlaid on ideal beam patterns in the log domain. The beam patterns are normalized. Ideally, the receiver is expected to achieve 55.4 dB SNR. The outer antennas of the 2.25 m antenna array receive significant echoes because they are outside of the 1 m quite zone of the anechoic chamber, resulting in some discrepancy between the ideal and measured patterns. Moreover, echoes and return loss from the 2-m-long antenna cables also cause measurement errors.

2) Wired Measurements: To more accurately measure beam patterns without the non-idealities of the anechoic chamber, we generate an array of 16 poly-phase input 1 GHz signals with 16 high-performance direct digital synthesizers (DDSs) shown in Fig. 21.

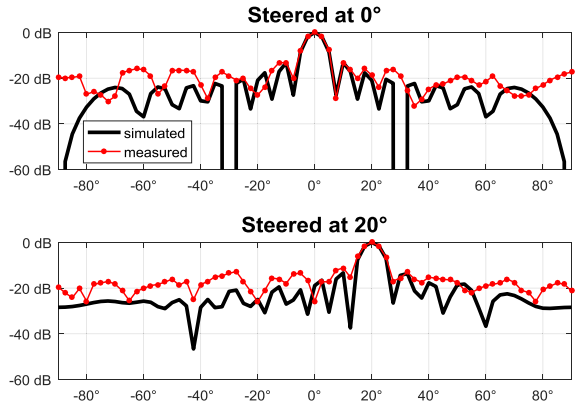

Fig. 20. Measured and simulated beam patterns of wireless test for 0° and 20° steered angles (input frequency: 1.006 GHz).

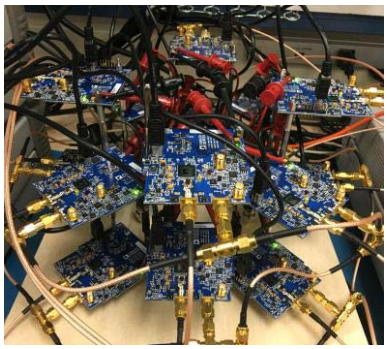

Fig. 21. 16 AD9164 DDS boards generate 16 synchronized 1 GHz signals.

a) Single main lobe beam pattern: Fig. 22 shows four measured simultaneous independent beam patterns with different incident angles (0°, 30°, 60°, and $-45°$). The measured beam patterns are near ideal, with a half-power beam width of 10° $-15°$ for a $+/-60°$ incident angle range.

b) Two main lobes beam pattern: IL-BSP also enables enhanced beam forming with multiple main lobes. As shown in Fig. 23, IL-BSP is programmed to produce a two-main-lobe beam pattern by averaging complex weights for two different single main lobe beam patterns as represented in the following equations:

$$\cos\theta_{1+2} = \frac{\cos\theta_1 + \cos\theta_2}{2} \tag{14}$$

$$\sin\theta_{1+2} = \frac{\sin\theta_1 + \sin\theta_2}{2}. \tag{15}$$

Theoretically, ABF can also achieve these beam patterns; however, hardware errors including channel mismatch limit the performance in practice [4]. The prototype digital beam former has measured beam patterns which are almost ideal for two incident angles 10°/50°.

c) Tapered beam pattern: Fig. 24 depicts measured tapered beam patterns with suppressed side lobes. This adaptive beam forming is performed by applying a Chebyshev window to the complex weights. The measured beam pattern for 0° incident angle has side lobes lower than -22.7 dB.

d) Beam patterns over the bandwidth: Fig. 25 shows the variation of the beam patterns over the $+/-50$ MHz input bandwidth to measure beam squinting (direction) error.

TABLE I
BEAMFORMER PERFORMANCE SUMMARY AND COMPARISON

	THIS WORK	J. Jeong JSSC 2016 [8]	F. Angiolini DATE 2017 [31]	H. Aliakbarian EuCAP 2010 [32]
Application	RF Communication	RF Communication	Ultrasound Imaging	Satellite
Integration	ADC + DDC + DBF	ADC + DDC + DBF	DBF	DBF
Center Frequency [GHz]	1.0	0.26	0.004	-
Bandwidth [MHz]	100	20	-	-
# of Elements	16	8	1024	2
# of Beams	4	2	1	1
Array SNR [dB]	59.6	-	-	-
Array SNDR [dB]	58.5	63.3	-	-
SNR improvement [dB]	11.2	-	-	-
SNDR improvement [dB]	10.5	8.9	-	-
Total Power [mW]	312	124	5000	500
DBF Power [mW]	68	19	5000	500
Active Area [mm^2]	0.22	0.28	-	-
Technology	40nm	65nm	FPGA	FPGA

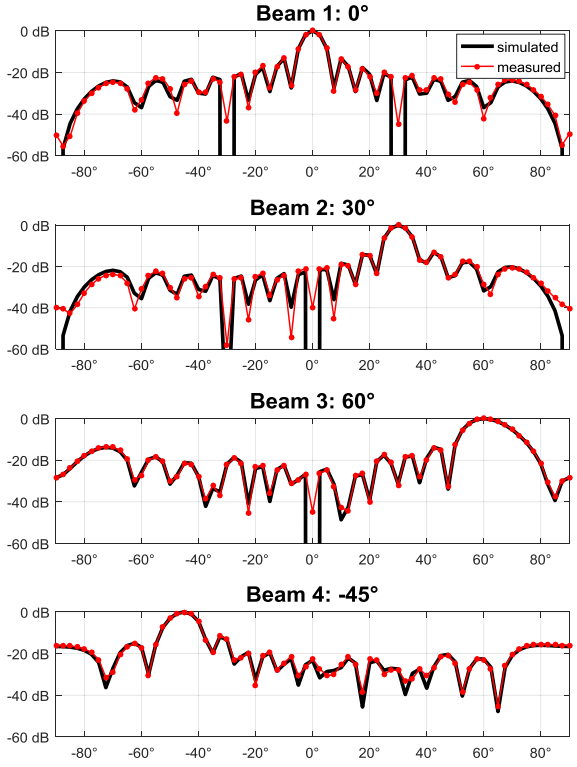

Fig. 22. Measured and simulated four independent simultaneous beams steered at different angles (input frequency: 994 MHz).

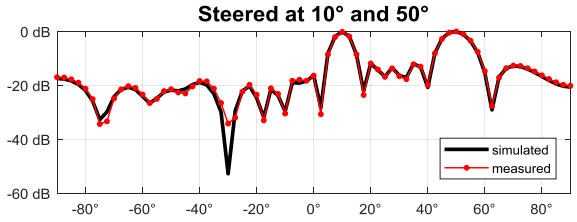

Fig. 23. Beam patterns with two main lobes (input frequency: 1.006 GHz).

The beam squinting error for a beamformer with ideal phase shifters can be approximated as

$$\Delta\Theta = -\frac{\tan\Theta_0}{f_0}\Delta f \tag{16}$$

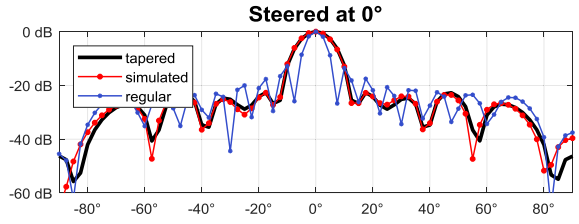

Fig. 24. Measured tapered beam patterns (input frequency: 1.006 GHz).

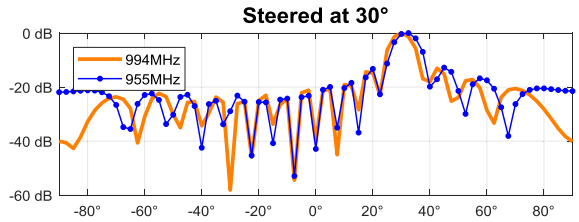

Fig. 25. Measured beam patterns over +/− 50 MHz bandwidth (input frequency: 994 and 955 MHz).

where $\Delta\Theta$ is the squinting error, Θ_0 is the main beam direction, f_0 is the center frequency, and Δf is the frequency offset of the input signals [30]. When a beamformer is steered at 30°, the theoretical beam squinting error for −45 MHz off-center frequency is 1.5°. The beam pattern in Fig. 25 has a 2.5° squinting error, which is the closest number to the theoretical error for a measurement angle step size of 2.5°.

e) Performance summary and comparison: Table I compares the digital beamformer prototype IC with state-of-the-arts. The digital beamformer in this paper has twice as many beams and elements as [8], which is the most for a published digital beamformer. The prototype consumes 312 mW (16 CTBPDSMs: 244 mW, DBF: 68 mW), and has a 11.2 dB array gain, which is 2.3 dB higher than [8]. It occupies 0.24 mm^2 (16 CTBPDSMs: 0.18 mm^2, DBF: 0.06 mm^2) of active area, which is 21% smaller than [8].

VII. CONCLUSION

This paper expands the complexity and performance of DBF with IL-BSP and compact, efficient bandpass delta-sigma ADCs. A digital beamformer with a 1 GHz center

frequency, 100 MHz bandwidth, and 16 elements generates four simultaneous beams. The prototype IC achieves 11.2 dB array gain and consumes only 20 mW/element. IL-BSP consumes 80% less power and occupies 80% less area compared to a conventional DSP implementation. The CTBPDSMs have 5 times higher bandwidth, 4 times higher center frequency, 1/3 area and 43% less energy per conversion than the ADCs in [8]. Thanks to DBF and accurate analog-to-digital conversion, the measured beam patterns, including single main lobe beam, two main lobes beam, and tapered beam, are near ideal.

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