

A Wideband Linear I/Q -Interleaving DDRM

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Abstract—This paper presents a wideband linear direct-digital RF modulator (DDRM) in 40-nm CMOS technology. An innovative I/Q -interleaving RF digital-to-analog converter (DAC) is proposed to enable the combination of in-phase (I) and quadrature (Q) signals in a more digital fashion, thereby improving the linearity performance at large bandwidths. The DDRM also features an advanced second-order hold digital interpolation filter to suppress the sampling spectral replicas in the presence of large bandwidth signals. Moreover, the harmonic rejection technique in the context of RF DAC operation is adopted and implemented. The 2×9 -bit DDRM core occupies 0.21 mm^2 and consumes 110 and 146 mW at 1 and 3 GHz, respectively, with the peak power of +9.2 dBm. The error vector magnitude (EVM) and adjacent channel power ratio (ACPR) at 3 GHz for a 57-MHz 64-QAM signal are better than -30 and -45 dB, respectively, and ACPR remains as low as -44 dBc up to a wide bandwidth of 113 MHz.

Index Terms—Carrier aggregation (CA), counter-intermodulation (C-IM), direct-digital RF modulator (DDRM), harmonic rejection (HR), IQ-interleaving, RF digital-to-analog converter (DAC), second-order hold (SOH).

I. INTRODUCTION

TO ENABLE high data rates, carrier aggregation (CA) can be used. The 4G long-term evolution advanced (LTE-A) standard allows up to five channels, each 20 MHz wide, to be dynamically allocated leading to an aggregated bandwidth of 100 MHz [1]. Moreover, a typical LTE-A transmitter (TX) is required to operate over multiple frequency bands (e.g., 0.7–3.8 GHz [1]). To address these demands, TX architectures are currently directed toward more digitally intensive implementations [2]–[20], as they can offer more reconfigurability as well as higher compatibility with nanoscale CMOS. Over the past decade, a number of digital in-phase/quadrature (I/Q) TXs that are capable of direct upconversion of the digital baseband (BB) signal to the desired RF carrier have been investigated [8], [10]–[12], [16], [17], [20]. Such direct-digital RF modulators (DDRM) [8] supersede the functionalities of

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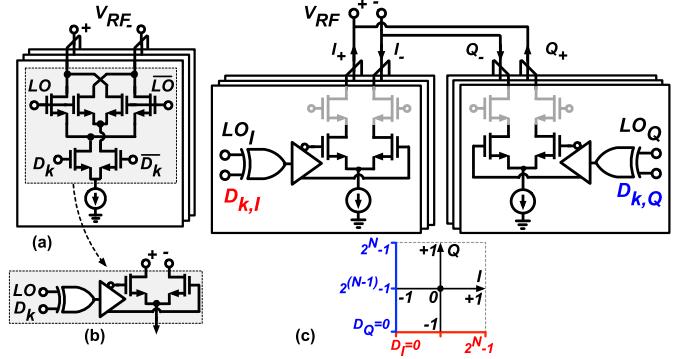


Fig. 1. (a) Gilbert-cell-based mixing DAC [15]. (b) Digital XOR-based mixing DAC [19]. (c) Possible I/Q RF DAC implementation using XORS and 50% LO.

BB I/Q digital-to-analog converters (DACs), low-pass filters, and mixers with two parallel-connected I/Q RF DACs [7].

We have recently proposed [21] a wideband linear DDRM architecture reconfigurable from 1 to 3 GHz. In this paper, we elaborate on the architecture analysis, system-/circuit-level design considerations, and extensive measurement results. Section II provides the background. The proposed architecture and its operating principles are presented in Section III. The circuit and layout implementation details are explained in Section IV, followed by the measurement results in Section V. Finally, the conclusions are drawn in Section VI.

II. BACKGROUND

Current-steering RF DACs, similar to that shown in Fig. 1(a), are the most promising candidates for high linearity at large bandwidths [15], [19]. However, a single RF DAC contains a large RF image component at $f_{\text{LO}} - f_{\text{in}}$ [15]. To address this issue, an I/Q modulator based on two I/Q RF DACs with parallel-connected Gilbert-cell mixers was proposed in [8] and [9], in which the upconverted I/Q signals were combined in an analog fashion by hardwiring all of the output drain nodes.

To move toward more digitally intensive realizations and benefit from advanced CMOS processes, the Gilbert-cell mixer can be replaced with differential switches and a digital XOR gate [19] similar to Fig. 1(b), and the I/Q modulation can be performed as in Fig. 1(c). In principle, when using XOR gates to upconvert the data by the local oscillator (LO) clock, the LO must have a 50% duty-cycle, and the I/Q data must be in *unsigned format* to correctly cover the four quadrants of the Cartesian plane. In the following, we analyze the challenges of (I/Q) RF DACs.

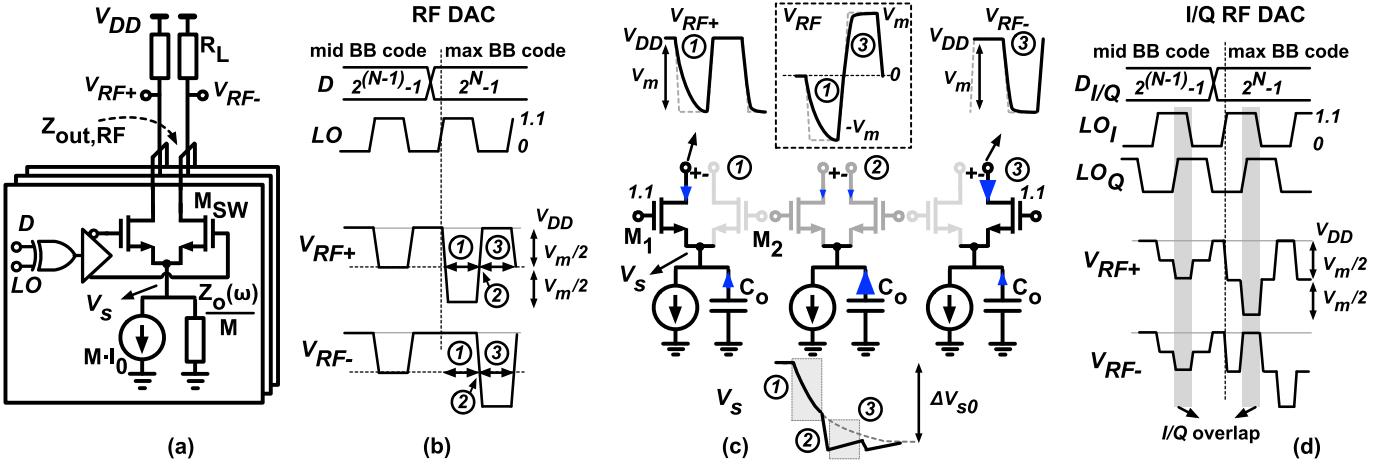


Fig. 2. (a) Simplified schematic of an RF DAC and (b) its example output waveforms for a large input code step. (c) Transients of an unary current cell of the RF DAC demonstrating faster settling behavior due to the LO switching operation. (d) Example output waveforms of an I/Q RF DAC in Fig. 1(c).

A. I/Q Summation and Nonlinearity

Two mechanisms are the primary sources of linearity degradation in DACs at high frequencies, namely, code-dependent switching transient (CDST) and code-dependent loading variation (CDLV) [22]–[25]. In a CDST effect, the output transition is strongly dependent on the previous signal sample (ISI) [25]. To eliminate the CDST effect in high-speed DACs, various return-to-zero (RZ) methods have been proposed [22], [24]–[26]. An RF DAC operates in a very similar fashion, offering the same advantage of the ISI alleviation [7].

The CDLV effect is caused by the finite output impedance of the current source (CS), denoted as \$Z_o\$ in Fig. 2(a). For non-RZ DACs, the third-order intermodulation distortion (IMD3) is proportional to \$(R_L N / |Z_o|)^2\$, where \$R_L\$ and \$N\$ are the DAC resistive load and the total number of current cells, respectively [23], [24]. At high output frequencies, \$|Z_o(\omega)| \approx 1/(\omega C_o)\$, indicating that \$C_o\$ becomes the main source of IMD3 degradation. However, in an RF DAC, the switching pair mixing operation alters the effective impedance seen at the RF side, denoted as \$Z_{out,RF}\$ in Fig. 2(a). Assuming an ideal switching behavior for \$M_{SW}\$ and following a similar approach to [27], \$Z_{out,RF}\$ can be found as being proportional to \$Z_o(\omega - \omega_{LO})\$ for a single current cell, which is basically upconverted \$Z_o(\omega)\$ to around the LO frequency. Consequently, the impedance in parallel to \$R_L\$ becomes proportional to \$1/((\omega - \omega_{LO})C_o)\$, which turns out to be large around \$\omega_{LO}\$, mitigating the CDLV effect.

Moreover, the presence of \$C_o\$ causes slower output settling, which is one of the main contributors to CDST and DAC linearity degradation at large bandwidths as well. Such a \$C_o\$-induced settling problem is more relaxed in the case of an RF DAC. This can be observed in Fig. 2(b) and (c), which illustrate an RF DAC settling behavior for a large input code step from \$2^{(N-1)} - 1\$ (zero differential output) to \$2^N - 1\$ (maximum output voltage). Fig. 2(c) shows the transients of one of the current cells right after the code step occurs, and it can explain the settling behavior of the RF DAC. During Phase 1, the current is steered to the plus

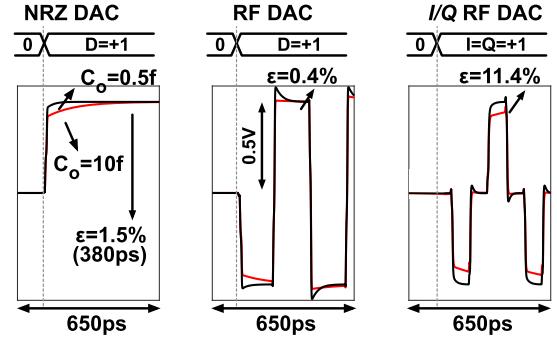


Fig. 3. Comparison of settling behaviors in different (RF) DACs.

side through \$M_1\$. As \$V_{RF+}\$ is decreasing, the \$M_1\$ source (\$V_S\$) is reduced as well in order to be able to provide sufficient current, compensating for the \$V_{DS}\$ drop by the increase of \$V_{GS}\$. However, due to \$C_o\$, such an increase of \$V_{GS}\$ occurs slowly. During the LO transition (Phase 2), the current quickly flows into \$C_o\$ causing a sudden negative jump on \$V_S\$. Once \$M_2\$ is switched ON, \$V_{RF-}\$ can settle faster and reach its final value due to the larger \$V_{GS}\$ value. Since such a transition is code-dependent, it can degrade linearity, especially at large modulation bandwidths. Fig. 3 shows the simulated Spectre transient output waveforms for a 9-bit segmented (RF) DAC with 6-bit thermometer coding, \$R_L = 50 \Omega\$, \$f_{LO} = 3\$ GHz, a switch size of \$1 \mu\text{m}/40 \text{ nm}\$, \$V_{DD} = 1.1\$ V, a differential output swing of 0.5 V, and two different values of \$C_o\$. It can be observed that, when the input code changes from 255 to 511, the RF DAC output settling error is approximately four times smaller than the NRZ DAC within the same time duration.

However, the linearity of I/Q RF DAC in Fig. 1(c) is prone to more severe deterioration in the presence of the aforementioned nonidealities. In general, the analog hardwiring \$I\$ and \$Q\$ summation [8]–[12], [18], [20] has a number of drawbacks. First, it can lead to excessive parasitics, mostly capacitive, at the output and attenuate the RF signal amplitude at high frequencies. Second, in both the \$I\$ and \$Q\$ paths, the switching

output elements (e.g., CSs) as well as the logics, clock, and data buffers may suffer from mismatch, limiting the intrinsic image-rejection ratio (IRR). Finally and most importantly, the overlap between the *I* and *Q* signals causes unwanted *I* and *Q* interaction that degrades the *I/Q* modulator error vector magnitude (EVM) [12] and linearity [11].

When aiming for high linearities, the *I* and *Q* interaction can be the primary source of linearity degradation. This can be explained by the output waveforms of the *I/Q* RF DAC in Fig. 1(c) as shown in Fig. 2(d). During the *I/Q* LO overlap time, both current branches [I_+/Q_+ or I_-/Q_- in Fig. 1(c)] can be connected simultaneously to the same side (V_{RF+} or V_{RF-}), intensifying the CDLV effect by dramatically lowering $Z_{out,RF}$. The CDST effect can be analyzed in a similar manner as that in Fig. 2(c) for a large input code change. It can be shown that, once M_2 begins to conduct, its drain voltage has already reduced to $V_{DD} - V_M/2$ (as opposed to V_{DD} in the case of the single RF DAC), which diminishes the transistor driving capability and gives rise to slower V_{RF-} transition from $V_{DD} - V_M/2$ to $V_{DD} - V_M$. Moreover, such a transition must be completed within only 25% of the clock cycle. The same situation occurs for the subsequent cycles, hindering proper output settling, as shown in Fig. 3. For the same C_o value as in the single RF DAC, the *I/Q* RF DAC in Fig. 1(c) settling is significantly slower.

To address the challenges of analog *I/Q* summation, the upconverted *I/Q* signals summation can be performed in the digital domain. References [28] and [29] exploit 25% duty-cycle LOs and time-division multiplex operation of the *I/Q* signals to drive a single power amplifier (PA) unit cell, and the multiplexer is implemented with transmission [28] or NAND gates [29]. Alternatively, [16] deploys 50% LOs to upconvert the *I/Q* signals and perform the summation via AND and OR gates, respectively, while requiring the *I/Q* signals to satisfy $|I| + |Q| \leq N$, where N is the total number of cells. This causes distortion and makes the use of digital pre-distortion (DPD) inevitable. To address this issue, a novel approach is discussed in Section III-A.

B. DDRM System Challenges

1) *Frequency Planning*: One possible DDRM configuration to support the LTE-A 5 × 20 MHz CA is to fix ω_{LO} to be located in the middle of the desired band and to shift each carrier component (CC) relative to ω_{LO} in the digital, leading to a low-digital-IF configuration. In a scenario when only one CC is active, the worst case can be located ±50 MHz away from the LO. Operating the DDRM in the arrangement of Fig. 4 with such a relatively large low-digital-IF imposes challenges on the DDRM linearity and spurious emissions, especially with the absence of any explicit BB and RF filters.

2) *C-IM Due to LO Harmonics*: Counter-intermodulation (C-IM) is a well-recognized distortion mechanism in TXs [30]–[34]. Similarly, the DDRM hard-switching mixing-operation can produce strong LO harmonics, making it prone to C-IM, especially when the DDRM is used as a pre-driver for an external PA stage as in Fig. 4. The C-IM distortion is caused by the intermodulation of the desired

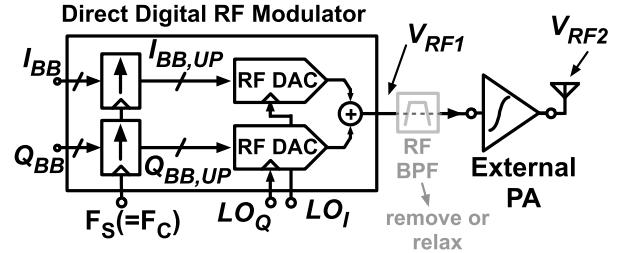


Fig. 4. Typical application of a generic DDRM. It is desirable to remove or relax the filtering between the DDRM and PA.

signal (at, e.g., $\omega_1 = \omega_c + \omega_{IF}$) with the unwanted components around the LO harmonics (e.g., third: $\omega_2 = 3\omega_c - \omega_{IF}$) through the nonlinear PA stage. Such an intermodulation product can fall back nearly to the desired signal frequency (e.g., $\omega_{C-IM3} = |2\omega_1 - \omega_2| = \omega_c - 3\omega_{in}$) as also shown in Fig. 5, which is very difficult to filter. In the LTE-A CA, the CC can be located ±50 MHz away from f_{LO} , and C-IM products fall out-of-band, where the spurious emission requirements are strict (−30 dBm/MHz [1, Sec. 6.6.4]). In the worst case scenario, the signal power can be concentrated in a single 200-kHz CC requiring C-IM level of −61 dBc for a TX with an average output power of +24 dBm (LTE-A pico-cell).

The C-IM level strongly depends on the PA nonlinearity and the level of unwanted components around the LO harmonics. For instance, in Fig. 4, C-IM3 can be expressed in terms of the power of components at ω_1 and ω_2 (P_{TX} and P_{H3LO}) and the PA OIP3 as

$$C-IMD3 \text{ (dBc)} = P_{TX} + P_{H3LO} - 2OIP3 \quad (1)$$

where the nonlinearity of PA is modeled with a (memoryless) third-order polynomial [$v_{RF2}(t) = \beta_1 v_{RF1}(t) + \beta_3 v_{RF1}^3(t)$] and $OIP3 = 10 \log(4\beta_1/3\beta_3)$ [35]. For the LTE-A base station (BS) application with $P_{TX} = +24$ dBm (average) and a typical OIP3 of +30–+40 dBm for the PA, it can be seen from (1) that P_{H3LO} should be 29–49 dB lower than P_{TX} to meet the C-IM3 requirement of −61 dBc.

To avoid the C-IM, several LO harmonic rejection (HR) techniques have been implemented by using either HR Gilbert-cell mixers [30] or shaping the LO to be closer to an ideal sinusoidal [6], [36] and minimize hard-switching. Since the third harmonic for an ideal square-wave LO is inherently 9.5 dB smaller than the fundamental, the HR technique should provide an extra suppression of 19.5–39.5 dB, respectively. In Section III-C, we have proposed an HR technique similar to [30] but based on *I/Q* RF DACs to suppress the LO third and fifth harmonics at the DDRM output.

3) *Complex Baseband Nonlinearity Effects*: The complex BB odd-order nonlinearity can also cause harmonic distortion (denoted as H_{3BB} and H_{5BB}) that, when upconverted to the RF, falls at the same frequency as the C-IM products [32] as shown in Fig. 5. Despite having the same frequency, such a distortion term has an entirely different source than the C-IM and does not require the LO harmonics or the PA nonlinearity. To prove this, we express the DDRM output as

$$v_{RF1}(t) = \Re\{y_{IQ}(t) \times LO_{IQ}(t)\} \quad (2)$$

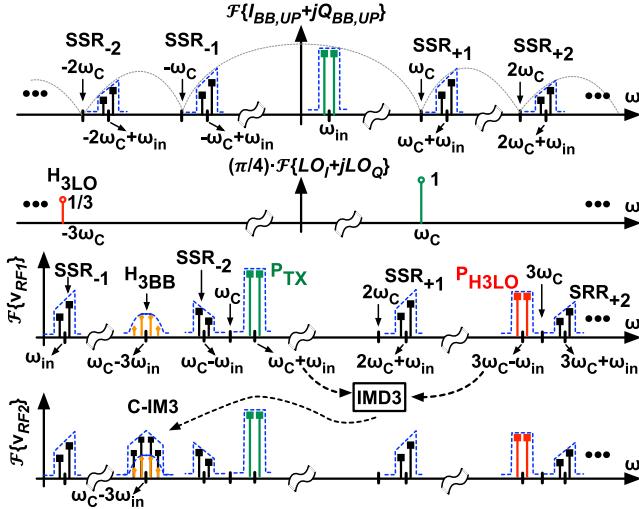


Fig. 5. Identifying various spurious components along the DDRM/PA chain.

where $\text{LO}_{IQ}(t)$ is the complex LO and $y_{IQ}(t)$ is the complex BB signal. Now let us approximate the BB nonlinearity for the I and Q paths separately as $y_{IQ}(t) \approx \alpha_1 x_{IQ}(t) + \alpha_3 x_{IQ}^3(t) + \dots$, where $x_{IQ}(t)$ are the ideal BB signals. Representing the low-digital-IF signal as $x_{IQ}(t) = e^{-j\omega_{in}t}$ and expanding the right-hand side up to the third-order-term only, the distorted BB signal can be written as $y_{IQ}(t) = (\alpha_1 + 3\alpha_3/4)e^{-j\omega_{in}t} + \alpha_3/4e^{j3\omega_{in}t}$. By replacing $y_{IQ}(t)$ in (2) and assuming a harmonic-free $\text{LO}_{IQ}(t) = e^{-j\omega_c t}$, the DDRM output is found to be $v_{RF1}(t) = \Re\{(\alpha_1 + 3\alpha_3/4)e^{-j(\omega_c + \omega_{in})t} + (\alpha_3/4)e^{-j(\omega_c - 3\omega_{in})t}\}$, which indicates that C-IM-like contents can already be produced at the DDRM output. In an (I/Q) RF DAC in the absence of analog BB blocks, we must emphasize that the RF DAC BB nonlinearity can arise from the CDLV/CDST effects as discussed earlier even though it might appear that the digital BB signal is directly upconverted to the RF and, hence, no BB distortion.

4) Sampling Spectral Replicas: The contamination of the DDRM output with sampling spectral replicas (SSRs) is another well-known issue, caused by the finite sample rate (F_{BB}) of the digital complex BB signals ($IQ[n]$) and the elimination of analog/RF reconstruction filters [3], [8], [10], [12], [14], [37]. The signal can be partly reconstructed in the digital by upsampling and digital filtering (interpolation) using a larger sampling frequency F_S , where F_S should be an integer ratio of the carrier frequency ($F_S = f_{LO}/N$) to avoid timing synchronization issues [10], [12]. Now, by expressing $y_{IQ}(t)$ in terms of $IQ[n]$ as $y_{IQ}(t) = \sum_{n=-\infty}^{+\infty} IQ[n]\delta(t - nT_S) * h_{DTCT}(t)$ [38] and replacing it in (2), we can find the analytical representation of the DDRM output as

$$V_{a,RF1}(\omega) = \frac{1}{T_S} \sum_{n=-\infty}^{+\infty} IQ(\omega - \omega_c - n\omega_S) \cdot \text{sinc}\left(\frac{\omega - \omega_c}{\omega_S}\right) \quad (3)$$

where $T_S = 1/F_S$, and we have assumed $\text{LO}_{IQ}(t) = e^{-j\omega_c t}$ and $h_{DTCT}(t)$, the impulse response of the DDRM, to be a zero-order hold (ZOH). If the complex BB signal is represented as a pure single tone at $\omega = +\omega_{in}$, we can see

from (3) that the output will contain replicas at $\omega = |\omega_{in} + \omega_c + n\omega_S|$ (n is an integer number) with an amplitude ratio equal to $|\text{sinc}(\omega_{in}/\omega_S + n)|$ while the desired fundamental located at $\omega = \omega_{in} + \omega_c$ for $n = 0$ and unwanted SSRs for $n \neq 0$, as shown in Fig. 5(b) for $\omega_c = \omega_S$. Most of these SSRs fall out-of-band and can cause spurious emission. However, we must point out that, for $n = -2\omega_c/\omega_S$, the SSR falls at $|\omega_{in} - \omega_c|$, which is the same frequency as the I/Q image component, limiting the inherent IRR (e.g., for $f_c = F_S = 2$ GHz and $f_{in} = \pm 50$ MHz, SSR₋₂ falls at the same location as the image, limiting IRR to -38 dBc). Note that, in general, mixing of higher odd LO harmonics with even SSRs, namely $\Re\{\text{SSR}_{\pm\text{even}} \times \text{LO}_{IQ,(\mp\text{odd})}\}$, folds back at $|\omega_{in} - \omega_c|$, e.g., SSR₊₆ \times LO_{IQ,(-7)} or SSR₋₄ \times LO_{IQ,(+5)}. Moreover, the mixing operation of $\Re\{\text{SSR}_{\pm\text{even}} \times \text{LO}_{IQ,(\pm\text{odd})}\}$ folds back at $|\omega_{in} + \omega_c|$, i.e., on top of the desired main tone.

It is obvious that in order to reduce the SSR-induced image component and out-of-band spurious emission, F_S should be as large as possible, with the maximum value determined by the digital interpolation filter speed, complexity, and power consumption.

III. PROPOSED ARCHITECTURE

A. Digital I/Q -Interleaving

To circumvent the problems associated with the I/Q RF DACs using two separate I/Q paths, an I/Q -interleaving technique based on 50% LO is proposed. In this technique, the I/Q data and LO bit-wise multiplication are carried out as XOR/XNOR gates and, subsequently, the upconverted I/Q signals are digitally combined using NOR gates to produce $(IQ)(LO)^+$ and $(IQ)(LO)^-$. In this configuration, as shown in Fig. 6(a), the CS is now shared between I and Q . The corresponding waveforms of a single current cell based on 50% LOs for all possible combinations of I/Q bits are shown in Fig. 6(b). Due to the used bit-wise X(N)OR/NOR logic, each unit-cell can generate a non-overlapping 25% duty-cycle output signal (v_{RF}) covering all four quadrants of the I/Q -plane. As $(IQ)(LO)^{+/-}$ is only active during 25% of the cycle, its complementary and differential values are not, in principle, the same, and hence, different logics are required to generate each. For the current-steering operation, M_1 (M_3) and M_2 (M_4) need to be driven with complementary signals that are simply generated by the logical NOT of $(IQ)(LO)^{+/-}$ signals. However, the differential RF output is generated by using XNOR and XOR to upconvert data by the LO, resulting in $(IQ)(LO)^+$ and $(IQ)(LO)^-$, respectively, as in Fig. 6(a).

When M_1 and M_4 are not active, the currents should be dumped into a constant voltage source (V_{dmy}) via M_2 and M_3 for an ideal current steering operation. Alternatively, to reduce the power dissipation during M_1 and M_4 idle duration, M_2 and M_3 in Fig. 6(a) can be removed, and M_1 and M_4 can be directly driven by $(IQ)(LO)^+$ and $(IQ)(LO)^-$, respectively. This allows the CS to switch OFF by going into the deep triode region, as shown in the switched CS (SCS) implementations in [13] and [20].

In the SCS operation, the CSs mainly determine the matching performance and the linearity similar to the

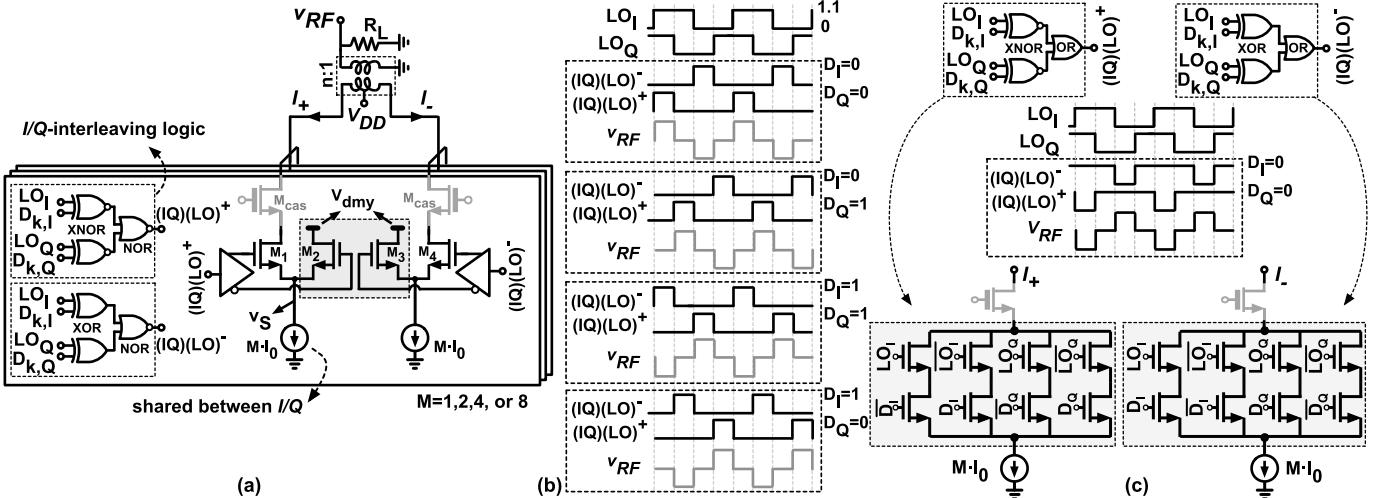


Fig. 6. Proposed I/Q -interleaving technique. (a) Possible current-steering realization using 25%-active operation. (b) Corresponding waveforms for the 25%-active operation. (c) 75%-active scheme with SCSs and current-mode realization of the I/Q -interleaving logic.

current-steering structure. This indicates that removing the CSs can lead to relatively large switches, hence, lower speed and increase in the power consumption of the driving buffers. Moreover, keeping the CSs allows more control over the output power range without impacting the RF DAC dynamic range.

It should be pointed out that the SCS operation can affect the CS speed, since V_S ideally has to drop to 0 V when the switch (M_{SW}) is not conducting and charge up again to the desired CS voltage overhead when M_{SW} is turned on. The presence of the parasitics over the CS can make V_S settling rather slow. Nonetheless, it does not necessarily lead to any linearity degradation compared with the current-steering operation. By using a (thick-oxide) cascode transistor (M_{cas}) on the top, the impact of (code-dependent) output voltage swing on the settling errors, hence, CDST and CDLV distortions, becomes very similar to both the SCS and current-steering operations. Moreover, as explained earlier, by using an XOR-based data and LO multiplication, only the on-period of the current cells is modulated (by 0°, 90°, 180°, or 360° depending on D_I/D_Q). Consequently, the output stage average current remains constant, and the unwanted code-dependent supply current modulation, which can also cause distortion, is avoided, as opposed to [13] and [20], which use AND gates to multiply data and LO.

The I/Q -interleaving logic in Fig. 6(a) can be alternatively implemented using OR gates instead of NOR gates, which means a 75% duty-cycle for $(IQ)(LO)^+$ and $(IQ)(LO)^-$, as shown in Fig. 6(c). An important advantage of the 75%-active scheme is that the XOR/OR and XNOR/OR gates can be realized as a current-mode logic with the minimum possible number of transistors by stacking it on the top of CSs, as shown in Fig. 6(c) (gray area). Such a minimal logic implementation can offer better matching performance, a more compact layout, and potentially less power consumption by re-using the output stage current, compared with a separate logic and output stage implementation at the cost of an extra V_{DSAT} drop in the output stage.

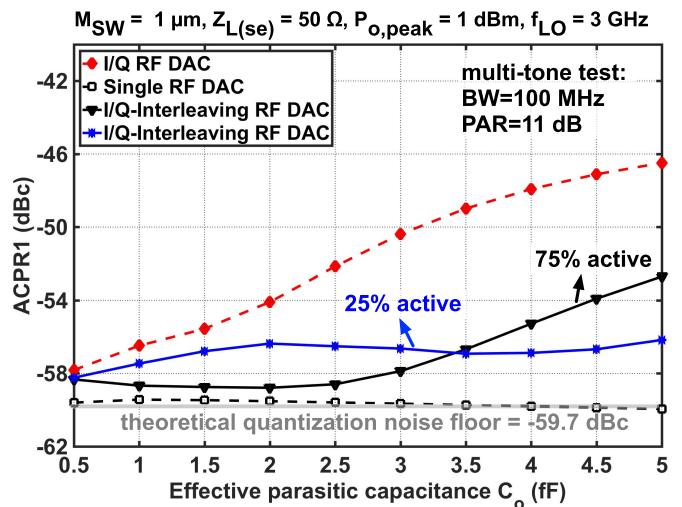


Fig. 7. Comparison between the simulated ACPR of the proposed 9-bit I/Q -interleaving RF DAC and the conventional (I/Q) RF DAC.

For both the 75%- and 25%-active schemes, the output maximum fundamental voltage remains the same and equal to

$$V_{RF(1st)} = (\sqrt{2}/\pi)2^N I_0 n R_L \quad (4)$$

where n , I_0 , R_L , and N are the output transformer impedance conversion ratios, unary-cell current, and the RF DAC number of bits, respectively. The (output drain) power consumptions, however, are different and are $P_{dc(75\%)} = (3/4)2^{N+1} I_0 V_{DD}$ and $P_{dc(25\%)} = (1/4)2^{N+1} I_0 V_{DD}$, respectively, excluding the power dissipated in V_{dmy} . Although the 75%-active scheme consumes three times more power than the 25%-scheme, it can save a considerable amount of power in the digital by re-using I_0 to implement the XOR/XNOR/OR gates. For the 75%-active scheme, the drain efficiency becomes equal to $\eta_{D(75\%)} = 2^{N+1}n^2 R_L I_0 / (3\pi^2 V_{DD})$, which theoretically

reaches $\approx 13.5\%$ (or, for the 25%-active scheme, up to 40.5%) assuming an ideal drain voltage with a differential fundamental value of $(2\sqrt{2}/\pi)V_{DD}$. Nevertheless, to maintain a sufficient voltage headroom on the CSs, we have selected a lower drain voltage swing at the cost of lowered efficiency.

Fig. 7 shows the simulated linearity of the proposed I/Q -interleaving RF DAC in case of both 75%- and 25%-active schemes compared with the I/Q RF DAC in Fig. 1(c) and the single RF DAC [one branch of I/Q RF DAC in Fig. 1(c)]. For a fair comparison, the fundamental output power, the switch (W/L), and the output resistive load are all maintained the same for all the RF DAC configurations. Note that, for the same output power and $V_{DD} = 1.1$ V, I_0 of the I/Q -interleaving RF DAC should be two times larger than I_0 of the I/Q RF DAC due to the elimination of one I or Q bank. The linearity improvement is clearly evident as C_o increases and, for $C_o = 5$ fF, it is up to 6 and 10 dB for the 75% and 25%-active schemes, respectively. Such improvement originates from the reduced CDLV and CDST effects. The former arises from the fact that fewer branches are now connected at the same time to the output node. This results in larger $Z_{out,RF}$ as indicated in Fig. 2(a). The latter can be explained by noting that, when M_1 or M_4 is OFF, V_S settles to a value that is rather independent of the output, and hence, there is a mitigation of the ISI effect.

Despite its linearity improvement advantage over the I/Q RF DAC with 50% LO, the proposed I/Q -interleaving approach can cause relatively large common-mode (CM) components around the even-order LO harmonics due to the 75% or 25% duty-cycle of the I/Q -interleaved pulses. Although such even-order CM components can be cancelled in the differential-mode, their suppression will strongly depend on the CM rejection (CMR) of the output balun/transformer at those frequencies. Note that, this issue also applies to all of the TXs based on the 25% duty-cycle LO.

Both the 75% and 25% schemes have their own (dis-)advantages and, depending on the output power requirement, operating frequency, and the technology node, one scheme might be preferred over the other. In our prototype DDRM, the 75% configuration was adopted mainly, because it allowed us to make the I/Q -interleaving logic very compact and combine it with the output stage for a better speed and matching performance. In the 25%-active scheme, the combined structure will introduce a strong asymmetry with respect to the I/Q data and LO path due to the required AND operation, and hence, the image rejection performance will degrade. Consequently, the logic must be implemented separately, which requires more stages of logic and transistors, thus causing more timing mismatch and slower transitions. The 25% scheme is particularly advantageous in a more advanced technology nodes where the logics have higher speed and better matching for a given area.

B. High-Speed Digital Interpolation Filter

For a wideband suppression of the SSRs, first-order hold (FOH) and second-order hold (SOH) interpolation FIR filters with $sinc^2$ and $sinc^3$ transfer functions, respectively, are

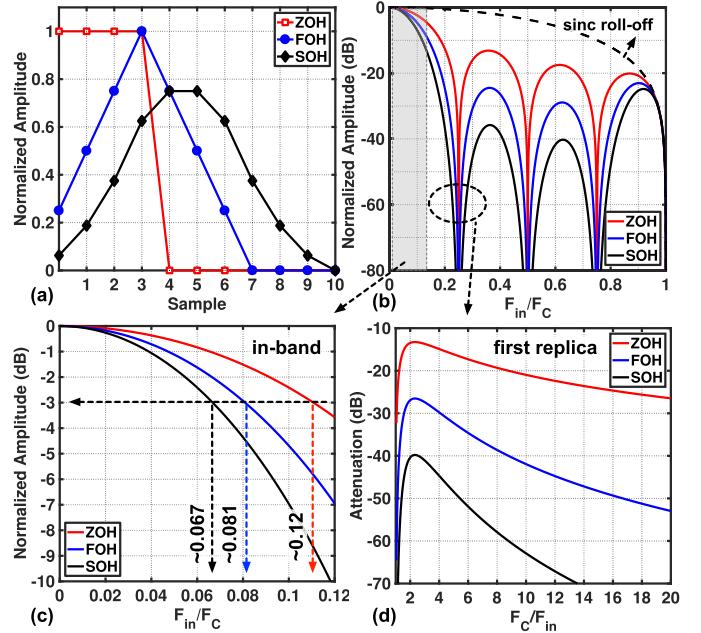


Fig. 8. ZOH versus FOH versus SOH. (a) Impulse response. (b) Magnitude response. (c) In-band magnitude response. (d) First replica attenuation.

proposed. The filter is deployed to upsample the complex BB signals at F_{BB} by a factor of $n = 4$ up to $F_S (=f_c)$ and suppress the SSRs located $n \cdot F_{BB}$ away from f_c below the modulator noise floor. The selection of F_{BB} and the upsampling factor balances the SSRs location, data path power consumption, and the filter complexity.

The impulse response of a ZOH interpolation filter with an upsampling factor of N can be expressed as $h_{ZOH}[n] = \sum_{i=0}^{N-1} \delta(n-i)$. The FOH filter can be built by the convolution of two consecutive ZOHs, namely, $h_{FOH}[n] = (h_{ZOH}[n] * h_{ZOH}[n])/N$. Likewise, the SOH can be constructed by cascading three ZOHs, resulting in $h_{SOH}[n] = (h_{FOH}[n] * h_{ZOH}[n])/N$. Equivalently, in the frequency domain, their (voltage) transfer functions are $sinc$, $sinc^2$, and $sinc^3$, respectively. For $N = 4$, the FOH coefficients are $c_3 = 1$ and $c_{0..2} = c_{6..4} = 0.25, 0.5$, and 0.75 . Similarly, the SOH coefficients are $c_{0..4} = c_{9..5} = 0.0625, 0.1875, 0.375, 0.625$, and 0.75 . Note that deriving the coefficients in this manner always results in signed power-of-two terms that can be implemented in a more power and area-efficient manner using adders and bit shift operation [4]. The impulse and magnitude responses are also shown in Fig. 8. As a tradeoff between the in-band distortion and out-of-band replica suppression, we can choose between the ZOH, FOH, or SOH filters.

For a power-efficient implementation, an equivalent polyphase structure can be simply used by decomposing the filter into four parallel sub-filters, as shown in Fig. 9. Using the z -domain representation, the polyphase structure for $N = 4$ can be expressed as $H(z) = E_0(z^4) + z^{-1}E_1(z^4) + z^{-2}E_2(z^4) + z^{-3}E_3(z^4)$, where $E_{0..3}$ are the polyphase components, and, for the SOH filter, are $E_0(z) = c_0 + c_4 z^{-1} + c_8 z^{-2}$, $E_1(z) = c_1 + c_5 z^{-1} + c_9 z^{-2}$, $E_2(z) = c_2 + c_6 z^{-1}$, and $E_3(z) = c_3 + c_7 z^{-1}$. One possible realization of $E_{0..3}$ for the SOH filter that

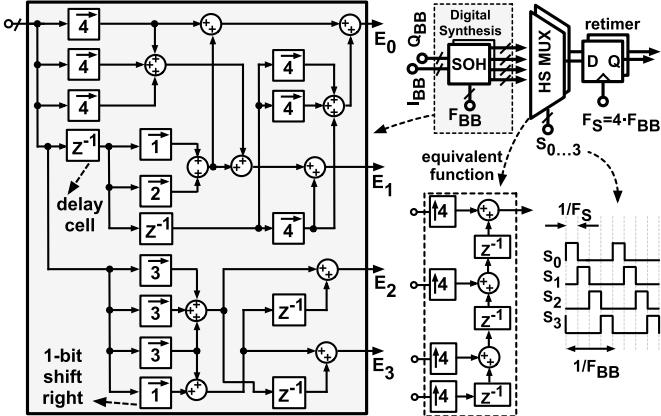


Fig. 9. Implementation details of the SOH filter.

results in the minimum number of delay and shift operations is shown in Fig. 9. Note that the $4 \times$ upsampling process in realizing $H(z)$ generates three zeros and merely one sample of the input signal during one period of the BB data. As a result, the upsampling and summing operation can be effectively implemented using a multiplexer operating at $4 \times F_{BB}$ while the remainder of the filter, namely $E_{0..3}$ branches, operates at F_{BB} . Doing so remarkably simplifies the filter design and reduces power consumption. More importantly, at $4 \times F_{BB}$, the suppression of the interpolation filter is again back to ZOH operation, meaning that any interpolation filter can only suppress the replicas below its final upsampling rate. One of the advantages of the proposed filter structure is that it can directly extend into higher order hold by cascading more ZOH functions.

C. Harmonic Cancellation I/Q-Interleaving RF DACs

The proposed DDRM also incorporates a multi-phase LO HR technique to attenuate the third/fifth harmonics, hence avoiding C-IMD3 and C-IMD5, respectively. For this purpose, three parallel-connected I/Q -interleaving RF DACs based on the 75%-active scheme and current re-used logic are used. The RF DACs are driven by the same digital I/Q signals but different LO phases of $(0^\circ, 45^\circ, 90^\circ)$ together with current scaling factors of $(1, \sqrt{2}, 1)$. It should be noted that the multi-phase LO approach was first demonstrated in [30] using conventional (Gilbert cell) mixers. However, in this paper, for the first time, the multi-phase LO HR is implemented with RF DACs using the same principle. The HR operation principle can be mathematically described as $v_{a,\text{RF}1}(t) = y_{IQ}(t) \times (\text{LO}_{IQ(0)}(t) + \sqrt{2}\text{LO}_{IQ(45)}(t) + \text{LO}_{IQ(90)}(t))$. By using $\text{LO}_{IQ}(t) = (4/\pi) \sum_{n=1}^{\infty} (e^{(-1)^n j(2n-1)\omega_c t})/(2n-1)$, the coefficients of fundamental, third, fifth, and seventh harmonics are given by $|1 + \sqrt{2}e^{-j\pi/4} + e^{-j\pi/2}| = 2\sqrt{2}$, $|1 + \sqrt{2}e^{+j3\pi/4} + e^{+j3\pi/2}| = 0$, $|1 + \sqrt{2}e^{-j5\pi/4} + e^{-j5\pi/2}| = 0$, and $|1 + \sqrt{2}e^{+j7\pi/4} + e^{+j7\pi/2}| = 2\sqrt{2}$, respectively. Evidently, the third and fifth harmonics are cancelled out, while the fundamental and seventh harmonics are constructively added, resulting in $2\sqrt{2}$ larger amplitude.

Any error in the actual circuit implementation of the $\sqrt{2}$ scaling factor (ϵ_s) will limit the third/fifth HR to \approx

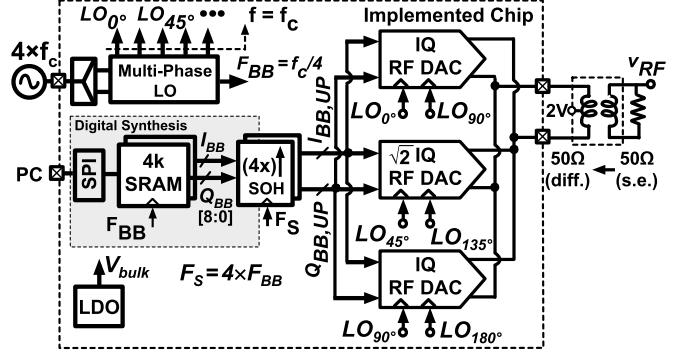


Fig. 10. Top-level architecture of the implemented DDRM.

$20 \log(\epsilon_s/2)$ (in excess to the inherent 9.5/14 dB HR3/5). Thus, to meet the third harmonic suppression requirement of 29–49 dB (see Section II-B2), $|\epsilon_s|$ must be less than 21.2%–2%, which is rather easily achievable without any type of calibration techniques. The HR limit due to only the LO phase error can also be approximated as $-10 \log_{10}(2\epsilon_{45^\circ}^2 + \epsilon_{90^\circ}^2 - 2\epsilon_{45^\circ}\epsilon_{90^\circ})$, where ϵ_{45° and ϵ_{90° are the errors (in radians) in the 45° and 90° LO phases, respectively. To also meet 29–49 dB of HR requirement, the LO phase error (assuming $\epsilon_{45^\circ} \approx \epsilon_{90^\circ}$) must be less than 2–0.2°, respectively.

The $\sqrt{2}$ factor is implemented by maintaining the same W/L value for the transistors used to realize I_0 and only scaling the bias voltage. Although this entails larger V_{DSAT} and more voltage headroom for the CSs, it is better for the matching between the CSs and avoids excessive parasitic capacitance. To mitigate the crosstalk between various branches with different phases, thick-oxide cascode transistors locally placed per each cell are also used.

IV. IMPLEMENTATION DETAILS

The block diagram of the proposed DDRM based on the HR I/Q -interleaving RF DACs is revealed in Fig. 10. In this proof-of-concept implementation, a resolution of 2×9 -bit (per I/Q) is selected as a tradeoff between the in-band linearity, far-out noise, power consumption, and the overall complexity of the DDRM. The quantization noise power spectrum density (PSD) (N_{PSD}) around the carrier for an N -bit I/Q RF DAC with a data sample of F_S (after upsampling and interpolation) is given by

$$N_{PSD} (\text{dBc/Hz}) = - \left(6.02N + 1.76 + 10 \log_{10} \left(\frac{F_S}{2} \right) + 3 \right) \quad (5)$$

where the 3-dB factor arises from the I and Q operation. For $N = 9$ and F_S of 1.8 GSps, N_{PSD} will be -148.5 dBc. While this is not sufficient to meet the stringent spurious emission limits that are typically required for frequency division duplex operations (e.g., LTE-A Home BS TX requires -138 dBm/Hz [1, Sec. 6.6.4.2] or -169 dBc/Hz for a peak power of $+31$ dBm), it provides a dynamic range of >54.9 dB¹ (with a target BW, PAR, and F_S of 100 MHz,

¹quantization-noise-limited DR of the DDRM is given by $-N_{PSD} - \text{PAR} - 10 \log_{10}(\text{BW})$, where BW and PAR are the occupied signal bandwidth and peak-to-average ratio, respectively.

11 dB, and ≥ 1 GSps, respectively), which has a sufficient margin for meeting the stringent in-band spectral requirement [e.g., adjacent channel power ratio (ACPR) of -45 dBc for LTE-A BS]. Although it is beyond the scope of this paper, several techniques exist [10], [14], [39]–[41] that aim at improving the digital TX out-of-band noise. One such technique is using digital $\Delta\Sigma$ modulation [41] to suppress the noise at a particular frequency offset from the TX band rather than merely increasing the number of bits, which would impose stringent requirements on the matching and timing errors, hence, power consumption and area.

As a tradeoff between the advantages of a fully thermometer-coded design, such as relaxed matching requirements and reduced switching glitches, and that of a fully binary-coded design, such as lower area and complexity [23], a segmented structure with 3-bit binary-coded LSB and 6-bit thermometer-coded MSB cells were adopted. The digital I/Q BB data are stored on two 4-K SRAMs with a sample-rate of $F_{BB} = f_{LO}/4$, which are programmed through the low-speed SPI interface. The output balun is placed off-chip. Since the DDRM output power and the CMR depend on the balun characteristics, after testing a few off-the-shelf balun designs, a wideband $50\text{-}\Omega$ single-ended to $50\text{-}\Omega$ differential balun ($n = 1$) with an insertion loss of around 1 dB and an input S_{11} of <-14 dB over 1–3 GHz response was selected. Although a larger n is expected to increase the output power according to (4), it also increases the load seen by the RF DAC to $n^2 R_L$ and affects the output RF bandwidth.

A. Output Stage

The implementation of the output stage, which is based on the 75%-active scheme with the combined logic topology, and the corresponding device sizes are detailed in Fig. 11(a). The unit-cell current (I_0) is set by a current mirror consisting of M_1/M_2 , which, as mentioned earlier, is shared between the I/Q paths. I_0 is adjustable by an off-chip reference current (I_{REF}) and a digitally programmable current mirror. For the final measurements, I_0 is set to approximately $11 \mu\text{A}$, resulting in a total output current of $\approx 30 \text{ mA}$ for the three HR RF DACs².

Stacking M_{SW1} and M_{SW2} in the output stage introduces an extra voltage drop of 200 mV ($=V_{DSAT}$ of M_{SW2}), causing $\approx 6\text{-mW}$ extra power consumption in the output stage. Based on our estimation of the separate logic and output-stage topology, combining the logic into the output stage not only offers better performance but also saves at least 22.5 mW.

M_1/M_2 sizes are determined as a tradeoff between the mismatch, total area, and their drain parasitic capacitance. The matching requirement is determined by simulating the linearity and noise-floor degradation as a function of MOS CSs mismatch of a 9-bit, otherwise ideal, RF DAC with $F_S = 3$ GSps and an arbitrary 100-MHz input signal with 11-dB PAR. The unit ($1\times$) current cell was designed and

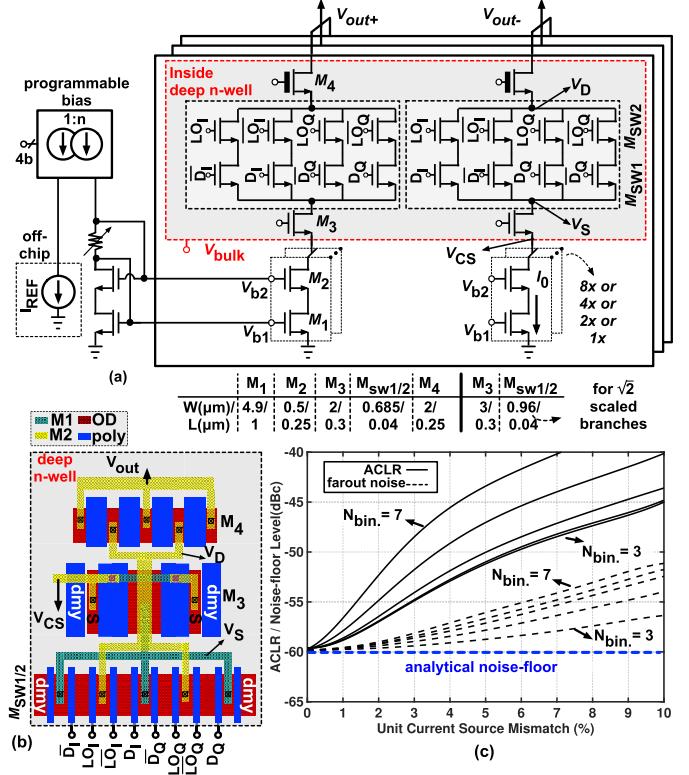


Fig. 11. Unit cell (a) circuit implementation and (b) layout. (c) System-level simulation of linearity versus CS mismatch for a 9-bit RF DAC.

implemented for a mismatch standard deviation of around 4%, resulting in a mismatch-induced ACLR limit of -53 dBc.

A W/L value of $685 \text{ nm}/40 \text{ nm}$ is selected for M_{SW1} and M_{SW2} to have V_{DSAT} of around 200 mV and a contribution of less than 10% to the unary cells mismatch. The placement and layout of the core device was fulfilled with utmost care to avoid excessive parasitics. M_3 sufficiently shields the source of switching transistors (M_{SW}) from the drain parasitic capacitance of M_2 , thereby improving the linearity performance at high frequencies. A customized compact layout for the switching transistors, M_3 and M_4 , shown in Fig. 11(c) helps to further minimize the parasitics. By avoiding the unnecessary metal contacts to the shared node of M_{SW1} and M_{SW2} , the parasitics were kept limited to the minimum possible junction capacitance. According to the post-layout extractions, the parasitic capacitance on V_S and V_{CS} (of a thermometer-coded cell) are also less than 2.5 and 15 fF, respectively.

The $\sqrt{2}$ factor for HR is implemented by properly scaling V_{b1} and V_{b2} via the current mirror as well as M_3 and M_{SW} widths. Sufficient voltage headroom over all of the cascode devices is provided by choosing V_{DD} of 2 V. To withstand large voltage swings at the output nodes and alleviate interaction between DAC branches, thick-oxide cascode devices (M_4) are locally utilized per each cell.

B. Floorplan and LO Distribution

For a compact layout and sufficient isolation between the analog and digital, the switching core with its corresponding

²The total output current for the 75%-active scheme HR RF DACs is equal to $I_{dc(75\%)} = (3/4)2^{N+1}I_0(2 + \sqrt{2})$, where the $(2 + \sqrt{2})$ factor arises from the HR implementation.

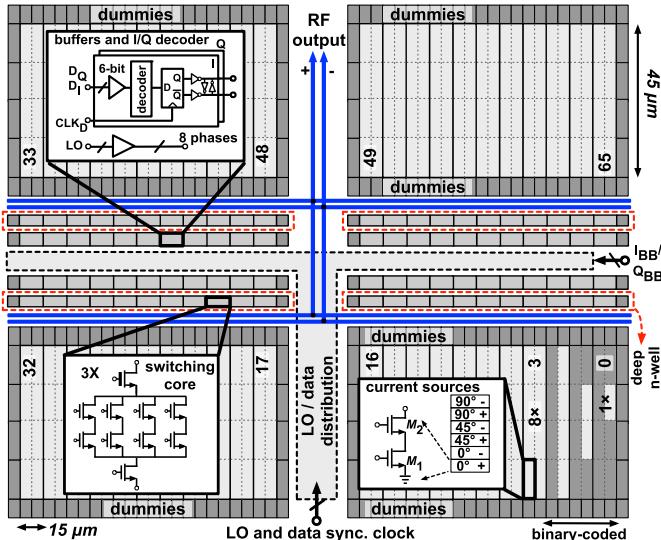


Fig. 12. DDRM floorplan.

logic and the CSs were separately placed as shown in Fig. 12. The DDRM core is split into three major parts, namely, 65 unary cells of the cascaded CSs along with 64 unit cells of the miniature *I/Q* modulator in conjunction with 64 unary cells of a small *I/Q* digital decoder. All of the CSs that are required for the HR were juxtaposed for the best matching performance. The single-row binary-to-thermometer decoder logic was implemented locally per each unit cell in order to reduce the digital *I/Q* data routing. To avoid glitches due to the decoder logic, the digital bitstream was also re-timed at each unit cell, which slightly increased the overall power consumption. As a tradeoff between the errors due to the clock propagation delay and the area, complexity, and power consumption of the distribution network, instead of a fully binary tree [15], the LO tree was broken into four sections, distributed over one metal layer and driven by four global LO buffers. Since, for the HR technique, the required number of LO lines will increase by a factor of four compared with a single (RF) DAC, it was crucial to simplify the LO tree to avoid excessive parasitics and power dissipation at the cost of a systematic delay error of up to ± 1 ps based on the RC extractions. Based on the Monte Carlo simulations, the standard deviation (1σ) of timing mismatch between the global LO buffers was also around 1.2 ps. Moreover, to mitigate the crosstalk mainly caused by capacitive coupling, ground lines were placed in the middle of different LO phases.

V. MEASUREMENT RESULTS

The proposed DDRM was implemented as a proof-of-concept in a 40-nm low power digital CMOS process. The DDRM core composed of the CS arrays, the decoders and switches, and the interpolation filter, and the LO and *I/Q* data distribution network occupies an area of 0.21 mm^2 as shown in Fig. 13(a). The entire digital BB front end and the multi-phase clock circuit are shared with other TX designs implemented on the same die. Consequently, their area and power consumption are not particularly optimized for the DDRM. The low-speed part of the interpolation filter is also

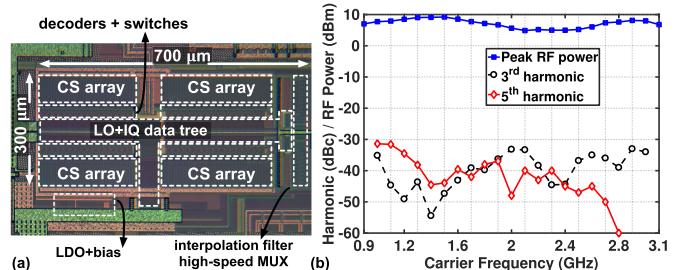


Fig. 13. (a) Chip microphotograph of the DDRM. (b) Measured peak RF output power (with an input static code of $I_{BB} = Q_{BB} = 511$) and HR (with two-tone input signal) versus f_{LO} .

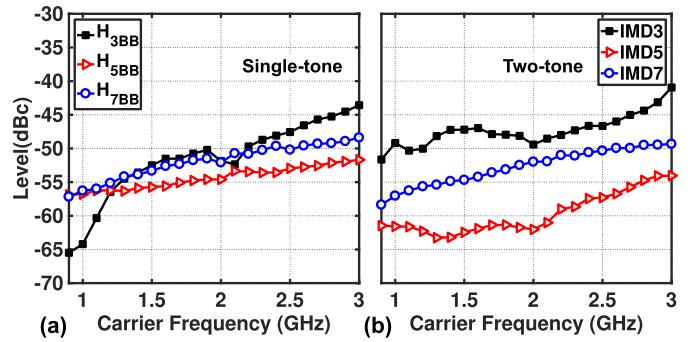


Fig. 14. Measured BB distortion for (a) one-tone and (b) two-tone signals.

implemented on the same digitally synthesized sea-of-gates. The LO generation consumes from 17 to 29 mW at $f_{LO} = 1\text{--}3$ GHz. The output draws 35–29 mA at $f_{LO} = 1\text{--}3$ GHz from a 2-V supply, and the LO and data buffers, decoders, and the high-speed part of the interpolation filter draw 36–80 mA at $f_{LO} = 1\text{--}3$ GHz from a 1.1-V supply.

Fig. 13(b) shows the peak output power measured over a frequency range of 0.9–3.125 GHz with an input static code of $I_{BB} = Q_{BB} = 511$. The maximum achieved drain efficiency, defined as $P_{out,peak}/P_{dc,out}$, and the output power occurs at 1.5 GHz and reaches 13% and +9.2 dBm, respectively, after deembedding the measurement setup loss of 1.7 dB. The RF power variation over the entire frequency range is less than 5 dB and is mainly caused by the output parasitics and the balun.

Fig. 14(a) and (b) shows the measured BB distortion levels across f_{LO} for single- and two-tone signals, respectively. We should emphasize that, since the results pertain to the output of DDRM (without PA), the C-IMD-like products (referred to as H_{BB}) are caused by the complex BB nonlinearity (see Section II-B3). Up to 3 GHz, H_{3BB} and IMD3 remain below -44 and -41 dBc, respectively. Based on the measured P_{out} and IMD3 value at 3 GHz, the corresponding OIP3 value is around +25.2 dBm. The *I/Q* image and LO feedthrough are -49 and -39 dBc, respectively, whereby both can be reduced to below -66 dBc after a simple *I/Q* gain and dc offset correction. The uncalibrated third/fifth HR, shown in Fig. 13(b) for a two-tone signal, remains better than 30 dBc over the entire frequency range, including 9.5 dB/14 dB of the inherent third/fifth harmonic attenuation.

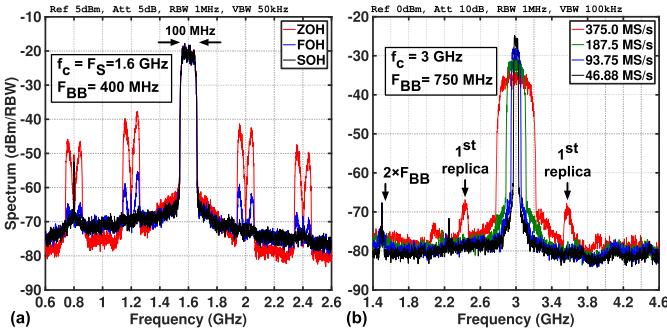


Fig. 15. Measured (a) suppression of SSRs using the SOH filter and (b) RF spectrum for various symbol rates at 3 GHz using the SOH filter.

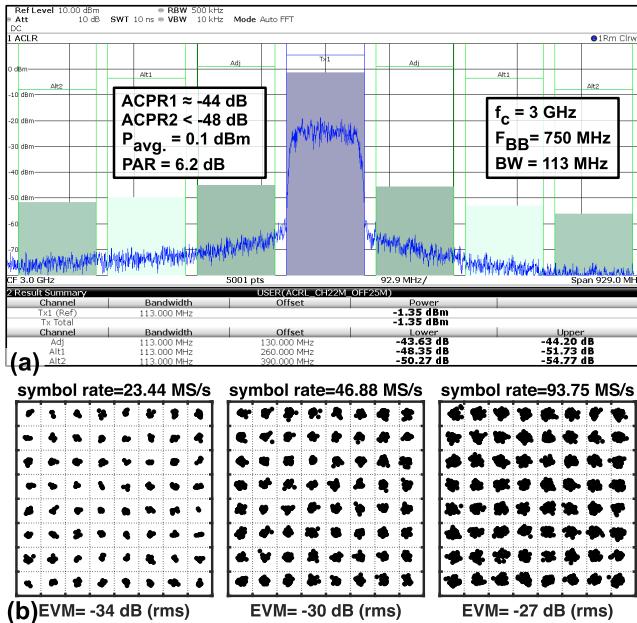


Fig. 16. (a) SC 93.75-MS/s 64-QAM ACPR at 3 GHz. (b) Measured constellation points and EVM at $f_{LO} = 3$ GHz versus the symbol rate.

The effectiveness of the SOH filter on the suppression of wideband SSRs is demonstrated in Fig. 15 where an arbitrary single-carrier (SC) 100-MHz 64-QAM signal with $F_s = 400$ MS/s is applied to the DDRM, and the interpolation filter order is varied. The SOH filter achieves a suppression of more than 30 dB compared with a ZOH for such a wideband signal and can bury the SSRs below the output noise floor.

Fig. 16 shows the spectrum for an SC 113-MHz 64-QAM signal at $f_{LO} = 3$ GHz. Without employing any types of DPD techniques, ACPR1 and ACPR2 are -44 and <-48 dBc, respectively. The measured output spectrum for multiple symbol rates is also shown in Fig. 15, which clearly demonstrates the in-band roll-off due to the sinc^3 function as well as the suppression of the closest SSR below the noise floor up to a bandwidth of around 200 MHz. The DDRM constellation points and EVM for an SC 64-QAM at 3 GHz are also shown in Fig. 16. The EVM is -34 dB (rms) for a symbol rate of 23.44 MS/s and degrades to -27 dB (rms) at 93.75-MS/s symbol rate. The in-band amplitude distortion due to the SOH filter sinc^3 response (see Section III-B) partly accounts for

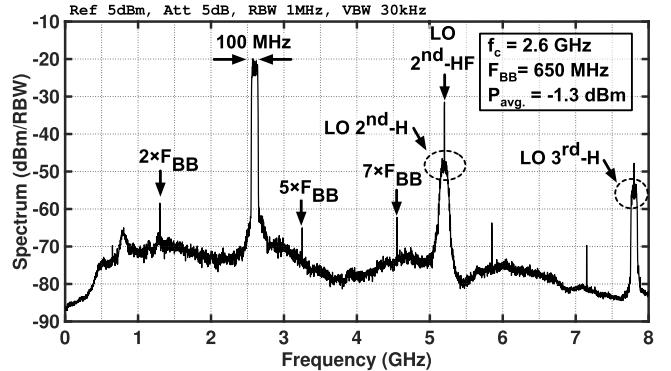


Fig. 17. Measured far-out spectrum of an SC 64-QAM signal.

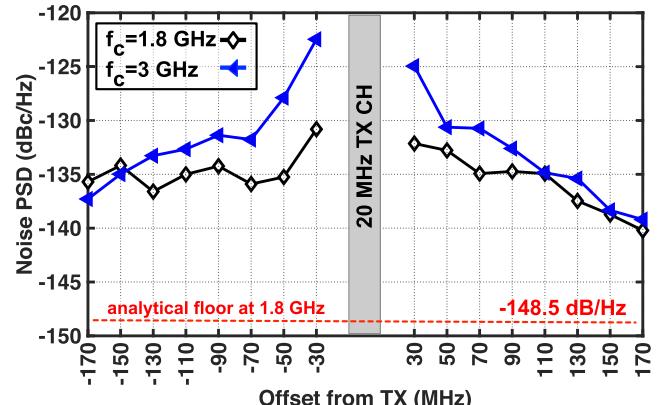


Fig. 18. Measured noise in the RX band as a function of the offset frequency.

such degradation (an ideal DDRM system simulation with an SOH filter predicts an EVM of -33 dB at 93.75 MS/s). It should be noted that a multi-carrier modulation scheme (e.g., OFDM in the case of LTE) is less sensitive to the SOH filter distortion at wide bandwidths.

The spectrum of a 100-MHz SC QAM signal from dc to 8 GHz is shown in Fig. 17, showing the attenuated LO harmonics and no visible SSRs. The large second LO harmonic in Fig. 17 is mainly caused by the 75% duty-cycle that leads to relatively large even-order CM output components and the poor CMR of the chosen balun (<10 dB at frequencies above 4 GHz). By using a different off-chip balun with a CMR of 30 dB at 4.6 GHz, the second harmonic level could be improved from -24 to -38 dBc at $f_{LO} = 2.3$ GHz. The harmonics of the digital BB clock (F_{BB}) are also visible in the spectrum, which is partly due to the parasitic coupling between the shared digital supplies and partly due to the coupling via the substrate. The $n \times F_{BB}$ spurs can either directly appear at the output or get upconverted by f_{LO} (and its harmonics) and appear at $|m \times f_{LO} \pm n \times F_{BB}|$. For the particular chosen f_{LO} of 2.6 GHz in Fig. 17, only $1 \times$, $2 \times$, $5 \times$, $7 \times$, $9 \times$, and $11 \times F_{BB}$ spurs are present ($4 \times$ and $8 \times$ fall on top of the desired signal and its second harmonic, respectively). For a different f_{LO} of 2.3 or 3 GHz, all of the F_{BB} spurs also appear.

The measured output noise at 1.8 GHz with static input I/Q code ($I_{BB} = Q_{BB} = 511$) is between -145 and -150 dBc from 10- to 100-MHz offset frequency and reaches -155 dBc

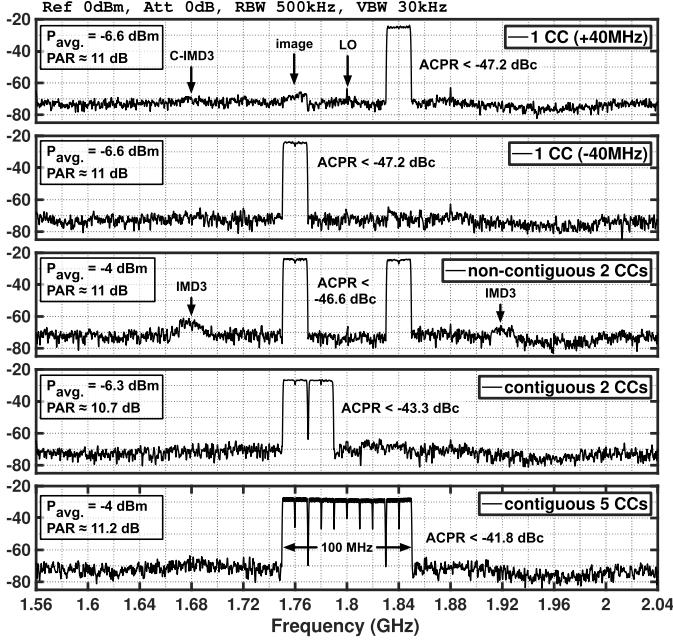


Fig. 19. Measured multi-tone CA spectrum with various 20-MHz CC arrangements at $f_{\text{LO}} = 1.8$ GHz ($F_{\text{BB}} = 450$ MSps).

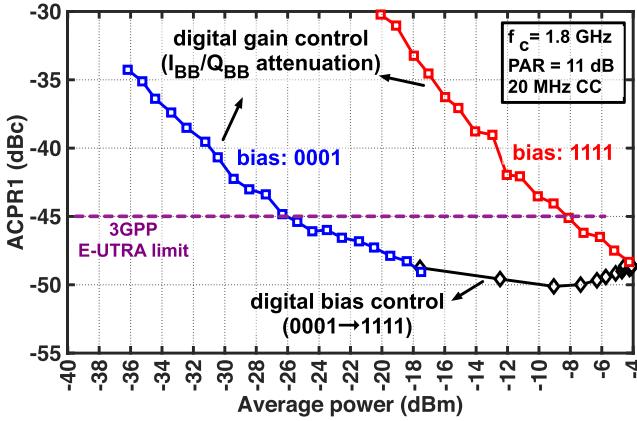


Fig. 20. Measured ACPR as a function of the average output power.

at 300 MHz, which is dominated by the (thermal) noise of the CSs, the LO buffers, and the multi-phase clock generation circuitry. The DDRM noise with a modulated carrier (≈ 20 -MHz 64-QAM) at various frequency offsets is also measured and shown in Fig. 18. The rather significant ≈ 10 dB difference between the measured noise floor and its theoretical value (-148.5 dBc with $f_{\text{LO}} = 1.8$ GHz) arises from the error mechanisms such as the mismatch between the CSs and switching transistors, and the timing errors caused by the LO buffers mismatch that can degrade the close-in linearity as well as the far-out noise.

To demonstrate the CA capability, the DDRM was tested with multiple CCs at a 1.8-GHz band as shown in Fig. 19. Constrained by the SRAMs size, the performance could not be measured with an actual LTE signal. However, in lieu of the 20-MHz LTE CCs, a multi-tone signal with a PAR of 11 dB and a bandwidth of 18 MHz was incorporated. For a single CC

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR ART

| Parameter | This work | [14] | [17] | [42] | [15] | [20] |
|---------------------------|-----------------|----------|--------------------|--------------------|---------------------|----------|
| Architecture | DDRM | QDAC | RQDAC | DDRM | RF DAC | DDRM |
| Process | nm | 40 | 28 | 28 | 65 | 65 |
| Core area | mm ² | 0.21 | 0.25 | 0.22 | 0.18 | 1.6 |
| Balun/Inductor | | off-chip | off-chip | off-chip | off-chip | off-chip |
| Resolution | bit | 9-IQ | 10-IQ | 12-IQ | 9-IQ | 16 |
| Peak P_{RF} | dBm | +9.2 | +8 | +3.5 | +11.9 | -8 |
| Peak $\eta_{\text{sys.}}$ | % | 7 | 15.3 | 1.8 ^(d) | 6.8 | 0.04 |
| f_{LO} | GHz | 0.9 | 3 | 1 | 2.4 | 1.9/4.1 |
| F_{BB} | MHz | 250 | 750 | 128 | 500 | 860 |
| P_{DC} | mW | 110 | 146 ^(a) | 41.3 | 24.8 | 227 |
| I/Q image | dBc | -45 | -49 | -44 | -44 | N/A |
| C-IMD | dBc | -56 | -44 | <-50 | <-50 ^(d) | N/A |
| Modulation | | 64QAM | M-T ^(b) | M-T ^(b) | LTE | LTE |
| Bandwidth | MHz | 18 | 57 | 18 | 18 | 18 |
| $P_{\text{avg.}}$ | dBm | -0.3 | +1 | +1 | -3.87 | +2.5 |
| ACPR1 | dB | -50 | -44 | -42 ^(c) | -47.1 | -33.4 |
| EVM | dB | -35 | -30 | N/A | <-36 ^(e) | -28 |

^a excluding the LO generation power consumption; ^b multi-tone signal;

^c 5 MHz BW at 12.5 MHz offset; ^d 7 dB backoff;

^e QPSK, 16QAM and 64QAM; ^f estimated from die photo;

^g WLAN 64QAM;

located 40 MHz away from f_{LO} , ACPR and C-IMD3/ $H_{3\text{BB}}$ of <-45 dBc are achieved. With all of the five CCs active (and maintaining a PAR of 11 dB), the ACPR drops to -41.8 dBc.

Fig. 20 shows the ACPR as a function of the average output power for a 20-MHz multi-tone signal with a 11-dB PAR (resembling LTE20) at 1.8 GHz. By digitally changing the CSs bias, the output power could be controlled within a 14-dB range with less than a 1 dB impact on the ACPR (black curve). In our implementation, only 4 bits were considered for the bias control. To further adjust the power, digital gain back-off was applied (black curve). It can be seen that the 3GPP ACPR (≤ -45 dBc for LTE-A BS TX) is satisfied for an average output power range of -26 to -4 dBm.

Table I summarizes the proposed DDRM performance and compares it to the prior art. This is the first reported DDRM that implements the LO HR and suppresses the SSRs for large bandwidths. The mixing-DAC in [15] has a considerably better linearity; however, it uses calibration and has significantly lower output power, larger area, and higher power consumption. Compared with [14], our DDRM achieves better linearity and a larger bandwidth over a broader frequency range at the cost of lower efficiency. The reported linearity of [42] is notably less with a comparable efficiency and an RF output power. The DDRM implementation of [20] features the highest output power and efficiency among others; however, compared with our DDRM, its achieved linearity is approximately 7 dB less despite using a 2-D look-up table DPD. Finally, compared with the state-of-the-art analog-intensive TX of [43] that is

targeted for commercial BSs, which can achieve -54 -dBc ACPR (at 2.6 GHz) for $3 \times$ LTE20 with 0-dBm output power and a total power consumption of 500 mW (excluding the DAC and the synthesizer), our solution only draws 130 mW (excluding LO generation) at 1.8 GHz with -48 -dBc ACPR (20-MHz CC and 11-dB PAR) and -4 -dBm output power. This indicates that digital RF modulators can potentially achieve adequate performance with equivalent or less power consumption.

VI. CONCLUSION

In this paper, a wideband, linear DDRM incorporating a novel I/Q -interleaving RF-DAC featuring HR operation in conjunction with an advanced SOH interpolation filter was proposed. The DDRM simultaneously enables sufficient suppression of SSRs and LO harmonics over a 0.9- to 3.1-GHz frequency range while consuming only 146 mW at 3 GHz. With $+9.2$ -dBm peak output power, 13% drain efficiency, and <-48 -dBc ACPR, the realized DDRM can act as an energy-efficient pre-driver for the next generation multi-band/multi-band BS PAs using CA.

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