Split-Array, C-2C Switched-Capacitor Power Amplifiers

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***Abstract*— This paper presents a 13-b C-2C split-array (SA) multiphase switched-capacitor power amplifier (SAMP-SCPA) implemented in 65-nm CMOS. The SAMP-SCPA was designed for 16-b resolution to offer extra states for linearization/calibration using digital pre-distortion (DPD). Resolution limits for SA SCPAs are presented. The SAMP-SCPA allows for the improvement of the SCPA resolution while minimizing the impact on the input power required driving it. A prototype SAMP-SCPA, occupying 0.85 mm × 2 mm, delivers a peak output power of 24 dBm with a peak system efficiency (SE) of 40% at 1.8 GHz. When amplifying a long-term evolution (LTE) signal, the average output power and SE are 18.8 dBm and 21.6%, respectively, with an adjacent channel leakage ration (ACLR) < −30 dBc and error vector magnitude (EVM) of 2.65% rms. The increased resolution allows output power to be traded off for improved linearity and a low power mode demonstrates an EVM as low as 1% rms.**

***Index Terms*— C-2C array, class-D power amplifier (PA), digital PA, multiphase switched-capacitor power amplifier (SCPA), radio frequency digital-to-analog converter (RF DAC).**

I. Introduction

THE pursuit of high data rates in wireless communications has led to the prevalence of non-constant envelops (non-CE) modulation with high peak-to-average power ratios (PAPR) [e.g., Wi-Fi and long-term evolution (LTE) for 3G]. Because efficiency is inversely proportional to output power, linear power amplifiers (PAs) are inefficient when outputting less than peak output power, as is the average for large PAPR signals. Switching PAs are more efficient when compared to linear counterparts; additionally, CMOS scaling focuses on optimization of transistors as low-loss and high-speed switches [1], rather than as linear transconductors [2]. However, due to their limited sensitivity to input signal amplitude, external linearization techniques are required.

Techniques such as envelope elimination and restoration (EER) [3], [4], digital polar [5]–[9], outphasing/LINC/Chireix [10]–[12], pulse-modulation [13], [14], and digital-Doherty [15], [16] have been proposed, but in each case they rely on polar components of the non-CE modulated signal. The polar components require high bandwidth amplitude and/or phase modulators that are difficult to build in CMOS. In addition, these circuits can require significant static power consumption and/or more chip area. Furthermore, the bandwidth expansion involved with polar conversion [17], [18] limits the capability to operate in closed loops and the systematic errors (e.g., group delay and finite bandwidth) dominate the overall non-linearity.

Conventional switched-capacitor PAs (SCPAs) operate as polar transmitters (TX), combining the functions of a digital-to-analog converter (DAC), baseband filtering, frequency upconversion, and amplification into a single block. They are versatile and can readily be tuned to different frequencies and power levels and scaled with process changes [9], [19]. They suffer from the drawbacks of all polar TXs, with the additional drawback of being quantized. Quantization noise from prior SCPAs dominated the out-of-band (OOB) noise, which is typically only filtered by a resonant matching network at the output.

In recent years, quadrature [20]–[22] and multiphase [23] digital PAs have been proposed. Quadrature- and multiphase-SCPAs (Q-SCPA and MP-SCPA, respectively) reduce the challenges associated with polar conversion and modulation [21], [23], while leveraging the other benefits of the SCPA. They do not suffer the same systematic non-linearities as polar TXs, but do suffer from reduction in output amplitude when compared to polar systems [24], [25]. The Q-SCPA is a special case of the MP-SCPA, where the number of phases M is equal to four. Q-SCPAs have a phase-dependent power drop caused by the 90° phase difference of the I and Q signals. Additional basis phases can be used to decrease the phase difference (e.g., increase constructive summation). Still, the critical challenge for prior SCPA designs is their output resolution limiting the OOB noise. The minimum available size of a capacitor in each CMOS process and the associated matching due to process, voltage, and temperature (PVT) variations determine the maximum resolution of prior SCPAs.

Split-array SCPAs (SA-SCPA) [26], [27] are introduced to overcome the challenges of simultaneously designing SCPAs with high resolution and high output power. SAs [Fig. 1(a)]

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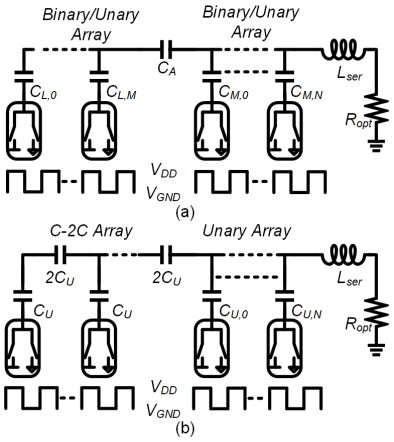


Fig. 1. SA SCPA schematics. (a) Traditional binary–unary SA. (b) C-2C/unary SA.

allow a capacitance array to be subdivided with the aid of an attenuation capacitor C_A to balance the charge between the arrays, regardless of the size of the arrays, or their associated capacitance [28]. This allows a reduction in area and allows for array capacitance to be scaled to usable values for high-resolution arrays. The LSB sub-array capacitance, in series with the capacitance from C_A presents the equivalent of a unit capacitance in the MSB sub-array. More than one split can be added to an array, but linearity is sensitive to matching and parasitic effects from C_A. C-2C arrays [20], [21] are widely used because of the low ratio of the maximum-to-minimum capacitance, which allows for the better capacitor matching [29], at the expense of sensitivity to parasitic effects [30], [31]. The size of the C-2C array increases linearly with the resolution, thus occupying less area then a binary-weighted array. The sizes of the capacitors are fixed and small, making the switches see approximately the same small capacitive load, thus easing the switch design as well as the layout, since the entire topology is composed of the replicas of a small C-2C block.

This paper presents a C-2C SA, multiphase SCPA [SAMP-SCPA, Fig. 1(b)] [22] that achieves high output power, efficiency, and linearity. This paper is organized as follows. In Section II, theoretical operation of SCPAs, including the MP-SCPA is discussed. Analysis for resolution limits in SCPAs is provided in Section III. In Section IV, implementation details are provided, followed by measurement results in Section V. Finally, conclusions are presented in Section VI.

II. Theory of Operation

A. Conventional SCPA

Taking advantage of low-loss, fast CMOS switches, area-efficient capacitors, and precisely controlled capacitance ratios, the SCPA is becoming commonly used for RF-mixed-signal circuit design [9], [19]. The SCPA is an arrayed class-D PA that controls the output voltage using a capacitive voltage divider at its output. The core of the SCPA is a logic-gated inverter driving one plate of a capacitor, whose opposite plate is common to an array of such circuits. The gating logic controls whether the capacitor is switched at the radio frequency (RF) carrier frequency, or held at a fixed-potential. The common top-plates are connected to an inductive impedance and load resistance, typically, via an impedance matching circuit. The matching circuit is tuned such that an equivalent resistor-inductor-capacitor (RLC) circuit is realized and tuned to select the RF carrier frequency, while rejecting harmonics of the switching waveform.

Several unit capacitors share a common plate, while the other plates are selectively driven by phased-modulated pulse-waves, switching between the supply voltage (V_{DD}) and ground (V_{GND}) or held at V_{GND}. By controlling the ratio of the total capacitance switched between V_{DD} and V_{GND}, arbitrary voltages can be generated at the output. If switching all N capacitors, peak voltage is generated, while switching only some of the capacitors reduces the output voltage proportional to the n total capacitors that are switched. The output voltage V_{out} is then given by the following:

$$V_{\mathrm{out}} = \frac{2}{\pi}\frac{n}{N}V_{\mathrm{DD}} \tag{1}$$

where $2/\pi$ is the Fourier coefficient for the fundamental frequency of the square switching wave. The output power is given by the square of the RMS value of the output voltage, divided by the load resistance it is driving, R_{opt}

$$P_{\mathrm{out}} = \frac{2}{\pi^2}\left(\frac{n}{N}\right)^2\frac{V_{\mathrm{DD}}^2}{R_{\mathrm{opt}}}. \tag{2}$$

An SCPA design begins by choosing R_{opt} to provide the desired output power.

The input power is due the power dissipated in charging the total input capacitance to its final voltage

$$P_{\mathrm{in}} = C_{\mathrm{in}}V_{\mathrm{DD}}^2 f_0 \tag{3}$$

where C_{in} is the input capacitance that varies with the selected input code n and f_0 is the operation frequency. C_{in} is given as

$$C_{\mathrm{in}} = \frac{n(N-n)}{N^2}\cdot C \tag{4}$$

where C is the total capacitance in the array. The efficiency of the SCPA is determined by the ratio of output power to total power

$$\eta_{\mathrm{SCPA,ideal}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}+P_{\mathrm{out}}} = \frac{4n^2}{4n^2+\frac{\pi n(N-n)}{Q_{\mathrm{NW}}}} \tag{5}$$

where Q_{NW} represents the loaded quality factor of the equivalent RLC network which is given by the following:

$$Q_{\mathrm{NW}} = \frac{X}{R_{\mathrm{opt}}} = \frac{1}{2\pi f_0 C_{\mathrm{tot}} R_{\mathrm{opt}}}. \tag{6}$$

where C_{tot} is the total capacitance in the array (i.e., the sum of all unit capacitances). In practice, the choice of Q_{NW} is dominated by the quality factors of integrated CMOS inductors. Typically, the qualify factor of on-chip inductors is <20. The efficiency for a two-element downward transforming impedance match, comprising an inductor and capacitor, can be given by [32]

$$\eta_{\mathrm{match}} = \frac{1-\frac{Q_{\mathrm{NW}}}{Q_{\mathrm{cap}}}}{1+\frac{Q_{\mathrm{NW}}}{Q_{\mathrm{ind}}}} \approx \frac{1}{1+\frac{Q_{\mathrm{NW}}}{Q_{\mathrm{ind}}}}. \tag{7}$$

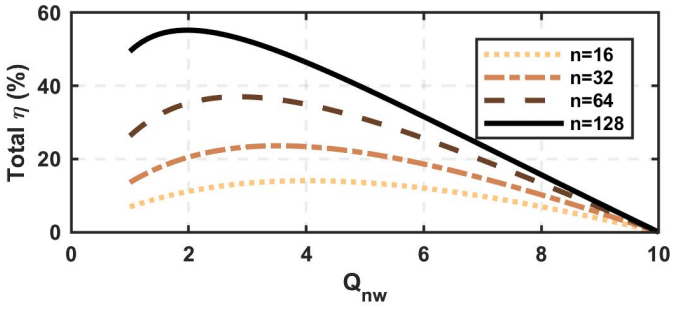


Fig. 2. SCPA total efficiency versus loaded network quality factor.

The total drain efficiency η_{tot} of the SCPA is the product of (4) and (6)

$$\eta_{\text{tot}} = \eta_{\text{SCPA,ideal}} \cdot \eta_{\text{match}}. \tag{8}$$

where η_{tot} is plotted versus Q_{NW} ($Q_{\text{ind}} = 15$) in Fig. 2, and shows a convex optimum. The optimum Q_{NW} is between 2–4 for typical inductor quality factors in integrated RF CMOS processes. It is noted that inductors with high Q_{ind} would allow a proportionally higher network quality factor to achieve optimal efficiency.

B. Operation of MP-SCPA

Unlike the original SCPA that used polar multiplication to achieve a linear output, the MP-SCPA utilizes vector summation, where the SCPA weights and sums a set of basis vectors using a capacitor array. Conceptually, in an MP-SCPA, the capacitor array is divided into sub-arrays that are clocked by different phases of an MP clock. The arrays are typically "shared" [20], [23]. A set of basis clock phases which span the unit circle are generated by an MP clock generator. The phases are typically uniformly spaced. Two of the phases clock the SCPA such that the capacitor array weights each basis vector. Charge re-distribution on the common plate of the capacitors allows the vector summation of the two weighted phases so that the output has the desired amplitude and phase corresponding to the input amplitude and phase modulation. Typically, adjacent phases are summed, but the MP-SCPA is not inherently limited to summing adjacent clock phases. It can also sum more than two phases. The only requirement is that the charge contribution of each phase should settle before another phase is input.

An example of a 16-phase MP-SCPA is shown in Fig. 3. An MP clock generator, which can be created with a phased-locked loop (PLL), delay-locked loop (DLL), polyphase filter, or a multistage ring-oscillator, is used to generate RF clock signals that are divided into 16 output phases (ϕ_1 to ϕ_{16}). From the 16 phases, the two adjacent output phases (e.g., ϕ_1 and ϕ_{16}) that are closest to the desired PM phase are routed to an MP logic decoder. The logic decoder decides whether an individual capacitor in the array is switched on ϕ_1, or ϕ_{16}, or held at ground. In this way, the basis phases are weighted and summed.

The number of basis phases can be different than 16, and does not have to be symmetric. If fewer phases are used,

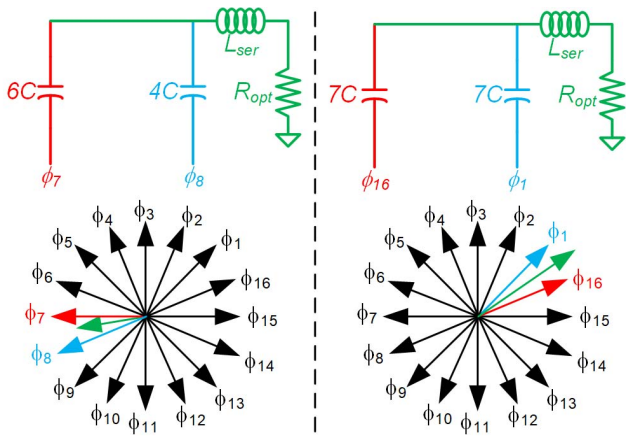


Fig. 3. Examples operation of an MP-SCPA with 16-phases SCPA.

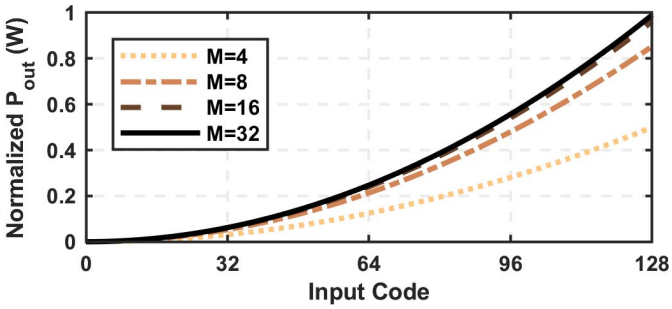


Fig. 4. Normalized P_{out} versus code for different numbers of phases, M.

the maximum output power is reduced, while if more phases are used, more complex digital signal processing and faster charge settling requirements are required. The normalized output power of an MP-SCPA as a function of the number of cells switched on phase 1, n_1, phase 2, n_2, the total number of cells N and the number of phases M is provided in the following equation [23]:

$$\|P_{\text{out}}\| = \left(\frac{n_1^2 + n_2^2 + 2n_1 n_2 cos\,(2\pi/M)}{4N^2}\right). \tag{9}$$

Fig. 4 shows $\|P_{\text{out}}\|$ versus the number of switching capacitors (7-bit array) and the number of phase vectors, M. It is observed that there is a significant increase in output power when increasing the number of phases from $M = 4$ to $M = 8$ and again from $M = 8$ to $M = 16$, but not a significant jump when increasing M beyond 16. Another factor in choosing M is that the charge should settle on each capacitor that is switched on phase m before the beginning of phase $m+1$; with an increase in M, less time is available for settling between edges. Hence, interaction between the phases would cause non-linearity. For further detail on the MP-SCPA, the reader is referred to [23].

C. Operation of SA-SCPA

An SA allows for a capacitor array (Fig. 1) to be divided into two, or more, sub-arrays with larger unit capacitors, mitigating the challenge of designing small MiM capacitors or using lossier, more parasitic laden vertical natural capacitors.

In the SA, an attenuation capacitor C_A is placed in series between the LSB and MSB sub-arrays to allow for charge re-distribution. The capacitor sizes on the LSB and MSB sub-arrays are given as follows:

$$C_{B0,\mathrm{LSB}} = C_{\mathrm{tot}}/2^L \tag{10}$$

$$C_{\mathrm{BL,LSB}} = C_{B0,\mathrm{LSB}}2^L \tag{11}$$

$$C_{B0,\mathrm{MSB}} = C_{\mathrm{tot}}/2^{M+\log 2^{N+1}} \tag{12}$$

$$C_{\mathrm{BM,MSB}} = C_{B0,\mathrm{MSB}}2^M \tag{13}$$

and

$$C_{U,\mathrm{MSB}} = C_{B0,\mathrm{MSB}} \tag{14}$$

where C_{tot} is the desired total size of capacitor array, L is the total number of binary-weighted cells in the LSB sub-array, M is the total number of binary weighted cells in the MSB sub-array, and N is the total number unary-weighted cells in the MSB sub-array. The attenuation capacitance is expressed as follows:

$$C_A = \frac{\sum C_{\mathrm{LSB}}}{\sum C_{\mathrm{MSB}}} C_{U,\mathrm{MSB}}. \tag{15}$$

The capacitance seen from the input is given by (3). The maximum power occurs for $n = N/2$, corresponding to a half input code. Hence, the maximum input power based on (2) is found as

$$P_{\mathrm{IN}} = \frac{1}{4} C_{\mathrm{tot}} V_{\mathrm{DD}}^2 f_0. \tag{16}$$

The minimum capacitor must be larger than the minimum geometry possible in each technology. Minimum sized capacitors offer poor matching; hence, using small capacitors reduces the SCPA linearity. In addition, if binary-weighted capacitors are used, the ratio of capacitance in the design grows geometrically, also reducing the matching accuracy

$$C_{\mathrm{ratio}} = 2^M. \tag{17}$$

The resolution of the array is limited by the minimum capacitance available in the process for a given output power and network quality factor. Using an SA allows larger capacitors to be used for LSBs and hence enables increasing the resolution of the SCPA, while being able to control C_{ratio}. This comes at the expense of slightly larger input power needed to switch larger capacitors in the LSB sub-array(s). For best linearity and efficiency, an optimal design would minimize the product of the capacitance ratio and the input power. Hence, a figure of merit (FoM) is defined as follows [33]:

$$\mathrm{FOM} = \max(P_{\mathrm{in}}) C_{\mathrm{ratio}}. \tag{18}$$

The position of C_A can be located at any bit position between the LSB and the MSB, impacting the size of both arrays, which impacts both input power consumption and linearity. For all possible LSB sub-array and MSB sub-array combinations in Fig. 1, the FoM versus the position of the attenuation capacitance C_A for a total capacitor array resolution of 16 bits is shown in Fig. 5. The sub-arrays can be either binary weighted, unary weighted, or C-2C. It is noticed that due to higher FoM and worse performance compared with other configurations, the unary LSB, binary MSB configuration is neglected. Only the switching losses and conduction losses of the output state are considered when calculating input power; all other kinds of power consumption would scale similarly for all of the varying designs. Owing to the same total capacitance and capacitance ratio for both binary LSB, binary MSB and binary LSB, unary MSB configurations, the binary–unary design is not pictured, though it is noted that the FoM of both are identical. In this case a binary–binary array will always be preferable to a binary–unary array due to its reduced size and no need for a decoder.

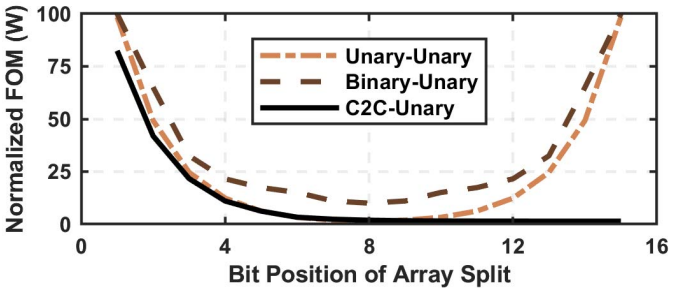


Fig. 5. FoM versus bit positon of the array split for different SA-SCPA configurations.

An even split between the LSB and MSB sub-arrays (e.g., position of the attenuation capacitor is equal to half of the total number of bits) yields the best FoM for any array combinations except for C-2C-unary array. This is because the ratio of the maximum-to-minimum capacitance is only two, which reduces the effect of mismatch and total capacitance decreases when increasing the number of bits in the C-2C array. The total equivalent capacitance for a C-2C array increase linearly as the number of C-2C bits is increased. The unit capacitor in the C-2C segment should be equal to $1.5\times$ the unit capacitor in the unary array to achieve better resolution.

C-2C segmented arrays uses the same number of unit cells as binary segmented arrays; hence, they preserve the area efficiency benefits. Moreover, they use the same unit cells throughout the C-2C array; hence, they provide better matching in the layout. However, nodal parasitics degrade their linearity. As seen from Fig. 5, for C-2C arrays the FoM is better when increasing the number of C-2C bits. However, the resolution of C-2C arrays cannot be made arbitrarily high due to the nodal parasitics that will be discussed in Section III. Due to the trade-offs made to minimize the layout area, maximize the efficiency and achieve good linearity simultaneously, a C-2C LSB, unary MSB configuration is chosen.

Because the total capacitance seen by the switches of both C-2C and unary-weighted arrays are different, the size of the switches should be optimized in both sub-arrays to maximize the switching efficiency and minimize delay differences. The switches are sized using logical effort calculations to optimize the delay versus power consumption tradeoff. Though the size of the unary-weighted unit capacitor is designed to be the same as that in the C-2C array to reduce the effect of mismatches in the capacitors, the resolution limit of C-2C arrays is still determined based on the mismatch due to PVT variations of the capacitors in the array [31], parasitics between internal

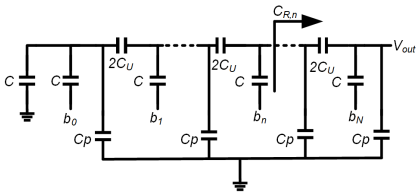


Fig. 6. C-2C DAC with nodal parasitic.

nodes and the substrate [29], [30], [34] and the jitter limitation of the clock, which will be discussed in Section III.

III. Resolution Limit of C-2C Array

In C-2C arrays the significant parameters affecting linearity are the capacitor matching and the intra-nodal parasitics, as well as the jitter. Jitter will not be examined here since the limit is well known and no different for any SC-DAC. Nodal parasitics, mismatch and their effects on integrated and differential non-linearity (INL and DNL, respectively) will be examined in Sections III-A and III-B.

A. Nodal Parasitic

Unlike traditional unary or binary array capacitor arrays, the C-2C array has a major disadvantage due to the parasitic capacitances located at intermediate nodes inside the DAC which are dependent on each bit rather than the segmentation number of the DAC. This is because some of the charge from the switching capacitors is distributed to the nodal parasitic capacitors during the conversion process which effectively serves to change the voltage contribution from each capacitor in the array. These nodal parasitic effects of C-2C arrays results in poor linearity at higher output resolutions; hence, they significantly limit the resolution of such arrays.

The nodal parasitic capacitance associated with C-2C array is shown in Fig. 6, where C_P is the sum of bottom-plate and top-plate parasitic capacitances of the interconnecting capacitors (2C) and the top-plate parasitic capacitance of the branch capacitor (C). The output voltage of a parasitic laden C-2C array, for any codeword n can be expressed as follows:

$$V_{\text{out}} = \sum_{n=0}^{N} \frac{b_n(N-n)}{\frac{3C+C_{R,n+1}+C_P}{C+C_{R,n+1}+C_P} \cdot \frac{3C+C_{R,n+2}+C_P}{C+C_{R,n+2}+C_P} \cdots \frac{3C+C_{R,N}+C_P}{C+C_{R,N}+C_P}}. \tag{19}$$

where $C_{R,n+1}$ is the equivalent capacitance looking toward the output from any bit position, and b_n is the value of the codeword at bit position n. The equivalent capacitance is found as follows:

$$C_{R,N} = C \tag{20}$$

$$C_{R,N-1} = [C_{R,N} + (C + C_P)] \| 2C \tag{21}$$

$$\vdots$$

$$C_{R,n+1} = [C_{R,n+2} + (C + C_P)] \| 2C \tag{22}$$

$$C_{R,n} = [C_{R,n+1} + (C + C_P)] \| 2C. \tag{23}$$

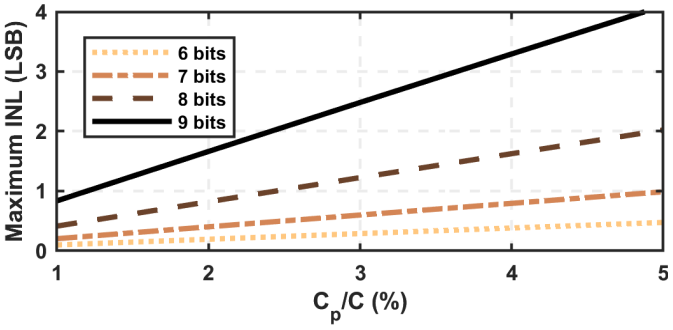


Fig. 7. Maximum INL versus C_p of a C-2C array for different resolutions.

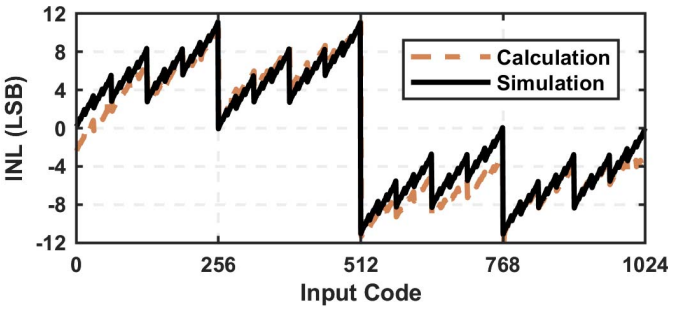


Fig. 8. Calculated versus simulated INL for 10-bit C-2C array with 5% C_p.

Nodal parasitics primarily affect the INL of the design, as they are assumed to be uniformly distributed. The maximum INL can be found by integrating the difference of V_{out} to an ideal ramp over all input codes. Maximum INL for a C-2C array is plotted as a function of the size of C_p, relative to C, in Fig. 7. For a typical value of parasitic (e.g., 3%–5% of C), the INL is only less than 1 LSB for array resolutions of ~7 b. The calculated INL for a 10-b array is plotted as a function of the input code and compared to an ideal simulation in Fig. 8. C_p is set at 5% of the branch capacitance and the simulation shows an INL of ~11 LSB (e.g., loss of 3–4 b). Simulation and theoretical calculations match well.

B. Mismatch

An additional limitation on the accuracy of the SA, C-2C SCPA is related to the matching between the capacitors, which sets another limit on the INL and DNL that are achievable. INL and DNL depend on both the final DAC resolution, B, and element matching, σ_E, which can be expressed as follows:

$$\sigma_E \approx \frac{K}{\sqrt{\text{Area}}} \tag{24}$$

where K is a process parameter (e.g., 0.86 for the 65-nm CMOS process used in this paper). The INL/DNL can be calculated for the C-2C array and unary array separately to determine the matching accuracy required in the capacitors to achieve the designed resolution. The maximum allowed capacitor mismatch for the unary capacitors can be calculated

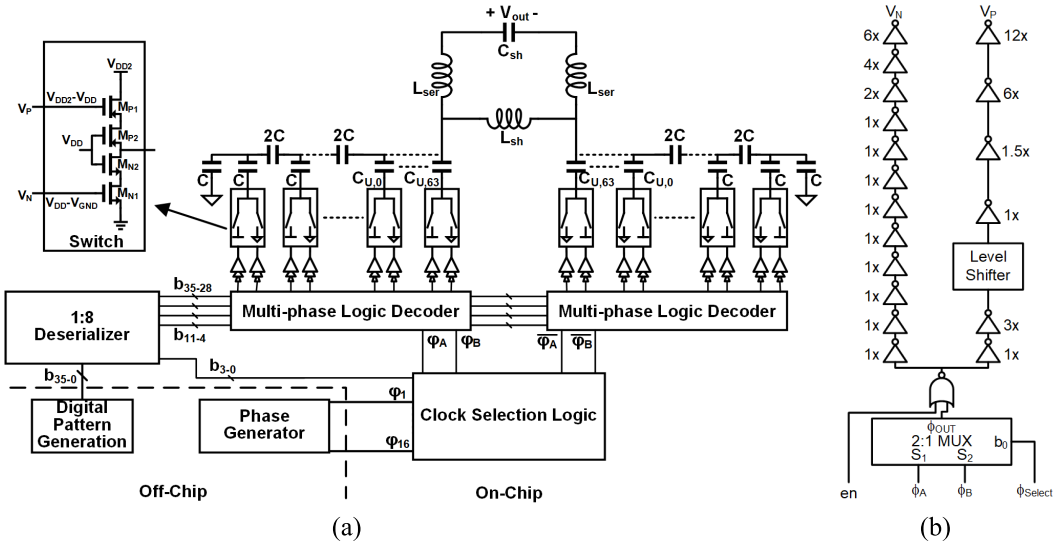


Fig. 9. (a) Block diagram schematic of the prototype 13-b, 16-phase C-2C SAMP-SCPA. (b) Block diagram of the slice enable and phase selection logic.

using the following expressions [31]:

$$\sigma_{\mathrm{INL}} = \frac{\mathrm{INL}}{\sqrt{2}\,(erfinv\,(Y))} \tag{25}$$

$$\sigma_{\mathrm{DNL}} = \frac{\mathrm{DNL}}{\sqrt{2}\,(erfinv\,(Y))} \tag{26}$$

$$\sigma_{u_I NL} = \frac{2\sigma_{\mathrm{INL}}}{\sqrt{2}^B} \tag{27}$$

$$\sigma_{u_D NL} = \frac{\sigma_{\mathrm{DNL}}}{\sqrt{2^B - 1}} \tag{28}$$

where B is the number of bits, Y is the confidence interval (e.g., 95%), *erfinv* is the inverse error function, and $\sigma_{u_I NL}$ and $\sigma_{u_D NL}$ are the standard deviations of the capacitance mismatches. INL and DNL typically are desired to be less than one LSB at the designed resolution. The array is segmented with a 6-b unary array; hence, $\sigma_{u\_DNL} < 6.4\%$ and $\sigma_{u\_INL} < 12.6\%$. Even minimum area MiM capacitors in the process can easily meet these matching limits.

For the C-2C array, the nodal parasitic dominates the INL. However, mismatch does have a significant impact on the DNL, which can be calculated as follows:

$$\sigma_{\mathrm{DNL}} = \frac{\mathrm{DNL}}{\sqrt{2}\,(\mathrm{erfinv}\,(Y))} \tag{29}$$

$$\sigma_{u\_\mathrm{DNL}} = \frac{2\sigma_{\mathrm{DNL}}}{2^B}. \tag{30}$$

The calculated acceptable standard deviation for the unit capacitance is <1.5%, which requires a capacitor of only 3 $\mu\mathrm{m}^2$. It is noted that at the designed resolution for the unary array and the C-2C arrays, nodal parasitics limit the response more than mismatch.

It is also noted that the total capacitance in the SCPA array is chosen to satisfy the desired network quality factor from (8), based on the desired output power from (2). For the designed PA, the unit capacitance is ~40 $\mu\mathrm{m}^2$, resulting in a mismatch of 0.14%, which is a significantly smaller mismatch than is required meeting the INL and DNL limits as calculated above.

IV. Circuit Design Details

A 16-b, 16-phase SAMP-SCPA (Fig. 9) was chosen for implementation, where the array was segmented into a 10-b C-2C LSB sub-array and a 6-b unary MSB sub-array. Though the C-2C is only accurate to ~7 b, extra states in the C-2C array allow for digital calibration or DPD. Given area, the unary array could be scaled to increase the total resolution up to the presented limits. Details of the design follow.

A. Top Level of the 13-b SAMP-SCPA

A block diagram of the proposed differential 16-b, 16-phase SAMP-SCPA is shown in Fig. 9. The capacitor arrays are designed using MiM capacitors with layout techniques similar to those found in [30], as shown in Fig. 10. This layout provides balanced parasitics at every node to minimize differential non-linearities associated at every bit position in the C-2C arrays. It is also noted that an m-bit C-2C array scales linearly in area for each added bit, whereas an n-bit unary array scales exponentially in area with each added bit of resolution. Hence, the C-2C SA allows for an overall smaller design than a fully unary array would at the same output resolution. The array is designed to offer extra states that can be used for linearization, enabling the array to meet signal fidelity requirements for signals with large PAPR [e.g., error vector magnitude (EVM) and adjacent channel leakage ration (ACLR)]. Amplitude and phase control bits are generated by a high-speed digital I/O with a clock rate of 100 MHz. To minimize the number of digital I/O pads on the chip, the 36 control bits are serialized at a rate of 8:1. The digital pattern is input to a 1:8 deserializer. The four LSB bits are used to control the clock selection MUX, while the 32 MSBs control the multiphase logic decoder. In the proposed design, 16 evenly distributed phase vectors ($\varphi_1 - \varphi_{16}$) are created by an off-chip phase generator. The details of individual blocks will be discussed as following.

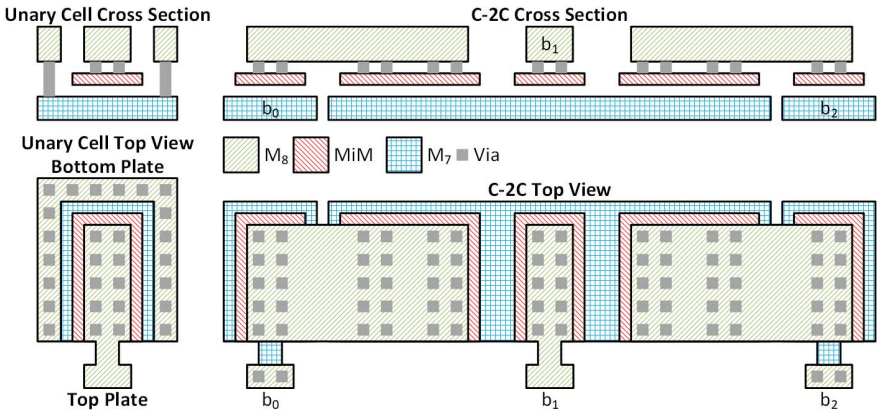


Fig. 10. Capacitor layout and cross section for the unit unary cell and the C-2C array.

B. Unit Cell

1) Switch and Logic Design: A cascode CMOS inverter serves as the output switch for the capacitor array [Fig. 9(a), upper left]. This permits the switch output voltage to be as high as $2\times V_{\mathrm{DD}}$ without exceeding the breakdown voltage rating of the transistors. This choice allows an increase in the output power that helps to reduce losses due to impedance transformation in the matching network [9]. The cascode inverter (Fig. 9) is designed such that the gates of the inner transistors of the inverter are tied to V_{DD}, while the outer transistors in the cascode are switched by time aligned non-overlapping clock signals with different logic levels. Non-overlapping signals allow crowbar current from V_{DD} to V_{GND} to be minimized, realizing a tri-state circuit. The NMOS transistors are switched by logic levels from V_{GND} to V_{DD}, while a level shifter is used to change the logic levels for the PMOS transistors to switch between V_{DD} and $2V_{\mathrm{DD}}$. The switch design is optimized to drive the input capacitance using sizing for logical effort to drive the desired capacitance.

2) Capacitor Design: The capacitors are designed on the MiM layer and are sized based upon the chosen network quality factor (e.g., $Q_{NW} = 3$) and the output power requirements, as dictated in (2) and (6). Equation (6) gives the total array capacitance, and then a unit cell is designed such that the unit cell capacitance is equal to the total capacitance divided by the number of unary bits. A layout of both the unary capacitor cell and C-2C capacitors is shown in Fig. 10. The layout shows both the top view and the cross section to detail the parasitic reduction efforts at the cell layout level. The capacitors are laid out between layers M7 and M8 using a mezzanine MiM layer.

All unary capacitors share a common bottom plate that forms a ring around the top plate to minimize fringing capacitance between adjacent bits. The C-2C array is designed such that alternating inputs to the array are on either metal 7 or metal 8, to balance the parasitic between inputs.

C. Switch Driver Slice Design

The driver slice for each capacitor cell is shown in Fig. 9. Each slice consists of a phase selection 2:1 MUX that selects the phase of the clock to switch from and is followed by an OR gate that controls whether the slice is enabled (e.g., switches at the clock rate) or is held at ground. Because the two phases that are routed to each cell propagate at the same frequency, clock routing can be matched using a standard H-tree distribution to each cell. No additional calibration is necessary, as each cell is designed to present the same load to the clock tree.

A chain of inverters is sized using to provide delay matched switching signals to drive the cascoded output switch that is connected to a capacitor in the array. The slice is designed to be pitch matched to the capacitor it is driving in the array for maximal layout compactness. The PMOS and NMOS switches in the output stage switch are driven from separate supply ranges to protect the devices from the $2V_{\mathrm{DD}}$ supply swing. A level shifter [35] is used to change the supply domain for the PMOS switches to operate between V_{DD} and $2V_{\mathrm{DD}}$, while the NMOS switches operate between V_{GND} and V_{DD}. Simulations are run to ensure that the timing in the separate PMOS and NMOS paths match well.

It is noted that all capacitors in the unary array are identical; hence, all devices in the unary slices are sized equally. The input capacitance in the C-2C slices varies by bit position; hence, each element in the C-2C array is optimized to match the delay in the unary array paths.

Note that the logic that enables and disables each slice is changing at the modulation rate, which is significantly slower than the clock rate and hence jitter limitations are not considered in this design.

D. Phase Selector and Amplitude Decoder Logic

The deserializer, phase selection logic and MP decoder logic are designed in Verilog and synthesized using a standard cell library. The decoders control a total of 68 billion output states.

The deserializer is designed as a set of parallel 8-b shift registers and the outputs are segmented on chip before being input to the clock selection logic or multiphase decoder logic.

The 16 evenly distributed phases are input to the clock selection logic, which is comprised of logic selection bits controlling MUX tree decoder. The two adjacent phases to the desired output phase (e.g., φ_A, φ_B and $\bar{\varphi}_A$, $\bar{\varphi}_B$) are chosen by the MUX and passed to the multiphase logic decoder.

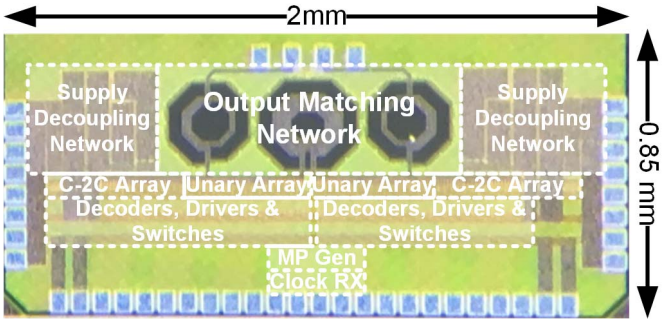


Fig. 11. 65-nm experimental prototype SAMP-SCPA chip microphotograph.

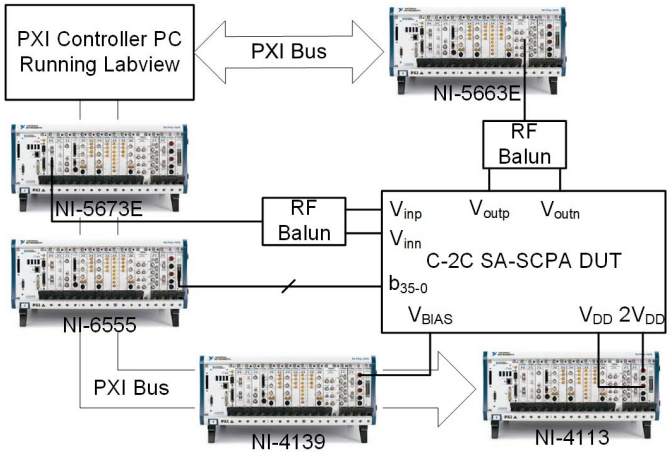


Fig. 12. Measurement setup for static and dynamic measurements. Note that all instruments reside in a single NI-PXI chassis.

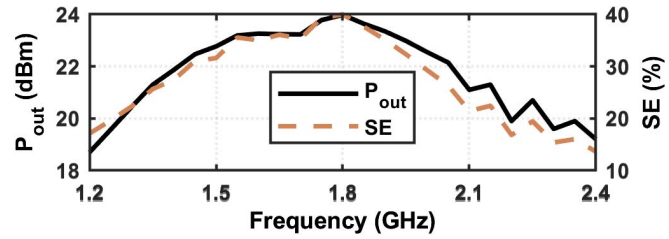
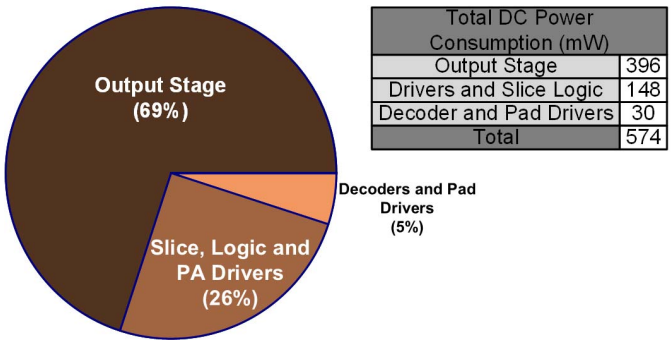


Fig. 13. Measured output power and SE versus frequency.



Total DC Power Consumption (mW)	
Output Stage	396
Drivers and Slice Logic	148
Decoder and Pad Drivers	30
Total	574

Fig. 14. Simulated output power breakdown of the output stage, slice logic and PA drivers and Input Decoders and Pad Drivers.

The multiphase logic decoder comprises a cascade of two binary-to-thermometer (B-T) decoders. The first 16-b (B-T) decoder controls how many cells are switched by

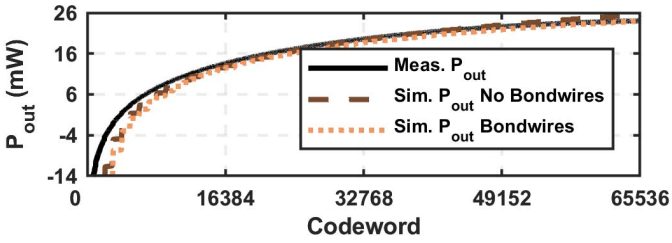


Fig. 15. Measured and simulated output power versus Code at 1.8 GHz.

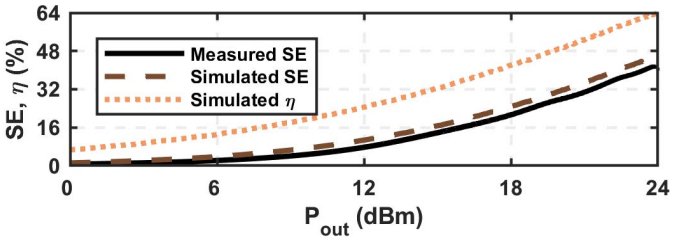


Fig. 16. Measured and simulated SE and drain efficiency versus output power.

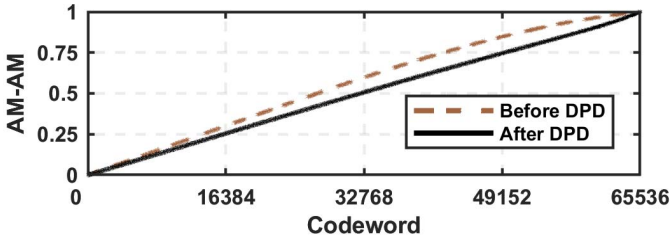


Fig. 17. AM–AM distortion versus codeword before and after DPD.

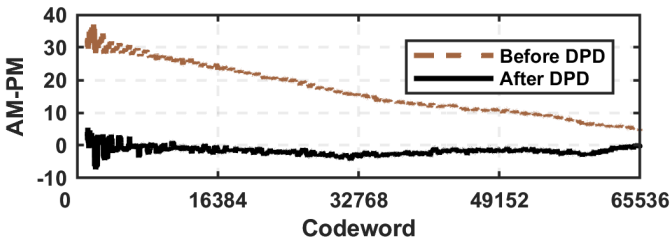


Fig. 18. AM–PM distortion versus codeword before and after DPD.

phase $\varphi_A(\bar{\varphi}_A)$. The second 16 b (B-T) decoder controls whether the balance of cells are switched by φ_B $(\bar{\varphi}_B)$ or held at ground.

The synthesized decoders are designed to match the timing in each bit path to minimize mismatch in the enable/disable delays and phase selection for each cell.

E. Matching Network

The matching network that transforms the antenna impedance of 50 Ω to the optimum termination impedance consists of a shunt symmetric inductor, L_{sh}, a series inductor, L_{ser}, and a shunt capacitor, C_{sh}, forming a bandpass resonant circuit at the design frequency. This network is chosen to provide a high impedance path toward the output to minimize the output contribution from high-frequency harmonics.

Fig. 19. Measured ACLR for a 1.4-MHz, 64-QAM LTE signal at (a) optimized for maximum output power and (b) optimized for best EVM.

Because the total capacitance seen by the matching network remains constant, regardless of the number of capacitors being switched, it can be sized to be resonant with the total array capacitance and remains unchanged for any choice of input code. The value of the loaded quality factor is chosen to be $\sim$3, leading to a circuit with $>$600 MHz $-$3 dB bandwidth centered at around 1.8 GHz. If off-chip impedance transformations are used, higher quality factors can be chosen. The experimental results of the prototype SAMP-SCPA are now discussed.

V. Experimental Results

The prototype MPSA-SCPA is fabricated in a 65-nm RF CMOS process with ultra-thick top metal for high-quality passive components. The chip microphotograph is shown in Fig. 11. It occupies a total area of 0.85 mm $\times$ 2 mm, including the matching network, output stage, logic decoders, and all of the I/O pads for supply and data. The C-2C SA-SCPA is implemented as an MP-SCPA, as shown in Fig. 9. The core logic for this process runs at 1.2 V, allowing the cascoded output stage to operate at 2.4 V. The measurement setup can be seen from Fig. 12. 16-phase vectors generated by an off-chip phase generator and received on-chip using low-voltage differential signaling (LVDS) amplifier are input to the clock selection logic. Due to the large numbers of digital I/O on this chip, the control bits are serialized to minimize the required pads. In system-on-chip (SoC) operation serialization is not necessary, but can be used to reduce wiring busses.

A. Static Measurements

Shown in Fig. 13 is the measured static output power P_{out} and system efficiency (SE) versus frequency. It is noted that the SE is the ratio of P_{out} to all input (dc and RF) power to the chip, including pad drivers. Operating at a center frequency of 1.8 GHz, the SAMP-SCPA outputs a peak power of 24 dBm with a peak SE of 40%. The measured $-$3 dB output power bandwidth of the PA is $\approx$700 MHz, which is determined by the loaded quality factor of the bandpass matching network. The power consumed in each major block is broken down in Fig. 14. The measured and simulated P_{out} with and without bond wires is plotted as a function of the digital input code at 1.8 GHz in Fig. 15. The simulation with estimated bond wire inductance matches well with the measurement. The simulated drain efficiency and measured and simulated SE (w/bond wire effects) is plotted versus output power in Fig. 16, showing a good agreement between simulation and measurement. The output power displays a weak non-linearity due primarily to supply inductance, with some INL contribution from parasitic capacitance in the C-2C array. This can be mitigated with low-inductance packaging (e.g., flip-chip or wafer level chip scale packaging). The AM–AM and AM–PM before and after DPD are shown in Figs. 17 and 18, respectively.

B. Dynamic Measurements

To verify the SAMP-SCPAs performance with signals with large PAPR, it is tested with a 1.4-MHz, 64-QAM LTE signal. The non-linearity from supply and ground bondwire inductance and any mismatch/parasitic effects are corrected with a polar digital pre-distortion (DPD) [36]. The ACLR performance at maximum output power is shown in Fig. 19(a). The DPD is optimized to meet the E-UTRA ACLR specification for an uplink signal of $<$ $-$30 dBc. The signal is de-troughed to reduce the PAPR down to the ACLR limit. De-troughing can be traded off for better ACLR at the expense of reduced efficiency. The transmitted power at this ACLR is 18.8 dBm with an average SE of 21.6%. The measured EVM at this output power is less than 2.65% rms.

Due to the versatility of the SAMP-SCPA, output power can be traded off for improved linearity. When adjusting

TABLE I
COMPARISON TO PRIOR ART

	This Work	[21]	[20]	[23]	[8]	[38]	[39]	[40]
CMOS Process (nm)	65	65	65	130	65	40	45-SOI	28
Supply (V)	2.4	1.2/2.4	1.3	3	1.2	0.5	1.2/2.4	1.2
Resolution (bits)	13-MP	9-IQ	13-IQ	7-MP	9-Polar	9-Polar	10-Polar	8-Polar
Center Frequency (GHz)	1.8	2.0	2.4	1.8	2.2	2.2	3.5	3.2
Peak P_{out} (dBm)	24	20.5	22.8	26	23.3	14.6	25.3	24.9
Peak SE (%)	40	20.0	34*	24.9	38	26	30.4	42.7#
Modulation	LTE 1.4 MHz 64-QAM	LTE 10 MHz 64-QAM	SC 22MHz, 64 QAM	LTE 10 MHz 64-QAM	802.11g 20 MHz 64-QAM	20 MHZ, OFDM 64-QAM	10 MHz, 32 Carrier 256-QAM	20MS/s 256-QAM
Average P_{out} (dBm)	18.9	14.5	15	20.9	16.8	6.2	17.1	17.5
Average SE (%)	21.2	12.2	NA	15.2	21.8	10.7	21.4	21.3#
EVM (%-rms)	2.65	3.6	3.98	3.5	3.98	1.6	1.0	2.39
ACLR (dBc)	-30.5/-30.9	-30.7/-31.0	<-43	-30.3/-31.7	NA	-46/-46	-45	-31.3
Matching Network	On-Chip LC	On-Chip LC	XFMR	On-Chip LC	XFMR	On-Chip LC	On-Chip LC	XFMR
DPD	Yes	Yes	Yes	Yes	No	Yes	Yes	No

*Includes Frequency Generation #Drain Efficiency

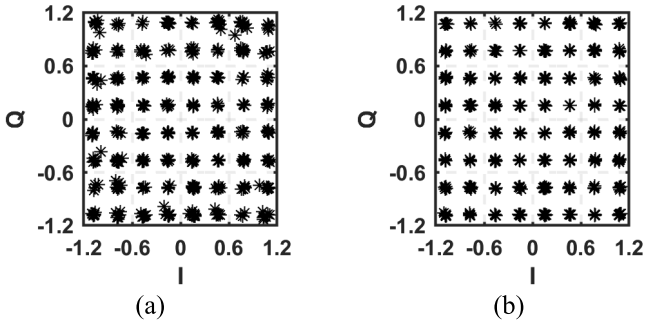


Fig. 20. Constellation for 1.4-MHz, 64-QAM LTE, (a) at max P_{out} (2.65% rms) and (b) at 4.3-dB backoff (1.03% rms), optimized for lowest EVM.

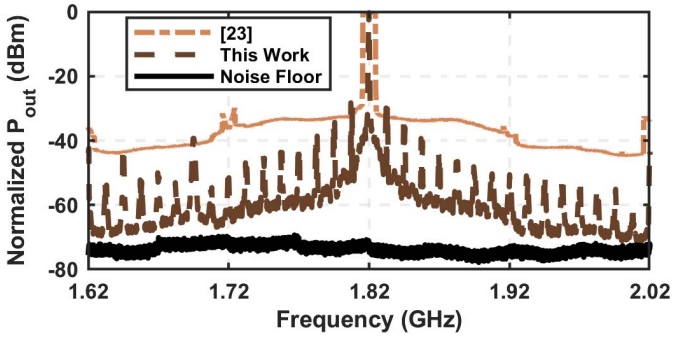


Fig. 21. Measured PSD of the 13-b SAMP-SCPA and [13].

the input code to slightly less than half power and using polar DPD, the ACLR is < -37 dBc [Fig. 19(b)] when outputting 14.6 dBm.

The LTE constellation is shown in Fig. 20(a) for maximum output power and Fig. 20(b) at reduced output power when optimized for the lowest EVM. The constellation shows improved EVM as power is traded off for linearity.

The SAMP-SCPA is a quantized system; therefore, the OOB noise is dominated by signal quantization. The OOB noise for the 16-bit C-2C SAMP-SCPA when transmitting a 1.4-MHz, 64-QAM LTE signal compared with the previous work at lower resolution is shown in Fig. 21. The power spectral density (PSD) demonstrates an OOB noise for a DAC with an effective number of bits (ENOB) of ∼13 b [37]. To minimize the space required for digital I/O pads, the input bits are serialized at 8:1; the HSDIO utilized offers a maximum clock rate of 100 MHz, resulting in a bit rate of 12.5-MHz input to the chip. This limits the maximum signal bandwidth; it is expected that without this limitation the bandwidth performance would be similar to other implementations of the SCPA [9], [21], [23]. Due to the I/O and instrument limitation, the switching spurs are closer in; however, the overall noise floor of the SAMP-SCPA achieves an signal to noise ratio expected for an ENOB of ∼13 b.

VI. CONCLUSION

SA SCPA techniques are introduced and implemented in a prototype SAMP-SCPA in 65-nm CMOS. The concept of multiphase signaling is used to leverage the advantages of DPAs while not requiring the wideband phase modulator of polar DPAs, or having the high combining loss of quadrature DPAs. When operating at 1.8 GHz, this PA delivers a peak P_{out} of 24 dBm with 40% SE. The performance is validated from static and modulation measurements using a 1.4-MHz, 64-QAM LTE signal. With polar DPD, the ACLR is below the required -30 dBc LTE standard and the measured EVM is 2.65% rms. A comparison to prior art is provided in Table I. The SAMP-SCPA is compared to prior MP DPAs [23], quadrature DPAs [20], [21], as well as polar DPAs [8], [38]–[40], SAMP-SCPA achieves similar output power and SE to prior art in digital PAs, while offering reduced OOB noise. The SAMP-SCPA is not just a PA, but a versatile digital TX front end.

REFERENCES

[1] R. B. Staszewski *et al.*, "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2278–2291, Dec. 2004.

[2] G. E. Moore, "Cramming more components onto integrated circuits," *Proc. IEEE*, vol. 86, no. 1, pp. 82–85, Jan. 1998.
[3] L. R. Kahn, "Single-sideband transmission by envelope elimination and restoration," *Proc. IRE*, vol. 40, no. 7, pp. 803–806, Jul. 1952.
[4] D. K. Su and W. J. McFarland, "An IC for linearizing RF power amplifiers using envelope elimination and restoration," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2252–2258, Dec. 1998.
[5] A. Kavousian, D. K. Su, M. Hekmat, A. Shirvani, and B. A. Wooley, "A digitally modulated polar CMOS power amplifier with a 20-MHz channel Bandwidth," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2251–2258, Oct. 2008.
[6] C. Presti, F. Carrara, A. Scuderi, P. Asbeck, and G. Palmisano, "A 25 dBm digitally modulated CMOS power amplifier for WCDMA/EDGE/OFDM with adaptive digital predistortion and efficient power control," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 1883–1896, Jul. 2009.
[7] D. Chowdhury, S. V. Thyagarajan, L. Ye, E. Alon, and A. M. Niknejad, "A fully-integrated efficient CMOS inverse class-D power amplifier for digital polar transmitters," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. 1113–1122, May 2012.
[8] L. Ye, J. Chen, L. Kong, E. Alon, and A. M. Niknejad, "Design considerations for a direct digitally modulated WLAN transmitter with integrated phase path and dynamic impedance modulation," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3160–3177, Dec. 2013.
[9] S.-M. Yoo, J. S. Walling, E. C. Woo, B. Jann, and D. J. Allstot, "A switched-capacitor RF power amplifier," *IEEE J. Solid State Circuits*, vol. 46, no. 12, pp. 2977–2987, Dec. 2011.
[10] H. Chireix, "High power outphasing modulation," *Proc. Inst. Radio Eng.*, vol. 23, no. 11, pp. 1370–1392, Nov. 1935.
[11] H. Xu, Y. Palaskas, A. Ravi, M. Sajadieh, M. A. El-Tanani, and K. Soumyanath, "A flip-chip-packaged 25.3 dBm class-D outphasing power amplifier in 32 nm CMOS for WLAN application," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1596–1605, Jul. 2011.
[12] T. W. Barton and D. J. Perreault, "Four-way microstrip-based power combining for microwave outphasing power amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 10, pp. 2987–2998, Oct. 2014.
[13] J. S. Walling *et al.*, "A class-E PA with pulse-width and pulse-position modulation in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 6, pp. 1668–1678, Jun. 2009.
[14] K. Cho and R. Gharpurey, "A digitally intensive transmitter/PA using RF-PWM with carrier switching in 130 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1188–1199, May 2016.
[15] W. H. Doherty, "A new high efficiency power amplifier for modulated waves," *Proc. Inst. Radio Eng.*, vol. 22, no. 9, pp. 1163–1182, Sep. 1936.
[16] S. Hu, S. Kousai, J. S. Park, O. L. Chlieh, and H. Wang, "Design of a transformer-based reconfigurable digital polar Doherty power amplifier fully integrated in bulk CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1094–1106, May 2015.
[17] J. S. Walling and D. J. Allstot, "Linearizing CMOS switching power amplifiers using supply regulators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 9. pp. 497–501, Jul. 2010.
[18] J. S. Walling and D. J. Allstot, "Design considerations for supply modulated EER power amplifiers," in *Proc. IEEE WAMICON*, Apr. 2013, pp. 1–4.
[19] S.-M. Yoo *et al.*, "A class-G switched-capacitor RF power amplifier," *IEEE J. Solid-State Circuits*, vol. 48, no. 5, pp. 1212–1224, May 2013.
[20] H. Jin *et al.*, "Efficient digital quadrature transmitter based on IQ cell sharing," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 168–170.
[21] W. Yuan, V. Aparin, J. Dunworth, L. Seward, and J. S. Walling, "A quadrature switched capacitor power amplifier," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1200–1209, May 2016.
[22] M. S. Alavi, R. B. Staszewski, L. C. N. de Vreede, and J. R. Long, "A Wideband 2×13-bit all-digital I/Q RF-DAC," *IEEE Trans. Microw. Theory Tech.*, vol. 62, no. 4, pp. 732–752, Apr. 2014.
[23] W. Yuan and J. S. Walling, "A multiphase switched capacitor power amplifier," *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1320–1330, May 2017.
[24] E. W. McCune, "Concurrent polar and quadrature modulator," in *Proc. Wireless Microw. Technol. Conf. (WAMICON)*, Jun. 2014, pp. 1–4.
[25] E. W. McCune, "Wideband phase modulation methods and apparatus," U.S. Patent 0266089, Oct. 10, 2013.
[26] Z. Bai, D. Johnson, A. Azam, and J. S. Walling, "A 12 bit split-array switched capacitor power amplifier in 130 nm CMOS," in *Proc. IEEE SOC Conf.*, Sep. 2016, pp. 1–4.
[27] Z. Bai, W. Yuan, A. Azam, and J. S. Walling, "A split-array, C-2C switched-capacitor power amplifier in 65 nm CMOS," in *IEEE Radio Freq. Integr. Circuits Symp. Dig. Papers*, Jun. 2017, pp. 336–339.
[28] R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation*, 3rd ed. Piscataway, NJ, USA: IEEE Press, 2010.
[29] S. P. Singh, A. Prabhakar, and A. B. Bhattacharyya, "C-2C ladder voltage dividers for application in all-MOS A/D convertors," *Electron. Lett.*, vol. 18, no. 12, pp. 537–538, Jun. 1982.
[30] S. W. Lee, H. J. Chung, and C. H. Han, "C-2C digital-to-analogue converter on insulator," *Electron. Lett.*, vol. 35, no. 15, pp. 1242–1243, Jul. 1999.
[31] W. Xiong, Y. Guo, U. Zschieschang, H. Klauk, and B. Murmann, "A 3-V, 6-bit C-2C digital-to-analog converter using complementary organic thin-film transistors on glass," *IEEE J. Solid-State Circuits*, vol. 45, no. 7, pp. 1380–1388, Jul. 2010.
[32] Y. Han and D. J. Perreault, "Analysis and design of high efficiency matching networks," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1484–1491, Sep. 2006.
[33] Y. Li and Y. Lian, "Improved binary-weighted split-capacitive-array DAC for high-resolution SAR ADCs," *Electron. Lett.*, vol. 50, no. 17, pp. 1194–1195, Aug. 2014.
[34] S. P. Singh, A. Prabhakar, and A. B. Bhattcharyya, "C-2C ladder-based D/A converters for PCM codecs," *IEEE J. Solid-State Circuits*, vol. SSC-22, no. 6, pp. 1197–1200, Dec. 1987.
[35] B. Serneels, M. Steyaert, and W. Dehaene, "A high speed, low voltage to high voltage level shifter in standard 1.2 V 0.13 μm CMOS," *ACM Analog Integr. Circuits Signal Process.*, vol. 55, pp. 85–91, Jan. 2008.
[36] A. Azam, Z. Bai, W. Yuan, and J. S. Walling, "SCPA revolution: Linearization of multiphase SCPAs," in *Proc. IEEE CICC*, Austin, TX, USA, Apr. 2017, pp. 1–8.
[37] R. Bhat and H. Krishnaswamy, "A watt-level 2.4 GHz RF I/Q power DAC transmitter with integrated mixed-domain FIR filtering of quantization noise in 65 nm CMOS," in *Proc. IEEE RFIC Symp.*, Jun. 2014, pp. 413–416.
[38] M. Hashemi, Y. Shen, M. Mehrpoo, M. S. Alavi, and L. C. N. de Vreede, "An intrinsically linear wideband polar digital power amplifier," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3312–3328, Dec. 2017.
[39] V. Vorapipat, C. S. Levy, and P. M. Asbeck, "A class-G voltage-mode Doherty power amplifier," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3348–3360, Dec. 2017.
[40] J. Park, Y. Wang, S. Pellerano, C. Hull, and H. Wang, "A 24 dBm 2-to-4.3 GHz wideband digital power amplifier with built-in AM-PM distortion self-compensation," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 230–231.

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