

A Noise Reconfigurable All-Digital Phase-Locked Loop Using a Switched Capacitor-Based Frequency-Locked Loop and a Noise Detector

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Abstract—Programmability is one of the most significant advantages of a digital phase-locked loop (PLL) compared with a charge-pump PLL. In this paper, a digital PLL that extends programmability to include noise is introduced. A digitally controlled oscillator (DCO) using a switched capacitor for frequency feedback is proposed to maintain a constant figure of merit while reconfiguring its noise performance. The proposed DCO offers an accurate and linear frequency tuning curve that is insensitive to environmental changes. A noise detection circuit using the statistical property of a bang-bang phase and frequency detector is proposed to autonomously adjust the output noise level depending on the noise specification. A prototype design is fabricated in a 28-nm FDSOI process. The integrated phase noise of the proposed PLL can be configured from 2.5 to 15 ps, while the power consumption ranges from 1.7 to 5 mW.

Index Terms—All-digital phase-locked loop (ADPLL), clock generation, linearization, noise reconfiguration, phase-locked loop (PLL), switched capacitor.

I. INTRODUCTION

RECENTLY, all-digital phase-locked loops (ADPLLs) have been widely adopted for their small size, configurability, and portability [1]–[3]. Although an ADPLL is less susceptible to environmental variation compared with its analog counterparts, it is still affected by process and temperature changes. This leads to overly restrictive design specifications to ensure robust performance over the entire process and temperature range, causing a power penalty. For instance, gain of a digitally controlled oscillator (DCO) and a phase detector are the dominant factors that can cause variation in the loop dynamics. When a time-to-digital converter (TDC) is used as a phase detector, its delay elements are susceptible to environmental variation, so its quantization step represented as unit delay of the TDC is variable [4]–[9]. A 1-bit TDC or bang-bang phase frequency detector (BBPFD) is usually

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considered to operate independently of environmental changes because it does not have a delay element. However, the output amplitude of a BBPFD is fixed as 1 and 0 regardless of the input amplitude, making the input-to-output ratio dependent solely on the input amplitude [10]–[12]. Thus its gain is dependent on the amplitude of the input signal, which comes from DCO phase noise in a digital PLL. Therefore, the need for a DCO design, which provides stable gain and noise, is emphasized in a BBPFD-based digital PLL in order to ensure robust operation under the environmental changes.

Reusability also contributes to variation in PLL operation. The increased fabrication, design, and verification costs in the latest technologies have led to a demand for reusability. Reusability also reduces the development time of a product. However, there is a classic tradeoff between productivity and efficiency. A generic PLL should cover a wide range of specifications. Thus, it cannot be optimized for any specific product and will inevitably result in wasted energy.

There are a few requirements for a generic PLL. First, a generic PLL must have a wide frequency range to make it suitable for many products. Noise optimization for both short-term and long-term jitters is required to broaden its application space. Reconfigurability of the PLL mode is beneficial so that it can operate near an energy-optimal point in many applications. A charge-pump PLL is a well-known architecture showing robust operation. However, its analog nature creates problems such as a large loop filter size and limited reconfiguration ability in deep submicrometer technologies. For instance, digital loop filter reconfiguration is much more flexible with less area overhead compared to a charge-pump PLL using current digital-to-analog converter (DAC) and loop filter switches [8]. In addition, two-point modulation for the spread spectrum can be done easily without employing addition DAC [13]. Delta-sigma modulator (DSM) noise cancellation in a fractional-N mode is also more straightforward with high accuracy and less overhead, whereas a charge-pump PLL requires additional charge pump and pulselwidth control and suffers from mismatch [6], [14]. A multiplying delay-locked loop (MDLL) offers the advantage of reduced oscillator noise by refreshing the oscillator phase with a reference [15]. Nevertheless, its limited multiplication ratio and large period jitter at edge insertion make the MDLL an undesirable architecture for a generic PLL [16]. On the other hand, a digital PLL can provide robust operation across wide input and output

frequency ranges. In addition, its digital nature helps make it small and reconfigurable in the latest technology. Therefore, a digital PLL offers an attractive architecture to meet the requirements of a generic PLL.

A DCO is considered the most important building block of a generic digital PLL for a couple reasons. First, the output phase noise is mostly governed by DCO noise, especially when a ring oscillator is used. An *LC* oscillator reduces the noise significantly but is difficult to adopt in a generic PLL due to the frequency range and size requirements. Noise filtering techniques have been proposed to improve the phase noise in a ring oscillator [17], [18]. However, their figure of merit (FoM) is still worse than the theoretical limit of a ring oscillator [19] due to the additional power consumption and noise generation of the frequency detection circuit. Therefore a ring oscillator structure that can operate near its theoretical limit [19] is desirable. Second, a DCO's gain and frequency range affect the performance of a PLL significantly. Nevertheless, the gain and frequency range vary significantly because its delay relies on the intrinsic parameters of the transistors. The change in the DCO gain results in variation of the PLL loop bandwidth as it moves away from the optimal point. Therefore, an accurate and linearized frequency tuning curve is required to maintain a constant loop bandwidth.

In this paper, we implemented a digital PLL with a nested frequency-locked loop (FLL) that linearizes the DCO frequency tuning curve, providing stable gain. Therefore, the loop dynamics are insensitive to environmental variations. We propose a noise reconfiguration scheme using a noise reconfigurable DCO to create a tradeoff between power and noise. We furthermore propose a noise detection circuit that uses the statistical behavior of BBPFD to self-adjust the noise depending on the noise specification.

II. PROPOSED APPROACH

A. Basic Concept

The proposed design adopts an FLL structure using a switched capacitor for the frequency feedback [20]–[26]. Its basic concept is introduced in Fig. 1. The input current I_{IN} is generated by regulating a resistor R_0 with the voltage V_R . The feedback current I_F is defined by the following equation:

$$I_F = C_{sw} V_{sw} f_{out} \quad (1)$$

where C_{sw} , V_{sw} , and f_{out} are switching capacitance, voltage on C_{sw} , and output frequency, respectively. Assuming a large gain from the frequency detection block, I_F should be equal to I_{IN} in the steady state. Therefore, the output frequency can be calculated using the following equation:

$$\begin{aligned} C_{sw} V_{sw} f_{out} &= \frac{V_R}{R_0} \\ f_{out} &= \frac{V_R}{V_{sw}} \frac{1}{R_0 C_{sw}}. \end{aligned} \quad (2)$$

When the identical voltage is used for V_R and V_{sw} , the oscillation frequency of the FLL is defined in the following equation:

$$f_{out} = \frac{1}{R_0 C_{sw}}. \quad (3)$$

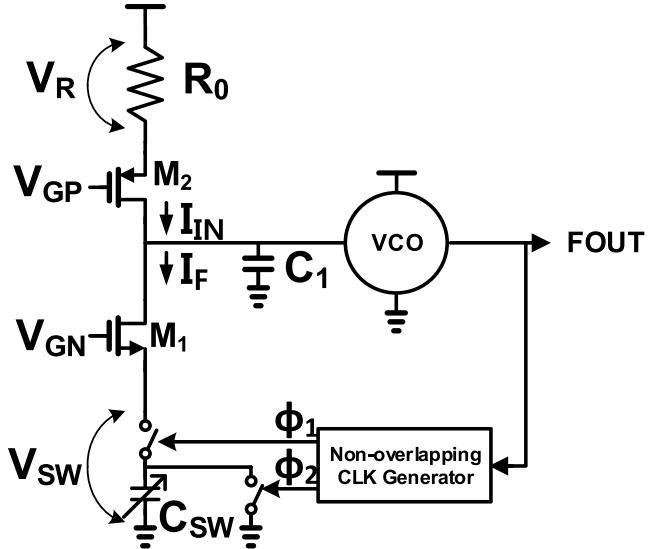


Fig. 1. Conceptual schematic of an FLL using a switched capacitor frequency feedback

Therefore, the PLL loop can tune either R_0 or C_{sw} in order to lock the FLL frequency to the PLL target frequency.

Conventional methods of DCO implementation includes a gate voltage control of a current starving transistor [27], a series resistance control to load capacitor [28] or to supply voltage [29], a delay cell size control [30] or a digital current control for a current-controlled oscillator [31], all relying on the physical device characteristics, and it is difficult to achieve high linearity or process, voltage, temperature (PVT) invariance [24]. In contrast, an FLL using switched capacitor can accurately control the output frequency because it is explicitly determined as (3) using a negative feedback loop [20]–[26].

As an example, Fig. 2 shows simulated frequency tuning curves of conventional and proposed DCOs. Fig. 2(a) shows a conventional case where a DAC is attached to a current starved voltage-controlled oscillator (VCO) to form a DCO that shows a non-linear and PVT dependent frequency tuning curve. In contrast, a DCO with the proposed scheme demonstrates a highly linear and accurate tuning curve, as shown in Fig. 2(b).

B. Loop Dynamics of the Proposed FLL

In this section, the loop dynamics of the proposed FLL are analyzed. First, the feedforward path of the FLL is from the output current generated by the frequency detection block to the output frequency of the DCO marked with a dotted line in Fig. 3. The control voltage v_{ctrl} is generated by the output current i_o multiplied by the output impedance of the detection block as shown in the following equation:

$$\begin{aligned} r_{out} &= (R_0 + r_{op}(1 + g_{mp}R_0)) \parallel (R_{eq} + r_{on}(1 + g_{mn}R_{eq})) \\ &\simeq r_{op}R_0g_{mp} \parallel r_{on}R_{eq}g_{mn} \end{aligned} \quad (4)$$

where r_{op} , r_{on} , g_{mp} , and g_{mn} are PMOS output resistance, NMOS output resistance, PMOS transconductance, and NMOS transconductance, respectively. Assuming $r_{op} = r_{on} = r_o$, and M_1 and M_2 are in a subthreshold region so that their transconductance is maximized to I_{bias}/mvT , r_{out} can be

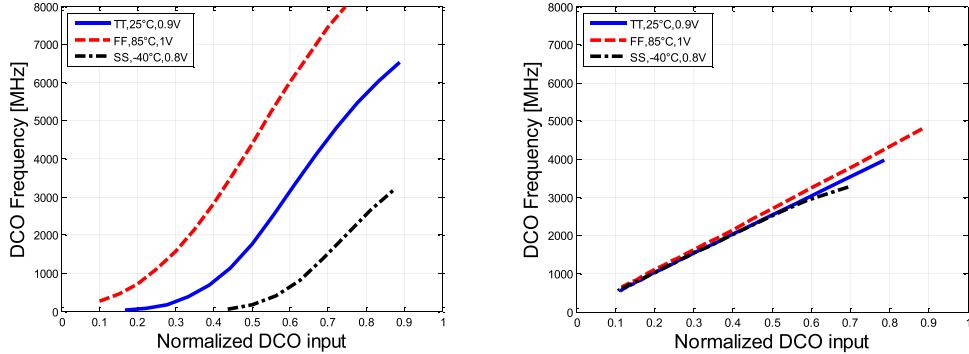


Fig. 2. Simulated frequency tuning curves. (a) With DAC attached to a VCO. (b) Proposed FLL using switched capacitor frequency feedback.

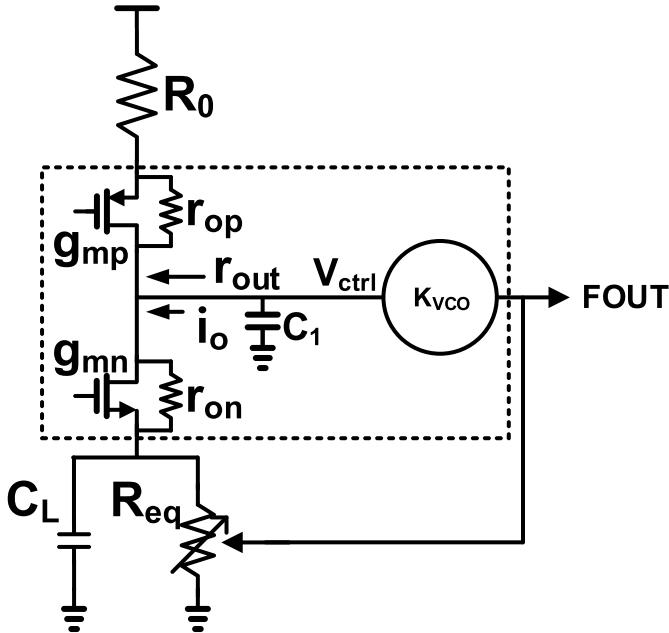


Fig. 3. Simplified schematic of the proposed FLL for the analysis of the feedforward transfer function.

simplified to $(r_o R_0 I_{bias} / 2m v_T)$ where m is $1 + C_d/C_{ox}$ and C_d and C_{ox} are depletion and oxide capacitances, respectively. Then, v_{ctrl} can be found as

$$v_{ctrl} = z_{out} i_o = \frac{r_{out}}{1 + s \cdot r_{out} C_1} i_o. \quad (5)$$

The output frequency f_{out} can be calculated by multiplying the gain for the VCO, K_{VCO} , to (5)

$$f_{out} = \frac{K_{VCOR_{out}}}{1 + s \cdot r_{out} C_1} i_o. \quad (6)$$

Then, the feedforward transfer function from the output current of the frequency detector to the output frequency is

$$H_{ff}(s) = \frac{f_{out}}{i_o} = \frac{K_{VCOR_{out}}}{1 + s \cdot r_{out} C_1}. \quad (7)$$

Note that $1/r_{out}C_1$ is the dominant pole of the FLL.

To analyze the feedback path of the proposed topology, we first need to analyze the transfer function of the switched capacitor. f_{out} serves as an input to the switched capacitor, and its equivalent resistance r_{eq} is the output. Then, the transfer

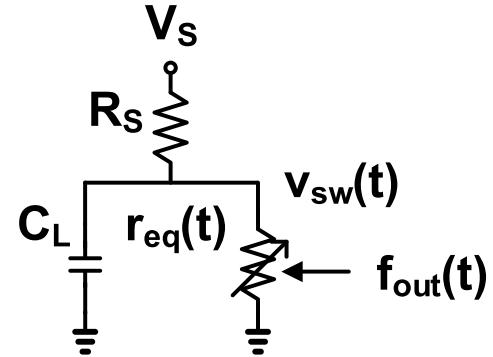


Fig. 4. Simplified and linearized schematic at the source of the M_1 for the analysis of feedback transfer function.

function of the switched capacitor is

$$r_{eq} = \frac{\partial i_f}{\partial f_{out}} = \frac{\partial}{\partial f_{out}} \left(\frac{1}{C_{sw} f_{out}} \right) = -\frac{1}{C_{sw} f_{out}^2}. \quad (8)$$

The change in r_{eq} results in a change in the output current of M_1 by modulating its gate-to-source voltage. Fig. 4 shows the linearized circuit diagram at the source of M_1 . R_s is the source resistance of M_1 (shown in Fig. 1), which is expressed as $1/g_{m1}$. C_L is a capacitor connected in parallel to the switched capacitor to lower the ripple magnitude. V_s is a virtual source voltage that provides dc voltage on the switched capacitor. v'_{sw} is the voltage on the switched capacitor, and v_{sw} is the voltage on the switched capacitor excluding the sawtooth ripple caused by the switching operation. Then, V_s can be defined as

$$V_s = \left(1 + \frac{R_s}{R_{eq}} \right) V_{sw} \quad (9)$$

where V_{sw} is the dc voltage on the switched capacitor, which is 250 mV in this design. Then, v_{sw} can be found as

$$v_{sw}(t) = \frac{r_{eq}(t)}{R_s + r_{eq}(t)} V_s. \quad (10)$$

Therefore, the transfer function from the change of r_{eq} to the change of v_{sw} is determined using the following equation:

$$\frac{\partial v_{sw}}{\partial r_{eq}} = \frac{\partial}{\partial r_{eq}} \left(\frac{r_{eq}(t)}{R_s + r_{eq}(t)} V_s \right)_{r_{eq}(t)=R_{eq}} = \frac{R_s}{(R_{eq} + R_s)^2} V_s. \quad (11)$$

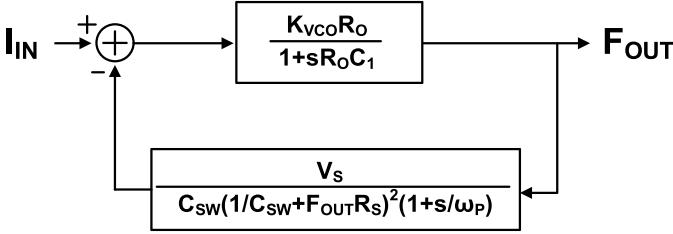
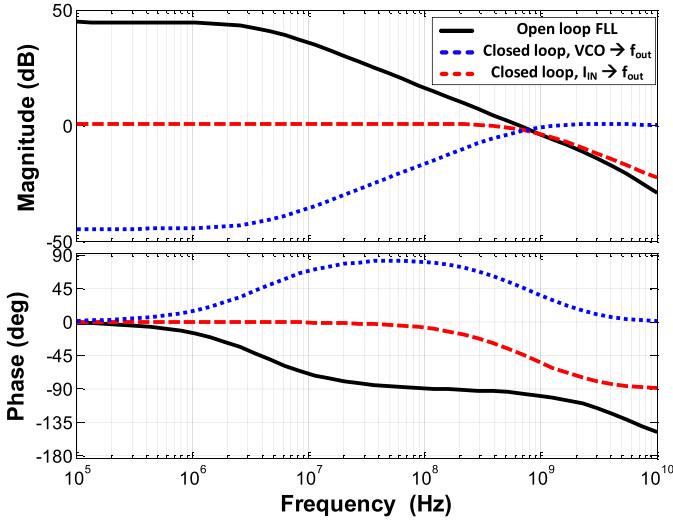


Fig. 5. Linear model of the proposed FLL.

Fig. 6. Bode plot of open-loop transfer function and closed transfer functions of the proposed FLL when V_s , K_{VCO} , R_s , f_{out} , and C_{SW} are 0.25 V, 15 GHz/V, 17 Ω, 2 GHz, and 7.5 pF, respectively.

Note that C_L is ignored for simplicity in (8). The gain from f_{out} to v_{sw} is calculated by combining (8) and (11) as shown in the following equation:

$$\frac{\partial v_{sw}}{\partial f_{out}} = \frac{\partial v_{sw}}{\partial r_{eq}} \frac{\partial r_{eq}}{\partial f_{out}} = -\frac{1}{C_{sw} f_{out}^2} \frac{R_s V_s}{(R_{eq} + R_s)^2} \frac{1}{(1 + s/\omega_{p2})} \\ = -\frac{R_s V_s}{C_{sw}(1/C_{sw} + f_{out} R_s)^2} \frac{1}{(1 + s/\omega_{p2})}. \quad (12)$$

ω_{p2} is the secondary pole generated by C_L and parallel resistance of R_s and R_{eq}

$$\omega_{p2} = \frac{1}{C_L(R_s \parallel R_{eq})}. \quad (13)$$

Finally, the feedback transfer function from f_{out} to the feedback current i_f is determined by multiplying $-g_{m1}$ by v_{sw}

$$H_{fb}(s) = -g_{m1} \frac{\partial v_{sw}}{\partial f_{out}} = \frac{V_s}{C_{sw}(1/C_{sw} + f_{out} R_s)^2(1 + s/\omega_{p2})}. \quad (14)$$

The linear model of the FLL is shown in Fig. 5, and its open loop transfer function (black) is shown in Fig. 6 when V_s , K_{VCO} , R_s , f_{out} , and C_{sw} are 0.25 V, 15 GHz/V, 17 Ω, 2 GHz, and 7.5 pF, respectively. A wide regulation bandwidth (f_{BW}) of more than 500 MHz is achieved.

The closed-loop gain is determined by the feedback factor using the following equation assuming a large feedforward

path gain:

$$1/H_{fb}(0) = \frac{C_{sw}(1/C_{sw} + f_{out} R_s)^2}{V_s} [Hz/A]. \quad (15)$$

To minimize the gain from the noise current to the output frequency, R_s must be minimized. However, given the dc bias current of I_{bias} , there is a limit to how much the transconductance can be increased, which is subthreshold transconductance, I_{bias}/mv_T . Therefore, the minimum closed-loop gain can be found as the following:

$$A_{noise} = \frac{C_{sw}(1/C_{sw} + f_{out} R_s)^2 I_{bias}}{V_s} \frac{f_{out}}{f_{out}} \\ = \frac{C_{sw}(1/C_{sw} + R_s/R_{eq} C_{sw})^2 I_{bias}}{(1 + R_s/R_{eq}) V_{sw}} \frac{f_{out}}{f_{out}} \\ = \frac{(1 + R_s/R_{eq})^2 I_{bias}}{(1 + R_s/R_{eq}) C_{sw} V_{sw} f_{out}} = 1 + \frac{R_s}{R_{eq}} \quad (16)$$

$$A_{noise,min} = 1 + \frac{mv_T/I_{bias}}{1/f_{out} C_{sw}} = 1 + \frac{mv_T}{V_{sw}}. \quad (17)$$

It can be seen that a large V_{sw} results in reduced noise gain; however, it also reduces the control voltage range. Therefore, a tradeoff is made in the proposed design to set V_{sw} to ten times v_T , allowing a 10% increase in noise gain while maintaining 400-mV control voltage range with 1-V supply. A bode plot of the closed-loop transfer function from the current input to the frequency output is displayed in Fig. 6. The noise generated by the detection circuits, primarily due to the switched capacitor and biasing resistor, is low-pass filtered at the loop bandwidth.

C. Linearized Loop Dynamics of the PLL

The linearized loop dynamics of the proposed PLL follows the conventional formula [11], [12], [32], [33] except for the parasitic nondominant pole added by the FLL:

$$HOLG(s) = \frac{T_{REF} K_{PD} K_{DCO} K_P}{s \cdot M} \left(1 + \frac{\omega_z}{s}\right) \frac{1}{1 + s/\omega_{FLL}} \quad (18)$$

where $K_{PD} = G/\sqrt{2\pi\sigma_{PLL}^2}$ [11], $\omega_z = K_I/(K_P T_{REF})$, and σ_{PLL} is the PLL output jitter. G is 1 when the PLL limit cycle dominates σ_{PLL} and 2 when DCO noise dominates σ_{PLL} [11]. M and T_{REF} are the frequency multiplication ratio and the period of reference clock, respectively. Note that (18) is equal to [32, eq. (7)] with the DCO period gain k_T replaced using the DCO frequency gain, K_{DCO} ($k_T = K_{DCO} T_{REF}^2/M^2$). Another important observation on K_{DCO} is that it is half of the frequency change Δf_P caused by proportional path control. It is because +1 and -1 outputs of BBPFD corresponds to the DCO frequency change of $+\Delta f_P/2$ and $-\Delta f_P/2$ making effective frequency gain of DCO be $\Delta f_P/2$. $1/(1 + s/\omega_{FLL})$ is the parasitic pole generated by the FLL, and ω_{FLL} can be approximated to $2\pi f_{BW}$. Note that the closed-loop transfer function of the FLL is simplified to a first-order system in (18). As f_{BW} is order-of-magnitude higher compared to the unit gain frequency of $HOLG(s)$, the effect of this parasitic pole is negligible. In Fig. 7, open-loop transfer function of the proposed PLL is depicted when T_{REF} , K_{PD} , K_{DCO} , K_P , M ,

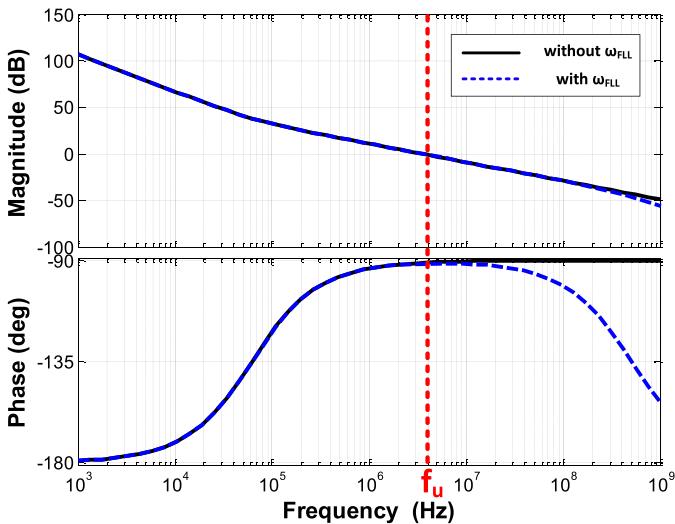


Fig. 7. Open-loop transfer function of the proposed PLL.

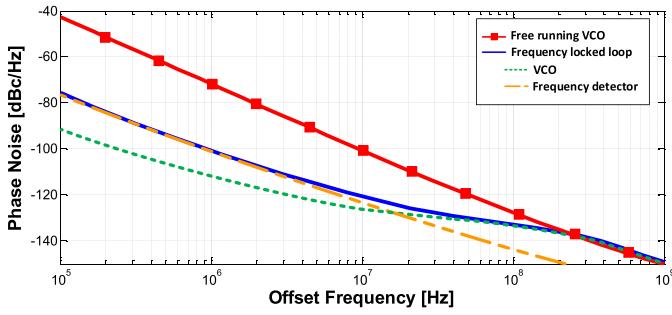


Fig. 8. Simulated phase noise curves of the free running VCO (red line) and the proposed FLL (blue curve).

ω_z , and ω_{FLL} are 20 n, 6.7×10^{10} , 650 k, 1, 40, 390 k, and 3.1 G, respectively. It can be seen that the effect of ω_{FLL} is negligible in the PLL loop dynamics.

III. NOISE ANALYSIS

One of the merits of the proposed architecture is that the output noise of the FLL is mostly determined by the frequency detection circuit. The VCO noise is high-pass filtered at the FLL bandwidth so that the noise becomes negligible when calculating the integrated phase noise, as shown in the closed-loop transfer function from the VCO noise to f_{out} [see Fig. 6 (blue dotted line)]. The noise generated by the detection circuit dominates the output noise across most of the frequency range because f_{BW} is large. Phase noise simulation results of the proposed FLL (blue line) and a free running VCO (red line) are shown in Fig. 8. The VCO noise is high-pass filtered at the FLL bandwidth (208 MHz), and the lower frequency noise is dominated by the detection circuits.

To calculate the noise property of the detection circuit, we first need to analyze the current noise generated by the switched capacitor. Fig. 9 shows the transient waveform at the top node of C_{sw} , V_c . The sampling operation happens twice per f_{out} cycle, once for charging it to V_{sw} and once for

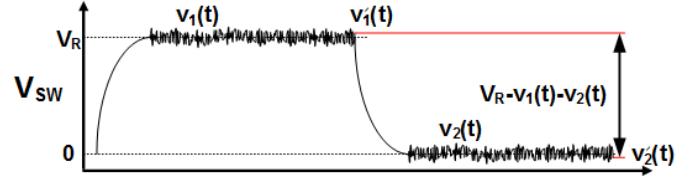
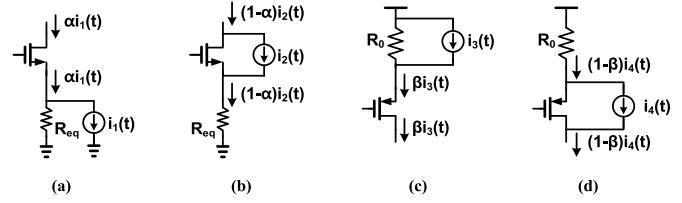
Fig. 9. Transient waveform at the top node of C_{sw} .

Fig. 10. Current division branches in the frequency detection block.

discharging it to ground. In each sampling process, kT/C noise with bandwidth $1/2f_{\text{out}}$ is generated, so its power spectral density can be written as

$$S_{v1}(f) = S_{v2}(f) = \frac{2kT}{C_{\text{sw}}f_{\text{out}}} \quad (19)$$

where v_1 and v_2 are the sampled voltages at V_c . The amount of charge injected at every switching cycle to V_{sw} can be written as $C_{\text{sw}}(v_1(t) - v_2(t))$, so the noise current of the switched capacitor can be calculated using the following equation:

$$i_1(t) = C_{\text{sw}}f_{\text{out}}(v_1(t) - v_2(t)). \quad (20)$$

As v_1 and v_2 are uncorrelated, the power spectral density of the switched capacitor noise can be written as the following equation:

$$\overline{i_1^2} = 4kTf_{\text{out}}C_{\text{sw}} = 4kT\frac{1}{R_{\text{eq}}}. \quad (21)$$

Note that the noise generated by the switched capacitor is equal to the noise of a physical resistor, whose size is equal to R_{eq} .

Then, we need to analyze the current division branches at the sources of M_1 and M_2 . First, the current division ratio at the source of M_1 is analyzed in Fig. 10. The equivalent current noise from the switched capacitor $i_1(t)$ is divided by the impedance ratio of R_{eq} and R_s

$$i_{\text{out},1} = \frac{R_{\text{eq}}}{R_{\text{eq}} + R_s}i_1 = \alpha i_1 = \frac{1}{A_{\text{noise}}}i_1 \quad (22)$$

where $i_{\text{out},1}$ is the amount of current produced at the output of the detection circuit. As mentioned in Section II, it is advantageous to increase the size of M_1 to reduce the noise gain. The current division ratio α is simply

$$\alpha = \frac{\frac{V_{\text{sw}}}{I_{\text{bias}}}}{\frac{V_{\text{sw}}}{I_{\text{bias}}} + \frac{mv_T}{I_{\text{bias}}}} = \frac{V_{\text{sw}}}{V_{\text{sw}} + mv_T}. \quad (23)$$

On the other hand, i_2 , the noise generated by M_1 , is highly degenerated by the source resistance M_1 , and only a small

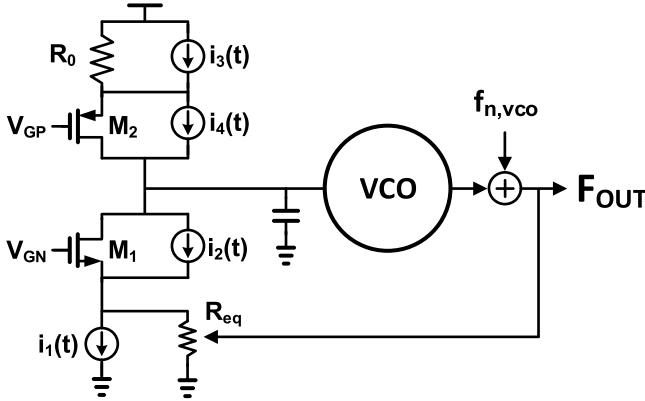


Fig. 11. Schematic of the proposed FLL with the noise sources.

fraction of i_2 is delivered to the output, as described by the following equation:

$$i_{\text{out},2} = (1 - \alpha)i_2. \quad (24)$$

Similarly, the current noise from R_0 and M_2 can be calculated, as described the following equations:

$$i_{\text{out},3} = \beta i_3 \quad (25)$$

$$i_{\text{out},4} = (1 - \beta)i_4 \quad (26)$$

where β is the current division ratio at the source of M_2 , which is defined as the following equation when M_2 is biased in a subthreshold region:

$$\beta = \frac{V_R}{V_R + mv_T}. \quad (27)$$

Fig. 11 shows equivalent noise sources in the detection circuit, $i_{1-4}(t)$. The output frequency noise can be calculated by multiplying the closed-loop gain from the output current of the detection block to the output frequency. The noise contributions from C_{sw} , R_0 , M_1 , and M_2 can be found as follows:

$$L_{C_{\text{sw}}}(f) = \frac{4kT}{I_{\text{bias}}V_{\text{sw}}} \frac{f_{\text{out}}^2}{f^2} \quad (28)$$

$$L_{M_1}(f) = \left(\frac{1-\alpha}{\alpha}\right)^2 \frac{4kT\gamma_n g_{m1}}{I_{\text{bias}}^2} \frac{f_{\text{out}}^2}{f^2} \quad (29)$$

$$L_{R_0}(f) = \frac{\beta^2}{\alpha^2} \frac{4kT}{I_{\text{bias}}V_R} \frac{f_{\text{out}}^2}{f^2} \quad (30)$$

$$L_{M_2}(f) = \left(\frac{1-\beta}{\alpha}\right)^2 \frac{4kT\gamma_p g_{m1}}{I_{\text{bias}}^2} \frac{f_{\text{out}}^2}{f^2}. \quad (31)$$

Note that the noise from M_1 and M_2 are relatively negligible compared with the noise from C_{sw} and R_0 because α and β are close to 1. By rewriting α and β in (28)–(31) using (23) and (27) and by summing all of the noise sources, the overall phase noise can be found as follows:

$$L(f) = \frac{4kT}{I_{\text{bias}}} \left(\frac{1}{V_{\text{sw}}} \left(1 + \frac{\gamma_n mv_T}{V_{\text{sw}}} \right) + A_{\text{noise}}^2 \frac{V_R + \gamma_p mv_T}{(V_R + mv_T)^2} \right) \frac{f_{\text{out}}^2}{f^2}. \quad (32)$$

Detailed derivation on the phase noise is described in Appendixes A and B. The discussion to this point shows that the output noise improves with a larger V_{sw} . A_{noise} is

a function of V_{sw} as well, so increasing V_{sw} helps lower the noise not only from M_1 and C_{sw} but also from M_2 and R_0 . The smaller overdrive voltage of M_1 helps reduce the noise generated by M_1 . Therefore, it is advantageous to maximize the transconductance of M_1 by increasing the width until M_1 operates in the subthreshold region. The latter part of (32) and (B5) show that increasing both V_R and $V_{\text{ov},m2}$ helps reduce the output noise generated by M_1 and R_0 . However, increasing V_R and $V_{\text{ov},m2}$ limits the voltage tuning range of the VCO. As increasing V_R is almost twofold more effective than increasing $V_{\text{ov},m2}$, the size of M_2 should be again maximized until M_2 operates in the subthreshold region given a fixed voltage allocation of V_R and $V_{\text{ov},m2}$ combined. Note that the overall phase noise has I_{bias} in the denominator, so the DCO noise can be reconfigured by tuning the bias current while keeping the bias conditions, V_{sw} , V_R , $V_{\text{ov},m1}$, and $V_{\text{mv},m2}$ constant. For instance, the FLL is configured in a low-noise mode with high current to prioritize noise performance. On the other hand, when power consumption is more important, the FLL is configured in a low-current mode, sacrificing its noise performance.

In an attempt to find an optimal biasing condition on C_{sw} , R_0 , M_1 , and M_2 , the conclusion thus far is to set M_1 and M_2 at subthreshold mode and maximize V_{sw} and V_R . Here, we will discuss a strategy in deciding the optimal ratio between V_{sw} and V_R . First, the voltage assigned to them is defined as V_B as follows:

$$V_B = V_{\text{sw}} + V_R = V_{\text{DD}} - V_{c,\text{range}} - 4v_T \quad (33)$$

where $V_{c,\text{range}}$ is the input voltage range of the VCO to generate the target frequency under the PVT variation. $4v_T$ is subtracted from V_{DD} as well to give sufficient V_{ds} to either M_1 or M_2 . Then, (32) can be rewritten as the following by substituting V_R with $V_B - V_{\text{sw}}$:

$$L(f) = \frac{4kT}{I_{\text{bias}}} \left(\frac{1}{V_{\text{sw}}} \left(1 + \frac{\gamma_n mv_T}{V_{\text{sw}}} \right) + \left(1 + \frac{mv_T}{V_{\text{sw}}} \right)^2 \frac{V_B - V_{\text{sw}} + \gamma_p mv_T}{(V_B - V_{\text{sw}} + mv_T)^2} \right) \frac{f_{\text{out}}^2}{f^2}. \quad (34)$$

The phase noise at 10-MHz offset is shown in Fig. 12 when T , I_{bias} , γ_n , γ_p , v_T , m , and f_{out} are 300 °C, 3 mA, 2/3, 2/3, 26 mV, 1.2, and 2 GHz, respectively. The optimal noise performance is achieved when V_R is almost equal to V_{sw} . The numerical solutions $V_{\text{sw}} = 0.271$ and $V_R = 0.229$ are found when $V_B = 0.5$ after differentiating (34) and setting it equal to 0. Note that V_{sw} is weighted slightly more than V_R because A_{noise} affects both the noise from C_{sw} and V_R .

Equation (34) can be simplified assuming equal V_R and V_{sw} to intuitively understand its theoretical limit in terms of its FOM

$$\begin{aligned} L_{\text{opt}}(f) &= \frac{4kT}{I_{\text{bias}}} \left(\frac{1}{V_{\text{sw}}} \left(1 + \frac{\gamma_n mv_T}{V_{\text{sw}}} \right) + \frac{1}{V_R} \left(1 + \frac{\gamma_p mv_T}{V_R} \right) \right) \frac{f_{\text{out}}^2}{f^2} \\ &= \frac{8kT}{I_{\text{bias}}V_{\text{sw}}} \left(1 + \frac{\gamma_n mv_T}{V_{\text{sw}}} \right) \frac{f_{\text{out}}^2}{f^2}. \end{aligned} \quad (35)$$

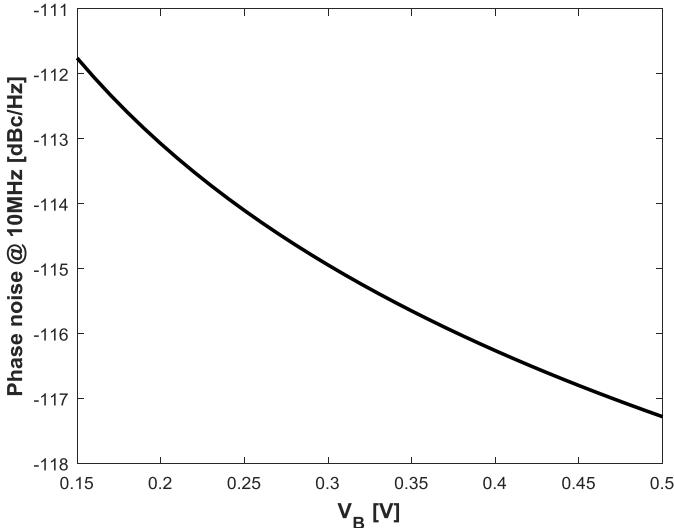


Fig. 12. Phase noise at 10-MHz offset according to (4) when T , I_{bias} , γ_n , γ_p , v_T , and f_{out} are 300 °C, 3 mA, 2/3, 2/3, 26 mV, and 2 GHz, respectively.

Finally, the FoM of the proposed oscillator at its optimal biasing state can be found as the following:

$$\begin{aligned} \text{FoM} &= 10 \log \frac{8kT}{I_{\text{bias}} V_{\text{sw}}} \left(1 + \frac{\gamma_n m v_T}{V_{\text{sw}}} \right) \frac{f_{\text{out}}^2}{f^2} \times \frac{I_{\text{bias}} V_{\text{DD}}}{1 \text{ mW}} \times \frac{f^2}{f_{\text{out}}^2} \\ &= 10 \log \frac{8kT V_{\text{DD}}}{10^{-3} V_{\text{sw}}} \left(1 + \frac{\gamma_n m v_T}{V_{\text{sw}}} \right). \end{aligned} \quad (36)$$

The first observation regarding (36) is that the FoM of the proposed oscillator only depends on the voltage ratio of V_{DD} and V_{sw} , assuming $V_{\text{sw}} \gg \gamma_n v_T$. The theoretical FoM maximum is found when $V_{\text{sw}} = V_{\text{DD}}/2$, in which case $V_B = V_{\text{DD}}$, allowing zero voltage for $V_{c,\text{range}}$, M_1 , and M_2 . It is also assumed that $\gamma_n v_T / V_{\text{sw}} \ll 1$.

$$\text{FoM}_{\min} = 10 \log \frac{8kT V_{\text{DD}}}{10^{-3} V_{\text{DD}}/2} = 10 \log \frac{16kT}{10^{-3}} \approx -161.79. \quad (37)$$

As an example of a practical case, when $V_{\text{DD}} = 1$, $V_{\text{sw}} = V_R = 0.25$, and there is 10% additional power consumption in the VCO and non-overlapping clock generation, the FoM of the proposed oscillator is -158.1 dBc/Hz. As a comparison, the theoretical FoM limit of a CMOS ring oscillator analyzed in [19] is determined as the following:

$$\text{FoM}_{\min, \text{ring}} = 10 \log \frac{7.33kT}{10^{-3}} \approx -165.2. \quad (38)$$

The theoretical limit of the proposed oscillator is approximately 3.3 dB worse than that of a conventional ring oscillator. However, there are several other factors that need to be considered.

- 1) While adding transistors to give frequency tunability to a CMOS ring oscillator, the FoM typically gets worse. On the other hand, frequency tuning of the proposed oscillator can be achieved without FoM penalty. Therefore, the minimum FoM of a conventional ring oscillator is more over-estimated than that of the proposed oscillator.

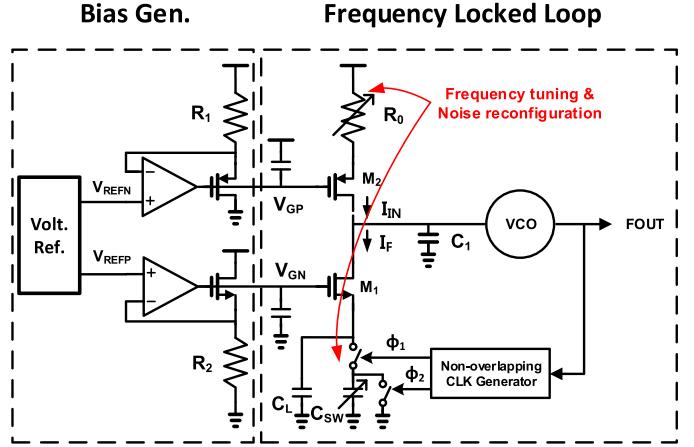


Fig. 13. Block diagram of the proposed digitally controlled oscillator.

- 2) The frequency tuning curve of the proposed oscillator is less sensitive to environmental change as it relies on an RC time constant rather than the transistor speed.
- 3) The proposed oscillator offers a highly linear frequency tuning curve, which is advantageous in the reduction of PLL loop bandwidth variation and two-point modulation [24].
- 4) The proposed oscillator offers noise reconfiguration capability by programming its bias current.

Therefore, the proposed oscillator is more efficient than a conventional ring oscillator in many applications.

IV. CIRCUIT IMPLEMENTATION

A schematic of the proposed circuit is shown in Fig. 13. The gate voltages of M_1 and M_2 are generated using replica cells of the ones in the main branch. The amplifiers are designed to consume 500 nW so that the noise generated by those two amplifiers resides only in a very low-frequency range and is filtered by the PLL loop. Low-power voltage references are implemented using the 2-T structure proposed in [34]. R_0 and C_{sw} are used to tune the output frequency and the noise. The size of M_1 and M_2 are tuned together with R_0 and C_{sw} so the voltages on R_0 and C_{sw} do not change depending on their values.

A. Multi-Phase Feedback

C_L is placed in parallel with C_{sw} to minimize the voltage ripple caused by the switching operation. When the switched capacitor is grounded, and only C_L is connected to the source of M_1 , V_{sw} increases by the bias current, reducing the gate to the source voltage of M_1 as shown in Fig. 14(a). Then, C_{sw} is connected to the source of M_1 , causing an abrupt drop at the source voltage. The ripple magnitude is determined by the ratio between C_L and C_{sw} . If a small C_L is used, the voltage ripple becomes large, modulating V_{GS} of M_1 substantially. As M_1 provides a non-linear relationship between its V_{GS} and I_{ds} , such fluctuation can perturb the linearity of the DCO frequency tuning curve. Therefore, C_L must be at least 10× greater than C_{sw} to sufficiently lower the ripple

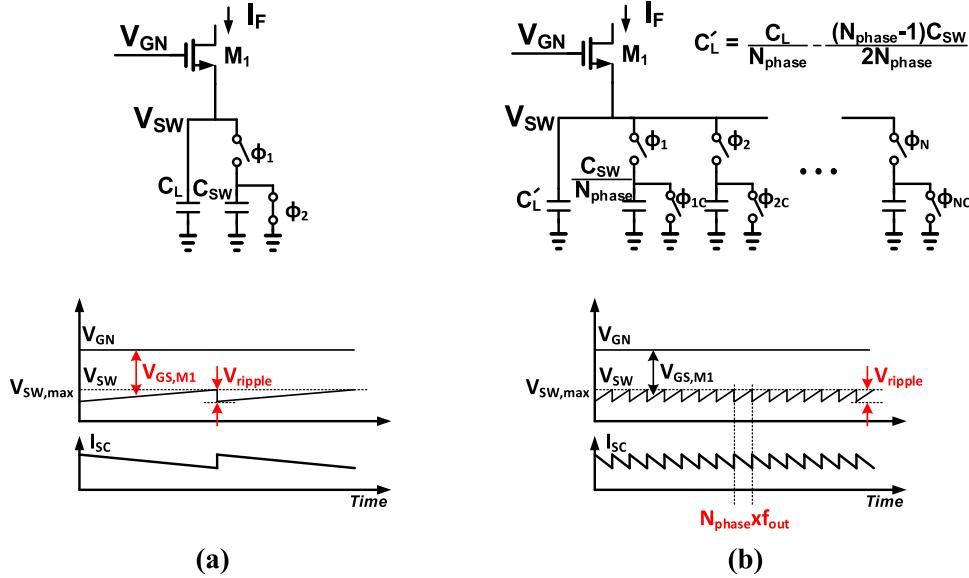


Fig. 14. Voltage ripple caused by the switching operation. (a) When a single phase is used. (b) When multi-phases are used.

magnitude. However, a large C_L incurs low second pole frequency in the FLL, degrading the stability, and causing area penalty. In this paper, we adopted multi-phase feedback from the VCO so that its effective switching frequency becomes N_{phase} times higher, where N_{phase} is the number of VCO phases as shown in Fig. 14(b). Then, the total capacitance connected in parallel with the switching capacitance is reduced by the factor N_{phase} , and it helps to provide higher f_{BW} and phase margin. In addition, the multi-phase feedback helps to greatly reduce the area. As the switching capacitance is reduced by the factor N_{phase} , the total parallel capacitance can also be reduced by the same factor. Furthermore, nearly half of the non-switching capacitors are connected to the source of M_1 , serving as parallel capacitors. Therefore, the size of the additional capacitance is $C_L/N_{phase} - (N_{phase} - 1)C_{SW}/2N_{phase}$, which is approximately 5 pF, while the total switching capacitance is 7.5 pF. Compared with 75 pF, when single-phase feedback is used, 93% of the area is saved.

B. Noise Detector

In this section, a noise detector circuit using the statistical behavior of the BBPFD output is demonstrated. A digital PLL using a BBPFD has a limit cycle due to the non-linearity of the BBPFD. Assuming no DCO noise is present, the DCO control alternates between two numbers neighboring the target frequency at every reference cycle. The BBPFD output also alternates between 1 and 0, and the resulting feedback phase is shown in Fig. 15. The VCO phase drawn in a blue color follows the reference phase. The peak difference between the feedback and reference phase is the magnitude of the limit cycle, Φ_{lmt} . It can be found as the following equation where K_{DCO} is the DCO gain, K_P is the proportional path gain, and K_I is the integral path gain:

$$\Phi_{lmt} = \frac{2\pi K_{DCO}(K_P + K_I)T_{REF}}{M}. \quad (39)$$

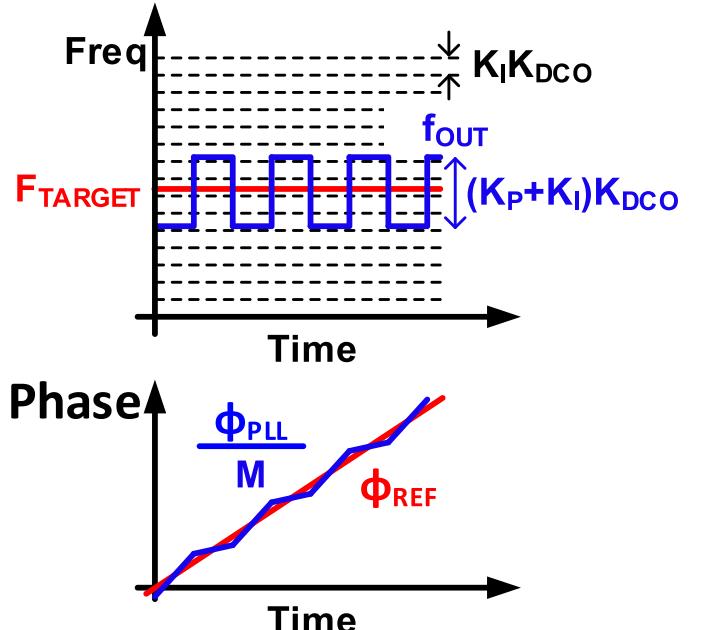


Fig. 15. Behavior of BBPFD-based digital PLL when DCO noise is not present.

When DCO noise presents, it perturbs the DCO output phase, and its magnitude may exceed $\Phi_{lmt}/2$. In such cases, BBPFD produces consecutive 1 or 0 s. In Fig. 16, early is the output of the BBPFD. At times t_1 and t_2 , BBPFD generates either consecutive 1 or 0 s due to the excessive noise of the DCO.

The histogram of the feedback phase is shown in Fig. 17. The DCO phase noise produces a Gaussian distribution in the feedback phase, and the limit cycle offsets the distribution by $\pm\Phi_{lmt}/2$. The shaded region represents the possibility that the accumulated DCO noise exceeds $\Phi_{lmt}/2$, in which case the BBPFD produces either consecutive 1 or 0 s. $\sigma_{PLL,C}$ is the

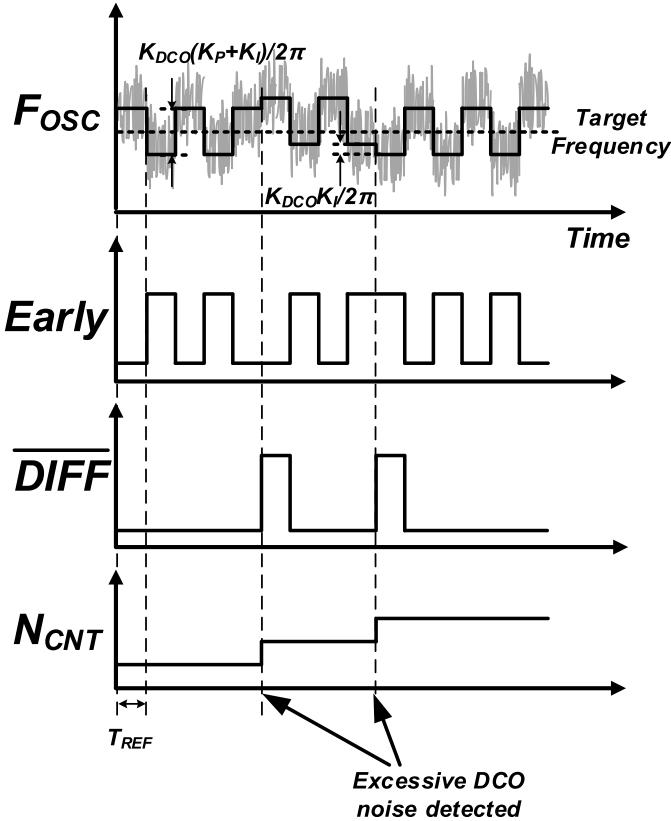


Fig. 16. Transient waveforms (drawn from simulation results) of output frequency (f_{out}), PFD output (early), and the noise detection result (DIFF).

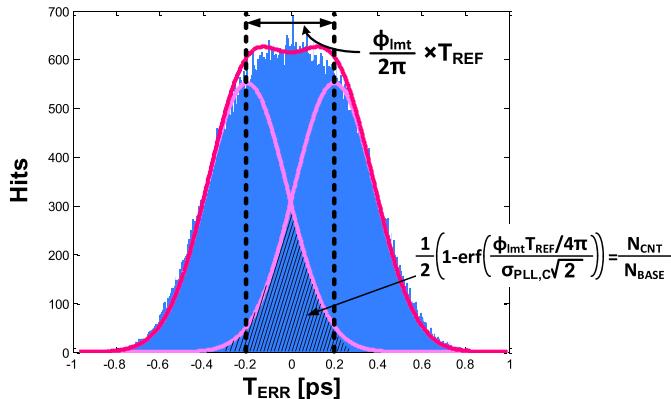


Fig. 17. Simulated histogram of the feedback time error.

continuous random part of the PLL output noise which will be explained at the end of this Section IV-B. A schematic to detect such an event is shown in Fig. 18. The BBPFD output is compared with its previous value, and when they are the same, the noise count is increased by 1. After N_{BASE} cycles of F_{REF} , the noise count N_{CNT} is delivered to the DCO control block. f_{out} is inversely proportional to the switching capacitance as shown in (3). Therefore, K_{DCO} can be accurately determined as a capacitance ratio between total switching capacitance, C_{sw} and unit capacitance, $f_{\text{out}} C_u / C_{\text{sw}}$, assuring robust operation of the noise detector. As the DCO noise is adjusted using the proposed noise detector and the

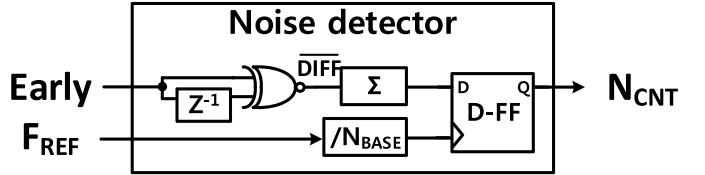


Fig. 18. Proposed noise detection circuit.

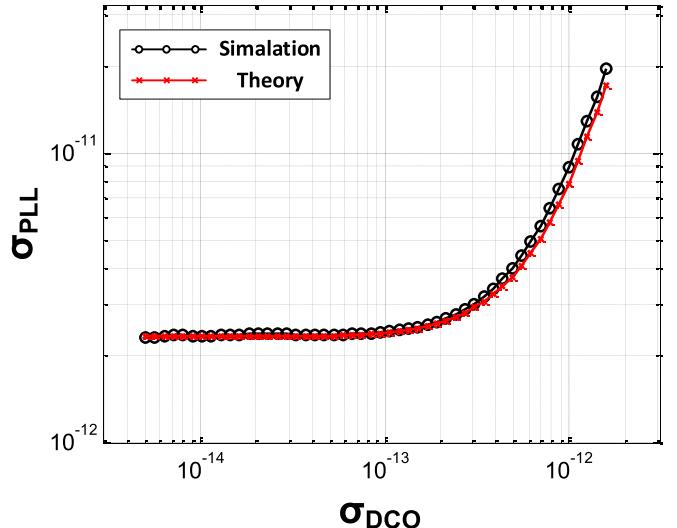


Fig. 19. Simulated PLL output noise as a function of DCO noise.

DCO gain is accurately controlled using a capacitor ratio, the PLL loop dynamics stay largely invariant to environmental changes.

In this part, the PLL bandwidth and output jitter will be derived in terms of the DCO noise and other PLL configuration parameters. The unity gain frequency of the open-loop transfer function of the PLL f_u can be found by equalizing the absolute value of (18) to 1 and it is

$$f_u = \frac{1}{2\pi} \frac{T_{\text{REF}} K_{\text{PD}} K_{\text{DCO}} K_P}{M} = \frac{1}{2\pi} \frac{T_{\text{REF}} K_{\text{DCO}} K_P}{M} \frac{G}{\sqrt{2\pi} \sigma_{\text{PLL}}}. \quad (40)$$

σ_{PLL} is composed of three major elements of the integrated DCO noise ($\sigma_{\text{PLL,DCO}}$), the random noise caused by a random walk of BBPFD input phase ($\sigma_{\text{PLL,rw}}$), and the limit cycle ($\sigma_{\text{PLL,lmt}}$). First of all, $\sigma_{\text{PLL,lmt}}$ can easily be calculated by assuming a noiseless DCO as shown in Fig. 15. As the feedback phase alternates $\pm\Phi_{\text{lmt}}/2$, the PLL jitter can be found as

$$\sigma_{\text{PLL,lmt}} = \frac{\Phi_{\text{lmt}} T_{\text{REF}}}{4\pi} \simeq \frac{K_{\text{DCO}} K_P T_{\text{REF}}^2}{2M}. \quad (41)$$

Assuming there exists a very small DCO noise compared to $\sigma_{\text{PLL,lmt}}$, the input jitter of BBPFD random walks from $-\Phi_{\text{lmt}}/2$ to $+\Phi_{\text{lmt}}/2$. This noise can be assumed to follows a uniform distribution [10], so that $\sigma_{\text{PLL,rw}}$ is:

$$\sigma_{\text{PLL,rw}} = \frac{K_{\text{DCO}} K_P T_{\text{REF}}^2}{\sqrt{12M}}. \quad (42)$$

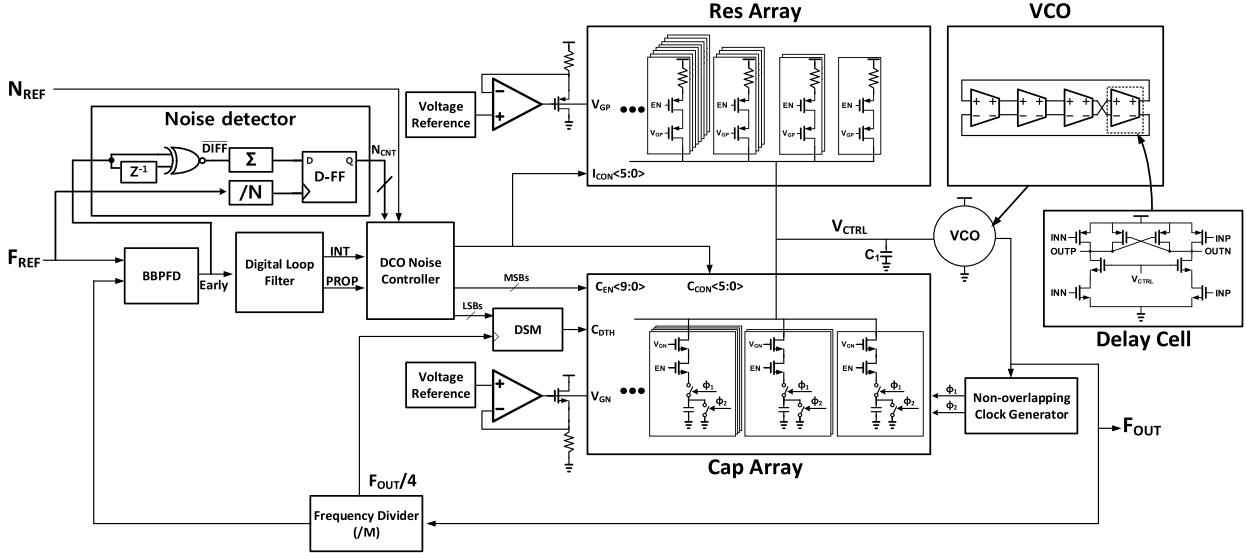


Fig. 20. Detailed schematic of the proposed digital PLL.

Note that standard deviation of the noise injected from the limit cycle behavior and the random walk is $(\sigma_{PLL,lm}^2 + \sigma_{PLL,rw}^2)^{1/2} = K_{DCO}K_P T_{REF}^2 / \sqrt{3} M$ which is equal to [32, eq. (12)].

Assuming that the DCO noise is dominant at the output of the PLL and its flicker noise is negligible compared to the white noise, the PLL output noise induced by DCO, $\sigma_{PLL,DCO}$ can be approximated as a function of σ_{DCO} and f_u as the following [32]:

$$\sigma_{PLL,DCO} = \sigma_{DCO} \sqrt{\frac{f_{out}}{4\pi f_u}} = \sigma_{DCO} \sqrt{\frac{M}{4\pi f_u T_{REF}}}. \quad (43)$$

Assuming $\sigma_{PLL,DCO}$ is dominant compared to $\sigma_{PLL,lm}$ and $\sigma_{PLL,rw}$, σ_{PLL} in (40) can be replaced with $\sigma_{PLL,DCO}$ in (42) and $\sigma_{PLL,DCO}$ can be found as

$$\sigma_{PLL,DCO} = \sigma_{DCO}^2 \frac{\sqrt{\pi} M^2}{\sqrt{2} T_{REF}^2 K_{DCO} K_P G}. \quad (44)$$

Note that $\sigma_{PLL,DCO}$ is proportional to the square of the DCO noise because it exacerbates $\sigma_{PLL,DCO}$ by reducing the phase detector gain as well as by its own power. The total continuous random noise without the limit cycle is

$$\begin{aligned} \sigma_{PLL,C} &= \sqrt{\sigma_{PLL,DCO}^2 + \sigma_{PLL,rw}^2} \\ &= \sqrt{\left(\sigma_{DCO}^2 \frac{\sqrt{\pi} M^2}{\sqrt{2} T_{REF}^2 K_{DCO} K_P G}\right)^2 + \left(\frac{K_P K_{DCO} T_{REF}^2}{\sqrt{12} M}\right)^2}. \end{aligned} \quad (45)$$

The distribution of the total continuous random noise is shifted by $\pm \sigma_{PLL,lm}$ depending on the BBPFD output. Therefore,

the output jitter of the PLL can be found as the following:

$$\begin{aligned} \sigma_{PLL} &= \sqrt{\sigma_{PLL,C}^2 + \sigma_{PLL,lm}^2} \\ &= \sqrt{\left(\sigma_{DCO}^2 \frac{\sqrt{\pi} M^2}{\sqrt{2} T_{REF}^2 K_{DCO} K_P G}\right)^2 + \left(\frac{K_P K_{DCO} T_{REF}^2}{\sqrt{3} M}\right)^2}. \end{aligned} \quad (46)$$

Equation (46) is compared with a behavioral simulation result in Fig. 19 when T_{REF} , K_{DCO} , M , and K_P are 20 n, 400 k, 50, and 1, respectively.

In this paper, we found that the resulting distribution of the continuous random noise can be approximated as a Gaussian distribution when the integrated DCO noise is dominant compared to $\sigma_{PLL,rw}$. Assuming an accurate noise adjustment, $\sigma_{PLL,C}$ can be derived from the equation shown in Fig. 17

$$\sigma_{PLL,C} = \frac{\Phi_{lm} T_{REF} / 4\pi}{\sqrt{2} \cdot \text{erf}^{-1} \left(1 - \frac{2N_{CNT}}{N_{BASE}}\right)} \approx \frac{K_{DCO} K_P T_{REF}^2}{2\sqrt{2} M \cdot \text{erf}^{-1} \left(1 - \frac{2N_{CNT}}{N_{BASE}}\right)}. \quad (47)$$

Finally, f_u and σ_{PLL} can be expressed as the following equations which are independent to the environmental changes. Note that K_{DCO} is replaced to $(M/T_{REF}) \times (C_u/C_{SW})$

$$\sigma_{PLL,C} = \frac{K_P T_{REF} (C_u / C_{SW})}{2\sqrt{2} \text{erf}^{-1} \left(1 - \frac{2N_{CNT}}{N_{BASE}}\right)} \quad (48)$$

$$f_u = \frac{1}{2\pi} \frac{T_{REF} K_{DCO} K_P}{M} \frac{G}{\sqrt{2\pi} \sigma_{PLL}} = \frac{G \cdot \text{erf}^{-1} \left(1 - \frac{2N_{CNT}}{N_{BASE}}\right)}{\pi \sqrt{\pi} T_{REF}}. \quad (49)$$

C. Overall Implementation

Fig. 20 shows a block diagram of the proposed BBPFD-based digital PLL with PI control. A DCO noise controller tunes R_0 and C_{SW} values while keeping their products constant

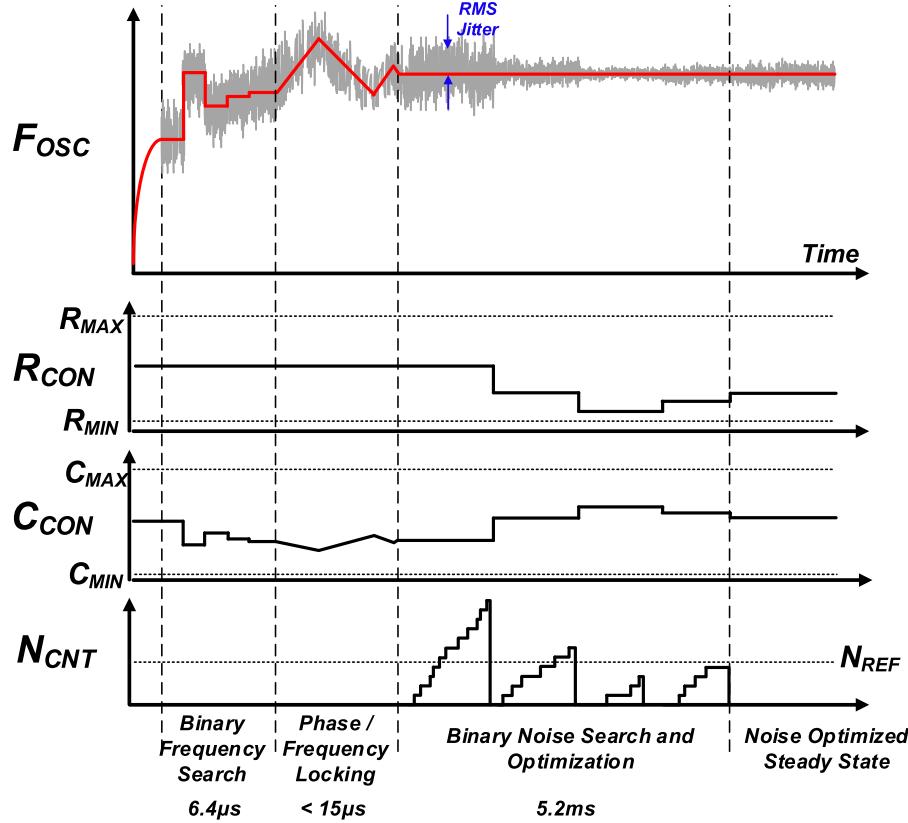


Fig. 21. Transient waveform (drawn from simulation results) of the proposed PLL.

at a value dependent on $N_{\text{CNT}}/N_{\text{BASE}}$, forming a noise self-adjustment loop. Note that I_{bias} is inversely proportional to R_0 as shown in (1) and (2), and the DCO noise is also inversely proportional to I_{bias} as shown in (32). DCO frequency tuning is achieved by controlling C_{sw} . The capacitance in an integral path consists of 6-bit coarse input, 10-bit fine input, and 1-bit dithering input. The proportional path is designed with 5-bit control to maintain constant DCO gain while reconfiguring C_{sw} .

Fig. 21 shows a transient waveform of the proposed PLL. Initially, an automatic frequency control operates to find the switching capacitance that generates the target frequency. Then, the PLL loop is enabled to lock the output phase again using C_{con} . After phase lock is achieved, a binary noise search is enabled using the noise detection block. Overall phase locking is achieved within 10 μs , and the noise locking takes 5.2 ms with 50-MHz reference clock.

V. MEASUREMENT RESULT

The proposed design is fabricated in a 28-nm FDSOI process. The overall area is 0.045 mm². The proposed PLL is tested with 50-MHz input frequency generated using a function generator (Keysight33600A), and its output noise is measured using a spectrum analyzer (Agilent N9030A). Frequency tuning curves of the proposed FLL are measured in Fig. 22. It shows highly linear frequency tuning curve until the VCO tuning range is limited by the supply headroom. Fig. 23 shows the power consumption of the PLL and the

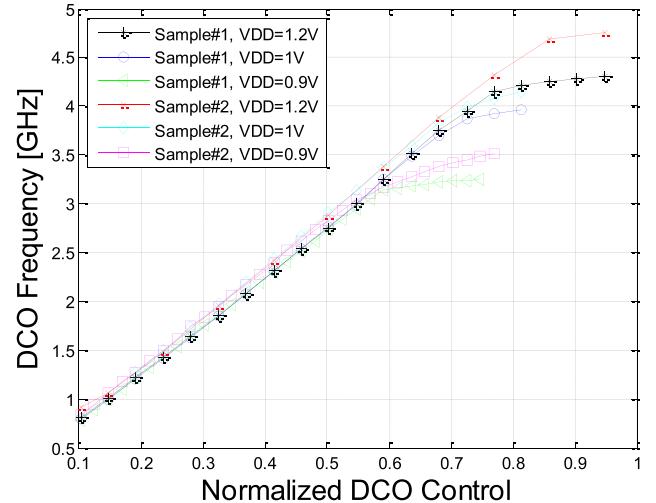


Fig. 22. Measured DCO frequency tuning curve.

integrated phase noise. The integrated output phase noise is inversely proportional to the power consumption, as expected in (32). The integrated jitter can be configured from 2.5 to 15 ps while making a tradeoff with the power consumption from 1.7 to 5 mW. Fig. 24 illustrates the function of the noise detection circuit depending on the configuration of the PLL. $K_{\text{DCO}}K_P$ is changed from 600 kHz/LSB to 4 MHz/LSB and $K_{\text{DCO}}K_I$ is adjusted in accordance with K_P keeping K_P/K_I as 128 assuring the PLL loop stability. The noise count shows a monotone relationship between the DCO noise amount and the noise count enabling the stable operation.

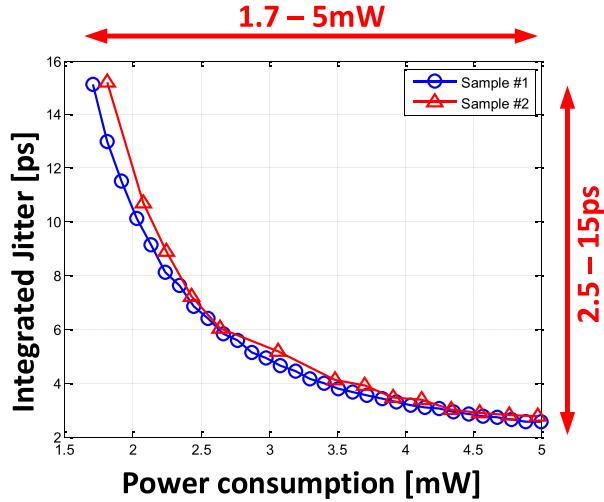


Fig. 23. Measurement results of the integrated phase noise and the power consumption depending on the jitter configuration.

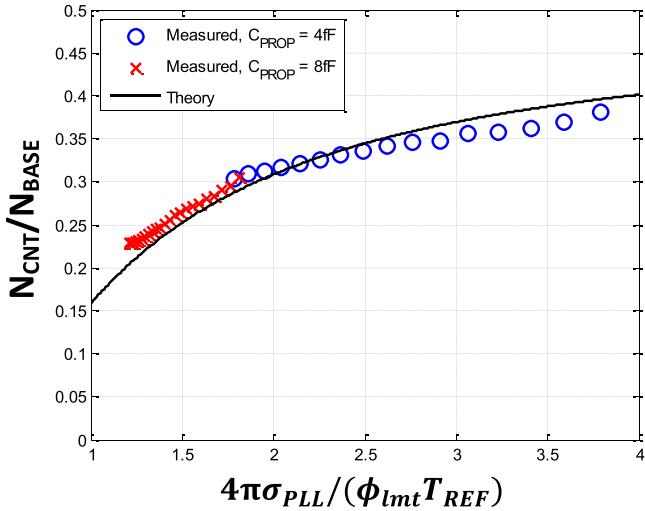


Fig. 24. Measurement results of the noise detector output across varying DCO gain and noise.

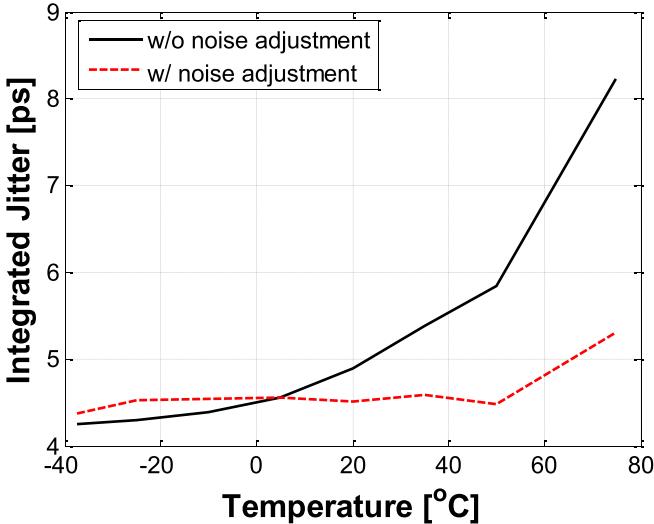


Fig. 25. Measurement results of the integrated jitter depending on the temperature.

The proposed noise detector assumes Gaussian distribution of output noise. However, DSM in the integral path generates quantization noise that does not follow Gaussian distribution,

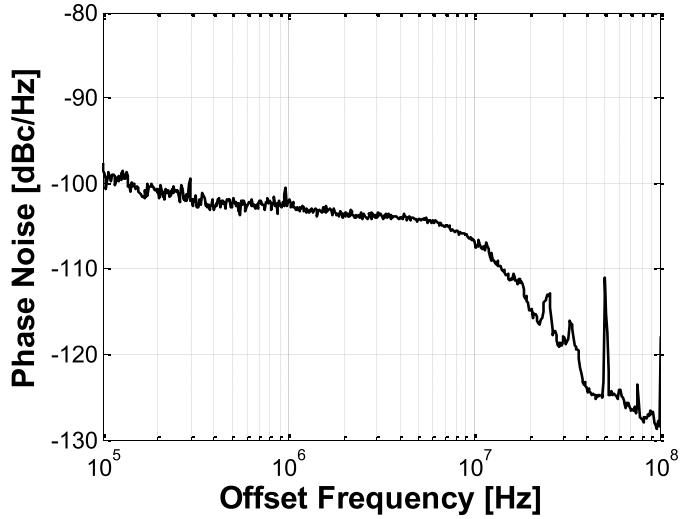


Fig. 26. Phase noise measurement result when f_{out} is 2.4 GHz and the PLL is configured to the lowest noise mode.

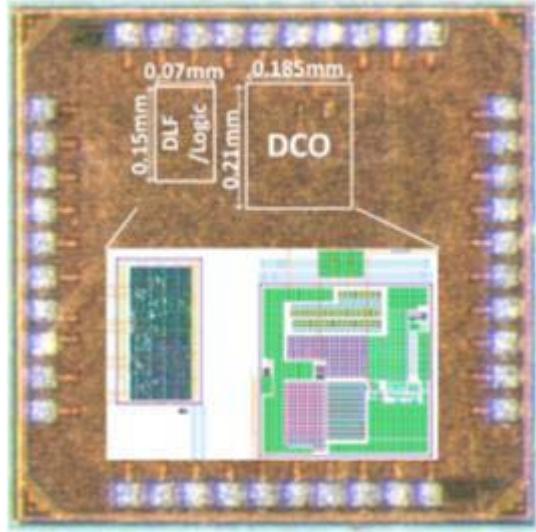


Fig. 27. Die photograph of the proposed design.

and it can cause a discrepancy between the measurement and the theoretical calculation. This effect is more pronounced when the intrinsic DCO noise is small, i.e., when $\sigma_{\text{DCO}}/\Phi_{lmt}$ is small, making DSM quantization noise non-negligible as shown in Fig. 24. The proposed PLL is tested with temperature sweep to verify the operation of noise self-adjustment. The DCO phase noise caused by device thermal noise is linear with temperature as shown in (32), whereas the PLL output jitter is proportional to the square of the DCO jitter because of the reduced bandwidth (42). Therefore, the PLL jitter has a quadratic relationship with temperature as it can be observed in Fig. 25. When the noise adjustment is enabled, the output noise remains relatively constant to the temperature change.

Fig. 26 shows the phase noise measurement results when the output frequency is 2.4 GHz and DCO is configured at a minimum noise state. The integrated phase noise is 2.522 ps while consuming 5 mW. A die photograph of the layout is

TABLE I
PERFORMANCE SUMMARY OF THE PROPOSED DESIGN AND COMPARISON TO PRIOR ARTS OF INDUCTORLESS DESIGNS

	This work	[35]	[36]	[37]	[38]	[1]	[39]		[16]
Output Frequency (GHz)	0.8-3.2	3.2	2.4	1.6	0.2-3.8	0.2-3.2	0.8-1.8		2.4
Oscillator Type	Ring	Ring	Ring	Ring	Ring	Ring	Ring	MDLL	MDLL
Reference Frequency (MHz)	50	200	26	266	300	N/A	375	375	75
RMS Integrated Jitter (ps)	3 @ 1GHz 2.7 @ 1.6GHz 2.52 @ 2.4GHz	3.85	2.418	2.418	2.13*	3.1-14	3.2	0.4	0.7
Integration Range (MHz)	0.1-100	N/A	0.01-40	0.01-2	N/A*	0.01-100	0.01-100	0.01-100	0.01-40
Power Consumption (mW)	2.5 @ 1GHz 3.8 @ 1.6 GHz 5 @ 2.4 GHz	2.915	6.4	2.7	1.98	0.7-3.4	0.9	0.6	0.43
Noise Reconfiguration	DCO Noise & Pwr	N/A	N/A	N/A	PLL Loop Bandwidth	N/A	N/A	N/A	N/A
Figure of Merit (dB)	-225.1 ~ -226.5	-224	-221.6	-226.7	-230.5	-224.8 ~ -218.6	-228.59	-248.7	-246.7
Area (mm ²)	0.049	0.0216	0.013	0.019	0.026	0.017	0.2	0.2	0.024
Technology	28nm SOI	40nm	40nm	65nm	65nm	22nm	130nm	130nm	28nm

* Measured as time-interval error

displayed in Fig. 27. Table I compares the performance of the proposed PLL with previous works using ring oscillators. The proposed work provides a wide output frequency range of 0.8–3.2 GHz. Also this paper shows less than 3-ps integrated jitter while using a cost effective 50-MHz reference. Overall, the proposed PLL shows competitive performance compared with the previous works while providing power and noise reconfigurability and noise self-adjustment capability.

VI. CONCLUSION

In this paper, a digital PLL using a nested FLL as a DCO is introduced. The proposed DCO provides accurate gain insensitive to the environmental changes as its period is locked to an $R-C$ constant. Also, phase noise of the DCO can be controlled using a bias current so it can be adaptively tuned according to the noise specification. Further, a noise detection and self-adjustment scheme are proposed to maintain constant noise performance under the environmental changes. The proposed work showed wide noise reconfigurability from 2.5 to 15 ps while controlling its power consumption from 1.5 to 5 mW.

APPENDIX A DETAILED PHASE NOISE DERIVATION

Equations (30)–(33) are calculated as follows:

$$L_{C_{sw}}(f) = A_{noise}^2 \overline{\frac{i_{1,out}^2}{I_{bias}^2} \frac{f_{out}^2}{f^2}} = A_{noise}^2 \alpha^2 \frac{4kT}{I_{bias} V_{sw}} \frac{f_{out}^2}{f^2} \quad (A1)$$

$$\begin{aligned} L_{M_1}(f) &= A_{noise}^2 \overline{\frac{i_{2,out}^2}{I_{bias}^2} \frac{f_{out}^2}{f^2}} \\ &= A_{noise}^2 (1-\alpha)^2 \frac{4kT \gamma_n g_{m1}}{I_{bias}^2} \frac{f_{out}^2}{f^2} = \left(\frac{1-\alpha}{\alpha}\right)^2 \times \frac{4kT \gamma_n g_{m1}}{I_{bias}^2} \frac{f_{out}^2}{f^2} \end{aligned} \quad (A2)$$

$$\begin{aligned} L_{R_0}(f) &= A_{noise}^2 \overline{\frac{i_{3,out}^2}{I_{bias}^2} \frac{f_{out}^2}{f^2}} \\ &= A_{noise}^2 \beta^2 \frac{4kT}{I_{bias}^2 R} \frac{f_{out}^2}{f^2} = \frac{\beta^2}{\alpha^2} \frac{4kT}{I_{bias} V_R} \frac{f_{out}^2}{f^2} \end{aligned} \quad (A3)$$

$$\begin{aligned} L_{M_2}(f) &= A_{noise}^2 \overline{\frac{i_{4,out}^2}{I_{bias}^2} \frac{f_{out}^2}{f^2}} \\ &= A_{noise}^2 (1-\beta)^2 \frac{4kT \gamma_p g_{m1}}{I_{bias}^2} \frac{f_{out}^2}{f^2} = \left(\frac{1-\beta}{\alpha}\right)^2 \times \frac{4kT \gamma_p g_{m1}}{I_{bias}^2} \frac{f_{out}^2}{f^2}. \end{aligned} \quad (A4)$$

Then, noise generated from the represented in terms of voltage ratios as follows:

$$L_{M_1}(f) = \frac{mv_T}{V_{sw}^2} \frac{4kT \gamma_n}{I_{bias}} \frac{f_{out}^2}{f^2} \quad (A5)$$

$$L_{M_2}(f) = A_{noise}^2 \frac{mv_T}{(V_R + mv_T)^2} \frac{4kT \gamma_p}{I_{bias}} \frac{f_{out}^2}{f^2}. \quad (A6)$$

The overall noise can be found by making summation of (A1), (A3), (A5), and (A6) which is shown in (32).

APPENDIX B PHASE NOISE CALCULATION WHEN TRANSISTORS ARE OPERATING AT A SATURATION REGION

In Section III, phase noise analysis of the proposed DCO is presented when the transistors, M_1 and M_2 in Fig. 1 are biased at a subthreshold region to maximize their transconductance. Sometimes, it is not possible to increase the gate size large enough to bias them at a subthreshold region due to area or gate leakage. In this appendix, phase noise of the proposed DCO with devices in a saturation region is discussed.

The current division ratio α (24) can be rewritten by the following equation when M_1 is biased at a saturation region:

$$\begin{aligned}\alpha &= \frac{\frac{V_{sw}}{I_{bias}}}{\frac{V_{sw}}{I_{bias}} + \frac{V_{gs,m1} - V_{thn}}{2I_{bias}}} = \frac{2V_{sw}}{2V_{sw} + V_{gs,m1} - V_{thn}} \\ &= \frac{2V_{sw}}{2V_{sw} + V_{ov,m1}}\end{aligned}\quad (\text{B1})$$

where V_{gs} and V_{ov} are the gate-to-source voltage and the overdrive voltage, respectively. Similarly, the current division ratio at the source of M_2 , β , is

$$\beta = \frac{2V_R}{2V_R + V_{ov,m2}}. \quad (\text{B2})$$

By replacing α and β in (31) and (33) to (A1) and (A2), the phase noise contributions from M_1 and M_2 can be found as

$$\begin{aligned}L_{M_1,\text{Sat}}(f) &= \left(\frac{V_{ov,m1}}{2V_{sw}}\right)^2 \frac{8kT\gamma_n}{I_{bias}V_{ov,m1}} \frac{f_{out}^2}{f^2} \\ &= \frac{V_{ov,m1}}{V_{sw}^2} \frac{2kT\gamma_n}{I_{bias}} \frac{f_{out}^2}{f^2}\end{aligned}\quad (\text{B3})$$

$$\begin{aligned}L_{M_2,\text{Sat}}(f) &= A_{\text{noise}}^2 \left(\frac{V_{ov,m2}}{2V_R + V_{ov,m2}}\right)^2 \frac{8kT\gamma_p}{I_{bias}V_{ov,m2}} \frac{f_{out}^2}{f^2} \\ &= A_{\text{noise}}^2 \frac{V_{ov,m2}}{(2V_R + V_{ov,m2})^2} \frac{8kT\gamma_p}{I_{bias}} \frac{f_{out}^2}{f^2}.\end{aligned}\quad (\text{B4})$$

Finally, the overall phase noise of the proposed FLL can be described as the following equation when M_1 and M_2 are in a saturation region:

$$\begin{aligned}L_{\text{Sat}}(f) &= \frac{4kT}{I_{bias}} \left(\frac{1}{V_{sw}} \left(1 + \frac{\gamma_n V_{ov,m1}}{2V_{sw}}\right) \right. \\ &\quad \left. + A_{\text{noise}}^2 \left(\frac{4V_R + 2\gamma_p V_{ov,m2}}{(2V_R + V_{ov,m2})^2} \right) \right) \frac{f_{out}^2}{f^2}.\end{aligned}\quad (\text{B5})$$

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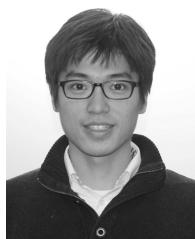
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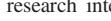
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