

A 61-GHz SiGe Transceiver Frontend for Energy and Data Transmission of Passive RFID Single-Chip Tags With Integrated Antennas

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Abstract—This paper presents SiGe-based transmitter and receiver chips for a radio frequency identification (RFID) frontend in the 61-GHz industrial, scientific, and medical (ISM) frequency band. The chips are fabricated in a modern 130-nm SiGe BiCMOS technology with HBTs offering an f_T of 250 GHz and f_{max} of 370 GHz. The presented transmitter consists of a fundamental voltage-controlled oscillator (VCO), a power amplifier (PA), lumped element Wilkinson power dividers, and a static divide-by-16 chain for stabilization within a phase-locked loop (PLL). Two variants of the transmitter are fabricated with supply voltages of 3.3 and 5 V, respectively. The transmitters are designed to provide an efficient signal source to supply a passive RFID tag with the maximum allowed 20-dBm effective isotropic radiated power (EIRP) for short-range devices. The 3.3-V transmitter chip achieves a peak output power of 17 dBm, PAE_{PA} of 18.6% and dc-to-RF efficiency of 12.9% (excluding the divider). At 61 GHz, a phase noise of -102 dBc/Hz at 1 MHz offset is achieved. The power consumption for the 5- and 3.3-V transmitter chips is 710 and 482 mW, respectively. The receiver chip is implemented as two Gilbert cell mixers in phase quadrature configuration to compensate for destructive interference that may be caused by varying distance between reader and tag.

Index Terms—Millimeter-wave (mm-wave) VCOs, MMICs, power amplifier (PA), radio frequency identification (RFID), SiGe bipolar integrated circuits, ultra-wideband.

I. INTRODUCTION

RECENT advances in silicon technologies and especially in silicon-germanium (SiGe) technologies enable the operation at higher frequencies reaching the upper end of the millimeter-wave (mm-wave) region [1]. While these advances can either be used for higher frequencies, they can also be used

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to achieve a better efficiency and performance at frequencies, where robust operation has already been proven. Here, it is used for the second reason in order to implement a radio frequency identification (RFID) system using the 61-GHz industrial, scientific, and medical (ISM) radio band with passive single-chip tags beside the key driving technologies 5G and Internet of things (IoT). Several transmitter and receiver frontends for communication systems for this ISM band have already been published in [2]–[4]. Transmitters using other frequencies at 94 GHz [5] have also been reported. Recent publications target higher frequencies such as 320 GHz [6] or multiple frequencies such as 61 and 122 GHz [7]. Also, very efficient single components [power amplifiers (PAs), see [8]] have been demonstrated.

Prior work in the field of mm-wave RFID as well as single-chip RFID tags with on-chip antennas has been published in several papers. Functional circuitry (without antenna) of a passive RFID tag operating in the 60-GHz band was shown in [9]. First research works on on-chip antennas for single-chip RFID tags at these frequencies have been presented in [10]. Successful operation of a passive printed circuit board (PCB)-based RFID tag working at 10 GHz was shown in [11]. A fully functional single-chip tag with an on-chip antenna was presented in [12], achieving a range of 50 cm by making use of two frequencies: 24 GHz for the reader-to-tag (R2T) communication as well as power supply and 60 GHz for the tag-to-reader communication. A similar approach was used in [13], where an external 2.45-GHz loop antenna was used for energy harvesting, while on-chip 60-GHz antennas were used for communication. To increase the data rate between reader and tag, the use of a self-oscillating mixer within the tag was proposed in [14]. In [15], it is concluded that the 60-GHz band presents several advantages over the 3.1–10.6-GHz ultra-wideband band for RFID applications.

The main source of this paper lies within the demand to counter plagiarism and falsification. The high economical and reputational damage it is doing to the society results in calling for modern ways to identify and authenticate, e.g., automotive spare parts, legal drugs, banknotes, and luxury goods. The authentication process is intended to be implemented by means of cryptography, which is implemented

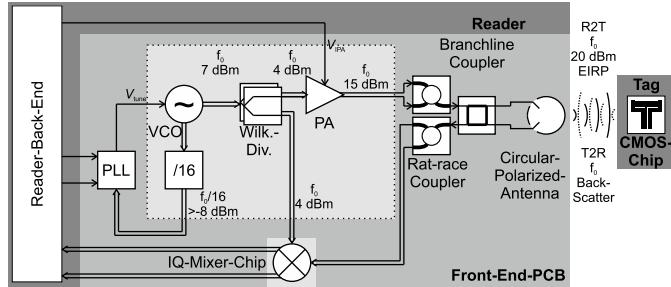


Fig. 1. Block diagram of the proposed RFID system with intended frequency and level plan. Differential signals are shown by double lines.

into the reader and the tag. The extra energy consumption caused by the cryptographic circuit blocks demands for more power to be transferred to the tag compared to the presented prior work. To realize this vision, the passive RFID tag with integrated antenna should be fabricated in a modern mass market silicon standard complementary metal-oxide-semiconductor (CMOS) technology to retain the tag costs as low as possible. The reader can then be used to prove the origin of items through these RFID tags. The reduced unit quantity and higher performance demand [e.g., 20-dBm effective isotropic radiated power (EIRP)] render a modern SiGe Bipolar and CMOS (BiCMOS) technology, which is an appropriate choice for the frontend in this frequency region.

A block diagram highlighting all parts and an intended level and frequency plan of the RFID system is shown in Fig. 1. This paper addresses the design of the frontend transmitter [16] and receiver of the RFID reader. The transmitter will be used to supply the passive tag with power for operation and also for the R2T communication. The tag communicates toward the reader (tag-to-reader, T2R) by modulating its reflection coefficient (backscatter modulation). The purpose of the receiver is to down convert the signal received from the tag. As the CMOS tag is still work in progress, the T2R communication was tested by a dummy tag, which was especially designed for this purpose. The remainder of this paper is organized as follows. In Section II, the considered system concept and circuit design of the transmitter and receiver chips are discussed. Section III will provide the experimental results and conclusions are drawn in Section IV.

II. CIRCUIT DESIGN

In Fig. 1, the block diagram of the transmitter chips is shown. For the stabilization phase-locked loop (PLL) of the integrated fundamental voltage-controlled oscillator (VCO), the mm-wave part of a frequency divider chain is integrated on the same chip (see Fig. 1). The VCO is directly driving a lumped element Wilkinson power divider, which splits the VCO signal into a local oscillator (LO) signal for the external mixer and also for the input signal of the integrated PA. The external mixer will be used to detect the backscattered signal of the passive tag for the T2R communication. The implementation of the mixer is quite interesting and very challenging, due to the possible total reflection at the antenna output, which will drive most mixers into deep saturation,

TABLE I
COMPONENT DESIGN VALUES FOR THE 61-GHz VCO.
DRAWN DIMENSIONS ARE GIVEN

Component	Design value	Additional note
L_1	35 μm	41 Ω
L_2	460 μm	61 Ω
L_3	60 μm	41 Ω
L_4	170 μm	61 Ω
L_5	260 μm	61 Ω
L_B	115 μm	33 Ω
T_1	$2 \times 0.22 \mu\text{m} \times 10 \mu\text{m}$	CBEBC
T_2	$3 \times 0.22 \mu\text{m} \times 10 \mu\text{m}$	CBEBC
C_1	50 fF	-
C_2	500 fF	-
$C_{var}/C^*\text{ var}$	$10 \times 1 \mu\text{m} \times 16 \mu\text{m}$	-
I_0	28.7 mA	-

especially mixers integrated in silicon technologies. The mixer was fabricated in the same technology as the transmitter chip.

The PA is designed with an additional external pin which is used to modulate the core current of the amplifier. This resulting amplitude modulation is used for the R2T communication in the whole planned RFID system concept. The VCO core current can also be adjusted in the same manner. The transmitter circuits were designed for a supply voltage of 3.3 and 5 V to better gauge and compare the performance-efficiency tradeoff for the transmitter chip.

The chips have been designed in Infineon's high-speed B11HFC 130-nm SiGe:C BiCMOS technology featuring heterojunction bipolar transistors ($f_T = 250$ GHz and $f_{max} = 370$ GHz), dedicated RF-MIM capacitors and RF-TaN resistors, a metal stack of six copper layers and a top aluminum layer. The technology is qualified for automotive purposes, and hence, is suitable for mass market applications due to the production grade stability. A further insight into the technology and a comparison to the preceding B7HF200 technology can be found in [1] and [17]. All circuits are arranged in a fully differential way for its several benefits and most inductive elements, except for the lumped element Wilkinson power divider and the bond-pad compensation networks, are realized through short transmission lines ($l < \lambda/4$).

The spiral inductors for the bond-pad compensation networks and the Wilkinson divider as well as the degeneration and interstage matching inductors within the mixer are simulated with Sonnet, a 2.5-D electromagnetic (EM) Simulator, and are optimized within a time-consuming iterative process. Furthermore, the Wilkinson divider is completely EM simulated in Sonnet with the dedicated RF-MIM capacitors, RF-TaN resistor, and the spiral inductor. This is done to account for all parasitic capacitance and wiring inductance introduced to the lumped elements by the layout and area consumption of the passive structures. Through this, the Wilkinson divider can be realized quite compact with an area consumption of only $90 \times 150 \mu\text{m}^2$ including a $10-\mu\text{m}$ guard ring.

A. 61-GHz Fundamental Wideband VCO

The integrated fundamental VCO is based on the 80-GHz VCO architecture proposed in [18]. It is based on the Colpitts topology which is commonly used for mm-wave

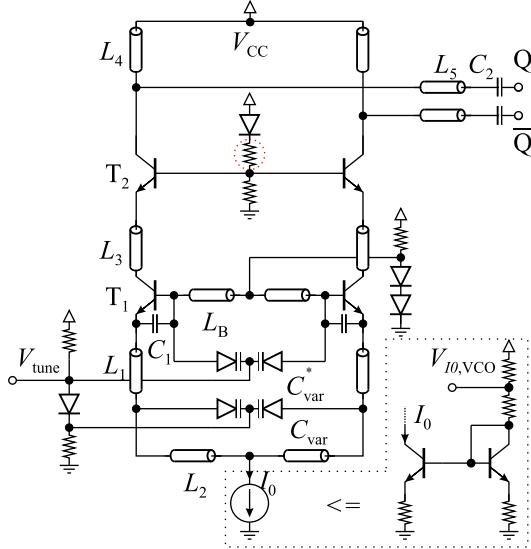


Fig. 2. Schematic of the used 61-GHz VCO. Dotted circle: differences to the 5-V version. Here, it is an omitted resistor in the cascade-stage biasing.

integrated SiGe VCOs. The most important design values of the VCO components are given in Table I. The main difference compared to the original differential Colpitts lies within the second tunable varactor called C_{var}^* at the base node of the oscillating transistor pair T_1 . Due to the use of the three capacitors C_1 , C_{var} , and C_{var}^* and the inductance L_B for the resonant tank, the architecture is best described as a merged Colpitts-Clapp topology. The main goal of this second varactor is a wider tuning range (TR) for the VCO. In [18], an increase in TR by 45% compared to the Colpitts-only topology was shown. In addition, a current reusing base stage with the transistor pair T_2 is used to decouple the core of the VCO from the output. Here, however, no additional current is injected into the emitter of the base stage for linearization as done in [18]. The VCO is followed by a dedicated PA for delivering high output power, and therefore, the extra current for the base stage is not needed in the VCO. By simply omitting this additional current, the TR is also further increased. This was shown with an increase from 24.3 GHz (30%) [18] to 25.6 GHz (32%) [19] in TR on the exact same VCO.

With two simulations of the complete 3.3-V transmitter chip, the advantage of the Colpitts-Clapp over the original Colpitts topology is shown. The topology and the component design values from Fig. 2 and Table I apply for both simulations. Instead of using two varactors (C_{var} and C_{var}^*) at the base and emitter nodes of the transistor pair T_1 for the Colpitts-Clapp case, the two varactors are used in parallel $2 \times C_{\text{var}}$ for the Colpitts VCO to achieve the same total varactor area and, therefore, the same variable capacitance to constant inductance proportion in both the cases. In Fig. 3, the tuning curves of these simulations are shown. When the center frequency f_C is shifted to lower frequencies by 7.85 GHz due to C_{var}^* , the absolute frequency tuning range (FTR) is increased by 4 GHz even though it is operating at lower frequencies. This results in a rather large profit of more than 10% in relative TR for the Colpitts-Clapp topology compared to the simulated

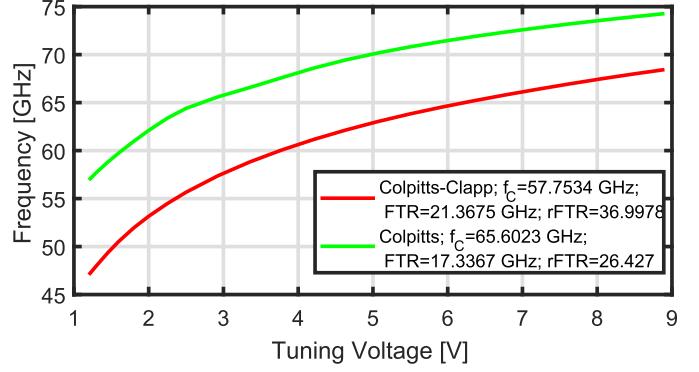


Fig. 3. Simulated oscillation frequency versus tuning voltage of the 3.3-V VCO in Colpitts-Clapp versus Colpitts topology. Component design values for both simulated topologies are the same and both topologies are using the identical total varactor area.

Colpitts case. The lowest simulated phase noise at an offset frequency of 1 MHz for the Colpitts-Clapp topology is about -103 dBc/Hz around the center frequency and also at 61 GHz. The Colpitts topology, on the other hand, only shows a phase noise minimum of -97 dBc/Hz.

The VCO circuit remains the same for both supply voltage versions. The main differences of the circuits lie within the transistor biasing networks. The voltage drop for the dedicated transistor current source providing the core current I_0 is kept the same. The voltage at the base node of the oscillating transistor pair T_1 also stays the same for both versions. The compromises for the smaller voltage headroom of 3.3 V were realized with a decreased V_{CB} voltage for the oscillating transistor pair T_1 and the base stage transistor pair T_2 . This was achieved by removing the resistor in the dotted circle of Fig. 2. This drop of 1.7 V was mainly absorbed by $V_{CB,1}$, which was reduced by 1.55 V, while $V_{CB,2}$ was only reduced by the remaining 0.15 V.

The core current and the biasing currents of all networks were the same for both versions, which resulted in a current consumption of 41 mA for the VCO. The core consumes a current of 28.7 mA while the biasing circuitry consumes the rest. The relatively high biasing current of more than 12 mA is used to realize low ohmic terminals especially at the base nodes of transistor pair T_1 and in the reference current of the current mirror for the core current. This is done to reduce the injected noise into the oscillating tank for good noise performance.

To achieve a good temperature stability, much effort was invested in the design of the biasing circuitry of the VCO. For temperature stable tuning characteristics, the core current I_0 is very important and should be as constant over temperature as possible. An increasing core current would otherwise degrade the TR of the VCO, as already stated before, for the additional base current. Here, a dedicated current mirror with resistive degeneration is used instead of a simple current mirror to decrease the proportional to absolute temperature (PTAT) behavior of I_0 . Simulations have shown that the PTAT behavior can be reduced to a factor of approximately 0.7 at the cost of a slightly higher voltage drop compared to the simple

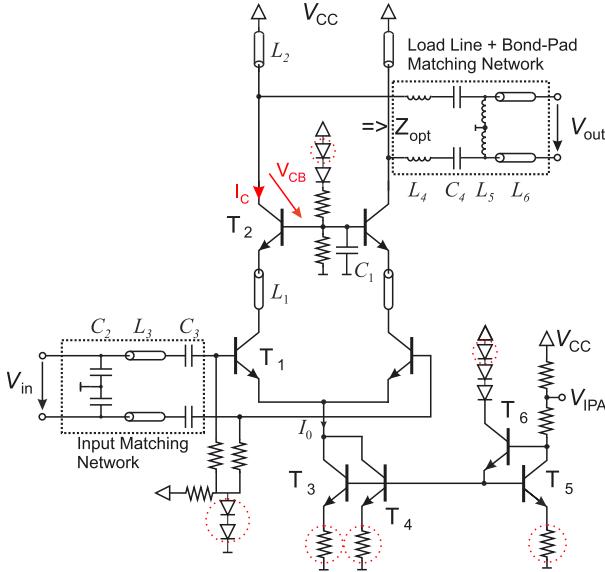


Fig. 4. Schematic of the designed 61-GHz PA. Dotted circles: differences between the 3.3-and the 5-V version.

current mirror. As a second measure, the current densities in all used transistors and diodes, which are realized by using the HBTs, are the same in their corresponding counterpart. This assures the same temperature-dependent V_{BE} voltage drop at all nodes. Even with these measures, a temperature-dependent impact was still expected due to the change of $V_{CB,1}$ with temperature, especially on the output power. This could be compensated by a stronger PTAT behavior of I_0 , but for the sake of TR this was intentionally not pursued here.

An additional external pin is added in the VCO to vary the reference current for I_0 . This can be used to optimize the tradeoff between current consumption, output power, and noise performance of the VCO. Furthermore, here it is only used to indirectly characterize the on-chip wideband PA by variation of the VCO output power and, hence, the input power to the PA.

B. 61-GHz Wideband PA

In Fig. 4, the schematic of the PA is shown. This design is taken from [20] and was scaled to the intended frequency range and redeveloped for the new technology. Design component values are given in Table II. The PA consists of a common emitter stage T_1 with a dedicated transistor current source formed by $T_3 - T_6$, followed by a cascode stage T_2 which is connected to an inductive load L_2 . An additional capacitor C_1 of 400 fF at the virtual ground of the base stage is used for ac grounding. In the layout, this capacitance is as close as possible to the base nodes of transistor pair T_2 . The input matching network, which is realized by MIM capacitors and short transmission lines, is designed for wideband operation to exploit the full TR of the VCO. The output is connected to a load-line and bond-pad matching network, where in comparison to the input network additional spiral inductors are used. A simple current mirror is used as a current source

TABLE II
COMPONENT DESIGN VALUES FOR THE 61-GHz PA. DRAWN DIMENSIONS ARE GIVEN AND DIFFERENCES FOR THE 3.3-V VERSION ARE GIVEN IN RED

Component	Design value	Additional note
L_1	60 μm	50 Ω
L_2	270 μm	61 Ω
L_3	230 μm	61 Ω
L_4	150 pH	-
L_5	350 pH	Differential
L_6	350 μm	61 Ω
T_1	$3 \times 0.22 \mu\text{m} \times 10 \mu\text{m}$	CBEBC
T_2	$3 \times 0.22 \mu\text{m} \times 10 \mu\text{m}$	CBEBC
C_1	400 fF	-
C_2	125 fF	-
C_3	125 fF	-
C_4	35 fF	-
I_0	54 mA / 60 mA	-

to bias the PA in Class-A with a quiescent current of I_0 for the differential transistor pairs $T_{1,2}$.

Large HBTs with the maximum number of base fingers were used for the core transistor pairs $T_{1,2}$ of the PA to keep the parasitic base wiring inductance and resistance as low as possible. This is of exceptional importance for the cascode stage which, due to its differential architecture, has a low-impedance virtual ground connection at the base nodes for differential high-frequency signals. Hence, the collector-base breakdown voltage BV_{CES} can be exploited for these transistors. Every increase in parasitic impedance would lead to a higher load impedance and a resulting lower breakdown voltage. In the worst case, the usable voltage at the output would be reduced to the open base breakdown voltage BV_{CEO} , which in this technology is typically smaller by a factor of 3.5 ($BV_{CES} = 5.3$ V versus $BV_{CEO} = 1.5$ V).

Another important performance factor is the high current limit, which degrades the transistor's cutoff frequencies at higher current densities. The high current limit restricts the maximum possible current amplitude, while the avalanche breakdown limit restricts the maximum possible differential voltage amplitude. In order to achieve maximum output power, it is necessary to reach maximum voltage and current amplitude at the same time. This is accomplished by the load-line matching and bond-pad compensation network at the output of the PA. This network transforms the differential 100- Ω load parallel to the inductive load L_2 into the optimum load impedance Z_{opt} of the PA. The design of this network is very critical as it should be low loss to enhance the efficiency and the usability over a wide frequency range.

From load-pull simulations, the optimum load impedance $Z_{opt} = (72.84 + j53.12)$ Ω for the PA at 61 GHz with an output power of 20.2 dBm is obtained on the Smith chart. The simulated power contours with 1-dB offset are shown in Fig. 5. The input impedance Z_{in} of the output matching network with the given design component values of Table II and an assumed bond wire length of 250 μm is $Z_{in} = (80.7 + j5.6)$ Ω . This Z_{in} lies close to the 1-dB power contour from the load-pull simulations in Fig. 5. The simulated

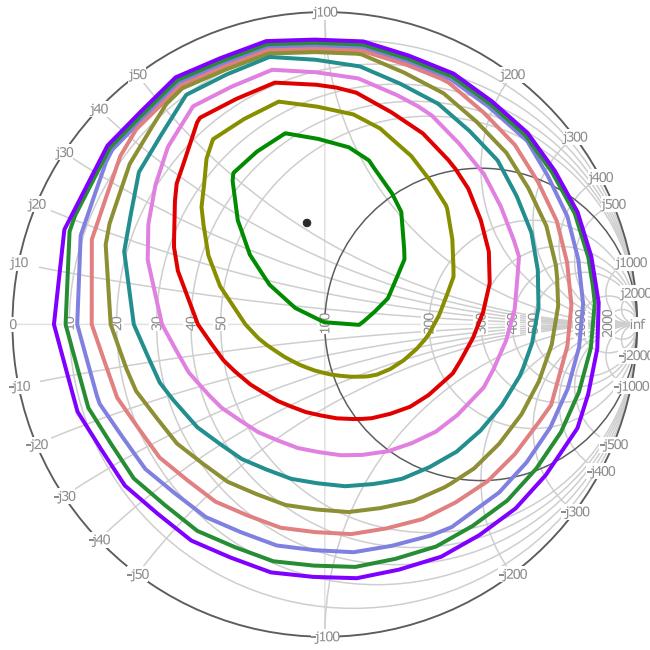


Fig. 5. 1-dB Power contours of the PA from load-pull simulations at 61 GHz. The reference impedance is 100Ω due to differential operation. Black dot: optimum load impedance $Z_{\text{opt}} = (72.84 + j53.12) \Omega$ with a maximum output power of 20.2 dBm.

loss of the passive network is 1.5 dB at 61 GHz and the 3-dB bandwidth is well within 40 to 80 GHz.

The considerations for the output network also apply for the VCO output. But as the VCO is only intended to produce a moderate output power and is directly driving an on-chip Wilkinson divider, the situation is more relaxed and no special and complex network was required. The last statement is also apparent in the differences between the two supply versions. More devices in the biasing networks had to be omitted to realize the same performance for both voltage versions. These changes are depicted in red dotted circles in Fig. 4. Although this reduces the temperature stability of the PA, the degeneration resistors in the current source of the PA had to be removed. This tradeoff between the performance and temperature stability was accepted as the temperature stability in the PA is not that important for a temperature stable TR. In addition, the core current had to be increased by 6 mA. This results in a current consumption for the PA with biasing of 71 and 77 mA for the 5- and 3.3-V variant, respectively. In addition, the two diodes for the biasing of T_1 were exchanged for a simple resistor also neglecting the impact on temperature stability. The amplitude modulation is obtained by variation of the reference current at the pin V_{IPA} and also this pin is used to further optimize the current consumption and, hence, the efficiency and saturated output power P_{sat} of the PA in measurements after fabrication.

C. 61-GHz Static Divide-By-16 Chain

The block diagram of the divide-by-16 stage is shown in Fig. 6. It consists of four cascaded static divide-by-two cells and is followed by a buffer which provides more than -8 dBm of output power to drive the external off-the-shelf

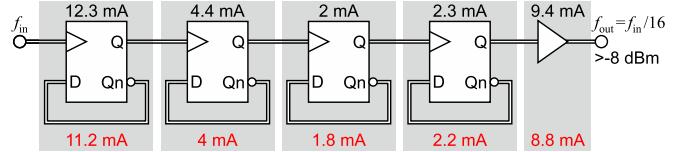


Fig. 6. Block diagram of the divide-by-16 chain with dedicated buffer and annotated current consumption. The current consumption for the 3.3-V version is given in red.

PLL chips. The divider chain including the buffer consumes 30 and 28 mA for the 5- and 3.3-V variant, respectively. The current consumption of each stage is given in black for the 5 V and in red for the 3.3-V version. The drastic reduction in current consumption for each following stage can be clearly seen. The divide-by-16 output can also be used for easier measurements and verification. The comparison between the current mode logic -static divider and emitter-coupled logic (ECL)-static divider for low-power and high-speed designs in [21] heavily influenced the chosen architecture for the realized divider chain.

The schematic of the first stage and, due to the highest frequency, most critical stage is illustrated in Fig. 7. It can be divided into four parts, the input stage, the two latches, and the output stage. As the input of the divider chain is directly connected to the collectors of the cascode stage T_2 in the VCO (see Fig. 2), which is connected to the supply voltage, an input stage is needed for dc decoupling and biasing of the first stage. The following stages, the three divide-by-2 and the buffer stage, are directly connected to the preceding stage without the need for additional dc decoupling. The extra high ohmic resistor $R_1 = 50 \text{ k}\Omega$ at the positive input of the input stage keeps the divider stage from self-oscillation, when no or only a small input signal is supplied to the divider.

All transistors in the first stage have an emitter length of $1.3 \mu\text{m}$. The input transistors $T_{1,2}$ of the latches are dc biased for maximum f_T of the technology and the upper transistors of the latch T_{3-6} are hence operated at half the optimum current density. The differential emitter follower at the output of the divide-by-2 stage is operated only slightly below the optimum current density. For the second and third stages, the current densities drop to half and $1/5$ the optimum current density for transistors $T_{1,2}$ with emitter stripes of $1 \mu\text{m}$ length. The latches of the fourth stage are the same as of the third. A further drop in the used current below $1/10$ of the optimum current density was intentionally prevented. This was conservatively done as to not risk leaving the limits of the used bipolar models. The use of slower HBT's or even the available MOS transistors to further reduce the current consumption should be investigated in the future.

The higher total current consumption in the fourth stage is exclusively used in the emitter follower of the output stage which drives the buffer for the external PLL circuitry. The design of the output buffer consists of one differential emitter follower directly connected to the emitter follower of the fourth divide-by-2 stage. A subsequent differential amplifier is used to drive a differential $100-\Omega$ load with more than -8 dBm.

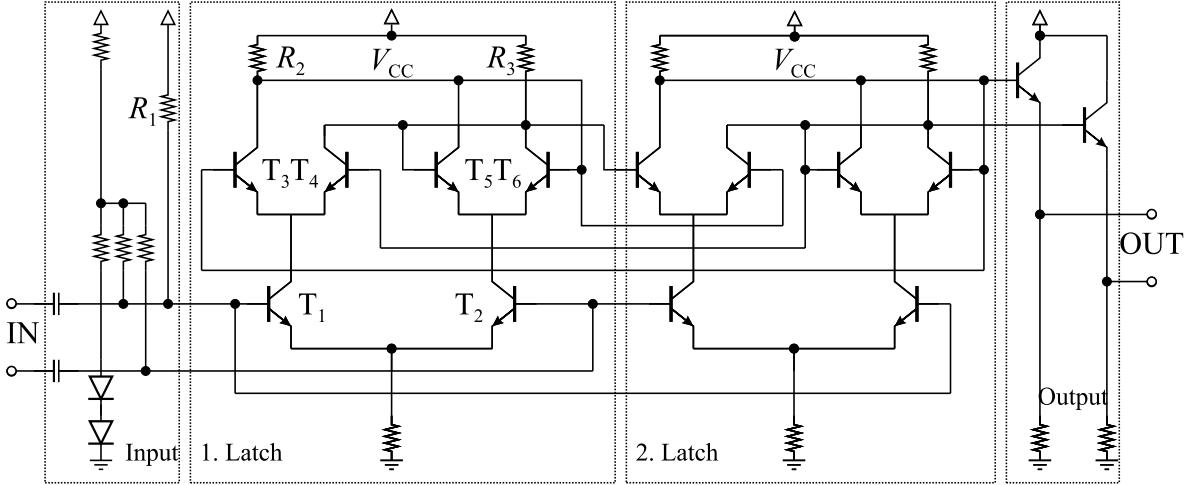


Fig. 7. Schematic of the first divide-by-2 stage with two latches, an input and output stage operating at 61 GHz.

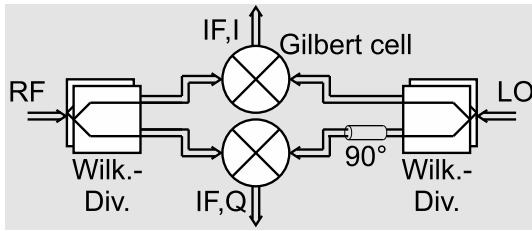


Fig. 8. Block diagram of the quadrature receive mixer chip. Double lines: differential signals.

D. 61-GHz Receive Mixer

The design of the receive mixer has to face some challenges resulting from the system concept. One issue is that there will be LO crosstalk (CT) into the receive path. This CT is expected to have much higher power than the receive signal. This can cause intermodulations in the desired baseband signal. Besides this, there is another issue. Simulations of the system's signal flow showed that the amplitude of the mixer output is proportional to the phase shift between the LO signal and the signal received from the tag. Because the phase of the received signal varies with distance, the phase difference to the LO also changes during the system operation, which results in an altering amplitude of the down-converted signal.

To overcome this problem, a mixer with a quadrature architecture is chosen. This ensures a successful demodulation of the received signal for an arbitrary phase shift. In addition, the quadrature architecture also improves the linearity, because the power of the CT is spread over two separate mixer cells.

In Fig. 8, the block diagram of the receive mixer is shown. It consists of two identical mixer cells, which are each driven by two 61-GHz LO signal with a phase shift of 90°. To realize the two LO signals for both mixer cells, two Wilkinson dividers are used. These dividers are identical to the dividers that distribute the VCO signal on the transmitter-monolithic microwave integrated circuit (MMIC). The phase shift for the quadrature mixer cell is achieved by using a transmission line with an electrical length of $\lambda/4$ as a delay. At a frequency

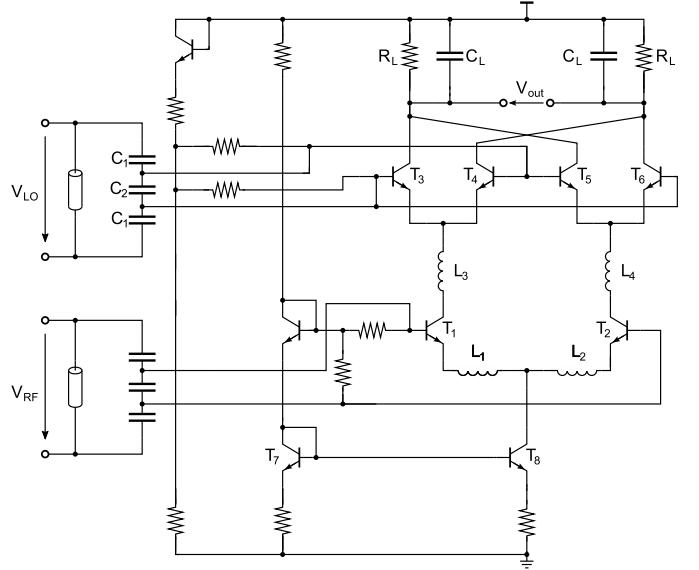


Fig. 9. Schematic of the Gilbert cell.

of 61 GHz, the transmission line is a good option due to its physical length and due to the fact that it can be trimmed using fuses.

For a single mixer cell, a Gilbert topology is used. To design a Gilbert cell that is still in linear operation for a high input power, some modifications compared to the standard Gilbert cell are done (see Fig. 9). The main adjustment is realized using an inductive degeneration of the g_m stage ($T_{1,2}$). This increases the linearity of the cell [22]. But the benefit in linearity stays in conflict with a loss of conversion gain. To overcome this loss, another inductor pair $L_{3,4}$ is used to improve the interstage matching between the g_m -stage and the switching quad (T_{3-6}). This additional effort results in an increased conversion gain that compensates the gain reduction, caused by the degeneration [23]. The inductors were designed and optimized with Sonnet to get accurate simulation models.

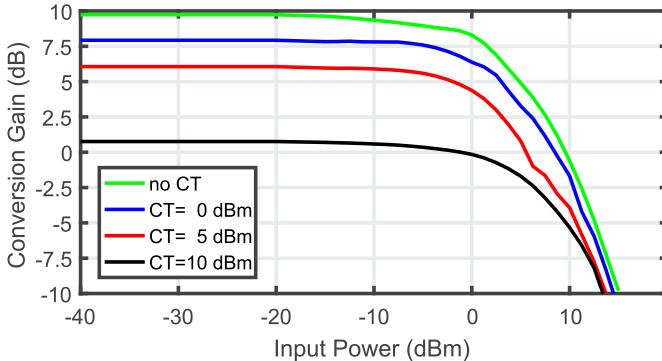


Fig. 10. Simulation of the mixer's conversion gain versus input power for different cross talks at an LO level of 3 dBm.

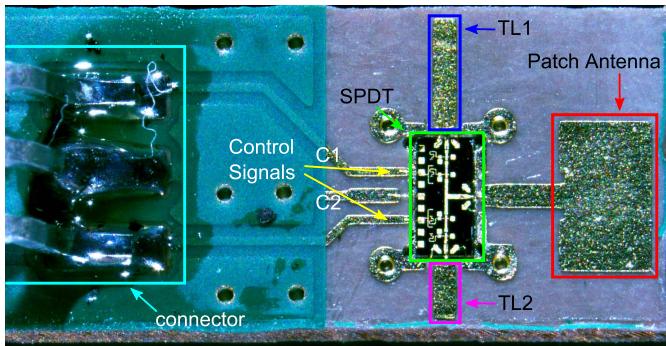


Fig. 11. Microphotograph of the dummy tag PCB used to verify the receive path of the RFID reader frontend. The PCB dimensions are 14.9 mm by 5.5 mm.

They were taken into account during the design process of the Gilbert cell, to simulate the circuit as realistic as possible.

Due to the degeneration inductors, an input referred 1-dB compression point of 2 dBm can be achieved. For a sufficient signal-to-noise ratio, the noise figure was designed to a minimum of 12 dB. The circuit's conversion gain versus input power is plotted in Fig. 10. To consider the finite isolation between transmit and receive path, the conversion gain was simulated for different CT powers that superimpose the desired input signal. Depending on the CT, the conversion gain ranges from 9.5 to 0.75 dB for moderate input powers up to -15 dBm. It can be seen that the CT power impairs the mixer's performance. To avoid mismatch at the mixer's input ports, a combination of capacitors and transmission lines is used to ensure a low reflection coefficient. The mixer is loaded with an RC low-pass filter. For a stable bias point, a current mirror is used as a current source. It is degenerated resistively to improve temperature stability. The mixer MMIC consumes 12 mA at a supply voltage of 5 V.

E. Test Dummy Tag

Since the CMOS RFID tag is not yet available, a test dummy tag was developed in order to verify the tag-to-reader communication. Its purpose is to replicate the ability of an RFID tag to change its reflection coefficient. The dummy tag was realized as a PCB with a patch antenna and a GaAs-based single pole double throw (SPDT) MMIC

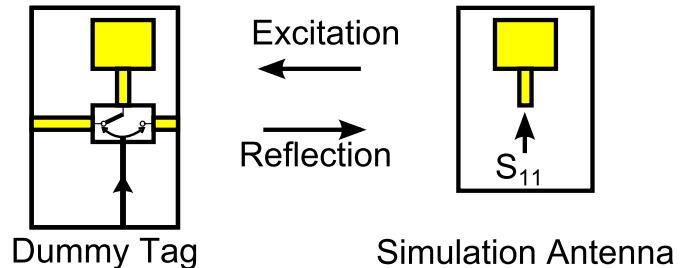


Fig. 12. Setup used to simulate the reflection of the dummy tag.

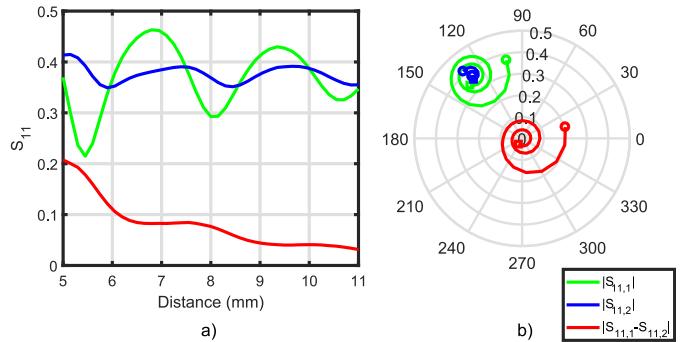


Fig. 13. Simulated $S_{11,1}$ and $S_{11,2}$ and their difference at 61 GHz according to the setup depicted in Fig. 12 depending on the distance between the simulation antenna and dummy tag in linear (a) and polar (b) representations. In the polar plot, the circle indicates a distance of 5 mm and the square indicates 11 mm.

switch (HMC-SDD112). The dummy tag PCB is shown in Fig. 11. A patch antenna is connected via a 50Ω microstrip line to the input of the SPDT switch. The outputs of the switch are connected to transmission lines (TL) TL1 and TL2. Both lines are open ended. Thus, an incoming signal is reflected. TL1 is 0.9 mm longer than TL2 which is equivalent to $(\lambda/4)$ in the used Rogers 5880 substrate. Control signals C1 and C2 set the state of the switch. In one state, the switch connects TL1 to the patch antenna and in the other state TL2 is connected. A signal received by the antenna is thus reflected either at the open end of TL1 or TL2. The extra $(\lambda/4)$ length of TL1 causes a phase shift of 180° of the reflected signal which causes a change in the total radar cross section of the dummy tag. The RFID reader frontend can then be tested by placing the dummy tag in front of the reader antenna and modulating the dummy tag with a signal generator connected to the PCB. The generator's signal should then be measurable at the output of the mixer chip.

The reflection behavior of the dummy tag was simulated with a 3-D EM solver. Fig. 12 shows the setup used to simulate the reflection behavior of the dummy tag. The same patch antenna present in the dummy tag is used to stimulate the dummy tag and to receive the reflected signal. S_{11} is thus an indicator for the reflectance of the dummy tag. The switch was modeled by using a transmission line model that matched the S-parameters taken from the SPDT switch's datasheet at 61 GHz. The desired behavior is a large difference in reflection of the dummy tag for the two switch states $S_{11,1}$ and $S_{11,2}$. This simulation result is shown in Fig. 13

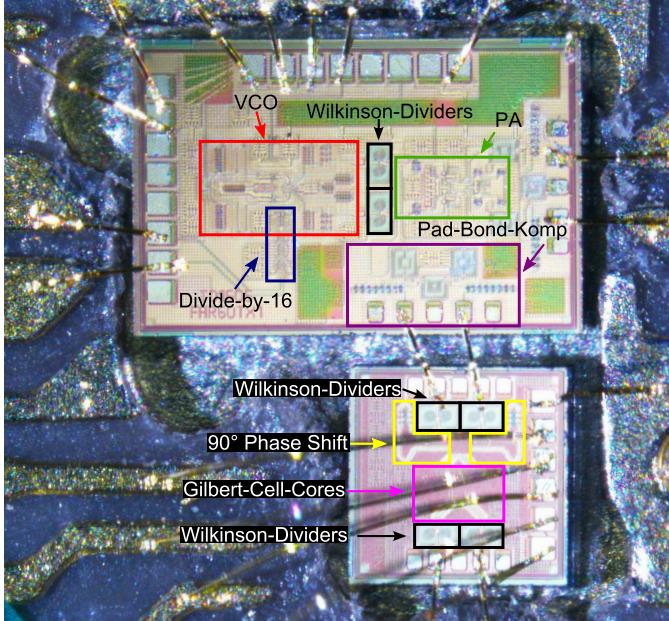


Fig. 14. Photograph of the cavity with the bonded 5-V transmitter chip (top) and the receive mixer chip (bottom). The overall needed area of the transmitter chips is $1448 \times 930 \mu\text{m}^2$, while the receive mixer chip is $672 \times 672 \mu\text{m}^2$.

depending on the distance between the dummy tag and the stimulating antenna.

III. EXPERIMENTAL RESULTS

On-wafer measurements of the transmitter chips are presented in Section III-A. Because the level of TX to RX CT could not be properly estimated, the functionality of the receiver has been verified by fabricating a complete RFID reader frontend and testing it by using the dummy tag. This measurement is described in Section III-B.

A. On-Wafer Measurement Results

Fig. 14 shows the photograph of the cavity of the frontend board with the bonded 5-V transmitter chip (3.3-V version not shown) and the receive mixer chip with the highlighted building blocks. The die area for both versions of the transmitter chip is $1448 \times 930 \mu\text{m}^2$ including the pads. The receive mixer chip consumes an area of $672 \times 672 \mu\text{m}^2$. The transmitter chips were fully characterized on-wafer with RF probes at the divider (lower left side in GSSG configuration), the external LO (bottom edge with GSGSG), and PA output (right side, also GSGSG). The supply and control voltages for V_{tune} as well as the core current of the VCO and PA were contacted via the upper pad row with a multi-contact probe.

As a first result, the frequency response of the Wilkinson divider was compared to the simulated results from Sonnet as shown in Fig. 15. For clarity purposes, the curves for the symmetrical responses are not given (S33, S23, S31, S13, and S12). The Wilkinson divider was measured on-wafer with a test chip containing the 3.3-V transmitter version as well as other various test circuits which are not related to this paper. A three-Port calibration to the probe

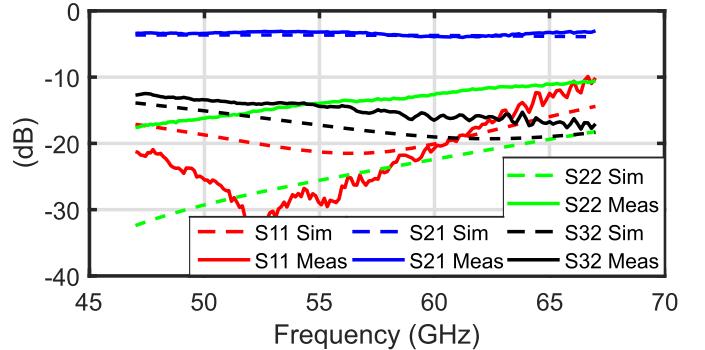


Fig. 15. Frequency responses (S_{11} , S_{21} , S_{22} , and S_{32}) of the 61-GHz Wilkinson power divider for measurement and simulation. The symmetrical responses (S_{33} , S_{23} , S_{31} , S_{13} , and S_{12}) are not shown for clarity.

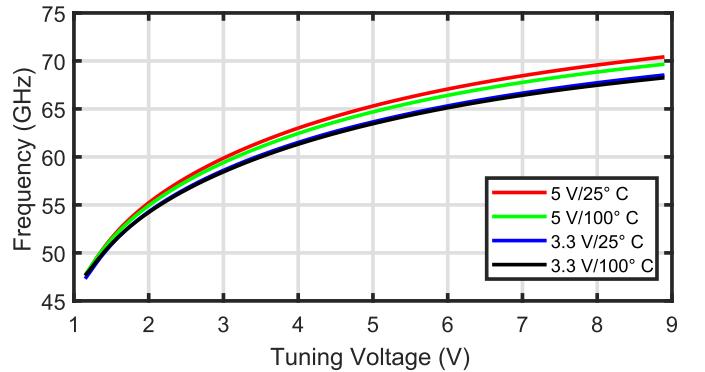


Fig. 16. Measured oscillation frequency versus tuning voltage of the chips at room temperature ($\approx 25^\circ \text{C}$) and 100°C .

tips, which were a Cascade GSGSG and ground-signal-ground (GSG) probe, was done with a Cascade calibration substrate. The measurement itself was done with a four-Port Keysight PNA-X working up to 67 GHz. The pad-capacitance for the GSG and GSGSG configuration was de-embedded offline. The measurement shows a good agreement between measurement and the Sonnet simulation for the input match S_{11} , the insertion loss S_{21} and the isolation between the splitted ports S_{32} , while the matching at ports S_{22} and S_{33} (not shown) differs quite strongly. The match of S_{22} and S_{33} is mainly depended on the dedicated 100Ω resistor between the two ports. The simulation in Sonnet for the TaN-resistor of the used technology is probably too optimistic and caused the mismatch between simulation and measurement. At the intended operating frequency of 61 GHz, the results for all ports are quite good and proves the usability of the whole lumped element Wilkinson divider.

Fig. 16 shows the measured tuning characteristics of the two transmitter chips for ≈ 25 and 100°C . The 5-V chip shows a slightly larger TR while the 3.3-V chip shows a slightly better temperature stability. The center frequency f_0 is 59 GHz with a TR of 22.8 GHz and a relative FTR of 38.6% for the 5-V chip (3.3 V: $f_0 = 57.9 \text{ GHz}$, TR = 21.23 GHz, FTR = 36.7%). The small decrease in TR and center frequency is due to the lower voltage V_{CB} , and hence an increased junction capacitance of the oscil-

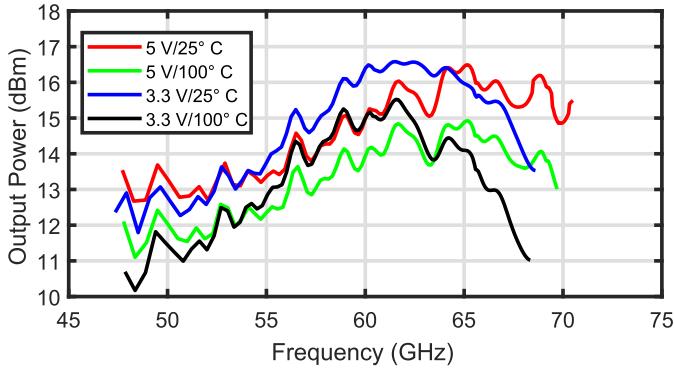


Fig. 17. Measured nominal differential output power versus frequency for the two different transmitter chips. The results were taken at room temperature ($\approx 25\text{ }^{\circ}\text{C}$) as well as $100\text{ }^{\circ}\text{C}$.

lating transistors. The measurement results for the tuning characteristic of the 3.3-V VCO and $\approx 25\text{ }^{\circ}\text{C}$ agree very well to the simulation results in Fig. 3.

In Fig. 17, the measured nominal output power over oscillation frequency is shown for both chips at the same temperatures. The output power is measured at one port while the other one is terminated with $50\text{ }\Omega$ at the differential probe. Losses from the measurement setup are corrected. The maximum nominal output power, taking the systematic ripple from the measurement setup into account, is found to be 15.9 dBm at 65.2 GHz and 17 dBm at 61.6 GHz for the 5- and 3.3-V version, respectively. This 17 dBm also fits well to the load-pull simulation in Fig. 5 considering a maximum output power of 20.2 dBm , a loss of 1.5 dB from the matching network and 1 dB from the slight mismatch of Z_{in} from Z_{opt} . The temperature stability of both versions is excellent with a degradation of only 1 dB over a temperature range of $75\text{ }^{\circ}\text{C}$. The same ripple can be observed in all measurements even though chips, probe touch downs, and temperature changed, which indicates a systematic problem in the measurement setup. The observed ripple in the measured output power is probably due to the probe which is matched to a differential $100\text{ }\Omega$ while the output is matched to $100\text{ }\Omega$ only when a short bond wire is present. The periodicity of the ripple is $\approx 3.1\text{ GHz}$. With an assumed Polytetrafluoroethylene dielectric ($\epsilon_r = 2.1$), this corresponds to a length of the disturbance of $\approx 33\text{ mm}$, which fits well with the probe dimensions from the tip to the coax-adapter transition.

The frequency response shown in Fig. 17 for the two chips and the two different temperatures, also considering the ripple on the measurements, stays within a variation of approximately 3 dB . Therefore, the whole TR of the VCO equals the 3-dB bandwidth of the transmitter chips. These are good results for a PA with resonant loads considering the wide relative TR of the systems. This is mainly achieved by driving the single stage PA into saturation with the input power of the VCO.

The unnecessary systematic approach toward an ultra-wideband design for a continuous-wave (CW) application at 61 GHz was pursued to overcome fabrication tolerances. In main part, this was done to counter the expected fabrication

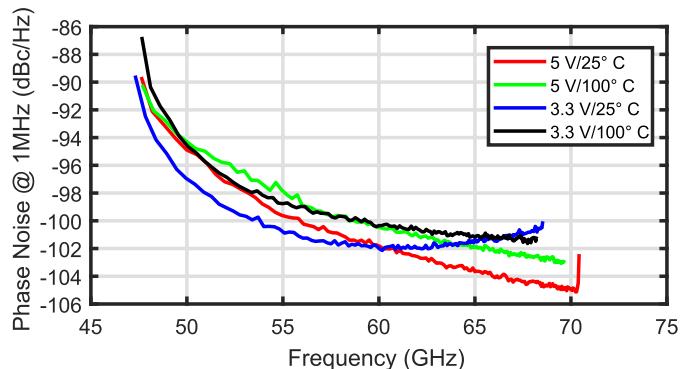


Fig. 18. Measured phase noise versus frequency for the two transmitter chips also verified at chuck temperatures of $25\text{ and }100\text{ }^{\circ}\text{C}$.

spread of the prototype CMOS-RFID-tags with integrated on-chip antennas and only in small part for the tolerances of the reader itself. This allows the reader to cover a wide spread of still to be fabricated CMOS tags in early demonstrations with the here presented reader frontend. Also, the presented designs can be easily reused in the future for possible wideband applications with small modifications for, e.g., a frequency modulated continuous wave radar system.

In Fig. 18, the comparison regarding phase noise at 1-MHz offset frequency for both transmitters is shown versus the frequency. The phase noise for all curves stays below -87 dBc/Hz , even at the lower end of the TR, where the PN varactors are slightly operated in the forward region. Around the intended frequency of 61 GHz , both chips show a phase noise of better than -102 dBc/Hz at room temperature. While the 3.3-V version shows a minimum around 60 GHz , the 5-V version shows an even better phase noise performance with increasing frequency with a phase noise as low as -105 dBc/Hz . At room temperature, the deviation from measurement to simulation results given in Section II-A is only about 1 dB .

For high temperatures, the response of the 3.3-V version changes and gets very similar to the 5-V version not only in the results but also in the shape of the curve. This is most probably due to the slightly changed biasing points especially for the oscillating transistor pair of the VCO. All three temperature dependent V_{BE} 's with a voltage drop of about $-2\text{ mV}/\text{ }^{\circ}\text{C}$ let the oscillating transistors exclusively benefit from an increase of V_{CB} with temperature. The drop in phase noise due to the temperature change of about $75\text{ }^{\circ}\text{C}$ is approximately 2 dB .

As a last shown experimental result of the transmitter chip, the input power $P_{\text{PA},\text{In}}$ to and the output power $P_{\text{PA},\text{Out}}$ of the PA are shown in Fig. 19 at the intended frequency of 61 GHz . The power added efficiency (PAE) of the PA is also given in Fig. 19. For clearness only results of the 3.3-V version are shown. The output power of the VCO is varied by changing the core current of the VCO, and this can be done in the same manner as the core current of the PA. The input power to the PA is taken through the external LO output of the chip and is calculated back to the output of the Wilkinson divider. The maximum gain of the PA is 17 dB and the input referred compression point is -0.14 dBm . The nominal

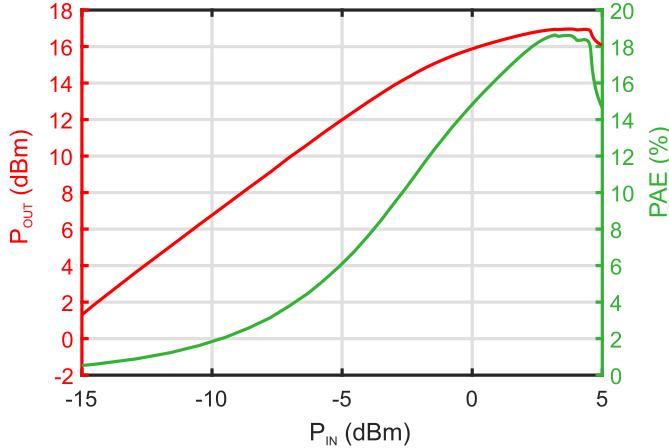


Fig. 19. Measured output power and PAE of the 61 GHz 3.3-V PA versus input power. The VCO output power and, hence, the input power to the PA are varied by changing the VCO core current.

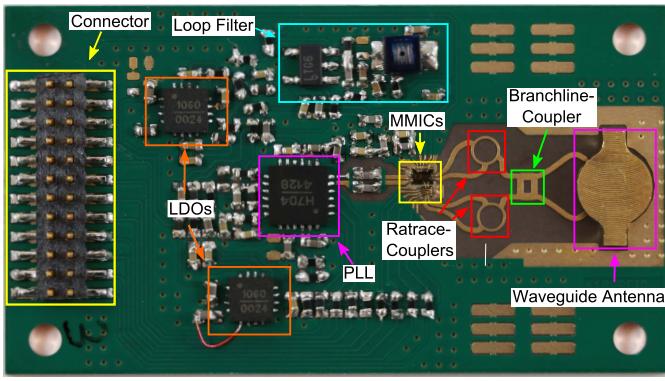


Fig. 20. RFID reader frontend PCB with transmitter and receiver MMIC. The board dimensions are 45 mm by 25 mm. The substrate material is Rogers5880.

biasing point of the VCO is at an input power to the PA of 3.7 dBm which drives the PA well into saturation with a nominal output power of 17 dBm, resulting in a PAE of 18.6% (5 V: $P_{PA,In} = 3.1$ dBm, $P_{PA,Out} = 15.9$ dBm, PAE = 10.5%).

B. System Results

Both chips, the transmitter (5-V version) and receiver MMIC, have been integrated onto the PCB as shown in Fig. 20. The VCO is stabilized by a commercial PLL integrated circuit (HMC 704), while two low-dropout regulators provide the necessary 5 V for the MMICs. The connector allows the board to be connected to the backend board of the reader (not presented here). The backend provides serial peripheral interface bus programming signals and the reference clock signal for the PLL as well as the supply voltage. The MMICs are connected via a network of couplers to a waveguide antenna, which radiates toward the bottom of the board. Two rat-race couplers provide differential to single-ended conversion of the transmitter output and single ended to differential conversion of the receiver input. A branch line coupler provides isolation between the TX and RX paths and also feeds the waveguide antenna with two signals which have a phase difference of 90° to allow the transmission of a circular polarized wave by the waveguide antenna.

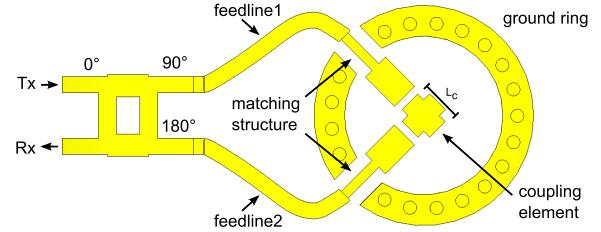


Fig. 21. Drawing of the PCB top side metal of the waveguide antenna including branchline coupler. The antenna radiates into the drawing plane.

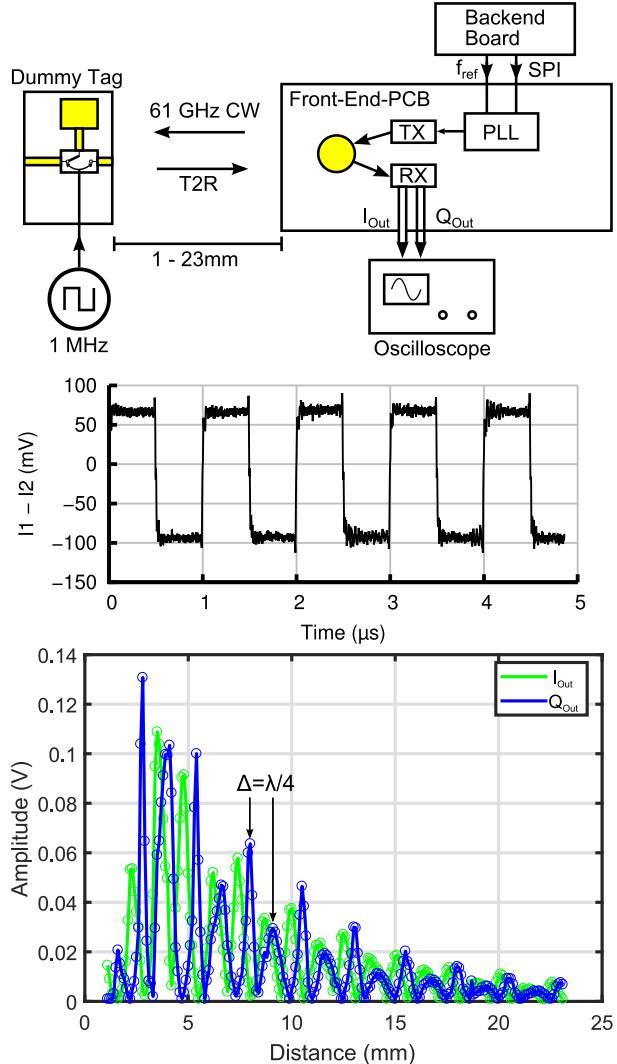


Fig. 22. Setup used to test the receive path of the of the RFID reader frontend. The Reader PCB was mounted on a translation stage that allows to change the distance between reader and dummy tag between 1 and 23 mm (top). Output signal measured by the oscilloscope. Only one channel of the receiver output is shown (I_{out}) (middle). Distance-dependent amplitude of I_{out} and Q_{out} (bottom).

Two major design goals were achieved during the design process of the antenna: First, the radiation direction must be toward the bottom of the PCB, as the tag will be close to the antenna aperture and it must be prevented that the MMIC and other sensitive devices on the top of the PCB touch the tag or its surrounding. As the tag antenna will be linear polarized, but the communication should be independent of rotation, the reader antenna must be circular polarized.

TABLE III
PERFORMANCE SUMMARY OF THE VCOs AND COMPARISON TO THE STATE OF THE ART

Ref.	Tech./ f_T/f_{max} -/(GHz)/(GHz)	P_{out} (dBm)	f_0 (GHz)	TR/FTR (GHz)/(%)	PN@1 MHz (dBc/Hz)	P_{DC} (mW)	FoM _{VCO-PAT} (dB)
This Work 5 V	SiGe/250/370	6.6	59	22.8/38.6%	-105	205	-195.6
This Work 3.3 V	SiGe/250/370	7.2	57.9	21.23/36.7%	-102	136	-194.4
[4]	SiGe/250/340	9	61.1	5.6/9.2%	-101	198	-182
[26]	65 nm CMOS/-/-	-10	62.8	15.3/24.4%	-92	21.5	-172.4
[27]	28 nm CMOS/-/-	-15.6	61.5	19/30.9%	-93	68	-164.7
[28]	SiGe/200/250	10.5	65.8	21.5/32.7%	-96	462	-186.5
[18]	SiGe/170/250	12	80	24.3/30%	-97	240	-192.9
[19]	SiGe/170/250	9	80.8	25.6/31.7%	-97	165	-192
[29]	SiGe/175/265	18.5	77	6.7/8.7%	-97	1200	-182.2

TABLE IV
PERFORMANCE SUMMARY OF THE PAS AND COMPARISON TO THE STATE OF THE ART

Ref.	Tech./ f_T/f_{max} -/(GHz)/(GHz)	f_0 (GHz)	3 dB-Bandwidth (GHz)	Gain (dB)	P_{Sat} (dBm)	P_{DC} (mW)	PAE _{Peak} (%)
This Work 5 V	SiGe/250/370	59	22.8	16.5	15.9	355	10.5
This Work 3.3 V	SiGe/250/370	57.9	21.23	17	17	254	18.6
[4]	SiGe/300/350	60	8.5	25.5	15.5	264	9.5
[30]	SiGe/300/350	60	7	20	20	240-640	12.7
[31]	SiGe/150/150	60	10	20	20	353	20
[32]	65 nm CMOS/-/-	60.5	15	15.5	18.1	1504	3.6
[33]	90 nm CMOS/-/-	60	24.5	20.1	20.6	535-573	20.3
[34]	45 nm CMOS-SOI/-/-	60	< 8	17.4	27.9	-	23.4

These features are provided by the circular waveguide antenna shown in Fig. 21. The design is based on the circular waveguide to microstrip transition presented in [24]. The waveguide is composed of a circular hole in the copper backing, a ground ring on the front side of the PCB which is connected by vias to the copper backing and a lid of approximately $\lambda/4$ height which is placed on the ground ring and provides a termination of the waveguide (not shown in Fig. 20 but visible in Fig. 21). Compared to [24], a second feedline was added to support the circular polarization of the antenna. The feedlines are connected via a matching structure to the coupling element located in the center of the waveguide. The length L_C of the coupling element is approx. $\lambda/4$. The radius of the waveguide must be larger than 1.44 mm and smaller 1.88 mm to allow only the fundamental mode to propagate. The exact dimensions of the waveguide and feedlines have been found using an optimizer within an EM simulation software.

The isolation between TX and RX has also been estimated by means of EM simulation: According to the 3-D EM simulation, the TX to RX isolation is better than 25 dB if the reader is placed in an empty space. It must be assumed that in more realistic scenarios, the RX to TX feedthrough is dominated by reflections of whatever object is located in front of the reader antenna. For example, the RX to TX isolation reduces to 7 dB, when a perfect electric conductor plate is placed in a distance of 5 mm in front of the reader antenna. This is, however, a worst-case scenario. In reality, an isolation between these two extremes can be expected. The T2R communication has been tested with the dummy tag described in Section II-E and the setup shown in Fig. 22. A simplified version of the reader backend was connected to the reader frontend. The output of

the receiver chip was connected to an oscilloscope to measure the received and down converted signal. The dummy tag was connected to a 1-MHz rectangular signal generator. Since the 1-MHz rectangle could be measured with the oscilloscope, as shown in Fig. 22, the functionality of the T2R path could be verified. A distance-dependent measurement reveals that up to the highest measured distance of 23 mm, a usable signal can be received. For distances smaller than 3.5 mm, a degradation of the signal strength can be observed caused by the reduced conversion gain in case of high TX to RX CT as shown in Fig. 10. The higher CT was caused by metal in the vicinity of the dummy tag. When using the final tag, it is expected that the range is limited by the R2T power transfer to less than 10 mm. The communication distance of more than 20 mm is thus more than sufficient.

IV. CONCLUSION

This paper presents a transmitter and a receiver MMIC used in an RFID reader frontend operating at 61 GHz, which were fabricated in a SiGe technology. The transmitter chip was presented with two different supply voltages, while using the same architectural topology and technology. Both variants are able to cover the requirements from Fig. 1 and are usable in an RFID reader. The 3.3-V version shows a dc-to-RF-efficiency of 12.9% which is more efficient than the mere voltage change would suggest (5 V: 6.9%). To the best of the authors knowledge the rel. bandwidth of 36.7% is a record for signal generators with fundamental VCOs in SiGe and it is only exceeded by its 5 V sibling with 38.6%, especially considering that this is the 3-dB bandwidth and not the frequency TR. Otherwise the two sources are comparable in performance and

are both on par with the state of the art. The receiver MMIC has been designed to tolerate high carrier feed through which could be verified by a measurement of the complete RFID reader frontend by using a dummy RFID tag.

To give a fair comparison of oscillators in Table III, we used the FoM_{VCO-PAT} defined in [25]. In this table, only VCOs with a continuous analog TR are compared. This defined figure of merit (FoM) factors every key performance element and is based on the three FoMs defined by the International Technology Roadmap for Semiconductors. It is defined as

$$\text{FoM}_{\text{VCO-PAT}} = \left(\frac{f_0}{\Delta f} \right)^2 \left(\frac{\text{FTR}}{10} \right)^2 \frac{P_{\text{Out}}}{\mathcal{L}(\Delta f) P_{\text{dc}}} \quad (1)$$

with f_0 is the center frequency, Δf is the offset frequency at which the phase noise $\mathcal{L}(\Delta f)$ is taken, FTR is the relative frequency TR in percent, P_{Out} is the output power of the signal source, and P_{dc} is the power consumption of the signal source. Based on this FoM_{VCO-PAT}, the presented VCOs show, to the best of the authors knowledge, the best overall performance.

An additional comparison of the state of the art with the here presented PAs in the same frequency range is given in Table IV. The developed PAs show a comparable performance to the state of the art in regard to P_{Sat} and PAE_{Peak}. Overall, they show a good total performance even with high temperature variations and are not relying on power combining techniques. Especially the 3.3-V PA shows a very good peak efficiency considering the chosen Class-A topology. Concerning the 3-dB bandwidth, the developed PAs also reflect the complete wideband system design and are limited in measurements only by the on-chip VCO.

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