

# A 60-GHz 8-Way Phased-Array Front-End With T/R Switching and Calibration-Free Beamsteering in 28-nm CMOS

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**Abstract**—An eight-way phased-array TRX front-end with RF phase shifting and on-chip transmit/receive switching is implemented in 28-nm CMOS. The TX  $P_{1\text{dBout}}$  and RX noise figure (NF) are 10 dBm and 6.8 dB, respectively. The active phase shifter shows less than  $5^\circ$  phase resolution and amplitude errors within  $\pm 0.35$  dB. The 9.6-mm<sup>2</sup> chip consumes 231 mW in RX and 508 mW in the TX mode from a 0.9-V supply. When combined with PCB antennas, a  $\pm 46^\circ$  scan angle is obtained with  $<0.4$  dB peak-to-peak gain ripples without calibration. We also present an approach to express the noise performance of a phased-array receiver in terms of the effective isotropic NF, as an extension to the NF, which is only defined for a two-port system.

**Index Terms**—Low-noise amplifiers (LNAs), millimeter-wave communication, millimeter-wave integrated circuits, noise figure (NF), phase shifter (PS), phased arrays, power amplifiers, transmit/receive (T/R) switch, wireless.

## I. INTRODUCTION

WIRELESS communication at millimeter-wave frequencies becomes a necessity to cope with the ever-growing demand for higher data rates. For multi-Gb/s wireless communication, the 57–66-GHz band has been allocated already since more than 10 years. With 2 GHz of channel bandwidth, datarates of up to 4.62 Gb/s can be achieved with 16-quadratic-amplitude modulation. However, it is expected that the first massive deployment of wireless communication well above 6 GHz will come with the introduction of 5G, using some lower frequency bands, e.g., around 28 GHz [1]. This paper describes a TRX front-end chip for wireless communication in the 57–66-GHz band, but many insights and design concepts of this paper can be adopted for lower millimeter-wave frequency bands. An important concept that improves the link budget in millimeter-wave wireless communication is beamforming. Thanks to the smaller wavelength at millimeter-wave frequencies, the size of the antenna arrays needed for beamforming

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can be kept small. The TRX front-end chip described here performs eight-way beamforming.

To limit the complexity of chips or modules with a large antenna array, beamforming at RF is the most viable approach. Beamforming at baseband (analog or digital) and beamforming with phase shifting in the local oscillator (LO) path are not preferred as they both lead to a duplication of up- and down-conversion mixers, giving rise to a heavy LO distribution. In addition, those approaches complicate calibration. For example, in a direct conversion architecture, the compensation of the LO feedthrough in the TX and of dc offset in the RX is duplicated over the antenna paths.

For the implementation of RF beamforming, a wide variety of phase shifters (PSs) can be found, which can be classified into four categories [2]: reflective-type, loaded-line, switched-delay PSs, and vector modulators. Practical implementations of the first three types have an insertion loss that varies with the required phase shift. This requires compensation by a high-resolution variable-gain amplifier and, consequently, a complex calibration procedure. Vector modulators, on the other hand, are more suitable to minimize the dependence of insertion loss on phase shift [3], [4]. In this paper, an active vector modulator is used for phase shifting at RF with minimal gain variations over phase shift. Although limited in linearity compared to its passive counterpart, gain blocks following an active PS can overcome its linearity limitation. A passive combiner and splitter complete the beamforming operation in the RX and TX, respectively.

Next to the eight-way RF beamforming functionality, this chip includes on-chip transmit/receive (T/R) switching and programmable gain (see Fig. 1). The T/R switching has little impact on the TX OP<sub>1dB</sub> and the RX noise figure (NF). Furthermore, RX and TX gain values are flat over the phase shift values.

The noise performance of a phased-array receiver cannot simply be characterized accurately with the NF of one single antenna path while all other antenna paths are not excited. To this end, we introduce the effective isotropic (equivalent) NF (EINF) as a counterpart of the EIRP in a phased-array transmitter.

The outline of this paper is as follows. The circuit design as well as a discussion on the layout and on the mounting

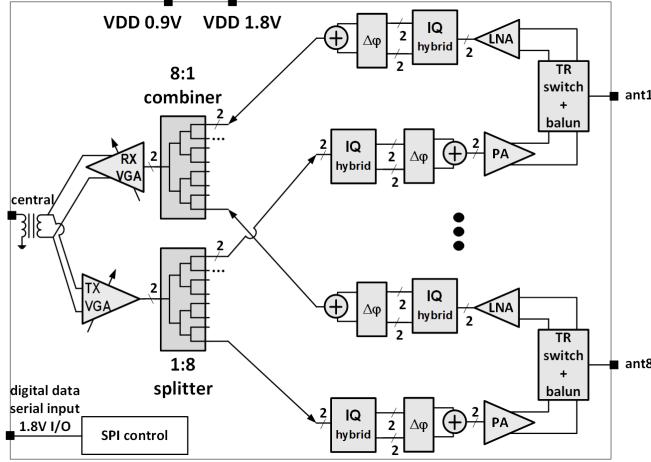


Fig. 1. Block diagram of the eight-way TRX front-end.

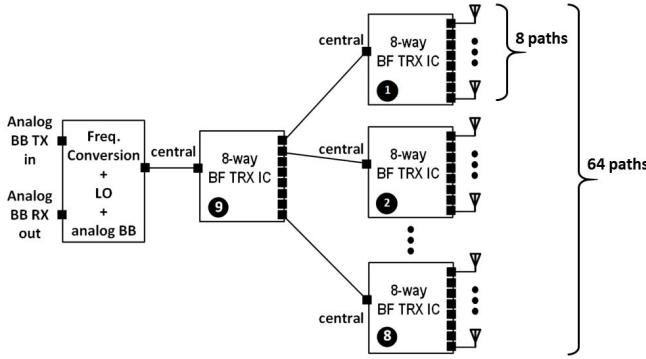


Fig. 2. Use of the TRX front-end chip in a cascade for 64 antenna paths.

on the PCB with antennas is discussed in Section II. Detailed characterizations and a discussion on the EINF are discussed in Section III. Finally, the conclusion is presented in Section IV.

## II. ARCHITECTURE AND CIRCUIT IMPLEMENTATION

### A. Architecture

This front-end chip with eight-way beamforming in RX and the TX mode is assumed to operate both for short-range indoor communication with eight antenna paths and for longer ranges with 64 antenna paths targeting for example small-cell backhaul applications. This can be obtained by cascading eight of these front-end chips with an identical one at the center, as shown in Fig. 2. To address both scenarios, the gain of the RX and TX signal paths must be adjustable. For example, in the case of Fig. 2, gain is needed to overcome the loss of the wiring on the PCB between the central chip and the other eight chips that are connected to the antennas. The down-conversion circuitry is not provided in this chip. The use of an identical central chip allows combining this solution with an existing single (or few) path 60-GHz chip. However, a more efficient approach is to combine the central chip and the baseband chip in one in order to avoid the extra connecting line and two additional T/R switches (at the baseband chip output and the central chip input).

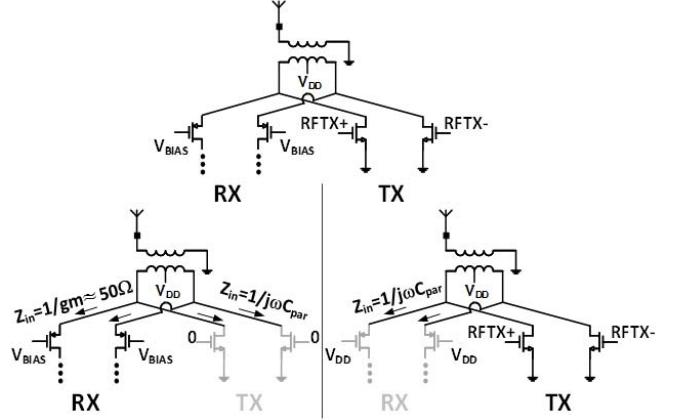


Fig. 3. T/R switch functionality combining a pMOS common-gate RX input stage with an nMOS common-source TX output stage.

The RF beamforming approach (see Fig. 1) is the same for RX and TX. The phase shift is realized by first making  $I$  and  $Q$  components of the signal using a  $90^\circ$  hybrid, after which they are combined in a weighted strength according to the target phase shift. This approach can be implemented using passive attenuators, as in [3]. The loss of these attenuators, however, leads to several problems: it requires extra gain for the LNA to minimize the impact of that loss on the overall NF. Second, it requires extra TX gain to achieve a given output power. Extra gain stages make the signal path longer and as such they form a challenge to maintain a wide bandwidth. In this paper, the variable attenuators are avoided and variable-gain amplifiers are used instead. The beamforming operation is completed by a passive splitter (TX) and combiner (RX).

The LNA and PA in each antenna path are designed and connected with each other in such a way that switching the bias of LNA and PA mimics the T/R switch functionality while avoiding explicit switches in the signal path. Finally, variable-gain amplifiers are provided both after the combiner in the RX part and alongside the chain in the TX part.

### B. LNA, PA, and Transmit Receive Switching Scheme

The 28-nm bulk CMOS technology does not allow using a single-pole double-throw (SPDT) switch without a significant degradation of the RX NF and/or the output 1-dB compression point  $P_{1dBout}$  of the TX part. For example, circuit simulations show that a switch that would limit the increase of the NF to 1.5 dB leads to a switch size that in the TX mode forms an unacceptably high capacitive load. Moreover, transistor models of a planar bulk transistor are often incomplete to accurately predict the switch behavior at millimeter-wave frequencies.

Instead of using an SPDT switch in the signal path, the combination of a common-gate stage as an RX input stage and common-source stage as a TX output stage avoids the use of physical switches, as either of these two stages can be made invisible for each other by just disabling them via their gate bias [5], [6]. The extension of that concept to differential circuits and to millimeter-wave frequencies is shown in Fig. 3. The pMOS common-gate stage at the LNA input stage leads to a relatively easy input matching thanks to the significant

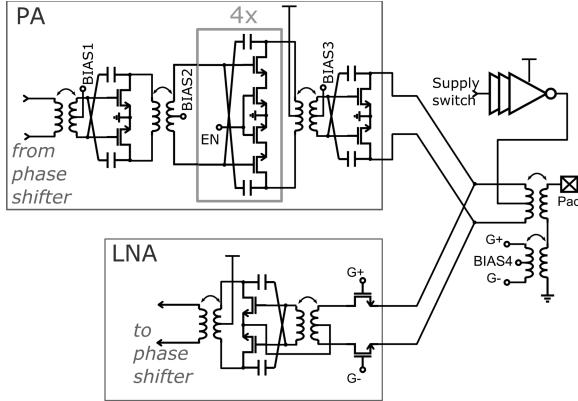
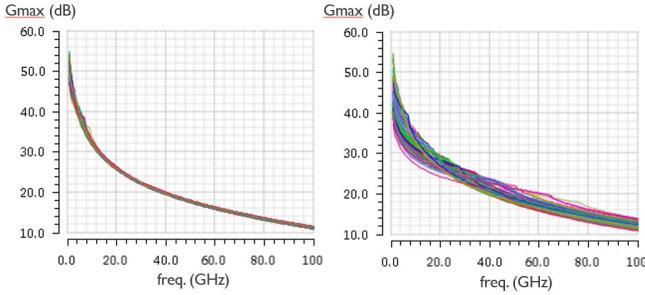


Fig. 4. PA-LNA with T/R switch functionality using nMOS stages only.

Fig. 5. Simulated values of  $G_{\max}$  as a function of frequency for capacitive neutralization in the PA output stage using MOS capacitors (left) and MOM capacitors (right).

real part of the input impedance which is close to  $1/g_m$  of the common-gate transistor. Switching this device off via the gate bias in the TX mode removes that real part, such that it does not lead to power loss in the TX mode while it makes the TX output matching easier. This RX input stage is combined with a common-source amplifier as a TX output stage. When the latter is switched OFF, again via its gate bias, then its output impedance is mainly capacitive.

While the differential T/R switching scheme of Fig. 3 avoids lossy switches in the signal path, the pMOS transistors in the common-gate stage lead to an inferior performance compared to the usage of nMOS devices. Therefore, switching the supply voltage in addition to the gate voltages allows using an nMOS common-gate LNA instead of a pMOS one and it provides extra isolation by reducing the loading effect of the PA and LNA blocks on each other when switched OFF(see Fig. 4). The large inverter used to switch the supply has a negligible impact on the PA efficiency. This concept is different from [7] which in the low-GHz range reuses a differential cascode stage for PA and LNA, controlled by a switch in the common-mode path and two series switches in the differential path, which are lossy at millimeter-wave frequencies.

The PA uses three pseudo-differential transformer-coupled stages with cross-coupled capacitive neutralization (see Fig. 4). The transistors in the output stage have minimum length and a width of  $160 \mu\text{m}$ , divided into fingers of  $1 \mu\text{m}$ . For the capacitive neutralization, MOS capacitors are used (80 fingers in the output stage) instead of method of moments (MOM) capacitors as the latter ones yield a performance that is sensitive to process variations. This is illustrated in Fig. 5 with

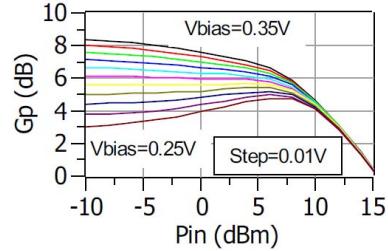
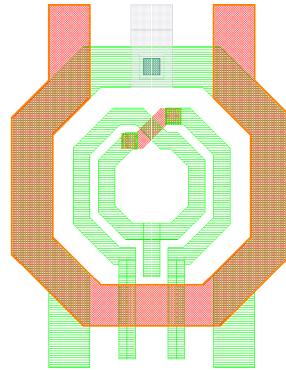
Fig. 6. Simulation of the power gain  $G_p$  as a function of the input power for different gate bias voltages at 61 GHz. Gain expansion is seen in class AB operation and can be controlled with the gate bias voltage.

Fig. 7. Front-end balun with a turn on metal 8 (red) connected to the pad, a turn on top metal 9 (green) connected to the PA and source node of the LNA CG device, and an additional third inner turn for gain boosting.

the simulated value of the maximum available gain  $G_{\max}$  over process corners for neutralizing MOS and MOM capacitors. Only the active part of the PA output stage is evaluated here, using schematic circuit views. It is seen that  $G_{\max}$  values change by 4.5 dB when using MOM capacitors. Although MOS capacitors are bigger in layout, they follow the process changes of the main transistors yielding much less variation of  $G_{\max}$  over process corners.

To limit power consumption in the output stage at backoff, class AB operation is preferred over class A at the expense of a lower power gain  $G_p$  (see Fig. 6). In class AB operation, gain expansion occurs, which can be controlled by adjusting the gate bias voltage.

The second stage of the PA consists of four parallel stages that can be enabled/disabled, yielding variable gain.

The common-gate input stage of the LNA (see Fig. 4) uses transformer-coupled  $g_m$ -boosting that is combined with the input balun as in [8]. The balun layout is shown in Fig. 7, where top metal layers 8 (red) and 9 (green) are used for the connections to the pad and to the circuit, respectively. An inner inductor is implemented in metal 9 for gain boosting with a smaller diameter to reduce coupling from the input signal on metal 8 in the RX mode. This boosting also improves the NF of the common-gate stage, similar to capacitive  $g_m$  boosting [9]. The second LNA stage (see Fig. 4) is a differential common-source stage with capacitive neutralization. The dc current of the two LNA stages is reused as in [10]. While this halves power consumption, the transconductance of the

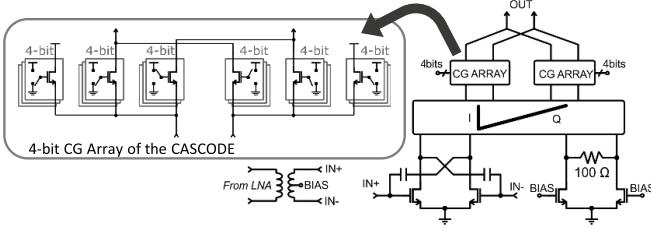


Fig. 8. Phase shifter schematic.

common-gate transistors is reduced, as for minimum-length devices,  $g_m$  depends on  $V_{DS}$ , which is now halved due to the current reuse. Circuit simulations show a degradation in NF of around 0.5 dB compared to a design without current reuse. Furthermore, the second stage has also less gain due to a lower  $g_m$  caused by a lower available  $V_{DS}$ . The LNA gain reduction is 3.1 dB reaching a simulated value of 12 dB. Power consumption is 17 mW.

The supply switch uses three inverter stages to buffer the large output stage, where the PMOS total width is 2.88 mm to allow a large PA current to flow with minimal series resistance. Compared to a direct supply connection to the center tap, the PA performance is reduced by 0.4-dB output compression point, 0.1-dB gain, and 1% efficiency (from 22%). The use of an inverter does not provide any power supply common-mode rejection. For that a voltage regulator can be used.

The LNA CG source node swings in the TX mode. Since the gate is weakly coupled to the input for gain boosting, the gate node also slightly swings in antiphase. This potentially leads to a large negative gate-source voltage in the TX mode that can deteriorate the device reliability. Instead of biasing the LNA CG stage at 0 V in the TX mode, the gate node can be kept at 0.5 V. In this case, simulations show that the LNA gate-source voltage at TX compression does not exceed  $-1.4$  V in the TX mode, controlling the voltage stress on the device. This comes with an acceptable loading influence on the PA, where the compression point is reduced by 0.5 dB in simulation. This is not seen from measurements as the TX VGA before the splitter also contributes to the overall TX compression point. Therefore, switching between TX and RX modes can be performed by acting only on the supply switch and the PA bias voltage.

### C. Phase Shifter, Splitter, Combiner, and VGAs

The PS, shown in Fig. 8, is based on a vector modulator. To generate  $I/Q$  components from the differential input, a wideband differential hybrid [11] is inserted between the common-source and common-gate part of a pseudo-differential cascode stage. This way, no extra current is needed for  $I/Q$  generation. Compared to [4], where  $I/Q$  generation is realized in a pseudo-differential cascode stage in which a transmission line is inserted in one of the stages, our approach is more wideband, compact and provides common-mode rejection in the frequency band of operation thanks to the use of transformer-based implementation.

In both  $I$  and  $Q$  branches of the PS, the common-gate stage consists of a binary weighted array to which the 4-bit phase

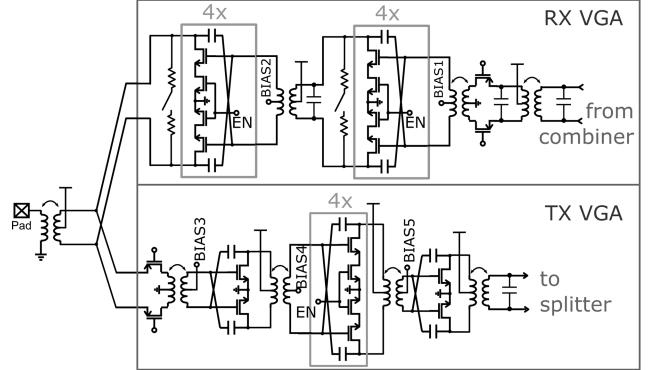


Fig. 9. Schematic of variable-gain amplifiers in the RX part and TX part.

control is applied at the gate. A copy of the 4-bit arrays with crossed outputs is implemented for the sign bit. This leads to a total of 5 bits for phase control in each  $I$  and  $Q$  branches of the PS including the sign bit. The common-gate topology establishes a conjugate match at  $I$  and  $Q$  outputs of the hybrid. The input port of the hybrid is connected to a neutralized pseudo-differential pair that shares the dc current with the  $I$  branch of the hybrid. The branch at the isolated port of the hybrid shares the current with the  $Q$  branch. A floating 100- $\Omega$  resistor is used for terminating the isolated port. To maintain a similar impedance level at the hybrid output over the PS settings, a 4-bit controlled array of common-gate transistors is provided with their drain connected to the power supply. In this way, the dc current is kept constant over all phase shift values. Still, the impedance seen at the  $I$  and  $Q$  outputs of the hybrid changes slightly over the code values for  $I$  and  $Q$ . Furthermore, the summation of  $I$  and  $Q$  is performed in the current domain with a finite output impedance of the  $I$  and  $Q$  branches that depend on the code for  $I$  or  $Q$ . These effects slightly distort phase and amplitude of the combined signal, as will be evidenced with the measurements in Section III-A.

The signal combination uses a differential three-stage Wilkinson combiner. Although a passive structure is bidirectional, it is not reused as a TX splitter (see Fig. 1) in order to avoid a lossy switch in the signal path selecting between TX and RX modes. Instead, the TX splitter layout runs in parallel to the RX combiner. The structure is quite narrow ( $35 \mu\text{m}$ ) and needs to bridge long distances between each front-end and the central VGAs fixed by the chip floorplan. Crossovers are used to swap the position of the TX splitter output and RX combiner input connections to match their corresponding position in each front-end. The simulated loss of the splitter or combiner compared to a lossless one is 1.5 dB per stage. This leads to 6 dB loss in the three Wilkinson stages (combiner or splitter) including 1.5-dB mismatch losses. Furthermore, coupling between the TX splitter and RX combiner is not relevant here.

The variable-gain stages after the combiner in the RX part and in front of the splitter in the TX part are depicted in Fig. 9. The VGA stage in the RX part consists of three stages, the first stage, a pMOS common-gate stage, is followed by two variable-gain stages. In each of these two stages, the gain is not adjusted by any fine-tuning of the gate bias voltage but rather by selecting the number of parallel stages between one and

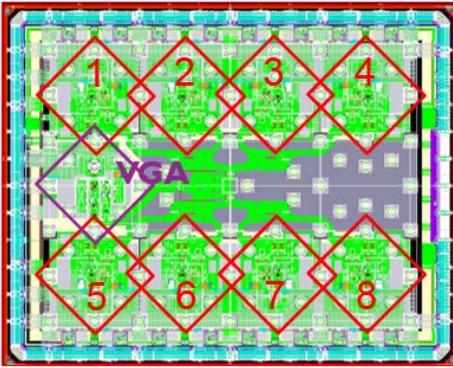


Fig. 10. Layout of the TRX chip showing different power domains.

four, using the “EN” signal in each capacitively neutralized stage. Furthermore, a switchable differential resistive load is used for an additional low-gain value with a high linearity. In this way, a gain range from 0 to 20 dB is realized in the VGA.

At the TX side, a four-stage VGA is foreseen in front of the splitter, with a gain from 9 to 18.5 dB. This VGA has an input common-gate pMOS stage, such as shown in Fig. 3. This way, the same transformer can be used as input matching network for the TX input and as output matching network for the RX VGA. The inferior pMOS performance in the common-gate stage still leads to a better overall performance than the use of a lossy series switch.

#### D. Layout, Processing, and PCB Assembly

The signal operations at millimeter-wave frequency required for the RF beamforming, in combination with the amplification stages give rise to a lengthy signal path, comprising eight transformers in the RX signal path and nine in the TX signal path. The primary and secondary windings of these transformers resonate with the capacitances seen by each of these windings. Staggering the resonance frequencies is used to improve the overall chain bandwidth.

The RF part of the chip, designed in 28-nm planar bulk CMOS, is partitioned in nine power domains, one for the central VGAs in the RX and TX paths and eight identical domains comprising PA, LNA, and PSs (see Fig. 10).

Several precautions have been taken to confine the electromagnetic fields as much as possible which limits unwanted couplings. Long interconnects are made with differential transmission lines with a small cross section, having a linewidth of 2  $\mu\text{m}$ , a pitch of 3.5  $\mu\text{m}$ , and shielding from the substrate underneath the conductors with a ground plane, comprising the four lowest metal layers. The ground is extended up to the highest copper level as shielding between parallel interconnect lines (see Fig. 11), which represents the most effective coupling mechanism in the structure as compared to others (e.g., crossovers). Substrate contacts are only used close to the active regions to avoid potential unwanted substrate couplings. Furthermore, ground and VDD planes on top of each other, comprising all metal layers, are used throughout the entire power domain. Both planes are composed of square

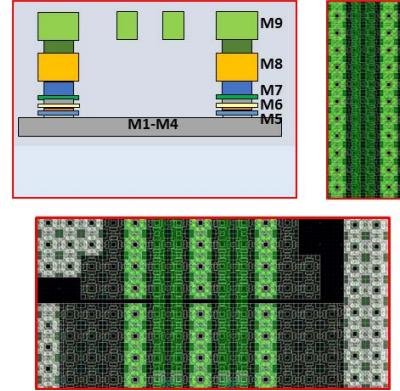


Fig. 11. Cross section and top view of the differential transmission lines used as interconnect on the chip (top). Crossing of these lines over the boundary between two power domains (bottom).

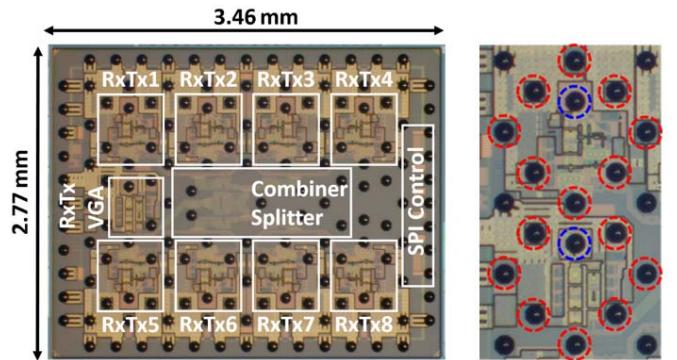


Fig. 12. Chip micrograph and detail of the transition between the chip and the microstrip lines on the PCB.

layout cells that are perforated in such a way that layout density rules are met.

A small gap of 1  $\mu\text{m}$  [close to DRC limits as shown in Fig. 11 (bottom)] is used between the ground planes of the central (i.e., VGA) and each front-end power domain to help limiting characteristic impedance variations of transmission lines connecting circuit blocks from both domains.

The chip (see Fig. 12) occupying 9.6  $\text{mm}^2$  is flipped on two different 12-layer Megrion six PCBs for testing, one with pads for probing and one with an antenna array.

Flip-chip connections at millimeter-wave frequencies can cause a parallel plate mode resonance between chip and package grounds. This can be a cause for strong electromagnetic coupling between different domains. This can be avoided by using a coaxial connection shielding the signal bump with a ring of ground bumps (see Fig. 12). The same coaxial structure is also preserved throughout the PCB with vertical vias. The ground vias are connected in every metal layer, leaving behind a perforated coaxial structure where the remaining holes are constrained by the minimum via pitch and spacing on the PCB.

The best shielding is realized when the coaxial structure is terminated with solid ground planes on both the chip and package sides. The grounds of different power domains are connected to one single ground plane on the PCB. Cuts in the chip ground plane within the coaxial structure are not

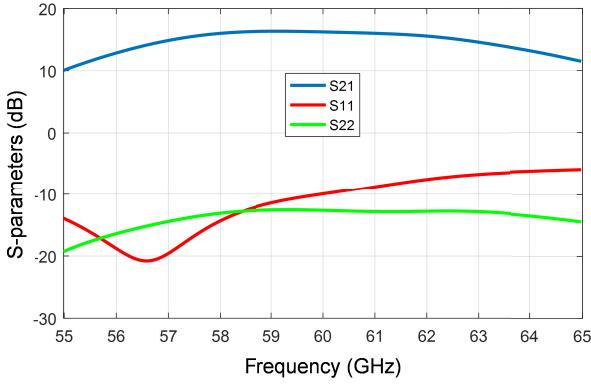


Fig. 13. Measured  $S_{21}$ ,  $S_{11}$ , and  $S_{22}$  of one single RX signal path with PS set at  $0^\circ$ .

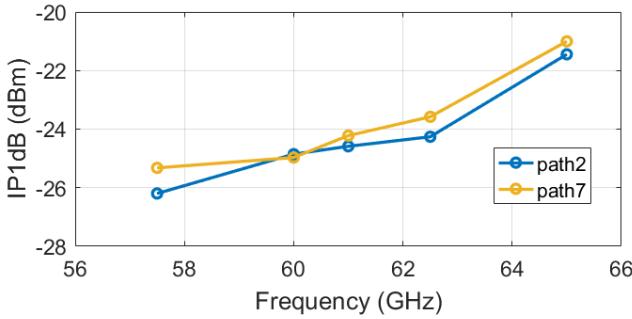


Fig. 14. Measured RX input compression point for different antenna paths.

preferred to avoid potential signal leakage in the substrate. Therefore, any necessary cuts (e.g., between ground planes of neighboring front-ends to avoid common impedance current path disturbances at low frequencies) were minimized to  $1 \mu\text{m}$ .

### III. MEASUREMENT RESULTS

#### A. Probed Measurements

The chip consumes 231 mW in RX mode and 508 mW in TX small-signal mode from a 0.9-V supply. One antenna path is characterized first with wafer probes put on PCB. With only one antenna path active, the Wilkinson combiner gives extra losses, which has its impact on gain and NF. Therefore, NF is only characterized with the antenna module where all paths are activated, as explained in Section III-B.

The single-path RX gain and the matching at input and output are shown in Fig. 13. The maximum  $S_{21}$  is 16.7 dB. As this has been obtained with all other antenna paths powered down, then, in order to estimate from this value the entire gain of the phased-array RX, one has to add 18 dB [ $20\log_{10}(N)$  dB for  $N$  antenna paths].

Gain and bandwidth can be traded off with the LNA bias: the maximum gain varies by 3.7 dB while bandwidth is between 7.7 and 9.8 GHz. The measured  $P_{1\text{dB}in}$  as a function of frequency (see Fig. 14) shows a value of  $-25$  dBm at 60 GHz. Differences between antenna paths are due to inevitable differences in probing of the antenna paths.

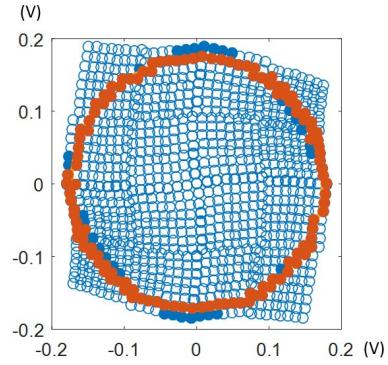


Fig. 15. VNA measurement of  $S_{21}$  (without de-embedding) at the RX output (path 4) at 60 GHz as a function of  $IQ$  settings in the PS. Approximation to a unit circle is shown for default settings (blue) and calibrated settings (red).

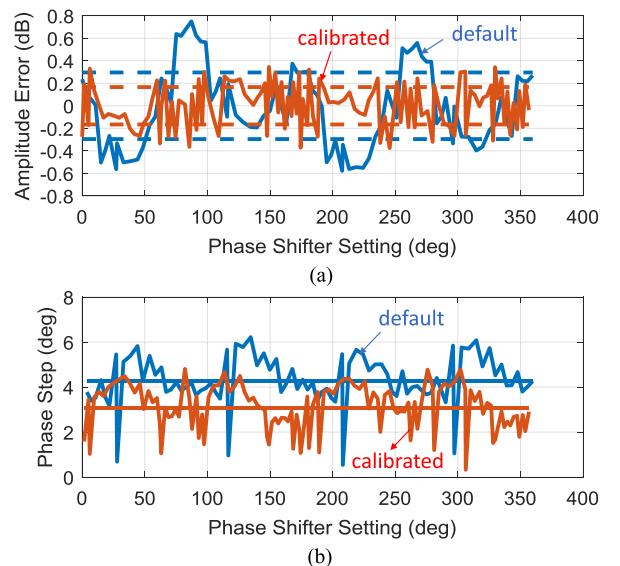


Fig. 16. Errors of the selected PS settings in Fig. 15. (a) Amplitude errors. (b) Phase steps.

To evaluate the PS, the RX gain is measured for all 1024  $I/Q$  settings at 60 GHz and an input power of  $-27$  dBm. In the  $IQ$  plane, different gain values ideally appear on a constellation plot with a rectangular grid, but due to the nonidealities explained in Section II-C, some deviations are observed. The used settings are also shown (in solid), where the points are closest to a circle either based on an ideal constellation (default settings) or based on the measured constellation (calibrated settings). The selected calibration algorithm chooses the PS points with minimum amplitude error to an ideal circle such that the maximum phase step is below  $6^\circ$ . Fig. 16 shows the amplitude errors and phase steps of the selected PS settings versus their angles. The default settings have a maximum amplitude error of  $\pm 0.8$  with 0.36-dB rms, while the phase step is better than  $6.1^\circ$  with an average value of  $4.3^\circ$ . After calibration, the amplitude error is within  $\pm 0.35$  at 0.16-dB rms, while the maximum phase step is  $4.9^\circ$  with an average value of  $3.1^\circ$ .

When the input power is lowered from  $-27$  to  $-40$  dBm, then the differences between the newly generated circles

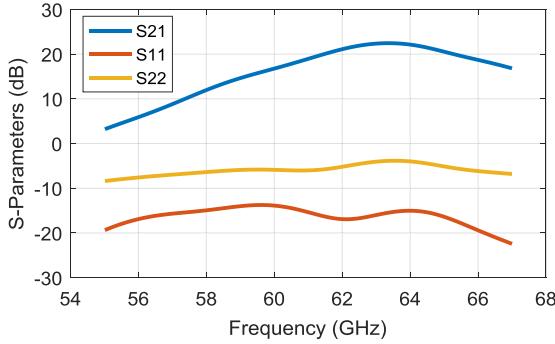


Fig. 17. TX S-parameters at 0° PS setting.

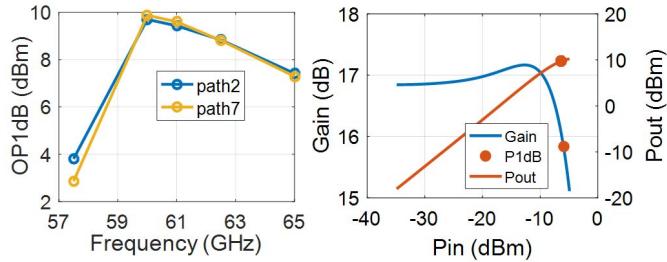


Fig. 18. P1dBout of TX as a function of frequency (left) and gain at 60 GHz as a function of input power for operation of the TX output stage in deep class AB while other stages operate at nominal settings (right).

and the one from Fig. 15 are less than 0.13 dB, which confirms that the phase shifts are not affected by compression.

It is difficult to judge phase mismatch between different front-ends based on the probed measurement since the measurement conditions are not exactly the same. For example, the probe contact can be different and probing pads that are on the PCB opposite to each other, with a probe from the same direction can cause 0.5-dB gain variations. It is found that the maximum calibrated circle amplitude variations are around 0.5 dB.

To have an idea of how the PS circle error behaves at the sides of a channel when using optimum settings for the middle of the channel, we take 60 GHz as an example of the middle of a channel and 59 and 61 GHz as examples of the sides of the channel. Using the calibration circle of 60 GHz, the maximum peak-to-peak amplitude error over the 2-GHz band is less than 1 dB with 0.3-dB rms, while the phase step remains below 4.9° with 3.1° average. When using the settings for 60 at 63 GHz, then the amplitude error is ±0.64 dB with rms values of 0.25 dB, while it remains below ±0.35 dB with an rms value of 0.16 dB when calibrated at 63 GHz. Extra errors over the whole frequency band may lead to using different PS settings for each 60-GHz channel.

The same setup is used to characterize one TX antenna path. The maximum  $S_{21}$  is 24.2 dB (see Fig. 17). At 60 GHz, the TX has a maximum  $P_{1dBout}$  between 9.5 and 10 dBm over different paths (see Fig. 18). This compression point can be further increased to 11 dBm by increasing the TX VGA linearity at the expense of more power consumption. At 5-dB backoff, the whole TX power consumption is 661 mW due to the class AB operation of the final stage.

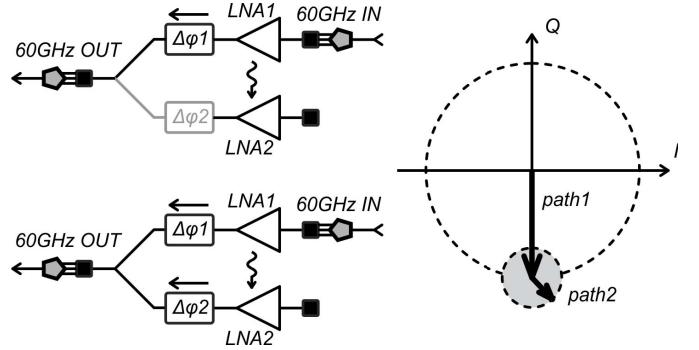
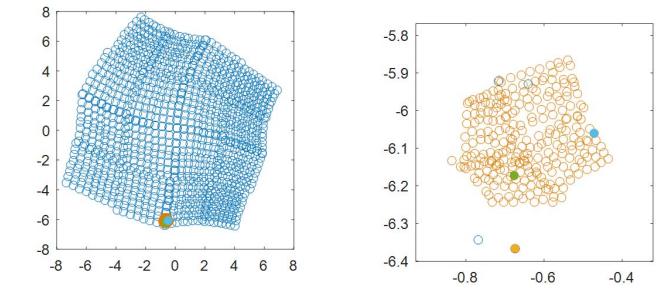
Fig. 19. Symbolic representation of RX path1 and path2 for the isolation test: path2 is switched on with zero  $I$  and  $Q$  PS settings representing the green point of Fig. 20 (top), and path2 PS is set to maximum representing the blue point of Fig. 20 (bottom). A phasor representation is also shown on the right.

Fig. 20. Isolation test: reference constellation with isolation constellation on top (left), and zoom-in on the isolation constellation (right).

Measurements of the TX gain as a function of PS settings yield similar results as for the RX, also when sweeping the operating frequency. For example, at 63.3 GHz, the maximum amplitude error is below 0.89 dB with an rms value of 0.34 dB. The maximum phase step is 6.25° and the average is 4.3°. After calibration, the amplitude error is within ±0.4 dB with an rms value of 0.2 dB while the max phase step is 5.7° with an average of 3.1°.

Finally, an experiment is performed to get an idea of the isolation between two adjacent RX front-end paths. This is useful to get an idea of the chip contribution to the leakage between two front-ends, leading to antenna pattern nonidealities (e.g., higher null depth and side lobes). The signal enters the input of one RX path, while the other path is either enabled or disabled (see Fig. 19) and the difference in the combined output represents the amount of signal leaking from the first path to the second. First, path1 is enabled and a full PS settings sweep is performed. At a fixed path1 PS setting, here a maximally negative  $Q$  value, and a zero  $I$  value, path2 is then powered up and its PS settings are swept. A phasor representation is also shown in Fig. 19, where changing the phase of path2 represents a small vector moving in a circle and added to the vector of path1.

Fig. 20 shows the uncalibrated PS constellation diagram of both cases and a zoomed-in view on the second case. The orange solid point (fixed path1 PS setting) moves to the green solid point when the second path is powered up with its PS set to  $I$  and  $Q$  values of 0, i.e., without its output going to the combined output. The move represents an amplitude drop that is mostly due to an IR drop after switching path2 ON.

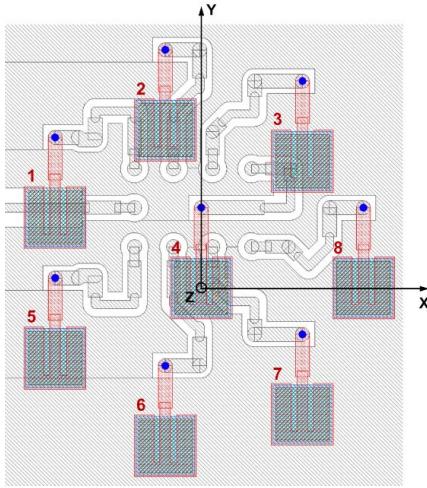


Fig. 21. Detail of the stacked patch antenna array with the stripline interconnection from chip to antennas. The stripline connection to the “central” terminal of the chip (see Fig. 1) enters the drawing from the left side.

Although the second constellation does not look very clean (probably due to the measurement accuracy), still we can get an idea about the maximum effect of the second path on the combined output, where the right side of the constellation is closer to the expected constellation shape. The blue solid point represents a second PS setting, which lies on the default PS circle. The amplitude difference between the solid green and blue points represent the change in  $S_{21}$  as an effect of leakage from path1 to path2 and are  $0.2321 \times$  (i.e.,  $-12.7$  dB). The gain of path1 when no signal from path2 is combined (amplitude of the green solid point) is  $6.21 \times$  (i.e.,  $15.86$  dB). Therefore, the leakage is  $0.2321/6.21$  (i.e.,  $-28.5$  dB), and the estimated isolation of path2 from path1 is  $28.5$  dB.

### B. Wireless Measurements and EINF

The layout of the antenna array test module is shown in Fig. 21. The distance between two elements on the outer circle is  $2.5$  mm (i.e.,  $\lambda/2$ ). The distance between the central element and any outer element is  $2.88$  mm, slightly optimized for the scan performance. Width of the feeding lines is used for impedance matching, where the vertical via connection in the PCB between the chip and the microstrip line leads to higher impedance.

A vector network analyzer (VNA) is used to measure the S-parameters of the wireless module. One VNA port feeds the central node of the chip using a waveguide transition to the board. The second VNA port is connected to a horn antenna with a nominal gain of  $15$  dBi. A two-port calibration is performed to remove the impact of the coaxial cables that connect the VNA to the waveguide and horn. Since measurements have not been performed in an anechoic environment, time gating is applied on the measured data to remove the impact of multipath reflections from the measurements. This technique is effective against reflections far ( $>10$  cm) from the antenna. Board edge reflections due to surface waves on the antenna module are reduced by a circular absorber placed around the array.

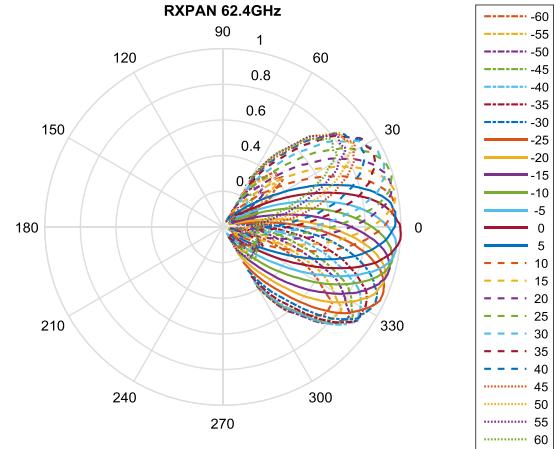


Fig. 22. Measurement of the RX radiation pattern in the PAN direction. Default (uncalibrated) settings are used for the PSs. The legend shows the  $\theta$  steering angle parameter (degrees). The polar plot is proportional to the magnitude of measured S-parameter. Graphs are normalized to the maximum measured value for  $\theta = 0$  in the broadside direction.

The horn antenna is placed at a  $70$  cm distance from the module that is mounted on a scanning Pan/Tilt unit for measurement of the radiation patterns. For absolute measurements, the gain of the antenna is calibrated using the three-horn calibration procedure [12].

The constructive combination of all paths provides  $18$  dB higher gain compared to only a single RX or TX antenna path switched on. This leads to  $26$ -dBm maximum TX EIRP at  $5$ -dB backoff, including antenna feeding loss ( $1.2$  dB) and antenna element gain ( $4.2$  dB). PSs of all antenna paths are programmed to the same setting to form a straight beam. The wireless PS constellation (with all paths on) shows a similar performance to the probed constellation, where mismatches between antenna paths are averaged out. The constellation calibrated circle amplitude errors remain below  $\pm 0.5$  dB with  $0.2$ -dB rms and the phase steps remain below  $5^\circ$  with an average value of  $3^\circ$  at  $\pm 1$  GHz around  $60$  GHz.

As shown in Fig. 21, the antenna patches are placed in a circular configuration to have the same scan performance in both  $E$ - and  $H$ -planes. To steer the beam, the PS setting of each antenna path is programmed according to its  $xy$  coordinates and no calibration is required.

The measured radiation patterns for TX and RX are quite similar. For example, Figs. 22 and 23 show clean radiation patterns, lower than  $12$ -dB sidelobes and nulls below  $-20$  dB for the RX in the  $H$ -plane ( $xz$  plane in Fig. 21). At some angles, the measurements are troubled by the setup, when the scanning unit comes in the way of the horn antenna, causing reflections that dominate the resulting pattern.

Optimum PS settings can be found that maximize the received power for each scan angle. The plot of this maximum TX or RX power versus scan angle is the scan pattern of the phased array (see Fig. 24). Here, the default PS settings have been used. It is seen that the array achieves a  $3$ -dB scan angle of  $\pm 46^\circ$  with less than  $0.4$ -dB peak-to-peak ripples due to the averaging effect of all the antenna paths.

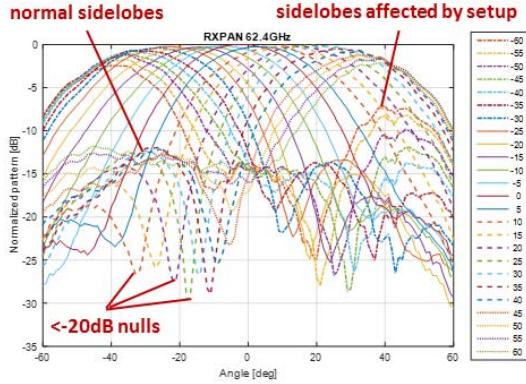


Fig. 23. Radiation patterns of Fig. 22 (decibel scale), revealing sidelobes, and nulls.

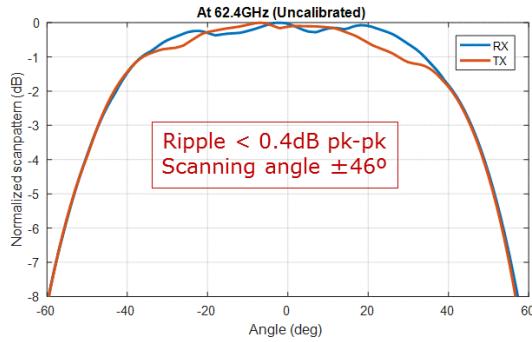


Fig. 24. Scan patterns for RX and TX measured at 62.4 GHz with default PS settings, involving no extra calibration.

The NF is only defined for a two-port network without an antenna. A probed measurement of a single path does not show the correct array performance since a Wilkinson combiner excited from one port only gives extra  $20 \log_{10}(N)$  losses. Therefore, a separate test circuit is often used to assess the single receive path performance. However, this underestimates the total noise in the phased array since the impact of the power combiner and subsequent circuits is ignored by this test measurement. An alternative approach that determines the overall phased-array performance is given in [12] and [13], which introduces the  $G/T$  ratio as a measure for the phased-array noise performance. In this ratio,  $G$  is the overall gain of the phased array and  $T$  is the equivalent output noise temperature.  $G/T$  then corresponds to the inverse of the input-referred noise. We extend this approach by formulating the  $G/T$  ratio as an EINF as follows. We measure the RX module output noise temperature ( $T_{out}$ ) and Gain ( $G_{mod}$ ).  $G_{mod}$  is de-embedded after using the three-antenna gain method to measure the horn antenna gain. Here, we can define an EINF representing the SNR difference before and after the module that can be measured as shown in Fig. 25(a)

$$\text{EINF} = 10 \times \log \left( \frac{T_{out}}{G_{mod}} \times \frac{1}{T_0} \right) \quad (1)$$

where  $T_0$  is the ambient temperature. From [12] and [13], we find EINF

$$\text{EINF} = \text{NF} - 10 \times \log(N) - G_{element} + L_{feed} \quad (2)$$

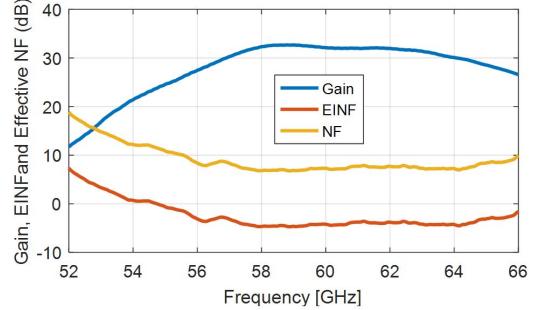
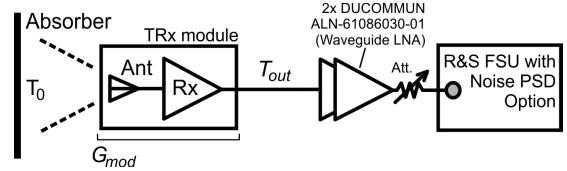


Fig. 25. RX NF measurement setup and result including module gain and EINF.

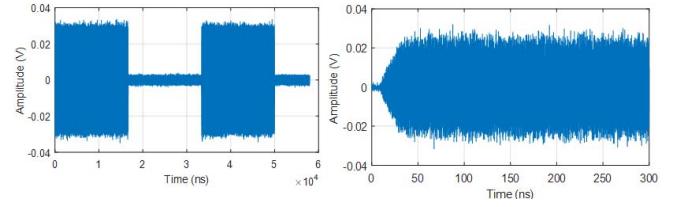


Fig. 26. Measurement of the RX power up time using a 30-kHz control signal for the antenna switch. The right figure is a zoomed-in view of the left figure.

where  $G_{element}$  and  $L_{feed}$  are the antenna element gain and the feeding loss, respectively, extracted from simulations. The minimum EINF [see Fig. 25(b)] is  $-4.7$  dB and the extracted minimum NF is  $6.8$  dB. From (2), it is seen that the EINF is equivalent to the EIRP of a phased-array transmitter. As such, EINF can be used in link budget calculations.

Finally, the speed of switching between transmit and receive is evaluated. The supply switch signal from the schematic in Fig. 4 is excited with an external 30-kHz square-wave signal. A 60-GHz signal generator is used to send a sine wave to the waveguide antenna, and the module output is down converted to 2 GHz. Fig. 26 shows the switching behavior of the RX with a zoomed-in view on the power-up (y-axis not normalized). Clearly, the RX power up time is smaller than 10 ns. A similar power up time for the TX has been measured.

Table I shows a comparison with other 60-GHz phased-array implementations in CMOS, where the TX  $P_{1dBout}$  and RX NF are still at competitive levels without increasing the power budget although using a T/R switch functionality. The RF PS provides the lowest amplitude errors and phase steps making it possible to have beamsteering without calibration. The chip achieves an attractive form factor although using separate passive Wilkinson combiner and splitter. Finally, the wide scan angle is the same in both  $E$ - and  $H$ -planes thanks to the circular array implementation.

TABLE I  
COMPARISON WITH STATE OF THE ART

	[3]	[14]	[4]	[10]	This work
# antenna paths	16	32	1TX,2RX	4	8
beamforming type	RF Passive	RF	RF Active	Analog baseband	RF Active
CMOS tech. (nm)	40	65	65	28	28
Integration	FE, PLL, IF	FE,PLL, IF,BB	FE	FE,PLL, BB	FE
Integ. T/R switch	Yes	No	No	No	Yes
TX P <sub>1dBout</sub> /path (dBm)	5.2 (PA, w/o switch)	9 (PA)	4	>7.5	10
EIRP (dBm)	24 @ -23dB EVM	28 @ -19dB EVM	NA	24 @ -21dB EVM	26 @ 5dB BO
EINF (dB)	NA	NA	NA	NA	-4.7
RX min. NF (dB)	5 (LNA, w/o switch)	<10	<7.2 (5.5 LNA)	4.8	6.8
Gain/path (dB)	TX	33 (PA)	22 (PA)	7.7	32
	RX	31 (LNA)	20 (LNA)	12	62
Pdc (mW)	TX	1190	1820	168	<546
	RX	960	1250	156	431
PS	amplitude error (dB)	NA	NA	±2	<1
	Phase resolution (°)	5.6 <sup>1</sup>	NA	22.5 <sup>1</sup>	<5 <sup>1</sup>
Scan angle (°)	±60 <sup>3</sup>	NA	NA	±45/±30	±46 <sup>4</sup>
Area (mm <sup>2</sup> )	26.3	72.7,77.2	1.6,1.7	7.9	9.6

(1) Average. (2) Maximum.

(3) Only for vertical polarization in H-plane. (4) In both E and H planes.

#### IV. CONCLUSION

A TRX front-end is presented that performs eight-way beamforming in the 60-GHz band. The TX P<sub>1dBout</sub> and RX NF are 10 and 6.8 dB including T/R switching and front-end loading. The NF has been derived from the EINF that has been introduced here to characterize the noise behavior of a phased-array receiver with wireless measurements.

Active RF phase shifting is used with a maximum amplitude error of ±0.35 dB and less than 4.9° phase step for all the settings. The variations remain below 5° and ±0.5 dB when tested at ±1 GHz. The antenna array achieves ±46° scan angle in both *E*- and *H*-planes thanks to the circular implementation. The scan pattern gain ripples are less than 0.4-dB peak-to-peak using PS default settings, showing no need for calibration to steer the beam.

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