A 12-bit 150-MS/s Sub-Radix-3 SAR ADC With Switching Miller Capacitance Reduction

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***Abstract*— This paper presents a 0.9-V 1.5-mW 150-MS/s 12-bit successive-approximation-register analog-to-digital converter (SAR ADC) in 40-nm CMOS, which achieves a synergistic integration of multi-bit per cycle (M-bit/cycle) and sub-radix techniques with the comprehensive enhancement of speed and error tolerance. The proposed sub-radix-3 architecture uses a merged digital-to-analog converter (DAC) with a two-input comparator instead of the conventional separated DACs (signal and reference DACs) with a four-input comparator to effectively improve the matching performance and the power efficiency. Alternative-reference-switching (ARS) DACs are developed to reduce the total DAC effective switching capacitance by 47.4%. Offset injection technique is implemented to calibrate the comparator offset without the speed and power penalty by eliminating the additional output loading of capacitor array or the extra input pair. The SAR logic of each conversion cycle is simplified into one single tri-latch current mode logic (CML) to directly control the DAC switches which effectively reduces the SAR delay by 2/3. The achieved peak signal to noise and distortion ratio (SNDR), spurious-free dynamic range (SFDR), and Walden FoM are 61.7 dB, 74.4 dB, and 10.3-fJ/conversion-step, respectively.**

***Index Terms*— Analog-to-digital (A-to-D), multi-bit per cycle (M-bit/cycle), quantization, redundancy, sub-radix, successive-approximation-register analog-to-digital converter (SAR ADC).**

I. Introduction

With the increasing device speed and matching property in the advanced CMOS technology, successive-approximation-register analog-to-digital converter (SAR ADC) has become a competitive architecture in high-speed (10–100 MS/s) and medium-resolution (10–12 bit) applications [1]. However, when the speed exceeds 100 MS/s and 12-bit resolution, SAR ADC suffers from the penalties of the serial bit-cycling conversion, less digital-to-analog converter (DAC) settling time, and severe comparator noise requirement. For high-speed 12-bit applications, the recently reported works illustrate the design trend of using hybrid architectures such as pipelined-SAR ADCs [2]–[8] and two-step ADCs [9]–[12]. Pipelined-SAR ADC improves the analog-to-digital (A-to-D) conversion throughput and relaxes the noise requirement of the afterward conversions with the residue amplification at the cost of huge power consumption on the residue amplifier. Two-step ADC optimizes the design tradeoff (power and noise) for the coarse and fine A-to-D conversions based on the corresponding performance requirement. However, the additional complicated calibrations are required for the mismatch compensation and the weight alignment between the coarse and fine ADCs.

Among the Nyquist-rate ADCs, SAR ADC has the architectural advantage of low complexity and energy efficiency. Thus, to push the conversion rate of SAR ADC to be compatible with pipelined-SAR and two-step ADCs becomes the primary target in this paper. To enhance the conversion rate of SAR ADC, there are two commonly used techniques. One is the architecture of multi-bit per cycle (M-bit/cycle) which saves the number of conversion cycles in a signal acquisition at the expense of hardware complexity [13], [14]. The other one is sub-radix or non-binary searching algorithm adopted on the DAC which creates redundancies to release the required DAC settling time with the tolerance of settling error and false comparison due to offset, noise, meta-stability, and mismatch of quantization thresholds [14], [15].

Our previous work [16] provides a hybrid A-to-D conversion algorithm and design methodology for the pure SAR architecture to overcome the speed limitation. Following the design procedure with the hardware-like parameters at 40-nm process node as in [16], this paper [17] proposes a SAR ADC which integrates the speed-up techniques of M-bit/cycle and sub-radix with a comprehensive enhancement of speed and error tolerance. The accuracy requirement of the multi-comparator operation is covered by the implemented speed-optimized error-tolerant redundancy and foreground offset calibration. Moreover, the proposed sub-radix-3 architecture uses a merged DAC with a two-input comparator instead of the conventional separated DACs (signal and reference DACs) with a four-input comparator to effectively improve the matching performance and power efficiency [13], [14]. The alternative-reference-switching (ARS) DACs are developed to reduce the effective switching capacitance. The reconfigurable-noise-level (RNL) comparators [18] are adopted to improve speed and power consumption by reconfiguring the comparators in different noise levels in cooperation with the redundancies of the sub-radix algorithm. The SAR logic of each conversion cycle is simplified into one single tri-latch current mode logic (CML) to directly control the DAC switches which effectively reduces the SAR delay by 2/3.

This paper is organized as follows. Section II introduces the proposed ADC architecture and operation. Section III introduces the operations of the speed-up and power efficient

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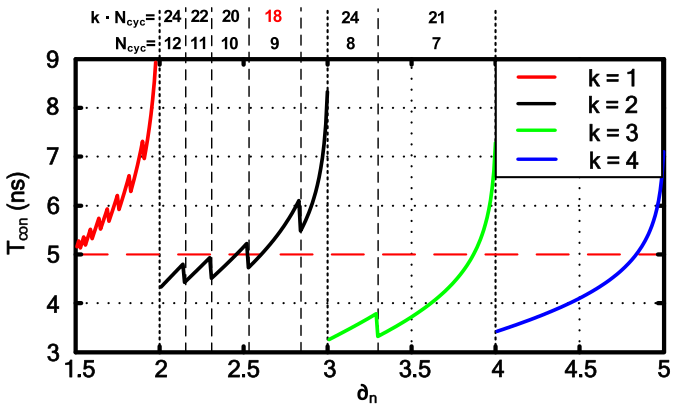


Fig. 1. HSPICE simulation results of ADC conversion time to achieve 12-bit resolution with the SAR logic delay $T_{\mathrm{SAR}} = 200$ ps and DAC switching time constant $\tau = 120$ ps.

techniques and the circuit implementations of the key building blocks in detail. Section IV shows the measurement results, and the conclusions are provided in Section V.

II. Parameters and Architecture

The proposed SAR ADC implementation is based on the constraints, guidelines, and tradeoff provided by the previous proposed A-to-D algorithm [16]. Using the step-by-step design procedure and the corresponding parameters at 40-nm process node, this paper realizes the optimal and efficient architecture with the consistency confirmation of MATLAB and HSPICE simulations.

A. Design Parameters

Fig. 1 shows the simulation results of a 12-bit SAR ADC using the hybrid A-to-D conversion algorithm and design procedure proposed in [16]. The plot illustrates the A-to-D conversion time T_{con} of SAR ADC versus radix ∂_n, where k indicates the number of quantization thresholds (comparators) and N_{cyc} indicates the number of conversion cycles. The parameters including DAC switching time constant $\tau = 120$ ps and the SAR logic delay $T_{\mathrm{SAR}} = 200$ ps are used for the simulation based on the provided information at the target 40-nm process node.

The discontinuities (bending points) in the conversion time (T_{con}) curves result from two main causes. Within the same number of quantization thresholds (k), the discontinuity is due to the integer number of conversion cycles (N_{cyc}) which discretizes T_{con} curves as N_{cyc} increases. The discontinuities at the integer radixes (∂_n) between two adjacent k values are caused by the dramatic change of the redundancy range (e.g., $k = 4$ has the largest redundancy range at radix -3 while $k = 3$ has no redundancy at radix -3).

The proposed SAR ADC aims at the sampling rate of 150 MS/s with a 25% sampling duty and the resulting maximum allowable A-to-D conversion time (T_{con}) of 5 ns (red dashed line).

Since the implementation complexity (the required number of comparators, reference DACs, DAC switches, and SAR logic) is proportional to the product of the number of quantizations per cycle (k) and the total number of conversion cycles (N_{cyc}), the lowest ($k \times N_{\mathrm{cyc}}$) means the most power and area efficient design under the target conversion speed. As shown in Fig. 1, to accomplish a SAR conversion within 5 ns, the optimal average radix is in the region of $k = 2$ (two comparators/cycle) and $N_{\mathrm{cyc}} = 9$ (nine conversion cycles) where $k \times N_{\mathrm{cyc}} = 18$.

B. ADC Architecture

Fig. 2 shows the proposed ADC architecture which is composed of two two-input comparators and two differential DAC arrays (upper and lower networks). Each DAC network consists of two 9-bit main DACs (P+/N+ and P−/N−) with adaptive radix to perform the top-plate voltage shifts and comparator's reference generations for M-bit/cycle operation, and two corresponding 9-bit binary calibration DACs (cal. DACs) to calibrate the offset mismatch between the comparators. Both main DAC and cal. DAC share the same top plate in each DAC network to match the capacitor ratio with the identical unit capacitor (weight).

Other than the conventional M-bit/cycle architecture [13], [14] with the extra reference generation DACs which are typically implemented by using the resistor ladder or charge redistribution capacitor array, the reference and signal DACs are merged together to share the top plate as one single DAC (main DAC) in this paper. The proposed merged main DAC omits the commonly required extra reference DACs and differential-difference (four-input) comparator [19], [20] to achieve a better matching performance and power efficiency.

The weights for both top-plate voltage shifts and comparator's reference generations are implicitly matched in the merged main DAC since they are generated from the identical capacitor rather than the different capacitors on the different DACs. Moreover, using the two-input comparator instead of the conventional differential-difference (four-input) comparator effectively omit the offset variation from the mismatch of the extra input pair.

Since the total switching capacitance of the merged DAC is only half of the separated DACs (assumed both signal and reference DACs are *kT/C* noise limited), the switching energy consumption of the merged DAC is less than that of the separated signal and reference DACs. Surely, the required power consumption of the reference generator is also reduced due to the less capacitance loading. Hence, in all aspects, the merged DAC surely achieves the improved power efficiency. Compared to the four-input comparator having the same trans-conductance (G_m) on both reference and signal input pairs, the implemented two-input comparator consumes only half of the power dissipation by using a single input pair to differentiate the signal riding on the reference. Thus, the proposed merged DAC and two-input comparator is more power efficient than the conventional separated DACs and four-input comparators.

To maintain a consistent comparator speed and power, the offset mismatch between the comparators is calibrated by injecting the corresponding amounts of the offsets from the cal. DAC instead of adding the capacitance loading

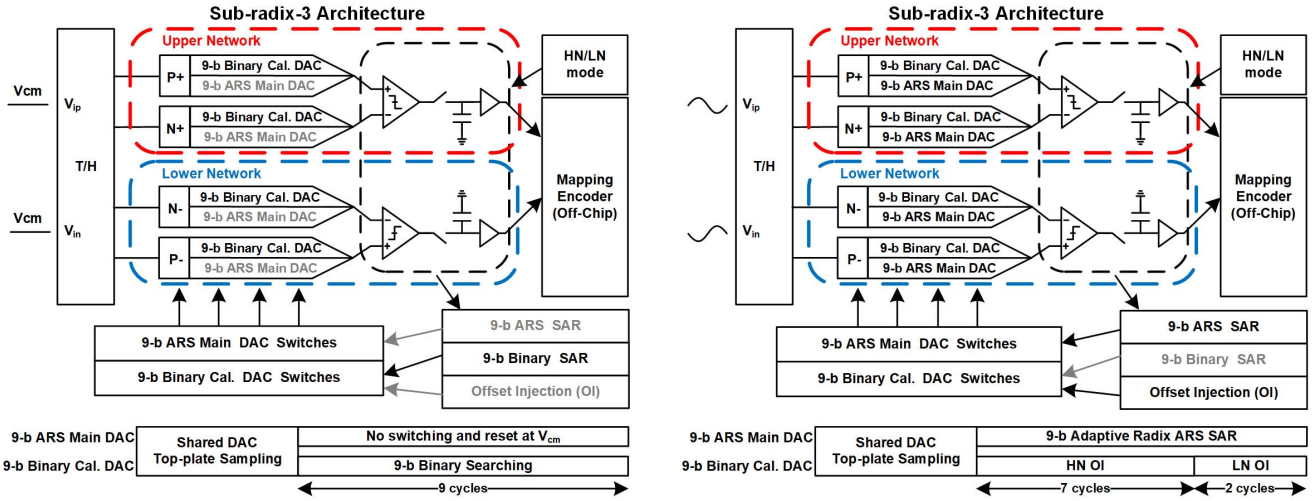


Fig. 2. Architecture and operation of the proposed SAR ADC in (a) foreground offset calibration mode and (b) normal operation mode.

(typically implemented by a capacitor bank) at the comparator outputs or the extra input pair for offset adjustment [21]. The radixes of the main DACs are designed and optimized for the adaptive error tolerance from the precedent (MSB) to the subsequent (LSB) conversions. The resultant 12-bit A-to-D conversion is completed in nine cycles with an equivalent 1.33 bit/cycle and radix -2.52 ($2^{12/9}$) operation in a viewpoint of the effective radix per cycle with two quantization thresholds ($k = 2$). The 18-bit (9 conversion cycles $\times$ 2 bits/cycle) output codes are then remapped to the binary codes as the 12-bit binary codes through the off-chip mapping encoder.

C. Operation of Reconfigurable-Noise-Level Comparators

For 12-bit resolution applications, the power consumption of the comparator is considerable to meet the rigorous noise and speed requirement. However, the comparator noise can be considered as a dynamic error source during the SAR conversion, in other words, it only affects the current quantization result rather than the following quantization results. As long as the comparator noise is less than the redundancy of sub-radix architecture, the noise induced error is tolerable and recoverable. Therefore, with the redundancies in the precedent conversions, the noise requirement of the comparators is released. The RNL operation is developed for the power saving by switching the comparators to the different precisions (noise levels) according to the corresponding redundancy.

The RNL operation is described as follows. The comparators are designed to operate in the high-noise (HN) mode (without bypass capacitance at outputs) which are fast, power efficient, but noisy in the first seven cycles with the large redundancies. Then, the comparators are switched to the low-noise (LN) mode (with bypass capacitance at outputs) which are slow, accurate, but power hungry in the last two cycles with no redundancies. By enabling the RNL operation, the simulated comparator power and speed in an A-to-D conversion are improved by 37.3% and 36.6%, respectively.

D. Foreground Offset Calibration

In the architecture of M-bit/cycle, it is necessary to calibrate the offset mismatches among the comparators that directly induce the non-linearity. In this paper, a foreground offset calibration is implemented to calibrate the offset mismatch between the upper and lower comparators. The A-to-D operation starts from two times of the foreground calibration in both HN and LN modes as depicted in Fig. 2(a). With the top plate sampled identical input $V_{\rm cm}$ by the differential T/Hs, the proposed ADC performs a 9-bit binary searching through the cal. DACs (full range of 128 LSB and resolution of 0.5 LSB) to track the comparator offsets in both HN and LN modes for both upper and lower networks, respectively. The differential 9-bit binary weighted cal. DACs are implemented from 64 $C_{\rm unit}$ to 0.5 $C_{\rm unit}$ (with one-side switching of 0.5 $C_{\rm unit}$ for the LSB switching) corresponding to the unit capacitance of the main DACs, which covers a 2.5-sigma distribution of the comparator offsets with the PVT variation (0.81–0.99 V, -20 °C–120 °C) in a resolution of 0.5 LSB. The total stored offset codes are four sets of 9-bit codes (2 comparators $\times$ 2 modes).

In the normal operation mode as depicted in Fig. 2(b), with the stored offset calibration codes, the top plate sampled signals ($V_{\rm ip}$ and $V_{\rm in}$) are converted through the main DACs with the ARS operation which will be introduced in detail in Section III-A. In the meantime, the offsets of the comparators are calibrated by the HN and LN offsets injection (OI) through the cal. DACs at the corresponding cycles (cycle 1 for HN offsets and cycle 8 for LN offsets).

E. DAC Radix Arrangement

Fig. 3 and Table I illustrate the radix arrangement and the corresponding redundancy of the main DAC implemented by the integer numbers of unit capacitor (0.5 fF). Compared to the fractional implementation, the integer arrangement has the better matching property, less digital processing complexity (without the extra floating point operation), and less

TABLE I
PARAMETERS OF SUB-RADIX DAC ARRANGEMENT

	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9
Capacitor Ratio (C_{unit})	**1142**	**511**	**224**	**101**	**42**	**17**	**7**	**3**	**1**
Radix	**2.26**	**2.29**	**2.31**	**2.43**	**2.47**	**2.48**	**2.56**	**3**	**3**
Redundancy (LSB)	**670**	**279**	**118**	**39**	**14**	**5**	**1**	**0**	**0**
Tolerance (%)	**29.3**	**27.3**	**26.3**	**19.3**	**166.7**	**14.7**	**7.1**	**0**	**0**

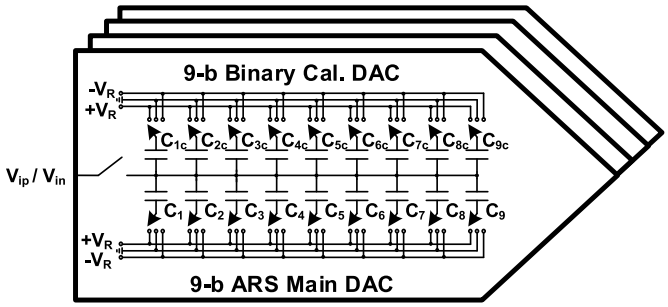


Fig. 3. Top plate shared 9-bit ARS main DAC and 9-bit binary cal. DAC.

power consumption in the mapping encoder. Since the settling requirement of the DAC switching is more critical in the precedent (MSB) portion due to its larger capacitance and parasitic loading, the radixes are increased from the precedent (MSB) to the subsequent (LSB) conversions (instead of using a fixed radix value) with an average value $\partial_n = 2.52$. The radix arrangement provides the resultant redundancies of 670, 279, and 118–1 LSB with the corresponding error tolerance ratios of 29.3%, 27.3%, and 26.3%–7.1% in the first seven cycles. The mapping equation of the mapping encoder is

$$W[n+1] = W[n] + D[n] \cdot C_n \tag{1}$$

where $W[1]$ is equal to 0, n denotes the order of conversion cycle, $D[n]$ is equal to $+2$ at code 11, $+1$ at code 01/10, 0 at code 00, and C_n is the capacitor ratio as depicted in Table I.

III. IMPLEMENTATION OF SAR ADC

A. Alternative-Reference-Switching DACs

Fig. 4 shows a two-cycle example with and without the ARS operation. For simplicity, take the case of $V_{\text{ip}} - V_{\text{in}} > V_{t1}$ as an example, where V_{t1} denotes the quantization thresholds in the MSB conversion. In this section, the cal. DACs are excluded for simplicity, since the cal. DACs only operate for the offset injection which is irrelevant to the SAR conversion. At the sampling phase, the differential input signals are sampled on the top plates of the upper and lower DACs (1.6 pF for each DAC) simultaneously. In the MSB conversion, the required voltage shifts ($\pm V_{t1}$) as the quantization thresholds of both comparators are generated by one-side switching the corresponding capacitor C_n's in P+ and P− DACs. After each cycle, the 2-bit comparator's output code (11, 01/10, and 00) decides the following DAC switching operation based on the SAR logic operation. In the MSB-1 conversion, C_n's and C_{n-1}'s in all DACs are switched according to the MSB results to create the next reference quantization thresholds ($\pm V_{t2}$) for the MSB-1 conversion.

However, in the case without the ARS operation, the two adjacent capacitors C_n and C_{n-1} in P− DAC are switched to the opposite reference voltages ($+V_R$ and $-V_R$) which equivalently creates a Miller capacitance with the additional switching load, more power consumption, and degraded speed. The proposed ARS operation switches the two adjacent capacitors C_n and C_{n-1} in the P− DAC to the identical reference voltage ($-V_R$) instead of the opposite ones ($+V_R$ and $-V_R$) to eliminate the induced Miller capacitance.

Fig. 5 shows the modeling and the effective switching capacitance (C_{eq}) reduction ratio (RR) with the ARS operation. Take the MSB conversion as an example, the DAC array is shown as a Y-configuration, where C_n and C_{n-1} are the switched capacitors (by V_A and V_B) and C_R is the summation of the rest un-switched capacitors (from C_{n-2} to C_0). For the analysis purpose, the Y-configuration DAC is transformed to Δ-configuration, where

$$C_a = \frac{C_n \times C_R}{C_n + C_{n-1} + C_R} \tag{2}$$

$$C_b = \frac{C_n \times C_{n-1}}{C_n + C_{n-1} + C_R} \quad \text{(Miller capacitor)} \tag{3}$$

$$C_c = \frac{C_n \times C_{n-1}}{C_n + C_{n-1} + C_R}. \tag{4}$$

In the case without the ARS operation, V_A and V_B are switched to the opposite directions with the same amount of the voltage shift that equivalently sees a Miller capacitor of $2C_b$ at both terminals (V_A and V_B) during the switching. Note that the coefficient of C_b (in this case is 2) depends on the voltage shift difference between V_A and V_B, and the effective switching capacitances at V_A and V_B are derived and normalized to V_R as shown in the following equations, respectively. On the contrary, in the case with the ARS operation, V_A and V_B are switched to the identical direction with the same amount of the voltage shift, where the Miller capacitance is vanished and equivalently the coefficient of C_b becomes 0

$$C_{\text{eff},A} = \frac{|\Delta V_A|}{V_R} \cdot \left(C_a + \frac{\Delta V_A - \Delta V_B}{\Delta V_A} \cdot C_b \right) \tag{5}$$

$$C_{\text{eff},B} = \frac{|\Delta V_B|}{V_R} \cdot \left(C_c + \frac{\Delta V_B - \Delta V_A}{\Delta V_B} \cdot C_b \right). \tag{6}$$

Hence, the ARS operation swaps the purposes of the P+ and P− DACs and also the upper and lower networks without

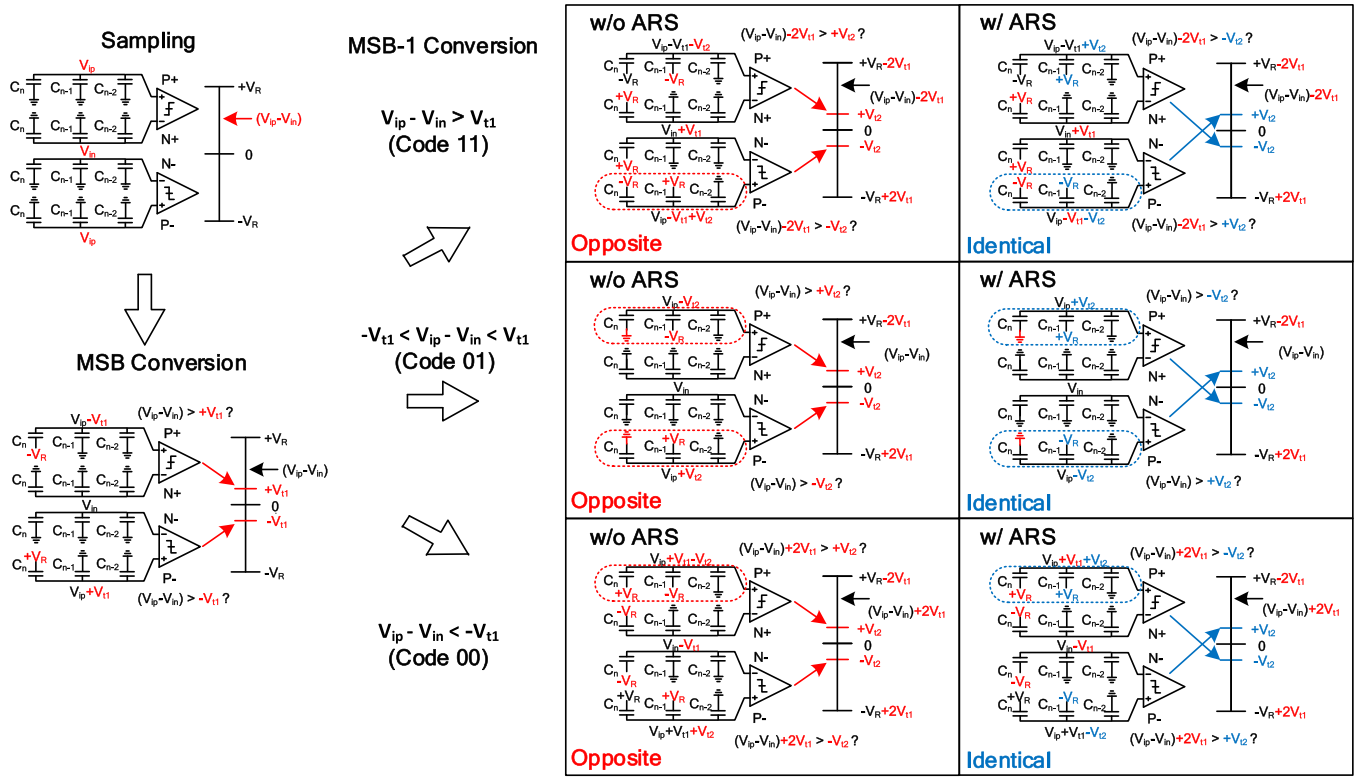


Fig. 4. Two-cycle example of the proposed ARS DAC operation.

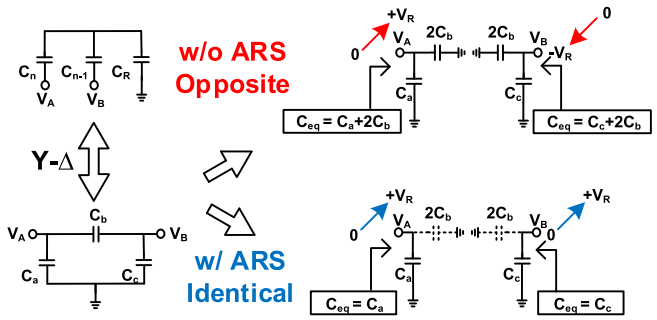


Fig. 5. Equivalent model of the effective switching capacitance with and without the ARS operation.

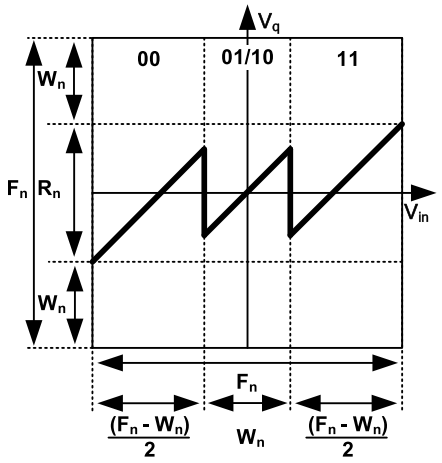


Fig. 6. V_{in}–V_q transfer curve of $k = 2$ A-to-D conversion.

the extra effort by only slightly modifying the SAR logic (as depicted in Section III-C). In the case of $V_{\text{ip}} - V_{\text{in}} > V_{t1}$ (code 11), the Miller capacitance induced by C_n and C_{n-1} in the $P-$DAC is eliminated. In the case of $-V_{t1} < V_{\text{ip}} - V_{\text{in}} < V_{t1}$ (code 01), the Miller capacitances induced by C_n's and C_{n-1}'s in both P− and P+ DACs are eliminated. In the case of $V_{\text{ip}} - V_{\text{in}} < -V_{t1}$ (code 00), the Miller capacitance induced by C_n and C_{n-1} in the P+ DAC is eliminated. The comparison of the resulting effective capacitance with and without the ARS operation is depicted in Table II.

To calculate the average RR of the effective switching capacitance with the ARS operation, Fig. 6 illustrates the parameters defined in [16] and the $V_{\text{in}} - V_q$ (input-to-residue) transfer curve with a $k = 2$ A-to-D conversion. Assumed the input signal (in the MSB conversion) or residue (from the MSB-1 to the LSB conversion) is uniformly distributed in the voltage amplitude (V_{in} in x-axis), the occurrence rate (P_{11}, $P_{01/10}$, and P_{00}) of each input range (00, 01/10, and 11) is defined by the proportion of each input range to the full range as shown in the following equations:

$$P_{11,n} = P_{00,n} = \frac{\left(\frac{F_n - W_n}{2}\right)}{F_n} = \frac{\frac{1}{2}\left(\sum_{i=1}^{n} C_i - C_n\right)}{\sum_{i=1}^{n} C_i} \quad (7)$$

$$P_{01/10,n} = \frac{W_n}{F_n} = \frac{C_n}{\sum_{i=1}^{n} C_i} \quad (8)$$

where n denotes the nth conversion, and F_n and W_n represent the full range and weight in the nth conversion, respectively.

TABLE II
COMPARISON OF THE EFFECTIVE SWITCHING CAPACITANCE

w/o ARS	N- / N+ DACs		P- DAC		P+ DAC		
Code	$C_{eff,A}$	$C_{eff,B}$	$C_{eff,A}$	$C_{eff,B}$	$C_{eff,A}$	$C_{eff,B}$	$C_{tot,code}$
11	C_a+C_b	0	$2(C_a+3C_b/2)$	C_c+3C_b	0	C_c+C_b	$4C_a+9C_b+C_c$
01/10	0	0	C_a+2C_b	C_c+2C_b	C_a+2C_b	C_c+2C_b	$2C_a+4C_b+2C_c$
00	C_a+C_b	0	0	C_c+C_b	$2(C_a+3C_b/2)$	C_c+3C_b	$4C_a+9C_b+C_c$
w/ ARS	N- / N+ DACs		P- DAC		P+ DAC		
Code	$C_{eff,A}$	$C_{eff,B}$	$C_{eff,A}$	$C_{eff,B}$	$C_{eff,A}$	$C_{eff,B}$	$C_{tot,code}$
11	C_a+C_b	0	$2(C_a+C_b/2)$	C_c-C_b	0	C_c+C_b	$4C_a+3C_b+C_c$
01/10	0	0	C_a	C_c	C_a	C_c	$2C_a+2C_c$
00	C_a+C_b	0	0	C_c+C_b	$2(C_a+C_b/2)$	C_c-C_b	$4C_a+3C_b+C_c$

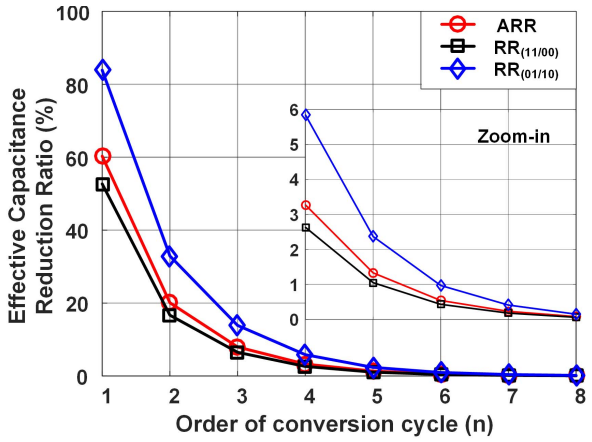


Fig. 7. Plot of the effective capacitance RR in each conversion cycle.

The capacitance RR of each code $(\mathrm{RR})_{\mathrm{code}}$ is the normalized number of the total effective switching capacitance difference in each code ($C_{\mathrm{tot,\,code}}$) with and without the ARS operation in Table II as

$$(\mathrm{RR})_{\mathrm{code}} = \frac{C_{\mathrm{tot,code}(w/o\ \mathrm{ARS})} - C_{\mathrm{tot,code}(w/i\ \mathrm{ARS})}}{C_{\mathrm{tot,code}(w/o\ \mathrm{ARS})}}. \quad (9)$$

By substituting the corresponding DAC capacitor in the nth conversion (C_n, C_{n-1}, and C_R) as depicted in Table I into the effective switching capacitors (C_a, C_b, and C_c) as derived in (2)–(4), the numerical value of the capacitance RR in each code in the nth conversion $(\mathrm{RR})_{\mathrm{code,\,n}}$ is obtained. Hence, the average reduction ratio (ARR) of the effective switching capacitance in the nth conversion $(\mathrm{ARR})_n$ is obtained as

$$(\mathrm{ARR})_n = \sum_{\substack{\mathrm{code}= \\ 00,01/10,11}} P_{\mathrm{code},n} \times (\mathrm{RR})_{\mathrm{code,n}}. \quad (10)$$

Fig. 7 shows the corresponding parameters as mentioned in (9) and (10). The ARR from the MSB to the MSB-7 conversions are 60.31%, 20.08% to 0.08%, and a resultant average of 41.96% per A-to-D conversion, which efficiently reduces the DAC settling time and power dissipation.

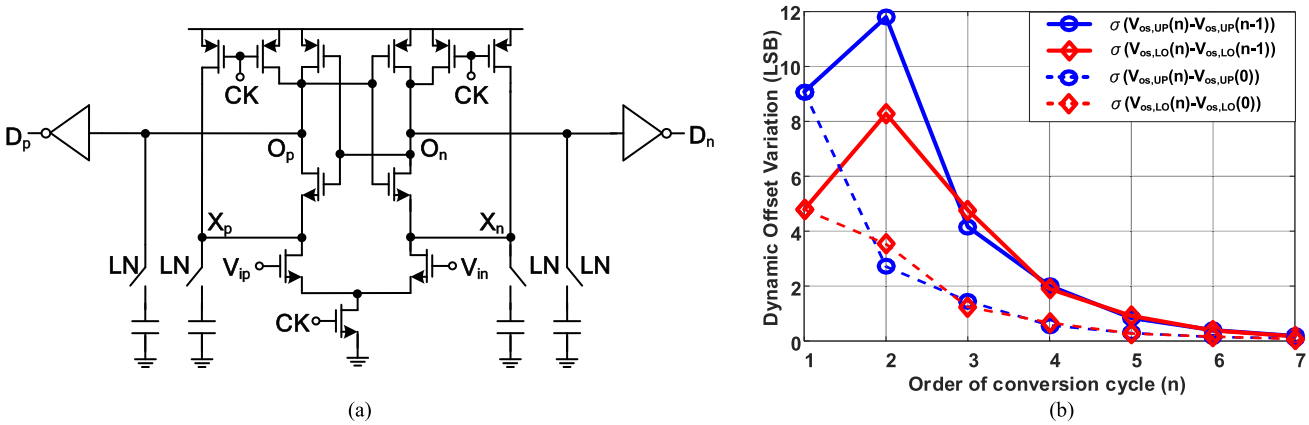
B. Reconfigurable-Noise-Level Comparators

Fig. 8(a) shows the implemented reconfigurable comparators in the HN and LN modes to achieve the RNL operation. The strong-arm dynamic comparator [22] is adopted for the fast decision and no dc power consumption. In the HN mode, the bypassing capacitors are disconnected for the high bandwidth (fast decision) but noisy (less power dissipation) operation to meet the speed and power requirements. In the LN mode, 30-fF capacitance loadings are added to the nodes O_p, O_n and X_p, X_n for the noise reduction at the cost of speed and power. The simulated input-referred noises in the HN and LN modes are 1-sigma of 0.83 and 0.36 LSB, respectively. With the RNL technique, the speed and power are improved by 47.1% and 48.6% compared to the conventional approach (only LN comparator for all bit-conversion cycles), respectively.

Since the ARS operation will introduce the common-mode shifts during the conversion cycles, the dynamic offsets induced by the common-mode shifts should be taken into consideration. Fig. 8(b) shows the variations of the dynamic offset (1-sigma) of the HN comparators in each conversion cycle. The variations of the dynamic offsets of the LN comparators are neglectable since the amounts of the common-mode shift are very small in the last two conversion cycles. The dynamic offset variations (dotted lines) for the upper and lower comparators both show the worst conditions (mismatch) in the MSB-1 conversion ($n = 1$) due to the largest common-mode shift. The offset mismatch variation between two adjacent conversion cycles defined by $\sigma(V_{\mathrm{os}}(n) - V_{\mathrm{os}}(n-1))$ is expressed in solid lines. The redundancies provided by sub-radix arrangement should cover the worst $\sigma(V_{\mathrm{os}}(n) - V_{\mathrm{os}}(n-1))$ in each conversion cycle to avoid the un-recoverable false conversion. By employing the radix arrangement as depicted in Table I, the simulation shows that a 3-sigma variation of the offset mismatch $(V_{\mathrm{os}}(n) - V_{\mathrm{os}}(n-1))$ in each cycle is tolerated within the implemented redundancies.

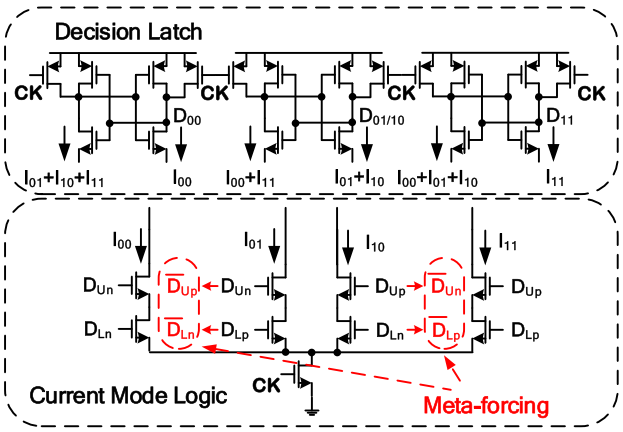
C. Tri-Latch CML With Meta-Stability Forcing

The tri-latch logic as depicted in Fig. 9 is proposed to shorten the conversion time by simplifying the complex SAR



(a) (b)

Fig. 8. (a) RNL comparator. (b) Variations of the dynamic offset versus conversion cycle due to the input common-mode shift.



Boolean		Comparator Ouputs				Latch Ouputs		
		D_{Up}	D_{Un}	D_{Lp}	D_{Ln}	D_{00}	$D_{01/10}$	D_{11}
Normal	00	0	1	0	1	1	0	0
	01	0	1	1	0	0	1	0
	10	1	0	0	1	0	1	0
	11	1	0	1	0	0	0	1
Meta-stability	X1	0	0	1	0	X→0	X→1	X→0
	X0	0	0	0	1	X→0	X→1	X→0
	1X	1	0	0	0	X→0	X→1	X→0
	0X	0	1	0	0	X→0	X→1	X→0
	XX	0	0	0	0	X→0	X→1	X→0

Fig. 9. Tri-latch CML with meta-stability forcing.

logic into a single CML without cascading gate logics and clocked D flip-flops (DFFs), which effectively reduces the SAR logic delay T_{SAR} by 2/3 (from 300 to 200 ps). The tri-latch logic is composed of three decision latches controlled by the CML. By applying the Boolean operations (truth table in Fig. 9) with respect to the comparator outputs in the CML, only one branch (I_{00}, I_{01}, I_{10}, or I_{11}) will conduct the current at a time while the other branches remain OFF. Thus, only one output of the decision latches (D_{00}, $D_{01/10}$, or D_{11}) will be 1 (while the others are 0's) which directly controls the DAC switches to one of three states (codes 00, 01/10, and 11) without the additional logic gates.

Moreover, the meta-stability forcing mechanism is also implemented. If the meta-stability occurs when the comparator

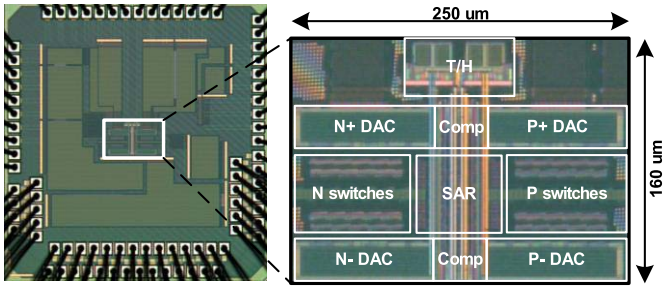


Fig. 10. Chip micrograph.

input difference is too small to generate a quantized (digitized) output within a certain time window, the comparator outputs would remain at the reset level (0) to turn off all the current branches ($I_{00} \sim I_{11}$) in the CML and result in an unknown latch output and a failed SAR decision. To avoid the logic failure in the meta-stability condition, the gate controls of the current branches I_{01} and I_{10} are replaced by the inverted complementary comparator outputs (i.e., D_{Up} to $\sim D_{Un}$ and so on) to force the comparison results to 01/10 by turning on the current branches I_{01} and I_{10}, which has the least effective switching capacitance (code 01/10 in Table II) for speed and power efficiency.

IV. Measurement Results

Fig. 10 shows the prototype chip fabricated in 1P9M 40-nm CMOS occupying an active area of 0.04 mm^2 (160 × 250 μm^2). Fig. 11 shows the dynamic performances (64× down sampled) of the implemented ADC. With a 0.9-V supply voltage, the prototyped SAR ADC consumes a total power of 1.5 mW at 150-MS/s sampling rate, where the analog, DAC reference, and digital parts (including the buffers to drive DAC switches) consume 0.28 (18.67%), 0.23 (15.06%), and 0.99 mW (66.27%), respectively. The measured signal to noise and distortion ratio (SNDR), SNR, and spurious-free dynamic range (SFDR) at 1-MHz input frequency are 61.7, 62.2, and 74.4 dB, respectively. Fig. 12 shows the SFDR, SNR, and SNDR versus input frequency (F_{in}) at 150-MS/s sampling frequency. The dynamic performance degradation at

TABLE III
COMPARISON TABLE OF THE STATE-OF-THE-ART ADCS

	[25] Tseng, JSSC 2016		[8] Lin, TCASI 2016	[4] Hong, JSSC 2015	[9] Zhou, JSSC 2015	[10]Mathew, VLSI 2015	[26] Tsai, JSSC 2015	This work
Architecture	SAR		Pipelined-SAR (2-ch)	Pipelined	Two-step SAR	Flash-TDC SAR	SAR	SAR
Technology	28 nm		65 nm	65 nm	40 nm	45 nm	28 nm	40 nm
Supply Voltage	1.2V/1.1V		1.0 V	1.2 V	1.1 V	0.85 V	1.0 V	0.9 V
Resolution	12 bit		12 bit	12 bit	12 bit	12 bit	10 bit	12 bit
Sampling Rate	104 MS/s		210 MS/s	250 MS/s	160 MS/s	200 MS/s	240 MS/s	150 MS/s
SNDR @ peak (dB)	60.5*	63**	63.4	67.0	66.5	68.5	57.1	61.7
SFDR @ peak (dB)	76*	N/A**	77.5	84.6	85.9	N/A	73	74.4
SNDR @ Nyq (dB)	45*	N/A**	60.1	65.7	65.3	68.0	53	56.2
SFDR @ Nyq (dB)	52*	N/A**	74.8	79.0	86.9	N/A	63	63.5
DNL (LSB)	< 0.5		-0.57 / +0.66	-0.86 / +0.52	N/A	-0.60 / +0.40	+0.45 / -0.23	-0.91 / +1.77
INL (LSB)	< 1.1		-0.68 / +1.45	-0.90 / +1.08	N/A	-0.90 / +0.80	+0.55 / -0.45	-2.63 / +2.95
Power (mW)	3.06*	0.88**	49.7	5.3	4.96	3.4	0.68	1.5
FoM_w @ peak (fJ/conv.-step)	34*	7.3**	20.9	108.5	17.7	7.9	4.8	10.3
FoM_w @ Nyq (fJ/conv.-step)	203*	N/A**	30.3	126.8	20.7	8	7.8	18.9
Core Area (mm^2)	* 0.024	** 0.003	0.594	0.48	0.042	0.06	0.003	0.04

* : ADC+Ref+Buf
** : ADC only

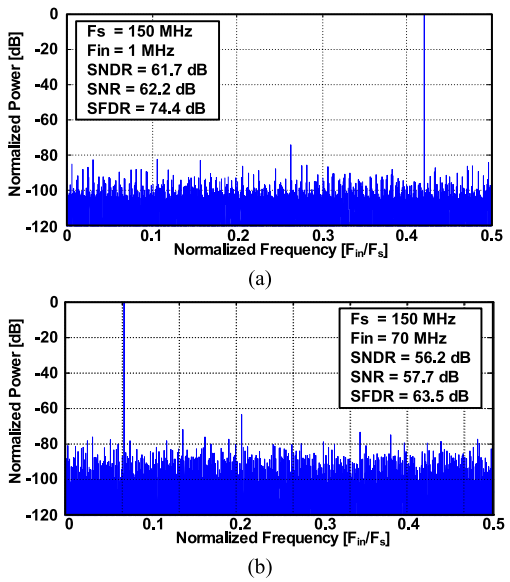


Fig. 11. Dynamic performances of (a) $F_{in} = 1$ MHz and (b) $F_{in} = 70$ MHz at 150 MS/s sampling frequency.

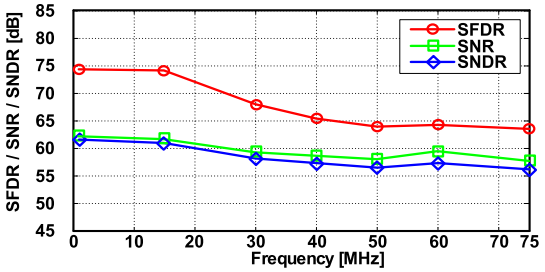


Fig. 12. SFDR, SNR, and SNDR versus input frequency (F_{in}) at 150 MS/s.

the Nyquist input is due to the degraded signal integrity of the un-buffered ADC input, which suffers from the high-frequency inductive ringing effect and clock jitter.

Fig. 13 shows the measured static performances of the implemented ADC. The differential non-linearity (DNL) and integral non-linearity (INL) peaks are −0.91/+1.77 LSB and −2.63/+2.95 LSB, respectively. Fig. 14 shows the measured DNL distribution with a standard deviation (1-sigma) of 0.42 LSB. To clarify the root cause of the degraded DNL performance, Fig. 15 shows the simulated statistical box plots of the standard deviation of the DNL (σ-DNL) in 1000 samples (without kT/C noise and comparator noise) with two non-ideal effects. One is simulated with the DAC mismatch $\sigma(\Delta C_{unit}/C_{unit}) = 1\%$ only (according to [23] and [24] in 0.5-fF C_{unit}). The other one is simulated with the comparator offset only and using the calibration DAC resolution of 0.5 LSB. It shows the median value of the σ-DNL with the comparator offset (0.53 LSB) is more consistent with the measured result (0.42 LSB).

Therefore, the degraded static performance is mainly due to the not-fine-enough offset calibration resolution

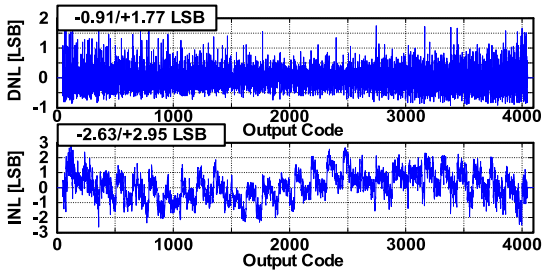


Fig. 13. Static performances.

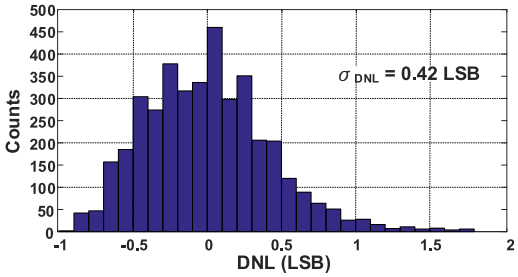


Fig. 14. Measured DNL distribution.

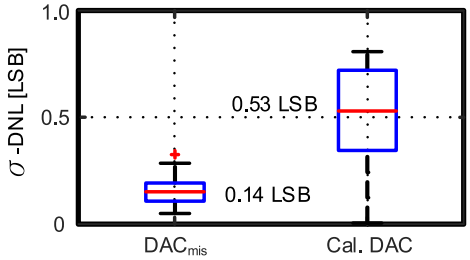


Fig. 15. Statistical box-plots of the standard deviation of DNL with the DAC mismatch $\sigma(\Delta C_{\text{unit}}/C_{\text{unit}}) = 1\%$ only, and with the calibrated comparator offsets with 0.5 LSB calibration resolution only.

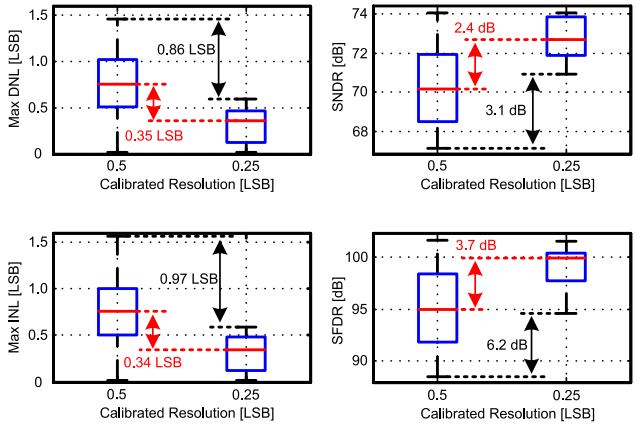


Fig. 16. Statistical box-plots of the static and dynamic performance with the different offset calibration resolutions (0.5 and 0.25 LSB).

of 0.5 LSB. By reducing the calibration resolution to 0.25 LSB, the amended statistical results are depicted in Fig. 16. The results show the DNL and INL are improved by 0.86 and 0.97 LSB, respectively, with a resulting SNDR improvements of 3.1 dB. Although the SFDR can be improved by using the calibration resolution of 0.25 LSB to reduce the high-order spurs, the third-order distortion from the measured shape of INL will dominate the achievable SFDR performance.

Table III summarizes the performance comparison of this paper with the state-of-the-art ADCs at a speed beyond 100 MS/s in 12-bit resolution. With the proposed sub-radix-3 architecture and low-power techniques (ARS DACs and RNL comparators), the implemented 150-MS/s 12-bit SAR ADC achieves a Walden FoM of 10.3- and 18.9-fJ/conversion-step at 1 MHz and Nyquist inputs, respectively.

V. Conclusion

This paper presents a 150-MS/s 12-bit SAR ADC with a synergistic integration of M-bit/cycle and sub-radix techniques. The implemented sub-radix-3 architecture is optimized to achieve a 12-bit conversion in nine cycles with the adaptive error tolerance using the proposed hybrid A-to-D design procedure. The ARS DACs are proposed to reduce the effective switching capacitance for the settling time and switching power savings. Offset injection-based foreground calibration is developed to maintain the speed and improve the power efficiency of the comparators. The RNL comparators are implemented to realize the optimized power and noise tradeoffs for the precedent (MSB) to the subsequent (LSB) conversions correspondingly. The tri-latch CML is proposed to simplify the SAR logic and shorten the SAR loop delay. The prototyped ADC demonstrates a competitive performance at a 0.9-V supply voltage with an excellent Walden FoM (FoM_W) of 10.3-fJ/conversion-step in an active area of 0.04 mm^2.

Acknowledgment

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