A Fully Integrated Buck Regulator With 2-GHz Resonant Switching for Low-Power Applications

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***Abstract*— This paper presents a fully integrated buck regulator design for low-power applications. In order to enable the usage of on-chip inductor for low load current 10–40 mA, the proposed buck regulator is designed with an ultra-high switching frequency at 2 GHz, which is the highest switching frequency reported so far. To reduce the power switch losses, resonant switching scheme is utilized to save the switching clock energy. Tunable slew rate recovery circuits are used to improve the efficiency of the design. The proposed buck regulator has been implemented in 65-nm CMOS technology with a 1.1-V input. Measurement shows a wide output range of 0.3–0.86 V. The proposed design achieves up to 73% power efficiency.**

***Index Terms*— Buck regulator, fully integrated, high switching frequency, low-power applications, resonant switching.**

I. Introduction

ENERGY-EFFICIENT operation at near-threshold or sub-threshold voltage for modern digital microprocessor has been often used to achieve the so-called minimum energy operating point [1]–[2]. The recent rapid developments on low-power applications, such as wearable electronics [3], Internet of Things [4], have created new demands on the power management circuits with low output voltages. To create low supply voltages for modern microprocessors, integrated on-chip voltage regulators are commonly used including low-dropout regulator (LDO), switched capacitor (SC) regulator, and buck regulator. LDO normally achieves good energy efficiency at high output voltages, but suffers significantly from low efficiency at lower output voltages [5], [6]. SC regulators have a better efficiency performance than LDO at large conversion ratio. However, the conversion ratio of SC regulator is typically fixed, e.g., 2-to-1, as the relatively fixed capacitor values of flying capacitors and output capacitors. To obtain wider output voltage range, configurable capacitor array and numerous switches need to be implemented increasing design complexity and overhead [7], [8]. Buck regulator utilizes inductor instead of capacitor to achieve voltage step-down [9]–[17]. Comparing with the SC regulator, buck regulator is implemented with inductors and relies on switching current for voltage conversion. By adjusting the duty cycle of the power switches of buck regulator, wide output voltage range can be easily obtained with single configuration rendering simplicity of the design.

Fig. 1(a) shows a simplified buck regulator and its key design parameters. For buck regulator, its step-down voltage ΔV is fundamentally determined by the inductance value L and the changing rate of inductor current di_L/dt, as follows:

$$\Delta V = L \cdot \frac{di_L}{dt} = L \cdot \frac{\Delta i_L}{D} \cdot f_{\text{sw}} \tag{1}$$

in which D is the duty cycle of the switching clock and f_{sw} is the regulator switching frequency. Δi_L is the current ripple of inductor L, which is determined by the inductance and switching frequency, as follows:

$$\Delta i_L = \frac{(V_{\text{in}} - V_{\text{out}}) \cdot D}{L \cdot f_{\text{sw}}}. \tag{2}$$

Therefore, given the target regulator specifications, e.g., $V_{\text{in}} - V_{\text{out}}$ and D, the designers can only adjust the inductance value L and the switching frequency f_{sw} to meet the design requirements. Fig. 1(b) shows the design parameter relationships between the inductance L and the switching frequency, with assuming fixed $\Delta V = 0.6$ V and $D = 0.5$. For the conventional buck regulators, the design strategy normally chose large value off-chip inductor L and slow switching frequency f_{sw} to achieve the power efficiency above 90% [9]–[11]. The value of off-chip inductors is normally more than a few hundreds of nH or even several μH, and the switching frequency is less than 20 MHz. Although this design approach achieves high-efficiency performance, the use of off-chip components increases the size and cost of the overall system.

Fully integrated buck regulator design using on-chip inductor attracts more and more attention in recent years due to the small form factor of the system and better integration with on-chip microprocessors [12]–[16]. However, on-chip inductors are expensive and hence supporting large inductance, e.g., more than dozens of nH becomes prohibitively costly. To realize the fully integrated designs, the limited chip area only allows small inductance value, i.e., less than 5 nH. Larger on-chip inductor (>5 nH) with small conduction resistance will need special customized design and is area costly. In addition, as shown in (2), the small on-chip inductance causes the magnitude of the inductor current ripple Δi_L increase proportionally, which could form the reverse current flowing through the inductor and significantly degrade the power efficiency. Therefore, to maintain small inductor current ripple with only

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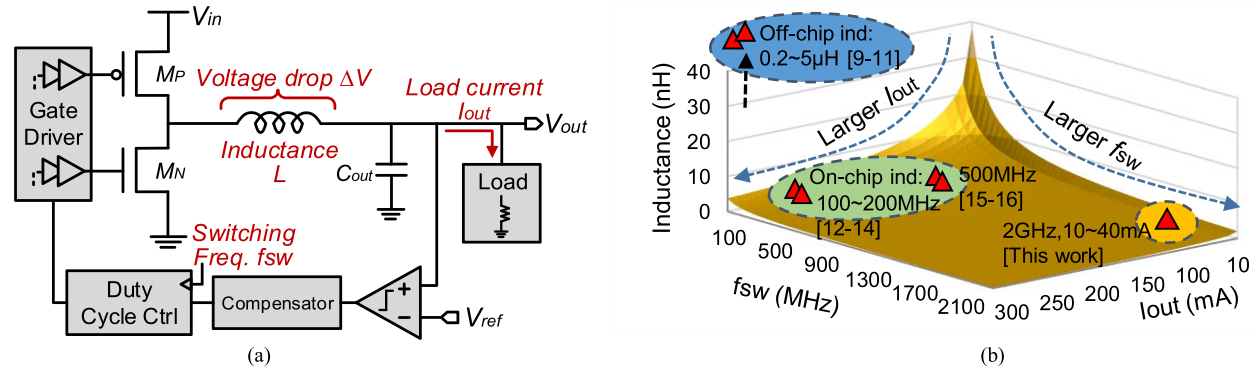


Fig. 1. (a) Simplified block diagram of buck regulator and the design parameters. (b) Inductance versus switching frequency and load current for buck regulator.

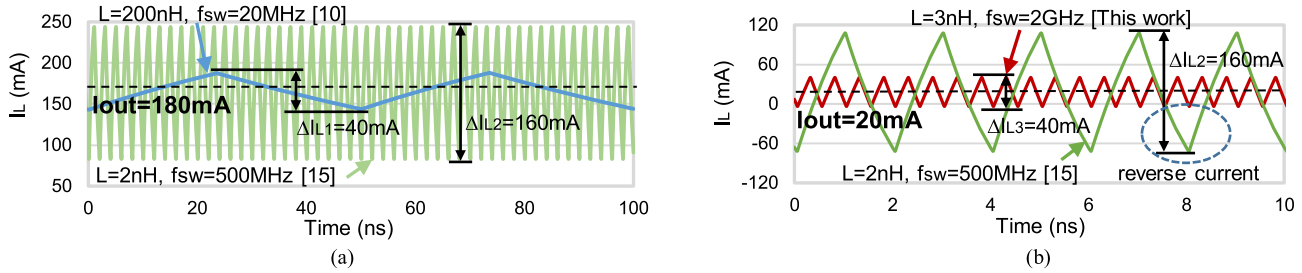


Fig. 2. Simulation waveforms for the inductor current i_L with different switching frequencies under (a) load current 180 mA and (b) low output current 20 mA.

few nH on-chip inductor L, the switching frequency f_{sw} has to be pushed much higher to 100–200 MHz [12]–[14], or even 500 MHz [15], [16] for the fully integrated buck regulator designs.

One important consideration for the fully integrated buck regulator design is that the power efficiency is lower than its off-chip counterparts. For example, the peak efficiency could only achieve 68% with switching frequency 500 MHz [15]. The low power efficiency of the fully integrated buck regulator mainly comes from the following two reasons. First, the on-chip inductor has much worse quality factor Q comparing with the off-chip inductor quality. This leads to much more conduction loss from the inductor resistance. Second, the power efficiency is significantly degraded due to the switching loss on the power switches at high switching frequency. Besides, the gate driver and loop control logics operating at higher frequency also consume more power. As a result, both the power losses from the inductor and power switches are significantly higher for fully integrated solution leading to lower conversion efficiency.

Fig. 2(a) shows the simulation waveforms of the inductor current i_L with a output current $I_{out} = 180$ mA at different switching frequency and inductance values. Comparing with the buck regulator with off-chip inductor [10], pushing the switching frequency from 20 to 500 MHz achieves fully integrated buck regulator with 100× smaller on-chip inductor [15]. However, the use of small inductor leads to both 4× larger inductor current ripple Δi_L and 25× higher switching frequency f_{sw}, which causes significant degradation of the power efficiency.

For low-power application, which refers to an output current I_{out} of only 10 of milliamps, the design of a fully integrated buck regulator is even more challenging. For example, if maintain the same $L = 2$ nH and $f_{sw} = 500$-MHz design strategy as [15] and reduce the output current from 180 to 20 mA, the large current ripple Δi_{L2} at 500-MHz results reverse inductor current leading to significant degradation on the efficiency, as shown in Fig. 2(b). As the inductor value is limited by the area, the only approach to resolve this issue is to further increase the switching frequency to reduce the inductor current ripple, as illustrated by (2). As shown in Fig. 2(b), by increasing the switching frequency from 500 MHz to 2 GHz, the inductor current ripple is reduced by 4× without negative inductor current, and the small on-chip inductance value is maintained.

To avoid this reverse inductor current issue, discontinuous conduction mode (DCM) at light load conditions can be adopted for buck regulators [11], [18]. However, implementing the DCM control logics and detecting the zero-current point at gigahertz frequency is very timing/delay challenging and power consuming. In addition, smaller duty cycle range, i.e., output voltage range, is available when the switching frequency increases due the current detection delay [9]. Therefore, in this paper, the proposed regulator is operating only at continuous conduction mode. But for the majority output current range, we guaranteed no reverse current during the operation.

In this paper, we present a fully integrated buck regulator design targeting at low-power and low output voltages. In order to utilize on-chip inductor and avoid the reverse

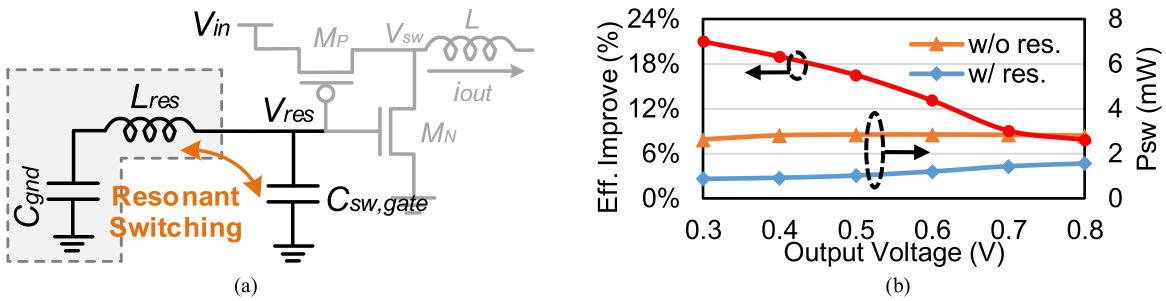


Fig. 3. (a) Conceptual diagram of the resonant switching scheme. (b) Simulation of the resonant switching benefits.

inductor current at light load conditions, the switching frequency is pushed to ultra-high frequency, i.e., 2 GHz, which is the highest switching frequency reported so far [17]. As mentioned above, the switching loss on the power switches will dominate at high switching frequency and limit the power efficiency. To improve the efficiency, a resonant switching scheme is proposed, which reduces the energy loss of the power switches clocking by forming a resonant network. The proposed design employs only 3 nH on-chip inductor for buck regulator and 8.2 nH on-chip inductor for resonant switching within 0.073 mm^2 area. The measured output voltage achieves wide tuning range of 0.3–0.86 V with efficiency up to 73%.

The rest of this paper is organized as follows. The idea and benefits of the resonant switching for high switching frequency buck regulator design is introduced in Section II. The overall schematic and detail design of each block is presented in Section III. The analysis for the inductor coupling and power loss breakdown is illustrated in Section IV. Measurement results obtained from the prototype buck regulator are shown in Section V, followed by the conclusion in Section VI.

II. Resonant Switching Scheme

Resonant clocking technique was previously proposed to save the clock power in modern microprocessor [19], [20]. Prior works also introduced to utilize the resonant switching to assist the SC regulator design [21]. To improve the power efficiency of buck regulator at ultra-high switching frequency, this paper applies resonant switching scheme to the buck regulator to reduce the switching power from the power switches.

As the conceptual diagram shown in Fig. 3(a), the power switches M_P and M_N have a total gate capacitance $C_{\text{sw,gate}}$. In the conventional clocking scheme, the power loss from the switching clock of the power switches is expressed by the following equation:

$$P_{\text{sw}} = \frac{1}{2} C_{\text{sw,gate}} V_{\text{in}}^2 f_{\text{sw}}. \tag{3}$$

The realization of resonant switching is by utilizing another inductor L_{res} to form the LC resonance between $C_{\text{sw,gate}}$ and L_{res}. The oscillation frequency is known as (4). Capacitor C_{gnd} provides ac ground for inductor L_{res}

$$f_{\text{res}} = \frac{1}{2\pi\sqrt{L_{\text{res}} C_{\text{sw,gate}}}}. \tag{4}$$

Around the frequency f_{res}, the LC tank impedance reaches the peak value and only requires smaller current to maintain a given clock magnitude. Comparing with the conventional switching power loss in (3), the resonant switching clock power loss is derived as follows [20]:

$$P_{\text{sw,res}} = \frac{\pi}{4Q} C_{\text{sw,gate}} V_{\text{dd}}^2 f_{\text{sw}}. \tag{5}$$

The quality factor here is the system Q, which is the parallel combination of the inductor Q_L and the gate capacitor Q_C, as expressed in the following equation [19]:

$$\frac{1}{Q} = \frac{1}{Q_L} + \frac{1}{Q_C}. \tag{6}$$

The Q value reaches its peak value at the LC resonant frequency. The benefit of power saving obtained from resonance switching scheme depend on a factor of $\pi/2Q$. If $Q = 5$, then the switching clock loss can be reduced by 68% of the conventional clock loss, which is a significant power saving. In a CMOS design, integrated on-chip inductor dominates the overall Q but is further degraded by metal routing and resistance on the connected gate capacitance leading to a Q value between 5 and 10 in our design.

To verify the resonant switching benefit for buck regulator design, we conducted simulations in a 65-nm CMOS process, as shown in Fig. 3(b). The switching frequency of regulator is set to be 2 GHz. A fixed 30-Ω resistor is utilized as the output load and the output voltage is swept from 0.3 to 0.8 V. With the assistance of the resonant switching scheme, the power loss from the switching clock P_{sw} can be reduced by 55%. In terms of power efficiency, the reduction of the switching clock loss improves the efficiency by at most 20% at 0.3 V. At higher output voltage, the power losses of other components (e.g., M_P, M_N, and L) increase due to the larger delivered load current. As a result, the switching clock loss P_{sw}take less percentage out of total losses and the efficiency improvement becomes less. In the simulation experiment, the resonant switching scheme improves the efficiency by 20% at 0.3 V and 8% at 0.8 V. The experiment shows that the proposed resonant switching scheme could significantly improve the efficiency for buck regulator at high switching frequency, with more improvement benefits obtained at lower output voltage conditions.

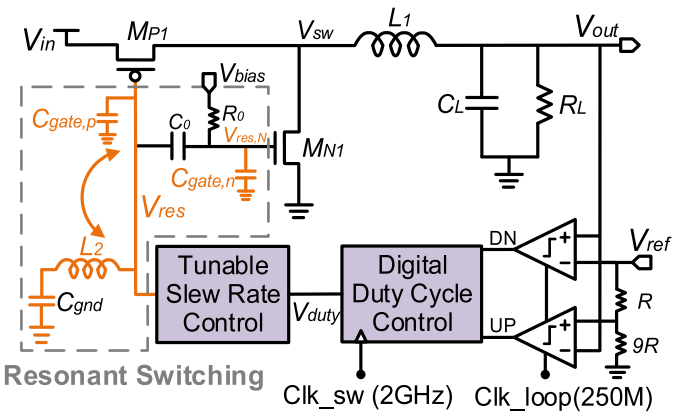


Fig. 4. Block diagram of the proposed buck regulator design.

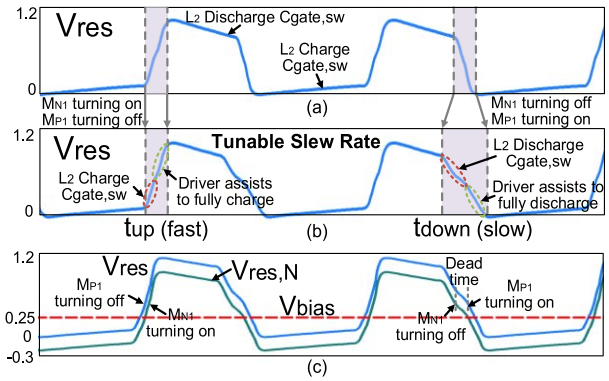


Fig. 5. Simulated switching clock V_{res} of the power switches. (a) Simulated V_{res} without adjusting slew rate. (b) Tunable SR strategy to extend the falling edge transition. (d) DC biasing level shift to insert "dead time."

III. Proposed Buck Regulator

A. Overall Topology

The overall scheme of the proposed resonant buck regulator is shown in Fig. 4. Different from conventional design, to utilize the proposed resonant switching scheme, the gate of the power switches M_{P1} and M_{N1} are jointly switched through a resonant network. The resonant switching V_{res} is formed between inductor L_2 with the power switches' gate capacitance $C_{\text{gate},p}$ and $C_{\text{gate},n}$. Capacitor C_{gnd} provides a self-biasing ac ground with a value of 30 pF. To suppress the shoot through current, switch M_{N1} is ac coupled by capacitor C_0 and biased at low-voltage V_{bias} near its threshold voltage. The capacitor C_0 is 4 pF, and the biasing voltage V_{bias} is connected through a 2-kΩ resistor R_0 and provided by external voltage with the range of 0.1–0.3 V. As voltage V_{bias} is connected through a high resistance to provide a dc offset, it will not block the original signal and consume more power.

The inductance value of main buck inductor L_1 is 3 nH, and the resonant inductor L_2 is 8.2 nH. The selection of the L_2 value is based on the resonance equation (4) with the target switching frequency of 2 GHz. The comparators compare the output voltage V_{out} with reference voltage V_{ref} at a loop sampling frequency 250 MHz, and issue the digital up/down (UP/DN) signals to the duty cycle control block. Signal V_{duty} is generated at 2 GHz with controlled duty cycle, which is then sent to the tunable slew rate control block.

For conventional buck regulator design, the switching clock signals for power switch M_{P1} and M_{N1} are normally provided by separated logics inside the gate driver. To reduce the possible short circuit current during the power switch transitions, also referred as shoot-through current, the gate driver normally leaves a "dead time" delay margin between the transitions of the power switches $M_{P1}$and M_{N1} [22]. For example, the M_{P1} should be turned OFF a short time ahead of the turn-ON of M_{N1}. Similarly, the M_{N1} should be turned OFF sometime before the M_{P1} is turned ON.

However, in the proposed buck regulator, as the gate of M_{P1} and M_{N1} are controlled by the same switching signal V_{res} to share the same resonant inductor L_2, there is no "dead time" control between the transition of M_{P1} and M_{N1}. As the simulated waveforms of node V_{sw} shown in Fig. 5(a), the resonant inductor L_2 discharge (charge) the power switch gate capacitance $C_{\text{gate},p}$ and $C_{\text{gate},n}$ after $M_{P1}(M_{N1})$ fully turned OFF and store (dissipate) the energy inside L_2. During the power switch transitions, inductor L_2 first provides the stored energy to charge or discharge the gate capacitance, until the gate driver has been turned ON to assist fully charge or discharge $C_{\text{gate,sw}}$, as shown in Fig. 5(b).

To leverage the most energy benefit from resonant switching, the slew rate of signal V_{res} is expected to be slow, i.e., longer transition time t_{up} and t_{down} to fully utilized the stored resonant energy. However, the slew rate degradation of V_{res} rising edge is detrimental to the overall power efficiency. The main reason is that the peak inductor current i_L happens during the rising edge of V_{res}, e.g., M_{P1} turning off. During the M_{P1} transition, it first turns into the saturation region, which has very large resistance. The peak inductor current flow through the large M_{P1} resistance generates large amount of power loss and degrade the efficiency. Therefore, the slew rate operation strategy used in the proposed design is to fully realize the resonant switching for the falling edge of V_{res}, and partially utilized for the rising edge of V_{res}, as shown in Fig. 5(b). The slew rate of V_{res} falling edge is degraded by the assistance of delayed switching of M_{N2}, as discussed in Section III-B.

In order to create some "dead time" between M_{P1} and M_{N1} transitions, biasing voltage V_{bias} is utilized to provide a different dc level for switch M_{N1}. As shown in Fig. 5(c), the transition time for turning on M_{N1} is postponed and the time for turning off M_{N1} is moved ahead. Thus the power switch transition is intentionally separated by different bias voltage, which leads to reduce the shoot through current. The effectiveness of utilizing this dc biasing will be illustrated in Section III-D.

B. Tunable Slew Rate Control

As the slew rate of the switching clock V_{res} is critical to the efficiency performance, a tunable slew rate control block is designed. Both the V_{res} slew rate of rising edge and falling edge can be tuned independently. The schematic of the proposed tunable slew rate control block is shown in Fig. 6. The input of this block is the signal V_{duty}, whose duty cycle is already tuned by the duty cycle control block. To tune the

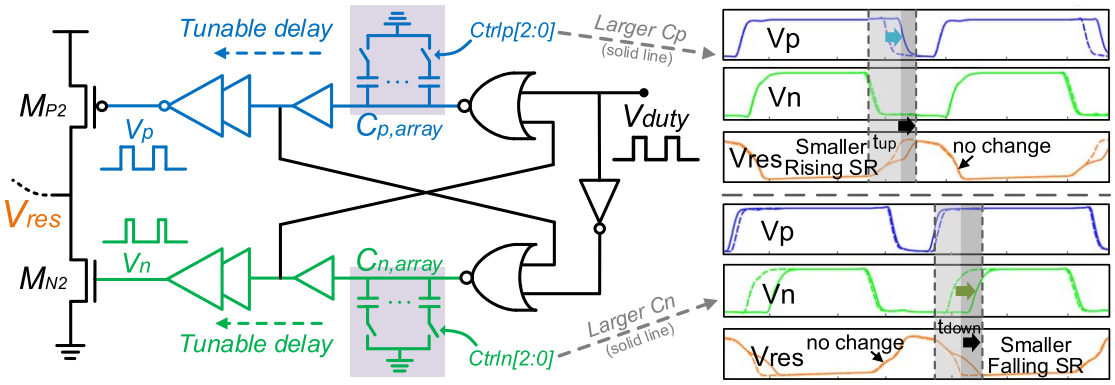


Fig. 6. Tunable slew rate control block design and the simulation waveforms for independent tuning the slew rate of V_{sw} falling and rising edge.

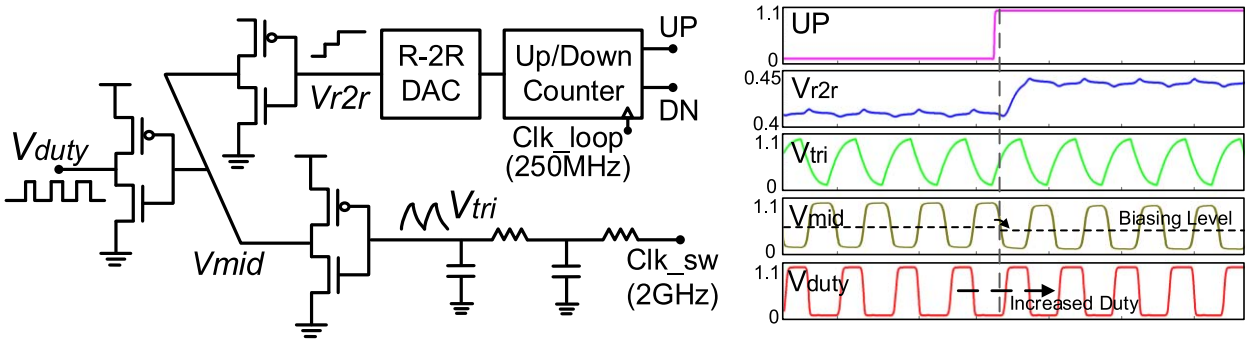


Fig. 7. Digital duty cycle control block and the simulation waveforms.

slew rate of each edge, the transition timings for the switch clock driver M_{P2} and M_{N2} at node V_p and V_n are adjusted, respectively. Two digitally controlled tunable capacitor array $C_{p,\text{array}}$ and $C_{n,\text{array}}$ are utilized to tune the transition delay time at V_p and V_n. As shown in the simulation waveforms in Fig. 6, with larger capacitance $C_{p,\text{array}}$, the falling transition at node V_p is postponed, while the node V_n transition maintains the same. Therefore the transition time for the V_{res} rising edge t_{up} becomes longer, and the slew rate of the V_{res} rising edge becomes smaller. Similarly, with tuning larger $C_{n,\text{array}}$, the node V_n rising is postponed to extend the transition time t_{down} and the slew rate of V_{res} falling edge becomes smaller.

As mentioned in Section III-A, fast rising slew rate and slow falling slew rate are desired for the signal V_{res}. Thus relative larger $C_{n,\text{array}}$ and smaller $C_{p,\text{array}}$ are used to tune the V_{res} slew rate. The tunable capacitance is realized by a 4-bit digital controlled capacitor array, which tunes the path delay with the resolution about 10 ps. In the proposed design, the rising time t_{up} is set at around 40 ps and the falling time t_{down} is 120 ps for V_{res} at 2-GHz switching frequency. At different switching frequencies f_{sw}, there is different optimal slew rate for the highest power efficiency performance. For lower switching frequency, the falling transition time t_{down} could be further extended to obtain more resonance power saving benefit.

C. Duty Cycle Control

When the output voltage becomes higher or lower than the reference voltage, the duty cycle of the switching signal V_{res} needs to be adjusted. In the proposed design, the regulator output voltage V_{out} compares with the reference voltage V_{ref} and a voltage level $0.9V_{\text{ref}}$ generated by an on-chip resistor divider, as shown in Fig. 4. If V_{out} higher than the V_{ref} or lower than 0.9 V_{ref}, signal DN or UP will be toggled to be high. Otherwise, both UP/DN signal will maintain low. Fig. 7 shows the schematic of the digital duty cycle control block. The UP/DN signals are sent to a UP/DN counter, which accumulates the comparison results and controls the following R-2R DAC. A 5-bit R-2R DAC is designed to generate the biasing voltage V_{r2r}. The feedback sampling frequency is provided by the clock "Clk_loop" at 250 MHz. Besides, another clock generator "Clk_sw" provides the high-frequency switching signal at 2 GHz, which has a wide frequency tuning range 1–3 GHz.

The 2-GHz switching signal is passed through a two-stage *RC* network to transform into a triangle waveform V_{tri}. To convert the triangle waveform V_{tri} back to square wave with tunable duty cycle, two inverter outputs are connected together at node V_{mid}, which works as an inverter with a movable reverse point. Based on the adjustable voltage V_{r2r}, the dc biasing level of point V_{mid} is also adjusted, as the simulation waveforms shown in Fig. 7. Another inverter is utilized following V_{mid} to transform V_{mid} back to rail-to-rail square waveform V_{duty} with tuned duty cycle. When a UP signal is triggered, it will generate larger V_{r2r} voltage, lower biasing level of V_{mid}, and consequently larger duty cycle of V_{duty}. Similar duty cycle control strategy using a *RC* network to transform to triangle waveform is also used in [23].

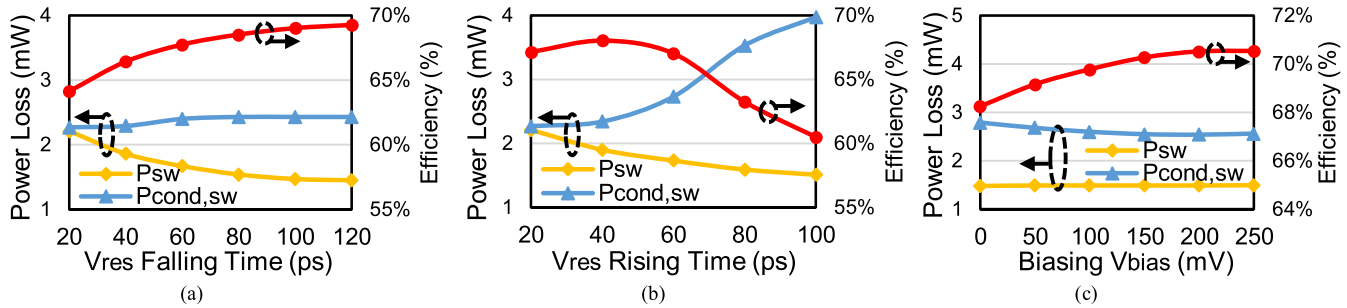


Fig. 8. Simulated efficiency and power loss changes versus (a) V_{res} falling time, (b) V_{res} rising time, and (c) dc biasing V_{bias}.

The UP/DN hysteresis-based feedback control can be approximated to a pole originating from the counter acting as an integrator [24]. For buck regulator, the output RLC can be treated as a simplified second-order RLC circuit, i.e., a series LC with the load R connected in parallel with C. As both the poles of the load RLC is located at the stable region of the S-plane, the stability of this hysteretic feedback loop can be guaranteed.

D. Design Parameter Discussion

In this section, some of the key design parameters and the tradeoffs are further discussed and experimented in detail.

1) V_{res} Slew Rate: The slew rate of the resonant switching signal V_{res} balances the tradeoff between obtaining more resonant energy saving and suffering more power switch conduction losses. The longer V_{res} transition time will bring more switching power saving. The impact of the V_{res} slew rate is simulated under the condition of output voltage/current 0.6 V/20 mA and shown in Fig. 8. In Fig. 8(a), the V_{res} rising time is fixed to 20 ps, and the falling time is adjusted by the proposed tunable slew rate control block. The experiment shows the resonant switching power P_{sw} reducing with longer falling time, which is due to the resonant inductor L_2 discharge more energy during the V_{res} transition, as shown in Fig. 5(b). During the V_{res} falling, the inductor L_1 current reaches its minimal value, thus longer power switch transition time will not cause too much increase of the power switch conduction loss $P_{\text{cond,sw}}$. Overall the extension of V_{res} falling time gains more resonant energy saving, which contributes more than 5% efficiency improvement.

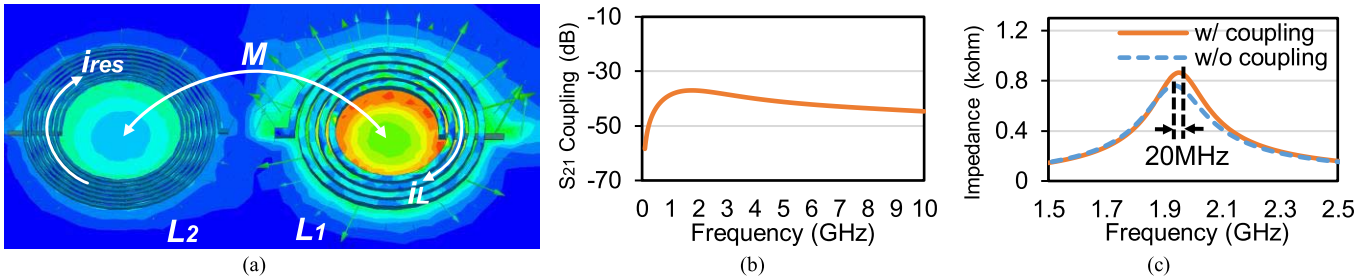
The sweep of V_{res} rising time is shown in Fig. 8(b) with a fixed 20-ps falling time. Similar as the extension of falling time, longer rising time will also store more resonant energy and reduce the switching power P_{sw}. However, as the inductor L_1 current reaches its peak value during the V_{res} rising, slower switch transition causes significant increase of the power switch conduction loss $P_{\text{cond,sw}}$. The overall efficiency will not get any improvement by the resonant switching. Therefore, the rising time of about 40 ps and the falling time of 120 ps is adopted for the resonant signal V_{res}.

2) V_{bias} Biasing Level: The transitions of power switch M_{P1} and M_{N1} are intentionally separated by utilizing different dc biasing levels. The benefit of using biasing voltage V_{bias} is shown in Fig. 8(c). With larger biasing voltage, the conduction loss on the power switches $P_{\text{cond,sw}}$ is reduced, which is mainly due to less losses during the power switch transitions. It needs to be known that the biasing voltage V_{bias} causes the lower gate voltage for M_{N1} and leads slightly larger turn on resistance. However, as the power loss is dominated by the M_{P1}, which will be shown in Section IV, the separation of the turn ON/OFF threshold of power switched can significantly reduce the shoot through current loss on M_{P1}. Hence the increasing of M_{N1} power loss is overwhelmed by the benefit of M_{P1} power loss reduction, as shown by the overall P_{sw} in Fig. 8(c). Besides, utilizing the dc biasing will not change the resonant power loss or cause more power consumption, as it is connected through a high impedance resistor. The reduction of power switch conduction loss is equivalent to about 2%–3% efficiency improvement.

3) Inductance Selection: The resonant frequency at 2 GHz in this paper is mainly determined by the limited inductor value and the requirement of low output current without reverse current. To achieve good power efficiency performance, the on-chip inductor used for the buck regulator is expected to have high quality, i.e., low resistance, within small area. Therefore, the inductor L_1 is designed with 4.5 turns and 8 μm width. Meanwhile, the resonant inductor L_2 is used for storing gate capacitor charge and discharge energy and only small amount current flow though. The quality requirement of the inductor L_2 is relative minor critical. But to meet the resonant frequency of 2 GHz, i.e., (4), the inductor L_2 value is designed large as the power switch gate capacitance is very small. In this paper, inductor L_2 is designed with seven turns and 4 μm width. Both inductor L_1 and L_2 occupied same die area.

It is worth to point out the inductor selection difference between the conventional buck regulator design and the proposed resonant buck regulator. Based on (1), the conventional buck regulator could be designed with 12 nH, i.e., about the total inductance of L_1 and L_2, at 500-MHz switching frequency. However, designing a 12 nH on-chip inductor with the same low conduction resistance as the 3 nH L_1 in this paper will be much more area costly. If maintain the same die area as this paper, counting the total area of L_1 and L_2, for a 12 nH on-chip inductor, the conduction loss on the on-chip inductor will become much larger and the regulator efficiency will be significantly degraded.

4) Sizing of the Power Switches: The sizing strategy of the power switches is slightly different with the conventional



(a) (b) (c)

Fig. 9. (a) EM simulation of the inductor mutual coupling. (b) Mutual coupling simulation. (c) Mutual coupling effects on the resonant frequency.

buck regulator operating at low switching frequency [9]–[11]. As the ultra-high switching frequency at 2 GHz in this paper, the switching driver for the power switches consumes significant power, i.e., 20%–30% total power loss as illustrated in Section IV. Therefore, the switching power loss needs to be taken into the consideration during the power switching sizing. Actually the tradeoff between the power switch sizing and the switching loss from the gate driver is one of the most critical design keys. With larger power switch size, the conduction loss on the power switches can be reduced, while the switching power is increased due to larger driving load. Comparing prior regulator design [13], [14], the power switch sizing in this paper is relative small to reduce the switching gate driver load, i.e., switching power loss. During the design period, the power switch size is swept to obtain the optimum efficiency performance and balance the tradeoff between the power switch loss and switching driver loss.

IV. EM and Power Loss Analysis

A. Electromagnetic Analysis

As there are two inductors in the proposed buck regulator design, the electromagnetic (EM) analysis and mutual coupling simulations are conducted with the actual inductor sizes and distance. As shown in Fig. 9(a), the current i_L flows through the inductor L_1, and the resonant switching current i_{res} flows on the inductor L_2. The mutual coupling M exists between L_1 and L_2. In the EM simulation, each terminal of the inductor is defined as a port. The mutual coupling can be represented by the S-parameter between L_1 ports and L_2 ports. During the simulation, we obtained the mutual coupling between L_1 and L_2 is less than -35 dB within the frequency range from 500 MHz to 10 GHz, as shown in Fig. 9(b). The inductor mutual coupling effects will be explained as following.

The voltages generated on the corresponding inductor can by expressed as follows:

$$V_1 = L_1\frac{di_L}{dt} + M\frac{di_{\text{res}}}{dt} \tag{7}$$

$$V_2 = L_2\frac{di_{\text{res}}}{dt} + M\frac{di_L}{dt}. \tag{8}$$

To compute the effective inductance, the other equation to express the inductor voltage is as follows [16]:

$$V_1 = L_{\text{eff},1}\frac{di_L}{dt}, \quad V_2 = L_{\text{eff},2}\frac{di_{\text{res}}}{dt}. \tag{9}$$

Therefore, the effective inductance could be derived as follows, which includes the self-inductance and the mutual inductance M:

$$L_{\text{eff},1} = L_1 + M\frac{di_{\text{res}}/dt}{di_L/dt} \tag{10}$$

$$L_{\text{eff},2} = L_2 + M\frac{di_L/dt}{di_{\text{res}}/dt}. \tag{11}$$

During the buck regulator operation, the inductor current i_L is normally much larger than the resonant switching current i_{res}. Therefore the effective inductance of L_1 can be simplified as follows, which shows the mutual coupling has little effect to the main buck inductance:

$$L_{\text{eff},1} \approx L_1. \tag{12}$$

However, the mutual coupling will slightly affect the effective inductance of L_2 as (11). Depend on the floorplan of the inductors, either positive or negative mutual inductance M could be obtained, which will increase or decrease the effective inductance of L_2. As shown in Fig. 9(c), the peak impedance of the resonant LC tank is simulated with or without the mutual coupling effect. The EM simulation shows only around 20-MHz resonant frequency shift due to mutual inductance, which is small effect on the resonant frequency.

B. Power Loss Analysis

The power loss breakdown of the proposed buck regulator is analyzed in this section. The power loss mainly comes from the power switch conduction loss $P_{\text{cond,sw}}$, inductor L_1 conduction loss P_{ind}, resonant switching power P_{sw}, and the feedback loop power P_{loop}, as follows:

$$P_{\text{Loss}} = P_{\text{cond,sw}} + P_{\text{ind}} + P_{\text{sw}} + P_{\text{loop}}. \tag{13}$$

1) Power Switch Loss $P_{cond,sw}$: The conduction loss on the power switches M_{P1} and M_{N1} consists of two parts. The first part is the conduction loss when the power switches are fully turned ON/OFF, which could be expressed by the $i^2_{\text{out.rms}}r_{\text{ON}}$. r_{ON} is the turn ON resistance of the power switches. Besides, there are also conduction losses during the power switch transition time t_{up} and t_{down}, as described in Fig. 5, which is proportional to the switching transition duration and the regulator switching frequency f_{sw}. The overall conduction loss for the power switches M_{P1} and M_{N1} could be summarized

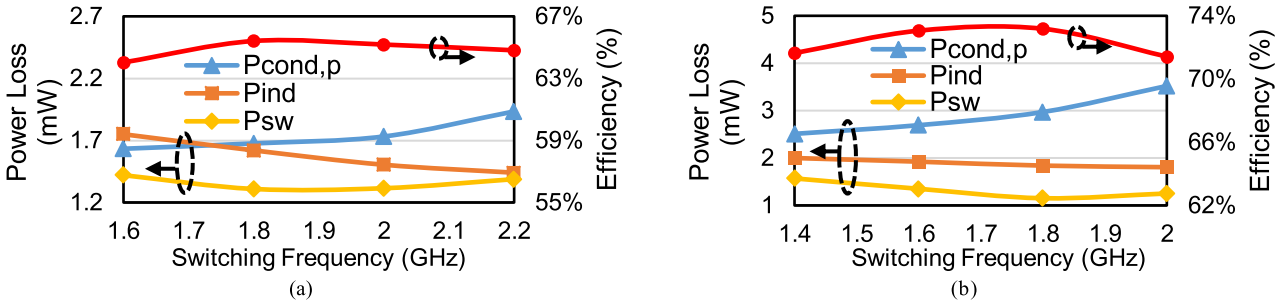


Fig. 10. Simulated power loss breakdown change versus switching frequency at (a) $V_{\text{out}} = 0.6$ and (b) $V_{\text{out}} = 0.75$ V.

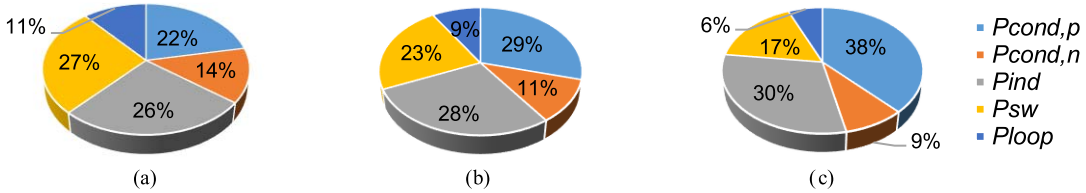


Fig. 11. Simulated power loss breakdown at (a) $V_{\text{out}} = 0.5$, (b) $V_{\text{out}} = 0.6$, and (c) $V_{\text{out}} = 0.75$ V.

as follows:

$$P_{\text{cond}.p} = i_{\text{out,rms}}^2 r_{\text{ON}} + \left(\int_0^{t_{\text{up}}} + \int_0^{t_{\text{down}}}\right) i_{\text{ds}}(v_{\text{in}} - v_{\text{sw}})dt \cdot f_{\text{sw}} \tag{14}$$

$$P_{\text{cond}.n} = i_{\text{out,rms}}^2 r_{\text{ON}} + \left(\int_0^{t_{\text{up}}} + \int_0^{t_{\text{down}}}\right) i_{\text{ds}} v_{\text{sw}} dt \cdot f_{\text{sw}}. \tag{15}$$

From (14) and (15), we can find out the basic approaches to suppress the power switch loss. First, reducing the power switch on resistance r_{ON} is the most effective method to reduce the conduction loss. However, the size of power switches is constrained by the power loss from high-speed switching of gate capacitance, as discussed previously. Second, the switching frequency and the power switch transition duration should also be well controlled to reduce the conduction loss. To reduce the power loss during transitions, the power switch transition time t_{up} and t_{down} should be short.

The simulated power loss breakdown versus switching frequency is shown in Fig. 10. As the conduction loss is proportional to the switching frequency f_{sw}, the power switch loss is increasing with higher switching frequency. Besides, the power loss breakdown at different output voltage levels is shown in Fig. 11, in which the conduction losses from power switches $P_{\text{cond},p}$ and $P_{\text{cond},n}$ dominate the overall power loss. In addition, the PMOS power loss is more than that from NMOS. As explained before, the reason is that the peak inductor current flows through large M_{P1} resistance during turning off the M_{P1} switch at V_{res} rising edge. With higher output voltage, the delivered output current is increased and causes more conduction power losses. For example, at output voltage 0.5 V, the $P_{\text{cond},p}$ contributes 22% power loss, while it contributes 38% power loss at output voltage 0.75 V. Overall, the conduction losses on the power switches ($P_{\text{cond},p} + P_{\text{cond},n}$) take 47% and 36% out of total power loss when output voltage is 0.75 and 0.5 V, respectively, which are the largest power loss contributors.

2) Inductor Loss P_{ind}: The output current flows through the buck inductor L_1 leads to the conduction power loss as follows:

$$P_{\text{ind}} = I_{\text{ind,rms}}^2 r_{\text{ind}} \tag{16}$$

where $I_{\text{ind,rms}}$ is the root mean square (rms) of the inductor current i_L. As shown in Fig. 2, the inductor current operates as a triangle wave, which rms value can be derived as follows:

$$I_{\text{ind,rms}} = \sqrt{I_{\text{out}}^2 + \frac{\Delta i_L{}^2}{12}} \tag{17}$$

in which Δi_L is the inductor current ripple, as expressed in (2). Therefore, the power loss of the inductor can be converted to the following equation:

$$P_{\text{ind}} = \left(I_{\text{out}}^2 + \frac{\Delta i_L{}^2}{12}\right) r_{\text{ind}} = \left[I_{\text{out}}^2 + \frac{(\Delta V D)^2}{12L^2} \cdot \frac{1}{f_{\text{sw}}^2}\right] r_{\text{ind}}. \tag{18}$$

It is necessary to point out that the inductor resistance r_{ind} here is the equivalent series resistance (ESR) includes both the dc and ac components. With higher switching frequency, the inductor metal line suffers from the skin and proximity effects, and r_{ind} becomes a function of frequency [25]. In [26], the ESR of inductor was approximately modeled by the following equation:

$$r_{\text{ind}} \approx r_{\text{DC}} \left[1 + \frac{1}{10}\left(\frac{\omega}{\omega_{\text{cir}}}\right)^2\right] \tag{19}$$

in which the term ω_{cir} is the inductor current crowding start frequency and determined by the inductor geometry. Although the inductor series resistance is a function of the frequency, the previous study also shown that the skin effects have relatively small impact below 2-GHz frequency as the inductor metal thickness is less or equal than the skin depth [26]. In our

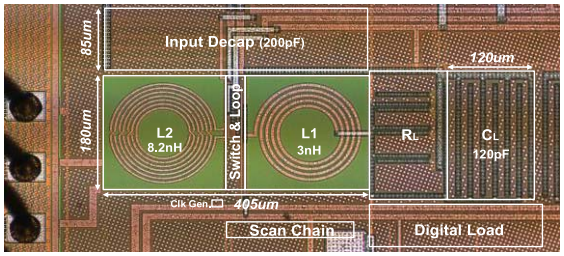


Fig. 12. Chip micrograph of the proposed buck converter.

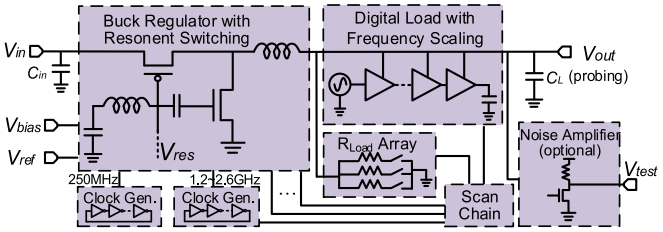


Fig. 13. Diagram of the test for prototype chip.

EM simulation, we observed the ESR r_{ind} only increase by 1.2× from 500 MHz to 2 GHz. However, the inductor ripple Δi_L is reduced 4×. Hence, the reduction of the Δi_L dominates the inductor loss scaling trend in (18) with scaling up the switching frequency f_{sw}.

As the simulated P_{ind} in Fig. 10, the inductor power loss is decreasing with the increase of switching frequency. As shown previously in Fig. 2(b), pushing the switching frequency from 500 MHz to 2 GHz decreases the Δi_L by 4 times, which reduces the inductor power loss P_{ind} by 30.6% when delivering the same amount of output power.

3) Resonant Switching Power P_{stv}: As analysis in Section II, the power loss from the resonant switching portion could be expressed as (5). The resonant switching power is proportional to the switching frequency, and inversely proportional with the *LC* tank quality factor Q, which reaches its peak value at the *LC* resonant frequency. With increasing the f_{sw}, the power P_{sw} will decrease first before reaching the resonant frequency. Beyond the resonant frequency, the Q will decrease and the switching power starts to increase. Therefore, the maximum resonant switching power saving happens at the resonant frequency. As the simulated P_{sw} in Fig. 10, the resonant frequency is around 1.8–1.9 GHz.

Besides the power loss components discussed above, there is power loss caused by the feedback control loop, which includes the comparators, duty cycle control block, etc. As the feedback loop design is relative simple and operates with lower frequency 250 MHz, the power loss on the feedback loop only takes less than 10% of the total power loss, as the P_{loop} shown in Fig. 11.

Within all the power loss sources, the PMOS switch M_{P1}, inductor L_1, and the resonant switching power are the major power loss contributors, which contribute 75%–85% power loss at different output voltage levels. At larger output voltage, the power losses on the switch M_{P1} and inductor L_1 significant increase due to larger load current.

V. Measurement Results

A. Measurement Setup

The proposed buck regulator is fabricated in a 65-nm CMOS process, as shown in Fig. 12. The on-chip inductor L_1 used for the buck regulator is 3 nH. Inductor L_2 is used for the resonant switching and its value is 8.2 nH. The power switches and the feedback control logics are placed between these two inductors. The overall area of the proposed buck regulator including the input/output decoupling capacitor is 0.13 mm^2. The core area which contains the regulator design is only 0.073 mm^2, with 91% area occupied by inductors at top metal.

The test diagram of the chip prototype is shown in Fig. 13. The input voltage is set as 1.1 V. Two ring oscillator-based clock generators are designed to provide a fast clock frequency (1.2–2.6 GHz) for the resonant switching and a low clock frequency (250 MHz) for the feedback loop. To suppress the input voltage noise, a 200-pF on-chip decoupling capacitor is placed near the regulator design. For testing the power efficiency under different output current, an on-chip static resistor array is connected to output voltage. Besides, a digital logic load is also built to test the dynamic frequency scaling (DFS) effects to the output voltage. To configure different test modes, the control bits are sent in by a scan chain.

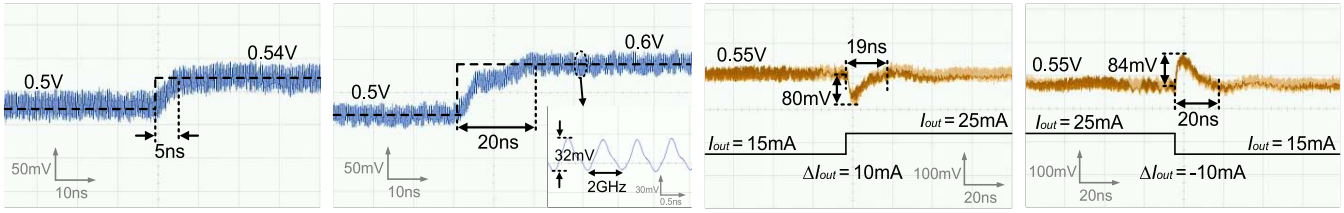
With the ultra-high switching frequency in the proposed buck regulator, the output voltage ripple is significant reduced. Hence, much smaller output decoupling capacitor C_L is needed. Compare with the previous work with a few nF or even μF output decoupling capacitor [13]–[15], we only utilize 120-pF decoupling capacitor and thus the total capacitor area of C_L is significantly reduced.

B. Transient Performance

Fig. 14 shows the transient output voltage tracking with the reference voltage or load current change. Under static loading, the response time of the proposed regulator is 5 ns, which is determined by the loop bandwidth, with reference voltage change of 40 mV. In Fig. 14(b), the reference voltage is changed with a larger step from 0.5 to 0.6 V, which requires multiple clock cycles, i.e., around 20 ns, to settle into larger voltage changes. Zoomed-in view waveform of the output voltage shows 2-GHz switching frequency with ripple magnitude of around 32 mV.

The transient response for the output current I_{out} change is demonstrated in Fig. 14(c) and (d). The transient change of the load current is generated by switching to a different on-chip static loading. With the load current changing by 10 mA, the undershoot and overshoot is around 80 mV and the settling time is 20 ns. Considering only 120-pF output decoupling capacitor is used, the current shoot magnitude could be further mitigated by using larger decoupling capacitors.

Besides the static resistor loading, a digital logic load is built to test the DFS effects to the regulator output. The digital load logics were activated with a DFS from 140 to 200 MHz, as shown in Fig. 15. A slightly larger dynamic ripple of ~60 mV was observed at digital clock frequency 140 MHz and 52-mV ripple at 200 MHz.



(a) (b) (c) (d)

Fig. 14. Measured transient response for the reference voltage change. (a) With $\Delta V_{\text{ref}} = 40$ mV, and (b) With $\Delta V_{\text{ref}} = 100$ mV, and measured transient load current response with (c) Undershoot and (d) overshoot.

TABLE I
PERFORMACE SUMMARY AND COMPARSION

	[15] 14' VLSI	[14] 17' ISSCC	[13] 17' JSSC	[8] 14' JSSC	[7] 17' JSSC	This work
Topology	Buck	Buck	Buck	SC	SC	Buck
Inductor/Capacitor	on-chip	on-chip	Wirebond	MIM Cap	MIM/MOM	on-chip
Process (nm)	22	14	130	22	65	65
Fsw (MHz)	500	100	125	250	33	2000
Iout (mA)	150	90-330	70	10-88	25-100	10-40
L (nH)	1.5	1.5	11.8	--	--	3 / 8.2
C_L (nF)	10	5	3.2	0.1	2	0.12
Vin (V)	1.5	1.5	1.2	1.23	1.6-2.2	1.1
Vout (V)	0.7~1.2	0.4-1.15	0.45-1.05	0.45-0.85 (SC)	0.6-1.2	0.3-0.86
Ripple (mV)	10	>50	84	43	30	32
Response (ns)	100 (0.15V)	700 (0.5V)	80ns (230mV)	3-5 (0.95V)	3 (58mV)	5 (40mV), 20 (0.1V)
Peak Eff. (%)	68	84	71	~73 (SC)	80	73
Eff. @0.5V_{in} (%)	--	<50	~55	~65	70	64
Area (mm^2)	1.5	0.4	0.5 (1.19 includes decap)	0.103	0.84	0.073 (0.13 includes decap)

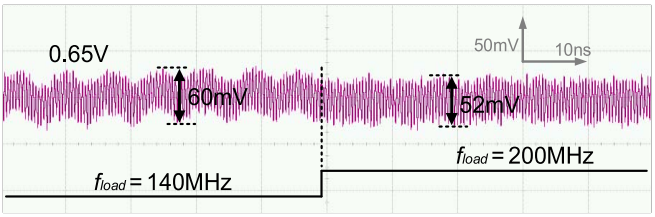


Fig. 15. Load current transient tracking.

C. Power Efficiency

The measured power efficiency versus output voltage at different load conditions is reported in Fig. 16(a). A wide output voltage range from 0.3 to 0.86 V is achieved with input voltage 1.1 V. The peak power is efficiency is 73% at 0.85 V. At 0.6 V, an efficiency of 65.1% was observed. Comparing with the ideal LDO, the proposed buck regulator achieves around 10%–20% efficiency improvement at the low output voltage range 0.4–0.6 V.

The optimal switching frequency for the best power efficiency at different output voltages is shown in Fig. 16(b). It is observed that the optimal switching frequency is around 1.9–2 G, which matches the simulation expectation in Fig. 9. With larger output voltage, the optimal switching frequency is slightly reduced. The reason is the conduction loss on the power switches becomes more dominate the overall power loss. Therefore, slightly reducing the switching frequency will reduce the power switch loss and improve the efficiency. However, at lower output voltage level, switching frequency around the natural resonant frequency is preferred due to the less loss contribution from power switches rendering better overall efficiency. The efficiency performance is also measured with different input voltages, as shown in Fig. 16(c). The peak efficiency is above 71% with input from 1.1 to 1.3 V. At output voltage range 0.4–0.5 V, the efficiency maintains larger than 50%.

The proposed buck regulator design is compared with some state-of-the-art fully integrated regulator designs, as listed in Table I. The prior fully integrated buck regulators using on-chip inductor are mainly designed for delivering load current 200–300 mA [14], [15]. In [14], a special designed planar magnetic core is utilized to improve the inductor quality and boost the peak efficiency to above 80%. However, without that special inductor design, the fully integrated buck regulator can only achieve 68% peak efficiency [15]. Comparing with the previous work, the proposed design is targeting for low output current ranges 10–40 mA. The prior buck regulator work with similar load current specifications is demonstrated in [13]. As discussed in Section I, either higher switching frequency or larger on-chip inductance is desired for low power fully integrated buck regulator. In [13], instead of using the on-chip inductor, a wirebond of 11.8 nH is utilized for the

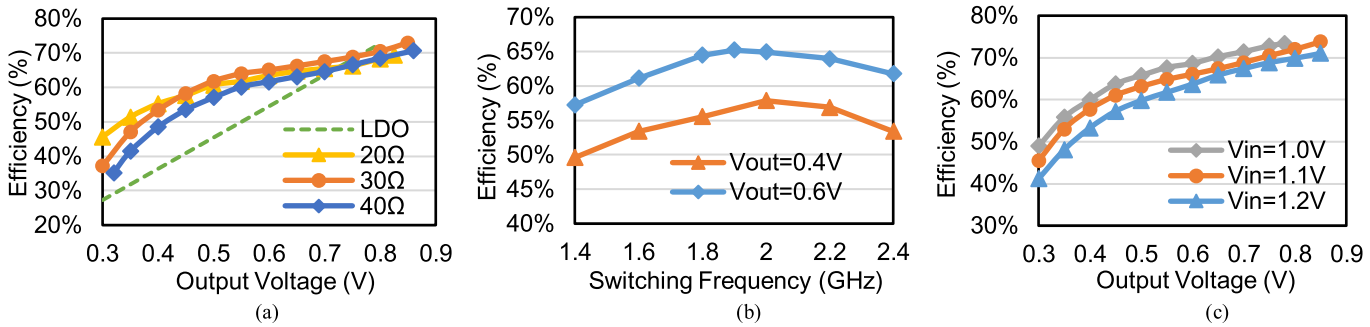


Fig. 16. Measured power efficiency versus (a) output voltage, (b) switching frequency, and (c) input voltage.

buck regulator, with a 71% peak efficiency. In this paper, the proposed buck regulator achieves 73% peak efficiency.

The proposed design is also compared with the previous SC regulator design with similar low-power design specification [7], [8]. For SC regulator, multiple configurations with different conversion ratio need to be implemented together to obtain wide output voltage range, which leading large design complexity. Although an 84% peak efficiency is reported in [8], it was obtained under a 1:1 conversion ratio, which operates as an LDO. For the SC operation configurations, only about 73% peak efficiency is obtained at 0.8 V. In another SC regulator, a peak efficiency of 80% is reported [7], while its area is more than 5× larger than the proposed design. Therefore, for the fully integrated regulator solutions, the SC regulator may obtain a little better (5%–10%) efficiency performance than the buck regulator solutions. However, the design complexity is much higher than buck regulator design, as multiple conversion configurations are required.

VI. Conclusion

This paper presents a fully integrated buck regulator design for low-power applications. The proposed buck regulator is designed with a switching frequency of 2 GHz, which is the highest switching frequency reported so far. The resonant switching scheme is utilized to form a resonant network between power switch gate and a resonant inductor to reduce the switching power loss. The proposed design is implemented in a 65-nm CMOS technology with 3 nH on-chip inductor. The measurement shows the output voltage in range of 0.3–0.86 V with input voltage 1.1 V. The proposed design achieves up to 73% power efficiency.

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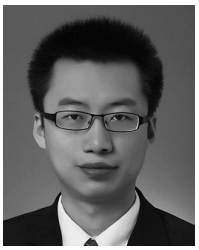

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