# A 2-GS/s 8-bit Non-Interleaved Time-Domain Flash ADC Based on Remainder Number System in 65-nm CMOS

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***Abstract*— A non-interleaved 2-GS/s, 8-bit flash analog-to-digital converter (ADC) utilizing the remainder number system (RNS) quantization principle is presented. The RNS quantization reduces the number of comparators and thus improves the figure of merit of the flash ADC. A time-domain implementation is adopted to reduce the ADC input capacitance with a voltage-to-time converter (VTC) front end. The ring oscillator-based time-to-digital converter (TDC) also provides a linear and efficient modulo (folding) operation for the RNS quantization with built-in dynamic element matching. Offline TDC mismatch calibration based on a histogram (code density) test is also employed to further improve the ADC linearity. The prototype RNS ADC was fabricated in a 65-nm CMOS process with an active area of 0.08 mm$^2$. It measures an SNDR of 40.7 dB for a Nyquist input and an effective resolution bandwidth of 1.74 GHz.**

***Index Terms*— Analog-to-digital converter (ADC), flash ADC, remainder number system (RNS), ring oscillator (RO), time domain (TD), time-to-digital converter (TDC), voltage-to-time converter (VTC).**

## I. Introduction

In ADVANCED pulsed/beamforming radar systems and digital signal processor (DSP)-based backplane/Ethernet receivers (Fig. 1), demanding performance is required for the analog front-end circuits, especially the analog-to-digital converter (ADC). For example, the pulsed/beamforming radar system [1]–[3] requires ADCs with a ≥8-bit resolution, a ≥2-GS/s sampling rate, and a large input bandwidth. The backplane/Ethernet receiver requires even higher sampling rates (e.g., 28 GS/s for PAM4 56-Gbps systems) with low bit error rates (BER) [4], [5]. Although time interleaving is inevitable to achieve such sampling rates, higher speed per sub-ADC is still preferred to avoid massive interleaving and to simplify the clock distribution and necessary calibration of the interleaving artifacts. The successive approximation register (SAR) and flash ADCs are two of the most common candidates in this regime. For the SAR ADC, its excellent power and area efficiencies are the main reasons why they are suitable for such applications. Meanwhile, the input loading of the SAR ADC is usually smaller than that of the flash ADC, making it easy to drive. However, its low conversion speed due to the looped operation and poor BER due to metastability result in severe challenges for SAR ADC arrays [6]. In contrast, the flash ADCs show advantages in speed and BER performance, in that its higher conversion speed obviates massive interleaving while open-loop latch pipelining [7] effectively reduces the BER of the flash ADC without significant speed degradation. What makes the flash ADC less attractive is its large power consumption, area, and input loading due to the exponential dependence of the comparator (CMP) number $N_C$ on the resolution $n$ ($N_C \approx 2^n$). For conventional gigahertz flash ADCs, the resolution is usually limited to 6–7 bits [8]–[11], even when signal folding is applied [12], [13].

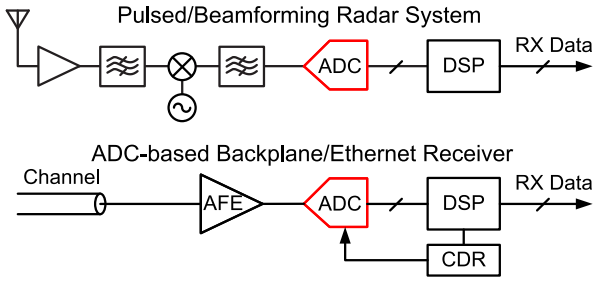


Fig. 1. Motivation.

In this paper, two techniques, a time-domain (TD) RNS quantizer and a voltage-to-time converter (VTC) front end are demonstrated to reduce the power/area consumption and input loading capacitance of an 8-bit, 2-GS/s flash ADC prototype without interleaving in 65-nm CMOS. The RNS architecture breaks the large flash quantizer into several small ones operating in parallel. Particularly, two small quantizers with 48 and 80 quantization levels produce a total of 240 levels (∼8 bits). Thus, the complexity and power consumption are greatly reduced. Meanwhile, a TD approach employing a VTC front end decouples the loading of the CMPs from the ADC input. It greatly broadens the input bandwidth of the ADC prototype. Simple inverters are employed as the VTC output buffers to drive the RNS quantizer instead of the power-hungry voltage-domain buffers commonly used in

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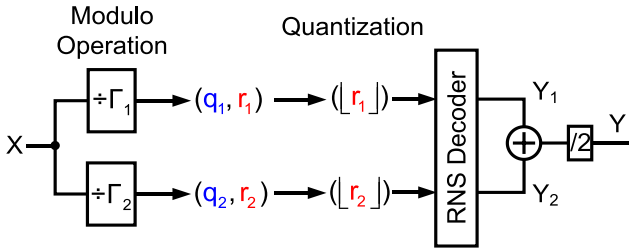


Fig. 2. Principle of RNS quantization.

TABLE I
RNS LUT WITH $\Gamma_1 = 3$ AND $\Gamma_2 = 5$

| X | 0-1 | 1-2 | 2-3 | 3-4 | 4-5 | 5-6 | 6-7 | 7-8 | 8-9 | 9-10 | 10-11 | 11-12 | 12-13 | 13-14 | 14-15 | 15-16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\lfloor r_1 \rfloor$ | **0** | 1 | 2 | 0 | 1 | 2 | 0 | 1 | 2 | 0 | 1 | 2 | 0 | 1 | 2 | **0** |
| $\lfloor r_2 \rfloor$ | **0** | 1 | 2 | 3 | 4 | 0 | 1 | 2 | 3 | 4 | 0 | 1 | 2 | 3 | 4 | **0** |

conventional flash ADCs. The prototype RNS ADC measures an SNDR of 40.7 dB for a Nyquist input and an effective resolution bandwidth (ERBW) of 1.74 GHz, reporting an outstanding figure of merit (FoM) among all flash/folding ADCs reported in the past decade.

This paper is organized as follows. Section II describes the fundamental theory of RNS quantization and its performance advantages. Section III explains the TD approach for the circuit realization of the RNS quantization. The details of the chip implementation are described in Section IV, followed by the measurement results in Section V. Finally, Section VI provides the conclusion.

## II. Principle of RNS Quantization

### A. Concept of RNS

The RNS is a non-weighted number system proposed by Garner [14] in 1959. Unlike the weighted number systems such as the binary number system, the RNS offers carry-propagation-free parallel arithmetic operation for addition, subtraction and multiplication [14], [15]. The concept of RNS quantization is shown in Fig. 2. By dividing a positive real number $X$ by $L$ positive integers $\{\Gamma_1, \Gamma_2, \ldots, \Gamma_L\}$, a set of quotients $\{q_1, q_2, \ldots, q_L\}$ and a set of remainders $\{r_1, r_2, \ldots, r_L\}$ are generated, where $\{q_i\} = \lfloor X/\{\Gamma_i\} \rfloor$ and $\{r_i\} = X \bmod \{\Gamma_i\}$, $i = 1, \ldots, L$. In RNS, the quantization of $X$ (i.e., $Y = \lfloor X \rfloor$) can be uniquely represented by the quantized remainders $\{\lfloor r_1 \rfloor, \lfloor r_2 \rfloor, \ldots, \lfloor r_L \rfloor\}$ if all the moduli $\{\Gamma_i\}$ are co-prime and $X$ is smaller than the full-scale range $\mathrm{FS} = \prod_{i=1}^{L} \Gamma_i$. If necessary, a digital RNS decoder can be used to further convert the quantization outcome $Y$ to either a binary or a decimal representation. The details of the RNS decoding algorithm are described in the Appendix. Alternatively, the remainder set $\{\lfloor r_i \rfloor\}$ can also be directly fed to an RNS DSP for a fast and totally parallel arithmetic operation [16], [17].

To give an intuitive example, let us assume two moduli $\Gamma_1 = 3$ and $\Gamma_2 = 5$. The input value and corresponding remainder values are listed in Table I. With an input $X$ of 8.3, we obtain $q_1 = 2$, $r_1 = 2.3$ and $q_2 = 1$, $r_2 = 3.3$. Thus, the integer part of the two remainders, $\lfloor r_1 \rfloor = 2$ and $\lfloor r_2 \rfloor = 3$, jointly represent 8, the quantized value of $X$.

The RNS quantizer provides two distinct advantages over the conventional flash-type quantizers. First, like subranging, the RNS quantization breaks a large quantizer into several small ones in parallel, which significantly reduces the architectural complexity of the flash quantizer. Let us consider the previous example again. All values within the range $[0, \mathrm{FS} = \Gamma_1\Gamma_2 = 15]$ can be quantized by $N_C = \Gamma_1 + \Gamma_2 = 8$ CMPs instead of 15 CMPs of a conventional 4-bit flash converter. In general, an $n$-bit RNS converter requires $\sim 2\sqrt{2^n}$ CMPs instead of $\sim 2^n$ ones of a full-flash converter for $L = 2$. Intuitively, the larger the number of remainders ($L$) the more hardware savings.

The second advantage of the RNS quantizer resides in the potential SNR gain due to the digital-domain output averaging. Naturally, with $L$ moduli, $L$ remainders are obtained and there are $L$ ways to obtain the final quantization outcome (see Appendix). Assuming that the quantization and circuit noises of the $L$ remainder generators are independent, a digital-domain averaging can be performed over the $L$ outcomes to suppress noise, i.e., the potential SNR improvement is

$$\Delta\mathrm{SNR} = \mathrm{SNR}\,|_L - \mathrm{SNR}\,|_1 = 10\log_{10} L. \tag{1}$$

### B. Redundancy in RNS Quantization

Albeit efficient, the RNS exhibits an error syndrome termed "aliasing." In Fig. 3(a), suppose that the remainder generation process is subject to an error, modeled as a small additive term $\Delta r_i$ to each remainder, i.e., $\hat{r}_i = r_i + \Delta r_i$. A behavioral simulation shows the transfer function (TF) of the RNS quantizer in Fig. 3(b) for $|\Delta r_i| \leq 1$. Besides the desired TF colored in blue, there are several parallel error bands. For example, with the same settings as in the previous example, let $\Delta r_1 = 1$ and $\Delta r_2 = -1$, then $r_1 = (2+1) \bmod 3 = 0$ and $r_2 = (3-1) \bmod 5 = 2$. The final outcome is $Y = 12$ instead of the correct value eight. Note that in a weighted number representation (i.e., binary and decimal), such alias error $\varepsilon_{\mathrm{alias}}$ does not present.

In practice, noise and analog imperfections are inevitable in a modulo operator (i.e., folding amplifier). Therefore, architectural redundancy is necessary to ensure the signal integrity in an RNS quantizer. The remainder redundancy [18] method is employed in this paper by introducing an integer common factor $M$ in every modulus as Fig. 3(a) shows. It has been proven that when an adequate $M$ is chosen, the RNS quantizer is robust to small remainder errors or circuit noise [18]. According to [18], $Y$ can be unconditionally correctly obtained if

$$M > 4|\Delta r_i|, \quad \text{for } 1 \leq i \leq L. \tag{2}$$

The TF of the RNS quantizer with $\Gamma_1 = 3$, $\Gamma_2 = 5$, $|\Delta r_i| = 3.9$, and $M = 16$ is shown in Fig. 3(c). In this case, all alias errors are eliminated. In addition, relative to the case $M = 1$, note that the full-scale (FS) range of the quantizer is also enlarged by $M$ times.

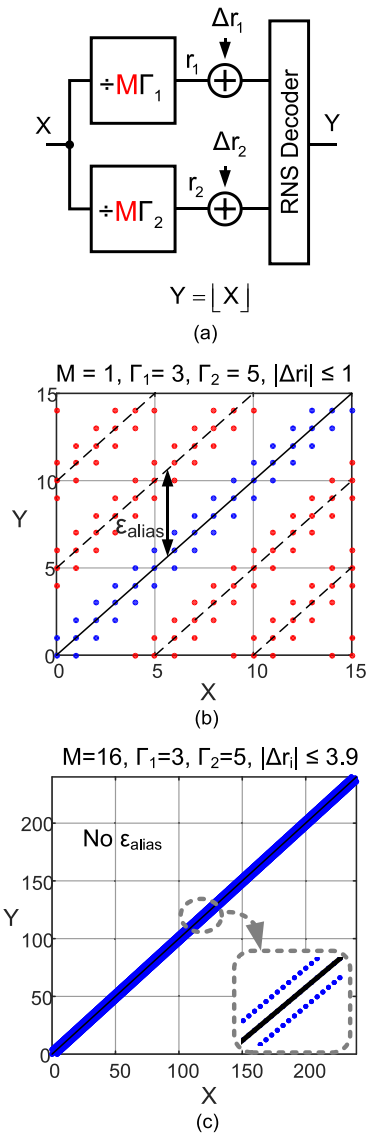


Fig. 3. (a) Redundant RNS quantizer with error/noise. (b) TF for $M = 1$, $\Gamma_1 = 3$, $\Gamma_2 = 5$, $|\Delta r_i| = 1$. (c) TF for $M = 16$, $\Gamma_1 = 3$, $\Gamma_2 = 5$, $|\Delta r_i| = 3.9$.

### C. Performance Gain of RNS Quantizer

With the redundancy factor $M$, we have

$$\begin{cases} \text{FS} = M \times \prod_{i=1}^{L} \Gamma_i \\ N_C = M \times \sum_{i=1}^{L} \Gamma_i. \end{cases} \tag{3}$$

For a certain FS and $M$, $N_C$ is minimized when all the moduli are approximately equal, i.e., $\Gamma_i \approx (\text{FS}/M)^{1/L} = (\prod_{i=1}^{L} \Gamma_i)^{1/L}$, according to the arithmetic mean–geometric mean inequality. For $M = 2^m$, we have

$$N_C \approx 2^m \times L \times \sqrt[L]{\frac{2^n}{2^m}} = L \times 2^{m+(n-m)/L}. \tag{4}$$

Fig. 4 shows the $N_C$ versus the resolution $n$ for $M = 16$ and the remainder number $L = 1$, 2, and 3. When $L = 1$, the quantizer degenerates to a conventional flash converter.

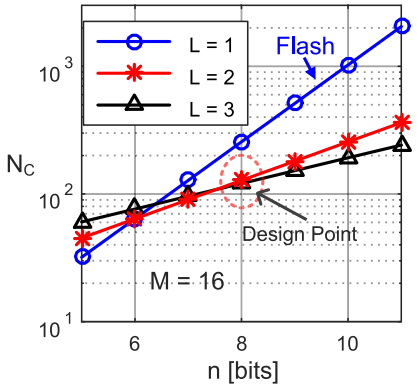


Fig. 4. CMP number ($N_C$) versus resolution $n$.

For $n \geq 8$, an RNS quantizer with two or more moduli can greatly reduce the $N_C$, resulting in large hardware savings.

The FoM of the RNS quantizer is of interest here. Two factors, the power consumption reduction by CMP number $N_C$ reduction and SNR improvement by result averaging, will improve the FoM of the RNS quantizer. The power consumption of the quantizer is proportional to $N_C$ while that of the modulo operator [i.e., ring oscillator (RO)] usually does not dominate. The RO is equivalent to the reference ladder in the conventional flash ADC. Thus, only the quantizer power is counted in the following derivation for simplicity. The Walden FoM is

$$\text{FoMw} = \frac{P}{f_S \times 2^{\text{ENOB}}} = \frac{P}{f_S \times 2^{\frac{\text{SNR}-1.76}{10\log 4}}}. \tag{5}$$

So, the RNS improvement of Walden FoM can be expressed as

$$\begin{aligned} \frac{\text{FoMw}}{\text{FoMw}\,|_{L=1}} &= \frac{P}{P\,|_{L=1}} \times \frac{1}{2^{\frac{\Delta\text{SNR}}{10\log 4}}} \\ &= \frac{L \times 2^{m+(n-m)/L}}{2^n} \times \frac{1}{2^{\frac{10\log L}{10\log 4}}} \\ &= \sqrt{L} \times 2^{(m-n)(1-1/L)}. \end{aligned} \tag{6}$$

This improvement is maximized for

$$L = (n - m)\ln 4. \tag{7}$$

Fig. 5(a) shows the Walden FoM improvement versus $L$ for 8- to 12-bit RNS quantizers with $M = 16$. Meanwhile, the Schreier FoM is

$$\text{FoMs} = \text{SNR} + 10\log\frac{\text{BW}}{P}. \tag{8}$$

So, the improvement in dB can be expressed as

$$\begin{aligned} \Delta\text{FoMs} &= \Delta\text{SNR} - 10\log_{10}\left(\frac{P}{P\,|_{L=1}}\right) \\ &= 10\log_{10} L - 10\log_{10}(L \times 2^{(m-n)(1-1/L)}) \\ &= 10\log_{10}(2^{(n-m)(1-1/L)}). \end{aligned} \tag{9}$$

The above analysis assumes that all the moduli are close to $\Gamma_i \approx (\text{FS}/M)^{1/L} = 2^{(n-m)/L}$. However, since the moduli also need to be co-prime, such a choice may not exist when $L$ is large. For example, for $n = 10$ and $m = 4$, $L$ can only

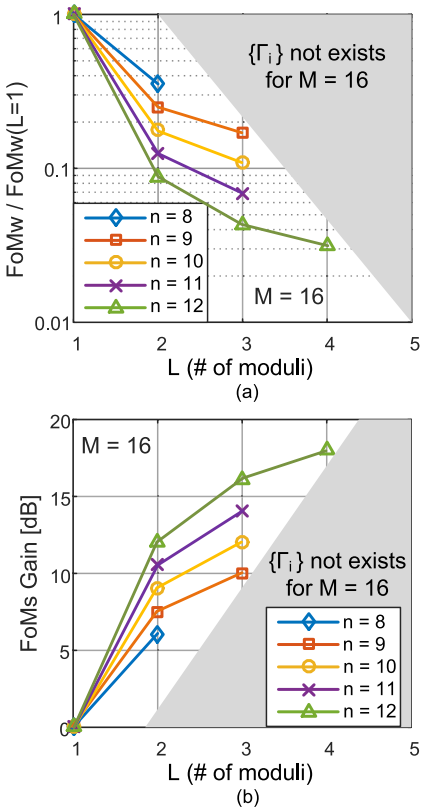


Fig. 5. FoM improvement of RNS quantizer. (a) Walden FoM improvement versus $L$. (b) Schreier FoM improvement versus $L$.

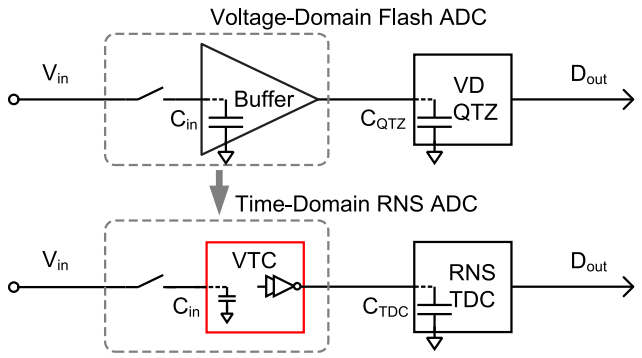


Fig. 6. $C_{in}$/power reduction of TD RNS ADC.

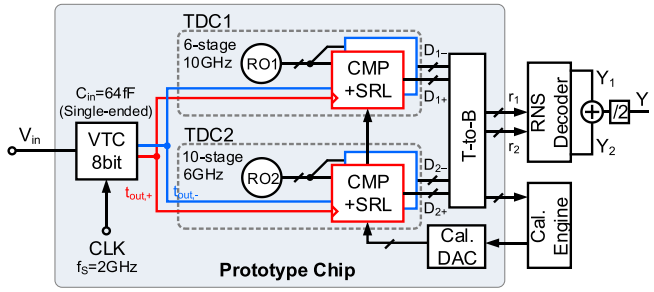


Fig. 7. Block diagram of RNS ADC prototype chip.

be 2 or 3, which gives rise to the moduli set of $\{7, 9\}$ or $\{3, 4, 5\}$, respectively. Furthermore, for $L = 4$, no valid moduli set can be found.

In this proof-of-concept design, for $n = 8$, a conservative $M = 16$ is chosen to tolerate $\pm$4-LSB noise and analog impairments in the remainder circuits. Thus, for $L = 2$, the only valid choice is $\Gamma_1 = 3$, $\Gamma_2 = 5$, which yields 240 quantization levels with an $N_C$ of $M \times (\Gamma_1 + \Gamma_2) = 128$. With a smaller $M$ or a larger $L$, more performance improvement can be achieved.

## III. Overall Architecture: A Time-Domain Approach

In this prototype, a TD circuit implementation is adopted. The benefits of a TD approach are: 1) to exploit the linear modulo or folding property of the RO and 2) to significantly reduce the input capacitance of the ADC (and thus power). The block diagrams of a conventional voltage-domain flash ADC and the TD RNS ADC are compared in Fig. 6. In the flash ADC, an input buffer is necessary to drive the voltage-domain quantizer. This buffer is power hungry due to its large static power to maintain a high sampling rate and good linearity. On the contrary, in this RNS ADC, simple inverters are employed at the VTC output to drive the trailing time-to-digital converter (TDC)—dynamic power dominates, and thus, it is more power efficient than voltage-domain buffers [19].

A critical part of the RNS quantizer is the remainder generator, which supports the modulo or signal folding operation. A persistent problem of the voltage-domain folding amplifier is its nonlinear transfer characteristic that limits the operation to only the vicinity of its center point where the linearity is good. In contrast, a TD RO is inherently linear in its folding characteristic [19], [20]. Therefore, it is more efficient than voltage-domain folding since the latter requires an increased number of folding amplifiers to form parallel folders for zero-crossing detection [21].

The overall system diagram of the RNS ADC prototype is sketched in Fig. 7. It consists of a front-end VTC, a backend TDC, a calibration DAC, and a thermometer-to-binary (T2B) converter. The calibration engine and the RNS decoder are implemented off-chip. At the core of the TDC are two sub-TDCs with a six-stage and a ten-stage pseudodifferential (PD) ROs as TD folders. The CMPs and the 4$\times$ set/reset latch (SRL) interpolators trailing the RO act as the TD quantizer. The raw thermometer codes of the TDC are then converted to the binary format and directly sent off-chip for further processing, including the histogram-based calibration. The RNS decoder finally converts the output data to weighted numbers for performance evaluation.

For the RNS decoder, the Appendix describes a computing-oriented (thus general) approach. For a specific design, a better way to realize the decoder is to employ a lookup table (LUT), similar to a conventional flash design wherein a ROM encoder is needed for converting the output to binary. The LUT design and thus power/complexity are similar to the conventional flash design.

Although [20] reports the first RNS TDC as a proof of concept, the design was not optimized. First, the redundancy in [20] is mainly realized by simply increasing the RO stage numbers, which is inefficient and power hungry. In this paper,

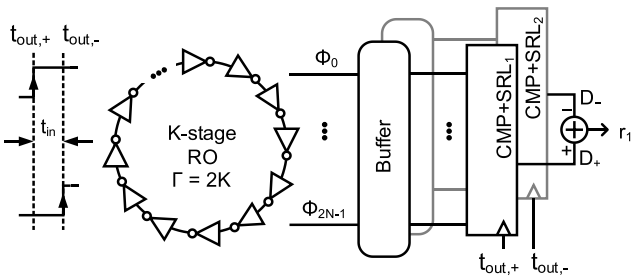


Fig. 8. Sub-TDC implementation.

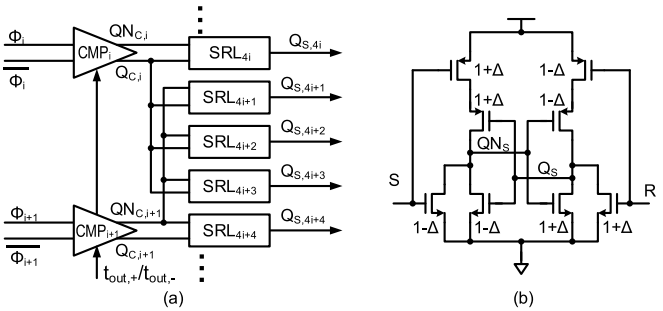


Fig. 9. (a) 4× SRL interpolation. (b) SRL with built-in skew.

the 4× redundancy is moved to interpolation, which not only reduces the power/area consumption, but also improves the conversion speed. Second, TDC calibration is introduced in this paper to enhance the RNS converter performance.

## IV. Circuit Implementation

### A. Time-to-Digital Converter

The block diagram of the sub-TDC is plotted in Fig. 8. In each sub-TDC, an RO functions as the TD signal folder. In normal operation, the RO phase (or state) represents the remainder of the measured time interval after the modulo operation. Two blocks (one for START and one for STOP) of CMPs and SRLs triggered by the differential output of the VTC, $t_{\text{out},+}$, and $t_{\text{out},-}$, respectively, trail each RO to record its phase status. In this paper, a 4× TD SRL interpolation [10] is employed to further cut down the $N_C$ from 128 to 32. Feed-forward inverters are used in the RO to reduce the TDC LSB size.

It is worthy to mention that a $K$-stage RO yields 2K states per cycle since both the rising edge and falling edge count. Taking a three-stage RO as an example, there are three nodes, $V_1$, $V_2$, and $V_3$. The voltage combination $\{V_1, \overline{V_2}, V_3\}$ circulates from $\{0, 0, 0\}$, $\{1, 0, 0\}$, $\{1, 1, 0\}$, $\{1, 1, 1\}$, $\{0, 1, 1\}$ to $\{0, 0, 1\}$. So, the RO provides an inherent redundancy factor of 2 [21]. Therefore, the six-stage and ten-stage ROs in this design represent $\Gamma_1 = 3$ and $\Gamma_2 = 5$ with a redundancy factor $M = 4$. The remaining 4× redundancy factor is provided by the 4× SRL interpolations.

The final quantization outcome is derived by differencing the digital codes of the two CMP + SRL blocks. The bipolar input time ($t_{\text{out},+} - t_{\text{out},-}$) further helps to halve the absolute conversion range, improving the speed of the TDC [21]. The double sampling and free running RO also provides an inherent dynamic element matching (DEM) effect at the cost of 3-dB SNR penalty [20], which is compensated by averaging the output data $Y_1$ and $Y_2$ in this paper.

The 4× TD SRL interpolation [10] is more power efficient than the shorted-inverter-based [22] or resistor-ladder-based interpolators [23], since the latter ones do not reduce $N_C$. As shown in Fig. 9, three SRLs (NOR gate-based) with a built-in timing skew are inserted between the outputs of two adjacent CMPs. When the RO phase is close to the middle of $\Phi_i$ and $\Phi_{i+1}$, $Q_{C,i}$ and $QN_{C,i+1}$ are two falling edges. By skew the sizing of the NOR gate, the trip voltage of the SRL is skewed. Assuming the falling edges of $Q_{C,i}$ and $QN_{C,i+1}$ have consistent slope, the skewed trip voltage is then equivalent to a timing skew by $t_{\text{skew}} = V_{\text{trip,skew}}/\text{slope}$. The timing skews of the three SRLs are set to $\{-\text{LSB}, 0, \text{LSB}\}$.

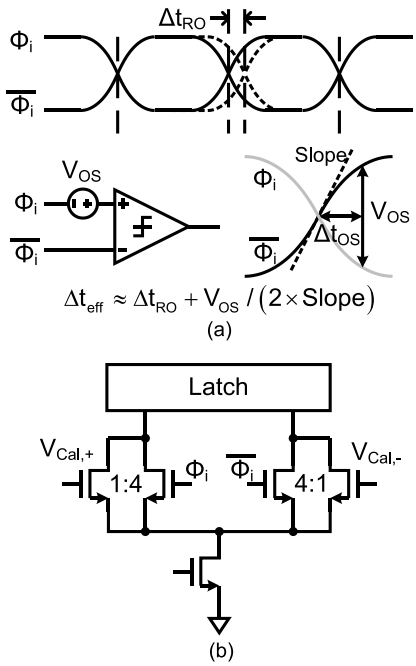


Fig. 10. TDC calibration. (a) Lumped RO + CMP mismatch model. (b) Auxiliary input pair of CMP.

### B. TDC Mismatch Calibration

Fig. 10(a) shows the lumped RO + CMP mismatch model of the TDC. First, the differential phase pair $\Phi_i$ and $\Phi_{i\_}$ of the RO introduces a zero-crossing point shift $\Delta t_{\text{RO}}$ due to mismatch. Second, the CMP input-referred offset voltage $V_{\text{OS}}$ also results in a time offset $\Delta t_{\text{OS}}$. If we define the effective time error of the TDC as $\Delta t_{\text{eff}}$, then

$$\Delta t_{\text{eff}} = \Delta t_{\text{RO}} + \Delta t_{\text{OS}} \approx \Delta t_{\text{RO}} + V_{\text{OS}}/(2 \times \text{Slope}). \quad (10)$$

Monte Carlo simulation suggests a 1.61-ps standard deviation of $\Delta t_{\text{OS}}$ and a 1.28-ps standard deviation of $\Delta t_{\text{RO}}$. As a result, $\Delta t_{\text{eff}}$ exhibits a standard deviation of 2.06 ps. For an LSB size of 2 ps, the ±4-LSB redundancy thus corresponds to $\pm 4\sigma$ of the random TD offset. While this is considered

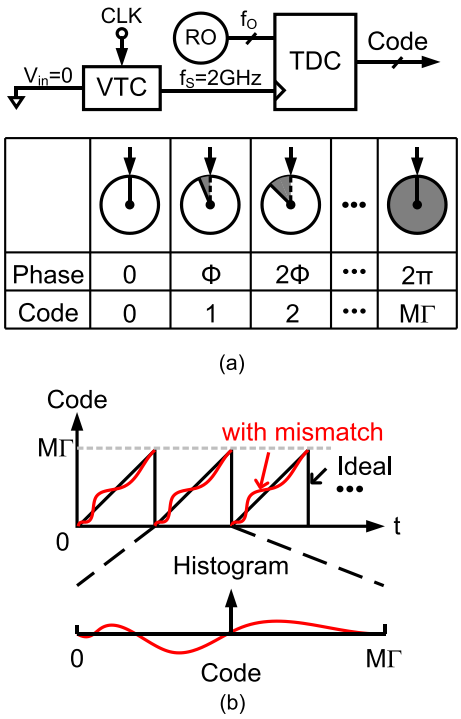


Fig. 11. TDC INL extraction. (a) Linear TD ramp generation. (b) Histogram-based extraction.

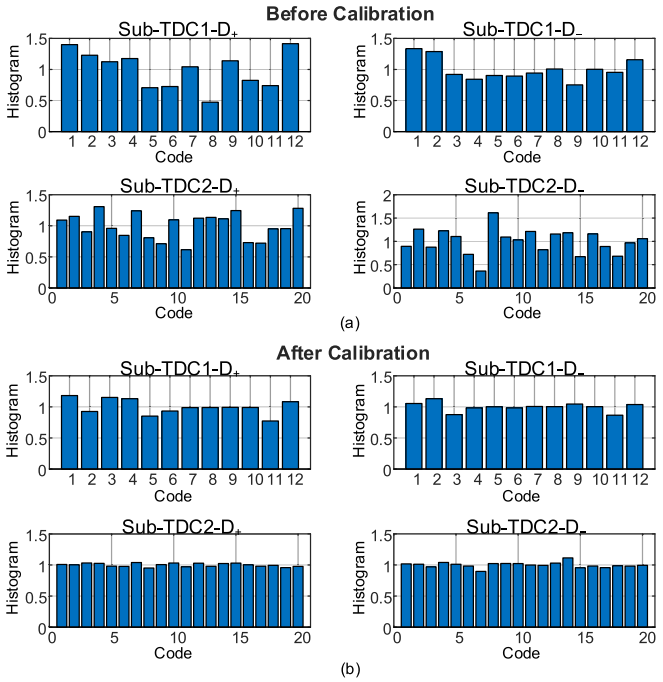


Fig. 12. Measured normalized histogram of TDC's CMP arrays (a) before calibration and (b) after calibration.

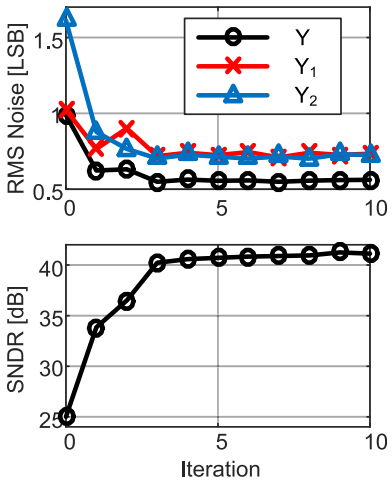


Fig. 13. Calibration convergence curves of RMS noise and SNDR.

mostly sufficient, we employed a digital calibration option to further reduce the RO mismatch and the CMP offset effect. As shown in Fig. 10(b), an auxiliary input pair controlled by a DAC is added to each CMP for mismatch calibration. The size of the auxiliary input pair is a quarter of the main pair. A calibration DAC with a 5-bit resolution is employed to provide ±5 LSB calibration range (∼300 mV) with an accuracy of 0.3 LSB. The SRLs are left un-calibrated with an RMS noise of 0.26 LSB after DEM.

To extract the TDC mismatch, a linear TD ramp is fed to the TDC as Fig. 11(a) illustrates. By leaving the RO free running and setting the VTC input to zero, the VTC's output is a copy of sampling clock $f_S$ without any phase variation. When the RO frequency $f_O$ is different with multiple of $f_S$, the RO frequency $f_O$ will beat with $f_S$. The RO phase will then accumulate linearly and all TDC's raw codes $D_+/D_-$ (not $r_1$ or $r_2$, the remainders after subtraction) will be hit periodically. The histogram of the raw codes directly reflects the integral nonlinearity (INL) of the TDC as shown in Fig. 11(b), which is employed to control the calibration DAC after digital processing.

Fig. 12(a) and (b) plots the measured histogram of the four CMP blocks of the TDC, before and after calibration, respectively. The calibration DAC voltage is adjusted iteratively during the calibration. At the $j$th iteration, $V_{\text{cal}}$ is given as

$$\begin{cases} V_{\text{cal},j+1} = V_{\text{cal},j} + \mu \times g_{\text{cal}} \times H_{\text{cal},j} \\ V_{\text{cal},0} = 0 \end{cases} \tag{11}$$

where $H_{\text{cal},j}$ is the histogram of the $j$th iteration, $g_{\text{cal}}$ is the gain from the histogram to voltage and $\mu$ is the step size. With $\mu = 0.6$–$0.8$, the lowest SNR fluctuation or the best calibration accuracy can be achieved. Fig. 13 plots the measured RMS noise (in calibration mode) and the corresponding SNDR (in normal mode) versus the iteration cycle. At the beginning, a large TDC RMS noise due to mismatch is observed, resulting in a large SNDR drop due to $\varepsilon_{\text{alias}}$. After a few iterations, the noise converges to 0.56 LSB and the SNDR reaches 41 dB.

The RMS noise of the $Y_1$ after calibration is about 0.72 LSB, which is a bit larger than the simulated value. This is caused by incomplete calibration due to an underestimated the TDC mismatch from layout and routing. As shown in Fig. 12(b), some residual histogram non-uniformity of the sub-TDC1-1 CMPs after calibration still exists. This can be easily addressed

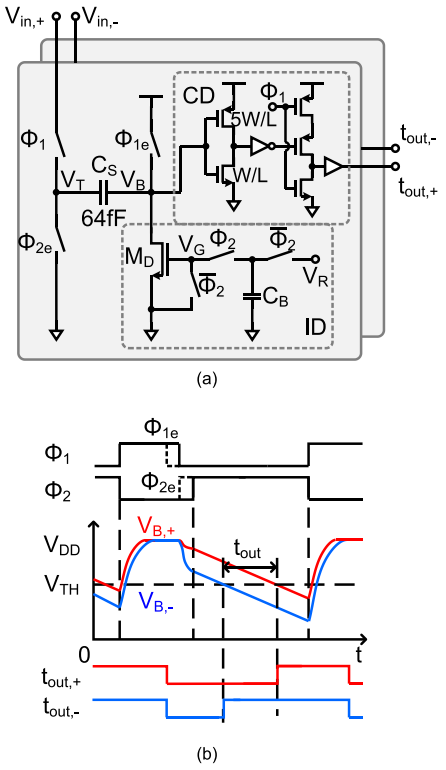


Fig. 14. VTC (a) circuit diagram and (b) timing diagram.

in the future by increasing the size of the auxiliary input pair or the calibration DAC range.

### C. Voltage-to-Time Converter

A constant-current discharging VTC is employed in this paper to achieve a 2-GS/s sampling rate and 8-bit linearity. The circuit and timing diagrams of the VTC are shown in Fig. 14. The PD VTC contains two identical half circuits to convert $V_{\text{in},+}/V_{\text{in},-}$ to $t_{\text{out},+}/t_{\text{out},-}$, respectively. It contains three parts, a sample-and-hold, a discharger (ID), and a crossing detector (CD). The input voltage is bottom plate sampled onto $C_S$ and then discharged by ID with a constant current. Last, the CD generates a rising edge $t_{\text{out},+}/t_{\text{out},-}$, corresponding to the differential input voltages. To the first order, since both the sampling and constant-current discharging processes are linear, this VTC presents better linearity than the current-starved inverter-based VTCs [24], [25].

In the ID, $C_B$ is charged to a reference voltage $V_R$ while $V_G$ is discharged to zero when $\Phi_2$ is low. Then $V_G$ is biased to a constant value when $\Phi_2$ goes high and $C_B$ shares its charge with the $C_{\text{gs}}$ of $M_D$. So, $V_R$ sets the gain of the VTC. The VTC's linearity relies on the constancy of the discharging current. To improve the linearity, the channel length of $M_D$ is set to 500 nm. In addition, the trip point of the CD, $V_{\text{TH}}$, is skewed up to 650 mV to prevent $M_D$ entering the triode region before the rising edges $t_{\text{out},\pm}$ are generated. Simple inverters are used in the CD. Due to the PD topology, process, voltage, and temperature (PVT) variations only introduce a static offset in $t_{\text{out},\pm}$. Simulation reveals a peak offset time of $\pm 16$ ps or $\pm 8$ LSBs. The spurious-free dynamic range (SFDR) and total harmonic distortion (THD)

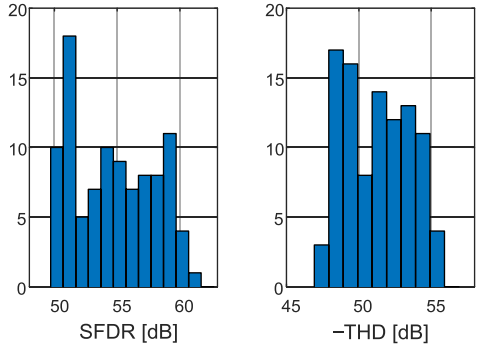


Fig. 15. Post-layout Monte Carlo simulation of SFDR and THD of the VTC.

of the VTC are simulated with process variation and mismatch. As shown in Fig. 15, an SFDR above 50 dB and a THD better than $-47$ dB are achieved with a low-frequency input.

Relative to the large input capacitance of a conventional flash ADC, the size of $C_S$ in the VTC is primarily determined by the noise requirement. Thus, the input bandwidth of this paper is greatly expanded. According to [21], the input-referred noise of the VTC is

$$V_{n,\text{in}}^2 = \frac{2kT}{C_S}\left(1 + 2\gamma\frac{V_{\text{DD}}}{V_{\text{ov},D}}\right) \tag{12}$$

where $\gamma$ and $V_{\text{ov}}$ are the thermal noise coefficient and the overdrive voltage of $M_D$. With an input swing of 1.2 $V_{\text{P-P,diff}}$ and a $C_S$ of 64-fF single ended, the SNR of the VTC is 48 dB.

### D. Layout Floor Plan and T2B Decoder

To maintain good linearity, the loading of each CMP's input node and output node needs to be as uniform as possible in layout. So, the CMPs need to be placed in a circular fashion. One possible way is to split the CMP array into two up-and-down blocks as done in [20]. In that paper, each RO stage is placed close to its corresponding CMP. However, since the dimension of the CMP is much larger than that of the RO stage, such floor plan will result in the RO stages far from each other, leading to extra loading of the RO. In this paper, the CMP array is placed in four sides of a rectangle surrounding the RO, like a real "ring."

The raw data of the TDC (thermometer code) is converted to the binary format on-chip before it is sent off-chip. In flash ADCs, several types of T2B encoders can be adopted, such as the ROM-based encoder [20], Wallace tree encoder [26], and fat tree encoder [27]. However, due to the layout floor plan mentioned above, the encoder must be routed across the entire outer perimeter of the TDC, resulting in extra loading and thus power consumption. To resolve this problem, a split fat tree encoder is employed. It consists of a one-hot encoder, 4-bit fat tree units and a multiplexer.

The outputs of the sub-TDC are grouped together every 16 codes. The fat tree encoder is split into several (three for sub-TDC1 and five for sub-TDC2) 4-bit units corresponding to the grouped sub-TDC outputs. These units generate 5-bit outputs $\{b_{1,1}[4:0], \ldots, b_{1,3}[4:0]\}$ for sub-TDC1. $\{b_{1,1}[4], b_{1,2}[4], b_{1,3}[4]\}$ are then used to select $\{b_{1,1}[3:0], \ldots, b_{1,3}[3:0]\}$ with a 3-to-1 multiplexer. A similar scheme

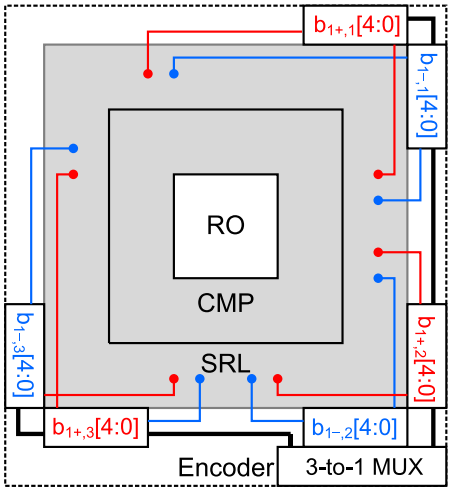


Fig. 16. Layout floor plan of sub-TDC1.

TABLE II
ADC NOISE BUDGET

| Source | | RMS Noise [LSB] | |
|---|---|---|---|
| | | Not averaged | Averaged |
| VTC | | 0.27 | 0.27 |
| TDC | RO | 0.10~0.165 | 0.10/√2~0.165/√2 |
| | CMP | 0.049 | 0.049/√2 |
| | SRL | 0.10 | 0.10/√2 |
| | $\varepsilon_q$ | 0.41 | 0.41/√2 |
| | DEM | 0.37 | 0.37/√2 |
| Total | | 0.63~0.65 | 0.49 |

for sub-TDC2 is used. In this way, only the 5-bit outputs are wired out of each unit. The one-hot encoder employs a three-input AND gate to suppress bubbles. The layout floor plan of sub-TDC1 is illustrated in Fig. 16.

### *E. ADC Noise Budget*

The noise budget of each block of the RNS ADC prototype is listed in Table II. The quantization noise is $\varepsilon_q = (2 \times (1/12))^{1/2} = 0.41$ LSBs due to the double sampling. The DEM transforms the TDC mismatch to white noise. Consider the un-calibrated SRL mismatch and calibration accuracy, the RMS noise introduced by DEM is about 0.37 LSBs. It indicates a total RMS noise of 0.63 LSBs (for a zero input) to 0.65 LSBs (for a full-scale input). The larger full-scale noise is caused by the cumulative jitter of the RO. With output averaging, all noise powers except the VTC noise are halved. With a full scale of ±120 LSBs, the peak SNR is about 44.8 dB.

## V. MEASUREMENT RESULTS

The prototype RNS ADC is fabricated in a 65-nm CMOS process with an active area of 0.08 mm$^2$ (380 $\mu$m × 210 $\mu$m) [28]. A die photograph is shown in Fig. 17. At 2 GS/s, the measured power consumption is 21 mW. A breakdown of the power consumption is shown in Fig. 18. The VTC and clock generator consumes 1.9 mW at a 1.2-V supply, indicating high power efficiency of the TD approach compared to the input T/H of the conventional flash converter.

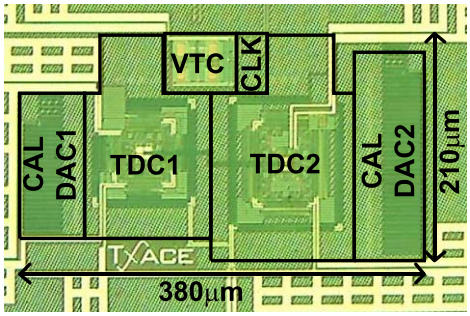


Fig. 17. Die photograph.

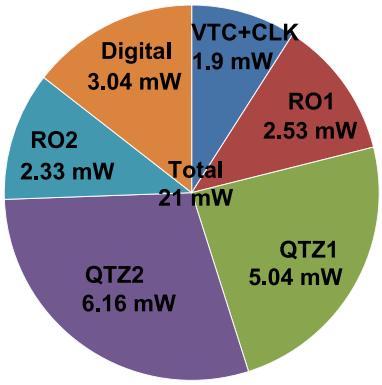


Fig. 18. Power breakdown.

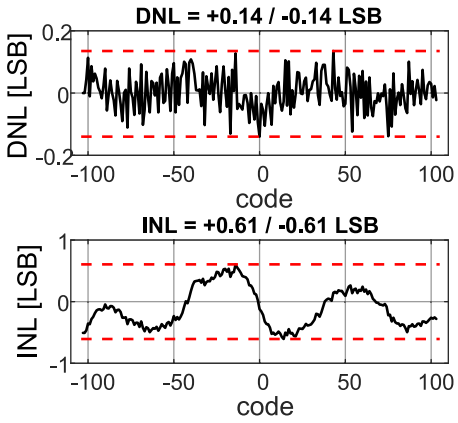


Fig. 19. Measured DNL and INL plots.

TDC1 and TDC2 consume 7.6 and 8.5 mW at a 1.3-V supply, respectively. Both ROs consume similar power due to their identical stage delays. The digital circuits consume 3 mW at a 1.2-V supply.

Thanks to the DEM, the measured differential nonlinearity (DNL) and INL after calibration (Fig. 19) are ±0.14 and ±0.61 LSBs, respectively. The ADC achieves a 41.2-dB SNDR for a low-frequency input and a 40.7-dB SNDR for a Nyquist input. Fig. 20(a) and (b) shows the measured ADC spectra with a 100-MHz input and a Nyquist input, respectively. The SFDR and THD are mainly limited by the INL of the VTC. Fig. 21 plots the dynamic performance of the ADC, revealing an ERBW of 1.74 GHz. The measured ERBW is limited by the input network, such as bonding pad capacitance.

TABLE III
PERFORMANCE COMPARISON

| | **This Work** | ISSCC'14 [13] | VLSI'12 [8] | VLSI'13 [9] | ASSCC'15 [10] | VLSI'09 [12] |
|---|---|---|---|---|---|---|
| Architecture | **RNS TD** | Folding TD | Flash | Flash | Flash | Folding |
| Technology | **65nm** | 40nm | 40nm | 32nm SOI | 65nm | 90nm |
| Sample Rate (GS/s) | **2** | 2.2 | 3 | 5 | 3.4 | 2.7 |
| Resolution (Bits) | **7.93** | 7 | 6 | 6 | 6 | 6 |
| Input Cap. (fF) | **128** | 300 | 72 | 135 | 120 | NA |
| Input Range ($V_{P-P}$) | **1.2** | 1.0 | 0.5 | NA | 0.8 | 0.8 |
| Bandwidth (GHz) | **1.74** | 1.2 | 1.5 | 2.5 | 1.8 | 1.35 |
| SNDR (dB) @NQ | **40.7** | 37.4 | 33.1 | 30.9 | 34.2 | 33.6 |
| ENOB (Bits) @NQ | **6.5** | 5.9 | 5.2 | 4.8 | 5.4 | 5.3 |
| DNL/INL (LSB) | **0.14/0.61** | 0.6/1.0 | NA/0.35 | 0.52/0.37 | 0.48/0.64 | 0.53/0.73 |
| Supply Voltage (V) | **1.2/1.3** | 1.1 | 1.1 | 0.85 | 1.0 | 1.0 |
| Power (mW) | **21** | 27.4 | 11 | 8.5 | 12.6 | 50 |
| Area ($mm^2$) | **0.08** | 0.052 | 0.021 | 0.02 | 0.034 | 0.36 |
| Walden FoM (fJ/step) | **119** | 210 | 100 | 59.4 | 89 | 470 |
| Schreier FoM (dB) | **150.6** | 143.3 | 144.4 | 145.6 | 145.7 | 137.9 |

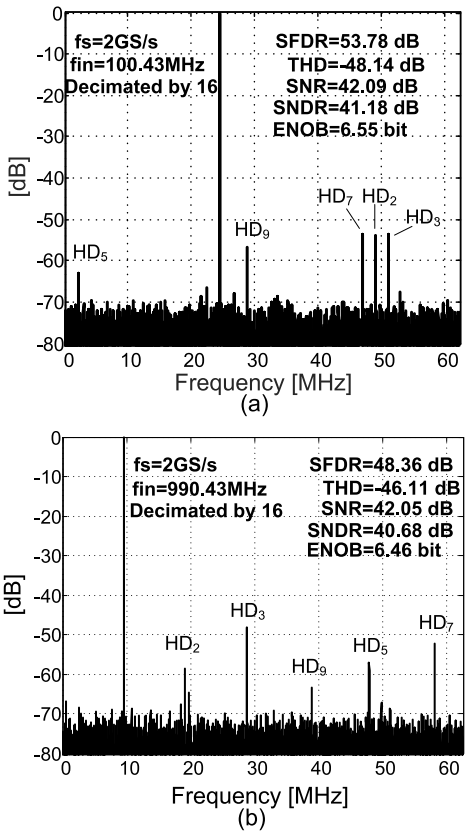


Fig. 20. Measured output spectra at 2 GS/s for (a) low-frequency input and (b) Nyquist input.

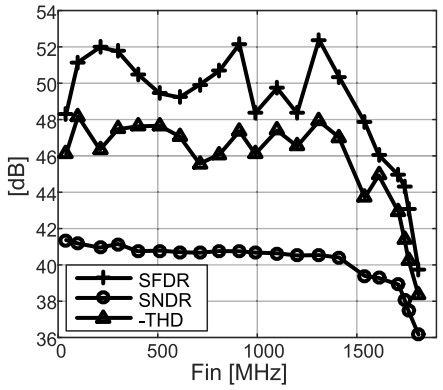


Fig. 21. Measured ADC dynamic performance.

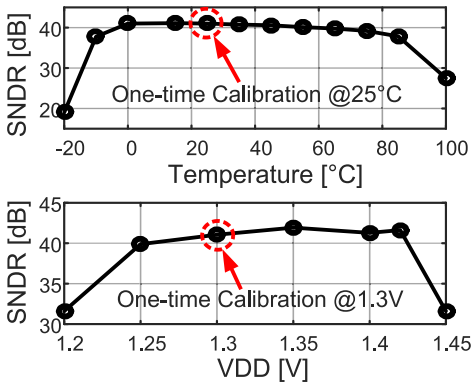


Fig. 22. Measured SNDR versus temperature and voltage variations.

Fig. 22 shows the measured SNDR ($F_{\text{in}} = 100$ MHz and $F_s = 2$ GHz) versus the temperature and supply voltage variations after a one-time calibration performed at 25 °C with a 1.3-V supply. A less than 1-dB SNDR variation is observed from 0 °C to 60 °C and from 1.3 to 1.42 V. Since the VTC conversion gain and the TDC LSB size display the same dependence on the temperature and supply voltage, they automatically track each other and the overall ADC displays very small sensitivity to the temperature and voltage variations. The residual SNDR variation is mostly caused by the RO frequency ($f_O$) variation (the lower the $f$o, the lower the SNDR). Because of the mobility's temperature dependence, the $f_O$ or SNDR exhibits a CTAT characteristic [29]. Similarly, a larger supply voltage will give rise to a higher $f_O$ and SNDR.

The performance of the RNS ADC prototype is summarized and compared with the state-of-the-art non-interleaved >6-bit, >1-GS/s flash/folding ADCs in Table III. This paper

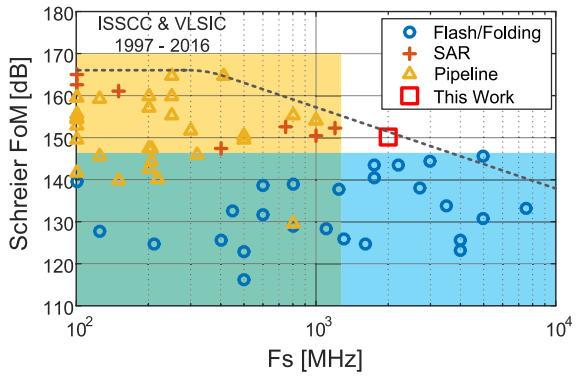


Fig. 23. Schreier FoM versus sampling rate of non-interleaved ADCs.

reports the first non-interleaved 8-bit flash ADC achieving a 2-GS/s sampling rate in CMOS technology. Thanks to the VTC front end, a small input capacitance is achieved. In summary, the RNS architecture provides a prominent SNDR and FoM, e.g., the best Schreier FoM, among all non-interleaved flash/folding ADCs published at ISSCC and VLSI from 1997 to 2016 [30] as shown in Fig. 23.

## VI. Conclusion

A flash ADC employing the RNS quantization principle is reported. It achieves a 2-GS/s sampling rate and an 8-bit resolution without time interleaving in 65-nm CMOS. The RNS quantization reduces the number of CMPs and improves the power efficiency of the converter. A TD approach also helps to cut down the input capacitance and to broaden the ERBW to 1.74 GHz. Furthermore, the RO-based TDC also provides a linear modulo operation and inherent DEM. A histogram-based TDC mismatch calibration is employed to improve the ADC performance. The prototype achieves an SNDR of 40.7 dB for a Nyquist input. This paper reports the best Schreier FoM among all non-interleaved flash/folding ADCs published at ISSCC and VLSI from 1997 to 2016.

## Appendix

Given collectively all the remainders $\{r_i\}$, several algorithms exist for decoding, such as the Chinese remainder theorem (CRT) and the mixed-radix conversion [15]. In this paper, the closed-form robust CRT [18] is used to decode RNS with redundancy. For a specific design, the decoder can also be realized by an LUT by pre-calculating the values with the following algorithm.

To convert the RNS into a weighted number system, $Y_i$ can be calculated from one remainder and the corresponding quotient, wherein the quotient is derived from the remainders and the moduli. So, $L$-decoded values $\{Y_i\}$ are obtained, one for each remainder

$$\begin{cases} Y_1 = q_1\Gamma_1 M + \hat{r}_1 \\ Y_2 = q_2\Gamma_2 M + \hat{r}_2 \\ \quad\vdots \\ Y_L = q_L\Gamma_L M + \hat{r}_L. \end{cases} \tag{13}$$

The quotients can be calculated as

$$\begin{cases} q_1 = \displaystyle\sum_{i=2}^{L}\left[\left(\xi_{i,1}b_{i,1}\frac{\Gamma}{\Gamma_1\Gamma_i}\right) \bmod \left(\frac{\Gamma}{\Gamma_1}\right)\right], & i = 1 \\ q_i = \dfrac{q_1\Gamma_1 - \hat{r}_{i,1}}{\Gamma_i}, & i > 1 \end{cases} \tag{14}$$

and

$$\begin{cases} \xi_{i,1} = (g_{i,1}\hat{r}_{i,1}) \bmod \Gamma_i \\ r_{i,1} = \left\| \dfrac{\hat{r}_i - \hat{r}_1}{M} \right\| \\ g_{i,1} \equiv \Gamma_1^{-1} (\bmod\ \Gamma_i) \qquad 2 \le i \le L \\ b_{i,1} \equiv \left(\dfrac{\Gamma}{\Gamma_1\Gamma_i}\right)^{-1} (\bmod\ \Gamma_i), \end{cases} \tag{15}$$

where $\|x\|$ is the rounding function and $y \equiv x^{-1}(\bmod\ R)$ is the modular multiplicative inverse operation, which is defined by

$$y \equiv x^{-1}(\bmod\ R) \Leftrightarrow (xy) \bmod (R) = 1. \tag{16}$$

The parameter $g_{i,1}$ and $b_{i,1}$ are constants, which can be pre-calculated to simplify the decoding process. In this design, $\Gamma_1 = 3$, $\Gamma_2 = 5$, and $M = 16$ are chosen. So

$$\begin{cases} g_{2,1} = 2 \\ b_{2,1} = 1. \end{cases} \tag{17}$$

Then

$$\begin{cases} q_1 = (2\hat{r}_{2,1}) \bmod \Gamma_2 \\ q_2 = \dfrac{q_1\Gamma_1 - \hat{r}_{2,1}}{\Gamma_2} = (-2\hat{r}_{2,1}) \bmod \Gamma_1. \end{cases} \tag{18}$$

For instance, if $X = 124.3$, then $r_1 = 28$ and $r_2 = 44$. So, $\widehat{r}_{2,1} = 1$ and $q_1 = 2$, $q_2 = 1$. The decoded values are $Y_1 = 3 \times 16 \times 2 + 28 = 124$ and $Y_2 = 5 \times 16 \times 1 + 44 = 124$. When considering noise in the remainders, i.e., $\Delta r_1 = 0.2$ and $\Delta r_2 = -0.3$, then $Y_1 = 124.2$ and $Y_2 = 123.7$ are obtained.

From the analysis and example above, we can observe that the noise of the decoded value $Y_{\rm i}$ only depends on the noise in the corresponding remainder $\widehat{r_i}$. Thus, a final averaging can be performed across all $L$-decoded values $\{Y_i\}$ (Fig. 2), resulting in improved SNR performance.

## Acknowledgment

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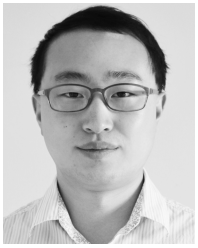

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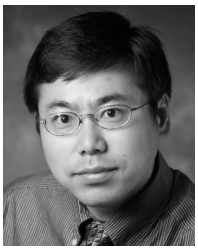

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