

# Compensator-Free Mixed-Ripple Adaptive On-Time Controlled Boost Converter

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**Abstract**—A mixed-ripple adaptive on-time controlled boost converter is proposed. With the proposed control method, the compensator network is no longer required. Hence, the chip area and cost can be reduced, and a satisfied load regulation still can be achieved. Besides, a novel on-time generator is proposed to fix the switching frequency in continuous conduction mode (CCM). Moreover, a differential difference comparator is proposed to simplify the circuits and further reduce chip area. Furthermore, with the proposed control, the converter is capable of smoothly switching between discontinuous conduction mode and CCM, depending on the loading condition. The proposed boost converter was implemented by using a 0.18- $\mu\text{m}$  1P6M mixed-signal process, and the chip area is 0.88 mm<sup>2</sup>. The input voltage may range from 0.8 to 1.4 V, the output voltage is set to 1.8 V, and the measured peak efficiency is 92.4%.

**Index Terms**—Adaptive on-time (AOT), boost converter, dc-dc power converter, power management, ripple-based control.

## I. INTRODUCTION

NOWADAYS, single-cell batteries are widely used as the power supply for portable electronic devices, such as medical diagnostic equipment and wireless headset [1]. The output voltage of a NiMH battery is around 1.2 V, and an alkaline battery offers a voltage ranging from 0.8 to 1.5 V. However, many mixed-signal systems of portable devices are still powered by 1.8 or 3.3 V. Therefore, these circuits cannot be powered directly by a single-cell battery. To overcome this barrier, boost dc-dc converters offer a popular solution to step up the battery voltage to a proper value [2]. Moreover, because long service time, small size, and low cost are desired for battery-powered portable devices, their dc-dc converters are required to have a high conversion efficiency, minimize the number of external components (e.g., capacitors and inductors), and be cost-effective, which means to make the chip area of their control circuits as small as possible.

In recent years, ripple-based controls, such as hysteretic and constant on/off-time control, have been receiving more and more attention because of their simple architecture and high efficiency over a wide load range [3]. However, their switching

Manuscript received April 10, 2017; revised July 17, 2017; accepted September 12, 2017. Date of publication October 18, 2017; date of current version January 25, 2018. This work was supported by the Ministry of Science and Technology, Taiwan, under Grant MOST 105-2628-E-006-008-MY3. The chip fabrication was supported by the National Chip Implementation Center, Taiwan. This paper was approved by Associate Editor Pavan Kumar Hanumolu. (*Corresponding author: Chia-Ling Wei*)

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Digital Object Identifier 10.1109/JSSC.2017.2756871

frequencies would vary with load current, which is not preferred for electromagnetic interference issues. Hence, adaptive on-time (AOT) controls are proposed for buck converters because their switching frequency can be quasi-fixed in the continuous conduction mode (CCM). On the other hand, in the discontinuous conduction mode (DCM), which usually occurs at light load, AOT control is similar to pulse-frequency modulation control, so high efficiency can be achieved at light load.

In addition, the fundamental principle of ripple-based controls is to regulate the output voltage directly by limiting the size of their output ripples, and no compensators are required. It works fine in buck converters because their output voltage ripples are in phase with the inductor current. However, for boost converters, the output voltage ripple and inductor current are out of phase, which makes it impractical to use only the output voltage as the feedback signal [4], [5]. To overcome this obstacle, the information of inductor current is also required and compensators cannot be removed [6]–[9]. In fact, in DCM, an on-time controlled boost converter without sensing inductor current can work stably, because the signal of zero inductor current, which can be detected by only using a comparator, can be used with the output voltage to determine the off-time length [10]. However, the inductor current never goes to zero in CCM, so the inductor current should be sensed for working in CCM. Fig. 1(a) shows the conventional current-mode AOT-controlled boost converter, which adopts a type-II compensator network and generates an error signal  $V_E$  to compare with the valley of the inductor current. The transient response of current-mode AOT control is shown in Fig. 1(b). Even worse, the compensator may include off-chip components. As a consequence, the cost and area of the whole converter are increased. To alleviate this problem, several on-chip compensation techniques have been proposed, such as capacitor multiplier [11], [12]. However, these techniques inevitable require extra power consumptions and increase chip area. For example, the on-chip compensator in [7] and [13] occupies approximately 23% and 32% of the chip area for the control circuits, respectively.

In this paper, a mixed-ripple AOT (MRAOT)-controlled boost converter is proposed and implemented by using TSMC 0.18- $\mu\text{m}$  CMOS mixed-signal process. The circuit of the proposed MRAOT control method can be implemented without any compensator, so the chip area can be reduced. Moreover, the converter is capable of switching between CCM and DCM smoothly, depending on the load current. Furthermore, a novel on-time generator is proposed to fix the switching frequency in CCM, and a simple differential difference

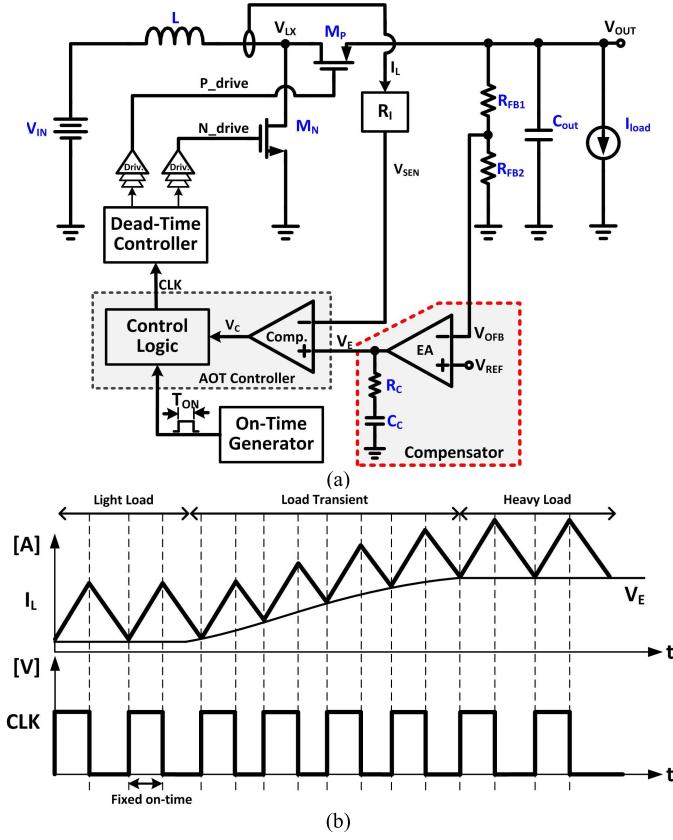


Fig. 1. (a) Conventional current-mode AOT boost converter and its (b) transient response.

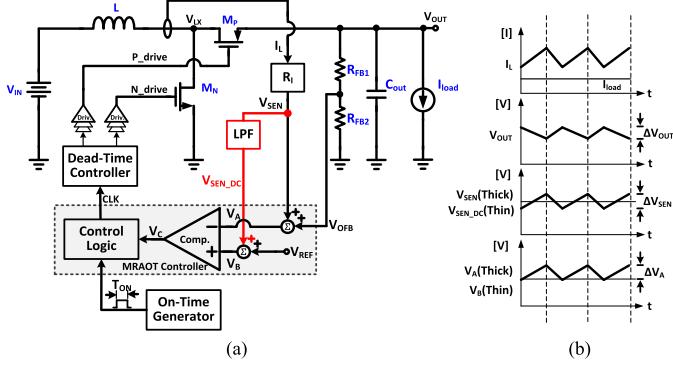


Fig. 2. (a) Simplified system architecture of the proposed MRAOT-controlled boost converter and its (b) related steady-state waveforms.

comparator (DDC) is proposed to replace the complicated addition-comparison circuits. The rest of content is organized as follows. Section II describes the fundamentals and working principle of the proposed MRAOT-controlled boost converter, and Section III shows the block diagram of the proposed boost converter and the implementation of some crucial control circuits. Section IV shows the measured results, and finally, a conclusion is drawn in Section V.

## II. FUNDAMENTALS OF THE MRAOT BOOST CONVERTER

Fig. 2(a) illustrates the simplified system architecture of the proposed MRAOT-controlled boost converter, and its related waveforms are shown in Fig. 2(b). The inductor current (\$I\_L\$)

is sensed and converted to a voltage signal (\$V\_{SEN}\$) by \$R\_I\$, and the feedback voltage signal (\$V\_{OFB}\$) is obtained from the divided resistors, \$R\_{FB1}\$ and \$R\_{FB2}\$. The on-time generator is used to generate an on-time whose length is adaptive to the difference between the input voltage (\$V\_{IN}\$) and the output voltage (\$V\_{OUT}\$). In other words, the on-time is fixed for given \$V\_{IN}\$ and \$V\_{OUT}\$. On the contrary, the off-time is automatically adjusted by the negative feedback loop to regulate \$V\_{OUT}\$. In fact, the off-time length is determined by the MRAOT controller, which comprises two adders, a comparator, and a control logic block. The two adders add \$V\_{SEN}\$ and the dc value of \$V\_{SEN}\$ (i.e., after the LPF) to \$V\_{OFB}\$ and the reference voltage \$V\_{REF}\$, respectively, and then these two summed voltages, \$V\_A\$ and \$V\_B\$, are compared with each other to output \$V\_C\$. The control logic block is used to control states of power transistors (\$M\_N\$ and \$M\_P\$) in different phases. For instance, when \$V\_C\$ changes from 0 to 1 during the off-time phase, the control logic block turns ON and OFF \$M\_N\$ and \$M\_P\$, respectively, and the converter enters the on-time phase. The dead-time controller is used to insert a dead time between two switching signals, so that \$M\_N\$ and \$M\_P\$ would not be turned ON at the same time.

As mentioned above, the output voltage and the inductor current ripples of a boost converter are out of phase, and it cannot use only \$V\_{OFB}\$ as the feedback signal. To cope with this problem, the feedback signal needs to be modified, and it should be in phase with inductor current and capable of sensing the variations of the output load. According to Fig. 2(a), \$V\_A\$ is the sum of \$V\_{SEN}\$ and \$V\_{OFB}\$. By choosing an appropriate current sensing resistance (\$R\_I\$), the ripple of \$V\_{SEN}\$ can be designed to be larger than the ripple of \$V\_{OFB}\$. Thus, \$V\_A\$ is in phase with the inductor current. In fact, the average of \$V\_{SEN}\$, or called the dc value of \$V\_{SEN}\$ (\$V\_{SEN\\_DC}\$), will affect the average of the output voltage, especially at heavy load. Fig. 3 shows the transient responses with the feedback signal including and excluding \$V\_{SEN\\_DC}\$, where these plots are obtained by stimulating the behavior models. If \$V\_{SEN\\_DC}\$ is included, as shown in Fig. 3(a), the average of the output voltage, or called the dc value of output voltage (\$V\_{OUT\\_DC}\$), significantly decreases with the increasing load, which means poor load regulation. In fact, inadequate dc regulation is one of the main problems for converters with ripple-based control [3]. As a matter of fact, the issue of poor load regulation can be solved by excluding \$V\_{SEN\\_DC}\$ from the feedback signal, as shown in Fig. 3(b). Therefore, an additional path to get \$V\_{SEN\\_DC}\$ is inserted in Fig. 2(a). With the LPF, \$V\_{SEN\\_DC}\$ can be extracted and then added to \$V\_{REF}\$ at the positive input terminal of the comparator (\$V\_B\$). By this way, \$V\_{SEN\\_DC}\$ can be eliminated from the feedback signal by nature. Notably, a 100-mV overshoot/undershoot voltage seems to occur only in Fig. 3(b), but not in Fig. 3(a). As a matter of fact, the overshoot/undershoot phenomenon also occurs in Fig. 3(a). However, because the steady-state output voltage at 10 mA is around 100 mV higher than that at 400 mA in Fig. 3(a) due to its poor load regulation, it seems that there is not any overshoot/undershoot voltage appeared at the output voltage. In fact, there is indeed a tradeoff between load regulation and overshoot/undershoot voltages. In the applications that place strict limitations on the amount of overshoot/undershoot

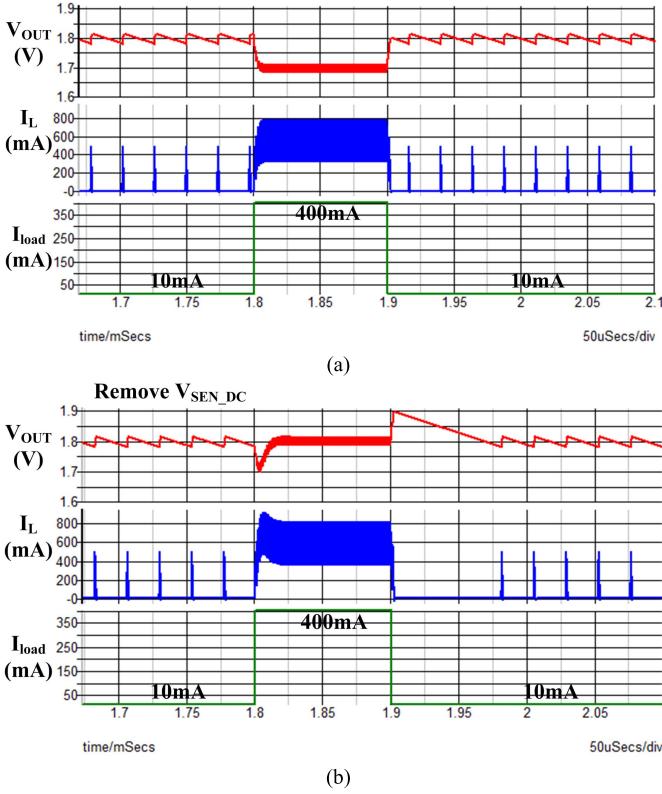


Fig. 3. Simulated transient responses by using behavior models. (a)  $V_{SEN\_DC}$  is included as part of the feedback signal. (b)  $V_{SEN\_DC}$  is removed from the feedback signal.

voltages during load transients, a technique called voltage droop is used to achieve smaller overshoot/undershoot voltages by sacrificing the load regulation.

As shown in Fig. 2(b), the valley of the ripple-contained signal  $V_A$  is limited by the dc signal  $V_B$  because of the comparator. In fact,  $V_{OUT\_DC}$  can be theoretically derived. From Fig. 2(a),  $V_A$  and  $V_B$  can be expressed as

$$V_A = V_{OFB} + V_{SEN} \quad (1)$$

$$V_B = V_{REF} + V_{SEN\_DC}. \quad (2)$$

As mentioned above, the ripple of  $V_{SEN}$  ( $\Delta V_{SEN}$ ) is designed to be larger than the ripple of  $V_{OFB}$  ( $\Delta V_{OFB}$ ), and they are out of phase, as shown in Fig. 2(b). Thus, the ripple of  $V_A$  ( $\Delta V_A$ ) can be expressed as

$$\Delta V_A = \Delta V_{SEN} - \Delta V_{OFB}. \quad (3)$$

In addition, the average of  $V_A$  ( $V_{A\_DC}$ ) should be the sum of the average of  $V_{OFB}$  ( $V_{OFB\_DC}$ ) and  $V_{SEN\_DC}$

$$V_{A\_DC} = V_{OFB\_DC} + V_{SEN\_DC}. \quad (4)$$

From Fig. 2(b),  $V_{A\_DC}$  in steady-state can also be expressed as

$$V_{A\_DC} = V_B + \frac{1}{2} \Delta V_A. \quad (5)$$

Combine (2), (4), and (5) to get

$$V_{OFB\_DC} = V_{REF} + \frac{1}{2} \Delta V_A. \quad (6)$$

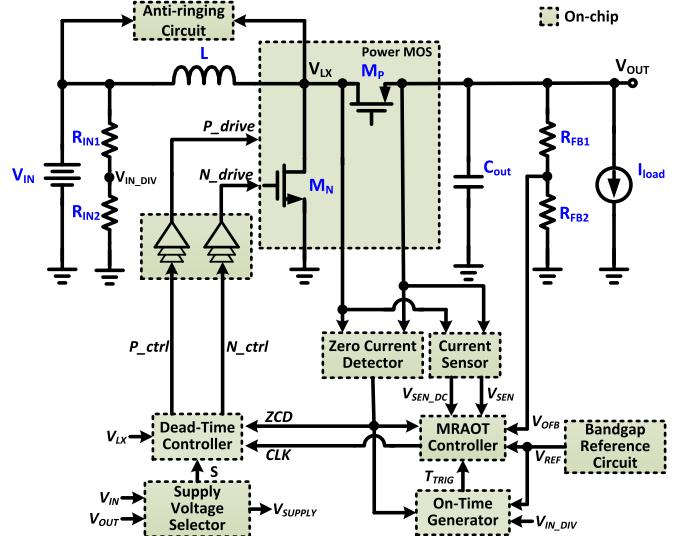


Fig. 4. Block diagram of the proposed MRAOT-controlled boost converter.

Note that  $V_{OFB\_DC}$  is  $K$  times that of  $V_{OUT\_DC}$ , where  $K$  is the divided ratio of the feedback resistors. Therefore,  $V_{OUT\_DC}$  can be expressed as

$$\begin{aligned} V_{OUT\_DC} &= \frac{1}{K} \left[ V_{REF} + \frac{1}{2} (\Delta V_{SEN} - \Delta V_{OFB}) \right] \\ &= \frac{V_{REF}}{K} + V_{offset} \end{aligned} \quad (7a)$$

where the offset of the output voltage ( $V_{offset}$ ) is defined as

$$V_{offset} \equiv \frac{1}{2K} (\Delta V_{SEN} - \Delta V_{OFB}). \quad (7b)$$

Hence,  $V_{OUT\_DC}$  is independent of  $V_{SEN\_DC}$ . However,  $\Delta V_{OFB}$  and  $\Delta V_{SEN}$  still have influences on  $V_{OUT\_DC}$ , but their magnitudes and impacts are much less than those of  $V_{SEN\_DC}$ .

### III. BLOCK DIAGRAM AND MAIN CIRCUIT IMPLEMENTATION

Fig. 4 depicts the block diagram of the proposed MRAOT-controlled boost converter. All the dashed-line shadowed blocks are implemented inside the chip, including the two power transistors ( $M_N$  and  $M_P$ ) and all the control circuits. The detailed circuit implementations of some important blocks are described as follows.

#### A. On-Time Generator

According to [9], the switching frequency in CCM ( $f_{S,CCM}$ ) can be expressed as

$$f_{S,CCM} = \frac{V_{OUT} - V_{IN}}{V_{OUT} T_{ON}} \quad (8)$$

where  $T_{ON}$  is the on-time length. In this paper, the output voltage  $V_{OUT}$  is set to 1.8 V, and the input voltage  $V_{IN}$  may range from 0.8 to 1.4 V. In other words, if  $T_{ON}$  is fixed,  $f_{S,CCM}$  may vary with  $V_{IN}$ , which is not desired as mentioned above. Therefore, to make  $f_{S,CCM}$  fixed,  $T_{ON}$  should be linearly proportional to  $(V_{OUT} - V_{IN})$ . Fig. 5 shows the circuit of the proposed on-time generator.

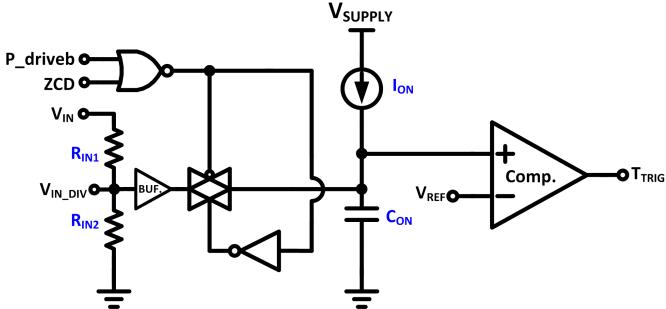


Fig. 5. Proposed on-time generator.

In the off-time phase, the voltage of capacitor  $C_{ON}$  is reset to  $V_{IN\_DIV}$ , which is a divided  $V_{IN}$  generated by two resistors,  $R_{IN1}$  and  $R_{IN2}$ . In the on-time phase, the transmission gate is turned OFF, and the current source  $I_{ON}$  starts to charge  $C_{ON}$ . Once the voltage on  $C_{ON}$  is higher than  $V_{REF}$ , the output of the comparator ( $T_{TRIG}$ ) goes to logic high to terminate the on-time. Thus,  $T_{ON}$  can be expressed as

$$T_{ON} = \frac{V_{REF} - V_{IN\_DIV}}{I_{ON}} C_{ON}. \quad (9)$$

The subtraction in (9) is performed spontaneously by resetting the voltage on capacitor  $C_{ON}$  to  $V_{IN\_DIV}$ . Besides, make the ratio between the two input divided resistors ( $R_{IN1}$  and  $R_{IN2}$ ) the same as the ratio between the two feedback resistors ( $R_{FB1}$  and  $R_{FB2}$ ), that is

$$\frac{R_{IN2}}{R_{IN1} + R_{IN2}} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} = K \quad (10a)$$

$$\therefore \frac{V_{IN\_DIV}}{V_{IN}} = \frac{V_{REF}}{V_{OUT}} = K. \quad (10b)$$

Combine (8), (9), and (10b) to get

$$T_{ON} = \frac{K(V_{OUT} - V_{IN})}{I_{ON}} \cdot C_{ON} \quad (11a)$$

$$\therefore f_{S,CCM} = \frac{I_{ON}}{K \cdot V_{OUT} \cdot C_{ON}}. \quad (11b)$$

As a result,  $T_{ON}$  is linearly proportional to  $V_{OUT} - V_{IN}$ , and  $f_{S,CCM}$  is theoretically fixed and independent of  $V_{IN}$ .

### B. Current Sensor

Fig. 6 shows the current sensing circuit. The p-type sensing transistor ( $M_{PSEN}$ ) generates a current  $I_{SEN}$ , which replicates the inductor current  $I_L$  with a ratio of 1/2000. While  $I_{SEN}$  flows through resistor  $R_S$ , it is then converted to a voltage signal  $V_{SEN}$ . Moreover, another function of this circuit is to extract the dc value of  $V_{SEN}$ . An analog LPF is employed, and it is composed of a 600-kΩ resistor  $R_{LPF}$  and a 6-pF capacitor  $C_{LPF}$ . The corner frequency of this LPF is designed to be far lower than the switching frequency of the converter to guarantee the accuracy of the obtained dc value. Note that the current sensing circuit works just in the off-time phase. Hence, a transistor  $M_{LPF}$  is used to disconnect  $V_{SEN}$  from the LPF in the on-time phase. As a result, the LPF output ( $V_{SEN\_DC}$ ) still remains at its previous value, even when  $V_{SEN}$  becomes zero in the on-time phase. In other words,  $V_{SEN\_DC}$  is actually the dc value of the inductor current in the off-time phase,

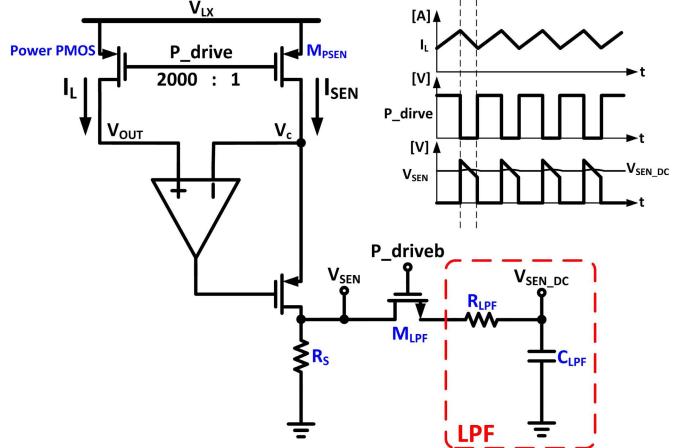
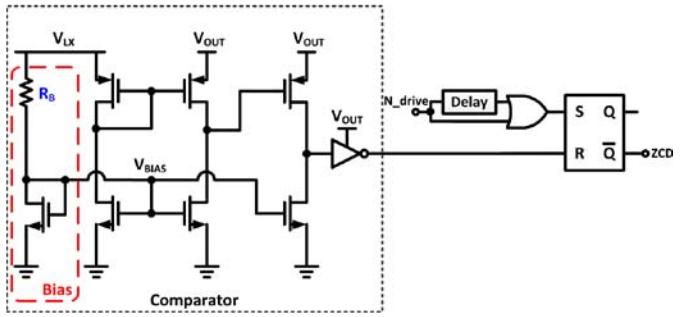
Fig. 6. Current sensing circuit and waveforms of  $I_L$ ,  $V_{SEN}$ , and  $V_{SEN\_DC}$ .

Fig. 7. ZCD.

which should be the same as the dc value of the inductor current in a complete cycle in steady states, as illustrated in Fig. 6.

### C. Zero Current Detector

Because the converter is supposed to be operated in DCM at light load, the zero current detector (ZCD) is essential to detect the timing of zero inductor current and then turn OFF power transistor  $M_P$  to prevent reverse inductor current. Fig. 7 shows the circuit of the ZCD. The detection is performed by comparing the two terminal voltages of  $M_P$ ,  $V_{LX}$ , and  $V_{OUT}$ . As a matter of fact,  $V_{LX}$  and  $V_{OUT}$  may be higher than the supply voltage of the control circuits. Thus, the comparator that uses source terminals of transistors as inputs is adopted [10]. The reverse current can occur only in the off-time phase. Thus, this circuit should be enabled only in the off-time phase for reducing power consumptions. To achieve it, the bias voltage ( $V_{BIAS}$ ) of the comparator is generated by the node voltage  $V_{LX}$ , a resistor, and a diode-connected transistor. As a result, the comparator is shut down automatically in the on-time phase, during which both  $V_{LX}$  and  $V_{BIAS}$  approximate ground. However, erroneous detections may occur during the transitions from the on-time phase to the off-time phase [10]. To prevent this circumstance, a delay block, which generates a 20-ns delay time, is inserted behind the gate-controlled signal,  $N_{drive}$ .

### D. MRAOT Controller and Differential Difference Amplifier

The AOT controller, as shown in Fig. 8(a), is designed to deal with several sensed/feedback signals, and to generate

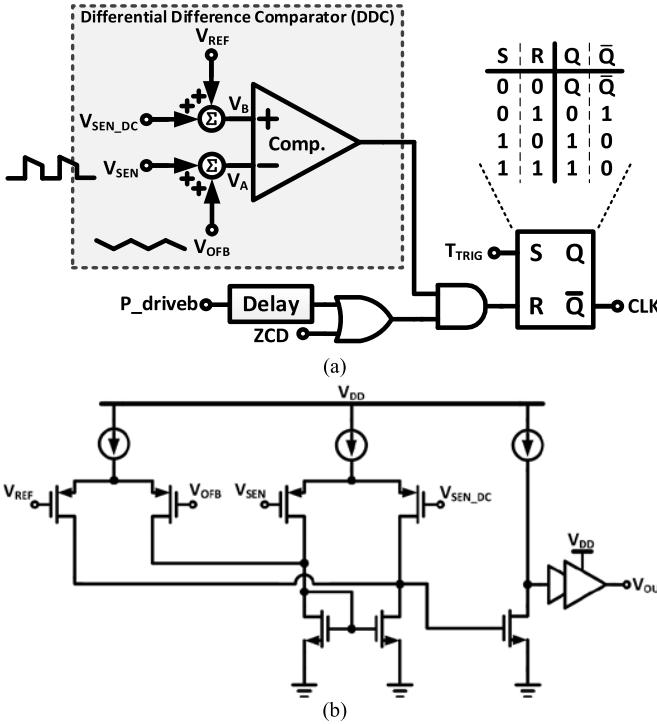


Fig. 8. (a) MRAOT controller. (b) DDC circuit.

a proper switching signal. As described in (1) and (2),  $V_{OFB}$  and  $V_{REF}$  should be summed up with  $V_{SEN}$  and  $V_{SEN\_DC}$ , respectively, and then compare with each other. In fact, adders can be implemented in either voltage or current domain. A conventional voltage adder is mainly an inverting opamp with one extra input signal/resistor. Hence, to perform this comparison, it needs two opamps (i.e., two adders) and one comparator. For a current adder, voltage-to-current ( $V$ -to- $I$ ) converters are usually required to convert the input voltage signals to current signals first. Then, the addition is performed by summing up those current signals. Finally, convert the resulting current to a voltage signal by using a current-to-voltage ( $I$ -to- $V$ ) converter. As to the  $V$ -to- $I$  and  $I$ -to- $V$  converters, the simplest architecture is to use opamps and resistors, and they occupy a significant amount of chip area. For example, the current adder in [6] occupies around 10% of the chip area for the control circuits. In other words, the addition-comparison circuit is complicated and quite power consuming, no matter whether the voltage or current adders are adopted. In this paper, a simple DDC is proposed to solve these issues.

Fig. 8(b) shows the DDC circuit, whose idea originated from the concept of a differential difference amplifier [14]. The DDC combines the circuits of addition and comparison into a single step, and its output  $V_{OUT}$  can be expressed as

$$V_{OUT} = 1, \text{ if } (V_{REF} + V_{SEN\_DC}) > (V_{SEN} + V_{OFB}) \quad (12a)$$

$$V_{OUT} = 0, \text{ if } (V_{REF} + V_{SEN\_DC}) < (V_{SEN} + V_{OFB}). \quad (12b)$$

Fig. 9 demonstrates the key waveforms of MRAOT controller operating in CCM and DCM. The on-time length is controlled by  $T_{TRIG}$ , the output of the on-time generator. In CCM, the off-time length is determined mainly by the inductor

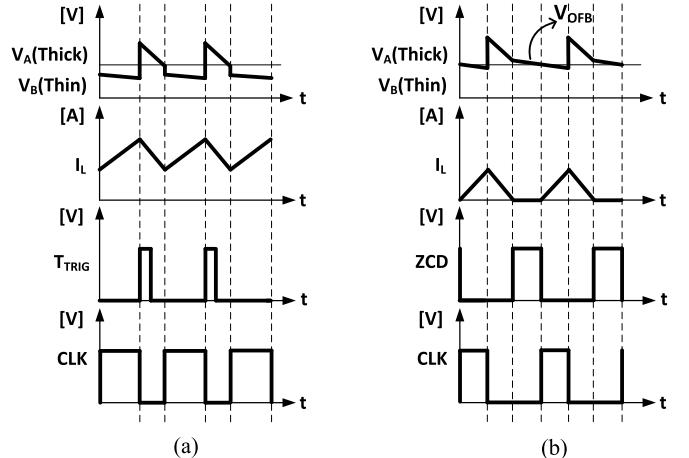


Fig. 9. Key waveforms of MRAOT controller operating in (a) CCM and (b) DCM.

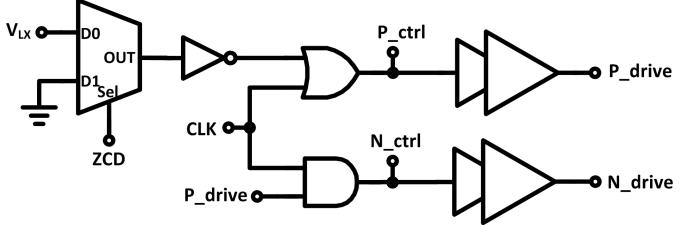


Fig. 10. Dead-time controller.

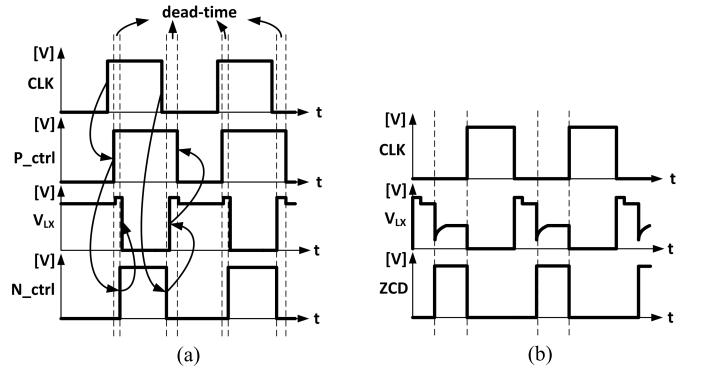


Fig. 11. Related waveforms when signal \$ZCD\$ is (a) not triggered and (b) triggered.

current ripple (from  $V_{SEN}$ ), not by the output voltage ripple (from  $V_{OFB}$ ). On the other hand, the output voltage ripple plays a more important role in determining the off-time length in DCM.

#### E. Dead-Time Controller and Buffers

Fig. 10 shows the circuit of the dead-time controller, and its related waveform is shown in Fig. 11. To obtain a proper dead time, adaptive dead-time control is employed. Hence,  $V_{LX}$  is used as an input signal in this block. Besides, when signal  $ZCD$  is high, power transistor  $M_P$  should be turned OFF. However, if  $V_{LX}$  and  $ZCD$  are sent to an AND gate to generate the corresponding signal to turn OFF  $M_P$ , malfunction may occur since  $V_{LX}$  is connected to the lower voltage  $V_{IN}$  at this time, not the higher voltage  $V_{OUT}$ . For this reason, the transmission-gate-based two-to-one multiplexer is adopted, rather than an AND gate.

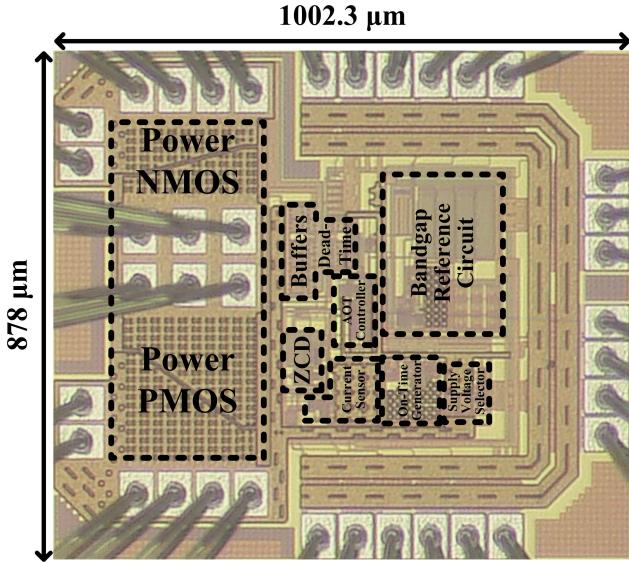


Fig. 12. Micrograph of the proposed chip.

#### IV. EXPERIMENTAL RESULTS

The proposed MRAOT-controlled boost converter was implemented and fabricated by using TSMC 0.18- $\mu\text{m}$  mixed-signal process, and the micrograph of the proposed chip is shown in Fig. 12. The chip size is  $878 \mu\text{m} \times 1002.3 \mu\text{m}$ . The input voltage ( $V_{\text{IN}}$ ) of the converter may range from 0.8 to 1.4 V, and the output voltage ( $V_{\text{OUT}}$ ) is set to 1.8 V with a built-in 0.9-V reference voltage. The inductor and the output capacitor are 1  $\mu\text{H}$  and 6.8  $\mu\text{F}$ , respectively. Moreover, both of them adopt surface mount devices to make the size of the proposed converter compact. The experimental results shows the maximal load current ( $I_{\text{load}}$ ) is 400 mA at  $V_{\text{IN}} = 1.4$  V.

Fig. 13(a) shows the steady-state waveforms of  $V_{\text{OUT}}$ , the inductor current ( $I_L$ ), and the driving signal of power transistor  $M_N$  ( $N_{\text{drive}}$ ) at heavy load ( $V_{\text{IN}} = 1.4$  V and  $I_{\text{load}} = 400$  mA), while Fig. 13(b) shows the waveforms at light load ( $V_{\text{IN}} = 0.8$  V and  $I_{\text{load}} = 10$  mA). Fig. 14 shows the transient responses of the proposed converter when  $I_{\text{load}}$  changes between 10 and 400 mA. Besides, it is worth mentioning that when the load changes from 400 to 10 mA, the excess energy from the inductor during the transition is accumulated in the output capacitor, which makes the output voltage surge and last for a relatively long time. The excess energy stored at the output capacitor can be consumed only by the load current and control circuits, and the power consumption of the latter one is much smaller than the load current typically. Therefore, it takes a while for the small 10-mA load current to restore the output voltage to its steady-state value. In other words, if the load changes from 400 to 100 mA, not 10 mA, the duration and amount of the voltage surge will be much shorter and smaller.

Fig. 15(a) plots the measured output ripple ( $\Delta V_{\text{OUT}}$ ) versus  $I_{\text{load}}$  with several different input voltages. The  $\Delta V_{\text{OUT}}$  range is of 20–42.5 mV only. In addition,  $\Delta V_{\text{OUT}}$  first decreases and then increases with the increasing  $I_{\text{load}}$ , which can be explained even if the small equivalent series resistance of the output capacitor ( $R_{\text{ESR}}$ ) is taken into account.

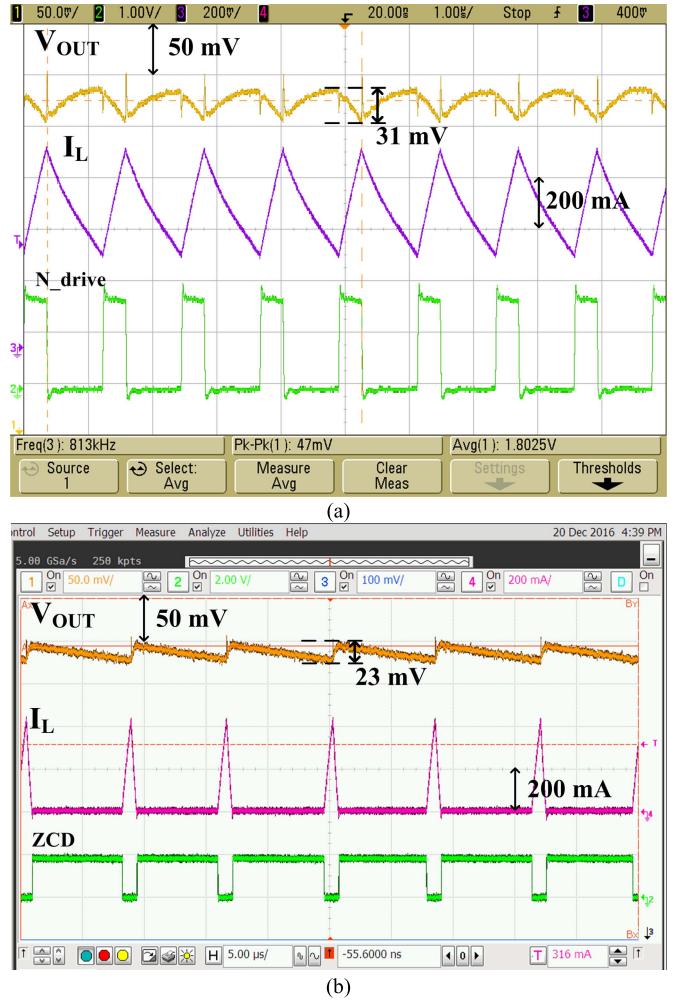


Fig. 13. Measured steady-state operations of the converter. (a)  $V_{\text{IN}} = 1.4$  V and  $I_{\text{load}} = 400$  mA. (b)  $V_{\text{IN}} = 0.8$  V and  $I_{\text{load}} = 10$  mA.

In fact,  $\Delta V_{\text{OUT}}$  can be analyzed in two different cases:  $I_L$  is sometimes smaller than  $I_{\text{load}}$ , and  $I_L$  is always larger than  $I_{\text{load}}$ . Fig. 15(b) and (c) plots the waveforms of some related signals in these two cases, where  $V_{\text{ESR}}$  is the voltage across  $R_{\text{ESR}}$ ,  $V_C$  is the voltage across the pure output capacitance ( $C_{\text{out}}$ ), and  $V_{\text{OUT}}$  is actually the sum of  $V_{\text{ESR}}$  and  $V_C$ . It can be found that  $V_{\text{OUT}}$  first increases and then decreases in the off-time phase in Fig. 15(b), while it keeps increasing in the off-time phase in Fig. 15(c). In Fig. 15(b),  $V_{\text{ESR}}$  reaches zero when  $I_L$  becomes the same as  $I_{\text{load}}$  (i.e., no current flows through  $R_{\text{ESR}}$  and  $C_{\text{out}}$ ), and  $\Delta V_{\text{OUT}}$  can be expressed as

$$\Delta V_{\text{OUT}} = (V_{C,H} - V_{C,L}) + I_{\text{load}} \cdot R_{\text{ESR}} \quad (13)$$

where  $V_{C,H}$  and  $V_{C,L}$  are the highest and lowest value of  $V_C$ , respectively. Denote the time that it takes to discharge the inductor current from its peak value ( $I_{L,\text{peak}}$ ) to  $I_{\text{load}}$  as  $\Delta t$ , and  $\Delta t$  can be calculated as

$$\Delta t = \frac{L(I_{L,\text{peak}} - I_{\text{load}})}{V_{\text{OUT}} - V_{\text{IN}}} \quad (14)$$

and

$$(V_{C,H} - V_{C,L}) = \frac{(I_{L,\text{peak}} - I_{\text{load}}) \cdot \Delta t}{2C_{\text{out}}} \quad (15)$$

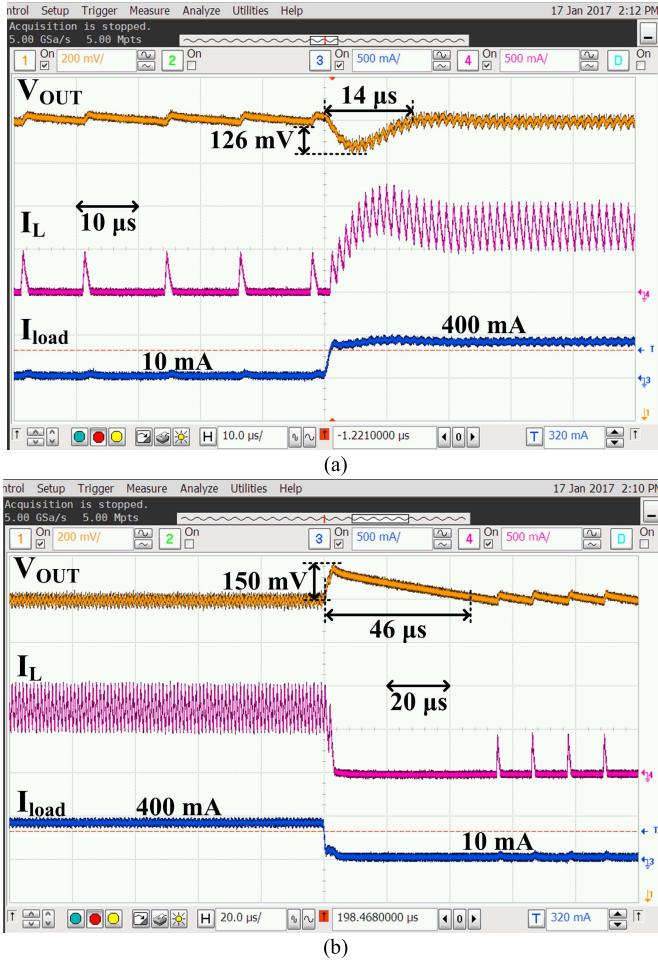


Fig. 14. Transient response of the proposed converter with load current (\$I\_{load}\$) changing from (a) 10 to 400 mA and (b) 400 to 10 mA.

By substituting (14) and (15) into (13), it gets

$$\Delta V_{OUT} = \frac{L(I_{L\_peak} - I_{load})^2}{2C_{out}(V_{OUT} - V_{IN})} + I_{load} \cdot R_{ESR} \quad (16)$$

Therefore, \$\Delta V\_{OUT}\$ decreases with the increasing \$I\_{load}\$, provided that \$(I\_{load} \cdot R\_{ESR})\$ is small (i.e., \$I\_{load}\$ and/or \$R\_{ESR}\$ are small). For the case in Fig. 15(c), \$\Delta V\_{OUT}\$ should be expressed as

$$\Delta V_{OUT} = [V_{C\_H} + (I_{L\_valley} - I_{load}) \cdot R_{ESR}] - [V_{C\_L} - I_{load} \cdot R_{ESR}] \quad (17)$$

where \$I\_{L\\_valley}\$ is the valley value of the inductor current. With the similar analysis technique, \$\Delta V\_{OUT}\$ can be rewritten as

$$\begin{aligned} \Delta V_{OUT} &= (V_{C\_H} - V_{C\_L}) - I_{L\_valley} \cdot R_{ESR} \\ &= \frac{I_{load}}{C_{out}} \cdot T_{ON} - I_{L\_valley} \cdot R_{ESR}. \end{aligned} \quad (18)$$

As a result, \$\Delta V\_{OUT}\$ increases with the increasing \$I\_{load}\$ at this time, provided that \$(I\_{L\\_valley} \cdot R\_{ESR})\$ is small.

Fig. 16 plots the dc value of the output voltage (\$V\_{OUT\\_DC}\$) against \$I\_{load}\$ with several different input voltages, and it can be used to calculate load regulation. According to (7a) and (8), the offset of the output voltage (\$V\_{offset}\$) is proportional to the factor, \$(\Delta V\_{SEN} - \Delta V\_{OFB})\$, where \$\Delta V\_{SEN}\$ is proportional

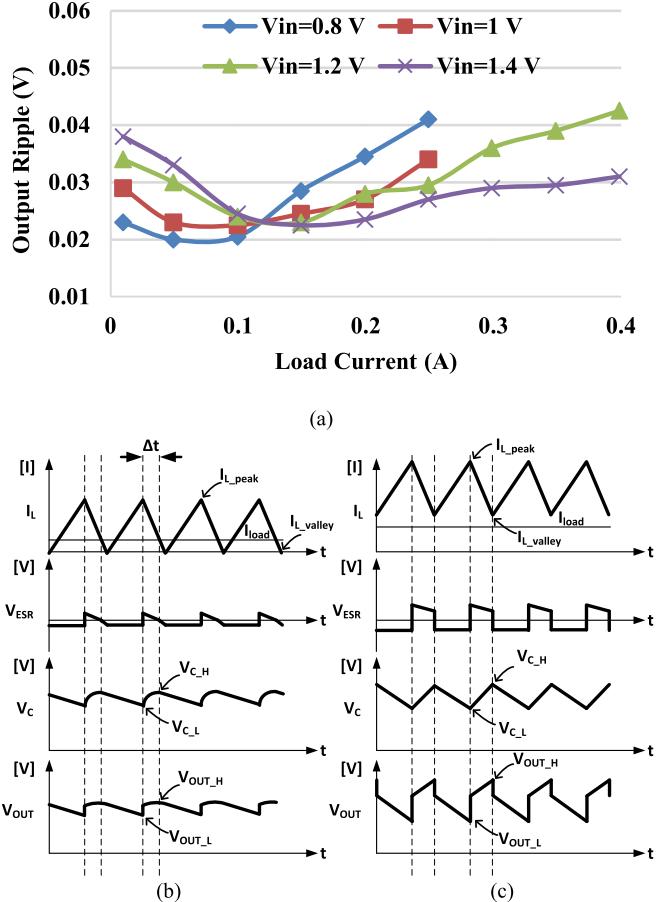


Fig. 15. (a) Output ripple versus the load current with different input voltages and waveforms of some related signals when (b) inductor current is always larger than the load current and (c) inductor current is sometimes smaller than the load current.

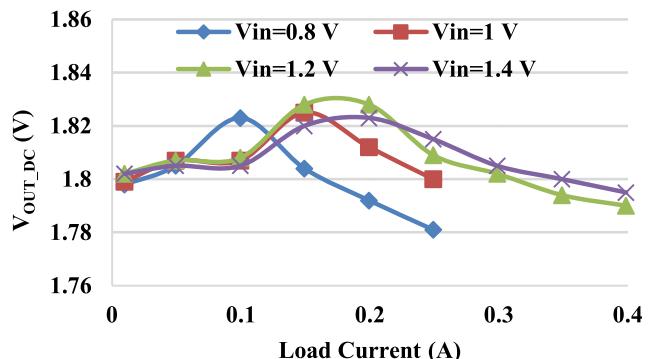


Fig. 16. Plot of dc value of the output voltage (\$V\_{OUT\\_DC}\$) versus the load current with different input voltages.

to the inductor current ripple (\$\Delta I\_L\$) and \$\Delta V\_{OFB}\$ is proportional to \$\Delta V\_{OUT}\$. As mentioned above, \$\Delta V\_{SEN}\$ is designed to be larger than \$\Delta V\_{OFB}\$, so \$V\_{offset}\$ is dominated by \$\Delta I\_L\$. In fact, \$\Delta I\_L\$ is proportional to \$T\_{ON}\$ and \$V\_{IN}\$ in steady states. From (11a), it can be expressed as

$$\Delta I_L = \frac{V_{IN} \cdot T_{ON}}{L} = \frac{K(V_{OUT} - V_{IN})V_{IN}}{I_{ON}} \cdot C_{ON}. \quad (19)$$

In this paper, \$V\_{OUT}\$ is set to 1.8 V, and \$V\_{IN}\$ is within the range of 0.8–1.4 V. Thus, \$\Delta I\_L\$ reaches its minimum at \$V\_{IN} = 1.4\$ V, and so does \$V\_{offset}\$. Accordingly, the load

TABLE I  
PERFORMANCE COMPARISON

Specification	[7]	[8]	[15]	[16]	[17]	[10]	[5]	This Work
Process	0.35 $\mu\text{m}$	0.5 $\mu\text{m}$	0.18 $\mu\text{m}$	0.3 $\mu\text{m}$	0.13 $\mu\text{m}$	0.18 $\mu\text{m}$	0.35 $\mu\text{m}$	<b>0.18 <math>\mu\text{m}</math></b>
Control	AOT	AOFT	Sigma-delta	Hysteretic	PFM/PWM	AOT	SMQH	<b>MRAOT</b>
Inductor	1 $\mu\text{H}$	3.3 $\mu\text{H}$	3.3 $\mu\text{H}$	1 $\mu\text{H}$	2.2 $\mu\text{H}$	4.7 $\mu\text{H}$	6.8 $\mu\text{H}$	<b>1 <math>\mu\text{H}</math></b>
Capacitor	10 $\mu\text{F}$	20 $\mu\text{F}$	10 $\mu\text{F}$	10 $\mu\text{F}$	10 $\mu\text{F}$	22 $\mu\text{F}$	10 $\mu\text{F}$	<b>6.8 <math>\mu\text{F}</math></b>
Conduction Mode	DCM/CCM	DCM/CCM	DCM/CCM	DCM/CCM	DCM/CCM	DCM	DCM/CCM	<b>DCM/CCM</b>
Compensator	PI (internal)	PI (internal)	PID (external)	PI (internal)	N/A	w/o	w/o	<b>w/o</b>
Input Voltage	1.8–3.2 V	5 V	0.8–1.2 V	2.5–4.2 V	5.5 V	0.5–1.3 V	0.45–0.9 V	<b>0.8–1.4 V</b>
Output Voltage	3–4.2 V	5.5–36 V	1.8 V	5 V	12 V	1.8 V	2 V	<b>1.8 V</b>
Output Ripple (max.)	80 mV	52 mV	45 mV	<50 mV	80 mV	40 mV	~40 mV	<b>42.5 mV</b>
Load Current (max.)	800 mA	500 mA	100 mA	500 mA	600 mA	130 mA	100 mA	<b>400 mA</b>
Load Transient	10 $\mu\text{s}$ @10→800 mA	42 $\mu\text{s}$ @150→350 mA	6 $\mu\text{s}$ @10→100 mA	27 $\mu\text{s}$ @200→400 mA	N/A	N/A	11.6 $\mu\text{s}$ @10→100 mA	<b>14 <math>\mu\text{s}</math></b> @10→400 mA
Recovery Time/ Load Current Step	0.0128 $\mu\text{s}/\text{mA}$	0.21 $\mu\text{s}/\text{mA}$	0.06 $\mu\text{s}/\text{mA}$	0.135 $\mu\text{s}/\text{mA}$	N/A	N/A	0.128 $\mu\text{s}/\text{mA}$	<b>0.036 <math>\mu\text{s}/\text{mA}</math></b>
Load Regulation	0.0001 %/mA	N/A	N/A	0.005 %/mA	N/A	~0.022 %/mA	~0.017 %/mA	<b>0.0156 %/mA</b>
Peak Efficiency	94.8%	92.94%	90%	90%	91%	90.6%	89.4%	<b>92.4%</b>
Chip Area	2.15 $\text{mm}^2$	4 $\text{mm}^2$	0.85 $\text{mm}^2$	1.9 $\text{mm}^2$	1.7 $\text{mm}^2$	0.72 $\text{mm}^2$	3.84 $\text{mm}^2$	<b>0.88 <math>\text{mm}^2</math></b>
Efficiency (mm <sup>2</sup> /A)	1.79	2.5 <sup>[1]</sup>	3.78	1.82	1.95 <sup>[1]</sup>	4	8.64	<b>1.56</b>

<sup>[1]</sup>Only one power transistor is implemented inside the chip in Ref. [8] and Ref. [17], while there are two on-chip power transistors in the other papers. Therefore, the calculated chip area efficiencies in Ref. [8] and Ref. [17] are multiplied by 1.5 for a fair comparison

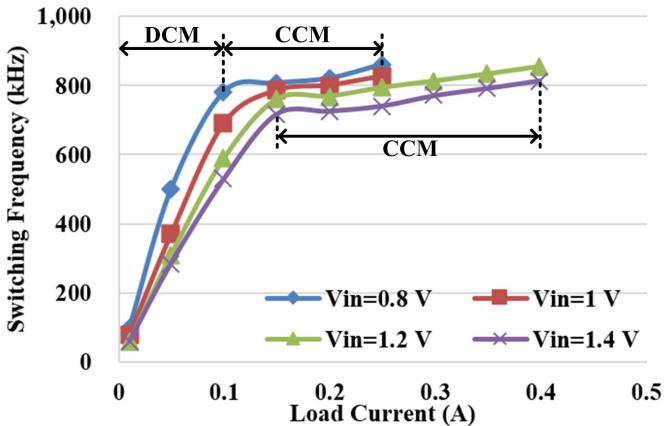


Fig. 17. Switching frequency versus the load current with different input voltages.

regulation is the best at  $V_{IN} = 1.4$  V. Moreover, for a given  $V_{IN}$ ,  $\Delta I_L$  is supposed to be fixed, so  $V_{offset}$  ( $V_{OUT\_DC}$ ) actually varies with  $\Delta V_{OFB}$  ( $\Delta V_{OUT}$ ). As shown in Fig. 15(a),  $\Delta V_{OUT}$  first decreases and then increases with the increasing  $I_{load}$ . Therefore,  $V_{OUT\_DC}$  first increases and then decreases with the increasing  $I_{load}$ .

Fig. 17 plots the switching frequency of the converter versus the load current with several different input voltages. It can be found that the switching frequency is approximately fixed in CCM (i.e., 750–860 kHz), not significantly varied with the load current. In DCM, the switching frequency is proportional to the load current, as expected. Moreover, the proposed converter can smoothly switch between DCM and CCM. Fig. 18 plots the measured efficiency versus the load current with several different input voltages. The peak efficiency is 92.4%, occurring at a 1.4-V input voltage and 170-mA load current.

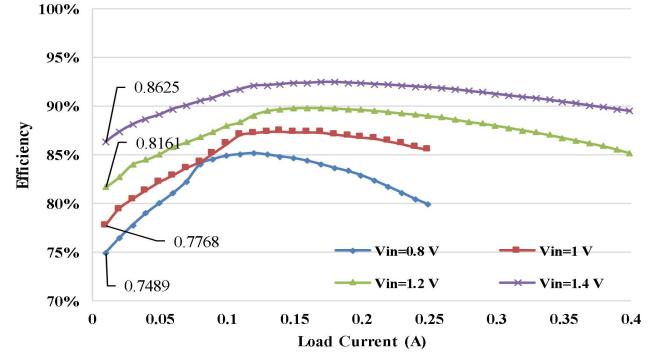


Fig. 18. Efficiency versus the load current with different input voltages.

Table I compares the measured performance of this paper with some state-of-the-art publications. The proposed MRAOT-controlled boost converter requires neither any compensator nor external compensation component. Among the work without compensators, the proposed converter has the best load regulation and the widest load range. Moreover, the number of external components and chip area are two important factors that are directly related to cost. Typically, the chip area of a power management IC (i.e., cost) is mainly occupied by its power transistors, and the sizes of these power transistors should be proportional to their maximal allowable current. Therefore, to get a relatively fair comparison among the work with different specifications, a parameter, chip area efficiency, is defined as

$$\text{Chip Area Efficiency} = \frac{\text{Chip area}}{I_{L\_AVG(max)}} = \frac{(1 - D) \cdot \text{Chip area}}{I_{load(max)}} \quad (20)$$

where the maximal average inductor current ( $I_{L\_AVG(max)}$ ) can be derived by the maximal load current ( $I_{load(max)}$ ) and the

duty ratio. It can be found that the proposed chip has the best chip area efficiency, which means that its chip area is the smallest for a given inductor current.

## V. CONCLUSION

The MRAOT-controlled boost converter is proposed in this paper. With the proposed MRAOT control, the converter can smoothly switch between DCM and CCM, depending on the load current. In CCM, the control mainly uses the inductor current ripples to regulate the output voltage, and the switching frequency is approximately fixed. In DCM, the output voltage ripples are used for regulation. Moreover, no compensator is required and a satisfied load regulation is achieved. Hence, a significant chip area can be reduced. Furthermore, the proposed on-time generator can fix the switching frequency in CCM, and the proposed DDC has the advantages of low power consumption and small area. According to the measured results, the maximal load current is 400 mA, and the peak conversion efficiency is 92.4%.

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