

# Modular 128-Channel $\Delta$ - $\Delta$ $\Sigma$ Analog Front-End Architecture Using Spectrum Equalization Scheme for 1024-Channel 3-D Neural Recording Microsystems

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**Abstract**—We report an area- and energy-efficient integrated circuit architecture of a 128-channel  $\Delta$ -modulated  $\Delta\Sigma$  analog front-end ( $\Delta$ - $\Delta$  $\Sigma$  AFE) for 1024-channel 3-D massive-parallel neural recording microsystems. Our platform has adopted a modularity of 128 channels and consists of eight multi-shank neural probes connected to individual AFEs through interposers in a small form factor. In order to reduce both area and energy consumption in the recording circuits, we implemented a spectrum equalization scheme to take advantage of the inherent spectral characteristics of neural signals, where most of the energy is confined in low frequencies and follows a  $\sim 1/f$  curve in the spectrum. This allows us to implement the AFE with a relaxed dynamic range by  $\sim 30$  dB, thereby contributing to the significant reduction of both energy and area without sacrificing signal integrity. The  $\Delta$ - $\Delta$  $\Sigma$  AFE was fabricated using  $0.18\text{-}\mu\text{m}$  CMOS processes. The single-channel AFE consumes  $3.05\text{ }\mu\text{W}$  from  $0.5$  and  $1.0\text{ V}$  supplies in an area of  $0.05\text{ mm}^2$  with  $63.8\text{-dB}$  signal-to-noise-and-distortion ratio,  $3.02$  noise efficiency factor (NEF), and  $4.56\text{ NEF}^2\text{V}_{DD}$ . We also have achieved an energy-area product, a figure-of-merit most critical for massive-parallel neural recording systems, of  $6.34\text{ fJ/C}\cdot\text{s}\cdot\text{mm}^2$ .

**Index Terms**— $\Delta$ -modulated  $\Delta\Sigma$  analog front-end ( $\Delta$ - $\Delta$  $\Sigma$  AFE),  $\Delta$ -modulation, continuous-time (CT)  $\Delta\Sigma$ , energy-area product, low power, massive-parallel, neural recording microsystem, spectrum equalization.

## I. INTRODUCTION

FOR the past few decades, the number of parallel recording in neural interface systems has been dramatically increased by the advancement of microelectromechanical-systems technologies and mixed-signal circuit techniques [1]–[3]. According to a recent survey, the number of the simultaneously recorded neurons has been doubled in every 7.4 years throughout last 5 decades, following a trend similar to the Moore’s law in electronic devices [1]. The availability of multi-electrode arrays in 2- or 3-D configuration has

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enabled the *in situ* monitoring of large-scale neural activities, and the recording integrated circuits have been either monolithically integrated with the electrode arrays [4]–[8] or assembled in a hybrid fashion [9]–[12] for reliable recording of a large number of neurons with the minimum lead connections, mitigating a tethering issue. This advancement has been important for comprehensive neuroscience research since high quality, parallel monitoring of a large number of neurons within a target region of the brain can provide in-depth understanding of interactions among individual neurons as well as neuronal information processing in system levels [13]–[15]. Such understanding can also be translated into clinical applications including visual, auditory, sensory, and motor prosthetics as well as bidirectional neural control systems for brain-machine interface.

Current state-of-the-art neural recording systems provide roughly one to three hundreds of channels in parallel [6]–[9], [11], [16]–[19]. A wireless 100-channel neural recording system was demonstrated with an *Utah* probe in *in vivo* environments in 2007 [9]. In 2012, a 96-channel recording system was introduced to fully cover both of local field potentials (LFPs) and action potentials (APs, or spikes) with wireless telemetry [19]. A modular architecture for a 3-D recording platform expandable to 128 channels was also proposed and showed the promising result for the multi-channel massive recordings in the same year [11]. More recently, IMEC presented a monolithically integrated CMOS active probe having 455 channels where 55 out of 455 channels could be selected for parallel recording [7], followed by a scaled version that enabled 384-channel parallel recording out of 966 electrodes using  $0.13\text{-}\mu\text{m}$  silicon on insulator technology [8].

Even though the current state-of-the-art neural recording systems has made a huge progress, the number of channels accessible for simultaneous recording is still not enough for comprehensive understanding of the structural and functional organization of neurons. The number of neurons in a small area of a rodent brain are far beyond a few hundred ( $n \approx 1000$  within a radius of  $\sim 140\text{ }\mu\text{m}$  in a rat cortex), and the interconnection between neurons is even more complex [13], [20]. The next generation neural recording system should be able to provide simultaneous recording of more than a thousand of neurons within a small volume. For the realization of such a high-density recording system, we should

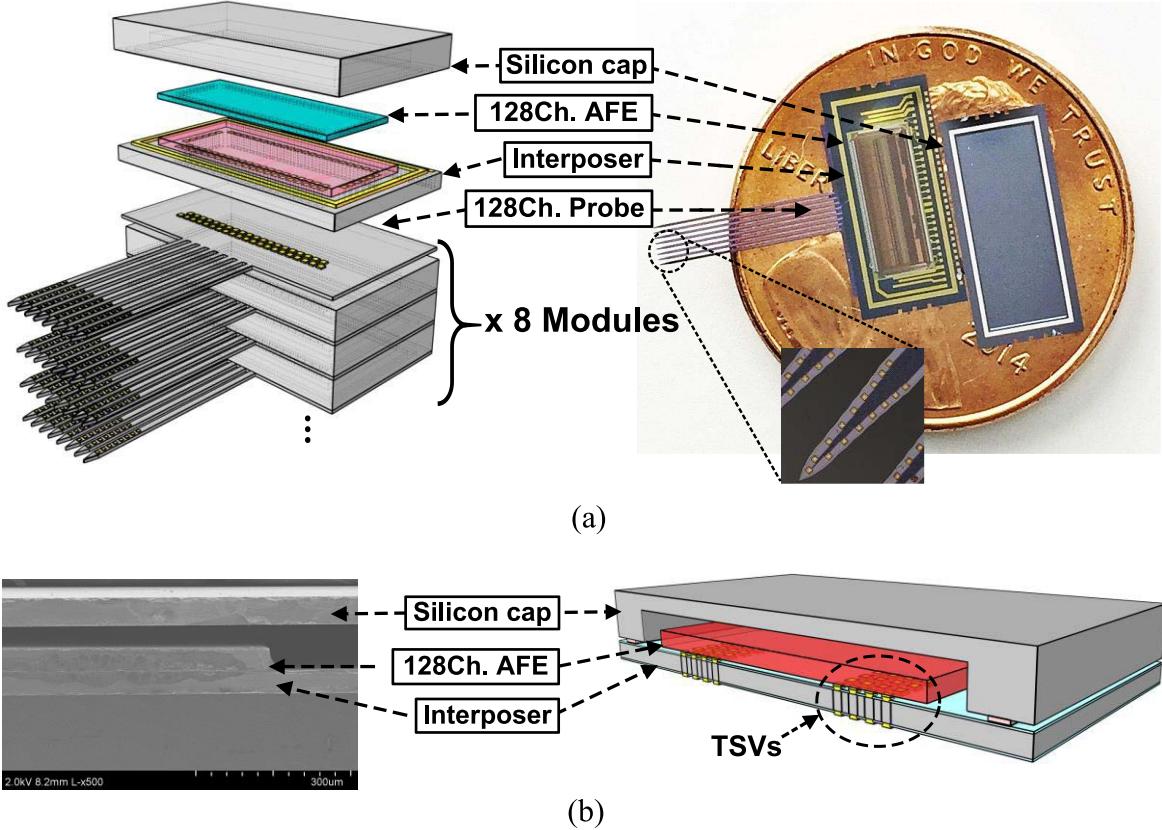


Fig. 1. (a) Conceptual diagram of a 1024-channel parallel-recording platform assembled with the proposed 128-channel AFEs, interposers, silicon caps, and 128-channel multi-shank probes and a photograph of the fabricated module on the top of a U.S. penny. (b) Cross-sectional view of the interposer providing the interconnection between the 128-channel neural probe and AFE chip with TSVs and an SEM image of the assembled module.

address the energy and area consumption of the integrated circuits concurrently since the high energy consumption of the large number of the electrical recording inevitably leads to tissue heating and a bulky system also limits chronic monitoring of brain activities, and is often improper to investigate a small target region of brain. A few recent works have been proposed to address the area and energy constraints [21], [22]. Muller *et al.* [21] pushed the limit of the area consumption in neural recording systems. They implemented a two-channel neural recording prototype that occupied only  $0.013 \text{ mm}^2/\text{channel}$  in 65-nm CMOS technology [21]. On the other hand, Han *et al.* [22] pushed energy consumption, realizing their analog front-end (AFE) with sub- $\mu\text{W}$  ( $0.94 \mu\text{W}/\text{channel}$ ) from 0.45/1-V dual supplies. The each individual work hits the record in terms of area or power consumption independently; however, to scale massive-parallel neural recording systems beyond 1000 channels, both the area and energy consumption must be simultaneously minimized.

In order to address this challenge, we proposed a spectrum equalization scheme in the AFE circuit to equalize the amplitude of neural signals: both LFPs (0.5–300 Hz) and spikes (0.3–10 kHz) without sacrificing signal integrity [23]. This approach alleviates the high dynamic range (DR) requirement for processing the neural signals;

therefore, significantly reducing power consumption in neural recording systems. On the top of that, we combined the equalization scheme with an oversampled analog-to-digital converter (ADC) ( $\Delta\Sigma$  ADC) which can be realized in a compact area than a successive approximation register (SAR) ADC, typically employed for neural recording systems due to its low power consumption [7]–[9], [11], [18], [19], [22]. Thus, the proposed AFE architecture is able to achieve both area and energy reduction. The fabricated  $\Delta\Delta\Sigma$  AFE chip achieved power consumption of only  $3.05 \mu\text{W}/\text{channel}$  within  $0.05 \text{ mm}^2/\text{channel}$  with  $>10\text{-b}$  resolution. The proposed AFE achieved the high energy-area efficiency while providing the state-of-the-art recording performance for capturing broadband neural signals (both LFP and spikes). We also present a conceptual modular platform of 1024-channel recording systems that can consist of 128-channel  $\Delta\Delta\Sigma$  AFE circuits in a multi-shank probe array. This allows flexibility in its configuration, thereby expandable to any integer multiples of the proposed 128 AFEs, not bounded by 1024-channel. The assembled whole 1024-channel platform occupies only a volume of  $<1 \text{ cm}^3$ , while providing robust performance and reliable recording in a behaving animal.

This paper is organized as follows. The concept of a modular architecture of 128-channel circuit  $\Delta\Delta\Sigma$  AFEs for

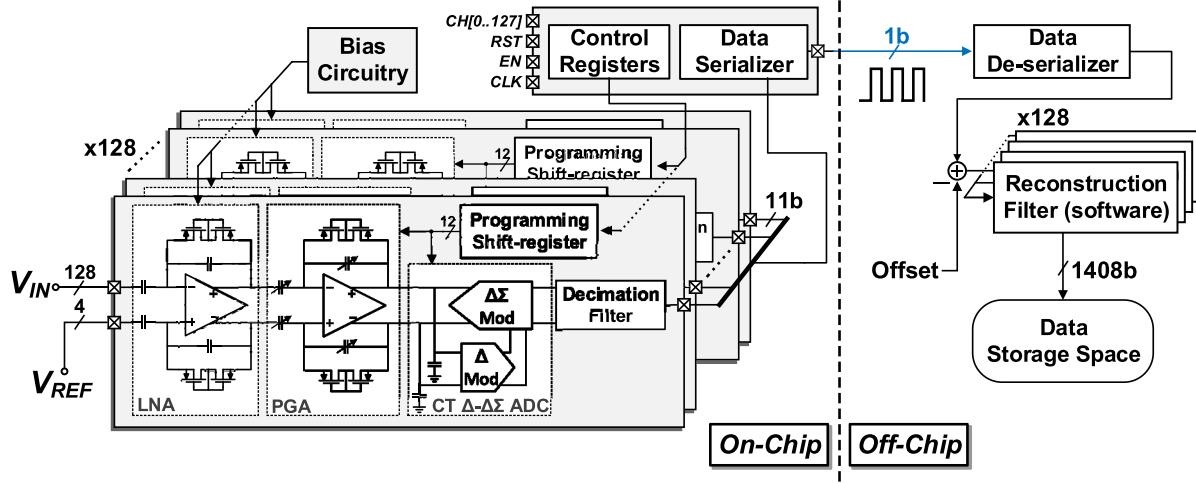


Fig. 2. Top-level circuit architecture of a 128-channel neural recording AFE.

1024-channel systems are described in Section II. In Section III, the main circuit blocks of the proposed  $\Delta$ - $\Delta$  $\Sigma$  AFE are presented in detail. Section IV provides the measurement results obtained from *ex vivo* electrical characterization and *in vivo* experiments conducted in a rodent. The measured performance is summarized and compared with other state-of-the-art works. Finally, Section V concludes this paper.

## II. ARCHITECTURE FOR NEURAL RECORDING MICROSYSTEMS

### A. Modular Platform for 1024-Channel Neural Recording Microsystems

In order to realize a high-density parallel-recording system, we propose a modular platform that consists of 128-channel AFEs and multi-shank neural probes connected through an interposer and stacked to form a 3-D large-scale recording system. Each 128-channel recording system can operate individually, allowing the platform to be scalable to any arbitrary multiples of 128 channels, depending on applications and the limit in system form factors. Fig. 1(a) shows a conceptual diagram of the proposed platform for a 1024-channel parallel neural recording system. Eight modules are stacked to form a complete 3-D recording array. Each module consists of a 128-channel neural probe, a 128-channel AFE chip, an interposer, and a silicon cap as shown in Fig. 1(a). The neural probe has eight 6-mm-long shanks of 70  $\mu$ m in width and 15  $\mu$ m in thickness, and 16 individual recording sites are assigned in each shank [see Fig. 1(b)]. To compensate for mechanical stress in the neural probe, the multiple layers of SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub> composite films have been used [5]. The electrode in each recording site is formed with iridium, and the impedance was measured as <1 M $\Omega$ . The routing traces are formed by gold in 3  $\mu$ m/3  $\mu$ m lines and spaces on the top of the phosphorous-doped silicon substrate encapsulated by a composite dielectric layer of 0.75  $\mu$ m in thickness. The resistance of the traces was distributed within 40–50 k $\Omega$  that is negligible compared with the site impedance ( $\sim$ 1 M $\Omega$ ).

From the equivalent electrical model [7], the crosstalk in between the electrodes was estimated as  $-50.4$  dB. As shown in Fig. 1(b), the 128-channel probe and AFE circuits are flip-chip bonded with through-silicon-vias (TSVs) embedded in the interposer. TSV is formed by using low-resistivity silicon pillars through trench etching and refilling processes with conformal oxide deposition. The contact and via resistances were measured as  $\sim$ 0.46 and  $\sim$ 1.93  $\Omega$ , respectively, and the coupling capacitance between vias as  $\sim$ 26.6 fF. This can provide the proximate interconnection between the probes and recording circuits; otherwise, it often results in bulky backend of high-density recording systems [3]. A scanning electron microscopic (SEM) image of the module in cross section is also shown in Fig. 1(b). The dimension of the interposer is 10.8  $\times$  5  $\times$  0.04 mm<sup>3</sup>. A custom silicon cap provides hermetic sealing by indium solder bonding in the rim [24]. The sealed package passed the gross leak test and satisfies the criteria in MIL-STD 750E. Microphotograph of an assembled single module is shown on a U.S. penny in Fig. 1(a).

### B. 128-Channel $\Delta$ - $\Delta$ $\Sigma$ Architecture

Fig. 2 shows the circuit architecture of 128-channel  $\Delta$ -modulated  $\Delta$  $\Sigma$  ( $\Delta$ - $\Delta$  $\Sigma$ ) AFEs and an off-chip post-processor. The on-chip AFE consists of 128-independent signal acquisition channels. Each channel includes a low-noise amplifier (LNA), a programmable gain amplifier (PGA), a  $\Delta$ - $\Delta$  $\Sigma$  ADC, and a digital decimation filter in series. The gain and bandwidth of LNA and PGA are programmable using shift registers. The bias voltage and current are generated on-chip. The 128-channel output data is serialized into 1-b and transmitted to a host system. The  $\Delta$ -modulated signals from  $\Delta$ - $\Delta$  $\Sigma$  AFE are de-serialized and fully retrieved by the reconstruction filters in an off-chip processor. Even though the offset from input signals is well-blocked from ac-coupling capacitors, the systematic offset can be accumulated. In the proposed architecture, the systematic offset can be cancelled out in every 0.1–0.5 Hz by measuring and subtracting the average dc drifts. Fig. 3 illustrates how the  $\Delta$ - $\Delta$  $\Sigma$  AFE can achieve high energy efficiency by equalizing the spectrum

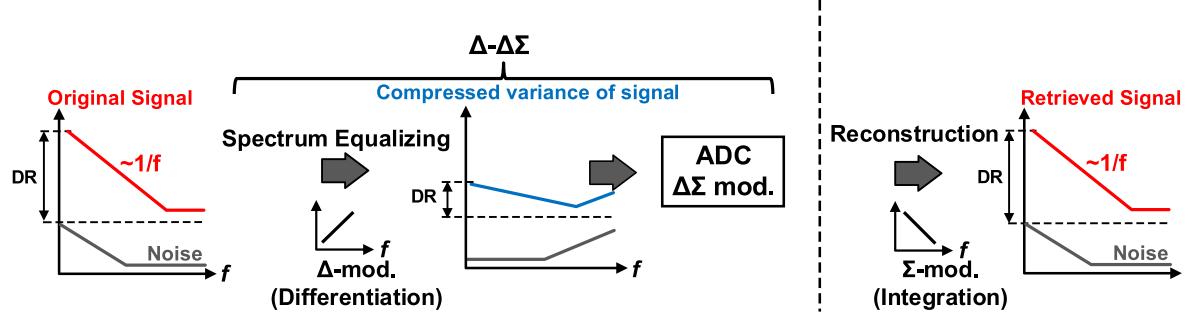


Fig. 3. On-chip spectrum equalization in  $\Delta\text{-}\Delta\Sigma$  AFE and off-chip signal reconstruction.

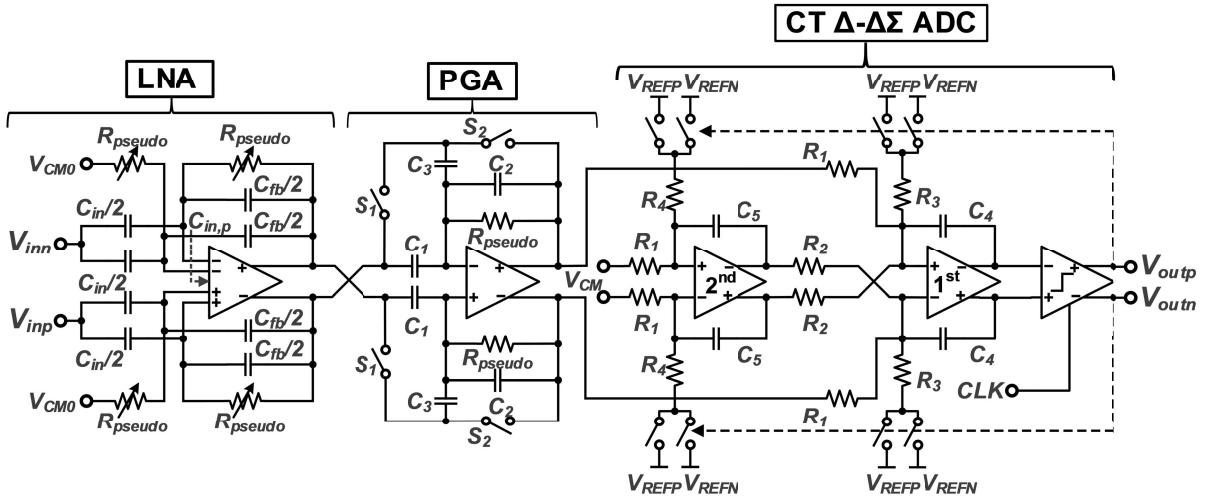


Fig. 4. Schematic of single-channel  $\Delta\text{-}\Delta\Sigma$  AFE.

of neural signals. To achieve a comprehensive understanding of brain activity, both LFPs and spikes should be monitored simultaneously [13]. The amplitude of these signal ranges from a few  $\mu\text{V}$  to  $\text{mV}$  (LFP: 1–3  $\text{mV}$ ; spikes: 100–300  $\mu\text{V}$ ), and the bandwidth spans from a few Hz to kHz (LFP: 1–300 Hz; spikes: 0.3–7.5 kHz). In order to cover both of the LFPs and spikes, the recording circuits have to be designed with a sufficiently low input-referred noise (IRN <5–10  $\mu\text{V}_{\text{rms}}$ ), a high gain, a wide DR ( $\text{DR} > 60 \text{ dB}$ ), and a large bandwidth (a few Hz to 10 kHz), which consequently leads to high power and large area consumption in the AFE. In order to address this, we developed a scheme to equalize the spectrum of neural signals (equalizing the amplitude of LFPs and spikes in the frequency domain) without sacrificing signal integrity by taking a temporal difference ( $\Delta$ -modulation) of neural signals. This is possible mainly due to the nature of neural signals where most of their energy resides at low frequencies and follows a  $\sim 1/f^n$  curve ( $n = 1\text{--}2$ ) in their power spectrum [25]. As shown in Fig. 3, the incoming neural signals including LFPs and spikes are  $\Delta$ -modulated, quantized, and then sent to the external system where the signals are processed and stored. By  $\Delta$ -modulation, the variance of neural signals is compressed since the modulation is, in fact high-pass filtering; thus, a relatively low-resolution ADC (5–6 b) is sufficient to fully embrace the entire signal range. This can

relax a high-resolution requirement in ADC. An 1-b  $\Delta\Sigma$  ADC with an oversampling ratio (OSR) of 32 is employed instead of an SAR ADC of more than 10-b resolution, which is typically employed in neural recording AFEs due to its low power consumption. The digitized signals are sent to the external system where the modulated neural signals are fully recovered from  $\Sigma$ -modulation that is equivalent to low-pass filtering (an inverse function of the high-pass filtering). The entire modulation and demodulation process can be understood as a cascaded system consisting of a system (on-chip) and its inverse (off-chip). The procedure does not deal with the noise and signal separately thus, overall signal-to-noise ratio (SNR) is not affected by the modulation and demodulation process.

In recent literature, the similar architectures were reported for broadband neural recording [26], [27] and electrocorticography recording [28], [29]. The spectrum shaping is implemented by exploiting the  $\sim 1/f$  characteristics of neural signals, and the state-of-the-art noise and DR performance were reported in [27]. However, the implementation of discrete-time (DT) frequency shaping incurred several non-idealities such as switch-induced noise and noise folding. Complex compensation techniques were used to minimize these non-idealities; thus, the reported architecture could not benefit for area and power reduction. On the contrary, our

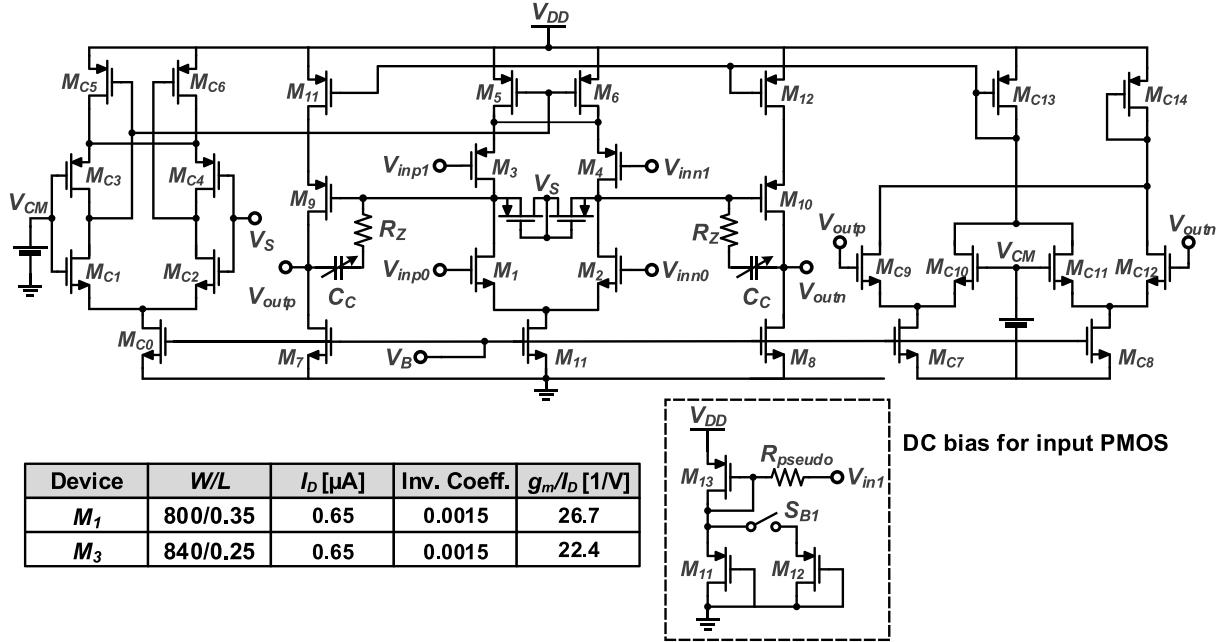


Fig. 5. Schematic of an OTA used in LNA. Input transistor sizes and operating conditions ( $M_1$ – $M_4$ ) are summarized in table.

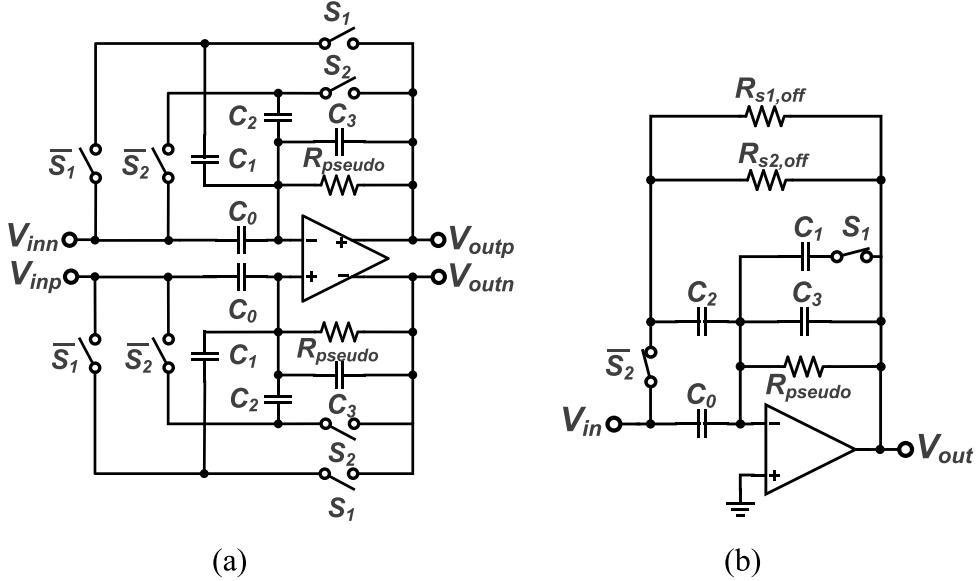


Fig. 6. (a) Schematic of PGA and (b) half-circuit of flip-over-capacitor configuration when  $S_1$  and  $S_2$  are set as “H” and “L,” respectively.

$\Delta$ - $\Delta$ Σ AFE can achieve significant area and energy reduction by taking advantage of spectrum equalization.

### III. CIRCUIT BLOCK IMPLEMENTATION

Fig. 4 shows circuit schematics of a single-channel  $\Delta$ - $\Delta$ Σ AFE. The AFE operates fully differentially through the entire signal acquisition chain in order to minimize common mode (CM) variations and increase the DR. Thanks to the continuous-time (CT) operation of  $\Delta$ - $\Delta$ Σ ADCs, no sample and hold circuit between PGA and ADC is necessary and anti-aliasing requirement is also relaxed [30]. All the analog blocks can adaptively operate from 0.5 to 1 V in supply voltage

except for the comparator that is connected to the digital blocks operating at 1-V fixed supply. The AFE consumes  $3.05 \mu\text{W}$ , while occupying an area of  $0.05 \text{ mm}^2$ . The operating parameters, such as low and high-frequency corners and a total gain of the channel, are individually programmable via a scan chain and can be adaptively reconfigured on the fly during *in vivo* measurements.

#### A. Low-Noise Amplifier

Since the LNA is the first stage of the signal acquisition chain as shown in Fig. 4, it must provide an enough gain while exhibiting low-noise performance. In addition, the LNA

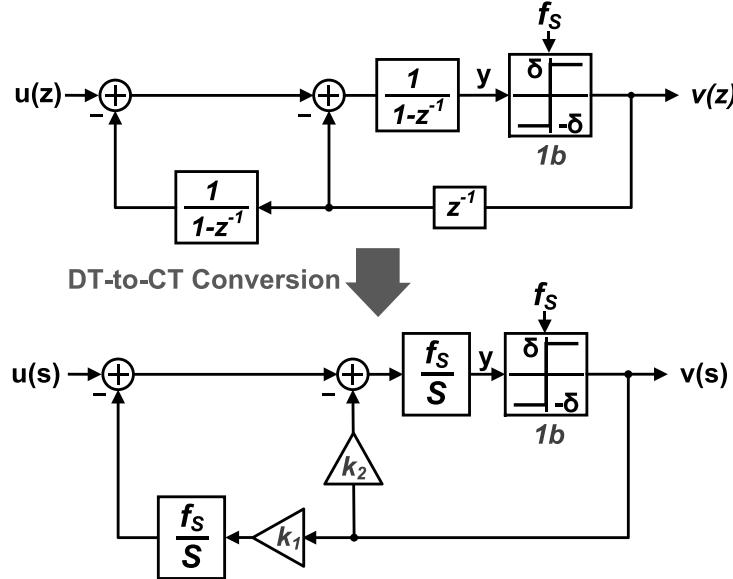


Fig. 7.  $z$ - and  $s$ -domain block diagrams of DT and CT  $\Delta$ - $\Delta\Sigma$  ADC, respectively.

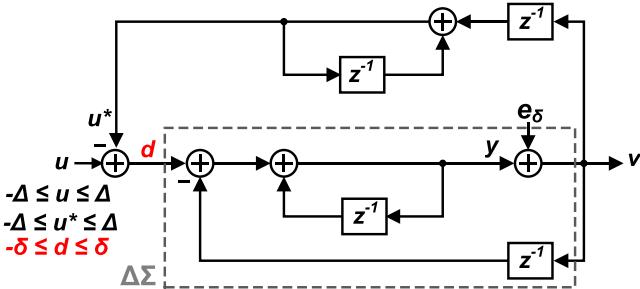


Fig. 8. Decomposed  $z$ -domain block diagram of  $\Delta$ - $\Delta\Sigma$  ADC.

should reject large dc fluctuations (typically, 50–100 mV) coming from electrode-tissue interface [31]. We adopted capacitive-coupled closed-loop feedback [32] and second-stage Miller-compensated operational transconductance amplifier (OTA) techniques. The transfer function of the LNA is given by

$$\frac{V_{\text{out}}}{V_{\text{in}}} \approx \frac{C_{\text{in}}}{C_{\text{fb}}} \frac{s C_{\text{fb}} R_{\text{pseudo}} \left(1 - s \frac{C_{\text{fb}}}{G_{m1} G_{m2} r_{\text{out1}}}\right)}{(1 + s C_{\text{fb}} R_{\text{pseudo}}) \left(1 + s \frac{C_{\text{in}}}{C_{\text{fb}}} \cdot \frac{C_C}{G_{m1}}\right)} \quad (1)$$

where  $C_{\text{in}}$ ,  $C_{\text{fb}}$ ,  $C_C$ , and  $R_{\text{pseudo}}$  are input, feedback, compensation capacitors, and feedback resistors, respectively, and  $G_{m1}$  and  $G_{m2}$  are the transconductances of the first- and second-stage of OTA used for LNA. Input neural signals are coupled to four capacitors  $C_{\text{in}}$  as shown in Fig. 4, and a sub-Hz high-pass corner frequency ( $f_L$ ) is formed to suppress the dc fluctuation by  $C_{\text{fb}}$  and  $R_{\text{pseudo}}$ . Another corner frequency ( $f_H$ ) located at  $\sim 10$  kHz is generated to suppress out-of-band noise by the combination of  $C_{\text{in}}$ ,  $C_C$ ,  $C_{\text{fb}}$ , and  $G_{m1}$ . The mid-band gain of LNA is solely set by the closed-loop feedback formed with  $C_{\text{in}}$  and  $C_{\text{fb}}$  once the open loop gain of OTA is large enough. In our implementation, the open loop gain of OTA is  $> 70$  dB. The feedforward path (a zero) formed by  $C_f$  is

usually located at a high frequency ( $\gg 10$  kHz) once the design parameters meet the following specification:

$$C_f \ll C_C \cdot (G_{m2} \cdot r_{\text{out1}}). \quad (2)$$

The value of  $C_{\text{in}}$  must be selected by considering several design specifications. In order to generate a large closed-loop gain (here,  $\sim 100$  V/V),  $C_{\text{in}}$  must be a few pF since the minimum value of  $C_{\text{fb}}$  ( $\sim 35$  fF) is set by the given  $0.18\text{-}\mu\text{m}$  process. At the same time,  $C_{\text{in}}$  should be chosen small enough to guarantee high input impedance in the frequency range of interests to minimize signal attenuation from the electrode [32], but also large enough to minimize the multiplication effect of the IRN of OTA. The IRN of LNA is given

$$\overline{v_{ni}^2} = \left( \frac{C_{\text{in}} + C_{\text{fb}} + C_{in,p}}{C_{\text{in}}} \right) \cdot \overline{v_{ni,\text{OTA}}^2} \quad (3)$$

where  $C_{in,p}$  is the parasitic input capacitance of OTA (indicated in Fig. 4),  $\overline{v_{ni}^2}$  and  $\overline{v_{ni,\text{OTA}}^2}$  are IRNs of LNA and OTA, respectively. In this design,  $C_{\text{in}}$  and  $C_{\text{fb}}$  are chosen as 4.6 and 45 fF, respectively; thus, the ratio of  $C_{\text{in}}$  to  $C_{\text{fb}}$  makes a mid-band gain of  $\sim 40$  dB and the input impedance at 1 kHz with the given  $C_{\text{in}}$  becomes a few tens of MΩ (found  $\sim 20$  MΩ both in simulation and measurement), which is at least ten times larger than the typical impedance of the microelectrode at the same frequency [33], while minimizing the capacitive multiplication effect (15% in simulation with  $C_p \approx 0.6$  pF). Even though  $C_{\text{in}}$  occupies a large area, it does not significantly contribute to the area overhead since metal-insulator-metal capacitors can be placed on the top of the active circuitry in the given  $0.18\text{-}\mu\text{m}$  process. Near OFF-state PMOS transistors (with parasitic bipolar junction transistors) are used for implementation of a large pseudo resistor  $R_{\text{pseudo}}$ , which is essential to generate  $f_L$  [34]. Since the value of  $R_{\text{pseudo}}$  is vulnerable to process variations, it is designed to be adjusted externally. The noise spectral density from  $R_{\text{pseudo}}$  is

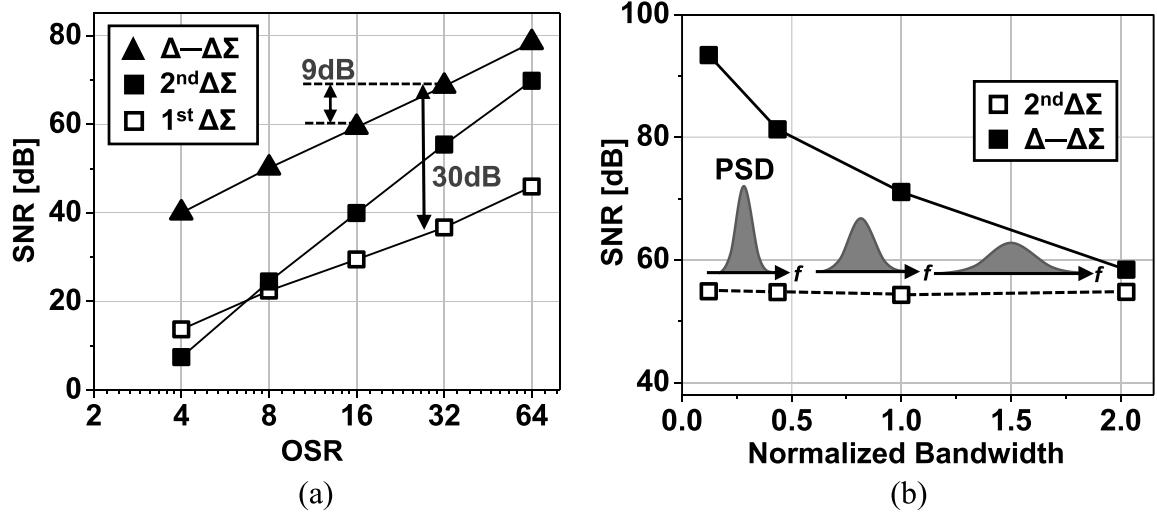


Fig. 9. (a) SNR of first- and second-order  $\Delta$  $\Sigma$  ADCs compared with  $\Delta$ - $\Delta$  $\Sigma$  ADC as a function of various OSRs. (b) SNR simulation of second-order  $\Delta$  $\Sigma$  modulator and  $\Delta$ - $\Delta$  $\Sigma$  ADC for four signals having different bandwidths.

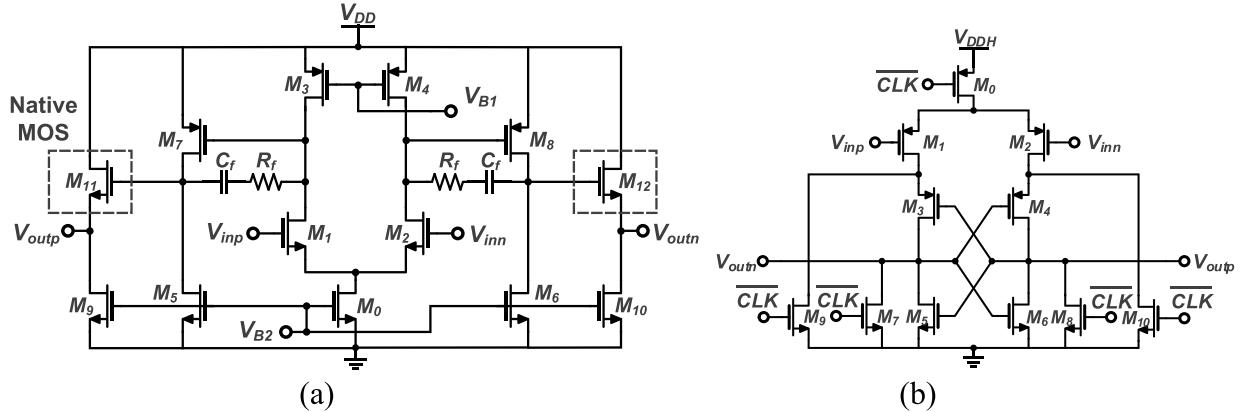


Fig. 10. (a) Circuit schematic of an op-amp used for the second integrator in CT  $\Delta$ - $\Delta$  $\Sigma$  ADC. (b) Dynamic comparator used as a 1-b quantizer for  $\Delta$ - $\Delta$  $\Sigma$  ADC.

given by

$$\overline{v_{ni,R}^2} \approx \overline{v_{n,R}^2} \cdot \left| \frac{C_{fb}/C_{in}}{1 + j\omega R_{pseudo}C_{fb}} \right|^2 \quad (4)$$

where  $\overline{v_{n,R}^2}$  is the thermal noise of  $R_{pseudo}$  and  $C_{in}/C_{fb}$  is  $\sim 100$ . According to (4), the noise beyond  $f_L$  is largely attenuated by both  $C_{fb}/C_{in}$  and  $R_{pseudo} - C_{fb}$  network. Therefore, the noise contribution from  $R_{pseudo}$  is negligible compared to thermal or flicker noise from OTA. The total IRN density of OTA is approximated by

$$\overline{v_{ni,OTA}^2} \approx \frac{16kT}{3} \cdot \left( \frac{1}{g_{m1} + g_{m3}} \right) + \frac{2}{C_{ox}} \cdot \left( \frac{K_n g_{m1}^2}{(WL)_1} + \frac{K_p g_{m3}^2}{(WL)_3} \right) \cdot \left( \frac{1}{g_{m1} + g_{m3}} \right)^2 \cdot \frac{1}{f} \quad (5)$$

where  $k$  is Boltzmann constant,  $T$  is the absolute temperature in Kelvin,  $C_{ox}$  is the oxide capacitance per unit area,  $K_n$  and  $K_p$  are the process-dependent  $1/f$  noise parameters for PMOS and NMOS of the given process, respectively, and  $g_{m1}$  and  $g_{m3}$  are transconductances of  $M_1$  and  $M_3$  in Fig. 5, respectively. To achieve low-noise performance, the input transistors in

OTA are designed to operate in deep subthreshold region where the transconductance efficiency is maximized [35]. The operating conditions of  $M_1$  and  $M_3$  are provided in Fig. 5. In addition, the OTA has two complementary inputs ( $M_1 - M_4$ ) as depicted in Fig. 5. The complementary inputs increase the transconductance of the first stage by a factor of 2, consequently reducing the input-referred thermal noise voltage by a factor of  $\sim \sqrt{2}$ , as given by (5). To reduce  $1/f$  noise, the large area is allocated for input transistors ( $800 \mu\text{m}/0.35 \mu\text{m}$  for  $M_1$  and  $M_2$ , and  $840 \mu\text{m}/0.25 \mu\text{m}$  for  $M_3$  and  $M_4$ , respectively). The simulated IRN of the OTA was  $\sim 3.5 \mu\text{V}_{\text{rms}}$ , and this value is enough to achieve the overall IRN of LNA less than  $5 \mu\text{V}_{\text{rms}}$  even if considering  $\sim 15\%$  multiplication effect in (3).

A single common voltage ( $V_{CM} = V_{DD}/2$ ) cannot effectively provide all the proper dc bias for the input transistors due to low  $V_{DD}$ . The input dc bias for  $M_1$  and  $M_2$  comes from the output CM,  $V_{CM}$ , while that for  $M_3$  and  $M_4$  is generated using two diode-connected PMOS transistors,  $M_{11-13}$  (enclosed by a dashed box in Fig. 5). The low supply voltage also deteriorates the CM rejection ratio (CMRR). In order to reduce the CM gain, we used the dual tail currents ( $M_0$ ,  $M_5$ , and  $M_6$ ).

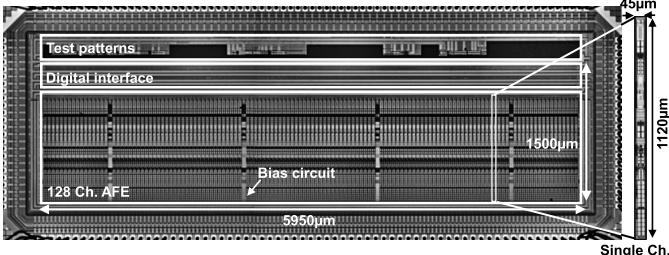


Fig. 11. Microphotograph of the fabricated 128-channel AFE. A single channel is enlarged on the right-hand side.

Since the OTA consists of two stages, it needs a frequency compensation to ensure enough phase margin. A programmable Miller compensation capacitor,  $C_C$  ( $1.5 \pm 0.1$  pF), is used along with a resistor,  $R_Z$ , to null the zero appeared through a feedforward path formed by  $C_C$ . The single CM feedback (CMFB) for two-stage amplifiers can reduce power consumption; however, there might be a dc latch-up in the first stage during the startup process when the output CM voltage is low [36]. We implemented two CMFBs in each stage to prevent the latch-up. The CMFB circuit for the first stage solidly defines the initial bias condition even when the output CM voltage is low enough to turn OFF the pull-down paths ( $M_1$  and  $M_2$ ) during the startup process. The CMFB circuits ( $M_{C0}-M_{C6}$ ,  $M_{C7}-M_{C14}$ ) are shown in Fig. 5. The LNA consumes  $\sim 1.6 \mu\text{A}$  current, and the power consumption remains in sub- $\mu\text{W}$  at 0.5-V supply. The important figure of merits (FoMs), such as noise efficiency factor (NEF) and  $\text{NEF}^2 V_{DD}$  for LNAs, are comparable to other state-of-the-art works or better.

### B. Programmable Gain Amplifier

The PGA is implemented between LNA and  $\Delta-\Delta\Sigma$  ADC to provide an additional gain and drive the input stage of  $\Delta-\Delta\Sigma$  ADC, as shown in Fig. 4. The existence of PGA in neural recording systems is essential to prevent possible circuit saturation since the amplitude of neural signals varies from one recording environment to another. The circuit schematics of PGA are shown in Fig. 6(a). The voltage gain of PGA is adjusted by four switches:  $S_1$  and  $S_2$ , and their complementary ones ( $\bar{S}_1$  and  $\bar{S}_2$ ). A typical approach for gain adjustment is to use switches to change the impedance in the feedback path; however, this scheme may bring signal distortion at very low frequencies due to off-resistance of switches. To avoid this distortion, a flip-over-capacitor scheme has been adopted [37]. Fig. 6(b) shows the flip-over-capacitor configuration when  $S_1$  and  $S_2$  are ON and OFF, respectively. As shown, the OFF-state resistance ( $R_{S1,\text{off}}$  and  $R_{S2,\text{off}}$ ) does not result in low-frequency distortion since they are eliminated from the feedback path. By flipping over each switch to either input or output nodes, four different gains of 0, 3, 9, and 15 dB can be achieved. The dc bias points of PGA are regulated by a fully balanced pseudoresistor with the fixed resistance [ $R_{\text{pseudo}}$  in Fig. 6(a)].  $R_{\text{pseudo}}$  is large enough to ensure its high-pass corner frequency is lower than  $f_L$  of the LNA.

### C. $\Delta-\Delta\Sigma$ Analog-to-Digital Converter

Fig. 7 shows the two equivalent block diagrams of the proposed  $\Delta-\Delta\Sigma$  ADC in both  $z$ - and  $s$ -domains, respectively. The  $\Delta-\Delta\Sigma$  ADC employs a first-order  $\Delta$  modulator followed by a  $\Delta\Sigma$  modulator within single-loop feedback configuration. For digitization, a single-bit quantizer has been chosen for its simplicity and less power and area consumption than a multi-bit quantizer [38]. This ADC is implemented in CT domain because it can outperform DT counterparts in terms of power efficient operation (precisely, smaller bandwidth and slew-rate requirement in the OTAs) [38]. The feedback digital-to-analog converter (DAC) is realized with non-return-zero (NRZ) signals to minimize its sensitivity to clock jitters. The DT loop gain  $L(z)$  of the  $\Delta-\Delta\Sigma$  ADC is given by

$$L(z) = \frac{2z - 1}{(z - 1)^2}. \quad (6)$$

The signal transfer function and noise transfer function (NTF) of the ADC can also be derived as  $1 - z^{-1}$  and  $(1 - z^{-1})^2$ , respectively, from Fig. 7. By applying impulse invariant transformation into (6) with NRZ DAC, the feedback coefficients,  $k_1$  and  $k_2$  for the CT implementation, are obtained as 1 and 1.5, respectively [39]. The overall NTF of  $\Delta-\Delta\Sigma$  ADC is first-order, i.e.,  $(1 - z^{-1})$  if including the off-chip integration to restore the input signals. Fig. 8 illustrates the operation of  $\Delta-\Delta\Sigma$  ADC. The input and output signals of  $\Delta-\Delta\Sigma$  are denoted as  $u$  and  $v$ , respectively, and the dotted line indicates a first-order  $\Delta\Sigma$  ADC. If the range of  $u$  is confined within  $[-\Delta, \Delta]$ , the returning signal  $u^*$  will also be in the same range as  $u$  because  $u^*$  is a delayed replica of  $u$ . Since the  $\Delta\Sigma$  ADC takes a difference between  $u$  and  $u^*$ , denoted as  $d$  having a smaller range of  $[-\delta, \delta]$  than  $[-\Delta, \Delta]$ , the DR of input signals can be significantly reduced. In addition, in this  $\Delta-\Delta\Sigma$  ADC the coefficient scaling is not necessary. The maximum amplitude of signals are only  $u$  and  $u^*$ , and the amplitudes of all the other nodes become much smaller because the operation in the  $\Delta-\Delta\Sigma$  handles only the time difference of  $u$  and  $u^*$ . The gain ( $G$ ) of this  $\Delta-\Delta\Sigma$  ADC over the conventional  $\Delta\Sigma$  ADCs is roughly given by

$$G \approx 20 \log_{10} \left( \frac{\Delta}{\delta} \right). \quad (7)$$

For the comparison with the conventional  $\Delta\Sigma$  ADCs, we simulated the SNRs of  $\Delta-\Delta\Sigma$  ADC along with the first- and second-order  $\Delta\Sigma$  ADCs as a function of various OSRs. The result is plotted in Fig. 9(a). For this simulation, a 100-Hz sinewave is used as an input and the quantization level of conventional ADCs and  $\Delta-\Delta\Sigma$  are set as  $\Delta$  and  $\delta$  ( $\delta/\Delta = 0.03$ ), respectively. As shown in Fig. 9(a), the slope of  $\Delta-\Delta\Sigma$  ADC is almost same as that of the first-order  $\Delta\Sigma$  ADC (+9 dB increase when doubling the OSR); however,  $\Delta-\Delta\Sigma$  ADC shows 30 dB improvement over the first-order  $\Delta\Sigma$  ADC. According to the numerical simulations in Fig. 9(a), the first-order  $\Delta\Sigma$  ADC can achieve 5–6 b resolution at OSR of 32 ( $f_S = 800 \text{ kHz} = f_B \cdot 2 \cdot \text{OSR}$ ,  $f_B = 10 \text{ kHz}$ ). On the contrary, the  $\Delta-\Delta\Sigma$  ADC can achieve >10-b resolution from the additional 30-dB gain from the  $\Delta$ -modulator.

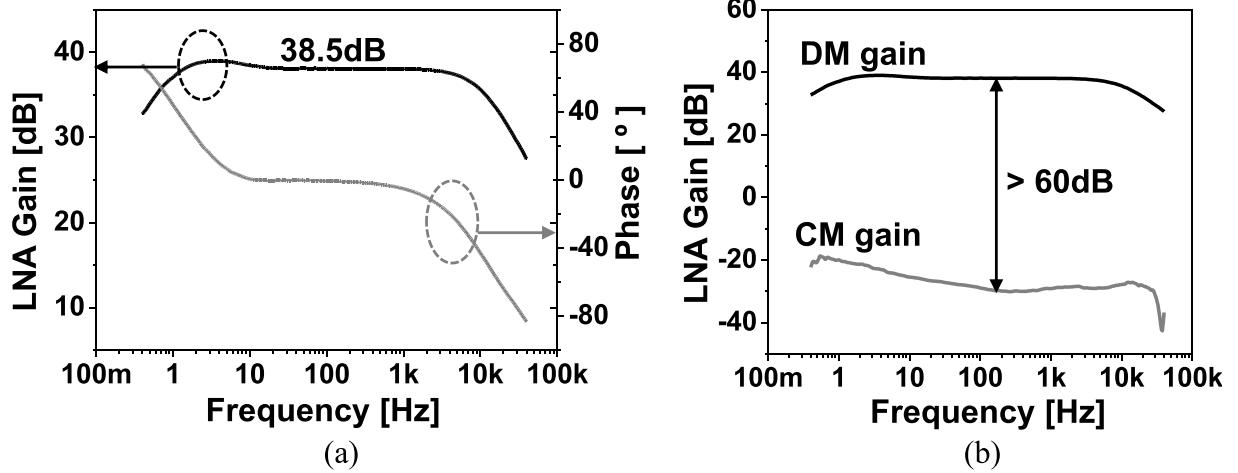


Fig. 12. (a) Measured DM gain and phase response of the fabricated LNA. (b) Comparison between DM and CM gains.

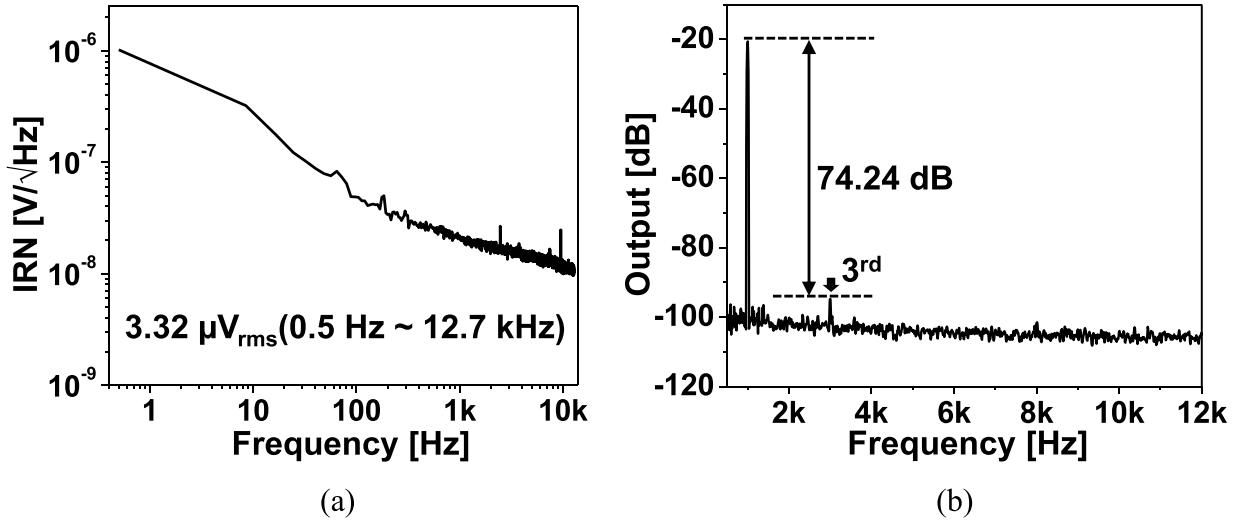


Fig. 13. Measured characteristic of LNA. (a) Input referred noise spectrum from 0.5 to 12.7 kHz and (b) output spectrum with a 3 mVpp, 1 kHz sinewave.

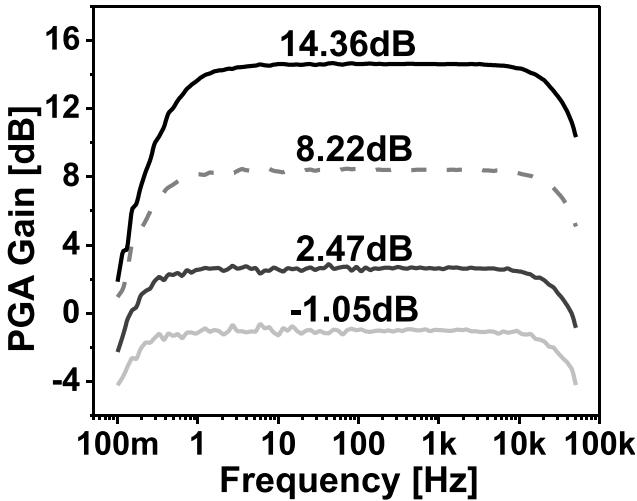


Fig. 14. Measured frequency response of PGA.

The value of  $\delta$  highly depends on signal characteristics. If the input signal resides in relatively lower frequencies than  $f_s$  and has high energy contents at those frequencies,  $\delta$  becomes significantly small. As shown in Fig. 9(b),

we conducted additional numerical simulations at a fixed OSR of 32 for four different sets of input signals where their spectra are distributed differently but the total energies are the same. In Fig. 9(b), the conceptual power spectral density functions are also depicted for the corresponding signals in three representative bandwidths. While the SNRs of the conventional second-order  $\Delta\Sigma$  ADC stays almost constant regardless of input spectral shapes, the SNRs of the proposed  $\Delta$ - $\Delta$  $\Sigma$  ADC increases significantly as the energy of signals is more concentrated in lower frequencies. These characteristics strongly support the idea why the proposed  $\Delta$ - $\Delta$  $\Sigma$  ADC is particularly beneficial for processing neural signals since the high energy spectra of LFPs mostly resides in the low-frequency range ( $<300$  Hz) while that of low energy APs occupies from a few to 10 kHz. However,  $\delta$  cannot be indefinitely small since it may cause system instability once the time difference of input signals ( $d$ ) becomes larger than the pre-determined value of  $\delta$ . If we define a ratio of  $\delta$  to  $\Delta$  as  $k$ , then the minimum value of  $k$  should meet the following condition:

$$k \geq \frac{1}{f_s} \cdot \left| \frac{1}{u(t)} \cdot \frac{du(t)}{dt} \right|_{\max} \quad (8)$$

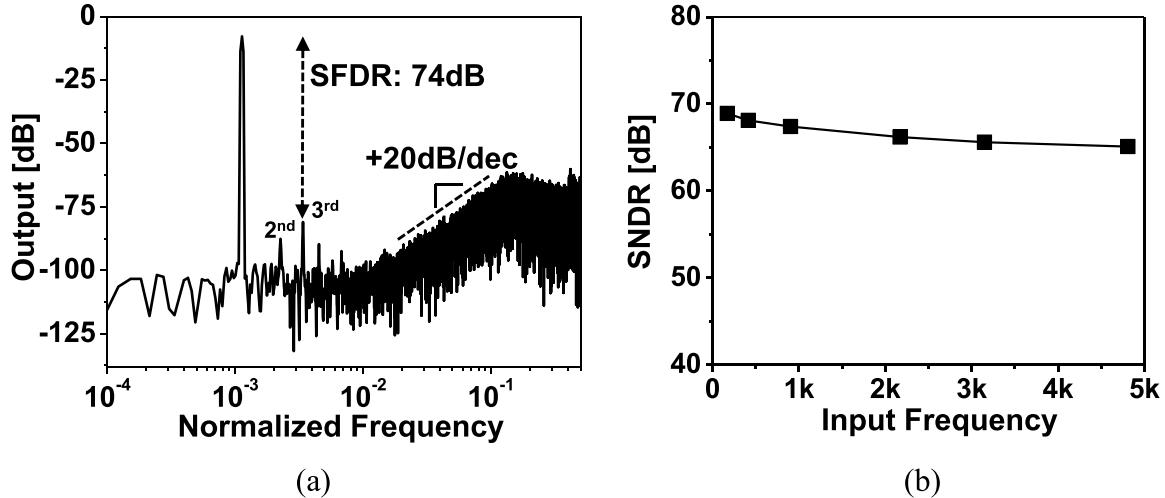


Fig. 15. (a) 32768-point FFT of output signals from  $\Delta\text{-}\Delta\Sigma$  ADC for  $\sim 1$  kHz sine waves. (b) FFT results with difference input frequencies.

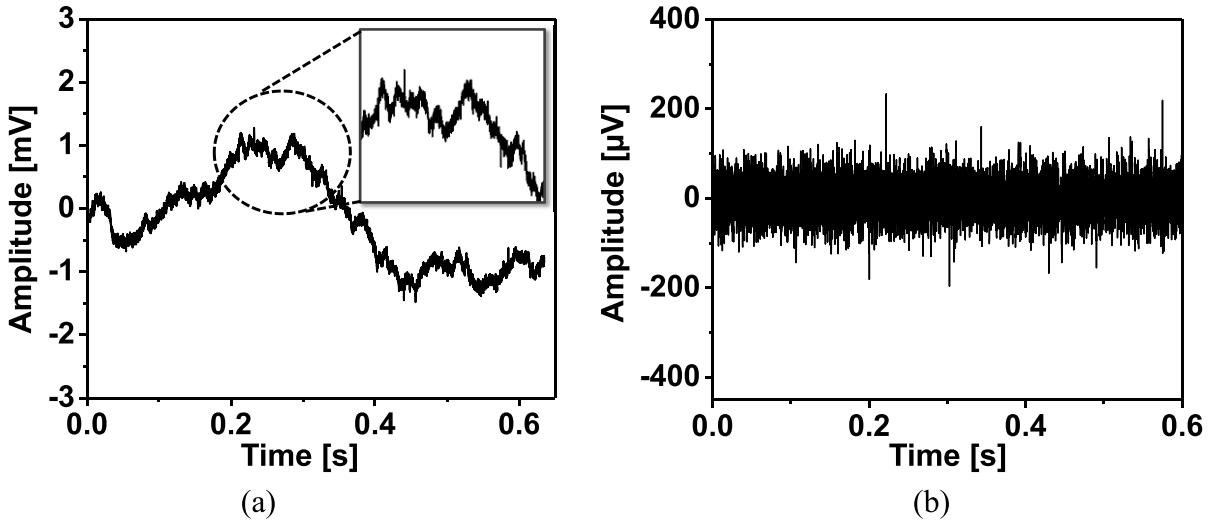


Fig. 16. (a) Snapshot of *in vivo* measurements for broadband neural signals including LFPs and spikes. (b) Spike signals extracted through a software bandpass filter after post-processing.

where  $f_S$  is a sampling rate and  $u(t)$  is the input signal of ADC. In this implementation, we set the values of  $k$  and  $f_S$  as 0.025–0.25 (adjustable) and 800 kHz, respectively, based on the numerical simulation results using the pre-recoded neural signals for a given power budget of  $\sim 2 \mu\text{W}$ .

As shown in Fig. 4, the  $\Delta\text{-}\Delta\Sigma$  ADC consists of two DACs, two integrators, and a dynamic comparator. The DAC is implemented with NMOS switches, passives, and reference voltages. The adjustment of a quantizer level ( $\delta$ ) is realized by setting the reference voltages ( $V_{\text{REFP}}$  and  $V_{\text{REFN}}$ ) and the values of passives ( $R_3$  and  $R_4$ ) in the feedback path. Without coefficient scaling, the gain of the integrators is 1. The nominal values of  $C_4$  and  $C_5$  are set to be 2 pF, where  $R_1$  and  $R_2$  are 625 k $\Omega$ . This gives the optimum area allocation between resistors and capacitors. All capacitance and resistance values are programmable up to  $\pm 20\%$  to cope with process variations. The simulated overall integrated IRN of the proposed  $\Delta\text{-}\Delta\Sigma$  ADC is  $\sim 23.9 \mu\text{V}_{\text{rms}}$  that would not significantly

affect the overall SNR of the whole signal acquisition chain.

Fig. 10(a) shows the circuit schematic of the op-amp used for the second integrator (CMFB not shown). The gain, bandwidth, and linearity requirement of the op-amp for the second integrator are more stringent than those of the op-amp for the first integrator, since it should generate the delayed replica of input signals. It consists of two stages with a Miller compensation network using passives ( $C_f$  and  $R_f$ ) with an additional output driving stage. The output stage is a buffer to drive the first integrator without gain degradation. Instead of using PMOS transistors which may favorably lower 1/ $f$  noise, large ( $W = 360 \mu\text{m}$ ) NMOS transistors ( $M_1$  and  $M_2$ ) are used to maximize the input transconductance.  $M_0\text{--}M_{10}$  are standard 1.8-V transistors while  $M_{11}$  and  $M_{12}$  are native transistors to provide a proper output CM level without severe voltage drop. Even though this is a two-stage OTA, we only use one CMFB since it will not suffer from latch-up due to low

TABLE I  
PERFORMANCE SUMMARY AND COMPARISON WITH RECENT OTHER WORKS

	[7]	[8]	[19]	[21]	[22]	[28]	This work
Power/Ch. [ $\mu\text{W}$ ]	7.02	4.7	68	5.04	0.73	0.63	<b>3.05</b>
IRN [ $\mu\text{V}_{\text{rms}}$ ]	3.2	6.36	2.2	4.9/4.3	3.2	1.13	<b>3.32</b>
Bandwidth [kHz]	6	10	10	10	10	0.5	<b>10.9</b>
NEF	3.08	—	4.5	5.99	1.57	2.86	<b>3.02</b>
NEF <sup>2</sup> $V_{\text{DD}}$	17.13	—	<sup>1)</sup> 24.3	17.96	1.12	9.82	<b>4.56</b>
CMRR [dB]	60	> 60	—	75	73	—	<b>&gt; 60</b>
ADC ENOB	9.2	—	9.72	7.15	8.27	<sup>1)</sup> 11.7	<b>10.9</b>
ADC $f_s$ [kHz]	<sup>1)</sup> 30	30	31.25	20	<sup>1)</sup> 20	<sup>1)</sup> 1	<b>25</b>
Ch. Multiplexing	Yes	Yes	No	No	Yes	No	<b>No</b>
FoM	84	42	219.7	22	22	<sup>1)</sup> 189.4	<b>35.2</b>
[fJ/C-s]	Ch. FoM	<sup>1)</sup> 397.9	<sup>1)</sup> 152.9	<sup>1)</sup> 2580	<sup>1)</sup> 1774.3	<sup>1)</sup> 118.2	<sup>3)</sup> <b>108.83</b>
E-A FoM		<sup>1)</sup> 75.60	<sup>1)</sup> 18.36	<sup>1)</sup> 670.8	<sup>1)</sup> 23.07	<sup>1)</sup> 21.28	<sup>3)</sup> <b>6.34</b>
Recording channels	54	384	96	1	100	64	<b>128</b>
Supply voltage [V]	1.8	1.2/1.8	1.2	0.5	0.45/1.0	1.2/3.3	<b>0.5/1.0</b>
Area/Ch. [ $\text{mm}^2$ ]	<sup>2)</sup> 0.19	<sup>2)</sup> 0.12	0.26	0.013	0.18	0.013	<sup>3)</sup> <b>0.058</b>
Technology	0.18 $\mu\text{m}$	0.13 $\mu\text{m}$ SOI	0.13 $\mu\text{m}$	65nm	0.18 $\mu\text{m}$	0.13 $\mu\text{m}$	<b>0.18<math>\mu\text{m}</math></b>

1) Estimated, 2) Included I/O and digital interface, 3) On-chip decimation filter included.

input dc voltage. The output CM voltage is controlled via  $V_{B1}$  in Fig. 10(a). Fig. 10(b) shows the schematic of the dynamic comparator used for 1-b quantization. For this comparator, 1-V supply is used to enhance the decision time and directly interface with the following digital circuits.

#### D. Decimation Filter

For extension of a modular architecture to a large number of channels over 1000, the data from a modular 128-channel chip is serialized into a single bit. However, the 1-b serialization of 128 channels at 800 kHz makes an output data rate over 100 Mb/s, which results in high power consumption for data transmission. A better tradeoff is to implement an on-chip decimation filter in each individual channel to reduce the data rate; but this will inevitably result in additional area overhead. We have implemented a second-order sinc filter to decimate the output bit stream from ADC. Since overall NTF of ADC including the off-chip signal restoration is first order, a sinc<sup>2</sup> filter can provide enough attenuation of out-band noise [30]. Even though the sinc<sup>2</sup> filter introduces a droop into the in-band frequency response, the degradation is less 0.5 dB that is negligible when compared with 60-dB SNR requirement. The sinc<sup>2</sup> filter is implemented by digital circuits using automatic place-and-routing, and it occupies a small area of 0.00822  $\text{mm}^2$  and consumes a power of  $\sim 0.38 \mu\text{W}$ .

#### IV. EXPERIMENTAL RESULTS

The proposed  $\Delta$ - $\Delta$  $\Sigma$  AFE architecture has been fabricated using 0.18- $\mu\text{m}$  1P6M CMOS processes. Fig. 11 shows a

microphotograph of the fabricated chip. The 128-channel AFE occupies an area of  $5950 \times 1500 \mu\text{m}^2$  excluding pads. There are four identical bias circuits and each is shared by 32 channels. The enlarged picture shows a single-channel AFE which occupies  $45 \times 1120 \mu\text{m}^2$  with 5- $\mu\text{m}$  channel separation to reduce the crosstalk between channels. There are 132 pads on the bottom side for inputs. 128 pads out of 132 are assigned to each positive input of 128 channels and four pads are connected to the shared negative inputs of the AFE (32 channels in one shared group).

#### A. Performance Measurement

The measured frequency response of LNA is shown in Fig. 12. The LNA forms a mid-band gain of 38.5 dB with  $f_L$  of 0.4 Hz and  $f_H$  of 10.9 kHz, respectively. Fig. 12(b) shows differential mode (DM) and CM gains. The CM gain is less than  $-20$  dB in the entire range of frequencies of interest, giving a CMRR of over 60 dB. The IRN of LNA, measured using the agilent dynamic signal analyzer 35670A, is shown in Fig. 13(a). The integrated IRN from 0.5 Hz to 12.7 kHz is  $3.32 \mu\text{V}_{\text{rms}}$ , smaller than  $10 \mu\text{V}_{\text{rms}}$ , a typical noise value required for neural amplifiers [31]. Fig. 13(b) shows the harmonic tones from LNA from a sinusoidal input of 1 kHz and 3 mV<sub>pp</sub>. The third tone was reduced by  $\sim 74$  dB from the fundamental tone. The gain of PGA is measured as shown in Fig. 14. The four different voltage gains: 0, 3, 9, and 15 dB can be selected by changing the settings in the PGA, and those are measured as  $-1.05$ , 2.47, 8.22, and 14.36 dB as shown in Fig. 14. The power consumption of PGA

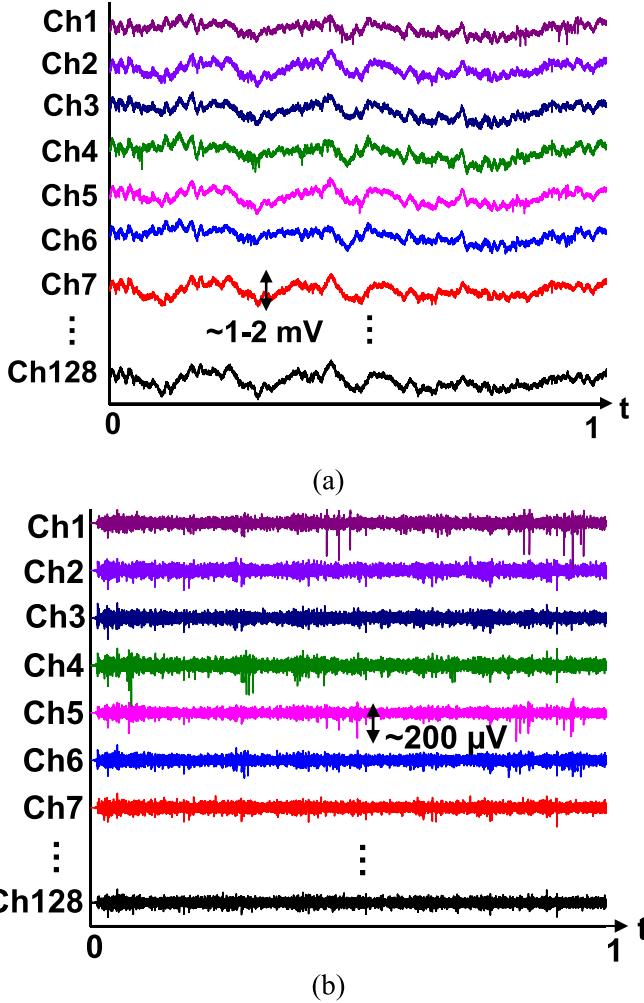


Fig. 17. 1-s *in vivo* data from multi-channel recordings. (a) Broadband neural signals including both LFPs and spikes. (b) Bandpass-filtered spikes after post-processing.

is 0.42  $\mu\text{W}$ . Fig. 15(a) depicts the fast Fourier transform (FFT) analysis of the fabricated  $\Delta - \Delta\Sigma$  ADC after the reconstruction. The third harmonic tone is measured as  $-86$  dB. The spurious-free DR is  $\sim 74$  dB, and the calculated signal-to-noise-and-distortion ratio (SNDR) is  $\sim 67.4$  dB, equivalent to  $\sim 10.9$  b effective number of bit (ENOB). The output band noise is asymptotic to a  $+20$  dB/dec line that is a typical frequency characteristic of  $\Delta\Sigma$  ADCs. Fig. 15(b) shows the SNDR measured with the sine waves having different input frequencies. The power consumption of ADC is measured as  $1.68 \mu\text{W}$ , and the FoM of ADC is  $35.2 \text{ fJ/C}\cdot\text{s}$ . The channel crosstalk was also measured, and it is undistinguishable from the thermal noise ( $<-100$  dB) due to the proposed independent channel structure (not depending on the time-division multiplexing) and the  $5\text{-}\mu\text{m}$  channel separation in the layout.

#### B. In Vivo Measurement

For *in vivo* signal measurements, a silicon multi-shank probe was implanted in the neo-cortex of a rodent and interfaced with the fabricated chip. Fig. 16(a) and (b) shows a 0.6-s snapshot

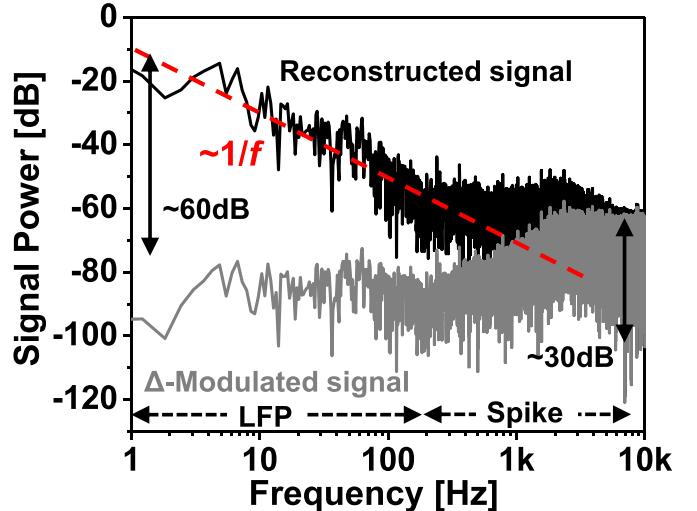


Fig. 18. Spectra of the recorded and reconstructed neural signals from *in vivo* measurements.

of the recorded broadband neural signals (LFP + spikes) and the spikes after bandpass filtering with 0.3- and 7.5-kHz corner frequencies, respectively. For clear visualization, the part of the recorded broadband signal is enlarged in Fig. 16(a). Small spikes which have an amplitude of  $\sim 200 \mu\text{V}$  are superimposed with the relatively large fluctuation of LFPs around 1.2 mV in amplitude. Fig. 17 shows the 1-s broadband waveforms recorded from the 128 channels to verify the feasibility of multi-channel recording (only a few channels are included in the plot). Similar to Fig. 16, the broadband waveform of both LFPs and spikes are plotted in Fig. 17(a) and the bandpass filtered spikes in Fig. 17(b). While the amplitude of LFPs spans around a few mV ( $\sim 1\text{-}2 \text{ mV}_{\text{pp}}$ ), that of spikes does around a few hundred  $\mu\text{V}$  ( $\sim 200 \mu\text{V}_{\text{pp}}$ ). Fig. 18 shows the power spectra of the reconstructed and spectrum-equalized neural signals. As expected, the power spectrum of the retrieved signals exhibits a  $\sim 1/f$  slope where the energy of signals is mostly distributed in the LFP regime. The full signal range of  $>60$  dB is modulated on-chip by the built-in  $\Delta$ -modulator into a smaller DR of  $\sim 30$  dB, and then the compressed signals are fully recovered by the off-chip  $\Sigma$ -modulation, as shown in Fig. 18.

#### C. Performance Comparison

The performance summary and comparison with the state-of-the-art works are given in Table I. For fair comparison, we define a channel FoM (Ch.FoM) as

$$\text{Ch.FoM} = \frac{P_{\text{Ch}}}{2^{\text{ENOB},\text{Ch}} \cdot f_S} \quad (9)$$

where  $P_{\text{Ch}}$  is the power consumption of a single-channel AFE, and ENOB, Ch is the measured maximum ENOB from the output of AFE. The Ch.FoM has the same analytic form as Walden's FoM widely used for performance comparison of ADCs [40]. It can fairly and also easily evaluate the performance of AFEs by simply replacing power and ENOB of ADCs with those of AFEs. Obviously, a larger ENOB

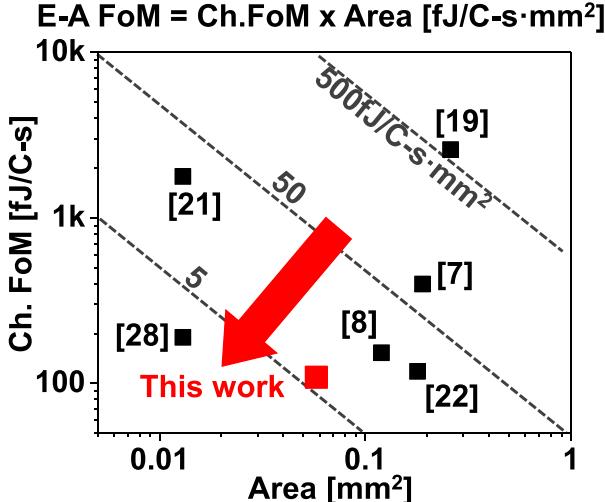


Fig. 19. E-A FoM compared with the previous state-of-the-art works.

with small power consumption gives better performance. The gain of AFEs does not affect Ch.FoM since it deteriorates SNDR, once the gain increases to the point where signals are distorted. From our fabricated chip, we have achieved Ch.FoM of 108.83 fJ/C·s with 10.3-b resolution. We have also evaluated another FoM, called energy-area FoM (E-A FoM). E-A FoM indicates how efficiently both area and energy are used for the realization of AFEs. The performance of the fabricated AFE has been compared with other state-of-the-art works in Table I and Fig. 19, using these new FoMs (Ch.FoM and E-A FoM). The E-A FoM can indicate the desired technology direction for scaling the number of recording channels, illustrated by an arrow in Fig. 19. Our work has achieved the E-A FoM of 6.34 fJ/C·s·mm<sup>2</sup>.

## V. CONCLUSION

We report an energy- and area-efficient 128-channel AFE architecture incorporating  $\Delta$ -modulated  $\Delta$  $\Sigma$  signal acquisition as a modular platform for high-density recording of brain activities over 1024 channels. The implemented  $\Delta$ - $\Delta$  $\Sigma$  AFE circuits employ spectrum equalizing and CT- $\Delta$  $\Sigma$  quantization to exploit the inherent spectral characteristics of brain signals in an energy and area efficient manner. From on-chip  $\Delta$ -modulation, the DR of the acquired signals has been compressed by  $\sim$ 30 dB and the fabricated AFE has achieved the decent energy-area product, 6.34 fJ/C·s·mm<sup>2</sup>, among the state-of-the-art works reported up to date, which is critical for scaling in massive-parallel neural recording systems. The fabricated chip consumes an area of 0.05 mm<sup>2</sup> and 3.05  $\mu$ W per channel and 63.8 dB SNDR, 3.02 NEF, and 4.56 NEF<sup>2</sup>V<sub>DD</sub>.

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