

IS31FL3733B

12×16 DOTS MATRIX LED DRIVER WITH INDIVIDUAL AUTO BREATH FUNCTION

October 2024

GENERAL DESCRIPTION

The IS31FL3733B is a general purpose 12×16 LEDs matrix driver with 1/12 cycle rate. The device can be programmed via an I2C compatible interface. Each LED can be dimmed individually with 8-bit PWM data which allowing 256 steps of linear dimming.

IS31FL3733B features 3 Auto Breathing Modes which are noted as ABM-1, ABM-2 and ABM-3. For each Auto Breathing Mode, there are 4 timing characters which include current rising / holding / falling / off time and 3 loop characters which include Loop-Beginning / Loop-Ending / Loop-Times. Every LED can be configured to be any Auto Breathing Mode or No-Breathing Mode individually.

Additionally each LED open and short state can be detected, IS31FL3733B store the open or short information in Open-Short Registers. The Open-Short Registers allowing MCU to read out via I2C compatible interface. Inform MCU whether there are LEDs open or short and the locations of open or short LEDs.

The IS31FL3733B operates from 2.7V to 5.5V and features a very low shutdown and operational current.

IS31FL3733B is available in QFN-48 (6mm×6mm) and eTQFP-48 packages. It operates from 2.7V to 5.5V over the temperature range of -40°C to +125°C.

FEATURES

- Supply voltage range: 2.7V to 5.5V
- 16 current source outputs for row control
- 12 switch current inputs for column scan control
- Up to 192 LEDs (12×16) in dot matrix
- Programmable 12×16 (64 RGBs) matrix size with de-ghost function
- 1MHz I2C-compatible interface
- Selectable 3 Auto Breath Modes for each dot
- Auto Breath Loop Features interrupt pin inform MCU Auto Breath Loop completed
- Auto Breath offers 128 steps gamma current, interrupt and state look up registers
- 1.05kHz/ 2.1kHz/ 4.2kHz/ 8.4kHz/ 26.7kHz PWM frequency options
- 256 steps Global Current Setting
- Individual on/off control
- Individual 256 PWM control steps
- Individual Auto Breath Mode select
- Individual open and short error detect function
- Cascade for synchronization of chips
- QFN-48 (6mm×6mm) and eTQFP-48 packages
- RoHS & Halogen-Free Compliance
- TSCA Compliance

APPLICATIONS

- Hand-held devices for LED display
- Gaming device (Keyboard, Mouse etc.)
- LED in white goods application

IS31FL3733B

TYPICAL APPLICATION CIRCUIT

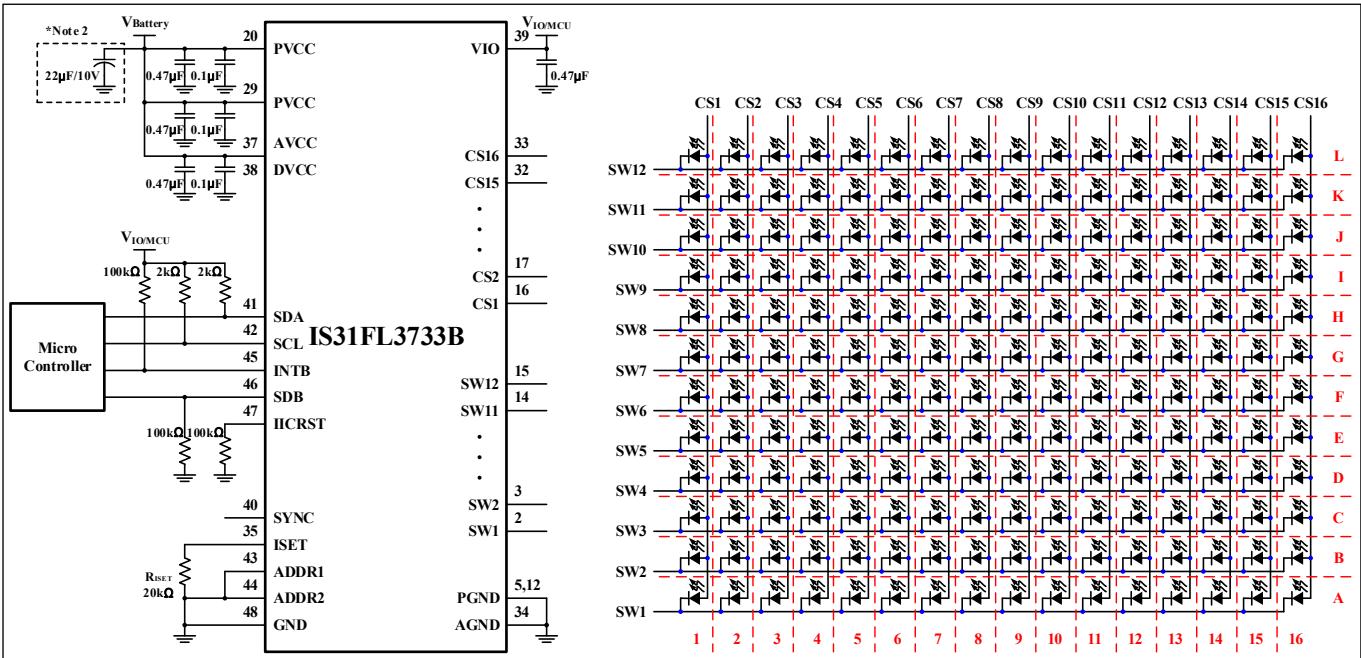


Figure 1 Typical Application Circuit (12×16)

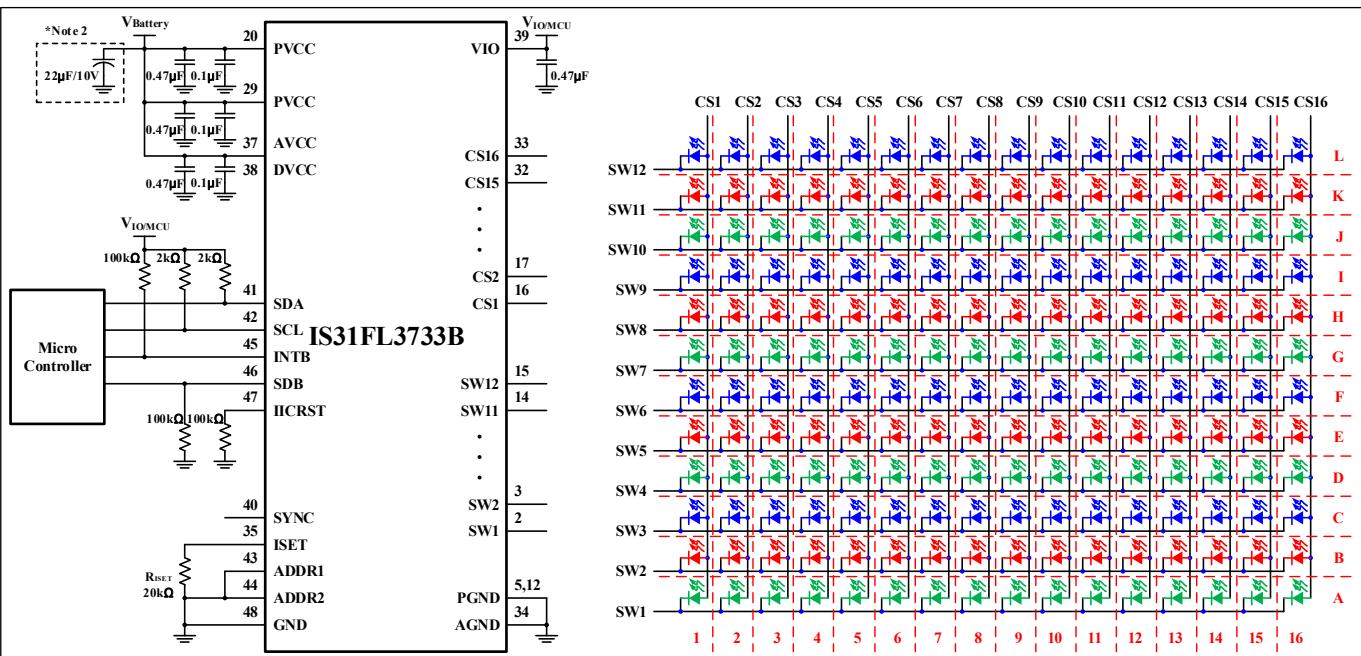


Figure 2 Typical Application Circuit (RGB)

IS31FL3733B

TYPICAL APPLICATION CIRCUIT (CONTINUED)

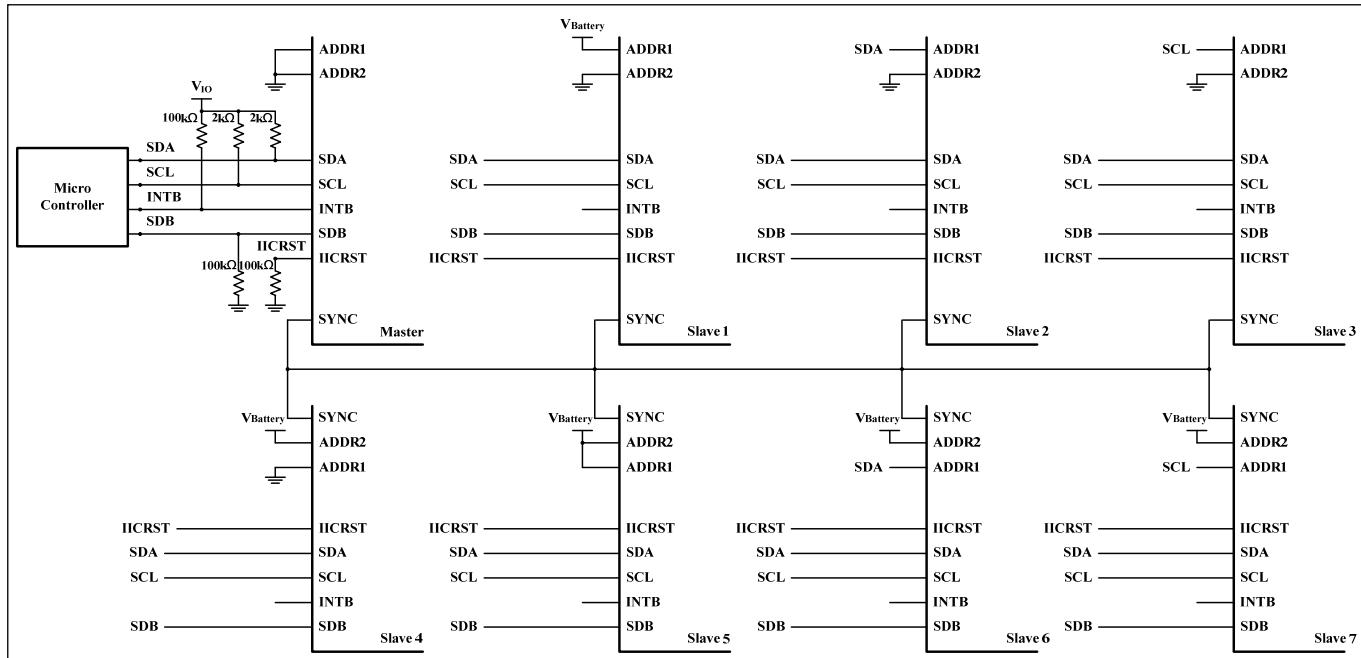


Figure 3 Typical Application Circuit (Eight Parts Synchronization-Work)

Note 1: IC should be placed far away from the antenna in order to prevent the EMI.

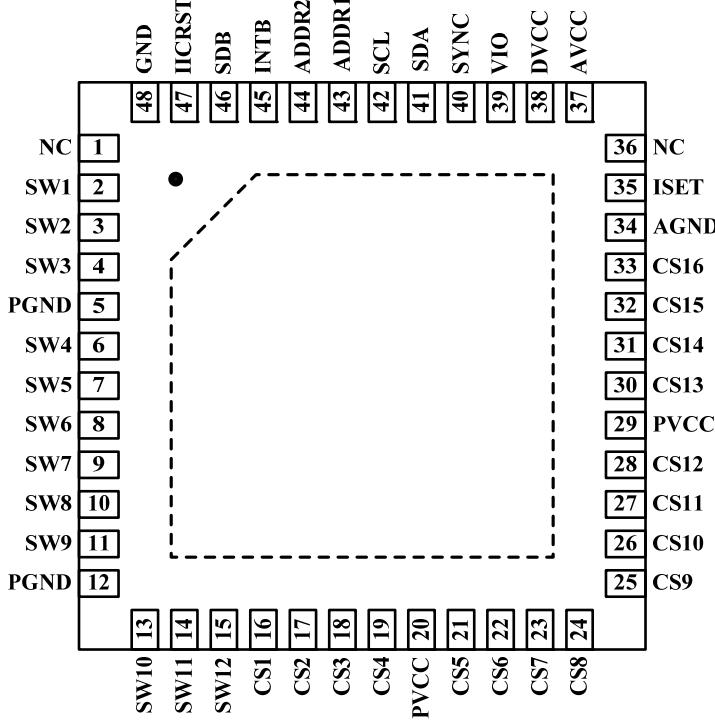
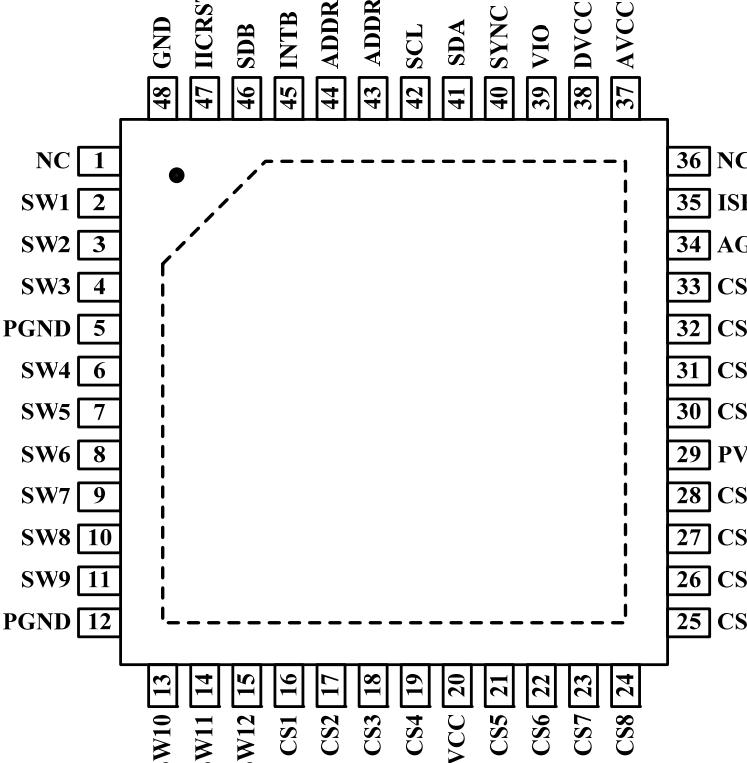
Note 2: Electrolytic/Tantalum Capacitor maybe considered for high current application to avoid audible noise interference.

Note 3: The V_{IO} should be $1.8V \leq V_{IO} \leq V_{CC}$. And it is recommended to be equal to V_{OH} of the micro controller. For example, if V_{OH}=1.8V, set V_{IO}=1.8V, if V_{OH}=3.3V, set V_{IO}=3.3V.

Note 4: One system should contain only one master, all slave parts should be configured as slave mode before the master is configured as master mode. Work as master mode or slave mode specified by Configuration Register (Function register, address 00h). Master part output master clock, and all the other parts which work as slave input this master clock.

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PIN CONFIGURATION

| Package | Pin Configuration (Top View) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|---|---------|---------|----|-----|-----|---|----|--------|-----|---|----|-----|-----|---|----|------|------|---|----|-------|-----|---|----|-------|-----|---|----|-----|-----|---|----|-----|-----|---|----|------|-----|----|----|-----|-----|----|----|------|------|----|----|------|--|---------|---------|---------|--|--------|--------|--------|--|--------|--------|--------|--|---------|--------|--------|
| QFN-48 |  <table border="0"> <tr><td>NC</td><td>1</td><td>48</td><td>GND</td></tr> <tr><td>SW1</td><td>2</td><td>47</td><td>IICRST</td></tr> <tr><td>SW2</td><td>3</td><td>46</td><td>SDB</td></tr> <tr><td>SW3</td><td>4</td><td>45</td><td>INTB</td></tr> <tr><td>PGND</td><td>5</td><td>44</td><td>ADDR2</td></tr> <tr><td>SW4</td><td>6</td><td>43</td><td>ADDR1</td></tr> <tr><td>SW5</td><td>7</td><td>42</td><td>SCL</td></tr> <tr><td>SW6</td><td>8</td><td>41</td><td>SDA</td></tr> <tr><td>SW7</td><td>9</td><td>40</td><td>SYNC</td></tr> <tr><td>SW8</td><td>10</td><td>39</td><td>VIO</td></tr> <tr><td>SW9</td><td>11</td><td>38</td><td>DVCC</td></tr> <tr><td>PGND</td><td>12</td><td>37</td><td>AVCC</td></tr> <tr><td></td><td>SW10 13</td><td>SW11 14</td><td>SW12 15</td></tr> <tr><td></td><td>CS1 16</td><td>CS2 17</td><td>CS3 18</td></tr> <tr><td></td><td>CS4 19</td><td>CS5 20</td><td>CS6 21</td></tr> <tr><td></td><td>PVCC 22</td><td>CS7 23</td><td>CS8 24</td></tr> </table> | NC | 1 | 48 | GND | SW1 | 2 | 47 | IICRST | SW2 | 3 | 46 | SDB | SW3 | 4 | 45 | INTB | PGND | 5 | 44 | ADDR2 | SW4 | 6 | 43 | ADDR1 | SW5 | 7 | 42 | SCL | SW6 | 8 | 41 | SDA | SW7 | 9 | 40 | SYNC | SW8 | 10 | 39 | VIO | SW9 | 11 | 38 | DVCC | PGND | 12 | 37 | AVCC | | SW10 13 | SW11 14 | SW12 15 | | CS1 16 | CS2 17 | CS3 18 | | CS4 19 | CS5 20 | CS6 21 | | PVCC 22 | CS7 23 | CS8 24 |
| NC | 1 | 48 | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW1 | 2 | 47 | IICRST | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW2 | 3 | 46 | SDB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW3 | 4 | 45 | INTB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PGND | 5 | 44 | ADDR2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW4 | 6 | 43 | ADDR1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW5 | 7 | 42 | SCL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW6 | 8 | 41 | SDA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW7 | 9 | 40 | SYNC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW8 | 10 | 39 | VIO | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW9 | 11 | 38 | DVCC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PGND | 12 | 37 | AVCC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | SW10 13 | SW11 14 | SW12 15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | CS1 16 | CS2 17 | CS3 18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | CS4 19 | CS5 20 | CS6 21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | PVCC 22 | CS7 23 | CS8 24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| eTQFP-48 |  <table border="0"> <tr><td>NC</td><td>1</td><td>48</td><td>GND</td></tr> <tr><td>SW1</td><td>2</td><td>47</td><td>IICRST</td></tr> <tr><td>SW2</td><td>3</td><td>46</td><td>SDB</td></tr> <tr><td>SW3</td><td>4</td><td>45</td><td>INTB</td></tr> <tr><td>PGND</td><td>5</td><td>44</td><td>ADDR2</td></tr> <tr><td>SW4</td><td>6</td><td>43</td><td>ADDR1</td></tr> <tr><td>SW5</td><td>7</td><td>42</td><td>SCL</td></tr> <tr><td>SW6</td><td>8</td><td>41</td><td>SDA</td></tr> <tr><td>SW7</td><td>9</td><td>40</td><td>SYNC</td></tr> <tr><td>SW8</td><td>10</td><td>39</td><td>VIO</td></tr> <tr><td>SW9</td><td>11</td><td>38</td><td>DVCC</td></tr> <tr><td>PGND</td><td>12</td><td>37</td><td>AVCC</td></tr> <tr><td></td><td>SW10 13</td><td>SW11 14</td><td>SW12 15</td></tr> <tr><td></td><td>CS1 16</td><td>CS2 17</td><td>CS3 18</td></tr> <tr><td></td><td>CS4 19</td><td>CS5 20</td><td>CS6 21</td></tr> <tr><td></td><td>PVCC 22</td><td>CS7 23</td><td>CS8 24</td></tr> </table> | NC | 1 | 48 | GND | SW1 | 2 | 47 | IICRST | SW2 | 3 | 46 | SDB | SW3 | 4 | 45 | INTB | PGND | 5 | 44 | ADDR2 | SW4 | 6 | 43 | ADDR1 | SW5 | 7 | 42 | SCL | SW6 | 8 | 41 | SDA | SW7 | 9 | 40 | SYNC | SW8 | 10 | 39 | VIO | SW9 | 11 | 38 | DVCC | PGND | 12 | 37 | AVCC | | SW10 13 | SW11 14 | SW12 15 | | CS1 16 | CS2 17 | CS3 18 | | CS4 19 | CS5 20 | CS6 21 | | PVCC 22 | CS7 23 | CS8 24 |
| NC | 1 | 48 | GND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW1 | 2 | 47 | IICRST | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW2 | 3 | 46 | SDB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW3 | 4 | 45 | INTB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PGND | 5 | 44 | ADDR2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW4 | 6 | 43 | ADDR1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW5 | 7 | 42 | SCL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW6 | 8 | 41 | SDA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW7 | 9 | 40 | SYNC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW8 | 10 | 39 | VIO | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW9 | 11 | 38 | DVCC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PGND | 12 | 37 | AVCC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | SW10 13 | SW11 14 | SW12 15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | CS1 16 | CS2 17 | CS3 18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | CS4 19 | CS5 20 | CS6 21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | PVCC 22 | CS7 23 | CS8 24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

IS31FL3733B

PIN DESCRIPTION

| No. | Pin | Description |
|------------------------|-------------|--|
| 1,36 | NC | Not connect. |
| 2~4,6~11, 13~15 | SW1~SW12 | Switch pin for LED matrix scanning. |
| 5,12 | PGND | Power GND. |
| 16~19, 21~28, 30~33 | CS1~CS16 | Current Source. |
| 20, 29 | PVCC | Power for current source. |
| 34 | AGND | Analog GND. |
| 35 | ISET | Input terminal used to connect an external resistor. This regulates current source DC current value. |
| 37 | AVCC | Power for analog circuits. |
| 38 | DVCC | Power for digital circuits. |
| 39 | VIO | Input logic reference voltage. |
| 40 | SYNC | Synchronize pin. It is used for more than one part work synchronize. If it is not used please float this pin. |
| 41 | SDA | I2C compatible serial data. |
| 42 | SCL | I2C compatible serial clock. |
| 43 | ADDR1 | I2C address setting. |
| 44 | ADDR2 | I2C address setting. |
| 45 | INTB | Open drain, interrupt output pin. Register F0h sets the function of the INTB pin and active low when the interrupt event happens. Can be NC (float) if interrupt function no used. |
| 46 | SDB | Shutdown the chip when pull to low. |
| 47 | IICRST | Reset I2C when pull high, need to pull down when normal operation. |
| 48 | GND | Connect to GND. |
| | Thermal Pad | Need to connect to GND pins. |

IS31FL3733B

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

| Order Part No. | Package | QTY/Reel |
|----------------------|---------------------|----------|
| IS31FL3733B-QFLS4-TR | QFN-48, Lead-free | 2500 |
| IS31FL3733B-TQLS4-TR | eTQFP-48, Lead-free | |

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- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Lumissil Microsystems is adequately protected under the circumstances

IS31FL3733B

ABSOLUTE MAXIMUM RATINGS

| | |
|--|----------------------------------|
| Supply voltage, V_{CC} | -0.3V ~ +6.0V |
| Voltage at any input pin | -0.3V ~ $V_{CC}+0.3V$ |
| Maximum junction temperature, T_{JMAX} | +150°C |
| Storage temperature range, T_{STG} | -65°C ~ +150°C |
| Operating temperature range, $T_A=T_J$ | -40°C ~ +125°C |
| Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA} | 37.5°C/W (QFN) 39°C/W (eTQFP) |
| ESD (HBM) | ±8kV |
| ESD (CDM) | ±750V |

Note 5: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for $V_{CC}= 3.6V$, $T_A= 25^\circ C$, unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|------------|---|--|------|-------|------|---------|
| V_{CC} | Supply voltage | | 2.7 | | 5.5 | V |
| I_{CC} | Quiescent power supply current | $V_{SDB}= V_{CC}$, all LEDs off | | 2 | 3 | mA |
| I_{SD} | Shutdown current | $V_{SDB}= 0V$ | | 2 | 5 | μA |
| | | $V_{SDB}= V_{CC}$, Configuration Register written "0000 0000" | | 2 | 5 | |
| I_{OUT} | Maximum constant current of CS1~CS16 | $R_{ISET}= 20k\Omega$ | 38 | 42 | 46 | mA |
| I_{LED} | Average current on each LED $I_{LED} = I_{OUT}/12.75$ | $R_{ISET} = 20k\Omega$, GCC= 255, PWM= 255 | 2.98 | 3.29 | 3.61 | mA |
| V_{HR} | Current sink headroom voltage SW1~SW12 | $I_{SINK}= 672mA$ (Note 6,7) | | 300 | 400 | mV |
| | Current source headroom voltage CS1~CS16 | $I_{SOURCE}= 42mA$ (Note 6) | | 150 | 200 | |
| t_{SCAN} | Period of scanning | PFS= "000" (8.4kHz) | 90 | 110 | 130 | μs |
| | | PFS= "010" (26.7kHz) | 30 | 35 | 40 | |
| | | PFS= "011" (2.1kHz) | 360 | 440 | 520 | |
| t_{NOL} | Non-overlap blanking time during scan, the SWy and CSx are all off during this time | PFS= "000" (8.4kHz) | 6.14 | 6.875 | 8.87 | μs |
| | | PFS= "010" (26.7kHz) | 2.08 | 2.43 | 2.77 | |
| | | PFS= "011" (2.1kHz) | 24.5 | 30 | 35.5 | |

Logic Electrical Characteristics (SDA, SCL, ADDR1, ADDR2, SYNC, SDB)

| | | | | | | |
|-----------|-----------------------------------|------------------------------|---------------|-----|-------------|----|
| V_{IL} | Logic "0" input voltage | $V_{IO}= 3.6V$ | GND | | $0.2V_{IO}$ | V |
| V_{IH} | Logic "1" input voltage | $V_{IO}= 3.6V$ | 0.75 V_{IO} | | V_{IO} | V |
| V_{HYS} | Input Schmitt trigger hysteresis | $V_{IO}= 3.6V$ | | 0.2 | | V |
| V_{OL} | Logic "0" output voltage for SYNC | $I_{OL}= 8mA$ | | | 0.4 | V |
| V_{OH} | Logic "1" output voltage for SYNC | $I_{OH}= 8mA$ | 0.75 V_{IO} | | | V |
| I_{IL} | Logic "0" input current | $V_{INPUT}= 0V$ (Note 8) | | 5 | | nA |
| I_{IH} | Logic "1" input current | $V_{INPUT}= V_{IO}$ (Note 8) | | 5 | | nA |

IS31FL3733B

DIGITAL INPUT SWITCHING CHARACTERISTICS (NOTE 8)

| Symbol | Parameter | Fast Mode | | | Fast Mode Plus | | | Units |
|---------------|--|-----------|------|------|----------------|------|------|---------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| f_{SCL} | Serial-clock frequency | - | | 400 | - | | 1000 | kHz |
| t_{BUF} | Bus free time between a STOP and a START condition | 1.3 | | - | 0.5 | | - | μs |
| $t_{HD, STA}$ | Hold time (repeated) START condition | 0.6 | | - | 0.26 | | - | μs |
| $t_{SU, STA}$ | Repeated START condition setup time | 0.6 | | - | 0.26 | | - | μs |
| $t_{SU, STO}$ | STOP condition setup time | 0.6 | | - | 0.26 | | - | μs |
| $t_{HD, DAT}$ | Data hold time | - | | - | - | | - | μs |
| $t_{SU, DAT}$ | Data setup time | 100 | | - | 50 | | - | ns |
| t_{LOW} | SCL clock low period | 1.3 | | - | 0.5 | | - | μs |
| t_{HIGH} | SCL clock high period | 0.7 | | - | 0.26 | | - | μs |
| t_R | Rise time of both SDA and SCL signals, receiving | - | | 300 | - | | 120 | ns |
| t_F | Fall time of both SDA and SCL signals, receiving | - | | 300 | - | | 120 | ns |

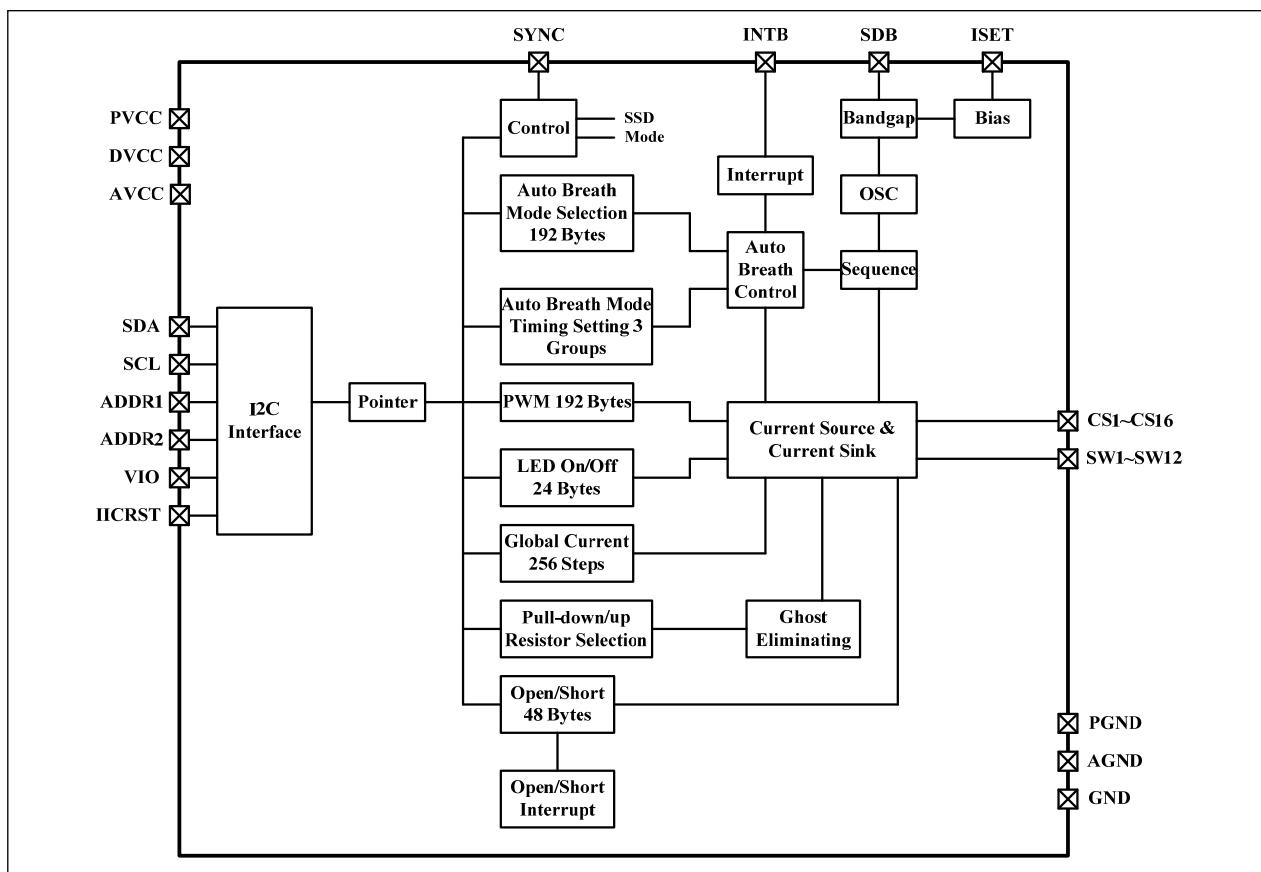
Note 6: In case of $R_{ISET} = 20\text{k}\Omega$, Global Current Control Register (PG3, 01h) written "1111 1111", GCC = "1111 1111".

Note 7: All LEDs are on and PWM = "1111 1111", GCC = "1111 1111".

Note 8: Guaranteed by design.

IS31FL3733B

FUNCTIONAL BLOCK DIAGRAM



IS31FL3733B

DETAILED DESCRIPTION

I2C INTERFACE

The IS31FL3733B uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3733B has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the ADDR1 pin. The value of bits A3 and A4 are decided by the connection of the ADDR2 pin.

The complete slave address is:

Table 1 Slave Address:

| ADDR2 | ADDR1 | A7:A5 | A4:A3 | A2:A1 | A0 |
|-------|-------|-------|-------|-------|-----|
| GND | GND | 101 | 00 | 00 | 0/1 |
| GND | SCL | | 00 | 01 | |
| GND | SDA | | 00 | 10 | |
| GND | VCC | | 00 | 11 | |
| SCL | GND | | 01 | 00 | |
| SCL | SCL | | 01 | 01 | |
| SCL | SDA | | 01 | 10 | |
| SCL | VCC | | 01 | 11 | |
| SDA | GND | | 10 | 00 | |
| SDA | SCL | | 10 | 01 | |
| SDA | SDA | | 10 | 10 | |
| SDA | VCC | | 10 | 11 | |
| VCC | GND | | 11 | 00 | |
| VCC | SCL | | 11 | 01 | |
| VCC | SDA | | 11 | 10 | |
| VCC | VCC | | 11 | 11 | |

ADDR1/2 connected to GND, (A2:A1)/(A4:A3)=00;

ADDR1/2 connected to VCC, (A2:A1)/(A4:A3)=11;

ADDR1/2 connected to SCL, (A2:A1)/(A4:A3)=01;

ADDR1/2 connected to SDA, (A2:A1)/(A4:A3)=10;

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 1kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3733B.

The timing diagram for the I2C is shown in Figure 4. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3733B's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3733B has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3733B, the register address byte is sent, most significant bit first. IS31FL3733B must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3733B must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3733B, load the address of the data register that the first data byte is intended for. During the IS31FL3733B acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3733B will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3733B (Figure 7).

READING OPERATION

Register FEh, F1h, 18h~45h of Page 0 and 11h of Page 3 can be read.

To read the FEh and F1h, after I2C start condition, the bus master must send the IS31FL3733B device address with the R/W bit set to "0", followed by the register address (FEh or F1h) which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3733B device address with the R/W bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3733B to the master (Figure 8).

To read the 18h~45h of Page 0 and 11h of Page 3, the FDh should write with 00h before follow the Figure 8 sequence to read the data, that means, when you want to read 18h~45h of Page 0 and 11h of Page 3 the FDh should point to Page 0 first and you can read the Page 0 data.

IS31FL3733B

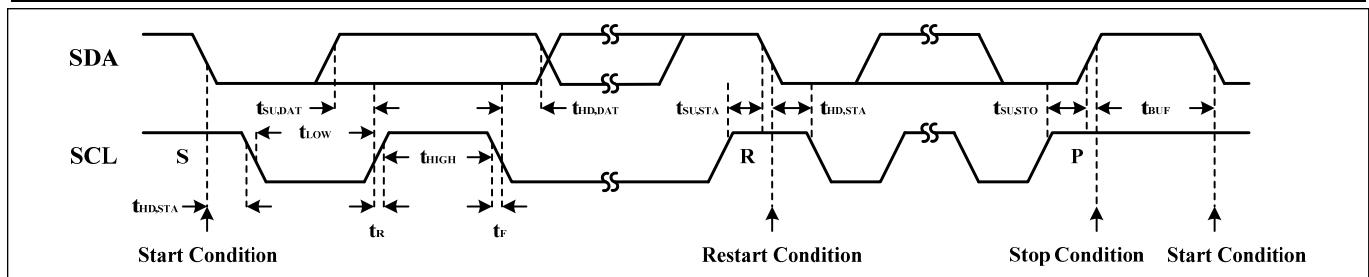


Figure 4 Interface Timing

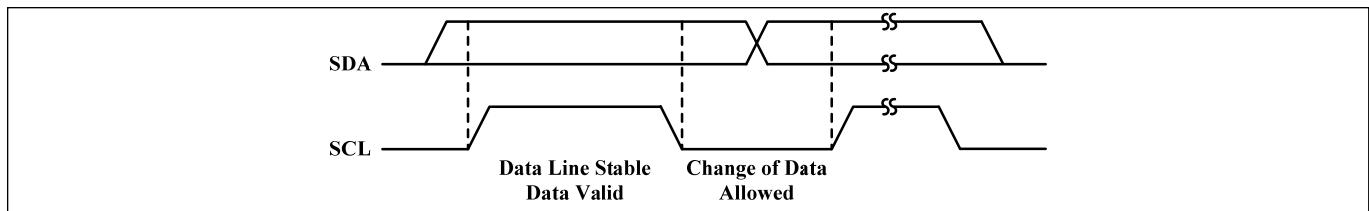


Figure 5 Bit Transfer

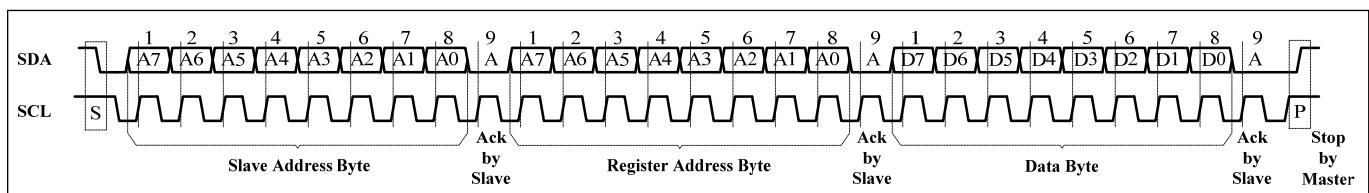


Figure 6 Writing to IS31FL3733B (Typical)

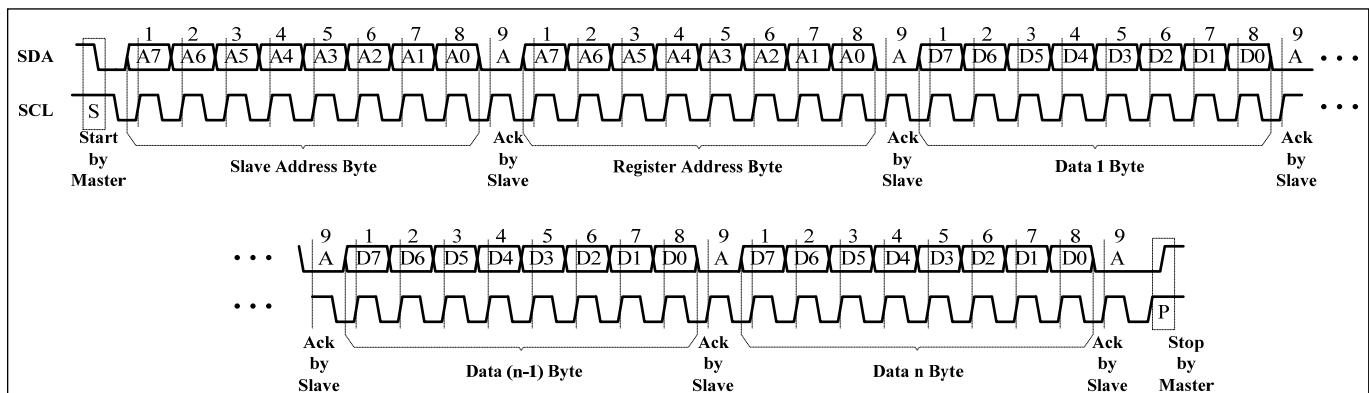


Figure 7 Writing to IS31FL3733B (Automatic Address Increment)

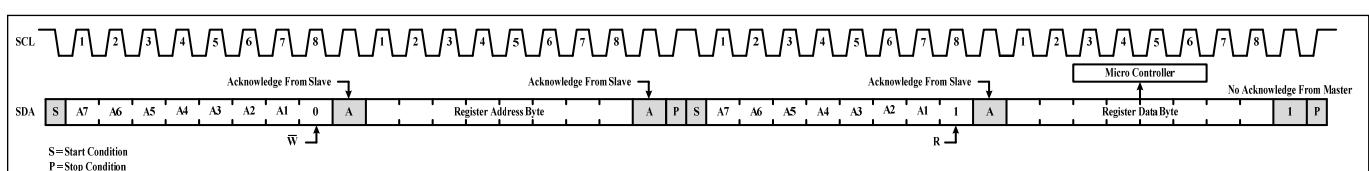


Figure 8 Reading from IS31FL3733B

IS31FL3733B

REGISTER DEFINITION-1

| Address | Name | Function | Table | R/W | Default |
|---------|-----------------------------|--------------------------------------|-------|-----|-----------|
| FDh | Command Register | Available Page 0 to Page 3 Registers | 2 | W | xxxx xxxx |
| FEh | Command Register Write lock | To lock/unlock Command Register | 3 | R/W | 0000 0000 |
| F0h | Interrupt Mask Register | Configure the interrupt function | 4 | W | |
| F1h | Interrupt Status Register | Show the interrupt status | 5 | R | |

REGISTER CONTROL

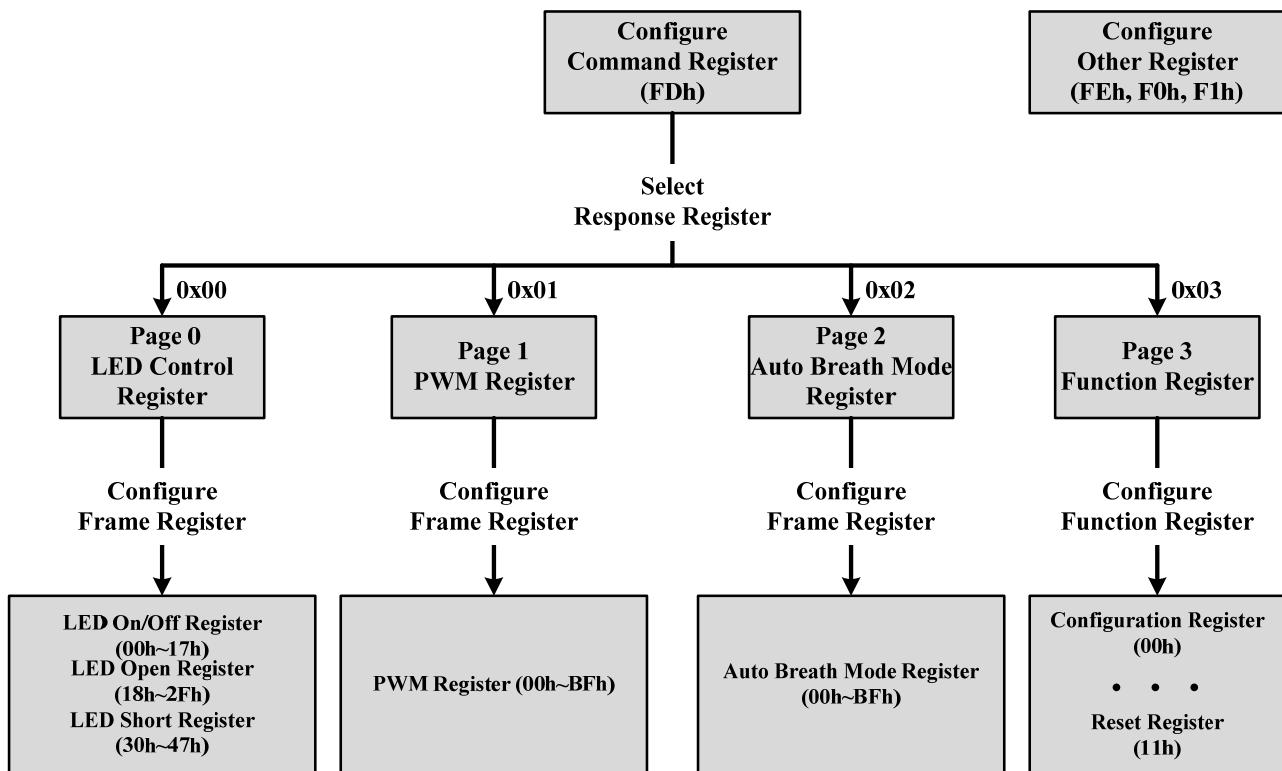


Table 2 FDh Command Register (Write Only)

| Data | Function |
|-----------|---|
| 0000 0000 | Point to Page 0 (PG0, LED Control Register is available) |
| 0000 0001 | Point to Page 1 (PG1, PWM Register is available) |
| 0000 0010 | Point to Page 2 (PG2, Auto Breath Mode Register is available) |
| 0000 0011 | Point to Page 3 (PG3, Function Register is available) |
| Others | Reserved |

Note: FDh is locked when power up, need to unlock this register before write command to it. See Table 3 for detail.

The Command Register should be configured first after writing in the slave address to choose the available register. Then write data in the choosing register. Power up default state is "0000 0000".

For example, when write "0000 0001" in the Command Register (FDh), the data which writing after will be stored in PWM Register (Page1).

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Table 3 FEh Command Register Write Lock (Read/Write)

| | | |
|---------|-------------------------------|--|
| Bit | D7:D0 | |
| Name | CRWL | |
| Default | 0000 0000 (FDh write disable) | |

To select the PG0~PG3, need to unlock this register first, with the purpose to avoid misoperation of this register. When FEh is written with 0xC5, FDh is allowed to modify once, after the FDh is modified the FEh will reset to be 0x00 at once.

CRWL Command Register Write Lock

0x00 FDh write disable

0xC5 FDh write enable once

Table 4 F0h Interrupt Mask Register (Write Only)

| | | | | | |
|---------|-------|-----|-----|----|----|
| Bit | D7:D4 | D3 | D2 | D1 | D0 |
| Name | - | IAC | IAB | IS | IO |
| Default | 0000 | 0 | 0 | 0 | 0 |

Configure the interrupt function for IC.

IAC Auto Clear Interrupt Bit

0 Interrupt could not auto clear

1 Interrupt auto clear when INTB stay low exceeds 8ms

IAB Auto Breath Interrupt Bit

0 Disable auto breath loop finish interrupt

1 Enable auto breath loop finish interrupt

IS Dot Short Interrupt Bit

0 Disable dot short interrupt

1 Enable dot short interrupt

IO Dot Open Interrupt Bit

0 Disable dot open interrupt

1 Enable dot open interrupt

Table 5 F1h Interrupt Status Register (Read Only)

| | | | | | | |
|---------|-------|------|------|------|----|----|
| Bit | D7:D5 | D4 | D3 | D2 | D1 | D0 |
| Name | - | ABM3 | ABM2 | ABM1 | SB | OB |
| Default | 000 | 0 | 0 | 0 | 0 | 0 |

Show the interrupt status for IC.

ABM3 Auto Breath Mode 3 Finish Bit

0 ABM3 not finish

1 ABM3 finish

ABM2 Auto Breath Mode 2 Finish Bit

0 ABM2 not finish

1 ABM2 finish

ABM1 Auto Breath Mode 1 Finish Bit

0 ABM1 not finish

1 ABM1 finish

SB Short Bit

0 No short

1 Short happens

OB Open Bit

0 No open

1 Open happens

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REGISTER DEFINITION-2

| Address | Name | Function | Table | R/W | Default |
|--|---|--|-------|-----|-----------|
| PG0 (0x00): LED Control Register | | | | | |
| 00h ~ 17h | LED On/Off Register | Set on or off state for each LED | 7 | W | 0000 0000 |
| 18h ~ 2Fh | LED Open Register | Store open state for each LED | 8 | R | |
| 30h ~ 47h | LED Short Register | Store short state for each LED | 9 | R | |
| PG1 (0x01): PWM Register | | | | | |
| 00h~BFh | PWM Register | Set PWM duty for LED | 10 | W | 0000 0000 |
| PG2 (0x02): Auto Breath Mode Register | | | | | |
| 00h~BFh | Auto Breath Mode Register | Set operating mode of each dot | 11 | W | 0000 0000 |
| PG3 (0x03): Function Register | | | | | |
| 00h | Configuration Register | Configure the operation mode | 13 | W | 0000 0000 |
| 01h | Global Current Control Register | Set the global current | 14 | W | |
| 02h | Auto Breath Control Register 1 of ABM-1 | Set fade in and hold time for breath function of ABM-1 | 15 | W | |
| 03h | Auto Breath Control Register 2 of ABM-1 | Set the fade out and off time for breath function of ABM-1 | 16 | W | |
| 04h | Auto Breath Control Register 3 of ABM-1 | Set loop characters of ABM-1 | 17 | W | |
| 05h | Auto Breath Control Register 4 of ABM-1 | Set loop characters of ABM-1 | 18 | W | |
| 06h | Auto Breath Control Register 1 of ABM-2 | Set fade in and hold time for breath function of ABM-2 | 15 | W | |
| 07h | Auto Breath Control Register 2 of ABM-2 | Set the fade out and off time for breath function of ABM-2 | 16 | W | |
| 08h | Auto Breath Control Register 3 of ABM-2 | Set loop characters of ABM-2 | 17 | W | |
| 09h | Auto Breath Control Register 4 of ABM-2 | Set loop characters of ABM-2 | 18 | W | |
| 0Ah | Auto Breath Control Register 1 of ABM-3 | Set fade in and hold time for breath function of ABM-3 | 15 | W | |
| 0Bh | Auto Breath Control Register 2 of ABM-3 | Set the fade out and off time for breath function of ABM-3 | 16 | W | |
| 0Ch | Auto Breath Control Register 3 of ABM-3 | Set loop characters of ABM-3 | 17 | W | |
| 0Dh | Auto Breath Control Register 4 of ABM-3 | Set loop characters of ABM-3 | 18 | W | |
| 0Eh | Time Update Register | Update the setting of 02h ~ 0Dh registers | - | W | |
| 0Fh | SWy Pull-Up Resistor Selection Register | Set the pull-up resistor for SWy | 19 | W | |
| 10h | CSx Pull-Down Resistor Selection Register | Set the pull-down resistor for CSx | 20 | W | |
| 11h | Reset Register | Reset all register to POR state | - | R | |

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Table 6 Page 0 (PG0, 0x00): LED Control Register

| LED Location | LED On/Off Register | LED Open Register | LED Short Register |
|-----------------------|------------------------|-------------------|--------------------|
| SW1(CS1~ CS8) | SW1(CS9~ CS16) | 00h | 01h |
| SW2(CS1~ CS8) | SW2(CS9~ CS16) | 02h | 03h |
| SW3(CS1~ CS8) | SW3(CS9~ CS16) | 04h | 05h |
| SW4(CS1~ CS8) | SW4(CS9~ CS16) | 06h | 07h |
| SW5(CS1~ CS8) | SW5(CS9~ CS16) | 08h | 09h |
| SW6(CS1~ CS8) | SW6(CS9~ CS16) | 0Ah | 0Bh |
| SW7(CS1~ CS8) | SW7(CS9~ CS16) | 0Ch | 0Dh |
| SW8(CS1~ CS8) | SW8(CS9~ CS16) | 0Eh | 0Fh |
| SW9(CS1~ CS8) | SW9(CS9~ CS16) | 10h | 11h |
| SW10(CS1~ CS8) | SW10(CS9~ CS16) | 12h | 13h |
| SW11(CS1~ CS8) | SW11(CS9~ CS16) | 14h | 15h |
| SW12(CS1~ CS8) | SW12(CS9~ CS16) | 16h | 17h |
| | | 2Eh | 2Fh |
| | | 46h | 47h |

Table 7 00h ~ 17h LED On/Off Register

| Bit | D7:D0 |
|---------|---|
| Name | C _{CS8} : C _{CS1} or C _{CS16} : C _{CS9} |
| Default | 0000 0000 |

The LED On/Off Registers store the on or off state of each LED in the Matrix.

C_{X-Y} LED State Bit
 0 LED off
 1 LED on

Table 9 30h ~ 47h LED Short Register

| Bit | D7:D0 |
|---------|---|
| Name | ST ₈ : ST ₁ or ST ₁₆ : ST ₉ |
| Default | 0000 0000 |

The LED Short Registers store the short or normal state of each LED in the Matrix.

ST_x LED Short Bit
 0 LED normal
 1 LED short

Table 8 18h ~ 2Fh LED Open Register

| Bit | D7:D0 |
|---------|---|
| Name | OP ₈ : OP ₁ or OP ₁₆ : OP ₉ |
| Default | 0000 0000 |

The LED Open Registers store the open or normal state of each LED in the Matrix.

OP_x LED Open Bit
 0 LED normal
 1 LED open

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Page 1 (PG1, 0x01): PWM Register

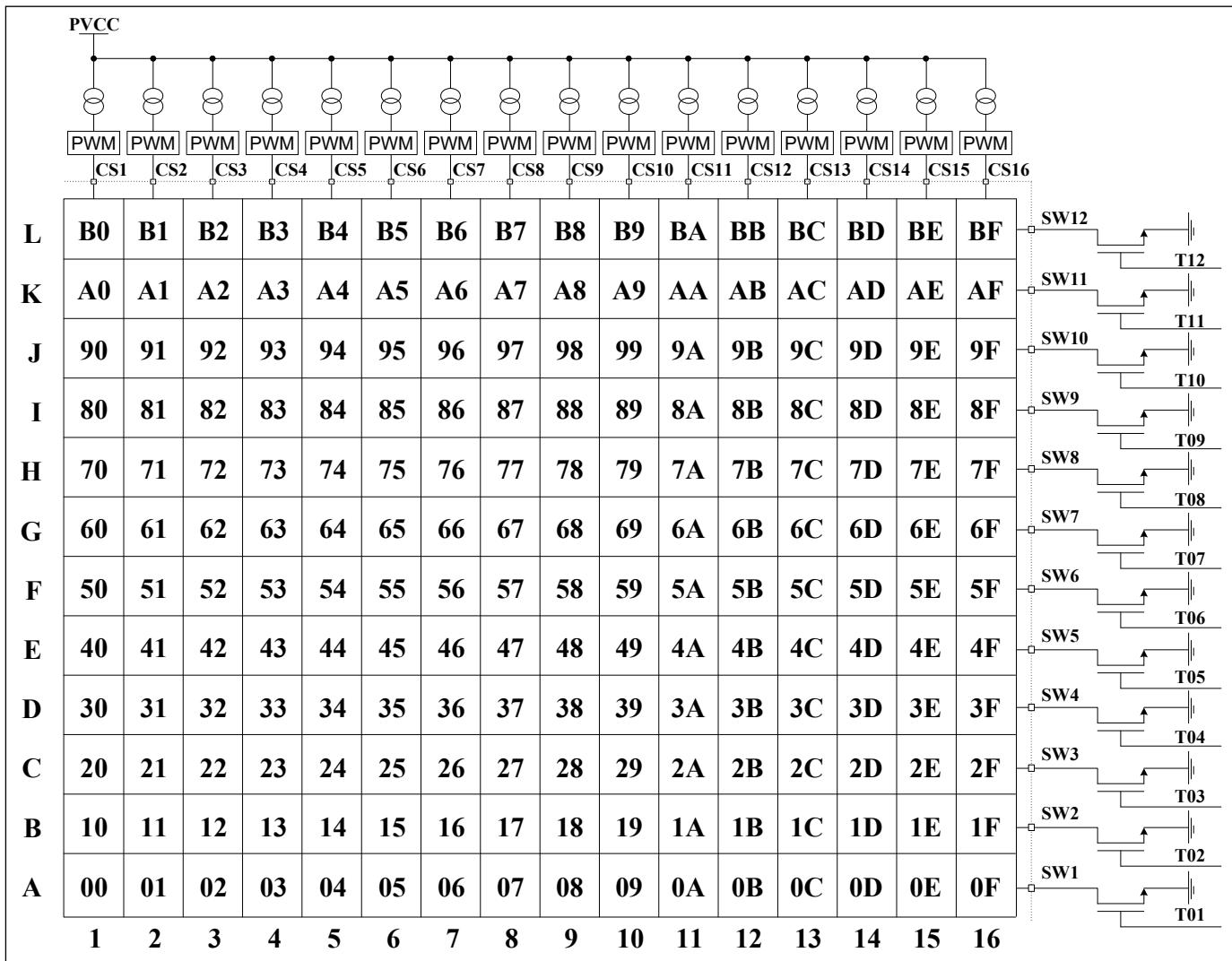


Figure 9 PWM Register

Table 10 00h ~ BFh PWM Register

| Bit | D7:D0 |
|---------|-----------|
| Name | PWM |
| Default | 0000 0000 |

Each dot has a byte to modulate the PWM duty in 256 steps.

The value of the PWM Registers decides the average current of each LED noted I_{LED} .

I_{LED} computed by Formula (1):

$$I_{LED} = \frac{PWM}{256} \times I_{OUT} \times Duty \quad (1)$$

$$PWM = \sum_{n=0}^7 D[n] \cdot 2^n$$

Where Duty is the duty cycle of SWy (PFS= "000"),

$$Duty = \frac{110\mu s}{(110\mu s + 6.875\mu s)} \times \frac{1}{12} = \frac{1}{12.75} \quad (2)$$

I_{OUT} is the output current of CSx ($x=1 \sim 16$),

$$I_{OUT} = \frac{840}{R_{ISET}} \times \frac{GCC}{256} \quad (3)$$

GCC is the Global Current Control register (PG3, 01h) value and R_{ISET} is the external resistor of ISET pin. $D[n]$ stands for the individual bit value, 1 or 0, in location n.

For example: if D7:D0= 10110101 (0xB5, 181), GCC=255, $R_{ISET}=20k\Omega$ ($I_{OUT}=42mA$),

$$I_{LED} = \frac{2^0 + 2^2 + 2^4 + 2^5 + 2^7}{256} \times I_{OUT} \times \frac{1}{12.75} = 2.34mA$$

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Page 2 (PG2, 0x02): Auto Breath Mode Register

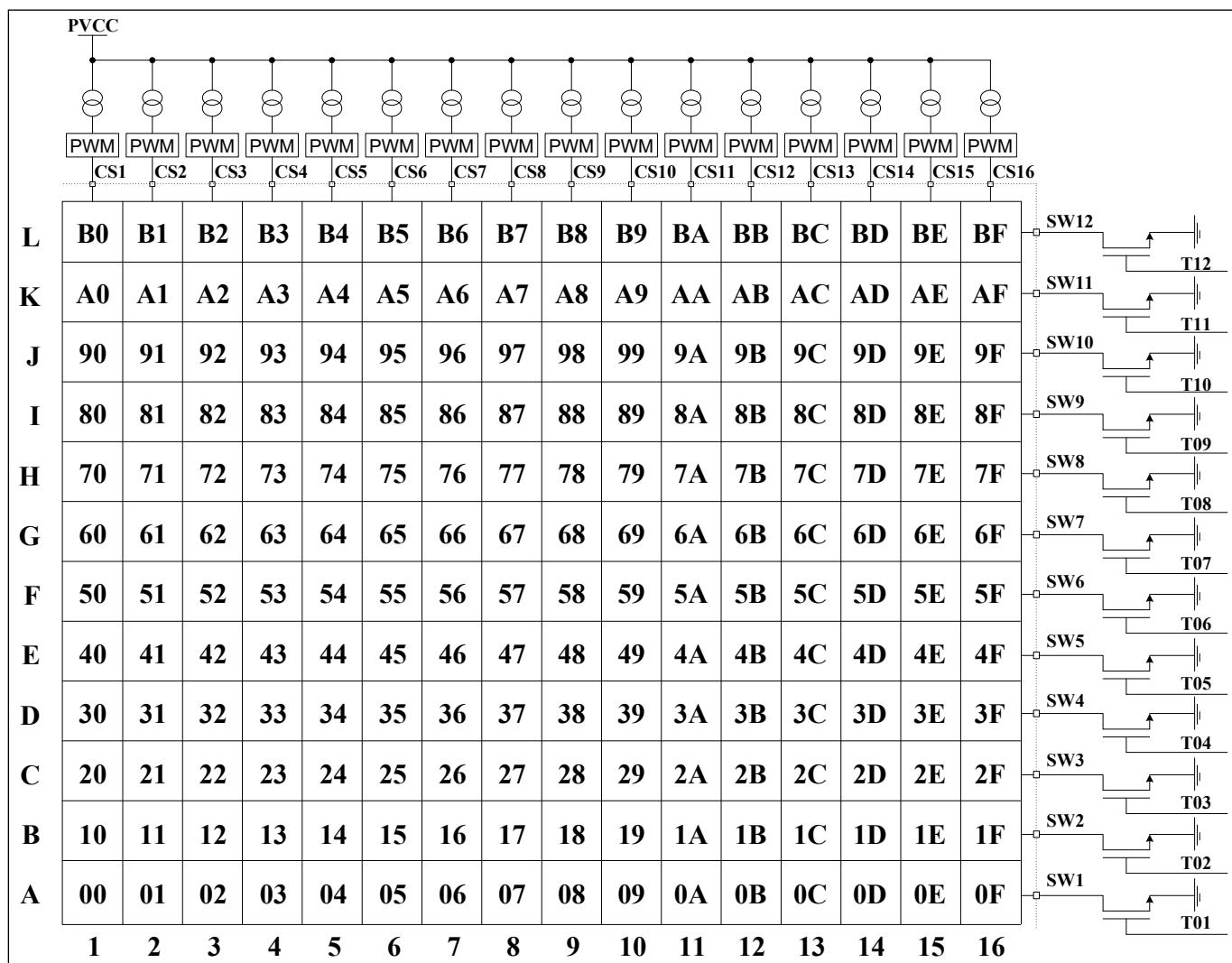


Figure 10 Auto Breath Mode Selection Register

Table 11 00h ~ BFh Auto Breath Mode Register

| Bit | D7:D2 | D1:D0 |
|---------|-------|-------|
| Name | - | ABMS |
| Default | - | 00 |

The Auto Breath Mode Register sets operating mode of each dot.

ABMS Auto Breath Mode Selection Bit

- 00 PWM control mode
- 01 Select Auto Breath Mode 1 (ABM-1)
- 10 Select Auto Breath Mode 2 (ABM-2)
- 11 Select Auto Breath Mode 3 (ABM-3)

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Table 12 Page 3 (PG3, 0x03): Function Register

| Register | Name | Function | R/W | Default |
|----------|---|--|-----|--------------|
| 00h | Configuration Register | Configure the operation mode | W | 0000 0000 |
| 01h | Global Current Control Register | Set the global current | W | |
| 02h | Auto Breath Control Register 1 of ABM-1 | Set fade in and hold time for breath function of ABM-1 | W | |
| 03h | Auto Breath Control Register 2 of ABM-1 | Set the fade out and off time for breath function of ABM-1 | W | |
| 04h | Auto Breath Control Register 3 of ABM-1 | Set loop characters of ABM-1 | W | |
| 05h | Auto Breath Control Register 4 of ABM-1 | Set loop characters of ABM-1 | W | |
| 06h | Auto Breath Control Register 1 of ABM-2 | Set fade in and hold time for breath function of ABM-2 | W | |
| 07h | Auto Breath Control Register 2 of ABM-2 | Set the fade out and off time for breath function of ABM-2 | W | |
| 08h | Auto Breath Control Register 3 of ABM-2 | Set loop characters of ABM-2 | W | |
| 09h | Auto Breath Control Register 4 of ABM-2 | Set loop characters of ABM-2 | W | |
| 0Ah | Auto Breath Control Register 1 of ABM-3 | Set fade in and hold time for breath function of ABM-3 | W | |
| 0Bh | Auto Breath Control Register 2 of ABM-3 | Set the fade out and off time for breath function of ABM-3 | W | |
| 0Ch | Auto Breath Control Register 3 of ABM-3 | Set loop characters of ABM-3 | W | |
| 0Dh | Auto Breath Control Register 4 of ABM-3 | Set loop characters of ABM-3 | W | |
| 0Eh | Time Update Register | Update the setting of 02h ~ 0Dh registers | W | |
| 0Fh | SWy Pull-Up Resistor Selection Register | Set the pull-up resistor for Swy | W | |
| 10h | CSx Pull-Down Resistor Selection Register | Set the pull-down resistor for CSx | W | |
| 11h | Reset Register | Reset all register to POR state | R | |

Table 13 00h Configuration Register

| Bit | D7:D6 | D5:D3 | D2 | D1 | D0 |
|---------|-------|-------|-----|------|-----|
| Name | SYNC | PFS | OSD | B_EN | SSD |
| Default | 00 | 000 | 0 | 0 | 0 |

The Configuration Register sets operating mode of IS31FL3733B.

When SYNC bits are set to "01", the IS31FL3733B is configured as the master clock source and the SYNC pin will generate a clock signal distributed to the clock slave devices. To be configured as a clock slave device and accept an external clock input the slave device's SYNC bits must be set to "10".

The PFS bits selects a fixed PWM operating frequency for all CSx, when PFS set "000", the PWM frequency is 8.4kHz, when PFS set to "010", the PWM frequency is 26.7kHz.

When OSD set high, open/short detection will be trigger once, the user could trigger OS detection again by set OSD from "0" to "1".

When B_EN enable, those dots select working in ABM-x mode will start to run the pre-established timing. If it is disabled, all dots work in PWM mode.

Following Figure 16 to enable the Auto Breath mode

When SSD is "0", IS31FL3733B works in software shutdown mode and to normal operate the SSD bit should set to "1".

IS31FL3733B

| | |
|-------------|---------------------------|
| SYNC | Synchronize Configuration |
| 00/11 | High Impedance |
| 01 | Master |
| 10 | Slave |

| | |
|------------|-----------------------|
| PFS | PWM Frequency Setting |
| 000 | 8.4kHz(default) |
| 010 | 26.7kHz |
| 001 | 4.2kHz |
| 011 | 2.1kHz |
| 100 | 1.05kHz |

| | |
|------------|---------------------------------|
| OSD | Open/Short Detection Enable Bit |
| 0 | Disable open/short detection |
| 1 | Enable open/short detection |

| | |
|-------------|-------------------------|
| B_EN | Auto Breath Enable |
| 0 | PWM Mode Enable |
| 1 | Auto Breath Mode Enable |

| | |
|------------|---------------------------|
| SSD | Software Shutdown Control |
| 0 | Software shutdown |
| 1 | Normal operation |

Table 15 02h, 06h, 0Ah Auto Breath Control Register 1 of ABM-x

| Bit | D7:D5 | D4:D1 | D0 |
|---------|-------|-------|----|
| Name | T1 | T2 | - |
| Default | 000 | 0000 | 0 |

Auto Breath Control Register 1 set the T1&T2 time in Auto Breath Mode.

T1 T1 Setting

| PFS T1 \ | 000(s) | 010(s) | 001(s) | 011(s) | 100(s) |
|-------------|--------|--------|--------|--------|--------|
| 000 | 0.21 | 0.07 | 0.42 | 0.84 | 1.68 |
| 001 | 0.42 | 0.14 | 0.84 | 1.68 | 3.36 |
| 010 | 0.84 | 0.28 | 1.68 | 3.36 | 6.72 |
| 011 | 1.68 | 0.56 | 3.36 | 6.72 | 13.44 |
| 100 | 3.36 | 1.12 | 6.72 | 13.44 | 26.88 |
| 101 | 6.72 | 2.24 | 13.44 | 26.88 | 53.76 |
| 110 | 13.44 | 4.48 | 26.88 | 53.76 | 107.52 |
| 111 | 26.88 | 8.96 | 53.76 | 107.52 | 215.04 |

Table 14 01h Global Current Control Register

| Bit | D7:D0 |
|---------|-----------|
| Name | GCCx |
| Default | 0000 0000 |

The Global Current Control Register modulates all CSx (x=1~16) DC current which is noted as Iout in 256 steps.

Iout is computed by the Formula (3):

$$I_{OUT} = \frac{840}{R_{ISET}} \times \frac{GCC}{256} \quad (3)$$

$$GCC = \sum_{n=0}^7 D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n, R_{ISET} is the external resistor of ISET pin.

For example: if D7:D0 = 1011 0101,

$$I_{OUT} = \frac{2^0 + 2^2 + 2^4 + 2^5 + 2^7}{256} \times \frac{840}{R_{ISET}}$$

T2 T2 Setting

| PFS T2 \ | 000(s) | 010(s) | 001(s) | 011(s) | 100(s) |
|-------------|-------------|--------|--------|--------|--------|
| 000 | 0 | 0 | 0 | 0 | 0 |
| 001 | 0.21 | 0.07 | 0.42 | 0.84 | 1.68 |
| 010 | 0.42 | 0.14 | 0.84 | 1.68 | 3.36 |
| 011 | 0.84 | 0.28 | 1.68 | 3.36 | 6.72 |
| 100 | 1.68 | 0.56 | 3.36 | 6.72 | 13.44 |
| 101 | 3.36 | 1.12 | 6.72 | 13.44 | 26.88 |
| 110 | 6.72 | 2.24 | 13.44 | 26.88 | 53.76 |
| 111 | 13.44 | 4.48 | 26.88 | 53.76 | 107.52 |
| 1000 | 26.88 | 8.96 | 53.76 | 107.52 | 215.04 |
| Others | Unavailable | | | | |

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Table 16 03h, 07h, 0Bh Auto Breath Control Register 2 of ABM-x

| Bit | D7:D5 | D4:D1 | D0 |
|---------|-------|-------|----|
| Name | T3 | T4 | - |
| Default | 000 | 0000 | 0 |

Auto Breath Control Register 2 set the T3&T4 time in Auto Breath Mode.

T3 T3 Setting

| PFS \ T3 | 000(s) | 010(s) | 001(s) | 011(s) | 100(s) |
|----------|--------|--------|--------|--------|--------|
| 000 | 0.21 | 0.07 | 0.42 | 0.84 | 1.68 |
| 001 | 0.42 | 0.14 | 0.84 | 1.68 | 3.36 |
| 010 | 0.84 | 0.28 | 1.68 | 3.36 | 6.72 |
| 011 | 1.68 | 0.56 | 3.36 | 6.72 | 13.44 |
| 100 | 3.36 | 1.12 | 6.72 | 13.44 | 26.88 |
| 101 | 6.72 | 2.24 | 13.44 | 26.88 | 53.76 |
| 110 | 13.44 | 4.48 | 26.88 | 53.76 | 107.52 |
| 111 | 26.88 | 8.96 | 53.76 | 107.52 | 215.04 |

T4 T4 Setting

| PFS \ T4 | 000(s) | 010(s) | 001(s) | 011(s) | 100(s) |
|----------|-------------|--------|--------|--------|--------|
| 0000 | 0 | 0 | 0 | 0 | 0 |
| 0001 | 0.21 | 0.07 | 0.42 | 0.84 | 1.68 |
| 0010 | 0.42 | 0.14 | 0.84 | 1.68 | 3.36 |
| 0011 | 0.84 | 0.28 | 1.68 | 3.36 | 6.72 |
| 0100 | 1.68 | 0.56 | 3.36 | 6.72 | 13.44 |
| 0101 | 3.36 | 1.12 | 6.72 | 13.44 | 26.88 |
| 0110 | 6.72 | 2.24 | 13.44 | 26.88 | 53.76 |
| 0111 | 13.44 | 4.48 | 26.88 | 53.76 | 107.52 |
| 1000 | 26.88 | 8.96 | 53.76 | 107.52 | 215.04 |
| 1001 | 53.76 | 17.92 | 107.52 | 215.04 | 430.08 |
| 1010 | 107.52 | 35.84 | 215.04 | 430.08 | 860.16 |
| Others | Unavailable | | | | |

Note: Do not set T4= "0000" in Auto Breath Mode when the PWM frequency is 26.7kHz (PFS= "010").

Table 17 04h, 08h, 0Ch Auto Breath Control Register 3 of ABM-x

| Bit | D7:D6 | D5:D4 | D3:D0 |
|---------|-------|-------|-------|
| Name | LE | LB | LTA |
| Default | 00 | 00 | 0000 |

Total loop times= LTA ×256 + LTB.

For example, if LTA=2, LTB=100, the total loop times is 256×2+100= 612 times.

For the counting of breathing times, do follow Figure 16 to enable the Auto Breath Mode.

If the loop starts from T4,

T4->T1->T2->T3(1)->T4->T1->T2->T3(2)->T4->T1->... and so on.

If the loop not start from T4,

Tx->T3(1) ->T4->T1->T2->T3(2)->T4-> T1->... and so on.

If the loop ends at off state (End of T3), the LED will be off state at last. If the loop ends at on state (End of T1), the LED will run an extra T4&T1, which are not included in loop.

LB Loop Beginning Time

00 Loop begin from T1

01 Loop begin from T2

10 Loop begin from T3

11 Loop begin from T4

LE Loop End Time

00 Loop end at off state (End of T3)

01 Loop end at on state (End of T1)

LTA 8-11 Bits Of Loop Times

0000 Endless loop

0001 1

0010 2

...

1111 15

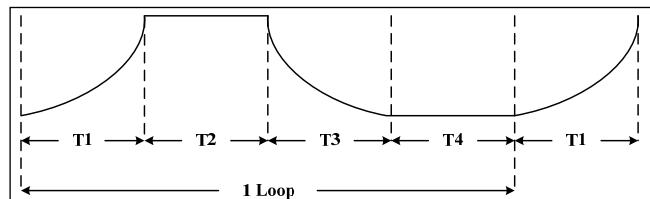


Figure 11 Auto Breathing Function

Table 18 05h, 09h, 0Dh Auto Breath Control Register 4 of ABM-x

| Bit | D7:D0 |
|---------|-----------|
| Name | LTB |
| Default | 0000 0000 |

Total loop times= LTA ×256 + LTB.

For example, if LTA=2, LTB=100, the total loop times is 256×2+100= 612 times.

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| | |
|------------|------------------------|
| LTB | 0-7 Bits Of Loop Times |
| 0000 0000 | Endless loop |
| 0000 0001 | 1 |
| 0000 0010 | 2 |
| ... | ... |
| 1111 1111 | 255 |

0Eh Time Update Register (02h~0Dh)

The data sent to the time registers (02h~0Dh) will be stored in temporary registers. A write operation of “0000 0000” data to the Time Update Register is required to update the registers (02h~0Dh). Please follow Figure 16 to enable the Auto Breath mode and update the time parameters.

Table 19 0Fh SWy Pull-Up Resistor Selection Register

| Bit | D7:D3 | D2:D0 |
|---------|-------|-------|
| Name | - | PUR |
| Default | 00000 | 000 |

Set pull-up resistor for SWy.

PUR SWy Pull-up Resistor Selection Bit

| | |
|-----|-----------------------------------|
| 000 | No pull-up resistor |
| 001 | 0.5kΩ pull-up in t _{NOL} |
| 010 | 0.5kΩ pull-up in t _{NOL} |
| 011 | 3.0kΩ pull-up all the time |
| 100 | 4.0kΩ pull-up all the time |
| 101 | 8.0kΩ pull-up all the time |
| 110 | 16kΩ pull-up all the time |
| 111 | 32kΩ pull-up in t _{NOL} |

Table 20 10h CSx Pull-Down Resistor Selection Register

| Bit | D7:D3 | D2:D0 |
|---------|-------|-------|
| Name | - | PDR |
| Default | 00000 | 000 |

Set the pull-down resistor for CSx.

PDR CSx Pull-down Resistor Selection Bit

| | |
|-----|-------------------------------------|
| 000 | No pull-down resistor |
| 001 | 0.5kΩ pull-down in t _{NOL} |
| 010 | 0.5kΩ pull-down in t _{NOL} |
| 011 | 3.0kΩ pull-down all the time |
| 100 | 68kΩ pull-down all the time |
| 101 | 8.0kΩ pull-down all the time |
| 110 | 16kΩ pull-down all the time |
| 111 | 32kΩ pull-down in t _{NOL} |

11h Reset Register

Once user read the Reset Register, IS31FL3733B will reset all the IS31FL3733B registers to their default value. On initial power-up, the IS31FL3733B registers are reset to their default values for a blank display.

IS31FL3733B

APPLICATION INFORMATION

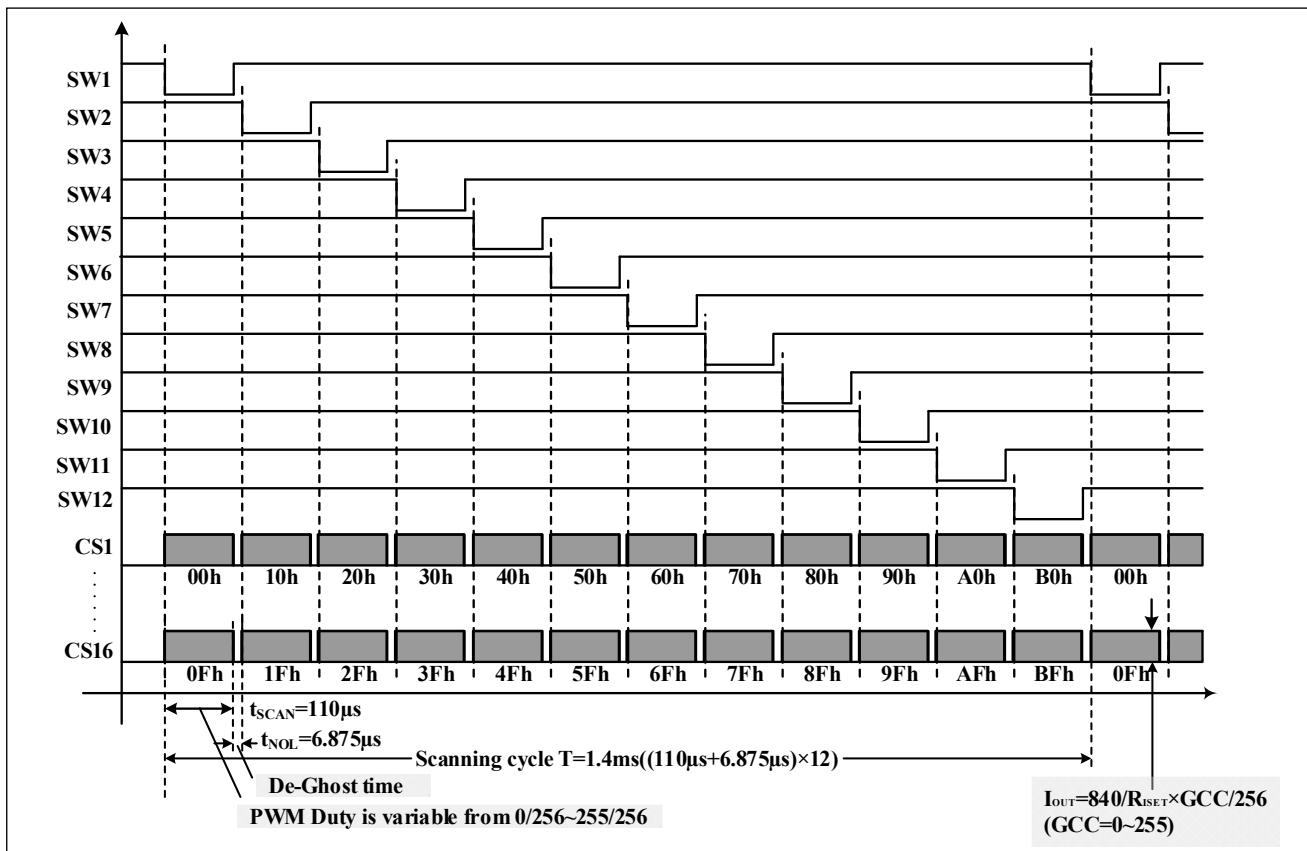


Figure 12 Scanning Timing (PFS="000")

SCANING TIMING

As shown in Figure 12, the SW1~SW12 is turned on by serial, LED is driven 16 by 16 within the SWy ($x=1\sim 12$) on time (SWy, $y=1\sim 12$) is sink and pull low when LED on), including the non-overlap blanking time during scan, the duty cycle of SWy (active low, $y=1\sim 12$) is (PFS= "000"):

$$Duty = \frac{110\mu s}{(110\mu s + 6.875\mu s)} \times \frac{1}{12} = \frac{1}{12.75} \quad (2)$$

Where $110\mu s$ is t_{SCAN} , the period of scanning and $8\mu s$ is t_{NOL} , the non-overlap time.

When PFS= "010" or others, the duty result is same.

EXTERNAL RESISTOR (R_{SET})

The output current for each CSx can be set by a single external resistor, R_{SET} , as described in Formula (3).

$$I_{OUT} = \frac{840}{R_{SET}} \times \frac{GCC}{256} \quad (3)$$

GCC is Global Current Control Register (PG3, 01h) data showing in Table 14.

PWM CONTROL

After setting the I_{OUT} and GCC, the brightness of each LEDs (LED average current (I_{LED})) can be modulated with 256 steps by PWM Register, as described in Formula (1).

$$I_{LED} = \frac{PWM}{256} \times I_{OUT} \times Duty \quad (1)$$

Where PWM is PWM Registers (PG1, 00h~BFh) data showing in Table 10.

For example, in Figure 1, $R_{SET}=20k\Omega$, if PWM=255, and GCC=255, then

$$I_{LED} = \frac{255}{256} \times \frac{840}{20k\Omega} \times \frac{255}{256} \times \frac{1}{12.75} = 3.27mA$$

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

LED AVERAGE CURRENT (I_{LED})

As described in Formula (1), the LED average current (I_{LED}) is effected by 3 factors:

1. R_{SET} , resistor which is connected ISET pin and GND. R_{SET} sets the current of all CSx ($x=1\sim 16$) based on Formula (3).

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2. Global Current Control Register (PG3, 01h). This register adjusts all CSx ($x=1\sim16$) output currents by 256 steps as shown in Formula (3).

3. PWM Registers (PG1, 00h~BFh), every LED has an own PWM register. PWM Registers adjust individual LED average current by 256 steps as shown in Formula (1).

GAMMA CORRECTION

In order to perform a better visual LED breathing effect we recommend using a gamma corrected PWM value to set the LED intensity. This results in a reduced number of steps for the LED intensity setting, but causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS31FL3733B can modulate the brightness of the LEDs with 256 steps, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the changes in brightness matches the human eye's brightness curve.

Table 21 32 Gamma Steps with 256 PWM Steps

| C(0) | C(1) | C(2) | C(3) | C(4) | C(5) | C(6) | C(7) |
|-------|-------|-------|-------|-------|-------|-------|-------|
| 0 | 1 | 2 | 4 | 6 | 10 | 13 | 18 |
| C(8) | C(9) | C(10) | C(11) | C(12) | C(13) | C(14) | C(15) |
| 22 | 28 | 33 | 39 | 46 | 53 | 61 | 69 |
| C(16) | C(17) | C(18) | C(19) | C(20) | C(21) | C(22) | C(23) |
| 78 | 86 | 96 | 106 | 116 | 126 | 138 | 149 |
| C(24) | C(25) | C(26) | C(27) | C(28) | C(29) | C(30) | C(31) |
| 161 | 173 | 186 | 199 | 212 | 226 | 10 | 255 |

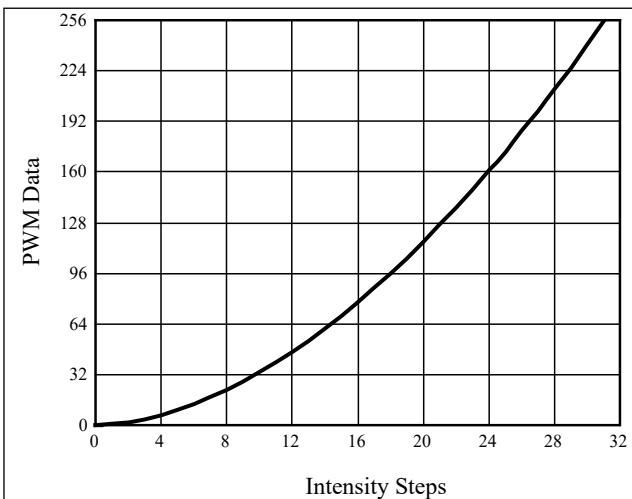


Figure 13 Gamma Correction (32 Steps)

Choosing more gamma steps provides for a more continuous looking breathing effect. This is useful for very long breathing cycles. The recommended configuration is defined by the breath cycle T. When T=1s, choose 32 gamma steps, when T=2s, choose

64 gamma steps. The user must decide the final number of gamma steps not only by the LED itself, but also based on the visual performance of the finished product.

Table 22 64 Gamma Steps with 256 PWM Steps

| C(0) | C(1) | C(2) | C(3) | C(4) | C(5) | C(6) | C(7) |
|-------|-------|-------|-------|-------|-------|-------|-------|
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| C(8) | C(9) | C(10) | C(11) | C(12) | C(13) | C(14) | C(15) |
| 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 |
| C(16) | C(17) | C(18) | C(19) | C(20) | C(21) | C(22) | C(23) |
| 24 | 26 | 29 | 32 | 35 | 38 | 41 | 44 |
| C(24) | C(25) | C(26) | C(27) | C(28) | C(29) | C(30) | C(31) |
| 47 | 50 | 53 | 57 | 61 | 65 | 69 | 73 |
| C(32) | C(33) | C(34) | C(35) | C(36) | C(37) | C(38) | C(39) |
| 77 | 81 | 85 | 89 | 94 | 99 | 104 | 109 |
| C(40) | C(41) | C(42) | C(43) | C(44) | C(45) | C(46) | C(47) |
| 114 | 119 | 124 | 129 | 134 | 140 | 146 | 152 |
| C(48) | C(49) | C(50) | C(51) | C(52) | C(53) | C(54) | C(55) |
| 158 | 164 | 170 | 176 | 182 | 188 | 195 | 202 |
| C(56) | C(57) | C(58) | C(59) | C(60) | C(61) | C(62) | C(63) |
| 209 | 216 | 223 | 230 | 237 | 244 | 251 | 255 |

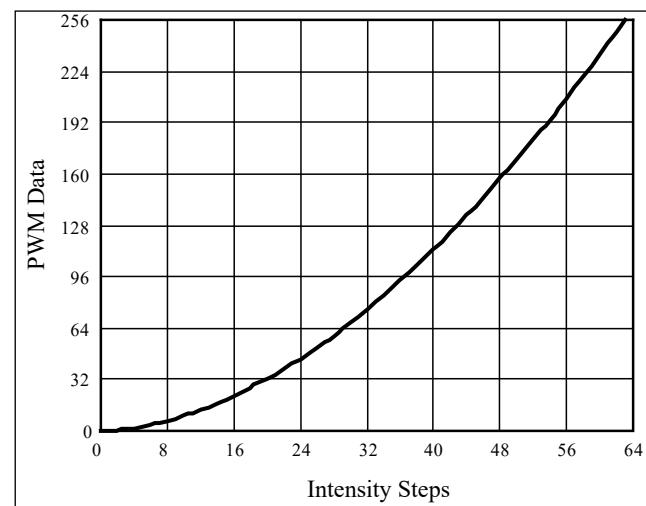


Figure 14 Gamma Correction (64 Steps)

Note: The data of 32 gamma steps is the standard value and the data of 64 gamma steps is the recommended value.

OPERATING MODE

Each dot of IS31FL3733B has two selectable operating modes, PWM Mode and Auto Breath Mode.

PWM Mode

By setting the Auto Breath Mode Register bits of the Page 2 (PG2, 00h~BFh) to "00", or disable the B_EN bit of Configure Register (PG3, 00h), the IS31FL3733B operates in PWM Mode. The brightness of each LED can be modulated with 256 steps by PWM registers. For example, if the data in PWM Register is "0000 0100", then the PWM is the fourth step.

IS31FL3733B

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

Auto Breath Mode

By setting the B_EN bit of the Configuration Register (PG3, 00h) to "1", breath function enables. When set the B_EN bit to "0", breath function disables.

By setting the Auto Breath Mode Register bits of the Page 2 (PG2, 00h~BFh) to "01" (ABM-1), "10" (ABM-2) or "11" (ABM-3), the IS31FL3733B operates in Auto Breath Mode.

IS31FL3733B has three auto breath modes, Auto Breath Mode 1, Auto Breath Mode 2 and Auto Breath Mode 3. Each ABM has T1, T2, T3 and T4, as shown below:

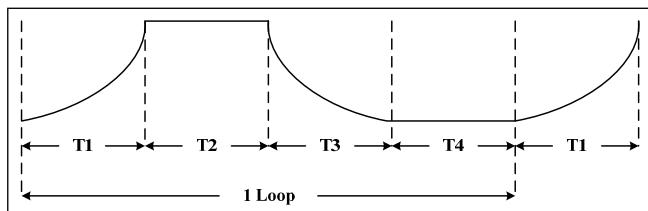


Figure 15 Auto Breathing Function

T1/T3 is variable from 0.21s to 26.88s, T2/T4 is variable from 0s to 26.88s, for each loop, the start point can be T1~T4 and the stop point can be on state (T2) and off state (T4), also the loop time can be set to 1~ 2^{12} times or endless. Each LED can select ABM-1~ABM-3 to work.

The setting of ABM-1~ABM-3 (PG2, 02h~0Dh) need to write the 0Eh in PG3 to update before effective.

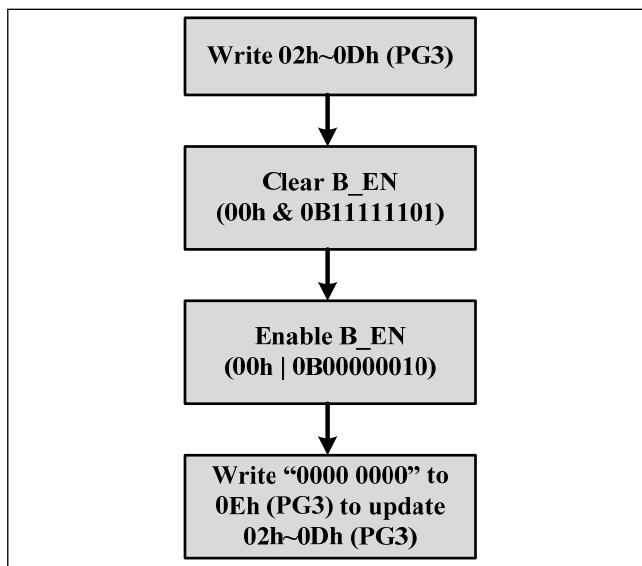


Figure 16 Enable Auto Breath Mode

If not follow this flow, first loop's start point may be wrong.

OPEN/SHORT DETECT FUNCTION

IS31FL3733B has open and short detect bit for each LED.

By setting the OSD bit of the Configuration Register (PG3, 00h) from "0" to "1", the LED Open Register and LED Short Register will start to store the open/short information and after at least 2 scanning cycle (3.264ms) the MCU can get the open/short information by reading the 18h~2fh/30h~47h, for those dots are turned off via LED On/Off Registers (PG0, 00h~17h), the open/short data will not get refreshed when setting the OSD bit of the Configuration Register (PG3, 00h) from "0" to "1".

The Global Current Control Register (PG3, 01h) need to set to 0x01 in order to get the right open/short data.

The detect action is one-off event and each time before reading out the open/short information, the OSD bit of the Configuration Register (PG3, 00h) need to be set from "0" to "1" (clear before set operation).

INTERRUPT CONTROL

IS31FL3733B has an INTB pin, by setting the Interrupt Mask Register (F0h), it can be the flag of LED open, LED short or the finish flag of ABM-1, ABM-2, and ABM-3.

For example, if the IO bit of the Interrupt Mask Register (F0h) set to "1", when LED open happens, the INTB will pull be pulled low and the OB bit of Interrupt Status Register (F1h) will store open status at the same time.

The INTB pin will be pulled high after reading the Interrupt Status Register (F1h) operation or it will be pulled high automatically after it stays low for 8ms (Typ.) if the IAC bit of Interrupt Mask Register (F0h) is set to "1". The bits of Interrupt Status Register (F1h) will be reset to "0" after INTB pin pulled high.

SYNCHRONIZE FUNCTION

SYNC bits of the Configuration Register (PG3, 00h) sets SYNC pin input or output synchronize clock signal. It is used for more than one part working synchronize. When SYNC bits are set to "01", SYNC pin output synchronize clock to synchronize other parts as master. When SYNC bits are set to "10", SYNC pin input synchronize clock and work synchronization with this input signal as slave. When SYNC bits are set to "00/11", SYNC pin is high impedance, and synchronize function is disabled. SYNC bit default state is "00" and SYNC pin is high impedance when power up.

DE-GHOST FUNCTION

The "ghost" term is used to describe the behavior of an LED that should be OFF but instead glows dimly when another LED is turned ON. A ghosting effect typically can occur when multiplexing LEDs. In matrix

IS31FL3733B

architecture any parasitic capacitance found in the constant-current outputs or the PCB traces to the LEDs may provide sufficient current to dimly light an LED to create a ghosting effect.

To prevent this LED ghost effect, the IS31FL3733B has integrated pull-up resistors for each SWy ($y=1\sim12$) and pull-down resistors for each CSx ($x=1\sim16$). Select the right SWy pull-up resistor (PG3, 0Fh) and CSx pull-down resistor (PG3, 10h) which eliminates the ghost LED for a particular matrix layout configuration.

Typically, selecting the $32k\Omega$ will be sufficient to eliminate the LED ghost phenomenon.

The SWy pull-up resistors and CSx pull-down resistors are active only when the CSx/SW y outputs are in the OFF state and therefore no power is lost through these resistors

I2C RESET

The I2C will be reset if the IICRST pin is pull-high, when normal operating the I2C bus, the IICRST pin need to keep low.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Configuration Register (PG3, 00h) to "0", the IS31FL3733B will operate in software shutdown mode. When the IS31FL3733B is in software shutdown, all current sources are switched off, so that the matrix is blanked. All registers can be operated. Typical current consume is $3\mu A$.

Hardware Shutdown

The chip enters hardware shutdown when the SDB pin is pulled low. All analog circuits are disabled during hardware shutdown, typical the current consume is $3\mu A$.

The chip releases hardware shutdown when the SDB pin is pulled high. During hardware shutdown state Function Register can be operated.

If V_{CC} has risk drop below 1.75V but above 0.1V during SDB pulled low, please re-initialize all Function Registers before SDB pulled high.

POWER DISSIPATION

The power dissipation of the IS31FL3733B can calculate as below:

$$P_{3733B} = I_{PVCC} \times PV_{CC} + I_Q \times DV_{CC}(AV_{CC}) - I_{PVCC} \times V_{F(AVR)} \quad (4)$$

$$\approx I_{PVCC} \times PV_{CC} - I_{PVCC} \times V_{F(AVR)}$$

$$\approx I_{PVCC} \times (PV_{CC} - V_{F(AVR)})$$

Where I_{PVCC} is the current of PVCC and $V_{F(AVR)}$ is the average forward of all the LED.

For example, if $R_{ISET}=20k\Omega$, $GCC=255$, $PWM=255$, $PV_{CC}=5V$, $V_{F(AVR)}=3.5V@42mA$,

then the $I_{PVCC}=42mA \times 16 \times 12 / 12.75 = 632.5mA$.

$$P_{3733B}=632.5mA \times (5V-3.5V)=0.948.75W$$

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Equation (5):

$$P_{D(MAX)} = \frac{125^\circ C - 25^\circ C}{\theta_{JA}} \quad (5)$$

$$\text{So, } P_{D(MAX)} = \frac{125^\circ C - 25^\circ C}{39^\circ C/W} \approx 2.56W(eTQFP)$$

$$\text{And, } P_{D(MAX)} = \frac{125^\circ C - 25^\circ C}{37.5^\circ C/W} \approx 2.67W(QFN)$$

Figure 17 and 18, shows the power derating of the IS31FL3733B on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

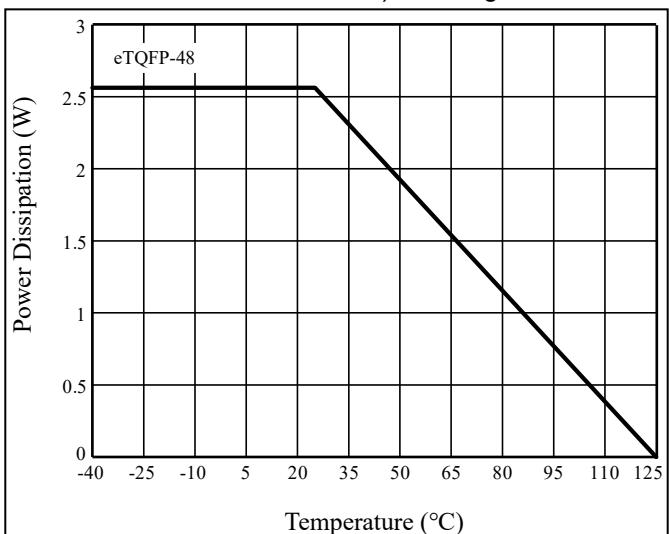


Figure 17 Dissipation Curve

IS31FL3733B

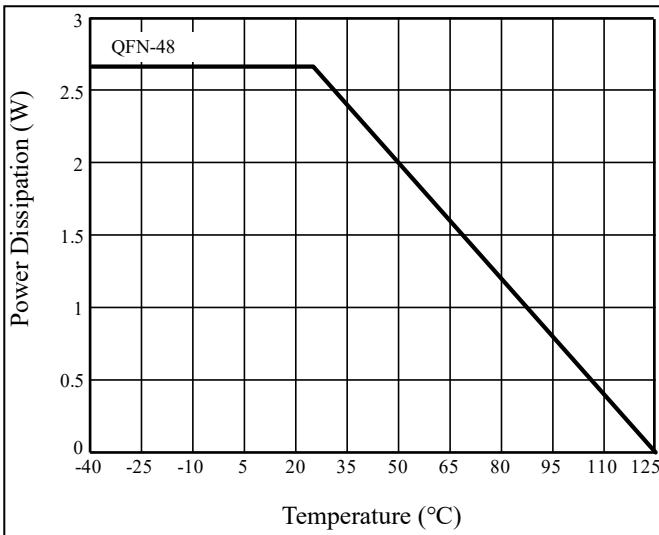


Figure 18 Dissipation Curve

LAYOUT

As described in external resistor (R_{ISET}), the chip consumes lots of power. Please consider below factors when layout the PCB.

1. The V_{CC} (PVCC, DVCC, AVCC, VIO) capacitors need to close to the chip and the ground side should well connected to the GND of the chip.
2. R_{ISET} should be close to the chip and the ground side should well connect to the GND of the chip.
3. The thermal pad should connect to ground pins and the PCB should have the thermal pad too, usually this pad should have 16 or 25 via thru the PCB to other side's ground area to help radiate the heat. About the thermal pad size, please refer to the land pattern of each package.
4. The CSx pins maximum current is 42mA ($R_{ISET}=20\text{k}\Omega$), and the SWy pins maximum current is 672mA ($R_{ISET}=20\text{k}\Omega$), the width of the trace, SWy should have wider trace then CSx.
5. In the middle of SDA and SCL trace, a ground line is recommended to avoid the effect between these two lines.

PWM FREQUENCY SELECT

The IS31FL3733B output channels operate with a default PWM frequency of 8.4kHz. Because all the CSx channels are synchronized, the DC supply will experience large instantaneous current surges when the CSx channels turn ON. These current surges will generate an AC ripple on the power supply which cause stress to the decoupling capacitors.

When the AC ripple is applied to a monolithic ceramic capacitor chip (MLCC) it will expand and contract causing the PCB to flex and generate audible hum in the range of between 20Hz to 20kHz, to avoid this hum, there are many countermeasures, such as selecting the capacitor type and value which will not cause the PCB to flex and contract.

An additional option for avoiding audible hum is to set the IS31FL3733B's output PWM frequency above the audible range. The Output Frequency Setting Register (00h)'s bit D4 can be used to set the switching frequency to 26.7kHz, which is beyond the audible range. Figure 19 below shows the variation of output PWM frequency across supply voltage and temperature.

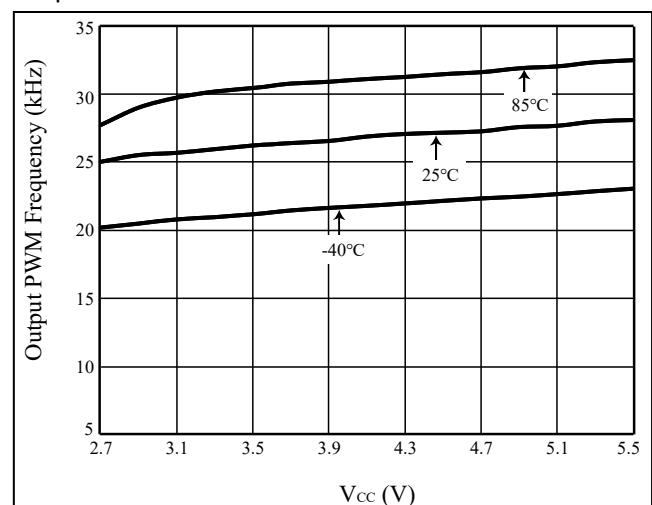


Figure 19 V_{CC} vs. CSx PWM Frequency

IS31FL3733B

CLASSIFICATION REFLOW PROFILES

| Profile Feature | Pb-Free Assembly |
|---|----------------------------------|
| Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts) | 150°C 200°C 60-120 seconds |
| Average ramp-up rate (Tsmax to Tp) | 3°C/second max. |
| Liquidous temperature (TL) Time at liquidous (tL) | 217°C 60-150 seconds |
| Peak package body temperature (Tp)* | Max 260°C |
| Time (tp)** within 5°C of the specified classification temperature (Tc) | Max 30 seconds |
| Average ramp-down rate (Tp to Tsmax) | 6°C/second max. |
| Time 25°C to peak temperature | 8 minutes max. |

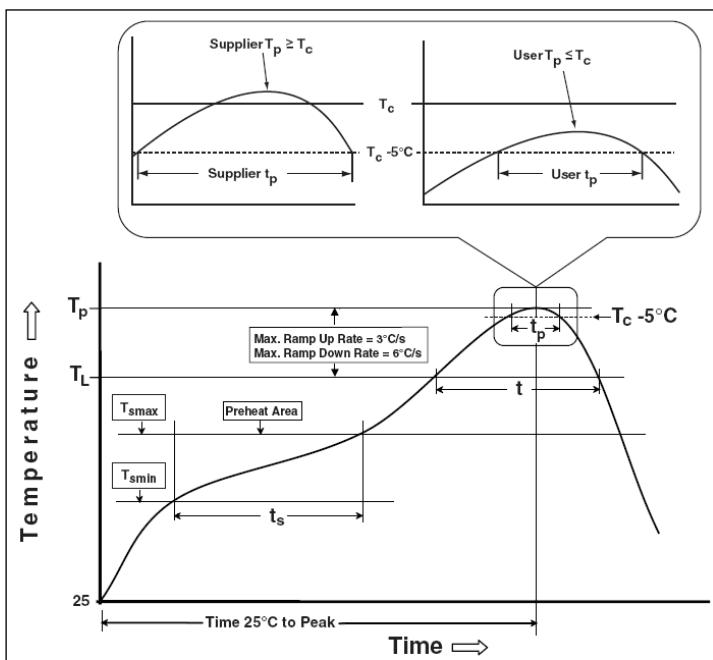
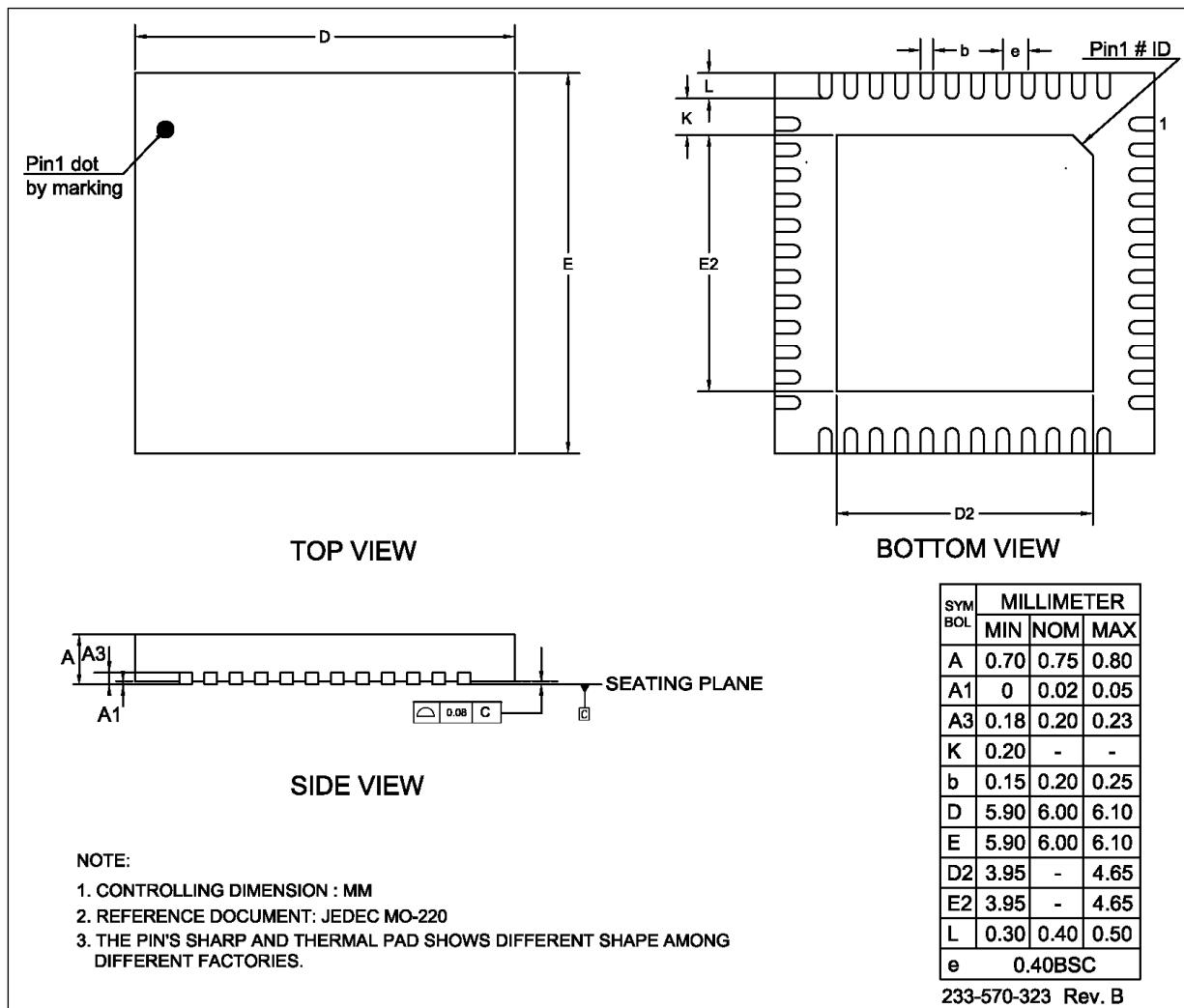


Figure 20 Classification Profile

IS31FL3733B

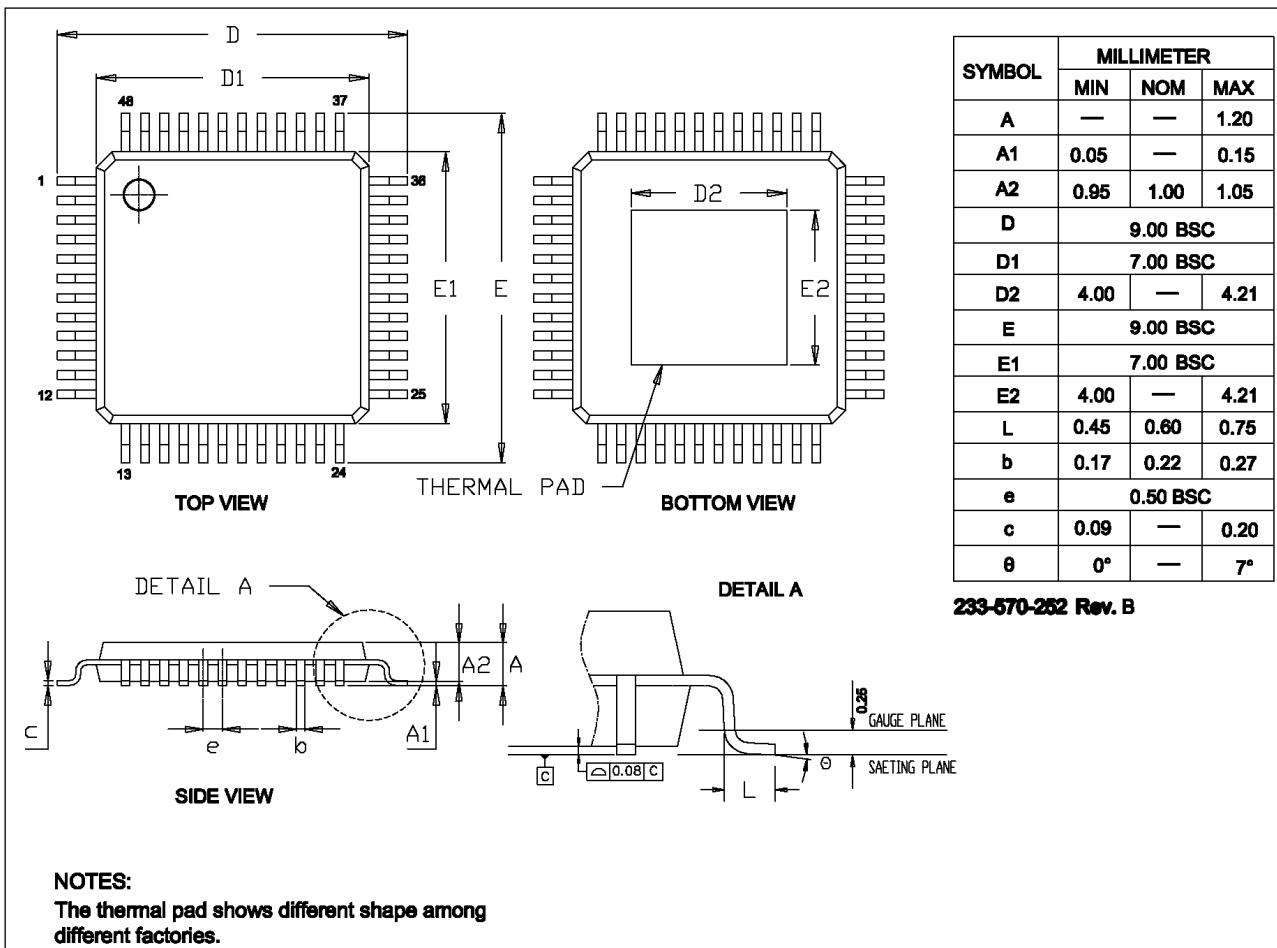
PACKAGE INFORMATION

QFN-48



IS31FL3733B

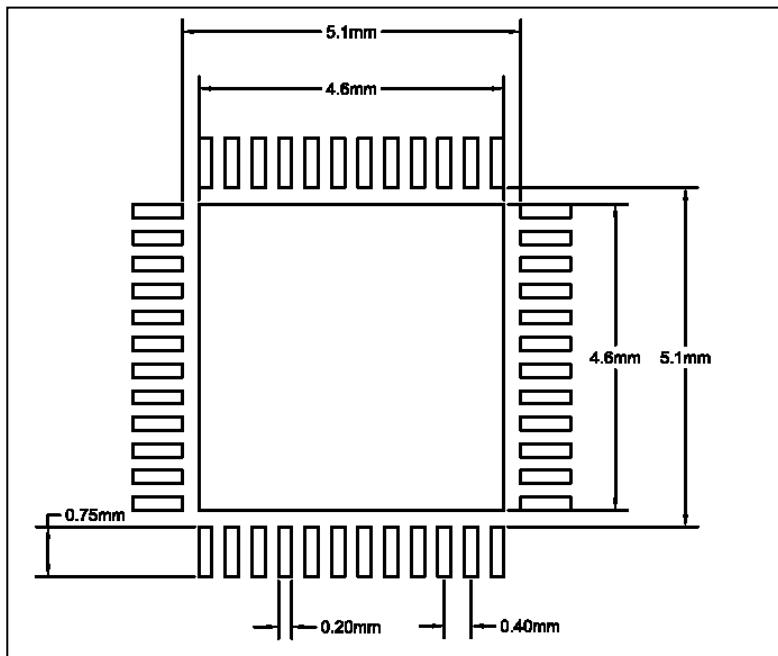
eTQFP-48



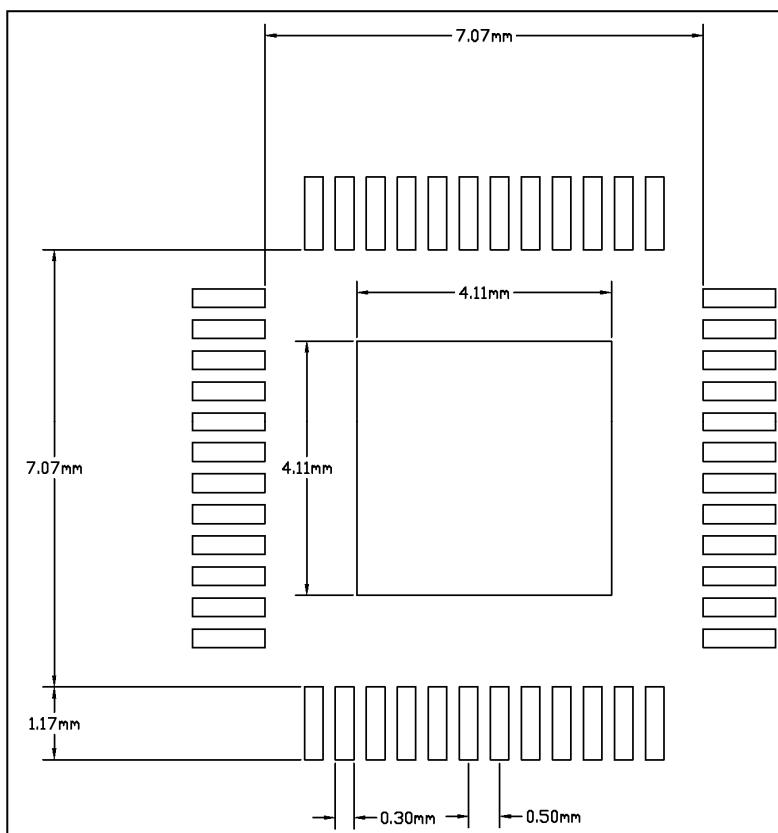
IS31FL3733B

RECOMMENDED LAND PATTERN

QFN-48



eTQFP-48



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

IS31FL3733B

REVISION HISTORY

| Revision | Detail Information | Date |
|----------|---|------------|
| 00A | Initial release | 2019.07.11 |
| 0A | Update PWM Frequency Setting | 2019.09.03 |
| A | Release to mass production | 2019.11.06 |
| B | Add 2500/reel for eTQFP package | 2020.07.23 |
| C | Correct PUR bit's mistake | 2020.10.19 |
| D | 1. Add note for T4 setting 2. Update POD and LP | 2021.11.03 |
| E | 1. Update to new Lumissil logo and add RoHS 2. Add “open drain” for INTB pin description | 2024.10.29 |