





This is an experimental "bit crusher" circuit. The signal is switched on/off at high frequency using the analog switch IC. This will reduce the resolution of the input signal in the time domain (as opposed to the normal bit crushing effect of reducing the amplitude resolution) The addition of capacitors after the analog switch IC, allows the block to function as a kind of Sample and Hold circuit. This should cause a smoothing effect on the output signal, which may or may not be desirable. Capacitor Position: Only one capacitor should be used, with the other footprint bridged. When using the lower capacitor, droop rate (during hold mode) will be directly related by the input voltage. When using the upper capacitor, the capacitor is connected to opamp virtual ground and the droop rate is constant. This is the recommended option. "The feedback significantly improves the accuracy of the S/H relative to the open-loop configuration, although the speed is somewhat less". Closed Loop is recommended option. Capacitor Value: "The acquisition time can be reduced by choosing a smaller hold capacitance; however, this will increase the hold step and droop rate." Default to 1nF but try other values: 1pF, 100nF, 1uF. https://www.ti.com/lit/an/snoa223/snoa223.pdf DNF if using other cap. Bridge the pins. 74HC4066 Analog Switch JP8 C8 1nF AS358AMTR AS358AMTR -DOUT U1B U1A C_DNF1 1nF GND +5V -5V U1C AS358AMTR C15 C18 100nF 100nF NegVoltRail3 >POS_VPP_IN NEG_VPP_OUTD GND GND File: NegVoltRail.kicad_sch Sheet: /InputBuffer/ File: Buffer.kicad_sch Title: Size: A4 Date: Rev: KiCad E.D.A. kicad (6.0.5-0) ld: 4/14

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