1. Description

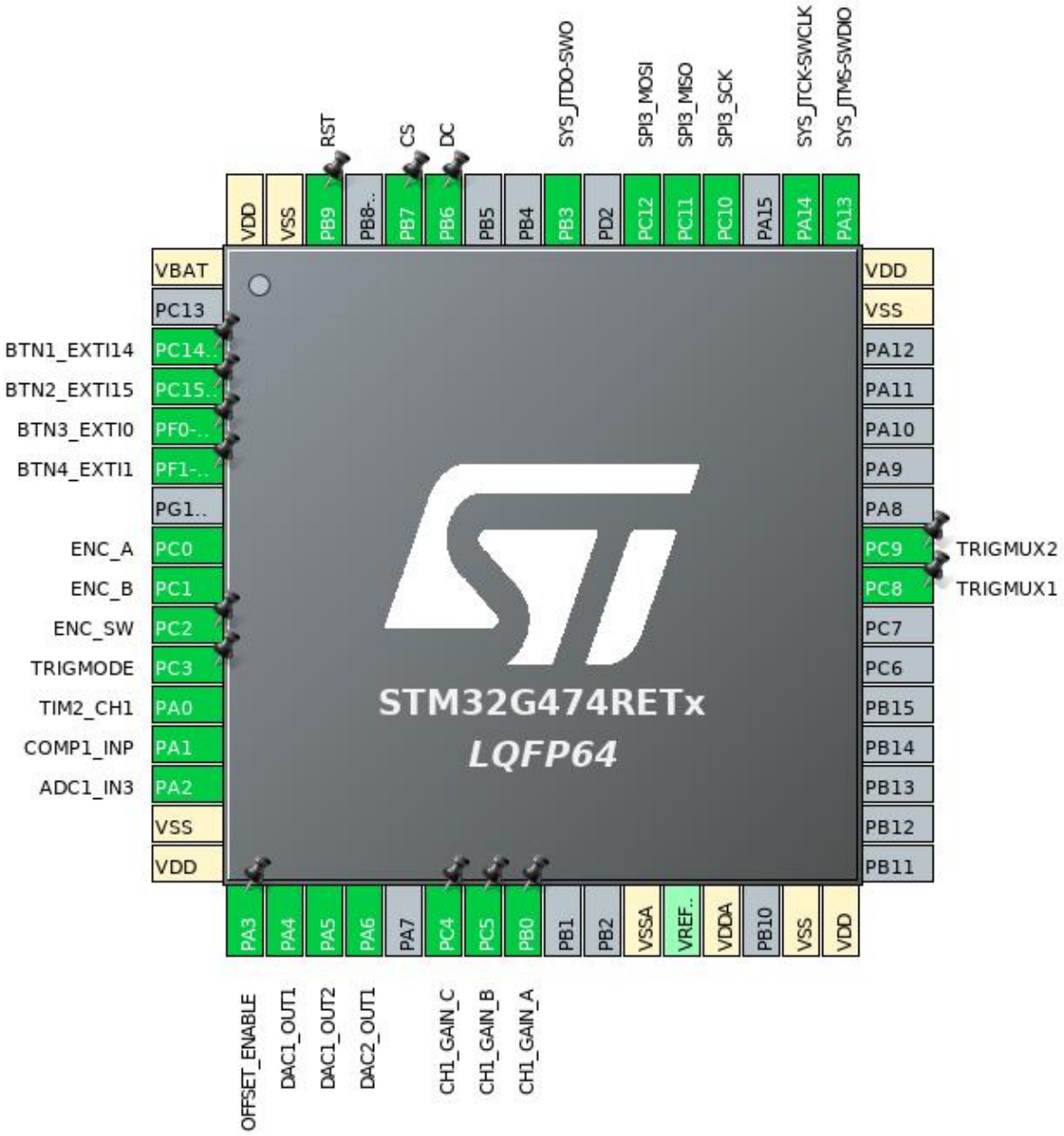
1.1. Project

Project Name	FunctionGeneratorCortexM4_SW_V1
Board Name	custom
Generated with:	STM32CubeMX 5.6.1
Date	06/21/2020

1.2. MCU

MCU Series	STM32G4
MCU Line	STM32G4x4
MCU name	STM32G474RETx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



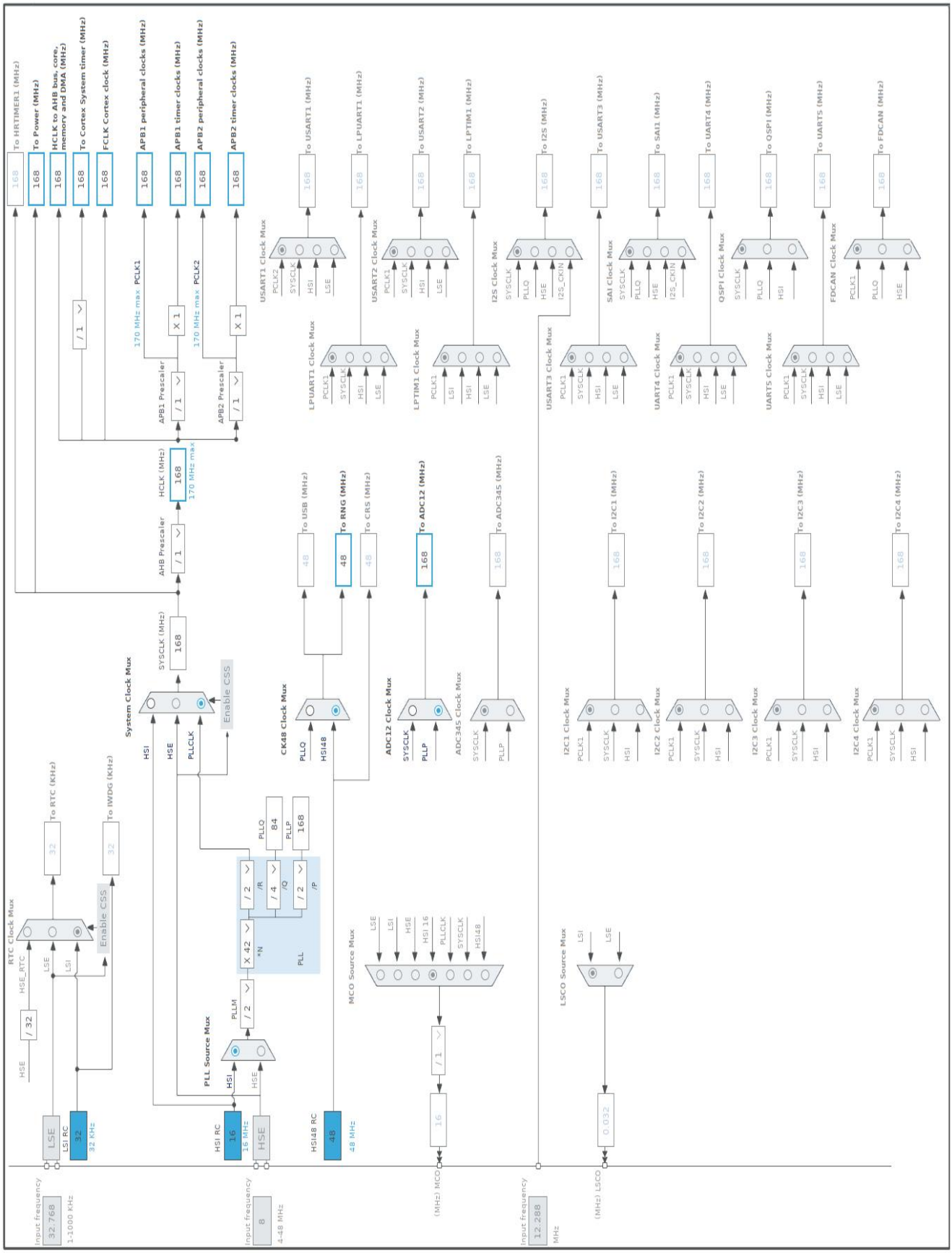
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
3	PC14-OSC32_IN	I/O	GPIO_EXTI14	BTN1_EXTI14
4	PC15-OSC32_OUT	I/O	GPIO_EXTI15	BTN2_EXTI15
5	PF0-OSC_IN	I/O	GPIO_EXTI0	BTN3_EXTI0
6	PF1-OSC_OUT	I/O	GPIO_EXTI1	BTN4_EXTI1
8	PC0	I/O	TIM1_CH1	ENC_A
9	PC1	I/O	TIM1_CH2	ENC_B
10	PC2	I/O	GPIO_EXTI2	ENC_SW
11	PC3 *	I/O	GPIO_Output	TRIGMODE
12	PA0	I/O	TIM2_CH1	
13	PA1	I/O	COMP1_INP	
14	PA2	I/O	ADC1_IN3	
15	VSS	Power		
16	VDD	Power		
17	PA3 *	I/O	GPIO_Output	OFFSET_ENABLE
18	PA4	I/O	DAC1_OUT1	
19	PA5	I/O	DAC1_OUT2	
20	PA6	I/O	DAC2_OUT1	
22	PC4 *	I/O	GPIO_Output	CH1_GAIN_C
23	PC5 *	I/O	GPIO_Output	CH1_GAIN_B
24	PB0 *	I/O	GPIO_Output	CH1_GAIN_A
27	VSSA	Power		
29	VDDA	Power		
31	VSS	Power		
32	VDD	Power		
40	PC8 *	I/O	GPIO_Output	TRIGMUX1
41	PC9 *	I/O	GPIO_Output	TRIGMUX2
47	VSS	Power		
48	VDD	Power		
49	PA13	I/O	SYS_JTMS-SWDIO	
50	PA14	I/O	SYS_JTCK-SWCLK	
52	PC10	I/O	SPI3_SCK	
53	PC11	I/O	SPI3_MISO	
54	PC12	I/O	SPI3_MOSI	
56	PB3	I/O	SYS_JTDO-SWO	
59	PB6 *	I/O	GPIO_Output	DC

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
60	PB7 *	I/O	GPIO_Output	CS
62	PB9 *	I/O	GPIO_Output	RST
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	FunctionGeneratorCortexM4_SW_V1
Project Folder	/home/chris/Projects/Embedded/FunctionGeneratorCortexM4_SW/FunctionGene
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_G4 V1.2.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32G4
Line	STM32G4x4
MCU	STM32G474RETx
Datasheet	DS12288_Rev0

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

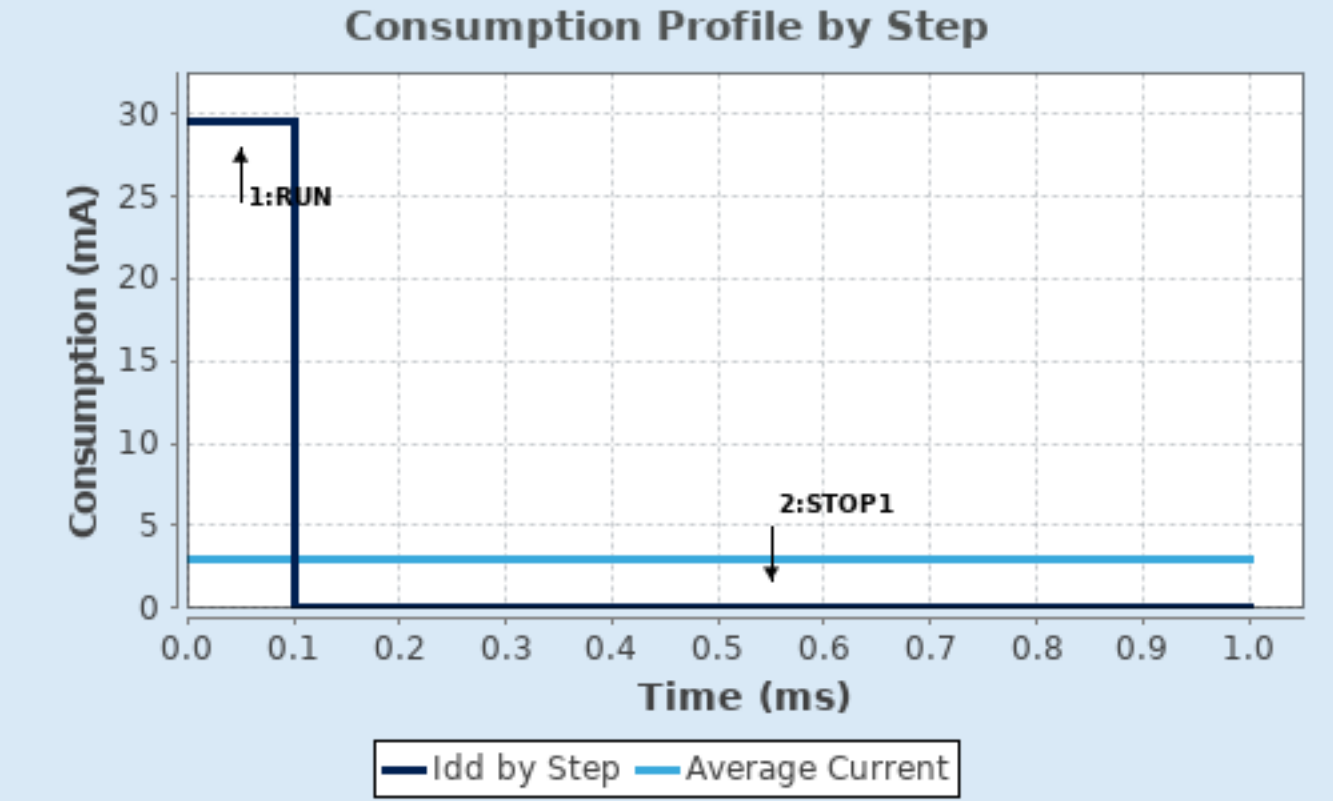
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP1
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-Boost	NoRange
Fetch Type	FLASH/DualBank/ART	NA
CPU Frequency	170 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	29.5 mA	80.5 µA
Duration	0.1 ms	0.9 ms
DMIPS	213.0	0.0
Ta Max	124.25	129.98
Category	In DS Table	In DS Table

6.5. RESULTS

Sequence Time	1 ms	Average Current	3.02 mA
Battery Life	1 month, 16 days, 9 hours	Average DMIPS	212.5 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
30
25
20
15
10
5
0
1:RUN
2:STOP1
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. IPs and Middleware Configuration

7.1. ADC1

IN3: IN3 Single-ended

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Gain Compensation	0
Scan Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Low Power Auto Wait	Disabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
Overrun behaviour	**Overrun data overwritten ***

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 3
Sampling Time	2.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. COMP1

mode: Input [+]

Input [-]: Internal VRef

7.2.1. Parameter Settings:

Basic Parameters:

Trigger Mode	**Rising/Falling Edge Interrupt ***
Hysteresis Level	**High ***

Output Configuration:

Blanking Source	None
Output Pol	COMP output on GPIO isn't inverted

7.3. DAC1

OUT1 mode: Connected to external pin only

OUT2 mode: Connected to external pin only

7.3.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
DAC High Frequency	**Mode Above 80MHz ***
DMA Double Data	Disable
Signed Format	Disable
Trigger	**Timer 8 Trigger Out event ***
Trigger2	None
Wave generation mode	Disabled
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

DAC Out2 Settings:

Output Buffer	Enable
DAC High Frequency	Mode Above 80MHz
DMA Double Data	Disable
Signed Format	Disable
Trigger	None
Trigger2	None
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

7.4. DAC2

OUT1 mode: Connected to external pin only

7.4.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
DAC High Frequency	**Mode Above 80MHz ***
DMA Double Data	Disable
Signed Format	Disable
Trigger	**Timer 8 Trigger Out event ***
Trigger2	None
Wave generation mode	Disabled
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

7.5. GPIO

7.6. RCC

7.6.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	8WS (7 CPU cycle)

RCC Parameters:

HSI Calibration Value	64
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1 boost

Peripherals Clock Configuration:

Generate the peripherals clock configuration	TRUE

7.7. RNG

mode: Activated

7.7.1. Parameter Settings:

Clock Error Detection	Enable

7.8. SPI3

Mode: Full-Duplex Master

7.8.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**8 ***
Baud Rate	**21.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.9. SYS

Debug: Trace Asynchronous Sw

Timebase Source: SysTick

mode: save power of non-active UCPD - deactive Dead Battery pull-up

7.10. TIM1

Combined Channels: Encoder Mode

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	**Center Aligned mode3 ***
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	**1024 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Pulse On Compare (Common for Channel 3 and 4):

Pulse Width Prescaler	0
Pulse Width	0

Encoder:

Encoder Mode	**Encoder Mode TI2 ***
Slave Mode Preload Activation	Disable
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.11. TIM2

Slave Mode: Reset Mode

Trigger Source: TI1FP1

Channel1: Input Capture direct mode

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**128 ***
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 32 bits value)	**65535 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***
Slave Mode Controller	Reset Mode

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***

Pulse On Compare (Common for Channel 3 and 4):

Pulse Width Prescaler	0
Pulse Width	0

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.12. TIM3

Clock Source : Internal Clock

7.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	**Down ***
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	**1 ***
Internal Clock Division (CKD)	**Division by 4 ***
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***

Pulse On Compare (Common for Channel 3 and 4):

Pulse Width Prescaler	0
Pulse Width	0

7.13. TIM5

Clock Source : Internal Clock

7.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 32 bits value)	**1024 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Pulse On Compare (Common for Channel 3 and 4):

Pulse Width Prescaler	0
Pulse Width	0

7.14. TIM8

Clock Source : Internal Clock

7.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	**1 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Pulse On Compare (Common for Channel 3 and 4):

Pulse Width Prescaler	0
Pulse Width	0

7.15. TIM15

mode: Clock Source

7.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**1024 ***
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	**1024 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.16. TIM16

mode: Activated

7.16.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**65535 ***
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	**65535 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

7.17. TIM17

mode: Activated

7.17.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**1024 ***
Counter Mode	Up
Dithering	Disable
Counter Period (AutoReload Register - 16 bits value)	**1024 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA2	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	
COMP1	PA1	COMP1_INP	Analog mode	No pull-up and no pull-down	n/a	
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	
	PA5	DAC1_OUT2	Analog mode	No pull-up and no pull-down	n/a	
DAC2	PA6	DAC2_OUT1	Analog mode	No pull-up and no pull-down	n/a	
SPI3	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC12	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	
TIM1	PC0	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	ENC_A
	PC1	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	ENC_B
TIM2	PA0	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PC14-OSC32_IN	GPIO_EXTI14	**External Interrupt Mode with Falling edge trigger detection**	**Pull-up ***	n/a	BTN1_EXTI14
	PC15-OSC32_OUT	GPIO_EXTI15	**External Interrupt Mode with Falling edge trigger detection**	**Pull-up ***	n/a	BTN2_EXTI15
	PF0-OSC_IN	GPIO_EXTI0	**External Interrupt Mode with Falling edge trigger detection**	**Pull-up ***	n/a	BTN3_EXTI0
	PF1-OSC_OUT	GPIO_EXTI1	**External Interrupt Mode with Falling edge trigger detection**	**Pull-up ***	n/a	BTN4_EXTI1
	PC2	GPIO_EXTI2	**External Interrupt Mode with Falling edge trigger detection**	**Pull-up ***	n/a	ENC_SW
	PC3	GPIO_Output	Output Push Pull	**Pull-down ***	Low	TRIGMODE
	PA3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OFFSET_ENABLE
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CH1_GAIN_C

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CH1_GAIN_B
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CH1_GAIN_A
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TRIGMUX1
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TRIGMUX2
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	DC
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	CS
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	RST

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low
DAC2_CH1	DMA1_Channel3	Memory To Peripheral	Low
DAC1_CH1	DMA1_Channel2	Memory To Peripheral	Low
TIM2_CH1	DMA1_Channel4	Peripheral To Memory	Low

ADC1: DMA1_Channel1 DMA request Settings:

Mode: **Circular ***
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: **Word ***
Memory Data Width: **Word ***

DAC2_CH1: DMA1_Channel3 DMA request Settings:

Mode: **Circular ***
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: **Word ***
Memory Data Width: **Word ***

DAC1_CH1: DMA1_Channel2 DMA request Settings:

Mode: **Circular ***
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: **Word ***
Memory Data Width: **Word ***

TIM2_CH1: DMA1_Channel4 DMA request Settings:

Mode: **Circular ***
Peripheral Increment: Disable
Memory Increment: **Enable ***

Peripheral Data Width:	Word
Memory Data Width:	Word

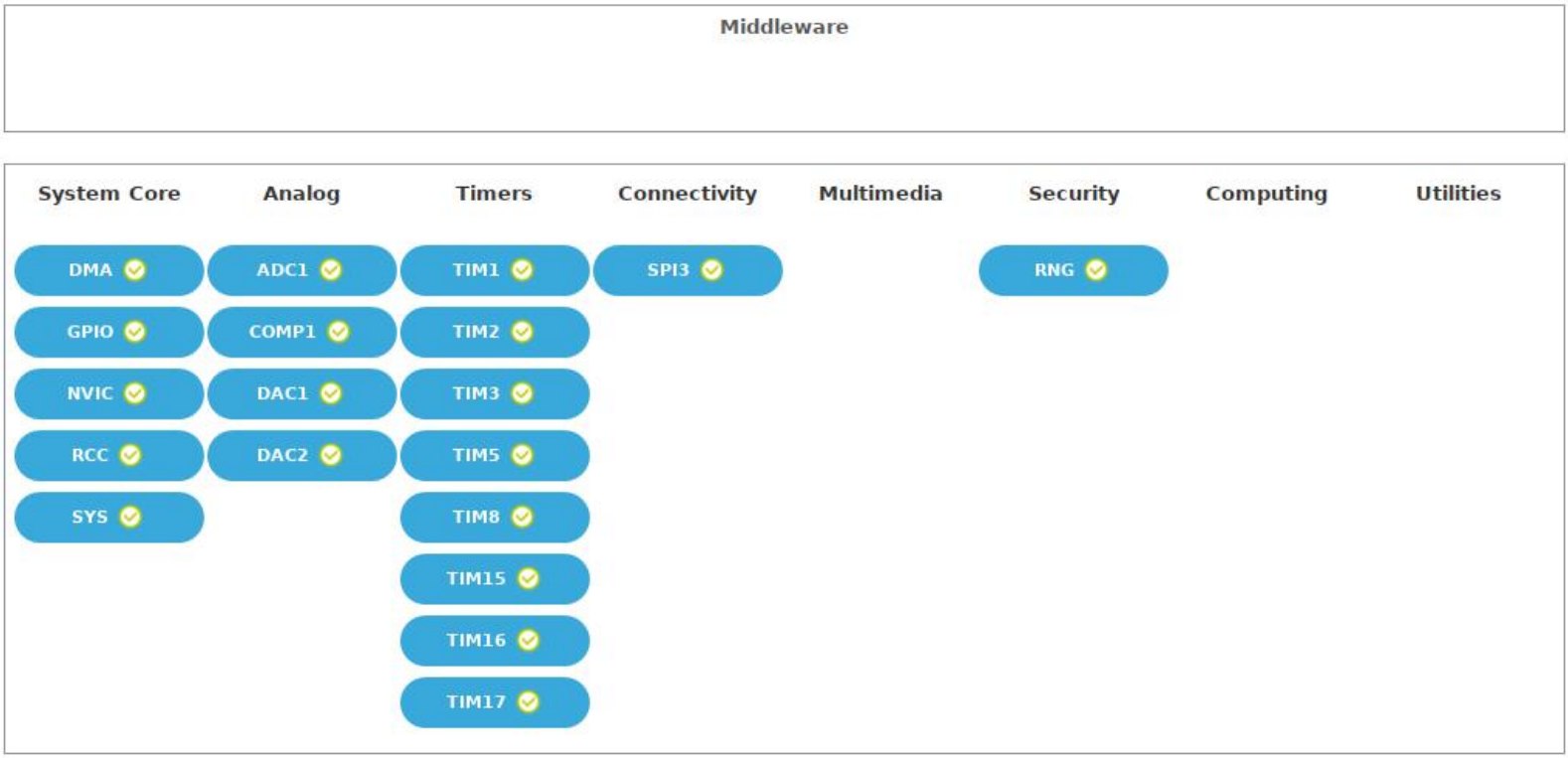
8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line0 interrupt	true	0	0
EXTI line1 interrupt	true	0	0
EXTI line2 interrupt	true	0	0
DMA1 channel1 global interrupt	true	1	0
DMA1 channel2 global interrupt	true	0	0
DMA1 channel3 global interrupt	true	0	0
DMA1 channel4 global interrupt	true	0	0
TIM1 break interrupt and TIM15 global interrupt	true	0	0
TIM1 trigger and commutation interrupts and TIM17 global interrupt	true	1	0
TIM3 global interrupt	true	0	0
EXTI line[15:10] interrupts	true	0	0
TIM5 global interrupt	true	2	0
COMP1, COMP2 and COMP3 interrupts through EXTI lines 21, 22 and 29	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/38/39/40/41	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupt	unused		
TIM1 update interrupt and TIM16 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM8 break interrupt	unused		
TIM8 update interrupt	unused		
TIM8 trigger and commutation interrupts	unused		
TIM8 capture compare interrupt	unused		
SPI3 global interrupt	unused		
TIM6 global interrupt, DAC1 and DAC3 channel underrun error interrupts	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
TIM7 global interrupt, DAC2 and DAC4 channel underrun error interrupts	unused		
FPU global interrupt	unused		
RNG global interrupt	unused		

*** User modified value**

9. Predefined Views - Category view : Current



10. Software Pack Report