# 1. Description

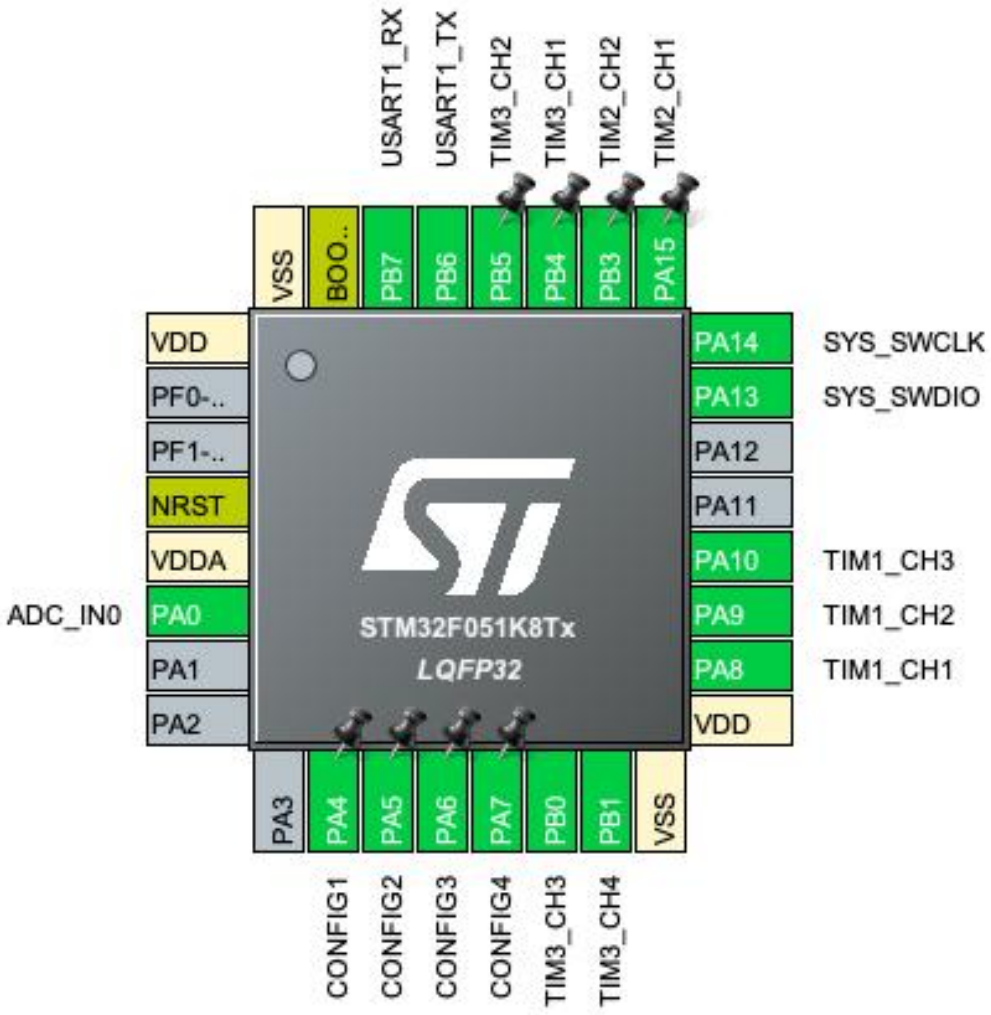
## 1.1. Project

| | |
|---|---|
| Project Name | MidiLedController_sw_2 |
| Board Name | custom |
| Generated with: | STM32CubeMX 5.6.0 |
| Date | 06/06/2020 |

## 1.2. MCU

| | |
|---|---|
| MCU Series | STM32F0 |
| MCU Line | STM32F0x1 |
| MCU name | STM32F051K8Tx |
| MCU Package | LQFP32 |
| MCU Pin number | 32 |

## 2. Pinout Configuration

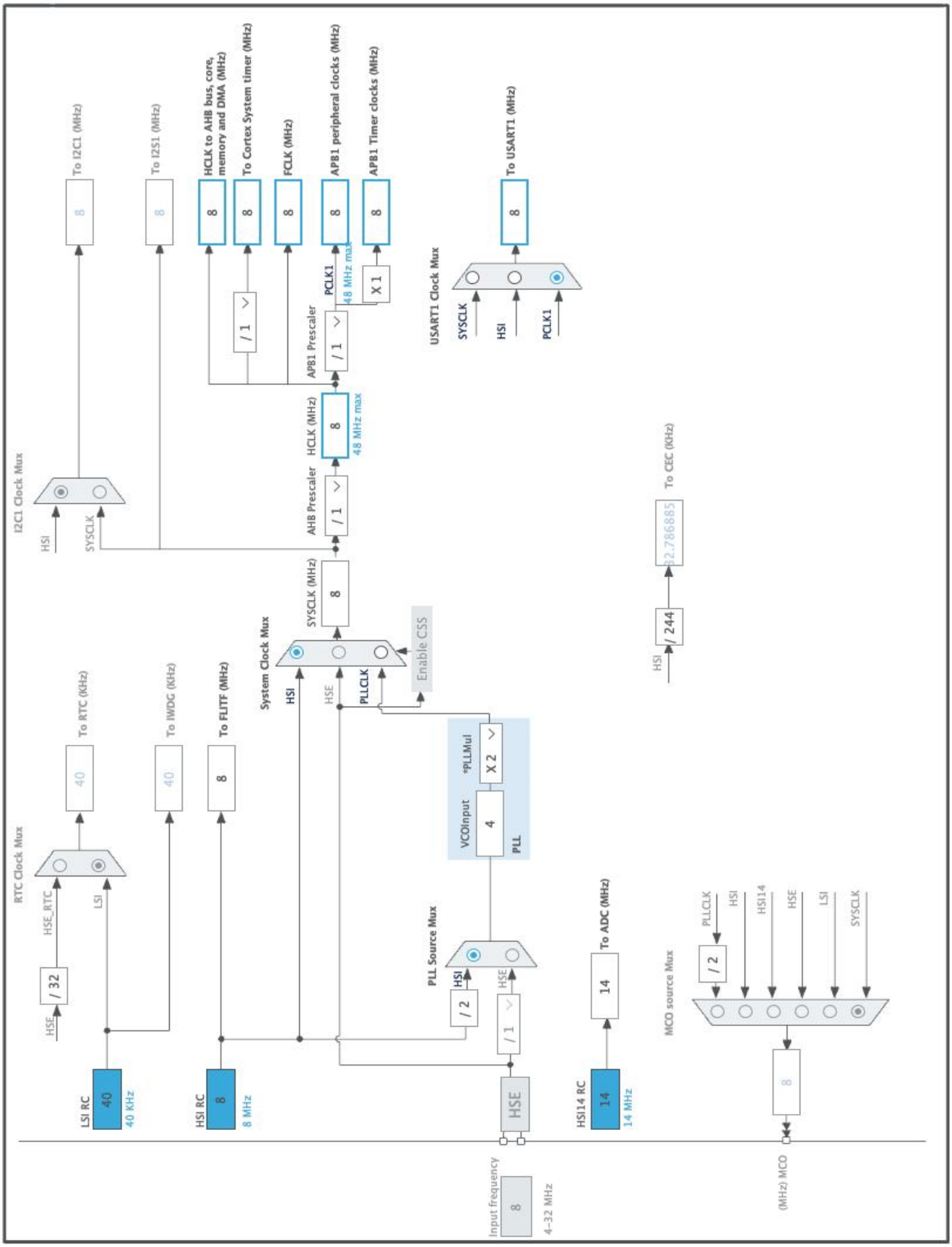


# 3. Pins Configuration

| Pin Number LQFP32 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 1 | VDD | Power | | |
| 4 | NRST | Reset | | |
| 5 | VDDA | Power | | |
| 6 | PA0 | I/O | ADC_IN0 | |
| 10 | PA4 * | I/O | GPIO_Input | CONFIG1 |
| 11 | PA5 * | I/O | GPIO_Input | CONFIG2 |
| 12 | PA6 * | I/O | GPIO_Input | CONFIG3 |
| 13 | PA7 * | I/O | GPIO_Input | CONFIG4 |
| 14 | PB0 | I/O | TIM3_CH3 | |
| 15 | PB1 | I/O | TIM3_CH4 | |
| 16 | VSS | Power | | |
| 17 | VDD | Power | | |
| 18 | PA8 | I/O | TIM1_CH1 | |
| 19 | PA9 | I/O | TIM1_CH2 | |
| 20 | PA10 | I/O | TIM1_CH3 | |
| 23 | PA13 | I/O | SYS_SWDIO | |
| 24 | PA14 | I/O | SYS_SWCLK | |
| 25 | PA15 | I/O | TIM2_CH1 | |
| 26 | PB3 | I/O | TIM2_CH2 | |
| 27 | PB4 | I/O | TIM3_CH1 | |
| 28 | PB5 | I/O | TIM3_CH2 | |
| 29 | PB6 | I/O | USART1_TX | |
| 30 | PB7 | I/O | USART1_RX | |
| 31 | BOOT0 | Boot | | |
| 32 | VSS | Power | | |

* The pin is affected with an I/O function

# 4. Clock Tree Configuration



# 5. Software Project

## 5.1. Project Settings

| Name | Value |
|---|---|
| Project Name | MidiLedController_sw_2 |
| Project Folder | /Users/chrissutton/Projects/EmbeddedProjects/MidiLedController_sw_2/MidiLedC |
| Toolchain / IDE | STM32CubeIDE |
| Firmware Package Name and Version | STM32Cube FW_F0 V1.11.0 |

## 5.2. Code Generation Settings

| Name | Value |
|---|---|
| STM32Cube MCU packages and embedded software | Copy only the necessary library files |
| Generate peripheral initialization as a pair of '.c/.h' files | Yes |
| Backup previously generated files when re-generating | No |
| Delete previously generated files when not re-generated | Yes |
| Set all free pins as analog (to optimize the power consumption) | No |

# 6. Power Consumption Calculator report

6.1. Microcontroller Selection

| | |
|---|---|
| Series | STM32F0 |
| Line | STM32F0x1 |
| MCU | STM32F051K8Tx |
| Datasheet | 022265_Rev7 |

6.2. Parameter Selection

| | |
|---|---|
| Temperature | 25 |
| Vdd | 3.3 |

6.3. Battery Selection

| | |
|---|---|
| Battery | Li-SOCL2(A3400) |
| Capacity | 3400.0 mAh |
| Self Discharge | 0.08 %/month |
| Nominal Voltage | 3.6 V |
| Max Cont Current | 100.0 mA |
| Max Pulse Current | 200.0 mA |
| Cells in series | 1 |
| Cells in parallel | 1 |

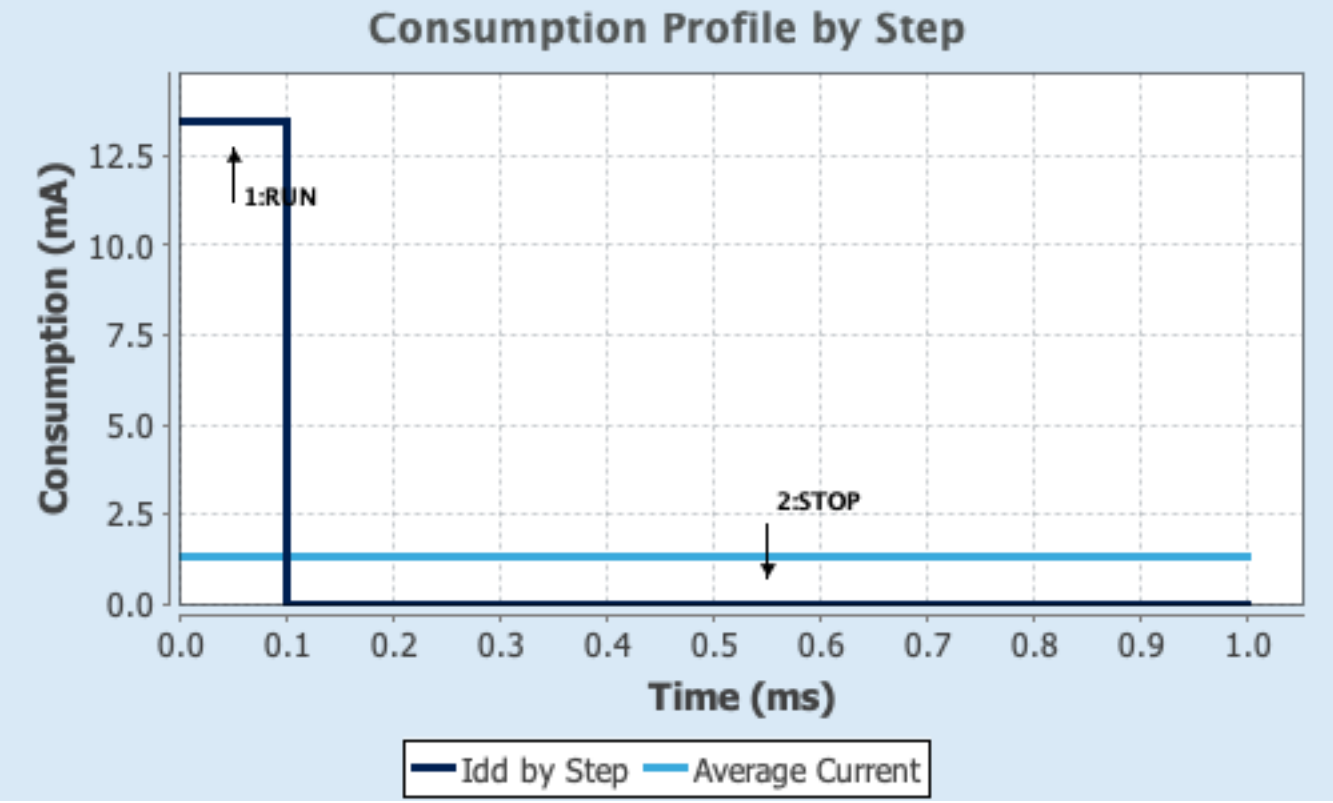
6.4. Sequence

| ***Step*** | Step1 | Step2 |
|---|---|---|
| ***Mode*** | RUN | STOP |
| ***Vdd*** | 3.3 | 3.3 |
| ***Voltage Source*** | Battery | Battery |
| ***Range*** | No Scale | No Scale |
| ***Fetch Type*** | FLASH | n/a |
| ***CPU Frequency*** | 48 MHz | 0 Hz |
| ***Clock Configuration*** | HSE PLL | Regulator_LP |
| ***Clock Source Frequency*** | 8 MHz | 0 Hz |
| ***Peripherals*** | | |
| ***Additional Cons.*** | 0 mA | 0 mA |
| ***Average Current*** | 13.45 mA | 6.2 µA |
| ***Duration*** | 0.1 ms | 0.9 ms |
| ***DMIPS*** | 0.0 | 0.0 |
| ***Ta Max*** | 102.51 | 105 |
| ***Category*** | In DS Table | In DS Table |

## 6.5. RESULTS

| Sequence Time | 1 ms | Average Current | 1.35 mA |
|---|---|---|---|
| Battery Life | 3 months, 13 days, 8 hours | Average DMIPS | 0.0 DMIPS |

## 6.6. Chart


Consumption Profile by Step
Consumption (mA)
12.5
10.0
7.5
5.0
2.5
0.0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

# 7. IPs and Middleware Configuration

## 7.1. ADC

**mode: IN0**

### 7.1.1. Parameter Settings:

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | Asynchronous clock mode |
| Resolution | ADC 12-bit resolution |
| Data Alignment | Right alignment |
| Scan Conversion Mode | Forward |
| Continuous Conversion Mode | **Enabled *** |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | **Enabled *** |
| End Of Conversion Selection | End of single conversion |
| Overrun behaviour | **Overrun data overwritten *** |
| Low Power Auto Wait | Disabled |
| Low Power Auto Power Off | Disabled |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Sampling Time | 1.5 Cycles |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |

**WatchDog:**

| | |
|---|---|
| Enable Analog WatchDog Mode | false |

## 7.2. GPIO

## 7.3. RCC

### 7.3.1. Parameter Settings:

**System Parameters:**

| | |
|---|---|
| VDD voltage (V) | 3.3 |
| Prefetch Buffer | Enabled |
| Flash Latency(WS) | 0 WS (1 CPU cycle) |

**RCC Parameters:**

| | |
|---|---|
| HSI Calibration Value | 16 |
| HSI14 Calibration Value | 16 |
| HSE Startup Timout Value (ms) | 100 |

| | |
|---|---|
| LSE Startup Timout Value (ms) | 5000 |

## 7.4. SYS

**mode: Debug Serial Wire**

**Timebase Source: SysTick**

## 7.5. TIM1

**Clock Source : Internal Clock**

**Channel1: PWM Generation CH1**

**Channel2: PWM Generation CH2**

**Channel3: PWM Generation CH3**

### 7.5.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **1 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | **255 *** |
| Internal Clock Division (CKD) | No Division |
| Repetition Counter (RCR - 8 bits value) | 0 |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

**Break And Dead Time management - BRK Configuration:**

| | |
|---|---|
| BRK State | Disable |
| BRK Polarity | High |

**Break And Dead Time management - Output Configuration:**

| | |
|---|---|
| Automatic Output State | Disable |
| Off State Selection for Run Mode (OSSR) | Disable |
| Off State Selection for Idle Mode (OSSI) | Disable |
| Lock Configuration | Off |

**Clear Input:**

| | |
|---|---|
| Clear Input Source | Disable |

**PWM Generation Channel 1:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |

| | |
|---|---|
| Fast Mode | Disable |
| CH Polarity | High |
| CH Idle State | Reset |

**PWM Generation Channel 2:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |
| CH Idle State | Reset |

**PWM Generation Channel 3:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |
| CH Idle State | Reset |

## *7.6. TIM2*

### Channel1: PWM Generation CH1

### Channel2: PWM Generation CH2

### 7.6.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **1 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 32 bits value ) | **64 *** |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

**Clear Input:**

| | |
|---|---|
| Clear Input Source | Disable |

**PWM Generation Channel 1:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (32 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |

| | |
|---|---|
| CH Polarity | High |

**PWM Generation Channel 2:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (32 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

## *7.7. TIM3*

**Channel1: PWM Generation CH1**
**Channel2: PWM Generation CH2**
**Channel3: PWM Generation CH3**
**Channel4: PWM Generation CH4**

### 7.7.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **1 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | **255 *** |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

**Clear Input:**

| | |
|---|---|
| Clear Input Source | Disable |

**PWM Generation Channel 1:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 2:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 3:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 4:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Output compare preload | Enable |
| Fast Mode | Disable |
| CH Polarity | High |

## *7.8. TIM16*

**mode: Activated**

**mode: One Pulse Mode**

### 7.8.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **64 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | **65535 *** |
| Internal Clock Division (CKD) | No Division |
| Repetition Counter (RCR - 8 bits value) | 0 |
| auto-reload preload | Disable |

## *7.9. USART1*

**Mode: Asynchronous**

### 7.9.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | **31250 *** |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |

### Advanced Features:

| | |
|---|---|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

*** User modified value**

# 8. System Configuration

## 8.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| ADC | PA0 | ADC_IN0 | Analog mode | No pull-up and no pull-down | n/a | |
| SYS | PA13 | SYS_SWDIO | n/a | n/a | n/a | |
| | PA14 | SYS_SWCLK | n/a | n/a | n/a | |
| TIM1 | PA8 | TIM1_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PA9 | TIM1_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PA10 | TIM1_CH3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| TIM2 | PA15 | TIM2_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PB3 | TIM2_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| TIM3 | PB0 | TIM3_CH3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PB1 | TIM3_CH4 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PB4 | TIM3_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PB5 | TIM3_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| USART1 | PB6 | USART1_TX | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| | PB7 | USART1_RX | Alternate Function Push Pull | No pull-up and no pull-down | **High *** | |
| GPIO | PA4 | GPIO_Input | Input mode | **Pull-up *** | n/a | CONFIG1 |
| | PA5 | GPIO_Input | Input mode | **Pull-up *** | n/a | CONFIG2 |
| | PA6 | GPIO_Input | Input mode | **Pull-up *** | n/a | CONFIG3 |
| | PA7 | GPIO_Input | Input mode | **Pull-up *** | n/a | CONFIG4 |

## 8.2. DMA configuration

| DMA request | Stream | Direction | Priority |
|---|---|---|---|
| ADC | DMA1_Channel1 | Peripheral To Memory | Low |

*ADC: DMA1_Channel1 DMA request Settings:*

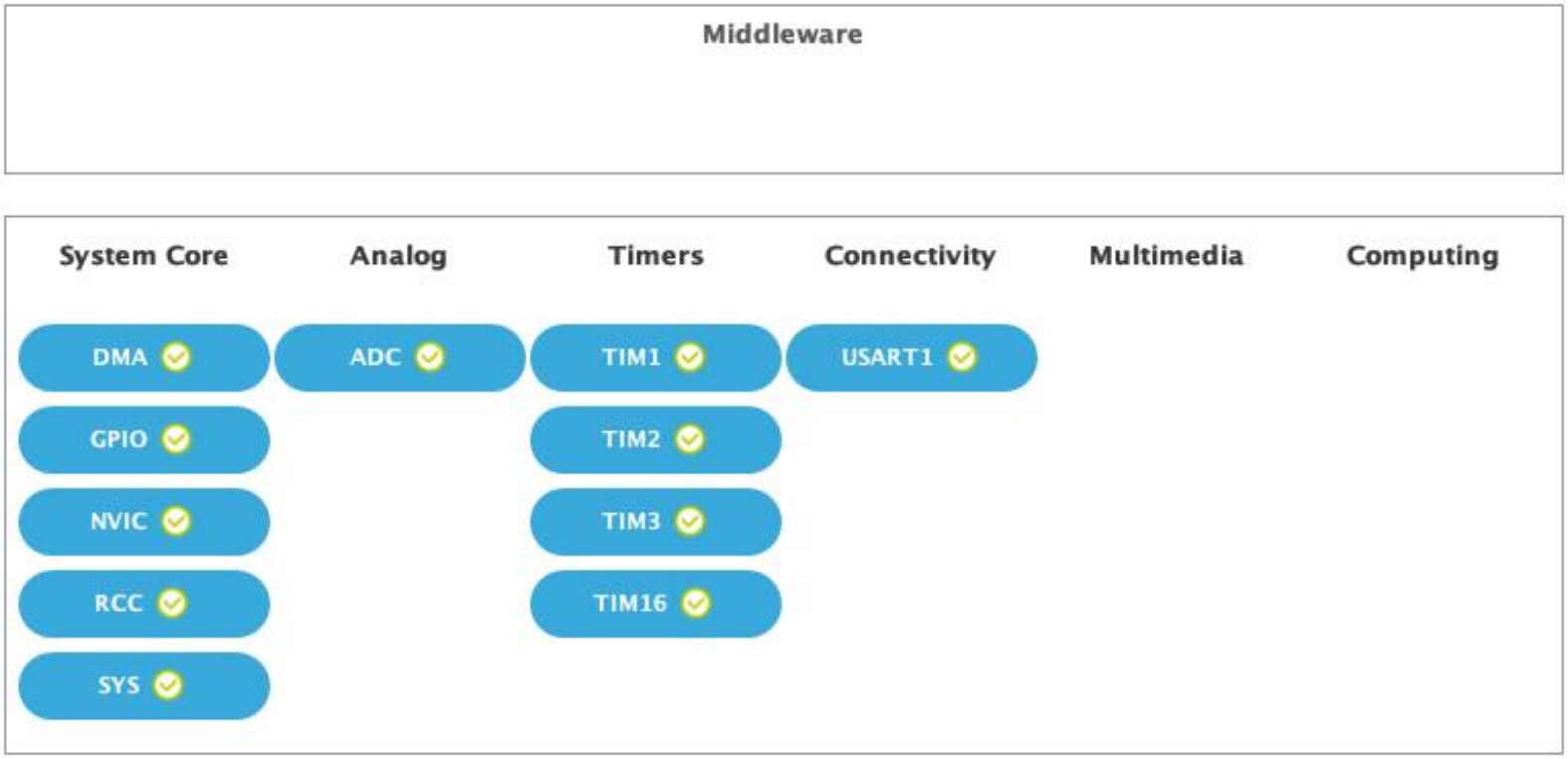
| | |
|---|---|
| Mode: | **Circular *** |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | **Word *** |
| Memory Data Width: | **Word *** |

## 8.3. NVIC configuration

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Pendable request for system service | true | 0 | 0 |
| System tick timer | true | 0 | 0 |
| DMA1 channel 1 interrupt | true | 1 | 0 |
| TIM16 global interrupt | true | 0 | 0 |
| USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25 | true | 0 | 0 |
| PVD interrupt through EXTI Line16 | unused | | |
| Flash global interrupt | unused | | |
| RCC global interrupt | unused | | |
| ADC and COMP interrupts (COMP interrupts through EXTI lines 21 and 22) | unused | | |
| TIM1 break, update, trigger and commutation interrupts | unused | | |
| TIM1 capture compare interrupt | unused | | |
| TIM2 global interrupt | unused | | |
| TIM3 global interrupt | unused | | |

*** User modified value**

## 9. Predefined Views - Category view : Current



# 10. Software Pack Report