

Powering an i.MX 6SX-based system using the PF3000 PMIC

1 Introduction

The PF3000 is a highly integrated Power Management IC ideally suited to power NXP's i.MX 6SX, i.MX 6SL, i.MX 6S, i.MX 6DL, i.MX 6UL and the i.MX 7 series of applications processors. This Application Note discusses the power tree configuration for powering an i.MX 6SX based system using the PF3000.

NXP analog ICs are manufactured using the SMARTMOS process, a combinational BiCMOS manufacturing flow that integrates precision analog, power functions and dense CMOS logic together on a single cost-effective die.

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2 PF3000 voltage regulators

[Table 1](#) shows a summary of the voltage regulators in the PF3000. Output voltage and startup sequence of the regulators is programmed into the PMIC through One Time Programmable (OTP) memory. For more details, refer to the product datasheet.

Table 1. PF3000 voltage regulators

Regulator	Output voltage range	Load current rating
SW1A	0.7 V to 1.425 V 1.8 V 3.3 V	1000 mA
SW1B	0.7 V to 1.475 V	1750 mA
SW2	1.5 V to 1.85 V 2.5 V to 3.3 V	1250 mA
SW3	0.9 V to 1.65 V	1500 mA
SWBST	5.0 V to 5.15 V	600 mA
VSNVS	3.0 V	1.0 mA
VLDO1	1.8 V to 3.3 V	100 mA
VLDO2	0.8 V to 1.55 V	250 mA
VLDO3	1.8 V to 3.3 V	100 mA
VLDO4	1.8 V to 3.3 V	350 mA
VCC_SD	1.8 V to 1.85 V 2.85 V to 3.3 V	100 mA
V33	2.85 V to 3.3 V	350 mA
VREFDDR	VINREFDDR/2	10 mA

3 i.MX 6SX power management using the PF3000

The i.MX 6SX processor features NXP's advanced implementation of the a single ARM® Cortex®-A9 MPCore™ multicore processor, which operates at speeds up to 1 GHz. [Table 2](#) shows how PF3000 can be used to power an i.MX 6SX based system. This include the voltage rails required by the processor as well as memory and common peripherals. As a programming PMIC, the PF3000 can be used in a number of ways to power the i.MX 6SX. [Table 2](#) lists one of the many possibilities. The power tree can be optimized based on specific application requirements.

Table 2. PF3000 + i.MX 6SX power tree

Regulator	Voltage	Sequence	Load domain
SW1A	1.375 V	2	VDDCORE
SW1B	1.375 V	2	VDDSOC
SW2	3.3 V	4	NVCC_SD4, NVCC_NAND, NVCC_GPIO, NVCC_KEY, NVCC_QSPI, NVCC_LCD1, NVCC_HIGH (SD3), LCD Connector, CAN, Sensors, SD3 (SD3.0 Card), SD4 (SD Card-boot), QSPI Flash
SW3	1.35 V	3	DDR3L
SWBST	5.0 V	Off	N/A
VSNVS	3.0 V	0	VDD_SNVS_IN
VLDO1	3.3 V	Off	N/A
VLDO2	1.5 V	Off	Camera Connector, MPCIE
VLDO3	2.5 V	Off	Camera Connector, Audio Codec
VLDO4	1.8 V	4	NVCC_LOW(SD3), NVCC_CSI
VCC_SD	3.3 V	5	VDD_AFE_3P3, VDDA_ADC_3P3 (12-bit ADC), ADC_VREFH (12-bit ADC)
V33	3.0 V	1	VDD_HIGH_IN,VDD_HIGH_CAP
VREFDDR	0.625 V	3	DRAM_VREF

4 PF3000 power input

PF3000 input voltage range is 2.8 V to 4.5 V or 3.7 V to 5.5 V. 2.8 V to 4.5 V when VIN is used at input. 3.7 V to 5.5 V when VPWR is used as input.

For non-battery operated applications, when the input supply voltage exceeds 4.5 V, the front-end LDO can be activated by populating the external PMOS pass FET Q16 in [Figure 1](#) and connecting the VPWR pin to the main supply. In this case, the LDO control block self-starts with a local bandgap reference.

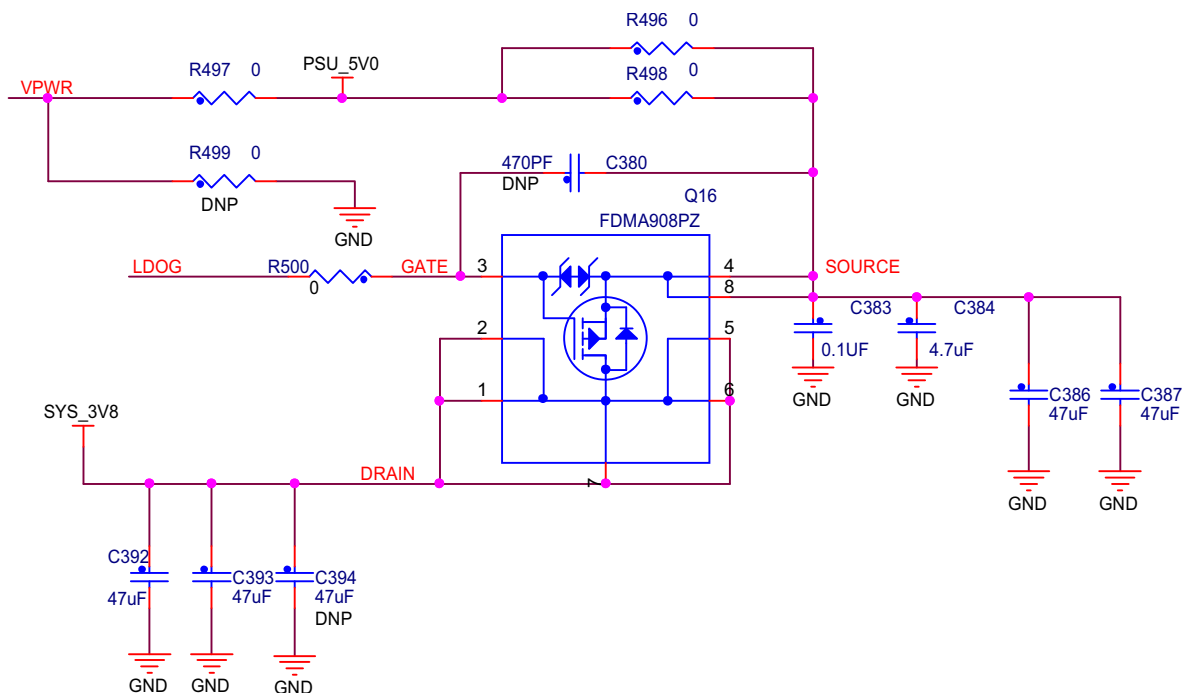


Figure 1. PF3000 5.0 V input circuit



The Application Note AN5094 provides best practices for the layout of the PF3000 device on printed circuit boards. To download AN5094, click on the following link: http://www.nxp.com/files/analog/doc/app_note/AN5094.pdf

NXP offers PF3000 code support for a custom i.MX 6 board at the NXP Community site <https://community.nxp.com/docs/DOC-105064>).



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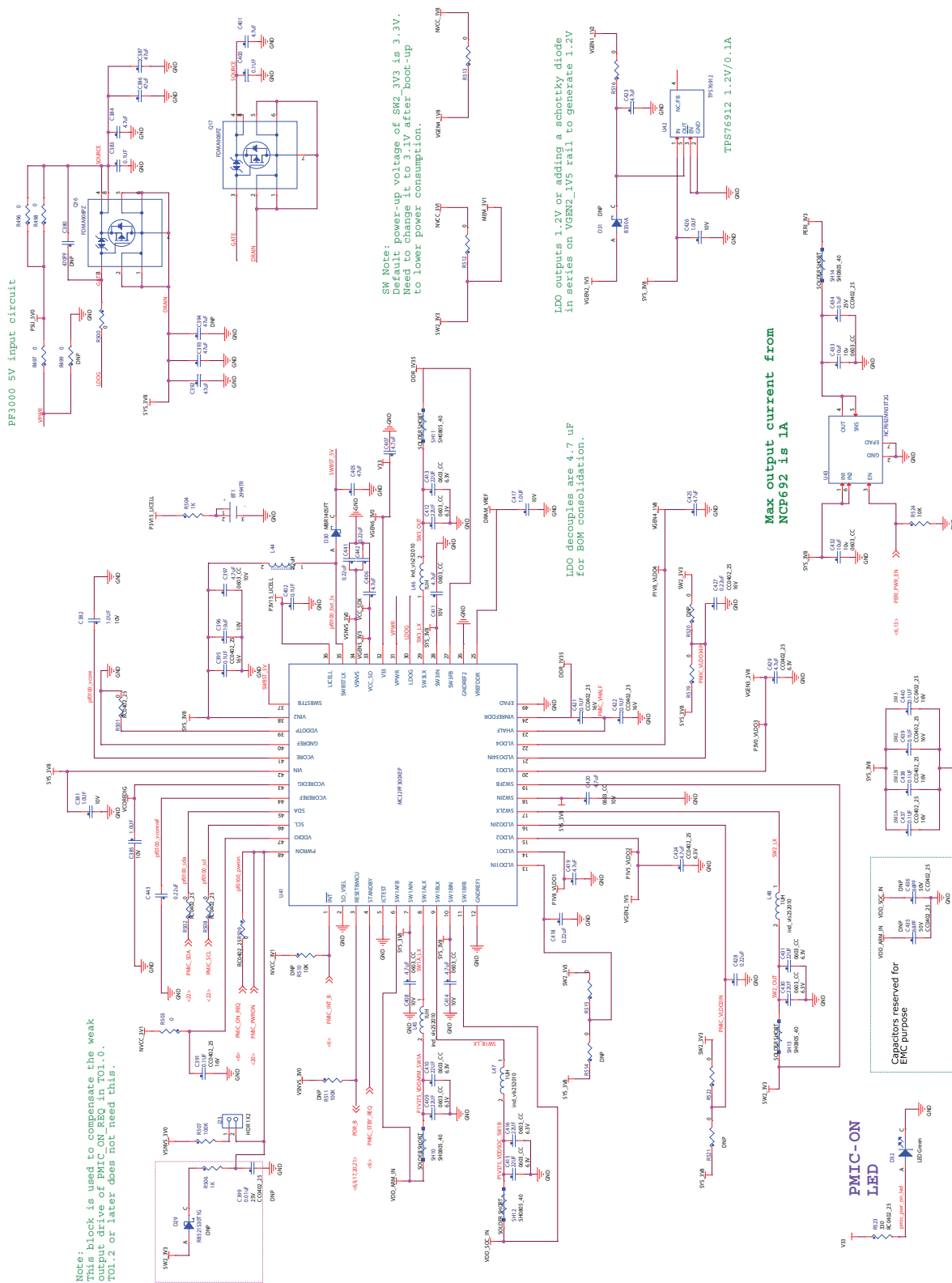
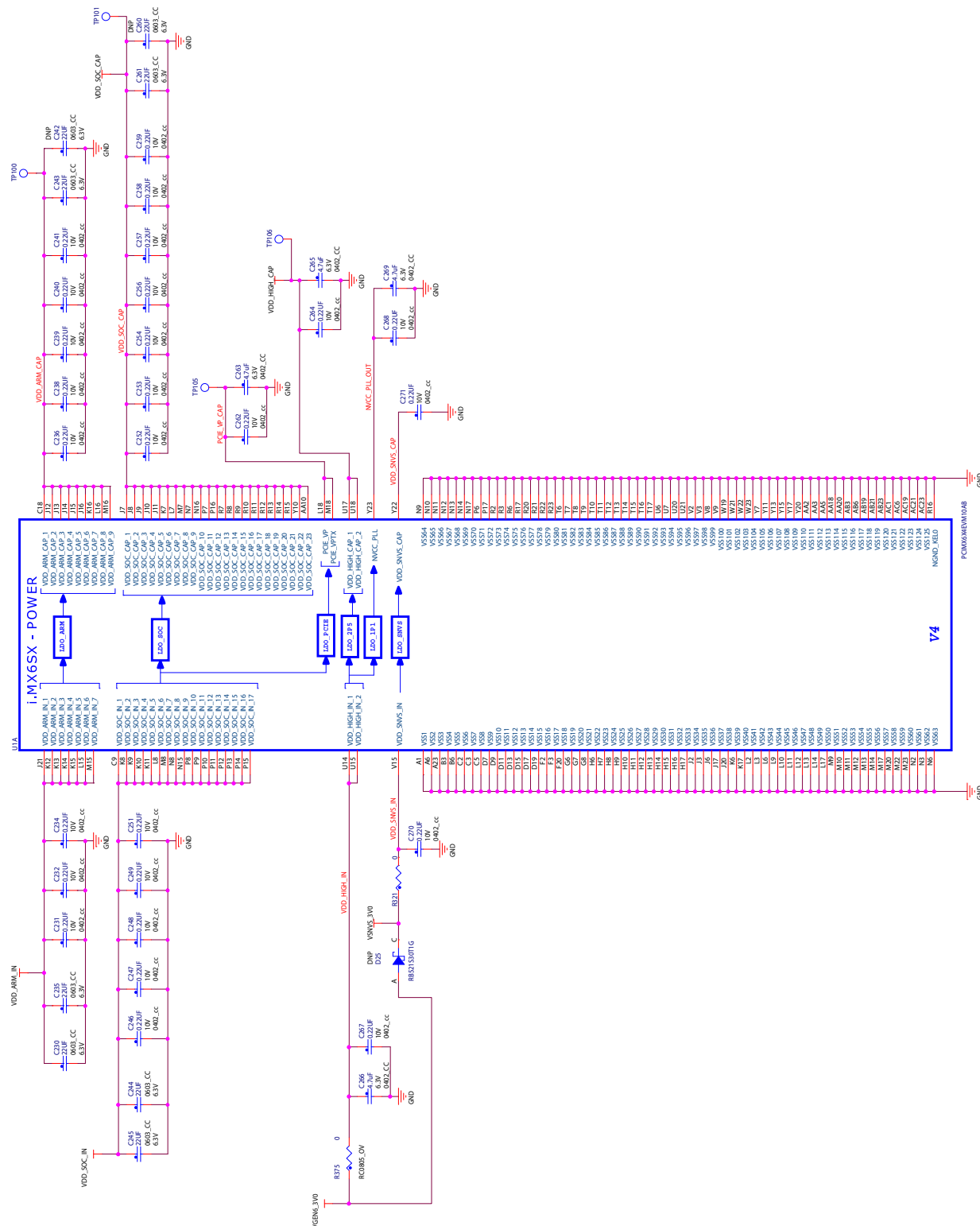


Figure 5. Schematic part 3



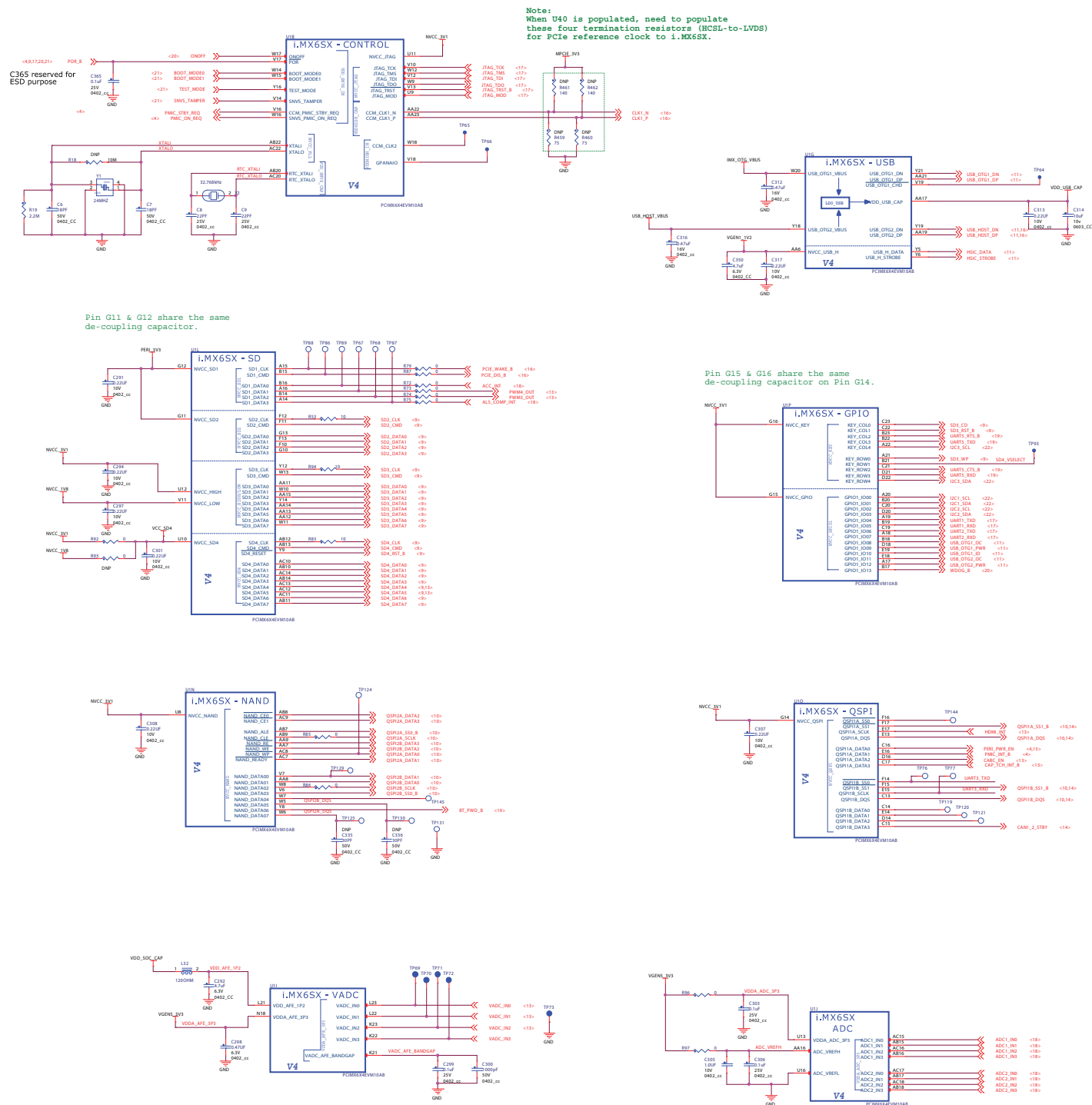
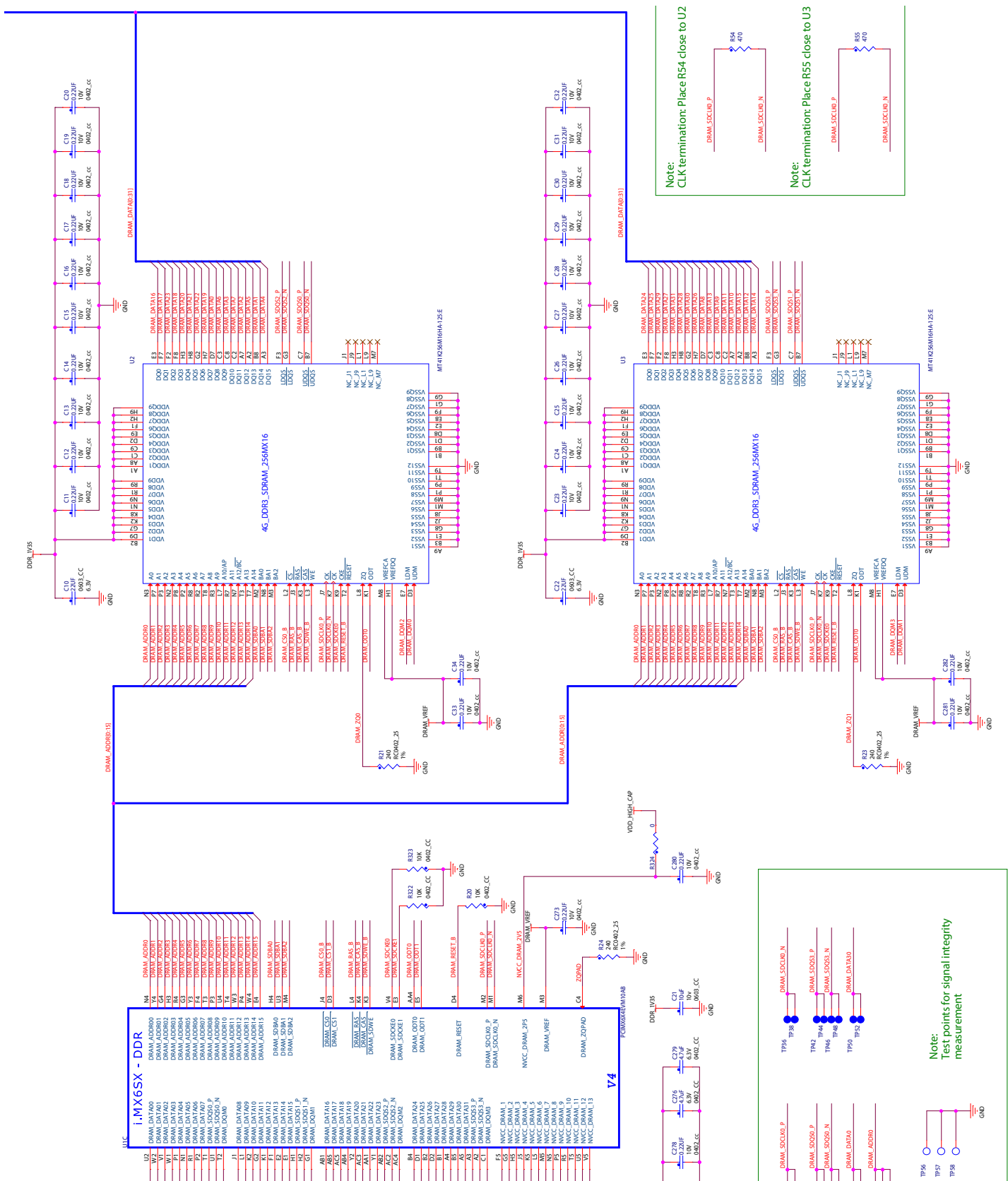


Figure 7. Schematic part 5

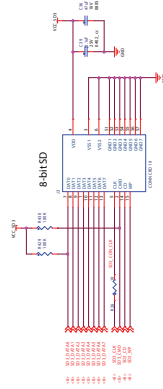


Figure 8. Schematic part 6

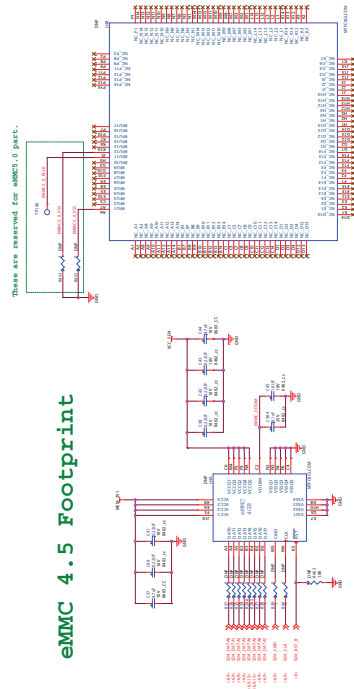


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SD3 - For Primary External Card Slot (SD3.0)

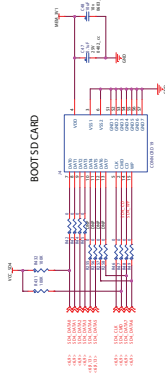


eMMC 4.5 Footprint



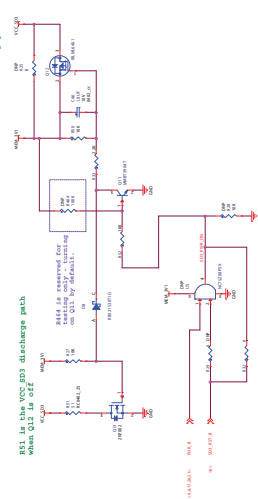
SD4 - For Boot Code

8-bit SD Card on SD4 slot
eMMC on SD4 is used as boot device



Power switch circuit for External SD Card (SD3)

Remove R11 when SD3 is populated.



SD2 - for WiFi and SD Accessories

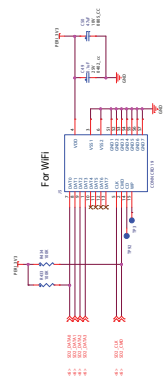


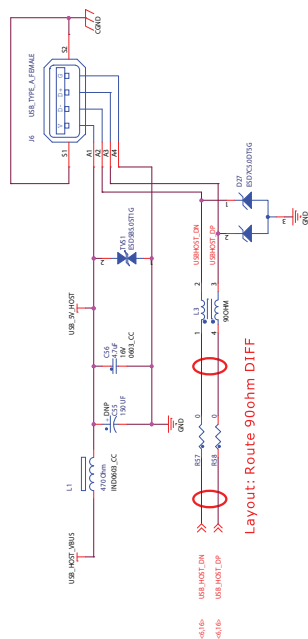
Figure 10. Schematic part 8

The image displays two circuit diagrams for connecting an N25Q256A13EF840 SPI flash memory to an NXP i.MX6UL microcontroller. The top diagram shows the connection to the QSPI2_A interface, and the bottom diagram shows the connection to the QSPI2_B interface. Both diagrams include the microcontroller, the flash memory, and various passive components like resistors and capacitors.

Top Diagram (QSPI2_A Interface):

- Microcontroller (U7):** NXP i.MX6UL, pins 5 (DQ0), 6 (DQ1), 7 (DQ2), 8 (DQ3), 9 (DQ4), 10 (DQ5), 11 (DQ6), 12 (DQ7), 13 (DQ8), 14 (DQ9), 15 (DQ10), 16 (DQ11), 17 (DQ12), 18 (DQ13), 19 (DQ14), 20 (DQ15), 21 (DQ16), 22 (DQ17), 23 (DQ18), 24 (DQ19), 25 (DQ20), 26 (DQ21), 27 (DQ22), 28 (DQ23), 29 (DQ24), 30 (DQ25), 31 (DQ26), 32 (DQ27), 33 (DQ28), 34 (DQ29), 35 (DQ30), 36 (DQ31), 37 (DQ32), 38 (DQ33), 39 (DQ34), 40 (DQ35), 41 (DQ36), 42 (DQ37), 43 (DQ38), 44 (DQ39), 45 (DQ40), 46 (DQ41), 47 (DQ42), 48 (DQ43), 49 (DQ44), 50 (DQ45), 51 (DQ46), 52 (DQ47), 53 (DQ48), 54 (DQ49), 55 (DQ50), 56 (DQ51), 57 (DQ52), 58 (DQ53), 59 (DQ54), 60 (DQ55), 61 (DQ56), 62 (DQ57), 63 (DQ58), 64 (DQ59), 65 (DQ60), 66 (DQ61), 67 (DQ62), 68 (DQ63), 69 (DQ64), 70 (DQ65), 71 (DQ66), 72 (DQ67), 73 (DQ68), 74 (DQ69), 75 (DQ70), 76 (DQ71), 77 (DQ72), 78 (DQ73), 79 (DQ74), 80 (DQ75), 81 (DQ76), 82 (DQ77), 83 (DQ78), 84 (DQ79), 85 (DQ80), 86 (DQ81), 87 (DQ82), 88 (DQ83), 89 (DQ84), 90 (DQ85), 91 (DQ86), 92 (DQ87), 93 (DQ88), 94 (DQ89), 95 (DQ90), 96 (DQ91), 97 (DQ92), 98 (DQ93), 99 (DQ94), 100 (DQ95), 101 (DQ96), 102 (DQ97), 103 (DQ98), 104 (DQ99), 105 (DQ100), 106 (DQ101), 107 (DQ102), 108 (DQ103), 109 (DQ104), 110 (DQ105), 111 (DQ106), 112 (DQ107), 113 (DQ108), 114 (DQ109), 115 (DQ110), 116 (DQ111), 117 (DQ112), 118 (DQ113), 119 (DQ114), 120 (DQ115), 121 (DQ116), 122 (DQ117), 123 (DQ118), 124 (DQ119), 125 (DQ120), 126 (DQ121), 127 (DQ122), 128 (DQ123), 129 (DQ124), 130 (DQ125), 131 (DQ126), 132 (DQ127), 133 (DQ128), 134 (DQ129), 135 (DQ130), 136 (DQ131), 137 (DQ132), 138 (DQ133), 139 (DQ134), 140 (DQ135), 141 (DQ136), 142 (DQ137), 143 (DQ138), 144 (DQ139), 145 (DQ140), 146 (DQ141), 147 (DQ142), 148 (DQ143), 149 (DQ144), 150 (DQ145), 151 (DQ146), 152 (DQ147), 153 (DQ148), 154 (DQ149), 155 (DQ150), 156 (DQ151), 157 (DQ152), 158 (DQ153), 159 (DQ154), 160 (DQ155), 161 (DQ156), 162 (DQ157), 163 (DQ158), 164 (DQ159), 165 (DQ160), 166 (DQ161), 167 (DQ162), 168 (DQ163), 169 (DQ164), 170 (DQ165), 171 (DQ166), 172 (DQ167), 173 (DQ168), 174 (DQ169), 175 (DQ170), 176 (DQ171), 177 (DQ172), 178 (DQ173), 179 (DQ174), 180 (DQ175), 181 (DQ176), 182 (DQ177), 183 (DQ178), 184 (DQ179), 185 (DQ180), 186 (DQ181), 187 (DQ182), 188 (DQ183), 189 (DQ184), 190 (DQ185), 191 (DQ186), 192 (DQ187), 193 (DQ188), 194 (DQ189), 195 (DQ190), 196 (DQ191), 197 (DQ192), 198 (DQ193), 199 (DQ194), 200 (DQ195), 201 (DQ196), 202 (DQ197), 203 (DQ198), 204 (DQ199), 205 (DQ200), 206 (DQ201), 207 (DQ202), 208 (DQ203), 209 (DQ204), 210 (DQ205), 211 (DQ206), 212 (DQ207), 213 (DQ208), 214 (DQ209), 215 (DQ210), 216 (DQ211), 217 (DQ212), 218 (DQ213), 219 (DQ214), 220 (DQ215), 221 (DQ216), 222 (DQ217), 223 (DQ218), 224 (DQ219), 225 (DQ220), 226 (DQ221), 227 (DQ222), 228 (DQ223), 229 (DQ224), 230 (DQ225), 231 (DQ226), 232 (DQ227), 233 (DQ228), 234 (DQ229), 235 (DQ230), 236 (DQ231), 237 (DQ232), 238 (DQ233), 239 (DQ234), 240 (DQ235), 241 (DQ236), 242 (DQ237), 243 (DQ238), 244 (DQ239), 245 (DQ240), 246 (DQ241), 247 (DQ242), 248 (DQ243), 249 (DQ244), 250 (DQ245), 251 (DQ246), 252 (DQ247), 253 (DQ248), 254 (DQ249), 255 (DQ250), 256 (DQ251), 257 (DQ252), 258 (DQ253), 259 (DQ254), 260 (DQ255), 261 (DQ256), 262 (DQ257), 263 (DQ258), 264 (DQ259), 265 (DQ260), 266 (DQ261), 267 (DQ262), 268 (DQ263), 269 (DQ264), 270 (DQ265), 271 (DQ266), 272 (DQ267), 273 (DQ268), 274 (DQ269), 275 (DQ270), 276 (DQ271), 277 (DQ272), 278 (DQ273), 279 (DQ274), 280 (DQ275), 281 (DQ276), 282 (DQ277), 283 (DQ278), 284 (DQ279), 285 (DQ280), 286 (DQ281), 287 (DQ282), 288 (DQ283), 289 (DQ284), 290 (DQ285), 291 (DQ286), 292 (DQ287), 293 (DQ288), 294 (DQ289), 295 (DQ290), 296 (DQ291), 297 (DQ292), 298 (DQ293), 299 (DQ294), 300 (DQ295), 301 (DQ296), 302 (DQ297), 303 (DQ298), 304 (DQ299), 305 (DQ300), 306 (DQ301), 307 (DQ302), 308 (DQ303), 309 (DQ304), 310 (DQ305), 311 (DQ306), 312 (DQ307), 313 (DQ308), 314 (DQ309), 315 (DQ310), 316 (DQ311), 317 (DQ312), 318 (DQ313), 319 (DQ314), 320 (DQ315), 321 (DQ316), 322 (DQ317), 323 (DQ318), 324 (DQ319), 325 (DQ320), 326 (DQ321), 327 (DQ322), 328 (DQ323), 329 (DQ324), 330 (DQ325), 331 (DQ326), 332 (DQ327), 333 (DQ328), 334 (DQ329), 335 (DQ330), 336 (DQ331), 337 (DQ332), 338 (DQ333), 339 (DQ334), 340 (DQ335), 341 (DQ336), 342 (DQ337), 343 (DQ338), 344 (DQ339), 345 (DQ340), 346 (DQ341), 347 (DQ342), 348 (DQ343), 349 (DQ344), 350 (DQ345), 351 (DQ346), 352 (DQ347), 353 (DQ348), 354 (DQ349), 355 (DQ350), 356 (DQ351), 357 (DQ352), 358 (DQ353), 359 (DQ354), 360 (DQ355), 361 (DQ356), 362 (DQ357), 363 (DQ358), 364 (DQ359), 365 (DQ360), 366 (DQ361), 367 (DQ362), 368 (DQ363), 369 (DQ364), 370 (DQ365), 371 (DQ366), 372 (DQ367), 373 (DQ368), 374 (DQ369), 375 (D

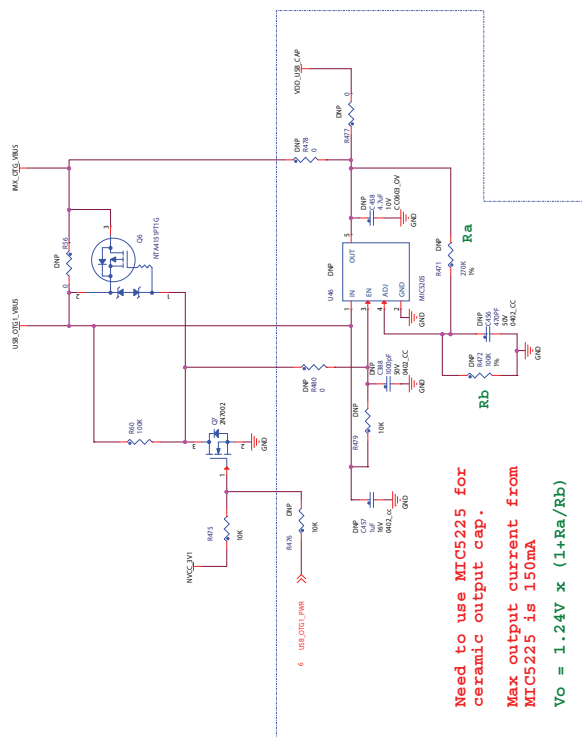
USB Host Port



Need to use MIC5225 for ceramic output cap.

Max output current from MIC5225 is 150mA

$V_o = 1.24V \times (1 + R_a/R_b)$



This block is reserved for USB OTG certification test.

Figure 12. Schematic part 10

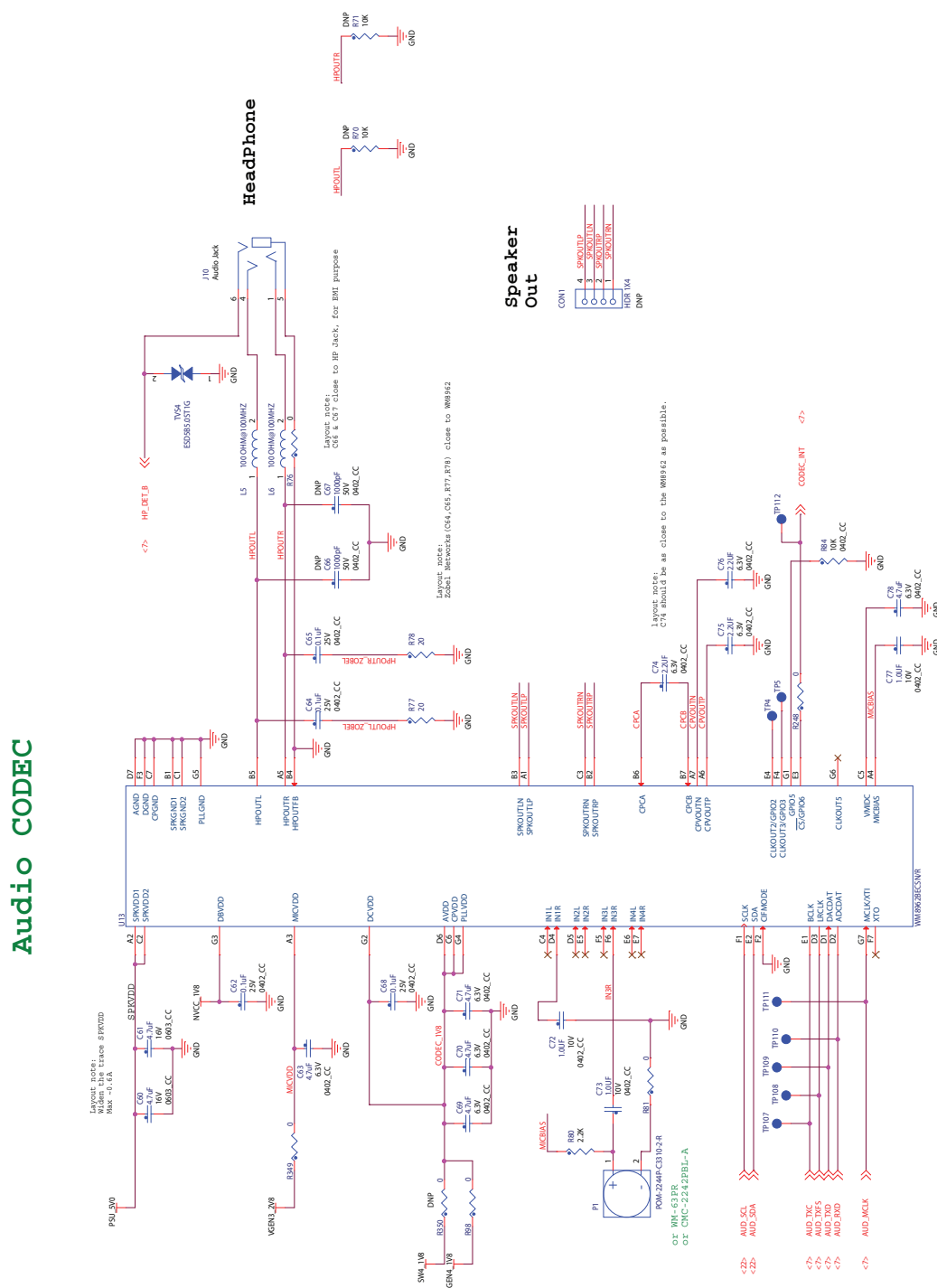


Figure 13. Schematic part 11



One of these two peripherals MUST BE REMOVED when a developer wishes to use the other.

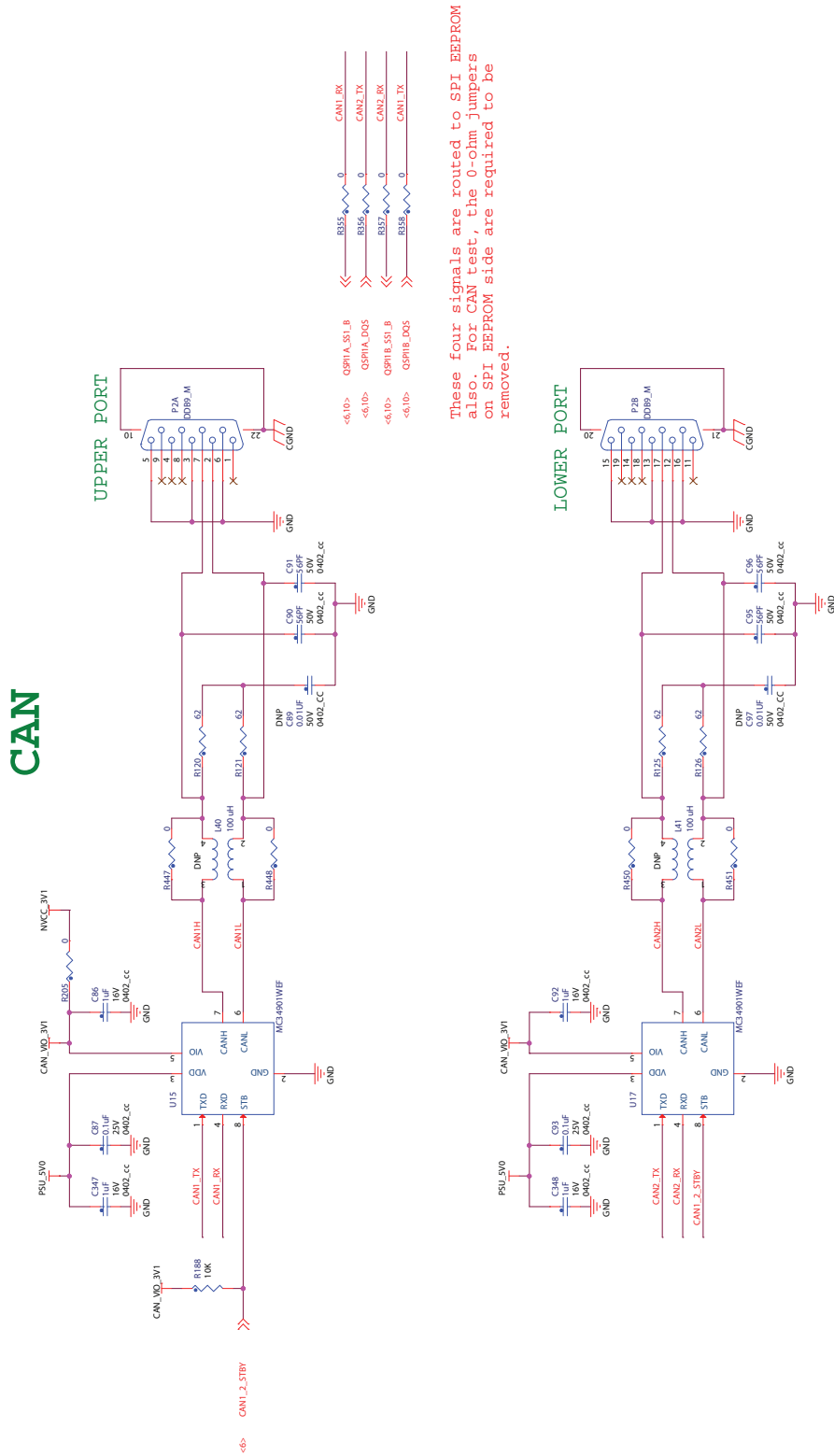


Figure 15. Schematic part 13



Mini-PCIE

Note:
All components in this block are needed
to be populated for PCIe GEN2 clock jitter test.

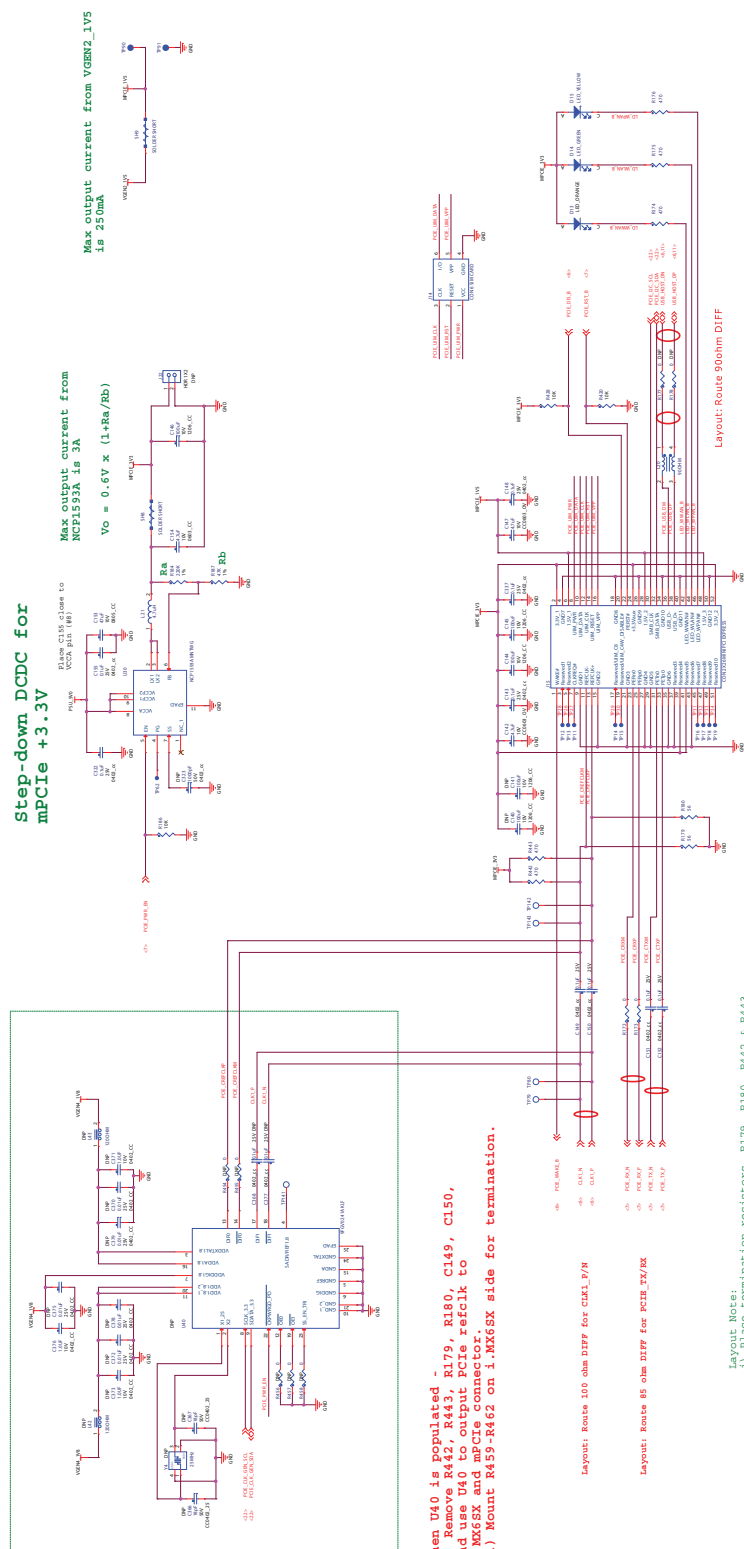


Figure 17. Schematic part 15

Debug UART to USB Converter

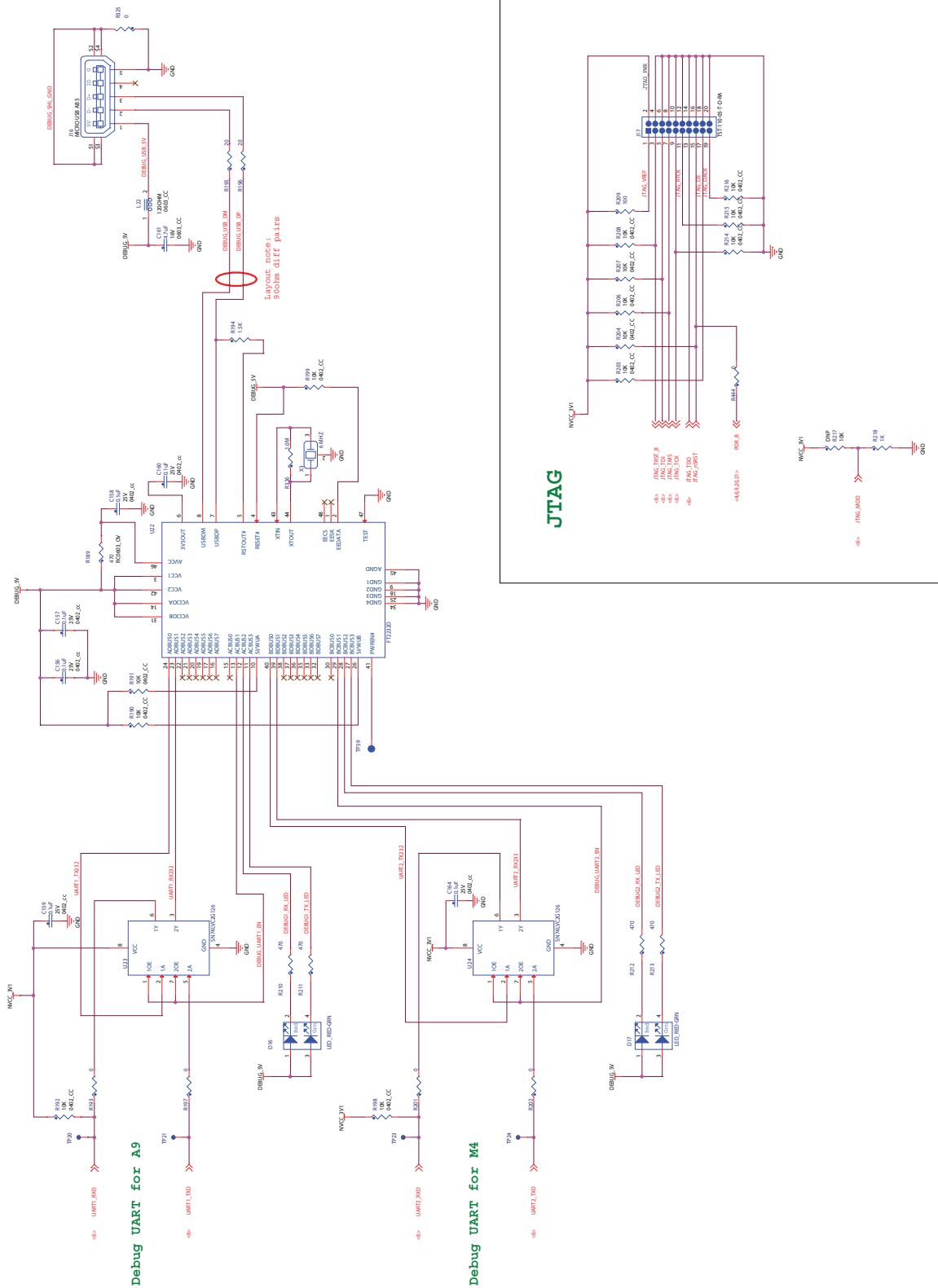


Figure 18. Schematic part 16

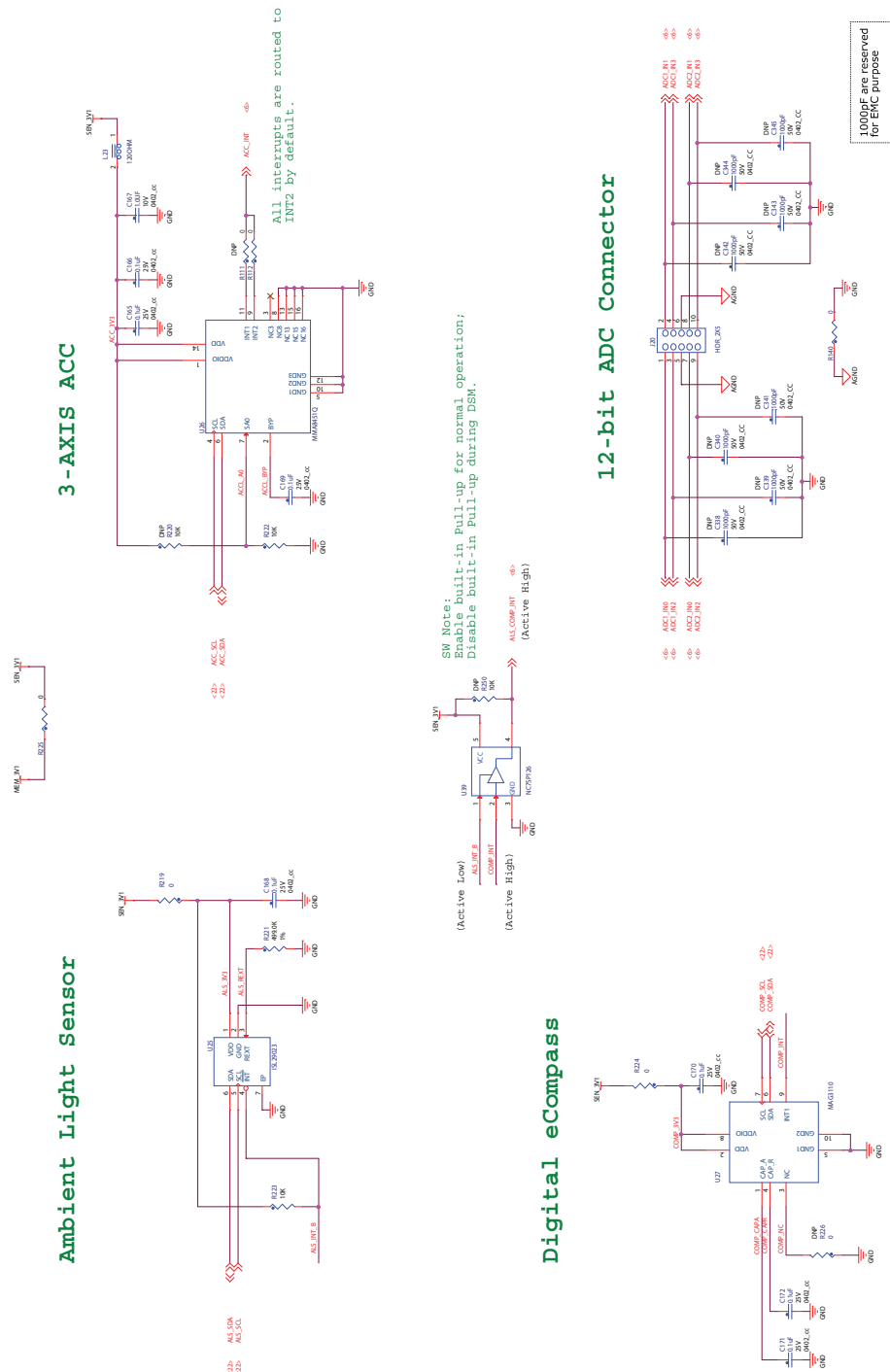


Figure 19. Schematic part 17

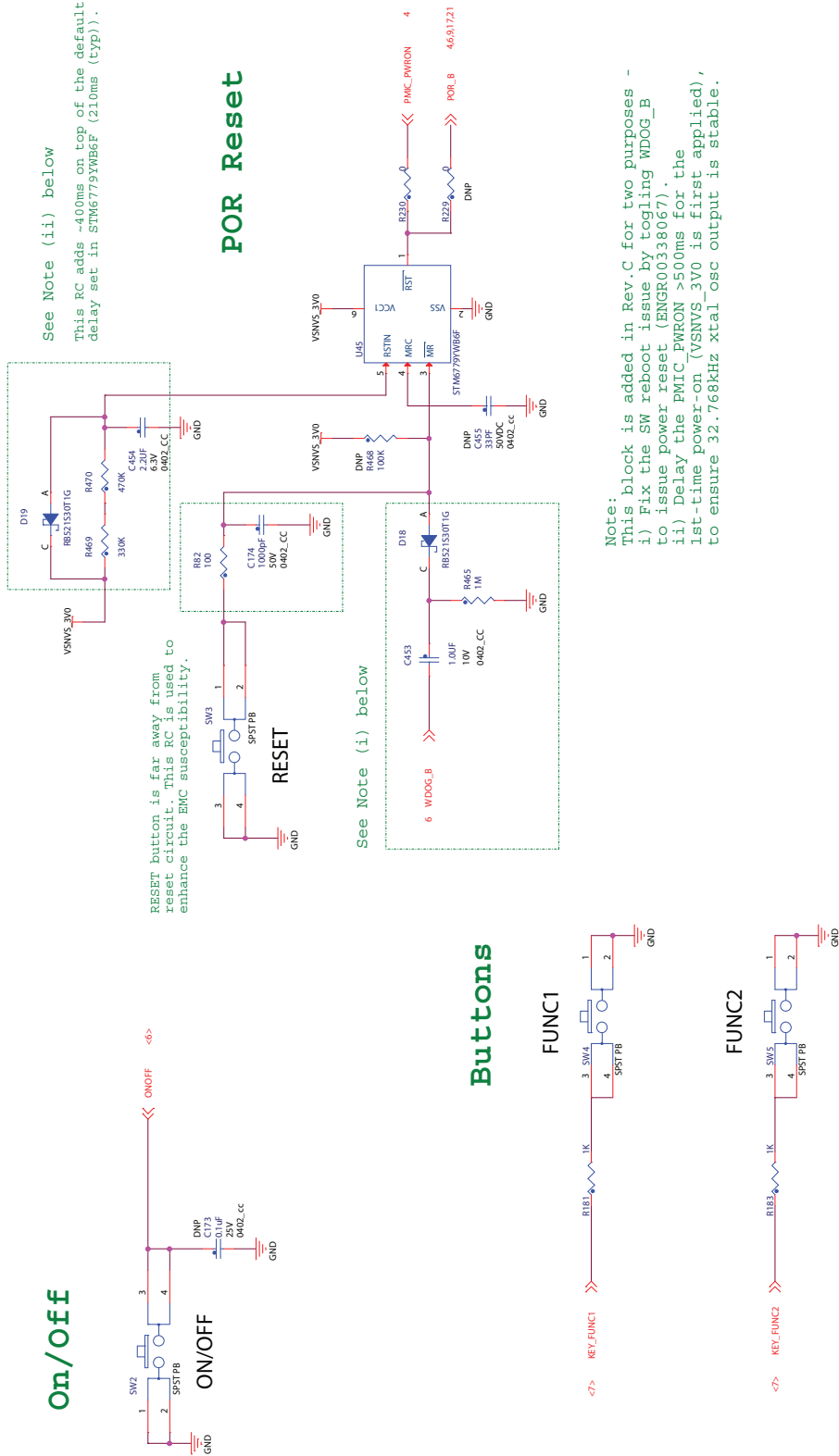
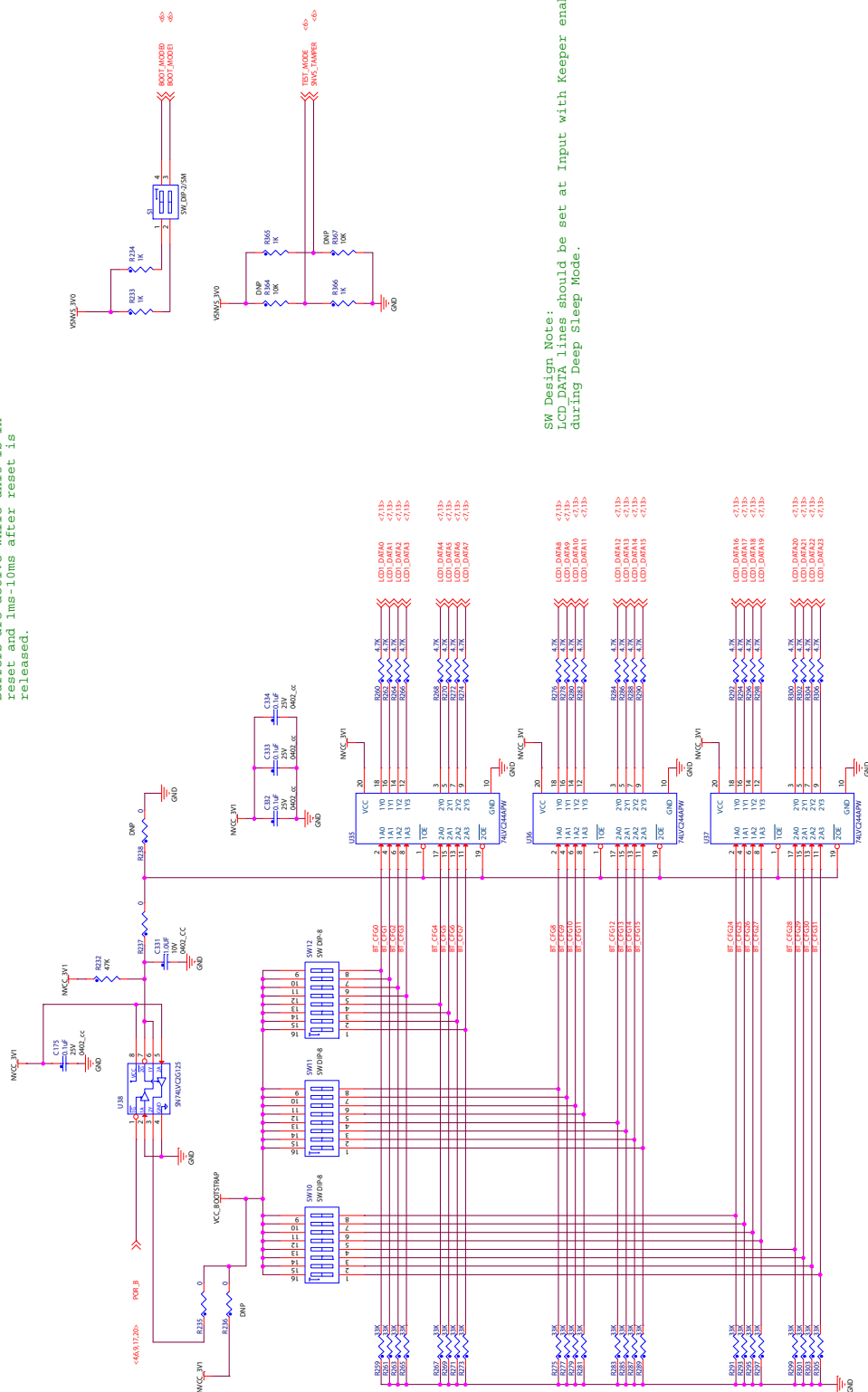


Figure 21. Schematic part 19

Note:
i.MX6SX reads values approximately 300µs to 1ms after reset released. Buffers are active while unit is in reset and 1ms-10ms after reset is released.



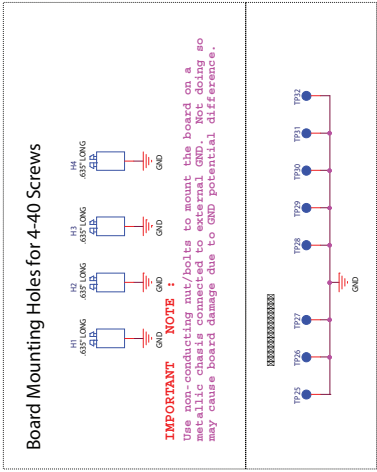
SW Design Note:
LCD_DATA lines should be set at Input with Keeper enable during Deep Sleep Mode.

Note:
i) SW10 settings are all "0".
ii) BT_CFG1 must be "1" for SD3 operation on SDB, as it has a power switch control for VCC_SD3.

BOOT MODE

1	2	3	4	5	6	7	8
BT_CFG7	BT_CFG6	BT_CFG5	BT_CFG4	BT_CFG3	BT_CFG2	BT_CFG1	BT_CFG0
0001 = QSP1 Boot	000	000	000	00000000	00000000	00000000	00000000
010 = SD/eSD Boot	0 = Regular	00 = Normal (3.3V)	0 = No PWR	0 = 1-bit	01 = eSDHC1	10 = eSDHC2	11 = eSDHC3
1 = Fast	1 = Enable PWR Cycle	01 = High (3.3V)	1 = Enable PWR Cycle	1 = 4-bit	10 = eSDHC2	11 = eSDHC3	11 = eSDHC3
0	0	0	0	0	0	0	0

Figure 22. Schematic part 20



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8 References

Following are URLs where you can obtain information on related NXP products and application solutions:

Support pages	Description	URL
i.MX 6SX	Product Summary Page	http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=i.MX6SX
PF3000	Product Summary Page	http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=PF3000
PF3000 Layout Guidelines	Application Note	http://www.nxp.com/files/analog/doc/app_note/AN5094.pdf
NXP Community	Support Site	https://community.nxp.com/docs/DOC-105064

9 Revision history

Revision	Date	Description
1.0	7/2015	• Initial release
	7/2016	• Updated to NXP document form and style

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