Sheet: STPMIC1_Board

File: STPMIC1_Board.sch

Sheet: PF3000_Board

File: PF3000_Board.sch

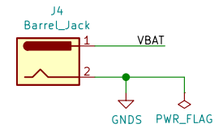
Chris Sutton

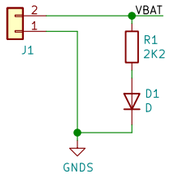
Sheet: /
File: STPMIC1_MC32PF3000_Board.sch

Title: System Overview

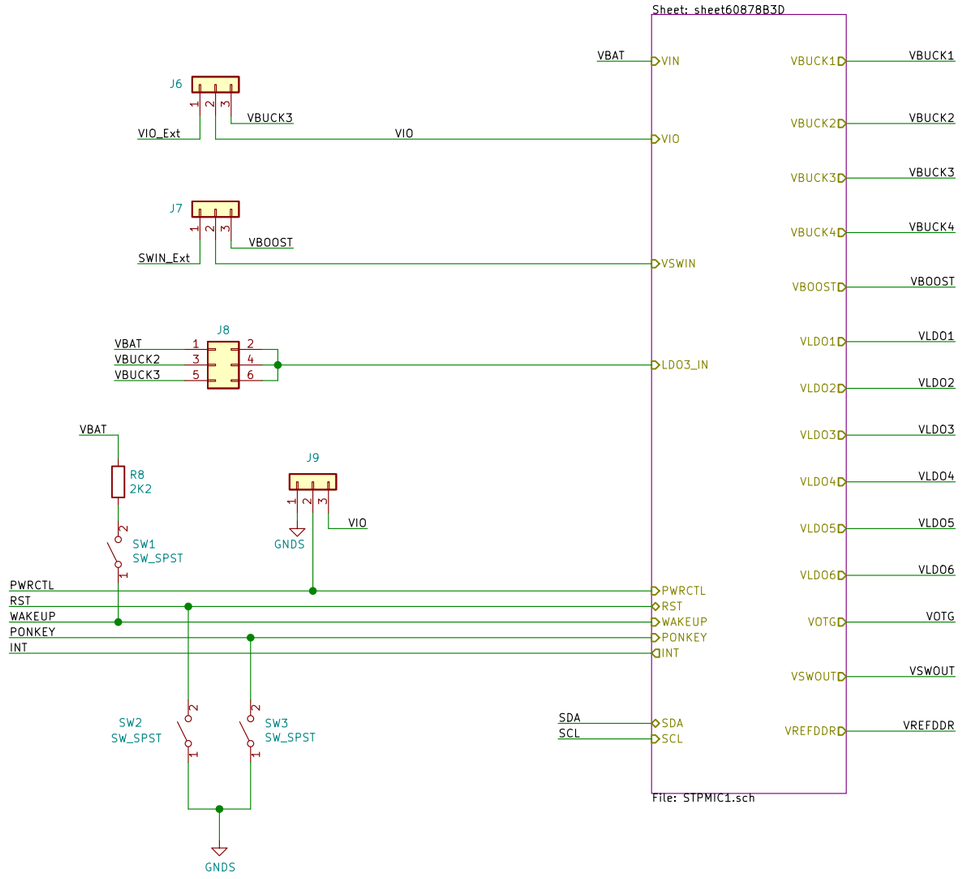
Size: A3	Date: 2021-03-02	**Rev: A**
KiCad E.D.A. kicad (5.1.8-0-10_14)		Id: 1/5

POWER INPUT

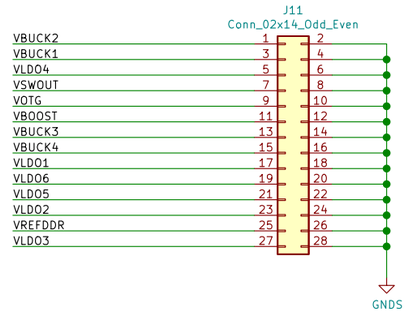




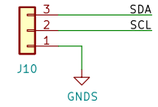
POWER MANAGEMENT IC



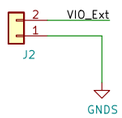
POWER OUTPUT

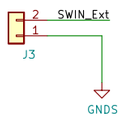


DEBUG OUTPUT

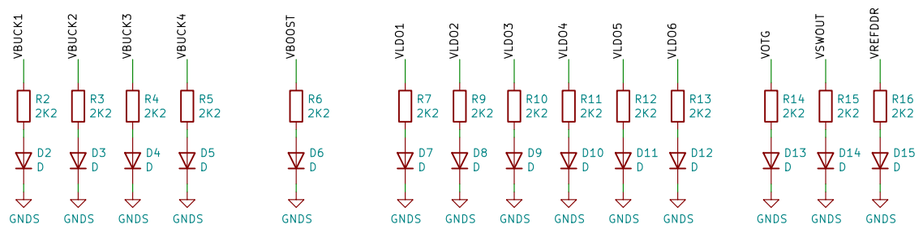


SUBSYSTEM JUMPERS

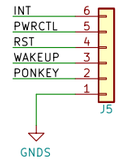




OUTPUT POWER INDICATORS



DIAGNOSTICS OUTPUT



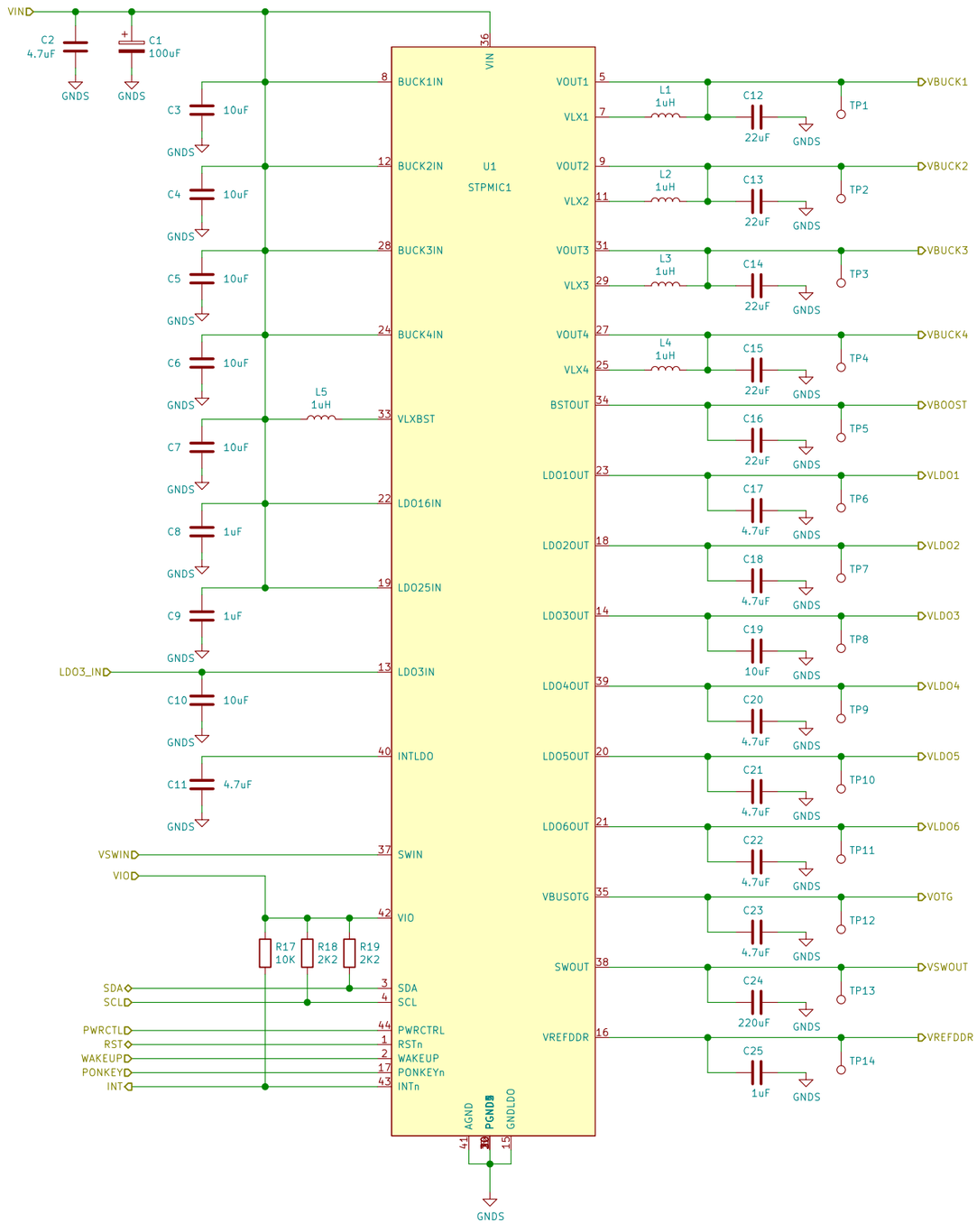
Development connections for STPMIC1

Chris Sutton

Sheet: /STPMIC1_Board/
File: STPMIC1_Board.sch

Title: STPMIC1 DEV

Size: A3	Date: 2021-03-02	**Rev: A**
KiCad E.D.A. kicad (5.1.8-0-10_14)		Id: 2/5



Minimum connections for STPMIC1

Chris Sutton

Sheet: /STPMIC1_Board/sheet60878B3D/
File: STPMIC1.sch

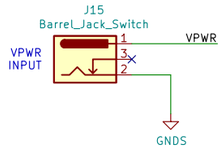
Title: STPMIC1 MAIN

Size: A3	Date: 2021-03-02	**Rev: A**
KiCad E.D.A. kicad (5.1.8-0-10_14)		Id: 3/5

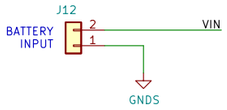
POWER INPUT

3.7 V to 5.5 V Supply input (Default).

Shorts VPWR to ground when not used (pin 3–2)

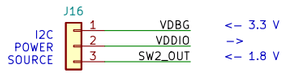


3.1 V to 4.5 V Supply input for batteries

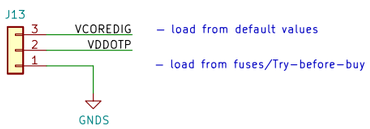


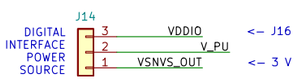
SUBSYSTEM POWER JUMPERS

Ensure that VDDIO is always lesser than or equal to VIN

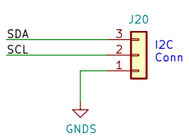


Supply to program OTP fuses. Connect VDDOTP to GND during normal application

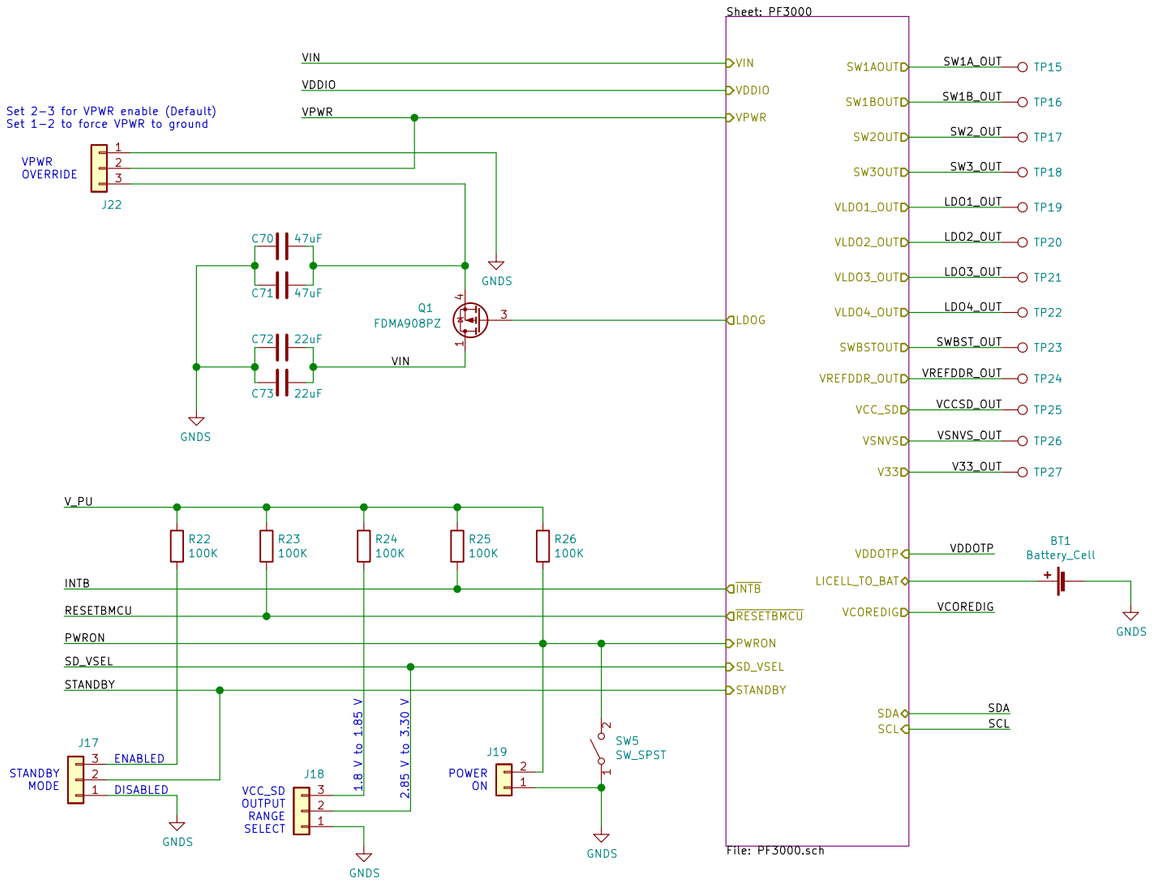




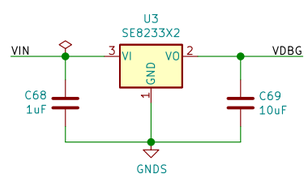
DEBUG OUTPUT CONNECTOR



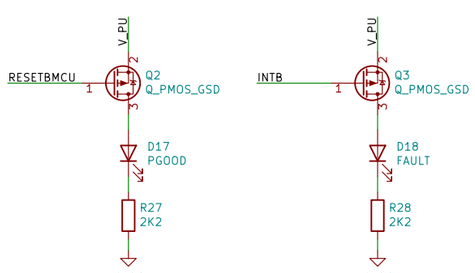
POWER MANAGEMENT IC



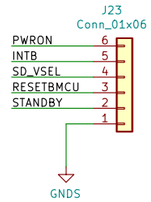
VDBG LDO



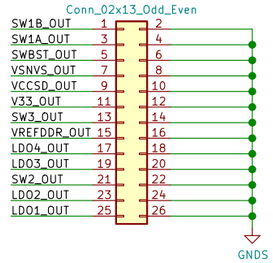
SYSTEM STATUS INDICATORS

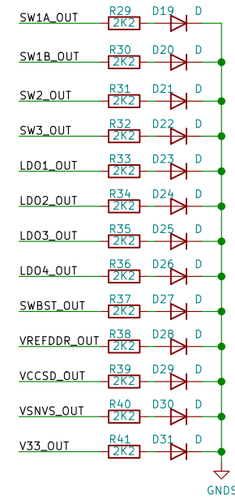


DIAGNOSTICS OUTPUT CONNECTOR



POWER OUTPUT CONNECTOR





Development connections for PF3000

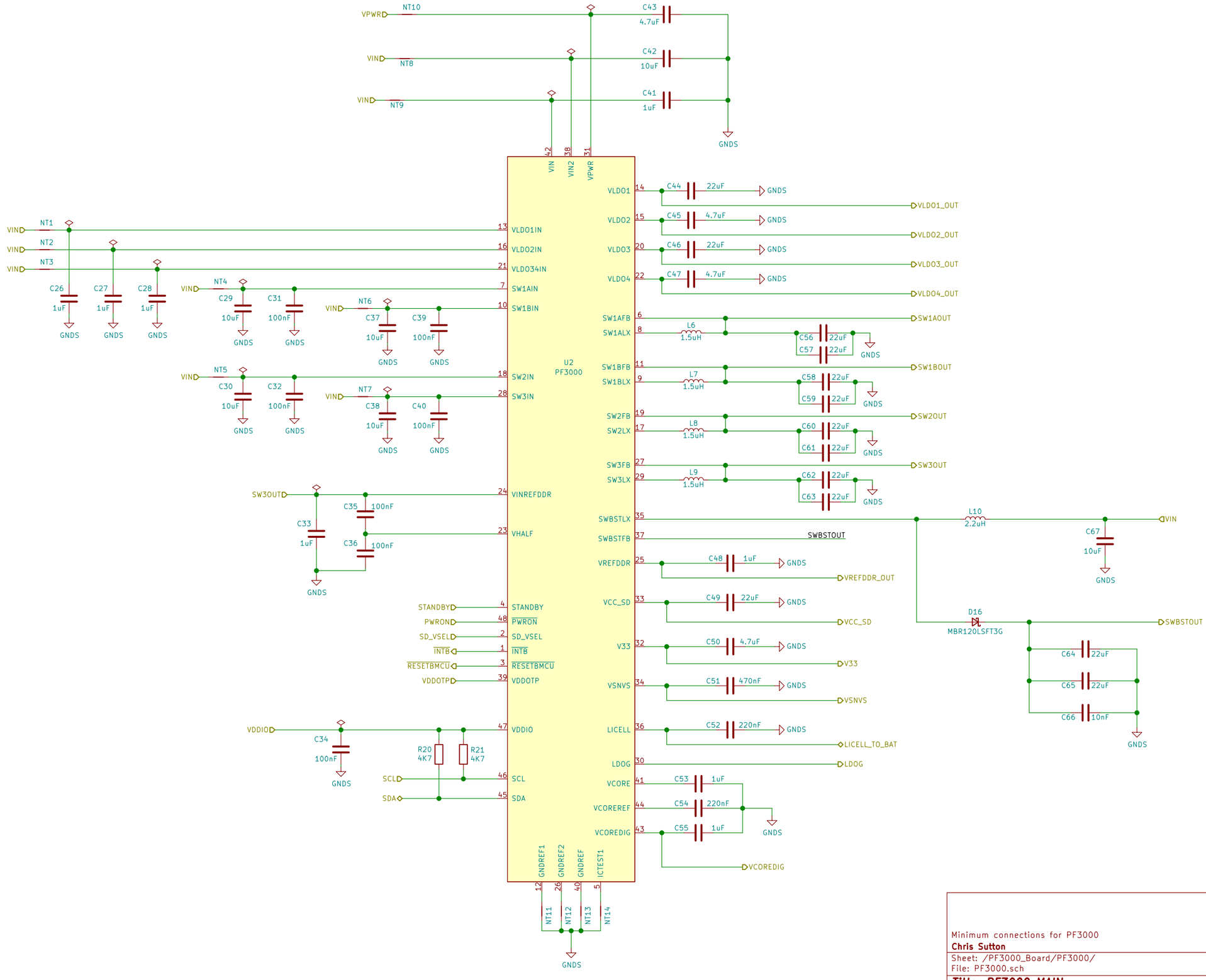
Chris Sutton

Sheet: /PF3000_Board/

File: PF3000_Board.sch

Title: PF3000 DEV

Size: A3	Date: 2021–03–02	**Rev: A**
KiCad E.D.A. kicad (5.1.8–0–10_14)		Id: 4/5


VPWR
NT10
C43
4.7uF
VIN
NT8
C42
10uF
VIN
NT9
C41
1uF
GNDS
VIN
VIN2
VPWR
U2
PF3000
VLDO1IN
VLDO2IN
VLDO34IN
SW1AIN
SW1BIN
SW2IN
SW3IN
VINREFDDR
VHALF
STANDBY
PWRON
SD_VSEL
INTB
RESETBMCU
VDDOTP
VDDIO
SCL
SDA
GNDREF1
GNDREF2
GNDREF
ICTEST1
VLDO1
VLDO2
VLDO3
VLDO4
SW1AFB
SW1ALX
SW1BFB
SW1BLX
SW2FB
SW2LX
SW3FB
SW3LX
SWBSTLX
SWBSTFB
VREFDDR
VCC_SD
V33
VSNVS
LICELL
LDOG
VCORE
VCOREREF
VCOREDIG
VLDO1_OUT
VLDO2_OUT
VLDO3_OUT
VLDO4_OUT
SW1AOUT
SW1BOUT
SW2OUT
SW3OUT
SWBSTOUT
VREFDDR_OUT
VCC_SD
V33
VSNVS
LICELL_TO_BAT
LDOG
VCOREDIG
VIN
SWBSTOUT
C44 22uF
C45 4.7uF
C46 22uF
C47 4.7uF
L6 1.5uH
L7 1.5uH
L8 1.5uH
L9 1.5uH
L10 2.2uH
D16 MBR120LSFT3G
C48 1uF
C49 22uF
C50 4.7uF
C51 470nF
C52 220nF
C53 1uF
C54 220nF
C55 1uF
C56 22uF
C57 22uF
C58 22uF
C59 22uF
C60 22uF
C61 22uF
C62 22uF
C63 22uF
C64 22uF
C65 22uF
C66 10nF
C67 10uF
C26 1uF
C27 1uF
C28 1uF
C29 10uF
C31 100nF
C37 10uF
C39 100nF
C30 10uF
C32 100nF
C38 10uF
C40 100nF
C33 1uF
C35 100nF
C36 100nF
C34 100nF
R20 4K7
R21 4K7
NT1
NT2
NT3
NT4
NT5
NT6
NT7
NT11
NT12
NT13
NT14
Minimum connections for PF3000
Chris Sutton
Sheet: /PF3000_Board/PF3000/
File: PF3000.sch
Title: PF3000 MAIN
Size: A3
Date: 2021-03-02
Rev: A
KiCad E.D.A. kicad (5.1.8-0-10_14)
Id: 5/5