NXP Semiconductors
Application Note

Document Number: AN5094
Rev. 2.0, 7/2016

PF3000 layout guidelines

1 Introduction

This document provides the best practices for the layout of the PF3000 device on printed circuit boards.

The PF3000 is a SMARTMOS Power Management Integrated Circuit (PMIC) designed specifically for use with the NXP i.MX 7 and i.MX 6 DL/SL/SX application processors.

2 Packaging

The PF3000 device is intended for use in consumer and industrial applications and is offered in a standard 48 QFN with an area of 7.0 mm x 7.0 mm. Refer to Table 1. for the package drawing information for both packages.

Refer to Application Note AN1902 for guidelines on the handling and assembly of NXP QFN packages during PCB assembly, guidelines for PCB design and rework, and package performance information (such as Moisture Sensitivity Level (MSL) rating, board level reliability, mechanical, and thermal resistance data).

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.freescale.com and perform a keyword search for the drawing's document number.

See the Thermal Characteristics section for specific thermal characteristics for each package.

Table 1. Package drawing information

Package	Suffix	Package outline drawing number
48-pin QFN 7X7 mm - 0.5mm pitch	EP	98ASA00719D

Contents

3 Recommended layer stack

Table 2. and Table 3. shows the recommended layer stack-up for the signals to receive best shielding.

Table 2. Four layer stack-up recommendation

Layer	Stack-up
Layer 1 (Top)	High di/dt nodes
Layer 2 (Inner 1)	GND
Layer 3 (Inner 2)	Small signal/Power
Layer 4 (Bottom)	Small signal/GND

Table 3. Six layer stack-up recommendation

Layer	Stack-up
Layer 1 (Top)	High di/dt nodes
Layer 2 (Inner 1)	GND
Layer 3 (Inner 2)	Small signal/Power
Layer 4 (Inner 3)	Small signal/Power
Layer 5 (Inner 4)	GND
Layer 6 (Bottom)	High di/dt nodes

It is highly recommended to place the ground layer between the high di/dt nodes layer and the sensitive small signal trace layer. This ground layer shields the small signal traces from switching traces and improves the stability and accuracy of the regulation.

Note: A more detailed layer design may be required to route the i.MX processor. If the PF3000 is being interfaced with an i.MX processor, just four of the layers are needed to route it.

4 Component placement hints

Place these components as close as possible to the IC in order of priority:

1. Input capacitor of the buck regulators (SW1A, SW1B, SW2, and SW3)
2. Output diode and output capacitor of the boost converter (SWBST)
3. VIN, VCOREREF, VCORE, and VCOREDIG capacitors
4. LICELL capacitor (if a coin cell is used in system)
5. VSNVS, VREFDDR, and linear regulators capacitors (VLDOx, VCC_SD and V33)
6. Switching regulator inductors

5 General routing guidelines

- Shield regulators feedback paths from noise planes and traces and connect them as close as possible to the load (ie. SW1AFB.)
- The exposed pad (EP) on the PF3000 is the high-current ground return for all the buck regulators and the boost regulator. Use vias under the EP to drop onto the ground plane(s) directly, ensuring sufficient copper for the ground return.
- The SWxIN, SWxLX, and SWBSTLX nodes are high dI/dt nodes and act as antennas. They are also high current paths. Hence their traces must be kept short and wide.
- Avoid coupling traces between sensitive signal/low noise supplies (like VCOREREF) and switching nodes.
- Power components should be all placed on the same side of board and their power traces routed on the same layer, In order to reduce voltage drop.
- If it is necessary to route a power trace to another layer, choose a trace in low di/dt paths (see Figure 2 and Figure 6) and use multiple vias for interconnection. - To minimize noise propagation and connection impedance between layers.

Minimize and isolate/shield the high dv/dt SW node areas. - To minimize the EMI noise source from the high dv/dt SW nodes

Separate input current paths among supplies if there is more than one supply on the same input rail (Figure 9) and the supplies are not synchronized. Have local input decoupling capacitor for each supply. - To avoid common impedance noise coupling among supplies.

6 I²C communication signals

To avoid contamination of these signals by nearby high power or high frequency signals, it is a good practice to shield them with ground planes placed on adjacent layers. Make sure the ground plane is uniform throughout the whole signal trace length

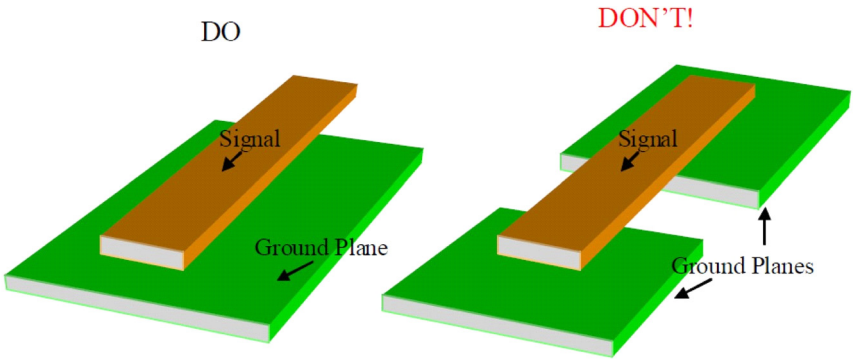

Figure 1. Recommended shielding for critical signals

7 Switching power supply traces

In the buck and boost configurations, length of the 'critical traces' must be kept minimal. 'Critical traces' refer to current paths which have high dI/dt. Refer to sections See Buck regulator on page 4 and See Boost converter on page 6 for details.

7.1 Buck regulator

Figure 2 shows current paths in a buck converter in the 'on' and 'off' periods of the switching cycle. Critical traces refer to traces which conduct either only during the 'on', or only during the 'off' periods, as highlighted in red.

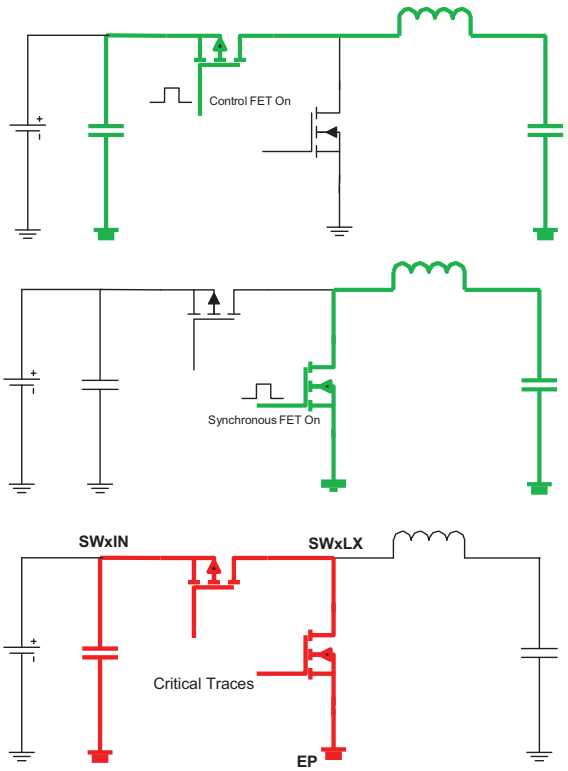

Figure 2. Buck converter critical traces

The top and bottom MOSFETs are integrated within the package in the buck regulators of the PF3000. Placement of the input capacitor close to the SWxIN pin and the exposed pad (EP) is critical. **Figure 4** and **Figure 5** show an example layout for the buck regulators.

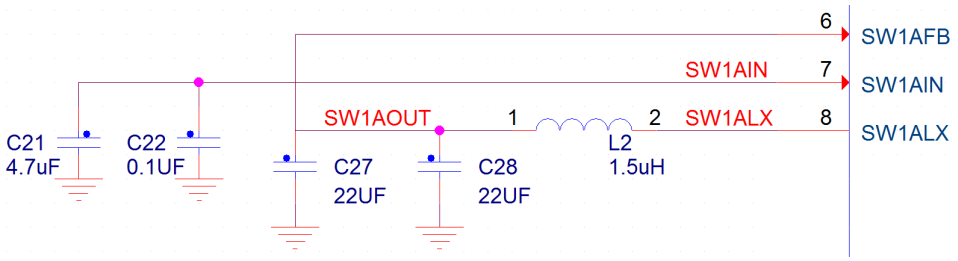

Figure 3. SW1A schematic - reference for Figure 4 and Figure 5

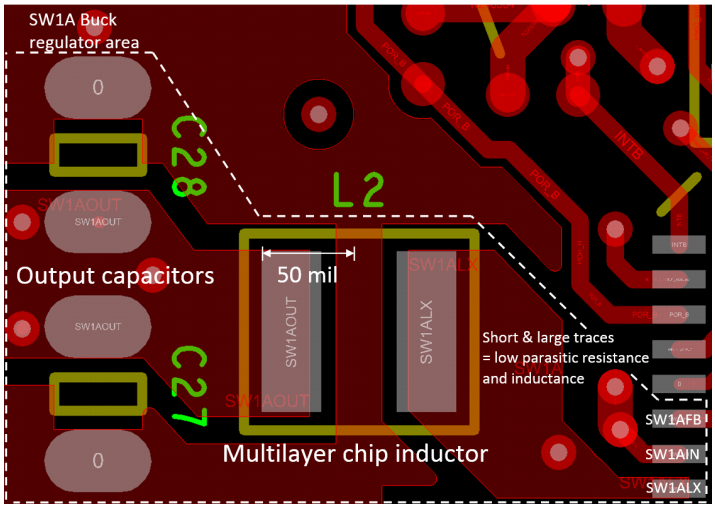

Figure 4. SW1A layout - top layer components + top silkscreen

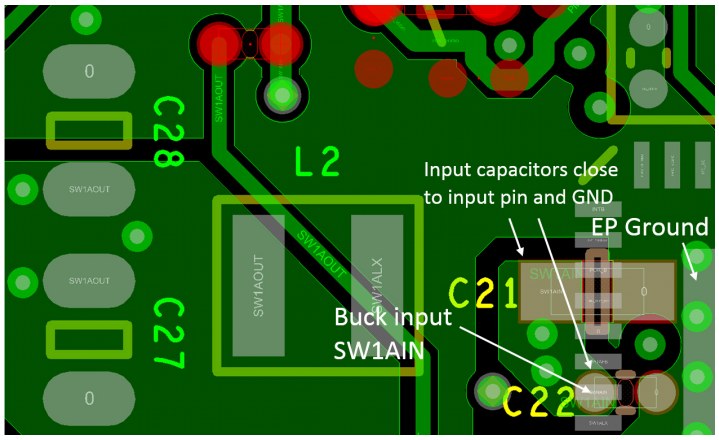

Figure 5. SW1A layout - top + bottom layer components and silkscreen

7.2 Boost converter

Figure 6 shows the critical traces in a boost converter.

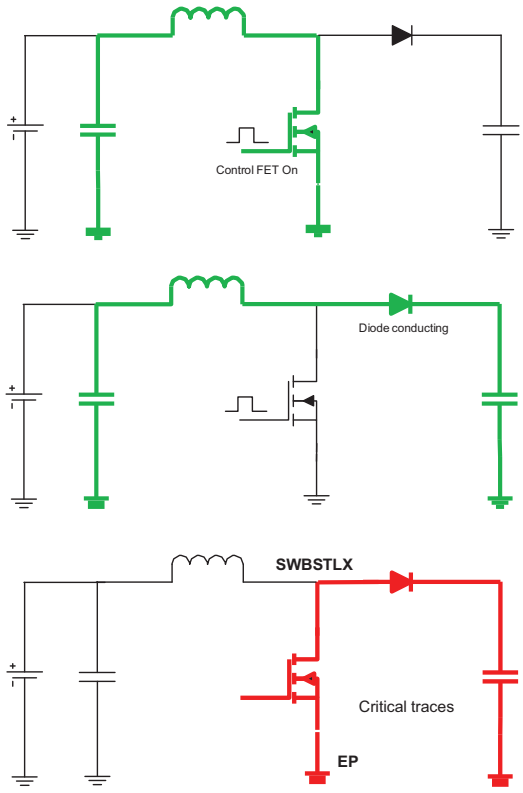

Figure 6. Boost converter critical traces

The switching MOSFET is integrated within the package in the SWBST regulator of the PF3000. The loop formed by the switching MOSFET, the diode, and the output capacitor, must be minimized to keep parasitic inductances small. **Figure 8** and **Figure 9** show an example of the SWBST layout.

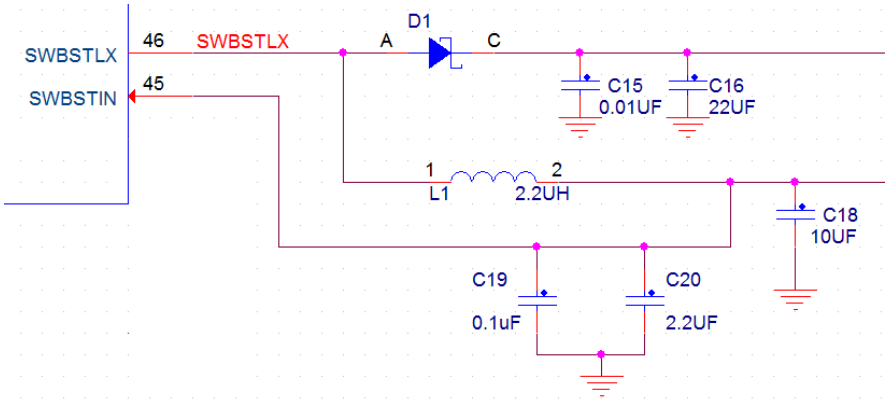

Figure 7. SWBST Schematic - Reference for Figure 8 and Figure 9

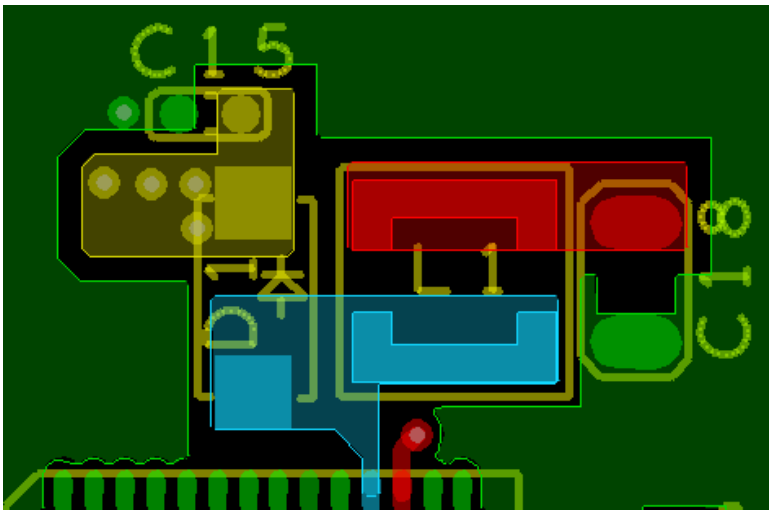

Figure 8. SWBST example layout. top layer components + top silkscreen

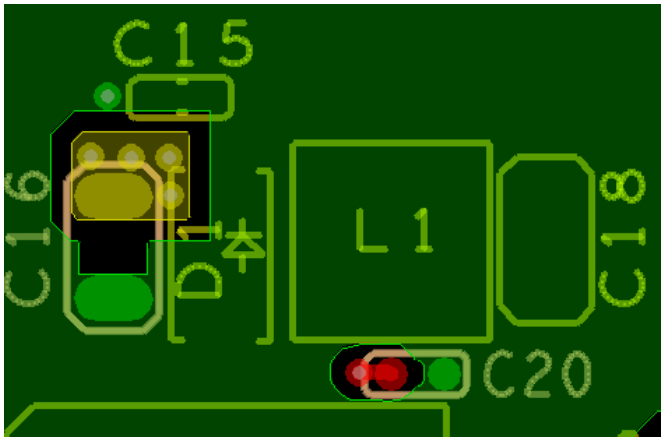

Figure 9. SWBST example layout. bottom layer components + top and bottom silkscreen

Observe that the critical traces (blue and yellow) are kept wide and short on the previous layout example. Notice the return current path is reduced by populating C16 on the bottom and with its negative terminal close to the EP ground plane. A sufficient number of vias is used when changing the high current path from top to bottom layer.

8 Effective grounding

- The practice of 'star grounding' must be followed for best performance of the PF3000.
- The exposed pad (EP) is the ground return for all the switching regulators and should be connected to the ground plane through multiple vias.
- GNDREF, GNDREF1, and GNDREF2 are signal ground pins and should be connected together though ground plane using separate vias, not through EP. This prevents coupling from return currents of the switching regulators which use the EP as a return path. Ground return currents from the switching regulators must not flow through these pins.

9 Exposed pad connection

The exposed pad (EP) is the ground return for all the switching regulators and should be connected to the ground plane(s) through vias. A minimum of 16 vias is recommended under the EP. The EP also acts as a heat sink for the PF3000, so the vias should not have thermal relief. The designer should also allow sufficient copper area for the EP to reduce unnecessary thermal stress. One efficient way to achieve this is to duplicate the EP ground plane on all layers. When routing high current paths, sufficient number of via should be placed in parallel to help reduce the parasitic impedance. They must be solid thermal vias as shown in Figure 10.

Figure 10. Types of via

'Wicking' of solder through the bore in the vias increase their thermal resistance. Follow techniques such as tenting or via encroaching to prevent solder wicking. Using a bore diameter of 0.3 mm or less also helps minimize wicking due to the surface tension of the liquid solder.

Apply the solder paste to approximately 50% to 75% of the area of the exposed pad. Rather than applying the solder paste in one large section, apply it in multiple smaller sections. This can be accomplished by using an array of openings in the solder stencil. Sectioning helps in even spreading of the solder, as well as in minimizing out-gassing, which can create voids and bridges under the exposed pad. Figure 11 shows an example of how the exposed pad can be laid out.

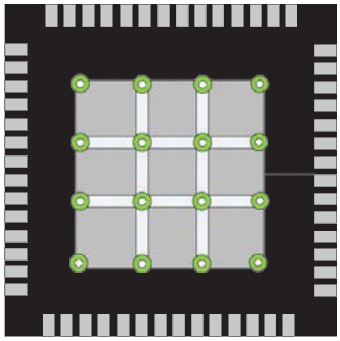

Figure 11. Exposed pad via array

10 Feedback signals

The control loop regulates output voltage at the point where the feedback trace meets the output rail. It is recommended to connect the feedback trace to the output voltage rail near the load for best load regulation. Ensure this trace does not couple noise from other traces/layers. One efficient way to route the feedback trace is alongside the output trace.

11 References

Document number and description		URL
PF3000	Data Sheet	http://www.nxp.com/files/analog/doc/data_sheet/PF3000.pdf
AN1902	QFN Application Note	http://www.nxp.com/files/analog/doc/app_note/AN1902.pdf
Support Pages		**URL**
PF3000 Product Summary Page		http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=PF3000
Power Management Home Page		http://www.nxp.com/webapp/sps/site/homepage.jsp?code=POWERMGTHOME
Analog Home Page		http://www.nxp.com/analog

12 Revision history

Revision	Date	Description of changes
1.0	3/2015	Initial release
	4/2015	Updated format
2.0	6/2015	AN4530 is replaced by AN1902
	7/2016	Updated to NXP document form and style

How to Reach Us:

Home Page:
NXP.com

Web Support:
http://www.nxp.com/support

Document Number: AN5094
Rev. 2.0
7/2016