

RN0063 Release note

MicroXplorer release 2.2

Introduction

This release note is updated periodically in order to keep you abreast of evolutions of the software and any problems or limitations found in this release. Check the ST microcontroller support website at www.st.com to ensure that this is the latest version of this release note.

Summary of the release notes for MicroXplorer release 2.2

Enhancements - Supports all STM32 devices as of September 2012.

Customer support

For more information or help concerning MicroXplorer, please contact the nearest sales office. For a complete list of ST offices and distributors, please refer to www.st.com.

Software updates

You can download software updates and all the latest documentation from the ST microcontroller support site at www.st.com.

Table 1. Applicable tools

Туре	Part number
Development tools	MicroXplorer

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RN0063 Read me first

1 Read me first

1.1 Overview

MicroXplorer is provided to help designers configure the microcontroller I/Os. You can choose the most suitable microcontroller for your application by specifying the required peripherals.

1.2 Host PC system requirements

PC and compatibles running with:

- Windows XP or Windows 7 32-bit operating systems
- Windows 7 64-bit operating systems

A Java Runtime Environment version 1.6 or newer must be installed. On Windows 7 64-bit, install the 32-bit version of Java.

2 What's new in MicroXplorer V2.2?

2.1 New features

- Supports STM32F302x(B-C)
- Supports STM32F303x(B-C)
- Supports STM32F313x(B-C)
- Supports STM32F372x(8-B-C)
- Supports STM32F373x(8-B-C)
- Supports STM32F383x(8-B-C)
- Supports STM32F405O(E-G) and STM32F415OGY

2.2 Microcontrollers supported by this release

- STM32F050C(4-6)Tx, STM32F050K(4-6)Ux
- STM32F051(C-R)(4-6-8)Tx, STM32F051K(4-6-8)Ux
- STM32F100C(4-6-8-B)Tx, STM32F100R(4-6-8-B)Hx,
- STM32F100R(4-6-8-B-C-D-E)Tx, STM32F100V(8-B-C-D-E)Tx,
- STM32F100Z(C-D-E)Tx
- STM32F101C(4-6-8-B)Tx, STM32F101C(4-6-8-B)Ux,
- STM32F101R(4-6-8-B-C-D-E-F-G)Tx, STM32F101T(4-6-8-B)Ux,
- STM32F101V(8-B-C-D-E-F-G)Tx, STM32F101Z(C-D-E-G)Tx
- STM32F102C(4-6-8-B)Tx, STM32F102R(4-6-8-B)Tx
- STM32F103C(4-6-8-B)Tx, STM32F103C(4-6-8-B)Ux,
- STM32F103R(4-6-8-B)Hx, STM32F103R(4-6-8-B-C-D-E-F-G)Tx,
- STM32F103R(C-D-E)Yx, STM32F103T(4-6-8-B)Ux,
- STM32F103V(8-B-C-D-E)Hx, STM32F103V(8-B-C-D-E-F-G)Tx,
- STM32F103Z(C-D-E-F-G)Hx, STM32F103Z(C-D-E-F-G)Tx
- STM32F105RxTx, STM32F105VxTx, STM32F105VxHx,
- STM32F107RxTx, STM32F107VxTx, STM32F107VxHx
- STM32F205RxYx, STM32F205RxTx, STM32F205VxTx, STM32F205ZxTx
- STM32F207VxTx, STM32F207ZxTx, STM32F207IxTx, STM32F207IxHx
- STM32F215RxTx, STM32F215VxTx, STM32F215ZxTx
- STM32F217VxTx, STM32F217ZxTx, STM32F217IxTx, STM32F217IxHx
- STM32F302C(B-C)Tx, STM32F302R(B-C)Tx, STM32F302V(B-C)Tx
- STM32F303C(B-C)Tx, STM32F303R(B-C)Tx, STM32F303V(B-C)Tx
- STM32F313C(B-C)Tx, STM32F313R(B-C)Tx, STM32F313V(B-C)Tx
- STM32F372C(8-B-C)Tx, STM32F372R(8-B-C)Tx, STM32F372V(8-B-C)Tx, STM32F372VCHx
- STM32F373C(8-B-C)Tx, STM32F373R(8-B-C)Tx, STM32F373V(8-B-C)Tx, STM32F373VCHx
- STM32F383C(8-B-C)Tx, STM32F383R(8-B-C)Tx, STM32F383R(8-B-C)Yx, STM32F383V(8-B-C)Tx, STM32F383VCHx
- STM32F405RGTx, STM32F405VGTx, STM32F405ZGTx, STM32F405O(E-G)Yx
- STM32F407I(E-G)Tx, STM32F407I(E-G)Hx,
- STM32F407V(E-G)Tx, STM32F407Z(E-G)Tx
- STM32F415RGTx, STM32F415VGTx, STM32F415ZGTx, STM32F415OGYx
- STM32F417I(E-G)Tx, STM32F417I(E-G)Hx,
- STM32F417V(E-G)Tx, STM32F417Z(E-G)Tx
- STM32L151C(6-8-B)Ux, STM32L151C(6-8-B)Tx,
- STM32L151QCHx, STM32L151QDHx,
- STM32L151R(6-8-B)Hx, STM32L151R(6-8-B)Tx, STM32L151RxY,
- STM32L151(R-V-Z)CTx, STM32L151(R-V-Z)DTx,
- STM32L151V(8-B)Hx, STM32L151V(8-B)Tx
- STM32L152C(6-8-B)Ux, STM32L152C(6-8-B)Tx,

- STM32L152QCHx, STM32L152QDHx,
- STM32L152R(6-8-B)Hx, STM32L152R(6-8-B)Tx, STM32L152RxY,
- STM32L152(R-V-Z)CTx, STM32L152(R-V-Z)DTx,
- STM32L152V(8-B)Hx, STM32L152V(8-B)Tx
- STM32L162QDHx, STM32L162RDY, STM32L162(R-V-Z)DTx

3 Known problems and limitations

This release of MicroXplorer has the same problems and limitations as release 2.0, please refer to *Chapter 4.2.3* for a detailed description.

- Peripheral interdependence cannot be configured
- Peripherals subparts cannot always be selected/unselected
- Chip View I/O pin may be erased when peripheral enabled
- Windows 7 64-bit: error message MSVCR71.dll missing

4 Release information for previous releases

4.1 Summary of changes in MicroXplorer V2.1

4.1.1 New features

- Supports STM32F050x(4-6)
- Supports STM32F051x(4-6-8)
- Supports STM32L151x(C-D)
- Supports STM32L152x(C-D)
- Supports STM32L162xD

4.1.2 Functional enhancements

- Supports all STM32 devices as of May 2012.
- A configuration report file can be generated at any time.
- MicroXplorer can be plugged into Eclipse.
- Supports BGA and CSP packages.
- Power pad present in some packages is now graphically represented in the pinout view

4.2 Summary of changes in MicroXplorer V2.0

4.2.1 New features

 Supports STM32F4x, STM32F100x, STM32F101x/F102x/F103x, STM32L15xx(6-8-B), STM32F205x/F207x including BGA-176 package, STM32F215x/F217x, STM32F105x/F107x including BGA-100 package

4.2.2 Functional enhancements

- A configuration report file can now be generated at any time.
- MicroXplorer can now be plugged into Eclipse (see Plug-in User Installation Guide).
- The MCU Selector window has been enhanced.
- BGA and CSP packages are now supported.
- Manual Remap can now be performed from Chip View proposing all the possible pins.
- Peripherals items or modes are highlighted in orange when they are partially available.
- The saved configuration can be reloaded later by either File -> Load Config menu or by Double-clicking on myConfig.ioc configuration file from Windows Explorer
- QFN packages display is now correct.

4.2.3 Known problems and limitations

- Interdependence between peripherals cannot be configured, so for example:
 - In STM32F207VxTx, IN0 can be shared between ADC1 and ADC2 but when IN0 is selected in the tool for ADC1, IN0 is not available for ADC2.

BKIN signal activation is not limited for some timers (e.g. on TIM1 and TIM8).

Workaround: None

- Subparts of peripherals cannot always be selected/unselected, so for example:
 - For the FSMC peripheral, the selection of one of these modes CF, CF IDE, NOR RAM, NOR Mux, NAND 16 - always allocates the largest amount of pins.
 - Selection of a timer mode allocates the largest amount of pins (STM32F207VxTx Timer3 PWM-input mode allocates 4 channels instead of the minimum of one).

Workaround: None

 If you select a pin as an I/O in Chip View, this pin may be erased when enabling a peripheral.

Workaround: Remap pin manually in Chip View and reallocate to original I/O value.

 On Windows 7 64-bit, you may get the following error message: The program can't start because MSVCR71.dll is missing from your computer.

Workaround: Copy MSVCR71.dll from C:\Program Files (x86)\Java\jre6\bin to C:\Windows\SysWOW64

4.3 Summary of changes in MicroXplorer V1.1

4.3.1 Known problems and limitations

Workarounds for problems:

- SPIx and I2Cx peripherals should not be accessible at the same time, but they are.
 Workaround: Do not select SPIx and I2Cx at the same time.
- **TIMx** peripheral **Active-external-clock** checkbox should only be available if a **TIMx** mode is set, but it is always available (STM32F205x/207x).
 - **Workaround**: Do not select **Active-external-clock** unless you also select a **TIMx** mode.
- SPIX peripheral With NSS checkbox should only be available if a SPIx mode is set, but it is always available (STM32F205x/207x).
 - Workaround: Do not select With NSS unless you also select an SPIx mode.
- Rule7 limitation for STM32F105x/107x. If Keep User Placement has not been set, MicroXplorer may suppress the pin location of a function that has been mapped individually (i.e. it may give this pin to a peripheral mode).

Workaround: set Keep User Placement, to keep the pin location of the function.

Limitations:

Validated on Windows XP only (validation on Win7 will be performed in a future release).

- **TIMx** peripherals. For all the following modes, the timer channels are mapped/unmapped as a group and not individually.
 - Input-capture(_Ext-clock),
 - Forced-output(Ext-clock),
 - Output-compare(_Ext-clock),
 - PWM-generation(_Break-input)(_Ext-clock),
 - One-pulse(_Ext-clock).

- For **Nonmuxed-Nor-Ram** mode all the **NOR RAM** peripheral functions are mapped as a group and not individually.
- For **Muxed-Nor-Ram** all the **NOR MUX** peripheral functions are mapped as a group and not individually.
- For **NAND-Flash** mode all the **NAND** peripheral functions are mapped as a group and not individually.
- BGA packages (STM32F105VxHx and STM32F107VxHx) are not available.
- In TIM1 Input-capture mode (STM32F105x/107x), remap3 pins (PA15, PB3, PB10, PB11) cannot be obtained by manual remapping.
 They can only be obtained by blocking PA0-WKUP, PA1, PA2 and PA3.
- TIM2 PWM-input-1 and PWM-input-4 mode issues. If TIM2 PWM-input-1 mode is activated from the Peripherals Panel, then TIM2_CH4 on PA3 is activated from Chip View, and then PWM-input-1 mode is disabled, the result is that PWM-input-4 is not selected (but it should be) and MII is available (but it should not be) in the Peripherals Panel.
- SYS Trace-Asynchro mode is missing (STM32F105x/107x). PB3 pin should be available either for Trace-Asynchro, or for Trace-Synchro modes (i.e. SYS_JTDO function should in fact be SYS_JTDO-SWO).
- Rule1 and Rule2 interference: a function mapped from Chip View is moved/unselected
 if a mode including this function is set elsewhere (for example, from the Peripheral
 Panel or Disable All button).

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RN0063 Revision history

5 Revision history

Table 2. Document revision history

Date	Revision	Changes
27-May-2011	1	Initial release for MicroXplorer version 1.1.
13-Feb-2012	2	Release for MicroXplorer version 2.0.
11-May-2012	3	Release for MicroXplorer version 2.1.
19-Oct-2012	4	Release for MicroXplorer version 2.2.

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