

Master Clock Generator

TITLE

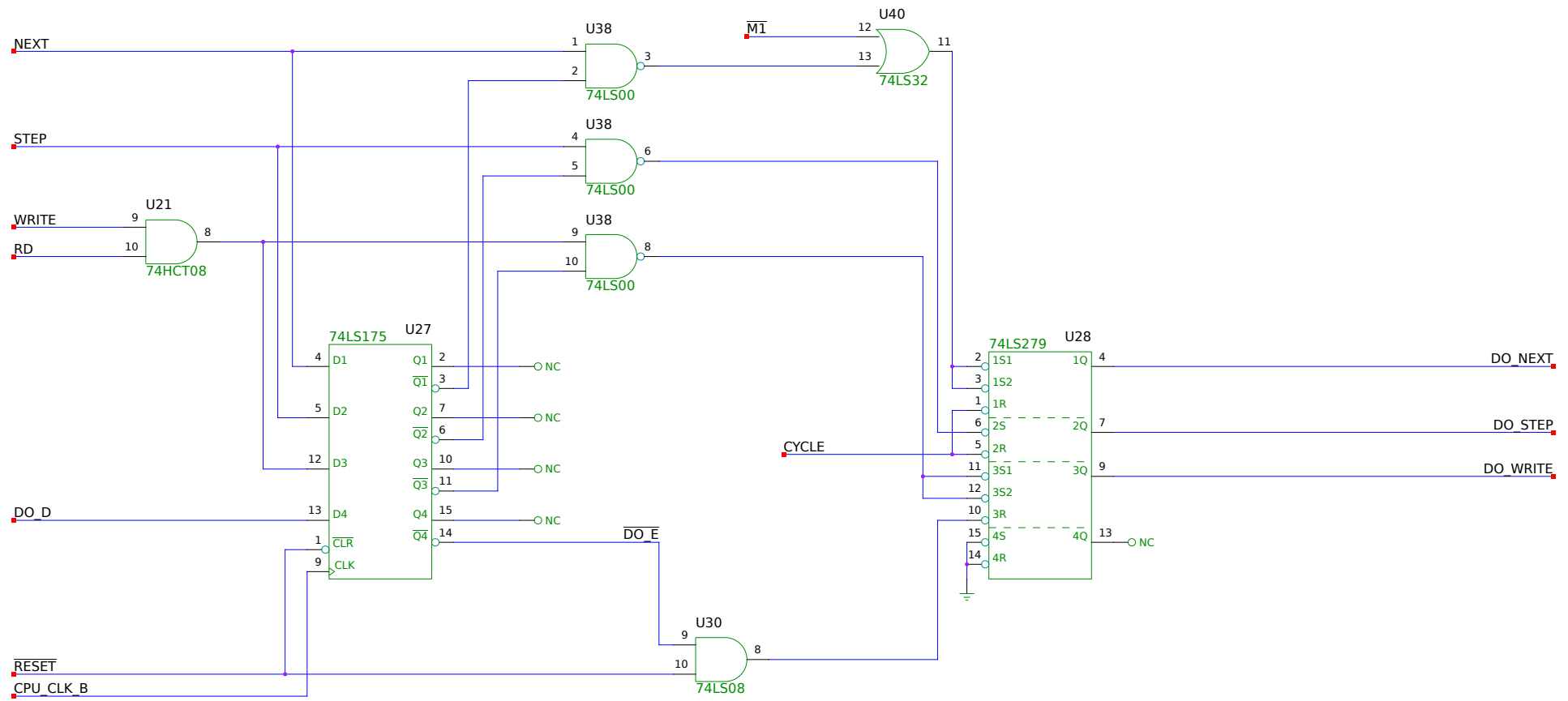
FILE: Clock.sch

PAGE

OF

REVISION 12/4/2019

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ZARC Front Panel Operation Triggers

TITLE

FILE: Control_3.sch

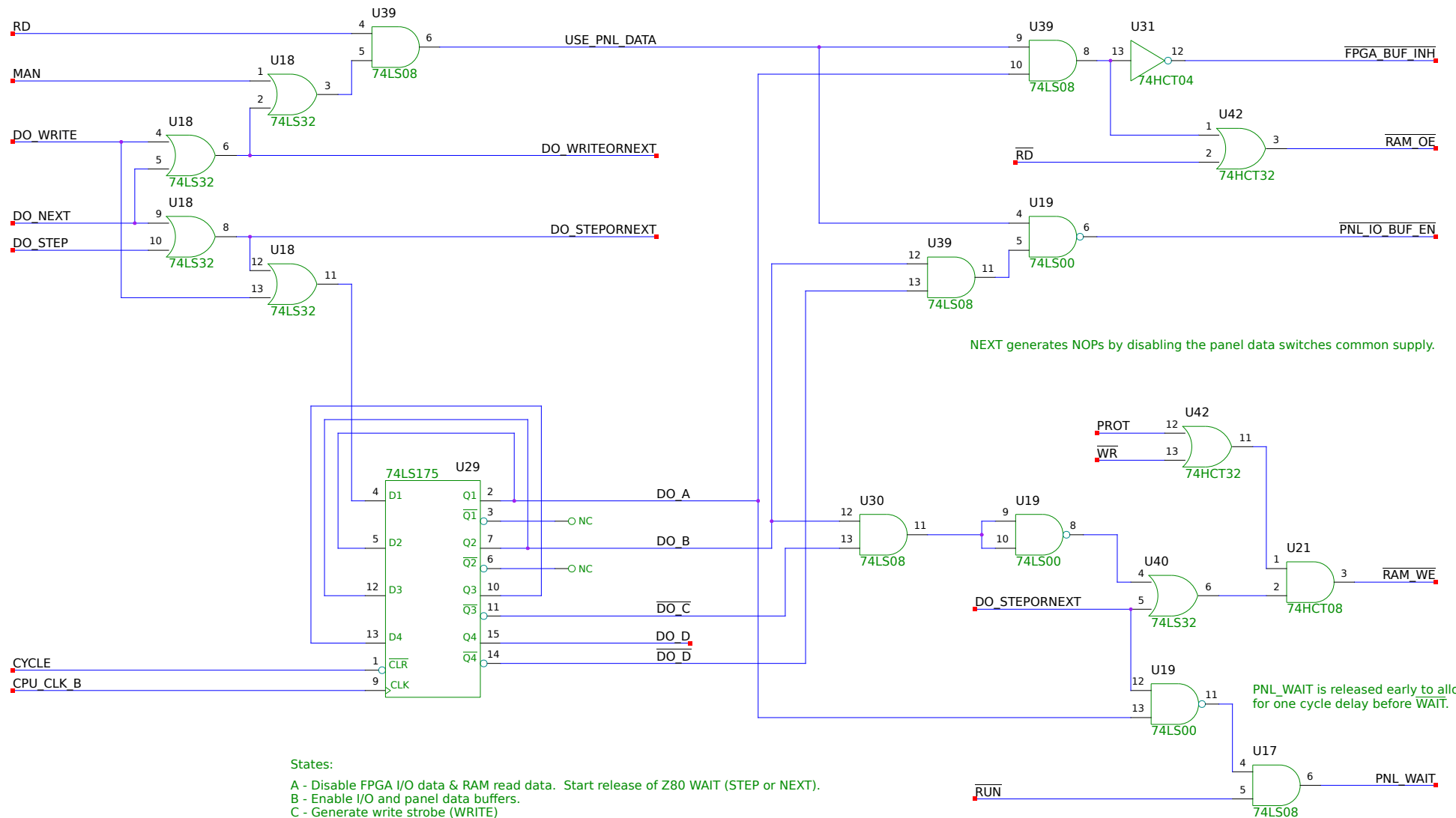
PAGE

OF

REVISION: 8/3/2019

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Note: panel data is only for reads, so we never need to cope with I/O buffer turnaround.



States:

- A - Disable FPGA I/O data & RAM read data. Start release of Z80 WAIT (STEP or NEXT).
- B - Enable I/O and panel data buffers.
- C - Generate write strobe (WRITE)
- D - Disable I/O and panel data buffers.
- E - End write cycle.

NEXT and STEP cycles are ended by the end of the Z80 bus cycle.

ZARC Front Panel Operation State Machine

TITLE

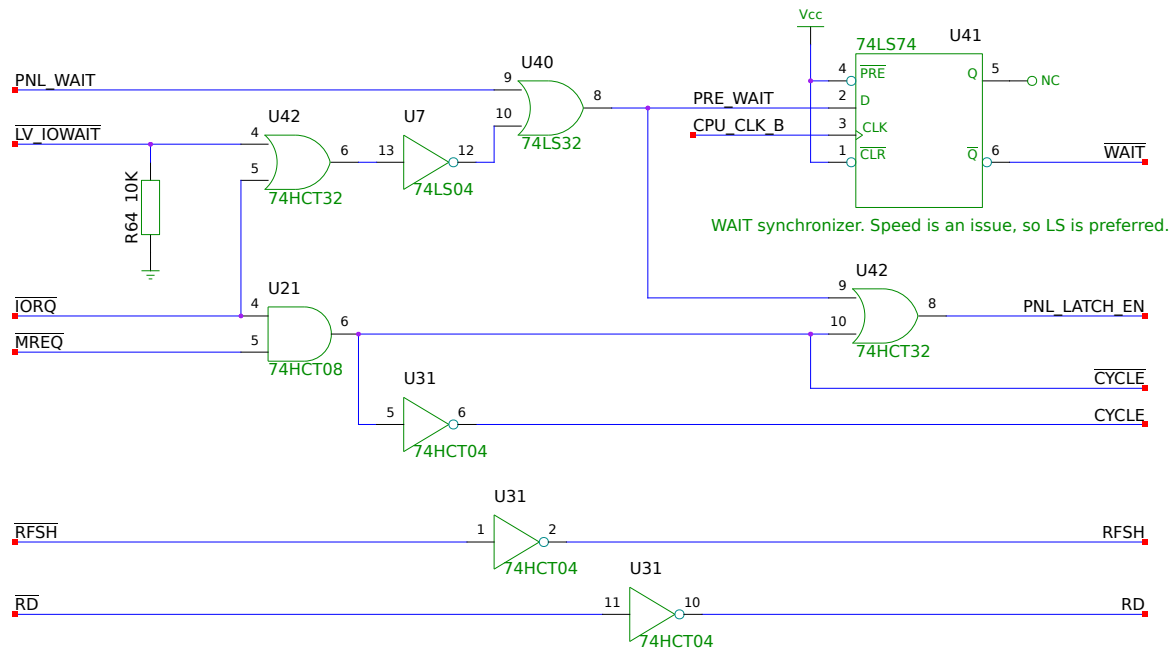
FILE: Control_4.sch

PAGE

OF

REVISION: 21/2/2021

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Panel data latch is transparent between cycles and when the processor is stopped by the panel logic.

ZARC Front Panel Control Signals
TITLE

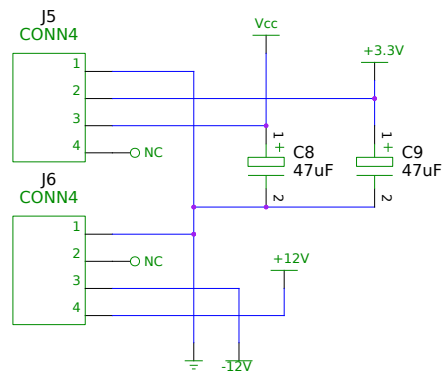
FILE: Control_5.sch

PAGE

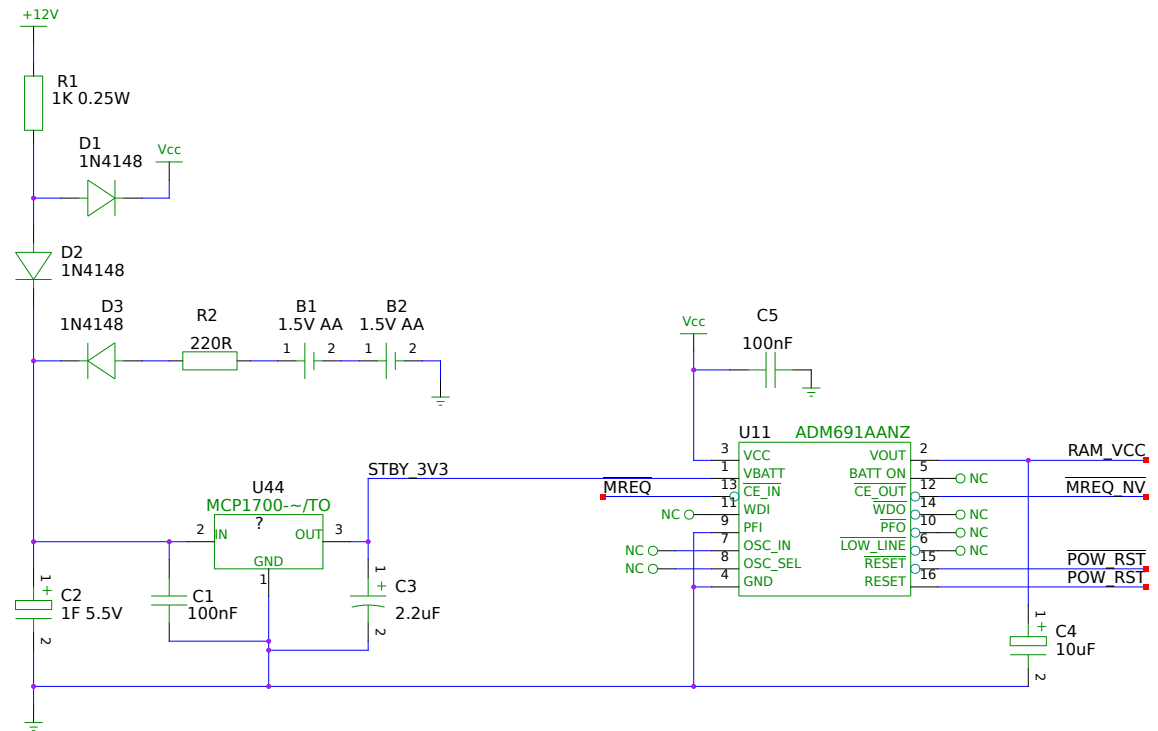
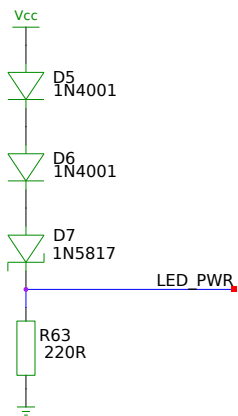
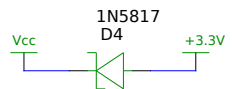
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Diode prevents 3.3V powered devices sinking current into unpowered 5V devices.



ZARC Backup Power and Reset Generation

TITLE

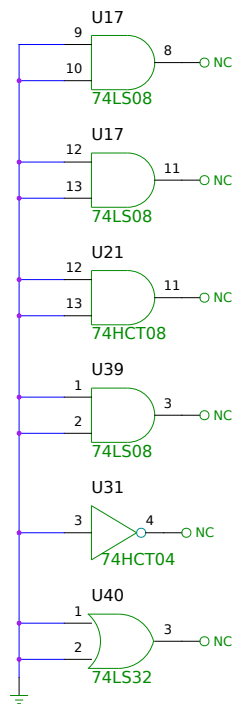
FILE: Power.sch

PAGE

OF

REVISION: 21/2/2021

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Spare Gates

TITLE

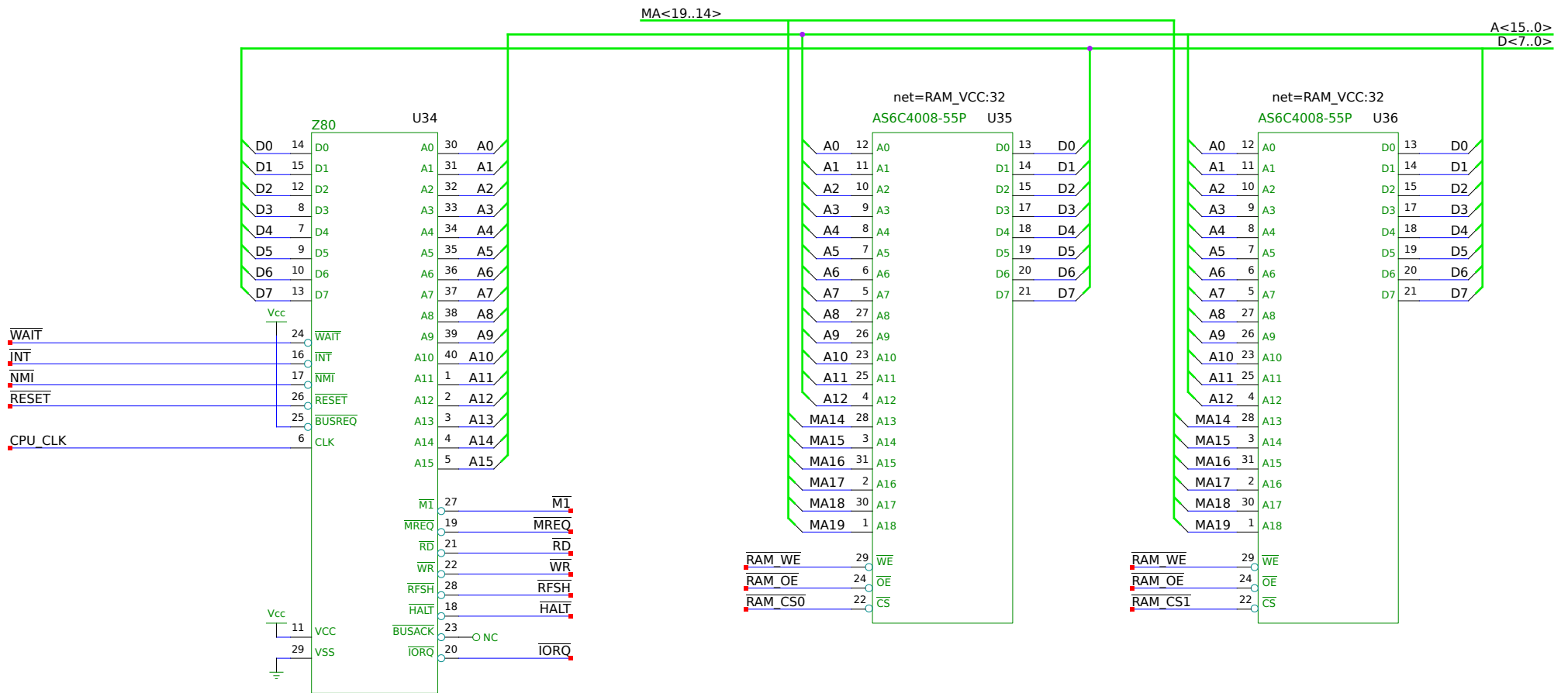
FILE: Spares.sch

PAGE

OF

REVISION: 21/2/2021

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ZARC Z80 CPU and RAM

TITLE

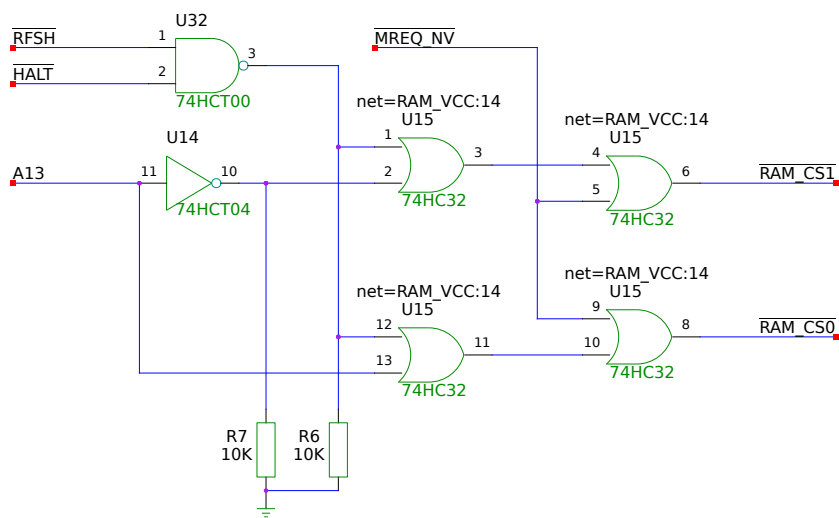
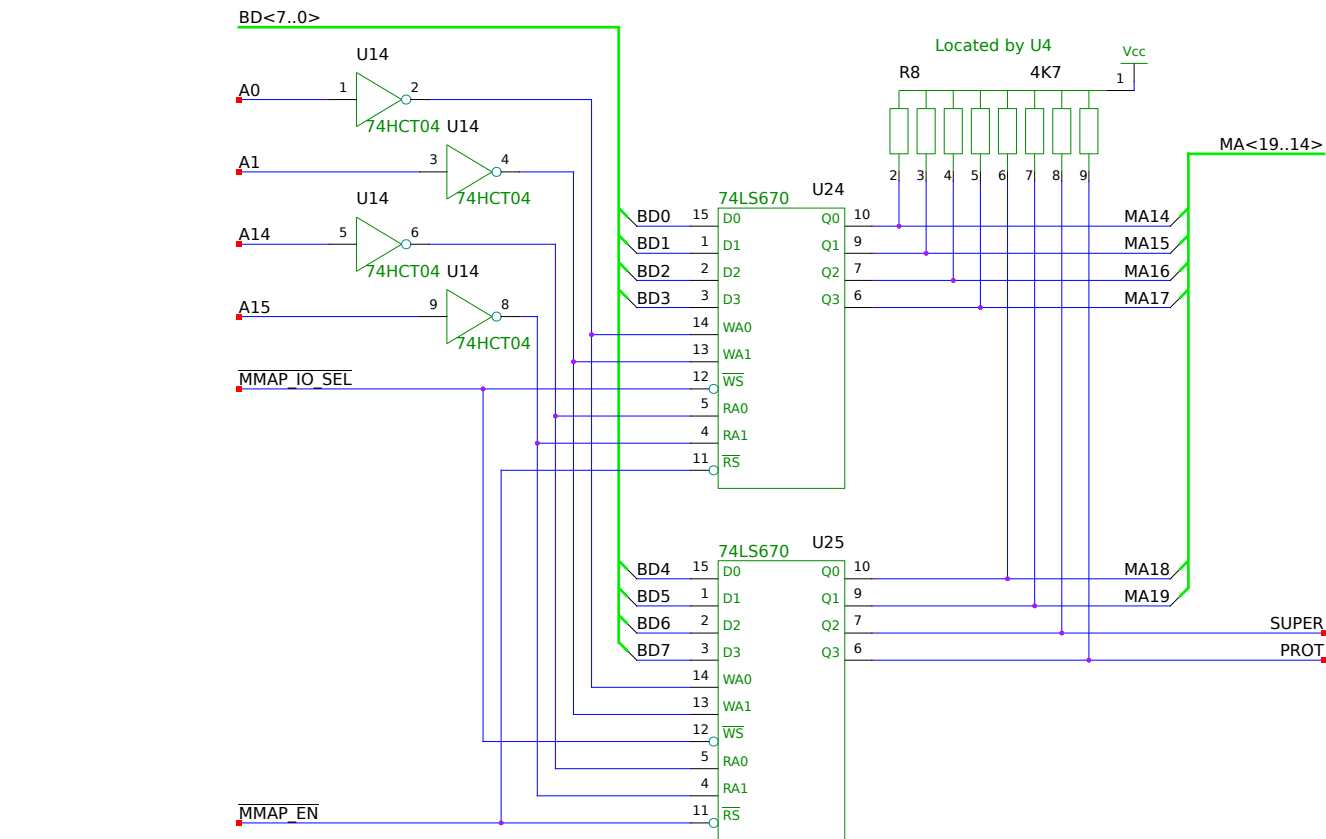
FILE: Z80_1.sch

PAGE

OF

REVISION: 19/1/2019

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ZARC RAM Chip Selects and Memory Mapping
TITLE

FILE: Z80_2.sch

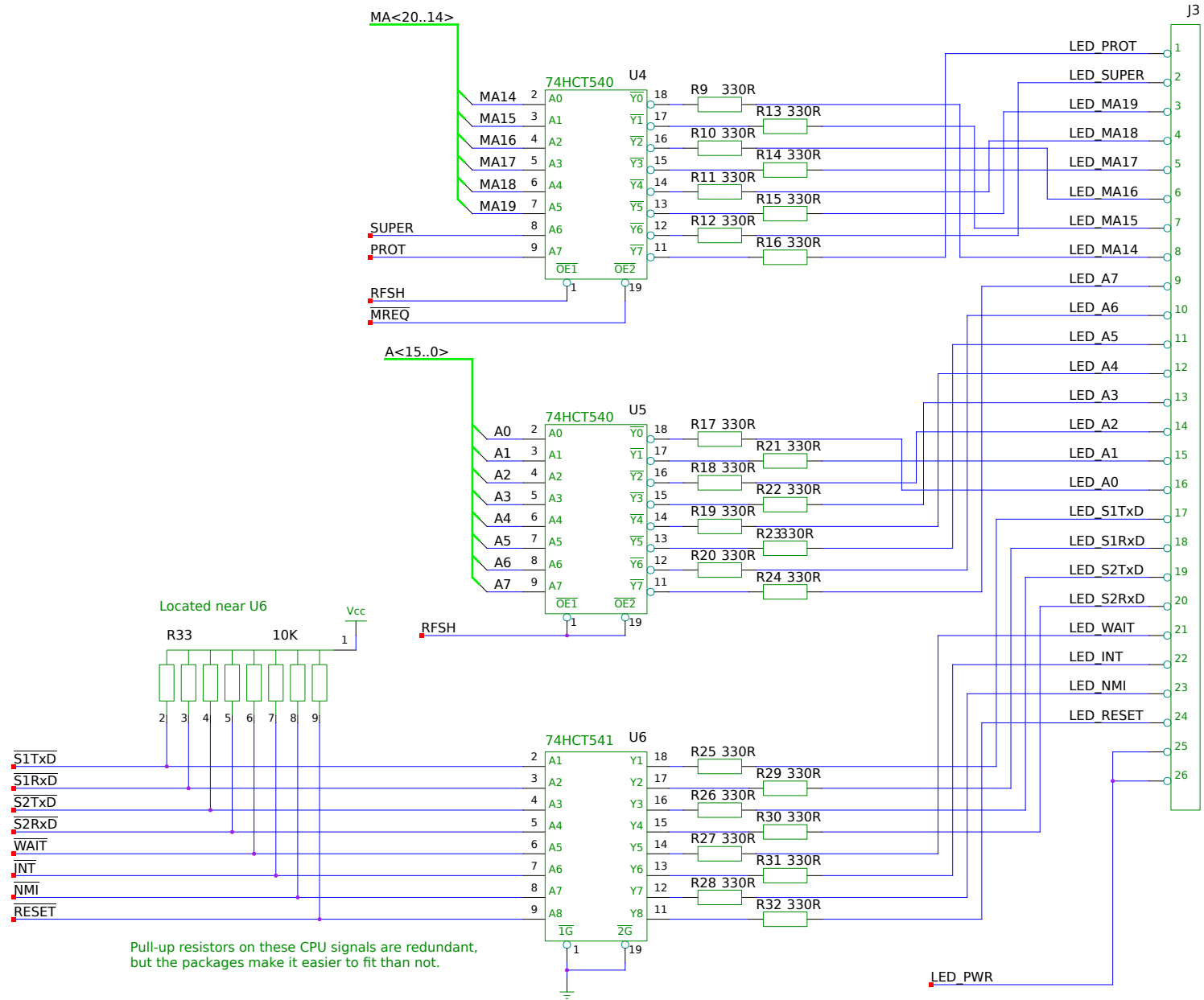
PAGE

OF

REVISION: 19/1/2019

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Display board (Right)



ZARC Front Panel LED Drivers (1 of 2)

TITLE

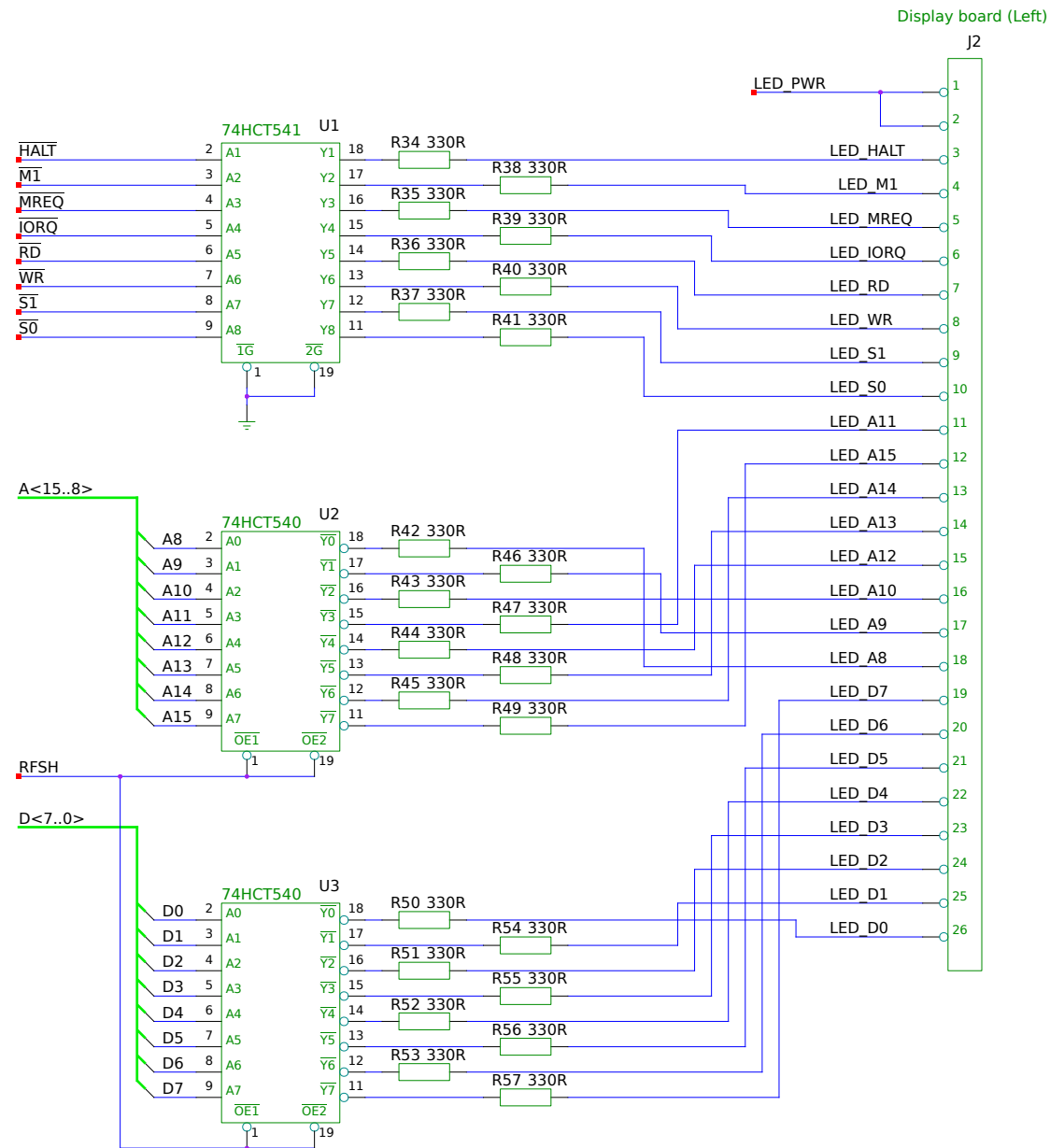
FILE: Z80_3.sch

PAGE

OF

REVISION: 21/2/2021

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ZARC Front Panel LED Drivers (2 of 2)
TITLE

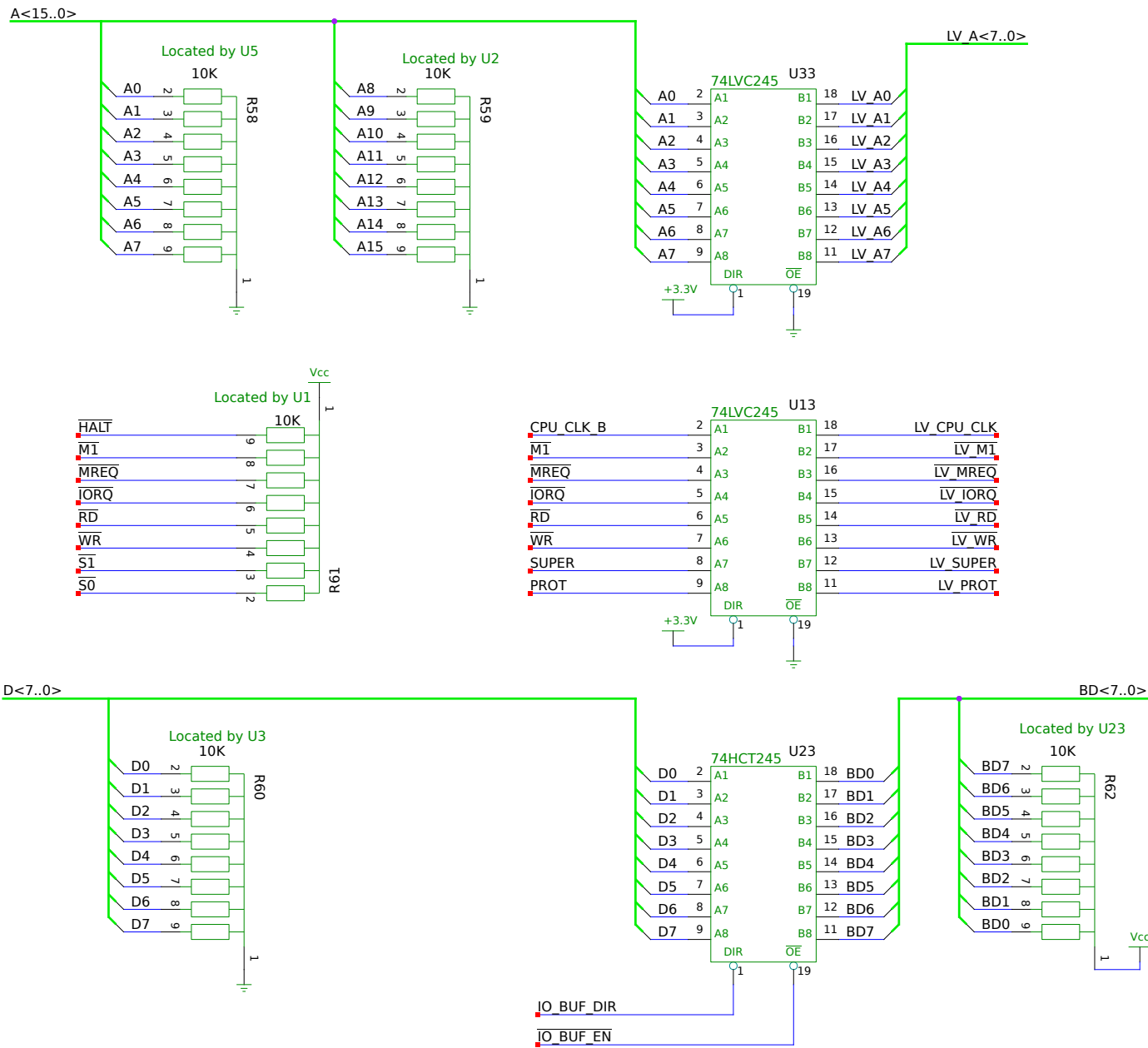
FILE: Z80_4.sch

PAGE

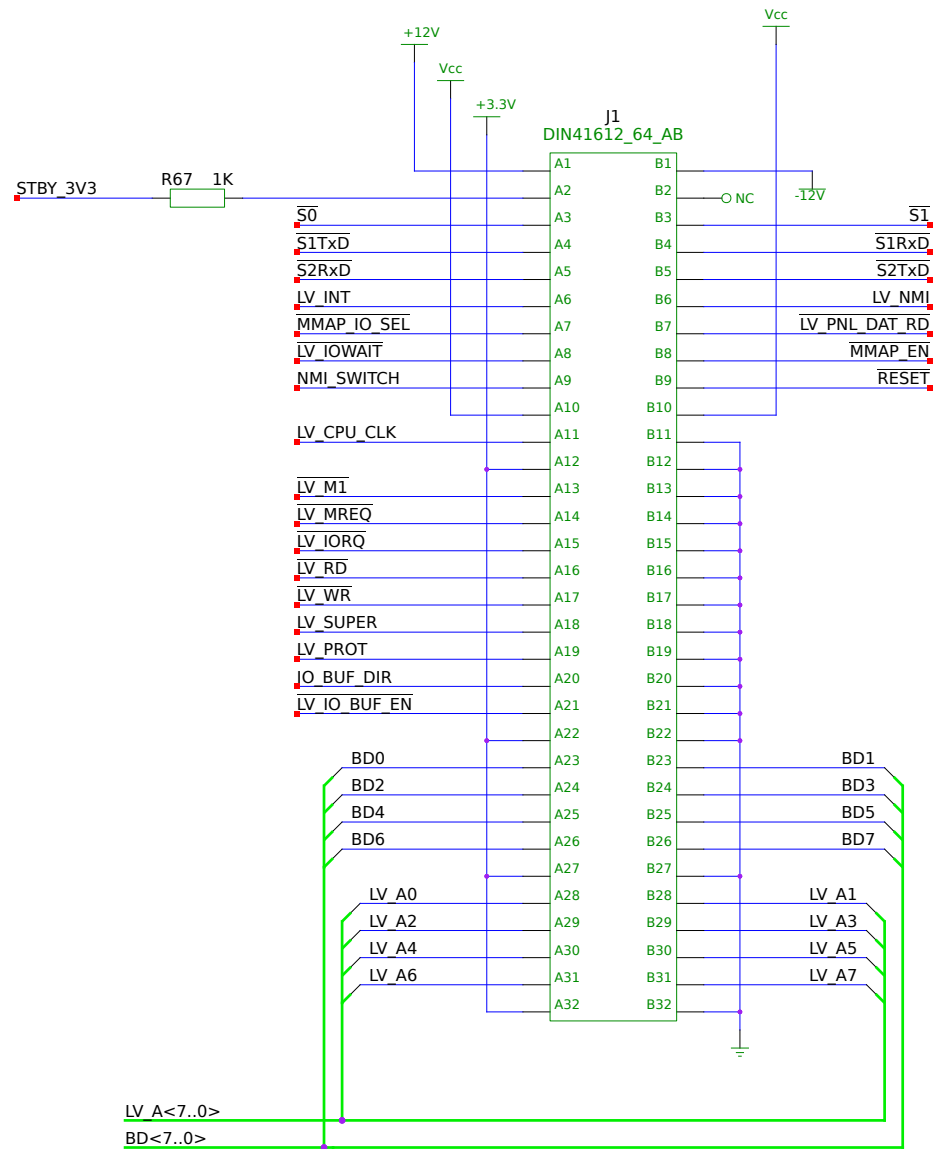
OF

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ZARC I/O Bus Buffers		
TITLE		
FILE: Z80_5.sch	REVISION: 21/2/2021	
PAGE	OF	DRAWN BY: Merlin Skinner



ZARC I/O Board Connector

TITLE

FILE: Z80_6.sch

PAGE

OF

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