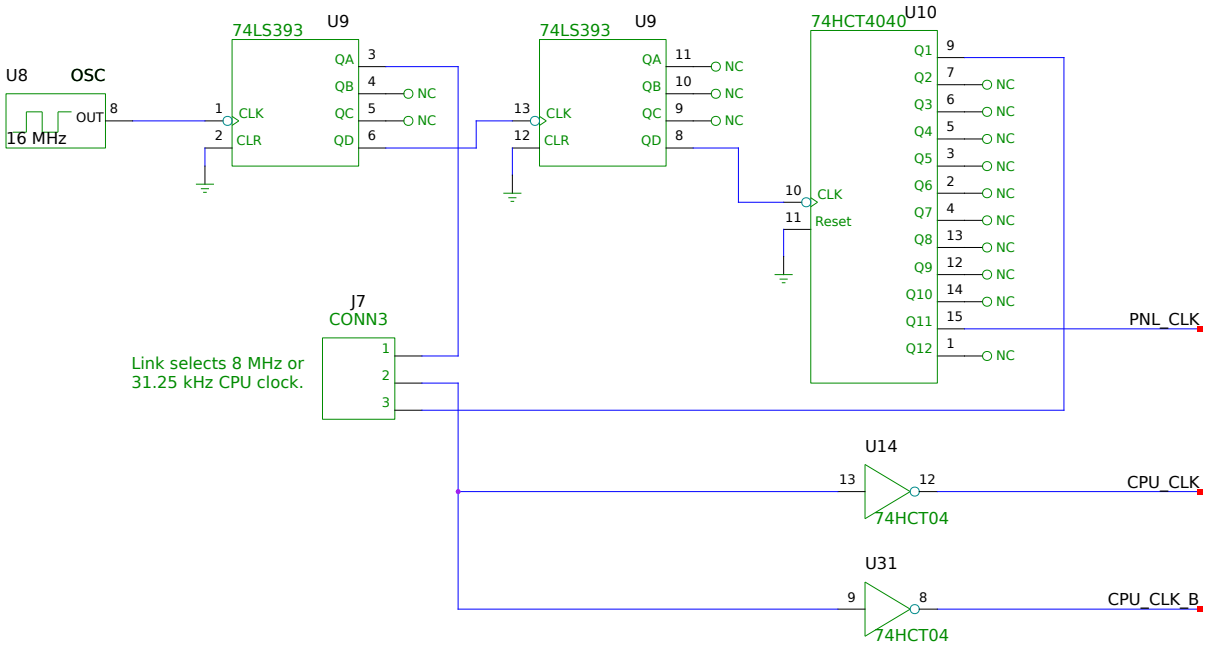

Master Clock Generator TITLE	
FILE: Clock.sch	REVISION 12/4/2019
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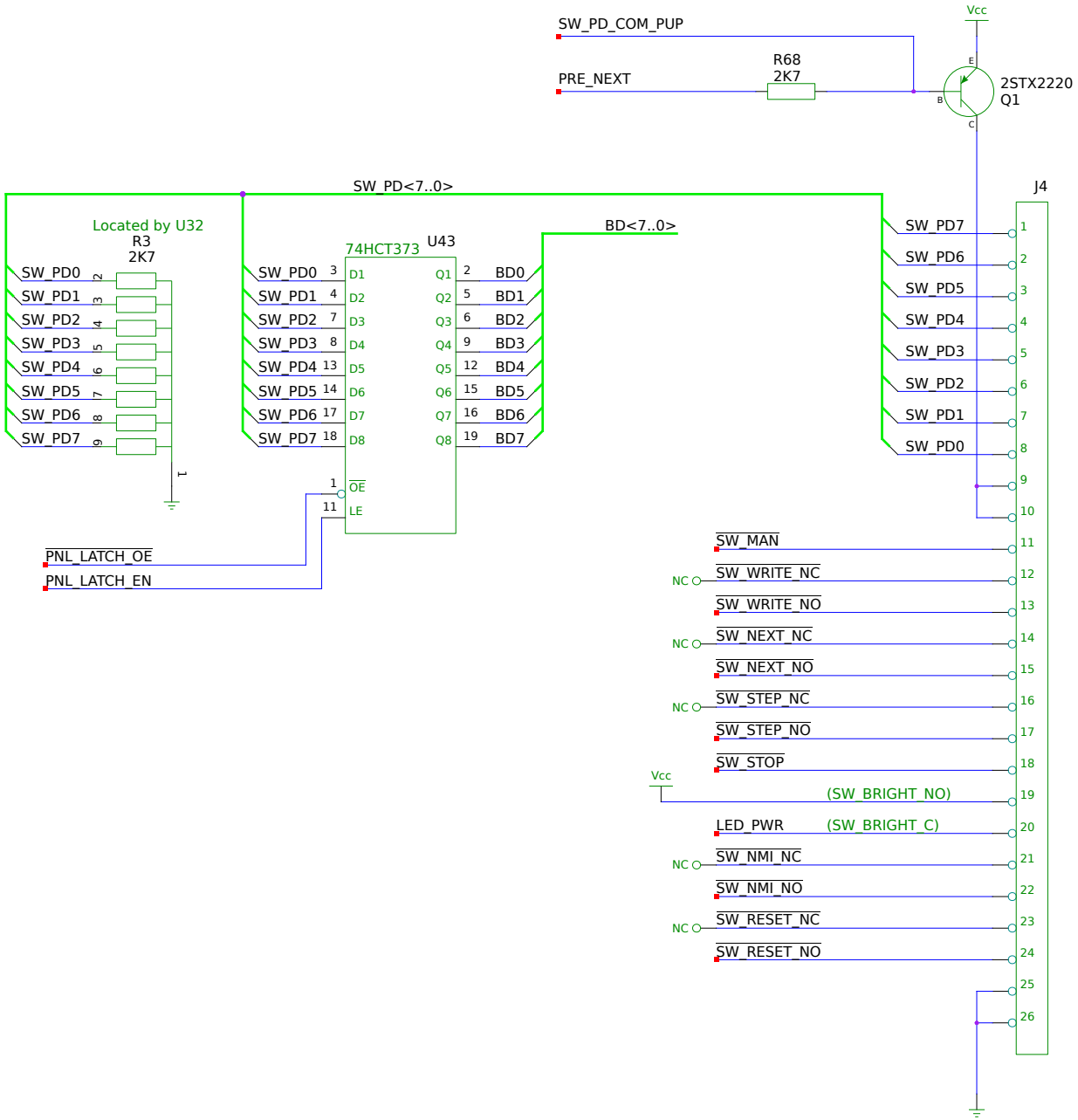

ZARC Front Panel Interface

TITLE

FILE: Control_1.sch

REVISION: 12/4/2019

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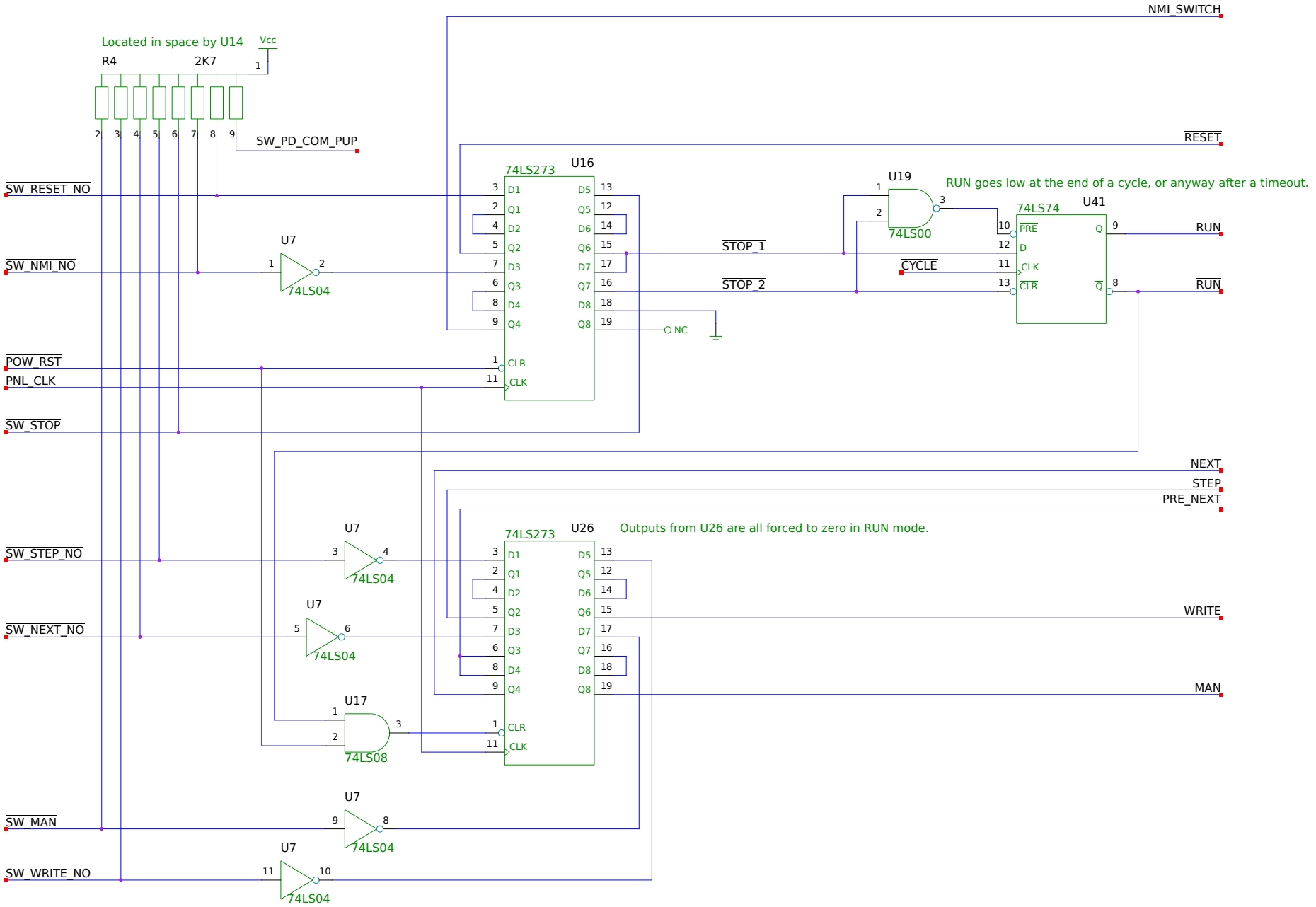

ZARC Switch Debouncing	
TITLE	
FILE: Control_2.sch	REVISION: 21/2/2021
PAGE OF	DRAWN BY: Merlin Skinner

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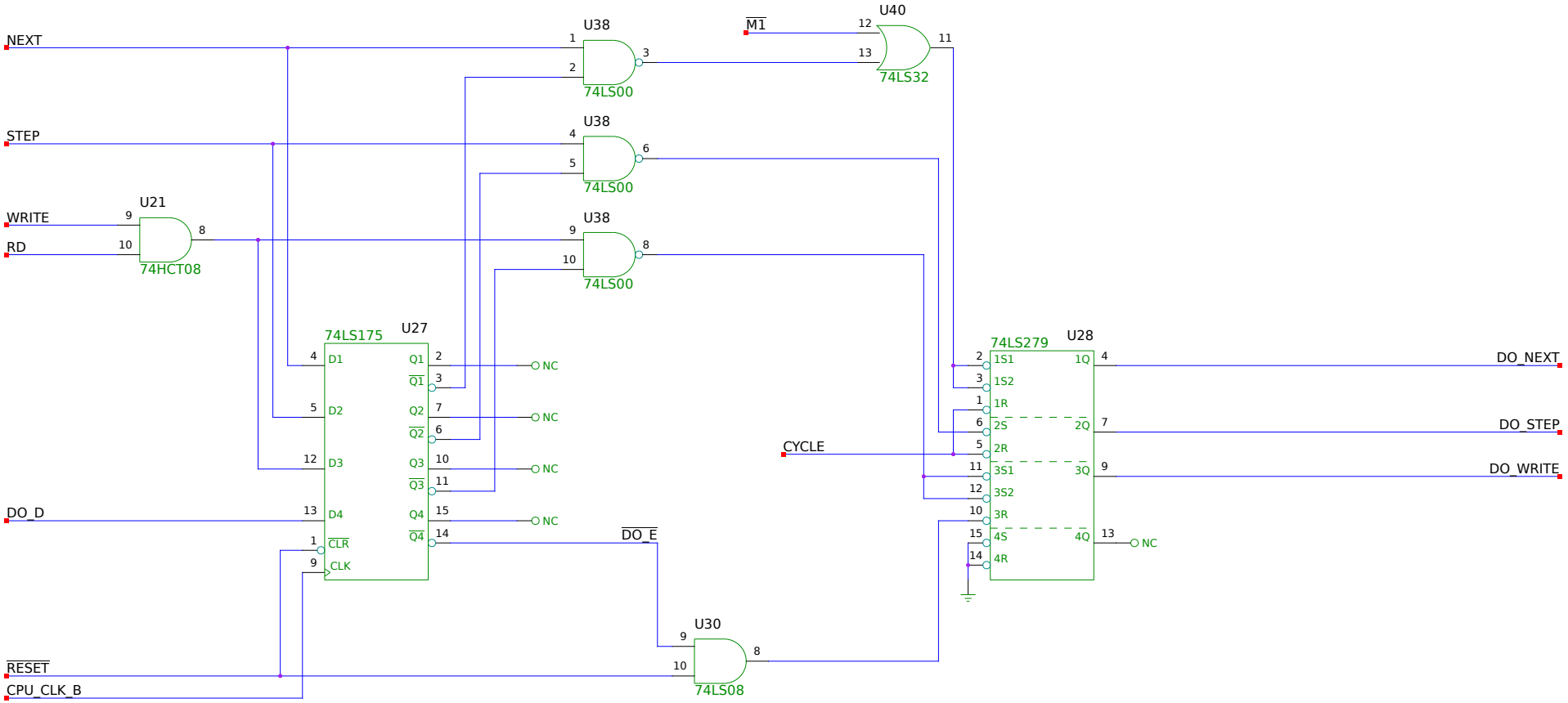

ZARC Front Panel Operation Triggers	
TITLE	
FILE: Control_3.sch	REVISION: 8/3/2019
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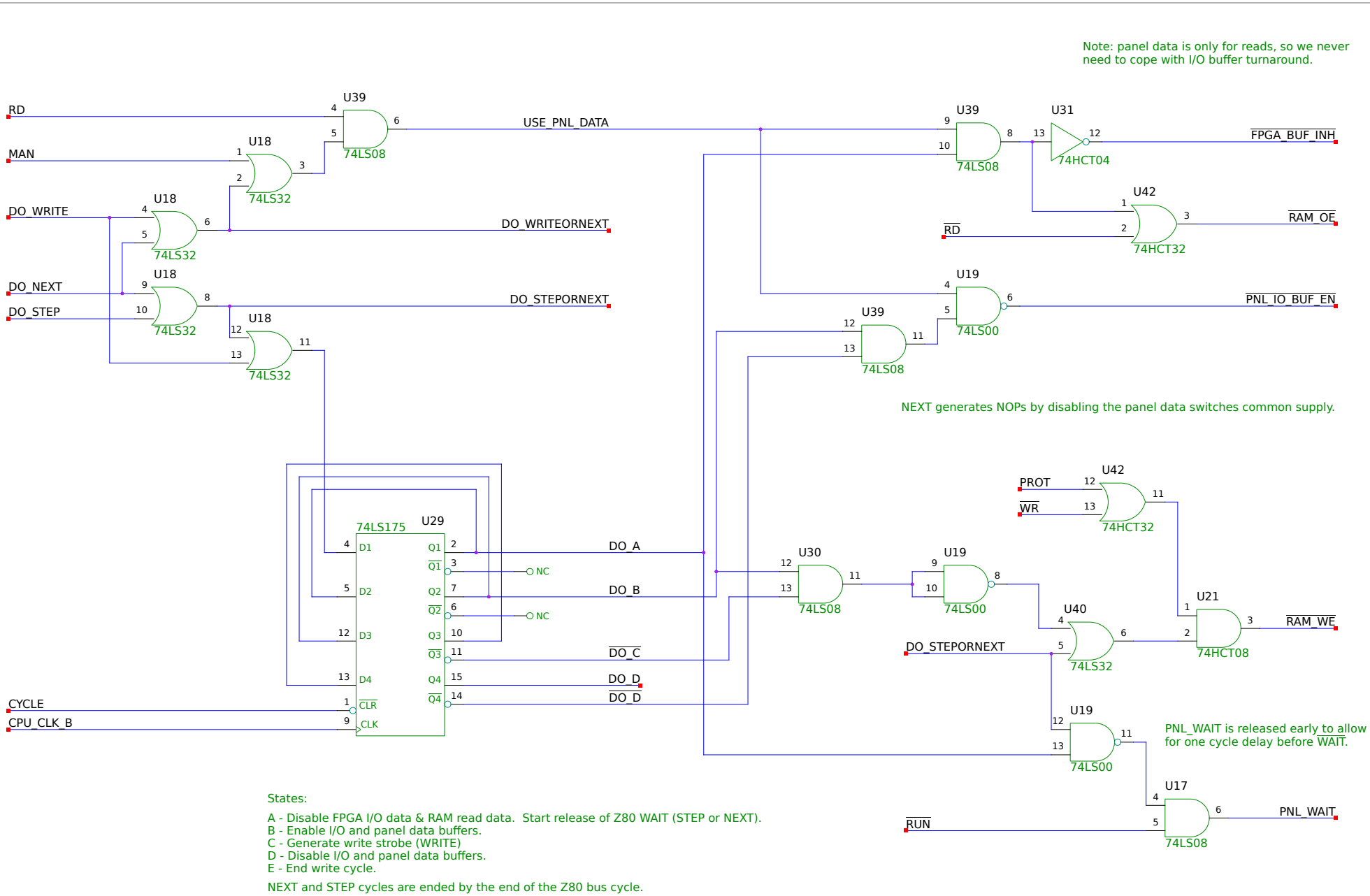

ZARC Front Panel Operation State Machine	
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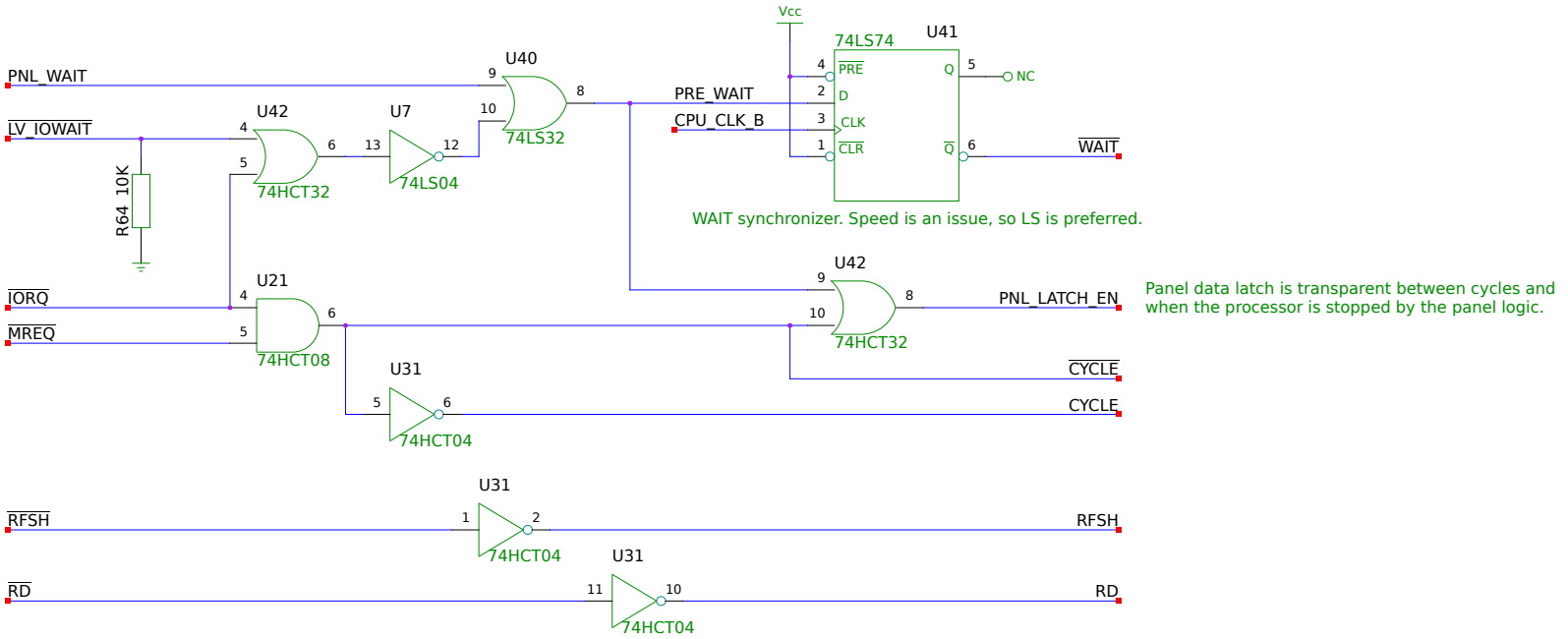

ZARC Front Panel Control Signals	
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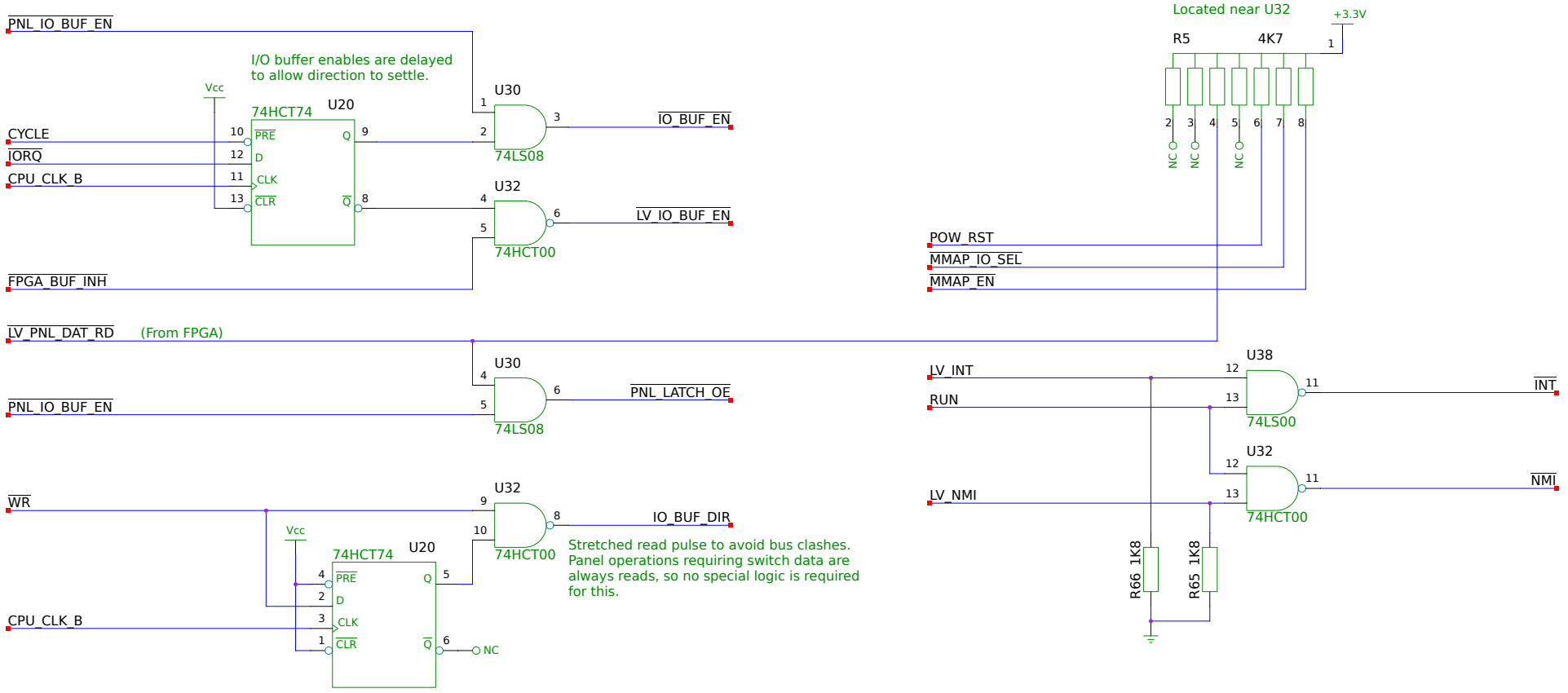

ZARC I/O Bus Control and Interrupt Logic

TITLE

FILE: Control_6.sch

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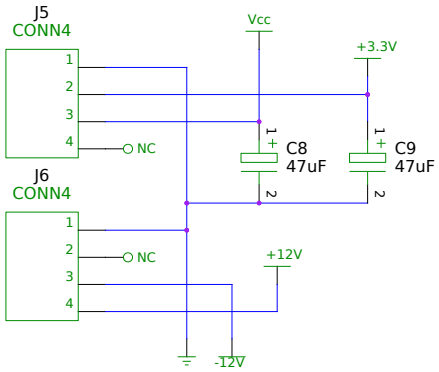
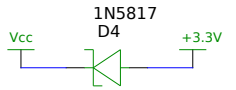
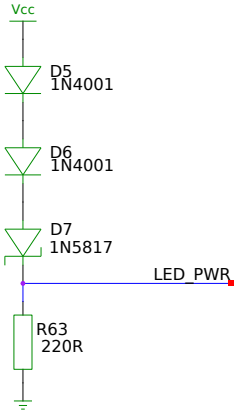
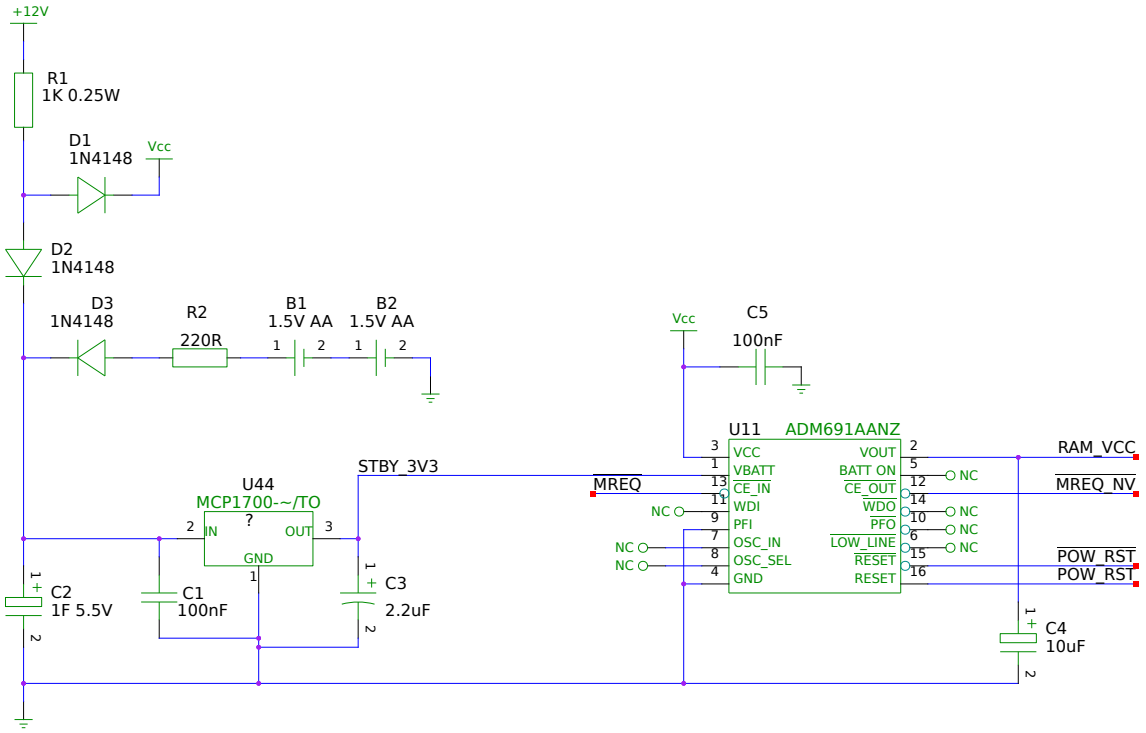


Diode prevents 3.3V powered devices sinking current into unpowered 5V devices.







ZARC Backup Power and Reset Generation	
TITLE	
FILE: Power.sch	REVISION: 21/2/2021
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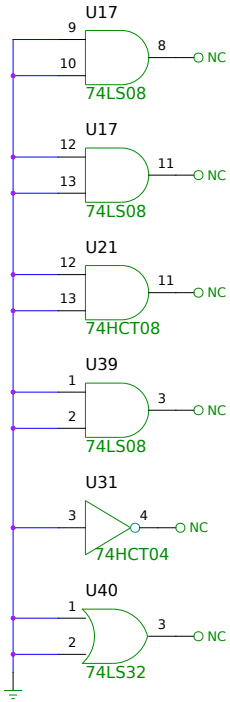

Spare Gates TITLE	
FILE: Spares.sch PAGE OF	REVISION: 21/2/2021 DRAWN BY: Merlin Skinner

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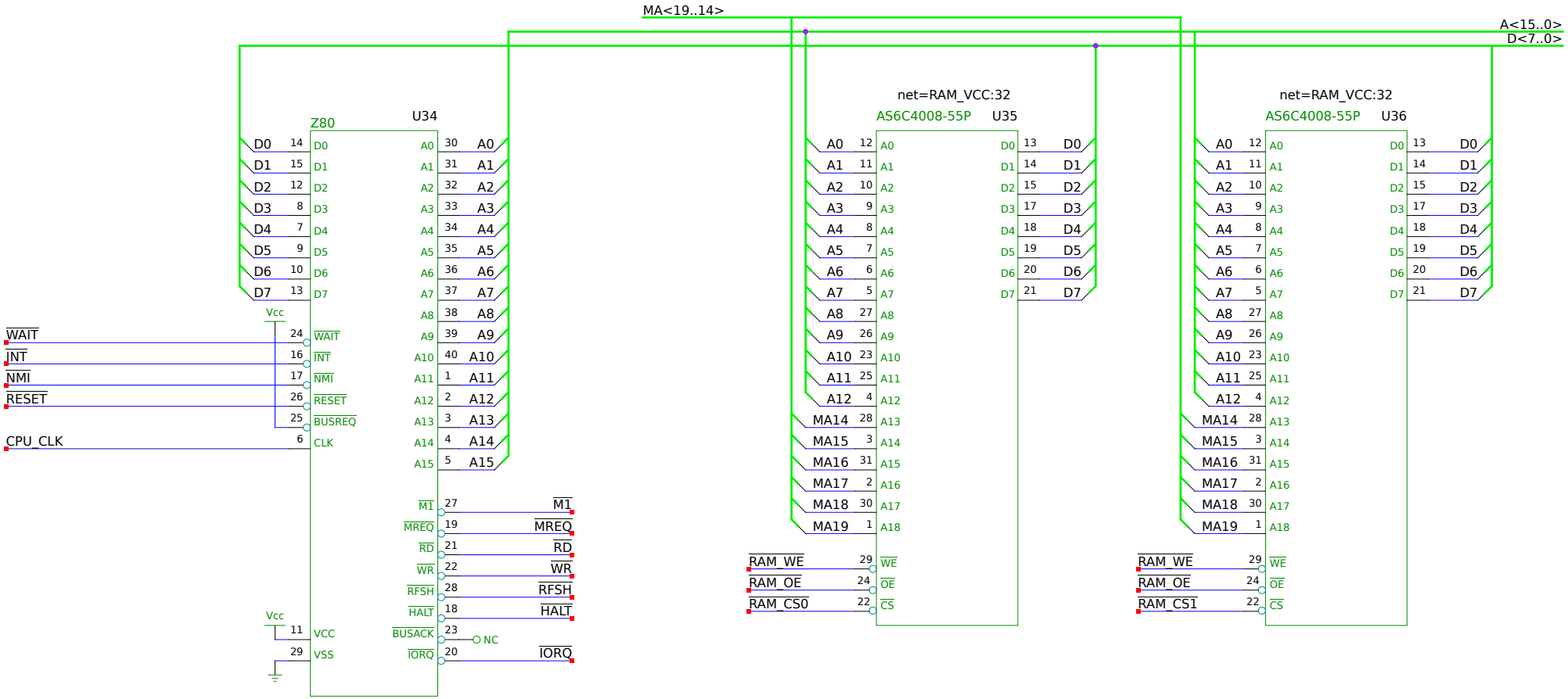

ZARC Z80 CPU and RAM

TITLE

FILE: Z80_1.sch

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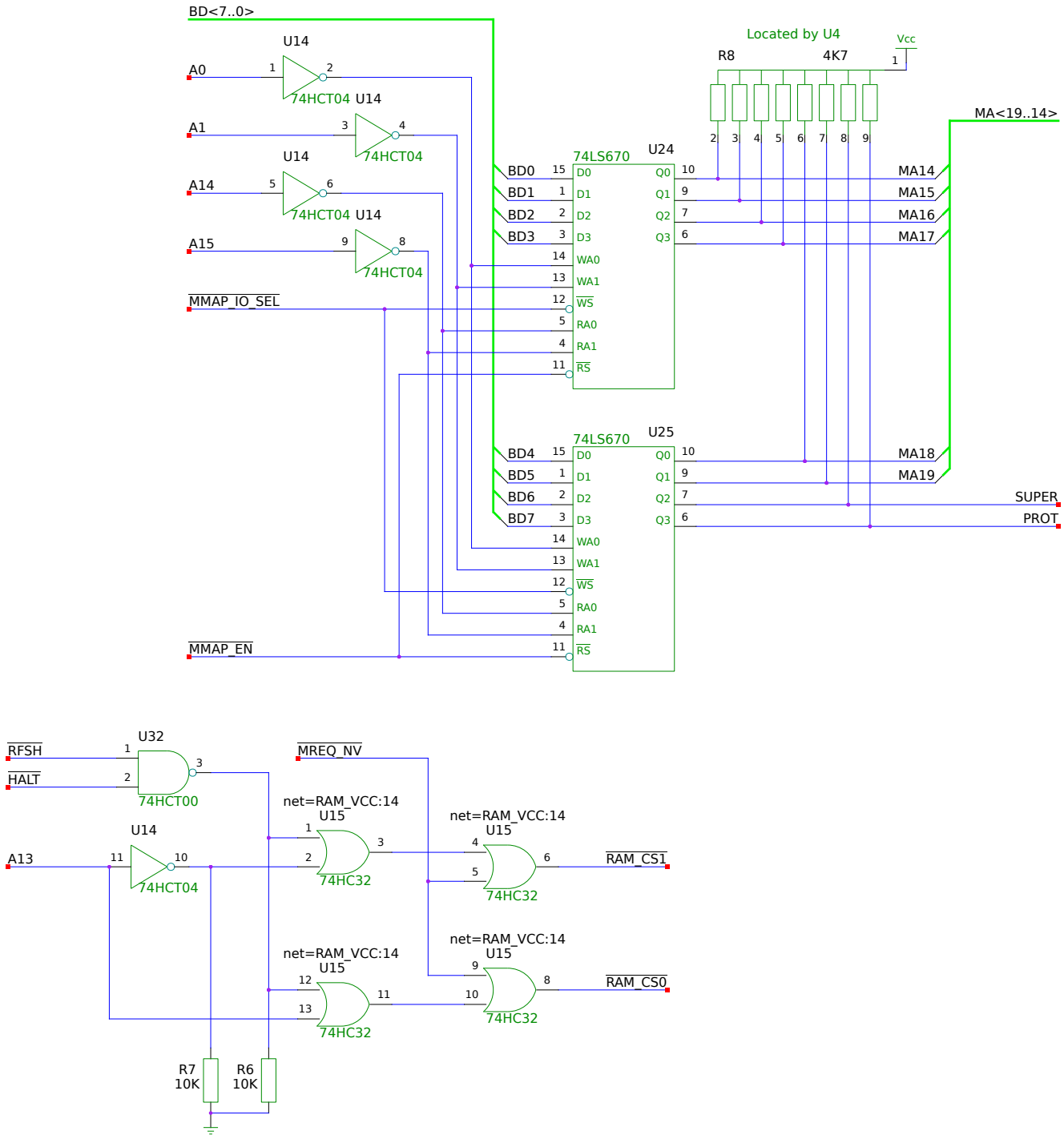

ZARC RAM Chip Selects and Memory Mapping

TITLE

FILE: Z80_2.sch

REVISION: 19/1/2019

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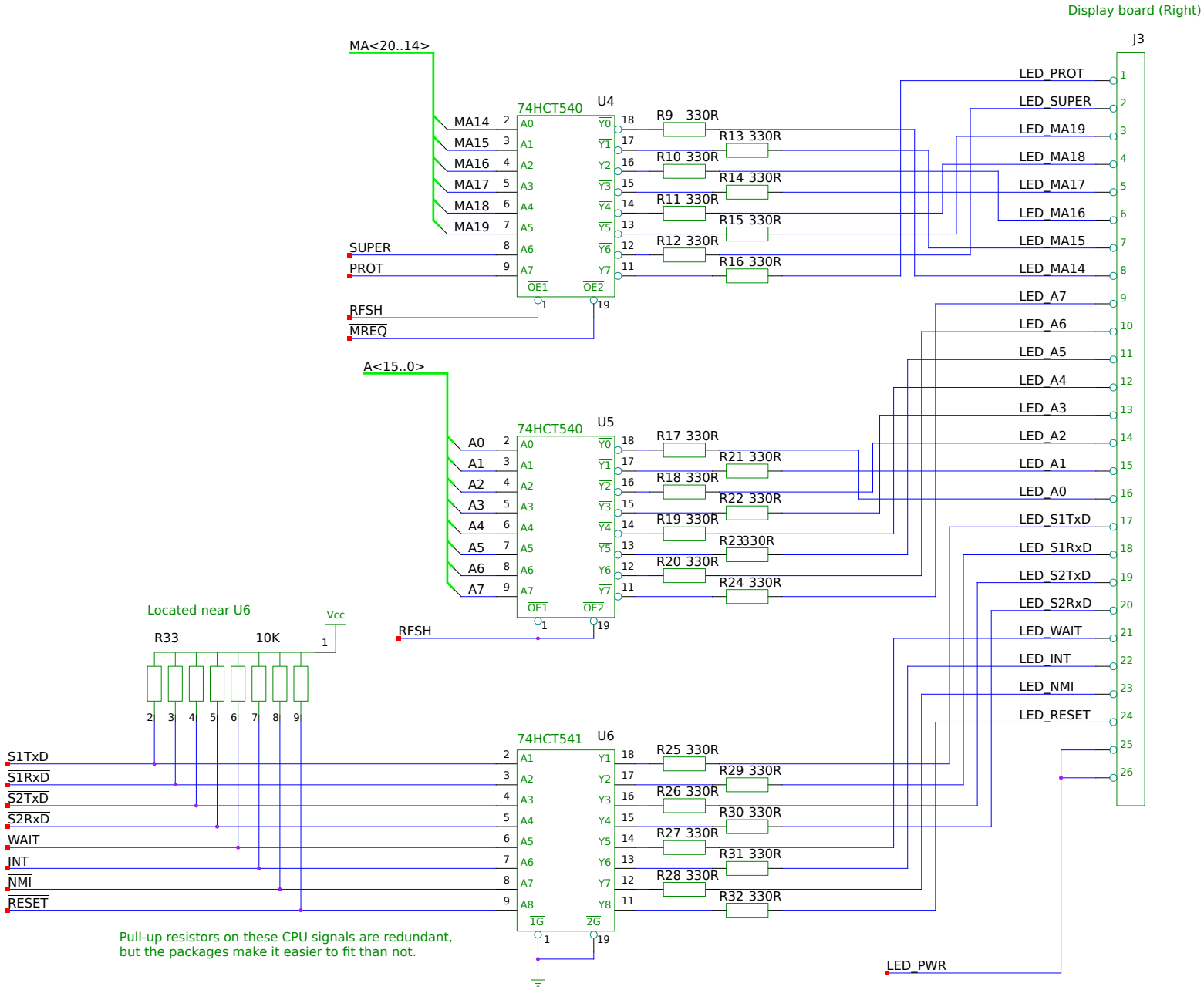

ZARC Front Panel LED Drivers (1 of 2)

TITLE

FILE: Z80_3.sch

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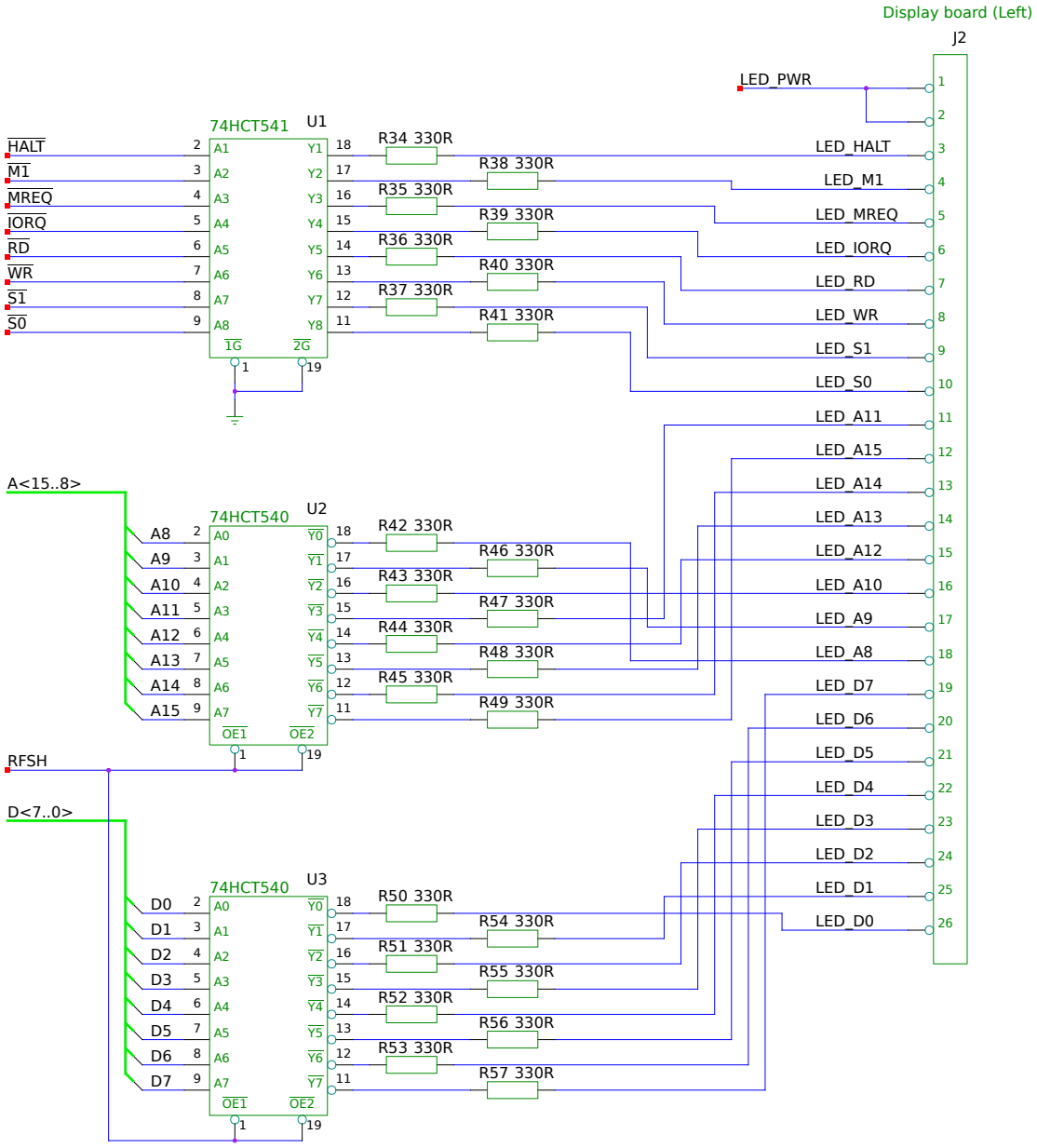

ZARC Front Panel LED Drivers (2 of 2)

TITLE

FILE: Z80_4.sch

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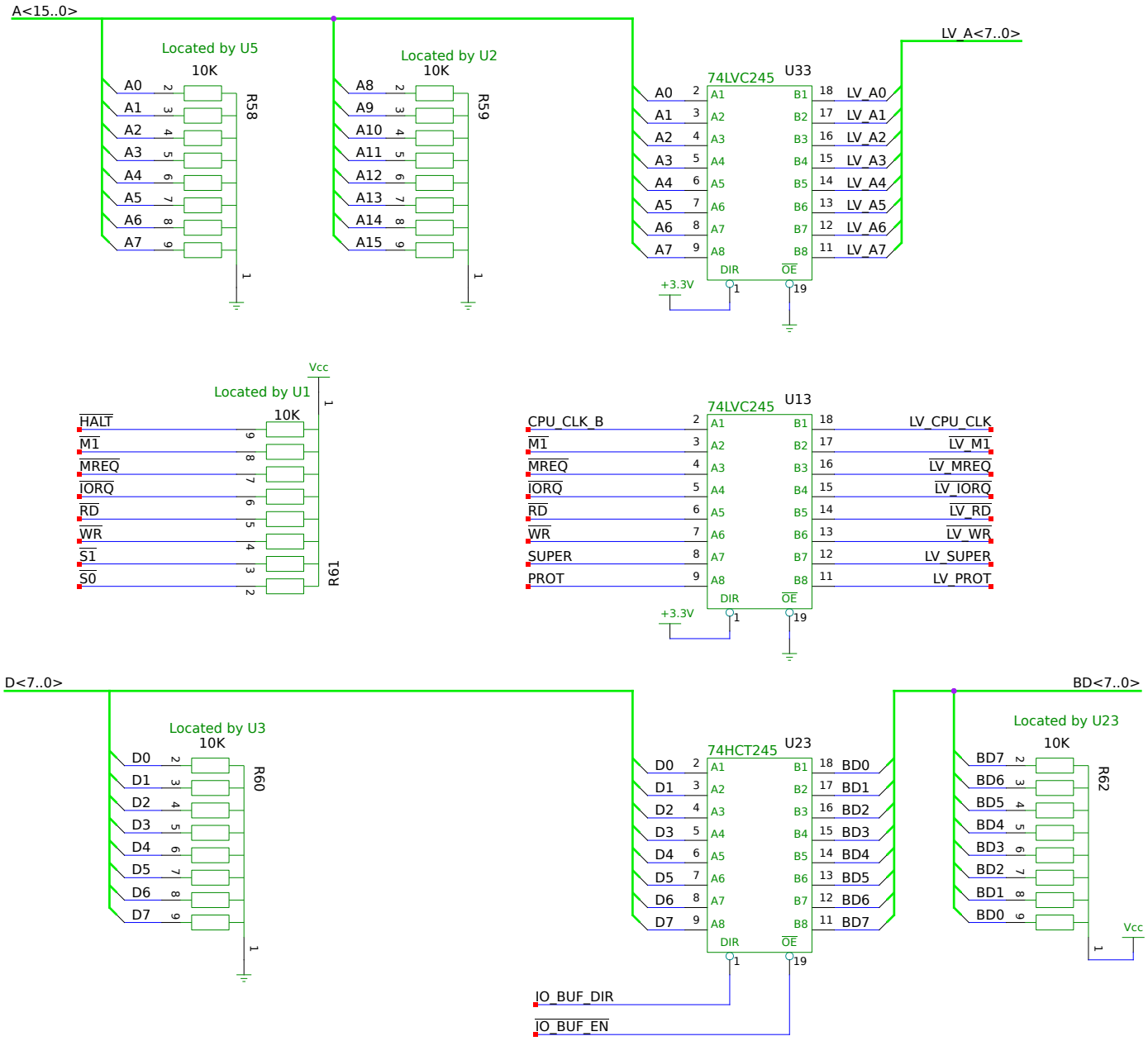

ZARC I/O Bus Buffers
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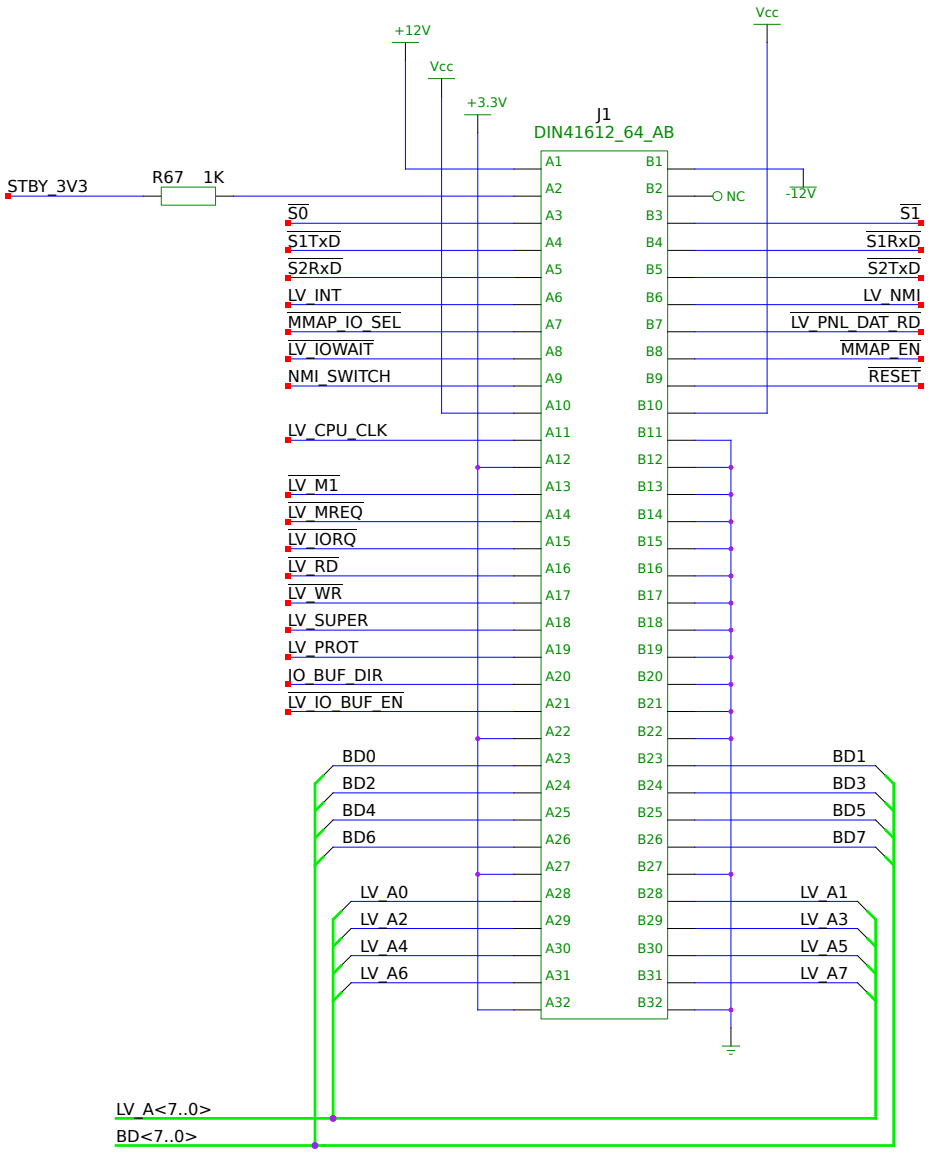

ZARC I/O Board Connector
TITLE

FILE: Z80_6.sch
REVISION: 8/3/2019
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