Chapter 5 - Group 04

5.3.1 Implement the Input Buffer

Q. The use of the flipflops has a disadvantage for the reaction rate of the system. What is that disadvantage and why does it occur?

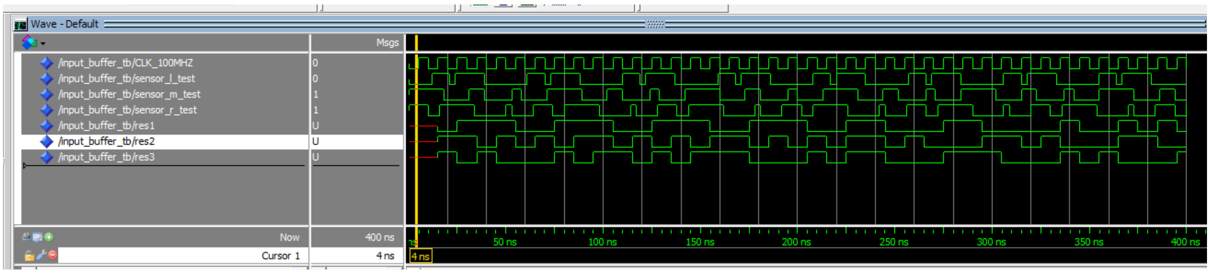
A. Instead of the sensor inputs directly fed to the controller the values are now only updated on the rising edge of the clock with a delay of 1 clock cycle. Since there are two registers placed in series. This also means that the output would become 1 or 0 for a clock cycle even though the value of the input was only on that level for a very short period of time (shorter than the clock cycle) . This delay may cause the robot to react too late to a change in the sensor value.

Q. Is it likely this will be a problem in the robot?

A. No, since the sensor inputs don’t change that often compared to the duration of a clock cycle.

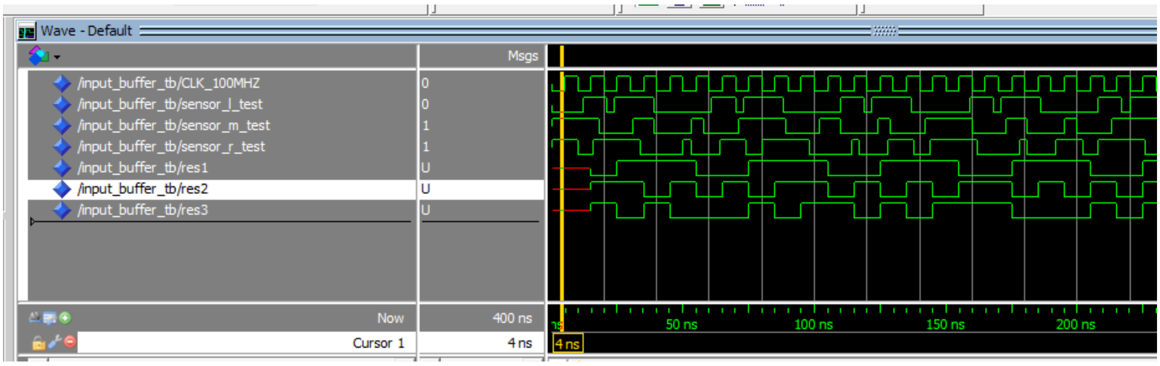
Testbench explanation

A. By creating processes of randomized values and delays for the individual sensor input test values we can check if the behaviour is as expected. We can clearly see the 1 clock cycle delay as well as short spikes in the input signal (way shorter than the clock cycle) right at the rising edge holding or switching the output unexpectedly.



Wave - Default

	Msgs
/input_buffer_tb/CLK_100MHZ	0
/input_buffer_tb/sensor_l_test	0
/input_buffer_tb/sensor_m_test	1
/input_buffer_tb/sensor_r_test	1
/input_buffer_tb/res1	U
/input_buffer_tb/res2	U
/input_buffer_tb/res3	U
Now	400 ns
Cursor 1	4 ns



Wave - Default

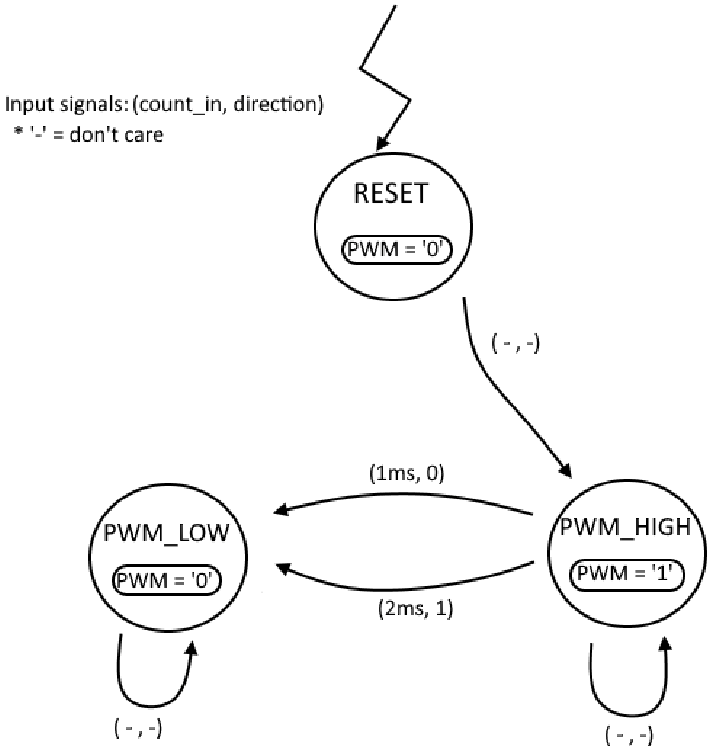
	Msgs
/input_buffer_tb/CLK_100MHZ	0
/input_buffer_tb/sensor_l_test	0
/input_buffer_tb/sensor_m_test	1
/input_buffer_tb/sensor_r_test	1
/input_buffer_tb/res1	U
/input_buffer_tb/res2	U
/input_buffer_tb/res3	U
Now	400 ns
Cursor 1	4 ns

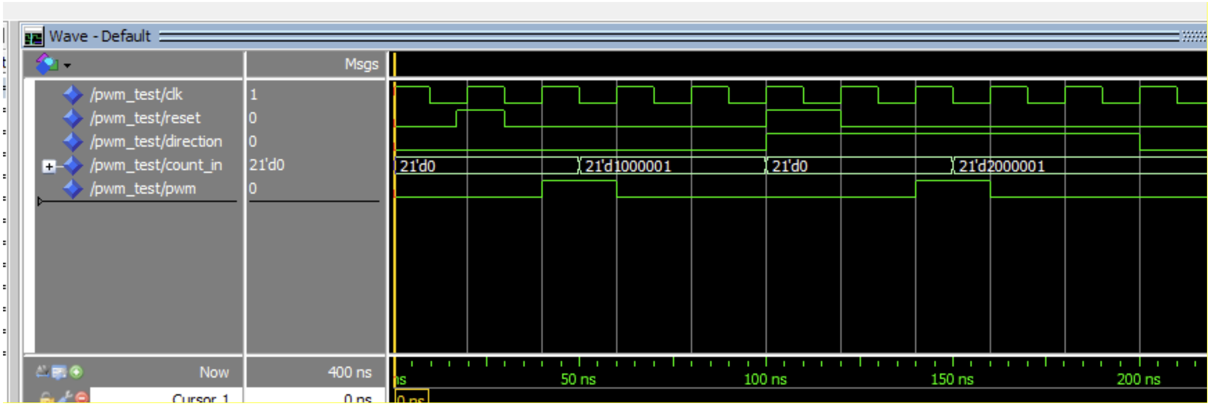
You can see in this example here on 115 ns that the value of sensor_r_test is very shortly 1 and since this is at the time the clock updates, res3 , which is the sensor_r_out value of the input_buffer, is 1 for a clock cycle.

5.3.2 Design and implement the PWM generator

FSM of PWM generator
frequency signal = 50 Hz, hence one period is 20 ms, 5-10% duty cycle, so pulse width becomes 1-2 ms. If the pulse duration is shorter than 1.5 ms, then the motor turns left. If longer, then the motor turns right.

FSM diagram:
After the reset is hit we switch from the reset state to the PWM_HIGH state. We are now generating the pulse. Depending on the ‘direction’ signal we switch to PWM_LOW at either 1ms or 2ms. We stay in the PWM_LOW state until the reset is hit again at the end of the 20ms period.





	Msgs
/pwm_test/clk	1
/pwm_test/reset	0
/pwm_test/direction	0
/pwm_test/count_in	21'd0
/pwm_test/pwm	0

From the picture above it can be seen that the PWM generator works as intended. When the reset is triggered the PWM generator goes to its reset state and the output is 0. One clock cycle after the reset goes back to 0 the state is PWM_HIGH with output 1. While direction is 0, this state is held until the counter reaches 1*10^6 (1 ms) and at the next rising edge of the clock the state goes to PWM_LOW with output 0. After another reset cycle the generator goes through its reset state to PWM_HIGH with output 1. While direction is 1, this state is held until the counter reaches 2*10^6 (2 ms). After the 2 ms the state goes to PWM_LOW and waits until the next reset.

5.3.3 Test the PWM generator

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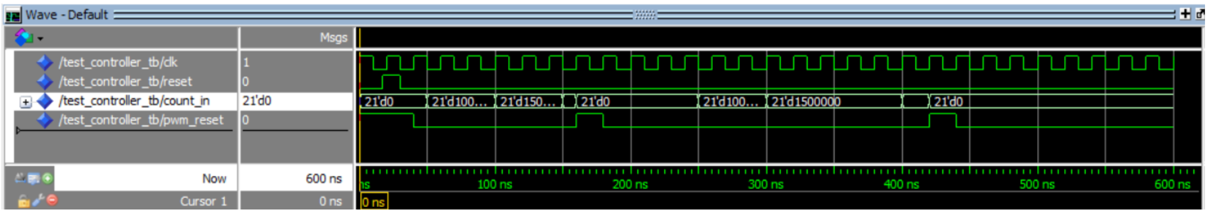
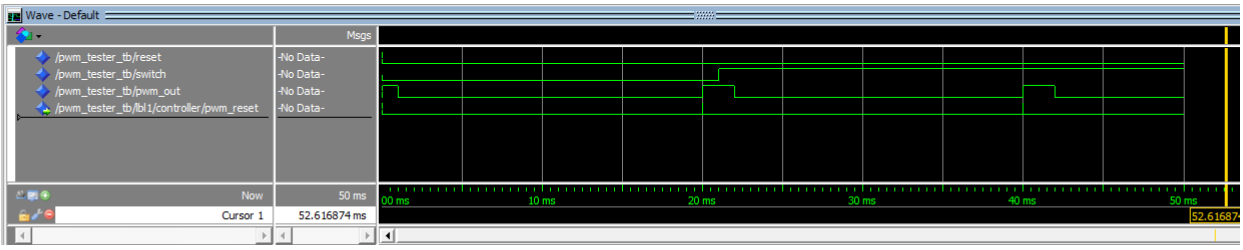


From the picture above it can be seen that the test controller works as intended. The first state is the reset state with output pwm_reset is 1. After the reset is set to 0 the test controller goes to its wait state with output pwm_reset = 0. It will stay in this state until count_in reaches 2*10^6. After it reaches 2*10^6 the whole cycle starts over again.


Wave - Default
Msgs
/pwm_tester_tb/reset -No Data-
/pwm_tester_tb/switch -No Data-
/pwm_tester_tb/pwm_out -No Data-
/pwm_tester_tb/lbl1/controller/pwm_reset -No Data-
Now 50 ms
Cursor 1 52.616874 ms
00 ms
10 ms
20 ms
30 ms
40 ms
50 ms
52.61687

From the picture above it can be seen that the test of the full system works as intended. There is a reset spike every 20ms and when switch is 0, the PWM pulse is 1ms and when switch is 1 the PWM pulse is 2ms.