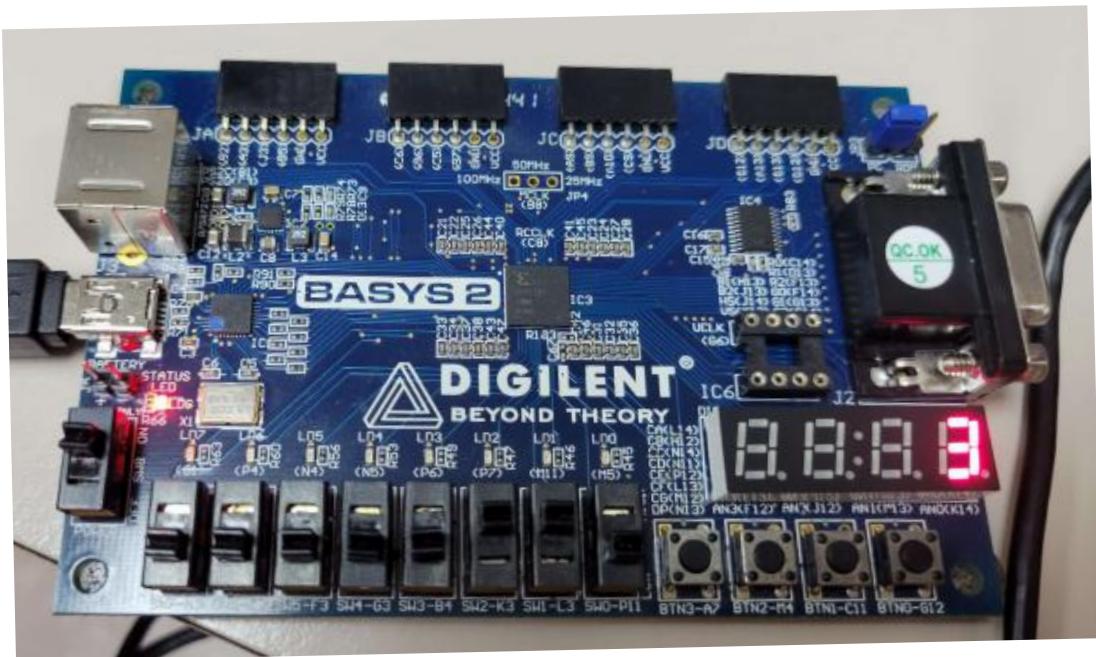
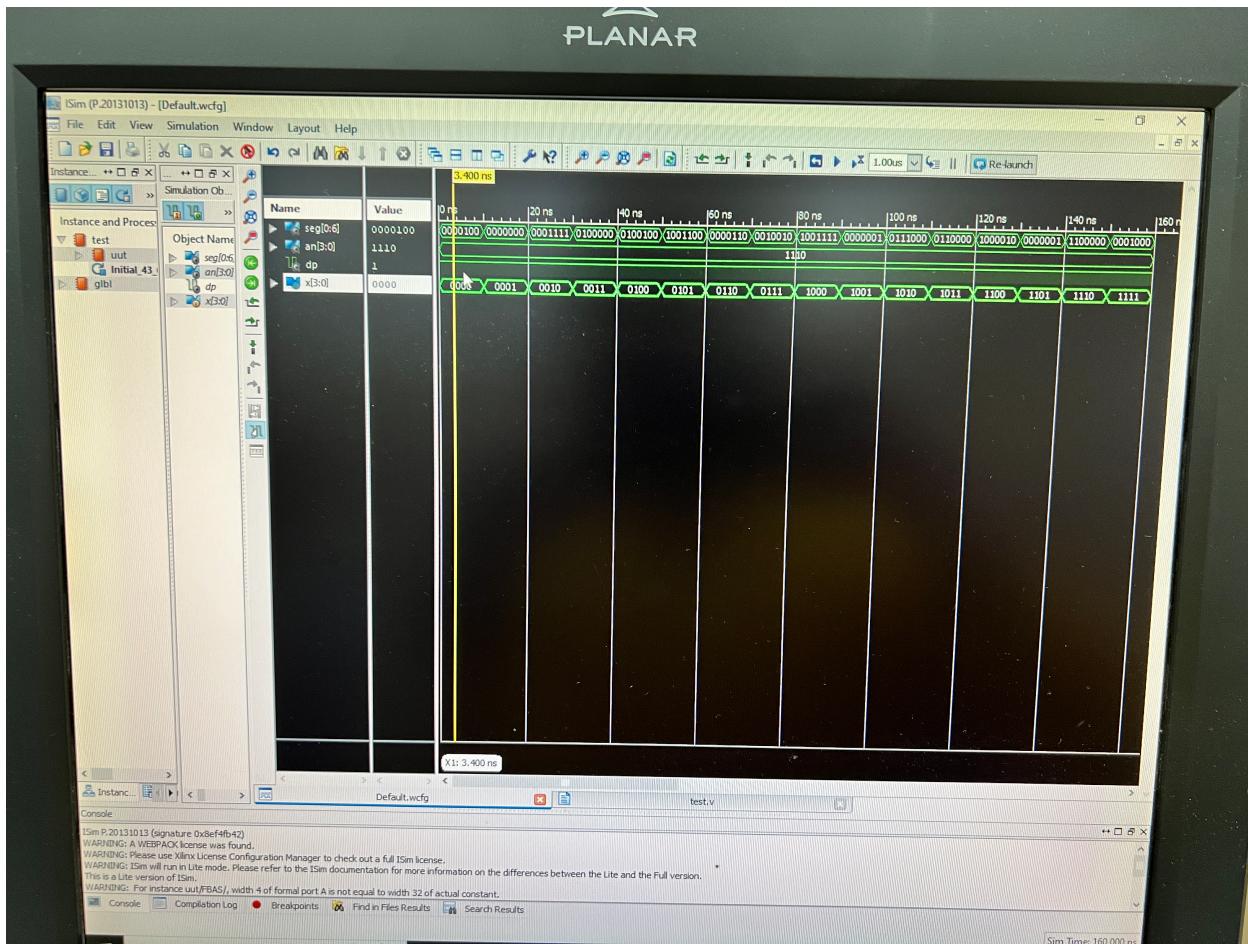


Lab 9 Classwork



Homework 9. <https://edaplayground.com/x/eZSA>

The screenshot shows the edaplayground.com web interface. At the top, there's a navigation bar with links for Chrome, File, Edit, View, History, Bookmarks, Profiles, Tab, Window, Help, and a date/time stamp (Tue Apr 25 12:35 PM). Below the navigation bar is a toolbar with icons for Run, Save, Copy, and other EDA tools.

The main area contains two code editors:

- testbench.sv**:
A Verilog testbench module. It includes a monitor for inputs A and B, and a loop that increments A from 0 to 15 and monitors the result. The code is as follows:

```
1 // Code your testbench here           SV/Verilog Testbench
2 // or browse Examples
3 module test;
4   reg [3:0]A;
5   wire [3:0]B;
6   BCD2Excess3 uut(A, B);
7   initial
8     begin
9       $dumpfile("dump.vcd"); $dumpvars(1,
10      test);
11      $monitor("A=%b;B=%b",A,B);
12      #10 A='b0001;
13      #10 A='b0010;
14      #10 A='b0011;
15      #10 A='b0100;
16      #10 A='b0101;
17      #10 A='b0110;
18      #10 A='b0111;
19      #10 A='b1000;
20      #10 A='b1001;
21    end
22 endmodule
```
- design.sv**:
A Verilog design module. It defines a four-bit adder U4 and a BCD2Excess3 module. The code is as follows:

```
40   wire [3:0] D; //Output of X0           SV/Verilog Design
41
42   xor U0(D[0], B[0], M);
43   xor U1(D[1], B[1], M);
44   xor U2(D[2], B[2], M);
45   xor U3(D[3], B[3], M);
46
47   four_bit_adder U4(S, C, A, D, M);
48
49
50 endmodule
51
52
53
54
55 module BCD2Excess3(A, B);
56   input [3:0] A;
57   output [3:0] B;
58   wire C4;
59
60   adder_subtractor AS(B, C4, A, 3, 0);
61
62 endmodule
63
```

Below the code editors are buttons for Log, Share, and Save. The URL in the address bar is https://edaplayground.com/x/eZSA, and the page title is Lab9homework. There are 0 views and 0 likes.

