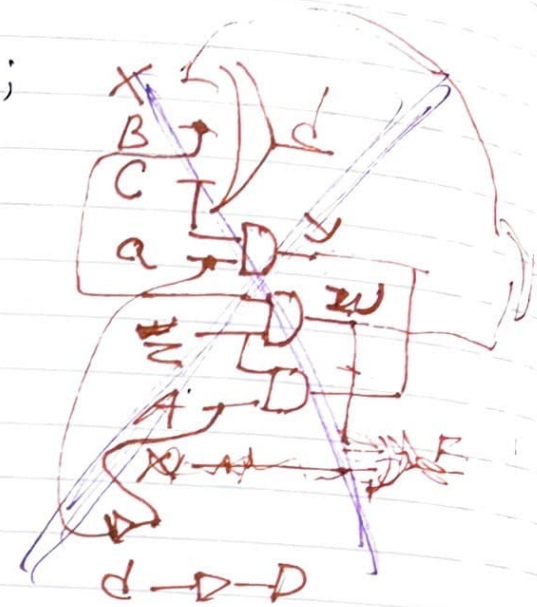
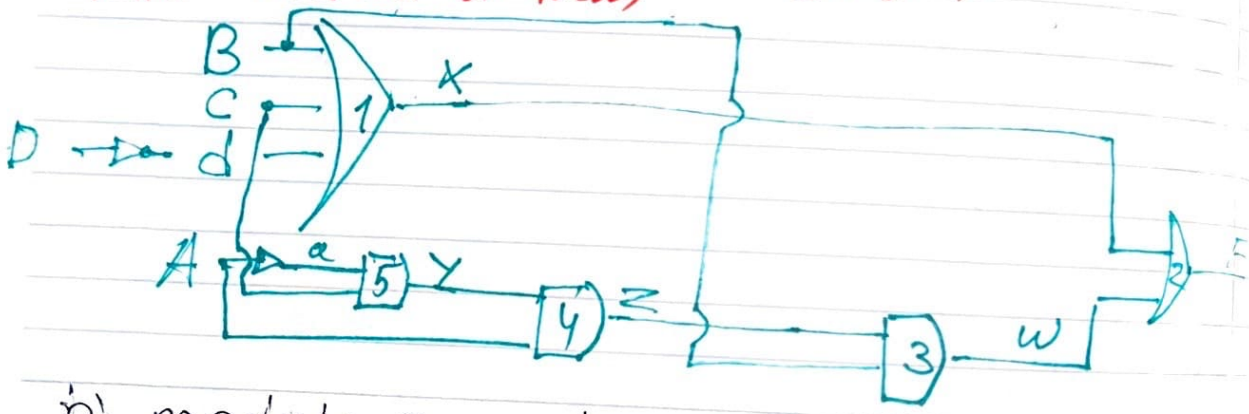
Homework 4.

1. Draw [illegible] diagram of digital circuit specified by the following Verilog description.

```
module circuit_A (A, B, C, D, F)
  input A, B, C, D;
  output F;
  wire w, x, y, z, a, d;
1 or  (x, B, C, d);
5 and (y, a, d);
3 and (w, z, F);
4 not (z, y);
2 or  (F, x, w);
  not (a, A);
  not (d, D);
endmodule
```

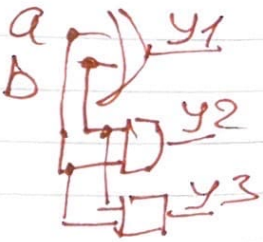


Here first is output letter in all of them



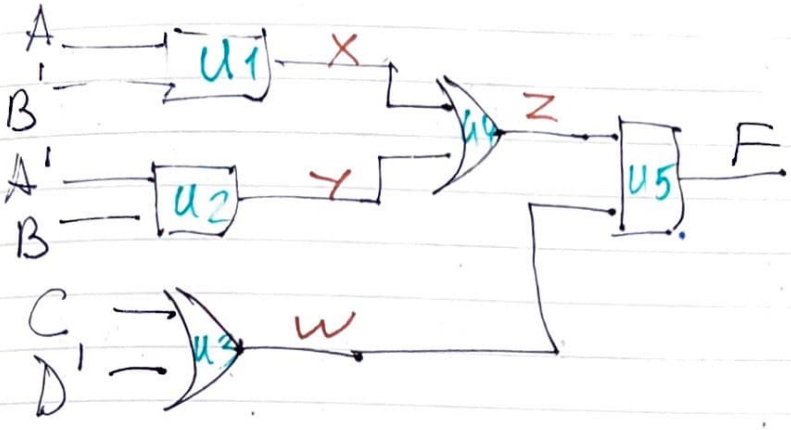
b) module circuit_B (y1, y2, y3, a, b)

```
output y1, y2, y3;
input a, b;
assign y1 = a || b;
and (y2, a, b);
assign y3 = a && b;
end module
```



Here we assign right hand side expression to y3.
It's data flow.

2. a) Write a Verilog description of the circuit shown below,




```
module something(F, A, B', A', B, C, D');
    input A, A', B, B', C, D';
    output F;
    wire X, Y, Z, W;
    and U1(X, A, B');
    and U2(Y, A', B);
     or U3(W, C, D');
     or U4(Z, X, Y);
    and U5(F, Z, W);
endmodule
```

b) write a verilog description of the circuit specified by the following Boolean functions: $Z = (A + B')C'(C + D)$

```
module h(Z, A, B', C', C, D);
    input A, B', C', C, D;
    output Z;
    assign Z = (A | B') & C' & (C | D);
endmodule
```

Data flow

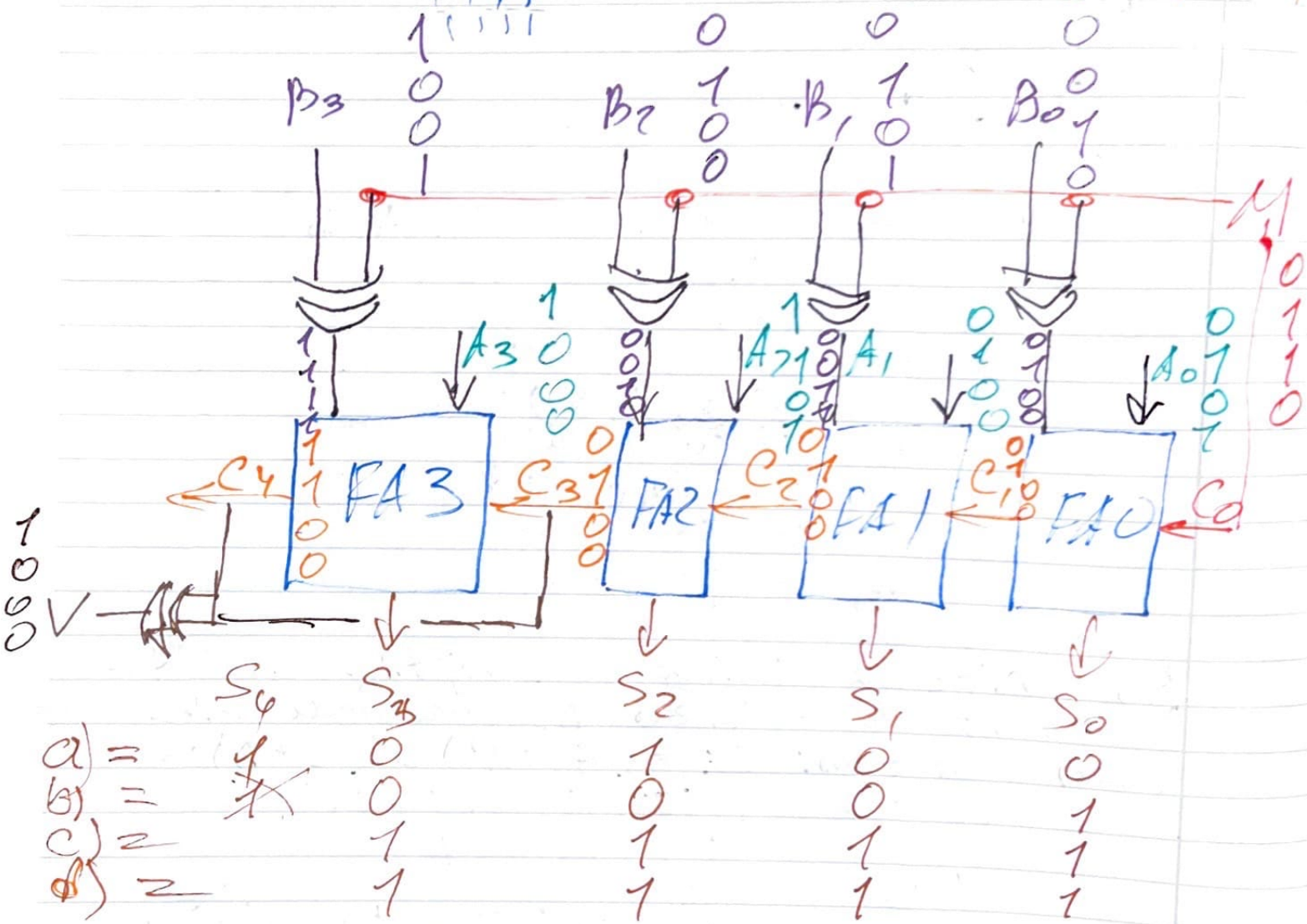
3: The adder - subtractor has the following

a) M=0 A 1100 = 12
B 1000 = 8
10000 : 20

b) M=1 A = 0111 = 7
B = 0110 = 6
1101 = -3

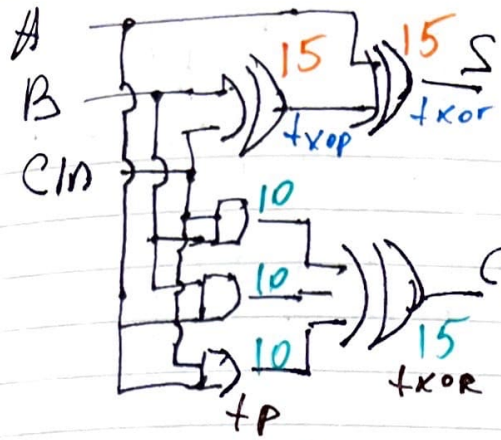
c) M=1 A = 0000
B = 0001
1110
1111

d) M=0 0101 = 5
1010 = 10
1111
1001 = -7
1010
10001 = 1



	S4	S3	S2	S1	S0
a) =	1	0	1	0	0
b) =	~~1~~	0	0	0	1
c) =		1	1	1	1
d) =		1	1	1	1

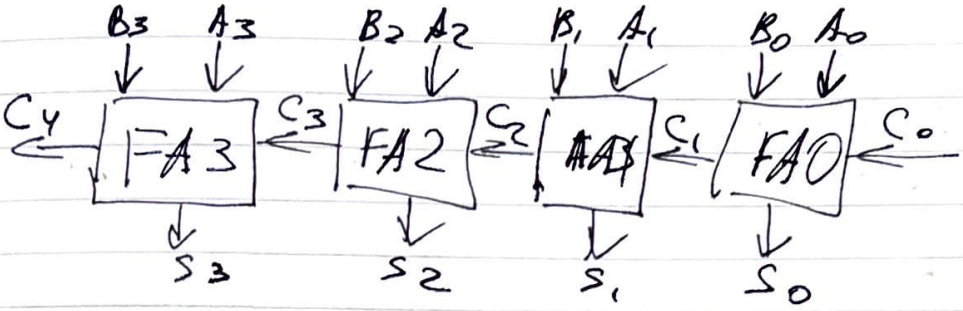
4) Propogation delay: XOR = 15 ns, AND and OR = 10 ns. a) What is propagation delay time of following 1-bit full adder, b) 4-bit ripple carry adder build using 1-bit full adder; c) 4 bit carry lookahead adder

a) 

$t_S = 2 \cdot t_{XOR} = 30\ ns$

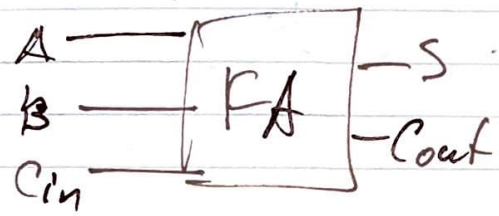
$t_{Cout} = t_p + t_{XOR} = 25\ ns$

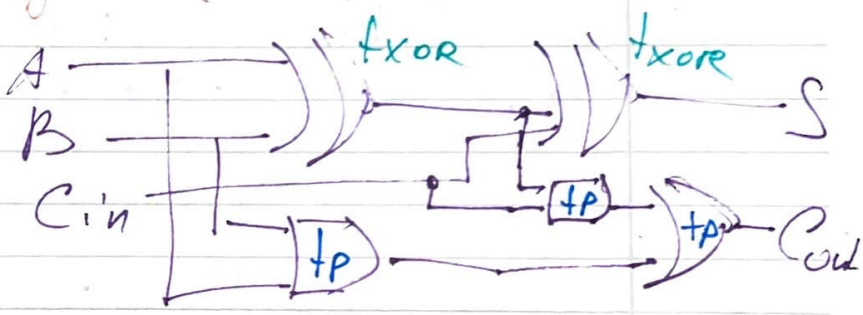
3

b) 

Total Propogation Delay for Sum output = $(n-1)t_c + t_c$

Total Propogation Delay for Carry Output = $n t_c$





$t_S = 4 \cdot 30 = 120\ ns$

$t_c = 3 \cdot 35 + 35 = 140\ ns$

$S = 2 \cdot t_{XOR} = 30$

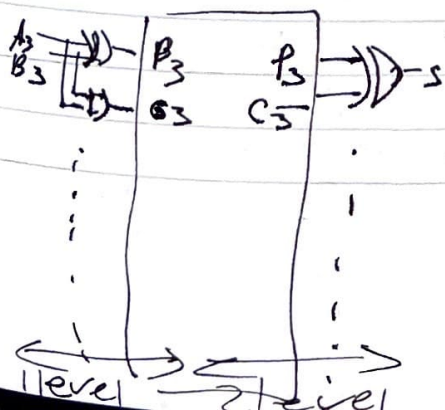
$Cout = t_{XOR} + 2t_p = 35$

$S_2 = (t_{XOR} + 2t_p) + t_{XOR}$, $C_2 = (t_{XOR} + 2t_p) + 2t_p$

Stable Carry output $C_4 = t_{XOR} + 2 \cdot 4 \cdot t_p = 15 + 80 = 95$

Stable Sum outp $S_4 = 2t_{XOR} + 2(4-1) \cdot t_p = 30 + 60 = 90$

c) Propogation Delay of Look Ahead Adder is faster than Ripple Head adder because it is only 2 level gates.



Based on RHA logic circuit we getting S and Cout and multiply by 2.

$t_S = 2 \cdot S = 2 \cdot 30 = 60ns$

$t_c = 2 \cdot Cout = 2 \cdot 35 = 70ns$

5) $F = A' \cdot \overline{A \cdot D} \cdot (\bar{A} + BC)$

$F = A' \cdot (A + D') \cdot (\bar{A} + BC)$

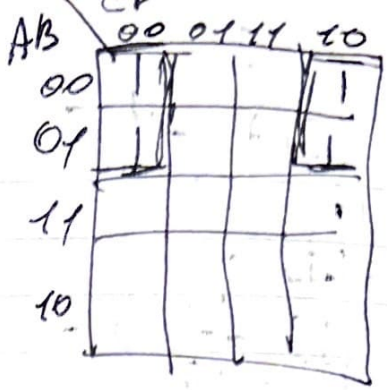
$F = \bar{A} \cdot A + \bar{A} \cdot D' \cdot (\bar{A} + BC)$

$F = \bar{A} A \bar{D} + \bar{A} D BC$

$F = \bar{A} \bar{D} + \bar{A} BC \bar{D}$

$F = \bar{A} \bar{D} (1 + BC)$

$F = \bar{A} \bar{D}$



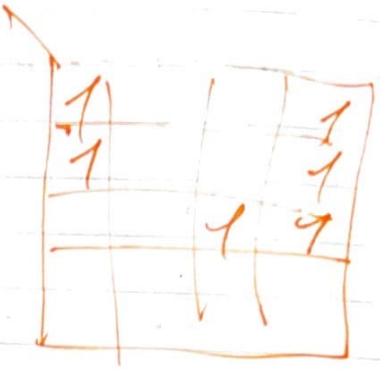
$G = (\bar{A} + BC)(\overline{\bar{A} D})$

$G = \bar{A} \overline{\bar{A} D} + \overline{\bar{A} D} BC$

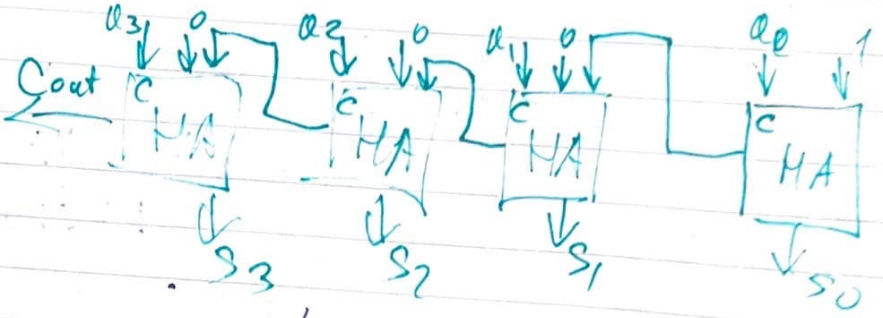
$G = \bar{A}(A + \bar{D}) + (A + \bar{D}) BC$

$G = 0 + \bar{A} \bar{D} + ABC + BC\bar{D}$

$G = \bar{A} \bar{D} + ABC$

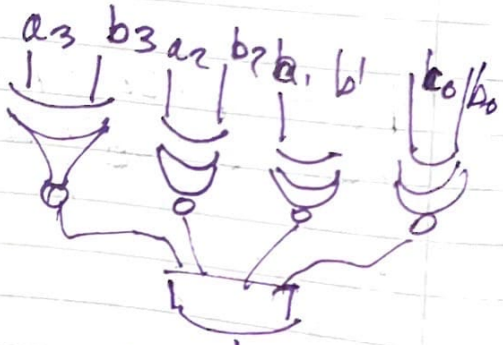


6)



7)

A	B	XOR	XNOR
0	0	0	1
0	1	1	0
0	0	1	0
1	1	0	1



$E = (a_3 \oplus b_3)' (a_2 \oplus b_2)' (a_1 \oplus b_1)' + (a_0 \oplus b_0)'$

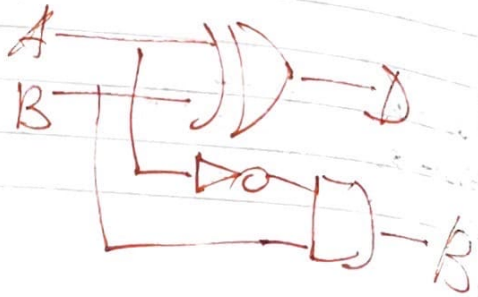
8) half subtractor

x	y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

x \ y	0	1
0	0	1
1	1	0

$D = x'y + xy' =$

$= x \oplus y$



$B = x'y$

0	1
0	0

b) Full Subtractor

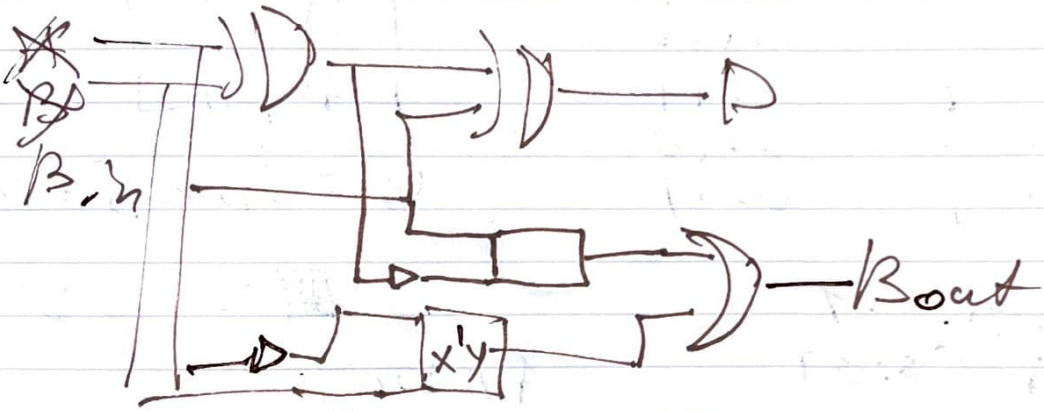
x	y	Bin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

x \ yBin	00	01	11	10
0		1	0	1
1	1	0	1	0

$D = x'y'B_{in} + x'yB_{in} + xy'B_{in}' + xyB_{in} = x \oplus y \oplus B_{in}$

0	1	1	1
0	0	1	0

$B_{out} = x'B_{in} + x'y + yB_{in} = x'y + B_{in}(x \oplus y)'$



g)

x	y	z	A	B	C
0	0	0	0	1	0
0	0	1	0	1	1
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	0	0	1
1	0	1	0	1	0
1	1	0	0	1	1
1	1	1	1	0	0

x \ yz	0	1
00		
01	1	1
11	1	1
10		

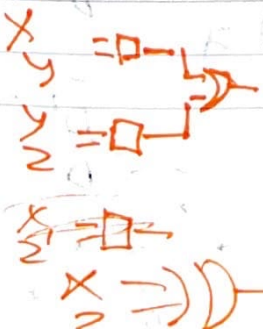
$A = \bar{x}y + yz$

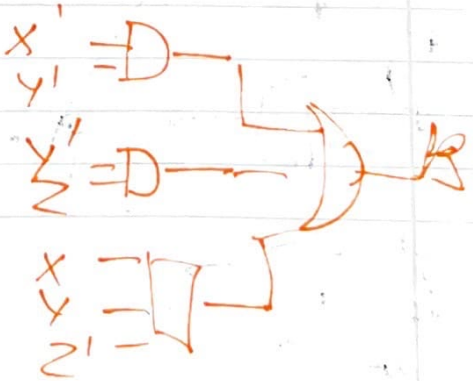
x \ yz	0	1
00	1	1
01	1	
11		1
10		1

$B = x'y' + y'z + xyz'$

x \ yz	0	1
00		1
01		1
11	1	
10	1	

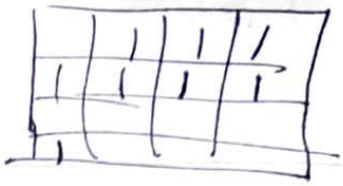
$C = xz + x'z = x \oplus z$





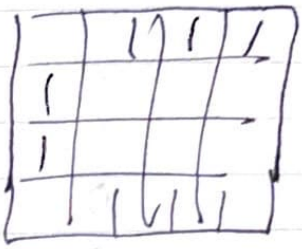
Input output

A	B	C	D	w	x	y	z
0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0
0	0	1	1	1	1	0	1
0	1	0	0	1	1	0	0
0	1	0	1	1	0	1	1
0	1	1	0	1	0	1	0
0	1	1	1	1	0	0	1
1	0	0	0	1	0	0	0
1	0	0	1	0	1	1	1
1	0	1	0	0	1	1	0
1	0	1	1	0	1	0	1
1	1	0	0	0	1	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	0	1	0
1	1	1	1	0	0	0	1



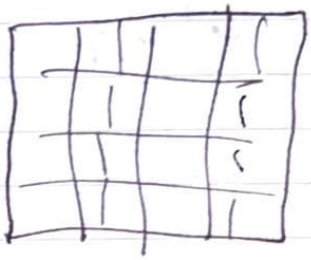
w

$w = \bar{A}D + A'C + A'B + AB\bar{C}\bar{D}$



x

$x = B\bar{D} + B\bar{C} + B\bar{C}\bar{D}$



y

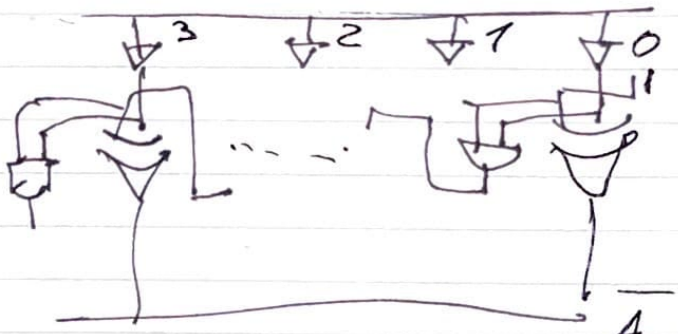
$y = \bar{C}D + C\bar{D} = C \oplus D$

z $z = D$

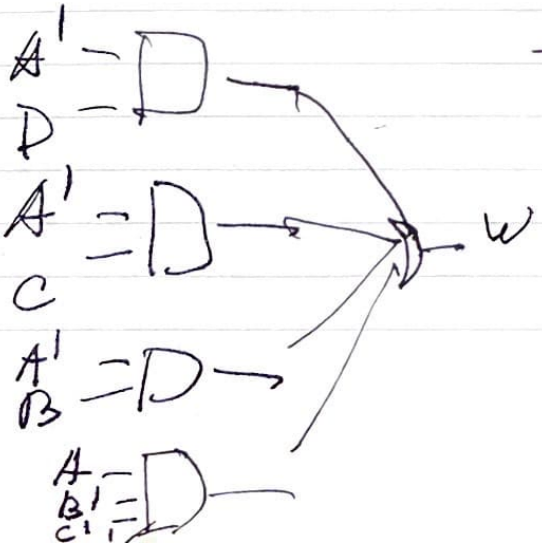
Input +1

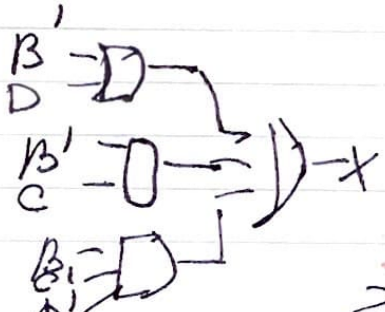
A [3:0]

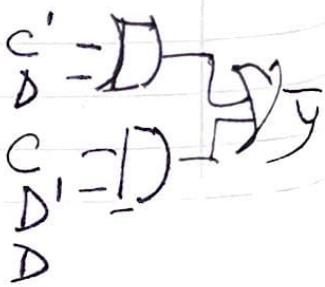
A [3:0]



$\bar{A} + 1$







z = D