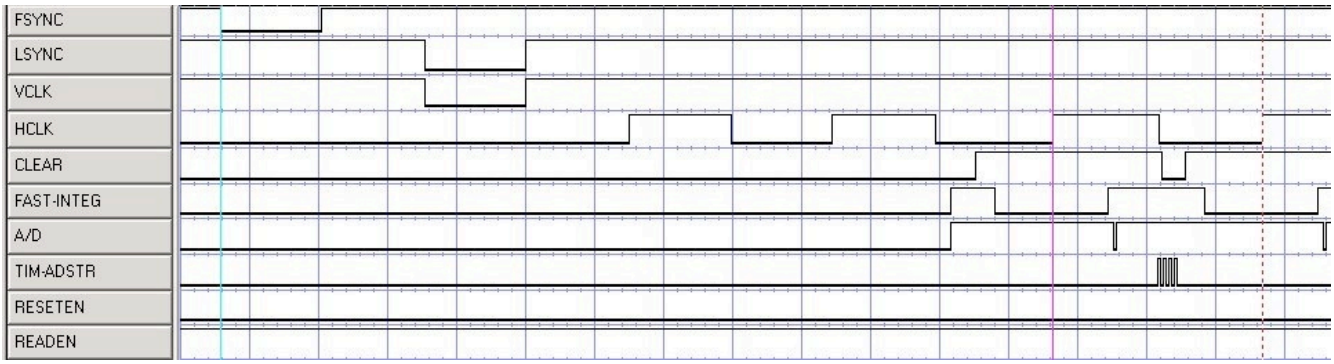
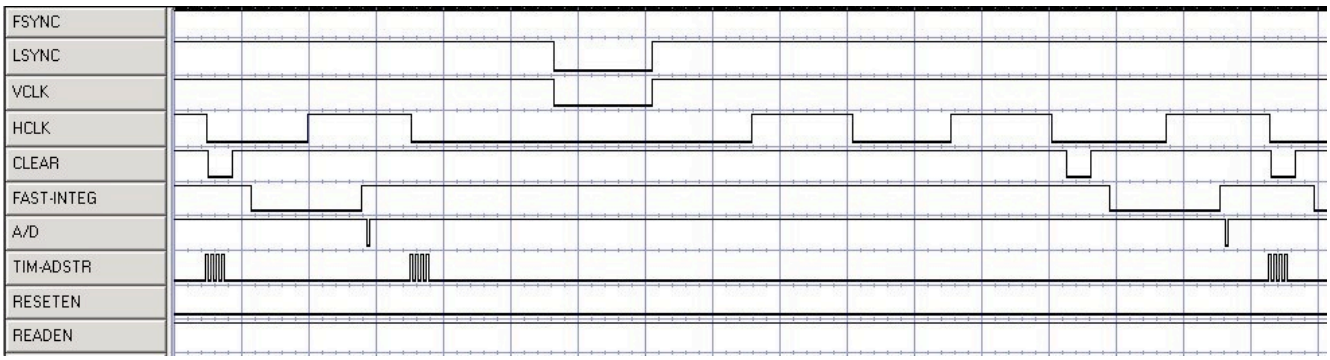
H2RG Controller, April 2012

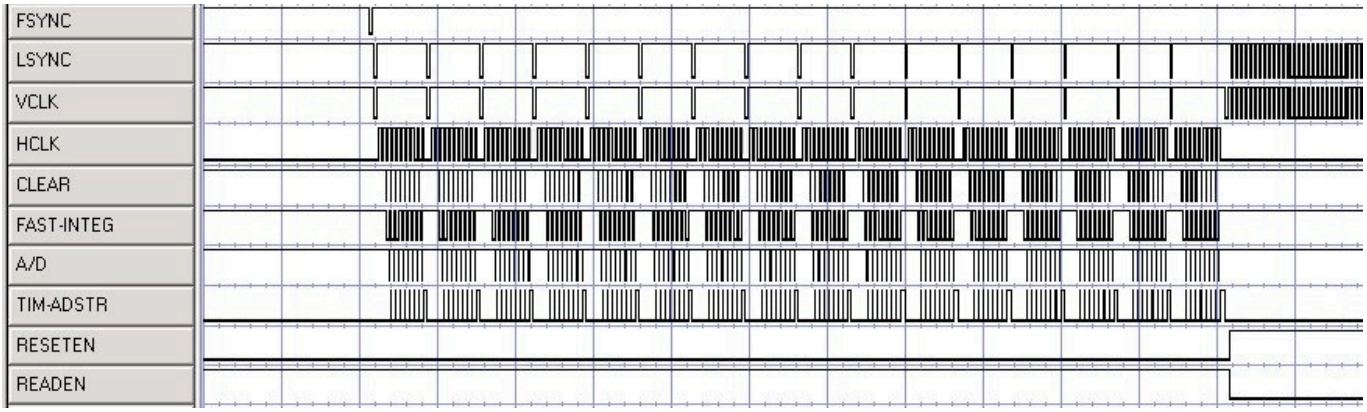
Timing diagrams for reading out the H2RG sensor are shown in the first few figures. The first one shows the beginning of the array readout with the low trued assertion of the frame sync clock FSYNC that resets the vertical multiplexer position to the beginning of the array. It is followed by the line sync clock LSYNC that resets the horizontal multiplexer to the beginning of the row. The signal HCLK advanced the horizontal multiplexer, with the first pixel value becoming valid only after its second falling edge. The video processing consists of the sequence of resetting the signal integrator on the video board (CLEAR), integrating the signal while the FAST-INTEG signal is low, initiating the A/D conversion on the low going edge of A/D and then transferring four channels of pixel data between the vide processor and timing boards of the controller.



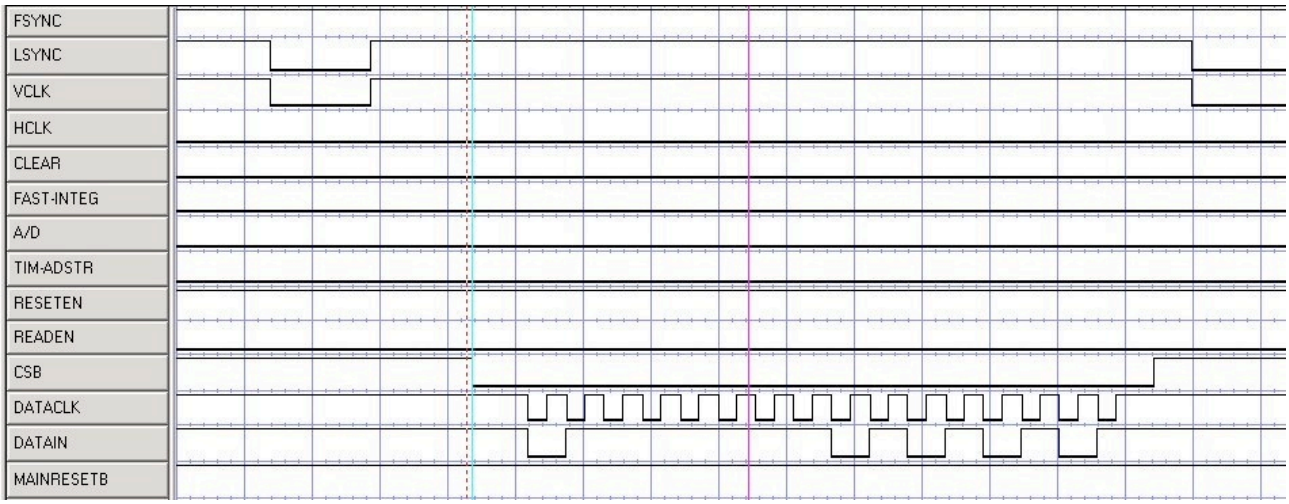
The next line is read after both the LSYNC and VCLK signals advance the multiplexer. Note that there are two HCLK pulses that do not produce pixel data, one at the beginning of the line and one at the end. Also note that the array reset enable signal RESETEN is disabled low false and the read enable signal READEN is asserted high true during readout.



The behavior of these two enable lines is further illustrated in the next figure where the number of rows and columns read out are set to small values to show the clock behavior throughout the readout. The READEN signal is asserted during readout and de-asserted as soon as readout is completed. Similarly, the RESETEN line is asserted high true after readout as the array is clocked in continuous line-by-line reset mode by the LSYNC and VCLK signals. During continuous reset the controller monitors the incoming fiber optic command port for commands from the host computer.



Serial commands can be transmitted to the H2RG internal registers over its three wire serial interface. The Chip Select Bar (CSB) signal is driven low to select the serial interface, and data is loaded from DATAIN on high-going transitions of DATACLK. Shown is the 16-bit data value 0x8F55 being written, most significant bits first.



The time scale in the plot is one microsec per division, so writing the data word takes 10 microseconds. The signals LSYNC and VCLK, normally continuously resetting the array,

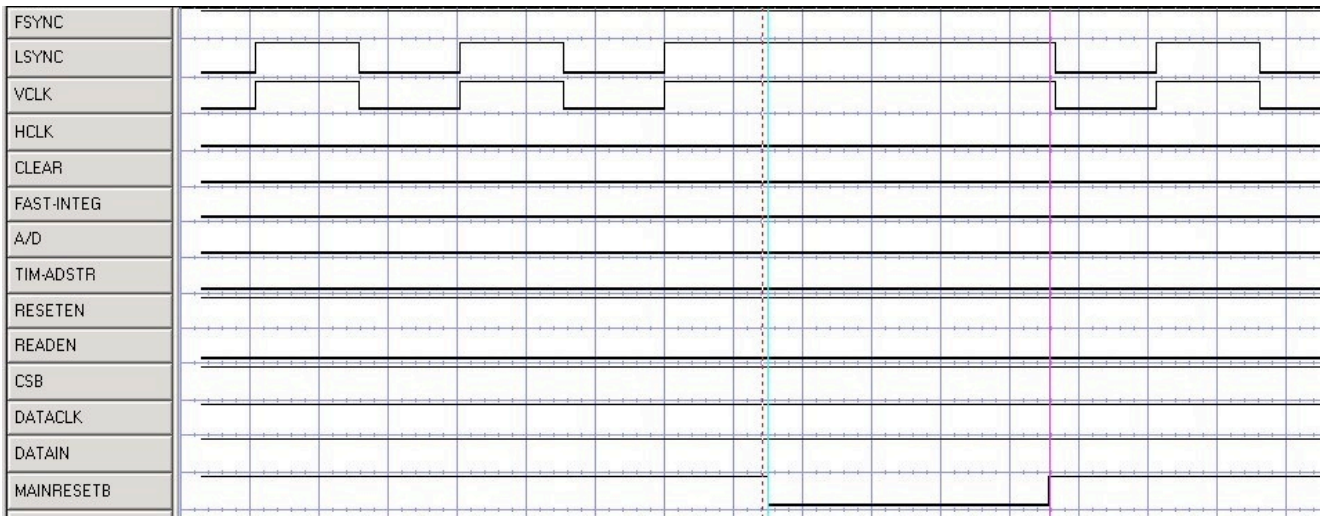
are inactive while the serial command is issued. The signal used to reset the internal register, MAINRESETB, is high. Serial words can be transmitted with the manual command "SER xxxx" in the "Owl" manual command window, or issued by the H2RG "Owl" script.

The serial register is reset to default values by bringing MAINRESETB low. This can be executed with the "Owl" manual command Reset Internal Registers "RIR" or in the H2RG "Owl" command script.

During the power-up sequence of the controller the serial register is initialized to non-default values with a short series of serial writes to designated registers. This is done in the INIT_H2RG routine in the "timIRmisc.asm" file, executed with the "Owl" manual command "INI" or in the H2RG "Owl" command script.

OUTPUT MODE	$04	32-output mode, use pin #7 for window output
OUTPUT BUFFER MODE	$11	Slow buffered readout mode
NORMAL MODE	$83	Enhanced clocking, global reset enabled
WINDOW MODE	$83	Enhanced clocking, global reset enabled

The H2RG array can be optionally reset before each exposure. This is done with the manual command Set Reset Mode, with "SRM 1" resetting the array, and "SRM 0" not resetting the array before each exposure. The resetting is implemented as a global reset, by asserting the RESETEN signal high and READEN signal low for 20 microsec. Alternatively, the H2RG script in "Owl" can be used to make the selection. Not resetting the array can be used to implement an "up-the-ramp" exposure and readout sequence.



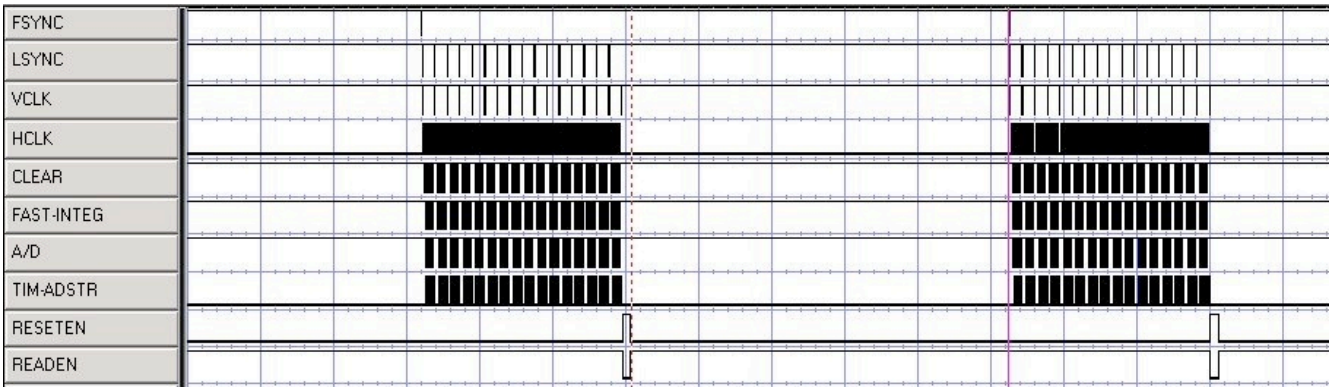
The default is to reset the array.

A delay can be imposed between clocking each line and beginning to read it. The command Set Read Delay "SRD ##" can be issued to delay by ## microseconds. The

default is to not delay. This command can be executed in the H2RG "Owl" script.

Similarly, correlated double sampling can be turned on with the command "CDS 1", or off with the command "CDS 0". Turning it on will cause a read of the array to occur after the array reset (if enabled) before the exposure, while a second identical read will occur after the end of the exposure. The image dimensions set in the setup window will be interpreted by the readout program to be the size of the combined images from each of the two readouts, so should be set to ncols = 2048 and nrows = 4096 for whole image readout of the H2RG array.

The number of readout channels can be selected from the allowed values for the H2RG sensor (1, 4, or 32), as well as for the value 8 (useful for isolating individual video processor boards). This is selectable with the command "SNC ##", or in the H2RG



script in "Owl". Note that the "Hawaii RG" de-interlacing routine in "Owl" reads the number of channels that was selected with the "RNC" command and properly de-interlaces the image. This works even for one channel, as the de-interlacing routine is simply bypassed.

One channel readout is a special case. If the number of channels is set to zero, but the native H2RG windowing is not selected (see below) then the channel that is read from can be selected with the command "SVC ##". This can be useful for sub array readout

where the user might select the best performing amplifier of the array, or for diagnostic and development tasks to generate images that have readout from only one channel of the H2RG sensor and one specified video channel of the electronics.

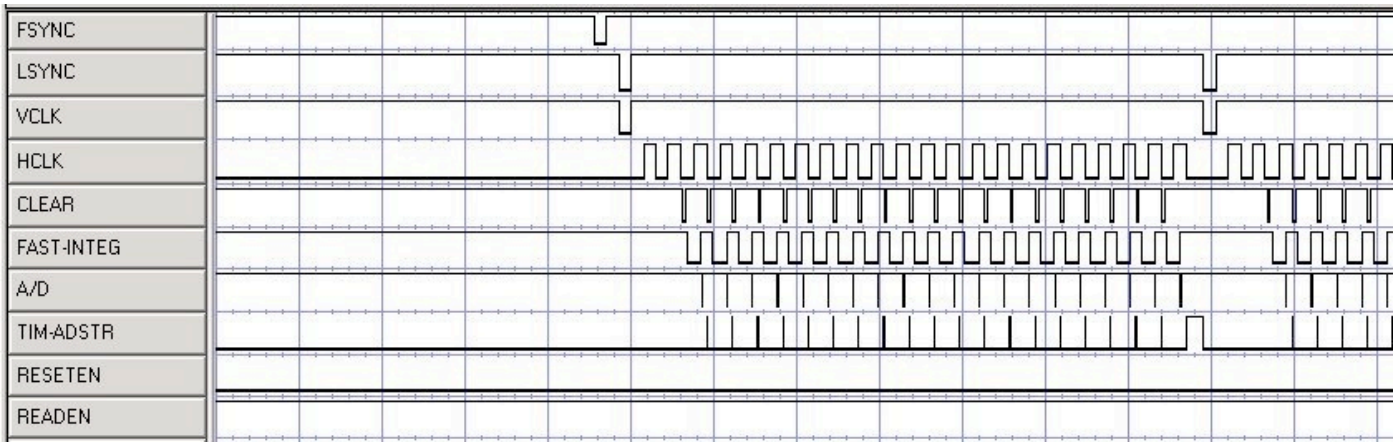
Sub-array or windowing readout is implemented in two ways. In the native H2RG mode the internal registers are written with the positions and sizes of the window to be read out, and the multiplexer clocks are exercised as many times as are indicated by the size of the window. The clocking to the window region is handled internally by the sensor. The controller clocks are shown below, resembling normal readout with fewer clocks: The video data is presented on only one channel, #7. This mode is selectable with the command "SWM 1", and de-selected with the command "SWM 0". The window sizes are entered with the Set Subarray Size command with three arguments, the first of which is not used, as follows:

SSS (not used) number_of_columns number_of_rows

The position of the window is set with the Set Subarray Position command, again with three arguments, with the third one not used:

SSP offset_number_of_rows offset_number_of_columns (not used)

These commands are adapted from CCD usage, which accounts for their awkwardness. The "Owl" subarray readout window may be used to enter these parameters, noting that several of the fields are not used because they apply to reading out the overscan (or bias) regions of CCDs.

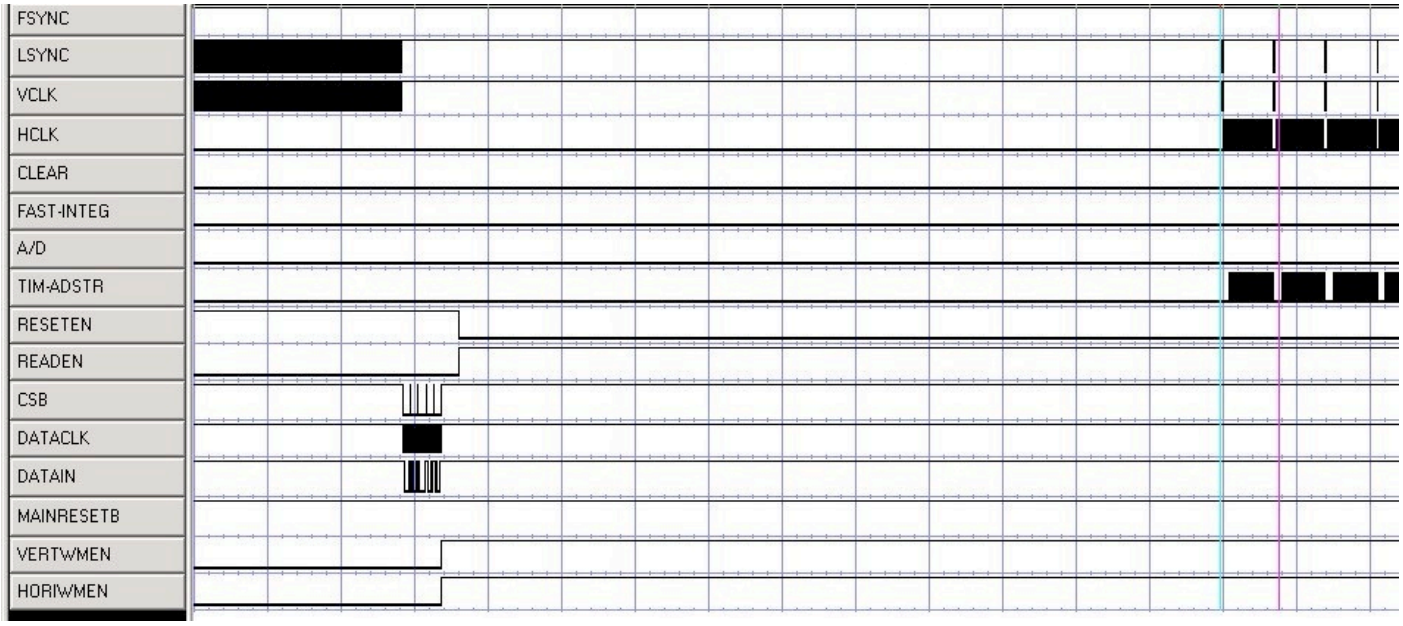


Native H2RG windowing mode is enabled in the readout code in two redundant ways. The signals HORIWMEN and VERWMEN signals are set high true to enable windowing mode in both direction if the "SWM 1" command is active. If these signals are wired from the clock driver to the H2RG array then the array will enter and exit windowing mode according to whether these signals are high or low. The second way of controlling

windowing mode is by having the controller issue commands to the serial register to enable or disable it whenever needed, by writing to the register:

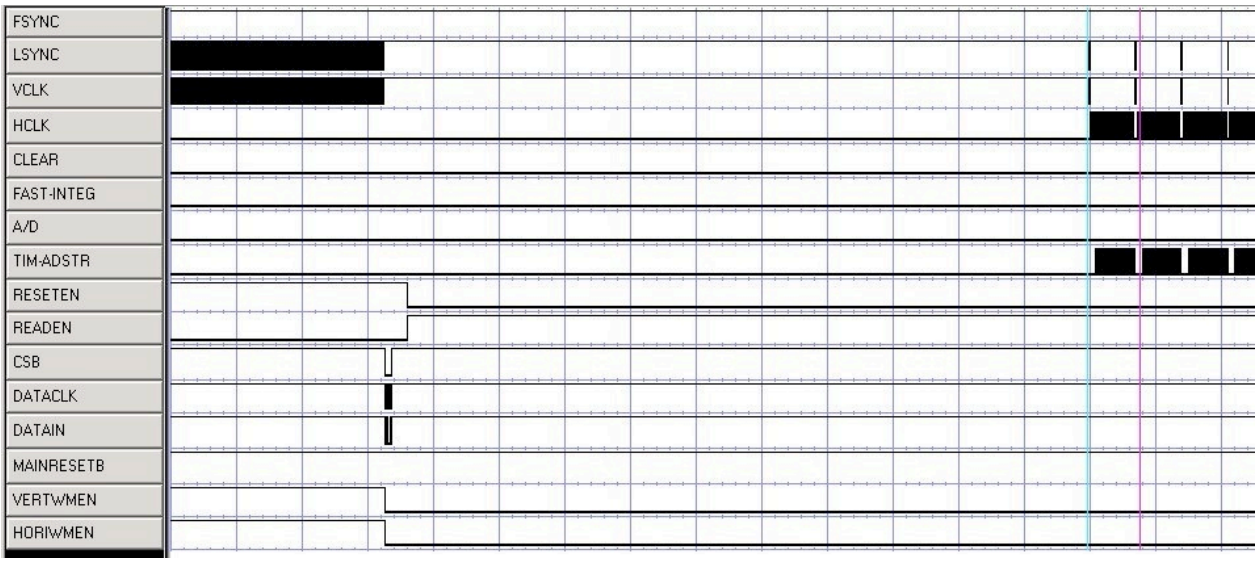
MISCELLANEOUS	$F	To enable windowing mode
	$C	To disable windowing mode

The windowing size and position registers HORIZ_START_REG, HORIZ_STOP_REG,

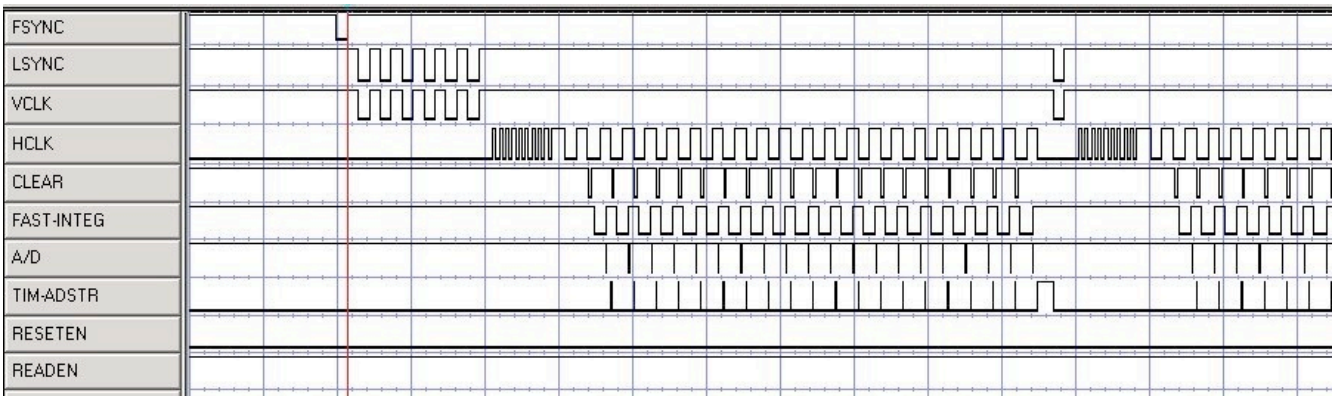


VERT_START_REG and VERT_STOP_REG are written to whenever this mode is enabled or the windowing parameters are changed.

Sub array readout may also be accomplished by normal clocking, in non-native H2RG subarray readout mode. The same SSS and SSP commands are used to set the subarray region(s). If the second argument "number_of_columns = 0" then subarray mode is disabled and entire array size specified in the "Owl" setup window will be read



out. Here the multiplexer is advanced in the horizontal and vertical directions without having the video signal processed. The horizontal clocking is done one clock per skipped column at a rate that is faster then regular readout. The vertical clocking is done one clock per skipped row, so is much faster than reading out the entire row. The timing to switch from native H2RG windowing readout to non-native sub-array readout is shown, with both the serial register and the two signals VERTWMEN and HORIWMEN redundantly taking the sensor out of windowing mode:



Note that subarray readout in the non-native H2RG mode can be done for any number of readout channels, though the subarray size and position will be the same in all the readout areas of the sensor. This might be convenient in some specialized applications, particularly for a small number of channels.

The video processor boards can be selected to transfer data from their A/D converters for readout over the bus in two different ways. For large numbers of channels being read the default method is to transfer all eight channels from all video boards in the system at the same time to the FIFO that is on each board. The timing board will read from each of the required FIFOS in turn after they have all been written to. This is desirable so noise from reading the A/D and moving the data around the board is minimized and made the same for all boards in the system. However, it doesn't work when fewer than eight channels are being read, in which case the data values are moved one-by-one to the FIFO as they are requested to be read by the timing board. Here the FIFO is transparent and only holds the image data for a few nanoseconds. The readout software selects between these two modes based on the number of channels to be read out, but may be overwritten with the "VRM 1" command for reading the A/Ds one-by-one into the FIFO as they are being read out, or "VRM 0" for writing them all eight at once.

There are digitally selectable video offsets that are applied to each of the video signals in the system. Higher video offset number result in fewer image counts, as they subtract from the video signal. These video offsets can be written to with the Set Video Offset command

SVO board_number (0 to 7) DAC_number (0-7) offset (0-4095)

or in the H2RG "Owl" script.

The DC bias voltages on each of the video boards may be selected with the Set Bias Number command that is common to all controllers.

SBN board_number (0 to 7) DAC_number (0-7) ['CLK' or 'VID'] voltage

The voltage is a twelve-bit number for the video processor (0-4095) and an eight bit number for the clock driver board (0-255). There is an "Owl" window for this selectable by Options, Developer Parameter...., Controller, then video or clock driver. The labels on the windows should be self-explanatory.

The controller may be operated in continuous readout mode wherein the beginning of exposures and readouts are initiated by the controller rather than the host computer. The advantage of this is a shorter and deterministic time between exposures since the controller immediately begins a new exposure once the previous one has completed its readout. The control of this is a normal part of "Owl", requiring only that the maximum number of exposures to be acquired in this mode be entered. An impossibly large number may be entered with the sequence terminated by pressing the Abort button. The image data is written continuously to a circular buffer in the host computer system memory, with pointer in the PCI or PCIe interface board keeping track of the current frame number.

A second fiber optic transmitter and receiver pair may optionally be installed on the timing and PCI-Express interface boards to double the image data transmission rate. The option is selected with the 'XMT 1' command, and disabled with a '0' argument.