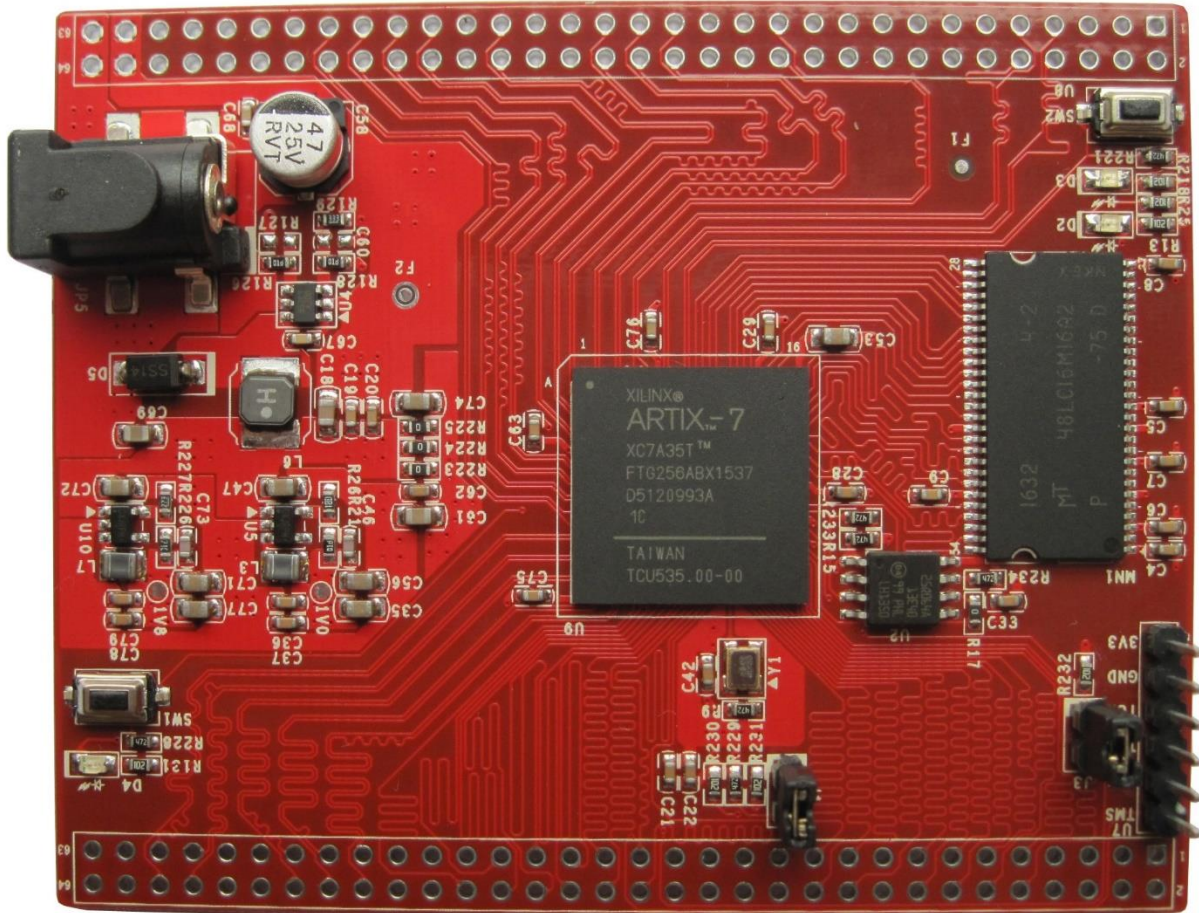# QM_XC7A35T_SDRAM CORE BOARD

USER MANUAL

Preface

The QMTech® XC7A35T SDRAM core board uses Xilinx Artix®-7 devices to demonstrate the highest performance-per-watt fabric, transceiver line rates, DSP processing, and AMS integration in a cost-optimized FPGA. Featuring the MicroBlaze™ soft processor and 1,066Mb/s DDR3 support, the family is the best value for a variety of cost and power-sensitive applications including software-defined radio, machine vision cameras, and low-end wireless backhaul.

Table of Contents

1.   Introduction

1.1   Document Scope

This demo user manual introduces the QM_XC7A35T_SDRAM core board and describes how to setup the core board running with application software Xilinx Vivado 2016.4. Users may employee the on board rich logic resource FPGA XC7A35T-1FTG256C and large SDRAM memory MT48LC16M16 to implement various applications. The core board also has 108 non-multiplexed FPGA IOs for extending customized modules, such as UART module, CMOS/CCD camera module, LCD/HDMI/VGA display module etc.

1.2   Kit Overview

Below section lists the parameters of the QM_XC7A35T_SDRAM core board:
➢ On-Board FPGA: XC7A35T-1FTG256C;
➢ On-Board FPGA external crystal frequency: 50MHz;
➢ XC7A35T-1FTG256C has rich block RAM resource up to 1,800Kb;
➢ XC7A35T-1FTG256C has 33,280 logic cells;
➢ On-Board N25Q064 SPI Flash，8M bytes for user configuration code;
➢ On-Board 32MB Micron SDRAM，MT48LC16M16A2-75;
➢ On-Board 3.3V power supply for FPGA by using MP2359 wide input range DC/DC;
➢ XC7A35T development board has two 64p, 2.54mm pitch headers for extending user IOs. All IOs are precisely designed with length matching;
➢ XC7A35T development board has 2 user switches;
➢ XC7A35T development board has 3 user LEDs;
➢ XC7A35T development board has JTAG interface, by using 6p, 2.54mm pitch header;
➢ XC7A35T development board PCB size is: 6.7cm x 8.4cm;
➢ Default power source for board is: 1A@5V DC, the DC header type: DC-050, 5.5mmx2.1mm;
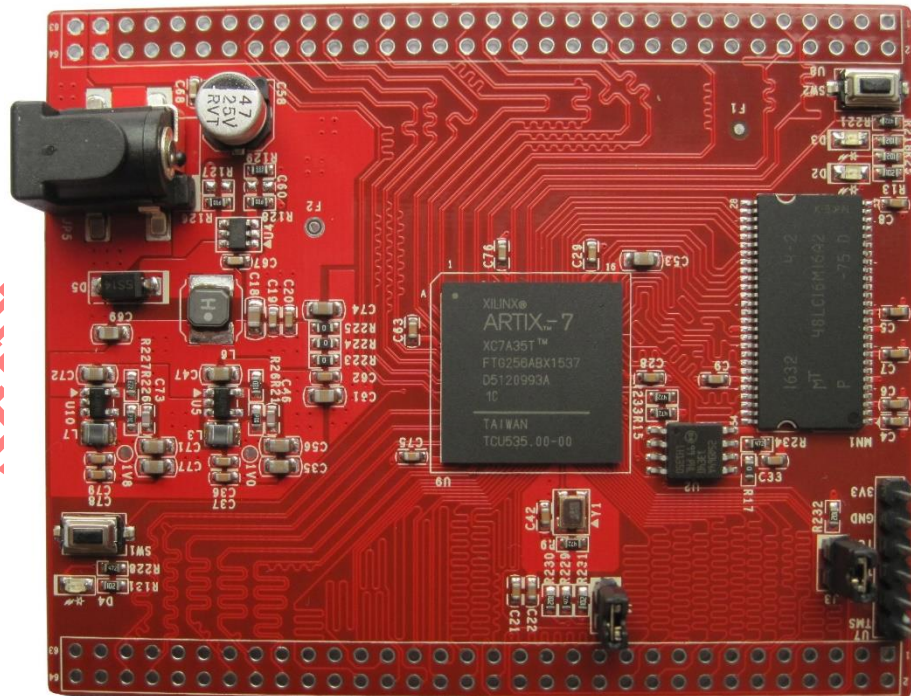

Figure 1-1. QM_XC7A35T_SDRAM Core Board Overview

2.   Getting Started

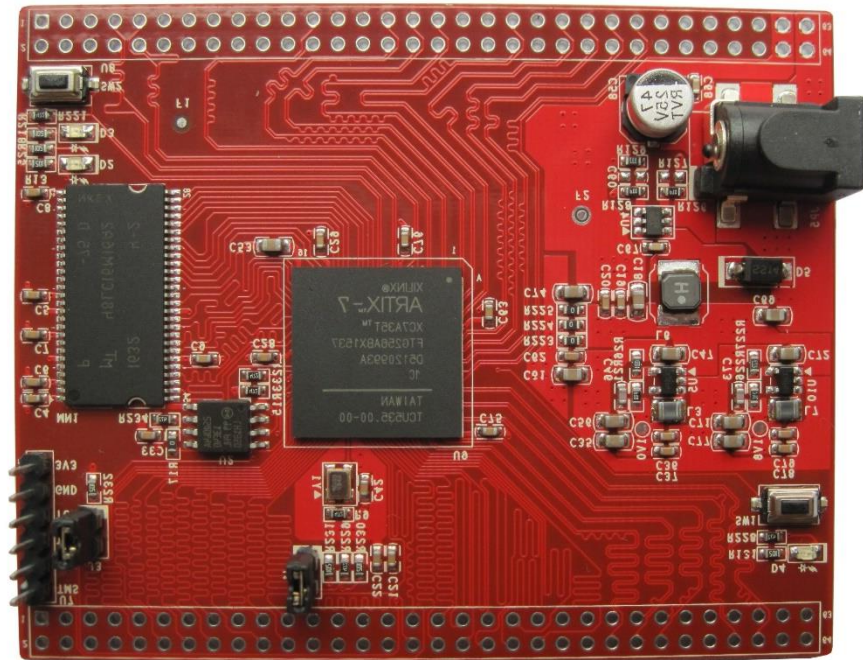The QM_XCA35T_SDRAM core board includes below item:

Figure 2-1. QM_XC7A35T_SDRAM Top View

Below image shows the dimension of the QM_XC7A35T_SDRAM core board: 6.7cm x 8.4cm. The unit in below image is millimeter(mm).
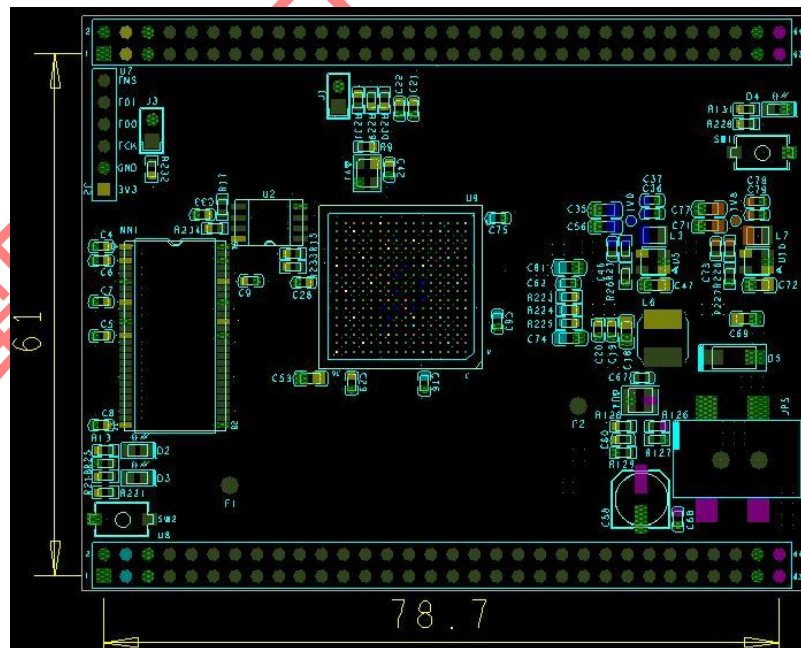
Figure 2-2. QM_XC7A35T_SDRAM Core Board Dimension

2.1   Install Development Tools

The QM_XC7A35T_SDRAM core board tool chain consists of Xilinx Vivado 2016.4, Xilinx USB platform cable, XC7A35T core board and 5V DC power supply. Below image shows the Xilinx Vivado 2016.4 development environment which could be downloaded from Xilinx office website:

Figure 2-3. Vivado 2016.4

Below image shows the JTAG connection between Xilinx USB platform cable and XC7A35T core board:

TMS   (Green)
TDI   (Purple)
TDO   (White)
TCK   (Yellow)
GND   (Black)
VREF   (Red)

5V DC

Figure 2-4. JTAG Connection and Power Supply

2.2 QM_XC7A35T_SDRAM Hardware Design

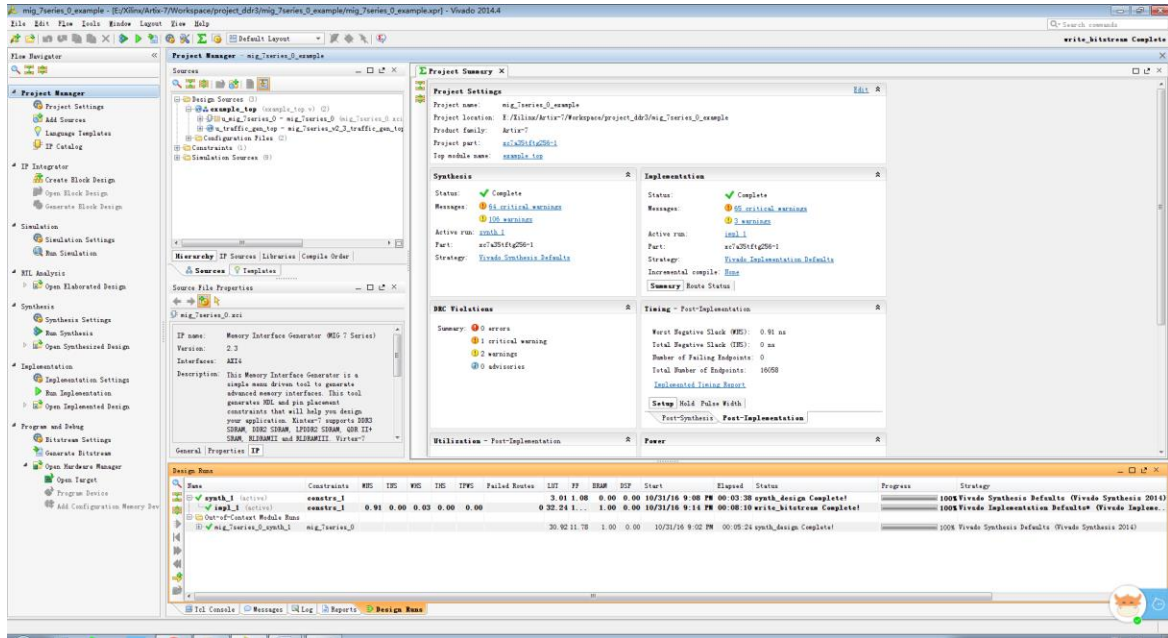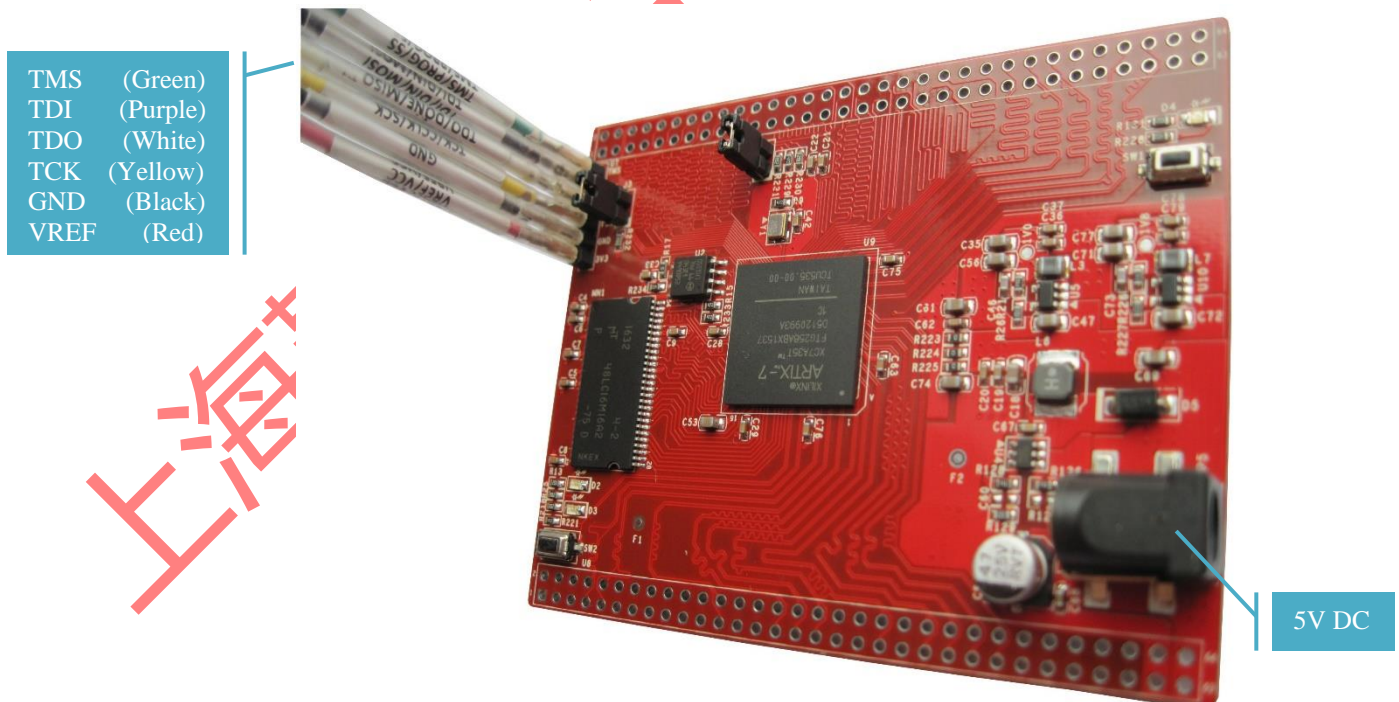### 2.2.1 QM_XC7A35T_SDRAM Power Supply

The core board needs 5V DC input as power supply which could be directly injected from power header or the 64P female header U7/U8. Users may refer to the hardware schematic for the detailed design. The on board LED D4 indicates the 3.3V supply, it will be turned on when the 5V power supply is active. In default status, all the FPGA banks IO power level is 3.3V because bank power supply is 3.3V. However, BANK34 and BANK35 IO's power level could be changed according to detailed custom requirement. There're three 0 ohm resisters could be removed: R223/R224/R225, and instead the BANK34 and BANK35's power supply could be injected from 64P female header U8. Detailed design refer to hardware schematic.

Note: FPGA core supply 1.0V is regulated by On-Semi DC/DC chip NCP1529 which could output maximum 1A current.
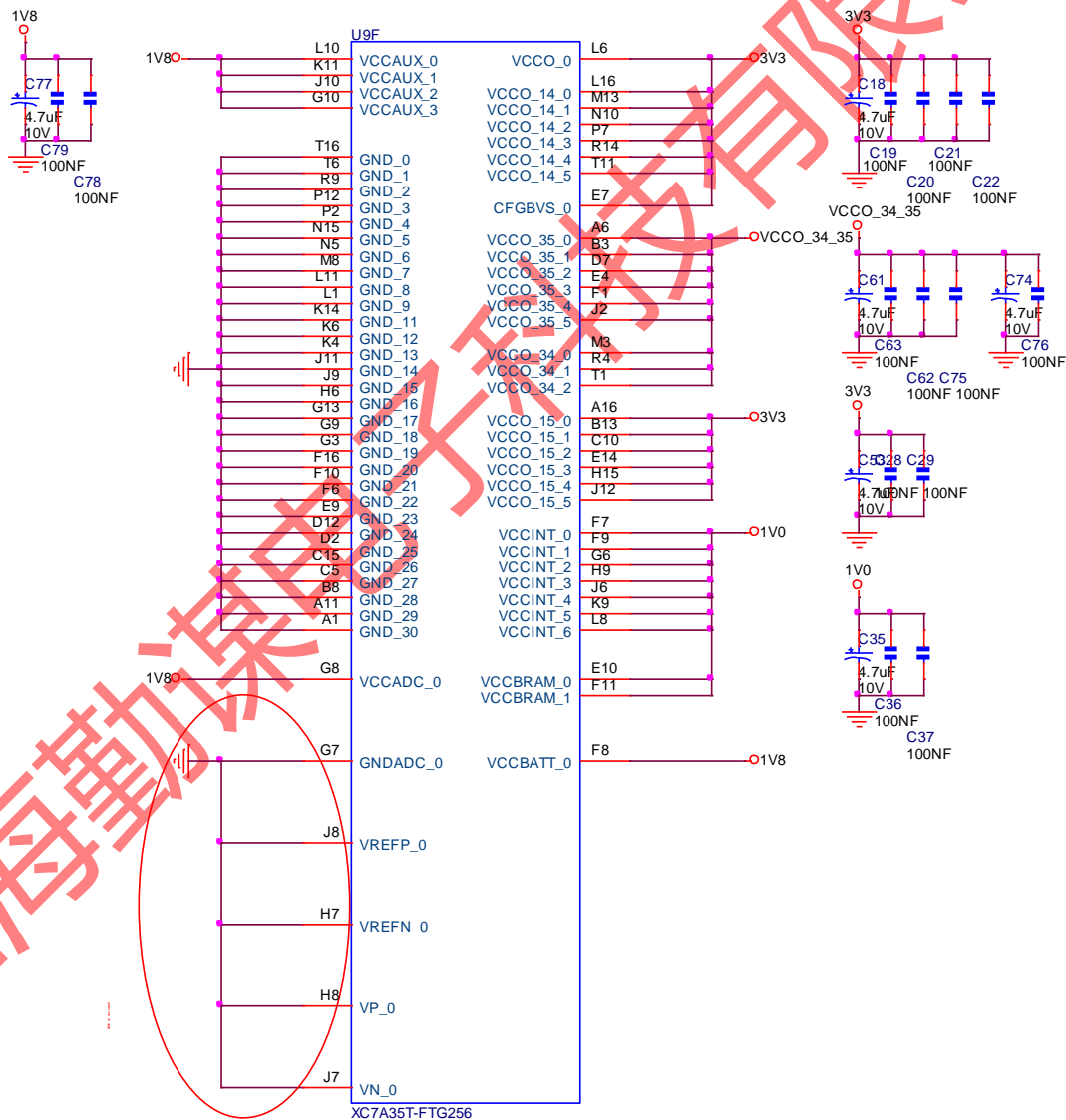
Figure 2-5. Power Supply for the FPGA

2.2.2 QM_XC7A35T_SDRAM SPI Boot

In default, QM_XC7A35T boots from external SPI Flash, detailed hardware design is shown in below figure. The SPI flash is using N25Q064 manufactured by Micron, with 64Mbit memory storage.
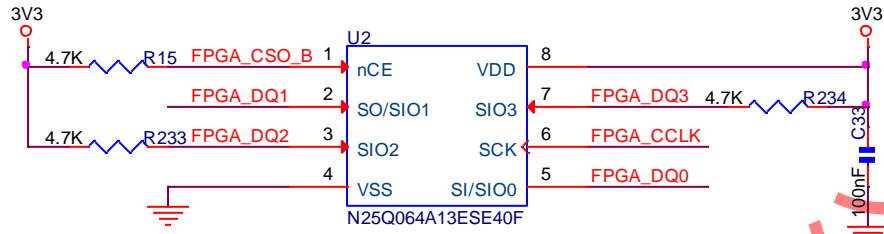
Figure 2-6. SPI Flash

The FPGA boot sequence setting M0:M1:M2 is configured as 1:0:0 which indicates FPGA will boot from SPI Flash after power on. In default, the jumper J1 is under closed status.
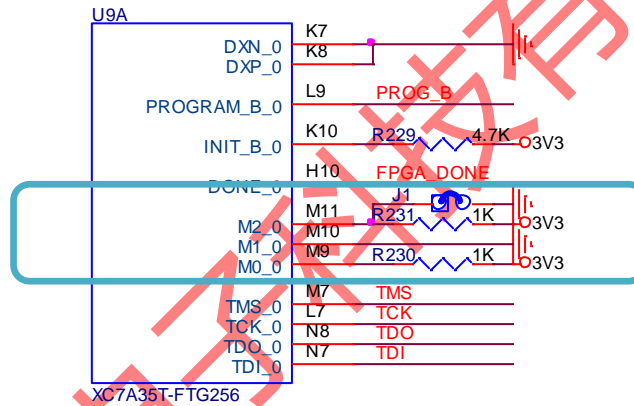
Figure 2-7. M0:M1 Hardware Settings

The LED D2 will be turned on after the FPGA successfully loading configuration file from SPI Flash during power on stage. In this case, LED D2 could be used as FPGA loading status indicator.
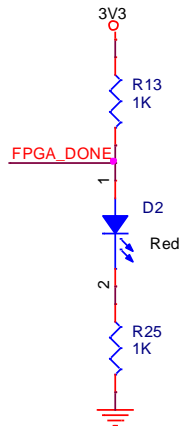
Figure 2-8. FPGA_DONE Status Indicator

2.2.3 QM_XC7A35T_SDRAM Memory

QM_XC7A35T has on board 16bit width data bus, 32MB memory size SDRAM MT48LC16M16 provided by Micron. Below image shows the detailed hardware design:
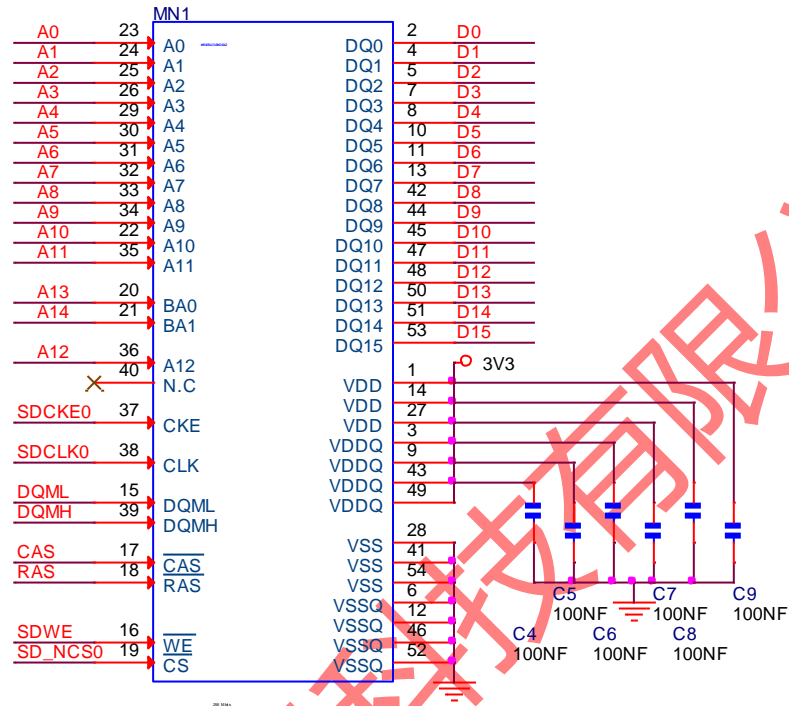
Figure 2-9. SDRAM

2.2.4 QM_XC7A35T_SDRAM System Clock

FPGA chip XC7A35T-1FTG256C has system clock frequency 50MHz which is directly provided by external crystal. The crystal is designed with high accuracy and stability with low temperature drift 10ppm/° c. Below image shows the detailed hardware design:

Figure 2-10. 50MHz System Clock

2.2.5   QM_XC7A35T_SDRAM Extension IO

The core board has two 64P 2.54mm pitch female headers which are used for extending user modules, such as ADC/DAC module, audio/video module, ethernet module, etc.

BANK34/35 Voltage Supply Pins.

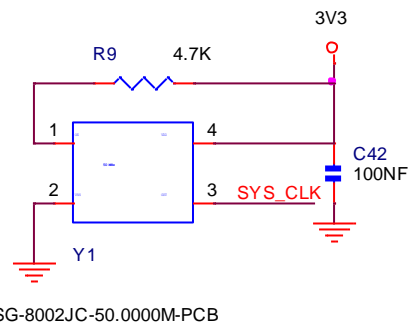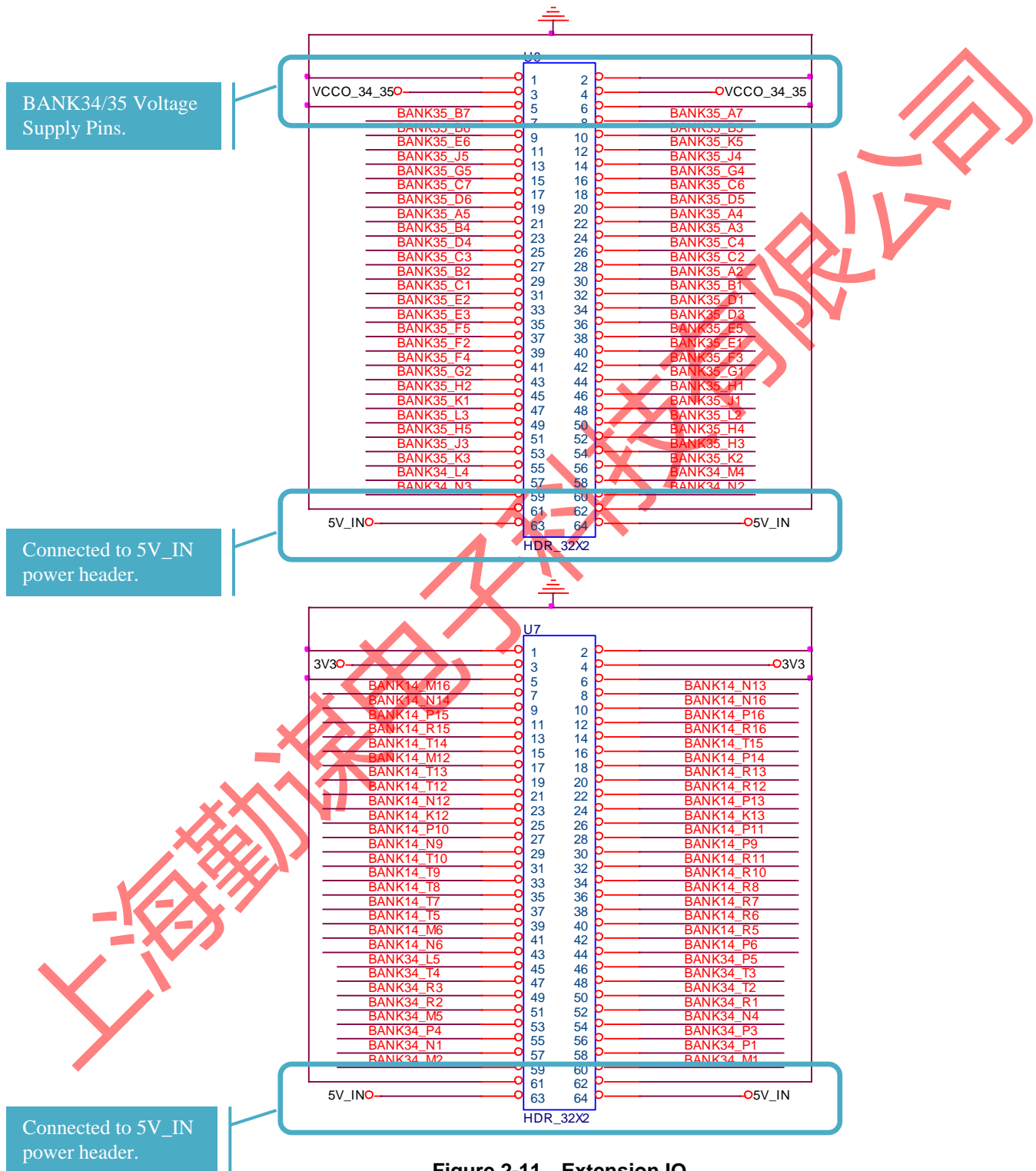|	U3	
VCCO_34_35	1 2	VCCO_34_35
	3 4	
BANK35_B7	5 6	BANK35_A7
BANK35_B6	7 8	BANK35_B5
BANK35_E6	9 10	BANK35_K5
BANK35_J5	11 12	BANK35_J4
BANK35_G5	13 14	BANK35_G4
BANK35_C7	15 16	BANK35_C6
BANK35_D6	17 18	BANK35_D5
BANK35_A5	19 20	BANK35_A4
BANK35_B4	21 22	BANK35_A3
BANK35_D4	23 24	BANK35_C4
BANK35_C3	25 26	BANK35_C2
BANK35_B2	27 28	BANK35_A2
BANK35_C1	29 30	BANK35_B1
BANK35_E2	31 32	BANK35_D1
BANK35_E3	33 34	BANK35_D3
BANK35_F5	35 36	BANK35_E5
BANK35_F2	37 38	BANK35_E1
BANK35_F4	39 40	BANK35_F3
BANK35_G2	41 42	BANK35_G1
BANK35_H2	43 44	BANK35_H1
BANK35_K1	45 46	BANK35_J1
BANK35_L3	47 48	BANK35_L2
BANK35_H5	49 50	BANK35_H4
BANK35_J3	51 52	BANK35_H3
BANK35_K3	53 54	BANK35_K2
BANK34_L4	55 56	BANK34_M4
BANK34_N3	57 58	BANK34_N2
	59 60	
	61 62	
5V_IN	63 64	5V_IN
	HDR_32X2	

Connected to 5V_IN power header.

	U7	
3V3	1 2	3V3
	3 4	
BANK14_M16	5 6	BANK14_N13
BANK14_N14	7 8	BANK14_N16
BANK14_P15	9 10	BANK14_P16
BANK14_R15	11 12	BANK14_R16
BANK14_T14	13 14	BANK14_T15
BANK14_M12	15 16	BANK14_P14
BANK14_T13	17 18	BANK14_R13
BANK14_T12	19 20	BANK14_R12
BANK14_N12	21 22	BANK14_P13
BANK14_K12	23 24	BANK14_K13
BANK14_P10	25 26	BANK14_P11
BANK14_N9	27 28	BANK14_P9
BANK14_T10	29 30	BANK14_R11
BANK14_T9	31 32	BANK14_R10
BANK14_T8	33 34	BANK14_R8
BANK14_T7	35 36	BANK14_R7
BANK14_T5	37 38	BANK14_R6
BANK14_M6	39 40	BANK14_R5
BANK14_N6	41 42	BANK14_P6
BANK34_L5	43 44	BANK34_P5
BANK34_T4	45 46	BANK34_T3
BANK34_R3	47 48	BANK34_T2
BANK34_R2	49 50	BANK34_R1
BANK34_M5	51 52	BANK34_N4
BANK34_P4	53 54	BANK34_P3
BANK34_N1	55 56	BANK34_P1
BANK34_M2	57 58	BANK34_M1
	59 60	
	61 62	
5V_IN	63 64	5V_IN
	HDR_32X2	

Connected to 5V_IN power header.

Figure 2-11. Extension IO

2.2.1 QM_XC7A35T_SDRAM 3.3V Power Supply

The core board's 3.3V power supply is using high efficiency DC/DC chip MP2359 provided by MPS Inc. The MP2359 supports wide voltage input range from 4.5V to 24V. In normal use case, 5V DC power supply is suggested to be applied on the board. Below image shows the MP2359 hardware design:
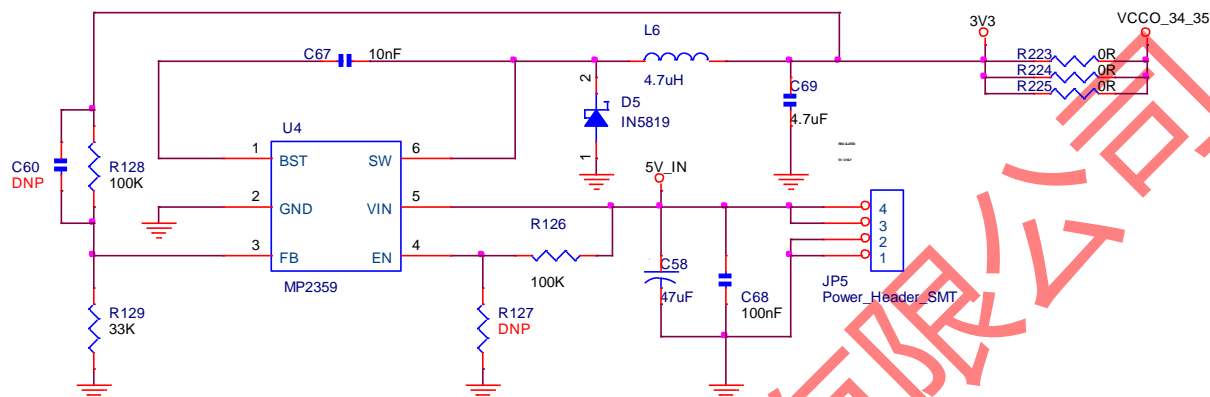

Figure 2-12. MP2359 Hardware Design

2.2.2 QM_XC7A35T_SDRAM JTAG Port

The on board JTAG port uses 6P 2.54mm pitch header which could be easily connected to Xilinx USB platform cable. Below image shows the hardware design of the JTAG port:
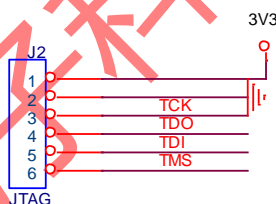

Figure 2-13. JTAG Port

2.2.3 QM_XC7A35T_SDRAM User LED

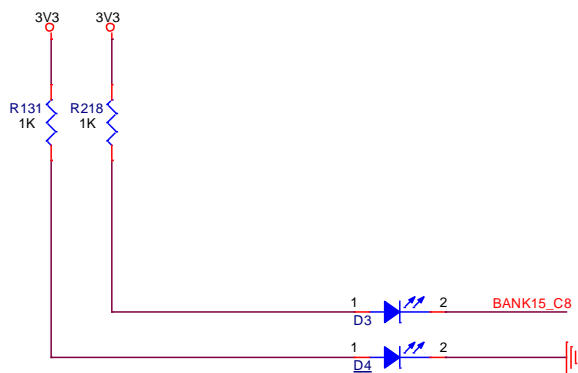Below image shows one user LED and 3.3V power supply indicator:

Figure 2-14. LEDs

2.2.4 QM_XC7A35T_SDRAM User Key

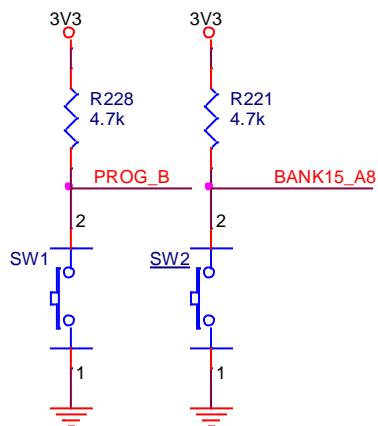Below image shows the PROGRAM_B key and one user key:

Figure 2-15. Keys

3.   Reference

[1] ug470_7Series_Config.pdf
[2] ds181_Artix_7_Data_Sheet.pdf
[3] ug475_7Series_Pkg_Pinout.pdf
[4] n25q_64a_3v_65nm.pdf
[5] MT48LC16M16.pdf
[6] MP2359.pdf
[7] NCP1529-D.PDF

4. Revision

Doc. Rev.	Date	Comments
0.1	05/10/2017	Initial Version.
1.0	05/14/2017	V1.0 Formal Release.