

1. Description

1.1. Project

Project Name	csModbus
Board Name	NUCLEO-F042K6
Generated with:	STM32CubeMX 6.8.0
Date	08/10/2024

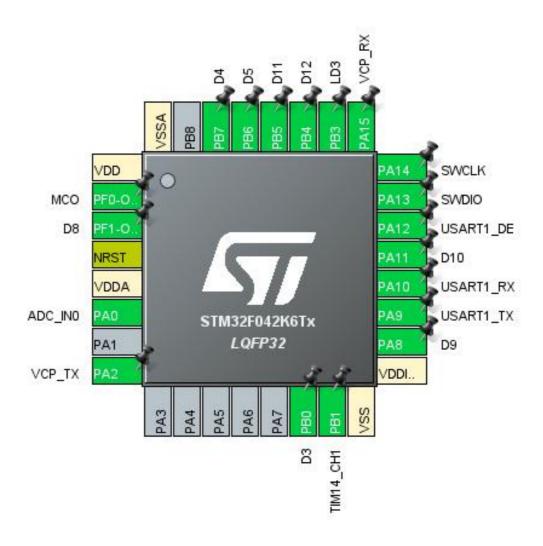
1.2. MCU

MCU Series	STM32F0
MCU Line	STM32F0x2
MCU name	STM32F042K6Tx
MCU Package	LQFP32
MCU Pin number	32

1.3. Core(s) information

Core(s)	Arm Cortex-M0

2. Pinout Configuration



3. Pins Configuration

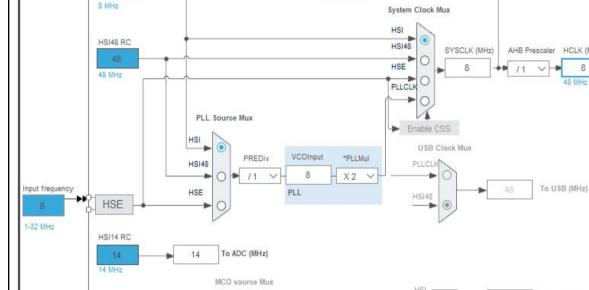
Pin Number LQFP32	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VDD	Power		
2	PF0-OSC_IN	I/O	RCC_OSC_IN	MCO
3	PF1-OSC_OUT *	I/O	GPIO_Output	D8
4	NRST	Reset		
5	VDDA	Power		
6	PA0	I/O	ADC_IN0	
8	PA2	I/O	USART2_TX	VCP_TX
14	PB0 *	I/O	GPIO_Output	D3
15	PB1	I/O	TIM14_CH1	
16	VSS	Power		
17	VDDIO2	Power		
18	PA8 *	I/O	GPIO_Input	D9
19	PA9	I/O	USART1_TX	
20	PA10	I/O	USART1_RX	
21	PA11 *	I/O	GPIO_Input	D10
22	PA12	I/O	USART1_DE	
23	PA13	I/O	SYS_SWDIO	SWDIO
24	PA14	I/O	SYS_SWCLK	SWCLK
25	PA15	I/O	USART2_RX	VCP_RX
26	PB3 *	I/O	GPIO_Output	LD3
27	PB4 *	I/O	GPIO_Input	D12
28	PB5 *	I/O	GPIO_Input	D11
29	PB6 *	I/O	GPIO_Output	D5
30	PB7 *	I/O	GPIO_Output	D4
32	VSSA	Power		

^{*} The pin is affected with an I/O function

I2C1 Clock Mux HSI Clock Tree **▶** (0) To I2C1 (MHz) To RTC (KHz) SYSCLK To 12S1 (MHz) To IWDG (KHz) HCLK to AHB bus, core, 8 To FLITF (MHz) memory and DMA (MHz) Configuration 11 V To Cortex System timer (MHz) 8 FCLK (MHz) SYSCLK (MHz) AHB Prescaler HCLK (MHz) APB1 Prescaler PCLK1 APB1 peripheral clocks (MHz) 8 11 48 MHz n 48 MHz max APB1 Timer clocks (MHz) X1 USART1 Clock Mux SYSCLK HSI To USART1 (MHz)

PCLK1

To CEC (KHz)



HSI HSI48

HSI14

LSI SYSCLK ▶ / 244

RTC Clock Mux

HSE_RTC

LSI (e)

/ 32

4 /1 V4

0

LSI RC

HSI RC

40 40 KHz

Page 4

(MHz) MCO

5. Software Project

5.1. Project Settings

Name	Value	
Project Name	csModbus	
Project Folder	D:\CraneSoft\Develop\GitHub\csModbus.cpp\Nucleo-F04K6\CubeMX\csModbus	
Toolchain / IDE	MDK-ARM V5	
Firmware Package Name and Version	STM32Cube FW_F0 V1.11.5	
Application Structure	Advanced	
Generate Under Root	No	
Do not generate the main()	No	
Minimum Heap Size	0x200	
Minimum Stack Size	0x400	

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_ADC_Init	ADC
4	MX_TIM14_Init	TIM14
5	MX_USART1_UART_Init	USART1
6	MX_USART2_UART_Init	USART2

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F0
Line	STM32F0x2
мси	STM32F042K6Tx
Datasheet	DS10147_Rev5

6.2. Parameter Selection

Temperature	25
Vdd	3.6

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

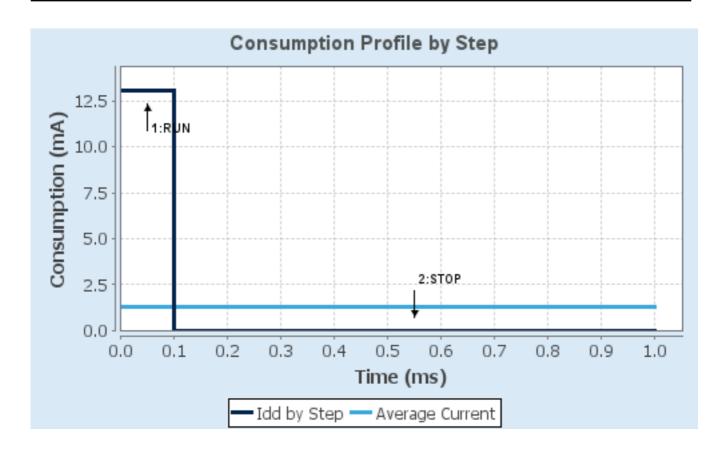
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.6	3.6
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	48 MHz	0 Hz
Clock Configuration	HSI PLL	Regulator LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	13.04 mA	6.2 µA
Duration	0.1 ms	0.9 ms
DMIPS	0.0	0.0
Та Мах	102.32	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	1.31 mA
Battery Life	3 months, 16	Average DMIPS	0.0 DMIPS
	days, 14 hours	_	

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC

mode: IN0

7.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler Asynchronous clock mode
Resolution ADC 12-bit resolution
Data Alignment Right alignment

Scan Conversion Mode Forward

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data preserved

Low Power Auto Wait Disabled
Low Power Auto Power Off Disabled

ADC_Regular_ConversionMode:

Sampling Time 1.5 Cycles

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

WatchDog:

Enable Analog WatchDog Mode false
Low Threshold 0

7.2. RCC

High Speed Clock (HSE): BYPASS Clock Source

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Prefetch Buffer Enabled

Flash Latency(WS) 0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value 16
HSI14 Calibration Value 16
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

7.3. SYS

mode: Debug Serial Wire

7.4. TIM14

mode: Activated

Channel1: PWM Generation CH1

7.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0
Counter Mode Up
Counter Period (AutoReload Register - 16 bits value) 65535
Internal Clock Division (CKD) No Division auto-reload preload Disable

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

7.5. USART1

Mode: Asynchronous

mode: Hardware Flow Control (RS485)

7.5.1. Parameter Settings:

Basic Parameters:

Baud Rate 19200 *

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
Polarity High

Assertion Time 0
Deassertion Time 0

Advanced Features:

Auto Baudrate Disable
TX Pin Active Level Inversion Disable
RX Pin Active Level Inversion Disable
Data Inversion Disable
TX and RX Pins Swapping Disable
Overrun Enable
DMA on RX Error Enable
MSB First Disable

7.6. USART2

Mode: Asynchronous

7.6.1. Parameter Settings:

Basic Parameters:

Baud Rate 38400

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable

Advanced Features:

TX Pin Active Level Inversion

RX Pin Active Level Inversion

Disable

Data Inversion

Disable

TX and RX Pins Swapping

Overrun

Enable

DMA on RX Error

Enable

MSB First

Disable

* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC	PA0	ADC_IN0	Analog mode	No pull-up and no pull-down	n/a	
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	MCO
SYS	PA13	SYS_SWDIO	n/a	n/a	n/a	SWDIO
	PA14	SYS_SWCLK	n/a	n/a	n/a	SWCLK
TIM14	PB1	TIM14_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PA12	USART1_DE	Alternate Function Push Pull	No pull-up and no pull-down	High *	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	High *	VCP_TX
	PA15	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	High *	VCP_RX
GPIO	PF1- OSC_OUT	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D8
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D3
	PA8	GPIO_Input	Input mode	Pull-down *	n/a	D9
	PA11	GPIO_Input	Input mode	Pull-down *	n/a	D10
	PB3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3
	PB4	GPIO_Input	Input mode	Pull-down *	n/a	D12
	PB5	GPIO_Input	Input mode	Pull-down *	n/a	D11
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D5
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D4

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
System service call via SWI instruction	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	0	0	
PVD and VDDIO2 supply comparator interrupts through EXTI lines 16 and 31	unused			
Flash global interrupt	unused			
RCC and CRS global interrupts	unused			
ADC interrupt	unused			
TIM14 global interrupt	unused			
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	unused			
USART2 global interrupt	unused			

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler
	sequence ordering	handler	
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
System service call via SWI instruction	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

* User modified value

9. System Views

- 9.1. Category view
- 9.1.1. Current



10. Docs & Resources

Type Link

IBIS models https://www.st.com/resource/en/ibis_model/stm32f0_ibis.zip

System View https://www.st.com/resource/en/svd/stm32f0_svd.zip

Description

Presentations https://www.st.com/resource/en/product_presentation/gt_stm32f0-l0.pdf

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