ECHIP, Inc

EC5128

4-Channel Audio/Video Decoders

With 33MHz PCI Interface

Preliminary Data Sheet from ECHIP, Inc

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Catalog

EC5128 4-CH Audio/Video Decoders with 33MHz PCI Interface

1. Features

Video decoder

- NTSC (M) and PAL (B, D, G, H, I, M), support with automatic format detection.
- Software selectable analog inputs allow any of 2 CVBS per one video ADC.
- Four 10-bit ADCs and analog clamping circuit for CVBS input.
- Fully programmable static gain or automatic gain control for the Y channel.
- Programmable white peak control for CVBS channel.
- 4-H adaptive comb filter Y/C separation.
- PAL delay line for color phase error correction.
- Image enhancement with 2D peaking and CTI.
- Digital sub-carrier PLL for accurate color decoding.
- Advanced synchronization processing and sync detection for handling non-standard and weak signal.
- Programmable hue, brightness, saturation, contrast, sharpness, Gamma control, and noise suppression.
- Automatic color control and color killer.
- Detection of level of copy protection according to Macrovision standard.
- Programmable output cropping.

Video scaler

- High quality horizontal filtered scaling with arbitrary scale down ratio.
- Phase accuracy better than 1/32 pixel
- Selectable anti-alias filter.

Audio Capture

- Four 10-bit ADC for Analog Sound digitizing.
- Programmable Sampling rate.

PCI

- 33MHz PCI interface
- PCI Rev. 2.2-3.0 compliant.
- ACPI support.
- Integrated Video/Audio DMA controller.
- Support both selectable four real-time videos and eight switching non real-time videos.

Miscellaneous

- Programmable RGB and YCbCr color space conversion.
- 400Kbps Two-wire MPU serial bus Master interface.
- Power-down mode.
- Single 27MHz crystal for all standards.
- 5V tolerant I/O.
- 1.8V power supply.
- 100-pin LQFP package.

2. Function Description

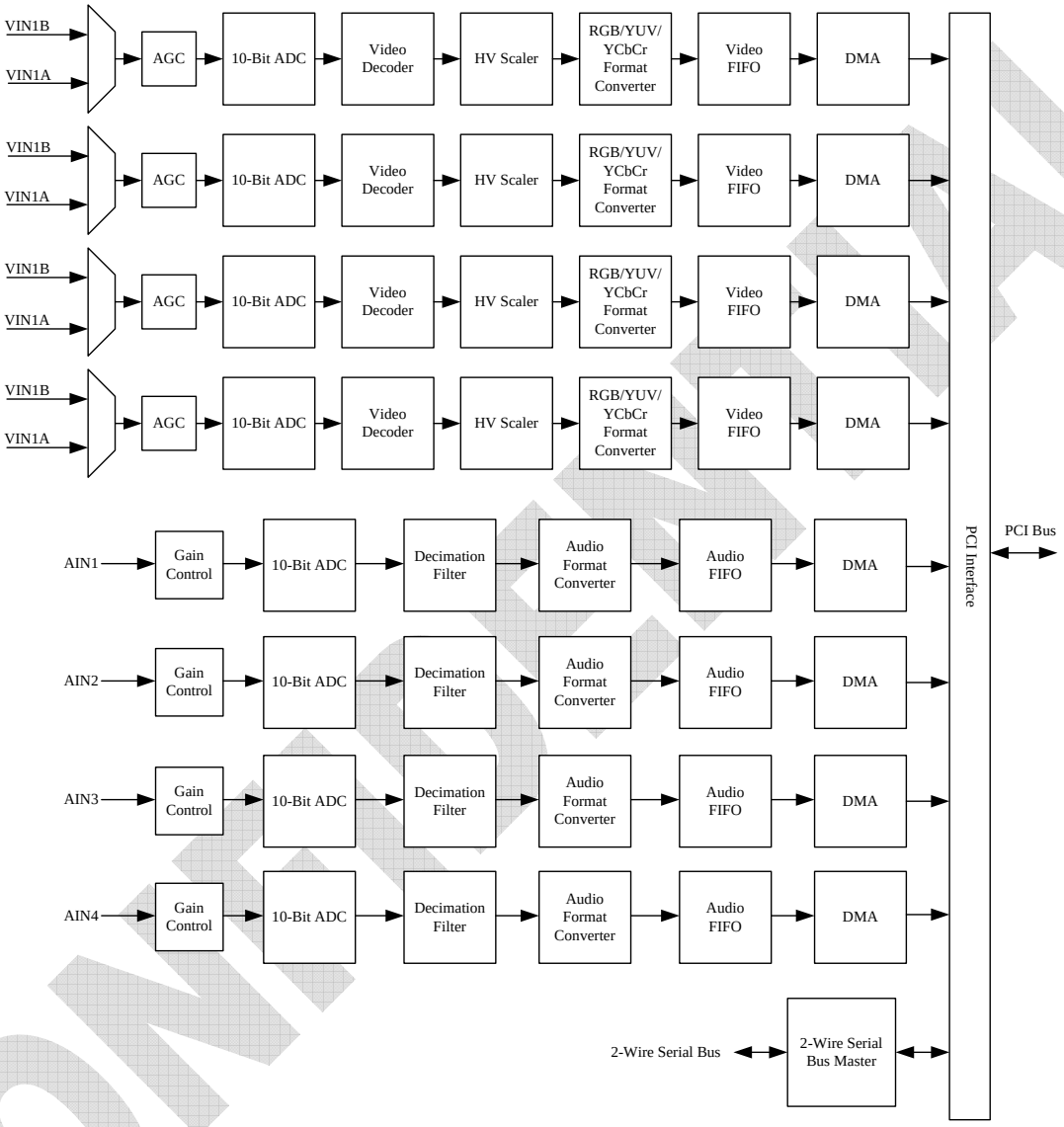


Figure 1: EC5128 Block Diagram

2.1 Video Decoder

2.1.1 Video Decoder Overview

The EC5128 is a multi-standard video decoder that is designed for multimedia applications. It uses the mixed-signal 1.8V CMOS technology to provide a low-power integrated solution.

The video decoder decodes the analog CVBS signals into digital YCbCr for output. It consists of analog front-end with input source selection, variable gain amplifier and analog-to-digital converters, Y/C separation circuit, multi-standard color decoder (PAL BDGHIM, NTSC M) and synchronization circuitry. The Y/C separation is done with highly adaptive 4H comb filter for reduced cross color and cross luminance. The advanced synchronization processing circuitry can produce stable pictures for non-standard signal as well as weak signal. A video scaler is provided to arbitrarily scale down the output video. It includes various control circuits like brightness, contrast, saturation, and dynamic aperture correction for best video quality.

2.1.2 Analog Front-end

The analog front-end converts analog video signals to the required digital format. There are four analog video channels with clamping circuits and ADCs. The Y channel has 2-input multiplexer, and a variable gain amplifier for automatic gain control (AGC). Its four inputs are identified as VINnA, VINnB, VINnC, VINnD(n=1,2).

Video Source Selection

All analog signals should be AC-coupled to these inputs.

The Y channel analog multiplexer selects one of the four inputs VINnA, VINnB, VINnC, VINnD(n=1,2).

Clamping and Automatic Gain Control

All two analog channels have built-in clamping circuit that restores the signal DC level. The Y channel restores the back porch of the digitized video to a level of 64 or a programmable level. This operation is automatic through internal feedback loop.

The Automatic Gain Control (AGC) of the Y channel adjusts input gain so that the sync tip is at a desired level. Programmable white peak protection logic is included to prevent saturation in the case of abnormal proportion between sync

and white peak level.

Analog to Digital Converter

EC5128 contains two 10-bit pipelined ADCs that consume less power than conventional flash ADC. The output of the Clamp and AGC connects to one ADC that digitizes the composite input or the Y signal input.

2.1.3 Sync Processing

The sync processor of EC5128 detects horizontal synchronization and vertical synchronization signals in the composite video or in the Y signal. The processor contains a decisional logic to achieve reliable sync detection in stable signal as well as in unstable signals such as those from VCR fast forward or backward.

Horizontal sync processing

The horizontal synchronization processing contains a sync separator and the related decision logic.

The horizontal sync detector detects the presence of a horizontal sync tip by examining low-pass filtered input samples whose level is lower than a threshold.

Vertical sync processing

The vertical sync separator detects the vertical synchronization pattern in the input video signals. An option is available to provide faster responses for certain applications. The field status is determined at vertical synchronization time. When the location of the detected vertical sync is inline with a horizontal sync, it indicates a frame start or the odd field start. Otherwise, it indicates an even field. The field logic can also be controlled to toggle automatically while tracking the input.

2.1.4 Color Decoding Y/C separation

The color-decoding block contains the luma/chroma separation for the composite video signal and multi-standard color demodulation. For NTSC and PAL standard signals, the luma/chroma separation can be done either by comb filter or notch/band-pass filter combination. The default selection for NTSC/PAL is comb filter. The characteristics of the band-pass filter are shown in the filter curve section.

In the case of comb filter, the EC5128 separates luma (Y) and chroma(C) of a composite video signal using a proprietary 4H, 5-line adaptive comb filter. The filter uses a four-line buffer. Adaptive logic combines the upper-comb and the lower-comb results based on the signal changes among the previous, current and next lines. This technique leads to good Y/C separation with small cross luma and cross color at both horizontal and vertical edges.

Due to the line buffer used in the comb filter, there is always two lines processing delay in the output images no matter what standard or filter option is chosen.

If notch/band-pass filter is selected, the characteristics of the filters are shown in the filter curve section.

Color demodulation

The color demodulation for NTSC and PAL standard is done by first quadrature mixing the chroma signal to the base band. The mixing frequency is equal to the sub-carrier frequency for NTSC and PAL. After the mixing, a low-pass filter is used to remove carrier signal and yield chroma components. The low-pass filter characteristic can be selected for optimized transient color performance. For the PAL system, the PAL ID or the burst phase switching is identified to aid the PAL color demodulation.

After the mixer and low-pass filter, it yields the FM modulated chroma. The filter characteristics are shown in filter curve section. During the FM demodulation, the chroma carrier frequency is identified and used to control the color demodulation.

The sub-carrier signal for use in the color demodulator is generated by direct digital synthesis PLL that locks onto the input sub-carrier reference (color burst). This arrangement allows any sub-standard of NTSC and PAL to be demodulated easily with single crystal frequency.

Automatic Chroma Gain Control

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by high-frequency loss in video signal. In the NTSC/PAL standard, the

color reference signal is the burst on the back porch. This color-burst amplitude is calculated and compared to standard amplitude. The chroma (Cx) signals are then increased or decreased in amplitude accordingly.

Low Color Detection and Removal

For low color amplitude signals, black and white video or very noisy signals, the color will be "killed". The color killer uses the burst amplitude measurement to switch-off the color when the measured burst amplitude falls below a programmed threshold. The threshold has programmed hysteresis to prevent oscillation of the color killer function. Programming a low threshold value can disable the color killer function.

Automatic standard detection

The EC5128 has build-in automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency and frame rate to identify NTSC or PAL color signals. The standards that can be identified are NTSC (M), PAL (B, D, G, H, I, M),. Each standard can be included or excluded in the standard recognition process by software control. The identified standard is indicated by the STD_NOW register. Automatic standard detection can be overridden by software controlled standard selection.

Video Format support

EC5128 supports all common video formats as shown in Table 1. The video decoder needs to be programmed appropriately for each of the composite video input formats.

Table 1. Video Input Formats Supported by EC5128

Format	Lines	Fields	Fsc	Country
NTSC-M	525	60	3.5795 MHz	U.S, many outhers
NTSC-Japan	525	60	3.5795 MHz	Japan
PAL-B,G,N	625	50	4.4336 MHz	Many
PAL-D	625	50	4.4336 MHz	China
PAL-H	625	50	4.4336 MHz	Belgiunm
PAL-I	625	50	4.4336 MHz	Great Britain, others
PAL-M	525	60	3.5795MHz	Brazil

2.1.5 Component Processing

Luminance Processing

The EC5128 adjusts brightness by adding a programmable value to the Y signal. It adjusts the picture contrast by changing the gain of the Y signal.

The EC5128 video decoder also performs a coring function. It can force all values below a certain level, programmed in the Coring Control Register, to zero. This is useful because human eyes are sensitive to variations in nearly black images. Changing levels near black to true black, can make the image appear clearer.

Sharpness

The EC5128 also provides a sharpness control function through control registers. It provides the control in 16 steps up to +12db. The center frequency of the enhancement curve is around 3.5Mhz. It also provides a high frequency coring function to minimize the amplification of high frequency noise. The coring level is adjustable through the Coring Control register. The same function can also be used to soften the images. This can be used to provide noise reduction on noisy signal.

To further enhance the image, a programmable vertical peaking function is provided for up to +6db of enhancement. A programmable coring level can be adjusted to minimize the noise enhancement.

The Hue and Saturation

When decoding NTSC signals, EC5128 can adjust the hue of the chroma signal. The hue is defined as a phase shift of the subcarrier with respect to the burst. This phase shift can be programmed through a control register.

The color saturation can be adjusted by changing the gain of Cb and Cr signals for all NTSC and PAL formats. The Cb and Cr gain can be adjusted independently for flexibility.

Color Transient Improvement

A programmable Color Transient Improvement circuit is provided to enhance the color bandwidth. Low-level noise enhancement can be suppressed by a programmable coring logic. Overshoot and undershoot are also removed by special circuit to prevent false color generation at the color edge.

2.1.6 Down-scaling and Cropping

The EC5128 provides two methods to reduce the amount of output video pixel data, downscaling and cropping. The downscaling provides full video image at lower resolution. Cropping provides only a portion of the video image output. All these mechanisms can be controlled independently to yield maximum flexibility in the output stream.

Down-Scaling

The EC5128 can independently reduce the output video image size in both horizontal and vertical directions using the HOR_DEC and VER_DEC. The HOR_DEC register's value can decide the point picked from every one, two or four points. The VER_DEC register's value can decide the line picked from every one, two or four lines.

EC5128 Cropping

Cropping allows only subsection of a video image to be output. The VACTIVE signal can be programmed to indicate the number of active lines to be displayed in a video field, and the HACTIVE signal can be programmed to indicate the number of active pixels to be displayed in a video line. The start of the field or frame in the vertical direction is indicated by the leading edge of VSYNC. The start of the line in the horizontal direction is indicated by the leading edge of the HSYNC. The start of the active lines from vertical sync edge is indicated by the VDELAY register. The start of the active pixels from the horizontal edge is indicated by the HDELAY register. The sizes and location of the active video are determined by HDELAY, HACTIVE, VDELAY, and VACTIVE registers.

The Horizontal delay register (HDELAY) determines the number of pixels delay between the leading edge of HSYNC and the leading edge of the HACTIVE. Note that this value is referenced to the unscaled pixel number. The Horizontal active register (HACTIVE) determines the number of active pixels to be output or scaled after the delay from the sync edge is met. This value is also referenced to the unscaled pixel number. Therefore, if the scaling ratio is changed, the active video region used for scaling remain unchanged as set by the HACTIVE register, but the valid pixels output are equal or reduced due to down scaling. In order for the cropping to work properly, the following equation should be satisfied.

HDELAY + HACTIVE < Total number of pixels per line.

The Vertical delay register (VDELAY) determines the number of lines delay between the leading edge of the VSYNC and the start of the active video lines. It indicates number of lines to skip at the start of a frame before asserting the VACTIVE signal. This value is referenced to the incoming scan lines before the

vertical scaling. The number of scan lines is 525 for the 60Hz systems and 625 for the 50Hz systems. The Vertical active register (VACTIVE) determines the number of lines to be used in the vertical scaling. Therefore, the number of scan lines output is equal or less than the value set in this register depending on the vertical scaling ratio. In order for the vertical cropping to work properly, the following equation should be observed.

VDELAY + VACTIVE < Total number of lines per field

2.2 Video Data Format Conversion

The decoded video from the video decoder within EC5128 is in the format of YCbCr 4:4:4.GPIO ITU-R BT656 video input data is in the format of YCbCr 4:2:2. Video data format conversion is needed to convert these video data to the selected output video format. The video data can be converted to variety of RGB video formats, and changes can be made in the byte order. The video stream from video decoder of EC5128 will be packed into DWORD in the selected format prior to input to the video FIFO.

YUV 4:2:2 {Y0[7:0], U0[7:0], Y1[7:0], V0[7:0]}

YCbCr 4:2:2 {Y0[7:0], Cb0[7:0], Y1[7:0], Cr0[7:0]}

RGB {R0[7:0], G0[7:0], R1[7:0], B0[7:0]}

2.3 Serial BUS Interface

If SBMODE is 1, Following Serial Bus transactions are supported. SBTRIG register initiates this Serial Bus transaction. S is START and SBDEV is SBDEV register. A is ACK, N is NAK, P is STOP.WB1-4, RB1-4 are registers. These Serial Bus transaction start after Value "1" is written into SBMODE register bit. After Serial Bus transaction is successfully completed, SBDONE register bit is set to 1.If Serial Bus transaction had any error including receiving NAK, SBERR register bit is set to 1 with SBDONE=1.RB1-4 registers are valid after receive transaction is completed and SBDONE is set to "1".

Send (Write) transaction: SBRW=0.

WDLEN=1: S – {SBDEV,0b} - A – WB1 – A - P

WDLEN=2: S – {SBDEV,0b} – A – WB1 – A – WB2 – A – P

WDLEN=3: S – {SBDEV,0b} – A – WB1 – A – WB2 – A – WB3 – A – P

WDLEN=4: S – {SBDEV,0b} – A – WB1 – A – WB2 – A – WB3 – A – WB4 – A – P

Receive (Read) transaction1: WREN=1,SBRW=1.

RDLEN=1: S – {SBDEV,0b} – A - WB1 – A – P – S – {SBDEV,1b} – A – RB1 – N – P

RDLEN=2: S – {SBDEV,0b} – A - WB1 – A – P – S – {SBDEV,1b} – A – RB1 – A - RB2 – N – P

RDLEN=3: S – {SBDEV,0b} – A - WB1 – A – P – S – {SBDEV,1b} – A – RB1 – A - RB2 – A – RB3 – N - P

RDLEN=4: S – {SBDEV,0b} – A - WB1 – A – P – S – {SBDEV,1b} – A – RB1 – A - RB2 – A – RB3 – A – RB4 – N - P

Receive (Read) transaction2: WREN=0,SBRW=1.

RDLEN=1: S – {SBDEV,1b} – A - RB1 – N – P

RDLEN=2: S – {SBDEV,1b} – A - RB1 – A - RB2 – N – P

RDLEN=3: S – {SBDEV,1b} – A - RB1 – A - RB2 – A – RB3 – N - P

RDLEN=4: S – {SBDEV,1b} – A - RB1 – A - RB2 – A – RB3 – A – RB4 – N - P

2.4 Audio Processing

2.4.1 Audio clock

Audio Clock is selected by SAMPLE_RATE register. By set the register, we can choose the frequency of audio clock. We have 5 choices, which are 48k, 44.1k, 32k, 16k and 8k. Detailed setting could be described by the register description.

2.4.2 Analog Audio Input

All analog Audio signals should be AC-coupled to these inputs. Audio ADC digitized analog Audio Input signal and generated ADC data. Internal audio processing generates either 8bit mono sound data or 16bit mono sound data from this analog audio input process.

2.5 PCI interface

2.5.1 Interfacing to Serial EEPROM

PCI Configuration Header Location 0x20 contains the subsystem vendor ID and the subsystem ID. Two-wire serial interface can be used to connect an external serial EEPROM, such as 24C02 or 24C02A. When the EEPROM is connected, EC5128 uploads subsystem Vendor ID from the EEPROM after a PCI reset.

After a PCI reset, EC5128 starts a 4-byte sequential read, starting at address 0xFE. If at any time the slave EEPROM issues a NACK, the sequence is aborted and the Subsystem Vendor ID is set to 0x1797. Table 2 shows the content of EEPROM.

Table 2 Register Table in EEPROM

EEPROM device address : 0x50 (7 bits)	
Index	**Value**
0xFE	Subsystem Vendor ID [15:8]
0xFF	Subsystem Vendor ID [7:0]

2.5.2 DMA Controller Instructions

Video Part:

	Bit	Description	SYNCO	SYNCE	JUMP	Line Start	InLine	Dummy
DW0	31-28	Header	1100	1101	1011	1001	1010	1110
	27	IRQ						
	26-24	Data Type	All 0s	All 0s	All 0s	All 0s or 1s	All 0s	All 0s
	23-12	Starting Byte	All 0s	All 0s	All 0s			All 0s
	11-0	Byte Count	All 0s	All 0s	All 0s			All 0s
DW1	31-0	Starting Address	All 0s	All 0s				All 0s

Audio Part:

	Bit	Description	JUMP	Astart	Dummy	SYNCO	SYNCE
DW0	31-28	Header	1011	1001	1110	1100	1101
	27	IRQ					
	26-24	Data Type	All 0s	All 0s	All 0s	All 0s	All 0s
	23-12	Starting Byte	All 0s		All 0s	All 0s	All 0s
	11-0	Byte Count	All 0s		All 0s	All 0s	All 0s
DW1	31-0	Starting Address			All 0s	All 0s	All 0s

In both LineStart and Inline, Starting Byte is a byte location of the video data byte of a scan line from which the DMA operation should start. Byte Count is the number of video data byte should be transferred to the host memory. Starting Address is the host memory address to which the video data should be transferred. The difference between LineStart and InLine is that LineStart also instructs the DMA controller to operate on video data of next video line in the video FIFO. If the image is not cropped or the target memory space is big enough for video data of a scan line, LineStart alone completes a line instruction set. Otherwise, InLine is needed to transfer video data of the same scan line as the previous LineStart. The IRQ field of each instruction is used to instruct the DMA controller to generate an interrupt on PCI bus at the time when the operation of that instruction is completed. If IRQ is set to 1, an interrupt is generated and the DMAPI bit of Interrupt Status register is set to 1 after the completion of the instruction. No interrupt is generated if IRQ is set to 0.

An example of line instruction set

	Instruction	IRQ	Starting Byte	Byte Count	Starting Address
1	LineStart	0	100	400	1000h
2	InLine	0	600	300	1258h
3	InLine	1	1100	200	144Ch
1	LineStart	0	0	1440	2000h

Above is an example of a line instruction set. Assuming that there are 1440 bytes of video data in a scan line. The first instruction in this line instruction set directs DMA controller to discard the first 100 bytes of data and transfer the following 400 bytes of data to host memory space starting from 1000h. After that, in the second instruction, another 100-byte data is discarded because DMA operation starts from 600-th byte of the scan line and lasts for 300 bytes to host memory from 1258h to 1383h. For the third instruction, DMA controller transfers 200 bytes of data to memory space from 144Ch to 1513h. Also, because IRQ is set to 1, an interrupt is generated after the completion of the third instruction. The last instruction shown in gray is a LineStart which is the first instruction of the next line instruction set and implies the end of this line instruction set, so the remaining 140 bytes of video data of this scan line are discarded. Figure 2 shows the result of the scan line to be transferred by the example line instruction set.

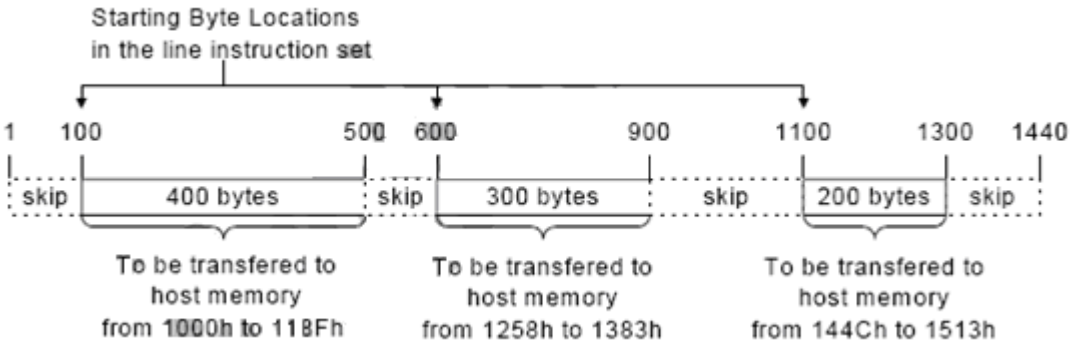
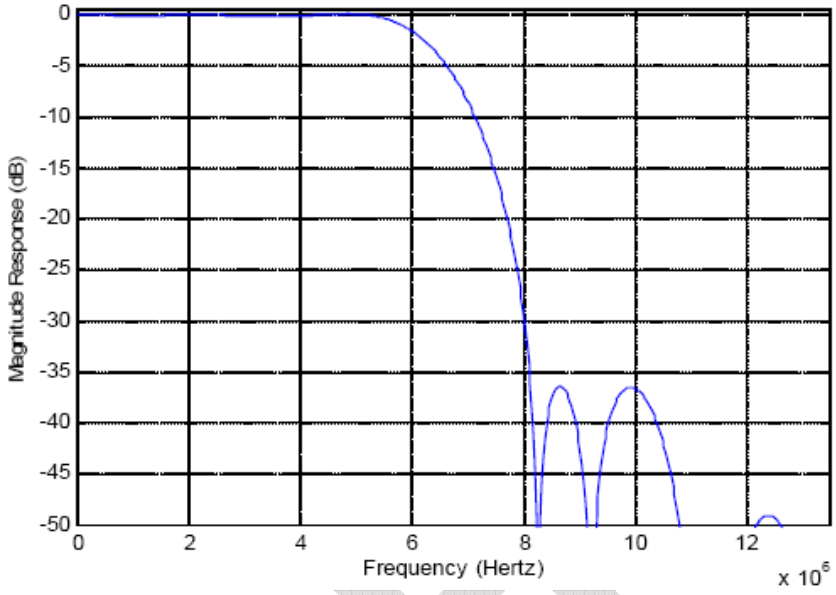


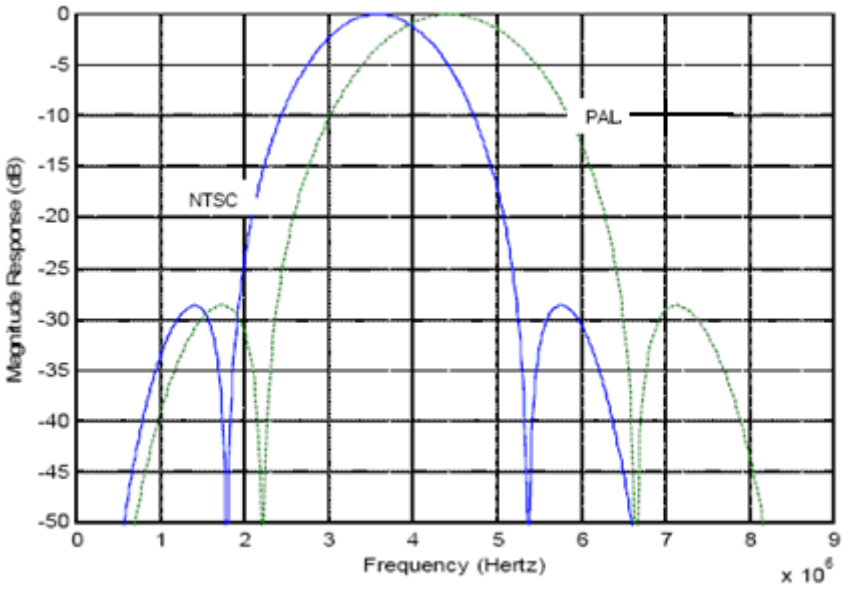
Figure 2. The result of the line instruction set shown above

2.6 Filter Curves

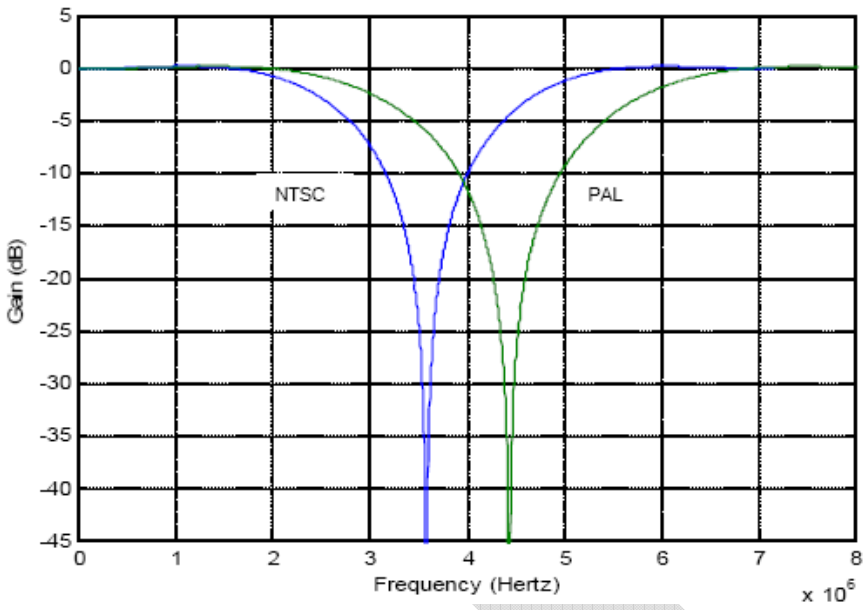
2.6.1 Decimation Filter



2.6.2 Chroma Band Pass Filter Curves



2.6.3 Luma Notch Filter Curve for NTSC and PAL



3. Control Registers

3.1 Register Description

EC5128 supports two types of address spaces. The first one is configuration address space of the pre-defined PCI configuration registers. The second includes all the local registers. The local registers are used to control EC5128 functions and provide status information. Both the PCI configuration address space and the memory address space start at memory location 00h. The PCI based system distinguishes the two address spaces based on the Initialization Device Select, PCI address and command signals that are issued during power on. In this section, the following types are used to indicate how the registers are implemented:

RO: read only. Write has no effect.

WO: write only. Read will produce uncertain value.

R/W: read and write

RR: same as R/W, but writing "1" resets corresponding bit location; writing "0" has no effect.

3.2 PCI Function 0/1/2/3 Configuration Space Registers for Video

0x00 – Vendor ID and Device ID

Bit	Function	R/W	Description	Reset
31-16	Device ID	RO	Device ID Function 0 : 6810h Function 1 : 6811h Function 2 : 6812h Function 3 : 6813h	 6810h 6811h 6812h 6813h
15-0	Vendor ID	RO	PCI vendor ID	1797h

0x04 – Command and Status Register

Bit	Function	R/W	Description	Reset
31,30	Reserved	RO	These bits are hardwired to 0.	0h
29	Received Master Abort	RR	Set when master transaction is terminated with Master Abort.	0
28	Received Target Abort	RR	Set when master transaction is terminated with Target Abort.	0
27	Reserved	RO	This bit is hardwired to 0.	0
26,25	Address Decode Time	RO	Responds with medium DEVSEL timing.	01b
24-22	Reserved	RO	These bits are hardwired to 0.	0h
21	66MHz CAPABLE	RO	This bit is hardwired to 1.	1
20	New Capabilities	RO	A value of 1 indicates that the value read at PCI configuration offset is a pointer in configuration space to a linked list of new capabilities.	1
19-16	Reserved	RO	These bits are hardwired to 0.	0h
15-10	Reserved	RO	These bits are hardwired to 0.	0h
9	Fast Back-to-Back Enable	R/W	This bit should be set to 0 normally.	0
8	SERR# Enable	R/W	This bit should be set to 0 normally.	0
7	Stepping Control	RO	This bit is hardwired to 0.	0
6	Parity Error Response	R/W	This bit should be set to 0 normally.	0

5	VGA Palette Snoop	RO	This bit is hardwired to 0.	0
4	Memory Write and Invalidate Enable	R/W	This bit should be set to 0 normally.	0
3	Special Cycles	R/W	This bit must be set to 0.	0
2	Bus Master	R/W	A value of 1 enables this function space to act as a bus initiator.	0
1	Memory Space	R/W	A value of 1 enables response to memory space accesses (target decoded to memory mapped registers).	0
0	IO Space	RO	This bit is always “0”.	0

0x08 – Revision ID and Class Code

Bit	Function	R/W	Description	Reset
31-8	Class code	RO	This function space is a multimedia video device	040000h
7-0	Revision ID	RO	Revision number	10h

0x0C – Cache Line Size

Bit	Function	R/W	Description	Reset
7-0	Cache Line Size	R/W	This read/write register specifies the system cacheline size in units of DWORDs. These bits should be set to 0 normally.	08h

0x0D – Latency Timer

Bit	Function	R/W	Description	Reset
15-8	Latency Timer	R/W	The number of PCI bus clocks for the latency timer used by the bus master. Once the latency expires, the master must initiate transaction termination as soon as GNT is removed.	40h
7-0	Reserved	R/W		0h

0x0E – Header Type

Bit	Function	R/W	Description	Reset
23-16	Header Type	RO	This chip is Multi-function PCI Device	80h

0x10 – Base Address 0

Bit	Function	R/W	Description	Reset
31-10	Relocatable Memory Pointer	R/W	Determine the location of the registers in the 32-bit addressable memory space.	Assigned by system at boot time
9-0	Memory Usage Specification	RO	Reserve 1kbytes of memory-mapped address space for local registers. Address space is prefetchable without side effects.	000h

0x2C – Subsystem ID and Subsystem Vendor ID

Bit	Function	R/W	Description	Reset
31-16	Subsystem ID	RO	Function 0 : 6810h Function 1 : 6811h Function 2 : 6812h Function 3 : 6813h	6810h 6811h 6812h 6813h
15-0	Subsystem Vendor ID	R/W	Vendor specific.	1797h

0x34 – Capabilities Pointer

Bit	Function	R/W	Description	Reset
7-0	Cap_Ptr	RO	DWORD aligned byte address offset in configuration space to the first item in the list of capabilities.	44h

0x3C – Interrupt Line, Interrupt Pin, Min_Gnt, Max_Lat

Bit	Function	R/W	Description	Reset
31-24	Max_Lat	RO	Require bus access every 18us, at a minimum, in units of 250ns. Affects the desired settings for the latency timer value.	48h
23-16	Min_Gnt	RO	Desire a minimum grant burst period of 8us to empty data FIFO, in units of 250ns. Affects the desired settings for the latency timer value.	20h
15-8	Interrupt Pin	RO	Chip interrupt pin is connected to INTA, the only one usable by a single function device.	01h
7-0	Interrupt Line	R/W	The Interrupt Line register communicates interrupt line routing Information between the POST code and the device driver. The POST code initializes this register with a value specifying to which input (IRQ) of the system interrupt controller the chip interrupt pin is connected. Device driver can use this value to determine interrupt priority and vector information.	System Assigned

0x44 – Power Management Capabilities

Bit	Function	R/W	Description	Reset
31-27	PME_Support	RO	The function does not capable of asserting the PME# signal.	00h
26	D2_Support	RO	The function does not support D2 state.	0
25	D1_Support	RO	The function does not support D1 state.	0
24-22	Aux_Current	RO	The function does not support PME# generation from $D3_{cold}$.	000b
21	DSI	RO	The function requires a device specific initialization sequence following transition to the D0 uninitialized state.	1
20	Reserved	RO		0
19	PME_Clk	RO	No PCI clock is requires for the function to generate PME#.	0
18-16	Version	RO	This function complies with Reversion 1.1 of PCI Power Management Interface Specification.	010b

15-8	Next_Item_Ptr	RO	Pointer to next item in the function's capability list. A value of 0 indicates there is no additional item.	00h
7-0	Cap_ID	RO	PCI power management capability ID.	01h

0x48 – Power Management Control/Status

Bit	Function	R/W	Description	Reset
31-24	Data	RO	The function does not support Data register.	00h
23-16	PMCSR_BSE	RO	The function does not support Bridge Support Extensions.	00h
15	PME_Status	RO	The function does not support PME# generation from $D3_{cold}$.	0
14-13	Data_Scale	RO	The function does not support Data register.	00b
12-9	Data_Select	RO	The function does not support Data register.	0h
8	PME_En	RO	The function does not support PME# generation from $D3_{cold}$.	0
7-2	Reserved	RO		00h
1-0	PowerState	R/W	This field is to determine the current power state of a function and to set the function into a new power state. 00 = D0 01 = D1 10 = D2 11 = $D3_{hot}$	00b

3.3 PCI Function 0/1/2/3 Memory Space Registers for Video

0x000 – VDMAC[31:0]

Bit	Function	R/W	Description	Reset
31-26	Reserved	RO		0
25-24	YSEL	RW	These two bits control the input video selection. 00 = VIN1A selected 01 = VIN1B selected 10 = Reserved 11 = Reserved	0
23-16	Reserved	RO		0
15-8	VDMATRIG	R/W	DMA trigger point. This register defines the number of dwords of data pre-stored in Video FIFO before the DMA controller starts to burst data onto PCI bus.	16h
7-1	Reserved	RO		0
0	VDMAP_EN	R/W	A value of 1 enables the VIDEO DMA Programmer to process DMAP program starting from VDMAP_SA.	0

0x004 – VDMAP_SA

Bit	Function	R/W	Description	Reset
31-0	VDMAP_SA	R/W	The starting address of VIDEO DMAP in the memory address space.	00000000h

0x008 – VDMAP_EXE

Bit	Function	R/W	Description	Reset
31-0	VDMAP_EXE	RO	The dword of DMAP instruction packet that the VIDEO DMA Programmer is currently executing.	00000000h

0x00C – VDMAP_PP

Bit	Function	R/W	Description	Reset
31-0	VDMAP_PP	RO	The memory address of the last dword of VIDEO DMAP in memory address space fetched by the DMA Programmer.	00000000h

0x014 – SBUSC

Bit	Function	R/W	Description	Reset
31-25	SBDEV	R/W	This is the slave device chip address for Hardware mode.	00h
24	SBRW	R/W	Hardware Read/Write mode.1: read, 0:write	1
23	Reserved	RO		0
22-20	RDLEN	R/W	This register defines the number of bytes after Slave Chip Address to the last data byte in Serial Bus Read mode. This value must be 1h to 4h.	1h
19	Reserved	RO		0
18-16	WDLEN	R/W	This register defines the number of bytes after Slave Chip Address to the last data byte in Serial Bus Write mode. This value must be 1h to 4h.	4h
15-8	SBCLK	R/W	This register defines half of the clock period of serial bus in the number of PCI clocks. One clock period = 2xSBCLK PCI clocks. The recommended value is 0xA6 at 99.4kHz and 0x2A at 392.8kHz.	A6h
7	SSDAT	R/W	Read this bit to get the current status of SDAT in both software and hardware modes. In software mode, write a 0 to force SDAT low, write a 1 to release SDAT.	1
6	SSCLK	R/W	Read this bit to get the current status of SCLK in both software and hardware modes. In software mode, write a 0 to force SCLK low, write a 1 to release SCLK.	1

5-2	Reserved	RO		0
1	WREN	R/W	This bit is only effective for Serial Bus Read Protocol. 0:sevd Device Chip address (with Read enable bit) and receive bytes. 1:Send Device Chip Address (with Write enable bit) and send WB1 1 byte, then send Device Chip Address (with Read enable bit) and receive bytes	0
0	SBMODE	R/W	This bit controls the operation of serial bus. 0: software mode. In this mode, driver software can control serial bus directly by reading and writing SSCLK and SSDAT. 1: Hardware mode.	0

0x018 – SBUSSD

Bit	Function	R/W	Description	Reset
31-24	WB4	R/W	The fourth data byte in a serial bus sends transaction.	00h
23-16	WB3	R/W	The third data byte in a serial bus send transaction.	00h
15-8	WB2	R/W	The second data byte in a serial bus send transaction.	00h
7-0	WB1	R/W	The first data byte in a serial bus send transaction after slave device chip address.	00h

0x01C – VDMAP_INTSTAT

Bit	Function	R/W	Description	Reset
31-25	Reserved	RO		0
24	SBERR	RR	Set if the operation on serial bus was completed, but not successful. This bit is valid if SBDONE is set.	0
23-19	Reserved	RO		0
18	NOVIDEO		No video in this channel	0
17-6	Reserved	RO		0

5	DMAPERR	RR	Set if DMA Programmer detects any error occurs on DMAP program.	0
4	Reserved	RO		0
3	Buf_Overflow	RR	Set if Frame Buffer overflow	0
2	Reserved	RO		0
1	VDMAPI	RR	When the IRQ bit in the DMAP instruction packet is set, this bit is set after DMA Programmer completes the Video data instruction.	0
0	SBDONE	RR	Set when serial bus has completed a read or write operation.	0

0x020 – INTMASK

Bit	Function	R/W	Description	Reset
31-0	INTMASK	R/W	Writing a 1 to INTMASK[n] enables the interrupt bit INTSTAT[n].	00000000h

0x030 – SBUSRD

Bit	Function	R/W	Description	Reset
31-24	RB4	RO	The fourth data byte in a serial bus receive transaction.	00h
23-16	RB3	RO	The third data byte in a serial bus receive transaction.	00h
15-8	RB2	RO	The second data byte in a serial bus receive transaction.	00h
7-0	RB1	RO	The first data byte in a serial bus receive transaction after slave device chip address.	00h

0x034 – SBUSTRIG

Bit	Function	R/W	Description	Reset
0	SBTRIG	WO	Write a 1 to trigger hardware state machine to perform Serial bus functions. This bit is rest to “0” automatically. SBMODE must be 1 when this function is used.	0

0x040 – Video Format Select

Bit	Function	R/W	Description	Reset
31-10	Reserved	RO		0
9-8	Video Format	R/W	Video format select of PCI: 00: D1(704x288 per field) 01: CIF(352x288 per field) 10: VGA(640x240 per field) 11: QVGA(320x240 per field)	2'b01
7-0	Reserved	RO		0

0x204 – Switch Mode Control

Bit	Function	R/W	Description	Reset
31-4	Reserved	RO		0
3	SWTCH_EN	R/W	This bit controls video channel work mode. 1'b0 : single channel real-time mode. 1'b1 : switch non-real time mode.	1'b0
2-0	Reserved	RO		1'b0

0x208 – Switch Time Count I

Bit	Function	R/W	Description	Reset
4-0	SWTCH_CNT_H	R/W	Channel switch time counter in non-real time mode, high bits	5'h10

0x20C – Switch Time Count II

Bit	Function	R/W	Description	Reset
7-0	SWTCH_CNT_M	R/W	Channel switch time counter in non-real time mode, middle bits	8'h7A

0x210 – Mode Control

Bit	Function	R/W	Description	Reset
2	FPS_TYPE	R/W	This bits controls video decode mode 0: decode CVBS type 525 lines / 60 fields. 1: decode CVBS type 625 lines / 50 fields.	1'h1
1-0	STD	R/W	Video decode standard in non-auto detect mode: 2'h0: PAL. 2'h1: NTSC. Others reserved	2'h0

0x214 – Soft Reset I

Bit	Function	R/W	Description	Reset
6	RST_ADCS_N	R/W	ADCS module soft reset; If the register's value is 0, pull down the reset signal.	1'h1
5	RST_ATD_N	R/W	Standard Auto Detection module soft reset, If the register's value is 0, pull down the reset signal.	1'h1
4	RST_AGC_N	R/W	Auto Gain Control module soft reset, If the register's value is 0, pull down the reset signal.	1'h1
3	RST_SWTCH_N	R/W	Real Time Work Mode Control module soft reset, If the register's value is 0, pull down the reset signal.	1'h1
2	RST_ITP_N	R/W	Resample module soft reset, If the register's value is 0, pull down the reset signal.	1'h1
1	RST_SYNC_N	R/W	Synchronization module soft reset, If the register's value is 0, pull down the reset signal.	1'h1
0	RST_LPF_N	R/W	Low Pass Filter module soft reset, If the register's value is 0, pull down the reset signal.	1'h1

0x218 – Soft Reset II

Bit	Function	R/W	Description	Reset
3	RST_PIS_N	R/W	Polar Inverse Scaler module soft reset, If the register's value is 0, pull down the reset signal.	1'h1
2	Reserved	R/W		1'h1
1	RST_YUV_N	R/W	Y/C Decode module soft reset, If the register's value is 0, pull down the reset signal.	1'h1
0	RST_VDU_N	R/W	Video Display Unit module soft reset, If the register's value is 0, pull down the reset signal.	1'h1

0x21c – Switch Time Count III

Bit	Function	R/W	Description	Reset
7-0	SWTCH_CNT_L	R/W	Channel switch time counter in non-real time mode, low bits	8'hC0

0x23C – PGA Initial Gain

Bit	Function	R/W	Description	Reset
7-0	PGA_INIT_GAIN	R/W	Control the video ADC PGA gain initial value.	8'h1

0x240 – PGA Max Gain

Bit	Function	R/W	Description	Reset
7-0	PGA_MAX_GAIN	R/W	Control the video ADC PGA gain up range.	8'h3

0x244 – PGA Min Gain

Bit	Function	R/W	Description	Reset
7-0	PGA_MIN_GAIN	R/W	Control the video ADC PGA gain down range.	8'h0

0x250 – Clamp Blank Level Reference

Bit	Function	R/W	Description	Reset
7-0	CLAMP_BLK_REF	R/W	Blank level reference value for clamping.	8'h40

0x254 – Video Sync Mode Control

Bit	Function	R/W	Description	Reset
31-4	Reserved	RO		0
3	VSYNC_PUL_NUM	R/W	This bit set the VSYNC pulse number in video decode: 0: 6 vsync_pulse. 1: 5 vsync_pulse.	1'h1
2-0	Reserved	RO		0

0x26C – Signal Detect Result

Bit	Function	R/W	Description	Reset
1-0	SYNC_CS_RESULT	R	Signal detect result 00: no result. 01: signal exist. 10: no signal.	2'h0

0x280 – Standard Auto Detect Status

Bit	Function	R/W	Description	Reset
3	DET_STATUS	R	Auto detect status: 0: idle. 1: detection in progress.	X
2-0	STD_NOW	R	Current standard invoked: 0 = PAL(B,D,G,H,I). 1 = NTSC(M). Others: Not Valid.	X

0x284 – Standard Selection Mode

Bit	Function	R/W	Description	Reset
2-0	ATD_STD	R/W	Standards selected: 0 = select PAL(B,D,G,H,I) mode. 1 = select NTSC(M) mode. 7 = select Auto detection mode. Others reserved	3'h0

0x288 – Standard Enable for Auto Detect

Bit	Function	R/W	Description	Reset
1	NTSCM_EN	R/W	1: enable recognition of NTSC(M). 0: disable recognition.	1'h1
0	PALD_EN	R/W	1: enable recognition of PAL(B, D, G, H, I). 0: disable recognition.	1'h1

0x28C – Auto Detect Start

Bit	Function	R/W	Description	Reset
0	ATD_ATSTART	W	Writing 1 to this bit will manually initiate the standard auto detection.	1'h0

0x290 – Line Number I

Bit	Function	R/W	Description	Reset
1-0	VLENGTH_H	R/W	Line number of one frame, high bits	2'h2

0x294 – Line Number II

Bit	Function	R/W	Description	Reset
7-0	VLENGTH_L	R/W	Line number of one frame, low bits	8'h71

0x328 – CBP Type Control

Bit	Function	R/W	Description	Reset
3	CBP_TYPE	R/W	Chroma band pass filter type control: 0: NTSC BPF. 1: PAL BPF.	1'h1
2-0	Reserved	R/W		3'h0

0x32C – FSC Frequency I

Bit	Function	R/W	Description	Reset
1-0	CB_FREQ_HH	R/W	Sub carrier frequency value, PAL-D default value is 44336/256. NTSC-M default value is 35795/256 fsc * Sampl_Rate*2^BitNum_NCO in PAL = 4.43361875 / 13.5 * 2^26 = 26'd22039639 = 26'h1504c57	2'h1

0x330 – FSC Frequency II

Bit	Function	R/W	Description	Reset
7-0	CB_FREQ_H	R/W	High part of sub carrier frequency.	8'h50

0x334 – FSC Frequency III

Bit	Function	R/W	Description	Reset
7-0	CB_FREQ_M	R/W	Middle part of sub carrier frequency.	8'h4c

0x338 – FSC Frequency IV

Bit	Function	R/W	Description	Reset
7-0	CB_FREQ_L	R/W	Low part of sub carrier frequency.	8'h56

0x358 – Active Video and Color Burst Position

Bit	Function	R/W	Description	Reset
7-6	SAV_LINE_H	R/W	High Bits of active video start position in one line	2'h0
5-4	EAV_LINE_H	R/W	High Bits of active video end position in one line	2'h3
3-2	SCB_LINE_H	R/W	High Bits of color burst start position in one line.	2'h0
1-0	ECB_LINE_H	R/W	High Bits of color burst end position in one line.	2'h0

0x35C – Active Video Start Position

Bit	Function	R/W	Description	Reset
7-0	SAV_LINE_L	R/W	Low bits of active video start position in one line PAL-D: 132 (0x84) (default) NTSC: 122 (0x7A)	8'h84

0x360 – Active Video End Position

Bit	Function	R/W	Description	Reset
7-0	EAV_LINE_L	R/W	Low bits of active video end position in one line PAL-D: 851 (0x353) (default) NTSC: 841 (0x349)	8'h53

0x364 – Color Burst Start Position

Bit	Function	R/W	Description	Reset
7-0	SCB_LINE_L	R/W	Low bits of color burst start position in one line. PAL-D: 76 (0x4c) (default)	8'h4C

0x368 – Color Burst End Position

Bit	Function	R/W	Description	Reset
7-0	ECB_LINE_L	R/W	Low bits of color burst end position in one line. PAL-D: 103 (0x67) (default)	8'h67

0x36C – Active Line Control

Bit	Function	R/W	Description	Reset
7-6	SAV_FLD_TOP_H	R/W	In top field, active video start line number, high bits	2'h0
5-4	EAV_FLD_TOP_H	R/W	In top field, active video end line number, high bits	2'h1
3-2	SAV_FLD_BOT_H	R/W	In bottom field, active video start line number, high bits	2'h1
1-0	EAV_FLD_BOT_H	R/W	In bottom field, active video end line number, high bits	2'h2

0x370 – Active Line in Top Field I

Bit	Function	R/W	Description	Reset
7-0	SAV_FLD_TOP_L	R/W	In top field, active video start line number, low bits. In PAL-D, 22(0x16) (default) In NTSC, 19 (0x13)	8'h16

0x374 – Active Line in Bottom Field II

Bit	Function	R/W	Description	Reset
7-0	EAV_FLD_TOP_L	R/W	In top field, active video end line number, low bits. In PAL-D, 309(0x135) (default) In NTSC, 257 (0x101)	8'h35

0x378 – Active Line in Bottom Field I

Bit	Function	R/W	Description	Reset
7-0	SAV_FLD_BOT_L	R/W	In bottom field, active video start line number, low bits. In PAL-D, 335(0x14f) (default) In NTSC, 257 (0x11b)	8'h4F

0x37C – Active Line in Bottom Field II

Bit	Function	R/W	Description	Reset
7-0	EAV_FLD_BOT_L	R/W	In bottom field, active video end line number, low bits. In PAL-D, 622(0x26e) (default) In NTSC, 521 (0x209)	8'h6E

0x380 – Color Burst Line Control

Bit	Function	R/W	Description	Reset
7-6	SCB_FLD_TOP_H	R/W	In top field, color burst start line number, high bits.	2'h0
5-4	ECB_FLD_TOP_H	R/W	In top field, color burst end line number, high bits.	2'h1
3-2	SCB_FLD_BOT_H	R/W	In bottom field, color burst start line number, high bits	2'h1
1-0	ECB_FLD_BOT_H	R/W	In bottom field, color burst end line number, high bits	2'h2

0x384 – Color Burst Line in Top Field I

Bit	Function	R/W	Description	Reset
7-0	SCB_FLD_TOP_L	R/W	In top field, color burst start line number, low bits. In PAL-D, 6 (default)	8'h7

0x388 – Color Burst Line in Top Field II

Bit	Function	R/W	Description	Reset
7-0	ECB_FLD_TOP_L	R/W	In top field, color burst end line number, low bits. In PAL-D, 307 (0x133) (default), after +1 = 0x134.	8'h34

0x38C – Color Burst Line in Bottom Field I

Bit	Function	R/W	Description	Reset
7-0	SCB_FLD_BOT_L	R/W	In bottom field, color burst start line number, low bits. In PAL-D, 319 (0x13f) (default), after +1 = 0x140.	8'h40

0x390 – Color Burst Line in Bottom Field II

Bit	Function	R/W	Description	Reset
7-0	ECB_FLD_BOT_L	R/W	In bottom field, color burst end line number, low bits. In PAL-D, 621 (0x26d) (default).	8'h6D

0x3D8 – CTI and Frame Rate Control

Bit	Function	R/W	Description	Reset
4	CTI_SUB_DIF	R/W	1: original signal minus diff value. 0: original signal add diff value.	1'h0
3	CTI_Y_BYPS	R/W	1: bypass y channel of CTI. 0: do y channel CTI.	1'h1
2	CTI_UV_BYPS	R/W	1: bypass uv channel of CTI. 0: do uv channel CTI..	1'h1
1	FRM_DROP_EN	R/W	1: drop one frame every two frame. 0: do not drop frame.	1'h0
0	FLD_DROP_EN	R/W	1: remove bottom field. 0: do not remove bottom field.	1'h0

0x3DC– U Scale Coefficient

Bit	Function	R/W	Description	Reset
7-0	U_SCALE_COEF	R/W	U scale coefficient, U_out = U_original * U_MUTE_COEF / 128	8'h40

0x3E0 – V Scale Coefficient

Bit	Function	R/W	Description	Reset
7-0	V_SCALE_COEF	R/W	V scale coefficient V_out = V_original * V_MUTE_COEF / 128	8'h40

0x3E4 – Y Scale Coefficient

Bit	Function	R/W	Description	Reset
7-0	Y_SCALE_COEF	R/W	Y scale coefficient Y_out = Y_original * Y_MUTE_COEF / 128	8'h40

0x3E8 – Horizontal Crop Control I

Bit	Function	R/W	Description	Reset
7-6	HACTIVE_H	R/W	The number of active video pixels (horizontal) high bits	2'h2
5-0	HDELAY	R/W	The number of cropping the left horizontal data.	6'h8

0x3EC – Horizontal Crop Control II

Bit	Function	R/W	Description	Reset
7-0	HACTIVE_L	R/W	The number of active video pixels (horizontal) low 8 bits.	8'hC0

0x3F0 – Vertical Crop Control I

Bit	Function	R/W	Description	Reset
7-6	VACTIVE_ H	R/W	The number of active video line (vertical) high bits	2'h1
5-0	VDELAY	R/W	The number of video line cropping (vertical).	6'h0

0x3F4 – Vertical Crop Control II

Bit	Function	R/W	Description	Reset
7-0	VACTIVE_LO	R/W	The number of active video line (vertical) low 8 bits.	8'h20

0x3F8 – Scaler Decimation Control

Bit	Function	R/W	Description	Reset
3-2	HOR_DEC	R/W	Indicate the decimation style in horizontal direction. 0: no decimation. 1: pick one point in every two points. 2: pick one point in every four points.	2'h0
1-0	VER_DEC	R/W	Indicate the decimation style in vertical direction. 0: no decimation. 1: remove one line in two lines. 2: remove one line in three lines. 3: remove one line in four lines.	2'h0

0x3FC – Display Control

Bit	Function	R/W	Description	Reset
2-1	DISPLAY_MODE	R/W	Control output image format. 0: YCbCr 4:2:2. 1: RGB 5:6:5.	2'h0
0	COLOR_CVT_MODE	R/W	Color format convertion control: 0: YUV to RGB. 1: YIQ to RGB.	1'h0

3.4 PCI Function 4/5/6/7 Configuration Space Registers for Audio

0x00 – Vendor ID and Device ID

Bit	Function	R/W	Description	Reset
31-16	Device ID	RO	Device ID Function 4 : 6814h Function 5 : 6815h Function 6 : 6816h Function 7 : 6817h	 6814h 6815h 6816h 6817h
15-0	Vendor ID	RO	PCI vendor ID	1797h

0x04 – Command and Status Register

Bit	Function	R/W	Description	Reset
31,30	Reserved	RO	These bits are hardwired to 0.	0h
29	Received Master Abort	RR	Set when master transaction is terminated with Master Abort.	0
28	Received Target Abort	RR	Set when master transaction is terminated with Target Abort.	0
27	Reserved	RO	This bit is hardwired to 0.	0
26,25	Address Decode Time	RO	Responds with medium DEVSEL timing.	01b
24-22	Reserved	RO	These bits are hardwired to 0.	0h
21	66MHz CAPABLE	RO	This bit is hardwired to 1.	1
20	New Capabilities	RO	A value of 1 indicates that the value read at PCI configuration offset is a pointer in configuration space to a linked list of new capabilities.	1
19-16	Reserved	RO	These bits are hardwired to 0.	0h
15-10	Reserved	RO	These bits are hardwired to 0.	0h
9	Fast Back-to-Back Enable	R/W	This bit should be set to 0 normally.	0
8	SERR# Enable	R/W	This bit should be set to 0 normally.	0
7	Stepping Control	RO	This bit is hardwired to 0.	0

6	Parity Error Response	R/W	This bit should be set to 0 normally.	0
5	VGA Palette Snoop	RO	This bit is hardwired to 0.	0
4	Memory Write and Invalidate Enable	R/W	This bit should be set to 0 normally.	0
3	Special Cycles	R/W	This bit must be set to 0.	0
2	Bus Master	R/W	A value of 1 enables this function space to act as a bus initiator.	0
1	Memory Space	R/W	A value of 1 enables response to memory space accesses (target decoded to memory mapped registers).	0
0	IO Space	RO	This bit is always “0”.	0

0x08 – Revision ID and Class Code

Bit	Function	R/W	Description	Reset
31-8	Class code	RO	This function space is a multimedia video device	048000h
7-0	Revision ID	RO	Revision number	10h

0x0C – Cache Line Size

Bit	Function	R/W	Description	Reset
7-0	Cache Line Size	R/W	This read/write register specifies the system cacheline size in units of DWORDs. These bits should be set to 0 normally.	08h

0x0D – Latency Timer

Bit	Function	R/W	Description	Reset
15-8	Latency Timer	R/W	The number of PCI bus clocks for the latency timer used by the bus master. Once the latency expires, the master must initiate transaction termination as soon as GNT is removed.	40h
7-0	Reserved	R/W		0h

0x0E – Header Type

Bit	Function	R/W	Description	Reset
23-16	Header Type	RO	This chip is Multi-function PCI Device	80h
15-0	Reserved	R/W		0h

0x10 – Base Address 0

Bit	Function	R/W	Description	Reset
31-10	Relocatable Memory Pointer	R/W	Determine the location of the registers in the 32-bit addressable memory space.	Assigned by system at boot time
9-0	Memory Usage Specification	RO	Reserve 1kbytes of memory-mapped address space for local registers. Address space is prefetchable without side effects.	00h

0x2C – Subsystem ID and Subsystem Vendor ID

Bit	Function	R/W	Description	Reset
31-16	Subsystem ID	RO	Function 0 : 6814h Function 1 : 6815h Function 2 : 6816h Function 3 : 6817h	6814h 6815h 6816h 6817h
15-0	Subsystem Vendor ID	R/W	Vendor specific.	1797h

0x34 – Capabilities Pointer

Bit	Function	R/W	Description	Reset
7-0	Cap_Ptr	RO	DWORD aligned byte address offset in configuration space to the first item in the list of capabilities.	44h

0x3C – Interrupt Line, Interrupt Pin, Min_Gnt, Max_Lat

Bit	Function	R/W	Description	Reset
31-24	Max_Lat	RO	Require bus access every 18us, at a minimum, in units of 250ns. Affects the desired settings for the latency timer value.	48h
23-16	Min_Gnt	RO	Desire a minimum grant burst period of 8us to empty data FIFO, in units of 250ns. Affects the desired settings for the latency timer value.	20h
15-8	Interrupt Pin	RO	Chip interrupt pin is connected to INTA, the only one usable by a single function device.	01h
7-0	Interrupt Line	R/W	The Interrupt Line register communicates interrupt line routing Information between the POST code and the device driver. The POST code initializes this register with a value specifying to which input (IRQ) of the system interrupt controller the chip interrupt pin is connected. Device driver can use this value to determine interrupt priority and vector information.	System Assigned

3.5 PCI Function 4/5/6/7 Memory Space Registers for Audio

0x210 – Audio Mode Control

Bit	Function	R/W	Description	Reset
4	FPS_TYPE	R/W	Synchronization to video format 1: current video is 50 fields/s 0: current video is 59.94 fields/s	1'b1
3-2	Reserved			
1	AAMPMD	R/W	Audio auto detect working mode: 0: absolute amplitude auto detect mode. 1: differential amplitude auto detect mode	1'b0
0	AUDIO_MODE	R/W	Audio function mode. 0h: 8bit mono sample from internal ADC. 1h: 16bit mono sample from internal ADC.	1'b0

0x214 – Audio Mix Control

Bit	Function	R/W	Description	Reset
7	MIX_DERATIO	R/W	Disable the mixing ratio value for all audio. 0:Apply individual mixing ratio value for each audio 1:Apply nominal value for all audio commonly	1'b0
6	MRATIO_MD	R/W	Audio Mixing ratio value divider control 0: MIX_RATIO default value 1: MIX_RATIO / 64	1'b0
5-0	MIX_RATIO	R/W	If MRATIOMD=0(default) : Mix Ratio Value 0 0.25 (default) Recommended for most cases. 1 0.31 2 0.38 3 0.44	6'h0

			4 0.50 5 0.63 6 0.75 7 0.88 8 1.00 9 1.25 10 1.50 11 1.75 12 2.00 13 2.25 14 2.50 15 2.75 If MRATIOMD=1,Mixing ratio is MIX_RATIOn / 64.	

0x220 – Audio Output Law Mode

Bit	Function	R/W	Description	Reset
1-0	LAWMD	R/W	Choose the output law mode. 0: PCM output. 1: SB(Signed MSB bit in PCM data is inverted) output. 2: u-Law output. 3: A-Law output.	2'b1

0x224 – Audio Soft Reset

Bit	Function	R/W	Description	Reset
2	RST_ADC	R/W	0: Pull down the reset signal in ADC module to reset all registers. 1: No change.	1'b1
1-0	Reserved	R/W		2’b11

0x22C – Audio ADC Digtial Input Offset Control I

Bit	Function	R/W	Description	Reset
7-0	DC_OFFSET[7:0]	R/W	Set the Audio DC offset register's low 8 bit. Digital ADC input data offset control.Digital ADC input data is adjusted by ADJAADCn = AUDnADC + AADCnOFS. AUDnADC is 2's formatted Analog Audio ADC output. AADCnOFS is adjusted offset value by 2's format.	8'b0

0x230 – Audio ADC Digital Input Offset Control II

Bit	Function	R/W	Description	Reset
1-0	DC_OFFSET[9:8]	R/W	Set the Audio DC offset register's high 2 bit.	2'b0

0x234 – Audio Detection

Bit	Function	R/W	Description	Reset
7-5	ADET_FLT	R/W	Select the filter for audio detection. 0: wide LPF(default) . . . 7:Narrow LPF.	3'b0
4-0	ADET_TH	R/W	Define the threshold value for audio detection. 0: low value. . . 31: high value.	5'b0

0x23C – Audio ADC Sample Rate

Bit	Function	R/W	Description	Reset
2-0	SAMPLE_RATE	R/W	Define audio ADC sample rate. 0: 48k sample rate. 1: 44.1k sample rate. 2: 32k sample rate. 3: 16k sample rate. 4: 8k sample rate.	3'b1

0x240 – Adjusted Analog Audio ADC Digital Input Value I

Bit	Function	R/W	Description	Reset
7-0	ADJAADC[7:0]	R	Bit7-0 of adjusted Audio ADC Digital Input Data Value.	X

0x244 – Adjusted Analog Audio ADC Digital Input Value II

Bit	Function	R/W	Description	Reset
1-0	ADJAADC[9:8]	R	Bit9-8 of adjusted Audio ADC Digital Input Data Value.	X

0x248 – Analog Audio ADC Digital Output Value I

Bit	Function	R/W	Description	Reset
7-0	AUDADC[7:0]	R	Bit7-0 of Analog Audio ADC Digital Output Data Value.	X

0x24C –Analog Audio ADC Digital Output Value II

Bit	Function	R/W	Description	Reset
1-0	AUDADC[9:8]	R	Bit9-8 of Analog Audio ADC Digital Output Data Value.	X

0x250 – Audio Detect Status

Bit	Function	R/W	Description	Reset
1	DETECT_AUDIO	R	1: Audio detected. 0: No audio detected.	X
0	LOST_AUDIO	R	1: Audio lost.	X

0x2F8 – Audio ADC Control

Bit	Function	R/W	Description	Reset
2	ADC_PD	R/W	1: Set the ADC in power down mode. 0: ADC in normal mode.	1'h0
1	ADC_CLK_POL	R/W	Define the ADC clock's polarity. 0: Inverse the clock’s polarity. 1: Normal	1'h1
0	ADC_CLK_EN	R/W	1: Enable the ADC's clock. 0: Not enable.	1'h1

4. Application Information

4.1 Video Input Interface

The EC5128 has a built-in 2:1 input MUX for software controllable input selections. This MUX can be used to select one composite video source of 2 input video sources. For a typical application, a video input should be first terminated with a 75-ohm resistor before it is AC coupled by a 0.1uF capacitor to the input of the MUX.

4.2 A/D Converter

The EC5128 has four internal A/D converters to cover all possible analog video signal sources. The reference supply generator for the A/D converter is also on-chip.

4.3 Clamping/AGC

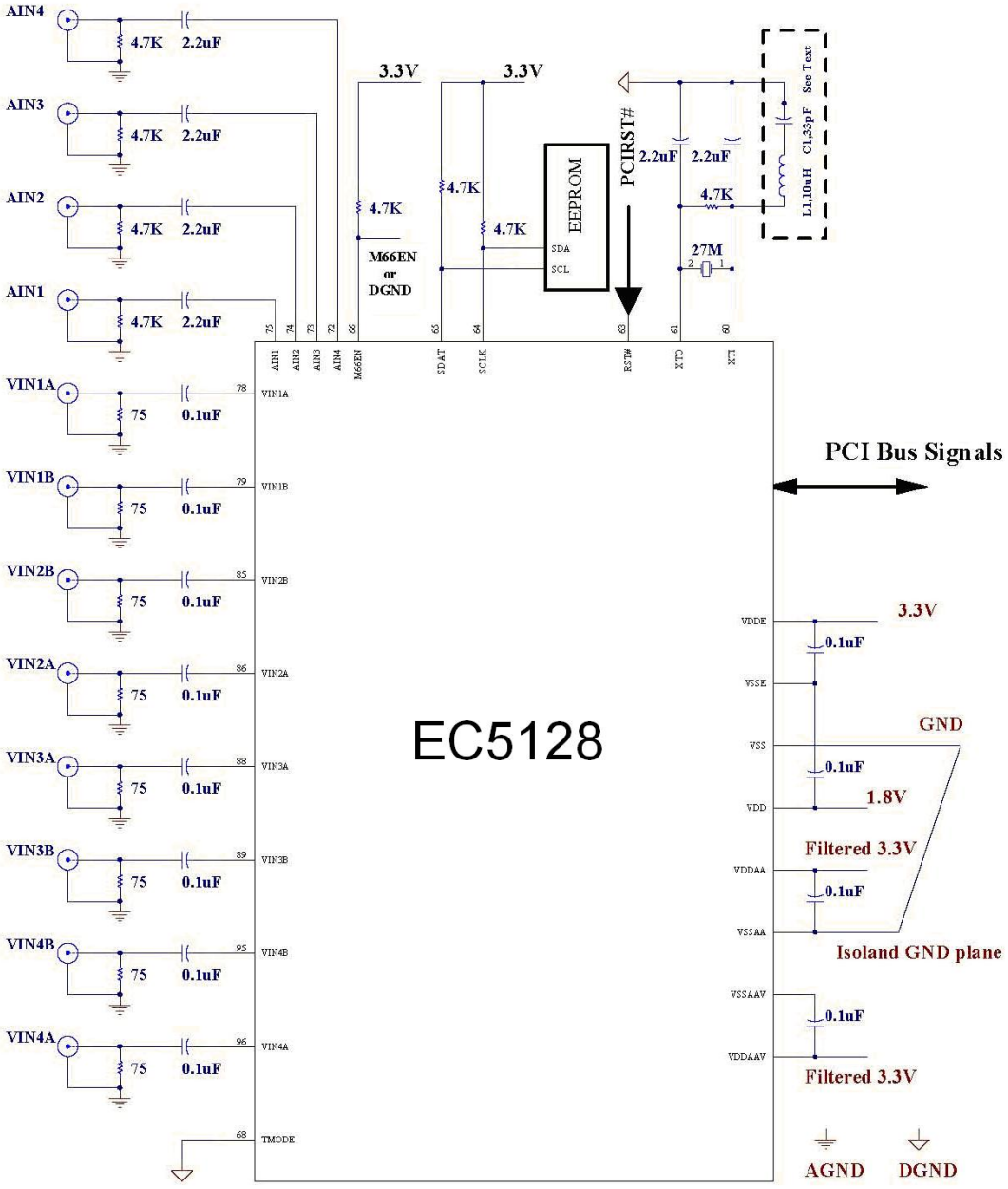
The EC5128 has built-in automatic clamping control circuitry. No extra external component is needed for this operation. The clamping loop gain can be controlled through register setting. The EC5128 also has built-in automatic AGC control circuitry. The AGC loop gain can also be controlled by register. The AGC loop response time is also register programmable.

4.4 Clock Generation

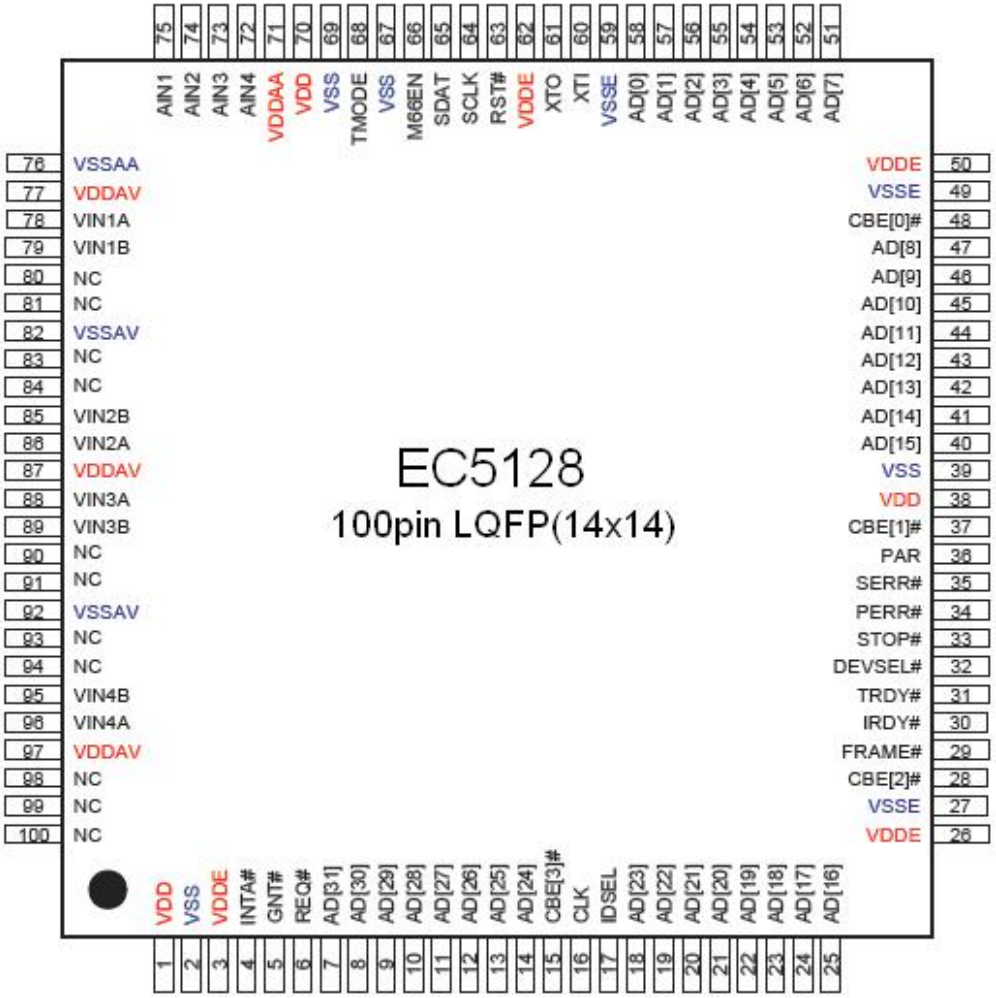
The EC5128 requires one 27MHz crystal connected to XTI and XTO for all format decoding. The default crystal type should be 27MHz, fundamental mode, 20pF load capacitance or less, +-50ppm, and with series resistance of 80 ohm or less. An external clock source of 27MHz can also be connected to the XTI input in place of the crystal. A typical 27MHz third overtone crystal circuit is shown in the following figure.

4.5 Application Schematics

Following pages show typical application schematics with EC5128.



5. Pin Diagram



6. Pin Description

6.1 PCI Interface Pins

Name	Number	Type	Description
CLK	16	I	This input provides timing for all PCI transactions. All PCI signals except RST and INTA are sampled on the rising edge of CLK, and all other timing parameters are defined with respect to this edge. The EC5128 supports a PCI clock up to 66MHz.
RST#	63	I	This input three-states all PCI signals asynchronous to the CLK signal.
GNT#	5	I	Agent granted bus.
REQ#	5	I	Agent desires bus.
IDSEL	17	I	This input is used to select the EC5128 during configuration read and write transactions.
AD[31:0]	7-14,18-25,40-47, 51-58	I/O	These tri-states, bi-directional, I/O pins transfer both address and data information. A bus transaction consists of an address phase followed by one or more data phases for either read or write operations.
CBE#[3:0]	15,28,37, 48	I/O	These three-state, bi-directional, I/O pins transfer both bus command and byte enable information. During the address phase of a transaction, CBE#[3:0] contain the bus command. During the data phase, CBE#[3:0] are used as byte enables.
PAR	36	I/O	This tri-state, bi-directional, I/O pin provides even parity across AD[31:0] and CBE[3:0]. This means that the number of 1's on PAR, AD[31:0], and CBE[3:0] equals an even number.
FRAME#	29	I/O	This sustained tri-state signal is driven by the current master to indicate the beginning and duration of an access
IRDY#	30	I/O	This sustained tri-state signal indicates the bus master's readiness to complete the current data phase. IRDY is used in conjunction with TRDY.
TRDY#	31	I/O	This sustained tri-state signal indicates the target's readiness to complete the current data phase. RTDY is used in conjunction with IRDY.
DEVSEL#	32	I/O	This sustained tri-state signal indicates device selection. When actively driven, DEVSEL indicates the driving

			device has decoded its address as the target of the current access.
STOP#	33	I/O	This sustained tri-state signal indicates the target is requesting the master to stop the current transaction.
PERR#	34	I/O	Report data parity error.
SERR#	35	O	Report address parity error. Open drain.
INTA#	4	O	This signal is an open drain output for interrupts.
M66EN	66	I	Connect M66EN on PCI Bus connector with Pull-up. If connected to digital GND, PCI Bus Interface is always working with 33MHz PCI clock mode.

6.2 Analog Video/Audio Interface Pins

Name	Number	Type	Description
VIN1A	78	A	Composite video input A of channel 1.
VIN1B	79	A	Composite video input B of channel 1.
VIN2A	86	A	Composite video input A of channel 2.
VIN2B	85	A	Composite video input B of channel 2.
VIN3A	88	A	Composite video input A of channel 3.
VIN3B	89	A	Composite video input B of channel 3.
VIN4A	96	A	Composite video input A of channel 4.
VIN4B	95	A	Composite video input B of channel 4.
AIN1	75	A	Audio input of channel 1.
AIN2	74	A	Audio input of channel 2.
AIN3	73	A	Audio input of channel 3.
AIN4	72	A	Audio input of channel 4.

6.3 Two-wire Serial Interface Pins

Name	Number	Type	Description
SCLK	64	I/O	Serial clock
SDAT	65	I/O	Serial data

6.4 Video Decoder Clock Pins

Name	Number	Type	Description
XTI	60	I	Clock Zero Pins. A 27MHz fundamental (or third harmonic) crystal can be connected directly to this pin or a single-ended oscillator can be connected

			to XTI.
XTO	61	O	For crystal 27MHz connection.

6.5 Test Pins

Name	Number	Type	Description
TMODE	68	I	Test Input pin. It must be connected to Digital ground during normal operation.

6.6 Power and Ground Pins

Name	Number	Type	Description
VDD	1,38,70	P	1.8V Power for digital circuitry. All VDD pins must be connected together as close to the device as possible. A 0.1uF ceramic capacitor should be connected between each group of VDD pins and the digital ground plane as close to the device as possible.
VSS	2,39,67,69	G	Core power return. Ground for digital circuitry.
VDDE	3,26,50,62	P	3.3v power supply for IO Pad. A 0.1uF ceramic capacitor should be connected between each group of VDDE pins and the ground plane as close to the device as possible.
VSSE	27,49,59	G	I/O power return
VDDAA	71	P	3.3v power supply for analog audio circuits. A 0.1uF ceramic capacitor should be connected between each group of VDDAA pins and the ground plane as close to the device as possible.
VSSAA	76	G	Analog 3.3v power return for analog audio circuits.
VDDAV	77,87,97	P	3.3v power supply for analog video circuits. All VDDAV pins must be connected together as close to the device as possible. A 0.1uF ceramic capacitor should be connected between each group of VDDAV pins and the analog ground plane as close to the device as possible.
VSSAV	82,92	G	Analog 3.3v power return for analog video circuits.

7. Parametric Information

7.1 AC/DC Electrical Parameters

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	units
VDDAV(measured to VSSAV)	V_{DDAVM}	3.0	3.3	3.6	V
VDDAA(measured to VSSAA)	V_{DDAAM}	3.0	3.3	3.6	V
VDD(measured to VSS)	V_{DDM}	1.6	1.8	2.0	V
Voltage on any signal pin(See the note below)	-	V_{SS}-0.5	-	V_{DDM}+0.5	V
Analog Input Voltage	-	VSSAV-0.5	-	V_{DDAVM}+0.5	V
		VSSAA-0.5	-	V_{DDAAM}+0.5	V
Storage Temperature	T_S	-65	-	+150	°C
Junction Temperature	T_J	-	-	+125	°C
Vapor Phase Soldering(15 Seconds)	T_{VSOL}	-	-	+220	°C

◆ Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation at these or any other conditions above those listed in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5v or drops below ground by more than 0.5v can induce destructive latchup.

Characteristics

Parameter	Symbol	Min	Typ	Max	units
Supply					
Power Supply - IO	VDDE	3.15	3.3	3.6	V
Power Supply - Analog	VDDAV	3.15	3.3	3.6	V
Power Supply - Digital	VDD	1.6	1.8	2.0	V

Maximum [VDDIO-VDDAV]					V
Maximum [VDDIO-VDDAA]					V
VIN1A,VIN1B,VIN2A,VIN2B, VIN3A,VIN3B,VIN4A,VIN4B		0.5	1.0	1.4	V
AIN1,AIN2,AIN3,AIN4 Input Range		0.5	1.0	2.0	V
Ambient Operation Temperature	T_A	0		70	°C
Analog Core Supply current - Video	VDDAV	-	TBD	-	mA
Analog Core Supply current - Audio	VDDAA	-	TBD	-	mA
Digital IO Supply current	VDDE	-	TBD	-	mA
Digital Core Supply current	VDD	-	TBD	-	mA
Digital Inputs					
Input High Voltage(TTL)	V_{IH}	2.0	-	VDDE+0,5	V
Input Low Voltage(TTL)	VIL	-	-	0.8	V
Input High Voltage(XTI)	VIH	2.0	-	VDDE+0.5	V
Input Low Voltage(XTI)	VIL	VSS-0.5	-	1.0	V
Input High Current(VIN=VDD)	IIH	-	-	10	uA
Input Low Current(VIN=VSS)	IIL	-	-	-10	uA
Input Capacitance(f=1MHz,VIN=2.4V)	CIN	-	5	-	pF
Digital Outputs					
Output High Voltage(IOH=4mA)	VOH	2.4	-	VDDE	V
Output Low Voltage(IOL=-4mA)	VOL	-	0.2	0.4	V
Tri-state Current	IOZ	-	-	10	uA
Output Capacitance	CO	-	5	-	pF
Analog Input					
Analog Pin Input Voltage	VI	-	1	-	Vpp
Analog Pin Input Capacitance	CA	-	7	-	pF
Crystal Spec					
Nominal frequency(fundamental)		-	27	-	MHz
deviation		-	-	±50	ppm
Temperature range	Ta	0	-	70	°C
Load capacitance	CL	-	20	-	pF
Series resistor	RS	-	80	-	Ohm
Oscillator Input					
Nominal frequency		-	27	-	MHz
Deviation		-	-	±50	ppm
Duty cycle		45	-	55	%

7.2 Video Decoder Parameters 1

Parameter	Symbol	Min	Typ	Max	units
ADCs					
ADC resolution	ADCR	-	10	-	Bits
ADC integral Non-linearity	AINL	-	±1	-	LSB
ADC differential non-linearity	ADNL	-	±1	-	LSB
ADC clock rate	f_{ADC}	-	27	-	MHz
Horizontal PLL					
Line frequency(50Hz)	f_{LN}	-	15.625	-	KHz
Line frequency(60Hz)	f_{LN}	-	15.734	-	KHz
Static deviation	$\triangle f_H$	-	-	6.2	%
Subcarrier PLL					
subcarrier frequency(NTSC-M)	f_{SC}	-	3579545	-	Hz
subcarrier frequency(PAL-BDGHI)	f_{SC}	-	4433619	-	Hz
subcarrier frequency(PAL-M)	f_{SC}	-	3575612	-	Hz
subcarrier frequency(PAL-N)	f_{SC}	-	3582056	-	Hz
Lock in range	$\triangle f_H$	±450	-	-	Hz
Oscillator Input					
nominal frequency		-	27	-	MHz
deviation		-	-	±50	ppm
duty cycle		-	-	55	%

7.3 Video Decoder Parameters 2

Parameter	Symbol	Min	Typ	Max	units
Lock Specification					
Sync Amplitude Range		1	-	200	%
Color Burst Range		5	-	200	%
Horizontal Lock Range		-5	-	5	%
Vertical Lock Range		45	-	65	Hz
F_{SC} Lock Range		-	±450	-	Hz
Color Burst Position Range		-	±2.2	-	us
Color Burst Width Range		-		-	cycle
Video Bandwidth					
Bandwidth		-	6	-	MHz
Noise Specification					
SNR(Luma flat field)		-	57	-	dB
Nonlinear Specification					
Y Nonlinearity		-	0.5	0.7	%
Differential Phase		-	0.4	0.6	Degree
Differential Gain		-	0.6	0.8	%
Chroma Specification					
Hue Accuracy		-	1	-	Degree
Chroma ACC Range		-	-	400	%
Chroma Amplitude Error		-	1	-	%
Chroma Phase Error		-	0.3	-	%
Chroma Luma Intermodulation		-	0.2	-	%
K-Factor					
K_{2T}		-	0.5	-	%
$K_{pulse/bar}$		-	0.5	-	%

7.4 Analog Audio Parameters

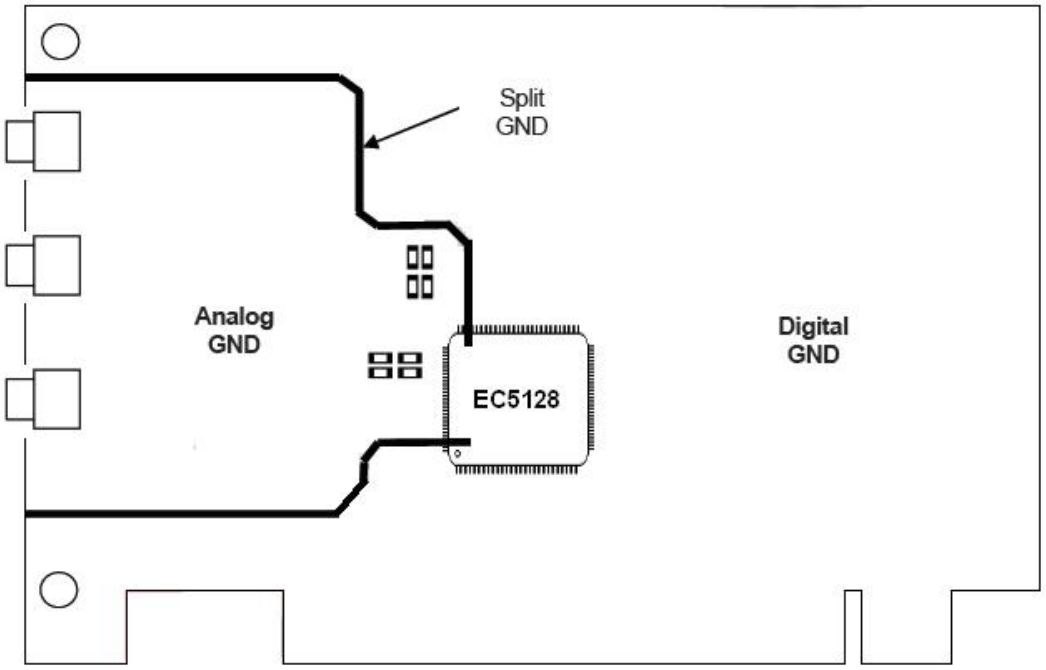
Parameter	Symbol	Min	Typ	Max	units
Analog Audio Input Characteristics					
AIN-5 Input Impedance	RINX	10	-	-	Kohm
Inter-channel gain mismatch		-	0.2	-	dB
Input voltage range		-	-	2	Vpp
Full scale input voltage[1]	V_{iFULL}	-	1	-	Vpp
Inter-channel isolation[2]		-	90	-	dB
Analog Audio Output Characteristics					
AOUT Output Load Resistance	RLAO	2K	10K	-	Ohm
AOUT Load Capacitance	CLAO	-	20	1000	pF
AOUT Offset Voltage	VOSAO	-	-	100	mV
Full scale output voltage[3]	V_{oFULL}	-	2.0	2.5	Vpp

1. Tested at input gain of 0dB, Fin = 1KHZ.
2. Tested at input gain of 0dB, Fs=8KHz and 16KHz.
3. Tested at output gain of 0dB, Fout=1KHz.

8. PCB Layout Considerations

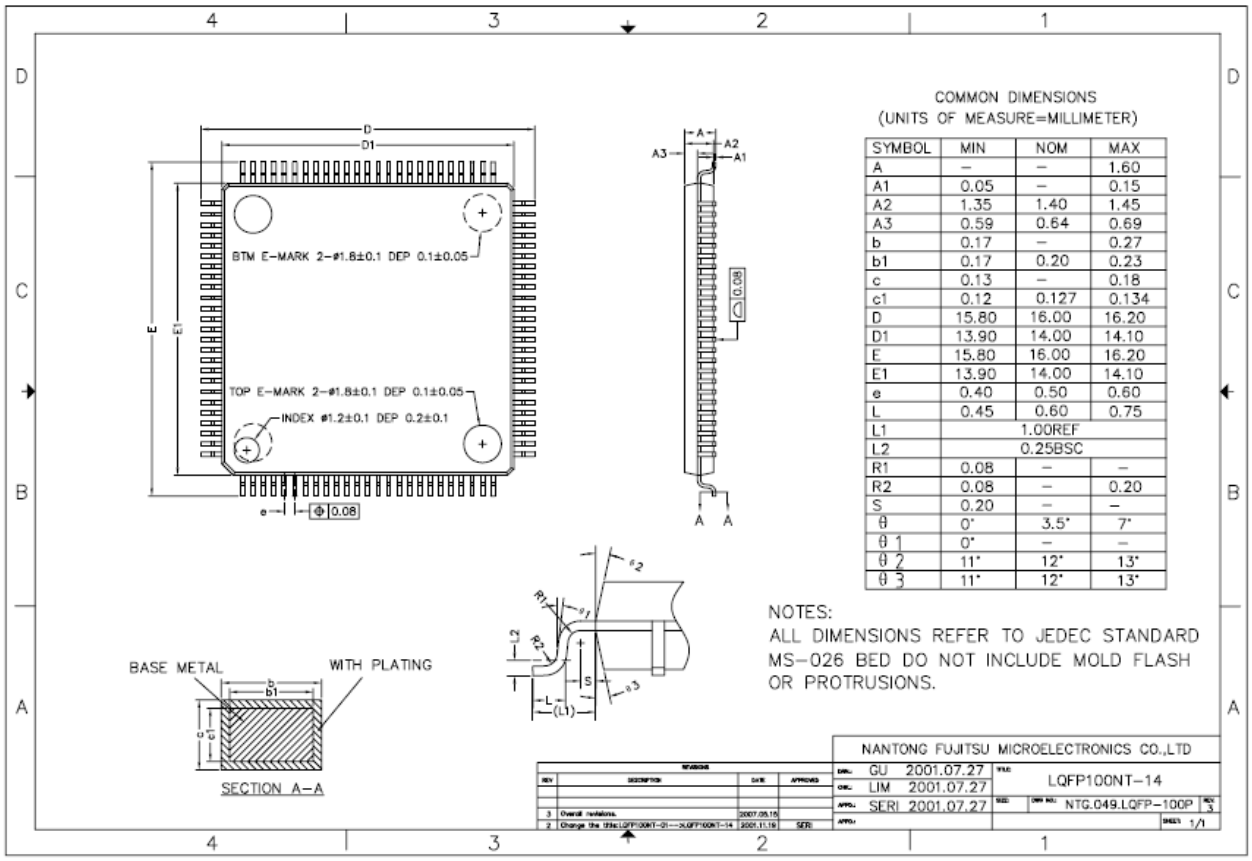
The PCB layout should be done to minimize the power and ground noise on the EC5128. This is done by good power de-coupling with minimum lead length on the de-coupling capacitors ; well-filtered and regulated analog power input shielding and ground plane isolation.

The ground plane should cover most of the PCB area with separated digital and analog ground planes. These two planes should be at the same electrical potential and connected together under the EC5128. The input capacitor and termination registers are placed close to the input pins. The following figure shows a ground plane layout example.



To minimize crosstalk, the digital signals of EC5128 should be separated from the analog circuitry. Moreover, the digital signals should not cross over the analog power and ground plane. Parallel running of digital lines for long distance should also be avoided.

9. Package Dimension



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	0.40	0.50	0.60
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ 1	0°	–	–
θ 2	11°	12°	13°
θ 3	11°	12°	13°