[DATA SHEET OF MV9205]

NON REAL TIME 16 CHANNEL PCI VIDEO & AUDIO DECODER

MV9205

4 CHANNEL VIDEO
8 CHANNEL AUDIO DECODER WITH PCI

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General Information

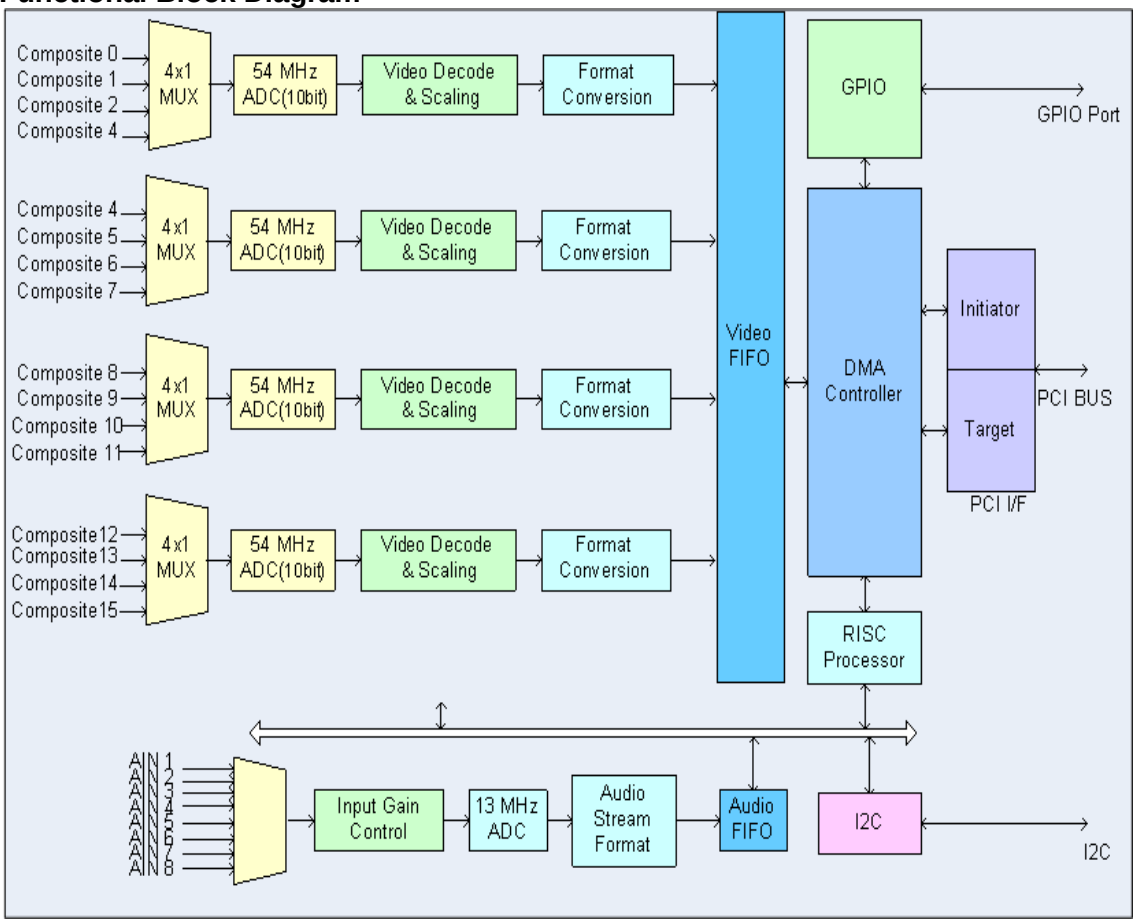
PCI Video Decoder

The MV9205 provides the capability to display up to four analog video signals simultaneously on a single screen. It also allows ability to capture four(4) video and eight(8) audio input signals moving data a real time using a PCI bus. Also the MV9205 includes 16CH NRT Video decoder. It accepts select 4CH(RT) or 16CH(NRT) inputs from Camera. It digitizes and NTSC/PAL video signal, transfers the converted data to pc via pci bus. MV9205 also transfers PCM digital voice signals converted from analog voice input signals.

MV9205 is a multifunctional high-performance chip, which is designed to fit in DVR system. MV9205 is a multimedia device component that can be easily designed on board level along with other devices when designing DVR system. MV9205 is compliant with PCI2.2 standard which is widely used for personal computers and industrial products.

Therefore, MV9205 is ideally designed and suitable for high-performance DVR system that can record and display analog multi-channel.

Functional Block Diagram



General Features

• Supports NTSC/PAL video decoding
• Supports image capture resolutions up to 768 x 576 (PAL), 720 x 480 (NTSC)
• On-chip PCI bus mastering and bridge functionality
• Accepts real time 4 channel video input and non_real time 16 channel video input. .
• Accepts 8 channel audio input
• Flexible 24-bit wide GPIO
• Supports 2-wire serial bus master (I2C) via PCI bus
• Programmable multi video input select. (4 to 1)
• NTSC and PAL with automatic format detection
• Horizontal and vertical free scaling
• Fully Programmable static gain or automatic gain control (AGC) for the video signal
• Multiple YCrCb and YUV420 planar formats supported on output
• Performs complex clipping of video source and VGA video overlay
• Permits different program control and color space/scaling for even and odd fields
• 100% PCI Rev. 2.2 compliant
• Packaged in compact 176-pin plastic LQFP

Applications

• PC based video capture
• DVR System (Digital Video Recorder)

Ordering Information

Model Number	Package	Operating Temperature
MV9205	176 pin LQFP	-25°C to + 125 °C

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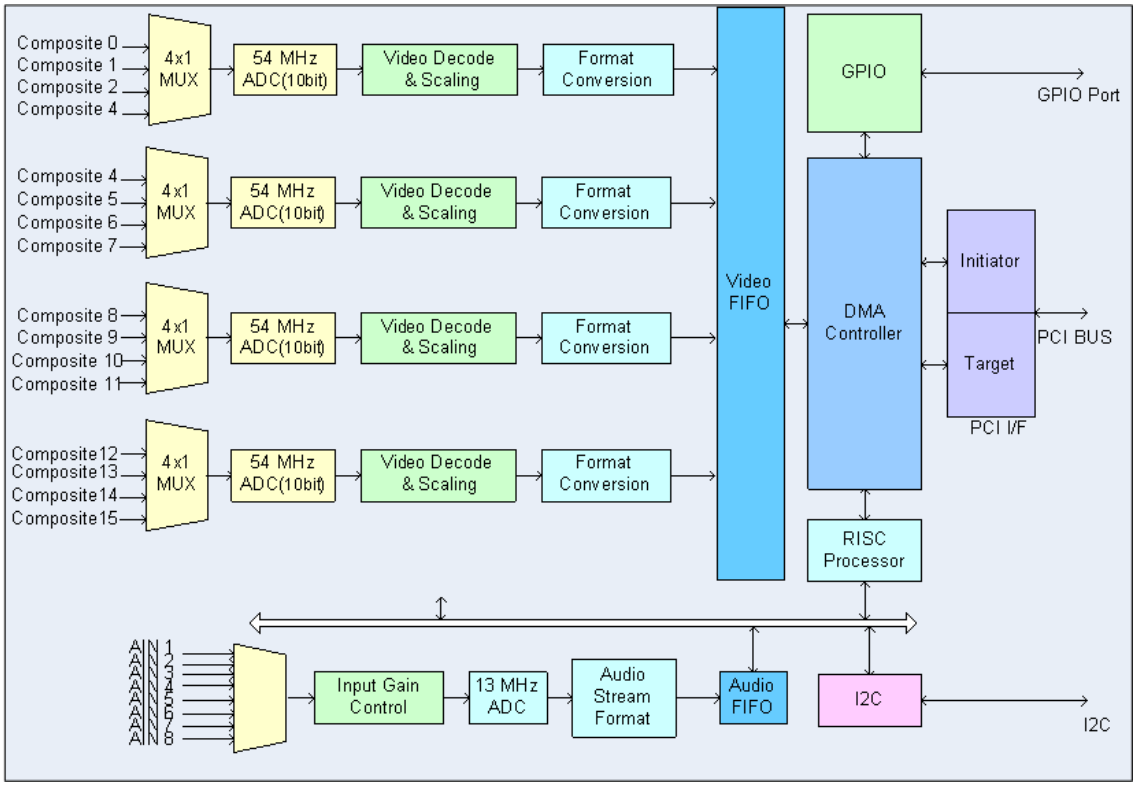
1.0 Product Overview

1.1 Functional Overview

MV9205 is a single chip operating at 3.3 V and 1.8V, that features the capability to capture (RT) 4channel ,(NRT)16channel video input signals and 8-channel audio input signals using a PCI bus.
It uses DMA for video data and audio data processing.
MV9205 differs from other existing decoder chips in the way that it processes all analog input signals into digital mode.
Additionally, it delivers higher quality screen and easy data processing due to the use of digital filters.
Video decoder function of MV9205 allows storage for real time moving picture transmission in every single channel depending on program registers. It accepts separate 4CH(RT) or 16CH(NRT) input from camera. Also 4-channel video and 8-channel audio can be captured simultaneously or displayed on a screen.
Please refer the MV9205 Block Diagram as shown in Figure 1-1.

Figure 1-1. Block Diagram of the MV9205.



1.2 Detailed Features

1.2.1 Video Capture

MV9205 is constructed with four video decoders, scaler, format conversion, DMA controller, and PCI interfaces. It also provides the capability to capture 4 types of video input data with ability to directly save them in host memory. These captured video data can be overlayed onto a video card.

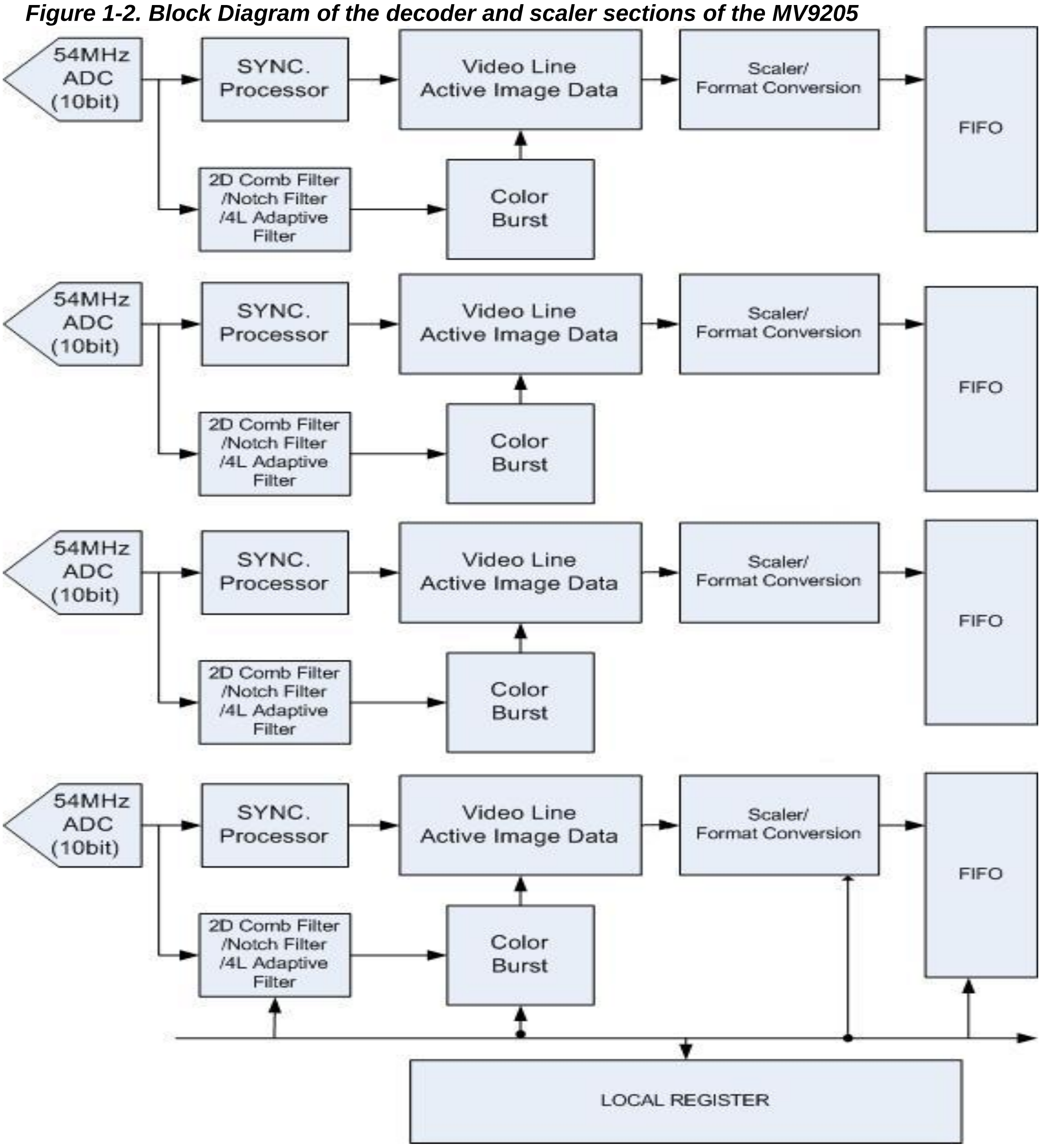
Video signal of each channel can operate all functions of video decoder such as video format conversion, scaler etc.

Video pixel data can be stored via FIFO, and transmitted to a PCI bus in data stream type.

With MV9205, you can process 4-channel video data simultaneously or choose a single channel to operate it.

Please refer to Figure 1-2.

Figure 1-2. Block Diagram of the decoder and scaler sections of the MV9205



1.2.2 Audio Capture

MV9205 supports 8 audio input signals. A DMA channel processes two audio signals of 8 audio channels. Each DMA channels can be chosen according to register of DMA controller. It allows to capture a single video and two audio channels. Audio data also transmitted to a PCI bus in stream form.

1.2.3 Video DMA Channels

When transmitting EVEN and ODD fields to the host memory, MV900 separates them according to commands from the controller. The commands sent from the controller are created by a MV9205 device driver. They serve to set target addresses and the corresponding video pixel data are transmitted to the target addresses via each DMA.

1.2.4 Audio DMA Channels

Audio channels 10-bit data samples are transmitted to one that is chosen from the four formats (16Bit Stereo, 16Bit Mono, 8Bit Stereo, 8Bit Mono). They have a total of 8 channels and selection of each channel is available via controller's commands. Data collected from sampling are transmitted by appointing target addresses, the same method to use video DMA.

1.2.5 PCI Bus Interface

MV9205 is efficiently designed by using a PCI bus with 33MHz or 66MHz clock. The 32-bit DWORD transmits image data via DMA to a PCI bus.

1.2.6 GPIO Port

MV9205 has a 24-bit GPIO, GPIO's normal mode port operates in a way so each bit can performs in/out control individually.

1.2.7 I2C Interface

MV9205 supports I2C operation. MV9205 controls other devices such as video cards or TV tuners using an I2C interface. MV9205 reads or records other devices' data via an I2C interface.

1.3 Pin Descriptions

Figure 1-3 shows pin arrangements on MV9205.

Figure 1-3. pin out diagram of MV9205

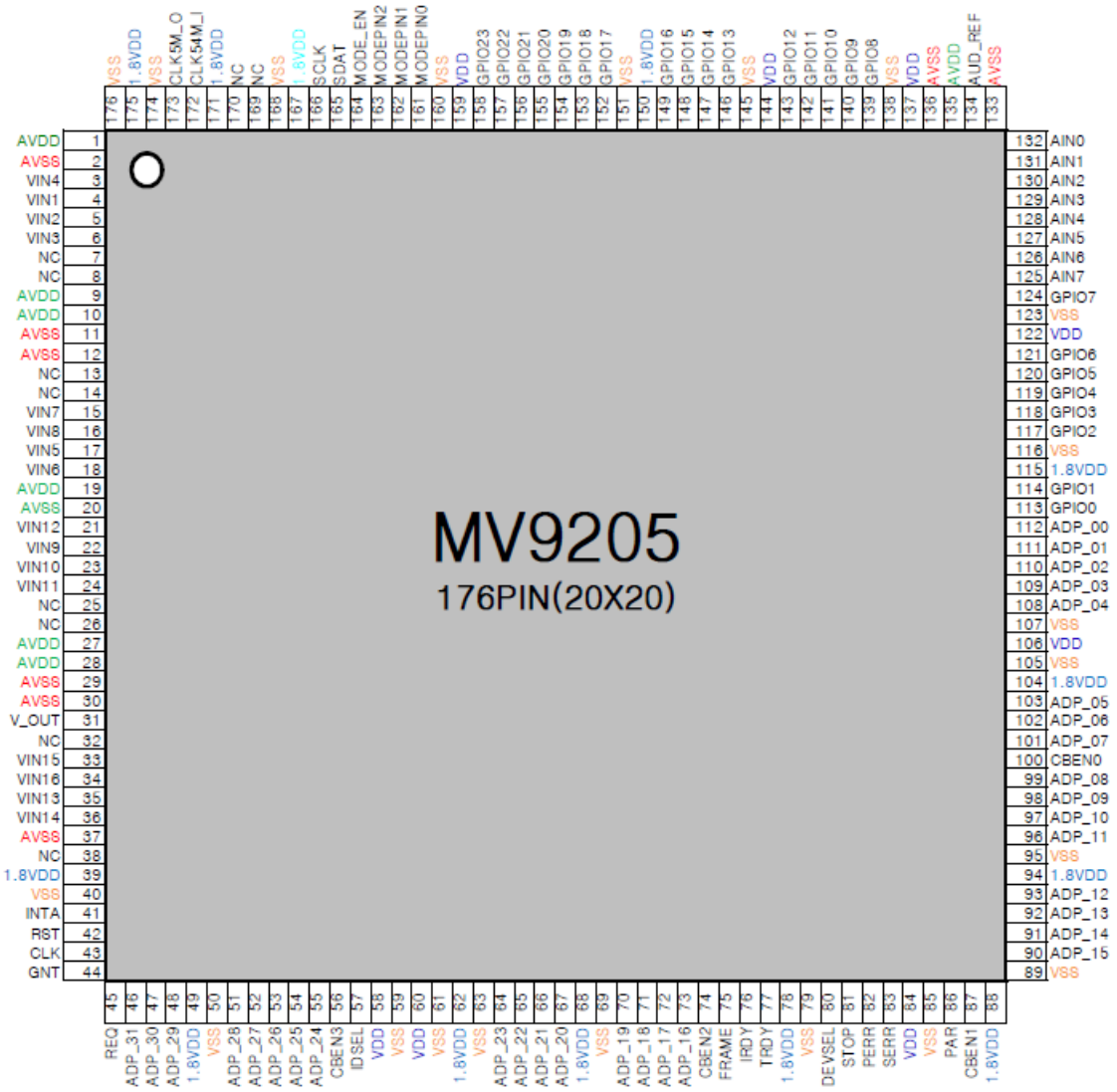


Figure 1-1 shows MV9205 pin numbers with their descriptions.

Table 1-1. provides a description of pin functions grouped by common function.

Pin#	Pin Name	I/O	Signal	Description
PCI Interface (50 pins)				
43	CLK	INPUT	Clock	The MV9205 supports a PCI clock up to 33.3333MHz
42	RST_N	INPUT	Reset	This input three-states all PCI signals asynchronous to the CLK signal.
45	REQ_N	OUTPUT	Request	Agent desires bus
44	GNT_N	INPUT	Grant	Agent granted bus
57	IDSEL	INPUT	Initialization Device Select	This input is used to select the MV9205 during configuration read and write transactions.
46	AD31	IN/OUT	Address/Data	These three-state, bidirectional I/O pins transfer both address and data information.
47	AD30			
48	AD29			
51	AD28			
52	AD27			
53	AD26			
54	AD25			
55	AD24			
64	AD23			
65	AD22			
66	AD21			
67	AD20			
70	AD19			
71	AD18			
72	AD17			
73	AD16			
90	AD15			
91	AD14			
92	AD13			
93	AD12			
96	AD11			
97	AD10			
98	AD9			
99	AD8			
101	AD7			
102	AD6			
103	AD5			
108	AD4			
109	AD3			
110	AD2			
111	AD1			
112	AD0			

Pin#	Pin Name	I/O	Signal	Description
56	CBE_N3	IN/OUT	Bus Command / Byte Enable	These three-state, bidirectional I/O pins transfer both bus command and byte enable information.
74	CBE_N2			
87	CBE_N1			
100	CBE_N0			
86	PAR	IN/OUT	Parity	These three-state bidirectional I/O pin provides even parity across AD[31:0] and CBE_N[3:0].
75	FRAME_N	IN/OUT	Cycle/Frame	This sustained, three-state signal is driven by the current master to indicate the beginning and duration of an access. FRAME_N is asserted to signal, the beginning of a bus transaction.
76	IRDY_N	IN/OUT	Initiator Ready	This sustained three-state signal indicates the bus master's readiness to complete the current data phase. IRDY_N is used in conjunction with TRDY_N.
80	DEVSEL_N	IN/OUT	Device Select	This sustained, three-state signal indicates device selection. When actively driven, DEVSEL_N indicates the driving device has decoded its address as the target of the current access.
77	TRDY_N	IN/OUT	Target Ready	This sustained, three-state signal indicates the target's readiness to complete the current data phase.
81	STOP_N	IN/OUT	Stop	This sustained three-state signal indicates that the target is requesting the master to stop the current transaction.
82	PERR_N	IN/OUT	Parity Error	Report data parity error
83	SERR_N	OUTPUT	System Error	Report address parity error. Open drain.
41	INTA_N	OUTPUT	Interrupt A	This signal is an open drain interrupt output.
I2C Interface(2 pins)				
166	SCL	IN/OUT	Serial Clock	Bus clock, output open drain.
165	SDA	IN/OUT	Serial Data	Bit Data or Acknowledge, output open drain.

Pin#	Pin Name	I/O	Signal	Description
General Purpose I/O(24 pins)				
158	GPIO23	IN/OUT	General Purpose I/O	MV9205 pin decoding in normal mode. Pins pulled up to VDD. For additional information.
157	GPIO22			
156	GPIO21			
155	GPIO20			
154	GPIO19			
153	GPIO18			
152	GPIO17			
149	GPIO16			
148	GPIO15			
147	GPIO14			
146	GPIO13			
143	GPIO12			
142	GPIO11			
141	GPIO10			
140	GPIO9			
139	GPIO8			
124	GPIO7			
121	GPIO6			
120	GPIO5			
119	GPIO4			
118	GPIO3			
117	GPIO2			
114	GPIO1			
113	GPIO0			
Reference Timing Interface Signals(2 pins)				
172	XTI	INPUT		A 54.000MHz crystal can be tied directly to these pins, or a single-ended oscillator can be connected to XTI
173	XTO	OUTPUT		
Video Input Signals(17 pins)				
3	VIN1	ANALOG IN	Video input	Analog composite video inputs to the on-chip. 4 Channel and 16 Channel analog video input.
4	VIN2			
5	VIN3			
6	VIN4			
15	VIN5			
16	VIN6			
17	VIN7			
18	VIN8			
21	VIN9			
22	VIN10			
23	VIN11			
24	VIN12			

33	VIN13			
34	VIN14			
35	VIN15			
36	VIN16			
31	V_OUT	OUTPUT	Video output of Reference Signal.	reference for video channel. Must connect 0.1uF capacitors to GNDA
Audio Input Signals(9 pins)				
132	AIN0	ANALOG IN	Audio Input	analog audio inputs to the on-chip. The ADC has multiplexed 8 input channels.
131	AIN1			
130	AIN2			
129	AIN3			
128	AIN4			
127	AIN5			
126	AIN6			
125	AIN7			
134	AUD_Ref	OUTPUT	Audio reference output.	reference for audio channel. Must connect 0.1uF capacitors to GNDA
3.3V I/O and Core Power and Ground(16pins)				
58,60,84 106,122, 137,144, 159	VDD	POWER		Digital outputs power supply.
59,61,85 107,123, 138,145, 160	GND	GROUND		Digital outputs ground.
Analog Video & Audio Power and Ground(16 pins)				
1,9,10, 19,27,28 ,135	AVDD	POWER	Video ADC Audio ADC	Analog outputs power supply.
2,11,12, 20,29,30 ,37,133, 136	AGND	GROUND	Video ADC Audio ADC	Analog outputs ground.
1.8V Analog and Core Power and Ground (26 pins)				
39,49,62 ,68,78, 88,94, 104,115, 150,167, 171,175	1.8VDD	POWER	ADC and Logic Core	Analog and Core Outputs power supply.

40,50,63,69,79,89,95,105,116,151,168,174,176	1.8GND	GROUND	ADC and Logic Core	Analog and Core Outputs ground.
N.C(14 pins)				
161	N.C	INPUT	Signal	No Connection
162	N.C	INPUT		No Connection
163	N.C	INPUT		No Connection
164	N.C	INPUT		No Connection
169,170,7,8,13,14,25,26,32,38	N.C	INPUT		No Connection

2.0 Functional Description

2.1 Composite Video Input Formats

MV9205 supports various kinds of composite video input signals. Table 2-1 shows different types of videos and standards for different countries. MV9205 is compliant with corresponding video types as it has an ability to adjust programs using the register. MV9205 also has an auto detector in each video which also uses the register.

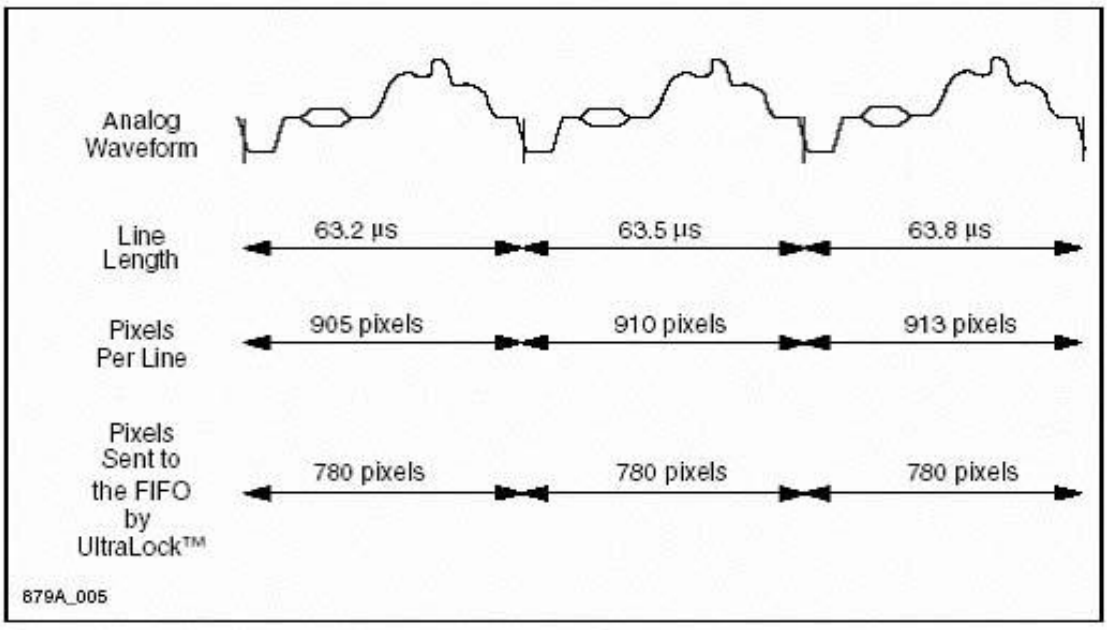
Table 2-1. Video Input Formats Supported by the MV9205

Format	Line	Fields	Fsc	Country
NTSC-M	525	60	3.58MHz	U.S., many others
NTSC-Japan	525	60	3.58MHz	Japan
PAL-B,G,H	625	50	4.43MHz	Western/Central Europe, others
PAL-D	625	50	4.43MHz	China
PAL-I	625	50	4.43MHz	U.K., Ireland, South Africa
PAL-M	525	60	3.58MHz	Brazil
PAL-Nc	625	50	3.58MHz	Argentina
PAL-N	625	50	3.58MHz	Paraguay, Uruguay
SECAM	625	50	4.406MHz 4.250MHz	Eastern Europe, France, Middle East

NOTE(S): (1) NTSC—Japan has 0 IRE setup.

Figure 2-1 shows the length and construction of an analog video line.

Figure 2-1. Video Line for NTSC Square Pixel Output

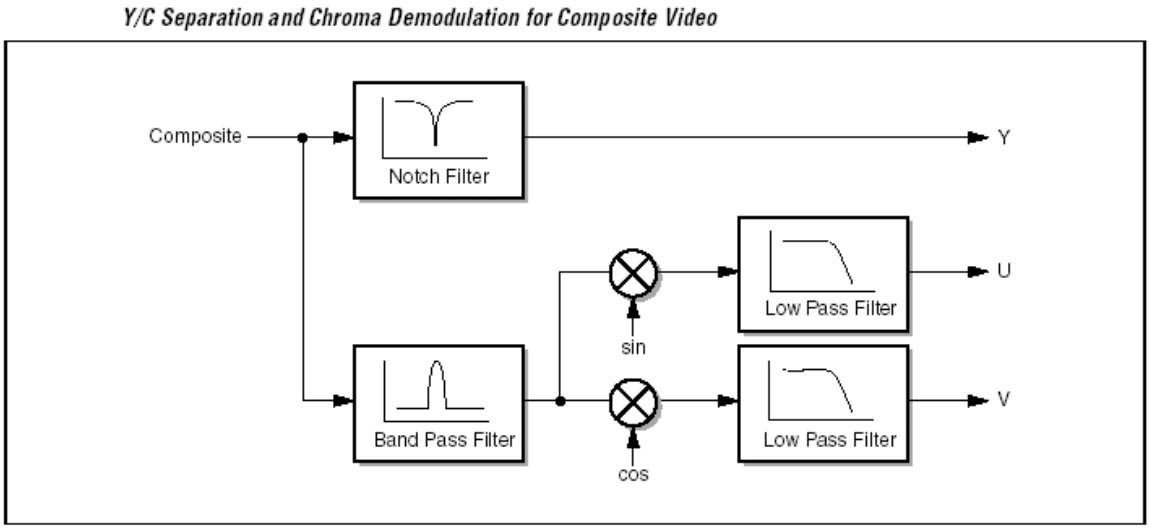


2.2 Y/C Separation and Chroma Demodulation

MV9205 can separate Y.I.Q by using a notch filter, band pass filter, and a flat filter in order to separate a Y/C from video sources being inputted. Figure 2-2 is a diagram of separation in Y/C filter showing a notch filter and band pass filter separating Y/C from the video sources.

Figure 2-2 shows the Y/C separation and chroma demodulation.

Figure 2-2. Y/C Separation and Chroma Demodulation for Composite Video



2.3 Video Adjustments

MV9205 can control brightness, contrast, hue, and saturation using program registers.
Hue adjust register, Contrast adjust register, Saturation adjust register, Brightness register
The Screen Control Register can be adjusted by a program to allow an easier control of screens.

Adjustable brightness range	0 – 255
Adjustable saturation range	0 – 255
Adjustable contrast range	0 – 255
Adjustable hue range	0 – 255

2.4 Video Data Format Conversion

2.4.1 Pixel Data Path

Format Conversion offer to YUV4:2:2.
YUV4:2:0 is created through Color Space Conversion.
Refer to Figure 2-7 for video data format conversion.

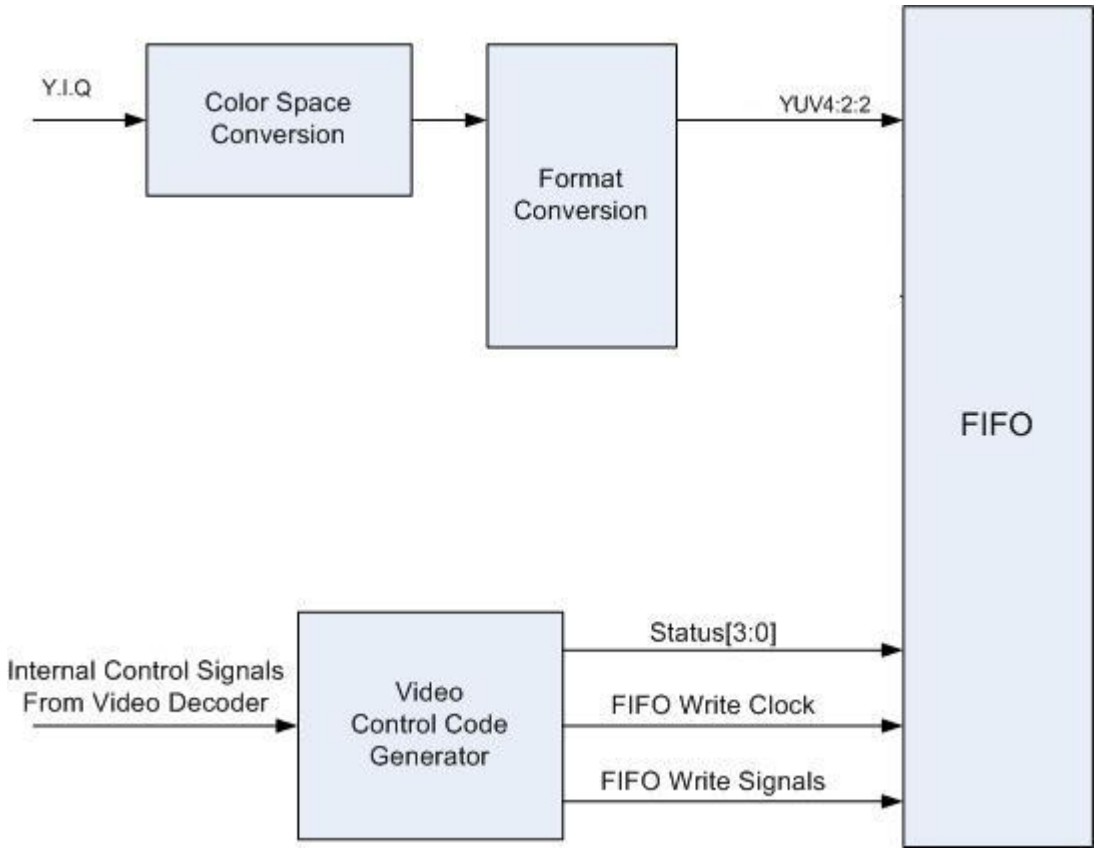


Figure 2-7. Video Data Format Converter

2.4.2 Video Control Code Status Data

MV9205 has 4 video decoders, each of which can choose its Video Mode using a corresponding 3bit csrColorFormat register.

Bit	Video Mode
000	YUV2-YCrCb 4:2:2
001	YUV4:1:1
010	Y8
011	YUV4:2:0

Table 2-2. Video Data Format

Format	DWORD	Pixel Data [31:0]			
		Byte Line 3 [31:24]	Byte Line 2 [23:16]	Byte Line 1 [15:8]	Byte Line 0 [7:0]
YUY2-YCrCb 4:2:2	dw0	Cr0	Y1	Cb0	Y0
	dw1	Cr2	Y3	Cb2	Y2
YUV4:1:1	dw0	Y1	Cr0	Y0	Cb0
	dw1	Y3	Cr4	Y2	Cb4
	dw2	Y7	Y6	Y5	Y4
Y8	dw0	Y3	Y2	Y1	Y0
YUV4:2:0	dw0 FIFO1	Y3	Y2	Y1	Y0
	dw1FIFO1	Y7	Y6	Y5	Y4
	dw0FIFO2	Cb6	Cb4	Cb2	Cb0
	dw0FIFO3	Cr6	Cr4	Cr2	Cr0

2.5 Video and Control Data FIFO

The FIFO block receives format-converted audio/video data and VBI data to transmit them to a PCI bus. It also outputs DWORD data to the DMA Controller.

2.5.1 FIFO Data Interface

Data stored on FIFO include all video data, audio data and also includes 4-bit Status as DMA control codes.

Table 2-3 shows the Status bit configuration.

Table 2-3 Status Bit

Status[3:0]	Code	Description
0110	FM1	FIFO Mode : packed data to follow
0010	SOL	First active pixel/data DWORD of scan line
0001	EOL	Last active pixel/data DWORD of scan line, 4 Valid Bytes
0100	VRE	VRESET following an even field-falling edge of FIELD
1100	VRO	VRESET following an odd field-falling edge of FIELD
0000	PXV	Valid pixel/data DWORD

2.6 DMA Controller

MV9205 uses the DMA controller to transmit data saved in FIFO to a PCI bus. All the data which are delivered to DMA controller includes all video data and audio data.
All data are transmitted to a PCI bus via the DMA controller while moving according to RISC Processor's commands.

2.6.1 RISC Instructions

RISC commands are comprised of 4 functions: WRITE, SYNC, JUMP, and REG_WRITE. For detailed descriptions, see Table 2-4 below.

Table 2-4. RISC Instructions

Instruction	Opcode	DWORDs	Description		
WRITE	0001	2	Write packed mode pixels to memory from the FIFO beginning at the specified target address.		
			DWORD0 :		
			[13:0]	Byte Count	
			[23:14]	Repeat count	
			[24]	IRQ	
			[25]	Clera command	
			[26]	EOL	
			[27]	SOL	
			[31:28]	Opcode	
			DWORD1 :		
			[31:0]	32bit Target Address	**Byte address of first pixel byte**
Instruction	Opcode	DWORDs	Description		
SYNC	1000	2	Synchronize all data in FIFO until the RISC instruction status bits equal the FIFO status bits.		
			DWORD0 :		
			[3:0]	Status	
			[15:23]	Reserved	
			[24]	IRQ	
			[27:26]	Reserved	
			[25]	Clear command	
			[31:28]	Opcode	
			DWORD1 :		
			[31:0]	Reserved	
Instruction	Opcode	DWORDs	Description		
JUMP	0111	2	Jump the RISC program counter to the jump address. This allows unconditional branching of the sequencer program.		
			DWORD0 :		
			[23:0]	Reserved	
			[24]	IRQ	
			[27:26]	Reserved	
			[25]	Clear command	
			[31:28]	Opcode	
			DWORD1 :		
			[31:0]	Jump Address	DWORD Aligned
Instruction	Opcode	DWORDs	Description		
Reg_WRITE	0100	2	Reg_Write mode is writer to the local register		
			DWORD0 :		
			[11:0]	Register address	
			[23:12]	Reserved	
			[24]	IRQ	
			[25]	Clear command	

			[26]	EOL	
			[27]	SOL	
			[31:28]	Opcode	
			DWORD1 :		
			[31:0]	32bit Target Address	**Data value of Register**

Each RISC command consists of 2 DWORD. The 32-bit DWORD command transmits various types of information including opcode, target address, status codes, synchronization code, byte count/enables and start/end of line code.

2.7 Audio A/D

2.7.1 Audio A/D Conversion

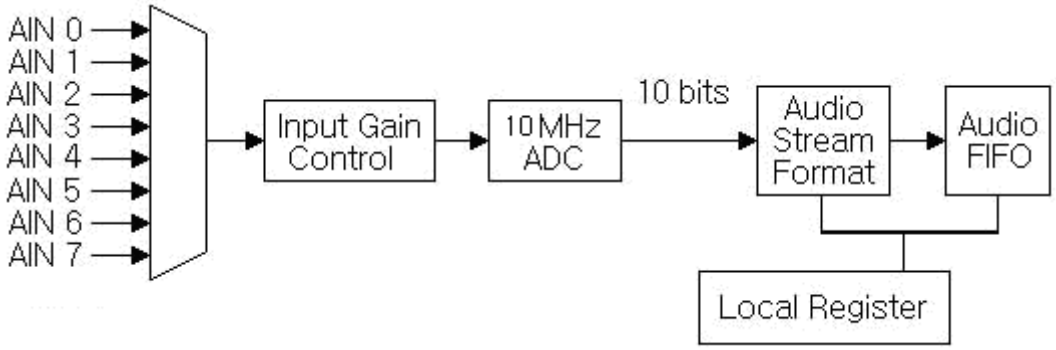
MV9205 has 8 audio channels input. It supports two audio channels for one video channel. Table 2-5 shows audio channels that are assigned to each video channel.

Table 2-5. Audio Channel for each Video Channel

Pin Number	Video Channel	Pin Number	Audio Channel
4	VAIN0 : Ch. 0	132	AIN0
		131	AIN5
17	VAIN1 : Ch. 1	130	AIN1
		129	AIN6
22	VAIN2 : Ch. 2	128	AIN2
		127	AIN7
35	VAIN3 : Ch. 3	126	AIN3
		125	AIN8

Each audio channel controls the sampling speed by csrAud_ADC_ClkScale Register. Audio signals sampled by 10-bit data are saved in FIFO after they are set to audio stream formats. Figure 2-8 shows how audio signals are processed.

Figure 2-8. Block Diagram of the Audio A/D flow



2.7.2 Audio Packets and Data Capture

Audio samples are divided into ALP_LEN(audio line packet of length) bytes by csrAudActive Register. And their audio line packets are split into AFP_LEN(audio field packet of length) by csrAudLine Register. Therefore, the number of data bytes within audio fields is ALP_LEN x AFP_LEN. The following shows FIFO Status and Data flow.

[FIFO Status]	[FIFO Data]
Begin Audio Field	
FM1	Don't Care
Begin Audio Line	// repeat (AFP_LEN)
SOL	audio DWORD
PXV	audio DWORD // repeat(AFP_LEN)
EOL(1-4)	audio DWORD or sub-DWORD
End Audio Line	
VRO	Don't Care
End Audio Field	

3.0 Electrical Interfaces

3.1 Input Interface

3.1.1 Analog Signal Selection

MV9205 supports 4 video channels and 8 audio signals input. Two audio signals are assigned to a single video channel. AGC(Automatic Gain Control) circuits compensate the amplitudes that are not up to MV9205 analog input signal standards. Figure 3-1 illustrates MV9205 outer circuits.

3.1.2 Crystal Inputs and Clock Generation

The inner PLL allows MV9205 to be compliant with NTSC and PAL video types. Clock interfaces are configured by connecting two I/O pins (XTI & XTO) to 54 MHz crystal.

For an oscillator, they are connected to XTI pins.

Figure 3-2. Clock Options

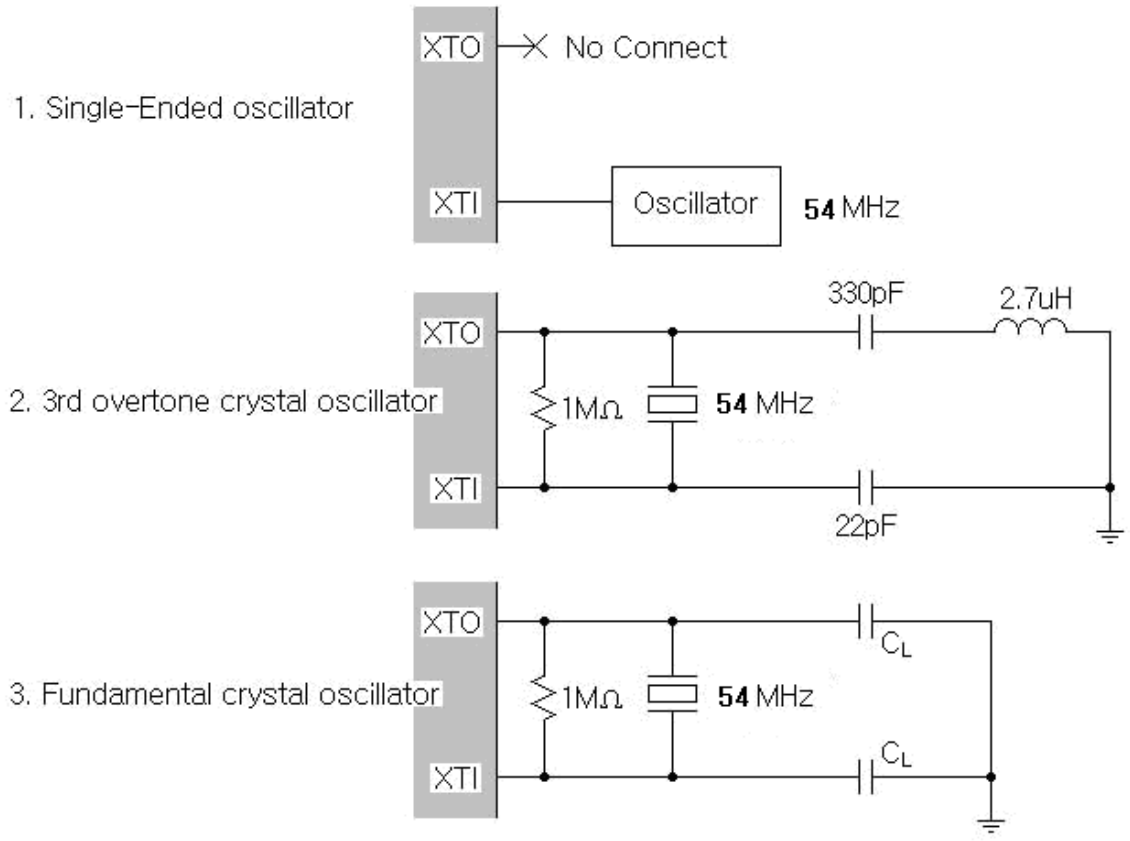
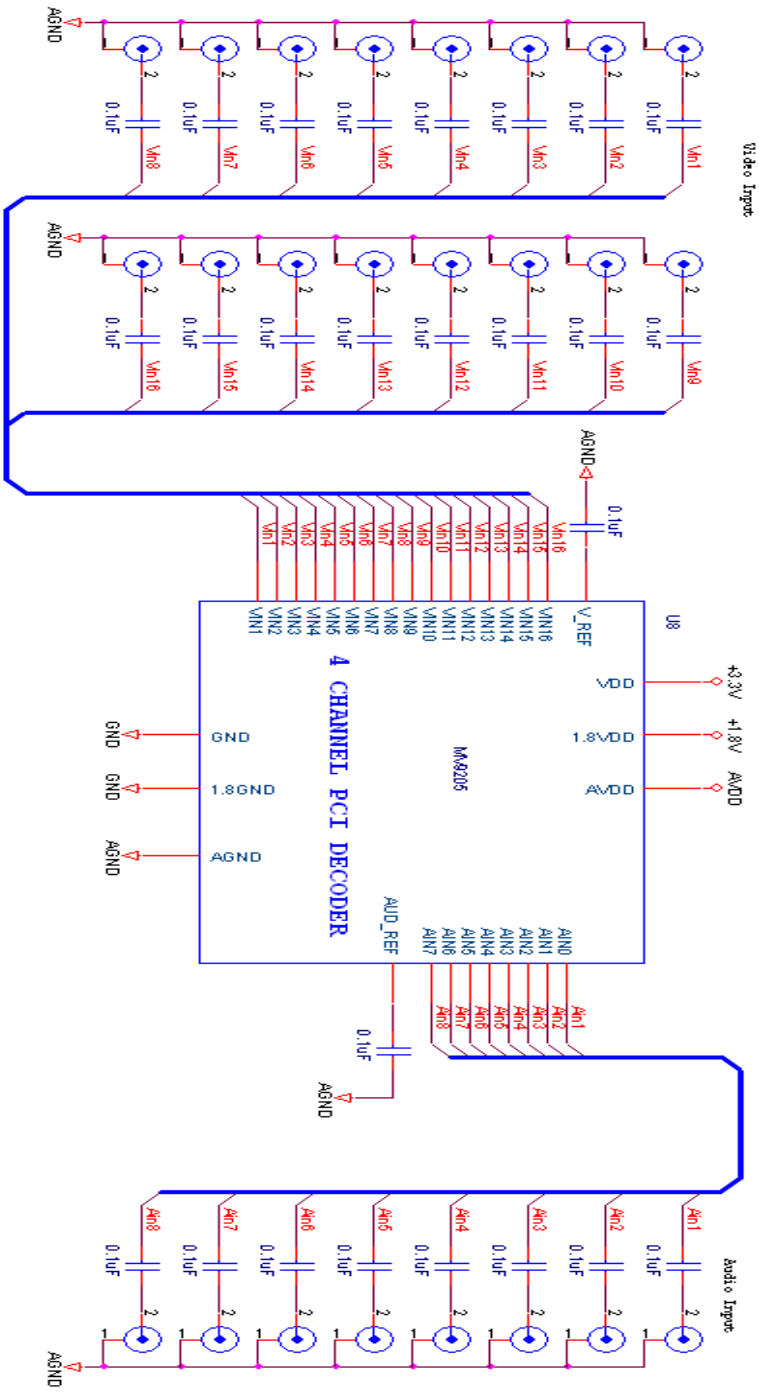


Figure 3-1. Typical External Circuitry



3.2 PCI Bus Interface

MV9205 uses a PCI local bus interface as a host CPU interface, and it is compliant with PCI Rev. 2.2.

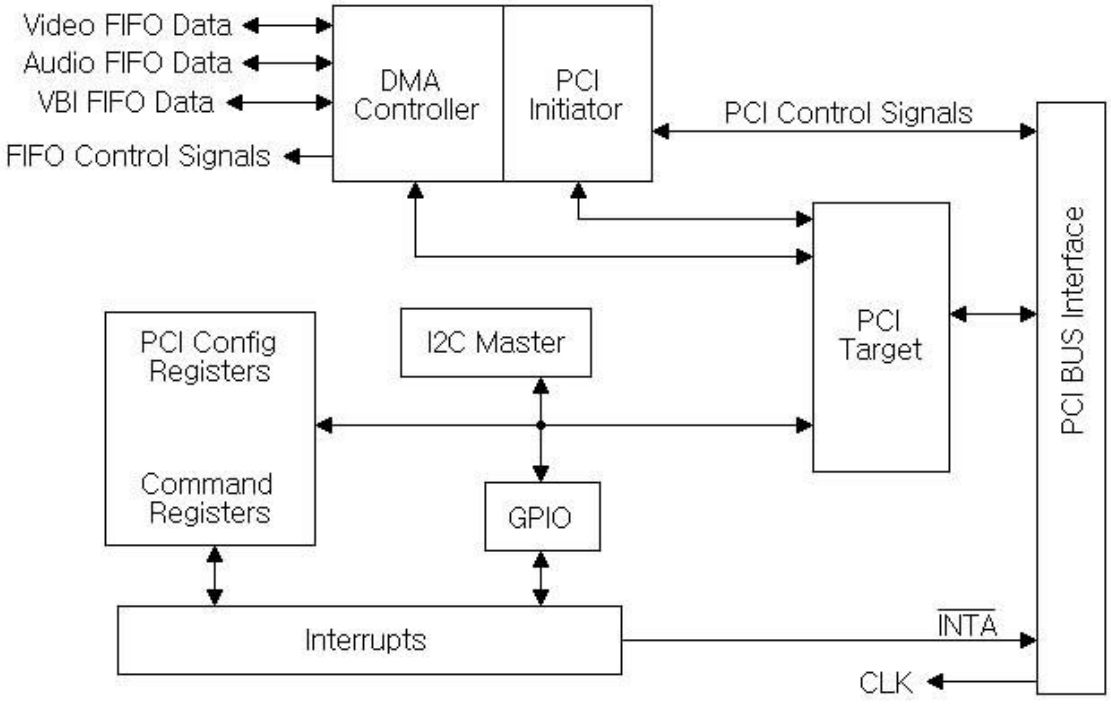
The PCI bus instruction cycle for a PCI Initiator and target is as follows;
- Memory read
- Memory write

The PCI bus instruction cycle only for a PCI target is as follows;
- Configuration read
- Configuration write
- Memory read multiple
- Memory read multiple
- Memory read line
- Memory write and invalidate

"Memory write and invalidate" is processed in a similar way to "Memory write". "Memory read multiple" and "Memory read line" are processed in a similar way to "Memory read".

The following PCI features are not supported.
- 64-bit bus extension
- I/O transactions
- Special, interrupt acknowledge, dual address cycles
- Locked transactions
- Caching protocol
- Initiator fast back-to-back transactions to different targets

Figure 3-4. PCI Data Block Diagram

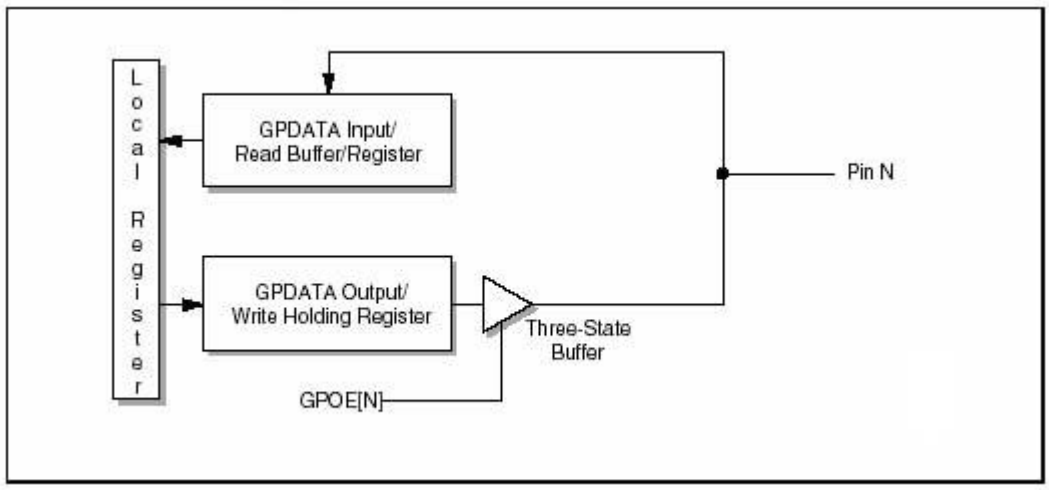


3.3 General Purpose I/O Port

3.3.1 GPIO Pin Architecture

Each GPIO pin is set by a default I/O buffer, together with a separate GPOE register that controls output.

Figure 3-5. GPIO Pin architecture



3.3.2 GPIO Normal Mode

The normal mode of a GPIO port allows the controlling of each bit unit from a 24-bit GPIO port. It also allows for GPIO BIT I/Os via a PCI interface. GPDATA can write or read via DATA signals on GPOE register. When signals are outputted via GPOE, information is recorded onto the registers within GPDATA, and it is outputted via pins. While signals are inputted via GPOE, buffer data are read directly from pins as shown in Figure 3- 5. Each GPIO pin is inputted or outputted according to GPOE registers. Each bit of GPOE register corresponds to each bit of the GPIO pins. If the value of the GPOE register is 1, use of output buffer is available and that pin is outputted. If the value of the GPOE register is 0, the output buffer cannot be used, and the corresponding pin becomes an input pin. In order to prevent this error from occurring, set the GPOE register to “INPUT(0xFFFFFFFF)” when turning on the power.

3.4 I2C Interface

The I2C bus is a 2-line serial interface, transmitting data between Master and Slave devices using a serial clock line(SCL) and a serial data line(SDA).

Refer to the following diagram.

Figure 3-9. Write mode in Serial Interface

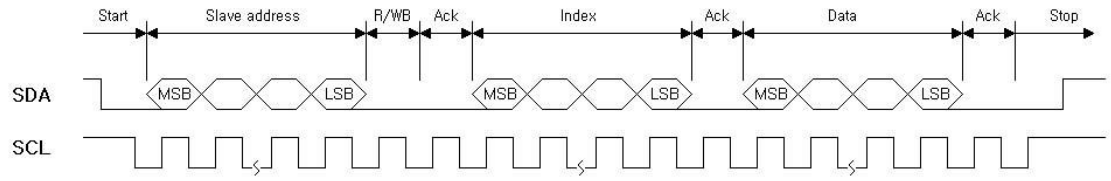
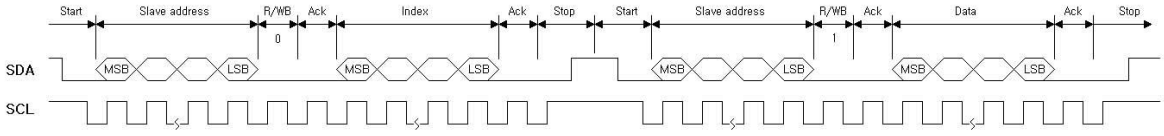


Figure 3-10. Read mode in Serial Interface



3.5 I2C Serial EEPROM Interface

The outer EEPROM must be connected into a I2C bus(SCL, SDA). This interface supports the 24C02(A) 2kbit Serial EEPROM. The address of 7-bit slave device is 1010000, and the EEPROM can be read at any time when the I2C operates in hardware or software mode.

The following sequence is found when an I2C reads information.

1. START
2. 0xA0
3. 8-bit byte address
4. START
5. 0xA1
6. 8-bit read data, followed by (master NACK &) STOP

3.5.1 EEPROM Address Mapping

MV9205 supports a single EEPROM(up to 256B). Table 3-3 below shows the memory structure of an external EEPROM.

Table 3-3. External EEPROM Memory Map

Logical Address	Physical Address	24C02
251	0x00	Read/Write
…	…	
124	0x7F	
123	0x80	Read - Only
…	…	
-4	0xff	

3.5.2 Subsystem Vendor ID

PCI Configuration Header Location 0x2C specifies the Subsystem Vendor ID and the Subsystem ID. If an external EEPROM is present, the subsystem vendor ID and subsystem ID and vital product data are uploaded. If an external EEPROM is not present, the 32 bits of the header register default to 0x0000, and the register can be programmed using BIOS.

-- EEPROM Upload at PCI Reset

The 32-bit subsystem ID is read from the EEPROM's physical address 0xFC after a PCI is reset. For detailed information, see Table 3-4.

Table 3-4. EEPROM Upload Sequence

Master		Slave		Master	Comment
Control	Data	Data	Control	Control	
START	0xA0	-	ACK	-	Write control byte with slave chip address
	0xFC	-	ACK	-	Data bytes base address
START	0xA1	-	ACK	-	Read control byte with slave chip address
-	-	0x	-	ACK	Subsystem ID[15:8] at 0xFC
-	-	0x	-	ACK	Subsystem ID[7:0] at 0xFD
-	-	0x	-	ACK	Subsystem Vendor ID[15:8] at 0xFE
-	-	0x	-	NACK,STOP	Subsystem Vendor ID[7:0] at 0xFF

4.0 Control Register Definitions

PCI Configuration Space Header

	31		16 15	0
0x00	Device ID		Vendor ID	
0x04	Status		Command	
0x08	Class Code			Revision ID
0x0C	Reserved	Header Type 0	Latency Timer	Reserved
0x10	Base Address Register			
0x14	Reserved			
0x18				
0x1C				
0x20				
0x24				
0x28	Reserved			
0x2C	Subsystem ID		Subsystem Vendor ID	
0x30	Reserved			
0x34	Reserved			Capabilities Pointer
0x38	Reserved			
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line

4.1 PCI Configuration Registers

4.1.1 Vendor and Device ID Register

PCI Configuration Header Location 0x00				
Bits	Type	Default	Name	Description
[31:16]	RO	9205	Device ID	Identifies the particular device or Part ID Code.
[15:0]	RO	316	Vendor ID	Identifies manufacturer of device, assigned by PCI SIG

4.1.2 Command and Status Register

The Command [15:0] register provides control over ability to generate and respond to PCI cycles.

When a 0 is written to this register, MV9205 is logically disconnected from the PCI bus except for configuration cycles. The unused bits in this register are set to a logical 0. The Status [31:16] register is used to record status information regarding PCI bus related events.

PCI Configuration Header Location 0x04				
Bits	Type	Default	Name	Description
[31]	RR	0	Detected Parity Error	Set when a parity error is detected, in the address or data, regardless of the Parity Error Response control bit.
[30]	RR	0	Signaled System Error	Set when /SERR is asserted.
[29]	RR	0	Received Master Abort	Set when master transaction is terminated with Master Abort.
[28]	RR	0	Received Target Abort	Set when master transaction is terminated with Target Abort.
[27]	RR	0	Signaled Target Abort	Set when target terminates transaction with Target Abort. This occurs when detecting an address parity error.
[26:25]	RO	01	Address Decode Time	Responds with medium /DEVSEL timing.
[24]	RR	0	Data Parity Reported	A value of 1 indicates that the bus master asserted /PERR during a read transaction or observed /PERR asserted by target when writing data to target. The parity Error Response bit in the command register must have been enabled.
[23]	RO	1	FB2B Capable	Target capable of fast back-to-back transactions.
[8]	RW	0	/SERR enable	A value of 1 enables the /SERR driver.
[6]	RW	0	Parity Error Response	A value of 1 enables parity error reporting.
[3]	RW	0	Special cycles	Controls a d4evice's action on Special Cycle operations.
[2]	RW	1	Bus Master	A value of 1 enables MV9205 to act as a bus initiator
[1]	RW	1	Memory Space	A value of 1 enables response to memory space accesses (target decode to memory mapped registers).
[0]	RW	1	I/O Space	Controls a device's response to I/O Space accesses.

4.1.3 Revision ID and class code Register

PCI Configuration Header Location 0x08				
Bits	Type	Default	Name	Description
[31:8]	RO	0x048000	Class Code	MV9205 is a multimedia video device.
[7:0]	RO	03	Revision ID	This register identifies the device revision.

4.1.4 Header Type Register

PCI Configuration Header Location 0x0C				
Bits	Type	Default	Name	Description
[23:16]	RO	0x00	Header type	Multi-function PCI device.

4.1.5 Latency Time Register

PCI Configuration Header Location 0x0C				
Bits	Type	Default	Name	Description
[15:8]	RW	0x64	Latency Timer	The number of PCI bus clocks for the latency timer used by the bus master. Once the latency expires, the master must initiate transaction termination as soon as /GNT is removed.

4.1.6 Bass Address Register

PCI Configuration Header Location 0x10				
Bits	Type	Default	Name	Description
[31:12]	RW	Assigned by CPU at boot-up	Relocatable memory pointer	Determine the location of the registers in the 32-bit addressable memory space.
[11:0]	RO	0x008	Memory usage specification	Reserve 4kB of memory-mapped address space for local registers. Address space is pre-fetchable without side effects.

4.1.7 Subsystem ID and Subsystem Vender ID Register

PCI Configuration Header Location 0x2C				
Bits	Type	Default	Name	Description
[31:16]	RW	FFFF	Subsystem ID	Vendor specific.
[15:0]	RW	FFFF	Subsystem Vendor ID	Identify the vendor of the add-on board or subsystem, assigned by PCI SIG.

4.1.8 Interrupt Line, Interrupt Pin, Min_Gnt, Max_Lat Register

PCI Configuration Header Location 0x3C				
Bits	Type	Default	Name	Description
[31:24]	RO	0xff	Max_Lat	Require bus access every 10µs, at a minimum, in units of 250 ns. Affects the desired settings for the latency timer value.
[23:16]	RO	0x04	Min_Gnt	Desire a minimum grant burst period of 4µs to empty data FIFO, in units of 250ns. Affects the desired settings for the latency timer value. Set for 128 DWORDs, with 0 wait states.
[15:8]	RO	0x01	Interrupt Pin	MV9205 interrupt pin is connecter to /INTA, the only one usable by a single function device.
[7:0]	RW	0X00	Interrupt Line	The Interrupt Line register communicates interrupt line routing information between the POST code and the device driver. The POST code initializes this register with a value specifying to which input (IRQ) of the system interrupt controller the MV9205 interrupt pin is connected. Device drivers can use this value to determine interrupt priority and vector information.

4.2 Local Registers

4.2.1 DMA Engine Register

Address	Bits	Type	Default	Name	Description
0050	[31:28]	R	Readonly	Reserved	Reserved
	[27:24]	R	Readonly	Reg_CH_Lock	Check to signal of the Video Which bit belongs in each ch (0=No Signal, 1=Detect Sign Bit 27: channel 3 Bit 26: channel 2 Bit 25: channel 1 Bit 24: channel 0
	[23:16]	R	Readonly	Dec_Field	Video decoder field 1 = Odd Field, 0 = even Field Bit 23: Decoder 7 Bit 22: Decoder 6 Bit 21: Decoder 5 Bit 20: Decoder 4 Bit 19: Decoder 3 Bit 18: Decoder 2 Bit 17: Decoder 1 Bit 16: Decoder 0
	[15:12]	R	0	Reserved	Reserved
	[11]	R/W	0	csrChSel_Mode	DMA Channel Select Mode (0= sequence, 1= biggest c
	[10:9]	R/W	2	csrFifoFullMode	FiFO mode 0=Stop Writting while has be 1=Stop Writting while has be 2=write EOL after Stop to un
	[8]	R	0		Reserved
	[7:1]	R/W	20	CsrDMABURST	Set data size transportable fr
	[0]	R/W	0	csrDMAPaused	DMA operation stops when s

DMA CHANNEL 0 -15

Address	Bits	Type	Default	Name	Description
0060 0074 0088 009C 00B0 00C4 00D8 00EC	[31:23]	R	1FF	Reserved	
	[22]	R/W	0	int_src_DMA	It interrupts when DMA operation is set to OP While occurring.
	[21]	R/W	0	int_src_OP	Error in OPCode
	[20]	R/W	0	int_src_ERR	Error during DMA operation
	[19:17]	R/W	0	ch_csr_INTmask	Bit2 : use interrupt in case of DMA Error Bit1 : use interrupt in case error occurs in OP Bit0 : use interrupt in case interrupt occurs a
	[16]	R	0	Reserved	
	[15:13]	R/W	0	ch_csr_pri	Priority given to DMA
	[12:11]	R	0	Reserved	
	[10]	R	0	ch_busy	DMA channel in use
	[9]	R	0	Ch_stop	Stop to DMA channel
	[8:1]	R	0	Reserved	
	[0]	R/W	0	ch_enable	If sets to 1, use DMA channel

Each channel Transmit data with DMA (0 –15)					
Address	Bits	Type	Default	Name	Description
0064 0078 008C 00A0 00B4 00C8 00DC 00F0	[31:14]	R	0	Reserved	
	[13:0]	R/W	0	Ch(0–15)_txsx	Remaining size after transmitting (transmit size : 32bit)

Opcode instruction in DMA (0 – 15)					
Address	Bits	Type	Default	Name	Description
0068 007C 0090 00A4 00B8 00CC 00E0 00F4	[31:28]	R/W	0	Opcode_CMD	DMA instruction in OPCode (1:Write, 4:Register write, 7:Jump, 8:Sync)
	[27]	R/W	0	Opcode_SOL	When it write “SOL” to be start.
	[26]	R/W	0	Opcode_EOL	“EOL” is the end
	[25]	R/W	0	Opcode_IRQ	When it set to register then occur “INT”
	[24]	R/W	0	Opcode_CLR	It clear saved “OPCode”
	[23:14]	R/W	0	Opcode_Repeat_Count	Repeat the number of times
	[13:0]	R/W	0	Opcode_DWRD_Count	To be write at “DWORD”(32bit) size.
	[3:0]	R/W	0	Opcode_Status	Sync code (FM:6, SOL:2, EOL:1, VRE:4, VRO:C, PXV:0)

Destination address in DMA instruction (0 –15)					
Address	Bits	Type	Default	Name	Description
006C 0080 0094 00A8 00BC 00D0 00E4 00F8	[31:0]	R/W	0	Ch(0–15)_taddr	Destination address in DMA instruction (JUMP = jump address, RWRITE = write data, SYNC = ignore) When opcode is wirte, that is Target address.

OPCODE in DMA instruction (0 –15)					
Address	Bits	Type	Default	Name	Description
0070 0084 0098 00AC 00C0 00D4 00E8 00FC	[31:0]	R/W	0	Ch(0–15)_pointer	The address of next opcode that will be read.

ERROR FROM DMA					
Address	Bits	Type	Default	Name	Description
01B4	[31:16]	R	0	Reserved	Reserved
	[15:14]	R	0	Err_Ch7	
	[13:12]	R	0	Err_Ch6	
	[11:10]	R	0	Err_Ch5	
	[9:8]	R	0	Err_Ch4	
	[7:6]	R	0	Err_Ch3	
	[5:4]	R	0	Err_Ch2	
	[3:2]	R	0	Err_Ch1	
	[1:0]	R	0	Err_Ch0	

4.2.2 GPIO Status Register

Address	Bits	Type	Default	Name	Description
0x1C0	[31:26]	R/W	0	GPIO_INT_ctrl	1:Rising Edge Bit0=GPIO[3:0] Bit1=GPIO[7:4] GPIO interrupts when its input value changes.
	[25:24]	R	0	Reserved	
	[23:0]	R/W	0	GP_INT_MASK	If set to 1, INT occurs. It performs command from GPIO_INT_ctrl.
Address	Bits	Type	Default	Name	Description
0x1C4	[31:24]	R	0	Reserved	
	[23:0]	R/W	FFFFFFFF	GPIO_Data_in	If Written, output from GPIO, If Read, input to GPIO data
Address	Bits	Type	Default	Name	Description
0x1C8	[31:24]	R	0	Reserved	
	[23:0]	R/W	FFFFFFFF	GPIO_oe	If set to 1, GPIO is output If set to 0, GPIO is input.

4.2.3 I2C Status Register

Address	Bits	Type	Default	Name	Description
0x1D0	[31:16]	R	FFFF	Reserved	
	[15:0]	R/W	D540	csrI2C_ClkCnt	I2C Clock=PCI CLK / (I2C_ClkCnt*2)
Address	Bits	Type	Default	Name	Description
0x1D4	[31]	R/W	0	I2C_SWMode	1=SWMode
	[30]	R/W	1	I2C_SData	I2C SData
	[29]	R/W	1	I2C_SCLK	I2C SClk
	[28:27]	R	0	Reserved	
	[26:24]	R/W	0	I2C_State	Bit2=ACK, bit1=busy, bit0=transmitting
	[23:16]	R/W	0	I2C_Read	I2C Read data
	[15:11]	R/W	0	I2C_Control	bit4:start, bit3:stop, bit2:read, bit1:write, bit0:ack
	[10:8]	R	0	Reserved	
	[7:0]	R/W	FF	I2C_Write	I2C Write data

I2C Write User manual

1. In 12C_Control make bit4 and Bit1 into 1, and make Bit0 into 0 (Start, Write, ACK), Write 12C address in 12C_Write.

2. In 12C_Control make bit1 into 1 and make bit0 into 0 (Write, ACK), Write 12C address in 12C_Write.

3. After occurring number 2, in 12C_Control make bit3 into 1(Stop,Wite,ACK) after writing the last data in 12C_Write, command is finished.

4. Through 12C_Control used in number 1,2,3, insert ACK that is wanted by bit0(ACK)

I2C Read user manual

1. In 12C_Control make bit4 and bit1 into 1 and bit0 to 0(start, write, ACK) then, write 12C write address(IC Addr) in 12C_Write.

2. In 12C_Control make bit1 into 1 and bit0 into 0(write, ACK) then write 12C Data (Register number in IC) in 12C_Write. If Register in IC is not required, number 1,2 is not needed.

3. In 12C_Control make bit4 and bit1 into 1 and bit0 into 0(start, write, ACK) then write 12C Read address (IC Addr) in 12_C write)

4. In 12C_Control make bit2 into 1 and bit0 into 0(write, ACK). If you read number HID4, there is a data read and used by 12C in 12C_Read.

5. After reading 12C repeat number4

6. If you read number HID4 after making bit3, bit2 and bit0 into 1 in 12C_Control, there is last data in 12C_Read.

4.2.4 VIDEO DECODER Status Register (each channel)

Video Decoder Status Register(each Channel)					
Address	Bits	Type	Default	Name	Description
0x200 0x280 0x300 0x380	[31]	R/W	0	Reg_DecEn	decoder enable(1=enable)
	[30]	R/W	0	Reg_StandardSet	Video input format select(1:PAL, 0:NTSC)
	[29]	R/W	1	Reg_StandardAuto	1= AUTO selecter 0=setting up "reg_StandardSet"
	[28:27]	R/W	0	Reg_LockMode	0= check Lock in VB period 1= active video image region 2= start line of the video image 3= end line of the video image
	[26]	R/W	1	Reg_UnlockSCR	1= unlock (Blue Screen),
	[25]	R/W	1	Reg_SyncAuto	1= auto detect HSync.
	[24]	R/W	1	Reg_AGCOn	1= AGC enable
	[23]	R/W	0	Reg_AGCBlkOffMod	1= Black Level Value, 0=1/8 of the total
	[22:15]	R/W	20	Reg_AGCBlkOffSet	black level value
	[14:12]	R/W	0	Reg_ColorFormat	0:YUV2, 1:BTYUV, 2:Y8, 3:YUV420, 4:RGB8 5:RGB15, 6:RGB16, 7:RGB24
	[11:0]	R/W	2500	Reg_27M_HTotal	Clock Number of One line(27MHz)
Address	Bits	Type	Default	Name	Description
0x204 0x284 0x304 0x384	[31:30]	R/W	0	Reg_Ch_MinMode	Mode of MIN's value.
	[29:24]	R/W	20	Reg_PalSwHuel	If PalSwHue =1 then turn on set value
	[23:16]	R/W	5	Reg_AGCMargin	When the input signal is in minimum range that is researching point
	[15:8]	R/W	30	Reg_AGCMargin_EnT	When the Compare value more big then change to Min value.
	[7:0]	R/W	40	Reg_AGCColor	The basic rate of the Color Range.
Address	Bits	Type	Default	Name	Description
0x208 0x288 0x308 0x388	[31:30]	R/W	0	Reg_UVOffset	UV Offset(90°)value
	[29;24]	R/W	20	Reg_PalSwRange	PAL Switch Range
	[23:16]	R/W	20	Reg_YRate	Y's amplitude rate
	[15:8]	R/W	20	Reg_URate	U's amplitude rate
	[7:0]	R/W	20	Reg_VRate	V's amplitude rate
Address	Bits	Type	Default	Name	Description
0x20C 0x28C 0x30C 0x38C	[31:24]	R/W	80	Reg_Bright	Brightness
	[23;16]	R/W	80	Reg_Contrast	Contrast
	[15:8]	R/W	80	Reg_Saturation	Saturation
	[7:0]	R/W	80	Reg_Hue	Hue

Address	Bits	Type	Default	Name	Description
0x210 0x290 0x310 0x390	[31:24]	R/W	127	Reg_UPos	The basic rate of the U Position.
	[23:22]	R/W	0	Reserved	
	[21:11]	R/W	352	Reg_HOScale	If odd then it is Horizontal output size of image
	[10:0]	R/W	352	Reg_HEScale	If even then it is Horizontal output size of image
Address	Bits	Type	Default	Name	Description
0x214 0x294 0x314 0x394	[31:24]	R/W	131	Reg_VPos	The basic rate of the V Position.
	[23:22]	R	0	Reserved	
	[21:11]	R/W	288	Reg_VOScale	If odd then it is Vertical output size of image
	[10:1]	R/W	288	Reg_VEScale	If even then it is Vertical output size of image
Address	Bits	Type	Default	Name	Description
0x218 0x298 0x318 0x398	[31]	R	0	Reserved	
	[30]	RW	1	Reg_LineMode	0=set to line number in VB Down 1=set to line number in VB UP
	[29:26]	RW	3	Reg_AGCIREatj	Set to changed maximum value in AGC IRE.
	[25]	R/W	2	Reg_ComFltSel1	0= used “Y” Peaking
	[24]	R/W	0	Reg_ComFltSel0	0=used “C” average value
	[23:16]	R/W	0	Reg_Peaking	Stress Peaking edge
	[15:8]	R/W	02	Reg_ComFltT1	Comb Filter Select 1
	[7:0]	R/W	04	Reg_ComFltT2	Comb Filter Select 2
Address	Bits	Type	Default	Name	Description
0x21C 0x29C 0x31C 0x39C	[31]	R/W	1	Reg_MultiOn	Multi channel use time deley. 0=not use, 1=use reg_multidelay
	[30;29]	R/W	0	Reg_MultiSel	Select external video input signal
	[28]	R/W	0	Reg_FieldMode	0=not use overlap field 1=use pertinent field
	[27]	R/W	0	Reg_VBMode	VB Selector if set to “1” = immediate output Set to “0” = according to HB Signal.
	[26:24]	R	0	Reserved	
	[23:0]	R/W	300	Reg_MultiDelay	After selecting channel it is used for value of clock delay.
Address	Bits	Type	Default	Name	Description
0x220 0x2A0 0x320 0x3A0	[31]	R	0	Reserved	
	[30;16]	R/W	21F0	Reg_NCLKRate	NTSC clock rate (54Mhz*reg_NCLKRate)
	[15]	R	0	Reserved	
	[14:0]	R/W	2A09	Reg_PCLKRate	PAL clock rate ((54Mhz*reg_PCLKRate)

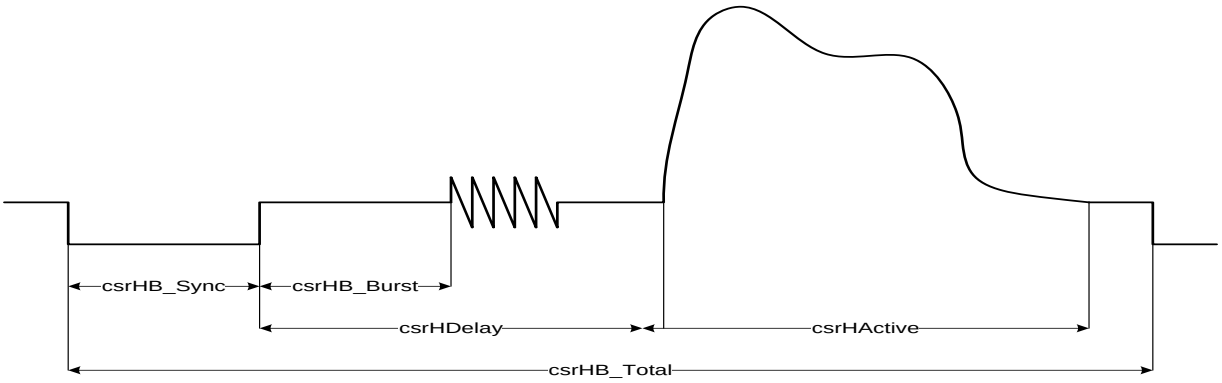
Address	Bits	Type	Default	Name	Description
0x240 0x2C0 0x340 0x3C0	[15:12]	R	4	AGCDebug_Min	Min value
	[11:8]	R	4	AGCDebug_Blk	Black Level value
	[7:4]	R	4	AGCDebug_Ran	Range value
	[3:0]	R	4	AGCDebug_Col	Color Range value

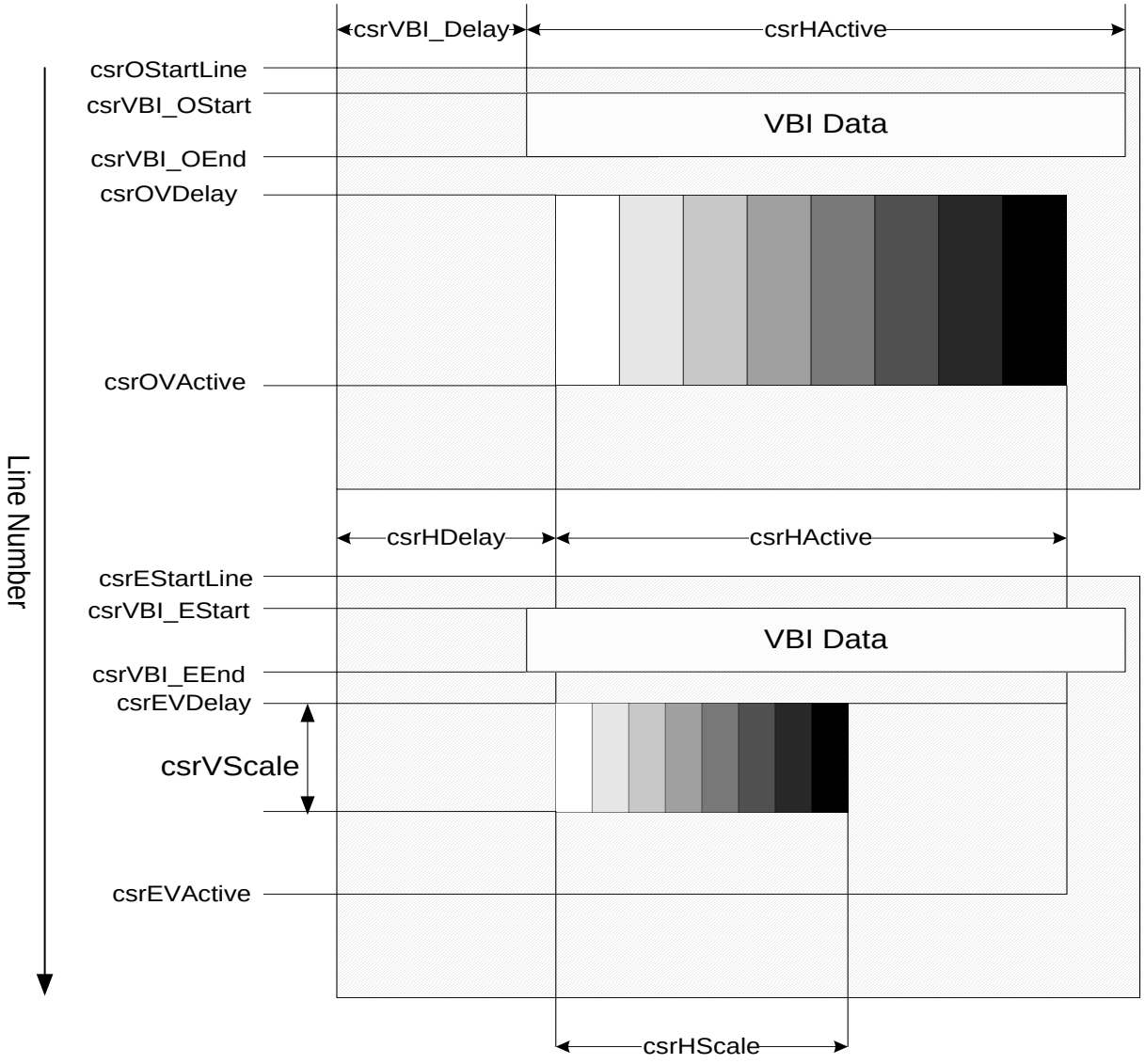
NTSC VIDEO SOURCE					
Address	Bits	Type	Default	Name	Description
0x244 0x2C4 0x344 0x3C4	[31:24]	R/W	68	Reg_NHSync	Clock size of NTSC horizontal sync
	[23]	R	0	Reserved	
	[22:12]	R/W	910	Reg_NHTotal	Total number of horizontal period(NTSC)
	[11]	R	0	Reserved	
	[10:0]	R/W	525	Reg_NVTotal	Total line number of video signal(NTSC)
Address	Bits	Type	Default	Name	Description
0x248 0x2C8 0x348 0x3C8	[31:24]	R/W	12	Reg_NHBurst	Start position of color burst(NTSC)
	[23]	R	0	Reserved	
	[22:12]	R/W	112	Reg_NHDelay	Start position of horizontal image(NTSC)
	[11]	R	0	Reserved	
	[10:0]	R/W	768	Reg_NHActive	Pixel number of horizontal period(NTSC)
Address	Bits	Type	Default	Name	Description
0x24C 0x2CC 0x34C 0x3CC	[31:22]	R/W	4	Reg_NOStart	Start line number of odd field(NTSC)
	[21]	R	0	Reserved	
	[20:11]	R/W	22	Reg_NODelay	Start line number for image display in odd field(NTSC)
	[10]	R	0	Reserved	
	[9:0]	R/W	240	Reg_NOActive	Line number of image period in odd field(NTSC)
Address	Bits	Type	Default	Name	Description
0x250 0x2D0 0x350 0x3D0	[31:22]	R/W	266	Reg_NEStart	Start line number of even field(NTSC)
	[21]	R	0	Reserved	
	[20:11]	R/W	285	Reg_NEDelay	Start line number for image display in even field(NTSC)
	[10]	R	0	Reserved	
	[9:0]	R/W	240	Reg_NEActive	Line number of image period in even field(NTSC)

PAL VIDEO SOURCE					
Address	Bits	Type	Default	Name	Description
0x254 0x2D4 0x354 0x3D4	[31:24]	R/W	82	Reg_PHSync	Clock size of PAL horizontal sync
	[23]	R	0	Reserved	
	[22:12]	R/W	1118	Reg_PHTotal	Total number of horizontal period(PAL)
	[11]	R	0	Reserved	
	[10:0]	R/W	625	Reg_PVTotal	Total line number of video signal(PAL)
Address	Bits	Type	Default	Name	Description
0x258 0x2D8 0x358 0x3D8	[31:24]	R/W	16	Reg_PHBurst	Start position of color burst(PAL)
	[23]	R	0	Reserved	
	[22:12]	R/W	150	Reg_PHDelay	Start position of horizontal image(PAL)
	[11]	R	0	Reserved	
	[10:0]	R/W	910	Reg_PHActive	Pixel number of horizontal period(PAL)
Address	Bits	Type	Default	Name	Description
0x25C 0x2DC 0x35C 0x3DC	[31:22]	R/W	1	Reg_POStart	Start line number of odd field(PAL)
	[21]	R	0	Reserved	
	[20:11]	R/W	23	Reg_PODelay	Start line number for image display in odd field(PAL)
	[10]	R	0	Reserved	
	[9:0]	R/W	288	Reg_POActive	Line number of image period in odd field(PAL)
Address	Bits	Type	Default	Name	Description
0x260 0x2E0 0x360 0x3E0	[31:22]	R/W	313	Reg_PEStart	Start line number of even field(PAL)
	[21]	R	0	Reserved	
	[20:11]	R/W	336	Reg_PEDelay	Start line number for image display in even field(PAL)
	[10]	R	0	Reserved	
	[9:0]	R/W	288	Reg_PEActive	Line number of image period in even field(PAL)
Address	Bits	Type	Default	Name	Description
0x26C 0x2EC 0x36C 0x3EC	[31:27]	R		Reserved	
	[26:16]	R		Debug_HTotal	Available counter number of total horizontal line
	[15]	R		Standard_Sel	NTSC, PAL select
	[14:8]	R		Reserved	
	[7:0]	R		Debug_HSync	Available counter number of horizontal sync

Audio Channel Register					
Address	Bits	Type	Default	Name	Description
0x270 0x2F0 0x370 0x3F0	[31]	R/W	0	Reg_AudEn	1= Audio Decoder Enable
	[30:29]	R/W	1	Reg_AudMode	Audio Format 0:8bit Mono,1:8bit Stereo, 2:16bit Mono, 3:16bit Stereo
	[28:25]	R/W	2	Reg_AudLine	Be Transmit line number with DMA
	[24:12]	R/W	1024	Reg_AudActive	Data number of one line with DMA
	[11:0]	R/W	451	Reg_AudClkScale	Audio sampling rate

4.2.5 Video Decoder Timing Relationship





5.0 Parametric Information

5.1 DC Electrical Parameters

Recommended operating conditions

Symbol	Parameter		Min	Norm	Max
VDD	Pre-driver supply voltage		1,62V	1.8V	1.98V
VDD33	I/O supply voltage		2.97V	3.3V	3.63V
V_{IH}	Input High Voltage		2.0V		5.5V
V_{IL}	Input Low Voltage		-0.3V		0.8V
V_T	Threshold point		1.45V	1.58V	1.74V
V_{T+}	Schmitt trig Low to High threshold point		1.44V	1.50V	1.56V
V_{T-}	Schmitt trig High to Low threshold point		0.89V	0.94V	0.99V
T_J	Junction Temperature		0℃	25℃	125℃
I_L	Input Leakage Current				±10uA
I_{OZ}	Tri-State output leakage current				±10uA
R_{PU}	Pull-up Resistor		39kohm	65kohm	116kohm
R_{PD}	Pull-down Resistor		40kohm	56kohm	108kohm
V_{OL}	Output low voltage @ I_{OL}=2.4 …24mA				0.4V
V_{OH}	Output high voltage @ I_{OH}=2.4 …24mA		2.4V		
I_{OL}	Low level output current @ V_{OL}=0.4V	2mA	2.4mA	4.0mA	5.0mA
		4mA	4.7mA	8.0mA	10mA
		8mA	9.4mA	15.9mA	19.8mA
		12mA	14.2mA	23.9mA	29.8mA
		16mA	18.9mA	31.8mA	39.8mA
		24mA	28.3mA	47.8mA	59.7mA
I_{OH}	High level outpur current @ V_{OH}=2.4V	2mA	2.8mA	5.9mA	9.5mA
		4mA	5.6mA	11.9mA	19mA
		8mA	11.2mA	23.8mA	38.3mA
		12mA	16.8mA	35.7mA	57mA
		16mA	22mA	47.7mA	76mA
		24mA	33.7mA	71.5mA	115mA

Absolute Maximum Ratings

Parameters	Value
Input Voltage, V_I	-0.5V~6V
Output Voltage, V_O	-0.5V~6V
Pre-driver power supply voltage	-0.5V~6V
Post-driver Power supply voltage	-0.5V~6V
Operation Temperature, T_{OPT}	-40℃~+125℃
Storage Temperature, T_{STG}	-65℃~+150℃

Recommended operating conditions

Symbol	Description	Min	Typ	Max	Unit
VCCK	Core power supply	1.62	1.8	1.98	V
VCC3IO	Power supply of 3.3V I/O	2.97	3.3	3.63	V
VCC18IO	Power supply of 1.8V I/O	1.62	1.8	1.98	V
VCC3A_ADC	Power supply of 3.3V Audio ADC Analog	3.0	3.3	3.6	V
VCC3D_ADC	Power supply of 3.3V Audio ADC Digital	3.0	3.3	3.6	V
VCC3K_ADCA	Power supply of 3.3V Video ADC1 Digital	3.0	3.3	3.6	V
VCC3A_ADCA	Power supply of 3.3V Video ADC1 Analog	3.0	3.3	3.6	V
VCC3K_ADCB	Power supply of 3.3V Video ADC2 Digital	3.0	3.3	3.6	V
VCC3A_ADCB	Power supply of 3.3V Video ADC2 Analog	3.0	3.3	3.6	V
T_J	Junction operating temperature	—40	25	125	℃

Leakage current and capacitance

Leakage current and capacitance

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Iin	Input current	No pull-up or pull-down	-10	?	10	uA
Ioz	Tri-state leakage current		-10	?	10	uA
Cin	Input capacitance			2.2		pF
Cout	Output capacitance			2.2		pF
Cbid	Bi-direction buffer capacitance			2.2		pF

I/O Cells (3.3V buffer)

[I/O Cells (3.3V buffer)]

Symbol	Description	Condition	Min	Typ	Max	Unit
Temp	Junction temperature		-40	25	125	℃
V_{il}	Input low voltage	3.3V LVTTL			0.8	V
V_{ih}	Input high voltage		2.0			V
V_{t-}	Schmitt trigger negative going threshold voltage	3.3V LVTTL	0.8	1.15		V

V_{t+}	Schmitt trigger positive going threshold voltage			1.65	2.0	V
V_{ol}	Output low voltage	$\|I_{ol}\|$ = 2 ~ 16mA			0.4	V
V_{oh}	Output high voltage	$\|I_{oh}\|$ = 2 ~ 16mA	2.4			V
R_{pu}	Input pull-up resistance	V_{in} = 0	40	75	190	KΩ
R_{pd}	Input pull-down resistance	V_{in} = VCC3I	40	75	190	KΩ
I_{in}	Input leakage current	V_{in} = VCC3IO or 0V	−10	±1	10	μA
C_{in}	Input capacitance	3.3V I/O		2.17		pF

I/O Cells (PCI 33/66 with 5V Tolerant buffer)

Symbol	Description	Condition	Min	Typ	Max	Unit
Temp	Junction temperature		−40	25	125	℃
VCC3V	I/O Supply Voltage		2.97	3.3	3.63	V
V_{il}	Input low voltage		-0.5		0.3Vcc3v	V
V_{ih}	Input high voltage		0.5Vcc3v		Vcc3v+0.5	V
V_{ol}	Output low voltage	I_{out} = 1500μA			0.1Vcc3v	V
V_{oh}	Output high voltage	I_{out} = - 500μA	0.9Vcc3v			V
I_{il}	Input leakage current	0<Vin<Vcc			±10	μA

5.2 AC Electrical Parameters

AC Characterization Condition

Type	Condition
Typical case	VDD33=3.3V, VDD=1.8V temperature=25℃ Process=Typical-Typical
Best case	VDD33=3.63V, VDD=1.98V temperature=0℃ Process=Fast-Fast
Worst case	VDD33=2.97V, VDD=1.62V temperature=125℃ Process=Slow-Slow
Low temperature	VDD33=3.63V, VDD=1.98V temperature=-40℃ Process=Fast-Fast

5.3 Package Mechanical Drawing

176-pin LQFP Package Mechanical Drawing