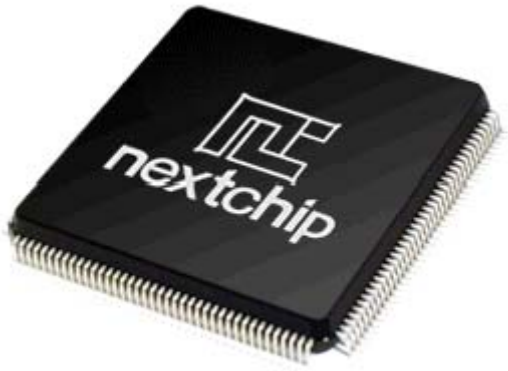
NVP1204

16-Ch NRT Video Decoder and 4-Ch Voice Decoder with DMA Controller Preliminary Data Sheet.



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Preliminary REV 1.0

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16-Ch NRT Video Decoder and 4-Ch Voice Decoder with DMA Controller

: NVP1204 includes 16 Channel NRT Video Decoder, 4 Channel Voice Decoder and Voice/Video DMA Controller. 16 Channel NRT Video Decoder delivers high quality images. It accepts separate 4 CVBS(RT) or 16 CVBS(NRT) inputs from Camera, TV, VCR and the other video signal sources. It digitizes and decodes NTSC/PAL video signal, transfers the converted data to PC via PCI bus. NVP1204 also transfers PCM digital voice signals converted from analog voice input signals. NVP1204 has 4 channel voice ADCs. It supports voice mute detection and volume control. NVP1204 transfers raw data to PC through execution of Voice/Video DMA applied PCI protocol.

Features

Video Decoder

- Fast switching for non-real time video up to 16 channel
- Robust Sync detection for weak and non standard signal
- 16ch NRT or 4ch RT analog CVBS inputs
  - -. Four 4:1 Inner Multiplexers
  - -. Four 10-bit ADCs and Analog clamping circuits
  - -. Fully programmable Static or Automatic gain control
- Accept NTSC-M/J/4.43 and PAL-B/G/H/I/D/K/L/M/N/Nc/60
- Accept Analog CVBS up to 16 channel.
- High-performance 3H/5H 2D adaptive comb filter
- Programmable peaking filter for Luminance
- Vertical Peaking filter
- CTI (Chrominance Transient Improvement)
- Color compensation for PAL
- IF compensation filter
- Robust No-video detection
- Programmable brightness, contrast, saturation and hue

Video Scaler

- High quality horizontal & vertical filtered scaling with arbitrary scale down ratio
- Support various frame resolution
  - -. NTSC : 720x240, 704x240, 640x240, 320x240
  - -. PAL : 720x288, 704x288, 640x288, 720x240, 704x240, 640x240

Voice Decoder

- Accept analog voice input up to 4 channel
- Built in a strong 10bit Pipe-Line ADC for noise
- Support Linear PCM
- Support 16bit/8bit, 8k/16k sampling
- Built in Input Volume Controller
- Built in Mute Detector

PCI

- Built in Voice/Video DMA controller
- Fully PCI Rev.2.2-3.0 compliant
- Support YUV 4:2:2, 4:1:1, 4:2:0 format
- Support 33MHz PCI Clock
- Built in PCI Test pattern generator

MISC.

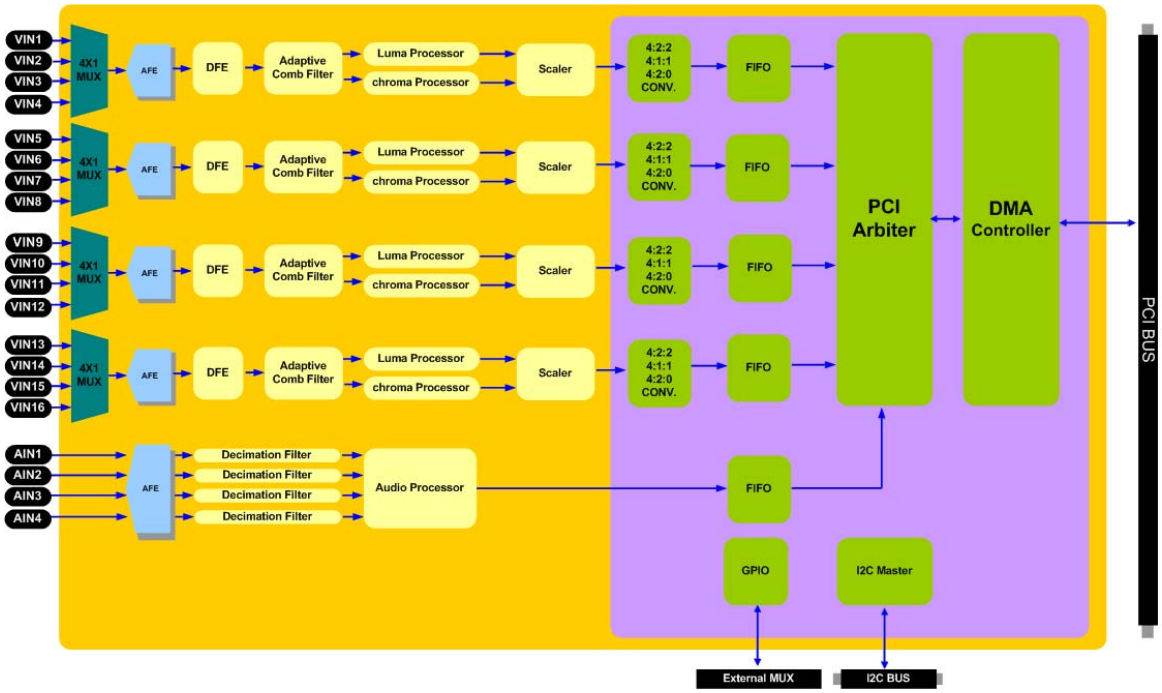
- Auxiliary GPIO port to support External Mux control
- Support two I2C Master
- Single 27MHz Oscillator for all standards
- 5V tolerant I/O

Applications

-. PC Based on Video Security System

Ordering Information

Device	Package	Temperature Range
NVP1204	208QFP	-10 ~ 80℃



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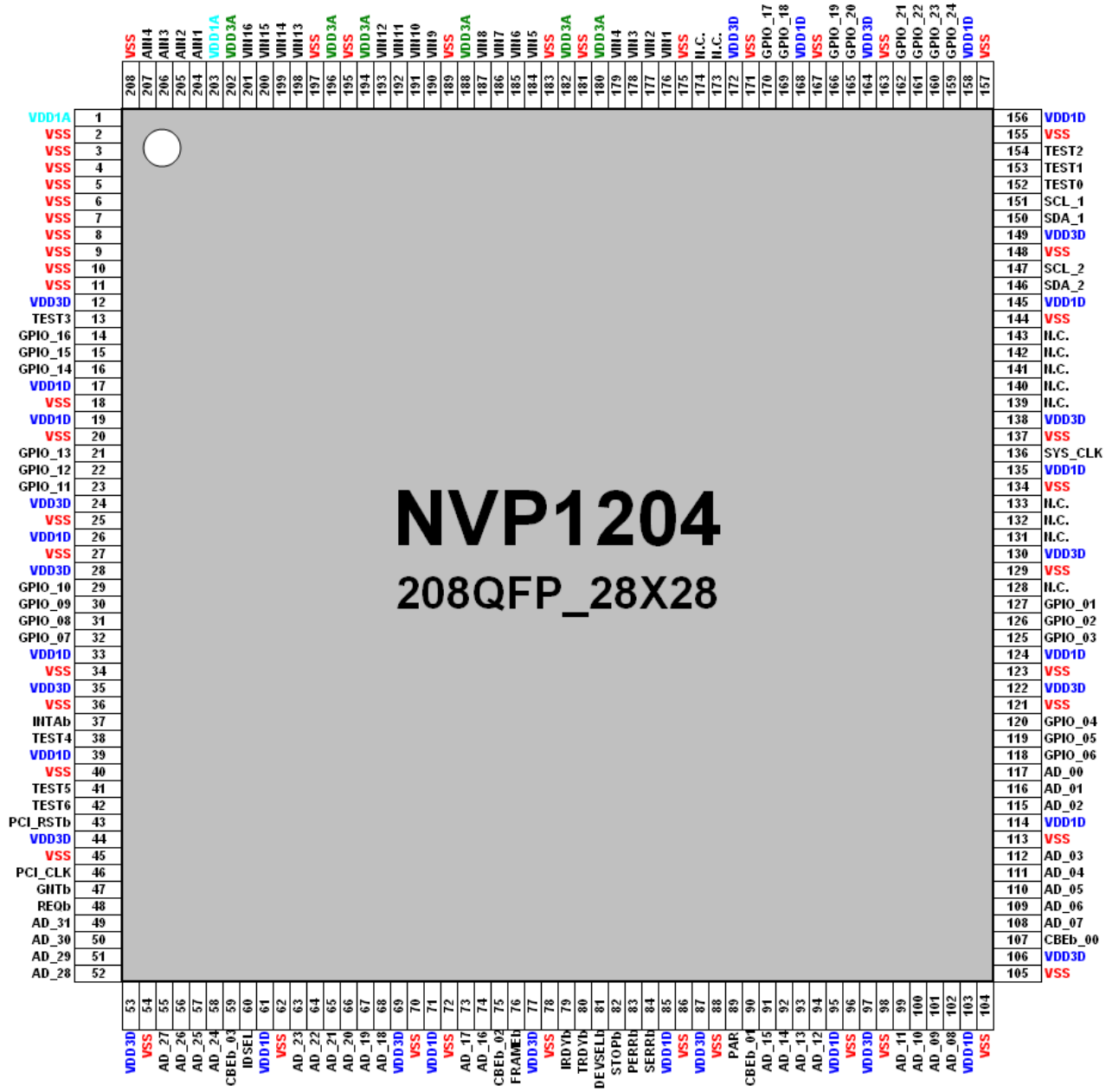
1. Pin Information

1.1 Pin Assignments



1.2 Pin Description

Pin name	Number	Type	Description
Analog Video Interface (16 Pins)			
VIN1, VIN2, VIN3, VIN4, VIN5, VIN6, VIN7, VIN8, VIN9, VIN10, VIN11, VIN12, VIN13, VIN14, VIN15, VIN16,	176, 177, 178, 179, 184, 185, 186, 187, 190, 191, 192, 193, 198, 199, 200, 201,	AI	Analog Video Inputs
Analog Voice Interface (4 Pins)			
AIN1, AIN2, AIN3, AIN4	204, 205, 206, 207	AI	Analog Voice Inputs
PCI Interface (50 Pins)			
PCI_CLK	46	I	PCI Clock (33MHz)
PCI_RSTb	43	I	PCI global Reset (Active Low)
INTAb	37	O	PCI Interrupt output (Active Low)
REQb	48	O	PCI Bus request signal (Active Low)
GNTb	47	I	PCI Bus grant signal (Active Low)
IDSEL	60	I	PCI initialization device select signal
AD_31, AD_30, AD_29, AD_28, AD_27, AD_26, AD_25, AD_24, AD_23, AD_22, AD_21, AD_20, AD_19, AD_18, AD_17, AD_16, AD_15, AD_14, AD_13, AD_12, AD_11, AD_10, AD_09, AD_08, AD_07, AD_06, AD_05, AD_04, AD_03, AD_02, AD_01, AD_00,	49, 50, 51, 52, 55, 56, 57, 58, 63, 64, 65, 66, 67, 68, 73, 74, 91, 92, 93, 94, 99, 100, 101, 102, 108, 109, 110, 111, 112, 115, 116, 117	I/O	Bi-directional PCI I/O pins transfer both address and data signals
CBEb_03, CBEb_02, CBEb_01, CBEb_00	59, 75, 90, 107	I/O	Bi-directional PCI I/O pins transfer both bus command and byte enable signals (Active Low)
FRAMEb	76	I/O	Bi-directional PCI cycle frame signal (Active Low)
IRDYb	79	I/O	Bi-directional PCI initiator ready signal (Active Low)
TRDYb	80	I/O	Bi-directional PCI target ready signal (Active Low)
DEVSELb	81	I/O	Bi-directional PCI device select signal (Active Low)
STOPb	82	I/O	Bi-directional PCI stop signal (Active Low)
PAR	89	I/O	Bi-directional PCI parity signal
SERRb	84	O	Report address parity error
PERRb	83	I/O	Report data parity error
I2C Interface (4 Pins)			
SCL_1, SCL_2	151, 147	I/O	Serial Clock 1, Serial Clock 2
SDA_1, SDA_2	150, 146	I/O	Serial Data 1, Serial Data 2
System Clock (1 Pins)			
SYS_CLK	136	I	System Clock (27MHz)

Pin name	Number	Type	Description
ETC (42 Pins)			
TEST0, TEST1, TEST2, TEST3	152, 153, 154, 13	I	Test Pins (Connect to ground)
TEST4, TEST5, TEST6	38, 41, 42	I	Refer to 8.3 Circuit Configuration
GPIO_24, GPIO_23, GPIO_22, GPIO_21, GPIO_20, GPIO_19, GPIO_18, GPIO_17, GPIO_16, GPIO_15, GPIO_14, GPIO_13, GPIO_12, GPIO_11, GPIO_10, GPIO_09, GPIO_08, GPIO_07, GPIO_06, GPIO_05, GPIO_04, GPIO_03, GPIO_02, GPIO_01	159, 160, 161, 162, 165, 166, 169, 170, 14, 15, 16, 21, 22, 23, 29, 30, 31, 32, 118, 119, 120, 125, 126, 127	I/O	General Purpose I/O
N.C.	128, 131, 132, 133, 139, 140, 141, 142, 143, 173, 174	-	Reserved pin, not connected internally
Power(42 Pins) / Ground (49 Pins)			
VSS (49 Pins)	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 18, 20, 25, 27, 34, 36, 40, 45, 54, 62, 70, 72, 78, 86, 88, 96, 98, 104, 105, 113, 121, 123, 129, 134, 137, 144, 148, 155, 157, 163, 167, 171, 175, 181, 183, 189, 195, 197, 208	G	Ground
VDD3D (17 Pins)	12, 24, 28, 35, 44, 53, 69, 77, 87, 97, 106, 122, 130, 138, 149, 164, 172	P	Digital Power (Digital 3.3V)
VDD1D (17 Pins)	17, 19, 26, 33, 39, 61, 71, 85, 95, 103, 114, 124, 135, 145, 156, 158, 168	P	Digital Power (Digital 1.8V)
VDD3A (6 Pins)	180, 182, 188, 194, 196, 202	P	Analog Power (Analog 3.3V)
VDD1A (2 Pins)	1, 203	P	Analog Power (Analog 1.8V)
NVP1204 208QFP_28x28			

2. Video Decoder

: NVP1204 includes 16 Channel NRT Video Decoder and delivers high quality images. It accepts separate 16 CVBS inputs from Camera, TV or VCR and so on. It digitizes and decodes NTSC/PAL video formats into digital components video.

: NVP1204 includes 4 channel analog processing circuit that comprise anti-aliasing filter, ADC, AGC and CLAMP. It shows the best picture quality adopted by high performance 2D adaptive comb filter and vertical peaking filter. It also supports programmable Saturation, Hue, Brightness and Contrast and several function such as CTI, Programmable peaking filter, PAL compensation, IF compensation filter and White Peak Detect.

2.1 Functional Overview

: The role of video decoder is to separate luminance and chrominance signals from composite video signal.
Figure 2.1 shows the block diagram of decoder part

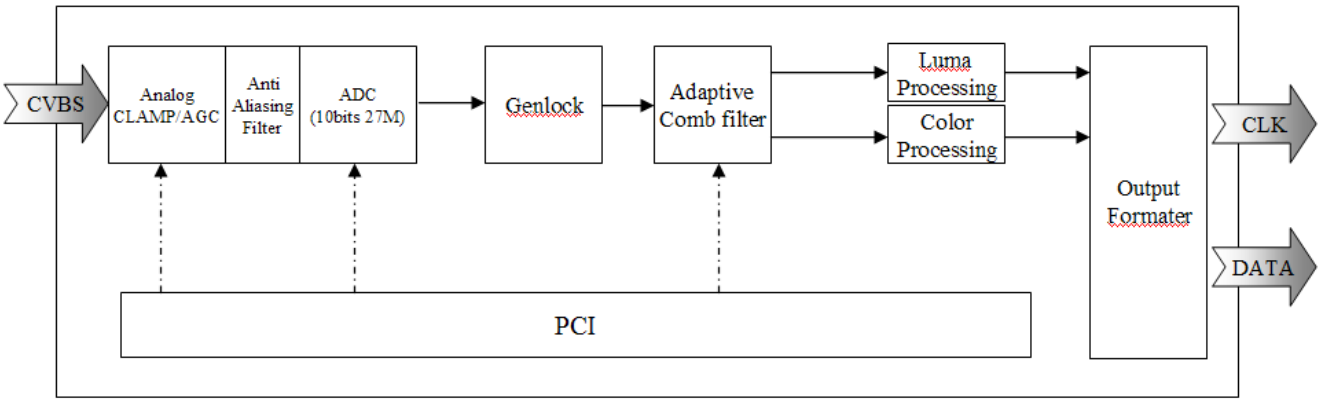


Figure 2.1. Video Decoder Data Flow of NVP1204

The First step to decode composite video signals is to digitize the entire composite video signal using an A/D converter (ADC). NVP1204 uses the 10-bit ADC whose frequency is 27MHz. Video inputs are usually AC-coupled and have a 75 Ohm AC and DC input impedance. As a result, the video signal must be DC restored every scan line during horizontal sync to position the sync tips at known voltage level using the AGC/CLAMP logic. The video signal also is lowpass filtered to about 9MHz in Anti aliasing Filter to remove any high-frequency components that may result in aliasing.

Vertical sync and horizontal sync information are recovered in Genlock block. When composite video signal is decoded, the luminance and chrominance are separated by Adaptive Comb Filter. The quality of decoded image is strongly dependent on the signal quality of separated Y and C. To achieve best quality of image, 2D Adaptive Comb Filter is used.

The chrominance demodulator in color processing block accepts modulated chrominance data from Adaptive Comb Filter which generates Cb/Cr color difference data. During active video period, the chrominance data is demodulated using sine and cosine subcarrier data.

2.2 Video Input Formats

: NVP1204 supports all NTSC/PAL Video Standard. Table 2.1 shows NTSC/PAL Video Standards and Register Setting Value (VIDEO FORMAT, 0x520/530/540/550[28:24]) to support them.

VIDEO_FORMAT	FORMAT	LINE	HZ	Fsc(MHz)
0x00	NTSC-M,J	525	60	3.579545
0x11	NTSC-4.43	525	60	4.43361875
0x1D	PAL-B,D,G,H,I	625	50	4.43361875
0x16	PAL-M	525	60	3.57561149
0x1F	PAL-Nc	625	50	3.58205625
0x15	PAL-60	525	60	4.433619
% Don't use auto-detect mode in case of NRT (Non Real Time) operation				

Table 2.1 NVP1204 Input Video Image Formats

2.3 Analog Front End (CLAMP, AGC, Anti-aliasing Filter)

: NVP1204 includes 4 channel analog processing circuit that comprise anti-aliasing filter, ADC, AGC and CLAMP. Because its design is dedicated to video application, Analog Processing circuit does not require external reference circuit. External coupling capacitance only is needed for NVP1204. Fig 2.2 demonstrates the bode plot of Anti-aliasing Filter. Anti-aliasing Filter is controlled by a Register (FLT_BYPS, 0x5D4[7:4]).

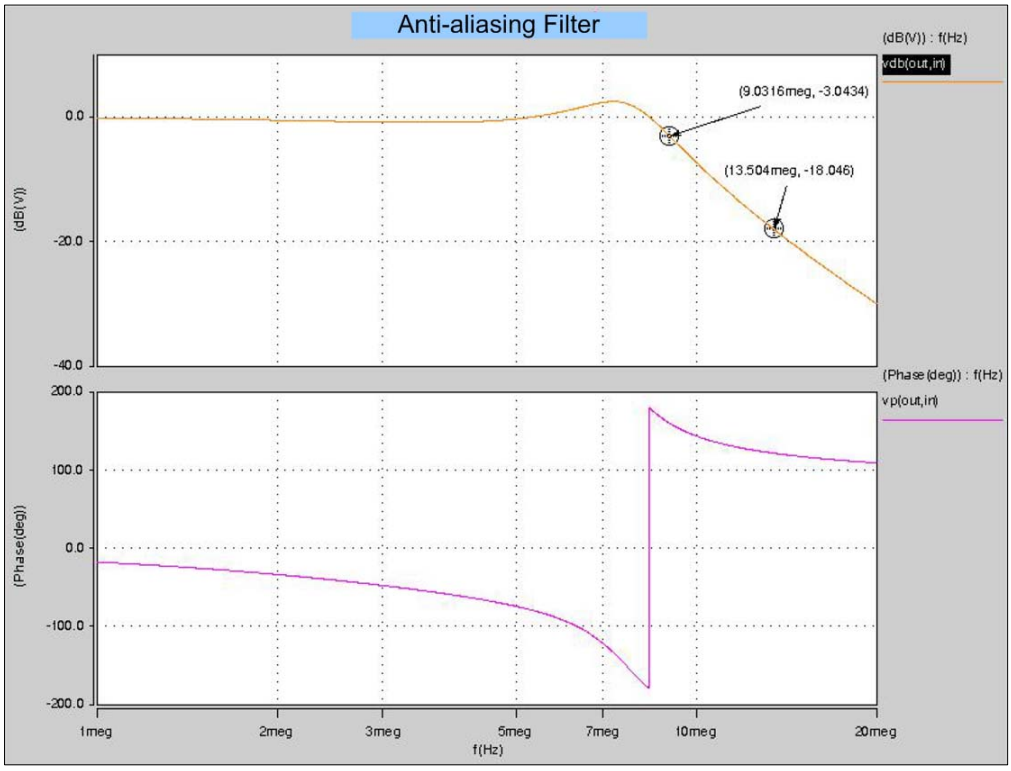


Figure 2.2 Anti-aliasing Filter characteristic

2.4 Genlock (Robust Sync Detection, Robust No-Video Detection)

: NVP1204 provides a fully digital GenLocking circuitry. The digital Genlocking Circuitry uses the locking method of the timing control signals such as horizontal sync, vertical sync, and the color subcarrier. NVP1204 uses the proprietary Genlocking mechanism for video application system. It supports very Robust Sync Detection & Robust No-Video Detection, and it is also showed reliable operation in Non-standard signal and Weak-signal.

2.5 Y/C separation (3H/5H Adaptive Comb Filter)

: An adaptive comb filter is used to separate Y and C signal from NTSC/PAL standard video signal. Therefore, The output image is sharper and clearer compared to other video decoder. To achieve this, BSF(Band Split Filter) is used. Figure 2.3. shows the Chroma BSF which is controlled by Register (BSF_MODE, 0x520/530/540/550[31:30]).

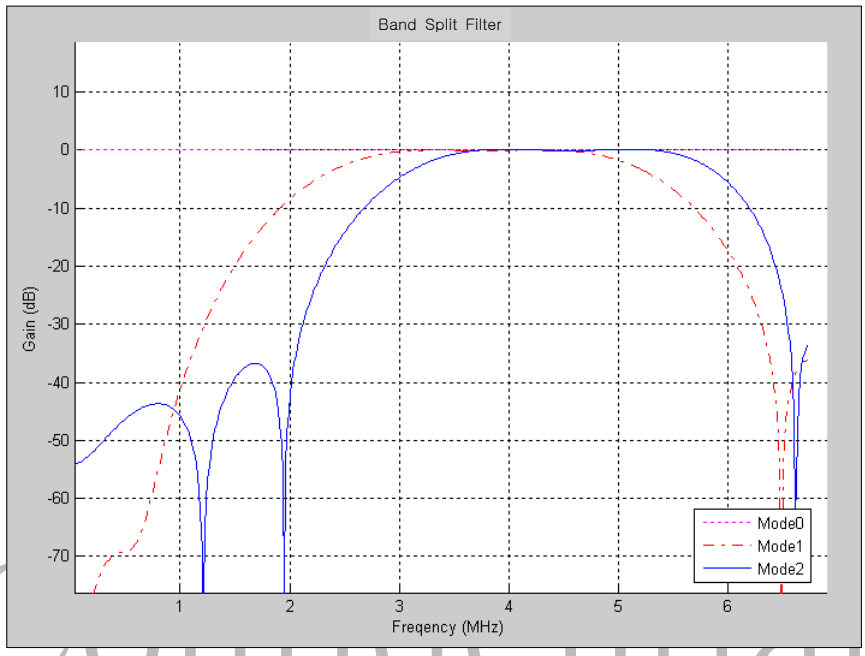


Figure 2.3 Band Split Filter Characteristic

NVP1204 can also separate Y signal from C signal out of input CVBS using the Notch Filter. And according to internal criteria in the NVP1204, the Notch and Comb filters can be mixed for use. In special case, use the Notch filter to separate Y signal from C signal to have a good-quality image.

2.6 Luma Processing

: The high-frequency range of Y/C separated data has a relatively smaller magnitude than the low-frequency range. The high-frequency range makes the image more distinct and remarkable, but may induce worse coding efficiencies when video signal is compressed.

NVP1204 provides the peaking filter and Gain control for emphasizing or depressing the high-frequency area to avoid this problem. The luma filter is applied to this purpose and its characteristics can be controlled by register. (Y_FIR_MODE, 0x528/538/548/558[27:24])

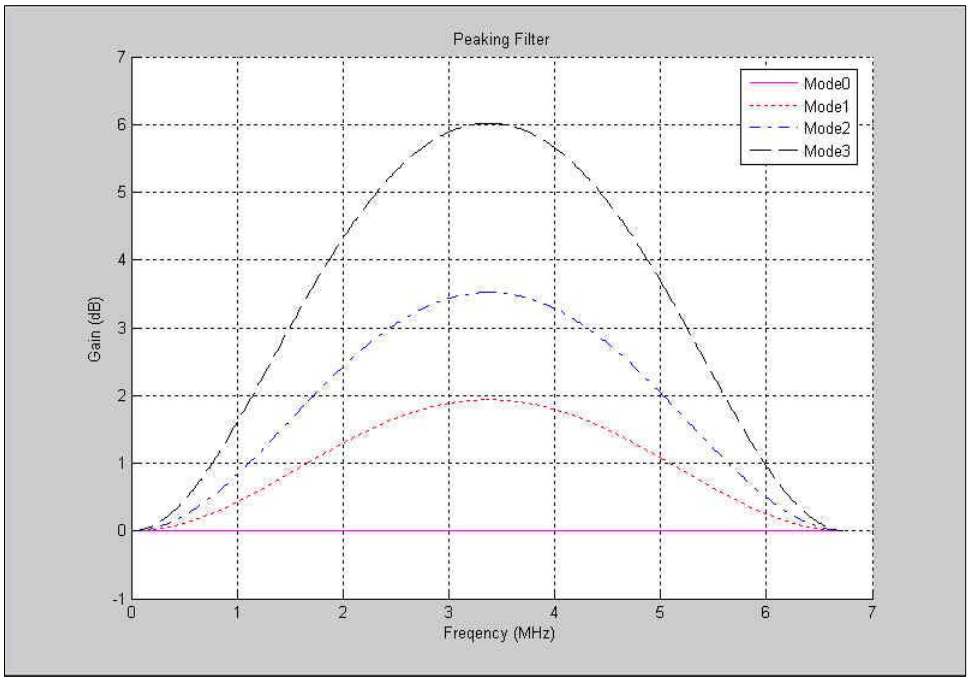


Figure 2.4 Peaking Filter Characteristic

2.7 Chroma Processing

: Chroma processing mainly consists of 3 parts: demodulation, filtering, and ACC(Automatic Chroma-gain Control). The chroma demodulator receives modulated chroma from Y/C separator, and generates demodulated color difference data. Demodulated data must be low-pass filtered to reduce anti-aliasing artifacts.

Figure 2.5. shows chroma demodulation and filtering process. Chroma LPF frequency characteristics is demonstrated in Figure 2.6. Users can select the chroma filter register (CLPF_SEL, 0x57C[25:24]).

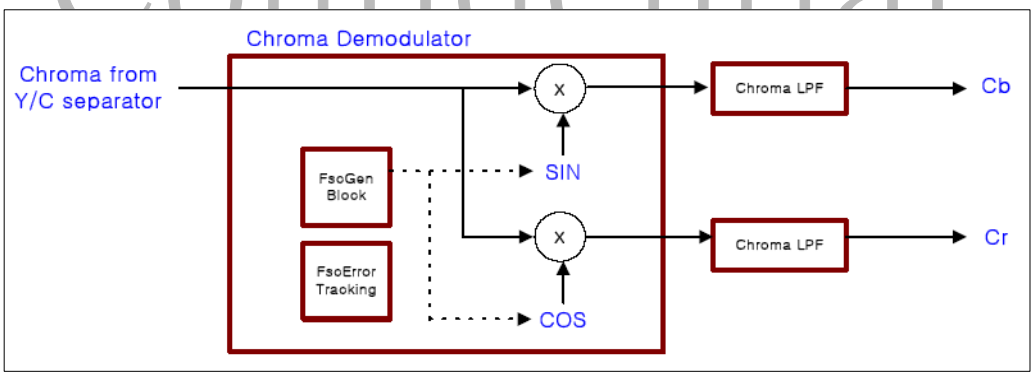


Figure 2.5 Chroma Process

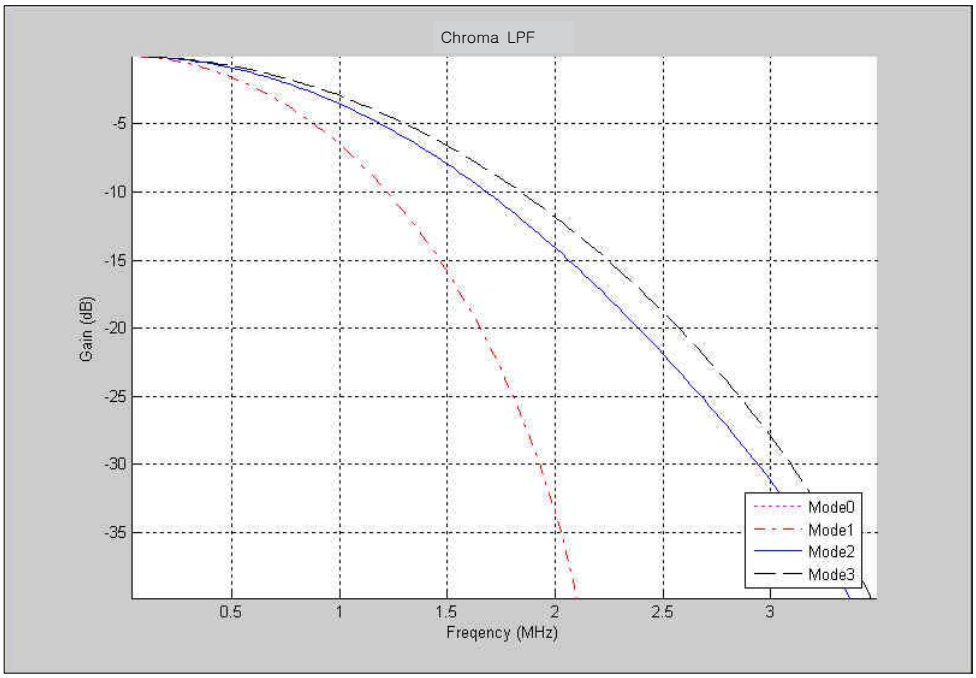


Figure 2.6 Chroma Low Pass filter Characteristic

2.8 White Peak Detector

: Out of the signals inputted from the Video Decoder, there are some signals whose ratio of the Sync Tip to the Video Ratio is not proportional due to the external factors such as Long Cable, Distributor...etc. as shown in Figure 2.7. In order to respond to such entry, NVP1204 supports White Peak Detect function that refers to the white peak information along with the Amplitude information of Sync Tip for the implementation of AGC to reach the Target Gain level. The "White Peak Detect function" can be set as follows depending on what the user needs as shown in Table 2.2.

In order to operate the White Peak Detector, the out of as seen in Figure 2.8 can be generated with the input like the one in Figure 2.7.

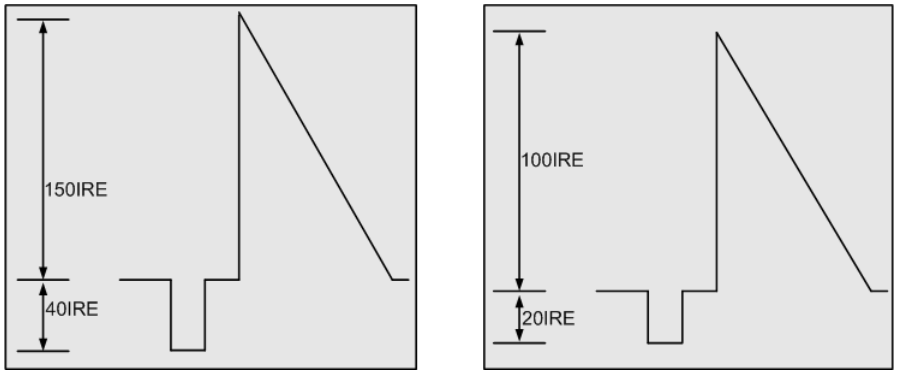


Figure 2.7 Input when the ratio of Sync Tip vs. Video Ratio is not proportional

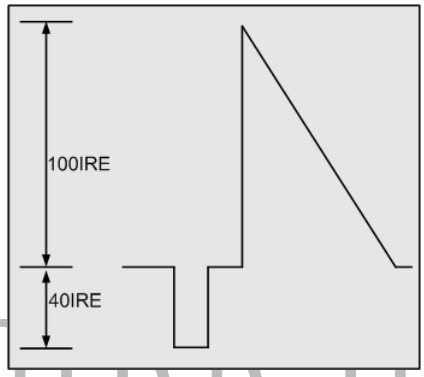


Figure 2.8 Outcome of the White peak Detector

Address	White Peak "On"	White Peak "Off"
0x58C max white value [15:8]	0xB8	0xB8
0x58C max white value num [7:0]	0x01	0x01
0x590 white peak detection AGC error #1 [31:24]	0x06	0x06
0x590 white peak detection AGC error #2 [23:16]	0x06	0x06
0x590 white peak on/off [15]	1	0

Table 2.2 White Peak Detector-Driven Register Setting Value

2.9 Scaler

: NVP1204 has 4 scalers. A Scaler plays a role to reduce input image size to the size user wants. Please refer to the figure as below.

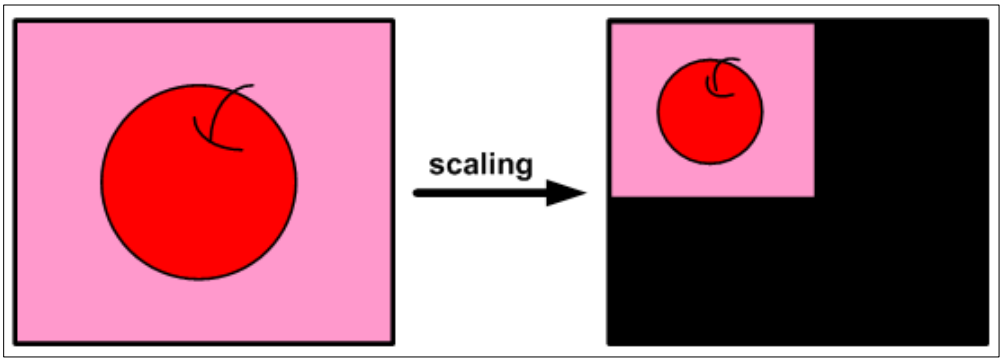


Figure 2.9 Function of Scaler

NVP1204 assigns each decoder to such channel. A User uses this scaler to control the size of input image by 1/32 for horizontal and vertical direction. H-direction's size can be controlled by the H_DTOx[20:0](0x620~0x62C) register and V-direction's one by V_DTOx[20:0](0x630~0x63C) register. The values of H_DTOx and V_DTOx is determined by following formula.

NTSC : H_DTOx[20:0] = (HP_scaled/720)× (2^20)
V_DTOx[20:0] = (VP_scaled/240)× (2^20)
PAL : H_DTOx[20:0] = (HP_scaled/720)× (2^20)
V_DTOx[20:0] = (VP_scaled/288)× (2^20)

Where, HP_scaled indicates horizontal pixel number or the size of the image which a user wants to get. VP_scaled does the same role as HP_scaled but for vertical direction.

For example of using this register, if you need 360x240 scaled image in NTSC, H_DTOx[20:0] shall have the value of (360/720)× 2^20. Simply, H_DTOx[20:0] = 2^19. And V_DTOx[20:0] becomes (120/240)× 2^20. Again, V_DTOx = 2^19

The table as below is register values for common scale sizes.

Register	704x240 (720x240)	640x240	360x240	352x240	320x240
H_DTO1[20:0] (0x620)	0x100000	0x0E8BA3	0x082900	0x080000	0x0745D2
V_DTO1[20:0] (0x630)	0x100000	0x100000	0x100000	0x100000	0x100000

Table 2.3. Register Value for Scale used frequently

NVP1204's scaler has two types of output as you can see in figure 2.9.
In mode1, the area which is not scaled is treated as blank. Therefore it can be longer than existing horizontal blank section. In this case, you should regard that in order to reduce the vertical size, it extend the horizontal blank section instead of using vertical blank. Hence, vertical blank section is able to have over 1 line range only for horizontal blank section under the standard status.(See the left side of Figure 2.10). Mode2 is output-way that let horizontal and vertical blank signals follow the standard and the section which is supposed to be blanked is changed to the value users define. Please refer to Figure 2.10(right side). The blue section displays the result that users define as blue.

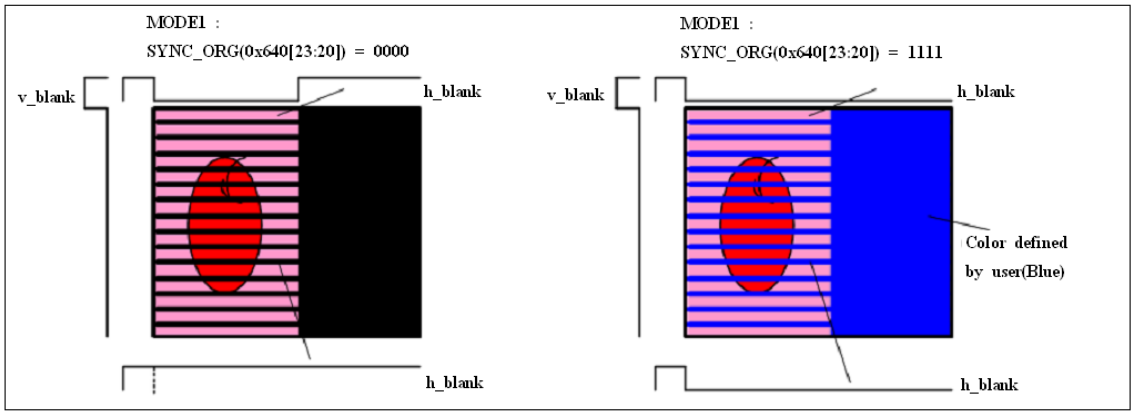


Figure 2.10 Function of Scaler

Figure 2.11 describes more detailed horizontal blank signal of Mode1. This is how scaled signal works in CCIR656 format. SAV packet(0xFF,0x00,0x00,SAV)is fixed, compared with input signal, and EAV packet takes a moving way.

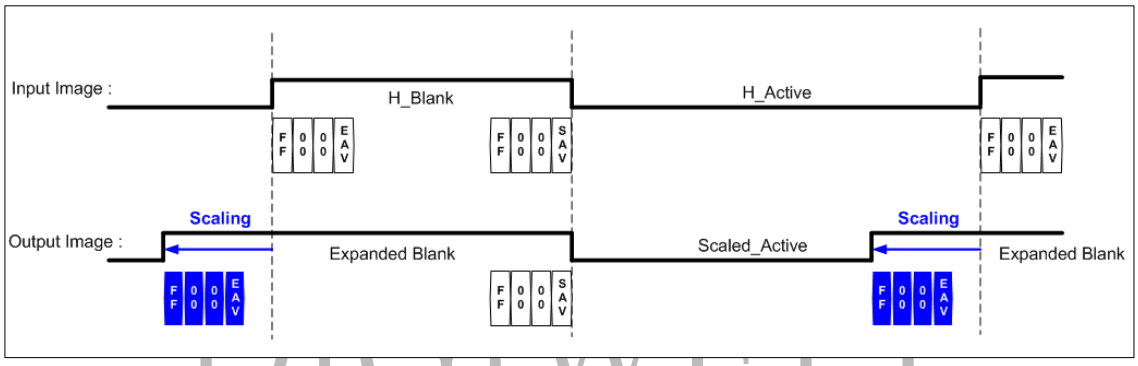


Figure 2.11 Scaled Horizontal Blank Signal of Mode 1

Figure 2.12 describes more detailed horizontal blank signal of Mode2. You might see in the figure that scaled signal is almost matched with horizontal blank signal's standard. But the rest section of the image that scaled signal is displayed is filled with the defined color(Blue) that users choose.

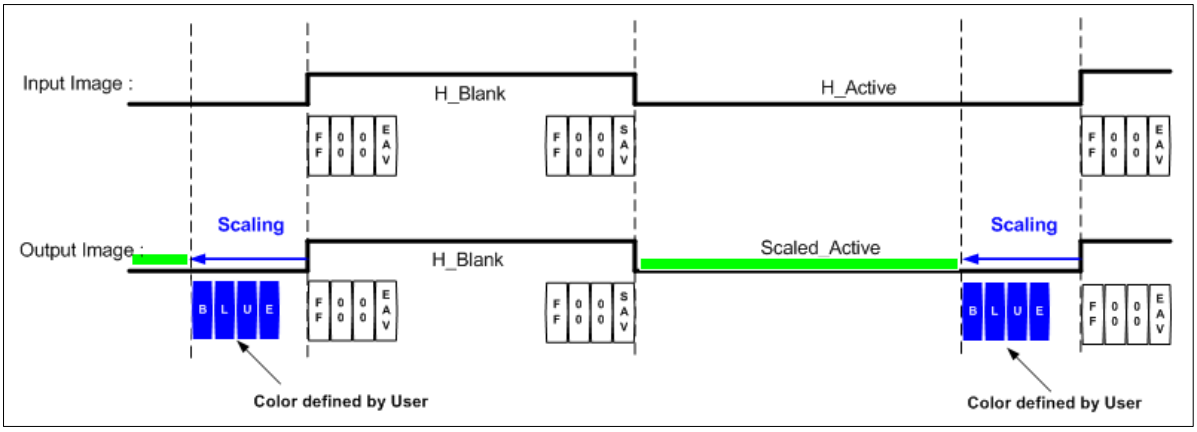


Figure 2.12 Scaled Horizontal Blank Signal of Mode 2

This scaler has a function to increase the 704 active pixel input to 720 size for horizontal direction. for using this function, there is the register to control start position in 16pixel range. That is H_DEL(0x62x[27:24]) (Figure 2.13)

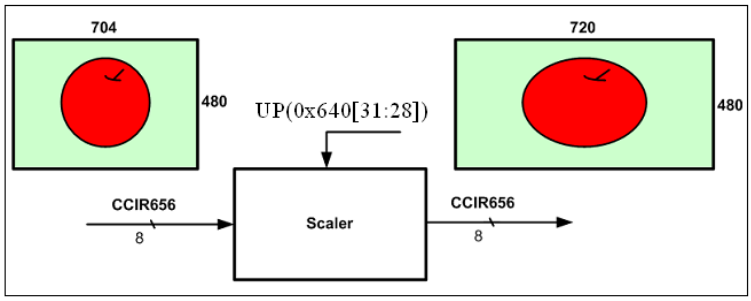


Figure 2.13 720 Extension function

3. Voice Decoder

3.1 Description

: NVP1204 outputs PCM digital voice signals converted from analog voice input signals and transfers voice data to PC via PCI bus. NVP1204 has 4 channel ADCs and each ADC generate 16K / 8K sampled 16bit / 8bit Voice data. In addition, NVP1204 supports voice mute detection and input volume control.

3.2 Mute Detection

: NVP1204 has an voice mute detection block for individual 4 channels. The mute detection scheme uses absolute/differential amplitude detection method. The detection method and accumulated period are defined by the ADET_MODE (0x6A8[15]) and ADET_FILT (0x6A8[18:16]) register, and the detecting threshold values are defined by ADET_TH register (0x6AC).

3.3 Volume Control

: NVP1204 can voice input volume control. Voice input volume control register is AIGAINx(0x6B4).

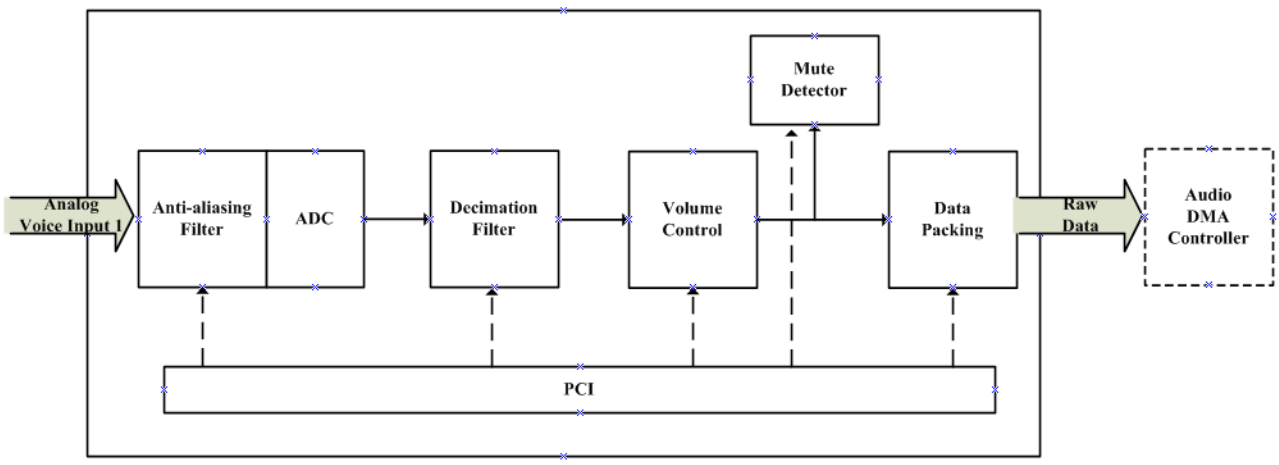


Figure 3.1 Audio Decoder Data Flow of NVP1204

4. PCI Descriptions

PIN Name	PIN #	I/O Type	Signal	Description
PCI Interface (50 Pins)				
PCI_CLK	46	I	PCI Clock	*PCI Clock* provides timing for all PCI transactions. All PCI signals except PCI_RSTb, INTAb are sampled on the rising edge of PCI_CLK and all other timing parameters are defined with respect to this edge. NVP1204 operates 33MHz.
PCI_RSTb	43	I	PCI Reset	*PCI Reset* is used to bring PCI-specific registers, sequencers, and signals to a consistent state. PCI_RSTb may be asynchronous to PCI_CLK when asserted or deasserted.
INTAb	37	O	Interrupt pin	Interrupts on PCI are optional and defined as "level sensitive," asserted low(low active), using open drain output drivers. *Interrupt A* is used to request an interrupt.
REQb	48	O	Request	*Request* indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQb which must be tri-stated while PCI_RSTb is asserted.
GNTb	47	I	Grant	*Grant* indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own GNTb which must be ignored while PCI_RSTb is asserted.
IDSEL	60	I	Initialization Device Select	*Initialization Device Select* is used as a chip select during configuration read and write transactions.
AD[31:0]	49, 50, 51, 52, 55, 56, 57, 58, 63, 64, 65, 66, 67, 68, 73, 74, 91, 92, 93, 94, 99, 100, 101, 102, 108, 109, 110, 111, 112, 115, 116, 117	I/O	Address/Data	*Address and Data* are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phase. PCI supports both read and write bursts. The address phase is the frist clock cycle in the FRAMEb is asserted. During the address phase, AD[31:0] contain a physical address(32bit). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases, AD[7:0] contain the least significant byte(LSB) and AD[32:24] contain the most significant byte (MSB). Write data is stable and valid when IRDYb is asserted; read data is stable and valid when TRDYb is asserted. Data is transferred during those clocks where both IRDYb and TRDYb are asserted.
CBEb[3:0]	59, 75, 90, 107	I/O	Bus Command/ Byte Enables	*Bus Command and Byte Enables* are multiplexed on the same PCI pins. During the address phase of a transaction, CBEb[3:0] define th bus command. During the data phase, CBEb[3:0] are used as Byte Enables. The Bye Enables are valid for the entire data phase and determine which byte lanes carry meaningful data.
FRAMEb	76	I/O	Cycle Frame	*Cycle Frame* is driven by the current master to indicate the beginning and duration of an access. FRAMEb is asserted to indicate a bus transaction is beginning. While FRAMEb is deasserted, the transaction is in the final data phase or has completed.
IRDYb	79	I/O	Initiator Ready	*Initiator Ready* indicates the initiating agent's ability to complete the current data phase of the transaction. IRDYb is usede in conjunction with TRDYb. A data phase is completed on any clock both IRDYb and TRDYb are asserted. During a write, IRDYb indicates that valid data is present on AD[31:0]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDYb and TRDYb are asserted together.

PIN Name	PIN #	I/O Type	Signal	Description
TRDYb	80	I/O	Target Ready	*Target Ready* indicates the target agent's ability to complete the current data phase of the transaction. TRDYb is used in conjunction with IRDYb. A data phase is completed on any clock both TRDYb and IRDYb are asserted. During a read, TRDYb indicates that valid data is present on AD[31:0]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDYb and TRDYb are asserted together.
DEVSELb	81	I/O	Device Select	*Device Select*, When actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSELb indicates whether any device on the bus has been selected.
STOPb	82	I/O	Stop	*Stop* indicates the current target is requesting the master to stop the current transaction.
PAR	89	I/O	Parity	*Parity* is even parity across AD[31:0] and CBEb[3:0]. Parity generation is required by all PCI agents. PAR is stable and valid one clock after each address phase. For data phases, PAR is stable and valid one clock after either IRDYb is asserted on a write transaction or TRDYb is asserted on a read transaction Once PAR is valid, it remains valid until one clock after the completion of the current data phase. The master drivers PAR for address and write data phases; the target dves PAR for read data phase.
SERRb	84	O	System Error	*System Error* is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. IF an agent does not want a non-maskable interrupt to be generated, a different reporting mechanism is required. SERRb is pure open drain and is actively driven for a single PCI clock by the agent reporting the error.
PERRb	83	I/O	Parity Error	*Parity Error* is only for the reporting data parity errors during all PCI transactions except a Special Cycle. The PERRb pin is sustained tri-state and must be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERRb is one clock for each data phase that a data parity error is detected.

5. Register Map

Addr	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x00	Device ID (0x1204)																Vendor_ID (0x1B07)																
0x04	Status																Command															
0x08	Class code																								Revision ID							
0x0C	BIST								Header Type								Latency Timer								Cacheline Size							
0x10	Base Address 0																															
0x14	Reserved																															
0018	Reserved																															
0x1C	Reserved																															
0x20	Reserved																															
0x24	Reserved																															
0x28	Reserved																															
0x2C	Subsystem ID																Subsystem Vendor ID															
0x30	Expansion ROM Base Address																															
0x34	Reserved																								Capabilities Ptr							
0x38	Reserved																															
0x3C	Max_Lat								Min_Gnt								Interrupt Pin								Interrupt Line							

Addr	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x100	VID_DMA_BA1_A_REG																															
0x104	VID_DMA_BA1_A_REG_U																															
0x108	VID_DMA_BA1_A_REG_V																															
0x120	VID_DMA_BA2_A_REG																															
0x124	VID_DMA_BA2_A_REG_U																															
0x128	VID_DMA_BA2_A_REG_V																															
0x140	VID_DMA_BA3_A_REG																															
0x144	VID_DMA_BA3_A_REG_U																															
0x148	VID_DMA_BA3_A_REG_V																															
0x160	VID_DMA_BA4_A_REG																															
0x164	VID_DMA_BA4_A_REG_U																															
0x168	VID_DMA_BA4_A_REG_V																															
0x190	0x00								H_SIZE1																0x0				PLANER_MODE			
0x194	0x00								H_SIZE2																0x00							
0x198	0x00								H_SIZE3																0x00							
0x19C	0x00								H_SIZE4																0x00							
0x1A0	0	0	ODD	EVEN	0x0				0x00								0x80								0x00							
0x1A4	0x00								0x20								0x80								0xAD							
0x1A8	0x00								0x00								0x00								0x00							
0x1AC	0x00								0x00								0x00								0x00							
0x1B0	0x00								0x00								0x00								0x00							
0x1B4	0x00								0x00								0x00								0x00							
0x1B8	0x00								0x00								0x00								0x00							
0x1BC	0x00								0x00								0x00								0x00							
0x1C0	VID_DMA_SIZE1_REG																															
0x1C4	VID_DMA_SIZE2_REG																															
0x1C8	VID_DMA_SIZE3_REG																															
0x1CC	VID_DMA_SIZE4_REG																															
0x1D0	0x00								0x00								0x00								0x0				DMA4	DMA3	DMA2	DMA1
0x1D4	VID_IRQ_MASK_REG																															
0x1D8	VID_IRQ_STS_REG																															
0x1F4	VID_CFG_REG																															
0x1F8	VID_DMA_STS_REG																															

Addr	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x200	AUD_DMA_BA_A																															
0x204	AUD_DMA_BA_B																															
0x210	AUD_DMA_SIZE																															
0x218	0x00								0x20								0x00								0x00							
0x220	0x00								0x00								0x00								0x0				0	0	AUD_DMA_CTRL	
0x224	0x00								0x00								AUD_INT_MASK															
0x228	0x00								0x00								0x00								0x0				AUD_INT_STAT			
0x240	0x00								0x00								0	0	I2C_P2_DIR_SDA	I2C_P2_DIR_SCL	I2C_P2_GET_SDA	I2C_P2_GET_SCL	I2C_P2_SET_SDA	I2C_P2_SET_SCL	0	0	I2C_P1_DIR_SDA	I2C_P1_DIR_SCL	I2C_P1_GET_SDA	I2C_P1_GET_SCL	I2C_P1_SET_SDA	I2C_P1_SET_SCL
0x264	0x00								0x00								0x00								0	0	0	0	0	0	0	IRQ_MASK
0x270	GPIO_DIR24	GPIO_DIR23	GPIO_DIR22	GPIO_DIR21	GPIO_DIR20	GPIO_DIR19	GPIO_DIR18	GPIO_DIR17	GPIO_DIR16	GPIO_DIR15	GPIO_DIR14	GPIO_DIR13	GPIO_DIR12	GPIO_DIR11	GPIO_DIR10	GPIO_DIR9	GPIO_DIR8	GPIO_DIR7	GPIO_DIR6	GPIO_DIR5	GPIO_DIR4	GPIO_DIR3	GPIO_DIR2	GPIO_DIR1	Reserved							
0x274	GPIO_OUT24	GPIO_OUT23	GPIO_OUT22	GPIO_OUT21	GPIO_OUT20	GPIO_OUT19	GPIO_OUT18	GPIO_OUT17	GPIO_OUT16	GPIO_OUT15	GPIO_OUT14	GPIO_OUT13	GPIO_OUT12	GPIO_OUT11	GPIO_OUT10	GPIO_OUT9	GPIO_OUT8	GPIO_OUT7	GPIO_OUT6	GPIO_OUT5	GPIO_OUT4	GPIO_OUT3	GPIO_OUT2	GPIO_OUT1	Reserved							
0x278	GPIO_IN24	GPIO_IN23	GPIO_IN22	GPIO_IN21	GPIO_IN20	GPIO_IN19	GPIO_IN18	GPIO_IN17	GPIO_IN16	GPIO_IN15	GPIO_IN14	GPIO_IN13	GPIO_IN12	GPIO_IN11	GPIO_IN10	GPIO_IN9	GPIO_IN8	GPIO_IN7	GPIO_IN6	GPIO_IN5	GPIO_IN4	GPIO_IN3	GPIO_IN2	GPIO_IN1	Reserved							

Addr	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x500	NOVID4	NOVID3	NOVID2	NOVID1	Reserved				Reserved								BW4	BW3	BW2	BW1	FSCLOCK4	FSCLOCK3	FSCLOCK2	FSCLOCK1	AGCSTA4	AGCSTA3	AGCSTA2	AGCSTA1	CMPSTA4	CMPSTA3	CMPSTA2	CMPSTA1
0x504	LINENUM4	LINENUM3	LINENUM2	LINENUM1	FLD4	FLD3	FLD2	FLD1	Reserved								Reserved								Reserved				ADET4	ADET3	ADET2	ADET1
0x508	Reserved								Reserved								Reserved								Reserved							
0x50C	Reserved								Reserved								Reserved								Reserved							
0x518	Reserved								Reserved								Reserved								DEV_ID							
0x51C	Reserved				REV_ID				Reserved								Reserved								Reserved							
0x520	BSF_MODE1		0		VIDEO_FORMAT1				BRIGHTNESS1								CONTRAST1								HUE1							
0x524	SATURATION1								U_GAIN1								V_GAIN1								U_OFFSET1				V_OFFSET1			
0x528	PED_ON1				Y_FIR_MODE1				HSYNC_INV1	VSYNC_INV1	FLD_INV1	Y_DELAY1					H_DELAY1								V_DELAY1							
0x52C	HBLK_END1								VBLK_END1								0x00								0x00							
0x530	BSF_MODE2		0		VIDEO_FORMAT2				BRIGHTNESS2								CONTRAST2								HUE2							
0x534	SATURATION2								U_GAIN2								V_GAIN2								U_OFFSET2				V_OFFSET2			
0x538	PED_ON2				Y_FIR_MODE2				HSYNC_INV2	VSYNC_INV2	FLD_INV2	Y_DELAY2					H_DELAY2								V_DELAY2							
0x53C	HBLK_END2								VBLK_END2								0x00								0x00							
0x540	BSF_MODE3		0		VIDEO_FORMAT3				BRIGHTNESS3								CONTRAST3								HUE3							
0x544	SATURATION3								U_GAIN3								V_GAIN3								U_OFFSET3				V_OFFSET3			
0x548	PED_ON3				Y_FIR_MODE3				HSYNC_INV3	VSYNC_INV3	FLD_INV3	Y_DELAY3					H_DELAY3								V_DELAY3							
0x54C	HBLK_END3								VBLK_END3								0x00								0x00							
0x550	BSF_MODE4		0		VIDEO_FORMAT4				BRIGHTNESS4								CONTRAST4								HUE4							
0x554	SATURATION4								U_GAIN4								V_GAIN4								U_OFFSET4				V_OFFSET4			
0x558	PED_ON4				Y_FIR_MODE4				HSYNC_INV4	VSYNC_INV4	FLD_INV4	Y_DELAY4					H_DELAY4								V_DELAY4							
0x55C	HBLK_END4								VBLK_END4								0x00								0x00							

Addr	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x560	A_CMP_MODE1		0	0	0x0				0x80								0x40								0x7C							
0x564	D_CMP_FZ	0	0	1	1	1	D_CMP_SPD		0x00								D_AGC_FZ	0	1	0	0x0				0x40							
0x568	0x80								SLICE_VALUE								DFE_CORE_LVL				0x8				0x0F							
0x56C	0x0C								0x01								0x15								0x0A							
0x570	0x80								U_OFFSET2				V_OFFSET2				0x88								0x04							
0x574	0x2A								FSC_LOCK_MODE				FSC_LOCK_SPD				0xF0								ACC_OFF		ACC_CORE_LVL		ACC_GAIN_SPD			
0x578	0x57								FLD_DET_MODE	0	0		NOVID_DET_B				0	0	NOVID_SPD						H_SHARPNESS				V_SHARPNESS			
0x57C	PAL_CM_OFF	IF_FIR_SEL			0	0	CLPF_SEL		CTI_CORE	CTI_GAIN			0x3				0x01								0x00							
0x580	0x80								0x00								0x00								0x8				DATA_OUT_MODE			
0x584	0x00								0x00								0x00								0x00							
0x58C	0x00								SLICE_MD								0xB8								0x01							
0x590	0x06								0x06								WPD_ON	0	0	1	0x1				0xB9							
0x594	0xB2								0x05								0x00								0x28							
0x598	V_LOC_SPD								0x00								CKILL4				CKILL3				CKILL2				CKILL1			
0x5A0	0x00								0x00								0x00								0x00							
0x5A4	0x76								0x54								0x32								0x10							
0x5A8	0xFE								0xDC								0xBA								0x98							
0x5AC	0x76								0x54								0x32								0x10							
0x5B0	0xFE								0xDC								0xBA								0x98							
0x5B4	0x00								0x00								0x00								0x00							
0x5B8	0x00								0x00								0x00								0x00							
0x5BC	Reserved (READ ONLY)																															
0x5C0	Reserved (READ ONLY)																															
0x5C4	Reserved (READ ONLY)																															

Addr	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x5D0	0x05								0x33								0x00								0x00							
0x5D4	0xFF								0x55								PD1	PD2	PD3	PD4	0x0				0x00							
0x5D8	G_SEL1								G_SEL2								G_SEL3								G_SEL4							
0x5DC	0xFF								0xAA								0xAA								0x55							
0x5E0	A_CMP_MODE2																0x00								0x00							
0x5E4	0x0F								0x0F								0x0F								0x0F							
0x5E8	0x00								0x00								0x0				0	0	A_ADC_CLK_SEL	0	0	0	0	V_ADC_CLK_SEL	0x0			

Addr	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x610	BLK_PKG1																															
0x614	BLK_PKG2																															
0x618	BLK_PKG3																															
0x61C	BLK_PKG4																															
0x620	0x0				H_DEL_1				0	0	0	H_DTO_1																				
0x624	0x0				H_DEL_2				0	0	0	H_DTO_2																				
0x628	0x0				H_DEL_3				0	0	0	H_DTO_3																				
0x62C	0x0				H_DEL_4				0	0	0	H_DTO_4																				
0x630	0x0				0	0	0	BLK_ OPER1	0	0	0	V_DTO_1																				
0x634	0x0				0	0	0	BLK_ OPER2	0	0	0	V_DTO_2																				
0x638	0x0				0	0	0	BLK_ OPER3	0	0	0	V_DTO_3																				
0x63C	0x0				0	0	0	BLK_ OPER4	0	0	0	V_DTO_4																				
0x640	UP_4	UP_3	UP_2	UP_1	0x0				0x0				SCALE R_SEL4	SCALE R_SEL3	SCALE R_SEL2	SCALE R_SEL1	H_BYP ASS_4	H_BYP ASS_3	H_BYP ASS_2	H_BYP ASS_1	V_BYP ASS_4	V_BYP ASS_3	V_BYP ASS_2	V_BYP ASS_1	0x00							
0x644	0xFF								0xFF								0xFF								0xBF							
0x64C	0x00								0x00								0x33								0x33							
0x650	0x88								0x88								0x00								0x09							
0x654	0x80								0x80								0x80								0x80							
0x658	0x49								0x49								0x49								0x49							
0x65C	0x37								0x37								0x37								0x37							
0x660	0x7B								0x7B								0x7B								0x7B							
0x664	0x58								0x58								0x58								0x58							
0x668	0x08								0x08								0x08								0x08							
0x66C	0x00								0x55								0x00								0x00							
0x670	0x00								0x00								0x00								0xF0							
0x674	0x00								0x00								0x00								0x00							
0x678	0x11								0x11								0x11								0x11							
0x67C	0x00								0x00								0x00								0x00							

Addr	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x680	0x00								0x00								0x00								0x00							
0x684	0x00								0x00								0x00								0x00							
0x688	0x80								0x00								0x00								0x00							
0x68C	0x13								0x13								0x13								0x13							
0x690	0x03								0x03								0x03								0x03							
0x694	0x22								0x22								0x22								0x22							
0x698	0x00								0x00								0x00								0x00							
0x69C	0x51								0xB5								0x51								0xB5							
0x6A0	0x51								0xB5								0x51								0xB5							
0x6A4	SMP_DTO_VALUE																0x03								0x03							
0x6A8	0x00								0x0				0	ADET_FILT			ADET_ MODE	EN_ RESET	0	1	0x0				ADET_1	ADET_2	ADET_3	ADET_4	0xF			
0x6AC	ADET_TH1				ADET_TH2				ADET_TH3				ADET_TH4				0x00								0x00							
0x6B0	0x02								0x00								0x02								0x00							
0x6B4	AIGAIN1				AIGAIN2				AIGAIN3				AIGAIN4				0x00								0x00							
0x6C0	0x00								0x00								0x00								0x00							
0x6C4	0x00								0x00								0x00								0x00							
0x6C8	0x00								0x00								0x00								0x00							
0x6CC	0x00								0x00								0x00								0x00							
0x6D0	0x00								0x00								0x00								0x00							
0x6D4	0x00								0x00								0x00								0x00							
0x6D8	0x00								0x00								0x00								0x00							
0x6DC	0x00								0x00								0x00								0x00							
0x6E0	0x00								0x00								0x00								0x00							
0x6E4	0x00								0x00								0x00								0x00							

6. Register Description

6.1 PCI Configuration space

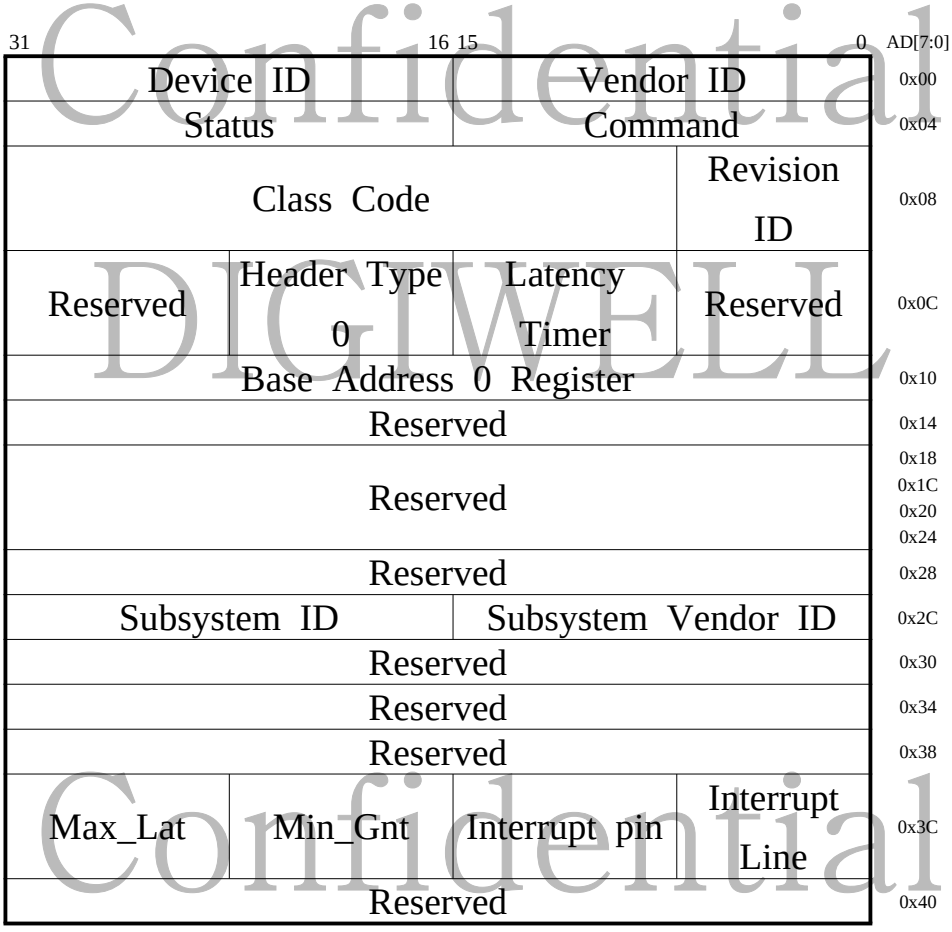


Figure 6.1 PCI Type 0 Configuration Space Header

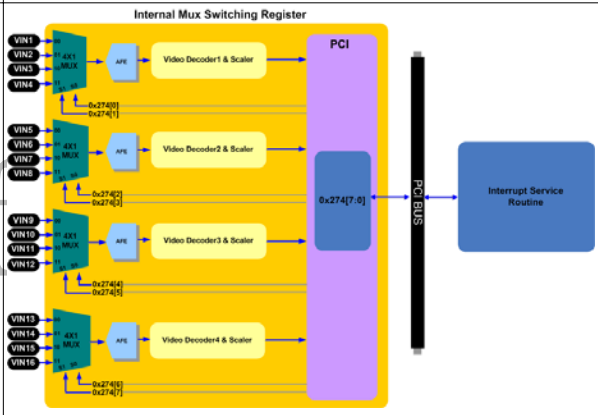
6.2 PCI Configuration register

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE
0x00	Device ID	[31:16]	R	Identifies the particular device of the device.	0x12041B07
	Vendor ID	[15:0]	R	Identifies manufacturer of device, assigned by the PCI SIG.	
0x04	Detected Parity Error	[31]	R/W	Set by a device whenever it detects a parity error, even if parity error handling is disabled.	0x04000000
	Signaled System Error	[30]	R/W	Set by a device that asserts SERR#	
	Received Master Abort	[29]	R/W	Set by a master when it terminates a transaction with Master Abort.	
	Received Target Abort	[28]	R/W	Set by a master when its transaction is terminated by Target Abort.	
	Signaled Target Abort	[27]	R/W	Set by a target when it terminates a transaction with Target Abort. This occurs when detecting an address parity error.	
	Address Decoder Time	[26:25]	R	DEVSEL# Timing 00 = Fast, 01 = medium, 10 = slow, 11 = reserved.	
	Data Parity Reported	[24]	R/W	Only implemented by masters.	
	FB2B Capable	[23]	R	1 = target device supports fasts back to back transactions to different targets.	
	Reserved	[22]	R	1 = device supports "user definable features".	
	66MHz Capable	[21]	R	1 = device is capable of 66MHz operation.	
	Reserved	[20:10]	R/W	Reserved registers	
	FB2B Enable	[9]	R/W	When 1, allows a master to execute fast back to back transactions to different targets.	
	SERR# enable	[8]	R/W	When 1, allows the device to assert SETT#.	
	Wait cycle Control	[7]	R/W	Controls whether a device does address/data stepping.	
	Parity Error Response	[6]	R/W	When 1, the device responds to a detected parity error by asserting PERR#.	
	VGA Palette snoop	[5]	R/W	Controls how VGA devices handle access to VGA palette registers.	
	Memory Write and Invalidate Enable	[4]	R/W	When 1, a master is allowed to use the Memory Write and Invalidate command if so capable. When 0, the master must use Memury Write instead.	
	Special Cycles	[3]	R/W	When 1, allows a device to monitor Special Cycle operations.	
	Bus Master	[2]	R/W	When 1, enables the device to act as a bus master.	
	MemorySpace	[1]	R/W	When 1, allows the device to respond to PCI memory space access	
	IO Space	[0]	R/W	When 1, allows the device to respond to PCI I/O space accesses.	
0x08	Class Code	[31:8]	R	NVP1204 is a multimedia video device.	0x04000000
	Revision ID	[7:0]	R	This register identifies the device revision.	
0x0C	BIST	[31:24]	R	Built In Self-Test Register	0x00001000
	Header Type	[23:16]	R	Type 00h = Configuration Space Header, 01h = PCI to PCI bridges	
	Latency Timer	[15:8]	R/W	The number of PCI bus clocks for the latency timer used by th bus master. Once the latency expires, the master must initiate transaction termination as soon as GNT# is removed.	
0x10	Base Address 0 Register	[31:0]	R/W	Determine the location of the registers in the 32-bit addressable memory space	assigned by cpu
0x2C	Subsystem ID	[31:16]	R	Vendor specific	0x00000000
	Subsystem Vendor ID	[15:0]	R	Identify the vendor of the add-on board or subsystem, assigned by PCI SIG.	
0x3C	Max_Lat	[31:24]	R	It is used for specifying how often the device needs to gain access the PCI bus. in units of 250ns(8clocks)	0x28
	Min_Gnt	[23:16]	R	It is used for specifying how long a burst period the device needs assuming a clock rate of 33MHz. in units of 250ns (8 clocks)	0x10
	Interrupt Pin	[15:8]	R	NVP1204 interrupt pin is connected to INTA#, the only one usable by a single function device.	0x01
	Interrupt Line	[7:0]	R/W	Post software will write the routing information into this register as it initializes and configures the system	assigned by cpu

6.3 PCI part

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x100	VID_DMA_BA1_A_REG	[31:0]	R/W	Assigns channel 1 y base address to main memory space.	**by cpu**
0x104	VID_DMA_BA1_A_REG_U	[31:0]	R/W	Assigns channel 1 cb base address to main memory space.	**by cpu**
0x108	VID_DMA_BA1_A_REG_V	[31:0]	R/W	Assigns channel 1 cr base address to main memory space.	**by cpu**
0x120	VID_DMA_BA2_A_REG	[31:0]	R/W	Assigns channel 2 y base address to main memory space.	**by cpu**
0x124	VID_DMA_BA2_A_REG_U	[31:0]	R/W	Assigns channel 2 cb base address to main memory space.	**by cpu**
0x128	VID_DMA_BA2_A_REG_V	[31:0]	R/W	Assigns channel 2 cr base address to main memory space.	**by cpu**
0x140	VID_DMA_BA3_A_REG	[31:0]	R/W	Assigns channel 3 y base address to main memory space.	**by cpu**
0x144	VID_DMA_BA3_A_REG_U	[31:0]	R/W	Assigns channel 3 cb base address to main memory space.	**by cpu**
0x148	VID_DMA_BA3_A_REG_V	[31:0]	R/W	Assigns channel 3 cr base address to main memory space.	**by cpu**
0x160	VID_DMA_BA4_A_REG	[31:0]	R/W	Assigns channel 4 y base address to main memory space.	**by cpu**
0x164	VID_DMA_BA4_A_REG_U	[31:0]	R/W	Assigns channel 4 cb base address to main memory space.	**by cpu**
0x168	VID_DMA_BA4_A_REG_V	[31:0]	R/W	Assigns channel 4 cr base address to main memory space.	**by cpu**
0x190	H_SIZE1	[23:8]	R/W	Set by a software that determines H size of channel 1 window.	**0x00002C01**
	PLANER_MODE	[3:0]	R/W	Selection of DMA transaction type. 0x1 = 4:2:2 YCbCr Packet mode, 0x2 = 4:1:1 YCbCr Planer mode, 0x4 = 4:2:0 YCbCr Planer mode.	
0x194	H_SIZE2	[23:8]	R/W	Set by a software that determines H size of channel 2 window.	**0x00002C00**
0x195	H_SIZE3	[23:8]	R/W	Set by a software that determines H size of channel 3 window.	**0x00002C00**
0x19C	H_SIZE4	[23:8]	R/W	Set by a software that determines H size of channel 4 window.	**0x00002C00**
0x1A0	ODD	[29]	R/W	Control odd field data of video DMA processing. 0 = enable, 1 = disable.	**0x00000000**
	EVEN	[28]	R/W	Control even field data of video DMA processing. 0 = enable, 1 = disable.	

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x1C0	VID_DMA_SIZE1_REG	[31:0]	R/W	Determines video dma size to occur interrupt signal in ch1. ex) 704x240(window size)/4(32bit transaction size)x2(Luma&Croma) DMA size = 0x14A00	**0x00014A00/ 0x00018C00**
0x1C4	VID_DMA_SIZE2_REG	[31:0]	R/W	Determines video dma size to occur interrupt signal in ch2. ex) 704x240(window size)/4(32bit transaction size)x2(Luma&Croma) DMA size = 0x14A00	**0x00014A00/ 0x00018C00**
0x1C8	VID_DMA_SIZE3_REG	[31:0]	R/W	Determines video dma size to occur interrupt signal in ch3. ex) 704x240(window size)/4(32bit transaction size)x2(Luma&Croma) DMA size = 0x14A00	**0x00014A00/ 0x00018C00**
0x1CC	VID_DMA_SIZE4_REG	[31:0]	R/W	Determines video dma size to occur interrupt signal in ch4. ex) 704x240(window size)/4(32bit transaction size)x2(Luma&Croma) DMA size = 0x14A00	**0x00014A00/ 0x00018C00**
0x1D0	DMA4	[3]	R/W	Enable video DMA processing in ch4. 1 = enable, 0 = disable.	**0x0000000F**
	DMA3	[2]	R/W	Enable video DMA processing in ch3. 1 = enable, 0 = disable.	
	DMA2	[1]	R/W	Enable video DMA processing in ch2. 1 = enable, 0 = disable.	
	DMA1	[0]	R/W	Enable video DMA processing in ch1. 1 = enable, 0 = disable.	
0x1D4	VID_IRQ_MASK_REG	[6]	R/W	a video interrupt mask in ch4.	**0x00000055**
		[4]	R/W	a video interrupt mask in ch3.	
		[2]	R/W	a video interrupt mask in ch2.	
		[0]	R/W	a video interrupt mask in ch1.	
0x1D8	VID_IRQ_STS_REG	[6]	R	a video interrupt status in ch4.	**Read only**
		[4]	R	a video interrupt status in ch3.	
		[2]	R	a video interrupt status in ch2.	
		[0]	R	a video interrupt status in ch1.	
0x1F4	VID_CFG_REG	[0]	R/W	Enable data order to change CbYCrY~ or YCbYCr~ 0 = CbYCrY, first Croma second Luma. 1 = YCbYCr, first Luma second Croma.	**0x00000001**
0x1F8	VID_DMA_STS_REG	[6]	R	a video DMA status in ch4.	**Read only**
		[4]	R	a video DMA status in ch3.	
		[2]	R	a video DMA status in ch2.	
		[0]	R	a video DMA status in ch1.	

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x200	AUD_DMA_REG_A	[31:0]	R/W	assigns Voice base address a to main memory space.	**by cpu**
0x204	AUD_DMA_REG_B	[31:0]	R/W	assigns Voice base address b to main memory space.	**by cpu**
0x210	AUD_DMA_SIZE	[31:0]	R/W	Determines Voice DMA size to occur interrupt signal.	**0x00003E80**
0x220	AUD_DMA_CTRL	[0]	R/W	Enable Voice DMA processing. 1 = enable, 0 = disable.	**0x00000001**
0x224	AUD_INT_MASK	[0]	R/W	a Voice interrupt mask_a	**0x00000003**
		[1]	R/W	a Voice interrupt mask_b	
0x228	AUD_INT_STAT	[0]	R	a Voice interrupt_a status	**Read only**
		[1]	R	a Voice interrupt_b status	
0x240	I2C_P2_DIR_SDA	[13]	R/W	Determines direction of SDA_2(I2C Data2) Pin.	**0x00000000**
	I2C_P2_DIR_SCL	[12]	R/W	Determines direction of SCL_2(I2C_Clock2) Pin	
	I2C_P2_GET_SDA	[11]	R/W	Input from SDA_2(I2C Data2) Pin	
	I2C_P2_GET_SCL	[9]	R/W	Input from SCL_2(I2C_Clock2) Pin	
	I2C_P2_SET_SDA	[8]	R/W	Output from SDA_2(I2C Data2) Pin	
	I2C_P2_SET_SCL	[7]	R/W	Output from SCL_2(I2C_Clock2) Pin	
	I2C_P1_DIR_SDA	[5]	R/W	Determines direction of SDA_1(I2C Data1) Pin.	
	I2C_P1_DIR_SCL	[4]	R/W	Determines direction of SCL_1(I2C_Clock1) Pin	
	I2C_P1_GET_SDA	[3]	R/W	Input from SDA_1(I2C Data1) Pin	
	I2C_P1_GET_SCL	[2]	R/W	Input from SCL_1(I2C_Clock1) Pin	
	I2C_P1_SET_SDA	[1]	R/W	Output from SDA_1(I2C Data1) Pin	
	I2C_P1_SET_SCL	[0]	R/W	Output from SCL_1(I2C_Clock1) Pin	
0x264	IRQ_MASK	[0]	R/W	a total interrupt mask.	**0x00000001**
0x270	GPIO_DIRx	[31:8]	R/W	Determines a direction of GPIO1 ~ GPIO24(General Purpose I/O) pin. 1 = Input direction, 0 = Output direction	**by cpu**
		[7:0]	R/W	Reserved	**0x00**
0x274	GPIO_OUTx	[31:8]	R/W	GPIO1 ~ GPIO24 output	**by cpu**
		[7:0]	R/W		
0x278	GPIO_INx	[31:0]	R/W	GPIO1 ~ GPIO24 input	**by cpu**
		[7:0]	-	Reserved	**0x00**

6.4 Video Decoder Part

◆ Show Status of NVP1204 (Read Only)

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x500	NOVID4	[31]	R	Each Channel No Video Status. (0 : On Video , 1 : No Video)	Read Only
	NOVID3	[30]	R		
	NOVID2	[29]	R		
	NOVID1	[28]	R		
	BW4	[15]	R	Each Channel B/W Status. (0 : Color , 1 : B/W)	Read Only
	BW3	[14]	R		
	BW2	[13]	R		
	BW1	[12]	R		
	FSCLOCK4	[11]	R	Each Channel FSC Lock Status. (0 : FSC Unlocked , 1 : FSC Locked)	Read Only
	FSCLOCK3	[10]	R		
	FSCLOCK2	[9]	R		
	FSCLOCK1	[8]	R		
	AGCSTA4	[7]	R	Each Channel AGC Status. (0 : AGC Unstable , 1 : AGC Stable)	Read Only
	AGCSTA3	[6]	R		
	AGCSTA2	[5]	R		
	AGCSTA1	[4]	R		
	CMPSTA4	[3]	R	Each Channel CLAMP Status. (0 : Clamp Unstable , 1 : Clamp Stable)	Read Only
	CMPSTA3	[2]	R		
	CMPSTA2	[1]	R		
	CMPSTA1	[0]	R		

◆ Show Status of NVP1204 (Read Only)

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x504	LINE_NUM4	[31]	R	Each Channel Line Number Status. (0 : 525 Line , 1 : 625 Line)	Read Only
	LINE_NUM3	[30]	R		
	LINE_NUM2	[29]	R		
	LINE_NUM1	[28]	R		
	FLD4	[27]	R	Each Channel Field Status. (0 : ODD Field , 1 : EVEN Field)	Read Only
	FLD3	[26]	R		
	FLD2	[25]	R		
	FLD1	[24]	R		
	ADET4	[3]	R	Each Channel Voice Detect Status. (0 : No Voice , 1 : On Voice)	Read Only
	ADET3	[2]	R		
	ADET2	[1]	R		
	ADET1	[0]	R		

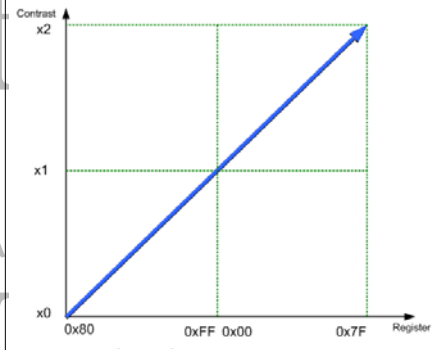
◆ Show Status of NVP1204 (Read Only)

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x518	DEV_ID	[7:0]	R	Device ID (0x74)	**Read Only**

◆ Show Status of NVP1204 (Read Only)

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x51C	REV_ID	[27:24]	R	Revision ID(0x0)	**Read Only**

◆ Registers to Control Comb Filter, Video Format and Luminance

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x520 **0x530** **0x540** **0x550**	BSF_MODE	[31:30]	R/W	Selects the filter to make primary separation of the brightness and color signals. 00 : Mode0 (1.3MHz Cut-off) 01 : Mode1 (1.88MHz Cut-off) 10 : Mode2 (2.65MHz Cut-off) 11 : Mode3 (2.5MHz Cut-off)	**0x4000AB02 / 0xBD00BE00**
	VIDEO_FORMAT	[28:24]	R/W	A register to determine the video standards of the input signal 00000 : NTSC-M,J 10001 : NTSC-4.43 11101 : PAL-B,D,G,H,I 10110 : PAL-M 11111 : PAL-Nc 10101 : PAL-60 Others : None	
	BRIGHTNESS	[23:16]	R/W	Brightness control, DC level of the Luma signal is adjustable up to -128 ~ +127. BRIGHTNESS consists of 2's Complements. 00000001 : +1 01111111 : +127 10000000 : -128 11111111 : -1	
	CONTRAST	[15:8]	R/W	Contrast control, Gain level of the Luma signal is adjustable up to x2. MSB represents an integral number while the rest the decimal fraction. 00000000 ≒ x1 01111111 ≒ x2 10000000 ≒ x0 11000000 ≒ x0.5 	
	HUE	[7:0]	R/W	Color HUE Control (360°/256) 00000000 : 0° 01000000 : 90° 10000000 : 180° 11111111 : 360°	

◆ Registers to Control Chrominance

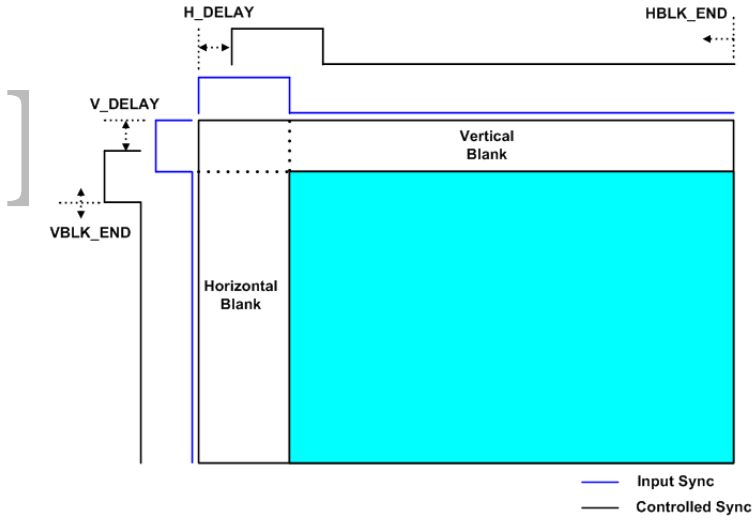
ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x524 0x534 0x544 0x554	SATURATION	[31:24]	R/W	Color Gain Control (Adjustable up to x2) 00000000 ≒ x0 10000000 ≒ x1 11000000 ≒ x1.5 11111111 ≒ x2	0x90000000 / 0x7E000000
	U_GAIN	[23:16]	R/W	U Gain Control (Adjustable up to x2) 00000000 ≒ x1 01111111 ≒ x2 10000000 ≒ x0 11000000 ≒ x0.5	
	V_GAIN	[15:8]	R/W	V Gain Control (Adjustable up to x2) 00000000 ≒ x1 01111111 ≒ x2 10000000 ≒ x0 11000000 ≒ x0.5	
	U_OFFSET	[7:4]	R/W	U/V OFFSET Control. (Adjustable up to ±7) U/V OFFSET consists of 2's Complements. 0001 : +1 0111 : +7 1000 : -8 1111 : -1	
	V_OFFSET	[3:0]	R/W		

◆ Registers to Control Luminance and Video Timing

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x528 0x538 0x548 0x558	**PED_ON**	**[31]**	**R/W**	Pedestal On/Off 0 : Off 1 : On	0x0A13A800 / 0x0B13C300
	Y_FIR_MODE	**[27:24]**	**R/W**	[27:26] : Peaking Filter control, Luma 3.5MHz frequency bandwidth amplification 00 : Bypass 01 : 2dB 10 : 3.5dB 11 : 6dB [25:24] : Low Pass Filter control 00 : Bypass 01 : 4.2MHz 10 : 5.6MHz 11 : 7.2MHz	
	HSYNC_INV	**[23]**	**R/W**	Horizontal Sync Signal Control, To inverse a phase of hsync.	
	VSYNC_INV	**[22]**	**R/W**	Vertical Sync Signal Control, To inverse a phase of vsync.	
	FLD_INV	**[21]**	**R/W**	Field Signal Control, To inverse a phase of field signal.	
	Y_DELAY	**[20:16]**	**R/W**	Y_DELAY Control, Controllable between 0 ~ 32.	
	H_DELAY	**[15:8]**	**R/W**	Register to determine the Horizontal start position of output image to Hsync extracted in analog input signal.	
	V_DELAY	**[7:0]**	**R/W**	Register to determine the Vertical start position of output image to Vsync extracted in analog input signal.	

◆ Registers to Control Video Timing

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x52C 0x53C	HBLK_END	[31:24]	R/W	Register to control Width of Horizontal Blanking, If user increments or decrements the value of this register, then the Active region is changed.	0x000A0000 / 0x000F0000
0x54C 0x55C	VBLK_END	[23:16]	R/W	Register to control Width of Vertical Blanking, If user increments or decrements the value of this register, then the Active region is changed	



◆ Registers to Control Analog Clamp

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x560	A_CMP_MODE1	[31:30]	R/W	Operation Mode1 of Analog Clamp 00 : Analog Clamp Off(NRT) 01 : Analog Clamp Test Mode 10 : Analog Clamp Test Mode 11 : Analog Clamp On(RT)	0xF080407C / 0xF080407C

◆ Registers to Control a Digital Front End

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x564	D_CMP_FZ	R/W	[31]	Digital Clamp On/Off Control 0 : Digital Clamp On 1 : Digital Clamp Off	0x9F002040 / 0x9F002040
	D_DMP_SPD	R/W	[25:24]	Digital Clamp Speed Selection 00 : Fastest 01 : Fast 10 : Middle 11 : Slow	
	D_AGC_FZ	R/W	[15]	Digital AGC On/Off Control 0 : Digital AGC On 1 : Digital AGC Off	

◆ Registers to Control a Digital Front End

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x568	SLICE_VALUE	[23:16]	R/W	Sync generation level Control	0x8050380F / 0x8050080F
	DFE_CORE_LVL	[15:12]	R/W	When the error value of the Digital AGC is smaller than DFE_CORE_LVL value, error value is transferred as "0". When it is larger than DFE_CORE_LVL value, the value deducting DFE_CORE_LVL from the error value is delivered	

◆ Registers to Control Chrominance

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x570	U_OFFSET2	[23:20]	R/W	U/V OFFSET2 Value is adjustable up to ±7. U/V OFFSET2 consists of 2's Complements	0x80238804 / 0x89238804
	V_OFFSET2	[19:16]	R/W		

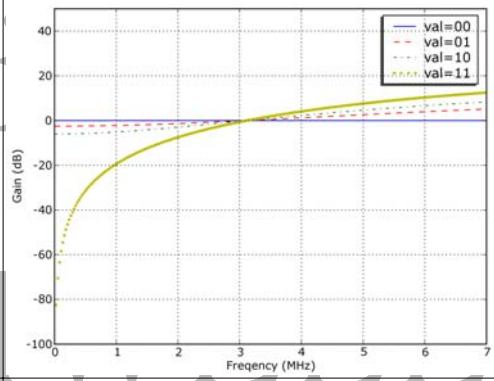
◆ Registers to Control Chrominance

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x574	FSC_LOCK_MODE	[23:20]	R/W	FSC error Tracing Mode 0xC : Normal (RT) 0xD : Fast(NRT) Others : Reserved	0x2ACCF02F / 0x2ACCF02F
	FSC_LOCK_SPD	[19:16]	R/W	FSC Locking Speed Control 0x5 : Fast(NRT) 0xC : Normal(RT) Others : Reserved	
	ACC_OFF	[7]	R/W	Continue to a constant gain value for chroma signal 0 : On 1 : Off	
	ACC_CORE_LVL	[5:4]	R/W	Adjust a coring level for ACC error 00 : 0 01 : 4 10 : 8 11 : 16	
	ACC_GAIN_SPD	[3:0]	R/W	1 step value applied to the ACC Gain Accumulator (ACC Accumulator 1 Step value = 4 * ACC_GAIN_SPD + 2)	

◆ Registers to Control No-video Detection and H/V Sharpness

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x578	FLD_DET_MODE	[23:22]	R/W	Select the method to create the field information that will be external output 00 : Middle 01 : Slow 10 : Fast 11 : Fastest	0x57431088 / 0x57431088
	NOVID_DET_B	[19:16]	R/W	Select Condition for No video detection, High Active [19] : wpd_novideo [18] : If Vertical sync don't exist, turn on the NOVID signal [17] : If Width of detected sync is narrower than video standard, turn on the NOVID signal [16] : If the input video is not detected sync, turn on the NOVID signal	
	NOVID_SPD	[15:8]	R/W	Novideo Sensitivity Control 0x00 → 0x3F : more insensitive 0x40 → 0xFF : Reserved	
	H_SHARPNESS	[7:4]	R/W	Select the H_SHARPNESS Value to calculate the Luma information. It consists of four bits in total. MSB represents an integral number while the rest the decimal fraction. 0000 : 0 0100 : x0.5 1000 : x1 1111 : x2	
	V_SHARPNESS	[3:0]	R/W	Select the V_SHARPNESS Value to calculate the Luma information. It consists of four bits in total. MSB represents an integral number while the rest the decimal fraction. 0000 : 0 0100 : x0.5 1000 : x1 1111 : x2	

◆ Registers to Control Chrominance

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x57C	PAL_CM_OFF	[31]	R/W	PAL Compensation On/Off 0 : PAL Compensation applied 1 : PAL Compensation no applied	0x82630100 / 0x01630100
	IF_FIR_SEL	[30:28]	R/W	IF Filter drive mode selected 000 : Bypass 001 : mode1 010 : mode2 others : mode3 	
	CLPF_SEL	[25:24]	R/W	Color low pass filter Selection for Demodulation 00 : Bypass 01 : 0.6MHz Cut Off 10 : 1.0MHz Cut Off 11 : 1.2MHz Cut Off	
	CTI_CORE	[23:22]	R/W	Adjust coring level for error element of CTI 00 : 0 01 : 3 10 : 6 11 : 9	
	CTI_GAIN	[21:20]	R/W	Adjust gain level for CTI 00 → 11 : more Larger gain	

◆ Registers to Control Output Data Range

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x580	DATA_OUT_MODE	[3:0]	R/W	It limits a level of output data, can change signals of Cb and Cr 0000 : Y(16~235), Cb(16~240), Cr(16~240) 0001 : Y(1~254), Cb(1~254), Cr(1~254) 0010 : Y(0~255), Cb(0~255), Cr(0~255) 0011 : Cb/Cr Change, Y(16~235), Cb(16~240), Cr(16~240) 0100 : Cb/Cr Change, Y(1~254), Cb(1~254), Cr(1~254) 0101 : Cb/Cr Kill, Y(16~235) 0110 : Cb/Cr Kill, Y(1~254) Others : Background color output	0x80000081 / 0x80000081

◆ Registers to Control Digital Front-End and White Peak Detection

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x58C	SLICE_MD	[23:16]	R/W	Slice Mode Selection 0x30 : Normal Mode(RT) 0x32 : Fast Mode(NRT) (SLICE_VALUE(0x568[23:16]x2)	0x0030B801 / 0x0030D801

◆ Registers to Control White Peak Detection

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x590	WPD_ON	[15]	R/W	White Peak Detection Operation ON/OFF 0 : OFF 1 : ON	**0x060611B9 / 0x060611B9**

◆ Registers to Control Color Killer

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x598	V_LOC_SPD	[31:24]	R/W	V Tracing Speed Control 0x50 : Normal (RT) 0x51 : Fast (NRT)	**0x5051B513 / 0x5051A813**
	CKILL4	[15:12]	R/W	[3] : Color kill mode 0 : Not Y/C separation 1 : Color kill after Y/C separation	
	CKILL3	[11:8]	R/W	[2:0] : Color kill control 000 : Burst Amplitude 10% Under & FSC Unlock 001 : Burst Amplitude 5% Under & FSC Unlock 010 : Burst Amplitude 10% Under 011 : Burst Amplitude 5% Under 100, 101 : Always color on 110, 111 : Always color off	
	CKILL2	[7:4]	R/W		
	CKILL1	[3:0]	R/W		

◆ Registers to Control Video Analog Front End

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x5D4	PD1	[15]	R/W	Video ADC Power Down Mode 0 : Normal Operation 1 : Power Down Mode	**0xFF550000 / 0xFF550000**
	PD2	[14]	R/W		
	PD3	[13]	R/W		
	PD4	[12]	R/W		

◆ Registers to Control Video Analog Front End

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x5D8	G_SEL1	[31:24]	R/W	Video PGA Gain Control 00111111 : Gain x1 (0dB) 10101001 : Gain x2 (6dB) 11111110 : Gain x4 (12dB)	**0x00000000 / 0x00000000**
	G_SEL2	[23:16]	R/W		
	G_SEL3	[15:8]	R/W		
	G_SEL4	[7:0]	R/W		

◆ Registers to Control Analog Clamp

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x5E0	A_CMP_MODE2	[31:00]	R/W	Operation Mode2 of Analog Clamp 0x00000000 : Analog Clamp On (NRT) 0xFFFFFFFF : Analog Clamp Off (RT)	**0x00000000 / 0x00000000**

◆ Registers to Control Voice/Video ADC Sampling Clock

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x5E8	A_ADC_CLK_SEL	[9]	R/W	Voice ADC Sampling Clock Inversion 0 : 0º Phase 1 : 180º Phase	0x00000300 / 0x00000300
	V_ADC_CLK_SEL	[4]	R/W	Video ADC Sampling Clock Inversion 0 : 0º Phase 1 : 180º Phase	

◆ Registers to Control Video Scaler

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x610	BLK_PKG1	[31:0]	R/W	Data insertion in the section of H or V Blank. [31:24] : Cb [23:16] : Y1 [15:8] : Cr [7:0] : Y2	0x80108010 / 0x80108010
0x614	BLK_PKG2				
0x618	BLK_PKG3				
0x61C	BLK_PKG4				

◆ Registers to Control Video Scaler

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x620 0x624	H_DELx	[27:24]	R/W	When input is 704 pixel, decider H start position(0~15)	0x00100000 / 0x00100000
0x628 0x62C	H_DTO_x	[20:0]	R/W	For Horizontal Direction, decide Ratio of Scale. NTSC/PAL : H scale = (H_DTO_x / 0x00_10_00_00) x 720	

◆ Registers to Control Video Scaler

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x630 0x634	BLK_OPERx	[24]	R/W	Change data of the V or H Blank section. Existing 0x80, 0x10, 0x80 and 0x10 stream is changed to BLK_PKG register value as below. 0 : Existing 0x80, 0x10 data stream.. 1 : Change to BLK_PKGx (0x610~0x61C register) value.	0x00100000 / 0x00100000
0x638 0x63C	V_DTO_x	[20:0]	R/W	For Vertical Direction, decide to V Scaled size. NTSC : V Scaled size = (V_DTO / 0x00100000) x 240 PAL : V Scaled size = (V_DTO / 0x00100000) x 288	

◆ Registers to Control Video Scaler

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x640	UP_4	[31]	R/W	According to only 720 pixel input, stretch the display size to 720-size. 0 : No Expand 1 : Expand	0x000FFF00 / 0x000FFF00
	UP_3	[30]			
	UP_2	[29]			
	UP_1	[28]			
	IDON_4	[27]		Decide if CH ID is inserted or not 0 : No Channel ID Insertion 1 : Channel ID Insertion	
	IDON_3	[26]			
	IDON_2	[25]			
	IDON_1	[24]			
	SYNC_ORG_4	[23]		Decide H blank length between standard and variable one based on scale ratio. 0 : Changed by a scale ratio. 1 : No changed by a scale ratio	
	SYNC_ORG_3	[22]			
	SYNC_ORG_2	[21]			
	SYNC_ORG_1	[20]			
	SCALE_SEL_4	[19]		Decide output between scale data and non-scale data which is same as bypass 0 : bypass an input data. 1 : output a scaled data	
	SCALE_SEL_3	[18]			
	SCALE_SEL_2	[17]			
	SCALE_SEL_1	[16]			
	H_BYPS_4	[15]		According to H direction, decide if it is treated as cubic convolution or bypass. 0 : Cubic Convolution 1 : Bypass	
	H_BYPS_3	[14]			
	H_BYPS_2	[13]			
	H_BYPS_1	[12]			
	V_BYPS_4	[11]		According to V direction, decide if it is treated as cubic convolution or bypass 0 : Cubic Convolution 1 : Bypass	
	V_BYPS_3	[10]			
	V_BYPS_2	[9]			
	V_BYPS_1	[8]			
	SUB_SAM_4	[3]		When you scale under 0.5, select between average method and sampling one which is extracting one by one. (But when you scale 0.5~1, set it only sampling(1)) 0 : Average 1 : Sampling	
	SUB_SAM_3	[2]			
	SUB_SAM_2	[1]			
	SUB_SAM_1	[0]			

◆ Registers to Control Voice Decoder

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x6A8	ADET_FILT	[18:16]	R/W	Set the time to decide the existence of AIN1-4 voice signals. 0 : 16 sec. 1 : 15 sec. 2 : 9 sec. 3 : 5 sec. 4 : 3 sec. 5 : 1 sec. 6 : 0.6 sec. 7 : 0.5 sec.	0x000010F0
	ADET_MODE	[15]		Select the method to decide the existence of AIN1-4 voice signals. 0 : Absolute amplitude detection mode 1 : Differential amplitude detection mode	
	EN_RESET	[14]		Initialize to voice processing (**High Active**)	
	ADET_1	[7]		Enable bit voice signal existence checking function for AIN1-4. 0 : Don't use this function 1 : Use this function	
	ADET_2	[6]			
	ADET_3	[5]			
	ADET_4	[4]			

◆ Registers to Control Voice Decoder

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x6AC	ADET_TH_1	[31:28]	R/W	Set the threshold value for voice signal existence of AIN1-4	0xAAAA0000
	ADET_TH_2	[27:24]			
	ADET_TH_3	[23:20]			
	ADET_TH_4	[19:16]			

◆ Registers to Control Voice Input Gain

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x6B4	AIGAIN_1	[31:28]	R/W	Control the gain of analog voice input AIN1 ~ 8 0 : Mute 1 : 0.25 2 : 0.31 3 : 0.38 4 : 0.5 5 : 0.63 6 : 0.75 7 : 0.88 8 : 1.0 9 : 1.25 10 : 1.5 11 : 1.75 12 : 2.0 13 : 2.25 14 : 2.5 15 : 2.75	0x88880000
	AIGAIN_2	[27:24]			
	AIGAIN_3	[23:20]			
	AIGAIN_4	[19:16]			

7. Electrical characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
1.8V Digital Power Supply Voltage	V_{POWER1}	1.65	1.8	1.95	V
1.8V Analog Power Supply Voltage	V_{DDA1}	1.65	1.8	1.95	V
3.3V Digital Power Supply Voltage	V_{POWER2}	3.0	3.3	3.6	V
Voltage on Any 1.8V input pins	V_{PIN1}	1.65	1.8	1.95	V
Voltage on Any 3.3V input pins	V_{PIN2}	3.0	3.3	3.6	V
Voltage on Any 5V input pins	V_{PIN5}	4.5	5	5.5	V
Storage Temperature	V_S	-40	-	125	℃
Junction Temperature	V_J	-40	-	125	℃
Vapor phase soldering (15 Sec)	V_{VSOL}	-	-	220	℃

7.2 Recommended Operating Condition

Parameter	Symbol	Min	Typ	Max	Unit
1.8V Digital Power Supply Voltage	V_{POWER1}	1.65	1.8	1.95	V
1.8V Analog Power Supply Voltage	V_{DDA1}	1.65	1.8	1.95	V
3.3V Digital Power Supply Voltage	V_{POWER2}	3.0	3.3	3.6	V
Ambient operating temperature	V_A	-10	-	80	℃

7.3 DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	VSSI-0.3	-	$0.3V_{POWER}$	V
Input High Voltage	V_{IH}	$0.7V_{POWER}$	-	V_{POWER}+0.3	V
Input Low Current (V_{IN} = VSS)	I_{IL}	-	-	-10	uA
Input High Current (VIN = V_{POWER})	I_{IH}	-	-	10	uA
Input Capacitance (f = 1Mhz, V_{IN} = 2.4V)	C_{IN}	-	-	10	pF
Output Low Voltage (I_{OL} = 8.0mA)	V_{OL}	-	-	0.4	V
Output High Voltage (I_{OH} = 11.9mA)	V_{OH}	2.4	-	V_{POWER}	V
Three-State Output Leakage Current	I_{OZ}	-	-	±10	uA
Output Capacitance	C_{OUT}	-	-	10	pF

7.4 AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Current					
1.8V Supply Current	I_{DD1}	-	TBD	-	mA
3.3V Supply Current	I_{DD2}	-	TBD	-	mA
PCI Clock					
PCI_CLK frequency	f_{CLK33}	-	33.0	-	MHz
PCI_CLK duty cycle	f_{DUTY}	45	-	55	%
PCI_CLK pulse width low	t_{PWL_CLK54}	15.0	-	-	nsec
PCI_CLK pulse width high	t_{PWH_CLK54}	15.0	-	-	nsec
SYSTEM Clock					
SYS_CLK frequency	f_{CLK27}	-	27.0	-	MHz
SYS_CLK duty cycle	f_{DUTY}	45	-	55	%
SYS_CLK pulse width low	t_{PWL_CLK54}	18.0	-	-	nsec
SYS_CLK pulse width high	t_{PWH_CLK54}	18.0	-	-	nsec
Host Interface Pins					
P_SCL frequency	f_{SCL}	-	-	6	PCI_CLK
P_SCL minimum pulse width low	t_{PWL_SCL}	6	-	-	PCI_CLK
P_SCL minimum pulse width high	t_{PWH_SCL}	4	-	-	PCI_CLK
P_SCL to P_SDA setup time	t_{IS_SDA}	2	-	-	PCI_CLK
P_SCL to P_SDA hold time	t_{IH_SDA}	2	-	-	PCI_CLK
P_SCL to P_SDA delay time	t_{OD_SDA}	-	-	6	PCI_CLK
P_SCL to P_SDA hold time	t_{OH_SDA}	3	-	-	PCI_CLK

8. System Application

8.1 Recommended NTSC Register

ADDRESS	NTSC
0x100	by cpu
0x104	by cpu
0x108	by cpu
0x120	by cpu
0x124	by cpu
0x128	by cpu
0x140	by cpu
0x144	by cpu
0x148	by cpu
0x160	by cpu
0x164	by cpu
0x168	by cpu
0x190	0x0002C001
0x194	0x0002C000
0x198	0x0002C000
0x19C	0x0002C000
0x1A0	0x00008000
0x1A4	0x002080AD
0x1A8	0x00000000
0x1AC	0x00000000
0x1B0	0x00000000
0x1B4	0x00000000
0x1B8	0x00000000
0x1BC	0x00000000
0x1C0	0x00014A00
0x1C4	0x00014A00
0x1C8	0x00014A00
0x1CC	0x00014A00
0x1D0	0x0000000F
0x1D4	0x00000055
0x1D8	read only
0x1F4	0x00000001
0x1F8	read only

ADDRESS	NTSC
0x200	by cpu
0x204	by cpu
0x210	0x00003E80
0x218	0x00200000
0x220	0x00000001
0x224	0x00000003
0x228	read only
0x240	0x00000000
0x264	0x00000001
0x268	real only
0x270	by gpio
0x274	by gpio
0x278	by gpio

ADDRESS	NTSC	
	RT	NRT
0x500	read only	
0x504	read only	
0x508	read only	
0x50C	read only	
0x510	read only	
0x514	read only	
0x518	read only	
0x51C	read only	
0x520	0x4000AB02	
0x524	0x90000000	
0x528	0x0A13A800	
0x52C	0x000A0000	
0x530	0x4000AB02	
0x534	0x90000000	
0x538	0x0A13A800	
0x53C	0x000A0000	
0x540	0x4000AB02	
0x544	0x90000000	
0x548	0x0A13A800	
0x54C	0x000A0000	
0x550	0x4000AB02	
0x554	0x90000000	
0x558	0x0A13A800	
0x55C	0x000A0000	
0x560	0xF080407C	0x0080407C
0x564	0x9F002040	0x1C00A040
0x568	0x8050380F	0x8042380F
0x56C	0x0C01150A	
0x570	0x80238804	
0x574	0x2ACCF02F	0x2AD5F0AF
0x578	0x57431088	0x57833F80
0x57C	0x82630100	0x82530100
0x580	0x80000001	
0x584	0x01000000	
0x58C	0x0030B801	0x0032B801
0x590	0x060611B9	
0x594	0xB2050028	
0x598	0x50003333	51003333
0x5A0	0x00000000	
0x5A4	0x76543210	
0x5A8	0xFEDCBA98	
0x5AC	0x76543210	
0x5B0	0xFEDCBA98	
0x5B4	0x00000000	
0x5B8	0x00000000	
0x5BC	read only	
0x5C0	read only	
0x5C4	read only	
0x5D0	0x05330000	
0x5D4	0xFF550000	
0x5D8	0x45454545	
0x5DC	0xFFAAAA55	
0x5E0	0xFFFF0000	0x00000000
0x5E4	0x0F0F0F0F	
0x5E8	0x00000300	

ADDRESS	NTSC
0x610	0x80108010
0x614	0x80108010
0x618	0x80108010
0x61C	0x80108010
0x620	0x00100000
0x624	0x00100000
0x628	0x00100000
0x62C	0x00100000
0x630	0x00100000
0x634	0x00100000
0x638	0x00100000
0x63C	0x00100000
0x640	0x000FFF00
0x644	0xFFFFFFB1
0x64C	0x00003333
0x650	0x88880009
0x654	0x80808080
0x658	0x49494949
0x65C	0x37373737
0x660	0x7B7B7B7B
0x664	0x58585858
0x668	0x08080808
0x66C	0x00550000
0x670	0x000000F0
0x674	0x00000000
0x678	0x11111111
0x67C	0x00000000
0x680	0x00000000
0x684	0x00000000
0x688	0x80000000
0x68C	0x13131313
0x690	0x03030303
0x694	0x22222222
0x698	0x00000000
0x69C	0x51B551B5
0x6A0	0x51B551B5
0x6A4	0x69780303
0x6A8	0x000010FF
0x6AC	0xAAAA0000
0x6B0	0x02000200
0x6B4	0x88880000
0x6C0	0x00000000
0x6C4	0x00000000
0x6C8	0x00000000
0x6CC	0x00000000
0x6D0	0x00000000
0x6D4	0x00000000
0x6D8	0x00000000
0x6DC	0x00000000
0x6E0	0x00000000
0x6E4	0x00000000

8.2 Recommended PAL Register

ADDRESS	PAL
0x100	by cpu
0x104	by cpu
0x108	by cpu
0x120	by cpu
0x124	by cpu
0x128	by cpu
0x140	by cpu
0x144	by cpu
0x148	by cpu
0x160	by cpu
0x164	by cpu
0x168	by cpu
0x190	0x0002C001
0x194	0x0002C000
0x198	0x0002C000
0x19C	0x0002C000
0x1A0	0x00008000
0x1A4	0x002080AD
0x1A8	0x00000000
0x1AC	0x00000000
0x1B0	0x00000000
0x1B4	0x00000000
0x1B8	0x00000000
0x1BC	0x00000000
0x1C0	0x00018C00
0x1C4	0x00018C00
0x1C8	0x00018C00
0x1CC	0x00018C00
0x1D0	0x0000000F
0x1D4	0x00000055
0x1D8	read only
0x1F4	0x00000001
0x1F8	read only

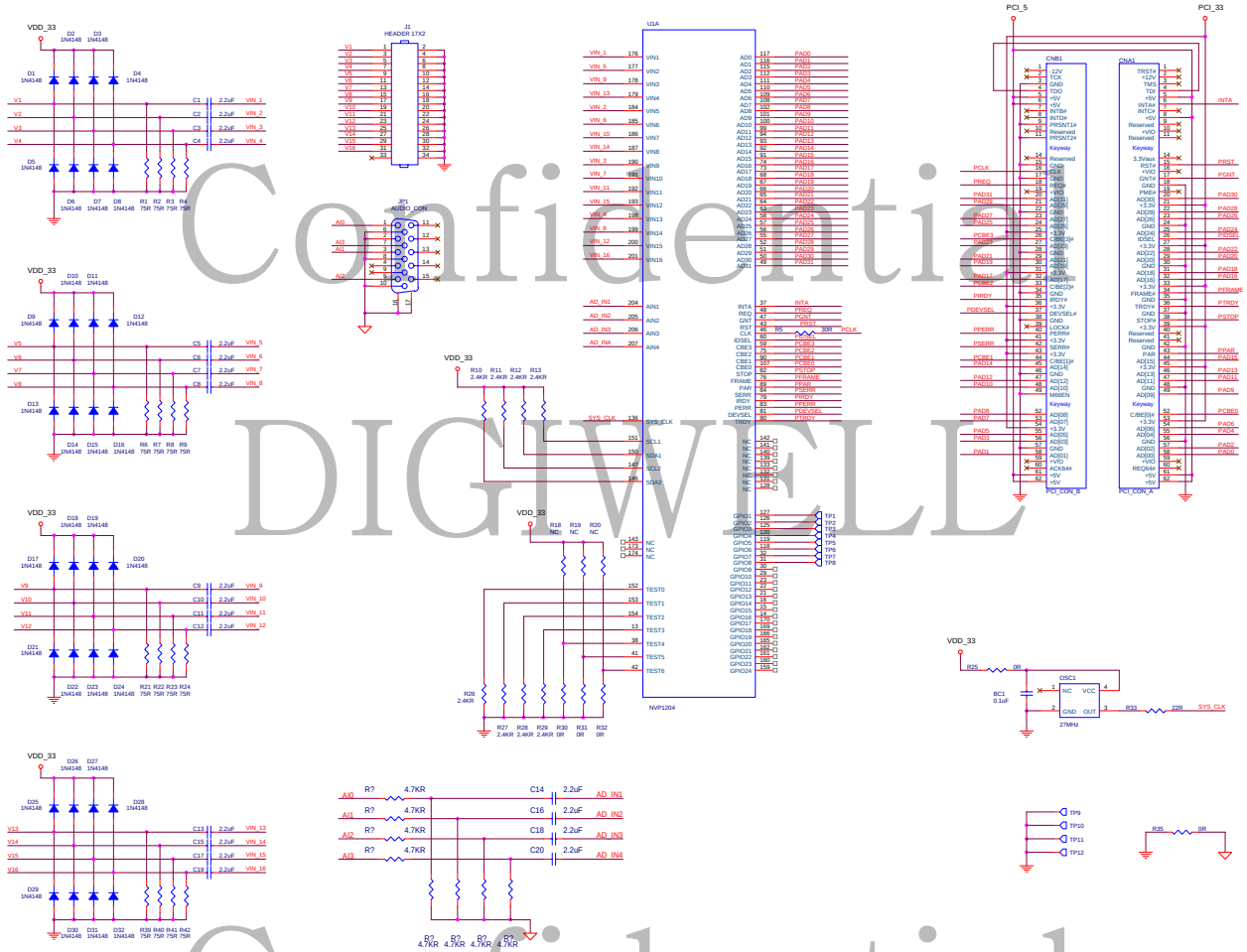
ADDRESS	PAL
0x200	by cpu
0x204	by cpu
0x210	0x00003E80
0x218	0x00200000
0x220	0x00000001
0x224	0x00000003
0x228	read only
0x240	0x00000000
0x264	0x00000001
0x268	read only
0x270	by gpio
0x274	by gpio
0x278	by gpio

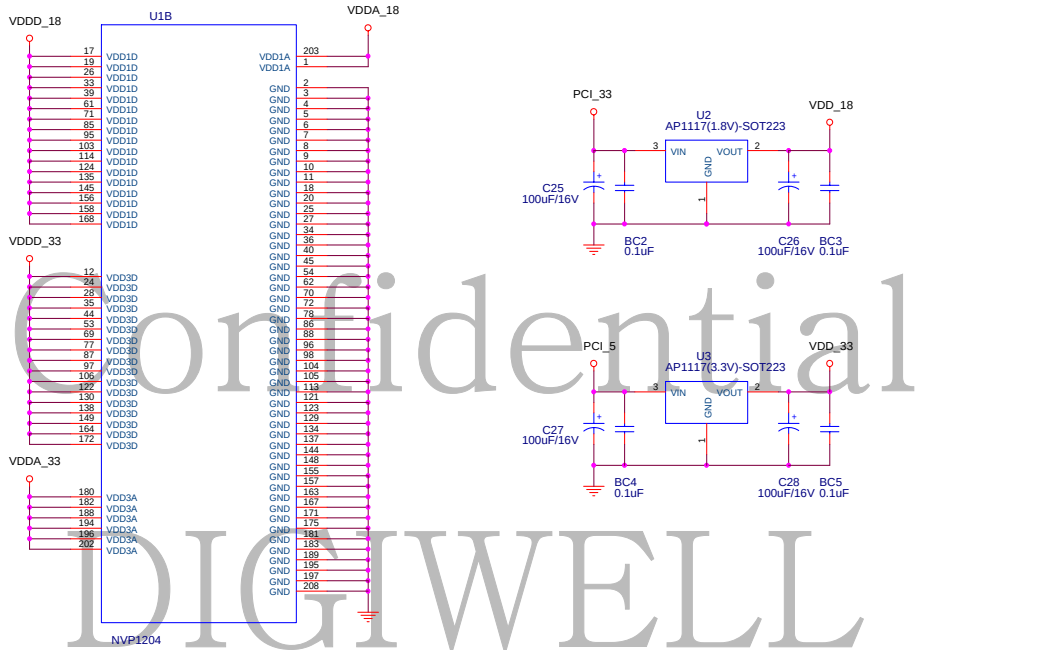
ADDRESS	PAL	
	RT	NRT
0x500	read only	
0x504	read only	
0x508	read only	
0x50C	read only	
0x510	read only	
0x514	read only	
0x518	read only	
0x51C	read only	
0x520	0xBD00BE00	
0x524	0x7E000000	
0x528	0x0B13C300	
0x52C	0x000F0000	
0x530	0xBD00BE00	
0x534	0x7E000000	
0x538	0x0B13C300	
0x53C	0x000F0000	
0x540	0xBD00BE00	
0x544	0x7E000000	
0x548	0x0B13C300	
0x54C	0x000F0000	
0x550	0xBD00BE00	
0x554	0x7E000000	
0x558	0x0B13C300	
0x55C	0x000F0000	
0x560	0xF080407C	0x0040807C
0x564	0x9F002040	0x1C00A040
0x568	0x8050080F	0x8042080F
0x56C	0x0C01150A	
0x570	0x89238804	
0x574	0x2ACCF02F	0x2AD5F0AF
0x578	0x57431088	0x57833F80
0x57C	0x01630100	0x01530100
0x580	0x80000081	
0x584	0x01000000	
0x58C	0x0030B801	0x0032B801
0x590	0x060611B9	
0x594	0xB2050028	
0x598	0x50003333	0x51003333
0x5A0	0x00000000	
0x5A4	0x76543210	
0x5A8	0xFEDCBA98	
0x5AC	0x76543210	
0x5B0	0xFEDCBA98	
0x5B4	0x00000000	
0x5B8	0x00000000	
0x5BC	read only	
0x5C0	read only	
0x5C4	read only	
0x5D0	0x05330000	
0x5D4	0xFF550000	
0x5D8	0x45454545	
0x5DC	0xFFAAAA55	
0x5E0	0xFFFF0000	0x00000000
0x5E4	0x0F0F0F0F	
0x5E8	0x00000300	

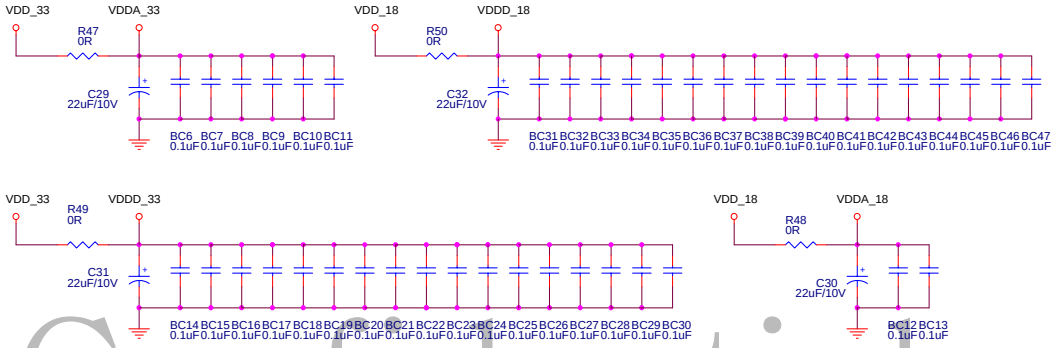
ADDRESS	PAL
0x610	0x80108010
0x614	0x80108010
0x618	0x80108010
0x61C	0x80108010
0x620	0x00100000
0x624	0x00100000
0x628	0x00100000
0x62C	0x00100000
0x630	0x00100000
0x634	0x00100000
0x638	0x00100000
0x63C	0x00100000
0x640	0x000FFF00
0x644	0xFFFFFFB1
0x64C	0x00003333
0x650	0x88880009
0x654	0x80808080
0x658	0x49494949
0x65C	0x37373737
0x660	0x7B7B7B7B
0x664	0x46464646
0x668	0x08080808
0x66C	0x00550000
0x670	0x000000F0
0x674	0x00000000
0x678	0x11111111
0x67C	0x00000000
0x680	0x00000000
0x684	0x00000000
0x688	0x80000000
0x68C	0x13131313
0x690	0x03030303
0x694	0x22222222
0x698	0x00000000
0x69C	0x51B551B5
0x6A0	0x51B551B5
0x6A4	0x69780000
0x6A8	0x000010FF
0x6AC	0xAAAA0000
0x6B0	0x02000200
0x6B4	0x88880000
0x6C0	0x00000000
0x6C4	0x00000000
0x6C8	0x00000000
0x6CC	0x00000000
0x6D0	0x00000000
0x6D4	0x00000000
0x6D8	0x00000000
0x6DC	0x00000000
0x6E0	0x00000000
0x6E4	0x00000000

8.3 Circuit Configuration

8.3.1 4channel Real Time / 16channel Non-Real Time Mode

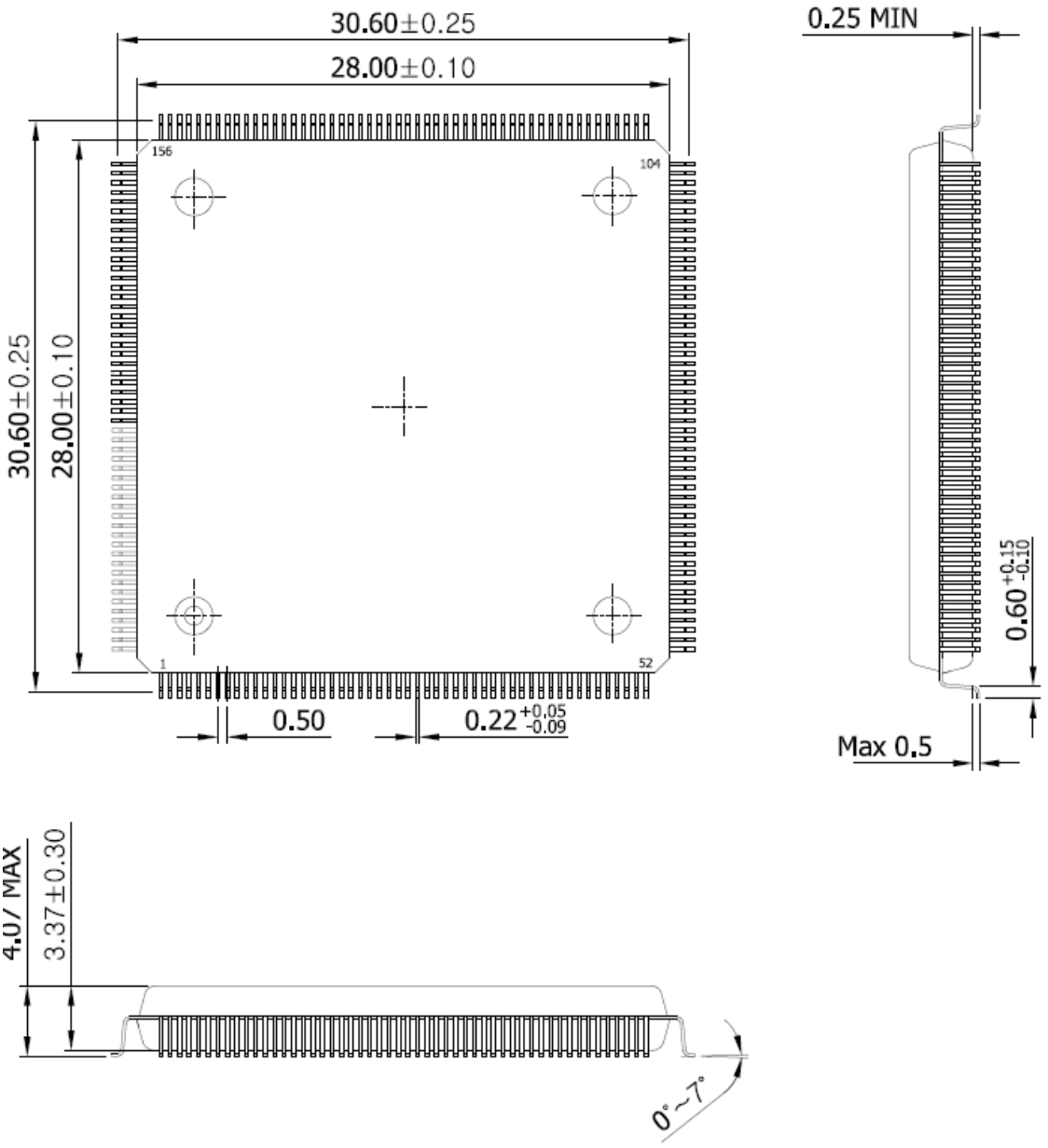






8.4 Package Information

Dimensions in millimeters



9. Revision History

REV	Date	Description
Preliminary 0.1	2009.09.01.	· Generated
Preliminary 1.0	2009.12.09.	· Modified 2.9 Scale Ratio numerical formula & Table 2.3 · Modified and Supplemented Register (Relate to NRT Operation) 5. Register Map , 6. Register Descriptions , 8. Recommended Register Values

10. Contact Information

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