NVP1208

Multi-Channel Real Time Video & Audio capture device

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Multi-Channel Real Time Video & Audio capture device

: NVP1208 supports multi-channel(up to 17ch - Record 16ch / Live 1ch) real time video and audio capture via PCI 33MHz Bus. It includes 4 channel Video decoder / 4 channel Audio processor and supports external 12ch Video/Audio digital input interface. NVP1208 digitizes and decodes NTSC/PAL video signal, transfers multi-channel video data to via PCI 33MHz bus. It also transfer PCM digital audio signal up to 16ch and support audio mute detection and volume control. NVP1208 includes high performance DMA controller that fully utilizes the PCI 33MHz Bandwidth.

Features

Video Decoder

· Accept NTSC-M/J/4.43 and PAL-B/G/H/I/D/K/L/M/N/Nc/60
- Robust Sync detection for weak and non-standard signals
- Fully programmable Static or Automatic gain control
· Accept Analog CVBS up to 4 channel
· High-performance 3H/5H 2D adaptive comb filter
· Programmable peaking filter for Luminance
· Programmable Vertical Peaking filter
· CTI (Chrominance Transient Improvement)
· Color compensation for PAL
· IF compensation filter
· Robust No-video detection
· Programmable brightness, contrast, saturation and hue

Video Scaler

· High quality horizontal & vertical filtered scaling with arbitrary scale down ratio
· Support various frame resolution
-. NTSC : 720x240, 704x240, 640x240, 320x240
-. PAL : 720x288, 704x288, 640x288, 720x240, 704x240, 640x240

Ordering Information

Device	Package	Temperature Range
NVP1208	208QFP	-10 ~ 80℃

Audio Processor

· Accept analog audio input up to 4 channel
· Built in a strong 10bit Pipe-Line ADC for noise
· Support Linear PCM
· Support 16bit/8bit, 8k/16k sampling
· Built in Input Volume Controller
· Built in Mute Detector

PCI

· Built in Video/Audio DMA controller
· Video capture
Input : 4ch CVBS +
12ch for Record & 3ch in 12ch for Live
Digital BT.656
Output : 16ch record + 1ch Live
· Audio capture
Input : 4ch Analog audio + 12ch Digital Cascade
Output : Linear PCM
· Fully PCI Rev.2.2-3.0 compliant
· Support YUV 4:2:2, 4:1:1, 4:2:0, Y only format
· Support 33MHz PCI Clock
· Built in PCI Test pattern generator for Hardware Debugging

MISC.

· Support Auxiliary 24 GPIO port
· Support two I2C Master
· 1.8V(Core), 3.3V(I/O)
· 5V tolerant I/O
· Package (208-QFP, 28mm x 28mm, 0.5P)

Applications

-. PC Based on Video Security System

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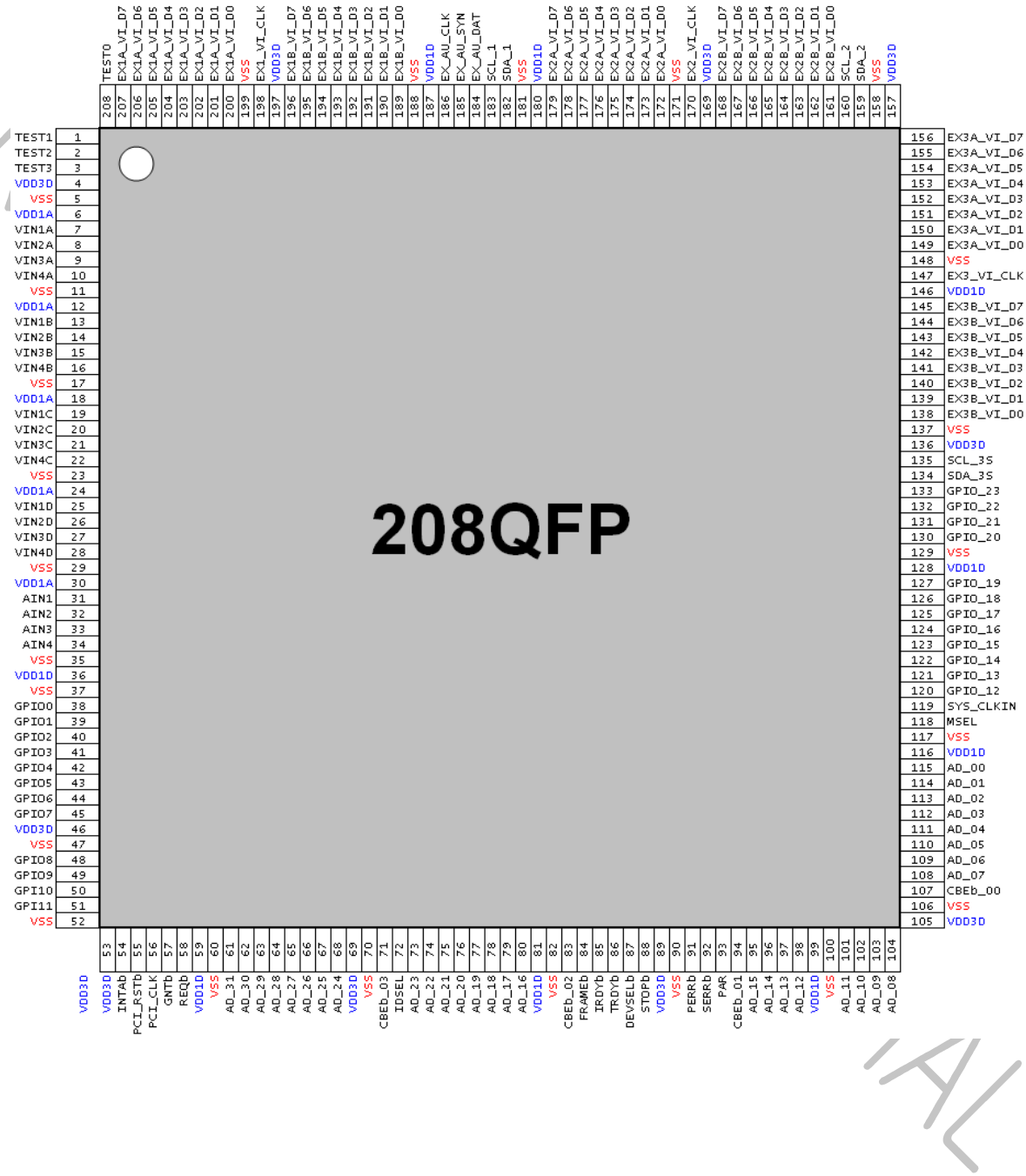
1. Pin Information

1.1 Pin Assignments



1.2 Pin Description

Pin name	Number	Type	Description
Analog Video Interface (16 Pins)			
VIN1A, VIN2A, VIN3A, VIN4A, VIN1B, VIN2B, VIN3B, VIN4B, VIN1C, VIN2C, VIN3C, VIN4C, VIN1D, VIN2D, VIN3D, VIN4D	7, 8, 9, 10, 13, 14, 15, 16, 19, 20, 21, 22, 25, 26, 27, 28	AI	Analog Video Inputs
Analog Audio Interface (4Pins)			
AIN1, AIN2, AIN3, AIN4	31, 32, 33, 34	AI	Analog Voice Inputs
PCI Interface (51 Pins)			
PCI_CLK	56	I	PCI Clock (33MHz)
PCI_RSTb	55	I	PCI global Reset (Active Low)
INTAb	54	O	PCI Interrupt output (Active Low)
REQb	58	O	PCI Bus request signal (Active Low)
GNTb	57	I	PCI Bus grant signal (Active Low)
IDSEL	72	I	PCI initialization device select signal
AD_31, AD_30, AD_29, AD_28, AD_27, AD_26, AD_25, AD_24, AD_23, AD_22, AD_21, AD_20, AD_19, AD_18, AD_17, AD_16, AD_15, AD_14, AD_13, AD_12, AD_11, AD_10, AD_09, AD_08, AD_07, AD_06, AD_05, AD_04, AD_03, AD_02, AD_01, AD_00,	61, 62, 63, 64 65, 66, 67, 68 73, 74, 75, 76, 77, 78, 79, 80, 95, 96, 97, 98, 101, 102, 103, 104, 108, 109, 110, 111, 112, 113, 114, 115	I/O	Bi-directional PCI I/O pins transfer both address and data signals
CBEb_03, CBEb_02, CBEb_01, CBEb_00	71, 83, 94, 107	I/O	Bi-directional PCI I/O pins transfer both bus command and byte enable signals (Active Low)
FRAMEb	84	I/O	Bi-directional PCI cycle frame signal (Active Low)
IRDYb	85	I/O	Bi-directional PCI initiator ready signal (Active Low)
TRDYb	86	I/O	Bi-directional PCI target ready signal (Active Low)
DEVSELb	87	I/O	Bi-directional PCI device select signal (Active Low)
STOPb	88	I/O	Bi-directional PCI stop signal (Active Low)
PAR	93	I/O	Bi-directional PCI parity signal
SERRb	92	O	Report address parity error
PERRb	91	I/O	Report data parity error
MSEL	118	I	Test Purpose Only (Connect to GND)
I2C Interface (6Pins)			
SCL_1, SCL_2	183, 160	I/O	Serial Clock 1, Serial Clock 2 for I2C Master
SDA_1, SDA_2	182, 159	I/O	Serial Data 1, Serial Data 2 for I2C Master
SCL_3	135	I/O	Test Serial Clock for I2C Slave
SDA_3	134	I/O	Test Serial Data for I2C Slave
System Clock (1 Pins)			
SYS_CLK	119	I	System Clock (27MHz/54MHz/108MHz)

Pin name	Number	Type	Description
External Digital Video Interface (51Pins)			
EX1A_07, EX1A_06, EX1A_05, EX1A_04, EX1A_03, EX1A_02, EX1A_01, EX1A_00	207, 206, 205, 204, 203, 202, 201, 200	I	BT.656 Data for Record from External 1st Video Decoder (#5ch~#8ch @108MHz)
EX1B_07, EX1B_06, EX1B_05, EX1B_04, EX1B_03, EX1B_02, EX1B_01, EX1B_00	196, 195, 194, 193, 192, 191, 190, 189	I	BT.656 Data for Live from External 1st Video Decoder (one ch in #5ch~#/8ch @27MHz)
EX1_VI_CLK	198	I	Clock Input from External 1st Video Decoder (@54MHz/108MHz)
EX2A_07, EX2A_06, EX2A_05, EX2A_04, EX2A_03, EX2A_02, EX2A_01, EX2A_00	179, 178, 177, 176, 175, 174, 173, 172	I	BT.656 Data for Record from External 2nd Video Decoder (#9ch~#12ch @108MHz)
EX2B_07, EX2B_06, EX2B_05, EX2B_04, EX2B_03, EX2B_02, EX2B_01, EX2B_00	168, 167, 166, 165, 164, 163, 162, 161	I	BT.656 Data for Live from External 2nd Video Decoder (one ch in #9ch~#/12ch @27MHz)
EX2_VI_CLK	170	I	Clock Input from External 2nd Video Decoder (@54MHz/108MHz)
EX3A_07, EX3A_06, EX3A_05, EX3A_04, EX3A_03, EX3A_02, EX3A_01, EX3A_00	156, 155, 154, 153, 152, 151, 150, 149	I	BT.656 Data for Record from External 3rd Video Decoder (#13ch~#16ch @108MHz)
EX3B_07, EX3B_06, EX3B_05, EX3B_04, EX3B_03, EX3B_02, EX3B_01, EX3B_00	145, 144, 143, 142, 141, 140, 139, 138	I	BT.656 Data for Live from External 3rd Video Decoder (one ch in #13ch~#/16ch @27MHz)
EX3_VI_CLK	147	I	Clock Input from External 3rd Video Decoder (@54MHz/108MHz)
External Digital Audio Interface (3Pins)			
EX_AU_CLK, EX_AU_SYN, EX_AU_DAT	186, 185, 184	I	External Digital Audio Clock, Sync, Data Input
ETC (28Pins)			
TEST0, TEST1, TEST2, TEST3	208, 1, 2, 3	I	Test Pins (Connect to ground)
GPIO_23, GPIO_22, GPIO_21, GPIO_20, GPIO_19, GPIO_18, GPIO_17, GPIO_16, GPIO_15, GPIO_14, GPIO_13, GPIO_12, GPIO_11, GPIO_10, GPIO_09, GPIO_08, GPIO_07, GPIO_06, GPIO_05, GPIO_04, GPIO_03, GPIO_02, GPIO_01, GPIO_00	133, 132, 131, 130, 127, 126, 125, 124, 123, 122, 121, 120, 51, 50, 49, 48, 45, 44, 43, 42, 41, 40, 39, 38	I/O	General Purpose I/O
Power(24 Pins) / Ground (24 Pins)			
VSS (24 Pins)	5, 11, 17, 23, 29, 35, 37, 47, 52, 60, 70, 82, 90, 100, 106, 117, 129, 137, 148, 158, 171, 181, 188, 199	G	Ground
VDD3D (10 Pins)	4, 46, 53, 69, 89, 105, 136, 157, 169, 197	P	Digital Power (Digital 3.3V)
VDD1D (9 Pins)	36, 59, 81, 99, 116, 128, 146, 180, 187	P	Digital Power (Digital 1.8V)
VDD1A (5 Pins)	6, 12, 18, 24, 30	P	Analog Power (Analog 1.8V)
NVP1208 208QFP_28x28 0.5P			

2. Video Decoder

: NVP1208 includes Four Channel Video Decoder and delivers high quality images. It accepts separate 4 CVBS inputs from Camera, TV or VCR and so on. It digitizes and decodes NTSC/PAL video formats into digital components video.

: NVP1208 includes 4 channel analog processing circuit that comprise anti-aliasing filter, CLAMP, AGC and ADC. . It shows the best image quality adopted by high performance 2D adaptive comb filter and vertical peaking filter. It also supports programmable Saturation, Hue, Brightness and Contrast and several function such as CTI, Programmable peaking filter, PAL compensation, IF compensation filter.

2.1 Functional Overview

: The role of video decoder is to separate luminance and chrominance signals from composite video signal.
Figure 2.1 shows the block diagram of decoder part

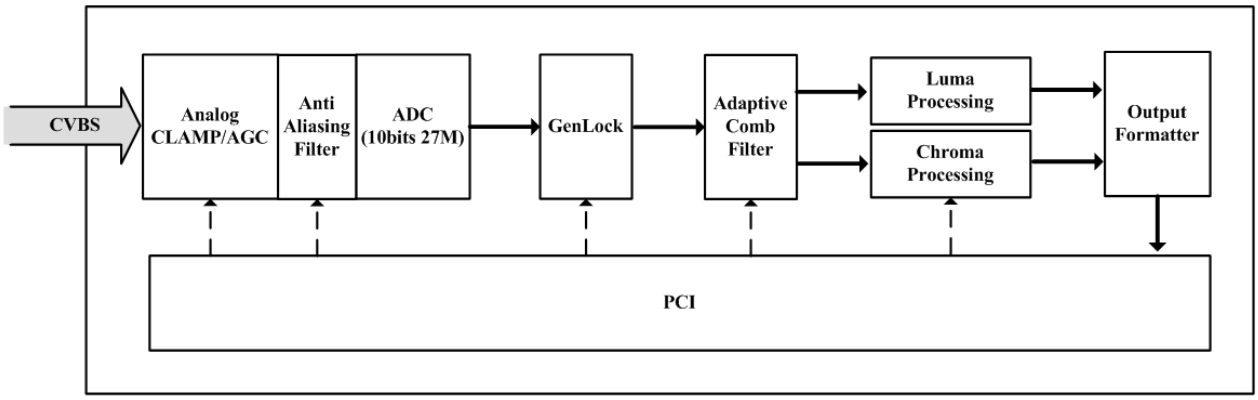


Figure 2.1. Video Decoder Data Flow of NVP1208

The First step to decode composite video signals is to digitize the entire composite video signal using an A/D converter (ADC). NVP1208 uses the 10-bit ADC whose frequency is 27Mhz. Video inputs are usually AC-coupled and have a 75 Ohm AC and DC input impedance. As a result, the video signal must be DC restored every scan line during horizontal sync to position the sync tips at known voltage level using the AGC/CLAMP logic. The video signal also is lowpass filtered to about 9MHz in Anti aliasing Filter to remove any high-frequency components that may result in aliasing.

Vertical sync and horizontal sync information are recovered in Genlock block. When composite video signal is decoded, the luminance and chrominance are separated by Adaptive Comb Filter. The quality of decoded image is strongly dependent on the signal quality of separated Y and C. To achieve best quality of image, 2D Adaptive Comb Filter is used.

The chrominance demodulator in color processing block accepts modulated chrominance data from Adaptive Comb Filter which generates Cb/Cr color difference data. During active video period, the chrominance data is demodulated using sine and cosine subcarrier data.

2.2 Video Input Formats

: NVP1208 supports all NTSC/PAL Video Standard. Table 2.1 shows NTSC/PAL Video Standards and Register Setting Value (VIDEO FORMAT, 0x208[4:0]/0x208[12:8]/0x208[20:16]/0x208[28:24]) to support them.

VIDEO_FORMAT	FORMAT	LINE	HZ	Fsc(MHz)
0x00	NTSC-M,J	525	60	3.579545
0x11	NTSC-4.43	525	60	4.43361875
0x1D	PAL-B,D,G,H,I	625	50	4.43361875
0x16	PAL-M	525	60	3.57561149
0x1F	PAL-Nc	625	50	3.58205625
0x15	PAL-60	525	60	4.433619
% Don't use auto-detect mode in case of NRT (Non Real Time) operation				

Table 2.1 NVP1208 Input Video Image Formats

2.3 Analog Front End (CLAMP, AGC, Anti-aliasing Filter)

: NVP1208 includes 4 channel analog processing circuit that comprise anti-aliasing filter, ADC, AGC and CLAMP. Because its design is dedicated to video application, Analog Processing circuit does not require external reference circuit. External coupling capacitance only is needed for NVP1208. Figure 2.2 demonstrates the bode plot of Anti-aliasing Filter. Anti-aliasing Filter is controlled by a Register (AFE_FIR_MODE, 0x070[28]).

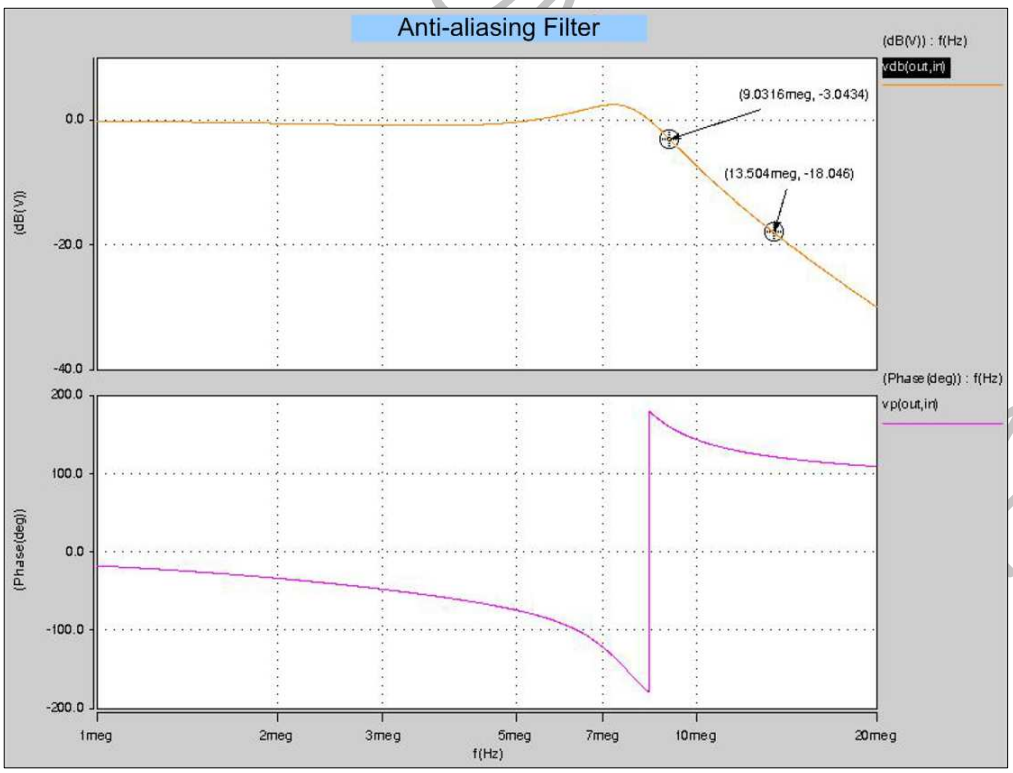


Figure 2.2 Anti-aliasing Filter characteristic

2.4 Genlock (Robust Sync Detection, Robust No-Video Detection)

: NVP1208 provides a fully digital GenLocking circuitry. The digital Genlocking Circuitry uses the locking method of the timing control signals such as horizontal sync, vertical sync, and the color subcarrier. NVP1208 uses the proprietary Genlocking mechanism for video application system. It supports very Robust Sync Detection & Robust No-Video Detection, and it is also showed reliable operation in Non-standard signal and Weak-signal.

2.5 Y/C separation (3H/5H Adaptive Comb Filter)

: An adaptive comb filter is used to separate Y and C signal from NTSC/PAL standard video signal. Therefore, The output image is sharper and clearer compared to other video decoder. To achieve this, BSF(Band Split Filter) is used. Figure 2.3. shows the Chroma BSF which is controlled by Register (BSF_MODE, 0x204[31:24]).

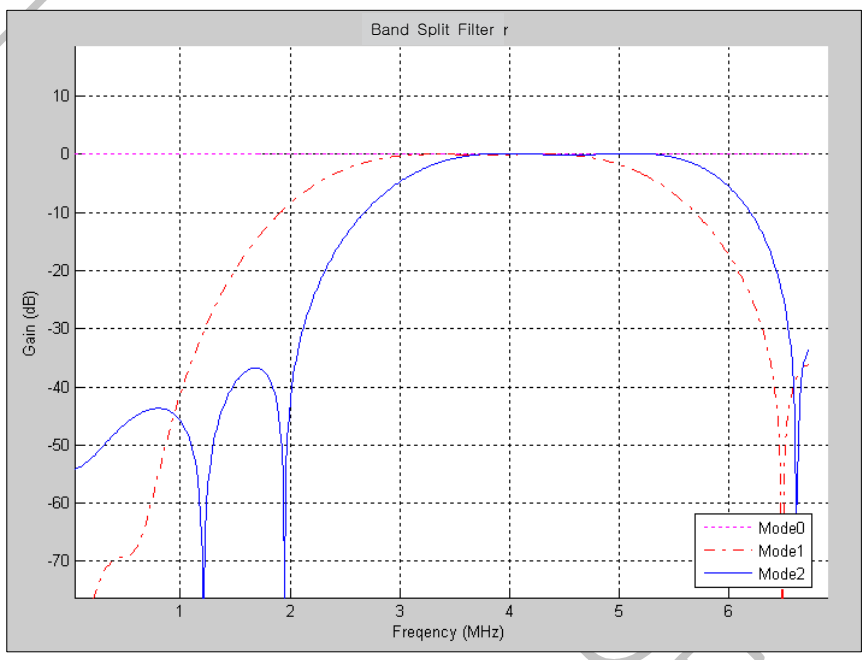


Figure 2.3 Band Split Filter Characteristic

NVP1208 can also separate Y signal from C signal out of input CVBS using the Notch Filter. And according to internal criteria in the NVP1208, the Notch and Comb filters can be mixed for use. In special case, use the Notch filter to separate Y signal from C signal to have a good-quality image.

2.6 Luma Processing

: The high-frequency range of Y/C separated data has a relatively smaller magnitude than the low-frequency range. The high-frequency range makes the image more distinct and remarkable, but may induce worse coding efficiencies when video signal is compressed.

NVP1208 provides the peaking filter and Gain control for emphasizing or depressing the high-frequency area to avoid this problem. The luma filter is applied to this purpose and its characteristics can be controlled by register.

(Y_FIR_MODE, 0x22C[15:0])

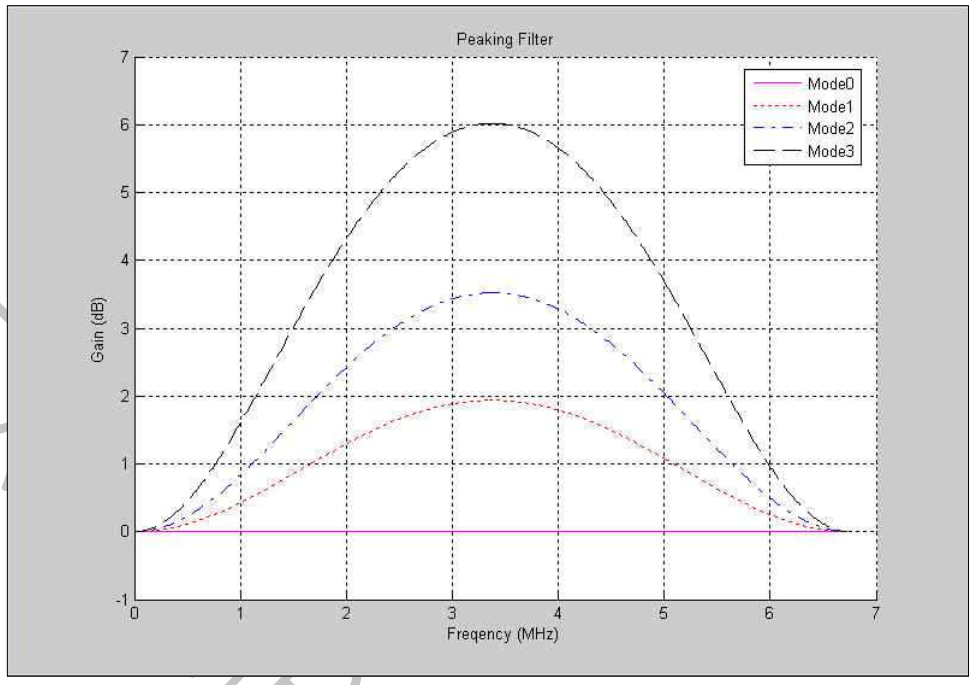


Figure 2.4 Peaking Filter Characteristic

2.7 Chroma Processing

: Chroma processing mainly consists of 3 parts: demodulation, filtering, and ACC(Automatic Chroma-gain Control). The chroma demodulator receives modulated chroma from Y/C separator, and generates demodulated color difference data. Demodulated data must be low-pass filtered to reduce anti-aliasing artifacts.

Figure 2.5. shows chroma demodulation and filtering process. Chroma LPF frequency characteristics is demonstrated in Figure 2.6. Users can select the chroma filter through I2C interface (CLPF_SEL, 0x0B8[9:8]).

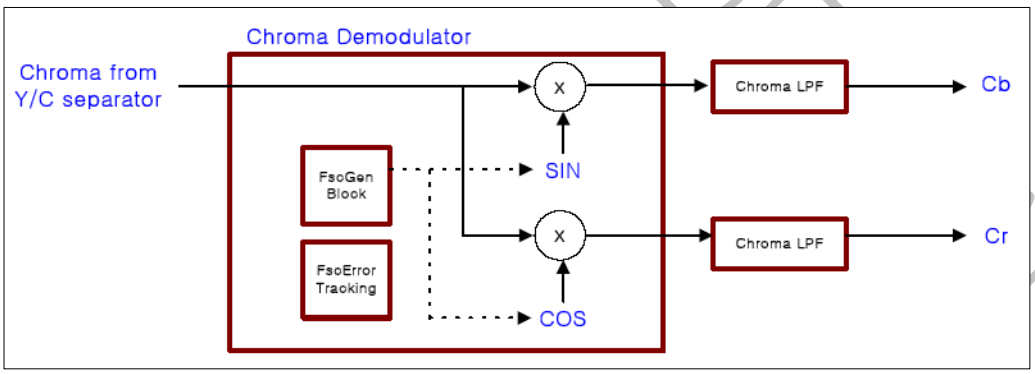


Figure 2.5 Chroma Process

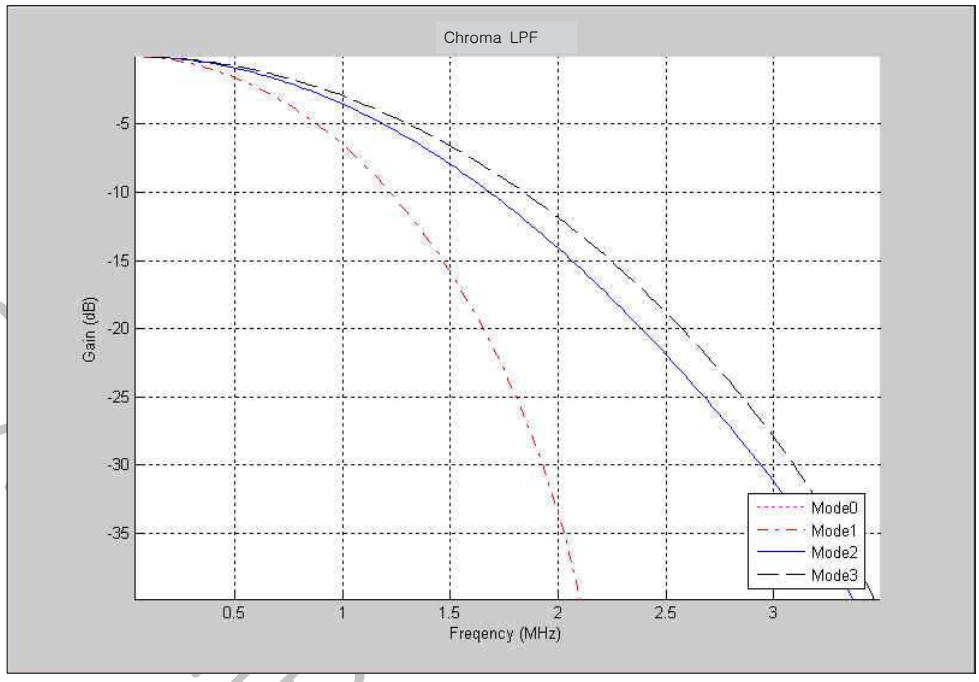


Figure 2.6 Chroma Low Pass filter Characteristic

2.8 Video Scaler

: NVP1208 has 5 scalers(4 scalers for Record Output, 1 scaler for Live Output). A Scaler plays a role to reduce input image size to the size user wants. Please refer to the figure 2.7 as below.

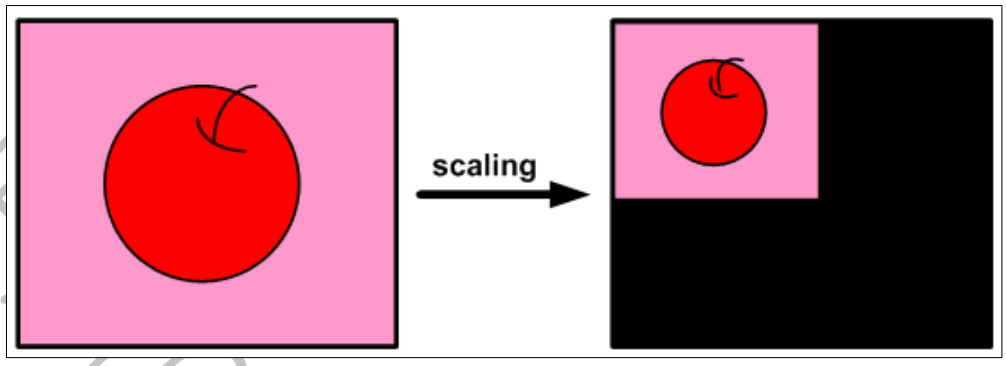


Figure 2.7 Function of Scaler

NVP1208 assigns each decoder to such channel. A User uses this scaler to control the size of input image by 1/32 for horizontal and vertical direction. H-direction's size can be controlled by the H_DTOx[20:0] (0x164/0x16C/0x174/0x17C/0x184) register and V-direction's one by V_DTOx[20:0] (0x168/0x170/0x178/0x180/0x188) register. The values of H_DTOx and V_DTOx is determined by following formula.

NTSC : H_DTOx[20:0] = (HP_scaled/720)× (2^20)
V_DTOx[20:0] = (VP_scaled/240)× (2^20)
PAL : H_DTOx[20:0] = (HP_scaled/720)× (2^20)
V_DTOx[20:0] = (VP_scaled/288)× (2^20)

Where, HP_scaled indicates horizontal pixel number or the size of the image which a user wants to get. VP_scaled does the same role as HP_scaled but for vertical direction.

For example of using this register, if you need 360x240 scaled image in NTSC, H_DTOx[20:0] shall have the value of (360/720)× 2^20. Simply, H_DTOx[20:0] = 2^19. And V_DTOx[20:0] becomes (120/240)× 2^20. Again, V_DTOx = 2^19

The table as below is register values for common scale sizes.

Register	704x240 (720x240)	640x240	360x240	352x240	320x240
H_DTO1 (0x164[20:0])	0x100000	0x0E8BA3	0x082900	0x080000	0x0745D2
V_DTO1 (0x168[20:0])	0x100000	0x100000	0x100000	0x100000	0x100000

Table 2.2 Register Value for Scale used frequently

NVP1208's scaler has two types of output as you can see in figure 2.8.
In mode1, the area which is not scaled is treated as blank. Therefore it can be longer than existing horizontal blank section. In this case, you should regard that in order to reduce the vertical size, it extend the horizontal blank section instead of using vertical blank. Hence, vertical blank section is able to have over 1 line range only for horizontal blank section under the standard status.(See the left side of Figure 2.8). Mode2 is output-way that let horizontal and vertical blank signals follow the standard and the section which is supposed to be blanked is changed to the value users define. Please refer to figure 2.8(right side). The blue section displays the result that users define as blue.

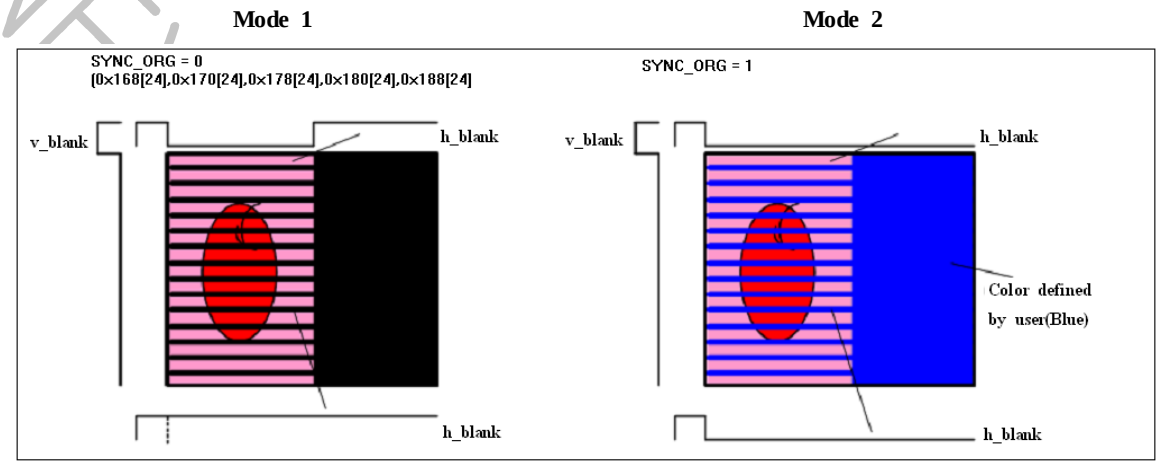


Figure 2.8 Function of Scaler

Figure 2.9 describes more detailed horizontal blank signal of Mode1. This is how scaled signal works in CCIR656 format. SAV packet(0xFF,0x00,0x00,SAV)is fixed, compared with input signal, and EAV packet takes a moving way.

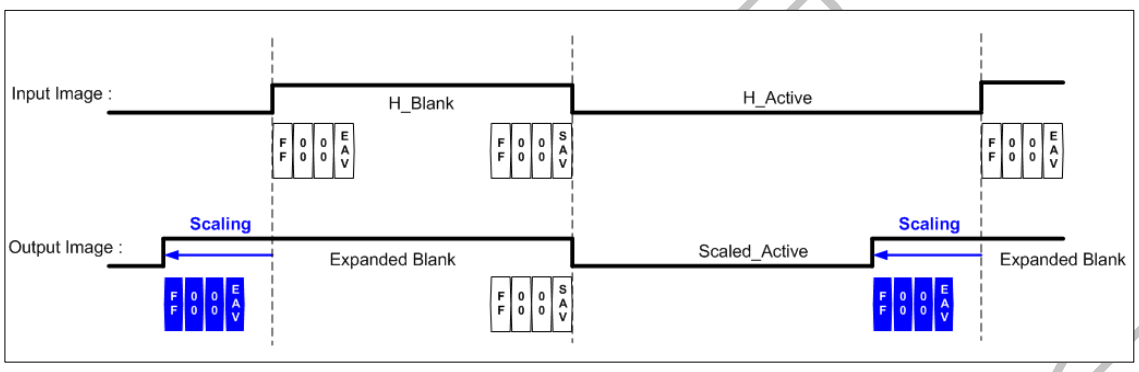


Figure 2.9 Scaled Horizontal Blank Signal of Mode 1

Figure 2.10 describes more detailed horizontal blank signal of Mode2. You might see in the figure that scaled signal is almost matched with horizontal blank signal's standard. But the rest section of the image that scaled signal is displayed is filled with the defined color(Blue) that users choose.

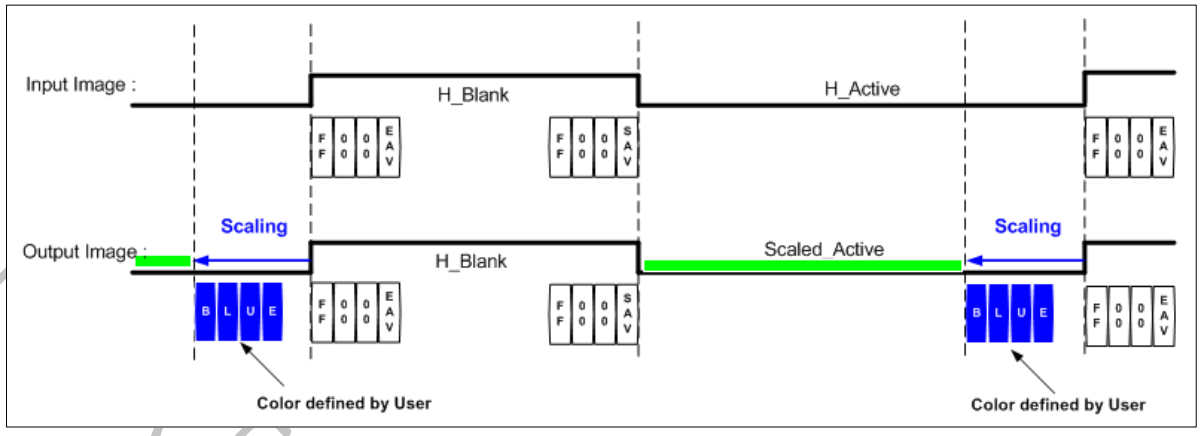


Figure 2.10 Scaled Horizontal Blank Signal of Mode 2

This scaler has a function to increase the 704 active pixel input to 720 size for horizontal direction. for using this function, there is the register to control start position in 16pixel range.
That is H_DEL(0x168/0x170/0x178/0x180/0x188[31:28]), UP(0x168/0x170/0x178/0x180/0x188[27]) (Figure 2.11)

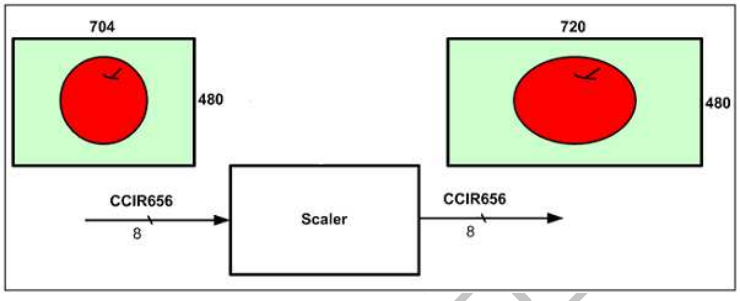


Figure 2.11 720 Extension function

3. Audio Processor

3.1 Description

: NVP1208 outputs PCM digital audio signals converted from analog audio input signals and transfers audio data to PC via PCI bus. NVP1208 has 4 channel ADCs and each ADC generate 16K / 8K sampled 16bit / 8bit audio data. In addition, NVP1208 supports audio mute detection and input volume control.

3.2 Mute Detection

: NVP1208 has an audio mute detection block for individual 4 channels. The mute detection scheme uses absolute/differential amplitude detection method. The detection method and accumulated period are defined by the ADET_MODE (0x058[11]) and ADET_FILT (0x058[10:8]) register, and the detecting threshold values are defined by ADET_TH register (0x05C[15:0]).

3.3 Volume Control

: NVP1208 can audio input volume control. Audio input volume control register is AU_DG(0x068[30:28]).

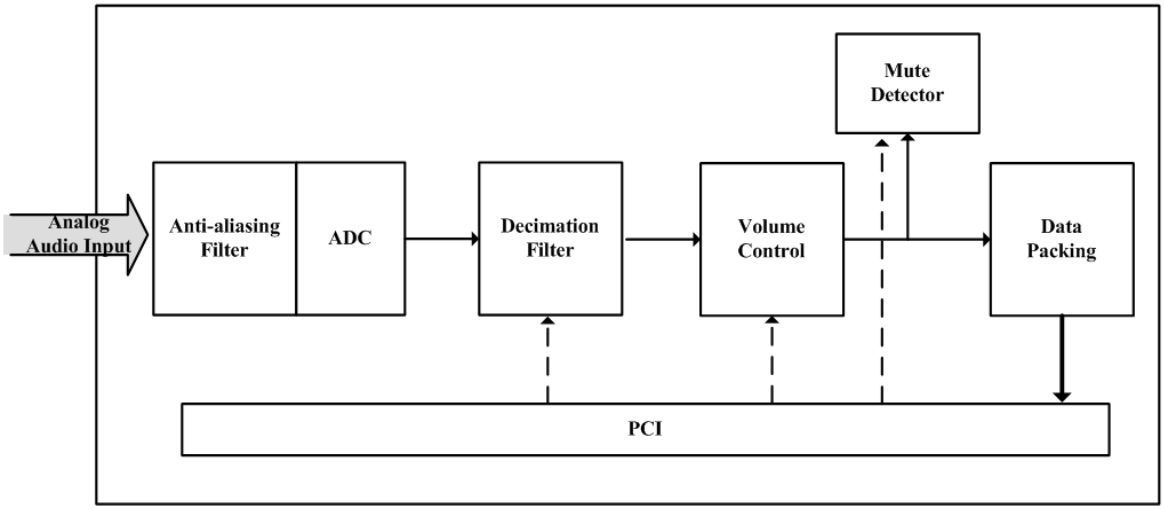


Figure 3.1 Audio Processor Data Flow of NVP1208

4. PCI Descriptions

PIN Name	PIN #	I/O Type	Signal	Description
PCI Interface (51 Pins)				
PCI_CLK	56	I	PCI Clock	*PCI Clock* provides timing for all PCI transactions. All PCI signals except PCI_RSTb, INTAb are sampled on the rising edge of PCI_CLK and all other timing parameters are defined with respect to this edge. NVP1204 operates 33MHz.
PCI_RSTb	55	I	PCI Reset	*PCI Reset* is used to bring PCI-specific registers, sequencers, and signals to a consistent state. PCI_RSTb may be asynchronous to PCI_CLK when asserted or deasserted.
INTAb	54	O	Interrupt pin	Interrupts on PCI are optional and defined as "level sensitive," asserted low(low active), using open drain output drivers. *Interrupt A* is used to request an interrupt.
REQb	58	O	Request	*Request* indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQb which must be tri-stated while PCI_RSTb is asserted.
GNTb	57	I	Grant	*Grant* indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own GNTb which must be ignored while PCI_RSTb is asserted.
IDSEL	72	I	Initialization Device Select	*Initialization Device Select* is used as a chip select during configuration read and write transactions.
AD[31:0]	61, 62, 63, 64, 65, 66, 67, 68, 73, 74, 75, 76, 77, 78, 79, 80, 95, 96, 97, 98, 101, 102, 103, 104, 108, 109, 110, 111, 112, 113, 114, 115	I/O	Address/Data	*Address and Data* are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phase. PCI supports both read and write bursts. The address phase is the frist clock cycle in the FRAMEb is asserted. During the address phase, AD[31:0] contain a physical address(32bit). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases, AD[7:0] contain the least significant byte(LSB) and AD[32:24] contain the most significant byte (MSB). Write data is stable and valid when IRDYb is asserted; read data is stable and valid when TRDYb is asserted. Data is transferred during those clocks where both IRDYb and TRDYb are asserted.
CBEb[3:0]	71, 83, 94, 107	I/O	Bus Command/ Byte Enables	*Bus Command and Byte Enables* are multiplexed on the same PCI pins. During the address phase of a transaction, CBEb[3:0] define th bus command. During the data phase, CBEb[3:0] are used as Byte Enables. The Bye Enables are valid for the entire data phase and determine which byte lanes carry meaningful data.
FRAMEb	84	I/O	Cycle Frame	*Cycle Frame* is driven by the current master to indicate the beginning and duration of an access. FRAMEb is asserted to indicate a bus transaction is beginning. While FRAMEb is deasserted, the transaction is in the final data phase or has completed.
IRDYb	85	I/O	Initiator Ready	*Initiator Ready* indicates the initiating agent's ability to complete the current data phase of the transaction. IRDYb is usede in conjunction with TRDYb. A data phase is completed on any clock both IRDYb and TRDYb are asserted. During a write, IRDYb indicates that valid data is present on AD[31:0]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDYb and TRDYb are asserted together.

PIN Name	PIN #	I/O Type	Signal	Description
TRDYb	86	I/O	Target Ready	*Target Ready* indicates the target agent's ability to complete the current data phase of the transaction. TRDYb is used in conjunction with IRDYb. A data phase is completed on any clock both TRDYb and IRDYb are asserted. During a read, TRDYb indicates that valid data is present on AD[31:0]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDYb and TRDYb are asserted together.
DEVSELb	87	I/O	Device Select	*Device Select*, When actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSELb indicates whether any device on the bus has been selected.
STOPb	88	I/O	Stop	*Stop* indicates the current target is requesting the master to stop the current transaction.
PAR	93	I/O	Parity	*Parity* is even parity across AD[31:0] and CBEb[3:0]. Parity generation is required by all PCI agents. PAR is stable and valid one clock after each address phase. For data phases, PAR is stable and valid one clock after either IRDYb is asserted on a write transaction or TRDYb is asserted on a read transaction Once PAR is valid, it remains valid until one clock after the completion of the current data phase. The master drivers PAR for address and write data phases; the target dves PAR for read data phase.
SERRb	92	O	System Error	*System Error* is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. IF an agent does not want a non-maskable interrupt to be generated, a different reporting mechanism is required. SERRb is pure open drain and is actively driven for a single PCI clock by the agent reporting the error.
PERRb	91	I/O	Parity Error	*Parity Error* is only for the reporting data parity errors during all PCI transactions except a Special Cycle. The PERRb pin is sustained tri-state and must be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERRb is one clock for each data phase that a data parity error is detected.

5. Register Map

Address Range	Description
0x00 ~ 0xFF	PCI Configuration
0x000 ~ 0x02C	Internal Processing Clock Selection
0x030 ~ 0x06C	Audio Processor Control (Almost Fix value, refer to recommand value table)
0x070 ~ 0x0FC	Video Decoder Control 1(Almost Fix value, refer to recommand value table)
0x130 ~ 0x18C	Test Pattern & Scaler Control
0x200 ~ 0x25C	Video Decoder Control 2
0x400 ~ 0x4FC	Video Record DMA Base Address
0x500 ~ 0x50C	Video Live DMA Base Address
0x600 ~ 0x674	Video Interrupt Status & H size Control
0x678 ~ 0x6DC	Video DMA Enable & DMA Burst Size
0x700 ~ 0x718	Audio DMA Control
0x720 ~ 0x764	Global DMA Interrupt Status

	Description
Constant	Fixed Register Value (System Values)
	This Color shows Reserved Register region

Addr	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x00	Device ID (0x1208)																Vendor_ID (0x1B07)																
0x04	Status																Command															
0x08	Class code																								Revision ID							
0x0C	BIST								Header Type								Latency Timer								Cacheline Size							
0x10	Base Address 0																															
0x14	Reserved																															
0018	Reserved																															
0x1C	Reserved																															
0x20	Reserved																															
0x24	Reserved																															
0x28	Reserved																															
0x2C	Subsystem ID																Subsystem Vendor ID															
0x30	Expansion ROM Base Address																															
0x34	Reserved																								Capabilities Ptr							
0x38	Reserved																															
0x3C	Max_Lat								Min_Gnt								Interrupt Pin								Interrupt Line							

Addr	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x130	DATA_SEL_8				DATA_SEL_7				DATA_SEL_6				DATA_SEL_5				DATA_SEL_8				DATA_SEL_3				DATA_SEL_2				DATA_SEL_1			
0x134	DATA_SEL_16				DATA_SEL_15				DATA_SEL_14				DATA_SEL_13				DATA_SEL_12				DATA_SEL_11				DATA_SEL_10				DATA_SEL_9			
0x138																					DATA_SEL_19				DATA_SEL_18				DATA_SEL_17			
0x13C	*0x00*								*0x00*								*0x00*								*0x00*							
0x140	*0x00*								*0x00*								*0x00*								*0x00*							
0x144																					*0x0*				*0x00*							
0x148	PAT_TYPE_8				PAT_TYPE_7				PAT_TYPE_6				PAT_TYPE_5				PAT_TYPE_8				PAT_TYPE_3				PAT_TYPE_2				PAT_TYPE_1			
0x14C	PAT_TYPE_16				PAT_TYPE_15				PAT_TYPE_14				PAT_TYPE_13				PAT_TYPE_12				PAT_TYPE_11				PAT_TYPE_10				PAT_TYPE_9			
0x150																					PAT_TYPE_19				PAT_TYPE_18				PAT_TYPE_17			
0x154																				FV_60		LIVE_CH_SEL			MV_CUR_COL				MV_CUR_SPD			MV_CUR_ON
0x158																																
0x15C																																
0x160				0	0	0	0	0				0	0	0	0	0									0	0	0	0	0				
0x164												H_DTO1																				
0x168	H_DEL1				UP1	SEL1	-	SYNC_ ORG1				V_DTO1																				
0x16C												H_DTO2																				
0x170	H_DEL2				UP2	SEL2	-	SYNC_ ORG2				V_DTO2																				
0x174												H_DTO3																				
0x178	H_DEL3				UP3	SEL3	-	SYNC_ ORG3				V_DTO3																				
0x17C												H_DTO4																				
0x180	H_DEL4				UP4	SEL4	-	SYNC_ ORG4				V_DTO4																				
0x184												H_DTO_L																				
0x188	H_DEL_L				UP_L	SEL_L	-	SYNC_ ORG_L				V_DTO_L																				
0x18C																																

Addr	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x200	*0x40*								*0x40*								*0x00*															
0x204	BSF_MODE_4		BSF_MODE_3		BSF_MODE_2		BSF_MODE_1		*0x00*								*0x40*								*0x40*							
0x208				VIDEO_FORMAT_4								VIDEO_FORMAT_3								VIDEO_FORMAT_2								VIDEO_FORMAT_1				
0x20C	BRIGHTNESS_4								BRIGHTNESS_3								BRIGHTNESS_2								BRIGHTNESS_1							
0x210	CONTRAST_4								CONTRAST_3								CONTRAST_2								CONTRAST_1							
0x214	SATURATION_4								SATURATION_3								SATURATION_2								SATURATION_1							
0x218	HUE_4								HUE_3								HUE_2								HUE_1							
0x21C	U_GAIN_4								U_GAIN_3								U_GAIN_2								U_GAIN_1							
0x220	V_GAIN_4								V_GAIN_3								V_GAIN_2								V_GAIN_1							
0x224	U_OFFSET_4								U_OFFSET_3								U_OFFSET_2								U_OFFSET_1							
0x228	V_OFFSET_4								V_OFFSET_3								V_OFFSET_2								V_OFFSET_1							
0x22C	VSYNC_INV4	VSYNC_INV3	VSYNC_INV2	VSYNC_INV1	HSYNC_INV4	HSYNC_INV3	HSYNC_INV2	HSYNC_INV1	FLD_INV_4	FLD_INV_3	FLD_INV_2	FLD_INV_1	PED_ON_4	PED_ON_3	PED_ON_2	PED_ON_1	Y_FIR_MODE_4				Y_FIR_MODE_3				Y_FIR_MODE_2				Y_FIR_MODE_1			
0x230				Y_DELAY_4								Y_DELAY_3								Y_DELAY_2								Y_DELAY_1				
0x234	H_DELAY_4								H_DELAY_3								H_DELAY_2								H_DELAY_1							
0x238	0	0	VDLY_EN4	V_DELAY_4					0	0	VDLY_EN3	V_DELAY_3					0	0	VDLY_EN2	V_DELAY_2					0	0	VDLY_EN1	V_DELAY_1				
0x23C	HBLK_END_4								HBLK_END_3								HBLK_END_2								HBLK_END_1							
0x240	0	0	VBLK_END_EN4	VBLK_END_4					0	0	VBLK_END_EN3	VBLK_END_3					0	0	VBLK_END_EN2	VBLK_END_2					0	0	VBLK_END_EN1	VBLK_END_1				
0x244	*0x00*								*0x00*								*0x00*								*0x00*							
0x248	*0x00*								*0x00*								*0x00*								*0x00*							
0x24C	*0x00*								*0x00*								*0x00*								*0x00*							
0x250	*0x00*								*0x00*								*0x00*								*0x00*							
0x254	*0x99*								*0x99*								*0x32*								*0x10*							
0x258																																*0x0*
0x25C	H_SHARPNESS_4				V_SHARPNESS_4				H_SHARPNESS_3				V_SHARPNESS_3				H_SHARPNESS_2				V_SHARPNESS_2				H_SHARPNESS_1							V_SHARPNESS_1

Addr	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x400	BASE_ADDR_1_Y																															
0x404	BASE_ADDR_1_U																															
0x408	BASE_ADDR_1_V																															
0x40C	DMA_SIZE_1																															
0x410	BASE_ADDR_2_Y																															
0x414	BASE_ADDR_2_U																															
0x418	BASE_ADDR_2_V																															
0x41C	DMA_SIZE_2																															
0x420	BASE_ADDR_3_Y																															
0x424	BASE_ADDR_3_U																															
0x428	BASE_ADDR_3_V																															
0x42C	DMA_SIZE_3																															
0x430	BASE_ADDR_4_Y																															
0x434	BASE_ADDR_4_U																															
0x438	BASE_ADDR_4_V																															
0x43C	DMA_SIZE_4																															
0x440	BASE_ADDR_5_Y																															
0x444	BASE_ADDR_5_U																															
0x448	BASE_ADDR_5_V																															
0x44C	DMA_SIZE_5																															
0x450	BASE_ADDR_6_Y																															
0x454	BASE_ADDR_6_U																															
0x458	BASE_ADDR_6_V																															
0x45C	DMA_SIZE_6																															
0x460	BASE_ADDR_7_Y																															
0x464	BASE_ADDR_7_U																															
0x468	BASE_ADDR_7_V																															
0x46C	DMA_SIZE_7																															
0x470	BASE_ADDR_8_Y																															
0x474	BASE_ADDR_8_U																															
0x478	BASE_ADDR_8_V																															
0x47C	DMA_SIZE_8																															
0x480	BASE_ADDR_9_Y																															
0x484	BASE_ADDR_9_U																															
0x488	BASE_ADDR_9_V																															
0x48C	DMA_SIZE_9																															
0x490	BASE_ADDR_10_Y																															
0x494	BASE_ADDR_10_U																															
0x498	BASE_ADDR_10_V																															
0x49C	DMA_SIZE_10																															
0x4A0	BASE_ADDR_11_Y																															
0x4A4	BASE_ADDR_11_U																															
0x4A8	BASE_ADDR_11_V																															
0x4AC	DMA_SIZE_11																															

Addr	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x4B0	BASE_ADDR_12_Y																															
0x4B4	BASE_ADDR_12_U																															
0x4B8	BASE_ADDR_12_V																															
0x4BC	DMA_SIZE_13																															
0x4C0	BASE_ADDR_13_Y																															
0x4C4	BASE_ADDR_13_U																															
0x4C8	BASE_ADDR_13_V																															
0x4CC	DMA_SIZE_13																															
0x4D0	BASE_ADDR_14_Y																															
0x4D4	BASE_ADDR_14_U																															
0x4D8	BASE_ADDR_14_V																															
0x4DC	DMA_SIZE_14																															
0x4E0	BASE_ADDR_15_Y																															
0x4E4	BASE_ADDR_15_U																															
0x4E8	BASE_ADDR_15_V																															
0x4EC	DMA_SIZE_15																															
0x4F0	BASE_ADDR_16_Y																															
0x4F4	BASE_ADDR_16_U																															
0x4F8	BASE_ADDR_16_V																															
0x4FC	DMA_SIZE_16																															

Addr	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x500	BASE_ADDR_17_Y																															
0x504	BASE_ADDR_17_U																															
0x508	BASE_ADDR_17_V																															
0x50C	DMA_SIZE_17																															

Addr	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x600																DMA_STS_17	DMA_STS_16	DMA_STS_15	DMA_STS_14	DMA_STS_13	DMA_STS_12	DMA_STS_11	DMA_STS_10	DMA_STS_9	DMA_STS_8	DMA_STS_7	DMA_STS_6	DMA_STS_5	DMA_STS_4	DMA_STS_3	DMA_STS_2	DMA_STS_1
0x604																IRQ_STS_17	IRQ_STS_16	IRQ_STS_15	IRQ_STS_14	IRQ_STS_13	IRQ_STS_12	IRQ_STS_11	IRQ_STS_10	IRQ_STS_9	IRQ_STS_8	IRQ_STS_7	IRQ_STS_6	IRQ_STS_5	IRQ_STS_4	IRQ_STS_3	IRQ_STS_2	IRQ_STS_1
0x608																VLOSS_STS_17	VLOSS_STS_16	VLOSS_STS_15	VLOSS_STS_14	VLOSS_STS_13	VLOSS_STS_12	VLOSS_STS_11	VLOSS_STS_10	VLOSS_STS_9	VLOSS_STS_8	VLOSS_STS_7	VLOSS_STS_6	VLOSS_STS_5	VLOSS_STS_4	VLOSS_STS_3	VLOSS_STS_2	VLOSS_STS_1
0x60C																EVEN_STS_17	EVEN_STS_16	EVEN_STS_15	EVEN_STS_14	EVEN_STS_13	EVEN_STS_12	EVEN_STS_11	EVEN_STS_10	EVEN_STS_9	EVEN_STS_8	EVEN_STS_7	EVEN_STS_6	EVEN_STS_5	EVEN_STS_4	EVEN_STS_3	EVEN_STS_2	EVEN_STS_1
0x610																ODD_STS_17	ODD_STS_16	ODD_STS_15	ODD_STS_14	ODD_STS_13	ODD_STS_12	ODD_STS_11	ODD_STS_10	ODD_STS_9	ODD_STS_8	ODD_STS_7	ODD_STS_6	ODD_STS_5	ODD_STS_4	ODD_STS_3	ODD_STS_2	ODD_STS_1
0x614																DMA_EN-17	DMA_EN-16	DMA_EN-15	DMA_EN-14	DMA_EN-13	DMA_EN-12	DMA_EN-11	DMA_EN-10	DMA_EN-9	DMA_EN-8	DMA_EN-7	DMA_EN-6	DMA_EN-5	DMA_EN-4	DMA_EN-3	DMA_EN-2	DMA_EN-1
0x618																IRQ_MASK_17	IRQ_MASK_16	IRQ_MASK_15	IRQ_MASK_14	IRQ_MASK_13	IRQ_MASK_12	IRQ_MASK_11	IRQ_MASK_10	IRQ_MASK_9	IRQ_MASK_8	IRQ_MASK_7	IRQ_MASK_6	IRQ_MASK_5	IRQ_MASK_4	IRQ_MASK_3	IRQ_MASK_2	IRQ_MASK_1
0x61C																DIG_SWAP_17	DIG_SWAP_16	DIG_SWAP_15	DIG_SWAP_14	DIG_SWAP_13	DIG_SWAP_12	DIG_SWAP_11	DIG_SWAP_10	DIG_SWAP_9	DIG_SWAP_8	DIG_SWAP_7	DIG_SWAP_6	DIG_SWAP_5	DIG_SWAP_4	DIG_SWAP_3	DIG_SWAP_2	DIG_SWAP_1
0x620	H_SIZE #2															H_SIZE #1																
0x624	H_SIZE #4															H_SIZE #3																
0x628	H_SIZE #6															H_SIZE #5																
0x62C	H_SIZE #8															H_SIZE #7																
0x630	H_SIZE #10															H_SIZE #9																
0x634	H_SIZE #12															H_SIZE #11																
0x638	H_SIZE #14															H_SIZE #13																
0x63C	H_SIZE #16															H_SIZE #15																
0x640																H_SIZE #17																
0x644																																
0x648																																
0x64C																																
0x650																																
0x654																																
0x658																																
0x65C																																
0x660																															FMT_PLANAR	
0x664																																
0x668																																
0x66C																																
0x670																FMT_CHAR_17	FMT_CHAR_16	FMT_CHAR_15	FMT_CHAR_14	FMT_CHAR_13	FMT_CHAR_12	FMT_CHAR_11	FMT_CHAR_10	FMT_CHAR_9	FMT_CHAR_8	FMT_CHAR_7	FMT_CHAR_6	FMT_CHAR_5	FMT_CHAR_4	FMT_CHAR_3	FMT_CHAR_2	FMT_CHAR_1
0x674																VIDEO_EN_17	VIDEO_EN_16	VIDEO_EN_15	VIDEO_EN_14	VIDEO_EN_13	VIDEO_EN_12	VIDEO_EN_11	VIDEO_EN_10	VIDEO_EN_9	VIDEO_EN_8	VIDEO_EN_7	VIDEO_EN_6	VIDEO_EN_5	VIDEO_EN_4	VIDEO_EN_3	VIDEO_EN_2	VIDEO_EN_1

Addr	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x678																									Y_BURST								
0x67C																																
0x680																																
0x684																																
0x688																																
0x68C																																
0x690																																
0x694																																
0x698																									C_BURST							
0x69C																																
0x6A0																																
0x6A4																																
0x6A8																																
0x6AC																																
0x6B0																																
0x6B4																																
0x6B8	*0x00*								*0x20*								*0x08*								*0x2D*							
0x6BC																																
0x6C0																ODD_EN_17	ODD_EN_16	ODD_EN_15	ODD_EN_14	ODD_EN_13	ODD_EN_12	ODD_EN_11	ODD_EN_10	ODD_EN_9	ODD_EN_8	ODD_EN_7	ODD_EN_6	ODD_EN_5	ODD_EN_4	ODD_EN_3	ODD_EN_2	ODD_EN_1
0x6C4																EVEN_EN_17	EVEN_EN_16	EVEN_EN_15	EVEN_EN_14	EVEN_EN_13	EVEN_EN_12	EVEN_EN_11	EVEN_EN_10	EVEN_EN_9	EVEN_EN_8	EVEN_EN_7	EVEN_EN_6	EVEN_EN_5	EVEN_EN_4	EVEN_EN_3	EVEN_EN_2	EVEN_EN_1
0x6C8																																
0x6CC																																
0x6D0																																
0x6D4																																
0x6D8																																
0x6DC																	*0x44*								*0x44*							

Addr	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x700	AUD_DMA_BA0_A																															
0x704	AUD_DMA_BA0_B																															
0x708	AUD_DMA_BA1_A																															
0x70C	AUD_DMA_BA1_B																															
0x710	AUD_DMA0_SIZE																															
0x714	AUD_DMA1_SIZE																															
0x718																	AUD_BURST_SIZE															
0x71C																																
0x720																																aud_ ctrl
0x724																												AUD_IRQ_MASK				
0x728																												AUD_IRQ_STS				
0x72C																																R_MASK
0x730									GPIO_DIR																							
0x734									GPIO_OUT																							
0x738									GPIO_IN																							
0x73C																																R_STS
0x740																																irq_ctrl
0x744																														rmt_irq	aud_irq	vid_irq
0x748																																
0x74C																																
0x750																											I2C_P1_ DIR_SD A	I2C_P1_ DIR_SC L	I2C_P1_ GET_SD A	I2C_P1_ GET_SC L	I2C_P1_ SET_SD A	I2C_P1 _SET_S CL
0x754																											I2C_P2_ DIR_SD A	I2C_P2_ DIR_SC L	I2C_P2_ GET_SD A	I2C_P2_ GET_SC L	I2C_P2_ SET_SD A	I2C_P2 _SET_S CL
0x758																											Test Only					
0x75C																																
0x760																	Rate_16	Rate_15	Rate_14	Rate_13	Rate_12	Rate_11	Rate_10	Rate_9	Rate_8	Rate_7	Rate_6	Rate_5	Rate_4	Rate_3	Rate_2	Rate_1
0x764																	R_STS_16	R_STS_15	R_STS_14	R_STS_13	R_STS_12	R_STS_11	R_STS_10	R_STS_9	R_STS_8	R_STS_7	R_STS_6	R_STS_5	R_STS_4	R_STS_3	R_STS_2	R_STS_1
0x768																																
0x76C																																
0x770																																
0x774																																

6. Register Description

6.1 PCI Configuration space

31	16 15	0	AD[7:0]
Device ID		Vendor ID	0x00
Status		Command	0x04
Class Code		Revision ID	0x08
Reserved	Header Type 0	Latency Timer	Reserved	0x0C
Base Address 0 Register			0x10
Reserved			0x14
Reserved			0x18 0x1C 0x20 0x24
Reserved			0x28
Subsystem ID		Subsystem Vendor ID	0x2C
Reserved			0x30
Reserved			0x34
Reserved			0x38
Max_Lat	Min_Gnt	Interrupt pin	Interrupt Line	0x3C
Reserved			0x40

Figure 6.1 PCI Type 0 Configuration Space Header

6.2 PCI Configuration register

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE
0x00	Device ID	[31:16]	R	Identifies the particular device of the device.	**0x12081B07**
	Vendor ID	[15:0]	R	Identifies manufacturer of device, assigned by the PCI SIG.	
0x04	Detected Parity Error	[31]	R/W	Set by a device whenever it detects a parity error, even if parity error handling is disabled.	**0x04000000**
	Signaled System Error	[30]	R/W	Set by a device that asserts SERR#	
	Received Master Abort	[29]	R/W	Set by a master when it terminates a transaction with Master Abort.	
	Received Target Abort	[28]	R/W	Set by a master when its transaction is terminated by Target Abort.	
	Signaled Target Abort	[27]	R/W	Set by a target when it terminates a transaction with Target Abort. This occurs when detecting an address parity error.	
	Address Decoder Time	[26:25]	R	DEVSEL# Timing 00 = Fast, 01 = medium, 10 = slow, 11 = reserved.	
	Data Parity Reported	[24]	R/W	Only implemented by masters.	
	FB2B Capable	[23]	R	1 = target device supports fasts back to back transactions to different targets.	
	Reserved	[22]	R	1 = device supports "user definable features".	
	66MHz Capable	[21]	R	1 = device is capable of 66MHz operation.	
	Reserved	[20:10]	R/W	Reserved registers	
	FB2B Enable	[9]	R/W	When 1, allows a master to execute fast back to back transactions to different targets.	
	SERR# enable	[8]	R/W	When 1, allows the device to assert SETT#.	
	Wait cycle Control	[7]	R/W	Controls whether a device does address/data stepping.	
	Parity Error Response	[6]	R/W	When 1, the device responds to a detected parity error by asserting PERR#.	
	VGA Palette snoop	[5]	R/W	Controls how VGA devices handle access to VGA palette registers.	
	Memory Write and Invalidate Enable	[4]	R/W	When 1, a master is allowed to use the Memory Write and Invalidate command if so capable. When 0, the master must use Memury Write instead.	
	Special Cycles	[3]	R/W	When 1, allows a device to monitor Special Cycle operations.	
	Bus Master	[2]	R/W	When 1, enables the device to act as a bus master.	
	MemorySpace	[1]	R/W	When 1, allows the device to respond to PCI memory space access	
	IO Space	[0]	R/W	When 1, allows the device to respond to PCI I/O space accesses.	
0x08	Class Code	[31:8]	R	NVP1204 is a multimedia video device.	**0x04000000**
	Revision ID	[7:0]	R	This register identifies the device revision.	
0x0C	BIST	[31:24]	R	Built In Self-Test Register	**0x00001000**
	Header Type	[23:16]	R	Type 00h = Configuration Space Header, 01h = PCI to PCI bridges	
	Latency Timer	[15:8]	R/W	The number of PCI bus clocks for the latency timer used by th bus master. Once the latency expires, the master must initiate transaction termination as soon as GNT# is removed.	
0x10	Base Address 0 Register	[31:0]	R/W	Determine the location of the registers in the 32-bit addressable memory space	**assigned by cpu**
0x2C	Subsystem ID	[31:16]	R	Vendor specific	**0x00000000**
	Subsystem Vendor ID	[15:0]	R	Identify the vendor of the add-on board or subsystem, assigned by PCI SIG.	
0x3C	Max_Lat	[31:24]	R	It is used for specifying how often the device needs to gain access the PCI bus. in units of 250ns(8clocks)	**0x28**
	Min_Gnt	[23:16]	R	It is used for specifying how long a burst period the device needs assuming a clock rate of 33MHz. in units of 250ns (8 clocks)	**0x10**
	Interrupt Pin	[15:8]	R	NVP1204 interrupt pin is connected to INTA#, the only one usable by a single function device.	**0x01**
	Interrupt Line	[7:0]	R/W	Post software will write the routing information into this register as it initializes and configures the system	**assigned by cpu**

6.3 PCI part

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x400	BASE_ADDR_1_Y	[31:0]	R/W	Base address of video channel 1ch for : - packed mode : whole video data - planar mode : Y Data only	**by cpu**
0x404	BASE_ADDR_1_U	[31:0]	R/W	Base address of video channel 1ch for : - packed mode : not used - planar mode : U Data only	**by cpu**
0x408	BASE_ADDR_1_V	[31:0]	R/W	Base address of video channel 1ch for : - packed mode : not used - planar mode : V Data only	**by cpu**
0x40C	DMA_SIZE_1	[31:0]	R/W	DMA size for channel 1ch - packed mode : whole video size with unit of 4bytes - planar mode : the same value as the size when packed mode, real DMA size is automatically calculated.	**by cpu**
0x410	BASE_ADDR_2_Y	[31:0]	R/W	Base address of video channel 2ch for : - packed mode : whole video data - planar mode : Y Data only	**by cpu**
0x414	BASE_ADDR_2_U	[31:0]	R/W	Base address of video channel 2ch for : - packed mode : not used - planar mode : U Data only	**by cpu**
0x418	BASE_ADDR_2_V	[31:0]	R/W	Base address of video channel 2ch for : - packed mode : not used - planar mode : V Data only	**by cpu**
0x41C	DMA_SIZE_2	[31:0]	R/W	DMA size for channel 2ch - packed mode : whole video size with unit of 4bytes - planar mode : the same value as the size when packed mode, real DMA size is automatically calculated.	**by cpu**
0x420	BASE_ADDR_3_Y	[31:0]	R/W	Base address of video channel 3ch for : - packed mode : whole video data - planar mode : Y Data only	**by cpu**
0x424	BASE_ADDR_3_U	[31:0]	R/W	Base address of video channel 3ch for : - packed mode : not used - planar mode : U Data only	**by cpu**
0x428	BASE_ADDR_3_V	[31:0]	R/W	Base address of video channel 3ch for : - packed mode : not used - planar mode : V Data only	**by cpu**
0x42C	DMA_SIZE_3	[31:0]	R/W	DMA size for channel 3ch - packed mode : whole video size with unit of 4bytes - planar mode : the same value as the size when packed mode, real DMA size is automatically calculated.	**by cpu**
0x430	BASE_ADDR_4_Y	[31:0]	R/W	Base address of video channel 4ch for : - packed mode : whole video data - planar mode : Y Data only	**by cpu**
0x434	BASE_ADDR_4_U	[31:0]	R/W	Base address of video channel 4ch for : - packed mode : not used - planar mode : U Data only	**by cpu**
0x438	BASE_ADDR_4_V	[31:0]	R/W	Base address of video channel 4ch for : - packed mode : not used - planar mode : V Data only	**by cpu**
0x43C	DMA_SIZE_4	[31:0]	R/W	DMA size for channel 4ch - packed mode : whole video size with unit of 4bytes - planar mode : the same value as the size when packed mode, real DMA size is automatically calculated.	**by cpu**

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x440	BASE_ADDR_5_Y	[31:0]	R/W	Base address of video channel 5ch for : - packed mode : whole video data - planar mode : Y Data only	by cpu
0x444	BASE_ADDR_5_U	[31:0]	R/W	Base address of video channel 5ch for : - packed mode : not used - planar mode : U Data only	by cpu
0x448	BASE_ADDR_5_V	[31:0]	R/W	Base address of video channel 5ch for : - packed mode : not used - planar mode : V Data only	by cpu
0x44C	DMA_SIZE_5	[31:0]	R/W	DMA size for channel 5ch - packed mode : whole video size with unit of 4bytes - planar mode : the same value as the size when packed mode, real DMA size is automatically calculated.	by cpu
0x450	BASE_ADDR_6_Y	[31:0]	R/W	Base address of video channel 6ch for : - packed mode : whole video data - planar mode : Y Data only	by cpu
0x454	BASE_ADDR_6_U	[31:0]	R/W	Base address of video channel 6ch for : - packed mode : not used - planar mode : U Data only	by cpu
0x458	BASE_ADDR_6_V	[31:0]	R/W	Base address of video channel 6ch for : - packed mode : not used - planar mode : V Data only	by cpu
0x45C	DMA_SIZE_6	[31:0]	R/W	DMA size for channel 6ch - packed mode : whole video size with unit of 4bytes - planar mode : the same value as the size when packed mode, real DMA size is automatically calculated.	by cpu
0x460	BASE_ADDR_7_Y	[31:0]	R/W	Base address of video channel 7ch for : - packed mode : whole video data - planar mode : Y Data only	by cpu
0x464	BASE_ADDR_7_U	[31:0]	R/W	Base address of video channel 7ch for : - packed mode : not used - planar mode : U Data only	by cpu
0x468	BASE_ADDR_7_V	[31:0]	R/W	Base address of video channel 7ch for : - packed mode : not used - planar mode : V Data only	by cpu
0x46C	DMA_SIZE_7	[31:0]	R/W	DMA size for channel 7ch - packed mode : whole video size with unit of 4bytes - planar mode : the same value as the size when packed mode, real DMA size is automatically calculated.	by cpu
0x470	BASE_ADDR_8_Y	[31:0]	R/W	Base address of video channel 8ch for : - packed mode : whole video data - planar mode : Y Data only	by cpu
0x474	BASE_ADDR_8_U	[31:0]	R/W	Base address of video channel 8ch for : - packed mode : not used - planar mode : U Data only	by cpu
0x478	BASE_ADDR_8_V	[31:0]	R/W	Base address of video channel 8ch for : - packed mode : not used - planar mode : V Data only	by cpu
0x47C	DMA_SIZE_8	[31:0]	R/W	DMA size for channel 8ch - packed mode : whole video size with unit of 4bytes - planar mode : the same value as the size when packed mode, real DMA size is automatically calculated.	by cpu

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x480	BASE_ADDR_9_Y	[31:0]	R/W	Base address of video channel 9ch for : - packed mode : whole video data - planar mode : Y Data only	by cpu
0x484	BASE_ADDR_9_U	[31:0]	R/W	Base address of video channel 9ch for : - packed mode : not used - planar mode : U Data only	by cpu
0x488	BASE_ADDR_9_V	[31:0]	R/W	Base address of video channel 9ch for : - packed mode : not used - planar mode : V Data only	by cpu
0x48C	DMA_SIZE_9	[31:0]	R/W	DMA size for channel 9ch - packed mode : whole video size with unit of 4bytes - planar mode : the same value as the size when packed mode, real DMA size is automatically calculated.	by cpu
0x490	BASE_ADDR_10_Y	[31:0]	R/W	Base address of video channel 10ch for : - packed mode : whole video data - planar mode : Y Data only	by cpu
0x494	BASE_ADDR_10_U	[31:0]	R/W	Base address of video channel 10ch for : - packed mode : not used - planar mode : U Data only	by cpu
0x498	BASE_ADDR_10_V	[31:0]	R/W	Base address of video channel 10ch for : - packed mode : not used - planar mode : V Data only	by cpu
0x49C	DMA_SIZE_10	[31:0]	R/W	DMA size for channel 10ch - packed mode : whole video size with unit of 4bytes - planar mode : the same value as the size when packed mode, real DMA size is automatically calculated.	by cpu
0x4A0	BASE_ADDR_11_Y	[31:0]	R/W	Base address of video channel 11ch for : - packed mode : whole video data - planar mode : Y Data only	by cpu
0x4A4	BASE_ADDR_11_U	[31:0]	R/W	Base address of video channel 11ch for : - packed mode : not used - planar mode : U Data only	by cpu
0x4A8	BASE_ADDR_11_V	[31:0]	R/W	Base address of video channel 11ch for : - packed mode : not used - planar mode : V Data only	by cpu
0x4AC	DMA_SIZE_11	[31:0]	R/W	DMA size for channel 11ch - packed mode : whole video size with unit of 4bytes - planar mode : the same value as the size when packed mode, real DMA size is automatically calculated.	by cpu
0x4B0	BASE_ADDR_12_Y	[31:0]	R/W	Base address of video channel 12ch for : - packed mode : whole video data - planar mode : Y Data only	by cpu
0x4B4	BASE_ADDR_12_U	[31:0]	R/W	Base address of video channel 12ch for : - packed mode : not used - planar mode : U Data only	by cpu
0x4B8	BASE_ADDR_12_V	[31:0]	R/W	Base address of video channel 12ch for : - packed mode : not used - planar mode : V Data only	by cpu
0x4BC	DMA_SIZE_12	[31:0]	R/W	DMA size for channel 12ch - packed mode : whole video size with unit of 4bytes - planar mode : the same value as the size when packed mode, real DMA size is automatically calculated.	by cpu

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x4C0	BASE_ADDR_13_Y	[31:0]	R/W	Base address of video channel 13ch for : - packed mode : whole video data - planar mode : Y Data only	by cpu
0x4C4	BASE_ADDR_13_U	[31:0]	R/W	Base address of video channel 13ch for : - packed mode : not used - planar mode : U Data only	by cpu
0x4C8	BASE_ADDR_13_V	[31:0]	R/W	Base address of video channel 13ch for : - packed mode : not used - planar mode : V Data only	by cpu
0x4CC	DMA_SIZE_13	[31:0]	R/W	DMA size for channel 13ch - packed mode : whole video size with unit of 4bytes - planar mode : the same value as the size when packed mode, real DMA size is automatically calculated.	by cpu
0x4D0	BASE_ADDR_14_Y	[31:0]	R/W	Base address of video channel 14ch for : - packed mode : whole video data - planar mode : Y Data only	by cpu
0x4D4	BASE_ADDR_14_U	[31:0]	R/W	Base address of video channel 14ch for : - packed mode : not used - planar mode : U Data only	by cpu
0x4D8	BASE_ADDR_14_V	[31:0]	R/W	Base address of video channel 14ch for : - packed mode : not used - planar mode : V Data only	by cpu
0x4DC	DMA_SIZE_14	[31:0]	R/W	DMA size for channel 14ch - packed mode : whole video size with unit of 4bytes - planar mode : the same value as the size when packed mode, real DMA size is automatically calculated.	by cpu
0x4E0	BASE_ADDR_15_Y	[31:0]	R/W	Base address of video channel 15ch for : - packed mode : whole video data - planar mode : Y Data only	by cpu
0x4E4	BASE_ADDR_15_U	[31:0]	R/W	Base address of video channel 15ch for : - packed mode : not used - planar mode : U Data only	by cpu
0x4E8	BASE_ADDR_15_V	[31:0]	R/W	Base address of video channel 15ch for : - packed mode : not used - planar mode : V Data only	by cpu
0x4EC	DMA_SIZE_15	[31:0]	R/W	DMA size for channel 15ch - packed mode : whole video size with unit of 4bytes - planar mode : the same value as the size when packed mode, real DMA size is automatically calculated.	by cpu
0x4F0	BASE_ADDR_16_Y	[31:0]	R/W	Base address of video channel 16ch for : - packed mode : whole video data - planar mode : Y Data only	by cpu
0x4F4	BASE_ADDR_16_U	[31:0]	R/W	Base address of video channel 16ch for : - packed mode : not used - planar mode : U Data only	by cpu
0x4F8	BASE_ADDR_16_V	[31:0]	R/W	Base address of video channel 16ch for : - packed mode : not used - planar mode : V Data only	by cpu
0x4FC	DMA_SIZE_16	[31:0]	R/W	DMA size for channel 16ch - packed mode : whole video size with unit of 4bytes - planar mode : the same value as the size when packed mode, real DMA size is automatically calculated.	by cpu

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x500	BASE_ADDR_17_Y	[31:0]	R/W	Base address of video channel 17ch for : - packed mode : whole video data - planar mode : Y Data only	by cpu
0x504	BASE_ADDR_17_U	[31:0]	R/W	Base address of video channel 17ch for : - packed mode : not used - planar mode : U Data only	by cpu
0x508	BASE_ADDR_17_V	[31:0]	R/W	Base address of video channel 17ch for : - packed mode : not used - planar mode : V Data only	by cpu
0x50C	DMA_SIZE_17	[31:0]	R/W	DMA size for channel 17ch - packed mode : whole video size with unit of 4bytes - planar mode : the same value as the size when packed mode, real DMA size is automatically calculated.	by cpu

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x600	DMA_STS	[16:0]	RO	Each channel DMA STATUS 1: DMA BUSY 0: idle	-
0x604	IRQ_STS	[16:0]	RO	Interrupt status for video, Write 1 to clear interrupt Each bit represents each DMA channel	-
0x608	VLOSS_STS	[16:0]	RO	Video Loss Status 1: Video Loss 0:Video On	-
0x60C	EVEN_FIELD	[16:0]	RO	Video Even Field Status 1: Even Field, 0: Odd Field	-
0x610	ODD_FIELD	[16:0]	RO	Video ODD Field Status 1: Odd Field, 0: Even Field	-
0x614	DMA_CTRL	[16:0]	R/W	Enable Video DMA Each bit represents each DMA channel	0x0001FFFF
0x618	IRQ_MASK	[16:0]	R/W	Enable or disable interrupt Mask Each bit represents each DMA channel	0x0001FFFF
0x61C	YC_SWAP	[16:0]	R/W	Data align in packed mode 1: YCbYCr 0: CbYCrY Each bit represents each DMA channel	0x00000000
0x620	H_size #1	[15:0]	R/W	Set by a software that determines H size of channel 1 window.	0x02D02D0
	H_size #2	[31:16]	R/W	Set by a software that determines H size of channel 2 window.	
0x624	H_size #3	[15:0]	R/W	Set by a software that determines H size of channel 3 window.	0x02D02D0
	H_size #4	[31:16]	R/W	Set by a software that determines H size of channel 4 window.	
0x628	H_size #5	[15:0]	R/W	Set by a software that determines H size of channel 5 window.	0x02D02D0
	H_size #6	[31:16]	R/W	Set by a software that determines H size of channel 6 window.	
0x62C	H_size #7	[15:0]	R/W	Set by a software that determines H size of channel 7 window.	0x02D02D0
	H_size #8	[31:16]	R/W	Set by a software that determines H size of channel 8 window.	
0x630	H_size #9	[15:0]	R/W	Set by a software that determines H size of channel 9 window.	0x02D02D0
	H_size #10	[31:16]	R/W	Set by a software that determines H size of channel 10 window.	
0x634	H_size #11	[15:0]	R/W	Set by a software that determines H size of channel 11 window.	0x02D02D0
	H_size #12	[31:16]	R/W	Set by a software that determines H size of channel 12 window.	
0x638	H_size #13	[15:0]	R/W	Set by a software that determines H size of channel 13 window.	0x02D02D0
	H_size #14	[31:16]	R/W	Set by a software that determines H size of channel 14 window.	
0x63C	H_size #15	[15:0]	R/W	Set by a software that determines H size of channel 15 window.	0x02D02D0
	H_size #16	[31:16]	R/W	Set by a software that determines H size of channel 16 window.	
0x640	H_size #17	[15:0]	R/W	Set by a software that determines H size of channel 17 window.	0x000002D0

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x660	FMT_PLANAR	[1:0]	R/W	Selection of DMA Trasaction of type 0 : 4:2:2 YCbCr Packet mode. 1 : 4:1:1 YCbCr Planar mode. 2 : 4:2:0 YCbCr planar mode. 3 : Don't use	**0x00000000**
0x670	FMT_CHAR_17	[16]	R/W	Enable to transfer data of Chrominance in planar mode 0 : Cb and Cr data are allowed to be trasfered. 1 : Transfer Y data only. Each bit represents each DMA channel	**0x00000000**
	FMT_CHAR_16	[15]			
	FMT_CHAR_15	[14]			
	FMT_CHAR_14	[13]			
	FMT_CHAR_13	[12]			
	FMT_CHAR_12	[11]			
	FMT_CHAR_11	[10]			
	FMT_CHAR_10	[9]			
	FMT_CHAR_9	[8]			
	FMT_CHAR_8	[7]			
	FMT_CHAR_7	[6]			
	FMT_CHAR_6	[5]			
	FMT_CHAR_5	[4]			
	FMT_CHAR_4	[3]			
	FMT_CHAR_3	[2]			
	FMT_CHAR_2	[1]			
	FMT_CHAR_1	[0]			
0x674	VIDEO_EN_17	[16]	R/W	Enable Video input signal Each bit represents each DMA channel	**0x0001FFFF**
	VIDEO_EN_16	[15]			
	VIDEO_EN_15	[14]			
	VIDEO_EN_14	[13]			
	VIDEO_EN_13	[12]			
	VIDEO_EN_12	[11]			
	VIDEO_EN_11	[10]			
	VIDEO_EN_10	[9]			
	VIDEO_EN_9	[8]			
	VIDEO_EN_8	[7]			
	VIDEO_EN_7	[6]			
	VIDEO_EN_6	[5]			
	VIDEO_EN_5	[4]			
	VIDEO_EN_4	[3]			
	VIDEO_EN_3	[2]			
	VIDEO_EN_2	[1]			
	VIDEO_EN_1	[0]			
0x678	Y_BURST	[7:0]	R/W	assign Y_Burst size ex) if Y_BURST[7:0] is 0x40, the Burst size of Y is 0x80	**0x00000040**
0x698	C_BURST	[7:0]	R/W	assign C_Burst size ex) if C_BURST[7:0] is 0x20, the Burst size of Y is 0x40	**0x00000020**

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x6C0	ODD_EN_17	[16]	R/W	Control odd field data of ODD DMA processing 0 = enable, 1 = disable Each bit represents each DMA channel	0x00000000
	ODD_EN_16	[15]			
	ODD_EN_15	[14]			
	ODD_EN_14	[13]			
	ODD_EN_13	[12]			
	ODD_EN_12	[11]			
	ODD_EN_11	[10]			
	ODD_EN_10	[9]			
	ODD_EN_9	[8]			
	ODD_EN_8	[7]			
	ODD_EN_7	[6]			
	ODD_EN_6	[5]			
	ODD_EN_5	[4]			
	ODD_EN_4	[3]			
	ODD_EN_3	[2]			
	ODD_EN_2	[1]			
	ODD_EN_1	[0]			
0x6C4	EVEN_EN_17	[16]	R/W	Conrol even field data of video DMA processing 0 = enable, 1 = disable Each bit represents each DMA channel	0x00000000
	EVEN_EN_16	[15]			
	EVEN_EN_15	[14]			
	EVEN_EN_14	[13]			
	EVEN_EN_13	[12]			
	EVEN_EN_12	[11]			
	EVEN_EN_11	[10]			
	EVEN_EN_10	[9]			
	EVEN_EN_9	[8]			
	EVEN_EN_8	[7]			
	EVEN_EN_7	[6]			
	EVEN_EN_6	[5]			
	EVEN_EN_5	[4]			
	EVEN_EN_4	[3]			
	EVEN_EN_3	[2]			
	EVEN_EN_2	[1]			
	EVEN_EN_1	[0]			

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x700	AUD_DMA_BA0_A	[31:0]	R/W	assigns Audio base address a to main memory space.	by cpu
0x704	AUD_DMA_BA0_B	[31:0]	R/W	assigns Audio base address a to main memory space.	by cpu
0x708	AUD_DMA_BA1_A	[31:0]	R/W	assigns Audio base address a to main memory space.	by cpu
0x70C	AUD_DMA_BA1_B	[31:0]	R/W	assigns Audio base address a to main memory space.	by cpu
0x710	AUD_DMA0_SIZE	[31:0]	R/W	Determines Audio DMA size to occur interrupt signal.	0x00003E80
0x714	AUD_DMA1_SIZE	[31:0]	R/W	Determines Audio DMA size to occur interrupt signal.	0x00003E80
0x718	AUD_BURST_SIZE	[15:0]	R/W	On DMA processing, This register determines a Audio burst size.	0x00000020
0x71C	reserved				-
0x720	Aud_DMA_CTRL	[0]	R/W	Enable Audio DMA processing. 1 = enable, 0 = disable.	0x00000001
0x724	AUD_IRQ_MASK	[3:0]	R/W	[0] : a Audio interrupt mask_a [1] : a Audio interrupt mask_b	0x00000003
0x728	AUD_IRQ_STS	[3:0]	RO	[0] : a Audio interrupt_a status [1] : a Audio interrupt_a status	-
0x72C	REMOTE_IRQ_MASK	[0]	R/W	Remote control interrupt mask	0x00000001
0x730	GPIO_DIR	[23:0]	R/W	Determines a direction of GPIO(General Purpose I/O) pin.	by cpu
0x734	GPIO_OUT	[23:0]	R/W	GPIO output	by cpu
0x738	GPIO_IN	[23:0]	RO	GPIO input	by cpu
0x73C	REMOTE_STS	[0]	RO	Remote control interrupt a status	-
0x740	GLOBAL_INT_MASK	[0]	R/W	Global interrupt mask(video + audio + remote interrupt mask)	0x00000001
0x744	GLOBAL_IRQ_STS	[2:0]	RO	[0] : video interrupt status [1] : audio interrupt status [2] : remote interrupt status	Read Only
0x750	I2C Port1	[5]	R/W	Determines direction of SDA_1(I2C Data1) Pin.	0x0
		[4]	R/W	Determines direction of SCL_1(I2C_Clock1) Pin	
		[3]	R/W	Input from SDA_1(I2C Data1) Pin	
		[2]	R/W	Input from SCL_1(I2C_Clock1) Pin	
		[1]	R/W	Output from SDA_1(I2C Data1) Pin	
		[0]	R/W	Output from SCL_1(I2C_Clock1) Pin	
0x754	I2C Port2	[5]	R/W	Determines direction of SDA_2(I2C Data2) Pin.	0x0
		[4]	R/W	Determines direction of SCL_2(I2C_Clock2) Pin	
		[3]	R/W	Input from SDA_2(I2C Data2) Pin	
		[2]	R/W	Input from SCL_2(I2C_Clock2) Pin	
		[1]	R/W	Output from SDA_2(I2C Data2) Pin	
		[0]	R/W	Output from SCL_2(I2C_Clock2) Pin	

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x760	RATE_16	[15]	RW	This register Generates Null interrupt signal in Rate Control and disable DMA Operation in the selected Channel.	0x00000000
	RATE_15	[14]	RW		
	RATE_14	[13]	RW		
	RATE_13	[12]	RW		
	RATE_12	[11]	RW		
	RATE_11	[10]	RW		
	RATE_10	[9]	RW		
	RATE_9	[8]	RW		
	RATE_8	[7]	RW		
	RATE_7	[6]	RW		
	RATE_6	[5]	RW		
	RATE_5	[4]	RW		
	RATE_4	[3]	RW		
	RATE_3	[2]	RW		
	RATE_2	[1]	RW		
	RATE_1	[0]	RW		
0x764	R_STS_16	[15]	RW	This register shows a status of Null interrupt in the selected Channel on the Rate Control Mode.	0x00000000
	R_STS_15	[14]	RW		
	R_STS_14	[13]	RW		
	R_STS_13	[12]	RW		
	R_STS_12	[11]	RW		
	R_STS_11	[10]	RW		
	R_STS_10	[9]	RW		
	R_STS_9	[8]	RW		
	R_STS_8	[7]	RW		
	R_STS_7	[6]	RW		
	R_STS_6	[5]	RW		
	R_STS_5	[4]	RW		
	R_STS_4	[3]	RW		
	R_STS_3	[2]	RW		
	R_STS_2	[1]	RW		
	R_STS_1	[0]	RW		

6.4 Audio Processor & Video Decoder Part

◆ Show Status of NVP1208 (Read Only)

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x018	DEV_ID	[31:24]	R	Show Internal Video Decoder Device ID (0x76)	**Read Only**
0x01C	REV_ID	[3:0]	R	Show Internal Video Decoder Revision ID (0x0)	**Read Only**

◆ Registers to Control Clock Delay of external device input clock

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x020	EX_DEC1_CLK_SEL4	[31:28]	R/W	From External 1st Decoder Out Clock Delay control for 8th channel	**0x00000004**
	EX_DEC1_CLK_SEL3	[27:24]		From External 1st Decoder Out Clock Delay control for 7th channel	
	EX_DEC1_CLK_SEL2	[23:20]		From External 1st Decoder Out Clock Delay control for 6th channel	
	EX_DEC1_CLK_SEL1	[19:16]		From External 1st Decoder Out Clock Delay control for 5th channel	
	VADC_CLK_SEL	[14:12]		Video ADC Sampling Clock Selection (108M OSC /54M OSC) 0 : 27MHz P1 / Don't use 1 : 27MHz P2 / Don't use 2 : 27MHz P3 / Don't use 3 : 27MHz P4 / Don't use 4 : Don't use / 27MHz P1 5 : Don't use / 27MHz P2 5 : Don't use / Don't use 7 : Don't use / Don't use	
	VDEC_CLK_SEL	[10:8]		Internal Video Decoder Clock Selection (108M OSC /54M OSC) 0 : 27MHz P1 / Don't use 1 : 27MHz P2 / Don't use 2 : 27MHz P3 / Don't use 3 : 27MHz P4 / Don't use 4 : Don't use / 27MHz P1 5 : Don't use / 27MHz P2 5 : Don't use / Don't use 7 : Don't use / Don't use	
	AADC_CLK_SEL	[4]		Audio ADC Sampling Clock Polarity Selection 0 : Positive 1 : Negative	
	AUD_CLK_SEL	[2:0]		Internal Audio Processor Clock Selection (108M OSC /54M OSC) 0 : Don't use / Don't use 1 : Don't use / Don't use 2 : Don't use / Don't use 3 : Don't use / Don't use 4 : 54MHz P1 / Don't use 5 : 54MHz P2 / Don't use 5 : Don't use / 54MHz P1 7 : Don't use / 54MHz P2	
0x024	EX_DEC3_CLK_SEL4	[31:28]	R/W	From External 3rd Decoder Out Clock Delay control for 16th channel	**0x0**
	EX_DEC3_CLK_SEL3	[27:24]		From External 3rd Decoder Out Clock Delay control for 15th channel	
	EX_DEC3_CLK_SEL2	[23:20]		From External 3rd Decoder Out Clock Delay control for 14th channel	
	EX_DEC3_CLK_SEL1	[19:16]		From External 3rd Decoder Out Clock Delay control for 13th channel	
	EX_DEC2_CLK_SEL4	[15:12]		From External 2nd Decoder Out Clock Delay control for 12th channel	
	EX_DEC2_CLK_SEL3	[11:8]		From External 2nd Decoder Out Clock Delay control for 11th channel	
	EX_DEC2_CLK_SEL2	[7:4]		From External 2nd Decoder Out Clock Delay control for 10th channel	
	EX_DEC2_CLK_SEL1	[3:0]		From External 2nd Decoder Out Clock Delay control for 9th channel	
0x028	EX_DEC3_LCLK_SEL	[31:28]	R/W	From External 3rd Decoder Out Clock Delay control for Live channel	**0x0**
	EX_DEC2_LCLK_SEL	[27:24]		From External 2nd Decoder Out Clock Delay control for Live channel	
	EX_DEC1_LCLK_SEL	[23:20]		From External 1st Decoder Out Clock Delay control for Live channel	
0x02C	SEP_MD	[15:14]	R/W	From External Decoder Time Multiplexed Data Separation Mode Selection 0 : 108MHz 4ch Time Multiplexed Data Separation 1 : 54MHz 2ch Time Multiplexed Data Separation	**0x0**

◆ Registers To Controls An Audio Interface

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x030	AIGAIN_04	[23:20]	R/W	Control the gain of analog audio input AIN1 ~ AIN4	0x00888802
	AIGAIN_03	[19:16]			
	AIGAIN_02	[15:12]			
	AIGAIN_01	[11:8]			
	AAFE_PD	[7]		Audio AFE Power Down Mode 0: Normal Operation 1: Power Down	
0x040	PB_MASTER	[31]	R/W	Set Master/Slave mode of ACLK_PB and ASYNC_PB 0: Slave mode 1 : Master mode	0x48E4FEDC
	PB_CLK	[30]	R/W	Set the relationship between audio signal inputted to ADATA_PB and clock inputted/outputed to ACLK_PB 0: inverted clock 1 : non-inverted clock	
	PB_SAMRATE	[27]	R/W	Set the sampleing rate of data inputted to ADATA_PB 0: 8KHz 1 : 16KHz	

◆ Registers To Controls An Audio Interface

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x060	DCA1	[23:16]	R/W	Set DC level LSB part of inputted audio signal through ADC	0x020002AA
	DCA0	[9:8]		Set DC level MSB part of inputted audio signal through ADC	

◆ Registers To Controls An Analog Front End

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x07C	NOVID_SPD	[21:16]	R/W	Novideo Detection Speed Control 0x10 -> 0x3F : More Slower Speed	0x00104304
	FLD_DET_SPD	[15:14]	R/W	Select the method to create the field information that will be externally output 0 : Middle 1 : Slow 2 : Fast 3 : Fastest	
	NOVID_MODE	[11:8]	R/W	Select Condition for No video detection, High Active NOVID_DET_B[0] : If the input video is not detected sync, turn on the NOVID signal NOVID_DET_B[1] : If Width of detected sync is narrower than video standard. turn on NOVID signal NOVID_DET_B[2] : If Vertical sync don't exist, turn on the NOVID signal NOVID_DET_B[3] : If the CLAMP is not stable, turn on the NOVID signal	

◆ Registers to Control Chrominance

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x0B4	ACC_OFF	[31]	R/W	Continue to a constant gain value for chroma signal. 0 : On 1 : Off	0x2FF0DC2A / 0x2FF0CC2A
	ACC_CORE_LVL	[29:28]	R/W	Adjust a coring level for ACC error. 00 : 0 01 : 4 10 : 8 11 : 16	
	ACC_GAIN_SPD	[27:24]	R/W	1 step value applied to the ACC Gain Accumulator (ACC Accumulator 1 Step value = 4 * ACC_GAIN_SPD + 2)	
	FSC_LOC_SENSE	[23:16]	R/W	Chroma Subcarrier frequency locking sensitivity control	

◆ Registers to Control Chrominance

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x0B8	CTI_GAIN	[31:24]	R/W	Adjust gain level for CTI. 00 : No Gain 11 : More larger gain	0x0FD38257 / 0x0FD30157
	CTI_DELAY_SEL	[21:20]	R/W	Adjust a delay between original color signal and value generated by CTI.	
	C_KILL	[19:16]	R/W	[19] : Color kill mode 0 : Color kill before Y/C seperation 1 : Color kill after Y/C seperation [18:16] : Color kill control 0 : Burst Amplitude 10% Under & FSC Unlock 1 : Burst Amplitude 5% Under & FSC Unlock 2 : Burst Amplitude 10% Under 3 : Burst Amplitude 5% Under 4 : Alway color on 5 : Alway color on 6 : Alway color off 7 : Alway color off	
	PAL_CM_OFF	[15]	R/W	PAL Compensation On/Off 0 : PAL Compensation applied 1 : PAL Compensation not applied.	
	IF_FIR_SEL	[14:12]	R/W	IF Filter drive mode selected 000 : Bypass 001 : mode1 010 : mode2 others : mode3	
	CLPF_SEL	[9:8]	R/W	Color low pass filter applied mode applied after demodulation 00 : Bypass 01 : 0.6M cutoff 10 : 1.0M cutoff 11 : 1.2M cutoff	

◆ Registers to Digital Video Interface

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x130 **0x134** **0x138**	DATA_SEL_#	4bit	R/W	Data Selection to PCI 0011 : Video Input Data 0111 : Internal Pattern data etc : Test Only	**0x3**
0x148	PAT_TYPE_8	[31:28]	R/W	Internal Pattern Type Selection 0000 : Color Bar Type 1 0001 : Color Bar Type 2 0010 : Color Bar Type 3 0011 : Color Bar Type 4 0100 : Fully White 0101 : Fully Yellow 0110 : Fully Cyan 0111 : Fully Green 1000 : Fully Red 1001 : Fully Blue 1010 : Fully Black etc : Test Only	**0x0**
	PAT_TYPE_7	[27:24]	R/W		
	PAT_TYPE_6	[23:20]	R/W		
	PAT_TYPE_5	[19:16]	R/W		
	PAT_TYPE_4	[15:12]	R/W		
	PAT_TYPE_3	[11:8]	R/W		
	PAT_TYPE_2	[7:4]	R/W		
	PAT_TYPE_1	[3:0]	R/W		
0x14C	PAT_TYPE_16	[31:28]	R/W		**0x0**
	PAT_TYPE_15	[27:24]	R/W		
	PAT_TYPE_14	[23:20]	R/W		
	PAT_TYPE_13	[19:16]	R/W		
	PAT_TYPE_12	[15:12]	R/W		
	PAT_TYPE_11	[11:8]	R/W		
	PAT_TYPE_10	[7:4]	R/W		
	PAT_TYPE_9	[3:0]	R/W		
0x150	PAT_TYPE_19	[11:8]	R/W		**0x0**
	PAT_TYPE_18	[7:4]	R/W		
	PAT_TYPE_17	[3:0]	R/W		

◆ Registers to Digital Video Interface

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x154	FV_60	[12]	R/W	Video Standard Selection for Internal Video Interface 0 : PAL 1 : NTSC	0x00001000 / 0x00000000
	LIVE_CH_SEL	[10:8]	R/W	Live video channel selection 000 : Internal ch1 001 : Internal ch2 010 : Internal ch3 011 : Internal ch4 100 : External Decoder #1 101 : External Decoder #2 110 : External Decoder #3 111 : Internal ch1	
	MV_CUR_COL	[7:4]	R/W	Internal Pattern Moving Cursor Color Selection 0000 : Color Bar Type 1 0001 : Color Bar Type 2 0010 : Color Bar Type 3 0011 : Color Bar Type 4 0100 : White 0101 : Yellow 0110 : Cyan 0111 : Green 1000 : Red 1001 : Blue 1010 : Black etc : Test Only	
	MV_CUR_SPD	[3:1]	R/W	Internal Pattern Moving Cursor Speed Control 000 → 111 more slower	
	MV_CUR_ON	[0]	R/W	Internal Pattern Moving Cursor On/Off Control 0 : Moving Cursor Off 1 : Moving Cursor On	
0x164 0x16C 0x174 0x17C 0x184	H_DTO#	[20:0]	R/W	For Horizontal direction, decide Ratio of scale NTSC/PAL : H scale = (H_DTO / 2^20) x 720	0x00100000
0x168 0x170 0x178 0x180 0x188	H_DEL#	[31:28]	R/W	When input is 704 pixel, decide H strat positin(0~15)	0x04100000
	UP#	[27]	R/W	According to only 720 pixel input, stretch the display size to 720 size 0 : No Expand 1 : Expand	
	SEL#	[26]	R/W	Decide to output between scale data and non-scale data which is same as bypass 0 : bypass an input data. 1 : output a scaled data	
	SYNG_ORG#	[24]	R/W	Decide H blank length between standard and variable one based on scale ratio 0 : Changed by a scale ratio. 1 : No changed by a scale ratio	
	V_DTO#	[20:0]	R/W	For Vertical direction, decide Ratio of scale NTSC : V scale = (V_DTO / 2^20) x 240 PAL : V scale = (V_DTO / 2^20) x 288	

◆ Registers to Internal Video Decoder

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x204	BSF_MODE_4	[31:30]	R/W	A register to determine the video standards of the input signal 00 : Mode0(1.3Mhz Cut-off) 01: Mode1(1.88Mhz Cut-off) 10 : Mode2(2.65Mhz Cut-off) 11: Mode3(2.5Mhz Cut-off)	0x55004040 / 0xAA004040
	BSF_MODE_3	[29:28]	R/W		
	BSF_MODE_2	[27:26]	R/W		
	BSF_MODE_1	[25:24]	R/W		
0x208	VIDEO_FORMAT_4	[28:24]	R/W	A register to determine the video standards of the input signal 00000 : NTSC-M,J 10001 : NTSC-4.43 11101 : PAL-B,D,G,H,I 10110 : PAL-M 11111 : PAL-Nc 10101 : PAL-60 Others : None	0x0 / 0x1D1D1D1D
	VIDEO_FORMAT_3	[20:16]	R/W		
	VIDEO_FORMAT_2	[12:8]	R/W		
	VIDEO_FORMAT_1	[4:0]	R/W		
0x20C	BRIGHTNESS_4	[31:24]	R/W	Brightness control; DC level of the Luma signal is adjustable up to -128 ~ +127. BRIGHTNESS consists of 2's Complements. 00000001 : +1 01111111 : +127 10000000 : -128 11111111 : -1	0x0
	BRIGHTNESS_3	[23:16]	R/W		
	BRIGHTNESS_2	[15:8]	R/W		
	BRIGHTNESS_1	[7:0]	R/W		
0x210	CONTRAST_4	[31:24]	R/W	Contrast control, Gain level of the Luma signal is adjustable up to x2. MSB represents an integral number while the rest the decimal fraction. 00000000 ≒ x0 10000000 ≒ x1 11000000 ≒ x1.5 11111111 ≒ x2	0x80808080
	CONTRAST_3	[23:16]	R/W		
	CONTRAST_2	[15:8]	R/W		
	CONTRAST_1	[7:0]	R/W		
0x214	SATURATION_4	[31:24]	R/W	Color Gain Value (Adjustable up to x2) 00000000 ≒ x0 10000000 ≒ x1 11000000 ≒ x1.5 11111111 ≒ x2	0x80808080
	SATURATION_3	[23:16]	R/W		
	SATURATION_2	[15:8]	R/W		
	SATURATION_1	[7:0]	R/W		
0x218	HUE_4	[31:24]	R/W	Color HUE Control Value (360°/256) 00000000 : 0° 01000000 : 90° 10000000 : 180° 11111111 : 360°	0x00000000
	HUE_3	[23:16]	R/W		
	HUE_2	[15:8]	R/W		
	HUE_1	[7:0]	R/W		
0x21C	U_GAIN_4	[31:24]	R/W	U Gain Value (Adjustable up to x2) 00000000 ≒ x1 01111111 ≒ x2 10000000 ≒ x0 11000000 ≒ x0.5	0x00000000
	U_GAIN_3	[23:16]	R/W		
	U_GAIN_2	[15:8]	R/W		
	U_GAIN_1	[7:0]	R/W		
0x220	V_GAIN_4	[31:24]	R/W	V Gain Value (Adjustable up to x2) 00000000 ≒ x1 01111111 ≒ x2 10000000 ≒ x0 11000000 ≒ x0.5	0x03030303
	V_GAIN_3	[23:16]	R/W		
	V_GAIN_2	[15:8]	R/W		
	V_GAIN_1	[7:0]	R/W		
0x224	U_OFFSET_4	[31:24]	R/W	U/V offset Value is adjustable up to ± 7. U/V OFFSET consists of 2's Complements. 00000001 : +1 01111111 : +127 10000000 : -128 11111111 : -1	0x00000000 / 0x04040404
	U_OFFSET_3	[23:16]	R/W		
	U_OFFSET_2	[15:8]	R/W		
	U_OFFSET_1	[7:0]	R/W		
0x228	V_OFFSET_4	[31:24]	R/W		
	V_OFFSET_3	[23:16]	R/W		
	V_OFFSET_2	[15:8]	R/W		
	V_OFFSET_1	[7:0]	R/W		

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x22C	VSYNC_INV4	[31]	R/W	Vertical Sync Signal Control, To inverse a phase of vsync	0x00006666 / 0x00007777
	VSYNC_INV3	[30]	R/W		
	VSYNC_INV2	[29]	R/W		
	VSYNC_INV1	[28]	R/W		
	HSYNC_INV4	[27]	R/W	Horizontal Sync Signal Control, To inverse a phase of hsync.	
	HSYNC_INV3	[26]	R/W		
	HSYNC_INV2	[25]	R/W		
	HSYNC_INV1	[24]	R/W		
	FPD_INV_4	[23]	R/W	Field Signal Control, To inverse a phase of field signal.	
	FPD_INV_3	[22]	R/W		
	FPD_INV_2	[21]	R/W		
	FPD_INV_1	[20]	R/W		
	PED_ON4	[19]	R/W	Pedestal On/Off 0 : Off 1 : On	
	PED_ON3	[18]	R/W		
	PED_ON2	[17]	R/W		
	PED_ON1	[16]	R/W		
	Y_FIR_MODE_4	[15:12]	R/W	[3:2] : Peaking Filter control, Luma 3.5MHz frequency bandwidth amplification 00 : bypass 01 : 2dB 10 : 3.5dB 11 : 6dB [1:0] : Y Low Pass Filter control 00 : bypass 01 : 4.2Mhz 10 : 5.6Mhz 11 : 7.2Mhz	
	Y_FIR_MODE_3	[11:8]	R/W		
	Y_FIR_MODE_2	[7:4]	R/W		
	Y_FIR_MODE_1	[3:0]	R/W		
0x230	Y_DELAY_4	[28:24]	R/W	Y/C DELAY Control, controllable between 0 ~ 32.	0x11111111
	Y_DELAY_3	[20:16]	R/W		
	Y_DELAY_2	[12:8]	R/W		
	Y_DELAY_1	[4:0]	R/W		
0x234	H_DELAY_4	[31:24]	R/W	Register to determine the Horizontal start position of output image to Hsync extracted in analog input signal.	0x30303030 / 0x56565656
	H_DELAY_3	[23:16]	R/W		
	H_DELAY_2	[15:8]	R/W		
	H_DELAY_1	[7:0]	R/W		
0x238	VDLY_EN4	[29]	R/W	Register to determine the Vertical start position of output image to Vsync extracted in analog input signal.(when, VDLY_EN# = 1)	0x1A1A1A1A / 0x1E1E1E1E
	V_DELAY_4	[28:24]	R/W		
	VDLY_EN3	[21]	R/W		
	V_DELAY_3	[20:16]	R/W		
	VDLY_EN2	[13]	R/W		
	V_DELAY_2	[12:8]	R/W		
	VDLY_EN1	[5]	R/W		
	V_DELAY_1	[4:0]	R/W		
0x23C	HBLK_END_4	[31:24]	R/W	Register to control Width of Horizontal Blanking, If user increments or decrements the value of this register, then the Active region is changed.	0x00000000
	HBLK_END_3	[23:16]	R/W		
	HBLK_END_2	[15:8]	R/W		
	HBLK_END_1	[7:0]	R/W		
0x240	VBLK_END_EN4	[29]	R/W	Register to control Width of Vertical Blanking. If user increments or decrements the value of this register, then the Active region is changed. (when, VBLK_END_EN# = 1)	0x07070707 / 0x0D0D0D0D
	VBLK_END_4	[28:24]	R/W		
	VBLK_END_EN3	[21]	R/W		
	VBLK_END_3	[20:16]	R/W		
	VBLK_END_EN2	[13]	R/W		
	VBLK_END_2	[12:8]	R/W		
	VBLK_END_EN1	[5]	R/W		
	VBLK_END_1	[4:0]	R/W		

ADDRESS	NAME	BIT	TYPE	DESCRIPTION	VALUE (NTSC/PAL)
0x25C	H_SHARPNESS_4	[31:28]	R/W	Selects the H_Sharpness Value to calculate the brightness information. It consists of four bits in total. MSB represents an integral number while the rest the decimal fraction. 0000 : 0 0100 : x0.5 1000 : x0 1111 : x2	0x80808080
	V_SHARPNESS_4	[27:24]	R/W	Selects the V_Sharpness Value to calculate the brightness information. It consists of four bits in total. MSB represents an integral number while the rest the decimal fraction. 0000 : 0 0100 : x0.5 1000 : x0 1111 : x2	
	H_SHARPNESS_3	[23:20]	R/W	Selects the H_Sharpness Value to calculate the brightness information. It consists of four bits in total. MSB represents an integral number while the rest the decimal fraction. 0000 : 0 0100 : x0.5 1000 : x0 1111 : x2	
	V_SHARPNESS_3	[19:16]	R/W	Selects the V_Sharpness Value to calculate the brightness information. It consists of four bits in total. MSB represents an integral number while the rest the decimal fraction. 0000 : 0 0100 : x0.5 1000 : x0 1111 : x2	
	H_SHARPNESS_2	[15:12]	R/W	Selects the H_Sharpness Value to calculate the brightness information. It consists of four bits in total. MSB represents an integral number while the rest the decimal fraction. 0000 : 0 0100 : x0.5 1000 : x0 1111 : x2	
	V_SHARPNESS_2	[11:8]	R/W	Selects the V_Sharpness Value to calculate the brightness information. It consists of four bits in total. MSB represents an integral number while the rest the decimal fraction. 0000 : 0 0100 : x0.5 1000 : x0 1111 : x2	
	H_SHARPNESS_1	[7:4]	R/W	Selects the H_Sharpness Value to calculate the brightness information. It consists of four bits in total. MSB represents an integral number while the rest the decimal fraction. 0000 : 0 0100 : x0.5 1000 : x0 1111 : x2	
	V_SHARPNESS_1	[3:0]	R/W	Selects the V_Sharpness Value to calculate the brightness information. It consists of four bits in total. MSB represents an integral number while the rest the decimal fraction. 0000 : 0 0100 : x0.5 1000 : x0 1111 : x2	

7. Electrical characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
1.8V Digital Power Supply Voltage	V_{POWER1}	1.65	1.8	1.95	V
1.8V Analog Power Supply Voltage	V_{DDA1}	1.65	1.8	1.95	V
3.3V Digital Power Supply Voltage	V_{POWER2}	3.0	3.3	3.6	V
Voltage on Any 1.8V input pins	V_{PIN1}	1.65	1.8	1.95	V
Voltage on Any 3.3V input pins	V_{PIN2}	3.0	3.3	3.6	V
Voltage on Any 5V input pins	V_{PIN5}	4.5	5	5.5	V
Storage Temperature	V_S	-40	-	125	℃
Junction Temperature	V_J	-40	-	125	℃
Vapor phase soldering (15 Sec)	V_{VSOL}	-	-	220	℃

7.2 Recommended Operating Condition

Parameter	Symbol	Min	Typ	Max	Unit
1.8V Digital Power Supply Voltage	V_{POWER1}	1.65	1.8	1.95	V
1.8V Analog Power Supply Voltage	V_{DDA1}	1.65	1.8	1.95	V
3.3V Digital Power Supply Voltage	V_{POWER2}	3.0	3.3	3.6	V
Ambient operating temperature	V_A	-10	-	80	℃

7.3 DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	VSSI-0.3	-	$0.3V_{POWER}$	V
Input High Voltage	V_{IH}	$0.7V_{POWER}$	-	V_{POWER}+0.3	V
Input Low Current (V_{IN} = VSS)	I_{IL}	-	-	-10	uA
Input High Current (VIN = V_{POWER})	I_{IH}	-	-	10	uA
Input Capacitance (f = 1Mhz, V_{IN} = 2.4V)	C_{IN}	-	-	10	pF
Output Low Voltage (I_{OL} = 8.0mA)	V_{OL}	-	-	0.4	V
Output High Voltage (I_{OH} = 11.9mA)	V_{OH}	2.4	-	V_{POWER}	V
Three-State Output Leakage Current	I_{OZ}	-	-	±10	uA
Output Capacitance	C_{OUT}	-	-	10	pF

7.4 AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Current					
1.8V Supply Current	I_{DD1}	-	TBD	-	mA
3.3V Supply Current	I_{DD2}	-	TBD	-	mA
PCI Clock					
PCI_CLK frequency	f_{CLK33}	-	33.0	-	MHz
PCI_CLK duty cycle	f_{DUTY}	45	-	55	%
PCI_CLK pulse width low	t_{PWL_CLK54}	15.0	-	-	nsec
PCI_CLK pulse width high	t_{PWH_CLK54}	15.0	-	-	nsec
SYSTEM Clock					
SYS_CLK frequency	f_{CLK27}	-	27/54/108	-	MHz
SYS_CLK duty cycle	f_{DUTY}	45	-	55	%
SYS_CLK pulse width low	t_{PWL_CLK54}	18/9/4.5	-	-	nsec
SYS_CLK pulse width high	t_{PWH_CLK54}	18/9/4.5	-	-	nsec
Host Interface Pins					
P_SCL frequency	f_{SCL}	-	-	6	PCI_CLK
P_SCL minimum pulse width low	t_{PWL_SCL}	6	-	-	PCI_CLK
P_SCL minimum pulse width high	t_{PWH_SCL}	4	-	-	PCI_CLK
P_SCL to P_SDA setup time	t_{IS_SDA}	2	-	-	PCI_CLK
P_SCL to P_SDA hold time	t_{IH_SDA}	2	-	-	PCI_CLK
P_SCL to P_SDA delay time	t_{OD_SDA}	-	-	6	PCI_CLK
P_SCL to P_SDA hold time	t_{OH_SDA}	3	-	-	PCI_CLK

8. System Application

8.1 Recommended NTSC Register

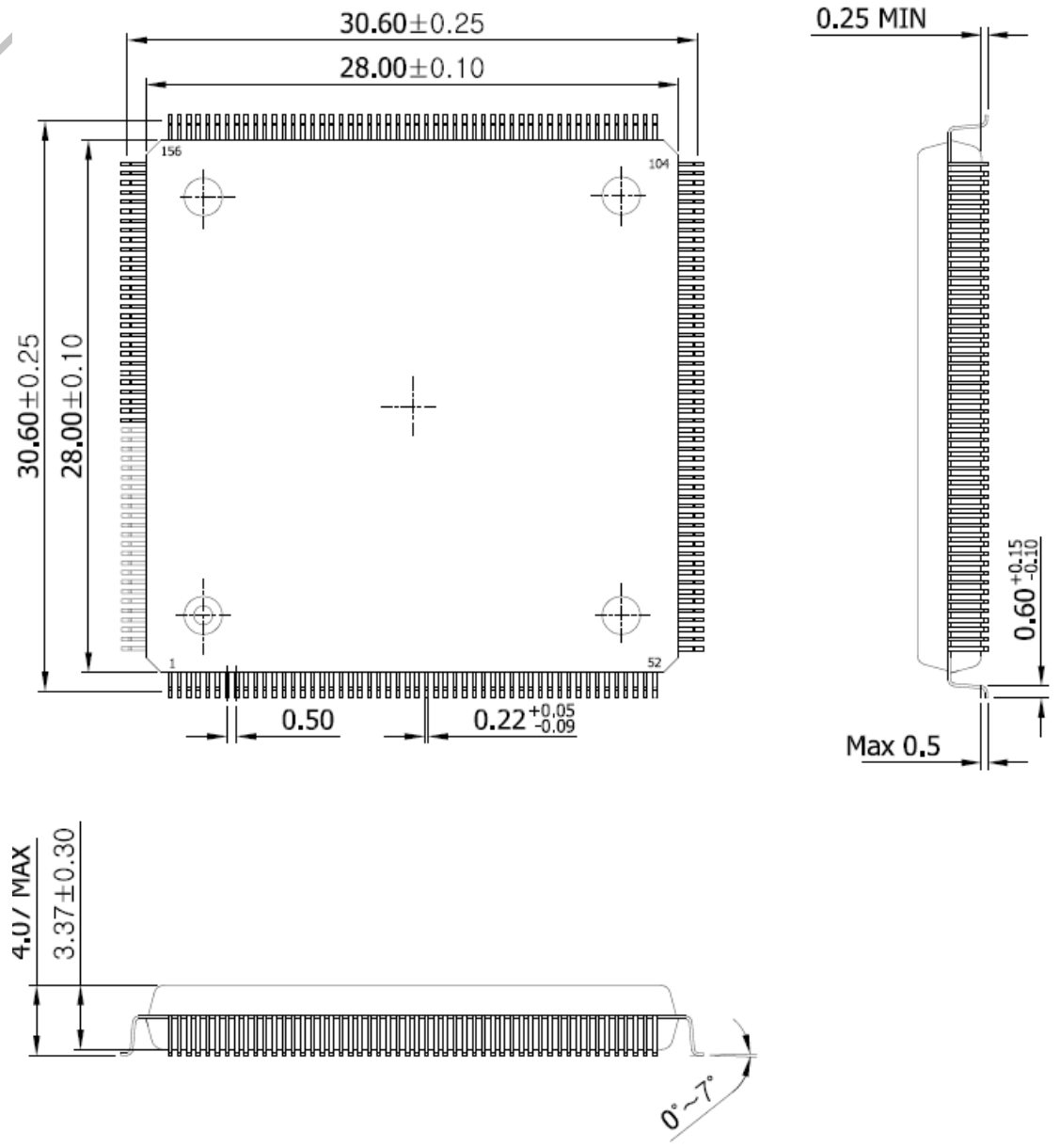
ADDRESS	VALUE	ADDRESS	VALUE	ADDRESS	VALUE	ADDRESS	VALUE	ADDRESS	VALUE	ADDRESS	VALUE	ADDRESS	VALUE
0x000	Read only	0x100	Null	0x200	40400000	0x400	By CPU	0x500	By CPU	0x600	Read Only	0x700	By CPU
0x004		0x104		0x204	55F04040	0x404		0x504		0x604		0x704	
0x008		0x108		0x208	00000000	0x408		0x508		0x608		0x708	
0x00C		0x10C		0x20C	00000000	0x40C		0x50C		0x60C		0x70C	
0x010		0x110		0x210	80808080	0x410				0x610		0x710	00007D00
0x014	Null	0x114		0x214	80808080	0x414				0x614	0001FFFF	0x714	Null
0x018	Read only	0x118		0x218	02020202	0x418				0x618	0001FFFF	0x718	00000020
0x01C		0x11C		0x21C	00000000	0x41C				0x61C	FFFFFFFF	0x71C	Null
0x020	00000004	0x120		0x220	03030303	0x420				0x620	02D002D0	0x720	00000000
0x024	00000000	0x124		0x224	00000000	0x424				0x624	02D002D0	0x724	00000000
0x028	00000000	0x128		0x228	00000000	0x428				0x628	02D002D0	0x728	00000000
0x02C	00000000	0x12C		0x22C	00006666	0x42C				0x62C	02D002D0	0x72C	00000001
0x030	00888802	0x130	33333333	0x230	11111111	0x430				0x630	02D002D0	0x730	By CPU
0x034	001A0000	0x134	33333333	0x234	30303030	0x434				0x634	02D002D0	0x734	
0x038	Null	0x138	00000333	0x238	3B3B3B3B	0x438				0x638	02D002D0	0x738	
0x03C		0x13C	00000000	0x23C	00000000	0x43C				0x63C	02D002D0	0x73C	00000000
0x040	48E4FEDC	0x140	00000000	0x240	28282828	0x440				0x640	000002D0	0x740	00000001
0x044	00000000	0x144	00000000	0x244	00000000	0x444				0x644	Null	0x744	Read Only
0x048	Null	0x148	99999999	0x248	00000000	0x448				0x648		0x748	Null
0x04C		0x14C	99999999	0x24C	00000000	0x44C				0x64C		0x74C	
0x050		0x150	00000999	0x250	00000000	0x450				0x650	00000000	0x750	0000003F
0x054		0x154	00001000	0x254	88883210	0x454				0x654	00000000	0x754	0000000F
0x058	000F0000	0x158	Null	0x258	00000000	0x458				0x658	00000000	0x758	00000000
0x05C	0000AAAA	0x15C		0x25C	80808080	0x45C				0x65C	00000000	0x75C	Null
0x060	020002AA	0x160	00000000			0x460				0x660	00000000	0x760	00000000
0x064	00000200	0x164	00100000			0x464				0x664	Null	0x764	00000000
0x068	3C550500	0x168	04100000			0x468				0x668		0x768	Null
0x06C	00070000	0x16C	00100000			0x46C				0x66C		0x76C	
0x070	6C4000D0	0x170	04100000			0x470				0x670	00000000	0x770	00000000
0x074	4020009F	0x174	00100000			0x474				0x674	0001FFFF	0x774	00000000
0x078	0F385080	0x178	04100000			0x478				0x678	00000080		
0x07C	00104304	0x17C	00100000			0x47C				0x67C	Null		
0x080	00B83000	0x180	04100000			0x480				0x680			
0x084	B9110606	0x184	00100000			0x484				0x684			
0x088	800005B2	0x188	04100000			0x488				0x688			
0x08C	37498037	0x18C	Null			0x48C				0x68C			
0x090	FFDFFFEF	0x190	Read Only			0x490				0x690			
0x094	Null	0x194				0x494				0x694			
0x098	800A1560	0x198				0x498				0x698	00000040		
0x09C	88010C80	0x19C				0x49C				0x69C	Null		
0x0A0	00000000	0x1A0				0x4A0				0x6A0			
0x0A4	80110180	0x1A4				0x4A4				0x6A4			
0x0A8	Null	0x1A8				0x4A8				0x6A8			
0x0AC	03008002	0x1AC				0x4AC				0x6AC			
0x0B0	00230000					0x4B0				0x6B0			
0x0B4	2FF0DC2A					0x4B4				0x6B4			
0x0B8	0FD38257					0x4B8				0x6B8	0020082D		
0x0BC	009D501F					0x4BC				0x6BC	Null		
0x0C0	30000000					0x4C0				0x6C0	0000220B		
0x0C4	0007001A					0x4C4				0x6C4	00000000		
0x0C8	09800068					0x4C8				0x6C8	00000000		
0x0CC	A243E010					0x4CC				0x6CC	00000000		
0x0D0	25150000					0x4D0				0x6D0	00000000		
0x0D4	00030300					0x4D4				0x6D4	00000000		
0x0D8	00321001					0x4D8				0x6D8	Read Only		
0x0DC	003FED00					0x4DC				0x6DC	00004444		
0x0E0	B5510000					0x4E0							
0x0E4	FF220313					0x4E4							
0x0E8	00000000					0x4E8							
0x0EC	0000008D					0x4EC							
0x0F0	10200000					0x4F0							
0x0F4	Null					0x4F4							
0x0F8						0x4F8							
0x0FC	10000000					0x4FC							

8.2 Recommended PAL Register

ADDRESS	VALUE	ADDRESS	VALUE	ADDRESS	VALUE	ADDRESS	VALUE	ADDRESS	VALUE	ADDRESS	VALUE	ADDRESS	VALUE
0x000	Read only	0x100	Null	0x200	40400000	0x400	By CPU	0x500	By CPU	0x600	Read Only	0x700	By CPU
0x004		0x104		0x204	AAF04040	0x404		0x504		0x604		0x704	
0x008		0x108		0x208	1D1D1D1D	0x408		0x508		0x608		0x708	
0x00C		0x10C		0x20C	00000000	0x40C		0x50C		0x60C		0x70C	
0x010		0x110		0x210	80808080	0x410				0x610		0x710	00007D00
0x014	Null	0x114		0x214	80808080	0x414				0x614	0001FFFF	0x714	Null
0x018	Read only	0x118		0x218	00000000	0x418				0x618	0001FFFF	0x718	00000020
0x01C		0x11C		0x21C	00000000	0x41C				0x61C	FFFFFFFF	0x71C	Null
0x020	00000004	0x120		0x220	03030303	0x420				0x620	02D002D0	0x720	00000000
0x024	00000000	0x124		0x224	04040404	0x424				0x624	02D002D0	0x724	00000000
0x028	00000000	0x128		0x228	04040404	0x428				0x628	02D002D0	0x728	00000000
0x02C	00000000	0x12C		0x22C	00007777	0x42C				0x62C	02D002D0	0x72C	00000001
0x030	00888802	0x130	33333333	0x230	11111111	0x430				0x630	02D002D0	0x730	By CPU
0x034	001A0000	0x134	33333333	0x234	54545454	0x434				0x634	02D002D0	0x734	
0x038	Null	0x138	00000333	0x238	1E1E1E1E	0x438				0x638	02D002D0	0x738	
0x03C		0x13C	00000000	0x23C	00000000	0x43C				0x63C	02D002D0	0x73C	00000000
0x040	48E4FEDC	0x140	00000000	0x240	0D0D0D0D	0x440				0x640	000002D0	0x740	00000001
0x044	00000000	0x144	00000000	0x244	00000000	0x444				0x644	Null	0x744	Read Only
0x048	Null	0x148	00000000	0x248	00000000	0x448				0x648		0x748	Null
0x04C		0x14C	00000000	0x24C	00000000	0x44C				0x64C		0x74C	
0x050		0x150	00000000	0x250	00000000	0x450				0x650	00000000	0x750	0000003F
0x054		0x154	00000000	0x254	88883210	0x454				0x654	00000000	0x754	0000000F
0x058	000F0000	0x158	Null	0x258	00000000	0x458				0x658	00000000	0x758	00000000
0x05C	0000AAAA	0x15C		0x25C	80808080	0x45C				0x65C	00000000	0x75C	Null
0x060	020002AA	0x160	00000000			0x460				0x660	00000000	0x760	00000000
0x064	00000200	0x164	00100000			0x464				0x664	Null	0x764	00000000
0x068	3C550500	0x168	04100000			0x468				0x668		0x768	Null
0x06C	00070000	0x16C	00100000			0x46C				0x66C		0x76C	
0x070	6C4000D0	0x170	04100000			0x470				0x670	00000000	0x770	00000000
0x074	4020009F	0x174	00100000			0x474				0x674	0001FFFF	0x774	00000000
0x078	0F385080	0x178	04100000			0x478				0x678	00000080		
0x07C	00104304	0x17C	00100000			0x47C				0x67C	Null		
0x080	00D83000	0x180	04100000			0x480				0x680			
0x084	B9110606	0x184	00100000			0x484				0x684			
0x088	800005B2	0x188	04100000			0x488				0x688			
0x08C	37498037	0x18C	Null			0x48C				0x68C			
0x090	FFDFFFEF	0x190	Read Only			0x490				0x690			
0x094	Null	0x194				0x494				0x694			
0x098	800A15BD	0x198				0x498				0x698	00000040		
0x09C	88010C80	0x19C				0x49C				0x69C	Null		
0x0A0	00000000	0x1A0				0x4A0				0x6A0			
0x0A4	80110180	0x1A4				0x4A4				0x6A4			
0x0A8	Null	0x1A8				0x4A8				0x6A8			
0x0AC	03008000	0x1AC				0x4AC				0x6AC			
0x0B0	00230404					0x4B0				0x6B0			
0x0B4	2FF0CC2A					0x4B4				0x6B4			
0x0B8	0FD30157					0x4B8				0x6B8	0020082D		
0x0BC	0080501F					0x4BC				0x6BC	Null		
0x0C0	40000000					0x4C0				0x6C0	00000000		
0x0C4	000D001E					0x4C4				0x6C4	00000000		
0x0C8	09800068					0x4C8				0x6C8	00000000		
0x0CC	A243E000					0x4CC				0x6CC	00000000		
0x0D0	25170000					0x4D0				0x6D0	00000000		
0x0D4	00020200					0x4D4				0x6D4	00000000		
0x0D8	00321011					0x4D8				0x6D8	Read Only		
0x0DC	003FED00					0x4DC				0x6DC	00004444		
0x0E0	A8510000					0x4E0							
0x0E4	FF220313					0x4E4							
0x0E8	00000000					0x4E8							
0x0EC	0000008D					0x4EC							
0x0F0	10200000					0x4F0							
0x0F4	Null					0x4F4							
0x0F8						0x4F8							
0x0FC	10000000					0x4FC							

8.3 Package Information

Dimensions in millimeters



9. Package Information

REV	Date	Description
Preliminary 0.0	2010.12.14.	· Generated

10. Contact Information

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