![WSI logo]

WAFERSCALE INTEGRATION, INC.

HIGH SPEED 8K × 8 CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  — 35 ns
- **Low Power Consumption**
- **Fast Programming**
- **DESC SMD 5962-87515**

- **Pin Compatible with AM27S49 and MB7144 Bipolar PROMs**
- **Immune to Latch-Up**
  — Up to 200 mA
- **ESD Protection Exceeds 2000V**

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GENERAL DESCRIPTION

The WS57C49B is an extremely HIGH PERFORMANCE 64K UV Erasable Electrically Re-Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts.

A further advantage of the WS57C49B over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This allows the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C49B is 100% tested with worst case test patterns both before and after assembly.

A unique feature of the WS57C49B is a designed-in output hold from address change. This allows the WS57C49B to be run at a cycle time equal to the address access time. While addresses are changing, output data is held long enough to be latched into external circuitry.

The WS57C49B is configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs.

MODE SELECTION

PINS \ MODE	$\overline{CS1}/V_{PP}$	V_{CC}	OUTPUTS
Read	V_{IL}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	V_{CC}	High Z
Program	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{CC}	D_{OUT}

PIN CONFIGURATION

TOP VIEW

Chip Carrier — CERDIP/Plastic DIP/Flatpack
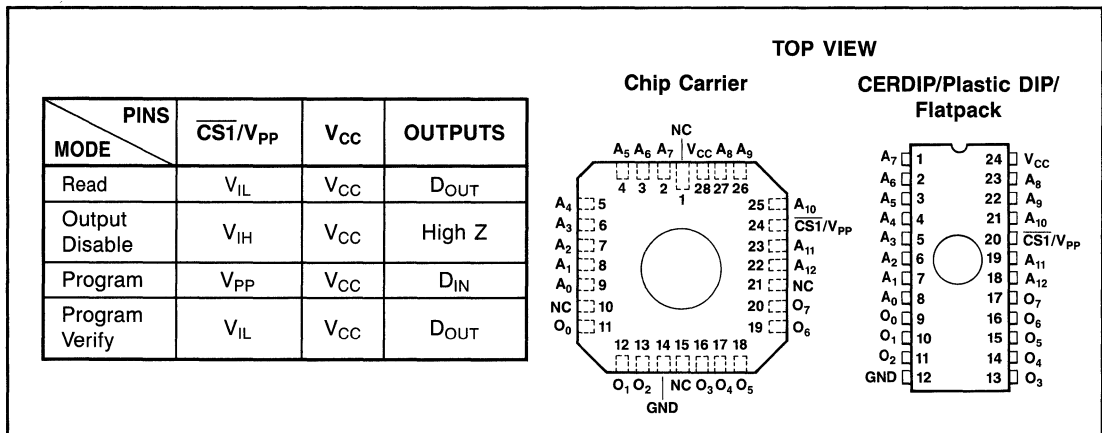
PRODUCT SELECTION GUIDE

PARAMETER	WS57C49B-35	WS57C49B-45	WS57C49B-55	WS57C49B-70
Address Access Time (Max)	35 ns	45 ns	55 ns	70 ns
Output Enable Time (Max)	20 ns	25 ns	25 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . −65°C to +150°C
Voltage on Any Pin with
   Respect to Ground . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . −0.6V to +14V
ESD Protection . . . . > 2000V

*Notice: Stresses above those listed under ''Absolute Maximum Ratings'' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Industrial	−40° to +85°C	+5V ± 10%
Military	−55° to +125°C	+5V ± 10%

## DC READ CHARACTERISTICS Over Operating Range. (See Above)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		
I_{CC1}	V_{CC} Active Current (CMOS)	Notes 1 and 3	Comm'l		30	mA
			Military		35	
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 3	Comm'l		40	
			Military		40	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	

NOTES: 1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.   3. Add 3 mA/MHz for A.C. power component.
         2. TTL inputs: V_{IL} ⩽ 0.8V, V_{IH} ⩾ 2.0V.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	57C49B-35		57C49B-45		57C49B-55		57C49B-70		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		45		55		70	ns
$\overline{CS}$ to Output Delay	t_{CS}		20		25		25		25	
Output Disable to Output Float	t_{DF}		25		25		25		25	
Address to Output Hold	t_{OH}	0		0		0		0		

AC READ TIMING DIAGRAM
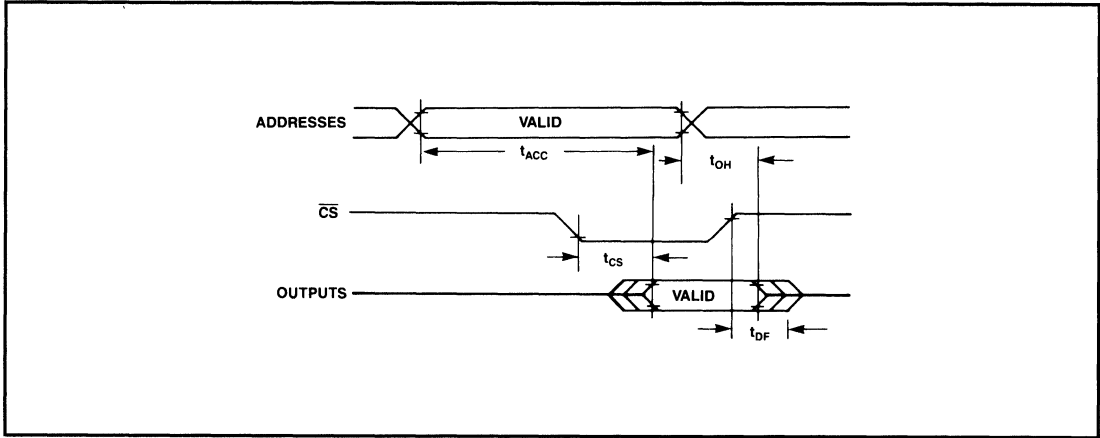
CAPACITANCE[4] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)   ## TIMING LEVELS
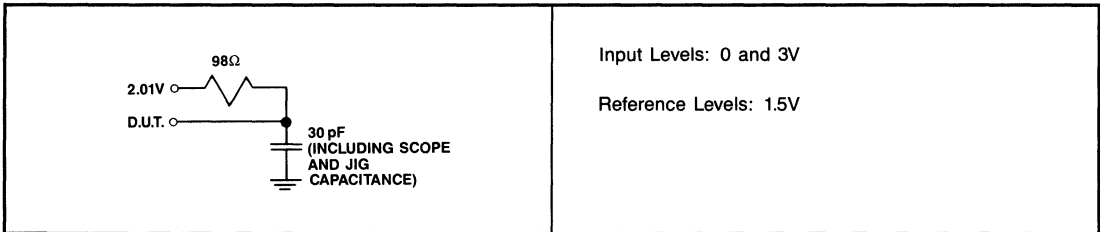
Input Levels: 0 and 3V

Reference Levels: 1.5V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 13.5 ± 0.5V)

| PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current V_{IN} = V_{CC} or Gnd	I_{LI}	−10	10	μA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		35	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

NOTE: 6 V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			μs
Chip Disable Setup Time	t_{DF}			30	ns
Data Setup Time	t_{DS}	2			μs
Program Pulse Width	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			μs
Chip Select Delay	t_{CS}			30	ns
V_{PP} Rise and Fall Time	t_{RF}	1			μs

NOTE: A single shot programming algorithm should use one 10 ms pulse.

PROGRAMMING WAVEFORM
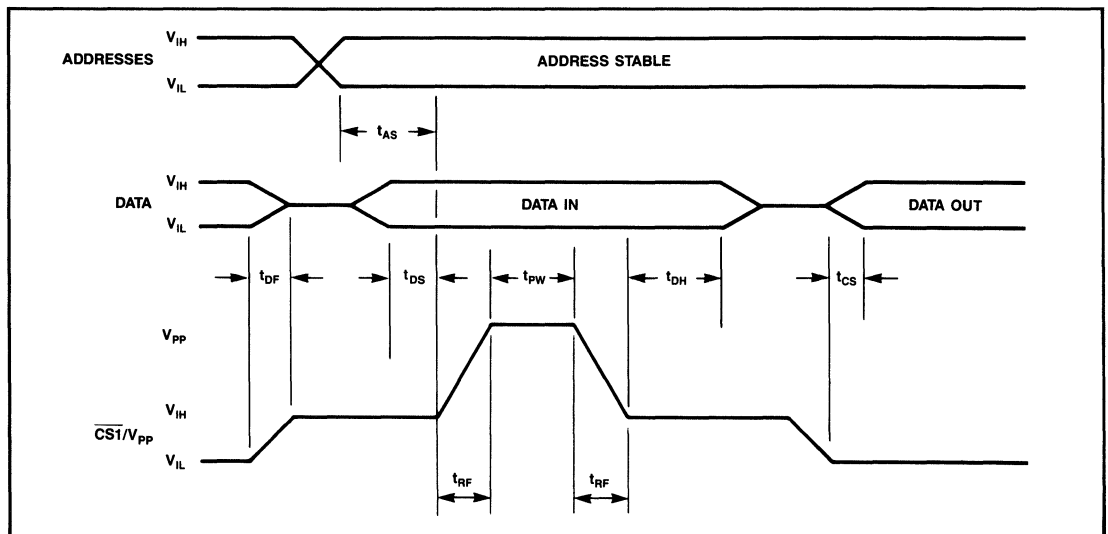
PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C49B-35D	35	24 Pin CERDIP, 0.6″	D1	Comm'l	Standard
WS57C49B-35J	35	28 Pin PLDCC	J3	Comm'l	Standard
WS57C49B-35P	35	24 Pin Plastic DIP, 0.6″	P2	Comm'l	Standard
WS57C49B-35T	35	24 Pin CERDIP, 0.3″	T1	Comm'l	Standard
WS57C49B-45CMB	45	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C49B-45D	45	24 Pin CERDIP, 0.6″	D1	Comm'l	Standard
WS57C49B-45DI	45	24 Pin CERDIP, 0.6″	D1	Industrial	Standard
WS57C49B-45DMB	45	24 Pin CERDIP, 0.6″	D1	Military	MIL-STD-883C
WS57C49B-45J	45	28 Pin PLDCC	J3	Comm'l	Standard
WS57C49B-45P	45	24 Pin Plastic DIP, 0.6″	P2	Comm'l	Standard
WS57C49B-45S	45	24 Pin Plastic DIP, 0.3″	S1	Comm'l	Standard
WS57C49B-45T	45	24 Pin CERDIP, 0.3″	T1	Comm'l	Standard
WS57C49B-45TI	45	24 Pin CERDIP, 0.3″	T1	Industrial	Standard
WS57C49B-45TMB	45	24 Pin CERDIP, 0.3″	T1	Military	MIL-STD-883C
WS57C49B-55CMB	55	28 Pad CLLCC	C1	Military	STD-MIL-883C
WS57C49B-55D	55	24 Pin CERDIP, 0.6″	D1	Comm'l	Standard
WS57C49B-55DMB	55	24 Pin CERDIP, 0.6″	D1	Military	MIL-STD-883C
WS57C49B-55FMB	55	24 Pin Ceramic Flatpack	F1	Military	MIL-STD-883C
WS57C49B-55T	55	24 Pin CERDIP, 0.3″	T1	Comm'l	Standard
WS57C49B-55TMB	55	24 Pin CERDIP, 0.3″	T1	Military	MIL-STD-883C
WS57C49B-70CMB	70	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C49B-70D	70	24 Pin CERDIP, 0.6″	D1	Comm'l	Standard
WS57C49B-70DMB	70	24 Pin CERDIP, 0.6″	D1	Military	MIL-STD-883C
WS57C49B-70T	70	24 Pin CERDIP, 0.3″	T1	Comm'l	Standard
WS57C49B-70TMB	70	24 Pin CERDIP, 0.3″	T1	Military	MIL-STD-883C

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