MOTOROLA

MCM68A30A
MCM68B30A

MOS
IN-CHANNEL, SIL ICON-GATE)

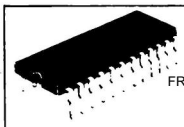
1024 X 8-BIT
READ ONLY MEMORY

1024 X 8-BIT READ ONLY MEMORY

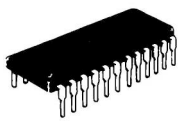
The MCM68A30A/MCM68B30A are mask-programmable byte-organized memories designed for use in bus-organized systems. They are fabricated with hl-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are defined by the customer.

- Organized as 1024 Bytes of 8 Bits
- Static Operation
- Three-State Data Output
- Four Chip Select Inputs (Programmable)
- Single ± 10% 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 350 ns — MCM68A30A
  250 ns - MCM68B30A

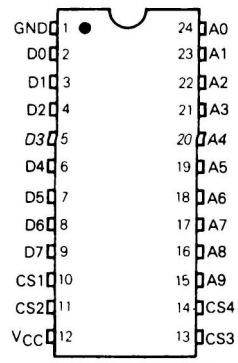


C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623-04



P SUFFIX
PLASTIC PACKAGE
CASE 709-02

PIN ASSIGNMENT

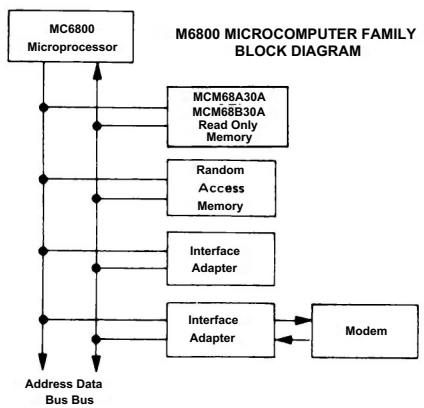


ABSOLUTE MAXIMUM RATINGS (See Note 1)

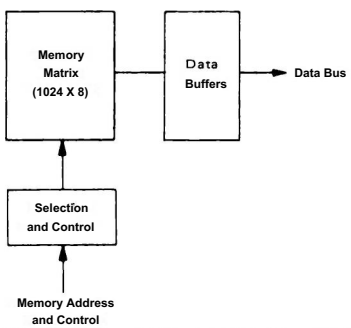
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to + 7 0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	Tstg	**-65 to +150**	°C

NOTE 1 Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



MCM68A30A/MCM68B30A READ ONLY MEMORY BLOCK DIAGRAM



DS9456 R1/6-78

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V | H	2.0	-	5.5	Vdc
Input Low Voltage	V_{IL}	-0.3	-	0.8	Vdc

DC CHARACTERISTICS

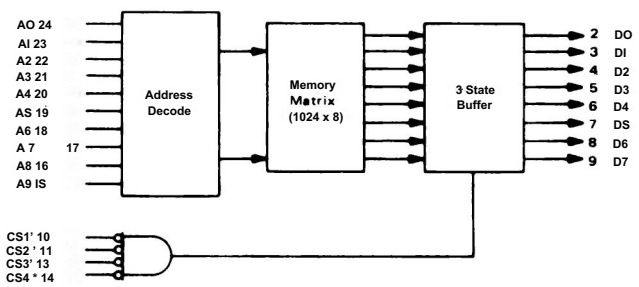
Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (V_{in} = Oto 5.5V)	* m	-	-	2.5	MAdc
Output High Voltage (|QH =~205мA)	V_{OH}	2.4	-	-	Vdc
Output Low Voltage (10L ' 1 6 mA)	V_{OL}	--	-	0.4	Vdc
Output Leakage Current (Three State) (CS = 0.8 V or $\overline{CS}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	^{1}LO	-	-	10	MAdc
Supply Current (V_{CC} = 5.5 V, T_A = 0°C)	'CC	--	-	130	mAdc

CAPACITANCE (f - 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance	Gin	7.5	pF
Output Capacitance	^{c}out	12.5	pF

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

BLOCK DIAGRAM



'Active level defined by the customer.

V_{CC} = pin 12
Gnd = Pin 1

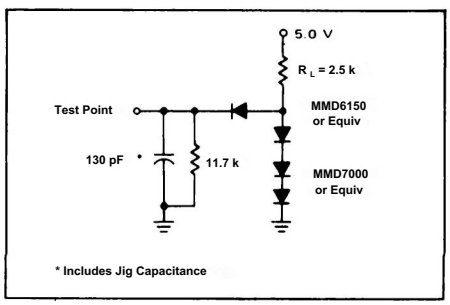
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

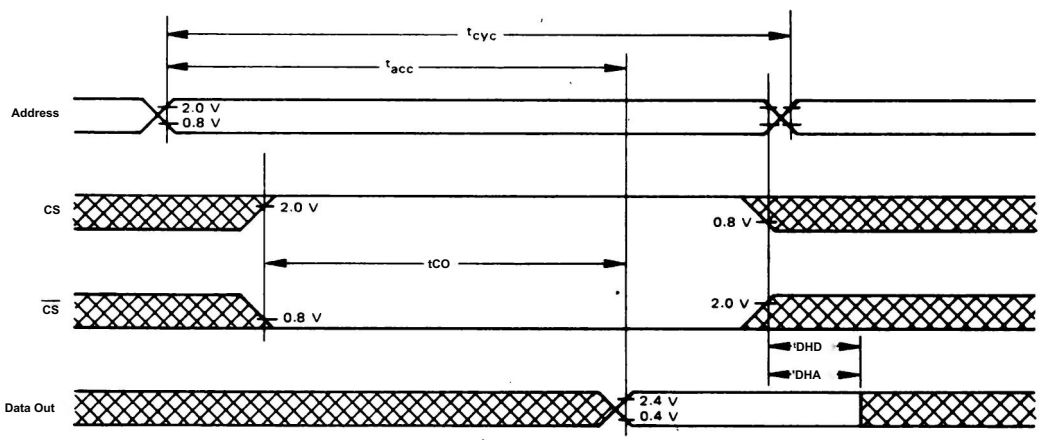
(All timing with t_r = tf = 20 ns. Load of Figure 1)

Characteristic	Symbol	MCM68A30AL		MCM68B30AL		Unit
		Min	Max	Min	Max	
Cycle Time	tcyc	350	-	250	-	ns
Access Time	tacc	-	350	—	250	ns
Chip Select to Output Delay	tco	-	150	—	125	ns
Data Hold from Address	tDHA	10	—	10	-	ns
Data Hold from Deselection	tDHD	10	150	10	125	ns

FIGURE 1 - AC TEST LOAD



TIMING DIAGRAM



CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68A30A/MCM68B30A, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM68A30A/MCM68B30A should be submitted on an Organizational Data form such as that shown in Figure 3. ("No Connect" must always be the highest order Chip Select pm(s).)

Information for custom memory content may be sent to Motorola in one of four forms (shown in order of preference):

1. Paper tape'output of the Motorola M6800 Software.
2. Hexadecimal coding using IBM Punch Cards.
3. EPROM (MCM2708, MCM27A08, or MCM68708).
4. Hand-punched paper tape (Figure 3).

PAPER TAPE

Included in the software packages developed for the M6800 Microcomputer Family is the ability to produce a paper tape output for computerized mask generation. The assembler directives are used to control allocation of memory, to assign values for stored data, and for controlling the assembly process. The paper tape must specify the full 1024 bytes.

FIGURE 2 - BINARY TO HEXADECIMAL CONVERSION

Binary Data				Hexadecimal Character
0	0	0	o	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	v	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	8
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

IBM PUNCH CARDS

The hexadecimal equivalent (from Figure 2) may be placed on 80 column IBM punch cards as follows:

Step	Column	
1	12	Byte "0" Hexadecimal equivalent for outputs D7 thru D4 (D7 = M.S.B.)
2	13	Byte "0" Hexadecimal equivalent for outputs D3 thru DO (D3 = M.S.B.)
3	14-75	Alternate steps 1 and 2 for consecutive bytes.
4	77-80	Card number (starting 0001)

FIGURE 3 - HAND-PUNCHED PAPER TAPE FORMA

Frames	
Leader	Blank Tape
1 toM	Allowed for customer use (M < 64)
M + 1, M + 2	CR; LF (Carriage Return; Line Feed)
M + 3 to M + 66	First line of pattern information (64 hex figures per line)
M + 67, M + 68	CR; LF
M + 69 to M + 2112	Remaining 31 lines of hex figures, each line followed by a Carriage Return and Line Feed

Blank Tape

Frames 1 to M are left to the customer for internal identification, where M <64. Any combination of alpha-numerics may be used. This information is terminated with a Carriage Return and Line Feed, delineating the start of data entry. (Note that the tape cannot begin with a CR and/or LF, or the customer identification will be assumed to be programming data.)

Option A (1024 x 8)

Frame M + 3 contains the hexadecimal equivalent of bits D7 thru D4 of byte 0. Frame M + 4 contains bits D3 thru DO. These two hex figures together program byte 0. Likewise, frames M + 5 and M + 6 program byte 1, while M + 7 and M + 8 program byte 2. Frames M + 3 to M + 66 comprise the first line of the printout and program, in sequence, the first 32 bytes of storage. The line is terminated with a CR and LF.

Option B (2048 x 4)

Frame M + 3 contains the hexadecimal equivalent of byte 0, bits D3 thru DO. Frame M + 4 contains byte 1, frame M + 5 byte 2. and so on. Frames M + 3 to M + 66 sequentially program bytes 0 to 31 (the first 32 bytes). The line is terminated with a CR and LF.

Both Options

The remaining 31 lines of data are punched in sequence using the same format, each line terminated with a CR and LF. The total 32 lines of data contain 32 x 64 or 2048 characters. Since each character programs 4 bits of information, a full 8192 bits are programmed.

As an example, a printout of the punched tape for Figure 13 would read as shown in Figure 10 (a CR and LF is implicit at the end of each line).

FIGURE 4 - FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68A30A/68B30A MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originate r _____

Phone No. _____

Motorola Use Only:

Quote: _____

Part No .: _____

Specif. No. : _____

Chip Select Options:

	Active High	Active Low	No Connect "Don't Care"
CS1	☐	☐	☐
CS2	☐	☐	☐
CS3	☐	☐	☐
CS4	☐	☐	☐