

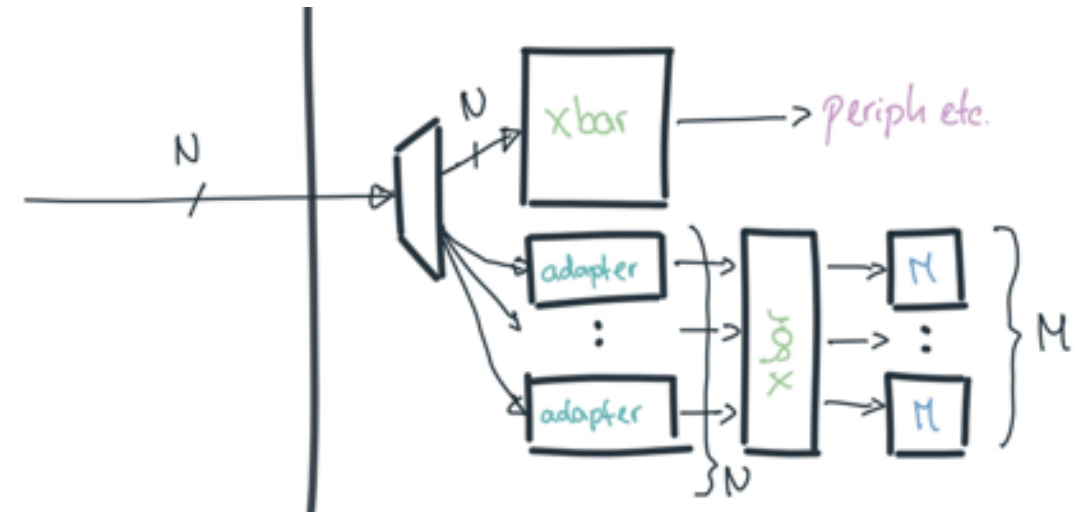
MemPool meets Systolic

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Multi-banked L2

- Merged into GitHub
 - Dedicated adapter for each group/axi channel
 - Crossbar after adapter allows interleaved memory
 - Easy to have parallel accesses
- Backend WIP



DMA

- Front-end integrated
- Single back-end integrated to get first working transfer
- Next step:
 - Mid-end
 - Backend

