Design of hybrid Vedic Multiplier for efficiency

Biplab Das S
Department of Electronics and Communication Engineering, Sri Shakthi Institute of Engineering and Technology
Coimbatore, Tamil Nadu 641062, India
biplabdas2001.bd@gmail.com

Abstract—This paper talks discusses feasibility of the so-called efficiency in power, area, and speed in the hybrid 4-bit Vedic multiplier using the ancient algorithm called Urdhva Tiryakbhayam Sutra. The entire design is implemented using the SkyWater 130nm pdk node files containing various methodologies like GDI, PTL, and DPL in CMOS structure.
Keywords—*Vedic Multiplier, Urdhva Tiryakbhayam, mGDI, SkyWater 130nm process.*

I. INTRODUCTION

In this era, energy efficiency is critical, so in the semiconductor field, approaches from Moore's law of transistors deal with the best attributes, creating a question in future power and area. In this work, the assumption of getting an increased throughput is more likely to be essential in this research, improving the processor's core.

II. DESIGN OVERVIEW

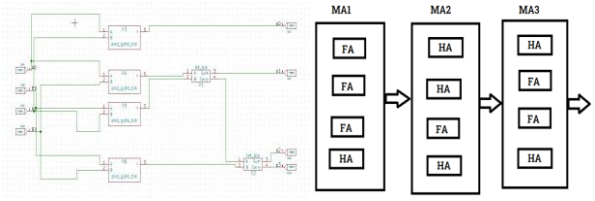
This design integrates a novel approach to the efficiency for any wireless technologies-DSP, computational chips and hardware. Comprising the SkyWater 130nm node files and the blocks of Vedic multiplier inside, Urdhva Tiryakbhayam Sutra (Vertically and Crosswire) for the 4-bit multiplication is used with the help of various methodologies in the existing papers, such as Conventional counts of transistors, speed coverage, delay optimization, area and power consumption.

A. mGDI:

Modified Gate Diffusion Input (GDI) is a technique for implementing various designs using transistors in a lesser count. Advantages like enhanced performance compared to GDI, PTL, DPL, Signal Integrity, etc., signify pivotal changes in the design of complex architectures. Unlike the other methodologies, mGDI proves to be better in parallel computations, has reduced hardware, and is feasible in swings.

B. Basic Gates and Adders

The crucial part of any design, including multipliers, is the logic counts. In Vedic multiplication, the modern requirements for the gates are lesser compared to conventional tape-outs. From the perceptions and observations of [3], the AND gate has a 4T count; from [4], the Half Adder has a 6T count added to the design. Compared to the [1] implementations, the swings, gate counts, and signal integrity levels tend to amplify more with the mGDI methodology.



(a) (b)

Fig 1. Overview of (a) 2-bit Vedic Multiplier Gates & (b) Modified Adders

With this methodology, the full adder of 8T from [2] LCAFA4 has increased performance due to the full swing from the bulk to power levels. Therefore. We get to see Sum = A ⊕ B ⊕ C and Cout = C as a result for FA.

C. Modified Adders

The Modified Adders, aka MA1, 2, 3 from Fig 1 (b), are used to use the bits multiplication carefully. Therefore, the sophisticated idea solves the extra bits that may follow in future definitions of floating and fixed points or signed and unsigned numbers.

III. IMPLEMENTATION

The implementation is carried out with the open source packages of SkyWater 130nm pdk process, which is the kludging of the previous designs, and 4-bit multiplication is achieved. The whole idea of input of 4 bits is converted to the output of 8 bits, utilising the multiplier bit A and multiplicands B from Fig 1 (a), respectively.

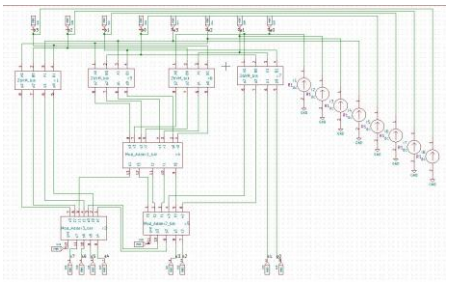


Fig 2. Overview of the proposed 4-bit Vedic Multiplier

IV. ISSUES AND IMPROVEMENTS

After these keen observations from the existing papers, this proposed design provides a valid performance to its full output swing compared to the other methodologies. The issues raised were the transistor counts and the area consumption, which is quite unavoidable for hardware costs.

V. CONCLUSION AND FUTURE SCOPE

The architecture substantially gives a novelty in research regarding hardware that comes out as a fully expedited tape-out. As far as the concerns of efficiency, this has the value of solving complexities in timing in deeper conditions of process nodes and other parameters, upgradations in the field of processing throughput, and excellent solutions in terms of power and savings.

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