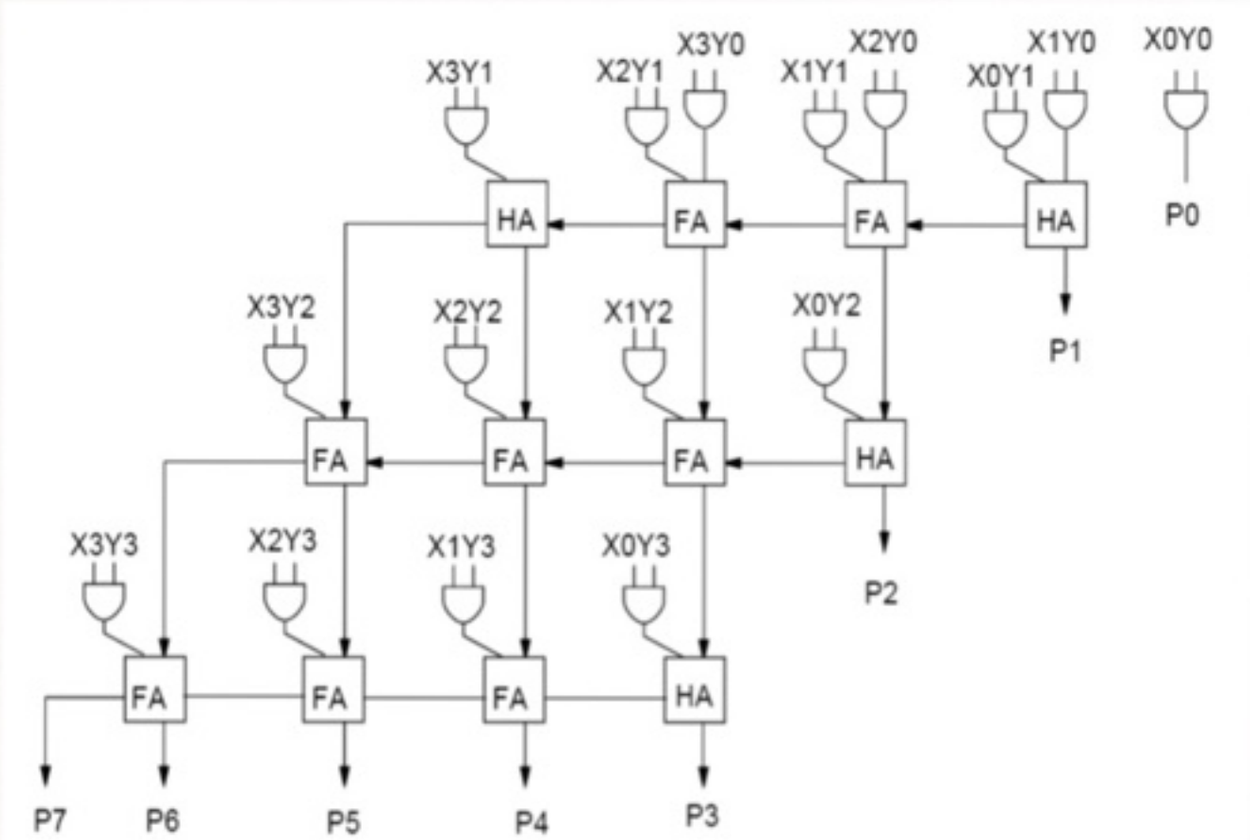
A3Q3 processor run @ 2GHz, delay of logic gates is 0.08ns
setup, hold, and clk-to-q time = 0. what's max number of gates in critical path?

$\frac{1}{2GHz} = 0.5(10^{-9}) = 0.5ns = N(0.08ns)$, $N \approx 6$ gates

A3Q4 what's the critical path of the multiplier?



the delay of a F.A. = 3Δ