ELEC 402 – Project 5
D-FlipFlop Layout

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Area	$\mathbf{t_{setup}}$	$\mathbf{t_{clk-Q}}$	$\mathbf{t_{hold}}$
$1.9 \times 3.06 = 5.814$	60.59ps	181.592ps	-34.43ps

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1 Design Process

The priority in my design was creating the smallest possible layout. I achieved this by only using two diffusion breaks, one in the NWELL and one in the PIMP. I also prioritized avoid any use of M2.

To do this I had to avoid increasing the size of the NMOS and PMOS transistors in order to make room for routing M1 and poly. Thus I sacrificed increasing my delays, however I thought reducing the layout size and not using M2 was a more interesting challenge than sizing for smaller timings.

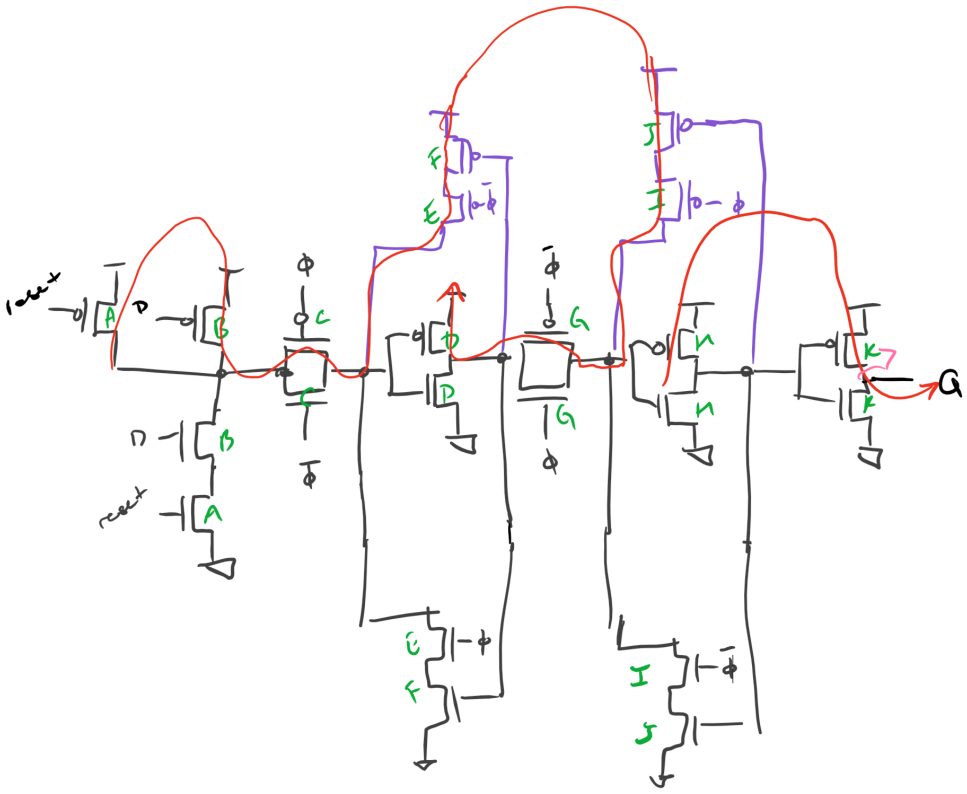

Figure 1: Flip-flop Schematic and Path with Fewest Diffusion Breaks

To achieve the minimum amount of diffusion breaks, I followed the trails seen in Figure 1. Because of the inverted clock signals on the transmission gates, this meant that the polys in the corresponding stick diagram did not align. I routed them together which added extra capacitance. However, this path gave me the smallest width.

To find my DFF setup/hold times. I used the `vbit` device from the `analogLib` library as my input. I created an input sequence that would trigger the FF to latch in a high value then latch in a low value.

I set this pattern to begin executing at a variable time using the `Delay time` property of the device. Then I modified the delay attribute to find the point at which one of the transitions failed.

For example, Figure 2 and 3 show the point at which the hold time was determined. In Figure 2, the delay is set to 215.57ps and the flip-flop can latch in both the rising value of `D` and the falling value of `D`.

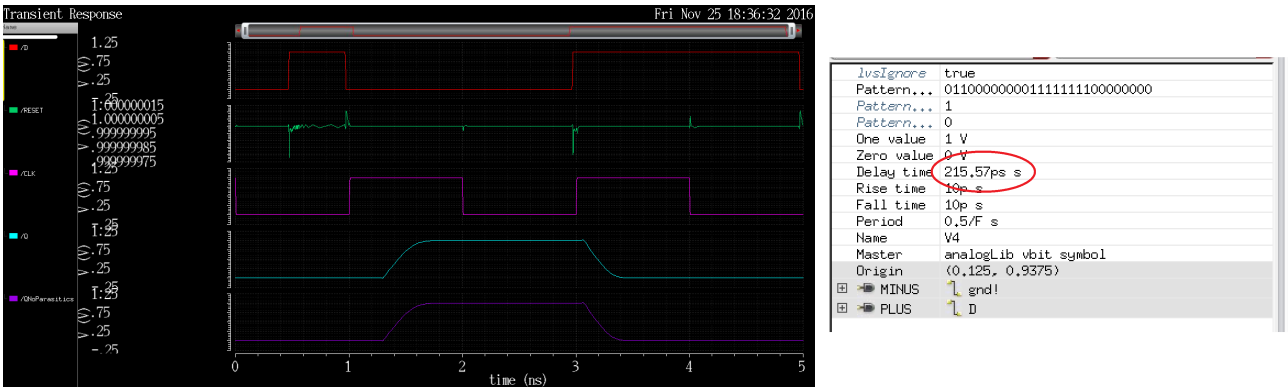

Figure 2: Flip-Flop Successfully Latches in Both High and Low Values

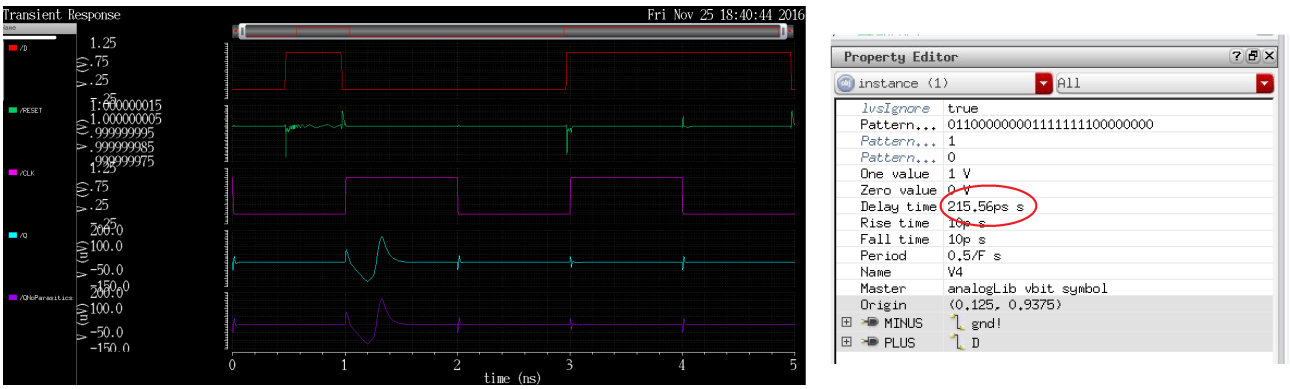

Figure 3: Flip-Flop Fails to Latches in High Value when Hold Time is Violated

In Figure 3, the delay is set to 215.56ps, so the input changes 0.01ps earlier than in Figure 2. However, the flip-flop fails to latch in the rising value of `D`. Thus the minimum hold-time is the difference between the falling edge of `D` and the rising edge of the clock in Figure 2.

Note: In my design, the `RESET` is active-low logic.

I created two copies of the flip-flop that are identical except that only one has had the parasitics extracted to it. Then I hooked them up to the same inputs and load in the same testbench. This way I could directly compare the output of both models.

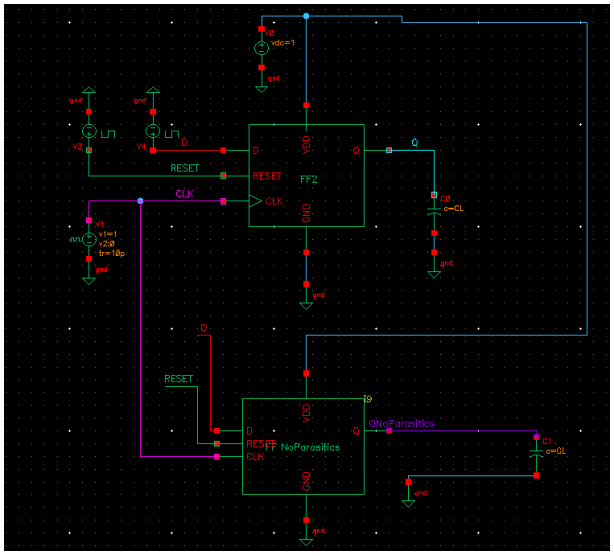

Figure 4: Testbench Schematic for FF with Parasitics (Top) and FF without (Bottom)

2 DFF Layout

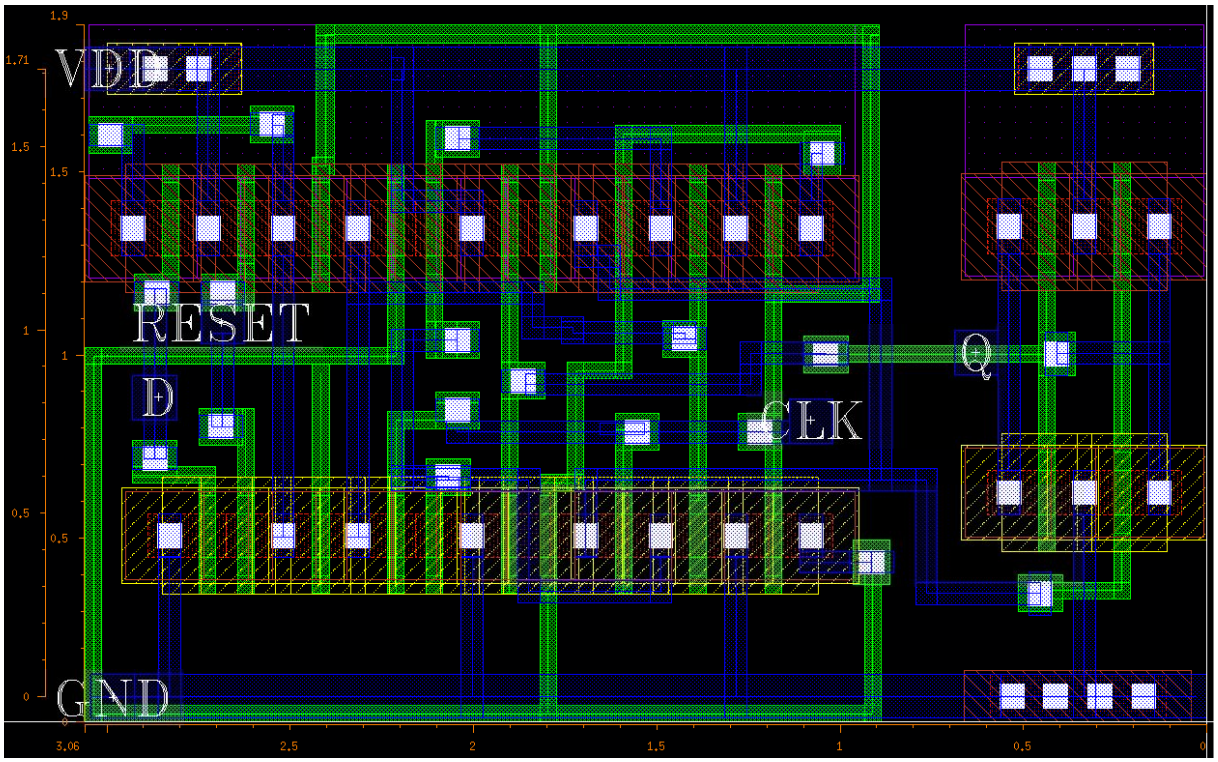

Figure 5: DFF Cadence Layout and Dimensions

3 Waveforms and Parasitics

3.1 Setup Time

Setup time is the minimum amount of time before the rising edge that the input must be stable for the flip-flop to latch it in correctly. My minimum setup time was **60.59ps**.

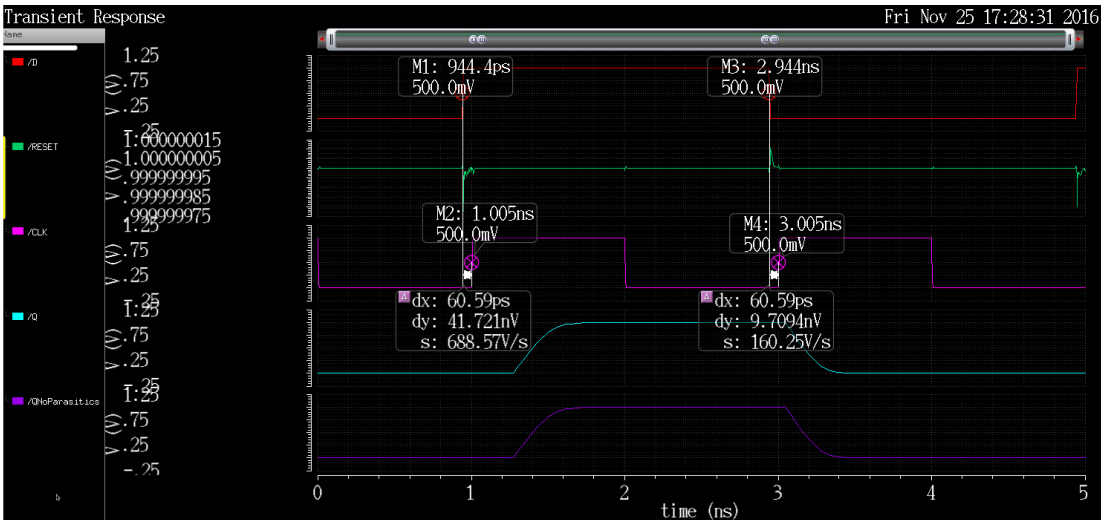

Figure 6: t_{setup} without Parasitics (Lowest) and with Parasitics (2nd Lowest)

3.2 Hold Time

Hold time is the minimum amount of time after the rising edge that the input must be stable for the data to stay latched into the flip-flop correctly. My setup time was **negative 34.43ps**.

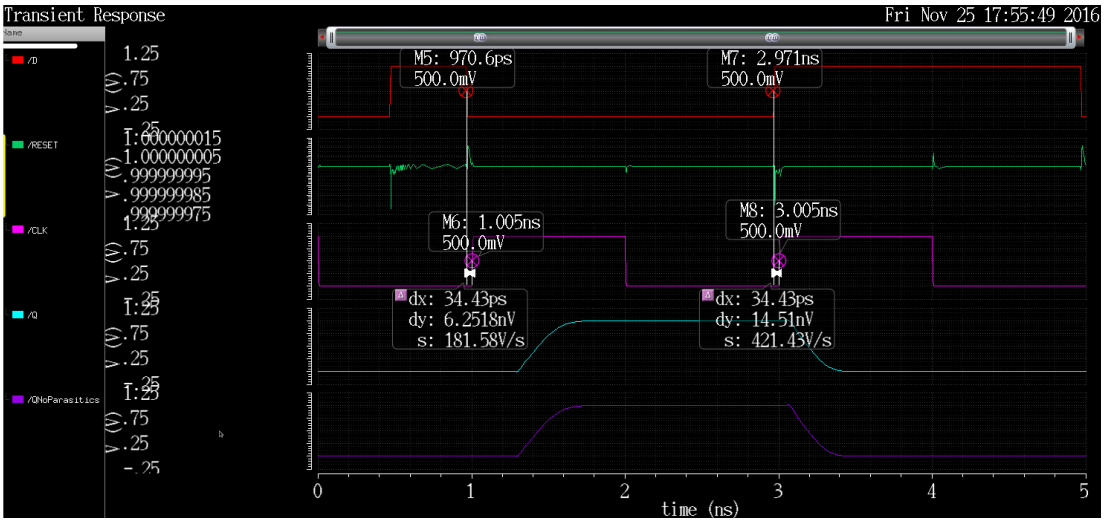

Figure 7: t_{hold} without Parasitics (Lowest) and with Parasitics (2nd Lowest)

3.3 Clock-to-Q Time

The clock-to-Q time is the delay between the 50% point of the clock edge and the 50% point of the the corresponding switching output.

There are four clock-to-Q times in order as shown in the waveform 1) `Q` falls due to low `D`, 2) `Q` rises due to high `D`, 3) `Q` falls due to low (enabled) `RESET`, 4) `Q` rises due to high (disabled) `RESET`. The worst case t_{clk-q} for my flip-flop is **181.592ps**.

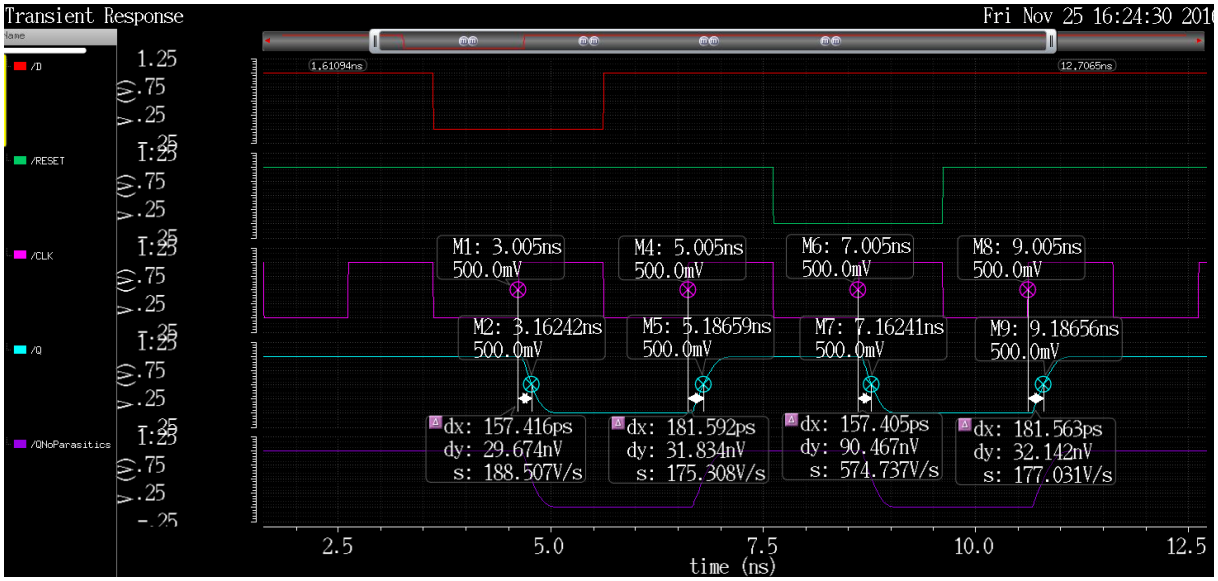

Figure 8: t_{clk-Q} with Parasitics

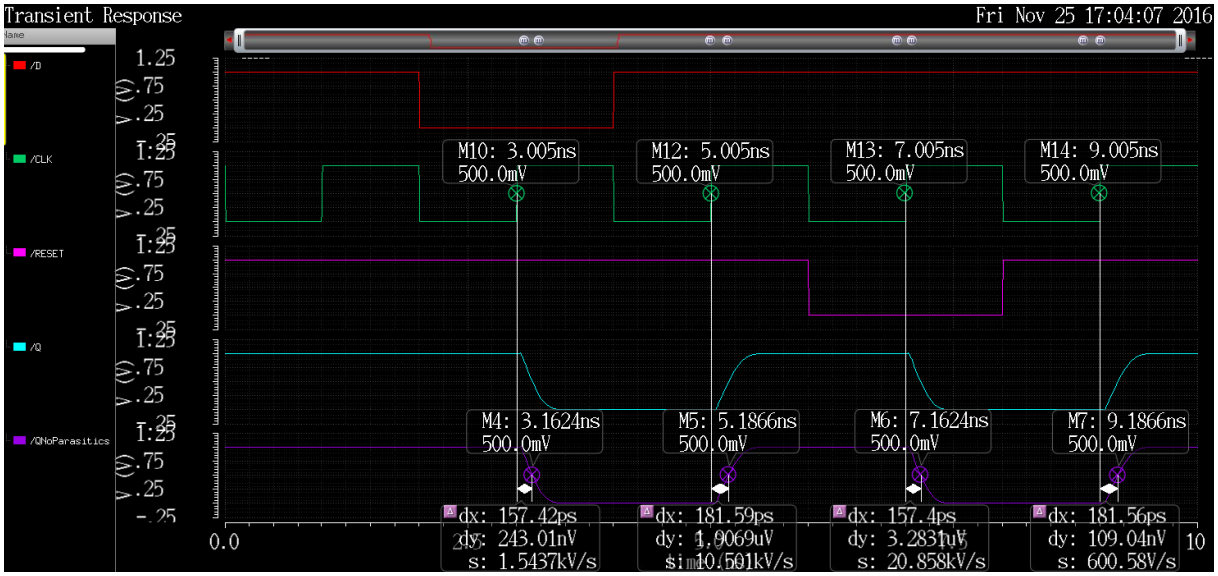

Figure 9: t_{clk-Q} without Parasitics

3.4 Extracted View

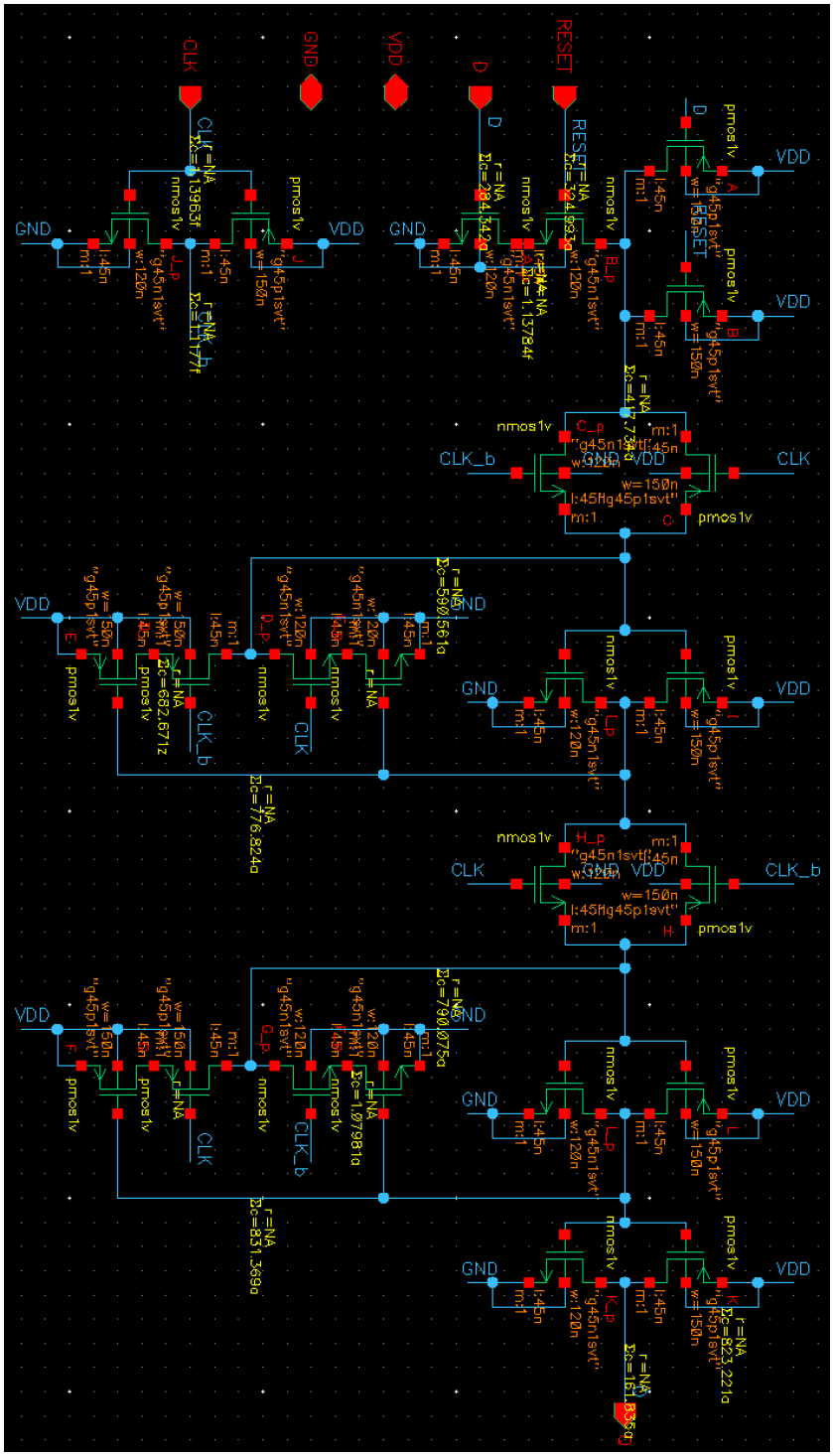

Figure 10: Flip-Flop Schematic with Extracted Parasitics (Rotated)

4 Cell Alignment

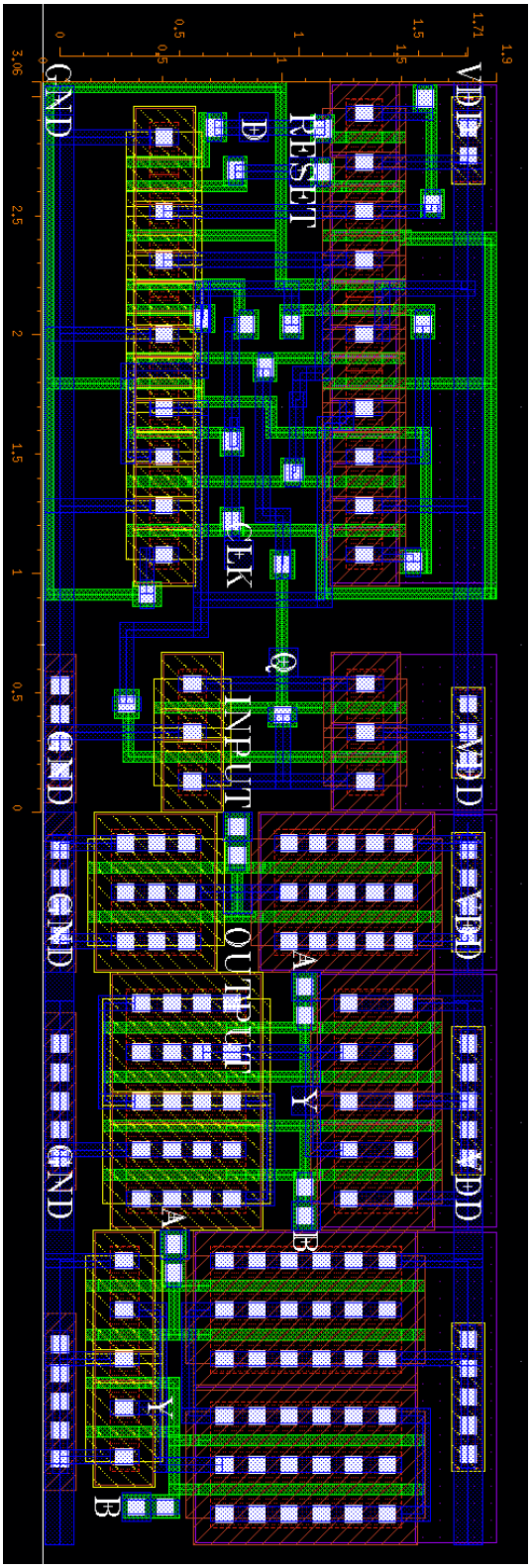

Figure 11: Cells Aligned Side-by-Side (Rotated)