ELEC 402 – Project 3
Inverter Simulation & Layout

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Area	Delay	Area × Delay
1.1891	30.79115	36.61375647

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1 Inverter Layout

Note that I chose to do a folded layout style. This was to reduce the diffusion area, thus reduce the diffusion capacitance and parasitic delay.

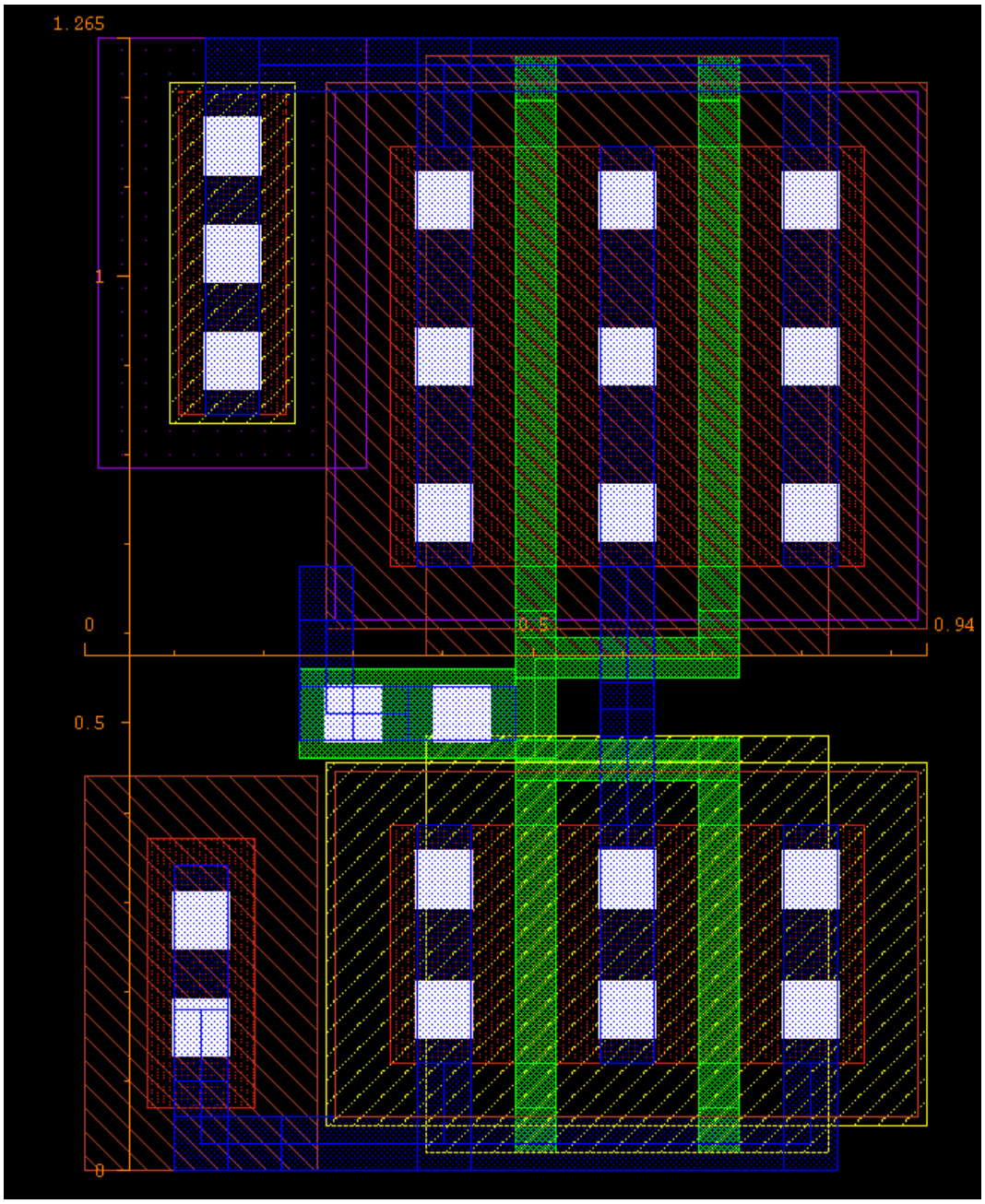

Figure 1: Inverter Layout with Dimensions

$$Area = W \times L = 0.94 \times 1.265 = 1.1891 \tag{1}$$

2 Transient Simulation Waveforms

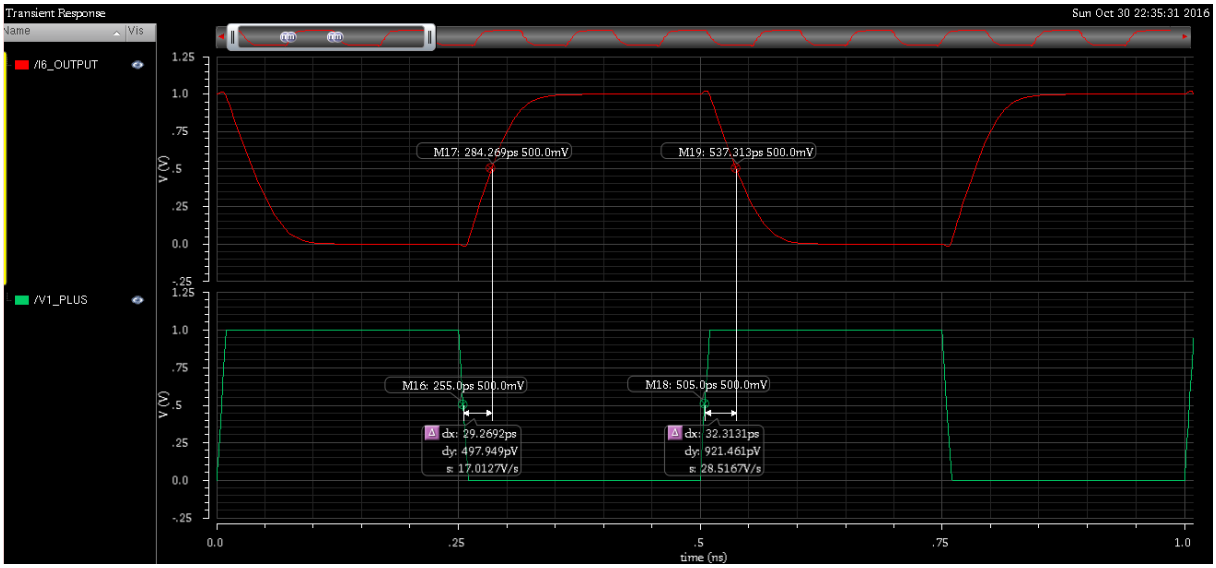

Figure 2: Rise and fall times of the layout inverter

$$Delay = \frac{t_{pHL} + t_{pLH}}{2} = \frac{32.3131 + 29.2692}{2} = 30.79115ps \tag{2}$$

$$Difference = |t_{pHL} - t_{pLH}| = |32.3131 - 29.2692| = 3.0439ps \tag{3}$$

3 Cadence Testbench Schematic

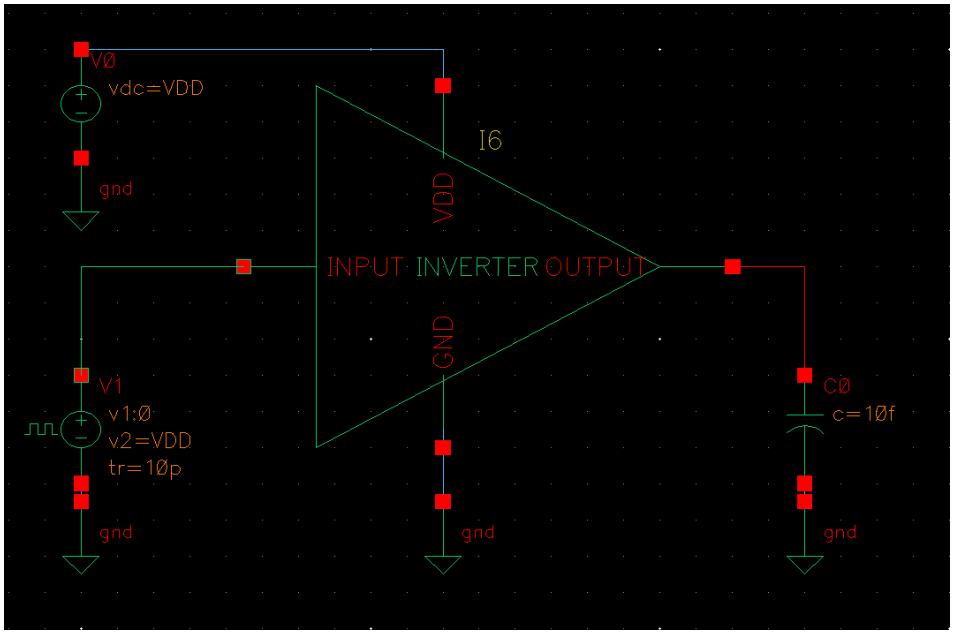

Figure 3: Testbench for Inverter

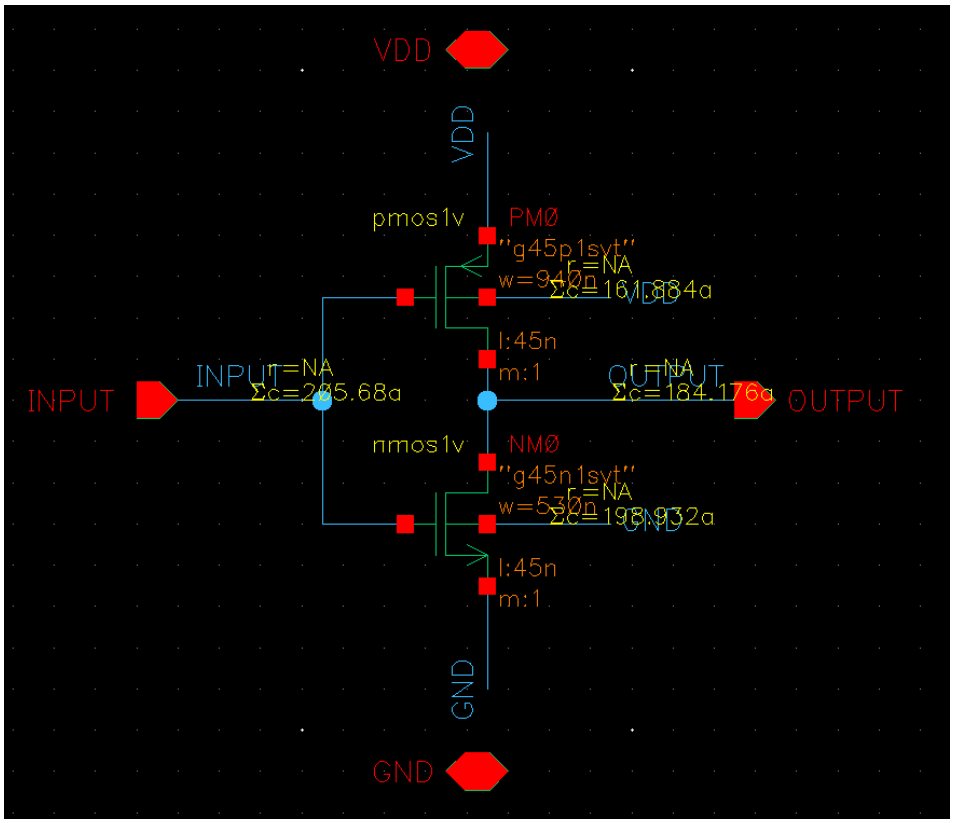

Figure 4: Schematic and Parasitics of Inverter