



FAC

valid	modified	tag	data
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Store Buffer → queue stores for later
→ allow loads to bypass

tag	index	block offset
		block address

$$CPU_{time} = \#inst \left(CPI + \frac{MemAccess}{inst} MissRate MissPenalty \right) \frac{1}{f}$$

$$CPU_{time} = \#inst \left(\frac{AluOps}{inst} CPI_{Alu} + \frac{MemAccess}{inst} AMAT \right) \frac{1}{f}$$

$$AMAT = HitTime + MissRate MissPenalty$$

Scoreboard							
				I	RO	EC	WR
1	LD	F6	34	R2	1	2	3
1	LD	F2	4S	R3	5	6	7
2-10	MUL	F0	F2	F4	6	9	19
2	SUB	F8	F6	F2	7	9	11
40	DIVD	F10	F0	F6	8	21	61
2	ADD	F6	F8	F2	13	14	16
							22 FU

Pipeline → RAW, stalling/forwarding
OO EX → WAW, scoreboard stalls if Rd write pending
OO RO → WAR, stall WB if Rd read pending
Tomasulo → no WAR/WAW, register renaming

I → must be in order
stall if FU not available until WB
stall if dest reg set (WAW)

RO → can do mult same cycle
stall until src reg WB (RAW)

EX → OO
clear bit using src reg

WB → OO
stall if other waiting to read dest until RO (WAR)

Tomasulo

I → stall until free RS

EX → stall until operands after WB
stall until FU free after WB

WB →

COM → stall to commit in order