# Introduction to Worst Case Loading and Timing Analysis

# *Worst Case Loading and Timing Analysis*



**Introduction**

- Timing is probably more important to the success of a microcomputer design than it is to Comedy !!!

- While it is possible to build and debug a single computer system, e.g. a 1-off or prototype, it is significantly more difficult to be able to guarantee that a batch of such systems will all work especially when you factor in the entire range of possible conditions that the components and system may be exposed to.

- For example, the following factors can all make the exact run-time operation of each and every mass-produced chip and circuit board unique.

  - Temperature.
  - Electrical supply voltage.
  - Capacitive loading.
  - Variations in component Min-Max timing due to production tolerances
  - Layout of chip/PCB (e.g. revisions).

# *Worst Case Loading and Timing Analysis*



- There are many designs in production right now that probably have a significant number of unidentified potential failures due to a lack of a worst case loading and timing analysis during design.

- Such failures, may be picked up during simulation and/or testing of initial prototypes or, as a last resort, in post-production testing as they come off the assembly line (assuming you are *rigorous enough)* but depends on volume and intended application – e.g. safety critical systems, as to whether all get rigorously tested.

- Worst case, the failures may not show up in significant numbers until the product is out in the field where it may need to be recalled and replaced leading to major expense and loss of "good will" with customers.

# *Worst Case Loading and Timing Analysis*



**Reasons for Timing Variation: Min-Max Component Tolerances**

- The most common cause of failure is variations in operational Timing
  - Maybe 2% of all systems fail simply because they were built from a random batch of chips whose timing characteristics were at the extreme edges of manufacturers "min-max" tolerances.

  When a system is put together using these "unlucky" components, the timing of critical signals as they pass through gates in the circuit and around the PCB may be altered just enough to result in races, hazards and glitches. Worst case it may result in the clock to a flip-flop arriving before its data, resulting in failed operation. Most designers only build a few prototypes so they mostly miss this.

  These types of failures are hard to pick up just by observing the "actual timings" of a few random prototypes, or even during production when perhaps just 5% of boards are *thoroughly* tested.

  Good simulators can help in the design phase of say a chip (e.g. an FPGA or ASIC), but it is more difficult to simulate a complete system where accurate simulation models of each manufacturer's chips may not exist, or more significantly, where the effects of PCB, component and track layout can be hard to simulate.

- Good engineers therefore need a handle on factors that can influence the timing in their design, particularly for aspects that are hard to simulate.

# *Worst Case Loading and Timing Analysis*



## Other effects that lead to timing variation

- **Revised PCB Layout**: Designs have been known to fail, simply because the manufacturer revised the layout of a PCB, resulting in a critical/marginal signal being routed differently in the new design which subtly altered it's timings. The layout of *very high speed* circuits onto PCBs is a real skill and best left to someone with experience.

- **RevisedChip Layout:** Similarly FPGA designs with tight timing tolerances in Quartus can fail when a different "fitter" algorithm is used to lay out the interconnect within the chip, or when new circuitry is added that causes the fitter to change layout. The system is only as good as the simulation, which in Quartus means it ends at the pins of the FPGA. After that all bets are off as it travels down tracks on PCBs etc.

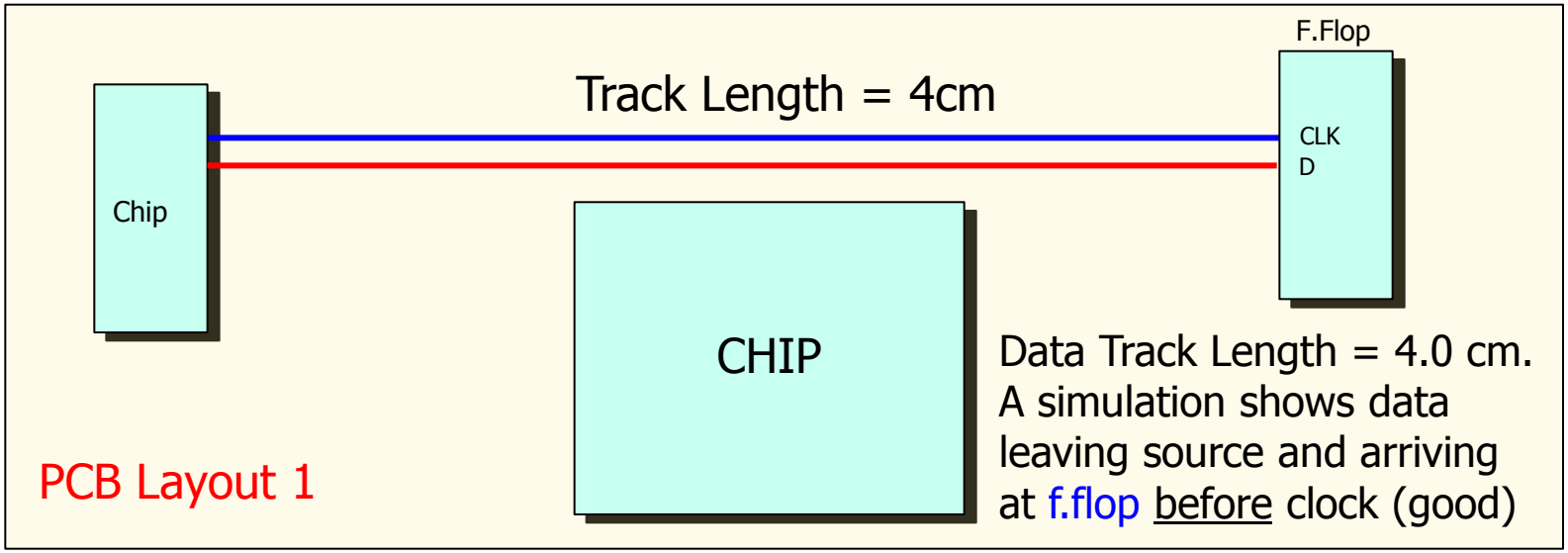
- Admittedly, the likelihood of such problems occurring at low clock speeds (e.g. <10MHz) is relatively small, but beyond 1GHz, a variation in the length of a PCB track, or an interconnect in an ASIC by even just a few mm can be critical.

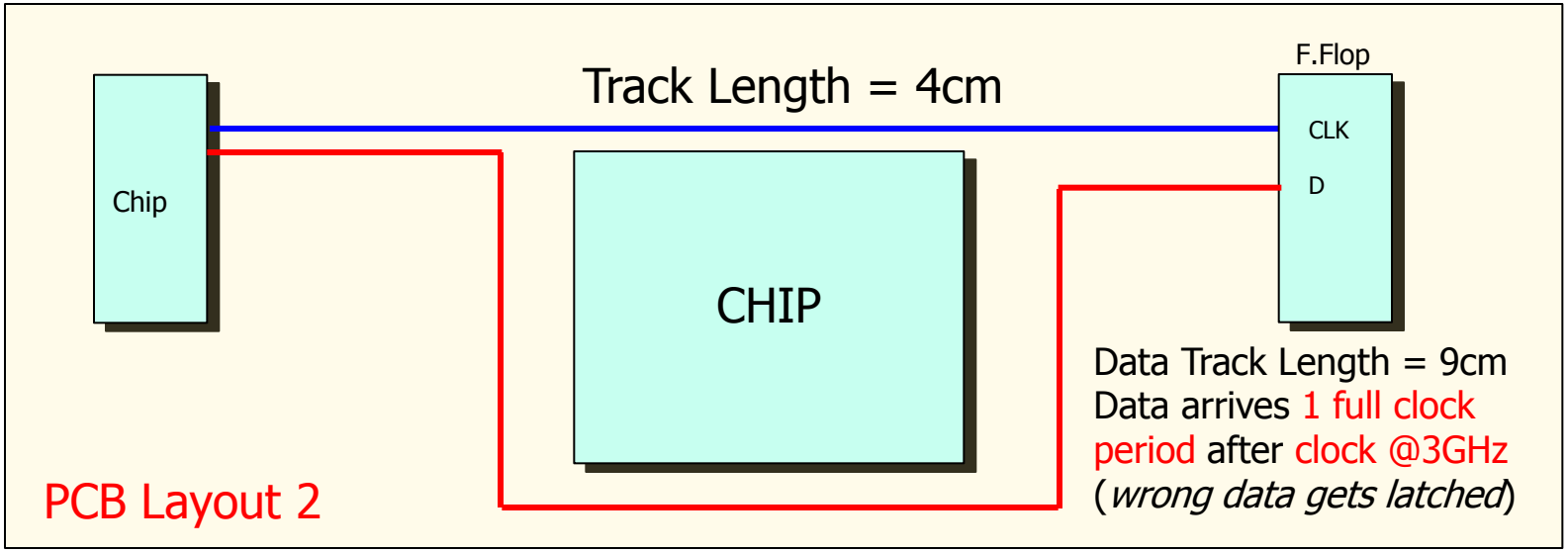
- For example a 3Ghz has a wavelength = ~5cm on a PCB track (at ~ ½ speed of light). An oscilloscope placed in the middle of that track would show a signal "phase shifted" by 180 degrees. A signal at the end of the track is 1 complete clock cycle behind the same signal at the start of the track.

- If a PCB track carrying that 3Ghz clock is shortened by say 1cm then the active edge of the clock could easily be shifted such that it occurs before the data arrives !!

# *Worst Case Loading and Timing Analysis*





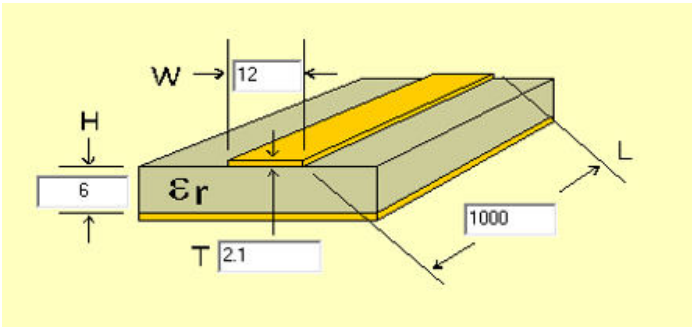



# Worst Case Loading and Timing Analysis

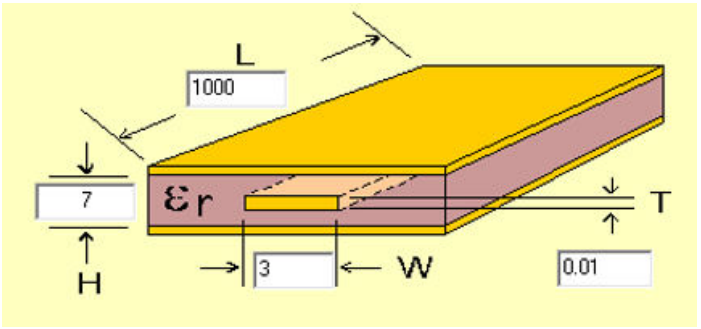


**Reasons for Timing Variation: PCB construction material**

- The speed at which a signal propagates along a PCB track is a function of the track geometry and the material from which is it constructed, i.e. its characteristic impedance $Z_0$. Two commonly used but different PCB construction techniques (microstrip and stripline) are shown below.




Microstrip



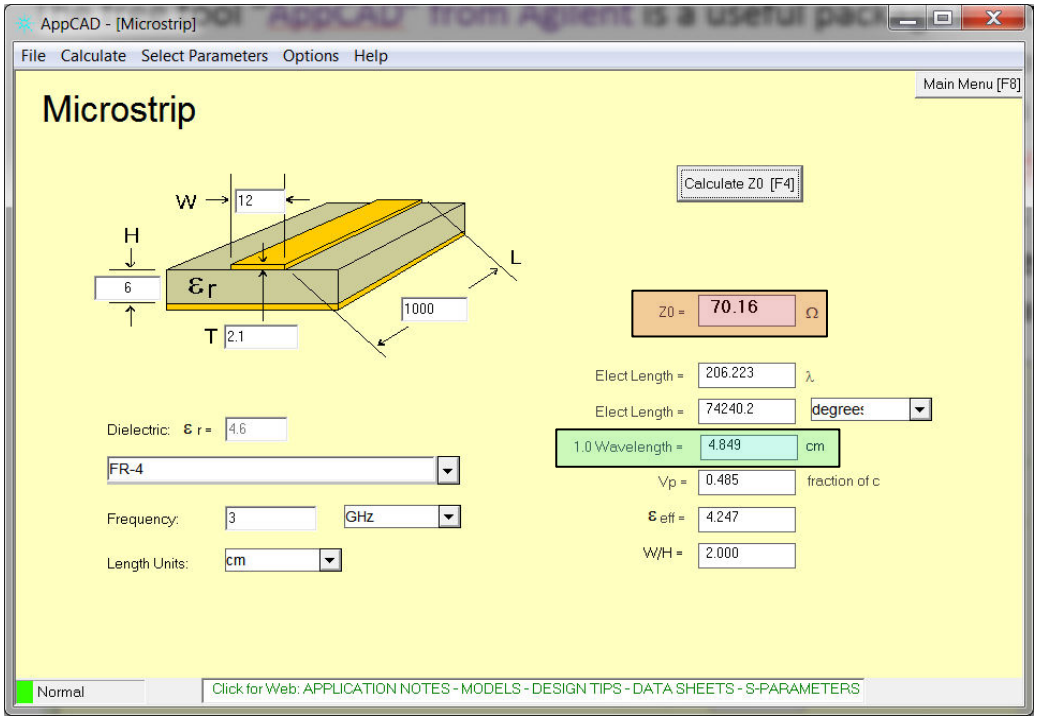

Stripline

| SYMBOL | DESCRIPTION |
|---|---|
| H | Height of the dielectric |
| W | Width of the trace |
| L | Length of the trace |
| Frequency | The frequency on which the calculations are based |
| $Z_0$ | Characteristic impedance of the trace |
| 1.0 Wavelength | Wavelength λ of the trace at the given frequency and the given effective dielectric $\lambda = \frac{3 \times 10_8 \text{ m/s}}{\sqrt{\epsilon_{eff}} \times f}$ |
| $V_P$ | Velocity of the signal on this trace with the given dimensions and frequency relative to the speed of light. The absolute velocity is calculated by $V_{P,.absolute} = V_{P,.relative} \times 3 \times 10^8$ m/s |
| $\varepsilon_{eff}$ | Combination of the several dielectrics which surrounds the microstrip |
| W/H | Ratio between trace width and trace length |

# Worst Case Loading and Timing Analysis



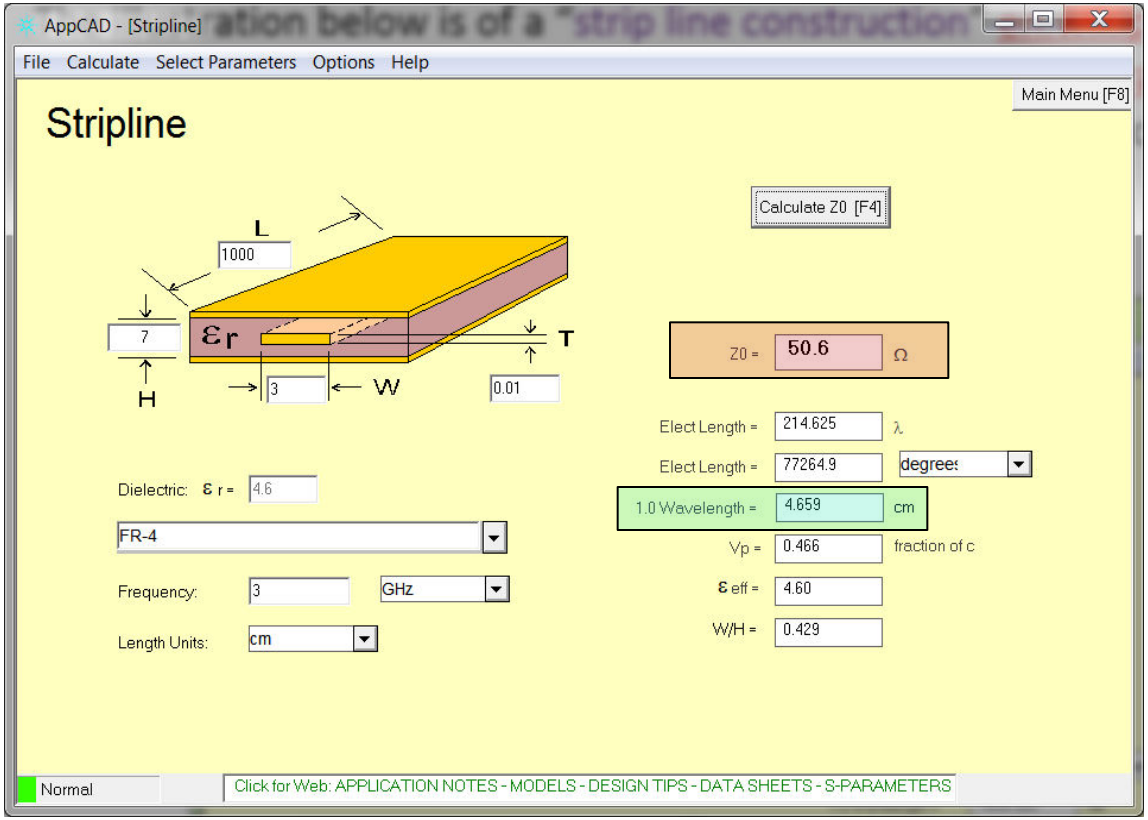
- The free tool "AppCAD" from Agilent is a useful package to download and experiment with, when determining how dielectric, and track construction affect the propagation speed and characteristic impedance $Z_0$ of a copper track on a circuit board.
- The example below shows an FR-4 Microstrip PCB (en.wikipedia.org/wiki/Microstrip) construction. FR4 is a glass-reinforced epoxy laminate sheets (en.wikipedia.org/wiki/FR-4) the most common PCB construction material.
- Signal speed $V_p$ is slightly less than ½ speed of light.
- Knowing the speed we can work out signal delay.



# Worst Case Loading and Timing Analysis



- The illustration below is of a "strip line construction" en.wikipedia.org/wiki/Stripline which uses a flat strip of metal sandwiched between two parallel ground planes. This technique, although more expensive to manufacture, leads to **better/reduced EMI** at higher frequencies compared to mirostrip construction.
- Speed is slightly less than ½ speed of light.



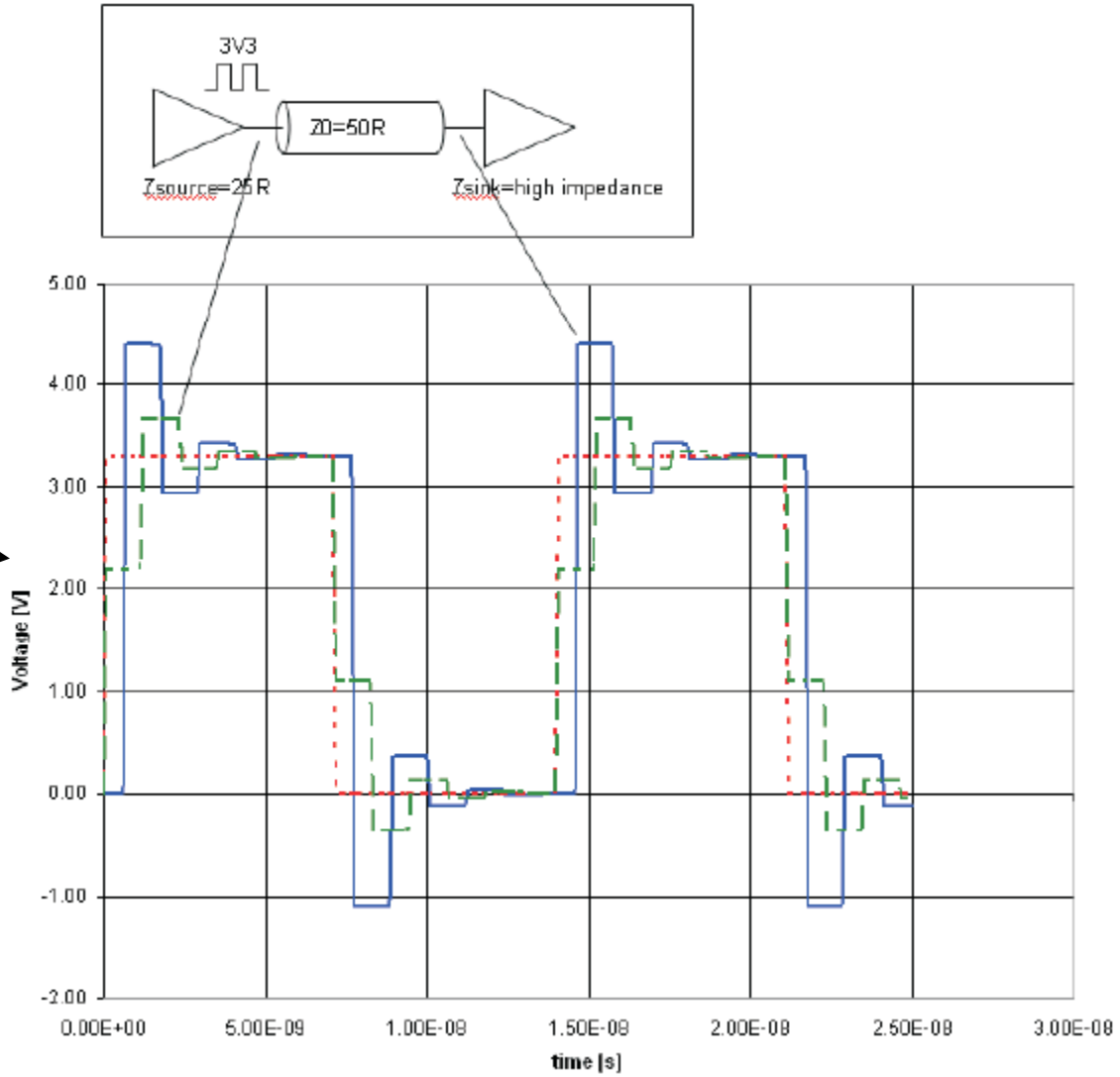
# Worst Case Loading and Timing Analysis



- Impedance mis-matching between chips and PCB tracks can lead to reflections of signals that exhibit fast rise/fall times.

- The effects of these reflections can lead to a partial cancelling of the propagating signal's "voltage wave front", i.e. the leading edge of the signal, resulting in slower rise/fall times (***red*** signal is the source, ***green*** *signal is entering PCB track,* ***blue*** *signal is at receiver*) and hence increased propagation times (*time to register a logic 0 or 1 at other end*)

- We'll return to this subject in a later lecture.

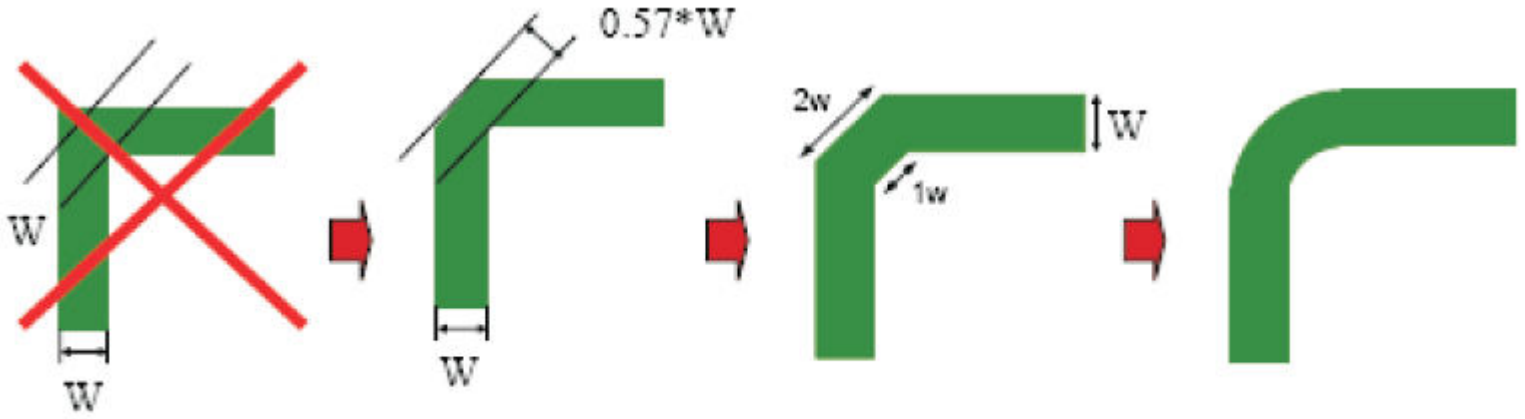


# *Worst Case Loading and Timing Analysis*



**PCB Track layout affects Propagation delay and also EMI**

- Layout of PCB tracks can also affect propagation delays of signal, particularly at sharp/abrupt corners where reflections back towards the source can occur.
- Abrupt corners can also lead to increased EMI at higher frequencies.
- Both undesirable side effects can be reduced by making the corner more "rounded". Something to "bear in mind" when laying out a PCB.

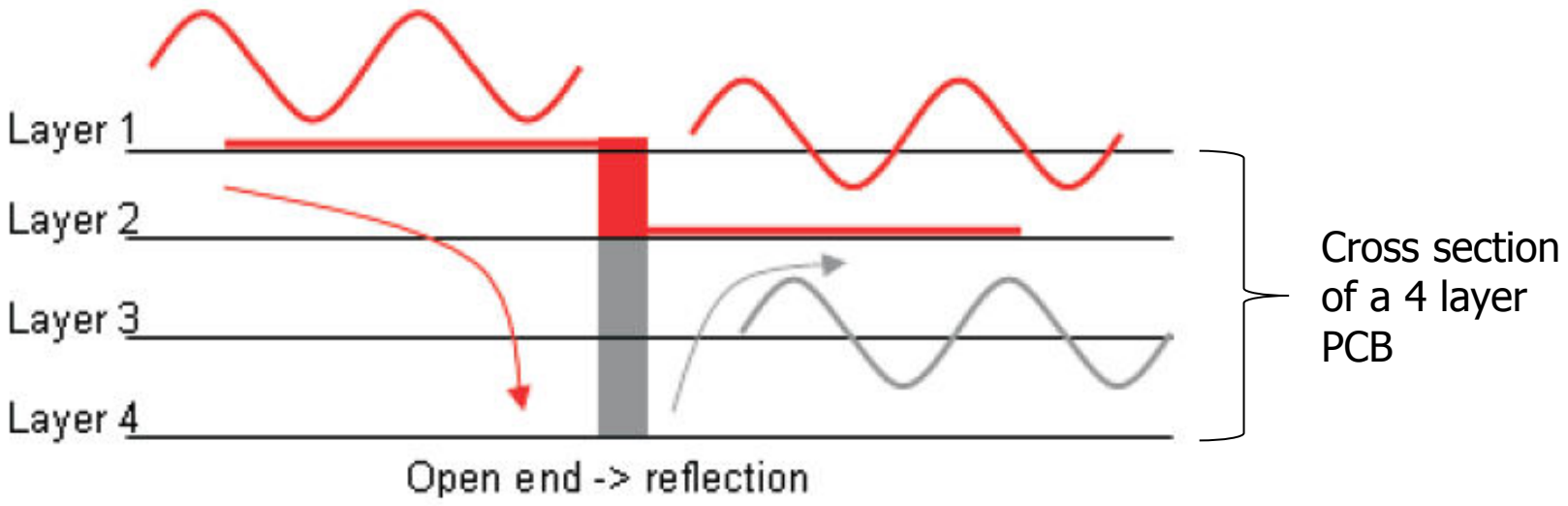



**Poor and Good Right Angle Bends**

# *Worst Case Loading and Timing Analysis*

**Using "vias" on PCB tracks** http://en.wikipedia.org/wiki/Via_%28electronics%29

- The use of vias is essential in most PCBs to connect signals on one layer to signals/tracks on another and they generally pass right through the board.
- A PCB designer has to be careful using them as they add additional inductance and capacitance, giving rise to reflections due to the change in the characteristic impedance at each end of the via.
- Vias also increase the trace length (connections between layers) leading to further delays.



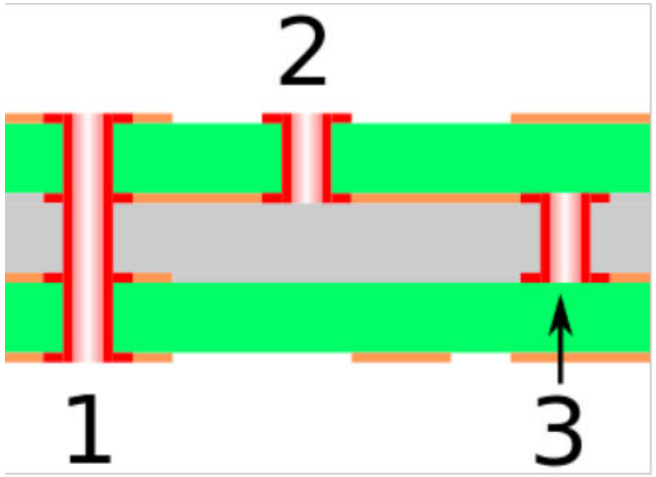

**Reflection Caused by Stubs in a Via**

# Worst Case Loading and Timing Analysis



**Tips for routing tracks and the use of vias:**

- Do **not** use $90^0$ corners on tracks with fast rise times.
- Ensure tracks on different layers of the PCB are routed at 90 degree angles to each other (e.g. east-west on Layer 1, north-south on layer 2 etc.) to avoid signal coupling.
- To minimize crosstalk, the distance between two tracks on the same layer should be approximately 2 to 3 times the width of the track.
- Differential signal tracks should be routed as close as possible to get a high coupling factor – leads to increased noise immunity due to common mode rejection of noise.
- Do **not** use vias on traces with sensitive signals
- Consider stubs created by vias - use blind vias or buried vias.




Different types of vias:
(**1**) Through hole.
(**2**) Blind via.
(**3**) Buried via.
The grey and green layers are non-conducting, while the thin orange layers and vias are conductive.

# *Worst Case Loading and Timing Analysis*



**Other Reasons for Timing Variation: Temperature, Power supply variations and Loading**

- Most manufacturers quote their chips min-max timings only for a specified Temperature, Voltage and Capacitive load value.

- Could you predict how your circuit timings will vary if these factors are altered? If you are lucky the manufacturer will tell you, if not then prepare for some failures if your design does not take these variations into account.

- Do you know for example what the actual voltage is, at the power pins of every chip on your PCB and what factors affect it? You may assume it's 5v or 3.3v etc. but have you actually **measured** it. What can you do to improve it?

- What is the operational temperature of your circuit?

- What is the capacitive loading on critical signals and how do all these things affect timing – more capacitive loading slows the rise and fall times of signals as the capacitance charges and discharges through the output resistance of the transistor driving the load?

# Worst Case Loading and Timing Analysis



**Factors affect Propagation Time:** Temperature

- Devices tend to get slower as temperatures rise, this is a physical effect, due to increased resistance change in Mosfets due to reduction in electron mobility, resulting in lower currents and slower switching times. This goes some way to explaining why computers fail as they get hotter, perhaps after they have been working OK for several mins.

- For some IC families, their propagation delays change by ~2nS over the entire temperature range of -50°C to +100°C which is significant at very high frequencies.

- It also explains why "Over clockers" (who try to raise the clock frequency of their CPU above manufacturers recommended maximum *generating more heat*), often have to resort to liquid cooling to keep the chip functioning at it's fastest speed.

- Tests for propagation delays are generally quoted by the manufacturer at room temperature e.g. 25 degrees C but you should consider the effect for other temperatures.

http://ihome.ust.hk/~eekursun/papers/c25.pdf

| 65nm CMOS Technology | Temp (°C) | Inverter | NAND2 | NAND4 | NOR2 | NOR4 |
|---|---|---|---|---|---|---|
| Average Delay (s) | 25 | 1.54E-11 | 5.62E-11 | 8.65E-11 | 6.86E-11 | 1.35E-10 |
| | 125 | 2.08E-11 | 8.52E-11 | 1.32E-10 | 1.05E-10 | 2.05E-10 |
| Delay Variation (%) | | 35.0 | 51.6 | 52.6 | 52.4 | 52.1 |

# *Worst Case Loading and Timing Analysis*



**Factors affect Propagation Time:** Power supply voltage

- A change in propagation delay might also be expected as $V_{cc}$ (supply voltage) varies between it's minimum and maximum operational values, the exact value varies from chip to chip.

- Reduced supply voltage at the chip (*i.e. below manufacturers recommended operating voltage*) may be as a result of poor power distribution on the PCB. Wider power tracks or better still, separate power/GND planes lead to reduced power line resistance, which in turn leads to less voltage drop at the chip.

- Increased chip voltages lead to increased currents (*generating more heat and stressing the chip*), which allow the transistors to switch state more rapidly since the increased current leads to faster charging/discharging of signal capacitance (loads), i.e. it affects the slew rate of the device.

- Over-clockers often have to raise the motherboard voltage to achieve higher clock frequencies while force-cooling the resulting hotter circuit.

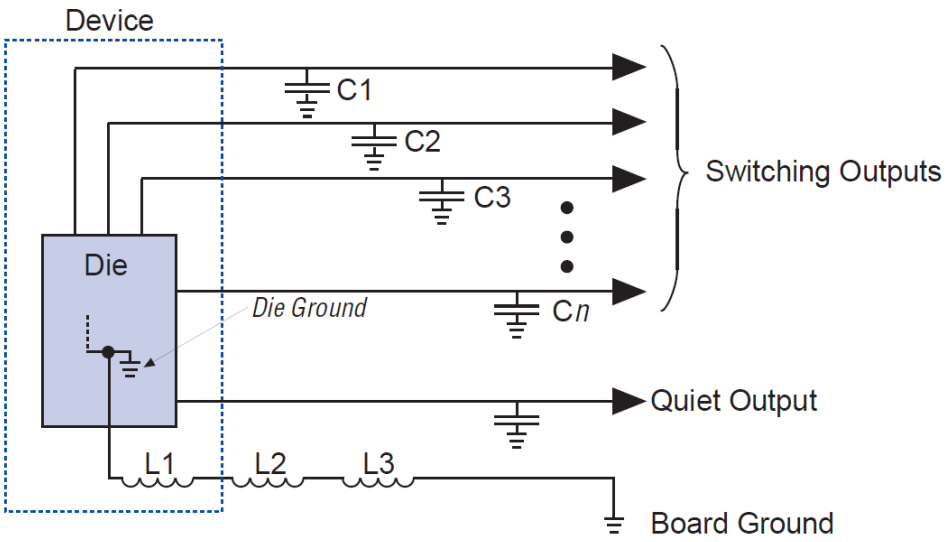
- Values quoted by the manufacturer are those for the device operating at it's recommended supply voltage, if you know it will operate outside that, then ideally you take it into account.

# Worst Case Loading and Timing Analysis



**Factors affect Propagation Time:** Number of outputs switching simultaneously

- The number of output pins that simultaneously switch from high to low within a chip can have an effect on the propagation delay of each *individual* output. e.g. an 8 bit counter rolling over from 11111111 to 00000000 is an example.
- This is due to the inherent inductance associated with the ground lines feeding the chip. The illustration below shows several output signals with inherent capacitance all currently charged to logic '1'. When they switch together a large momentary current is created as the chip tries to discharge those capacitors and the current flows via the GND pin.
- The inherent inductance of the Ground signal creates a back emf which can lead to a small reduction in the supply voltage inside the chip due to "ground bounce". This results in momentarily smaller operating voltages, reduced slew rates and longer discharge times for the capacitors. 74AHCTxx families add 250ps per output switching.



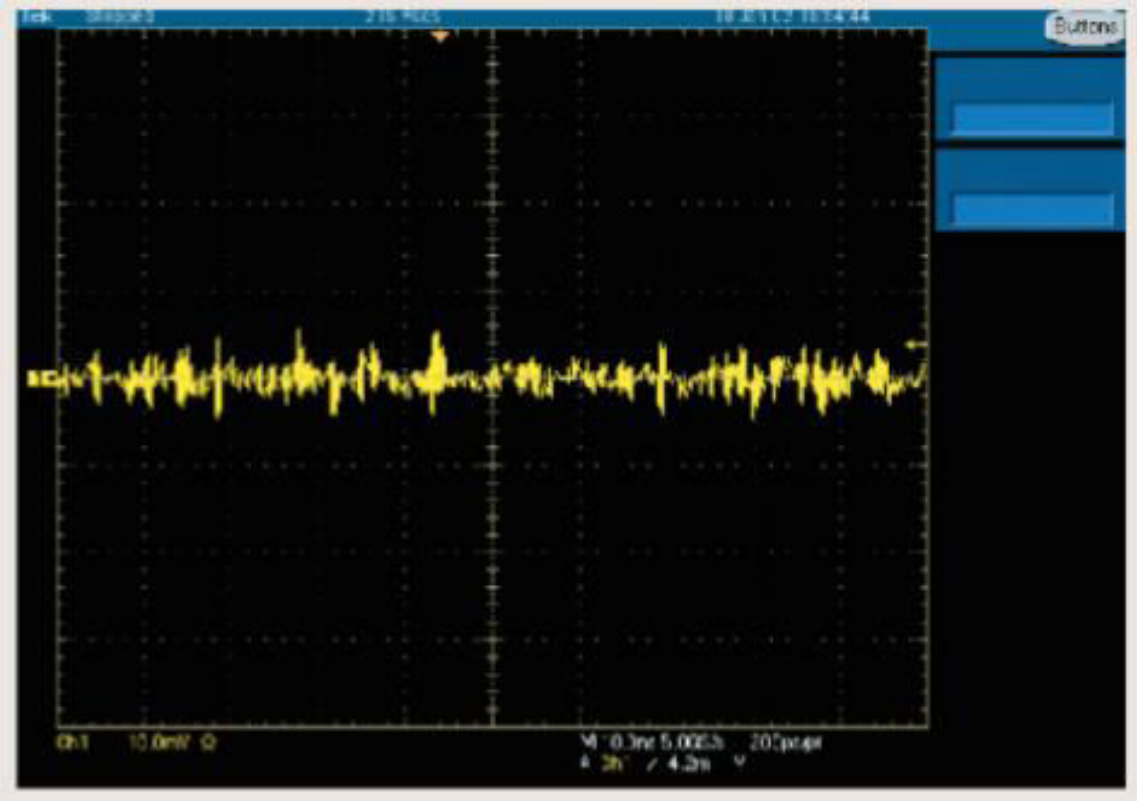

L1 = Inductance of bond wire in the chip from devices 'die' to the package pin
L2 = Inductance of the package pin to the PCB ground signal. This is greatest when the device in placed in a socket
L3 = Inductance of the PCB track back to the power supply ground reference.

Ground bounce can also cause "quiet output" signals (those at logic 0) to momentarily rise which could trigger other logic. Use gray code counters or series resistors to limit number of outputs switching and current.

# *Worst Case Loading and Timing Analysis*



- Ground Bounce captured on an oscilloscope due to excessive chip currents and/or high resistance in PSU or ground plane.



# *Worst Case Loading and Timing Analysis*



**What if you can't measure, simulate or take account of everything? : Soak Testing**

- When it is hard to factor in all the various parameters, manufacturers will sometimes resort to submitting each produced system to a Soak test as a way of weeding out flaky systems **after** assembly – but it's expensive, it's not a substitute for better design.

- Soak or "Burn in" Testing involves testing under stress, e.g. extremes of Temperatures, Capacitive Loading and Supply Voltage etc. This is particularly important in safety critical systems, e.g. Nuclear Power Stations, Railway Signalling, fly by wire aircraft etc. It also helps to identify systems that would fail early in their life.

**Designing for Worst Case**

- A worst case design would attempt to take account of as much of the information that is available, as possible, regarding the component variations in tolerances and timing.

- If this approach is adopted, then even when all component parameters are at their most adverse values, or anywhere in between, a worst-case design in theory should always work.

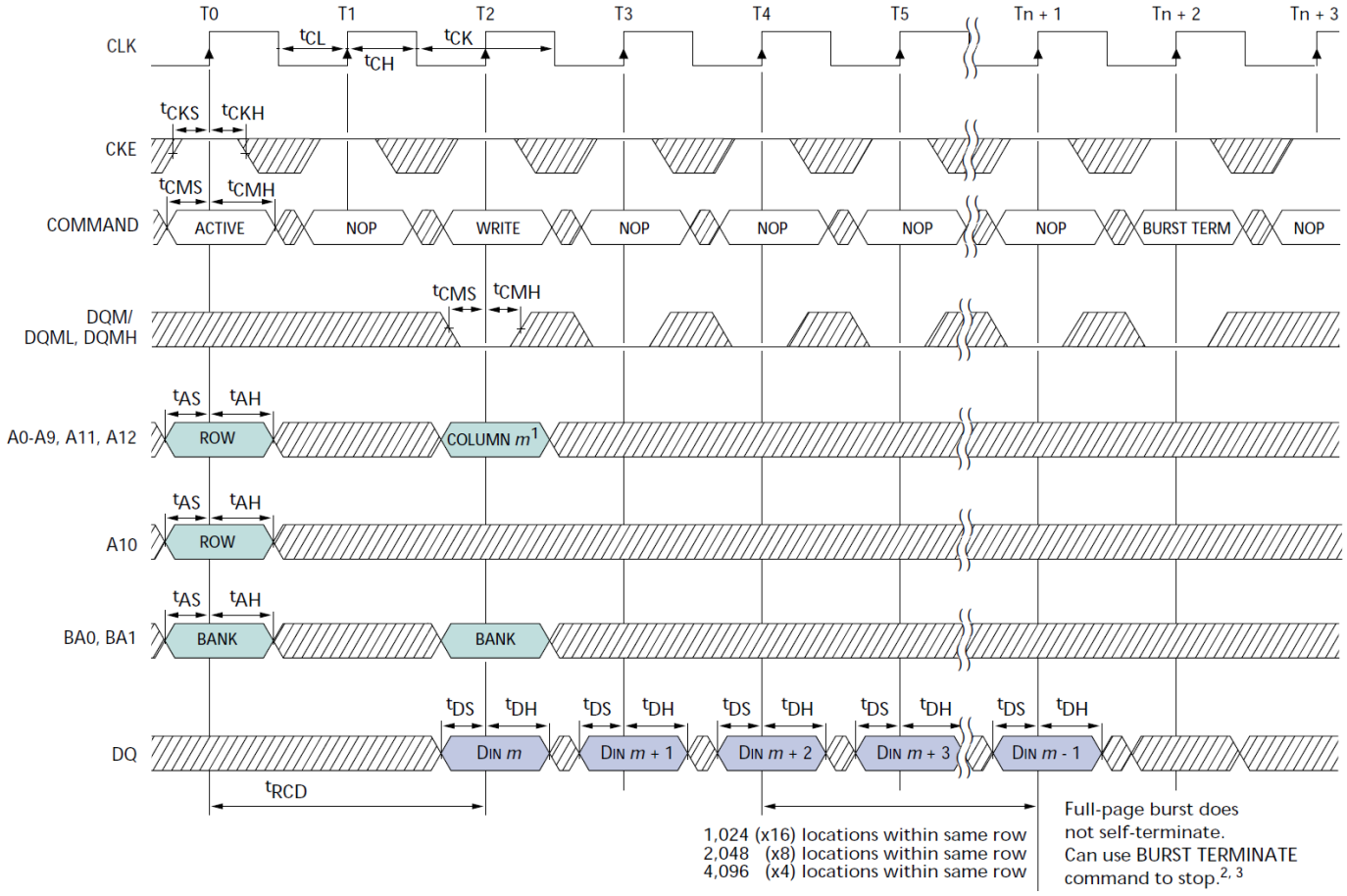
- If such a detailed analysis, is **not** undertaken then there is no way of knowing if the design will work reliably when it is mass produced and subjected to differing environments.

# Worst Case Loading and Timing Analysis



## Timing Diagrams

- To design for worst case, an Engineer must be able to understand and perform detailed timing analysis of manufacturers data sheets. Simulation results can then be compared to data sheets to verify timing (we do this in Assignment 1). Can you interpret this timing diagram, what do the signals and timing parameters mean and which of them are important?




An SDram Memory chip Timing diagram

# *Worst Case Loading and Timing Analysis*

## Timing Concepts

- Every microcomputer system design engineer should also have a handle on at least the following very important timing concepts and what can cause them to vary.

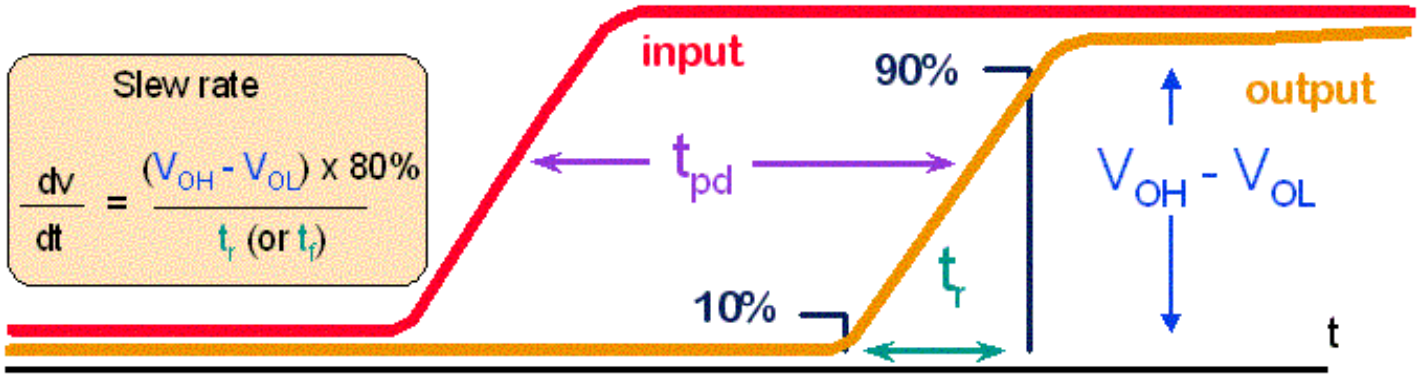
- Knowledge of these is essential to an understanding of how to interface CPUs to say memory systems, motherboards and backplanes.

  - Slew Rate of a signal.
  - Propagation Delay (*Latency*) of a signal.
  - Setup and Hold time (*Meta-stability issues)*

# Worst Case Loading and Timing Analysis



- **Slew rate: Causes and Effects on Timings**
  - The slew rate of an output signal is the rate of change of it's output voltage dV/dt, or more usefully is quoted as the time it takes an IC to switch from say 10% ($V_{OL}$) to 90% ($V_{OH}$) and vice-versa of it's final value i.e. from logic 0 to logic 1.
  - In other words, even if the circuit has made the decision internally as to what the output should be, it still takes time for the output transistor(s) to switch the end of the wire from one logic level to another.



# *Worst Case Loading and Timing Analysis*



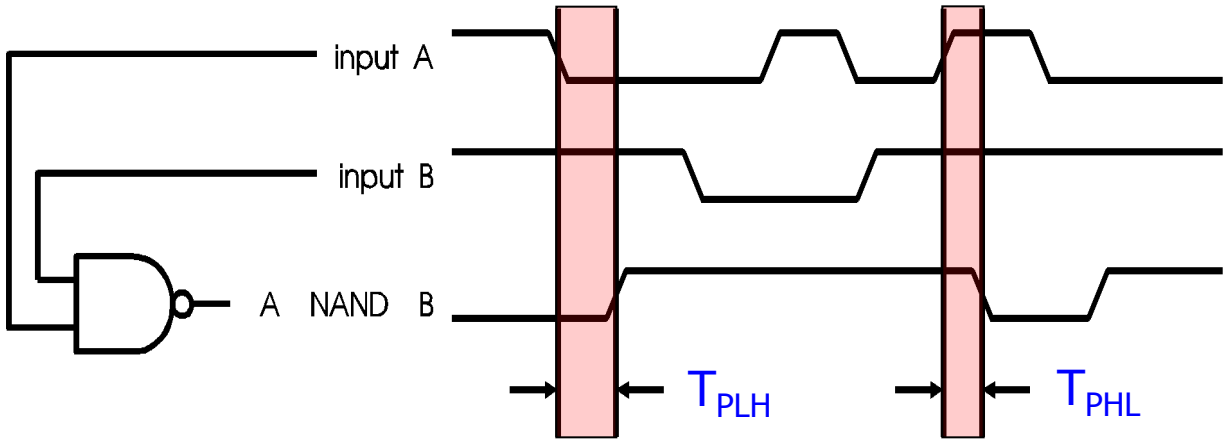
- **Factors affecting Slew Rates**
  - A circuit has to charge and discharge the inherent capacitance of the load (gates and PCB tracks) connected to the output signal via the output resistance of the transistor driving the signal (*as well as fight the back emf due to the inductance of any wires attached to it*). Thus increased capacitive/inductive loads slow the 'rise' and 'fall' time of the signal.
  - Manufacturers may quote the rise and fall times for an output signal but only a specific capacitive load. Differences, particularly in capacitive load can then be taken into account by you.
  - **SIGNAL** rise/fall times proportional to $e^{-(1/RC)}$
  - The move to lower supply voltages (3.3v and more recently 1.8v) means the 10% to 90% values are reduced, consequently output signals switch state faster when designed to operate at lower voltages. (*That's different to lowering the voltage from the one specified by the manufacturer*).

# Worst Case Loading and Timing Analysis



**Propagation Delays (Latency)**

- A propagation delay is a measure of the time taken for a change at the input of a device to effect a change at the output. Even wires, exhibit some delays.
- Not all devices have symmetrical delays for positive and negative transitions.
- In the diagram below, the propagation delays for a high to low transition ($T_{PHL}$) are shorter than for a low to high transition ($T_{PLH}$).
- This asymmetrical delay is common for TTL devices (**note** *CMOS devices tends to have more symmetrical timings*) open collector and open drain outputs because they are better at sinking current than sourcing it. Rise times for an open drain output are notoriously slow due to the pull up resistor being used to charge load capacitance.
- Serious timing issues can arise if a number of devices are cascaded all exhibiting their min (or max) propagation values. Under such circumstances, one signal can race another, perhaps overtaking it and arriving before (or after) it is required.



# Worst Case Loading and Timing Analysis





**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
$I_{CC}$ category: MSI

Note rise and fall times specified for a particular capacitive load

Note variation in times with temperature

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; $t_r = t_f$ = 6 ns; $C_L$ = 50 pF

| SYMBOL | PARAMETER | $T_{amb}$ (°C) 74HC +25 min. | +25 typ. | +25 max. | −40 to +85 min. | −40 to +85 max. | −40 to +125 min. | −40 to +125 max. | UNIT | TEST CONDITIONS $V_{CC}$ (V) | TEST CONDITIONS WAVEFORMS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PHL}/ t_{PLH}$ | propagation delay $A_n$ to $\overline{Y}_n$ | | 41<br>15<br>12 | 150<br>30<br>26 | | 190<br>38<br>33 | | 225<br>45<br>38 | ns | 2.0<br>4.5<br>6.0 | Fig.6 |
| $t_{PHL}/ t_{PLH}$ | propagation delay $E_3$ to $\overline{Y}_n$ | | 47<br>17<br>14 | 150<br>30<br>26 | | 190<br>38<br>33 | | 225<br>45<br>38 | ns | 2.0<br>4.5<br>6.0 | Fig.6 |
| $t_{PHL}/ t_{PLH}$ | propagation delay $\overline{E}_n$ to $\overline{Y}_n$ | | 47<br>17<br>14 | 150<br>30<br>26 | | 190<br>38<br>33 | | 225<br>45<br>38 | ns | 2.0<br>4.5<br>6.0 | Fig.7 |
| $t_{THL}/ t_{TLH}$ | output transition time | | 19<br>7<br>6 | 75<br>15<br>13 | | 95<br>19<br>16 | | 110<br>22<br>19 | ns | 2.0<br>4.5<br>6.0 | Figs 6 and 7 |

Note variation in times with Voltage

# Worst Case Loading and Timing Analysis

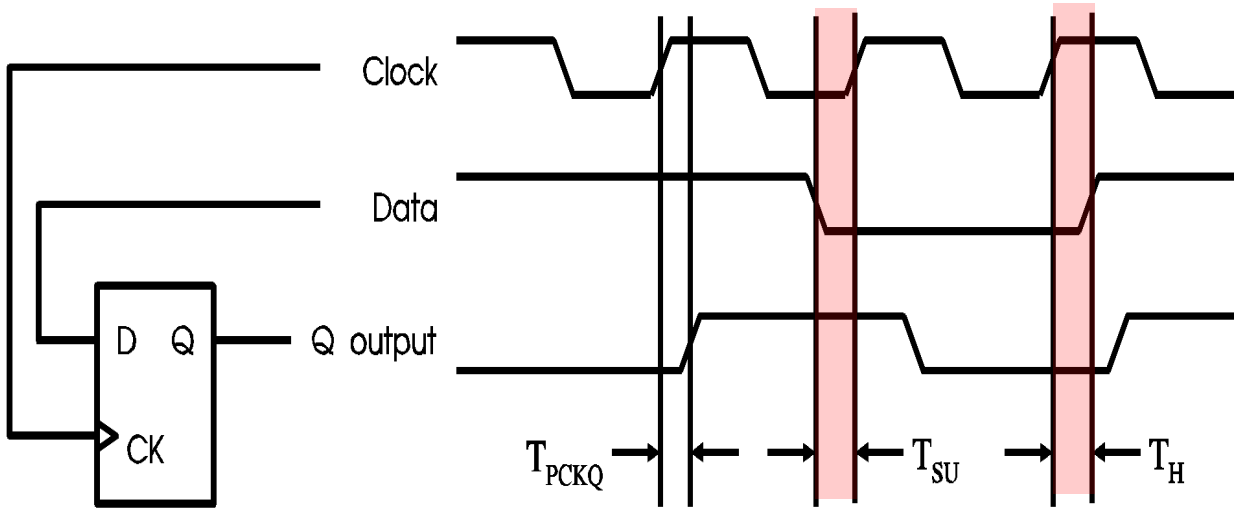


## Synchronous (clocked) Systems

- A huge problem in synchronous systems is ensuring that flip-flop setup and hold times are not violated

  - **Setup time** ($T_{SU}$) is the length of time the Data input to the flip-flop must be valid and stable, prior to being clocked.
  - **Hold time** ($T_H$) is the length of time the Data input to the flip-flop must be held valid and stable, after being clocked.

- If setup or hold times are violated, the Q output may become invalid or even oscillate, a condition referred to as metastability (see on-line Application note on metastability by Altera)

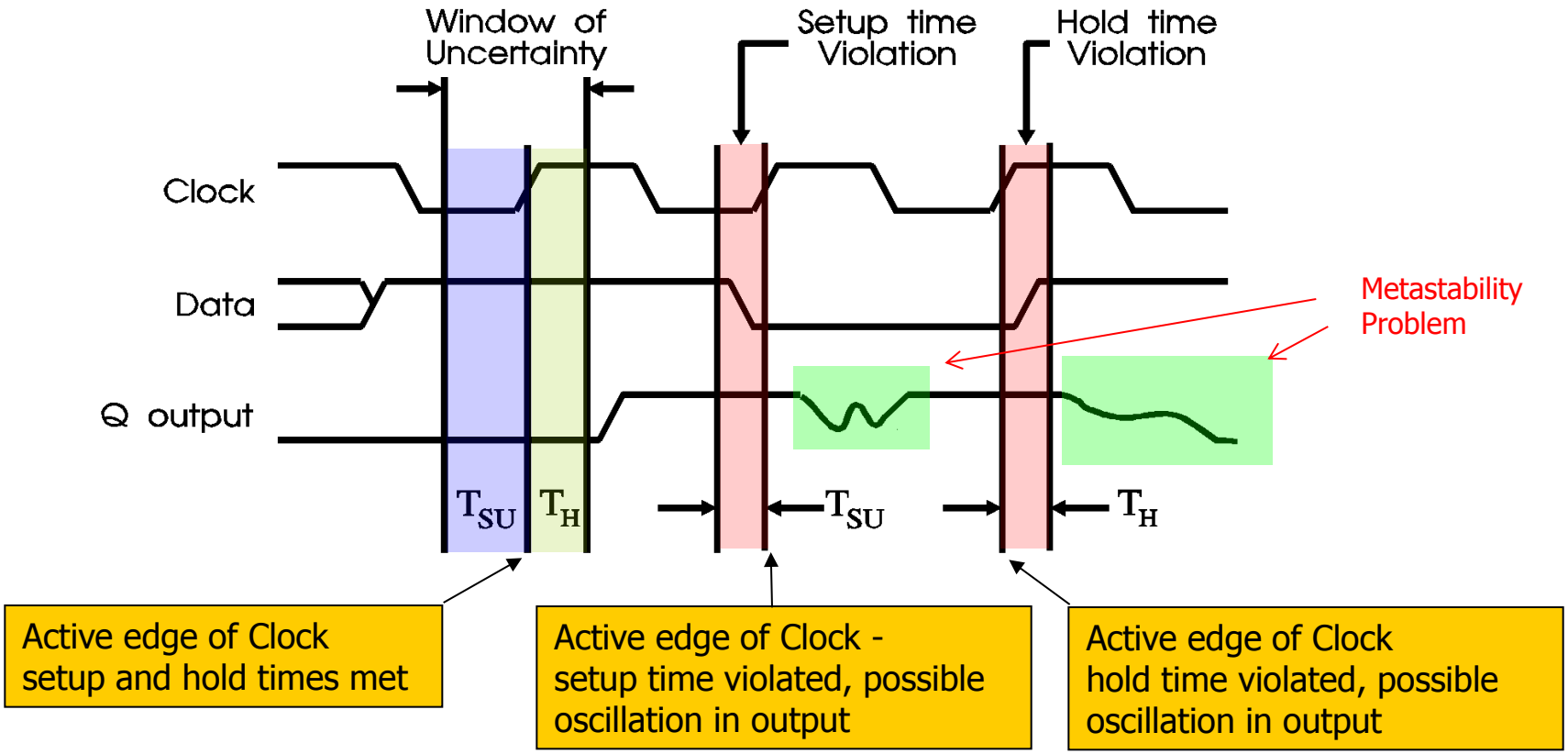


# Worst Case Loading and Timing Analysis



**Metastability**

- The illustration below shows what *can* happen to the output of a Flip-Flop when it's Set-Up and/or Hold-times are violated. This is a particularly important consideration in synchronous (clock driven) systems.
- When either of these times is violated, the output may take an invalid level, or more commonly oscillate for a undefined period of time. (*Read article from Altera on course web-site*)

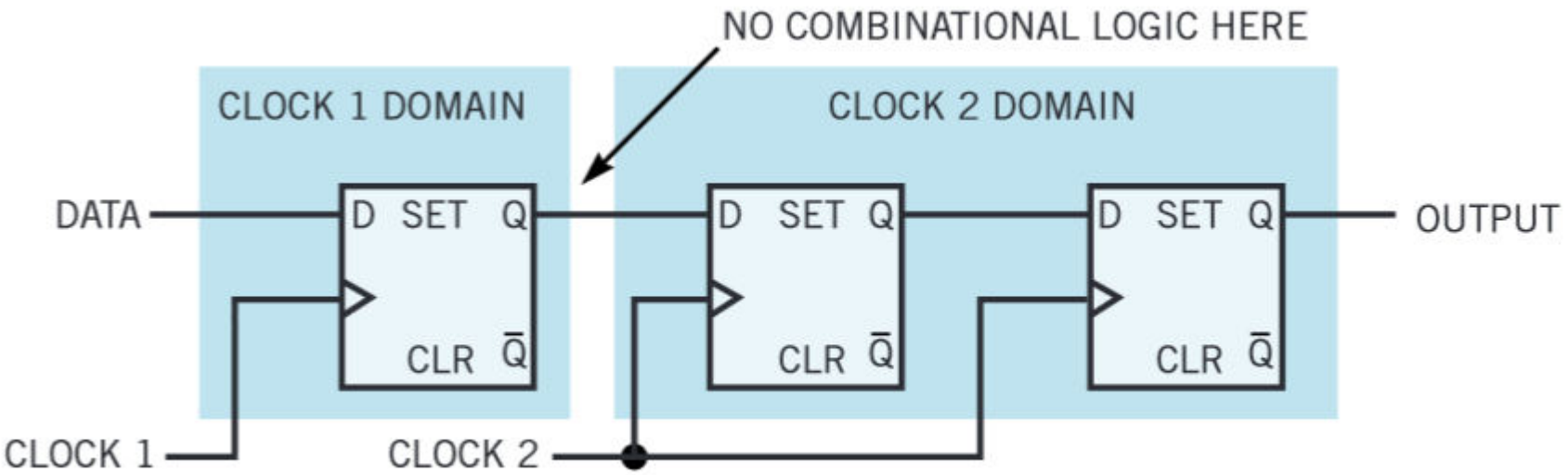


# Worst Case Loading and Timing Analysis



**Tolerating Metastability**

- It has been shown that once a flip flop enters a meta stable state, the probability of being in that state some time later decreases exponentially with time.
- When an asynchronous input arrives at a flip flop, perhaps from the real world, or from another circuit driven by a different clock (i.e. a signal crosses a clock domain) there is a possibility that it will induce metastability. The probability of this problem propagating to another part of the circuit can be reduced by having synchronising logics, such as that shown below.



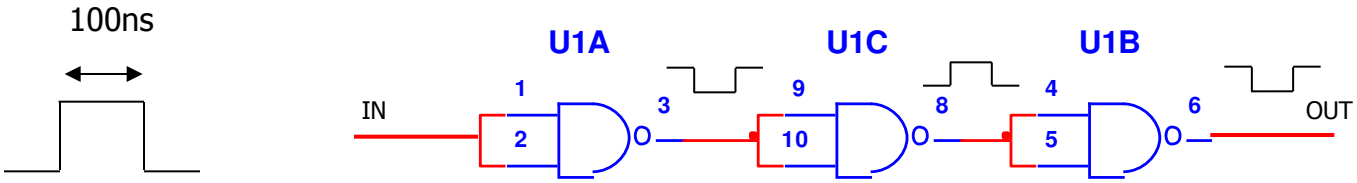

Synchronizer circuit

http://m.eet.com/media/1137372/17561-310388.pdf

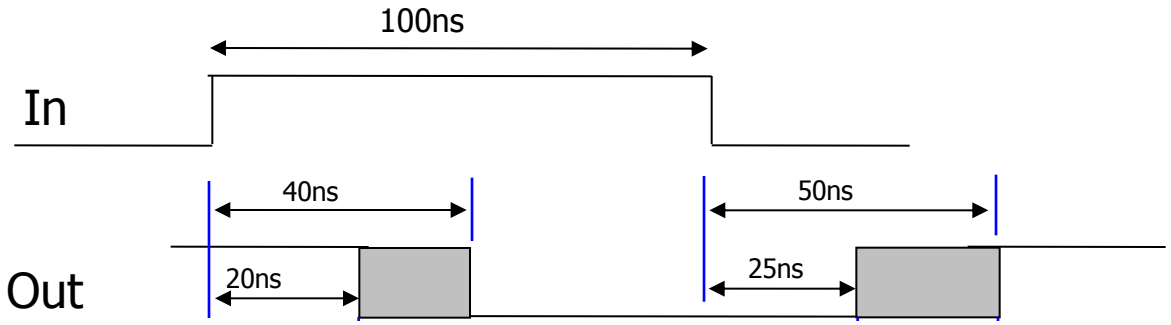
# Worst Case Loading and Timing Analysis



- Draw the min/max timing diagram for the output of the following circuit assuming nominal temperature and voltage supply and no adverse capacitive loading on any output.




**Solution**:

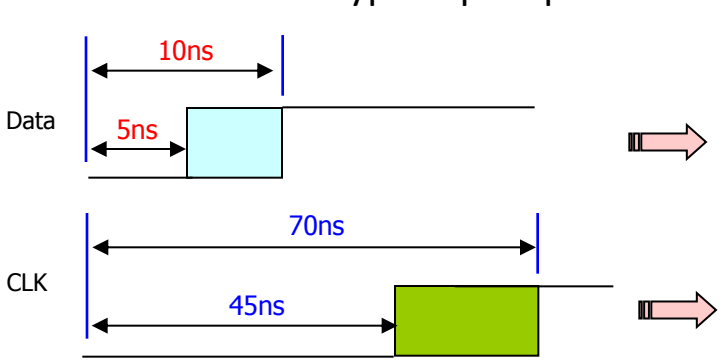


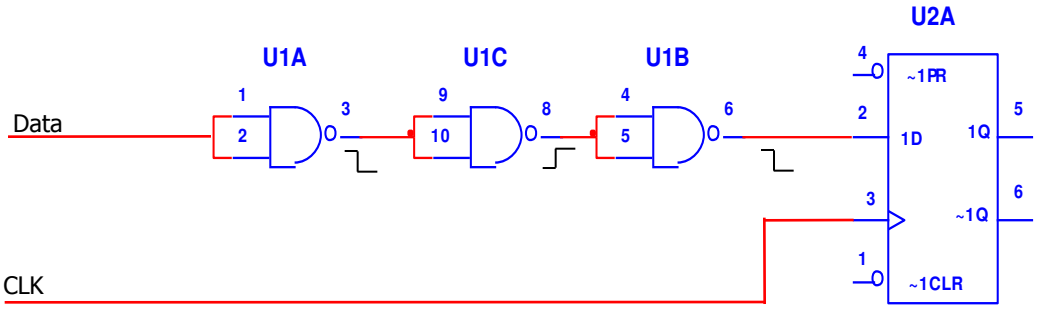

| Parameter | Min | Max |
|---|---|---|
| $t_{PHL}$ | 5ns | 10ns |
| $t_{PLH}$ | 10ns | 20ns |

# Worst Case Loading and Timing Analysis



Given the timing variation inherent in the Data signal below, is it possible that the Setup or Hold time of the D-Type Flip Flop could be violated?




Nand Gate

| Parameter | Min | Max |
|---|---|---|
| $t_{PHL}$ | 5ns | 10ns |
| $t_{PLH}$ | 10ns | 20ns |

D-Type

| Parameter | Min | Max |
|---|---|---|
| $t_{SU}$ | 15ns | |
| $t_{SH}$ | 10ns | |

**Solution**: The is a classical 'race' problem where the Data at the flip flop must arrive at least 15ns (worst case setup time) before the 'Clock'. First calculate the variation in signal timing at the 'D' input to the flip-flop

The fastest path to the D input signal is 5 + 5 + 10 + 5 = 25ns
The slowest path to the D input signal is 10 + 10 + 20 + 10 = 50ns.

To violate the setup time, the CLK signal would need to change less than 15ns after data. One possible example is that the data is at it's slowest (50ns) and the CLK changes anywhere between 50ns and 65ns

To violate the Hold time the D would need to change within 10ns of the clock arriving. This is possible if the data is slow and arrives at say 50ns and the clock arrives at 45ns.