ELEC 402 – Project 4
Cell Library Layout

Charles Clayton
#21518139

Cell	t_{pHL}	t_{pLH}
Inverter	24.9896ps	24.4149ps
NAND2	38.4855ps	43.1166ps
NOR	77.9923ps	36.9710ps

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1   Cell Layouts

- Rail-to-rail separation is 1.71μm from center to center
- Top-to-bottom cell high is 1.9μm
- Supply and ground rails are 0.12μm

1.1   Inverter
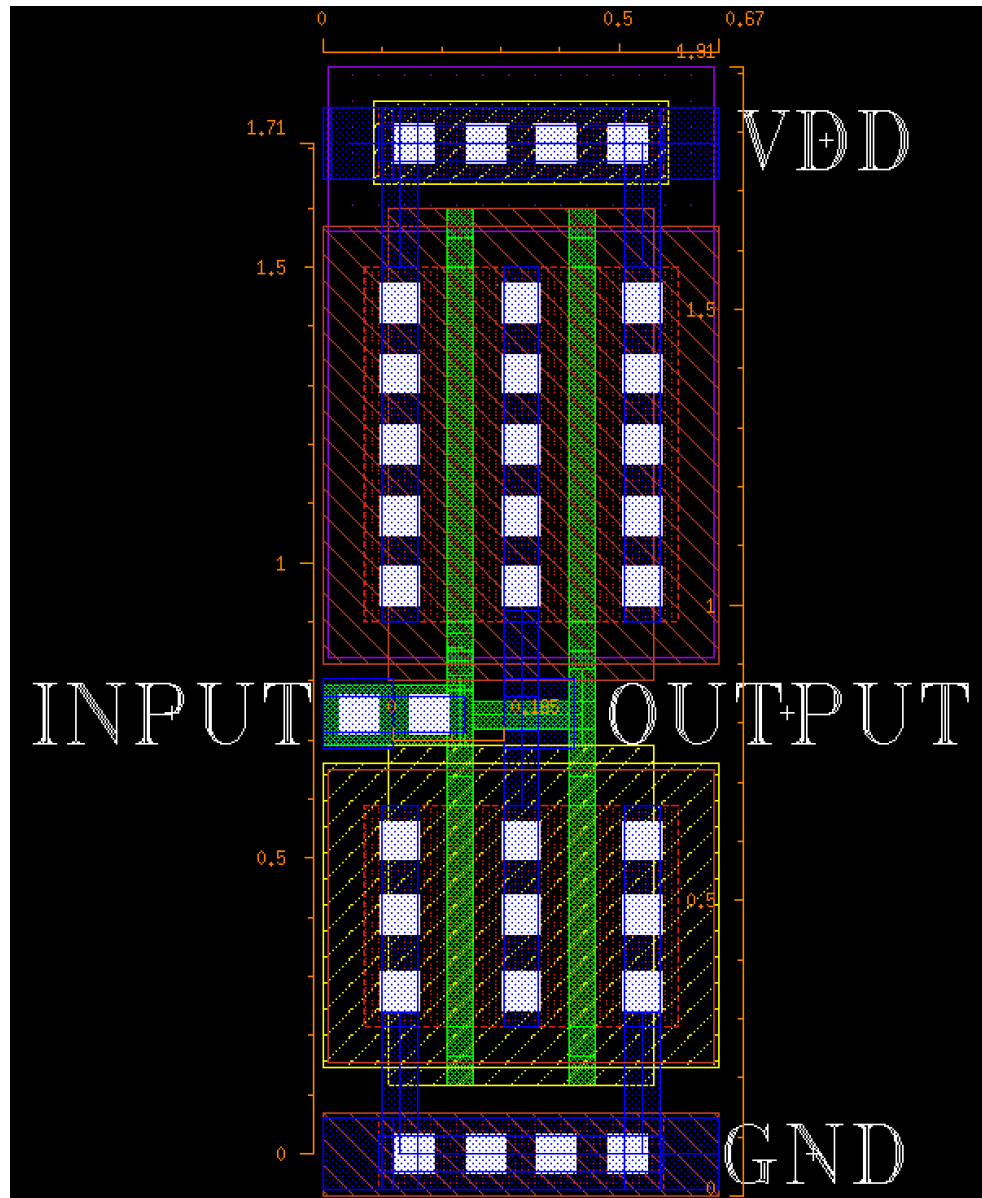

Figure 1: Inverter Layout and Dimensions

Distance between input and output pins is 0.105μm. Width is 0.67μm.
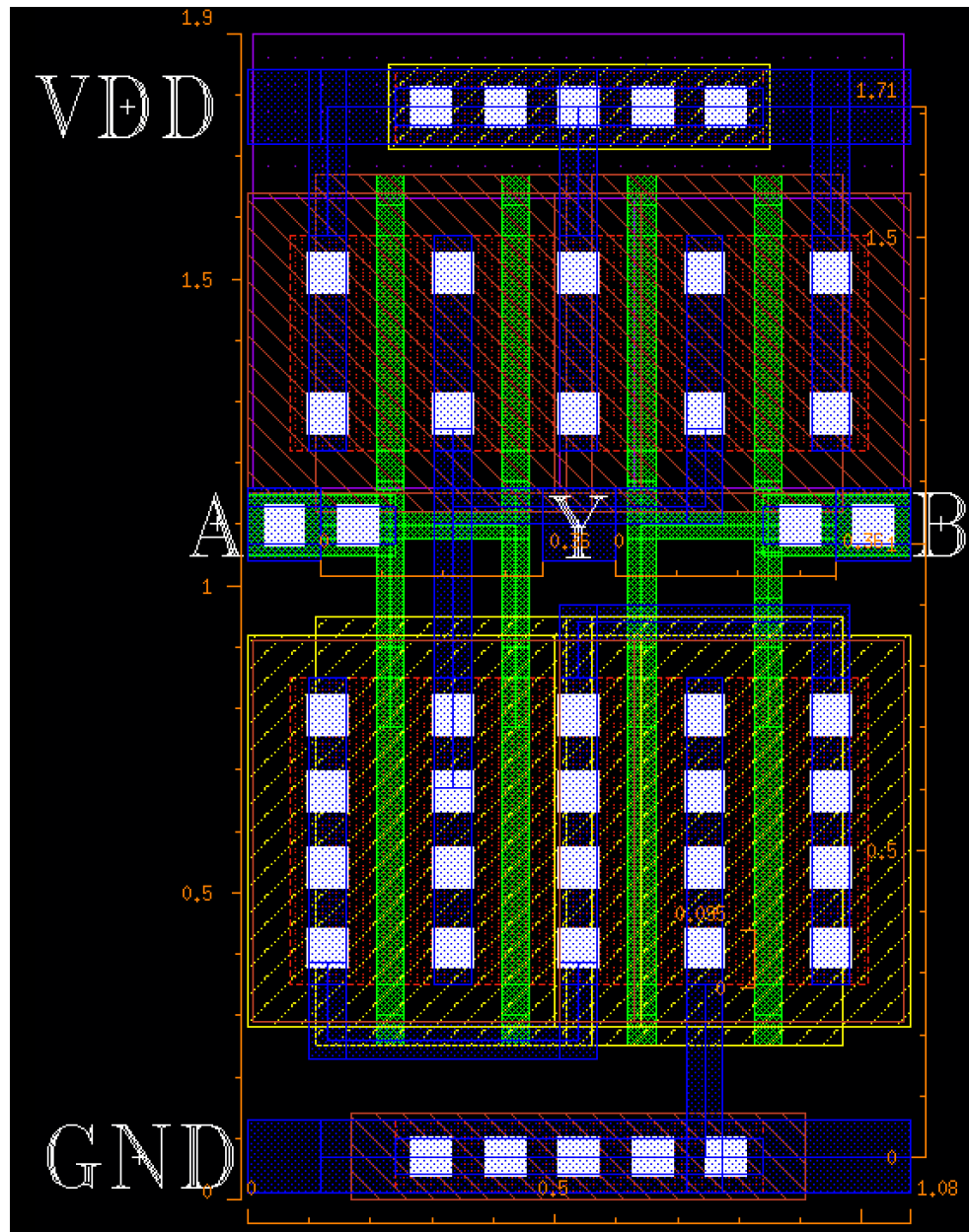
1.2   NAND2

Figure 2: NAND2 Layout and Dimensions

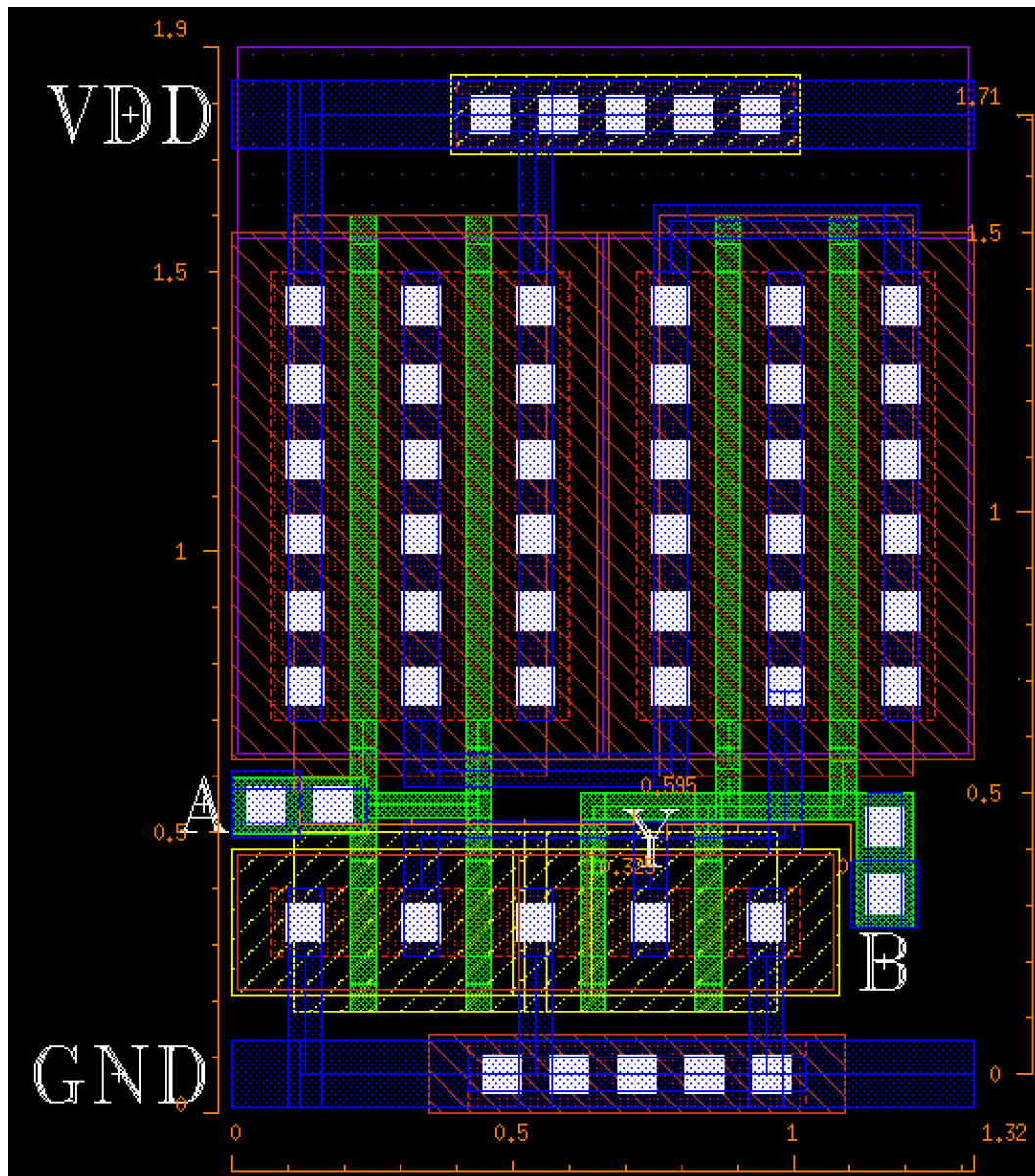Distance from pins A and B to pin Y is 0.36μm. Width is 1.08μm.

1.3   NOR2

Figure 3: NOR2 Layout and Dimensions

Distance from pin A to pin Y 0.325μm, distance from pin B to pin Y is 0.595μm. Width is 1.32μm.

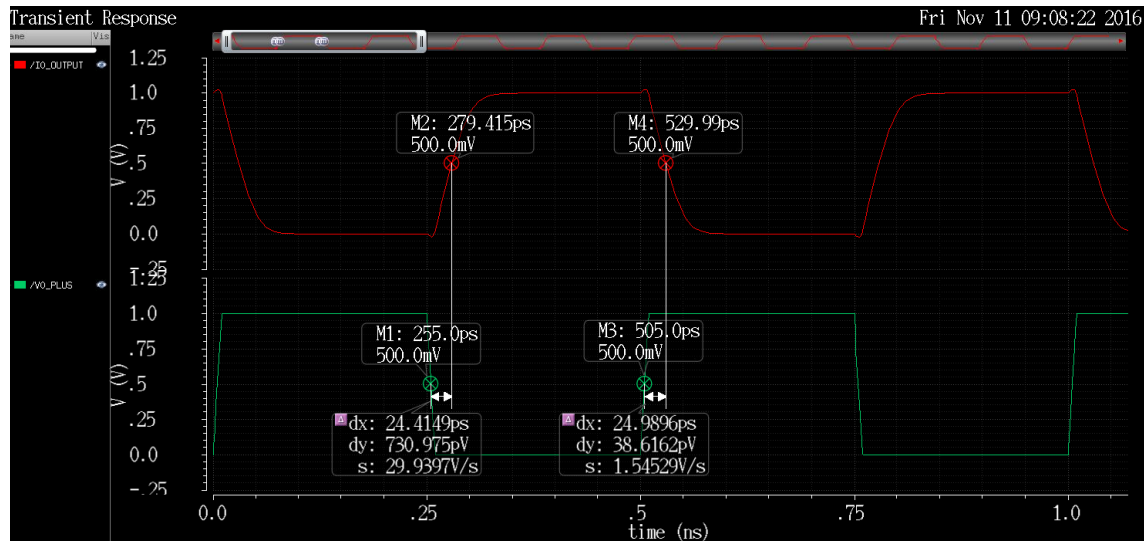# 2 Cell Waveforms and Parasitics

2.1 Inverter

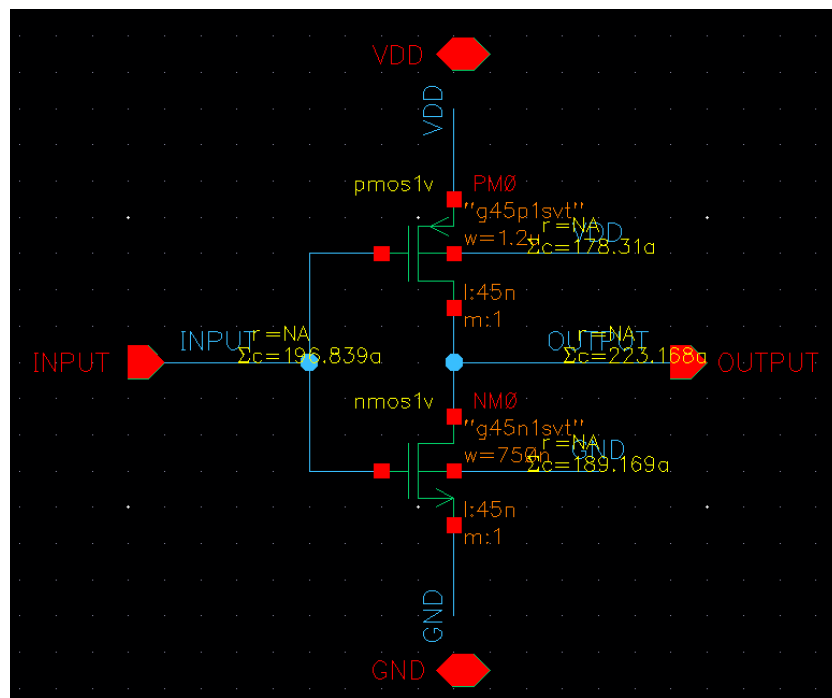Figure 4: Inverter rise time and fall time

Figure 5: Inverter schematic and parasitics

2.2   NAND2

The worst case scenario for the rise time of the NAND2 gate is where B and A are high then B switches to low, because the capacitance between the two NMOS transistors must be charged and there is only one open channel through the pull-up network to charge the output. The worst case for the fall time of the gate is that where both A and B go from low to high simultaneously.
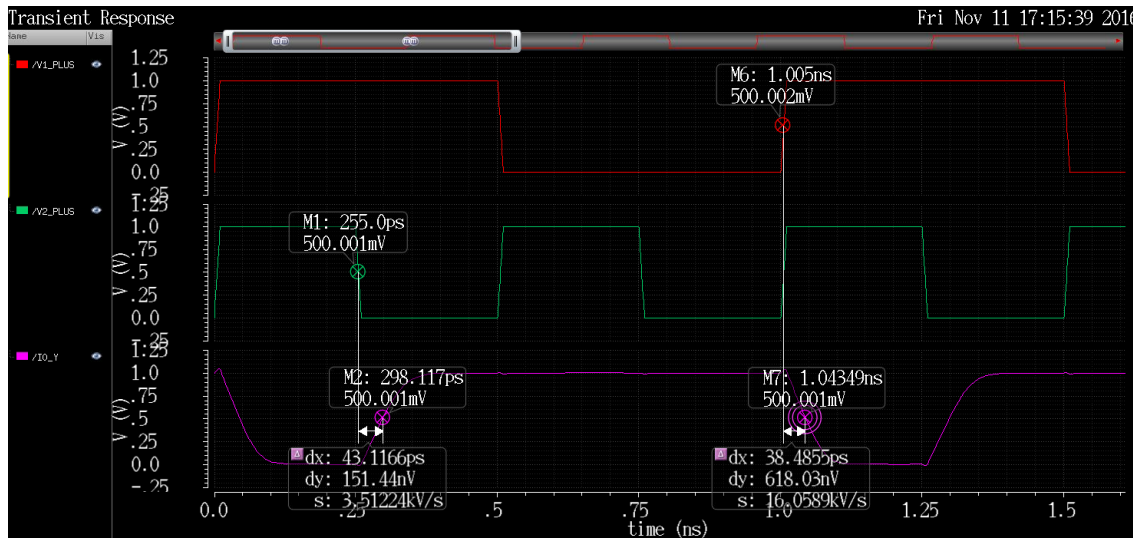

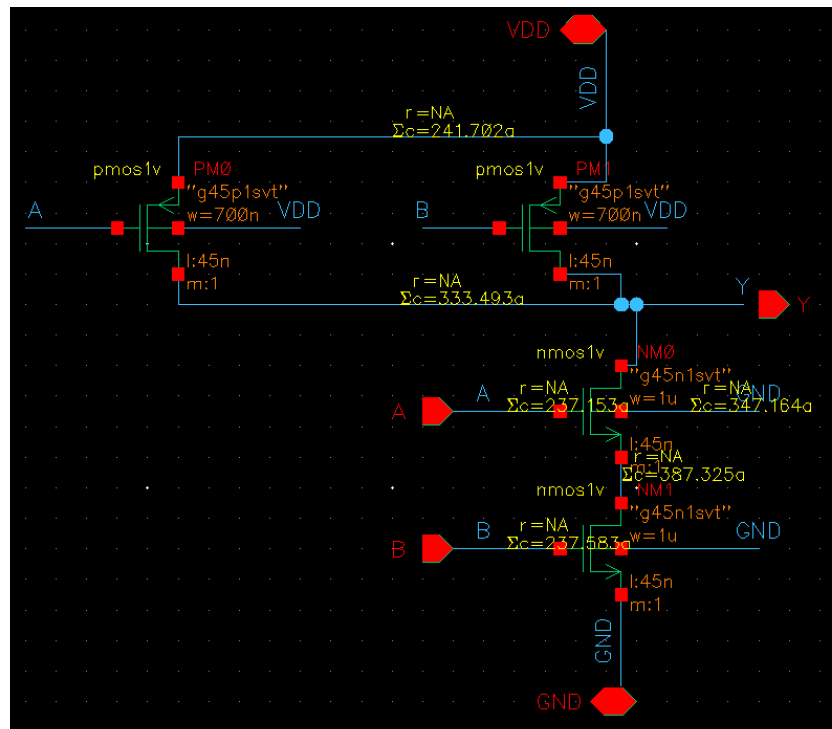Figure 6: NAND2 worst-case rise time and fall time

Figure 7: NAND2 schematic and parasitics

2.3 NOR2

The worst case scenario for the rise time of the NOR2 gate is that where A and B go from high to low simultaneously.
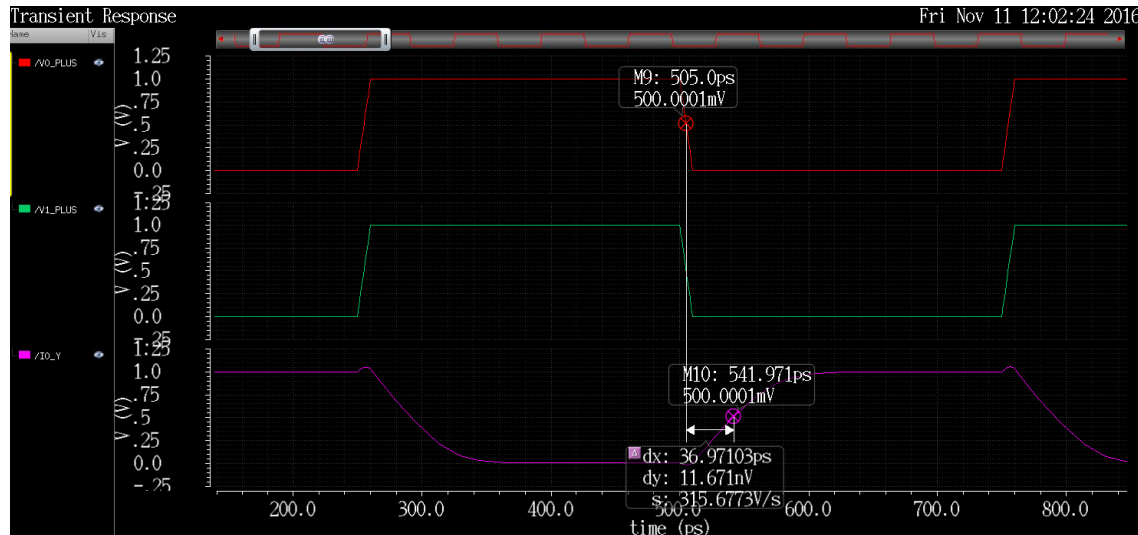

Figure 8: NOR2 worst-case rise time

The worst case for the fall time of the gate is when B stays low and A goes from low to high.
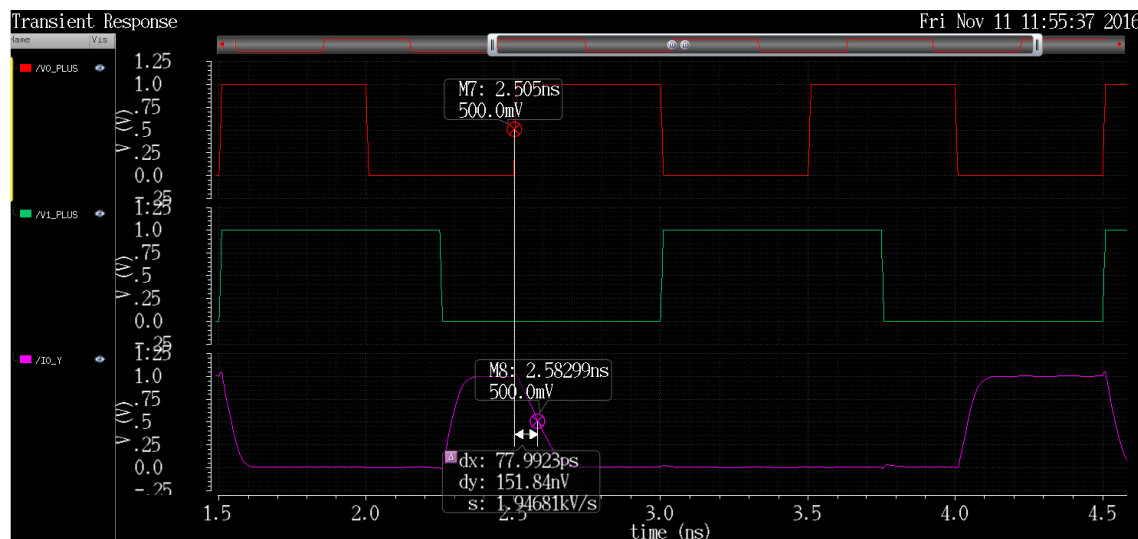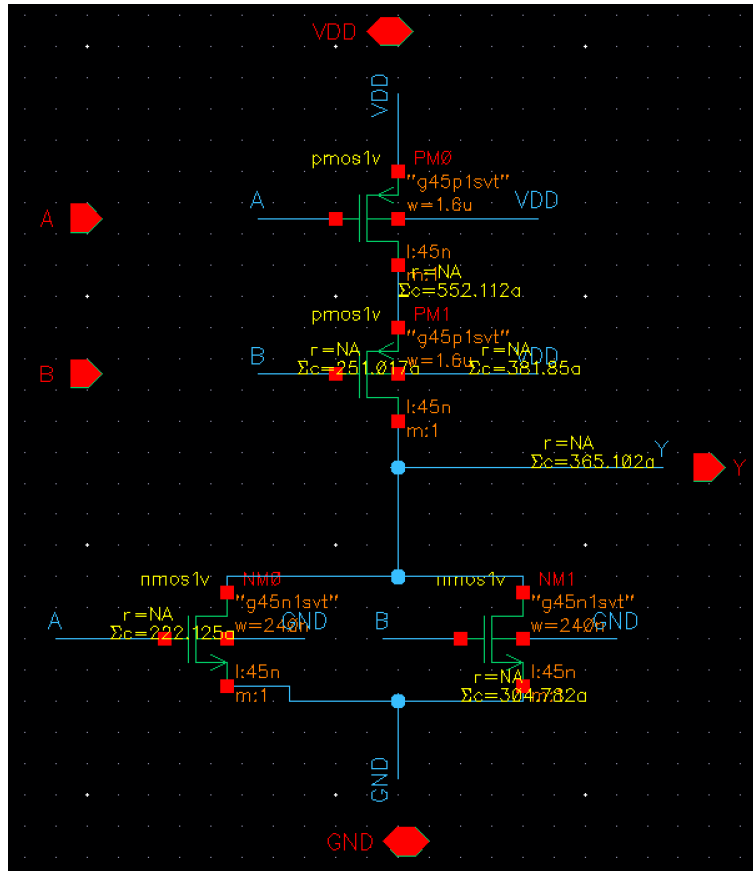

Figure 9: NOR2 worst-case fall time
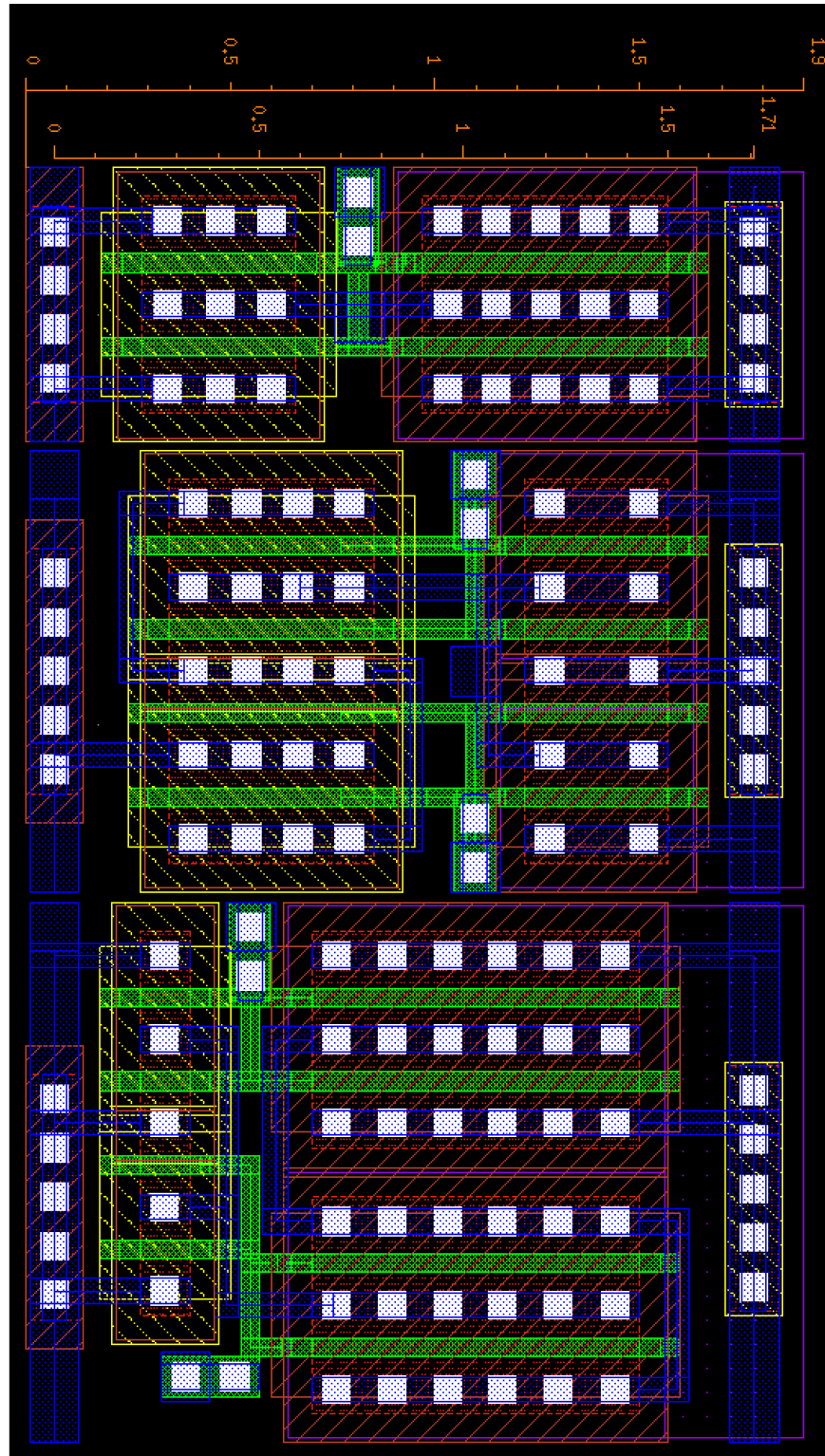
Figure 10: NOR2 schematic and parasitics

3   Cell Alignment

Figure 11: Cells aligned side-by-side (image rotated)