用于窄带系统的高性能射频 (RF) 收发器

特性

- 高性能单片收发器
  - 邻信道选择性：**12.5kHz** 偏移时为 **65dB**
  - 阻断性能：**10MHz** 时为 **90dB**
  - 出色的接收器灵敏度：
    - **1.2kbps** 时为 **123dBm**
    - **50kbps** 时为 **110dBm**
    - **127dBm** 使用内置编码增益
  - 低相位噪声：**10kHz** 偏移时为 **-111dBc/Hz**
- 适合面向欧洲电信标准协会 **(ETSI)** 类别**1** 符合 **169MHz** 和**433MHz** 频带标准的系统
- 高频谱效率（**12.5kHz** 信道中为 **9.6kbps** 与联邦通信委员会 **(FCC)** 窄带命令兼容
- 电源
  - 宽输入电源电压范围 **(2V-3.6V)**
  - 低流耗：
    - **RX**：**RX** 嗅探模式时为 **2mA**
    - **RX**：在低功率模式中峰值电流为 **17mA**
    - **RX**：在高性能模式中峰值电流为 **22 mA**
    - **TX**：**45mA+14dBm**
  - 断电模式时：**0.3μA**
  - 步长为 **0.4dB**，最高 **16dBm** 的可编程输出功率
  - 自动输出功率递增
  - 可配置数据传输速率：**0** 至 **200kbps**
  - 支持的调制格式：**2-FSK**，**2-GFSK**，**4-FSK**，**4-GFSK**，**MSK**，**OOK**
  - 波形监视：针对改进的同步检测性能的高级数字信号处理
  - 符合 **RoHS** 标准的 **5 x 5mm** 四方扁平无引线 **(QFN) 32** 封装

应用范围

- 信道间隔低至 **12.5kHz** 的窄带超低功耗无线系统
- **170/315/433/868/915/950MHz ISM/SRD** 频带
- 无线计量和无线智能电网（**AMR** 和 **AMI**）
- **IEEE 802.15.4g** 系统
- 家庭和楼宇自动化
- 无线警报和安全系统
- 工业用监控和控制
- 无线医疗应用
- 无线传感器网络和有源射频识别 **(RFID)**
- 私有移动无线电

符合的规范

- 欧洲 **- ETSI EN 300 220**，**ETSI EN 54-25**
- 美国 **- FCC CRF47** 部分 **15**，**FCC CFR47** 部分**90**，**24** 和 **101**
- 日本 **- ARIB RCR STD-T30**，**ARIB STD-T67**，**ARIB STD-T96**

外设和支持功能

- 针对自动低功耗接收轮询的增强型无线电唤醒功能
- 独立的 **128** 字节 **RX** 和 **TX** 先进先出 **(FIFO)**
- 包括针对天线多样性支持的功能
- 支持重传
- 支持对接收到的数据包进行自动应答
- **TCXO** 支持和控制，在功率模式中也是如此
- 针对对话前监听 **(LBT)** 系统的自动空闲信道评估 **(CCA)**
- 针对增加的范围和耐用性的内置编码增益支持
- 数字接收到的信号强度指示 **(RSSI)** 测量
- 支持与 **CC1190** 的无缝集成以实现范围扩展，使敏感度提升 **3dB** 和并提供高达 **+27dBm** 的输出功率

说明

CC1120 是一款完全集成的单片无线电收发器，此无线电收发器设计用于在经济高效的无线系统中的低功耗和低电压操作上实现高性能。 所有滤波器都已集成，因此无需昂贵的外部声表面波 (SAW) 和中频 (IF) 滤波器。 该器件主要用于 ISM（工业、科学和医疗）应用以及处于 164-192MHz，410-480MHz 和 820-960MHz 上的 SRD（短程器件） 频带。

CC1120 提供扩展硬件，以支持数据包处理、数据缓冲、突发传输、空闲信道评估、链路质量指示和无线电唤醒。 CC1120 主要运行参数可以通过串行外设接口 (SPI) 接口控制。 在典型系统中，CC1120 将与一个微控制器和极少的外部无源组件配合使用。

English Data Sheet: SWRS112

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DEVICE INFORMATION

3 Pin Configuration

Pin Number	Pin name	Type / direction	Description
1	vdd_guard	Power	3 V VDD
2	reset_n	Digital Input	Asynchronous, active-low digital reset
3	gpio3	Digital Input/Output	General purpose IO
4	gpio2	Digital Input/Output	General purpose IO
5	dvdd	Power	3 V VDD to internal digital regulator
6	dcpl	Power	Digital regulator output to external C
7	si	Digital Input	Serial data in
8	sclk	Digital Input	Serial data clock
9	so(gpio1)	Digital Input/Output	Serial data out (General purpose IO)
10	gpio0	Digital Input/Output	General purpose IO
11	cs_n	Digital Input	Active-low chip-select
12	dvdd	Power	3 V VDD
13	avdd_if	Power	3 V VDD
14	rbias	Analog	External high precision R
15	avdd_rf	Power	3 V VDD
16	not connected		
17	pa	Analog	Single-ended TX output
18	trx_sw	Analog	TX/RX switch
19	lna_p	Analog	Differential RX input
20	lna_n	Analog	Differential RX input
21	dcpl_vco	Power	Pin for external decoupling of VCO supply regulator
22	avdd_synth1	Power	3 V VDD
23	lpf0	Analog	External loopfilter components
24	lpf1		External loopfilter components
25	avdd_pfd_chp	Power	3 V VDD
26	dcpl_pfd_chp	Power	Pin for external decoupling of PFD and CHP regulator
27	avdd_synth2	Power	3 V VDD
28	avdd_xosc	Power	3 V VDD
29	dcpl_xosc	Power	Pin for external decoupling of XOSC supply regulator
30	xosc_q1	Analog	Crystal oscillator pin 1 (must be grounded if a TCXO or other external clock connected to ext_xosc is used)
31	xosc_q2	Analog	Crystal oscillator pin 2 (must be left floating if a TCXO or other external clock connected to ext_xosc is used)
32	ext_xosc	Digital Input	Pin for external xosc input (must be grounded if a regular xosc connected to xosc_q1 and xosc_2 is used)

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1 Electrical Specifications

All measurements performed on CC1120EM_868_915 rev.1.0.1, CC1120EM_955 rev.1.2.1, CC1120EM_420_470 rev.1.0.1 or CC1120EM_169 rev.1.2

1.1 Absolute Max Ratings

Parameter	Min	Typ	Max	Unit	Condition
Supply Voltage	-0.3		3.9	V	
Storage Temperature Range	-40		125	℃	
ESD			2000	V	HBM
ESD			500	V	CDM
Input RF level			+10	dBm	
Voltage on Any Digital Pin	-0.3		3.9	V	
Voltage on Analog Pins (including "DCPL" pins)	-0.3		2.0	V	

1.2 General Characteristics

Parameter	Min	Typ	Max	Unit	Condition
Voltage Supply Range	2.0		3.6	V	
Temperature Range	-40		85	℃	

1.3 RF Characteristics

Parameter	Min	Typ	Max	Unit	Condition
Frequency Bands	820		960	MHz	
	410		480	MHz	
	274		320	MHz	Please see application note AN115 "*Using the CC112x/CC1175 at 274 to 320 MHz*" for more information
	164		192	MHz	
Frequency Resolution		30		Hz	In 820-960 MHz band
		15		Hz	In 410-480 MHz band
		6		Hz	In 164-192 MHz band
Datarate	0		200	kbps	Packet mode
	0		100	kbps	Transparent mode
Datarate Step Size		1e-4		bps	

1.4 Regulatory Standards

Performance Mode	Frequency Band	Suitable for compliance with	Comments
High Performance Mode	820 – 960 MHz	ARIB T-96 ETSI EN 300 220 category 2 ETSI EN 54-25 FCC PART 101 FCC PART 24 SUBMASK D FCC PART 15.247 FCC PART 15.249 FCC PART 90 MASK G FCC PART 90 MASK J	Performance also suitable for systems targeting maximum allowed output power in the respective bands, using a range extender such as the CC1190
	410 – 480 MHz	ARIB T-67 ARIB RCR STD-30 ETSI EN 300 220 category 1 FCC PART 90 MASK D FCC PART 90 MASK G	Performance also suitable for systems targeting maximum allowed output power in the respective bands, using a range extender
	164 – 192 MHz	ETSI EN 300 220 category 1 FCC PART 90 MASK D	Performance also suitable for systems targeting maximum allowed output power in the respective bands, using a range extender
Low Power Mode	820 – 960 MHz	ETSI EN 300 220 FCC PART 15.247 FCC PART 15.249	
	410 – 480 MHz	ETSI EN 300 220	
	164 – 192 MHz	ETSI EN 300 220	

1.5 Current Consumption, Static Modes

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Power Down with Retention		0.3	1	µA	
		0.5		µA	Low-power RC oscillator running
XOFF Mode		170		µA	Crystal oscillator / TCXO disabled
IDLE Mode		1.3		mA	Clock running, system waiting with no radio activity

1.6 Current Consumption, Transmit Modes

950 MHz band (High Performance Mode)

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
TX Current Consumption +10 dBm		37		mA	
TX Current Consumption 0 dBm		26		mA	

868/915 MHz bands (High Performance Mode)

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
TX Current Consumption +14 dBm		45		mA	
TX Current Consumption +10 dBm		34		mA	

434 MHz band (High Performance Mode)

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
TX Current Consumption +15 dBm		50		mA	
TX Current Consumption +14 dBm		45		mA	
TX Current Consumption +10 dBm		34		mA	

170 MHz band (High Performance Mode)

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
TX Current Consumption +15 dBm		54		mA	
TX Current Consumption +14 dBm		49		mA	
TX Current Consumption +10 dBm		41		mA	

Low Power Mode

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
TX Current Consumption +10 dBm		32		mA	

1.7 Current Consumption, Receive Modes

High Performance Mode

T_A = 25℃, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
RX Wait for Sync 1.2 kbps, 4 Byte Preamble 38.4kbps, 4 Byte Preamble		 2 13.4		 mA mA	Using RX Sniff Mode, where the receiver wakes up at regular intervals to look for an incoming packet
RX Peak Current 433, 868/915 and 950 MHz bands 170 MHz band		 22 23		 mA mA	Peak current consumption during packet reception at the sensitivity threshold
Average Current Consumption Check for Data Packet Every 1 Second Using Wake on Radio		15		uA	50 kbps, 5 byte preamble, 32 kHz RC oscillator used as sleep timer

Low Power Mode

T_A = 25℃, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
RX Peak Current Low power RX mode 1.2 kbps		 17		 mA	Peak current consumption during packet reception at the sensitivity level

1.8 Receive Parameters[1]

General Receive Parameters (High Performance Mode)

T_A = 25℃, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Saturation		+10		dBm	
Digital Channel Filter Programmable Bandwidth	8		200	kHz	
IIP3, Normal Mode		-14		dBm	At maximum gain
IIP3, High Linearity Mode		-8		dBm	Using 6 dB gain reduction in front end
Datarate Offset Tolerance		±12 ±0.2		% %	With carrier sense detection enabled and assuming 4 byte preamble With carrier sense detection disabled
Spurious Emissions 1 - 13 GHz (VCO leakage at 3.5 GHz) 30 MHz to 1 GHz		 -56 < -57		 dBm dBm	Radiated emissions measured according to ETSI EN 300 220, f_c = 869.5 MHz

[1] All RX measurements made at the antenna connector, to a bit error rate limit of 1%

RX performance in 950 MHz band (High Performance Mode)

T_A = 25℃, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Sensitivity Note: Sensitivity can be improved if the TX and RX matching networks are separated.		-120		dBm	1.2 kbps, DEV=4 kHz CHF=10 kHz[2]
		-114		dBm	1.2 kbps, DEV=20 kHz CHF=50 kHz
		-107		dBm	50 kbps 2GFSK, DEV=25 kHz, CHF=100 kHz
		-100		dBm	200 kbps, DEV=83 kHz (outer symbols), CHF=200 kHz, 4GFSK[3]
Blocking and Selectivity 1.2 kbps 2FSK, 12.5 kHz channel separation, 4 kHz deviation, 10 kHz channel filter		51		dB	± 12.5 kHz (adjacent channel)
		52		dB	± 25 kHz (alternate channel)
		73		dB	± 1 MHz
		76		dB	± 2 MHz
		81		dB	± 10 MHz
Blocking and Selectivity 1.2 kbps 2FSK, 50 kHz channel separation, 20 kHz deviation, 50 kHz channel filter		47		dB	± 50 kHz (adjacent channel)
		48		dB	+ 100 kHz (alternate channel)
		69		dB	± 1 MHz
		71		dB	± 2 MHz
		78		dB	± 10 MHz
Blocking and Selectivity 50 kbps 2GFSK, 200 kHz channel separation, 25 kHz deviation, 100 kHz channel filter (Same modulation format as 802.15.4g Mandatory Mode)		43		dB	± 200 kHz (adjacent channel)
		51		dB	± 400 kHz (alternate channel)
		62		dB	± 1 MHz
		65		dB	± 2 MHz
		71		dB	± 10 MHz
Blocking and Selectivity 200 kbps 4GFSK, 83 kHz deviation (outer symbols), 200 kHz channel filter, zero IF		37		dB	± 200 kHz (adjacent channel)
		44		dB	± 400 kHz (alternate channel)
		55		dB	± 1 MHz
		58		dB	± 2 MHz
		64		dB	± 10 MHz

[2] DEV is short for deviation, CHF is short for Channel Filter Bandwidth

[3] BT=0.5 is used in all GFSK measurements

RX performance in 868/915 MHz bands (High Performance Mode)

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Sensitivity		-127		dBm	300 bps with coding gain (using a PN spreading sequence with 4 chips per databit)
		-123		dBm	1.2 kbps, DEV=4 kHz CHF=10 kHz
		-117		dBm	1.2 kbps, DEV=20 kHz CHF=50 kHz
		-114		dBm	4.8 kbps OOK
		-110		dBm	38.4 kbps, DEV=50 kHz CHF=100 kHz
		-110		dBm	50 kbps 2GFSK, DEV=25 kHz, CHF=100 kHz
		-103		dBm	200 kbps, DEV=83 kHz (outer symbols), CHF=200 kHz, 4GFSK
Blocking and Selectivity 1.2 kbps 2FSK, 12.5 kHz channel separation, 4 kHz deviation, 10 kHz channel filter		54		dB	± 12.5 kHz (adjacent channel)
		54		dB	± 25 kHz (alternate channel)
		75		dB	± 1 MHz
		79		dB	± 2 MHz
		87		dB	± 10 MHz
Blocking and Selectivity 1.2 kbps 2FSK, 50 kHz channel separation, 20 kHz deviation, 50 kHz channel filter		48		dB	± 50 kHz (adjacent channel)
		48		dB	+ 100 kHz (alternate channel)
		69		dB	± 1 MHz
		74		dB	± 2 MHz
		81		dB	± 10 MHz
Blocking and Selectivity 38.4 kbps 2GFSK, 100 kHz channel separation, 20 kHz deviation, 100 kHz channel filter		42		dB	+ 100 kHz (adjacent channel)
		43		dB	± 200 kHz (alternate channel)
		62		dB	± 1 MHz
		66		dB	± 2 MHz
		74		dB	± 10 MHz
Blocking and Selectivity 50 kbps 2GFSK, 200 kHz channel separation, 25 kHz deviation, 100 kHz channel filter (Same modulation format as 802.15.4g Mandatory Mode)		43		dB	± 200 kHz (adjacent channel)
		50		dB	± 400 kHz (alternate channel)
		61		dB	± 1 MHz
		65		dB	± 2 MHz
		74		dB	± 10 MHz
Blocking and Selectivity 200 kbps 4GFSK, 83 kHz deviation (outer symbols), 200 kHz channel filter, zero IF		36		dB	± 200 kHz (adjacent channel)
		44		dB	± 400 kHz (alternate channel)
		55		dB	± 1 MHz
		59		dB	± 2 MHz
		67		dB	± 10 MHz
Image Rejection (Image compensation enabled)		54		dB	1.2 kbps, 12.5 kHz channel separation, FSK, image at -125 kHz

RX performance in 434 MHz band (High Performance Mode)

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Sensitivity		-123		dBm	1.2 kbps, DEV=4 kHz CHF=10 kHz
		-109		dBm	50 kbps 2GFSK, DEV=25 kHz, CHF=100 kHz
		-116		dBm	1.2 kbps, DEV=20 kHz CHF=50 kHz
Blocking and Selectivity 1.2 kbps 2FSK, 12.5 kHz channel separation, 4 kHz deviation, 10 kHz channel filter		60		dB	± 12.5 kHz (adjacent channel)
		60		dB	± 25 kHz (alternate channel)
		79		dB	± 1 MHz
		82		dB	± 2 MHz
		91		dB	± 10 MHz
Blocking and Selectivity 1.2 kbps 2FSK, 50 kHz channel separation, 20 kHz deviation, 50 kHz channel filter		54		dB	± 50 kHz (adjacent channel)
		54		dB	+ 100 kHz (alternate channel)
		74		dB	± 1 MHz
		78		dB	± 2 MHz
		86		dB	± 10 MHz
Blocking and Selectivity 38.4 kbps 2GFSK, 100 kHz channel separation, 20 kHz deviation, 100 kHz channel filter		47		dB	+ 100 kHz (adjacent channel)
		50		dB	± 200 kHz (alternate channel)
		67		dB	± 1 MHz
		71		dB	± 2 MHz
		78		dB	± 10 MHz

RX performance in 170 MHz band (High Performance Mode)

T_A = 25℃, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Sensitivity		-123		dBm	1.2 kbps, DEV=4 kHz CHF=10 kHz
		-117		dbm	1.2 kbps, DEV=20 kHz CHF=50 kHz
Blocking and Selectivity 1.2 kbps 2FSK, 12.5 kHz channel separation, 4 kHz deviation, 10 kHz channel filter		64		dB	± 12.5 kHz (adjacent channel)
		66		dB	± 25 kHz (alternate channel)
		82		dB	± 1 MHz
		83		dB	± 2 MHz
		89		dB	± 10 MHz
Blocking and Selectivity 1.2 kbps 2FSK, 50 kHz channel separation, 20 kHz deviation, 50 kHz channel filter		60		dB	± 50 kHz (adjacent channel)
		60		dB	+ 100 kHz (alternate channel)
		76		dB	± 1 MHz
		77		dB	± 2 MHz
		83		dB	± 10 MHz
Spurious Response Rejection 1.2 kbps 2FSK, 12.5 kHz channel separation, 4 kHz deviation, 10 kHz channel filter		70		dB	
Image Rejection (Image compensation enabled)		66		dB	1.2 kbps, 12.5 kHz channel separation, FSK, image at -125 kHz

RX performance in Low Power Mode

T_A = 25℃, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Sensitivity		-111		dBm	1.2 kbps, DEV=4 kHz CHF=10 kHz
		-99		dBm	38.4 kbps, DEV=50 kHz CHF=100 kHz
		-99		dBm	50 kbps 2GFSK, DEV=25 kHz, CHF=100 kHz
Blocking and Selectivity 1.2 kbps 2FSK, 12.5 kHz channel separation, 4 kHz deviation, 10 kHz channel filter		46		dB	± 12.5 kHz (adjacent channel)
		46		dB	± 25 kHz (alternate channel)
		73		dB	± 1 MHz
		78		dB	± 2 MHz
		79		dB	± 10 MHz
Blocking and Selectivity 1.2 kbps 2FSK, 50 kHz channel separation, 20 kHz deviation, 50 kHz channel filter		43		dB	± 50 kHz (adjacent channel)
		45		dB	+ 100 kHz (alternate channel)
		71		dB	± 1 MHz
		74		dB	± 2 MHz
		75		dB	± 10 MHz
Blocking and Selectivity 38.4 kbps 2GFSK, 100 kHz channel separation, 20 kHz deviation, 100 kHz channel filter		37		dB	+ 100 kHz (adjacent channel)
		43		dB	+ 200 kHz (alternate channel)
		58		dB	± 1 MHz
		62		dB	± 2 MHz
		64		dB	+ 10 MHz
Blocking and Selectivity 50 kbps 2GFSK, 200 kHz channel separation, 25 kHz deviation, 100 kHz channel filter (Same modulation format as 802.15.4g Mandatory Mode)		43		dB	+ 200 kHz (adjacent channel)
		52		dB	+ 400 kHz (alternate channel)
		60		dB	± 1 MHz
		64		dB	± 2 MHz
		65		dB	± 10 MHz
Saturation		+10		dBm	

1.9 Transmit Parameters

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Max Output Power		+12			At 950 MHz
		+14 +15			At 915 MHz At 915 MHz with VDD = 3.6 V
		+15 +16			At 868 MHz At 868 MHz with VDD = 3.6 V
		+15 +16			At 433 MHz At 433 MHz with VDD = 3.6 V
		+15 +16			At 170 MHz At 170 MHz with VDD = 3.6 V
Min Output Power		-11 -40		dBm dBm	Within fine step size range Within coarse step size range
Output Power Step Size		0.4		dB	Within fine step size range
Adjacent Channel Power		-75		dBc	4-GFSK 9.6 kbps in 12.5 kHz channel, measured in 100 Hz bandwidth at 434 MHz (FCC Part 90 Mask D compliant)
		-58		dBc	4-GFSK 9.6 kbps in 12.5 kHz channel, measured in 8.75 kHz bandwidth (ETSI 300 220 compliant)
		-61		dBc	2-GFSK 2.4 kbps in 12.5 kHz channel, 1.2 kHz deviation
Spurious Emissions (Not including harmonics)		< -60		dBm	
Harmonics 2nd Harm, 170 MHz 3rd Harm, 170 MHz 2nd Harm, 433 MHz 3rd Harm, 433 MHz 2nd Harm, 450 MHz 3rd Harm, 450 MHz 2nd Harm, 868 MHz 3rd Harm, 868 MHz 2nd Harm, 915 MHz 3rd Harm, 915 MHz 4th Harm, 915 MHz 2nd Harm, 950 MHz 3rd Harm, 950 MHz		 -39 -58 -56 -51 -60 -45 -40 -42 56 52 60 -58 -42		 dBm dBm dBm dBm dBm dBm dBm dBm dBuV/m dBuV/m dBuV/m dBm dBm	Transmission at +14 dBm (or maximum allowed in applicable band where this is less than +14dBm) using TI reference design Radiated emissions measured according to ARIB T-96 in 950 MHz band, ETSI EN 300-220 in 170, 433 and 868 MHz bands and FCC part 15.247 in 450 and 915 MHz band Fourth harmonic in 915 MHz band will require extra filtering to meet FCC requirements if transmitting in long intervals (>50 ms periods)

1.10 PLL Parameters

High Performance Mode

T_A = 25℃, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Phase Noise in 950 MHz Band		-99		dBc/Hz	± 10 kHz offset
		-99		dBc/Hz	± 100 kHz offset
		-123		dBc/Hz	± 1 MHz offset
Phase Noise in 868/915 MHz Bands		-99		dBc/Hz	± 10 kHz offset
		-100		dBc/Hz	± 100 kHz offset
		-122		dBc/Hz	± 1 MHz offset
Phase Noise in 433 MHz Band		-106		dBc/Hz	± 10 kHz offset
		-107		dBc/Hz	± 100 kHz offset
		-127		dBc/Hz	± 1 MHz offset
Phase Noise in 170 MHz Band		-111		dBc/Hz	± 10 kHz offset
		-116		dBc/Hz	± 100 kHz offset
		-135		dBc/Hz	± 1 MHz offset

Low Power Mode

T_A = 25℃, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Phase Noise in 950 MHz Band		-90		dBc/Hz	± 10 kHz offset
		-92		dBc/Hz	± 100 kHz offset
		-124		dBc/Hz	± 1 MHz offset
Phase Noise in 868/915 MHz Bands		-95		dBc/Hz	± 10 kHz offset
		-95		dBc/Hz	± 100 kHz offset
		-124		dBc/Hz	± 1 MHz offset
Phase Noise in 433 MHz Band		-98		dBc/Hz	± 10 kHz offset
		-102		dBc/Hz	± 100 kHz offset
		-129		dBc/Hz	± 1 MHz offset
Phase Noise in 170 MHz Band		-106		dBc/Hz	± 10 kHz offset
		-110		dBc/Hz	± 100 kHz offset
		-136		dBc/Hz	± 1 MHz offset

1.11 Wake-up and Timing

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Powerdown to IDLE		0.4		ms	Depends on crystal
IDLE to RX/TX		166		µs	Calibration disabled
		461		µs	Calibration enabled
RX/TX Turnaround		50		µs	
RX/TX to IDLE time		296		µs	Calibrate when leaving RX/TX enabled
		0		µs	Calibrate when leaving RX/TX disabled
Frequency Synthesizer Calibration		0.4		ms	When using SCAL strobe
Minimum Required Number of Preamble Bytes		0.5		bytes	Required for RF front end gain settling only. Digital demodulation does not require preamble for settling
Time From Start RX Until Valid RSSI		4.6		ms	12.5 kHz channels
Including gain settling (function of channel bandwidth. Programmable for trade-off between speed and accuracy)		0.3		ms	200 kHz channels

1.12 32 MHz Crystal Oscillator

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Crystal Frequency	32		33.6	MHz	Note: It is recommended that the crystal frequency is chosen so that the RF channel(s) are >1 MHz away from multiples of XOSC in TX and XOSC/2 in RX
Load Capacitance (C_L)		10		pF	
ESR			60	Ω	Simulated over operating conditions
Start-up Time		0.4		ms	Depends on crystal

1.13 32 MHz Clock Input (TCXO)

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Clock Frequency	32		33.6	MHz	
Clock input amplitude (peak-to-peak)	0.8		VDD	V	Simulated over operating conditions

1.14 32 kHz Clock Input

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Clock Frequency		32		kHz	
32 kHz Clock Input Pin Input High Voltage	0.8×VDD			V	
32 kHz Clock Input Pin Input Low Voltage			0.2×VDD	V	

1.15 32 kHz RC Oscillator

T_A = 25°C, VDD = 3.0 V if nothing else stated.

Parameter	Min	Typ	Max	Unit	Condition
Frequency		32		kHz	After Calibration
Frequency Accuracy After Calibration		±0.1		%	Relative to frequency reference (i.e. 32 MHz crystal or TCXO)
Initial Calibration Time		1.6		ms	

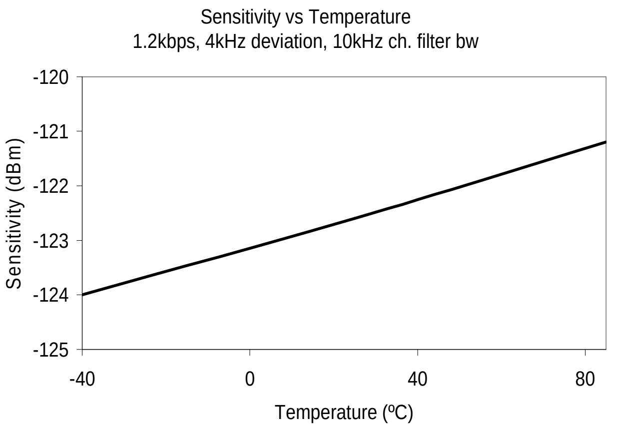
1.16 I/O and Reset

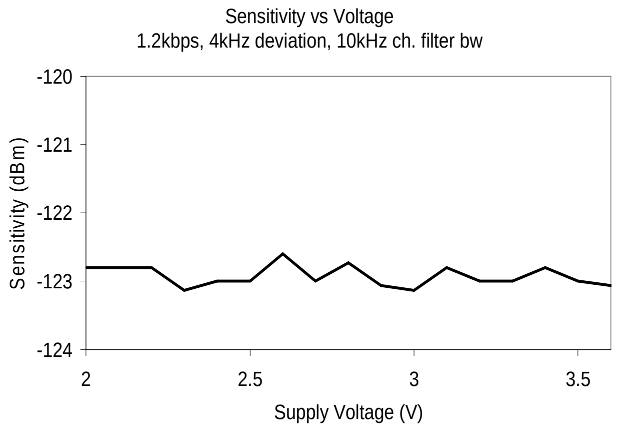
T_A = 25°C, VDD = 3.0 V if nothing else stated

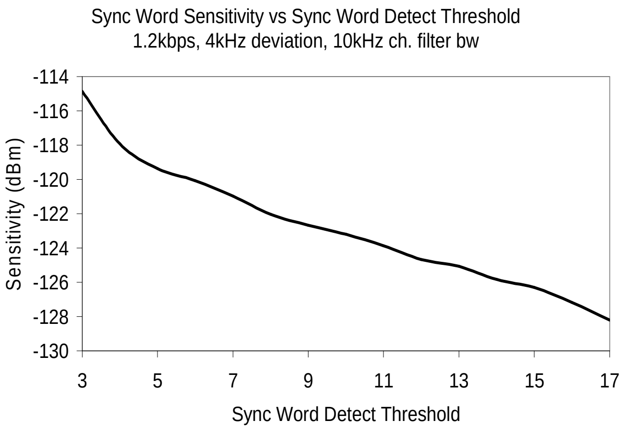
Parameter	Min	Typ	Max	Unit	Condition
Logic Input High Voltage	0.8×VDD			V	
Logic Input Low Voltage			0.2×VDD	V	
Logic Output High Voltage	0.8×VDD			V	At 4 mA output load or less
Logic Output Low Voltage			0.2×VDD	V	
Power-on Reset Threshold		1.3		V	Voltage on DVDD pin

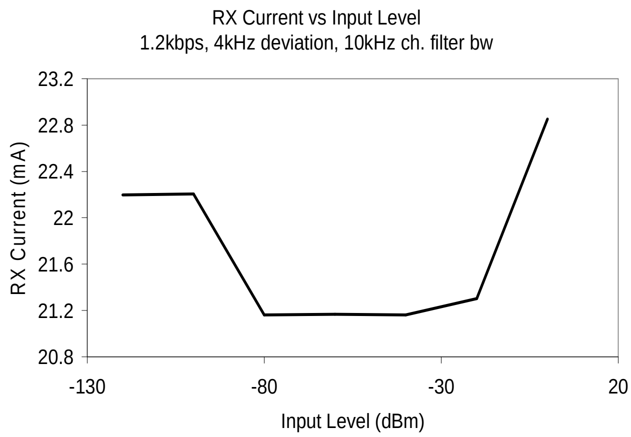
2 Typical Performance Curves

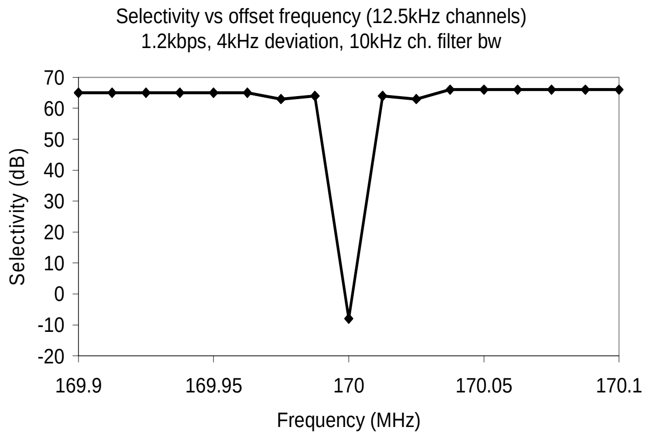
T_A = 25°C, VDD = 3.0 V if nothing else stated

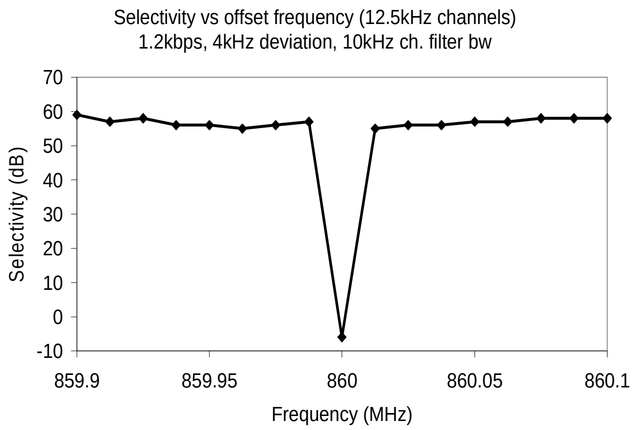


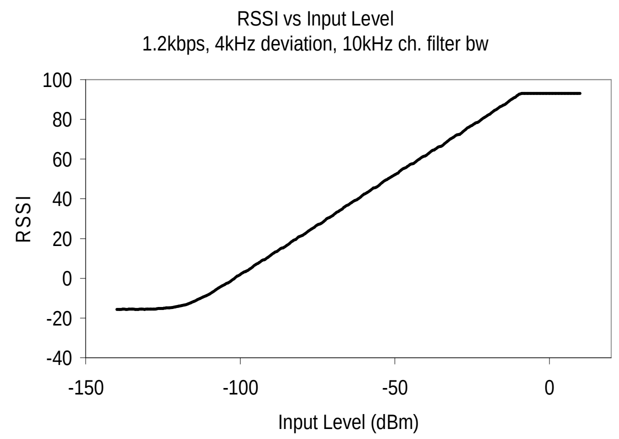


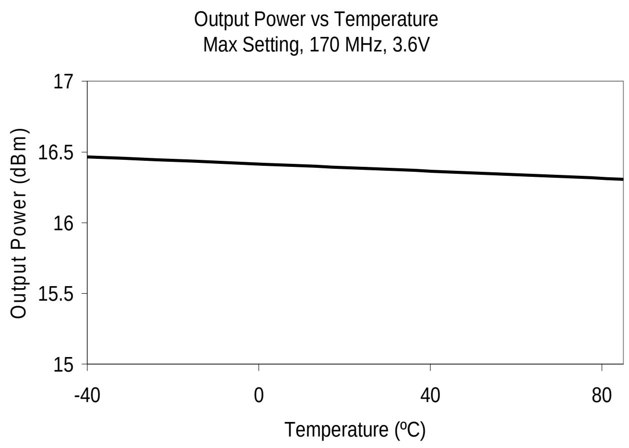


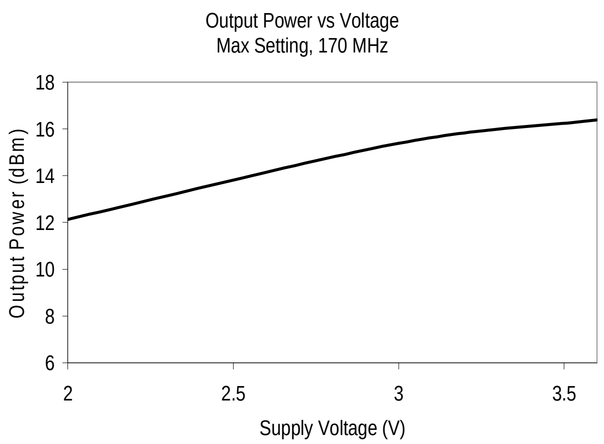


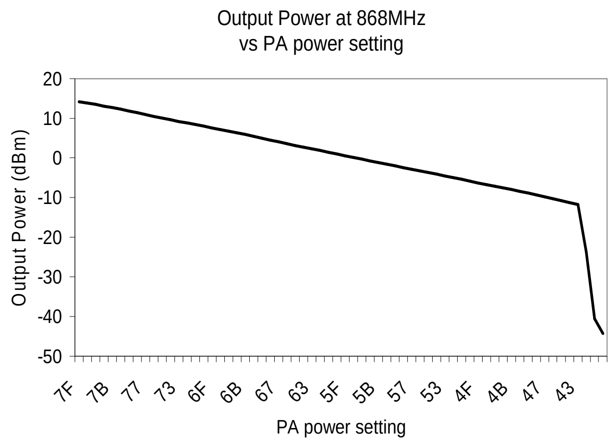


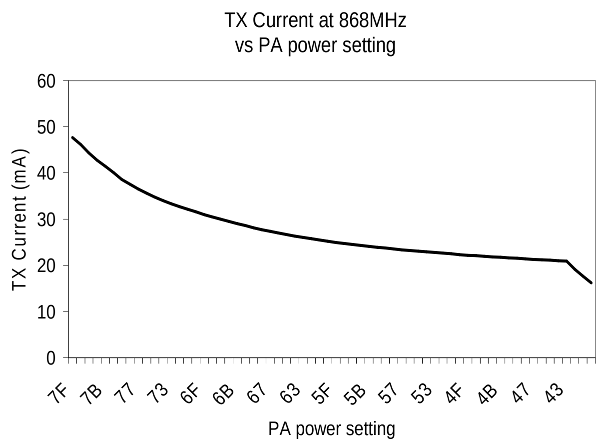


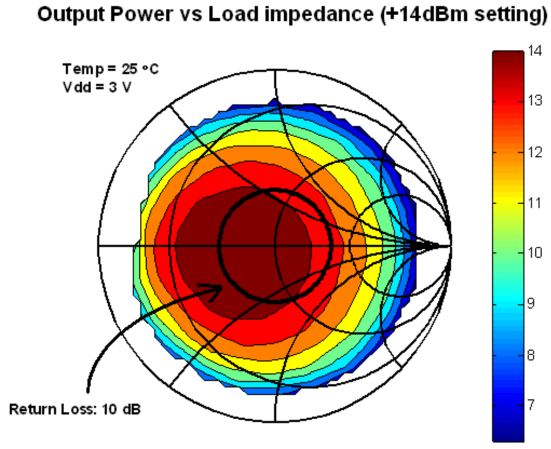

RSSI vs Input Level
1.2kbps, 4kHz deviation, 10kHz ch. filter bw
RSSI
Input Level (dBm)
100
80
60
40
20
0
-20
-40
-150
-100
-50
0


Output Power vs Temperature
Max Setting, 170 MHz, 3.6V
Output Power (dBm)
Temperature (ºC)
17
16.5
16
15.5
15
-40
0
40
80


Output Power vs Voltage
Max Setting, 170 MHz
Output Power (dBm)
Supply Voltage (V)
18
16
14
12
10
8
6
2
2.5
3
3.5

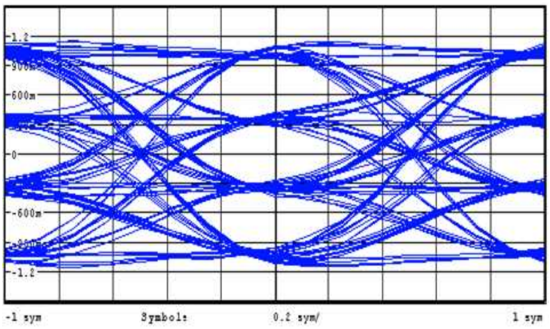

Output Power at 868MHz
vs PA power setting
Output Power (dBm)
PA power setting
20
10
0
-10
-20
-30
-40
-50
7F 7B 77 73 6F 6B 67 63 5F 5B 57 53 4F 4B 47 43


TX Current at 868MHz
vs PA power setting
TX Current (mA)
PA power setting
60
50
40
30
20
10
0
7F 7B 77 73 6F 6B 67 63 5F 5B 57 53 4F 4B 47 43


Output Power vs Load impedance (+14dBm setting)
Temp = 25 °C
Vdd = 3 V
Return Loss: 10 dB
14
13
12
11
10
9
8
7

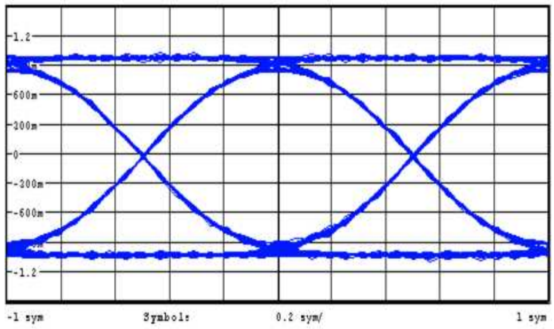
Eye Diagram

200 kbps, DEV=83 kHz (outer symbols), 4GFSK

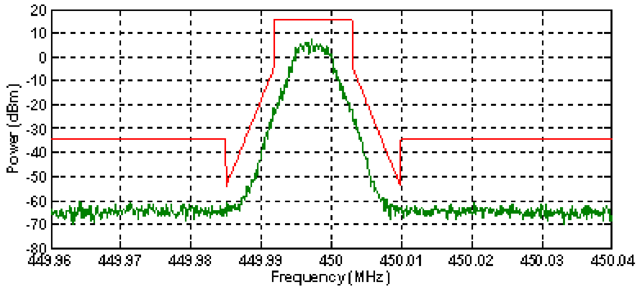


Eye Diagram

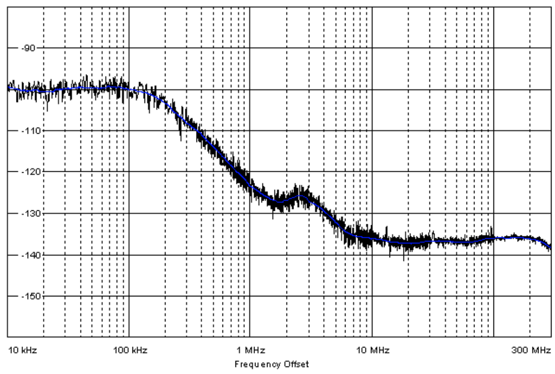
1.2 kbps 2-FSK, DEV=4 kHz



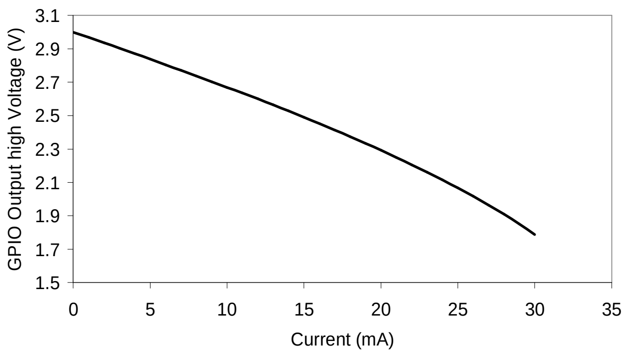
FCC Part 90 Mask D
9.6 kbps in 12.5 kHz Channel



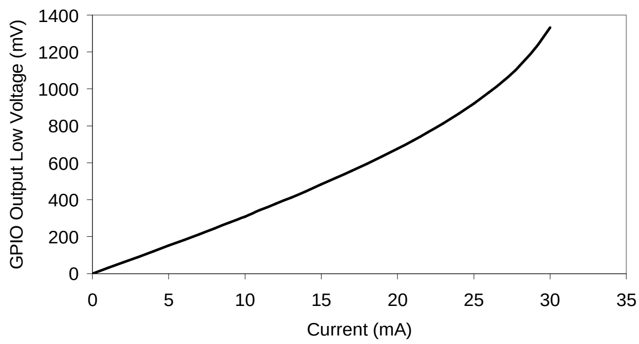
Phase Noise in 868 MHz band



GPIO Output High Voltage vs Current Being Sourced



GPIO Output Low Voltage vs Current Being Sinked



3 Pin Configuration

The **CC1120** pin-out is shown in the table below.

Pin #	Pin name	Type / direction	Description
1	VDD_GUARD	Power	2.0 - 3.6 V VDD
2	RESET_N	Digital Input	Asynchronous, active-low digital reset
3	GPIO3	Digital Input/Output	General purpose IO
4	GPIO2	Digital Input/Output	General purpose IO
5	DVDD	Power	2.0 - 3.6 VDD to internal digital regulator
6	DCPL	Power	Digital regulator output to external decoupling capacitor
7	SI	Digital Input	Serial data in
8	SCLK	Digital Input	Serial data clock
9	SO(GPIO1)	Digital Input/Output	Serial data out (General purpose IO)
10	GPIO0	Digital Input/Output	General purpose IO
11	CS_N	Digital Input	Active-low chip-select
12	DVDD	Power	2.0 - 3.6 V VDD
13	AVDD_IF	Power	2.0 - 3.6 V VDD
14	RBIAS	Analog	External high precision R
15	AVDD_RF	Power	2.0 - 3.6 V VDD
16	NC		Not connected
17	PA	Analog	Single-ended TX output
18	TRX_SW	Analog	TX/RX switch
19	LNA_P	Analog	Differential RX input
20	LNA_N	Analog	Differential RX input
21	DCPL_VCO	Power	Pin for external decoupling of VCO supply regulator
22	AVDD_SYNTH1	Power	2.0 - 3.6 V VDD
23	LPF0	Analog	External loopfilter components
24	LPF1	Analog	External loopfilter components
25	AVDD_PFD_CHP	Power	2.0 - 3.6 V VDD
26	DCPL_PFD_CHP	Power	Pin for external decoupling of PFD and CHP regulator
27	AVDD_SYNTH2	Power	2.0 - 3.6 V VDD
28	AVDD_XOSC	Power	2.0 - 3.6 V VDD
29	DCPL_XOSC	Power	Pin for external decoupling of XOSC supply regulator
30	XOSC_Q1	Analog	Crystal oscillator pin 1 (must be grounded if a TCXO or other external clock connected to EXT_XOSC is used)
31	XOSC_Q2	Analog	Crystal oscillator pin 2 (must be left floating if a TCXO or other external clock connected to EXT_XOSC is used)
32	EXT_XOSC	Digital Input	Pin for external XOSC input (must be grounded if a regular XOSC connected to XOSC_Q1 and XOSC_Q2 is used)
-	GND	Ground Pad	The ground pad must be connected to a solid ground plane

4 Block Diagram

A system block diagram of **CC1120** is shown Figure 4.1.

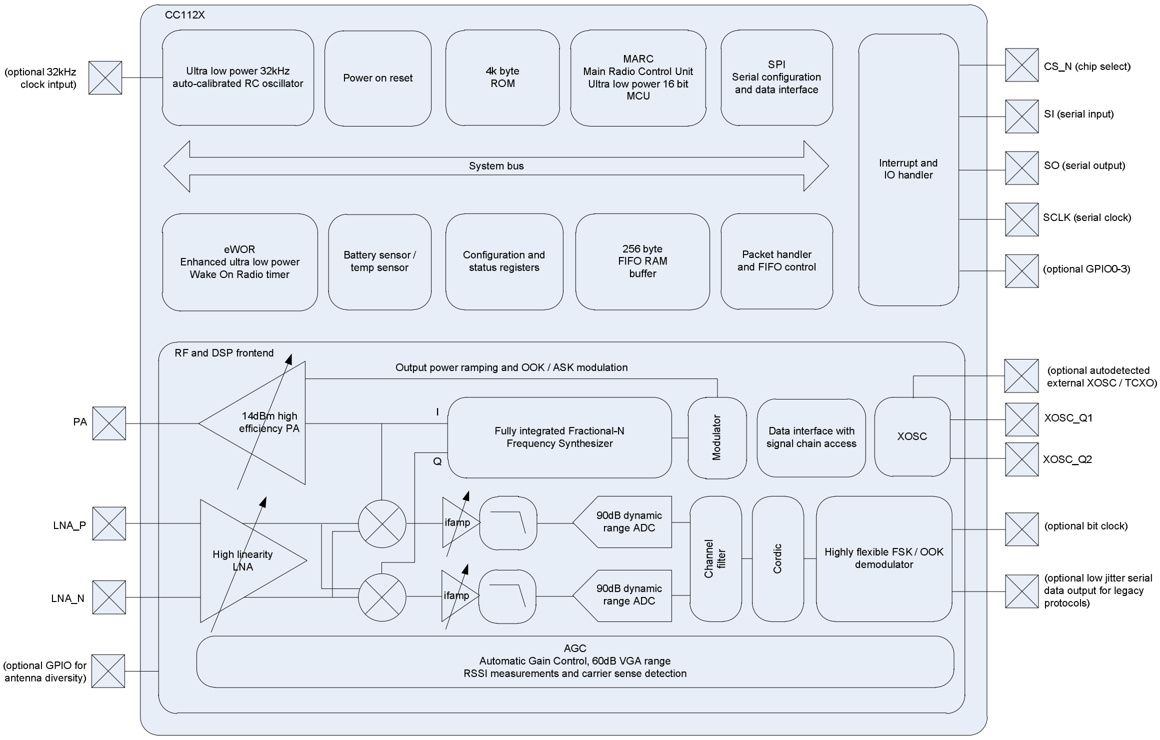


Figure 4.1 : System Block Diagram

4.1 Frequency Synthesizer

At the heart of **CC1120** there is a fully integrated, fractional-N, ultra high performance frequency synthesizer. The frequency synthesizer is designed for excellent phase noise performance, providing very high selectivity and blocking performance. The system is designed to comply with the most stringent regulatory spectral masks at maximum transmit power.

Either a crystal can be connected to XOSC_Q1 and XOSC_Q2, or a TCXO can be connected to the EXT_XOSC input. The oscillator generates the reference frequency for the synthesizer, as well as clocks for the ADC and the digital part. To reduce system cost, **CC1120** has high accuracy frequency estimation and compensation registers to measure and compensate for crystal inaccuracies, enabling the use of lower cost crystals. If a TCXO is used, the **CC1120** will automatically turn the TCXO on and off when needed to support low power modes and Wake-On-Radio operation.

4.2 Receiver

CC1120 features a highly flexible receiver. The received RF signal is amplified by the low-noise amplifier (LNA) and down-converted in quadrature (I and Q) to the intermediate frequency (IF). At IF, the I/Q signals are digitized by the high dynamic range ADCs.

An advanced Automatic Gain Control (AGC) unit adjusts the front end gain, and enables the **CC1120** to receive both strong and weak signals, even in the presence of strong interferers. High attenuation channel and data filtering enable reception with strong neighbor channel interferers. The I/Q signal is converted to a phase / magnitude signal to support both FSK and OOK modulation schemes.

A sophisticated pattern recognition algorithm locks onto the synchronization word without need for preamble settling bytes. Receiver settling time is therefore reduced to the settling time of the AGC, typically 4 bits. The advanced pattern recognition also greatly reduces the problem of false sync triggering on noise, further reducing power consumption and improving sensitivity and reliability. The pattern recognition logic can also be used as a high performance preamble detector to reliably detect a valid preamble in the channel.

A novel I/Q compensation algorithm removes any problem of I/Q mismatch and hence avoids time consuming and costly I/Q / image calibration steps in production or in the field.

4.3 Transmitter

The **CC1120** transmitter is based on direct synthesis of the RF frequency (in-loop modulation). To achieve effective spectrum usage, **CC1120** has extensive data filtering and shaping in TX to support high throughput data communication in narrowband channels. The modulator also controls power ramping to remove issues such as spectral splattering when driving external high power RF amplifiers.

4.4 Radio Control and User Interface

The **CC1120** digital control system is built around MARC (Main Radio Control) implemented using an internal high performance 16 bit ultra low power processor. MARC handles power modes, radio sequencing and protocol timing.

A 4-wire SPI serial interface is used for configuration and data buffer access. The digital baseband includes support for channel configuration, packet handling, and data buffering. The host MCU can stay in power down until a valid RF packet has been received, and then burst read the data, greatly reducing the power consumption and computing power required from the host MCU.

The **CC1120** radio control and user interface is based on the widely used **CC1101** transceiver to enable easy SW transition between the two platforms. The command strobes and the main radio states are the same for the two platforms.

For legacy formats **CC1120** also has support for two serial modes. In synchronous serial mode **CC1120** performs bit synchronization and provides the MCU with a bit clock with associated data. In transparent mode **CC1120** outputs the digital baseband signal using a digital interpolation filter to eliminate jitter introduced by digital filtering and demodulation.

4.5 Enhanced Wake-On-Radio (eWOR)

eWOR, using a flexible integrated sleep timer, enables automatic receiver polling with no intervention from the MCU. The **CC1120** will enter RX, listen and return to sleep if a valid RF packet is not received. The sleep interval and duty cycle can be configured to make a trade-off between network latency and power consumption. Incoming messages are time-stamped to simplify timer re-synchronization.

The eWOR timer runs off an ultra low power 32 kHz RC oscillator. To improve timing accuracy, the RC oscillator can be automatically calibrated to the RF crystal in configurable intervals.

4.6 Sniff Mode

The **CC1120** supports very quick start up times, and requires very few preamble bits. Sniff Mode uses this to dramatically reduce the current consumption while the receiver is waiting for data.

Since the **CC1120** is able to wake up and settle much faster than the length of most preambles, it is not required to be in RX continuously while waiting for a packet to arrive. Instead, the enhanced wake-on-radio feature can be used to put the device into sleep periodically. By setting an appropriate sleep time, the **CC1120** will be able to wake up and receive the packet when it arrives with no performance loss. This removes the need for accurate timing synchronization between transmitter and receiver, and allows the user to trade off current consumption between the transmitter and receiver.

4.7 Antenna Diversity

Antenna diversity can increase performance in a multi-path environment. An external antenna switch is required. The switch can be automatically controlled by **CC1120** using one of the GPIO pins (also support for differential output control signal typically used in RF switches).

If antenna diversity is enabled, the GPIO will alternate between states until a valid RF input signal is detected. An optional acknowledge packet can be transmitted without changing GPIO state.

An incoming RF signal can be validated by received signal strength, by using the automatic preamble detector, or a combination of the two. Using the preamble detector will make a more robust system and avoid the need to set a defined signal strength threshold, as this threshold will set the sensitivity limit of the system.

5 Typical Application Circuit

Very few external components are required for the operation of **CC1120**. A typical application circuit is shown below. Note that it does not show how the board layout should be done, which will greatly influence the RF performance of **CC1120**.

This section is meant as an introduction only. Note that decoupling capacitors for power pins are not shown in the figure below.

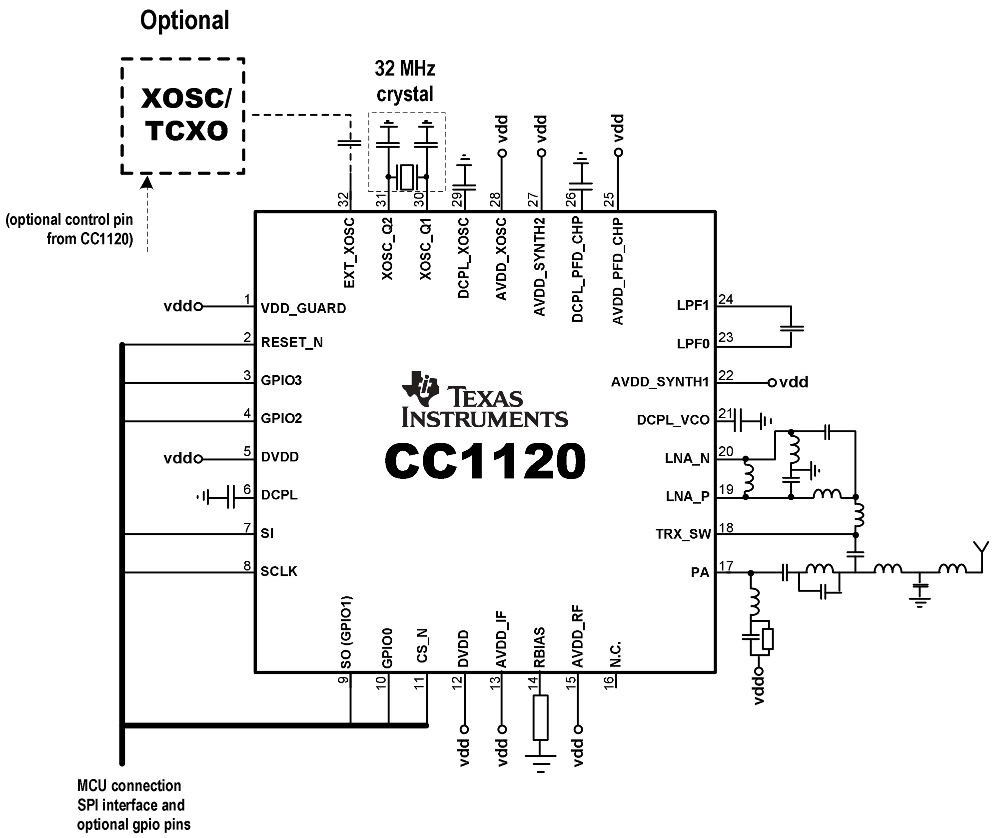


Figure 5.1 : Typical application circuit

6 History

Revision	Date	Description / Changes
SWRS112C	April 2012	Added ground pad on page 1 pin-out and pin description Added TCXO clock input voltage requirement Changed all pin names in pin description and figures to UPPERCASE Changed "PA OUT" to "PA" in block diagram Corrected deviation on 38.4kbps case from 50kHz to 20kHz Corrected error in EM list: CC1120EM_420_970 is corrected to CC1120EM_420_470 Added 274 - 320 MHz band and pointed to app note for more info (added mention of 315 MHz band on front page) Updated sniff mode current to 2 mA Added "WaveMatch:" in front of "Advanced digital signal processing ..." on front page Data rate offset tolerance: specified that 4 byte preamble only applies to 12% offset Removed solder reflow temperature and moisture sensitivity level under absolute max ratings Moved crystal ESR to ‘max’ column Added History section
SWRS112B	Sept. 2011	Initial release
SWRS112	Aug. 2011	Preliminary Data Sheet

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CC1120RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC1120	Samples
CC1120RHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC1120	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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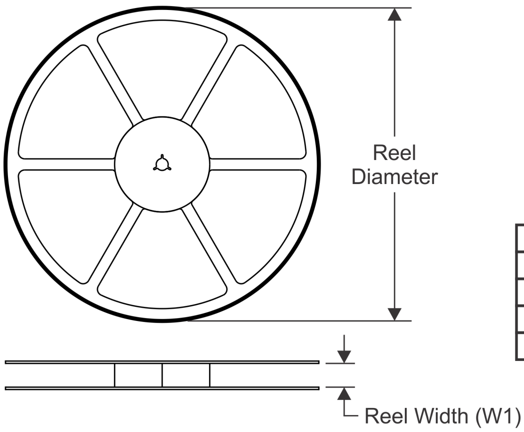
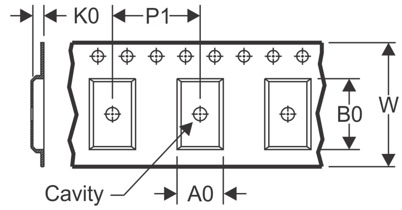
TAPE AND REEL INFORMATION

REEL DIMENSIONS

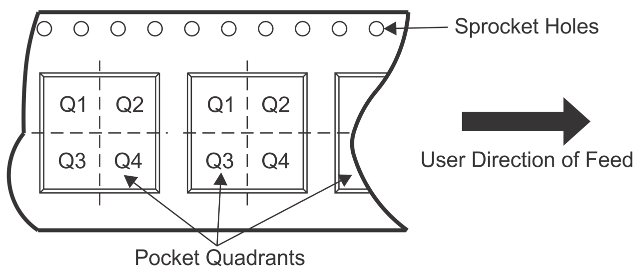


TAPE DIMENSIONS



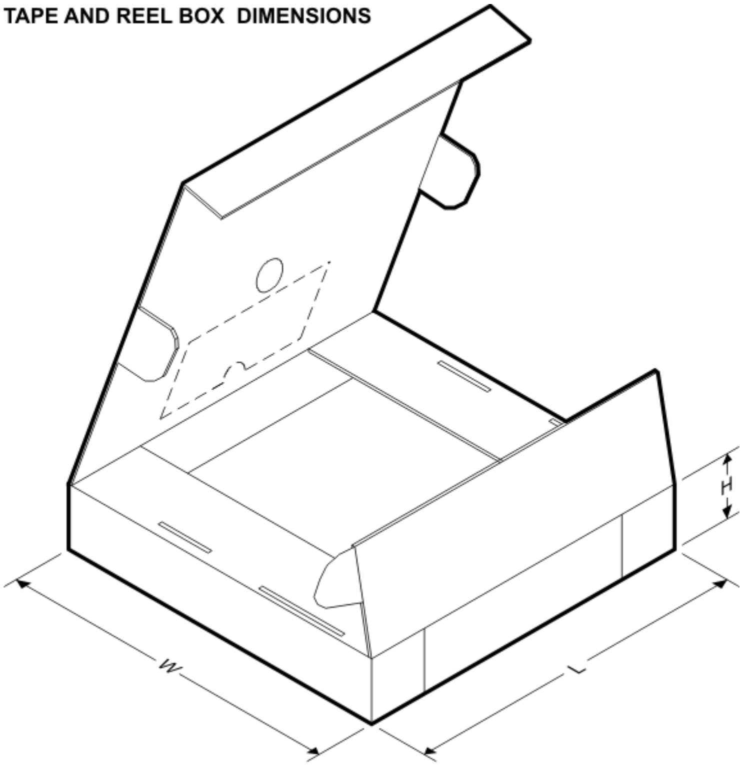
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

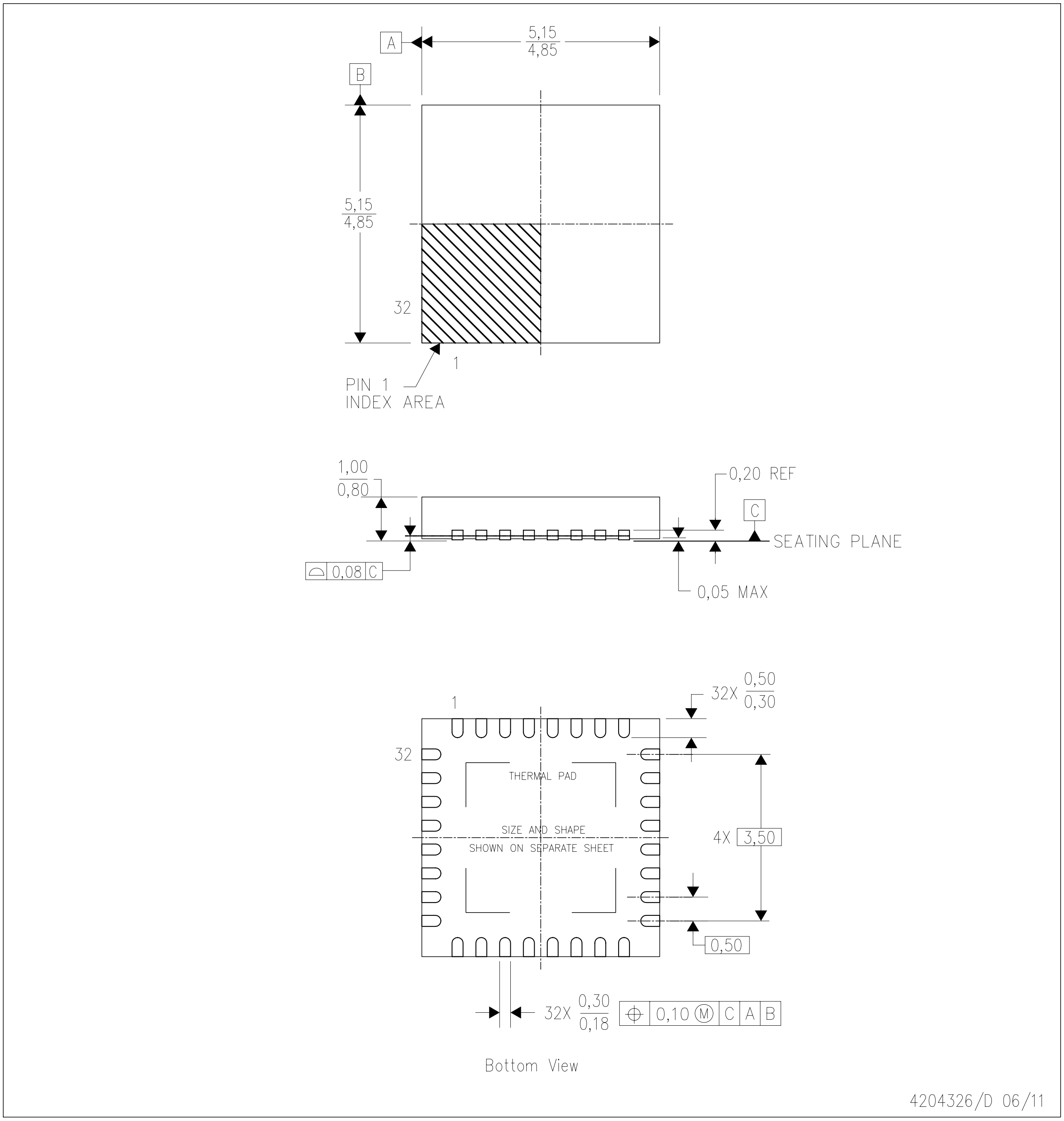
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC1120RHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
CC1120RHBT	QFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC1120RHBR	QFN	RHB	32	3000	338.1	338.1	20.6
CC1120RHBT	QFN	RHB	32	250	210.0	185.0	35.0

RHB (S-PVQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO-220.

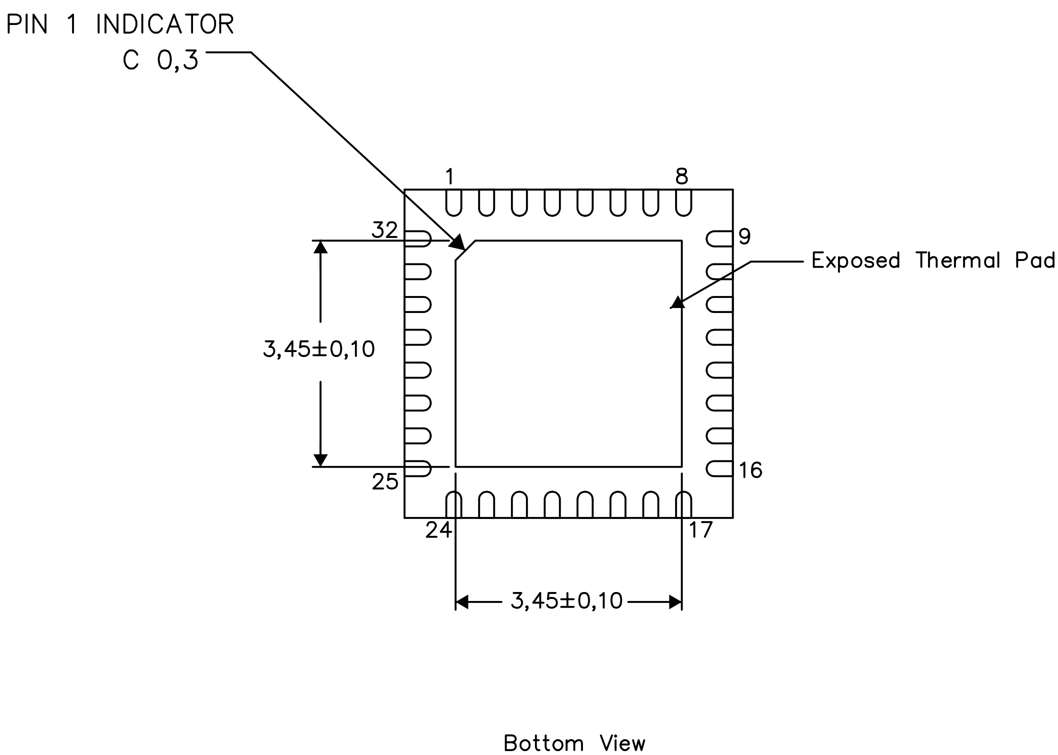
RHB (S-PVQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

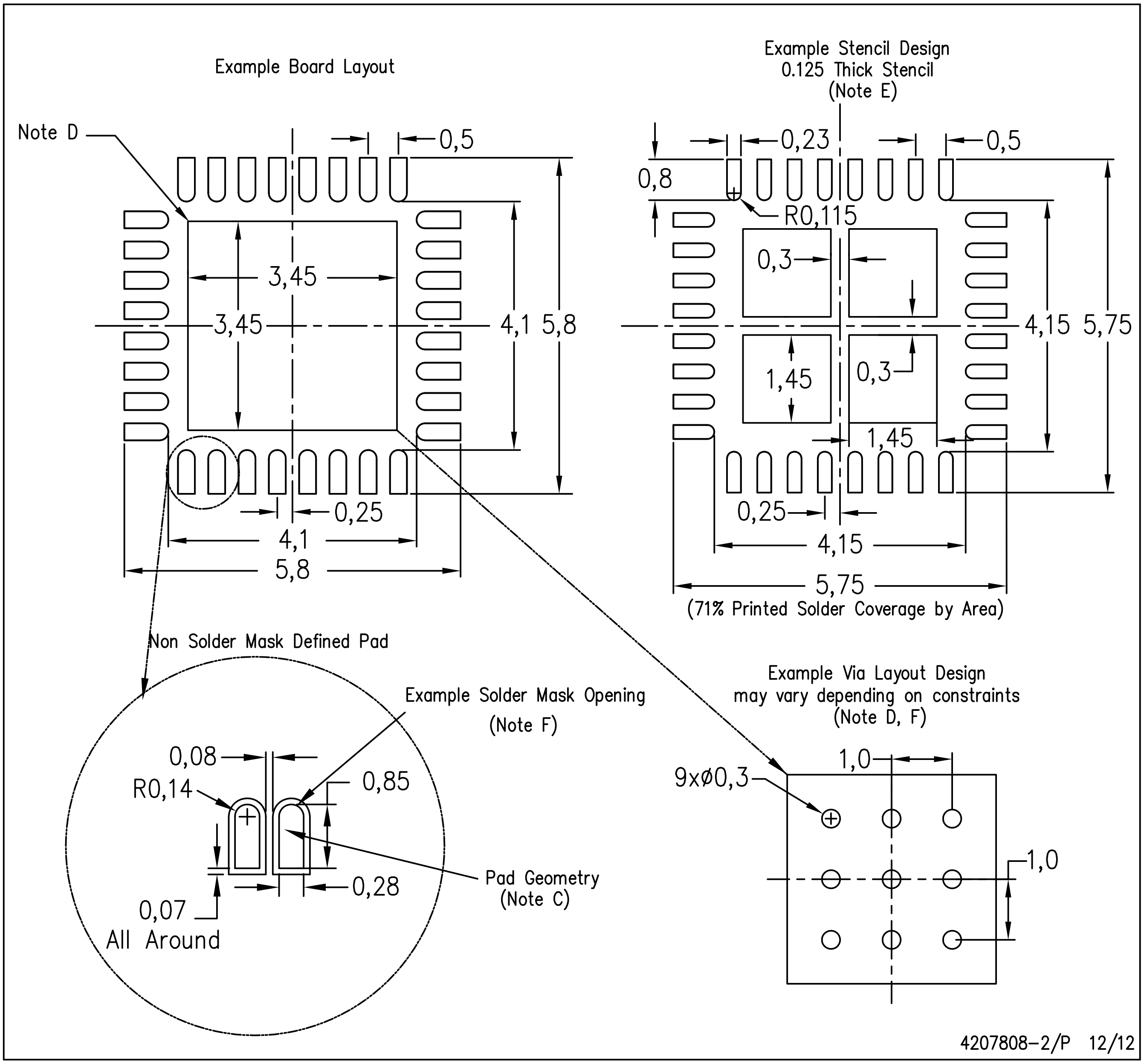


Exposed Thermal Pad Dimensions

4206356-2/X 12/12

NOTE: A. All linear dimensions are in millimeters

RHB (S-PVQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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