ILITEK
Enrich visual experience

ILI9320

a-Si TFT LCD Single Chip Driver
240RGBx320 Resolution and 262K color

Datasheet
Preliminary

Table of Contents

Figures

1. Introduction

ILI9320 is a 262,144-color one-chip SoC driver for a-TFT liquid crystal display with resolution of 240RGBx320 dots, comprising a 720-channel source driver, a 320-channel gate driver, 172,800 bytes RAM for graphic data of 240RGBx320 dots, and power supply circuit.

ILI9320 has four kinds of system interfaces which are i80-system MPU interface (8-/9-/16-/18-bit bus width), VSYNC interface (system interface + VSYNC, internal clock, DB[17:0]), serial data transfer interface (SPI) and RGB 6-/16-/18-bit interface (DOTCLK, VSYNC, HSYNC, ENABLE, DB[17:0]).

In RGB interface and VSYNC interface mode, the combined use of high-speed RAM write function and widow address function enables to display a moving picture at a position specified by a user and still pictures in other areas on the screen simultaneously, which makes it possible to transfer display the refresh data only to minimize data transfers and power consumption.

ILI9320 can operate with 1.65V I/O interface voltage, and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. The ILI9320 also supports a function to display in 8 colors and a sleep mode, allowing for precise power control by software and these features make the ILI9320 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, PDA and PMP where long battery life is a major concern.

2. Features

- ◆ Single chip solution for a liquid crystal QVGA TFT LCD display
- ◆ 240RGBx320-dot resolution capable with real 262,144 display color
- ◆ Support MVA (Multi-domain Vertical Alignment) wide view display
- ◆ Incorporate 720-channel source driver and 320-channel gate driver
- ◆ Internal 172,800 bytes graphic RAM
- ◆ High-speed RAM burst write function
- ◆ System interfaces
    - ➢ i80 system interface with 8-/ 9-/16-/18-bit bus width
    - ➢ Serial Peripheral Interface (SPI)
    - ➢ RGB interface with 6-/16-/18-bit bus width (VSYNC, HSYNC, DOTCLK, ENABLE, DB[17:0])
    - ➢ VSYNC interface (System interface + VSYNC)
- ◆ n-line liquid crystal AC drive: invert polarity at an interval of arbitrarily n lines (n: 1 ~ 64)
- ◆ Internal oscillator and hardware reset
- ◆ Resizing function (×1/2, ×1/4)
- ◆ Reversible source/gate driver shift direction
- ◆ Window address function to specify a rectangular area for internal GRAM access
- ◆ Bit operation function for facilitating graphics data processing
    - ➢ Bit-unit write data mask function

➢ Pixel-unit logical/conditional write function

◆ Abundant functions for color display control

➢ γ-correction function enabling display in 262,144 colors

➢ Line-unit vertical scrolling function

◆ Partial drive function, enabling partially driving an LCD panel at positions specified by user

◆ Incorporate step-up circuits for stepping up a liquid crystal drive voltage level up to 6 times (x6)

◆ Power saving functions

➢ 8-color mode

➢ standby mode

➢ sleep mode

◆ Low -power consumption architecture

➢ Low operating power supplies:

▪ IOVcc = 1.65V ~ 3.3 V (interface I/O)

▪ Vcc = 2.4V ~ 3.3 V (internal logic)

▪ Vci = 2.5V ~ 3.3 V (analog)

◆ LCD Voltage drive:

➢ Source/VCOM power supply voltage

▪ DDVDH - GND = 4.5V ~ 6.0V

▪ VCL – GND = -2.0V ~ -3.0V

▪ VCI – VCL $\leqq$ 6.0V

➢ Gate driver output voltage

▪ VGH - GND = 10V ~ 20V

▪ VGL – GND = -5V ~ -15V

▪ VGH – VGL $\leqq$ 32V

➢ VCOM driver output voltage

▪ VCOMH = 3.0V ~ (DDVDH-0.5)V

▪ VCOML = (VCL+0.5)V ~ 0V

▪ VCOMH-VCOML $\leqq$ 6.0V

◆ a-TFT LCD storage capacitor: Cst only

3. Block Diagram

4. Pin Descriptions

Pin Name	I/O	Type	Descriptions
			Input Interface
IM3, IM2, IM1, IM0/ID	I	IOVcc	Select the MPU system interface mode

IM3	IM2	IM1	IM0	MPU-Interface Mode	DB Pin in use
0	0	0	0	Setting invalid	
0	0	0	1	Setting invalid	
0	**0**	**1**	**0**	**i80-system 16-bit interface**	**DB[17:10], DB[8:1]**
0	**0**	**1**	**1**	**i80-system 8-bit interface**	**DB[17:10]**
0	**1**	**0**	**ID**	**Serial Peripheral Interface (SPI)**	**SDI, SDO**
0	1	1	*	Setting invalid	
1	0	0	0	Setting invalid	
1	0	0	1	Setting invalid	
1	**0**	**1**	**0**	**i80-system 18-bit interface**	**DB[17:0]**
1	**0**	**1**	**1**	**i80-system 9-bit interface**	**DB[17:9]**
1	1	*	*	Setting invalid	

When the serial peripheral interface is selected, IM0 pin is used for the device code ID setting. |

nCS	I	MPU IOVcc	A chip select signal.
			    Low: the ILI9320 is selected and accessible
			    High: the ILI9320 is not selected and not accessible
			Fix to the DGND level when not in use.

RS	I	MPU IOVcc	A register select signal.
			    Low: select an index or status register
			    High: select a control register
			Fix to DGND level when not in use.

nWR/SCL	I	MPU IOVcc	A write strobe signal and enables an operation to write data when the signal is low. *Fix to IOVCC level when not in use.* SPI Mode: Synchronizing clock signal in SPI mode.
nRD	I	MPU IOVcc	A read strobe signal and enables an operation to read out data when the signal is low. *Fix to IOVCC level when not in use.*
nRESET	I	MPU IOVcc	A reset pin. Initializes the ILI9320 with a low input. Be sure to execute a power-on reset after supplying power.
SDI	I	MPU IOVcc	SPI interface input pin. The data is latched on the rising edge of the SCL signal. *Fix to DGND level when not in use.*
SDO	O	MPU IOVcc	SPI interface output pin. The data is outputted on the falling edge of the SCL signal. *Let SDO as open when not in use.*

DB[17:0]	I/O	MPU IOVcc	An 18-bit parallel bi-directional data bus for MPU system interface mode
			    8-bit I/F: DB[17:10] is used.
			    9-bit I/F: DB[17:9] is used.
			    16-bit I/F: DB[17:10] and DB[8:1] is used.
			    18-bit I/F: DB[17:0] is used.
			
			18-bit parallel bi-directional data bus for RGB interface operation
			    6-bit RGB I/F: DB[17:12] are used.

Pin Name	I/O	Type	Descriptions
			16-bit RGB I/F: DB[17:13] and DB[11:1] are used. 18-bit RGB I/F: DB[17:0] are used. ***Unused pins must be fixed DGND level.***

ENABLE	I	MPU
		IOVcc
			Data ENEABLE signal for RGB interface operation.
			   Low: Select (access enabled)
			   High: Not select (access inhibited)
			The EPL bit inverts the polarity of the ENABLE signal.
			
			Fix to DGND level when not in use.

DOTCLK	I	MPU
		IOVcc
			Dot clock signal for RGB interface operation.
			   DPL = "0": Input data on the rising edge of DOTCLK
			   DPL = "1": Input data on the falling edge of DOTCLK
			Fix to DGND level when not in use.

VSYNC	I	MPU
		IOVcc
			Frame synchronizing signal for RGB interface operation.
			   VSPL = "0": Active low.
			   VSPL = "1": Active high.
			Fix to DGND level when not in use.

HSYNC	I	MPU
		IOVcc
			Line synchronizing signal for RGB interface operation.
			   HSPL = "0": Active low.
			   HSPL = "1": Active high.
			Fix to DGND level when not in use.

FMARK	O	MPU IOVcc	Output a frame head pulse signal. The FMARK signal is used when writing RAM data in synchronization with frame. ***Leave the pin open when not in use.***
OSC1 OSC2	I O	Oscillation resistor	Connect an external resistor for generating internal clock by internal R-C oscillation, or an external clock signal is supplied through OSC1.
LCD Driving signals			

S720~S1	O	LCD	Source output voltage signals applied to liquid crystal.
			To change the shift direction of signal outputs, use the SS bit.
			   SS = "0", the data in the RAM address "h00000" is output from S1.
			   SS = "1", the data in the RAM address "h00000" is output from S720.
			S1, S4, S7, … display red (R), S2, S5, S8, ... display green (G), and S3, S6, S9, ... display blue (B) (SS = 0).

G320~G1	O	LCD	Gate line output signals.
			   VGH: the level selecting gate lines
			   VGL: the level not selecting gate lines

VCOM	O	TFT common electrode	A supply voltage to the common electrode of TFT panel. VCOM is AC voltage alternating signal between the VCOMH and VCOML levels.
VCOMH	O	Stabilizing capacitor	The high level of VCOM AC voltage. Connect to a stabilizing capacitor.
VCOML	O	Stabilizing capacitor	The low level of VCOM AC voltage. Adjust the VCOML level with the VDV bits. Connect to a stabilizing capacitor.
VCOMR	I	Variable resistor or open	A reference level to generate the VCOMH level either with an externally connected variable resistor or by setting the register of the ILI9320. When using a variable resistor, halt the internal VCOMH adjusting circuit by setting the register and place the resister between VREG1OUT and AGND. ***When generating the VCOMH level by setting the register, leave this pin open.***
VGS	I	AGND or external resistor	Reference level for the grayscale voltage generating circuit. The VGS level can be changed by connecting to an external resistor.
Charge-pump and Regulator Circuit			

Pin Name	I/O	Type	Descriptions
Vci	I	Power supply	A supply voltage to the analog circuit. Connect to an external power supply of 2.5 ~ 3.3V.
AGND	I	Power supply	AGND for the analog side: AGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
VciLVL	I	Power supply	VciLVL must be at the same voltage level as Vci. VciLVL=2.5V ~ 3.3V. Connect to the external power supply. In COG case, connect the VciLVL with Vci on the FPC to prevent noise.
VciOUT	O	Stabilizing capacitor Vci1	An internal reference voltage generated between Vci and AGND. The amplitude between Vci and DGND is determined by the VC[2:0] bits.
Vci1	I	Stabilizing capacitor Vci1	An internal reference voltage for the step-up circuit1. The amplitude between Vci and DGND is determined by the VC[2:0] bits. Make sure to set the Vci1 voltage so that the VLOUT1, VLOUT2 and VLOUT3 voltages are set within the respective specification.
VLOUT1	O	Stabilizing capacitor, DDVDH	Output voltage from the step-up circuit 1, which is generated from Vci1. The step-up factor is set by "BT" bits. VLOUT1= 4.5 ~ 6.0V Place a stabilizing capacitor between AGND.
DDVDH	O	VLOUT1	Power supply for the source driver and Vcom drive. Connect to VLOUT1 and DDVDH = 4.5 ~ 6.0V
VLOUT2	O	Stabilizing capacitor, VGH	Output voltage from the step-up circuit 2, which is generated from Vci1 and DDVDH. The step-up factor is set by "BT" bits. VLOUT2= max.15V
VGH	I	VLOUT2	Power supply for the gate driver, connect to VLOUT2.
VLOUT3	O	Stabilizing capacitor, VGL	Output voltage from the step-up circuit 2, which is generated from Vci1 and DDVDH. The step-up factor is set by "BT" bits. VLOUT3= max. -12.5V Place a stabilizing capacitor between AGND and a shottkey diode between Vci.
VGL	I	VLOUT3	Power supply for the gate driver, connect to VLOUT3.
VCL	O	Stabilizing capacitor, VCL	VcomL driver power supply. VCLC = 0 ~ –3.3V. Place a stabilizing capacitor between AGND
C11+, C11- C12+, C12-	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 1.
C13+, C13- C21+, C21- C22+, C22- C23+, C23-	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 2.
VREG1OUT	I/O	Stabilizing capacitor or power supply	Output voltage generated from the reference voltage. The voltage level is set with the VRH bits. VREG1OUT is (1) a source driver grayscale reference voltage, (2) VcomH level reference voltage, and (3) Vcom amplitude reference voltage. Connect to a stabilizing capacitor. VREG1OUT = 3.0 ~ (DDVDH – 0.5)V.
Power Pads			
Vcc	I	Power supply	A supply voltage to the internal logic: Vcc = 2.4~3.3V
IOVcc	I	Power supply	A supply voltage to the interface pins: IM[3:0], nRESET, nCS, nWR, nRD, RS, DB[17:0], VSYNC, HSYNC, DOTCLK, ENABLE, SCL, SDI, SDO. IOVcc = 1.65 ~ 3.3V and Vcc $\geq$ IOVcc. In case of COG, connect to Vcc on the FPC if IOVcc=Vcc, to prevent noise.

Pin Name	I/O	Type	Descriptions
VDD	O	Power	Digital core power pad. Connect them with the 1uF capacitor.
GND	I	Power supply	DGND for the logic side: DGND = 0V.
IOGND	I	Power supply	IOGND for the interface pins. IOGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
Test Pads			
V0T, V31T	-	Open	Dummy pads. Connect to IOVcc, GND or leave these pins as open.
VTEST	-	Open	Dummy pad. Connect to IOVcc, GND or leave this pin as open.
VREFC	-	Open	Dummy pad. Connect to IOVcc, GND or leave this pin as open.
VREF	-	Open	Dummy pad. Connect to IOVcc, GND or leave this pin as open.
VDDTEST	-	Open	Dummy pad. Connect to IOVcc, GND or leave this pin as open.
VREFD	-	Open	Dummy pad. Connect to IOVcc, GND or leave this pin as open.
VMON	-	Open	Dummy pad. Connect to IOVcc, GND or leave this pin as open.
TESTA5	-	Open	Dummy pad. Connect to IOVcc, GND or leave this pin as open.
IOVCCDUM1~2	O	Power	Output the IOVcc voltage level. These pins are internally shorted to IOVCC
VCCDUM1	-	Power	Dummy pin. Connect to VCC or leave this pin as open.
IOGNDDUM1~3	O	Power	Output the GND voltage level. These pins are internally shorted to GND. When adjacent pins are needed to pull low, tie these pins to IOGNDDUM1~3.
OSC1DUM1~4	-	Open	Dummy pads. Connect to GND or leave these pins as open.
OSC2DUM1~2	-	Open	Dummy pads. Connect to GND or leave these pins as open.
AGNDDUM1	-	Power	Dummy pad. Leave this pin as open.
AGNDDUM2~4	O	Power	Output the GND voltage level. These pins are internally shorted to GND.
DUMMYR1~ 10	-	-	Dummy pads. Leave these pins as open.
VGLDMY1~4	O	Open	Dummy pads. Connect to IOVcc, GND or leave these pins as open.
TESTO1~38	O	Open	Test pins. Leave them open.
TEST1, 2, 5	I	IOGND	**Test pins (internal pull low).** **Connect to GND.**
TEST3	I	Open	Dummy pin. Connect to IOVcc or leave these pins as open.
TEST4	I	Open	Dummy pin. Connect to IOVcc or leave these pins as open.
TSC	I	Open	Dummy pin. Connect to GND or leave these pins as open.
TS0~8	I	Open	Test pins (internal pull low). Leave them open.
VPP1	-	Open	Test pins. Must let these pads as open.
VPP2	-	Open	Test pins. Must let these pads as open.
VPP3	-	-	Test pins. Must let these pads as open or connect to GND.

Liquid crystal power supply specifications Table 1

No.	Item		Description
1	TFT Source Driver		720 pins (240 x RGB)
2	TFT Gate Driver		320 pins
3	TFT Display's Capacitor Structure		Cst structure only (Common VCOM)
4	Liquid Crystal Drive Output	S1 ~ S720	V0 ~ V63 grayscales
		G1 ~ G320	VGH - VGL
		VCOM	VCOMH - VCOML: Amplitude = electronic volumes VCOMH=VCOMR: Adjusted with an external resistor
5	Input Voltage	IOVcc	1.65 ~ 3.30V
		Vcc	2.40 ~ 3.30V

		Vci	2.50 ~ 3.30V
6	Liquid Crystal Drive Voltages	DDVDH	4.5V ~ 6.0V
		VGH	10V ~ 20V
		VGL	-5V ~ -15V
		VCL	-1.9V ~ -3.0V
		VGH - VGL	Max. 32V
		Vci - VCL	Max. 6.0V
7	Internal Step-up Circuits	VLOUT1 (DDVDH)	Vci1 x2, x3
		VLOUT2 (VGH)	Vci1 x6, x7, x8
		VLOUT3 (VGL)	Vci1 x-3, x-4, x-5
		VCL	Vci1 x-1

5. Pad Arrangement and Coordination

Chip Size: 21680um x 1250um

Chip thickness : 400um (typ.) or 250um (customer order)

Pad Location: Pad Center.

Coordinate Origin: Chip center

Au bump height: 15um (typ.)

Au Bump Size:

1. 21um x 100um (No. 299 ~ 1354)
   Gate: G1 ~ G320
   Source: S1 ~ S720

2. 50um x 80um (No. 1 ~ 298)
   Input Pads
   Pad 1 to 298.

Alignment Marks

Alignment Mark: 1-a, 1-b.

Face Up
(Bump View)

Bump View
ILI9320
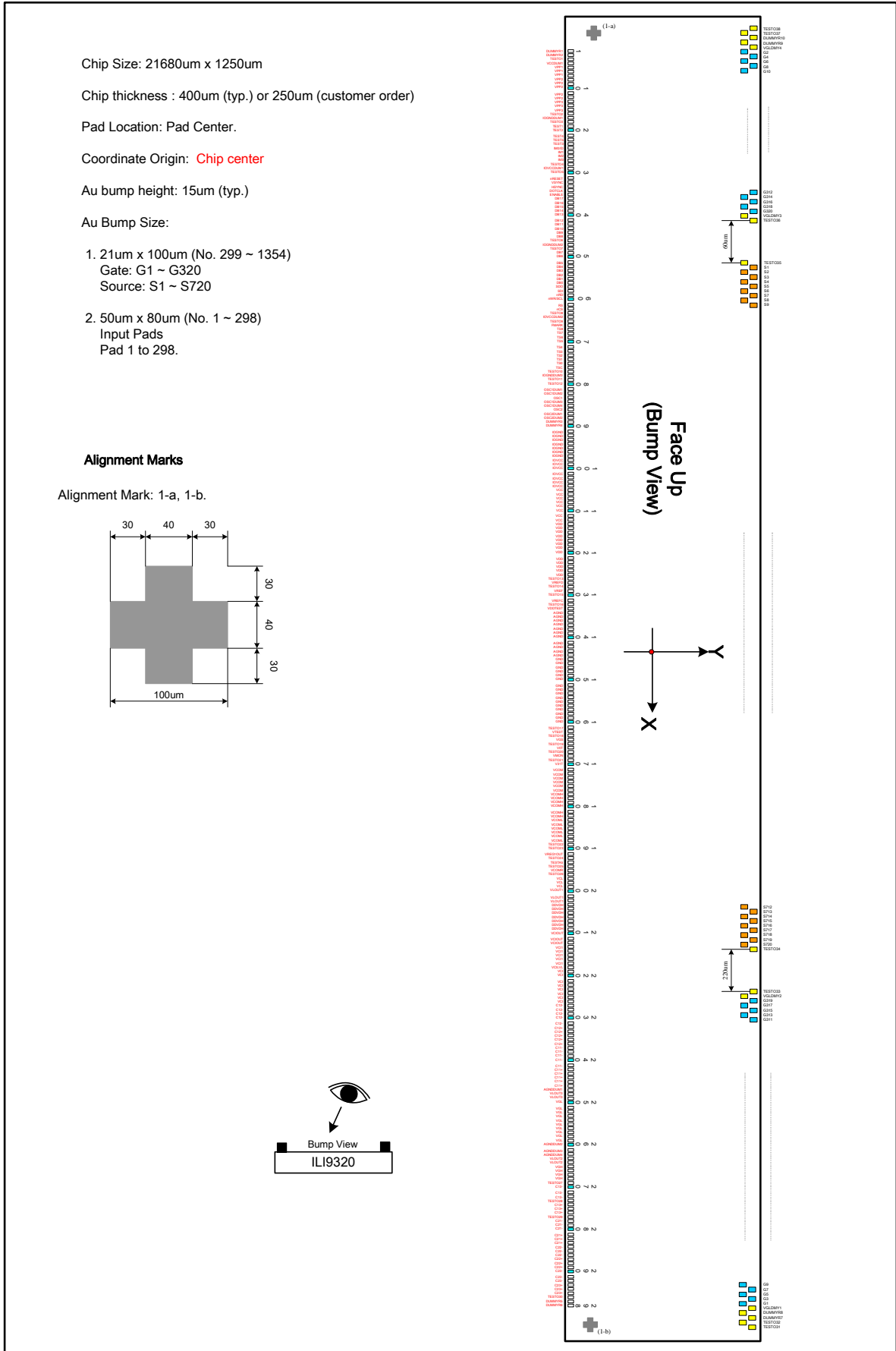
No.	Name	X	Y
1	DUMMYR1	-10395.0	-517.5
2	DUMMYR2	-10325.0	-517.5
3	TESTO1	-10255.0	-517.5
4	VCCDUM1	-10185.0	-517.5
5	VPP1	-10115.0	-517.5
6	VPP1	-10045.0	-517.5
7	VPP1	-9975.0	-517.5
8	VPP2	-9905.0	-517.5
9	VPP2	-9835.0	-517.5
10	VPP2	-9765.0	-517.5
11	VPP2	-9695.0	-517.5
12	VPP2	-9625.0	-517.5
13	VPP3	-9555.0	-517.5
14	VPP3	-9485.0	-517.5
15	VPP3	-9415.0	-517.5
16	TESTO2	-9345.0	-517.5
17	IOGNDDUM1	-9275.0	-517.5
18	TESTO3	-9205.0	-517.5
19	TEST1	-9135.0	-517.5
20	TEST2	-9065.0	-517.5
21	TEST4	-8995.0	-517.5
22	TEST5	-8925.0	-517.5
23	TEST3	-8855.0	-517.5
24	IM0/ID	-8785.0	-517.5
25	IM1	-8715.0	-517.5
26	IM2	-8645.0	-517.5
27	IM3	-8575.0	-517.5
28	TESTO4	-8505.0	-517.5
29	IOVCCDUM1	-8435.0	-517.5
30	TESTO5	-8365.0	-517.5
31	RESET*	-8295.0	-517.5
32	VSYNC	-8225.0	-517.5
33	HSYNC	-8155.0	-517.5
34	DOTCLK	-8085.0	-517.5
35	ENABLE	-8015.0	-517.5
36	DB17	-7945.0	-517.5
37	DB16	-7875.0	-517.5
38	DB15	-7805.0	-517.5
39	DB14	-7735.0	-517.5
40	DB13	-7665.0	-517.5
41	DB12	-7595.0	-517.5
42	DB11	-7525.0	-517.5
43	DB10	-7455.0	-517.5
44	DB9	-7385.0	-517.5
45	DB8	-7315.0	-517.5
46	TESTO6	-7245.0	-517.5
47	IOGNDDUM2	-7175.0	-517.5
48	TESTO7	-7105.0	-517.5
49	DB7	-7035.0	-517.5
50	DB6	-6965.0	-517.5
51	DB5	-6895.0	-517.5
52	DB4	-6825.0	-517.5
53	DB3	-6755.0	-517.5
54	DB2	-6685.0	-517.5
55	DB1	-6615.0	-517.5
56	DB0	-6545.0	-517.5
57	SDO	-6475.0	-517.5
58	SDI	-6405.0	-517.5
59	RD*	-6335.0	-517.5
60	WR*/SCL	-6265.0	-517.5

No.	Name	X	Y
61	RS	-6195.0	-517.5
62	CS*	-6125.0	-517.5
63	TESTO8	-6055.0	-517.5
64	IOVCCDUM2	-5985.0	-517.5
65	TESTO9	-5915.0	-517.5
66	FMARK	-5845.0	-517.5
67	TS8	-5775.0	-517.5
68	TS7	-5705.0	-517.5
69	TS6	-5635.0	-517.5
70	TS5	-5565.0	-517.5
71	TS4	-5495.0	-517.5
72	TS3	-5425.0	-517.5
73	TS2	-5355.0	-517.5
74	TS1	-5285.0	-517.5
75	TS0	-5215.0	-517.5
76	TSC	-5145.0	-517.5
77	TESTO10	-5075.0	-517.5
78	IOGNDDUM3	-5005.0	-517.5
79	TESTO11	-4935.0	-517.5
80	TESTO12	-4865.0	-517.5
81	OSC1DUM1	-4795.0	-517.5
82	OSC1DUM2	-4725.0	-517.5
83	OSC1	-4655.0	-517.5
84	OSC1DUM3	-4585.0	-517.5
85	OSC1DUM4	-4515.0	-517.5
86	OSC2	-4445.0	-517.5
87	OSC2DUM1	-4375.0	-517.5
88	OSC2DUM2	-4305.0	-517.5
89	DUMMYR3	-4235.0	-517.5
90	DUMMYR4	-4165.0	-517.5
91	IOGND	-4095.0	-517.5
92	IOGND	-4025.0	-517.5
93	IOGND	-3955.0	-517.5
94	IOGND	-3885.0	-517.5
95	IOGND	-3815.0	-517.5
96	IOGND	-3745.0	-517.5
97	IOGND	-3675.0	-517.5
98	IOVCC	-3605.0	-517.5
99	IOVCC	-3535.0	-517.5
100	IOVCC	-3465.0	-517.5
101	IOVCC	-3395.0	-517.5
102	IOVCC	-3325.0	-517.5
103	IOVCC	-3255.0	-517.5
104	IOVCC	-3185.0	-517.5
105	VCC	-3115.0	-517.5
106	VCC	-3045.0	-517.5
107	VCC	-2975.0	-517.5
108	VCC	-2905.0	-517.5
109	VCC	-2835.0	-517.5
110	VCC	-2765.0	-517.5
111	VCC	-2695.0	-517.5
112	VCC	-2625.0	-517.5
113	VDD	-2555.0	-517.5
114	VDD	-2485.0	-517.5
115	VDD	-2415.0	-517.5
116	VDD	-2345.0	-517.5
117	VDD	-2275.0	-517.5
118	VDD	-2205.0	-517.5
119	VDD	-2135.0	-517.5
120	VDD	-2065.0	-517.5

No.	Name	X	Y
121	VDD	-1995.0	-517.5
122	VDD	-1925.0	-517.5
123	VDD	-1855.0	-517.5
124	VDD	-1785.0	-517.5
125	VDD	-1715.0	-517.5
126	TESTO13	-1645.0	-517.5
127	VREFD	-1575.0	-517.5
128	TESTO14	-1505.0	-517.5
129	VREF	-1435.0	-517.5
130	TESTO15	-1365.0	-517.5
131	VREFC	-1295.0	-517.5
132	TESTO16	-1225.0	-517.5
133	VDDTEST	-1155.0	-517.5
134	AGND	-1085.0	-517.5
135	AGND	-1015.0	-517.5
136	AGND	-945.0	-517.5
137	AGND	-875.0	-517.5
138	AGND	-805.0	-517.5
139	AGND	-735.0	-517.5
140	AGND	-665.0	-517.5
141	AGND	-595.0	-517.5
142	AGND	-525.0	-517.5
143	AGND	-455.0	-517.5
144	AGND	-385.0	-517.5
145	GND	-315.0	-517.5
146	GND	-245.0	-517.5
147	GND	-175.0	-517.5
148	GND	-105.0	-517.5
149	GND	-35.0	-517.5
150	GND	35.0	-517.5
151	GND	105.0	-517.5
152	GND	175.0	-517.5
153	GND	245.0	-517.5
154	GND	315.0	-517.5
155	GND	385.0	-517.5
156	GND	455.0	-517.5
157	GND	525.0	-517.5
158	GND	595.0	-517.5
159	GND	665.0	-517.5
160	GND	735.0	-517.5
161	TESTO17	805.0	-517.5
162	VTEST	875.0	-517.5
163	TESTO18	945.0	-517.5
164	VGS	1015.0	-517.5
165	TESTO19	1085.0	-517.5
166	V0T	1155.0	-517.5
167	TESTO20	1225.0	-517.5
168	VMON	1295.0	-517.5
169	TESTO21	1365.0	-517.5
170	V31T	1435.0	-517.5
171	VCOM	1505.0	-517.5
172	VCOM	1575.0	-517.5
173	VCOM	1645.0	-517.5
174	VCOM	1715.0	-517.5
175	VCOM	1785.0	-517.5
176	VCOM	1855.0	-517.5
177	VCOMH	1925.0	-517.5
178	VCOMH	1995.0	-517.5
179	VCOMH	2065.0	-517.5
180	VCOMH	2135.0	-517.5

No.	Name	X	Y
181	VCOMH	2205.0	-517.5
182	VCOMH	2275.0	-517.5
183	VCOML	2345.0	-517.5
184	VCOML	2415.0	-517.5
185	VCOML	2485.0	-517.5
186	VCOML	2555.0	-517.5
187	VCOML	2625.0	-517.5
188	VCOML	2695.0	-517.5
189	TESTO22	2765.0	-517.5
190	TESTO23	2835.0	-517.5
191	VREG1OUT	2905.0	-517.5
192	TESTO24	2975.0	-517.5
193	TESTA5	3045.0	-517.5
194	TESTO25	3115.0	-517.5
195	VCOMR	3185.0	-517.5
196	TESTO26	3255.0	-517.5
197	VCL	3325.0	-517.5
198	VCL	3395.0	-517.5
199	VCL	3465.0	-517.5
200	VLOUT1	3535.0	-517.5
201	VLOUT1	3605.0	-517.5
202	VLOUT1	3675.0	-517.5
203	DDVDH	3745.0	-517.5
204	DDVDH	3815.0	-517.5
205	DDVDH	3885.0	-517.5
206	DDVDH	3955.0	-517.5
207	DDVDH	4025.0	-517.5
208	DDVDH	4095.0	-517.5
209	DDVDH	4165.0	-517.5
210	VCIOUT	4235.0	-517.5
211	VCIOUT	4305.0	-517.5
212	VCIOUT	4375.0	-517.5
213	VCI1	4445.0	-517.5
214	VCI1	4515.0	-517.5
215	VCI1	4585.0	-517.5
216	VCI1	4655.0	-517.5
217	VCI1	4725.0	-517.5
218	VCILVL	4795.0	-517.5
219	VCI	4865.0	-517.5
220	VCI	4935.0	-517.5
221	VCI	5005.0	-517.5
222	VCI	5075.0	-517.5
223	VCI	5145.0	-517.5
224	VCI	5215.0	-517.5
225	VCI	5285.0	-517.5
226	VCI	5355.0	-517.5
227	C12-	5425.0	-517.5
228	C12-	5495.0	-517.5
229	C12-	5565.0	-517.5
230	C12-	5635.0	-517.5
231	C12-	5705.0	-517.5
232	C12+	5775.0	-517.5
233	C12+	5845.0	-517.5
234	C12+	5915.0	-517.5
235	C12+	5985.0	-517.5
236	C12+	6055.0	-517.5
237	C11-	6125.0	-517.5
238	C11-	6195.0	-517.5
239	C11-	6265.0	-517.5
240	C11-	6335.0	-517.5

No.	Name	X	Y
241	C11-	6405.0	-517.5
242	C11+	6475.0	-517.5
243	C11+	6545.0	-517.5
244	C11+	6615.0	-517.5
245	C11+	6685.0	-517.5
246	C11+	6755.0	-517.5
247	AGNDDUM1	6825.0	-517.5
248	VLOUT3	6895.0	-517.5
249	VLOUT3	6965.0	-517.5
250	VGL	7035.0	-517.5
251	VGL	7105.0	-517.5
252	VGL	7175.0	-517.5
253	VGL	7245.0	-517.5
254	VGL	7315.0	-517.5
255	VGL	7385.0	-517.5
256	VGL	7455.0	-517.5
257	VGL	7525.0	-517.5
258	VGL	7595.0	-517.5
259	VGL	7665.0	-517.5
260	AGNDDUM2	7735.0	-517.5
261	AGNDDUM3	7805.0	-517.5
262	AGNDDUM4	7875.0	-517.5
263	VLOUT2	7945.0	-517.5
264	VLOUT2	8015.0	-517.5
265	VGH	8085.0	-517.5
266	VGH	8155.0	-517.5
267	VGH	8225.0	-517.5
268	VGH	8295.0	-517.5
269	TESTO27	8365.0	-517.5
270	C13-	8435.0	-517.5
271	C13-	8505.0	-517.5
272	C13-	8575.0	-517.5
273	TESTO28	8645.0	-517.5
274	C13+	8715.0	-517.5
275	C13+	8785.0	-517.5
276	C13+	8855.0	-517.5
277	TESTO29	8925.0	-517.5
278	C21-	8995.0	-517.5
279	C21-	9065.0	-517.5
280	C21-	9135.0	-517.5
281	C21+	9205.0	-517.5
282	C21+	9275.0	-517.5
283	C21+	9345.0	-517.5
284	C22-	9415.0	-517.5
285	C22-	9485.0	-517.5
286	C22-	9555.0	-517.5
287	C22+	9625.0	-517.5
288	C22+	9695.0	-517.5
289	C22+	9765.0	-517.5
290	C23-	9835.0	-517.5
291	C23-	9905.0	-517.5
292	C23-	9975.0	-517.5
293	C23+	10045.0	-517.5
294	C23+	10115.0	-517.5
295	C23+	10185.0	-517.5
296	TESTO30	10255.0	-517.5
297	DUMMYR5	10325.0	-517.5
298	DUMMYR6	10395.0	-517.5
299	TESTO31	10670.0	511.5
300	TESTO32	10650.0	386.5

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
301	DUMMYR7	10630.0	511.5	361	G115	9430.0	511.5	421	G235	8230.0	511.5	481	S706	6830.0	386.5	541	S646	5630.0	386.5
302	DUMMYR8	10610.0	386.5	362	G117	9410.0	386.5	422	G237	8210.0	386.5	482	S705	6810.0	511.5	542	S645	5610.0	511.5
303	VGLDMY1	10590.0	511.5	363	G119	9390.0	511.5	423	G239	8190.0	511.5	483	S704	6790.0	386.5	543	S644	5590.0	386.5
304	G1	10570.0	386.5	364	G121	9370.0	386.5	424	G241	8170.0	386.5	484	S703	6770.0	511.5	544	S643	5570.0	511.5
305	G3	10550.0	511.5	365	G123	9350.0	511.5	425	G243	8150.0	511.5	485	S702	6750.0	386.5	545	S642	5550.0	386.5
306	G5	10530.0	386.5	366	G125	9330.0	386.5	426	G245	8130.0	386.5	486	S701	6730.0	511.5	546	S641	5530.0	511.5
307	G7	10510.0	511.5	367	G127	9310.0	511.5	427	G247	8110.0	511.5	487	S700	6710.0	386.5	547	S640	5510.0	386.5
308	G9	10490.0	386.5	368	G129	9290.0	386.5	428	G249	8090.0	386.5	488	S699	6690.0	511.5	548	S639	5490.0	511.5
309	G11	10470.0	511.5	369	G131	9270.0	511.5	429	G251	8070.0	511.5	489	S698	6670.0	386.5	549	S638	5470.0	386.5
310	G13	10450.0	386.5	370	G133	9250.0	386.5	430	G253	8050.0	386.5	490	S697	6650.0	511.5	550	S637	5450.0	511.5
311	G15	10430.0	511.5	371	G135	9230.0	511.5	431	G255	8030.0	511.5	491	S696	6630.0	386.5	551	S636	5430.0	386.5
312	G17	10410.0	386.5	372	G137	9210.0	386.5	432	G257	8010.0	386.5	492	S695	6610.0	511.5	552	S635	5410.0	511.5
313	G19	10390.0	511.5	373	G139	9190.0	511.5	433	G259	7990.0	511.5	493	S694	6590.0	386.5	553	S634	5390.0	386.5
314	G21	10370.0	386.5	374	G141	9170.0	386.5	434	G261	7970.0	386.5	494	S693	6570.0	511.5	554	S633	5370.0	511.5
315	G23	10350.0	511.5	375	G143	9150.0	511.5	435	G263	7950.0	511.5	495	S692	6550.0	386.5	555	S632	5350.0	386.5
316	G25	10330.0	386.5	376	G145	9130.0	386.5	436	G265	7930.0	386.5	496	S691	6530.0	511.5	556	S631	5330.0	511.5
317	G27	10310.0	511.5	377	G147	9110.0	511.5	437	G267	7910.0	511.5	497	S690	6510.0	386.5	557	S630	5310.0	386.5
318	G29	10290.0	386.5	378	G149	9090.0	386.5	438	G269	7890.0	386.5	498	S689	6490.0	511.5	558	S629	5290.0	511.5
319	G31	10270.0	511.5	379	G151	9070.0	511.5	439	G271	7870.0	511.5	499	S688	6470.0	386.5	559	S628	5270.0	386.5
320	G33	10250.0	386.5	380	G153	9050.0	386.5	440	G273	7850.0	386.5	500	S687	6450.0	511.5	560	S627	5250.0	511.5
321	G35	10230.0	511.5	381	G155	9030.0	511.5	441	G275	7830.0	511.5	501	S686	6430.0	386.5	561	S626	5230.0	386.5
322	G37	10210.0	386.5	382	G157	9010.0	386.5	442	G277	7810.0	386.5	502	S685	6410.0	511.5	562	S625	5210.0	511.5
323	G39	10190.0	511.5	383	G159	8990.0	511.5	443	G279	7790.0	511.5	503	S684	6390.0	386.5	563	S624	5190.0	386.5
324	G41	10170.0	386.5	384	G161	8970.0	386.5	444	G281	7770.0	386.5	504	S683	6370.0	511.5	564	S623	5170.0	511.5
325	G43	10150.0	511.5	385	G163	8950.0	511.5	445	G283	7750.0	511.5	505	S682	6350.0	386.5	565	S622	5150.0	386.5
326	G45	10130.0	386.5	386	G165	8930.0	386.5	446	G285	7730.0	386.5	506	S681	6330.0	511.5	566	S621	5130.0	511.5
327	G47	10110.0	511.5	387	G167	8910.0	511.5	447	G287	7710.0	511.5	507	S680	6310.0	386.5	567	S620	5110.0	386.5
328	G49	10090.0	386.5	388	G169	8890.0	386.5	448	G289	7690.0	386.5	508	S679	6290.0	511.5	568	S619	5090.0	511.5
329	G51	10070.0	511.5	389	G171	8870.0	511.5	449	G291	7670.0	511.5	509	S678	6270.0	386.5	569	S618	5070.0	386.5
330	G53	10050.0	386.5	390	G173	8850.0	386.5	450	G293	7650.0	386.5	510	S677	6250.0	511.5	570	S617	5050.0	511.5
331	G55	10030.0	511.5	391	G175	8830.0	511.5	451	G295	7630.0	511.5	511	S676	6230.0	386.5	571	S616	5030.0	386.5
332	G57	10010.0	386.5	392	G177	8810.0	386.5	452	G297	7610.0	386.5	512	S675	6210.0	511.5	572	S615	5010.0	511.5
333	G59	9990.0	511.5	393	G179	8790.0	511.5	453	G299	7590.0	511.5	513	S674	6190.0	386.5	573	S614	4990.0	386.5
334	G61	9970.0	386.5	394	G181	8770.0	386.5	454	G301	7570.0	386.5	514	S673	6170.0	511.5	574	S613	4970.0	511.5
335	G63	9950.0	511.5	395	G183	8750.0	511.5	455	G303	7550.0	511.5	515	S672	6150.0	386.5	575	S612	4950.0	386.5
336	G65	9930.0	386.5	396	G185	8730.0	386.5	456	G305	7530.0	386.5	516	S671	6130.0	511.5	576	S611	4930.0	511.5
337	G67	9910.0	511.5	397	G187	8710.0	511.5	457	G307	7510.0	511.5	517	S670	6110.0	386.5	577	S610	4910.0	386.5
338	G69	9890.0	386.5	398	G189	8690.0	386.5	458	G309	7490.0	386.5	518	S669	6090.0	511.5	578	S609	4890.0	511.5
339	G71	9870.0	511.5	399	G191	8670.0	511.5	459	G311	7470.0	511.5	519	S668	6070.0	386.5	579	S608	4870.0	386.5
340	G73	9850.0	386.5	400	G193	8650.0	386.5	460	G313	7450.0	386.5	520	S667	6050.0	511.5	580	S607	4850.0	511.5
341	G75	9830.0	511.5	401	G195	8630.0	511.5	461	G315	7430.0	511.5	521	S666	6030.0	386.5	581	S606	4830.0	386.5
342	G77	9810.0	386.5	402	G197	8610.0	386.5	462	G317	7410.0	386.5	522	S665	6010.0	511.5	582	S605	4810.0	511.5
343	G79	9790.0	511.5	403	G199	8590.0	511.5	463	G319	7390.0	511.5	523	S664	5990.0	386.5	583	S604	4790.0	386.5
344	G81	9770.0	386.5	404	G201	8570.0	386.5	464	VGLDMY2	7370.0	386.5	524	S663	5970.0	511.5	584	S603	4770.0	511.5
345	G83	9750.0	511.5	405	G203	8550.0	511.5	465	TESTO33	7350.0	511.5	525	S662	5950.0	386.5	585	S602	4750.0	386.5
346	G85	9730.0	386.5	406	G205	8530.0	386.5	466	TESTO34	7130.0	511.5	526	S661	5930.0	511.5	586	S601	4730.0	511.5
347	G87	9710.0	511.5	407	G207	8510.0	511.5	467	S720	7110.0	386.5	527	S660	5910.0	386.5	587	S600	4710.0	386.5
348	G89	9690.0	386.5	408	G209	8490.0	386.5	468	S719	7090.0	511.5	528	S659	5890.0	511.5	588	S599	4690.0	511.5
349	G91	9670.0	511.5	409	G211	8470.0	511.5	469	S718	7070.0	386.5	529	S658	5870.0	386.5	589	S598	4670.0	386.5
350	G93	9650.0	386.5	410	G213	8450.0	386.5	470	S717	7050.0	511.5	530	S657	5850.0	511.5	590	S597	4650.0	511.5
351	G95	9630.0	511.5	411	G215	8430.0	511.5	471	S716	7030.0	386.5	531	S656	5830.0	386.5	591	S596	4630.0	386.5
352	G97	9610.0	386.5	412	G217	8410.0	386.5	472	S715	7010.0	511.5	532	S655	5810.0	511.5	592	S595	4610.0	511.5
353	G99	9590.0	511.5	413	G219	8390.0	511.5	473	S714	6990.0	386.5	533	S654	5790.0	386.5	593	S594	4590.0	386.5
354	G101	9570.0	386.5	414	G221	8370.0	386.5	474	S713	6970.0	511.5	534	S653	5770.0	511.5	594	S593	4570.0	511.5
355	G103	9550.0	511.5	415	G223	8350.0	511.5	475	S712	6950.0	386.5	535	S652	5750.0	386.5	595	S592	4550.0	386.5
356	G105	9530.0	386.5	416	G225	8330.0	386.5	476	S711	6930.0	511.5	536	S651	5730.0	511.5	596	S591	4530.0	511.5
357	G107	9510.0	511.5	417	G227	8310.0	511.5	477	S710	6910.0	386.5	537	S650	5710.0	386.5	597	S590	4510.0	386.5
358	G109	9490.0	386.5	418	G229	8290.0	386.5	478	S709	6890.0	511.5	538	S649	5690.0	511.5	598	S589	4490.0	511.5
359	G111	9470.0	511.5	419	G231	8270.0	511.5	479	S708	6870.0	386.5	539	S648	5670.0	386.5	599	S588	4470.0	386.5
360	G113	9450.0	386.5	420	G233	8250.0	386.5	480	S707	6850.0	511.5	540	S647	5650.0	511.5	600	S587	4450.0	511.5

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
601	S586	4430.0	386.5	661	S526	3230.0	386.5	721	S466	2030.0	386.5	781	S406	830.0	386.5	841	S346	-370.0	386.5
602	S585	4410.0	511.5	662	S525	3210.0	511.5	722	S465	2010.0	511.5	782	S405	810.0	511.5	842	S345	-390.0	511.5
603	S584	4390.0	386.5	663	S524	3190.0	386.5	723	S464	1990.0	386.5	783	S404	790.0	386.5	843	S344	-410.0	386.5
604	S583	4370.0	511.5	664	S523	3170.0	511.5	724	S463	1970.0	511.5	784	S403	770.0	511.5	844	S343	-430.0	511.5
605	S582	4350.0	386.5	665	S522	3150.0	386.5	725	S462	1950.0	386.5	785	S402	750.0	386.5	845	S342	-450.0	386.5
606	S581	4330.0	511.5	666	S521	3130.0	511.5	726	S461	1930.0	511.5	786	S401	730.0	511.5	846	S341	-470.0	511.5
607	S580	4310.0	386.5	667	S520	3110.0	386.5	727	S460	1910.0	386.5	787	S400	710.0	386.5	847	S340	-490.0	386.5
608	S579	4290.0	511.5	668	S519	3090.0	511.5	728	S459	1890.0	511.5	788	S399	690.0	511.5	848	S339	-510.0	511.5
609	S578	4270.0	386.5	669	S518	3070.0	386.5	729	S458	1870.0	386.5	789	S398	670.0	386.5	849	S338	-530.0	386.5
610	S577	4250.0	511.5	670	S517	3050.0	511.5	730	S457	1850.0	511.5	790	S397	650.0	511.5	850	S337	-550.0	511.5
611	S576	4230.0	386.5	671	S516	3030.0	386.5	731	S456	1830.0	386.5	791	S396	630.0	386.5	851	S336	-570.0	386.5
612	S575	4210.0	511.5	672	S515	3010.0	511.5	732	S455	1810.0	511.5	792	S395	610.0	511.5	852	S335	-590.0	511.5
613	S574	4190.0	386.5	673	S514	2990.0	386.5	733	S454	1790.0	386.5	793	S394	590.0	386.5	853	S334	-610.0	386.5
614	S573	4170.0	511.5	674	S513	2970.0	511.5	734	S453	1770.0	511.5	794	S393	570.0	511.5	854	S333	-630.0	511.5
615	S572	4150.0	386.5	675	S512	2950.0	386.5	735	S452	1750.0	386.5	795	S392	550.0	386.5	855	S332	-650.0	386.5
616	S571	4130.0	511.5	676	S511	2930.0	511.5	736	S451	1730.0	511.5	796	S391	530.0	511.5	856	S331	-670.0	511.5
617	S570	4110.0	386.5	677	S510	2910.0	386.5	737	S450	1710.0	386.5	797	S390	510.0	386.5	857	S330	-690.0	386.5
618	S569	4090.0	511.5	678	S509	2890.0	511.5	738	S449	1690.0	511.5	798	S389	490.0	511.5	858	S329	-710.0	511.5
619	S568	4070.0	386.5	679	S508	2870.0	386.5	739	S448	1670.0	386.5	799	S388	470.0	386.5	859	S328	-730.0	386.5
620	S567	4050.0	511.5	680	S507	2850.0	511.5	740	S447	1650.0	511.5	800	S387	450.0	511.5	860	S327	-750.0	511.5
621	S566	4030.0	386.5	681	S506	2830.0	386.5	741	S446	1630.0	386.5	801	S386	430.0	386.5	861	S326	-770.0	386.5
622	S565	4010.0	511.5	682	S505	2810.0	511.5	742	S445	1610.0	511.5	802	S385	410.0	511.5	862	S325	-790.0	511.5
623	S564	3990.0	386.5	683	S504	2790.0	386.5	743	S444	1590.0	386.5	803	S384	390.0	386.5	863	S324	-810.0	386.5
624	S563	3970.0	511.5	684	S503	2770.0	511.5	744	S443	1570.0	511.5	804	S383	370.0	511.5	864	S323	-830.0	511.5
625	S562	3950.0	386.5	685	S502	2750.0	386.5	745	S442	1550.0	386.5	805	S382	350.0	386.5	865	S322	-850.0	386.5
626	S561	3930.0	511.5	686	S501	2730.0	511.5	746	S441	1530.0	511.5	806	S381	330.0	511.5	866	S321	-870.0	511.5
627	S560	3910.0	386.5	687	S500	2710.0	386.5	747	S440	1510.0	386.5	807	S380	310.0	386.5	867	S320	-890.0	386.5
628	S559	3890.0	511.5	688	S499	2690.0	511.5	748	S439	1490.0	511.5	808	S379	290.0	511.5	868	S319	-910.0	511.5
629	S558	3870.0	386.5	689	S498	2670.0	386.5	749	S438	1470.0	386.5	809	S378	270.0	386.5	869	S318	-930.0	386.5
630	S557	3850.0	511.5	690	S497	2650.0	511.5	750	S437	1450.0	511.5	810	S377	250.0	511.5	870	S317	-950.0	511.5
631	S556	3830.0	386.5	691	S496	2630.0	386.5	751	S436	1430.0	386.5	811	S376	230.0	386.5	871	S316	-970.0	386.5
632	S555	3810.0	511.5	692	S495	2610.0	511.5	752	S435	1410.0	511.5	812	S375	210.0	511.5	872	S315	-990.0	511.5
633	S554	3790.0	386.5	693	S494	2590.0	386.5	753	S434	1390.0	386.5	813	S374	190.0	386.5	873	S314	-1010.0	386.5
634	S553	3770.0	511.5	694	S493	2570.0	511.5	754	S433	1370.0	511.5	814	S373	170.0	511.5	874	S313	-1030.0	511.5
635	S552	3750.0	386.5	695	S492	2550.0	386.5	755	S432	1350.0	386.5	815	S372	150.0	386.5	875	S312	-1050.0	386.5
636	S551	3730.0	511.5	696	S491	2530.0	511.5	756	S431	1330.0	511.5	816	S371	130.0	511.5	876	S311	-1070.0	511.5
637	S550	3710.0	386.5	697	S490	2510.0	386.5	757	S430	1310.0	386.5	817	S370	110.0	386.5	877	S310	-1090.0	386.5
638	S549	3690.0	511.5	698	S489	2490.0	511.5	758	S429	1290.0	511.5	818	S369	90.0	511.5	878	S309	-1110.0	511.5
639	S548	3670.0	386.5	699	S488	2470.0	386.5	759	S428	1270.0	386.5	819	S368	70.0	386.5	879	S308	-1130.0	386.5
640	S547	3650.0	511.5	700	S487	2450.0	511.5	760	S427	1250.0	511.5	820	S367	50.0	511.5	880	S307	-1150.0	511.5
641	S546	3630.0	386.5	701	S486	2430.0	386.5	761	S426	1230.0	386.5	821	S366	30.0	386.5	881	S306	-1170.0	386.5
642	S545	3610.0	511.5	702	S485	2410.0	511.5	762	S425	1210.0	511.5	822	S365	10.0	511.5	882	S305	-1190.0	511.5
643	S544	3590.0	386.5	703	S484	2390.0	386.5	763	S424	1190.0	386.5	823	S364	-10.0	386.5	883	S304	-1210.0	386.5
644	S543	3570.0	511.5	704	S483	2370.0	511.5	764	S423	1170.0	511.5	824	S363	-30.0	511.5	884	S303	-1230.0	511.5
645	S542	3550.0	386.5	705	S482	2350.0	386.5	765	S422	1150.0	386.5	825	S362	-50.0	386.5	885	S302	-1250.0	386.5
646	S541	3530.0	511.5	706	S481	2330.0	511.5	766	S421	1130.0	511.5	826	S361	-70.0	511.5	886	S301	-1270.0	511.5
647	S540	3510.0	386.5	707	S480	2310.0	386.5	767	S420	1110.0	386.5	827	S360	-90.0	386.5	887	S300	-1290.0	386.5
648	S539	3490.0	511.5	708	S479	2290.0	511.5	768	S419	1090.0	511.5	828	S359	-110.0	511.5	888	S299	-1310.0	511.5
649	S538	3470.0	386.5	709	S478	2270.0	386.5	769	S418	1070.0	386.5	829	S358	-130.0	386.5	889	S298	-1330.0	386.5
650	S537	3450.0	511.5	710	S477	2250.0	511.5	770	S417	1050.0	511.5	830	S357	-150.0	511.5	890	S297	-1350.0	511.5
651	S536	3430.0	386.5	711	S476	2230.0	386.5	771	S416	1030.0	386.5	831	S356	-170.0	386.5	891	S296	-1370.0	386.5
652	S535	3410.0	511.5	712	S475	2210.0	511.5	772	S415	1010.0	511.5	832	S355	-190.0	511.5	892	S295	-1390.0	511.5
653	S534	3390.0	386.5	713	S474	2190.0	386.5	773	S414	990.0	386.5	833	S354	-210.0	386.5	893	S294	-1410.0	386.5
654	S533	3370.0	511.5	714	S473	2170.0	511.5	774	S413	970.0	511.5	834	S353	-230.0	511.5	894	S293	-1430.0	511.5
655	S532	3350.0	386.5	715	S472	2150.0	386.5	775	S412	950.0	386.5	835	S352	-250.0	386.5	895	S292	-1450.0	386.5
656	S531	3330.0	511.5	716	S471	2130.0	511.5	776	S411	930.0	511.5	836	S351	-270.0	511.5	896	S291	-1470.0	511.5
657	S530	3310.0	386.5	717	S470	2110.0	386.5	777	S410	910.0	386.5	837	S350	-290.0	386.5	897	S290	-1490.0	386.5
658	S529	3290.0	511.5	718	S469	2090.0	511.5	778	S409	890.0	511.5	838	S349	-310.0	511.5	898	S289	-1510.0	511.5
659	S720	3270.0	386.5	719	S468	2070.0	386.5	779	S408	870.0	386.5	839	S348	-330.0	386.5	899	S288	-1530.0	386.5
660	S527	3250.0	511.5	720	S467	2050.0	511.5	780	S407	850.0	511.5	840	S347	-350.0	511.5	900	S287	-1550.0	511.5

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
901	S286	-1570.0	386.5	961	S226	-2770.0	386.5	1021	S166	-3970.0	386.5	1081	S106	-5170.0	386.5	1141	S46	-6370.0	386.5
902	S285	-1590.0	511.5	962	S225	-2790.0	511.5	1022	S165	-3990.0	511.5	1082	S105	-5190.0	511.5	1142	S45	-6390.0	511.5
903	S284	-1610.0	386.5	963	S224	-2810.0	386.5	1023	S164	-4010.0	386.5	1083	S104	-5210.0	386.5	1143	S44	-6410.0	386.5
904	S283	-1630.0	511.5	964	S223	-2830.0	511.5	1024	S163	-4030.0	511.5	1084	S103	-5230.0	511.5	1144	S43	-6430.0	511.5
905	S282	-1650.0	386.5	965	S222	-2850.0	386.5	1025	S162	-4050.0	386.5	1085	S102	-5250.0	386.5	1145	S42	-6450.0	386.5
906	S281	-1670.0	511.5	966	S221	-2870.0	511.5	1026	S161	-4070.0	511.5	1086	S101	-5270.0	511.5	1146	S41	-6470.0	511.5
907	S280	-1690.0	386.5	967	S220	-2890.0	386.5	1027	S160	-4090.0	386.5	1087	S100	-5290.0	386.5	1147	S40	-6490.0	386.5
908	S279	-1710.0	511.5	968	S219	-2910.0	511.5	1028	S159	-4110.0	511.5	1088	S99	-5310.0	511.5	1148	S39	-6510.0	511.5
909	S278	-1730.0	386.5	969	S218	-2930.0	386.5	1029	S158	-4130.0	386.5	1089	S98	-5330.0	386.5	1149	S38	-6530.0	386.5
910	S277	-1750.0	511.5	970	S217	-2950.0	511.5	1030	S157	-4150.0	511.5	1090	S97	-5350.0	511.5	1150	S37	-6550.0	511.5
911	S276	-1770.0	386.5	971	S216	-2970.0	386.5	1031	S156	-4170.0	386.5	1091	S96	-5370.0	386.5	1151	S36	-6570.0	386.5
912	S275	-1790.0	511.5	972	S215	-2990.0	511.5	1032	S155	-4190.0	511.5	1092	S95	-5390.0	511.5	1152	S35	-6590.0	511.5
913	S274	-1810.0	386.5	973	S214	-3010.0	386.5	1033	S154	-4210.0	386.5	1093	S94	-5410.0	386.5	1153	S34	-6610.0	386.5
914	S273	-1830.0	511.5	974	S213	-3030.0	511.5	1034	S153	-4230.0	511.5	1094	S93	-5430.0	511.5	1154	S33	-6630.0	511.5
915	S272	-1850.0	386.5	975	S212	-3050.0	386.5	1035	S152	-4250.0	386.5	1095	S92	-5450.0	386.5	1155	S32	-6650.0	386.5
916	S271	-1870.0	511.5	976	S211	-3070.0	511.5	1036	S151	-4270.0	511.5	1096	S91	-5470.0	511.5	1156	S31	-6670.0	511.5
917	S270	-1890.0	386.5	977	S210	-3090.0	386.5	1037	S150	-4290.0	386.5	1097	S90	-5490.0	386.5	1157	S30	-6690.0	386.5
918	S269	-1910.0	511.5	978	S209	-3110.0	511.5	1038	S149	-4310.0	511.5	1098	S89	-5510.0	511.5	1158	S29	-6710.0	511.5
919	S268	-1930.0	386.5	979	S208	-3130.0	386.5	1039	S148	-4330.0	386.5	1099	S88	-5530.0	386.5	1159	S28	-6730.0	386.5
920	S267	-1950.0	511.5	980	S207	-3150.0	511.5	1040	S147	-4350.0	511.5	1100	S87	-5550.0	511.5	1160	S27	-6750.0	511.5
921	S266	-1970.0	386.5	981	S206	-3170.0	386.5	1041	S146	-4370.0	386.5	1101	S86	-5570.0	386.5	1161	S26	-6770.0	386.5
922	S265	-1990.0	511.5	982	S205	-3190.0	511.5	1042	S145	-4390.0	511.5	1102	S85	-5590.0	511.5	1162	S25	-6790.0	511.5
923	S264	-2010.0	386.5	983	S204	-3210.0	386.5	1043	S144	-4410.0	386.5	1103	S84	-5610.0	386.5	1163	S24	-6810.0	386.5
924	S263	-2030.0	511.5	984	S203	-3230.0	511.5	1044	S143	-4430.0	511.5	1104	S83	-5630.0	511.5	1164	S23	-6830.0	511.5
925	S262	-2050.0	386.5	985	S202	-3250.0	386.5	1045	S142	-4450.0	386.5	1105	S82	-5650.0	386.5	1165	S22	-6850.0	386.5
926	S261	-2070.0	511.5	986	S201	-3270.0	511.5	1046	S141	-4470.0	511.5	1106	S81	-5670.0	511.5	1166	S21	-6870.0	511.5
927	S260	-2090.0	386.5	987	S200	-3290.0	386.5	1047	S140	-4490.0	386.5	1107	S80	-5690.0	386.5	1167	S20	-6890.0	386.5
928	S259	-2110.0	511.5	988	S199	-3310.0	511.5	1048	S139	-4510.0	511.5	1108	S79	-5710.0	511.5	1168	S19	-6910.0	511.5
929	S258	-2130.0	386.5	989	S198	-3330.0	386.5	1049	S138	-4530.0	386.5	1109	S78	-5730.0	386.5	1169	S18	-6930.0	386.5
930	S257	-2150.0	511.5	990	S197	-3350.0	511.5	1050	S137	-4550.0	511.5	1110	S77	-5750.0	511.5	1170	S17	-6950.0	511.5
931	S256	-2170.0	386.5	991	S196	-3370.0	386.5	1051	S136	-4570.0	386.5	1111	S76	-5770.0	386.5	1171	S16	-6970.0	386.5
932	S255	-2190.0	511.5	992	S195	-3390.0	511.5	1052	S135	-4590.0	511.5	1112	S75	-5790.0	511.5	1172	S15	-6990.0	511.5
933	S254	-2210.0	386.5	993	S194	-3410.0	386.5	1053	S134	-4610.0	386.5	1113	S74	-5810.0	386.5	1173	S14	-7010.0	386.5
934	S253	-2230.0	511.5	994	S193	-3430.0	511.5	1054	S133	-4630.0	511.5	1114	S73	-5830.0	511.5	1174	S13	-7030.0	511.5
935	S252	-2250.0	386.5	995	S192	-3450.0	386.5	1055	S132	-4650.0	386.5	1115	S72	-5850.0	386.5	1175	S12	-7050.0	386.5
936	S251	-2270.0	511.5	996	S191	-3470.0	511.5	1056	S131	-4670.0	511.5	1116	S71	-5870.0	511.5	1176	S11	-7070.0	511.5
937	S250	-2290.0	386.5	997	S190	-3490.0	386.5	1057	S130	-4690.0	386.5	1117	S70	-5890.0	386.5	1177	S10	-7090.0	386.5
938	S249	-2310.0	511.5	998	S189	-3510.0	511.5	1058	S129	-4710.0	511.5	1118	S69	-5910.0	511.5	1178	S9	-7110.0	511.5
939	S248	-2330.0	386.5	999	S188	-3530.0	386.5	1059	S128	-4730.0	386.5	1119	S68	-5930.0	386.5	1179	S8	-7130.0	386.5
940	S247	-2350.0	511.5	1000	S187	-3550.0	511.5	1060	S127	-4750.0	511.5	1120	S67	-5950.0	511.5	1180	S7	-7150.0	511.5
941	S246	-2370.0	386.5	1001	S186	-3570.0	386.5	1061	S126	-4770.0	386.5	1121	S66	-5970.0	386.5	1181	S6	-7170.0	386.5
942	S245	-2390.0	511.5	1002	S185	-3590.0	511.5	1062	S125	-4790.0	511.5	1122	S65	-5990.0	511.5	1182	S5	-7190.0	511.5
943	S244	-2410.0	386.5	1003	S184	-3610.0	386.5	1063	S124	-4810.0	386.5	1123	S64	-6010.0	386.5	1183	S4	-7210.0	386.5
944	S243	-2430.0	511.5	1004	S183	-3630.0	511.5	1064	S123	-4830.0	511.5	1124	S63	-6030.0	511.5	1184	S3	-7230.0	511.5
945	S242	-2450.0	386.5	1005	S182	-3650.0	386.5	1065	S122	-4850.0	386.5	1125	S62	-6050.0	386.5	1185	S2	-7250.0	386.5
946	S241	-2470.0	511.5	1006	S181	-3670.0	511.5	1066	S121	-4870.0	511.5	1126	S61	-6070.0	511.5	1186	S1	-7270.0	511.5
947	S240	-2490.0	386.5	1007	S180	-3690.0	386.5	1067	S120	-4890.0	386.5	1127	S60	-6090.0	386.5	1187	TESTO35	-7290.0	386.5
948	S239	-2510.0	511.5	1008	S179	-3710.0	511.5	1068	S119	-4910.0	511.5	1128	S59	-6110.0	511.5	1188	TESTO36	-7350.0	511.5
949	S238	-2530.0	386.5	1009	S178	-3730.0	386.5	1069	S118	-4930.0	386.5	1129	S58	-6130.0	386.5	1189	VGLDMY3	-7370.0	386.5
950	S237	-2550.0	511.5	1010	S177	-3750.0	511.5	1070	S117	-4950.0	511.5	1130	S57	-6150.0	511.5	1190	G320	-7390.0	511.5
951	S236	-2570.0	386.5	1011	S176	-3770.0	386.5	1071	S116	-4970.0	386.5	1131	S56	-6170.0	386.5	1191	G318	-7410.0	386.5
952	S235	-2590.0	511.5	1012	S175	-3790.0	511.5	1072	S115	-4990.0	511.5	1132	S55	-6190.0	511.5	1192	G316	-7430.0	511.5
953	S234	-2610.0	386.5	1013	S174	-3810.0	386.5	1073	S114	-5010.0	386.5	1133	S54	-6210.0	386.5	1193	G314	-7450.0	386.5
954	S233	-2630.0	511.5	1014	S173	-3830.0	511.5	1074	S113	-5030.0	511.5	1134	S53	-6230.0	511.5	1194	G312	-7470.0	511.5
955	S232	-2650.0	386.5	1015	S172	-3850.0	386.5	1075	S112	-5050.0	386.5	1135	S52	-6250.0	386.5	1195	G310	-7490.0	386.5
956	S231	-2670.0	511.5	1016	S171	-3870.0	511.5	1076	S111	-5070.0	511.5	1136	S51	-6270.0	511.5	1196	G308	-7510.0	511.5
957	S230	-2690.0	386.5	1017	S170	-3890.0	386.5	1077	S110	-5090.0	386.5	1137	S50	-6290.0	386.5	1197	G306	-7530.0	386.5
958	S229	-2710.0	511.5	1018	S169	-3910.0	511.5	1078	S109	-5110.0	511.5	1138	S49	-6310.0	511.5	1198	G304	-7550.0	511.5
959	S228	-2730.0	386.5	1019	S168	-3930.0	386.5	1079	S108	-5130.0	386.5	1139	S48	-6330.0	386.5	1199	G302	-7570.0	386.5
960	S227	-2750.0	511.5	1020	S167	-3950.0	511.5	1080	S107	-5150.0	511.5	1140	S47	-6350.0	511.5	1200	G300	-7590.0	511.5

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1201	G298	-7610.0	386.5	1261	G178	-8810.0	386.5	1321	G58	-10010.0	386.5
1202	G296	-7630.0	511.5	1262	G176	-8830.0	511.5	1322	G56	-10030.0	511.5
1203	G294	-7650.0	386.5	1263	G174	-8850.0	386.5	1323	G54	-10050.0	386.5
1204	G292	-7670.0	511.5	1264	G172	-8870.0	511.5	1324	G52	-10070.0	511.5
1205	G290	-7690.0	386.5	1265	G170	-8890.0	386.5	1325	G50	-10090.0	386.5
1206	G288	-7710.0	511.5	1266	G168	-8910.0	511.5	1326	G48	-10110.0	511.5
1207	G286	-7730.0	386.5	1267	G166	-8930.0	386.5	1327	G46	-10130.0	386.5
1208	G284	-7750.0	511.5	1268	G164	-8950.0	511.5	1328	G44	-10150.0	511.5
1209	G282	-7770.0	386.5	1269	G162	-8970.0	386.5	1329	G42	-10170.0	386.5
1210	G280	-7790.0	511.5	1270	G160	-8990.0	511.5	1330	G40	-10190.0	511.5
1211	G278	-7810.0	386.5	1271	G158	-9010.0	386.5	1331	G38	-10210.0	386.5
1212	G276	-7830.0	511.5	1272	G156	-9030.0	511.5	1332	G36	-10230.0	511.5
1213	G274	-7850.0	386.5	1273	G154	-9050.0	386.5	1333	G34	-10250.0	386.5
1214	G272	-7870.0	511.5	1274	G152	-9070.0	511.5	1334	G32	-10270.0	511.5
1215	G270	-7890.0	386.5	1275	G150	-9090.0	386.5	1335	G30	-10290.0	386.5
1216	G268	-7910.0	511.5	1276	G148	-9110.0	511.5	1336	G28	-10310.0	511.5
1217	G266	-7930.0	386.5	1277	G146	-9130.0	386.5	1337	G26	-10330.0	386.5
1218	G264	-7950.0	511.5	1278	G144	-9150.0	511.5	1338	G24	-10350.0	511.5
1219	G262	-7970.0	386.5	1279	G142	-9170.0	386.5	1339	G22	-10370.0	386.5
1220	G260	-7990.0	511.5	1280	G140	-9190.0	511.5	1340	G20	-10390.0	511.5
1221	G258	-8010.0	386.5	1281	G138	-9210.0	386.5	1341	G18	-10410.0	386.5
1222	G256	-8030.0	511.5	1282	G136	-9230.0	511.5	1342	G16	-10430.0	511.5
1223	G254	-8050.0	386.5	1283	G134	-9250.0	386.5	1343	G14	-10450.0	386.5
1224	G252	-8070.0	511.5	1284	G132	-9270.0	511.5	1344	G12	-10470.0	511.5
1225	G250	-8090.0	386.5	1285	G130	-9290.0	386.5	1345	G10	-10490.0	386.5
1226	G248	-8110.0	511.5	1286	G128	-9310.0	511.5	1346	G8	-10510.0	511.5
1227	G246	-8130.0	386.5	1287	G126	-9330.0	386.5	1347	G6	-10530.0	386.5
1228	G244	-8150.0	511.5	1288	G124	-9350.0	511.5	1348	G4	-10550.0	511.5
1229	G242	-8170.0	386.5	1289	G122	-9370.0	386.5	1349	G2	-10570.0	386.5
1230	G240	-8190.0	511.5	1290	G120	-9390.0	511.5	1350	VGLDMY4	-10590.0	511.5
1231	G238	-8210.0	386.5	1291	G118	-9410.0	386.5	1351	DUMMYR9	-10610.0	386.5
1232	G236	-8230.0	511.5	1292	G116	-9430.0	511.5	1352	DUMMYR10	-10630.0	511.5
1233	G234	-8250.0	386.5	1293	G114	-9450.0	386.5	1353	TESTO37	-10650.0	386.5
1234	G232	-8270.0	511.5	1294	G112	-9470.0	511.5	1354	TESTO38	-10670.0	511.5
1235	G230	-8290.0	386.5	1295	G110	-9490.0	386.5				
1236	G228	-8310.0	511.5	1296	G108	-9510.0	511.5				
1237	G226	-8330.0	386.5	1297	G106	-9530.0	386.5				
1238	G224	-8350.0	511.5	1298	G104	-9550.0	511.5				
1239	G222	-8370.0	386.5	1299	G102	-9570.0	386.5				
1240	G220	-8390.0	511.5	1300	G100	-9590.0	511.5				
1241	G218	-8410.0	386.5	1301	G98	-9610.0	386.5				
1242	G216	-8430.0	511.5	1302	G96	-9630.0	511.5				
1243	G214	-8450.0	386.5	1303	G94	-9650.0	386.5				
1244	G212	-8470.0	511.5	1304	G92	-9670.0	511.5				
1245	G210	-8490.0	386.5	1305	G90	-9690.0	386.5				
1246	G208	-8510.0	511.5	1306	G88	-9710.0	511.5				
1247	G206	-8530.0	386.5	1307	G86	-9730.0	386.5				
1248	G204	-8550.0	511.5	1308	G84	-9750.0	511.5				
1249	G202	-8570.0	386.5	1309	G82	-9770.0	386.5				
1250	G200	-8590.0	511.5	1310	G80	-9790.0	511.5				
1251	G198	-8610.0	386.5	1311	G78	-9810.0	386.5				
1252	G196	-8630.0	511.5	1312	G76	-9830.0	511.5				
1253	G194	-8650.0	386.5	1313	G74	-9850.0	386.5				
1254	G192	-8670.0	511.5	1314	G72	-9870.0	511.5				
1255	G190	-8690.0	386.5	1315	G70	-9890.0	386.5				
1256	G188	-8710.0	511.5	1316	G68	-9910.0	511.5				
1257	G186	-8730.0	386.5	1317	G66	-9930.0	386.5				
1258	G184	-8750.0	511.5	1318	G64	-9950.0	511.5		Alignment mark	X	Y
1259	G182	-8770.0	386.5	1319	G62	-9970.0	386.5		1-a	-10613.0	-468.0
1260	G180	-8790.0	511.5	1320	G60	-9990.0	511.5		1-b	10613.0	-468.0

S1 ~ S720 G1 ~ G320 DUMMY DUMMYR TESTO VGLDMY (No. 299 ~ 1354)	Unit: um
I/O Pads (No. 1 ~ 298)	Pad Pump Pad Pump

6. Block Description

MPU System Interface

ILI9320 supports three system high-speed interfaces: i80-system high-speed interfaces to 8-, 9-, 16-, 18-bit parallel ports and serial peripheral interface (SPI). The interface mode is selected by setting the IM[3:0] pins.

ILI9320 has a 16-bit index register (IR), an 18-bit write-data register (WDR), and an 18-bit read-data register (RDR). The IR is the register to store index information from control registers and the internal GRAM. The WDR is the register to temporarily store data to be written to control registers and the internal GRAM. The RDR is the register to temporarily store data read from the GRAM. Data from the MPU to be written to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in internal operation. Data are read via the RDR from the internal GRAM. Therefore, invalid data are read out to the data bus when the ILI9320 read the first data from the internal GRAM. Valid data are read out after the ILI9320 performs the second read operation.

Registers are written consecutively as the register execution time except starting oscillator takes 0 clock cycle.

Registers selection by system interface (8-/9-/16-/18-bit bus width)			I80
Function	RS	nWR	nRD
Write an index to IR register	0	0	1
Read an internal status	0	1	0
Write to control registers or the internal GRAM by WDR register.	1	0	1
Read from the internal GRAM by RDR register.	1	1	0

Registers selection by the SPI system interface		
Function	R/W	RS
Write an index to IR register	0	0
Read an internal status	1	0
Write to control registers or the internal GRAM by WDR register.	0	1
Read from the internal GRAM by RDR register.	1	1

Parallel RGB Interface

ILI9320 supports the RGB interface and the VSYNC interface as the external interface for displaying a moving picture. When the RGB interface is selected, display operations are synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface mode, data (DB17-0) are written in synchronization with these signals according to the polarity of enable signal (ENABLE) to prevent flicker on display while updating display data.

In VSYNC interface mode, the display operation is synchronized with the internal clock except frame synchronization, where the operation is synchronized with the VSYNC signal. Display data are written to the internal GRAM via the system interface. In this case, there are constraints in speed and method in writing data to the internal RAM. For details, see the "External Display Interface" section. The ILI9320 allows for switching between the external display interface and the system interface by instruction so that the optimum interface is

selected for the kind of picture to be displayed on the screen (still and/or moving picture(s)). The RGB interface, by writing all display data to the internal RAM, allows for transferring data only when updating the frames of a moving picture, contributing to low power requirement for moving picture display.

Bit Operation

The ILI9320 supports a write data mask function for selectively writing data to the internal RAM in units of bits and a logical/compare operation to write data to the GRAM only when a condition is met as a result of comparing the data and the compare register bits. For details, see "Graphics Operation Functions".

Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register for setting a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As writing data to the internal GRAM, the address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

Graphics RAM (GRAM)

GRAM is graphics RAM storing bit-pattern data of 172,820 (240 x 320x 18/8) bytes with 18 bits per pixel.

Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates a liquid crystal drive voltage according to grayscale data set in the γ-correction register to display in 262,144 colors. For details, see the "γ-Correction Register" section.

Timing Controller

The timing generator generates a timing signal for operation of internal circuits such as the internal GRAM. The timing for the display operation such as RAM read operation and the timing for the internal operation such as access from the MPU are generated in the way not to interfere each other.

Oscillator (OSC)

ILI9320 implements internal/external resistor to generate the oscillation frequency and internal resistor will be used in the default setting. User can adjust the frame rate by the R2bh and R90h registers when internal resistor is used or adjust the frame rate by the external resistor which is placed between the OSC1 and OSC2 pins.

LCD Driver Circuit

The LCD driver circuit of ILI9320 consists of a 720-output source driver (S1 ~ S720) and a 320-output gate driver (G1~G320). Display pattern data are latched when the 720th bit data are input. The latched data control the source driver and generate a drive waveform. The gate driver for scanning gate lines outputs either VGH

or VGL level. The shift direction of 720 source outputs from the source driver is set with the SS bit and the shift direction of gate outputs from the gate driver is set with the GS bit. The scan mode by the gate driver is set with the SM bit. These bits allow setting an appropriate scan method for an LCD module.

LCD Driver Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels VREG1OUT, VGH, VGL and Vcom for driving an LCD.

7. System Interface

7.1. Interface Specifications

ILI9320 has the system interface to read/write the control registers and display graphics memory (GRAM), and the RGB Input Interface for displaying a moving picture. User can select an optimum interface to display the moving or still picture with efficient data transfer. All display data are stored in the GRAM to reduce the data transfer efforts and only the updating data is necessary to be transferred. User can only update a sub-range of GRAM by using the window address function.

ILI9320 also has the RGB interface and VSYNC interface to transfer the display data without flicker the moving picture on the screen. In RGB interface mode, the display data is written into the GRAM through the control signals of ENABLE, VSYNC, HSYNC, DOTCLK and data bus DB[17:0].

In VSYNC interface mode, the internal display timing is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface mode enables to display the moving picture display through the system interface. In this case, there are some constraints of speed and method to write data to the internal RAM.

ILI9320 operates in one of the following 4 modes. The display mode can be switched by the control register. When switching from one mode to another, refer to the sequences mentioned in the sections of RGB and VSYNC interfaces.

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM[1:0])
Internal operating clock only (Displaying still pictures)	System interface (RM = 0)	Internal operating clock (DM[1:0] = 00)
RGB interface (1) (Displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM[1:0] = 01)
RGB interface (2) (Rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM[1:0] = 01)
VSYNC interface (Displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM[1:0] = 10)

Note 1) Registers are set only via the system interface.

Note 2) The RGB-I/F and the VSYNC-I/F are not available simultaneously.
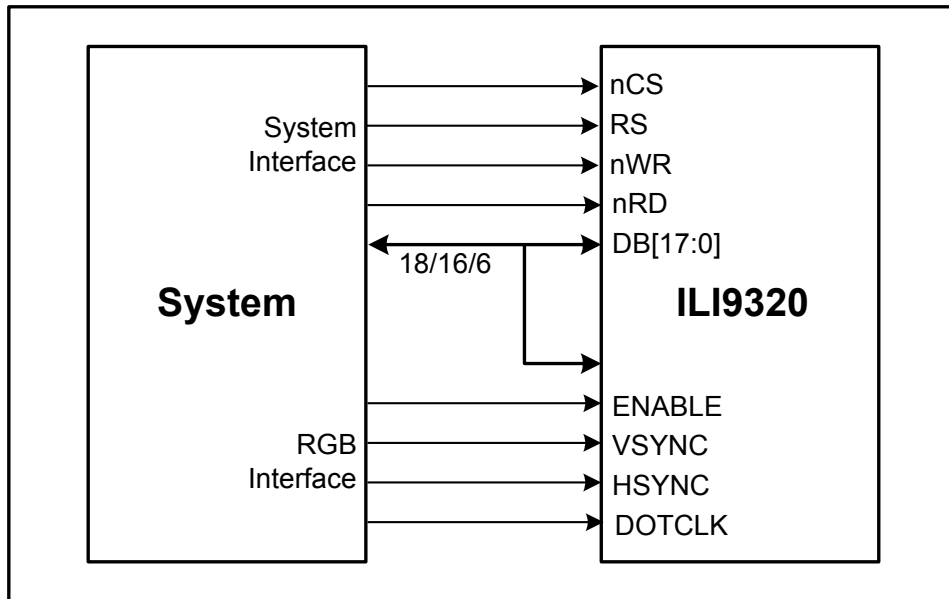
Figure1 System Interface and RGB Interface connection

7.2. Input Interfaces

The following are the system interfaces available with the ILI9320. The interface is selected by setting the IM[3:0] pins. The system interface is used for setting registers and GRAM access.

IM3	IM2	IM1	IM0/ID	Interface Mode	DB Pin
0	0	0	0	Setting invalid	
0	0	0	1	Setting invalid	
0	0	1	0	i80-system 16-bit interface	DB[17:10], DB[8:1]
0	0	1	1	i80-system 8-bit interface	DB[17:10]
0	1	0	ID	Serial Peripheral Interface (SPI)	SDI, SDO
0	1	1	*	Setting invalid	
1	0	0	0	Setting invalid	
1	0	0	1	Setting invalid	
1	0	1	0	i80-system18-bit interface	DB[17:0]
1	0	1	1	i80-system 9-bit interface	DB[17:9]
1	1	*	*	Setting invalid	

7.2.1. i80/18-bit System Interface

The i80/18-bit system interface is selected by setting the IM[3:0] as "1010" levels.
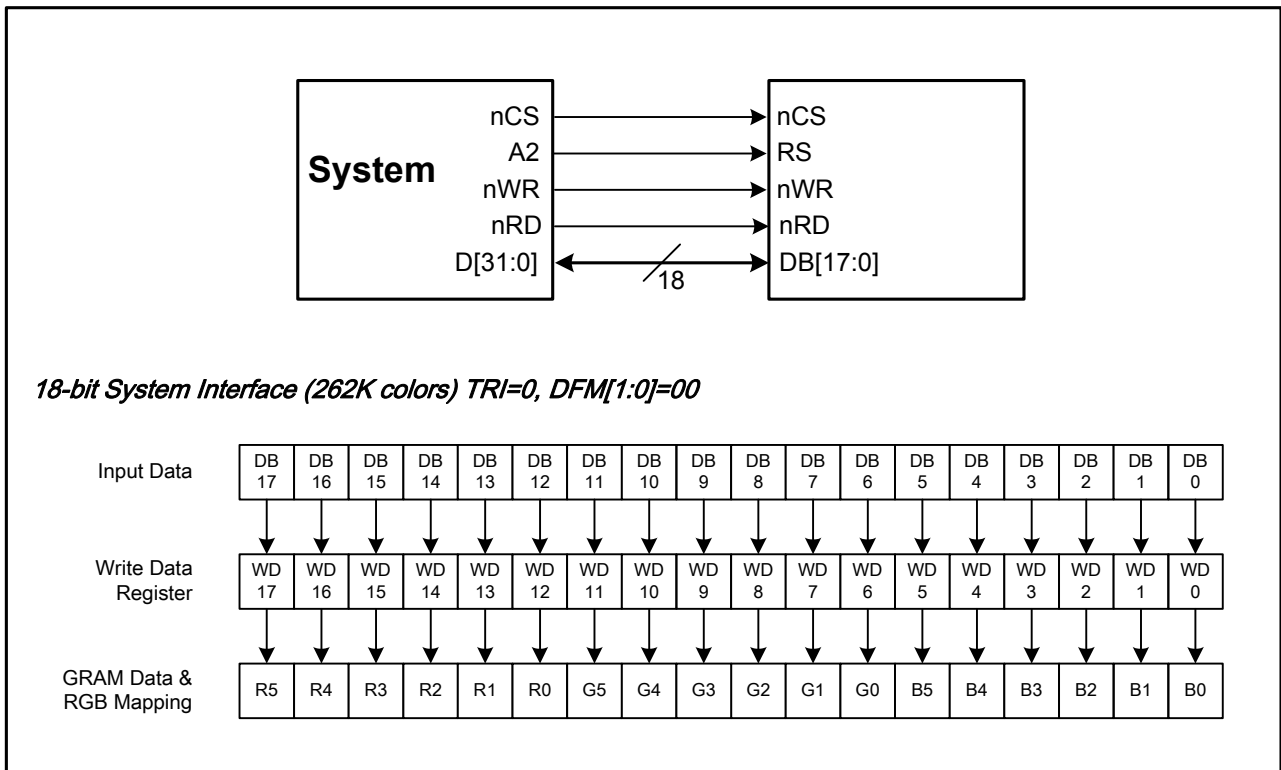
Figure2 18-bit System Interface Data Format

7.2.2. i80/16-bit System Interface

The i80/16-bit system interface is selected by setting the IM[3:0] as "0010" levels. The 262K or 65K color can be display through the 16-bit MPU interface. When the 262K color is displayed, two transfers (1st transfer: 2 bits, 2nd transfer: 16 bits or 1st transfer: 16 bits, 2nd transfer: 2 bits) are necessary for the 16-bit CPU interface.

TRI	DFM	16-bit MPU System Interface Data Format
0	*	**system 16-bit interface (1 transfers/pixel) 65,536 colors**
1	0	**80-system 16-bit interface (2 transfers/pixel) 262,144 colors**
1	1	**80-system 16-bit interface (2 transfers/pixel) 262,144 colors**
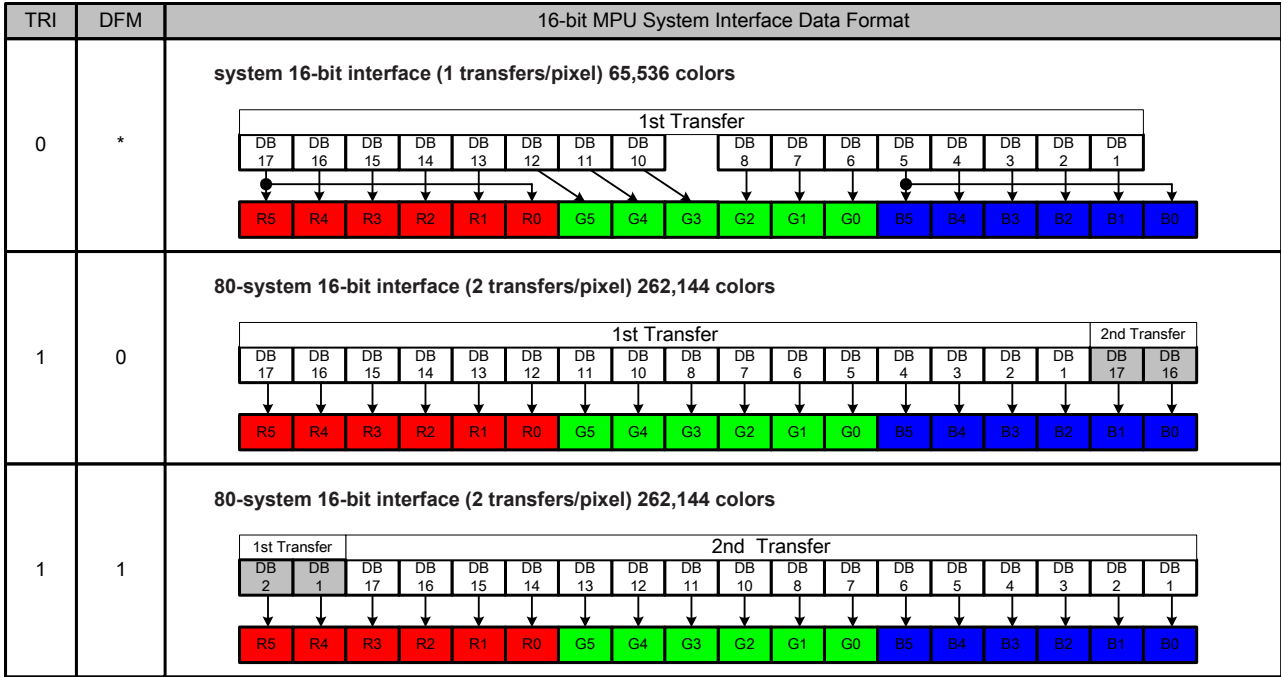
Figure3 16-bit System Interface Data Format

7.2.3. i80/9-bit System Interface

The i80/9-bit system interface is selected by setting the IM[3:0] as "1011" and the DB17~DB9 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (9 bits) and lower byte, and the upper byte is transferred first. The unused DB[8:0] pins must be tied to AGND.
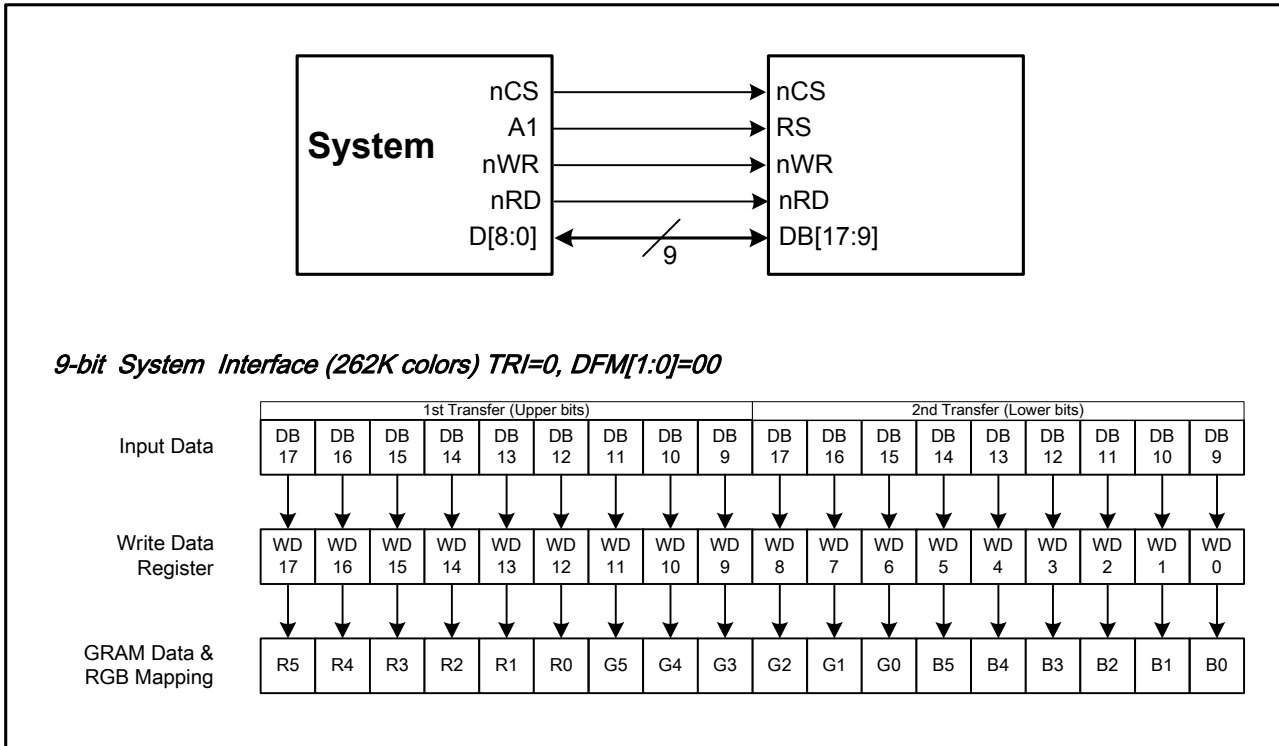
Figure4 9-bit System Interface Data Format

7.2.4. i80/8-bit System Interface

The i80/8-bit system interface is selected by setting the IM[3:0] as "0011" and the DB17~DB10 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (8 bits) and lower byte, and the upper byte is transferred first. The written data is expanded into 18 bits internally (see the figure below) and then written into GRAM. The unused DB[9:0] pins must be tied to AGND.
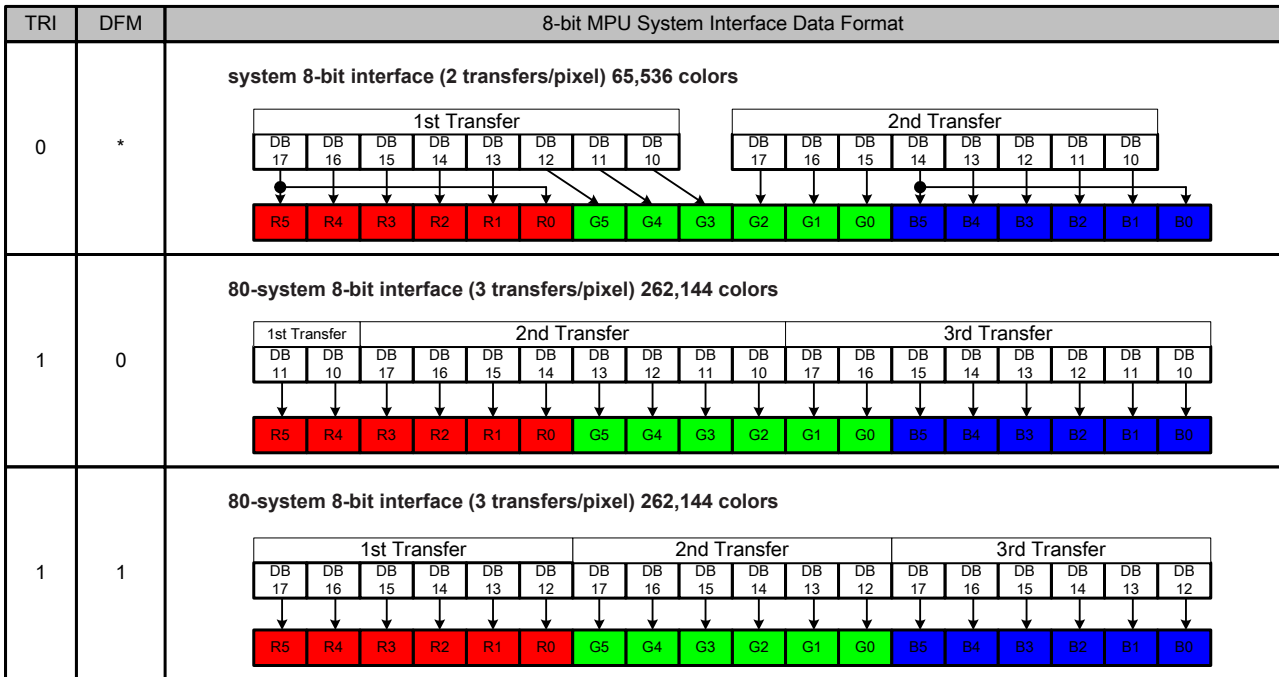
Figure5 8-bit System Interface Data Format

Data transfer synchronization in 8/9-bit bus interface mode

ILI9320 supports a data transfer synchronization function to reset upper and lower counters which count the transfers numbers of upper and lower byte in 8/9-bit interface mode. If a mismatch arises in the numbers of transfers between the upper and lower byte counters due to noise and so on, the "00"h register is written 4 times consecutively to reset the upper and lower counters so that data transfer will restart with a transfer of upper byte. This synchronization function can effectively prevent display error if the upper/lower counters are periodically reset.
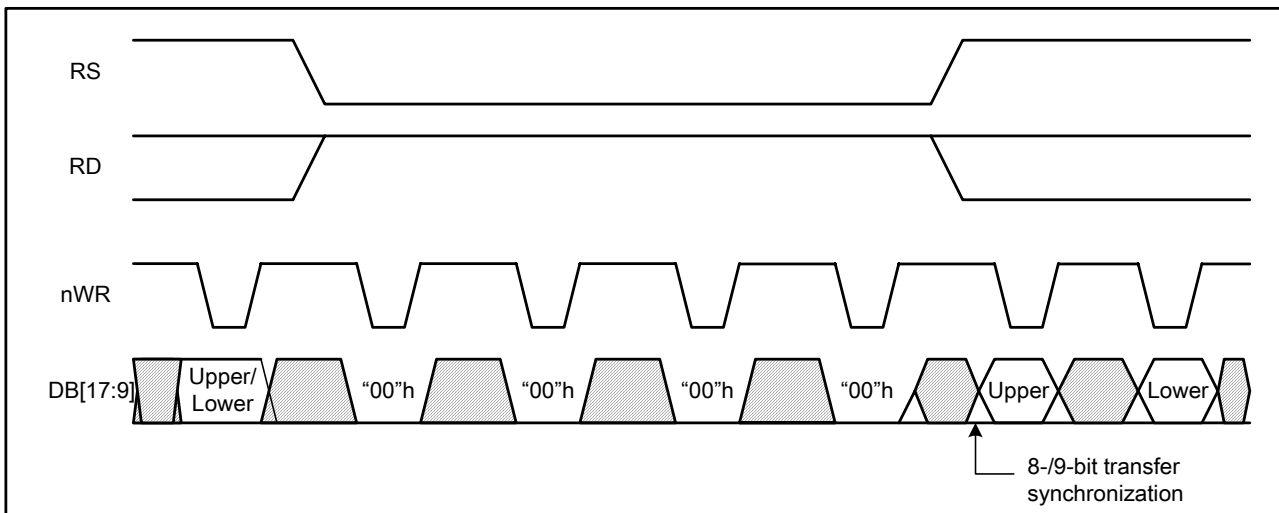
Figure6 Data Transfer Synchronization in 8/9-bit System Interface

7.3. Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is selected by setting the IM[3:0] pins as "010x" level. The chip select pin

(nCS), the serial transfer clock pin (SCL), the serial data input pin (SDI) and the serial data output pin (SDO) are used in SPI mode. The ID pin sets the least significant bit of the identification code. The DB[17:0] pins, which are not used, must be tied to DGND.

The SPI interface operation enables from the falling edge of nCS and ends of data transfer on the rising edge of nCS. The start byte is transferred to start the SPI interface and the read/write operation and RS information are also included in the start byte. When the start byte is matched, the subsequent data is received by ILI9320.

The seventh bit of start byte is RS bit. When RS = "0", either index write operation or status read operation is executed. When RS = "1", either register write operation or RAM read/write operation is executed. The eighth bit of the start byte is used to select either read or write operation (R/W bit). Data is written when the R/W bit is "0" and read back when the R/W bit is "1".

After receiving the start byte, ILI9320 starts to transfer or receive the data in unit of byte and the data transfer starts from the MSB bit. All the registers of the ILI9320 are 16-bit format and receive the first and the second byte datat as the upper and the lower eight bits of the 16-bit register respectively. In SPI mode, 5 bytes dummy read is necessary and the valid data starts from 6th byte of read back data.

Start Byte Format

Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start				Device ID code			RS	R/W
		0	1	1	1	0	ID	1/0	1/0

Note: ID bit is selected by setting the IM0/ID pin.

RS and R/W Bit Function

RS	R/W	Function
0	0	Set an index register
0	1	Read a status
1	0	Write a register or GRAM data
1	1	Read a register or GRAM data

Serial Peripheral Interface for register access

SPI Input Data	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8		D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Register Data	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8		IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0

Serial Peripheral Interface 65K colors

Input Data	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8		D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Write Data Register	WD 17	WD 16	WD 15	WD 14	WD 13	WD 12	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0
GRAM Data RGB mapping	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Figure 7 Data Format of SPI Interface

(a) Basic data transmission through SPI

nCS (Input) — Start ... End

SCL (Input) — 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24

SDI (Input) — 0 1 1 1 0 ID RS RW D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0

Start Byte | Index register, registers setting, and GRAM write

SDO (Output) — D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0

Status, registers read and GRAM read

(b) GRAM data read transmission

nCS (Input) — Start ... End

SCL (Input)

SDI (Input) — Start Byte RS=1, RW=1

SDO (Output) — Dummy read 1 | Dummy read 2 | Dummy read 3 | Dummy read 4 | Dummy read 5 | RAM read upper byte | RAM read lower byte

Note: Five bytes of invalid dummy data read after the start byte.

(c) Status/registers read transmission

nCS (Input) — Start ... End

SCL (Input) — 1 ... 8 9 ... 16 17 ... 24 25 ... 32

SDI (Input) — Start Byte

SDO (Output) — Dummy read 1 | Register 1 upper eight bits | Register 1 lower eight bits

Note: One byte of invalid dummy data read after the start byte.

Figure8 Data transmission through serial peripheral interface (SPI)

7.4. VSYNC Interface

ILI9320 supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the i80 system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = "10" and RM = "0".
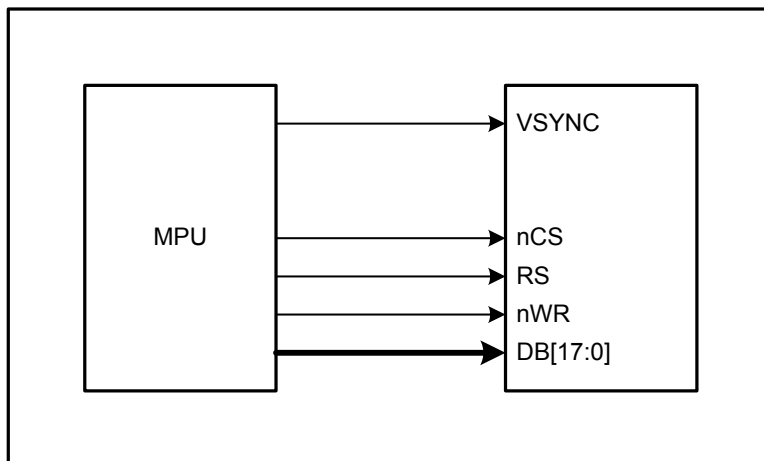
Figure9 Data transmission through VSYNC interface)

In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.
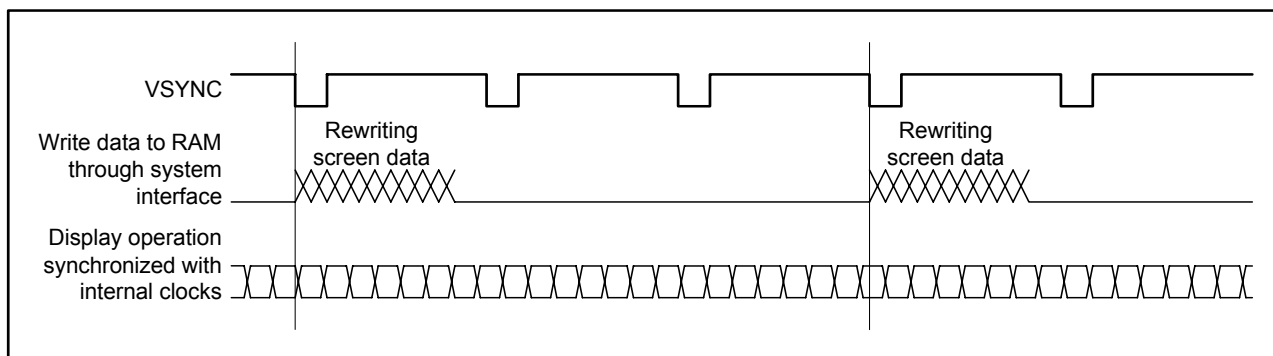
Figure10 Moving picture data transmission through VSYNC interface
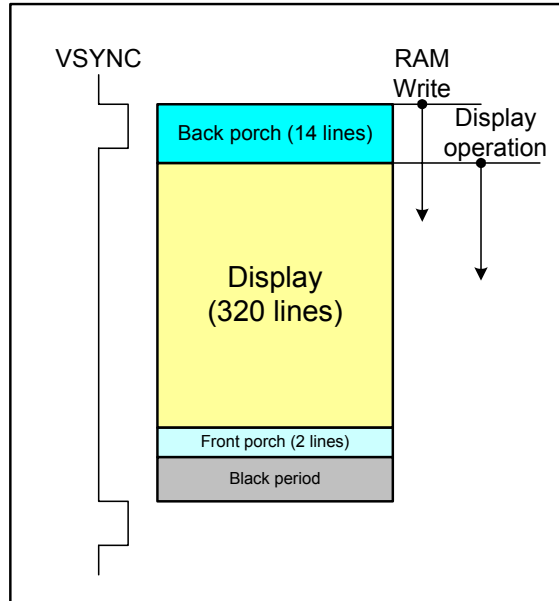
Figure11 Operation through VSYNC Interface

The VSYNC interface has the minimum speed limitation of writing data to the internal GRAM via the system interface, which are calculated from the following formula.

Internal clock frequency (fosc.) [Hz] = FrameFrequency x (DisplayLine (NL) + FrontPorch (FP) + BackPorch (BP)) x ClockCyclePerLines (RTN) x FrequencyFluctuation.

$$\text{Minimum RAM write speed (HZ)} > \frac{320 \times DisplayLines\ (NL)}{[(BackPorch(BP)+DisplayLines(NL) - margins] \times 16\ (clocks) \times 1/fosc}$$

Note: When the RAM write operation does not start from the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of minimum GRAM writing speed and internal clock frequency in VSYNC interface mode is as below.

[Example]

Display size: 240 RGB × 320 lines

Lines: 320 lines (NL = 1000111)

Back porch: 14 lines (BP = 1110)

Front porch: 2 lines (FP = 0010)

Frame frequency: 60 Hz

Frequency fluctuation: 10%

Internal oscillator clock (fosc.) [Hz] = 60 x [320+ 2 + 14] x 16 clocks x (1.1/0.9) $\fallingdotseq$ 394KHz

When calculate the internal clock frequency, the oscillator variation is needed to be taken into consideration. In the above example, the calculated internal clock frequency with ±10% margin variation is considered and ensures to complete the display operation within one VSYNC cycle. The causes of frequency variation come from fabrication process of LSI, room temperature, external resistors and VCI voltage variation.

Minimum speed for RAM writing [Hz] > 240 x 320 x 394K / [(14 + 320 − 2)lines x 16clocks] ≒ 5.7 MHz

The above theoretical value is calculated based on the premise that the ILI9320 starts to write data into the internal GRAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line and the GRAM line address where data writing operation is performed. The GRAM write speed of 5.7MHz or more will guarantee the completion of GRAM write operation before the ILI9320 starts to display the GRAM data on the screen and enable to rewrite the entire screen without flicker.

Notes in using the VSYNC interface

1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.

2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.

3. When switching from the internal clock operation mode (DM[1:0] = "00") to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.

4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode and set the AM bit to "0" to transfer display data.

System Interface Mode to VSYNC interface mode

System Interface

↓

Set HWM=1, AM=0

↓

Set GRAM Address

↓

Set DM[1:0]=10, RM=0
for VSYNC interface mode

↓

Set index register to R22h

↓

Wait more than 1 frame

↓

Write data to GRAM
through VSYNC interface

↓

**Opeartion through
VSYNC interface**

Display operation in
synchronization with
internal clocks

DM[1:0], RM become
enable after completion
of displaying 1 frame

Display operation in
synchronization with
VSYNC

VSYNC interface mode to System Interface Mode

**Opeartion through
VSYNC interface**

↓

Set DM[1:0]=00, RM=0
for system interface mode

↓

Wait more than 1 frame

↓

System Interface

Display operation in
synchronization with
VSYNC

DM[1:0], RM become
enable after completion
of displaying 1 frame

Display operation in
synchronization with
internal clocks

Note: input VSYNC for more than 1 frame
period after setting the DM, RM register.

Figure12 Transition flow between VSYNC and internal clock operation modes

7.5. RGB Input Interface

The RGB Interface mode is available for ILI9320 and the interface is selected by setting the RIM[1:0] bits as following table.

RIM1	RIM0	RGB Interface	DB pins
0	0	18-bit RGB Interface	DB[17:0]
0	1	16-bit RGB Interface	DB[17:13], DB[11:1]
1	0	6-bit RGB Interface	DB[17:12]
1	1	Setting prohibited	
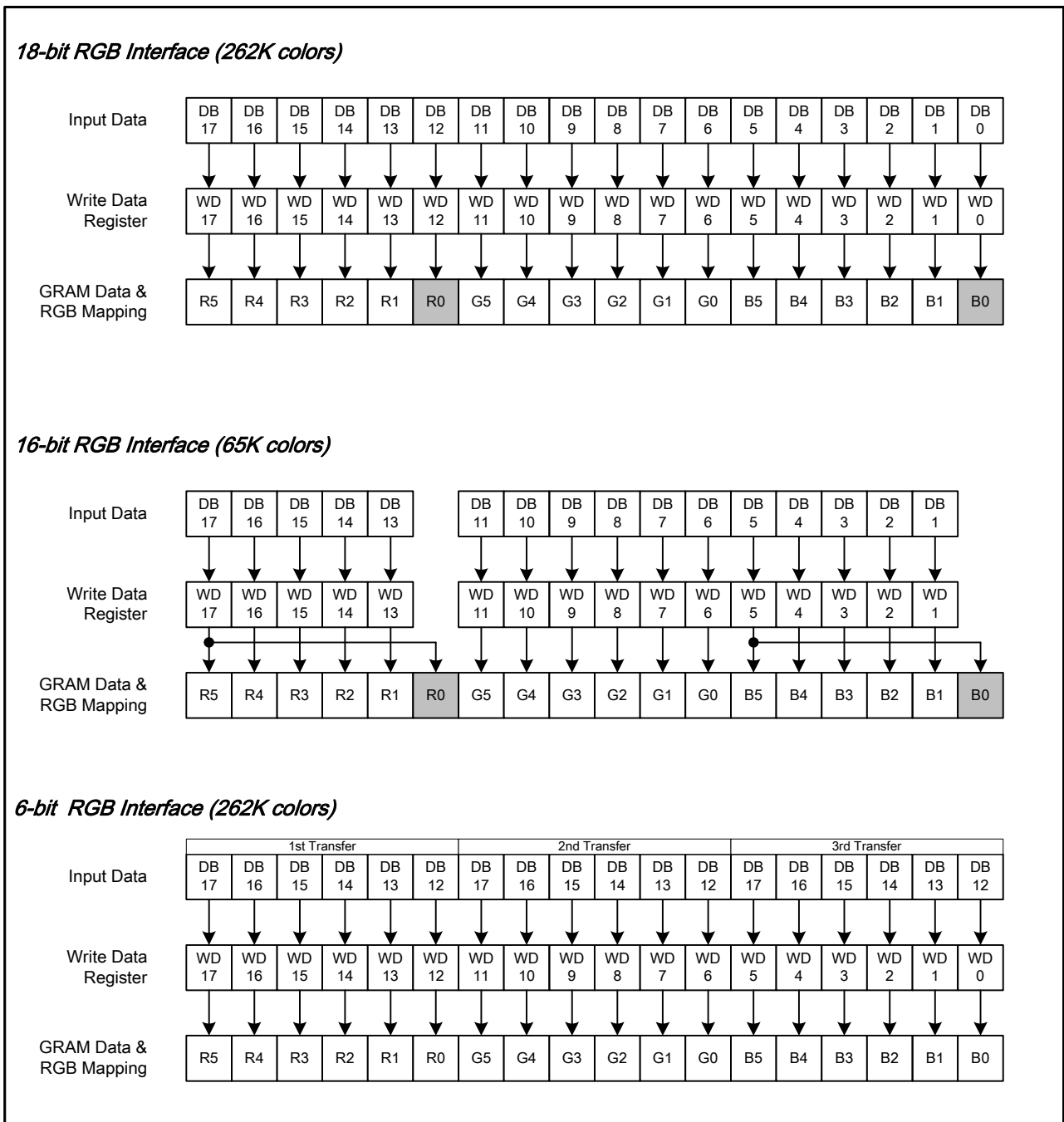
Figure13 RGB Interface Data Format

| Version: 0.51

7.5.1. RGB Interface

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The RGB interface transfers the updated data to GRAM with the high-speed write function and the update area is defined by the window address function. The back porch and front porch are used to set the RGB interface timing.
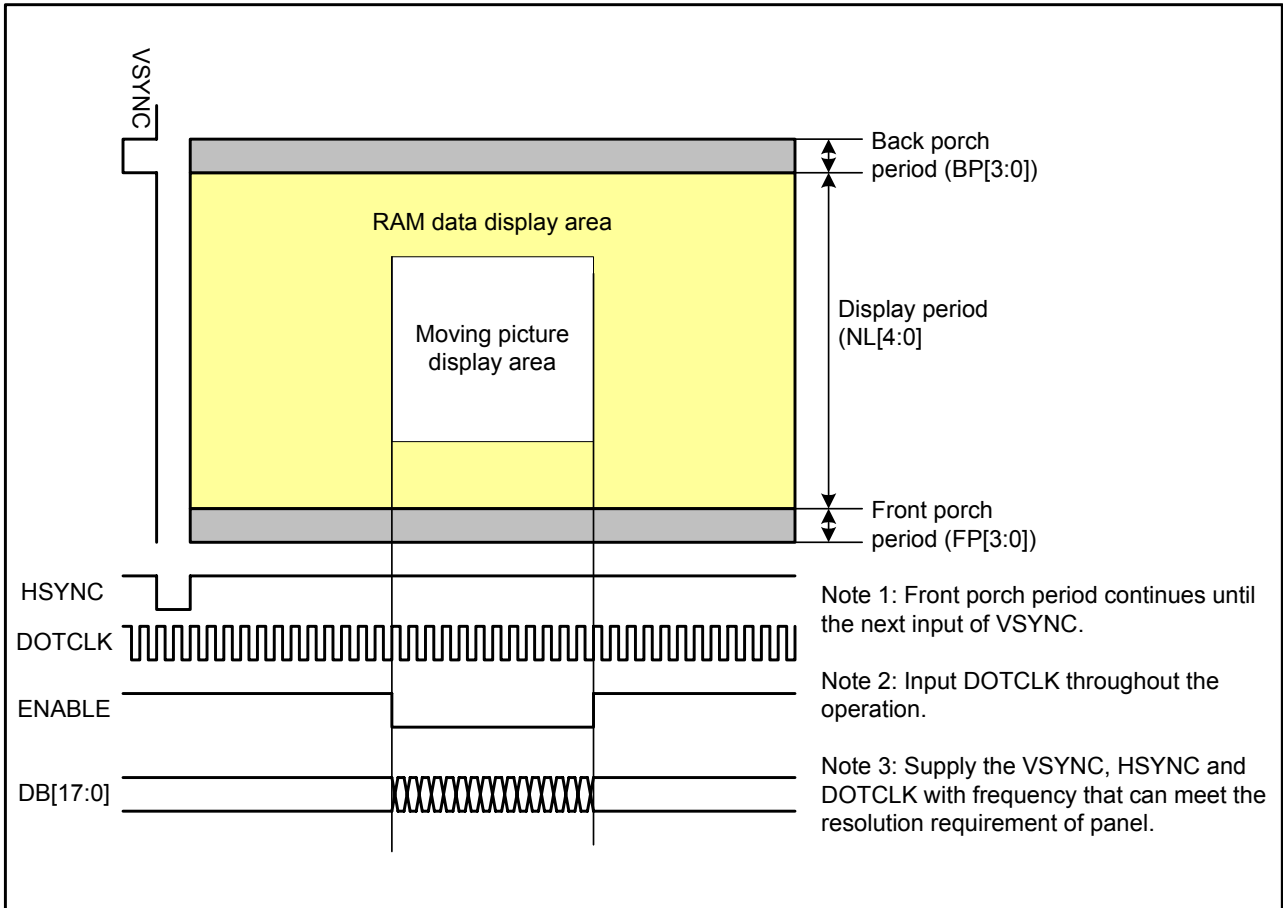
Figure14 GRAM Access Area by RGB Interface

7.5.2. RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as follows.
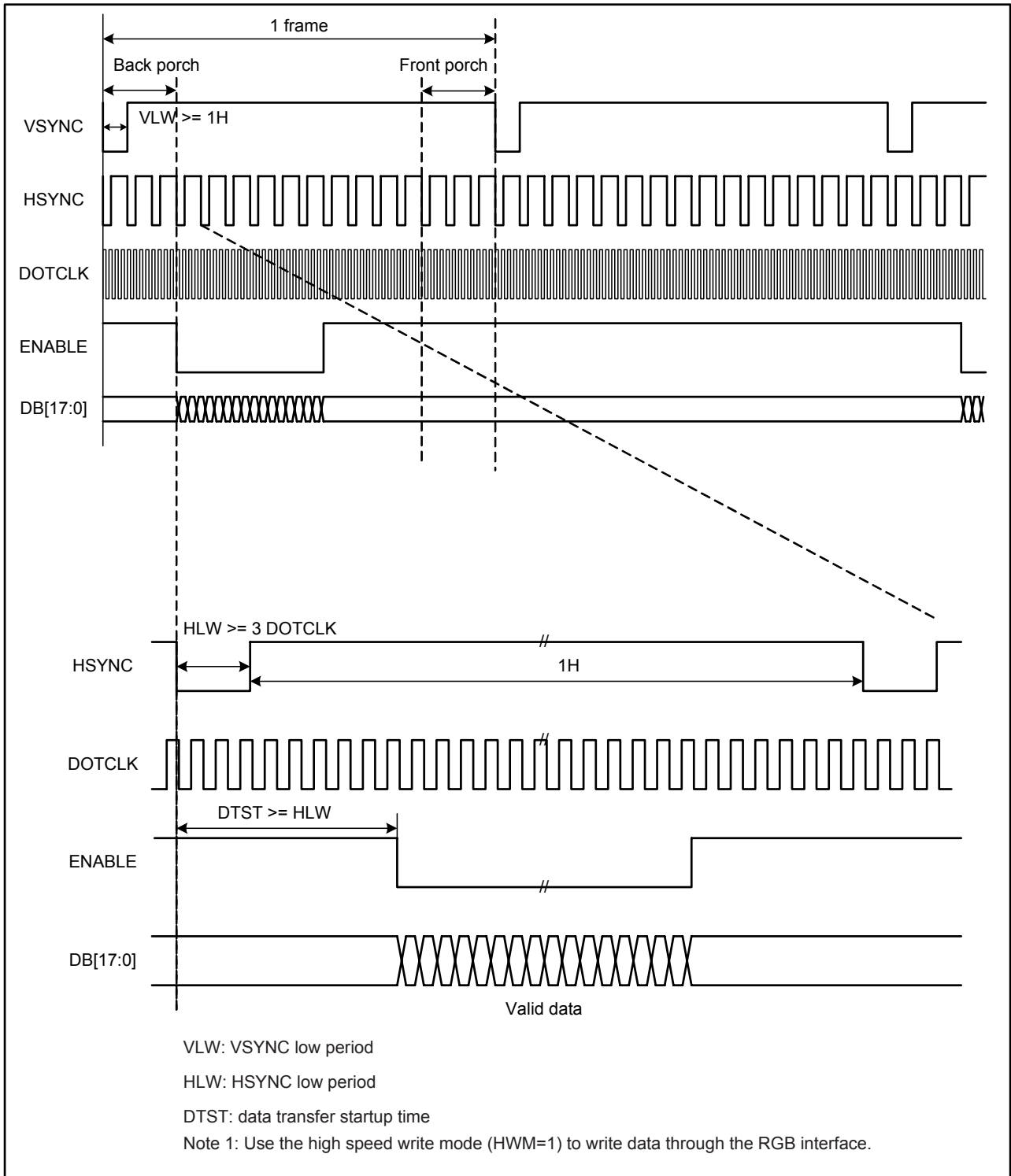
Figure15 Timing Chart of Signals in 18-/16-bit RGB Interface Mode

The timing chart of 6-bit RGB interface mode is shown as follows.

VLW: VSYNC low period

HLW: HSYNC low period

DTST: data transfer startup time

Note 1: Use the high speed write mode (HWM=1) to write data through the RGB interface.

Note 2) In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLKs.

Note 3) In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and ENABLE to 3 multiples of DOTCLKs.
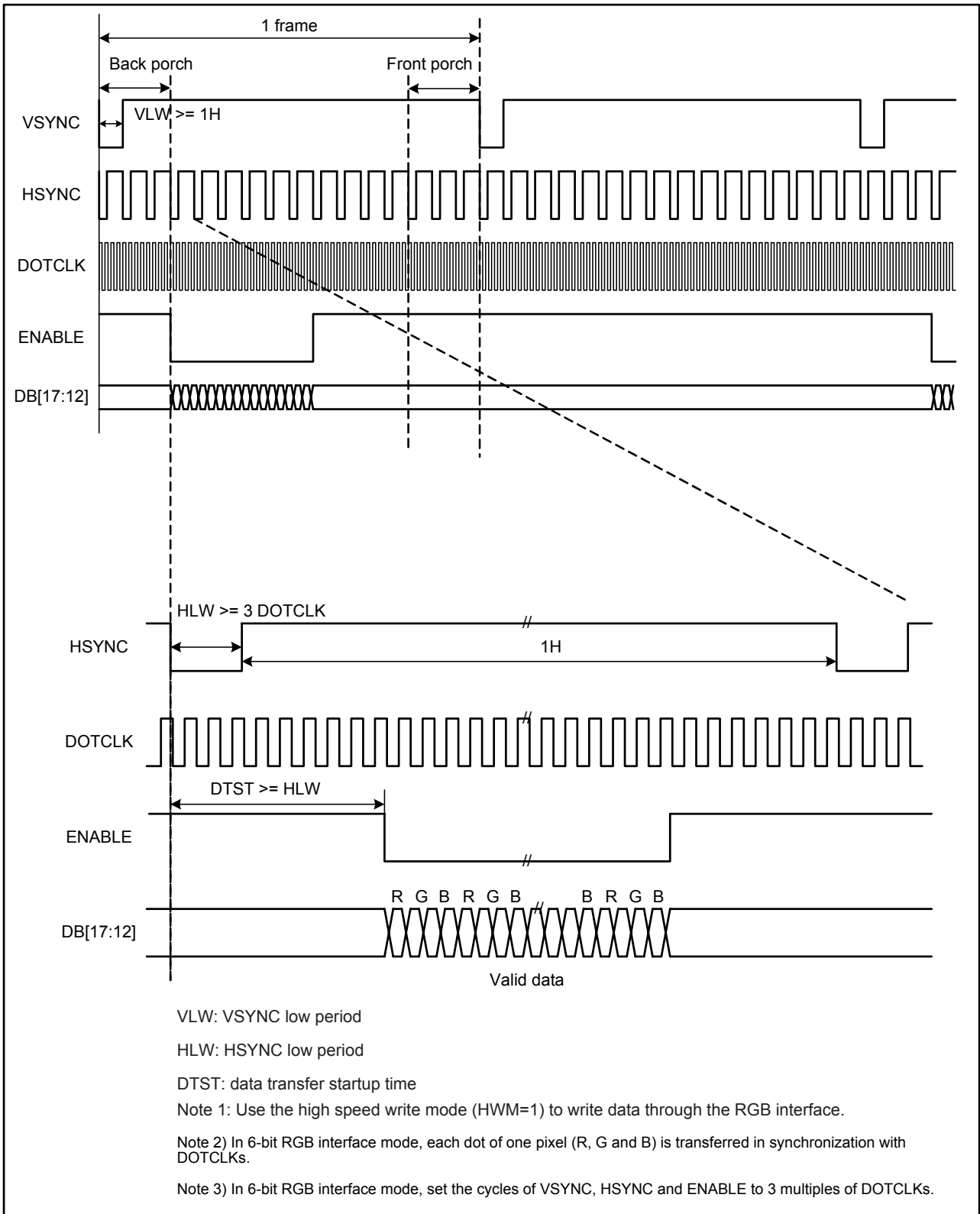
Figure16 Timing chart of signals in 6-bit RGB interface mode

7.5.3. Moving Picture Mode

ILI9320 has the RGB interface to display moving picture and incorporates GRAM to store display data, which has following merits in displaying a moving picture.

- The window address function defined the update area of GRAM.
- Only the moving picture area of GRAM is updated.
- When display the moving picture in RGB interface mode, the DB[17:0] can be switched as system interface to update still picture area and registers, such as icons.

RAM access via a system interface in RGB-I/F mode

ILI9320 allows GRAM access via the system interface in RGB interface mode. In RGB interface mode, data are written to the internal GRAM in synchronization with DOTCLK and ENABLE signals. When write data to the internal GRAM by the system interface, set ENABLE to terminate the RGB interface and switch to the system interface to update the registers (RM = "0") and the still picture of GRAM. When restart RAM access in RGB interface mode, wait one read/write cycle and then set RM = "1" and the index register to R22h to start accessing RAM via the RGB interface. If RAM accesses via two interfaces conflicts, there is no guarantee that data are written to the internal GRAM.

The following figure illustrates the operation of the ILI9320 when displaying a moving picture via the RGB interface and rewriting the still picture RAM area via the system interface.
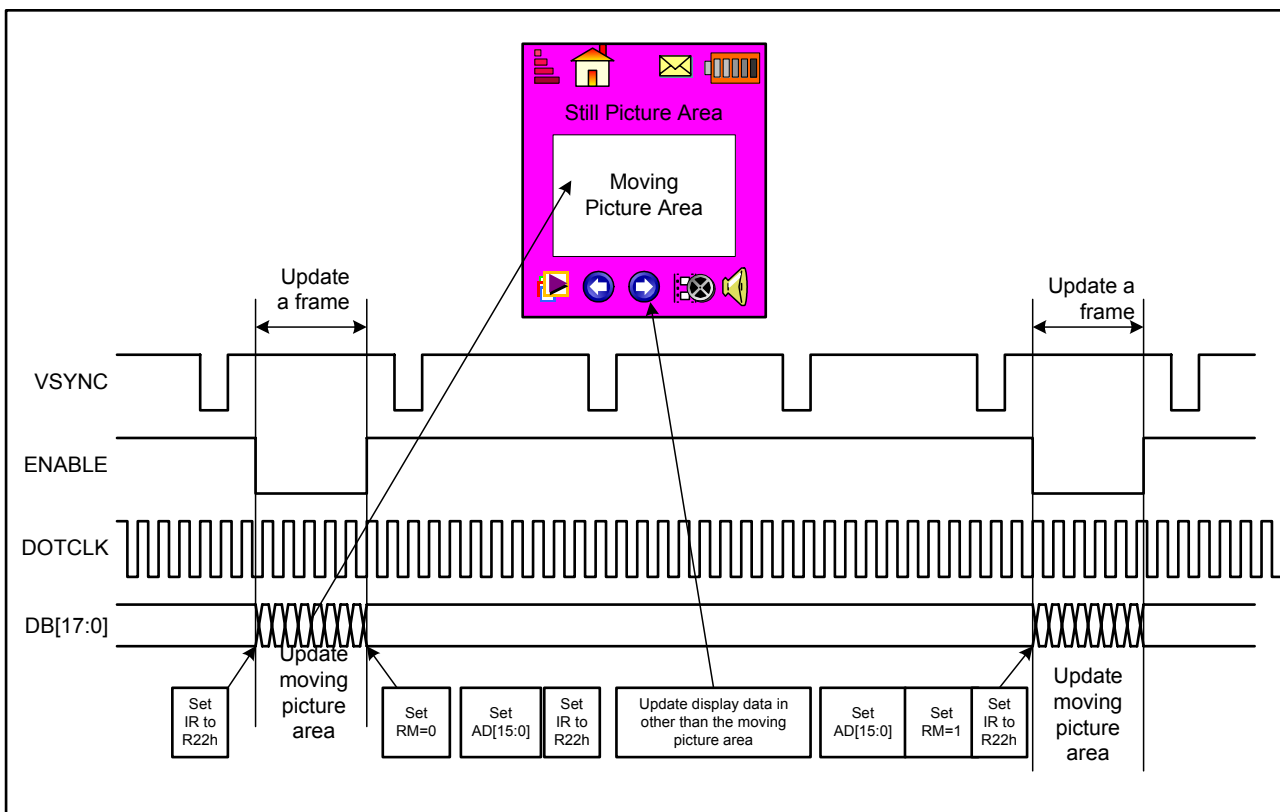
Figure17 Example of update the still and moving picture

7.5.4. 6-bit RGB Interface

The 6-bit RGB interface is selected by setting the RIM[1:0] bits to "10". The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (DB[17:12]) according to the data enable signal (ENABLE). Unused pins (DB[11:0]) must be fixed at either IOVcc or DGND level. Registers can be set by the system interface (i80/SPI).

RGB interface with 6-bit data bus

	1st Transfer						2nd Transfer						3rd Transfer					
Input Data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
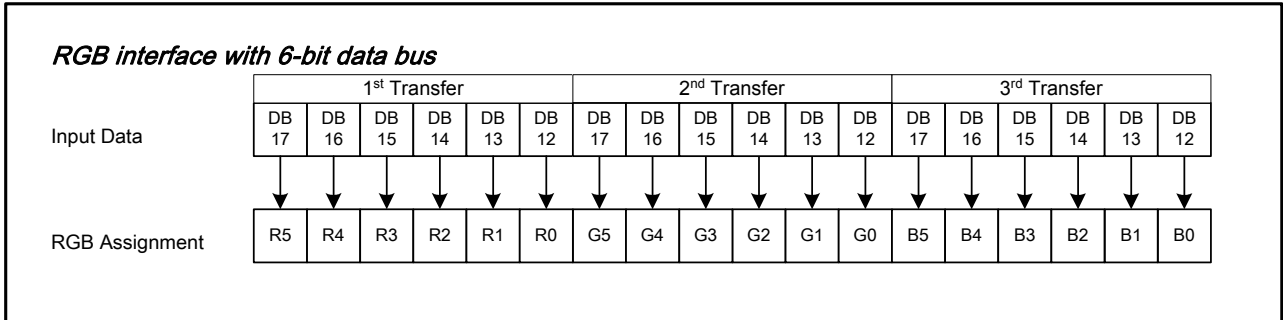
Data transfer synchronization in 6-bit RGB interface mode

ILI9320 has data transfer counters to count the first, second, third data transfers in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.

Transfer synchronization
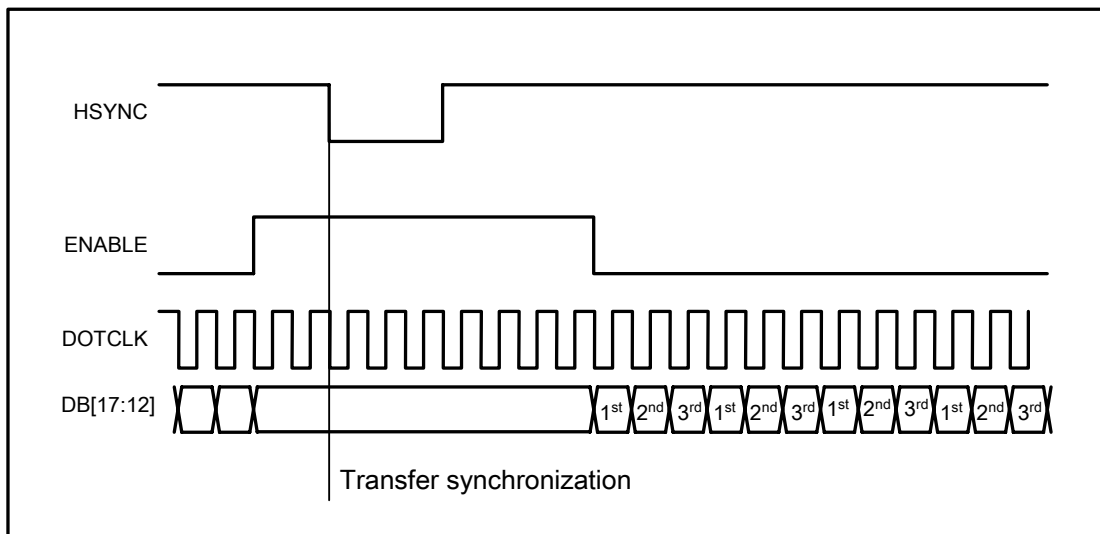
7.5.5. 16-bit RGB Interface

The 16-bit RGB interface is selected by setting the RIM[1:0] bits to "01". The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 16-bit RGB data bus (DB17-13, DB11-1) according to the data enable signal (ENABLE). Registers are set only via the system interface.

16-bit RGB Interface (65K colors)
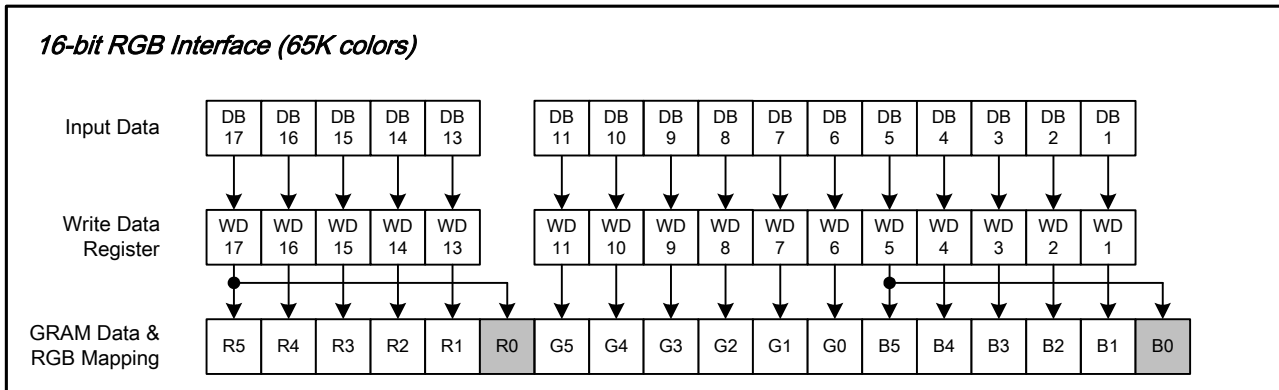
7.5.6. 18-bit RGB Interface

The 18-bit RGB interface is selected by setting the RIM[1:0] bits to "00". The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 18-bit RGB data bus (DB[17:0]) according to the data enable signal (ENABLE). Registers are set only via the system interface.

RGB interface with 18-bit data bus
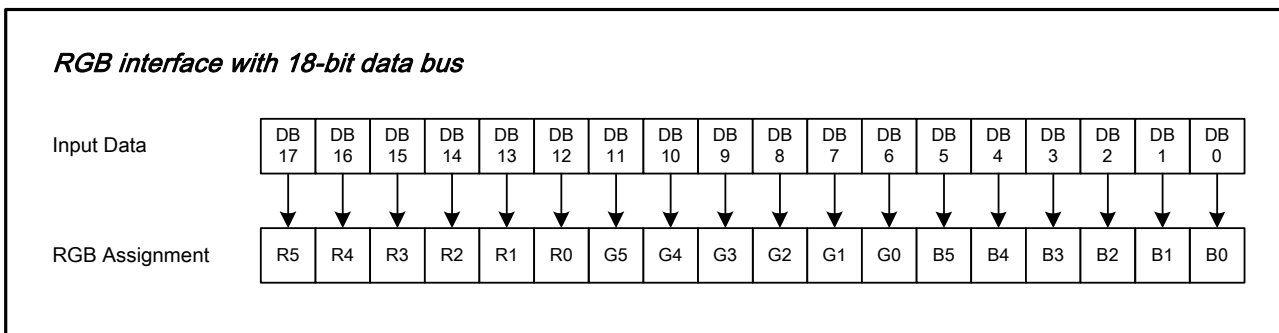
Notes in using the RGB Input Interface

1. The following are the functions not available in RGB Input Interface mode.

Function	RGB interface	I80 system interface
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation function	Not available	Available

2. VSYNC, HSYNC, and DOTCLK signals must be supplied throughout a display operation period.

3. The periods set with the NO[1:0] bits (gate output non-overlap period), STD[1:0] bits (source output delay period) and EQ[1:0] bits (equalization period) are not based on the internal clock but based on DOTCLK in

RGB interface mode.

4. In 6-bit RGB interface mode, each of RGB dots is transferred in synchronization with a DOTCLK input. In other words, it takes 3 DOTCLK inputs to transfer one pixel. Be sure to complete data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode.

5. In 6-bit RGB interface mode, data of one pixel, which consists of RGB dots, are transferred in units of 3 DOTCLK. Accordingly, set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC, ENABLE, DB[17:0]) to contain DOTCLK inputs of a multiple of 3 to complete data transfer in units of pixels.

6. When switching from the internal operation mode to the RGB Input Interface mode, or the other way around, follow the sequence below.

7. In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.

8. In RGB interface mode, a RAM address (AD[15:0]) is set in the address counter every frame on the falling edge of VSYNC.

Internal clock operation to RGB I/F

Internal clock operation

> HWM = 1, AM=0
>
> Set AD[15:0]
>
> Set RGB Interface mode
> DM[1:0]=01 and RM=1 *Note*
>
> Set IR to R22h
> (GRAM data write)
>
> Wait for more than 1 frame
>
> Write data through RGB I/F

RGB Interface Operation

Internal clock operation

* SPI interface can be used to set the registers and data

* DM[1:0] and RM become enable after completion of display 1 frame

RGB Interface (Display operation in synchronization with VSYNC, HSYNC, DOTCLK)

RGB I/F to Internal clock operation

RGB Interface Operation

> Set Internal Clock Operation mode
> DM[1:0]=00 and RM=0
>
> Wait for more than 1 frame

Internal clock operation

RGB Interface (Display operation in synchronization with VSYNC, HSYNC, DOTCLK)

* DM[1:0] and RM become enable after completion of display 1 frame

Display operation in synchronization with internal clock

Note: Input RGB Interface signals (VSYNC, HSYNC, DOTCLK) before setting DM[1;0] and RM to the RGB interface mode

Figure18 Internal clock operation/RGB interface mode switching

Write data through RGB
interface to write data
through system interface

RGB Interface operation

Set DM[1:0]=01, RM=0
with RGB interface mode

↓

HWM=1/0

↓

Set AD[15;0]

↓

Set IR to R22h
(GRAM data write)

↓

Write data to GRAM
through system interface

↓

System Interface operation

Write data through system
interface to write data
through RGB interface

System Interface operation

Write data to GRAM
through system interface

↓

HWM=1/0

↓

Set AD[15;0]

↓

Set DM[1:0]=01, RM=1
with RGB interface mode

↓

Set IR to R22h
(GRAM data write)

↓

RGB Interface operation

Figure19 GRAM access between system interface and RGB interface

7.6. Interface Timing

The following are diagrams of interfacing timing with LCD panel control signals in internal operation and RGB interface modes.
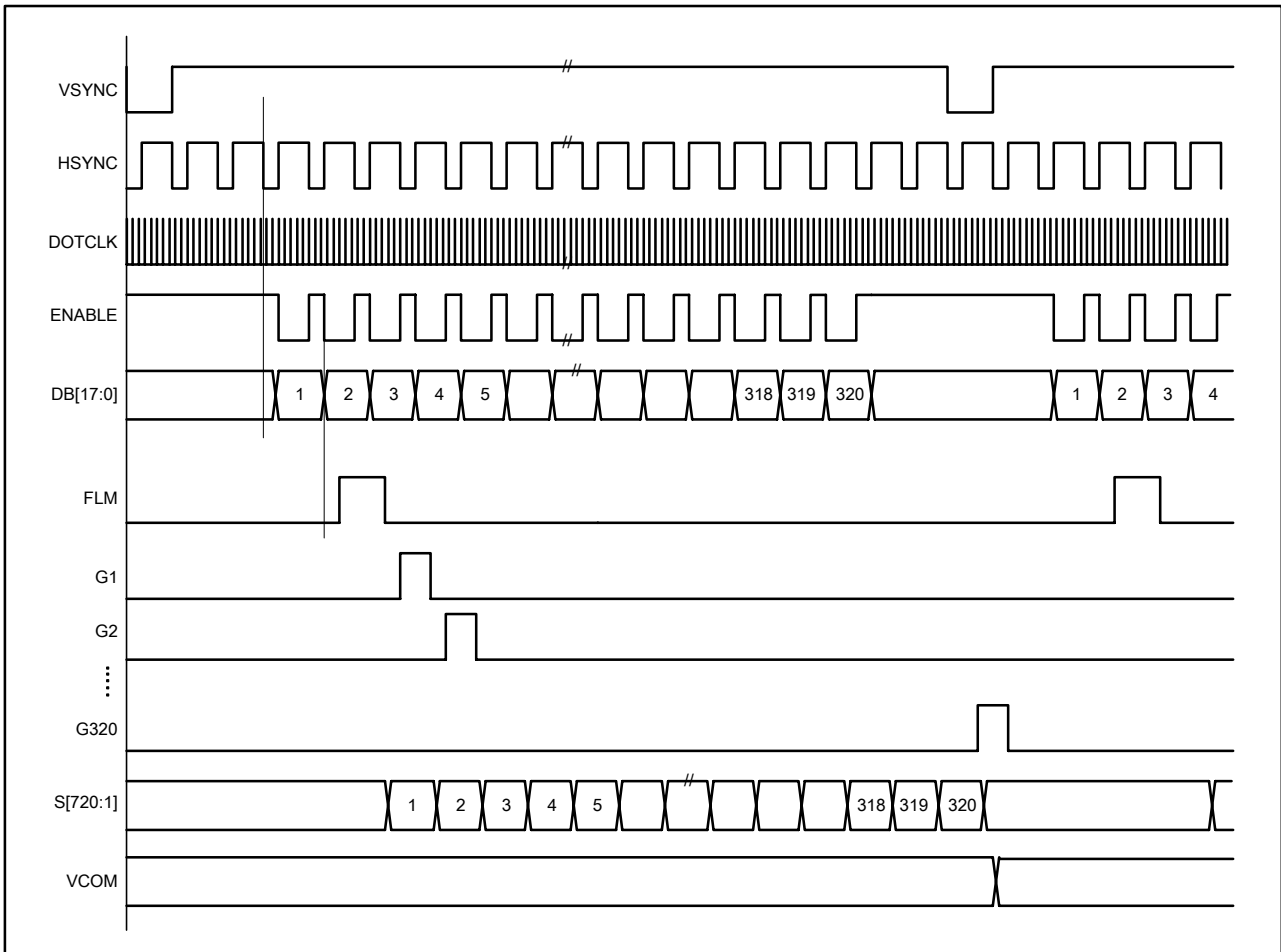
Figure20 Relationship between RGB I/F signals and LCD Driving Signals for Panel

8. Register Descriptions

8.1. Registers Access

ILI9320 adopts 18-bit bus interface architecture for high-performance microprocessor. All the functional blocks of ILI9320 starts to work after receiving the correct instruction from the external microprocessor by the 18-, 16-, 9-, 8-bit interface. The index register (IR) stores the register address to which the instructions and display data will be written. The register selection signal (RS), the read/write signals (nRD/nWR) and data bus D17-0 are used to read/write the instructions and data of ILI9320. The registers of the ILI9320 are categorized into the following groups.

1. Specify the index of register (IR)

2. Read a status

3. Display control

4. Power management Control

5. Graphics data processing

6. Set internal GRAM address (AC)

7. Transfer data to/from the internal GRAM (R22)

8. Internal grayscale γ-correction (R30 ~ R39)

Normally, the display data (GRAM) is most often updated, and in order since the ILI9320 can update internal GRAM address automatically as it writes data to the internal GRAM and minimize data transfer by using the window address function, there are fewer loads on the program in the microprocessor. As the following figure shows, the way of assigning data to the 16 register bits (D[15:0]) varies for each interface. Send registers in accordance with the following data transfer format.
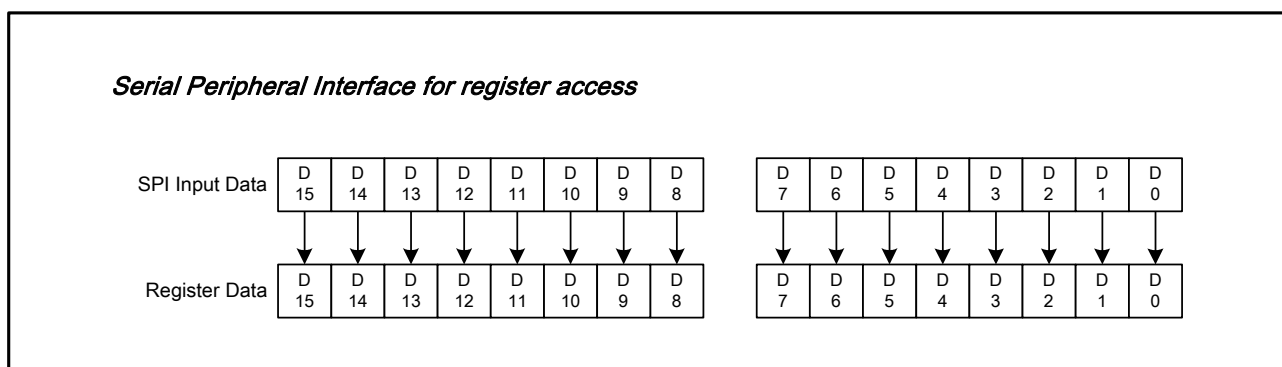
Figure21 Register Setting with Serial Peripheral Interface (SPI)

i80/M68 system 18-bit data bus interface

Data Bus (DB[17:0])	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Register Bit (D[15:0])	D15	D14	D13	D12	D11	D10	D9	D8		D7	D6	D5	D4	D3	D2	D1	D0	

i80/M68 system 16-bit data bus interface

Data Bus (DB[17:10]), (DB[8:1])	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1
Register Bit (D[15:0])	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

i80/M68 system 9-bit data bus interface

Data Bus (DB[17:9])	1st Transfer									2nd Transfer								
	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9
Register Bit (D[15:0])	D15	D14	D13	D12	D11	D10	D9	D8		D7	D6	D5	D4	D3	D2	D1	D0	

i80/M68 system 8-bit data bus interface/Serial peripheral interface (2/3 transmission)

Data Bus (DB[17:10])	1st Transfer								2nd Transfer							
	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10
Register Bit (D[15:0])	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
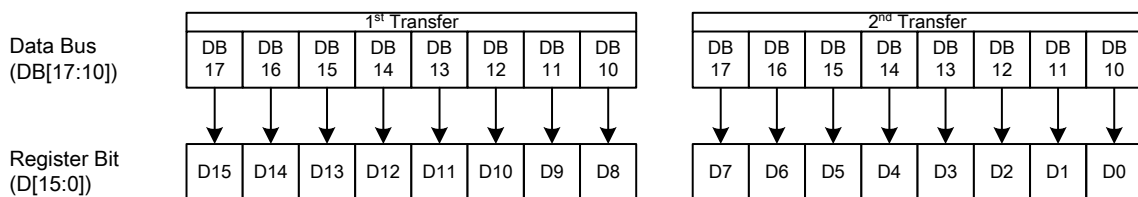
Figure22 Register setting with i80 System Interface

i80 18-/16-bit System Bus Interface Timing

(a) Write to register

nCS

RS

nRD

nWR

DB[17:0]   Write register "index"   Write register "data"

(b) Read from register

nCS

RS

nRD

nWR

DB[17:0]   Write register "index"   Read register "data"

i80 9-/8-bit System Bus Interface Timing

(a) Write to register

nCS

RS

nRD

nWR

DB[17:10]   "00h"   Write register "index"   Write register "high byte data"   Write register "low byte data"

(b) Read from register

nCS

RS

nRD

nWR

DB[17:10]   "00h"   Write register "index"   Read register "high byte data"   Read register "low byte data"

Figure 23 Register Read/Write Timing of i80 System Interface

8.2. Instruction Descriptions

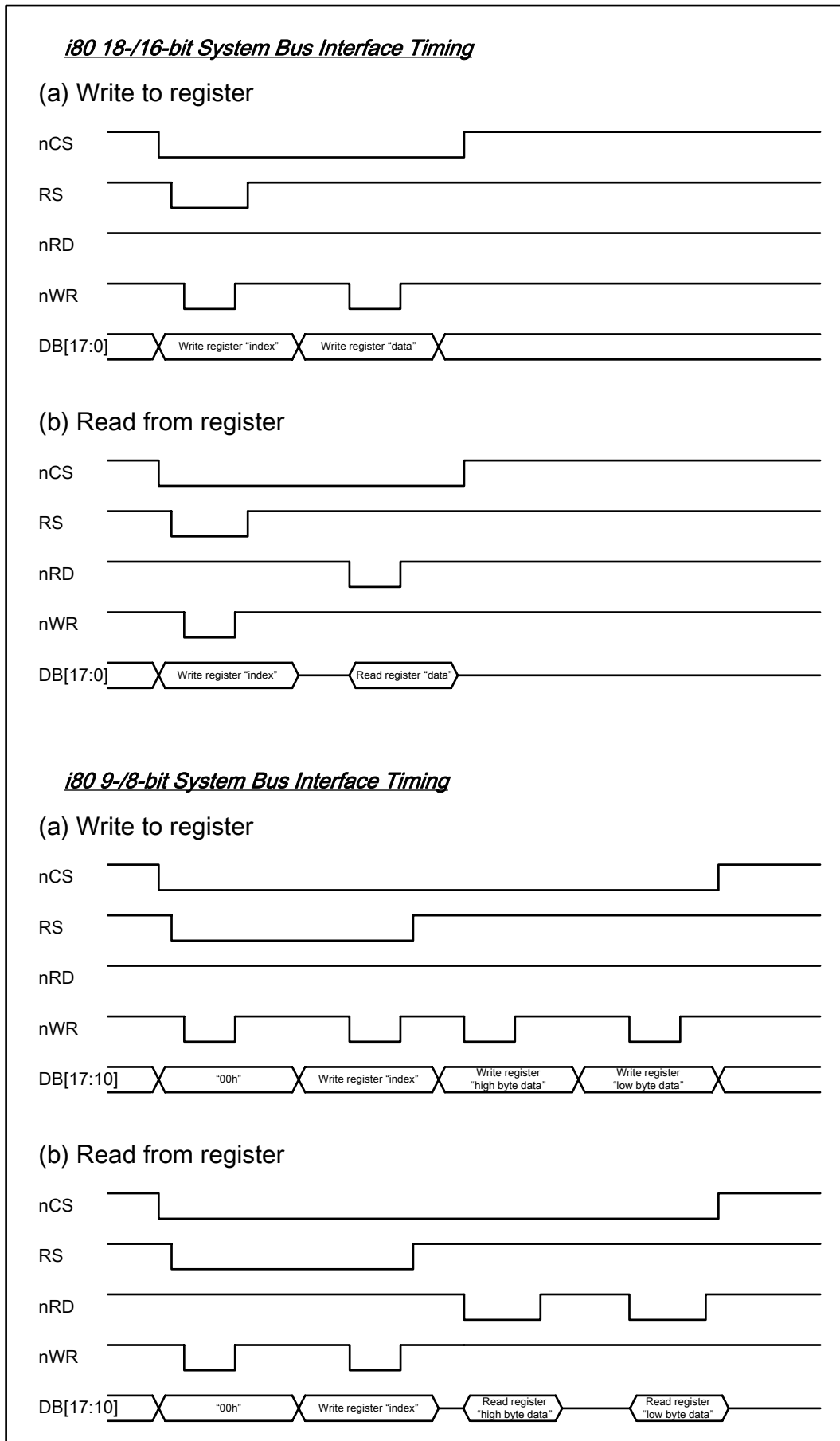| No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	Index Register	W	0	-	-	-	-	-	-	-	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
SR	Status Read	R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
00h	Driver Code Read	R	1	1	0	0	1	0	0	1	0	0	0	1	0	0	0	1	0
00h	Start Oscillation	W	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	OSC
01h	Driver Output Control 1	W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
02h	LCD Driving Control	W	1	0	0	0	0	0	1	B/C	EOR	0	0	0	0	0	0	0	0
03h	Entry Mode	W	1	TRI	DFM	0	BGR	0	0	HWM	0	ORG	0	I/D1	I/D0	AM	0	0	0
04h	Resize Control	W	1	0	0	0	0	0	0	RCV1	RCV0	0	0	RCH1	RCH0	0	0	RSZ1	RSZ0
07h	Display Control 1	W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0
08h	Display Control 2	W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
09h	Display Control 3	W	1	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
0Ah	Display Control 4	W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0
0Ch	RGB Display Interface Control 1	W	1	ENC2	ENC1	ENC0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
0Dh	Frame Maker Position	W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
0Fh	RGB Display Interface Control 2	W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
10h	Power Control 1	W	1	0	0	0	SAP	BT3	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	DSTB	SLP	0
11h	Power Control 2	W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
12h	Power Control 3	W	1	0	0	0	0	0	0	0	VCMR	0	0	0	PON	VRH3	VRH2	VRH1	VRH0
13h	Power Control 4	W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
20h	Horizontal GRAM Address Set	W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
21h	Vertical GRAM Address Set	W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
22h	Write Data to GRAM	W	1	RAM write data (WD17-0) / read data (RD17-0) bits are transferred via different data bus lines according to the selected interfaces.																
29h	Power Control 7	W	1	0	0	0	0	0	0	0	0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0
2Bh	Frame Rate and Color Control	W	1	0	0	0	0	0	0	0	0	EXT_R	0	FR_SEL1	FR_SEL0	0	0	0	0
30h	Gamma Control 1	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
31h	Gamma Control 2	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
32h	Gamma Control 3	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
35h	Gamma Control 4	W	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
36h	Gamma Control 5	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	VRP0[4]	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
37h	Gamma Control 6	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
38h	Gamma Control 7	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
39h	Gamma Control 8	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
3Ch	Gamma Control 9	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]

No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
3Dh	Gamma Control 10	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	VRN0[4]	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]
50h	Horizontal Address Start Position	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
51h	Horizontal Address End Position	W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
52h	Vertical Address Start Position	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
53h	Vertical Address End Position	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
60h	Driver Output Control 2	W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
61h	Base Image Display Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
6Ah	Vertical Scroll Control	W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
80h	Partial Image 1 Display Position	W	1	0	0	0	0	0	0	0	PTDP08	PTDP07	PTDP06	PTDP05	PTDP04	PTDP03	PTDP02	PTDP01	PTDP00
81h	Partial Image 1 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA08	PTSA07	PTSA06	PTSA05	PTSA04	PTSA03	PTSA02	PTSA01	PTSA00
82h	Partial Image 1 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA08	PTEA07	PTEA06	PTEA05	PTEA04	PTEA03	PTEA02	PTEA01	PTEA00
83h	Partial Image 2 Display Position	W	1	0	0	0	0	0	0	0	PTDP18	PTDP17	PTDP16	PTDP15	PTDP14	PTDP13	PTDP12	PTDP11	PTDP10
84h	Partial Image 2 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA18	PTSA17	PTSA16	PTSA15	PTSA14	PTSA13	PTSA12	PTSA11	PTSA10
85h	Partial Image 2 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA18	PTEA17	PTEA16	PTEA15	PTEA14	PTEA13	PTEA12	PTEA11	PTEA10
90h	Panel Interface Control 1	W	1	0	0	0	0	0	0	DIVI1	DIVI00	0	0	0	0	RTNI3	RTNI2	RTNI1	RTNI0
92h	Panel Interface Control 2	W	1	0	0	0	0	0	NOWI2	NOWI1	NOWI0	0	0	0	0	0	0	0	0
93h	Panel Interface Control 3	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPI2	MCPI1	MCPI0
95h	Panel Interface Control 4	W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0
97h	Panel Interface Control 5	W	1	0	0	0	0	NOWE3	NOWE2	NOWE1	NOWE0	0	0	0	0	0	0	0	0
98h	Panel Interface Control 6	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPE2	MCPE1	MCPE0

8.2.1. Index (IR)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	0	-	-	-	-	-	-	-	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the address of register (R00h ~ RFFh) or RAM which will be accessed.

8.2.2. Status Read (RS)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

The SR bits represent the internal status of the ILI9320.

L[7:0] Indicates the position of driving line which is driving the TFT panel currently.

8.2.3. Start Oscillation (R00h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	OSC
R	1	1	0	0	1	0	0	1	1	0	0	1	0	0	0	0	0

Set the OSC bit as '1' to start the internal oscillator and as '0' to stop the oscillator. Wait at least 10ms to let the frequency of oscillator stable and then do the other function setting. The device code "9320"h is read out when read this register.

8.2.4. Driver Output Control (R01h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0

SS: Select the shift direction of outputs from the source driver.

When SS = 0, the shift direction of outputs is from S1 to S720

When SS = 1, the shift direction of outputs is from S720 to S1.

In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, B dots to the source driver pins.

To assign R, G, B dots to the source driver pins from S1 to S720, set SS = 0.

To assign R, G, B dots to the source driver pins from S720 to S1, set SS = 1.

When changing SS or BGR bits, RAM data must be rewritten.

SM: Sets the gate driver pin arrangement in combination with the GS bit (R60h) to select the optimal scan mode for the module.

SM	GS	Scan Direction	Gate Output Sequence
0	0	G1 G2 G3 G4 / Odd-number / TFT Panel / Even-number / G1 to G319 / G2 to G320 / G317 G318 G319 G320 / ILI9320	G1, G2, G3, G4, …,G316 G317, G318, G319, G320
0	1	G1 G2 G3 G4 / Odd-number / TFT Panel / Even-number / G319 to G1 / G320 to G2 / G317 G318 G319 G320 / ILI9320	G320, G319, G318, …, G6, G5, G4, G3, G2, G1
1	0	Odd-number / G1 G2 / TFT Panel / G319 / G1 to G319 / G2 / Even-number / G2 to G320 / G320 / ILI9320	G1, G3, G5, G7, …,G311 G313, G315, G317, G319 G2, G4, G6, G8, …,G312 G314, G316, G318, G320
1	1	Odd-number / G1 G2 / TFT Panel / G319 / G319 to G1 / G2 / Even-number / G320 to G2 / G320 / ILI9320	G320, G318, G316, …, G10, G8, G6, G4, G2 G319, G317, G315, …, G9, G78, G5, G3, G1

8.2.5. LCD Driving Wave Control (R02h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	1	B/C	EOR	0	0	0	0	0	0	0	0

.**B/C**   0 : Frame/Field inversion

1 : Line inversion

EOR: EOR = 1 and B/C=1 to set the line inversion.

8.2.6. Entry Mode (R03h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	TRI	DFM	0	BGR	0	0	HWM	0	ORG	0	I/D1	I/D0	AM	0	0	0

AM Control the GRAM update direction.

When AM = "0", the address is updated in horizontal writing direction.

When AM = "1", the address is updated in vertical writing direction.

When a window area is set by registers R50h,R51h, R52h and R53h, only the addressed GRAM area is updated based on I/D[1:0] and AM bits setting.

I/D[1:0] Control the address counter (AC) to automatically increase or decrease by 1 when update one pixel display data. Refer to the following figure for the details.
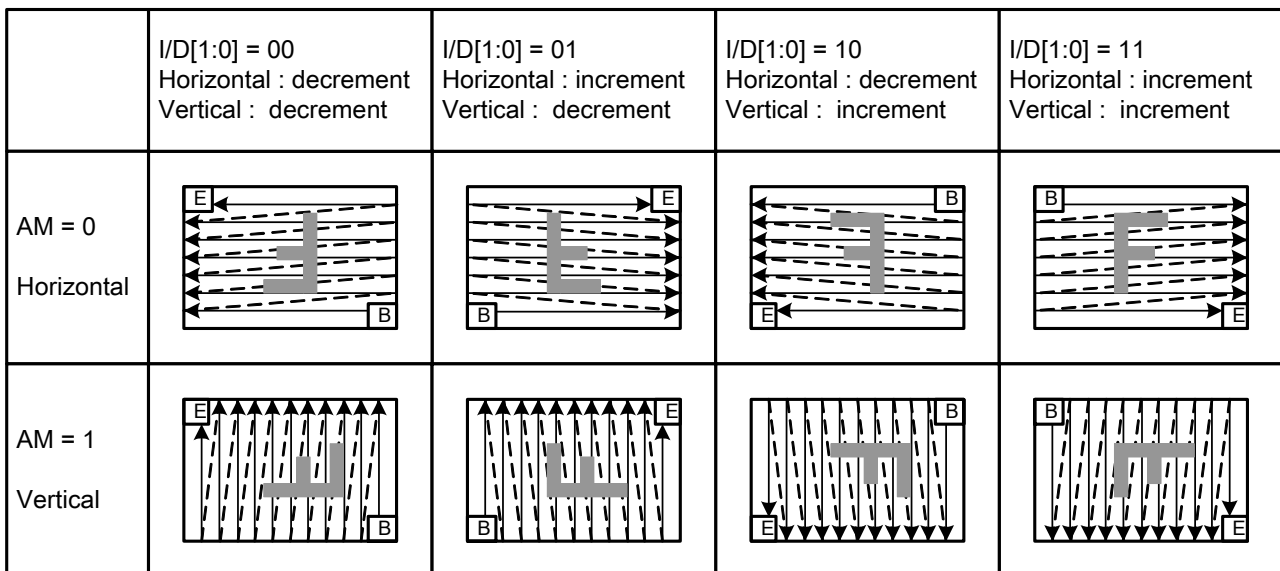
Figure24 GRAM Access Direction Setting

ORG   Moves the origin address according to the I/D[1:0] setting when a window address area is made. This function is enabled when writing data with the window address area using high-speed RAM write.

ORG = "0": The origin address is not moved. In this case, specify the address to start write operation according to the GRAM address map within the window address area.

ORG = "1": The original address "00000h" moves according to the I/D[1:0] setting.

Notes: 1. When ORG=1, only the origin address address"00000h" can be set in the RAM address set registers R20h, and R21h.

2. In RAM read operation, make sure to set ORG=0.

HWM GRAM high speed write function.

HWM="0": High speed write function disabled..

HWM="1": High speed write function enabled..

BGR Swap the R and B order of written data.

BGR="0": Follow the RGB order to write the pixel data.

BGR="1": Swap the RGB data to BGR in writing into GRAM.

TRI When TRI = "1", data are transferred to the internal RAM in 8-bit x 3 transfers mode via the 8-bit interface. It is also possible to send data via the 16-bit interface or SPI in the transfer mode that realizes display in 262k colors in combination with DFM bits. When not using these interface modes, be sure to set TRI = "0".

DFM Set the mode of transferring data to the internal RAM when TRI = "1". See the following figures for details.
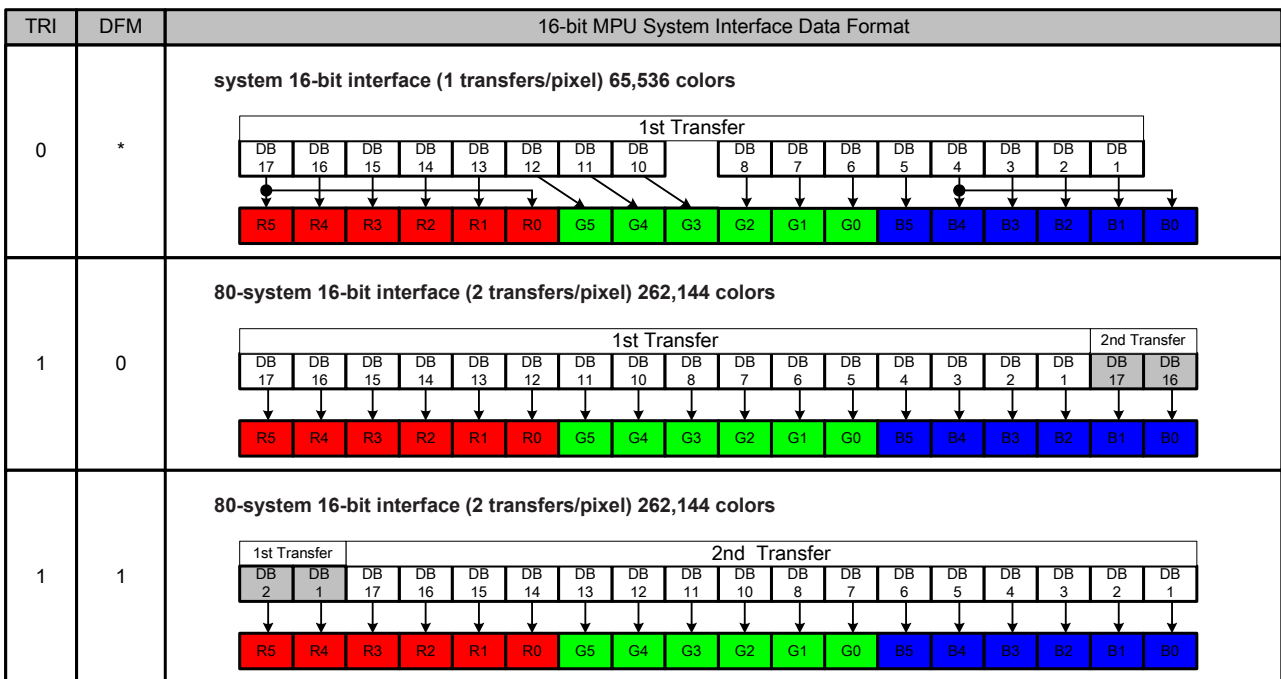
Figure25 16-bit MPU System Interface Data Format
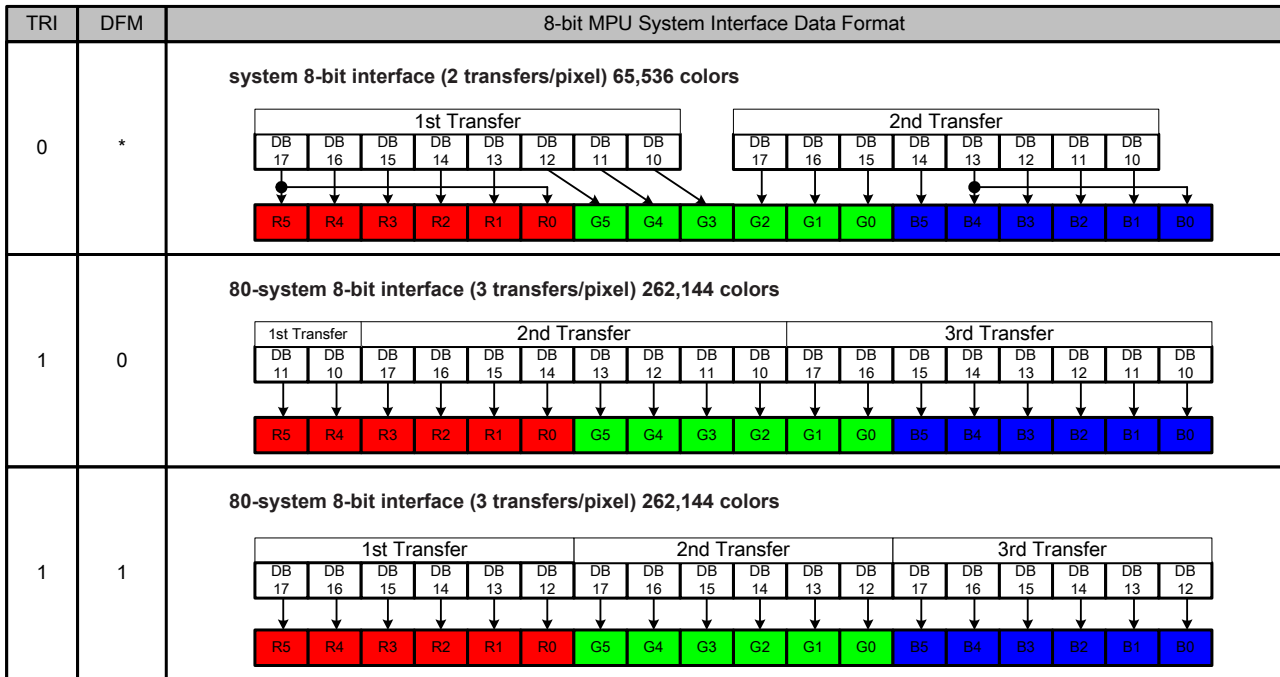
Figure26 8-bit MPU System Interface Data Format

8.2.7. Resizing Control Register (R04h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	RCV1	RCV0	0	0	RCH1	RCH0	0	0	RSZ1	RSZ0

RSZ[1:0] Sets the resizing factor.

When the RSZ bits are set for resizing, the ILI9320 writes the data according to the resizing factor so that the original image is displayed in horizontal and vertical dimensions, which are contracted according to the factor respectively. See "Resizing function".

RCH[1:0] Sets the number of remainder pixels in horizontal direction when resizing a picture.

By specifying the number of remainder pixels by RCH bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCH = 2'h0 when not using the resizing function (RSZ = 2'h0) or there are no remainder pixels.

RCV[1:0] Sets the number of remainder pixels in vertical direction when resizing a picture.

By specifying the number of remainder pixels by RCV bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCV = 2'h0 when not using the resizing function (RSZ = 2'h0) or there are no remainder pixels.

RSZ[1:0]	Resizing factor
00	No resizing (x1)
01	x 1/2
10	Setting prohibited
11	x 1/4

RCH[1:0]	Number of remainder Pixels in Horizontal Direction
00	0 pixel*

01	1 pixel
10	2 pixel
11	3 pixel

RCV[1:0]	Number of remainder Pixels in Vertical Direction
00	0 pixel*
01	1 pixel
10	2 pixel
11	3 pixel

*1 pixel = 1RGB

8.2.8. Display Control 1 (R07h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0

D[1:0] Set D[1:0]="11" to turn on the display panel, and D[1:0]="00" to turn off the display panel.

A graphics display is turned on the panel when writing D1 = "1", and is turned off when writing D1 = "0".

When writing D1 = "0", the graphics display data is retained in the internal GRAM and the ILI9320 displays the data when writing D1 = "1". When D1 = "0", i.e. while no display is shown on the panel, all source outputs becomes the GND level to reduce charging/discharging current, which is generated within the LCD while driving liquid crystal with AC voltage.

When the display is turned off by setting D[1:0] = "01", the ILI9320 continues internal display operation.   When the display is turned off by setting D[1:0] = "00", the ILI9320 internal display operation is halted completely. In combination with the GON, DTE setting, the D[1:0] setting controls display ON/OFF.

D1	D0	BASEE	Source, VCOM Output	ILI9320 internal operation
0	0	0	GND	Halt
0	1	1	GND	Operate
1	0	0	Non-lit display	Operate
1	1	0	Non-lit display	Operate
1	**1**	**1**	**Base image display**	**Operate**

Note: 1. data write operation from the microcontroller is performed irrespective of the setting of D[1:0] bits.

2. The internal state of the ILI9320 in standby mode become the same as when D[1:0] = "00". This does not mean the D[1:0] setting is changed when setting the standby mode.

3. The D[1:0] setting is valid on both 1st and 2nd displays.

4. The non-lit display level from the source output pins is determined by instruction (PTS).

CL When CL = "1", the 8-color display mode is selected.

CL	Colors
0	262,144
1	8

GON and DTE Set the output level of gate driver G1 ~ G320 as follows

GON	DTE	G1 ~G320 Gate Output
0	0	VGH
0	1	VGH
1	0	VGL
1	**1**	**Normal Display**

BASEE

Base image display enable bit. When BASEE = "0", no base image is displayed. The ILI9320 drives liquid crystal at non-lit display level or displays only partial images. When BASEE = "1", the base image is displayed. The D[1:0] setting has higher priority over the BASEE setting.

PTDE[1:0]

Partial image 2 and Partial image 1 enable bits

PTDE1/0 = 0: turns off partial image. Only base image is displayed.

PTDE1/0 = 1: turns on partial image. Set the base image display enable bit to 0 (BASEE = 0).

8.2.9. Display Control 2 (R08h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0

FP[3:0]/BP[3:0]

The FP[3:0] and BP[3:0] bits specify the line number of front and back porch periods respectively.

When setting the FP[3:0] and BP[3:0] value, the following conditions shall be met:

BP + FP ≤ 16 lines

FP ≥ 2 lines

BP ≥ 2 lines

Set the BP[3:0] and FP[3:0] bits as below for each operation modes

Operation Mode	BP	FP	BP+FP
I80 System Interface Operation Mode	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
RGB interface Operation	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
VSYNC interface Operation	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP = 16 lines

FP[3:0]	Number of lines for Front Porch
BP[3:0]	**Number of lines for Back Porch**
0000	Setting Prohibited
0001	Setting Prohibited
0010	2 lines
0011	3 lines
0100	4 lines
0101	5 lines
0110	6 lines
0111	7 lines
1000	8 lines
1001	9 lines
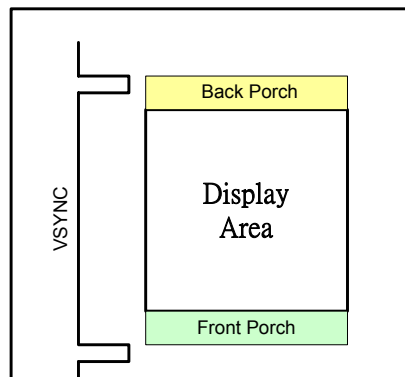
1010	10 lines
1011	11 lines
1100	12 lines
1101	13 lines
1110	14 lines
1111	Setting Prohibited

8.2.10. Display Control 3 (R09h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0

ISC[3:0]: Specify the scan cycle interval of gate driver in non-display area when PTG[1:0]="10" to select interval scan. Then scan cycle is set as odd number from 0~31 frame periods. The polarity is inverted every scan cycle.

ISC3	ISC3	ISC3	ISC3	Scan Cycle	f_{FLM}=60 Hz
0	0	0	0	0 frame	-
0	0	0	1	3 frame	50ms
0	0	1	0	5 frame	84ms
0	0	1	1	7 frame	117ms
0	1	0	0	9 frame	150ms
0	1	0	1	11 frame	184ms
0	1	1	0	13 frame	217ms
0	1	1	1	15 frame	251ms
1	0	0	0	17 frame	284ms
1	0	0	1	19 frame	317ms
1	0	1	0	21 frame	351ms
1	0	1	1	23 frame	384ms
1	1	0	0	25 frame	418ms
1	1	0	1	27 frame	451ms
1	1	1	0	29 frame	484ms
1	1	1	1	31 frame	518ms

PTG[1:0] Set the scan mode in non-display area.

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	Vcom output
0	**0**	**Normal scan**	Set with the PTS[2:0] bits	VcomH/VcomL
0	1	Setting Disabled	-	-
1	0	Interval scan	Set with the PTS[2:0] bits	VcomH/VcomL
1	1	Setting Disabled	-	-

PTS[2:0]

Set the source output level in non-display area drive period (front/back porch period and blank area between partial displays).

When PTS[2] = 1, the operation of amplifiers which generates the grayscales other than V0 and V63 are halted and the step-up clock frequency becomes half the normal frequency in non-display drive period in order to reduce power consumption.

PTS[2:0]	Source output level	Grayscale amplifier	Step-up clock frequency

	Positive polarity	Negative polarity	in operation	
000	V63	V0	V63 to V0	Register Setting(DC1, DC0)
001	Setting Prohibited	Setting Prohibited	-	-
010	GND	GND	V63 to V0	Register Setting(DC1, DC0)
011	Hi-Z	Hi-Z	V63 to V0	Register Setting(DC1, DC0)
100	V63	V0	V63 and V0	1/2 frequency setting by DC1, DC0
101	Setting Prohibited	Setting Prohibited	-	-
110	GND	GND	V63 and V0	1/2 frequency setting by DC1, DC0
111	Hi-Z	Hi-Z	V63 and V0	1/2 frequency setting by DC1, DC0

Notes: 1. The power efficiency can be improved by halting grayscale amplifiers and slowing down the step-up clock frequency only in non-display drive period.

2. The gate output level in non-lit display area drive period is determined by PTG[1:0].

8.2.11. Display Control 4 (R0Ah)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0

FMI[2:0] Set the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

FMARKOE When FMARKOE=1, ILI9320 starts to output FMARK signal in the output interval set by FMI[2:0] bits.

FMI[2:0]	Output Interval
000	1 frame
001	2 frame
011	4 frame
101	6 frame
Others	Setting disabled

8.2.12. RGB Display Interface Control 1 (R0Ch)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	ENC2	ENC1	ENC0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0

RIM[1:0] Select the RGB interface data width.

RIM1	RIM0	RGB Interface Mode
0	0	18-bit RGB interface (1 transfer/pixel), DB[17:0]
0	1	16-bit RGB interface (1 transfer/pixel), DB[17:13] and DB[11:1]
1	0	6-bit RGB interface (3 transfers/pixel), DB[17:12]
1	1	Setting disabled

Note1: Registers are set only by the system interface.

Note2: Be sure that one pixel (3 dots) data transfer finished when interface switch.

DM[1:0] Select the display operation mode.

DM1	DM0	Display Interface
0	0	Internal system clock
0	1	RGB interface
1	0	VSYNC interface

1	1	Setting disabled

The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode. However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

RM Select the interface to access the GRAM.

Set RM to "1" when writing display data by the RGB interface.

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

Display State	Operation Mode	RAM Access (RM)	Display Operation Mode (DM[1:0]
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM[1:0] = 00)
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM[1:0] = 01)
Rewrite still picture area while RGB interface Displaying moving pictures.		System interface (RM = 0)	RGB interface (DM[1:0] = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM[1:0] = 10)

Note 1: Registers are set only via the system interface or SPI interface.

Note 2: Refer to the flowcharts of "RGB Input Interface" section for the mode switch.

ENC[2:0] Set the GRAM write cycle through the RGB interface

ENC[2:0]	GRAM Write Cycle (Frame periods)
000	1 Frame
001	2 Frames
010	3 Frames
011	4 Frames
100	5 Frames
101	6 Frames
110	7 Frames
111	8 Frames

8.2.13. Frame Marker Position (R0Dh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0

EMP[8:0] Sets the output position of frame cycle (frame marker).

When FMP[8:0]=0, a high-active pulse FMARK is output at the start of back porch period for one display line period (1H).

Make sure the 9'h000 $\leq$ FMP $\leq$ BP+NL+FP

FMP[8:0]	FMARK Output Position
9'h000	0th line
9'h001	1st line
9'h002	2nd line

9'h003	3rd line
.	.
.	.
.	.
9'h175	373rd line
9'h176	374th line
9'h177	375th line

8.2.14. RGB Display Interface Control 2 (R0Fh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL

DPL: Sets the signal polarity of the DOTCLK pin.

DPL = "0" The data is input on the rising edge of DOTCLK

DPL = "1" The data is input on the falling edge of DOTCLK

EPL: Sets the signal polarity of the ENABLE pin.

EPL = "0" The data DB17-0 is written when ENABLE = "0". Disable data write operation when ENABLE = "1".

EPL = "1" The data DB17-0 is written when ENABLE = "1". Disable data write operation when ENABLE = "0".

HSPL: Sets the signal polarity of the HSYNC pin.

HSPL = "0" Low active

HSPL = "1" High active

VSPL: Sets the signal polarity of the VSYNC pin.

VSPL = "0" Low active

VSPL = "1" High active

8.2.15. Power Control 1 (R10h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	SAP	BT3	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	DSTB	SLP	0

SLP: When SLP = 1, ILI9320 enters the sleep mode and the display operation stops except the RC oscillator to reduce the power consumption. In the sleep mode, the GRAM data and instructions cannot be updated except the following two instructions.

a. Exit sleep mode (SLP = "0")

b. Start oscillation

DSTB: When DSTB = 1, the ILI9320 enters the deep standby mode. In deep standby mode, the internal logic power supply is turned off to reduce power consumption. The GRAM data and instruction setting are not maintained when the ILI9320 enters the deep standby mode, and they must be reset after exiting deep standby mode.

AP[2:0]: Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit. The

larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP[2:0] = "000" to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.

AP[2:0]	In LCD drive power supply amplifiers	In Source driver amplifiers
000	Halt	Halt
001	0.5	0.62
010	0.75	0.71
011	1	1
100	1	1
101	0.5	0.62
110	0.75	0.71
111	1	1

SAP: Source Driver output control

SAP=0, Source driver output is disabled.

SAP=1, Source driver output is enabled.

When starting the charge-pump of LCD in the Power ON stage, make sure that SAP=0, and set the SAP=1, after starting up the LCD power supply circuit.

APE: Power supply enable bit.

Set APE = "1" to start the generation of power supply according to the power supply startup sequence.

BT[3:0]: Sets the factor used in the step-up circuits.

Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

BT[3:0]	DDVDH	VCL	VGH	VGL
4'h0	Vci1 x 2	- Vci1	Vci1 x 6	- Vci1 x 5
4'h1	Vci1 x 2	- Vci1	Vci1 x 8	- Vci1 x 4
4'h2				- Vci1 x 3
4'h3	Vci1 x 2	- Vci1	Vci1 x 7	- Vci1 x 5
4'h4				- Vci1 x 4
4'h5				- Vci1 x 3
4'h6	Vci1 x 2	- Vci1	Vci1 x 6	- Vci1 x 4
4'h7				- Vci1 x 3
4'h8	Vci1 x 3	- Vci1	Vci1 x 9	- Vci1 x 7
4'h9	Vci1 x 3	- Vci1	Vci1 x 12	- Vci1 x 6
4'hA				- Vci1 x 4
4'hB	Vci1 x 3	- Vci1	Vci1 x 10	- Vci1 x 7
4'hC				- Vci1 x 6
4'hD				- Vci1 x 4
4'hE	Vci1 x 3	- Vci1	Vci1 x 9	- Vci1 x 6
4'hF				- Vci1 x 4

Notes: 1. Connect capacitors to the capacitor connection pins when generating DDVDH, VGH, VGL and VCL levels.

2. Make sure DDVDH = 6.0V (max.), VGH = 15.0V (max.), VGL = – 12.5V (max) and VCL= -3.0V (max.)

8.2.16. Power Control 2 (R11h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0

VC[2:0] Sets the ratio factor of VciLVL to generate the reference voltages VciOUT and Vci1.

VC2	VC1	VC0	VciOUT reference voltage Vci1 voltage
0	0	0	0.94 x Vci
0	0	1	0.89 x Vci
0	1	0	Setting disabled
0	1	1	Setting disabled
1	0	0	0.76 x Vci
1	0	1	Setting disabled
1	1	0	Setting disabled
1	1	1	1.0 x Vci

DC0[2:0]: Selects the operating frequency of the step-up circuit 1. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC1[2:0]: Selects the operating frequency of the step-up circuit 2. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC02	DC01	DC00	Step-up circuit1 step-up frequency (f_{DCDC1})	DC12	DC11	DC10	Step-up circuit2 step-up frequency (f_{DCDC2})
0	0	0	Fosc	0	0	0	Fosc / 16
0	0	1	Fosc / 2	0	0	1	Fosc / 32
0	1	0	Fosc / 4	0	1	0	Fosc / 64
0	1	1	Fosc / 8	0	1	1	Fosc / 128
1	0	0	Fosc / 16	1	0	0	Fosc / 256
1	0	1	Setting disabled	1	0	1	Setting disabled
1	1	0	Halt step-up circuit 1	1	1	0	Halt step-up circuit 2
1	1	1	Setting disabled	1	1	1	Setting disabled

Note: Be sure $f_{DCDC1} \geq f_{DCDC2}$ when setting DC0[2:0] and DC1[2:0].

8.2.17. Power Control 3 (R12h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	VCMR	0	0	0	PON	VRH3	VRH2	VRH1	VRH0

VRH[3:0] Set the amplifying rate (1.6 ~ 1.9) of VciLVL applied to output the VREG1OUT level, which is a reference level for the VCOM level and the grayscale voltage level.

VRH3	VRH2	VRH1	VRH0	VREG1OUT	VRH3	VRH2	VRH1	VRH0	VREG1OUT
0	0	0	0	Halt	1	0	0	0	VciLVL x 1.60

0	0	0	1	Setting inhibited	1	0	0	1	VciLVL x 1.65
0	0	1	0	Setting inhibited	1	0	1	0	VciLVL x 1.70
0	0	1	1	Setting inhibited	1	0	1	1	VciLVL x 1.75
0	1	0	0	Setting inhibited	1	1	0	0	VciLVL x 1.80
0	1	0	1	Setting inhibited	1	1	0	1	VciLVL x 1.85
0	1	1	0	Setting inhibited	1	1	1	0	VciLVL x 1.90
0	1	1	1	Setting inhibited	1	1	1	1	Setting inhibited

Make sure that VC and VRH setting restriction: VREG1OUT $\leq$ (DDVDH - 0.5)V.

PON: Control ON/OFF of circuit3 (VGL) output.

PON=0	VGL output is disable
PON=1	VGL output is enable

VCMR: Selects either external resistor (VcomR) or internal electric volume (VCM) to set the electrical

potential of VcomH (Vcom center voltage level).

VCMR = 0 → Using the external variable resistor to adjust the VcomH voltage level

VCMR = 1 → Using the Internal electronic volume (VCM[4:0]) to adjust the VcomH voltage level.

8.2.18. Power Control 4 (R13h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0

VDV[4:0] Select the factor of VREG1OUT to set the amplitude of Vcom alternating voltage from 0.70 to 1.24 x

VREG1OUT .

VDV4	VDV3	VDV2	VDV1	VDV0	VCOM amplitude		VDV4	VDV3	VDV2	VDV1	VDV0	VCOM amplitude
0	0	0	0	0	VREG1OUT x 0.70		1	0	0	0	0	VREG1OUT x 0.87
0	0	0	0	1	VREG1OUT x 0.72		1	0	0	0	1	VREG1OUT x 0.89
0	0	0	1	0	VREG1OUT x 0.74		1	0	0	1	0	VREG1OUT x 0.92
0	0	0	1	1	VREG1OUT x 0.76		1	0	0	1	1	VREG1OUT x 0.94
0	0	1	0	0	VREG1OUT x 0.78		1	0	1	0	0	VREG1OUT x 0.96
0	0	1	0	1	VREG1OUT x 0.80		1	0	1	0	1	VREG1OUT x 0.99
0	0	1	1	0	VREG1OUT x 0.82		1	0	1	1	0	VREG1OUT x 1.01
0	0	1	1	1	VREG1OUT x 0.84		1	0	1	1	1	VREG1OUT x 1.04
0	1	0	0	0	VREG1OUT x 0.86		1	1	0	0	0	VREG1OUT x 1.06
0	1	0	0	1	VREG1OUT x 0.88		1	1	0	0	1	VREG1OUT x 1.09
0	1	0	1	0	VREG1OUT x 0.90		1	1	0	1	0	VREG1OUT x 1.11
0	1	1	1	1	VREG1OUT x 0.92		1	1	1	1	1	VREG1OUT x 1.14
0	1	1	0	0	VREG1OUT x 0.94		1	1	1	0	0	VREG1OUT x 1.16
0	1	1	0	1	VREG1OUT x 0.96		1	1	1	0	1	VREG1OUT x 1.19
0	1	1	1	0	VREG1OUT x 0.98		1	1	1	1	0	VREG1OUT x 1.21
0	1	1	1	1	VREG1OUT x 1.00		1	1	1	1	1	VREG1OUT x 1.24

Set VDV[4:0] to let Vcom amplitude less than 6V.

8.2.19. GRAM Horizontal/Vertical Address Set (R20h, R21h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

AD[16:0] Set the initial value of address counter (AC).

The address counter (AC) is automatically updated in accordance to the setting of the AM, I/D bits

as data is written to the internal GRAM. The address counter is not automatically updated when read data from the internal GRAM.

AD[16:0]	GRAM Data Map
17'h00000 ~ 17'h000EF	1st line GRAM Data
17'h00100 ~ 17'h001EF	2nd line GRAM Data
17'h00200 ~ 17'h002EF	3rd line GRAM Data
17'h00300 ~ 17'h003EF	4th line GRAM Data
17'h13D00 ~ 17' h13DEF	318th line GRAM Data
17'h13E00 ~ 17' h13EEF	319th line GRAM Data
17'h13F00 ~ 17'h13FEF	320th line GRAM Data

Note1: When the RGB interface is selected (RM = "1"), the address AD[16:0] is set to the address counter every frame on the falling edge of VSYNC.

Note2: When the internal clock operation or the VSYNC interface mode is selected (RM = "0"), the address AD[16:0] is set to address counter when update register R21.

8.2.20. Write Data to GRAM (R22h)

R/W	RS	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	RAM write data (WD[17:0], the DB[17:0] pin assignment differs for each interface.																	

This register is the GRAM access port. When update the display data through this register, the address counter (AC) is increased/decreased automatically.

8.2.21. Read Data from GRAM (R22h)

R/W	RS	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	RAM Read Data (RD[17:0], the DB[17:0] pin assignment differs for each interface.																	

RD[17:0] Read 18-bit data from GRAM through the read data register (RDR).

18-bit System Interface

| GRAM Data & RGB Mapping | R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 |

| Write Data Register | RD 17 | RD 16 | RD 15 | RD 14 | RD 13 | RD 12 | RD 11 | RD 10 | RD 9 | RD 8 | RD 7 | RD 6 | RD 5 | RD 4 | RD 3 | RD 2 | RD 1 | RD 0 |

| Output Data | DB 17 | DB 16 | DB 15 | DB 14 | DB 13 | DB 12 | DB 11 | DB 10 | DB 9 | DB 8 | DB 7 | DB 6 | DB 5 | DB 4 | DB 3 | DB 2 | DB 1 | DB 0 |

16-bit System Interface

| GRAM Data & RGB Mapping | R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 |

| Write Data Register | RD 17 | RD 16 | RD 15 | RD 14 | RD 13 | RD 12 | RD 11 | RD 10 | RD 9 | RD 8 | RD 7 | RD 6 | RD 5 | RD 4 | RD 3 | RD 2 | RD 1 | RD 0 |

| Output Data | DB 17 | DB 16 | DB 15 | DB 14 | DB 13 | DB 12 | DB 11 | DB 10 | | DB 8 | DB 7 | DB 6 | DB 5 | DB 4 | DB 3 | DB 2 | DB 1 | |

9-bit System Interface

| GRAM Data & RGB Mapping | R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 |

| Write Data Register | RD 17 | RD 16 | RD 15 | RD 14 | RD 13 | RD 12 | RD 11 | RD 10 | RD 9 | RD 8 | RD 7 | RD 6 | RD 5 | RD 4 | RD 3 | RD 2 | RD 1 | RD 0 |

| Output Data | DB 17 | DB 16 | DB 15 | DB 14 | DB 13 | DB 12 | DB 11 | DB 10 | DB 9 | DB 17 | DB 16 | DB 15 | DB 14 | DB 13 | DB 12 | DB 11 | DB 10 | DB 9 |

1st Transfer / 2nd Transfer

8-bit System Interface / Serial Data Transfer Interface

| GRAM Data & RGB Mapping | R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 |

| Write Data Register | RD 17 | RD 16 | RD 15 | RD 14 | RD 13 | RD 12 | RD 11 | RD 10 | RD 9 | RD 8 | RD 7 | RD 6 | RD 5 | RD 4 | RD 3 | RD 2 | RD 1 | RD 0 |

| Output Data | DB 17 | DB 16 | DB 15 | DB 14 | DB 13 | DB 12 | DB 11 | DB 10 | | DB 17 | DB 16 | DB 15 | DB 14 | DB 13 | DB 12 | DB 11 | DB 10 | |

1st Transfer / 2nd Transfer

Figure 27 Data Read from GRAM through Read Data Register in 18-/16-/9-/8-bit Interface Mode
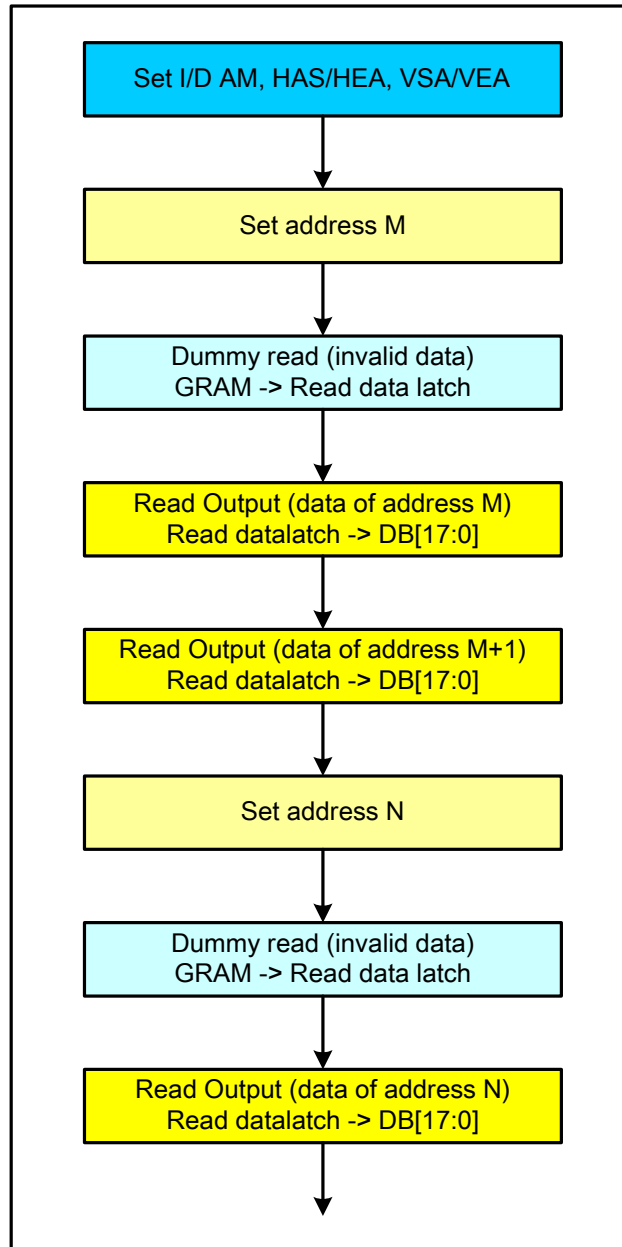
Figure 28 GRAM Data Read Back Flow Chart

8.2.22. Power Control 7 (R29h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0

VCM[4:0] Set the internal VcomH voltage.

VCMR =1, the VcomH voltage is generated based on the VCM[4:0] setting value.

VCMR =0, the VcomH voltage is generated based on the external reference voltage VCOMR.

VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
0	0	0	0	0	VREG1OUT x 0.69	1	0	0	0	0	VREG1OUT x 0.85
0	0	0	0	1	VREG1OUT x 0.70	1	0	0	0	1	VREG1OUT x 0.86
0	0	0	1	0	VREG1OUT x 0.71	1	0	0	1	0	VREG1OUT x 0.87
0	0	0	1	1	VREG1OUT x 0.72	1	0	0	1	1	VREG1OUT x 0.88
0	0	1	0	0	VREG1OUT x 0.73	1	0	1	0	0	VREG1OUT x 0.89

0	0	1	0	1	VREG1OUT x 0.74	1	0	1	0	1	VREG1OUT x 0.90
0	0	1	1	0	VREG1OUT x 0.75	1	0	1	1	0	VREG1OUT x 0.91
0	0	1	1	1	VREG1OUT x 0.76	1	0	1	1	1	VREG1OUT x 0.92
0	1	0	0	0	VREG1OUT x 0.77	1	1	0	0	0	VREG1OUT x 0.93
0	1	0	0	1	VREG1OUT x 0.78	1	1	0	0	1	VREG1OUT x 0.94
0	1	0	1	0	VREG1OUT x 0.79	1	1	0	1	0	VREG1OUT x 0.95
0	1	1	1	1	VREG1OUT x 0.80	1	1	0	1	1	VREG1OUT x 0.96
0	1	1	0	0	VREG1OUT x 0.81	1	1	1	0	0	VREG1OUT x 0.97
0	1	1	0	1	VREG1OUT x 0.82	1	1	1	0	1	VREG1OUT x 0.98
0	1	1	1	0	VREG1OUT x 0.83	1	1	1	1	0	VREG1OUT x 0.99
0	1	1	1	1	VREG1OUT x 0.84	1	1	1	1	1	VREG1OUT x 1.00

8.2.23. Frame Rate and Color Control (R2Bh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	EXT_R	0	FR_SEL1	FR_SEL0	0	0	0	0

EXT_R: Select the external or internal resistor for oscillator circuit.

EXT_R	Resistor Selection
0	**Internal Resistor (default)**
1	External Resistor

FR_SEL[1:0] Set the frame rate when the internal resistor is used for oscillator circuit.

FR_SEL1	FR_SEL0	Frame Rate (Hz)
0	0	**100 (default)**
0	1	90
1	0	120
1	1	110

8.2.24. Gamma Control (R30h ~ R3Dh)

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R30h	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
R31h	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
R32h	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
R35h	W	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
R36h	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	VRP0[4]	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
R37h	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
R38h	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
R39h	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
R3Ch	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]
R3Dh	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	VRN0[4]	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]

KP5-0[2:0] : γ fine adjustment register for positive polarity

RP1-0[2:0] : γ gradient adjustment register for positive polarity

VRP1-0[4:0] : γ amplitude adjustment register for positive polarity

KN5-0[2:0] : γ fine adjustment register for negative polarity

RN1-0[2:0] : γ gradient adjustment register for negative polarity

VRN1-0[4:0] : γ amplitude adjustment register for negative polarity

For details " γ -Correction Function" section.

8.2.25. Horizontal and Vertical RAM Address Position (R50h, R51h, R52h, R53h)

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R50h	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
R51h	W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
R52h	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
R53h	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0

HSA[7:0]/HEA[7:0] HSA[7:0] and HEA[7:0] represent the respective addresses at the start and end of the window address area in horizontal direction. By setting HSA and HEA bits, it is possible to limit the area on the GRAM horizontally for writing data. The HSA and HEA bits must be set before starting RAM write operation. In setting these bits, be sure "00"h ≤ HSA[7:0]< HEA[7:0] ≤ "EF"h. and "04"h≦HEA-HAS.

VSA[8:0]/VEA[8:0] VSA[8:0] and VEA[8:0] represent the respective addresses at the start and end of the window address area in vertical direction. By setting VSA and VEA bits, it is possible to limit the area on the GRAM vertically for writing data. The VSA and VEA bits must be set before starting RAM write operation. In setting, be sure "000"h ≤ VSA[8:0]< VEA[8:0] ≤ "13F"h.
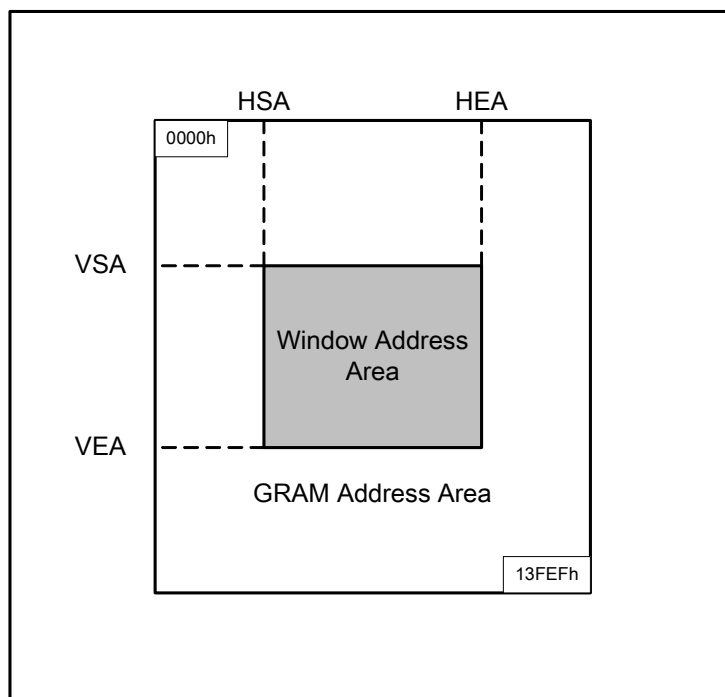

Figure 29 GRAM Access Range Configuration

"00"h ≤HAS[7:0] ≤HEA[7:0] ≤"EF"h

"00"h ≤VSA[7:0] ≤VEA[7:0] ≤"13F"h

Note1. The window address range must be within the GRAM address space.

Note2. Data are written to GRAM in four-words when operating in high speed mode, the dummy write operations should be inserted depending on the window address area. For details, see the High-Speed RAM Write Function section.

8.2.26. Gate Scan Control (R60h, R61h, R6Ah)

	R/W	RS		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R60h	W	1		GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
R61h	W	1		0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
R6Ah	W	1		0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0

SCN[5:0]   The ILI9320 allows to specify the gate line from which the gate driver starts to scan by setting the SCN[5:0] bits.

SCN[5:0]	Scanning Start Position			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
00h	G1	G320	G1	G320
01h	G9	G312	G17	G304
02h	G17	G304	G33	G288
03h	G25	G296	G49	G272
04h	G33	G288	G65	G256
05h	G41	G280	G81	G240
06h	G49	G272	G97	G224
07h	G57	G264	G113	G208
08h	G65	G256	G129	G192
09h	G73	G248	G145	G176
0Ah	G81	G240	G161	G160
0Bh	G89	G232	G177	G144
0Ch	G97	G224	G193	G128
0Dh	G105	G216	G209	G112
0Eh	G113	G208	G2	G96
0Fh	G121	G200	G18	G80
10h	G129	G192	G34	G64
11h	G137	G184	G50	G48
12h	G145	G176	G66	G32
13h	G153	G168	G82	G16
14h	G161	G160	G98	G319
15h	G169	G152	G114	G303
16h	G177	G144	G130	G287
17h	G185	G136	G146	G271
18h	G193	G128	G162	G255
19h	G201	G120	G178	G239
1Ah	G209	G112	G194	G223
1Bh	G217	G104	G114	G207
1Ch	G225	G96	G130	G191
1Dh	G233	G88	G146	G175
1Eh	G241	G80	G162	G159
1Fh	G249	G72	G178	G143

20h	G257	G64	G194	G127
21h	G265	G56	G210	G111
22h	G273	G48	G226	G95
23h	G281	G40	G242	G79
24h	G289	G32	G258	G63
25h	G297	G24	G274	G47
26h	G305	G16	G290	G31
27h	G313	G8	G306	G15
28h ~ 3Fh	Setting disabled	Setting disabled	Setting disabled	Setting disabled

NL[5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is

not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more

than the number of lines necessary for the size of the liquid crystal panel.

NL[5:0]	LCD Drive Line
6'h1D	240 lines
6'h1E	248 lines
6'h1F	256 lines
6'h20	264 lines
6'h21	272 lines
6'h22	280 lines
6'h23	288 lines
6'h24	296 lines
6'h25	304 lines
6'h26	312 line
6'h27	320 line
Others	Setting inhibited

NDL: Sets the source driver output level in the non-display area.

NDL	Non-Display Area	
	Positive Polarity	Negative Polarity
0	V63	V0
1	V0	V63

GS: Sets the direction of scan by the gate driver in the range determined by SCN[4:0] and NL[4:0]. The scan

direction determined by GS = 0 can be reversed by setting GS = 1.

When GS = 0, the scan direction is from G1 to G320.

When GS = 1, the scan direction is from G320 to G1

REV: Enables the grayscale inversion of the image by setting REV=1.

REV	GRAM Data	Source Output in Display Area	
		Positive polarity	negative polarity
	18'h00000	V63	V0
0	.	.	.
	.	.	.
	.	.	.
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63

.	.	.
.	.	.
.	.	.
18'h3FFFF	V63	V0

VLE: Vertical scroll display enable bit. When VLE = 1, the ILI9320 starts displaying the base image from the line (of the physical display) determined by VL[8:0] bits. VL[8:0] sets the amount of scrolling, which is the number of lines to shift the start line of the display from the first line of the physical display. Note that the partial image display position is not affected by the base image scrolling.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE = "0".

VLE	Base Image Display
0	Fixed
1	Enable Scrolling

VL[8:0]: Sets the scrolling amount of base image. The base image is scrolled in vertical direction and displayed from the line determined by VL[8:0]. Make sure that VL[8:0] ≤ 320.

8.2.27. Partial Image 1 Display Position (R80h)

R/W	RS		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1		0	0	0	0	0	0	0	PTD P0[8]	PTD P0[7]	PTD P0[6]	PTD P0[5]	PTD P0[4]	PTD P0[3]	PTD P0[2]	PTD P0[1]	PTD P0[0]

PTDP0[8:0]: Sets the display position of partial image 1. The display areas of the partial images 1 and 2 must not overlap each another.

8.2.28. Partial Image 1 RAM Start/End Address (R81h, R82h)

R/W	RS		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1		0	0	0	0	0	0	0	PTS A0[8]	PTS A0[7]	PTS A0[6]	PTS A0[5]	PTS A0[4]	PTS A0[3]	PTS A0[2]	PTS A0[1]	PTS A0[0]
W	1		0	0	0	0	0	0	0	PTE A0[8]	PTE A0[7]	PTE A0[6]	PTE A0[5]	PTE A0[4]	PTE A0[3]	PTE A0[2]	PTE A0[1]	PTE A0[0]

PTSA0[8:0] PTEA0[8:0]: Sets the start line address and the end line address of the RAM area storing the data of partial image 1. Make sure PTSA0[8:0] ≤ PTEA0[8:0].

8.2.29. Partial Image 2 Display Position (R83h)

R/W	RS		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1		0	0	0	0	0	0	0	PTS P1[8]	PTD P1[7]	PTD P1[6]	PTD P1[5]	PTD P1[4]	PTD P1[3]	PTD P1[2]	PTD P1[1]	PTD P1[0]

PTDP1[8:0]: Sets the display position of partial image 2 The display areas of the partial images 1 and 2 must not overlap each another.

8.2.30. Partial Image 2 RAM Start/End Address (R84h, R85h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1		0	0	0	0	0	0	0	PTS A1[8]	PTS A1[7]	PTS A1[6]	PTS A1[5]	PTS A1[4]	PTS A1[3]	PTS A1[2]	PTS A1[1]	PTS A1[0]
W	1		0	0	0	0	0	0	0	PTE A1[8]	PTE A1[7]	PTE A1[6]	PTE A1[5]	PTE A1[4]	PTE A1[3]	PTE A1[2]	PTE A1[1]	PTE A1[0]

PTSA1[8:0] PTEA1[8:0]: Sets the start line address and the end line address of the RAM area storing the data of partial image 2 Make sure PTSA1[8:0] ≤ PTEA1[8:0].

8.2.31. Panel Interface Control 1 (R90h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	DIVI1	DIVI0	0	0	0	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0

RTNI[4:0]: Sets 1H (line) clock number of internal clock operating mode. In this mode, ILI9320 display operation is synchronized with internal clock signal.

RTNI[4:0]	Clocks/Line	RTNI[4:0]	Clocks/Line
00000~01111	Setting Disabled	11000	24 clocks
10000	16 clocks	11001	25 clocks
10001	17 clocks	11010	26 clocks
10010	18 clocks	11011	27 clocks
10011	19 clocks	11100	28 clocks
10100	20 clocks	11101	29 clocks
10101	21 clocks	11110	30 clocks
10110	22 clocks	11111	31 clocks
10111	23 clocks		

DIVI[1:0]: Sets the division ratio of internal clock frequency.

DIVI1	DIVI0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

Formula to calculate frame frequency

$$Frame\ Rate\ =\ \frac{f_{osc.}}{Clock\ cycles\ per\ line \times division\ ratio \times (Lines + BP + FP)}$$

$f_{osc.}$: frequency if RC oscillation.
Clock cycles per line : RTN bits
Division ratio : DIV bits
Lines : number of lines for driving the LCD panel.
FP: Front porch lines
BP; Back porch lines

8.2.32. Panel Interface Control 2 (R92h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	NOWI[2]	NOWI[1]	NOWI[0]	0	0	0	0	0	0	0	0

NOWI[2:0]: Sets the gate output non-overlap period when ILI9320 display operation is synchronized with internal clock signal.

NOWI[2:0]	Gate Non-overlap Period
000	0 clocks
001	1 clocks
010	2 clocks
011	3 clocks
100	4 clocks
101	5 clocks
110	6 clocks
111	7 clocks

Note: The gate output non-overlap period is defined by the number of frequency-divided internal clocks, the frequency of which is determined by instruction (DIVI), from the reference point.

8.2.33. Panel Interface Control 3 (R93h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPI2	MCPI1	MCPI0

MCPI[2:0]: Sets the source output position when ILI9320 display operation is synchronized with internal clock signal.

MCPI[2:0]	Source Output Position
000	Setting inhibited
001	1 clocks
010	2 clocks
011	3 clocks
100	4 clocks
101	5 clocks
110	6 clocks
111	7 clocks

Note: The gate output non-overlap period is defined by the number of frequency-divided internal clocks, the frequency of which is determined by instruction (DIVI[1:0]), from the reference point.

8.2.34. Panel Interface Control 4 (R95h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0

RTNE[5:0]: Sets 1H (line) clock number of RGB interface mode. In this mode, ILI9320 display operation is synchronized with RGB interface signals.

DIVE (division ratio) x RTNE (DOTCLKs) ≤ DOTCLKs in 1H period.

RTNE[5:0]	Clocks per line period (1H)	RTNE[5:0]	Clocks per line period (1H)	RTNE[5:0]	Clocks per line period (1H)	RTNE[5:0]	Clocks per line period (1H)
00h	Setting Prohibited	10h	16 clocks	20h	32 clocks	30h	48 clocks
01h	Setting Prohibited	11h	17 clocks	21h	33 clocks	31h	49 clocks

02h	Setting Prohibited	12h	18 clocks	22h	34 clocks	32h	50 clocks
03h	Setting Prohibited	13h	19 clocks	23h	35 clocks	33h	51 clocks
04h	Setting Prohibited	14h	20 clocks	24h	36 clocks	34h	52 clocks
05h	Setting Prohibited	15h	21 clocks	25h	37 clocks	35h	53 clocks
06h	Setting Prohibited	16h	22 clocks	26h	38 clocks	36h	54 clocks
07h	Setting Prohibited	17h	23 clocks	27h	39 clocks	37h	55 clocks
08h	Setting Prohibited	18h	24 clocks	28h	40 clocks	38h	56 clocks
09h	Setting Prohibited	19h	25 clocks	29h	41 clocks	39h	57 clocks
0ah	Setting Prohibited	1ah	26 clocks	2ah	42 clocks	3ah	58 clocks
0bh	Setting Prohibited	1bh	27 clocks	2bh	43 clocks	3bh	59 clocks
0ch	Setting Prohibited	1ch	28 clocks	2ch	44 clocks	3ch	60 clocks
0dh	Setting Prohibited	1dh	29 clocks	2dh	45 clocks	3dh	61 clocks
0eh	Setting Prohibited	1eh	30 clocks	2eh	46 clocks	3eh	62 clocks
0fh	Setting Prohibited	1fh	31 clocks	2fh	47 clocks	3fh	63 clocks

DIVE[1:0]: Sets the division ratio of DOTCLK when ILI9320 display operation is synchronized with RGB interface signals.

DIVE[1:0]	Division Ratio	18/16-bit RGB Interface	DOTCLK=5MHz	6-bit x 3 Transfers RGB Interface	DOTCLK=5MHz
00	Setting Prohibited	Setting Prohibited	-	Setting Prohibited	-
01	1/4	4 DOTCLKS	0.8 μs	12 DOTCLKS	0.8 μs
10	1/8	8 DOTCLKS	1.6 μs	24 DOTCLKS	1.6 μs
11	1/16	16 DOTCLKS	3.2 μs	48 DOTCLKS	3.2 μs

8.2.35. Panel Interface Control 5 (R97h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	NOWE3	NOWE2	NOWE1	NOWE0	0	0	0	0	0	0	0	0

NOWE[2:0]: Sets the gate output non-overlap period when the ILI9320 display operation is synchronized with RGB interface signals.

NOWE[3:0]	Gate Non-overlap Period	NOWE[3:0]	Gate Non-overlap Period
0000	0 clocks	1000	8 clocks
0001	1 clocks	1001	9 clocks
0010	2 clocks	1010	10 clocks
0011	3 clocks	1011	11 clocks
0100	4 clocks	1100	12 clocks
0101	5 clocks	1101	13 clocks
0110	6 clocks	1110	14 clocks
0111	7 clocks	1111	15 clocks

Note: 1 clock = (number of data transfer/pixel) x DIVE (division ratio) [DOTCLK]

8.2.36. Panel Interface Control 6 (R98h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPE2	MCPE1	MCPE0

MCPE[2:0]: Sets the source output position when the ILI9320 display operation is synchronized with RGB interface signals.

MCPE[2:0]	Source Output Position
000	0 clocks
001	1 clocks
010	2 clocks
011	3 clocks

100	4 clocks
101	5 clocks
110	6 clocks
111	7 clocks

Note: 1 clock = (number of data transfer/pixel) x DIVE (division ratio) [DOTCLK]

9. GRAM Address Map & Read/Write

ILI9320 has an internal graphics RAM (GRAM) of 87,120 bytes to store the display data and one pixel is constructed of 18 bits. The GRAM can be accessed through the i80 system, SPI and RGB interfaces.
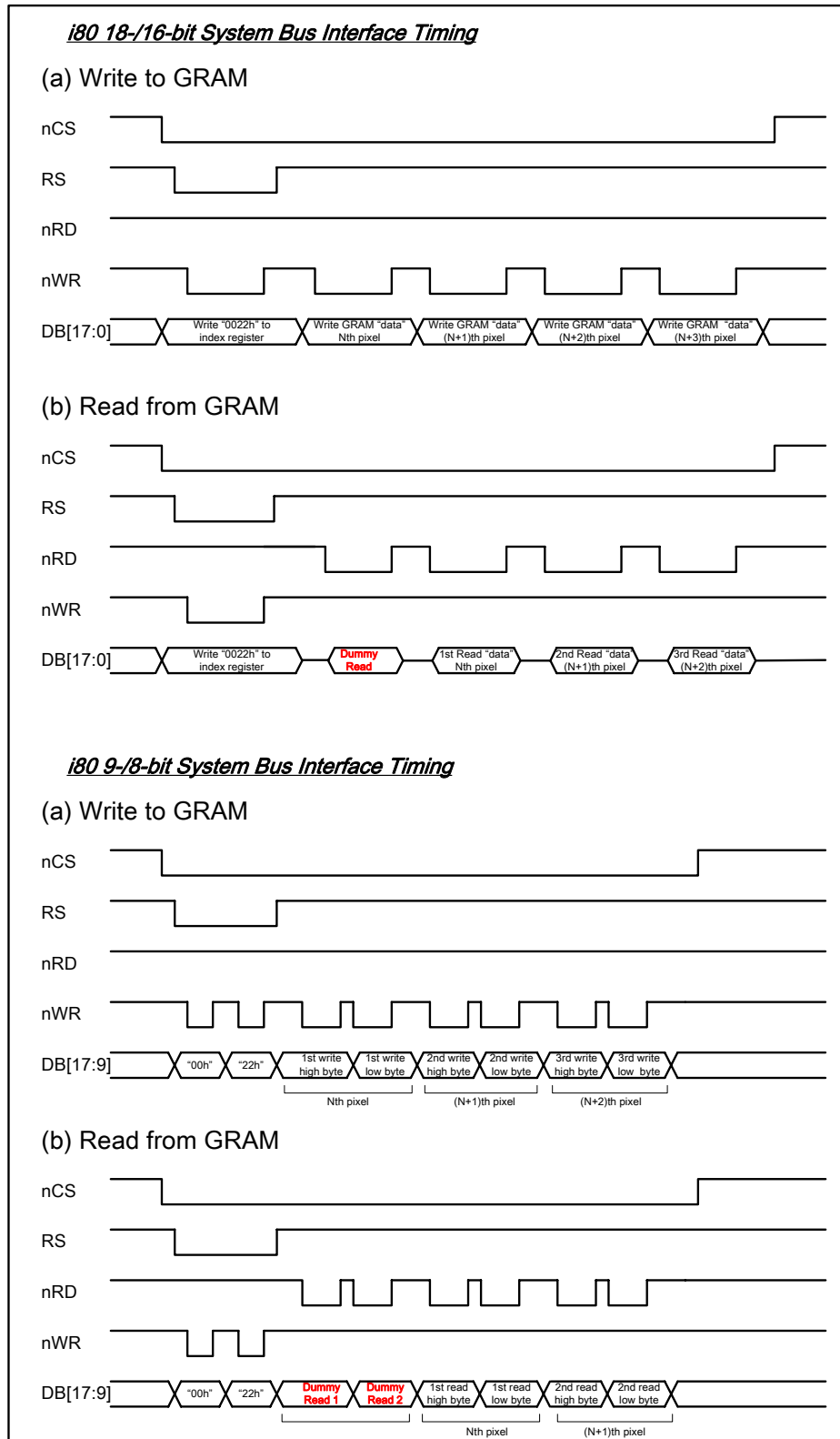

Figure30 GRAM Read/Write Timing of i80-System Interface

GRAM address map table of SS=0, BGR=0

SS=0, BGR=0		S1…S3	S4…S6	S7…S9	S10…S12	…	S517…S519	S520…S522	S523…S525	S526…S720
GS=0	GS=1	DB17…0	DB17…0	DB17…0	DB17…0	…	DB17…0	DB17…0	DB17…0	DB17…0
G1	G320	"00000h"	"00001h"	"00002h"	"00003h"	…	"000ECh"	"000EDh"	"000EEh"	"000EFh"
G2	G319	"00100h"	"00101h"	"00102h"	"00103h"	…	"001ECh"	"001EDh"	"001EEh"	"001EFh"
G3	G318	"00200h"	"00201h"	"00202h"	"00203h"	…	"002ECh"	"002EDh"	"002EEh"	"002EFh"
G4	G317	"00300h"	"00301h"	"00302h"	"00303h"	…	"003ECh"	"003EDh"	"003EEh"	"003EFh"
G5	G316	"00400h"	"00401h"	"00402h"	"00403h"	…	"004ECh"	"004EDh"	"004EEh"	"004EFh"
G6	G315	"00500h"	"00501h"	"00502h"	"00503h"	…	"005ECh"	"005EDh"	"005EEh"	"005EFh"
G7	G314	"00600h"	"00601h"	"00602h"	"00603h"	…	"006ECh"	"006EDh"	"006EEh"	"006EFh"
G8	G313	"00700h"	"00701h"	"00702h"	"00703h"	…	"007ECh"	"007EDh"	"007EEh"	"007EFh"
G9	G312	"00800h"	"00801h"	"00802h"	"00803h"	…	"008ECh"	"008EDh"	"008EEh"	"008EFh"
G10	G311	"00900h"	"00901h"	"00902h"	"00903h"	…	"009ECh"	"009EDh"	"009EEh"	"009EFh"
.	.	.	.	.	.	…	.	.	.	.
.	.	.	.	.	.		.	.	.	.
.	.	.	.	.	.		.	.	.	.
G311	G10	"13600h"	"13601h"	"13602h"	"13603h"	…	"136ECh"	"136EDh"	"136EEh"	"136EFh"
G312	G9	"13700h"	"13701h"	"13702h"	"13703h"	…	"137ECh"	"137EDh"	"137EEh"	"137EFh"
G313	G8	"13800h"	"13801h"	"13802h"	"13803h"	…	"138ECh"	"138EDh"	"138EEh"	"138EFh"
G314	G7	"13900h"	"13901h"	"13902h"	"13903h"	…	"139ECh"	"139EDh"	"139EEh"	"139EFh"
G315	G6	"13A00h"	"13A01h"	"13A02h"	"13A03h"	…	"13AECh"	"13AEDh"	"13AEEh"	"13AEFh"
G316	G5	"13B00h"	"13B01h"	"13B02h"	"13B03h"	…	"13BECh"	"13BEDh"	"13BEEh"	"13BEFh"
G317	G4	"13C00h"	"13C01h"	"13C02h"	"13C03h"	…	"13CECh"	"13CEDh"	"13CEEh"	"13CEFh"
G318	G3	"13D00h"	"13D01h"	"13D02h"	"13D03h"	…	"13DECh"	"13DEDh"	"13DEEh"	"13DEFh"
G319	G2	"13E00h"	"13E01h"	"13E02h"	"13E03h"	…	"13EECh"	"13EEDh"	"13EEEh"	"13EEFh"
G320	G1	"13F00h"	"13F01h"	"13F02h"	"13F03h"	…	"13FECh"	"13FEDh"	"13FEEh"	"13FEFh"

i80/M68 system 18-bit data bus interface

GRAM Data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0

RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Source Output Pin	S (3n+1)	S (3n+2)	S (3n+3)

N=0 to 175

i80/M68 system 16-bit data bus interface

GRAM Data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10		DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1

RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Source Output Pin	S (3n+1)	S (3n+2)	S (3n+3)

N=0 to 175

i80/M68 system 9-bit data bus interface

	1st Transfer									2nd Transfer								
GRAM Data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9

RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Source Output Pin	S (3n+1)	S (3n+2)	S (3n+3)

N=0 to 175

GRAM Data and display data of 18-/16-/9-bit system interface (SS="0", BGR="0")

Figure31 i80-System Interface with 18-/16-/9-bit Data Bus (SS="0", BGR="0")

i80/M68 system 8-bit interface / SPI Interface (2 transfers/pixel)

	1st transfer								2nd transfer							
GRAM Data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Source Output Pin	S (3n+1)						S (3n+2)						S (3n+3)			

N=0 to 175

i80/M68 system 8-bit interface (3 transfers/pixel, TRI="1", DFM[1:0]="00")

	1st Transfer		2nd Transfer								3rd Transfer							
GRAM Data	DB 11	DB 10	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Source Output Pin	S (3n+1)						S (3n+2)						S (3n+3)			

N=0 to 175

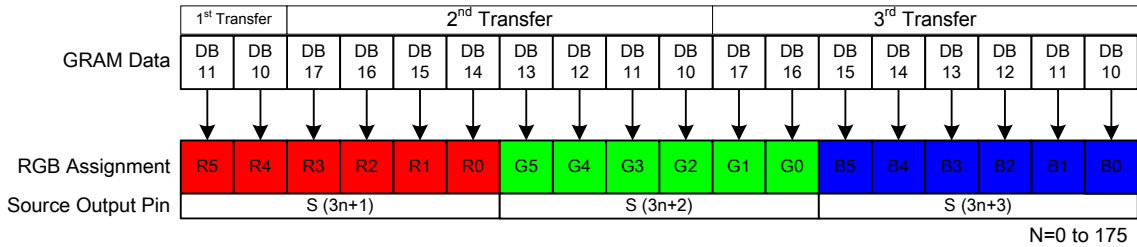## i80/M68 system 8-bit interface (3 transfers/pixel, TRI="1", DFM[1:0]="10")

	1st Transfer						2nd Transfer						3rd Transfer					
GRAM Data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Source Output Pin	S (3n+1)						S (3n+2)						S (3n+3)			

N=0 to 175

i80/M68 system 8-bit interface (SS="0", BGR="0")

Figure32 i80-System Interface with 8-bit Data Bus (SS="0", BGR="0")

GRAM address map table of SS=1, BGR=1
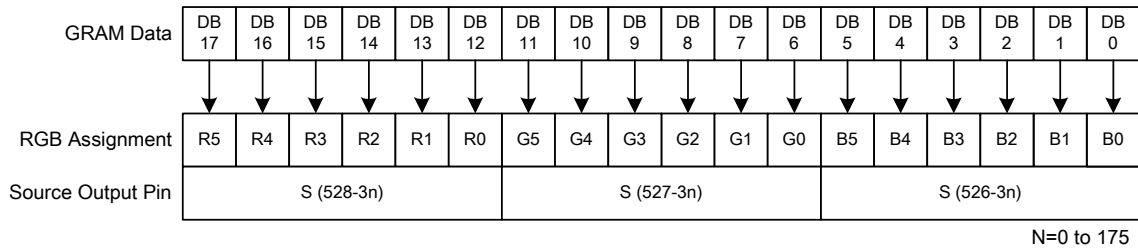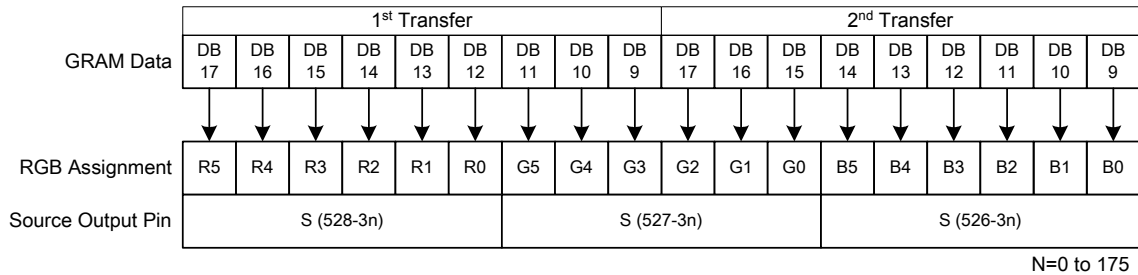
SS=0, BGR=0		S720…S718	S717…S715	S714…S712	S711…S709	…	S12…S10	S9…S7	S6…S4	S3…S1
GS=0	GS=1	DB17…0	DB17…0	DB17…0	DB17…0	…	DB17…0	DB17…0	DB17…0	DB17…0
G1	G320	"00000h"	"00001h"	"00002h"	"00003h"	…	"000ECh"	"000EDh"	"000EEh"	"000EFh"
G2	G319	"00100h"	"00101h"	"00102h"	"00103h"	…	"001ECh"	"001EDh"	"001EEh"	"001EFh"
G3	G318	"00200h"	"00201h"	"00202h"	"00203h"	…	"002ECh"	"002EDh"	"002EEh"	"002EFh"
G4	G317	"00300h"	"00301h"	"00302h"	"00303h"	…	"003ECh"	"003EDh"	"003EEh"	"003EFh"
G5	G316	"00400h"	"00401h"	"00402h"	"00403h"	…	"004ECh"	"004EDh"	"004EEh"	"004EFh"
G6	G315	"00500h"	"00501h"	"00502h"	"00503h"	…	"005ECh"	"005EDh"	"005EEh"	"005EFh"
G7	G314	"00600h"	"00601h"	"00602h"	"00603h"	…	"006ECh"	"006EDh"	"006EEh"	"006EFh"
G8	G313	"00700h"	"00701h"	"00702h"	"00703h"	…	"007ECh"	"007EDh"	"007EEh"	"007EFh"
G9	G312	"00800h"	"00801h"	"00802h"	"00803h"	…	"008ECh"	"008EDh"	"008EEh"	"008EFh"
G10	G311	"00900h"	"00901h"	"00902h"	"00903h"	…	"009ECh"	"009EDh"	"009EEh"	"009EFh"
.	.	.	.	.	.	…	.	.	.	.
.	.	.	.	.	.		.	.	.	.
.	.	.	.	.	.		.	.	.	.
G311	G10	"13600h"	"13601h"	"13602h"	"13603h"	…	"136ECh"	"136EDh"	"136EEh"	"136EFh"
G312	G9	"13700h"	"13701h"	"13702h"	"13703h"	…	"137ECh"	"137EDh"	"137EEh"	"137EFh"
G313	G8	"13800h"	"13801h"	"13802h"	"13803h"	…	"138ECh"	"138EDh"	"138EEh"	"138EFh"
G314	G7	"13900h"	"13901h"	"13902h"	"13903h"	…	"139ECh"	"139EDh"	"139EEh"	"139EFh"
G315	G6	"13A00h"	"13A01h"	"13A02h"	"13A03h"	…	"13AECh"	"13AEDh"	"13AEEh"	"13AEFh"
G316	G5	"13B00h"	"13B01h"	"13B02h"	"13B03h"	…	"13BECh"	"13BEDh"	"13BEEh"	"13BEFh"
G317	G4	"13C00h"	"13C01h"	"13C02h"	"13C03h"	…	"13CECh"	"13CEDh"	"13CEEh"	"13CEFh"
G318	G3	"13D00h"	"13D01h"	"13D02h"	"13D03h"	…	"13DECh"	"13DEDh"	"13DEEh"	"13DEFh"
G319	G2	"13E00h"	"13E01h"	"13E02h"	"13E03h"	…	"13EECh"	"13EEDh"	"13EEEh"	"13EEFh"
G320	G1	"13F00h"	"13F01h"	"13F02h"	"13F03h"	…	"13FECh"	"13FEDh"	"13FEEh"	"13FEFh"

i80/M68 system 18-bit data bus interface

GRAM Data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Source Output Pin	S (528-3n)						S (527-3n)						S (526-3n)					

N=0 to 175

i80/M68 system 9-bit data bus interface

	1st Transfer									2nd Transfer								
GRAM Data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Source Output Pin	S (528-3n)						S (527-3n)						S (526-3n)					

N=0 to 175

GRAM Data and display data of 18-/9-bit system interface (SS="1", BGR="1")

Figure 33 i80-System Interface with 18-/9-bit Data Bus (SS="1", BGR="1")

10. Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made on the internal RAM. The window address area is made by setting the horizontal address register (start: HSA[7:0], end: HEA[7:0] bits) and the vertical address register (start: VSA[8:0], end: VEA[8:0] bits). The AM bit sets the transition direction of RAM address (either increment or decrement). These bits enable the ILI9320 to write data including image data consecutively not taking data wrap positions into account.

The window address area must be made within the GRAM address map area. Also, the GRAM address bits (RAM address set register) must be an address within the window address area.
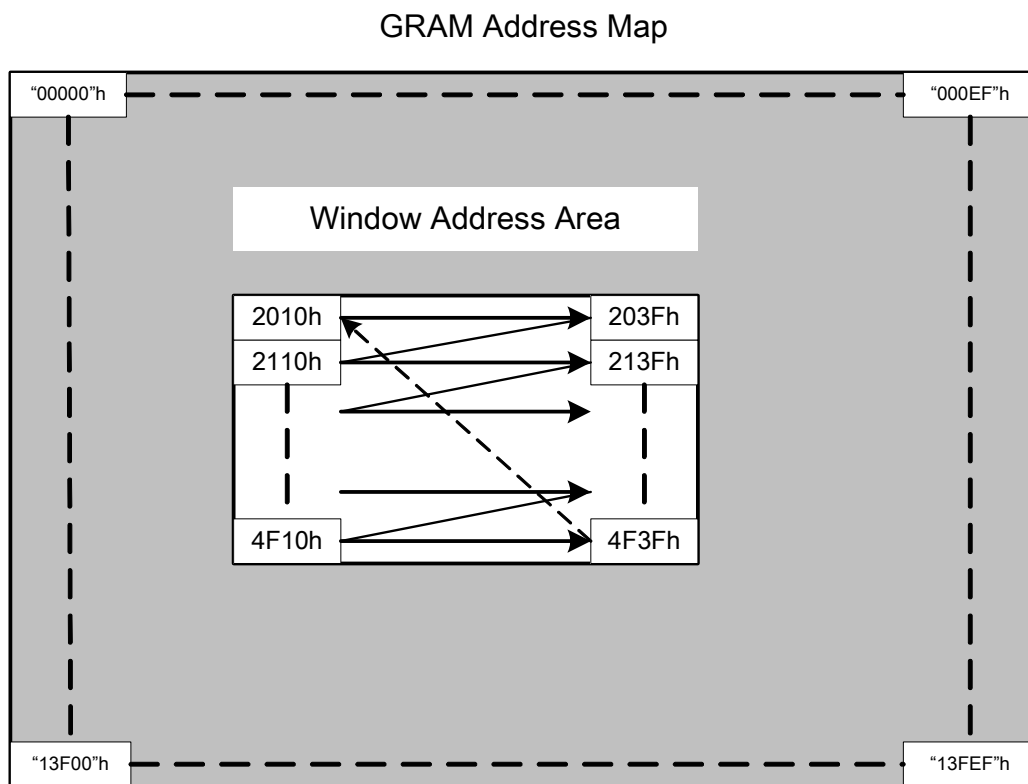
[Window address setting area]

   (Horizontal direction) 00H ≤ HSA[7:0] ≤ HEA[7:0] ≤ "EF"H

   (Vertical direction) 00H ≤ VSA[8:0] ≤ VEA[8:0]≤ "13F"H

[RAM address, AD (an address within a window address area)]]

   (RAM address) HSA[7:0] ≤ AD[7:0] ≤ HEA[7:0]

   VSA[8:0] ≤ AD[15:8] ≤ VEA[8:0]

GRAM Address Map

Window address setting area

   HSA[7:0] = 10h, HSA[7:0] = 3Fh,   I/D = 1 (increment)
   VSA[8:0] = 20h, VSA[8:0] = 4Fh,   AM = 0 (horizontal writing)

Figure 34 GRAM Access Window Map

Version: 0.51

11. Gamma Correction

ILI9320 incorporates the γ-correction function to display 262,144 colors for the LCD panel. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make ILI9320 available with liquid crystal panels of various characteristics.
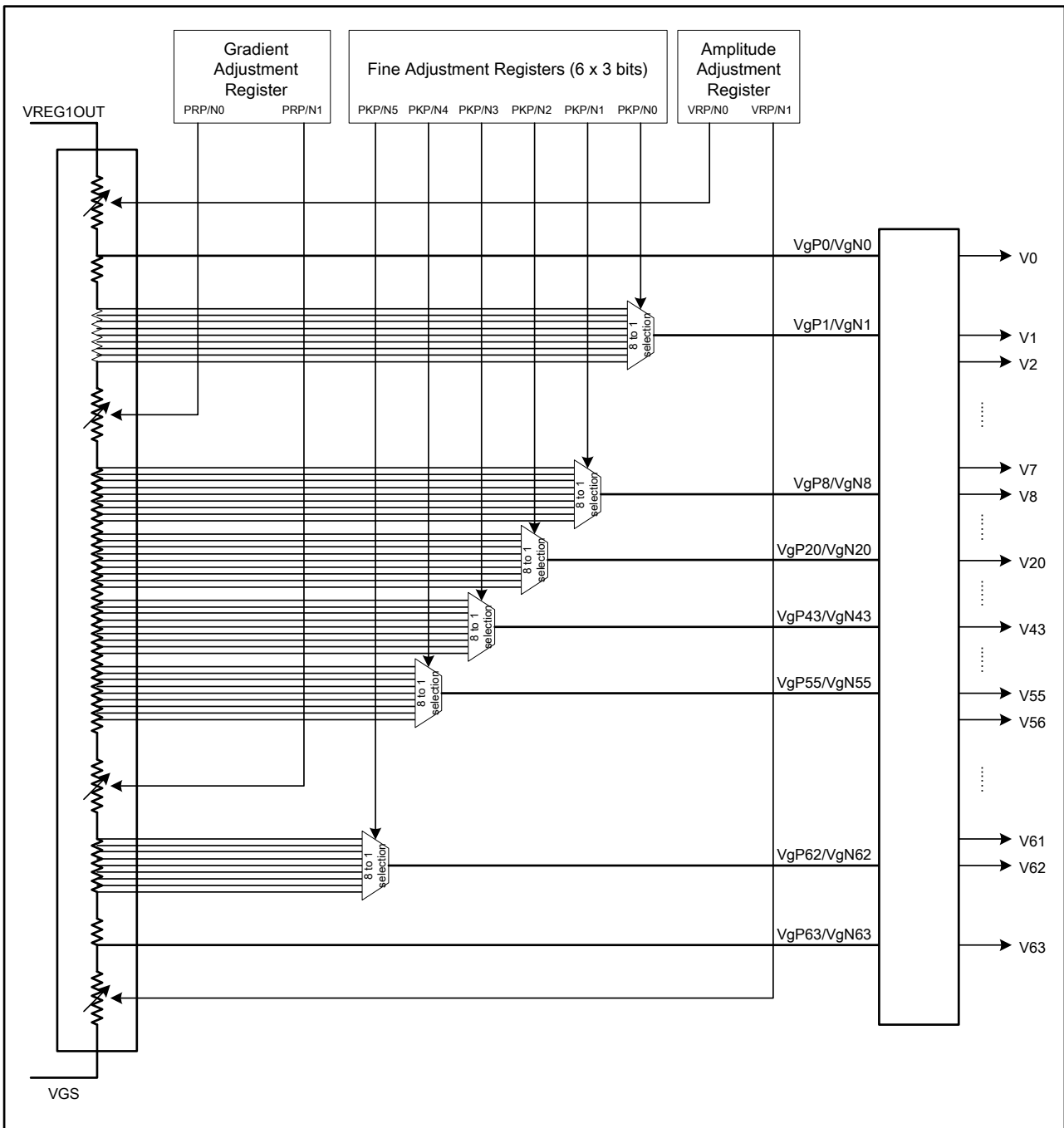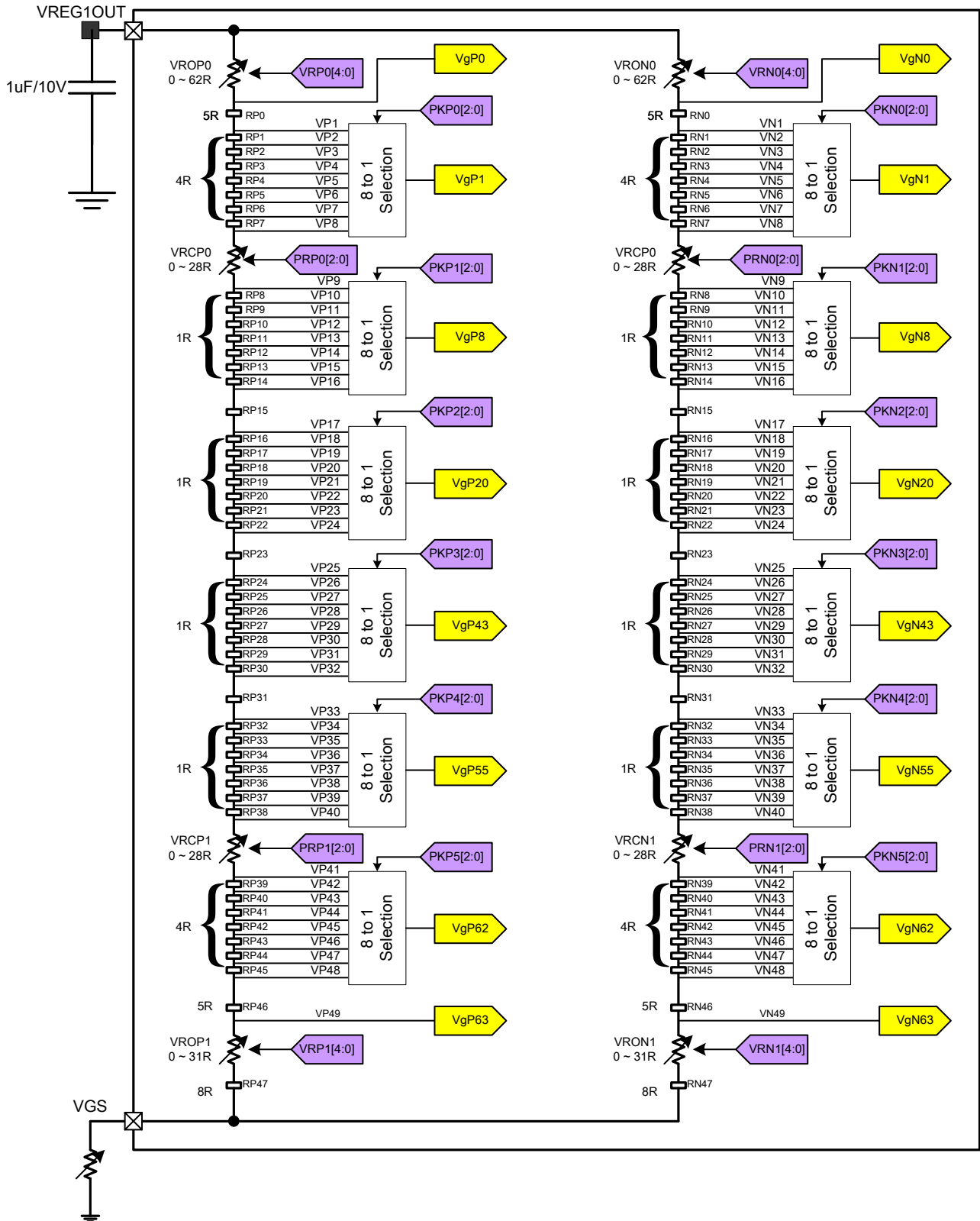

Figure 35 Grayscale Voltage Generation

Figure 36 Grayscale Voltage Adjustment

1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale reference voltage level. To adjust the gradient, the resistance values of variable resistors in the middle of the ladder resistor are adjusted by registers PRP0[2:0]/PRN0[2:0], PRP1[2:0]/PRN1[2:0]. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers, VRP0[4:0]/VRN0[4:0], VRP1[4:0]/VRN1[4:0], are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of variable resistors at the top and bottom of the ladder resistor are adjusted. Same as the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

3. Fine adjustment registers

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.
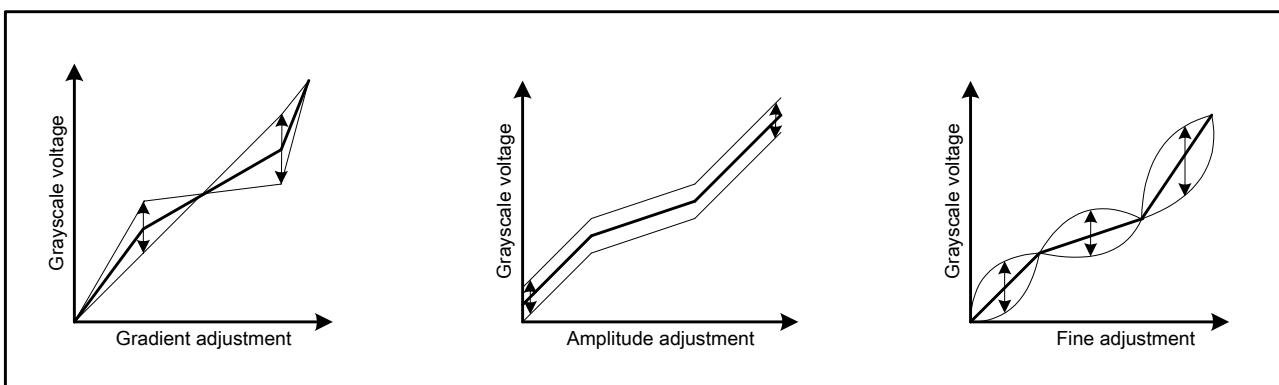

Figure 37 Gamma Curve Adjustment

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0 [2:0]	PRN0 [2:0]	Variable resistor VRCP0, VRCN0
	PRP1 [2:0]	PRN1 [2:0]	Variable resistor VRCP1, VRCN1
Amplitude adjustment	VRP0 [4:0]	VRN0 [4:0]	Variable resistor VROP0, VRON0
	VRP1 [4:0]	VRN1 [4:0]	Variable resistor VROP1, VRON1
Fine adjustment	KP0 [2:0]	KN0 [2:0]	8-to-1 selector (voltage level of grayscale 1)
	KP1 [2:0]	KN1 [2:0]	8-to-1 selector (voltage level of grayscale 8)
	KP2 [2:0]	KN2 [2:0]	8-to-1 selector (voltage level of grayscale 20)
	KP3 [2:0]	KN3 [2:0]	8-to-1 selector (voltage level of grayscale 43)
	KP4 [2:0]	KN4 [2:0]	8-to-1 selector (voltage level of grayscale 55)
	KP5 [2:0]	KN5 [2:0]	8-to-1 selector (voltage level of grayscale 62)

Ladder resistors and 8-to-1 selector Block configuration

The reference voltage generating block consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the **γ-**correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels.

Variable resistors

ILI9320 uses variable resistors of the following three purposes: gradient adjustment (VRCP(N)0/VRCP(N)1); amplitude adjustment (1) (VROP(N)0); and the amplitude adjustment (2) (VROP(N)1). The resistance values of these variable resistors are set by gradient adjustment registers and amplitude adjustment registers as follows.

Gradient adjustment		Amplitude adjustment (1)		Amplitude adjustment (2)	
PRP(N)0/1[2:0] Register	VRCP(N)0 Resistance	VRP(N)0[4:0] Register	VROP(N)0 Resistance	VRP(N)1[4:0] Register	VROP(N)1 Resistance
000	0R	00000	0R	00000	0R
001	4R	00001	2R	00001	1R
010	8R	00010	4R	00010	2R
011	12R	:	:	:	:
100	16R	:	:	:	:
101	20R	11101	58R	11101	29R
110	24R	11110	60R	11110	30R
111	28R	11111	62R	11111	31R

8-to-1 selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register and output the selected voltage level as a reference grayscale voltage (VgP(N)1~6). The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages.

Fine adjustment registers and selected voltage						
Register	Selected Voltage					
KP(N)[2:0]	VgP(N)1	VgP(N)8	VgP(N)20	VgP(N)43	VgP(N)55	VgP(N)62
000	VP(N)1	VP(N)9	VP(N)17	VP(N)25	VP(N)33	VP(N)41
001	VP(N)2	VP(N)10	VP(N)18	VP(N)26	VP(N)34	VP(N)42
010	VP(N)3	VP(N)11	VP(N)19	VP(N)27	VP(N)35	VP(N)43
011	VP(N)4	VP(N)12	VP(N)20	VP(N)28	VP(N)36	VP(N)44
100	VP(N)5	VP(N)13	VP(N)21	VP(N)29	VP(N)37	VP(N)45
101	VP(N)6	VP(N)14	VP(N)22	VP(N)30	VP(N)38	VP(N)46
110	VP(N)7	VP(N)15	VP(N)23	VP(N)31	VP(N)39	VP(N)47
111	VP(N)8	VP(N)16	VP(N)24	VP(N)32	VP(N)40	VP(N)48

Source Driver Output (S[384:1])

VCOM

Negative polarity   Postive polarity
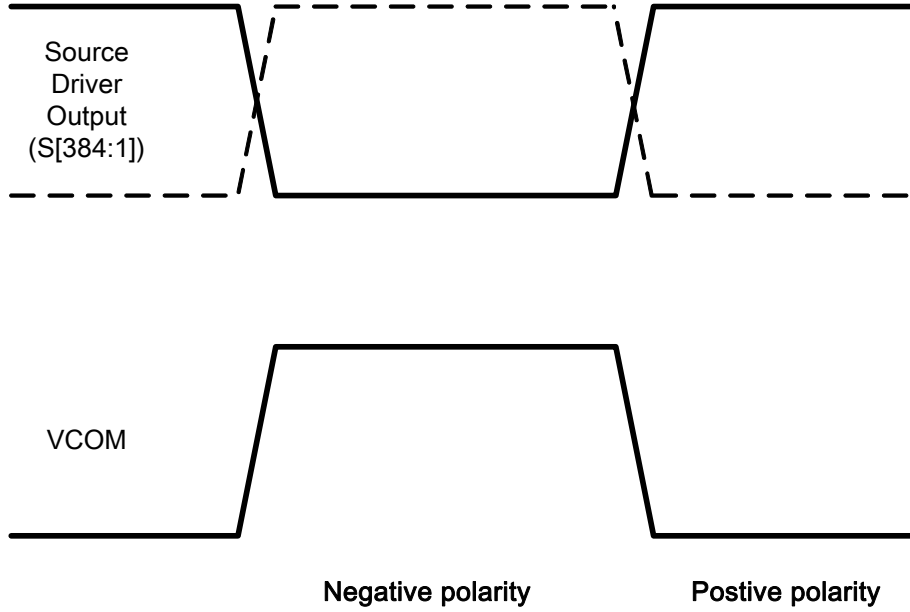
Figure 38 Relationship between Source Output and VCOM

V0

Source Output Levels

Negative Polarity

Positive Polarity

V63

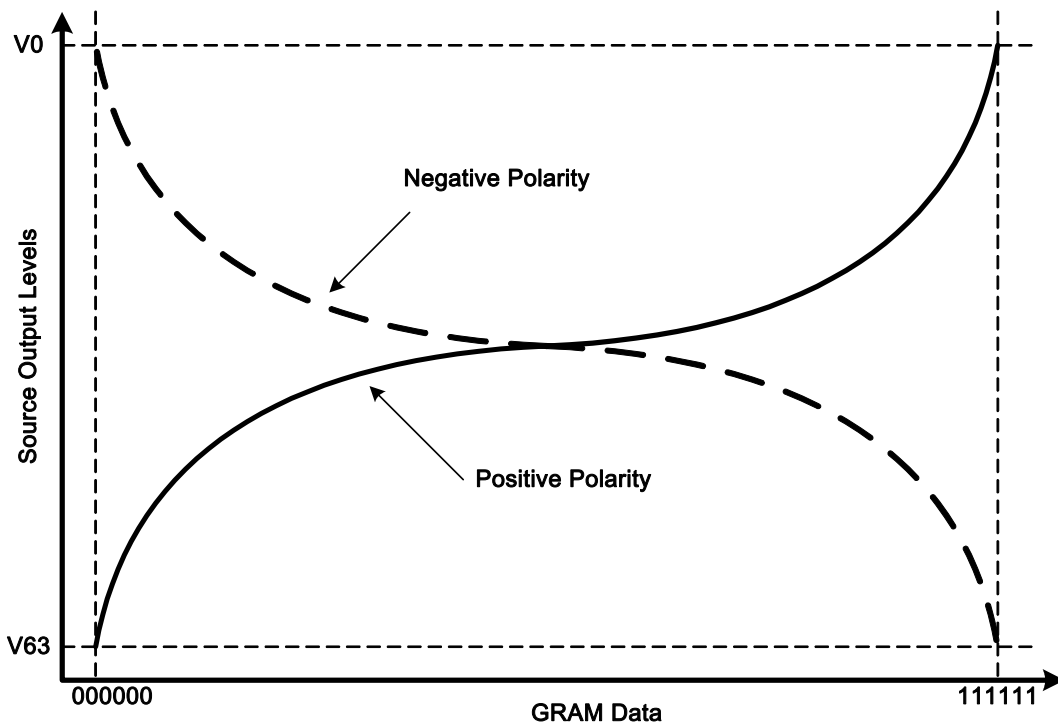000000   GRAM Data   111111

Figure 39 Relationship between GRAM Data and Output Level

12. Application

12.1. Configuration of Power Supply Circuit
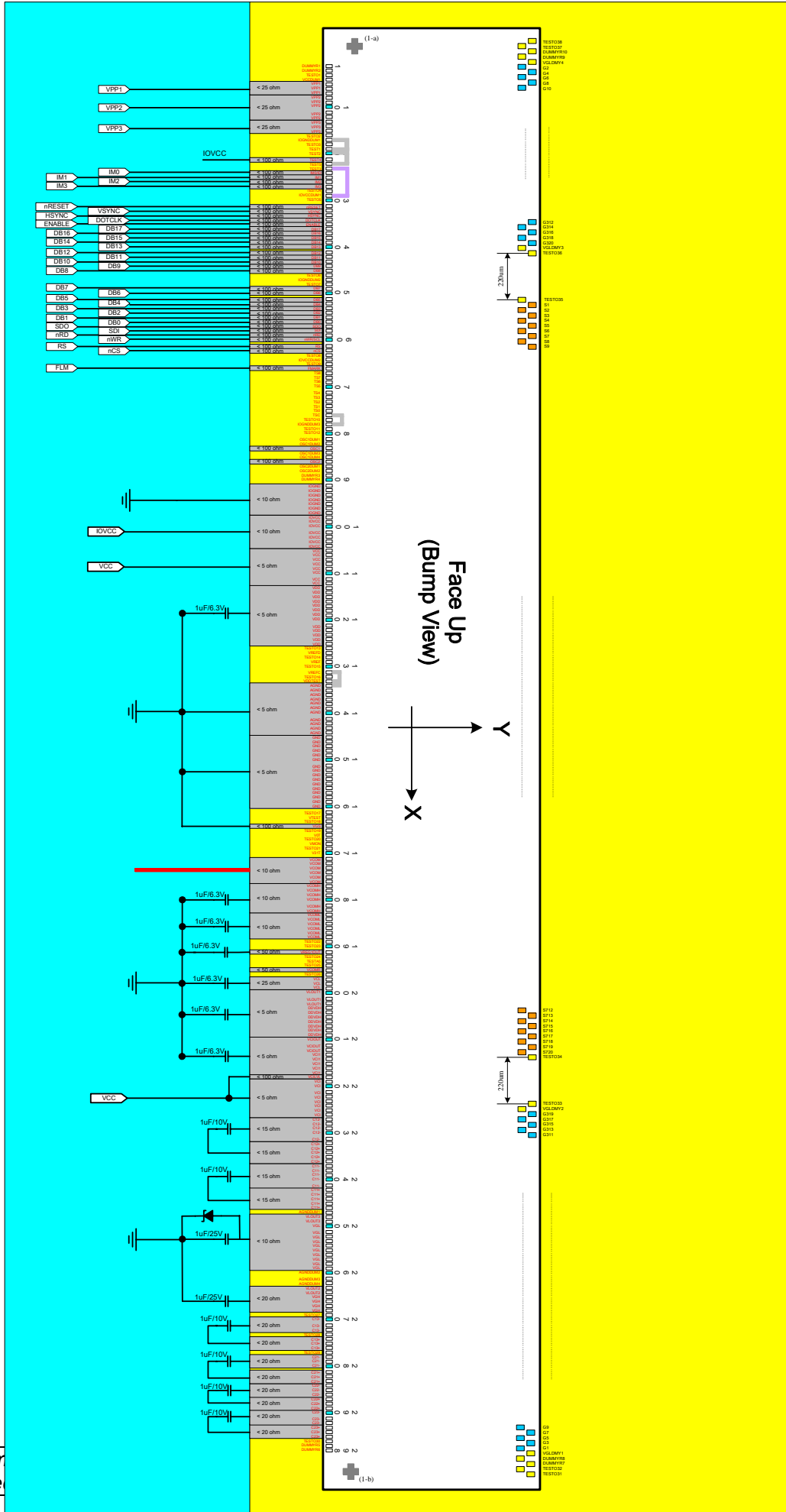
Face Up
(Bump View)

Figure 40 Power Supply Circuit Block

The following table shows specifications of external elements connected to the ILI9320's power supply circuit.

Items	Recommended Specification	Pin connection
Capacity 1 µF (B characteristics)	6V	VREG1OUT, VCI1, VDD, VCL, VCOMH, VCOML, C11+/-, C12+/-
	10V	DDVDH, C21+/-, C22+/-, C23+/-
	25V	VGH, VGL
Schottky diode	VF<0.4V/20mA at 25°C, VR ≥30V (Recommended diode: HSC226)	(AGND – VGL), (Vci – VGH), (Vci – DDVDH)
Variable resistor	> 200 kΩ	VCOMR

12.2. Display ON/OFF Sequence

Display Off Flow

Display On Flow

```
Display Off Flow                          Display On Flow

      |                                    ╭──────────────╮
      ▼                                    │ Power Setting │
┌──────────────┐                           ╰──────────────╯
│ Display OFF  │                                  │
│              │                                  ▼
│  GON = 1     │                           ┌──────────────┐
│  DTE = 1     │                           │  Display On   │
│  D[1:0] = 10 │                           │               │
└──────────────┘                           │  BASEE=0      │
      │                                    │  GON = 1      │
      ▼                                    │  DTE = 0      │
┌──────────────┐                           │  D[1:0] = 01  │
│Wait for 2    │                           └──────────────┘
│frames or more│                                  │
└──────────────┘                                  ▼
      │                                    ┌──────────────┐
      ▼                                    │Wait for 2     │
┌──────────────┐                           │frames or more │
│ Display OFF  │                           └──────────────┘
│              │                                  │
│  GON = 0     │                                  ▼
│  DTE = 0     │                           ┌──────────────┐
│  D[1:0] = 00 │                           │  Display On   │
└──────────────┘                           │               │
      │                                    │  BASEE=1      │
      ▼                                    │  GON = 1      │
┌──────────────┐                           │  DTE = 1      │
│Power Supply  │                           │  D[1:0] = 11  │
│Off           │                           └──────────────┘
│              │                                  │
│  SAP = 0     │                                  ▼
│  APE=0       │                            ╭──────────────╮
│  AP[2:0]=000 │                            │  Display ON   │
│  PON = 0     │                            ╰──────────────╯
└──────────────┘
      │
      ▼
 ╭──────────────╮
 │  Display Off  │
 ╰──────────────╯
```
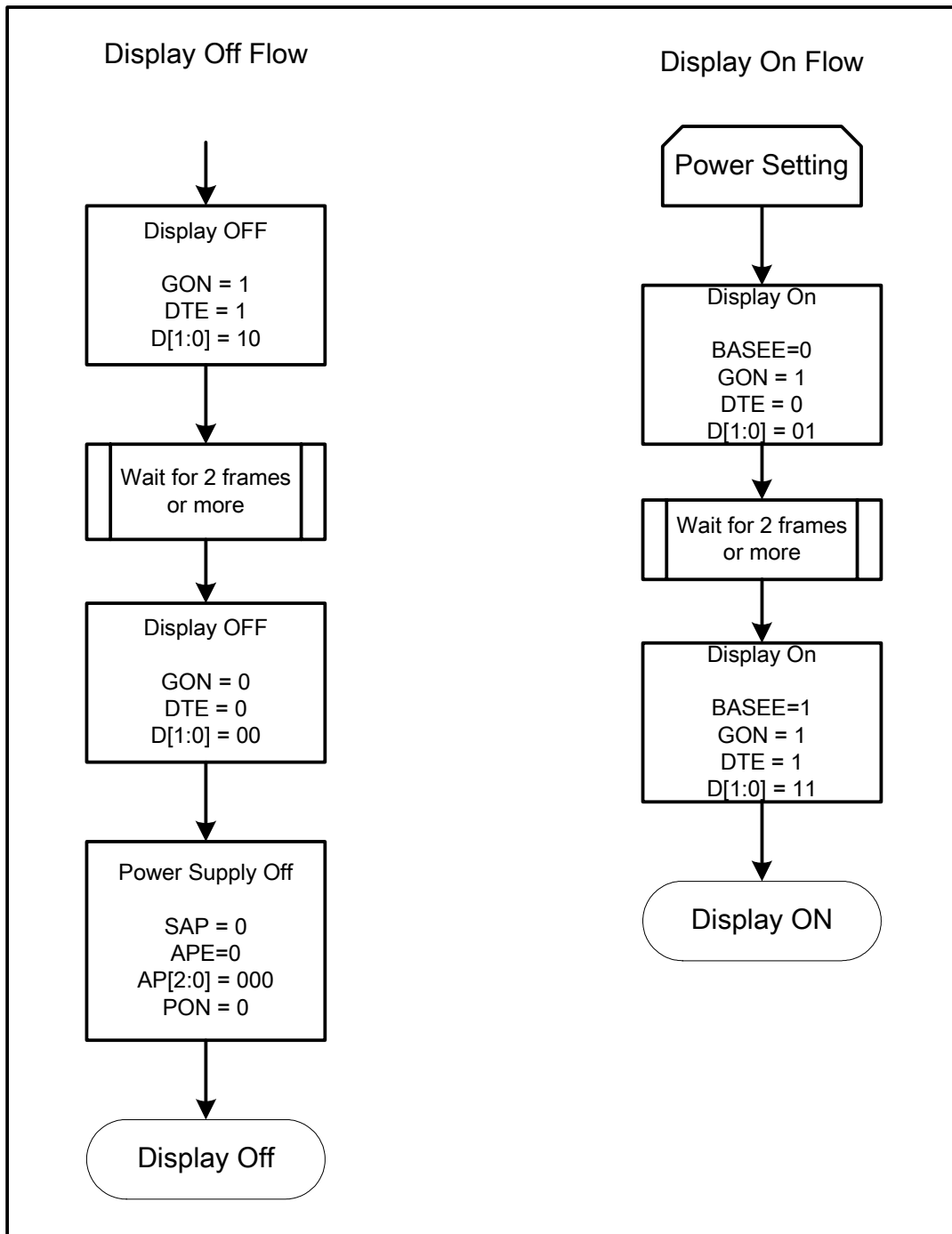
Figure 41 Display On/Off Register Setting Sequence
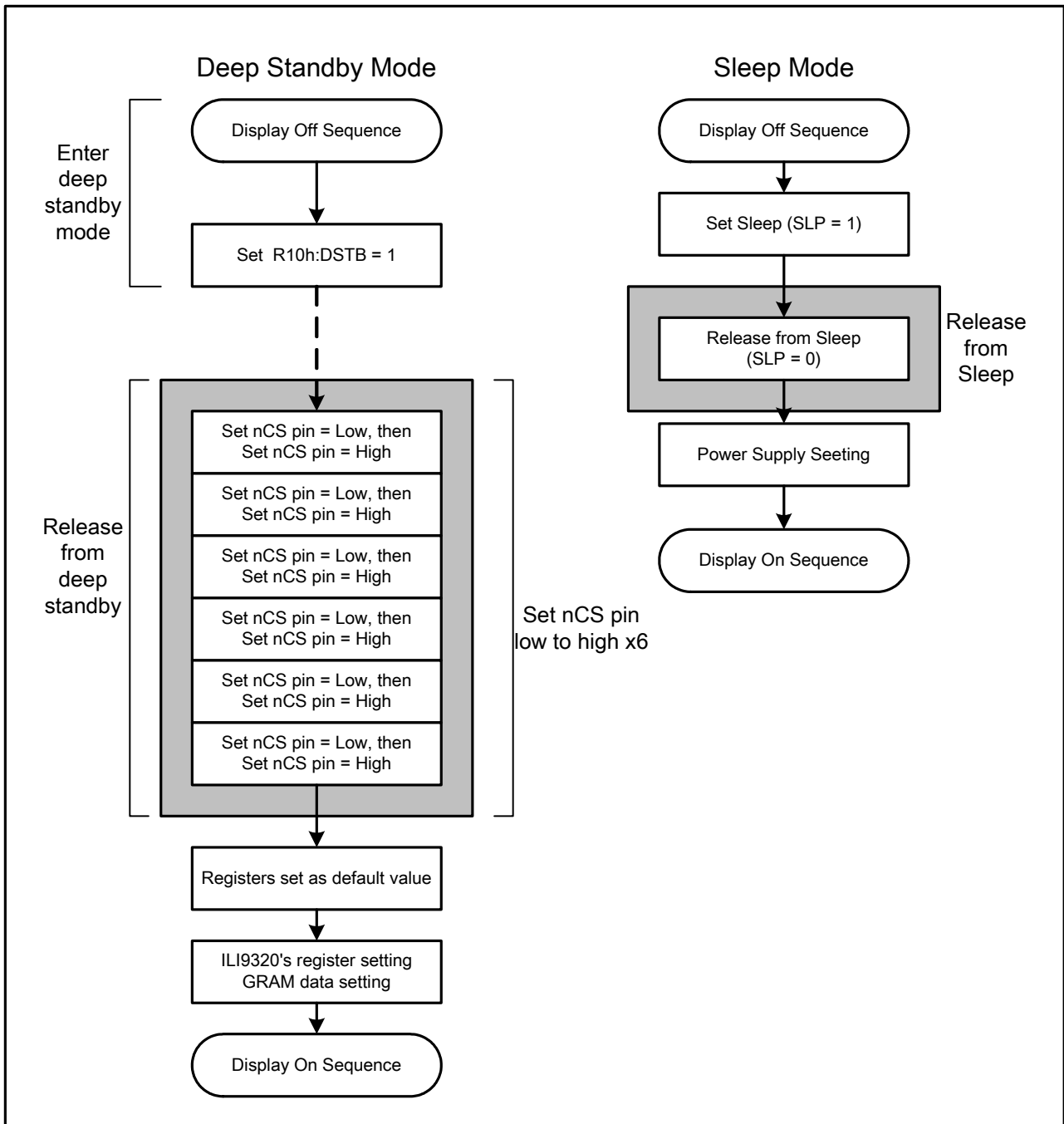
12.3. Deep Standby and Sleep Mode

Figure 42 Deep Standby/Sleep Mode Register Setting Sequence

12.4. Power Supply Configuration

When supplying and cutting off power, follow the sequence below. The setting time for oscillators, step-up circuits and operational amplifiers depends on external resistance and capacitance.
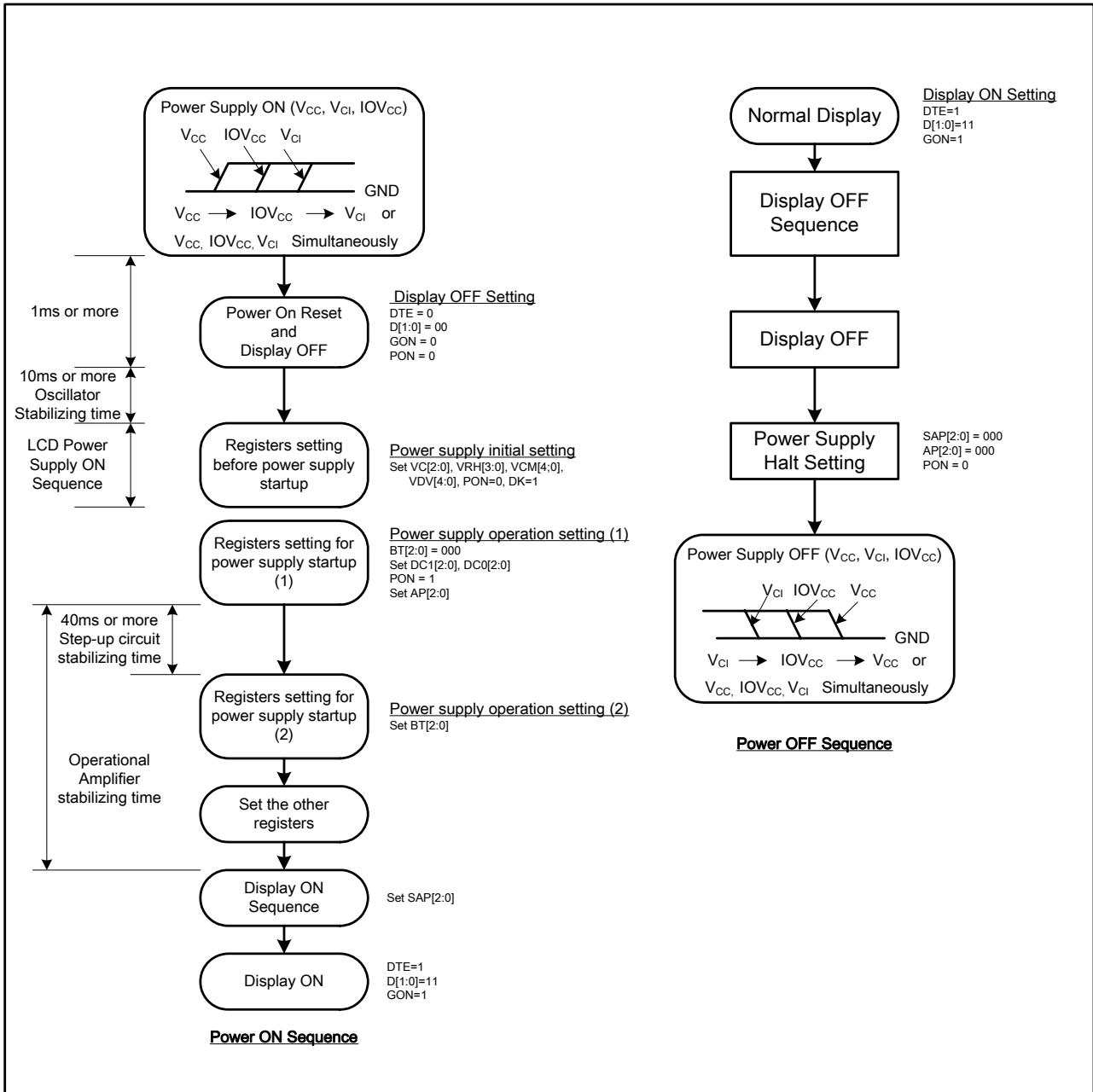

Figure 43 Power Supply ON/OFF Sequence

12.5. Voltage Generation

The pattern diagram for setting the voltages and the waveforms of the voltages of the ILI9320 are as follows.
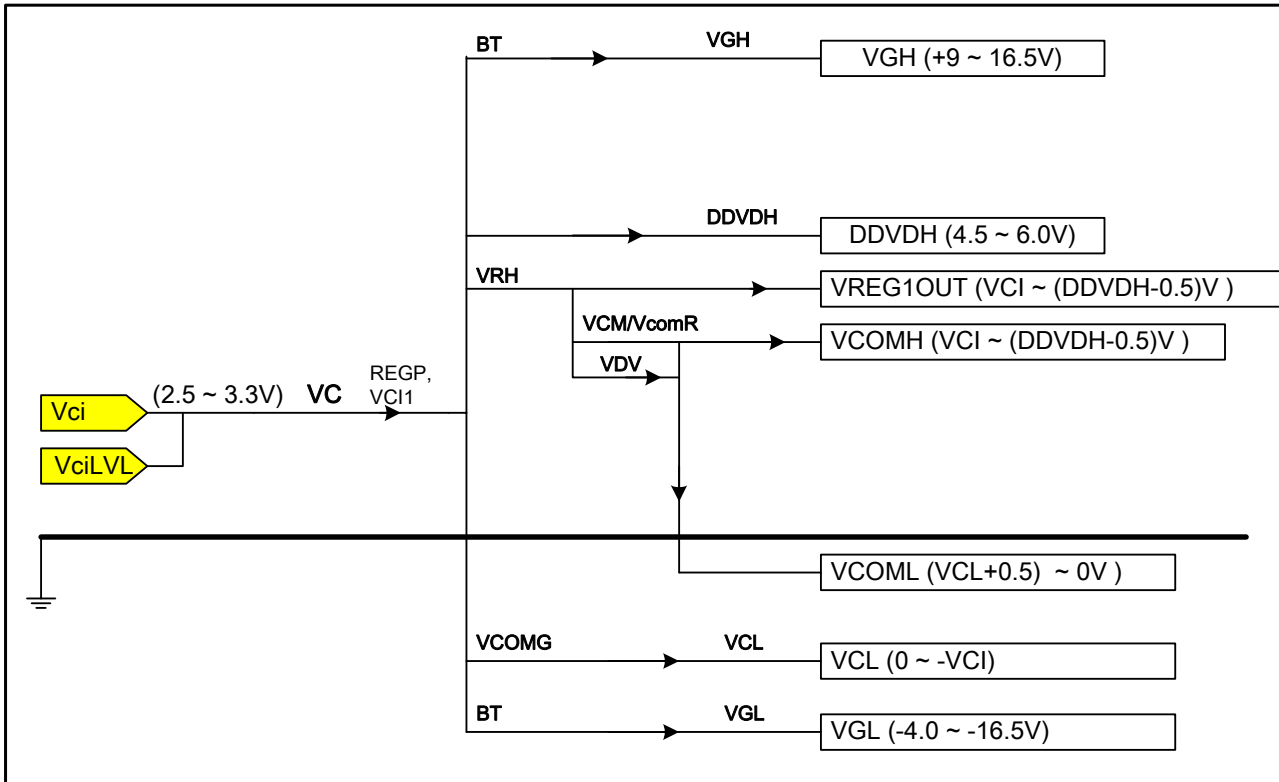
Figure 44 Voltage Configuration Diagram

Note: The DDVDH, VGH, VGL, and VCL output voltage levels are lower than their theoretical levels (ideal voltage levels) due to current consumption at respective outputs. The voltage levels in the following relationships (DDVDH – VREG1OUT) > 0.5V, (VCOML – VCL) > 0.5V, (VCOML – VCL) > 0.5V are the actual voltage levels. When the alternating cycles of VCOM are set high (e.g. the polarity inverts every line cycle), current consumption is large. In this case, check the voltage before use.

12.6. Applied Voltage to the TFT panel
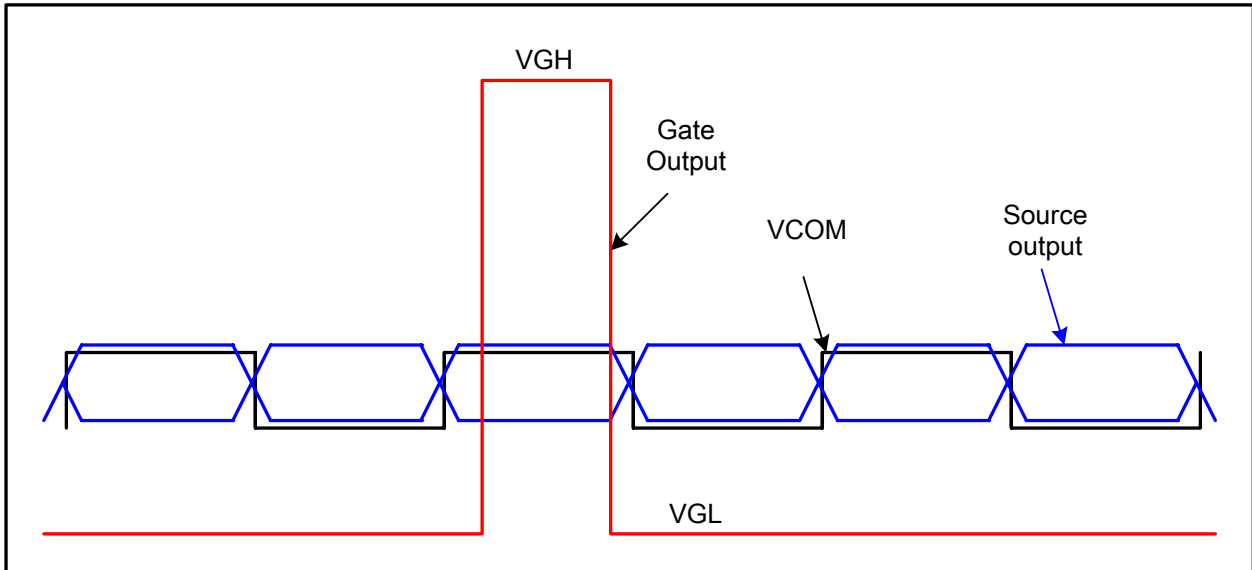
Figure 45 Voltage Output to TFT LCD Panel

12.7. Oscillator

ILI9320 generates oscillation with the ILI9320's internal RC oscillators by placing an external resistor between the OSC1 and OSC2 pins. The oscillation frequency varies with resistance value of external resistor, wiring distance, and operating supply voltage. For example, placing a Rosc resistor of larger resistance value or lower the supply voltage level will generate a lower oscillation frequency. See the "Notes to Electrical Characteristics" section for the relationship between resistance value of Rosc resistor and oscillation frequency.
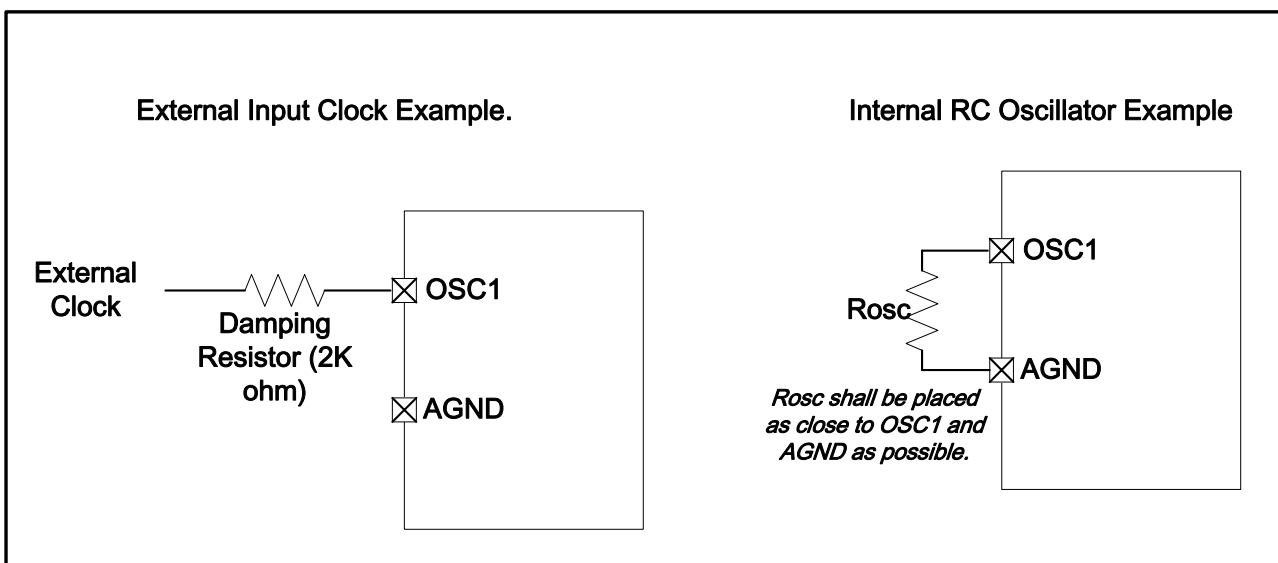
Figure 46 Oscillation Connection

The information contained herein is the exclusive property of ILI Technology Corp. and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of ILI Technology Corp.

12.8. Frame Rate Adjustment

The ILI9320 has a frame frequency adjustment function. The frame frequency for driving LCDs can be adjusted by registers (using the DIV, RTN bits) without changing the oscillation frequency.

To switch frame frequencies between when displaying a moving picture and when displaying a still picture, set a high oscillation frequency in advance. By doing so, it becomes possible to set a low frame frequency when displaying a still picture for saving power consumption and to set a high frame frequency when displaying a moving picture.

Relationship between Liquid Crystal Drive Duty and Frame Frequency

The relationship between the liquid crystal drive duty and the frame frequency is calculated from the following formula. The frame frequency is adjusted by register using the 1H period adjustment bits (RTN bits) and the operation clock division bits (DIV bits).

Formula to calculate frame frequency

$$ Formula\ rate\ =\ \frac{f_{osc.}}{Clock\ cycles\ per\ line\ \times\ division\ ratio\ \times\ (Lines\ +BP+FP)} $$

$f_{osc.}$: frequency if RC oscillation.
Clock cycles per line : RTN bits
Division ratio : DIV bits
Lines : number of lines for driving the LCD panel.
FP: Front porch lines
BP; Back porch lines

Example of Calculation: when maximum frame frequency = 60 Hz

Number of lines to drive the LCD: 320 lines

1H period: 16 clock cycle (RTNI[4:0] = "00000")

Operational clock division ratio: 1/1

   fosc = 60 Hz × (0 + 16) clock × 1/1 × (320 + 16) lines = 322.56 (kHz)

In this case, the RC oscillation frequency is 322.56kHz. Adjust the external resistor of the RC oscillator to 322.56kHz.

12.9. Partial Display Function

The ILI9320 allows selectively driving two partial images on the screen at arbitrary positions set in the screen drive position registers.

The following example shows the setting for partial display function:

Base Image Display Setting	
BASEE	0
NL[5:0]	6'h27

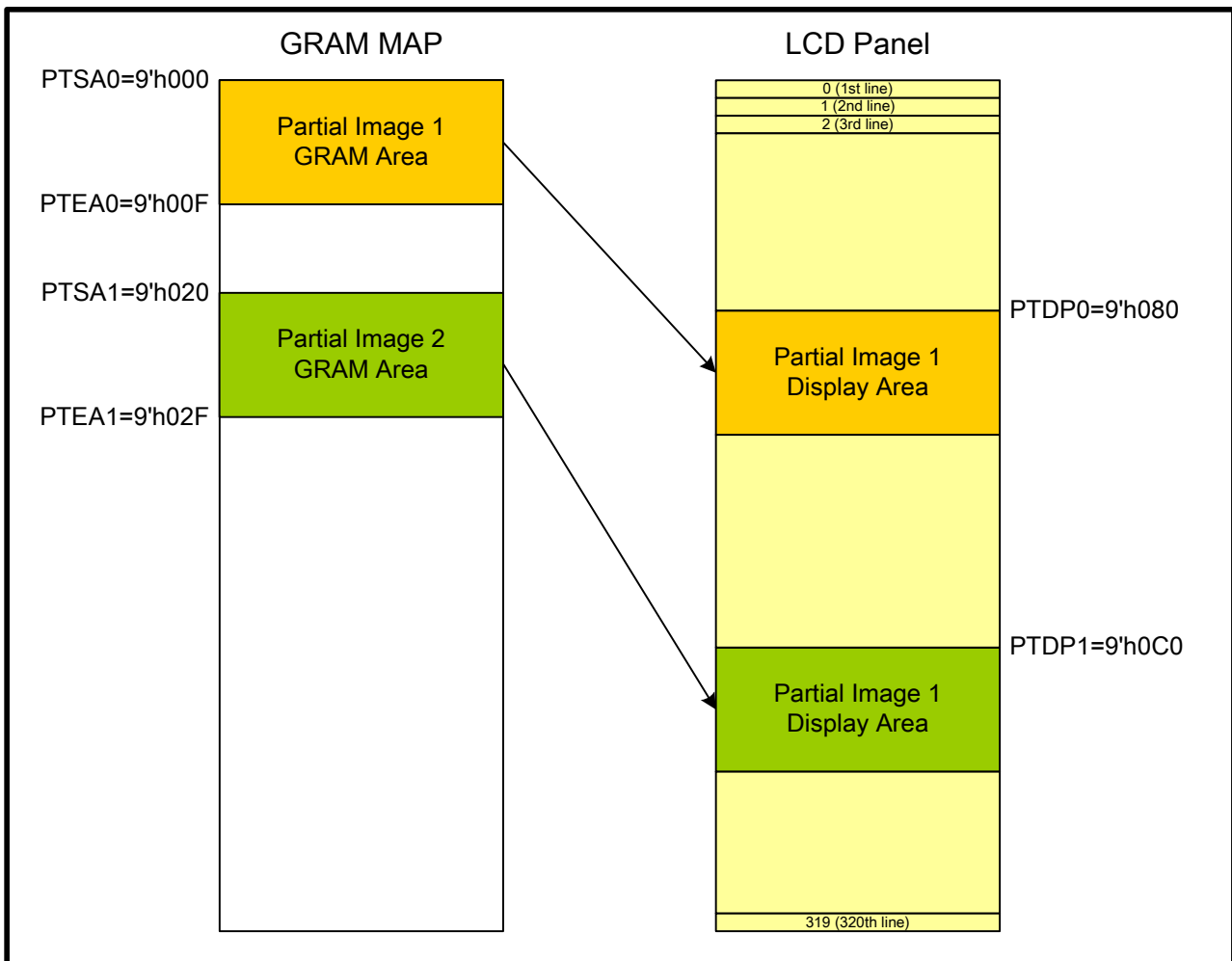| Partial Image 1 Display Setting	
PTDE0	1
PTSA0[8:0]	9'h000
PTEA0[8:0]	9'h00F
PTDP0[8:0]	9'h080
Partial Image 2 Display Setting	
PTDE1	1
PTSA1[8:0]	9'h020
PTEA1[8:0]	9'h02F
PTDP1[8:0]	9'h0C0

GRAM MAP   LCD Panel

PTSA0=9'h000

Partial Image 1
GRAM Area

PTEA0=9'h00F

PTSA1=9'h020

Partial Image 2
GRAM Area

PTEA1=9'h02F

0 (1st line)
1 (2nd line)
2 (3rd line)

PTDP0=9'h080

Partial Image 1
Display Area

PTDP1=9'h0C0

Partial Image 1
Display Area

319 (320th line)

Figure 47 Partial Display Example

12.10. Resizing Function

ILI9320 supports resizing function (x1/2, x1/4), which is performed when writing image data to GRAM. The

resizing function is enabled by setting a window address area and the RSZ bit which represents the resizing factor (x1/2, x1/4) of image. The resizing function allows the system to transfer the original-size image data into the GRAM with resized image data.
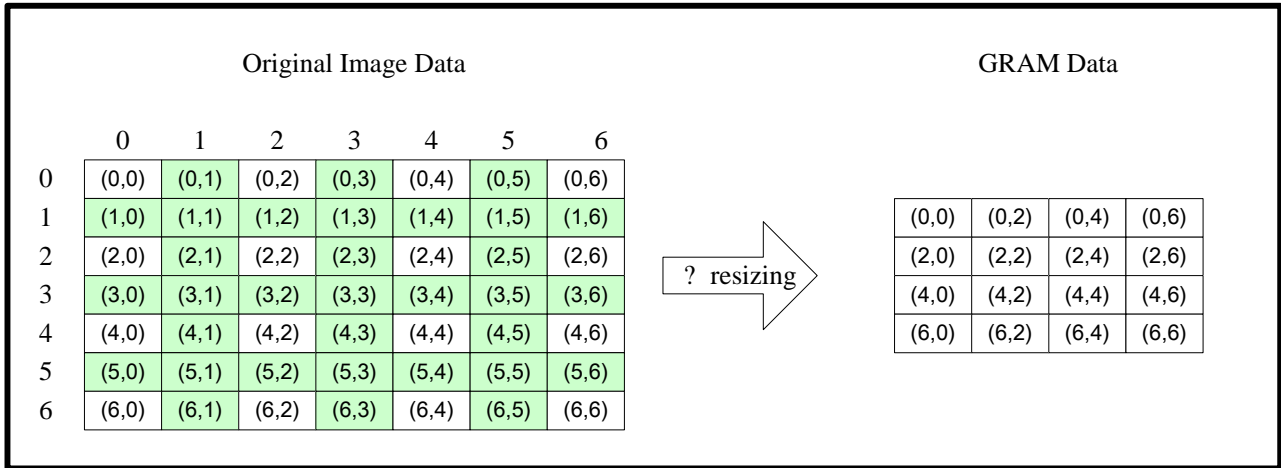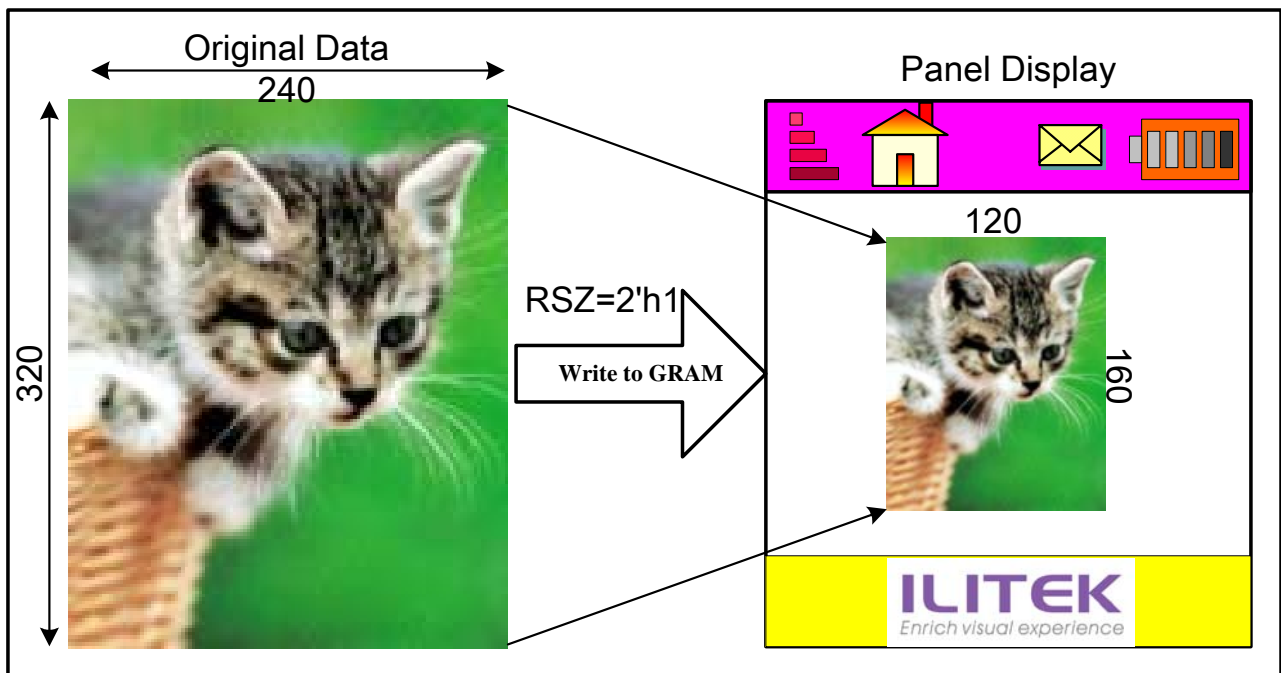

Figure 48 Data transfer in resizing

Figure 49 Resizing Example

Original Image Size (X × Y)	Resized Image Resolution	
	1/2 (RSZ=2'h1)	1/4 (RSZ=2'h3)
640 × 480	320 × 240	160 × 120
352 × 288	176 × 144	88 × 72
320 × 240	160 × 120	80× 60
176 × 144	88 × 72	44× 36
120 × 160	60× 80	30 × 40
132 × 132	66 × 66	33 × 33

The RSZ bit sets the resizing factor of an image. When setting a window address area in the internal GRAM, the GRAM window address area must fit the size of resized image. The following example show the resizing setting.

$$dx = (X-H)/N, \quad H = X \bmod N$$
$$dy = (Y-V)/N, \quad V = Y \bmod N$$
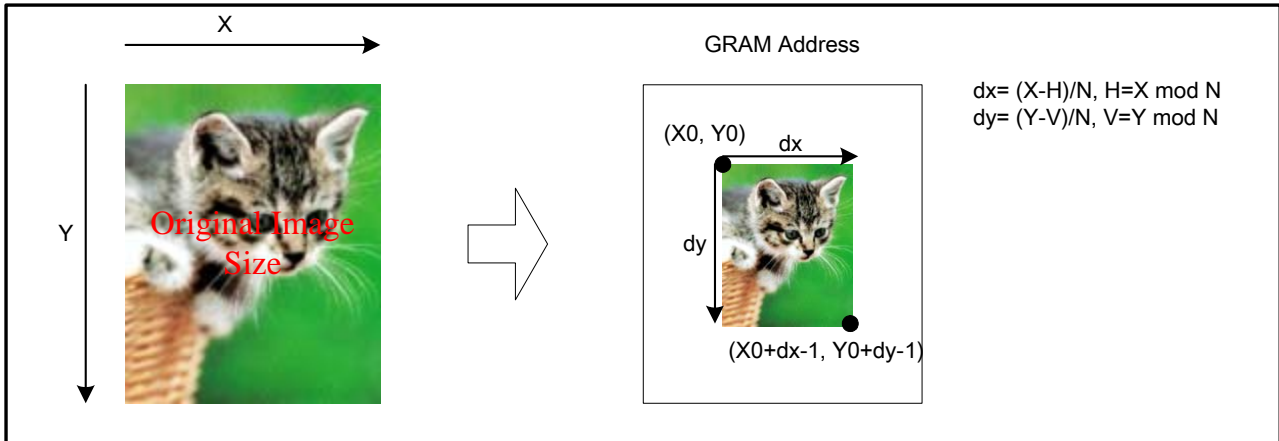
Original image data number in horizontal direction		X
Original image data number in Vertical direction		Y
Resizing Ration		1/N
Resizing Setting	RSZ	N-1
Remainder pixels in horizontal direction	RCH	H
Remainder pixels in vertical direction	RCV	V
GRAM writing start address	AD	(x0, y0)
GRAM window setting	HSA	x0
	HEA	x0+dx-1
	VSA	y0
	VEA	y0+dy-1

13. Electrical Characteristics

13.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9320 is used out of the absolute maximum ratings, the ILI9320 may be permanently damaged. To use the ILI9320 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ILI9320 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power supply voltage (1)	VCC, IOVCC	V	-0.3 ~ + 4.6	1, 2
Power supply voltage (1)	VCI - AGND	V	-0.3 ~ + 4.6	1, 4
Power supply voltage (1)	DDVDH - AGND	V	-0.3 ~ + 6.0	1, 4
Power supply voltage (1)	AGND -VCL	V	-0.3 ~ + 4.6	1
Power supply voltage (1)	DDVDH - VCL	V	-0.3 ~ + 9.0	1, 5
Power supply voltage (1)	VGH - AGND	V	-0.3 ~ + 18.5	1, 5
Power supply voltage (1)	AGND - VGL	V	-0.3 ~ + 18.5	1, 6
Input voltage	Vt	V	-0.3 ~ VCC+ 0.3	1
Operating temperature	Topr	°C	-40 ~ + 85	8, 9
Storage temperature	Tstg	°C	-55 ~ + 110	8, 9

Notes:
1. VCC,DGND must be maintained
2. (High) (VCC = VCC) ≥ DGND (Low), (High) IOVCC ≥ DGND (Low).
3. Make sure (High) VCI ≥ DGND (Low).
4. Make sure (High) DDVDH ≥ ASSD (Low).
5. Make sure (High) DDVDH ≥ VCL (Low).
6. Make sure (High) VGH ≥ ASSD (Low).
7. Make sure (High) ASSD ≥ VGL (Low).
8. For die and wafer products, specified up to 85°C.
9. This temperature specifications apply to the TCP package

13.2. DC Characteristics

(VCC = 2.40 ~ 3.30V, IOVCC = 1.65 ~ 3.30V, Ta= -40 ~ 85 °C)

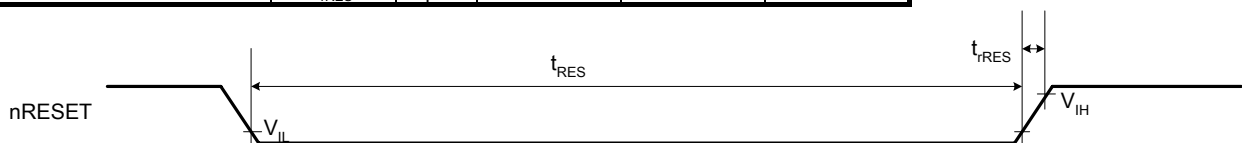| Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V_{IH}	V	VCC= 1.8 ~ 3.3V	0.8*IOVCC	-	IOVCC	-
Input low voltage	V_{IL}	V	VCC= 1.8 ~ 3.3V	-0.3	-	0.2*IOVCC	-
Output high voltage(1) (DB0-17 Pins)	V_{OH1}	V	IOH = -0.1 mA	0.8*IOVCC	-	-	-
Output low voltage (DB0-17 Pins)	V_{OL1}	V	IOVCC=1.65~3.3V VCC= 2.4 ~ 3.3V IOL = 0.1mA	-	-	0.2*IOVCC	-
I/O leakage current	I_{LI}	µA	Vin = 0 ~ VCC	-0.1	-	0.1	-
Current consumption during normal operation (V_{CC} – DGND)	I_{OP}	µA	VCC=2.8V , Ta=25°C , fOSC = 376KHz (Line) GRAM data = 0000h	-	100 (VCC)	-	-
Current consumption during standby mode (V_{CC} – DGND)	I_{ST}	µA	VCC=2.8V , Ta=25 °C	-	5	10	-
LCD Drive Power Supply Current (DDVDH-DGND)	ILCD	mA	VCC=2.8V , VREG1OUT =4.8V DDVDH=5.0V , fOSC = 376KHz (320 line) , Ta=25 °C, GRAM data = 0000h, REV="0", SAP="001", ON4-0="0", OP4-0="0", MP52-00="0", MN52-00="0", CP12-00="0" CN12-00="0	-	3.0	-	-
LCD Driving Voltage (DDVDH-DGND)	DDVDH	V	-	4.5	-	6	-
Output voltage deviation		mV	-	-	5	-	-
Dispersion of the Average Output Voltage	V	mV	-	-10	-	10	-

13.3. Clock Characteristics

VCC = 2.40 ~ 3.30V, IOVCC = 1.65 ~ 3.30V

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
External Clock Frequency	fcp	VCC = 2.4 ~ 3.3V	450	550	650	KHz
External Clock Duty	f_{Duty}	VCC = 2.4 ~ 3.3V	45	50	55	
External Clock Rising Time	Trcp	VCC = 2.4 ~ 3.3V	-	-	0.2	µs
External Clock Falling Time	Tfcp	VCC = 2.4 ~ 3.3V	-	-	0.2	µs
RC oscillation clock	f_{OSC}	Rf = 100KΩ, VCC = 2.8V	450	550	650	KHz

13.4. Reset Timing Characteristics

Reset Timing Characteristics (VCC = 1.8 ~ 3.3 V, IOVCC = 1.65 ~ 3.3 V)

Item	Symbol	Unit	Min.	Typ.	Max.
Reset low-level width	t_{RES}	ms	1	-	-
Reset rise time	t_{rRES}	µs	-	-	10

13.5. LCD Driver Output Characteristics

Item	Symbol	Timing diagram	Min.	Typ.	Max.	Unit
Driver output delay time	tdd	VCC=2.8V, DDVDH=5.0V, VREG1OUT =4.8V, RC oscillation: fosc =376kHz (320 lines), Ta=25°C REV=0, SAP=010, AP=010, 0N14-00=0, 0P14-00=0, MP52-00=0, MN52-00=0, CP12-00=0, CN12-00=0, Load resistance R=10kΩ, Load capacitance C=20pF • when the level changes from a same grayscale level on all pins • Time to reach +/-35mV when VCOM polarity inverts	-	35	-	µs

13.6. AC Characteristics

13.6.1. i80-System Interface Timing Characteristics

Normal Write Mode (IOVCC = 1.65~3.3V, VCC=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	100	-	-	-
	Read	t_{CYCR}	ns	300	-	-	-
Write low-level pulse width		PW_{LW}	ns	50	-	500	-
Write high-level pulse width		PW_{HW}	ns	50	-	-	-
Read low-level pulse width		PW_{LR}	ns	150	-	-	-
Read high-level pulse width		PW_{HR}	ns	150	-	-	
Write / Read rise / fall time		t_{WRr}/t_{WRf}	ns	-	-	25	
Setup time	Write (RS to nCS, E/nWR)	t_{AS}	ns	10	-	-	
	Read (RS to nCS, RW/nRD)			5	-	-	
Address hold time		t_{AH}	ns	5	-	-	
Write data set up time		t_{DSW}	ns	10	-	-	
Write data hold time		t_{H}	ns	15	-	-	
Read data delay time		t_{DDR}	ns	-	-	100	
Read data hold time		t_{DHR}	ns	5	-	-	

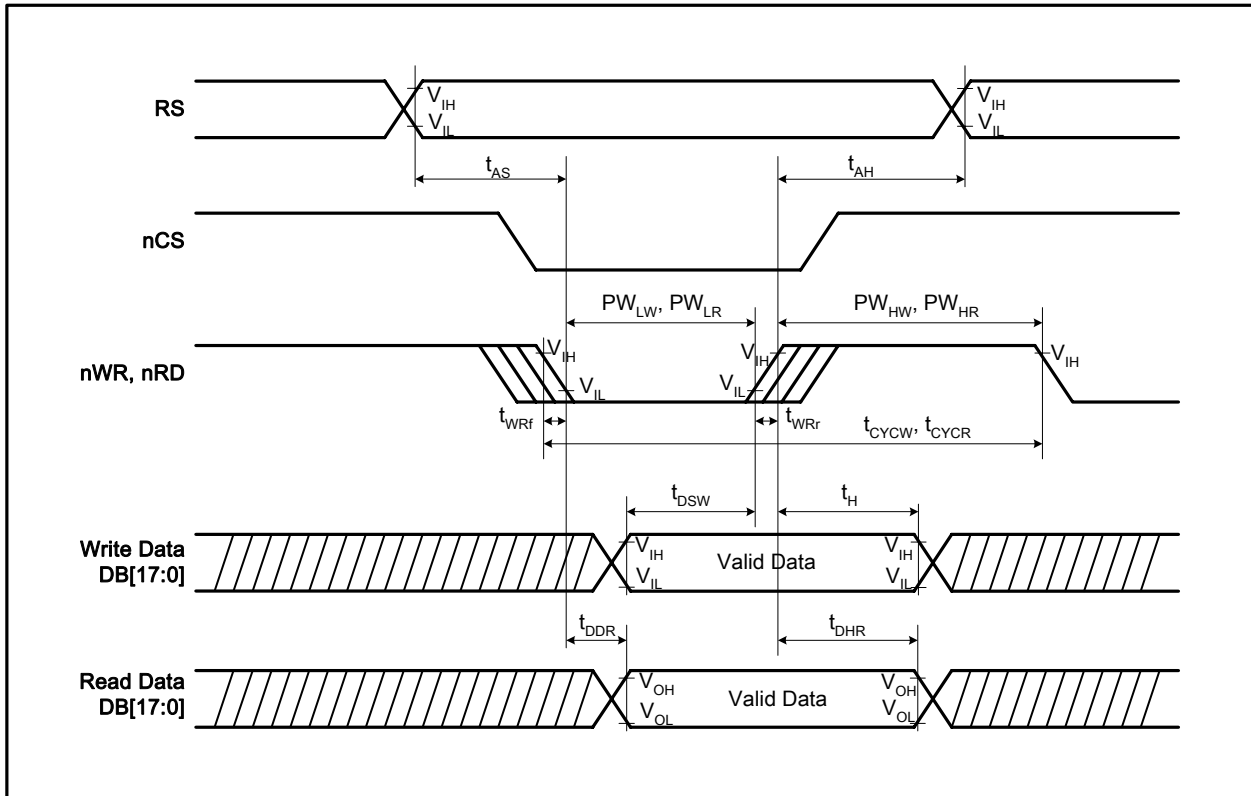**Figure 50 i80-System Bus Timing**

13.6.2. Serial Data Transfer Interface Timing Characteristics

(IOVCC= 1.653.3V and VCC=2.4~3.3V)

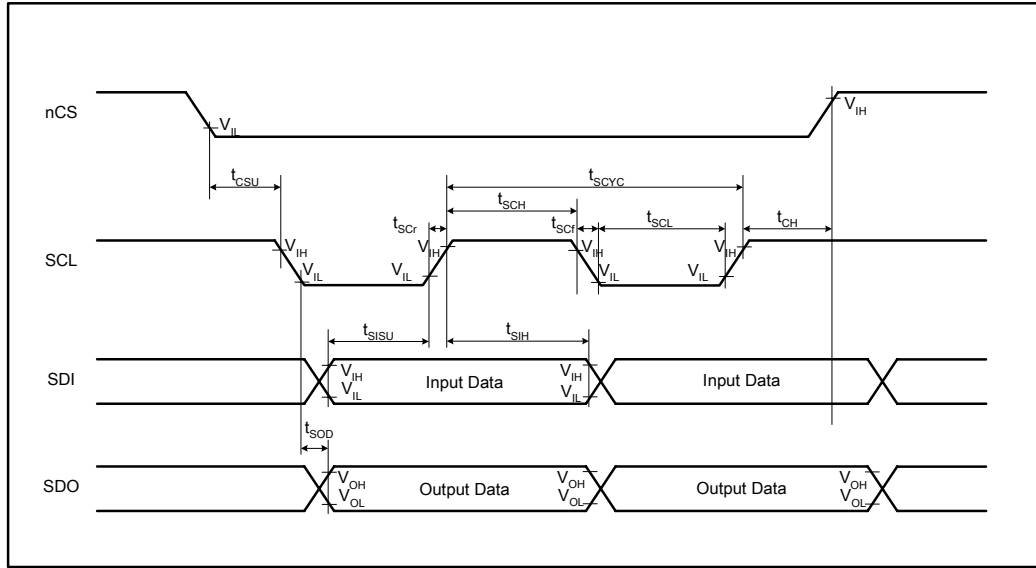| Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Serial clock cycle time	Write (received)	t_{SCYC}	ns	100	-	-	
	Read (transmitted)	t_{SCYC}	ns	200	-	-	
Serial clock high – level pulse width	Write (received)	t_{SCH}	ns	40	-	-	
	Read (transmitted)	t_{SCH}	ns	100	-	-	
Serial clock low – level pulse width	Write (received)	t_{SCL}	ns	40	-	-	
	Read (transmitted)	t_{SCL}	ns	100	-	-	
Serial clock rise / fall time		t_{SCr}, t_{SCf}	ns	-	-	5	
Chip select set up time		t_{CSU}	ns	10	-	-	
Chip select hold time		t_{CH}	ns	50	-	-	
Serial input data set up time		t_{SISU}	ns	20	-	-	
Serial input data hold time		t_{SIH}	ns	20	-	-	
Serial output data set up time		t_{SOD}	ns	-	-	100	
Serial output data hold time		t_{SOH}	ns	5	-	-	

Figure 51 SPI System Bus Timing

13.6.3. RGB Interface Timing Characteristics

18/16-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V, VCC=2.4~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	10	-	-	-
ENABLE hold time	t_{ENH}	ns	10	-	-	-
PD Data setup time	t_{PDS}	ns	10	-	-	-
PD Data hold time	t_{PDH}	ns	40	-	-	-
DOTCLK high-level pulse width	PWDH	ns	40	-	-	-
DOTCLK low-level pulse width	PWDL	ns	40	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	100	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rghr}, t_{rghf}	ns	-	-	25	-

6-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V, VCC=2.4~3.3V)

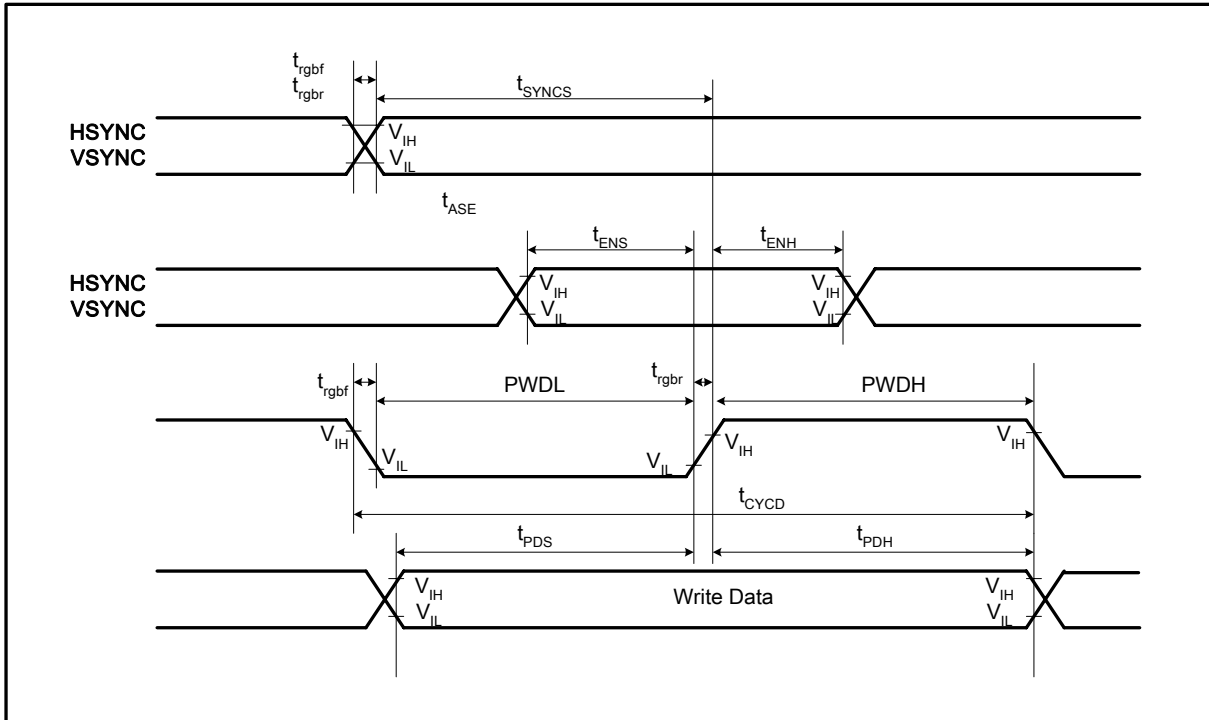| Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	10	-	-	-
ENABLE hold time	t_{ENH}	ns	10	-	-	-
PD Data setup time	t_{PDS}	ns	10	-	-	-
PD Data hold time	t_{PDH}	ns	30	-	-	-
DOTCLK high-level pulse width	PWDH	ns	30	-	-	-
DOTCLK low-level pulse width	PWDL	ns	30	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	80	-	-	-
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rghr}, t_{rghf}	ns	-	-	25	-

Figure52 RGB Interface Timing

14. Revision History

Version No.	Date	Page	Description
V0.1	2006/4/17		New Created
V0.41	2006/11/17		Modify the SPI interface.
V0.44	2006/11/17		Modify the OSC. description section, The internal resistor is used in the default setting.
V0.45	2006/12/27		1. Modify the VCOMR description. Let this pin as open when it's unused. 2. The unused interface pins are shorted to DGND. 3. Dithering function removed.
V0.46	2007/1/31	13	1. Modify the VCCDUM1, DUMMYR1~10, TEST3, TEST4, TSC pins connection.
V0.47	2007/3/16		Add the thickness of chip by customer order
V0.49	2007/05/09		Modify 16/9/8 bit System interface type error
V0.51	2007/6/20		Modify VPP3 pins connection to GND or floating.