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Application Note

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Kinetis KLx6/KL34 to Kinetis KL43/KL33/KL27/KL17 Migration Guide

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1 Introduction

This document describes the details of migrating from Kinetis KLx6/KL34 to Kinetis KL43/KL33/KL27/KL17 microcontrollers. Migrating between the two devices within the same family can require hardware and/or software changes in some cases. Changes that might be required are described in this document. Note that “x” in the name KLx6 does not include the lowest family devices, KL06 and KL03.

Contents

2 Part numbering and mask set information

Table 1 lists all of the KLx6 mask sets that have been produced as of the writing of this document. Table 2 shows the device mask set and a part number example for the devices which will be the source of the migration.

Table 1. KLx6/KL34 mask sets

Revision	Mask Set	Part Number Example
1.0	0N40H	MKL46Z256VLH4

Table 2. KL43/KL33/KL27/KL17 mask sets

Revision	Mask Set	Part Number Example
1.1	1N71K	MKL43Z256VLH4

This document is primarily focused on migration from KLx6/KL34 devices to KL17/KL27/KL33/KL43 devices within the same Kinetis family. For example, this document will help if you are migrating from MKL46Z256VLH4 to a MKL43Z256VLH4. However, this document does not focus on addressing the changes in functionality between the Kinetis L families, for example between MKL17Z128VLH4 and MKL33Z128VLH4.

3 About this document

This document describes migration between Kinetis KLx6/KL34 to Kinetis KL43/KL33/KL27/KL17 devices (excluding the KL06 and KL03 families) and is divided into four major sections:

- New modules/features
- Updated modules
- Modules with additional instantiations
- Removed modules

The “new modules/features” section provides a quick overview of modules that are completely new for the KL43/KL33/KL27/KL17 devices. These are modules that do not have any functional equivalent available in the KLx6/KL34 microcontrollers. If any of these new modules will be used in your application, then you will require software changes to use the new module.

The “updated modules” section outlines the modules that have been updated to use newer versions. The overall functionality provided will be similar; however, changes will be required in software. Hardware changes may be required to use the new features.

The “modules with additional instantiations” sections describe modules where the modules themselves have no changes, but there are more instantiations of the module included in the microcontroller.

“Removed modules” briefly describes which modules are not included on KL43/KL33/KL27/KL17 devices.

Color Key	
GREEN	Designates new additions
YELLOW	Designates changes
RED	Designates removals

4 New modules and features

The Kinetis KL43/KL33/KL27/KL17 MCUs have added these features:

- Lite version of the multipurpose clock generator module (MCG Lite)
- Voltage reference module (VREFV1)
- Flexible I/O module (FlexIO)
- Low power UART module (LPUART)

The KL43/KL33/KL27/KL17 MCUs also include ROM memory with Kinetis bootloader implemented. These modules or features are not available on the KLx6/KL34 MCUs. The following sections give an overview of the features of these modules. Applications able to take advantage of these new modules will require software changes, and in some cases hardware changes, to take advantage of the new functionality.

NOTE

Availability of these modules depends on the specific Kinetis device that you are using. Please refer to the reference manual for your Kinetis device for information on which features are available.

4.1 MCG Lite module

This module is not an update to the MCG module available on the KLx6/KL34–it is completely different–however, it does share several configuration registers. The main difference is that the MCG Lite module does not include FLL and PLL. Therefore there are no registers related to FLL and PLL configuration such as MCG_C3 through MCG_C8. The MCG Lite module includes a high frequency internal reference clock (48 MHz HIRC) and low frequency internal reference clocks (2 MHz and 8 MHz LIRC).

The maximum frequency clock source available is 48 MHz HIRC. It supports various trimming capabilities to achieve up to 1.5% accuracy. Clock stabilization latency is remarkably reduced with HIRC (less than 3 µs versus 1 ms to lock the PLL clock). HIRC does not support low power modes. The MCG Lite module allows HIRC to work with Full Speed USB in so-called USB clock recovery mode (available only in Full Speed USB device mode). The USB module monitors the HIRC clock and adjusts the fine trim based on its default values. With this implementation it is possible to achieve better than 1.5% clock accuracy.

The LIRC (2 MHz and 8 MHz) can be configured as the clock source for VLPR mode and can also work in all low power modes except low leakage modes (such as MCGIRCLK). The MCG Lite is powered off in all low leakage modes (LLS, VLLSx). It must be noted that there is no support for switching between

2 MHz and 8 MHz LIRC modes directly because they share the same logic circuit. It is necessary to switch to another clock mode (HIRC or EXT mode) and then switch to the appropriate LIRC mode (this is not allowed when running in VLPR mode).

Four different clock modes (see Figure 1) can be selected with the following clock sources:

- HIRC mode–high frequency (48 MHz) internal reference clock named HIRC48 (with USB recovery feature which allows drastic reduction of jitter)
- LIRC 8 MHz mode (default after reset)–low frequency 8 MHz internal reference clock
- LIRC 2 MHz mode–low frequency 2 MHz internal reference clock
- EXT mode–external clock source (available also on KLx6/KL34):
  - — Low frequency (1–32.768 kHz)
  - — High frequency mode 1 (1–8 MHz), the KLx6/KL34 uses 3–8 MHz
  - — High frequency mode 2 (8–32 MHz for the crystal, and up to 48 MHz for the external square wave clock)

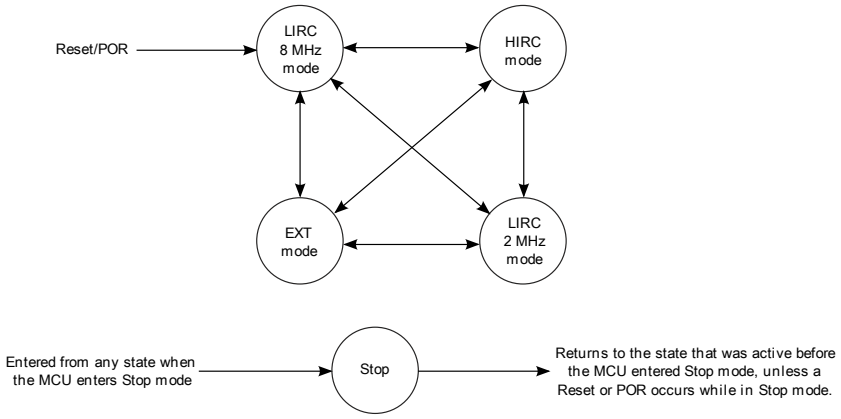

Figure 1. MCG Lite clock mode switching diagram

Some of the registers implemented in MCG Lite share the same fields with the MCG module. The following figures represent selected registers with colored fields (the color representation is explained in Section 3). All features related to the FLL and PLL are removed (red color).

The MCG_C1 register is shown in Figure 2. The clock source selection field is in principle the same as in the MCG module. A slight difference compared to the MCG (on KLx6/KL34) can be found in the IRCLKEN bit. This field controls enablement of the low frequency (2-8 MHz) internal reference clock (LIRC). The same field in the MCG module represents enablement of the internal reference clock for use as MCGIRCLK. The IREFSTEN field represents the same functionality. It enables the internal reference clock to be used in stop mode.

Bit	7	6	5	4	3	2	1	0
Read Write	CLKS		FRDIV			IREFS	IRCLKEN	IREFSTEN
Reset	0	0	0	0	0	1	0	0

Figure 2. MCG_C1 register differences

The control and status registers MCG_C2, MCG_S, and MCG_SC share the same fields with the same functionality as the MCG (on KLx6/KL34) except for fields related to FLL and PLL, which are removed (see figures below).

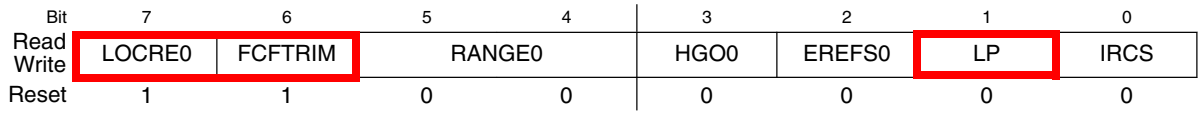

Figure 3. MCG_C2 register differences

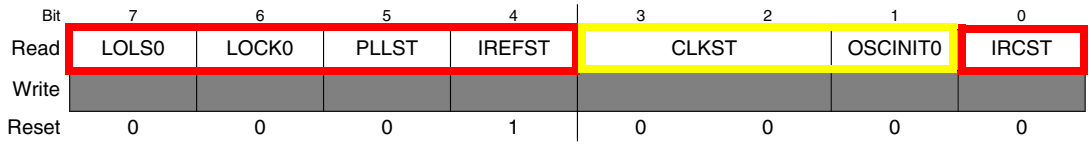

Figure 4. MCG_S register differences

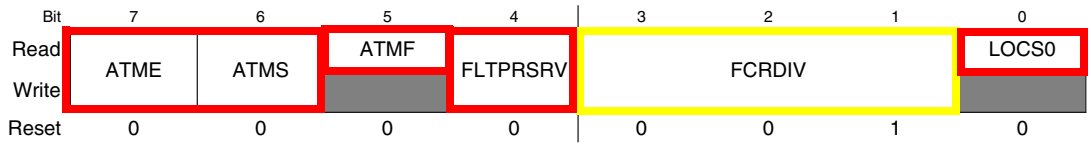

Figure 5. MCG_SC register differences

The MCG miscellaneous control register represents a completely new register implemented in the MCG Lite module. It contains two fields. The HIRCEN field enables the HIRC. The LIRC_DIV2 represents the second LIRC divider, which can be applied only to divide down the clock on the MCGIRCLK output.

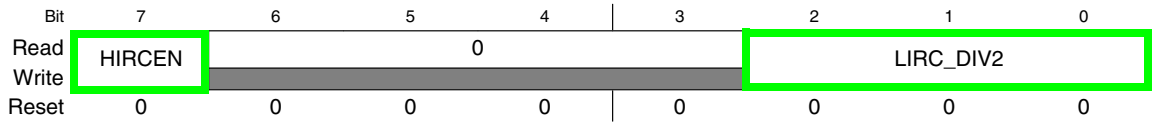

Figure 6. New register MCG_MC

4.1.1 Software impact

Only the EXT mode is not impacted when moving from KLx6/KL34 software to KL43/KL33/KL27/KL17. The remaining clock modes are completely different and require software overhead. If the FLL or PLL is used on the KLx6/KL34 MCUs then it is necessary to move to the appropriate clock mode of the MCG Lite (see Table 3).

Table 3. MCG to MCG Lite clock mode equivalents

KLx6/KL34 MCG mode	KLx3 MCG Lite mode equivalent
FEI	HIRC / 8 MHz LIRC / 2 MHz LIRC
FBI	HIRC / 8 MHz LIRC / 2 MHz LIRC
BLPI	LIRC (divided down to 4 MHz or lower)
FEE	EXT mode

Table 3. MCG to MCG Lite clock mode equivalents

FBE	EXT mode
BLPE	EXT mode (lower than 4 MHz)
PBE	EXT mode
PEE	EXT mode

4.1.2 Hardware impact

There is no hardware impact.

4.2 VREFV1 module

The KL43/KL33/KL27/KL17 devices also include voltage reference which can be used internally for ADC, CMP, or DAC modules, and can also be used by external devices. The voltage reference level is set to 1.2 V, via 0.5 mV programmable steps, using a trim register (see the device data sheet for the minimum and maximum voltage rating specifications). The maximum output current for the high power mode is 1 mA. It is highly recommended to build your hardware carefully and always remember that the voltage reference output pin (VREF_OUT) is shared with the VREFH pin. When the voltage reference module is enabled then a 100 nF capacitor must be connected to the VREFH (VREF_OUT) pin.

4.2.1 Software impact

There is no software impact when using the VREFV1 module.

4.2.2 Hardware impact

The VREFH pin is shared with the VREF_OUT pin. When the VREF module is enabled then a 100 nF capacitor must be connected to this pin. There is a potential hardware conflict when VREFH uses an external reference source and VREF is enabled.

4.3 FlexIO module

The FlexIO module is completely new for the Kinetis L portfolio and is a complex and highly configurable module. It can be targeted to perform emulation of serial/parallel communication protocols such as UART, I^2C, I^2S, and SPI (by means of using one module). However, the FlexIO module is not limited to communication only. It can also be used as a PWM signal generator, an LCD RGB, or as a pure programmable digital logic block, plus many other options.

The FlexIO includes four main features:

- Four 32-bit double-buffered shift registers with transmit, receive, and data match modes. Each shift register also supports read/write capability with bit-byte swap, byte swap, and bit swap
- Four 8- or 16-bit (dependent on mode selection) timers with highly flexible configuration
- Eight I/O pins (for shifter/timer input/output with polarity selection)
- Sixteen triggers (external or internal as shifter, timer, or pin, with polarity selection)

The FlexIO module supports the ability to work in Debug mode and for asynchronous operation during Stop mode (except low leakage modes). IRQ, DMA, or pure polling operation are all supported.

4.3.1 Software impact

There is no software impact when using the FlexIO module.

4.3.2 Hardware impact

There is no hardware impact when using the FlexIO module.

4.4 LPUART module

The LPUART module available on the KL43/KL33/KL27/KL17 MCUs (LPUART0, LPUART1) is a new module. It has similar features compared to the UART0 module available on the KLx6/KL34 MCUs. The main difference is in register access. The LPUART module (KL43/KL33/KL27/KL17) uses 32-bit registers and the UART0 (KLx6/KL34) uses 8-bit registers. There are also some additional new features on the LPUART:

- Match feature expansion:
  - Match configuration (MATCFG)
    - Address match wakeup (default on UART0 KLx6/KL34 MCUs)
    - Idle match wakeup
    - Match on and match off
    - Enablement of RWU on data match and match on/off for transmitter CTS input
  - Generation of IRQ on received data match event (MAxIE, MAxF)
  - Match address extension from 8-bit length to 10-bit length
- Configuration of IDLE flag generation by number of idle characters received (IDLECFG)
- Status flags for 9- and 10-bit data transfer–NOISY, PARITYE, FRETSC, RXEMPT, IDLINE

Figure 7 shows all differences between the UART0 module available on the KLx6/KL34 MCUs and the LPUARTx module available on the KL43/KL33/KL27/KL17 MCUs. The blue text in the figure represents the 8-bit fields in the 32-bit LPUART module registers which are identical with the UART0 registers. The only exception is the LPUARTx_BDH register. It includes an 8-bit field with similar content to the UART0_C5 but with a new feature related to match configuration. The green text in the figure represents all the new features available on the LPUART.

NOTE

Even the LPUART registers that include some identical features are located in memory at completely different address offsets (see Figure 7).

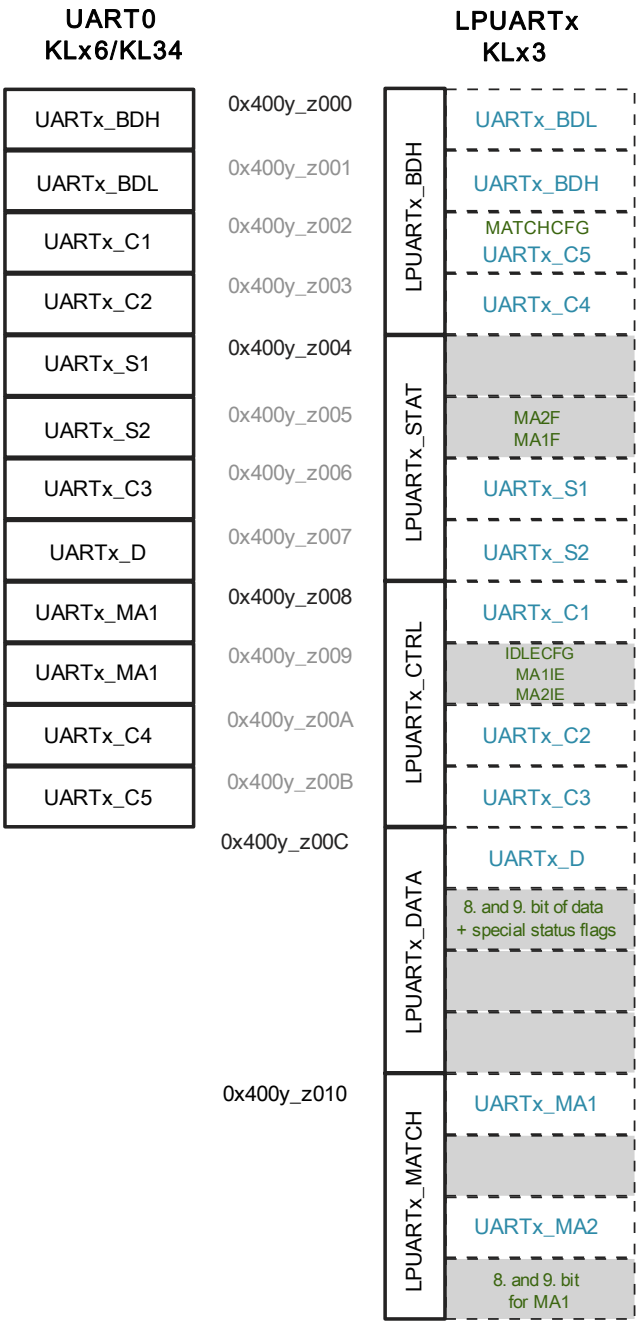

Figure 7. Primary differences between UART0 (KLx6/KL34) and LPUART (KL43/KL33/KL27/KL17)

4.4.1 Software impact

All previously discussed differences must be considered when moving from KLx6/KL34 to KL43/KL33/KL27/KL17 MCUs. If the header file uses the new 8-bit assigned register offsets and the new register fields are not used, then it is software compatible.

4.4.2 Hardware impact

There is no hardware impact when using the FlexIO module.

4.5 Boot option and ROM with Kinetis boot loader

The 16 KB ROM memory with built-in Kinetis boot loader (Kibble) is another new feature available on the KL43/KL33/KL27/KL17 MCUs. There is hardware logic at boot time which starts execution from flash memory (at 0x0000 0000 address) or starts execution of the Kibble from ROM (at 0x1C00 0000 address). The boot option is selectable via the flash nonvolatile option byte in the flash configuration field located in program flash memory (at address 0x40D) and can also be read by flash option register FTFA_FOPT located in the peripheral memory region (at address 0x4002 0003). The table below shows the new boot features implemented on the KL43/KL33/KL27/KL17 MCUs. In general there are two options to boot from ROM or flash memory:

- Using an external pin configuration via the BOOTCFG0 pin, which is shared with the NMI pin. This option is selected when the NMI function is enabled and BOOTPIN OPT is 0, then:
  - When BOOTCFG0 is low the boot starts from the ROM location.
  - When BOOTCFG0 is high the boot starts from the flash memory location.
- Using an internal configuration via the BOOTSRC_SEL field in the flash option field. This option is selected when the external pin configuration is disabled, which means that BOOTPIN_OPT = 1. In that case the BOOTSRC_SEL field selects the boot source.

In the default mode, the boot option is set to ROM because all bits in the FOPT field are set to logical one. The previously mentioned options are available and take place after each power-on reset (POR). There is another boot option which can force booting from ROM with a specified configuration (external pin or boot source selection or both) after any system reset (except POR). This option is available via the reset control module and is explained below.

The built-in bootloader (Kibble) simplifies the effort to program flash memory. All available flash memory programming API can run from ROM and write directly to flash memory. The Kibble supports multiple interfaces such as USB, UART, I^2C, or SPI (depending on the Kinetis family implementation).

An additional difference between the two MCUs is the low-power boot option (yellow area in Figure 8). The KL43/KL33/KL27/KL17 MCUs support booting into the low-power run mode (VLPR) which can rapidly decrease current peaks after reset appears (for example, a wakeup event from low leakage modes).

NOTE

Writing into internal flash memory is not supported when the MCU is running in VLPR mode. For example, when the device is configured to boot to VLPR mode and the user needs to write into flash memory, it is necessary to switch into normal Run mode prior to writing into flash memory.

Bit Num	Field	Value	Definition
7-6	BOOTSRC_SEL	Boot Source Selection: these bits select the boot sources if boot pin option bit BOOTPIN_OPT = 1	
		00	Boot from Flash
		01	Reserved
		10	Boot from ROM
		11	Boot from ROM
5	FAST_INIT	Selects initialization speed on POR, VLLSx, and any system reset.	
		0	Slower initialization: The flash initialization will be slower with the benefit of reduced average current during this time. The duration of the recovery will be controlled by the clock divider selection determined by the LPBOOT setting.
		1	Fast Initialization: The flash has faster recoveries at the expense of higher current during these times.
3	RESET_PIN_CFG	Enables/disables control for the RESET pin.	
		0	RESET pin is disabled following a POR and cannot be enabled as reset function. When this option is selected, there could be a short period of contention during a POR ramp where the device drives the pinout low prior to establishing the setting of this option and releasing the reset function on the pin. This bit is preserved through system resets and low-power modes. When RESET pin function is disabled, it cannot be used as a source for low-power mode wake-up. **NOTE:** When the reset pin has been disabled and security has been enabled by means of the FSEC register, a mass erase can be performed only by setting both the Mass Erase and System Reset Request fields in the MDM-AP register.
		1	RESET_b pin is dedicated. The port is configured with pullup enabled, open drain, passive filter enabled.
2	NMI_DIS	Enables/disables control for the NMI function.	
		0	NMI interrupts are always blocked. The associated pin continues to default to NMI pin controls with internal pullup enabled. When NMI pin function is disabled, it cannot be used as a source for low-power mode wake-up.
		1	NMI_b pin/interrupts reset default to enabled.
1	BOOTPIN_OPT	External pin selects boot options	
		0	Force Boot from ROM if BOOTCFG0 asserted, where BOOTCFG0 is the boot config function which is muxed with NMI pin. RESET pin must be enabled when this option is selected.
		1	Boot source configured by FOPT[7:6] (BOOTSRC_SEL) bits
4,0	LPBOOT	Controls the reset value of OUTDIV1 value in SIM_CLKDIV1 register, and the state of the RUNM register in SMC_PMCTRL. Larger divide value selections produce lower average power consumption during POR, VLLSx recoveries and reset sequencing and after reset exit. The recovery times are also extended if the FAST_INIT option is not selected.[1]	
		00	Core and system clock divider (OUTDIV1) is 0x7 (divide by 8). Device is configured for VLPR mode on exit from reset.
		01	Core and system clock divider (OUTDIV1) is 0x3 (divide by 4). Device is configured for VLPR mode on exit from reset.
		10	Core and system clock divider (OUTDIV1) is 0x1 (divide by 2). Device is configured for RUN mode on exit from reset.
		11	Core and system clock divider (OUTDIV1) is 0x0 (divide by 1). Device is configured for RUN mode on exit from reset.

Figure 8. New and changed boot option available on KL43/KL33/KL27/KL17 MCUs (green area) – in flash memory nonvolatile option byte

4.5.1 Software impact

There is no software impact when using the boot option and ROM with Kinetis boot loader.

NOTE

The default boot source on the KL43/KL33/KL27/KL17 is ROM. Hence, some latency due to ROM code execution can be expected compared to the KLx6/KL34 MCUs where flash memory is the default boot source.

4.5.2 Hardware impact

There is no hardware impact when using the boot option and ROM with Kinetis boot loader.

5 Modules\features updates and differentiations

5.1 NVIC interrupt vector differences

There are a few changes in the NVIC related to interrupt vectors. All expected differences are highlighted in Table 4.

Table 4. NVIC interrupt vectors update

Address	Vector	IRQ	KLx6/KL34		KL43/KL33/KL27/KL17	
			Source Module	Source Description	Source Module	Source Description
0x0000_0070	28	12	UART0	Status and error	LPUART0	LPUART0 Status and error
0x0000_0074	29	13	UART1	Status and error	LPUART1	LPUART1 Status and error
0x0000_0078	30	14	UART2	Status and error	UART2 or FLEXIO	UART2 Status and error or all integrated FlexIO flags
0x0000_00A0	40	24	USB0	USB0 interrupt (OTG)	USB	USB interrupt (FS device)
0x0000_00A2	42	26	TSI0	TSI interrupt		Reserved
0x0000_00A3	43	27	MCG	Loss of external clock + loss of lock		Reserved

5.1.1 Software impact

The appropriate callback function is called in the interrupt service routine on the basis of interrupt flag checking in a case of shared UART2 and FlexIO vector. The UART2 interrupt (KLx6/KL34) must be recognized in the interrupt service routine. Otherwise program flow will not be correct. All service routines related to interrupt vectors which are not defined (especially TSI and MCG) are not used. The additional software overhead is caused by the use of different names.

5.1.2 Hardware impact

There is no hardware impact when considering the NVIC interrupt vector differences.

5.2 AWIC wakeup source differences

There are also some differences in AWIC wakeup sources which are used to exit stop modes (except low-leakage stop modes). They are related to similar peripherals as those mentioned in the NVIC interrupt vector section, and are highlighted in Table 5.

Table 5. AWIC wakeup sources update

KLx6/KL34		KLx3	
Wake-up Source	**Description**	**Wake-up Source**	**Description**
UART0	Any interrupt provided clock remains enabled	LPUART0, LPUART1	Any enabled interrupt can be a source as long as the module remains clocked.
UART1, UART2	Active edge on RXD	UART2	Active edge on RXD
TSI	Any interrupt		
		FlexIO	Any enabled interrupt can be a source as long as the module remains clocked.

5.2.1 Software impact

All software overhead related to the TSI module need not be considered when the KL43/KL33/KL27/KL17 MCUs are used.

5.2.2 Hardware impact

A potential hardware conflict will exist when the TSI module is used.

5.3 LLWU wakeup source differences

There is only one difference in the LLWU wakeup source on the KL43/KL33/KL27/KL17 MCUs. Internal peripheral flags LLWU_M4IF will not take effect on the KL43/KL33/KL27/KL17 because the TSI module is not implemented.

5.3.1 Software impact

All software overhead related to the TSI module need not be considered when the KL43/KL33/KL27/KL17 MCUs are used.

5.3.2 Hardware impact

A potential hardware conflict will exist when the TSI module is used.

5.4 System integration module (SIM)

The KL43/KL33/KL27/KL17 SIM module also includes changes which will be discussed here. As the SIM module interacts with most of the peripheral modules (optional setting for some of peripherals, clock-gated control, and so on) it also includes new features related to the new modules.

The specific feature available on the KL43/KL33/KL27/KL17 MCUs is that the PTE0 and PTE20 pins can be configured as 32 K oscillator clock output. This feature is available via system option SIM_SOPT1 register (see Figure 9).

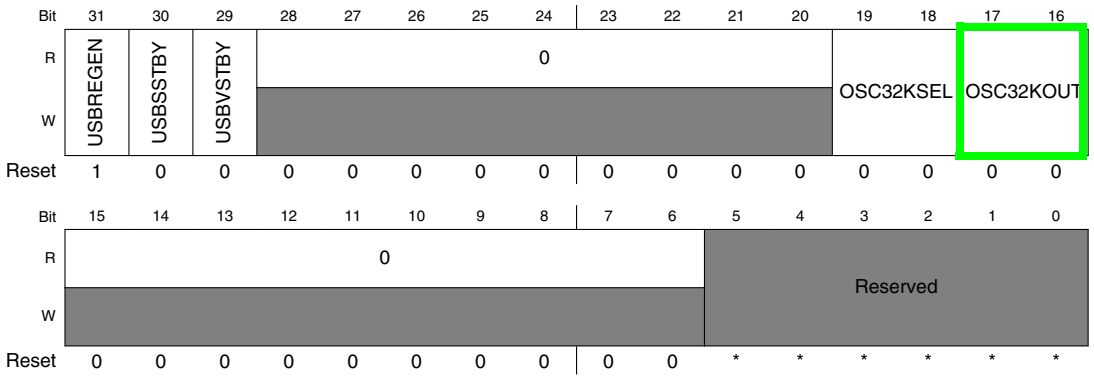

Figure 9. SIM_SOPT1 register new field

The system option SIM_SOPT2 includes new features related to LPUART1 and FlexIO modules. These are completely new features on the KL43/KL33/KL27/KL17 MCUs. Both modules keep functionality in stop modes (except low-leakage stop modes), therefore they require the ability to be clocked asynchronously as in a case of LPUART0 or TPM (these two modules are available on the KLx6/KL34 MCUs). The selection of clock source for both modules is available in the SIM_SOPT2 register (see Figure 10). They use the new field names LPUART1SRC and FLEXIOSRC plus the renamed LPUART0SRC (instead of UART0SRC).

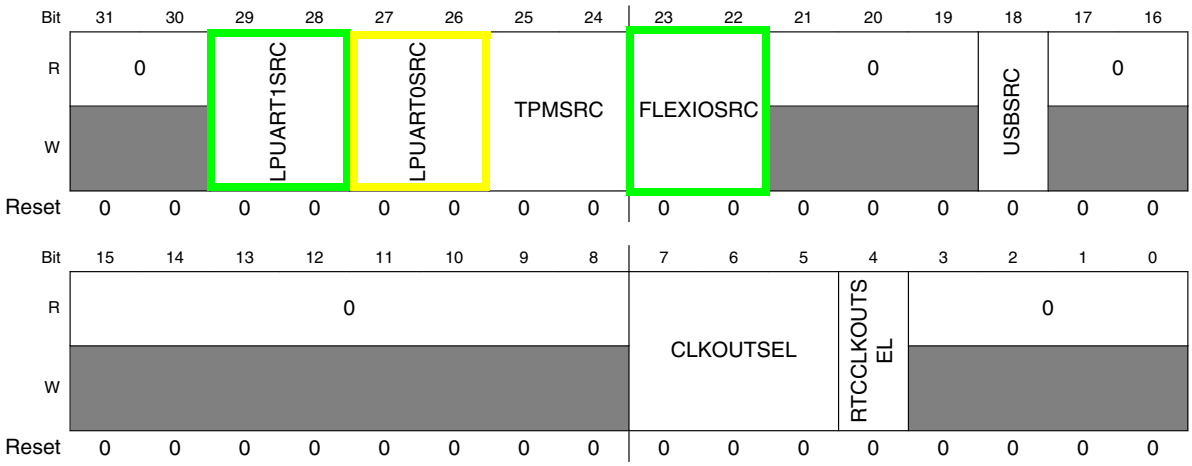

Figure 10. SIM_SOPT2 register new fields

A similar difference can be found in system option register 5 SIM_SOPT5. All register fields are renamed according to the low-power feature (LP).

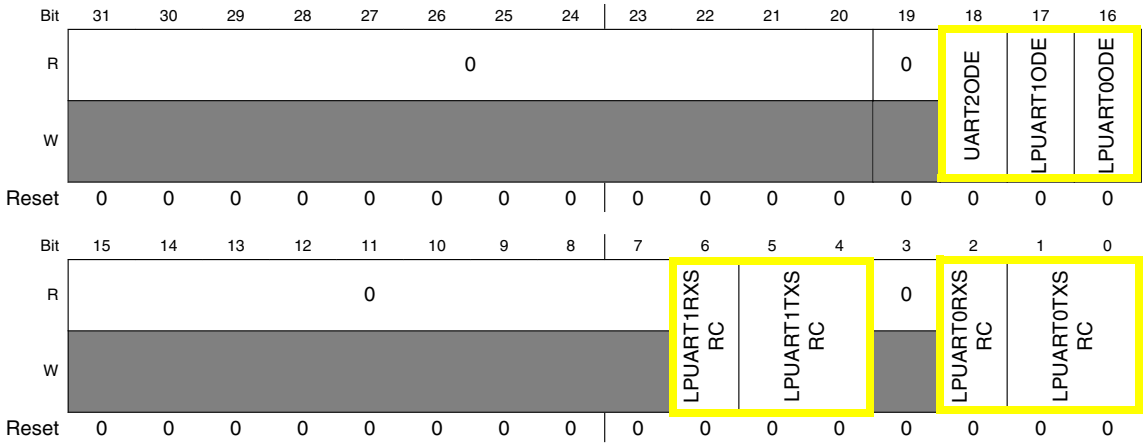

Figure 11. 11 SIM_SOPT5 register new field

All new modules available on the KL43/KL33/KL27/KL17 MCUs need clock gate control. Therefore these are defined in the system clock gate control register in the SIM module. Clock gate control for the VREF module is defined in the SIM_SCGC4 register (see Figure 11). The USB clock gate control uses the new name of the bit field in the SIM_SCGC4 register. The USBOTG (on-the-go) bit used on the KLx6/KL34 MCUs is renamed to USBFS on the KL43/KL33/KL27/KL17 MCUs, which support only device class. The additional new modules FLEXIO, LPUART0, and LPUART1 clock gate control are defined in the SIM_SCGC5 register.

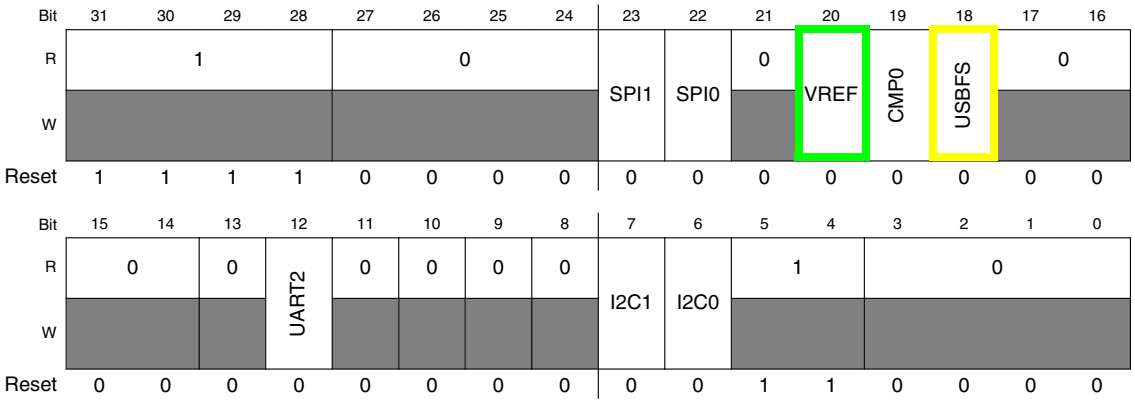

Figure 12. SIM_SCGC4 register – new and updated fields

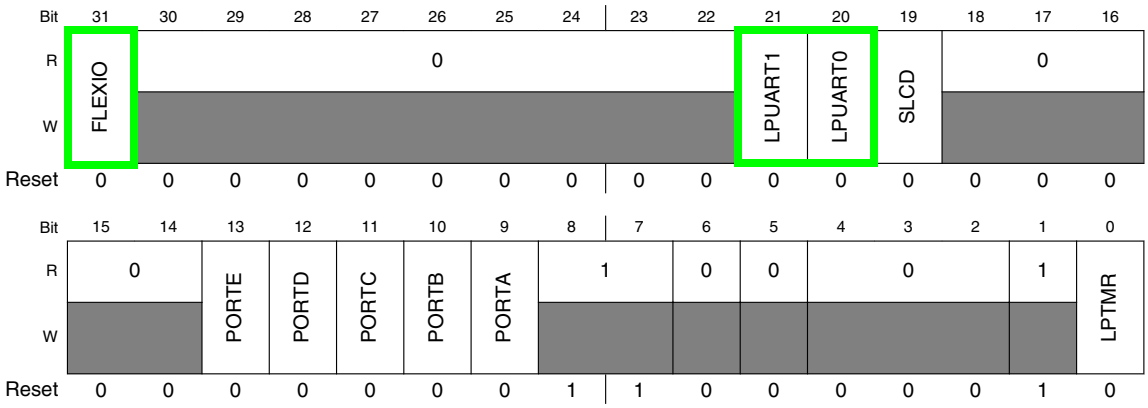

Figure 13. SIM_SCGC5 register – new fields

The KL43/KL33/KL27/KL17 MCUs include some changes in the COP watchdog. The COP is updated by three new fields in SIM_COPC (see Figure 14). The main difference is the selection of the clock source for the COP watchdog. Except for LPO and BUSCLK (available also on the KL43/KL33/KL27/KL17/KL34 MCUs) it is possible to choose from two additional clock sources: MCGIRCLK and OSCERCLK.

A small difference can also be found in timeout selection. There are more options for the number of cycles to be chosen by each clock source. The short timeout option can be chosen from 25, 28, and 210 cycles (on the KLx6/KL34 this option is valid only if LPO is the clock source). The long timeout option can be chosen from 213, 216, and 218 cycles (on the KLx6/KL34 this option is valid only if BUSCLK is the clock source). The additional new feature of the KL43/KL33/KL27/KL17 MCUs is enabling the functionality to work in debug and stop modes.

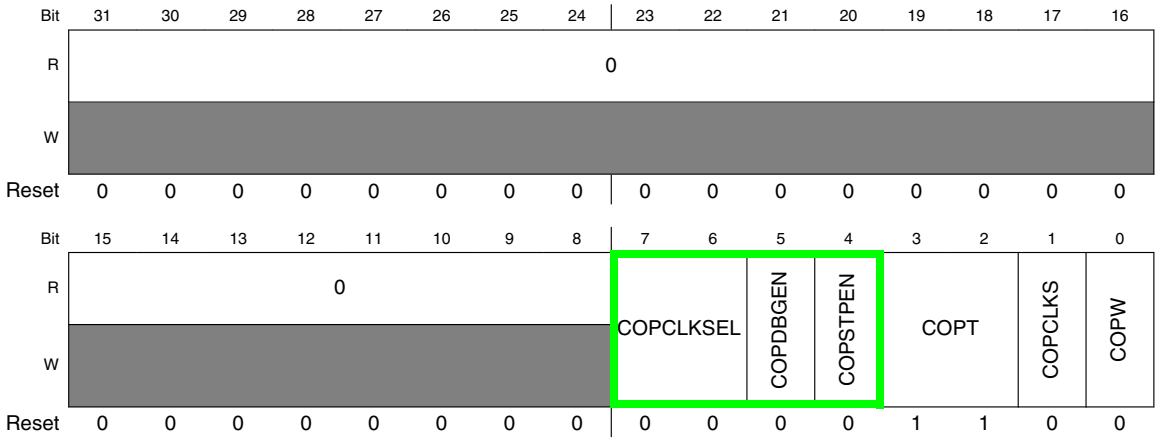

Figure 14. COP control register SIM_COPC register update

5.4.1 Software impact

The software overhead when using the SIM can be found in different bit field names which are shared between the two MCUs.

5.4.2 Hardware impact

There is no hardware impact when using the SIM.

5.5 RCM update

The reset control module RCM on the KL43/KL33/KL27/KL17 MCUs was updated by adding two new features:

- Boot source force and boot source identification
- Sticky system reset status

Besides the boot option provided by flash option FOPT, there is also the possibility to force booting by setting appropriate bits in the force mode register RCM_FM (using the force ROM boot configuration field FORCEROM – see Figure 15). The RCM_FM with FORCEROM option can force booting from ROM with the specified setting in boot source mode register RCM_MR. The force boot option will take place after all subsequent system resets.

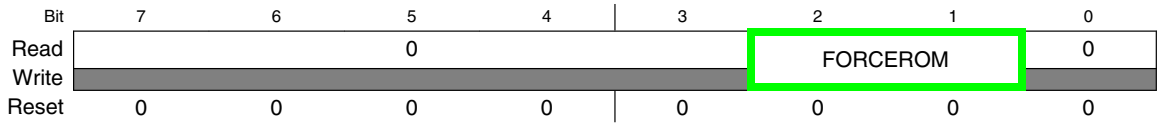

Figure 15. New RCM_FM force mode register

The last boot source can be identified by boot ROM configuration status in the RCM_MR register shown in Figure 16 (if not cleared earlier by software). The four boot sources are:

- Boot from flash memory
- Boot from ROM, caused by:
  - External BOOTCFG0 pin
  - Boot source selection BOOTSRC_SEL
  - Both BOOTCFG0 and BOOTSRC_SEL

The RCM_MR is also affected by the previously mentioned force ROM boot setting. This is a read-once—write-once register.

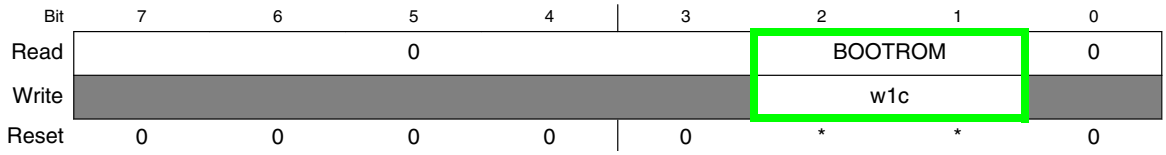

Figure 16. New RCM_MR mode register

Sticky reset status flags represent an additional new feature implemented on the KL43/KL33/KL27/KL17 MCUs. Sticky reset status flags are available via sticky system status registers RCM_SSRS0/1. These status registers can be used to identify all reset sources generated since the last POR, LVD, or VLLS wakeup (if not previously cleared by software). These status flags are implemented in the same fashion as system reset status flags in RCM_SRS0/1 registers with an 8-byte offset.

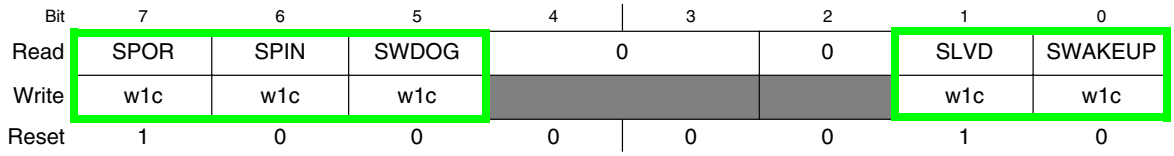

Figure 17. New RCM_SSRS0 sticky system reset status register 0

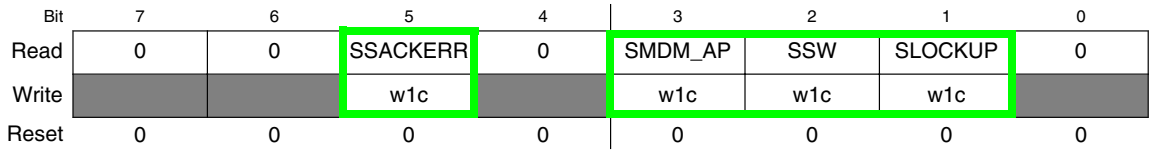

Figure 18. New RCM_SSRS1 sticky system reset status register 1

5.5.1 Software impact

There is no software impact when using the updated reset control module.

5.5.2 Hardware impact

There is no hardware impact when using the updated reset control module.

5.6 DMA MUX differences

The following table highlights the main differences in DMA request sources between the KL43/KL33/KL27/KL17 and KL46/34 MCUs. The update can be seen in LPUART1 source 4 and 5. The DMA source also supports asynchronous requests when in stop mode (VLPS and normal STOP). The new module FlexIO has four new sources: 10-13. This source also supports asynchronous DMA requests. The last difference is in the TSI source which is not included on the KL43/KL33/KL27/KL17 MCUs.

Table 6. AWIC wake-up sources update

Source Number	KLx6/KL34			KLx3		
	DMA Request Sources	Source Description	Async DMA Capable	DMA Request Sources	Source Description	Async DMA Capable
2	UART0	Receive	Yes	LPUART0	Receive	Yes
3	UART0	Transmit	Yes	LPUART0	Transmit	Yes
4	UART1	Receive	No	LPUART1	Receive	Yes
5	UART1	Transmit	No	LPUART1	Transmit	Yes
10	Reserved			Flex_IO	FlexIO_Ch0	Yes
11	Reserved			Flex_IO	FlexIO_Ch1	Yes
12	Reserved			Flex_IO	FlexIO_Ch2	Yes
13	Reserved			Flex_IO	FlexIO_Ch3	Yes
57	TSI		Yes			

5.6.1 Software impact

DMA request based on TSI module will not take effect. Software related to this feature should be removed.

5.6.2 Hardware impact

The TSI module is not available on the KL43/KL33/KL27/KL17 MCUs.

5.7 DAC module update

The new feature on the KL43/KL33/KL27/KL17 MCUs in the DAC module is FIFO buffer work mode, which is selected via the DAC control register (DAC0_C1, field DACBFMD). In this mode the DAC buffer (data registers DAC0_DATx) is organized as FIFO. Any valid write to the DAC data register (data access restriction can be found in the reference manual) will increase the write pointer and put data into FIFO format.

5.7.1 Software impact

There is no software impact when using the updated DAC module.

5.7.2 Hardware impact

There is no hardware impact when using the updated DAC module.

5.8 UART module updates and differences

The UART2 module available on the KL43/KL33/KL27/KL17 MCUs includes the basic features of UART0/UART1/UART2 modules available on the KLx6/KL34 MCUs. Additionally the UART2 module on the KL43/KL33/KL27/KL17 includes these features:

- Address match wakeup feature (this feature is also available on UART0, not the UART1/UART2 of KLx6/KL34)
- ISO 7816 protocol support

The next section discusses the differences between the UART2 module (on KL43/KL33/KL27/KL17) and the UART0/UART1/UART2 modules (KLx6/KL34). The UART2 module does not support LIN break detection and data character with two stop bits. Hence, these features are also removed in registers, especially in baud rate register high UARTx_BDH register (see Figure 19) and status UARTx_S2 register (see Figure 22).

Bit	7	6	5	4	3	2	1	0
Read Write	LBKDIE	RXEDGIE	SBNS	SBR				
Reset	0	0	0	0	0	0	0	0

Figure 19. UARTx_BDH register differences

The UART2 module (KL43/KL33/KL27/KL17) does not support the module control in wait mode. Therefore DOZE mode enable is removed from UART2 control register UARTx_C1 (see Figure 20).

Bit	7	6	5	4	3	2	1	0
Read Write	LOOPS	DOZEEN	RSRC	M	WAKE	ILT	PE	PT
Reset	0	0	0	0	0	0	0	0

Figure 20. UARTx_C1 register differences

None of the flags in status register UARTx_S1 can be cleared by writing one to them (see Figure 21). The detailed description of the flag-clearing mechanism is provided in the appropriate reference manual.

Bit	7	6	5	4	3	2	1	0
Read	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
Write				w1c	w1c	w1c	w1c	w1c
Reset	1	1	0	0	0	0	0	0

Figure 21. UARTx_S1 register differences

Bit	7	6	5	4	3	2	1	0
Read	LBKDIF	RXEDGIF	MSBF	RXINV	RWUID	BRK13	LBKDE	RAF
Write								
Reset	0	0	0	0	0	0	0	0

Figure 22. UARTx_S2 register differences

The UART2 module (KL43/KL33/KL27/KL17) does not support 10-bit data mode as is the case for the UART0 module of the KLx6/KL34 MCUs. Only 9-bit data mode is available. The 9th bit of received data can be read from the 7th bit of control register UARTx_C3. For 9-bit transfer, the 9th data bit must be written into the 6th bit of control UARTx_C3 register. The control registers UARTx_C3 of UART (KL43/KL33/KL27/KL17) and UART1/UART2 (KLx6/KL34) are equivalent.

Bit	7	6	5	4	3	2	1	0
Read Write	R8T9	R9T8	TXDIR	TXINV	ORIE	NEIE	FEIE	PEIE
Reset	0	0	0	0	0	0	0	0

Figure 23. UARTx_C3 register differences (versus UART0_C3 on KLx6/KL34)

As mentioned before, the UART2 module (KL43/KL33/KL27/KL17) does not support 10-bit data mode as UART0 module (KLx6/KL34) does. The M10 field in control register UARTx_C4 represents the position of the parity bit. When set, the parity bit is represented by the 10th bit in serial transmission. The baud rate generator used in the UART2 module (KL43/KL33/KL27/KL17) is a bit different than the UART0/UART1/UART2. It includes five bits of fine adjustment (fractional segment BRFD = 32/BRFA) available as the BRFA field in control UARTx_C4 register. The baud rate calculation differences between the UART2 module available on the KL43/KL33/KL27/KL17 and the UART0/UART1/UART2 modules available on the KLx6/KL34 are shown in Figure 24.

KLx6/KL34		KL43/KL33/KL27/KL17
UART0	UART1/UART2	UART2
$baud\ rate = \frac{\text{UART clock}}{((OSR+1)xSBR[12:0])}$	$baud\ rate = \frac{\text{UART clock}}{(16xSBR[12:0])}$	$baud\ rate = \frac{\text{UART clock}}{(16x(SBR[12:0]+BRFA/32))}$

Figure 24. UART_C4 register differences

NOTE

UART1/UART2 modules on the KLx6/KL34 MCUs have control register UARTx_C4, which is equivalent to control register UARTx_C5 in the UART module on the KL43/KL33/KL27/KL17 MCUs.

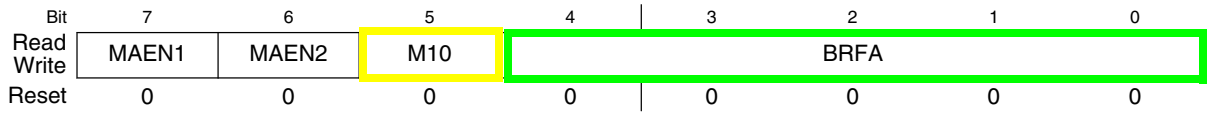

Figure 25. UARTx_C4 register differences

The UART2 module (KL43/KL33/KL27/KL17) does not support both rising and falling edge sampling by the receiver, as well as not supporting control of resynchronization during data word reception. Hence, this feature is removed, as seen in Figure 26.

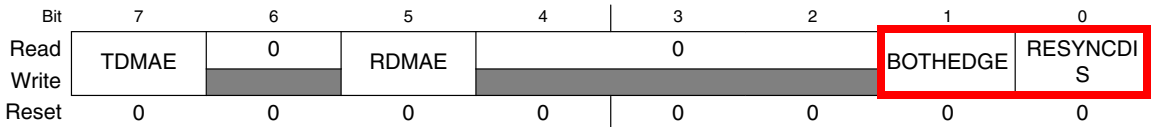

Figure 26. UARTx_C5 register differences

All additional differences are related to the new features which are available only on the UART2 module on KL43/KL33/KL27/KL17, as is ISO7816, and do not affect migration from KLx46/KL34.

5.8.1 Software impact

All previously mentioned differences should be considered when migrating from KLx6/KL34 MCUs to KL43/KL33/KL27/KL17 MCUs.

5.8.2 Hardware impact

There is no hardware impact when using the updated UART module.

5.9 I²C module update

The main change to the I²C module available on the KL43/KL33/KL27/KL17 MCUs is a higher communication rate due to double-buffering support (which is not supported on the KLx6/KL34 MCUs). The interface is designed to operate at up to 400 kbit/s as opposed to the maximum 100 kbit/s available on the KLx6/KL34 MCUs.

The first difference can be found in the status register. The I^{2}C module on the KL43/KL33/KL27/KL17 has extended the number of status flags, which results in two status registers: I2Cx_S1 and I2Cx_S2. The status register I2Cx_S1 is identical to status register I2Cx_S implemented on the KLx6/KL34 MCUs (with the same address offset). The status register I2Cx_S2 (see Figure 27) includes status flags related to the double-buffering feature. Buffer empty (EMPTY) and buffer read/write error (ERROR) flags are implemented.

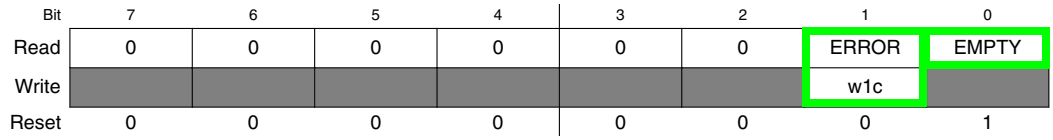

Figure 27. New I2Cx_S2 register

The I^{2}C module on the KL43/KL33/KL27/KL17 MCUs supports both start and stop flag detection with shared interrupt control. Start flag detection is not available on the KLx6/KL34 MCUs. Hence the input glitch filter register is updated by this feature on the KL43/KL33/KL27/KL17 (see Figure 28). However, this feature reduces the number of bits available for the filter factor. Therefore only up to 15 module clock cycles for glitch width can be configured, compared to up to 32 bus cycles on the KLx6/KL34 MCUs.

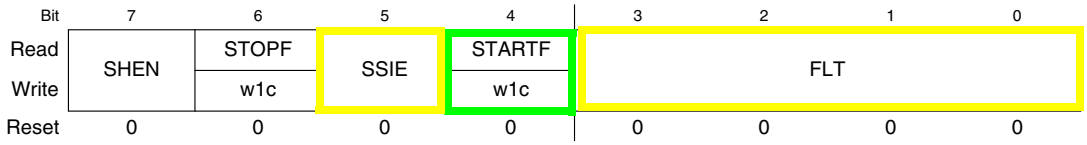

Figure 28. I2Cx_FLT register update

Table 7. I^{2}C module clocks (KL43/KL33/KL27/KL17 versus KLx6/KL34 pinouts)

Module	KLx6/KL34	KLx3
	Clock	Clock
I^{2}C0	Bus Clock	System Clock
I^{2}C1	System Clock	System Clock

NOTE

The I^{2}C1 module on the KL43/KL33/KL27/KL17 MCUs does not support high drive capability of I^{2}C1 pads.

5.9.1 Software impact

There is no software impact when using the updated I^{2}C module.

5.9.2 Hardware impact

There is no hardware impact.

5.10 USB module

The USB module on the KL43/KL33/KL27/KL17 MCUs supports only full-speed (FS) devices. All features related to the host (OTG) supported by the KLx6/KL34 MCUs are removed (see Figures 29-34).

The highest advantage of the USB module available on the KL43/KL33/KL27/KL17 MCUs is the clock recovery feature for the crystal-less solution, which is configurable by the USB clock recovery registers:

- Control register USBx_CLK_RECOVER_CTRL
- Enable register USBx_CLK_RECOVER_IRC_EN
- Interrupt enable register USBx_CLK_RECOVER_INT_EN
- Interrupt status register USBx_CLK_RECOVER_INT_STATUS

The module allows the FS USB controller to work with the HIRC 48 MHz clocks whose accuracy is ±1.5% after factory trim. This feature is not supported on the KLx6/KL34 MCUs.

NOTE

The clock recovery feature is only available when USB is working in full-speed device mode.

The additional new feature available only on the KL43/KL33/KL27/KL17 MCUs is Keep Alive. This feature enables the USB module be active in STOP/VLPS modes. Hence there is no need to re-enumerate when exiting low-power modes. This feature is configurable by two registers:

- Keep Alive mode control register USBx_KEEP_ALIVE_CTRL
- Wakeup control register USBx_KEEP_ALIVE_WKCTRL

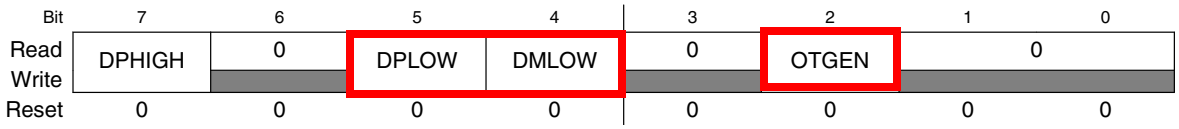

Figure 29. Eliminated bit fields in Control register (USBx_CTL0 vs. USBx_OTGCTL)

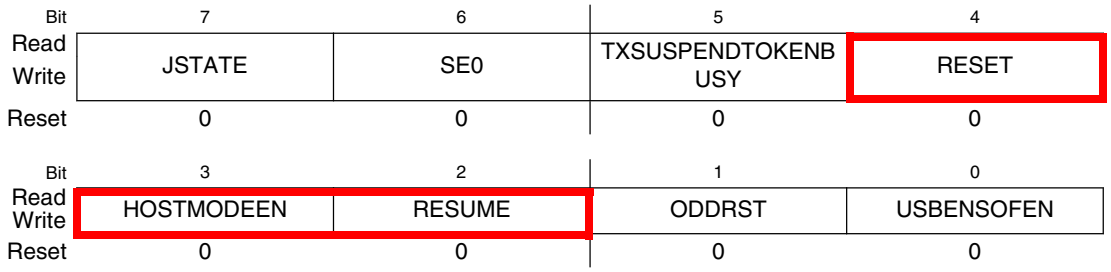

Figure 30. Eliminated bit fields in Control register (USBx_CTL1 vs. USBx_CTL)

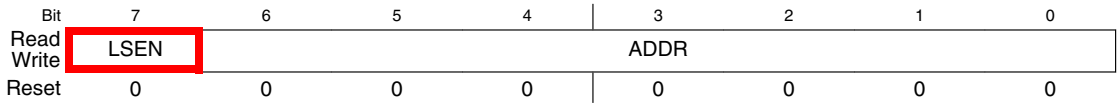

Figure 31. Eliminated bit fields in address register (USBx_ADDR)

Bit	7	6	5	4	3	2	1	0
Read	HOSTWOHUB	RETRYDIS	0	EPCTLDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
Write								
Reset	0	0	0	0	0	0	0	0

Figure 32. Eliminated bit fields in endpoint control register (USBx_ENDPTn)

Bit	7	6	5	4	3	2	1	0
Read	STALL	ATTACH	RESUME	SLEEP	TOKDNE	SOFTOK	ERROR	USBRST
Write	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0

Figure 33. Eliminated bit fields in interrupt status register (USBx_ISTAT)

Bit	7	6	5	4	3	2	1	0
Read Write	STALLEN	ATTACHEN	RESUMEEN	SLEEPEN	TOKDNEEN	SOFTOKEN	ERROREN	USBRSTEN
Reset	0	0	0	0	0	0	0	0

Figure 34. Eliminated bit fields in interrupt enable register (USBx_INTEN)

5.10.1 Software impact

All previously mentioned features must be considered. The USB host is not supported on the KL43/KL33/KL27/KL17 MCUs. The USB device has minimum impact to the software because all features related to the device are included.

5.10.2 Hardware impact

There is no hardware impact when using the USB module.

5.11 SLCD module differences

The KL43/KL33/KL27/KL17 MCUs support a smaller segment SLCD. It is able to generate only 8 backplane signals and 47 front plane signals. The KLx6/KL34 MCUs include 8 back planes and 63 front planes.

5.11.1 Software impact

The previously mentioned feature must be considered when migrating software. When up to 8×47 planes are used then there is no software impact. However, when a higher-segment display than 8×47 (4×51) is used on the KLx6/KL34 MCUs, then it will require complete module reconfiguration. Considering the maximum package available on the KL43/KL33/KL27/KL17 MCUs 64LQFP (BGA), there is no software impact.

5.11.2 Hardware impact

When a higher volume segment display is used then the pin-related planes which are not available on the device should be appropriately handled. Considering the maximum package available on the KL43/KL33/KL27/KL17 MCUs 64LQFP (BGA), there should be no hardware impact.

6 Removed modules

6.1 TSI module

The TSI module was removed on the KL43/KL33/KL27/KL17 MCUs. Hence software touch sensing methods (TSS or Freescale Touch FT) based on GPIO, and so on, should be used.

6.1.1 Software impact

All software related to the TSI module should be removed. If the TSS (FT) library was previously used on the KLx6/KL34 MCUs, then the TSI method could be replaced by the GPIO method on the KL43/KL33/KL27/KL17.

6.1.2 Hardware impact

If the GPIO method based on TSS (FT) is used then it has less impact. However, it is still necessary to make considerable changes related to the GPIO method principle.

7 Appendices

7.1 Pin multiplexing

The tables below show pin multiplexing differences between KL43 and KL46 devices in the same 64LQFP package. This section is focused on making it easier to reuse hardware between the MCUs.

This table uses the following conventions:

Color Key	
GREEN	Designates new additions
RED	Designates removals

Table 8. KL43 versus KL46 pinouts

64 LQFP	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	PTE0	DISABLED	LCD_P48	PTE0/CLKOUT32K	SPI1_MISO	UART1_TX	RTC_CLKOUT	CMP0_OUT	I2C1_SDA	LCD_P48
2	PTE1	DISABLED	LCD_P49	PTE1	SPI1_MOSI	UART1_RX		SPI1_MISO	I2C1_SCL	LCD_P49
3	VDD	VDD	VDD							
4	VSS	VSS	VSS							
5	USB0_DP	USB0_DP	USB0_DP							
6	USB0_DM	USB0_DM	USB0_DM							

Table 8. KL43 versus KL46 pinouts (continued)

7	VOUT33	VOUT33	VOUT33							
8	VREGIN	VREGIN	VREGIN							
9	PTE20	ADC0_DP0/ADC0_SE0	LCD_P59/ADC0_DP0/ADC0_SE0	PTE20		TPM1_CH0	UART0_TX		FXIO0_D4	LCD_P59
10	PTE21	ADC0_DM0/ADC0_SE4a	LCD_P60/ADC0_DM0/ADC0_SE4a	PTE21		TPM1_CH1	UART0_RX		FXIO0_D5	LCD_P60
11	PTE22	ADC0_DP3/ADC0_SE3	ADC0_DP3/ADC0_SE3	PTE22		TPM2_CH0	UART2_TX		FXIO0_D6	
12	PTE23	ADC0_DM3/ADC0_SE7a	ADC0_DM3/ADC0_SE7a	PTE23		TPM2_CH1	UART2_RX		FXIO0_D7	
13	VDDA	VDDA	VDDA							
14	VREFH	VREFH/VREF_OUT	VREFH/VREF_OUT							
15	VREFL	VREFL	VREFL							
16	VSSA	VSSA	VSSA							
17	PTE29	CMP0_IN5/ADC0_SE4b	CMP0_IN5/ADC0_SE4b	PTE29		TPM0_CH2	TPM_CLKIN0			
18	PTE30	DAC0_OUT/ADC0_SE23/CMP0_IN4	DAC0_OUT/ADC0_SE23/CMP0_IN4	PTE30		TPM0_CH3	TPM_CLKIN1			
19	PTE31	DISABLED		PTE31		TPM0_CH4				
20	PTE24	DISABLED		PTE24		TPM0_CH0		I2C0_SCL		
21	PTE25	DISABLED		PTE25		TPM0_CH1		I2C0_SDA		
22	PTA0	SWD_CLK	TSI0_CH1	PTA0		TPM0_CH5				SWD_CLK
23	PTA1	DISABLED	TSI0_CH2	PTA1	UART0_RX	TPM2_CH0				
24	PTA2	DISABLED	TSI0_CH3	PTA2	UART0_TX	TPM2_CH1				
25	PTA3	SWD_DIO	TSI0_CH4	PTA3	I2C1_SCL	TPM0_CH0				SWD_DIO
26	PTA4	NMI_b	TSI0_CH5	PTA4	I2C1_SDA	TPM0_CH1				NMI_b
27	PTA5	DISABLED		PTA5	USB_CLKIN	TPM0_CH2			I2S0_TX_BCLK	
28	PTA12	DISABLED		PTA12		TPM1_CH0			I2S0_TXD0	

Table 8. KL43 versus KL46 pinouts (continued)

29	PTA13	DISABLED		PTA13		TPM1_CH1			I2S0_TX_FS	
30	VDD	VDD	VDD							
31	VSS	VSS	VSS							
32	PTA18	EXTAL0	EXTAL0	PTA18		UART1_RX	TPM_CLKIN0			
33	PTA19	XTAL0	XTAL0	PTA19		UART1_TX	TPM_CLKIN1		LPTMR0_ALT1	
34	PTA20	RESET_b		PTA20						RESET_b
35	PTB0/LLWU_P5	LCD_P0/ADC0_SE8/**TSI0_CH0**	LCD_P0/ADC0_SE8/**TSI0_CH0**	PTB0/LLWU_P5	I2C0_SCL	TPM1_CH0				LCD_P0
36	PTB1	LCD_P1/ADC0_SE9/**TSI0_CH6**	LCD_P1/ADC0_SE9/**TSI0_CH6**	PTB1	I2C0_SDA	TPM1_CH1				LCD_P1
37	PTB2	LCD_P2/ADC0_SE12/**TSI0_CH7**	LCD_P2/ADC0_SE12/**TSI0_CH7**	PTB2	I2C0_SCL	TPM2_CH0				LCD_P2
38	PTB3	LCD_P3/ADC0_SE13/**TSI0_CH8**	LCD_P3/ADC0_SE13/**TSI0_CH8**	PTB3	I2C0_SDA	TPM2_CH1				LCD_P3
39	PTB16	LCD_P12/**TSI0_CH9**	LCD_P12/**TSI0_CH9**	PTB16	SPI1_MOSI	UART0_RX	TPM_CLKIN0	SPI1_MISO		LCD_P12
40	PTB17	LCD_P13/**TSI0_CH10**	LCD_P13/**TSI0_CH10**	PTB17	SPI1_MISO	UART0_TX	TPM_CLKIN1	SPI1_MOSI		LCD_P13
41	PTB18	LCD_P14/**TSI0_CH11**	LCD_P14/**TSI0_CH11**	PTB18		TPM2_CH0	I2S0_TX_BCLK			LCD_P14
42	PTB19	LCD_P15/**TSI0_CH12**	LCD_P15/**TSI0_CH12**	PTB19		TPM2_CH1	I2S0_TX_FS			LCD_P15
43	PTC0	LCD_P20/ADC0_SE14/**TSI0_CH13**	LCD_P20/ADC0_SE14/**TSI0_CH13**	PTC0		EXTRG_IN	audioUSB_SOF_OUT	CMP0_OUT	I2S0_TXD0	LCD_P20
44	PTC1/LLWU_P6/RTC_CLKIN	LCD_P21/ADC0_SE15/**TSI0_CH14**	LCD_P21/ADC0_SE15/**TSI0_CH14**	PTC1/LLWU_P6/RTC_CLKIN	I2C1_SCL		TPM0_CH0		I2S0_TXD0	LCD_P21
45	PTC2	LCD_P22/ADC0_SE11/**TSI0_CH15**	LCD_P22/ADC0_SE11/**TSI0_CH15**	PTC2	I2C1_SDA		TPM0_CH1		I2S0_TX_FS	LCD_P22
46	PTC3/LLWU_P7	LCD_P23	LCD_P23	PTC3/LLWU_P7	SPI1_SCK	UART1_RX	TPM0_CH2	CLKOUT	I2S0_TX_BCLK	LCD_P23
47	VSS	VSS	VSS							
48	VLL3	VLL3	VLL3							
49	VLL2	VLL2	VLL2/LCD_P4	PTC20						LCD_P4
50	VLL1	VLL1	VLL1/LCD_P5	PTC21						LCD_P5

Table 8. KL43 versus KL46 pinouts (continued)

51	VCAP2	VCAP2	VCAP2/LCD_P6	PTC22						LCD_P6
52	VCAP1	VCAP1	VCAP1/LCD_P39	PTC23						LCD_P39
53	PTC4/LLWU_P8	LCD_P24	LCD_P24	PTC4/LLWU_P8	SPI0_PCS0	UART1_TX	TPM0_CH3	I2S0_MCLK		LCD_P24
54	PTC5/LLWU_P9	LCD_P25	LCD_P25	PTC5/LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0		CMP0_OUT	LCD_P25
55	PTC6/LLWU_P10	LCD_P26/CMP0_IN0	LCD_P26/CMP0_IN0	PTC6/LLWU_P10	SPI0_MOSI	EXTRG_IN	I2S0_RX_BCLK	SPI0_MISO	I2S0_MCLK	LCD_P26
56	PTC7	LCD_P27/CMP0_IN1	LCD_P27/CMP0_IN1	PTC7	SPI0_MISO	audioUSB_SOF_OUT	I2S0_RX_FS	SPI0_MOSI		LCD_P27
57	PTD0	LCD_P40	LCD_P40	PTD0	SPI0_PCS0		TPM0_CH0		FXIO0_D0	LCD_P40
58	PTD1	LCD_P41/ADC0_SE5b	LCD_P41/ADC0_SE5b	PTD1	SPI0_SCK		TPM0_CH1		FXIO0_D1	LCD_P41
59	PTD2	LCD_P42	LCD_P42	PTD2	SPI0_MOSI	UART2_RX	TPM0_CH2	SPI0_MISO	FXIO0_D2	LCD_P42
60	PTD3	LCD_P43	LCD_P43	PTD3	SPI0_MISO	UART2_TX	TPM0_CH3	SPI0_MOSI	FXIO0_D3	LCD_P43
61	PTD4/LLWU_P14	LCD_P44	LCD_P44	PTD4/LLWU_P14	SPI1_PCS0	UART2_RX	TPM0_CH4		FXIO0_D4	LCD_P44
62	PTD5	LCD_P45/ADC0_SE6b	LCD_P45/ADC0_SE6b	PTD5	SPI1_SCK	UART2_TX	TPM0_CH5		FXIO0_D5	LCD_P45
63	PTD6/LLWU_P15	LCD_P46/ADC0_SE7b	LCD_P46/ADC0_SE7b	PTD6/LLWU_P15	SPI1_MOSI	UART0_RX		SPI1_MISO	FXIO0_D6	LCD_P46
64	PTD7	LCD_P47	LCD_P47	PTD7	SPI1_MISO	UART0_TX		SPI1_MOSI	FXIO0_D7	LCD_P47

8 References

The following documents are available on freescale.com.

KL46 Sub-Family Reference Manual

KL46 Sub-Family Data Sheet

Kinetis L Series MCUs

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