Freescale Semiconductor, Inc.
Application Note

Document Number: AN5052
Rev. 0, 01/2015

Low-Power Rotation Sensing with L-C Sensors and Kinetis L MCUs

The Freescale Kinetis L low-power MCU family offers low-power features that enable the use of various MCU peripherals in an asynchronous mode, while the CPU is in one of many low-power modes, as well as with other peripherals.

The LPUART, SPI, I²C, ADC, DAC, LP timer and DMA support the low-power mode operation without waking up the core, and enables designer engineers the freedom to build various low-power sensing devices.

Contents

1 Introduction

This application note shows how to build a low-power encoder based on inductive (LC) sensors. The goal is to build a very low power/low rotation speed design which may be used in the paddle wheel flow meters to measure paddle wheel rotation.

The LC sensor used for rotation movement is a common practice in the hybrid flow meter design. The flow meter paddle wheel rotation is measured by means of an LC sensor detecting the presence of conducting material on the rotation disc attached to the meter's paddle wheel. The electronic

paddle wheel flow meters (hybrid flow meters) are battery operated and current consumption is a critical part of the design.

2 The LC sensor principle and how to build a quadrature encoder

A key element of the encoder is contactless sensing of conductive material by means of the LC circuit. If the LC circuit is excited, it starts to oscillate. The oscillation decays at a rate which is determined by the attenuation given by the value of the parasitic inductance resistivity and also the damping factor due to the eddy current generated in the near conductive material.

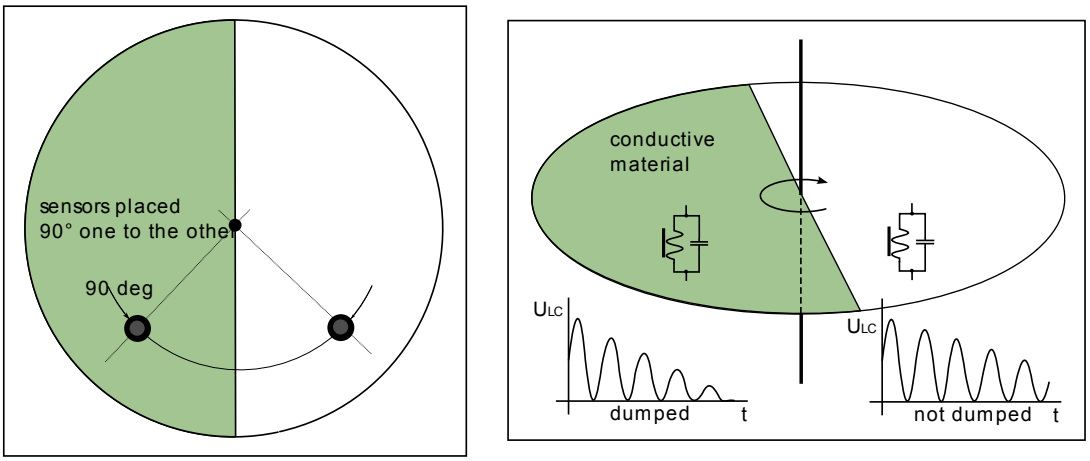

Figure 1. The LC sensor principle at work

[1] Two coils are placed near the rotation disc. The rotation disc is partially covered with a conductive material and forms the quadrature encoder.

The LC sensors are periodically excited (sampling rate) and the LC circuit oscillation dampening factor is measured to determine whether the conductive material is near to the sensor or not.

Two coil sensors placed at 90 degrees to each other, and near the rotation disc, with half of its surface covered with a conductive material, as shown in Figure 1, make up the quadrature encoder.

The quadrature encoder produces the signal shown in Figure 2.

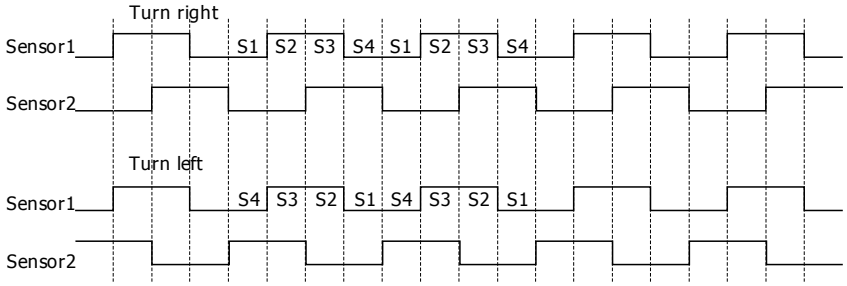

Figure 2. The quadrature encoder signals from the sensors when turned right/left in continuous mode

In Figure 2, there is a graph of signals produced by the encoder. The rotation and rotation direction may be determined. The signals in the picture are continuous, but the LC sensor allows only sampling of these signals by a given sampling rate.

For accuracy and safe rotation detection, a correct sampling rate needs to be chosen. Use the following formula to calculate the minimal sampling rate, provided that two sensors spaced 90 degrees to each other are used.

$$fs = 2\,(sensors) * 2\,(disc\ parts) * 2(nuynquist) * \ rot_{max}$$

$$rot_{max} \ldots rotation\ disc\ maximal\ rotation\ [\frac{turns}{sec}]$$

The samples of the signal produced by the coils are then processed to calculate the turns of the disc.

3 Set up the Kinetis L periphery for low-power encoder measurement

The Kinetis L family of microcontrollers has a rich set of peripherals and features that enable the sensing and processing of analog signals without CPU intervention. A smart combination of the low-power peripherals with the unique features of DMA works as an independent scanning engine to sense an encoder.

This section covers interfacing of the LC sensors, configuration of the peripherals and a description of the measurement technique.

3.1 The LC sensor schematic and interface to Kinetis L periphery

As mentioned previously, hybrid flow meters are battery operated and power consumption is obviously very important, and the way of interfacing the sensors determines the final consumption. To achieve low power consumption while sensing the LC sensors, only the peripherals are working while the CPU is in the very low-power mode. Figure 3 is a block diagram of interfacing the LC sensors.

- The timers TPM0, TPM1, clocked directly from the 32 kHz crystal, may stay running while the CPU is in one of the many power saving modes. The timers continue to count clocks, and, if in the PWM mode, the timers' outputs may be propagated on the pins.
- Timers TMP0 and TMP1 generate control signals to the sensors.
- The TMP0CH1 signal controls the excitation of the sensors. The timer generates a 30uS pulse at the rate of the sampling frequency.
- The TPM1 CH0 and TPM1 CH1 signals enable the actual sensor if multiple sensors are used. Only one sensor is measured for each measurement sequence. Enabling / disabling an actual sensor helps to save energy.
- At the end of TPM0CH1 pulse, the comparator CMP reads out the voltage on the actual sensor. The comparator's multiplexer MUX selects the signal from the actually measured sensor.

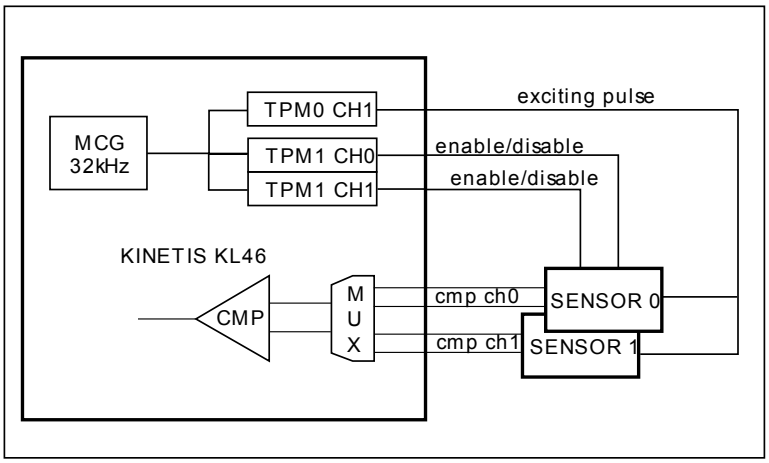

Figure 3. The LC sensor interfacing block diagram

[1] Timer TPM0 to excite and supply the sensor, timer TPM1 to enable/disable the actual sensor.

It is clear how the sensor is connected to the controller, but what exactly is the sensor? Let's call a piece of electronic and sensing coil the "sensor."

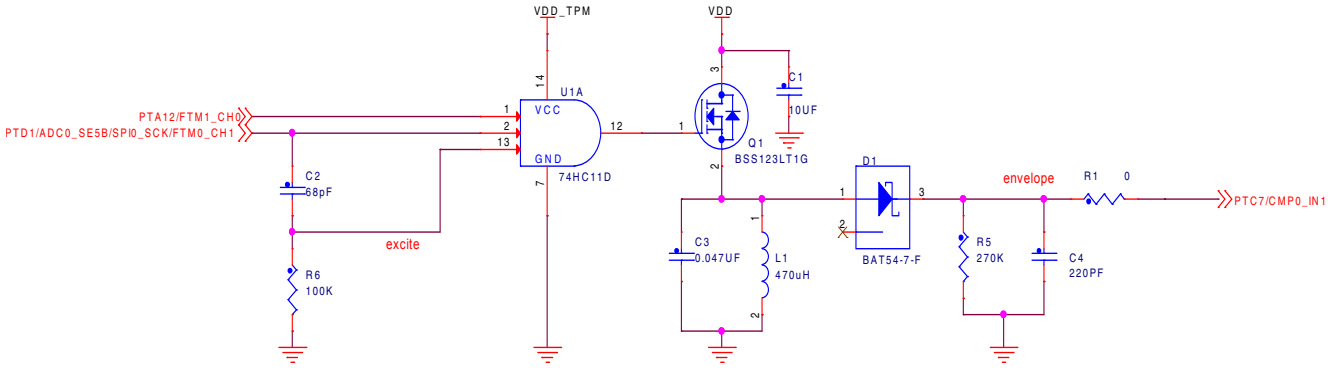

Figure 4. Single LC sensor schematic

The L1-C2 resonant circuit is charged through the Q1 NMOS transistor. The gate of the transistor is controlled by the AND logic gate output pin 12. The AND logic gate has three inputs, controlled by:

- The first AND gate input is controlled by the TPM1CH0 output. The TPM1CH0 timer enables the actual sensor. If the sensor is enabled, then timer TPM1CH0 has logic high on the output.
- The second AND gate input is controlled by the TMP0CH1 output. The timer TMP0CH1 generates the exciting pulse (logic high) of length 30us at the rate of the sampling frequency.
- The third AND gate input, "exciting", is controlled by the C1-R2 delay element. Due to the time domain derived from the 32kHz low-power crystal, the smallest time step the timer can generate is ~30us, but this is too long to charge the L-C element. It is useful to use a shorter time to excite the LC circuit and save energy flowing to the coil. The time constant of R2-C1 combination controls the time of the L-C tank excitation. The time of excitation is roughly t = R2 * C1, and is

set to 6us. Once capacitor C1 is charged to VDD/2, the AND gate output switches to logic zero, Q1 transistor is closed and the L-C circuit starts to oscillate.

The main component of the sensor is the L1 coil which is a sensing element. The coil L1 resonates with the C2 capacitor. The coil and capacitor parameters are important for proper sensitivity. The equivalent serial resistance of the coil and oscillation frequency influence the dampening factor and dampening time. Also, the physical dimensions of the coil influence the current flowing into the coil and affect the overall current consumption.

The voltage on the LC tank goes through the envelope detector formed by D1-R3-C3. The output voltage from the envelope detector voltage is compared by a comparator against the threshold voltage set on the comparator DAC.

3.2 Sensor measurement timing diagram

The detailed sensor control timing diagram is shown in Figure 5. The TPM1CH0 and TPM1CH1 signals are inverted to each other to generate alternating enable/disable signals to sensors 0 and sensor 1. The TPM0CH1 timer generates an excitation signal to both sensors simultaneously.

The RC timing element derives a short pulse from the TPM0CH1 signal and drives the Q1 transistor gate to charge the LC sensing element. Only the enabled sensor is charged and then measured by means of the comparator. The sensor 0 and sensor 1 signals in Figure 5 show the voltage on the LC sensing element – the black line. The red signal line shows the voltage on the envelope detector D1-R3-C3. This signal is compared against the preset voltage threshold on a TPM0 overflow event.

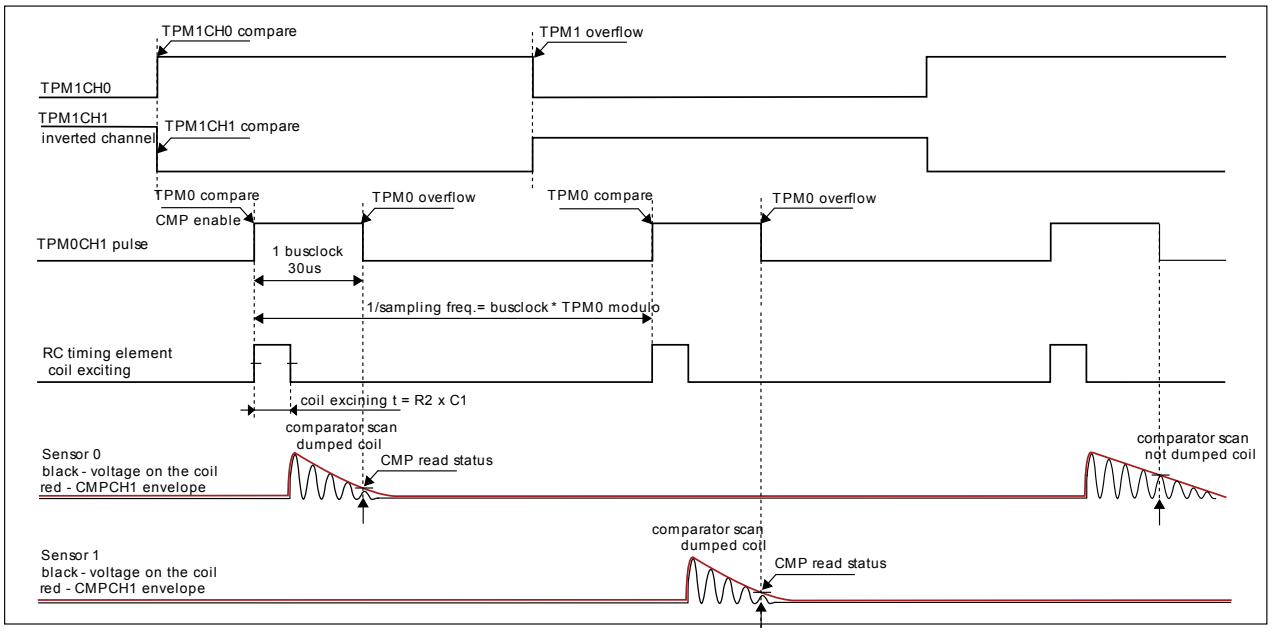

Figure 5. Sensor control signal timing diagram

As the 32 kHz bus clock gives quite a rough time resolution, carefully select the LC tank resonating frequency. The time between coil excitation and envelope voltage measurement is approximately 30us, and the dampened resonance (with metal close to the coil) must last roughly a bit longer than 30us. The

47nF capacitor and 20uH coil give a 150 kHz resonant frequency, which is ~5 oscillations per single bus clock (32 kHz). This is enough to achieve good sensitivity to determine the dumping factor.

3.3 How the comparator is controlled

In the previous section, it was mentioned that the comparator compares the envelope voltage against the preset voltage on a TMP0 overflow event. How is this driven and how is the comparator output status processed?

The guts of the sensor sampling mechanism are three channels of the Direct Memory Access (DMA) periphery running in the VLPS mode without CPU intervention. The DMA periphery can move data between RAM and registers of arbitrary periphery. This technique allows the DMA to control periphery by setting their control register. In the opposite transfer direction, the DMA may read the periphery status register and store content in the RAM.

The DMA transfers operate in the triggered mode, which means that a single DMA transfer (1 or 2 Bytes) is performed every time the DMA channel is triggered.

The timer TPM0 runs in the VLPS modes and TPM can also trigger a DMA transfer. By the proper setting of the TPM0 timer and related timer channel TPM0CH1, both working as the trigger event of associated DMA channels, the state machine may be formed. The state machine performs scanning by the CMP comparator inputs and stores results into the RAM memory. After a predefined number of scanning cycles, the CPU wakes up and the results in the RAM are processed.

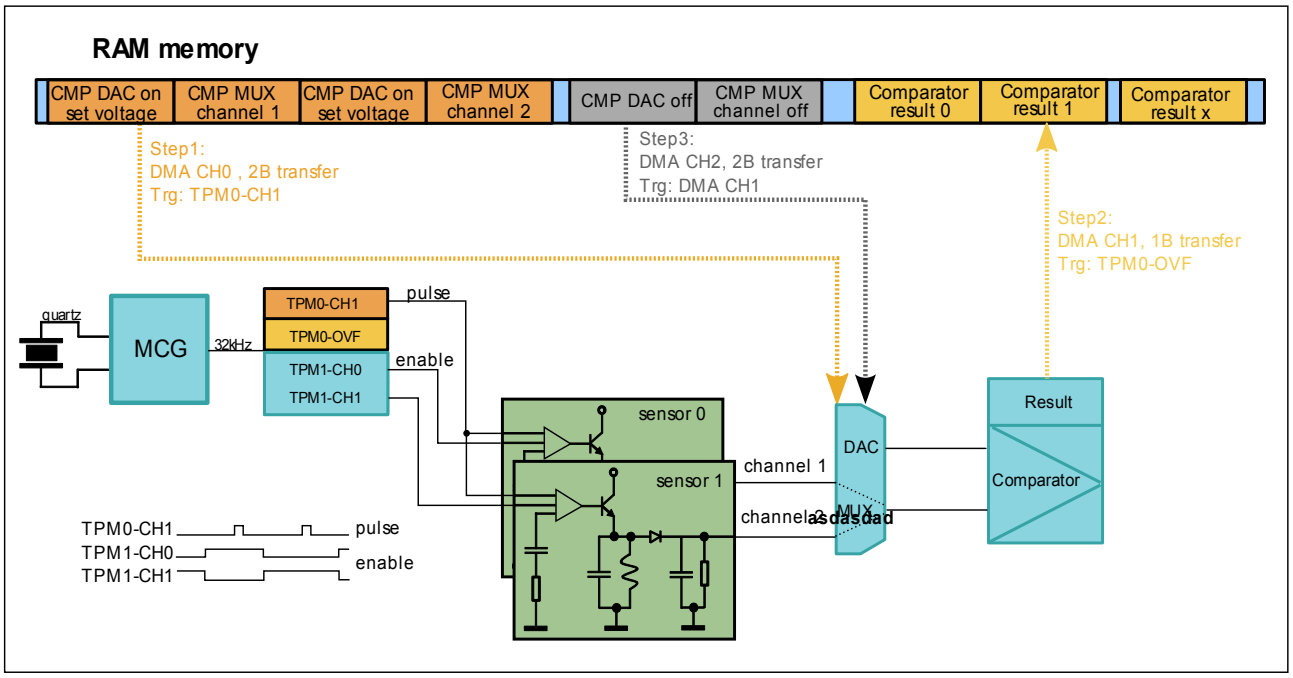

Figure 6. Setting of the DMA channels to build a scanning machine

Figure 6 is a block diagram that shows the connection of the peripherals and DMA channels. The CPU is in the VLPS mode, the time domain is generated by the quartz crystal so that the bus clock is 32,768 kHz.

The TPM0 and TPM1 timers are clocked from the bus clock. The TPM0 timer is used to trigger the DMA and to excite the LC sensors. The TPM1 timer is used to enable / disable the actually scanned sensor.

The TPM0 modulo register value defines the timer overflow and thus the sampling rate. Provided that the bus clock is 32 kHz and the sampling rate is 320Hz, the TPM modulo register must be set to the value 32k/320.

The common paddle wheel-based flow meter has a rotation ~40 rotations per second at maximal flow and then the minimal sampling rate is 320 samples per second (180 samples per second each sensor).

The scanning state machine is repeatedly performing the following steps:

- Step 1: TPM0 CH1 compare event triggers an associated DMA CH0 channel transfer. The DMA CH0 is set to transfer two bytes, to the CMP DAC register and CMP MUX register. The CMP DAC register contains control bits to enable the DAC and to set the output voltage level. The first transferred byte thus enables the CMP DAC and sets the compare threshold voltage. The second byte transferred by DMA sets the CMP MUX register to connect the comparator to sensor1 and the CMP DAC output. The CMP MUX channel setting also controls the comparator on/off state. If the CMP MUX channels are set to a non-valid state (for example, comparator positive and negative input to the same pin), the comparator switches off. Correctly selected MUX inputs will switch the comparator on again. The TPM CH0 logic state is propagated to the output pin and the LC tank exciting pulse is generated.
- Step 2: TPM0 overflow event triggers a DMA CH1 and transfers the CMP output status register value to the RAM. Results from both the sensors are stored into the single array in the form: *sensor1result, sensor2result, sensor1result, sensor2result, sensor1result, sensor2result,…* .
- Step 3: DMA CH2 is linked to DMA CH1 and is triggered once DMA CH1 finishes a transfer. The DMA CH2 is set to transfer 2 bytes to the CMP DAC register and CMP MUX register again. The DMA CH2 transfers the first byte from RAM to the CMP DAC register and switches it off. The second byte is transferred to the CMP MUX register with both inputs set to the same pin and switches the comparator OFF.

After a predefined number of DMA cycles, the CPU is awoken and the results stored in RAM are processed. In the RAM memory, there is a byte array filled with values corresponding to the state of the sensors.

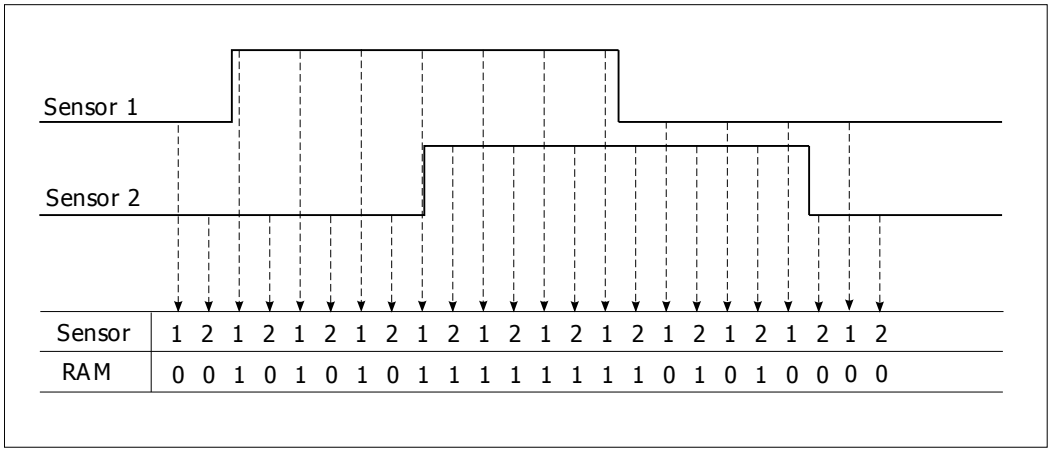

Figure 7. Comparator output state is stored in RAM in the array

[1] The states of the sensors and the corresponding RAM array content are shown in this figure.

3.4 Hardware used to implement the encoder

The encoder framework was implemented on a Kinetis MKL46Z256 processor. For the development, the tower system was used. The development set contains the TWR-KL46Z48M processor board, the primary and secondary elevators (TWR-ELEV-PRIMARY, TWR-ELEV-PRIMARY,) and the peripheral module TWR-FLOW-LC. See the boards in the following figures.

Figure 8. Tower system set used for the LC sensor-based encoder

The TWR-FLOW-LC board was designed to test encoder functionality. The board has two LC sensors assembled and a spindle to attach the encoder disc. In Figure 9, a paddle wheel with aluminum is used instead of an encoder disc. The board is equipped with several jumpers and test pins.

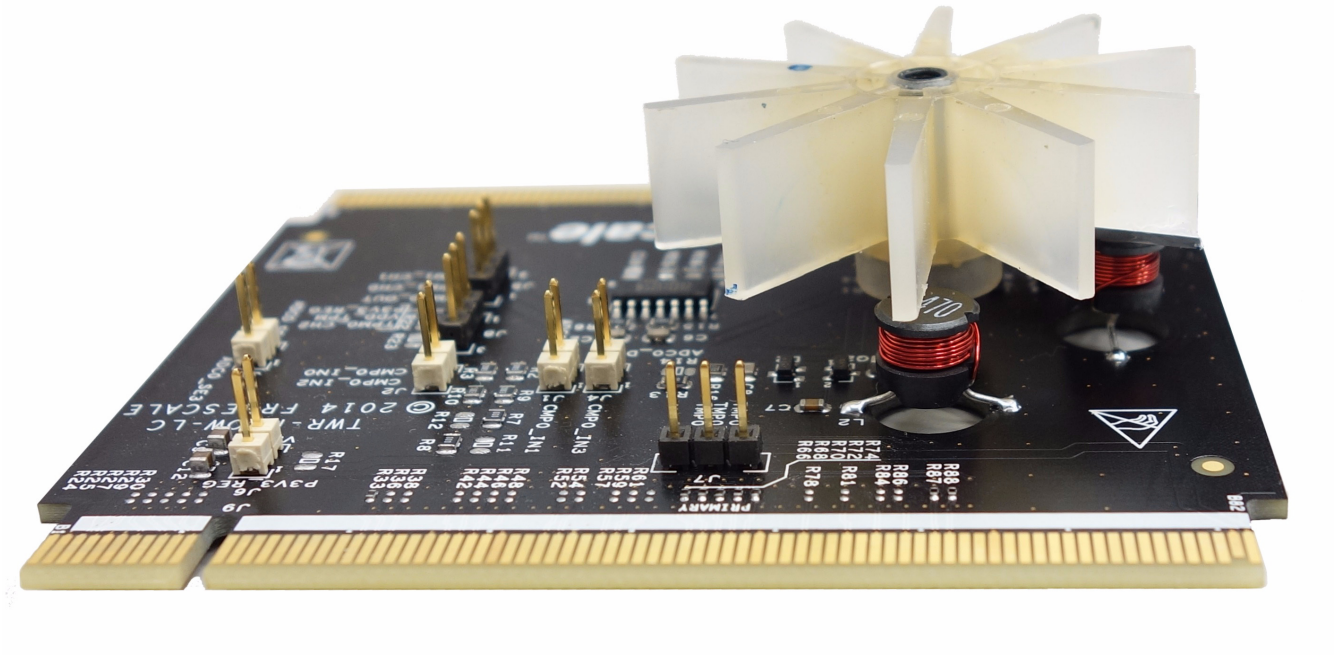

Figure 9. TWR-FLOW-LC board with a paddle wheel as the encoder

There are several jumpers and header connectors on the board, serving as test points and to configure the power supply of the coils and associated logic. For detailed information, refer to Appendix A, "Board schematic.

Detailed board description:

- J1 : test point to observe output from the envelope detector for sensor1.
- J1[Pin1] is connected to the MKL46 comparator CMP0_IN1.
- J1[Pin2] is connected to the analog-to-digital converter ADC_SE0
- J2, J3: There are two voltage dividers on the board to create the threshold voltage to be compared against sensor voltage – output from the envelope detector.
- J2[Pin1]: The R2-R9 voltage divider to be compared with sensor 1 output voltage – CMP0_IN0 input
- J2[Pin2]: The R3-R10 voltage divider to be compared with sensor 2 output voltage – CMP0_IN2 input
- J3[Pin1] - The R2-R9 voltage divider – connected to the analog-to-digital converter ADC0DP3
- J3[Pin2] - The R3-R10 voltage divider – connected to the analog-to-digital converter ADC0DP3

In an actual application, the threshold voltage is generated by the comparator digital-to-analog converter CMP_DAC instead of voltage from the divider.

- J4 : test point to observe output from the envelope detector for sensor2.
- J4[Pin1] is connected to the MKL46 comparator CMP0_IN3.
- J1[Pin2] is connected to the analog-to-digital converter ADC_SE4
- J5 : test points
- J5[Pin1]: comparator output CMP0_OUT
- J5[Pin2]: timer TMP1_CH0 output
- J5[Pin3]: timer TMP1_CH1 output
- J6 : VDD power supply of the coils. This has to be connected by jumper to allow sensors excitation. The header may be also used to measure current to the coils.
- J8: VDD_TMP power supply of the voltage dividers and the AND logic gate. There are two options on how to feed them
- J8[Pins 1-2]: the AND gate and voltage dividers are supplied from the board power supply 3.3V
- J8[Pins 2-3]: the AND gate and voltage dividers are supplied from the TPM0CH2 output. This option allows supplying the circuit only for a limited time of measurement, and, thus, lowers the supply current.

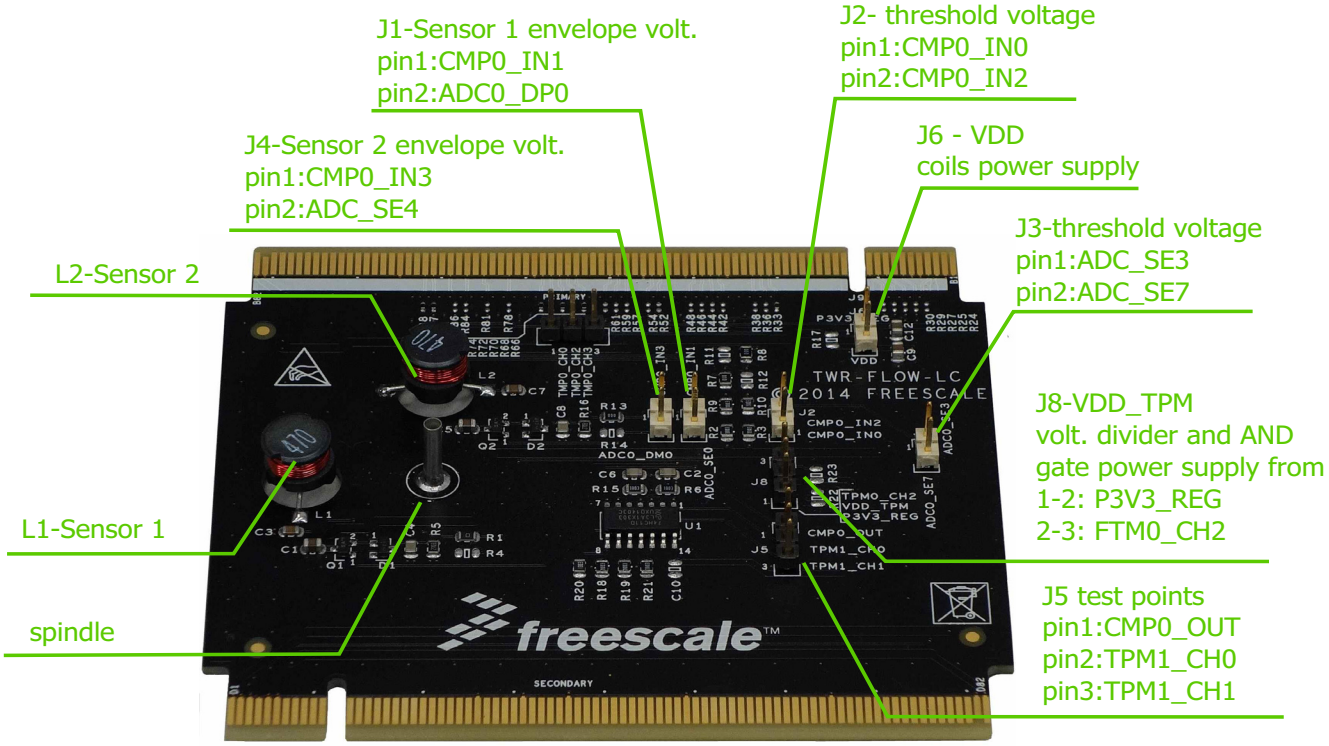

Figure 10. The TWR-FLOW-LC detailed description

4 Software

This section describes the software application of the Kinetis L LC sensor encoder demo. The software application consists of setting the peripherals needed, and the measurement and calculation of the paddle wheel turns.

The application software has been written in C-language and compiled using the IAR Embedded Workbench for ARM (version 6.50.6), with full optimization for execution speed. The software application is based on the Kinetis-L bare-metal software drivers.

The software consists of a few basic blocks. In the beginning, the processor is awoken by a Power on Reset. At the start, the clock is changed to the 32 kHz crystal.

In the following steps, all the peripheries are configured. The clock is enabled only to the peripheries used, to save current. The low-voltage detect unit is enabled to sense the battery level. Both the TMP0 and TMP1 timers are configured and related pins are set to output.

Then the LCD driver periphery and RTC are initialized. As the last step, the comparator CMP and DMA channels are set up and then an interrupt is enabled.

The CPU goes into VLPS mode and may be woken up by one of the following interrupts:

- DMA interrupt service routine is called after a predefined number of DMA cycles. Values with sensor states stored in the RAM are processed and turn counters are updated.
- DMA channels are re-initialized and the LCD screen is refreshed.
- PORT interrupt service routine is called whenever the SW4 button is pressed. In the routine, the index to the LCD screen is updated
- Real-time clock (RTC) interrupt service routine is called each second and the task scheduler is called. The task scheduler is the table of tasks called at a defined time
- LVD interrupt service routine – this interrupt is called once the power supply voltage drops below a preset level, indicating that the battery is empty. The user should do the maintenance necessary to avoid a CPU runaway and data corruption.

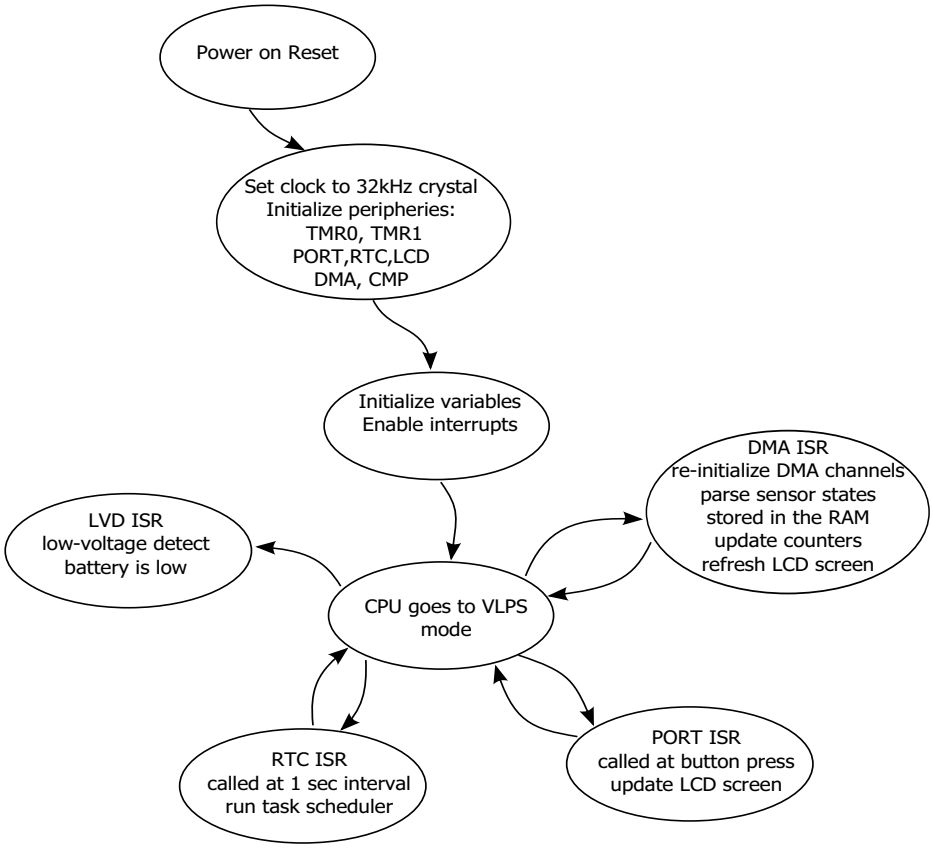

Figure 11. Software flow chart

5 Conclusion

5.1 The current consumption

All measurements were done in a laboratory at 25°C, the current measured by an HP34401A multimeter.

Table 1 is divided into two parts; the five rows at the beginning show the current consumption of the static peripherals which are not dependent on the selected sampling rate. Periphery current consumption is in the row “Current.” The row “Total” shows the cumulative current.

The CPU current consumption is in the VLPS mode, and draws 2.8uA. Adding TMP0, TMP1, RTC and LCD to the processor current gives a total static current consumption of 4uA. In this state, the CPU remains in the VLPS mode forever.

The second part of the table is dynamic and is dependent on the selected sampling rate, measured at 100, 200, 300 and 400 samples per second. The selected sampling rate also affects the current consumption of the comparator and the comparator digital-to-analog converter CMP_DAC periphery, as those are enabled only at measurement and stay disabled the rest of time.

Table 1. Current consumption

Adder static part	Current [uA]	Total [uA]
CPU VLPS mode	2.8	2.8
TPM0	0.3	3.1
TPM1	0.3	3.4
RTC	0.1	3.5
LCD	0.5	4
Adder dynamic part / sampling rate		
DMA + CMP + CMP ADC @ 100Hz	4	8
DMA + CMP + CMP ADC @ 200Hz	7	11
DMA + CMP + CMP ADC @ 300Hz	11	15
DMA + CMP + CMP ADC @ 400Hz	15	19

Appendix A Board schematic

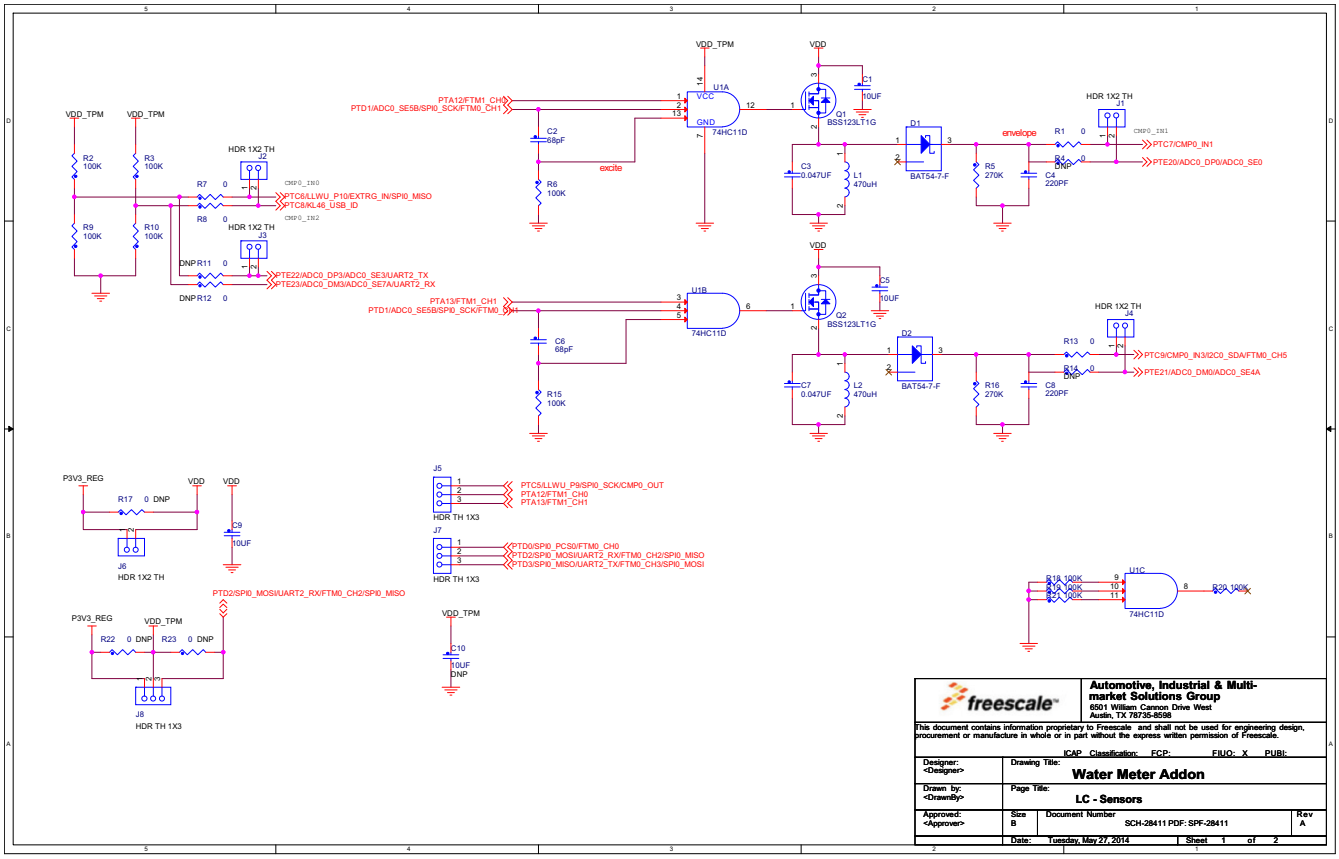

Figure 12. Water meter addon

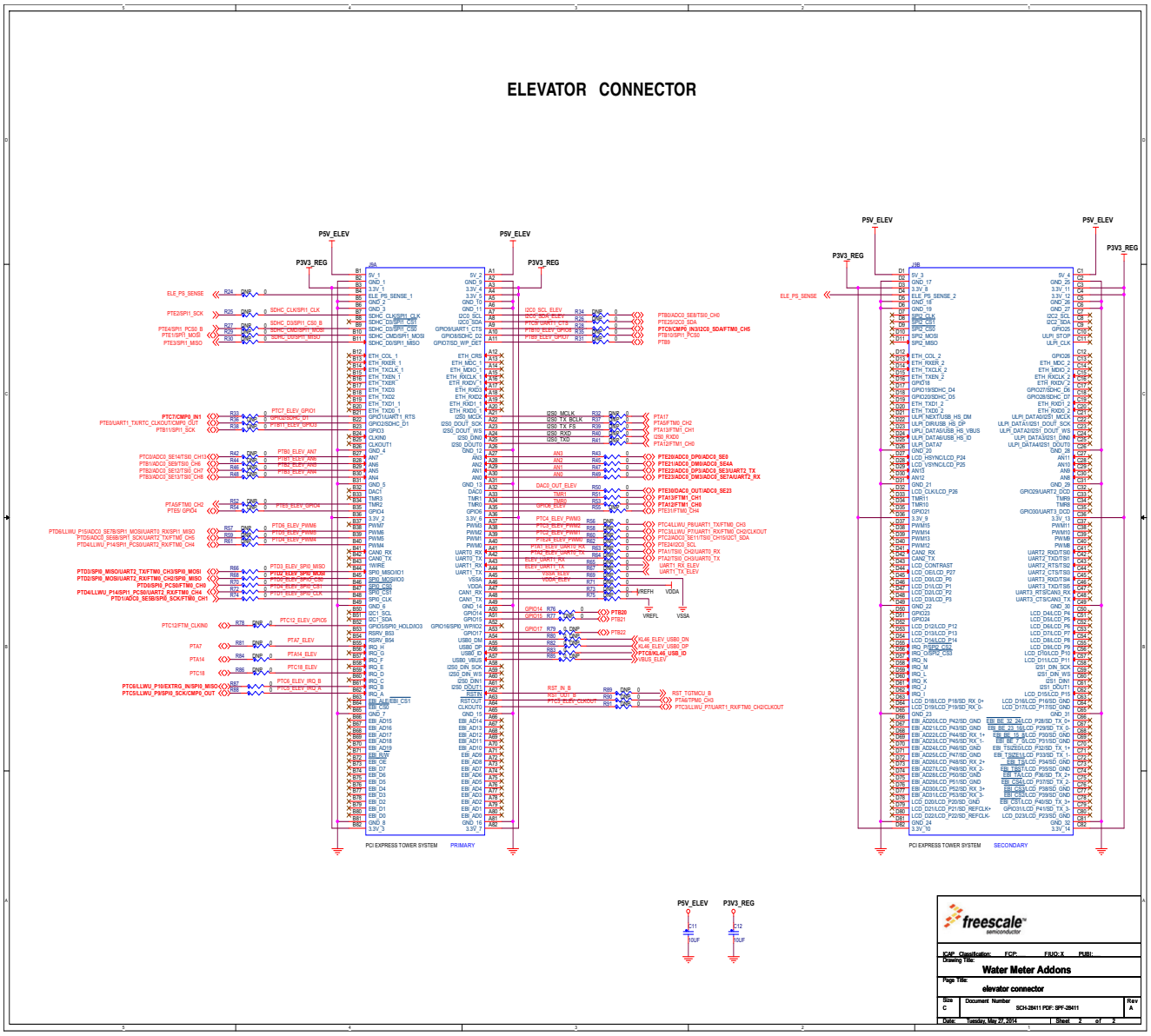

Figure 13. Elevator connector

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number: AN5052
Rev. 0
01/2015