

EMC Design Tips for Kinetis L Family

by: Dennis Lui and T.C. Lun

1 Introduction

Electromagnetic Compatibility (EMC) design consideration is one of the critical factors to ensure a system is robust in design, able to operate flawlessly in harsh environments, and does not disturb others in terms of interference. This application note provides design tips on how to use Kinetis L series MCU in applications with EMC requirements. Different techniques in hardware design, PCB layout, and software setting are illustrated here to help customers to apply EMC enhancements on their products at the beginning of the design phase. In general, the fixes of EMC issues in final stage are more complicated, expensive, and time consuming. There are lots of constraints on circuit and PCB layout modifications, some are as follows:

- When all component or module placements are fixed inside the system
- The cost structure is also higher due to additional components used for those corrective actions.
- The impact on project schedule is sometimes uncertain if the solution invokes a major design change on mechanical aspect.

Contents

1	Introduction.....	1
2	System overview.....	2
3	EMC design tips.....	3
4	Hardware design	3
4.1	Multilayer PCB board	3
4.2	Placement methods.....	4
4.3	Power supply and ground routing	4
4.4	Decoupling and bypassing	5
4.5	Crystal oscillator circuit	5
4.6	Spacing and isolation	6
4.7	Input and output port.....	6
5	Software design.....	6
5.1	Enable WatchDog function	7
5.2	Refresh data direction setting registers	7
5.3	Fill unused memory.....	7
5.4	Define all interrupt vectors.....	7
5.5	Select FLL engaged mode.....	7
5.6	Reconfirm edge-triggered	8
5.7	Enable digital filter.....	8
5.8	Enable slew rate control	8
6	Conclusion	8
7	References.....	8
8	Revision history	9

required for high-power control circuits. For example, most of power relay switches are controlled by 12 V driving circuits but the high current stages are drawn from AC power line input directly.

The Kinetis L MCU is used for all signal detections on user input interface from traditional pushbuttons and new developed capacitive touch pads, communications to host controller through legacy serial port or universal USB port, system monitoring from sensor devices on IIC bus or direct voltage input at ADC pins, and power controls using GPIO pins with specific sequential order for system protection purpose. The segment LCD module inside the MCU generates all the waveforms required for an LCD display panel and also includes features such as blinking, alternate display, segment fault detection, and load adjustment.

3 EMC design tips

The EMC design tips are discussed in following sections separately from hardware and software point of views. Hardware or software engineers can select the section according to their requirements and apply the tips directly into their design.

The hardware design tips cover the considerations in board level which include design techniques on PCB layout and precautions for different type of I/O ports. The primary objective is make use of EMC knowledge to prevent any internal or external noises that affect the system operation and stability; minimize the coupling effectiveness from the noise source to the victim (for example, the MCU), reduce the noise magnitude from the interfering source, and increase the noise immunity of the receptor.

Defensive software design concept is another direction to address the EMC issues caused by improper software handling on false triggered events in noisy environment. The software must be able to identify if a particular event is a false alarm triggered by noise sources or it is a normal driven event and then make a smart decision on corresponding actions. For example, the MCU must not start a high-power control stage if there is any uncertainty on the requested action.

4 Hardware design

The hardware considerations for MCU application in noisy environment consist of PCB layout design and external component connections for peripheral interfaces. In board-level, the PCB layout is the key factor for noise coupling from internal or external noise sources. The traces on the layout act as coupling paths and the geometry factors of the traces (length, width, shape, and position) affect the coupling effectiveness significantly. A proper board and cable placement in the system can help to isolate noise sources from the system and increase the system immunity level. The following subsections describe techniques recommended for a robust hardware design.

4.1 Multilayer PCB board

It is more difficult to design a single-layer PCB for application board with a high pin-count device even though it is more cost effective. Double-layer PCB design provides more flexibility on component

placement, signal trace routing, power supply decoupling, and reference grounding. However, the size and shape of the PCB board are limited by the mechanical form factor which is the key obstacle for PCB design in most of the cases. Four-layer PCB design is a good choice for complicated product design. The top and bottom layers are usually assigned for signal trace routing, the middle layer next to the layer with MCU is used as a ground plane for shielding purpose and adds all the power supply routing on another middle layer.

4.2 Placement methods

The placement of components must be satisfied with the list of mechanical constraints for the product. The general guidelines for reference are as follows:

- Mark all positions for screw holes and mounting points as keep-out area.
- Place all user interface components with fixed position requirement, for example display panel, control buttons, and connectors.
- Separate high-power circuitry from low-power and noise sensitive circuitry.
- Place associated components into small group and try to align the groups in a logic order which matches with the corresponding signal flow.
- Identify all critical components that need to be placed near the MCU; external components connected from MCU input ports to power or ground, for example, supply decoupling capacitors and filter components for input signals.
- Minimize the area formed by the power loops and ground loops.
- Reduce the common mode impedance from power and ground to the MCU.

It requires a lot of effort to finalize an acceptable version which is able to fulfill all the constraints.

4.3 Power supply and ground routing

The PCB layout for power supply and ground plane are extremely important for EMC performance in board-level, especially in multi-supply system with 3.3 V and 12 V. PCB layout technique is used to separate the ground plane into two portions, one is defined as the return path for 12 V circuits and another is the 3.3 V return path for MCU and other critical components. The noise from 12 V ground will not be coupled with the 3.3 V ground through the ground traces.

In some application cases, the 12 V ground is intentionally used as the return path for components operated in 3.3 V supply rail and subject to ESD damage in air-discharge test. The reason to connect the 12 V ground to those 3.3 V components is to prevent the ESD discharge energy couples into the 3.3 V ground directly. The MCU may be forced to reset, halt or even damage if there is a high energy passing the MCU ground.

The MCU ground connection method in PCB layout is an essential factor of the EMC performance, fills up a ground plane underneath the MCU and connects all VSS pins together, which is a good practice for EMC consideration. This method ensures all MCU VSS pins are kept at same potential level and also minimizes the inductance on current return path from MCU to bypass capacitors for high-frequency noise. For LQFP package, the MCU ground plane can be further extended to the package corner points

to achieve short ground paths with minimum loop area for other peripheral components around the MCU.

4.4 Decoupling and bypassing

It is necessary to have better understanding on the concepts of decoupling and bypassing to avoid any incorrect implementation for EMC issue:

- Decoupling is used to isolate noise between circuits on its common line. The power trace is one of the common lines from a voltage regulator to the MCU.
- Bypassing is used to reduce the high-frequency current flows in an impedance path by shunting that path with a bypass capacitor.

The effectiveness of adding decoupling and bypass capacitors for the MCU are very dependent on joining position and sequence. The guidelines of PCB layout on MCU supply pins (VDD and VSS) are as follows:

- Connect the power and ground traces from the power source to the decoupling capacitors and then connect them to the bypass capacitors before going to MCU's VDD and VSS pins.
- Place the power and ground traces in parallel to minimize the loop area.
- Place the bypass capacitor to each VDD and VSS pair as close as possible.

4.5 Crystal oscillator circuit

The crystal oscillator components connected at MCU EXTAL and XTAL pins are very sensitive to external noise. The PCB routing of ground trace in form of a guard ring along with the traces connecting to the EXTAL and XTAL pins can minimize the noise coupling into the crystal circuit. The general guidelines are as follows:

- Do not place any signal trace (except the ground traces) near crystal circuit or across the bottom side of the circuit.
- Place the oscillator circuit to the EXTAL and XTAL pins as close as possible, that are the crystal, feedback resistor, and loading capacitors.
- Select the internal oscillator as clock source for better EMC performance.
- In double-layer or multilayer PCB, connect the ground of loading capacitor to the ground plane directly.
- Select minimum bus frequency to fulfill system requirements.
- Apply minimum trace length to oscillator circuit.
- Use suitable value of feedback resistor and loading capacitors.

4.6 Spacing and isolation

The isolation for different circuit blocks is important when an AC high-power circuit is involved side by side to a low-power circuit on the same board. In some cases, you may need to add a physical slot for better isolation if the board size is limited. Similarly, apply enough isolation space between the PCB trace and mounting screw holes or board edge for ESD consideration.

4.7 Input and output port

The MCU I/O ports, configured as input function, are more sensitive to noise as compared with the output function. In general, an RC filter is added for each input function pin to attenuate the noise injected into the pin from external noise sources. The placement of the filter should be close to the pin. The value of the RC filter depends on the input signal and its characteristic (digital or analogue, and rate of change). The typical value of the series resistor is in the range of 100 Ω to 1 k Ω while the value of filtering capacitor is in the range of 1000 pF to 0.1 μ F.

The RESET_b and NMI_b are special pins in the Kinetis L MCU. Placement of decoupling capacitor for RESET_b pin and the external pullup for both pins should be considered as power pin filtering. It is recommended to minimize the ground loop for the capacitor and the VDD loop for the pullup resistor of these pins.

For each unused I/O pin, do not connect to anything, just make it floating and then set it as output low in software. Periodically refresh state of the pin to avoid change in state by noise. If floating pins are not allowed in particular application, connect a 10 k Ω pulldown resistor for each unused pin. Do not connect any unused I/O pin to power or ground directly.

5 Software design

A good software design with EMC considerations improves overall system performance and operating stability in noisy environments. In general, the software design cannot change the physical media which couples noise into the system, or reduce the absolute magnitude of noise generated from external sources. However, the software provides an intelligent method to select corrective actions in fault conditions and implement precautionary features for system protection. Following software techniques are recommended for a good defensive software design:

- Enable WatchDog function to avoid code runaway.
- Refresh data direction setting registers periodically.
- Fill unused memory to avoid code runaway.
- Define all interrupt vectors even those are not used.
- Select Frequency-Locked Loop (FLL) engaged mode.
- Always reconfirm edge triggered event.
- Enable digital filter on input port.
- Enable slew rate control on output port.

5.1 Enable WatchDog function

The WatchDog (WDOG) function forces a system reset when the application software fails to execute as expected. For example, a running software jumps into an unexpected memory location or runs into an infinite loop when transient noise is injected into the MCU. It is important to make sure that the system will not halt even the software loop is out of control in harsh conditions. Holding the MCU in uncontrollable state is very dangerous and unacceptable, especially for high-power control application with safety requirements. It is recommended to add the WDOG refresh routine in the main loop instead of sub-routines and interrupt routines.

5.2 Refresh data direction setting registers

The input or output direction state for each port pin should be recovered to the expected condition, if it has been changed by any transient noise accidentally. It is recommended to define a simple routine to refresh all data directions periodically. The refresh period depends on the application requirement and timing pattern of the injected noise. For AC power application, the 50 Hz or 60 Hz periodic signal captured from AC power line through an optical coupling circuit can be used as a trigger signal.

5.3 Fill unused memory

Unused memory, flash memory or RAM should be filled with a predefined content such that the MCU does not execute any unexpected instruction when the normal execution flow is disturbed by external noise sources. One of the choices is to fill all unused memory with instruction which is not defined in ARM® Cortex®-M0+ core. The execution of an undefined instruction will force the processor to go through the fault routine for appropriate action.

NOTE

For details, see ARM Cortex-M0+ Devices Generic User Guide, available on arm.com.

5.4 Define all interrupt vectors

The reason to define the interrupt vectors for each unused interrupt function is to allow the MCU to jump into a predefined interrupt routine when a particular unused interrupt flag is false triggered by a noise source. The MCU is able to resume the execution steps correctly after the interrupt function.

5.5 Select FLL engaged mode

It is recommended to enable the FLL engaged mode with internal or external reference clock in the multipurpose clock generator (MCG) module, which provides clock source option for the MCU. The reference clock source first divides the lower frequency by reference divider and then multiplies the frequency up in FLL module. The final core or bus clock is equal to FLL output frequency divided by the core or bus frequency divider.

The advantages of the frequency conversion in MCG module are:

- The impact of transient noise glitch on high-frequency clock source (before the reference divider) is more significant compared to a low-frequency clock source (after the reference divider) in terms of the glitch width against the clock cycle.
- In general, the response of the FLL module is not fast enough to react to such kind of short pulse noise due to the low-pass filter characteristic.

5.6 Reconfirm edge-triggered

Multiple reading on input data for each edge-triggered interrupt service is almost an essential technique to confirm if the input event is valid and driven by determined sources. The timing slot between each successive reading inside the loop should be adjusted with some kind of irregular pattern such that an even distributed noise pattern will not be recognized as a valid event. A simple random delay function is inserted between each reading such that the overall repeat period is not consistent. The random delay variable can be equal to a free-running counter value captured when there is an interrupt trigger even.

5.7 Enable digital filter

The digital filter is a feature in Kinetis L MCU that provides a simple low-pass filter characteristic for each port pin that is configured as a digital input. The filter width in clock size is same for all enabled digital filters within one port and should be changed only when all digital filters for that port are disabled. This configurable filter provides an adaptive way to handle different types of transient noises with deterministic pulse width in nature which are difficult to handle by traditional analog filters.

5.8 Enable slew rate control

Slew rate control can be enabled for each port pin by setting the corresponding bit in the pin control register. When enabled, slew control limits the rate at which an output can transition. This feature reduces the output rise and fall time, so it can help to minimize the radiated emissions generated on output port switching. Slew rate control has no effect on pins which are configured as inputs.

6 Conclusion

EMC design tips are illustrated in this application note to help customers apply EMC considerations in early design phase using Kinetis L MCU. Detail descriptions on hardware and software techniques are listed out as quick reference for customer to adapt Freescale solution more effectively.

7 References

- Freescale application note *EMC Design Considerations for MC9S08PT60* (document AN4438) T.C. Lun., 2012.

- Freescale application note *System Design Guideline for 5V 8-bit families in Home Appliance Applications* (document AN4476) by T.C. Lun, Dennis Lui, 2012.
- Freescale application note *How to Develop a Robust Software in Noise Environment* (document AN4463) by Dennis Lui, T.C. Lun, 2012.
- Freescale application note *Designing for Board Level Electromagnetic Compatibility* (document AN2321) by T.C. Lun, 2002.
- Freescale application note *Improving the Transient Immunity Performance of Microcontroller-Based Applications* (document AN2764) by Ross Carlton, Greg Racino, and John Suchyta, 2005.

8 Revision history

Revision number	Date	Substantive changes
0	06/2013	Initial release

How to Reach Us:

Home Page:

freescale.com

Web Support:

freescale.com/support



Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. Freescale reserves the right to make changes without further notice to any products herein.

Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address:
freescale.com/SalesTermsandConditions.

Freescale, the Freescale logo and Kinetis are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. All other product or service names are the property of their respective owners. ARM is the registered trademark of ARM Limited. Cortex-M0+ is the trademark of ARM Limited.

© 2013 Freescale Semiconductor, Inc.

Document Number: AN4747
Rev. 0, 06/2013
June 03, 2013

