

Bitwise operations support the following operations. The control input values are given for each operation.

Operation	Control Input Values
0000	ZERO
0011	NOT y
0110	x XOR y
1000	x AND y
1100	x OR y
1110	x NOR y
1111	255

NOTE: We are only using one of two available ALU slices in each chip. It is possible to swap which one is used to make routing easier.

NOTE: There are more combinations of control input values. Do they do anything interesting?

Legend:

- BitControl_3
- BitControl_2
- BitControl_1
- BitControl_0

[illegible]

The image displays two circuit diagrams for intermediate latches in a 16-bit adder. Both diagrams are clocked by a common 'CLK' signal.

Left Diagram (First Stage):

- Inputs:** A[15:0] and B[15:0].
- Logic:** The inputs are fed into a 16-bit adder block (labeled 'adder16'). The output of the adder is connected to a 16-bit register block (labeled 'u39').
- Outputs:** The output of the register is labeled 'U39' and is connected to the input of the next stage (labeled 'U40').

Right Diagram (Second Stage):

- Inputs:** A[15:0] and B[15:0].
- Logic:** The inputs are fed into a 16-bit adder block (labeled 'adder16'). The output of the adder is connected to a 16-bit register block (labeled 'u41').
- Outputs:** The output of the register is labeled 'U41' and is connected to the input of the next stage (labeled 'U42').

[illegible]