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Total ionizing dose-hardened carbon nanotube thin-film transistors with silicon oxynitride gate dielectrics

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Abstract

We investigate the radiation response of single-walled carbon nanotube (SWCNT) thin-film transistors fabricated with 23 nm silicon oxynitride gate dielectric layers, for total ionizing doses (TIDs) of Co-60 gamma irradiation up to 2 Mrad(Si). Irradiations with ±1 MV/cm across the gate dielectric have little effect on the threshold voltage, yielding shifts of less than ±0.25 V and no detrimental effect on SWCNT mobility or maximum drain current. This illustrates the need to consider the total device material composition when investigating the radiation response of carbon nanoelectronics and substantiates the applicability of SWCNT-based nanoelectronics for use in high TID environments.

Significant advances in performance, functionality, and high-yield directed self-assembly of single-walled carbon nanotube (SWCNT)-based nanoelectronics continue to shift the technology closer toward adoption in niche terrestrial and space-based applications.[1–6] Regarding space applications, the small cross section and strong bonding structure of SWCNTs may reduce the susceptibility of SWCNT-based transistors [either single-nanotube field-effect transistors or those based on SWCNT thin films (TFTs)] to single event upsets or defect formation. However, total ionizing dose (TID) effects that result from repeated exposure to ionizing radiation primarily degrade the dielectric components of metal oxide semiconductor (MOS) devices and remain the principal vulnerability for SWCNT-TFTs.[7,8] For example, we recently observed a threshold voltage shift of about −0.8 V following a TID of 2 Mrad(Si) for SWCNT-TFTs with a SiO_2 gate oxide of 100 nm.[9] Therefore, developing dielectric materials for TID hardening SWNCT-based devices, by reducing the susceptibility or mitigating the effects of ionizing radiation-induced trapped charge accumulation, is necessary to ensure stable performance characteristics (i.e., threshold voltage, leakage current) when operated in radiation environments.

Presently, we investigate the radiation response of SWCNT-TFTs having scaled silicon oxynitride (SiON) gate dielectrics. The dielectric constant of SiON ranges from $\varepsilon_r = 3.9$ (SiO_2) to $\varepsilon_r = 7.5$ (Si_3N_4), depending on the nitrogen/oxygen ratio,[10] and is often used for radiation hardening of gate dielectrics due to its more balanced hole and electron trapping characteristics.[11] Hardening is achieved by (i) a reduced trapping rate via thinning the gate dielectric layer, and (ii) a compensating trapped charge population that balances the trapped hole and trapped electron charge to yield a net-zero field across the dielectric layer. By combining these techniques, we demonstrate TID-hardened SWCNT-TFTs that show little shift in threshold voltage up to a TID of 2 Mrad(Si) tested under vacuum ($<1 \times 10^{-5}$ Torr).

Figure 1(a) provides a schematic representation of the SWCNT-TFTs under study. A typical fabrication process begins with a p-type Si substrate capped with a thermally grown 1000 Å SiO_2 layer. The wafer is photolithographically patterned and etched using buffered oxide etch (BOE) to expose the Si surface in localized regions that ultimately become the back-gate. Following the BOE etch, we briefly rinse the substrate in H_2O (<10 s), dry with N_2, and immediately load into a plasma-enhanced chemical vapor deposition (PECVD) for dielectric deposition. These steps ensure a pristine hydrogen-passivated Si surface for SiON deposition, which minimizes the density of interface states.[12,13] SiON deposition occurs at 350 °C, 2 Torr, 1500 sccm of N_2, 30 sccm NH_3, and 20 sccm SiH_4, creating a conformal coating over the entire surface as depicted in yellow in Fig. 1(a). We place a BOE-etched Si witness sample alongside the TFT substrate for use in optical thickness measurements following growth. We expose the witness sample to the same thermal

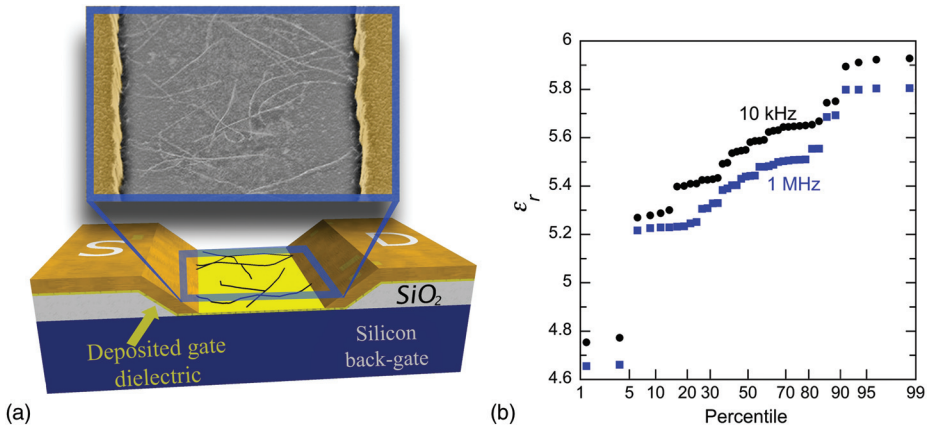

Figure 1. (Color online) (a) Schematic of the locally etched back-gated SWCNT-TFT device depicting the etched layer and a false color SEM image of the SWCNTs within the channel region. The distance between electrodes is 2 μm. (b) Probability plot of capacitor test structure (0.005 cm^2 Au contact, thickness of 23 nm) dielectric constant calculated from capacitance–voltage sweeps measured at 10 kHz (black circles) and 1 MHz (blue squares).

treatment (300 °C for 16 h in air) to match that of the SWCNT-TFTs, which causes the optically measured index of refraction to reduce from 1.97 (near-stoichiometric Si_3N_4) to 1.75. The witness samples are then coated with circular gold pads (0.005 cm^2) using a shadow mask and electron-beam evaporation for capacitance measurements [Fig. 1(b)] and x-ray photoelectron spectroscopy (XPS). The capacitance measurements yielded an average dielectric constant (at 10 kHz) of $\varepsilon_r = 5.6$ (about 75% that of Si_3N_4), and XPS analysis measured 18 at% oxygen and a slightly elevated carbon concentration in comparison with a commercial Si_3N_4 membrane. The remainder of the processing, including the deposition of 98% pure semiconducting SWCNT (purchased from NanoIntegris, Inc.) thin films, and subsequent SWCNT-TFT photolithographic processing are based on the procedure reported in Cress et al.[9] The false-color scanning electron micrograph in Fig. 1(a) illustrates a representative SWCNT thin film between two Ti/Au source–drain electrodes with 2 μm spacing. Prior to testing, devices are vacuum annealed at 125 °C for 16 h at a pressure $<1 \times 10^{-5}$ Torr. We conduct TID testing in the same chamber under static vacuum, with the gate biased during Co-60 γ-irradiation to yield gate electric fields of +0.25, +1.0, and −1.0 MV/cm referenced to the source electrode. The total elapsed time to conduct an irradiation series, i.e., the time under static vacuum, is typically 60 min or less.

The transfer characteristics in Fig. 2(a) illustrate the radiation hardness of the device where we observe only a minor variation in the linear (left axis, solid lines) or subthreshold (right axis, dashed lines) transfer characteristics up to a TID of 2 Mrad(Si). We apply a constant +1 MV/cm gate field during irradiation to provide the electromotive force necessary to separate the electron–hole pairs generated in the gate dielectric by the incident radiation. A +1 MV/cm gate field results in a charge trapping efficiency in SiO_2 gate dielectrics under Co-60 irradiation of about 90%.[14] A positive gate bias drives holes toward the SiON:SWCNT interface, which yields the maximum threshold voltage shift (toward increasing negative gate voltage) if hole trapping is the dominant radiation-induced mechanism. In contrast, under no applied gate field, charge carriers generated within the dielectric layer rapidly recombine having little effect on device performance. The observed stability in transfer characteristics indicates that electrons and holes in the SiON gate dielectric are being generated at a rate that maintains a consistent potential drop between the Si back-gate and the SWCNT channel. Furthermore, we observe a significant radiation-induced increase in gate current (also referred to as photocurrent) increasing from ∼10 pA to ∼2 nA, indicating that a significant fraction of the generated carriers are able to escape from this 23 nm SiON layer by tunneling into the gate electrode. Overall, this leads to an improved stability over our previously reported results of SWCNT-TFTs fabricated on 100 nm SiO_2 gate oxides, which had a maximum shift of −0.8 V after a TID of 2 Mrad(Si) and was irradiated with a gate field of 0.2 MV/cm, which yields a lower charge trapping efficiency (∼40%). For comparison, the observed shift is much less than expected for Si CMOS devices with 23 nm SiO_2 gate oxides, for which we estimate a threshold voltage shift in the range of −0.8 to −1.2 V.[7] Figure 2(b) contains the SWCNT-TFT current–voltage characteristics before and after exposure to 2 Mrad(Si); the gate biases range from −5 to 0 V in steps of 1 V, while the drain–source voltage was swept from 0 to −2 V. Following irradiation, the current–voltage characteristics remain largely unaltered, the main variation being an increased drain current for gate voltages of −3 to −5 V.

Figures 2(c) and 2(d) contain the transfer characteristics and family of curves, respectively, for an SWCNT-TFT device irradiated with a negative gate bias applied yielding a −1 MV/cm field across the SiON gate dielectric. Under such biasing conditions, electrons are driven toward the SiON:SWCNT interface and should yield a positive shift in the transfer characteristics if electron trapping is a dominant

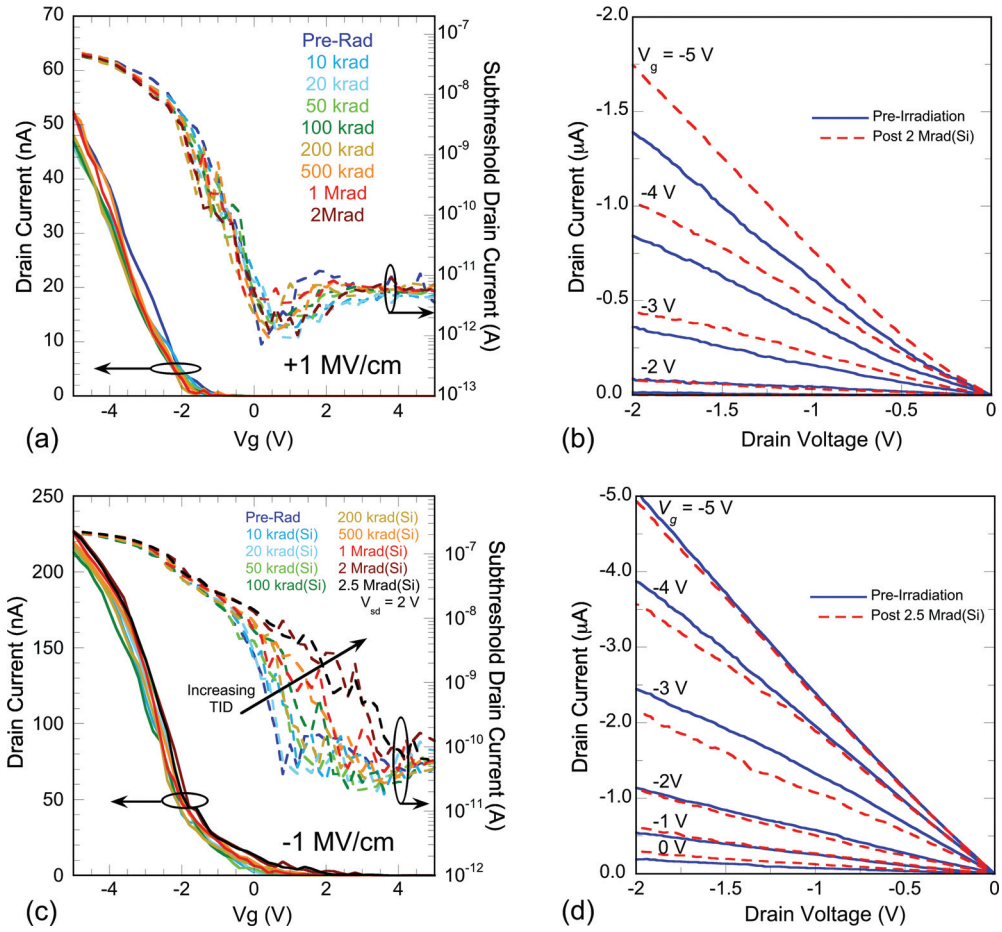

Figure 2. (Color online) (a) Gate transfer characteristics following incremental TIDs. Irradiation was conducted under vacuum with a positive gate electric field of +1 MV/cm. (b) Family of curves for the device in (a) for pre-irradiation (blue, solid lines) and post 2 Mrad(Si) (red, dashed lines). (c) Gate transfer characteristics following incremental TIDs with a negative gate electric field of −1 MV/cm. (d) Corresponding family of curves for the device in (c) for pre-irradiation (blue, solid lines) and post 2.5 Mrad(Si) (red, dashed lines). The gate is biased from −5 to 0 V in +1 V steps for both (b) and (d), and the dose rate for all radiation exposures was 1.1 krad(Si)/s.

radiation-induced mechanism. Like the device reported in Figs. 2(a) and 2(b), we observe little radiation-induced effect on the transfer characteristic in the linear regime, as shown in Fig. 2(c) (left axis, solid lines). However, we do observe an increase in the subthreshold current (leakage current), which trends with TID and corresponds to an increased hole concentration in the SWCNT channels. This increased hole doping may be the result of trapped electrons in the SiON that are driven toward the SiON:SWCNT and screen the electric field of the back-gate. Alternatively, the formation of negatively charged adsorbed molecules on the surface of the SWCNTs would have a similar effect; such molecules may persist through vacuum annealing or are adsorbed during irradiation. For this device we also observe a gate photocurrent, but of opposite sign, supporting the notion of radiation-generated carrier escape from the thin SiON gate dielectric.

Following a TID of 2 Mrad(Si), we investigated the effect of high drain current by applying a V_{sd} of 2 V and exposing the device to an additional 500 krad(Si). This additional biasing during irradiation has little effect on the transfer characteristics, which remain qualitatively similar to the post 2 Mrad(Si) performance.

Figure 3 provides a summary of the change in threshold voltage, mobility, maximum drain current, and drain off-current for three devices irradiated with varying gate biases all monitored *in situ*. For the two high-field biasing conditions (±1 MV/cm), the threshold voltage shifts slightly above and below the pre-irradiation value with the change in threshold voltage ranging between ±0.25 V. In contrast, the change in threshold voltage while irradiated with a +0.25 MV/cm gate field tends toward negative gate bias until ∼100 krad(Si), after which point it begins to recover. This type of behavior may result from holes initially migrating toward the SiON: SWCNT interface: then, with additional TID, a large enough electron trap concentration is formed to compensate the effects of the accumulated holes.[11] Additionally, the lower applied

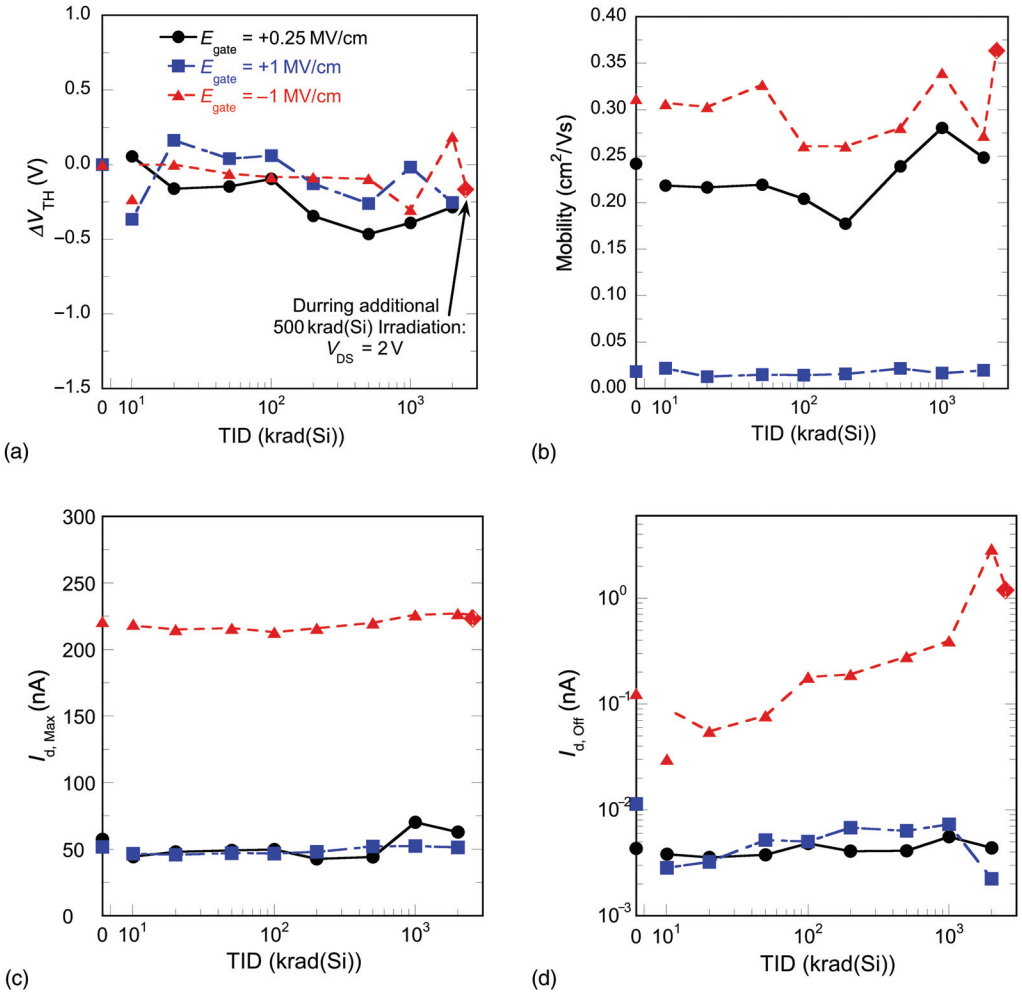

Figure 3. (Color online) (a–d) Change in threshold voltage, mobility, maximum drain current, and drain off-current for three irradiated SWCNT-TFT devices. The devices were irradiated under vacuum with a gate field of +0.25 MV/cm (black lines, circles), +1 MV/cm (blue lines, squares), and −1 MV/cm (red line, triangles). For all −1 MV/cm data, the red diamond at 2.5 Mrad(Si) was measured following an additional 500 krad(Si) with V_{sd} = 2 V during irradiation. The threshold voltage is extracted from the gate transfer characteristics [as shown in Figs. 2(a) and 2(c), along with one additional data set] by taking the *x*-intercept of a tangent line drawn from the point of maximum transconductance (slope).

field may reduce the escape rate of charge carriers generated in the SiON gate dielectric. The mobility and maximum drain current remain essentially unchanged for all devices, reflecting the resilience of SWCNTs to ionizing radiation. The drain off-current corresponds to the drain current at a fixed positive gate bias of 2 V, and reflects the change in leakage current of the devices with increasing TID. This parameter remains nearly constant for the two positive gate field irradiation conditions, but shows an appreciable increase for the −1 MV/cm gate field irradiation condition, reflecting the increased leakage current consistent with Fig. 2(c). However, the subthreshold swings for irradiation conditions with gate fields of +0.25, +1.0, and −1.0 MV/cm remained consistent and averaged 377, 435, and 505 mV/decade, respectively. The higher average subthreshold swing for the device irradiated with a negative gate field reflects a higher SWCNT channel capacitance, perhaps due to SWCNT bundles or a higher density network, while the consistency of the subthreshold swing with TID indicates that leakage current increases result from local trapped charges rather than radiation-induced changes in the SWCNT transport properties.

We have demonstrated radiation-hardened SWCNT-TFTs using a SiON gate dielectric with threshold voltage shifts of <0.25 V for a TID of 2 Mrad(Si), and which show no statistically significant changes in mobility or maximum drain current. The extreme radiation tolerance observed in the SWCNT-TFTs results from the combined effects of a thin gate dielectric and the compensating trap population that is formed in PECVD SiON. Physically, this implies that radiation-generated charge carriers are able to escape the thin SiON layer, and the electron and hole trapping rates are nearly equal. Based on the results of the device irradiated under reverse bias, SiON may have a

slight propensity to favor electron trapping over hole trapping since a slight increase in subthreshold current was observed. However, this may also result from electron injection into adsorbed molecules on the surface of the SWCNTs not removed by vacuum annealing. This demonstration confirms the TID hardness of SWCNTs and further supports the development of SWCNT-based nanoelectronics for radiation environments.

Acknowledgments

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