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Demonstration of a *nipi*-diode photovoltaic

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ABSTRACT

The simulation, growth, processing, and characterization of a three-period GaAs n-type/intrinsic/p-type/intrinsic . . . (*nipi*) doping solar cell is demonstrated. A V-groove etching process is characterized and used to expose the multiple n-type and p-type layers for electrical connection made by interdigitated grid-finger electrodes. A five-layer photolithographic process flow is developed and used to make $1 \times 1\,cm^2$ devices with varying grid-finger separation. Device simulations of the structure indicate that strong rectification can be achieved in the parallel-connected three period *nipi* GaAs solar cell structure provided the necessary semiconductor doping compensation is achieved in the region near the metal-semiconductor interfaces. Experimentally, the improvements observed in the open circuit voltage, short circuit current, and ideality of the devices following thermal annealing suggests the formation of barriers near the contacts, which support the simulation results. A comparison of the short circuit current and series resistance under illumination indicate a tradeoff between shadowing and series resistance, which may be overcome with modification to the device structure. Ultimately, these results show promise towards the development of high efficiency solar cells or radioisotope batteries, and offer a novel device structure for the incorporation of nano-structures such as quantum wells or quantum dots. Copyright © 2010 John Wiley & Sons, Ltd.

KEYWORDS

nipi diode; solar cell modeling; quantum dot solar cell; quantum well solar cell; band structure engineering; ohmic contact; etching GaAs

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1. INTRODUCTION

A *nipi*-diode is comprised of periodically n-type/intrinsic/p-type/intrinsic (*nipi*) doped layers forming a multi-junction device. When lateral electrical contact is made to the doped layers as depicted in Figure 1, a parallel-connected multi-junction device is formed. In *nipi*-diodes, the periodic doping structure results in a sinusoidal-like band structure along the growth direction. As a result, minority carriers formed anywhere within the device are exposed to a strong electric field which rapidly sweeps them toward the proximal junction either above or below. Therefore, carrier extraction is drift-field dependent, which enhances the extraction efficiency and reduces the susceptibility of minority carriers to recombination at defect sites [1]. Furthermore, with sufficiently narrow layers and high doping, the pure crystal energy bands are split into subbands, which are of the Bloch form [2]. The carrier-concentration dependent aspects of the resulting *nipi*-superlattice structure have been experimentally demonstrated in light emitting diodes, in which the emission energy can be tuned by nearly 1/3 the bandgap with increased electrical bias [3].

Outside the superlattice regime, the properties of *nipi*-diodes remain attractive for a number of power generation devices, such as photo-, alpha-, or beta-voltaics. All of these devices rely on the rapid separation and transport of charge carriers to lateral contacts made at adjacent edges of the doped structure. As a direct-conversion radioisotope battery, where the energy deposited by alpha or beta particles is converted into electricity, the tailorable thickness of the *nipi*-diode structure can be utilized to ensure full energy deposition of the incident radiant energy [4] and the field assisted carrier separation can lead to

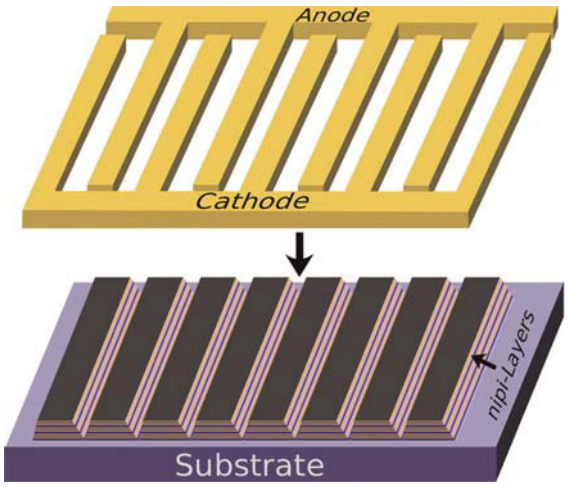

Figure 1. Schematic illustrating the interdigitated contacts that are deposited onto an array of V-groove etched mesa structures consisting of periodically doped *nipi*-epitaxial layers forming a macroscopic device.

enhanced radiation tolerance increasing the lifetime of the device [1]. These aspects are also ideal for photovoltaic power generation, especially in harsh environments, such as those found in space, where resilience to high temperatures and ionizing radiation is a necessity [4,5].

A promising area of research for *nipi*-diode structures may be to combine them with the emergent field of nano-structured photovoltaics including quantum well and quantum dot solar cells [6,7]. Nano-structured solar cells utilize the size-dependent optoelectronic properties of quantum dots and quantum wells to tune the spectral absorption range and improve the overall power conversion efficiency of single and multi-junction (series connected) solar cells [8]. Currently, a limiting feature of these technologies is the number of nano-structured layers that can be grown within the device, especially for quantum dot solar cells [7,9–11]. Therefore, the *nipi*-diode structure can be used to distribute the nano-structured layers across many thin junctions thereby maintaining the high-field to assist in the carrier extraction while avoiding the detrimental effects of strain/nano-structure induced defects formed within the devices [12]. Furthermore, thinning the layers of the *nipi*-diode to achieve a *nipi*-superlattice, used in conjunction with the size dependent electronic confinement in the nano-structures, may be paramount to achieving efficient photon absorption within, and carrier transport out of, the nano-structures. The ability to tailor the band structure of the nano-structures and the *nipi*-supperlattice host [2,3,13] yields an additional degree of freedom for band structure engineering allowing the optimal band alignment to be achieved.

Successful development of a *nipi*-diode device requires precise doping profiles and a method for selectively contacting all of the n- and p-type layers at isolated contacts. Abrupt doping profiles comprising donor and acceptor atoms have been achievable with molecular beam epitaxy (MBE) and organometallic vapor phase epitaxy (OMVPE) for many years and have been demonstrated in a number of materials systems. However, ohmic contacts that are selective to the n- or p-type layers have been more difficult to achieve and have generally been approached by two different techniques. A smart metallization scheme has been employed which relies on compensating the semiconductor material near the contacts by thermal diffusion of an appropriate dopant contained in deposited metal–alloy contacts during annealing [14]. Ion implantation followed by metal deposition has also been used with slightly better results in high-frequency *nipi*-multiple quantum well optical modulators [15]. *In situ* growth techniques have also been used to achieve selectively doped regions. Hasnain *et al*., utilized a procedure where shadow masking of the dopant beam within the MBE growth chamber was able to achieve selectively doped regions in GaAs (with $\sim$1 mm pitch) that yielded low resistance contacts [16]. A similar method was used to form selectively doped regions for contacting Si *nipi*-doped structures [17].

In the present work, the design, fabrication, and experimental results of a three period GaAs *nipi*-diode photovoltaic device is demonstrated. A three period *nipi* device with thick layers (200–1,000 nm) was chosen so as to reduce the complexity of the growth while maintaining a sufficiently large absorption cross section. As a result, the layer thicknesses of the device fabricated are greater than that necessary to achieve carrier confinement effects [13], so the advantages of increased lifetimes are sacrificed in place of reduced series resistance and larger contact area with thicker layers. A device simulation has been performed to assist in understanding the fields and carrier transport within a device, with an emphasis on carrier transport in the doped layers near the lateral contacts. Experimentally, a V-groove etching scheme was developed and the smart metallization technique was employed to make selective ohmic contact to the doped layers of the device. Full characterization of the device photovoltaic performance including dark and illuminated current–voltage measurements and external quantum efficiency (EQE) are provided. This paper concludes with an investigation into the effects of series resistance within the device and a discussion regarding the implications of the results demonstrated.

2. EXPERIMENTAL

The devices in this study were grown using OMVPE on semi-insulating (100) GaAs wafers off-cut 2° towards the <110>. Standard precursors of trimethylgallium, trimethylindium, phosphine, and arsine were used for alkyl and hydride sources, respectively. The n- and p-type layers were doped using disilane and diethylzinc, respectively. A cross sectional scanning electron microscope (SEM) image of the fabricated *nipi*-diode, is provided in Figure 2. In this

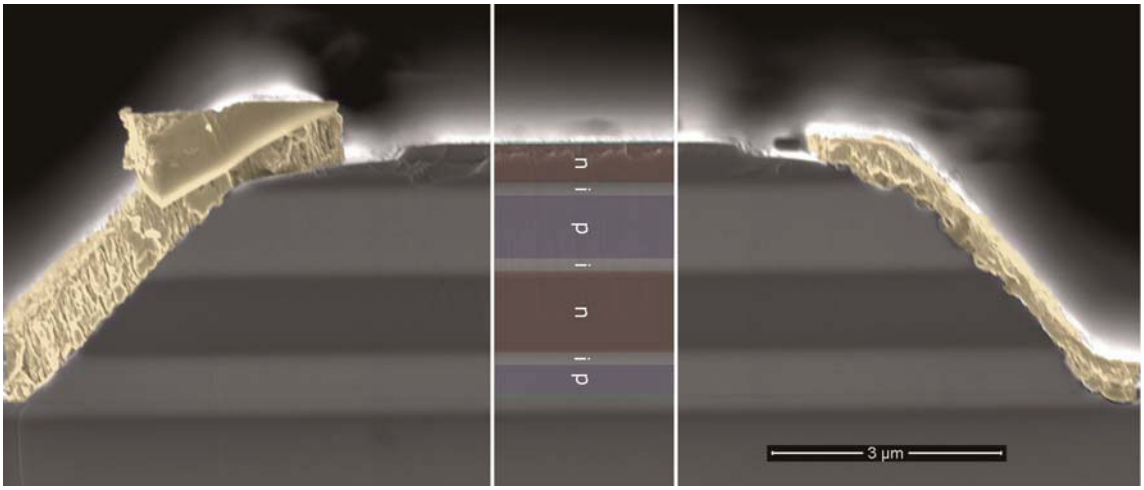

Figure 2. Scanning electron microscope image depicting the layers of the *nipi*-diode. False coloring is provided to better differentiate the n-type (red), p-type (blue), and intrinsic (white) GaAs layers, the $InGaP_2$ (green), and metal contacts (gold).

figure, false coloring was used to emphasize the alternating n-type, intrinsic, and p-type layers. The device was isolated from the substrate using a 50 nm p^+ $InGaP_2$ back surface field layer which also acts as an etch stop (colored green in the figure). The $InGaP_2$ ($In_{0.49}Ga_{0.51}P$) was grown lattice matched to the GaAs substrate with <0.1% residual strain as confirmed by X-ray diffraction. The bottom most p-type GaAs layer and the top n-type GaAs layer are 500 nm thick since they are adjacent to only a single layer, while the two middle doped regions are both 1,000 nm thick. All intrinsic regions were grown 200 nm thick. The thicknesses of the doped layers were chosen to be <1 diffusion length for both charge carriers and to be of sufficient thickness to minimize resistive losses for carriers transported laterally to the contacts. Finally, the surface of the device is capped with an n^+ $InGaP_2$ window layer to passivate surface states thereby reducing the surface recombination velocity in the top n-type layer.

A key feature of the device is to achieve low-aspect ratio V-grooves to maximize the surface area between the metal contacts and the *nipi*-layers to reduce contact resistance. To etch V-groove profiles in GaAs, a solution of sulfuric acid (33%), hydrogen peroxide (90%), and deionized water in a volume ratio of 4:1:5 was used. When being prepared the solution rapidly heats to a temperature in excess of 70°C, and therefore was allowed to cool to room temperature prior to etching the GaAs to ensure anisotropic etching. For this etchant, the orientation of the wafer and the orientation of the patterned lines are critical in achieving V-groove structures. The wafer orientation used here is (100) with the grid lines perpendicular to the major flat, or along the $<01\bar{1}>$. Anisotropic etching results from the different reactivity of the 4:1:5 solution between the anion (As) and the cation (Ga). Since the solution reacts faster with As, the Ga terminated (111) and $(1\bar{1}\bar{1})$ etch at a slower rate than the (100) resulting in the slanted sidewalls observed in the SEM image. Three test bulk GaAs samples were pattered with grid fingers using photolithography and etched for 1–30 s followed by immersion in deionized water. The depth and undercutting amounts were measured using cross sectional scanning electron microscopy and used to determine the depth and undercutting etch rates. A depth etch rate of 155 nm/s was determined with a depth-to-undercut ratio of 3.3. This ratio indicates that significant undercutting will occur for devices comprising active regions that are in excess of 1 μm. Therefore, the photolithographic contact masks were designed with 10 μm V-groove etch openings and 20 μm metal grid-finger widths.

Standard photolithographic processing was used to pattern test samples for etching studies and for device processing. Full processing of the *nipi*-diodes consists of five lithographic layers including Alignment, V-groove etch, Metal-1, Metal-2, and Mesa etch. The Alignment layer consisted of 50 nm of electron-beam deposited Ti to serve as a layer that all subsequent lithographic steps are aligned to. This is necessary because the deep etching, and corresponding undercutting, makes it difficult to align to the V-groove etch layer. V-groove etching then followed, which exposed the edges of the *nipi*-layers on which interdigitated electrode fingers extending from larger bus-bars located at opposite ends of the devices were subsequently deposited (see Figure 1). The n-type metal alloy contacts, consisting of 250 Å Ge, 500 Å Au, 350 Å Ni, and 10,000 Å of Au, were then deposited using thermal evaporation. Following lift off in acetone, another layer of photoresist was patterned to define the p-type contact layer, followed by thermal evaporation deposition of 200 Å Au, 200 Å Zn, and 3,400 Å Au. The wafers were annealed at 410°C for 10 min in nitrogen ambient to reduce the contact resistance and to alloy the metal contacts promoting diffusion into the semiconductor, thereby improving the contact selectivity. Finally, the $1 \times 1\,cm^2$ devices were mesa-isolated by etching the $InGaP_2$ window

with HCl for 10 s followed by an isotropic GaAs etch in a solution of H_2O_2:H_3PO_4:H_2O (4:3:1); the back window serves as an etch stop for this step. Two-inch GaAs wafers were processed with a total of 12 devices, 3 devices each with grid-finger separations of 40, 90, 190, and 490 μm; a constant 20 μm grid-finger width was used for all devices. No anti-reflection coatings were applied.

Solar cell current–voltage characteristics of the devices were measured under one-sun air mass zero (AM0) illumination conditions provided by a 1,000 W Oriel solar simulator with AM0 filtering. Verification of one-sun AM0 illumination intensity is performed before all testing by adjusting the bulb intensity to obtain the rated short circuit current of a GaAs calibration cell supplied by the NASA Glenn Research Center. Solar cell spectral responsivity measurements were measured using an OL Series 750 spectroradiometric measurement system with high-intensity light source attached.

3. DEVICE SIMULATION

Device simulations of the *nipi*-diode photovoltaic identified the properties of the selective contacts that are necessary to achieve optimal performance. The device simulation proceeded by simulating the process flow using Silvaco-Athena. Subsequent analysis in Silvaco-Atlas illustrated the band structure and electric field distribution within the device, especially near the contact regions. Two configurations were simulated; the first assumed no dopant diffusion occurs resulting in ohmic and rectifying Schottky contacts to the doped layers. The second configuration included a re-growth of 200 nm degenerately n-type and p-type doped GaAs inserted between the metal contacts and the *nipi*-layers at the cathode and anode, respectively. The latter was designed to provide the best-case device performance for a *nipi*-diode as optimal selectivity of the contacts is achieved.

Considering the work function of the cathode metallization AuGe, ∼5.15 eV, and the anode metallization AuZn,∼4.73 eV, in comparison to the work function of n-type GaAs, ∼4.12 eV, both metallization schemes will serve as Schottky ohmic contacts for minority carrier holes since no barriers exist. This is depicted in Figure 3a where the holes (+) can diffuse unobstructed to either electrode. Conversely, for majority carrier electrons in the n-type layer barriers of 1.08 and 0.66 eV exist at the cathode and anode, respectively. Therefore, in the standard Ge–Au–Ni–Au contact metallization scheme, a Schottky tunnel contact is formed where transport of electrons proceeds by tunneling through the narrow Schottky barrier. As depicted in Figure 3b, a similar band structure exists for metal contact made to p-type GaAs (work function ∼5.4 eV), where Schottky ohmic contact is achieved for the minority carrier electrons and a Schottky tunnel contact results for the majority carrier holes. By type-compensating the semiconductor adjacent to these contacts, holes and electrons can be driven away from the opposite electrode

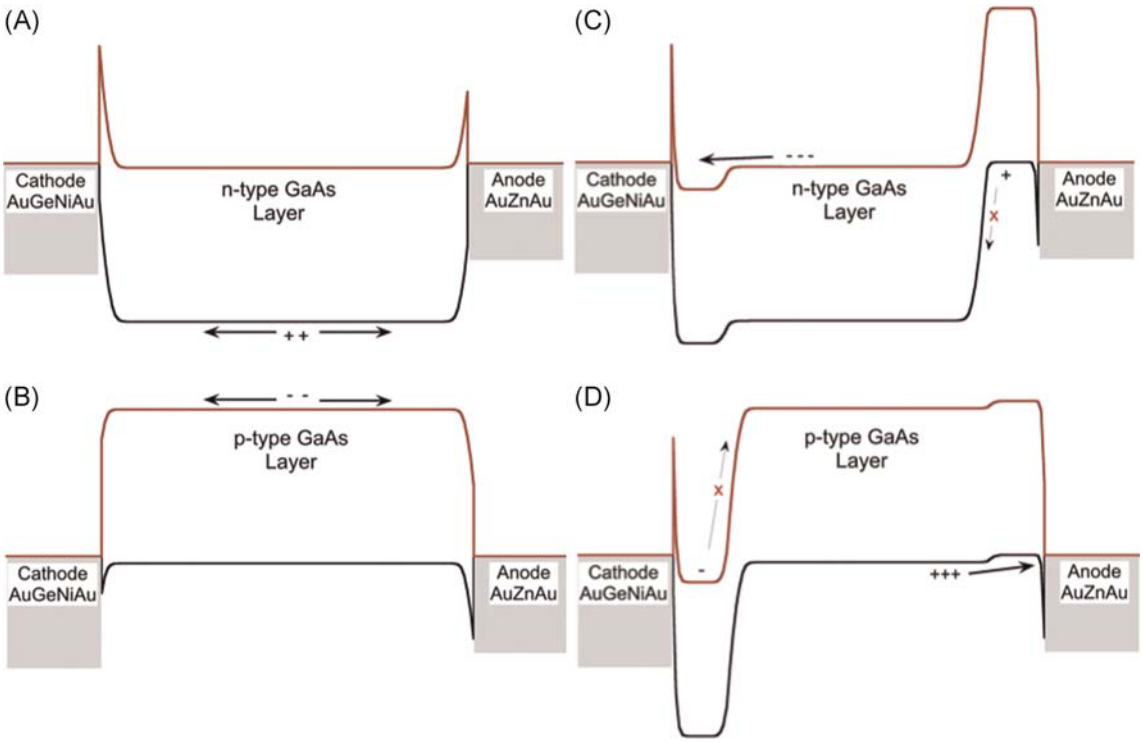

Figure 3. Band structures in the direction parallel to the *nipi*-layers for (A) an n-type layer, (B) a p-type layer, (C) n-type layer with diffused contacts, and (D) a p-type layer with diffused contacts.

by the lateral p–n junction formed. Though transport of holes in the p-type layers into n-type contact is still energetically favorable, the type compensation introduces a narrow region of higher potential opposing this transport path. The effect of these thin diffused regions are illustrated in Figure 3c,d for n and p-type GaAs layers, respectively.

In general, the band structure simulation results above indicate that in an ideal structure, a diode that achieves good rectification can be obtained. When compared to a traditional planar solar cell, the main loss observed in a *nipi*-diode is an increased dark current and reduced shunt resistance. Both of these terms are expected to vary in proportion with total junction area including the number of vertical *nipi* junctions, and the lateral p–n junctions adjacent to the metal contacts [4]. Series resistance may also become a hindrance at higher current levels. However, a practical issue associated with the selective contacting scheme employed here is the lack of rectification resulting in a partial electric short at the contact between adjacent layers. Assuming ohmic contact is achieved with one of the layers, the maximum achievable open circuit voltage would then become the difference in work functions between the metal alloy contact and the semiconductor of the opposite polarity.

4. RESULTS AND DISCUSSION

Dark and AM0 illumination current density–voltage (*J–V*) characterization of the device pre- and post-annealing at 410°C is provided in Figure 4. The data shown here is from the best performing device measured, which has a grid-finger spacing of 90 μm. Prior to annealing, the contact metallization has not been alloyed and therefore at best is providing a Schottky type rectification to both the n- and p-type layers. A large dark current is observed in Figure 4a, with no evidence of a transition from a recombination dominated to a diffusion dominated current regime.

The dark current improves following anneal and an inflection in the *J–V* characteristics is observed at approximately 0.31 V. This is indicative of improved rectification in the device and likely results from reduced recombination and leakage currents at or near the metal-semiconductor interface (MSI) region. Slight diffusion of the dopants contained within the deposited metal contacts form a MSI with a small potential energy barrier helping to reflect charge carriers towards their respective metal contacts rather than acting as a region of high recombination. A least squares curve fit of the post anneal dark *J–V* characteristics to a two diode model including series resistance yielded saturation currents and ideality parameters of $J_1 = 1.8 \times 10^{-7}$ A/cm^2, $n_1 = 1.88$, $J_2 = 5.3 \times 10^{-6}$ A/cm^2, $n_2 = 2.11$, and a shunt and series resistance of 1.01 kΩ and 0.52 Ω, respectively. The lower contribution and better ideality of the first fitting parameters correspond with the higher voltage range, while the second parameters describe the lower voltage range of the curve where recombination current dominates.

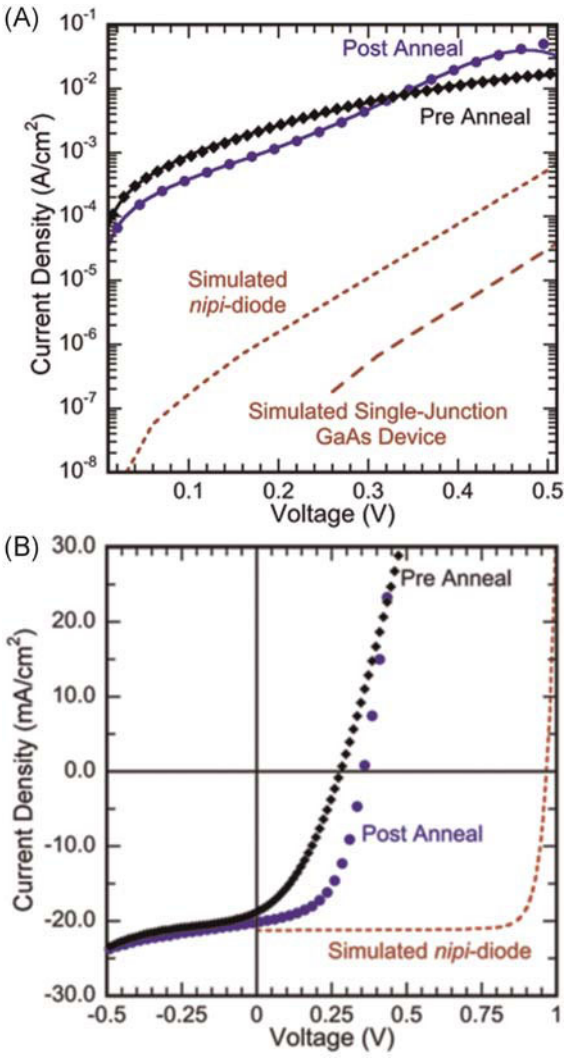

Figure 4. (a) Dark and (b) AM0 illuminated current–voltage characteristics of the *nipi*-diode with 90 μm grid-finger spacing before and after contact annealing. The red dashed lines depict the dark and illuminated current-voltage characteristics for the simulated *nipi*-diode, while the large red dashed line is the dark current-voltage characteristics for a GaAs solar cell with a traditional single-junction design.

At higher voltage, this ideality value is consistent with that obtained for the simulated *nipi*-diode device dark current (red-dashed line) although the overall dark current is 2 orders of magnitude greater due to the low shunt resistance, which is typically on the order of 10^6 Ω for GaAs devices. Prior to the anneal, only a single diode is needed to fit the model, yielding a saturation current and ideality of $J_2 = 1.74 \times 10^{-4}$ and $n_2 = 4.45$, the shunt resistance was nearly the same (1.2 kΩ) while the 2.75 Ω series resistance was much higher prior to annealing. This comparison illustrates the importance of proper band alignment near the contacts, as it is capable of improving the ideality and reducing the dark currents of the device.

The illuminated *J–V* characteristics, shown in Figure 4b further emphasize the improvement achieved following anneal. Before anneal, a short circuit current density of $J_{sc} = 19.3\,mA/cm^2$ and an open circuit voltage of $V_{oc} = 0.28\,V$ were measured. The illuminated *J–V* characteristics following anneal also show evidence of localized compensation and improved contacts as the fill factor of the device is increased significantly (from 36% to 53%), the J_{sc} increased to $20.7\,mA/cm^2$ and the V_{oc} increased to 0.36 V. The simulated *nipi*-diode has a V_{oc} of 0.95 V, which is slightly lower than typical single junction GaAs devices (e.g., 1.04 V is typical [7]), while the simulated J_{sc} of $21.3\,mA/cm^2$ is similar to the results obtained indicating good collection by the device. The lower measured V_{oc} is indicative of increased recombination current, possibly at the interfaces. However, the good agreement in short circuit current with simulation shows that the overall material quality, for example, diffusion length, has been maintained. Overall, a measured AM0 efficiency of 3.17% was achieved, which is significant considering the low shunt resistance and large grid-finger shadowing.

The shadow corrected EQE spectra of the best performing devices with 490 and 40 μm grid-finger separations are depicted in Figure 5. In both spectra, the band-edge occurs at ~870 nm and the absorption cut-off of the $InGaP_2$ window layer is clearly apparent between 660 and 680 nm (bandgap of $InGaP_2 = 1.85\,eV$ or ~670 nm). These EQE characteristics are typical for GaAs and indicate that the front surface recombination is low and there is minimal loss of carriers generated deeper into the devices. However, slightly enhanced short wavelength (<670 nm) and reduced long wavelength (>670 nm) carrier collection is observed in the device with 40 μm grid-finger separation. This suggests that reducing the grid-finger separation improves the collection efficiency of carriers in the top most *nip* junction while slightly reducing the efficiency of the bottom most *pin* junction. The large absorption coefficient of GaAs causes much of the light to be absorbed in the top most *nip* region. Therefore, reducing the collection distance may reduce internal series resistance losses in that region. However, reducing the grid-finger separation has the additional effect of increasing the relative fraction of shadowed area in the bottom most cell from 2% to 20%. Recombination and low injection effects can dominate in the shadowed region and are likely causing the reduced EQE for this device at longer wavelengths (>700 nm).

The effects of grid-finger separation on the short circuit current and on the series resistance can be observed in Figure 6. Here, the average J_{sc} and series resistances, obtained from curve fits of the linear portion of the illuminated *J–V* curves at high voltages (>0.45 V) where series resistance dominates, are plotted as a function of the grid-finger separation. The error bars correspond with 1 standard deviation from the mean. Under illumination, current in the device must travel laterally within each of the thin-doped layers resulting in a non-linear current increase and concomitant spreading resistance increase as the current flows to the electrodes. The resulting series resistance is much greater than that obtained from series resistance fitted under dark conditions since the current will be more uniformly injected into all of the layers. As shown in Figure 6, wider grid-finger separation increases the J_{sc} by 33% from 16.8 to $22.3\,mA/cm^2$, which is consistent with the difference in shadowing which reduces from 36.5% to 7.9% for the 40 and 490 μm grid-finger separations, respectively. However, increased grid-finger separation has the unwanted effect of increased illuminated series resistance, which increases from an average of about 4 Ω to nearly 9 Ω. For this particular set of devices, a grid-finger separation between 90 and 190 μm is likely to yield a device structure that balances these competing effects.

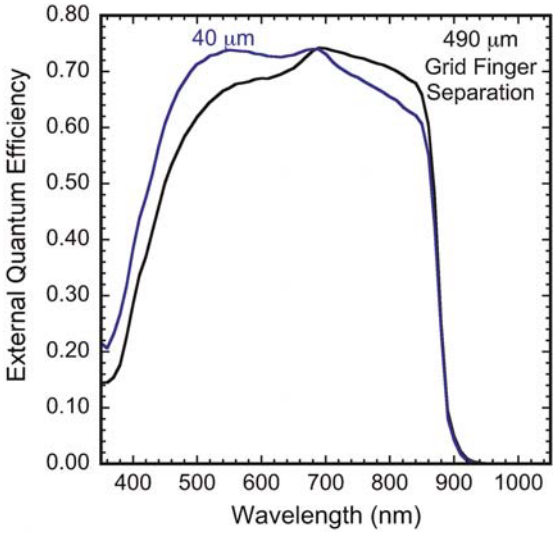

Figure 5. Shadow corrected external quantum efficiency of *nipi*-diodes with grid-finger spacing of 40 and 490 μm.

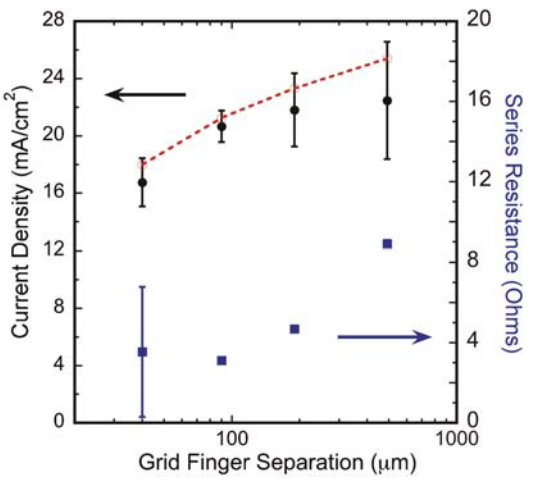

Figure 6. Variation in short circuit current density (black circles) and series resistance (blue squares) as a function of grid-finger spacing. Error marks indicate one standard deviation from the mean value.

Finally, the red-dashed line in Figure 6 shows the simulated *nipi*-diode short circuit current values for each of the four grid-finger separations. These simulations results are slightly higher than the experimentally measured values, but follow a similar trend that indicates contact shadowing is the dominant factor. In general, these results suggest that the *nipi*-diodes demonstrated hear are near ideal for current collection and need slightly better contact rectification to achieve high efficiency.

The experimental and simulation results presented provide an in depth understanding of device operation and elucidate a number of different steps that may be identified to further improve the device performance. Foremost, the reduced V_{oc}, when compared to simulation, implies that improved barriers to leakage current at the contacts are needed. The simulations results indicate that this can be achieved by compensating the semiconductor in the region adjacent to the metal contacts to form lateral p–n junctions. As demonstrated in previous work, this could be accomplished using two ion-implantation and drive-in annealing steps prior to metallization to form locally doped n- and p-type regions [15]. Alternatively, re-growth of heavily doped GaAs in the V-groove trenches could be used to increase the barrier width and maintain defect free GaAs in the MSI region [18].

The trade-off between shadowing and series resistance must be addressed especially for devices with thinner *nipi* layers. One alternative would be to metallize nearly the entire front surface (maintaining a thin separation between the cathode and anode contacts) and etching though the structure or using a lift-off process like that used for the inverted metamorphic solar cell [19], to illuminate the structure through the bottom. In such a device, the metallization would serve as a reflector for transmitted light as well as the light that is incident on the angled region of the V-groove, which is lost in the top-illuminated design. Such a structure would provide further benefit if nanostructures are incorporated, such as quantum wells, as it would increase their effective absorption cross section and align the electric field parallel with *z*-axis of the structure which may help improve the absorption probability for intersubband transitions.

5. CONCLUSION

A three-period GaAs *nipi*-diode solar cell was simulated, grown by OMVPE, processed, and tested. A V-groove etching scheme was developed to expose regions of the multi-junction structure for contact metallization. Thermally deposited metal–alloy contacts, which were designed to make ohmic contact selectively to either n- or p-type GaAs were deposited in alternating V-groove trenches to form $1 \times 1\,cm^2$ solar cell devices with interpenetrating grid fingers with spacing ranging from 40 to 490 μm. Dark characteristics of the devices showed significant improvement with annealing due to improved diffused barriers near the contacts, while the short circuit current and EQE of the devices were similar to standard GaAs devices. However, the overall device performance was reduced in comparison with standard GaAs solar cells, mainly due to a high dark current and correspondingly low open circuit voltage. Results of device simulations indicate that good rectification can be achieved in *nipi*-diodes provided the necessary band structure is obtained near the contacts. Suggestions to the device structure in which ion-implantation or re-growth of heavily doped GaAs is used to improve the band alignment were proposed. Furthermore, a bottom illumination scheme, formed by etching the substrate or using a lift-off process, was suggested as a possible method for reducing the effects of shadowing and series resistances. This structure may have an additional benefit for the incorporation of nanostructures as it increases the absorption cross-section and properly aligns the electric field of reflected photons for improved absorption probability.

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