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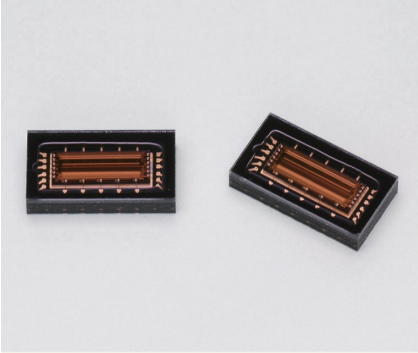
NEW

Distance linear image sensor



S11961-01CR

Measures the distance to an object by TOF (Time-Of-Flight) method

The distance image sensors are designed to measure the distance to an object by TOF method. When used in combination with a pulse modulated light source, this sensor outputs phase difference information on the timing that the light is emitted and received. The sensor output signals are arithmetically processed by an external signal processing circuit or a PC to obtain distance data.

Features

- **High-speed charge transfer structure**
- **Wide dynamic range, low noise by non-destructive readout**
- **Operates with minimal detection errors even under fluctuating (charge drain function)**
- **Real-time distance measurement**

Applications

- **Obstacle detection (self-driving, robots, etc.)**
- **Security (intrusion detection, etc.)**
- **Shape recognition (logistics, robots, etc.)**
- **Motion capture**

Structure

Parameter	Specification	Unit
Image size	5.12 × 0.05	mm
Pixel pitch	20	µm
Pixel height	50	µm
Number of pixels	272	pixels
Number of effective pixels	256	pixels
Package	22-pin PWB	-
Window material	AR-coated glass	-

Note: This product is not hermetically sealed.

Absolute maximum ratings

Parameter		Symbol	Condition	Value	Unit
Analog supply voltage		Vdd(A)	Ta=25 °C	-0.3 to +6	V
Digital supply voltage		Vdd(D)	Ta=25 °C	-0.3 to +6	V
Analog input terminal voltage	Pixel amplifier	Vsf	Ta=25 °C	-0.3 to Vdd(A) + 0.3	V
	Pixel reset	Vr			
	Photosensitive area	Vpg			
Digital input terminal voltage	Pixel reset pulse	p_res	Ta=25 °C	-0.3 to Vdd(D) + 0.3	V
	Signal sampling pulse	phis			
	Master clock pulse	mclk			
	Signal readout trigger pulse	trig			
	Output signal synchronous pulse	dclk			
Charge transfer clock pulse voltage		VTX1, VTX2, VTX3	Ta=25 °C	-0.3 to Vdd(A) + 0.3	V
Operating temperature		Topr	No condensation	-25 to +85	°C
Storage temperature		Tstg	No condensation	-40 to +100	°C
Reflow soldering conditions*1		Tsol		260 °C max. 2 times (see P.8)	-

*1: JEDEC level 3

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Recommended terminal voltage (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Analog supply voltage		Vdd(A)	4.75	5	5.25	V
Digital supply voltage		Vdd(D)	4.75	5	5.25	V
Bias voltage	Pixel amplifier	Vsf	4.5	5	Vdd(A)	V
	Pixel reset	Vr	4	4.25	4.5	V
	Photosensitive area	Vpg	0.8	1.0	1.2	V
Pixel reset pulse voltage	High level	p_res	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	
Signal sampling pulse voltage	High level	phis	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	
Master clock pulse voltage	High level	mclk	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	
Signal readout trigger pulse voltage	High level	trig	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	
Output signal synchronous pulse voltage	High level	dclk	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	

Electrical characteristics [Ta=25 °C, Vdd(A)=Vdd(D)=5 V]

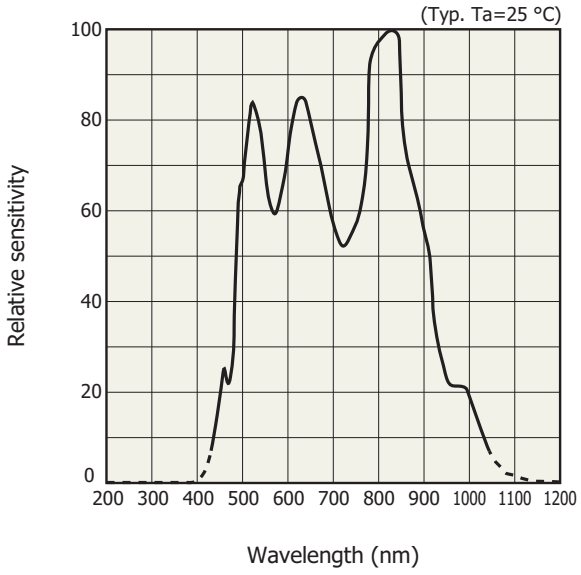
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock pulse frequency	f(mclk)		1 M	-	5 M	Hz
Video data rate	VR		-	f(mclk)	-	Hz
Current consumption	Ic	Dark state	-	15	30	mA

Electrical and optical characteristics [Ta=25 °C, Vdd(A)=Vdd(D)=5 V, Vsf=5 V, Vr=4.25 V, MCLK=5 MHz]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Spectral response range	λ		400 to 1100		nm
Peak sensitivity wavelength	λp	-	800	-	nm
Photosensitivity*2	S	1.05×10^{12}	2.1×10^{12}	4.2×10^{12}	V/W·s
Dark output	Vd	-	0.5	10	V/s
Random noise	RN	-	0.4	0.8	mV rms
Dark output voltage*3	Vor	2.95	3.3	4.35	V
Saturation output voltage	Vsat	-	-	2	V
Sensitivity ratio*4	SR	0.7	-	1.43	-
Photoresponse nonuniformity*5	PRNU	-	-	±10	%

*2: Monochromatic wavelength source (λ=805 nm)
*3: Output voltage right after reset in dark state
*4: Sensitivity ratio of Vout1 (VTX1=3 V, VTX2=VTX3=0 V) to Vout2 (VTX2=3 V, VTX1=VTX3=0 V)
*5: Photoresponse nonuniformity (PRNU) is the output nonuniformity that occurs when the entire photosensitive area is uniformly illuminated by light which is 50% of the saturation exposure level. PRNU is measured using 256 pixels excluding 8 pixels each at both ends, and is defined as follow:
PRNU = ΔX/X × 100 [%]
X: average output of all pixels, ΔX: difference between X and maximum or minimum output

Spectral response



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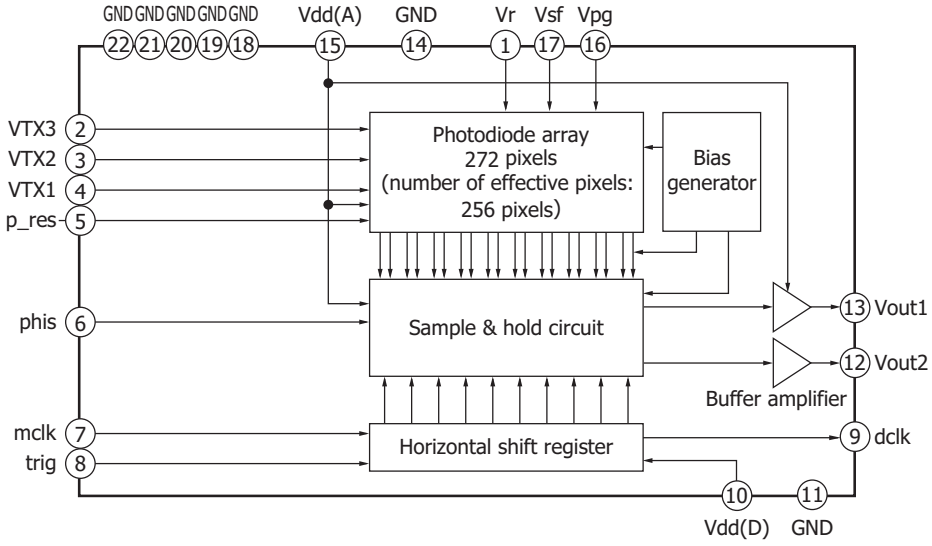
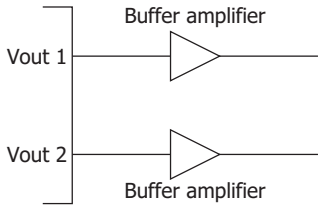
Block diagram



KMPDC0430EC

Basic connection example



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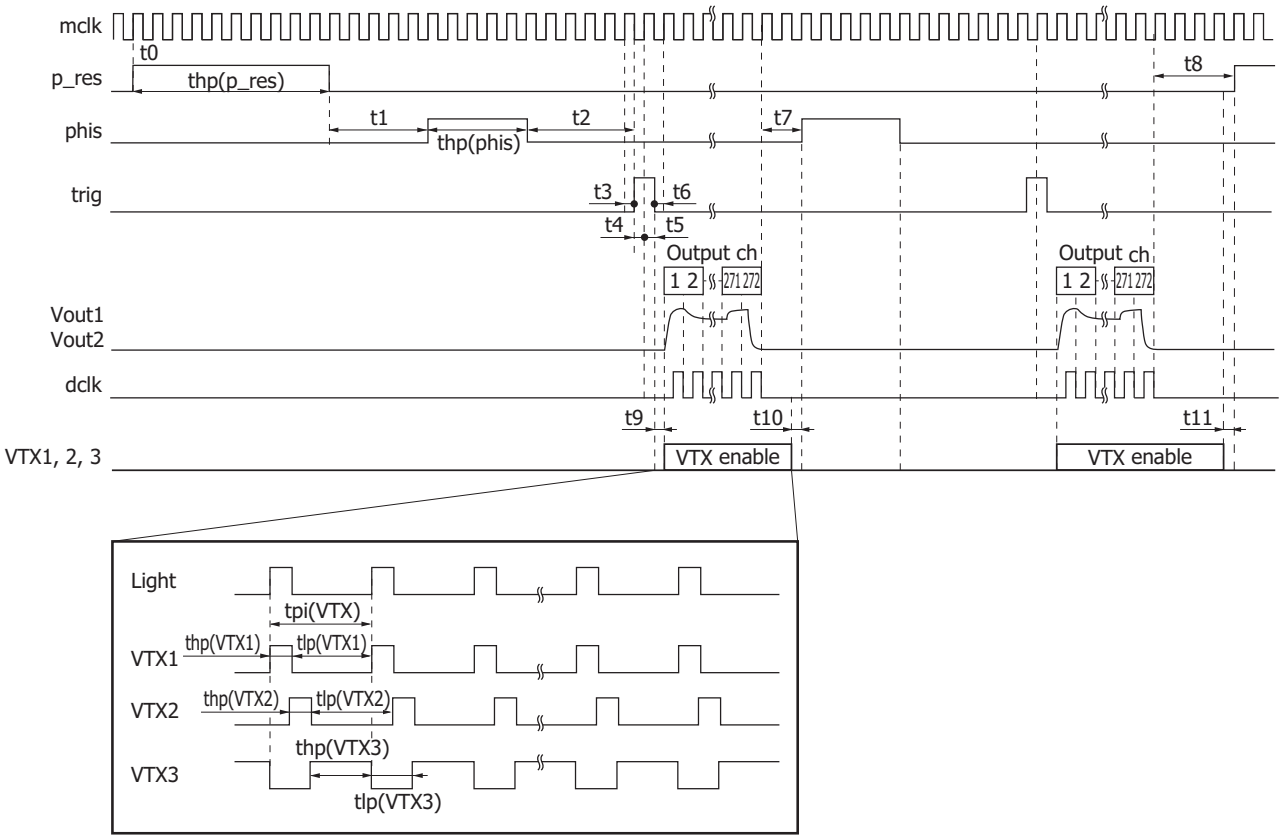
Timing chart



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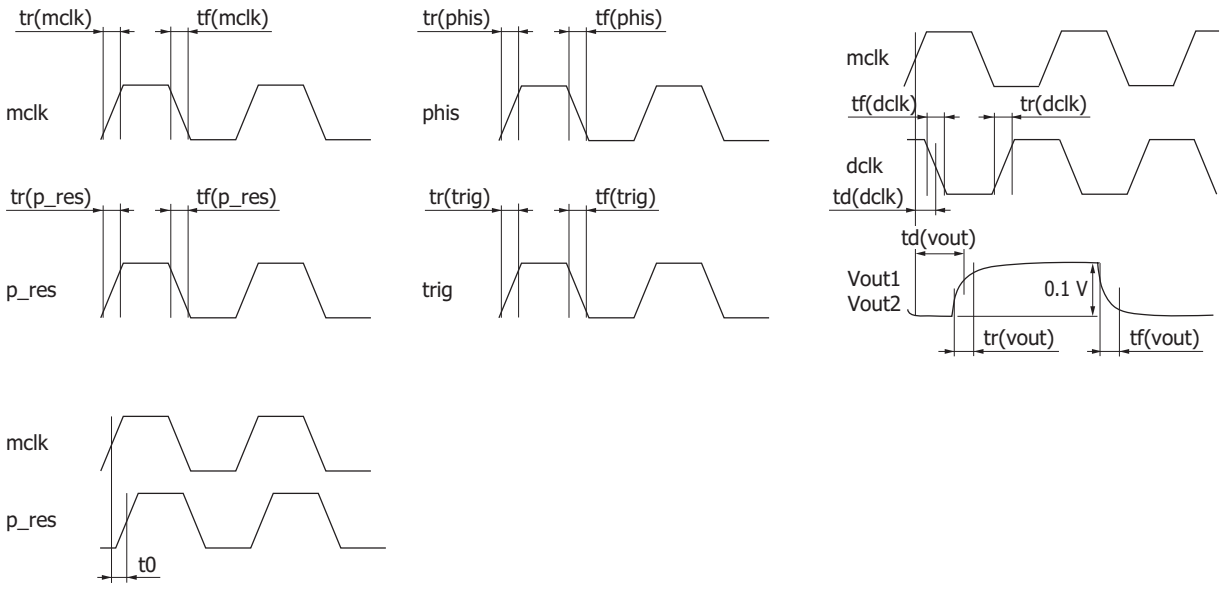


KMPDC0432EA

Calculation method of frame rate

Frame rate=1/(Time per frame)
=1/(Integration time + Readout time)

Integration time:
It is necessary to be changed by the required distance accuracy and usage environment factors such as fluctuating background light.

$$\text{Readout time}=\frac{1}{\text{Clock pulse frequency}} \times \text{Number of horizontal pixels}$$

=Time per clock (Readout time per pixel) × Number of horizontal pixels

Calculation example of readout time (clock pulse frequency: 5 MHz, number of horizontal pixels: 272)

$$\text{Readout time}=\frac{1}{5 \times 10^{6}\,[\text{Hz}]} \times 272$$

=200 [ns] × 272
=0.0544 [ms]

When operating in non-destructive readout mode:
Time per frame=Integration time + (Readout time × Non-destructive readout count)

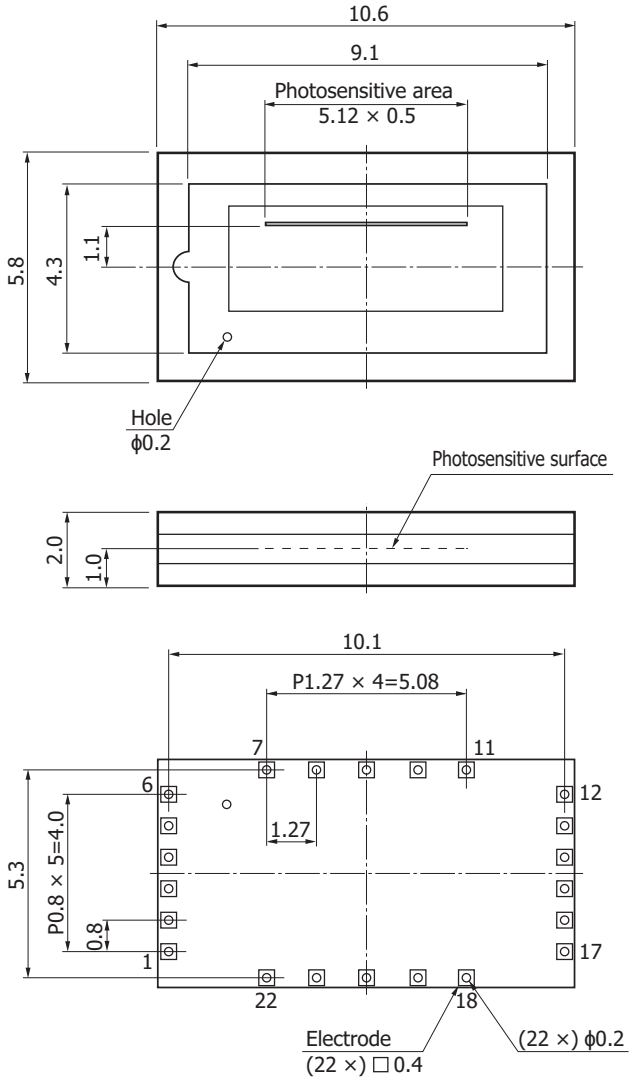
Parameter		Symbol	Min.	Typ.	Max.	Unit
Master clock pulse duty ratio		-	45	50	55	%
Master clock pulse rise and fall times		tr(mclk), tf(mclk)	0	-	20	ns
Pixel reset pulse high period		thp(p_res)	10	-	-	µs
Pixel reset pulse rise and fall times		tr(p_res), tf(p_res)	0	-	20	ns
Signal sampling pulse high period		thp(phic)	1	-	-	µs
Signal sampling pulse rise and fall times		tr(phic), tf(phic)	0	-	20	ns
Signal readout trigger pulse rise and fall times		tr(trig), tf(trig)	0	-	20	ns
Time from rising edge of master clock pulse to pixel reset pulse		t0	0	-	-	ns
Time from rising edge of pixel reset pulse to rising edge of signal sampling pulse		t1	1	-	-	µs
Time from falling edge of signal sampling pulse to rising edge of signal readout trigger pulse		t2	1.2	-	-	µs
Time from rising edge of master clock pulse to rising edge of signal readout trigger pulse		t3	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from rising edge of signal readout trigger pulse to rising edge of master clock pulse		t4	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from rising edge of master clock pulse to falling edge of signal readout trigger pulse		t5	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from falling edge of signal readout trigger pulse to rising edge of master clock pulse		t6	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from rising edge of master clock pulse (after reading signals from all pixels) to rising edge of output signal sampling pulse		t7	1/f(mclk)	-	-	s
Time from rising edge of master clock pulse (after reading signals from all pixels) to rising edge of pixel reset pulse		t8	1/f(mclk)	-	-	s
Time from rising edge of master clock pulse to falling edge of output signal synchronous pulse*6		td(dclk)	0	25	50	ns
Output signal synchronous pulse output voltage rise time (10 to 90%)*6		tr(dclk)	-	20	40	ns
Output signal synchronous pulse output voltage fall time (10 to 90%)*6		tf(dclk)	-	20	40	ns
Settling time of output signal 1, 2 (10 to 90%)*6 *7		tr(Vout), tf(Vout)	-	35	70	ns
Time from rising edge of master clock pulse to output signal 1, 2 (output 50%)*6		td(Vout)	-	40	80	ns
Charge transfer clock pulse interval		tpi(VTX)	60	-	-	ns
Charge transfer clock pulse (VTX1) high period		thp(VTX1)	30	-	-	ns
Charge transfer clock pulse (VTX1) low period		tlp(VTX1)	-	tpi(VTX) - thp(VTX2) - thp(VTX3)	-	ns
Charge transfer clock pulse (VTX2) high period		thp(VTX2)	30	-	-	ns
Charge transfer clock pulse (VTX2) low period		tlp(VTX2)	-	tpi(VTX) - thp(VTX1) - thp(VTX3)	-	ns
Charge transfer clock pulse (VTX3) high period		thp(VTX3)	0	-	-	ns
Charge transfer clock pulse (VTX3) low period		tlp(VTX3)	-	tpi(VTX) - thp(VTX1) - thp(VTX2)	-	ns
Charge transfer clock pulse voltage rise time		tr(VTX)	-	3	-	ns
Charge transfer clock pulse voltage fall time		tf(VTX)	-	3	-	ns
Charge transfer clock pulse voltage	High level	VTX1, VTX2, VTX3	-	3	-	V
	Low level		-	0	-	V
Time from rising edge of signal readout trigger pulse to start VTX operation		t9	1/f(mclk)	-	-	s
Time from finish VTX operation to rising edge of output signal synchronous pulse		t10	1/f(mclk)	-	-	s
Time from finish VTX operation to rising edge of pixel reset pulse		t11	1/f(mclk)	-	-	s

*6: C_L=3 pF
*7: Output voltage=0.1 V

Input terminal capacitance (Ta=25 °C, Vdd=5 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Charge transfer clock pulse internal load capacitance	CLTX	-	25	-	pF

Dimensional outline (unit: mm)



Tolerance unless otherwise noted: ±0.2, ±2°

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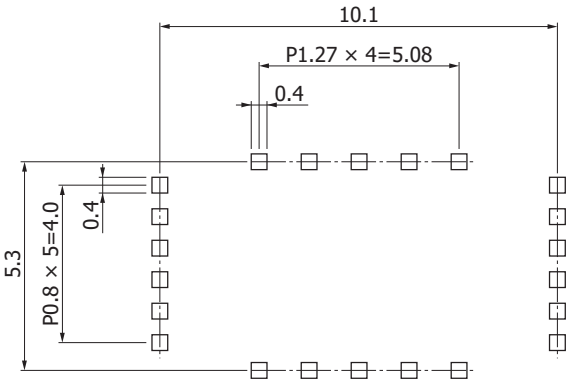
Recommended land pattern (unit: mm)



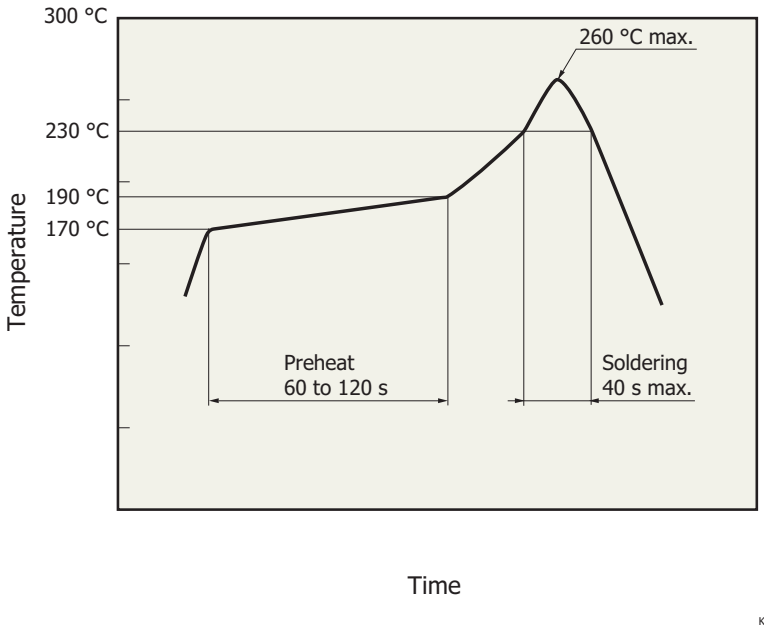
KMPDC0437EA

Pin connections

Pin no.	Symbol	I/O	Description
1	Vr	I	Bias voltage (pixel reset)
2	VTX3	I	Charge transfer clock pulse 3
3	VTX2	I	Charge transfer clock pulse 2
4	VTX1	I	Charge transfer clock pulse 1
5	p_res	I	Pixel reset pulse
6	phis	I	Signal sampling pulse
7	mclk	I	Master clock pulse
8	trig	I	Signal readout trigger pulse
9	dclk	O	Output signal synchronous pulse
10	Vdd(D)	I	Digital supply voltage
11	GND	I	Ground
12	Vout2	O	Output signal 1
13	Vout1	O	Output signal 2
14	GND	I	Ground
15	Vdd(A)	I	Analog supply voltage
16	Vpg	I	Bias voltage (photosensitive area)
17	Vsf	I	Bias voltage (pixel amplifier)
18	GND	I	Ground
19	GND	I	Ground
20	GND	I	Ground
21	GND	I	Ground
22	GND	I	Ground

Note: Connect an impedance converting buffer amplifier to Vout1/Vout2 so as to minimize the current flow.

Measured example of temperature profile with our hot-air reflow oven for product testing



- This product supports lead-free soldering. After unpacking, store it in an environment at a temperature of 30 °C or less and a humidity of 60% or less, and perform soldering within 168 hours.
- The effect that the product receives during reflow soldering varies depending on the circuit board and reflow oven that are used. Before actual reflow soldering, check for any problems by testing out the reflow soldering methods in advance.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions

· Notice
· Surface mount type products / Precautions
· Image sensors / Precautions

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HAMAMATSU PHOTONICS K.K., Solid State Division
1126-1 Ichino-cho, Higashi-ku, Hamamatsu City, 435-8558 Japan, Telephone: (81) 53-434-3311, Fax: (81) 53-434-5184
U.S.A.: Hamamatsu Corporation: 360 Foothill Road, Bridgewater, N.J. 08807, U.S.A., Telephone: (1) 908-231-0960, Fax: (1) 908-231-1218
Germany: Hamamatsu Photonics Deutschland GmbH: Arzbergerstr. 10, D-82211 Herrsching am Ammersee, Germany, Telephone: (49) 8152-375-0, Fax: (49) 8152-265-8
France: Hamamatsu Photonics France S.A.R.L.: 19, Rue du Saule Trapu, Parc du Moulin de Massy, 91882 Massy Cedex, France, Telephone: 33-(1) 69 53 71 00, Fax: 33-(1) 69 53 71 10
United Kingdom: Hamamatsu Photonics UK Limited: 2 Howard Court, 10 Tewin Road, Welwyn Garden City, Hertfordshire AL7 1BW, United Kingdom, Telephone: (44) 1707-294888, Fax: (44) 1707-325777
North Europe: Hamamatsu Photonics Norden AB: Torshamnsgatan 35 16440 Kista, Sweden, Telephone: (46) 8-509-031-00, Fax: (46) 8-509-031-01
Italy: Hamamatsu Photonics Italia S.r.l.: Strada della Moia, 1 int. 6, 20020 Arese (Milano), Italy, Telephone: (39) 02-93581733, Fax: (39) 02-93581741
China: Hamamatsu Photonics (China) Co., Ltd.: B1201, Jiaming Center, No.27 Dongsanhuan Beilu, Chaoyang District, Beijing 100020, China, Telephone: (86) 10-6586-6006, Fax: (86) 10-6586-2866

Cat. No. KMPD1140E03 Jul. 2014 DN