XpressK7

Reference Manual

Version 3.0.1 July 2014

XpressK7

Reference Manual

Document Change History

Date	Doc Version	Board Version	Change
July 2014	3.0.1	3.0.0	• Corrected PCIe clock and PCIe reset pin assignments.
June 2014	3.0.0	3.0.0	• Updated for Version 3.0 of XpressK7 board.
April 2014	1.0.2	1.0.0	• Corrected FMC description and FMC HPC pin assignments.
February 2014	1.0.1	1.0.0	• Updated FlashPROM description.
January 2014	1.0.0	1.0.0	• First release

Proprietary Notice

Table of Contents

List of Tables

List of Figures

Preface

About this Document

This document has been written for design managers, system engineers, and designers of ASICs and FPGAs who are evaluating or using the PLDA XpressK7 board. Prior knowledge of PCI Express is assumed.

Images in this document are for illustrative purposes only. They are not contractual and are subject to change.

Additional Reading

PLDA periodically updates its documentation. Please contact PLDA Technical Support or check the Web site at http://www.plda.com for current versions.

Please refer to the following documents for further information:

- *PLDA XpressK7 Getting Started Guide*: Describes how to install the XpressK7 board and how to test board functionality.
- *PLDA Linux Driver Installation Guide*: Describes how to install the Linux Driver that is used for communication between the API and the user mode application.
- *PLDA Windows Driver Installation Guide*: Describes how to install the Windows Driver that is used for communication between the API and the user mode application.
- *PLDA QuickPCIe API Reference Manual:* Describes how to use the QuickPCIe API to manage board functions.

Please refer to the following documents for information on specification standards:

- *PCI Express™ Specification, Revision 3.0*
- *PCI Express Card Electromechanical Specification, Revision 2.0*

Feedback and Contact Information

Feedback about this document

PLDA welcomes comments and suggestions about this documentation. Please contact PLDA Technical Support and provide the following information:

- the title of the document
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Chapter 1 Introduction

1.1 Purpose of the Board

The XpressK7 board is designed to enable all engineers, even those with little PCI Express experience, to design complex applications using PCIe as their main communication interface.

XpressV7-LP is a standard-profile (111.15 x 167.65mm), PCI Express FPGA board with partial HPC FMC and a SODIMM DDR3 connector, engineered for both prototyping and field deployment.

The board is based on the Xilinx Kintex-7 FPGA in the FBGA 676 package and can be mounted with the XC7K160-2FBG676C device, the XC7K325-2FBG676C device or the XC7K325-2FFG676C device. Contact sales@plda.com for more information.

1.2 Features List

- PCI Express X4 2.5/5.0/8.0 Gbps (Gen1, 2 or 3):
  - PCI Express edge connector
  - **Note**: PCI Express Gen3 is only available when the XpressK7 is mounted with an FFG device.
- Kintex7 FPGA default packages are:
  - XC7K160-2FBG676C
  - XC7K325-2FBG676C
  - XC7K325-2FFG676C (Gen3 capable)
- Partial HPC FMC interface providing:
  - 4 Gigabit Transceivers (vs 8 for full VITA57.1 FMC HPC)
  - 80 LVDS pairs (70 pairs + 10 single-ended signals compatible with VITA57.1 FMC HPC)
  - 4 LVDS clock signals
  - an LPC FMC that is fully-compliant with VITA57.1 specification
- DDR3 SDRAM SODIMM supporting:
  - up to 4GB SODIMM module
  - up to 533MHz
- Board module configuration:
  - BPI mode
  - 1Gb Numonyx FlashPROM
  - Configurable via JTAG
  - up to 4 boot sectors
  - configuration push button
- General IOs:
  - 4 on-board CMS LEDs
  - one tricolor dual LED (on bracket)
  - 4 user switches
  - reset push button
- Clock circuitry:
  - 50MHz (SE/Protocore, config clock)
  - 100MHz (HSCL/PCIe)
  - 200MHz (LVDS/DDR3)
- Power Supply:
  - 12V from PCIe slot
  - 12V From a Jack connector (stand-alone mode)
  - On/Off power switch
  - 3V Encryption battery

A detailed description of board features can be found in Section 2.3.

1.3 System Requirements

To use XpressK7 board features, you must install the **PLDA Software Tools**. The PLDA Software Tools can be downloaded from PLDA's extranet site. You can log in to the extranet from PLDA's web site www.plda.com.

1.4 Board Configuration Requirements

- Xilinx Platform USB cable
- Vivado 2014.1 or later

Chapter 2 XpressK7 Architecture

2.1 XpressK7 Layout

The following figure shows the component side of the XpressK7 board:

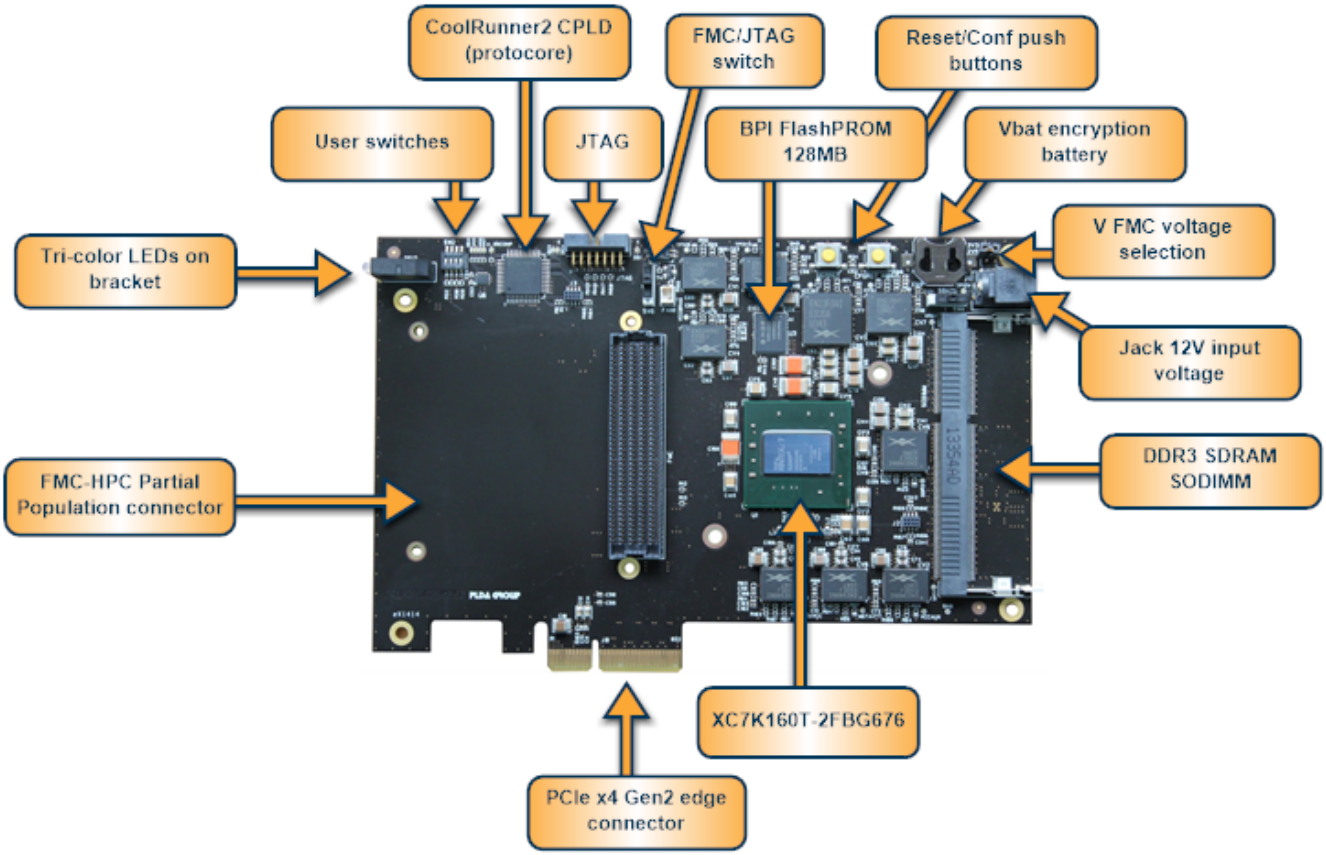

Figure 1: XpressK7 layout

2.2 Block Diagram of the Board

The XpressK7 board is based on a Xilinx Kintex-7 FPGA, as shown below:

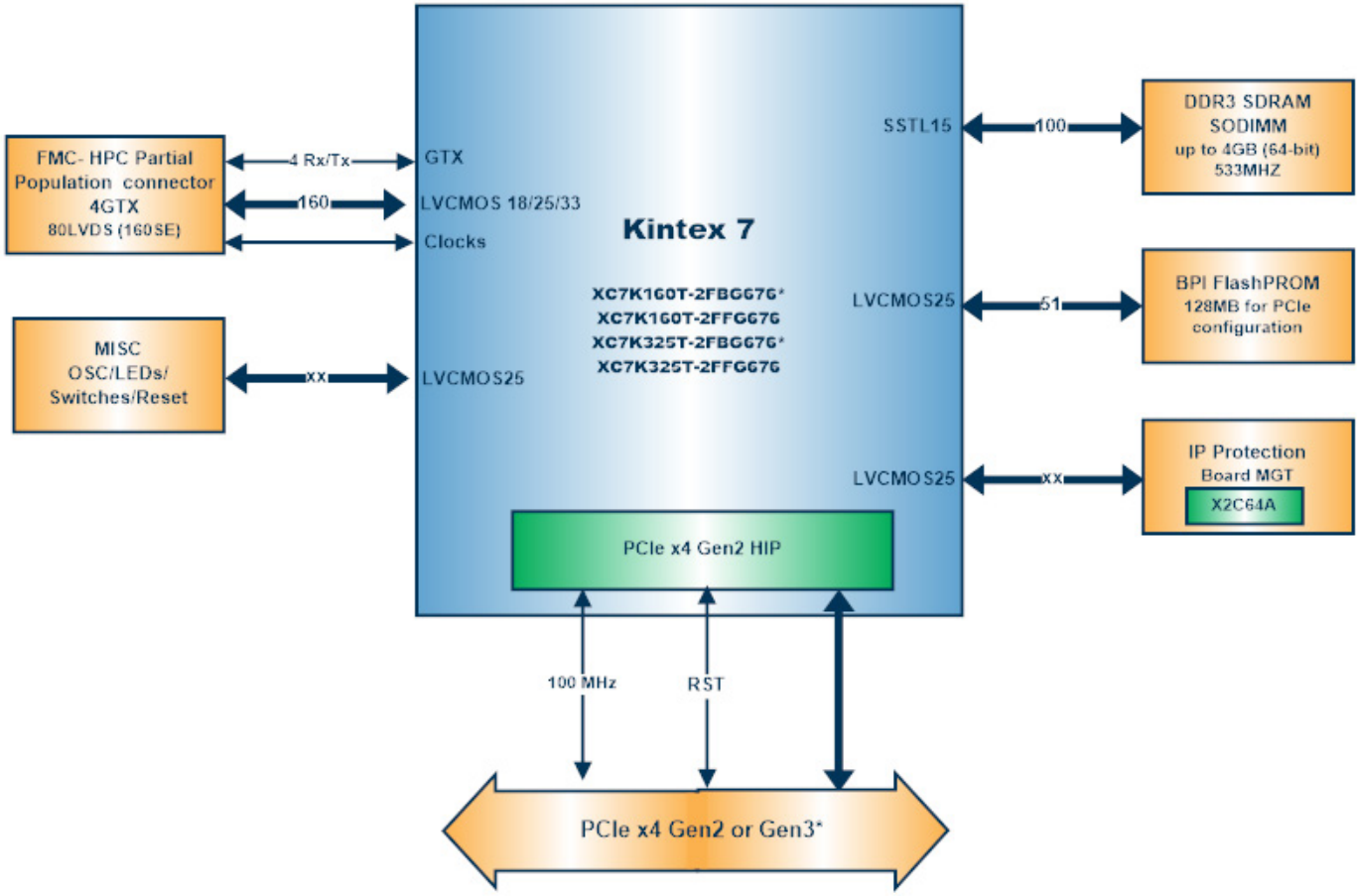

Figure 2: XpressK7 block diagram

2.3 Board Features

The following table describes XpressK7 board features:

Feature	Description	For more information, see...
x4 PCI Express 2.0 edge connector	This connector supports PCI Express Gen3 (8.0 Gbps), Gen2 (5.0 Gbps), and Gen1 (2.5 Gbps) in x4, x2 and x1 Hard IP mode. **Note**: PCI Express Gen3 is only available when the XpressK7 is mounted with an FFG device.	Section 3.4
FMC-HPC (Partial Population) connector interface	The FMC-HPC (Partial Population) connector interface features: • four Gigabit transceivers (a full VITA57.1 FMC HPC has eight) • 80 LVDS pairs (70 pairs + 10 single-ended signals compatible with VITA57.1 FMC HPC) • four LVDS clock signals • an LPC (low pin count) FMC that is fully-compliant with VITA57.1 specification	Section 3.6
DDR3 SDRAM SODIMM	The DDR3 SDRAM SODIMM connector supports • up to 4GB SODIMM modules • a clock frequency of 533MHz	Section 3.5
Board configuration module	A 16-bit BPI configuration module (50 MHz) is available to configure the FPGA at each board boot-up. This module is made of a 1Gb Numonyx Flash device (PC28F00AP30BF) connected to the Kintex-7 BPI interface. Flash devices can be programmed using a JTAG connector. Up to 4 boot sectors can be selected using two microswitches. A configuration reset push button is available to reload the FPGA.	Section 3.2
JTAG connector	A JTAG connector enables FPGA configuration using a XilinX HW-USB blaster and the Xilinx Vivado 2014.1 tool.	
Miscellaneous features	• four on-board SMD LEDs • one tricolor dual LED (on the bracket) • four user switches, • one reset push button • one CoolRunner2 CPLD (protocore)	Section 3.7 - Section 3.10
Power supply	The XpressK7 is supplied with 12V power either from: • the PCIe Slot, or • a 2.1mm Jack connector, when used in stand-alone mode (AC/DC converter is not provided). This featured must NOT be used when the XpressK7 is plugged into a PCIe slot An On/Off power switch enables you to switch the board on or off.	--
VBAT	An encryption battery slot is available on board	--

Table 1: Board features description

2.4 Mechanical Description

The following diagram illustrates the mechanical architecture of the XpressK7 board without the heatsink or daughter card mounted.

Note: The overall height of the board, that is, the height of the highest component, is 11.2mm.

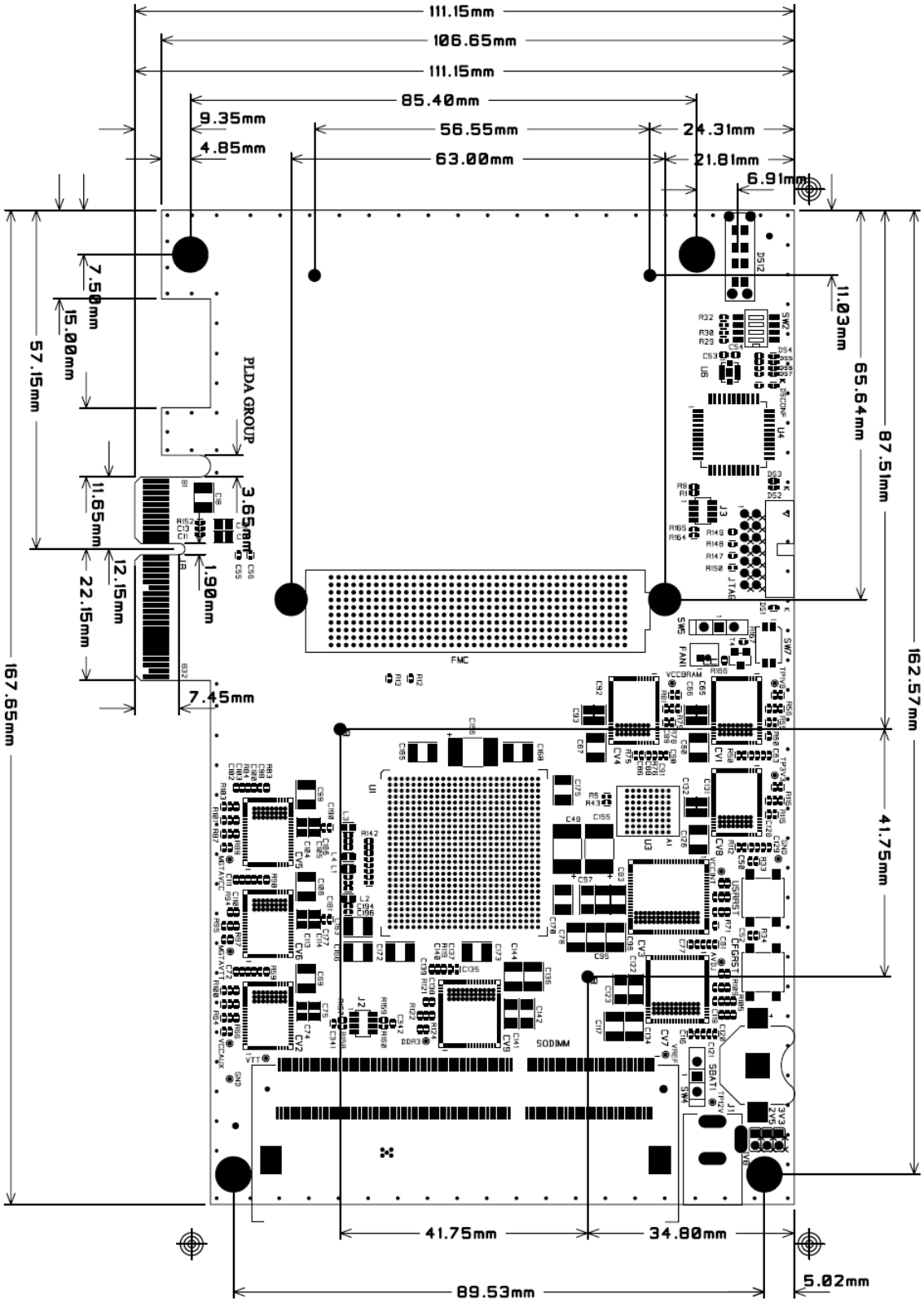

Figure 3: XpressK7 component side without daughter card

Chapter 3 XpressK7 Features

3.1 Kintex-7 FPGA Device

The board is based on the Xilinx Kintex-7 FPGA in the FBGA 676 package and can be mounted with the XC7K160-2FBG676C device, the XC7K325-2FBG676C device or the XC7K325-2FFG676C device. Contact sales@plda.com for more information.

The following table shows the resources of each device:

FPGA	Logic Cells	CLB Flip Flop	Total Block RAM	DSP48 Slices
XC7K160	162240	202800	11700 Kbit	600
XC7K325	326080	407600	16020 Kbit	840

Table 2: Kintex-7 FPGA Resources

3.2 Board Configuration Module

The XpressK7 uses the Kintex-7 integrated BPI configuration module. Each time the board is booted, the FPGA is reloaded with one of the configurations on the FlashPROM; this requires no external component.

The Configuration Module consists of a single 1Gb 16-bit wide Numonyx FlashPROM (PC28F00AP30BF), which is directly connected to the Kintex-7 BPI-configuration dedicated pins. This enables the FlashPROM to be configured via the Xilinx USB-Blaster using the Vivado 2014.1 tool.

Two switches are available to select up to 4 boot sectors. A reset push button is available to reload the FPGA.

The following figure shows the configuration components of the XpressK7:

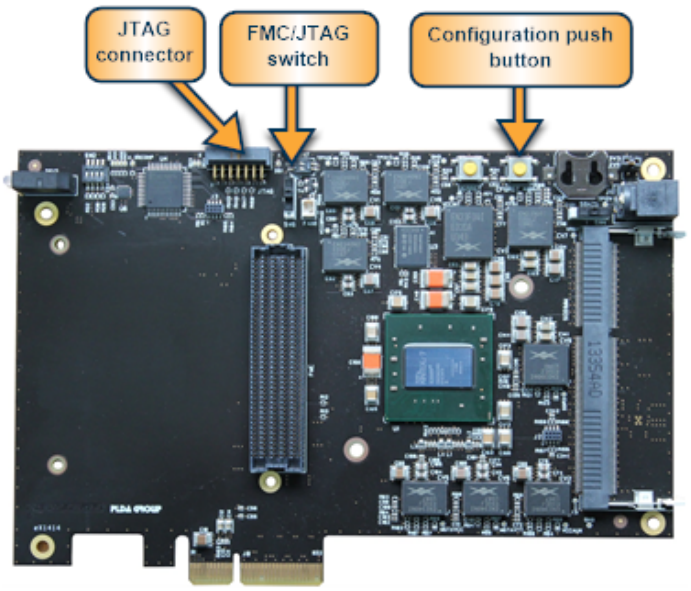

Figure 4: Board configuration components

Note: If no FMC card is mounted or, if there is no FPGA on the mounted FMC card, the SW5 switch (FMC JTAG Switch) must be in the closed position as shown in the image above.

The following table shows pin assignments for the FlashPROMs on the FPGA:

Signal name	FGPA Pin	Signal name	FGPA Pin
flash_ad00	J23	flash_adv#	D20
flash_ad01	K23	flash_ce#	C23
flash_ad02	K22	flash_clk	C8
flash_ad03	L22	flash_data00	B24
flash_ad04	J25	flash_data01	A25
flash_ad05	J24	flash_data02	B22
flash_ad06	H22	flash_data03	A22
flash_ad07	H24	flash_data04	A23
flash_ad08	H23	flash_data05	A24
flash_ad09	G21	flash_data06	D26
flash_ad10	H21	flash_data07	C26
flash_ad11	H26	flash_data08	C24
flash_ad12	J26	flash_data09	D21
flash_ad13	E26	flash_data10	C22
flash_ad14	F25	flash_data11	B20
flash_ad15	G26	flash_data12	A20
flash_ad16	K17	flash_data13	E22
flash_ad17	K16	flash_data14	C21
flash_ad18	L20	flash_data15	B21
flash_ad19	J19	flash_oe#	M17
flash_ad20	J18	flash_rst#	G7
flash_ad21	J20	flash_wait	E25
flash_ad22	K20	flash_we#	L18
flash_ad23	G20	--	--
flash_ad24	H19	50MHz_emcclk	B26
flash_ad25	E20	Prog_b (conf_reset)	P6
flash_ad25 (RS0)	K18	--	--
flash_ad26	F19	flash_boot_sector	AD26
flash_ad26 (RS1)	L17	flash_reload	AE26

Table 3: FlashPROM pin assignments on the FPGA

Note: The signals `FLASH_BOOT_SECTOR` and `FLASH_RELOAD` are reserved for future use.

3.3 Dedicated Clocks

The following table describes clock assignments for the board:

Signal	FPGA Pin	Type	Comment
50MHz_emcclk	B26	LVCMOS25	50MHz clock for BPI configuration
50MHz_fpga	AB11	LVCMOS25	50MHz clock for user purposes
gbtclk0_m2c_p/n	H6/H5	LVDS	FMC LPC transceiver Ref_clock
osc1_100MHz_p/n	K6/K5	LVDS	FMC transceiver 100MHz (not connected)
clk0_c2m_p/n	N21/N22	LVDS	FMC LPC card to mezzanine clock
clk0_m2c_p /n	R21/P21	LVDS	FMC LPC mezzanine to card clock
clk1_c2m_p/n	Y22/AA22	LVDS	FMC HPC card to mezzanine clock
clk1_m2c_p/n	Y23/AA24	LVDS	FMC HPC mezzanine to card clock
PCIe_CLKp/n	D6/D5	HCSL	PCIe Reference clock
osc2_100MHz_p/n	F6/F5	LVDS	100MHz Stand-alone reference clock
osc3_200MHz_p/n	AA10/AB10	LVDS	200MHz Reference clock

Table 4: XpressK7 clock assignments

3.4 PCI Express Endpoint Connector

The PCI Express male connector enables access to Endpoint PCI Express components as x1 or x4 PCI Express 2.0 or 3.0 links.

The connector supports PCI Express Gen2 and Gen1 in x4, x2 & x1 Hard IP mode.

x4 Gen3 is supported with a PLDA soft IP and a board mounted with the XC7K160-2FFG676 (or 325/410) device.

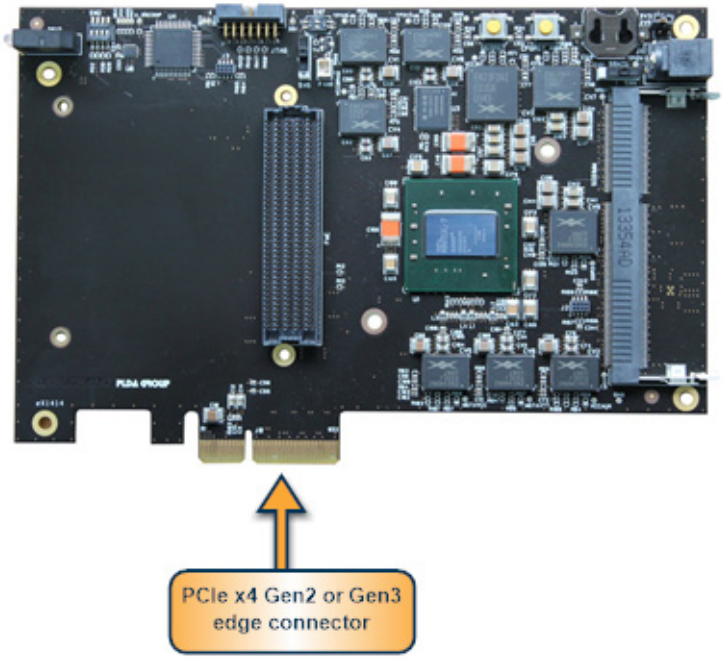

Figure 5: PCI Express connector

The table below describes pin assignments for the PCI Express Endpoint connector. Shaded signals are defined as optional by the *PCI Express Card Electromechanical Specification 2.0*, and signals that appear bold are active signals implemented on the XpressK7.

Side B			Side A		
PCI Express Pin	**FPGA Pin**	**Signal**	**PCI Express Pin**	**FPGA Pin**	**Signal**
1	--	+12V	1	connected to mPRSNT#2	mPRSNT1#
2	--	+12V	2	--	+12V
3	--	+12V	3	--	+12V
4	--	GND	4	--	GND
5	--	Sm_clk	5	nc	JTAG2
6	--	Sm_dat	6	nc	JTAG3
7	--	GND	7	nc	JTAG4
8	--	+3.3V	8	nc	JTAG5
9	nc	JTAG1	9	--	+3.3V
10	nc	3.3Vaux	10	--	+3.3V
11	nc	mWAKE#	11	U16	**mPERST#**

Table 5: Pin assignments for the PCI Express endpoint connector

Side B			Side A		
PCI Express Pin	FPGA Pin	Signal	PCI Express Pin	FPGA Pin	Signal
--	--	--	--	--	--
12	--	RSVD	12	--	GND
13	--	GND	13	H6	**PCIe_CLKp**
14	B6	**mPER0_p**	14	H5	**PCIe_CLKn**
15	B5	**mPER0_n**	15	--	GND
16	--	GND	16	A4	**mPET0_p**
17	connected to mPRSNT#1	mPRSNT2#	17	A3	**mPET0_n**
18	--	GND	18	--	GND
19	C4	**mPER1_p**	19	--	RSVD
20	C3	**mPER1_n**	20	--	GND
21	--	GND	21	B2	**mPET1_p**
22	--	GND	22	B1	**mPET1_n**
23	E4	**mPER2_p**	23	--	GND
24	E3	**mPER2_n**	24	--	GND
25	--	GND	25	D2	**mPET2_p**
26	--	GND	26	D1	**mPET2_n**
27	G4	**mPER3_p**	27	--	GND
28	G3	**mPER3_n**	28	--	GND
29	--	GND	29	F2	**mPET3_p**
30	--	RSVD	30	F1	**mPET3_n**
31	connected to mPRSNT#1	mPRSNT#2	31	--	GND
32	--	GND	32	--	RSVD

Table 5: Pin assignments for the PCI Express endpoint connector

3.5 DDR3 SDRAM SODIMM Connector

The XpressK7 features a DDR3 SODIMM connector that enables you to use DDR3 modules up to 4GB with a maximum frequency of 533MHz:

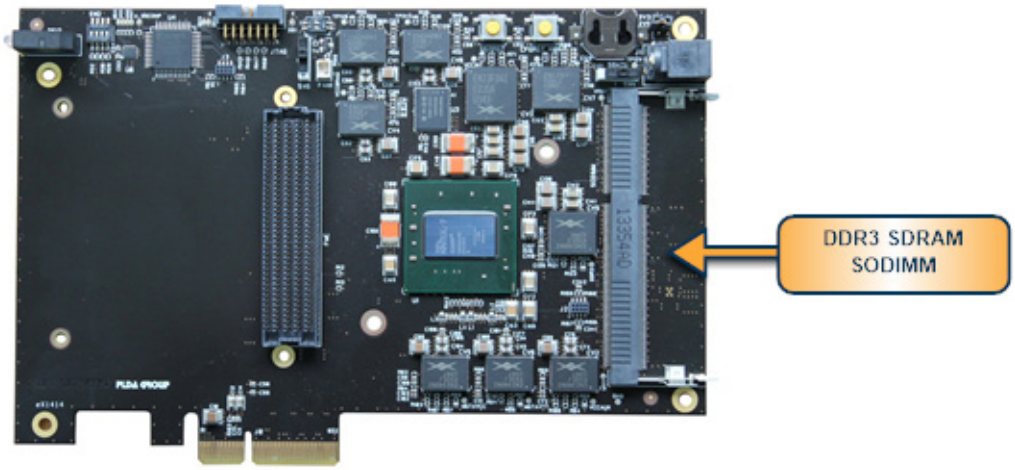

Figure 6: DDR3L SDRAM

Note: PLDA supports the memory stick MT8KTH51264HZ-1G6E1 for use with the DDR3 SODIMM connector and can provide it with the XpressK7. Please contact PLDA Sales for shipment details.

The following table shows pin assignments for the DDR3L SDRAM SODIMM:

FPGA Pin	Signal	FPGA Pin	Signal
ddr3_a00	AC7	ddr3_d00	V17
ddr3_a01	AE7	ddr3_d01	V19
ddr3_a02	AF7	ddr3_d02	V16
ddr3_a03	AD9	ddr3_d03	Y17
ddr3_a04	AD8	ddr3_d04	W16
ddr3_a05	AB9	ddr3_d05	W15
ddr3_a06	AF8	ddr3_d06	W14
ddr3_a07	AE8	ddr3_d07	V14
ddr3_a08	AA9	ddr3_d08	AA19
ddr3_a09	AE10	ddr3_d09	AA20
ddr3_a10	AB7	ddr3_d10	AD19
ddr3_a11	AC9	ddr3_d11	AD18
ddr3_a12	AF10	ddr3_d12	AB20
ddr3_a13	AA7	ddr3_d13	AC19
ddr3_a14	AD10	ddr3_d14	AC17
ddr3_a15	AF9	ddr3_d15	AB17
ddr3_ba0	AB12	ddr3_d16	AA17

Table 6: DDR3L SDRAM pin assignments

FPGA Pin	Signal	FPGA Pin	Signal
ddr3_ba1	AC12	ddr3_d17	AA18
ddr3_ba2	AD13	ddr3_d18	AC14
ddr3_cas#	Y12	ddr3_d19	AB15
ddr3_cke0	AA12	ddr3_d20	AB16
ddr3_cke1	AC13	ddr3_d21	AC16
ddr3_clk0_n	AF13	ddr3_d22	AB14
ddr3_clk0_p	AE13	ddr3_d23	AA14
ddr3_clk1_n	AF12	ddr3_d24	AF20
ddr3_clk1_p	AE12	ddr3_d25	AE17
ddr3_cs0#	AD11	ddr3_d26	AF17
ddr3_cs1#	Y11	ddr3_d27	AD16
ddr3_dm0	V18	ddr3_d28	AF15
ddr3_dm1	AC18	ddr3_d29	AE15
ddr3_dm2	AD14	ddr3_d30	AD15
ddr3_dm3	AF19	ddr3_d31	AF14
ddr3_dm4	AE2	ddr3_d32	AE6
ddr3_dm5	AC4	ddr3_d33	AE5
ddr3_dm6	Y2	ddr3_d34	AE3
ddr3_dm7	U5	ddr3_d35	AF2
ddr3_dqs0_n	W19	ddr3_d36	AD4
ddr3_dqs0_p	W18	ddr3_d37	AF3
ddr3_dqs1_n	AE20	ddr3_d38	AD1
ddr3_dqs1_p	AD20	ddr3_d39	AE1
ddr3_dqs2_n	Y16	ddr3_d40	AD6
ddr3_dqs2_p	Y15	ddr3_d41	Y6
ddr3_dqs3_n	AF18	ddr3_d42	Y5
ddr3_dqs3_p	AE18	ddr3_d43	AA4
ddr3_dqs4_n	AF4	ddr3_d44	AB6
ddr3_dqs4_p	AF5	ddr3_d45	AC6
ddr3_dqs5_n	AB5	ddr3_d46	AB4
ddr3_dqs5_p	AA5	ddr3_d47	AC3
ddr3_dqs6_n	AC1	ddr3_d48	AC2
ddr3_dqs6_p	AB1	ddr3_d49	AA2
ddr3_dqs7_n	W5	ddr3_d50	Y3
ddr3_dqs7_p	W6	ddr3_d51	Y1

Table 6: DDR3L SDRAM pin assignments

FPGA Pin	Signal	FPGA Pin	Signal
ddr3_odt0	AC8	ddr3_d52	AA3
ddr3_odt1	AA8	ddr3_d53	AB2
ddr3_ras#	AE11	ddr3_d54	V1
ddr3_reset#	AA13	ddr3_d55	W1
ddr3_we#	AC11	ddr3_d56	V3
--	--	ddr3_d57	W3
--	--	ddr3_d58	U1
--	--	ddr3_d59	U2
--	--	ddr3_d60	U7
--	--	ddr3_d61	V6
osc3_200MHz_n	AB10	ddr3_d62	U6
osc3_200MHz_p	AA10	ddr3_d63	V4

Table 6: DDR3L SDRAM pin assignments

3.6 FMC-HPC Connector

The FMC-HPC (Partial Population) connector features:

- four Rx/Tx transceivers from the FPGA (the standard HPC FMC features eight transceivers)
- one clock input (LVDS) transceiver
- 80 LVDS pairs (available as 160 LVCMOS 18/25/33 single-ended signals)
- four LVDS clock signals
- JTAG configuration signals
- +12V/+3.3V/Vadj (1.8V / 2.5V) power supplies

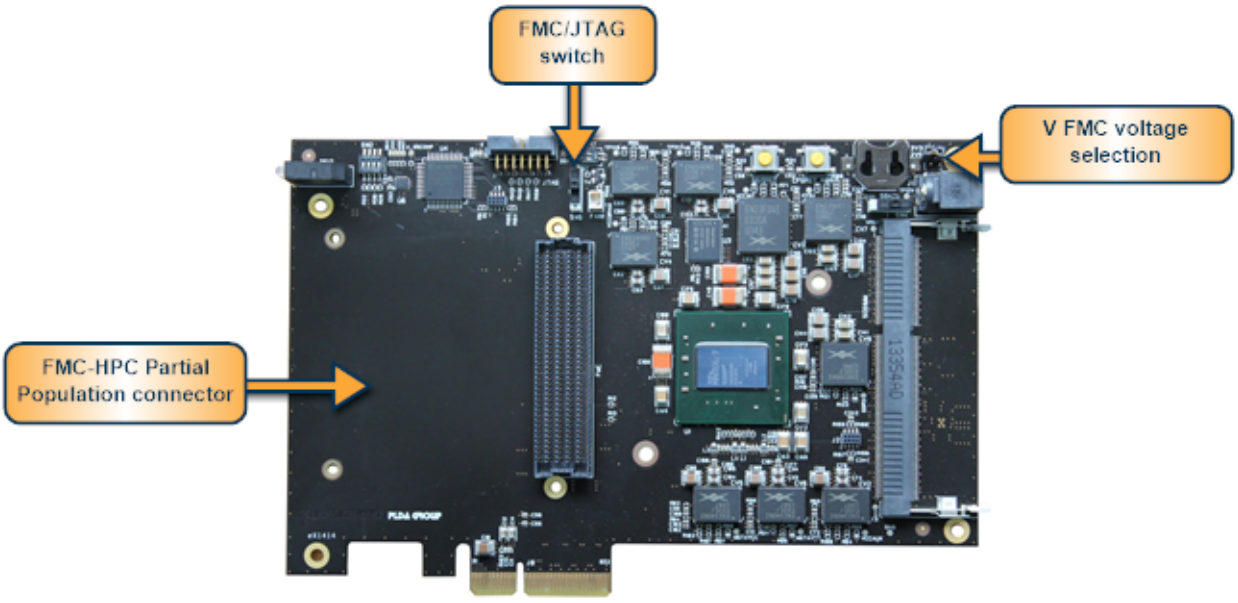

Figure 7: FMC-HPC Partial Population connector

The XpressK7 FMC connector conforms to ANSI VITA57 mechanical requirements, so any FMC mezzanine card can be mounted on the XpressK7 and integrated into a regular computer.

3.6.1 FMC Connector Pins

Low Pin Count FMC		High Pin Count FMC Bank A		High Pin Count FMC Bank B	
Signal Name	FPGA Pin	Signal Name	FPGA Pin	Signal Name	FPGA Pin
la00_cc_n	R23	ha00_cc_n	AB24	hb00_cc_n	H18
la00_cc_p	R22	ha00_cc_p	AA23	hb00_cc_p	H17
la01_cc_n	N23	ha01_cc_n	AC24	hb01_n	A19
la01_cc_p	P23	ha01_cc_p	AC23	hb01_p	A18
la02_n	AC26	ha02_n	P26	hb02_n	R17
la02_p	AB26	ha02_p	R26	hb02_p	R16
la03_n	M26	ha03_n	AD24	hb03_n	T17
la03_p	N26	ha03_p	AD23	hb03_p	U17
la04_n	W26	ha04_n	AC22	hb04_n	G16
la04_p	W25	ha04_p	AB22	hb04_p	H16
la05_n	L24	ha05_n	AC21	hb05_n	E16
la05_p	M24	ha05_p	AB21	hb05_p	E15
la06_n	Y21	ha06_n	L25	hb06_cc_n	C11
la06_p	W20	ha06_p	M25	hb06_cc_p	C12
la07_n	V24	ha07_n	AB25	hb07_n	J16
la07_p	V23	ha07_p	AA25	hb07_p	J15
la08_n	K26	ha08_n	W24	hb08_n	F15
la08_p	K25	ha08_p	W23	hb08_p	G15
la09_n	F23	ha09_n	Y26	hb09_n	A14
la09_p	G22	ha09_p	Y25	hb09_p	B14
la10_n	V22	ha10_n	F24	hb10_n	D10
la10_p	U22	ha10_p	G24	hb10_p	E10
la11_n	T25	ha11_n	V26	hb11_n	C13
la11_p	T24	ha11_p	U26	hb11_p	C14
la12_n	D24	ha12_n	U25	hb12_n	F13
la12_p	D23	ha12_p	U24	hb12_p	F14
la13_n	R20	ha13_n	W21	hb13_n	G14
la13_p	T20	ha13_p	V21	hb13_p	H14
la14_n	T19	ha14_n	M22	hb14_n	A12
la14_p	T18	ha14_p	M21	hb14_p	A13
la15_n	P18	ha15_n	U20	hb15_n	B9
la15_p	R18	ha15_p	U19	hb15_p	C9

Table 7: FMC Connector pin assignments

Low Pin Count FMC		High Pin Count FMC Bank A		High Pin Count FMC Bank B	
Signal Name	FPGA Pin	Signal Name	FPGA Pin	Signal Name	FPGA Pin
la16_n	M20	ha16_n	P25	hb16_n	J10
la16_p	N19	ha16_p	R25	hb16_p	J11
la17_cc_n	D18	ha17_cc_n	E23	hb17_cc_n	F10
la17_cc_p	E18	ha17_cc_p	F22	hb17_cc_p	G11
la18_cc_n	E17	ha18_n	N24	hb18_n	H8
la18_cc_p	F17	ha18_p	P24	hb18_p	H9
la19_n	A17	ha19_n	N17	hb19_n	B11
la19_p	B17	ha19_p	P16	hb19_p	B12
la20_n	M19	ha20_n	T23	hb20_n	A10
la20_p	N18	ha20_p	T22	hb20_p	B10
la21_n	D16	ha21_n	P20	hb21_n	G9
la21_p	D15	ha21_p	P19	hb21_p	G10
la22_n	C18	ha22_n	B16	--	--
la22_p	C17	ha22_p	C16	--	--
la23_n	F18	ha23_n	B19	--	--
la23_p	G17	ha23_p	C19	--	--
la24_n	D13	--	--	--	--
la24_p	D14	dp1_c2m_n	K1	--	--
la25_n	E12	dp1_c2m_p	K2	--	--
la25_p	E13	dp1_m2c_n	L3	--	--
la26_n	H13	dp1_m2c_p	L4	--	--
la26_p	J13	dp2_c2m_n	M1	--	--
la27_n	A15	dp2_c2m_p	M2	--	--
la27_p	B15	dp2_m2c_n	N3	--	--
la28_n	F12	dp2_m2c_p	N4	--	--
la28_p	G12	dp3_c2m_n	P1	--	--
la29_n	D11	dp3_c2m_p	P2	--	--
la29_p	E11	dp3_m2c_n	R3	--	--
la30_n	H11	dp3_m2c_p	R4	--	--
la30_p	H12	--	--	--	--
la31_n	A8	clk1_c2m_n	AA22	--	--
la31_p	A9	clk1_c2m_p	Y22	--	--
la32_n	F8	clk1_m2c_n	AA24	--	--
la32_p	F9	clk1_m2c_p	Y23	--	--

Table 7: FMC Connector pin assignments

Low Pin Count FMC		High Pin Count FMC Bank A		High Pin Count FMC Bank B	
Signal Name	FPGA Pin	Signal Name	FPGA Pin	Signal Name	FPGA Pin
la33_n	D8	--	--	--	--
la33_p	D9	pg_m2c	U21	--	--
gbtclk0_m2c_n	H5	--	--	--	--
gbtclk0_m2c_p	H6	--	--	--	--
dp0_c2m_n	H1	--	--	--	--
dp0_c2m_p	H2	--	--	--	--
dp0_m2c_n	J3	--	--	--	--
dp0_m2c_p	J4	--	--	--	--
clk0_c2m_n	N22	--	--	--	--
clk0_c2m_p	N21	--	--	--	--
clk0_m2c_n	P21	--	--	--	--
clk0_m2c_p	R21	--	--	--	--

Table 7: FMC Connector pin assignments

Note:

- White cells show FMC LPC or HPC-compliant signals.
- Orange cells show FMC HPC-compliant signals with naming mismatch with VITA57.1 specification.
- Red cells show non-FMC compliant signals; these signals should ONLY be used if your daughter card is for use with the XpressK7. Daughter cards that use these 10 signals must not be used on a full HPC FMC carrier board. If not used, the 10 GND in the red cells should not be routed on the daughter card FMC connector.

- You must verify that every FMC signal used on your FMC daughter card is present on the XpressK7.

3.6.2 FMC-HPC Connector

An FMC (FPGA Mezzanine Card) is an ANSI/VITA standard that defines I/O mezzanine modules with a connection to an FPGA or other device with reconfigurable I/O capability.

The FMC mezzanine module uses a high-pin count 400 pin high-speed array connector. The following table shows the pin assignments on the FMC-HPC connector:

	K		J		H		G		F	
1	+VREF	VFMC / 2	GND		+VREF	VFMC / 2	GND		pg_m2c	U21
2	GND		clk1_c2m_p	Y22	UnCnnctd		clk0_c2m_p	N21	GND	
3	GND		clk1_c2m_n	AA22	GND		clk0_c2m_n	N22	GND	
4	clk1_m2c_p	Y23	GND		clk0_m2c_p	R21	GND		ha00_cc_p	AA23
5	clk1_m2c_n	AA24	GND		clk0_m2c_n	P21	GND		ha00_cc_n	AB24
6	GND		ha03_p	AD23	GND		la00_cc_p	R22	GND	
7	ha02_p	R26	ha03_n	AD24	la02_p	AB26	la00_cc_n	R23	ha04_p	AB22
8	ha02_n	P26	GND		la02_n	AC26	GND		ha04_n	AC22
9	GND		GND		GND		la03_p	N26	GND	
10	ha06_p	M25	ha07_p	AA25	la04_p	W25	la03_n	M26	ha08_p	W23
11	ha06_n	L25	ha07_n	AB25	la04_n	W26	GND		ha08_n	W24
12	GND		GND		GND		la08_p	K25	GND	
13	ha10_p	G24	ha11_p	U26	la07_p	V23	la08_n	K26	ha12_p	U24
14	ha10_n	F24	ha11_n	V26	la07_n	V24	GND		ha12_n	U25
15	GND		GND		GND		la12_p	D23	GND	
16	ha17_cc_p	F22	ha14_p	M21	la11_p	T24	la12_n	D24	ha15_p	U19
17	ha17_cc_n	E23	ha14_n	M22	la11_n	T25	GND		ha15_n	U20
18	GND		GND		GND		la16_p	N19	GND	
19	ha21_p	P19	ha18_p	P24	la15_p	R18	la16_n	M20	ha19_p	P16
20	ha21_n	P20	ha18_n	N24	la15_n	P18	GND		ha19_n	N17
21	GND		GND		GND		la20_p	N18	GND	
22	ha23_p	C19	ha22_p	C16	la19_p	B17	la20_n	M19	hb02_p	R16
23	ha23_n	B19	ha22_n	B16	la19_n	A17	GND		hb02_n	R17
24	GND		GND		GND		la22_p	C17	GND	
25	hb00_cc_p	H17	hb01_p	A18	la21_p	D15	la22_n	C18	hb04_p	H16
26	hb00_cc_n	H18	hb01_n	A19	la21_n	D16	GND		hb04_n	G16
27	GND		GND		GND		la25_p	E13	GND	
28	hb06_cc_p	C12	hb07_p	J15	la24_p	D14	la25_n	E12	hb08_p	G15
29	hb06_cc_n	C11	hb07_n	J16	la24_n	D13	GND		hb08_n	F15
30	GND		GND		GND		la29_p	E11	GND	
31	hb10_p	E10	hb11_p	C14	la28_p	G12	la29_n	D11	hb12_p	F14
32	hb10_n	D10	hb11_n	C13	la28_n	F12	GND		hb12_n	F13
33	GND		GND		GND		la31_p	A9	GND	
34	hb14_p	A13	hb15_p	C9	la30_p	H12	la31_n	A8	hb16_p	J11
35	hb14_n	A12	hb15_n	B9	la30_n	H11	GND		hb16_n	J10
36	GND		GND		GND		la33_p	D9	GND	
37	hb17_cc_p	G11	hb18_p	H9	la32_p	F9	la33_n	D8	hb20_p	B10
38	hb17_cc_n	F10	hb18_n	H8	la32_n	F8	GND		hb20_n	A10
39	GND		UnCnnctd		GND		+VADJ	VFMC	GND	
40	UnCnnctd		GND		+VADJ	VFMC	GND		+VADJ	VFMC

E		D		C		B		A	
		pg_c2m	LED DS1	GND		UnCnnctd		GND	
ha01_cc_p	AC23	GND		dp0_c2m_p	H2	GND		dp1_m2c_p	L4
ha01_cc_n	AC24	GND		dp0_c2m_n	H1	GND		dp1_m2c_n	L3
GND		gbtclk0_m2c_p	H6	GND		UnCnnctd		GND	
GND		gbtclk0_m2c_n	H5	GND		UnCnnctd		GND	
ha05_p	AB21	GND		dp0_m2c_p	J4	GND		dp2_m2c_p	N4
ha05_n	AC21	GND		dp0_m2c_n	J3	GND		dp2_m2c_n	N3
GND		la01_cc_p	P23	GND		UnCnnctd		GND	
ha09_p	Y25	la01_cc_n	N23	GND		UnCnnctd		GND	
ha09_n	Y26	GND		la06_p	W20	GND		dp3_m2c_p	R4
GND		la05_p	M24	la06_n	Y21	GND		dp3_m2c_n	R3
ha13_p	V21	la05_n	L24	GND		UnCnnctd		GND	
ha13_n	W21	GND		GND		UnCnnctd		GND	
GND		la09_p	G22	la10_p	U22	GND		UnCnnctd	
ha16_p	R25	la09_n	F23	la10_n	V22	GND		UnCnnctd	
ha16_n	P25	GND		GND		UnCnnctd		GND	
GND		la13_p	T20	GND		UnCnnctd		GND	
ha20_p	T22	la13_n	R20	la14_p	T18	GND		UnCnnctd	
ha20_n	T23	GND		la14_n	T19	GND		UnCnnctd	
GND		la17_cc_p	E18	GND		UnCnnctd		GND	
hb03_p	U17	la17_cc_n	D18	GND		UnCnnctd		GND	
hb03_n	T17	GND		la18_cc_p	F17	GND		dp1_c2m_p	K2
GND		la23_p	G17	la18_cc_n	E17	GND		dp1_c2m_n	K1
hb05_p	E15	la23_n	F18	GND		UnCnnctd		GND	
hb05_n	E16	GND		GND		UnCnnctd		GND	
GND		la26_p	J13	la27_p	B15	GND		dp2_c2m_p	M2
hb09_p	B14	la26_n	H13	la27_n	A15	GND		dp2_c2m_n	M1
hb09_n	A14	GND		GND		UnCnnctd		GND	
GND		tck		GND		UnCnnctd		GND	
hb13_p	H14	tdi		scl	J14	GND		dp3_c2m_p	P2
hb13_n	G14	tdo_fmc		sda	N16	GND		dp3_c2m_n	P1
GND		+3V3_aux		GND		UnCnnctd		GND	
hb19_p	B12	tms		GND		UnCnnctd		GND	
hb19_n	B11	UnCnnctd		GND		GND		UnCnnctd	
GND		GND		+12V		GND		UnCnnctd	
hb21_p	G10	+3V3		GND		UnCnnctd		GND	
hb21_n	G9	GND		+12V		UnCnnctd		GND	
GND		+3V3		GND		GND		UnCnnctd	
+VADJ	VFMC	GND		+3V3		GND		UnCnnctd	
GND		+3V3		GND		UnCnnctd		GND	

Note:

- Blue cells show FMC LPC-compliant signals.
- Green cells show FMC HPC-compliant signals.
- Orange cells show FMC HPC-compliant signals with naming mismatch with VITA57.1 specification.
- Red cells show non-FMC compliant signals; these signals should ONLY be used if your daughter card is for use with the XpressK7. Daughter cards that use these 10 signals must not be used on a full HPC FMC carrier board. If not used, the 10 GND in the red cells should not be routed on the daughter card FMC connector.

- You must verify that every FMC signal used on your FMC daughtercard is present on the XpressK7.

Note: If no FMC card is mounted or if there is no FPGA on the mounted FMC card, switch SW5 (the FMC JTAG switch) must be in the closed position as shown in Figure 7.

3.6.3 VFMC (VADJ) Settings

All signals on the FMC connector are linked to the high-range banks of the FPGA, meaning that these banks support 1.8V/2.5V and 3.3V signaling.

By default, the high range banks are set to 2.5V via the VFMC selection jumper, as shown below:

Figure 8: VFMC selection jumper

You can select a different voltage (1.8V or 3.3V) by moving the VFMC selection jumper.

Note:

- You should *only* move the VFMC selection jumper when the XpressK7 is switched off.
- Even if you do not use the FMC, you must still plug the VFMC into one on the 3 voltages (1.8V/2.5V/3.3V). If you do not, the FPGA may not work correctly.

3.6.4 FMC Mechanical Dimensions

The following diagram shows the mechanical dimensions of the FMC Mezzanine card:

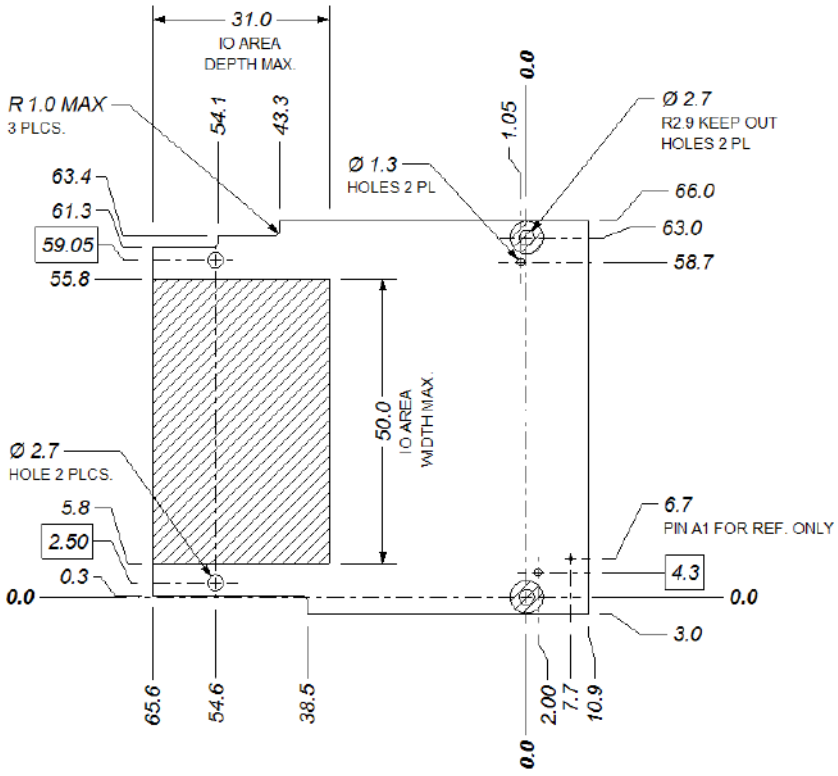

Figure 9: Mechanical dimensions of the FMC-HPC card

Note: The XpressK7 board package contains a DWG/STEP drawing of the XpressK7.

3.7 Local Reset

One active low reset push button is available on the board to enable register initialization:

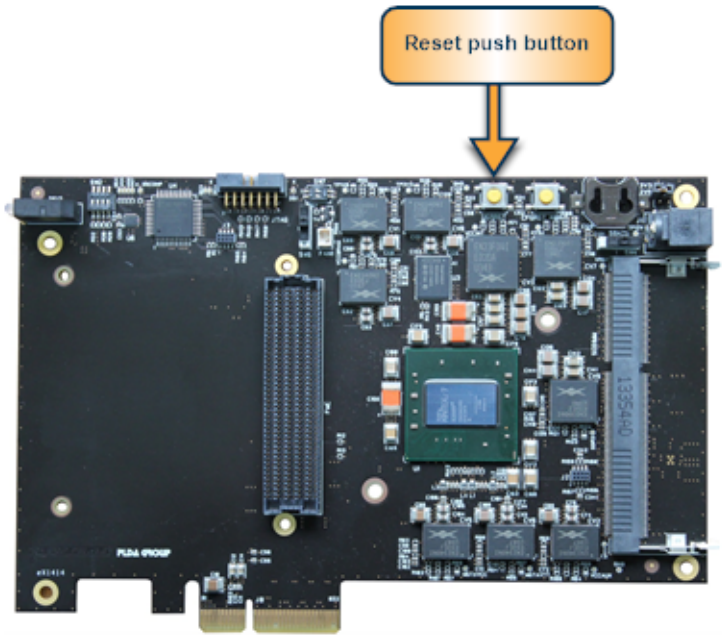

Table 8: Reset button

Signal	FPGA Pin
user_reset#	Y20

Table 9: Reset button pin assignment

3.8 Front Tricolor LEDs

One active-high tricolor LED is available on the front-facing bracket of the XpressK7. This LED can be lit red, green and amber (red and green together), depending on the associated signal.:

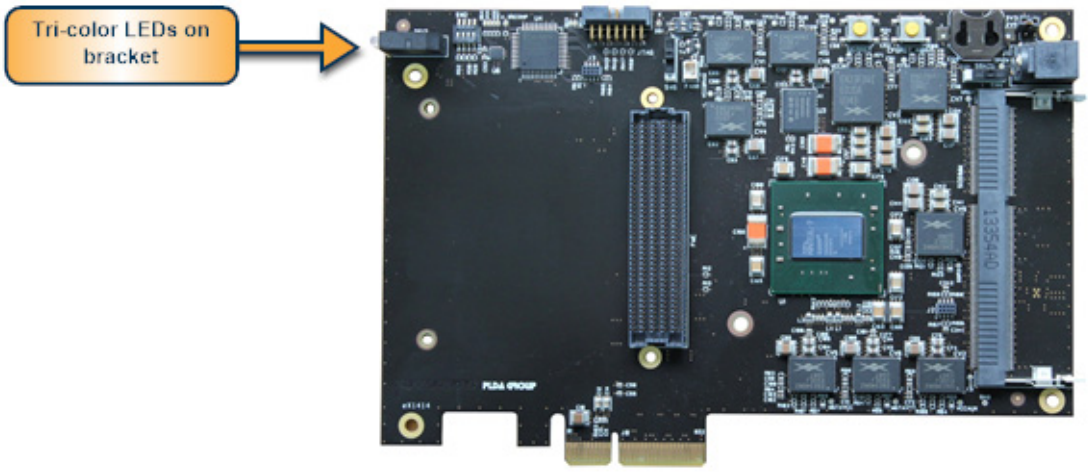

Table 10: Tricolor LEDs

Signal	FPGA Pin	LED
led_g1_hp	T7	Lower Green LED
led_r1_hp	V7	Lower Red LED
led_g2_hp	U4	Upper Green LED
led_r2_hp	V2	Upper Red LED

Table 11: Tricolor LED pin assignment

3.9 On-Board LEDs

Four active-high SMD LEDs are available on the board.:

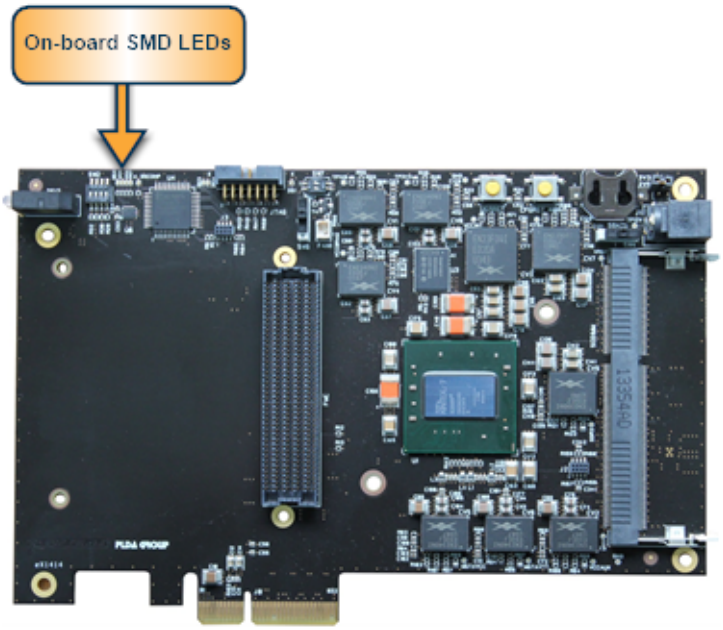

Table 12: On-board LEDs

Signal	FPGA Pin
user_led0_hp	W10
user_led1_hp	V11
user_led2_hp	Y10
user_led3_hp	W13

Table 13: On-board LED pin assignment

3.10 Mechanical Switches

Four user switches are available on the solder side of the XpressK7. These enable four IOs to be set to a logical ’0’ or a logical ’1’. .

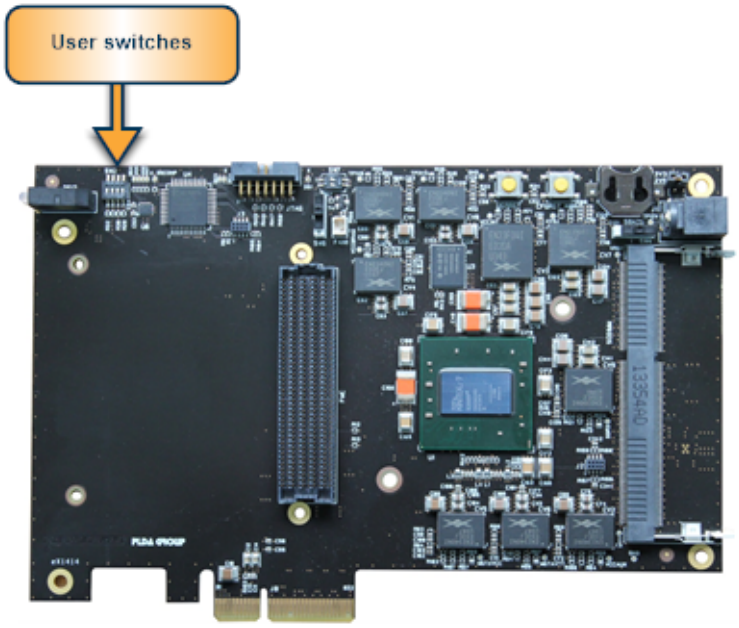

Figure 10: Mechanical switches

Signal Name	FPGA Pin
usr_sw1	AA15
usr_sw2	V8
usr_sw3	Y8
usr_sw4	Y7

Table 14: Pin assignments for the mechanical switches