## **QuickPCle Expert for Xilinx Build History**



Version	Build	Package Changes
1.5.6	085	Added support for Virtex UltraScale.
		Updated PCIe Hard IP to Vivado 2015.3:
		<ul> <li>updated 7 Series FPGA Gen2 Integrated Block for PCI Express to v3.2.</li> </ul>
		<ul> <li>updated Virtex-7 FPGA Gen3 Integrated Block for PCI Express to v4.1.</li> </ul>
		<ul> <li>updated UltraScale Series FPGA Gen3 Integrated Block for PCI Express to v4.1.</li> </ul>
1.5.5	080	Added support for Kintex UltraScale.
1.5.4	075	<ul> <li>Added support for all configurations of lanes and PCle link speed - x1/x2/x4/x8 and Gen1/Gen2/ Gen3.</li> </ul>
1.5.3	070	<ul> <li>Added AXI Master user side band signal to report Memory errors, PCIe TLP Attributes and Requester/Completer ID for Data Integrity, Cache Coherency and Virtualization support.</li> </ul>
		<ul> <li>Added ability by AXI Master Interfaces to issue narrow transfers, down to 8-bits accesses.</li> </ul>
		<ul> <li>Added support for BAR01 remapping for customer purposes (NVMe for instance).</li> </ul>
		Added support for data protection.
		Updated Bridge Internal Bus.
		<ul> <li>Implemented parity based data protection through Bridge datapath.</li> </ul>
		<ul> <li>Added support for PCIe to AXI and AXI to PCIe Ordering Rules Observance.</li> </ul>
		<ul> <li>Added support for DMA and Address Translation modules to limit AXI burst size to cache line size (32 or 64 Bytes).</li> </ul>
		<ul> <li>Added support for ECC reporting.</li> </ul>
1.5.2	060	Added AXI4 Stream Out Reset Feature.
1.5.1	055	Added support for Artix-7 and Zynq 7000 FPGA Hard IP.
		Added AXI4 Stream In Reset Feature.
		Timing optimizations when packing is enabled.
1.5.0	050	Added support for x4 gen3.
1.4.6	045	Added support for Virtex-7 Gen3 HIP.
1.4.5	035	Timing optimizations

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Version	Build	Package Changes	
1.4.3	030	Added support for AXI Slave configurable ID Width.	
		Added support for Completion Ordering Rules.	
		<ul> <li>Added support for Mixed AXI4-Lite and AXI Slave Interface.</li> </ul>	
		<ul> <li>Added support for V7 x4 gen2 and x8 gen1.</li> </ul>	
		<ul> <li>Added support for AXI Slave Fixed and Wrap Burst Types.</li> </ul>	
		Added support for AXI Slave Narrow Transfers.	
		Added support for AXI Slave Non-Contiguous Strobes.	
		Updated Help content for wizard.	
1.4.2	026	Fixed timing issues	
1.4.1	025	Removed CDC from the Reference Design application.	
		Fixed issue linked to throughput calculation.	
		Updated Core Wizards.	
1.4.0	020	First release	