QuickPCIe HIP Core for Xilinx v1.5.6

Revision history

Release	Classification	Level	Description	Files modified	Impact	Workaround
1.4.0	Feature	High	First release			
1.4.1	Feature	Medium	Added Stream In Packing: uncontiguous strobes are now supported.	qpcie_axi4_sti2sto.v, qpcie_axi4str_if.v, qpcie_top.v		
1.4.1	Feature	Medium	Added Early termination with Byte granularity.	qpcie_dma_engine.v, qpcie_axi4str_if.v, qpcie_unifiedbus_h.v		
1.4.1	Feature	High	Added Interconnect Pipeline options: Full, Automatic, Custom or No Pipeline modes.	qpcie_interconnect.v, qpcie_util_pkg.v		
1.4.1	Feature	High	Speed Optimizations.	All files		
1.4.1	Feature	Medium	Updated Xilinx Series-7 Hard IP with version 1.5	qpcie_v7_hip_top.v, v7_pcie_hip/*.v		
1.4.1	Feature	Low	Added Stream In Packet Number optional setting	qpcie_ref_design_v0.v		
1.4.1	Feature	Low	Added REFD_PERF register.	qpcie_ref_design_v0.v		
1.4.3	Fix	Medium	Applied Xilinx workaround for Ivy Bridge interoperability.	qpcie_v7_hip_128b_gt_wrapper.v		
1.4.3	Fix	Low	Added Synthesis Project for PLDA XpressV7-LP Board			
1.4.3	Fix	Medium	Fixed Completion Timout counter calculation.	qpcie_*_pcie_hip_if.v		
1.4.3	Fix	Medium	Fixed Early Termination issue when it occurs on last Byte position reaches the end of the Page minus Datapath.	qpcie_dma_engine.v		
1.4.3	Fix	High	Fixed properties of Internal Registers	qpcie_internal_reg.v		
1.4.3	Feature	Low	Added support for AXI Slave configurable ID Width.	qpcie_top.v, qpcie_layer.v, qpcie_axi4_slv_if.v, qpcie_axi4_mst2slv.v		
1.4.3	Feature	Medium	Added support for Completion Ordering Rules.	qpcie_ad_translator.v, qpcie_layer.v		
1.4.3	Feature	Low	Added support for Mixed AXI4-Lite and AXI Slave Interface.	qpcie_internal_reg.v, qpcie_ad_translator.v		
1.4.3	Fix	High	Fixed Bridge Configuration Space Content.	qpcie_internal_reg.v		
1.4.3	Feature	Low	Added optional support for Bridge Internal Registers implemention as "Read As Zero - Write Ignored".	qpcie_internal_reg.v		
1.4.3	Enhancement	Low	Updated AXI Master Write ID Management.	qpcie_ad_translator.v, qpcie_axi4_mst_if.v		
1.4.3	Fix	Medium	Fixed issue on Stream In Interface resulting in missing packet with SG-Reporting in random conditions.	qpcie_axi4_str_if.v		
1.4.3	Enhancement	Low	Reviewed Error Management.	qpcie_axi4lite_mst_if.v, qpcie_axi4lite_slv_if.v, qpcie_axi4_mst_if.v, qpcie_axi4_slv_if.v, qpcie_plda_pcie3_sip_if.v, qpcie_unifiedbus_h.v, qpcie_dma_engine.v, qpcie_ad_translator.v		
1.4.3	Feature	Medium	Added support for AXI Slave Fixed and Wrap Burst Types.	qpcie_axi4_mst2slv.v, qpcie_axi4_slv_if.v, qpcie_ad_translator.v		
1.4.3	Feature	Medium	Added support for AXI Slave Narrow Transfers.	qpcie_axi4_mst2slv.v, qpcie_axi4_slv_if.v		
1.4.3	Feature	Medium	Added support for AXI Slave Non-Contiguous Strobes.	qpcie_ad_translator.v		
1.4.3	Fix	High	Fixed UNB Write Completion Transfer ID management when AXI Write Completions are not returned in order.	qpcie_axi4_mst_if.v		
1.4.3	Feature	Medium	Added support for V7 x4 gen2 and x8 gen1.	qpcie_v7_hip_128b*		
1.4.4	Fix	Low	Fixed DMA Abort mechanism.	qpcie_axi4str_if.v		
1.4.4	Fix	Medium	Fixed Address Translation Table Events Assertion.	qpcie_internal_reg.v		
1.4.4	Fix	Low	Fixed Packet split mechanism to ensure PCIe MWR with length of 3 DW or more enable only bytes that are contiguous.	qpcie_ad_translator.v		
1.4.4	Fix	Low	Fixed issue when split read completion are received.	qpcie_ad_translator.v		
1.4.4	Feature	Medium	Added ECAM support.			
1.4.4	Fix	Low	Fixed incorrect packet split when first DW byte enables are not contiguous.	qpcie_ad_translator.v		
1.4.4	Fix	Low	Fixed AXI Write Fixed Burst Type conversion to PCIe MWR when AXI Slave Datapath is equal or greater than Bridge Datapath.	qpcie_axi4_slv_if.v		
1.4.4	Fix	Low	Fixed Address Translation Discard and Fetch Error assertion.	qpcie_ad_translator.v		
1.4.4	Fix	Medium	Fixed AXI Master Read Data Response deassertion.	qpcie_axi4_mst_if.v, qpcie_axi4_slv2mst_if.v		
1.4.4	Feature	Low	Added optional RAM arbitration mode to force arbitration even when End Of Packet is not asserted.	qpcie_ram_access.v		
1.4.4	Fix	High	Fixed issue when AXI Slave Datapath is narrower than Bridge Datapath and Write Valid is asserted before Address Write Valid.	qpcie_axi4_mst2slv.v		
1.4.4	Fix	Low	Fixed DMA end: DMA is ended after 256us timeout only if aborted.	qpcie_dma_engine.v		
1.4.4	Fix	Low	Fixed Address Translation Doorbell assertion.	qpcie_ad_translator.v		
1.4.4	Fix	Medium	Speed Optimizations.	qpcie_interconnect.v, qpcie_str_pipeline.v		
1.4.4	Feature	High	Spyglass and LEC Checking and IP Clean-Up	All files		
1.4.4	Fix	High	Fixed MSI messages reception in Rootport mode.	qpcie_internal_reg.v		
1.4.5	Fix	Low	Fixed DMA Early Termination when last valid dataphase contains no valid byte.	qpcie_dma_engine.v		

1.4.5	Fix	Medium	Fixed Address Translation write pointer assignment when several consecutive write transactions with no valid bytes are received.	qpcie_ad_translator.v		
1.4.5	Fix	Medium	Fixed DMA Abort termination.	qpcie_dma_engine.v		
1.4.5	Feature	High	Timing Optimizations	qpcie_util_pkg.v.v, qpcie_dma_engine.v, qpcie_interconnect.v		
1.4.5	Fix	Low	Fixed potential issue on PCIe to AXI Ordering Rule D2b.	qpcie_ad_translator.v		
1.4.6	Fix	Low	Fixed AXI to PCIe D4 Ordering Rule : Completions can now pass before CFGWR and IOWR.	qpcie_ad_translator.v		
1.4.6	Fix	Low	Fixed AXI to PCIe A3,A4,D3,D4 Ordering Rules : Posted and Completions can now overtake Non-Posted and one CFGWR if no sufficient NP credits are available.	qpcie_ad_translator.v		
1.4.6	Fix	Medium	Fixed Memory Read split mechanism when all outstanding requests are busy.	qpcie_ad_translator.v		
1.4.6	Fix	Low	Fixed AXI Stream In data storage when back to back early termination is detected.	qpcie_ad_translator.v		
1.4.6	Fix	Low	Added V7 Gen3 HIP Support.	qpcie_v7g3_*.v		
1.5.0	Fix	Low	Masked transmitted unvalid bytes to prevent X from RAM models to be propagated on PCIe link causing retraining in simulation.	qpcie_v7_pcie3_hip_if.v		
1.5.0	Fix	Medium	Fixed AXI Stream Alignment when supported Read Request Size is set to multiple of 4 Bytes.	qpcie_axi4str_if.v		
1.5.0	Fix	Low	Fixed issue when Direct DMA size is not multiple of datapath, AXI Stream Datapath < Bridge Datapath and no TLAST is asserted.	qpcie_axi4_sti2sto.v, qpcie_axi4str_if.v		
1.5.0	Enhancement	Low	Regenerated all IP Core Instances with Wizard v146b045 (20130726).	qpcie_ipcore_refd_*.v		
1.5.0	Feature	Low	Replacing 'hXX by 'hFF on AXI Master wdata when wstrb is 0b to prevent errors in simulation.	qpcie_axi4_mst_if.v		
1.5.0	Fix	Medium	Fixed data alignment issue when in SG DMA type 00 mode.	qpcie_dma_engine.v		
1.5.0	Enhancement	Low	Regenerated all IP Core Instances with Wizard v150b050 (20130731).	qpcie_ipcore_refd_*.v		
1.5.0	Fix	High	Fixed multiple Read Completion issued when MRD is throttled to prevent p2q_rdtable_wren assertion conflict.	qpcie_v6_pcie_hip_if.v, qpcie_v7_pcie_hip_if.v		
1.5.0	Fix	High	Fixed PCIe MRD possible loss when all PCIe to AXI outstanding read requests are pending.	qpcie_v6_pcie_hip_if.v, qpcie_v7_pcie_hip_if.v		
1.5.0	Enhancement	Medium	Added Zynq 7000 Support			
1.5.0	Enhancement	Medium	Added Artix 7 Support			
1.5.0	Enhancement	Low	Forced Xilinx DCRAM, used for CDC, to be synthesized with Distributed RAM for timing purpose.	qpcie_dcram.v		
1.5.0	fix	Medium	Fixed dw_offset computation in 128-bit datapath	qpcie_v7_pcie3_if.v		
1.5.0	fix	High	Fixed unb write request ack management	qpcie_v7_pcie3_if.v		
1.5.0	Enhancement	High	Fixed unb write completion ack management	qpcie_v7_pcie3_if.v		
1.5.0	Enhancement	Low	Added error reporting	qpcie_v7_pcie3_if.v		
1.5.1	Fix	Low	Forces SG-DMA interruption when SG-Descriptor EndOfChain (DESC_SE_COND bit 0) is set, even if NextDescReady is not set.	qpcie_dma_engine.v		
1.5.1	Fix	Low	Fixed unexpected SG-Descriptor Status's EndOfPacket (DESC_STATUS bit 2) report when SG-DMA source is not of type Stream.	qpcie_dma_engine.v		
1.5.1	Fix	Low	Fixed SG-DMA reporting issue if write completion is received in the same clock cycle the write request is issued.	qpcie_dma_engine.v		
1.5.1	Enhancement	Low	Timing Optimizations when Packing is enabled.	qpcie_axi4_sti2sto.v		
1.5.1	Fix	High	Fixed possible data corruption when data extraction from Hard IP is throtlled due to MRD received at the same time a Completion is sent.	qpcie_v6_pcie_hip_if.v, qpcie_v7_pcie_hip_if.v		
1.5.1	Fix	High	Fixed MSI sending. Allow up to 32 MSI number support.	qpcie_v7_pcie3_hip_if.v		
1.5.1	Fix	High	Fixed PCIe MRD possible loss when all PCIe to AXI outstanding read requests are pending. Fixed possible data corruption when data extraction from Hard IP is throtlled due to MRD received at the same time a Completion is sent.	qpcie_v7_pcie3_hip_if.v		
1.5.1	Fix	Low	Fixed possible improper SG-DMA End termination and Page length computation when requested DMA Length is less than Descriptor Page size.	qpcie_dma_engine.v		
1.5.1	Feature	Low	Added AXI4 Stream In Reset Feature.	qpcie_axi4str_if.v		
1.5.1	Fix	Medium	Fixed split PCIe Competion sending when two back to back Completions with same tag are sent.	qpcie_v7_pcie3_hip_if.v		
1.5.1	Fix	High	Fixed possible Bridge to PCIe write completion loss when V7-GTH Hard IP issues pcie_rq_se_num_vld before the end of MWR transmission.	qpcie_v7_pcie3_hip_if.v		
1.5.2	Fix	Low	Fixed possible issue when Direct DMA is ended through early termination.	qpcie_dma_engine.v		
1.5.2	Feature	Low	Added AXI4 Stream Out Reset Feature.	qpcie_resync.v, qpcie_axi4str_if.v		
1.5.2	Fix	Medium	Fixed unexpected Uncorrectable Internal Error generated by V7 Gen3 HIP on HP servers.	qpcie_v7_pcie3_hip_if.v		
1.5.3	Enhancement	High	Added AXI Master user side band signal to report Memory errors, PCIe TLP Attributes and Requester/Completer ID for Data Integrity, Cache Coherency and Virtualization support. Updated Bridge Internal Bus to v150.	All files		
1.5.3	Enhancement	Medium	Added ability by AXI Master Interfaces to issue narrow transfers, down to 8-bits accesses.	qpcie_axi4_mst_if.v		
1.5.3	Enhancement	Low	Code enhancements to get rid of Lint and CDC warnings.	All files, qpcie_resync/dcfifo.v moved in cdc directory	Some Lint/CDC warnings are reported by SpyGlass and Blue Pearl tools.	No workaround.
1.5.3	Enhancement	Medium	Added support for BAR01 remapping for customer purpose.	qpcie_xx_hip_top.v, qpcie_ad_translator.v		
1.5.3	Fix	Low	Fixed DMA read request size according to PCIe negotiated read request size.	qpcie_dma_engine.v	When DMA read request size is higher than 512 Bytes and greater than PCIe negotiated read request size, DMA issues on PCIe size read request of larger size than expected.	Set DMA read request size equal to 256 Bytes, or ensure SW sets PCIe negotiated read request size equal or larger than DMA ones.

1.5.3	Enhancement	High	Added support for Data Protection: - Added RAM rderr output port to report if data error has been detected. - Used same memory model as XR2 and XR3 IPs. - Added AXI Master and Slave wderr and rderr signals to allow Bridge and Application to report Memory errors. - Updated Bridge Internal Bus to v151.	All files		
1.5.3	Enhancement	High	Reviewed Xilinx Hard IP structure: - Updated Hard IP files content and hierarchy with Vivado 2014.2 - Hard IP files are now in source code, even in full and eval versions - Designed Common PCIe Interface module for all Hard IPs - Enhanced Error Reporting - Added support for PCIe to AXI and AXI to PCIe Ordering Rules Observance	core/source/vlog/hip/*/*, qpcie_xx_hip_top.v, qpcie_pcie_if.v, qpcie_p2q_wr_mgt.v, qpcie_p2q_rd_mgt.v, qpcie_q2p_p_mgt.v, qpcie_q2p_np_mgt.v, qpcie_cfgio_mgt.v		
1.5.3	Fix	Low	Fixed some LINT issues.	qpcie_p2q_wr_mgt.v, qpcie_q2p_p_mgt.v	Some Lint/CDC warnings are reported by SpyGlass and Blue Pearl tools.	No workaround.
1.5.3	Enhancement	High	Implemented parity based data protection through Bridge datapath (not through Hard IP). Updated SCRAM models: ECC port is now 1 bit per 64 bits of data.	All files		
1.5.3	Enhancement	Medium	Added support for DMA and Address Translation modules to limit AXI burst size to cache line size (32 or 64 Bytes).	qpcie_dma_engine.v, qpcie_ad_translator.v		
1.5.3	Fix	Medium	Fixed PCIe to AXI B.2 Ordering Rule issue: PCIe Non-Posted requests were able to pass a PCIe posted request if it was throttled (because all Memory Write Buffers are busy).	qpcie_ad_translator.v	PCIe Non-Posted requests were able to pass a PCIe posted request if it was throttled (because all Memory Write Buffers are busy).	No workaround.
1.5.3	Enhancement	Medium	Added support for ECC reporting (AXI data protection signal is corrupted when Bridge Memory Buffer reports ECC error).	qpcie_axi4_mst_if.v		
1.5.3	Enhancement	High	Added early support for DMA-Lite. When enabled: - Reduced Gate Count - Features limited to infinite PCIe <-> AXI-Stream SG-DMA with Desc Reporting	qpcie_axi4str_lite_c2h.v, qpcie_axi4str_lite_h2c.v, qpcie_dma_lite_h2c, qpcie_dma_lite_c2h.v		
1.5.3	Fix	Low	When a Packet is discarded by Address Translation module because of ECRC or Memory Error, a AXI Write Completion now returns an error.	qpcie_ad_translator.v		
1.5.3	Fix	Low	Fixed some LINT issues.	qpcie_q2p_p_mgt.v		
1.5.3	Fix	High	Fixed MSI generation when MSI Number is less than 32. When MSI are enabled and MSI Number is less than 32, if an Interrupt source was asserted while its number is greater than MSI Number, it caused multiple MSI to be sent.	qpcie_pcie_if.v	When MSI are enabled and MSI Number is less than 32, if an Interrupt source is asserted while its number is greater than MSI Number, it causes multiple MSI to be sent.	Use MSI Number equal to 32.
1.5.4	Fix	Low	Fixed some LINT issues.	qpcie_axi4str_if.v		
1.5.4	Fix	High	Fixed Critical issue which may caused incorrect CPLD tag to be returned when more than QPCIE_ATR_PCIE_RBUF_NUM outstanding read requests are received at the same time.	qpcie_p2q_rd_mgt.v	When more than QPCIE_ATR_PCIE_RBUF_NUM outstanding read requests is received, returned CPLD tag may be wrong.	Use QPCIE_PCIE3_NPBUF_SIZE != 0.
1.5.4	Enhancement	High	Added all QuickPCIe Xilinx PCIe configurations, from x1 gen1 up to x8 gen3: - Added support for 64-bit datapath. - Updated Xilinx Series-7 PCIe Hard IP with Vivado 2014.3. - Added support for x1/x2/x4/x8 gen1/gen2 to Xilinx Series-7 PCIe Hard IP. - Added support for x1/x2/x4/x8 gen1/gen2/gen3 to Xilinx Virtex-7 FPGA Gen3 PCIe Hard IP.	core/source/vlog/hip/s7/*, qpcie_ad_translator.v, qpcie_pcie_if.v, qpcie_p2q_wr_mgt.v, qpcie_p2q_rd_mgt.v, qpcie_q2p_p_mgt.v, qpcie_q2p_np_mgt.v		
1.5.4	Fix	High	Fixed Critical issue which may caused PCIe to AXI MWR (or CPLD) corruption when its reception immediately follows CPLD (or respectively MWR) reception with an odd combination of packet size and lower address.	qpcie_p2q_rd_mgt.v, qpcie_q2p_np_mgt.v	PCIe to AXI MWR (or CPLD) data is corrupted: first dataphase is skipped.	No workaround.
1.5.4	Fix	Low	Fixed CDC issue reported by SpyGlass.	qpcie_dcfifo.v, qpcie_dcram.v	SpyGlass reports error in cdc_structural_check.	Ignore this SpyGlass reported error.
1.5.5	Fix	Medium	Fixed improper handling of incoming write request when an ECRC Error, Receive Buffer Memory Error or AXI Application Data Error is received on subsequent dataphases (not on first dataphase) and when erroneous packets are not to be committed.	qpcie_ad_translator.v	One Write Buffer resource can never be released, resulting in possible hang due to ordering rules observance.	Set QPCIE_PKT_ERROR_COMMIT to 1.
1.5.5	Enhancement	High	Add support for Kintex Ultrascale Hard IP, from x1 gen1 up to x8 gen3.	core/source/vlog/hip/*/*, qpcie_xx_hip_top.v		
1.5.5	Fix	Medium	Fixed Bridge Interconnect issue when Bridge's AXI Master Interface receives Interleaved Read Data towards different Destination (for instance to PCIe and to AXI).	qpcie_interconnect.v	Read Data reception hangs, resulting into a deadlock.	Do not allow Read Data Interleaving on Bridge AXI Master Interface.
1.5.5	Fix	Medium	When an AXI Slave write transaction ending with a null dataphase (that is with TSTRB=0) is translated into an AXI Stream burst, AXI Stream Out now transmits a null dataphase (that is with TRSB=TKEEP=0) along with TLAST asserted.	qpcie_ad_translator.v	When an AXI Slave write transaction ending with a null dataphase (that is with TSTRB=0) is translated into an AXI Stream burst, TLAST was not asserted at the end of the burst if the AXI Slave write transaction crosses Bridge maximum payload size.	Do not send AXI write transaction with null last dataphase (that is with TSTRB=0).
1.5.6	Enhancement	Medium	Added AXI Write Completion Timeout: if PCIe link is down, and awrite request is submitted by AXI application to PCIe, a SLVERR write response is returned after 2**QPCIE_A2P_WRCPL_TIMEOUT ms (128 ms by default) (us in simulation), and write request is discarded.	qpcie_pcie_if.v, qpcie_q2p_p_mgt.v		
1.5.6	Enhancement	Low	Endpoint now reports it is ready for turn off when there is no pending non-posted requests or pending completions to return.	qpcie_pcie_if.v		
1.5.6	Fix	Low	Bridge now sets PCIe No Snoop and Relaxed Ordering bits in the TLP Attributes field only if they are enabled in the Device Control Register of the PCIe Configuration Space.	qpcie_pcie_if.v, qpcie_q2p_np_mgt.v, qpcie_q2p_p_mgt.v	If translation parameters in the Address Translation module or DMA Engines specifies No Snoop and Relaxed Ordering bits to be asserted, the Bridge sent them regardless of Device Control Register settings.	The application should check that Device Control Register allows No Snoop and Relaxed Ordering bits to be asserted before setting these values in the translation parameters.
1.5.6	Enhancement	High	Added support for Automatic conversion between PCIe Attributes and Traffic Class and AXI memory types and Quality of Service.	qpcie_internal_reg.v, qpcie_ad_translator.v		
1.5.6	Enhancement	Low	Added support for AXI to PCIe read completion discarding.	qpcie_top.v, qpcie_bridge_axi_layers.v, qpcie_axi4_mst_if.v, qpcie_axi4_slv2mst.v		

1.5.6	Fix	Medium	Fixed Malformed Completion detection: the value of the IDO bit must not be considered by Receivers when determining if a TLP is a Malformed Packet.	qpcie_q2p_np_mgt.v	If the bridge issues a PCIe read request with IDO unset, but the returned completion has IDO bit set, the bridge detected it as malformed.	Do not set the IDO Completion Enable bit in the Device Control 2 register of the Completer.
1.5.6	Enhancement	High	Added MSI per-vector masking support.	qpcie_top.v, qpcie_internal_reg.v, qpcie_pcie_if.v		
1.5.6	Fix	Medium	Fixed Incorrect setting of PCIe MWR field: "First Dword Byte Enable" when write transaction is split on PCIe Maximum Payload size while Packet must be split later due to uncontiguous byte strobes.	qpcie_ad_translator.v	If an AXI write transaction must be split due to uncontiguous byte strobes, and also crosses PCIe maximum payload size boundary, split PCIe MWR have their "First Dword Byte Enable" field equal to first uncontiguous Dword Byte strobes.	No workaround.
1.5.6	Enhancement	Low	Added an option to enable AXI to AXI ordering rules. By default, this option is disabled. To enable this option, QPCIE_A2A_ORDRULES_EN must be defined equal to 1.	qpcie_ad_translator.v	When a PCIe to AXI Completion is to be returned to an AXI Slave Interface, it observes AXI to AXI ordering were observed. That is, if an AXI Write transaction was submitted to another AXI Slave Interface, PCIe to AXI Completion can't pass this AXI Write transaction.	No workaround.
1.5.6	Fix	Medium	Fixed Incorrect setting of PCIe MWR field: "First Dword last Enable" when write transaction is split on PCIe Maximum Payload size while Packet must be split later due to uncontiguous byte strobes.	qpcie_ad_translator.v	If an AXI write transaction must be split due to uncontiguous byte strobes, and also crosses PCIe maximum payload size boundary, split PCIe MWR have their "First Dword last Enable" field equal to AXI write transaction last Dword Byte strobes.	No workaround.
1.5.6	Enhancement	Low	Added support for Address Translation Table default values when Address Translation Tables are reconfigurable.	qpcie_internal_reg.v	When Address Translation Tables were reconfigurable, Address Translation Table default values were 0s.	No workaround.
1.5.6	Enhancement	Low	Restuctured Bridge according to Power Domains. Bridge Internal Registers module is now located in the top-level, rather than in the Bridging layer.	qpcie_top.v, qpcie_internal_reg.v, qpcie_bridge_axi_layers.v, qpcie_bridge_layer.v, qpcie_pcie_if.v	When implementing Clock and Power Gating, UPF needed to point on several modules, whose numbers depends on the number of DMA and Address Translation modules. Restructuring the IP allows the UPF to only point onto the Bridging and AXI layers top-level.	No workaround.
1.5.6	Fix	Low	Fixed RTL Syntax issue when QPCIE_DATA_PROT = 1.	qpcie_bridge_layer.v	A warning: "Select index out of bounds" occured when QPCIE_DATA_PROT = 1.	This warning could be safely ignored.
1.5.6	Fix	Low	Fixed possible violation of PCIe to AXI B.2 Ordering Rule: in specific condition, a PCIe Non-Posted requests was able to pass a PCIe posted request if it was throttled (because all Memory Write Buffers are busy or shared PCIe2AXI SCRAM access is granted to another module).	qpcie_ad_translator.v	PCIe Non-Posted requests were able to pass a PCIe posted request if it was throttled (because all Memory Write Buffers are busy or shared PCIe2AXI SCRAM access is granted to another module).	No workaround.
1.5.6	Enhancement	Low	Added support for control of request transmission to PCIe according to Bus Master Enable bit: when this bit is cleared in Endpoint mode, Bridge now doesn't issue Memory and I/O Read/Write Requests.	qpcie_top.v, qpcie_pcie_if.v, qpcie_q2p_np_mgt.v, qpcie_q2p_p_mgt.v	In Endpoint mode, when Bus Master Enable bit was cleared in PCI Command Register (Offset 04h), Bridge was able to sent Memory and I/O Read/Write Requests to PCIe.	Endpoint application shouldn't issue AXI to PCIe request while Bus Master Enable bit was cleared in PCI Command Register (Offset 04h).
1.5.6	Enhancement	Low	Added support for dynamic reconfiguration of PCIe Message Reception settings.	qpcie_internal_reg.v, qpcie_pcie_if.v, qpcie_p2q_wr_mgt.v, qpcie_ad_translator.v	PCIe Message Reception settings weren't dynamically reconfigurable. That is, PCIe Message Reception Support, Destination ID and Destination Address were fixed.	
1.5.6	Fix	Medium	Fixed DMA error reporting in AXI Master Write Channels. axi4_mstx_awuser[1] and axi4_mstx_wderr are now asserted when the source of the transfer has indicated that this packet is erroneous (for instance AXI SLVERR or DECERR, or PCIe Unsupported Request or Address).	qpcie_dma_engine.v, qpcie_axi4_mst_if.v	When the source of the DMA transfer reports an error of any type, although it is properly reported in DMA Descriptor and DMA Status Register, it wasn't reported in the awuser and wderr signals on AXI Interfaces.	Use Scatter Gather Descriptor or DMA Status Register to reject corrupted packets.