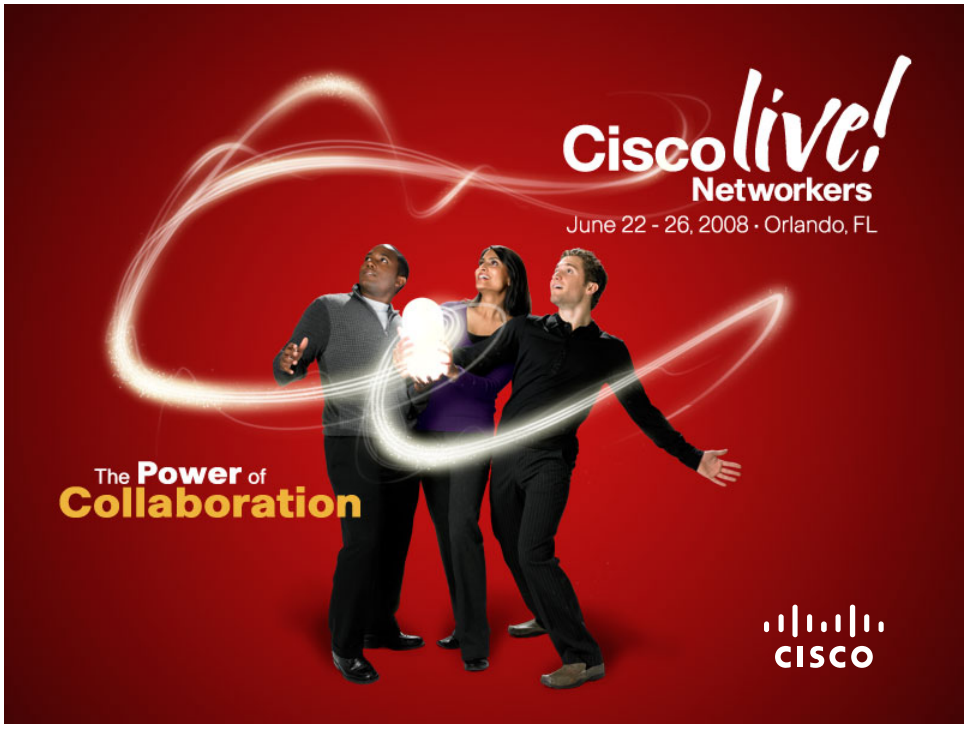
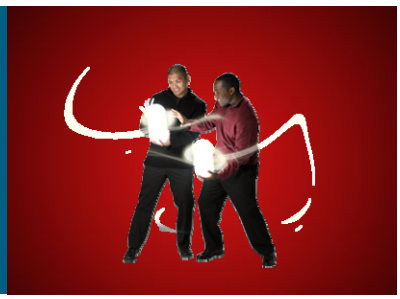


CISCO

Cisco live! Networkers

Cisco Catalyst 6500 Technical Deep Dive



BRKRST-3465

Session Goal

- To provide you with a thorough understanding of the Catalyst® 6500 switching architecture, packet flow, and key forwarding engine functions

Agenda

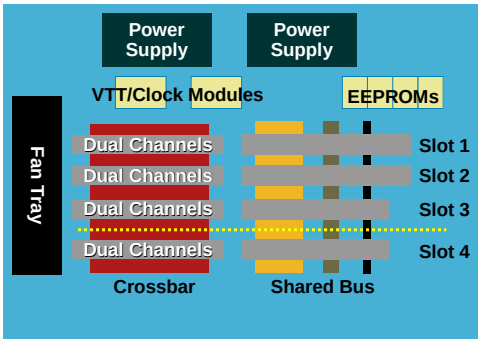
- Chassis and Power Supplies
- Supervisor Engine and Switch Fabric Architecture
- Cisco IOS Boot Process
- Module Architecture
- Layer 2 Forwarding
- IPv4 Forwarding
- IPv4 Multicast Forwarding
- Packet Walks

Catalyst 6500 Chassis Architecture

- Modular chassis in a variety of form factors
  - 3, 4, 6, 9, and 13-slot versions
- Enhanced (“E”) chassis offer higher system power capacity and better signal integrity
  - 3, 4, 6, and 9-slot versions
- Classic switching bus traces/connectors
- Crossbar fabric traces/connectors
- Redundant power supplies
- Fan tray for system cooling
  - 6509-NEB-A and 6509-V-E chassis offers redundant fan trays and air filtration
- Redundant voltage termination (VTT)/ clock modules
- Redundant MAC address EEPROMs

Catalyst 6503/6503E and 6504E

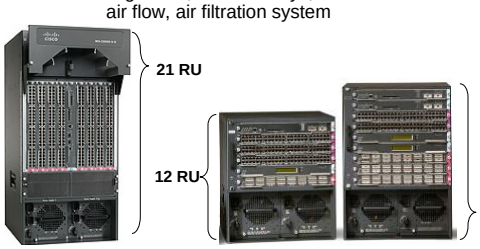
- Slots 1 and 2—Supervisor engine or switching module
- Other slots—Any switching module
- Two fabric channels per slot
- Power supplies in rear
  - 6503/6503E—Power entry modules (PEMs) in front of chassis provides power connection
- 950W AC/DC and 1400W AC power supplies for 6503/6503E
- 2700W AC/DC power supplies for 6504E

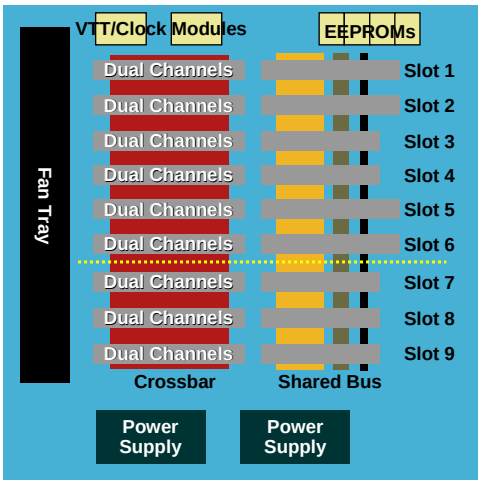


Note: CEF720 Modules Not Supported in Catalyst 6503 (Non-E) Chassis

Catalyst 6506/6509 and 6506E/6509E

- Slots 1 and 2—Supervisor Engine 1A / 2 or switching module
- Slots 5 and 6—Supervisor Engine 32/720 or switching module
- Other slots—Any switching module
- Two fabric channels per slot
- Wide variety of power supplies, from legacy 1000W to new 8700W—E chassis requires at least 2500W PS
- NEB-A and V-E chassis have vertical slot alignment, dual fan trays, front-to-back air flow, air filtration system

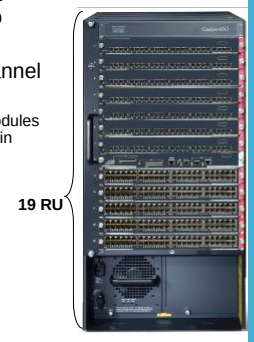


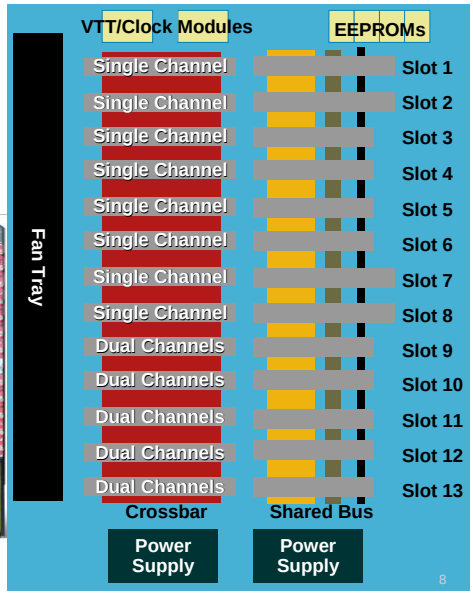


Note: WS-C6509-V-E supports only Supervisor 32 and Supervisor 720.

Catalyst 6513

- Slots 1 and 2—Supervisor Engine 2, or switching module
- Slots 7 and 8—Supervisor Engine 32/720, or switching module
- Wide variety of power supplies from 2500W to new 8700W
- One fabric channel slots 1–8
  - Dual-fabric modules not supported in slots 1–8!
- Two fabric channels slots 9–13
  - Any switching module





Power Supplies

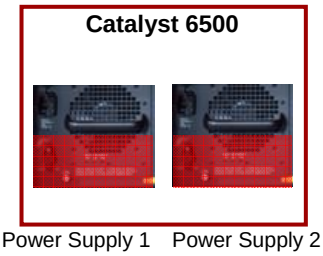
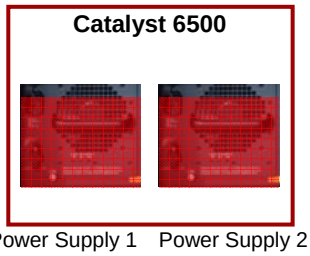
- Power Supplies for six, nine and thirteen slot chassis are located at front bottom of chassis
- Power Supplies for three and four slot chassis are located in the rear

AC Power Supplies	DC Power Supplies
950W**	950W
1000W**	1300W
1300W**	2500W
1400W	2700W
2500W**	4000W*
2700W	
3000W	
4000W	
6000W	
8700W	

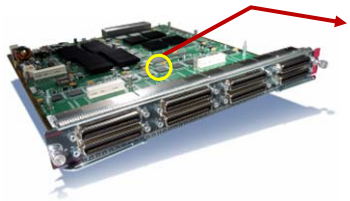
** Now EOS

Power Supply Redundancy

The Catalyst 6500 Can Utilize Two Power Supplies to Work in Either Combined or Redundant Mode

Redundant Mode	Combined Mode
 Power Supply 1 Power Supply 2	 Power Supply 1 Power Supply 2
In redundant mode, each power supply operates at ~50% capacity and provides the same total power as a single power supply – if one fails, the backup reverts to providing 100% power	In combined mode, each power supply operates at up to 83% capacity - if one fails, then the running supply provides 100% of its power capacity

Power Management



All Supervisors and Linecards have a power value programmed in EEPROM - this is used to identify how much power to reserve from the power budget.

Use the Power Calculator on cisco.com to determine the power supply and heat dissipation requirements - http://www.cisco.com/go/powercalculator

If insufficient power is available, the system powers down Power Devices, then switching modules, then services modules

Powered Devices and modules are powered off from highest numbered to lowest numbered (port or slot)

Agenda

- Chassis and Power Supplies
- Supervisor Engine and Switch Fabric Architecture
- Cisco IOS Boot Process
- Module Architecture
- Layer 2 Forwarding
- IPv4 Forwarding
- IPv4 Multicast Forwarding
- Packet Walks

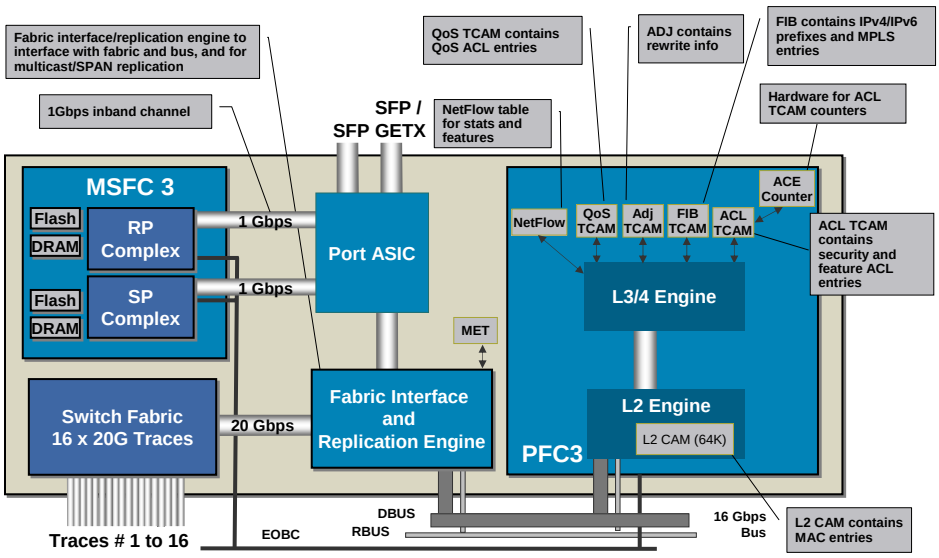
Supervisor 720

- 720-Gbps crossbar fabric
- PFC3A/B/BXL forwarding engine daughter card
- Integrated RP/SP CPUs on MSFC3 daughter card (600MHz MIPS)
- Supported from Cisco IOS 12.2(14)SX and Catalyst OS 8.1(1)

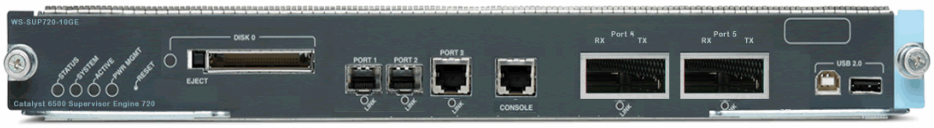
- 512/512MB (3A/B) or 1/1GB (3BXL) DRAM
- Internal RP and SP bootflash (64MB each)
- Optional 512MB and 1GB CF bootflash upgrade for SP
  - WS-CF-UPG-1GB=
  - WS-CF-UPG= (512MB)*
- Dual external compact flash slots
- 2 x GbE uplink ports—
  2 x SFP <or>
  1 x SFP and 1 x 10/100/1000

* Internal CF Adapter with 512MB CF comes standard on all Supervisor 720s ordered with 12.2(18)SXE5 or newer

Supervisor 720/PFC3 Architecture

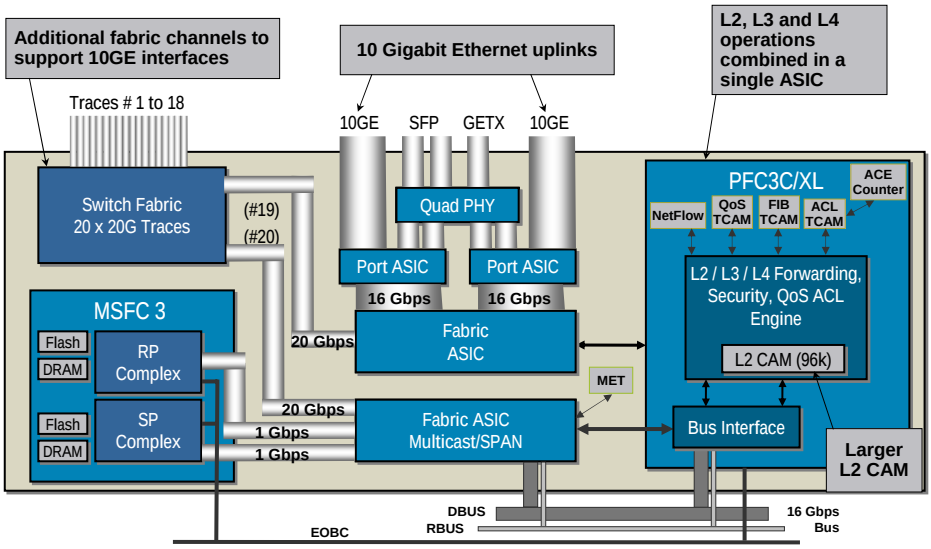


Supervisor 720-10G



- 720-Gbps crossbar fabric
- PFC3C/CXL forwarding engine daughter card
- Integrated RP/SP CPUs on MSFC3 daughter card
- Supported from Cisco IOS 12.2(33)SXH
- NOT supported with Catalyst OS
- 1GB SP/1GB RP DRAM
- Internal RP (64MB) and SP (1GB) boot devices
- Single external compact flash slot
- Uplink ports:
  - **2 x 10GE (X2)**
  - **2 x SFP**
  - **1 x 10/100/1000**
- All uplink ports are available in a redundant Supervisor configuration
- Two USB ports (one console, one device—currently disabled)

Supervisor 720-10G Architecture



Supervisor 32

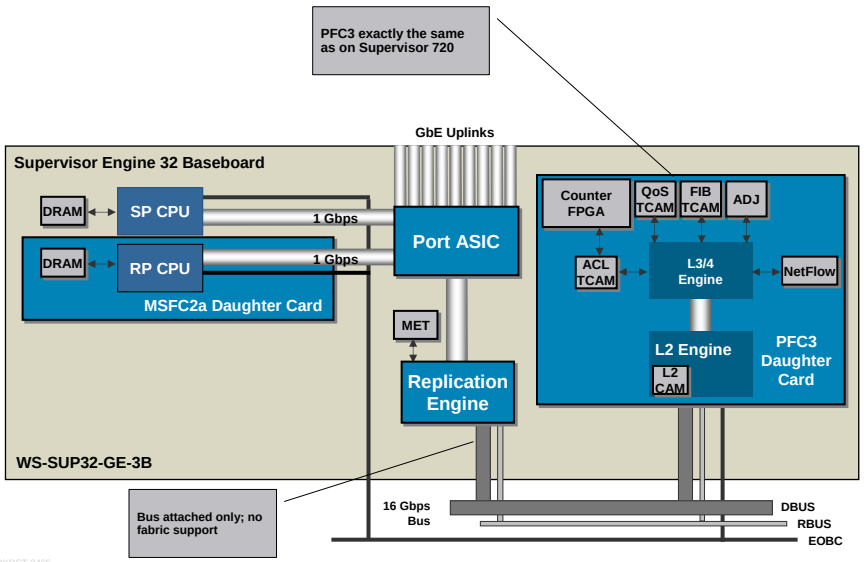
- Classic Supervisor—no fabric, uses 16-Gbps bus only
- PFC3B forwarding engine daughter card
- SP CPU (400MHz Sibyte)
- MSFC2a routing engine
- 512MB/512MB DRAM
- Internal CF bootdisk (256MB) and MSFC2A bootflash (64MB)
- External CF slot
- Uplink options:
  - 8 SFP + 1 10/100/1000
  - 2 10GE + 1 10/100/1000

2 10GE Xenpak +
1 10/100/1000 RJ-45 uplink ports

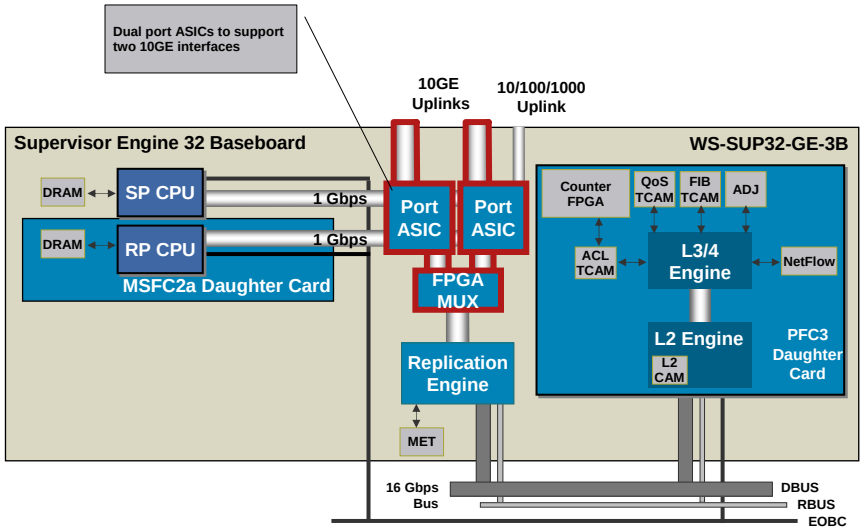
8 1GE SFP +
1 10/100/1000 RJ-45
uplink ports

Supported from Cisco IOS 12.2(18)SXF and Catalyst OS 8.4(1)/12.2(17)SXB7

Supervisor 32-8G/PFC3 Architecture



Supervisor 32-10GE/PFC3 Architecture

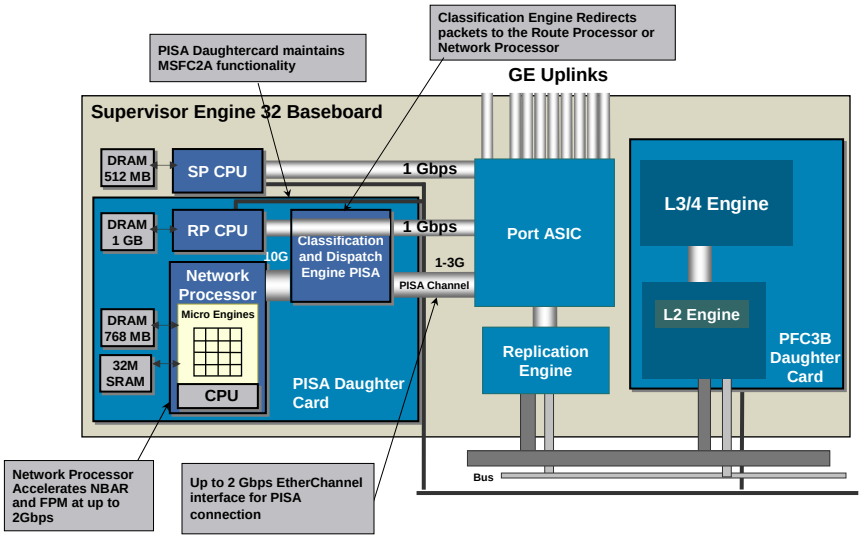


Supervisor 32 + PISA

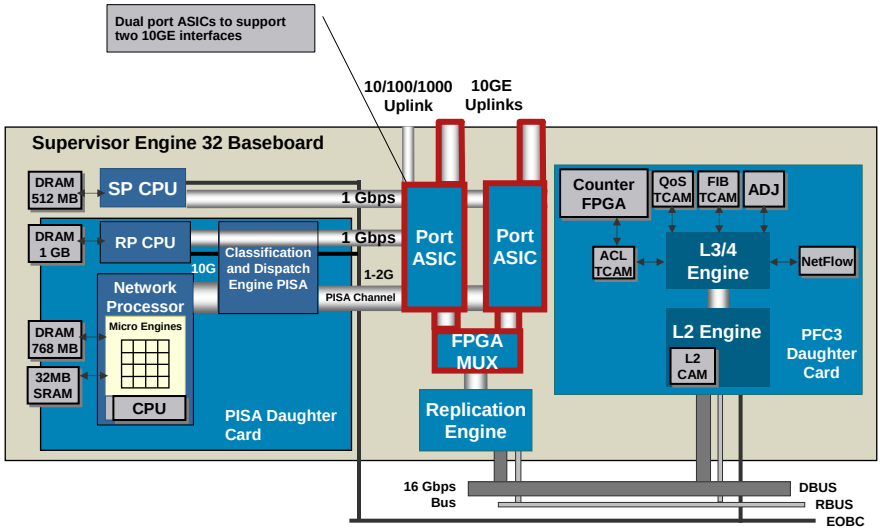
- Same Bus, SP and PFC3B characteristics as other Supervisor 32
- Improved Route Processor (750Mhz)
- 1GB RP DRAM by default
- PISA CF bootdisk (256MB)
- Deep and Stateful Packet Inspection
- Provides acceleration for NBAR (QoS) and FPM (security) For L3 IPv4 unicast packets at up to 2-Gbps
- Requires IOS 12.2(18)ZY—No support for Software Modularity
- Uplink options:
  - 8 SFP + 1 10/100/1000
  - -or-
  - 2 10GE + 1 10/100/1000

Supervisor 32 PISA Hardware Architecture

WS-S32-GE-PISA Diagram

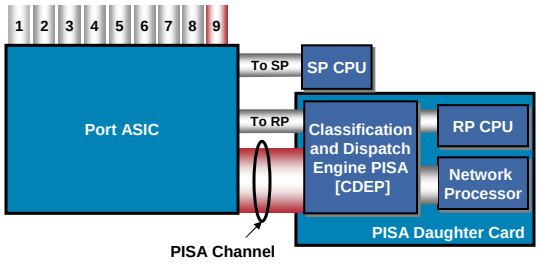


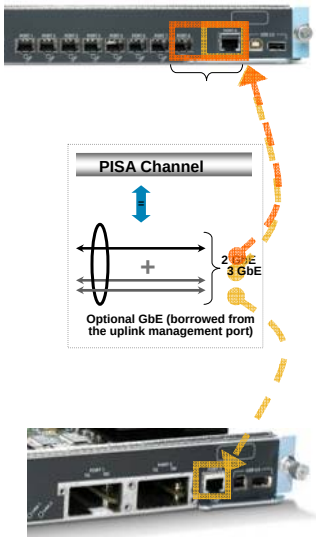
Supervisor 32-10GE/PFC3 Architecture



Supervisor 32 PISA Hardware Architecture
PISA Inband Channel

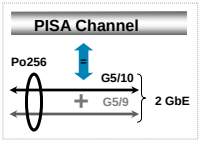
- In its default configuration, the PISA channel to the backplane is 1Gbps
- Max performance obtained when uplink copper port is dedicated for PISA
- On the WS-S32-GE-PISA, port 8 can also be added to the PISA channel to allow up to 3Gbps to PISA





Supervisor 32 PISA Hardware Architecture
PISA Inband Channel

- The copper port can be added or removed from the PISA channel during runtime




```
Sup32-PISA#sh run int Po256
<…>
!
interface Port-channel256
 mtu 4160
 no ip address
 load-interval 30
 speed nonegotiate
 mls qos trust cos
 flowcontrol receive on
 flowcontrol send on
 pisa-channel
end

Sup32-PISA(config-if)#int G5/9
Sup32-PISA(config-if)# channel-group 256 mode on
Sup32-PISA(config-if)#
*Apr 17 09:34:18: %PISA-4-PISA_CHANNEL_ADD:
   Uplink port g5/9 will be used for internal
   PISA channel.
*Apr 17 09:34:18: %PISA-4-PISA_CHANNEL_CFG:
   Configuration commands must not be applied on
   pisa-channel port(s).
```

```
Sup32-PISA#show etherchannel 256 summary
Flags:  D - down        P - bundled in port-channel
        I - stand-alone s - suspended
        H - Hot-standby (LACP only)
        R - Layer3      S - Layer2
        U - in use      f - failed to allocate aggregator

        M - not in use, minimum links not met
        u - unsuitable for bundling
        w - waiting to be aggregated
Number of channel-groups in use: 4
Number of aggregators:           4

Group  Port-channel  Protocol    Ports
------+-------------+-----------+-----------------------
   ----------------------
256    Po256(RU)        -        Gi5/9(P)   Gi5/10(P)
```

Reference: Sup32 vs Sup32 PISA Comparison

	Sup32	Sup32 PISA
Hardware architecture	Sup32 Base + MSFC2a	Sup32 Base + PISA
Hardware Features	PFC3B L2-L4 features	PFC3B L2-L4 features
Max Performance	32Gbps / 15Mpps	32Gbps / 15Mpps
DPI in hardware	No	Yes (Multi-gigabit speeds)
RP Control Plane Performance	R7K 300 MHz	Faster RP: BCM1250 750MHz
RP DRAM Memory	512 MB at default (up to 1 GB)	1 GB
RP internal Bootflash / Bootdisk	64 MB default	256 MB (Compact Flash)
Hardware crypto capable	No	Crypto Processor integrated on PISA daughterboard
Linecard support	61xx and 65xx linecards*	61xx and 65xx linecards*

* Check Release Notes for Exact Support

Reference: MSFC2a and PISA Hardware Comparison

	MSFC2a	PISA
RP CPU	R7K 300 MHz	BCM1250 750MHz
RP DRAM (ECC protected)	512 MB (up to 1 GB)	1 GB
RP NVRAM	2 MB	2 MB
RP Bootflash / Bootdisk	64 MB	256 MB (Compact Flash)
RP inband data channel	1 Gbps	1 Gbps
NP	N/A	IXP 2805, 700MHz Xscale, 16*1.4GHz Micro engines
NP DRAM (ECC protected)	N/A	3 * 256 MB
NP SRAM	N/A	4 * 8 MB
Crypto Processor	N/A	Nitrox II (CN2430)
Nitrox DRAM (ECC protected)	N/A	128 MB

Supervisor Chassis Requirements

Supervisor 720 (all variants) and

Supervisor 32 (all variants) require:

- Catalyst 6500 or 6500-E chassis
- High speed fan tray (FAN2/E-FAN)
  - E-Fan cannot be used in non-E Chassis
  - Fan2 cannot be used in E-Series
- 2500W power supply (AC or DC) or greater
  - 3000W supply for new AC deployments since 2500W AC is End-of-Sale
- Specific chassis slots:
  - Slot 1 or 2 in 3/4 slot
  - Slot 5 or 6 in 6/9 slot
  - Slot 7 or 8 in 13 slot

Supervisor 720 Switch Fabric

- 720-Gbps crossbar switch fabric provides
  - Multiple conflict-free paths between switching modules
- Integrated on Supervisor 720 baseboard
- Fabric channels run at up to
  - 20-Gbps full duplex
  - 20-Gbps in/20-Gbps out per channel
- Works with all fabric-capable modules
  - Fabric channels auto-sync speed on per-slot basis (8-Gbps or 20-Gbps)
- Two fabric channels per slot in 6503/6504/6506/6509
- In 6513:
  - One fabric channel slots 1–8
  - Two fabric channels slots 9–13
  - Dual-fabric channel" modules not supported in slots 1–8 of 6513

Monitoring Fabric Status and Utilization

- **Cisco IOS: show fabric [active | channel-counters | errors | fpoe | medusa | status | switching-mode | utilization]**
- **Cisco IOS: show platform hardware capacity fabric**
- **Catalyst OS: show fabric {channel {counters | switchmode | utilization} | status}**

```
6506#show fabric utilization
 slot  channel   speed    Ingress %   Egress %
    1        0      8G           22         23
    2        0      8G            4          9
    3        0     20G            0          1
    3        1     20G           11         12
    4        0     20G            0          1
    4        1     20G           10         13
    6        0     20G            0          1
6506#
```


Monitoring System Bus Utilization

- Monitor the traditional Catalyst 6500 bus when using:
  - Classic modules
  - Centralized forwarding with a fabric

- **Cisco IOS: show catalyst6000 traffic-meter**
- **Cisco IOS: show platform hardware capacity fabric**
- **Catalyst OS: show traffic**

```
6506#show catalyst6000 traffic-meter

  traffic meter =   7%  Never cleared
          peak =  46%       reached at 08:07:50 PST Fri Dec 30 2005
6506#
```

Policy Feature Card 3

- Mandatory daughter card for supervisor engine
- Provides the key components enabling high-performance hardware packet processing
- Supervisor 32 (all variants) supports PFC3B
- Supervisor 720 supports:
  - PFC3A
  - PFC3B
  - PFC3BXL
- Supervisor 720-10G supports:
  - PFC3C
  - PFC3CXL

Policy Feature Card 3 (Cont.)

Key Hardware-Enabled Features:

- Layer 2 switching
- IPv4 and IPv6 unicast forwarding
- IPv4 and IPv6 multicast forwarding
- Security ACLs
- QoS/policing
- NetFlow accounting
- MPLS*/VRF-lite
- Bidir PIM,
- GRE/v6 tunnels,
- CoPP

PFC3C and PFC3CXL Also Support VSS

* MPLS on All but PFC3A VSS Is Covered in RST-3468 Cisco Catalyst Virtual Switch (VSS)

Reference: PFC3 Comparison

Feature	PFC3A	PFC3B / BXL	PFC3C / CXL
FIB TCAM	256K	256K / 1M	256K / 1M
Adjacency Table	1M	1M	1M
NetFlow Table	128K (64K)	128K (115K) / 256K (230K)	128K (115K) / 256K (230K)
MAC Table	64K (32K)	64K (32K)	96K (80K)
IPv6	Hardware	Hardware	Hardware
Bidir PIM	Hardware	Hardware	Hardware
Native MPLS	No (VRF Lite Only)	Yes	Yes
EoMPLS	No	Yes	Yes
NAT, Tunnels	Hardware	Hardware	Hardware
uRPF Check	Yes (Multipath)	Yes (Multipath)	Yes (Multipath)
VSS	No	No	Yes

= Change from Earlier Version

33

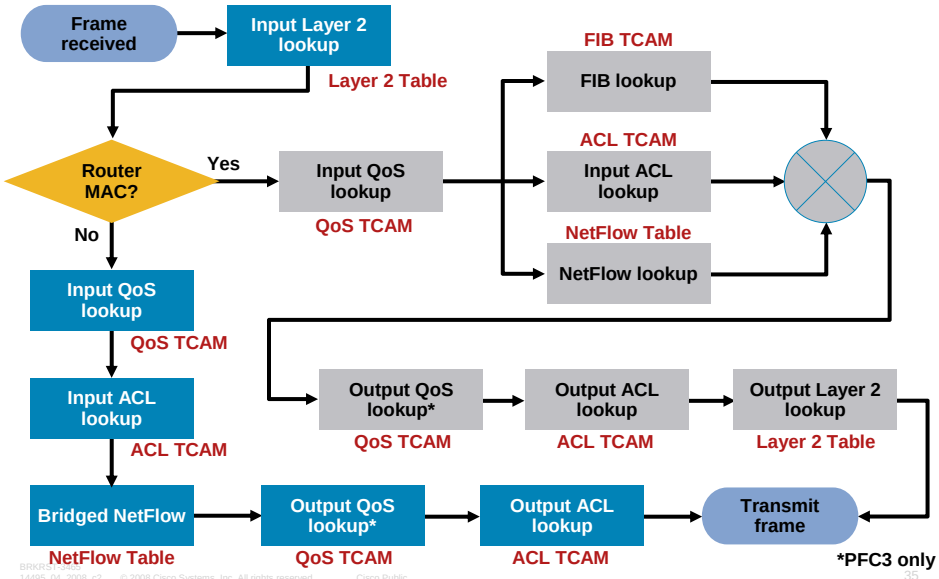
Reference: PFC3 Comparison (Cont.)

Feature	PFC3A	PFC3B / BXL	PFC3C / CXL
ACL TCAM	32K/4K Dual-Bank	32K/4K Dual-Bank	32K/4K Dual-Bank
PACLs	Yes	Yes	Yes
ACL Counters	No	Yes	Yes
QoS TCAM	32K/4K	32K/4K	32K/4K
ACL Labels	512	4K	4K
ACL LOUs	64	64	64
CPU Rate Limiters	8 (L3), 2 (L2)	8 (L3), 2 (L2)	8 (L3), 2 (L2)
CoPP	Yes	Yes	Yes
User-Based Policing	Yes	Yes	Yes
Egress Policing	Yes	Yes	Yes
HSRP/VRRP Groups	Protocol limit	Protocol limit	Protocol limit
Unique MAC/Interface	Yes	Yes	Yes

= Change from Earlier Version

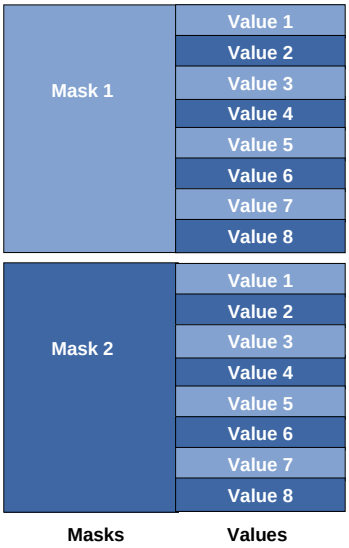
34

High-Level Forwarding Engine Logic

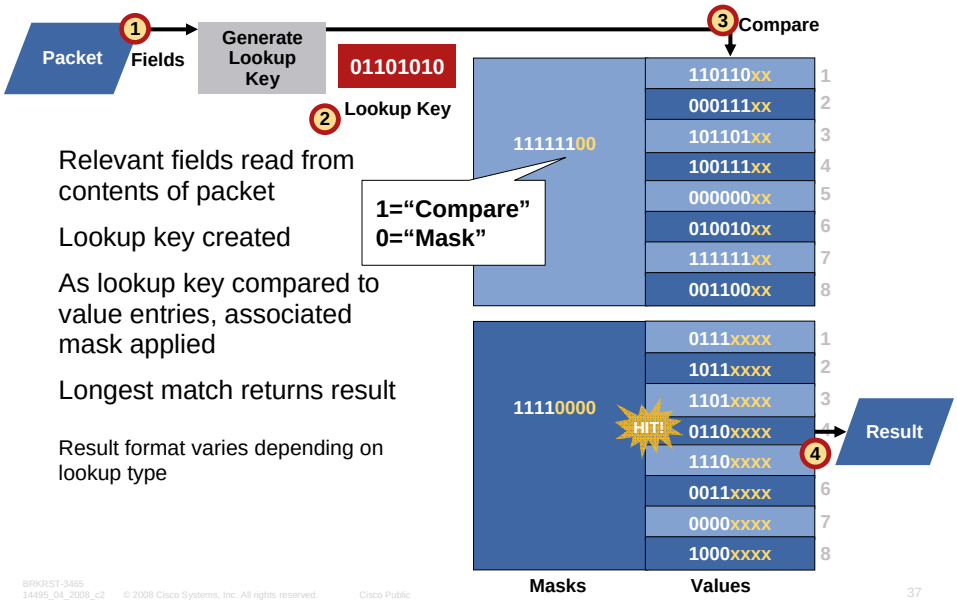


PFC TCAM Technology

- TCAM—Ternary Content Addressable Memory
- Leveraged heavily in Catalyst 6500
  - FIB, ACL, QoS, NetFlow all utilize TCAM memory
- All entries accessed in parallel—fixed performance independent of number of entries
- Memory consists of groups of values and associated masks
  - 8:1 ratio of values to masks
- Masks are used to “wildcard” some portion of values



Generic TCAM Lookup Logic



Relevant fields read from contents of packet

Lookup key created

As lookup key compared to value entries, associated mask applied

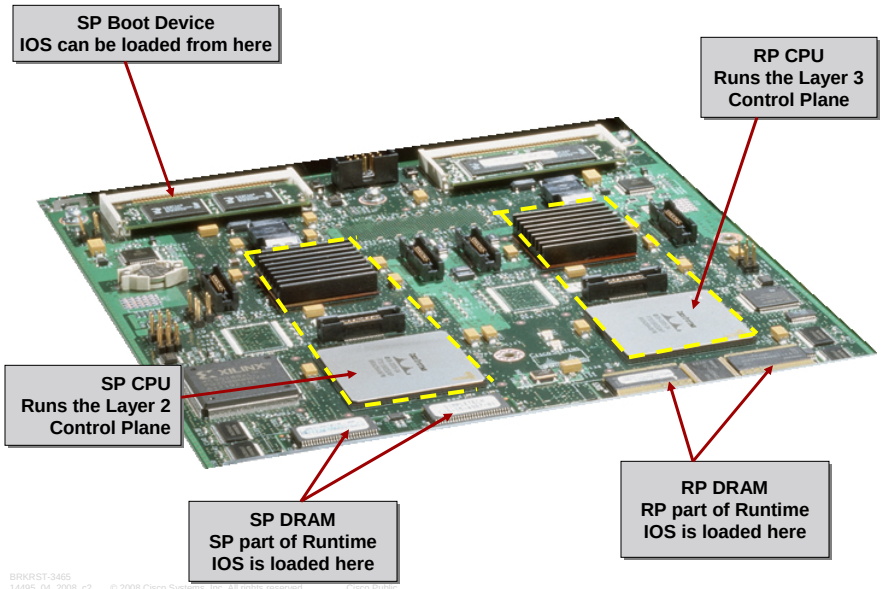
Longest match returns result

Result format varies depending on lookup type

Agenda

- Chassis and Power Supplies
- Supervisor Engine and Switch Fabric Architecture
- Cisco IOS Boot Process
- Module Architecture
- Layer 2 Forwarding
- IPv4 Forwarding
- IPv4 Multicast Forwarding
- Packet Walks

Cisco IOS Supervisor Hardware Components

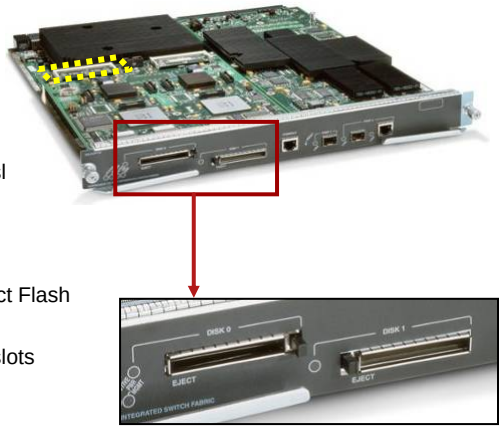


Cisco IOS Image Locations

Depending on which Supervisor you have, there are different options for storage of the Cisco IOS image for booting:

Supervisor 32

- 256MB SP Internal Compact Flash bootdisk
- 512MB SP Internal Compact Flash bootdisk for Sup32-PISA
- 1 Type II External Compact Flash sl



Supervisor 720

- 64MB SP Bootflash –or-
- 512MB or 1GB SP Internal Compact Flash bootdisk
- 2 Type II External Compact Flash slots

Supervisor 720-10G

- 1GB SP Internal Compact Flash bootdisk
- 1 Type II External Compact Flash slot

Supervisor 720 Internal Compact Flash Adapter

An Internal Compact Flash Adapter That Can Take the Place of the 64MB Bootflash on the Supervisor 720…

COMPACT FLASH ADAPTER

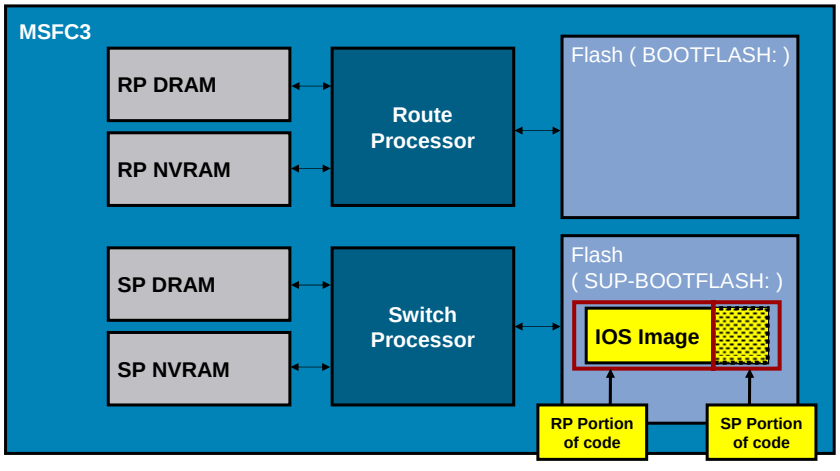
CF Adapter Specifications

- **Part Number WS-CF-UPG= (512MB)**
- **Part Number WS-CF-UPG-1GB= (1GB)**
- **Both supported in Sup720, Sup720-3B, Sup720-3BXL**
- **1GB version supported in Sup720-10G**
- **CF Adapter is NOT OIR capable**
- **Requires IOS 12.2(18)SXE5 and SP ROMMON 8.4(2)**
- **LED located on CF Adapter which will flash green when CF is accessed; designed for use during troubleshooting**

Installation instructions at
http://www.cisco.com/univercd/cc/td/doc/product/lan/cat6000/cfgnotes/78_17277.htm

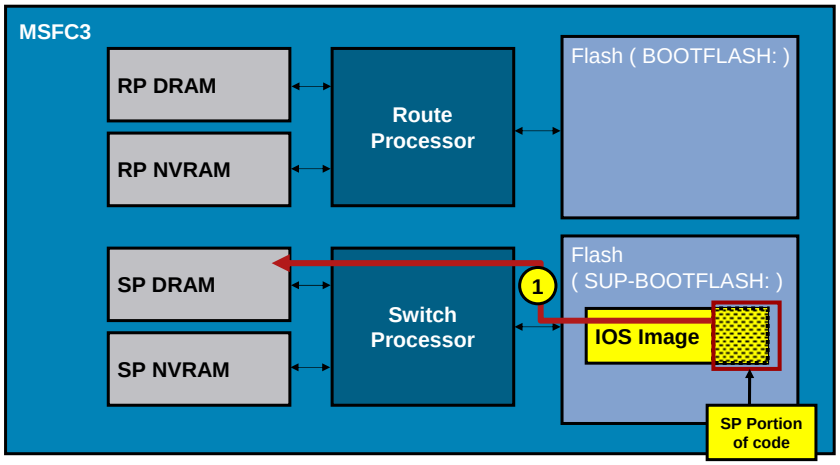
Booting Cisco IOS

The Runtime Image for the Catalyst 6500 Is Delivered as a Single BINARY Image That Is Loaded on the SP Bootflash or Bootdisk



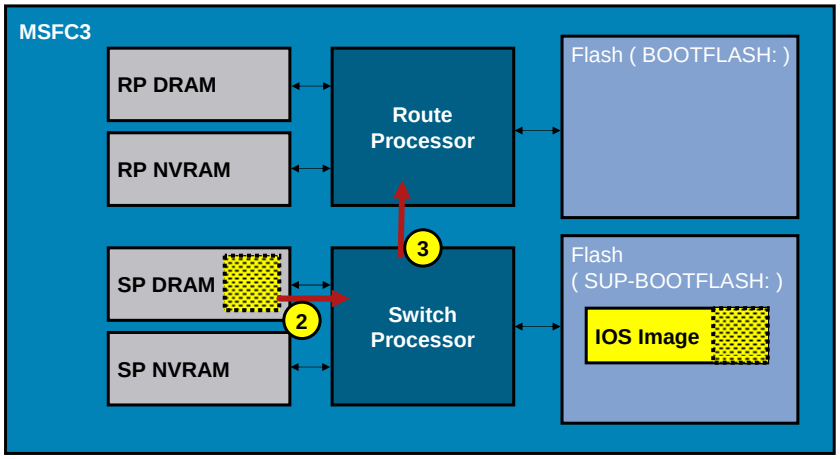
Booting Cisco IOS (Cont.)

The SP Initially Owns the Boot Process—First the SP Portion of the Image Is Decompressed and Loaded into the SP DRAM…



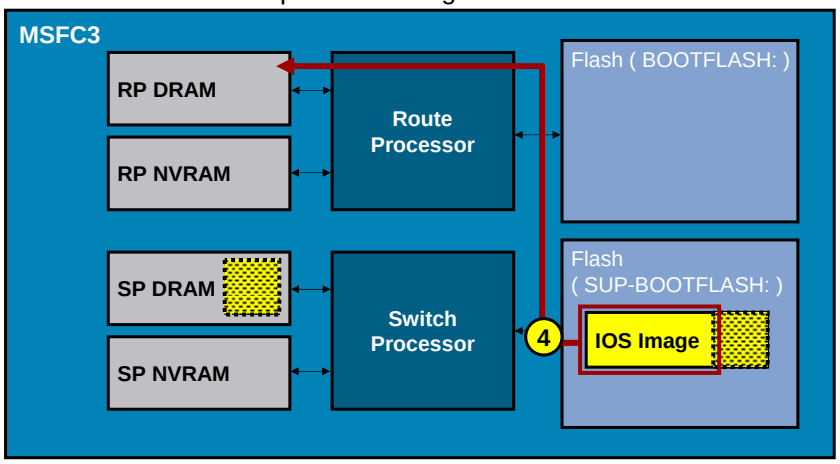
Booting Cisco IOS (Cont.)

The SP Then Begins the Boot Process by Booting from This Image—When It Has Completed Its Boot Process, It Hands over the Console to the RP to Continue the Boot Process



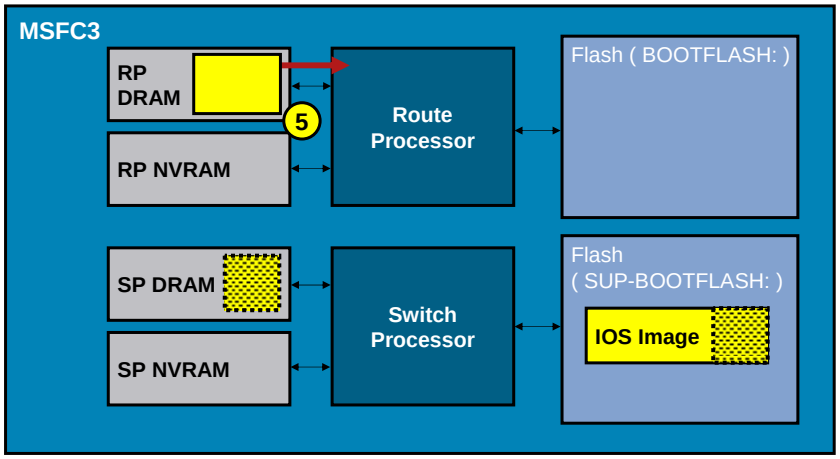
Booting Cisco IOS (Cont.)

The RP Then Downloads the RP Portion of the Cisco IOS Image into RP DRAM—Once It Has Fully Downloaded the Image, the RP Will Then Decompress the Image



Booting Cisco IOS (Cont.)

After Decompressing the Image, the RP Will Boot Using This Image in RP DRAM to Complete the Boot Process—Once Fully Booted, The Console Remains Under Control of the RP



Booting Cisco IOS (Cont.)

```
System Bootstrap, Version 7.7(1)
Copyright (c) 1994-2003 by cisco Systems, Inc.
Cat6k-Sup720/SP processor with 524288 Kbytes of main memory

Autoboot executing command: "boot disk0:s72033-ipservicesk9_wan-vz.122-18.SXF2

Self decompressing the image : ################################################]

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subject to restrictions as set forth in subparagraph
(c) of the Commercial Computer Software - Restricted
Rights clause at FAR sec. 52.227-19 and subparagraph
(c) (1) (ii) of the Rights in Technical Data and Computer
Software clause at DFARS sec. 252.227-7013.

      cisco Systems, Inc.
      170 West Tasman Drive
      San Jose, California 95134-1706

Cisco Internetwork Operating System Software
IOS (tm) s72033_sp Software (s72033_sp-IPSERVICESK9_WAN-VM), Version 12.2(18)SXF2,
RELEASE SOFTWARE (fc1)
TAC Support: http://www.cisco.com/tac
Copyright (c) 1986-2003 by cisco Systems, Inc.
Compiled Tue 27-May-03 20:48 by ccai
Image text-base: 0x40020C10, data-base: 0x40B98000
```

1 SP portion of code is decompressed

2 SP portion of code identified by "SP" keyword in image name

Booting Cisco IOS (Cont.)

3 When the SP has fully booted, the console is handed over to the RP

```
00:00:28: %PFREDUN-6-ACTIVE: Initializing as ACTIVE processor
00:00:28: %OIR-SP-6-CONSOLE: Changing console ownership to route processor
```

4 RP portion of image is loaded into RP DRAM

```
System Bootstrap, Version 12.2(14r)S1, RELEASE SOFTWARE (fc1)
TAC Support: http://www.cisco.com/tac
Copyright (c) 2003 by cisco Systems, Inc.
Cat6k-Sup720/RP platform with 524288 Kbytes of main memory

Download Start
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
Download Completed! Booting the image.
Self decompressing the image : ################################################]
```

5 RP image is booted from RP DRAM

Booting Cisco IOS (Cont.)

```
<SNIP>
Cisco Internetwork Operating System Software
IOS (tm) s72033_rp Software (s72033_rp-IPSERVICESK9_WAN-VM), Version 12.2(18)SXF2,
RELEASE SOFTWARE (fc1)
Technical Support: http://www.cisco.com/techsupport
Copyright (c) 1986-2006 by cisco Systems, Inc.
Compiled Wed 18-Jan-06 21:59 by dchih
Image text-base: 0x01020150, data-base: 0x01021000

cisco WS-C6503 (R7000) processor (revision 1.1) with 491520K/32768K bytes of memory.
Processor board ID FOX063513LV
SR71000 CPU at 600Mhz, Implementation 1284, Rev 1.2, 512KB L2 Cache
Last reset from power-on
Bridging software.
X.25 software, Version 3.0.0.
SuperLAT software (copyright 1990 by Meridian Technology Corp).
TN3270 Emulation software.
1 Virtual Ethernet/IEEE 802.3 interface
48 FastEthernet/IEEE 802.3 interfaces
4 Gigabit Ethernet/IEEE 802.3 interfaces
1917K bytes of non-volatile configuration memory.

65536K bytes of Flash internal SIMM (Sector size 512K).

Press RETURN to get started!

6500>
```

RP image is now active

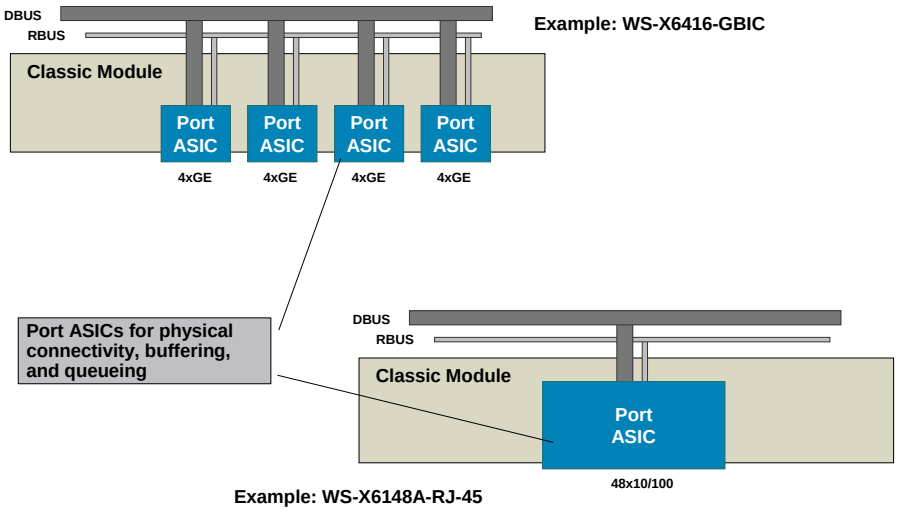
6

Image boots up and console user presented with CLI prompt

Agenda

- Chassis and Power Supplies
- Supervisor Engine and Switch Fabric Architecture
- Cisco IOS Boot Process
- Module Architecture
- Layer 2 Forwarding
- IPv4 Forwarding
- IPv4 Multicast Forwarding
- Packet Walks

Classic Module



Reference: Classic Module Family

Copper 10/100 and 10/100/1000:
- WS-X6148A-GE-TX
- WS-X6148A-GE-45AF
- WS-X6148-GE-TX
- WS-X6148V-GE-TX
- WS-X6148-GE-45AF
- WS-X6148-RJ-21
- WS-X6148-RJ21V
- WS-X6148-RJ-45V
- WS-X6148A-RJ-45
- WS-X6148A-45AF
- WS-X6148X2-RJ-45
- WS-X6148X2-45AF
- WS-X6148-RJ-45
- WS-X6148-21AF
- WS-X6148-45AF
- WS-X6196-RJ-21
- WS-X6196-21AF
- WS-X6248A-TEL
- WS-X6248-TEL
- WS-X6248-RJ-45
- WS-X6316-GE-TX
- WS-X6348-RJ-45
- WS-X6348-RJ21V
- WS-X6348-RJ-45V

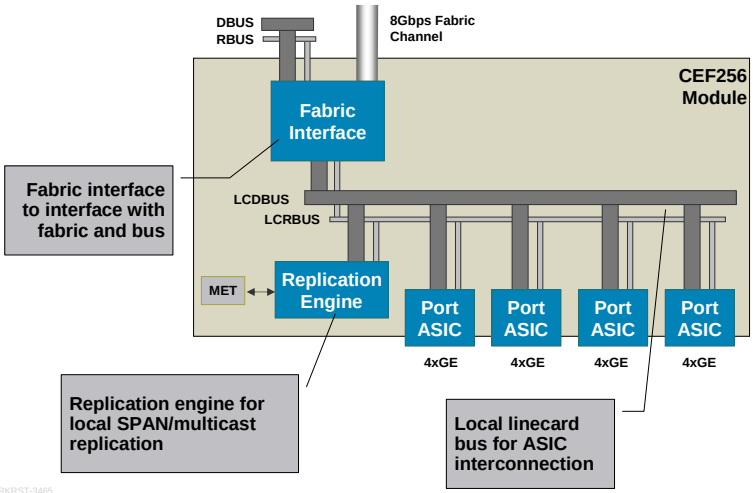
Fiber 10, 100, and GE:
- WS-X6024-10FL-MT
- WS-X6148-FE-SFP
- WS-X6224-100FX-MT
- WS-X6324-100FX-SM
- WS-X6324-100FX-MM
- WS-X6408-GBIC
- WS-X6408A-GBIC
- WS-X6416-GBIC
- WS-X6416-GE-MT

WAN:
- WS-X6182-2PA

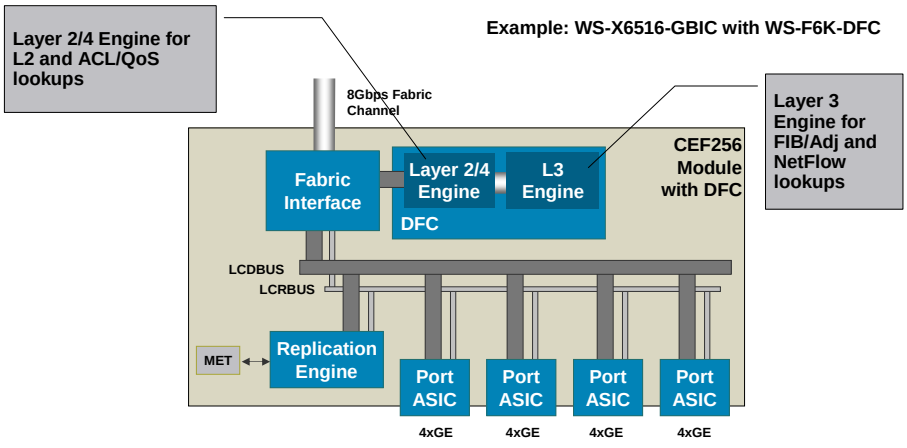
Service Modules:
- WS-X6380-NAM
- WS-X6381-IDS3
- WS-X6066-SLB-APC9
- WS-X6066-SLB-S-K9
- WS-X6624-FXS
- WS-X6608-E1
- WS-X6608-T1

CEF256 Module

Example: WS-X6516-GBIC



CEF256 Module with DFC



Reference: CEF256 Module Family

10GE:
- WS-X6502-10GE*
- Copper 10/100 and 10/100/1000:
- WS-X6548-RJ-21*
- WS-X6548-RJ-45*
- WS-X6548-GE-TX
- WS-X6548V-GE-TX
- WS-X6548-GE-45AF
- WS-X6516-GE-TX

Fiber 100 and GE:
- WS-X6524-100FX-MM*
- WS-X6516-GBIC*
- WS-X6516A-GBIC*
- WS-X6816-GBIC (dCEF256)**

DFCs:
- WS-F6K-DFC
- WS-F6K-DFC3A
- WS-F6K-DFC3B
- WS-F6K-DFC3BXL

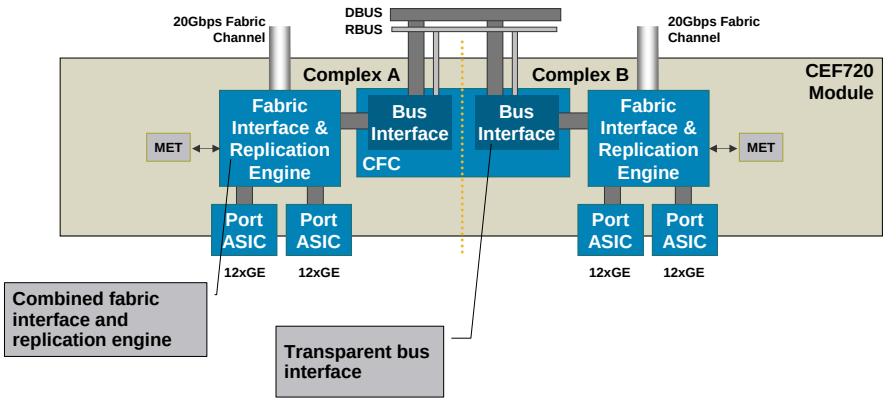
WAN:
- WS-X6582-2PA

Service Modules:
- WS-SVC-NAM-1
- WS-SVC-NAM-2
- WS-SVC-IDSM2-BUN-K9
- WS-SVC-FWM-1-K9
- WS-SVC-SSL-1
- WS-SVC-CSG-1
- WS-SVC-CMM
- WS-SVC-AON-1-K9
- WS-SVC-ADM-1-K9,
- WS-SVC-AGM-1-K9
- WS-SVC-CSG-1
- WS-SVC-IPSEC-1
- WS-SVC-MWAM-1
- WS-SVC-PSD-1
- WS-SVC-WLAN-1-K9

* Supports Optional DFC/DFC3, ** Requires DFC/DFC3

CEF720 Module

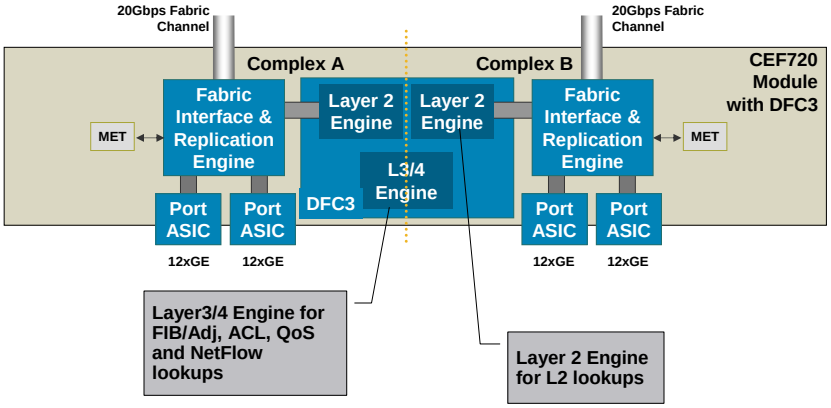
Example: WS-X6748-SFP



Bus interface for control information only!!

CEF720 Module with DFC3

Example: WS-X6748-SFP with WS-F6700-DFC3B



Reference: CEF720 Module Family

10GE:

- WS-X6704-10GE*
- WS-X6708-10G**
- WS-X6716-10G**

Copper 10/100/1000:

- WS-X6748-GE-TX*

Fiber GE:

- WS-X6724-SFP*
- WS-X6748-SFP*

Service Modules:

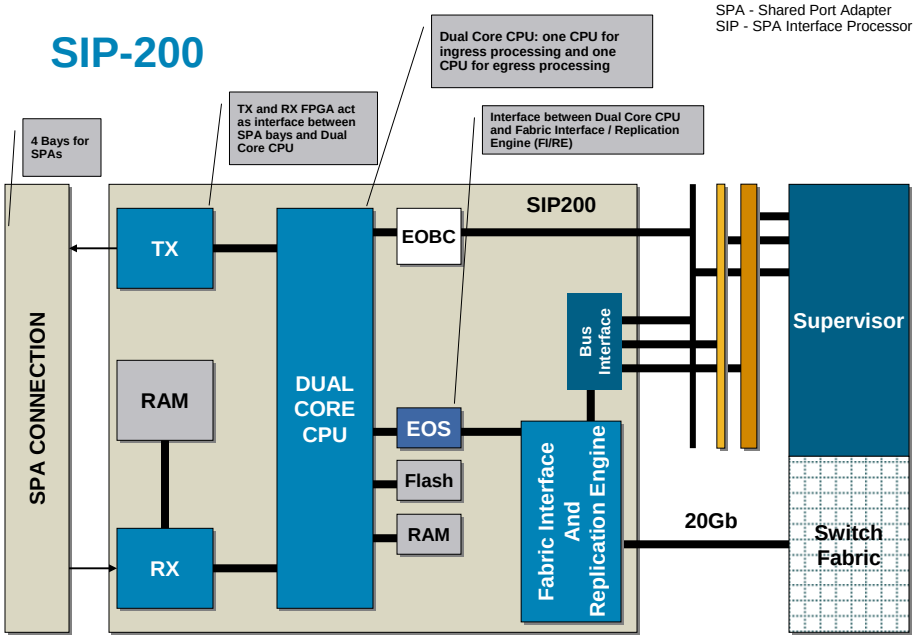
- WS-SVC-WiSM-1-K9

DFCs:

- WS-X6700-CFC (Centralized Forwarding Card)
- WS-F6700-DFC3A
- WS-F6700-DFC3B
- WS-F6700-DFC3BXL
- WS-F6700-DFC3C
- WS-F6700-DFC3CXL

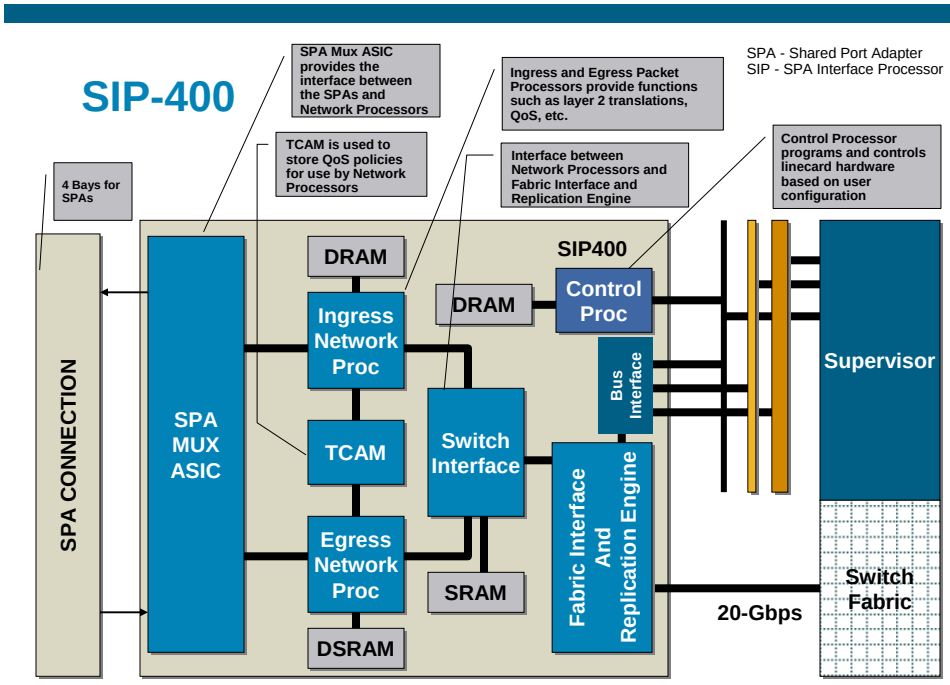
*Supports Optional DFC3
** Requires DFC3

SIP-200



Reference: SPAs for SIP-200

SPA Name	Description	Height
SPA-CH8TE1	8- port Channelized T1/E1 SPA	Single height
SPA-4XT3/E3	4-port T3/E3 SPA	Single height
SPA-2XT3/E3	2-port T3/E3 SPA	Single height
SPA-4XCT3/DS0	4- port Channelized T3 SPA	Single height
SPA-2XCT3/DS0	2- port Channelized T3 SPA	Single height
SPA-4XOC3-POS	4- port POS OC3 SPA	Single height
SPA-2XOC3-POS	2- port POS OC3 SPA	Single height
SPA-4XOC3-ATM	4- port ATM OC3 SPA	Double height
SPA-2XOC3-ATM	2- port ATM OC3 SPA	Double height



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Reference: SPAs for SIP-400

SPA	Ports	Interface	Form Factor
OC-3/STM-1 POS	2, 4	SFP	Single Height
OC-12/STM-4 POS	1, 2, 8	SFP	Single Height
OC-3/STM-1 ATM	2, 4	SFP	Double Height
OC12/STM-4 ATM	1	SFP	Double Height
OC48/STM-16 POS/RPR	2, 4	SFP	Single Height
OC48/STM-16 ATM	1	SFP	Double Height
T3/E3 ATM	2, 4	Copper	Single Height
Channelized T1/E1	8	Copper	Single Height
Clear Channel T3/E3	2, 4	Copper	Single Height
Channelized T3	2, 4	Copper	Single Height
Channelized OC-3/STM-1	1	SFP	Single Height
FE	4, 8	TX, FX	Single Height
GE	1, 2	SFP	Single Height

ATM SPAs are not supported in 12.2(33)SXH releases.

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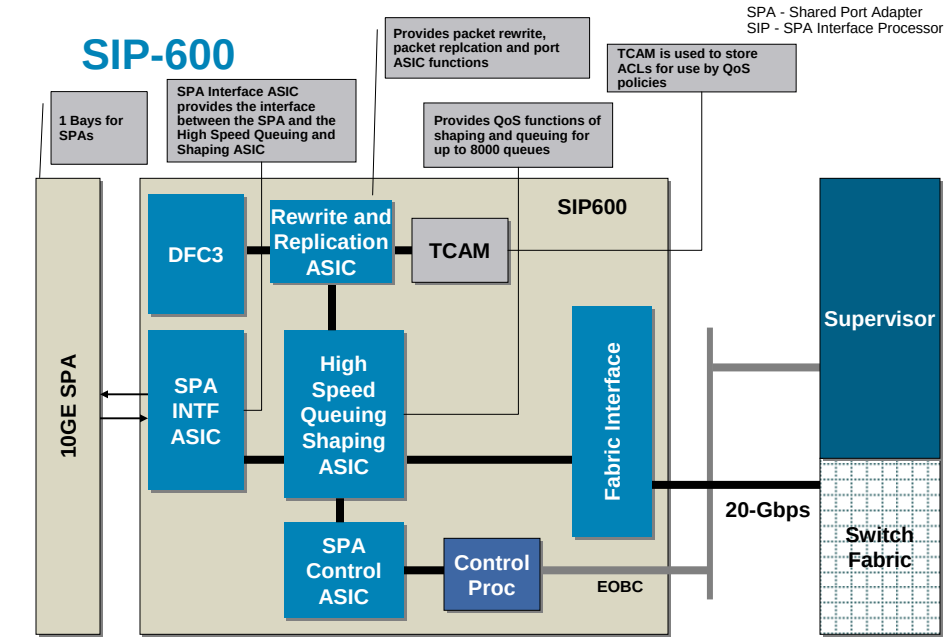


Reference: SPAs for SIP-600

SPA	Ports	Interface	Form Factor
PA-1XTENGE-XFP	1	XFP	Single Height Dual Width
SPA-10X1GE	10	SFP	Double Height
SPA-5X1GE	5	SFP	Single Height
SPA-OC192POS-VSR	1	Fixed	Double Height
SPA-OC192POS-LR	1	Fixed	Double Height
SPA-OC192POS-XFP	1	XFP	Single Height

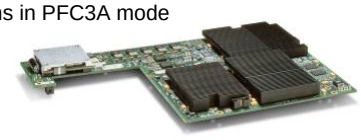
SIP-600 is not supported in 12.2(33)SXH releases.

Distributed Forwarding

- One or more modules have a local forwarding engine (DFC—Distributed Forwarding Card)
- Central engine and distributed engines perform different lookups independently and simultaneously
- Implementation is fully distributed
  - All hardware from PFC is present on the DFC
  - Full Layer 2, Layer 3, ACL/QoS information downloaded from Supervisor
  - Ingress DFC performs all lookups locally
- Deterministic, highly scalable—Not flow-based
- NOT just for local switching—destination interface irrelevant
- DFCs always require Cisco IOS software on both the SP and the RP

Distributed Forwarding Cards

- PFC "major" module version must be identical
  - PFC/DFC "minor" module version mismatch supported in lowest common denominator mode
  - Example: System with PFC3B and DFC3As runs in PFC3A mode
- DFC3 is an optional daughter card for CEF256/CEF720 modules
  - Several flavors and form factors available
- WS-X6816-GBIC module REQUIRES either DFC or DFC3
- WS-X6708-10G and WS-X6716-10G modules REQUIRE either DFC3C or DFC3CXL
- Local CPU for managing hardware tables
- No DFC3C/3CXL for 65xx or 6816
- Use remote login module command to access the DFC console
  - Commands available on DFC console for troubleshooting use, under direction from Cisco TAC/escalation



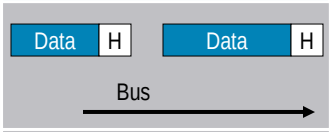
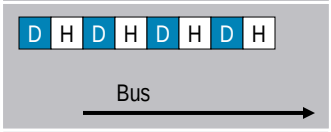
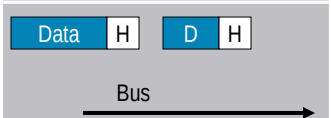
DFC3x and PFC3x Interoperability

The use of a DFC3 requires it to operate with the equivalent PFC3 version —a mix of PFC3 and DFC3 versions will result in the system operating at the lowest common denominator

	PFC3A	PFC3B	PFC3BXL	PFC3C	PFC3CXL
DFC3A		Operate as PFC3A	Operate as PFC3A	Operate as PFC3A	Operate as PFC3A
DFC3B	Operate as DFC3A		Operate as PFC3B	Operate as PFC3B	Operate as PFC3B
DFC3BXL	Operate as DFC3A	Operate as DFC3B		Operate as PFC3B and DFC3B	Operate as PFC3BXL
DFC3C	Operate as DFC3A	Operate as DFC3B	Operate as PFC3B and DFC3B		Operate as PFC3C
DFC3CXL	Operate as DFC3A	Operate as DFC3B	Operate as DFC3BXL	Operate as DFC3C	

Mixing Different Linecard Architectures

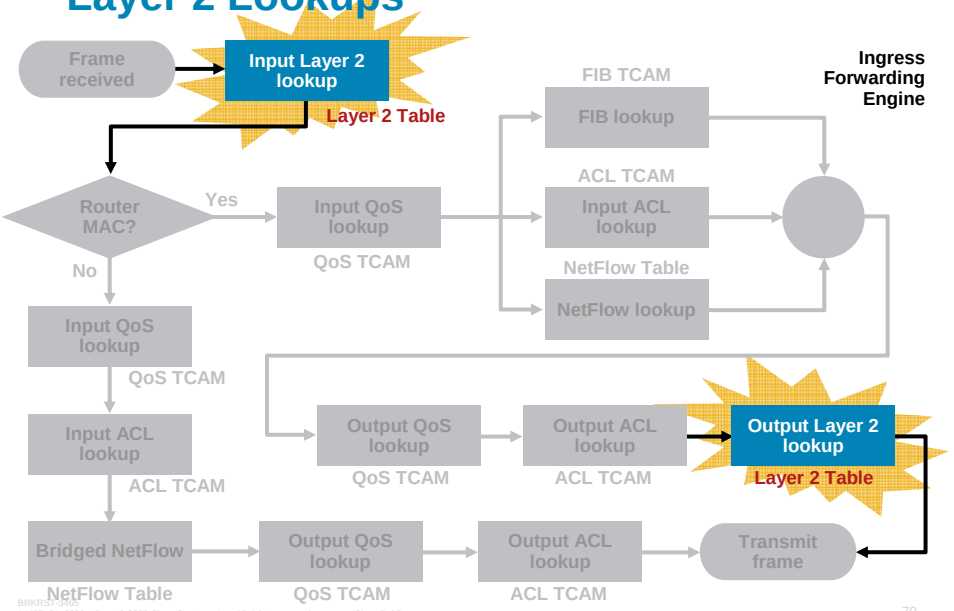
When utilizing Centralized Forwarding, the backplane will operate in one of three modes—these modes are determined by the combination of linecards installed in the chassis and from which module the traffic sourced and to which module the traffic is destined

Mode	Description	Illustration
FLOW THROUGH	▪ Between non fabric modules and between a non fabric and a fabric enabled linecard ▪ Throughput – 15 Mpps (@ 64 byte frames) ▪ Bandwidth – 16 Gbps of bandwidth shared throughout ▪ Data Bus frame size is variable; min of 4 cycles (64B Data) on the DBus for every frame +1 wait cycle	
COMPACT	▪ When only ALL fabric enabled linecards in a chassis ▪ Throughput – 30 Mpps (@ any frame size) ▪ Bandwidth – 8 G CEF256; 20 G/channel CEF720 ▪ Data Bus frame size is constant (compact header); 2 cycles (32 B Data) on the DBus for every frame + no wait cycle	
TRUNCATED	▪ Between fabric linecards when a non fabric linecard is in the chassis. ▪ Throughput – 15 Mpps (@ 64 byte frames); independent of frame size for CEF256 and CEF720 ▪ Bandwidth – 16 G shared for classic; 8 G per CEF256; 20 G/channel CEF720. ▪ Data Bus frame size is variable; min of 4 cycles (64 Bytes Data) on the Data Bus for every frame.	

Agenda

- Chassis and Power Supplies
- Supervisor Engine and Switch Fabric Architecture
- Cisco IOS Boot Process
- Module Architecture
- Layer 2 Forwarding
- IPv4 Forwarding
- IPv4 Multicast Forwarding
- Packet Walks

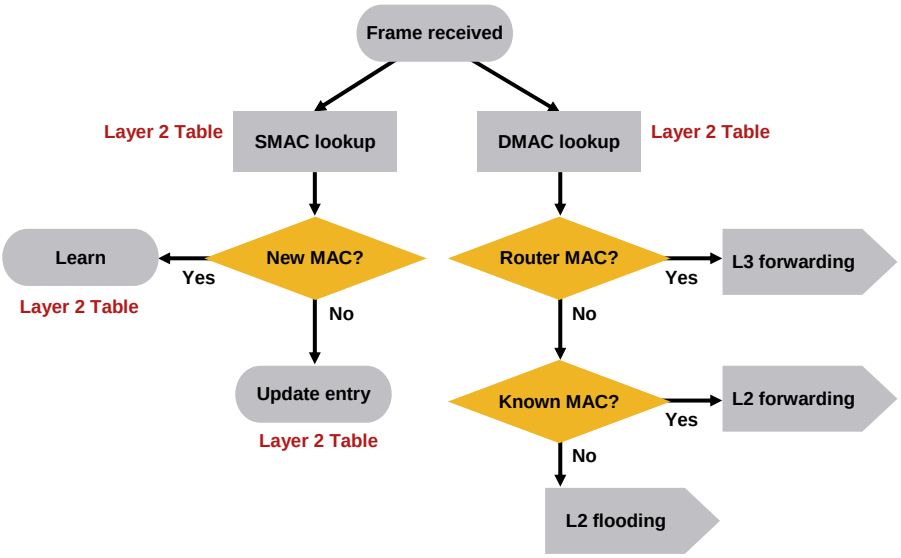
Layer 2 Lookups



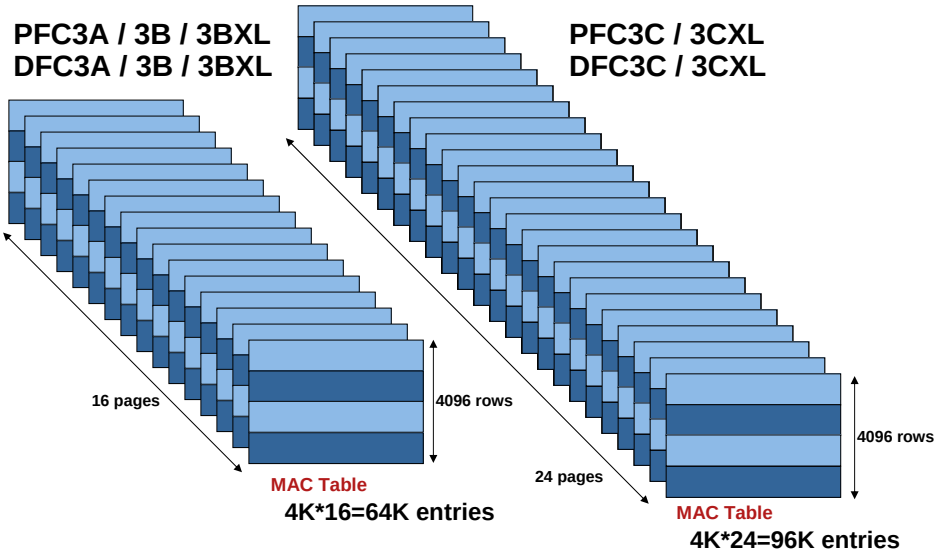
Layer 2 Forwarding

- Layer 2 forwarding is based on {VLAN, MAC} pairs
  - Same MAC can be learned in multiple VLANs
- MAC learning is fully hardware based
  - CPU not involved in learning
- PFC and DFCs have copies of the MAC table
  - Refreshing of entries based on “seeing” traffic—forwarding engines age entries independently
  - New learns on one forwarding engine communicated to other engines
- MAC table size:
  - 64K entries on PFC3A/3B/3BXL and DFC3A/3B/3BXL (32K effective)
  - 96K entries on PFC3C/3CXL and DFC3C/3CXL (80K effective)

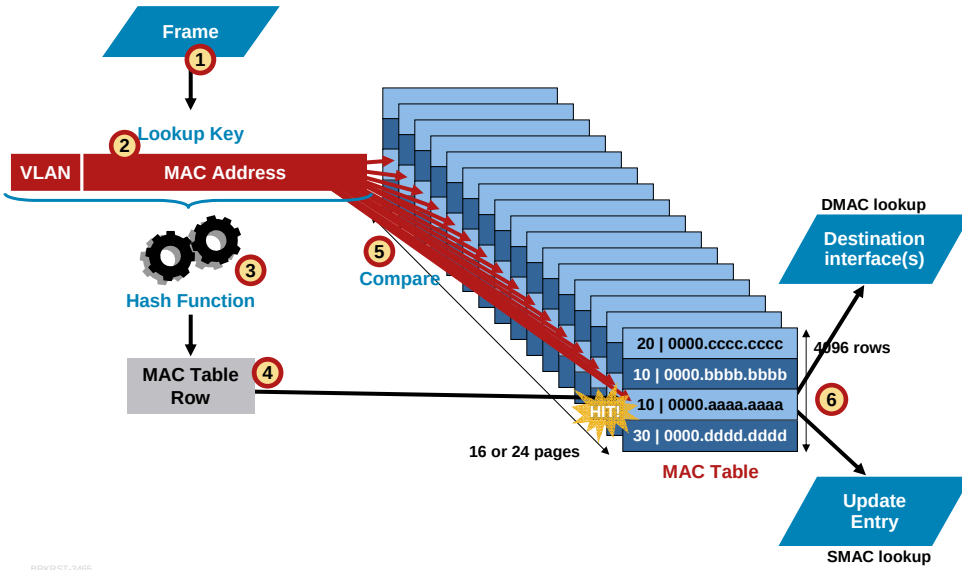
Layer 2 Forwarding Logic



Layer 2 Forwarding Table Design



PFC3 Layer 2 Lookup



Reference: PFC3 Layer 2 Lookup Process

Source and Destination Lookups Occur in Parallel

1. Frame received by forwarding engine
2. Lookup key generated by extracting VLAN and MAC from received frame
3. VLAN and MAC input to hash function
4. Hash result identifies row in MAC table
5. Lookup key (VLAN and MAC) compared to contents of indexed row on all pages simultaneously
6. Destination lookup: Match returns destination interface(s), miss results in flood

   Source lookup: Match updates age of matching entry, miss installs new entry in table

Displaying the Layer 2 Table

- Cisco IOS: show mac-address-table
- Catalyst OS: show cam

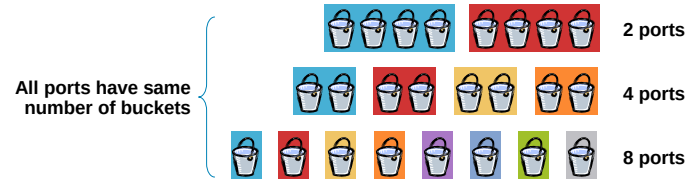
```
6509#show mac-address-table dynamic vlan 30
  Codes: * - primary entry

    vlan   mac address     type    learn qos            ports
  ------+---------------+--------+-----+---+---------------------
--*   30  0003.a088.c408   dynamic  Yes   --           Fa3/18
  *    30  0012.d949.04d2   dynamic  Yes   --           Gi5/1
  *    30  0003.a08a.15f3   dynamic  Yes   --           Fa3/24
  *    30  0090.a400.1850   dynamic  Yes   --           Fa3/14
  *    30  0003.a08a.15f9   dynamic  Yes   --           Fa3/25
  <…>
  6509#
```

EtherChannel Load Sharing

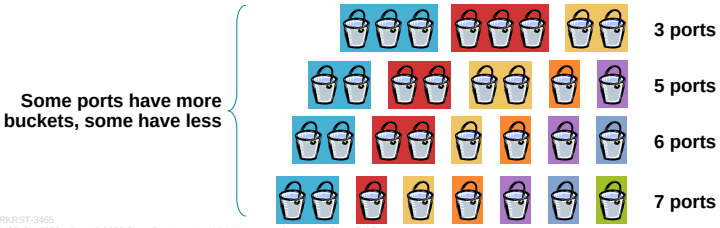
- Joins multiple physical interfaces into a single logical interface
  - Traffic destined for logical interface distributed across physical members
  - Up to eight member ports supported
  - Member ports can be spread over multiple modules
- EtherChannel load-sharing is deterministic
  - Based on hash algorithm
  - Given same hash input, same member port always selected
- Load-sharing method is configurable
  - Configured mode varies which values taken as input to hash
- Per-packet load sharing is **not** supported
- EtherChannel can be:
  - Layer 2—Configured as switchport (or trunk)
  - Layer 3—Configured as routed interface

EtherChannel "Power-of-2" Member Ports

- EtherChannel has 8 "buckets" to distribute among member ports
- Even bucket distribution with 2, 4, or 8 member ports



- Uneven bucket distribution with 3, 5, 6, or 7 member ports



Checking EtherChannel Bucket Distribution

```
6513#show interfaces port-channel 1 etherchannel
   Age of the Port-channel   = 00d:00h:08m:58s
   Logical slot/port   = 14/3            Number of ports = 2
   GC                  = 0x00010001      HotStandBy port = null
   Passive port list   = Gi9/1 Gi9/3
   Port state          = Port-channel L3-Ag Ag-Inuse

   Ports in the Port-channel:

   Index   Load   Port    EC state
   ------+------+------+------------
       0     55     Gi9/1    on
       1     AA     Gi9/3    on3
```

Reference: EtherChannel Inputs

Etherchannel Uses a Load Balancing Algorithm to Determine Which Link in the Bundle to Use—the Inputs to the Algorithm Are a Combination of L2, L3 or L4 Addresses

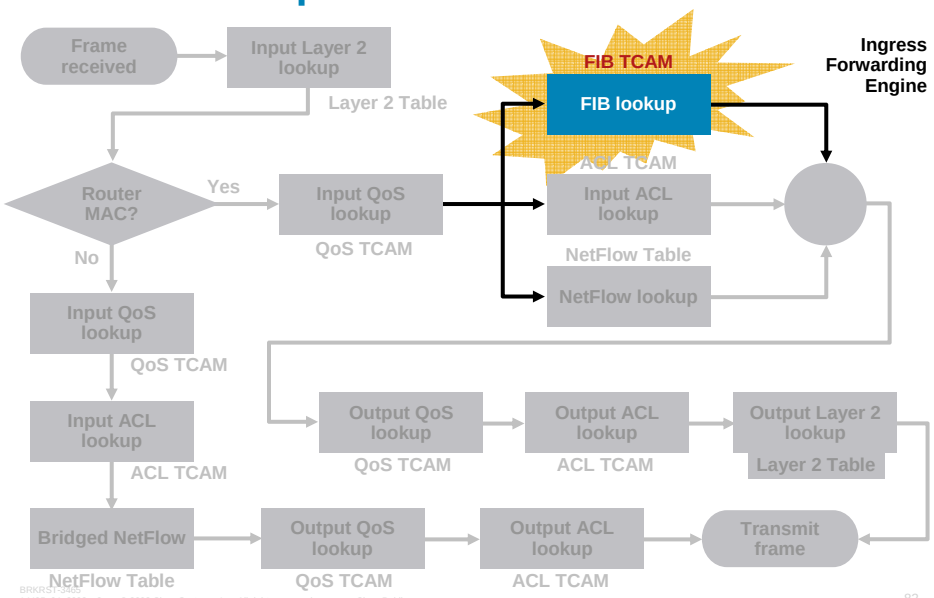
dst-ip	Destination IP Address
dst-mac	Destination Mac Address
dst-mixed-ip-port	Destination IP Address and TCP / UDP Port *
dst-port	Destination TCP/UDP Port
mpls	Load Balancing for MPLS packets
src-dst-ip	Source XOR Destination IP Address
src-dst-mac	Source XOR Destination Mac Address
src-dst-mixed-ip-port	Source XOR Destination IP Address abd TCP / UDP Port *
src-dst-port	Source-Destination TCP/UDP Port
src-ip	Source IP Address
src-mac	Source Mac Address
src-mixed-ip-port	Source IP Addrees and TCP / UDP Port *
src-port	Source TCP/UDP Port

* Requires 12.2(33)SXH or newer and PFC3 (any version)

Agenda

- Chassis and Power Supplies
- Supervisor Engine and Switch Fabric Architecture
- IOS Boot Process
- Module Architecture
- Layer 2 Forwarding
- IPv4 Forwarding
- IPv4 Multicast Forwarding
- Packet Walks

IPv4 Lookups



Hardware-Based CEF

- Catalyst 6500 leverages existing software Cisco Express Forwarding (CEF) model
- Supervisor 32, Supervisor 720 and Supervisor 720-10G extend CEF to hardware
- What is CEF, in a nutshell?
  - Boil down the routing table = FIB table (IP Prefixes)
  - Boil down the ARP table = adjacency table (Next-hop Information)
- Decouples control plane and data plane
  - Forwarding tables built on control plane (MSFC3)
  - Tables downloaded to hardware for data plane forwarding (PFC3 / DFC3)
- CEF process:
  - FIB lookup based on destination prefix (longest-match)
  - FIB "hit" returns adjacency, adjacency contains rewrite information (next-hop)
  - ACL, QoS, and NetFlow lookups occur in parallel and affect final result

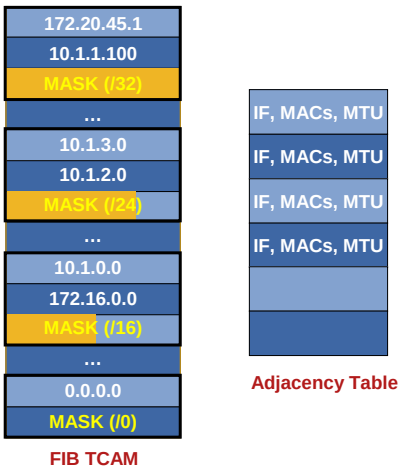
FIB TCAM and Adjacency Entries

FIB:

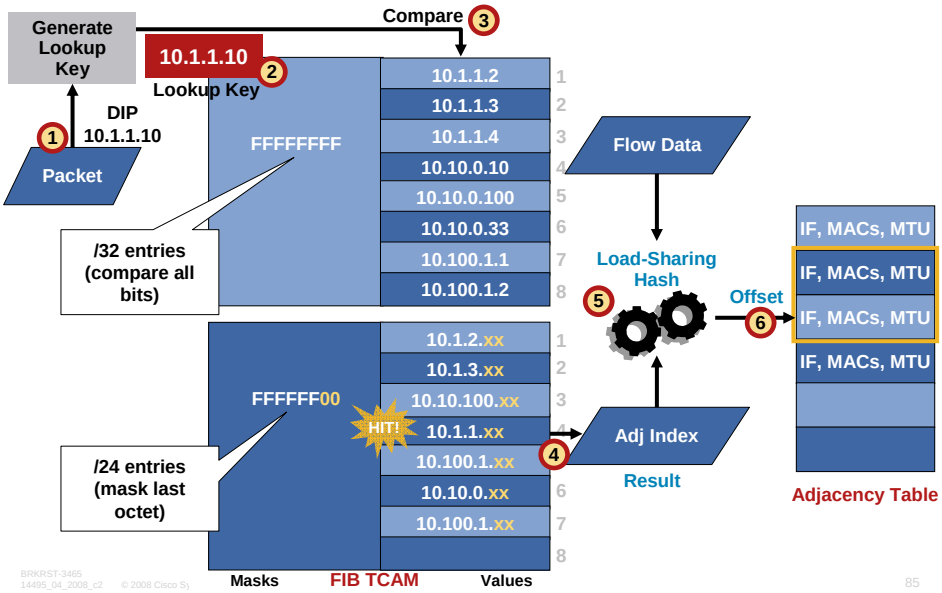
- IPv4 entries logically arranged from most to least specific
- 0/0 default entry terminates unicast FIB entries
- Overall FIB hardware shared by
  - IPv4 unicast
  - IPv4 multicast
  - IPv6 unicast
  - IPv6 multicast
  - MPLS

Adjacency Table:

- Hardware adjacency table also shared among protocols
- Actual adjacency table entries are not shared



IPv4 FIB TCAM Lookup



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14495_04_2008_c2 © 2008 Cisco Sy 85

Reference: IPv4 FIB TCAM Lookup Process

1. Destination IP read from packet
2. Lookup key created based on destination IP
3. As lookup key compared to TCAM entries, associated mask applied
4. Longest match returns index to adjacency block and number of adjacencies in load-sharing block
5. Packet flow data input to load-sharing hash function
6. Hash result returns adjacency offset value, selecting an adjacency entry (containing next-hop information) in the indexed adjacency block

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Supervisor FIB TCAM Resources

- IPv6 and IPv4 multicast require two entries
  - MPLS and IPv4 only one
- PFC3BXL/3CXL = 1M entries
- PFC3A/3B/3C = 256K entries
- By default TCAM is allocated as seen in the table

	PFC3A / 3B / 3C	PFC3BXL / 3CXL
IPv4, MPLS	192k	512k
IPv6, Multicast	32k	256k

SUP720-3BXL Example

```
engine#sh mls cef maximum-routes
FIB TCAM maximum routes :
========================
Current :-
-------
 IPv4 + MPLS     - 512k (default)
 IPv6 + IP Multicast - 256k (default)
```

Changing default (requires Reboot!)

```
engine(config)#mls cef maximum-routes ?
 ip      number of ip routes
 ip-multicast number of multicast routes
 ipv6     number of ipv6 routes
 mpls     number of MPLS labels
```


Displaying IPv4 Forwarding Summary Information

- Cisco IOS:
  - show mls cef summary
  - show mls cef statistics
  - show mls statistics
  - show mls cef hardware
  - show platform hardware capacity forwarding
- Catalyst OS:
  - show mls cef
  - show mls

```
6509-neb#show mls cef summary
Total routes:                   8309
    IPv4 unicast routes:        5948
    IPv4 Multicast routes:      2359
    MPLS routes:                0
    IPv6 unicast routes:        0
    IPv6 multicast routes:      0
    EoM routes:                 0

6509-neb#
```

Displaying Hardware IPv4 Prefix Entries

```
6509-neb#show mls cef
Codes: decap - Decapsulation, + - Push Label
Index   Prefix                Adjacency
64      127.0.0.51/32         receive
65      127.0.0.0/32          receive
66      127.255.255.255/32    receive
67      0.0.0.0/32            receive
68      255.255.255.255/32    receive
75      10.10.1.1/32          receive
76      10.10.1.0/32          receive
77      10.10.1.255/32        receive
78      10.10.1.2/32          Gi1/1,          0030.f272.31fe
3200    224.0.0.0/24          receive
3201    10.10.1.0/24          glean
3202    10.100.0.0/24         Gi1/1,          0030.f272.31fe
3203    10.100.1.0/24         Gi1/1,          0030.f272.31fe
3204    10.100.2.0/24         Gi1/1,          0030.f272.31fe
3205    10.100.3.0/24         Gi1/1,          0030.f272.31fe
<…>
```

- Cisco IOS:
  `show mls cef`
- Catalyst OS:
  `show mls entry cef ip`

Displaying Detailed Hardware Entries

- Cisco IOS:
  `show mls cef <prefix> [detail]`
  `show mls cef adjacency [entry <entry> [detail]]`
- Catalyst OS:
  `show mls entry cef ip <prefix/mask> [adjacency]`

```
6509-neb#show mls cef 10.100.20.0 detail
<…>
M(3222  ): E | 1 FFF 0 0 0 0  255.255.255.0
V(3222  ): 8 | 1 0  0 0 0 0  10.100.20.0    (A:98304 ,P:1,D:0,m:0 ,B:0 )

6509-neb#show mls cef adjacency entry 98304
Index: 98304  smac: 000f.2340.5dc0, dmac: 0030.f272.31fe
        mtu: 1518, vlan: 1019, dindex: 0x0, l3rw_vld: 1
       packets: 4203, bytes: 268992
6509-neb#
```

Finding the Longest-Match Prefix Entry

- Cisco IOS: `show mls cef lookup <ip_address> [detail]`

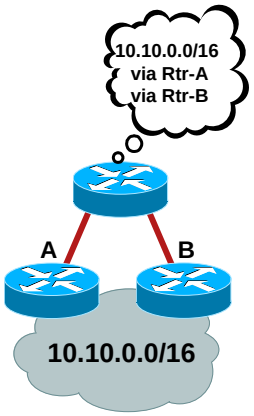
```
6509-neb#show mls cef 10.101.1.0

Codes: decap - Decapsulation, + - Push Label
Index  Prefix              Adjacency
6509-neb#show mls cef lookup 10.101.1.0

Codes: decap - Decapsulation, + - Push Label
Index  Prefix              Adjacency
3203   10.101.0.0/16       Gi2/12,         0007.b30a.8bfc
6509-neb#
```

IPv4 CEF Load Sharing

- Up to 16* hardware load-sharing paths per prefix
- Use **`maximum-paths`** command in routing protocols to control number of load-sharing paths
- IPv4 CEF load-sharing is per-IP flow
- Per-packet load-balancing not supported
- Load-sharing based on Source and Destination IP addresses by default
  - "Unique ID" in PFC3 prevents polarization
- Configuration option supports inclusion of L4 ports in the hash
  - `mls ip cef load-sharing full`
- Unique ID not included in hash in "full" mode



*Starting with 12.2(33)sxh. Prior to 12.2(33)SXH the Maximum Is 8.

Load-Sharing Prefix Entry Example

- show mls cef
- show mls cef lookup

```
6509-neb#show mls cef lookup 10.100.20.1

Codes: decap - Decapsulation, + - Push Label
Index  Prefix              Adjacency
3222   10.100.20.0/24      Gi1/1,            0030.f272.31fe
                           Gi1/2,            0008.7ca8.484c
                           Gi2/1,            000e.382d.0b90
                           Gi2/2,            000d.6550.a8ea

6509-neb#
```


Identifying the Load-Sharing Path

show mls cef exact-route

```
6509-neb#show mls cef exact-route 10.77.17.8 10.100.20.199

Interface: Gi1/1, Next Hop: 10.10.1.2, Vlan: 1019, Destination Mac: 0030.f272.31fe

6509-neb#show mls cef exact-route 10.44.91.111 10.100.20.199

Interface: Gi2/2, Next Hop: 10.40.1.2, Vlan: 1018, Destination Mac: 000d.6550.a8ea

6509-neb#
```

Agenda

- Chassis and Power Supplies
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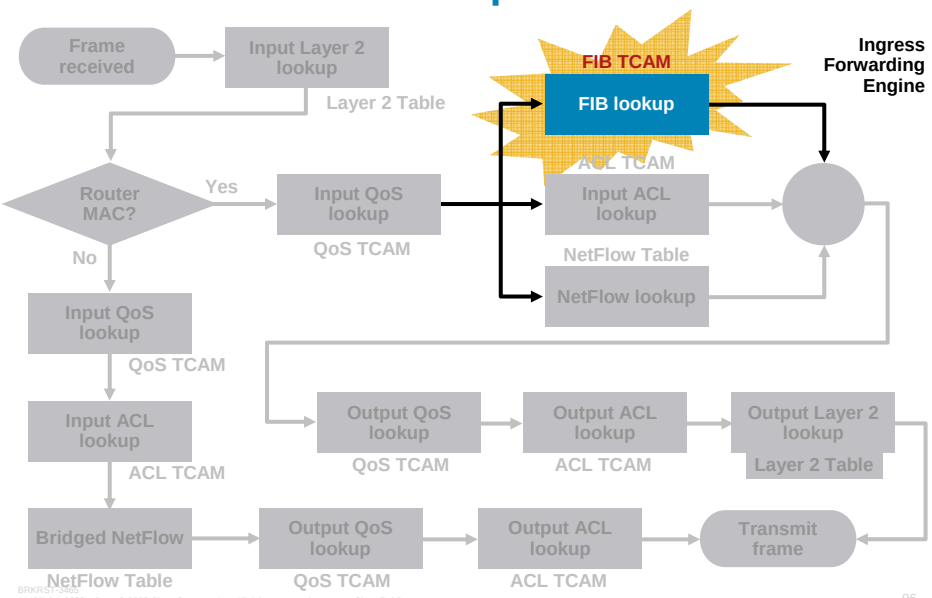
- IPv4 Multicast Forwarding
- Packet Walks

IPv4 Multicast Lookups



IPv4 Multicast Forwarding

- Central and distributed IPv4 multicast hardware forwarding
- Distributed multicast replication with appropriate switching modules†
- PIM-SSM and PIM-SM forwarding in hardware
- BiDirectional-PIM forwarding in hardware
- Off-loads majority of forwarding tasks from RP CPU

† With Fabric-Enabled Modules

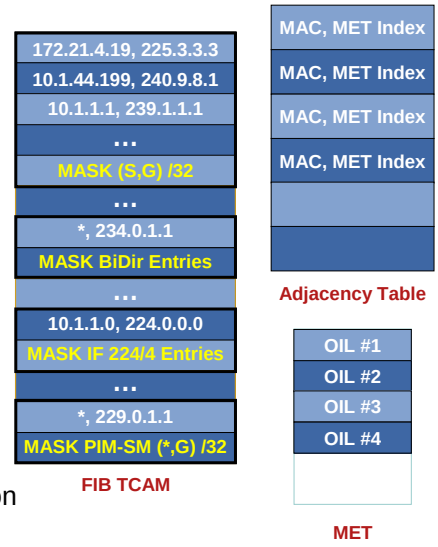
Multicast Forwarding Tables

The Hardware Elements Used to Facilitate Multicast Forwarding Are…

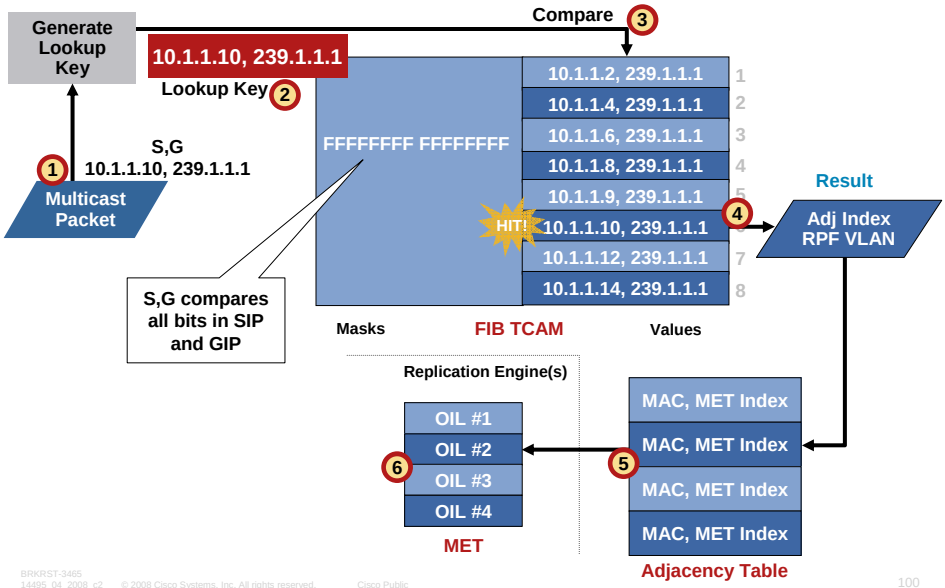
RP/SP CPU	RP builds MROUTE Table, SP downloads into FIB
FIB	Contains the Multicast routes - also known as mroutes
ADJACENCY TABLE	Contains the rewrite information and index into MET table
MULTICAST EXPANSION TABLE (MET)	Contains Output Interface Lists (OIL) - list of interfaces requiring replication

Multicast Hardware Entries

- FIB
  - IPv4 multicast entries arranged logically from most to least specific
- Adjacency table
  - Different format than unicast
  - Key piece of data is MET index
- MET
  - Contains OILs for multicast routes
  - Memory resident on replication engines (not PFC/DFC)



Multicast FIB TCAM Lookup



Reference: Multicast FIB TCAM Lookup Process

1. Source and group IP read from packet
2. Lookup key created based on source and group IPs
3. As lookup key compared to TCAM entries, associated mask applied (for S,G, all bits are compared)
4. Longest match returns RPF interface and index to adjacency entry
5. Adjacency entry contains MET index, which is returned to module as part of lookup result
6. Replication engines access indexed MET block and replicate to specified interfaces

Displaying Summary Hardware Multicast Information

- Cisco IOS: show mls ip multicast summary
- show mls ip multicast statistics
- Catalyst OS: show mls multicast

```
6506#show mls ip multicast summary
21210 MMLS entries using 3394656 bytes of memory
Number of partial hardware-switched flows: 0
Number of complete hardware-switched flows: 21210

Directly connected subnet entry install is enabled
Hardware shortcuts for mvpn mroutes supported
Current mode of replication is Ingress
Auto-detection of replication mode is enabled
Consistency checker is enabled
Bidir gm-scan-interval: 10
6506#
```

Displaying Hardware Multicast Forwarding Entries

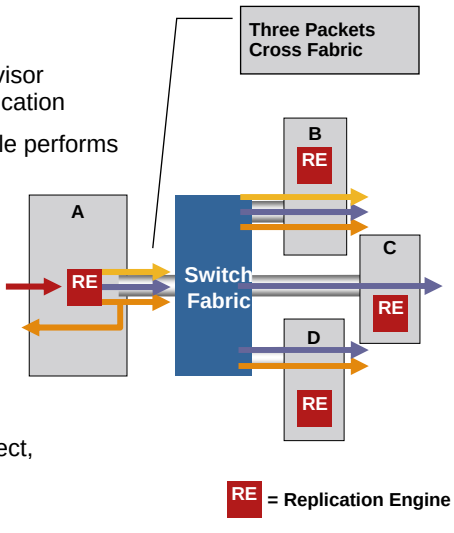
- Cisco IOS: show mls ip multicast
- Catalyst OS: show mls multicast entry

```
6506#show mls ip multicast
Multicast hardware switched flows:
(10.3.1.100, 239.1.1.100) Incoming interface: Gi3/1, Packets switched: 720396460
Hardware switched outgoing interfaces:
    Gi3/2 Vlan100 Vlan150 Gi4/1 Gi4/2 Vlan200
RPF-MFD installed

(10.3.1.103, 230.100.1.1) Incoming interface: Gi3/1, Packets switched: 443201
Hardware switched outgoing interfaces:
    Gi3/2 Gi4/1
RPF-MFD installed
<…>
```

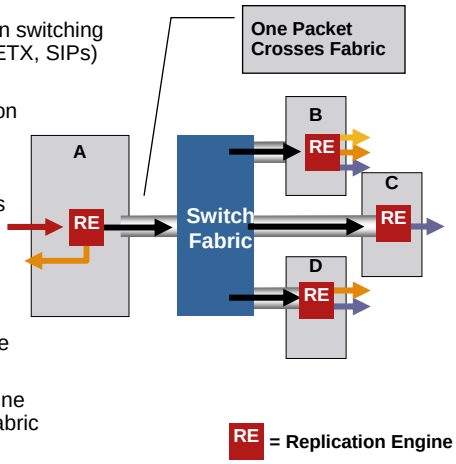

Multicast Ingress Replication Model

- Requires fabric-enabled modules
- Replication load distributed—Supervisor and switching modules perform replication
- Replication engine on ingress module performs replication for all OIFs
- Input and replicated packets get lookup on PFC or ingress DFC
- Replicated copies pass over fabric to egress modules
- Multiple MET tables, but MET on all replication engines synchronized
- Default replication mode is auto-detect, but this can be changed



Multicast Egress Replication Model

- Supported on Supervisor 720 with certain switching modules only (CEF720, 6516A, 6548-GETX, SIPs)
- Replication load distributed—Supervisor and switching modules perform replication
- All modules in chassis must be egress-capable
- Egress mode not optimized unless DFCs present on modules
- Input packets get lookup on ingress DFC, replicated packets get lookup on egress DFC
- For OIFs on ingress module, local engine performs the replication
- For OIFs on other modules, ingress engine replicates a single copy of packet over fabric to all egress modules
- Engine on egress module performs replication for local OIFs
- MET tables on different modules can be asymmetric



Agenda

- Chassis and Power Supplies
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- IPv4 Forwarding
- IPv4 Multicast Forwarding
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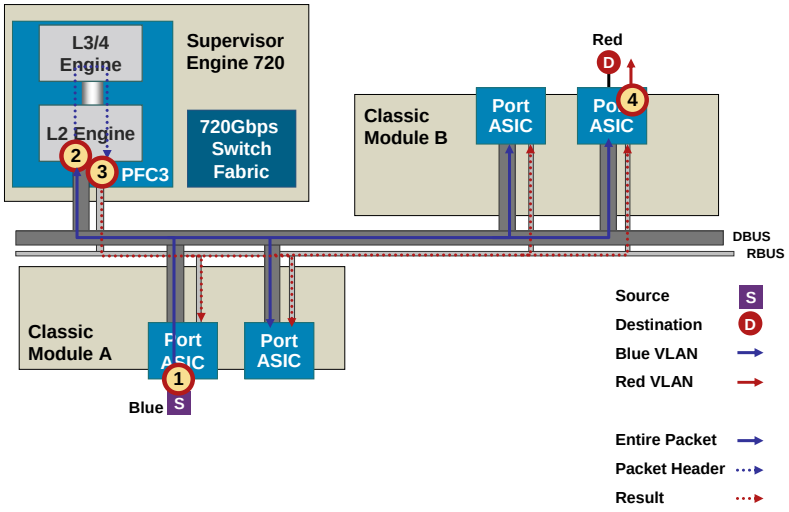
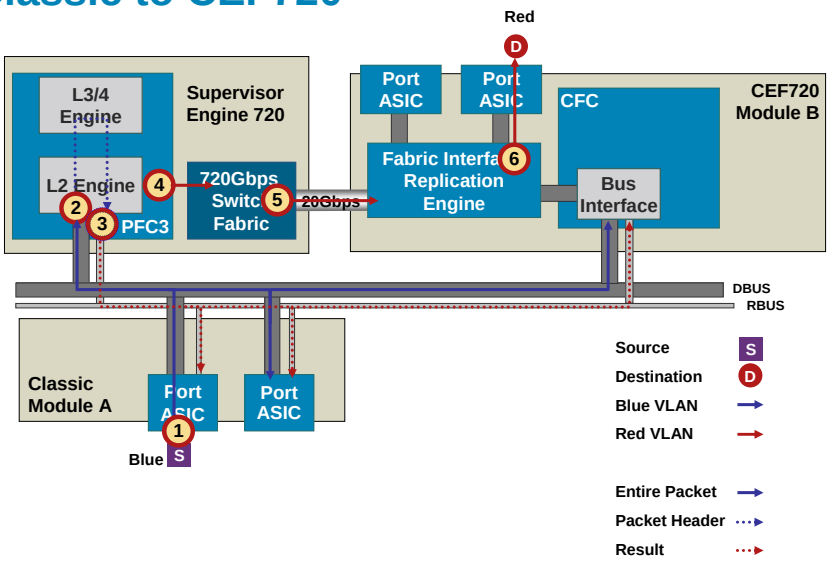
Centralized Forwarding: Classic to Classic



Reference: Classic to Classic

1. Unicast IPv4 packet received on Classic Module A; entire packet is flooded on DBUS and all devices, including the PFC on the supervisor engine, receive it
2. PFC makes a forwarding decision for the packet
3. PFC floods forwarding decision result on RBUS
4. Egress port ASIC on Classic Module B is selected to transmit the packet—all other devices on the bus discard the packet

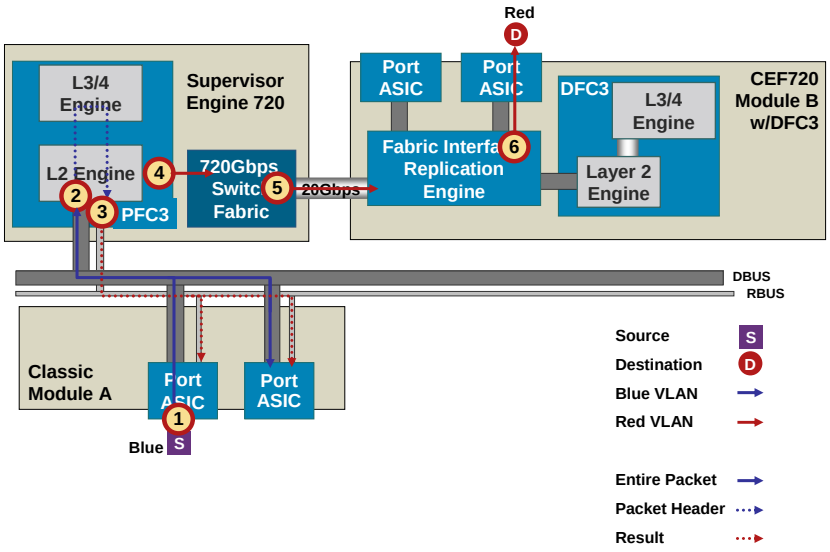
Centralized Forwarding: Classic to CEF720



Reference: Classic to CEF720

1. Unicast IPv4 packet received on Classic Module A; entire packet is flooded on DBUS and all devices, including the PFC on the supervisor engine, receive it; CFC on CEF720 Module B ignores the packet
2. PFC makes a forwarding decision for the packet
3. PFC floods forwarding decision result on RBUS; all devices on the bus discard the packet since the Egress port is on linecard CEF720 Module B; CFC on CEF720 Module B ignores the result
4. The packet is forwarded to the Switch Fabric ASIC
5. Fabric interface transmits packet across the fabric
6. CEF720 Module B receives the packet and transmits the packet to the egress port ASIC

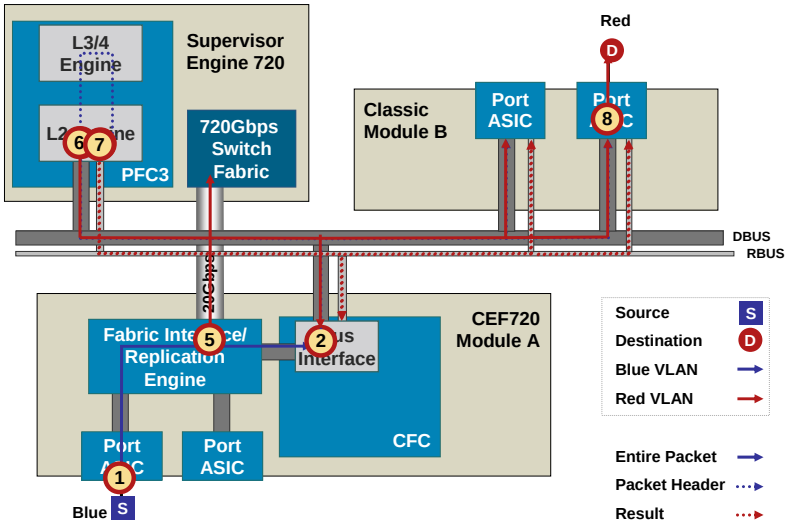
Centralized Forwarding: Classic to CEF720 w/DFC3



Reference: Classic to CEF720 w/DFC3

1. Unicast IPv4 packet received on Classic Module A; entire packet is flooded on DBUS and all devices, including the PFC on the supervisor engine, receive it
2. PFC makes a forwarding decision for the packet
3. PFC floods forwarding decision result on RBUS, and all devices on the bus discard the packet since the Egress port is on linecard CEF720 w/DFC3 Module B
4. The packet is forwarded to the Switch Fabric ASIC
5. Fabric interface transmits packet across the fabric
6. CEF720 Module B receives the packet and transmits the packet to the egress port ASIC

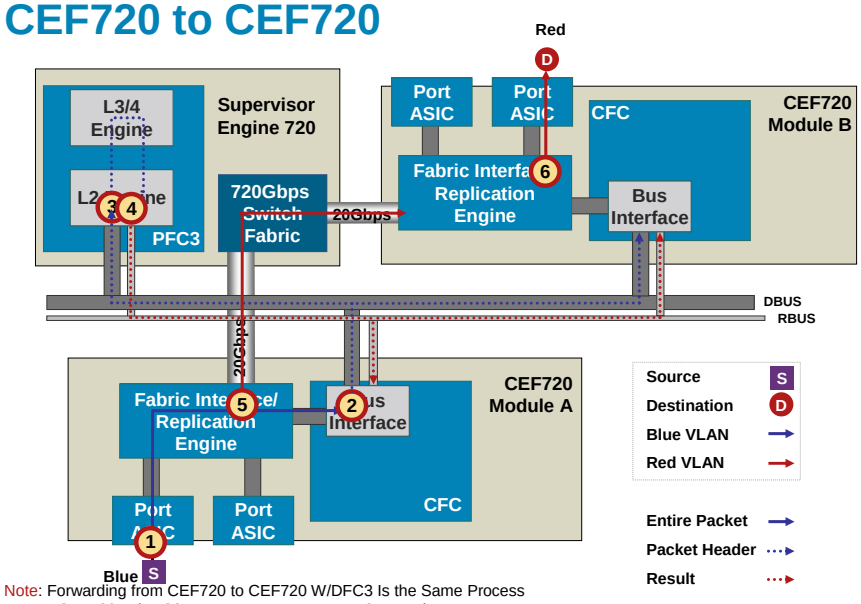
Centralized Forwarding with Fabric: CEF720 to Classic



Reference: CEF720 to Classic

1. A Unicast IPv4 packet received on CEF720 Module A; entire packet is forwarded to the Bus Interface on the CFC
2. The Bus Interface ASIC on CFC forwards the header (compact or truncated) to the Data Bus (DBUS); the header is received by the PFC3 and is ignored by any other device attached to the DBUS
3. The PFC makes a forwarding decision for the packet
4. The PFC floods forwarding decision result on RBUS; only the source Bus Interface processes the result; other devices on the RBUS ignore the result
5. The result + packet is sent from the CFC to the Fabric interface which transmits the packet and result across the fabric to the Sup720, based on the PFC forwarding decision
6. The Sup720 floods the packet onto the DBUS and all devices receive it; CFC on CEF720 Module A ignores the frame
7. The Sup720 generates a new result, identical to the original, and floods it onto the RBUS; CFC on CEF720 Module A ignores the result
8. Egress port ASIC on Classic Module B is selected to transmit the packet—all other devices on the bus discard the packet

Centralized Forwarding with Fabric: CEF720 to CEF720

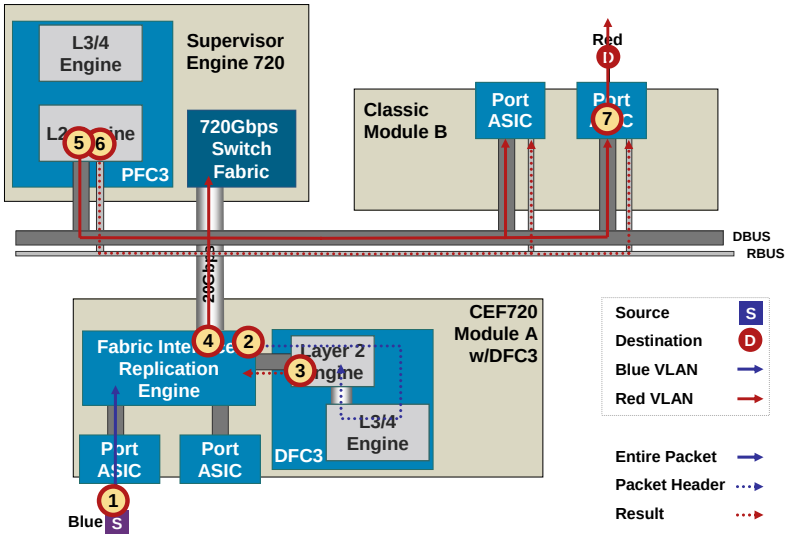


Note: Forwarding from CEF720 to CEF720 W/DFC3 Is the Same Process Except CEF720 W/DFC3 Does Not Have Any Bus Connections

Reference: CEF720 to CEF720

1. A Unicast IPv4 packet received on CEF720 Module A; entire packet is forwarded to the Bus Interface on the CFC
2. The Bus Interface ASIC on CFC of CEF720 Module A forwards the header (compact or truncated) to the Data Bus (DBUS); the header is received by the PFC3 and is ignored by any other device attached to the DBUS
3. The PFC makes a forwarding decision for the packet
4. The PFC floods forwarding decision result on RBUS; only the source Bus Interface processes the result; other devices on the RBUS ignore the result
5. The result + packet is sent from the CFC to the Fabric interface on CEF720 Module A which transmits the packet and result across the fabric to CEF720 Module B, based on the PFC forwarding decision
6. CEF720 Module B receives the packet and transmits the packet to the egress port ASIC

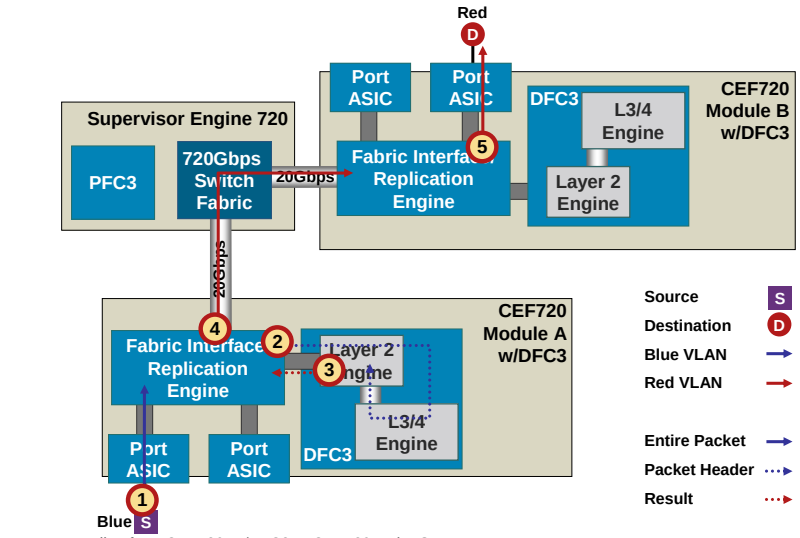
Distributed Forwarding: CEF720 w/ DFC3 to Classic



Reference: CEF720 w/DFC3 to Classic

1. Unicast IPv4 packet received on CEF720 w/DFC3 Module A; entire packet is forwarded to the fabric interface
2. Fabric interface sends just the packet header to the DFC3; DFC3 makes a forwarding decision for the packet
3. DFC3 returns the forwarding decision result to the fabric interface
4. The frame is sent across the fabric to the Sup720, based on the DFC3 forwarding decision
5. The Sup720 floods the packet onto the DBUS and all devices receive it
6. The Sup720 generates a new result, identical to the original, and floods it onto the RBUS
7. Egress port ASIC on Classic Module B is selected to transmit the packet—all other devices on the bus discard the packet

Distributed Forwarding: CEF720 w/DFC3 to CEF720 w/DFC3

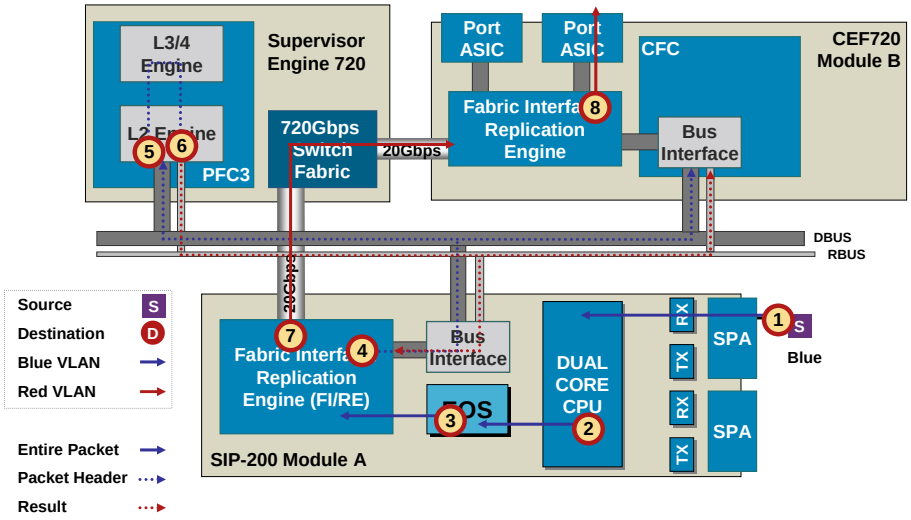


Note: Forwarding from CEF720 W/DFC3 to CEF720 Is the Same Process Except CEF720 Does Not Have Any Bus Connections

Reference: CEF720 w/DFC3 to CEF720 w/DFC3

1. Unicast IPv4 packet received on CEF720 w/DFC3 Module A; entire packet is forwarded to the fabric interface
2. Fabric interface sends just the packet header to the DFC3; DFC3 makes a forwarding decision for the packet
3. DFC3 returns the forwarding decision result to the fabric interface
4. Fabric interface transmits packet across the fabric
5. CEF720 w/DFC3 Module B receives the packet and transmits the packet to the egress port ASIC

WAN Forwarding: SIP-200 to CEF720

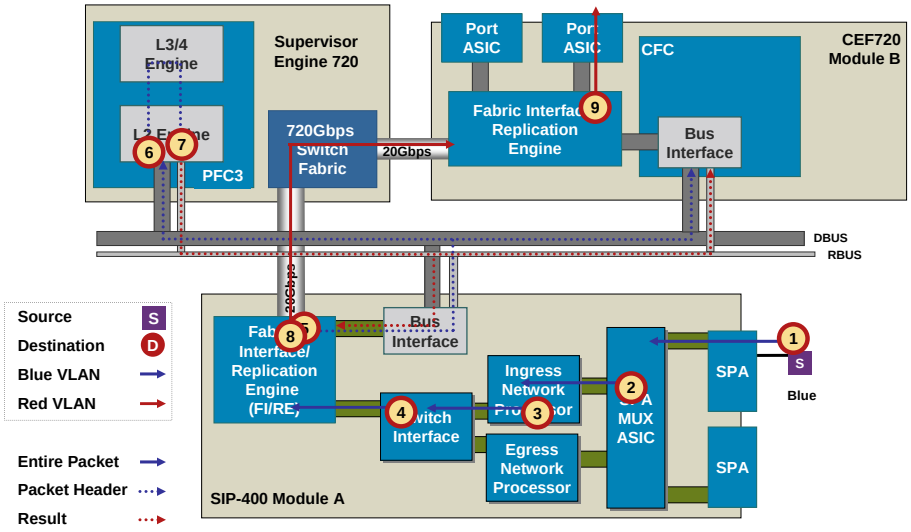


Reference: SIP-200 to CEF720

1. A Unicast IPv4 packet received on SIP-200 Module A SPA interface; entire packet is forwarded through the RX FPGA to the Dual Core CPU
2. Dual Core CPU removes the WAN header and classifies the packet: non-IP packets are sent to the Supervisor 720 RP, IP packets have a DBUS header appended and are sent to EOS
3. EOS generates CRC for DBUS header and payload and forwards the packet to FI/RE.
4. FI/RE saves the packet in memory and floods DBUS header onto DBUS; header is received by PFC3 and ignored by CFC on CEF720 Module B
5. PFC3B makes a forwarding decision for the packet
6. The PFC floods forwarding decision result on RBUS; only the source Bus Interface processes the result; other devices on the RBUS ignore the result
7. The result is sent to FI/RE which transmits the packet and result across the fabric to CEF720 Module B, based on the PFC forwarding decision
8. CEF720 Module B receives the packet and transmits the packet to the egress port ASIC

Note: Forwarding from SIP-200 to CEF720 W/DFC3 Is the Same Process Except CEF720 W/DFC3 Does Not Have Any Bus Connections

WAN Forwarding: SIP-400 to CEF720

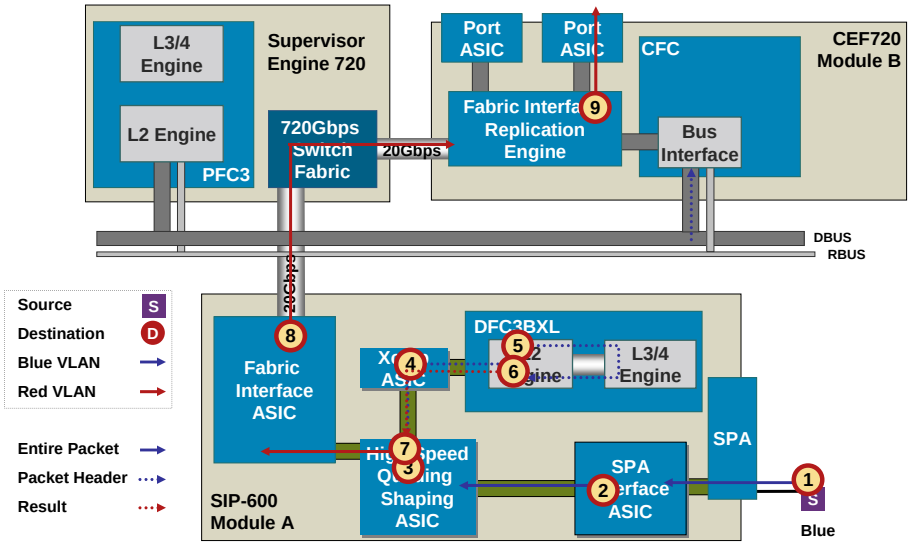


Reference: SIP-400 to CEF720

1. A Unicast IPv4 packet received on SIP-400 Module A SPA interface; entire packet is forwarded to SPA MUX ASIC
2. SPA MUX ASIC sends the packet on to the Ingress Network Processor (INP)
3. INP classifies the packet: non-IP packets are sent to the Supervisor 720 RP; IP packets have outer header (WAN or .1q) stripped, have a DBUS header appended and are sent to Switch Interface
4. Switch Interface updates the DBUS header CRC and forwards to FI/RE
5. FI/RE saves the packet in memory and floods DBUS header onto DBUS; header is received by PFC3 and ignored by CFC on CEF720 Module B
6. PFC3B makes a forwarding decision for the packet
7. The PFC floods forwarding decision result on RBUS; only the source Bus Interface processes the result; other devices on the RBUS ignore the result
8. The result is sent to FI/RE which transmits the packet and result across the fabric to CEF720 Module B, based on the PFC forwarding decision
9. CEF720 Module B receives the packet and transmits the packet to the egress port ASIC

Note: Forwarding from SIP-400 to CEF720 W/DFC3 Is the Same Process Except CEF720 W/DFC3 Does Not Have Any Bus Connections

WAN Forwarding: SIP-600 to CEF720

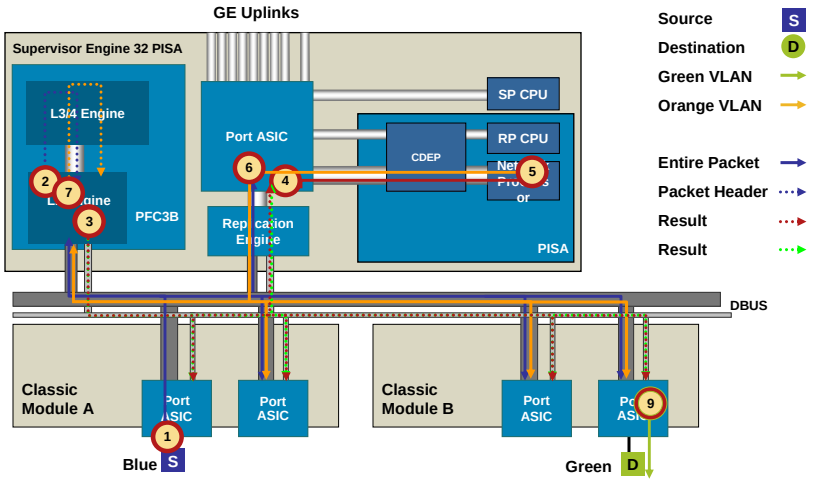


Reference: SIP-600 to CEF720

1. A Unicast IPv4 packet received on SIP-600 Module A SPA interface; entire packet is forwarded to SPA Interface ASIC
2. SPA Interface ASIC sends the packet on to the High Speed Queuing and Shaping ASIC
3. High Speed Queuing and Shaping ASIC saves the packet in memory and sends the header to the Xchip ASIC
4. The Xchip will determine if the packet is to be sent directly to the Supervisor 720 Route Processor for processing (mostly for control plane traffic) or if it is to be sent to the DFC3BXL for processing; in this case it is sent to the DFC3BXL since it is data traffic
5. DFC3BXL makes a forwarding decision for the packet
6. DFC3BXL forwards the result to Xchip (which does the L2/L3 rewrites and any replication)) and back to the High Speed Queuing and Shaping ASIC
7. The High Speed Queuing and Shaping ASIC assembles the newly rewritten header with the previously stored packet and forwards it to the Fabric Interface ASIC.
8. The Fabric Interface ASIC transmits the packet across the fabric to CEF720 Module B, based on the PFC forwarding decision
9. CEF720 Module B receives the packet and transmits the packet to the egress port ASIC

Note: Forwarding from SIP-600 to CEF720 W/DFC3 Is the Same Process Except CEF720 W/DFC3 Does Not Have Any Bus Connections

PISA Forwarding Ingress NBAR/FPM



Reference: PISA Forwarding Ingress NBAR/FPM

1. Unicast IPv4 packet received on Classic Module A; entire packet is flooded on DBUS and all devices, including the PFC3B and Port ASIC on the Supervisor 32-PISA, receive it
2. PFC3B makes a forwarding decision for the packet; If ingress FPM/NBAR is configured, the ingress ACL result would trigger traffic redirection to the PISA.
3. PFC3B floods forwarding decision result on RBUS
4. Egress port ASIC on Sup32-GE-PISA is selected to transmit the packet—all other devices on the bus discard the packet
5. The Network Processor receives the packet over the PISA Channel, performs ingress NBAR/FPM (including L3 QoS) and sends the packet back to the forwarding engine on the Orange internal VLAN over the PISA Channel
6. Port ASIC on Sup32-GE-PISA floods the packet on DBUS and all devices, including the PFC3B, receive it
7. PFC3B makes a forwarding decision for the packet
8. PFC3B floods forwarding decision result on RBUS
9. Egress port ASIC on Classic Module B is selected to transmit the packet—all other devices on the bus discard the packet

Conclusion

- You should now have a thorough understanding of the Catalyst 6500 switching architecture, packet flow, and key forwarding engine functions…

  Any Questions?

Reference: Acronym Decoder

- ACL—Access Control List
- ADJ—Adjacency
- CAM—Content Addressable Memory
- CEF—Cisco Express Forwarding
- CF—Compact Flash
- CFC—Central Forwarding Card
- CoPP—Control Plane Policing
- COS—Class of Service
- DBUS—Data Bus
- DFC—Distributed Forwarding Card
- DSCP—Differentiated Services Code Point
- EEPROM—Electrically Erasable Programmable ROM
- EOBC—Ethernet Out of Band Channel
- EoMPLS—Ethernet over MPLS
- FIB—Forwarding Information Base
- GRE—Generic Route Encapsulation
- HSRP—Hot Standby Router Protocol
- IGMP—Internet Group Management Protocol
- LCDBUS—Line Card DBUS
- LCRBUS—Line Card RBUS
- LOU—Logical Operation Unit
- MET—Multicast Expansion Table
- MMLS—Multicast Multilayer Switching
- MPLS—Multiprotocol Label Switching
- MSFC—Multilayer Switch Feature Card
- NAT—Network Address Translation
- NDE—NetFlow Data Export
- NMP—Network Management Processor
- OIF—Output Interface
- OIL—Output Interface List
- PACL—Port ACL
- PAT—Port Address Translation (L4 NAT)
- PBR—Policy-Based Routing
- PD—Powered device
- PEM—Power entry module
- PFC—Policy Feature Card
- PIM—Protocol Independent Multicast
- QoS—Quality of Service
- RBUS—Results Bus
- RP—Route Processor
- RPF—Reverse Path Forwarding
- RPF-MFD—RPF Multicast Fast Drop
- SFM—Switch Fabric Module
- SFP—Small-Formfactor Pluggable
- SIP – SPA Interface Processor
- SP—Switch Processor
- SPA – Shared Port Adapter
- TCAM—Ternary CAM
- UBRL—User-based rate limiting (microflow policing)
- uRPF—Unicast RPF
- VACL—VLAN ACL
- VRRP—Virtual Router Redundancy Protocol
- VTT—Voltage termination
- WRED—Weighted Random Early Detection
- WRR—Weighted Round Robin

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- RST-3143: Troubleshooting Catalyst 6500 Series Switches
- RST-3467: Cisco IOS Software Modularity—Architecture and Deployment
- RST-3468: Cisco Catalyst Virtual Switch System (VSS)
- TECRST-2001: Enterprise High Availability
- TECRST-2002: Cisco Catalyst 6500 Technical Deep Dive

Q and A

Recommended Reading

- Continue your Cisco Live learning experience with further reading from Cisco Press
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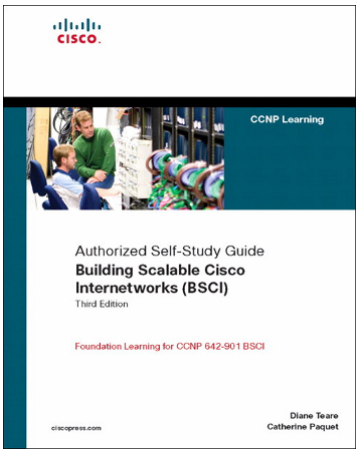

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