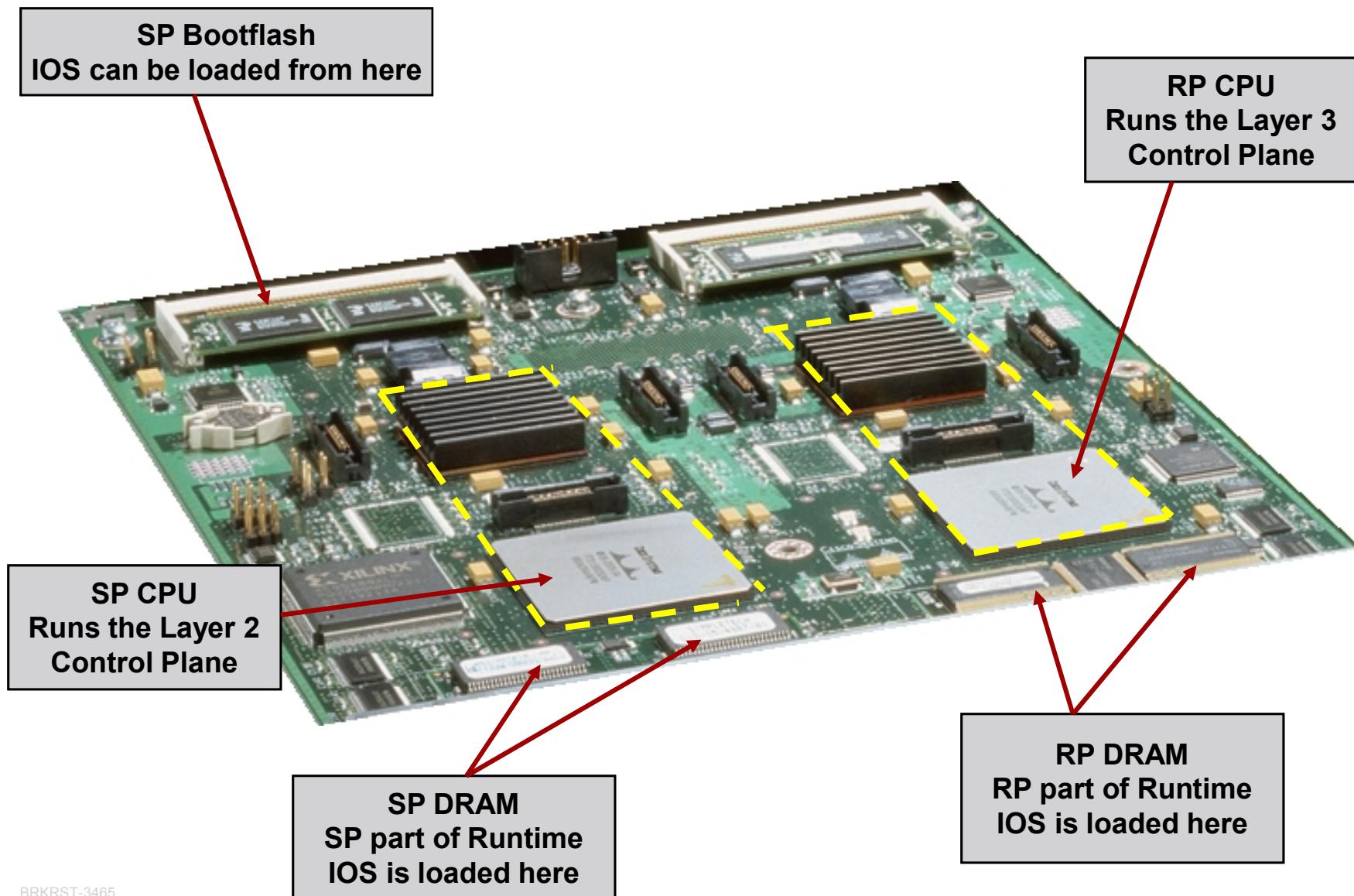


Catalyst 6500 Boot Process

Catalyst 6500 Bootcamp

Cisco IOS Supervisor Hardware Components



Cisco IOS Image Locations

Depending on which Supervisor You Have, there Are Different Options for Storage of the Cisco IOS Image for Booting:

- **Supervisor 32**

- 256MB SP Internal Compact Flash bootdisk

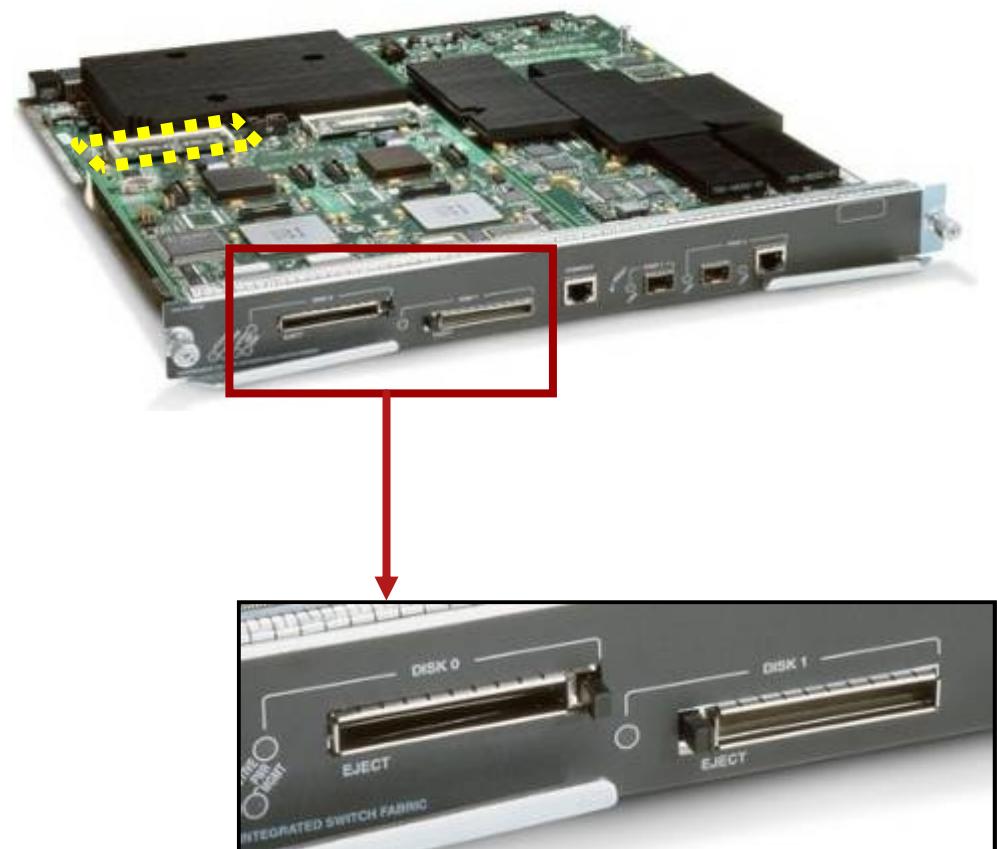
- 1 Type II External Compact Flash slot

- **Supervisor 720**

- 64MB SP Bootflash –or–

- 512MB SP Internal Compact Flash bootdisk

- 2 Type II External Compact Flash slots



Supervisor 720 Internal Compact Flash Adapter

An Internal Compact Flash Adapter that Can Take the Place of the 64MB Bootflash on the Supervisor 720

COMPACT FLASH ADAPTER



CF Adapter Specifications

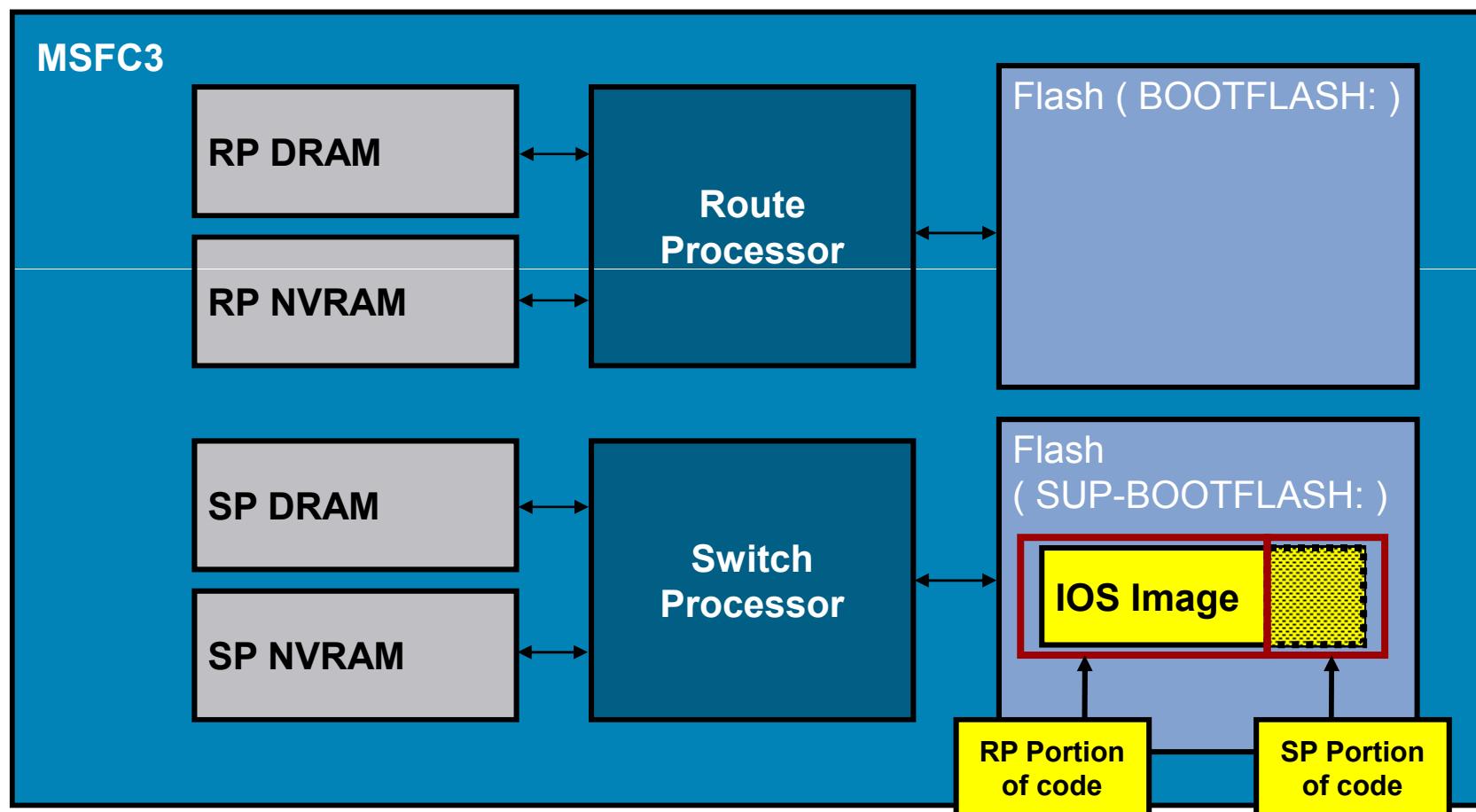
- Part Number WS-CF-UPG=
- Supported in Sup720, Sup720-3B, Sup720-3BXL
- WS-CF-UPG= comes by default with 512MB
- CF Adapter is NOT OIR capable
- Requires IOS 12.2(18)SXE5 and SP ROMMON 8.4(2)
- LED located on CF Adapter which will flash green when CF is accessed; designed for use during troubleshooting

Installation instructions at

http://www.cisco.com/univercd/cc/td/doc/product/lan/cat6000/cfgnotes/78_17277.htm

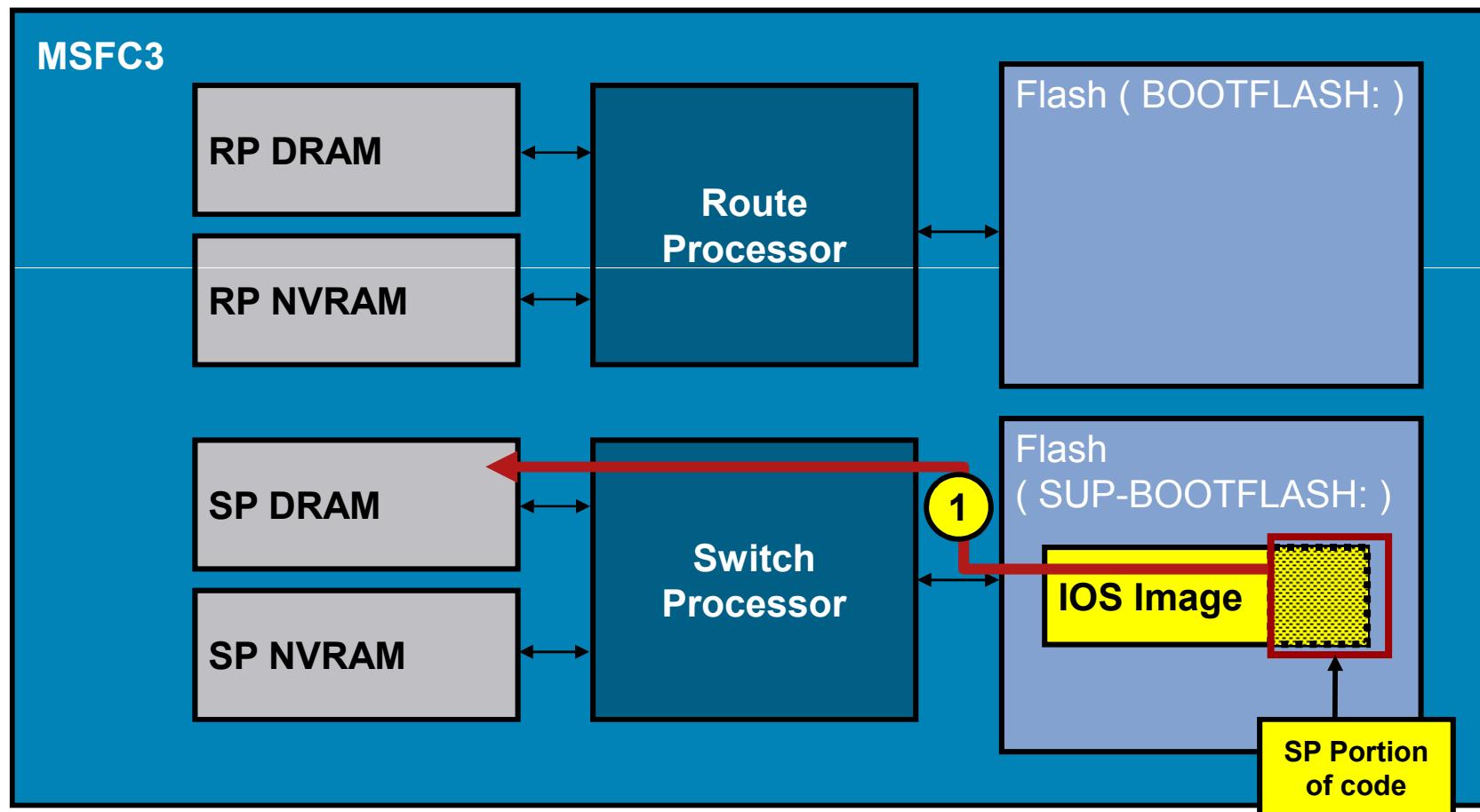
Booting Cisco IOS

The Runtime Image for the Catalyst 6500 is Delivered as a Single BINARY Image that Is Loaded on the SP Bootflash or Bootdisk



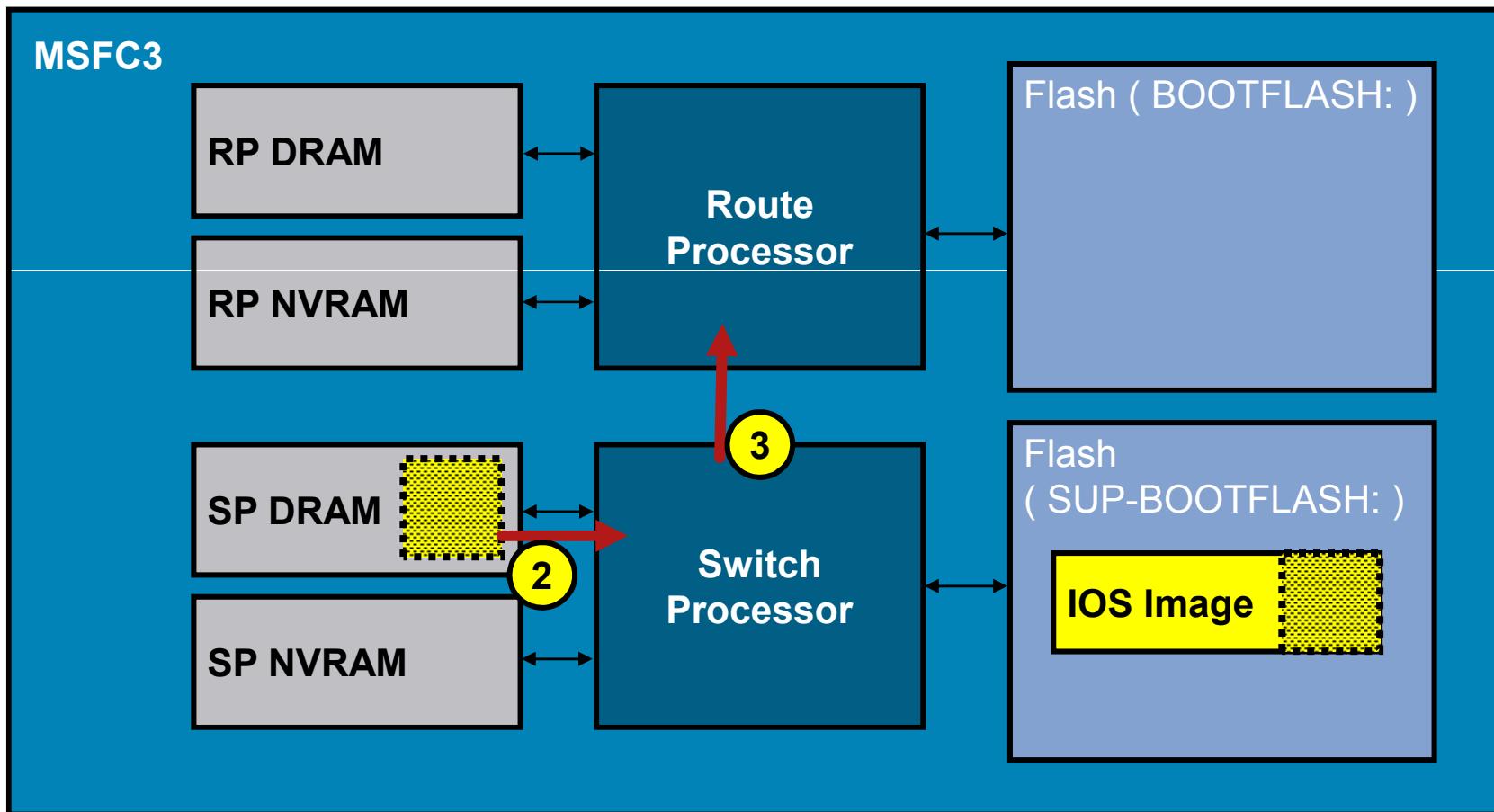
Booting Cisco IOS (Cont.)

The SP Initially Owns the Boot Process—First the SP Portion of the Image Is Decompressed and Loaded into the SP DRAM...



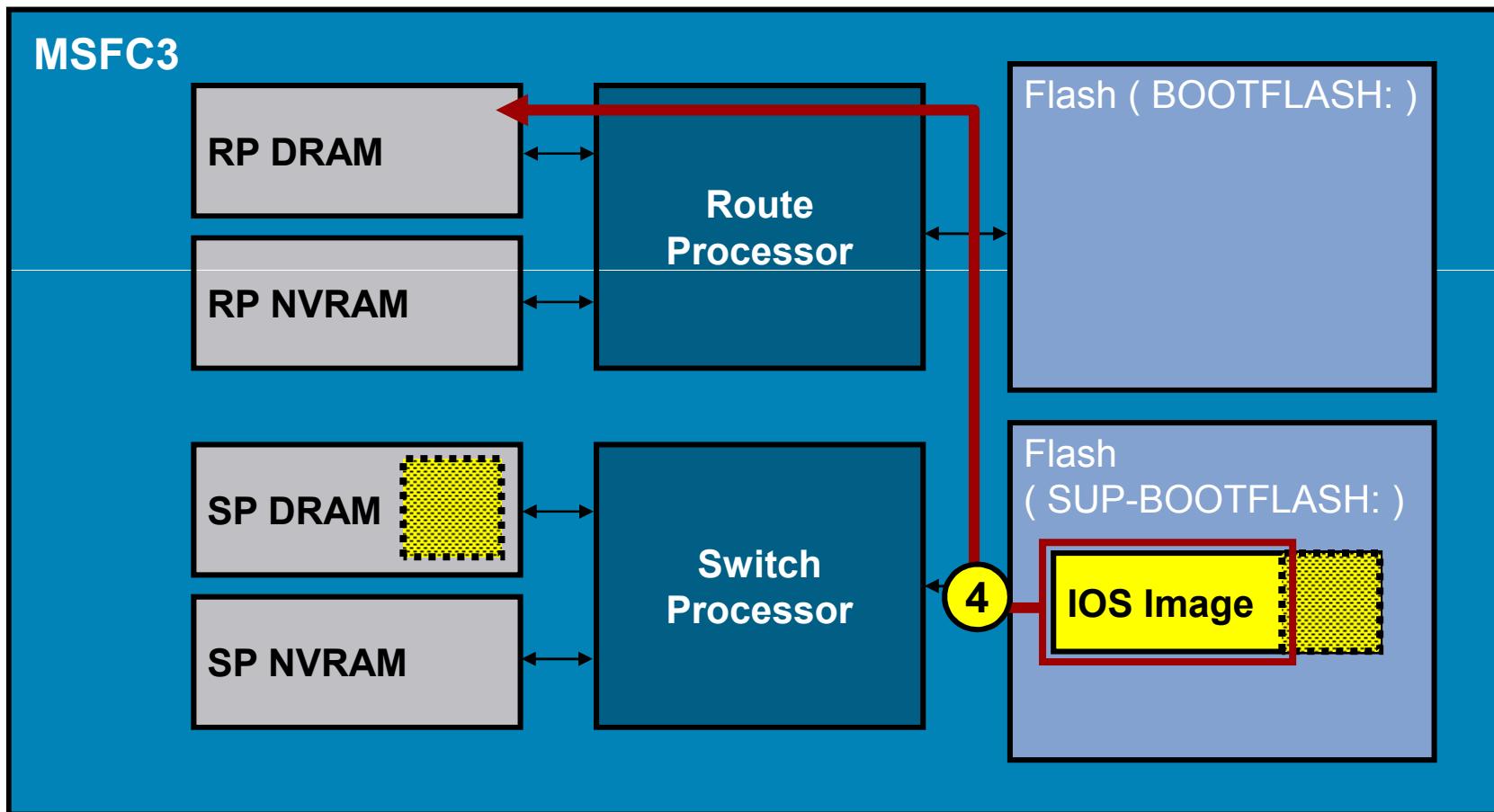
Booting Cisco IOS (Cont.)

The SP then begins the Boot Process by Booting from this Image—When It Has Completed Its Boot Process, It Hands Over the Console to the RP to Continue the Boot Process



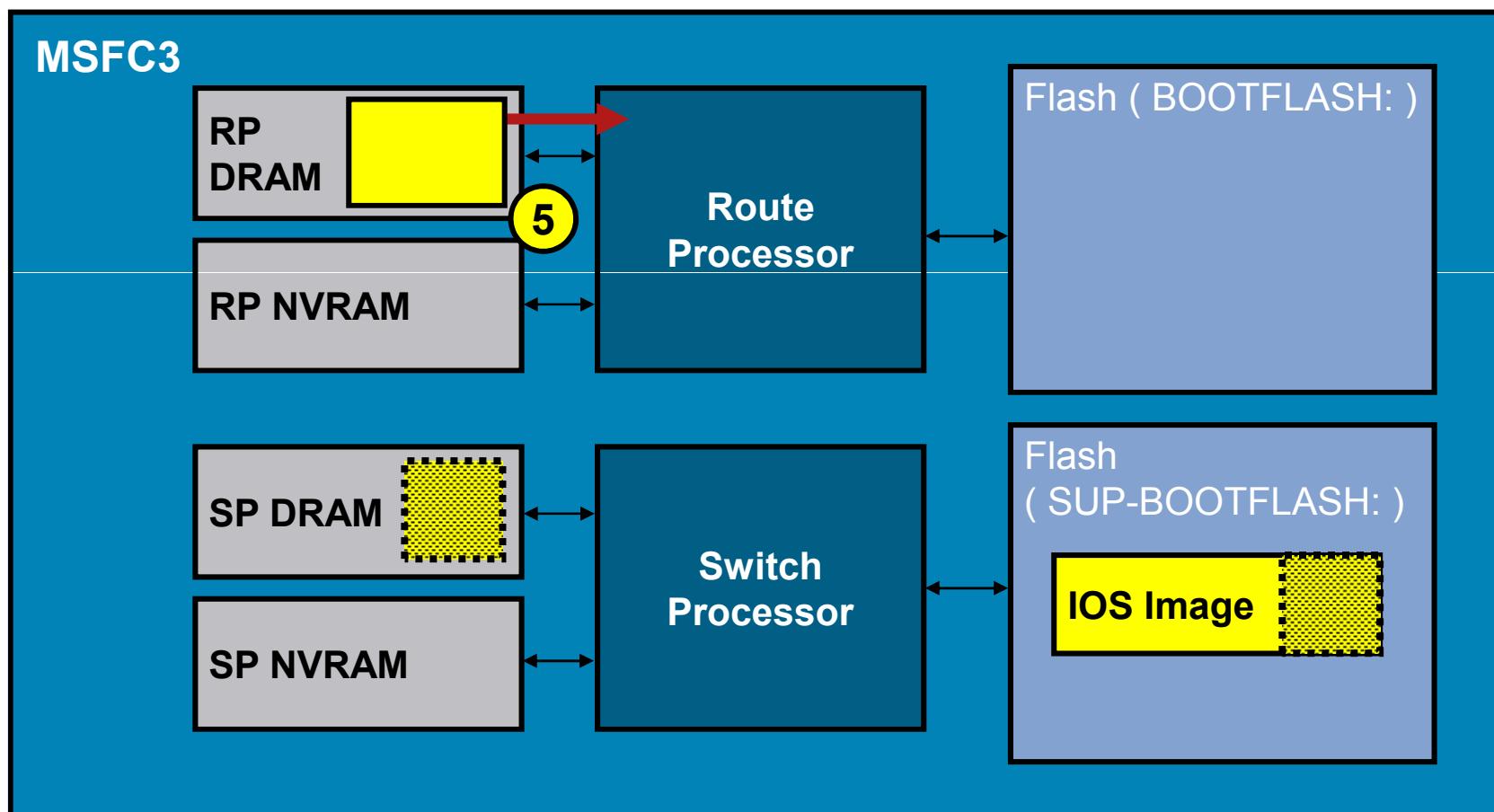
Booting Cisco IOS (Cont.)

The RP then Downloads the RP Portion of the Cisco IOS Image into RP DRAM—Once It Has Fully Downloaded the Image, the RP Will then Decompress the Image



Booting Cisco IOS (Cont.)

After Decompressing the Image, the RP Will Boot Using this Image in RP DRAM to Complete the Boot Process—Once Fully Booted, the Console Remains Under Control of the RP



Booting Cisco IOS (Cont.)

```
System Bootstrap, Version 7.7(1)
Copyright (c) 1994-2003 by cisco Systems, Inc.
Cat6k-Sup720/SP processor with 524288 Kbytes of main memory
```

```
Autoboot executing command: "boot disk0:s72033-ipservicesk9_wan-vz.122-18.SXF2
```

```
Self decompressing the image : #####
```

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cisco Systems, Inc.
170 West Tasman Drive
San Jose, California 95134-1706

Cisco Internetwork Operating System Software
IOS (tm) s72033_sp Software (s72033_sp-IPSERVICESK9_WAN-VM), Version 12.2(18)SXF2,
RELEASE SOFTWARE (fc1)
TAC Support: <http://www.cisco.com/tac>
Copyright (c) 1986-2003 by cisco Systems, Inc.
Compiled Tue 27-May-03 20:48 by cc当地
Image text-base: 0x40020C10, data-base: 0x40B98000

1

SP portion of code is decompressed

2

SP portion of code identified by “SP” keyword in image name

Booting Cisco IOS (Cont.)

3

When the SP has fully booted, the console is handed over to the RP

```
00:00:28: %PFREDUN-6-ACTIVE: Initializing as ACTIVE processor  
00:00:28: %OIR-SP-6-CONSOLE: Changing console ownership to route processor
```

4

RP portion of image is loaded into RP DRAM

```
System Bootstrap, Version 12.2(14r)S1, RELEASE SOFTWARE (fc1)  
TAC Support: http://www.cisco.com/tac  
Copyright (c) 2003 by cisco Systems, Inc.  
Cat6k-Sup720/RP platform with 524288 Kbytes of main memory
```

Download Start

```
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
```

Download Completed! Booting the image.

```
Self decompressing the image : #####
```

5

RP image is booted from RP DRAM

Booting Cisco IOS (Cont.)

<SNIP>

```
Cisco Internetwork Operating System Software
IOS (tm) s72033_rp Software (s72033_rp-IPSERVICESK9_WAN-VM), Version 12.2(18)SXF2,
RELEASE SOFTWARE (fc1)
Technical Support: http://www.cisco.com/techsupport
Copyright (c) 1986-2006 by cisco Systems, Inc.
Compiled Wed 18-Jan-06 21:59 by dchih
Image text-base: 0x01020150, data-base: 0x01021000
```

RP image is now active

```
cisco WS-C6503 (R7000) processor (revision 1.1) with 491520K/32768K bytes of memory.
Processor board ID FOX063513LV
SR71000 CPU at 600Mhz, Implementation 1284, Rev 1.2, 512KB L2 Cache
Last reset from power-on
Bridging software.
X.25 software, Version 3.0.0.
SuperLAT software (copyright 1990 by Meridian Technology Corp).
TN3270 Emulation software.
1 Virtual Ethernet/IEEE 802.3 interface
48 FastEthernet/IEEE 802.3 interfaces
4 Gigabit Ethernet/IEEE 802.3 interfaces
1917K bytes of non-volatile configuration memory.
```

65536K bytes of Flash internal SIMM (Sector size 512K)

Press RETURN to get started!

6500>

Image boots up and console user presented with CLI prompt

6