Block	Signal Name	Description	Register	Register Hex	SPI bits <?:0>	Functional Name	# of bits	Defaults	NOTE	SPI DEFAULTS
PGA	pga_bypass_preamp	Bypass preamp section of PGA	0	0	[0]	pga_ctrl	1	1'b0	PGA gain = SC gain when preamp is bypassed	0x0012
	pga_hg	Gain of SC stage	0	0h	[1]	pga_ctrl	1	1'b1	0 --> SC gain = 1, 1 --> SC gain is 2	
	pga_gain_sel<3:0>	Selects PGA preamp gain	0	0h	[5:2]	pga_ctrl	4	4'b0100	0001 -> 2, 0010 -> 3, 0100 -> 4, 1000 -> 6 (Overall PGA gain is preamp gain * SC gain)	
OFFSET DAC	offset_mode<1:0>	Choose offset calibration mode	1	1h	[1:0]	offset_dac_ctrl	2	2'b11	00 -> use DAC values from SPI, 01 -> use vtop external pin voltage, 10 -> use DAC values from SPI, 11 -> self-calibrate	0x007F
	offset_dac_default<5:0>	Offset DAC value output to use in offset_mode = 2'b10	1	1h	[7:2]	offset_dac_ctrl	6	6'b011111		
	offset_channel<4:0>	Select which channel used to calculate offset	1	1h	[12:8]	offset_dac_ctrl	5	5'b00000		
ADC	adc_bias_adj<3:0>	Selects ADC bias current	2	2h	[3:0]	adc_ctrl	4	4'b0111	ADC bias current = (1.875*imasterbias) - adc_bias_adj<3:0>*imasterbias/8 µA	0x0257
	adc_comp_bias_adj<3:0>	Selects ADC comparator bias current. Scales with ADC bias current.	2	2h	[7:4]	adc_ctrl	4	4'b0101	current = 150uA - adc_comp_bias_adj<3:0>*10uA	
	adc_extern_reference	Selects internal or external ADC reference voltages	2	2h	[8]	adc_ctrl	1	1'b0	0 --> internal references 1 --> external references	
	adc_output_format	Format of digital output data	2	2h	[9]	adc_ctrl	1	1'b1	0--> two's complement, 1 --> offset binary,	
Digital Core	cal_cycles<7:0>	Number of ADC samples to take for each measurements	3	3h	[7:0]	cal_engine_cycles	8	8'h0f	# of cycles is 2^(cal_cycles). Trades off calibration speed vs. noise resistance	0x000F
	calbits<2:0>	Number of ADC stages to calibrate	4	4h	[2:0]	cal_engine_ctrl	3	3'b011	There are 8 calibrated stages in HIPSTER	0x0003
	sso_adc_select<4:0>	Select which ADC read out through SSO	5	5h	[5:0]	sso_ctrl	4	5'b00000		0x0000
	sso_data_select	Selects whether decisions or calibrated ADC data set through SSO.	5	5h	[6]	sso_ctrl	1	1'b0	0 --> stage decisions, 1 --> calibrated data	
	sso_enable	Enables SSO port.	5	5h	[7]	sso_ctrl	1	1'b0	0 --> port disabled. 1 --> port enabled.	
TX	tx_bypass_eq	Bypass EQ section of TX	6	6h	[0]	tx_bypass	1	1'b1	0 --> do not bypass EQ, 1 --> bypass EQ.Bypass EQ by default	0x0001
	eq_precursor_tap_sign	Selects sign of EQ precursor taps.	7	7h	[0]	tx_eq_sign	1	1'b1	0 --> positive weight. 1 --> negative weight	0x0007
	eq_cursor_tap_sign	Selects sign of EQ cursor taps.	7	7h	[1]	tx_eq_sign	1	1'b1	0 --> positive weight. 1 --> negative weight	
	eq_postcursor_tap_sign	Selects sign of EQ postcursor taps.	7	7h	[2]	tx_eq_sign	1	1'b1	0 --> positive weight. 1 --> negative weight	
	bypass_tap_ctrl[5:0]<3:0>	Four-bit current DAC setting for bypass driver. Independent DAC setting for each of 6 Transmitters. Nominal current (in bypass mode) is 6.4 mA.	8,9	8h,9h	[3:0] 0 [7:4] 1 [11:8] 2 [15:12] 3 +[3:0] 4 +[7:4] 5	bypass_tap_ctrl_{0,1}	24	4'b0111 (each)	Drive current is 16*(bypass_tap_ctrl<3:0> * 50µA)	0x7777_7777
	precursor_tap_ctrl[5:0]<3:0>	Four-bit current DAC setting for precursor driver. Independent DAC setting for each of 6 Transmitters.	10,11	Ah,Bh	[3:0] 0 [7:4] 1 [11:8] 2 [15:12] 3 +[3:0] 4 +[7:0] 5	precursor_tap_ctrl_{0,1}	24	4'b0000 (each)	Drive current is 16*(precursor_tap_ctrl<3:0> * 50 µA)	0x0000_0000
	cursor_tap_ctrl[5:0]<3:0>	Four-bit current DAC setting for cursor (main) driver. Independent DAC setting for each of 6 Transmitters. Nominal current (in EQ mode) is 6.4 mA.	12,13	Ch,Dh	[3:0] 0 [7:4] 1 [11:8] 2 [15:12] 3 +[3:0] 4 +[7:4] 5	cursor_tap_ctrl_{0,1}	24	4'b0000 (each)	Drive current is 16*(cursor_tap_ctrl<3:0> * 50 µA)	0x0000_0000
	postcursor_tap_ctrl[5:0]<3:0>	Four-bit current DAC setting for postcursor driver. Independent DAC setting for each of 6 Transmitters.	14,15	Eh,Fh	[3:0] 0 [7:4] 1 [11:8] 2 [15:12] 3 +[3:0] 4 +[7:4] 5	postcursor_tap_ctrl_{0,1}	24	4'b0000 (each)	Drive current is 16*(postcursor_tap_ctrl<3:0> * 50 µA)	0x0000_0000
PLL	c1_select<7:0>	Selects value of C1 in PLL LF	16	10h	[7:0]	pll_cap1_ctrl	8	8'h83	C1 = c1_select*0.625pF	0x0083
	c2_select<7:0>	Selects value of C2 in PLL LF	17	11h	[7:0]	pll_cap2_ctrl	8	8'h03	C2 = c2_select*25fF	0x0003
	r1_select<2:0>	Selects value of R1 in PLL LF	18	12h	[2:0]	pll_res_ctrl	3	3'h5	R1 = r1_select*2.5kOhm + 2.5kOhm	0x0075
	pll_cp_bias_adj<3:0>	Adjusts PLL charge pump current	18	12h	[7:4]	pll_res_ctrl	4	4'b0111	PLL CP bias current = (1.875*imasterbias) - pll_cp_bias_adj<3:0>*imasterbias/8 µA	
	clk_mon_sel	Selects clock to monitor	19	13h	[0]	pll_ctrl	1	1'b0	0 -> refclk, 1 -> fbclk	0x2200

Block	Signal Name	Description	Register	Register Hex	SPI bits <?:0>	Functional Name	# of bits	Defaults	NOTE	SPI DEFAULTS
	bypass_vco	Route external VCO to TX , bypassing internal VCO	19	13h	[1]	pll_ctrl	1	1'b0		
	observe_vctrl	Route vctrl to pin	19	13h	[2]	pll_ctrl	1	1'b0		
	observe_pfd<2:0>	Route pfd signals to pin	19	13h	[6:4]	pll_ctrl	3	3'h0	bit 0: PFD_UP, bit 1: PFD_DOWN, bit2: not used	
	force_vctrl	Forces external value for VCTRL (VCO frequency control)	19	13h	[8]	pll_ctrl	1	1'b0		
	bypass_retimer	Forces bypass of retimer internal to FBDIV	19	13h	[9]	pll_ctrl	1	1'b1		
	ldo_output_select<2:0>	Selects LDO output voltage	19	13h	[14:12]	pll_ctrl	3	3'h2	Vout = 1.8V + 0.05*ldo_output_select	
BIAS	bias_readback<1:0>	Chooses bias current to read out for diagnostics	20	14h	[1:0]	bias_ctrl	2	2'h0	afe: 00 --> master, 01 -> ADC, 10 -> master, 11 -> refbuffer; tx: 00 -> master, 01 -> CML_50u (actual CML current is 8X this value), 10 -> master, 11 -> PLL_CP	0x8880
	bgr_kickstart	Forces BGR away from zero-current state	20	14h	[2]	bias_ctrl	1	1'b0	To kickstart BGR, set bgr_kickstart -> 1 and then immediately return it to 0	
	master_bias_adj<3:0>	Adjusts master bias current to correct for resistor tolerance	20	14h	[7:4]	bias_ctrl	4	4'h8	imasterbias = 93.75uA - master_bias_adj<3:0>*6.25 µA	
	cml_bias_adj<3:0>	Adjusts bias current for CML logic.	20	14h	[11:8]	bias_ctrl	4	4'h8	CML bias current = 8*(1.875*imasterbias) - cml_bias_adj<3:0>*imasterbias/8 µA	
	refbuffer_bias_adj<3:0>	Adjusts bias current for ADC Reference Buffer	20	14h	[15:12]	bias_ctrl	4	4'h8	Ref buffer current = ((1.875*imasterbias) - refbuffer_bias_adj<3:0>*imasterbias/8 µA))	
	testbuffer_ctrl<2:0>	Selects signal to read back through testbuffer	21	15h	[2:0]	testbuff_ctrl	3	3'h0	000 -- > vbg, 001 -> vrefp, 010 -> vrefn, 011 -> vcm, 100 -> vthreshp, 101 -> vthreshn, 110 -> vmasterbias, 111 -> vbg	0x0000
Powerdown	pd_lvds_tx	Powers down LVDS transmitters used for clock readback	22	16h	[0]	pd_ctrl	1	1'b0		0x001E
	pd_testbuffer	Powers down analog testbus monitor buffers	22	16h	[1]	pd_ctrl	1	1'b1		
	pd_precursor	Powers down precursor tap of TX equalizer	22	16h	[2]	pd_ctrl	1	1'b1	EQ is bypassed by default	
	pd_cursor	Powers down cursor tap of TX equalizer	22	16h	[3]	pd_ctrl	1	1'b1		
	pd_postcursor	Power down postcursor tap of TX equalizer	22	16h	[4]	pd_ctrl	1	1'b1		
	pd_ldo	Powers down internal LDO when set to HIGH	22	16h	[5]	pd_ctrl	1	1'b0	Must drive VDDA1P8_PLL_REG when LDO is powered down	
	pd_bgr	Powers down Bandgap references	22	16h	[6]	pd_ctrl	1	1'b0	Must drive BGR_AFE and BGR_TX pins when BGR is powered down	
	pd_tx<5:0>	Powers down TX block X	22	16h	[13:8]	pd_ctrl	6	6'b0		
	pd_vcobuffer	Powers down readback of HF clock	22	16h	[14]	pd_ctrl	1	1'b0		
	pd_readbackclk_mon	Powers down readback clock (refclk or fbclk)	22	16h	[15]	pd_ctrl	1	1'b0		
	pd_analog_channel<23:0>	Powers down ADC X (and PGA X)	23,24	17h,18h	[15:0] -> [15:0] +[7:0] -> [23:16]	pd_adc_ctrl_{0,1}	24	24'b0	Uses two full SPI registers	0x0000_0000
	reserved for later use		25	19h						0
JESD204B										
	jesd_numlanes	Number of lanes	26	1Ah	[1:0]	jesd_config	2	2'b10	`define LANES12 2'b11 `define LANES6 2'b10 `define LANES4 2'b01 `define LANES3 2'b00	0x56AA
	jesd_ds_en	Scramble enable	26	1Ah	[2]	jesd_config	1	1'b0		
	jesd_cr_en	Character Replacement Enable	26	1Ah	[3]	jesd_config	1	1'b1		
	jesd_bid	BID (Bank ID)	26	1Ah	[7:4]	jesd_config	4	4'b1010		
	jesd_did	DID (Device ID)	26	1Ah	[15:8]	jesd_config	8	8'h56		
	jesd_testmode	JESD204B test signals	27	1Bh	[2:0]	jesd_test	3	3'b000	0 Normal operation 1 Send /K/ 2 infinite ILAS loop 3 Send /K28.7/ 4 Send /D21.5/ 5 Send modified RPAT	0x0000
	reserved	JESD204B test signals	27	1Bh	[3]	reserved	1	1'b0	keep at zero	
	jesd_datasel	Fake ADC data (fixed pattern, ramp, LFSR)	27	1Bh	[5:4]	jesd_test	2	2'b00	`define TESTMODE_ADC 2'd0 `define TESTMODE_CONSTANT 2'd1 `define TESTMODE_RAMP 2'd2 `define TESTMODE_LFSR 2'd3	

Block	Signal Name	Description	Register	Register Hex	SPI bits <?:0>	Functional Name	# of bits	Defaults	NOTE	SPI DEFAULTS
	jesd_reset	JESD204B reset source	27	1Bh	[7:6]	jesd_test	2	2'b00	0: PLL lock or reset_n 1: assert reset 2: deassert reset	
	jesd_testval	Fake ADC 0 data value	28	1Ch	[11:0]	jesd_fake_adc[0]	12	64		0x0040
	jesd_testval	Fake ADC 1 data value	29	1Dh	[11:0]	jesd_fake_adc[1]	12	128		0x0080
	jesd_testval	Fake ADC 2 data value	30	1Eh	[11:0]	jesd_fake_adc[2]	12	192		0x00C0
	jesd_testval	Fake ADC 3 data value	31	1Fh	[11:0]	jesd_fake_adc[3]	12	256		0x0100
	jesd_testval	Fake ADC 4 data value	32	20h	[11:0]	jesd_fake_adc[4]	12	320		0x0140
	jesd_testval	Fake ADC 5 data value	33	21h	[11:0]	jesd_fake_adc[5]	12	384		0x0180
	jesd_testval	Fake ADC 6 data value	34	22h	[11:0]	jesd_fake_adc[6]	12	448		0x01C0
	jesd_testval	Fake ADC 7 data value	35	23h	[11:0]	jesd_fake_adc[7]	12	512		0x0200
	jesd_testval	Fake ADC 8 data value	36	24h	[11:0]	jesd_fake_adc[8]	12	576		0x0240
	jesd_testval	Fake ADC 9 data value	37	25h	[11:0]	jesd_fake_adc[9]	12	640		0x0280
	jesd_testval	Fake ADC 10 data value	38	26h	[11:0]	jesd_fake_adc[10]	12	704		0x02C0
	jesd_testval	Fake ADC 11 data value	39	27h	[11:0]	jesd_fake_adc[11]	12	768		0x0300
	jesd_testval	Fake ADC 12 data value	40	28h	[11:0]	jesd_fake_adc[12]	12	832		0x0340
	jesd_testval	Fake ADC 13 data value	41	29h	[11:0]	jesd_fake_adc[13]	12	896		0x0380
	jesd_testval	Fake ADC 14 data value	42	2Ah	[11:0]	jesd_fake_adc[14]	12	960		0x03C0
	jesd_testval	Fake ADC 15 data value	43	2Bh	[11:0]	jesd_fake_adc[15]	12	1024		0x0400
	jesd_testval	Fake ADC 16 data value	44	2Ch	[11:0]	jesd_fake_adc[16]	12	1088		0x0440
	jesd_testval	Fake ADC 17 data value	45	2Dh	[11:0]	jesd_fake_adc[17]	12	1152		0x0480
	jesd_testval	Fake ADC 18 data value	46	2Eh	[11:0]	jesd_fake_adc[18]	12	1216		0x04C0
	jesd_testval	Fake ADC 19 data value	47	2Fh	[11:0]	jesd_fake_adc[19]	12	1280		0x0500
	jesd_testval	Fake ADC 20 data value	48	30h	[11:0]	jesd_fake_adc[20]	12	1344		0x0540
	jesd_testval	Fake ADC 21 data value	49	31h	[11:0]	jesd_fake_adc[21]	12	1408		0x0580
	jesd_testval	Fake ADC 22 data value	50	32h	[11:0]	jesd_fake_adc[22]	12	1472		0x05C0
	jesd_testval	Fake ADC 23 data value	51	33h	[11:0]	jesd_fake_adc[23]	12	1536		0x0600
						TOTAL CONFIG BITS	549			