Study of Analog to Digital convertor (ADC) and Digital to Analog Convertor (DAC)

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Digital-to-Analog Converter (DAC) and Analog-to-Digital Converter (ADC) circuits were analysed in this experiment. A 3-bit and a 4-bit R–2R ladder DAC using an operational amplifier were implemented, and a 2-bit comparator-based ADC was made. The output characteristics were measured and compared with theoretical predictions. Linear fits were used to examine the linearity of the converters, and the accuracy of the DACs was quantified using RMS errors. The results show good agreement with theory, with small deviations attributed to component tolerances and circuit non-idealities. This experiment provides practical insight into signal conversion between analog and digital domains, which is fundamental to modern measurement and instrumentation systems.

I. OBJECTIVE

1. To construct and study DAC and ADC.
2. To design a 3-bit and a 4-bit R/2R ladder DAC using a 741 op amp and test the circuit.
3. To construct an ADC circuit to convert a 2-bit digital input to an anolog output

II. THEORY

Modern digital systems process information in binary form, while most physical quantities such as temperature, light intensity, and voltage are analog in nature. Therefore, interface circuits are required to convert signals between these two domains. A Digital-to-Analog Converter (DAC) converts a digital (binary) input into a corresponding analog voltage, whereas an Analog-to-Digital Converter (ADC) performs the reverse operation by converting an analog voltage into a digital code.

A. Digital-to-Analog Converter (DAC)

A DAC generates an analog output voltage proportional to a given digital input word. A simple weighted-resistor DAC requires resistors of many different precise values, which becomes impractical for higher-bit resolution. To overcome this limitation, the R–2R ladder network is commonly used [1].

The R–2R ladder DAC (see Fig. 1) employs only two resistor values, R and $2R$, arranged in a ladder structure. Each digital input bit controls a switch that connects either to a reference voltage (logic 1) or to ground (logic 0). The ladder network ensures that each bit contributes a properly weighted fraction of the reference voltage to the output, with the most significant bit (MSB) contributing the largest weight and the least significant bit (LSB) the smallest.

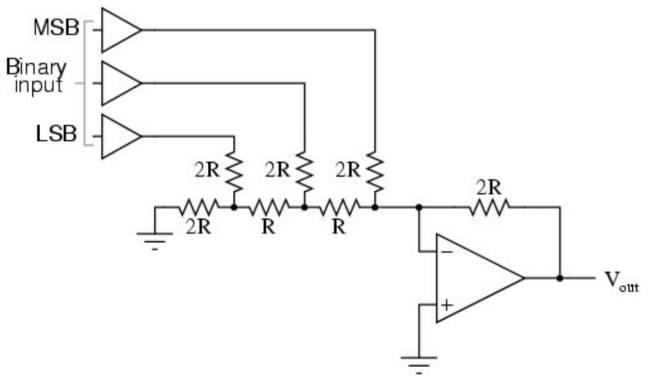

FIG. 1. Circuit diagram of the R–2R ladder DAC using an operational amplifier for digital-to-analog conversion.

When the R–2R ladder DAC with n-bit input is connected to an inverting operational amplifier, the output voltage is given by

$$V_{\text{out}} = -\frac{R_f}{R}\left(\frac{d_1}{2^1} + \frac{d_2}{2^2} + \frac{d_3}{2^3} + \cdots + \frac{d_n}{2^n}\right), \qquad (1)$$

where $d_1, d_2, \ldots, d_n$ are the digital input bits (each 0 or 1), with d_1 as the MSB, and R_f is the feedback resistance of the operational amplifier. For the common choice $R_f = 2R$, the output voltage becomes directly proportional to the binary input number.

An advantage of the R–2R ladder DAC is that its output impedance = R (constant), independent of the number of bits. This simplifies the design of subsequent analog stages such as filtering or amplification circuits.

The performance of a DAC is characterized by the following parameters:

- **Resolution**: The smallest change in output voltage corresponding to a one-bit change in the input.

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- **Accuracy**: The closeness of the actual output to the ideal value.
- **Linearity**: The degree to which the output follows a linear relationship with the input.
- **Monotonicity**: The property that the output strictly increases with respect to the input.
- **Settling Time**: The time required for the output to become stable after a change in input.

B. Analog-to-Digital Converter (ADC)

An ADC converts a continuous analog voltage into a discrete digital code.Here, the analog input voltage is compared with a set of reference voltages using comparators. Each comparator produces a digital output indicating whether the input voltage is greater or smaller than its reference level.

The set of comparator outputs forms a code, which is then converted into a binary code using a priority encoder. The priority encoder assigns a binary number corresponding to the highest active comparator output, thereby providing the digital representation of the analog input voltage.

For an n-bit ADC, $2^n - 1$ comparators are required, each with a distinct reference voltage. This architecture offers very fast conversion since all comparisons are performed simultaneously. However, the required number of comparators increases rapidly with resolution, making this method hardware-intensive for higher-bit ADCs.

The main advantage of the ADC is its high speed while its main disadvantages are increased circuit complexity and power consumption at higher resolutions.

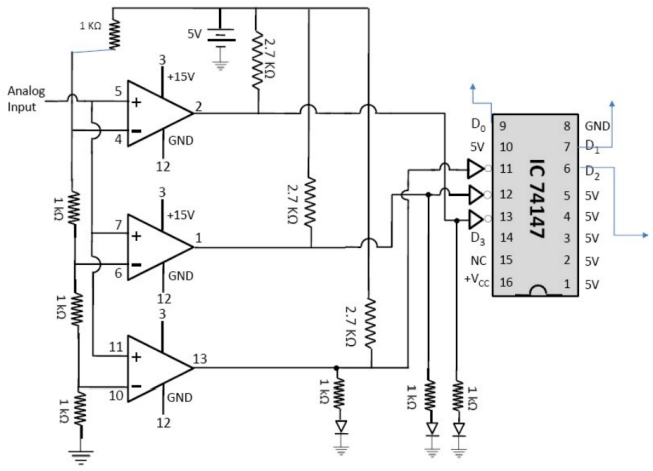

FIG. 2. Circuit diagram of the comparator-based 2-bit ADC using a priority encoder for analog-to-digital conversion.

C. Conversion of Binary display to Decimal display

After converting analog voltage to binary number, further it can be converted to binary coded decimal and displayed on a BCD display. IC 7447 is used to convert binary to BCD display. 7447 is an input active high IC and output active low IC. We use the Common Anode BCD display, which is input active low.

III. APPARATUS REQUIRED

IC 741 Op-Amp, LM339 Comparator, 74LS147 Priority Encoder, 7447 Decoder (optional), Seven Segment Display (optional), resistors (R, 2R, 1 kΩ, 3 kΩ, 330 Ω), DC power supply, breadboard, LEDs, connecting wires, and digital multimeter.

IV. OBSERVATIONS

TABLE I. Digital to Analog convertor (DAC) (3-bit)

S.no.	Digital Signal	Analog Signal (V)	Theoretical Value (V)
1.	000	-0.001	0
2.	001	-1.284	-1.285
3.	010	-2.569	-2.57
4.	011	-3.855	-3.855
5.	100	-5.10	-5.14
6.	101	-6.39	-6.425
7.	110	-7.68	-7.71
8.	111	-8.96	-8.995

TABLE II. Digital to Analog convertor (DAC) (4-bit)

S.no.	Digital Signal	Analog Signal (V)	Theoretical Value (V)
1.	0000	-0.001	0
2.	0001	-0.639	-0.6425
3.	0010	-1.282	-1.285
4.	0011	-1.924	-1.9275
5.	0100	-2.569	-2.57
6.	0101	-3.219	-3.2125
7.	0110	-3.857	-3.855
8.	0111	-4.50	-4.4975
9.	1000	-5.11	-5.14
10.	1001	-5.75	-5.7825
11.	1010	-6.39	-6.425
12.	1011	-7.04	-7.0675
13.	1100	-7.68	-7.71
14.	1101	-8.32	-8.3525
15.	1110	-8.96	-8.995
16.	1111	-9.61	-9.6375

TABLE III. Analog to Digital Converter (ADC) (2-bit)

S.no.	Analog input (V)	Digital Output	BCD Display
1.	0	00	0
2.	1.3	01	1
3.	2.6	10	2
4.	3.8	11	3

V. DATA ANALYSIS

For the DAC (3-bit and 4-bit) and the 2-bit ADC, the measured analog output (or digital code for ADC) was plotted as a function of the corresponding digital (or analog) input. A least-squares linear fit was performed in each case to examine the linearity of the conversion.

We fit the observed data-points $\{x_i, y_i\}$ into a form,

$$y = mx + c$$

The statistical error calculated in linear fit is done using the following formulae [2],

$$\sigma_y = \sqrt{(\sum_i \frac{(y_n - y_i)^2}{N-2})} \tag{2}$$

Errors in slope and intercept,

$$\Delta m = \sigma_y \sqrt{\frac{\sum_i x_i^2}{((N\sum_i x_i^2) - (\sum_i x_i)^2)}} \tag{3}$$

$$\Delta c = \sigma_y \sqrt{\frac{N}{((N\sum_i x_i^2) - (\sum_i x_i)^2)}} \tag{4}$$

The linear plots obtained are shown in Fig. 3,4 and 6.

A. Digital to Analog Convertor (DAC)

The slope obtained from the linear fit are,

$$\text{3-bit DAC, } m_1 = -1.279 \pm 0.002$$
$$\text{4-bit DAC, } m_2 = -0.640 \pm 0.001$$
$$\text{2-bit ADC, } m_3 = +0.787 \pm 0.011$$

Deviations of the measured points from the fitted line arise mainly due to resistor tolerances, op-amp offset, and supply variations.

The accuracy of each conversion was quantified using the root-mean-square (RMS) error between the measured values and the theoretical values (obtained by the Eq. (1)). The obtained RMS errors are given by,

$$RMS = \sqrt{\frac{1}{N}(\sum_i (V^i_{obs.} - V^i_{theoretical})^2)} \tag{5}$$

We obtained the RMS errors to be 0.0249 and 0.0223 for 3-bit DAC and 4-bit DAC respectively.

The RMS errors were found to be small compared to the full-scale output, indicating reasonable agreement with the ideal behavior.

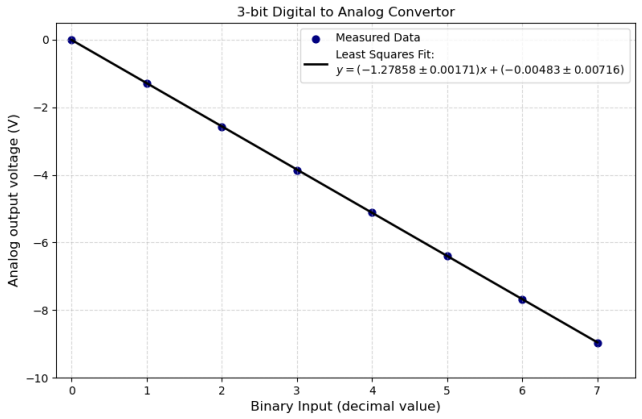

FIG. 3. Least-squares linear fit of analog output voltage versus digital input code for the 3-bit DAC.

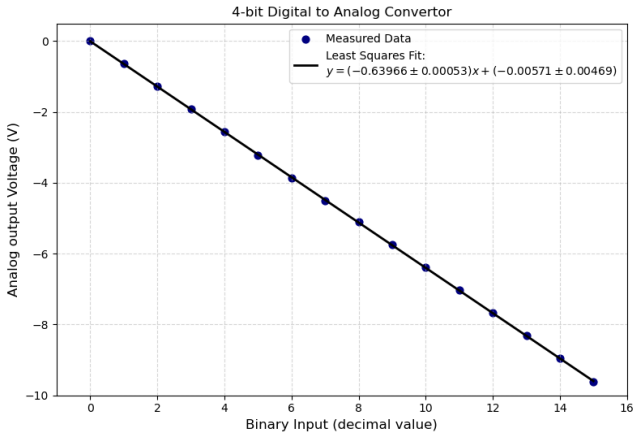

FIG. 4. Least-squares linear fit of analog output voltage versus digital input code for the 4-bit DAC.

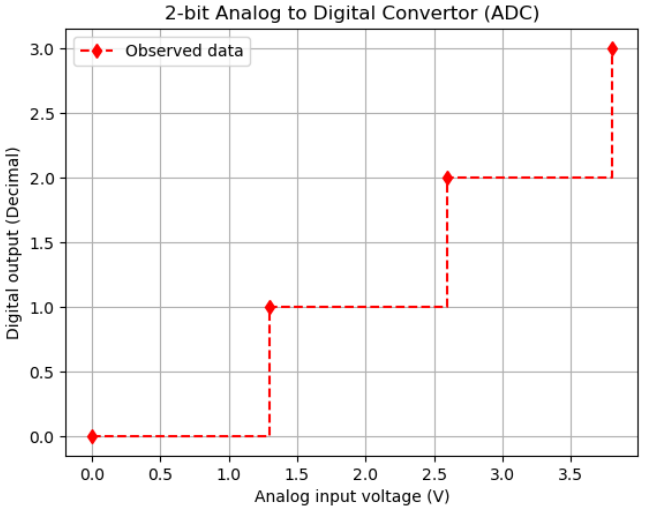

FIG. 5. Step-wise transfer characteristic of the 2-bit ADC showing digital output code as a function of the analog input voltage.

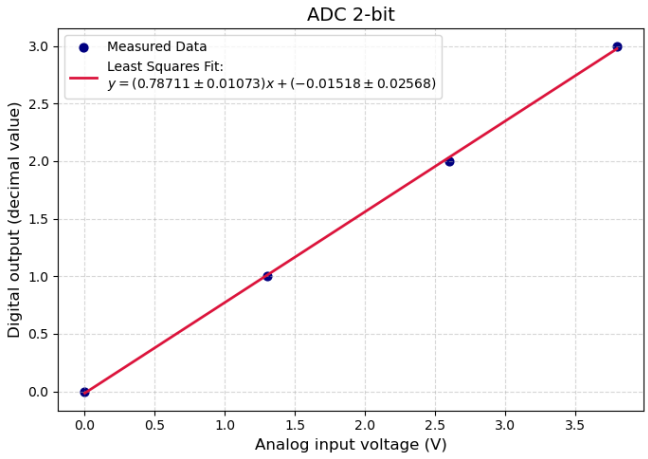

FIG. 6. Linear fit of digital output code versus analog input voltage for the 2-bit ADC.

B. Analog to Digital Convertor (ADC)

For the 2-bit ADC, the digital output code was plotted as a function of the analog input voltage and fitted with a straight line to examine the overall linearity of the conversion. Although the ideal transfer characteristic of an ADC is step-wise due to quantization (see Figure 5), the linear fit estimates the effective gain of the converter and verifies the linearity.

All code related to the plot, fitting and calculations is available on this Github Repository [3].

VI. RESULTS AND DISCUSSION

The measured output voltages of the 3-bit and 4-bit R–2R ladder DACs show good agreement with the theoretical values. The plots of analog output versus digital input exhibit an approximately linear behaviour, as confirmed by least-squares fitting. The obtained slopes, $m_1 = -1.279 \pm 0.002$ for the 3-bit DAC and $m_2 = -0.640 \pm 0.001$ for the 4-bit DAC, are consistent with the expected scaling, with the negative sign arising from the inverting amplifier configuration.

The RMS errors were found to be 0.0249 V and 0.0223 V for the 3-bit and 4-bit DAC, respectively, which are small compared to the full-scale output, indicating good accuracy of the converters. The remaining deviations are attributed to resistor tolerances, op-amp offset, and supply variations.

For the 2-bit ADC, the digital output code varies linearly with the analog input voltage with a slope, $m_3 = +0.787 \pm 0.011$. Although the ideal transfer characteristic is step-wise due to quantization, the linear fit verifies the overall linear trend and correct operation of the ADC. Minor deviations arise from comparator offsets and reference voltage uncertainties.

VII. CONCLUSION

The 3-bit and 4-bit R–2R ladder DACs and the 2-bit comparator-based ADC were constructed and tested. The DACs exhibit good linearity and small RMS errors, showing close agreement with theoretical predictions. This experiment verifies the basic principles of digital-to-analog and analog-to-digital conversion and illustrates the effects of finite resolution and circuit non-idealities.

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[2] John R. Taylor. *An Introduction to Error Analysis: The Study of Uncertainties in Physical Measurements*. University Science Books, Sausalito, CA, 2nd edition, 1997.

[3] Aryan Shrivastava. P341 - nuclear physics and instrumentation lab. `https://github.com/crimsonpane23/P341-Nuclear-Physics-and-Instrumentation-Lab.git`, 2026.