Synopsys Users Group
SINGAPORE 2011

Fast Forward with In-Design Lithography DFM using DRC+ in Synopsys ICC / ICV

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Agenda

- DFM Challenges to Lithography
- Conventional Approach to Litho DFM Design Flow
- Design Fast forward using DRC+ in In-Design Flow
- DRC+ ICV Pattern Matching : Detection and Fixing
- Conclusion

Agenda

- DFM Challenges to Lithography
  - Physical Design Dependent Yield
  - More Rules, Increasing Complexity
- Conventional Approach to Litho DFM Design Flow
- Design Fast forward using DRC+ in In-Design Flow
- DRC+ ICV Pattern Matching : Detection and Fixing
- Results
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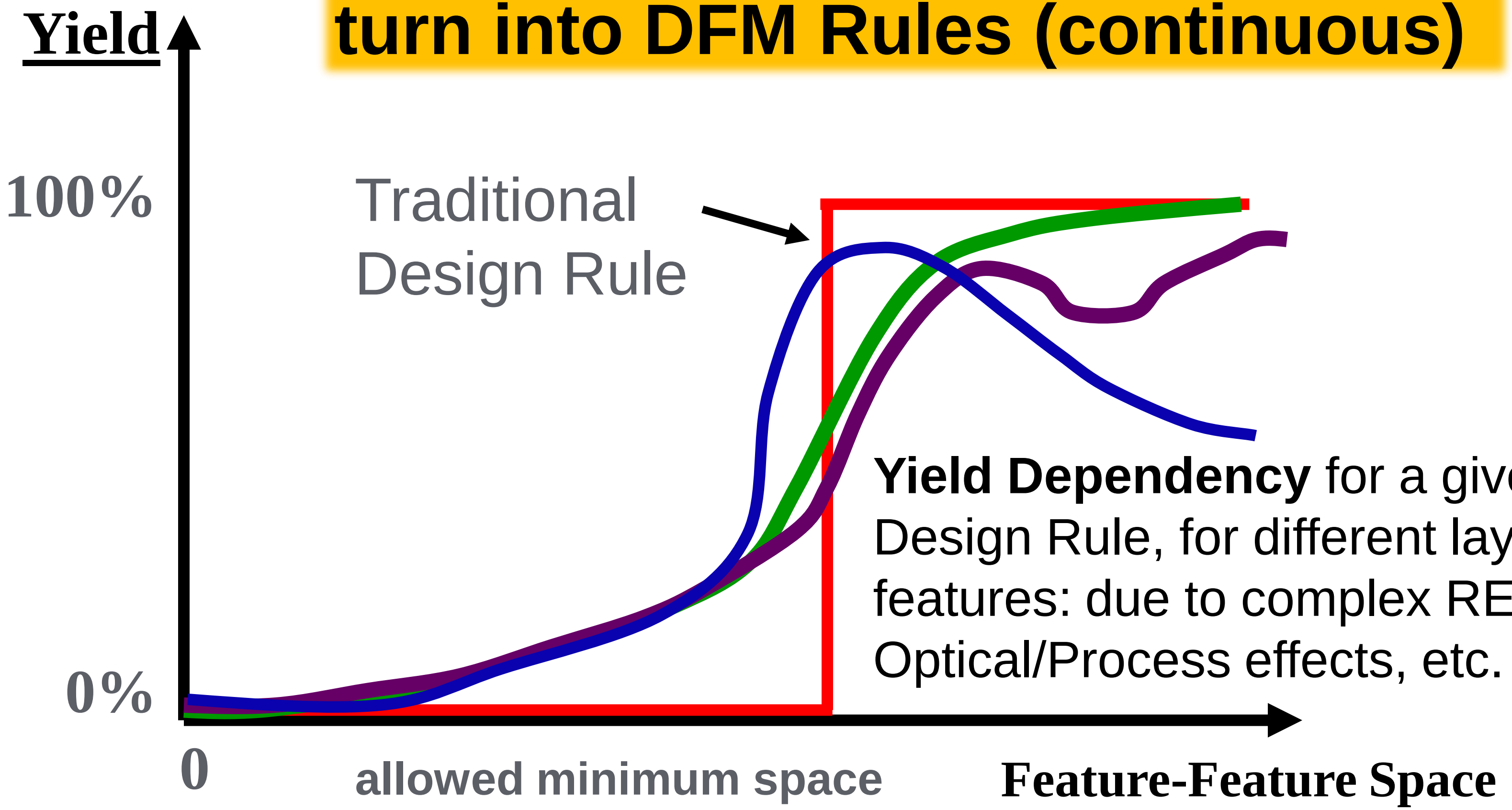
DFM Challenges: 28nm and below
Physical Design dependent Yield

Ground Rules (binary) …
turn into DFM Rules (continuous)

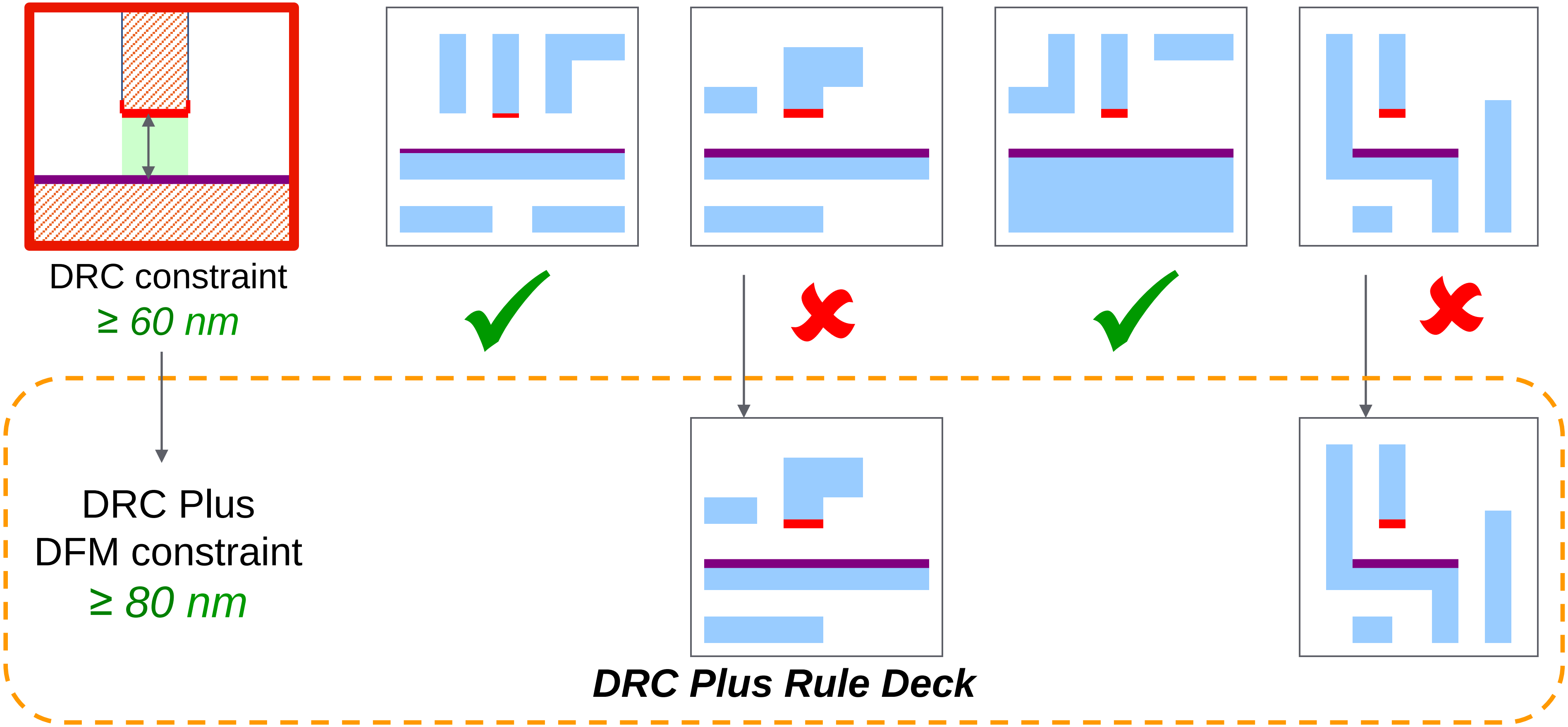


Yield Dependency for a given Design Rule, for different layout features: due to complex RET/OPC, Optical/Process effects, etc.

Dr. Luigi Capodieci, Director of DFM, GLOBALFOUNDRIES, GTC 2010

DFM Challenges: 28nm and below Physical Design dependent Yield

Configuration: tip-to-side



DRC constraint

≥ 60 nm

DRC Plus

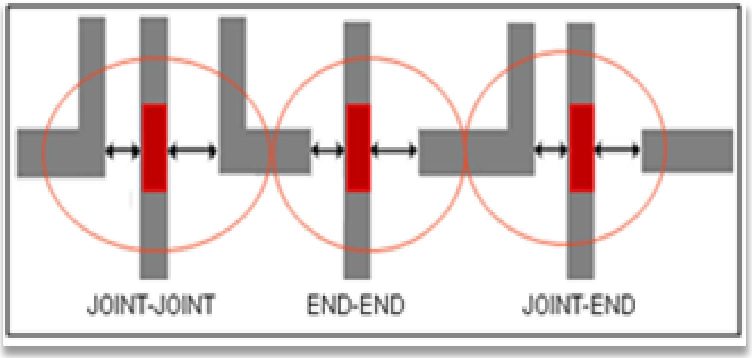
DFM constraint

≥ 80 nm

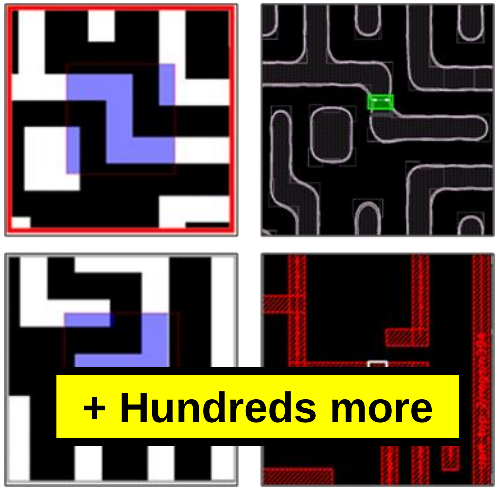
DRC Plus Rule Deck

DFM Challenges: More Rules…

- Not all DFM critical layout patterns can easily and rightfully be translated into design rules.



Few DFM Critical patterns supported by Design Rules

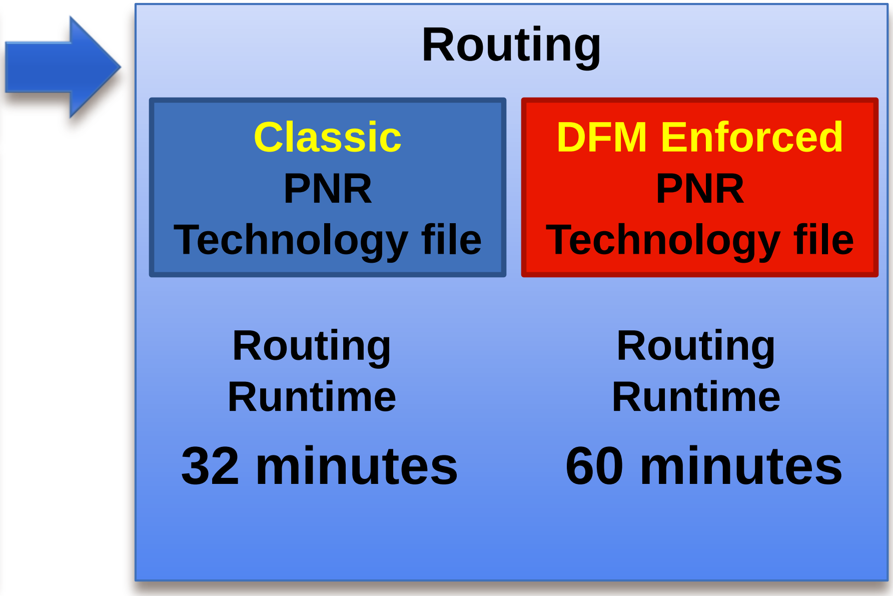


Hundreds more DFM patterns needs to be supported

DFM Challenges: Increasing Complexity

- DFM routing rules: pessimistic and restrictive.
- Significant impact on routing runtime.

Placed Design	
Chip Area	0.041 mm^2
Core Area	0.037 mm^2 (192µm x 192µm)
Std. Cell Density (Cell Utilization)	82.26%
Instance Count	~ 25 K



Routing

Classic PNR Technology file	DFM Enforced PNR Technology file
Routing Runtime	Routing Runtime
32 minutes	60 minutes

Agenda

- DFM Challenges
- Conventional Approach to Litho DFM Design Flow
  - Implement then Verify
  - Model Based Lithography Simulation
- Design Fast forward using DRC+ in In-Design Flow
- DRC+ ICV Pattern Matching : Detection and Fixing
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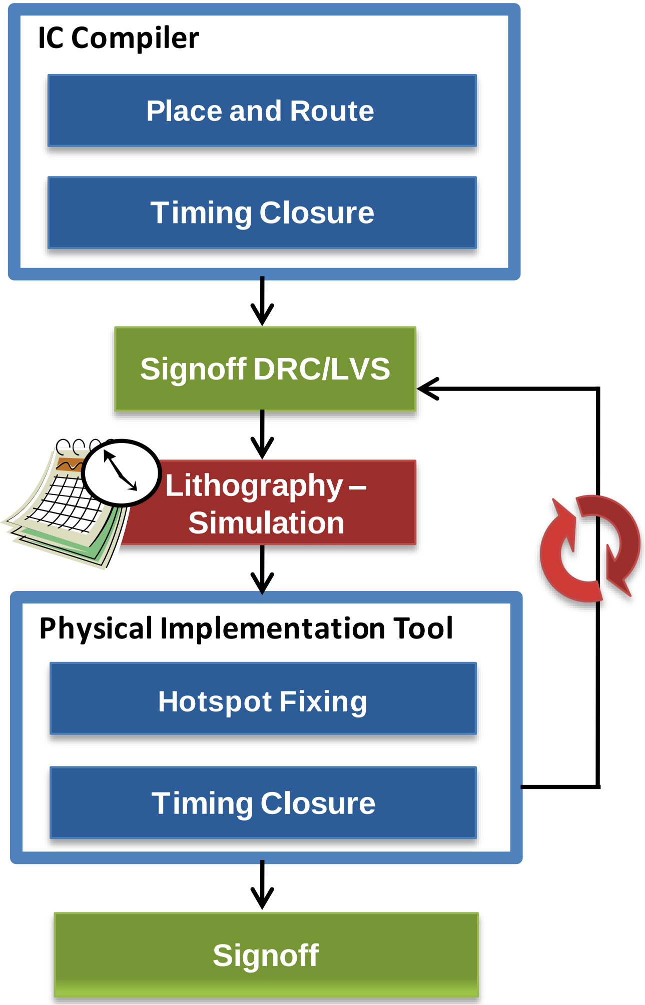
Conventional DFM Design Flow



Iterations due to DFM lithography simulations being done in late stage of design can result into tapeout delays

Design Iterations + Hours and Days of Model Based Lithography Simulation

Like digging a mountain until a rat comes out.

Conventional Design Flow Issues

- Late stage surprises: DFM Physical verification only at the end of design.
- GDS streaming-in and out
- Model Based Lithography Simulation –
  - time consuming stage.
- Pushing all DFM into Design rules cannot support all your DFM needs.

Agenda

- DFM Challenges
- Conventional Approach to Litho DFM Design Flow
- Design Fast forward using DRC+ in In-Design Flow
  - Ultra-Fast DRC+ Pattern-Matching in IC Validator
  - Seamless Integration With IC Compiler
- DRC+ ICV Pattern Matching : Detection and Fixing
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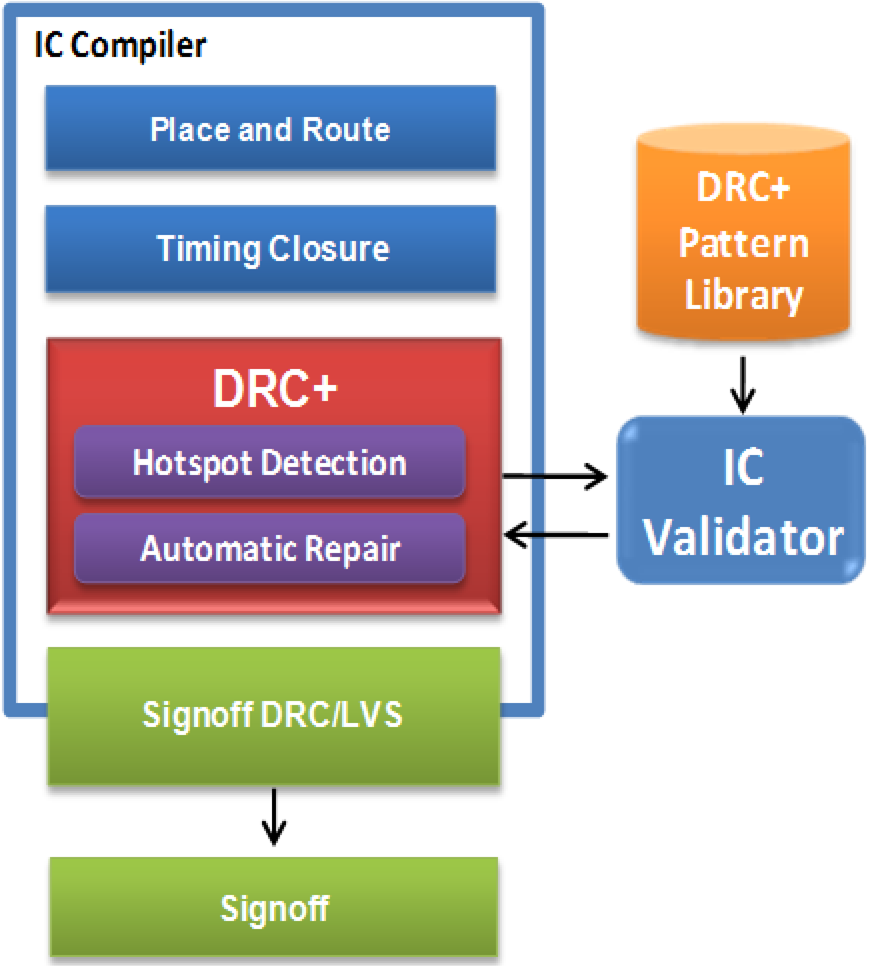
DRC+ in Integrated Design Flow



- Use Ultra-Fast DRC+ Pattern-Matching in IC Validator
- In-Design Automatic Fixing of Lithography Hotspots
- Address timing issues Immediately inside the design

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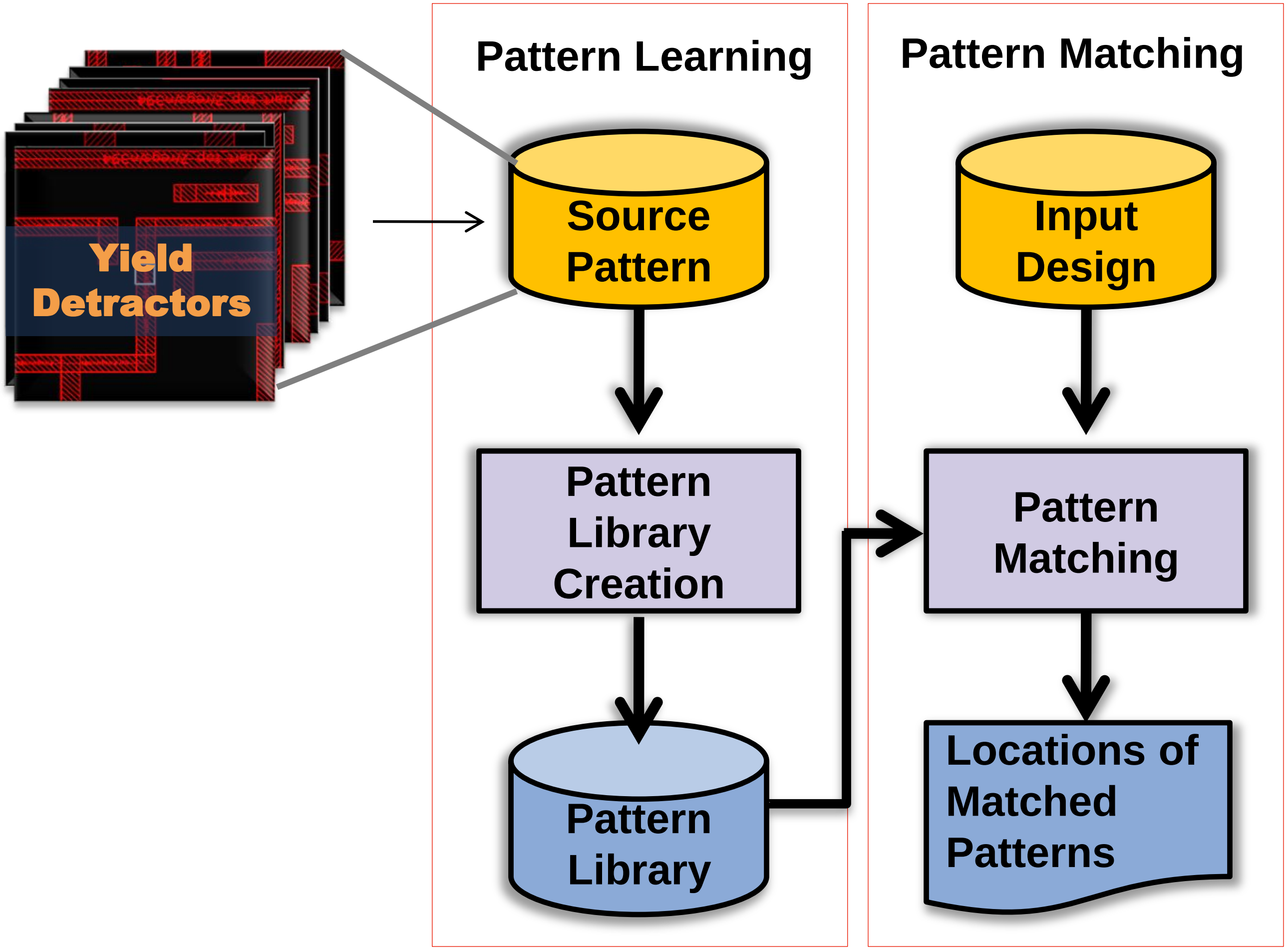
DRC+ ICV Pattern Matching Flow



Yield Detractors

Pattern Learning

Source Pattern

Pattern Library Creation

Pattern Library

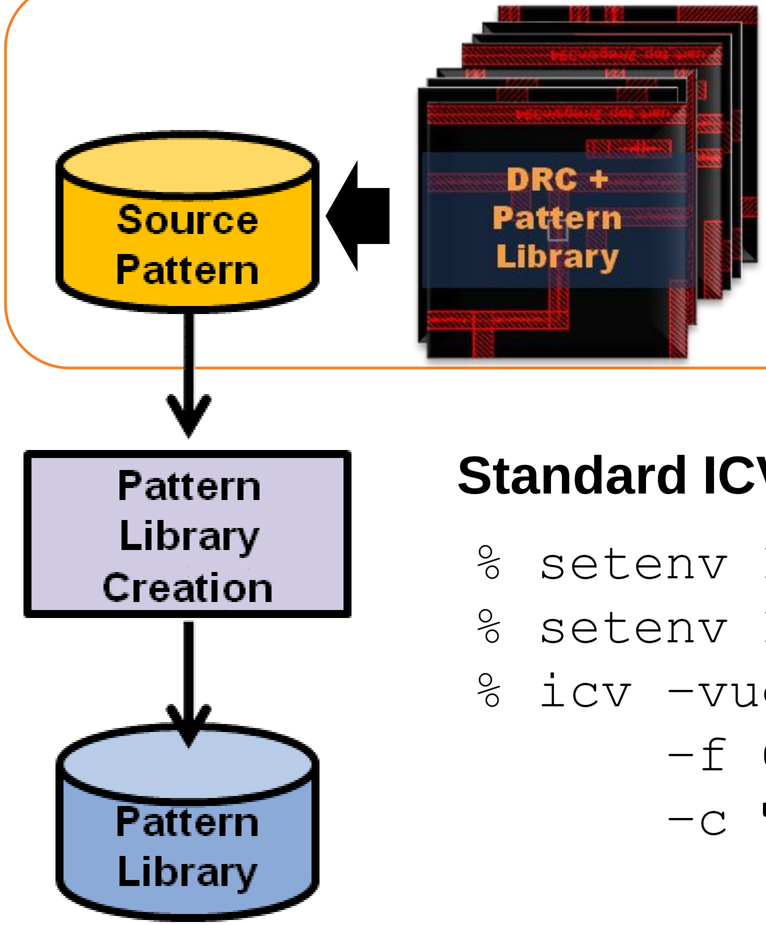
Pattern Matching

Input Design

Pattern Matching

Locations of Matched Patterns

ICV Pattern Library Preparation



Collection of foundry silicon correlated DRC+ lithography problematic patterns.

Standard ICV Execution

```
% setenv PM_LIB_PATH .
% setenv PM_LIB_NAME PATTERN_LIB
% icv -vue \
        -f GDSII-i pattern.gds \
        -c TOP learn.rs
```

ICV Pattern Library Preparation Runset Overview

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learn.rs

```
#define PM_RS
#include <icv.rh>
//*********************************************
//  Synopsys, Inc. All rights reserved.
//  Pattern Match Sample runset
//*********************************************
```

User Defined Environment Variables

```
#pragma envvar default PM_LIB_PATH "."
#pragma envvar default PM_LIB_NAME “PATTERN_LIB"
pattern_options (
pattern_library_path = $PM_LIB_PATH
);
```

Pattern Database Specific

```
library (
    format   = GDSII,
    library_name = pattern.gds,
    cell = TOP
);
```

Layout Number

```
metal : polygon_layer                 = assign ( {{3,0}} );
pattern_marker : polygon_layer  = assign ( {{4,0} , {5,0} } );
pattern_text_id : text_layer          = assign_text( {{6,0}};
```

Pattern Library Learn

```
tmp_violation @= {
@"UNMATCHED_pattern_marker";
pattern_learn (
pattern_library_layer = $PM_LIB_NAME,
pattern_layers = {metal},
pattern_marker = pattern_marker,
pattern_text_id = pattern_text_id,
match_ambit = {x.xx,x.xx,x.xx,x.xx},
pattern_fuzziness = PM_EDGE_UNIFORM,
uniform_fuzzy_size = x.xxx,
.....
              );
}
```

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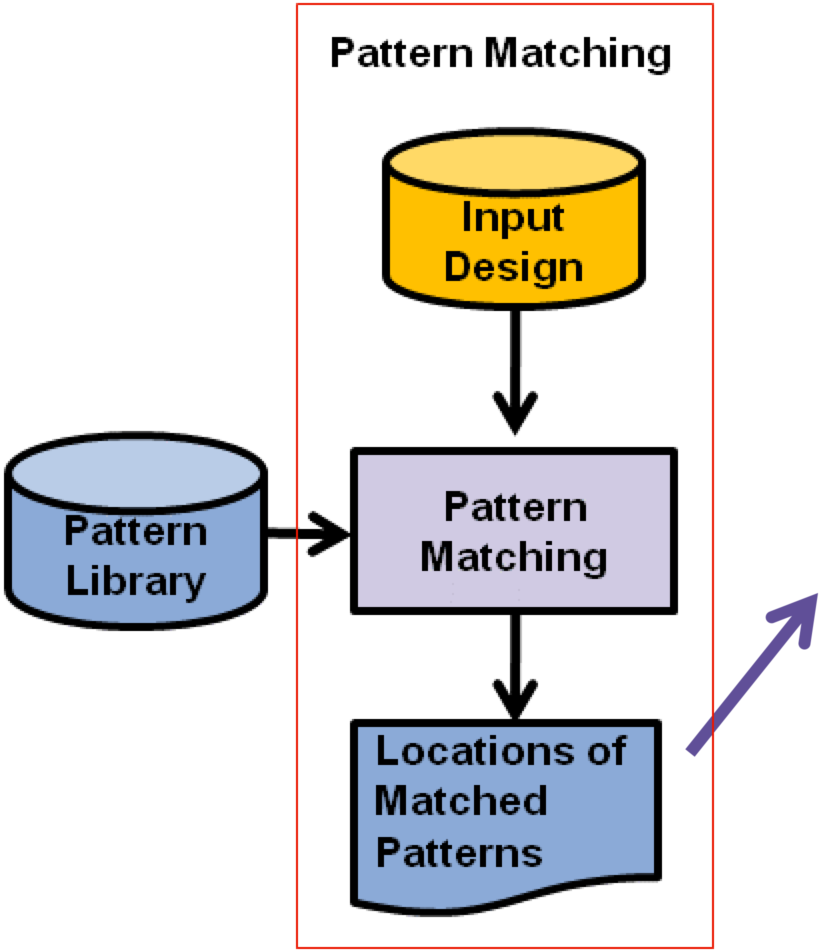
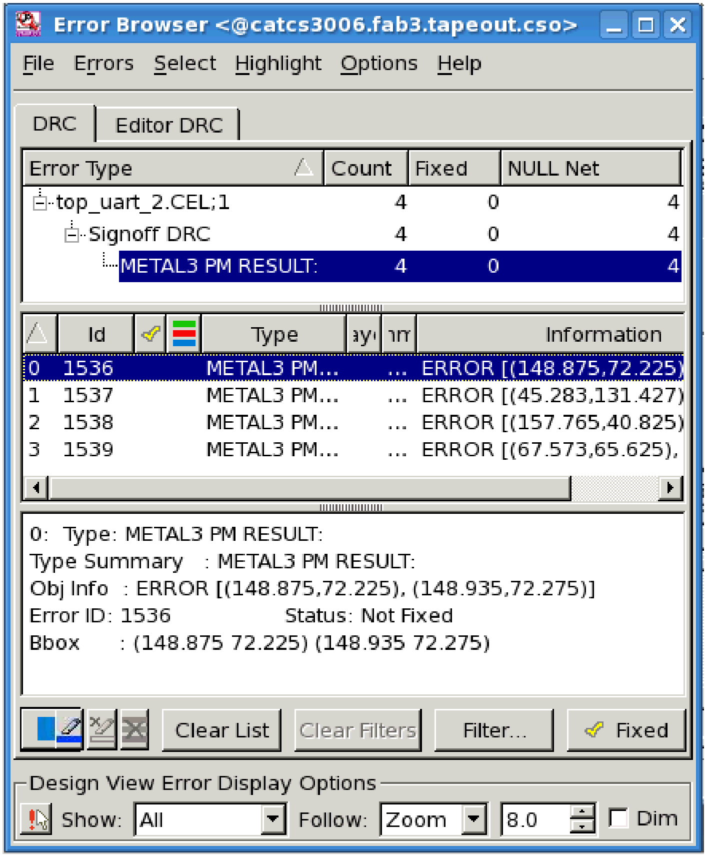
DRC+ ICV Pattern Matching Flow




Error Browser <@catcs3006.fab3.tapeout.cso>
File Errors Select Highlight Options Help
DRC
Editor DRC

Error Type	Count	Fixed	NULL Net
top_uart_2.CEL;1	4	0	4
Signoff DRC	4	0	4
METAL3 PM RESULT:	4	0	4

	Id	Type	ay	m	Information
0	1536	METAL3 PM...	...		ERROR [(148.875,72.225)
1	1537	METAL3 PM...	...		ERROR [(45.283,131.427)
2	1538	METAL3 PM...	...		ERROR [(157.765,40.825)
3	1539	METAL3 PM...	...		ERROR [(67.573,65.625),

```
0:  Type: METAL3 PM RESULT:
Type Summary   : METAL3 PM RESULT:
Obj Info   : ERROR [(148.875,72.225), (148.935,72.275)]
Error ID: 1536                Status: Not Fixed
Bbox       : (148.875 72.225) (148.935 72.275)
```

Show: All   Follow: Zoom   8.0   □ Dim

ICV Pattern Pattern Matching Runset Overview

match.rs

User Defined Environment Variables

```
#pragma envvar default PM_LIB_PATH "/pat_lib "
#pragma envvar default PM_LIB_NAME " PATTERN_LIB"
#pragma envvar default PM_TOP_MET "7"
…
pattern_options (
pattern_library_path = $PM_LIB_PATH
);
```

Design Layer Numbers

```
MET1 : polygon_layer = assign ( {{15,0}} );
MET2 : polygon_layer = assign ( {{17,0}} );
MET3 : polygon_layer = assign ( {{19,0}} );
MET4 : polygon_layer = assign ( {{21,0}} );
MET5 : polygon_layer = assign ( {{31,0}} );
MET6 : polygon_layer = assign ( {{44,0}} );
MET7 : polygon_layer = assign ( {{46,0}} );
```

```
metal_layer_list : list of polygon_layer =
  {MET1, MET2, MET3, MET4, MET5, MET6,
MET7};
```

Pattern Matching

```
for ( i = 0 to strtoi ( $PM_TOP_MET)-1) {
      layer_index : integer = i + 1;
       tmp_violation @= {@"M"+layer_index: ";

      pattern_match (
          pattern_library_layer = $PM_LIB_NAME,
          pattern_layers = {metal_layer_list[i]},);
}
}
……
```

Standard ICV Execution

```
% setenv PM_LIB_PATH .
% setenv PM_LIB_NAME PATTERN_LIB
% icv -vue -f GDSII -I design.gds -c top \
        match.rs
```

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Performance of DFM Verification : ICV Pattern Matching

Design Name	A	B	C	D	E	F	G	H
Chip Size (mm^2)	0.024	0.033	0.240	0.309	0.464	0.027	0.036	0.032
Core Size (mm^2)	0.023	0.031	0.115	0.294	0.440	0.026	0.035	0.030
Std Cell Density	85%	68%	56%	95%	64%	76%	60%	93%
Instance Count	18K	18.5K	83.5K	294K	303K	13.5K	14K	34K
DRC+ ICV Hotspots Found	14	8	35	199	133	1	1	11
Normalized Hotspots Found to 1mm^2	605	259	306	678	302	39	29	363

322 Lithography Hotspots / mm^2

- Consists of Design such as CPU and JPEG.
- Designs routed with different levels of design complexity.

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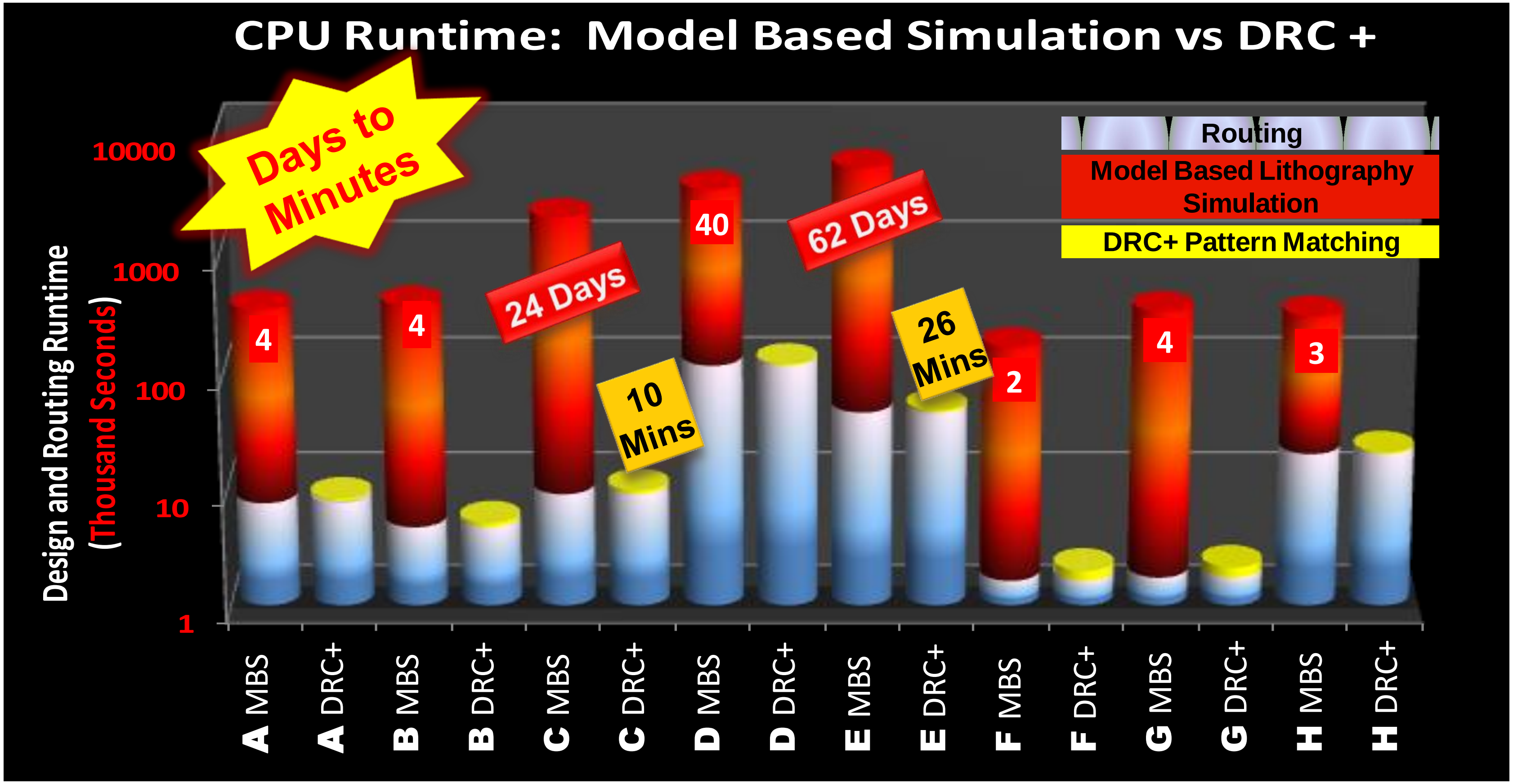
Performance of DFM Verification : ICV Pattern Matching

Design Name	A	B	C	D	E	F	G	H
DRC+ ICV Hotspots Found	14	8	35	199	133	1	1	11
Runtime: Multi-threading (8 threads) (minutes)	1.17	0.72	1.22	6.52	3.22	0.62	0.67	1.17
Runtime: Normalized to 1 thread (minutes)	9	6	10	52	26	5	5	9
Peak Memory (Mb)	71	55	102	314	324	38	37	80
Memory Usage (Mb)	248	248	248	248	247	248	247	247

Performance of DFM Verification : Printability Simulation vs. DRC+



- DRC+ is over 10,000 times faster than printability simulation
- DRC+ detection and fixing adds very little to the overall routing runtime

Performance of ICC In-Design Pattern Matching and Fixing

Design Name		I	J	K
Chip Size (mm²)		0.594	0.340	0.594
Core Size (mm²)		0.505	0.263	0.505
Std Cell Density		73.41%	77%	73.41%
Instance Count		364K	16K	364K
DRC+ ICV Hotspots Found		15	4	1335
Autofix Iteration Remaining Error	1	0	0	244
	2	-	-	163
	3	-	-	83
	4	-	-	83
DRC+ ICV Detection Fixing Runtime (seconds)		180	145	4800

DRC+ In-Design Pattern Matching Commands

- Setting Up the Physical Sign-Off Options

```
icc_shell> set_physical_signoff_options \
                    -exec_cmd icv \
                    -drc_runset match.rs
```

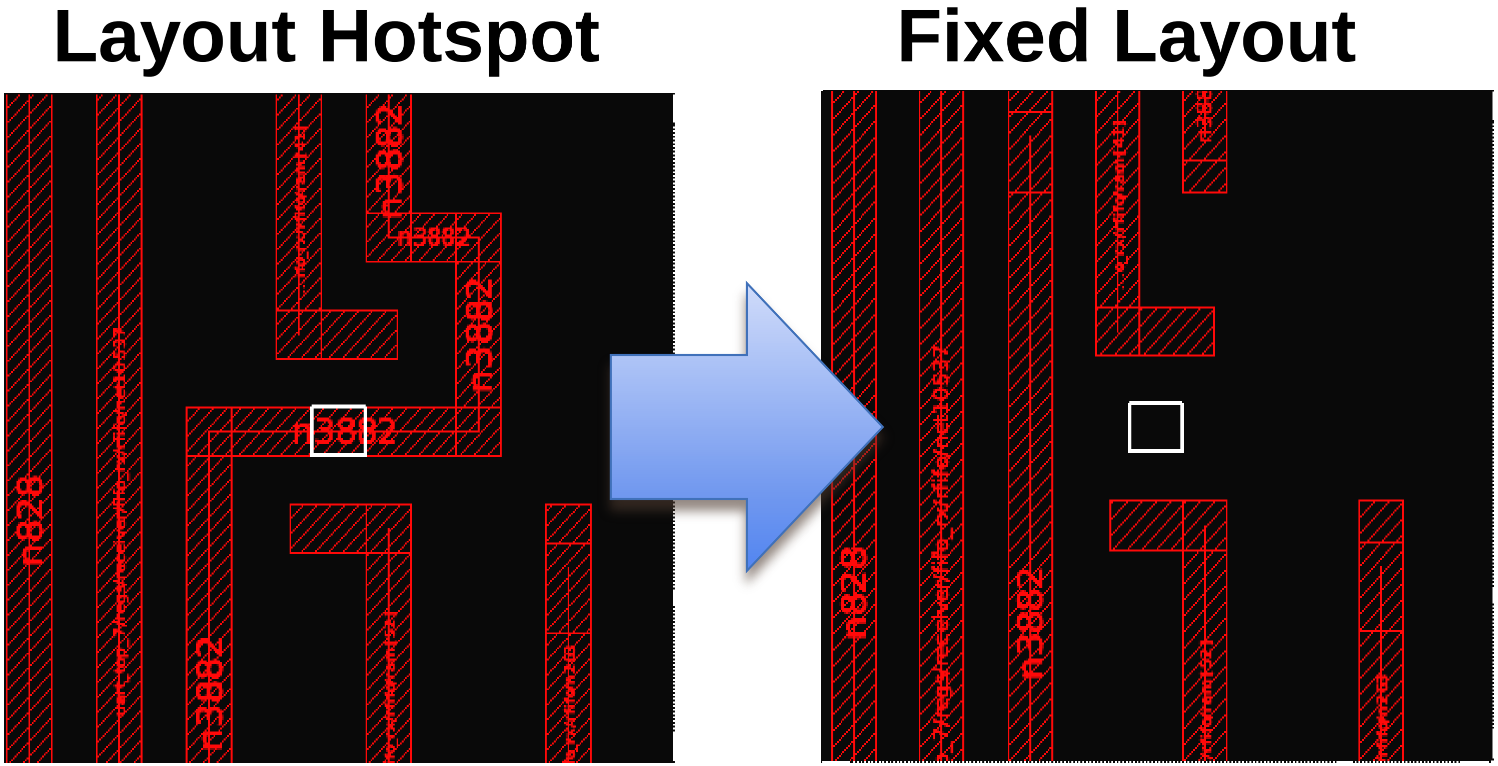
- Running Pattern-Matching for Hotspot Detection

```
icc_shell> signoff_drc \
                    -error_view s1_top_dummy_pm.err
```

- Automatically Fixing Hotspot Patterns

```
icc_shell> signoff_autofix_drc \
                    -config_file pm_layer.map \
                    -init_drc_error_db signoff_drc_run \
                    -keep_repair_loop_data true
```

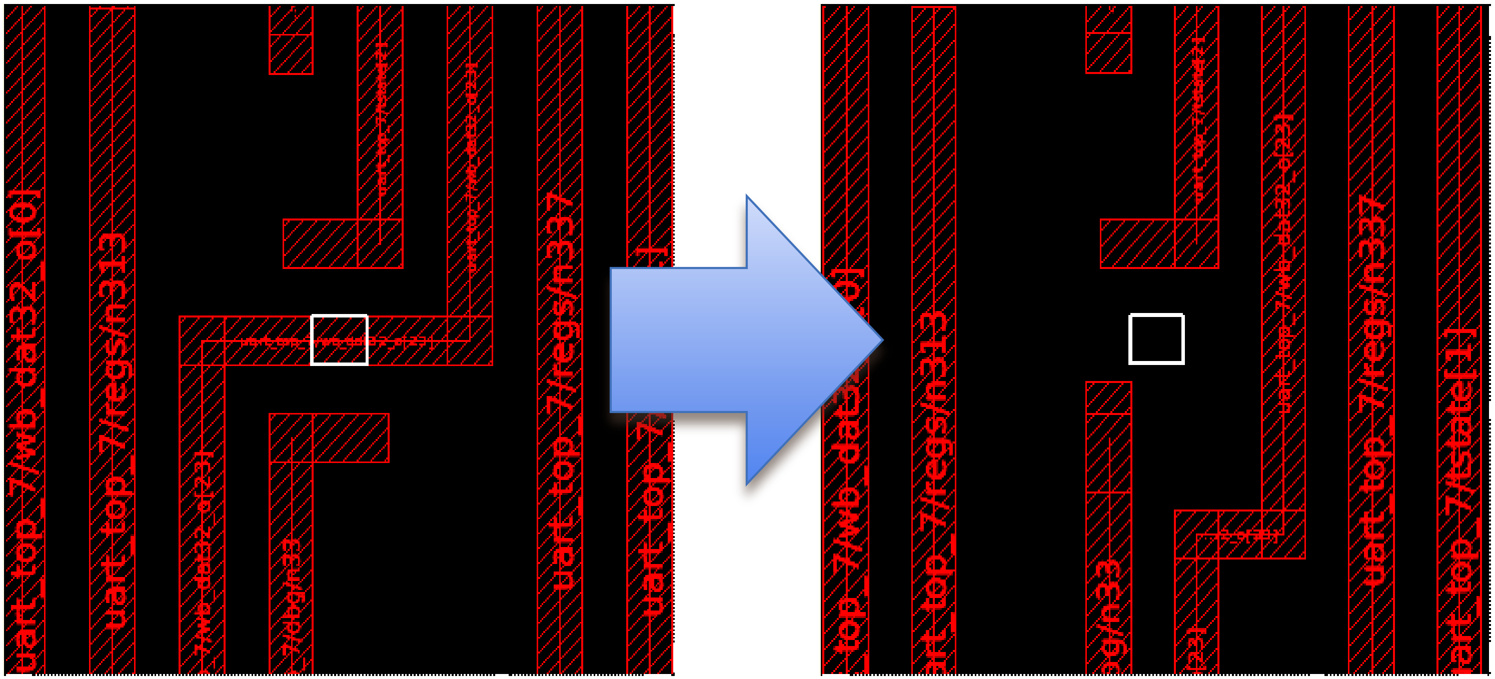
DRC+ Auto-fixing Results :1



Layout Hotspot

Fixed Layout

DRC+ Auto-fixing Results:2


Layout Hotspot

Fixed Layout

Timing Impact Analysis Results:

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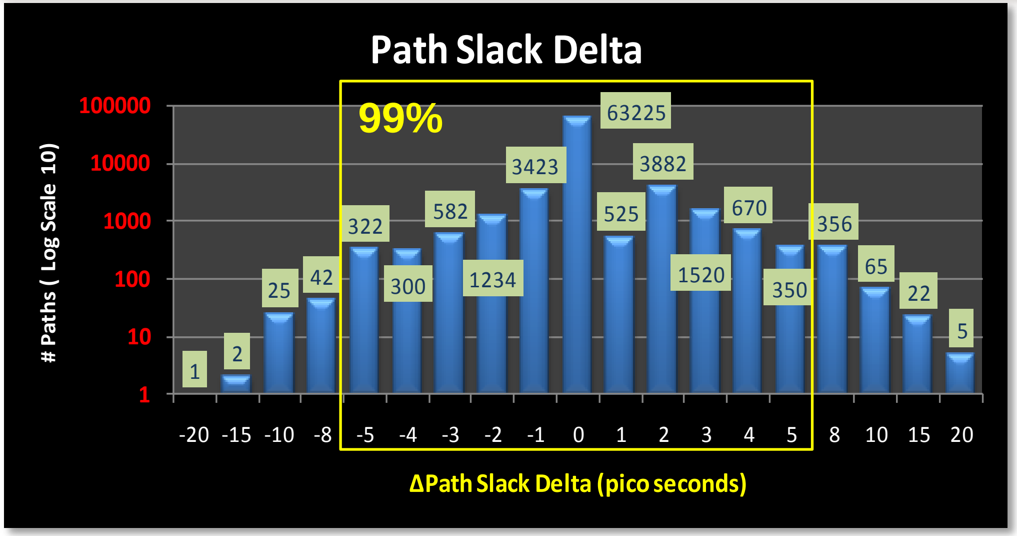

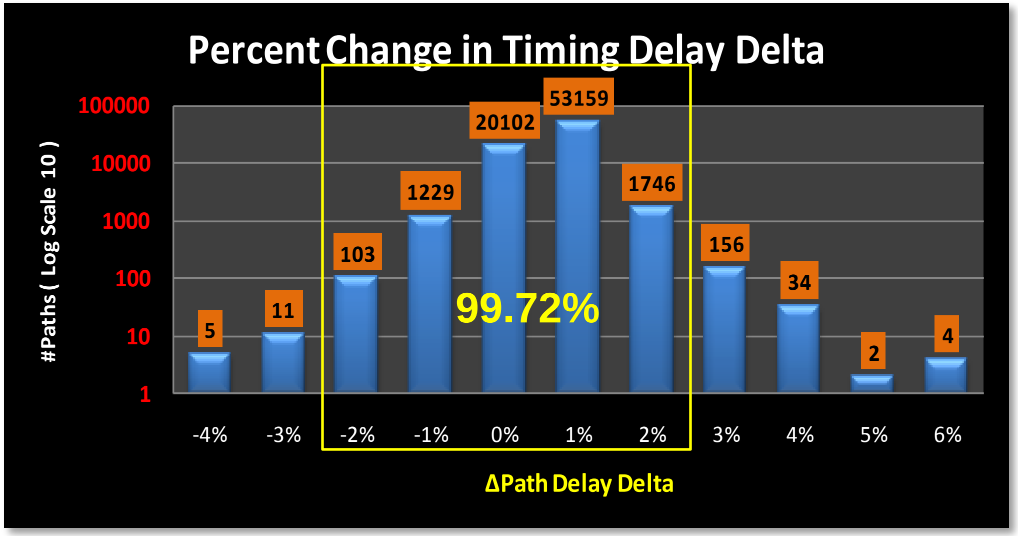

Design analyzed is with 1252 of 1335 hotspots violations fixed inside ICC with 4 Iterations.

- high fixing rate of 94% at 4th iteration with minimal timing impact.

- 99% of timing paths has timing delta of only ±5ps.

- 99.72% of the slack paths that changed have path slack changes of ± 2%.

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Conclusion

- DRC+
  - 28nm library of yield-critical patterns
    Industry first from GLOBALFOUNDRIES
- At 28nm and below, DFM is required for yield
- DRC+ in IN-DESIGN ICC/ICV
  - ICV PM 10,000 times faster than printability simulation
  - DFM physical verification integrated in the timing closure loop
  - Router Integrated Hotspots Detection and Fixing.
  - Ultra fast pattern matching engine minimizes cost to router runtime.

Acknowledgements
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Q & A

Thank You!

Now Your Time
Q&A Session