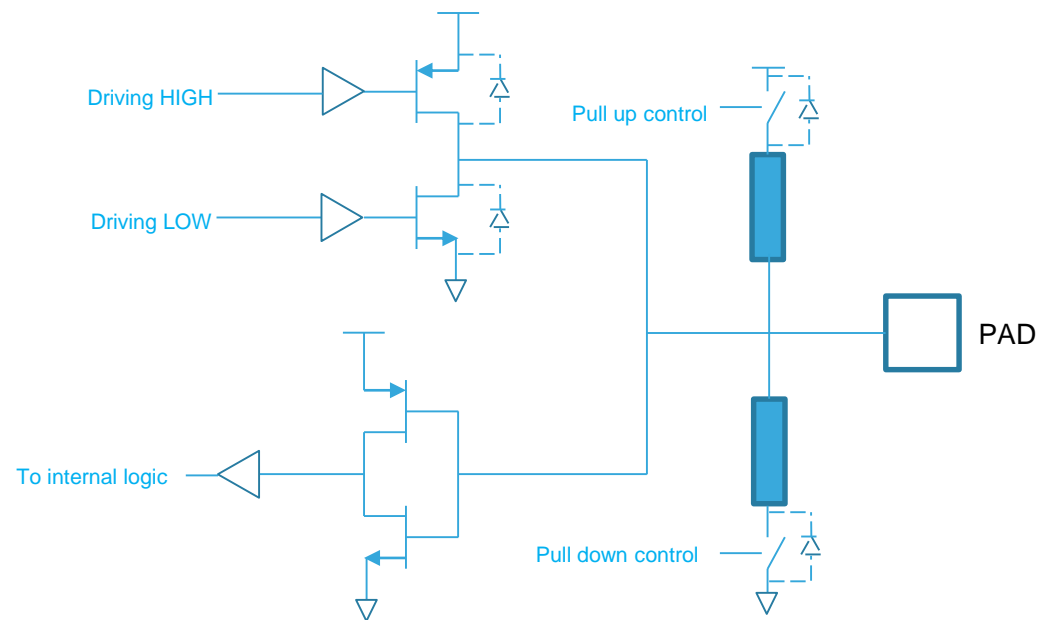# 5V tolerant IO

MCD application

life.augmented

- STM32s embed the 5V tolerant pads.

- Those pad can communicate 5V signaling, however it needs certain pre-caution and the external circuitry in some cases.

Ordinary CMOS IO structure

- The circuit is made with 3.3V technology transistors, which can accept up to 3.6V.
  - There is parasitic diode from PAD to VDD, GND to PAD. Pad voltage must be put in the -0.3V to the VDD + 0.3V (where parasitic diode does not become forward biased).
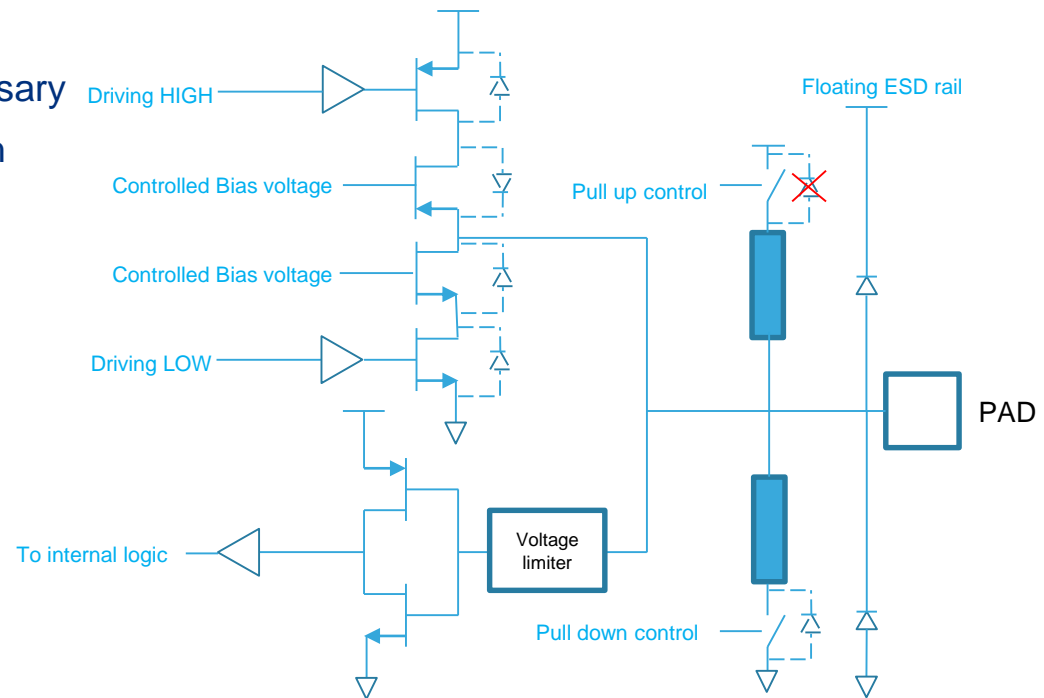
IO equivalent circuit

5V tolerant CMOS IO strucutre

- Thanks to the voltage limiter, even 5V is applied to pad, transistor does not get 5V directly to the input stage.

- For the output stage, cascoded transistor technique is used such that off transistor does not get the more than 3.6V on each terminal (gate/source/drain)
  - For the bias generation VDD is necessary
  - Pull up switch also use isolated switch

5V IO equivalent circuit

- ## In reality there are VDD+3.6V tolerant.
  - ### The pad can accept VDD+3.6V without introducing pad leakage (in general <1uA @125°C)
  - ### When VDD is not connected, (internal bias circuit disabled), only accept 3.6V.

- ## When Output buffer is enabled, it is not any more 5V tolerant
  - ### When PAD is 5V, then IO drives high, it will create simply short circuit between 5V to VDD.
  - ### When PAD is 5V, then IO drives low, it will create simply short circuit between 5V to GND.

- ## When Open drain with external pull up 5V is used
  - ### Hi-Z behaves High output, external pull up will define the output voltage (5V). (No problem)
 - ### Low means driving low. Thanks to pull up resistor with voltage drop, when NMOS is enabled, output PAD become low (0V).

- Input threshold voltage is CMOS level
    - VIH ~= 2/3 VDD
    - VIL ~= 1/3 VDD
    - The voltage higher than VDD is simply translated as high level

Application example : I2C

- STM32 supplied by 1.8V or 3.3V can directly communicate with 5V I2C bus.

VDD=1.8V or 3.3V

VDDX=5.0V (max 5.4V when VDD=1.8V)

VDDX=5.0V

SDA

STM32

5V IC

SCL
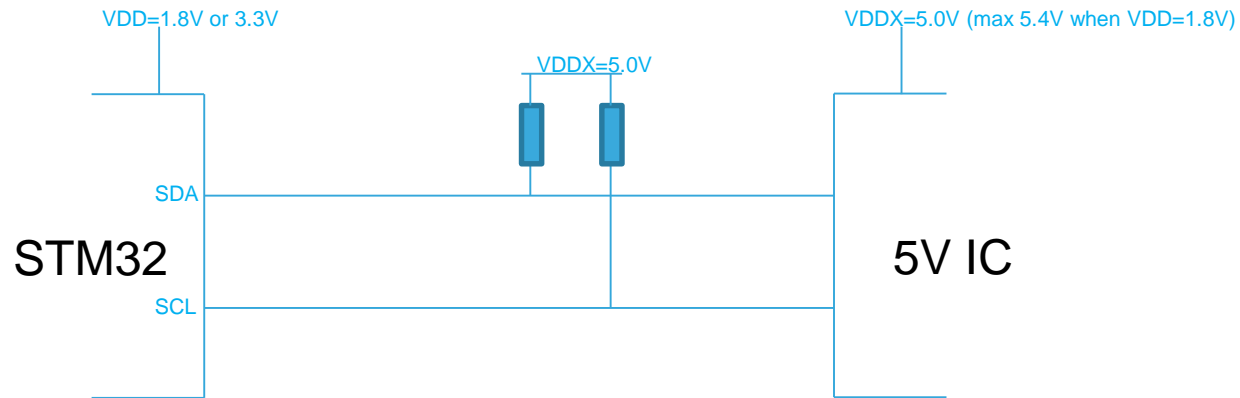
- If there is condition when VDD=0V, VDDX=5V(even it is transient), it is recommended to place the zenner diode(ex. 3.3V) between VDD and VDDX.

  - For example VDD is output of LDO supplied by VDDX

3.3(ex.)

VDDX=5V

LDO

VDD=3.3V To STM32 VDD
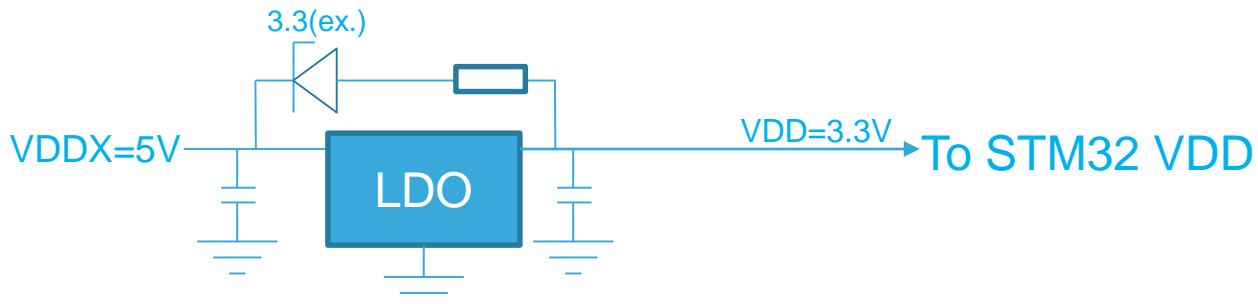
Application example : USB VBUS

- VBUS pad of STM32 is 5V tolerant.
  - However it needs to respect the VDD+3.6V absolute maximum ratings

  - If STM32 supply is from independent supply.
    - It is not allowed to connect VBUS when STM32 is not supplied.
    - Or place the zenner diode (ex.3.3V) between VBUS and VDD

  - If STM32 supply is from LDO supplied by VBUS
    - It is recommended to have zenner diode(ex. 3.3V)
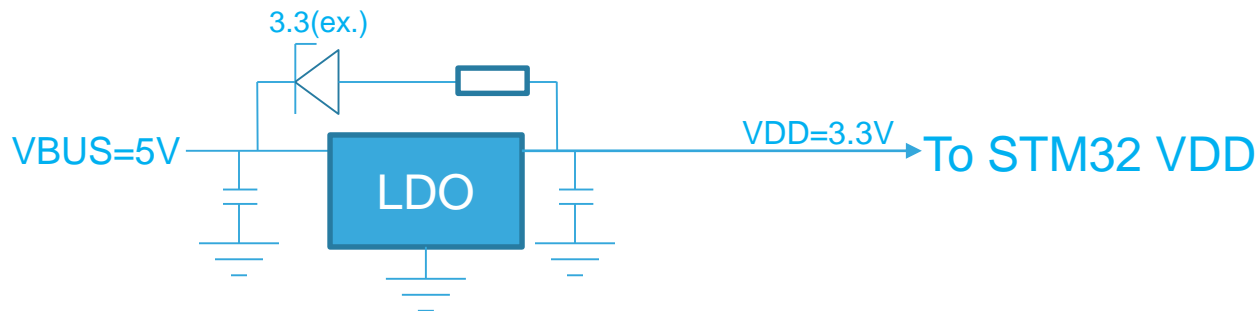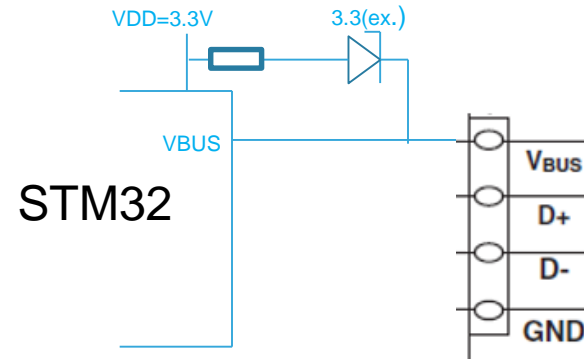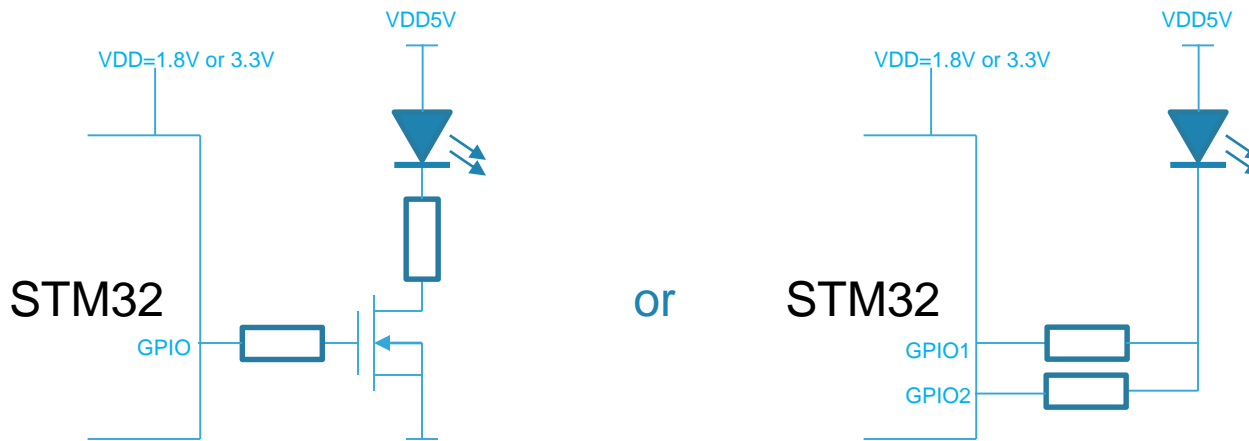
Application example : Triac Drive

- This example is shown for the -5V supply system
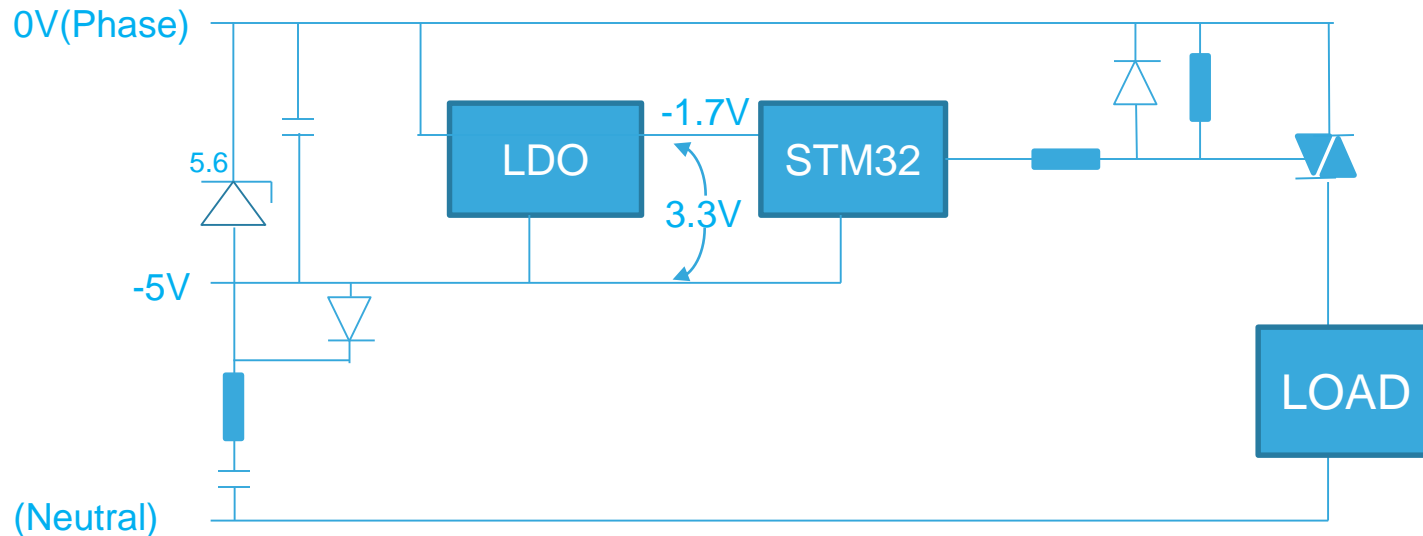
- STM32 GPIO need to be set up as Open-drain mode
  - If IO drive current is not enough, coupled of GPIO can be paralleled.

Application example : White LED Drive

- White LED need typical ~20mA of the current with Vf of 3.5V(typ) 4V(max)
  - As STM32 maximum sink current is 25mA, it is not enough margin to drive direct
  - Use External MOSFET(or BJT) or Drive by two GPIO can be the option.

- For the GPIO parallel drive, open drain mode must be used.
  - The Ground current will be huge compare to the MCU consumption. GND layout need to be attentioned.
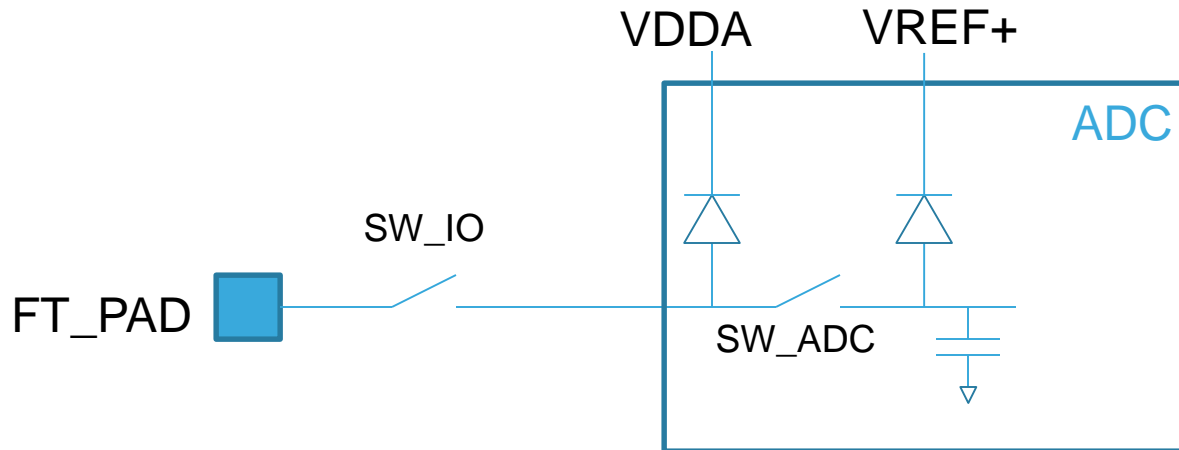
Application example : UART

- If UART transceiver to communicate is 5V supply with TTL compatible, STM32 can communicate directly
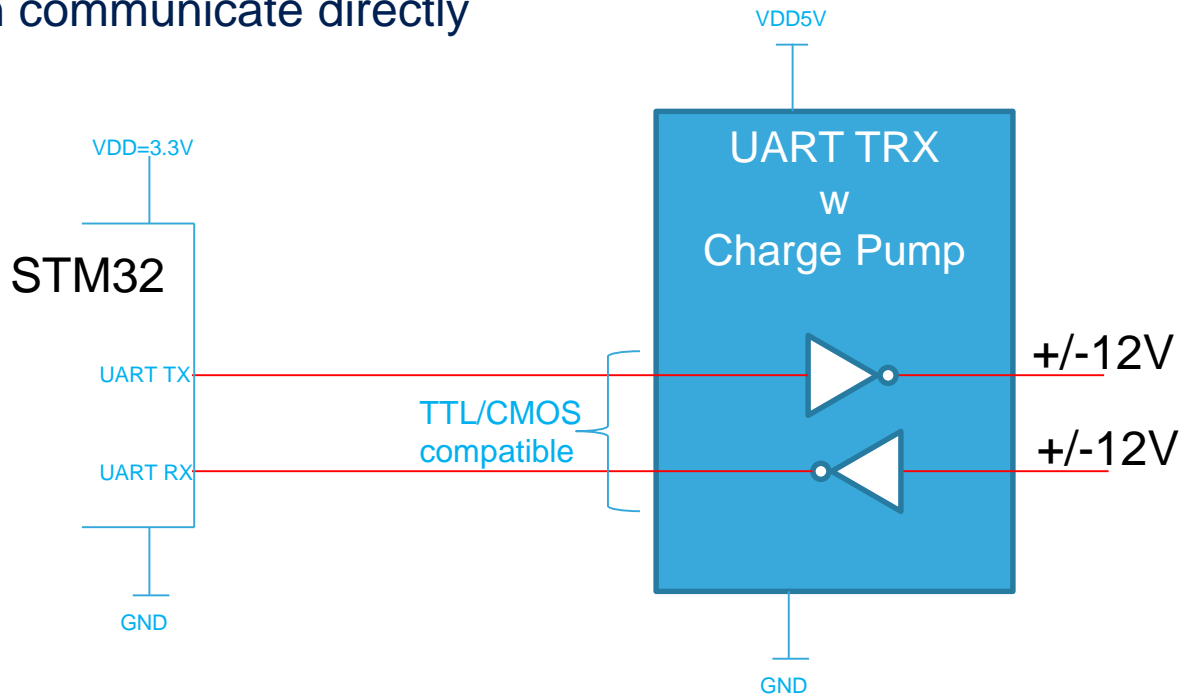
- If 5V UART interface input is TTL compatible, VOI<0.8V, VOH>2.0V so 3.3V CMOS output can drive without problem

- STM32 FT pad can accept 0 to 5V CMOS level input when VDD=3.3V.

IO usage for the 5V ADC connection

- STM32 has FT (5V tolerant) pads which connected to the ADC input.

- When ADC is not connected (analog switch in IO is not closed), IO can accept VDD+3.6V. So 5V apply to FT pad can be granted.

- However once IO input is connected to the ADC, and during the sampling phase, parasitic diode to VDDA and/or VREF+ will be forward biased.

- It is recommended to clamp the input voltage with external clamp (e.g. series resistor and the schottky diode to VREF+ voltage level)

The parasitic diode are not characterized for the reliability, STMicroelectronics cannot guarantee the level of current which can accept those diodes.
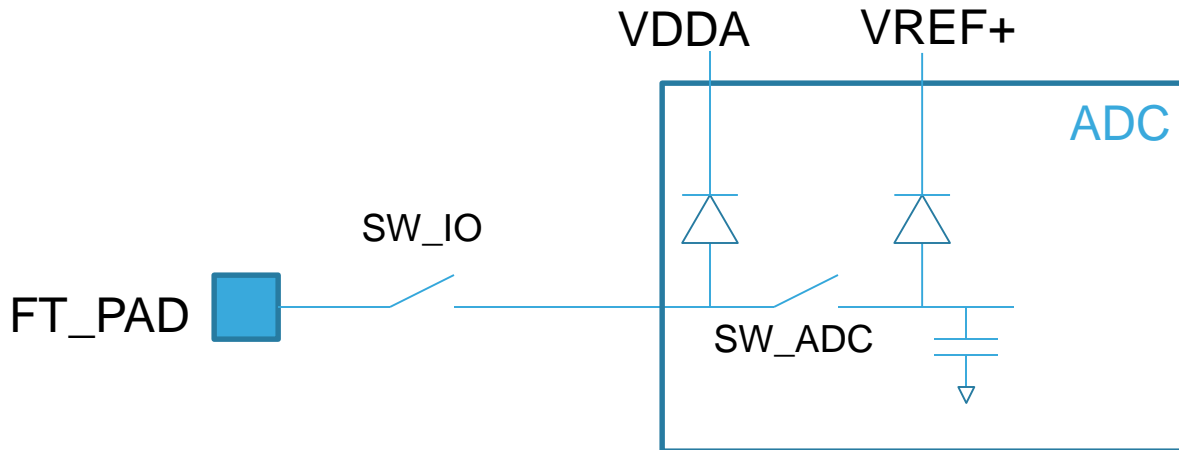
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- If there is unused FT pad available on STM32, connect this IO to the ADC input pad with parallel configuration.

DC source
0~5V

STM32

SW_IO

To ADC

27kohm

FT_PAD

Pull-down
45kohm(typ)
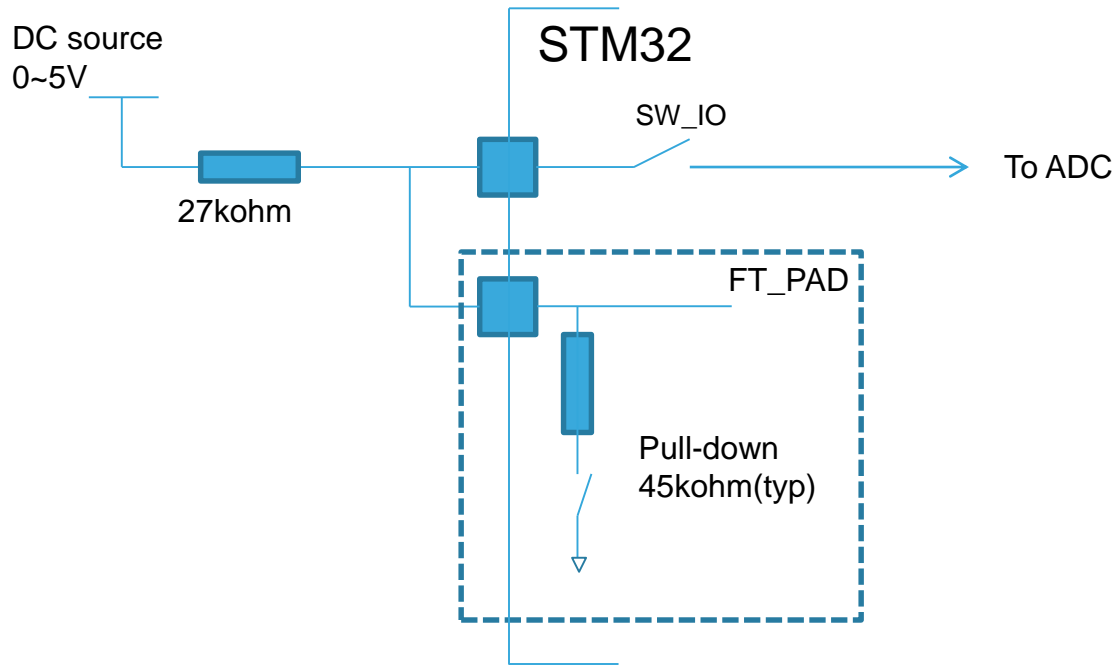
1. The ADC will make conversion with other FT_PAD pull-down enabled

2. If first ADC conversion result is less than 2V(which indicated the DC source is inside the ADC input range), ADC will re-do the conversion with pull-down disabled.

- Above method avoid the parasitic diode forward bias.