**Digital Design and Computer Architecture LU**

# Lab Protocol

# Exercise I

Cristian Avram, Matr. Nr. 01304470

e01304470@student.tuwien.ac.at

Vienna, March 25, 2018

# Task 1: Structural modeling

- RTL.png

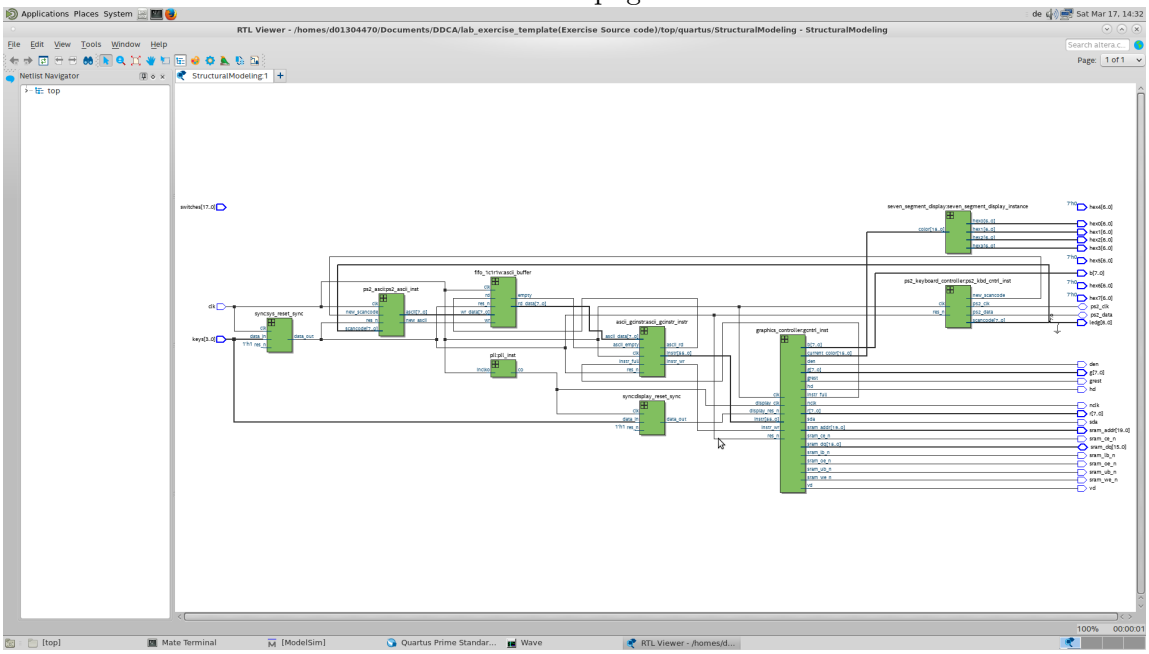

Figure 1: Screenshot showing the top level design in the RTL netlist viewer

# Task 2: Seven Segment Display I

**Question:** Are the hex* signals high or low-active? Explain!

**Answer:** The **hex*** signals are **low active**. This means, that when you want to see something on the seven segment display, you need to give them value 0 in order to have them active.

# Task 3: Behavioral Simulation

Table 1: Timing measurements

| Time | Value |
|---|---|
| First transition of a character input on the PS/2 interface to ASCII character output of *ps2_ascii* | 40 ns |
| Output of the last ASCII character ('4') to the seven segment display changing its output | 140 ns |
| 1/Display frame rate (vd period) | 22,176 ms |

- 4 Propagation.png

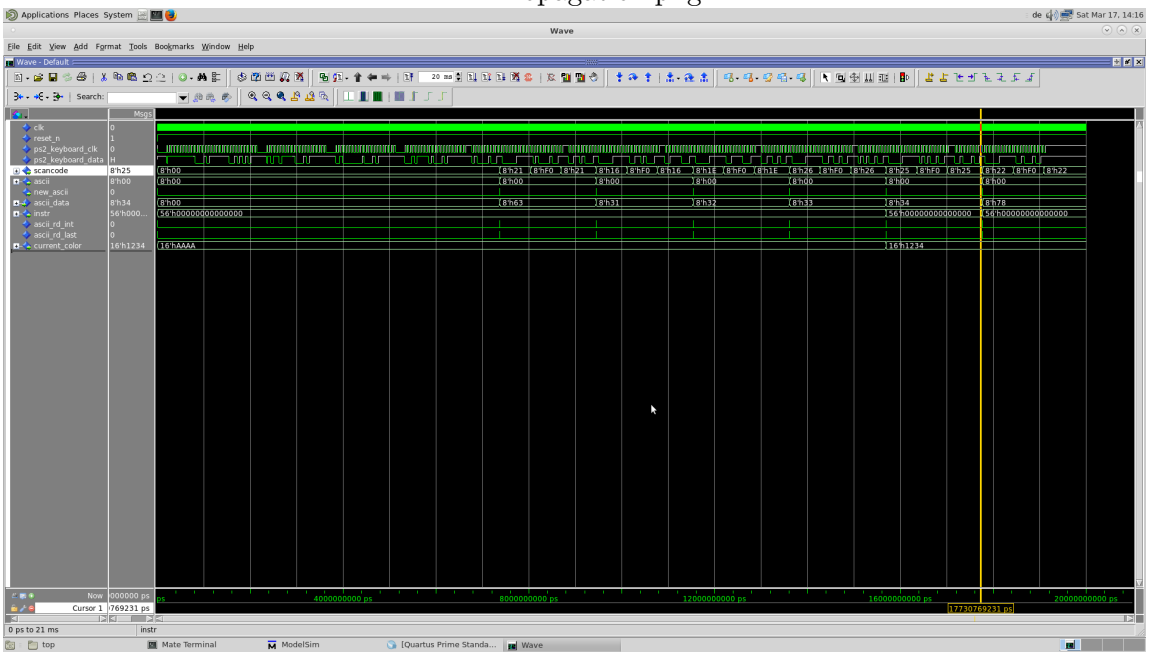

Figure 2: Simulation showing the character propagation through the system

- Table1.png

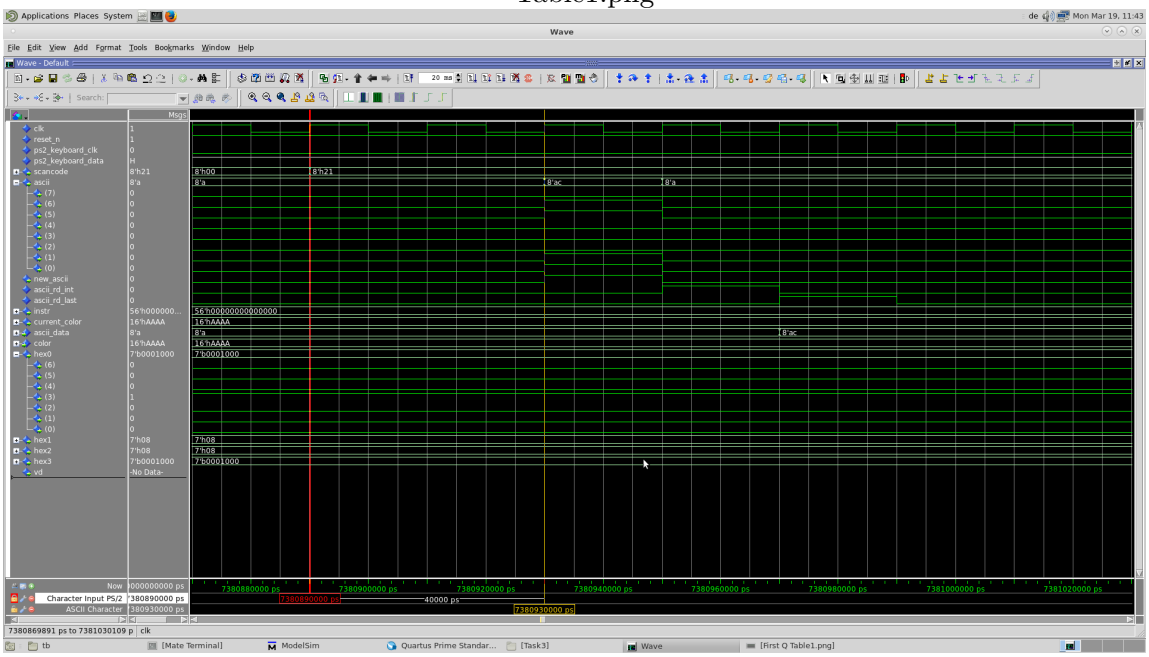

Figure 3: Interval Measurement using markers - Q1

**Question:** How long is the execution time of the clear screen command. How can you determine when the command has finished execution by just observing the signals to the SRAM?

- Table1.png

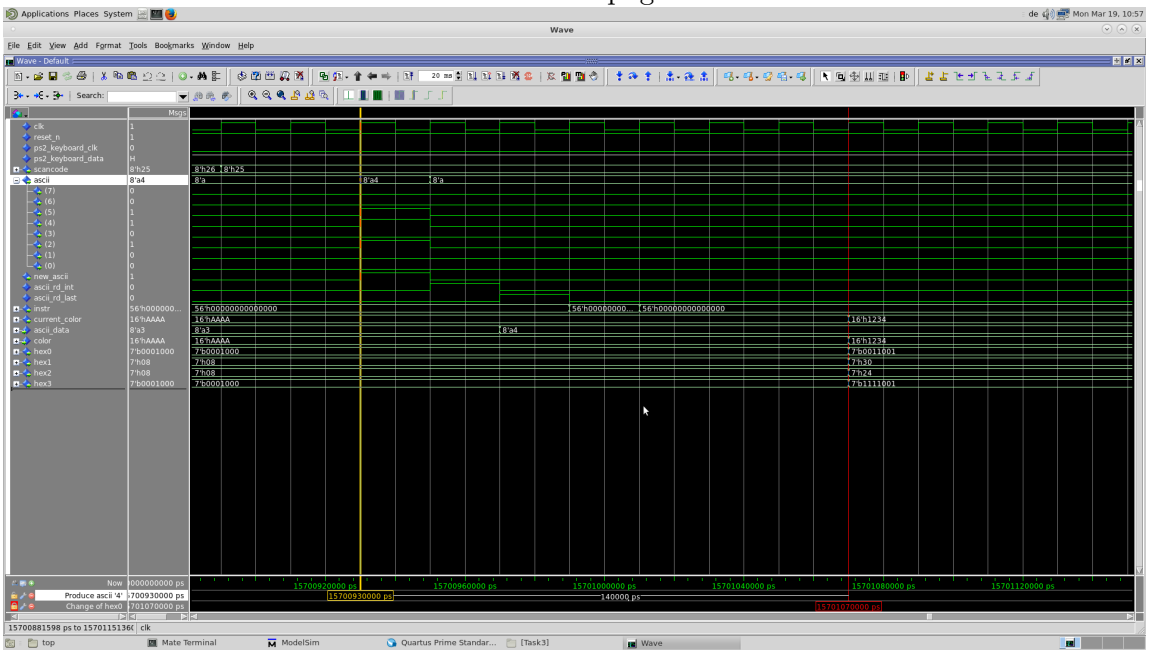

Figure 4: Interval Measurement using markers - Q2

- Table1.png

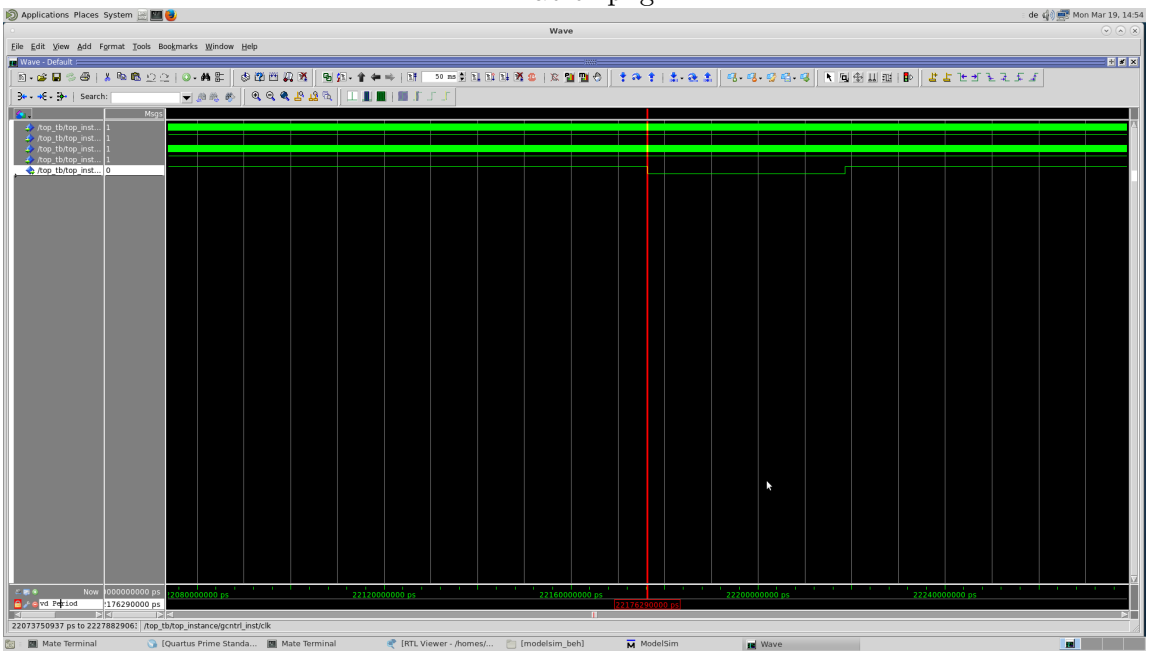

Figure 5: Interval Measurement using markers - Q3

**Answer:** The execution time is 45,79ms. It can be identified using *top_tb.vhd* file by adding *sram_dq* signal. The Length of the simulation should be around 80ms.

**Question:** Describe how the bug in the *ps2_ascii* component affects the design.

**Answer:** The Bug being referred is the one in *ps2_ascii.vhd* and it consists of "Y" and "y" being mapped to letter "Z" and "z". By using the command *make sim_fileio* we are greeted with and Error that says "y" expected=0x79, actual=0x7a, and "Y" expected=0x59, actual=0x5a. The only thing to do is to change the values in the above mentioned document and redo the test.

## Task 4: Postlayout Simulation

**Question:** Different propagation delays: How long is the transition time you measured when the seven segment display output bus changes its value and multiple signals toggle?

**Answer:** Based on *StructuralModeling_7_1200mv_Oc_slow.vho* file
and *StructuralModeling_7_1200mv_Oc_vhd_slow.sdo* the transition time is 3572 ps.

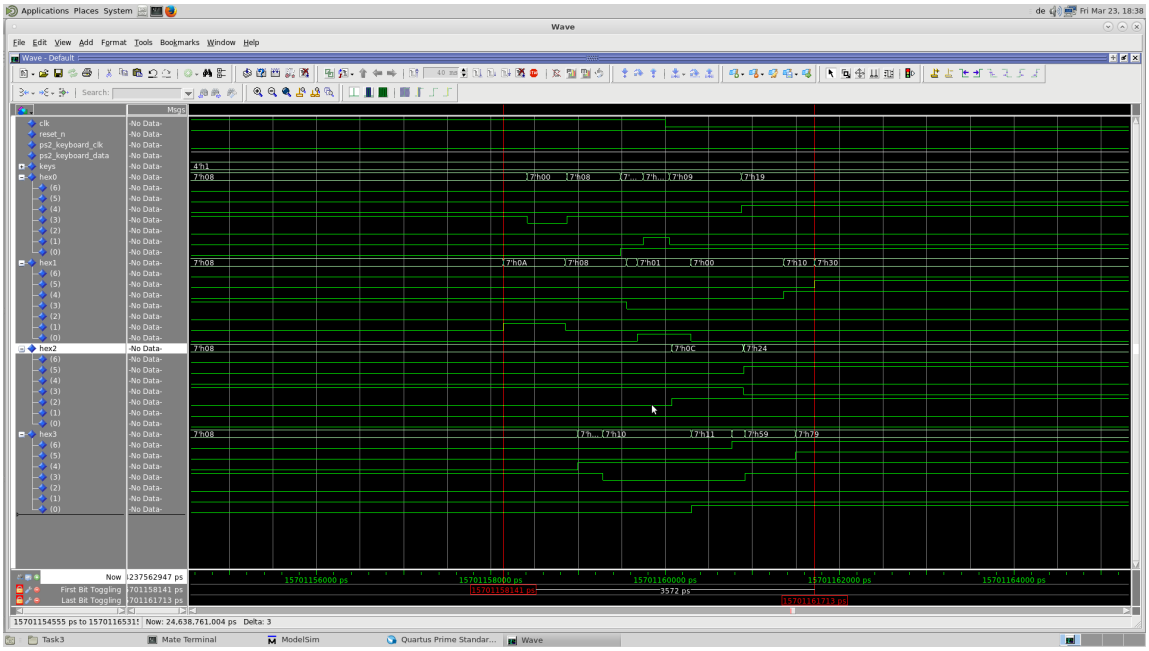


Figure 6: Different propagation delays on the seven segment display bus

## Task 5: Seven Segment Display II

**Question:** Argue why the output on the signals hex{4-5} is correct.

**Answer:** The RGB color signal will have $hE795$ value. It will consist of $h1c$ as red channel, $h15$ as blue channel, and $h3c$ as green channel

- decimal.png

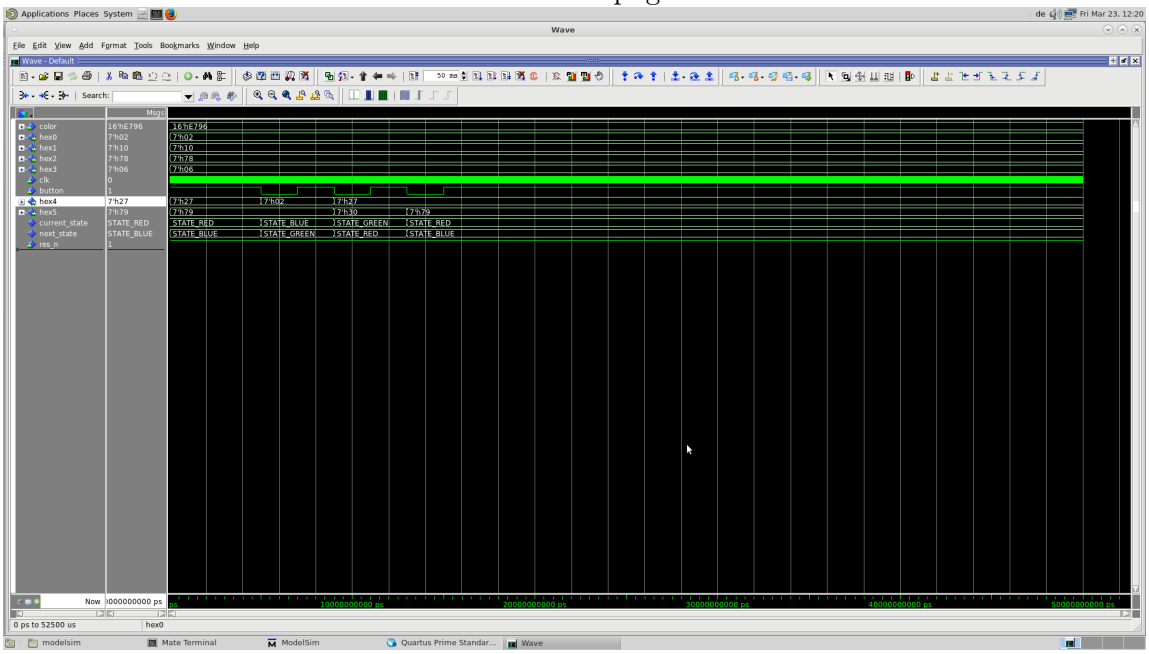

Figure 7: Simulation of the extended seven segment display (3 button presses)

# Task 6: Serial Port

- Simulation receiver.png

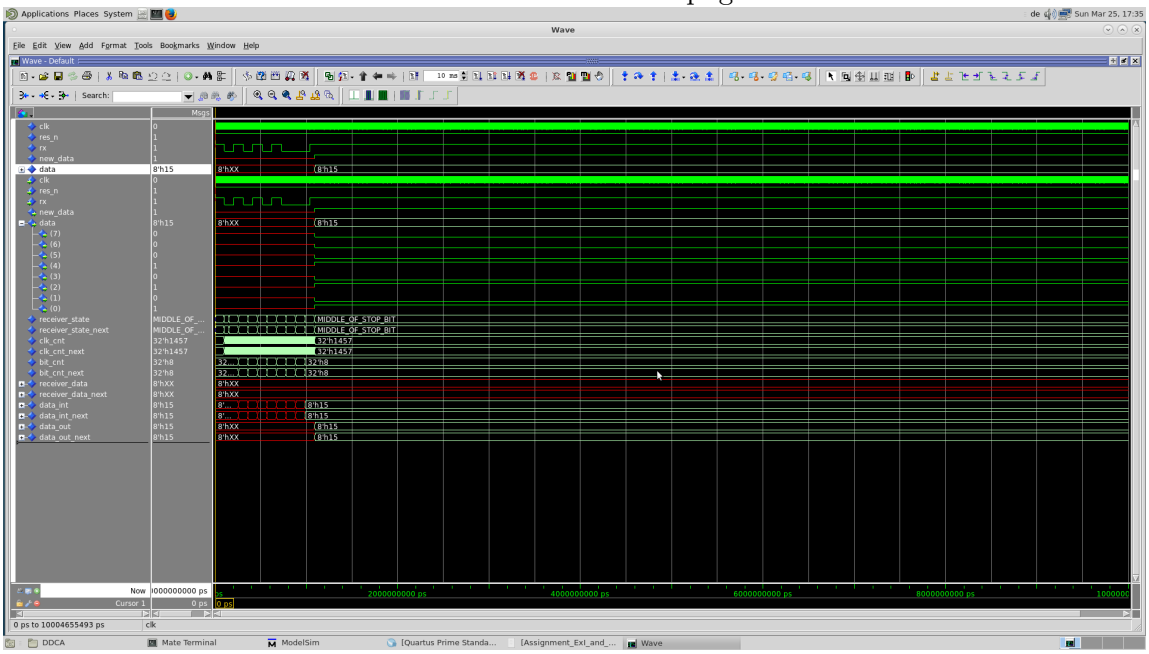

Figure 8: Screenshot of a simulation showing the reception of a whole UART frame.

**Question:** Which baudrate did you use for the above simulation? How long should the

transmission take for the whole frame (including start and stop bit)? What is the time you measured in the simulation (not including the stop bit)?

**Answer:** I used 9600 bps as Baudrate value, which means that 1 bit will be transferred in 1/9600 seconds. In total, we have 10 bits including start, stop and data bits. The time that I measured is $941\mu s$.

**Question:** Why does the state machine only count to *CLK_DIVISOR-2* and not *CLK_DIVISOR-1*?

**Answer:** It does need to go back to $WAIT\_DATA\_BIT$, so this is why it reserves one last clock cycle for that. For every clock cycle, it moves to another state.

**Question:** What is the purpose of the *MIDDLE_OF_START_BIT* state of the receiver FSM? Is it really necessary or could it be optimized away?

**Answer:** The purpose is to prevent glitches as start bit. Another reason, is to make sure that the middle of start bit is still low.

Table 2: Resouce usage of the serial module (including all submodules).

| | LC Combinationals | LC Registers | Memory |
|---|---|---|---|
| Absolute number | 302 | 236 | 0 |
| % of whole design | 1374 | 1618 | 56320 |
| % of whole FPGA resources | 3 | 1 | 1 |