Digital Design and Computer Architecture LU

Lab Protocol

Exercise IV

Group ?

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Forwarding Simulation

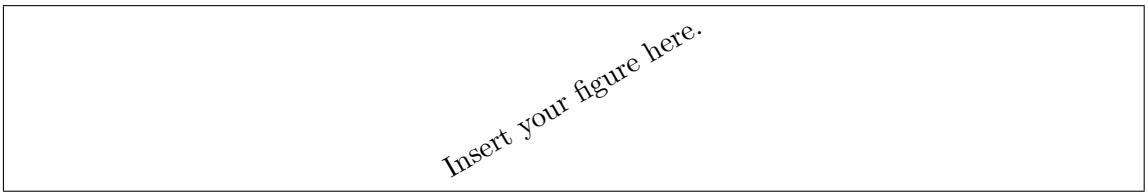

Figure 1: Simulation screenshot for Listing 1.

Make sure that at least the following signals are visible in Figure 1: the program counter in the fetch stage, the instruction being fetched, and the signals `wraddr`, `wrdata`, and `regwrite` of the register file.

Listing 1: Assembler example with forwarding

```
addi $1, $0, 7
addi $2, $0, 5
and $1, $2, $1
nop
nop
```

Branch Hazards Simulation

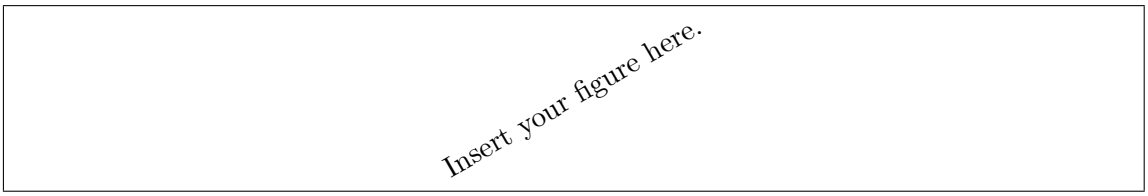

Figure 2: Simulation screenshot for Listing 2.

Make sure that at least the following signals are visible in Figure 2: the program counter in the fetch stage, the instruction being fetched, and the signals `wraddr`, `wrdata`, and `regwrite` of the register file.

Listing 2: Assembler example with branch delay slot

```
loop:   j loop
        addi $1, $1, 1
        addi $2, $2, 1
        nop
```

Synthesis Results

Table 1: Resource usage by entity, including resources used by sub-entities.

	LC Combinationals	LC Registers	Memory Bits
Fetch Stage			
Decode Stage			
– Register File			
Execute Stage			
– ALU			
Memory Stage			
– Jump Unit			
– Memory Unit			
Write-Back Stage			
Forwarding Unit			
Control Unit			
Sum			

Question: What is the maximum frequency of your design?

Answer:

Question: Where is the critical path of your design?

Answer: