Charles Jake Dickie

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Education

Imperial College London

September 2019 - August 2023

MEng Computing (Artificial Intelligence and Machine Learning)

London, UK

• First class honours (79.3% overall). Awards: Distinguished Project (93% in Master's Dissertation); Dean's List (top 10% of cohort) in Year 4 (83.5%).

Radley College

September 2013 – June 2018

Secondary School Oxford, UK

• A-levels (Maths, Further Maths, Physics, Chemistry: A*A*A); GCSEs (10 A*s); Student Mentor; Social Prefect; Further Maths Prize Winner (2018).

Experience

Arctic Lake

November 2023 - Present

Electronic Trading Developer | SystemVerilog, Python, Java, C

London, UK

- Developing an FPGA design for low-latency (sub-microsecond) risk checks on outbound trades. Includes: implementing custom risk checking models in hardware; adding two-way communication with host system by implementing DMA over PCIe, writing drivers and designing a custom 'frame' communication protocol for managing data exchange; parsing/decoding of network messages; risk and configuration state management modules; encoding of risk event messages for communication over PCIe; development of test-harness for physical testing of trading/risk scenarios and adverse network scenarios (such checksum failures, resends, corruption, duplicates); integration with existing trading platform logic; writing simulation tests.
- Owner of ISO 27001 Annex A controls 'Secure Coding' and 'Application Security Requirements'. Ensuring compliance
 by: developing systems (e.g. using YouTrack worflows, writing automation scripts); drafting policies; coordinating
 across teams to delegate work and meet deadlines; communicating with and providing evidence to auditors.
- Representing company at recruitment and outreach events. Delivered presentation at Imperial College London as part of the 'Applications of Computing in Industry' lecture series about the challenges of developing low-latency applications in FPGA.

Arctic Lake April – September 2022

Electronic Trading Developer Intern | Java, Python, SystemVerilog

London, UK

- Developed new features and optimizations for real-time trading event analysis using the Esper library: improved the
 performance of order book consolidation and flattening by rewriting the underlying representation; added user
 support for live querying of events; created a testing framework for simplified injection/replay of trading events for
 integration tests.
- Designed entirely new systems for onboarding, incident management and ticket management using YouTrack workflow API.
- Created an FPGA design using Vivado and Vitis HLS to prototype hardware modifications to UDP packets as a proof of concept for a low-latency risk checking project.

Projects & Publications

Aggregating Bipolar Opinions by Arguing

November 2024

Autonomous Agents and Multi-Agent Systems, Volume 39, Article 4

• Primary author of peer-reviewed publication in *Autonomous Agents and Multi-Agent Systems*. Established results and corresponding proofs related to the preservation of semantic properties during the aggregation of bipolar assumption-based argumentation frameworks. Keywords: *Opinion Aggregation, Computational Argumentation, Social Choice Theory, Knowledge Representation and Reasoning*. Available at: https://doi.org/10.1007/s10458-024-09684-3

Aggregating Bipolar Opinions

November 2022 - June 2023

Master's Dissertation

• Established core theoretical results of above publication. Developed a web platform, *ArgSolve*, to facilitate argumentative debates amongst users in real-time, leveraging theoretical results to evaluate the preservation of consensus amongst debate participants when aggregating expressed opinions of debates as argumentation frameworks. Implemented and proved the correctness (soundness and completeness) of a novel program written in ASP to identify 'strong' sets of arguments in bipolar ABA frameworks according to well-known semantics. Awards: 93% (Distinguished Project); Corporate Partnership Programme Award for Techincal Innovation. Available at: https://crjake.github.io/thesis.pdf.