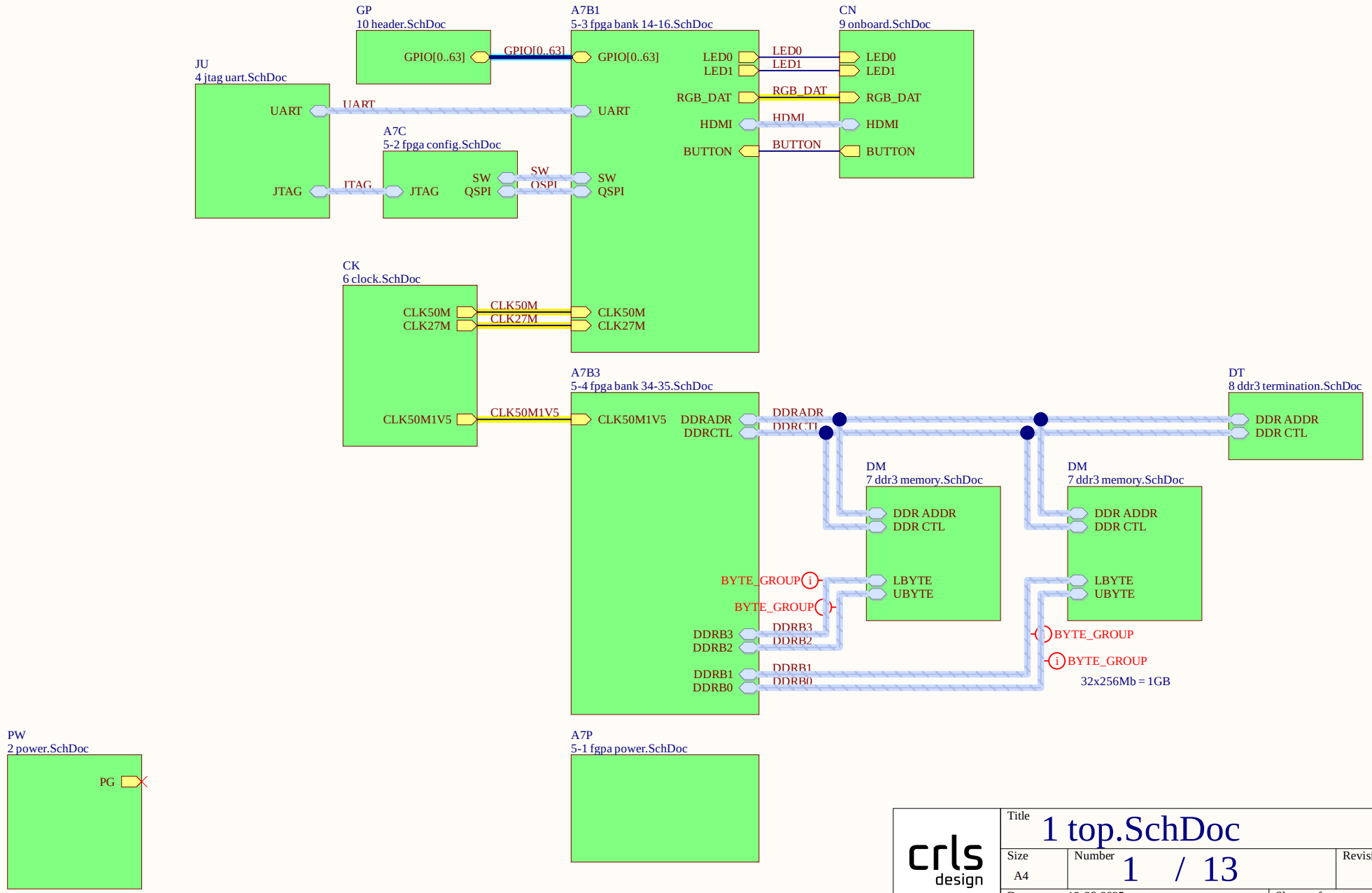
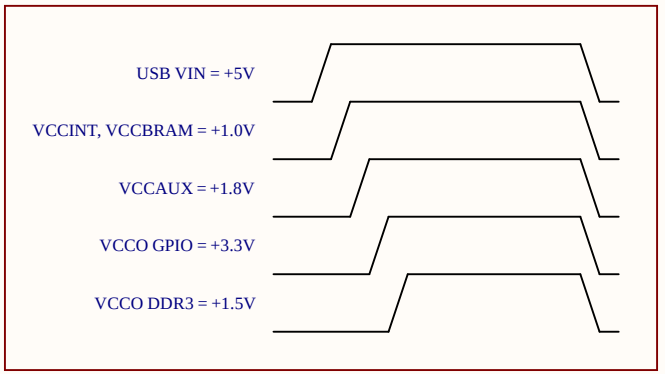

GP
10 header.SchDoc
GPIO[0..63]
GPIO[0..63]
A7B1
5-3 fpga bank 14-16.SchDoc
GPIO[0..63]
LED0
LED1
RGB_DAT
HDMI
BUTTON
CN
9 onboard.SchDoc
LED0
LED1
RGB_DAT
HDMI
BUTTON
JU
4 jtag uart.SchDoc
UART
UART
UART
A7C
5-2 fpga config.SchDoc
JTAG
JTAG
JTAG
SW
QSPI
SW
QSPI
SW
QSPI
CK
6 clock.SchDoc
CLK50M
CLK27M
CLK50M1V5
CLK50M
CLK27M
CLK50M1V5
A7B3
5-4 fpga bank 34-35.SchDoc
CLK50M1V5
DDRADR
DDRCTL
DDRB3
DDRB2
DDRB1
DDRB0
DT
8 ddr3 termination.SchDoc
DDR ADDR
DDR CTL
DM
7 ddr3 memory.SchDoc
DDR ADDR
DDR CTL
LBYTE
UBYTE
BYTE_GROUP
DM
7 ddr3 memory.SchDoc
DDR ADDR
DDR CTL
LBYTE
UBYTE
BYTE_GROUP
BYTE_GROUP
32x256Mb = 1GB
PW
2 power.SchDoc
PG
A7P
5-1 fgpa power.SchDoc
crls
design
Title
1 top.SchDoc
Size
A4
Number
1 / 13
Revision
Date:
12-28-2025
Sheet of
File:
C:\My Drive\..\1 top.SchDoc
Drawn By:

+5 USB
+3.3
+1.8
+1.5 DDR3
+1.0
+0.75 VTT
+0.75 VTTREF

The recommended power-on sequence is VCCINT, VCCBRAM, VCCAUX, and VCCO



BC
3 buck.SchDoc
EN
VOUT
FB
VIN
PG

R202
100k
0402

R201
68k
0402

R203
100k
0402

0.6 * (168/100) = 1.008V

R204
200k
0402

R205
100k
0402

0.6 * (300/100) = 1.8V

R206
450k
0402

R208
100k
0402

0.6 * (550/100) = 3.3V

R209
150k
0402

R210
100k
0402

0.6 * (250/100) = 1.5V

R207
1k
0402

DS201

Q201
2N7002-7-F

PG

U201
S3
S5
VDDQSNS
VLDOIN
VDD
VTT
VTTSNS
VTTREF
EP
PGND
GND
TPS51206DSQR

C202
10u
0603

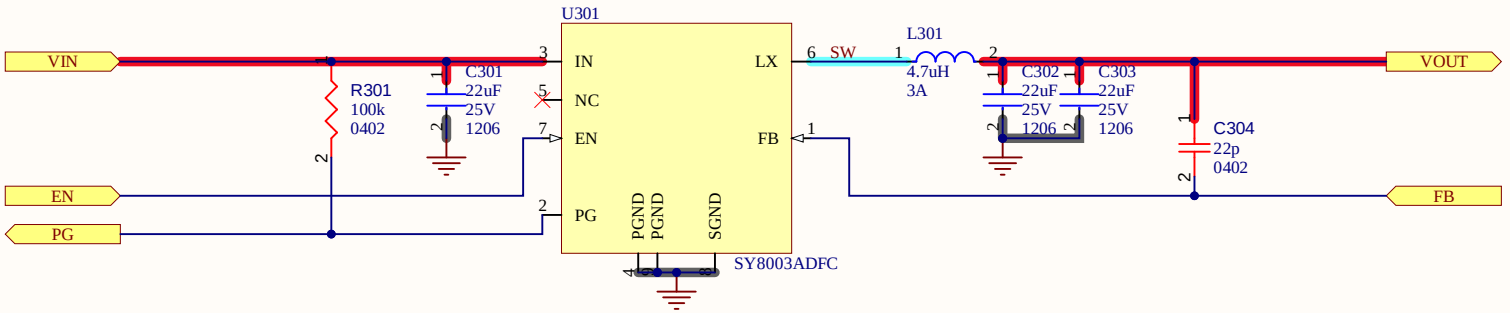
C204
100n
0402

C203
220n
0402

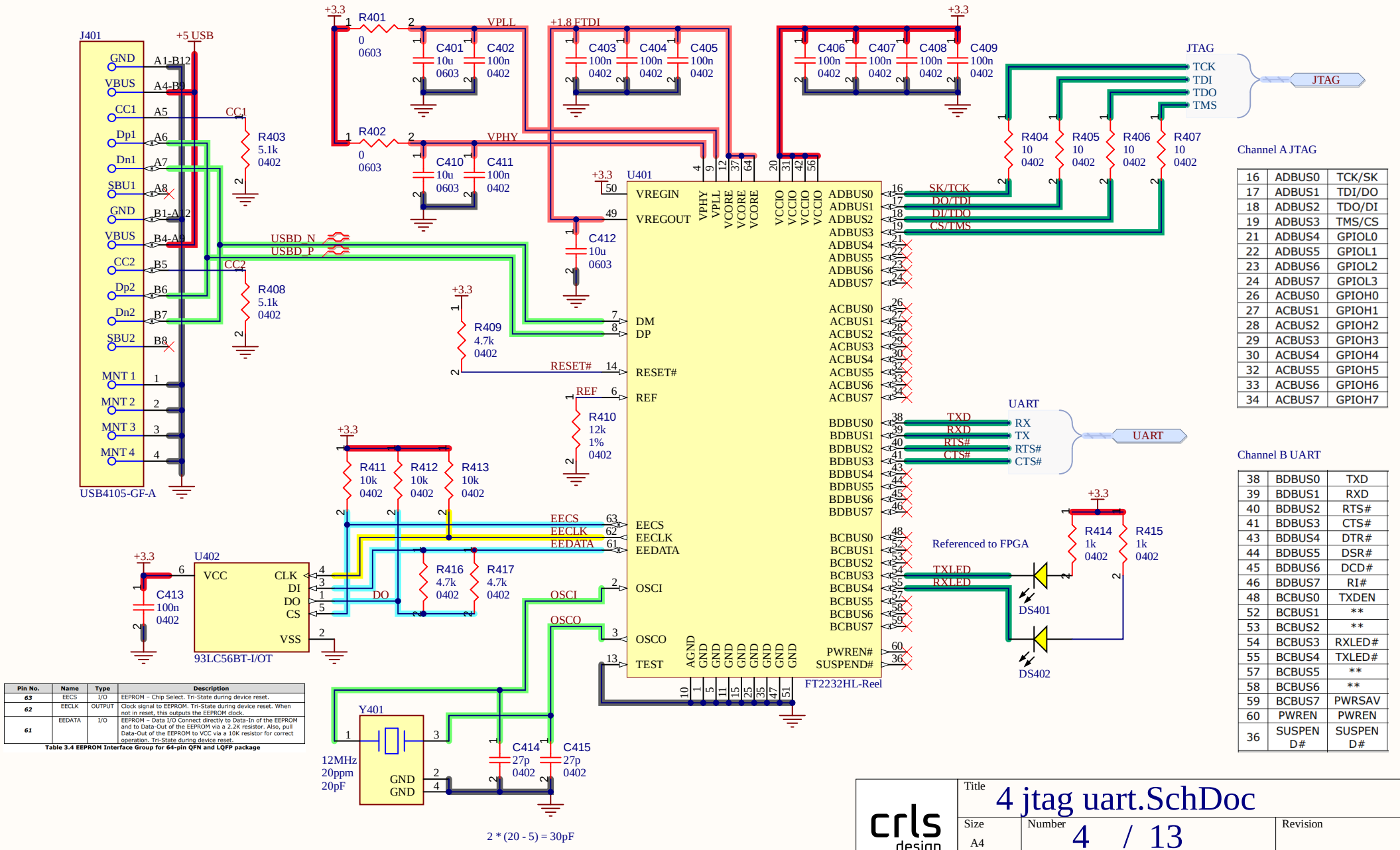
C201
10u
0603

Title	2 power.SchDoc		
Size A4	Number 2 / 13		Revision
Date: 12-28-2025		Sheet of	
File: C:\My Drive\..\2 power.SchDoc		Drawn By:	

crls design



crls design	Title	3 buck.SchDoc	
	Size: A4	Number: 3 / 13	Revision:
	Date: 12-28-2025		Sheet of
	File: C:\My Drive\..\3 buck.SchDoc		Drawn By:



Channel A JTAG

16	ADBUS0	TCK/SK
17	ADBUS1	TDI/DO
18	ADBUS2	TDO/DI
19	ADBUS3	TMS/CS
21	ADBUS4	GPIOL0
22	ADBUS5	GPIOL1
23	ADBUS6	GPIOL2
24	ADBUS7	GPIOL3
26	ACBUS0	GPIOH0
27	ACBUS1	GPIOH1
28	ACBUS2	GPIOH2
29	ACBUS3	GPIOH3
30	ACBUS4	GPIOH4
32	ACBUS5	GPIOH5
33	ACBUS6	GPIOH6
34	ACBUS7	GPIOH7

Channel B UART

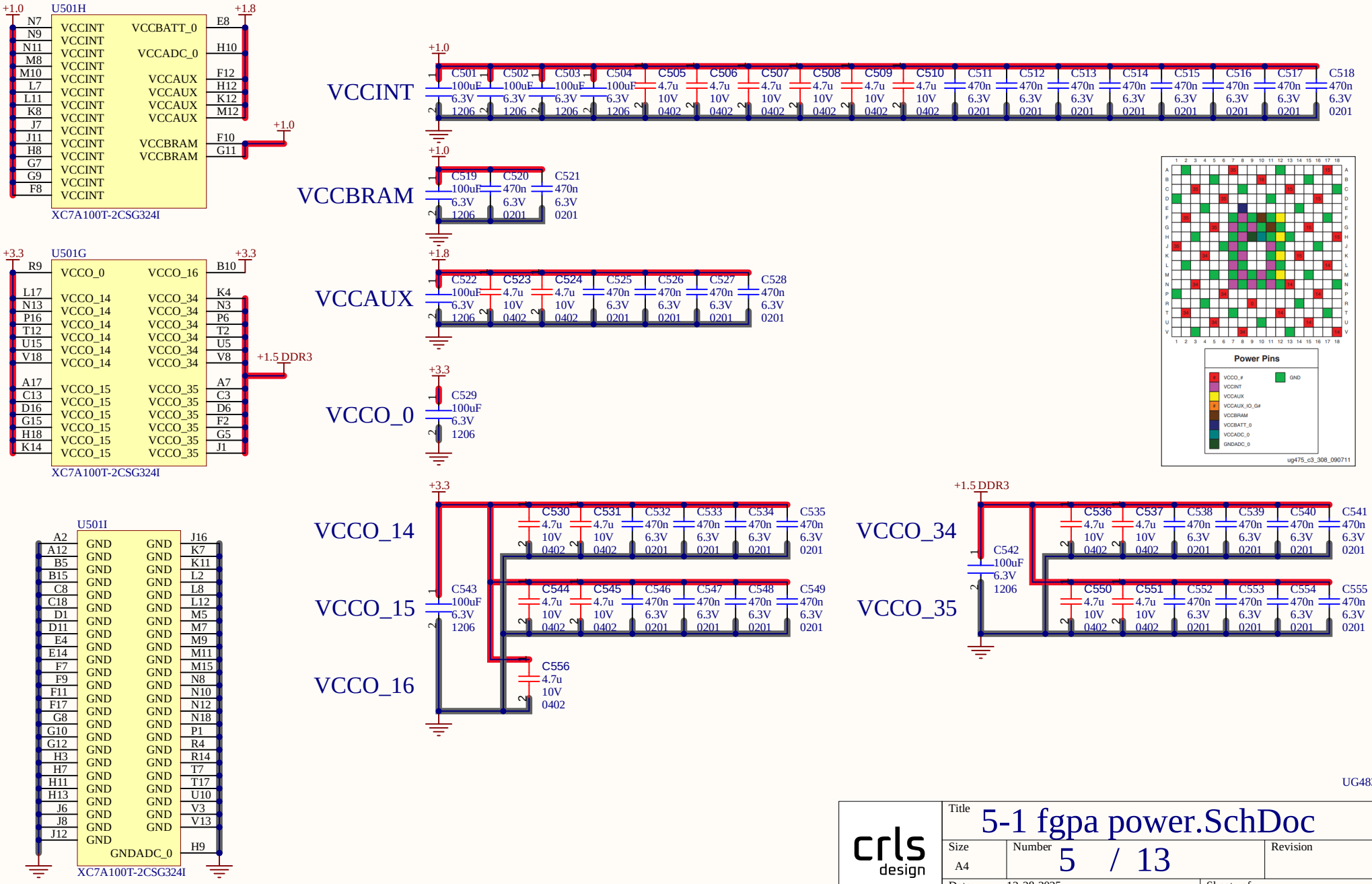
38	BDBUS0	TXD
39	BDBUS1	RXD
40	BDBUS2	RTS#
41	BDBUS3	CTS#
43	BDBUS4	DTR#
44	BDBUS5	DSR#
45	BDBUS6	DCD#
46	BDBUS7	RI#
48	BCBUS0	TXDEN
52	BCBUS1	**
53	BCBUS2	**
54	BCBUS3	RXLED#
55	BCBUS4	TXLED#
57	BCBUS5	**
58	BCBUS6	**
59	BCBUS7	PWRSAV
60	PWREN	PWREN
36	SUSPEN D#	SUSPEN D#

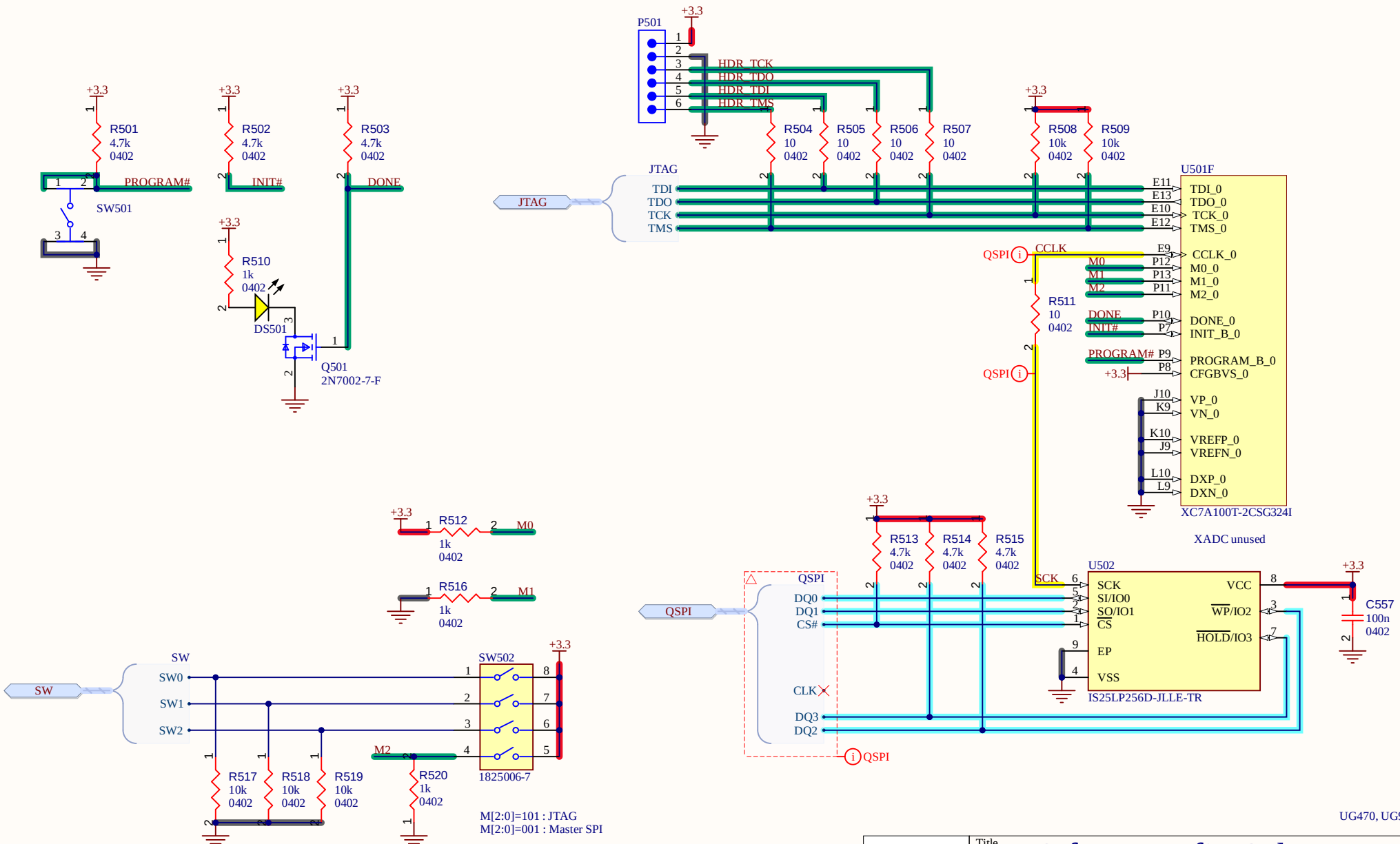
Pin No.	Name	Type	Description
63	EECS	I/O	EEPROM – Chip Select. Tri-State during device reset.
62	EECLK	OUTPUT	Clock signal to EEPROM. Tri-State during device reset. When not in reset, this outputs the EEPROM clock.
61	EEDATA	I/O	EEPROM – Data I/O Connect directly to Data-In of the EEPROM and to Data-Out of the EEPROM via a 2.2K resistor. Also, pull Data-Out of the EEPROM to VCC via a 10K resistor for correct operation. Tri-State during device reset.

Table 3.4 EEPROM Interface Group for 64-pin QFN and LQFP package

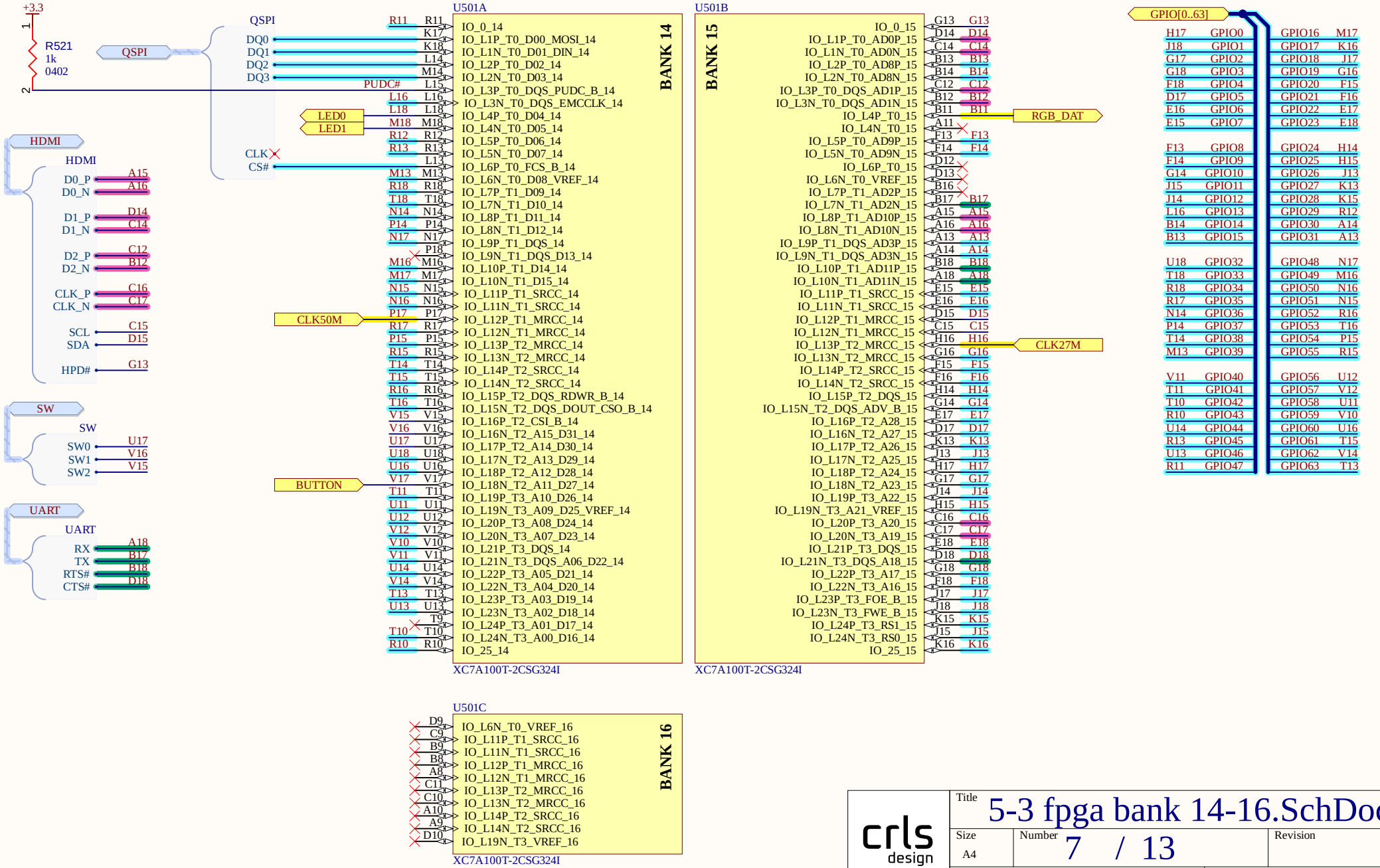
crls design

Title	4 jtag uart.SchDoc	
Size A4	Number 4 / 13	Revision
Date: 12-28-2025		Sheet of
File: C:\My Drive\..\4 jtag uart.SchDoc		Drawn By:


U501H
+1.0
+1.8
N7 VCCINT
N9 VCCINT
N11 VCCINT
M8 VCCINT
M10 VCCINT
L7 VCCINT
L11 VCCINT
K8 VCCINT
J7 VCCINT
J11 VCCINT
H8 VCCINT
G7 VCCINT
G9 VCCINT
F8 VCCINT
VCCBATT_0 E8
VCCADC_0 H10
VCCAUX F12
VCCAUX H12
VCCAUX K12
VCCAUX M12
VCCBRAM F10
VCCBRAM G11
XC7A100T-2CSG324I
U501G
+3.3
+1.5 DDR3
R9 VCCO_0
VCCO_16 B10
L17 VCCO_14
N13 VCCO_14
P16 VCCO_14
T12 VCCO_14
U15 VCCO_14
V18 VCCO_14
VCCO_34 K4
VCCO_34 N3
VCCO_34 P6
VCCO_34 T2
VCCO_34 U5
VCCO_34 V8
A17 VCCO_15
C13 VCCO_15
D16 VCCO_15
G15 VCCO_15
H18 VCCO_15
K14 VCCO_15
VCCO_35 A7
VCCO_35 C3
VCCO_35 D6
VCCO_35 F2
VCCO_35 G5
VCCO_35 J1
XC7A100T-2CSG324I
U501I
A2 GND
A12 GND
B5 GND
B15 GND
C8 GND
C18 GND
D1 GND
D11 GND
E4 GND
E14 GND
F7 GND
F9 GND
F11 GND
F17 GND
G8 GND
G10 GND
G12 GND
H3 GND
H7 GND
H11 GND
H13 GND
J6 GND
J8 GND
J12 GND
GND J16
GND K7
GND K11
GND L2
GND L8
GND L12
GND M5
GND M7
GND M9
GND M11
GND M15
GND N8
GND N10
GND N12
GND N18
GND P1
GND R4
GND R14
GND T7
GND T17
GND U10
GND V3
GND V13
GNDADC_0 H9
XC7A100T-2CSG324I
VCCINT
C501 100uF 6.3V 1206
C502 100uF 6.3V 1206
C503 100uF 6.3V 1206
C504 100uF 6.3V 1206
C505 4.7u 10V 0402
C506 4.7u 10V 0402
C507 4.7u 10V 0402
C508 4.7u 10V 0402
C509 4.7u 10V 0402
C510 4.7u 10V 0402
C511 470n 6.3V 0201
C512 470n 6.3V 0201
C513 470n 6.3V 0201
C514 470n 6.3V 0201
C515 470n 6.3V 0201
C516 470n 6.3V 0201
C517 470n 6.3V 0201
C518 470n 6.3V 0201
VCCBRAM
C519 100uF 6.3V 1206
C520 470n 6.3V 0201
C521 470n 6.3V 0201
VCCAUX
C522 100uF 6.3V 1206
C523 4.7u 10V 0402
C524 4.7u 10V 0402
C525 470n 6.3V 0201
C526 470n 6.3V 0201
C527 470n 6.3V 0201
C528 470n 6.3V 0201
VCCO_0
C529 100uF 6.3V 1206
VCCO_14
C530 4.7u 10V 0402
C531 4.7u 10V 0402
C532 470n 6.3V 0201
C533 470n 6.3V 0201
C534 470n 6.3V 0201
C535 470n 6.3V 0201
VCCO_15
C543 100uF 6.3V 1206
C544 4.7u 10V 0402
C545 4.7u 10V 0402
C546 470n 6.3V 0201
C547 470n 6.3V 0201
C548 470n 6.3V 0201
C549 470n 6.3V 0201
VCCO_16
C556 4.7u 10V 0402
Power Pins
VCCO_#
VCCINT
VCCAUX
VCCAUX_IO_G#
VCCBRAM
VCCBATT_0
VCCADC_0
GNDADC_0
GND
ug475_c3_308_090711
+1.5 DDR3
VCCO_34
C542 100uF 6.3V 1206
C536 4.7u 10V 0402
C537 4.7u 10V 0402
C538 470n 6.3V 0201
C539 470n 6.3V 0201
C540 470n 6.3V 0201
C541 470n 6.3V 0201
VCCO_35
C550 4.7u 10V 0402
C551 4.7u 10V 0402
C552 470n 6.3V 0201
C553 470n 6.3V 0201
C554 470n 6.3V 0201
C555 470n 6.3V 0201
UG483
crls design
Title 5-1 fgpa power.SchDoc
Size A4
Number 5 / 13
Revision
Date: 12-28-2025
Sheet of
File: C:\My Drive\..\5-1 fgpa power.SchDoc
Drawn By:

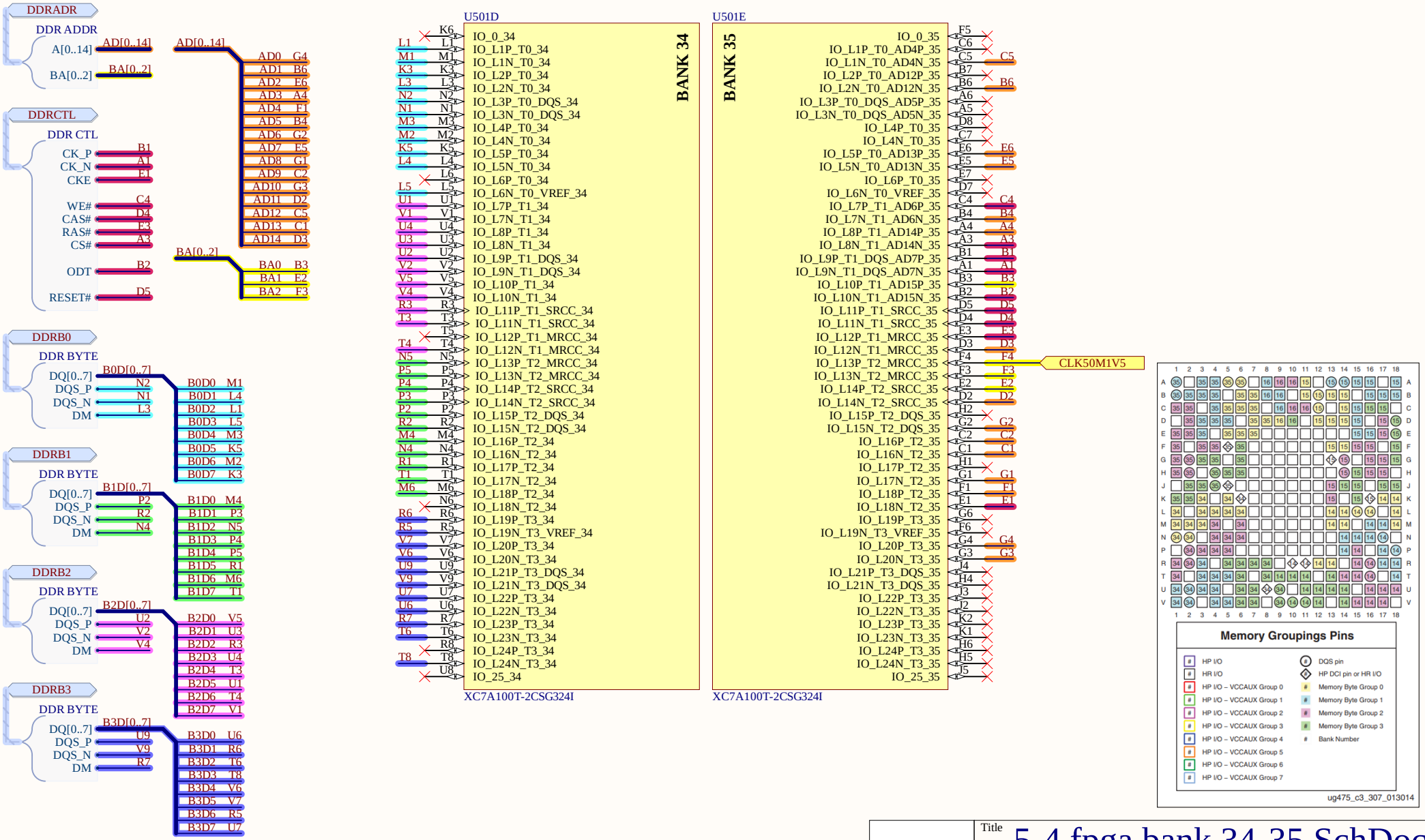


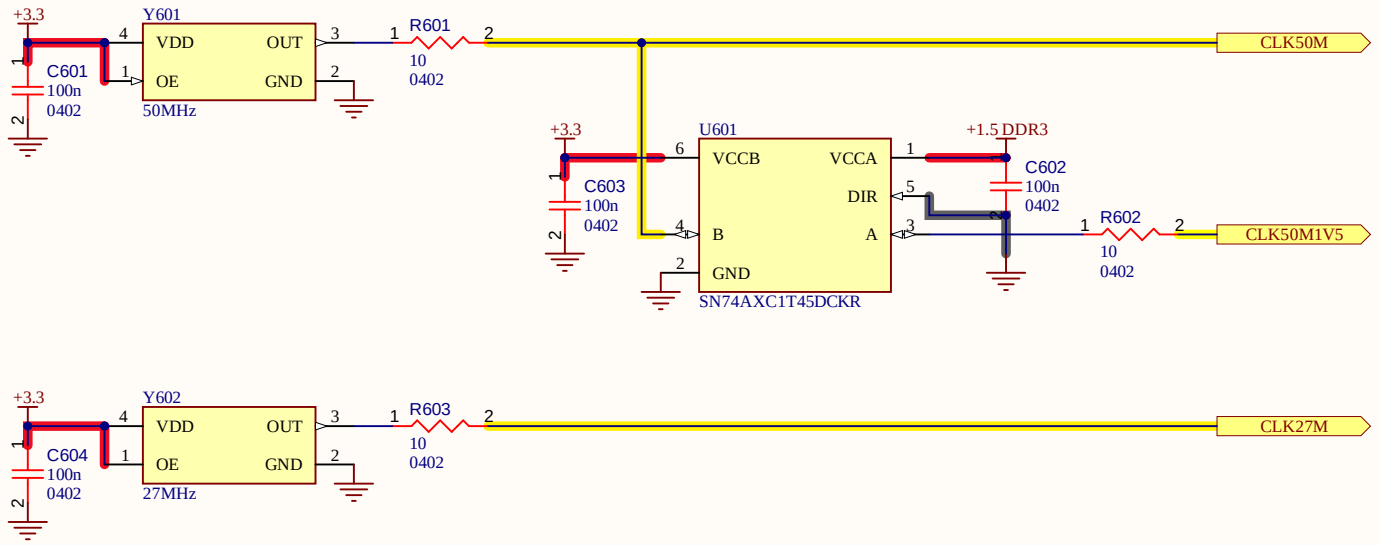
crls design	Title: 5-2 fpga config.SchDoc	
	Size: A4	Number: 6 / 13
	Revision:	
	Date: 12-28-2025	Sheet of
	File: C:\My Drive\..\5-2 fpga config.SchDoc	Drawn By:



Title	5-3 fpga bank 14-16.SchDoc
Size	A4
Number	7 / 13
Revision	
Date:	12-28-2025
Sheet of	12
File:	C:\My Drive\..\5-3 fpga bank 14-16.SchDoc
Drawn By:	

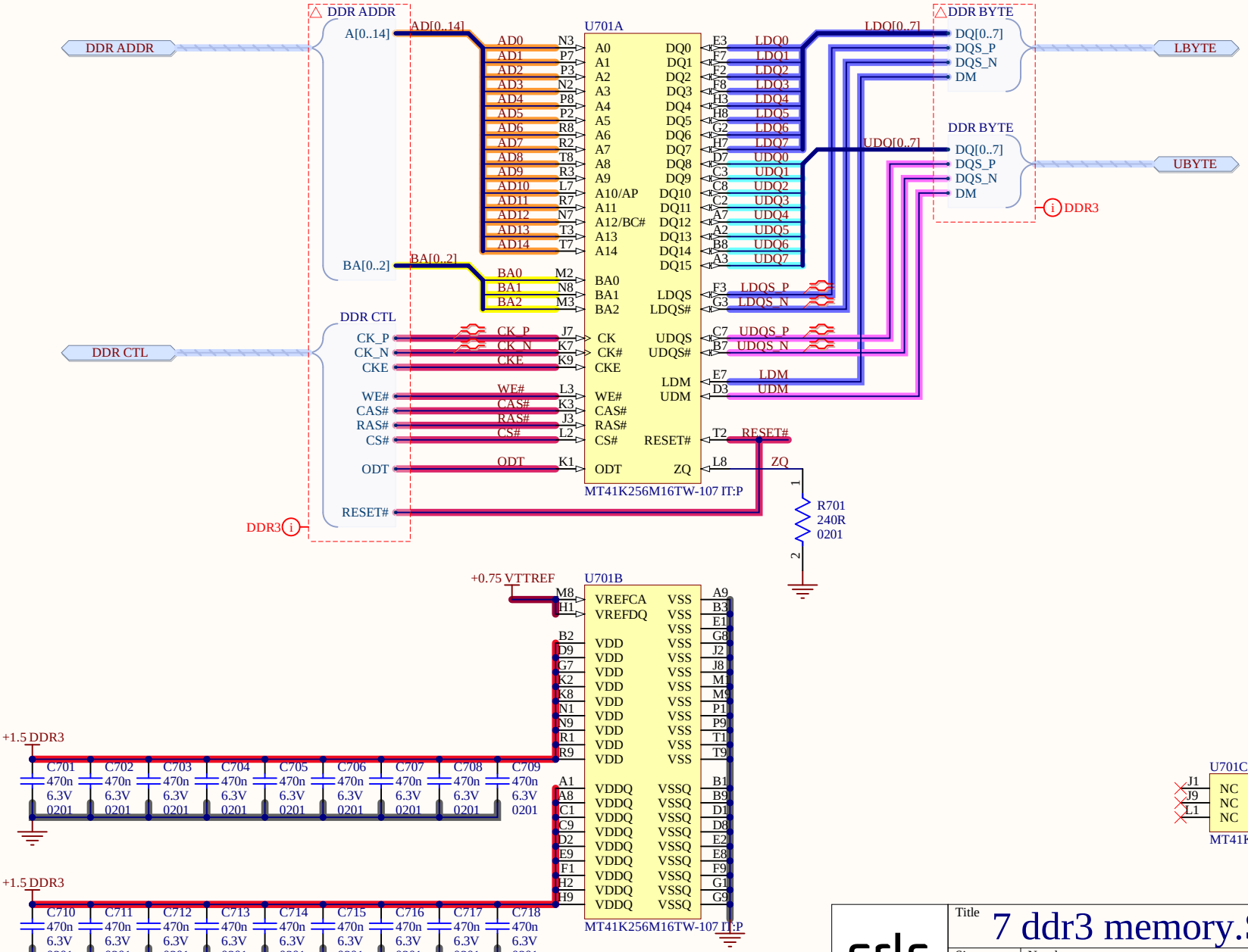
crls design


DDRADR
DDR ADDR
A[0..14]
AD[0..14]
BA[0..2]
BA[0..2]
DDRCTL
DDR CTL
CK_P B1
CK_N A1
CKE E1
WE# C4
CAS# D4
RAS# E3
CS# A3
ODT B2
RESET# D5
AD[0..14]
AD0 G4
AD1 B6
AD2 E6
AD3 A4
AD4 F1
AD5 B4
AD6 G2
AD7 E5
AD8 G1
AD9 C2
AD10 G3
AD11 D2
AD12 C5
AD13 C1
AD14 D3
BA[0..2]
BA0 B3
BA1 E2
BA2 F3
DDRB0
DDR BYTE
DQ[0..7]
DQS_P
DQS_N
DM
B0D[0..7]
N2
N1
L3
B0D0 M1
B0D1 L4
B0D2 L1
B0D3 L5
B0D4 M3
B0D5 K5
B0D6 M2
B0D7 K3
DDRB1
DDR BYTE
DQ[0..7]
DQS_P
DQS_N
DM
B1D[0..7]
P2
R2
N4
B1D0 M4
B1D1 P3
B1D2 N5
B1D3 P4
B1D4 P5
B1D5 R1
B1D6 M6
B1D7 T1
DDRB2
DDR BYTE
DQ[0..7]
DQS_P
DQS_N
DM
B2D[0..7]
U2
V2
V4
B2D0 V5
B2D1 U3
B2D2 R3
B2D3 U4
B2D4 T3
B2D5 U1
B2D6 T4
B2D7 V1
DDRB3
DDR BYTE
DQ[0..7]
DQS_P
DQS_N
DM
B3D[0..7]
U9
V9
R7
B3D0 U6
B3D1 R6
B3D2 T6
B3D3 T8
B3D4 V6
B3D5 V7
B3D6 R5
B3D7 U7
U501D
BANK 34
K6 IO_0_34
L1 IO_L1P_T0_34
M1 IO_L1N_T0_34
K3 IO_L2P_T0_34
L3 IO_L2N_T0_34
N2 IO_L3P_T0_DQS_34
N1 IO_L3N_T0_DQS_34
M3 IO_L4P_T0_34
M2 IO_L4N_T0_34
K5 IO_L5P_T0_34
L4 IO_L5N_T0_34
L6 IO_L6P_T0_34
L5 IO_L6N_T0_VREF_34
U1 IO_L7P_T1_34
V1 IO_L7N_T1_34
U4 IO_L8P_T1_34
U3 IO_L8N_T1_34
U2 IO_L9P_T1_DQS_34
V2 IO_L9N_T1_DQS_34
V5 IO_L10P_T1_34
V4 IO_L10N_T1_34
R3 IO_L11P_T1_SRCC_34
T3 IO_L11N_T1_SRCC_34
T5 IO_L12P_T1_MRCC_34
T4 IO_L12N_T1_MRCC_34
N5 IO_L13P_T2_MRCC_34
P5 IO_L13N_T2_MRCC_34
P4 IO_L14P_T2_SRCC_34
P3 IO_L14N_T2_SRCC_34
P2 IO_L15P_T2_DQS_34
R2 IO_L15N_T2_DQS_34
M4 IO_L16P_T2_34
N4 IO_L16N_T2_34
R1 IO_L17P_T2_34
T1 IO_L17N_T2_34
M6 IO_L18P_T2_34
N6 IO_L18N_T2_34
R6 IO_L19P_T3_34
R5 IO_L19N_T3_VREF_34
V7 IO_L20P_T3_34
V6 IO_L20N_T3_34
U9 IO_L21P_T3_DQS_34
V9 IO_L21N_T3_DQS_34
U7 IO_L22P_T3_34
U6 IO_L22N_T3_34
R7 IO_L23P_T3_34
T6 IO_L23N_T3_34
R8 IO_L24P_T3_34
T8 IO_L24N_T3_34
U8 IO_25_34
XC7A100T-2CSG324I
U501E
BANK 35
F5 IO_0_35
C6 IO_L1P_T0_AD4P_35
C5 IO_L1N_T0_AD4N_35
B7 IO_L2P_T0_AD12P_35
B6 IO_L2N_T0_AD12N_35
A6 IO_L3P_T0_DQS_AD5P_35
A5 IO_L3N_T0_DQS_AD5N_35
D8 IO_L4P_T0_35
C7 IO_L4N_T0_35
E6 IO_L5P_T0_AD13P_35
E5 IO_L5N_T0_AD13N_35
E7 IO_L6P_T0_35
D7 IO_L6N_T0_VREF_35
C4 IO_L7P_T1_AD6P_35
B4 IO_L7N_T1_AD6N_35
A4 IO_L8P_T1_AD14P_35
A3 IO_L8N_T1_AD14N_35
B1 IO_L9P_T1_DQS_AD7P_35
A1 IO_L9N_T1_DQS_AD7N_35
B3 IO_L10P_T1_AD15P_35
B2 IO_L10N_T1_AD15N_35
D5 IO_L11P_T1_SRCC_35
D4 IO_L11N_T1_SRCC_35
E3 IO_L12P_T1_MRCC_35
D3 IO_L12N_T1_MRCC_35
F4 IO_L13P_T2_MRCC_35
F3 IO_L13N_T2_MRCC_35
E2 IO_L14P_T2_SRCC_35
D2 IO_L14N_T2_SRCC_35
H2 IO_L15P_T2_DQS_35
G2 IO_L15N_T2_DQS_35
C2 IO_L16P_T2_35
C1 IO_L16N_T2_35
H1 IO_L17P_T2_35
G1 IO_L17N_T2_35
F1 IO_L18P_T2_35
E1 IO_L18N_T2_35
G6 IO_L19P_T3_35
F6 IO_L19N_T3_VREF_35
G4 IO_L20P_T3_35
G3 IO_L20N_T3_35
J4 IO_L21P_T3_DQS_35
H4 IO_L21N_T3_DQS_35
J3 IO_L22P_T3_35
J2 IO_L22N_T3_35
K2 IO_L23P_T3_35
K1 IO_L23N_T3_35
H6 IO_L24P_T3_35
H5 IO_L24N_T3_35
J5 IO_25_35
XC7A100T-2CSG324I
C5
B6
E6
E5
C4
B4
A4
A3
B1
A1
B3
B2
D5
D4
E3
D3
F4
CLK50M1V5
F3
E2
D2
G2
C2
C1
G1
F1
E1
G4
G3
Memory Groupings Pins
HP I/O
HR I/O
HP I/O – VCCAUX Group 0
HP I/O – VCCAUX Group 1
HP I/O – VCCAUX Group 2
HP I/O – VCCAUX Group 3
HP I/O – VCCAUX Group 4
HP I/O – VCCAUX Group 5
HP I/O – VCCAUX Group 6
HP I/O – VCCAUX Group 7
DQS pin
HP DCI pin or HR I/O
Memory Byte Group 0
Memory Byte Group 1
Memory Byte Group 2
Memory Byte Group 3
Bank Number
ug475_c3_307_013014
crls design
Title
5-4 fpga bank 34-35.SchDoc
Size
A4
Number
8 / 13
Revision
Date: 12-28-2025
Sheet of
File: C:\My Drive\..\5-4 fpga bank 34-35.SchDoc
Drawn By:



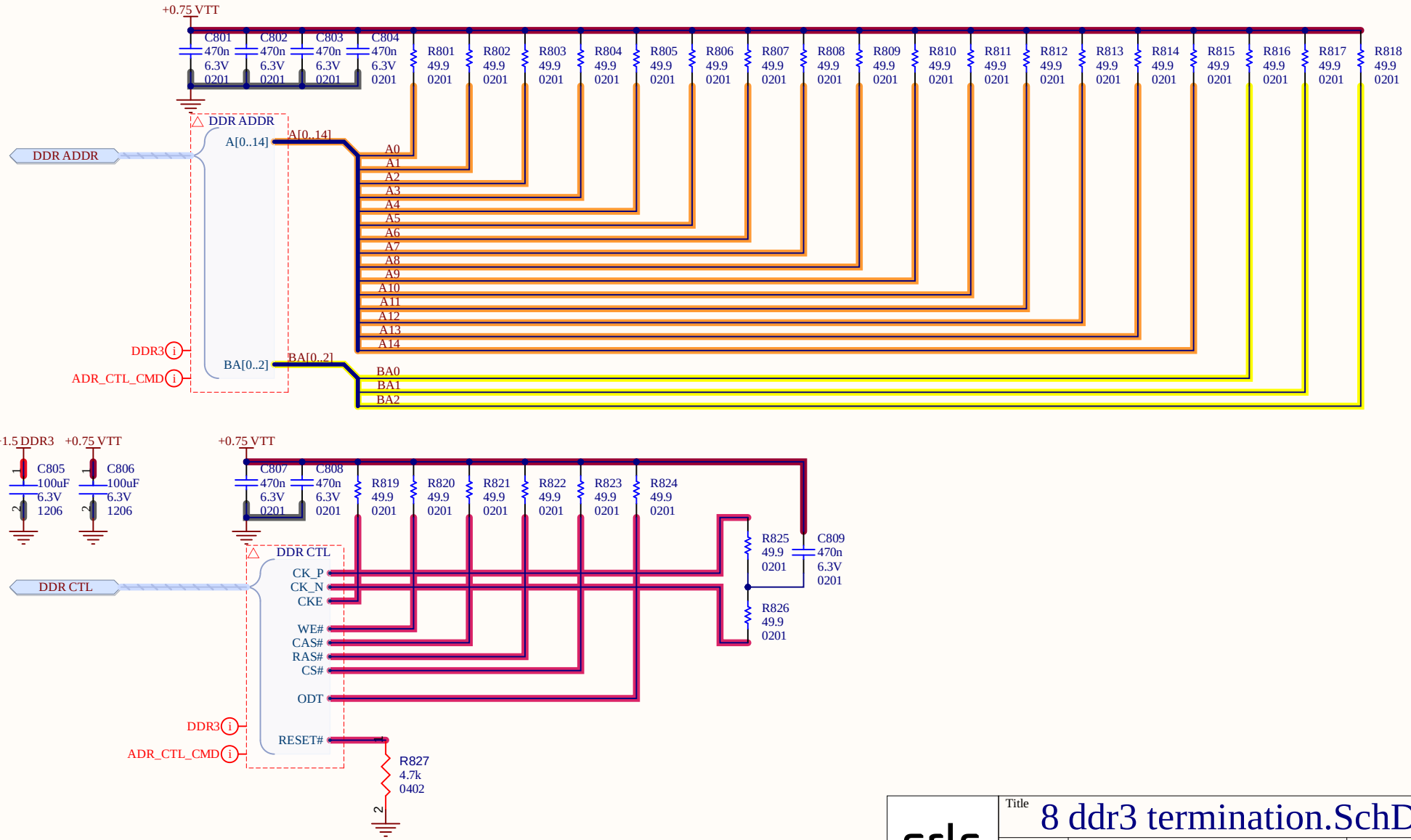
crls design

Title: 6 clock.SchDoc		
Size: A4	Number: 9 / 13	Revision:
Date: 12-28-2025		Sheet of
File: C:\My Drive\..\6 clock.SchDoc		Drawn By:

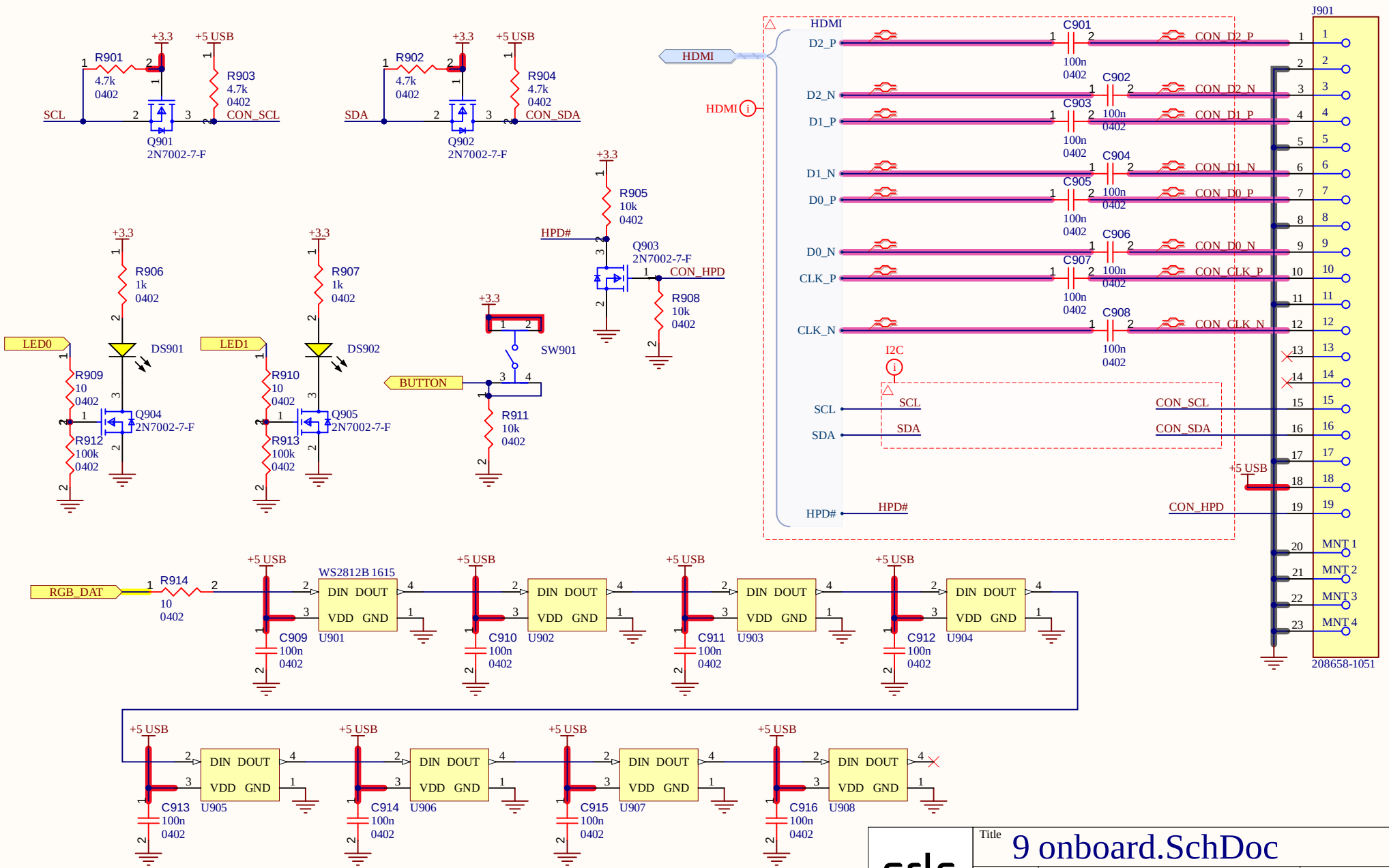


Title	7 ddr3 memory.SchDoc		
Size A4	Number 10 / 13	Revision	
Date: 12-28-2025		Sheet of	
File: C:\My Drive\..\7 ddr3 memory.SchDoc		Drawn By:	

crls design

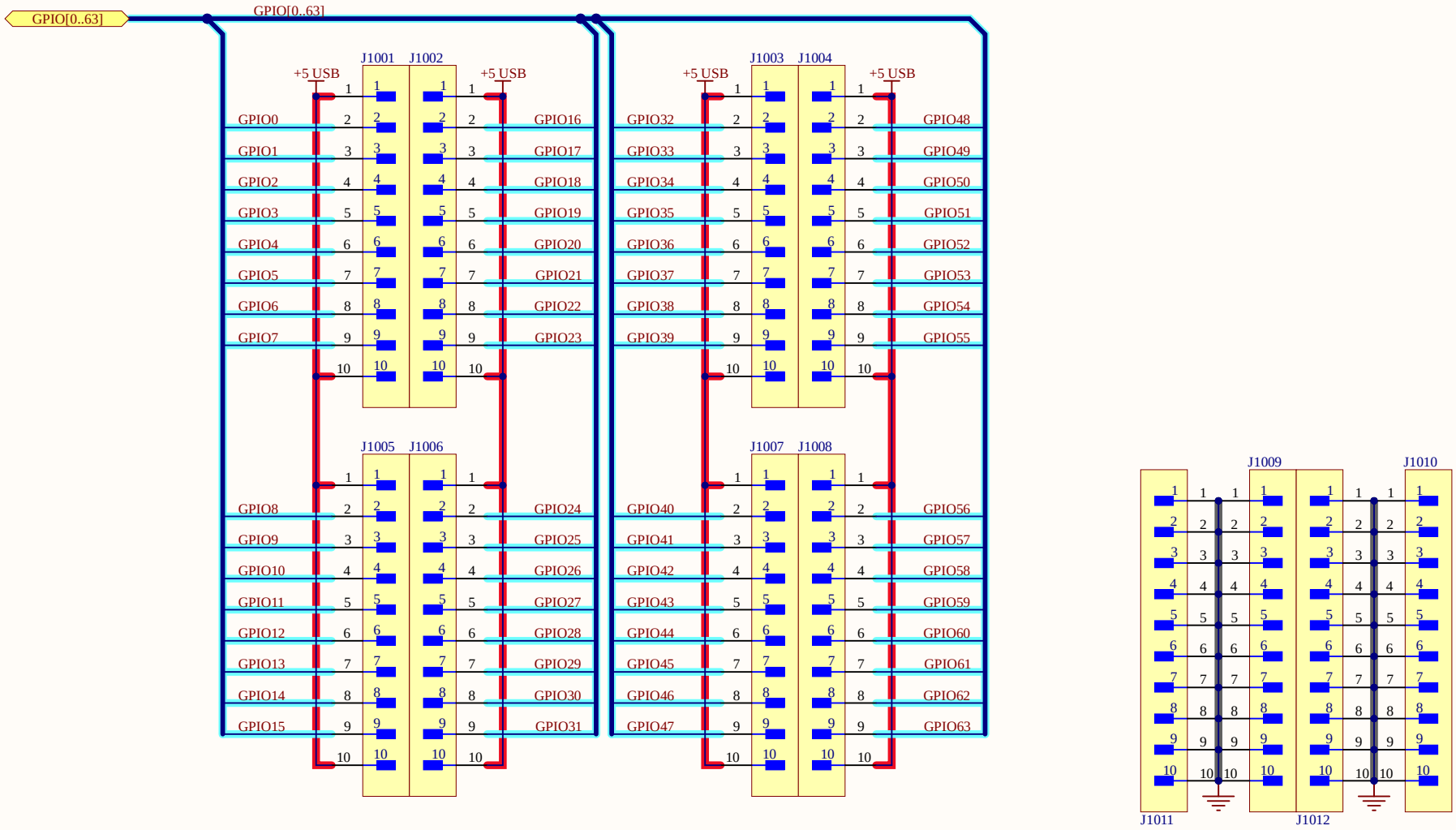


crls design	Title	8 ddr3 termination.SchDoc	
	Size A4	Number 11 / 13	Revision
	Date: 12-28-2025	Sheet of	
	File: C:\My Drive\..\8 ddr3 termination.SchDoc	Drawn By:	



Title	9 onboard.SchDoc	
Size: A4	Number: 12 / 13	Revision:
Date: 12-28-2025		Sheet of
File: C:\My Drive\..\9 onboard.SchDoc		Drawn By:

crls design



crls design

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