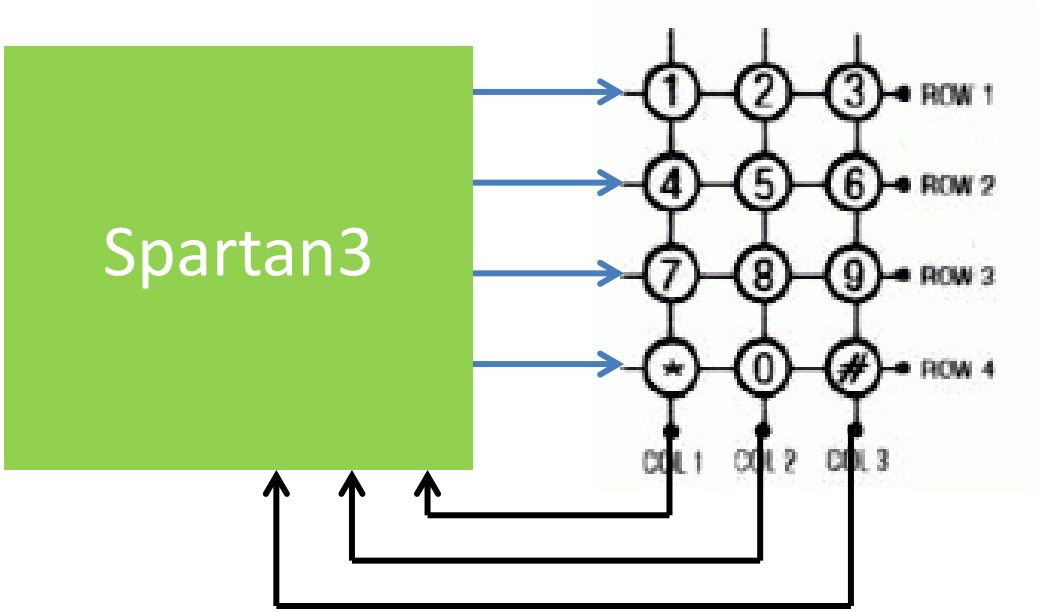
FPGA - Keypad

Asst. Prof. Dr. Wannarat Suntiamorntut

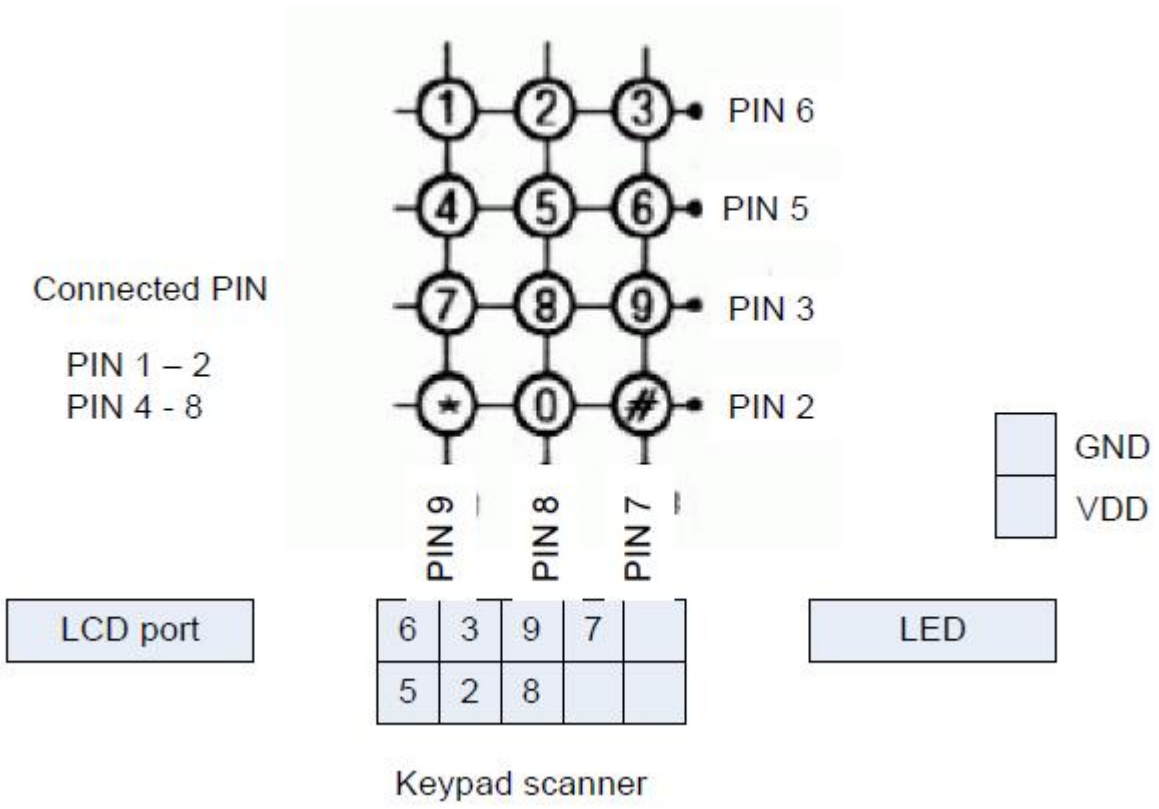
FPGA – Keypad Diagram



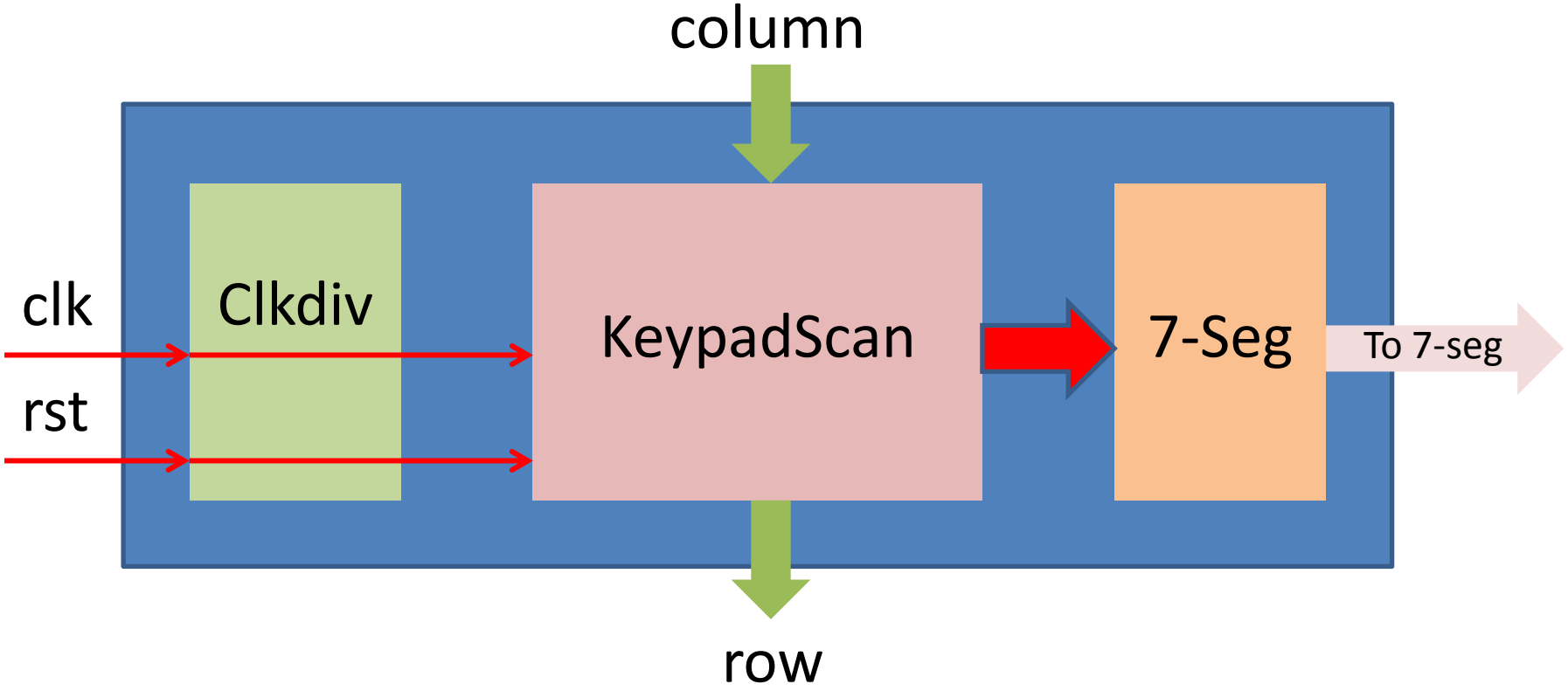
FPGA – Keypad Decoder

Data Output				Data Input			Key Pressed
R1	R2	R3	R4	C1	C2	C3	
0	1	1	1	0	1	1	1
0	1	1	1	1	0	1	2
0	1	1	1	1	1	0	3
1	0	1	1	0	1	1	4
1	0	1	1	1	0	1	5
1	0	1	1	1	1	0	6
1	1	0	1	0	1	1	7
1	1	0	1	1	0	1	8
1	1	0	1	1	1	0	9
1	1	1	0	0	1	1	*
1	1	1	0	1	0	1	0
1	1	1	0	1	1	0	#

FPGA – Keypad Diagram



FPGA – Keypad Scanner & Display

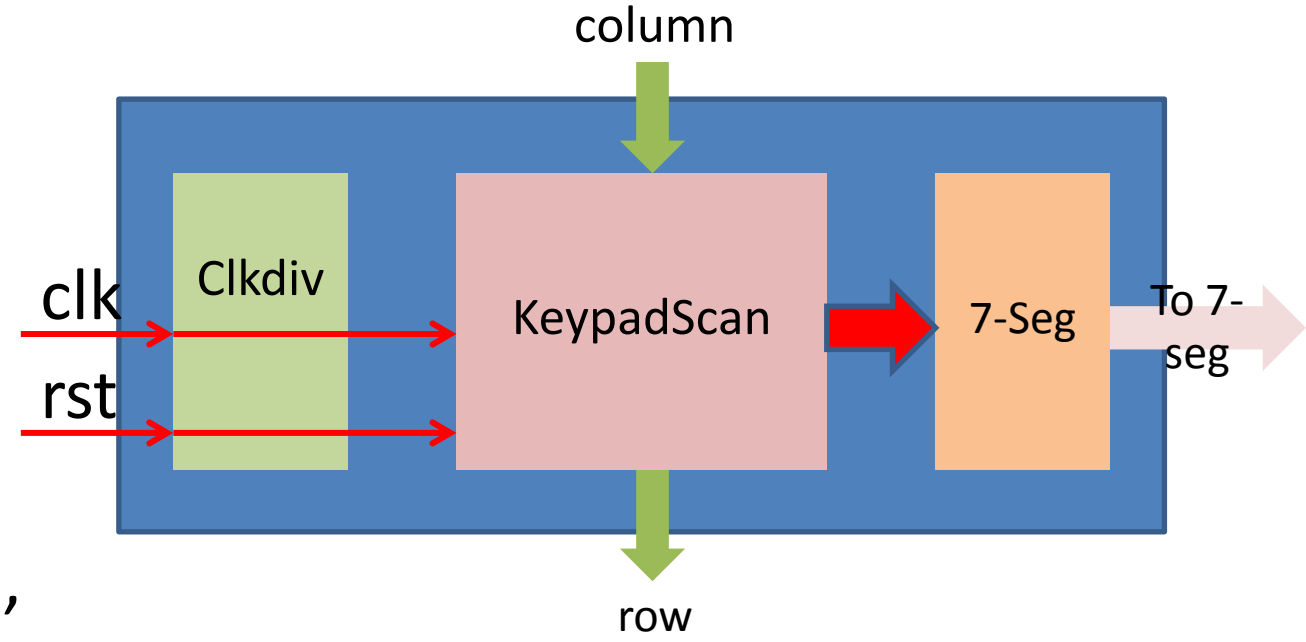


FPGA – Top Module

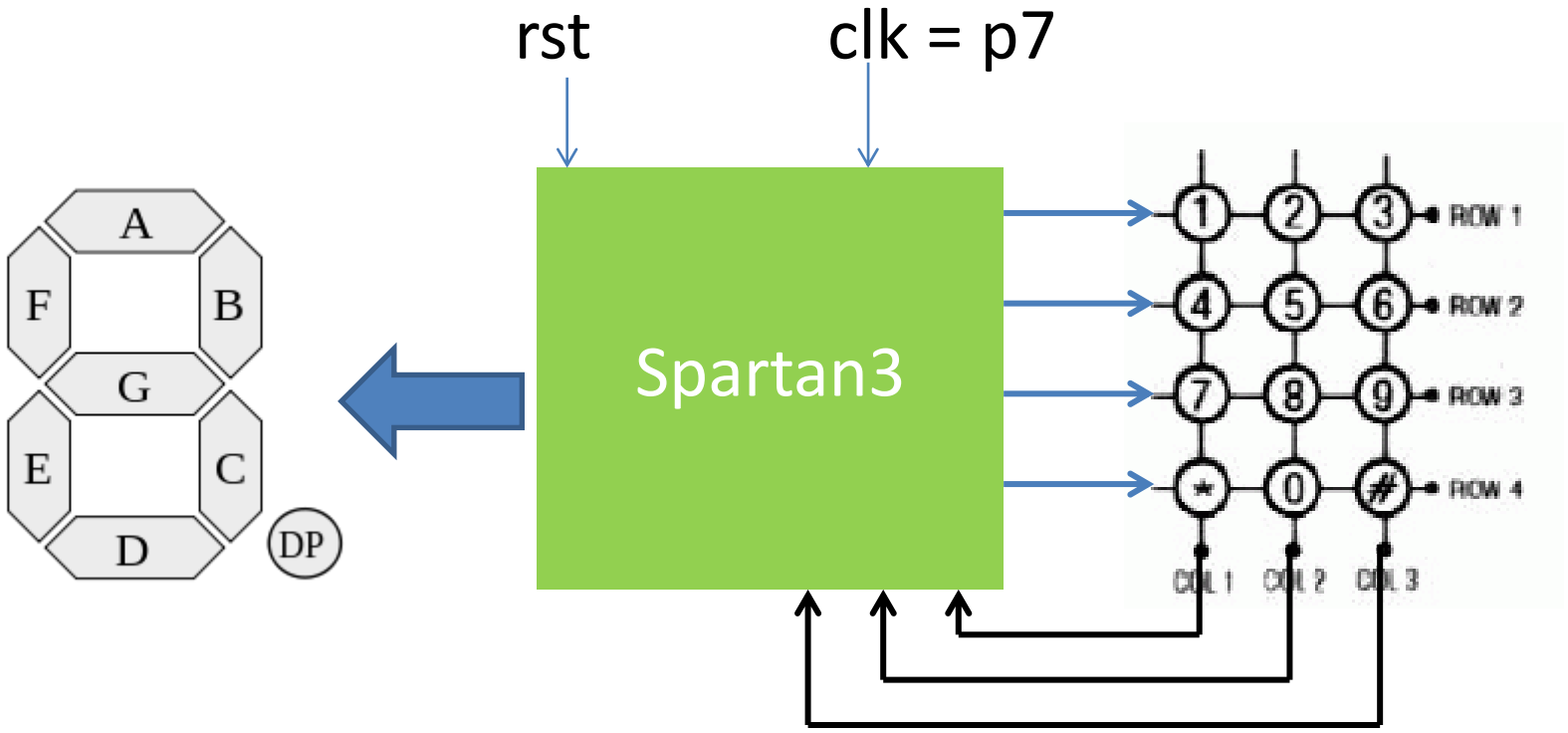
```
module keypadtop (clk,rst,out,row,column,res,digit);
input ….
output …

wire ….

clkdiv u0 (
        .clk_in(clk),
        .rst(rst),
        .q(q)
            );
```



Check-Point



Edit .ucf file and insert this line.

NET "clk" CLOCK_DEDICATED_ROUTE = TRUE;

FPGA – Keypad Scanner & Display