Lab 04

Designing the Controller of the CPU

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Pre-lab	50	50
In-lab Module & Testbench Design	50	50
In-lab Testbench Sim. & Analysis	50	50
In-lab FPGA Synthesis & Analysis	50	50
Lab Report Writing	50	50

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1 Lab Purpose

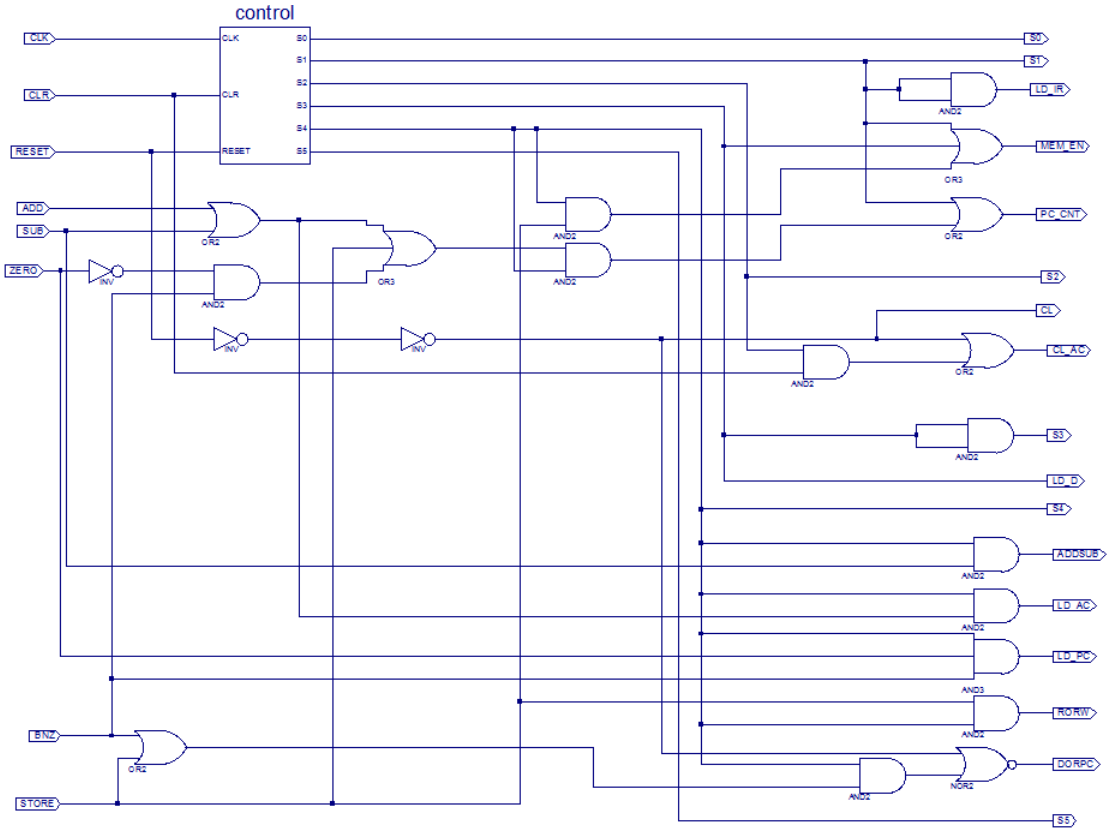
2 Implementation Details

2.1 Part 1

```
//control.v
```

2.2 Part 2

2.3 Part 3




```
//controller_tb.v
```

3 Experimental Results

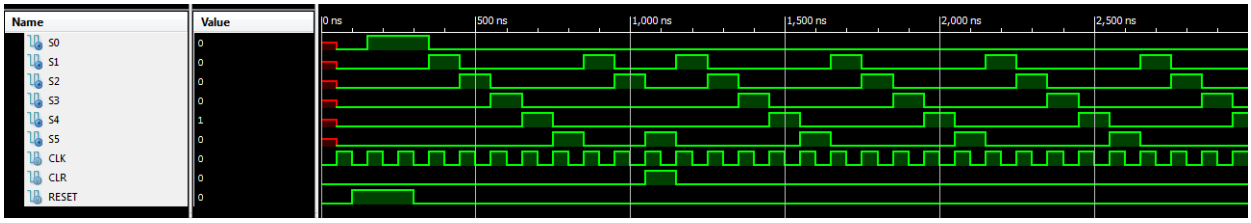


Figure 1:

Figure 2:

4 Significance

5 Comments/Suggestions