MC26LS30

Dual Differential (EIA-422-A)/ Quad Single-Ended (EIA-423-A) Line Drivers

The MC26LS30 is a low power Schottky set of line drivers which can be configured as two differential drivers which comply with EIA−422−A standards, or as four single−ended drivers which comply with EIA−423−A standards. A mode select pin and appropriate choice of power supplies determine the mode. Each driver can source and sink currents in excess of 50 mA.

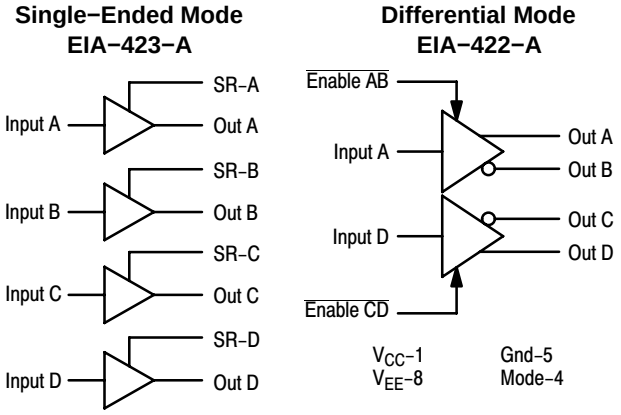
In the differential mode (EIA−422−A), the drivers can be used up to 10 Mbaud. A disable pin for each driver permits setting the outputs into a high impedance mode within a +10 V common mode range.

In the single−ended mode (EIA−423−A), each driver has a slew rate control pin which permits setting the slew rate of the output signal so as to comply with EIA−423−A and FCC requirements and to reduce crosstalk. When operated from symmetrical supplies (+5.0 V), the outputs exhibit zero imbalance

The MC26LS30 is available in a 16−pin surface mount package. Operating temperature range is −40°C to +85°C.

- Operates as Two Differential EIA−422−A Drivers, or Four Single−Ended EIA−423−A Drivers
- High Impedance Outputs in Differential Mode
- Short Circuit Current Limit In Both Source and Sink Modes
- ±10 V Common Mode Range on High Impedance Outputs
- ±15 V Range on Inputs
- Low Current PNP Inputs Compatible with TTL, CMOS, and MOS Outputs
- Individual Output Slew Rate Control in Single−Ended Mode
- Replacement for the AMD AM26LS30 and National Semiconductor DS3691
- Pb−Free Packages are Available

Representative Block Diagrams



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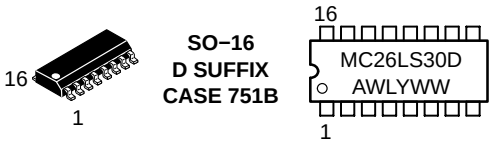
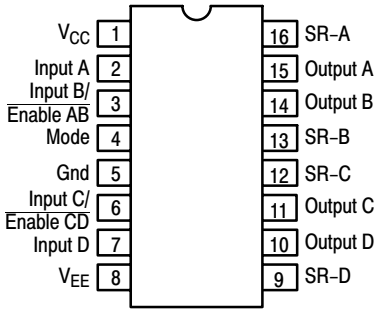
MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
MC26LS30D	SO−16	48 Units/Rail
MC26LS30DG	SO−16 (Pb−Free)	48 Units/Rail
MC26LS30DR2	SO−16	2500 Tape & Reel
MC26LS30DR2G	SO−16 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MAXIMUM OPERATING CONDITIONS (Pin numbers refer to SO−16 package only.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	−0.5, +7.0 −7.0, +0.5	Vdc
Input Voltage (All Inputs)	V_{in}	−0.5, +20	Vdc
Applied Output Voltage when in High Impedance Mode (V_{CC} = 5.0 V, Pin 4 = Logic 0, Pins 3, 6 = Logic 1) Output Voltage with V_{CC}, V_{EE} = 0 V	V_{za} V_{zb}	±15 ±15	Vdc
Output Current	I_O	Self limiting	−
Junction Temperature	T_J	−65, +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.
Devices should not be operated at these limits. The “Recommended Operating Conditions” table provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (Differential Mode)	V_{CC} V_{EE}	+4.75 −0.5	5.0 0	+5.25 +0.3	Vdc
Power Supply Voltage (Single−Ended Mode)	V_{CC} V_{EE}	+4.75 −5.25	+5.0 −5.0	+5.25 −4.75	
Input Voltage (All Inputs)	V_{in}	0	−	+15	Vdc
Applied Output Voltage (when in High Impedance Mode)	V_{za}	−10	−	+10	
Applied Output Voltage, V_{CC} = 0	V_{zb}	−10	−	+10	
Output Current	I_O	−65	−	+65	mA
Operating Ambient Temperature (See text)	T_A	−40	−	+85	°C

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (EIA−422−A differential mode, Pin 4 ≤ 0.8 V, −40°C < T_A < 85°C, 4.75 V ≤ V_{CC} ≤ 5.25 V, V_{EE} = Gnd, unless otherwise noted. Pin numbers refer to SO−16 package only.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (see Figure 1)					
Differential, R_L = ∞, V_{CC} = 5.25 V	$\|V_{OD1}\|$	−	4.2	6.0	Vdc
Differential, R_L = 100 Ω, V_{CC} = 4.75 V	$\|V_{OD2}\|$	2.0	2.6	−	Vdc
Change in Differential Voltage, R_L = 100 Ω (Note 4)	$\|\Delta V_{OD2}\|$	−	10	400	mVdc
Offset Voltage, R_L = 100 Ω	V_{OS}	−	2.5	3.0	Vdc
Change in Offset Voltage*, R_L = 100 Ω	$\|\Delta V_{OS}\|$	−	10	400	mVdc
Output Current (each output)					
Power Off Leakage, V_{CC} = 0, −10 V ≤ V_O ≤ +10 V	I_{OLK}	−100	0	+100	μA
High Impedance Mode, V_{CC} = 5.25 V, −10 V ≤ V_O ≤ +10 V	I_{OZ}	−100	0	+100	
Short Circuit Current (Note 2)					
High Output Shorted to Pin 5 (T_A = 25°C)	I_{SC-}	−150	−95	−60	mA
High Output Shorted to Pin 5 (−40°C < T_A < +85°C)	I_{SC-}	−150	−	−50	
Low Output Shorted to +6.0 V (T_A = 25°C)	I_{SC+}	60	75	150	
Low Output Shorted to +6.0 V (−40°C < T_A < +85°C)	I_{SC+}	50	−	150	
Inputs					
Low Level Voltage	V_{IL}	−	−	0.8	Vdc
High Level Voltage	V_{IH}	2.0	−	−	Vdc
Current @ V_{in} = 2.4 V	I_{IH}	−	0	40	μA
Current @ V_{in} = 15 V	I_{IHH}	−	0	100	
Current @ V_{in} = 0.4 V	I_{IL}	−200	−8.0	−	
Current, 0 ≤ V_{in} ≤ 15 V, V_{CC} = 0	I_{IX}	−	0	−	
Clamp Voltage (I_{in} = −12 mA)	V_{IK}	−1.5	−	−	Vdc
Power Supply Current (V_{CC} = +5.25 V, Outputs Open) (0 ≤ Enable ≤ V_{CC})	I_{CC}	−	16	30	mA

TIMING CHARACTERISTICS (EIA−422−A differential mode, Pin 4 ≤ 0.8 V, T_A = 25°C, V_{CC} = 5.0 V, V_{EE} = Gnd, (Notes 1 and 3) unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Differential Output Rise Time (Figure 3)	t_r	−	70	200	ns
Differential Output Fall Time (Figure 3)	t_f	−	70	200	ns
Propagation Delay Time − Input to Differential Output					ns
Input Low to High (Figure 3)	t_{PDH}	−	90	200	
Input High to Low (Figure 3)	t_{PDL}	−	90	200	
Skew Timing (Figure 3)					ns
$\|t_{PDH}$ to $t_{PDL}\|$ for Each Driver	t_{SK1}	−	9.0	−	
Max to Min t_{PDH} Within a Package	t_{SK2}	−	2.0	−	
Max to Min t_{PDL} Within a Package	t_{SK3}	−	2.0	−	
Enable Timing (Figure 4)					ns
Enable to Active High Differential Output	t_{PZH}	−	150	300	
Enable to Active Low Differential Output	t_{PZL}	−	190	350	
Enable to 3−State Output From Active High	t_{PHZ}	−	80	350	
Enable to 3−State Output From Active Low	t_{PLZ}	−	110	300	

1. All voltages measured with respect to Pin 5.
2. Only one output shorted at a time, for not more than 1 second.
3. Typical values established at +25°C, V_{CC} = +5.0 V, V_{EE} = −5.0 V.
4. V_{in} switched from 0.8 to 2.0 V.
5. Imbalance is the difference between $|V_{O2}|$ with V_{in} < 0.8 V and $|V_{O2}|$ with V_{in} > 2.0 V.

ELECTRICAL CHARACTERISTICS (EIA−423−A single−ended mode, Pin 4 ≥ 2.0 V, −40°C < T_A < 85°C, 4.75 V ≤ $|V_{CC}|$, $|V_{EE}|$ ≤ 5.25 V, (Notes 1 and 3) unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (V_{CC} = $\|V_{EE}\|$ = 4.75 V)					Vdc
Single−Ended Voltage, R_L = ∞ (Figure 2)	$\|V_{O1}\|$	4.0	4.2	6.0	
Single−Ended Voltage, R_L = 450 Ω, (Figure 2)	$\|V_{O2}\|$	3.6	3.95	6.0	
Voltage Imbalance (Note 5), R_L = 450 Ω	$\|\Delta V_{O2}\|$	−	0.05	0.4	
Slew Control Current (Pins 16, 13, 12, 9)	I_{SLEW}	−	±120	−	μA
Output Current (Each Output)					
Power Off Leakage, V_{CC} = V_{EE} = 0, −6.0 V ≤ V_O ≤ +6.0 V	I_{OLK}	−100	0	+100	μA
Short Circuit Current (Output Short to Ground, Note 2)					
V_{in} ≤ 0.8 V (T_A = 25°C)	I_{SC+}	60	80	150	mA
V_{in} ≤ 0.8 V (−40°C < T_A < +85°C)	I_{SC+}	50	−	150	
V_{in} ≥ 2.0 V (T_A = 25°C)	$I_{SC−}$	−150	−95	−60	
V_{in} ≥ 2.0 V (−40°C < T_A < +85°C)	$I_{SC−}$	−150	−	−50	
Inputs					
Low Level Voltage	V_{IL}	−	−	0.8	Vdc
High Level Voltage	V_{IH}	2.0	−	−	Vdc
Current @ V_{in} = 2.4 V	I_{IH}	−	0	40	μA
Current @ V_{in} = 15 V	I_{IHH}	−	0	100	
Current @ V_{in} = 0.4 V	I_{IL}	−200	−8.0	−	
Current, 0 ≤ V_{in} ≤ 15 V, V_{CC} = 0	I_{IX}	−	0	−	
Clamp Voltage (I_{in} = −12 mA)	V_{IK}	−1.5	−	−	Vdc
Power Supply Current (Outputs Open)	I_{CC}	−	17	30	mA
V_{CC} = +5.25 V, V_{EE} = −5.25 V, V_{in} = 0.4 V	I_{EE}	−22	−8.0	−	

TIMING CHARACTERISTICS (EIA−423−A single−ended mode, Pin 4 ≥ 2.0 V, T_A = 25°C, V_{CC} = 5.0 V, V_{EE} = −5.0 V, (Notes 1 and 3) unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Timing (Figure 5)					
Output Rise Time, C_C = 0	t_r	−	65	300	ns
Output Fall Time, C_C = 0	t_f	−	65	300	
Output Rise Time, C_C = 50 pF	t_r	−	3.0	−	μs
Output Fall Time, C_C = 50 pF	t_f	−	3.0	−	
Rise Time Coefficient (Figure 16)	C_{rt}	−	0.06	−	μs/pF
Propagation Delay Time, Input to Single Ended Output (Figure 5)					ns
Input Low to High, C_C = 0	t_{PDH}	−	100	300	
Input High to Low, C_C = 0	t_{PDL}	−	100	300	
Skew Timing, C_C = 0 (Figure 5)					ns
$\|t_{PDH}$ to $t_{PDL}\|$ for Each Driver	t_{SK4}	−	15	−	
Max to Min t_{PDH} Within a Package	t_{SK5}	−	2.0	−	
Max to Min t_{PDL} Within a Package	t_{SK6}	−	5.0	−	

1. All voltages measured with respect to Pin 5.
2. Only one output shorted at a time, for not more than 1 second.
3. Typical values established at +25°C, V_{CC} = +5.0 V, V_{EE} = −5.0 V.
4. V_{in} switched from 0.8 to 2.0 V.
5. Imbalance is the difference between $|V_{O2}|$ with V_{in} < 0.8 V and $|V_{O2}|$ with V_{in} > 2.0 V.

Table 1

Operation	V_{CC}	V_{EE}	Inputs					Outputs			
			Mode	A	B	C	D	A	B	C	D
Differential (EIA−422−A)	+5.0	Gnd	0	0	0	0	0	0	1	1	0
			0	1	0	0	1	1	0	0	1
			0	X	1	0	1	Z	Z	0	1
			0	1	0	0	0	1	0	1	0
			0	0	0	0	1	0	1	0	1
			0	1	0	1	X	1	0	Z	Z
Single−Ended (EIA−423−A)	+5.0	−5.0	1	0	0	0	0	0	0	0	0
			1	1	0	0	0	1	0	0	0
			1	0	1	0	0	0	1	0	0
			1	0	0	1	0	0	0	1	0
			1	0	0	0	1	0	0	0	1
X	0	X	X	X	X	X	X	Z	Z	Z	Z

X = Don't Care
Z = High Impedance (Off)

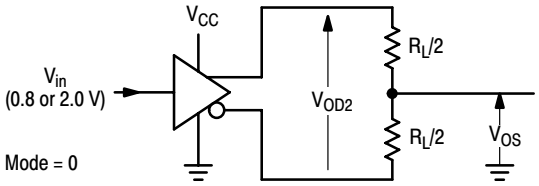


Figure 1. Differential Output Test

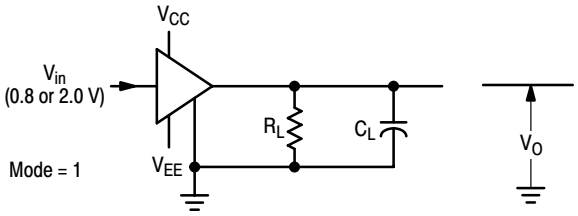
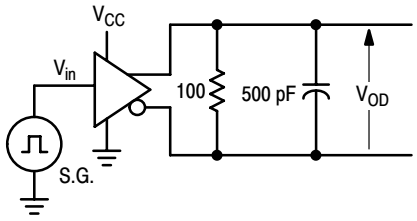
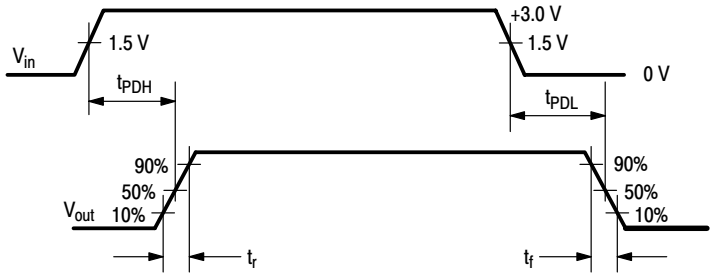


Figure 2. Single−Ended Output Test

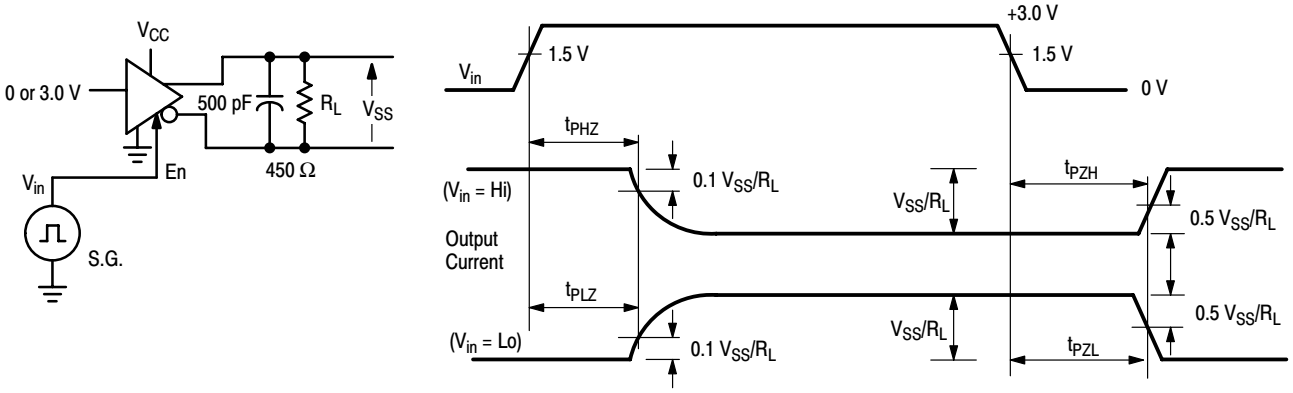




NOTES:

1. S.G. set to: f ≤ 1.0 MHz; duty cycle = 50%; t_r, t_f, ≤ 10 ns.
2. $t_{SK1} = |t_{PDH} - t_{PDL}|$ for each driver.
3. t_{SK2} computed by subtracting the shortest t_{PDH} from the longest t_{PDH} of the 2 drivers within a package.
4. t_{SK3} computed by subtracting the shortest t_{PDL} from the longest t_{PDL} of the 2 drivers within a package.

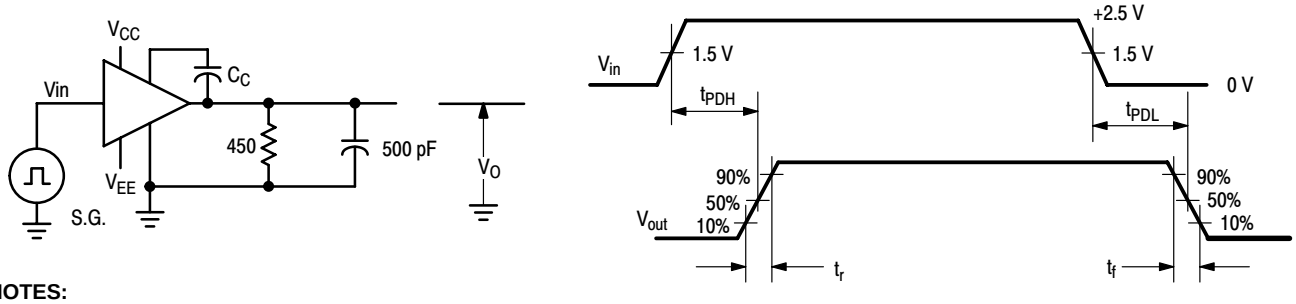
Figure 3. Differential Mode Rise/Fall Time and Data Propagation Delay



NOTES:

1. S.G. set to: f ≤ 1.0 MHz; duty cycle = 50%; t_r, t_f, ≤ 10 ns.
2. Above tests conducted by monitoring output current levels.

Figure 4. Differential Mode Enable Timing



NOTES:

1. S.G. set to: f ≤ 100 kHz; duty cycle = 50%; t_r, t_f, ≤ 10 ns.
2. $t_{SK4} = |t_{PDH} - t_{PDL}|$ for each driver.
3. t_{SK5} computed by subtracting the shortest t_{PDH} from the longest t_{PDH} of the 4 drivers within a package.
4. t_{SK6} computed by subtracting the shortest t_{PDL} from the longest t_{PDL} of the 4 drivers within a package.

Figure 5. Single−Ended Mode Rise/Fall Time and Data Propagation Delay

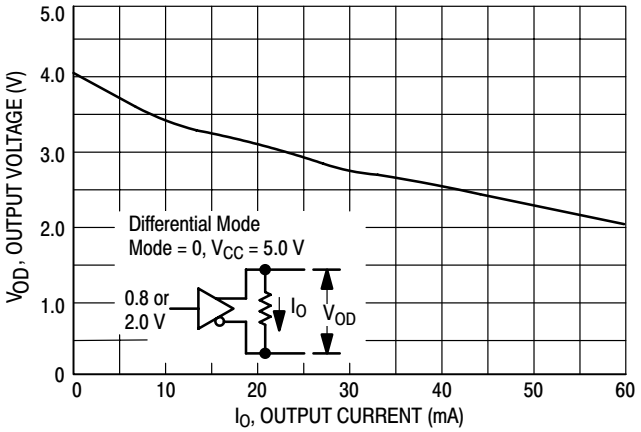


Figure 6. Differential Output Voltage versus Load Current

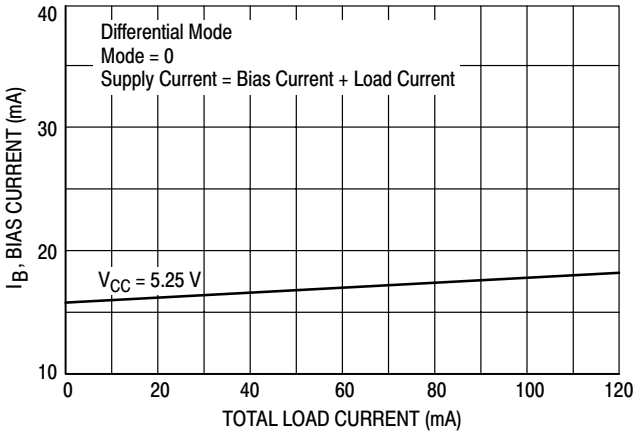


Figure 7. Internal Bias Current versus Load Current

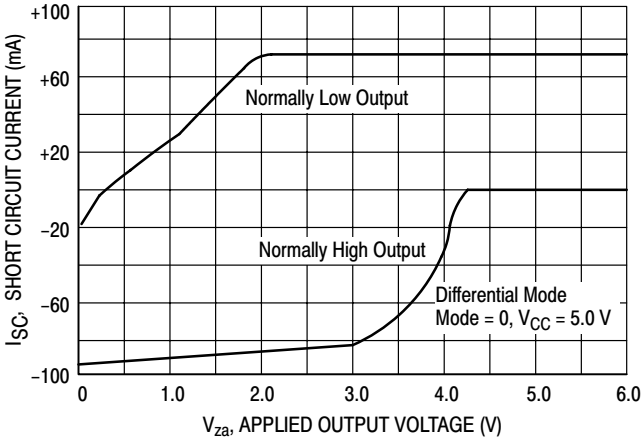
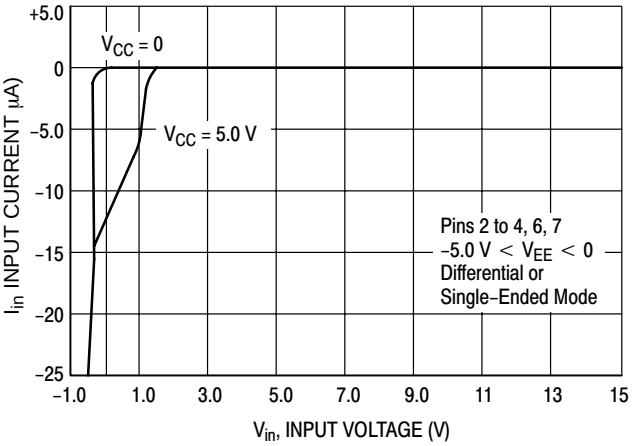


Figure 8. Short Circuit Current versus Output Voltage



(Pin numbers refer to SO−16 package only.)

Figure 9. Input Current versus Input Voltage

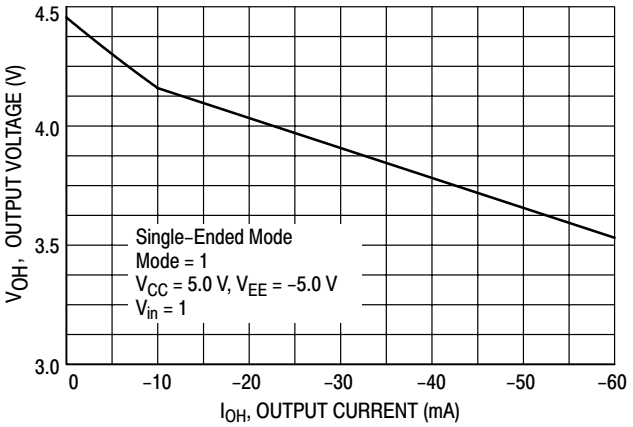


Figure 10. Output Voltage versus Output Source Current

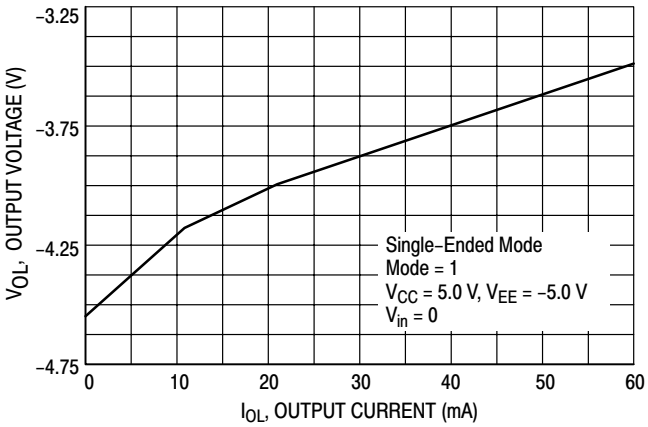


Figure 11. Output Voltage versus Output Sink Current

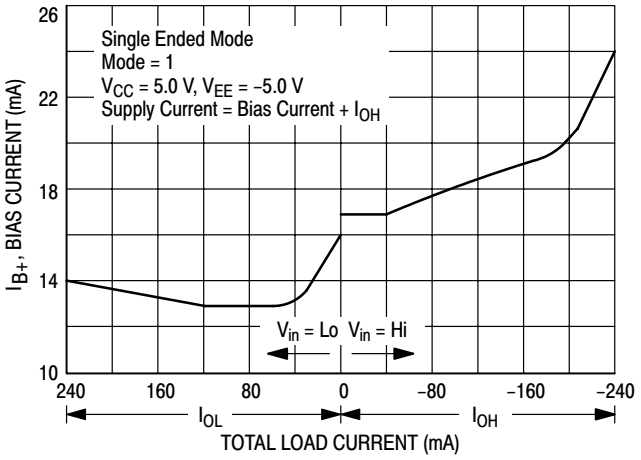


Figure 12. Internal Positive Bias Current versus Load Current

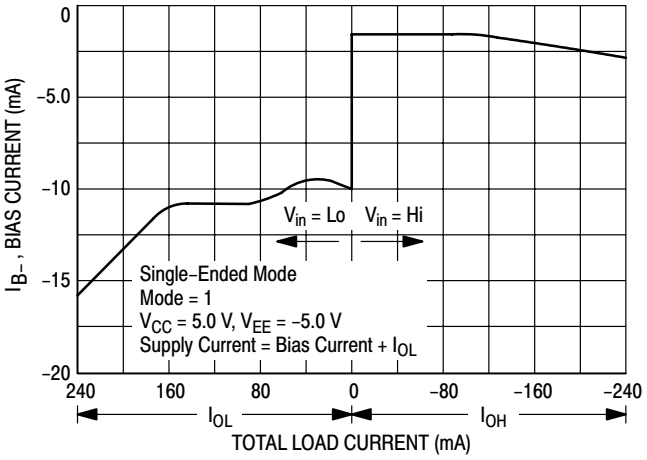


Figure 13. Internal Negative Bias Current versus Load Current

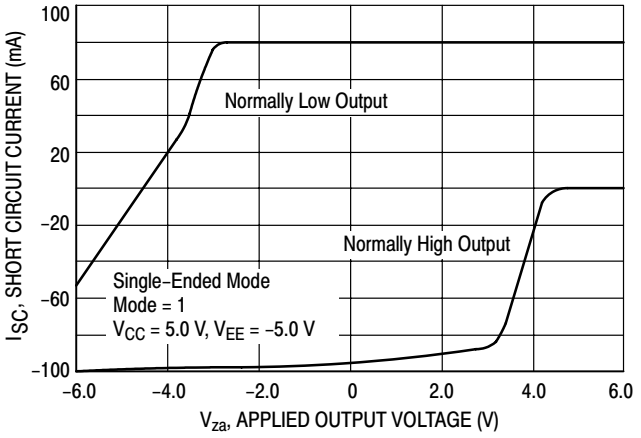


Figure 14. Short Circuit Current versus Output Voltage

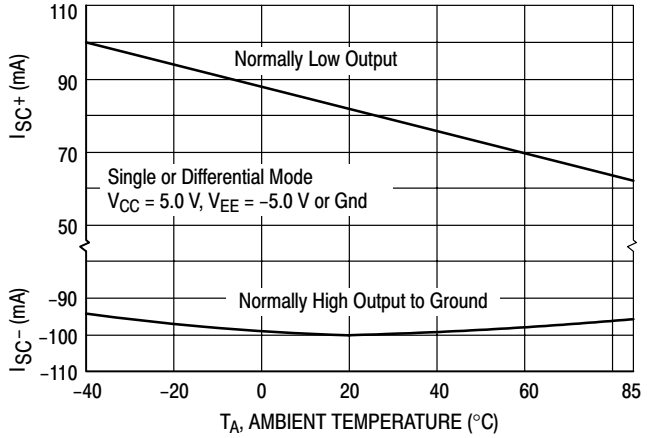


Figure 15. Short Circuit Current versus Temperature

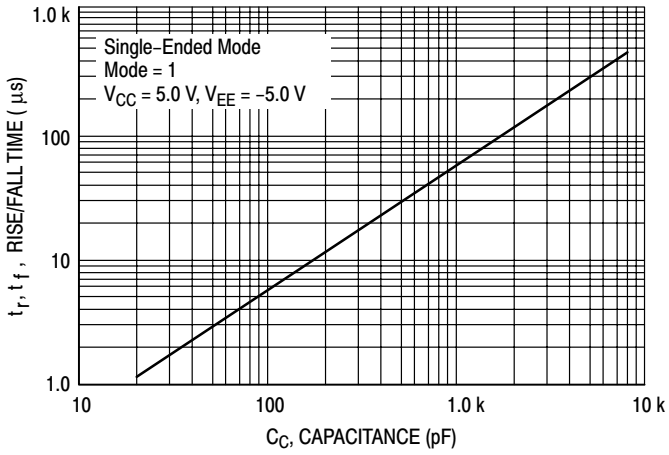


Figure 16. Rise/Fall Time versus Capacitance

APPLICATIONS INFORMATION

(Pin numbers refer to SO−16 package only.)

Description

The MC26LS30 is a dual function line driver − it can be configured as two differential output drivers which comply with EIA−422−A Standard, or as four single−ended drivers which comply with EIA−423−A Standard. The mode of operation is selected with the Mode pin (Pin 4) and appropriate power supplies (see Table 1). Each of the four outputs is capable of sourcing and sinking 60 to 70 mA while providing sufficient voltage to ensure proper data transmission.

As differential drivers, data rates to 10 Mbaud can be transmitted over a twisted pair for a distance determined by the cable characteristics. EIA−422−A Standard provides guidelines for cable length versus data rate. The advantage of a differential (balanced) system over a single−ended system is greater noise immunity, common mode rejection, and higher data rates.

Where extraneous noise sources are not a problem, the MC26LS30 may be configured as four single−ended drivers transmitting data rates to 100 Kbaud. Crosstalk among wires within a cable is controlled by the use of the slew rate control pins on the MC26LS30.

Mode Selection (Differential Mode)

In this mode (Pins 4 and 8 at ground), only a +5.0 V supply ±5% is required at V_{CC}. Pins 2 and 7 are the driver inputs, while Pins 10, 11, 14 and 15 are the outputs (see Block Diagram on page 1). The two outputs of a driver are always complementary and the differential voltage available at each pair of outputs is shown in Figure 6 for V_{CC} = 5.0 V. The differential output voltage will vary directly with V_{CC}. A “high” output can only source current, while a “low” output can only sink current (except for short circuit current − see Figure 8).

The two outputs will be in a high impedance mode when the respective Enable input (Pin 3 or 6) is high, or if $V_{CC} \leq$ 1.1 V. Output leakage current over a common mode range of ± 10 V is typically less than 1.0 μA.

The outputs have short circuit current limiting, typically, less than 100 mA over a voltage range of 0 to +6.0 V (see Figure 8). Short circuits should not be allowed to last indefinitely as the IC may be damaged.

Pins 9, 12, 13 and 16 are not normally used when in this mode, and should be left open.

(Single−Ended Mode)

In this mode (Pin 4 ≥ 2.0 V) V_{CC} requires +5.0 V, and V_{EE} requires −5.0 V, both ±5.0%. Pins 2, 3, 6, and 7 are inputs for the four drivers, and Pins 15, 14, 11, and 10 (respectively) are the outputs. The four drivers are independent of each other, and each output will be at a positive or a negative voltage depending on its input state, the load current, and the supply voltage. Figures 10 & 11 indicate the high and low output voltages for V_{CC} = 5.0 V, and V_{EE} = −5.0 V. The graph of Figure 10 will vary directly with V_{CC}, and the graph of Figure 11 will vary directly with V_{EE}. A “high” output can only source current, while a “low” output can only sink current (except short circuit current − see Figure 14).

The outputs will be in a high impedance mode only if $V_{CC} \leq$ 1.1 V. Changing V_{EE} to 0 V does not set the outputs to a high impedance mode. Leakage current over a common mode range of ±10 V is typically less than 1.0 μA.

The outputs have short circuit current limiting, typically less than 100 mA over a voltage range of ±6.0 V (see Figure 14). Short circuits should not be allowed to last indefinitely as the IC may be damaged.

Capacitors connected between Pins 9, 12, 13, and 16 and their respective outputs will provide slew rate limiting of the output transition. Figure 16 indicates the required capacitor value to obtain a desired rise or fall time (measured between the 10% and 90% points). The positive and negative transition times will be within ≈ ±5% of each other. Each output may be set to a different slew rate if desired.

Inputs

The five inputs determine the state of the outputs in accordance with Table 1. All inputs (regardless of the operating mode) have a nominal threshold of +1.3 V, and their voltage must be kept within a range of 0 V to +15 V for proper operation. If an input is taken more than 0.3 V below ground, excessive currents will flow, and the proper operation of the drivers will be affected. An open pin is equivalent to a logic high, but good design practices dictate that inputs should never be left open. Unused inputs should be connected to ground. The characteristics of the inputs are shown in Figure 9.

Power Supplies

V_{CC} requires +5.0 V, ±5%, regardless of the mode of operation. The supply current is determined by the IC’s internal bias requirements and the total load current. The internally required current is a function of the load current and is shown in Figure 7 for the differential mode.

In the single−ended mode, V_{EE} must be −5.0 V, ±5% in order to comply with EIA−423−A standards. Figures 12 and 13 indicate the internally required bias currents as a function of total load current (the sum of the four output loads). The discontinuity at 0 load current exists due to a change in bias current when the inputs are switched. The supply currents vary ≈ ± 2.0 mA as V_{CC} and V_{EE} are varied from |4.75 V| to |5.25 V|.

Sequencing of the supplies during power−up/ power−down is not required.

Bypass capacitors (0.1 μF minimum on each supply pin) are recommended to ensure proper operation. Capacitors reduce noise induced onto the supply lines by the switching action of the drivers, particularly where long P.C. board tracks are involved. Additionally, the capacitors help absorb

transients induced onto the drivers' outputs from the external cable (from ESD, motor noise, nearby computers, etc.).

Operating Temperature Range

The maximum ambient operating temperature, listed as +85°C, is actually a function of the system use (i.e., specifically how many drivers within a package are used) and at what current levels they are operating. The maximum power which may be dissipated within the package is determined by:

$$P_{Dmax} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

where $R_{\theta JA}$ = package thermal resistance which is typically:

120°C/W for the SOIC (D) package,

T_{Jmax} = max. allowable junction temperature (150°C)

T_A = ambient air temperature near the IC package.

1) Differential Mode Power Dissipation

For the differential mode, the power dissipated within the package is calculated from:

$$P_D = [\,(V_{CC} - V_{OD}) \times I_O\,] \text{ (each driver)} + (V_{CC} \times I_B)$$

where: V_{CC} = the supply voltage

V_{OD} = is taken from Figure 6 for the known value of I_O

I_B = the internal bias current (Figure 7)

As indicated in the equation, the first term (in brackets) must be calculated and summed for each of the two drivers, while the last term is common to the entire package. Note that the term ($V_{CC} - V_{OD}$) is constant for a given value of I_O and does not vary with V_{CC}. For an application involving the following conditions:

T_A = +85°C, I_O = −60 mA (each driver), V_{CC} = 5.25 V, the suitability of the package types is calculated as follows.

The power dissipated is:

$$P_D = [\,3.0\text{ V} \times 60\text{ mA} \times 2\,] + (5.25\text{ V} \times 18\text{ mA})$$
$$P_D = 454\text{ mW}$$

The junction temperature calculates to:

$T_J = 85^\circ C + (0.454\text{ W} \times 120^\circ C/W) = 139^\circ C$ for the SOIC package.

Since the maximum allowable junction temperature is not exceeded in any of the above cases, either package can be used in this application.

2) Single−Ended Mode Power Dissipation

For the single−ended mode, the power dissipated within the package is calculated from:

$$P_D = (I_{B+} \times V_{CC}) + (I_{B-} \times V_{EE}) + [\,(I_O \times (V_{CC} - V_{OH})\,] \text{ (each driver)}$$

The above equation assumes I_O has the same magnitude for both output states, and makes use of the fact that the absolute value of the graphs of Figures 10 and 11 are nearly identical. I_B+ and I_B- are obtained from the right half of Figures 12 and 13, and ($V_{CC} - V_{OH}$) can be obtained from Figure 10. Note that the term ($V_{CC} - V_{OH}$) is constant for a given value of I_O and does not vary with V_{CC}. For an application involving the following conditions:

T_A = +85°C, I_O = −60 mA (each driver), V_{CC} = 5.25 V, V_{EE} = −5.25 V, the suitability of the package types is calculated as follows.

The power dissipated is:

$$P_D = (24\text{ mA} \times 5.25\text{ V}) + (-3.0\text{ mA} \times -5.25\text{ V}) + [\,60\text{ mA} \times 1.45\text{ V} \times 4.0\,]$$
$$P_D = 490\text{ mW}$$

The junction temperature calculates to:

$T_J = 85^\circ C + (0.490\text{ W} \times 120^\circ C/W) = 144^\circ C$ for the SOIC package.

Since the maximum allowable junction temperature is not exceeded in any of the above cases, either package can be used in this application.

SYSTEM EXAMPLES

(Pin numbers refer to SO−16 package only.)

Differential System

An example of a typical EIA−422−A system is shown in Figure 17. Although EIA−422−A does not specifically address multiple driver situations, the MC26LS30 can be used in this manner since the outputs can be put into a high impedance mode. It is, however, the system designer's responsibility to ensure the Enable pins are properly controlled so as to prevent two drivers on the same cable from being "on" at the same time.

The limit on the number of receivers and drivers which may be connected on one system is determined by the input current of each receiver, the maximum leakage current of each "off" driver, and the DC current through each terminating resistor. The sum of these currents must not exceed the capability of the "on" driver (≈60 mA). If the cable is of any significant length, with receivers at various points along its length, the common mode voltage may vary along its length, and this parameter must be considered when calculating the maximum driver current.

The cable requirements are defined not only by the AC characteristics and the data rate, but also by the DC resistance. The maximum resistance must be such that the minimum voltage across any receiver inputs is never less than 200 mV.

The ground terminals of each driver and receiver in Figure 17 must be connected together by a dedicated wire (or the shield) in the cable to provide a common reference. Chassis grounds or power line grounds should not be relied on for this common connection as they may generate significant common mode differences. Additionally, they usually do not provide a sufficiently low impedance at the frequencies of interest.

Single−Ended System

An example of a typical EIA−423−A system is shown in Figure 18. Multiple drivers on a single data line are not possible since the drivers cannot be put into a high impedance mode. Although each driver is shown connected to a single receiver, multiple receivers can be driven from a single driver as long as the total load current of the receivers and the terminating resistor does not exceed the capability of the driver (≈60 mA). If the cable is of any significant length, with receivers at various points along its length, the common mode voltage may vary along its length, and this parameter must be considered when calculating the maximum driver current.

The cable requirements are defined not only by the AC characteristics and the data rate, but also by the DC resistance. The maximum resistance must be such that the minimum voltage across any receiver inputs is never less than 200 mV.

The ground terminals of each driver and receiver in Figure 18 must be connected together by a dedicated wire (or the shield) in the cable so as to provide a common reference. Chassis grounds or power line grounds should not be relied on for this common connection as they may generate significant common mode differences. Additionally, they usually do not provide a sufficiently low impedance at the frequencies of interest.

Additional Modes of Operation

If compliance with EIA−422−A or EIA−423−A Standard is not required in a particular application, the MC26LS30 can be operated in two other modes.

1) The device may be operated in the differential mode (Pin 4 = 0) with V_{EE} connected to any voltage between ground and −5.25 V. Outputs in the low state will be referenced to V_{EE}, resulting in a differential output voltage greater than that shown in Figure 6. The Enable pins will operate the same as previously described.

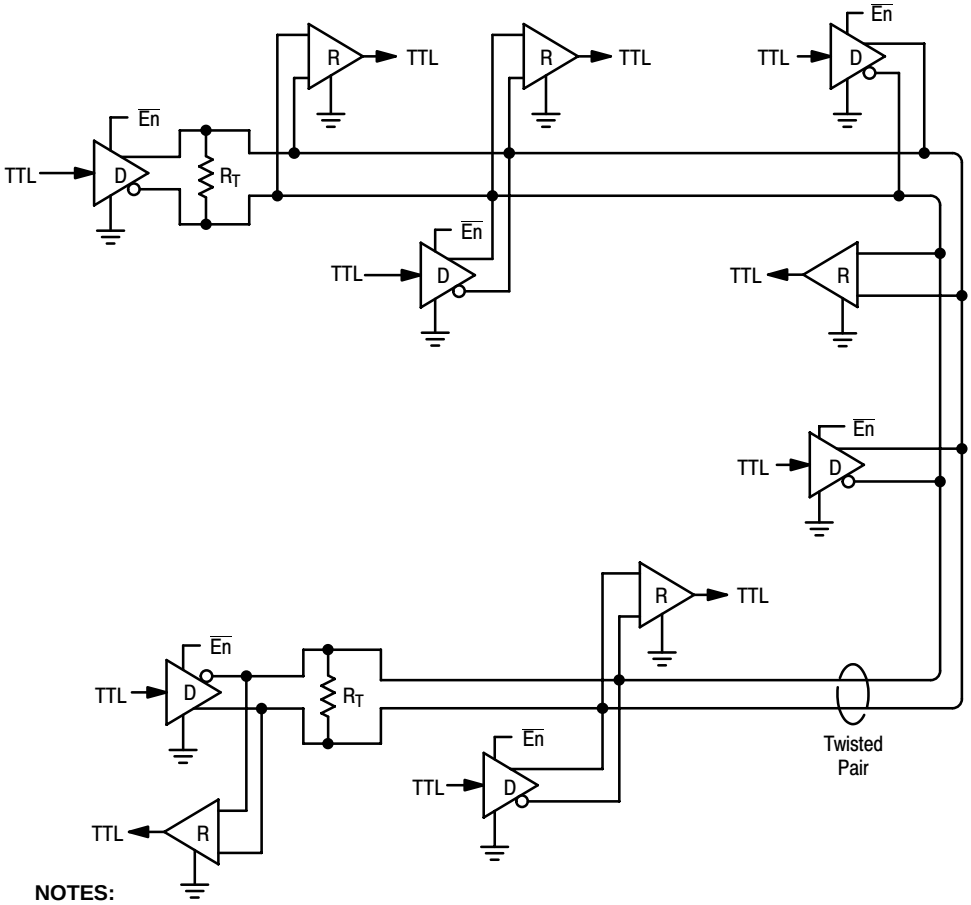
2) The device may be operated in the single−ended mode (Pin 4 = 1) with V_{EE} connected to any voltage between ground and −5.25 V. Outputs in the high state will be at a voltage as shown in Figure 10, while outputs in a low state will be referenced to V_{EE}.

Termination Resistors

Transmission line theory states that, in order to preserve the shape and integrity of a waveform traveling along a cable, the cable must be terminated in an impedance equal to its characteristic impedance. In a system such as that depicted in Figure 17, in which data can travel in both directions, both physical ends of the cable must be terminated. Stubs leading to each receiver and driver should be as short as possible.

In a system such as that depicted in Figure 18, in which data normally travels in one direction only, a terminator is theoretically required only at the receiving end of the cable. However, if the cable is in a location where noise spikes of several volts can be induced onto it, then a terminator (preferably a series resistor) should be placed at the driver end to prevent damage to the driver.

Leaving off the terminations will generally result in reflections which can have amplitudes of several volts above V_{CC} or several volts below ground or V_{EE}. These overshoots/undershoots can disrupt the driver and/or receiver, create false data, and in some cases, damage components on the bus.



NOTES:

1. Terminating resistors R_T should be located at the physical ends of the cable.
2. Stubs should be as short as possible.
3. Receivers = AM26LS32, MC3486, SN75173 or SN75175.
4. Circuit grounds must be connected together through a dedicated wire.

Figure 17. EIA−422−A Example

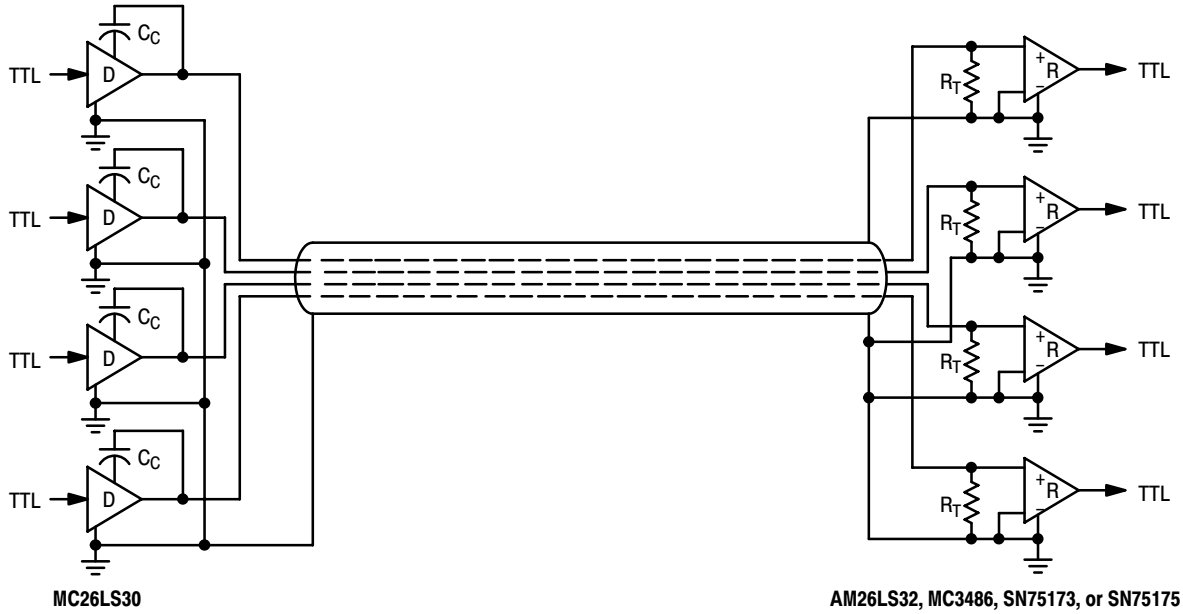
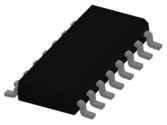


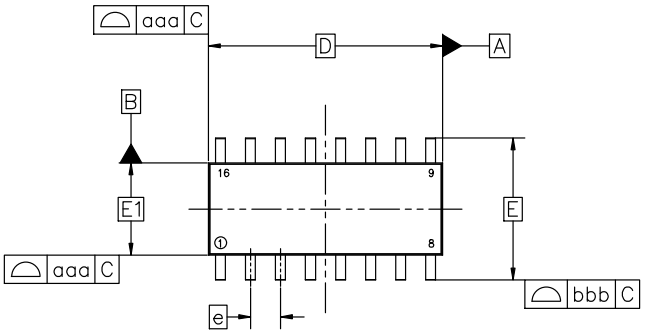
Figure 18. EIA−423−A Example



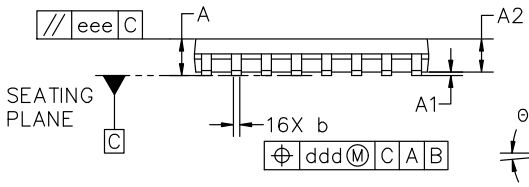
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

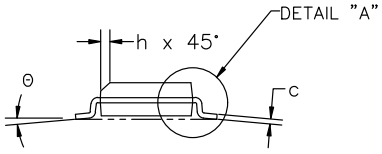
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



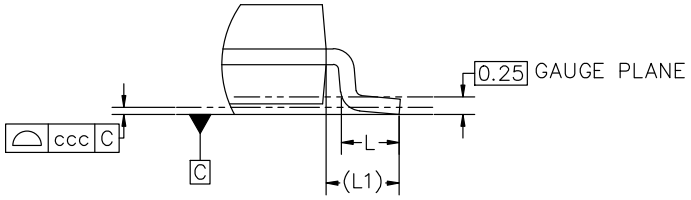
TOP VIEW



SIDE VIEW

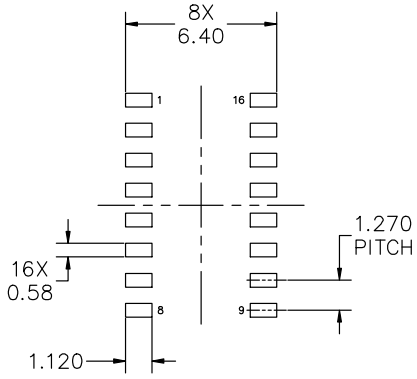


END VIEW



DETAIL "A"
Scale 3:1

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

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DESCRIPTION:	**SOIC−16 9.90X3.90X1.37 1.27P**		**PAGE 1 OF 2**

SOIC−16 9.90x3.90x1.37 1.27P
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ISSUE M

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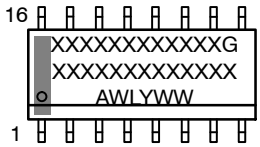
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN	
1.	COLLECTOR
2.	BASE
3.	EMITTER
4.	NO CONNECTION
5.	EMITTER
6.	BASE
7.	COLLECTOR
8.	COLLECTOR
9.	BASE
10.	EMITTER
11.	NO CONNECTION
12.	EMITTER
13.	BASE
14.	COLLECTOR
15.	EMITTER
16.	COLLECTOR

STYLE 2:

PIN	
1.	CATHODE
2.	ANODE
3.	NO CONNECTION
4.	CATHODE
5.	CATHODE
6.	NO CONNECTION
7.	ANODE
8.	CATHODE
9.	CATHODE
10.	ANODE
11.	NO CONNECTION
12.	CATHODE
13.	CATHODE
14.	NO CONNECTION
15.	ANODE
16.	CATHODE

STYLE 3:

PIN	
1.	COLLECTOR, DYE #1
2.	BASE, #1
3.	EMITTER, #1
4.	COLLECTOR, #1
5.	COLLECTOR, #2
6.	BASE, #2
7.	EMITTER, #2
8.	COLLECTOR, #2
9.	COLLECTOR, #3
10.	BASE, #3
11.	EMITTER, #3
12.	COLLECTOR, #3
13.	COLLECTOR, #4
14.	BASE, #4
15.	EMITTER, #4
16.	COLLECTOR, #4

STYLE 4:

PIN	
1.	COLLECTOR, DYE #1
2.	COLLECTOR, #1
3.	COLLECTOR, #2
4.	COLLECTOR, #2
5.	COLLECTOR, #3
6.	COLLECTOR, #3
7.	COLLECTOR, #4
8.	COLLECTOR, #4
9.	BASE, #4
10.	EMITTER, #4
11.	BASE, #3
12.	EMITTER, #3
13.	BASE, #2
14.	EMITTER, #2
15.	BASE, #1
16.	EMITTER, #1

STYLE 5:

PIN	
1.	DRAIN, DYE #1
2.	DRAIN, #1
3.	DRAIN, #2
4.	DRAIN, #2
5.	DRAIN, #3
6.	DRAIN, #3
7.	DRAIN, #4
8.	DRAIN, #4
9.	GATE, #4
10.	SOURCE, #4
11.	GATE, #3
12.	SOURCE, #3
13.	GATE, #2
14.	SOURCE, #2
15.	GATE, #1
16.	SOURCE, #1

STYLE 6:

PIN	
1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 7:

PIN	
1.	SOURCE N-CH
2.	COMMON DRAIN (OUTPUT)
3.	COMMON DRAIN (OUTPUT)
4.	GATE P-CH
5.	COMMON DRAIN (OUTPUT)
6.	COMMON DRAIN (OUTPUT)
7.	COMMON DRAIN (OUTPUT)
8.	SOURCE P-CH
9.	SOURCE P-CH
10.	COMMON DRAIN (OUTPUT)
11.	COMMON DRAIN (OUTPUT)
12.	COMMON DRAIN (OUTPUT)
13.	GATE N-CH
14.	COMMON DRAIN (OUTPUT)
15.	COMMON DRAIN (OUTPUT)
16.	SOURCE N-CH

ADDITIONAL INFORMATION

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