stablised

POWER GND
IN +5V
J1

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NMI

0V + CB2 CA1
CB1 CA2
J4

R6 220R

D1 1N5401
K

C2 10uF

D2 C1 10nF
POWER

'THREE CHIP PLUS'

GND

PB0
Port B

FE60

C6 100nF

D3

PA7
Port A

FE61

U4 6522

R2 5K6
R1 5K3
R3 3K3
R4 1K

PB7
GND

J2

J5

A15 ADDRESS BUS A0

C7 100nF

JP1
6502: short
65C02: open

CPU

JP2
6502: short
65C02: open

PA0

J3

R5 1K8

C8 100nF

U1 74LS14

J7 J6
R/W GND

U6

U7

2716

JP3
CLK OUT
CLK IN
GND

X1 ACO-1MHz

data

address

C4 100nF

U3 74LS08

UNILAB
Blackburn, England

C5 100nF

C3 100uF

SW1

RESET

C9 100nF U6 74LS138 C10 100nF U2 74LS32 U8 2114 C11 100nF U9 2114 C12 100nF

540.300

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2021-05-31 (ISS2): Power in legend corrected
2021-05-31 (ISS2): Added missing C5, R8 legends
2021-05-31 (ISS2): Corrected PHI2 / PHI2 clock routing

Sheet:
File: three chip plus.kicad_pcb

Title: UNILAB 3 CHIP PLUS CLONE

Size: USLetter   Date: 2021-05-31   Rev: ISS2
KiCad E.D.A. kicad (5.0.1-3-g963ef8bb5)   Id: 1/7