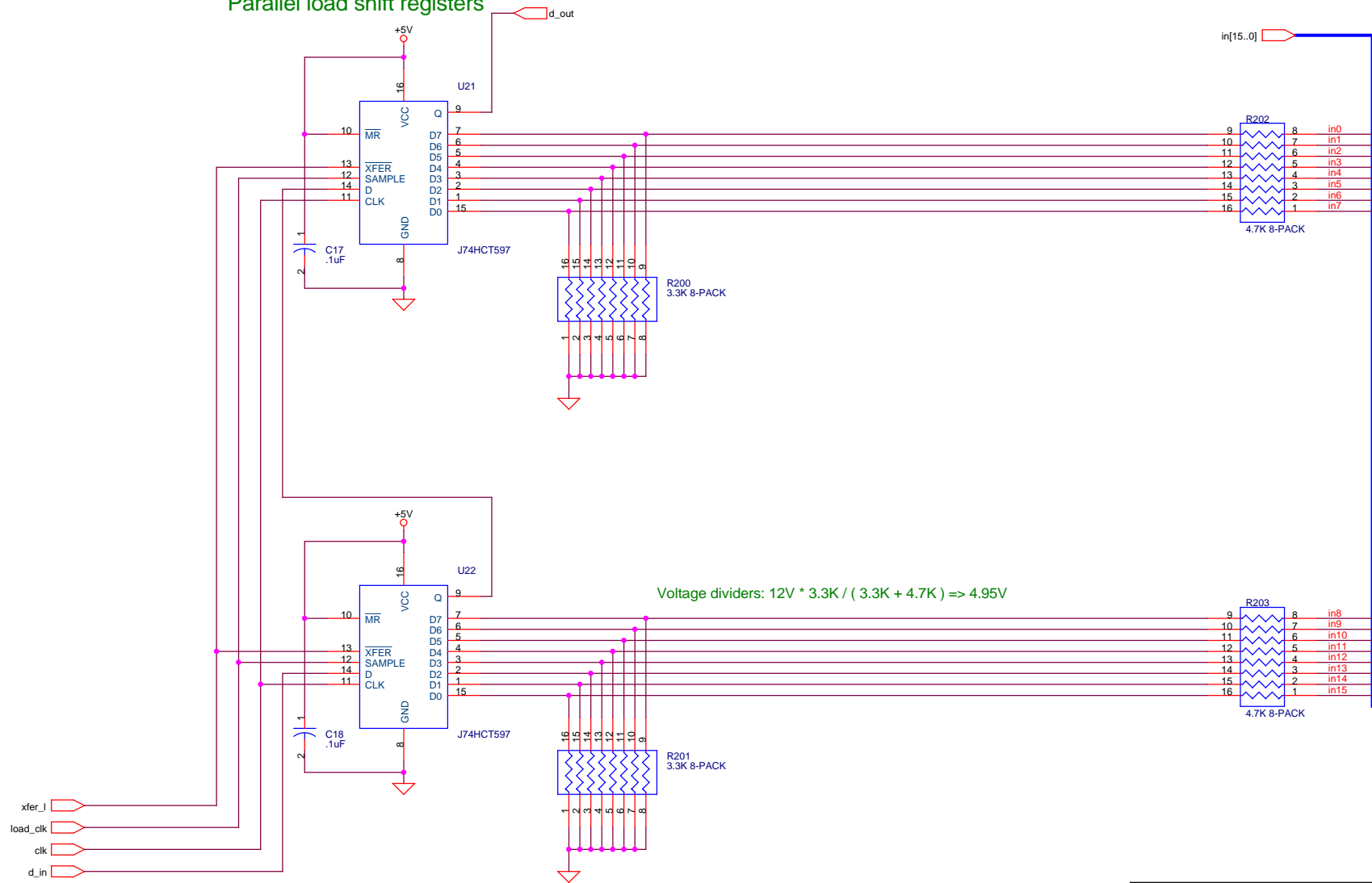
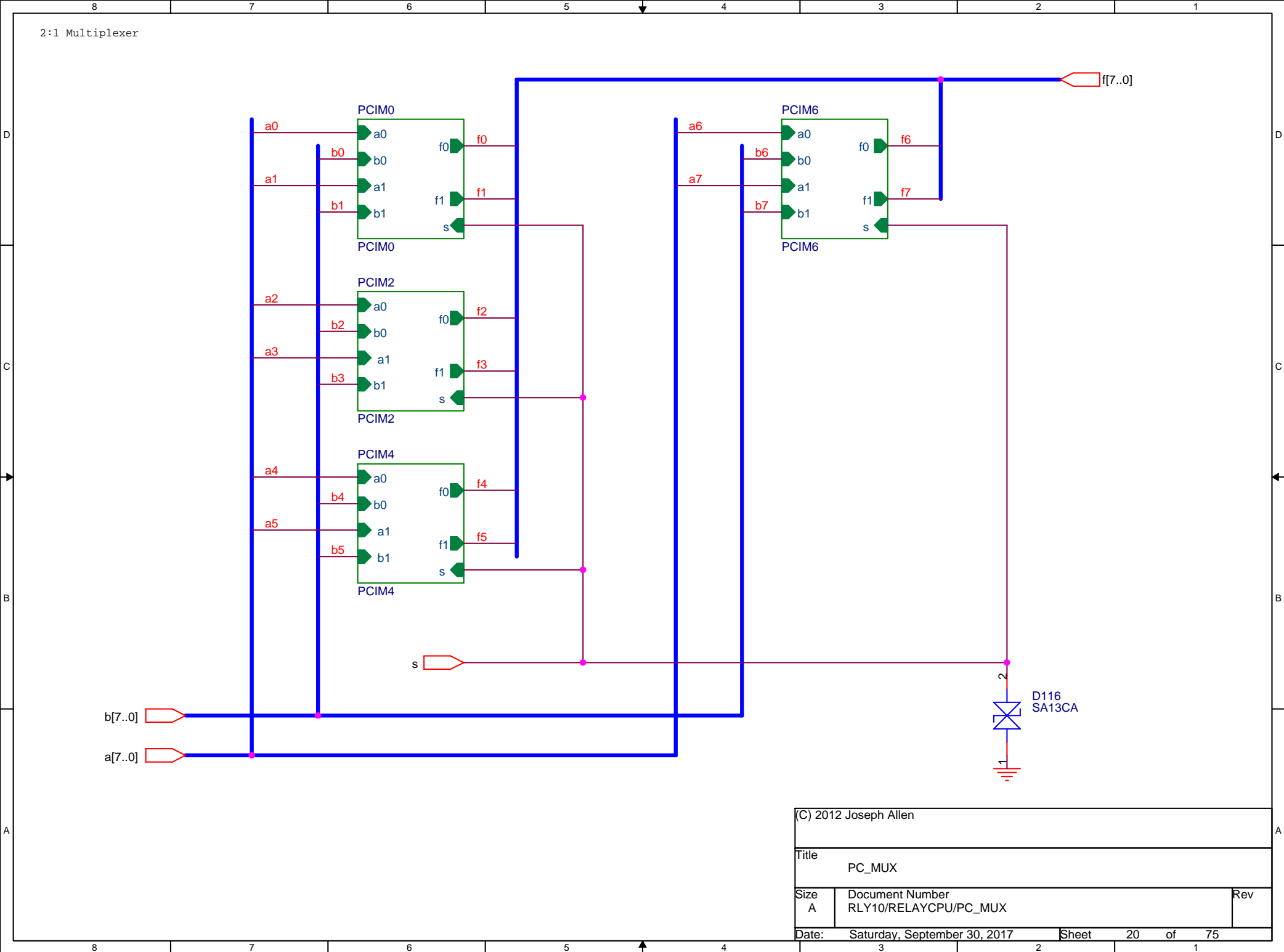
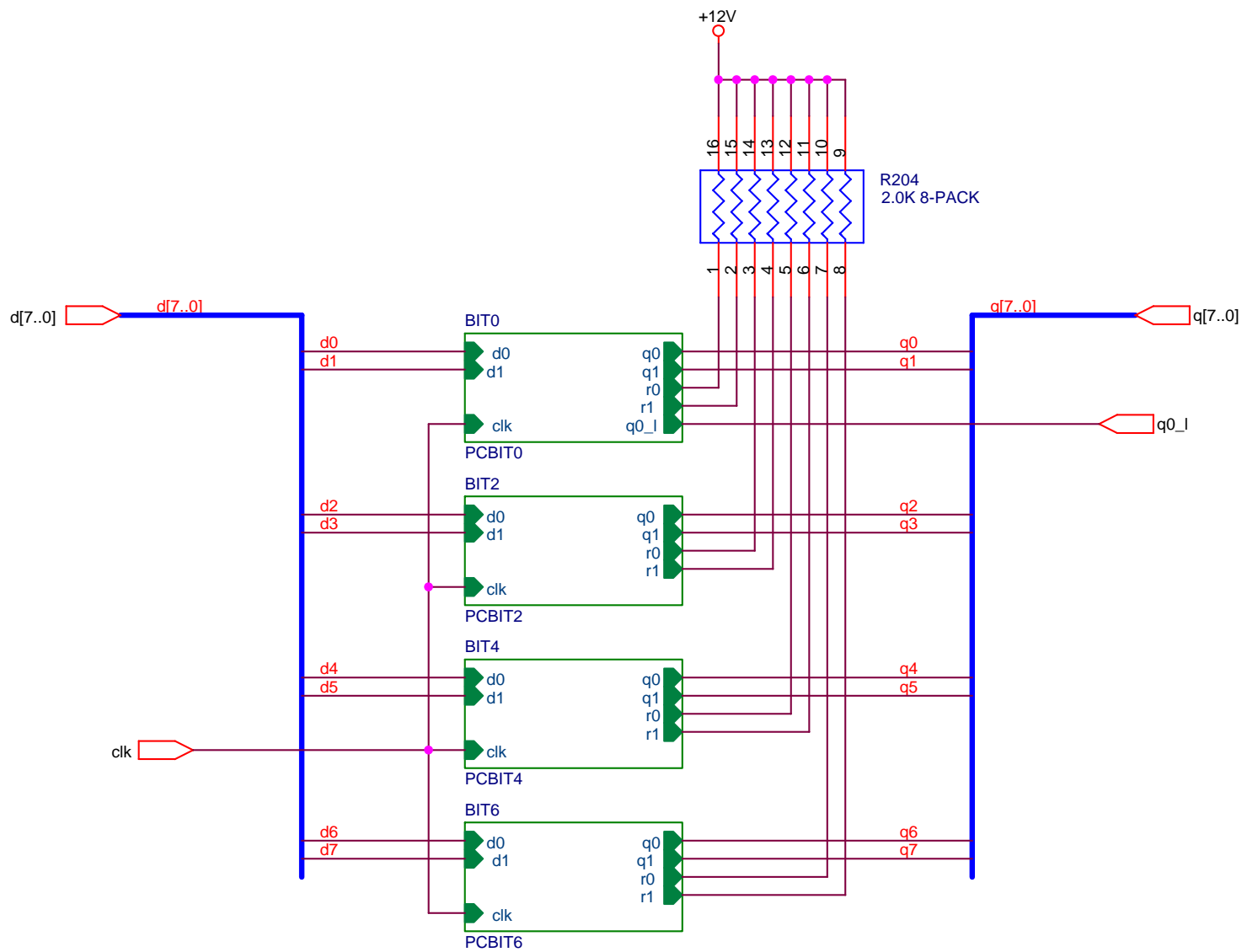


Parallel load shift registers



(C) 2012 Joseph Allen		
Title		
RELAYRCV		
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B	RLY10/RELAYRCV	
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(C) 2012 Joseph Allen

Title

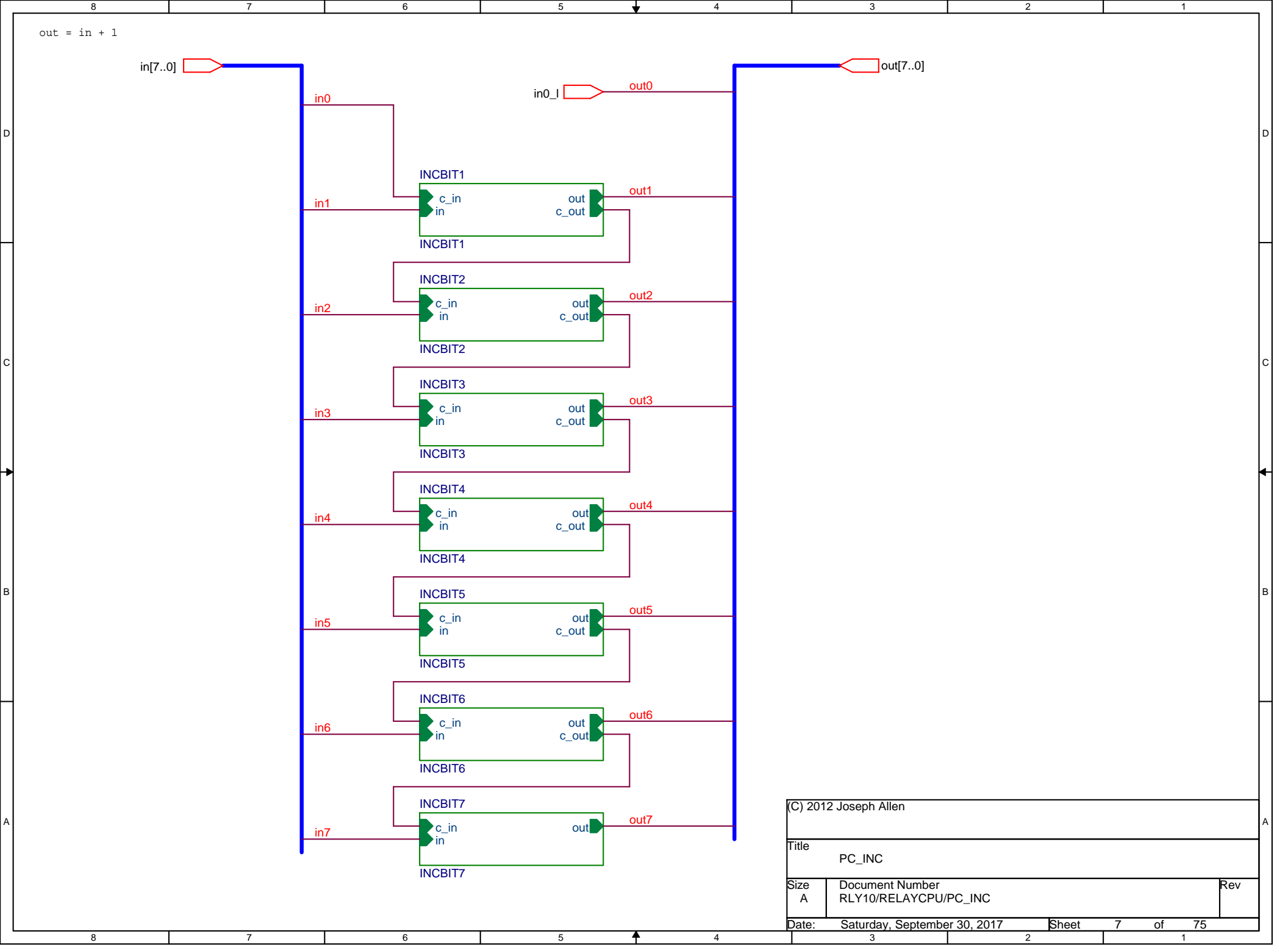
PC

Size
ADocument Number
RLY10/RELAYCPU/PC

Rev

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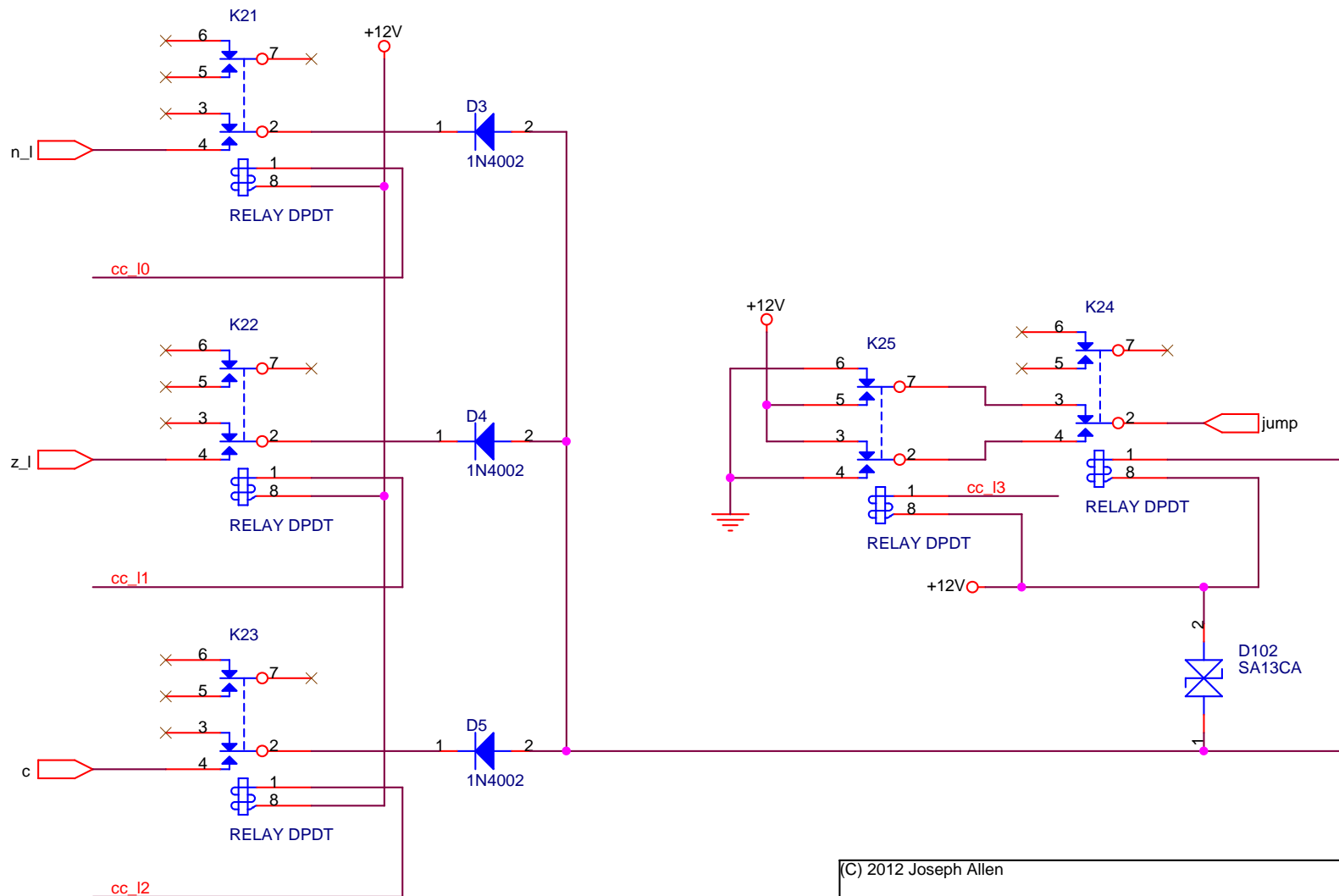


(C) 2012 Joseph Allen			
Title			
PC_INC			
Size	Document Number		Rev
A	RLY10/RELAYCPU/PC_INC		
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Condition logic:

$\text{jump} = (\text{cc}[0] \& \text{n} \mid \text{cc}[1] \& \text{z} \mid \text{cc}[2] \& \sim \text{c}) \wedge \text{cc}[3]$

cc_l[3..0]  cc_l[3..0]



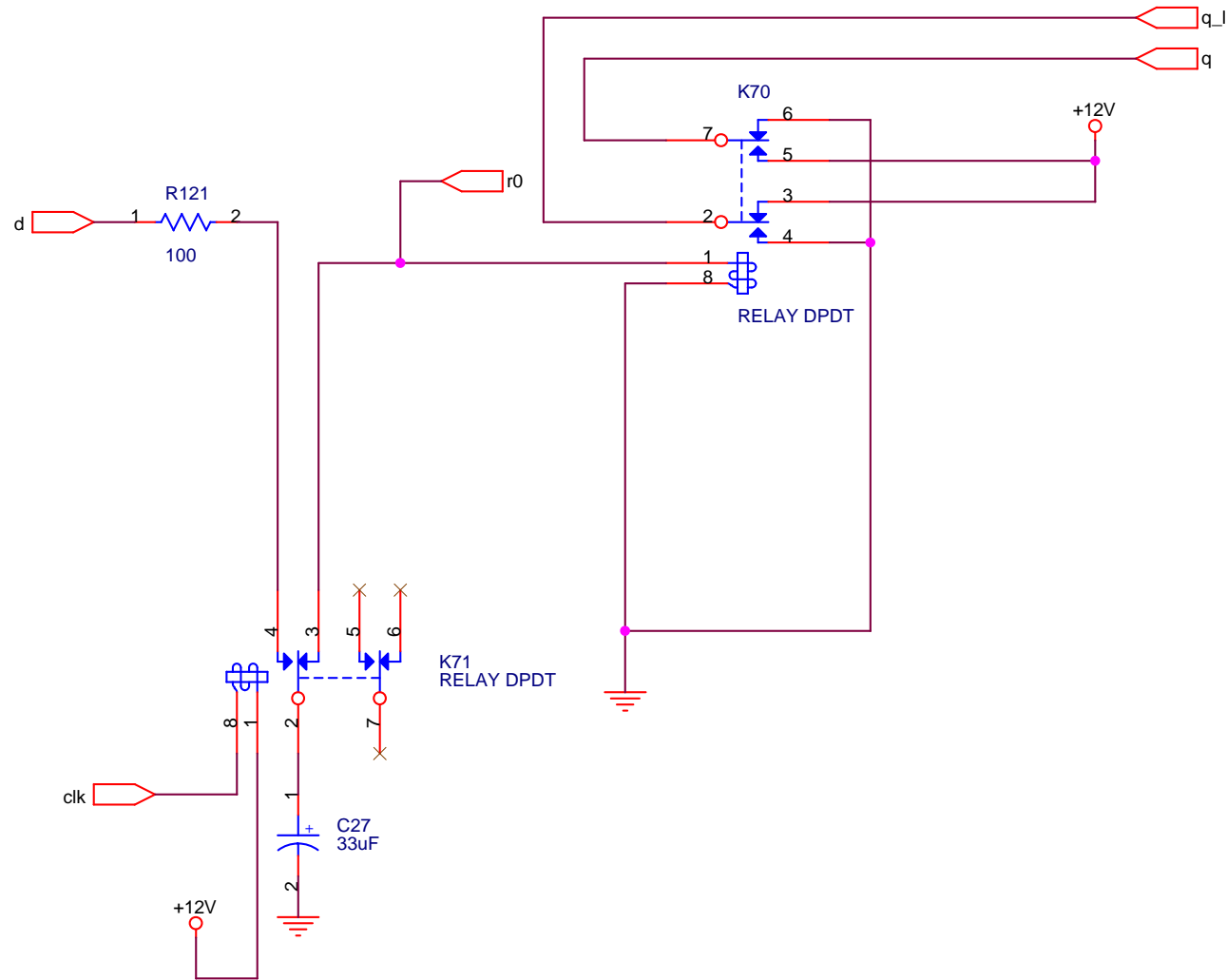
(C) 2012 Joseph Allen

Title
CC

Size A Document Number
RLY10/RELAYCPU/CC

Rev

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(C) 2012 Joseph Allen

Title

C_FLAG

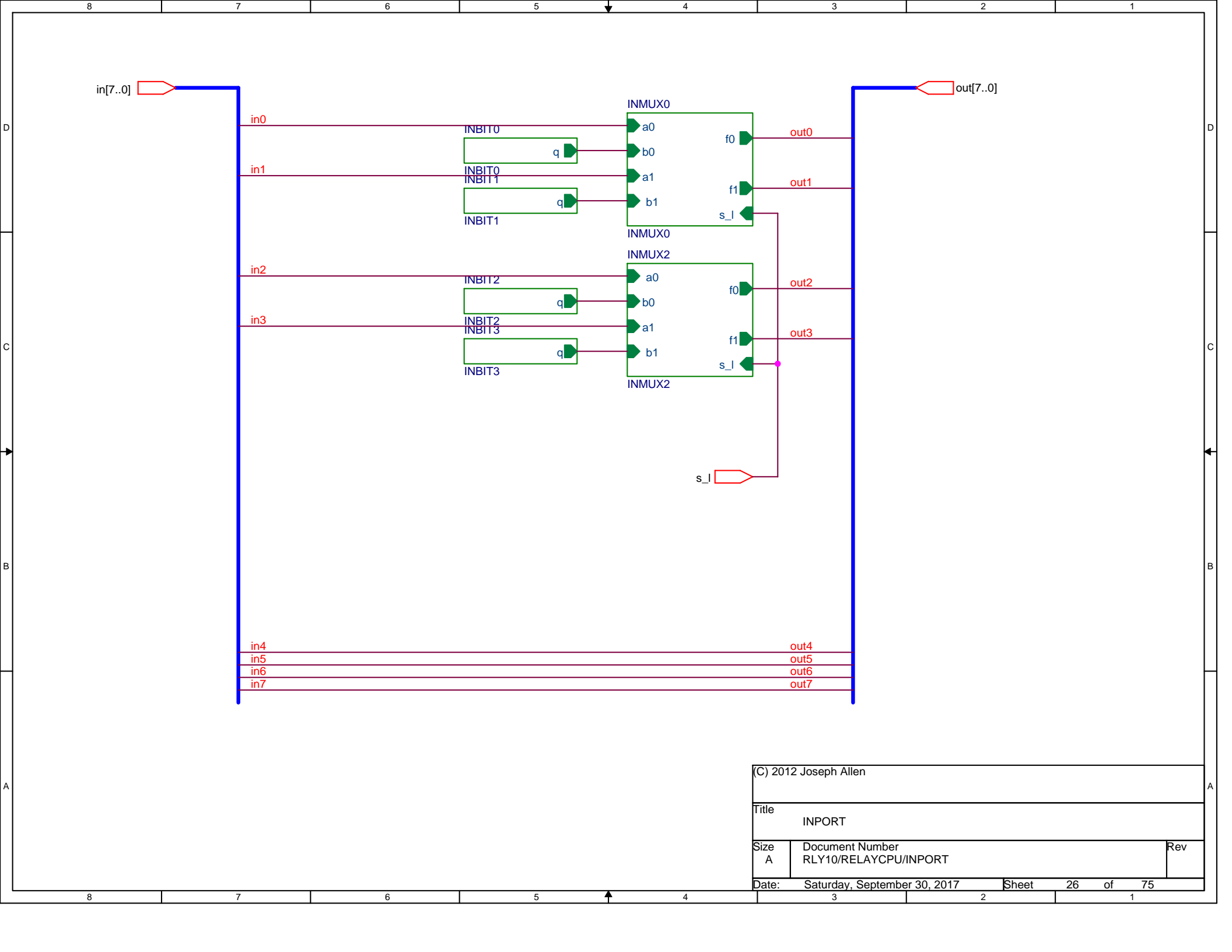
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Document Number
RLY10/RELAYCPU/C_FLAG

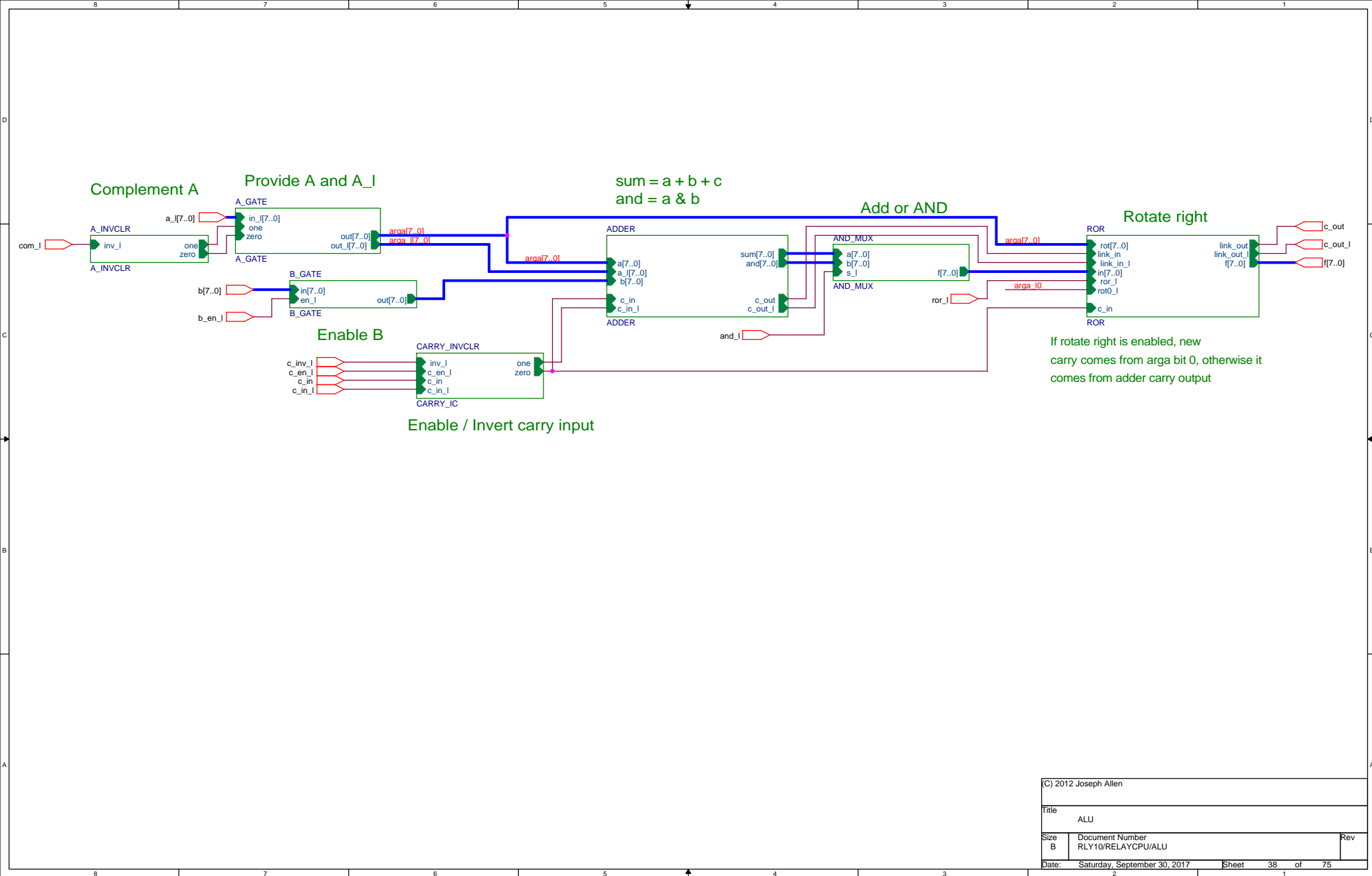
Rev

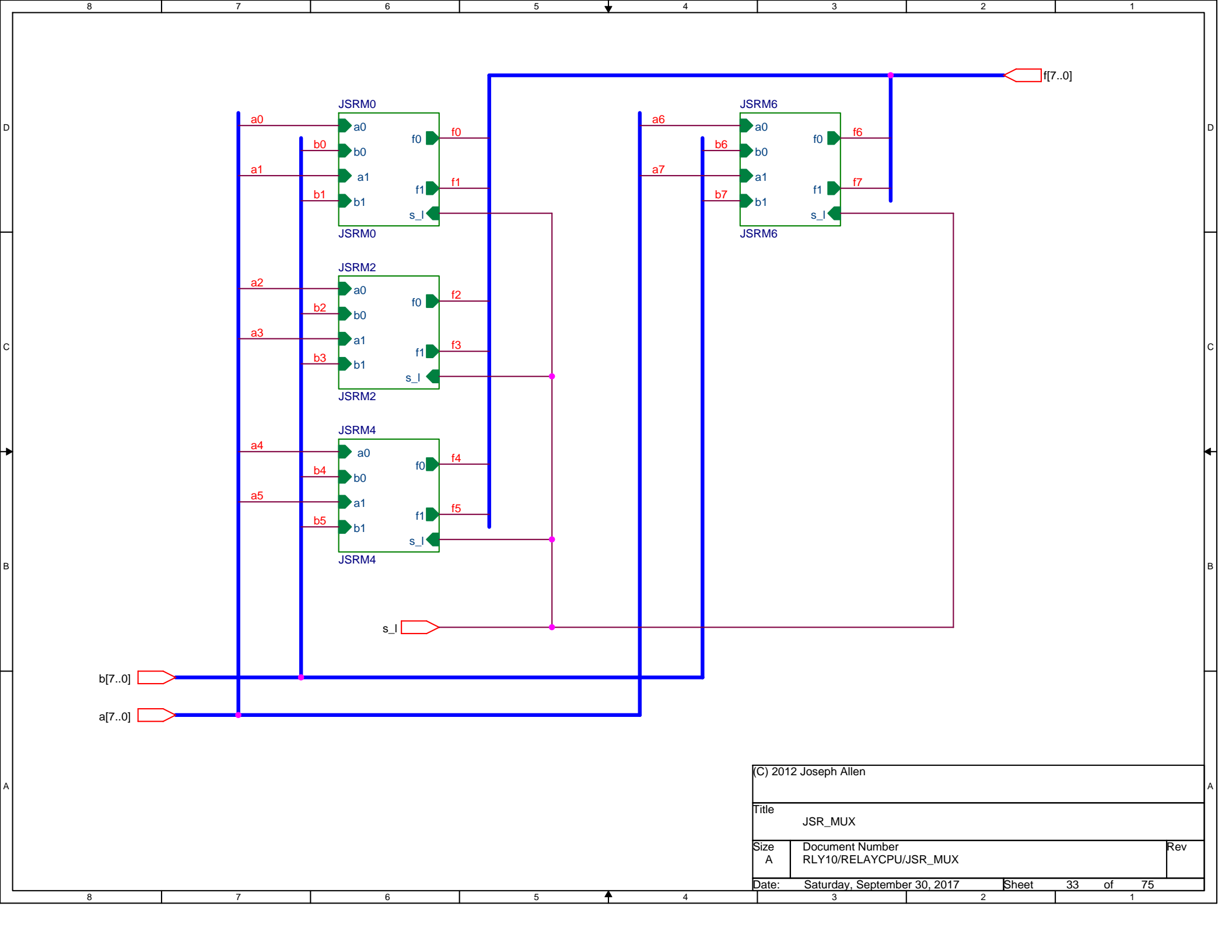
Date: Saturday, September 30, 2017

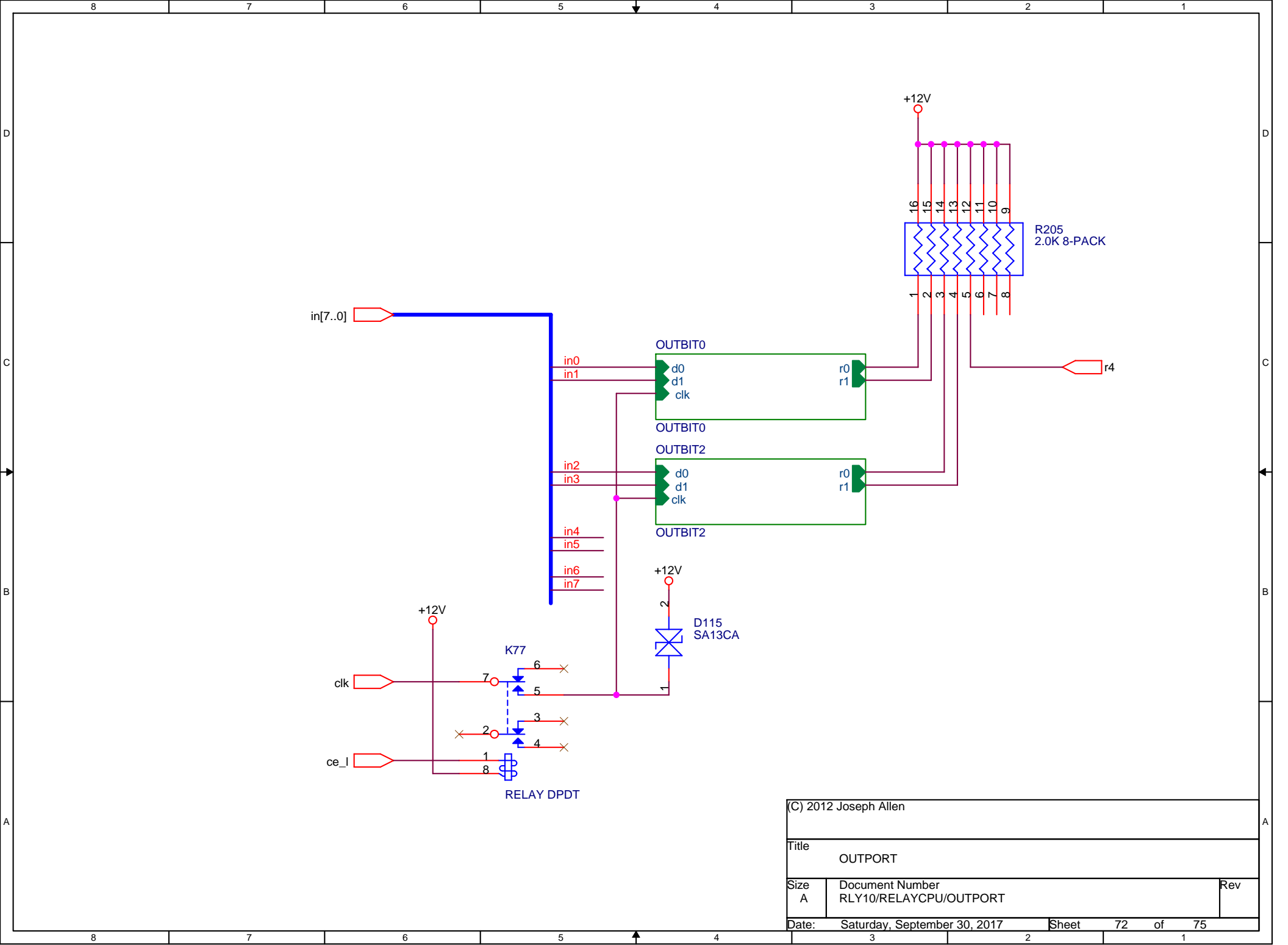
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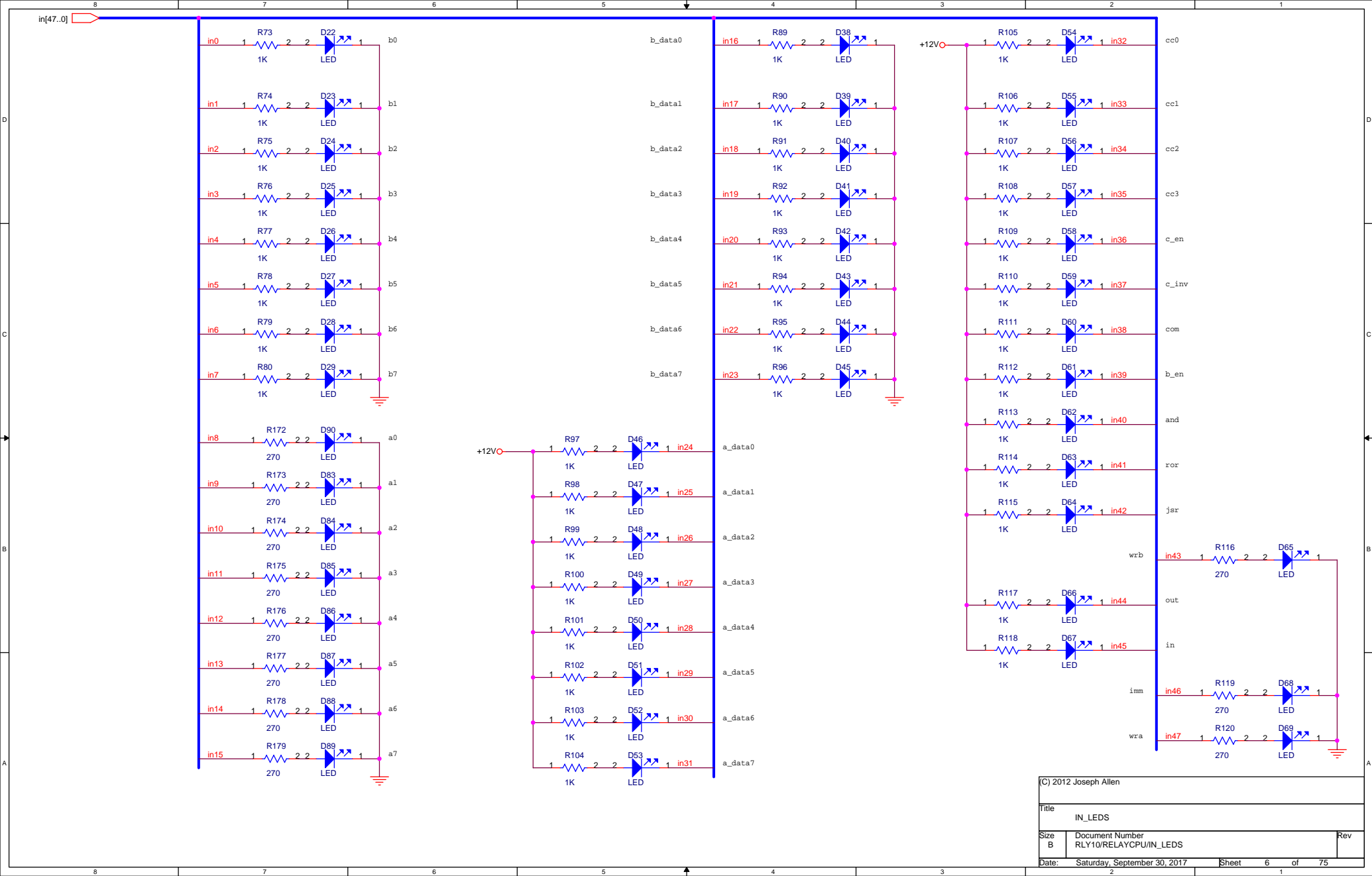
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Title			
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Size	Document Number		Rev
A	RLY10/RELAYCPU/INPORT		
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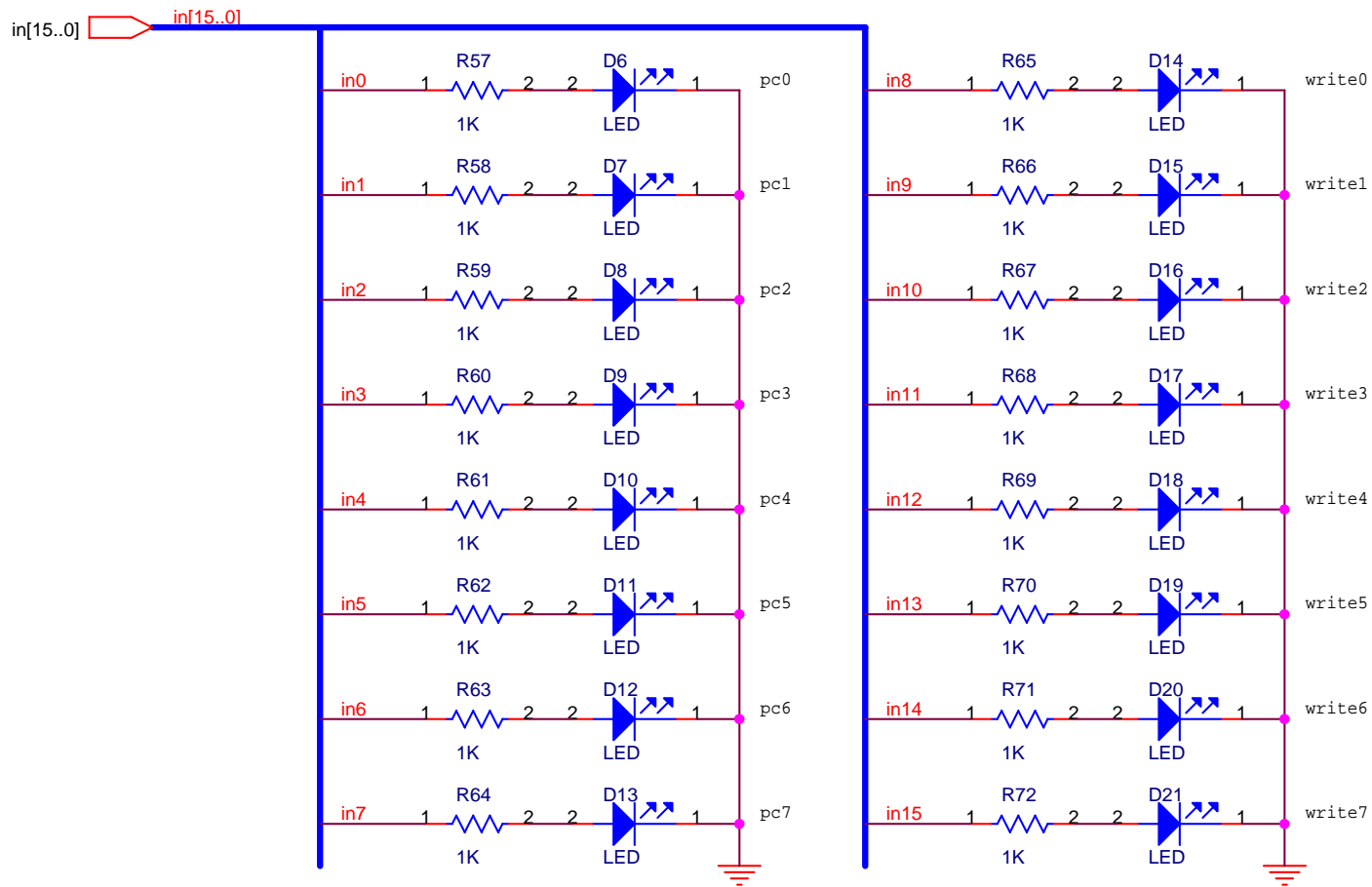






(C) 2012 Joseph Allen		
Title		
OUTPORT		
Size	Document Number	Rev
A	RLY10/RELAYCPU/OUTPORT	
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(C) 2012 Joseph Allen

Title

OUT_LEDS

Size
A

Document Number
RLY10/RELAYCPU/OUT_LEDS

Rev

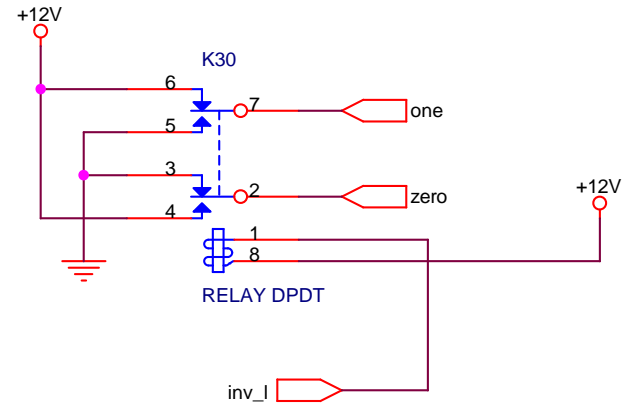
Date: Saturday, September 30, 2017

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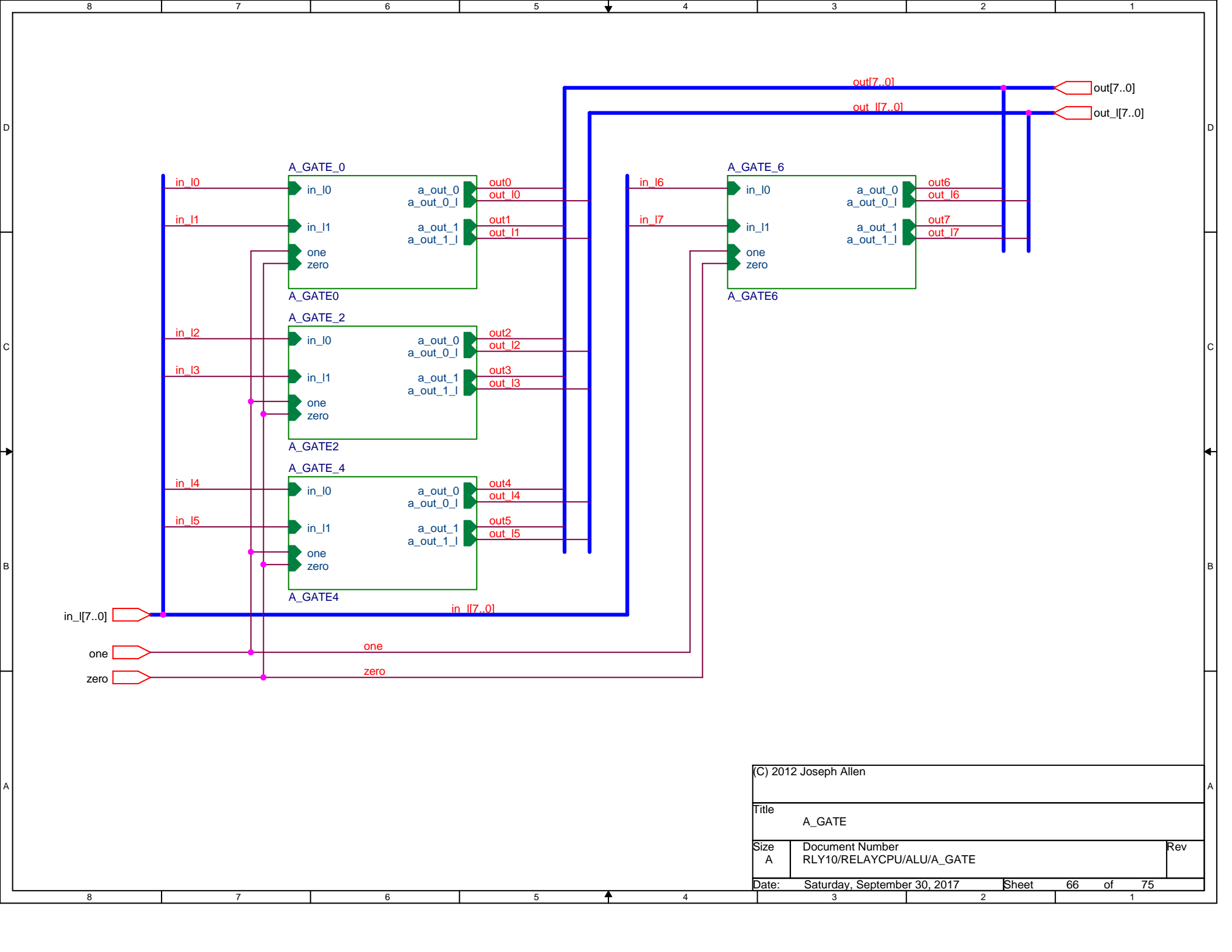

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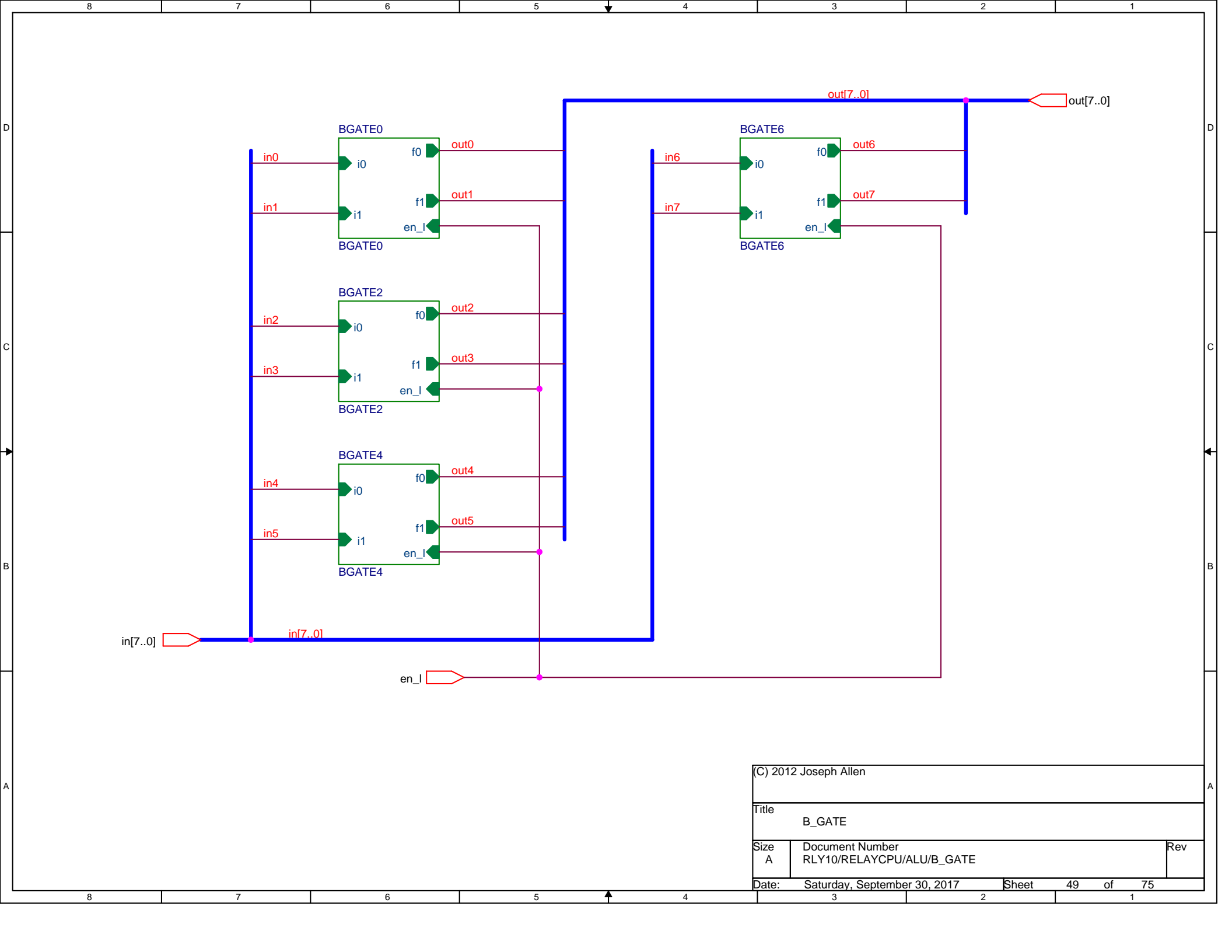
sim
assign one = (inv === 1'bx) ? 1'bx :
              (inv === 1'b1) ? 1'b0 :
              1'b1;
assign zero = (inv === 1'bx) ? 1'bx :
              (inv === 1'b1) ? 1'b1 :
              1'b0;

```



(C) 2012 Joseph Allen			
Title			
A_INVCLR			
Size	Document Number		Rev
A	RLY10/RELAYCPU/ALU/A_INVCLR		
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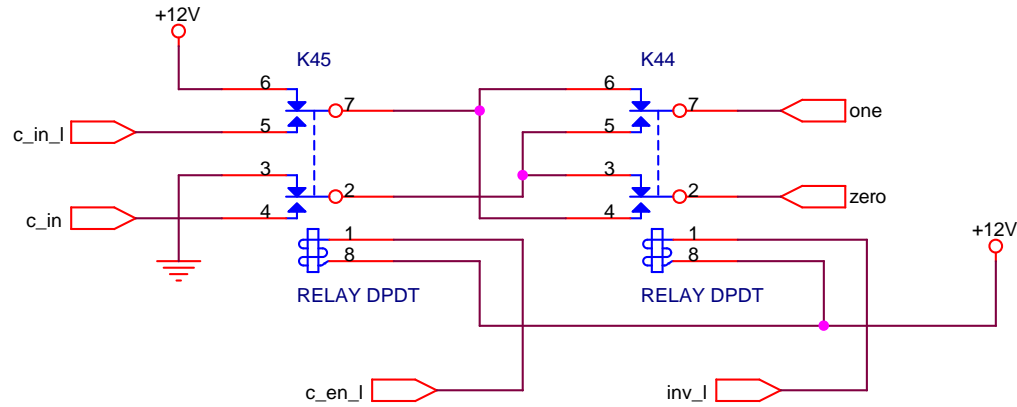




```

sim
assign one = (inv === 1'bx) ? 1'bx :
              (inv === 1'b1) ? 1'b0 :
              1'b1;
assign zero = (inv === 1'bx) ? 1'bx :
              (inv === 1'b1) ? 1'b1 :
              1'b0;

```



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Title

CARRY_INVCLR

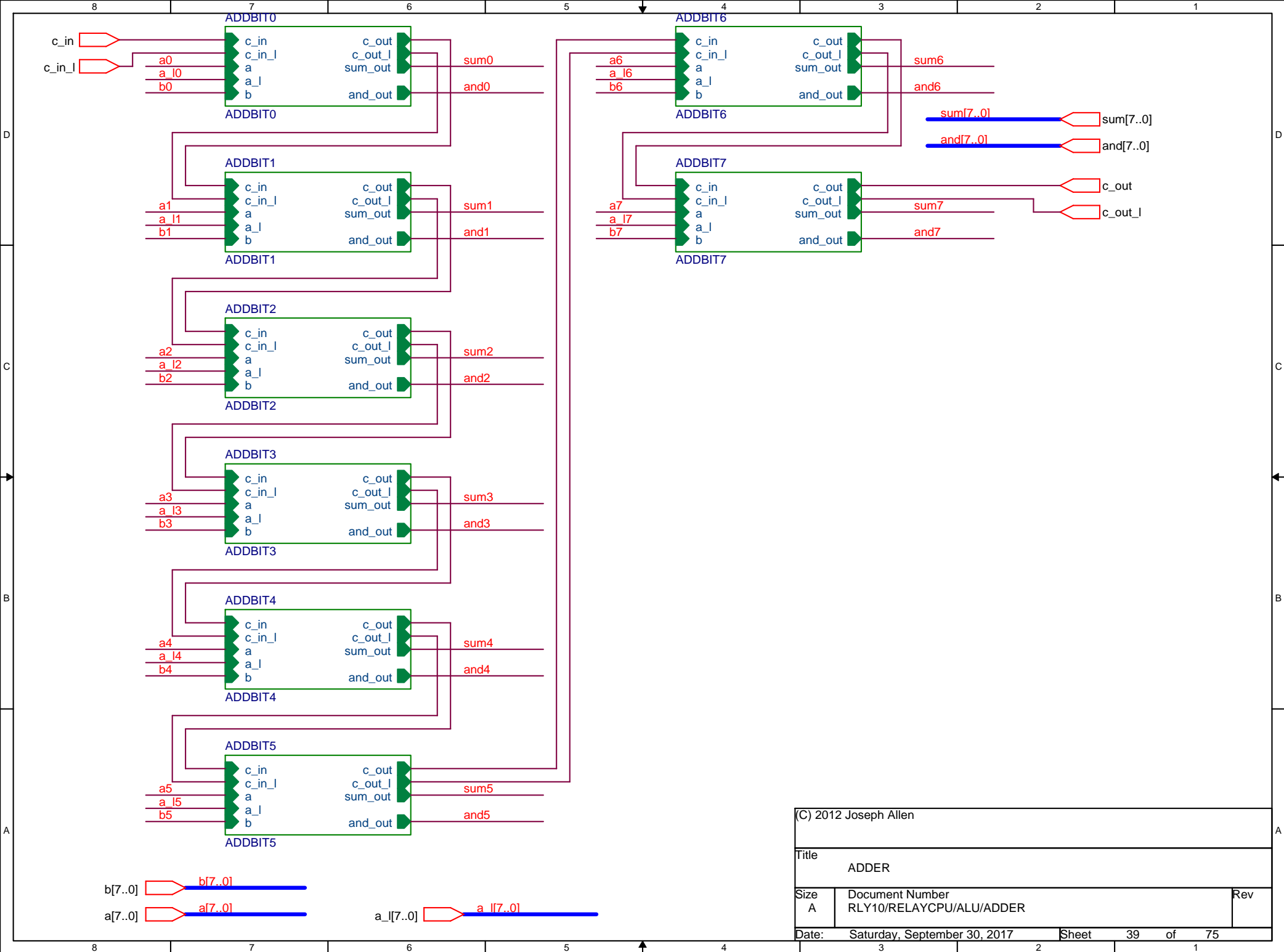
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Document Number
RLY10/RELAYCPU/ALU/CARRY_INVCLR

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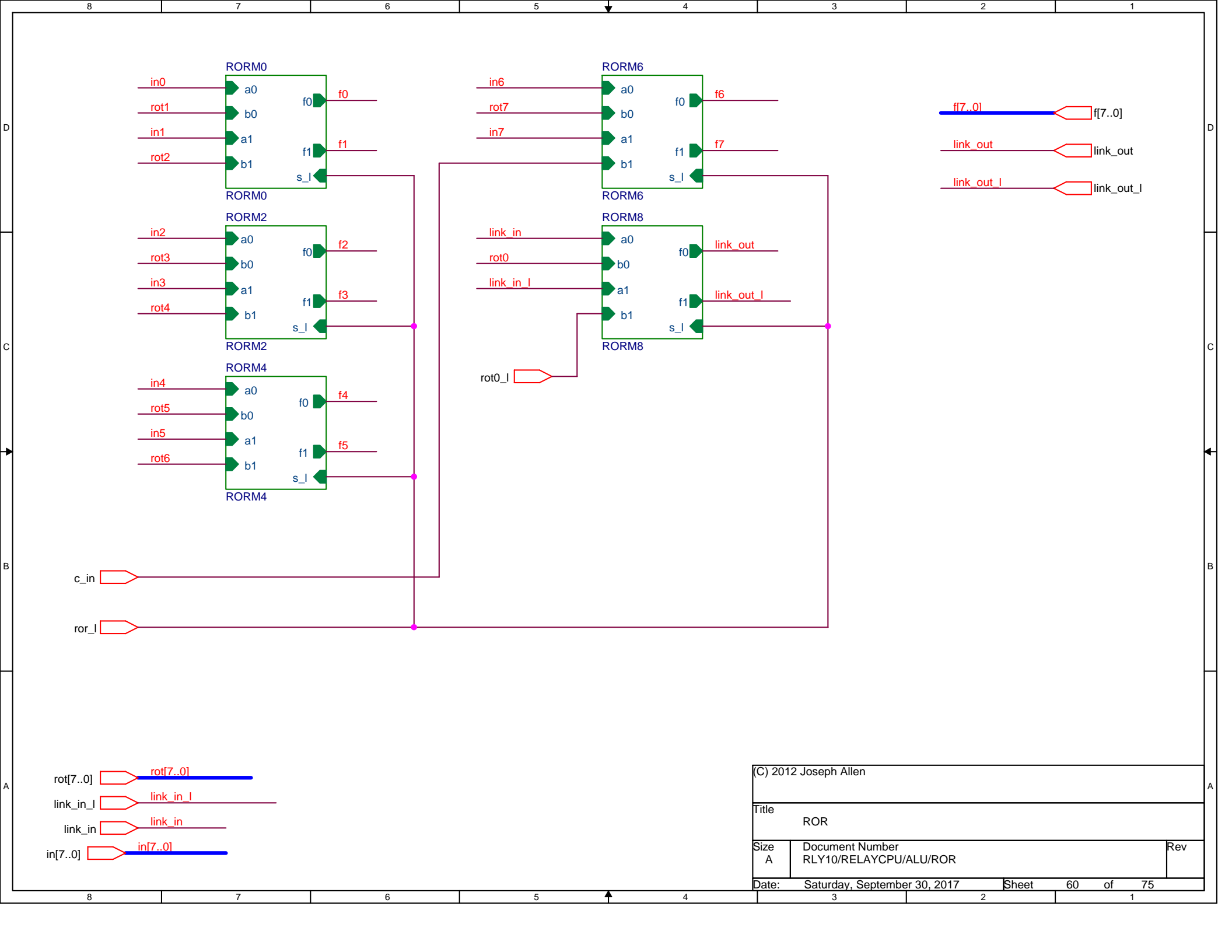
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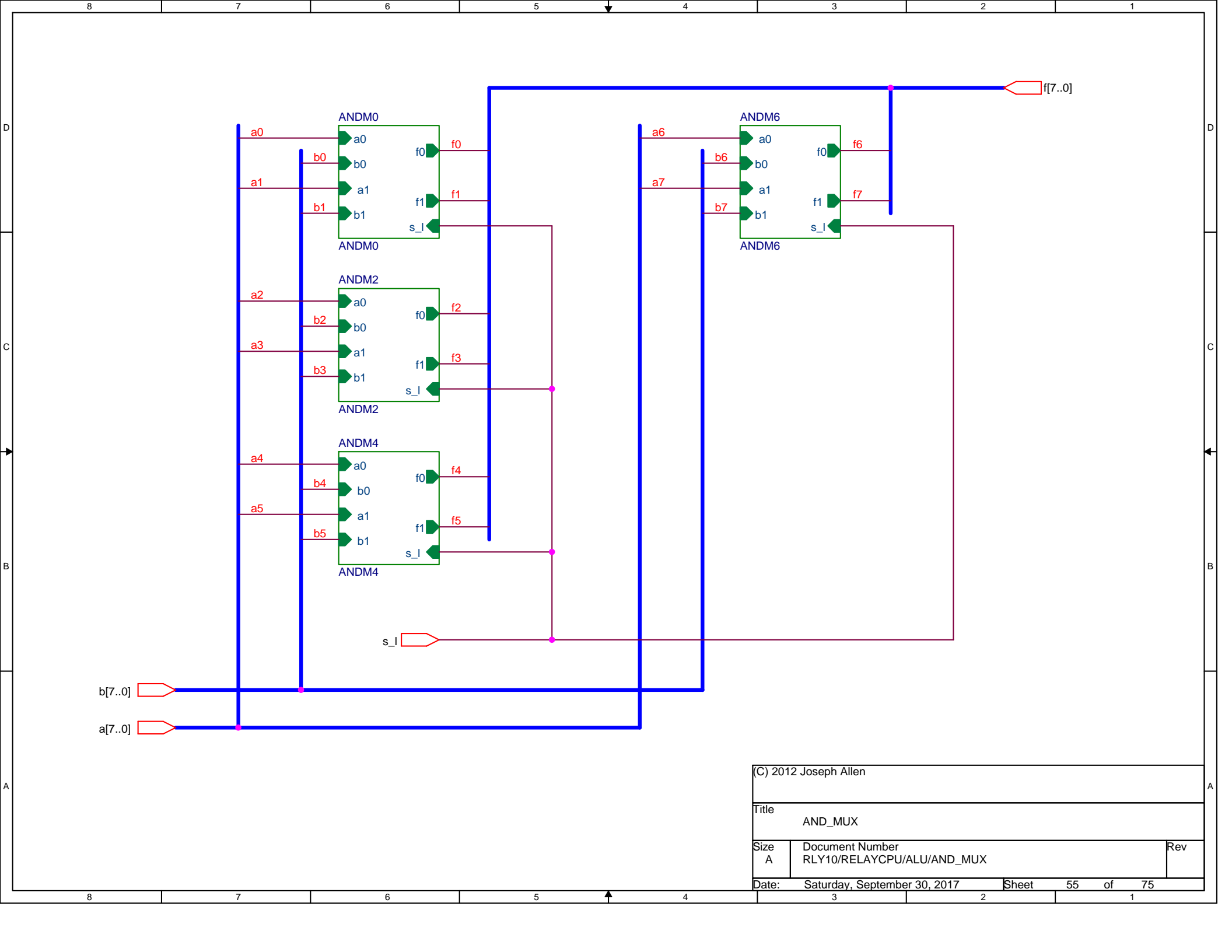
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Size A Document Number
RLY10/RELAYCPU/ALU/ADDER

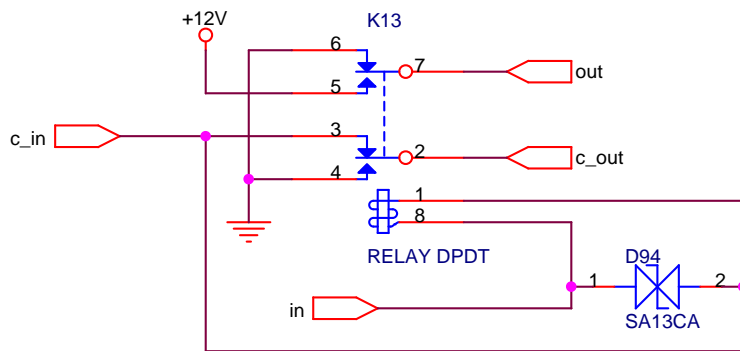
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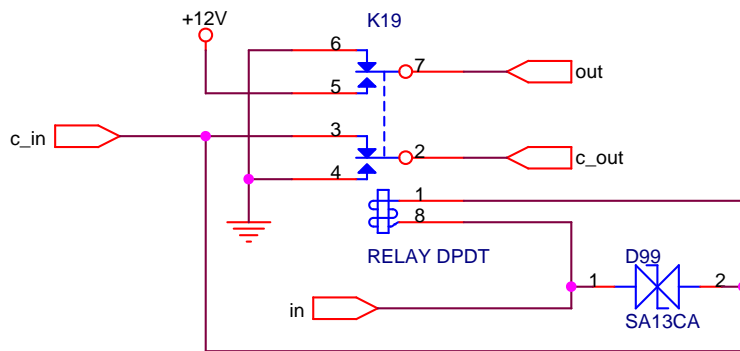




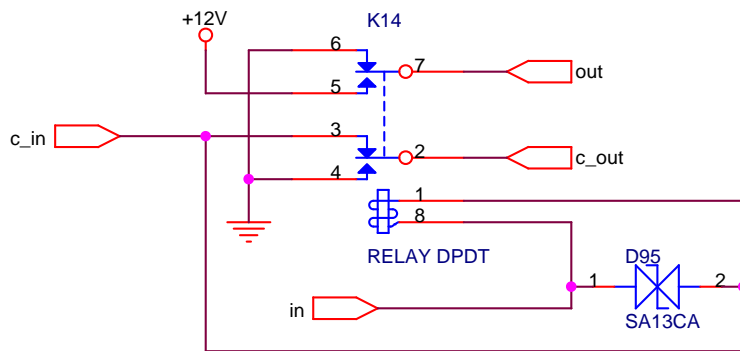
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Size	Document Number		Rev
A	RLY10/RELAYCPU/ALU/AND_MUX		
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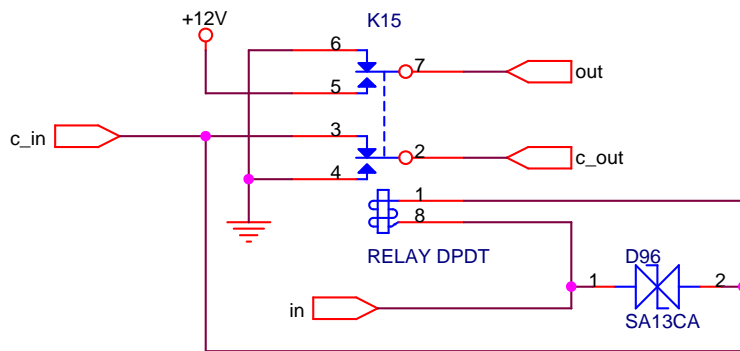
(C) 2012 Joseph Allen			
Title			
INCBIT1			
Size	Document Number		Rev
A	RLY10/RELAYCPU/PC_INC/INCBIT1		
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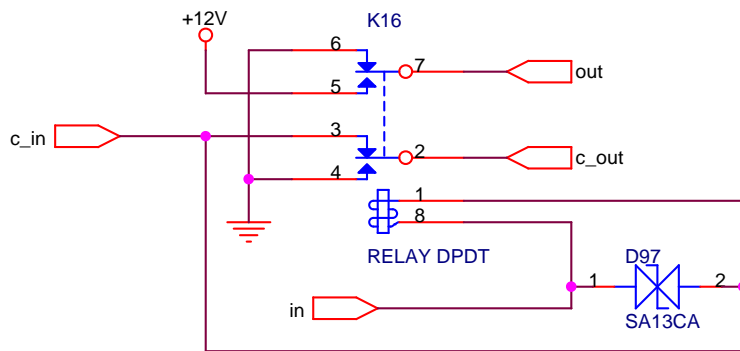
(C) 2012 Joseph Allen			
Title			
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Size	Document Number		Rev
A	RLY10/RELAYCPU/PC_INC/INCBIT2		
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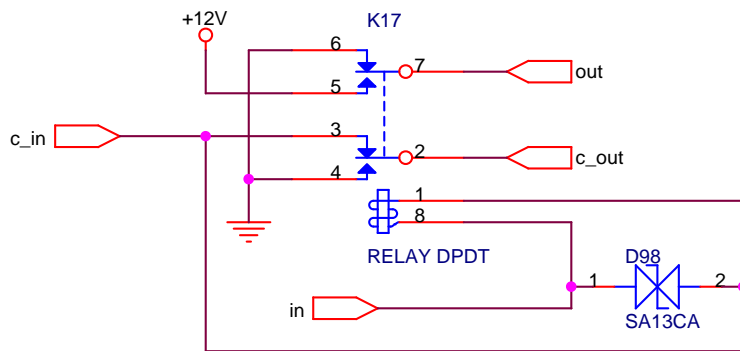
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Size	Document Number		Rev
A	RLY10/RELAYCPU/PC_INC/INCBIT3		
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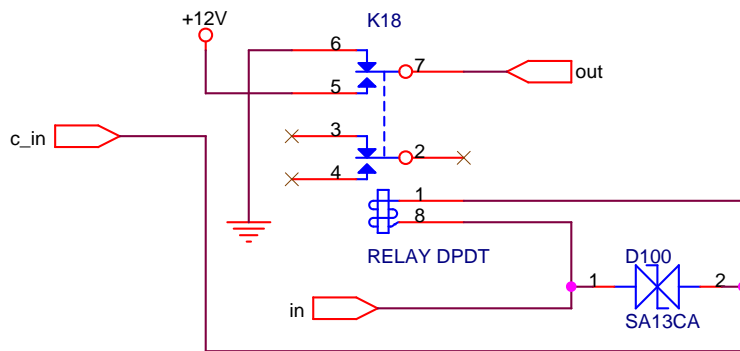
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Size	Document Number		Rev
A	RLY10/RELAYCPU/PC_INC/INCBIT4		
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(C) 2012 Joseph Allen			
Title			
INCBIT5			
Size	Document Number		Rev
A	RLY10/RELAYCPU/PC_INC/INCBIT5		
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(C) 2012 Joseph Allen			
Title			
INCBIT6			
Size	Document Number		Rev
A	RLY10/RELAYCPU/PC_INC/INCBIT6		
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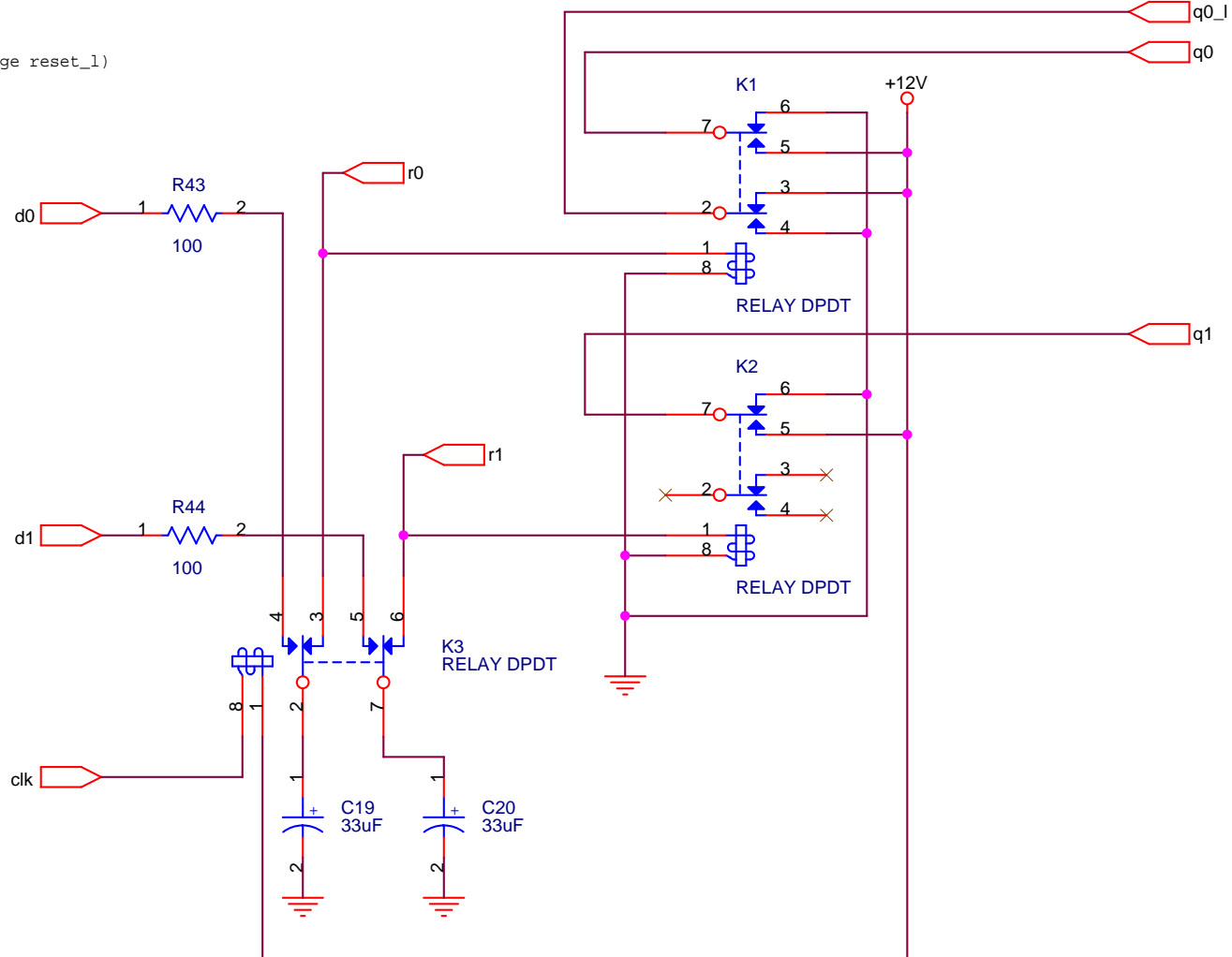


(C) 2012 Joseph Allen			
Title			
INCBIT7			
Size	Document Number		Rev
A	RLY10/RELAYCPU/PC_INC/INCBIT7		
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```

sim
reg x0;
assign q0 = x0;
always @(posedge clk or negedge reset_l)
  if (!reset_l)
    x0 <= 0;
  else
    x0 <= d0;
reg x1;
assign q1 = x1;
always @(posedge clk or negedge reset_l)
  if (!reset_l)
    x1 <= 0;
  else
    x1 <= d1;

```



(C) 2012 Joseph Allen

Title

BIT0

Size
A

Document Number
RLY10/RELAYCPU/PC/BIT0

Rev

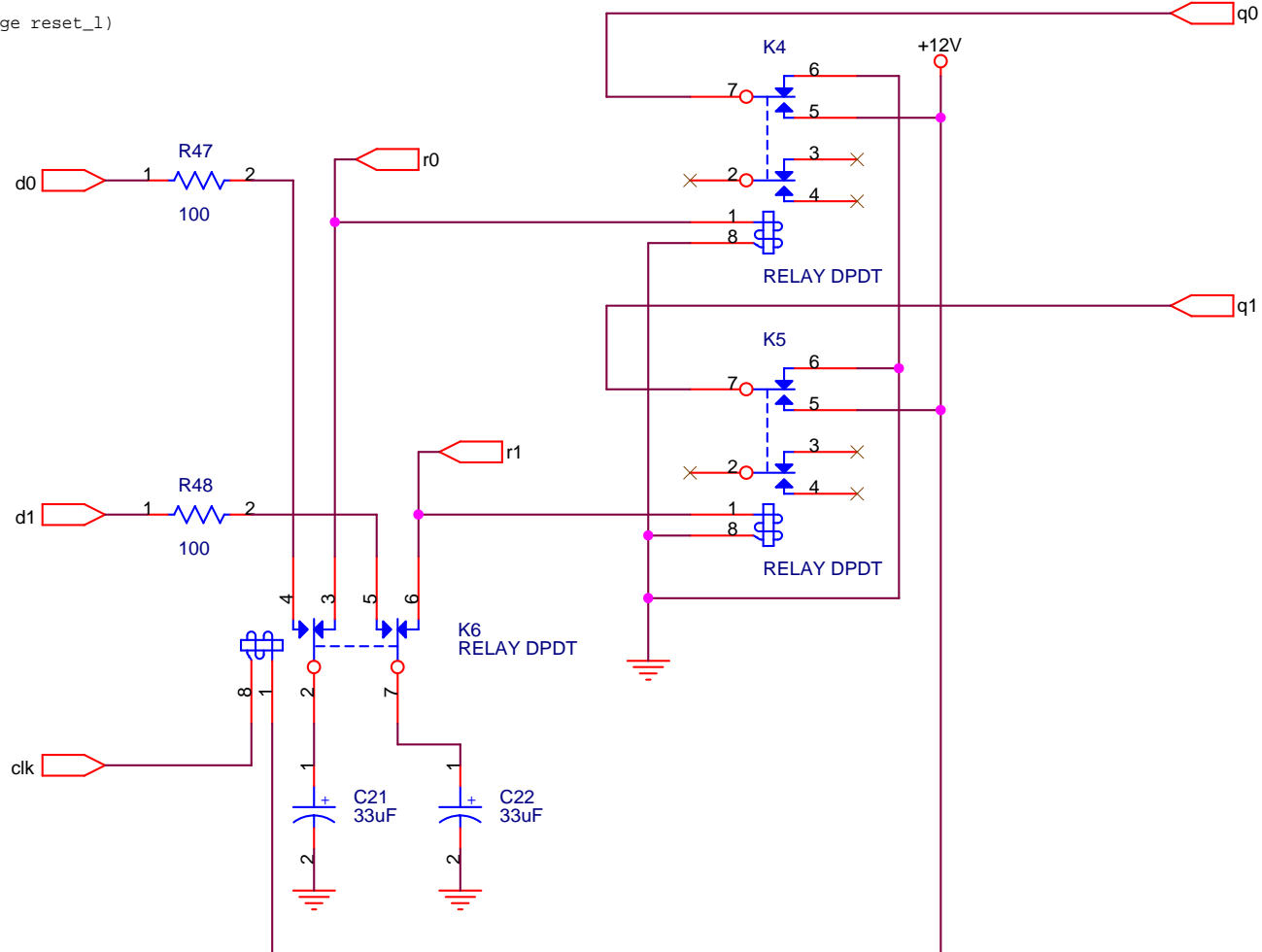
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```

sim
reg x0;
assign q0 = x0;
always @(posedge clk or negedge reset_1)
  if (!reset_1)
    x0 <= 0;
  else
    x0 <= d0;
reg x1;
assign q1 = x1;
always @(posedge clk or negedge reset_1)
  if (!reset_1)
    x1 <= 0;
  else
    x1 <= d1;

```



(C) 2012 Joseph Allen

Title

BIT2

Size
A

Document Number
RLY10/RELAYCPU/PC/BIT2

Rev

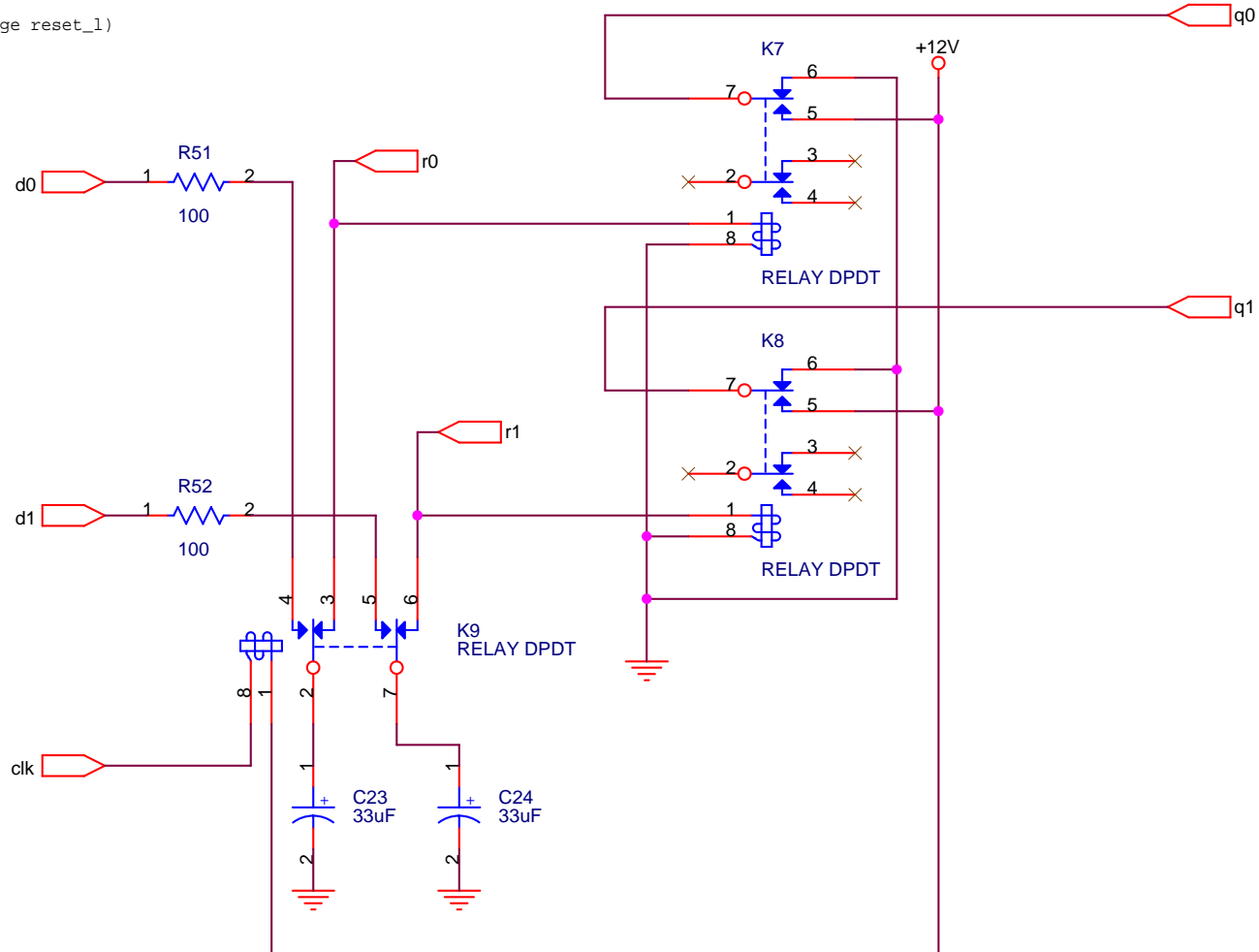
Date: Saturday, September 30, 2017

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```

sim
reg x0;
assign q0 = x0;
always @(posedge clk or negedge reset_1)
  if (!reset_1)
    x0 <= 0;
  else
    x0 <= d0;
reg x1;
assign q1 = x1;
always @(posedge clk or negedge reset_1)
  if (!reset_1)
    x1 <= 0;
  else
    x1 <= d1;

```



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Title

BIT4

Size
A

Document Number
RLY10/RELAYCPU/PC/BIT4

Rev

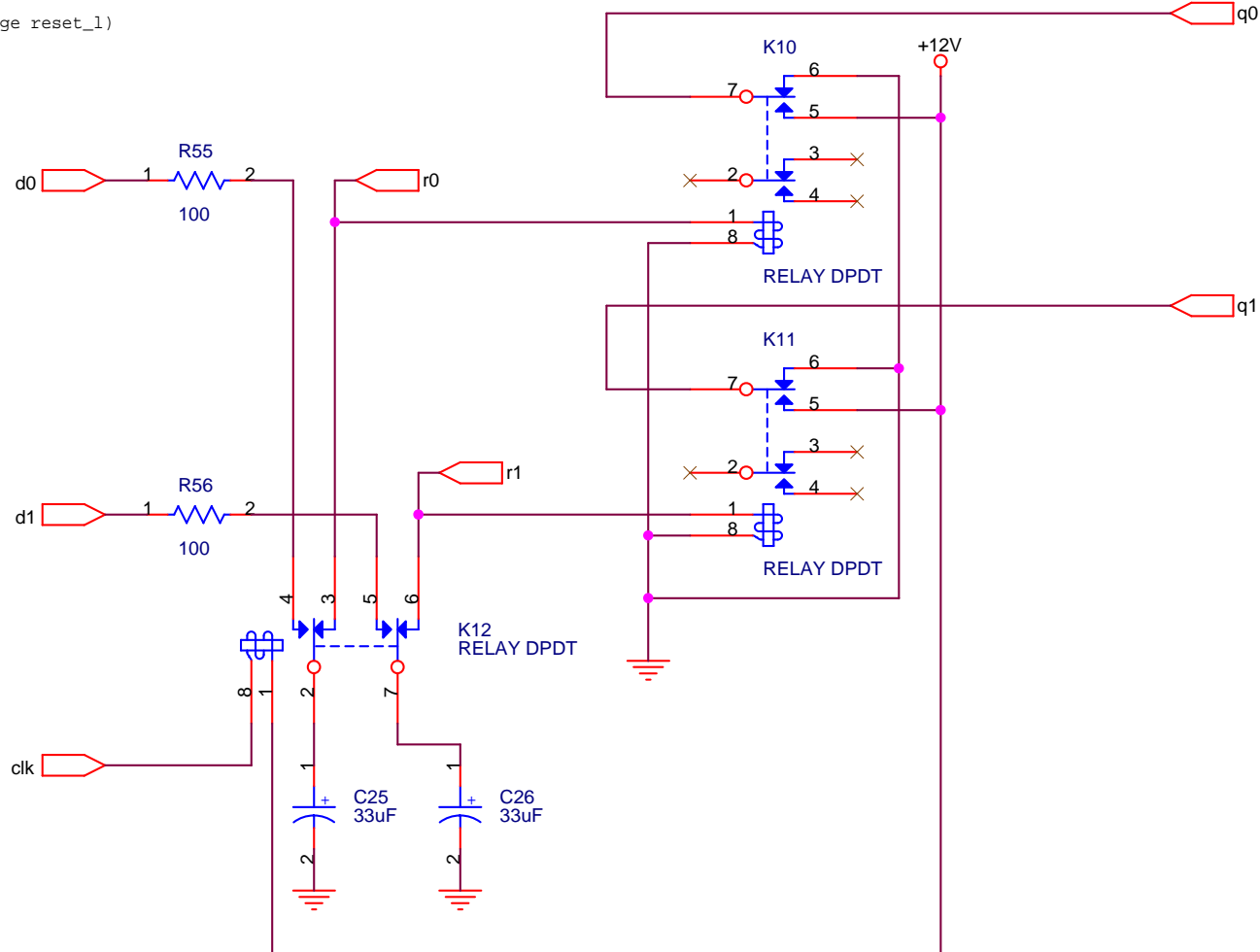
Date: Saturday, September 30, 2017

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```

sim
reg x0;
assign q0 = x0;
always @(posedge clk or negedge reset_1)
  if (!reset_1)
    x0 <= 0;
  else
    x0 <= d0;
reg x1;
assign q1 = x1;
always @(posedge clk or negedge reset_1)
  if (!reset_1)
    x1 <= 0;
  else
    x1 <= d1;

```



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Title

BIT6

Size
A

Document Number
RLY10/RELAYCPU/PC/BIT6

Rev

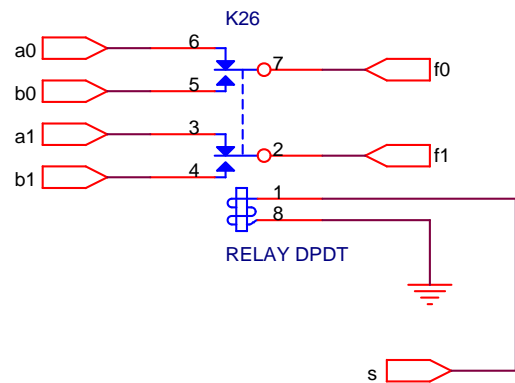
Date: Saturday, September 30, 2017

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```

sim
assign f0 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b0 :
            a0;
assign f1 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b1 :
            a1;

```



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Title

PCIM0

Size
A

Document Number
RLY10/RELAYCPU/PC_MUX/PCIM0

Rev

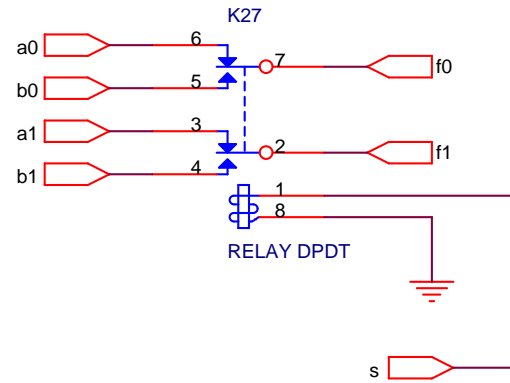
Date: Saturday, September 30, 2017

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```

sim
assign f0 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b0 :
            a0;
assign f1 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b1 :
            a1;

```



(C) 2012 Joseph Allen

Title

PCIM2

Size
A

Document Number
RLY10/RELAYCPU/PC_MUX/PCIM2

Rev

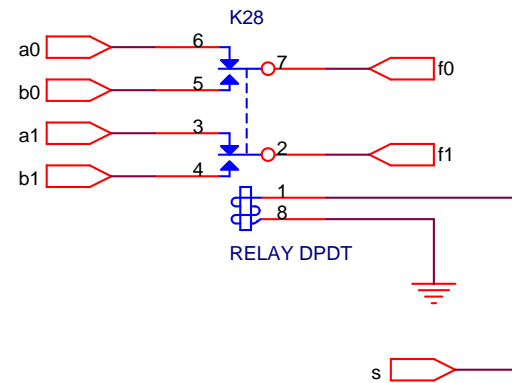
Date: Saturday, September 30, 2017

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```

sim
assign f0 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b0 :
            a0;
assign f1 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b1 :
            a1;

```

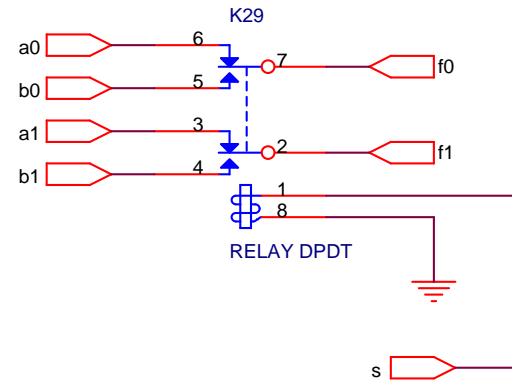


(C) 2012 Joseph Allen			
Title PCIM4			
Size A	Document Number RLY10/RELAYCPU/PC_MUX/PCIM4		Rev
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```

sim
assign f0 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b0 :
            a0;
assign f1 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b1 :
            a1;

```



(C) 2012 Joseph Allen

Title

PCIM6

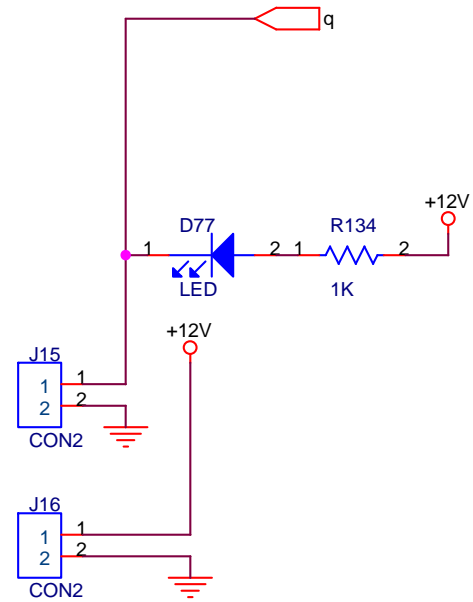
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Document Number
RLY10/RELAYCPU/PC_MUX/PCIM6

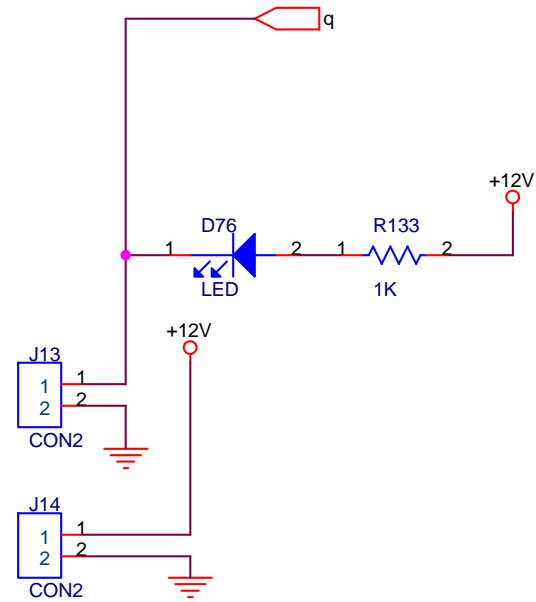
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Date: Saturday, September 30, 2017

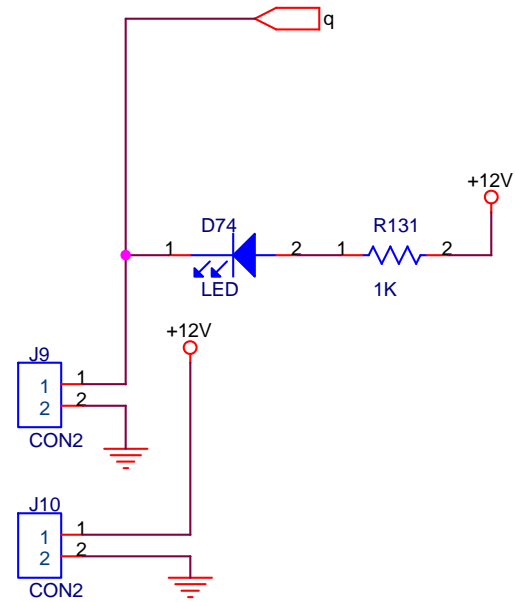
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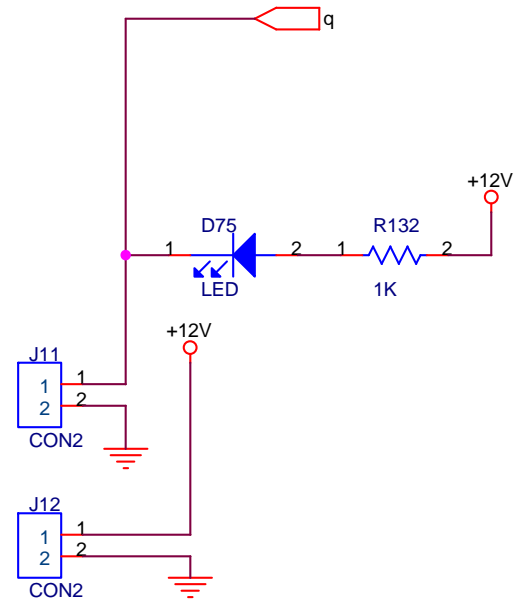
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Title			
INBIT0			
Size	Document Number		Rev
A	RLY10/RELAYCPU/INPORT/INBIT0		
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(C) 2012 Joseph Allen			
Title			
INBIT1			
Size	Document Number		Rev
A	RLY10/RELAYCPU/INPORT/INBIT1		
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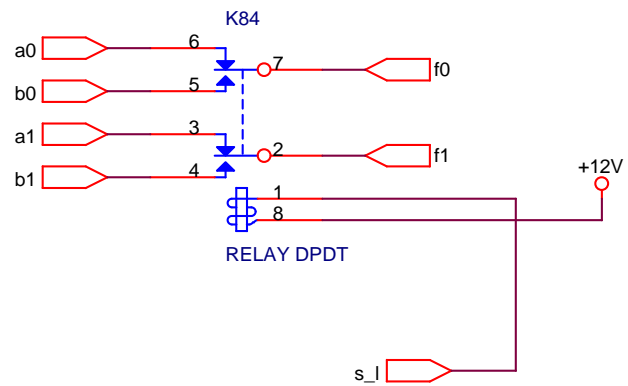


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Title			
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Size	Document Number		Rev
A	RLY10/RELAYCPU/INPORT/INBIT2		
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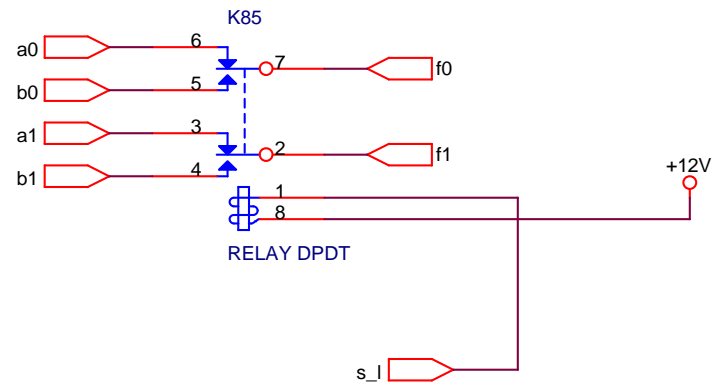


(C) 2012 Joseph Allen			
Title			
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Size	Document Number		Rev
A	RLY10/RELAYCPU/INPORT/INBIT3		
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2:1 Multiplexer



(C) 2012 Joseph Allen			
Title			
INMUX0			
Size	Document Number		Rev
A	RLY10/RELAYCPU/INPORT/INMUX0		
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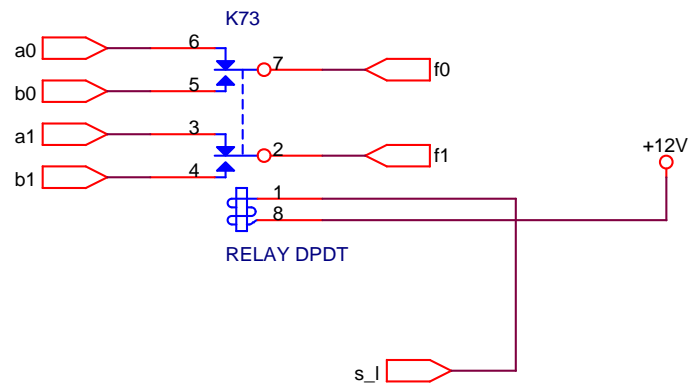


(C) 2012 Joseph Allen			
Title			
INMUX2			
Size	Document Number		Rev
A	RLY10/RELAYCPU/INPORT/INMUX2		
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```

sim
assign f0 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b0 :
            a0;
assign f1 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b1 :
            a1;

```

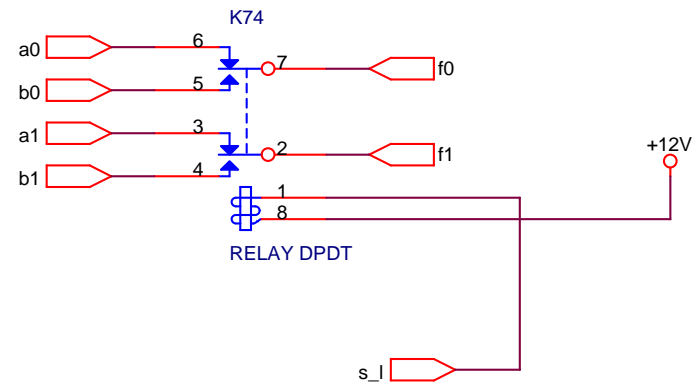


(C) 2012 Joseph Allen		
Title		
JSRM0		
Size	Document Number	Rev
A	RLY10/RELAYCPU/JSR_MUX/JSRM0	
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```

sim
assign f0 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b0 :
            a0;
assign f1 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b1 :
            a1;

```

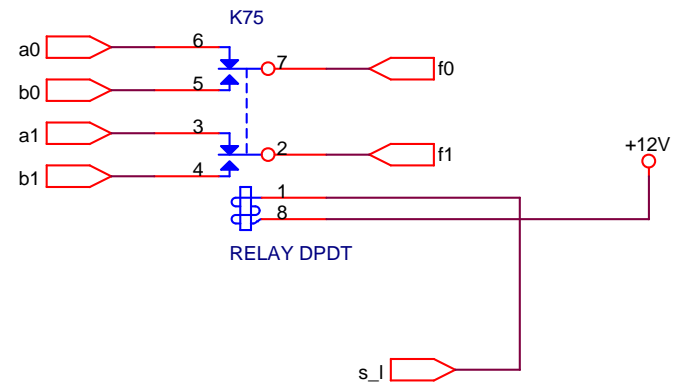


(C) 2012 Joseph Allen			
Title			
JSRM2			
Size	Document Number		Rev
A	RLY10/RELAYCPU/JSR_MUX/JSRM2		
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```

sim
assign f0 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b0 :
            a0;
assign f1 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b1 :
            a1;

```

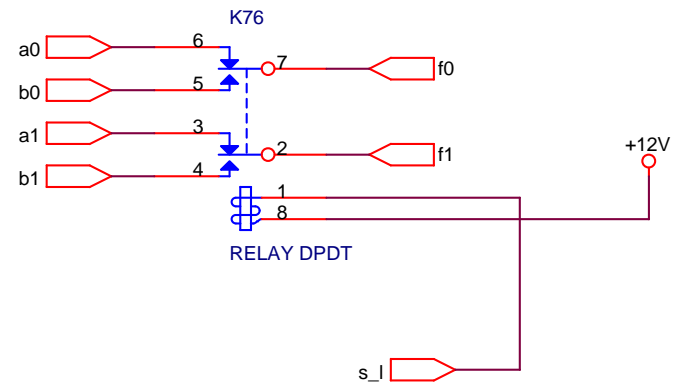


(C) 2012 Joseph Allen			
Title			
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Size	Document Number		Rev
A	RLY10/RELAYCPU/JSR_MUX/JSRM4		
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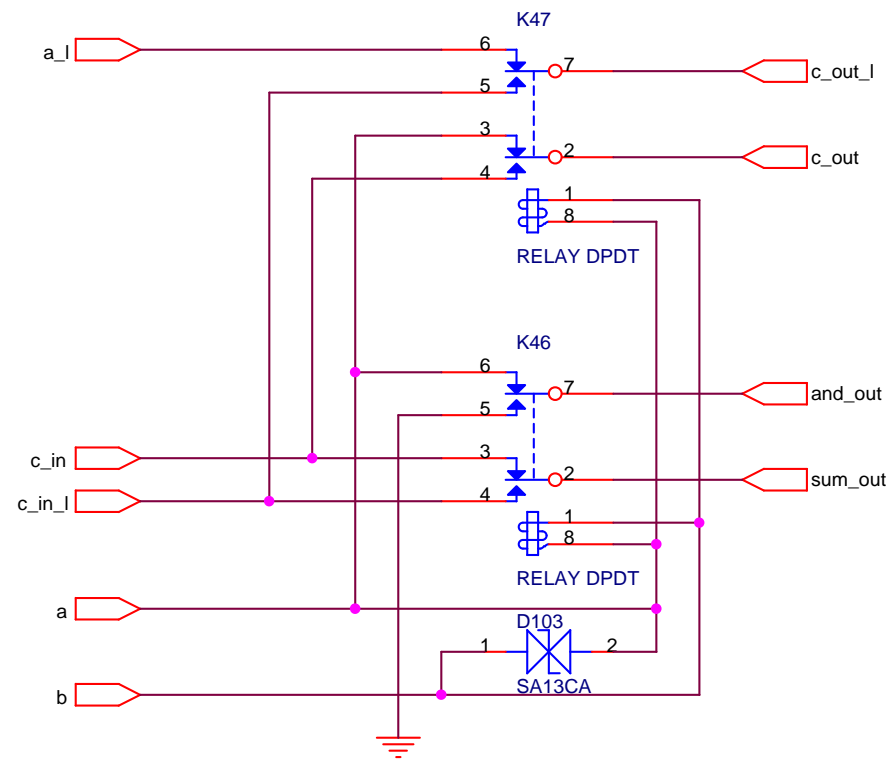
```

sim
assign f0 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b0 :
            a0;
assign f1 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b1 :
            a1;

```



(C) 2012 Joseph Allen			
Title			
JSRM6			
Size	Document Number		Rev
A	RLY10/RELAYCPU/JSR_MUX/JSRM6		
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```

sim
assign sum_out = a ^ b ? c_in_l : c_in;
assign and_out = a ^ b ? 1'b0 : a;
assign c_out = a ^ b ? c_in : a;
assign c_out_l = a ^ b ? c_in_l : a_l;

```

(C) 2012 Joseph Allen

Title

ADDBIT0

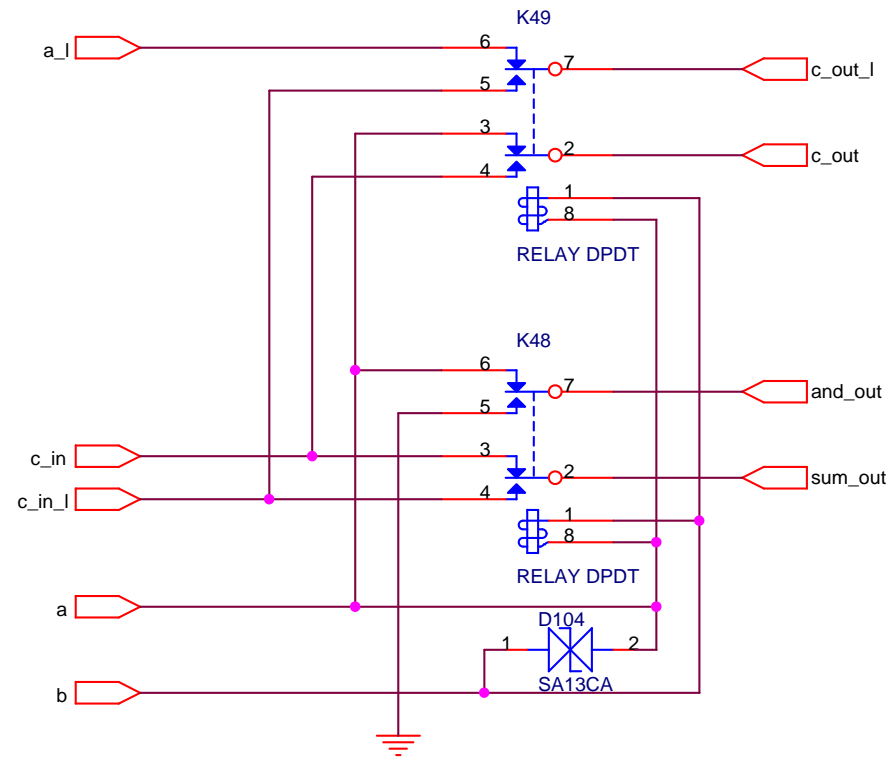
Size
A

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RLY10/RELAYCPU/ALU/ADDER/ADDBIT0

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```

sim
assign sum_out = a ^ b ? c_in_l : c_in;
assign and_out = a ^ b ? 1'b0 : a;
assign c_out = a ^ b ? c_in : a;
assign c_out_l = a ^ b ? c_in_l : a_l;

```

(C) 2012 Joseph Allen

Title

ADDBIT1

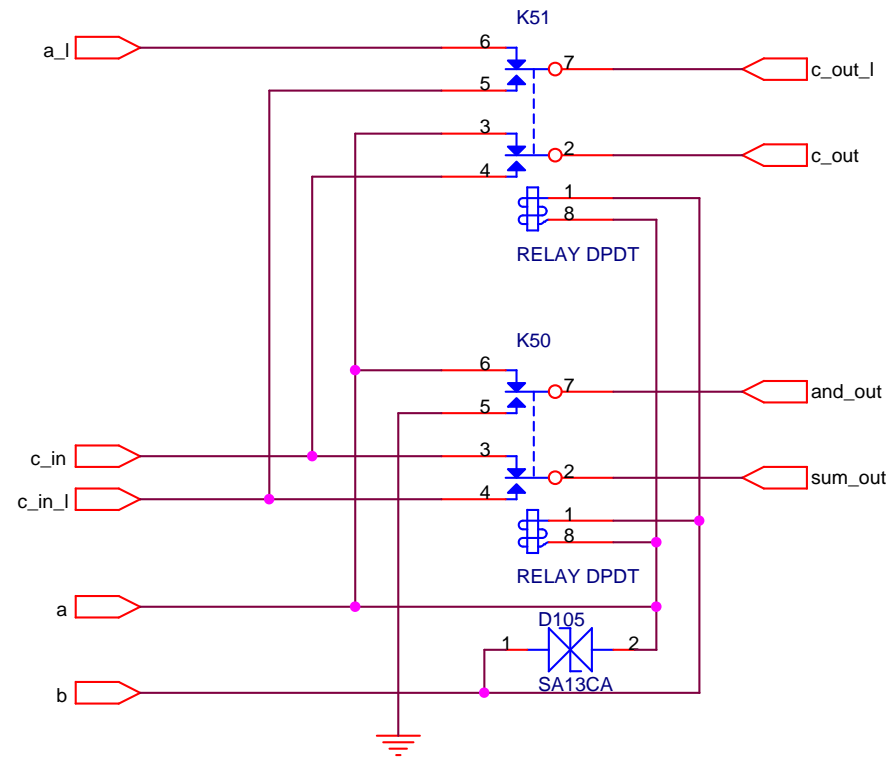
Size
A

Document Number
RLY10/RELAYCPU/ALU/ADDER/ADDBIT1

Rev

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```

sim
assign sum_out = a ^ b ? c_in_l : c_in;
assign and_out = a ^ b ? 1'b0 : a;
assign c_out = a ^ b ? c_in : a;
assign c_out_l = a ^ b ? c_in_l : a_l;

```

(C) 2012 Joseph Allen

Title

ADDBIT2

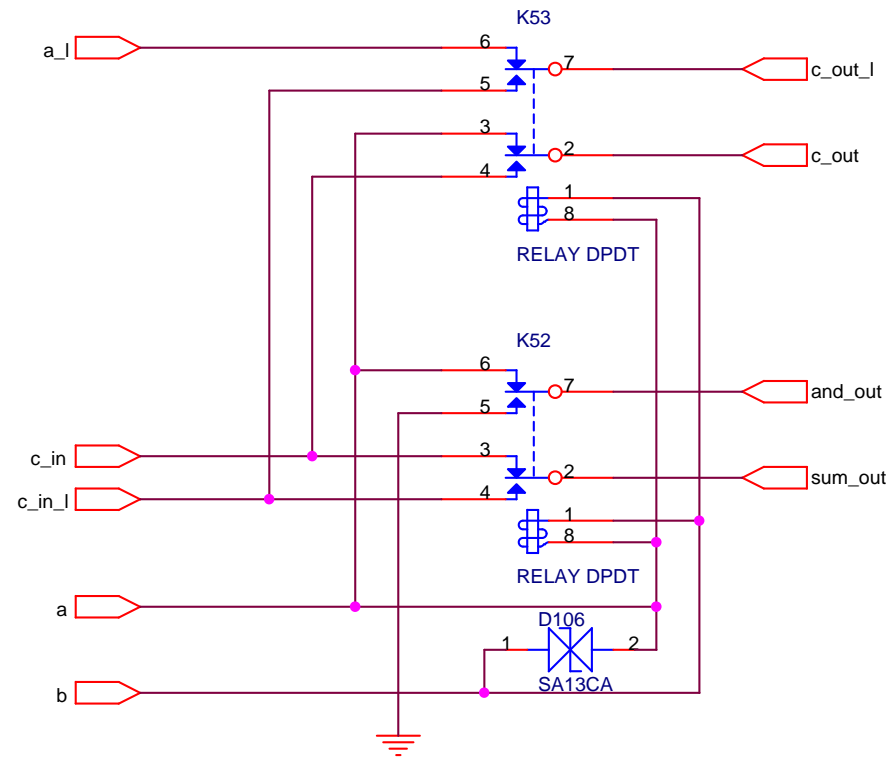
Size
A

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```

sim
assign sum_out = a ^ b ? c_in_l : c_in;
assign and_out = a ^ b ? 1'b0 : a;
assign c_out = a ^ b ? c_in : a;
assign c_out_l = a ^ b ? c_in_l : a_l;

```

(C) 2012 Joseph Allen

Title

ADDBIT3

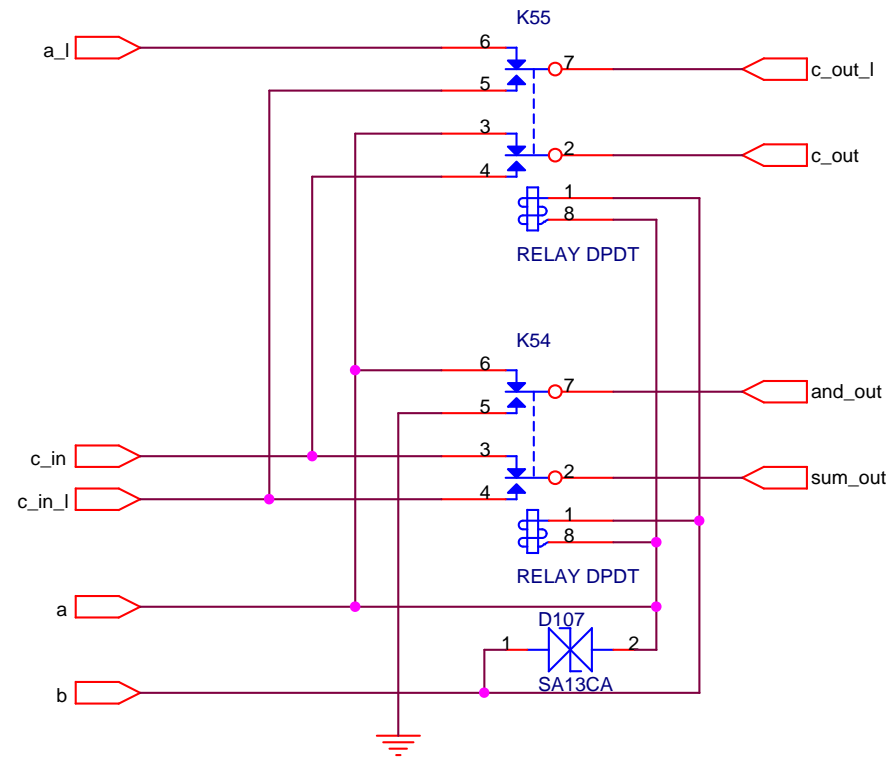
Size
A

Document Number
RLY10/RELAYCPU/ALU/ADDER/ADDBIT3

Rev

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```

sim
assign sum_out = a ^ b ? c_in_l : c_in;
assign and_out = a ^ b ? 1'b0 : a;
assign c_out = a ^ b ? c_in : a;
assign c_out_l = a ^ b ? c_in_l : a_l;

```

(C) 2012 Joseph Allen

Title

ADDBIT4

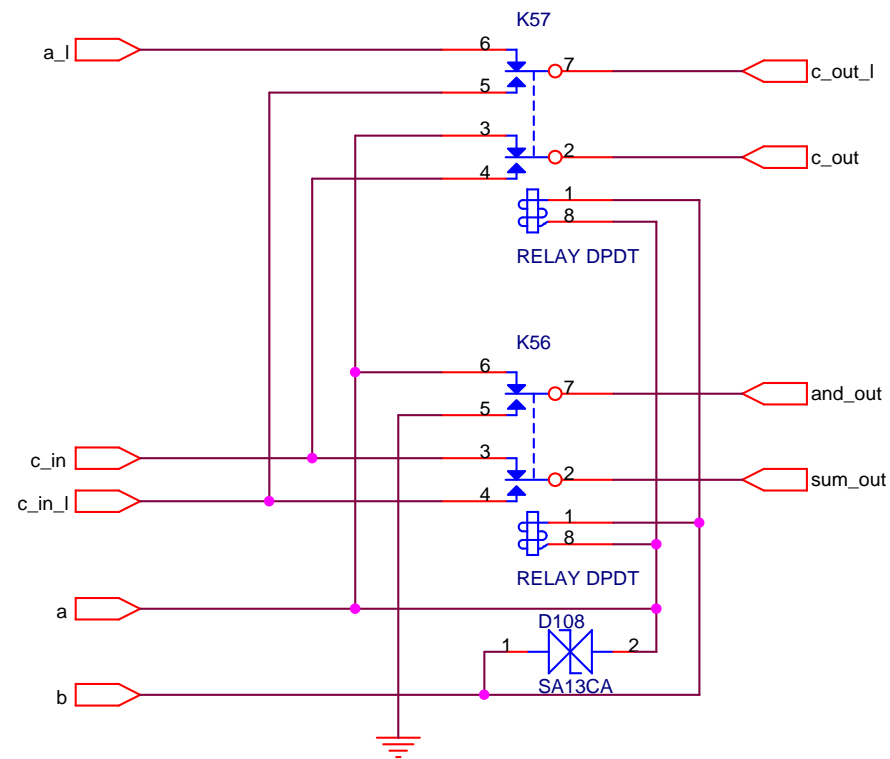
Size
A

Document Number
RLY10/RELAYCPU/ALU/ADDER/ADDBIT4

Rev

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```

sim
assign sum_out = a ^ b ? c_in_l : c_in;
assign and_out = a ^ b ? 1'b0 : a;
assign c_out = a ^ b ? c_in : a;
assign c_out_l = a ^ b ? c_in_l : a_l;

```

(C) 2012 Joseph Allen

Title

ADDBIT5

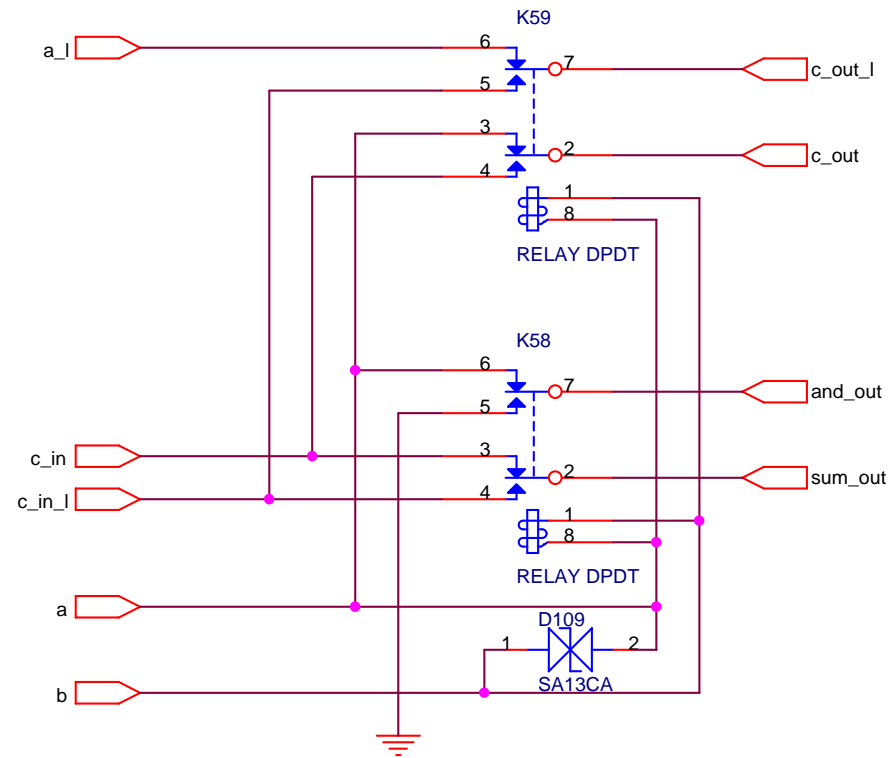
Size
A

Document Number
RLY10/RELAYCPU/ALU/ADDER/ADDBIT5

Rev

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```

sim
assign sum_out = a ^ b ? c_in_l : c_in;
assign and_out = a ^ b ? 1'b0 : a;
assign c_out = a ^ b ? c_in : a;
assign c_out_l = a ^ b ? c_in_l : a_l;

```

(C) 2012 Joseph Allen

Title

ADDBIT6

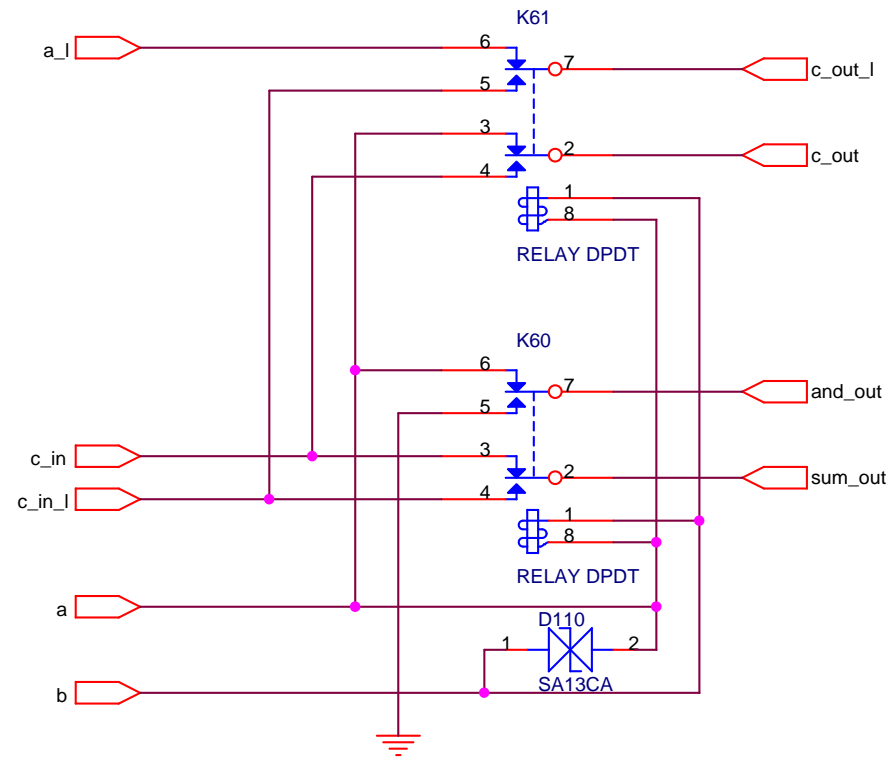
Size
A

Document Number
RLY10/RELAYCPU/ALU/ADDER/ADDBIT6

Rev

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```

sim
assign sum_out = a ^ b ? c_in_l : c_in;
assign and_out = a ^ b ? 1'b0 : a;
assign c_out = a ^ b ? c_in : a;
assign c_out_l = a ^ b ? c_in_l : a_l;

```

(C) 2012 Joseph Allen

Title

ADDBIT7

Size
A

Document Number
RLY10/RELAYCPU/ALU/ADDER/ADDBIT7

Rev

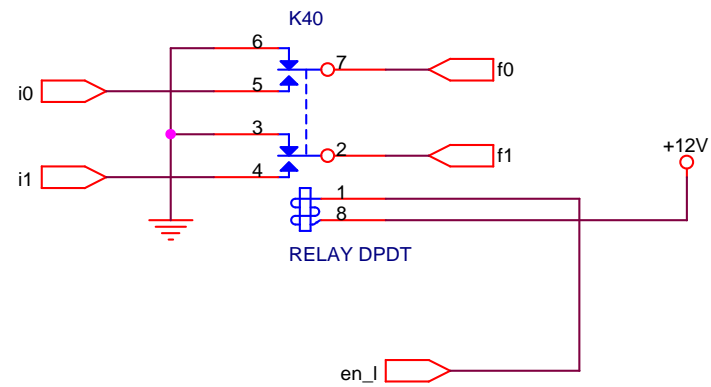
Date: Saturday, September 30, 2017

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```

sim
assign f0 = (en == 1'bx) ? 1'bx :
            (en == 1'b1) ? i0 :
            1'b0;
assign f1 = (en == 1'bx) ? 1'bx :
            (en == 1'b1) ? i1 :
            1'b0;

```

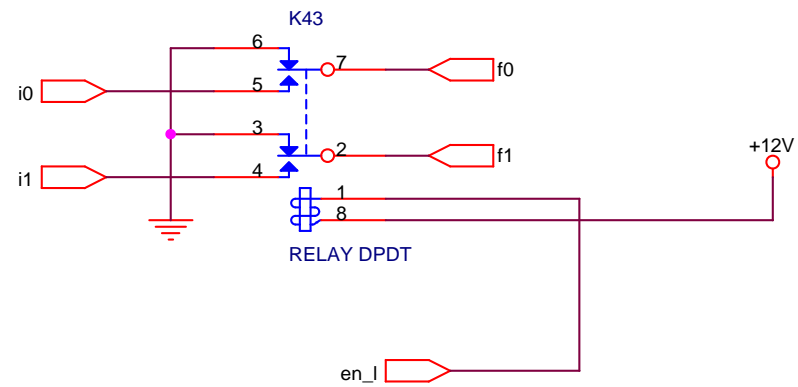


(C) 2012 Joseph Allen			
Title			
BGATE0			
Size	Document Number		Rev
A	RLY10/RELAYCPU/ALU/B_GATE/BGATE0		
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```

sim
assign f0 = (en == 1'bx) ? 1'bx :
            (en == 1'b1) ? i0 :
            1'b0;
assign f1 = (en == 1'bx) ? 1'bx :
            (en == 1'b1) ? i1 :
            1'b0;

```



(C) 2012 Joseph Allen

Title

BGATE2

Size
A

Document Number
RLY10/RELAYCPU/ALU/B_GATE/BGATE2

Rev

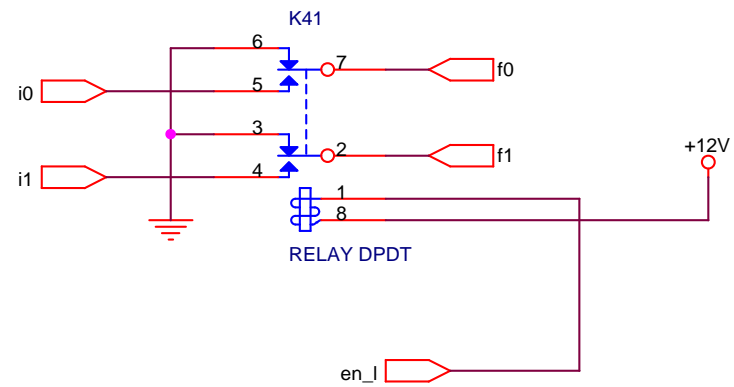
Date: Saturday, September 30, 2017

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```

sim
assign f0 = (en == 1'bx) ? 1'bx :
            (en == 1'b1) ? i0 :
            1'b0;
assign f1 = (en == 1'bx) ? 1'bx :
            (en == 1'b1) ? i1 :
            1'b0;

```

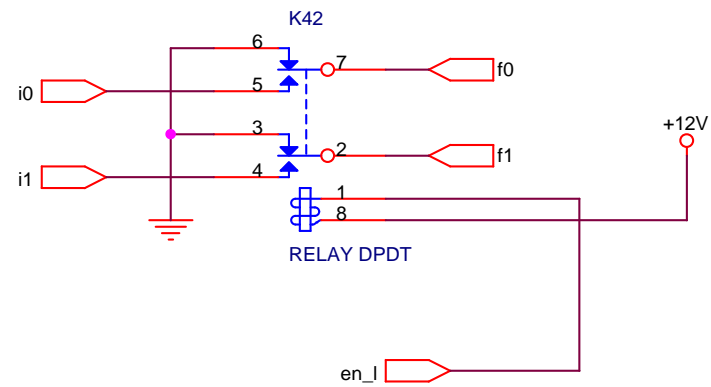


(C) 2012 Joseph Allen			
Title			
BGATE4			
Size	Document Number		Rev
A	RLY10/RELAYCPU/ALU/B_GATE/BGATE4		
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```

sim
assign f0 = (en == 1'bx) ? 1'bx :
            (en == 1'b1) ? i0 :
            1'b0;
assign f1 = (en == 1'bx) ? 1'bx :
            (en == 1'b1) ? i1 :
            1'b0;

```



(C) 2012 Joseph Allen

Title

BGATE6

Size
A

Document Number
RLY10/RELAYCPU/ALU/B_GATE/BGATE6

Rev

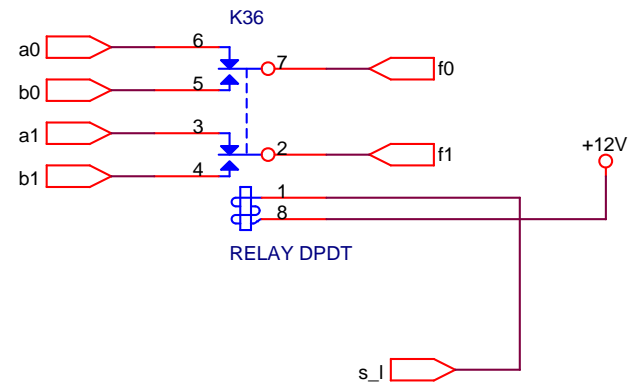
Date: Saturday, September 30, 2017

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```

sim
assign f0 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b0 :
            a0;
assign f1 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b1 :
            a1;

```

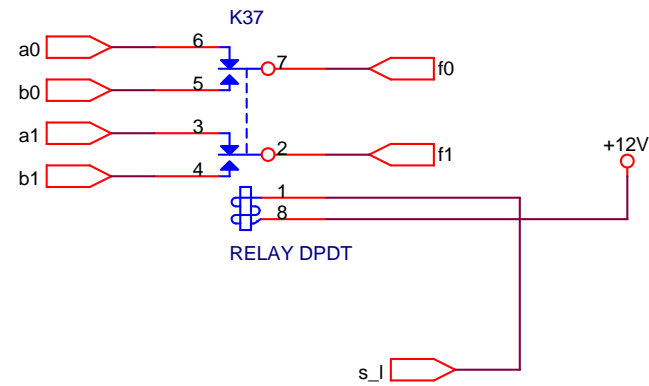


(C) 2012 Joseph Allen			
Title			
ANDM0			
Size	Document Number		Rev
A	RLY10/RELAYCPU/ALU/AND_MUX/ANDM0		
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```

sim
assign f0 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b0 :
            a0;
assign f1 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b1 :
            a1;

```

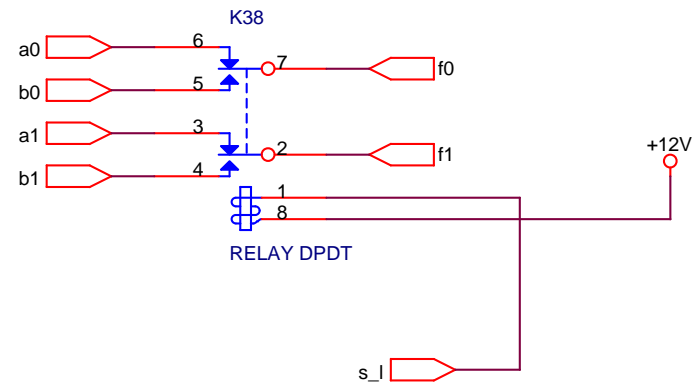


(C) 2012 Joseph Allen			
Title			
ANDM2			
Size	Document Number		Rev
A	RLY10/RELAYCPU/ALU/AND_MUX/ANDM2		
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```

sim
assign f0 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b0 :
            a0;
assign f1 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b1 :
            a1;

```

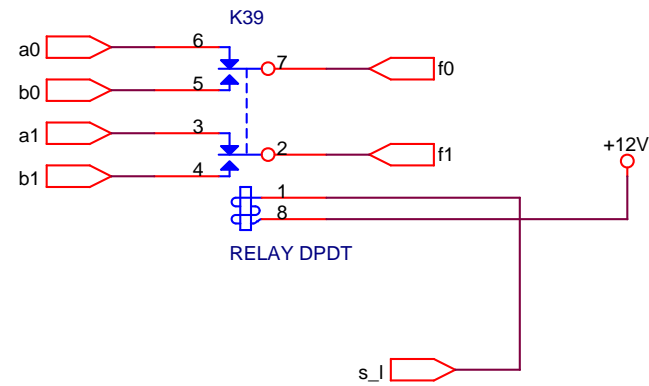


(C) 2012 Joseph Allen			
Title			
ANDM4			
Size	Document Number		Rev
A	RLY10/RELAYCPU/ALU/AND_MUX/ANDM4		
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```

sim
assign f0 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b0 :
            a0;
assign f1 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b1 :
            a1;

```

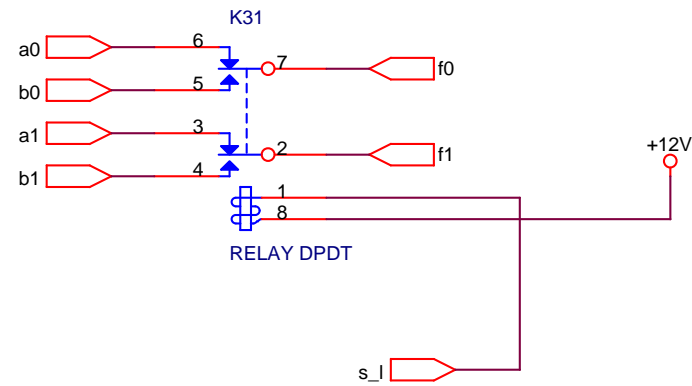


(C) 2012 Joseph Allen			
Title			
ANDM6			
Size	Document Number		Rev
A	RLY10/RELAYCPU/ALU/AND_MUX/ANDM6		
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```

sim
assign f0 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b0 :
            a0;
assign f1 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b1 :
            a1;

```

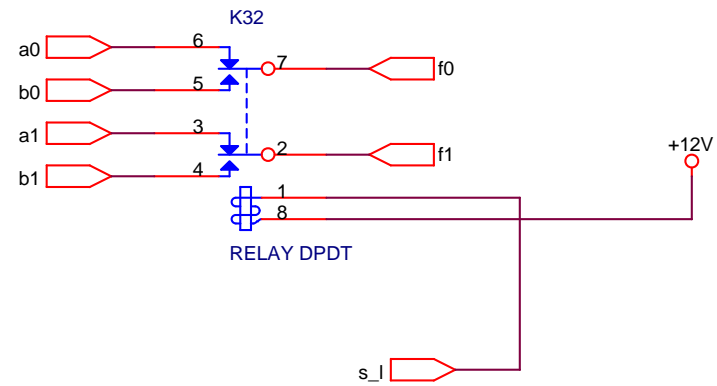


(C) 2012 Joseph Allen			
Title			
RORM0			
Size	Document Number		Rev
A	RLY10/RELAYCPU/ALU/ROR/RORM0		
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```

sim
assign f0 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b0 :
            a0;
assign f1 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b1 :
            a1;

```

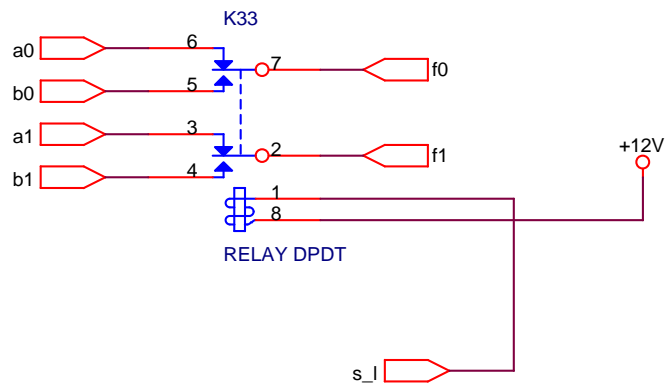


(C) 2012 Joseph Allen			
Title			
RORM2			
Size	Document Number		Rev
A	RLY10/RELAYCPU/ALU/ROR/RORM2		
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```

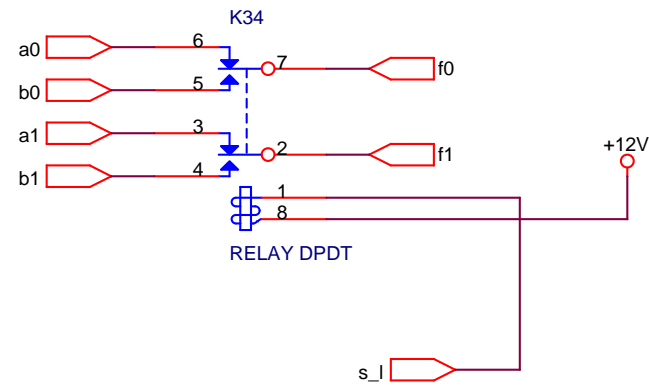
sim
assign f0 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b0 :
            a0;
assign f1 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b1 :
            a1;

```



(C) 2012 Joseph Allen			
Title			
RORM4			
Size	Document Number		Rev
A	RLY10/RELAYCPU/ALU/ROR/RORM4		
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```
sim
assign f0 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b0 :
            a0;
assign f1 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b1 :
            a1;
```

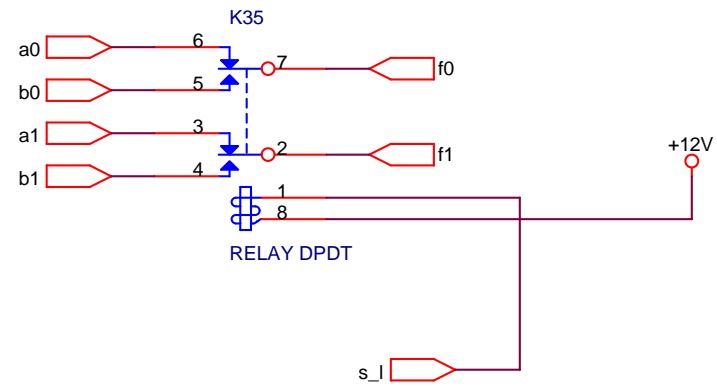


(C) 2012 Joseph Allen			
Title			
RORM6			
Size	Document Number		Rev
A	RLY10/RELAYCPU/ALU/ROR/RORM6		
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```

sim
assign f0 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b0 :
            a0;
assign f1 = (s === 1'bx) ? 1'bx :
            (s === 1'b1) ? b1 :
            a1;

```

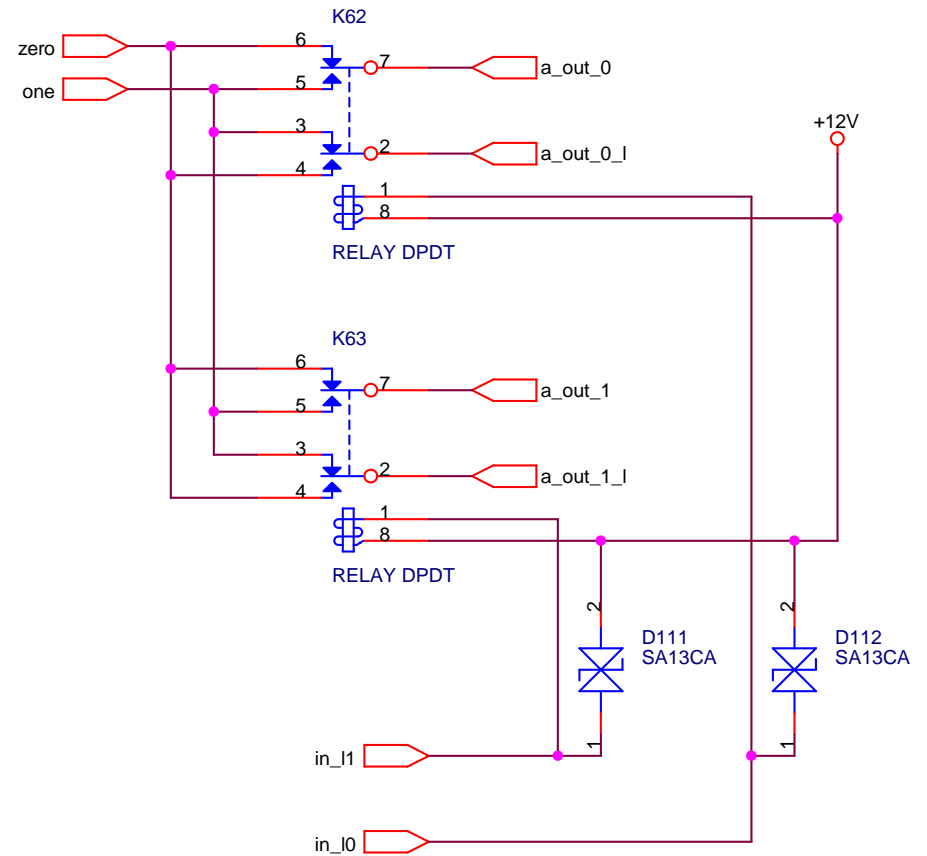


(C) 2012 Joseph Allen			
Title			
RORM8			
Size	Document Number		Rev
A	RLY10/RELAYCPU/ALU/ROR/RORM8		
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```

sim
assign a_out_0 = (clr === 1'bx) ? 1'bx :
  (clr === 1'b1) ? zero :
  (a_in_0 === 1'bx) ? 1'bx :
  (a_in_0 === 1'b1) ? one :
  zero;
assign a_out_1 = (clr === 1'bx) ? 1'bx :
  (clr === 1'b1) ? zero :
  (a_in_1 === 1'bx) ? 1'bx :
  (a_in_1 === 1'b1) ? one :
  zero;
assign a_out_0_1 = (clr === 1'bx) ? 1'bx :
  (clr === 1'b1) ? one :
  (a_in_0 === 1'bx) ? 1'bx :
  (a_in_0 === 1'b1) ? zero :
  one;
assign a_out_1_1 = (clr === 1'bx) ? 1'bx :
  (clr === 1'b1) ? one :
  (a_in_1 === 1'bx) ? 1'bx :
  (a_in_1 === 1'b1) ? zero :
  one;

```



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Title
A_GATE_0

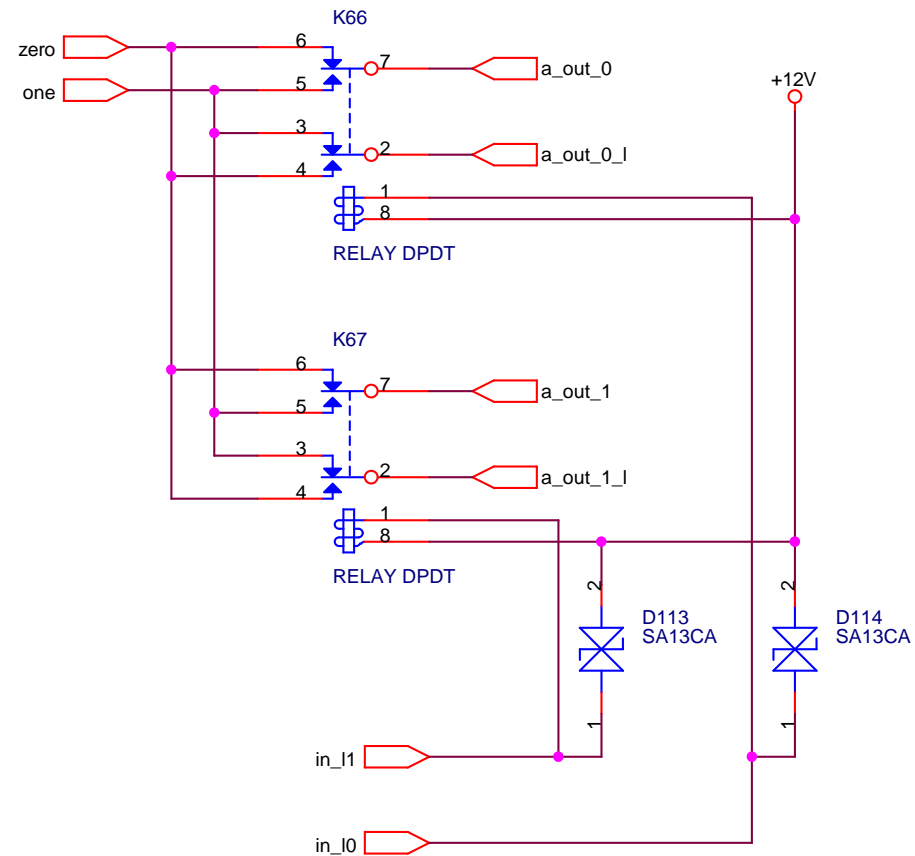
Size A Document Number RLY10/RELAYCPU/ALU/A_GATE/A_GATE_0 Rev

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```

sim
assign a_out_0 = (clr === 1'bx) ? 1'bx :
                 (clr === 1'b1) ? zero :
                 (a_in_0 === 1'bx) ? 1'bx :
                 (a_in_0 === 1'b1) ? one :
                 zero;
assign a_out_1 = (clr === 1'bx) ? 1'bx :
                 (clr === 1'b1) ? zero :
                 (a_in_1 === 1'bx) ? 1'bx :
                 (a_in_1 === 1'b1) ? one :
                 zero;
assign a_out_0_1 = (clr === 1'bx) ? 1'bx :
                  (clr === 1'b1) ? one :
                  (a_in_0 === 1'bx) ? 1'bx :
                  (a_in_0 === 1'b1) ? zero :
                  one;
assign a_out_1_1 = (clr === 1'bx) ? 1'bx :
                  (clr === 1'b1) ? one :
                  (a_in_1 === 1'bx) ? 1'bx :
                  (a_in_1 === 1'b1) ? zero :
                  one;

```



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Title

A_GATE_2

Size
A

Document Number
RLY10/RELAYCPU/ALU/A_GATE/A_GATE_2

Rev

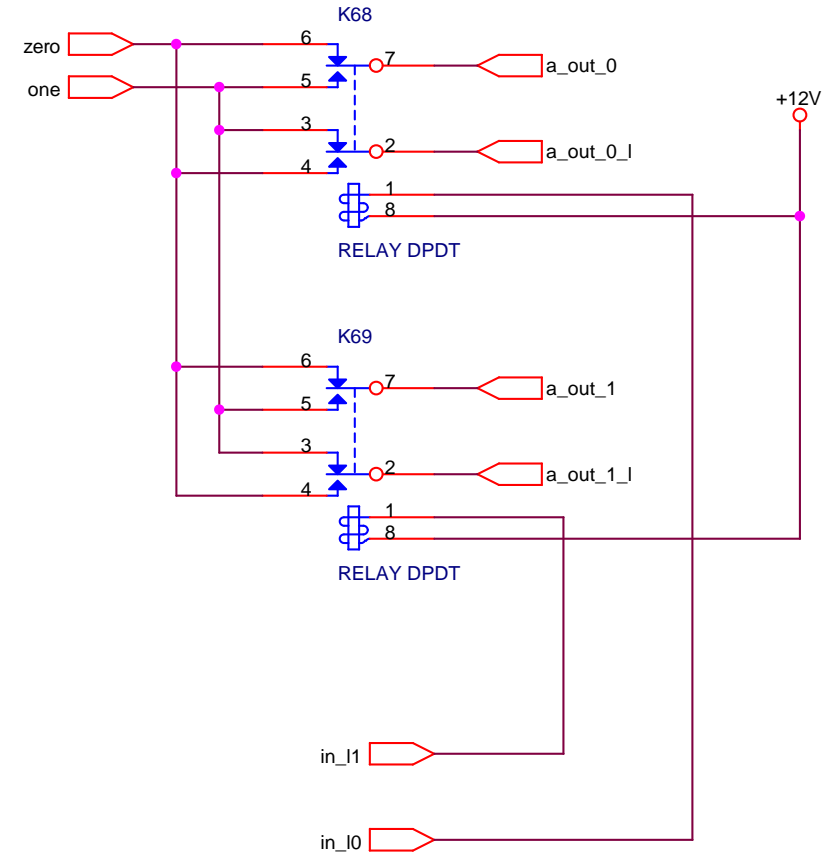
Date: Saturday, September 30, 2017

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```

sim
assign a_out_0 = (clr == 1'bx) ? 1'bx :
  (clr == 1'b1) ? zero :
  (a_in_0 == 1'bx) ? 1'bx :
  (a_in_0 == 1'b1) ? one :
  zero;
assign a_out_1 = (clr == 1'bx) ? 1'bx :
  (clr == 1'b1) ? zero :
  (a_in_1 == 1'bx) ? 1'bx :
  (a_in_1 == 1'b1) ? one :
  zero;
assign a_out_0_l = (clr == 1'bx) ? 1'bx :
  (clr == 1'b1) ? one :
  (a_in_0 == 1'bx) ? 1'bx :
  (a_in_0 == 1'b1) ? zero :
  one;
assign a_out_1_l = (clr == 1'bx) ? 1'bx :
  (clr == 1'b1) ? one :
  (a_in_1 == 1'bx) ? 1'bx :
  (a_in_1 == 1'b1) ? zero :
  one;

```



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Title

A_GATE_4

Size
A

Document Number
RLY10/RELAYCPU/ALU/A_GATE/A_GATE_4

Rev

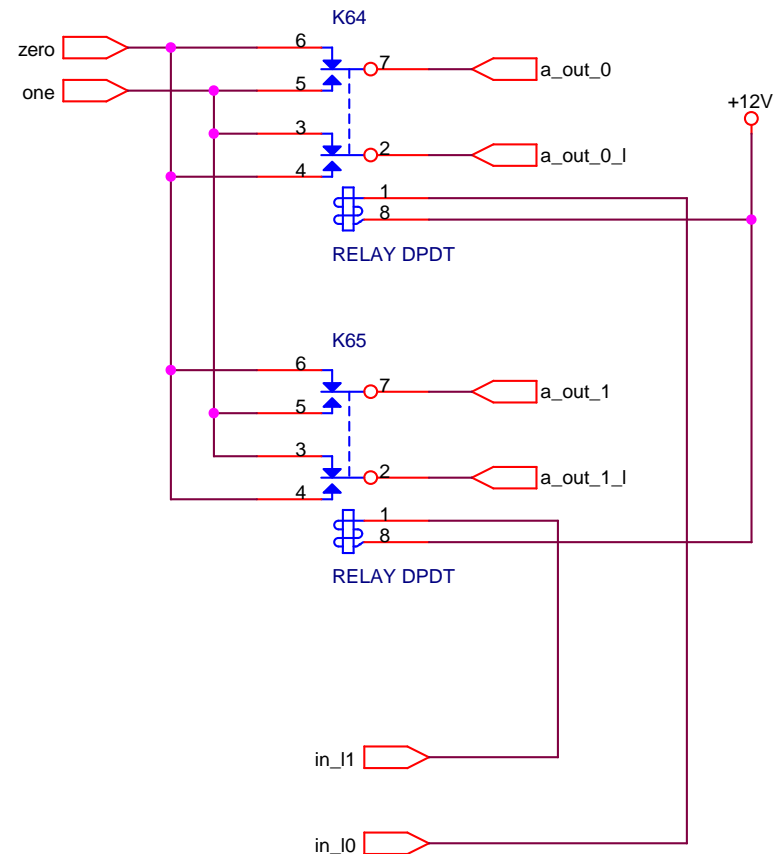
Date: Saturday, September 30, 2017

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```

sim
assign a_out_0 = (clr === 1'bx) ? 1'bx :
                 (clr === 1'bl) ? zero :
                 (a_in_0 === 1'bx) ? 1'bx :
                 (a_in_0 === 1'bl) ? one :
                 zero;
assign a_out_1 = (clr === 1'bx) ? 1'bx :
                 (clr === 1'bl) ? zero :
                 (a_in_1 === 1'bx) ? 1'bx :
                 (a_in_1 === 1'bl) ? one :
                 zero;
assign a_out_0_1 = (clr === 1'bx) ? 1'bx :
                  (clr === 1'bl) ? one :
                  (a_in_0 === 1'bx) ? 1'bx :
                  (a_in_0 === 1'bl) ? zero :
                  one;
assign a_out_1_1 = (clr === 1'bx) ? 1'bx :
                  (clr === 1'bl) ? one :
                  (a_in_1 === 1'bx) ? 1'bx :
                  (a_in_1 === 1'bl) ? zero :
                  one;

```



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Title
A_GATE_6

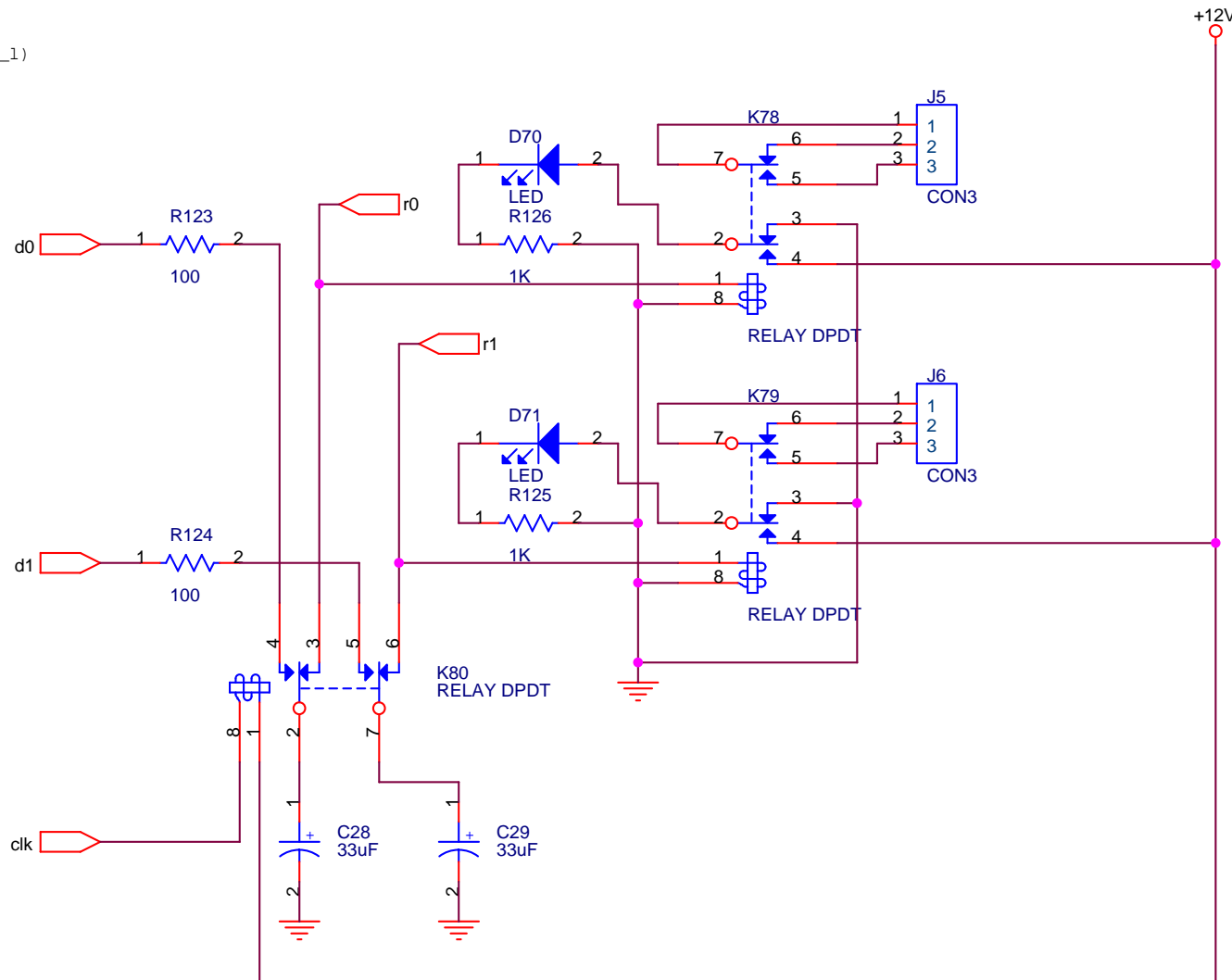
Size A Document Number RLY10/RELAYCPU/ALU/A_GATE/A_GATE_6 Rev

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```

sim
reg x0;
assign q0 = x0;
always @(posedge clk or negedge reset_l)
  if (!reset_l)
    x0 <= 0;
  else
    x0 <= d0;
reg x1;
assign q1 = x1;
always @(posedge clk or negedge reset_l)
  if (!reset_l)
    x1 <= 0;
  else
    x1 <= d1;

```



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Title

OUTBIT0

Size
A

Document Number
RLY10/RELAYCPU/OUTPORT/OUTBIT0

Rev

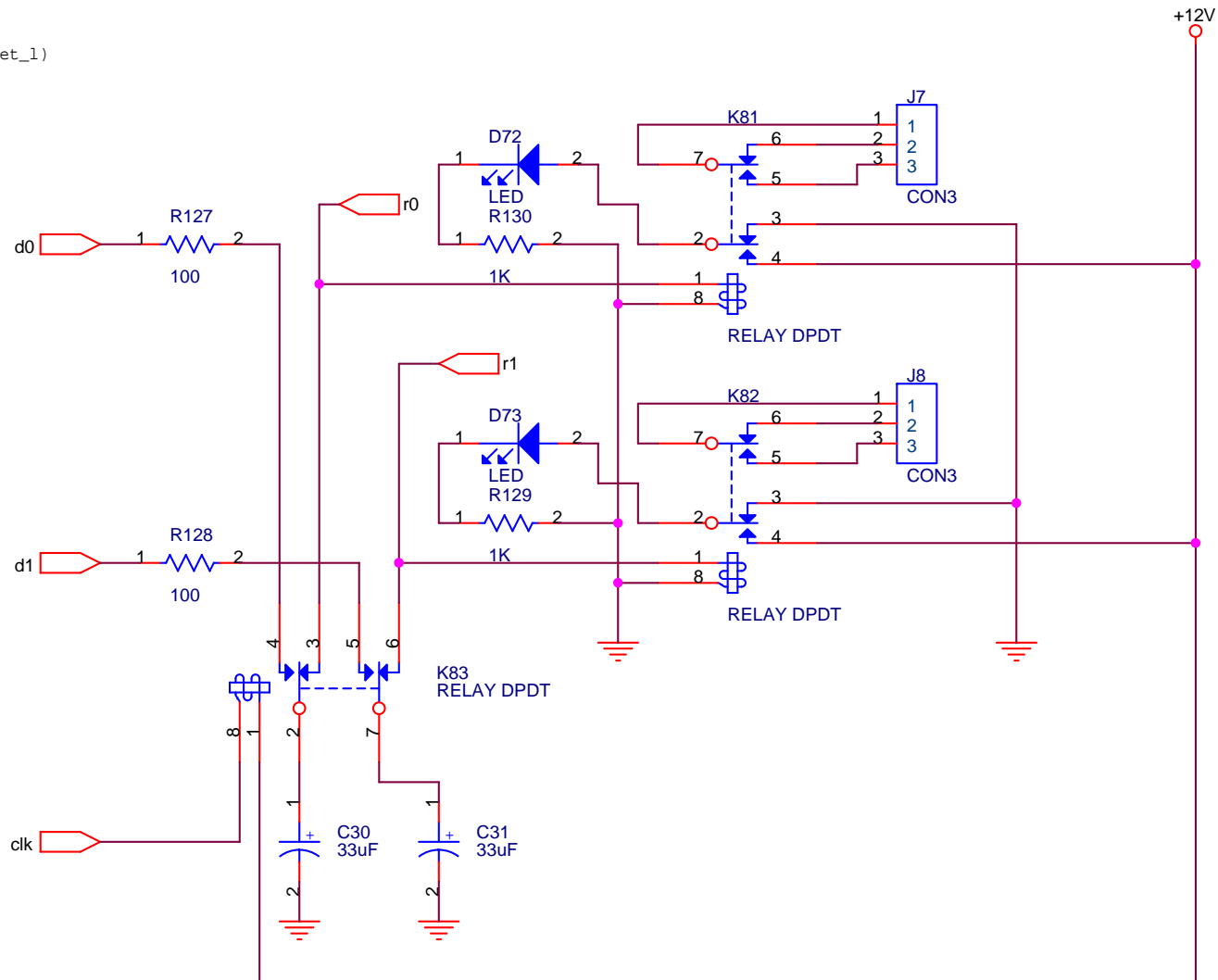
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```

sim
reg x0;
assign q0 = x0;
always @(posedge clk or negedge reset_1)
  if (!reset_1)
    x0 <= 0;
  else
    x0 <= d0;
reg x1;
assign q1 = x1;
always @(posedge clk or negedge reset_1)
  if (!reset_1)
    x1 <= 0;
  else
    x1 <= d1;

```



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Title

OUTBIT2

Size
A

Document Number
RLY10/RELAYCPU/OUTPORT/OUTBIT2

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