AN486: High-Side Bootstrap Design Using ISODrivers in Power Delivery Systems

Silicon Labs ISOdrivers are isolated gate drivers that combine low latency, high-drive-strength gate drive circuits with on-chip isolation.

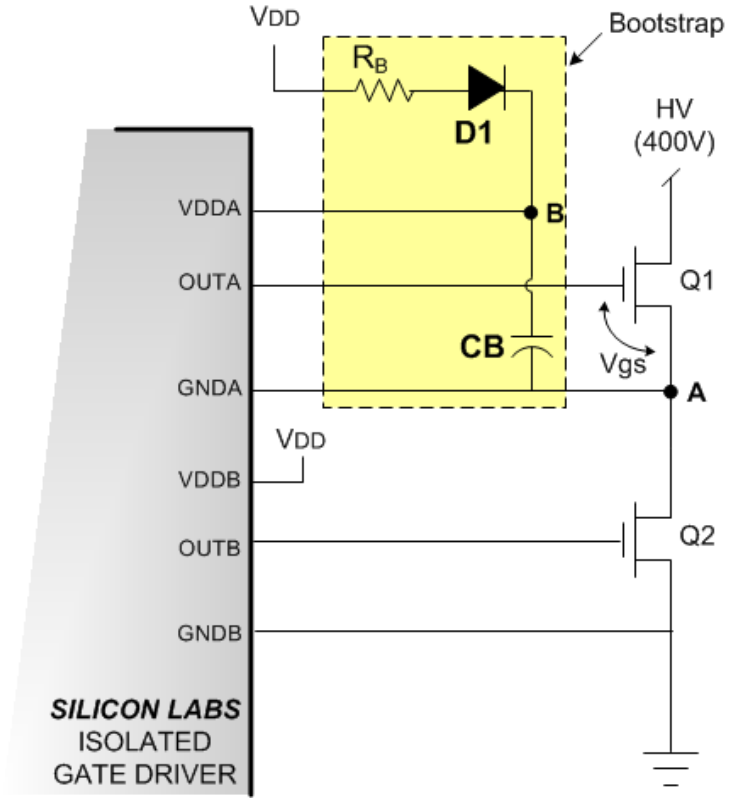
For robust and safe operation, designers of ac-dc and isolated dc-dc switch mode power supplies (SMPS), uninterruptible power supplies (UPS), solar inverters, and electronic lighting ballasts must rely not only on a properly selected high side/low-side gate driver IC, but also on an external bootstrap circuit and its PCB layout.

The ISOdriver high-side drive channel(s) require(s) a bootstrap circuit when the high-side switch has a drain voltage greater than the ISOdriver's VDDA supply.

The bootstrap capacitor, C_B, in the figure below charges when the low-side driver is active, then supplies driver bias to the high side driver when active. At first glance, the bootstrap appears as a simple, low-cost circuit consisting only of diode D1 and capacitor C_B (and sometimes resistor R_B). But beneath this humble facade lurks potential design challenges. This application note discusses the operation and design of the high side bootstrap circuit shown below and presents a methodology for bootstrap design.

KEY POINTS

- Bootstrap tutorial
- Step-by-step ISOdriver bootstrap design guide and example
- Summary of best layout practices for ISOdriver with bootstrap circuitry
- Bootstrap calculator available



1. Bootstrap Operation

Bootstrap operation is straightforward: C_B is charged during low-side drive where Q2 is on and Q1 is off, as shown in Figure 1.1 Bootstrap Circuit—C_B Charging on page 2. During this period, charge current from the VDD supply flows into the ISOdriver VDDA input and through the charge loop from bootstrap resistor R_B through diode D1, capacitor C_B, and Q2 to ground.

At the end of the low-side drive period, Q2 is turned off and Q1 turned on, as depicted in Figure 1.2 Bootstrap Circuit—C_B Sourcing on page 3. This causes the voltage at Q1's source (and GNDA) to quickly rise toward the Q1 drain voltage, VDRAIN. The voltage at VDDA is equal to the Q1 source voltage plus the voltage across C_B, which has been charged up to approximately VDD – 0.7 V. So, as the Q1 source (and GNDA) voltage rises, diode D1 becomes reverse-biased, effectively disconnecting the ground-based VDD supply from C_B. With D1 reverse-biased, capacitor C_B now provides a supply voltage of VDD– 0.7 V for VDDA, and C_B supplies all the current required to maintain high-side driver operation during the entire time Q2 is turned off.

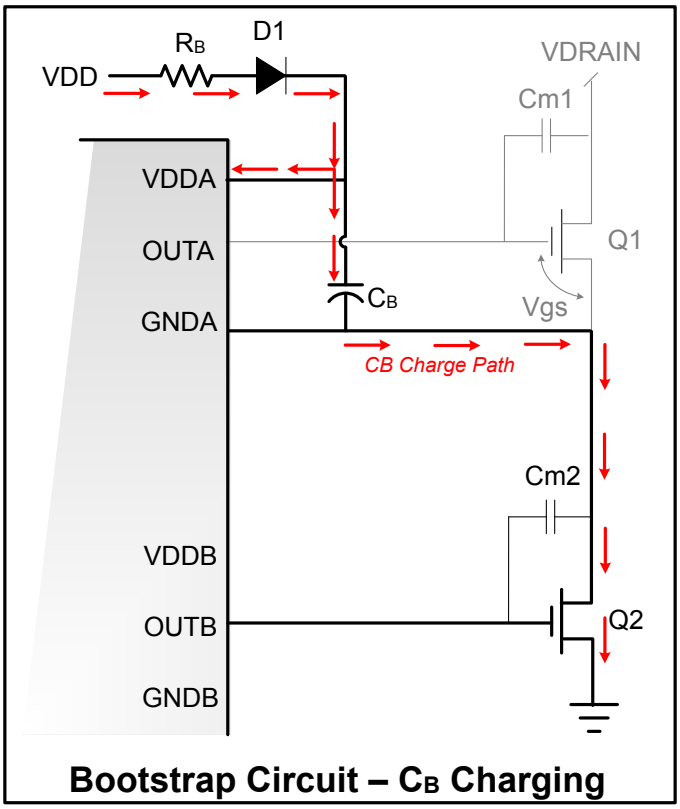


Figure 1.1. Bootstrap Circuit—C_B Charging

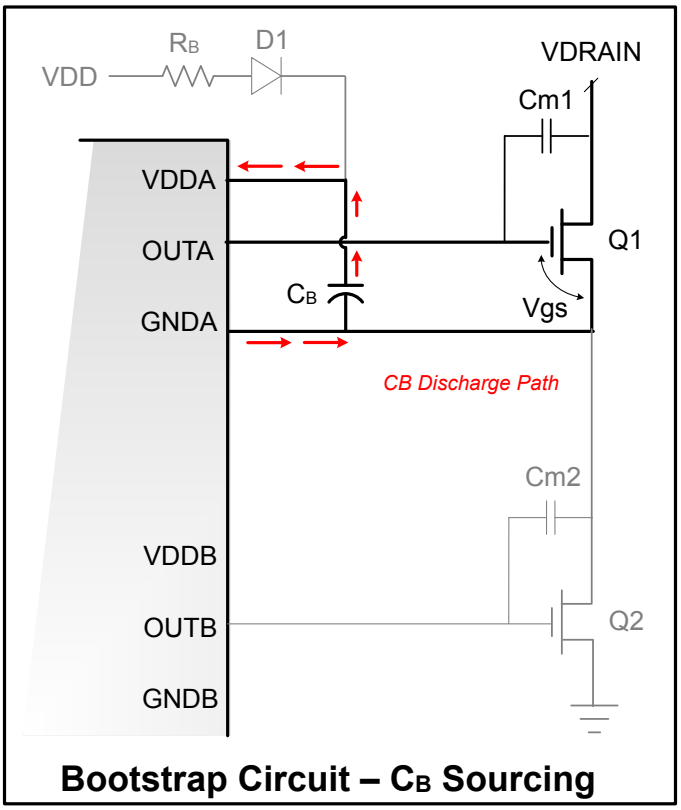


Figure 1.2. Bootstrap Circuit—C_B Sourcing

The figure below shows a typical waveform for the voltage across C_B. The voltage increases through the charging period when Q2 is on. The end of the charge cycle is closely followed by a high negative dV/dt, as the current needed for VOA to charge the gate capacitance of Q1 must be provided through the VDDA supply input from capacitor C_B. The value for the total gate charge, Q_G, should be provided in the datasheet for Q1. After the gate of Q1 is fully charged, current is required only for the gate driver VDDA bias and the current required to maintain charge on the Q1 gate; so, the voltage on CB falls much more slowly. The VDDA bias value is found in the driver data sheet as Output Supply Quiescent Current.

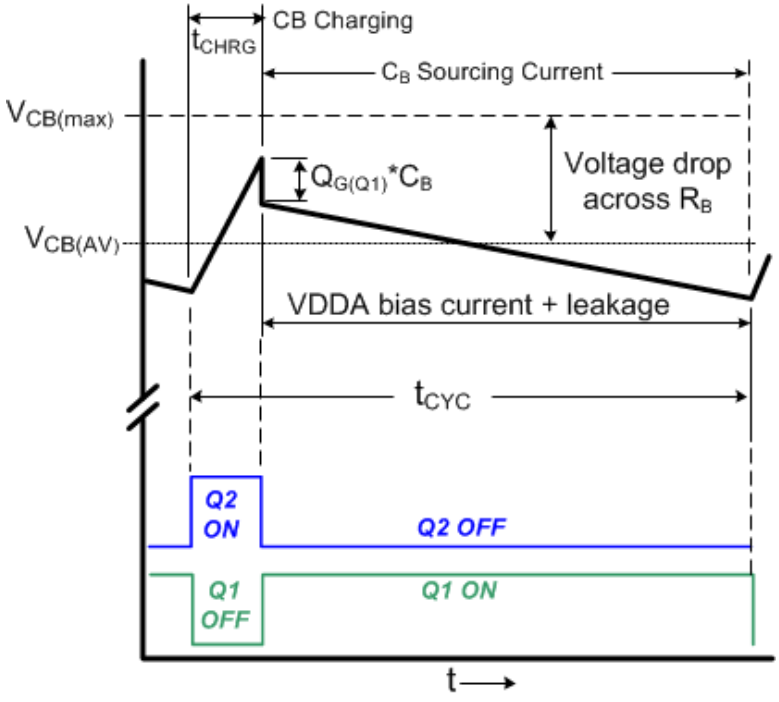


Figure 1.3. Typical C_B Ripple Cycle

1.1 Bootstrap Design

While it is a simple circuit, the bootstrap can be problematic if not designed correctly. In particular, care must be taken to ensure low C_B ripple to avoid triggering the driver's undervoltage lockout, which can halt converter operation; additionally, the refresh period must be sufficient to fully charge C_B. The inherent limitation of the high-side bootstrap circuit is the time required to sufficiently refresh C_B. Some power topologies may have an excessively high duty cycle or frequency to support refresh, or they may have a high-side circuit that causes the load to be in series with the charge path. For those applications, a charge pump (instead of a high-side bootstrap) may be required.

A typical bootstrap design flow first determines the total charge that C_B must deliver during the high-side drive cycle (Q_{CB}). With Q_{CB} known, the value of C_B is calculated based on allowable ripple amplitude and verified adequate refresh under worst-case timing conditions. Note, in the figure below, that only the timing for the low-side switch, Q2, is used and not the high-side switch, Q1. This is done because the time that Q2 is on represents the time provided to refresh C_B, and the time that Q2 is off represents the amount of time for which C_B must provide charge to turn on Q1 as well as maintain the power supply for the high-side driver. By using this timing, we include any dead time used in the driver or built into the input signals.

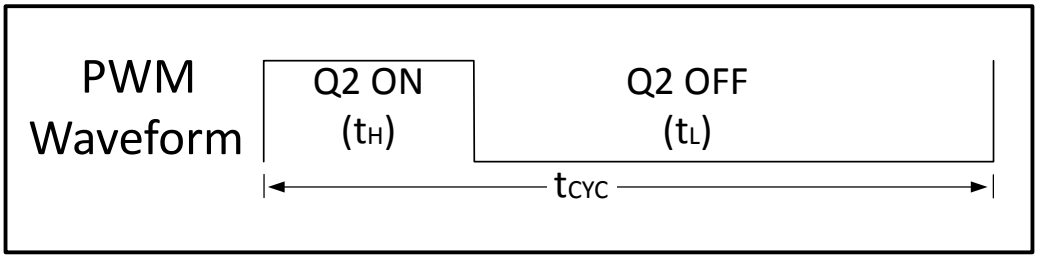


Figure 1.4. Q2 Timing Definition

1.2 Design Procedure

The design begins with the calculation of the minimum and maximum off time, and the minimum on time of the low-side MOSFET, Q2. This will allow the programmed dead time to be incorporated into the calculations as described in Figure 1.4 Q2 Timing Definition on page 4.

Because the dead time is implemented in the driver as a delay between the falling edge of one channel and the rising edge of the other channel, the on time of Q2 can be derived as follows:

$$T_H = \frac{(1 - D)}{F_{SW}} - T_{DT}$$

Where:

T_H is the on time of Q2.

D is the duty cycle of the input signal.

F_{SW} is the switching frequency.

T_{DT} is the dead time.

The on time, t_H, is minimized when the duty cycle, D, is at its maximum value:

$$T_{Hmin} = \frac{(1 - D_{max})}{F_{sw}} - t_{DT}$$

Where:

T_{Hmin} is the minimum time Q2 is on.

D_{max} is the maximum duty cycle in the application.

Equation 1.

Similarly, the off time, T_L, is given by:

$$T_L = \frac{D}{F_{sw}} + t_{DT}$$

For which the maximum and minimum are given by:

$$T_{Lmax} = \frac{D}{F_{sw}} + t_{DT}$$

Equation 2.

$$T_{Lmin} = \frac{D_{min}}{F_{sw}} + t_{DT}$$

Equation 3.

Next, the total charge (QCB) that must be delivered by the boot strap capacitor, CB, at maximum duty cycle (maximum Q2 off time) is found. There are two primary components of this charge: VDDA supply bias current IB and Q1 gate charge QG. Other sources of leakage, such as Q1 gate and D1 leakage, are negligible in comparison and are assumed to be zero.

Q_{CB} is calculated using Equation 4:

$$Q_{CB} = Q_G + (t_{Lmax} \times I_B)$$

Where:

Q_G is the total gate charge for Q1.

t_{Lmax} is the maximum amount of time during each cycle that Q2 is off (see Figure 1.4 Q2 Timing Definition on page 4).

I_B is the maximum quiescent supply current for the high side driver (see driver datasheet).

Equation 4.

The value of C_B is driven by the maximum allowable ripple (ΔV_{CB}) and calculated using Equation 5.

$$C_B \geq \frac{Q_{CB}}{\Delta V_{CB}}$$

Equation 5.

With a known value for C_B, the value of bootstrap resistor R_B can now be calculated. The purpose of R_B is to limit inrush current in the first cycle at startup. It can also be used to protect the isolation barrier in case of a catastrophic failure of the driver die. The idea is to select a resistor of high enough value to provide some current limit in startup conditions, and in case of driver failure, without being too large to prevent C_B from being properly refreshed during the worst case Q2 on time.

The combination of R_B and C_B form an RC circuit that has a time constant of R_B x C_B. As a starting point, it is suggested that resistor RB be selected such that tHmin is at least three times R_B x C_B.

With this information, R_B can be calculated using Equation 3.

$$R_B \leq \frac{t_{Hmin}}{3 \times C_B}$$

Where t_{Hmin} is the minimum time Q2 will be turned on in the application.

Equation 6.

The amount of charge, Q_{CB}, needs to be transferred into C_B during the minimum low-side on time, t_{HMIN}. This equates to a maximum average current during t_{LMIN}.

$$Iavg = \frac{Q_{CB}}{t_{Hmin}}$$

Equation 7.

This current represents the current through the boot strap diode during each charging cycle in the steady state. However, the peak current through the diode will happen during startup conditions when the capacitor CB is initially completely discharged. This is given by:

$$Ipk = \frac{V_{DD} - V_D}{R_B}$$

Where V_D is the diode forward voltage drop.

Equation 8.

The diode chosen must be able to handle the maximum average current given by Equation 7 as well as the peak current from Equation 8 for short periods of time during startup conditions.

In addition to the forward current ratings, the maximum repetitive reverse voltage specification of the boot strap diode must be at least as high as the high-side MOSFET drain voltage minus the low-side MOSFET source voltage. Also, the diode must be able to switch from conducting forward current to blocking reverse current sufficiently fast to prevent excessive reverse current from flowing into the driver power supply and causing damage. Furthermore, the diode reverse leakage current must be sufficiently low at all operating temperatures to prevent the same issue.

1.3 Design Example

For this example, we will use the following values as given for the application:

- High-side MOSFET Q_G = 85 nC
- Diode D1 V_F = 0.7 V
- V_{DDA} input = 12 V
- I_B = 3 mA (Output supply quiescent current from datasheet)
- F_{SW} = 200 kHz, D = 10% to 90%
- Programmed dead time, t_{DT} = 100 nsec

The design begins with the calculation of the maximum and minimum off time, and the minimum on time of the low-side MOSFET, Q2.

Using Equations 1, 2 and 3, we get:

$$T_{Hmin} = \frac{(1 - 0.9)}{200kHz} - 100ns$$

$$T_{Hmin} = 0.4\mu s$$

$$T_{Lmax} = \frac{0.9}{200kHz} + 100ns$$

$$T_{Lmax} = 4.6\mu s$$

$$T_{Lmin} = \frac{0.1}{200kHz} + 100ns$$

$$T_{Lmin} = 0.6\mu s$$

Next, calculate the total charge (QCB) that must be delivered by C_B at maximum duty cycle. There are two primary components of this charge: VDDA supply bias current IB and Q1 gate charge Q_G. Other sources of leakage, such as Q1 gate and D1 leakage, are negligible in comparison and are assumed to be zero.

From Equation 4, we get:

$$Q_{CB} = 85nC + (4.6\mu s \times 3mA)$$

$$Q_{CB} = 98.8nC$$

This means C_B must supply a total of 98.8 nC of charge during the high-side drive cycle.

The value of C_B is driven by the maximum allowable ripple (ΔV_{CB}), and calculated using Equation 5. In this design, ΔV_{CB} is chosen to be 5% of VDD.

$$C_B \geq \frac{98.8nC}{12 \times .05}$$

$$C_B \geq 164.7nF$$

Use the closest standard value of 180 nF.

Now calculate the value of resistor R_B using Equation 6.

$$R_B \leq \frac{0.4\mu s}{3 \times 180nF}$$

$$R_B \leq 0.74\Omega$$

Using 0.75 Ω will be sufficient.

In this design, 98.8 nC of charge must be transferred into CB within the minimum low-side on time t_{HMIN}. Equation 7 calculates the current required to meet this criterion:

$$I_{avg} = \frac{98.8nC}{0.4\mu s}$$

$$I_{avg} = 247mA$$

From Equation 7, a maximum average current of 247 mA is required to fully refresh C_B at maximum duty cycle time. However, the peak current during startup conditions is given by Equation 8:

$$Ipk = \frac{12 - 0.7}{0.75\Omega}$$

$$I_{pk} = 15A$$

The diode chosen must be able to handle the maximum average current given by Equation 7 as well as the peak current from Equation 8 for short periods of time during startup conditions.

In addition to the forward current ratings, the maximum repetitive reverse voltage specification of the boot strap diode must be at least as high as the full high-side MOSFET drain voltage.

Also, the diode must be able to switch from conducting forward current to blocking reverse current sufficiently fast to prevent excessive reverse current from flowing into the driver power supply and causing damage. Many MOSFET specifications include information on how fast the transistor's drain-to-source voltage, VDS, will drop once the gate has been charged. In addition, there will be a turn on delay time indicating how fast the VDS will start dropping once the gate-to-source voltage, VGS, begins rising. The sum of these two numbers can be used to approximate when the ground reference of the high-side driver will reach the high-side drain voltage. The reverse recovery time of the boot strap diode should be lower than this turn on time of the high-side MOSFET.

Furthermore, the diode reverse leakage current must be sufficiently low at all operating temperatures to prevent the same issue.

2. Layout Considerations

Good layout is important in high-side bootstrap design. C_B should be located as close to the driver IC pins as possible. A tantalum or ceramic capacitor (preferably ceramic) can be used for C_B as they provide low leakage and low ESR. If an electrolytic capacitor is used for C_B, it is recommended that a small, low-ESR decoupling capacitor be added in parallel with the electrolytic, as shown in the following figure.

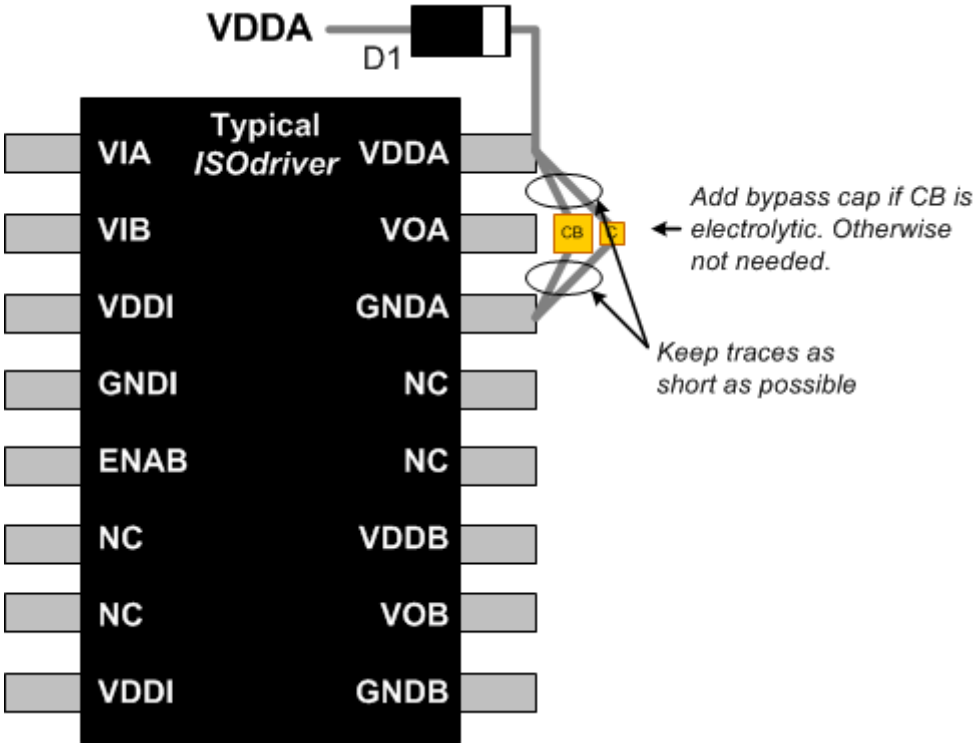


Figure 2.1. Bootstrap Layout Guidelines

3. Conclusion

Proper attention to bootstrap component selection and PCB layout are critical to ensuring reliable, high-performance isolated gate driver circuits.

To assist customers in performing some of these calculations, a boot strap calculation tool is available on the Silicon Labs website at https://www.silabs.com/support/isolation-bootstrap-calculator.

4. Revision History

Revision 0.3

January, 2020

- Modified text and equations to be more descriptive and accurate.
- Corrected minor errors in figures.
- Added hyperlink to the online boot strap calculator.

Revision 0.2

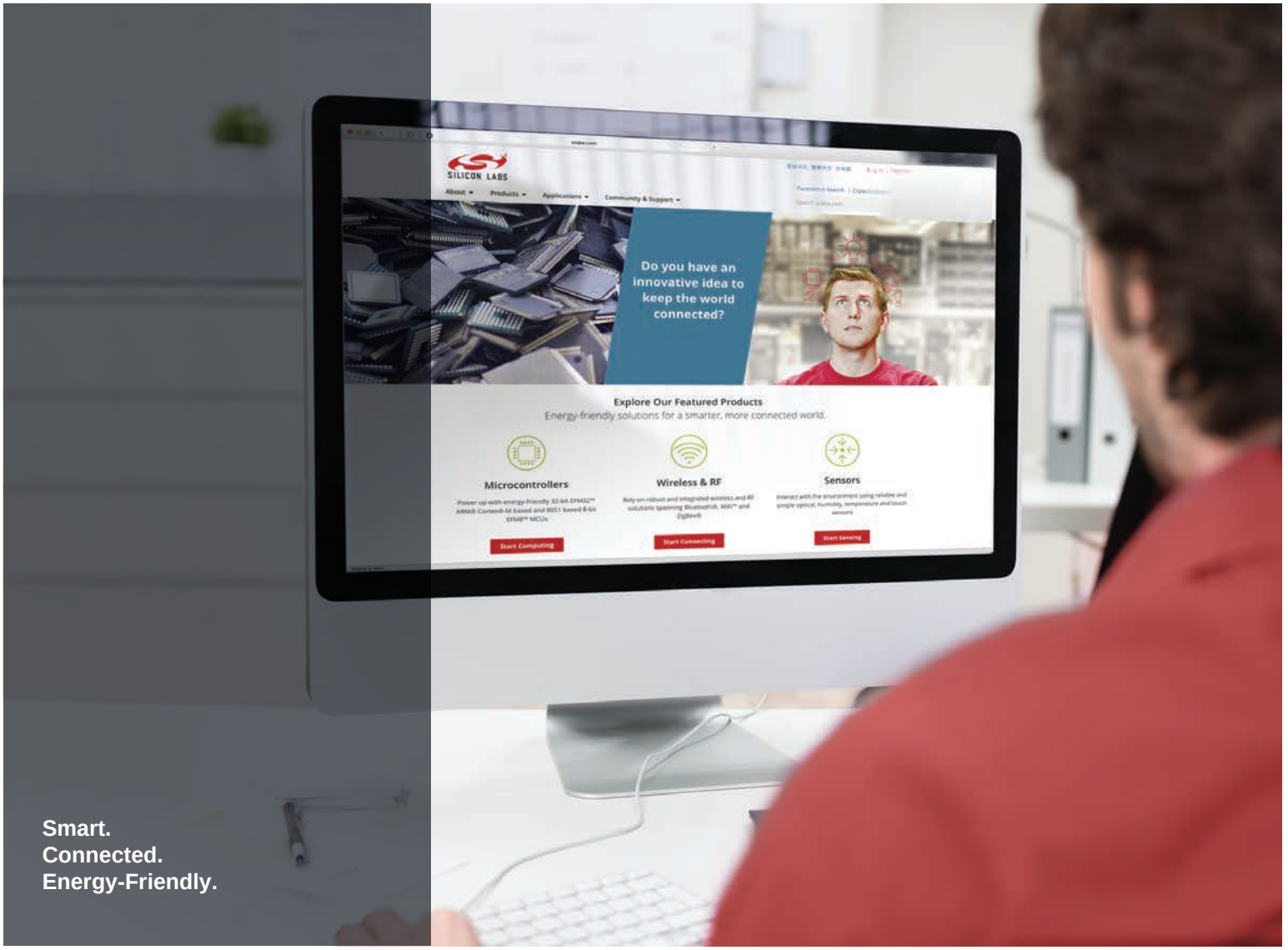
September, 2015

- Removed references to Si823x throughout.

Revision 0.1

March, 2010

- Initial release.



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