MP-IO MC6821 PIA and MC6850 ACIA I/O

The MP-IO Printed Circuit Assembly (PCA) incorporates the two most popular MC6800 family peripheral chips, the MC6821 Peripheral Interface Adapter (PIA) and the MC6850 Asynchronous Communications Interface Adapter (ACIA).
Many 6800 evaluation boards and kits used either or both for a user interface to allow engineers and enthusiasts to enter, run and debug programs.
The PCA is also able to be used as a SWTPC MP-S and, with a little additional logic, as a MP-C.
It is designed to plug into a 68retro MP style microprocessor PCA but can also be used in a SS50-100 bus motherboard.

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1. I/O ADDRESSING

I/O address decoding allows for either 8, 4 address chip selects or 8, 16 address chip selects to make it compatible with SWTPC I/O addressing.

Use the A,B,C jumpers to select either A2,A3, and A4 to be decoded for four address chip selects or A4,A5 and A6 for sixteen address chip selects according to the tables below.

The PIA chip select connects to the top row of the jumper block (J3) and the ACIA chip select connects to the bottom row. In the middle row are the outputs from the 3 to 8-line decoder IC2. Connect the top or bottom row to the middle row to select the I/O address for the PIA or ACIA according to the J3 column in the tables below.

As each output of the decoder is connected to the middle row of the jumper block it can only be connected to one jumper, preventing the two I/O devices from being selected at the same addresses.

J3	C = A4	B = A3	A = A2	Range
0	0	0	0	$00 - $03
1	0	0	1	$04 - $07
2	0	1	0	$08 - $0B
3	0	1	1	$0C - $0F
4	1	0	0	$10 - $13
5	1	0	1	$14 - $17
6	1	1	0	$18 - $1B
7	1	1	1	$1C –$1F

Four address chip selects

J3	C = A6	B = A5	A = A4	Range
0	0	0	0	$00 - $0F
1	0	0	1	$10 - $1F
2	0	1	0	$20 - $2F
3	0	1	1	$30 - $3F
4	1	0	0	$40 - $4F
5	1	0	1	$50 - $5F
6	1	1	0	$60 - $6F
7	1	1	1	$70 –$7F

16 address chip selects

2. MC6821 PIA INTERRUPT JUMPERS

MC6800 peripheral IC's use an open collector output on the IRQ pin so that they can be wired together in a 'Wired OR' configuration to the microprocessor IRQ pin.

The PA and PB straps allow both the Port A IRQ and the Port B IRQ to be separately connected to either IRQ or NMI or connected to both depending on the how the software handles the PIA interrupts if used.

3. MC6821 PIA REGISTER ADDRESS SWAP JUMPERS

The register swap jumpers allow you to change the ordering of the registers within the PIA. This makes it possible to read and write the output registers (PRA,PRB) with a 16-bit load or Store.
You might do this if you want to read or write all port pins at as close as possible to the same time.

A1 (RS1)	A0 (RS0)	
0	0	PRA
0	1	DDRA / CONTROL A
1	0	PRB
1	1	DDRB / CONTROL B

'Normal' connection.

A1 (RS0)	A0 (RS1)	
0	0	PRA
0	1	PRB
1	0	DDRA / CONTROL A
1	1	DDRB / CONTROL B

'Swapped' connection.

4. MC6821 PIA OUTPUT CONNECTORS

CN1 is a single-in-line 24 pin header with all of the port pins,+5V and GND. CN1 is for making connections via Dupont connectors or for plugging in a small IO board.
CN2 is a 26-way IDC connector and has all the port pins, +5V and GND, /NMI and /RESET.
This connector is a more convenient way to use the PIA pins on a larger board, perhaps a keyboard and display like many early 6800 evaluation kits.

5. MC6850 ACIA

The ACIA on this board will primarily be used to connect to a terminal, well a PC running a terminal program perhaps.
The PCB has been designed to take a FTDI style TTL to USB converter which also passes through 5V power so is a convenient way to connect to the board. Of course you can use a MAX232 style connection to a RS232 port on your 'Terminal' as well, many adapters are available.

Apart from being able to supply 5V power the FTDI style USB converter has another major advantage, the use of non-standard Baud rates.
When the driver for the FTDI converter is asked to open a port it will attempt to configure the FTDI chip to the Baud rate requested by the application, adjusting the clock divider to match the Baud requested.
For example, for a MC6802 with a 4MHz crystal the E clock is (divide by four) 1MHz.
Typically the MC6850 ACIA is configured for a divide by 16 clock making the Baud rate;
1MHz / 16 = 62500.
Most terminal software like Teraterm, allows the entry of non-standard Baud rates.
The caveat is that most old monitor software polls the ACIA for a character and so will have a maximum Baud rate that can be successfully received.

6. MC6850 ACIA MODEM CONTROL SIGNALS

For correct operation the modem control input signals /DCD and /CTS are pulled low, both these inputs and the /RTS output are available via pads for experiments with hardware handshaking. There are also pads for the FTDI DTR and CTS signals.
Resistors are in-line with the TX and RX signals to try to prevent leakage from the potentially powered FTDI adapter into the rest of the unpowered circuit. Be aware that +5V power can still be available from a PC USB port when the PC is off.

7. MC6850 BAUD RATE GENERATOR

The Baud Rate Generator is constructed around a 74HC4060 Ripple Carry Binary Counter.
The input of the IC is configured as a crystal oscillator and the binary counter divides the oscillator down into usable frequencies for use by the MC6850 as Baud rate clocks.
Internally the MC6850 can also divide the applied RX CLK and TX CLK by 16 or 64, selectable with the 'Counter Divide Select Bits (CR1 and CR0) in the Control Register. Most software configures this divider as 'divide by 16'.

The clock divisor jumper block, J12, is used to select the (16x) Baud rate clock according to the following table.

Jumper		**Tx,Rx Clock**	**Baud Rate (CR0,CR1 = /16)**
E	Microprocessor E clock	1 MHz	62500
X	74HC4060 Oscillator	2.4576 MHz	153600
4	Oscillator divided by16	153.6 kHz	9600
5	Oscillator divided by 32	76.8 kHz	4800
6	Oscillator divided by 64	38.4 kHz	2400
7	Oscillator divided by 128	19.2 kHz	1200
8	Oscillator divided by 256	9.6 kHz	600
9	Oscillator divided by 512	4.8 kHz	300
10	Oscillator divided by 1024	2.4 kHz	150

Clock Divider Jumper Block

8. POWER

The MP-IO PCA has a jumper for +5V power to be connected via a jack or via the TTL to USB to Serial adapter. The MP-IO PCA supplies power to the connected Microprocessor PCA via the SS50-100 bus connector.
Most USB to TTL Serial adapters route the USB power through to the output connector and so can provide, usually USB version 2 power, 5V at 500mA.
Note that there is no power supply protection against reverse polarity or excess current on the PCB.

Figure 1. FULL I/O ADDRESSING
The SS50-100 Bus I/O signal provides the top 8 bits of the I/O address.

I/O ADDRESS RANGE – (8 X 4 I/O PORTS)

				C	**B**	**A**	RS1	RS0	
J3	A7	A6	A5	**A4**	**A3**	**A2**	A1	A0	RANGE
CS0	0	X	X	0	0	0	-	-	$00-$03
CS1	0	X	X	0	0	1	-	-	$04-$07
CS2	0	X	X	0	1	0	-	-	$08-$0B
CS3	0	X	X	0	1	1	-	-	$0C-$0E
CS4	0	X	X	1	0	0	-	-	$10-$13
CS5	0	X	X	1	0	1	-	-	$14-$17
CS6	0	X	X	1	1	0	-	-	$18-$1B
CS7	0	X	X	1	1	1	-	-	$1C-$1F

I/O ADDRESS RANGE – (8 X 16 I/O PORTS)

		C	**B**	**A**	RS3	RS2	RS1	RS0	
J3	A7	**A6**	**A5**	**A4**	A3	A2	A1	A0	RANGE
CS0	0	0	0	0	-	-	-	-	$00-$0F
CS1	0	0	0	1	-	-	-	-	$10-$1F
CS2	0	0	1	0	-	-	-	-	$20-$2F
CS3	0	0	1	1	-	-	-	-	$30-$3F
CS4	0	1	0	0	-	-	-	-	$40-$4F
CS5	0	1	0	1	-	-	-	-	$50-$5F
CS6	0	1	1	0	-	-	-	-	$60-$6F
CS7	0	1	1	1	-	-	-	-	$70-$7F