68retro MP-02 6802 Microprocessor Board

FEATURES

- Powerful 1,1.5 or 2 MHz Motorola MC6802 Microprocessor.
- DIP Switch programmable shared 64k memory map for ROM and RAM.
- DIP Switch programmable I/O addressing.
- Expandable, Breadboard Friendly, modified SS50 Bus (SS50-100).
- Up to 56k of RAM.
- Supports a single JEDEC JESD21-C 0.6" Wide 2k / 4k / 8k / 32k x 8 (E)EPROM.
- Supports a single JEDEC JESD21-C 0.6" Wide 2k / 8k / 32k / 128k/ 512k x 8 SRAM.
  or a JEDEC JESD21-C 0.3" Wide 64k x 8 SRAM.
- Less than half the size of a regular SS50 card.
- 5V only operation.

The MP-02 MC6802 Microprocessor board hardware originates from the SWTPC 6800 computer and the SS50 bus.

The unique banked addressing scheme provides a high level of flexibility, allowing existing code to be accommodated without modification at the address where it originally ran.

Similarly, I/O paging allows memory mapped I/O to be set anywhere across the memory map via a DIP switch, overlaying the ROM and RAM so you lose the minimum amount of address space to I/O.

The 50 way SS50 bus connection, re-imagined with a spacing of 0.1", is perfect for expansion and hacking with solderless breadboard and stripboard. Small changes to the bus itself, like making it 5V, make the SS50-100 bus simpler to use.

CONTENTS

1. MICROPROCESSOR

The MC6802 microprocessor is software compatible with the MC6800 but includes an on-chip clock oscillator and 128 bytes of on-chip RAM, 32 bytes of which can be retained by a backup supply.
To accommodate the new features of the MC6802 the DMA capability of the MC6800 was removed.

Available in three speed grades, 1 MHz (MC6802), 1.5 MHz (MC68A02) and 2 MHz (MC68B02) and commonly available in the P suffix, Plastic package or the less common L suffix, Ceramic package.
There were many second source manufacturers so you may find it without the familiar MC prefix.

The 128 Bytes of RAM included on the IC is addressed from $0000 to $007F and is disabled by default on the MP-02 PCA, strapping pins 1 and 2 together on the RE jumper will enable the RAM.

2. OSCILLATOR

The crystal footprint has been designed for the HC49 case style and has provision for a wire to hold the crystal down against the PCB. A lower profile HC49/U crystal can be used but needs to be installed off the board a little to avoid the possibility of the case of the crystal shorting out the crystal pins by contacting the top layer pads.

In some ‘modern’ minimal retro systems the microprocessor crystal oscillator is also used as the serial Baud clock. The MP-02 PCA does not make the microprocessor crystal output available on the SS50-100 Bus but the E clock is available for use as a Baud rate clock.

A table of common microprocessor crystals and E clock frequencies is presented below.

MPU Crystal (X1)	Load Capacitors (C2,C3)	E Clock
3.6864 MHz	27 pF	921.6 KHz
3.58 MHz	27 pF	895.0 KHz
4 MHz	27 pF	1 MHz
6 MHz	20 pF	1.5 MHz
7.3728 MHz	18 pF	1.8432 MHz
8 MHz	18 pF	2 MHz

Crystal, E clock and loading capacitors.

3. RESET CIRCUIT

The reset circuit can either be a RC (R2,C1) time constant or a DS1233-5 5V EconoReset IC.
The DS1233 is recommended but if you don’t use it then the capacitor C1 should be increased to 1uF for an adequate reset.

4. MEMORY DEVICES - ROM

The 28 pin ROM footprint can accept (E)EPROM devices from 2k x 8 Bytes to 32k x 8 Bytes using three jumpers J2, J3 and J4 as presented in the table below.

Device	J2	J3	J4
2k x 8 EPROM	NC	1-2	1-2
2k x 8 EEPROM	NC	1-2	1-2
4k x 8 EPROM	NC	1-2	2-3
8k x 8 EPROM	1-2	NC	2-3
8k x 8 EEPROM	NC	NC	2-3
32k x 8 EPROM	1-2	2-3	2-3
32k x 8 EEPROM	2-3	2-3	2-3

ROM Strap Settings (NC = no strap connection)

5. MEMORY DEVICES - RAM

The 32 pin RAM footprint can accept SRAM devices from 2k x 8 Bytes to 512k x 8 Bytes using three jumpers J5, J6 and J7 as presented in the table below.
The MC6802 can only address 64k Bytes so the higher capacity devices can only be addressed up to 64k. The larger devices (> 64k Bytes) are included to help with parts procurement.

Device	J5	J6	J7
2k x 8	1-2	1-2	1-2
8k x 8	2-3	1-2	1-2
32k x 8	2-3	2-3	2-3
64k x 8 (300mil)	2-3	2-3	2-3
128k x 8	2-3	2-3	2-3
512k x 8	2-3	2-3	2-3

RAM Strap Settings

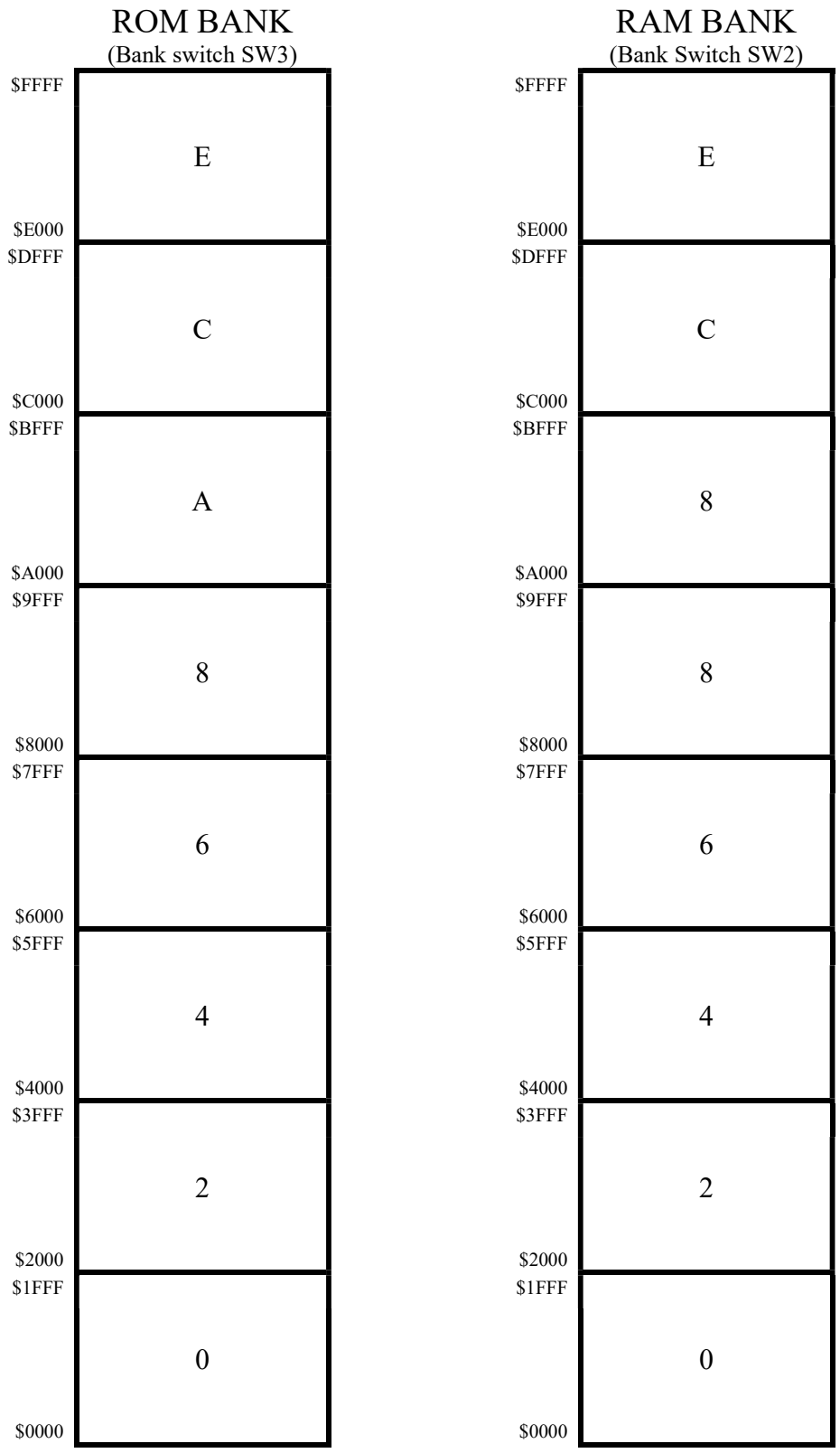
6. SS50-100 BUS

The SS50 bus has been changed to make it a little easier to use.
The original SS50 bus uses 0.156” pitch Molex connectors, by reducing the pitch of the connector to 0.1” the bus can be used with a variety of commonly available connectors, solderless breadboard and the similar Molex 0.1” connector.

The unregulated 7-8V DC power rail has been replaced with a single +5V DC power rail.
Compatibility with future processor cards and increased memory addressing has also been catered for with the removal of the baud rate oscillator outputs on the bus.

Finally, due to the reduced width of the bus connector, the board size has been reduced by more than 50% compared to a regular SS50 Bus printed circuit board.

Figure 1. 68retro MP-02 MEMORY MAP



Memory Mapped I/O

I/O Page (SW4) Upper I/O Address								Lower I/O Address							
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
$01 - $FE*								$00 - $FF Decoded on I/O boards							

* See Text.

7. BANK ADDRESS DECODING

The complete 64k memory map is decoded into 8, 8k x 8 Byte banks. Both RAM (DIP switch 2) or ROM (DIP switch 3) can be switched in and out of all banks.
The single memory device can be switched to appear in more than one bank and smaller devices, less than 8k, have aliases through the rest of the 8k bank.

Switch the DIP switch to the ON position to enable the RAM or ROM for each 8k bank and make sure you don't enable both RAM and ROM on the same bank!
If the 128 Byte internal MC6802 RAM is enabled there can be no other memory devices enabled in bank 0.

8. MEMORY MAPPED I/O PAGE DECODING

The Magnitude Comparator (IC8) 74xx688 compares for equality the valid upper byte of the address bus with the I/O PAGE DIP switch setting (SW4). The output active when an address match occurs.

This output is active for all the addresses where the upper byte matches the DIP switch giving a 256 byte I/O address space that can be set to any page in the whole memory map.

The I/O output is provided on the SS-50-100 bus in true and inverted form for additional I/O decoding on other attached boards.
The I/O output also disables the chip selection of both the RAM and the ROM to ensure that neither is enabled during an I/O cycle. In this way only 256 bytes of memory is lost in the whole 64k address space for memory mapped I/O.

Since the ROM and RAM devices are disabled by the I/O the top page ($FF) should not be used as the reset and interrupt vectors are located there.
Similarly if you want to use the direct addressing mode of the MC6802 or the internal RAM is enabled then using the bottom page ($00) should also be avoided.

Figure 2. ROM and RAM Strap settings

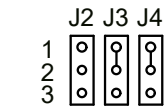
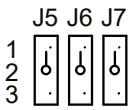
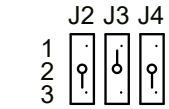
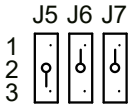
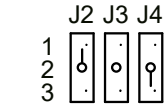
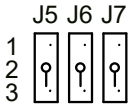
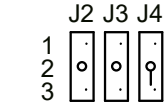
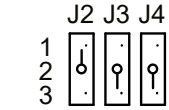
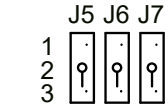
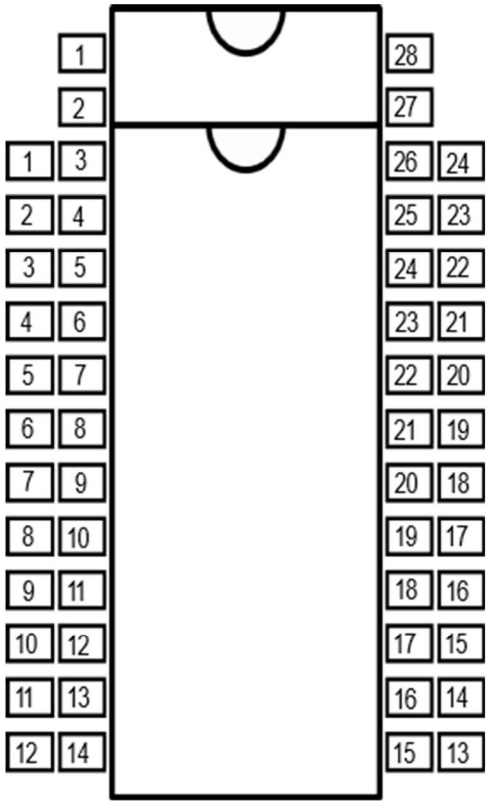
Jumpers	ROM Device	Jumpers	SRAM Device
	2k x 8 EPROM EEPROM		2k x 8
	4k x 8 EPROM		8k x 8
	8k x 8 EPROM		32k x 8
	8k x 8 EEPROM		64k x 8
	32k x 8 EPROM		128k x 8
	32k x 8 EEPROM		512k x 8

Figure 3. EPROM / EEPROM PINOUTS JEDEC JESD21-C

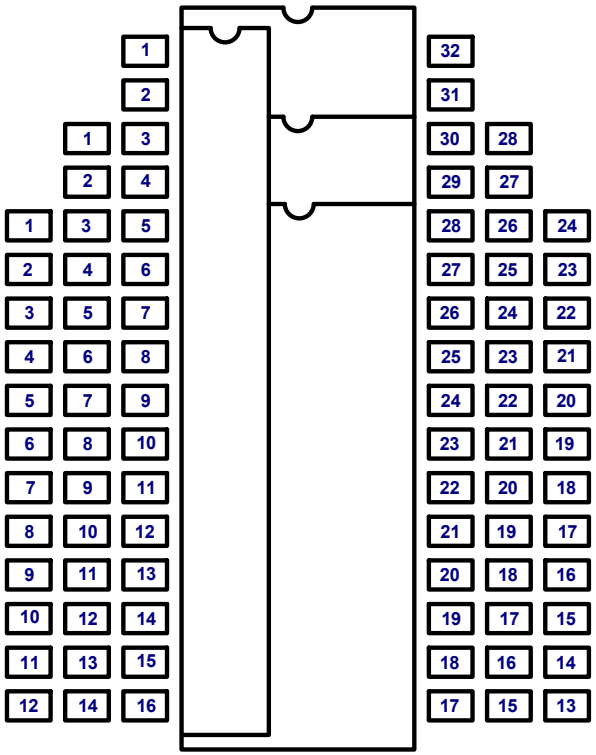
EEPROM	EPROM	EEPROM	EPROM	EPROM	EEPROM	EPROM
28C256	27256	28C64	2764	2732	28C16	2716
A14	VPP	NC	VPP			
A12	A12	A12	A12			
A7	A7	A7	A7	A7	A7	A7
A6	A6	A6	A6	A6	A6	A6
A5	A5	A5	A5	A5	A5	A5
A4	A4	A4	A4	A4	A4	A4
A3	A3	A3	A3	A3	A3	A3
A2	A2	A2	A2	A2	A2	A2
A1	A1	A1	A1	A1	A1	A1
A0	A0	A0	A0	A0	A0	A0
D0	D0	D0	D0	D0	D0	D0
D1	D1	D1	D1	D1	D1	D1
D2	D2	D2	D2	D2	D2	D2
GND	GND	GND	GND	GND	GND	GND



EPROM	EEPROM	EPROM	EPROM	EEPROM	EPROM	EEPROM
2716	28C16	2732	2764	28C64	27256	28C256
			VCC	VCC	VCC	VCC
			PGM	$\overline{WE}$	A14	$\overline{WE}$
VCC	VCC	VCC	NC	NC	A13	A13
A8	A8	A8	A8	A8	A8	A8
A9	A9	A9	A9	A9	A9	A9
VPP	$\overline{WE}$	A11	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$/VPP	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A10	A10	A10	A10	A10	A10	A10
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
D7	D7	D7	D7	D7	D7	D7
D6	D6	D6	D6	D6	D6	D6
D5	D5	D5	D5	D5	D5	D5
D4	D4	D4	D4	D4	D4	D4
D3	D3	D3	D3	D3	D3	D3

Figure 4. SRAM PINOUTS JEDEC JESD21-C

512k x 8	128k x 8	64k x 8	32k x 8	8k x 8	2k x 8
A18	NC	NC			
A16	A16	NC			
A14	A14	A14	A14	NC	
A12	A12	A12	A12	A12	
A7	A7	A7	A7	A7	A7
A6	A6	A6	A6	A6	A6
A5	A5	A5	A5	A5	A5
A4	A4	A4	A4	A4	A4
A3	A3	A3	A3	A3	A3
A2	A2	A2	A2	A2	A2
A1	A1	A1	A1	A1	A1
A0	A0	A0	A0	A0	A0
D0	D0	D0	D0	D0	D0
D1	D1	D1	D1	D1	D1
D2	D2	D2	D2	D2	D2
GND	GND	GND	GND	GND	GND



2k x 8	8k x 8	32k x 8	64k x 8	128k x 8	512k x 8
			VCC	VCC	VCC
			A15	A15	A15
	VCC	VCC	CE2	CS2	A17
	$\overline{WE}$	$\overline{WE}$	$\overline{WE}$	$\overline{WE}$	$\overline{WE}$
VCC	CS2	A13	A13	A13	A13
A8	A8	A8	A8	A8	A8
A9	A9	A9	A9	A9	A9
$\overline{WE}$	A11	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A10	A10	A10	A10	A10	A10
$\overline{CE}$	$\overline{CS1}$	$\overline{CE}$	$\overline{CE1}$	$\overline{CS1}$	$\overline{CE}$
D7	D7	D7	D7	D7	D7
D6	D6	D6	D6	D6	D6
D5	D5	D5	D5	D5	D5
D4	D4	D4	D4	D4	D4
D3	D3	D3	D3	D3	D3